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MARCH 1986 95p

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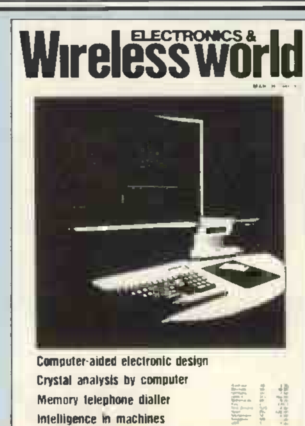
FEATURES

REGULARS



Cover picture is the Daisy Systems Personal Logician, a c.a.d. system for application-specific i.cs. Further details in our c.a.d. feature, starting on p.35.

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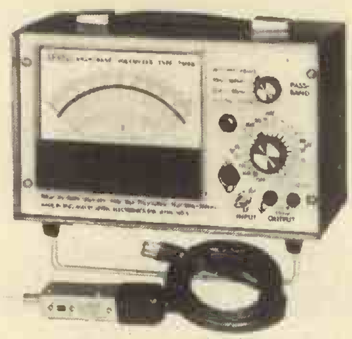

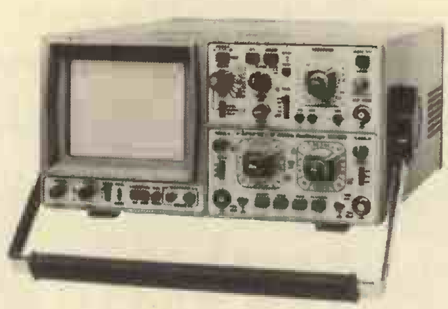

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74LS25	.27	.25	8155	1.50	1.30	27256	4.20	3.60
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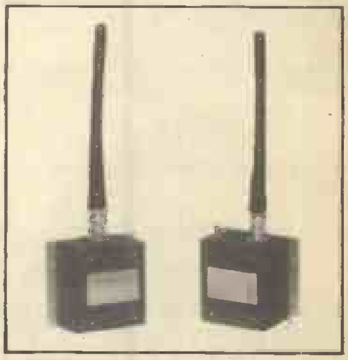

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CIRCLE 23 FOR FURTHER DETAILS.

Acorn's new Beeb

Acorn Computers have at last announced the latest version of the BBC Micro, called the Master series. Over the years since the Model B was launched, there have been a number of additions both from Acorn and from third party manufacturers; extra memory, better disc interfaces, rom expansions, word processors, graphics extensions, second processors and so on.

The new series incorporates many of these upgrades in the basic model, the Master 128 which is still recognisable as being an enhanced Model B.

Master 128

Externally it is wider to accommodate an extra numerical keypad and the top cover has been made deeper to allow space for plug-in expansions.

Internally it has a lot more memory: 128K of ram which is divided between main ram and paged 'sideways' ram. It also has 128K of rom in one i.c. nicknamed the Megarom. This contains the operating system which has been enhanced to include extended graphics facilities and terminal software: BBC Basic (version 4) which includes extra commands to take advantage of the other enhancements; an Edit rom which is used as a Basic program and text editor, the View wordprocessor and Viewsheet spreadsheet program and two disc filing systems. The DFS ensures some compatibility with software developed on the Model B; and the ADFS which is a double-density system with, at last, an unlimited number of files. To make this possible Acorn have devised an hierarchical system with file directories nested within files.

There is space for four additional roms inside the computer and it is possible to have three other 128K roms or even two 256Kbyte roms. This has limited application because such monster roms have to be programmed and be made available. However there are also two external cartridge rom sockets which offer the 1MHz bus of the Model B, uprated to 2MHz. Through these not only can rom firmware be plugged in but also sound input/output with such peripherals as the Music 500, and, for example, a video genlock. Each cartridge socket has a capacity of 256Kbyte.

Another addition is the provision of a battery-backed real-time clock and some ram which is reserved for the start-up options so that the computer will automatically switch itself into the wordprocessor mode, for example, if needed.

The display modes are similar to those of the Model B, though the additional ram means that 'shadow' modes do not take any ram from the user. Similarly there is no extra ram required for the filing systems. The rest of the specification duplicates the facilities of the Model B: The same video outputs are provided; modulated u.h.f, composite video and RGB. It uses the same sound chip and internal loudspeaker though an audio socket has been added to drive an external loudspeaker or amplifier. Also duplicated are the user port, the 1MHz bus, the Tube for connecting external second processors, analogue input and cassette interface. Software is provided on a "Welcome" disc and tape which includes a suite of demonstration programs, assorted utilities including disc filing system utilities and Basic 128 — BBC Basic for use in sideways ram. The package is completed with a Welcome manual and reference cards for the firmware utilities. The Master 128 costs £499.

One feature we have omitted is the internal Tube bus and socket which enables the plugging in of additional processors and memory. These permit the expansion of the system and the expanded versions are also available as computers in their own right. There is no difference in price between buying the 128 and upgrading it or buying the enhanced versions of the computer.

Turbo

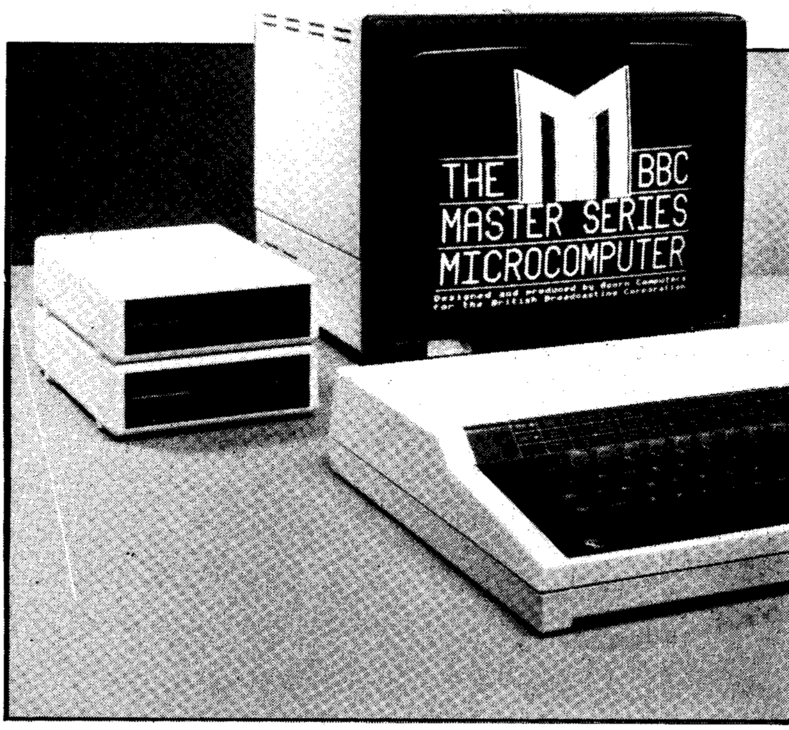
The first expansion adds to the 128 an additional 64C102 processor with a clock frequency of 4MHz, along with 64Kbyte of ram and 4Kbyte of rom, and a disc with a version of Basic for use with the system. It is designed for high-speed processing and is claimed to be faster than any other microcomputer for interpreted Basic. Turbo costs an additional £125.

Master 512

This adds a 16-bit 80186 processor, running at 8MHz and 512Kbyte of ram; up to 128K of rom. This is provided with Digital Research's DOS-plus which makes it compatible with MS-DOS and CP/M 86 and opens up a wide field of applications software. MS-DOS being almost identical to PC-DOS enables some software written fro the IBM-PC to be used. Also provided on disc is DR's GEM suite of utilities: GEM Desk Top, GEM Paint and GEM Write. The price of this addition is yet to be announced but is likely to be about £500, making the combined computer cost £1000.

Master Scientific

This adds the facilities of the Acorn Cambridge Workstation: 32-bit 32016 processor and a floating-point 32081 co-processor; 512K ram, 16K rom



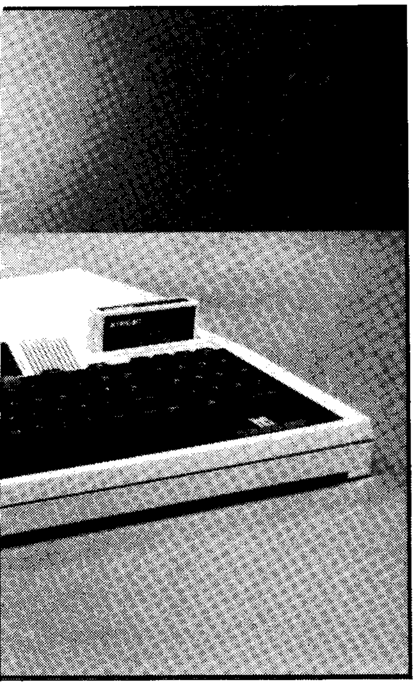
Poor job prospects

Job prospects in the electronics engineering field are poor for at least the first quarter of this year. Statistics have come from Manpower Ltd, who specialize in such surveys.

The decline in confidence now being shown by electronics manufacturers reflects the decline in confidence in all sectors of employment, according to Manpower. Their survey points out that this is the first time in five years that New-year prospects in Britain have failed to show an improvement over the previous year.

Fewer employers in electronics manufacturing are planning to increase their workforce and projected job cuts are higher than in the last quarter of 1985. The relative decline in job prospects in electronics is shown clearly by the 'balance' or difference between the proportion of employers increasing their staff and those cutting jobs. The balance now stands at +9, only barely positive, in contrast with +24 last quarter.

Manpower claims these results confirm its forecasts made in three prior surveys during 1985, that job prospects in Britain will increasingly "flatten" over the next 12 months. ■



plus the Acorn Pandora operating system core. On the accompanying disc comes the Panos operating system, Fortran 77, ISO Pascal, C, BBC Basic, the 32000 series macro-assembler and support software for the programming languages.

There is also a whole library of supporting manuals and operating guides. All for an extra £1500 (still to be officially announced) giving a total price of £2000.

Econet terminal

Acorn have not neglected their educational customers many of whom run networked Model Bs. The Master Econet Terminal leaves out some of the facilities of the Master 128 as these can be made available through the network. It uses the same processor and has the same quantity of ram as the 128. The rom is 64K and contains the operating system, BBC Basic, and in place of a disc filing system an advanced network filing system (ANFS).

This cut-down version of the Master series cost the same price as the old Model B; £399.

Acorns seems to have got its sums right this time. The BBC micro has established itself as a standard over the years but was beginning to look a little tired in contrast to some newer computers, many of whom tried to emulate the facilities on the BBC. This injection of new technology can revive its reputation. ■

Anglo-French super computer

The Esprit programme in Europe is helping the funding of a modular parallel-processing super-computer that will be capable of 500 million floating-point operations per second (megaflops) and yet will cost less than a tenth of a current computer with equivalent power.

The main contractor of the project is the Royal Signals and Radar Establishment, Malvern who will be working in collaboration with French companies: Telmat, Apsis and the Laboratoire de Genie Informatique: and in the UK with Southampton University and Thorn-EMI Inmos.

The modular computer will be constructed around 'nodes' with each node typically consisting of 16 floating-point transputers connected by a programmable switching network. The interconnection strategy will allow a variety of architecture types to be implemented: thus the machine could be re-configured for a wide range of applications. During the programme, high-level programming languages will be developed, together with diagnostic and support software, to allow both hardware and software debugging. Application software is to be developed for use in science and engineering, signal and image processing, image synthesis, computer-aided design and computer-aided management.

It is intended to demonstrate that the configurable super-node architecture can serve both as a powerful single-user workstation and, because of the expandability of the system, as the basis of a very large array of replicated nodes suitable for the most demanding of computer applications. ■

Euro-deal on ASICs

A "memorandum of understanding" has been signed by GEC and Thomson for the joint development of design and manufacturing tools for c-mos application-specific integrated circuits.

[Application-specific i.c. is, we feel, a much better description of the chips that up to now have been known as semi-custom i.cs. These are chips which are half-completed and need their individual cells to be wired up by a layer of interconnecting metal to define their function and purpose.]

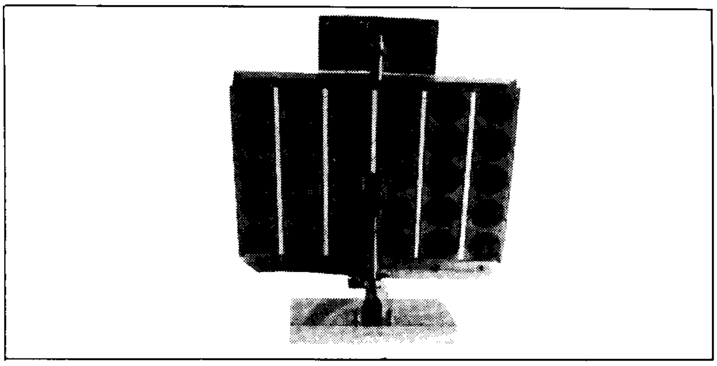
GEC, through Marconi Electronic Devices and Thomson, have agreed to develop a prototyping service which will improve and enhance the European a.s.i.c. capability; serve the rapidly increasing market for such circuits, particularly in data processing and telecommunications; and establish dual sources in Europe for such high-performance devices in 1.2μm, and later 0.8μm geometries.

The initial objective will be to establish a two-layer metal E-beam facility, leading to three layers by the end of the programme. A parallel objective is to further develop and combine the Macrocell design capabilities of the two companies. These cells are used as building blocks in the design of a.s.i.cs. These are to be combined into a family of semi-standard programmable building blocks or megachips. Design will be fully supported by c.a.d. tools available from both companies which are to be interchanged so that all the facilities are available from both.

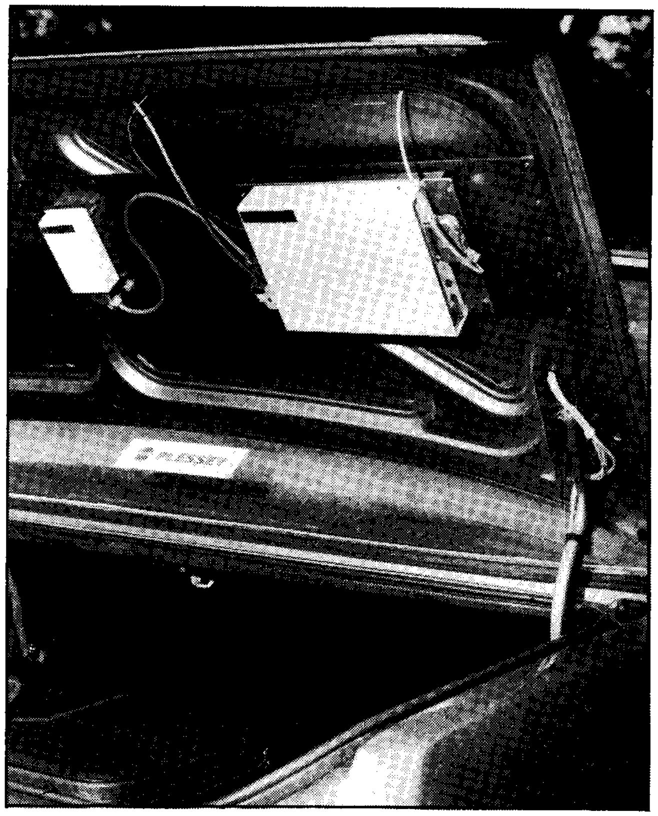
The medium-term objective is to use silicon compilation extensively to develop fast manufacturing techniques for full wafer production. Particular emphasis will be placed on ease of use for compilers which will allow the automatic compilation of megacells from behavioural descriptions. The system will also manage interconnection layout and test sequence definition of the circuit and interfaces with testers for E-beam debugging.

The program has been submitted to Eureka for partial funding. Other joint initiatives, including power semiconductors, are planned.

For further details of similar equipment see the c.a.d. feature in these pages. ■



This solar array automatically adjusts its position to gain the maximum power from the sun. It is fitted with two extra solar cells separated by an opaque screen which casts a shadow on one of the cells if the array is not aligned. The output voltage of the cells is compared; if one is stronger than the other then the differential voltage with the polarity of the stronger cell is used to drive a miniature d.c. motor/gearbox combination which moves the array until both cells are equally illuminated. This sytem is claimed to give about double the output of a fixed array. Picture from Portescap who provided the motor.



One PACE forward — an in-car pilot

From time to time in the last 25 years, attempts have been made to develop electronic equipment to help car drivers find their way about: the 'moving map' is one result of this effort. Most of the developments seen during this time have exhibited drawbacks caused by deficiencies in accelerometers or gyros.

Plessey Electronic Systems Research at Roke Manor has now announced PACE (Plessey Adaptive Compass Equipment) which, in demonstration in that locality, is extremely impressive in its performance.

Essentially, it consists of a fluxgate magnetometer, rotation sensors on two opposite wheels to provide distance, speed and turning information, a 6502-based processor and two kinds of display. To use the equipment, the driver enters the map references of starting point and destination. A map of the relevant road system appears on a small v.d.u. and an arrow continuously indicates the car's position, together with its current map reference and heading. Since it is illegal in the UK to have a display of this kind where the driver can see it, a second, l.c.d. panel shows map reference and heading and instructions such as 'left in 100m' or 'Bear right at fork'. Voice synthesis could be used instead of the display, and the data could be transmitted to a base receiver in the case of a taxi or a police car.

Small inaccuracies of the compass are reduced by the dead-reckoning mode of operation and by the fact that the software used enables the equipment to 'recognise' features such as road junctions, at which errors are corrected, if necessary. Calibration updating of the compass, which is affected by changes in the permanent field of the car, is carried out by software and is effective enough to correct the errors introduced by a complete reversal of the field: the wheel sensors interpolate while this is done. It is not necessary to locate the magnetometer in any specially selected part of the car, provided that the engine compartment is avoided.

Plessey expect to start production of PACE in 1988, following development of a v.l.s.i. chip-set, and the provision of world-wide digitized maps for incorporation into processor firmware. We hope to provide a detailed account of this development in a future issue. ■

PACE in place. The equipment shown here is in its development stage and consists of a portable micro, which would be replaced by something a great deal simpler and smaller, with the l.c.d. in the dashboard, and the v.d.u. map display. On the right is shown the mounting of the magnetometer (left) and processor.

Listening word-processor

One of the major projects in the Alvey advanced computer programme is a word-processor that can respond directly to the human voice. The prime contractor is Plessey and chairman Sir John Clark said: "We are now within sight of producing a form of direct user/machine communication that, in the next decade, will begin to replace keyboard control. The prospect for instantaneous voice-to-voice translation, and many other applications, are tremendous. We believe that we lead the world in this area — combining phonetic, linguistic and human engineering with the advanced principles arising from fifth-generation computer technology."

Plessey are collaborating with Edinburgh and Loughborough Universities and University College, London. The system is planned to accept and respond to normal speech. The spoken words will be displayed on a screen when they can be corrected or edited before printing. A virtually unlimited vocabulary will have several thousand words initially. As well as text preparation the system will be used with artificial-intelligence programs to provide translation or answer questions from a database.

The project will use the fifth-generation computer technology developed under the Alvey 'Flagship' project. ■

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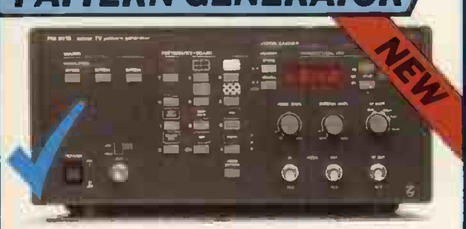

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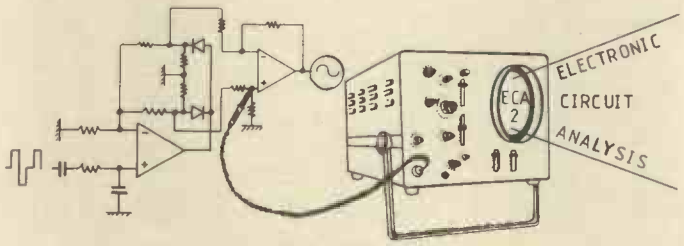

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MODEMS

MIRACLE WS 2000
The world standard BT approved modem covering all standard CCITT and BELL (outside UK only) standards upto 1200 baud. Allows communication with virtually any computer system in the world. Expandability to Auto Dial and Auto Answer with full software control enhance the considerable features already provided on the modem. Mains powered. WS 2000 **£125 (c)** Auto Dial Board/Auto Answer Board (awaiting BABT approved) **£30 (d)** Software Control Kit **£10 (d)**

NEW WS-3000 RANGE — the new professional series. All are intelligent and 'Hayes' compatible, allowing simply 'English' commands to control its many features. All models feature Auto-Dial with 10 number memory, Auto-Answer, Speed Buffering, printer port, data security option etc. All models are factory upgradeable.

WS3000 V2123 (V21 & V23 + Bell) **£295 (a)**
WS3000 V22 (as above plus 1200 baud full duplex) **£495 (a)**
WS3000 V22bis (as above plus 2400 baud full duplex) **£650 (a)**
The WS3000 range all have BT approval.

GEC DATACHAT 1223 £86(b)

SOFTY II

This low cost intelligent eprom programmer can program 2716, 2516, 2532, 2732, and with an adaptor, 2564 and 2764. Displays 512 byte page on TV — has a serial and parallel I/O routines. Can be used as an emulator, cassette interface.
Softy II ....£195.00 (b)
Adaptor for 2764/2564 ....£25.00

SPECIAL OFFER

2764-25 £2:00(d);
27128-25 £2:75(d);
6264 LP-15 £3:75(d);

ACORN IEEE INTERFACE £278(a)

INDUSTRIAL PROGRAMMER EP8000 £695 (a)

DISC DRIVES

PD800P (2 x 400K/2 x 640K 40/80T DS) with built in monitor stand....£254 (a)
PD800 (2 x 400K/2 x 640K 40/80T DS)....£224 (a)
TS400 1 x 400K/1 x 640K 40/80T DS....£99 (b)
PS400 with psu 1 x 400K/1 x 640K 40/80T DS....£120 (b)

SPECIAL OFFER

ACORN's Single Drive 1 x 100K/1 x 160K 40T SS £49 (b)

3.5" DRIVES
1 x 400K/1 x 640K 80T DS
TS35 1....£99 (b) PS35 1 with psu....£119 (b)
2 x 400K/1 x 640K 80T DS
TS35 2....£174 (b) PS35 2 with psu....£189 (b)

3M FLOPPY DISCS

Industry Standard floppy discs with a lifetime guarantee Discs in packs of 10.

5¼" DISCS				3½" DISCS	
40 T SS DD	£12(d)	40 T DS DD	£16(d)	80 T SS DD	£30(d)
80 T SS DD	£21(d)	80 T DS DD	£22(d)	80 T DS DD	£38(d)

FLOPPICLENE DRIVEHEAD CLEANING KIT

FLOPPICLENE Disc Head Cleaning Kit with 28 disposable cleaning discs ensures continued optimum performance of the drives. **£14.50 (b)**

DRIVE ACCESSORIES

Single Disc Cable £6 (d) — Dual Disc Cable £8.50 (d)
10 Disc Library Case £1.80 (d) — 30 Disc Storage Box £6 (c)
30/40 Disc Lockable Box £14 (c) — 100 Disc Lockable Box £16(c)

MONITORS

All 14" monitors now avilable in plastic or metal cases, please specify your requirement.
14" RGB 1431 STD Res £185 (a); 1451 Med Res £240 (a); 1441 Hi Res £375 (a).
14" RGB with PAL & Audio 1431 AP Std Res £205 (a) 1451 AP Med Res £275 (a)
Swivel Base for Plastic 14" Microvitecs £20 (c)
20" RGB with PAL & Audio 2030CS Std Res £380 (a); 2040CS Hi Res £685 (a).

KAGA TAXAN 12" RGB

VISION II Hi Res £210 (a); VISION III Plus £330 (a)
SUPERVISION III Plus £330 (a)
MITSUBISHI 14" RGB Med RES IBM & BBC Compatible £229 (a)

MONOCHROME MONITORS:

SANYO DM8112CX Hi Res 12" Green Screen £95 (a)
KAGA KX1201G Hi Res 12" Etched Green Screen £99 (a)
KAGA KX1203A Hi Res 12" Etched Amber screen £105 (a)
PHILIPS BM7502 12" Hi Res Green Screen £75 (a)
PHILIPS BM7522 12" Hi Res Amber Screen £79 (a)
BBC Leads RGB £5(d) Microvitec £3.50m (d) Monochrome £3.50 (d)

UVERASERS

UV1T Eraser with built-in timer and mains indicator. Built-in safety interlock to avoid accidental exposure to the harmful UV rays.
It can handle up to 5 eproms at a time with an average erasing time of about 20 mins. **£59 + £2 p&p.**
UV1 as above but without the timer. **£47 + £2 p&p.**
For Industrial Users, we offer UV140 & UV141 erasers with handling capacity of 14 eproms. UV141 has a built in timer. Both offer full built in safety features UV140 **£69**, UV141 **£85, p&p £2.50.**

PRINTER BUFFER

The buffer offers a storage of 64K. Data from three computers can be loaded into the buffer which will continue accepting data until it is full. The buffer will automatically switch from one computer to next as soon as that computer has dumped all its data. The computer then is available for other uses. LED bar-graph indicates memory usage. Simple push button control provides. REPEAT, PAUSE and RESET functions. Integral power supply. **£199 (a).**
BBC Cable Set £30.

Serial Test Cable

Serial Cable switchable at both ends allowing pin options to be re-routed or linked at either end — making it possible to produce almost any cable configuration on site.
Available as M/M or M/F **£24.75 (d)**

Serial Mini Patch Box

Allows an easy method to reconfigure pin functions without rewiring the cable assay. Jumpers can be used and reused. **£22 (d)**

Serial Mini Test

Monitors RS232C and CCITT V24 Transmissions, indicating status with dual colour LEDs on 7 most significant lines. Connects in Line. **£22.50 (d)**

CONNECTOR SYSTEMS

I.D. CONNECTORS

(Speedblock Type)

No of ways	Header Plug	Receptacle	Edge Conn.
10	90p	85p	120p
20	145p	125p	195p
26	175p	150p	240p
34	200p	160p	320p
40	220p	190p	340p
50	235p	200p	390p

D CONNECTORS

No of Ways	9	15	25	37
MALE:				
Ang Pins	120	180	230	350
Solder	60	85	125	170
IDC	175	275	325	—
FEMALE:				
St Pin	100	140	210	380
Ang Pins	160	210	275	440
Solder	90	130	195	290
IDC	195	325	375	—
St Hood	90	95	100	120
Screw Lock	130	150	175	—

TEXTOOL ZIF

SOCKETS 24-pin £7.50
28-pin £9.10 40-pin £12:10

EDGE CONNECTORS

	0.1"	0.156"
2 x 6-way (commodore)	—	300p
2 x 10-way	150p	—
2 x 12-way (vic 20)	—	350p
2 x 18-way	—	140p
2 x 23-way (ZX81)	175p	220p
2 x 25-way	225p	220p
2 x 28-way (Spectrum)	200p	—
2 x 36-way	250p	—
1 x 43-way	260p	—
2 x 22-way	190p	—
2 x 43-way	395p	—
1 x 77 way	400p	500p
2 x 50-way (S100conn)	600p	—

EURO CONNECTORS

DIN 41612	Plug	Skt
2 X 32 way St Pin	230p	275p
2 X 32 way Ang Pin	275p	320p
3 X 32 way St Pin	260p	300p
3 X 32 way Ang Pin	375p	400p
IDC Skt A + B	400p	
IDC Skt A + C	400p	

For 2 X 32 way please specify spacing (A + B, A + C).

MISC CONNS

21 pin Scart Connector 200p
8 pin Video Connector 200p

AMPHENOL CONNECTORS

36 way plug Centronics (solder 500p (IDC) 475p
36 way skt Centronics (solder) 550p (IDC) 500p
24 way plug IEEE (solder) 475p (IDC) 475p
24 way skt IEEE (solder) 500p (IDC) 500p
PCB Mtg Skt Ang Pin
24 way 700p 36 way 750p

GENDER CHANGERS

25 way D type

Male to Male....£10
Male to Female....£10
Female to Female....£10

RS 232 JUMPERS

(25 way D)

24" Single end Male	£5.00
24" Single end Female	£5.25
24" Female Female	£10.00
24" Male Male	£9.50
24" Male Female	£9.50

DIL SWITCHES

4-way 90p 6-way 105p
8-way 120p 10-way 150p

RIBBON CABLE

(grey/metre)

10-way	40p	34-way	160p
16-way	60p	40-way	180p
20-way	85p	50-way	200p
26-way	120p	64-way	280p

DIL HEADERS

	Solder	IDC
14 pin	40p	100p
16 pin	50p	110p
18 pin	60p	—
20 pin	75p	—
24 pin	100p	150p
28 pin	160p	200p
40 pin	200p	225p

ATTENTION

All prices in this double page advertisment are subject to change without notice.
ALL PRICES EXCLUDE VAT
Please add carriage 50p unless indicated as follows:
(a) £8 (b) £2.50 (c) £1.50 (d) £1.00

TECHNOLINE VIEWDATA SYSTEM. TEL: 01-450 9764

Using 'Prestel' type protocols. For information and orders — 24 hour service, 7 days a week

74 SERIES

7400	0.30
7401	0.30
7402	0.30
7403	0.30
7404	0.36
7405	0.30
7406	0.40
7407	0.40
7408	0.30
7409	0.30
7410	0.30
7411	0.30
7412	0.30
7413	0.50
7414	0.70
7416	0.36
7417	0.40
7420	0.30
7421	0.60
7422	0.36
7423	0.36
7425	0.40
7426	0.40
7427	0.32
7428	0.43
7430	0.30
7432	0.36
7433	0.30
7437	0.30
7438	0.40
7439	0.40
7440	0.40
7441	0.90
7442A	0.70
7443A	1.00
7444	1.10
7445	1.00
7446A	1.00
7447A	1.00
7448	1.00
7450	0.36
7451	0.35
7453	0.38
7454	0.38
7460	0.55
7470	0.50
7472	0.45
7473	0.45
7474	0.50
7475	0.60
7476	0.45
7480	0.65
7481	1.80
7483A	1.05
7484A	1.25
7485	1.10
7486	0.42
7489	2.10
7490A	0.55
7491	0.70
7492A	0.70
7493A	0.55
7494	1.10
7495A	0.60
7496	0.80
7497	2.10
74100	1.90
74107	0.50
74109	0.75
74110	0.75
74111	0.55
74116	1.70
74118	1.10
74119	1.70
74120	1.00
74121	0.55
74122	0.70
74123	0.80
74125	0.65
74126	0.55
74128	0.55
74132	0.75
74136	0.70
74141	0.90
74142	2.50
74143	1.30
74144	2.70
74145	1.10
74147	1.70
74148	1.40
74150	1.75
74151A	0.70
74153	0.80
74154	1.40
74155	0.80
74156	0.90
74157	0.80
74159	1.75
74160	1.10
74161	0.80
74162	1.10
74163	1.10
74164	1.20
74165	1.10
74166	1.40
74167	4.00
74170	2.00
74172	4.20
74173	1.40
74174	1.10
74175	1.05
74176	1.00
74178	1.50
74179	1.50
74180	1.00
74181	3.40
74182	1.40
74184	1.80
74185A	1.80
74190	1.30
74191	1.30
74192	1.10
74193	1.15
74194	1.10
74195	0.80
74196	1.30
74197	1.10
74198	2.20
74199	2.20
74221	1.10
74251	1.00
74259	1.50
74265	0.80
74273	2.00
74276	1.40
74278	1.70
74279	0.90
74283	1.05
74742	3.20
74290	0.90
74293	0.90
74298	1.80
74351	2.00
74365A	0.80
74366A	0.80
74367A	0.80
74376	1.60
74390	1.10
74393	1.20
74490	1.40

74LS SERIES

74LS00	0.24
74LS01	0.24
74LS02	0.24
74LS03	0.24
74LS04	0.24
74LS05	0.24
74LS08	0.24
74LS09	0.24
74LS10	0.24
74LS11	0.24
74LS13	0.34
74LS14	0.50
74LS15	0.24
74LS20	0.24
74LS21	0.24
74LS22	0.24
74LS24	0.50
74LS26	0.26
74LS27	0.24
74LS28	0.24
74LS30	0.24
74LS32	0.24
74LS33	0.24
74LS37	0.24
74LS38	0.24
74LS40	0.24
74LS42	0.50
74LS43	1.50
74LS48	0.90
74LS49	1.00
74LS51	0.24
74LS54	0.24
74LS55	0.24
74LS73A	0.30
74LS74A	0.35
74LS75	0.45
74LS76A	0.36
74LS78	0.42
74LS83A	0.70
74LS85	0.75
74LS86	0.35
74LS90	0.48
74LS91	0.90
74LS92	0.35
74LS93	0.54
74LS95B	0.75
74LS96	0.90
74LS107	0.40
74LS109	0.40
74LS112	0.45
74LS113	0.45
74LS114	0.45
74LS122	0.70
74LS123	0.80
74LS125	0.50
74LS126	0.50
74LS132	0.65
74LS133	0.55
74LS136	0.45
74LS138	0.55
74LS139	0.55
74LS145	0.95
74LS147	1.75
74LS148	1.40
74LS151	0.65
74LS152	2.00
74LS153	0.65
74LS154	1.60
74LS155	0.65
74LS156	0.65
74LS157	0.50
74LS158	0.65
74LS160A	0.65
74LS161A	0.75
74LS162A	0.75
74LS163A	0.75
74LS164	0.75
74LS165A	1.10
74LS166A	1.50
74LS168	1.30
74LS169	1.00
74LS170	1.40
74LS173A	1.00
74LS174	0.75
74LS175	0.75
74LS181	2.00
74LS183	1.90
74LS190	0.75
74LS191	0.75
74LS192	0.80
74LS194A	0.75
74LS195A	0.75
74LS196	0.80
74LS197	0.80
74LS221	0.90
74LS240	0.80
74LS241	0.80
74LS242	0.90
74LS243	0.90
74LS244	0.80
74LS245	1.10
74LS247	1.10
74LS248	1.10
74LS249	1.10
74LS251	0.75
74LS253	0.75
74LS256	0.90
74LS2457A	0.70
74LS258A	0.70
74LS259	1.20
74LS260	0.75
74LS266	0.60
74LS273	1.25
74LS279	0.70
74LS280	1.90
74LS283	0.80
74LS290	0.80
74LS292	9.00
74LS293	0.80
74LS295	1.40
74LS297	9.00
74LS298	1.00
74LS299	2.20
74LS321	3.70
74LS322A	3.90
74LS323	3.00
74LS324	3.20
74LS348	2.00
74LS352	1.20
74LS353	1.20
74LS356	2.10
74LS363	1.80
74LS364	1.80
74LS365	0.50
74LS366	0.50
74LS367	0.52
74LS368	0.50
74LS373	0.90
74LS374	0.90
74LS375	0.75
74LS377	1.30
74LS378	0.95
74LS379	1.30
74LS381	4.50
74LS385	3.25
74LS390	0.60
74LS393	1.00
74LS395A	1.00
74LS399	1.40
74LS445	1.80
74LS465	1.20
74LS467	1.20
74LS490	1.50
74LS540	1.00
74LS541	1.00
74LS608	7.00
74LS610	19.00
74LS612	19.00
74LS624	3.50
74LS626	2.25
74LS628	2.25
74LS629	1.25
74LS640	2.00
74LS640-1	3.00
74LS641	1.50
74LS642	2.50
74LS642-1	3.00
74LS643	2.50
74LS643-1	3.00
74LS644	3.50
74LS645	2.00
74LS645-1	4.00
74LS668	0.90
74LS669	0.90
74LS670	1.70
74LS682	2.50
74LS683	3.00
74LS684	3.50
74LS687	3.50
74LS688	3.50
74LS783	21.00

74S SERIES

74S00	0.50
74S02	0.50
74S04	0.50
74S05	0.50
74S08	0.50
74S10	0.50
74S11	0.75
74S20	0.50
74S22	0.50
74S30	0.50
74S32	0.60
74S37	0.60
74S38	0.60
74S40	0.50
74S51	0.60
74S64	0.45
74S74	0.70
74S85	3.00
74S86	1.00
74S112	1.50
74S113	1.20
74S114	1.20
74S124	3.00
74S132	1.00
74S133	0.60
74S138	1.80
74S139	1.80
74S140	1.00
74S151	1.50
74S153	1.50
74S157	2.00
74S158	2.00
74S163	3.00
74S169	5.50
74S174	3.00
74S175	3.20
74S188	1.80
74S189	1.80
74S194	3.00
74S195	3.00
74S196	3.50
74S200	4.50
74S201	3.20
74S225	5.20
74S240	4.00
74S241	4.00
74S244	4.50
74S251	2.50
74S257	2.50
74S258	2.50
74S260	1.00
74S261	3.00
74S283	2.70
74S287	2.25
74S288	2.00
74S289	2.25
74S299	4.50
74S373	4.00
74S374	4.00
74S387	2.25

74C SERIES

74C00	0.70
74C04	0.50
74C08	0.70
74C10	0.70
74C14	0.50
74C20	0.70
74C32	1.00
74C42	1.50
74C48	1.50
74C73	1.00
74C74	1.20
74C76	1.00
74C83	2.00
74C85	2.25
74C86	0.50
74C90	1.90
74C93	1.50
74C95	1.60
74C107	1.00
74C150	5.00
74C151	2.00
74C157	2.50
74C160	1.80
74C161	1.80
74C162	1.80
74C163	1.80
74C173	1.00
74C174	1.50
74C175	1.50
74C193	1.50
74C194	1.50
74C195	1.50
74C221	2.50
74C244	2.00
74C245	2.25
74C373	2.25
74C374	2.25
74C902	1.20
74C911	9.00
74C912	4.50
74C922	6.00
74C923	6.50
74C925	6.50
74C926	7.50

74ALS SERIES

74ALS00	0.45
74ALS02	0.45
74ALS04	0.50
74ALS08	0.50
74ALS10	0.45
74ALS20	0.45
74ALS32	0.45
74ALS74	0.70
74ALS138	1.50
74ALS139	1.50
74ALS244	4.00
74ALS245	4.75
74ALS573	2.60
74ALS574	4.50
74ALS580	2.60

4000 SERIES

4000	0.20
4001	0.24
4002	0.25
4006	0.70
4007	0.25
4008	0.60
4009	0.45
4010	0.60
4011	0.24
4012	0.25
4013	0.36
4014	0.60
4015	0.70
4016	0.36
4017	0.55
4018	0.60
4019	0.60
4020	0.80
4021	0.60
4022	0.70
4023	0.30
4024	0.48
4025	0.24
4026	0.90
4027	0.40
4028	0.60
4029	0.75
4030	0.35
4031	1.25
4032	1.00
4033	1.25
4034	2.50
4035	0.70
4036	2.50
4037	1.10
4038	1.00
4040	0.60
4041	0.55
4042	0.50
4043	0.60
4044	0.60
4045	1.00
4046	0.60
4047	0.60
4048	0.55
4049	0.36
4050	0.35
4051	0.65
4052	0.60
4053	0.60
4054	0.80
4055	0.80
4056	0.85
4060	0.70
4063	0.85
4066	0.40
4067	2.30
4068	0.25
4069	0.24
4070	0.24
4071	0.24
4072	0.24
4073	0.24
4075	0.24
4076	0.65
4077	0.25
4078	0.25
4081	0.24
4082	0.25
4085	0.60
4086	0.75
4089	1.25
4093	0.35
4094	0.90
4095	0.95
4096	0.90
4097	2.70
4098	0.75
4099	0.99
4501	0.36
4502	0.55
4503	0.36
4504	0.95
4505	3.60
4506	0.90
4507	0.35
4508	1.20
4510	0.55
4511	0.55
4512	0.55
4513	1.50
4514	1.10
4515	1.10
4516	0.55
4517	2.20
4518	0.48
4519	0.32
4520	0.60
4521	1.15
4522	0.80
4526	0.70
4527	0.80
4528	0.65
4529	1.00
4531	0.75
4532	0.65
4534	3.80
4536	2.50
4538	0.75
4539	0.75
4541	0.90
4543	0.70
4551	1.00
4553	2.40
4555	0.36
4556	0.50
4557	2.40
4560	1.40
4566	1.40
4568	2.40
4569	1.70
4572	0.45
4583	0.90
4584	0.48
4585	0.60
4724	1.50
14411	7.50
14412	7.50
14416	3.00
14419	2.60
14490	4.20
14495	4.50
145000	6.50
14599	2.00
22100	3.50
22101	7.00
22102	7.00
40014	0.48
40085	1.20
40097	0.36
40098	0.40
40100	1.50
40101	1.25
40102	1.30
40103	2.00
40104	1.20
40105	1.50
40106	0.48
40107	0.55
40108	3.20
40109	0.80
40110	2.25
40114	2.25
40147	2.80
40163	1.00
40173	1.20
40174	1.00
40175	1.00
40192	1.00
40193	1.00
40194	1.00
40244	1.50
40245	1.50
40257	1.80
40373	1.80
40374	1.80
80C95	0.75
80C97	0.75
80C98	0.75

LINEAR ICs

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75454	0.70
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6.00MHz	1.40
6.144MHz	1.40
7.00MHz	1.50
7.16MHz	1.75
8.00MHz	1.50
8.867MHz	1.75
10.00MHz	1.75
10.50MHz	2.50
10.70MHz	1.50
11.00MHz	3.00
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14.31MHz	1.60
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CIRCLE 62 FOR FURTHER DETAILS.

Memory telephone dialler

by T. Segaran

UM91610 provides number storage, last-number redialling and call-progress monitoring.

Mr Segaran was formerly with STC, working on the design of electronic telephone equipment. He is now at Tunstall Telecom, where he is involved with emergency communications equipment for the elderly.

The dialling part of this circuit is based around the UM 91610 dialler i.c. (Fig. 1(a), 2(b)), which is a low-voltage c.mos device with an operating current of 500μA and data-retention current of 3 μA. Timing for the dialling is derived from an RC oscillator, which has an overall variation of ± 5%. The dialling pulse rate is normally 10 pulses per second and the "mark/space" ratio 33.3/66.6 to suit the needs of the British Network,* but can be changed if necessary to meet foreign telephone network requirements: dial rate can be changed to 20 pulses per second and the mark/space to 40/60. XY matrix keyboards will interface directly to the chip.

Figure 2 shows the block diagram of the complete unit. The polarity bridge is necessary since BT do not guarantee the polarity of the direct voltage when it reaches the subscriber's home: in fact, during call set-up the polarity can change. The high-voltage switch shown is operated by the 'on-line' buttons: it is solid state and is used by the dialler chip to signal by breaking the line current. The need for constant voltage-drop and constant-current circuits is explained later. Finally, the low-current detector circuit is used to turn off the high-voltage switch when a parallel 'phone is picked up. Figure 3 shows the circuit details.

Breaking and looping of the line is carried out by a high-

* Any apparatus for connection to the public switched network must be approved by the appropriate telecommunications body. In the UK, this is BABT, the British Approvals Board for Telecommunications.

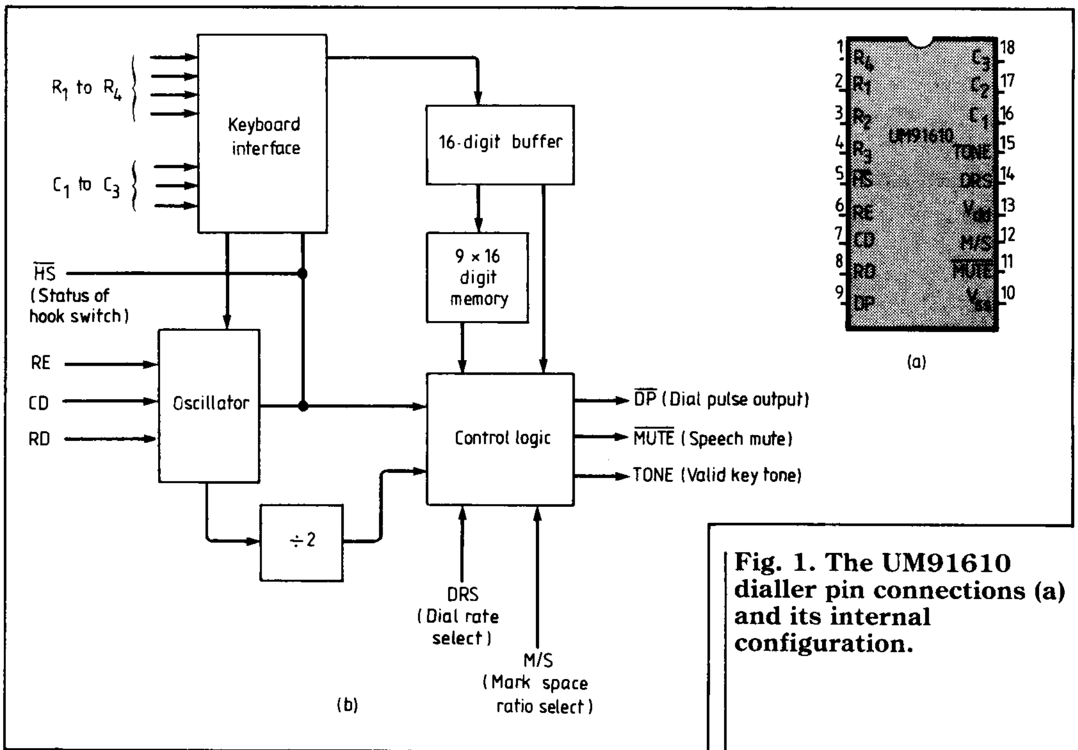
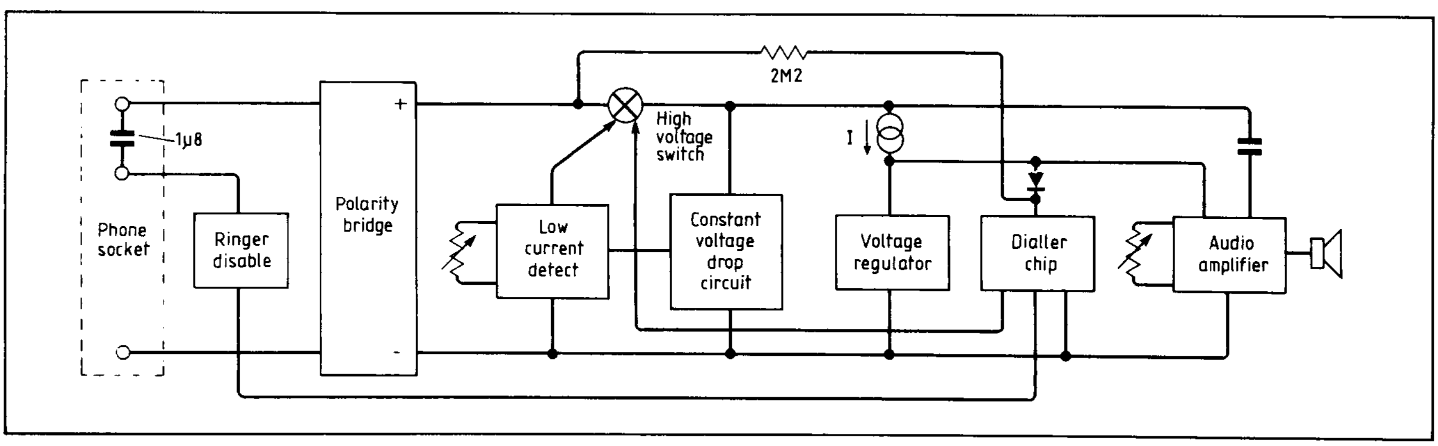


Fig. 1. The UM91610 dialler pin connections (a) and its internal configuration.

Fig. 2. Block diagram of the dialler unit.



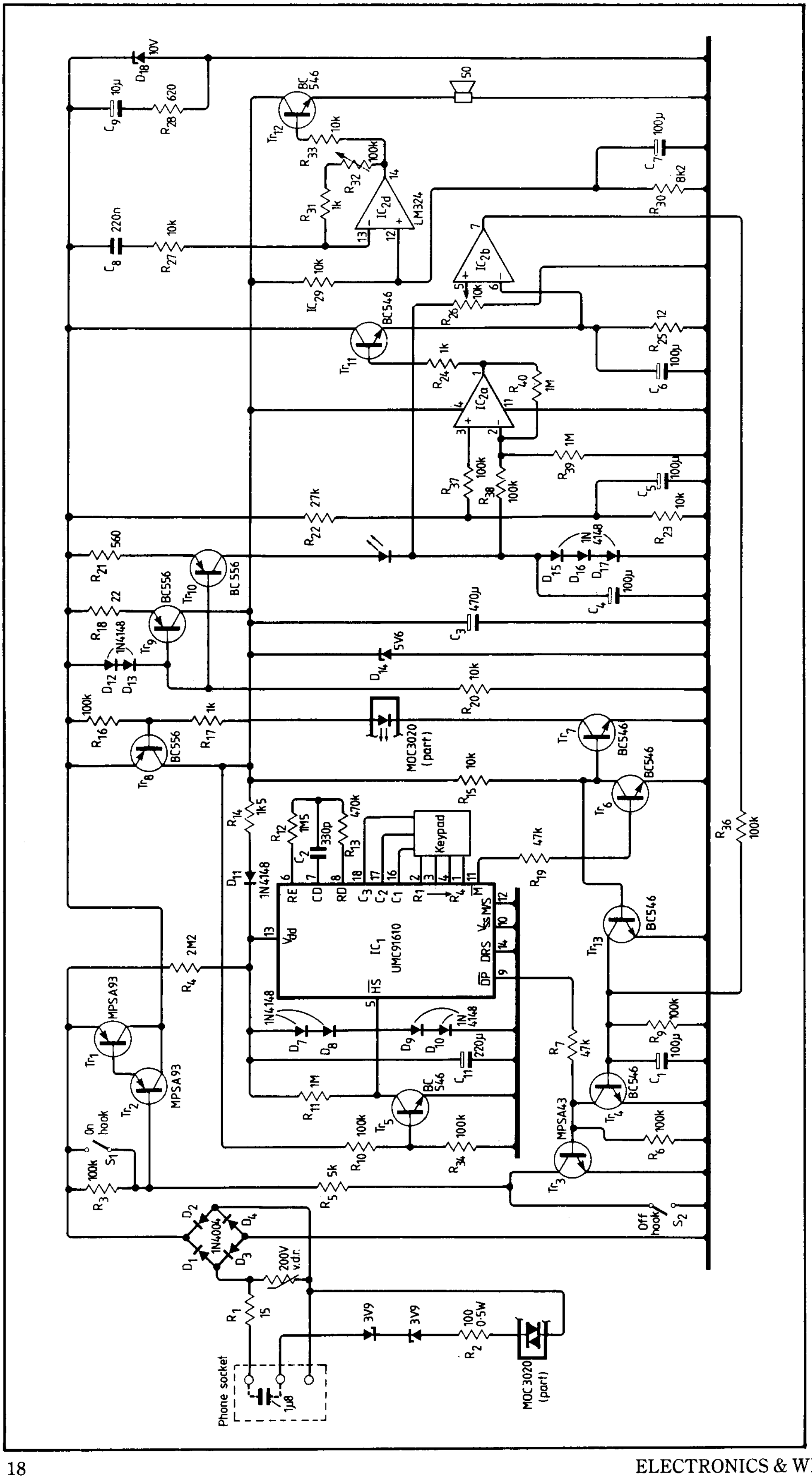


Fig. 3. Complete circuit diagram of the memory telephone dialler.

voltage bipolar device, the MPSA-93, which has a collector-emitter breakdown voltage of 300V, necessary because of the high voltage generated when the current through the exchange relay is interrupted. The voltage dependent resistor will, however, clamp this voltage to about 250V. During dialling, one needs to prevent dialling pulses from tinkling the bells on parallel-connected telephones: an optically isolated triac, the MOC 3020, controlled by Tr_6 and Tr_7, puts a 100 ohm shunt across the 'bell-wire' during dialling. In addition to this function, the 100 ohm resistor and the 1.8μF capacitor found in the "master" socket provides a spark-quench circuit during dialling. The i.c. and the speech amplifier are driven from a supply derived from the line: the speech amplifier needs about 5.6V and the dialler 2.5V. The 5.6 supply is zener-regulated and supplied by a constant-current source set to about 25 mA, so that a high a.c. impedance is presented to the telephone line. The constant-current source itself is driven by a supply kept at about 7.5 volts by a feedback control circuit, formed by IC_{2a} and T_{r11}. However, a.c. signals such as speech are decoupled by the capacitors and can be superimposed on the d.c. level. The impedance of the unit is set at roughly 600Ω by R_{28}.

Speech amplification is carried out by IC_{2d} and Tr_{12}, with a simple volume control provided.

IC_{2b} monitors the current shunted through R_{25}, while R_{26} is set so that on a particular line, the output of IC_{2b} is low and the unit remains on line, because Tr_4 is switched off. However, when a parallel telephone is used, it shunts some of the current away, the voltage across R_{25} drops and the output of IC_{2b} goes high, which switches on Tr_4 and the circuit switches off from the line.

The dialler chip is supplied by the 5.6V regulated supply, using a resistor and diode to step the voltage down to about 2.5V. There is also a 2M2 resistor that provides the i.c. with data-retention current when the unit is off-line. Dual pulses are taken directly to Tr_3, which controls Tr_1 and Tr_2, the line loop transistors. Each time the unit is placed in the off-line condition, the $\overline{HS}$ pin of the i.c. receives an input from Tr_5.

Using the dialler

Digits 1-9 are used for normal dialling after the *on-line* button has been operated. To place the unit in standby, either the *off-line* button or the parallel telephone is operated to start a conversation, and hence disconnect the dialler. The last number dialled can be redialled by coming on-line and pressing #0. To store a telephone number one needs to operate *, followed by the telephone number and another *. Then, the location for storage (any number from 0-9) is pressed. To recall a number from store operate #, followed by the location.

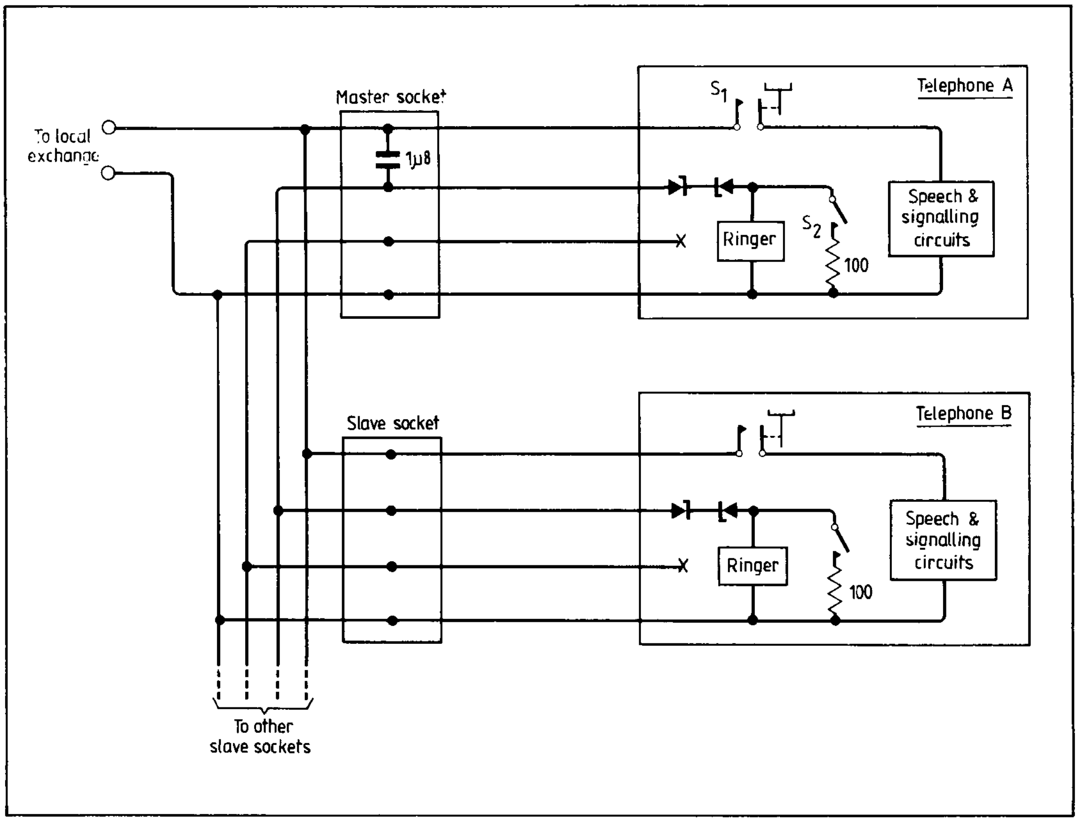


Fig. 4. British Telecom's telephone interconnection layout.

- storage and easy dialling of ten, 16-digit telephone numbers.
- last number redial
- no external power source required
- monitoring of progress of call on built-in speaker, with volume control provided
- when handset on parallel telephone is lifted, unit automatically disconnects.

'New' interconnection scheme

To enable one to connect additional telephones on one exchange line easily, British Telecom have come up with a new wiring scheme. The wiring is a simple four-wire interconnect, connecting all sockets in parallel on any one telephone line. There is one master socket and normally up to three slave sockets on any one line. A telephone unit can be plugged into any one of the sockets to function correctly.

When telephone A (Fig. 4) is used, Sw_1 closes and draws line current. At the same time, Sw_2 closes and places 100 ohms shunt across its own ringer and also across the ringer of telephone B. Therefore the high voltages generated on the line during dialling do not cause tinkling of the bells. The ringer impedance is usually greater than 4kΩ.

The 1.8 μF and 100 ohm components also appear across the line and perform the spark-quench function when the current through the exchange relay is broken during signalling. The back-to-back zeners present a high impedance to speech, while allowing ringing signals through and performing the spark quench function. When ringing voltage is present, it is fed via the 1.8 μF capacitor to telephone A, telephone B and all other ringers.

BOOKS

A First Electronics Course by R.B. Arnold. Stanley Thornes (Publishers), 86 A4-size pages, soft covers: £3.25 including post and packing from the publishers at Old Station Drive, Leckhampton, Cheltenham, GL53 0DN. Aimed at 11 to 15-year-olds, this most attractively-presented book wears its learning very lightly. Chapters cover basic electricity and electronic components, switching, amplification, electronic systems, integrated circuits and digital techniques. Throughout, the emphasis is on the practical side. The author suggests many experiments and gives constructional details of a variety of simple projects including a burglar alarm, an intercom, a radio receiver and a binary counter. Entertainment value is very high: the pages are packed with diagrams, photographs and cartoons and at the end of most chapters there are questions or a puzzle. The book is intended for the classroom, but would be a lot of fun at home too. Very good value for money.

BBC Basic Programming for Schools and Colleges by Mark Bindley. Stanley Thornes, 170 pages, soft covers: available from the publishers at the address above for £3.65 inclusive. Systematic, thorough introduction to BBC Basic aimed at 16+ exmination courses in computer studies, with flow-charts, program examples and many interesting exercises based on practical problems to investigate at the keyboard. Plenty of information and again, excellent value.

MEDICAL r.f.

The effects of electric and magnetic fields on the human body remain in dispute. With the exception of thermal effects, directly related to power, everything else still seems to be open to question. At the recent IEE conference "Electric and Magnetic Fields in Medicine and Biology" (IEE Conference Publication No 257) for every claim there seemed to be a counterclaim.

For example, Dr A.T. Barker of Sheffield University accepts that many thousands of difficult bone fractures have been cured, particularly in the USA, by treatments involving the use of low-energy, low-frequency pulsed waveforms "to stimulate bone growth", but he provided experimental evidence that the pulsed waveforms do not actually contribute significantly to the healing process since he claimed that similar successes can be achieved with the generator switched off.

Similarly, a "double-blind" clinical trial at Sheffield of pulsed 27MHz in the treatment of soft tissue injuries failed to show a statistically significant difference between those so treated and control groups on whom "dummy" machines were used. This trial was based on extensive monitoring of some 70 patients. On the other hand, the Sheffield group speak highly of magnetic stimulators, and many of the 33 papers similarly seem to show useful applications of magnetic or electric fields or currents in medicine, without any clear idea of how this comes about.

The impression is one of "service engineers attempting to diagnose and cure faults on complex (human) equipment with nothing more than a simple lay-out diagram and little or no idea of how the active devices or the test instruments actually work. It was noticeable that the references listed in the papers were invariably to medical journals rather than electronic publications, and a not very successful "marriage" of two very different disciplines.

In a session on safety, J.A. Dennis of NRPB put forward views on allowable exposure limits for low-frequency (under 3kHz) electromagnetic fields. He points out that the existence of even slight perceptible effects, whether harmful or not, in people's homes and gardens are probably not acceptable. His suggested figure for public places is less than 12kV/m. A study at Manchester University, funded by the CEGB, sought to answer the question "Can induced 50Hz body currents affect mental functions?" The experimental results seen to be open to more than one interpretation, though it is interesting to note that the technique was tested also against the amount of alcohol drunk the previous night and that "the observation that subjects responded faster in the syntactic-reasoning test when they had had a longer night's sleep is also not unexpected." It really does seem that the human body is too complex for anyone to come up with the simple yes or no answers or even to achieve similar results to those reported elsewhere. This uncertainty was reflected also in papers on leukemia and electromagnetic fields, overhead power lines and childhood cancers.
Absolute certainty was little in evidence.

50kW SOLID-STATE

The first all-solid-state v.h.f. television transmitting installation providing an r.f. output of 50kW (vision) has been taken into service by Tokyo Broadcasting System Inc (TBS) a Japanese commercial broadcaster. It has been developed jointly by TBS and Toshiba and based on 1.5kW field-effect transistor amplifiers. The installation comprises two 25kW vision transmitters, each having 20 power amplifier units plus five amplifiers in the sound section.

It has sometimes been suggested that the electronics industry has much in common with pig farming. It is all too easy to increase production faster than demand. The past few months have underlined the problems that face manufacturers catering for a specialised market such as broadcast television studio equipment. Pye TVT Ltd which, as the broadcast company of Philips has long specialized in major turnkey studio contracts, has announced that it is dicontinuing its studio systems division this year, although continuing its broadcast transmitter business. RCA, even before announcing its merger with General Electric (US), was in process of withdrawing from the broadcast market. Some months ago, GEC closed its GEC-McMichael factory at Slough, transferring only some of its television studio products back to Marconi at Chelmsford. In the USA, the broadcast industry has been pressing the National Association of Broadcasters to make the annual NAB convention more cost-effective by concentrating even more on the associated exhibition — the largest international event in the broadcasting calendar.

Pye TVT believe that the industry-wide overcapacity results from the reduced level of spending on studio systems, claiming that "there have been no new broadcast companies of significance established in recent years and the existing broadcast companies are buying more of their equipment direct from individual specialist manufacturers. The trend is away from complete systems with re-equipping of existing studios carried out on a piece-meal basis." The many independent production companies on the West Coast of the USA have increasingly ceased to be captivated by the claims of "new technology", except where this offers something entirely new or reduces costs significantly, and are retaining colour cameras for 10-15 years or more operational service. "If it ain't broke why fix it?" is the current attitude. Japanese manufacturers have captured a large share of this market, although Link Electronics claim to have received over 50 orders for their new 130 automated camera in its first year of production. It is often claimed, however, that sales need to reach several hundred before a new model becomes profitable. The broadcast transmitter market is benefitting from the improved efficiency now possible with klystron amplifiers, capable of substantially reducing overall power costs both for new installations and as retrofits.

Although the studio and broadcast transmitter market is small in comparison with some other segments of electronics, it remains a significant element in the diminishing part of the civilian "high-tech" industry in which the UK still retains advanced research, design and production capability in an increasingly competitive international market. How long this will continue remains to be seen.

FCO GIVE UP ORFORDNESS

In the September 1984 Communications Commentary I noted the proposal to transfer responsibility for the high-power broadcast transmitters at Orfordness, Crowborough, Cyprus and Masirah Island from the Foreign and Commonwealth Office to the BBC. The plant to "cut" FCO staff by transferring them to the BBC was, however, resisted both by those concerned and also by the BBC who were not anxious to take on more staff at a time when they were actively cutting down their own engineering departments. It was not until July 1985 that an interim arrangement was announced, and talks are still continuing.

The present plan seems to be that the BBC will provide management and technical support from April for Orfordness. Crowborough has been closed down. There is to be no change in the status of the Cyprus and Oman relay stations but managerial responsibility will pass to the BBC. Some members of the FCO broadcast group are being transferred to other Civil Service departments, some to the BBC and some face early retirement or being made redundant. The FCO broadcast engineering centre in Buckinghamshire is to close.

The closing of Crowborough is the end of what started as "a big hole in the ground" in 1942. The underground Aspidistra transmitter was first used in November that year at the time of the "Torch" landings in North Africa. A feature of the RCA 600kW transmitter was the speed at which it could change frequency for purposes of "black broadcasting". It has been claimed that by operating at periods on the Rabat Vichy-controlled frequency it succeeded in misleading the Royal Navy into assuming that Rabat, Morocco was already in Allied hands! Whether the "black" announcements had other more useful results is open to question — but the Crowborough transmitter certainly provided many listeners in south-east England with excellent reception of the BBC World Service over many years. A growing problem, however, was seepage of water into the "big hole".

Crowborough was also the site of a special wartime v.l.f. communications link with North America. Later it was for this circuit that the original version of the Piccolo radio-teleprinter system was developed by the Diplomatic Wireless Service, now incorporated into the FCO Communications Branch.

WIDE-WORLD OF E.M.C.

The increasing recognition that much that is typed on an electric or electronic keyboard is vulnerable to "bugging" from outside the building will do something to persuade manufacturers to do more to reduce radio frequency interference from business and personal computers. The military have been forced into taking the stringent precautions laid down by "Tempest" that can put the cost of a small computer installation into the five-figure bracket. This form of interception can defeat any form of enciphering within the computer. Some of the recent low-cost word processors put out sufficient r.f. to interfere with the weak-signal reception over a considerable area.

The 7th International Zurich symposium and technical exhibition on "electromagnetic compatibility" is scheduled for March 3-5, 1987. A recent "call for papers" listed the topics now covered by the term e.m.c. as including the social and economic impact; electromagnetic pollution, control and enforcement; spectrum economy and management; national and international co-operation; immunity of electronic systems; biological effects of medical electronics; nuclear electromagnetic pulse (nemp) impact; and even "emp education".

VIDEO DISCS

Although the capacitive-type video type disc of RCA failed to attract consumers in the USA and the UK and the LaserVision player has so far made few inroads on the VCR market, Japanese firms are reporting increasing sales of both formats in their home market and are continuing to develop new techniques and applications. Toshiba is planning h.d.tv systems for both disc and tape (barium ferrite) and a 40-inch screen. The disc is on the LaserVision-based approach. Victor and Sharp are hoping to market "three-dimensional" VHD videodiscs for which the viewer would wear high-speed liquid-crystal glasses to which would be fed a switching signal. Each side of the disc plays for 30 minutes. Videodiscs suitable for recording as well as playback are also in the pipeline although unlikely to reach the market for a year or two.

Amateur Radio

50MHz OPENED

The 50.0 to 50.5MHz band was officially released to all British "Class A" amateurs on February 1. The DTI has promised to review the position, especially in regard to including Class B licence holders, after the first year.

Maximum power must not exceed a carrier of 14dBW (25 watts) effective radiated power or peak envelope power 20dBW (100 watts) e.r.p. The earlier higher-power experimental permits for non-television hours have been withdrawn. There are now no time limits but a number of restrictions have been imposed inititally in order to minimize the possibility of interference to European Band 1 (channel E2) transmissions, with particular reference to the low-power System B/PAL transmitter at Antwerp, Belgium (vision carrier 48.25MHz, sound carrier 53.75MHz, 0.1/0.01kW e.r.p. with vertical polarization). Restrictions include: maximum transmitting antenna height above ground of 20 metres; horizontal polarization only; no mobile, portable or "temporary premises" operation; no "repeater installations". There are however no special restrictions on times or modes of operation. Within the UK, amateurs will be regarded as the "primary" users of the band.

'The DTI have indicated that individual exemptions from the "20m above ground level" rule may be made for amateurs living in high-rise flats. Reciprocal licensing for 50MHz is not possible in Region 1 where the primary use in countries other than the UK remains television broadcasting.

The results achieved over the past few years by UK amateurs holding the "night-time" 50MHz experimental permits, together with the use of this band by amateurs in Regions 2 and 3, have underlined that interesting anomalous propagation conditions at such frequencies including occasional ionospheric reflection, even in sunspot minimum years, which can result in long-distance "openings". The band is also excellent for Sporadic E and meteor scatter propagation and has unique characteristics at what, in effect, is the true junction of h.f. and v.h.f.

LIMITED E.R.P?

The imposition, at least during a trial period, of a power limit on 50MHz in the form 14dBW carrier or 20dBW p.e.p. e.r.p. may seem logical enough from an administrative viewpoint but highlights, once again, the problems of adopting such criteria for amateur stations. In practice there is no way in which the average amateur can "measure" his effective radiated power, which must therefore be derived from a series of calculations based in many cases on manufacturers' specifications or blind guesswork.

The gain of the antenna, the attenuation of the feeder, the losses in antenna tuning units, the efficiency of the power amplifier are seldom known with any degree of certainty even by those who are fully conversant with the term "effective radiated power". Output power meters are not mandatory and low-cost units often have a wide tolerance, particularly when the answer is multiplied by a high-gain antenna.

The attenuation of a coaxial cable and the associated plugs and sockets may increase significantly over a period of months or years. Home-built and factory antennas seldom have the gain that theory predicts.

Then again, when it is a question of potential interference to continental television, the antenna height above ground is only one factor. Height above sea level in relation to intervening hills is more significant.

I suspect that a random check on how many Class A licensed amateurs fully understand the 50MHz regulations would prove embarrassing to all concerned.

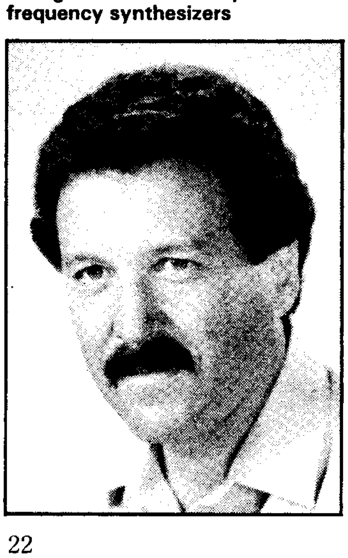
PAT HAWKER, G3VA

by K. Lewis M.I.E.R.E.

Level-translating full-wave rectifiers

Using transistors as rectifiers to provide high-impedance output and isolation between source and load.

The author
Mr Lewis started his career at Plessey, Ilford, where he designed a v.h.f. synthesizer. In 1973, he joined Grinaker Electronics in South Africa, where he is now group leader with responsibility for design and development of frequency synthesizers



Deriving full-wave, or even half-wave, rectified signals, usually requires compromises and a liberal use of diodes. A rectified output signal is often derived from a peak detecting circuit which exhibits a non-linear output impedance.

A simple circuit was developed by the author in which the rectifiers are transistors and the output is a high impedance current source. This enables level translating without capacitive coupling and also provides isolation between the output load and the driving source.

From this circuit a number of related circuits were developed including two precision voltage-to-current magntitude converters, the first of which employs one op-amp and the second two.

The circuits shown in Figs 1(a) and (b) use only four components each to produce output currents I+ or I−, proportional to the magnitude of a voltage source $|V_s|$. In terms of generalized solution it is convenient to label the two inputs as ports A and B, and the outputs as ports C and D as shown. In the circuits illustrated, port B is shown grounded via the dotted line and the signal is applied to port A. Voltages V + and V−, with respect to 0V, are the supply voltages to which the rectified currents are returned. Any output load may be inserted at port C or D.

The operation of the p-n-p fullwave rectifier is shown in Fig. 1(b): ignore the dotted line connections to Fig 1(a). When V_s is positive, Tr_3 is cut off and Tr_4 is driven in the common base mode. Tr_4 base will be close to 0V and Tr_4 emitter is clamped positive, at a potential effectively equal to the voltage drop across a diode. This voltage for Tr_4 is denoted by V_{be4}. The resulting current in the collector of Tr_4 therefore approximates to $I_{C4} = (V_s - V_{be4})/R1$.

When V_s is negative, Tr_4 is cut off and Tr_3 is driven in the common-emitter mode. The base-emitter voltage, V_{be3}, is now subtracted from the source voltage, so that Tr_3 collector current, I_{c3}, approximates to $(V_s - V_{be3})/R_2$. If $R_2 = R_1$ and $V_{be4} = V_{be3} = V_{be}$, then the combined output current will approximate to:

$$I- = (|V_s| - V_{be})/R_1 \text{ for } |V_s| > V_{be}. \quad (1)$$

For $|V_s| < V_{be}$, the output current is comparatively small and non-linear.

Equation 1 represents a full-wave-rectified current output with some distortion introduced by V_{be}. In a practical circuit, resistance R_1 must include the output resistance of the voltage source so that V_s is, in effect, the open circuit voltage. The output current is, of course, essentially independent of V− and in the more general solution I− or I + is proportional to the differential voltage $|V_{AB}|$.

As the base-emitter junction of one transistor limits the reverse base-emitter voltage on the other, V_s can be considerable and is limited by the normal collector voltage ratings of the transistors used. However, in the limit, any load resistor R_L connected to port D must be small enough and the negative supply large enough to ensure that Tr_3 does not bottom on the peak negative excursion of V_s.

In normal operation the load introduced by the rectifier to V_s changes between R_1 plus one diode drop for positive V_s, to $(B_3 + 2)R_1$ plus one diode drop for negative V_s, where B_3 equal the current gain of Tr_3. In effect, the voltage source supplies half-wave current to the rectifier and therefore the source must provide a d.c. return path to V−. If the return path is a low impedance op-amp, for example, there will normally be no problem.

A balanced-input load may be regarded as a load presented by the rectifier which is independent of the polarity of V_s. This may be achieved by combining p-n-p and n-p-n rectifiers as shown by the dotted lines in Fig. 1. With this circuit, simultaneous complementary rectified outputs are available.

In the circuits shown in Fig. 2 (a) and (b), resistors R_1 and R_2 are placed directly in series with the emitters of the transistors. The circuits are similar in operation to those of Fig. 1 and equation 1 still approximates to the output current. The two bases are now connected directly to the voltage source and 0V and the circuits can therefore expect to have an improved frequency response. The disadvantage of this is that both base-emitter junctions are reversed biased to the maximum source voltage. Therefore if $|V_s|$ exceeds 5V, the base-emitter junction can be expected to zener, which is normally undesirable. In the case of a practical circuit where the source resistance R_s cannot be ignored, an additional resistor equal to R_s can be included between 0V and R2 to retain the circuit balance.

In Fig. 2, the load seen by the source voltage varies in a similar manner to that of Fig. 1. Again, balanced operation is achieved by combining n-p-n and p-n-p circuits as shown by the dotted lines. If with this circuit the corresponding emitters are also joined, as indicated, and one pair of resistors R_1 and R_2 are removed, the combined circuit is both simplified and improved. This circuit, shown in Fig. 3. has an elegant simplicity to which a parallel can be drawn with a conventional four-diode bridge rectifier. The transistor version, however, develops high impedance current outputs, whilst the diode version usually develops low impedance voltage outputs. As the reverse base emitter voltages of each transistor are limited with this circuit, the voltage limitations of the circuit of Fig. 1 are applicable.

Depending on the choice of components, all the circuits shown in Fig. 1, 2 and 3 can operate up to several megahertz and, with a sinusoidal source, can exhibit excellent rejection of the fundamental frequency. The performance of practical circuits are detailed in the appendix.

Consider now the operation of the circuit in Fig. 3 when it is driven by a high-impedance current source, I_s, applied to port A, and port B is connected to 0V. I_s comprises the current in R_1 plus the small bias current flowing into the base of Tr_2. A positive voltage V_{AB} will be set up due to the voltage drop across R_1 and the voltage V_{be4}. Tr_2 combined with R_2 forms a current mirror and similar currents are established in both R_1 and R_2. These currents will be close to the value of I_s if the current gains of the respective transistors are high. The current matching between transistors Tr_2 and Tr_4 also depends on the matching of their V_{be} v I_c characteristics. If I_s is reversed, a similar negative voltage V_{AB} is set up. It is apparent that the current in any pair of transistors will closely approximate to I_s and the largest source of error which was V_{be} for the constant voltage source, is now reduced to the respective voltage offsets. It is interesting to note that if all the transistors were matched, the two resistors R_1 and R_2 could be reduced to zero. However, in a practical circuit these resistors are always necessary as they also serve to increase the output impedance of each transistor.

The ideal current source can be approached in the feedback of an op-amp. The circuit shown in Fig. 4 incorporates the circuit of Fig. 3 to produce a precision voltage-magnitude-to-current converter. In this circuit port A has become a virtual earth. This now enables the bases of Tr_2 and Tr_3 to be connected directly to 0V, which considerably improves the accuracy of the circuit. Now the current I_s, equal to V_s/R_s, only feeds R_1 and is no longer required to bias Tr_2 and Tr_3. These transistors are now outside the feedback path and effectively operate as current mirrors to Tr_1 and Tr_4. The op-amp's current drive capability must be equal to the maximum value of I_s.

Transistors are now available with minimum current gains of at least 200 and the largest source of error in this circuit is likely to be their voltage offsets. The contribution of this offset can be reduced by increasing R_1 and R_2. However, as I_s is reduced these offsets again become significant.

The final circuit shown in Fig. 5 eliminates the error due to these discrete transistor offsets by employing a second op-amp in the non-inverting mode. If the two source resistors, Rs_1 and Rs_2, are equal, the currents injected into both pairs of emitters are equal regardless of the transistors' offsets. Since these offsets are no longer important even greater

Rejection of fundamental in circuits shown

	1 kHz rej	f_0 at −40dB	f_0 at −30dB	f_0 for $2f_0$ out −0.5dB	f_0 for d.c. −0.5dB
Fig. 1(b) p-n-p	−52dB	653 kHz	2.24 MHz	3.36 MHz	3.68 MHz
Fig. 2(b) p-n-p	−58dB	1.16 MHz	3.3 MHz	4.6 MHz	9.34 MHz
Fig. 3 n-p-n	−66dB	2.04 MHz	6.38 MHz	4.8 MHz	7.26 MHz
p-n-p	−67dB	1.26 MHz	3.31 MHz	4.79 MHz	7.15 MHz
Fig. 4 n-p-n	−56dB	62.6 kHz	186 kHz	456 kHz	304 kHz
p-n-p	−58dB	62.6 kHz	208 kHz	460 kHz	308 kHz
Fig. 5 n-p-n	−58dB	93.6 kHz	265 kHz	382 kHz	402 kHz
p-n-p	−66dB	99.3 kHz	265 kHz	631 kHz	487 kHz

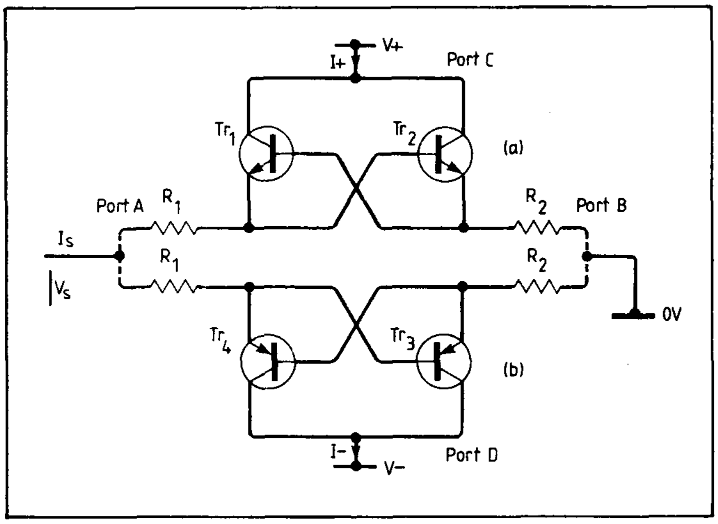


Fig. 1 N-p-n full-wave rectifier at (a) sinks current I+, while p-n-p circuit at (b) sources current I−

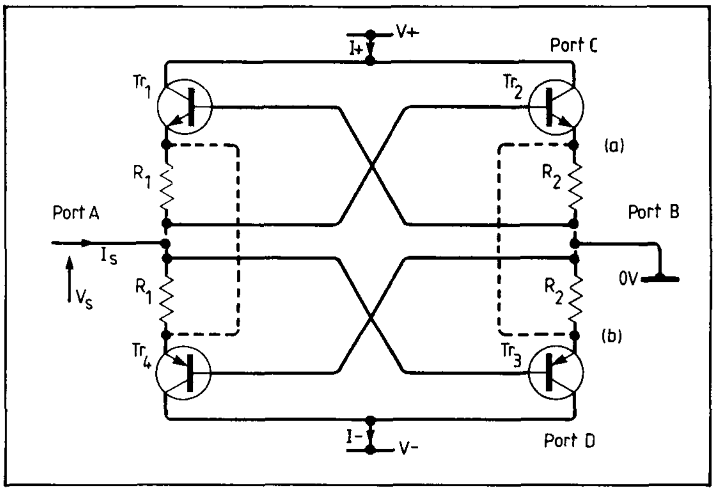


Fig. 2. N-p-n(a) and p-n-p alternative solutions in which the bases are driven directly by the signal.

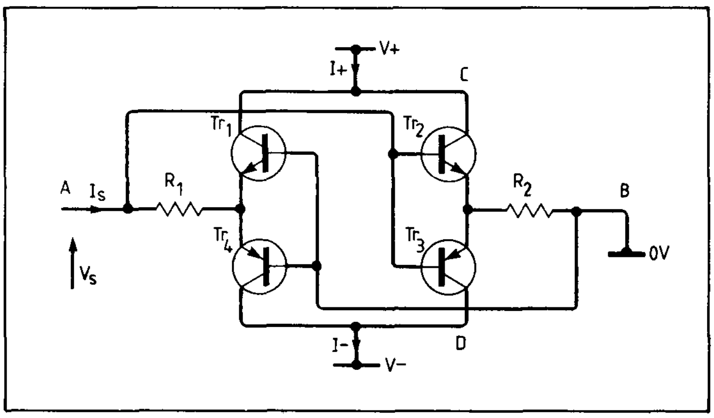


Fig. 3. Full-wave rectifier providing a balanced load to the signal and complementary rectified curents.

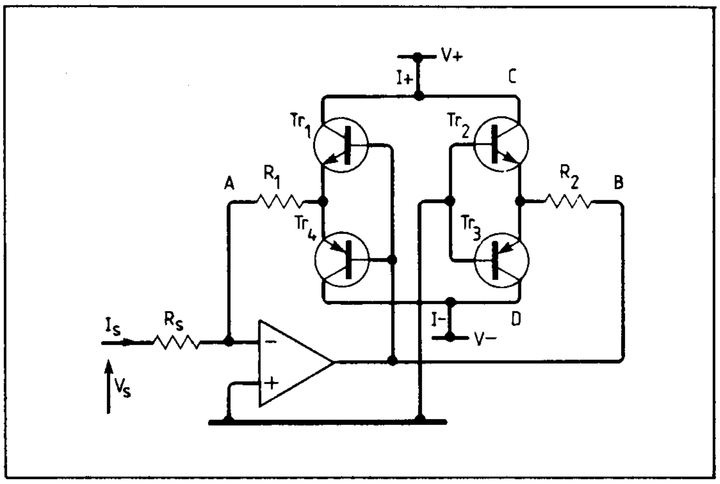


Fig. 4. Precision voltage-magnitude-to-current converter, which incorporates the circuit of Fig. 3.

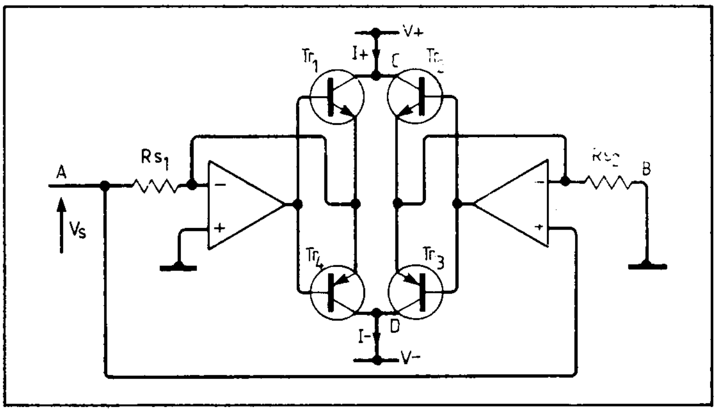


Fig. 5. Precision voltage-magnitude-to-current converter, in which the errors due to the discrete transistor voltage offsets have been removed.

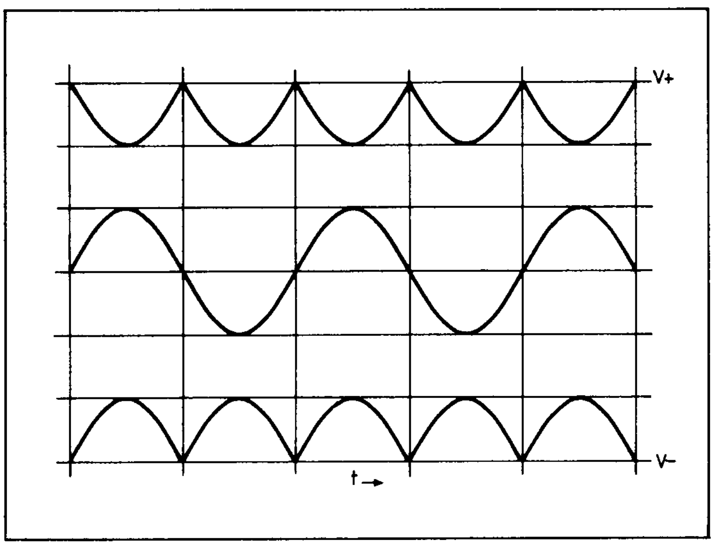


Fig. 6 Waveforms obtained from circuits of Figs 4 and 5.

accuracy may be achieved by employing darlington transistors or enhancement-mode mos fets in place of the discrete transistors shown. Another advantage of this circuit is that the op-amp's current-drive capability need only be limited to the bias currents of the transistors employed.

If only I + or I − is required, it is tempting to simplify the circuits by removing apparently redundant transistors. For example, in Fig. 4, if only I − is required, Tr_2 can be removed and Tr_1 can be replaced by a diode. The ideal diode would however be formed from a third p-n-p transistor with its base and collector shorted and connected to the emitter of Tr_4 and its emitter connected to the base of Tr_4. With this arrangement the op-amp is now required to source twice the current I_s. Although it may now appear attractive to use three similar transistors, at higher levels of I_s the temperature of Tr_3 will exceed that of the transistor diode, resulting in increased V_{be} offsets. In Fig. 4, Tr_1 and Tr_3 will dissipate comparatively similar powers and with a discrete circuit solution, temperature tracking can be expected to be quite reasonable. Also in a practical circuit the frequency response of the circuit in Fig. 4 is superior to the simplified version.

All the circuits shown may be practically utilized. As the transistors employed are essentially current steering or reverse biased the frequency performance can be very good. In the case of the op-amp circuits, for high frequency operation, high slew rate op-amps should be used to minimize rectifying errors in the region where the signal source reverses its polarity. For optimum performance discrete transistors should be matched and resistors close toleranced. However good results were obtained in actual circuits as shown in the appendix using unmatched transistors.

Appendix

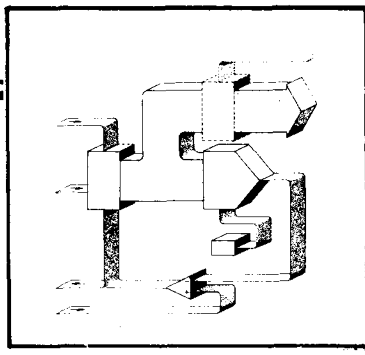
The static and low-frequency operation of the circuits discussed may be fairly easily predicted, so the table below presents only the frequency-response performance. To simplify presentation the same transistors and resistors were used for each circuit. Close tolerance 1k resistors were used throughout and these include the load resistors, not shown in the circuits, inserted at ports C and D. This value gives an incremental voltage gain approaching unity. The complementary transistors employed were 2N3906 and 2N3904 which are p-n-p and n-p-n respectively. These do not necessarily represent the optimum choice, particularly for the op-amp circuits. The supply voltages were set to plus and minus 15V and a TL072 dual op-amp was used.

For all the circuits, the 10V peak to peak sine wave used was obtained from a Wavetek function generator type 142 which exhibited a second harmonic distortion of −57dB that was approximately constant up to 100 kHz. The d.c. component of this signal was reduced to less than 5mV using the generator offset control before directly coupling this source to each circuit under test.

For the circuits in Figs 1, 2 and 3, compensation was included for the 50 ohm generator source resistance as described above. A HP8568B spectrum analyser with a 5k probe was used to measure each frequency component.

Perhaps the most useful measurement to make when assessing full-wave rectifier frequency performance is the rejection of the fundamental frequency. The first column of the table gives the rejection measured at f_o equal to 1 kHz. Columns 2 and 3 gives f_0 for which the fundamental was rejected by 40dB and 30dB respectively. Column 4 gives the frequency f_o for which the fundamental output frequency, equal to $2f_o$, dropped by 0·5dB.

Data conversion



This supplement to January's data conversion feature is the second and final part of a comprehensive list of d-to-a and a-to-d converters and modules.

Digital-to-analogue converters form the first part of this table and analogue-to-digital converters the second. Devices from manufacturers in the first part of the alphabet appeared last month.

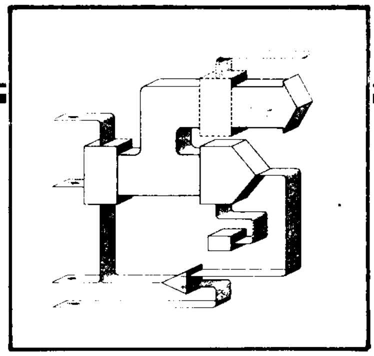
Note that there are some discrepancies between specifications of devices with the same type number but from different manufacturers. This is often because some manufacturers quote the most attractive figures and others quote typical ones, but some devices are intentionally different, having, for example, a shorter conversion time or consuming less power. Where full specifications were available, we chose typical figures for the table.

Burr Brown had a particularly unlucky time last month. The company's data-book supplement arrived too late for us to use, and on top of that, our computer decided to ignore the final section of the data that we did have. Burr Brown also changed addresses on 1 February.

Digital-to-analogue converters

Manufacturer	Device	Bits	Speed	Interface	Tech.	Features
Burr Brown II	DAC70BH	16	<15μ	Par.	Monol.	±0.003% lin. DAC70, I o/p, 14bit monotonic
	DAC72BH	16	<10μ	Par.	Monol.	V/I o/p (10/3μs) DAC70, ±0.003% nonlinearity
	DAC703	16	<8μ	Latch	Hyb.	Int. ref., ±5V output, <±0.003% f.s. lin.
	DAC710	16	350n	Par.	Monol.	Servo-appl., low diff. lin. error near bip. zero
	DAC711	16	<8μ	Par.	Monol.	As DAC710 but voltage output
	DAC800/I	12	300n	Par.	Monol.	Int. ref., 2 I o/p ranges, ±½bit linearity
	DAC800/V	12	<5μ	Par.	Monol.	Int. ref., 5 V o/p ranges, ±½bit linearity
	DAC811	12	<4μ	Proc.	Monol.	Int. ref., 3 V o/p ranges, ±½bit linearity
	DAC812	12	55n	Par.	Hyb.	Int. ref., -10 or ±5mA o/p, ±½bit linearity
	DAC850/I	12	300n	Par.	Monol.	Int. ref., 2 I o/p ranges, -55 to 125°C option
	DAC850/V	12	<5μ	Par.	Monol.	Int. ref., 5 V o/p ranges, -55 to 125°C option
	DAC1200	12	7μ	Par.	Monol.	Int. ref., low cost, ±10V output
	DAC1201	12	7μ	Latch	Monol.	Int. ref., ±10V o.p, 4/8/12/16bit interface
	DAC1600	16	10μ	Par.	Monol.	Int. ref., 13/14bit monotonic, ±10V output
	PCM51/I	16	350n	Par.	Hyb.	Audio 0.0025% f.s. t.h.d., 96dB range, ±5mA o/p
	PCM51/V	16	5μ	Par.	Hyb.	Audio 0.0025% f.s. t.h.d., 96dB range, ±5-±10V o/p
	PCM52	16	3μ	Par.	Monol.	Audio 0.002% f.s. t.h.d., 96dB range, ±5V output
	PCM53/I	16	350n	Par.	Monol.	Aud. 0.002% t.h.d., int. ref., 1mA o/p, 96dB range
	PCM53/V	16	3μ	Par.	Monol.	As PC53/I but ±10V output
	PCM54	16	3μ	Par.	Monol.	Audio, 96dB dynamic range, ±0.001% diff. lin. err.
	PCM55	16	3μ	Par.	Monol.	Audio, similar to PCM54 but low power
MPS	MP370	18	2μ	Latch	Hyb.	Mult., I o/p, 60mW 15V supply, 0.0008% f.s. lin.
	MP377-18	18	20μ	Latch	Hyb.	10 or ±10V o/p, int. ref., 0.0008% f.s. linearity, 0.5W
	MP562	12	1.5μ	Par.	Bip.	±0.006% f.s. error, 2mA o/p, 200mW
	MP3140	14	2μ	Par.	C-mos	Mult., ±0.006% f.s. linearity, I o/p, 30mW, 2ppm gain t.c.
	MP5520	6	3.0μ	Par.	Monol.	=DAC01, 10, ±5 or ±10V o/p opts, int. ref., 250mW
	MP7520	10	500n	Par.	C-mos	Mult., 20mW 5-15V supply, I o/p, ±0.05% f.s. lin.
	MP7521	12	500n	Par.	C-mos	Mult., 20mW 5-15V supply, I o/p, ±0.05% f.s. lin.
	MP7522	10	500n	Proc.	C-mos	Mult., ±0.05% f.s. lin., I o/p, 20mW, serial load
	MP7523	8	100n	Par.	C-mos	Mult., I o/p, 10mW, ±0.05% f.s. linearity
	MP7524	8	100n	Proc.	C-mos	Mult., ±0.05% f.s. linearity, 5-15V supply, 10mW, I out
	MP7528	8x2	80n	Par.	C-mos	Mult., ±0.02% error, I o/p, 15mW, 10ppm gain t.c.
	MP7530	10	500n	Par.	C-mos	Mult., I o/p, 20mW, 5-15V supply, ±0.05% f.s. lin.
	MP7531	12	500n	Par.	C-mos	Mult., I o/p, 20mW, 5-15V supply, ±0.05% f.s. lin.
	MP7533	10	600n	Par.	C-mos	Mult., I o/p, 30mW, 5-15V supply, ±0.05% f.s. lin.
	MP7541	12	1μ	Par.	C-mos	Mult., I o/p, 20mW, ±0.012% f.s. linearity
	MP7542	12	1μ	Proc.	C-mos	I o/p, ±0.012% error, 2ppm gain t.c., 20mW
	MP7543	12	1μ	Ser/par.	C-mos	I o/p, ±0.012% error, 2ppm gain t.c., 20mW
	MP7545	12	1μ	Par.	C-mos	Mult., I o/p, ±0.012% error, 2ppm gain t.c., 20mW
	MP7614	14	2μ	Par.	C-mos	Mult., I o/p, ±0.006% error, 10ppm gain t.c., 40mW
	MP7616	16	2μ	Par.	C-mos	Mult., I o/p, ±0.006% error, 10ppm gain t.c., 40mW
	MP7621	12	1μ	Par.	C-mos	Mult., I o/p, ±0.012% error, 0.5ppm gain t.c., 20mW
	MP7622	12	1μ	Latch	C-mos	Mult., I o/p, ±0.012% error, 2ppm gain t.c., 40mW
	MP7623	12	1μ	Par.	C-mos	Mult., I o/p, ±0.012% error, 0.5ppm gain t.c., 20mW
	MP7628	8	500n	Par.	C-mos	Mult., I o/p, ±0.05% error, 2ppm gain t.c., 25mW
	MP7633	10	500n	Par.	C-mos	Mult., I o/p, ±0.05% error, 2ppm gain t.c., 20mW
	MP7636	16	1μ	Par.	C-mos	Mult., I o/p, ±0.05% error, 2ppm gain t.c., 100mW
	MP9331	16	2μ	Latch	Hyb.	Mult., I o/p, ±0.0008% error, 60mW 15V supply
	MP9377-16	16	20μ	Latch	Hyb.	V o/p, ±0.0008% error, 5ppm gain t.c., int. ref., 500mW
Motorola	AD562	12	1μ	Par.	Bip.	Mult., I o/p, ±½ or ±¼ l.s.b. error opts, range pins
	AD563	12	1.2μ	Par.	Bip.	Mult., I o/p, ±½ or ±¼ l.s.b. err. opts, int. ref. & range pins
	DAC-08	8	150n	-	Bip.	Mult., ±¼ to ±1 l.s.b. error & 135ns opts
	MC1406	6	300n	-	Bip.	Mult., ±½ l.s.b error
	MC1408	8	300n	-	Bip.	Mult., ±½ to ±2 l.s.b. error opts, 5 & -15V supply
	MC1506	6	300n	-	Bip.	Mult., ±½ l.s.b error, wide temp. range
	MC1508	8	300n	-	Bip.	Mult., ±½ to ±2 l.s.b. err. opts, 5 & -15V supp., wide temp. rng
	MC3410	10	250n	-	Bip.	Mult., ±½ or ±1 l.s.b. error opts, 5 & -15V supply
	MC3412	12	400n	-	Bip.	±½ l.s.b. error, ±15V supply, int. apps resistors

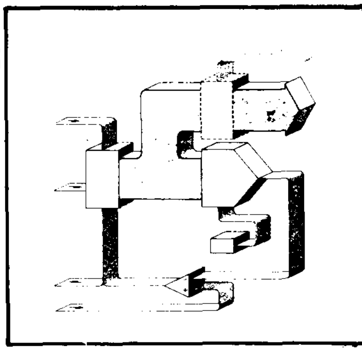
DATA CONVERSION



* Advance information

Manufacturer	Device	Bits	Speed	Interface	Tech.	Features
	MC3510	10	250n	-	Bip.	Mult., ±½ l.s.b. error, 5 & -15V supply wide temp. range
	MC3512	12	400n	-	Bip.	±½ l.s.b. err., ±15V supply, int. apps resistors, wide temp. rng.
	MC6890	8	300n	Proc.	Bip.	±½ l.s.b. error, ±5 to ±10V supply
	MC6890A	8	300n	Proc.	Bip.	±½ l.s.b. error, ±5 to ±10V supply, int. ranging resistors
	MC10318	8	10n	Par.	Bip.	±1 or ±2 l.s.b. error opts, -5.2V supply, e.c.l. i/p
	MC144110	6x4	-	Ser.	C-mos	±2% error, 4.5-15V supply
	MC144111	6x6	-	Ser.	C-mos	±2% error, 4.5-15V supply
Mullard	Am6012	12	250n	Par.	Bip.	Mult., 4mA o/p, ±0.025% error, 230mW
	DAC-08	8	<135n	Par.	Bip.	Mult., I o/p, ±0.1 to ±0.39% f.s. error opts, 33mW
	MC1408-7	8	70n	Par.	Bip.	Mult., I o/p, ±0.39% f.s. error, 5/-15V supply
	MC1408-8	8	70n	Par.	Bip.	Mult., I o/p, ±0.19% f.s. error, 5/-15V supply
	MC1508-8	8	70n	Par.	Bip.	As 1408-8 but wide temperature range
	MC3410	10	250n	Par.	Bip.	Mult., I o/p, ±0.1 & ±0.05% f.s. err. opts, 5/-15V supp.
	MC3510	10	250n	Par.	Bip.	As above but wide temp. range (±0.05% f.s. error)
	NE5018	8	2.3µ	Latch	Bip.	<±0.19% error, ±5 or 10V o/p, internal reference
	NE5019	8	2.3µ	Latch	Bip.	<±0.1% error, ±5 or 10V o/p, internal reference
	NE5020	10	5µ	Proc.	Bip.	±5 or 10V o/p, <±0.1% error, internal reference
	NE5118	8	200n	Latch	Bip.	<±0.19% error, 2mA o/p, internal reference
	NE5119	8	200n	Latch	Bip.	<±0.1% error, 2mA o/p, internal reference
	NE5410	10	250n	Par.	Bip.	Mult., I o/p, <±½ l.s.b. error
	PNA7518 *	8	3n	Par.	N-mos	Video 20MHz samp., 7V o/p, 5V supply, ±½ l.s.b. error
	TDA1540D	14	500n	Ser.	Bip.	Audio 85dB s/n, internal ref., ½ l.s.b. err., 12Mbit/s
NEC	µPD7011-1	8	1µ	Proc./ser.	N-mos	Int. ref., 5V supp., 1mA o/p, 3/4 l.s.b. lin.
Nat. Semicon.	AD7520	10	500n	Par.	C-mos	Mult., I o/p, 20mW, 5-15V supply
	AD7521	12	500n	Par.	C-mos	Mult., I o/p, 20mW, 5-15V supply
	AD7530	10	500n	Par.	C-mos	Mult., I o/p, 20mW, 5-15V supply
	AD7531	12	500n	Par.	C-mos	Mult., I o/p, 20mW, 5-15V supply
	DAC0800	8	100n	Par.	Bip.	Mult., ±5-±15V supp. 33mW, I o/p, ±0.19% f.s. lin.
	DAC0801	8	100n	Par.	Bip.	Mult., ±5-±15V supp. 33mW, I o/p, ±0.39% f.s. lin.
	DAC0802	8	100n	Par.	Bip.	Mult., ±5-±15V supply 33mW, I o/p, ±0.1% f.s. linearity
	DAC0806	8	150n	Par.	Bip.	Mult., ±5-±15V supply 33mW, I o/p, ±0.78% f.s. linearity
	DAC0807	8	150n	Par.	Bip.	Mult., ±5-±15V supp. 33mW, I o/p, ±0.39% f.s. lin.
	DAC0808	8	150n	Par.	Bip.	Mult., ±5-±15V supp. 33mW, I o/p, ±0.19% f.s. lin.
	DAC0830	8	1µ	Proc.	Bip.	4-q. mult., 5-15V supply, 20mW, I o/p, ±0.05% f.s. lin.
	DAC0831	8	1µ	Proc.	Bip.	4-q. mult., 5-15V supply, 20mW, I o/p, ±0.1% f.s. lin.
	DAC0832	8	1µ	Proc.	Bip.	4 q. mult., 5-15V supply, 20mW, I o/p, ±0.2% f.s. lin.
	DAC1000	10	500n	Proc.	Bip.	Mult., 5-15V supply, 20mW, I o/p, ±0.05% f.s. linearity
	DAC1001	10	500n	Proc.	Bip.	Mult., 5-15V supply, 20mW, I o/p, ±0.1% f.s. linearity
	DAC1002	10	500n	Proc.	Bip.	Mult., 5-15V supply, 20mW, I o/p, ±0.2% f.s. linearity
	DAC1006	10	500n	Proc.	Bip.	As 1000 but for right just. data only
	DAC1007	10	500n	Proc.	Bip.	As 1001 but for right just. data only
	DAC1008	10	500n	Proc.	Bip.	As 1002 but for right just. data only
	DAC1020	10	500n	Par.	C-mos	4-q. mult., I o/p, ±0.05% f.s. linearity, 10mW
	DAC1021	10	500n	Par.	C-mos	4-q. mult., I o/p, ±0.1% f.s. linearity, 10mW
	DAC1022	10	500n	Par.	C-mos	4-q. mult., I o/p, ±0.2% f.s. linearity, 10mW
	DAC1200	12	300n	Par.	Bip.	I or V o/p modes, ±0.01% f.s. err., int. ref.
						2.5µs conv. for V o/p, ±12V o/p
	DAC1201	12	300n	Par.	Bip.	I or V o/p modes, ±0.05% f.s. err., int. ref.
						2.5µs conv. for V o/p, ±12V o/p
	DAC1208	12	1µ	Proc.	C-mos	4-q. mult., I o/p, 5-15V supp., ±0.012% f.s. lin., 20mW
	DAC1209	12	1µ	Proc.	C-mos	4-q. mult., I o/p, 5-15V supp., ±0.024% f.s. lin., 20mW
	DAC1210	12	1µ	Proc.	C-mos	4-q. mult., I o/p, 5-15V supp., ±0.05% f.s. linearity, 20mW
	DAC1218	12	1µ	Par.	Bip.	4-q. mult., I o/p, 5-15V supply, ±0.012% f.s. lin, 20mW
	DAC1219	12	1µ	Par.	Bip.	4-q. mult., I o/p, 5-15V supply, ±0.024% f.s. lin, 20mW
	DAC1220	12	500n	Par.	C-mos	4-q. mult., I o/p, ±0.05% f.s. linearity, 10mW
	DAC1221	12	500n	Par.	C-mos	4-q. mult., I o/p, ±0.1% f.s. linearity, 10mW
	DAC1222	12	500n	Par.	C-mos	4-q. mult., I o/p, ±0.2% f.s. linearity, 10mW
	DAC1230	12	1µ	Proc.	C-mos	4-q. mult., I o/p, 5-15V supp., ±0.012% f.s. lin., 20mW
	DAC1231	12	1µ	Proc.	C-mos	4-q. mult., I o/p, 5-15V supp., ±0.024% f.s. lin., 20mW
	DAC1232	12	1µ	Proc.	C-mos	4-q. mult., I o/p, 5-15V supp., ±0.05% f.s. lin., 20mW
	DAC1265	12	200n	Par.	C-mos	±15V supply, ±0.006% linearity, I o/p
	DAC1265A	12	200n	Par.	C-mos	±15V supply, ±0.012% linearity, I o/p
	DAC1280	12	300n	Par.	Bip.	2mA o/p, ±0.024% lin., int. ref. & R's for 5 rngs of V
	DAC1280A	12	300n	Par.	Bip.	2mA o/p, ±0.012% linearity, int. ref. & R's for 5 rngs of V
Plessey	SP9768	8	5n	Par.	Bip.	Mult., ±½ l.s.b. err., I o/p, e.c.l. comp. i/ps, int. ref.
	SP9770	10	12n	Par.	Bip.	Mult., ±½ l.s.b. err., I o/p, e.c.l. comp. i/ps, int. ref.
PMI	DAC8012	12	1µ	Proc.	C-mos	5-15V supply, ±½ or 1 bit linearity options, current output
	PM562	12	1.5µ	Par.	Bip.	±¼ or ±½ l.s.b. linearity options, low power AD562
	PM7524	8	300n	Proc.	C-mos	4-q. mult., 5-15V supp., ±½ or ⅛ l.s.b. lin. opts, 5mW @ 5V
	PM7528	8x2	180n	Proc.	C-mos	Dual 1% match, I o/p, 4-q. mult., 5-15V supply, ±½ l.s.b. lin.
	PM7533	10	600n	Par.	C-mos	4-q. mult., I o/p, ±½ or 1 l.s.b. linearity options,
	PM7541	12	1µ	Par.	C-mos	4-q. mult., I o/p, ±½ l.s.b. linearity, 5-15V supply
	PM7545	12	1µ	Latch	C-mos	Mult., 5-15V supply, ±½ l.s.b. linearity, current output
	PM7645	12	1µ	Latch	C-mos	As above but optimized for 15V supply
STC	UVC3100	10	-	Par.	-	Combined 8bit a-to-d and 10bit d-to-a converter
						with internal references and buffers
						for tv and fast digital processing, 38MHz clock
	UVC3101	8	-	Par.	-	As above but 8bit for both a-to-d & d-to-a conversion
Siemens	SDA8005	8	7n	Par.	Bip.	5.2V supply, e.c.l. input, 40mA output
Silicon Gen.	ZDA1600	16	8µ	-	Mod.	4 V & 2 I o/p ranges, 0.4ppm/°C differential lin. t.c.
	ZDA1800	18	15µ	-	Mod.	4 V & 2 I o/p ranges, 0.2ppm/°C differential lin. t.c.
Sony	CX20051A	10	-	Latch	Bip.	Video 30MHz clock, 62Ω o/p, ±0.8 l.s.b. diff. lin.
TRW	TDC1018	8	7n	Par.	Bip.	125MHz sampling video 75Ω o/p, e.c.l. i/p, ±½l.s.b. lin.
	TDC1334	4x3	10n	Par.	Bip.	100MHz sampling video 75Ω o/p, int. ref., ±⅛ l.s.b. lin.
	TDC1335	4	7n	Par.	Bip.	125MHz sampling video 75Ω o/p, 5V supply, ±⅛ l.s.b. lin.

Analogue-to-digital converters



Manufacturer	Device	Bits	Speed	Interface	Tech	Meth.	Features
Burr Brown II	ADC80H	12	25μ	Ser/par	Hyb.	S.a.	Low power ADC80
	ADC574	12	25μ	Proc.	Hyb.	S.a.	4 input ranges, 150ns bus access time
	ADC600	12	100n	Par.	Hyb.	Flash	Internal s-&-h, >70dB s/n, low power
	ADC674	12	15	Proc.	Hyb.	S.a.	4 input ranges, 150ns bus access time
MPS	MP7550	13	40m	Proc.	C-mos	Q.slo.	Ratiom., 1ppm/C, ±1 l.s.b. acc., 9mW
	MP7570	10	40μ	Proc.	C-mos	S.a.	Ratiom., ±0.05% f.s. acc., 40mW
	MP7574	8	15μ	Proc	C-mos	S.a.	Ratiom., 5V supply, 25mW, internal clock
	MP7581	8x8	66μ	Proc.	C-mos	S.a.	8-inp. mpx, 64-bit mem., ratiom , 40mW
	MP7682	6	33n	Par.	C-mos	Flash	±½bit lin., 15/25/30MHz opts, 150mW, 3-8V supp.
	MP7683	8	100n	Par.	C-mos	Flash	±½bit lin. 5/10MHz opts, 75mW, 3-8V supp.
	MP7684	8	50n	Par.	C-mos	Flash	±½bit lin., 20MHz samp., 3-8V supp., 0.3W
	MP7685	11	500n	Par.	C-mos	Flash	±½bit lin., 2MHz samp., 3-8V supp., 0.15W
Motorola	MC6108	8	2μ	Proc.	Bip.	–	Int. ref., ±5, 5 or 10V i/p, ±½ l.s.b. err.
	MC10315	7	66n	Par.	Bip.	Flash	±½ l.s.b. err., 1-2V p-p i/p, ±5V supp.
	MC10317	7	66n	Par.	Bip.	Flash	As 10315 but expandable to 8bit
	MC10319	8	50n	Par.	Bip.	Flash	±½ l.s.b. err., 2V p-p i/p, Int. gray code
	MC14433	3½dig	40m	Par.	C-mos	2-sl.	±0.05% error, 5-8V supply
	MC14442	8x12	32μ	Proc.	C-mos	S.a.	12 ch. mpx, ±½ l.s.b. err., 5V supp.
	MC14443	8-10	300μ	Proc.	C-mos	1-sl.	Sing. slope, 6-ch. mpx, ±0.3% err., 4-18V supp.
	MC14444	8x16	32μ	Proc.	C-mos	S.a.	16 ch. mpx, ±½ l.s.b. err., 5V supp.
	MC145040	8x11	50μ	Ser.i/o	C-mos	S.a.	Fully serial, Ratiom., ±½ l.s.b. err., 5V supp.
	MC145041	8	50μ	Ser i/o	C-mos	S.a.	As above but internal clock.
	MC145402	13	3μ	Ser.	C-mos	S.a.	Codec chip to 32kHz, 9bit lin., int. ref./s.h.
Mullard	NE5034	8	17μ	Par. 3s	Bip.	S.a.	Internal clock, <±½ l.s.b. err.
	NE5036	6	23μ	Ser. 3s	Bip.	S.a.	<±½ l.s.b. err., 5V supp., 30MΩ typ. i/p, 8 pin i.c.
	NE5037	6	9μ	Par. 3s	Bip.	S.a.	<±½ l.s.b. err., 5V supp., 30MΩ typ. i/p
	PNA7509	7	–	Par. 3s	Bip.	Flash	22MHz samp., O/U flow o/ps, 2's comp. or bin. o/p
NEC	μPD7001	8	140μ	Ser.	C-mos	S.a.	4 ch. mpx, 1GΩ i/p, 5V supp., auto-scale, 0.8% lin.
	μPD7002	10	5m	Proc.	C-mos	Integ.	4 ch. mpx, 1GΩ i/p, 5V supp., auto-scale, 15mW
	μPD7002-1	10	5m	Proc.	C-mos	Integ.	As 7002 but 0.1% f.s. err. not 0.2%
	μPD7003	8	4μ	Proc.	C-mos	Flash	250kHz samp., ±1.25 l.s.b. err., 5V 50mA supp.
	μPD7004	8	100μ	Proc.	C-mos	S.a.	8-ch., par/ser. i/o, 1 l.s.b. lin., 5V supp., 15mW
National Semi.	ADC0800	8	50μ	Proc.	Mos	S.a.	Ratiom., ±5 or 0-10V i/p, ±1bit lin. err.
	ADC0801	8	110μ	Proc.	C-mos	S.a.	Ratiom., int. ck., diff. 5V i/p, 5V supp., ±¼bit err.
	ADC0802/3	8	110μ	Proc.	C-mos	S.a.	Ratiom., int. ck., diff. 5V i/p, 5V supp., ±½bit err.
	ADC0804	8	110μ	Proc.	C-mos	S.a.	Ratiom., int. ck., diff. 5V i/p, 5V supp., ±1bit err.
	ADC0805	8	110μ	Proc.	C-mos	S.a.	As ADC804 but works with 5V reference
	ADC0808	8	100μ	Proc.	C-mos	S.a.	8-ch. mpx, ratiom., 5V supp. & i/p, int. ck., ±½bit err.
	ADC0809	8	100μ	Proc.	C-mos	S.a.	8-ch. mpx, ratiom., 5V supp. & i/p, int. ck., ±1bit err.
	ADC0811	8x11	32μ	Proc./ser.	Bip.	S.a.	11-ch. mpx, 5V supp., simul. ser. i/o, ±½ or 1bit err.
	ADC0816	8	100μ	Proc.	C-mos	S.a.	16-ch. mpx, ratiom., 5V supp. & i/p, int. ck., ±½bit err.
	ADC0817	8	100μ	Proc.	C-mos	S.a.	16-ch. mpx, ratiom., 5V supp. & i/p, int. ck., ±1bit err.
	ADC0831B	8	32μ	Par./ser.	Bip.	S.a.	Ratiom., ser. i/o, 5V diff. i/p, 5-9V supp., ±½bit err.
	ADC0831C	8	32μ	Par./ser.	Bip.	S.a.	Ratiom., ser. i/o, 5V diff. i/p, 5-9V supp., ±1bit err.
	ADC0832B	8	32μ	Par./ser.	Bip.	S.a.	2-ch. mpx, ser. i/o, 5-9V supp., ±½bit err. 5V i/p
	ADC0832C	8	32μ	Par./ser.	Bip.	S.a.	2-ch. mpx, ser. i/o, 5-9V supp., ±1bit err. 5V i/p
	ADC0833B	8	32μ	Par./ser.	Bip.	S.a.	4-ch. mpx, ser. i/o, 5-9V supp., ±½bit err. 5V i/p
	ADC0833C	8	32μ	Par./ser.	Bip.	S.a.	4-ch. mpx, ser. i/o, 5-9V supp., ±1bit err. 5V i/p
	ADC0834B	8	32μ	Par./ser.	Bip.	S.a.	4-ch. mpx, ser. i/o, 5-9V supp., ±½bit err. 5V i/p
	ADC0834C	8	32μ	Par./ser.	Bip.	S.a.	4-ch. mpx, ser. i/o, 5-9V supp., ±1bit err. 5V i/p
	ADC0838B	8	80μ	Par./ser.	Bip.	S.a.	8-ch. mpx, ser. i/o, 5-9V supp., 5V i/p, ±½bit err.
	ADC0838C	8	80μ	Par./ser.	Bip.	S.a.	8-ch. mpx, ser. i/o, 5-9V supp., 5V i/p, ±1bit err.
	ADC0844	8x4	40μ	Proc.	C-mos	S.a.	4-ch. mpx, 5V supp, ratiom., int. ck., 15mW
	ADC0848	8x8	40μ	Proc.	C-mos	S.a.	8-ch. mpx, 5V supp, ratiom., int. ck., 15mW
	ADC1001B	10	200μ	Proc.	C-mos	S.a.	Diff. i/p., ratiom., ref=±Vcc, var. i/p span, ±½bit err.
	ADC1001C	10	200μ	Proc.	C-mos	S.a.	Diff. i/p., ratiom., ref=±Vcc, var. i/p span, ±1bit err.
	ADC1021B	10	200μ	Proc.	C-mos	S.a.	As 1001B but 10bit data bus, not 8bit multiplexed
	ADC1021C	10	200μ	Proc.	C-mos	S.a.	As 1001C but 10bit data bus, not 8bit multiplexed
	ADC1080	10	21μ	Par.	Bip.	S.a.	Diff. i/p., int. ck/ref., 4 i/p rngs, ±½bit err.
	ADC1203	12+1	100μ	Proc.	C-mos	S.a.	12bit + sign in 2 bytes, 5V i/p & supp., 25mW, ±0.012% err.
	ADC1210	12	100μ	Par.	C-mos	S.a.	5 to ±15V supp., 200kΩ i/p with range R's, ±½bit err.
	ADC1211	12	100μ	Par.	C-mos	S.a.	5 to ±15V supp., 200kΩ i/p with range R's, ±1bit err.
	ADC1205	12+1	100μ	Proc.	C-mos	S.a.	12bit + sign in 1 byte, 5V i/p & supp., 25mW, ±0.012% err.
	ADC1280	12	25μ	Par.	Bip.	S.a.	Diff. i/p., int. ck/ref., 4 i/p rngs, ±½bit err.
	ADC3511	3½d	200m	Proc.	–	Integ.	3½-digit, 2V i/p, 5V supp., 0.05% error
	ADC3711	3¾d	400m	Proc.	–	Integ.	3¾-digit, 2V i/p, 5V supp., 0.05% error
	ADD3501	3½d	200m	7s led	–	–	3½-digit led d.v.m. 2V i/p, 5V supp., 0.05% err.
	ADD3701	3¾d	400m	7s led	–	–	3¾-digit led d.v.m., 2V i/p, 5V supp., 0.05% err.
OKI	MSM5204RS	8	82.5μ	Proc.	C-mos	S.a.	Int. s-&-h, ±½ l.s.b. err., 5V 0.9mA supp.
Plessey	SP9754	4	10n	Latch	Bip.	Flash	110MHz samp., e.c.l. comp. o/p, encod. for 8bit exp.
	SP9756-6	6	9n	Latch	Bip.	Flash	110MHz samp., e.c.l. comp. o/p, -5.2V supp., int. ref.
	SP9756-8	6	9n	Latch	Bip.	Flash	As above but expandable to 8bit.
PMI	ADC910	10	6μ	Proc.	Bip.	S.a.	Int. ref./ck, 4 i/p rngs, ±½ l.s.b. err.
Panasonic Ind.	AN6853	4	50n	Par.	Bip.	Flash	20MHz samples, t.t.l. o/p
	AN6856	6	30n	Par.	Bip.	Flash	35MHz samples, e.c.l. o/p
	AN6857	8	30n	Par.	Bip.	Flash	35MHz samples, e.c.l. o/p
	AN6859	10	50n	Par.	Bip.	Flash	20MHz samples, 2V i/p, 53dB quant. noise
STC	UVC3100	8	40n	Par.	Bip.	Flash	Combined 8bit flash a-to-d & 10bit d-to-a conv. with references and buffers for tv & fast dig. proc., 38MHz ck

Manufacturer	Device	Bits	Speed	Interface	Tech	Meth.	Features
	UVC3101	8	40n	Par.	Bip.	Flash	As UVC3101 but 8bit d-to-a converter
Siemens	SDA5200N	6	10n	Par.	Bip.	Flash	100MHz samp., e.c.l. o/p, 0.55W, ±5V supp., ±¼ l.s.b. lin.
	SDA5200S	6	10n	Par.	Bip.	Flash	As 5200N but overflow does not block remaining o/ps
	SDA6020	6	40n	Par.	Bip.	Flash	50MHz samp., e.c.l. o/p, 0.5W, ±5V supp., ±¼ l.s.b. lin.
	SDA8010	8	10n	Par.	Bip.	Flash	100MHz samp., e.c.l. o/p, 1.5W, ±5Vsupp., 1V pk-pk i/p
Silicon Gen.*	ZAD2735	15	5µ	Par.	Bip.	Subrng.	Module, int. ref. & s-&-h, ±½ l.s.b. lin., ±0.005% t.h.d.
	ZAD2736	16	5µ	Par. 3s	Bip.	Subrng.	Module, int. ref. & s-&-h, ±¼ l.s.b. lin., ±0.005% t.h.d.
	ZAD2836	16	3.5µ	Par. 3s	Bip.	Subrng.	Module, int. ref. & s-&-h, ±½ l.s.b. lin., ±0.003% t.h.d.
Siliconix	Si520	8x8	70µ	Proc.	C-mos	S.a.	8-ch. mpx, int. s-&-h, 5V supp., ratiom.
	Si602	8x8	25µ	Proc.	C-mos	S.a.	8-ch. mpx, int. s-&-h, 2.5mW, 10V i/p
	Si860	8x8	25µ	Proc.	C-mos	S.a.	8-ch. mpx, int. s-&-h, 5V supp., ratiom.
Sony	BX1200A	8	50n	Par.	Hyb.	Flash	20MHz samp. vid. hyb., int. s-&-h, e.c.l. o/p
	CXA1016P	8	33n	Par.	Bip.	Flash	30MHz samp. vid., 35pF i/p, 420mW, ±½ l.s.b. err.
	CXA1056P	8	20n	Par.	Bip.	Flash	50MHz samp. vid., 35pF i/p, 550mW, ±½ l.s.b. err.
	CXA1066K	8	20n	Par.	Bip.	Flash	As 20116 but chip-carrier package
	CX20018	16x2	2.2µ	Par./ser.	Bip.	2-sl.	44kHz p.c.m. stereo, 1.7W, 12V supp.
	CX20052A	8	50n	Par.	Bip.	Flash	20MHz samp. vid., 70pF 20µA bias i/p
	CX20116	8	20n	Par.	Bip.	Flash	100MHz samp. vid., 35pF i/p, 1.2W
	CX20220-1	10	50n	Par.	Bip.	Flash	20MHz samp. vid., 350mW
TRW	TDC1046	6	40n	Par.	Bip.	Flash	25MHz samp., 2's comp. or true o/p, ±¼ l.s.b. lin.
Teledyne **	TSC500	4½d	4µ	Compar.	C-mos	Integ.	Auto-z. analogue processor
	TSC800	15+1	0.4	Proc/ser.	C-mos	Integ.	15bit+sign, int. ck/ref., uart ctrl signals
	TSC7109	12+1	0.13	Proc/ser	C-mos	Integ.	12bit+sign, int. ck/ref., uart ctrl signals
	TSC8700	8	1.25m	Latch	C-mos	Integ.	<±½ l.s.b. err., 20mW, strobed or free-run
	TSC8701	10	5m	Latch	C-mos	Integ.	<±½ l.s.b. err., 20mW, strobed or free-run
	TSC8702	12	20m	Latch	C-mos	Integ.	<±½ l.s.b. err., 20mW, strobed or free-run
	TSC8703	8	1.25m	3s latch	C-mos	Integ.	<±½ l.s.b. err., 20mW, strobed or free-run
	TSC8704	10	5m	3s latch	C-mos	Integ.	<±½ l.s.b. err., 20mW, strobed or free-run
	TSC8705	12	20m	3s latch	C-mos	Integ.	<±½ l.s.b. err., 20mW, strobed or free-run
Texas	ADC0801	8	100µ	Proc.	C-mos	S.a.	Ratiom., int. ck., diff. 5V i/p, 5V supp., ±¼bit err.
	ADC0802/3	8	100µ	Proc.	C-mos	S.a.	Ratiom., int. ck., diff. 5V i/p, 5V supp., ±½bit err.
	ADC0804	8	100µ	Proc.	C-mos	S.a.	Ratiom., int. ck., diff. 5V i/p, 5V supp., ±1bit err.
	ADC0805	8	100µ	Proc.	C-mos	S.a.	As ADC804 but works with 5V ref.
	ADC0808	8	100µ	Proc.	C-mos	S.a.	8-ch. mpx, ratiom., 5V supp. & i/p, int. ck., ±½bit err.
	ADC0809	8	100µ	Proc.	C-mos	S.a.	8-ch. mpx, ratiom., 5V supp. & i/p, int. ck., ±1bit err.
	ADC0831A	8	<84µ	Par./ser.	Bip.	S.a.	Ratiom., ser. i/o, 5V diff. i/p, 5-9V supp., ±1bit err.
	ADC0831B	8	<84µ	Par./ser.	Bip.	S.a.	Ratiom., ser. i/o, 5V diff. i/p, 5-9V supp., ±½bit err.
	ADC0832A	8	<84µ	Par./ser.	Bip.	S.a.	2-ch. mpx, ser. i/o, 5V supp., ±1bit err., 15mW
	ADC0832B	8	<84µ	Par./ser.	Bip.	S.a.	2-ch. mpx, ser. i/o, 5-9V supp., ±½bit err. 15mW
	ADC0834A	8	<84µ	Par./ser.	Bip.	S.a.	4-ch. mpx, ser. i/o, 5-9V supp., ±1bit err. 15mW
	ADC0834B	8	<84µ	Par./ser.	Bip.	S.a.	4-ch. mpx, ser. i/o, 5-9V supp., ±½bit err. 15mW
	ADC0838A	8	<84µ	Par./ser.	Bip.	S.a.	8-ch. mpx, ser. i/o, 5-9V supp., 15mW, ±1bit err.
	ADC0838B	8	<84µ	Par./ser.	Bip.	S.a.	8-ch. mpx, ser. i/o, 5-9V supp., 15mW, ±½bit err.
	TL0808	8	100µ	Par. 3s	C-mos	S.a.	8-ch. As ADC0808 but 300µW
	TL0809	8	100µ	Par. 3s	C=mos	S.a.	As TL0808 but ±1 l.s.b. err. not ±½ l.s.b.
	TL500	13	-	-	C-mos	2-sl.	Analogue proc. for TL502, TL503 or micro.
	TL501	10-12	-	-	C-mos	2-sl.	Analogue proc. for TL502, TL503 or micro.
	TL502	4½d	-	-	C-mos	-	4½-dig. 7-seg. o/p dig. processor
	TL503	-	-	-	C-mos	-	Mpx b.c.d. o/p dig. processor
	TL505	8-10	-	-	C-mos	2-sl.	Analogue proc. for TL502, TL503 or micro.
	TL507	7	-	Proc.	C-mos	1-sl.	P.w.m. converter, 5-18V supply, 8 pin
	TL530	8	300µ	Par. 3s	C-mos	S.a.	10 anal. & 6 anal./dig. i/ps, ±½ l.s.b. err., 15mW
	TL531	8	300µ	Par. 3s	C-mos	S.a.	10 anal. & 6 anal./dig. i/ps, ±1 l.s.b. err., 15mW
	TLC532A	8	15µ	Par. 3s	L/C	S.a.	5 anal. & 6 anal./dig. i/ps, ±½ l.s.b. err., 6mW typ.
	TLC533A	8	30µ	Par. 3s	L/C	S.a.	5 anal. & 6 anal./dig. i/ps, ±½ l.s.b. err., 6mW typ.
	TLC540	8	12µ	Ser.	L/C	S.a.	11 analogue i/ps, ±½ l.s.b. err., 6mW typ.
	TLC541	8	26µ	Ser.	L/C	S.a.	11 analogue i/ps, ±½ l.s.b. err., 6mW typ.
	TLC549	8	19µ	Ser.	L/C	S.a.	±½ l.s.b. err., 6mW typ., 8pin device.

* Silicon General's subsidiary, Analog Solutions, designs a-to-d and d-to-a converters to suit applications.
** Teledyne, Intersil and Ferranti manufacture a-to-d converters for driving display devices.

Data conversion product suppliers and manufacturers

Addresses

Burr Brown
1 Millfield House
Woodshot's Meadow
Watford
Herts WD1 8YX

Design Consultancy
West Hill
The Street
Cottesey
Norwich NR8 5DF

Dialogue Distribution
(Maxim)
Watchmoor Rd
Camberley
Surrey GU15 3AQ

Electrovalue
(Siemens)
28 St Judes Rd
Engelfield Green
Egham
Surrey TW20 0BH

Honeywell Control Systems
Honeywell Hse
Charles Sq.
Bracknell
Berks RG12 1EB

Micro Power Sys.
Orion House
49 High St.
Addlestone
Surrey KT15 1TU

Micro Networks
see Unitrode

Motorola
York Hse
Empire Way
Wembley
Middx HA9 0PR

Mullard
Torrington Place
London WC1E 7HD

National Semicon.
301 Harpur Centre
Horne Lane
Bedford MK40 1TR

Maxim, see Dialogue

Manhattan Skyline
(Oki, Sony)
Manhattan House
Bridge Rd.
Maidenhead
Berks SL6 8DB

NEC
116 Stevenston St.
New Stevenston
Motherwell
Lanarks ML1 4LT

Panasonic
280 Bath Rd
Slough
Berks SL1 6JG

Plessey Semicons
Crowdys Hill Estate
Kembrey Street
Swindon
Wilts SN2 6BA

PMI
Bourns Electronics
Hodford Hse.
17 High St.
Hounslow
Middx TW3 1TE

Siemens
Components Group
Siemens Hse.
Windmill Rd.
Sunbury-on-Thames
Middx.

Silicon General
17 Bridge St.
Leatherhead
Surrey KT22 8BL

Silinconix
Morriston
Swansea SA6 6NE

Hakuto International
(Sony)
Hakuto Hse.
159a Chase Side
Enfield
Middx. EN2 0PW

STC Mercator
South Denes
Gt. Yarmouth
Norfolk NR30 3PX

SSI (Teledyne)
Dawson Hse
128 Carshalton Rd
Sutton
Surrey SM1 4RS

Teknis (Intech)
Teknis Hse.
Meadrow
Godalming
Surrey GU7 3HQ

Teledyne
Heathrow House
Bath Rd.
Cranford
Hounslow
Middx.

Texas
Hawke Electronics
Amotex Hse.
45 Hanworth Rd.
Sunbury-on-Thames
Middx.

Thame Components
(Nat. Semicon.,
Maxim, AMD)
Thame Park Rd.
Thame
Oxon OX9 3XD

TRW
HiTek Electronics
Beadle Trading Est.
Ditton Walk
Cambridge CB5 8QD

Unitrode
6 Cresswell Park
Blackheath
London SE3 9RD

Tech. Inquiry Service
Texas Instruments Ltd.
Manton Lane
Bedford MK41 7PA

COMPACT disc DIGITAL AUDIO

Digital audio editing

by J.R. Watkinson

Master recordings for cutting Compact Discs are made on videocassettes using a pcm adaptor. This two-part article looks at additional equipment needed to edit the final master recording.

One of the most important aspects of Compact Disc cutting to appreciate is that the entire process takes place in the digital domain. The final disc contains left and right sound samples which arrive at the converters in the player at 44.1kHz; some 400 million 16-bit samples in a 75 minute recording. The value of every sample on the disc has to be provided by the master tape, and if the quality of the disc pressing is adequate, there will be no difference in sound quality between playing the compact disc or playing the master tape into the same converters.

The disc cutting process is independent of musical content, and the responsibility for the subjective quality of the recording falls on those who make the master tape. The duration of each musical piece, the length of any pauses between pieces, and the relative levels of the pieces on the disc have to be determined at the time of mastering. The master tape will be made from source tapes which may each contain only some of the pieces required on the final disc, in any order. The recordings will vary in level, and some may contain several unsatisfactory re-takes of a passage.

The purpose of the digital editor is to take each piece, and insert sections from re-takes to correct errors, and then to assemble the pieces in the right order, with appropriate pauses between and with the correct relative levels, to create the master tape. All of this is done by copying in the digital domain; the source tapes will not need to be changed in any way, and no degradation results from the additional stage of copying. The master tape will also have contiguous timecode.

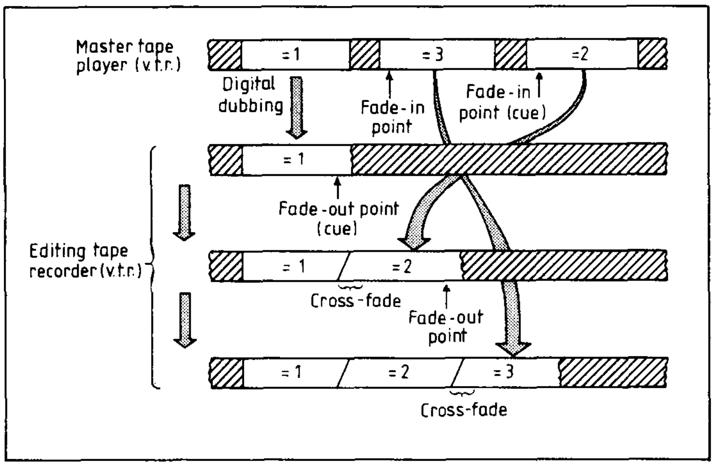


Fig. 1. An editor performs a series of assembles to produce a master tape from source tapes.

Digital editors work by assembling, a term which has the same meaning as in the context of video recording, where new material is attached to the end of a previous recording without any loss of sync.

A master tape is made up by assembling from source tapes, Fig. 1. Clearly one recorder and one player are necessary in an editing system. Where there are many different source tapes, a system with two players will work faster because one can be locating the next piece whilst the other assembles.

As in video recording, digital audio edits are controlled using timecode on the tape cassettes. Editing *per se* can be done using drop-frame timecode or true frame timecode, but the CD cutter will reject a master with drop-frame code, and this will not be mentioned further. The time code used is SMPTE standard. Fig. 2. This stores hours, minutes, seconds and frames as binary-coded decimal, which is serially encoded along with user bits into a fm channel code recorded on one of the linear

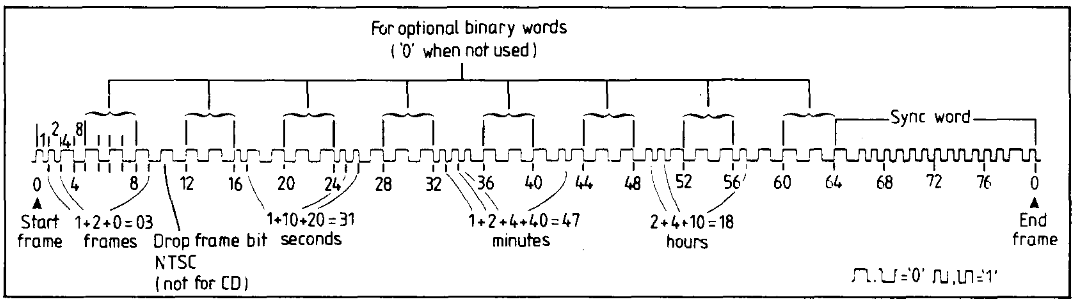


Fig. 2. In SMPTE standard timecode, frame number and time are stored as eight b.c.d. symbols. There is also space for 32 user defined bits. Code repeats every frame.

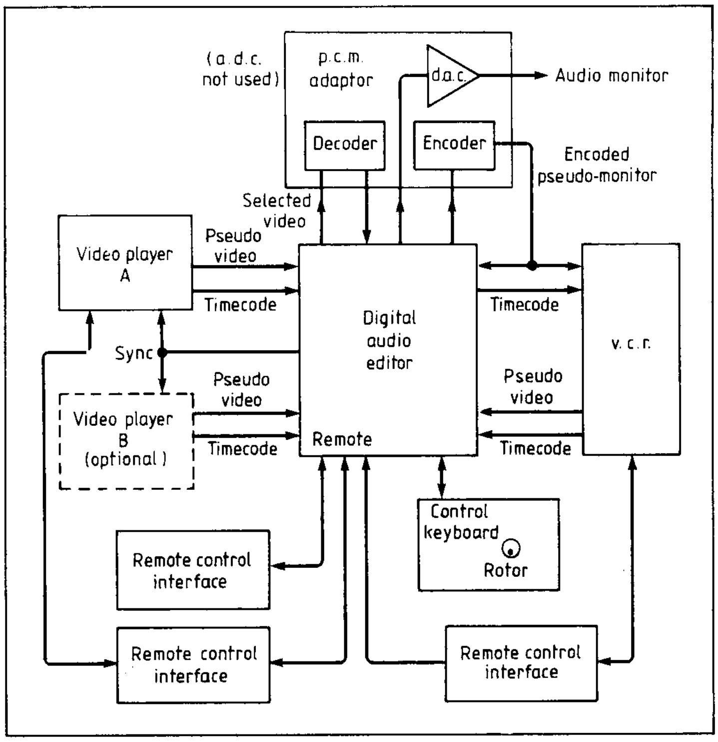


Fig. 3. Block diagram of edit system. The editor makes use of a p.c.m. adaptor for tape encoding and decoding, and for monitoring; second player is optional

audio tracks of the video-cassette. An exception to this is the JVC editor which buries timecode as a field count code on one of the pseudo-video lines recorded by the rotary heads. The user-bits are not specified in the SMPTE standard, but a common use in digital audio is to record the take or session number.

Editing is performed in two basic steps, edit point location and assembling. The edit point is located under manual control, whereas assembly takes place automatically. Edit point location will be described here the assembly mechanism will be detailed in a second article.

Edit point location

The digital audio editor makes use of the p.c.m. adaptor described in an earlier article. The encode and decode sections are used for assembling, and the d.a.c. is used for monitoring. The a.d.c. is not normally used during editing, but in principle assembly could be done with an analogue tape recorder connected to the converter, provided that the a.t.r. has a timecode track and the editor had supporting software.

The units of an edit complex interconnect as in the illustration (Fig. 3). The two or three v.c.rs all have remote control, sync, timecode and video replay connections. And the recorder has additional record video and timecode connections. The three sections of the p.c.m. adaptor are connected to the editor individually. The timing generator in the adaptor synchronizes the entire system with locked 44.1kHz and 525/60 sync.

In video editing, the location of the edit points is easy, as these will always be at a vertical interval in the video waveform and the only care needed is with colour framing. Furthermore, the professional video recorders permit the picture to be viewed at any speed[1], so that the editor can rock the tape back and forward to find the precise edit point.

In digital audio, the industrial v.c.rs do not have the track following systems of their video counterparts, so the heads only follow the tape tracks correctly at exactly normal speed. Even if track following were provided, the problems of data seperation in the presence of timing vatiations are severe. Furthermore, the accuracy to which the edit point must be found in audio is much greater than the frame boundary accuracy needed in video. A video frame lasts 33.3ms (525/60), whereas audio needs to be edited to an accuracy of about 00ms.

Digital audio editors simulate the process of edit point location in analogue audio recorders and video recorders. As the v.c.r. can only play at normal speed, the area of the edit point is transferred into a memory, and the precise edit point is located by accessing the memory, and which can be done at variable speed.

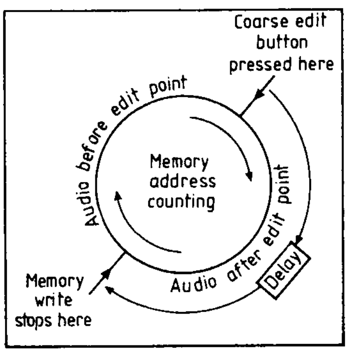
Figure 4 shows how the area of the edit point is transferred to memory. The v.c.r. is set into play, and the operator listens to offtape samples via the d.a.c. in the p.c.m. adaptor. The same samples are continuously written into a memory within the editor, addressed by a counter that repeatedly overflows to give the memory a ring structure rather like a timebase corrector. When the operator hears the approximate area in which the edit point is required, pressing a button will stop the memory writing one-half of the memory capacity later. The effect of this is that the memory contains a section of the recording which is symmetrical about the coarse edit point.

Typically, an operator needs to hear about 30 seconds of audio to be able to mentally synchronize to the rhythm and anticipate the edit point. In a stereo system, this represents a storage requirement of about $2 \times 44100 \times 30 = 2.6$ million samples, or more than five megabytes. This represents a lot of memory and significant cost. To reduce the size of the memory needed, most editors use some form of data reduction or companding [2,3].

One obvious step is to add left and right sample values to obtain a monophonic signal, giving a factor of two saving. A further reduction of memory can be obtained by reducing the sampling rate. It is easy to reduce the sampling rate by a factor that is some power of two as output samples will coincide in time with input samples, thus simplifying the circuitry. Typically the sampling rate will be halved, reducing the bandwidth of the audio to 10 on 11kHz. Sampling-rate reduction cannot be performed by simply discarding alternate samples: this is the equivalent of sampling at half the rate and results in aliasing, as shown in Fig.5.

It is necessary to use a digital filter. finite impulse response filter is highly suitable, and the impulse response chosen will be that of a perfect 11kHz low-pass analogue filter. This is shown in Fig. 6, superimposed

Fig. 4. A ring memory that overwrites allows storage of samples before and after the course edit point.



on the sampling rate. The response is a sinx/x curve having zeros at integral multiples of the two sample periods, therefore to produce a filtered sample it is necessary to add to the central sample 0.64 of the adjacent samples, 0.21 of the samples three periods away and 0.13 of the samples five periods away, and so forth, and divide by some normalizing factor.

As the sinx/x curve is infinite, it will have to be truncated and this will cause some distortion. The filter can be conveniently implemented with a ram that allows transversal access to several samples and a rom that contains coefficients, both of which feed a multiplier accumulator. It is possible to eliminate the multiplier if the impulse response is distorted so that all coefficients are 1/2, 1/4, 1/8 etc, as multiplication by these factors can be done by bit shifting.

The final stage of data reduction will be to convert to a floating-point notation, where the value is expressed to reduced accuracy, but over the same range, as a mantissa and an exponent. In true floating-point notation, every mantissa has its own exponent, but in digital audio samples adjacent samples tend to have similar exponents. Thus one common exponent can be used for, typically, four mantissae — known as floating-point block coding. If a seven-bit mantissa is used, four of these plus one common four-bit exponent can be stored in four bytes.

Floating-point block coding is simply performed. A set of four input samples is loaded into four shift registers. These are shifted up until a 'one' appears in the m.s.b. of one of the registers. The number of shifts determines the common exponent, and the top seven bits of each register become the mantissae. Floating-point block coding reduced memory requirement by a further factor of two. Fig. 7 shows the complete reduction process which illustrates the factor of eight reduction in memory size to 650Kbyte.

Once the recording is in the memory, it can be accessed at leisure, and the v.c.r. plays no further part in the edit point location. The v.c.r. will typically perform a partial unthread so that the tape no longer contacts the rotating thread. If the memory address is supplied by a counter which is clocked at an appropriate rate, the edit area can be replaced at normal speed, or at half speed, repeatedly.

To simulate the usual methods of locating an edit point the operator is provided with a handwheel or rotor, and the memory address will change at a rate proportional to the speed with which the rotor is turned, and in the same direction. Thus the sound can be heard backward or forward at any speed, and the effect is exactly that of manually rocking an analogue tape past the a.t.r. heads.

Simple as it sounds, there are difficulties to overcome. The human hand cannot turn the rotor smoothly enough to enable the output to address the memory directly; this would result in annoying flutter. A phase-locked loop is necessary to damp rotor speed fluctuations and provide a stable average frequency. Further, it is necessary to feed the monitor d.a.c. at the standard sampling rate of 44.1kHz otherwise the reconstruction process would be impaired because sampling sidebands could pass the filter. An interpolator or sampling-rate converter is necessary to produce a constant sample-rate whatever the rotor speed. This follows the conversion from floating to fixed point.

Look at a typical rotor output, Fig. 8. The rotor carries a grating which moves over a fixed grating which has non-

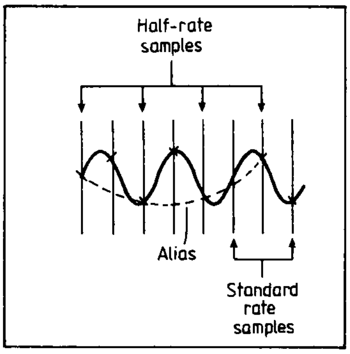


Fig. 5. If a high frequency is sampled and then alternate samples dropped, the result is aliasing, where the output is a difference frequency between the signal and the new sampling rate (shown as dashed line).

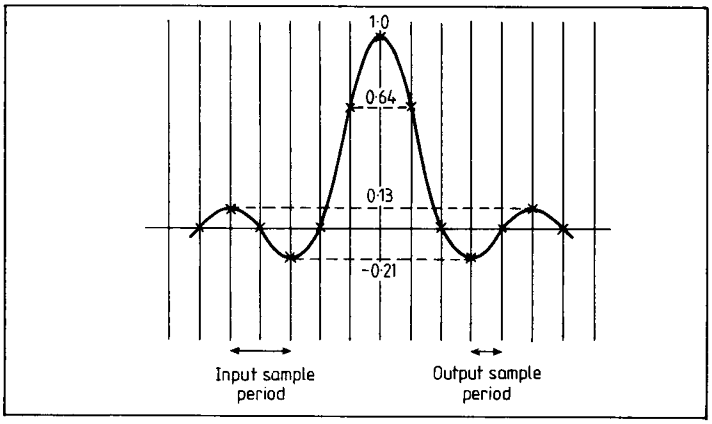


Fig. 6. Impulse response of an 11kHz low-pass filter is zero at two sample period spacing on the output, one sample spacing on the input. As so many coefficients are zero, the filter can be realised with little hardware.

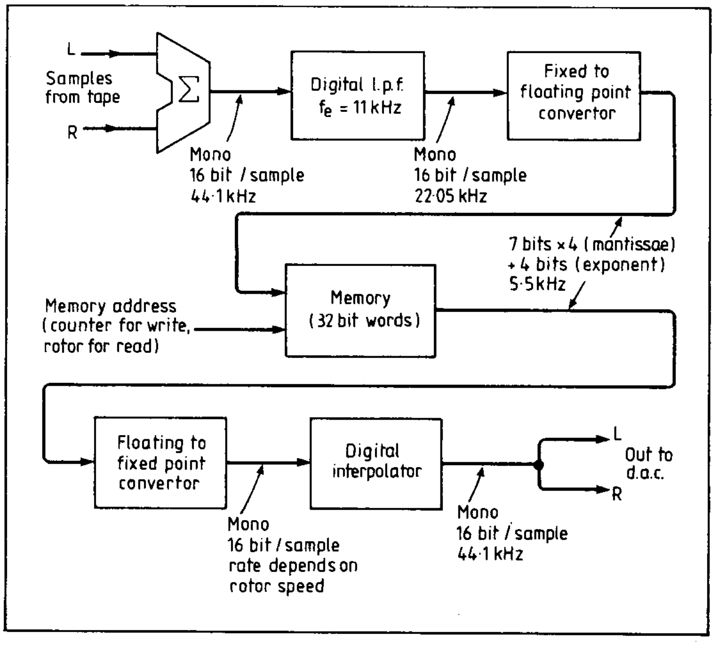


Fig. 7. to economize on memory size, sampling rate is reduced, and floating-point block coding used to write the memory. Reverse process is necessary on reading the memory.

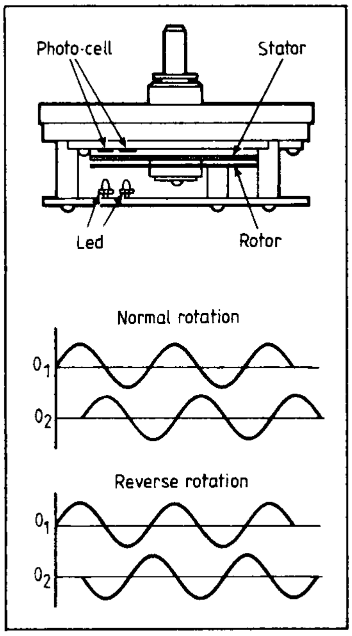


Fig. 8. Fixed and rotating gratings produce Moiré fringes that are detected by two light paths as quadrature sinusoids. Relative phase determines the direction, and frequency is proportional to speed of rotation.

paralled bars. The resultant moiré patterns are picked up by two light paths positioned to produce outputs in quadrature. By comparing the phase of the two outputs, the direction of rotation can be determined. The frequency of one of the outputs is fed to the digital p.l.l. to be multiplied up to the required rate. The loop works as follows: A counter fed from a stable high frequency measures the period of the rotor output. The period is fed to an accumulator which multiplies by repeatedly adding new inputs to previous outputs.

If the accumulator output were fed to a presettable counter, the counter would overflow at a new value each time the accumulator operated, resulting in an output rate similar to the input rate. However, by bit-shifting the accumulator output, the period fed to the output counter can be divided by powers of two, thus raising the output frequency by powers of two. There is a clear parallel with analogue loops in that the multiplication of frequency achieved is a function of the division ratio. The accumulator averages input periods, reducing flutter.

The resultant clock now drives the memory address bus, and samples are read out at arbitrary rate. The samples are expanded to fixed point by using the exponent to shift down the mantissae in sets of four. These fixed-point samples are the input to the sampling rate converter, similar to the oversampling digital filter described in a previous article, though more filter phases are needed. The interpolated sample values then pass the p.c.m. adaptor, where the d.a.c. returns them to the analogue domain for monitoring.

Samples that go to make the master tape never pass through the rate reduction and companding processes: the sound quality of the edit point location system is not particularly impressive.

Pressing the coarse edit point button it stores the timecode at that point. As the rotor turns the memory address is monitored as this changes the time code. When the rotor is at the chosen point, the timecode will have been updated by the distance from the course-point memory centre to the current address. Internal to the editor, the edit point has now been determined to great accuracy, and is stored as hours, minutes, seconds, frames and position within the frame.

Before assembly can be performed two edit points must be determined, the out-point at the end of the previously recorded signal and the in-point at the beginning of the new signal. The editor's microprocessor stores these two points as the precise timecodes of the two tapes. They will be used to control the assemble process.

Part 2 outlines the assembly process and shows how the greater accuracy required in digital audio editing results in processes that are considerably more complex than their video counterparts.

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Understanding Radar by Henry W. Cole. Collins, 267 pages, soft covers, £9.95. A comprehensive and very readable guide to radar technology, concentrating on its applications in aviation. The aim is to give radar users a clearer understanding of how their systems work and what limitations they have. Sections cover basic techniques, primary radar, secondary surveillance radar and methods of display.

IEEE Transactions on Microwave Theory and Techniques, volume MTT-32, No.9; ISSN 0018-9480. Special hard-bound issue to mark the centenary of the IEEE, with 29 articles and invited papers on microwaves, most of them with a historical perspective. Topics include the multiple rediscovery of the waveguide, microwave printed circuits and i.cs, the evolution of low-noise techniques, microwave ferrites, GaAs fet digital i.cs, instrumentation, medical applications, astronomy and power transmission by radio waves. A section on U.S. patent abstracts contains excerpts from a selection of landmark patents ranging from 1898 to 1970. Details from the IEEE Service Center, 445 Hoes Lane, Piscataway, New Jersey 08854.

Dictionary of Electronics and Computer Abbreviations by P.R. Brown. Butterworths, 237 pages, hard covers, £19. Wide-ranging guide to the mass of jargon spawned by the electronic age — the U.S. variety as well as the home-grown. Inevitably there a few omissions and errors (for instance, CP/M 2.0 is *not* the latest version). At the end, is an appendix on batteries, which includes a cross-reference chart to different manufacturers' type numbers. Though useful, it gives the impression of having strayed from someone else's book. Rather expensive.

Analog-Digital Conversion Handbook by staff of Analog Devices. Prentice Hall, 669 pages plus a bibliography and index, hard covers, £20: from Analog Devices, Central Avenue, East Molesey, Surrey KT8 0SN. Essential manual for circuit designers hungering for more after our current survey. Design examples are largely based on AD's own devices, but most of the information given is universal. This third edition has been expanded and updated with seven new chapters.

Human responses to 'intelligent' machines

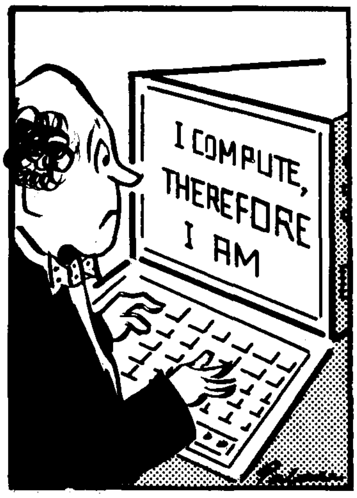
Tom Ivall

A discussion on the interaction of living beings with dead, but cognitively-active, matter

When we describe a person as intelligent we mean that he or she has the ability to understand subtle or complex situations, problems, processes, distinctions, explanations, hypotheses and so forth. More specifically, we might assume this person would obtain high scores in solving the artificial problems set in intelligence (IQ) tests.

If we disagree with the concept of intelligence as something which is innate, fixed and measurable, we might accept the dynamic model proposed by Piaget. In this, intelligence is seen as a complex hierarchy of information-processing skills underlying a state of adaptive equilibrium achieved between the person and the environment.

But whatever the view of intelligence — and it is certainly a controversial subject — evidence of its existence can only be obtained through some kind of performance. A person asleep or in a coma might well be intelligent, but we wouldn't know this until he woke up and we could assess his performance by criteria of some kind.



'Intelligent' machines

There is no doubt that machines — in manufacturing industry, public services and the home — are becoming more 'intelligent', in so far as this description refers to their performance. They can not only do more, in both kinds and quantity of tasks, but also function more autonomously than was possible, say, a century ago. Two basic inventions are mainly responsible. One is closed-loop control; the other is programming by software.

Closed-loop control started from simple mechanical devices like the steam-engine governor and developed through electronics to complex systems which can be adaptive, predictive, multi-variable, and make use of optimization techniques such as computer-implemented dynamic programming. They will function not only deterministically, where all required information is permanently available, but also stochastically, where the laws are probabilistic and future behaviour cannot be calculated from past and present information.

Programming of machines started with mechanical sequence control, became electrical in the form of hand-set switches and plugged connections — an early form of firmware — and finally, through the computer revolution, extended to software. Programmable controllers, with software using conditional branching instructions which allow decisions to be implemented in response to sensed data or states, are now commonplace in manufacturing industry. We also have automated plants relying on centralized or distributed computer control and second-generation robots with visual and tactile sensing systems which extend outside of the robot to include the workpieces, materials and tools being manipulated.

In the future we can expect to see both closed-loop and programming systems supplemented by artificial intelligence (AI). Expert systems in the form of software are already available commercially and these have been one means of introducing interference into information processing — to be distinguished from implication, which is essentially a logical operator (if... then...) in deductive logic.

The man-made interface

Human interaction with machines — at the so-called man-machine interface (m.m.i) — has developed partly in step with the nature of the machines themselves and partly in response to the demands of the tasks to be performed. The levers, handles and steam pressure gauges of the Industrial Revolution gave way to the switches, rheostats, indicators and meters of electrically driven machinery. Now the m.m.i. is increasingly provided by keyboards, v.d.us and printers. In turn, these data entry and display devices are being supplemented and to some extent replaced by voice input and output, based on digital speech recognition and synthesis systems.

So the picture that emerges of human interaction with machines is one of increasing involvement between the living organisms and the dead matter. First, the human mental processes are dealing with increasingly complex machine functions with higher and higher levels of internal organization. And the interaction is taking place through increasingly sophisticated arrangements between human sensors and effectors and their corresponding devices in the machine.

It would seem that ergonomics and human-factors engineering, as it is called, will have to be extended to include the psychology as well as the physiology of *Homo sapiens.* (The subject could perhaps be called 'psychonomics' if the word did not already have an established meaning in pyschology.)

Certainly, with this greater intimacy between man and machine, the feeling of the human being towards the machine — his 'perceptions' of it, to use a current buzz-word — are likely to become increasingly important relative to his purely rational knowledge of its workings. For example, now that speech synthesizers are beginning to be used to provide output information, the 'tone of voice' of the artificial speech might have a certain character which could elicit an emotional response in the human listener — or at least a sense of what 'that sort of voice' means.

This could effect the efficiency of information transfer and the working harmony desirable between the human and the machine. A tone of voice which could be interpreted as posh, unctuous, patronising etc., or had a foreign or class-related accent, could easily prove counter-productive. Anyone who has formed a mental picture of an unknown person just from a voice at the other end of a telephone line will understand this problem.

Uneasy and happy relationships

A fairly common experience nowadays of interacting with a machine is that of speaking to a telephone answering machine. Emotional reactions vary with people, but a feeling of unease or embarrassment is often reported. Rationally we know we are really speaking to a piece of magnetic recording material, but we try to behave naturally, as in a normal telephone conversation, for the sake of the end result. This is difficult, because of the absence of the normally expected audible responses from the other end, if only "yes", "no" or an occasional meaningful grunt. The consequence is a mild mental conflict caused by instinctive behaviour being thwarted by the pressure of the rational requirement (to leave a clear message), which psychiatrists tell us is the basis of neurosis.

But not all interaction with machines is like this. The late Dr C.R. Evans, a psychologist at the National Physical Laboratory, reported some experiments with computer-aided medical diagnosis in which in which certain patients actually preferred interacting with a computer, in a question-and-answer duologue, to interacting with a human doctor.[1] (this must also say something about certain doctors.)

Dorinda Bath of Nottingham University, in experiments with autistic and retarded children, found that a simple voice synthesizer which they could play with like a toy acted as a 'catalyst' for assisting interpersonal relations.[2] (Autistic children withdraw from human contact and prefer things to people.)

Such experiences are, of course, typical subject matter for psychology — in the sense of man's interaction with his social and physical environment — and studies in this field keep up with the changing nature of machines. In the UK such research on human-machine interaction is being done at Loughborough University and at the Medical Research Council's Applied Psychology Unit at Cambridge. There is, however, another level of man-machine interaction which is intellectual rather than emotional, concerned with content rather than manner, with the message rather than the medium. This is the interaction between the human and the machine as two information processing systems, differently constructed but using the same symbols, syntax, semantics and logical conventions.

As such it is appropritate subject for cognitive psychology — the scientific study of thinking — but also has considerable underpinnings in the philosophy of mind.

Philosophical viewpoints

It may well be helpful to consider these philosophical underpinnings of 'cognitive man-machine interaction' as a background to the empirical psychological work needed to achieve good results from advanced automation. There are two traditional and related philosophical problems which seem to be relevant: the 'problem of other minds' and the broader 'mind-body problem'. And these lead on eventually to a modern theory in the philosophy of mind, called functionalism, which attempts to solve these problems.

An 'intelligent' machine which demonstrates very well the relevance of these two problems and the theory is a computer running a program expressly written to stimulate human thinking and verbal communication. A famous example is a program called Eliza, composed by Prof. J Weizenbaum at the Massachusetts Institute of Technology, USA, with which a person can 'converse' in English. (It was named after Eliza Doolittle in Bernard Shaw's *Pygmalion.*)[3]

The program has a language analysis section and a 'script' section — providing a set of rules which enable the program to 'improvise' around a given topic. What was remarkable about the performance of this program was that it created a very strong illusion in many different people 'conversing' with it that the computer 'understood' the conversation. Those who knew it was only a computer program soon forgot the realities of the situation, as in watching a good piece of theatre. Those who knew little or nothing about computers insisted firmly that the machine understood them.

The 'Turing test' again

Eliza would have passed with flying colours the once-famous 'Turing test'. Alan Turing, the mathematician and pioneer of computer science, proposed that a stringent test of a programmed computer's abilities would be for an observer to judge if the responses it printed-out in answer to questions were produced by a machine or by a human being.[4] If the observer could not tell any difference then the machine could justifiably be described as thinking.

The question of whether machines can 'think' has already been discussed at great length. What is significant about the 'Turing test' in the present context is that it parallels, in its person-to-machine relationship, the person-to-person relationship in the above-mentioned 'problem of other minds'. The essence of this philosophical problem is that we can only be absolutely sure of the existence of our own minds. Our evidence is obtained by the process of introspection, or inwardly observing our own mental processes and stream of consciousness. There is no way in which we can demonstrate objectively the existence of minds (or consciousness or mental processes) in other persons. All that we can do objectively is to observe the external behaviour of other persons. From this we can only infer, that they too have minds possibly similar to your own.

Monism versus dualism

One possible solution to this problem is that we are mistaken in conceiving the mind as a separate, ghostly entity, different in kind from the body because it cannot be described as an arrangement of atoms and molecules in space-time. This is the position of 'monism' in philosophy — that there is only one basic reality. It is in opposition to 'dualism', which posits two separate entities, consciousness and matter, or mind and body, which somehow interact or function in step with each other. Nowadays, scientifically minded people tend to favour monism because they cannot see any means by which a separate, non-physical mind could interact with the body and its brain (e.g. as in conation, or 'willing').

Ironically it was Descartes, the great originator of scientific methods of investigation (including Cartesian co-ordinates, of course) who was responsible for dualism in the first place. In seeking to find a system of enquiry free from the inhibiting scholastic traditions and theological dogmas of the time, he proposed as a basis the absolute certainty we have of knowing that we are thinking. Even if we are deluded or deceived by God or the Devil in *what* we think, we still know for sure that we *are* thinking. And if thinking is taking place there must be something doing it.

Hence the famous *Cogito, ergo sum* (I think, therefore I am). This approach, of course, is what produced the modern scientific dichotomy between subjective experience and objective description, the observer outside of and detached from the thing observed. It is central to our whole way of proceeding in science and technology.

Answers to dualism

Unfortunately, this peculiar split between consciousness and the external world (which is foreign to Eastern ways of thought) also produced the concept of the duality of mind and body, and philosophers have been occupied with the 'mind-body problem' mentioned above ever since. Various monist solutions to the problem have been proposed. Spinoza thought everything was unified through God/Nature, Hobbes that everything was just matter, Berkeley that everything was just mind. Leibnitz, who among many other activities designed calculating machines, suggested that everything, whether mental or physical, was composed of certain entities which he called monads. More recently, James argued that consciousness was a function, not an entitity, and Ryle that the concept of mind as a "ghost in the machine" was a mistake in categorization.

James was among other scientist-philosophers including Mach and Russell who supported a theory of 'neutral' monism — neutral in the sense that it centred neither exclusively on consciousness nor exclusively on matter. It

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Computer aids in electronic design

Computers are playing an increasingly larger role in the lives of electronics engineers. Right through the industry from school pupils and apprentices through to the integrated-circuit manufacturer there is a design tool that will aid the user to produce anything from a simple circuit or p.c.b. layout to a highly complex multilayer p.c.b. or i.c.

What is CAD?

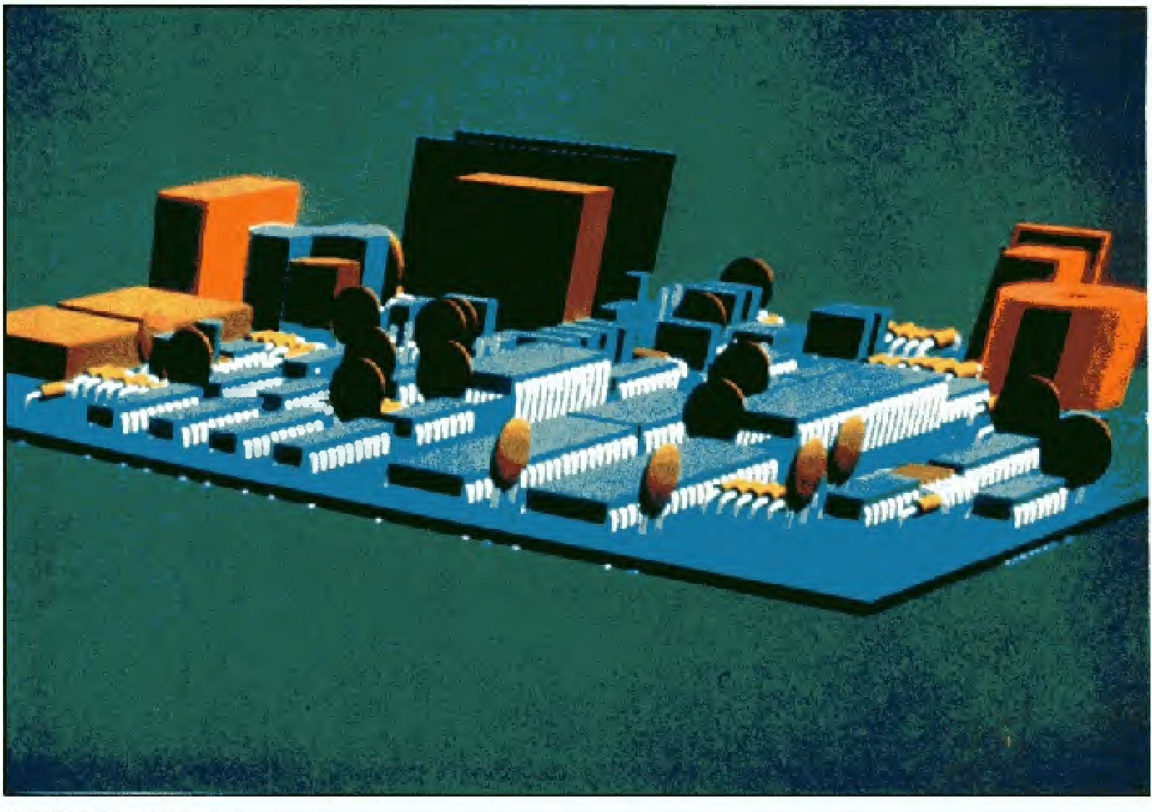
The term computer-aided design has been used to describe many functions. At the simplest level it is used purely to indicate the physical design of a p.c.b. or circuit where the designer has to provide all the component positions and the computer system can plot and interconnect them as indicated by the user. This is more like an electronic drawing board and can perhaps be better designated 'computer-aided draughting'. At the next level, the computer can be provided with a circuit and organise the components and position them to give an optimum layout design. At the ultimate level, especially in i.c. design, the user enters the inputs and the required outputs and the computer can then follow specific rules to design the circuit that will meet the requirements.

Not only can computers aid the designer to produce the circuit, but they can produce the necessary masks or etching patterns and be linked to automatic machinery to produce the finished product. They can provide a list of parts. They can simulate the circuit and check that it will perform the required tasks. I.c. design tools can also check that the circuit obeys the design rules and that stray capacitance will not damage the circuit.

Testing is an integral part of the design process. Design systems can test the circuit before it physically exists and then use the same test patterns to test the prototype and final product when it has been made. There is also a wide range of computer-aided testing (c.a.t.) equipment which is a separate branch in its own right.

Unlike some of our recent surveys, it is not our intention to provide a comprehensive list of all the services available but to present examples from the range and indicate the sort of tools that are available to aid in design tasks at the various levels; from linear circuit analysis on a home micro to a complete semi-custom design and manufacturing plant.

This 3-dimensional model of a p.c.b. was produced by Computervision's ElectroCADDS system interfaced with a mechanical modelling package through the CADDS connect interface.



Michael A. Lloyd, B.Sc.

Prototyping gate-arrays in seven days

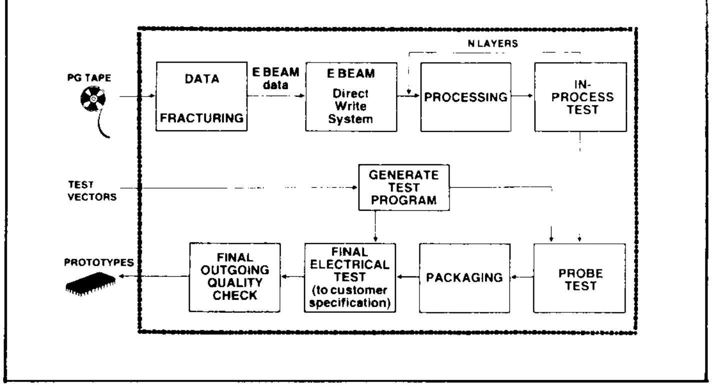
Using electron-beam direct-write facilities it is possible to achieve a turn-around time for prototypes of seven days. This method encourages innovation and reduces costs and risks.

A gate-array logic device consists of a number of logic cells which are uncommitted to any specific purpose. The addition of a metallic layer (or layers) interconnects the cells and creates an integrated circuit specially made for a specific task. Circuits so produced are called semi-custom or application-specific i.cs.

The advantages of semi-custom i.cs are that they can reduce cost, are of smaller size, faster, use less power with design security and reliability. Their disadvantages are the costs incurred by the delays in the development phase; waiting for prototypes from a standard production line; the question of whether to breadboard the circuit; and the difficulties of obtaining small quantities of prototypes for evaluation and test modelling.

Most of the disadvantages stem from the fact that the semi-custom i.c. is manufactured on a production line which is devised for the large-scale production of standard i.cs. These can be stored in large numbers and are available for prototyping whenever required. Semi-custom i.cs need to be produced in relatively small quantities of many different designs and are specially manufactured for a specific user. The methods described here can overcome the disadvantages and provide a quick turn-around for application-specific i.cs.

The flow through the E-beam manufacturing process.



The manufacturing facility

A fully integrated facility is able to design, produce the metallic-layer pattern (in our example by E-beam lithography) and complete all tests before packaging the circuit. The system is intentionally designed for low-volume production with an upper limit of a few hundred i.cs. Greater volume can be achieved by the conventional mass-production facility. With this in mind, the design produced can be transferred to a high-volume factory if required.

The design stage, in our example, is carried out on a Vax minicomputer. Three complete design packages are installed from Plessey, Ferranti and Mullard/Philips. The schematic layout can also be produced on an independent work-station and transferred to the Vax-based system. Most of the parameters needed in the creation of a new design can be set up and performed automatically, using computer-aided manufacturing techniques. The design package checks that the proposed device complies with certain rules of construction, rather like building regulations, and its electrical and capacitative performance are checked automatically. The software can simulate the device and also provide test patterns for testing the finished i.c. On completion, the design output is converted to a binary pattern of x-y co-ordinates (Cambridge binary format) to drive the E-beam. This is performed by specially developed software and is known as "pattern processing". E-beam lithography eliminates the need to produce a mask for the metallization process.

E-beam processing

The Cambridge EBMF 6.5 is an E-beam device which is capable of "writing" on up to ten wafers in one run. Different designs can be written on different parts of the same wafer and it is even possible to mix wafers from different manufacturers which will have a different 'floorplan'.

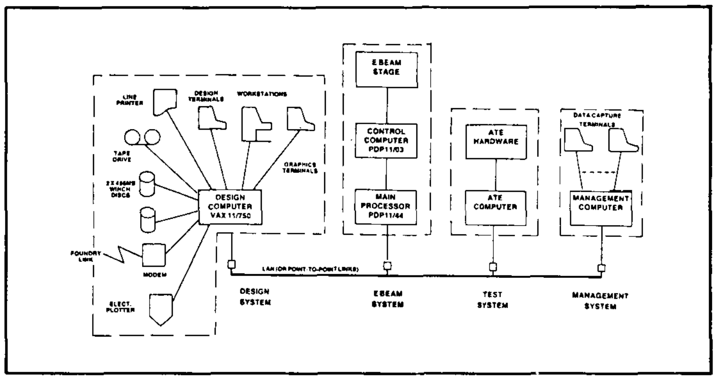
A wafer is coated with an etch-resistant layer which will be sensitive to the electron beam when exposed. It is then positioned in the machine which must be aligned to recognise features on the wafer. No special alignment marks are provided, so the software must learn to recognise specific features. Once aligned the E-beam devices sets up an x-y co-ordinate system across the wafer. Each die (which will end up as the integrated circuit) is individually exposed. If necessary, the machine can automatically compensate for any distortion inherent in the base wafer. Test patterns can also be made on the wafer to check the wafer quality and processing tolerances.

Once the wafer has been exposed, the rest of the process, i.e. resist development and etching is conventional. Wet etch techniques are used for geometries of more than 3μm. Below this, a dry or plasma etch is used. If the array being produced has more than one metal layer, at least two more runs through the E-beam are required to expose 'via' holes in the oxide dielectric and the pattern for the second layer of metal. The facility can also deposit oxide and polyiomide layers, and sputter metal.

The processed wafer is probe tested and sawn into dice. Each good die is bonded into a ceramic package (d.i.l, chip-carrier and pin-grid arrays can all be handled). A final test and inspection is carried out, using a Vanwall tester and other bench-top test equipment. Test patterns and outputs from the computer circuit simulators can be downloaded directly from the development system, thus minimizing the time taken. Testing is an essential part of the whole process.

The time taken from pattern processing to completion of the tested prototype is around seven days for a single level metal device. The system can cope with bi-polar and c-mos devices. Future developments will include 2μm geometry, double-layer metal c-mos arrays and e.c.l. Eventually full processing of standard cell devices in small quantities is expected.

The system described here has been used successfully by one company and the facilities and techniques are to be transferred to a new company being started by the author.



The complete design and production computer chain for an E-beam facility.

PC-based workstation

Computer-aided engineering is a concept introduced by Daisy Systems to describe their design workstation for electronics. The founders of Daisy, Aryeh Finegold and Dave Stamm, had themselves been designers at Intel, and had recognised the need for specialised tools for electronics engineers.

The more general term, computer-aided design (c.a.d.) is, says Daisy, really only applied to draughting aids, and could be retitled 'computer-aided drawing'. Computer-aided engineering, on the other hand, assists the designer in all aspects of the task — from the initial conception of the design through to the generation of production information, whether this is an integrated circuit or a p.c.b. Further, all the data is held in a common database, so that all the stages of the design process are fully compatible and integrated.

The CAE workstation

Over recent years a number of advanced c.a.e. systems have been developed, some of which run on special dedicated computers with special features designed to optimize performance of specific tasks. Daisy produce such equipment, and have evolved a line of c.a.e. workstations. These provide for the full spectrum of engineering tasks from entry of a circuit diagram, through logic simulation, timing verification, gate-array layout, full integrated circuit design and printed circuit board layout. It is also possible to generate test data and verification patterns so that the finished device can be plugged into a 'Physical modelling extension' (PMX) and tested by the system that was used to design them.

One such system is the Daisy Logician, a graphics workstation that can be equipped to perform any of the above tasks, and upgraded with dedicated high-speed processor where a very high performance is required. The central processor use in the Logician is the Intel iAPX286.

When IBM introduced a version of the Personal Computer called the AT, which also used a '286, Daisy saw the opportunity to produce a system which could provide the abilities of the Logician to the PC AT.

The Personal Logician

This is essentially an upgrade to the IBM PC AT that extends memory size and provides a high-resolution graphics controller and monitor in order to run the Daisy suite of electronic design tools. Fully expanded the system can carry 3.25Mbyte of ram and the disc capacity can be increased to 88Mbytes. This provides all the facilities of the big brother Logician but on a smaller scale.

A special high-speed graphics controller was developed for the AT which provided a resolution of 1024 by 1024 panels in colour or monochrome, and addi-

Daisy's Personal Logician can be used as the grpahics terminal to this MicroVax-based Logician VX.

tionally emulated the standard IBM screen format. This was designed to fit a standard plug-in IBM card, so that it fits into the AT and allows standard IBM applications to be run as well as the design tools. The display provides clear graphics, but in addition is suitable for the operating system used by the design suite; Daisy-DNIX, a version of Unix that is enhanced to include 'windows' to display different application programs on the screen at the same time, and 'mouse'-controlled pop-up menus which are easy to use.

Further recent enhancements to the Personal Logician include physical modelling, (PMX), formerly only available on the full Logician and 'mixed mode' simulations using Daisy's Advanced Behavioral Description Language (DABL). For printed circuit design, there is a bi-directional software interface to allow a Daisy database to communicate with p.c.b. layout systems from other makers including SCICards, Computervision and Racal-Redac.

Networking

The Personal Logician may be used on its own and is considered to be suitable for the smaller company, or used for a specific project. However an Ethernet interface is available and the software is compatible with all other Daisy workstations and can use any resources available on the system. So a system could consist of a number of PL-ATs communicating over Ethernet to each other and a Mega-Logician simulation accelerator, or a MegaGatemaster gate-array layout workstation, allowing individual engineers to develop their own design locally and then share the more expensive resource of the accelerated tools.

Completing the Daisy chain

The latest development in the Daisy line is the integration of the DEC MicroVax with the Daisy design suite allowing engineers in a larger company to access Vax-based software on a MicroVax, or even a mainframe, from a Daisy terminal. Thus a complete range of design tools is available, from the relatively low-cost single-user workstation to a fully integrated corporate design environment.
Daisy Systems, Basing View, Basingstoke, Hants RG21 2HG. **EWW 250.**

Linear circuit analysis on a BBC micro

The pulse response of a transformer-coupled low-pass filter; simulated by the circuit analysis program.

After reading an article in *Wirleless World*, 'Circuit analysis by a small computer' by A.S. Beasley (WW Feb, 1980), David Markie had a two-year project to create a system that would implement the ideas set out in the article. It is in fact a whole suite of programs, included on two discs. The first disc is a 'system' disc with the software to run the tests; the second disc is a 'user' disc containing example circuits and results.

The system works exactly as if the circuit was physically built and then tested with a sinewave sweep oscillator at the input and an oscilloscope or phase-sensitive a.c. voltmeter at the output.

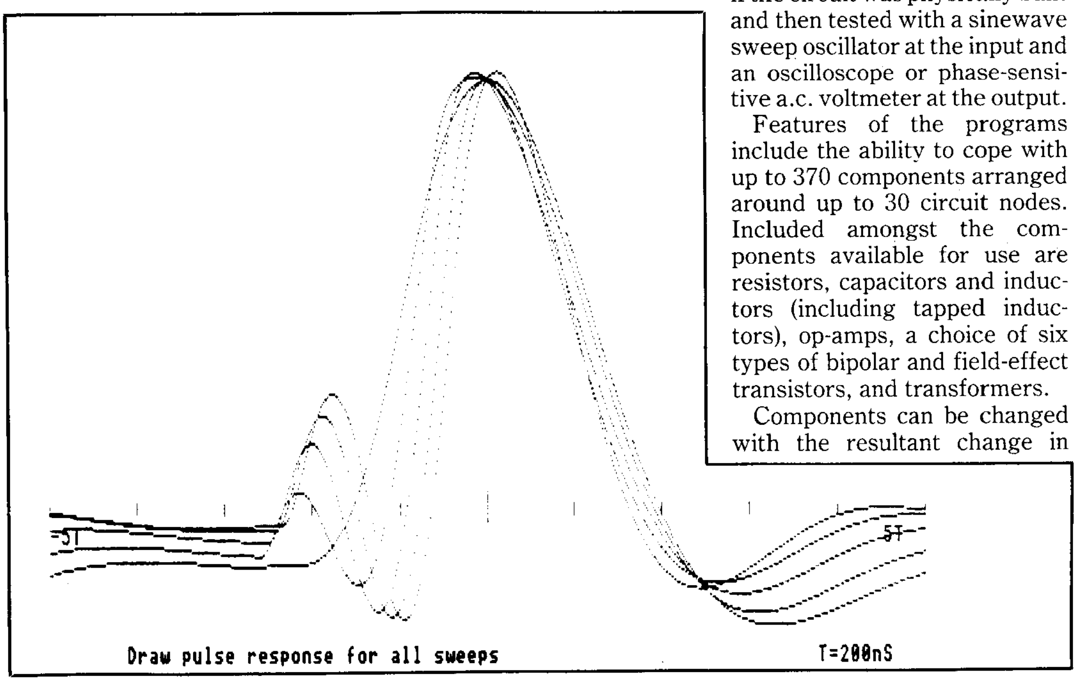
Features of the programs include the ability to cope with up to 370 components arranged around up to 30 circuit nodes. Included amongst the components available for use are resistors, capacitors and inductors (including tapped inductors), op-amps, a choice of six types of bipolar and field-effect transistors, and transformers.

Components can be changed with the resultant change in response displayed very quickly. The frequency sweep to test the circuit can be linear or logarithmic and up to 50 frequency steps can be plotted; scaled automatically or manually. Gain and phase-shift of a circuit are calculated as well as the magnitude and phase of the input and output impedances and the group delay. Transient response is tested with a "raised cosine" test pulse.

Up to five sets of test results can be displayed simultaneously and the output, in graphic or tabular form can be dumped to a printer.

Much of the software is written in Basic but to speed the calculations, machine code is used in critical sections of the program. All the software is interlinked and menu driven so that the system is easy to use. It is also provided with a comprehensive user guide.

The price of the discs and manual is £60 inclusive and can be obtained from David Markie, Markie Enterprises, 17 Percy Road, London W12. EWW **251**



Simulation is the name of the game

Integrated circuit and p.c.b. designs are getting larger and more complex, increasing the need for better design and testing tools. At the same time, product life-cycles are shrinking, increasing the need to produce new i.cs rapidly. HHB-Softron, who specialise in logic simulation, claim that general purpose computers are too slow for thorough logic simulators and systems, and that logic simulation for p.c.bs requires extensive libraries of models and specific components. Fault simulation shows how well a circuit can be tested but requires even more computer time than 'good' circuit simulation.

Combining both computer-aided design and computer aided testing into one integrated whole, HHB-Softron market a range of Cadat systems. The simulation software consists of logic and fault simulation, worst case timing, switch level simulators and automatic test generation. Hardware includes accelerators, chip modellers and prototype testers.

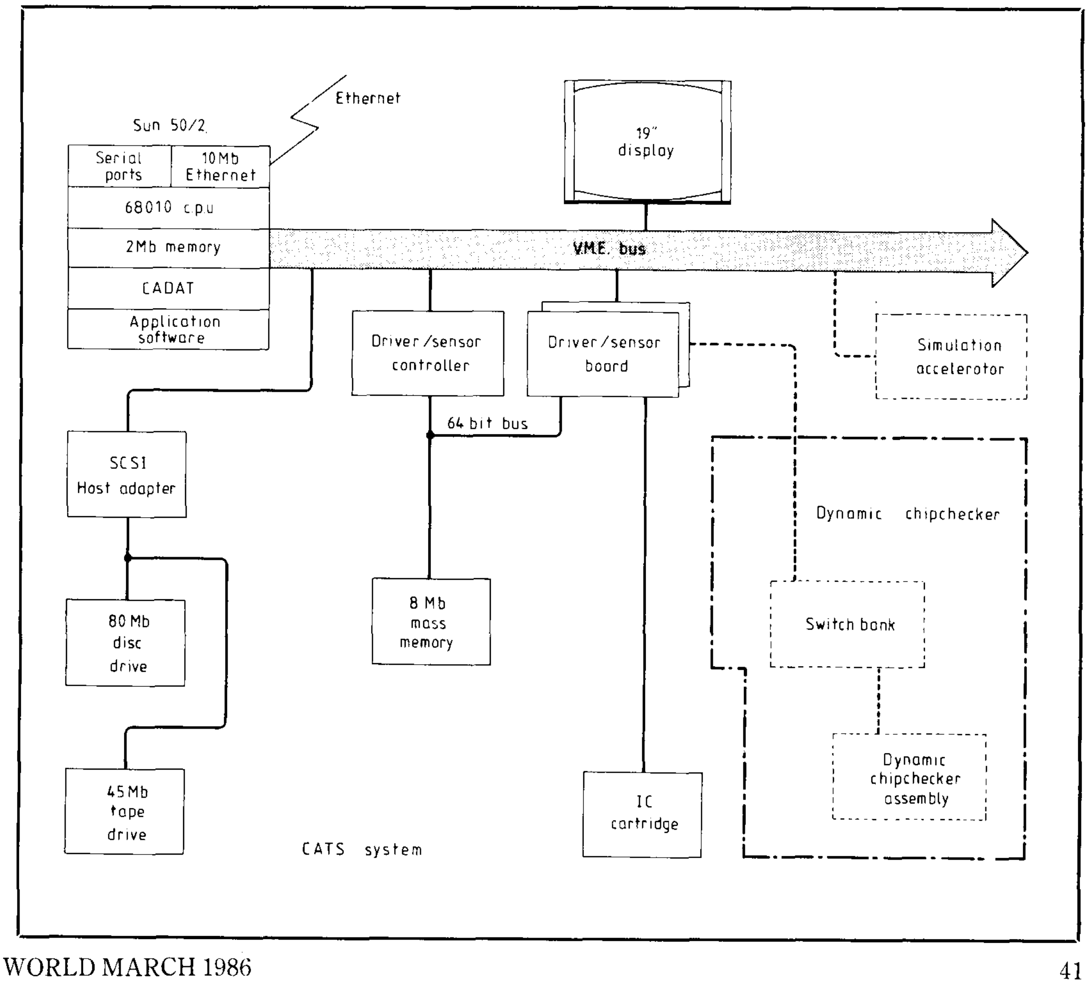
At the basic level, Personal Cadat offers simulation on an IBM PC/AT computer. It can verify the performance of complex logic designs with up to 3000 devices. It can simulate mos devices with charge decay and switch-level analysis. Timing with minimum and maximum tolerances is simulated. The system uses its own high-level computer language to provide the 'probes' and 'stimuli' for the virtual circuit under test. The output is displayed in logic analyser wave diagrams. HHB stress their ability to model "real world" conditions by developing timing algorithms.

Cadat is available for use at many different levels and is also incorporated into Cats (computer-aided test simulation) which offers a stand-alone system for all stages of circuit development and production. A circuit description is generated at an engineering workstation and is then passed to the Cats system for analysis. Cats combines simulation, evaluation and prototype verification. It is designed for its specific tasks and is very fast. It incorporates a hardware evaluator and includes a library of software and hardware l.s.i. and v.l.s.i. devices which can be used in a variety of hardware/software combinations as if they were all physically present. The system includes post-processors to generate the test patterns for automatic test equipment. Networking enables the linking together of several workstation nodes with shared resources.

Optional additions include a "dynamic chipchecker" which makes it possible for the design or test engineer to exercise prototype devices at the workstation. It offers testing at rates of up ti 8MHz and can provide up to 256,000 test vectors. It can test devices with up to 608 i/o pins and has a sense resolution of 1ns. Another option is an accelerator which comes on a plug-in board for the Cats system. It can speed up processing over 500 times compared with Cadat used on a Vax11/780 computer.

HHB-Softron products are incorporated into many c.a.e. workstation systems including those of Mentor Graphics, Racal/Redac, Factron and Futurenet and, partly to offer local support for these companies, the American company has set up a European sales/support centre at HHB Europe, 10-12 Oxford Road, Marlow, Bucks SL7 2NL. **EWW 253**

Complete flowchart of the HHB Cats system.



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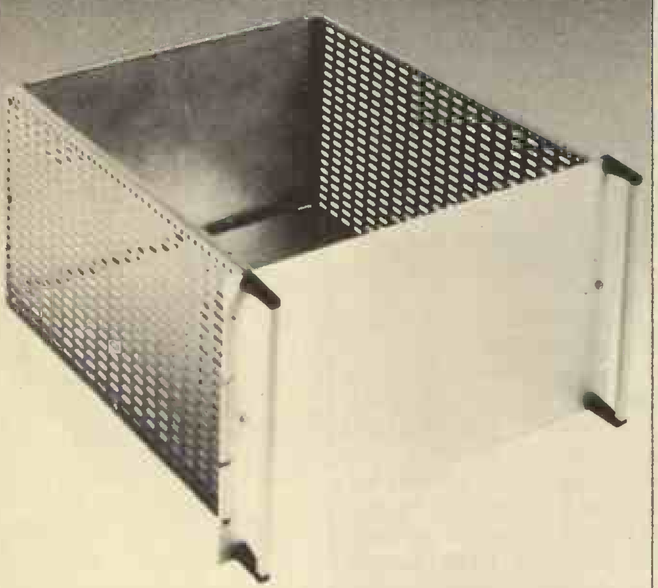

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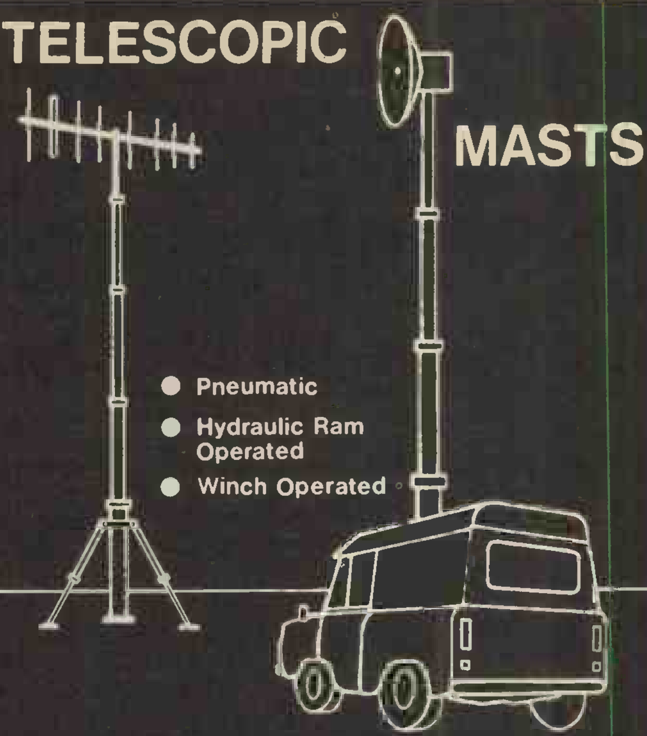

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A look inside: computer-aided metallurgy

by L. Paul Goodwin, B.Sc. A.M.I.E.E.

Paul Goodwin is telecommunications engineer with Mott, Hay & Anderson, a Croydon firm of consulting engineers. He joined Marconi Avionics in 1978 as a student apprentice, and subsequently graduated from London's City University with an honours degree in electrical and electronic engineering.
He is a licensed radio amateur (G6ANO), and hobbies include computer programming, audio and video production.

Video processing and computer technology combine to allow automatic analysis of metallic structures

In the field of metallurgy it is possible to obtain a great deal of information about a sample of metal by the physical (magnified) picture it presents to the outside world. Using a magnification of 300, and a short etching and polishing process, it is possible to clearly see boundaries and occlusions within the metal.

With the aid of a video camera, the image displayed provides enough detail to allow an electronic solution to the problem of carrying out measurements on the metal structure. Although this article deals with a specific case of measurement, the techniques outlined are equally applicable to any situation where a measurement between black and white transitions on a video image is required.

What information can be obtained from such a picture? The task of digitizing a video picture in real time is both complicated and costly. In a situation where an image is moving this approach would be necessary, but where the image is fixed — such as that seen by the microscope and camera combination — a fast conversion process is not justified.

For any kind of computer analysis of a picture, conversion from the analogue video signal to the equivalent digital representation is required. Analysing the information available and the results required, it is only necessary to determine at any instant whether the video signal is either above or below a given voltage threshold. It is then easy to discriminate between light and dark areas of the displayed picture, thus identifying the crystal boundaries, by appropriate choice of the threshold. Applying this to a practical system a video signal can be processed with a simple high-speed comparator circuit at a fraction of the cost of a high-speed 'flash' a-to-d converter.

The hardware described is designed to be as flexible as possible in its interface requirements to allow interface to almost any computer system or even to a dedicated microprocessor system. The hardware presents its data output in eight-bit parallel form, with no parity but with three control lines to provide a form of parity checking and device handshaking. Complete parity checking is not included because the error in the final result produced by a 'bit error' doesn't justify the extra work required to implement the process.

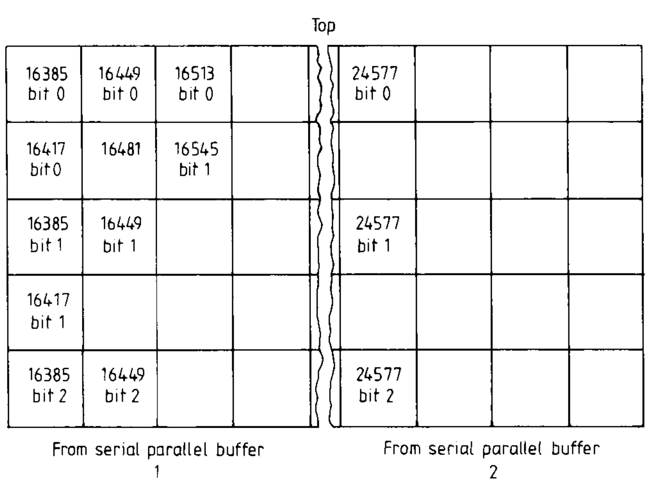
The system is designed to provide the following information about the crystal structure

- maximum width of the lar gest crystal sample (the largest distance between two black areas in the picture)
- maximum height of any lat tice element in the picture
- number of occlusions in the area under investigation
- size (both length and width) of the largest occlusion.

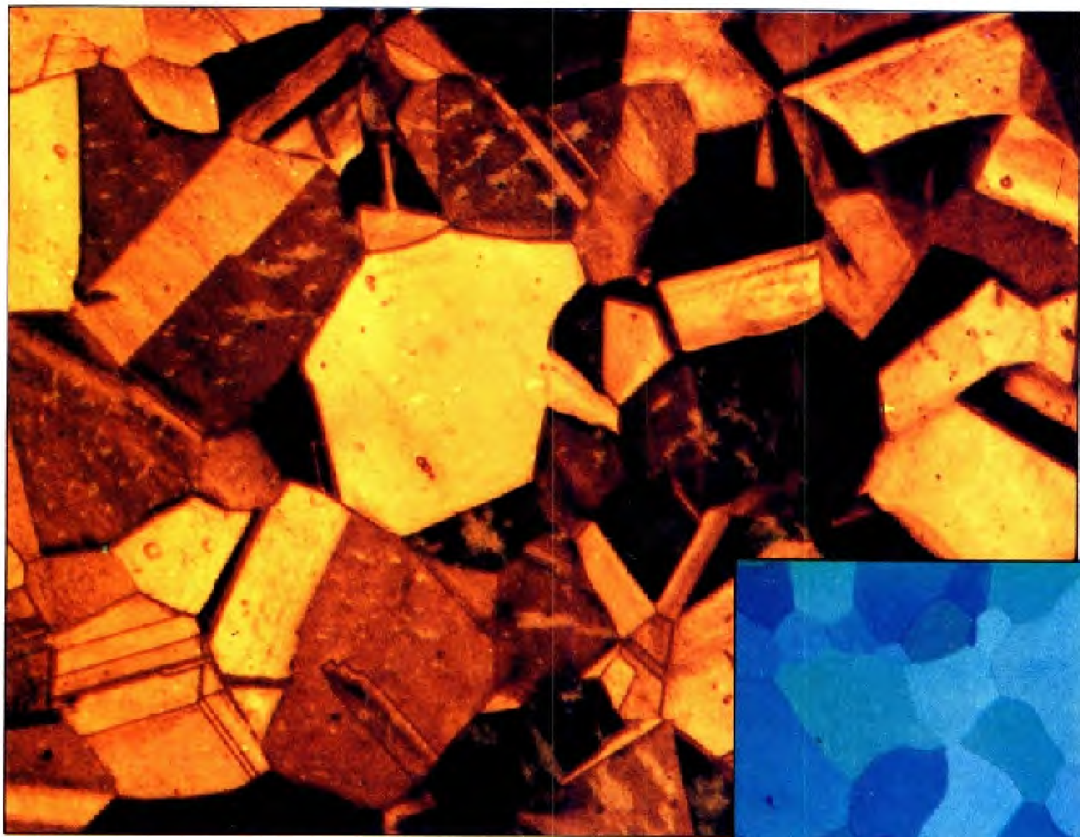
The final hardware system provides a matrix of 512 by 256 elements, allowing convenient storage of data with a reasonably high resolution system.

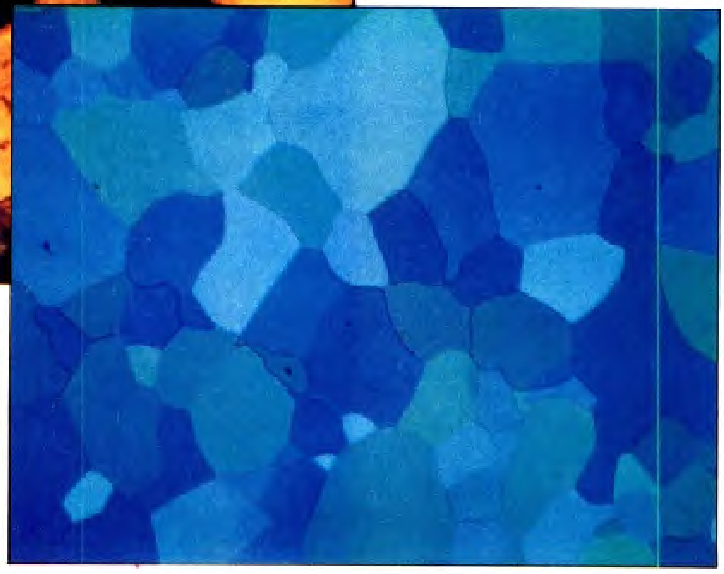
Using the criteria outline it is

1



For the resolution required the memory size of the computer must be at least 16Kbytes for data storage plus any memory required for the input and analysis program. Because only one bit is used to define any one element's state, use is made of a serial-to-parallel converter to produce a normal eight-bit word-length for input to the processor. Diagram 1 shows the way in which the information is stored in the memory of the computer.



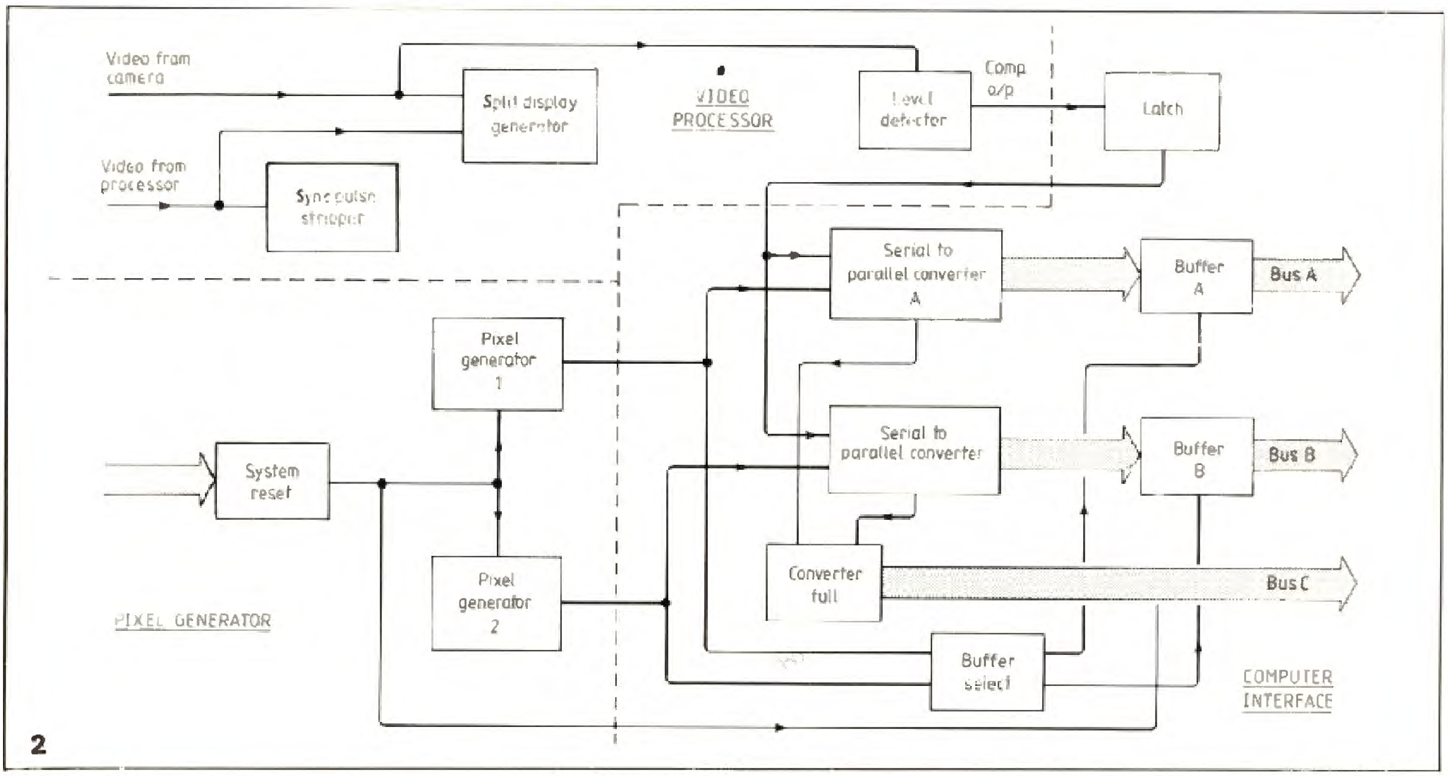


Microsections of fully annealed electrical-grade copper (above) and aluminium (below) pictured at City University. Polarized light picture (below) shows 25μm crystals, the film of oxide polarizing the illumination.

not possible to digitize the frame in one pass (40ms) so the hardware is designed to take two samples from each video line per frame. As the period is 64μs this allows approximately 32μs for the data to be transferred to the analysis computer — ample time to format the data into the final memory map for analysis.

Part 2 of this article will detail video processor and computer interface.

Composite video output is provided with sync pulses extracted from the video output of the computer system. Sync pulses allow the video camera to be genlocked to the computer system so that a simple video switching circuit can superpose the computer analysis results onto the lattice picture.



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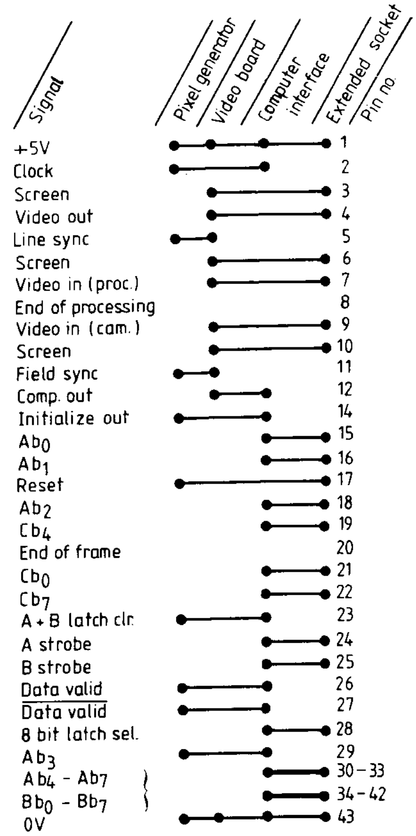

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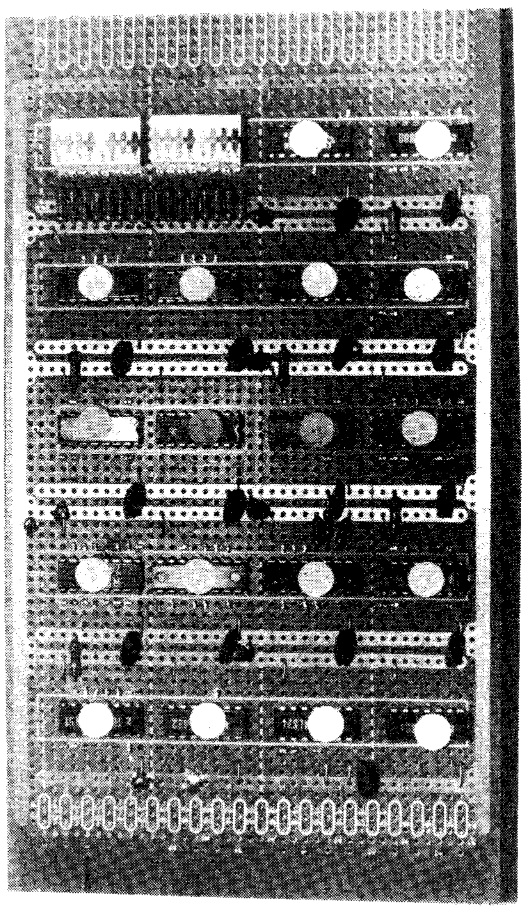
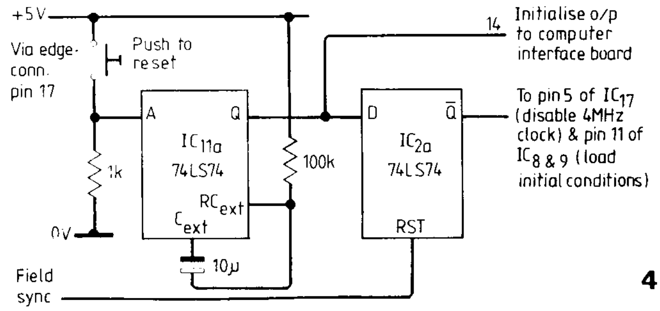
Each circuit board provides a number of different system functions and all interlinking signals are passed between boards using a common bus arrangement.



Original design fitted onto three Eurocard circuit boards, ◄ designated pixel generator, video processor and computer interface.



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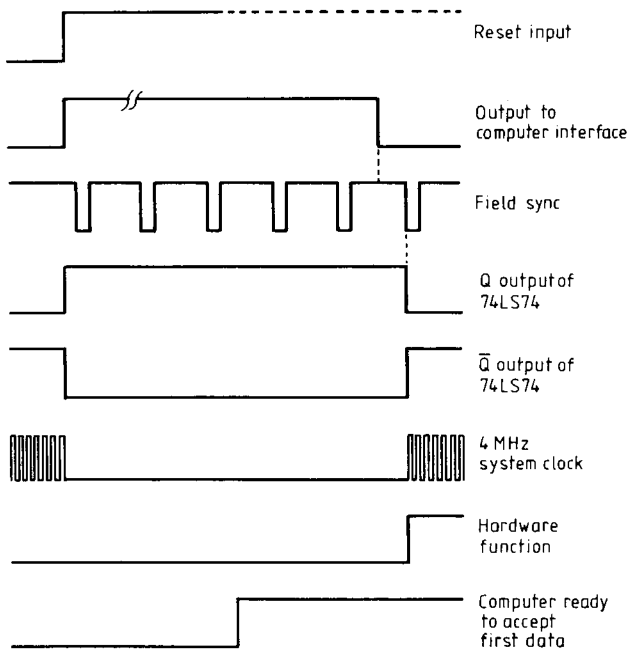

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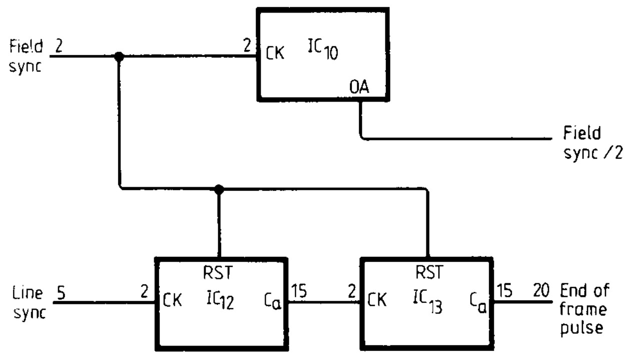
System reset is required to reset all the hardware counters and to provide a pulse to the computer to initialize the program to accept data. On application of a reset command to the circuit the system reset cycle shown is initiated.



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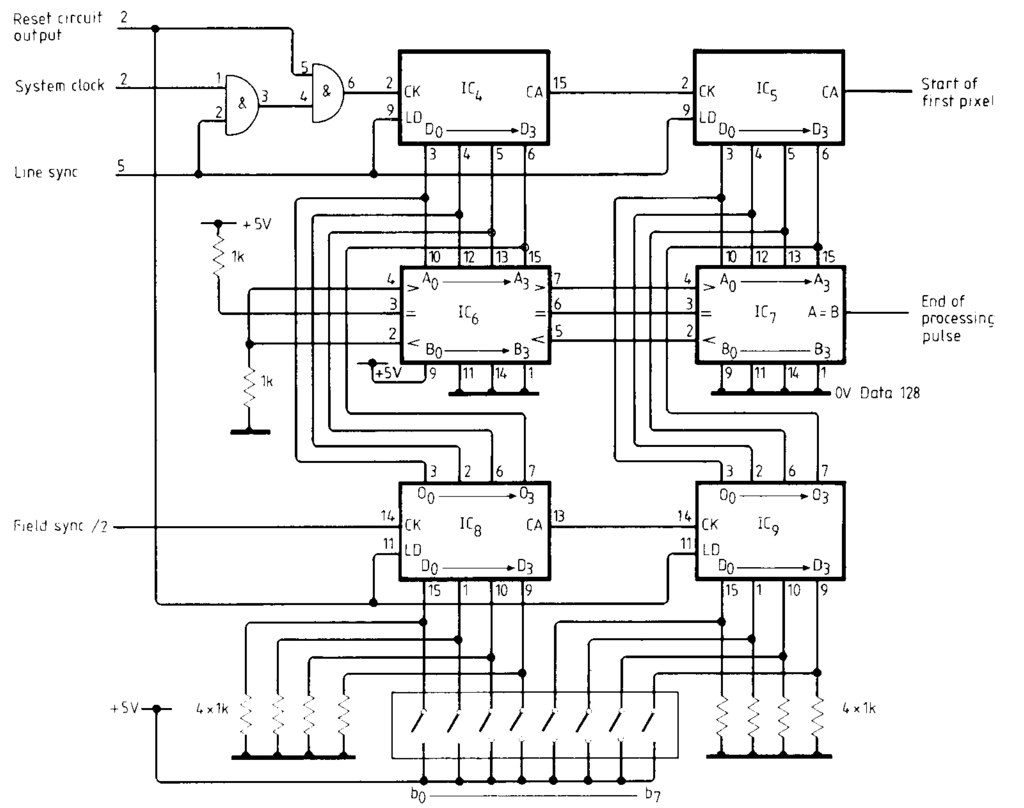
Because of the interlace of field scans a signal which discriminates between odd and even fields is needed. This simple counter circuit provides a field sync ÷2 output and also produces a pulse after every 256 lines of video (512 for two frames).

Generator one produces a pulse that indicates the beginning of the first element to be sampled per video line. This position obviously has to increment once every frame (two fields) so that sampling moves across the screen. IC4 & 5 are cascaded to form an eight-bit up counter while IC8 & 9 form an eight-bit down counter. The last-mentioned are initially loaded with 255 by the initialization pulse from the system reset circuit (Fig. 4). The counter outputs provide the data inputs to IC4 & 5. The start of the first element is defined as the time when the output of the up-counter changes from 255 to 0, and is taken from the carry output.

After the system reset the up-counter contains 255 and so the next clock input produces the start of the first pixel pulse. The line sync pulse to IC4 & 5 loads data into the counter and inhibits the 4MHz clock during this operation. The pixel position is stationary for two fields (one frame). IC8 & 9 are then clocked to give an output of 254, to be loaded into the up-counter on the occurrence of the next line sync pulse, so that when the 4MHz clock is enabled it will take the up counter one clock cycle more to produce a carry pulse.

Thus the position of the start of th epixel has moved along the tv line by one clock cycle or 250ns. Decrementing the down-counter continues until the output is 128 and the end of the first sample is at the centre of the screen, where generator two will have begun sampling.

Circuits 6 & 7 are cascaded to form an eight-bit magnitude comparator that has data inputs set to 128. The second set of inputs are the outputs from the down-counter. When this reaches 128 all the elements on the screen will have been sampled and an 'end-of-processing' pulse is produced. (7)



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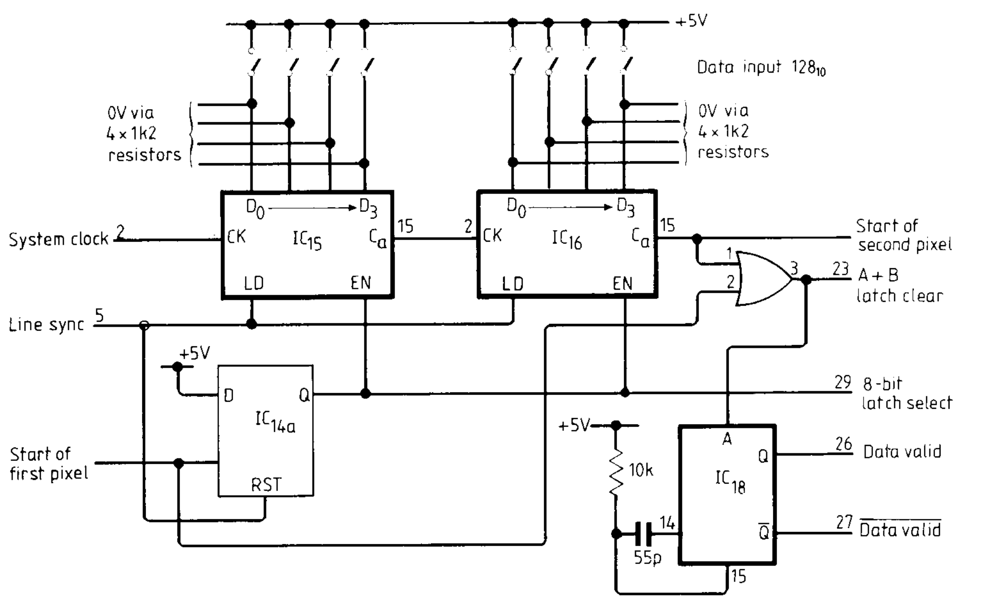
Generator two provides the position of the start of the second element to be sampled on one line, as well as the 'data valid' signal, which marks the length of one element and the 'eight-bit latch select' for the computer interface. A pulse is also generated to clear the level detector latch on the video processor board. IC15 & 16 form an eight-bit counter, the output of which provides the 'start of second pixel' indication. When the start of the first has occurred this eight-bit counter is enabled, already set up at the beginning of the line by the line sync pulse. The 4MHz clock is again used and 128 clock pulses occur between the start of elements one and two. The second is always half a tv line away from the first. The 'eight-bit latch select' line indicates whether the system is taking the first or the second sample on the line, thus defining which of the two latches is to receive the data. 'Data valid' is triggered at the beginning of each pixel and is active for one pixel length, 250ns. DIL switches were used on the prototype to allow flexibility in setting the timing thresholds and to modify the area of the picture sampled.



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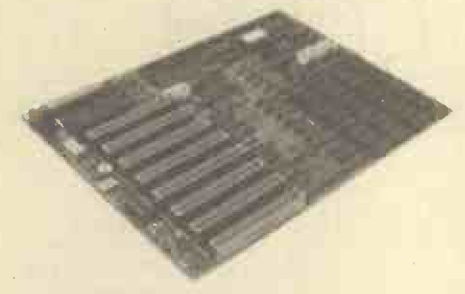

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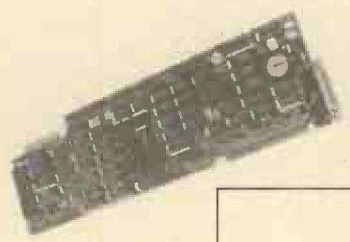

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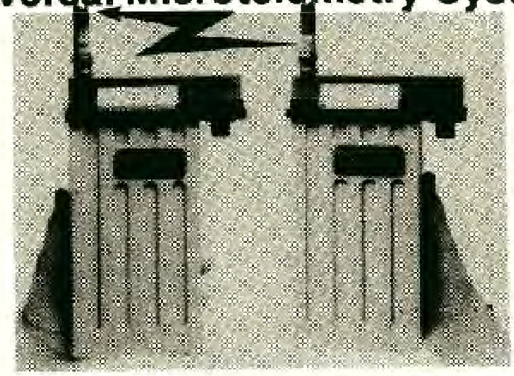

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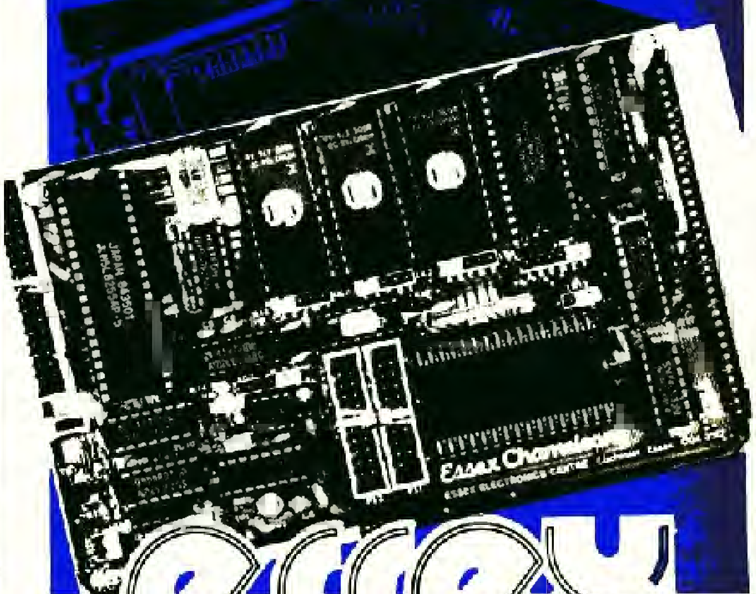

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CIRCLE 17 FOR FURTHER DETAILS.

Decoding for faster memory access

Increases in the system clock frequency without the need for faster eproms and rams is possible in many microprocessor systems by making a small modification to decoding logic.

For 2716 eproms, data is available 450ns after a stable address and chip-select signal CS going low, but only 120ns from output-enable line OE going low if CS was low 330ns before.

In many systems, CS is generated by gating the address with an E signal so the minimum machine cycle time must be twice the maximum memory access time with processor data set-up and logic propagation delays added.

If instead CS is derived only from an address, and OE gated with E, about ⅓ of the total cycle time is gained.

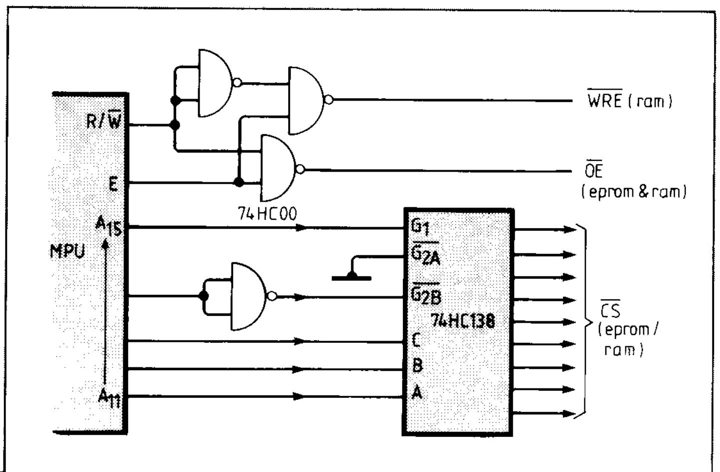
Rams are normally faster, with typically 200ns access time for 6116 c-mos rams, but producing the write-enable signal in the same way as OE gives a safety margin large enough for the system to work in all conditions.

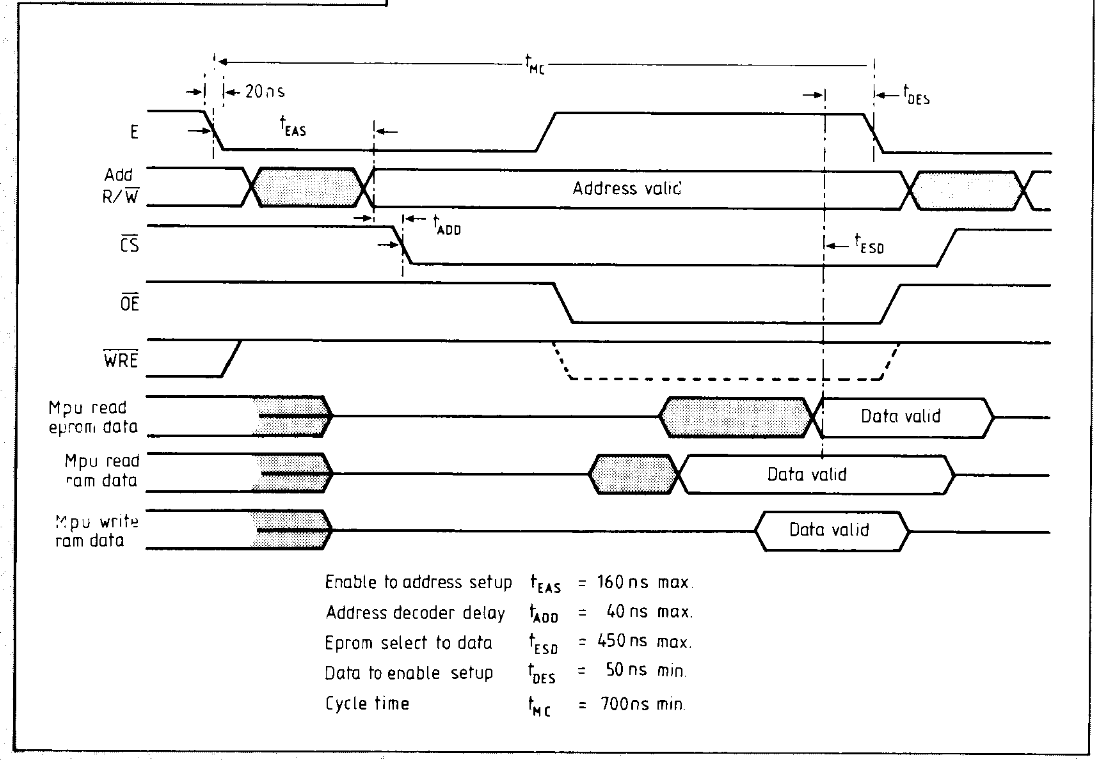
Now machine cycle time can be shortened to about 700ns, with the worst-case condition being shown in the diagram.

Power consumption is not greatly affected as devices are active for much the same amount of time. Increased power is mainly due to the processor and buffers switching faster, but this is compensated for by shorter execution time.

Battery-powered systems, i.e. c-mos, can greatly benefit from this configuration. I have used this idea with 6802, 6301 and 6303 processors, but the principle applies to other processors.

Erik Margan
Ljubljana
Yugoslavia





High-speed switching of inductive loads

Switching off current through an inductive load causes a high-voltage pulse which usually needs limiting. A diode in parallel with the inductor limits switch-off voltage to about 0.7V but makes discharge time very long:

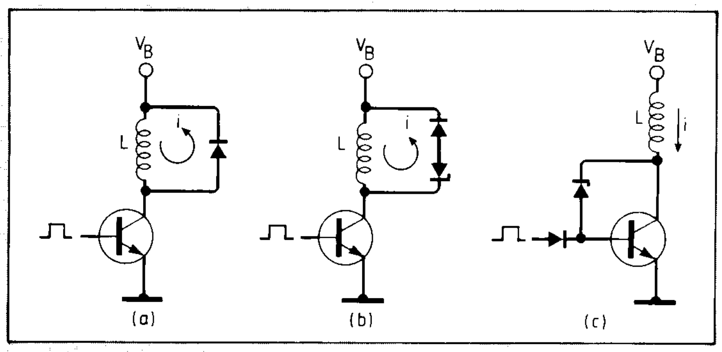
$$t \approx \frac{L.i_{trip}}{V_D}$$

where i_{trip} is inductor current just before the transistor switches off and V_D is about 0.7V.

This method is well known for increasing relay release time. Using a higher voltage as in the second diagram shortens discharge time by raising voltage V_D to $V_D + V_Z$. Voltage of the zener diode is

$$V_Z \leq V_{CEmax} - V_B - V_D,$$

and it must be able to withstand the maximum inductor current. Inductive loads, like solenoids and relays, store much energy so a power diode is needed.



Using the third configuration, the power transistor does the work. If voltage across L rises as a consequence of switching off the transistor, the zener diode conducts when

$$V_{CE} = V_Z + V_{BE}$$

and turns on the transistor.

Discharge time in this case is

$$t \approx \frac{L.i}{V_Z - V_B}$$

where V_B is the supply voltage. Coil voltage, V_L is

$$V_Z + V_{BE} - V_B \approx V_Z - V_B.$$

For example with $V_B = 24V$, $i = 6A$, $L = 10mH$, $V_Z = 200V$ and $V_D = 0.7V$, discharge using the first configuration is

$$t \approx \frac{10^{-2}H.6A}{0.7V} = 86ms$$

whereas for the third figure,

$$t \approx \frac{10^{-2}H.6A}{200V} 0.3ms$$

F. Braunschmid
Vienna
Austria

Electronic irrigation controller

An automatic system for watering a garden or greenhouse can be very useful, especially when you're on a long holiday.

With a properly adjusted controller, water is used economically, which is important in countries where water is scarce.

This system works just as well in a large plantation as it does in a small back garden, provided that a central control for water distribution is used.

Soil conductivity depends on moisture content. As the soil dries, its conductivity decreases and the change can be detected electronically and used to switch a water valve or pump to restore the soil's moisture content.

Conductivity is measured by a probe consisting of two graphite rods which is inserted into the soil. These rods come from a pair of old C-type batteries. They are cleaned and bonded to an insulating block with epoxy resin adhesive after having a pair of wires soldered to their metal caps. These wires protrude about 4-5cm above the insulator and their first 3-4cm is covered with tape or insulating sleeving.

Silicone rubber sealing compound is applied to the metal caps to stop rusting. The probe is then pushed into the soil in the sunniest part of the garden until the insulating block rests on the surface.

Soil conductivity is measured by passing a.c. through the probe and measuring voltage drop. Using d.c. was found to cause electrolysis resulting in erratic operation.

Alternating drive for the probe is taken from one side of the 9-0-9V transformer and adjusted for sensitivity using a potentiometer. Voltage from the wiper feeds the base of Tr_1 and the probe connects between this point and ground. When the soil dries enough to produce about 0.65V peak across the probe, Tr_1 conducts at the positive peak of the waveform.

Capacitor C_2 gradually discharges towards ground and Darlington pair $Tr_{2,3}$ starts to conduct, switching on the relay which in turn triggers the triac. Now the electric valve or pump starts.

Components R_3 and C_3 provide additional smoothing since the voltage over C_2 contains some 50Hz hum.

As water penetrates the soil, voltage across the probe falls below the threshold of Tr_1 and C_2 charges through R_{2-4} towards the supply rail. Eventually, the Darlington pair stops conducting and the relay switches off the triac, and hence the water supply.

I used Vero board and a metal case for construction. It is only important to note that Tr_3 switches on gradually; no Schmitt trigger is used, due to a.c. operation of the probe. Because of this, Tr_3 needs a heat sink, especially if a low impedance relay is used.

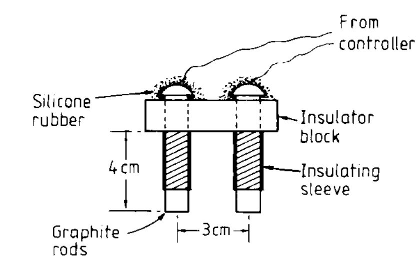
Heat sinking might be needed for the triac, depending on the load. This triac supplies about 4A (400V). Adjustment is simple. After installing the probe, turn on the system. After thoroughly watering the soil, allow it to dry by natural evaporation. When you feel that the soil needs watering again, adjust the potentiometer slowly so that probe current is increased until the system switches on. It should then be allowed to water the soil until it switches off by itself. It takes some time for the probe to settle in the soil, so the potentiometer may need adjusting from time to time.

During hot dry weather water is supplied for about 30 minutes every two days. Here in Cyprus, hot and dry means 35°C and at least 30% humidity. The area served is a $250m^2$ flower, shrub and vegetable patch.

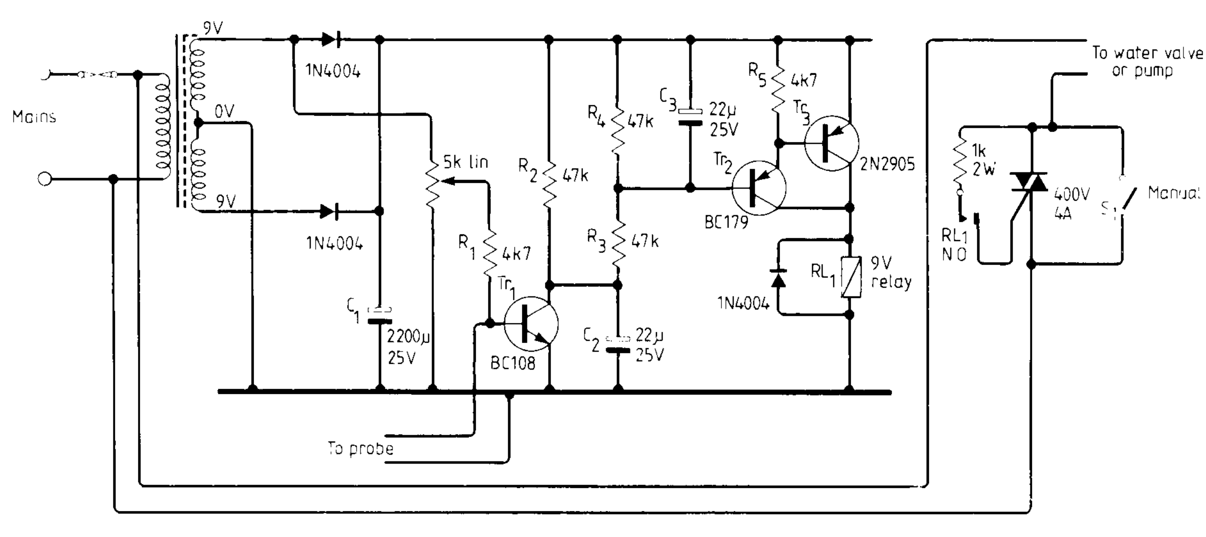
Finally, an interesting and rather peculiar advantage comes with this sytem. During hot weather, the unit only turns on late in the evening well after sunset. It seems that the reason is that the increase of the soil's temperature from solar radiation increases the conductivity of the soil somehow, thus delaying switch-on until the soil cools in the evening.

This is beneficial for most plants, as watering them with sprinklers under the hot sunshine can be harmful and wasteful of water. Another possible explanation is that the base-emitter threshold of Tr_1 changes with temperature, reducing in the evening with the cool breeze coming into my home through open windows.

Neoklis Kyriazis
Limassol
Cyprus



Last month's shaft-encoder counting idea attributed to M. Winder was actually sent in by Andrew Armstrong of Leighton Buzzard. Mr Winder sent us a letter on the same subject which led to some confusion. Our apologies go to both contributors.



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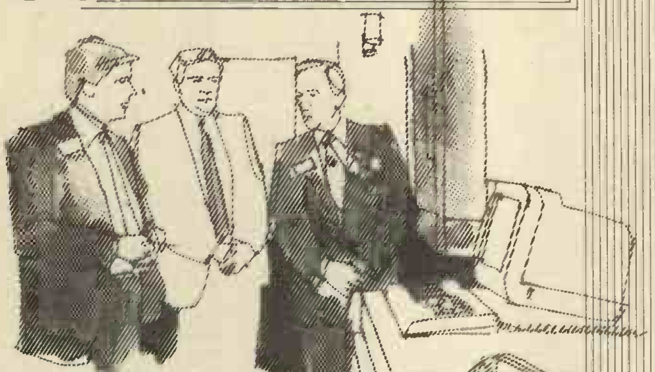

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AU113	4.50
BC107A	0.11
BC107B	0.11
BC108	0.10
BC108A	0.11
BC108B	0.12
BC109	0.10
BC109B	0.12
BC109C	0.12
BC114	0.11
BC116A	0.15
BC117	0.19
BC119	0.24
BC125	0.25
BC139	0.20
BC140	0.31
BC141	0.25
BC142	0.21
BC143	0.24
BC147A	0.12
BC147B	0.12
BC148A	0.09
BC148B	0.09
BC149	0.09
BC157	0.12
BC158	0.09
BC159	0.09
BC174	0.09
BC174A	0.09
BC177	0.15
BC178	0.15
BC182	0.10
BC182LB	0.10
BC183	0.10
BC183L	0.09
BC184LB	0.09
BC204	0.10
BC207B	0.13
BC208B	0.13
BC212	0.09
BC212L	0.09
BC212LA	0.09
BC213	0.09
BC213L	0.09
BC214	0.09
BC214C	0.09
BC214L	0.09
BC237B	0.09
BC238	0.09
BC239	0.12
BC251A	0.12
BC252A	0.15
BC258	0.25
BC258A	0.39
BC284	0.30
BC300	0.30
BC301	0.30
BC303	0.26
BC307B	0.09
BC327	0.10
BC328	0.10
BC337	0.10
BC338	0.09
BC347A	0.13
BC461	0.35
BC478	0.20
BC527	0.20
BC547	0.10
BC548	0.10
BC549A	0.10
BC550	0.14
BC557	0.08
BC557B	0.80
BC558	0.10
BCY33A	1.60
BD115	0.30
BD124P	0.59
BD131	0.42
BD132	0.42
BD133	0.40
BD135	0.30
BD136	0.30
BD137	0.32
BD138	0.30
BD139	0.32
BD140	0.30
BD144	1.10
BD150C	0.29
BD159	0.65
BD160	1.50
BD166	0.55
BD179	0.72
BD182	0.70
BD183	0.70
BD201	0.83
BD202	0.65
BD203	0.78
BD204	0.70
BD222	0.46
BD223	0.59
BD225	0.48
BC232	0.35
BD233	0.35
BD234	0.35
BD236	0.49
BD237	0.40
BD238	0.40
BD242	0.65
BD246	0.75
BD376	0.32
BD410	0.65
BD434	0.65
BD437	0.75
BD438	0.75
BD520	0.65
BD538	0.65
BD597	0.95
BD589	0.45
BD701	1.25
BD702	1.25
BD707	0.90
BDX32	1.50
BF115	0.35
BF119	0.35
BF119	0.65
BF127	0.39
BF154	0.20
BF158	0.22
BF160	0.27
BF167	0.27
BF173	0.22
BF177	0.38
BF178	0.26
BF179	0.34
BF180	0.29
BF181	0.29
BF182	0.29
BF183	0.29
BF184	0.28
BF185	0.28
BF194	0.11
BF195	0.11
BF196	0.11
BF197	0.11
BF198	0.16
BF199	0.14
BF200	0.40
BF241	0.15
BF245	0.30
BF257	0.28
BF258	0.28
BF259	0.28
BF271	0.26
BF273	0.18
BF336	0.34
BF337	0.29
BF338	0.32
BF355	0.37
BF362	0.38
BF363	0.65
BF371	0.25
BF394	0.19
BF422	0.32
BF457	0.32
BF458	0.36
BF459	0.36
BF467	0.68
BF494	0.45
BF495	0.45
BF595	0.23
BF597	0.25
BFR39	0.23
BFR40	0.23
BFR81	0.25
BFR88	0.30
BFR90	1.50
BFR91	1.75
BFT42	0.35
BFT43	0.35
BFW92	0.85
BFX29	0.30
BFX84	0.26
BFX85	0.32
BFX86	0.30
BFX88	0.25
BFY50	0.21
BFY51	0.21
BFY52	0.25
BFY90	0.77
BLY48	1.75
BRY39	0.45
BR100	0.26
BR110	0.49
BR103	0.55
BRC4443	1.15
BT100A/02	0.85
BT106	1.49
BT116	1.20
BT119	3.15
BT120	1.65
BU105	1.95
BU108	1.69
BU124	1.25
BU125	1.25
BU126	1.60
BU204	1.55
BU205	1.30
BU208	1.39
BU208A	1.52
BU208D	1.85
BU3276	1.20
BU407	1.24
BU500	2.25
BU508A	1.95
BU526	1.90
BU80Y	2.25
BUY69B	1.70
MJ3000	1.98
MJE340	0.40
MJE520	0.48
MPSA13	0.29
MPSA92	0.30
MRF237	4.95
MRF450A	13.95
MRF453	17.50
MRF454	26.50
MRF455	17.50
MRF475	2.95
MRF477	10.00
MRF838	13.95
OC16W	2.50
OC23	1.50
OC28	1.50
OC29	2.25
OC32	2.25
OC42	0.75
OC44	0.75
OC45	0.55
OC70	0.45
OC71	0.55
OC72	0.85
OC75	0.95
OC81	0.50
OC171	3.50
R2008B	1.45
R2010B	1.45
R2322	0.58
R2323	0.66
R2540	2.48
HCA16334	0.90
RCA16335	0.80
SKE5F	1.45
TIP29	0.40
TIP29C	0.42
TIP30C	0.43
TIP31C	0.55
TIP32C	0.42
TIP33C	0.95
TIP34B	0.95
TIP41A	0.45
TIP41C	0.45
TIP42C	0.47
TIP47	0.65
TIP120	0.60
TIP125	0.65
TIP142	1.75
TIP161	2.95
TIP2955	0.85
TIP3055	0.55
TIS91	0.20
TV106/2	1.50
2N1308	1.35
2N2219	0.28
2N2222	0.29
2N2905	0.40
2N3053	0.40
2N3054	0.59
2N3055	0.52
2N3702	0.12
2N3703	0.12
2N3704	0.12
2N3705	0.20
2N3706	0.12
2M3708	0.12
2N3733	9.50
2N3773	2.75
2N3792	1.35
2N4427	1.95
2N4444	1.15
2N5294	0.42
2N5296	0.48
2N5298	0.60
2N5485	0.45
2N5496	0.95
2SA715	0.60
2SC495	0.80
2SC496	0.80
2SC1096	0.80
2SC1106	2.50
2SC1172Y	2.20
2SC1173	1.15
2SC1306	1.40
2SC1307	1.75
2SC1364	0.50
2SC1449	0.80
2SC1678	1.25
2SC1909	1.25
2SC1945	2.65
2SC1954	0.95
2SC1957	0.80
2SC1969	1.95
2SC2028	1.15
2SC2029	1.95
2SC2078	1.45
2SC2091	0.85
2SC2098	2.95
2SC2166	1.95
2SC2314	0.80
2SC2371	0.36
2SO234	0.50
3N211	2.95
3SK88	0.95
3SK88	0.95

DIODES

AA119	0.80
BA115	0.13
BA145	0.16
BA148	0.17
BA154	0.06
BA156	0.15
BA157	0.30
BAX13	0.04
BAX16	0.06
BB105B	0.30
BT151	0.79
BY126	0.10
BY127	0.11
BY133	0.15
BY164	0.45
BY176	1.20
BY179	0.63
BT182	0.55
BY184	0.35
BY199	0.40
BY206	0.14
BY208-800	0.33
BY210-800	0.33
BY223	0.90
BY298-400	0.22
BY299-800	0.22
BYX10	0.20
BYX36-150R	0.20
BYX38-600R	0.60
BXY55-600	0.30
BYX71-600	1.10
BZY95C30	0.35
CS4B	4.50
CS10B	8.45
OA47	0.09
OA90	0.05
OA91	0.06
OA95	0.06
OA202	0.10
IN21DR	5.00
IN23B	5.00
IN23C	5.00
IN23ER	5.00
IN23WE	5.00
IN4001	0.04
IN4003	0.04
IN4004	0.05
IN4005	0.05
IN4007	0.06
IN4148	0.02
IN4448	0.10
IN5401	0.12
IN5402	0.14
IN5403	0.12
IN5406	0.13
IN5407	0.16
IN5408	0.16
ITT44	0.04
ITT923	0.15
ITT2002	0.10

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CME1431W	39.00
CME202GH	45.00
CME2024W	45.00
CME2325W	45.00
CME3128W	45.00
CME3132GH	45.00
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CV5320	85.00
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D13-51GM/26	85.00
D13-45GH/01	55.00
D13-471GH/26	69.00
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D13-610GH	59.00
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D13-611GM	59.00
D13-630GH	59.00
D14-150GH	75.00
D14-150GM	75.00
D14-162GH/84	69.00
D14-172GR	55.00
D14-172GV	55.00
D14-173GH	55.00
D14-173GM	53.00
D14-173GR	55.00
D14-181GH/98	65.00
D14-181GJ	55.00
D14-181GM	53.00
D14-181GM50	59.00
D14-182GH	59.00
D14-200BE	89.00
D14-200GA/50	85.00
D14-200GM	75.00
D14-210GH	75.00
D14-270GH/50	75.00
D14-310W	110.00
D14-320GH/82	85.00
D14-340GH/KM	45.00
D14-340KA	45.00
D16-100GH	65.00
D16-100GH/65	69.00
D16-100GH/67	65.00
D16-100GH/79	69.00
D16-100GH97	65.00
D18-160GH	69.00
D21-10GH	65.00
DG7-5	55.00
DG7-6	35.00
DB7.36	55.00
DG7.32	45.00
DG13.2	45.00
DH3-91	55.00
DH7.91	45.00
DP7.5	35.00
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DN13.78	35.00
F16-101GM	75.00
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F31-10LC	75.00
F31-10LD	75.00
F31-12LD	75.00
F31-13GR	75.00
F31.13LD	75.00
F31-13LG	75.00
F41-123LC	185.00
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M17-151GVR	175.00
M17-151GR	175.00
M19-100W	45.00
M19-103W	55.00
M23-110GH	55.00
M23-111LD	55.00
M23-112GM	55.00
M23-112GV	55.00
M23-112GW	55.00
M23-112KA	55.00
M24-120GM	59.00
M24-120LC	59.00
M24-120WAR	59.00
M24-121GH	55.00
M28-12GH	55.00
M28-13LC	49.00
M28-13LG	49.00
M28-13GR	49.00
M28-131GR	55.00
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M31-101GH	55.00
M31-182GR	55.00
M31-182GV	53.00
M31-184W	65.00
M31-184GH	85.00
M31-184P31	65.00
M31-185W	69.00
M31-190GH	55.00
M31-190GR	55.00
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M31-220W	59.00
M31-270GY	65.00
M31-271P31	65.00
M31-271GW	65.00
M31-271W	65.00
M36-141W	75.00
M36-170LG	75.00
M38-101GH	65.00
M38-103GR	65.00
M38-120W	65.00
M38-120WA	65.00
M38-121GHR	65.00
M38-121LA	65.00
M38-122GW	65.00
M38-140LA	65.00
M38-142LA	65.00
M38-341P31	65.00
M38-344P39	65.00
M40-120W	59.00
M43-12LG/01	65.00
M44-120LC	65.00
M44-120GR	65.00
M50-120GH	65.00
M50-120GR	65.00
M50-120GV	65.00
M50-120LC	65.00
M61-120W	75.00
S6AB	45.00
SE4/D/P7	45.00
SE42BP31AL	55.00
SE42BP31	55.00
SE5FP31	55.00
T937	65.00
T948N	65.00
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V4150LC	55.00
V5004GR	59.00
V5004LD	59.00
V6001	65.00
V6007DP31	59.00
V6008GW	59.00
V6034WA	59.00
V6048CAL	59.00
V6048J	49.00
V6064BP31	55.00
V6064CLA	55.00
V6069GH	55.00
V6070P31	65.00
V7030	59.00
V7031GH	59.00
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5BP1	9.00
5BHP1	30.00
5BHP1FF	30.00
5BHP31	30.00
5CP1	10.00
6EP7/S	39.00
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13BPA4	17.50
17DWP4	25.00
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4-527V-51000	5150	Capston Motor	29.95
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143-2-457T-05900	VTC9455	Stopper Reel Base	0.55
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ANODE CAP (27kV)	0.69

by J.L. Linsley Hood

Synchrodyne a.m. receiver

3-Circuit details of the demodulator and r.f. stages

The receiver section of Fig. 1 (last month) consists of a separate phase sensitive detector, which would well be of an identical type to that used in the p.l.l., followed by a steep-cut low-pass filter, to give the required adjacent channel selectivity, and some kind of muting circuit, in operation when the incoming signal is not in synchronism, to remove the off-tune whistle which is characteristic of the synchrodyne system.

The adjustable steep-cut low-pass filter is built from a cascaded pair of 'bootstrap' filter circuits, in the form shown in Fig. 9, having a Q chosen to give a slope, for each section, of about 20dB/octave. With the component values shown in Fig. 9, the turn-over frequency is 9kHz, though this could be modified, as desired by the user, by proportional adjustments to the filter component values.

A potential problem in any synchrodyne system is that of unwanted demodulation of r.f. signals presented to the phase detector. Since most i.c. op-amps have a poor performance in this respect, it is highly desirable that any r.f. signals present at the output of the p.s.d. (MC1496) should be removed before the a.f. signal is presented to the a.f. filter i.cs. This is done most simply by putting the two third-order RC component elements in front of the filter stages.

Since resistors are cheaper, smaller, and available in a wider range of values, the design of the filter circuit has been chosen so that the required choice of filter cut-off requirements can be obtained by switching resistor values. The complete circuit of the demodulator and frequency switched filter/amplifier is shown in Fig. 10. The response of the filter stages is flat within ±1dB at frequencies below the cut-off point, and is shown, for an F_t value of 9kHz, in Fig. 11.

Problems with direct conversion systems

Although some of the difficulties inherent in this type of receiver, such a microphony in the local oscillator, due to the bulk of the required signal gain being obtained at a.f., and aerial-sourced mains hum, due to the same cause, can be reduced or eliminated by pre-demodulator r.f. amplification — as can the intrusion of spurious signals due to oscillator harmonics or demodulator non-linearities — the use of signal amplification prior to the demodulator worsens the problem of demodulator input cross-modulation.

This difficulty seems to be an endemic fault in such systems, and the LM/MC1496, though a very good device in many respects, is not above criticism in respect of cross modulation. This manifests itself as a spurious interfering signal, present at a low level, and at normal tonal pitch, when a powerful, but unsynchronized, adjacent signal is present at the demodulator input, along with another signal which is, correctly, being synchronously demodulated.

It was the apparently intractable nature of this problem which led to this project being abandoned, after a lot of useful preliminary work, some years ago, only to be taken up when the possibility of new insights into the problem appeared.

The solutions necessary depend on the demodulator type employed. In the case of the LM/MC1496, the essential requirement is to ensure that all signal levels at the demodulator input, (pins 1 or 4), are kept below some 30mV. It is also desirable that the peak-to-peak level of local oscillator drive shall be below some 450mV.

Better performance in this respect is also given if both the signal input and the local oscillator drive are applied as single-ended rather than as push-pull inputs. Finally, the modulator should be adjusted for d.c.

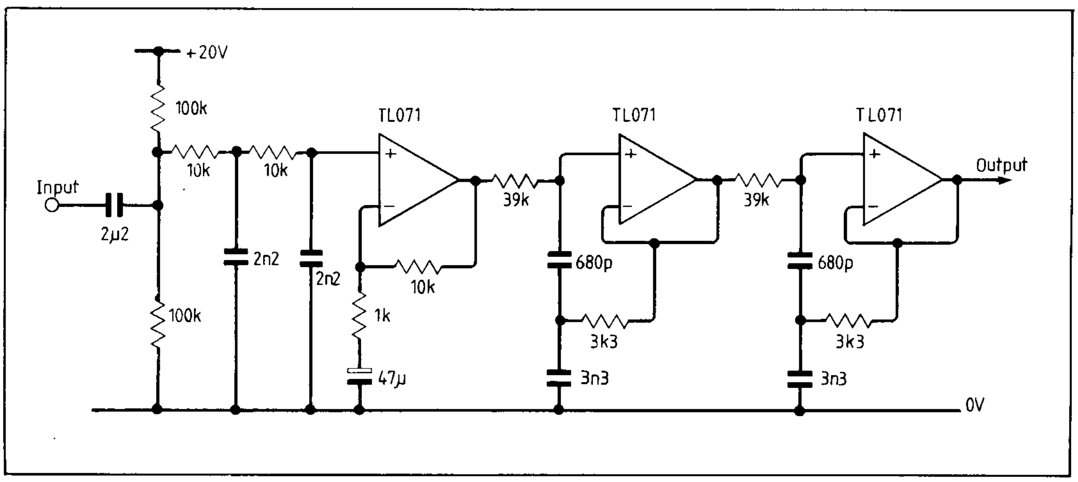
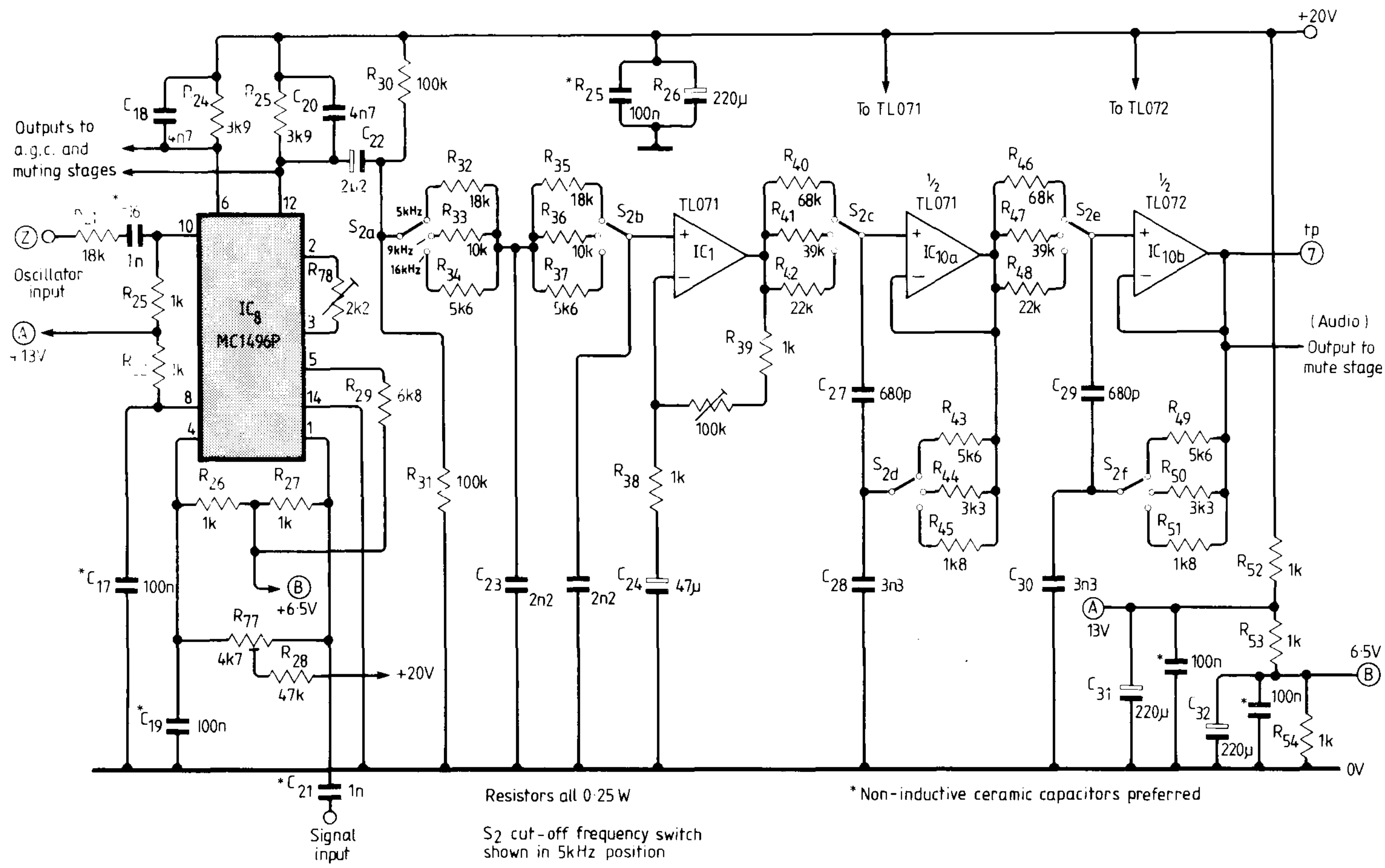


Fig. 9. Basic sixth order low-pass filter. Performance is shown in Fig. 11 opposite.



balance, by means of the circuit shown in Fig. 8(b). In practice, if an intruding signal of this type can be heard in the background to a silent carrier, this potentiometer and the 'sensitivity' control, (R_{77} and R_{78} in Fig. 10) can be adjusted to achieve a truly silent background level — assuming that the intruding signal is not so great that input overload is occurring.

On initial commissioning, R_{77} slider should be set to its mid-point, and R_{78} should be preset to about 1kΩ. It should be borne in mind that the actual setting of R_{78} will influence the overall sensitivity of the receiver, so, if there is no very clear optimum setting, this factor may decide its value. However, it is prudent, in order not to sacrifice ease of locking on to wanted signals, not to make R_{78} less than two thirds of the value of the corresponding resistor (R_{11}) in the p.l.l.

I have, perhaps, dwelt on the subject of cross-modulation at undue length, but since it was an inability to find a completely satisfactory solution to this problem which had led me to abandon an earlier design for a synchrodyne receiver, it looms large in my mind.

A.g.c. and muting stages

Initial experimentation with the synchrodyne, in its more primitive early forms, drew attention, quite forcefully, to the variation in signal strength between local and more remote stations. This is of particular importance since the synchronous demodulator i.c. which is used has a relatively limited maximum input level for correct operation.

Some form of automatic gain adjustment of the input r.f. signal is therefore essential to the proper operation of this circuit, quite apart from the normal problems of fading which occur on long distance or night-time reception of a.m. signals, which must be remedied. Happily, a characteristic of the synchronous demodulator is that there is present at the phase detector output a d.c. component which is directly related to the magnitude of the carrier of the radio signal applied to it.

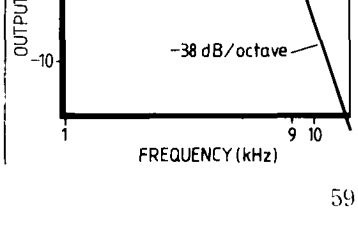
This allows the isolation of this d.c. component, and its amplification to provide a highly signal specific a.g.c. control voltage, unaffected by the presence of adjacent signals within the input pass-band of the r.f. stages.

The circuit employed for this purpose is shown in Fig. 12. In this, IC_{11a} is a d.c. gain stage with a gain of 21. Under normal conditions, both output pins of IC_8 sit within a few tens of millivolts of one another, and the output of IC_{11a} sits at some +16V. This gives a normal, no-signal, a.g.c. voltage of some +8V. For a signal having an amplitude approaching the overload voltage of IC_8, the output differential voltage would increase to some 500mV or more, and this would cause the output of IC_{11a} to fall to its limiting voltage of some +1V. Long before this signal level is reached, the a.g.c. output voltage, used to control the gain of the r.f. stages, by means of the potential applied to the second gates of dual-gate mosfets, will have fallen to zero.

The capacitor C_{34} is used to remove a.f. components from the a.g.c. line, and should be as large as possible commensurate with adequate a.g.c. response time, for which a time constant of about 0.5 seconds seems suit-

Fig. 10. Complete filter-demodulator stage. Turnover frequencies can be changed by proportional adjustment of the resistor values. All resistors are 0.25W types.

Fig. 11. Frequency response of the filter shown in Fig. 9.



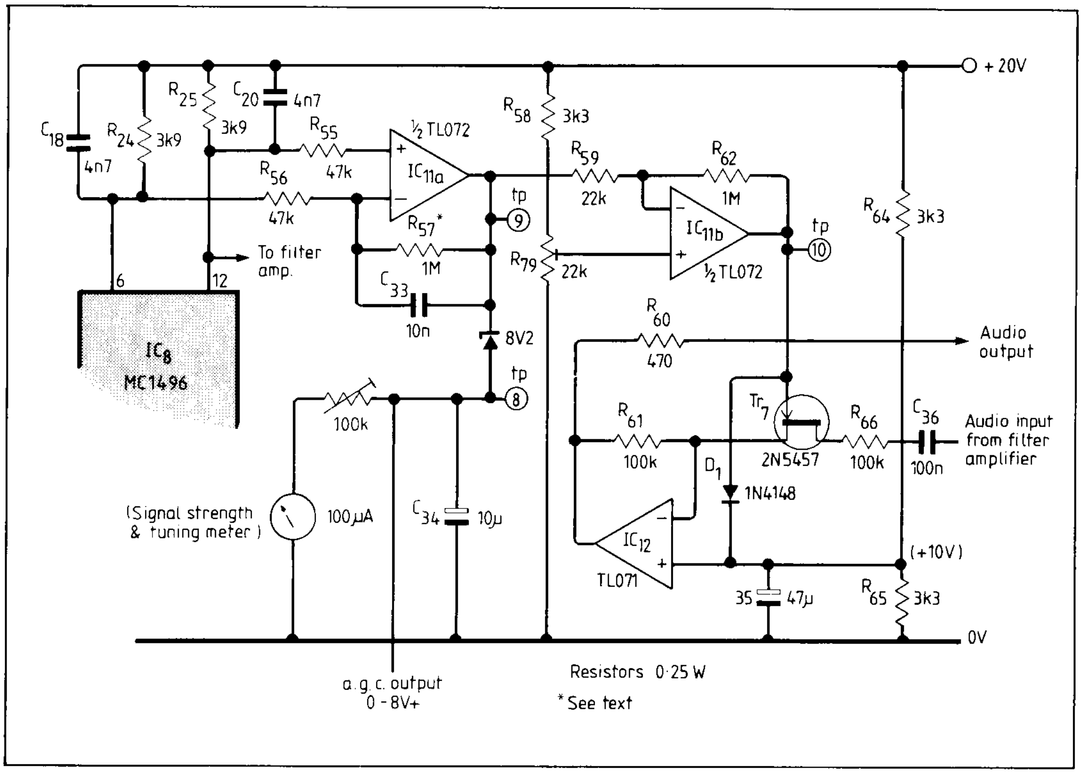


Fig. 12. This a.g.c. generator provides an effective solution to cross-modulation problems caused by strong adjacent-channel signals. The fet muting stage supresses noise and whistles between stations.

Fig. 13. Gain-controlled r.f. amplifier. A second tuned stage would have made it better still, but three-gang tuning capacitors are hard to find.

able for normal use. Unfortunately, some element of compromise is necessary with respect to the gain and time-constants of the a.g.c. circuit, (C_{18}/C_{20}, C_{33}, C_{34}, C_{38}/R_{69}, and C_{40}/R_{72}), since any amplified a.g.c. arrangement is effectively a closed-loop servo system, containing time-delaying (phase-shifting) RC components, and may, therefore, become unstable if the time constants are inappropriate or the loop gain is too high.

Because of the nature of the system, some RC elements are unavoidable, since they are needed to remove r.f. and a.f. components of the signal, so too high a gain setting of the demodulator, by way of R_{78}, may cause instability. This would generally be observed on l.w. signals, as an l.f. (10-400Hz) 'flutter' superimposed on the signal. I did not, in the prototype, make R_{57} variable, to allow more freedom in the choice of demodulator gain, but it might be convenient.

The second function of this circuit is to operate a muting arrangement, which will suppress the audio output when the received signal is not in lock. This is done using IC_{11b} as a voltage threshold detector, to sense the output potential of IC_{11a}. If this normally sits at, say, +16V, and the non-inverting input of IC_{11b} is set by R_{79} to, say, +15V, then the output of IC_{11b} will be hard against its negative output limit, and the n-channel fet, Tr_7, will be cut off and the gain of IC_{12} will be zero.

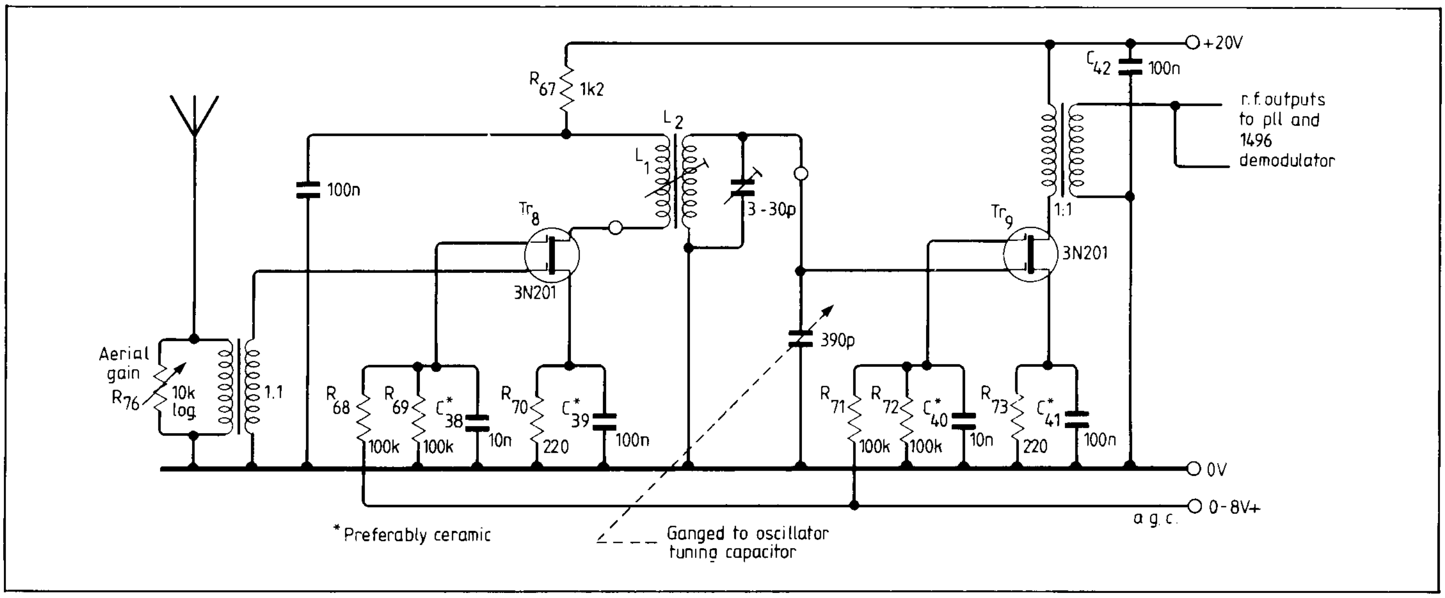
If, however, an incoming signal, on synchronism, produces a +100mV d.c. offset between pins 6 and 12 of IC_8, then output voltage of IC_{11a} will fall to +14V, and the output of IC_{11b} will swing hard against its positive output limit, and D_1 will conduct, holding the gate of Tr_1 sufficiently positive for it to have a low dynamic resistance. The gain of IC_{12} then increases to 1.

This arrangement gives effective muting, and a distortion, when in conduction, of only about 0.01%, for a 1V r.m.s. input, due to the very low level of a.f. present at the inverting input of IC_{12}, and due to the swamping effect of the input resistor, R_{66}.

A 100μA meter, in series with a preset 100k resistor to set the meter full scale deflection, connected across the a.g.c. rail serves as a signal strength/tuning meter. This has a reversed mode of operation, in that zero signal gives f.s.d., whereas strong signals give a progressive diminution of meter deflection.

R.f. stages

From the point of view of a fixed-position receiver, a ferrite rod aerial is less convenient than a length of wire, in that it



does not make the receiver orientation-sensitive in relation to the compass direction of the transmitter. Also, it is convenient, in high quality audio gear, to use screened metal housings, and these also do not marry very well to ferrite rod aerials.

On the other hand long pieces of aerial wire are unsightly and inconvenient. The design of the r.f. stages were therefore aimed at a sensitivity for the commencement of a.g.c. operation, of 50-100µV. This gives more than adequate signal strength, at distances of up to 100 miles from normal m.f./l.f. transmitters, with a four or five foot length of wire attached to the aerial input socket.

The circuit employed, shown in Fig. 13, is very simple and straightforward, employing two stages of r.f. gain, using r.f. dual-gate mosfets, with an a.g.c. voltage applied to Gate 2. Maximum signal gain is given with a G2 voltage of about +4V, and the gain decreases as G2 voltage is reduced.

I would have preferred to have used a layout employing two tuned r.f. stages, in the interests of better interference rejection from signals which are far enough away in frequency to be cut out by the post demodulator filtering, but nevertheless strong enough to cause some cross modulation of the demodulator i.c.

However, this would have required the use of a three-gang tuning capacitor, and, nowadays, in the UK, these are very rare indeed, so, even if I were able to track one down in some forgotten hiding place, other would-be constructors might not have my good fortune.

On the other hand, two-gang tuning condensers, though not plentiful, are still available.

Consequently, and with some regrets, I decided to make both the input and output couplings aperiodic, using small ferrite cored 1:1 transformers. Interestingly the small pulse transformers from RS Components work quite well in this application, and have an adequately flat pass-band from 100kHz to rather more than 10MHz, and I used these in the prototype to save the labour of winding some specially. The oscillator and r.f. coils were wound on standard 7mm coil formers, internally threaded to take 6mm dust-iron or ferrite threaded cones.

The oscillator coils for m.f. and l.f. are 55 and 400 turns of 34 s.w.g. cotton/enamel covered wire, scramble wound between rubber grommets on the coil former to hold the windings in a reasonably tidy lump. The r.f. coils are 100 and 700 turns, with coupling windings of 20 and 80 turns respectively. Undoubtedly, if one was persistent, one could find coils of commercial origin for this purpose.

The screw cores and the trimmer capacitors are used to set the sensitivity to maximum, using signals which are, respectively, somewhere near the bottom and top of the tuning band. Because the ratrios of maximum and minimum frequencies are the same for both oscillator and r.f. tuning, very good tracking is possible.

I have not shown the switching connections for the coils in Figs 7 or 13 in order to simplify the drawings, since I assume that the necessary connections will be self-evident. It will also be understood that reasonable care must be taken in the layout of the r.f. stages, and in the r.f. input connections to the two demodulator i.cs, in order to avoid possible r.f. instability.

The layout adopted, with the demodulator, p.l.l., and filter amplifier mounted on one p.c.b., and the r.f., a.g.c., and muting circuitry mounted on another, with the two p.c.b.s supported and separated by a vertical metal screening plate, can be seen in the photograph below. The simple 20V d.c. power supply unit is shown in Fig. 14.

The a.g.c. action, applied over the two r.f. stages, is effective over an input signal range of about 46dB (200:1), and this copes adequately with the range of broadcast signals received in my own locality. However, since it is inconvenient to have to modify the aerial wire layout if the signal picked up from a powerful local station is found to overload the receiver, I have included a 10k pot, connected across the aerial input, to give a measure of input signal adjustment. For those remote from powerful local transmitters this may be unnecessary.

The sound quality, in the absence of distortion due to selective fading under night-time listening conditions, has proved to be very good, and better than that given by a good quality, valve operated superhet of mid-1950s vintage, in terms of the silence of the background, freedom from unwanted and unavoidable whistles, and in respect of the cleanness and openness of the sound. In a direct comparison with a BBC f.m. broadcast, usually, but not invariably, the f.m. signal had a better h.f. response — presumably a function of the transmitted signal.

In normal day-time use, some eight or ten BBC transmitters are receivable on a five or six foot aerial wire. At night, some fifty or sixty stations, of continental origins, also exceed the signal level needed to overcome the muting threshold.

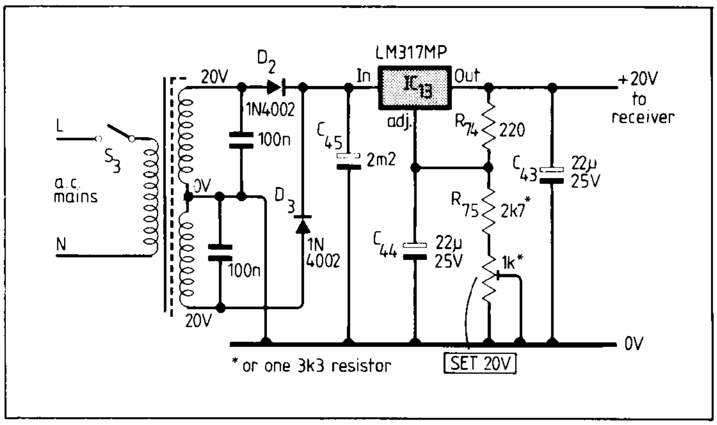
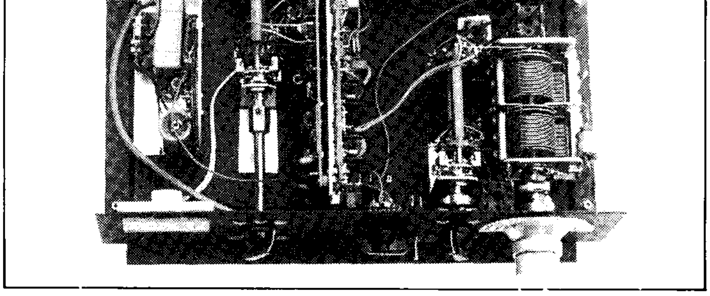


Fig. 14. Power supply for the receiver.



A kit of parts for this project is in preparation. Details from Hart Electronics, Penylan Mill, Oswestry, Shropshire SY10 9AF.

A QUESTION ABOUT Q

Although not answering Lady Jeffreys' question (Feedback, December 1985) on who first used the letter "Q" to denote the ratio of the reactance to the resistance of a tuned circuit, it may be of interest that Nikola Tesla called this quantity "magnifying factor" as early as 1899 in his calculations on the coils that now bear his name (*Colorado Springs Notes 1899-1900*, published by the Tesla Museum, Belgrade), though he did not denote it by a symbol.

As I reported in a letter in the *Quarterly Journal of the Royal Astronomical Society (1985) 26, 529*, an early reference to Q occurs in "Principles of Radio" by Henney (published by Wiley in 1929). Henney says in the Preface that "considerable material has been taken from *Radio Broadcast*" and it could be that an earlier mention of Q might be found in that journal (which was published over the years 1922 to 1930 in Garden City, New York). Unfortunately, it does not appear to be held in any of the main libraries of the UK, but perhaps a reader in the USA might be able to refer to it.

However, it may be that Tesla himself used the letter Q for his magnifying factor, but unless more of his private papers become available it is impossible to say since his publications (mainly patents) are non-mathematical.

D. McMullan
Cavendish Laboratory
Cambridge

HDTV

On the subject of standards with respect to h.d.tv as discussed in your February 1986 issue it is nice to think that the television industry is choosing a standard from the film industry, the aspect ratio of the new system, IBA's 5:3 (1.66:1). Does this mean another showing of all the old films, this time around the viewer seeing what was cut off before?

Roger Sharland
Sharland Electronics
New Southgate
London N11

NEW LOGIC SYMBOLS

In answer to Mr Eyckmans' letter in the January issue, there is nothing mystical about Grindrod's circuit on page 59 of the October 1983, but it is rather clever. Just looking at the circuit and its text, that is without reference to any other information, you should be able to see that it relies on the fact that roms are normally never written to by the processor. The interesting aspect of the circuit is that it uses this redundant write function to select roms.

An address for the required rom is placed on the lower three bits of the data bus and written to the circuit. All that the rest of the logic does is to latch and decode the address. Had we expanded the description and added explanations of the 'telephone numbers' and boxes — which are already published in data books — there wouldn't have been room for the cheap voltager doubler on the same page.

Continental students are surely as clever as ours, but I think that it would be more fruitful for you to explain this circuit to them and offer a prize for an equally useful one. We would all be interested in that. Incidentally the circuit was drawn as it was, with consecutive pin numbers on the 'boxes', to simplify one-off p.c.b. design and later testing.

Martin Eccles
Technical Editor

FUNDAMENTALS OF ENERGY TRANSFER

I write concerning the discussion between Chris Parton, Ivor Catt and Phillip Drake (*WW* Dec., 1984, p.65, E&WW Feb., 1985, p.77 and E&WW Dec., 1985, p.19 respectively) under the above heading, particularly their remarks relating to the definition of the ampère. Some of the confusion has arisen because they have incorrectly generated the phrase 'NPL definition of the ampère'.

The ampere is the Système Internationale (SI) unit of electric current. The present definition of the ampère was adopted by the 9th Conférences Générales des Poids et Mesures (CGPM) 1948. This implemented the recommendation made two years earlier by the Comité Consultatif des Unités (CIPM: Resolution 2, Proc. Verb. *20*, 131, 1946) which comes under the authority of the CGPM. The CGPM consists of delegates from all the Member States of the Metre Convention and at present meets every four years. Their definition should not be referred to as the 'NPL definition of the ampère'.

It may interest readers that the NPL issues a 'Units of Measurement' Poster which is available (free) on request to: Information Services, National Physical Laboratory, Teddington, Middlesex TW11 0LW. The poster includes the agreed English translations of the definitions of the SI units which have been promulgated by the CGPM, references to further publications concerning the SI units, and the organisations which are responsible for them.

B W Petley
Division of Quantum Metrology
NPL, Teddington

COMPUTER CONTROLLED RADIO RX

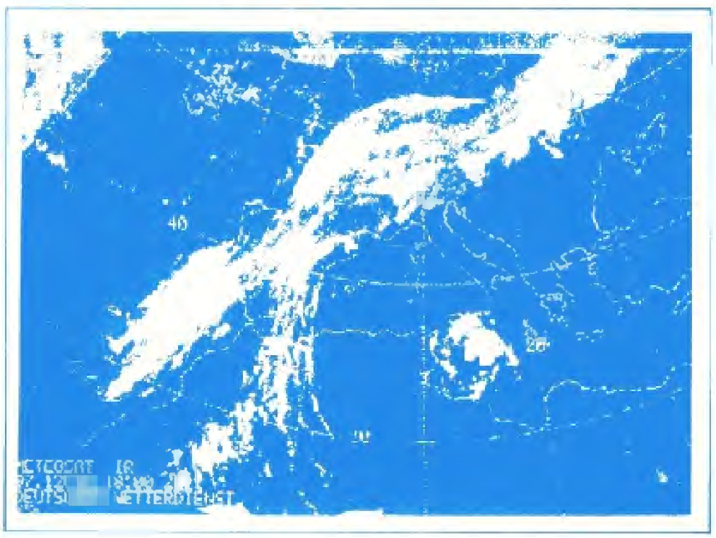
I was interested to read the above article by D.W. Harris, as it could almost have flowed from my own pen — viz. I am a BBC micro owner, have had an ICF2001 for some years and also studied electronic engineering at Southampton University, leaving 2 years before Mr Harris.

I have been considering possible applications for the Sony for some time, and Mr Harris's article was food for thought.

On the subject of interference from the BBC micro, I have been using the Sony as an input of FAX and RTTY to the BBC for some considerable time. I suffered from fairly bad e.m.c. problems until hitting on the idea of low-capacitance audio isolation. This is achieved by the use of a telephone pickup coil taped to the centre of the loudspeaker grill. This produces several tens of millivolts and I then amplify this by means of a small amplifier (telephone pickup amplifer). Physical separation of a couple of metres between receiver and micro cuts down radiated e.m.c.

The output can be applied direct to the cassette tape input. I have added a switch to connect the BBC's tape interface u.l.a. to one of the joystick push-button inputs. With suitable software which uses the line interleaving to obtain a suitable aspect ratio, very acceptable FAX pictures can be obtained from h.f. weather broadcasts. I have included two such examples. The l.f. transmissions were actually received using an old germanium transistor radio board on 134 kHz with the Sony used as a tuneable i.f.

A.F. Abbey
Stony Stanton
Leicestershire



RAKES' PROGRESS

I feel that Mr Catt (January 1986) has missed the purpose of mathematics in science. Mathematics provides a formal description of a theoretical model for empirically discovered results. Such a description is necessary for predicting other results from those already discovered.

Since the mathematical description is of a model, it cannot be expected to fit the world, warts and all. The model will deal with an idealisation; in particular, since the model is not a description of all and everything, it will entail concentrating on some effects and ignoring others. Hence the problems with defining (e.g.) ampères experimentally. Further, formulisations based on "real" numbers entail using limits which are impossible experimentally. Overcoming these problems means inventing a better model, one which includes more forces, or can be described by quantised mathematics.

The universe is quite complex, and it is often useful to deal in idealisations which ignore "irrelevant" forces. Presumably, the next round of "complete" or unified theories will bring together astrophysics, electromagnetism and subatomic physics; however, I suspect that predicting simple effects from such a theory will be very complicated.

It is for precisely the above reasons that it is wrong to attack the use of mathematics in computing science. Here, one is dealing with a situation which is wholly understood, since it has been created synthetically. One can produce complete mathematical descriptions of (e.g.) the languages in use. It is the very artificiality of the computing science world that allows this accurate formalisation, in contrast to the situation generally in physics.

Whilst I agree that there is a temptation to set examples on the mathematical description of a theory (simply because such questions are easily set) this does not detract from the importance or usefulness of mathematics in describing theoretical models.
Professor Leslie Smith
University of Stirling

BLACK BOXES

I was interested to read, though not without some disappointment, of the decline in the number of youngsters becoming interestested in the hobby of amateur radio, (*WW* January 1986, p.64). Could this have anything to do with the black box syndrome that has increasingly typified the hobby in the last 20 years, I wonder? The first and most obvious reason is the cash requirements of getting set up for instant QSO on whatever bands are being considered: the other being the inscrutability of the guts of the equipment. Phase-lock-loop detectors, r.i.t circuitry, microprocessor-controlled scanning, to mention but three functions commonly found on a modern rig involve a level of complexity which must baffle and isolate the newcomer. The pleasure I have had from running 30 watts c.w. through a frame output tv valve driven into the blue, all homebrew, far exceeds that to be had from black box technology and it is this element of the magic of radio that I think is missing. The boots and braces radio ham is a dying breed and therefore, some would argue, amateur radio is following along the same track.
Dr M. Buck
British Telecom
Cardiff

RENTING THE SPECTRUM

In criticising my IEE lecture, your correspondent ('Communications Commentary', Dec. 1985) missed or misunderstood two important issues.

First, the sole purpose of the Window Tax in the 17th century was to raise revenue. Its bad effect was to induce people to brick up their windows to reduce their tax, thus *reducing* the total number of windows in the country. Nobody was better off, except the Treasury. But if some spectrum users reduced their bandwidths, shared with others or moved to less crowded bands so as to save rent, that would *not* reduce the total size of the spectrum. The bands they no longer occupied could then be taken up by all sorts of would-be users who are at present unable to get licences. Your correspondent reported the ways in which, as I explained, present users could release substantial bands of useful spectrum if they had any financial inducement to do so — but he omitted to mention the benefits which their actions would bring to those frustrated would-be users.

The second point is more general. It is not enough to reject a proposed solution to a real problem, without saying what you would do instead. By rejecting, out of hand, any use of the price mechanism to apportion the spectrum, your correspondent is tacitly supporting a continuation of the present method, which the Merriman Report described as 'a somewhat arcane businss'. 'Arcane' means 'secret' and your correspondent has allied himself with the large established users — the spectrum 'haves' who staked their claims under that system before there was a shortage. But some of your readers may be among the small latecomers — the spectrum 'have-nots' who are still waiting patiently for the benefits of current radio-technology. The Merriman Report forecast that their number will increase over the next 5 to 10 years, even after the substantial re-allocations in Bands I and III. Some of them might prefer to pay something instead of waiting for an indefinitely long period. If so they can now read my lecture in the January issue of the IEE Journal, Part A.
David Rudd
Department of Transport
London SW1

ENERGY TRANSFER

Recently, since Ivor Catt first elaborated his iconoclastic views, several Wireless World readers have surfaced with their own problems relating to electric current theory. To these I would like to add my own.

At school, I was taught that the resistance of a conducting wire was inversely proportional to the cross-sectional area of the wire.

$R \alpha 1/A \alpha 1/r^2$ (where r = radius of the wire) This seemed reasonable since, just as with water running down a pipe, the thicker the wire/pipe, the more space there would be for the charge/water to pass through.

Later, I learned that electric charge only flowed along the surface of a conducting wire, (down to a certain small "skin depth"). This seemed to square with the idea that the residual charge on a conductor is to be found on the surface. However, this would lead one to imply that the resistance would be inversely proportional to the cross-sectional perimeter of the wire.

$R \alpha 1/r$

Furthermore, does a hollow conducting wire (with wall thickness greater than skin depth) have the same resistance as a solid conducting wire of the same radius?
Ivan L. E. Fant
Stoke Newington
London N6

TELEPHONE RECORDING

This circuit (circuit ideas, November 1985), contributed by Mr H. T. Wynne, has several serious failings, which make it unsuitable for connection to the British Telecom network.

The mains voltage of the cassette recorder power supply is not adequately isolated from the telephone line. A 600 Ω isolating transformer of 1:1 ratio should be connected to the terminations A and B via a suitable fuse — 250 mA quickblow is suitable.

It should be remembered that the ringing voltage on the line is far higher than the 37 V mentioned, and can give a serious shock. Even through a step-down transformer, it is risky connecting this to a tape-recorder microphone input, especially without a fuse.

Telephones incorporate a Varistor to ensure that, irrespective of local loop length, the volume at the telephone handset remains at a suitable level. Without this regulator, this circuit may deliver too much, or too little, power to the input of the recorder for satisfactory recording.

Connecting this circuit to the telephone line may make it impossible to dial out on any telephone connected to that line. The dial contacts (or transistor switch if a pressbutton telephone is used) will be shorted out by this cirucit, and the central office may be unable to distuinguish between 'connected' and 'disconnected' states of a loop-disconnect line.

This circuit has *not* received BABT approval, and it is therefore *illegal* to connect it to the telephone line. BABT will not grant approval to DIY constructed apparatus as standards cannot be guaranteed. This circuit should be marked in accordance with the marking Order — it would be a service to your readers to indicate that if they build and connect this circuit they will be breaking the law. Of course, Mr Wynne has almost admitted openly to doing so, and runs the risk of prosecution.

The building of telephone attachments cannot be advised unless the constructor knows exactly what he is doing, unlike domestic wiring of telephone sockets, which is not technically difficult, and, if a complete kit is used, unlikely to have any adverse effect on the safety and integrity of the network.
O. F. Carter
Aberystwyth
Dyfed

STEREO HISS

Mr Peter Hirschmann in his letter (**EWW**, January 1986, p.40) advocated abandoning the system presently used for radio broadcasting on v.h.f.-f.m. in favour of a new system which would give a better signal to noise performance in stereo. He suggested that such an improvement would not have to be made compatible with the present system.

When broadcasters contemplate changing an existing system, whether it is to add additional service or to improve some aspect of the present system, one of the primary considerations has to be that of compatibility. No change can be made until it has been conclusively shown that the services presently enjoyed by listeners or viewers will not be noticeably degraded. Changes that are not compatible with existing systems inevitably have to be added as additional or duplicate services and the changeover can then take literally years. For example, the complete conversion from 405-line to 625-line television in the UK took more than 15 years.

The present system used for stereo broadcasting on v.h.f.-f.m. was adopted largely because it was compatible with the existing monophonic receivers. Today over half of all listening to BBC v.h.f.-f.m. broadcasts is still done on portable mono receivers. Therefore, compatibility with these mono receivers would still be a prime requirement of any new system.

I am sure that today, starting from scratch, a new stereo broadcasting system (possibly using digital techniques) could be devised that would give a better performance than the present system. For example, a possible digital stereophonic system for use with television was described in the July 1984 edition of *Electronics & Wireless World*. However, in view of the large investment that has been made by members of the public in the purchase of both stereo and mono receivers for the present v.h.f.-f.m. system, I feel that overall compatibility would have to remain one of the main requirements of any new system.
Henry Price
Assistant Head
Engineering Information
Department
BBC

by William E. Barr

Digital input circuitry using voltage comparators

Versatile alternative to the Schmitt trigger, with input protection

The usual method of converting analogue signals into digital form is to feed the analogue signals into a Schmitt-trigger circuit. Although t.t.l. types of trigger are readily available, their voltage thresholds are normally set at fixed levels (about +0.8 volt and 1.6 volts) and these are restricted in use to operate from a single 5 volt supply. C-mos trigger circuits have more tolerance of supply voltage but also suffer from fairly defined threshold potentials.

Voltage comparators are easily designed to operate as Schmitt triggers. However, the type of comparator chosen should have an output terminal which can switch to the extremes of the supply. In spite of their limited switching speed (compared with t.t.l. devices) comparators offer several advantages. It is easy to design both inverting and non-inverting trigger circuits around them using a minimum of external components. They may operate off single or dual power supplies and the voltage switching thresholds may be set as desired over the full range of supply voltage. Finally, because their inputs have high impedance (typically megohm) it is easy to incorporate input over-voltage protection circuitry using clamping diodes.

This article describes the design of inverting and non-inverting Schmitt trigger circuits. In addition, some ways of providing adequate input over-voltage protection are discussed. Methods of reducing hysteresis variation due to sourced impedances of connected devices are looked at.

Finally a short computer program is given which allows the user to input the values of external components in the design of an inverting trigger circuit. The program displays the design parameters and also provides the ratios of two pairs of alternative resistances needed to produce a non-inverting trigger circuit having the same switching characteristics.

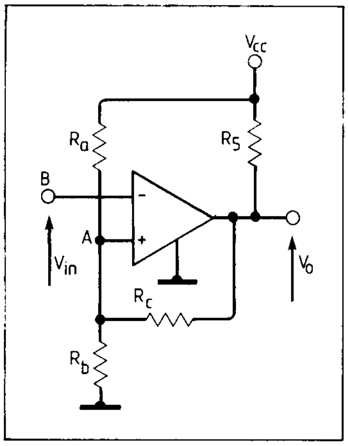


Fig. 1. Basic circuit of inverting trigger.

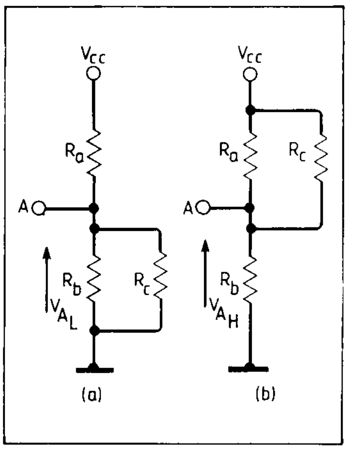


Fig. 2. Equivalent input circuit for low (a) and high (b) output states.

Basic inverting trigger

In the circuit of Fig.1 input analogue signals are applied to the inverting input of the comparator. Both the upper and lower threshold switching potentials are set by the resistors R_a, R_b and R_c. For input analogue signals with frequency less than 1 MHz, comparators such as the inexpensive LM339 (quad) or LM393 (dual) are ideal. The resistor R_c must be made very much larger in value than the output pull-up resistor R_5 so that the output terminal of the comparator can go to both of its bistable states of ground and V_{cc}. The potential of the non-inverting input, A, switches between two thresholds set by R_a, R_b and R_c. To understand how these are set, suppose a large voltage is applied at input B. This causes the output to go low, ideally to ground potential. Figure 2(a) shows how A's potential is fixed. Here V_a is given by

$$V_a = \frac{(R_b//R_c).V_{cc}}{R_a + (R_b//R_c)} = \frac{R_p}{R_c} = V_{cc}$$

where $R_p = R_a//R_b//R_c$.

For the output to switch to V_{cc} the potential of B must fall below this value of V_a, so that the low threshold at B is

$$V_l = \frac{R_p}{R_a} V_{cc}. \quad (1)$$

When V_b falls below this value the potential of A rises to a new value which can be found from Fig.2(b). This new value of V_a is

$$\frac{R_b V_{cc}}{R_a//R_c + R_b} = (1 - \frac{R_p}{R_b}) V_{cc}.$$

This means that the output will not go low again until V_b rises above this new level at A.

$$\text{i.e. } V_h = (1 - \frac{R_p}{R_b}) V_{cc} \qquad (2)$$

The hysteresis of the circuit is the difference between the two thresholds, say ΔV i.e.

$$\Delta V = V_h - V_l$$

or

$$\Delta V = (1 - \frac{R_p}{R_b} - \frac{R_p}{R_a}) V_{cc}$$

from which

$$\Delta V = \frac{R_p}{R_c} V_{cc} \qquad (3)$$

However, in practice suitable values of R_a, R_b and R_c must be based on the known value of V_{cc} to give the desired values of V_h and V_l. The first step then is to choose V_h and V_l arbitrarily. When this is done the three feedback resistor values may be calculated as follows. Combining equations (1) and (3)

$$\frac{\Delta V}{V_l} = \frac{R_p R_a}{R_c R_p} = \frac{R_a}{R_c} = n \qquad (4)$$

while from equation (2) we have

$$V_{cc} - V_h = \frac{R_p}{R_b} V_{cc}$$

and combining this with equation (1) we find that

$$\frac{V_l}{V_{cc} - V_h} = \frac{R_b}{R_a} \qquad (5)$$

Also, from equations (1) and (2) we obtain

$$\frac{V_h}{V_l} = \frac{R_b.(R_a + R_c)}{R_b.R_c} = 1 + n$$

If a value of R_a is chosen, then the values of R_b and R_c can be obtained, since they are now defined in terms of R_a i.e.

$$R_c = \frac{R_a}{n}$$

and

$$R_b = \frac{V_l}{V_{cc} - V_h} R_a$$

However, it is also convenient to express R_a and R_b in terms of R_c and this can be done as follows.

$$\frac{R_b}{R_c} = \frac{R_b}{R_a} \times \frac{R_a}{R_c} = \frac{V_l}{V_{cc} - V_h} \times \frac{\Delta V}{V_l}$$

i.e.

$$\frac{R_b}{R_c} = \frac{\Delta V}{V_{cc} - V_h}.$$

This means that a suitable value of R_c may be first selected, from which the value of R_a and R_b are obtained using the relationships

$$R_a = nR_c$$

and

$$R_b = \frac{\Delta V}{V_{cc} - V_h} R_c.$$

Basic non-inverting trigger

Figure 3 illustrates a non-inverting trigger circuit. Here the feedback resistors R_e and R_f (along with the supply voltage V_{cc}) set the value of hysteresis of the circuit. However, V_h and V_1 lie above and below some reference voltage, V_{ref}, applied to the inverting input of the comparator. Resistors R_6 and R_7 are used to fix V_{ref}. As in the previous trigger circuit, R_5 should be made very small in comparison with R_f.

In this circuit the input signals are applied to the non-inverting input via R_a. To understand how R_e and R_f set the switching threshold voltages, suppose the input potential is below V_1. Consequently the output is grounded. Figure 4(a) indicates the relevant potentials.

For the circuit to switch, V_{in} must rise to a value that makes V_a go above V_{ref}. This occurs when

$$V_{in} = V_{ref} (1 + \frac{R_e}{R_f})$$

i.e.

$$V_h = V_{ref} (1 + m) \qquad (7)$$

where

$$m = \frac{R_e}{R_f}.$$

The potential of A immediately rises to a value greater than V_{ref} after switching because the terminal of R_c, connected to the output, rises to V_{cc}. This is shown in Fig.4 (b). where

$$V_a = V_h + \frac{R_e}{R_e + R_f} (V_{cc} - V_h)$$

i.e.

$$V_a = \frac{R_p}{R_e} V_h + \frac{R_p}{R_f} V_{cc}$$

where $R_p = R_e // R_f$.

For the comparator's output to switch back to ground, the value of V_{in} must fall to some value, V_1, such that V_a becomes equal to V_{ref}. This condition is shown in Fig. 4(c). Here

$$V_a = V_{ref} = \frac{R_f}{R_e + R_f} V_l + \frac{R_e}{R_e + R_f} V_{cc}$$

i.e.

$$V_l = V_{ref} (1 + m) - m V_{cc}. \qquad (8)$$

The hysteresis of the circuit is

$$\Delta V = V_h - V_l$$
$$= V_{ref} (1 + m) - [V_{ref} (1 + m) - m V_{cc}]$$

i.e.

$$\Delta V = m V_{cc}. \qquad (9)$$

Summing up this circuit, the design steps are straightforward once the values of V_{cc}, V_h and V_l have been decided i.e.

$$\frac{\Delta V}{V_{cc}} = \frac{R_e}{R_f} = m$$

so that

$$R_e = m R_f$$

and

$$V_{ref} = \frac{V_h}{1 + m}.$$

The value of V_{ref} is related to V_{cc}, R_6 and R_7 by

$$V_{ref} = \frac{R_7}{R_6 + R_7} V_{cc}$$

or

$$R_7 = \frac{V_{ref}}{V_{cc} - V_{ref}} R_6. \qquad (10)$$

Input over-voltage protection

Figure 5 shows one simple method of incorporating over-voltage protection. The input signal is applied via R_1 (the excess voltage dropping resistor) which is in a series with the trigger's input. Diodes D_1 and D_2 provide voltage

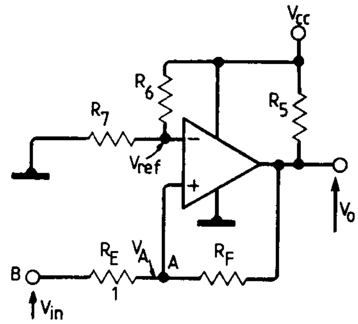


Fig. 3. Non-inverting trigger.

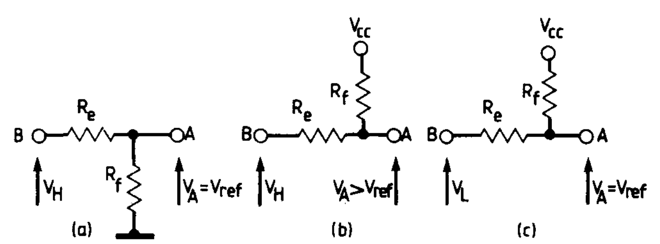


Fig. 4. Equivalent input circuit of Fig. 3 for low (a) input. At (b) is the condition after a rise of input voltage and at (c) the condition for switching V_0 to GND.

Fig. 5. Simple over-voltage protection, with clamping diodes; giving inadequate protection.

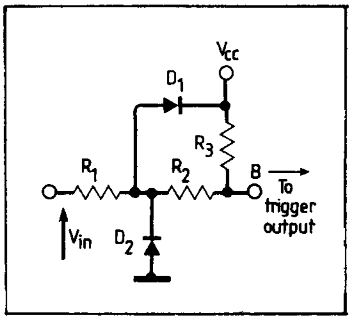
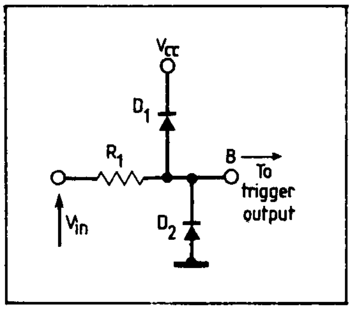


Fig. 6. Resistors R_1 and R_3 provide additional protection.



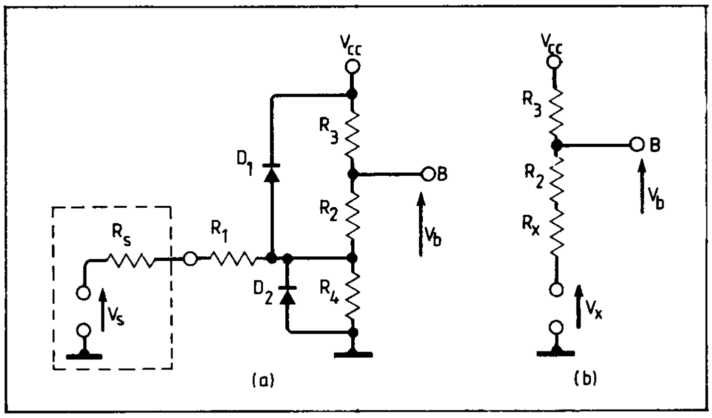


Fig. 7. Resistor R_4 reduces dependence of V_b on R_s at (a). Thévenin equivalent is shown at (b).

Fig. 8. Inverting (a) and non-inverting (b) trigger circuits in final form, with speed-up capacitors C_1.

clamping. If V_{in} rises above V_{cc} + 0.5 volt, then D_1 conducts, clamping the terminal, C, to one forward diode volt drop above V_{cc}. The excess voltage dropped across R_1 must be no greater than V_r. Here

$$V_r = \sqrt{PR_1}$$

where P is the rating of R_1 in watts and R_1 is in ohms. If negative input voltages are applied, diode D_2 will conduct, clamping C at one diode volt drop below ground potential. Unfortunately, this will not adequately protect a comparator operating off a single supply voltage. Many comparators have their input terminals which must not go more negative than 0.3 volt below the negative supply rail or damage will result. One way round this problem is to include resistors R_2 and R_3 as shown in Fig. 6. Under large negative input voltage, D_2 conducts clamping C to $-V_d$ while the potential of B becomes

$$V_b = -V_d + \frac{R_2}{R_2+R_3}(V_{cc}+V_d)$$

Clearly then, if V_b can be prevented from going below ground potential a large margin of safety results. This situation is established provided

$$\frac{R_2}{R_3} \geq \frac{V_d}{V_{cc}}$$

The transfer function of this protection circuit for input voltages between V_{cc} and ground is given by

$$V_b = p\,V_{in} + (1-p)V_{cc}$$

where

$$p = \frac{R_3}{R_1+R_2+R_3}.$$

However, this is true only for signal sources having negligible output impedance. In practice the signal source, V_s, has finite impedance. Let us assume it is purely resistive and of value R_s. Where R_s is not negligible compared with the series combination of R_1 and R_2, the value of V_b will alter appreciably (for a given value of V_s applied) when the variation of R_s is significant. This variation of V_b may be reduced by including the resistor R_4 as shown in Fig. 7(a).

The Thévenin equivalent is given in Fig. 7(b), where

$$R_x = R_4//(R_1+R_s)$$

and

$$V_x = \frac{R_4}{R_1+R_4+R_5}$$

The transfer function of the circuit in terms of V_x is

$$V_b = V_x + \frac{R_2+R_x}{R_2+R_x+R_3}(V_{cc}-V_x).$$

Expressing this in terms of V_s we have

$$V_b = \frac{R_3 . R_x}{R_t . (R_1+R_s)}V_s + \left(1-\frac{R_s}{R_t}\right)V_{cc} \qquad (11)$$

where

$$R_t = R_x + R_2 + R_3.$$

One obvious effect of this protection circuitry is the attenuated hysteresis of output compared with input. In other words, the difference in voltage thresholds of the source is greater than those of the trigger circuit. The attenuation factor is

$$\frac{\Delta V_b}{\Delta V_s} = \frac{R_3 . R_x}{R_t . (R_1+R_s)}.$$

One important point may be easily overlooked. When the ground potential input terminals are open-circuited, the potential at B, V_{bo} is fixed by the potential divider formed by R_2, R_3 and R_4 where

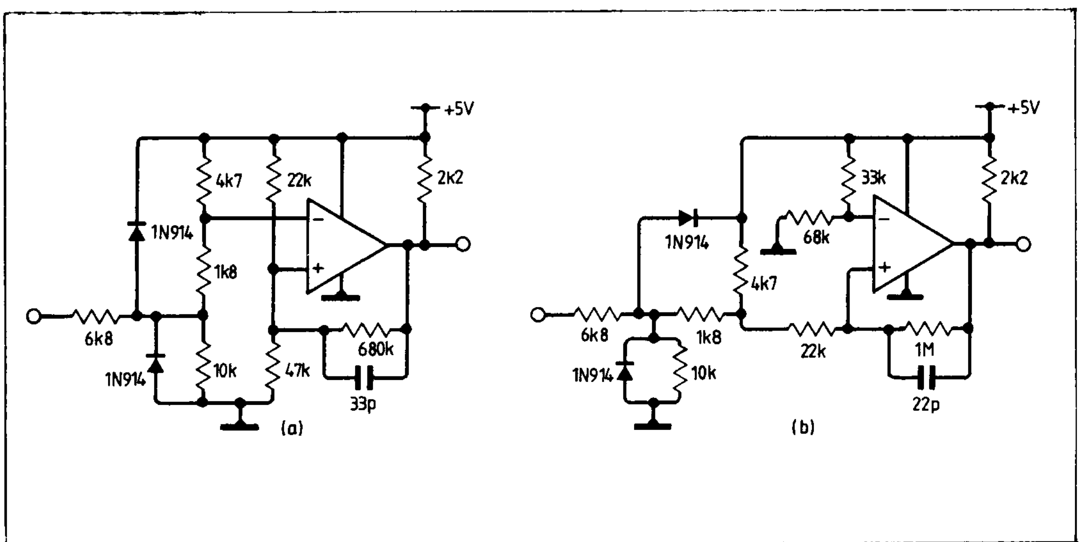
$$V_{bo} = \frac{R_2+R_4}{R_2+R_3+R_4}V_{cc}. \qquad (12)$$

It is important that this does not lie within the deadband of the trigger circuit. It should therefore be arranged that either

$$V_{bo} > V_h \quad \text{or} \quad V_{bo} < V_l$$

to ensure that the comparator's output digital state is clearly defined in the open circuit input condition.

The circuits of Fig. 8(a) and Fig. 8(b) illustrate the inverting and non-inverting trigger circuits respectively with their protection circuitry. Capacitor C_1 is added to both circuits to enhance the switching speed.



Design example

Suppose we wish to design both types of trigger circuit (inverting and non-inverting) with identical characteristics, to operate from a single 5 volt supply. In addition they are to be protected for input signals over the range of +40V to −40V and it is desirable to have threshold levels of about +2.5V and +2.0V with respect to the input terminals. The first step we may take is to select the value of R_1. If a 0.25 watt resistor is used, the minimum value of R_1 is found by

$$R_{1\,(min)} = 1600/0.25 = 6.4 \text{ kilohms}$$

The nearest preferred value is 6k8, so this is chosen. One possible inverting circuit is shown in Fig. 9(a). The threshold voltages at the comparator's non-inverting input are found as follows.

$$R_p = 22k//47k//680k = 14.66k$$

also

$$n = \frac{22}{680} = 0.0324.$$

Using equation (1) V_l and V_h may be calculated using

$$V_l = \frac{14.66}{22} \times 5 = 3.33V$$

and

$$V = 3.33 \times 1.0324 = 3.44V.$$

When the source resistance, R_s, is zero the value of R_x and R_t are

$$R_x = 6.8\,//10k = 4.05k$$

and

$$R_t = 1.8k + 4.7k + 4.05k = 10.55k.$$

The corresponding transfer function becomes

$$V_b = 0.265\,V_s + 2.77.$$

To find the upper and lower threshold values of V_s make V_b equal to V_h and V_l respectively so that

$$V_{sh} = \frac{3.44 - 2.77}{0.265} = 2.53V$$

and

$$V_{sl} = \frac{3.33 - 2.77}{0.265} = 2.11V.$$

When R_s has a value of 10k, the new values of R_x and R_t become

$$R_x = 16.8k//10k = 6.27k$$

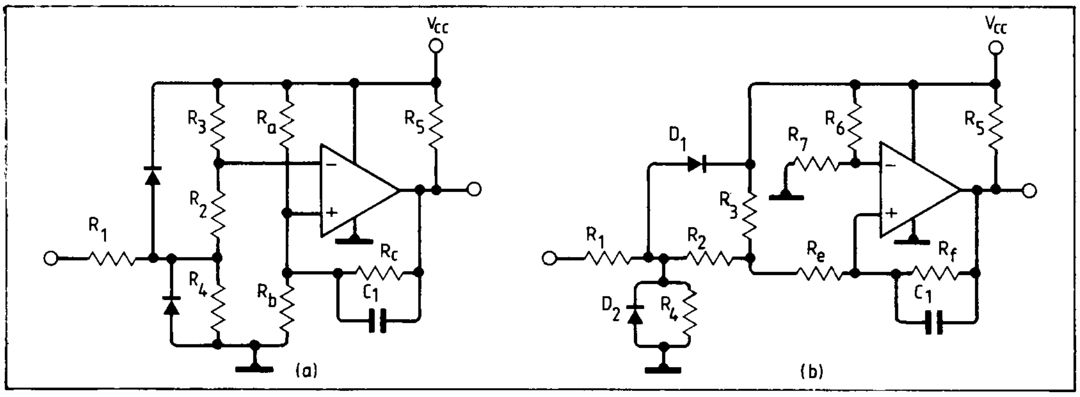


Fig. 9. Worked design examples of inverting and non-inverting triggers.

and

$$R_t = 1.8k + 4.7k + 6.27k = 12.77k.$$

The new transfer function is given by

$$V_b = 0.137\,V_s + 3.16.$$

The new threshold values of V_s may now be obtained as previously

$$V_{sh} = \frac{3.44 - 3.16}{0.137} = 2.04V$$

and

$$V_{sl} = \frac{3.33 - 3.16}{0.137} = 1.26V.$$

The value of V_{bo} is given by

$$V_{bo} = \frac{5 \times 11.8}{16.5} = 3.57V.$$

This is satisfactory since it lies above V_h and is outside the deadband region. To set these potentials accurately it is worth using 1% tolerance resistors in the design. Figure 10 indicates how the hysteresis, ΔV_s, varies with R_s. The variation is highly linear and may be extrapolated for values of R_s greater than 10k.

To obtain a non-inverting trigger having the same characteristics we use the same input protection circuitry. It only remains to find suitable values of R_e, R_f, R_6 and R_7 to replace R_a, R_b and R_c.

The values of V_h and V_l must be maintained at 3.44 volts and 3.33 volts. From equation (9) we have

$$\frac{\Delta V}{V_l} = \frac{R_e}{R_f} = 0.22$$

or

$$R_e = 0.022\,R_f.$$

Suitable values are therefore R_f = 1 megaohm and R_e = 22k.

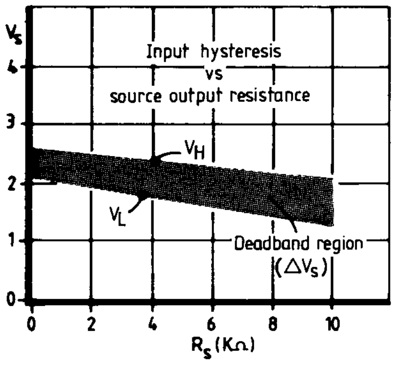
From equation (7) we have

$$V_{ref} = \frac{3.44}{1.022} = 3.366V.$$

```
        RS        VHS         VLS
         0        2.519       2.113
         1        2.472       2.027
         2        2.424       1.942
         3        2.376       1.856
         4        2.329       1.771
         5        2.281       1.685
         6        2.234       1.6
         7        2.186       1.515
         8        2.138       1.429
         9        2.091       1.344
        10        2.043       1.258

   RA = 22  RB = 47  RC = 680  VCC = 5

   VH = 3.44 VL = 3.332  VBO = 3.576

   ************************************
   * R1= 6.8  R2= 1.8  R3= 4.7  R4= 10 *
   *                                   *
   * RE = .022 X RF       R7 = 2.06 X R6 *
   ************************************
```

```
1   REM     ****************************************
2   REM     *                                      *
3   REM     * DIGI-DESIGN  -  W.E. BARR  -  DEC 1983 *
4   REM     *                                      *
5   REM     ****************************************
10  TEXT : HOME : DIM VHS(21),VLS(21),RX(21),RT(21),RS(21)
20  PRINT "ENTER THE VALUE OF VCC (VOLTS)";: INPUT VCC
30  PRINT "ENTER THE VALUE OF RA (KOHMS)";: INPUT RA
40  PRINT "ENTER THE VALUE OF RB (KOHMS)";: INPUT RB
50  PRINT "ENTER THE VALUE OF RC (KOHMS)";: INPUT RC
60 RP = RA * RB * RC / (RA * RB + RA * RC + RB * RC)
70 VL = RP * VCC / RA:VH = VL * (RA + RC) / RC
80  HOME
90  PRINT "ENTER THE VALUE OF R1 (KOHMS)";: INPUT R1
100  PRINT "ENTER THE VALUE OF R2 (KOHMS)";: INPUT R2
110  PRINT "ENTER THE VALUE OF R3 (KOHMS)";: INPUT R3
120  PRINT "ENTER THE VALUE OF R4 (KOHMS)";: INPUT R4
130 RS = 0
140  FOR N = 0 TO 20
150 RX(N) = (R1 + RS) * R4 / (R1 + RS + R4):RT(N) = R2 + R3 + RX
    (N)
160 A = R3 * RX(N) / (RT(N) * (R1 + RS)):B = VCC * (R2 + RX(N)) /
    (R2 + R3 + RX(N))
170 VHS(N) = (VH - B) / A:VLS(N) = (VL - B) / A
180 VBO = VCC * (R2 + R4) / (R2 + R3 + R4):VBO =  INT (1000 * VB
    O + .5) / 1000
190 RS = RS + 1
200  NEXT N
210  HOME : PRINT  TAB( 8)"RS" TAB( 17)"VHS" TAB( 28)"VLS"
220  FOR N = 0 TO 10
230  IF N > 9 THEN T = 8
240  IF N < 10 THEN T = 9
250  PRINT  TAB( T)N TAB( 16) INT (1000 * VHS(N) + .5) / 1000 TAB(
    27) INT (1000 * VLS(N) + .5) / 1000
260  NEXT N
270  PRINT : PRINT " RA = ";RA;"  RB = ";RB;"  RC = ";RC;"  VCC
    = ";VCC
280 X = (VH - VL) / VCC:X =  INT (1000 * X + .5) / 1000:CR = 1 +
    X:VR = VH / CR:Y = VR / (VCC - VR):Y =  INT (1000 * Y + .5) /
    1000
290 VH =  INT (1000 * VH + .5) / 1000:VL =  INT (1000 * VL + .5)
     / 1000
300  PRINT : PRINT " VH = ";VH;" VL = ";VL;"  VBO = ";VBO: PRINT

310  PRINT "*************************************"
320  PRINT "* R1= ";R1;"  R2= ";R2;"  R3= ";R3;"  R4= ";R4;" *"
330  PRINT "*                                   *": PRINT "* RE
    = ";X" X RF" TAB( 22)"R7 = ";Y" X R6 *"
340  PRINT "*************************************"
```

Fig. 10. Variation of input hysteresis with source resistance.



To obtain the ratio of R_7/R_6 we use equation (10), from which

$$R_7 = \frac{3.366}{1.634} R_6$$

or

$$R_7 = 2.06\ R_6.$$

Suitable values are

$$R_6 = 33k \text{ and } R_7 = 68k.$$

The circuit of Fig. 9(b) has identical input switching levels to that of Fig. 9(a).

Computer-aided design

There are a few basic rules of thumb which aid the initial selection of some of the components used in these circuits. However, in the final selection the repetitive calculations are time consuming to say the least. It is very convenient to use a simple Basic program which prints out the parameters from the component values which the designer supplies . Trial and error, with the computer doing the real donkey work, can yield the final component selection in a short period of time.

The program was written for an Apple microcomputer, but is easily adapted to run on any other machine. It allows the user to input values of V_{cc}, R_a, R_b and R_c, which are processed to determine V_h and V_l. When the additional values of R_1, R_2, R_3 and R_4 are input, the program calculates and displays the upper and lower input terminal threshold potentials for input source resistances, varying in 1k steps, from zero to 10k. It also displays V_h, V_l and V_{bo}, indicating where the latter lies relative to the deadband region.

Finally the ratios of R_e / R_f and R_7 / R_6 are also given. In this way both inverting and non-inverting trigger circuit component values are provided. Other variations of program may be written using the design equations quoted. For example, the priority may be to set more stringent input hysteresis levels. In this case the optimum relative values of R_1, R_2, R_3 and R_4 may require to be evaluated first. V_h and V_l will then be established, from which the ratios of R_a: R_b: R_c will be determined. Some compromise will be inevitable, however, if the choice of resistor values is restricted to the common preferred value ranges.

Reference
Linear Applications Handbook, National Semiconductor Corporation, Application Note 74.
R.T. Smathers, T.M. Frederiksen and W.M. Howard

Human responses to 'intelligent' machines

continued from page 34

proposed that the mental experience and the space-time description of the physical world were two different groupings of the same reality, a 'neutral stuff', which could not be known in any other way. Rather similar is the theory of 'identity' — that the reality experienced subjectively and the reality described objectively are identical. The psychical and physical are two different aspects of it.

Let your mind alone
— James Thurber

The software programmable digital computer provides a modern metaphor for this sort of monism. Such a computer in operation can be decribed either on the level of its physical construction and successive electrical states or on the level of the abstract functions and logical relationships of its program. Both explanations are true but neither is complete in itself and we have no other way of knowing the reality of the machine.

Functionalism

It was perhaps the programmable computer, and certainly artificial intelligence, which contributed to the theory of functionalism as a philosophy of mind.[6] Here, as the name implies, function is everything. The question of what actually functions, whether living cells in humans or electronic devices in machines, is not important. So the physical processes which represent mental states are ignored in this theory, but the functional role of these states, their abstract causal relationships, is the thing that really matters. All meaning is conveyed by this functional role. Thus, in the words of J.A. Fodor writing in *Scientific American*, "Functionalism . . . recognizes the possibility that systems as diverse as human beings, calculating machines and disembodied spirits could have all mental states."

Obviously this theory is highly abstract, but it is attractive because it raises none of the problems of dualism or of materialism. It draws on modern ideas from computer science, artificial intelligence, linguistics, cybernetics and psychology. Furthermore it seems to provide something of a solution to the 'problem of other minds.' Causal relationships in the functioning of anything are objective and open to public inspection and debate. If mental states have this nature, as suggested by functionalism, then they must be accessible to scientific investigation like other things and events.

However, there are objections to the theory (see reference 6). One argues that it is just wrong. Another that it is true but in a very trivial way because any property in the world can be specified in terms of its functional role and causal relationships. But whether valid or not, functionalism is relevant to the present discussion because it is compatible with biological and technological realities and it provides a common factor in humans and 'intelligent' machines.

Summing up

If, as some philosophers argue, the common-sense, dualistic concept of mind is a mistake, we should not really be outraged by the idea that the processing activity we do perform could also take place in machines. Secondly, as the existence of 'other minds' can only be inferred in humans on the evidence of external behaviour, we would be at least consistent if we inferred that the activity we thus described as 'mind' could also go on in machines when the evidence of *their* external behaviour warranted it.

Thirdly, if functionalism is a valid theory, it gets rid of the weakness of having to rely on inference to solve the problem of 'other minds', because it proposes that the causal relationships in the functioning of mental processes are objectively real and therefore open to public inspection. Finally, if these philosophical considerations are reasonable, they could influence the way we perceive and react to 'intelligent' machines and hence the way we design and use them.

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A non-technical and easily understood explanation of the mind-body problem in the light of modern science and technology was given by Prof. J. Searle in the BBC's 1984 Reith Lectures, "Minds, brains and science." These were printed in *The Listener,* 8, 15, 22, 29 Nov., 6, 13, 20 Dec. 1984.

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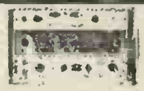

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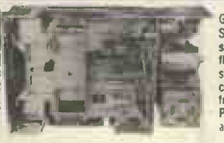

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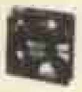

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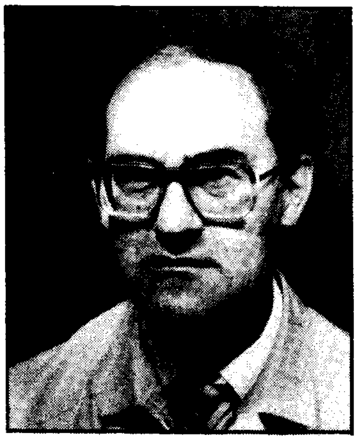
CIRCLE 65 FOR FURTHER DETAILS.

High-speed interface/buffer

by J.F. van der Walle, M.I.E.E.



J.F. van der Walle is senior experimental officer at Manchester University Physics Department and has been principally engaged in interfacing fast analogue-to-digital converters to computers. In addition he designs charge-coupled-device support circuits for use in nuclear experiments.

Using output from an a-to-d converter as an address, this buffer interface can store 500 million data words in 16Kbyte of memory.

When attempting to use high data-rate peripherals with a computer, one can find that the computer is too slow to collect the data and reset any flags involved. To overcome this problem I have designed a buffer interface to connect the peripheral device — in this case an analogue-to-digital converter, or a-to-d converter — to the computer.

Two static 8K-by-8bit memories are used to store around 537 million data words ($2^{13}.2^{16}=2^{29}$). To store this data block, the computer sends 8192 13bit addresses sequentially and receives 8192 16bit data words.

This action greatly reduces the amount of computing time required. Resetting of the end-of-conversion flag and a-to-d converter data storage are carried out independently of the computer within the interface.

Another advantage is that the converter runs at its maximum speed because the buffer interface resets the converter flag 300 to 500ns after the end of conversion; the computer has access to the data at all times.

The trick of the design is to use a-to-d converter output as an address (maximum 13bit) for the two 8k by 8bit memories. There are 13 address lines, A_0 to A_{12}, ranging from zero to $1FFF_{16}$.

Each time that the converter presents the same data word (0000_{16} to $1FFF_{16}$), the logic section of the buffer interface counts these data words and stores them in the data section of the memories. Counting must start with the memory contents set to zero. Considering the 8192 addresses as 8192 channels, by connecting the address lines of the two memories in parallel, with A_0 of the first memory to A_0 of the second and so on, a data-word width of 2^{16} is created.

This means that each channel can store 2^{16} counts. For example, if the converter generates data word $03F9_{16}$ 2663 times in a long run of conversions, then the data section of the two memories combined reads 2663 in address $03F9_{16}$.

Features

By using the HM6264P-12 static memory with an access time of 120ns data throughput is about 500kHz. This can be significantly increased by using faster memories and shift registers and raising clock frequency from 18MHz to 25MHz (40ns steps).

Large amounts of data can be stored — 2^{29} data-words — without any computer interruption, other than for magnetic tape storing and graphics. To store this block of data only 8192 direct memory access interruptions are needed.

The buffer takes only 900ns for storing one data word from the converter and 600ns for a computer read-request operation. To reset the buffer internally before starting a new data-acquisition run of 2^{29} data words takes only 110ms.

Bus system — data in

From the bus system diagram you can see that the data word of the converter, or any other external device, is loaded into latch/bus-driver $IC_{15,16}$ on the rising edge of pin 5 of IC_{30}. Simultaneously the converter receives a reset signal from pin 5 of IC_{30} through a monostable i.c.

The converter is now free to generate another data word. Note that the computer is not interrupted in any way. From $IC_{15,16}$ the data word is now transferred to register/counter $IC_{13,14}$, freeing $IC_{15,16}$ to accept another converter data word.

By enabling the three-state output of $IC_{13,14}$, the data word is presented to the address inputs of the two memories $IC_{10,6}$. Address decoding in $IC_{10,6}$ selects one of the 8192 locations (2^{13}), each consisting of a 16bit data word. Data acquisition runs start with all locations zeroed as detailed later.

With output enable $\overline{OE}$ low, data word zero appears on the input/output pins of $IC_{6,10}$ and is loaded into register/counter $IC_{7,11}$. Signal $\overline{OE}$ goes high again and the counter of $IC_{7,11}$ receives a clock signal which increments zero by one.

Output of $IC_{7,11}$ is enabled and the data word 0001 is written back into the memories using $\overline{WE}$. Note that the three-state output of $IC_{13,14}$ is enabled during reading from and writing to the memories, so this operation takes place in the same address location.

Because the a-to-d converter generates data words between values zero and $1FFF_{16}$, all address locations are used. If after a long data acquisition run the converter has generated a unique data word 2^{16} (65536) times, the buffer interface stops taking data, Fig. 1.

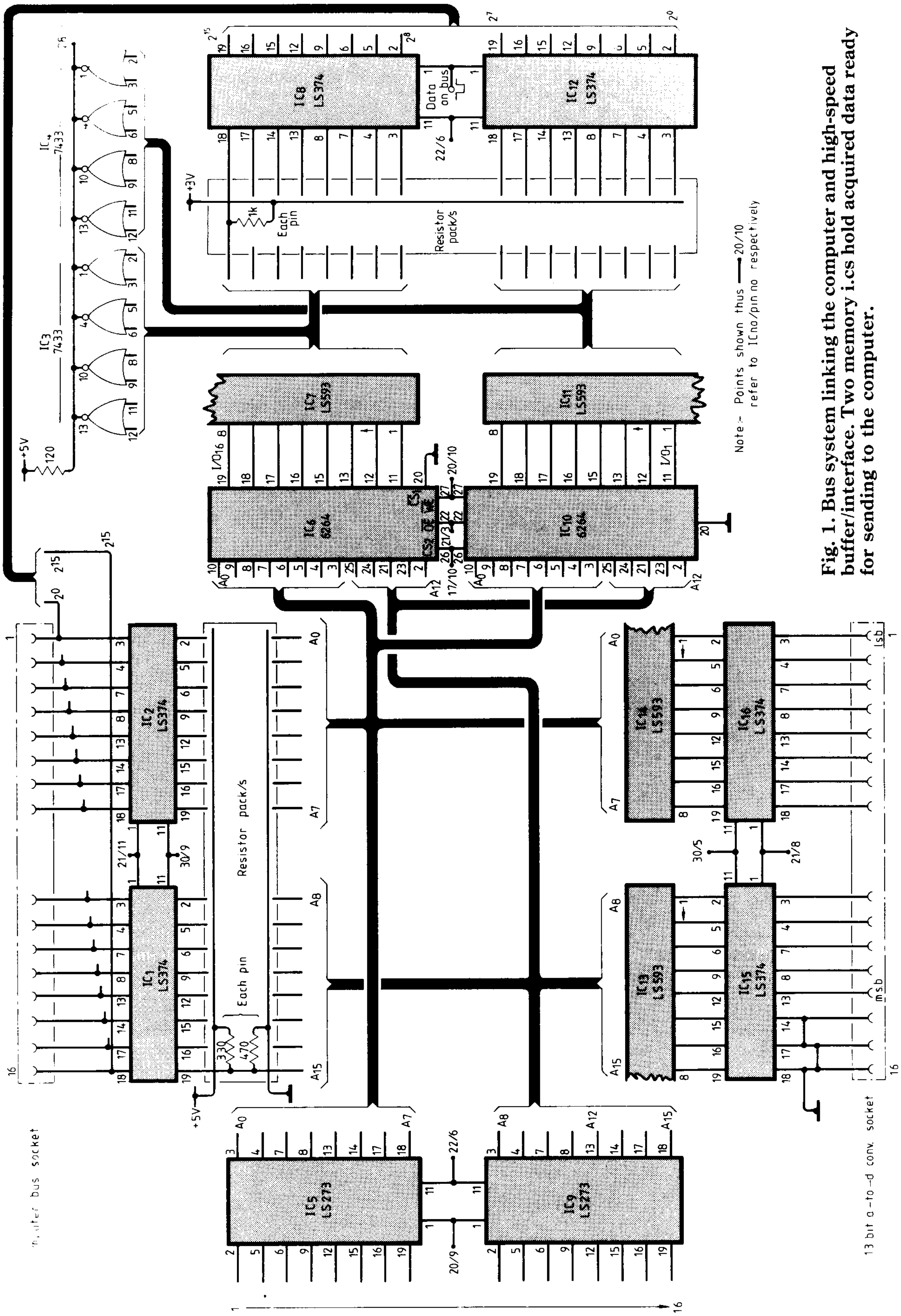


Fig. 1. Bus system linking the computer and high-speed buffer/interface. Two memory i.cs hold acquired data ready for sending to the computer.

Bus system — data out

The buffer interface now sets a flag — Data ready — to the computer. There are several ways of getting the data into the computer.

One alternative is to take only a few data words into the computer, i.e. if one wants to check only a few data channels. Another alternative is for the computer to take in all 8192 data words by sending all of the addresses in sequence and receiving the data words in return.

From the diagram follows that the computer puts a 13bit address word into latch/bus-driver $IC_{1,2}$. This word is presented to the memory address inputs by enabling the three-state output of $IC_{1,2}$. When low, signal $\overline{OE}$ transfers a 16bit memory data word into $IC_{8\text{-}12}$ and the Read data flag is set.

The computer now enables the three-state output of $IC_{8,12}$ and the 16bit data word goes through a 16-way data bus into computer memory. Direct memory access is here the best solution.

This procedure carries on until the computer has reached address-word 1FFF. Note that the data word goes through $IC_{8,12}$ and that each address from the computer is clocked sequentially into latch $IC_{5,9}$.

When address word 1FFF appears on the latch output, it resets the buffer interface through a NAND gate so that data acquisition resumes.

The computer has access to the data at all times, under light-pen or real time-clock control, while acquisition takes place.

From the bus system diagram you can see that the address bus links $IC_{1,2,5,9,13\text{-}16}$ and address inputs of the memories and is terminated by line resistors from resistor packs. Each line resistor is 330Ω in series with a 470Ω resistor to ground, so address bus voltage has a high level of about 3V and a low of approximately 400mV.

The internal data bus is formed by input/output of $IC_{6,10}$, $IC_{7,8,11,12}$ inputs and 16 terminator resistors of 1kΩ each connected to a 3V supply, Fig. 2.

Logic section

Dual bistable device IC_{25}, driven by an 18MHz oscillator, and decoder IC_{19} form the

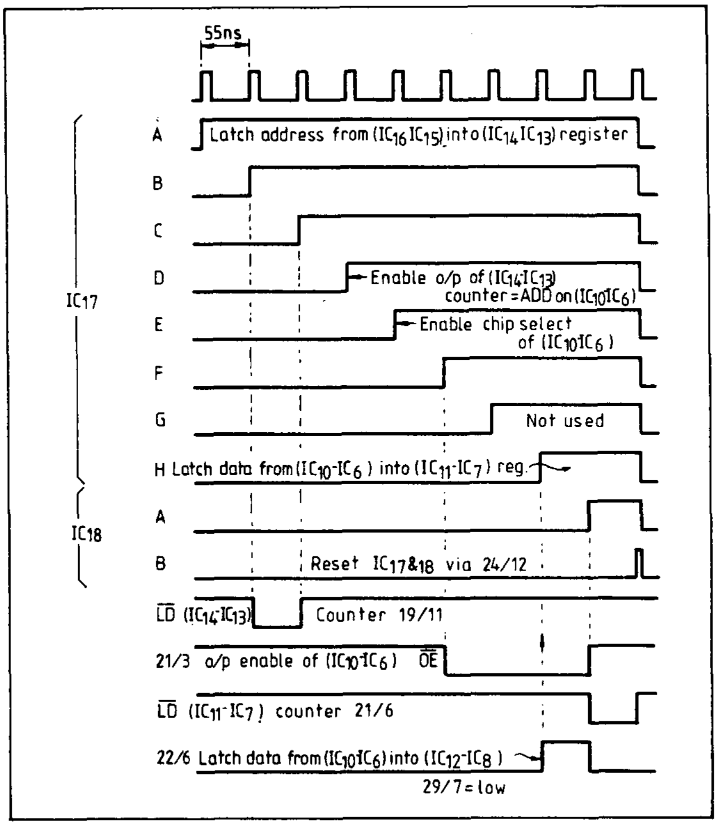


Fig. 2. Timing for data output. The 13bit address is latched then presented B to the memory address lines.

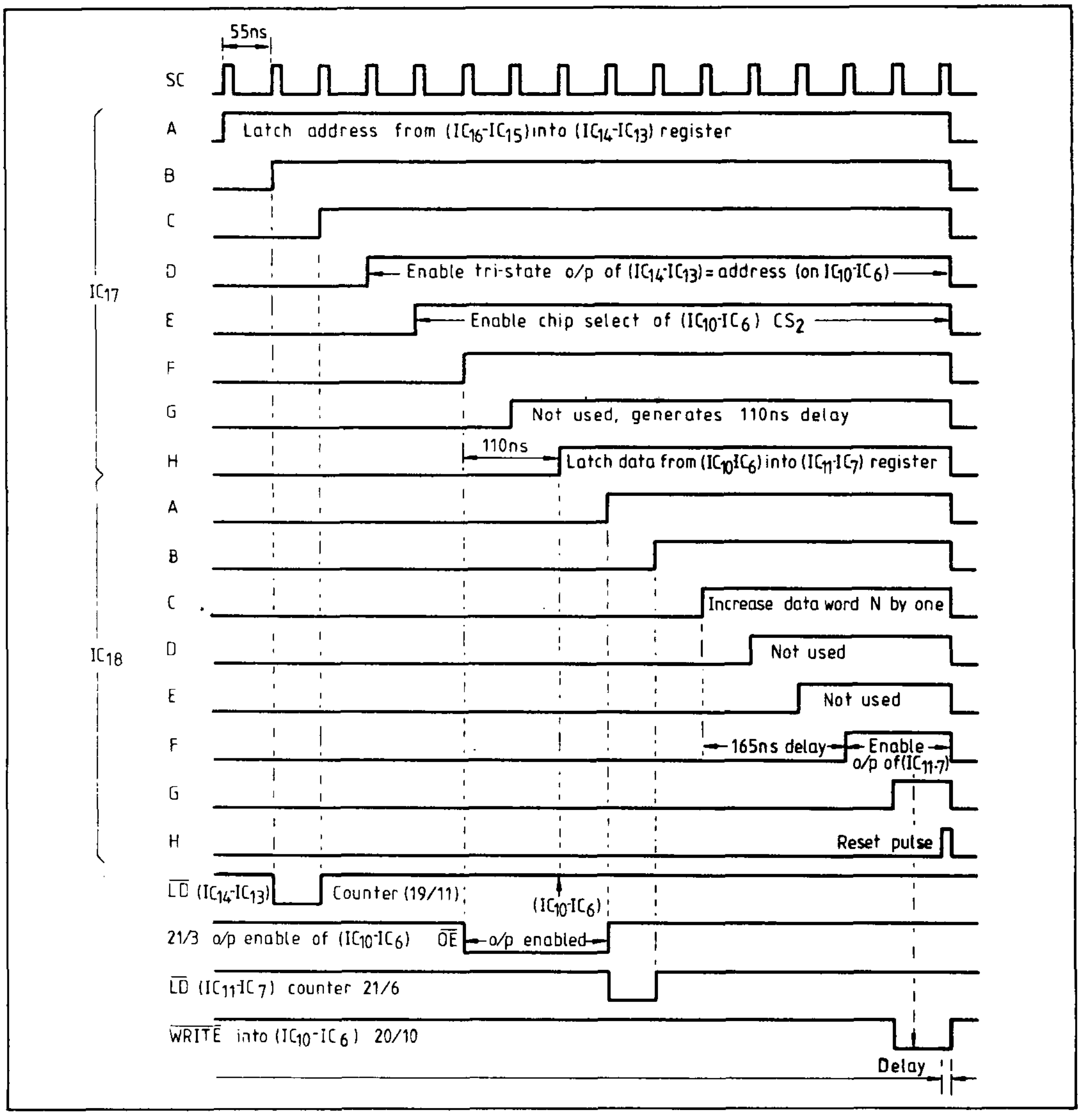


Fig. 3. Timing for data input. Shift register outputs determine the sequence. SC is the 18MHz system clock.

search and execute section of the buffer-interface. To prevent switching transients, the decoder-output sequence is 0-1-3-2-0.

When output three of decoder output IC_{19}, pin 7 goes low and there is a converter Flag signal at pin 11 of IC_{22} (low) or a read request signal, RDRQ, from the computer at pin 11 of IC_{30} (high), or both, bistable device IC_{30} will clock in those signals. The converter flag causes pin 5 of IC_{30} to go high and the converter data word is latched into $IC_{15,16}$; the read-request address-word from the computer is placed into $IC_{1,2}$ by pin 9 of IC_{30}.

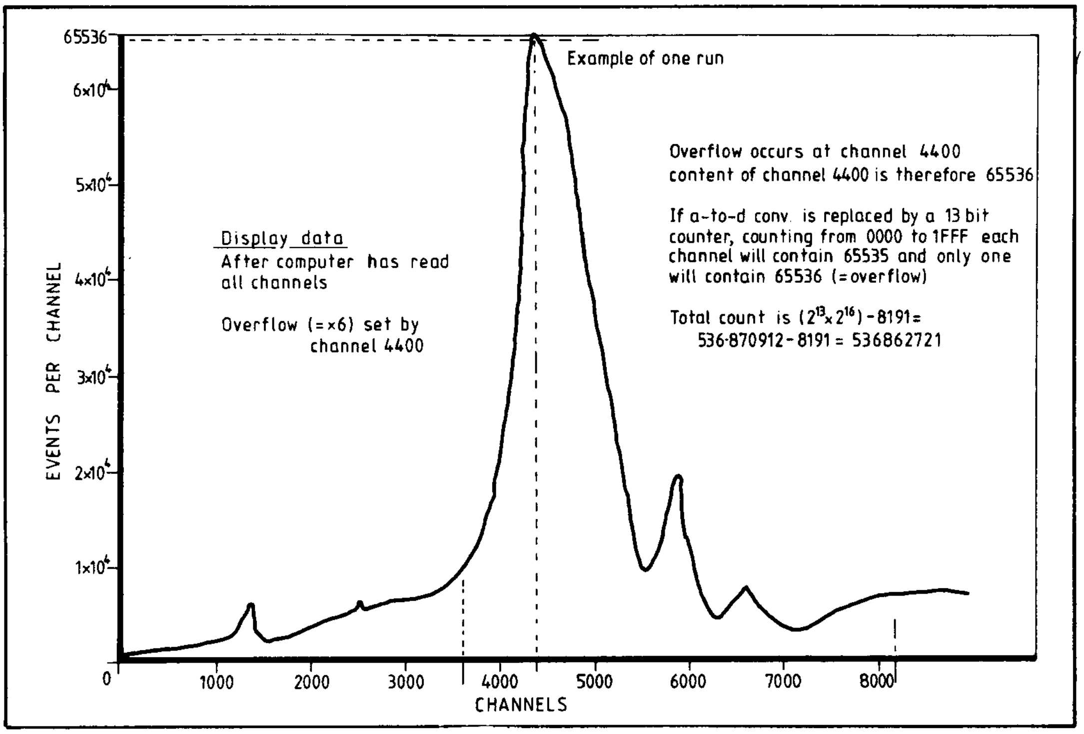
Next, decoder output pin 6 of IC_{19} goes low. Because pin 5 of IC_{30} is high, pin 6 of IC_{30} is low and pin 3 of IC_{29} is high. Pin 6 of IC_{29} goes low and causes a low on the preset of bistable device IC_{24}. As a result, pin 10 of IC_{24} goes high and serial-in parallel-out shift registers IC_{17} and IC_{18} generate a sequence of levels because inputs A_1 and B_1 of IC_{17} are continuously high. Converter data is now processed according to Table 1.

Storing of a converter data word takes approximately 900ns. Bistable device IC_{25} starts driving the decoder IC_{19} again which steps from zero to one. Read-request signal RDRQ causes pin 7 of IC_{30} to go low and pin 9 to go high.

When pin 5 of IC_{19} goes low, the low on IC_{30}, pin 7 will cause pin 7 of IC_{29} to go low and now the same sequence of events occurs. However, because pin 7 of IC_{29} is low, pin 6 of IC_{22} goes high for 55ns to load the data word from the memories into $IC_{8,12}$ and the address, as it appears on the address bus, into $IC_{5,9}$.

Another difference is that now pin 5 of IC_{29} is low again so bistable device IC_{24} changes state on the leading edge of pin 4 of IC_{18} preventing any writing into the memories. Hence data in the memories will not be incremented or corrupted during RDRQ Fig. 4.

Control logic circuitry, memory operation and data transfer are subjects of the next and final article. Some i.cs mentioned here appear in the control logic circuit.



Results from one run after overflow in location 4400_{10}. This means that the a-to-d converter produced the word 1130_{16} a total of 65536 times. Data for this display came from a scintillation counter measuring a radioactive material. The buffer/interface is particularly suited to testing high-speed a-to-d converters for linear performance at maximum conversion speed.

Table 1. Shift registers determine the converter data processing sequence.

IC	Pin	Function
17	3	Clocks data word from $IC_{15,16}$ to register $IC_{13,14}$. Bus driver $IC_{15,16}$ is enabled by IC_{21}, pin 8.
17	4	Disables $IC_{15,16}$ output and loads counter $IC_{13,14}$ with data.
17	5	End of load pulse.
17	6	Enables bus-driver output of $IC_{13,14}$. Data word now appears at address inputs of $IC_{6,10}$.
17	10	Enables chip-select on $IC_{6,10}$.
17	11	Removes preset through pin 9 of IC_{26} from IC_{24} pin 11, enables output of $IC_{6,10}$. The data word belonging to the specified address now appears on $IC_{6,10}$ i/o pins.
17	12	Unused, gives a delay of 110ns between previous and following steps.
17	13	Enables inputs A_1 and B_1 of IC_{18} and clocks data word from $IC_{6,10}$ to register of $IC_{11,7}$.
18	3	Loads data word from register of $IC_{11,7}$ into counter of same i.cs. Output enable OE goes high.
18	4	End of load pulse.
18	5	Increments counter contents of $IC_{11,7}$ by one.
18	6,10	Unused, giving 165ns delay between previous step and the next, allowing the counter to ripple through.
18	11	Enables bus driver of $IC_{11,7}$.
18	12	Writes incremented data word back to $IC_{6,10}$. Because IC_{17} pin 6 is still high, reading and writing into $IC_{6,10}$ occurs in the same address location.
18	13	Clears bistable device IC_{24}, sending reset to pins 6 of $IC_{29,30}$, and sets pin 9 of IC_{24}, Fig 3.

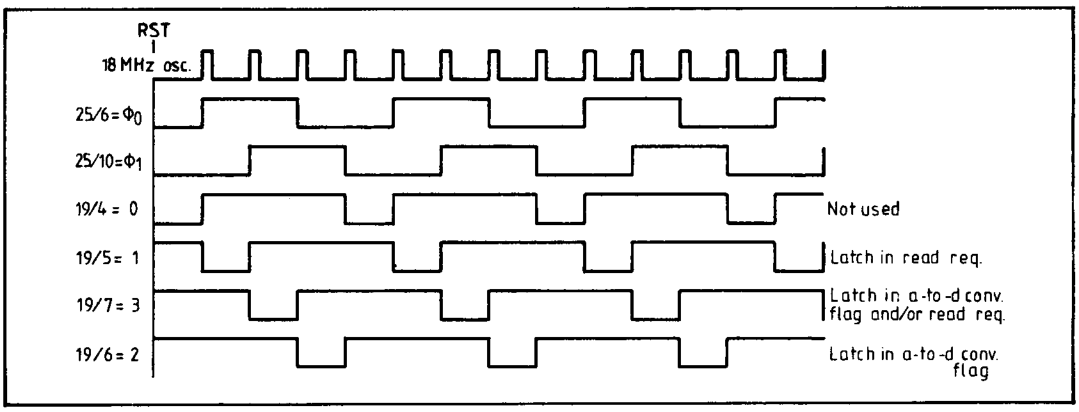


Fig. 4. Decoder output sequence is 0-1-3-2-0 to avoid switching spikes.

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ASZ16	2.00
ASZ17	1.60
ASZ20	4.50
ASZ21	4.75
AUY10	3.50
BA145	0.13
BA148	0.15
BA154	0.06
BA155	0.11
BA156	0.06
BAW62	0.05
BAX13	0.05
BAX16	0.06
BC107	0.12
BC108	0.13
BC109	0.14
BC113	0.12
BC114	0.12
BC115	0.12
BC116	0.19
BC117	0.24
BC118	0.30
BC125	0.25
BC126	0.25
BC135	0.18
BC136	0.18
BC137	0.22
BC147	0.12
BC148	0.12
BC149	0.12
BC157	0.12
BC158	0.13
BC159	0.12
BC167	0.10
BC170	0.09
BC171	0.11
BC172	0.09
BC173	0.09

BC177	0.15
BC178	0.28
BC179	0.15
BC182	0.11
BC183	0.09
BC184	0.11
BC212	0.11
BC213	0.11
BC214	0.11
BC237	0.09
BC238	0.09
BC301	0.36
BC303	0.36
BC307	0.09
BC308	0.09
BC327	0.09
BC328	0.09
BC337	0.09
BC338	0.09
BCY30	3.75
BCY31	3.75
BCY32	3.75
BCY33	2.50
BCY34	2.50
BCY39	3.60
BCY40	3.00
BCY42	0.32
BCY43	0.45
BCY58	0.25
BCY70	0.21
BCY71	0.21
BCY72	0.21
BCZ1	3.50
BD115	0.35
BD123	2.30
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BD135	0.27
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BD138	0.30
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BD183	0.75
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BD238	0.35
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BDY10	2.40
BDY20	1.50
BDY60	1.50
BF115	0.30
BF152	0.16
BF153	0.19
BF154	0.17
BF159	0.20
BF160	0.20
BF166	0.35
BF167	0.30
BF173	0.45
BF177	0.30
BF178	0.30
BF179	0.30
BF180	0.30
BF181	0.25
BF182	0.30
BF183	0.30
BF184	0.30
BF185	0.30
BF194	0.15
BF195	0.15
BF196	0.15
BF197	0.15
BF200	0.33
BF224	0.12
BF241	0.12
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BF259	0.30
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BFW10	1.04
BFW11	1.01
BFX84	0.28
BFX85	0.28
BFX87	0.28
BFX88	0.28
BFY50	0.28
BFY51	0.28
BFY52	0.28
BFY64	0.36
BFY90	0.65
BSX19	0.27
BSX20	0.27
BSX21	0.27
BT106	1.65
BTY79 400K	3.00
BU205	1.20
BU206	1.20
BU208	2.00
BY100	0.42
BY126	0.15
BY127	0.15
BZX61	0.17
Series BZY88	0.10
Series BZY91	8.00
Series BZY93	0.12
Series BZY95	1.64
Series BZY96	2.00

Series CRS1 40	0.60
CRS3 40	0.75
CRS3 60	0.90
GEX66	3.00
GEX541	6.50
GJ3M	3.00
GM0378A	1.75
KS100A	0.45
MJE340	0.79
MJE370	0.73
MJE371	1.05
MJE520	0.75
MJE521	0.73
MJE2955	2.25
MJE3055	2.00
MPF102	0.55
MPF103	0.55
MPF104	0.55
MPF105	0.55
MPSA06	0.17
MPSA56	0.17
MPSU01	1.11
MPSU06	1.33
MPSU56	1.71
NE555	0.45
NKT401	4.00
NKT403	3.50
NKT404	4.00
OA5	1.75
OA7	0.75
OA10	0.55
OA47	0.15
OA70	0.22
OA79	0.21
OA81	0.21
OA85	0.21
OA90	0.08
OA91	0.08
OA95	0.08
OA200	0.15
OA202	0.15

OA211	1.00
OAZ200	1.50
OAZ201	1.50
OAZ206	1.50
OAZ207	1.50
OC16	5.00
OC20	6.00
OC22	4.50
OC23	10.00
OC24	3.00
OC25	1.75
OC26	1.50
OC28	5.50
OC29	4.40
OC35	4.00
OC36	4.00
OC41	1.20
OC42	1.50
OC43	1.50
OC44	1.25
OC45	0.85
OC71	0.65
OC72	2.20
OC73	1.45
OC74	1.40
OC75	1.40
OC76	1.60
OC77	2.75
OC81	0.90
OC81Z	1.20
OC82	0.95
OC83	1.40
OC84	1.40
OC122	6.50
OC123	6.50
OC139	12.00
OC140	18.00
OC141	18.00
OC170	4.40
OC171	4.40
OC200	4.00
OC201	5.50

OC202	5.50
OC203	5.50
OC204	7.00
OC205	10.00
OC206	8.50
OC207	18.00
OCP71	2.50
ORP12	2.40
R2008B	1.95
R2009	2.25
R2010B	2.00
TIC44	0.48
TIC226D	1.20
TIL209	0.29
TIP29A	0.35
TIP30A	0.36
TIP31A	0.25
TIP32A	0.25
TIP33A	0.53
TIP34A	0.60
TIP41A	0.38
TIP42A	0.42
TIP110	0.40
TIP117	0.45
TIP125	0.35
TIP130	0.45
TIP131	0.45
TIP132	0.48
TIP135	0.45
TIP137	0.48
TIP140	0.85
TIP141	0.85
TIP142	0.85
TIP2955	0.60
TIP2955T	0.45
TIP3055	0.60
TIP3055T	0.45
ZS140	0.25
ZS170	0.21
ZS178	0.54
ZS272	0.23
ZS278	0.57

ZTX107	0.12
ZTX108	0.12
ZTX109	0.12
ZTX300	0.13
ZTX301	0.14
ZTX302	0.14
ZTX303	0.14
ZTX304	0.14
ZTX311	0.13
ZTX314	0.25
ZTX500	0.14
ZTX501	0.14
ZTX502	0.14
ZTX503	0.14
ZTX504	0.20
ZTX531	0.20
ZTX550	0.25
1N914	0.03
1N916	0.03
1N4001	0.04
1N4002	0.04
1N4003	0.04
1N4004	0.04
1N4005	0.04
1N4006	0.04
1N4007	0.05
1N4009	0.06
1N4148	0.03
1N5400	0.10
1N5401	0.11
1S44	0.04
1S920	0.10
1S921	0.12
2G301	1.00
2G302	1.20
2G306	1.50
2N404	1.50
2N696	0.30
2N697	0.36
2N698	0.38
2N705	2.50
2N706	0.20

2N708	0.22
2N930	0.25
2N1131	0.35
2N1132	0.35
2N1302	1.80
2N1303	0.90
2N1304	3.00
2N1305	1.00
2N1306	3.00
2N1307	1.20
2N1308	4.00
2N1309	1.50
2N1613	0.30
2N1671	5.00
2N1893	0.30
2N2147	8.00
2N2148	2.75
2N2218	0.32
2N2219	0.32
2N2220	0.22
2N2221	0.22
2N2222	0.20
2N2223	7.50
2N2368	0.23
2N2369A	0.23
2N2484	0.24
2N2646	0.75
2N2904	0.30
2N2904A	0.30
2N2905	0.30
2N2906	0.22
2N2907	0.22
2N2924	0.12
2N2925	0.12
2N2926	0.12
2N3053	0.30
2N3054	0.55
2N3055	0.70
2N3440	0.60
2N3441	0.75
2N3442	1.00
2N3614	5.00

2N3702	0.11
2N3703	0.11
2N3704	0.11
2N3705	0.11
2N3706	0.11
2N3707	0.11
2N3708	0.11
2N3709	0.11
2N3710	0.11
2N3711	0.10
2N3771	1.20
2N3772	1.20
2N3773	1.60
2N3819	0.50
2N3820	0.60
2N3823	0.80
2N3866	1.00
2N3904	0.10
2N3905	0.10
2N3906	0.10
2N4058	0.12
2N4059	0.20
2N4060	0.12
2N4061	0.12
2N4062	0.15
2N4124	0.13
2N4126	0.13
2N4248	0.25
2N4288	0.15
2N4289	0.12
2N4400	0.12
2N4401	0.12
2N4402	0.12
2N5457	0.45
2N5458	0.40
2N5459	0.40
2S017	16.00
2S019	25.00
2S024	35.00
2S025	35.00
2S026	40.00
2S103	2.50
2S302	5.50
2S303	5.50
2S322	5.00
2S324	4.00
2S701	12.50
2S745A	1.75
2S746A	1.75

VALVES

A1834	9.00
A2087	13.50
A2134	17.50
A2293	16.00
A2426	35.00
A2521	25.00
A2900	15.00
A3343	45.00
AZ31	2.75
AZ41	2.60
BK448	114.90
BK484	155.35
BS90	58.00
BS810	60.00
BT5	58.95
BT17	185.00
BT19	44.05
BT29	349.15
BT69	354.80
BT95	129.90
CBL31	4.00
CL33	4.00
CY31	3.00
C1K	20.00
C3A	22.00
C3JA	22.00
DA41	25.00
DA42	18.70
DAF91	1.75
DAF96	1.75
DET22	35.00
DET	49.00
DF91	1.75
DF96	1.75
DK91	1.75
DK92	2.00
DK96	1.75
DL92	2.00
DL94	1.75
DL96	1.75
DLS10	14.00
DLS15	12.50
DLS16	12.50
DLS19	12.50
DM70	2.00
DM71	2.00
DM160	4.75
DY87	1.50
DY802	1.50
E55L	50.00
E80CC	15.00
E80CF	11.27
E80F	14.19
E80L	13.73
E81CC	8.00
E81L	13.27
E82CC	8.10
E83CC	8.40
E86C	8.25
E88C	8.25
E88CC	10.33
E90CC	9.47
E90F	9.90
E91H	6.25
E92CC	8.75
E99F	9.10
E130L	18.50

E180CC	10.50
E180F	12.05
E182CC	13.25
E186F	11.50
E188CC	8.91
E280F	22.51
E283CC	12.00
E288CC	17.50
E810F	35.48
EA52	32.25
EA76	2.50
EA8C80	1.25
EAC91	3.50
EAF42	2.50
EAF801	2.00
EB41	4.00
EB91	1.50
EBC33	2.50
EBC41	2.50
EBC81	1.50
EBC90	1.25
EBF	1.50
EBF83	1.75
EBF89	1.50
EBL31	10.00
EC90	1.25
EC91	8.00
EC92	1.75
EC157	440.00
ECC33	4.50
ECC35	4.50
ECC40	5.50
ECC81	1.75
ECC82	1.75
ECC83	1.75
ECC84	1.75
ECC85	1.75
ECC86	2.50
ECC88	3.50
ECC89	2.00
ECC91	8.93
ECC189	2.10
ECC807	1.75
ECC808	3.00
ECF80	1.50
ECF82	1.50
ECF86	2.50
ECH35	3.00
ECH42	3.50
ECH81	3.00
ECH83	2.50
ECH84	2.50
ECL80	1.50
ECL81	1.75
ECL82	1.50
ECL83	3.00
ECL84	1.50
ECL85	1.50
ECL86	1.75
EF37	5.00
EF39	2.75
EF40	5.00
EF41	3.50
EF42	4.50
EF50	2.50
EF54	5.00
EF55	3.50
EF80	1.75
EF83	4.00
EF85	1.70

EF86	3.50
EF89	2.50
EF91	2.95
EF92	6.37
EF93	1.50
EF94	2.50
EF95	5.99
EF98	2.00
EF183	2.00
EF184	2.00
EF804S	12.00
EF805S	15.00
EH90	1.75
EK90	1.50
EL32	2.50
EL33	4.00
EL34MU1	4.00
EL36	2.50
EL41	2.80
EL42	2.50
EL81	5.25
EL83	6.00
EL84	2.25
EL86	2.75
EL90	3.25
EL91	7.39
EL95	2.00
EL156	30.00
EL360	8.50
EL500	3.00
EL509	10.00
EL821	13.00
EL822	13.97
ELL80	19.00
EM34	8.00
EM80	2.50
EM81	2.50
EM84	2.00
EM85	2.75
EM87	2.50
EN32	25.00
EN91	6.50
EN92	6.96
EY51	2.75
EY81	2.50
EY83	2.50
EY84	9.24
EY86	1.75
EY88	1.75
EY500A	3.00
EY802	1.75
EZ35	1.75
EZ40	2.50
EZ41	2.50
EZ80	1.50
EZ81	1.50
EZ90	3.00
FW4-500	3.50
FW4-800	3.50
G1.371K	35.00
G551K	12.00
G180.2M	17.50
G240.2D	12.00
G400.1K	17.50
GN4	9.00
GN4A	9.00
GN4A	9.00
GS16	16.00
GT1C	25.00
GU50	20.00
GU51	20.00

GXU1	15.35
GXU2	3.50
GXu3	25.40
GXU4	44.50
GXU50	20.00
GY501	3.00
GZ32	4.00
GZ33	4.75
GZ34	4.00
GZ37	4.75
KT61	5.00
KT66	15.00
KT77 Gold Lion	12.00
KT88 Gold Lion	20.00
KTW61	2.50
KTW62	2.50
KTW63	2.50
M8079	12.34
M8080	8.25
M8081	9.82
M8082	9.69
M8083	10.25
M8091	10.43
M8096	6.80
M8097	8.10
M8098	8.15
M8099	8.00
M8100	10.30
M8136	11.75
M8137	12.25
M8140	6.00
M8141	6.50
M8142	8.75
M9144	7.50
M8149	6.50
M8161	9.35
M8162	11.75
M8163	8.25
M8190	5.00
M8195	10.85
M8196	7.50
M8204	7.05
M8212	11.37
M8223	6.00
M8224	6.30
M8225	4.50
M8248	14.03
MD2901	115.00
MU14	2.50
MX119	55.00
MX123	76.00
MX145	56.70
MX151	17.25
MX152	131.25
MX161	152.25
MX163	20.25
MX164	25.52
MX166	147.00
MX168	50.00
N78	15.00
OA2	3.25
OA3	2.50
OA4	6.00
OB2	4.35
OB3	2.50
OC2	4.35
OC3	2.50

OD3	2.50
OZ4	3.50
PC86	2.50
PC88	2.50
PC95	1.75
PC97	1.75
PC900	1.75
PCC84	1.50
PCC85	1.50
PCC88	2.00
PCC89	1.75
PCC189	2.50
PCC805	1.60
PCC806	1.60
PCE82	2.00
PCF80	2.00
PCF82	1.50
PCF86	2.50
PCF87	2.00
PCF200	3.25
PCF201	3.25
PCF801	2.50
PCF802	2.50
PCF805	1.70
PCF806	1.70
PCF808	1.70
PCL82	2.00
PCL83	3.00
PCL84	2.00
PCL85	2.50
PCL86	2.50
PCL805/85	2.50
PD500	6.00
PE06-40N	45.00
PFL200	2.50
PL36	2.50
PL81	1.75
PL81A	2.00
PL82	1.50
PL83	2.50
PL84	2.00
PL504 5	2.50
PL508	5.50
PL509	6.00
PL519	6.00
PL801	1.50
PL802	6.00
PY33	2.50
PY81	1.50
PY82	1.50
PY83	1.25
PY88	2.00
PY500A	4.00
PY800	1.50
PY801	1.50
QF451	82.50
QQV02-6	34.00
QQV03-10	25.00
QQV03-20A	48.38
QQV06-40A	46.00
QQV07-50	
69, 74 QQZ20	
6-4QA	62.20
QU37	12.50
QV03-12	6.80
QV04-7	3.50
QV08-100	188.00

QY3-65	63.24
QY3-125	72.00
QY4-250	74.00
QY4-400	80.00
QY5-500	199.00
QY5-3000A	472.00
QZ06-20	32.70
R10	6.00
R17	3.00
R18	3.00
R19	9.24
R20	2.50
RG3-250	32.68
RG3-250A	32.68
RG3-1250	59.00
RG4-1250	61.60
RG4-3000	99.45
RR3-250	40.00
RR3-1250	45.75
SHE12	65.00
S130	6.00
S130P	6.00
STV280-40	14.00
STV280-80	21.00
SU41	5.00
SU42	10.00
TD03-10	35.00
TD03-10F	35.00
T15	50.00
TT21	37.50
TT22	37.50
TT100	60.00
TY2-125	75.00
TY4-400	84.00
TY4-500	110.00
TY5-500	225.00
TY6-800	220.00
TY6-500A	515.00
TY6-5000B	395.00
TY6-5000W	446.00
TY7-6000A	552.00
TY7-6000W	552.00
TZ40	25.00
U18.20	3.50
U19	13.75
U25	2.50
U26	2.50
U37	12.00
UABC80	1.25
UAF42	2.50
UB41	3.00
UBC41	2.25
UBF89	1.50
UCC84	1.75
UCC85	1.85
UFC80	2.00
UCH42	2.50
UCH81	2.50
UCL82	1.75
UCL83	2.75

UF41	2.00
UF42	2.10
UF80	1.75
UF85	1.75
UF89	2.00
UL41	5.00
UL84	1.75
UM80	2.00
UY41	2.25
UY81	2.25
VLS631	15.00
XG1-2500	55.00
XG2-6400	141.90
XG5-500	30.00
XG2-6400	185.00
XR1-1600A	53.75
XR1-3200	110.00
XR1-3200A	
XR1-6400	150.00
YD1120	395.00
YD1240	490.00
Z803U	25.00
Z259	25.00
ZM1001	8.00
ZM1020	9.00
ZM1021	9.00
ZM1022	9.00
ZM1023	9.00
ZM1040	19.36
ZM1041	16.66
ZM1042	17.77
1B3GT	3.00
1B24	25.00
1B35A	48.00
1B63	64.00
1R5	1.75
1S5	1.75
1T4	1.75
2AS15	11.50
2C39A	60.00
2C43	70.00
2D21	3.25
2E26	8.25
2J42	98.00
2J55	245.00
2J70A	383.00
2J70B	336.00
2K25	125.00
3400Z	115.00
3500Z	100.00
3A5	3.00
3B24	11.00
3B28	15.35
3B29	20.05
3B240M	17.50
3B241M	17.50
3C23	25.00
3C24	24.50
3CX100A	47.00
3E29	45.00
3S4	2.00
3V4	1.75
4-65A	60.00
4-125A	60.00

4-250A	80.00
4-400A	87.00
4B32	20.00
4C35	120.00
4CX250B	58.00
4CX350A	105.00
4X150A	60.00
4X150D	56.00
5B254M	35.00
5B255M	35.00
5C22	160.00
5J180E	1650.00
5R4GY	5.50
5U4G	3.00
5U4GB	2.50
5V4G	2.50
5Y3GT	2.50
5Z3	4.00
5Z4G	2.50
5Z4GT	2.50
6-30L2	1.75
6AB4	1.75
6AB7	3.00
6AC7	3.00
6AF4A	4.25
6AG7	3.00
6AH6	5.00
6AK5	5.99
6AK6	2.50
6AL5	1.50
6AM4	4.00
6AM5	9.69
6AM6	6.02
6ANS	4.75
6AN8A	3.50
6AQ5	3.25
6AS6	8.66
6AS7G	8.75
6AT6	1.25
6AU5GT	5.00
6AU6	2.50
6AV5GA	4.50
6AV6	1.50
6AX5GT	3.00
6B7	3.25
6B8	3.25
6BA6	1.50
6BA7	5.00
6BA8A	4.00
6BC4	4.00
6BE6	1.50
6BH6	2.50
6BJ6	2.25
6BK4	4.50
6BL6	85.00
6BL7GT	4.50
6BM6	115.00
6BN6	2.00
6BQ7A	3.50
6BR7	6.00
6BR8A	3.50
6BS7	6.00
6BW6	6.00
6BW7	1.50
6BX7GT	5.00
6BZ6	2.75
6C4	1.25
6CB6A	2.54
6CD6GA	5.00

6CG7	2.50
6CH6	13.00
6CL6	3.75
6CW4	8.00
6D2	1.50
6DK6	3.00
6DQ6B	4.75
6EA8	3.00
6EB8	2.50
6EW6	2.25
6F6	3.00
6F23	1.60
6F28	1.60
6F33	33.50
6H1	14.00
6H2N	2.75
6H3N	2.75
6H6	3.00
6J4	5.50
6J6	8.93
6J7	4.75
6JE6	7.50
6K4N	2.50
6K6GT	2.75
6K7	3.00
6K8	3.00
6KD6	7.00
6L6G	3.00
616GA	3.50
6L6GC	5.75
6L6GT	3.00
6L7	2.50
6N2P	2.50
6N3P	2.50
	2.50
6N7	3.00
6P225	4.00
6Q7	3.75
6K7	3.25
6RHH8 6KN8	10.00
6SA7	3.00
6SC7	2.75
6SF7	2.50
6SH7	3.00
6SJ7	3.25
6SK7	3.50
6SK7GT	3.00
6SN7GT	3.00
6SQ7	3.40
6SR7	4.00
6SS7	2.75
6U5G	3.50
6U8A	2.25
6V6GT	4.25
6X4	3.00
6X5GT	1.75
7B7	2.50
7C3	4.00
7C6	2.50
7H7	4.00
7R7	4.25
7S7	3.50
7Y4	2.25
7Z4	2.00
HE3	55.00
12AH8	5.00
12AT6	1.50
12AT7	1.75
12AU6	2.50

12AU7	1.75
12AV6	2.50
12AW7	3.50
12AX7	1.75
12AY7A	4.00
12B4A	3.50
12BA6	2.50
12BE6	2.50
12BH7	2.75
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7409	0.36
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7412	0.42
7413	0.36

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7417	0.48
7420	0.48
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7423	0.36
7425	0.36
7427	0.36
7428	0.36
7430	0.36
7432	0.36
7433	0.55
7437	0.36
7438	0.36
7439	0.36

7440	0.36
7441	0.48
7442	1.25
7450	0.30
7451	0.30
7453	0.30
7454	0.30
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7474	0.36
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7476	0.48
7480	0.32

7483	0.48
7484	0.72
7486	0.54
7490	0.72
7491	0.36
7492	0.54
7493	0.54
7494	0.78
7495	0.65
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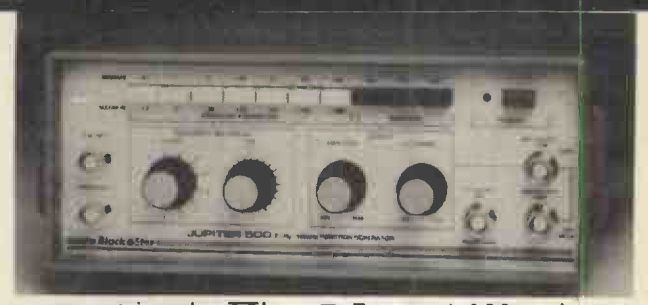

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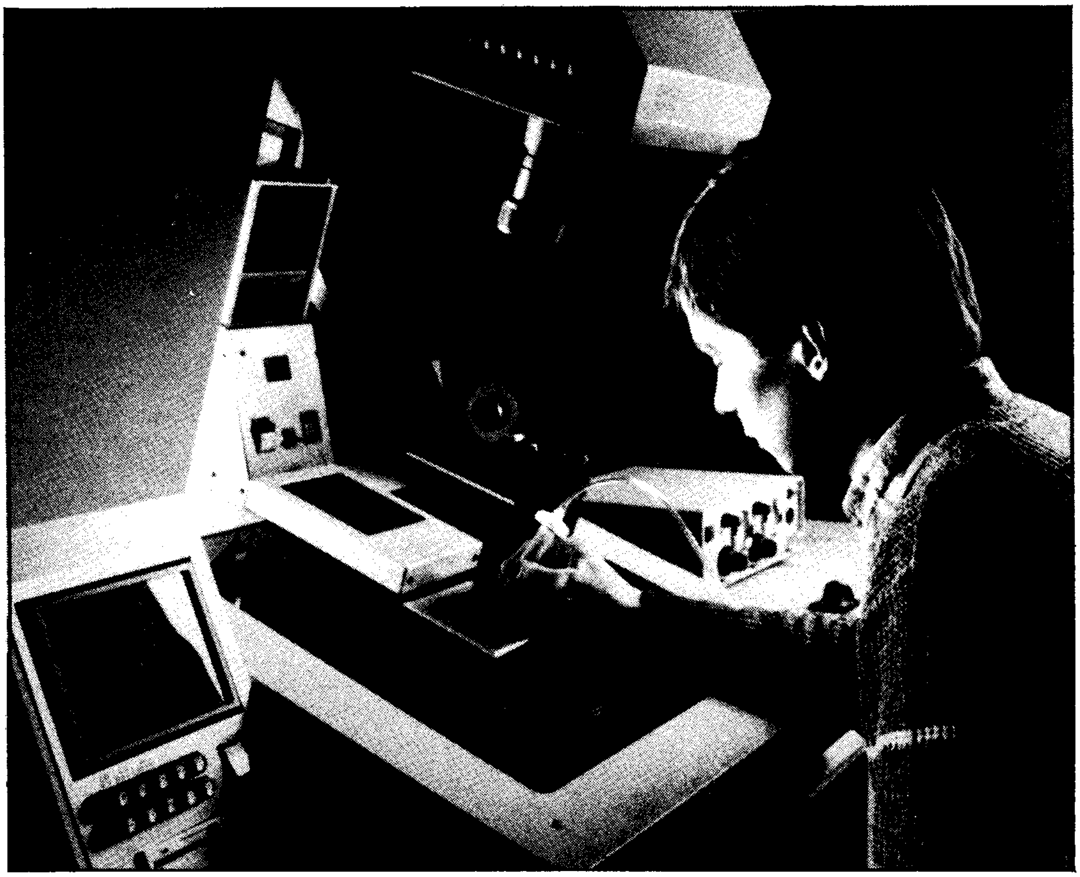
to all the other design levels. This controls all the versions of a chip and is part of the core database management. Each member of the consortium has a degree of freedom so that there is some overlap in design tools. This is beneficial for the user as it can cater for different approaches to the design process. The system can be selected from a wide range of program modules.

It is possible to design a circuit from the inside-out (from the specific detail to the whole device) or from the outside-in (from the device to the detail). It allows the user to build a library of sub-assemblies (macro-cells). Specific portions of the circuit may be positioned manually or automatically with automatic routing of the connections between them. A module generator can define quite a complex structure by just defining some parameters. Combined, the floor planner, placers, routers, component and macro library and the module generator form a powerful system that can provide a fast design time.

The flexibility of the system is based on the completely hierarchical progam and systems architecture. It is fully portable between process technologies and layout styles and also between design environments. The system also generates project information and documentation.

The system is still being developed further and will include micron and sub-micron architecture, and the development of special-purpose tools, e.g. for the design of parallel processors. Existing c.a.d. standards are adhered to, where they exist, in c.a.d. tools and in data exchange.

Spirit has been developed under Unix and will run on any computer that has Unix compatible with the AT&T system V, has a minimum of 2MB of main memory and 55 to 80MB of external store with an 8-bit plane colour graphics device. The software currently runs on HP-9000/500 and 320, VAX, Sel, Gould, Geminix, Masscomp and PCS computers. It is to be distributed by hardware suppliers but details can be obtained directly from ICD, PO Box 3132, 7500 DC Enschede, The Netherlands.
EWW 215



Semi-automatic pick-and-place for surface mounting

Printed circuits using surface-mounted devices can be assembled using the component placing workstation from Blakell-Parfitt. It uses a light projector to indicate the spot on the board where the next component is to be placed and has an automatic component dispenser to present that component.

The p.c.b. is mounted on an x-y table so that the component mounting position always falls in the same place. Substrates up to 250mm square can be handled by the machine in its standard form. Optional modifications accommodate larger boards.

The delivery system consists of a vertical magazine with a conveyor system to present the selected component close to the operators hand. This magazine can handle up to 270 different loose components, allowing it to be used with very complex p.c.bs. Passive components on tape reels can also be coped with. Components can be picked up and mounted using a vacuum pen or tweezers. The system can be configured to suit both right and left-handed operators. A s.m.c. station can be combined with an assembly station for conventional through-mounted components as there are p.c.bs manufactured which use both types.

The control for the optical guidance beam is programmable to give component size, shape, position and polarity. A separate information screen displays the component type and value. Programming is performed off-line on a separate programming station, though a future option will be to program the system through the station's own computer. Programming consists of building a file of x-y coordinates complete with the component's position and polarity and matching this with the component's number. The c.r.t. display can be programmed to display comments and special instructions as well as the component details. Programs are stored and loaded through a disc drive, while the component dispensers are loaded with the appropriate components. The program is stepped through by operating a foot switch or push button.

Blackell-Parfitt Systems Ltd, Blandford Heights, Blandford Forum, Dorset DT11 7TE.
EWW 220

What is a silicon compiler?

Perhaps the answer to the question is best provided by a specific example. The Spirit integrated circuit designer which is produced in Holland by ICD, but is the result of multi-national European consortium, the British contribution being provided by BT Research Laboratories, Martlesham.

Spirit is a design environment which enables the production of a hierarchical design database. Every level in the hierarcy can be available to the user at the touch of a finger on the keyboard.

The system covers the four aspects of i.c. design: function, structure, geometry and testability.

The floorplanner which defines the area and main sections of an i.c. is the gateway

Forth on a chip

Amidst all this talk of computer-aided design it may be interesting to meet an actual product; a chip using such state-of-the-art technology. An example is the Novis NC4000, a processor that uses high-level language Forth as its operating code.

In most processors, machine-code instructions are decoded which subsequently invoke internal microcode instructions. These actually control the silicon components. In the NC4000 however, bit patterns within each opcode control directly the processor's components. As a result, each instruction is executed in a single clock cycle. The elimination of machine-code instructions and internal microcodes leads to a very high speed. Forth works as a series of nested subroutines and the NC4000 can call a subroutine in each clock cycle, and through parallel processing, requires no clock time to return.

The chip is a 4000-gate c-mos array which can execute between four and 40 million Forth operations per second (mifops!). In a typical application, 12 mifops is the norm. To give this some perspective, it has a seventeenth of the gate-count of a 68000 processor but eleven times the processing power. It can run Forth code 20 times as fast. Because of its concurrent operation, the device has simultaneous access to the return stack, data stack, main memory, and i/o bus.

The NC4000 is a 16-bit processor. It executes most Forth instructions in a single cycle, 125ns. For nested Forth words it only takes one cycle to go to the subroutine and zero time to return. By comparison 'Call' and 'Return' take 27 cycles on a 80186. Mathematical functions (multiply, divide, square root) take one cycle/step.

The combined input/output ports are 21 bits wide. It supports a 16k-word memory, or 4Mbytes using the address extension port.

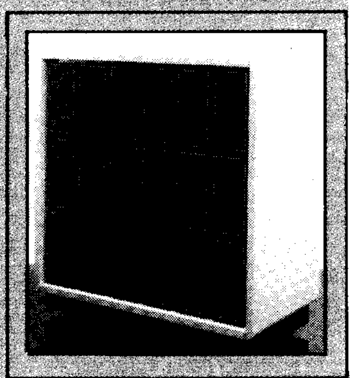
The development system for the NC4000 is called the Beta board. It is almost all c-mos, drawing only 600mA. On the board are: the Novix c.p.u; 56KB of static ram; 8K of stack memory; an 8K rom containing PolyForth, the programming language which runs the system; two serial ports; two expansion sockets giving access to all address, data and i/o lines. The Beta board can be linked through one of the serial ports to an IBM PC or an Apricot, which acts as a v.d.u. and a disc peripheral. All the software for the interactive development of the system is on the Beta board. The PC is used purely as a convenient disc sub-system.

At a recent demonstration of the system a small p.c.b. was prepared with analogue and digital interfaces. It was used to make a real-time digital audio pre-amplifier. The microphone input was processed and passed to an output amplifier. Simple Forth control words were used to alter the volume. The signals are also fed into a buffer and by adding data from earlier in the buffer it was possible to provide an echo. More complex control operations provided reverberation and pitch transformation. All in real time. In the most complex of the operations the 6MHz Novix took 38μs to perform 194 steps in the transformation and maintained a sampling rate of better than 20KHz.

The Beta board, complete with software on MS-DOS compatible discs, costs £3,800 which includes a licence to produce closed rom-driven systems. Novix NC4000 has been developed under the aegis of Forth Inc, the company formed by the inventors of Forth. It is available in the UK through Computer Solutions Ltd, 1 Cogmore Lane, Chertsey, Surrey KT16 9AP. **EWW 221**

High-level fault simulation

Zycad has developed a concurrent fault-simulation engine known as the Fault Evaluator which provides fault grading on v.l.s.i. circuits and system designs. It enables design engineers to develop chips and systems that are fully tested, as well as helping them to design more effective test programs. The system also permits full exercising of logic designs, revealing untestable or redundant portions of a circuit or system, at the design stage.



The Fault evaluator achieves its high performance by the use of a concurrent fault-simulation algorithm implemented in hardware. This allows fault simulation to be performed hundreds of times faster than is possible with conventional software-based fault simulators — typically in seconds rather than hours. Another benefit is that it allows the implementation of "design-for-test" facilities which can improve the reliability of the manufacturing process, increasing yields, and reducing returns and service calls.

The Evaluator has a capacity of up to 256 000 modelling elements, which cover the whole spectrum of circuit design requirements including rams, roms, programmable logic arrays; uni-directional, bidirectional or wired modelling elements; zero, connect and gate rise and fall delyas; flip-flops and latches; and defined combinational gates. The Fault Evaluator is comaptible with other Zycad products and supports the Zylos input language and output displays. It is available as a stand-alone fault-simulation engine or a field upgrade to the Zycad Logic Evaluator, providing logic simulation and fault simulation within the same unit. Zycad UK Ltd, PO Box 108, Woking, Surrey GU24 9SQ. **EWW 219**

Gate-array packaging

Gate-array single or multi-chip assemblies, ruggedized to military specification can be obtained from Teledyne through MeTL of Oxford. This forms part of Teledyne's logic and analogue array design and packaging service. The new facility can be applied to new projects and also to re-design of existing products.

Customers interested in the service can choose the level at which they wish to involve themselves in the project. Teledyne could complete an entire design project from a customer's circuit diagram and test pattern, or the client can direct the design process at any stage. The customer retains complete access to all software generated and to all steps in the development process. Final packaging can be provided in any form that may be desired. Teledyne specializes in the more complex multi-chip configurations where there is the most saving of space. Information from MeTL Ltd, Unit 2, Great Haseley Trading Estate, Great Haseley, Oxon OX9 7PF. **EWW 216**

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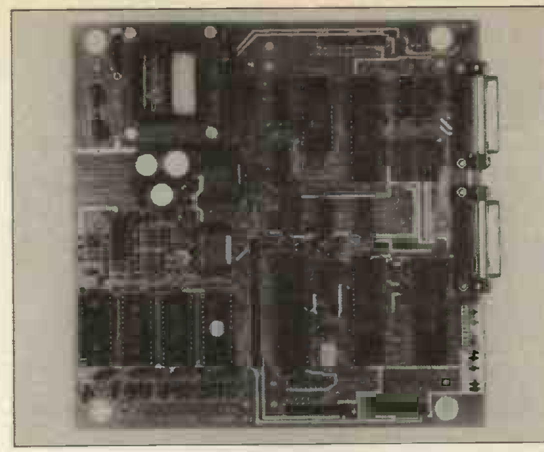

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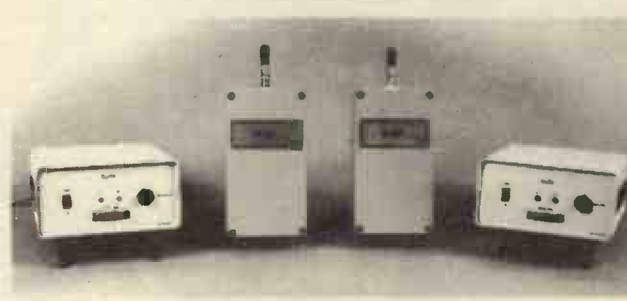

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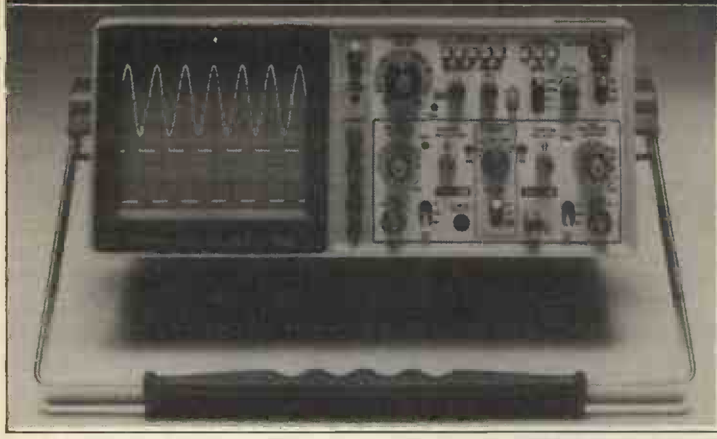

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V-422	40MHz Dual Trace	V-134	10MHz Tube Storage
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We hold the range in stock for immediate delivery.

For colour brochure giving specifications and prices ring **(0480) 63570**
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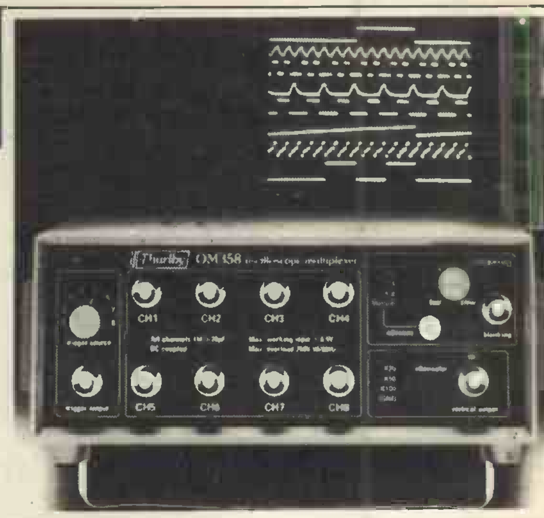
Add 8 channels to your 'scope

New Thurlby OM358 multiplexer £179+vat



The Thurlby OM358 gives any oscilloscope an 8 channel display. Observing many waveforms simultaneously can be essential when analysing sophisticated equipment. Application areas include microprocessor based products, data transmission systems, A to D converters, frequency synthesizers etc.
The OM358 is ideal for digital equipment (it can often solve problems that would otherwise need a fast logic analyser) but, unlike dedicated logic test instruments, it is equally suited to analogue waveforms.
The OM358 has a bandwidth of 35MHz and 3% calibration accuracy. Each input has an impedance of 1MΩ - 20pF and accepts signals up to ±6V. An 8 channel, 4 channel, or single channel display can be selected with triggering from any channel. *Colour data sheet with full specifications available.*

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- State and timing displays
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- 2K word acquisition memory
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*20	6.11	1.70
40	9.96	1.89
100	11.63	2.10
200	16.47	2.36
250	19.92	2.77
350	24.64	2.84
500	30.69	3.10
1000	55.65	4.70
1500	71.79	5.95
2000	86.38	6.35
3000	121.12	OA
6000	258.77	OA

*115 or 240V sec only.

400/440 to 200/240 CT
(60-1000VA Tap Secs)

VA	Price	P&P
60	9.98	1.90
100	11.88	2.10
200	16.47	2.36
250	19.92	2.52
350	24.64	2.84
500	30.69	3.10
1000	55.65	4.20
2000	86.38	5.50
3000	121.14	OA
6000	258.77	OA

24/12V or 12-0-12V
2×12V Secs. pri. 240V

12V		24V	Price	P&P
0.3A		15	2.53	90
1		05	3.45	1.30
2		1	4.46	1.36
4		2	5.15	1.70
6	A	3	8.07	1.76
8	M	4	9.43	1.82
10	P	5	10.31	2.05
12	S	6	11.43	2.15
16		8	13.62	2.33
20		10	18.33	2.66
30		15	22.79	2.85
60		30	46.67	4.50
83		41	53.76	5.50

96/48V. Pri 2×120V
Secs 2×36/48V
60, 72, 84, 96, 360-0-36
or 48-0-48V

72/96		36/48V	Price	P&P
1		2	9.38	1.52
2	A	4	15.42	2.31
3	M·	6	18.68	2.52
4	P	8	23.84	2.60
5	S	10	33.84	3.36
6		12	42.38	3.68
8		16	46.23	3.98

50/25V or 25-0-25V
2×25V Tap Secs Volts available 5, 7, 8, 10, 13, 15, 17, 20, 25, 30, 33,40.
20-0-20 or 25-0-25V

50V		25V	Price	P&P
0.5		1	4.34	1.47
1		2	5.28	1.50
2	A	4	9.12	1.94
3	M	6	10.97	1.96
4	P	8	14.80	2.22
6	S	12	18.91	2.30
8		16	26.75	2.86
10		20	31.74	2.20
12		24	37.99	3.36

60/30V or 30-0-30V
Pri 2×120V. 2×30V Tap Secs. Volts available 6, 8, 10, 12, 16, 18, 20, 24, 30, 36, 40, 48, 60, 24-0-24 or 30-0-30V.

60V		30V	Price	P&P
0.5		1	4.93	1.58
1		2	7.51	1.60
2		4	9.66	2.00
3	A	6	13.96	2.10
4	M	8	15.91	2.31
5	P	10	20.11	2.36
6	S	12	22.95	2.78
8		16	32.26	3.20
10		20	37.55	3.47
12		24	43.28	3.68

MINIATURES

Sec V	Amp	Price	P&P
3-0-3V	0.2	3.26	.96
6×2	1A×2	3.12	1.30
0-0-9	0.1	2.72	.96
9×2	0.33×2	2.63	.96
8-9×2	.5×2	3.63	1.30
8-8×2	1A×2	4.48	2.31
15×2	2×2	2.53	.96
12-0-12	.05	3.11	.96
20×2	15×2	3.55	1.30
15-27×2	.5	5.88	1.70
15-27×2	1A	7.66	.50
0-CT×15V	.5	2.66	.96
0-CT–15V	4A	2.28	1.08

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30V		15V	Price	P&P
0.5		1	3.35	1.36
1		2	4.54	1.48
2		4	7.34	1.69
3		6	8.50	1.45
4	A	8	10.15	1.99
5	M	10	12.55	2.10
6	P	12	14.20	2.30
8	S	16	19.00	2.36
10		20	21.92	2.46
12		24	24.36	2.63
15		30	27.96	3.20
20		40	37.42	5.14

AUTOS
105, 115, 220, 230, 240V
For step-up or down

VA	Price	P&P
80	5.08	1.49
150	7.36	1.69
250	8.96	1.76
500	13.96	2.34
1000	24.93	2.90
1500	29.58	3.35
2000	44.34	4.20
3000	75.22	5.10
5000	113.11	OA
7500	175.51	OA
10KVA	207.89	OA

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80	9.81	1.69
150	12.70	1.99
250	15.47	2.78
500	25.38	2.90
1000	35.43	3.97
2000	63.49	4.76
3000	91.14	OA

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14, 8, 0, 8, 14V SEC
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250W	£208.00
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Transformers T1, T2
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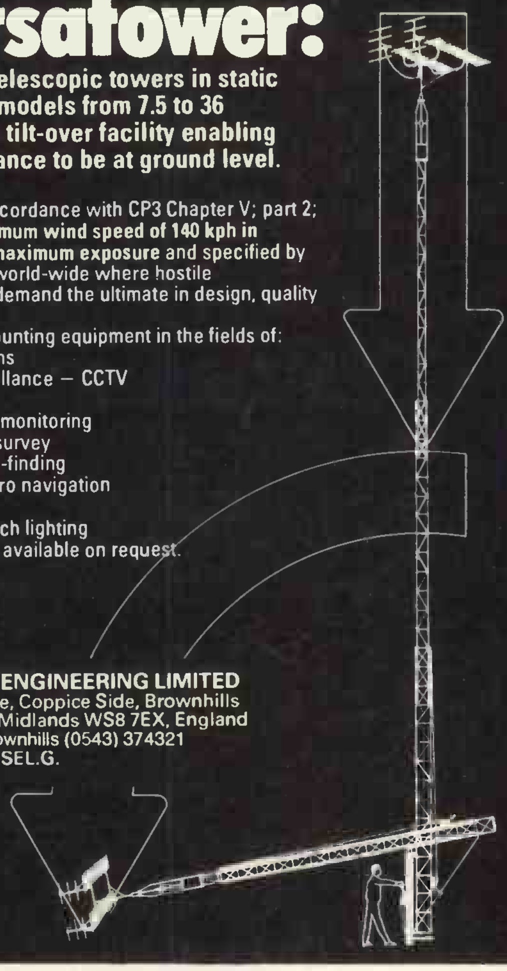

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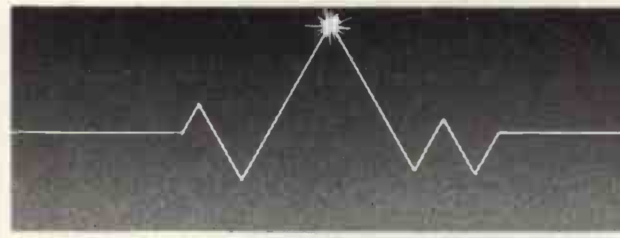
THE PEAK...



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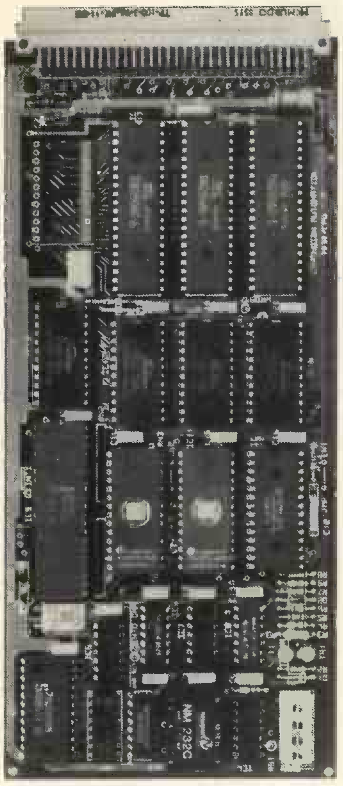

Based around the Intel 8051 family of advanced 8 bit microcontrollers the Cavendish Automation CPU comes complete with an effective implementation of Bryte-Forth.* The low cost of the CA7032 CPU enables it to be used for both development and/or target systems. Bryte-Forth is a subset of forth 79-standard and the implementation allows user ROM based applications to be created with ease. 5 interrupts, a 24 hour Real Time clock calendar and full serial communications are all supported on card.

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Comprehensive documentation is supplied with the CPU which requires only +5 volts and dumb terminal for operation.

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CPU Card Advantages:

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To find out more about the CA7000 series controllers contact:

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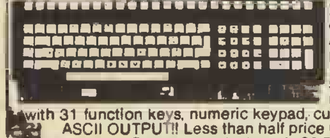

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(172)

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