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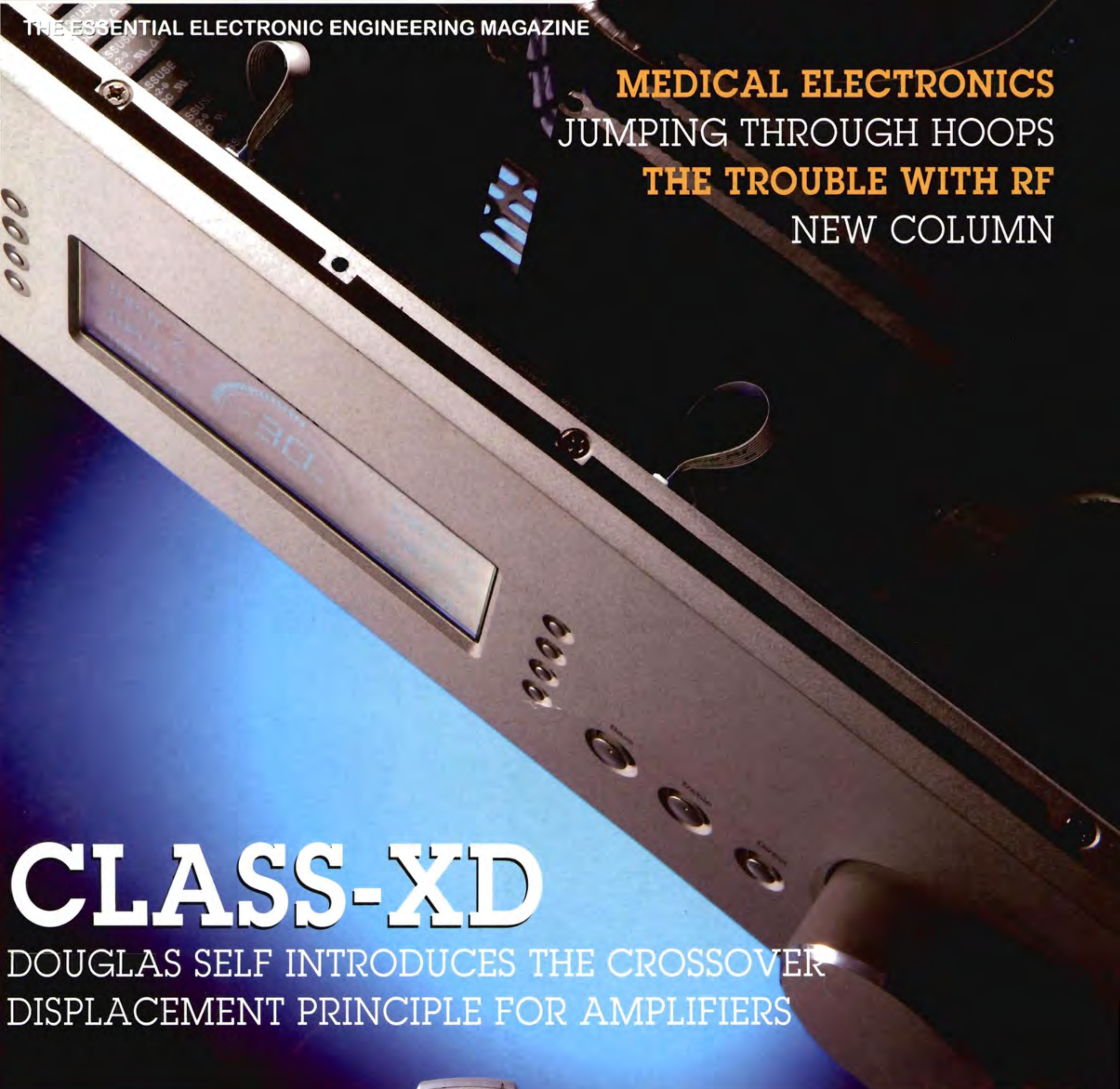

MEDICAL ELECTRONICS
JUMPING THROUGH HOOPS

THE TROUBLE WITH RF
NEW COLUMN

CLASS-XD

DOUGLAS SELF INTRODUCES THE CROSSOVER DISPLACEMENT PRINCIPLE FOR AMPLIFIERS

SPECIAL REPORT
PROCESSORS AND CONTROLLERS

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He who dares, wins

Two years have gone by and Electronica – the biggest bi-annual electronics components and systems event in the world – is on the cards again (Munich, Germany, 14 – 17 November 2006). The buzz preceding it is palpable, even in August. Companies have already announced their stands and are previewing their latest products.

If you try to get accommodation and flights to attend Electronica now, you've probably left it too late.

This year, however, Electronica will be even more special for *Electronics World* magazine than before. For the first time since its inception, *Electronics World* is going to have a stand at Electronica. We will be in the A5 hall, smack in the middle of semiconductor giants' stands, which include STMicroelectronics, Infineon Technologies, ON Semiconductor and International Rectifier. If you plan to come to Electronica, why not join us for a beer; come to share your views with us, or indeed your announcements, or even simply to just catch your breath.

It'll be interesting to see what Electronica brings this year. As usual, I am expecting the buzz, the adrenalin, the hype even. But, it will also be a good indication of how European and American electronics firms are doing. So far, we've seen that the business has been cautious – after all, "once bitten twice shy" when thinking about the last slump we had in the electronics industry. Who would want to go through that again?! So, companies have been very cautious with their investments, with their target areas of interest and their developments. According to Malcolm Penn of market research firm Future Horizons, semiconductor companies are in a very good position now and have been for over a year, but they simply do not acknowledge this state. And yet, now is the time to invest for reaping rewards later.

So, why not be daring? After all, as in the famous words of a UK TV character: "He who dares, wins."

Svetlana Josifovska
Editor

In June this year, we run a special new subscriber offer, where anybody who started a new subscription to Electronics World magazine before August 31st would be entered into a draw to win a Birdie Faultracker test system from Laplace Instruments.

The winner of that competition is P C Hettiaratchi, system engineer from Rajagiriya, Sri Lanka.

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Philips Semiconductors has split from Royal Philips of the Netherlands and in the process it changed its name to NXP (according to its CEO, Frans van Houten, the name is short for Next Experience). A consortium consisting of Kohlberg Kravis Roberts & Co (KKR), Bain Capital, Silver Lake Partners, Apax and AlpInvest Partners took an 80.1% stake in the semiconductor operation with Philips retaining a 19.9% interest.

The new company will focus on media technologies for the next generation of consumer entertainment products. In the process, the firm is trying to decide whether it should stay in the Crolles2 fab alliance with STMicroelectronics and Freescale Semiconductor.

* * *

The UK's first independent organisation dedicated to supporting the growth of high-tech companies through the provision of world-class R&D, coupled with business and academic support services, has opened in West Yorkshire.

The Advanced Digital Institute's primary role will be to act as an intermediate technology development centre of expertise helping companies identify and develop new high-value products and services. Working directly with industry and collaborating with the region's universities, it will aim to build specialist teams focusing on key industry sectors such as wireless communications, digital TV and consumer networking among others.

* * *

British businesses are considered to be some of the worst payers in Europe, suffering a poor reputation with customers both at home and abroad, according to research amongst 1,200 European firms carried out by global credit insurer, Atradius.

Atradius reveals that 42% of European companies believe that payment practices in the UK are "poor" or "average", the second lowest score of the 12 countries rated. Only Italy has a lower rating with 64% of European businesses saying the country was poor with payments.

In addition, 33% of European businesses say they experience payment delays from British customers "rather frequently". Again, only Italy scored a worse rating, with 45% of businesses saying they experience delays from Italians "very frequently".

ARM will be winner in the MCU space too, says start-up

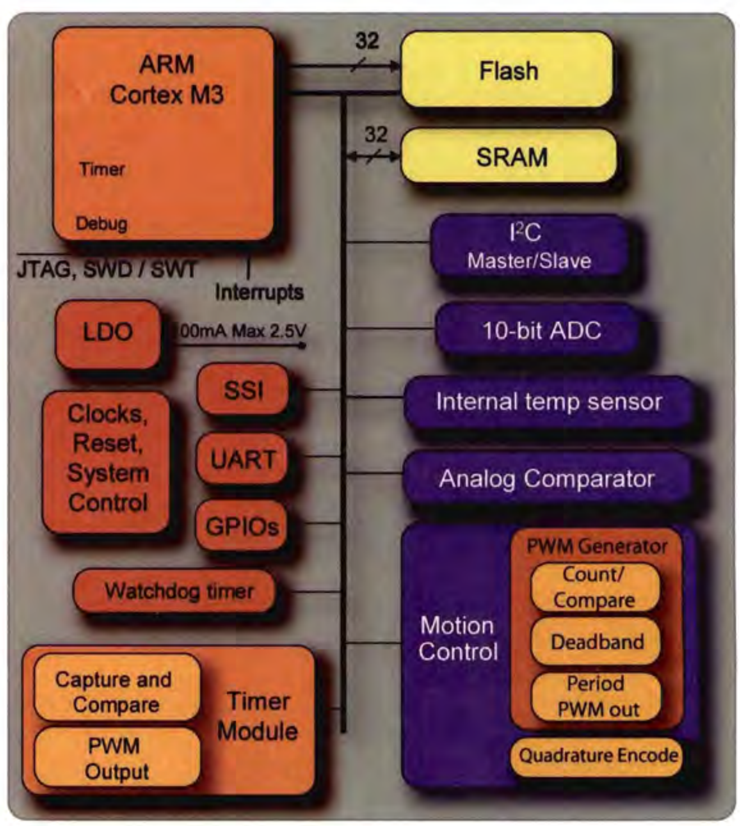
Jean-Anne Booth, founder and chief marketing officer (CMO) of fabless semiconductor start-up Luminary Micro says that the microcontroller (MCU) market is ripe for consolidation and that an ARM-based architecture will emerge as the winner in this space.

"The only market that has not consolidated yet is the microcontroller market. It is very fragmented and no architecture dominates it. Just like in the computing industry, where everything consolidated to the 8086 architecture, and in the embedded space everything consolidated to ARM, in microcontrollers the same will happen but with the 32-bit ARM based MCU," said Booth.

According to Booth, when this happens (some 18 to 24 months from now, this time being the typical length of a design cycle in the embedded space), Luminary Micro will reap the rewards. The company was founded two years ago to design and sell ARM Cortex-M3 based MCUs. Its Stellaris family of products currently comprises 19 devices with different memories and capacities, as well as peripherals and packages, but all of them offer 32-bit performance. The entry-level price is a very palatable $1 in volumes, equivalent to the price of an 8-bit microcontroller.

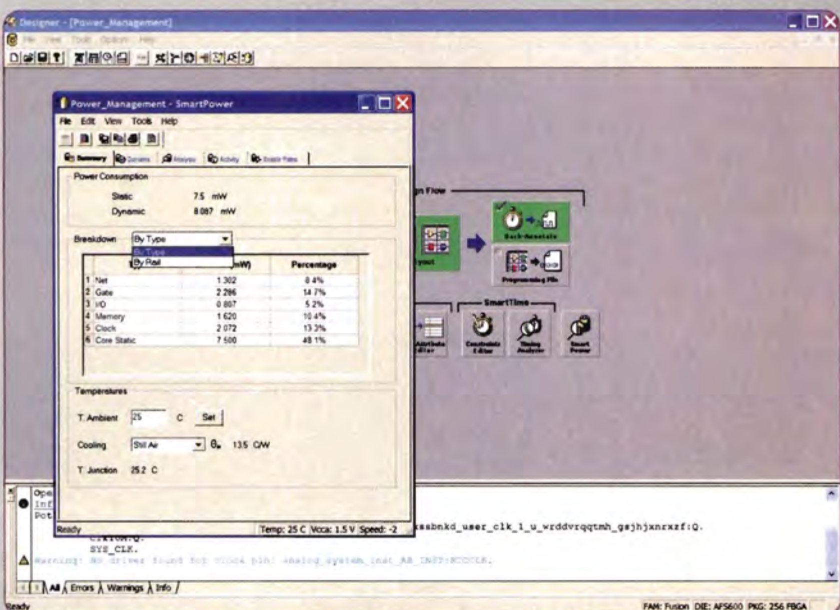
Luminary Micro is currently using distributors, such as Alpha Micro, to sell its devices and even design them in. "The 18- to 24-month design-in cycles in industrial embedded applications suits us fine as a start-up. But, once we grow up, I'm sure you'll see us in the automotive business as well, where the design cycles are 48 months and the whole business works slightly differently," said Booth.

Luminary Micro's devices are fabricated by TSMC in a 0.25µm CMOS process.



Luminary Micro's Stellaris family currently consists of 19 devices, all of them stem from the ARM Cortex-3 32-bit architecture

Aggressive power-cut by Igloo



Actel's Igloo allows for power estimate and tweaking by type

Last month, Actel introduced the lowest power FPGAs yet in its portfolio of flash-based devices. Actel's executives believe that the new Igloo family will take the portable systems design space by storm. The family's lowest static power is 5µW (compared to 19.8µW for a similar device from the nearest competitor), operational power is 1.2V (down from 1.8V currently used) and dynamic power is lower than that of the Actel's ProAsic3 family.

"Static power has become a big element of design. The static power of 5µW is more aggressive than that of CPLDs and even microcontrollers," said Dennis Kish, senior sales VP. "We've optimised all the current sources of the [Igloo] fabric and we've added FlashFreeze – a pin that allows for quick and easy low-power mode."

With FlashFreeze the device can be switched into low power mode within 1µs, without having to power off its voltage. In the process, core registers, SRAM and I/O still continue to keep their data and configuration. FlashFreeze uses weak pull-up resistors, with a light current available.

In addition, there's the SmartPower advanced power analysis package, part of the Libero IDE. This allows analysis of block power by type, instance or rail; it offers a design-level power summary, detailed hierarchical reports of dynamic power consumption and all types of readings linked to switching activities, ambient and junction temperature, and others.

The Igloo family is available with between 30k and three million system gates, up to 504kbit of dual-port SRAM, up to 616 user I/O and six PLLs. It will be available early next year at entry-level price of $1.50 in volumes of 250k.

Engineers at the University of Southampton have developed a method to make bipolar transistors twice as fast as current devices. Bipolar transistors are solid state semiconductor devices that are used in a variety of electronic systems.

According to Professor Peter Ashburn at the University's School of Electronics and Computer Science (ECS), who undertook this research in collaboration with STC Microelectronics, the researchers used a standard silicon bipolar technique with fluorine implants to deliver a record fT of 110GHz, which is twice as fast as the current record.

The fluorine implants are used to suppress boron diffusion in the base of the transistor, which means that the base width is narrower, allowing electrons to travel across it faster.

* * *

Cambridge Consultants has created a medical device for managing diabetes based on Near Field Communication (NFC). It links a glucometer and insulin pump wirelessly. The glucometer records the blood sugar reading and then recommends a dose of insulin. If the patient accepts the dose, then they simply swipe the glucometer against the insulin pump, which could be located beneath clothing, and the drug is delivered. NFC operates in the 13.56MHz frequency range, over a distance of typically a few centimeters, and combines the functions of a contactless reader, a contactless card and peer-to-peer functionality on a single chip.

The prototype device was developed in conjunction with Philips.

* * *

Team Simoco has launched TETRA-G technology, a fully TETRA-compliant, scalable architecture for IP-switched TETRA, with voice and data system integration and network management facilities built in.

The company claims that TETRA-G removes traditional scalability and cost barriers to TETRA deployment for customers deploying either single site or multisite digital radio systems. It features integrated connectivity with land-line telephony and IP network traffic, giving maximum operational flexibility.

University creates a bond between electronics and organic molecules

Molecular electronics came closer to realisation with a recent success from the academics at Liverpool University, who managed to link up an organic molecule with electronics. The scientists created a firm chemical bond between a single gold atom and a single organic molecule called pentacene, a compound of carbon and hydrogen, reported to have the highest field-effect mobility values for organic thin film field-effect transistors.

"Our experiment showed that it is possible to control the arrangement and shape of chemical bonds and gave us new insights into making contact with a single molecule," said Professor Mats Persson of the University's Department of Chemistry.

The experiment also highlighted a way of controlling extremely small electronic structures at the atomic scale by the way of chemical bonds between single molecules and atoms. "The atomic scale control of single molecule chemistry in this experiment opens up new perspectives in the emerging field of molecular electronics, particularly in connecting organic molecules with electronic components. This could be important in creating electronics for future computers which are faster, smaller and with lower power consumption," said Persson.

The research was conducted in collaboration with IBM Zurich Research Laboratory; Tampere University of Technology in Finland and Chalmers University of Technology in Sweden.

TOP 10 TIPS

DESIGNING RGB LED LIGHTING SYSTEMS

- **How do I calculate the right ratio of red, green and blue light to get the colour that I want?**
- **Do I need to calculate the RGB ratio for each colour that I want?**
- **An LED's wavelength and intensity varies from part-to-part. Do I need to calculate the RGB ratio for each system that I build?**
- **An LED's wavelength and intensity shifts over temperature, driving conditions and time. How do I deal with that?**
- **How do I manage or maintain the mixed colour as the RGB LEDs degrade and at different rate?**
- **How can I insure the mixed RGB light is best detected?**
- **Do I need to be involved and experienced in software development using the close loop system?**
- **What else is needed to implement a plug-and-play RGB close loop system into my application?**
- **Can I use any kind of red, green or blue LED or light source?**
- **How to calibrate different systems next to each other in order to run as one unit?**

This month's Top Ten Tips were supplied by Patrick Trueson, European Marketing Manager for Optoelectronic Products at Avago Technologies. To find out more log on to avagotech.com

If you want to send us your top five or ten tips on any engineering and design subject, please write to the Editor at EWeditor@nexusmedia.com.

Reality not a dream

Dr Peter Harrop, Chairman of market analyst firm IDTechEx, explains how printing electronics technology, typically portrayed as an academic dream, is already widely used and is rapidly becoming a very large business, one that will overtake the silicon industry

Silicon chips have had a massive impact on our lives since their invention almost sixty years ago. They are used in ever more applications and they'll still be around many years from now. However, there are applications where their cost, fragility and time-to-market mean they are not viable.

In addition, the silicon chip has limited relevance to electrics, which is beginning to merge with electronics. For example, although we have silicon photovoltaics, silicon chip technology is of little relevance to making batteries or laminar fuel cells. Silicon chips are not used for mainstream lighting or electronic displays, as opposed to driving circuits.

Not so with printed electronics and electrics, because, for example, there really is a prospect of printing moving colour billboards using Organic Light Emitting Diode (OLED) technology. Indeed, printed batteries, electronic displays, antennas, RF and electrostatic shielding and even sensors are a reality today.

RFID and other electronic circuits could be printed for diagnostic applications or information on every-day packaging to rival normal graphics. Wallpaper could be printed that will change colour and pattern, but also act as room lighting and a TV screen, powered by solar energy.

All of these applications are now becoming possible and many are already on the market. They will rarely replace the silicon chip, but they will certainly threaten it, especially as silicon R&D and production costs increase.

In general, printed electronics is leveraging silicon technology or creating new electronic markets at price points that are way below anything that silicon proponents can dream of. For example, Omron sells the most RFID labels in Japan with a chip in them; it holds costs down by gravure printing the antennas at high speed. Examples of new markets are the T-ink talking tablecloth for Hallmark, or its radio pillow for Toys R Us, or its interactive placemat for McDonald's.

Then there are the latest talking and recording gift cards. These are only partly printed as yet but they employ interconnects, electrochromic displays, manganese dioxide zinc batteries and switches that are all printed. Fully printed or at least deposited laminar electronics and electrics have hit the market in the form of OLED displays in NEC cellphones and charge indicators in Duracell batteries. In the last year, both Mreal (a project with VTT Technology in Finland) and ACREO of Sweden have demonstrated RFID based on conductive polymers printed at high speed. Costs are one hundredth of the cost of using equivalent silicon chip alternatives, but with the added improvement of being on biodegradable paper.

Printing of electronics and electrics usually involves familiar technologies such as silk screen, flexo, gravure, litho and ink-jet but in modified form. Nonetheless, the result can be an add-on to a conventional printing machine and the benefits of low cost, economical, small runs, rapid production turnaround and devolved manufacture are not lost.

Most printed electronics and electrics today employ inorganics as in silver ink interconnects, sensors and antennas, electroluminescent displays and printed batteries. However, most development work uses soluble organic semiconductors, dielectrics, light emitters, colour changing reflectors and conductors. This is because they can be used to make transistors, high resolution displays, flexible laminar lighting and other components at very high speed. The potential for cost reduction is also greater with organics.

Unlike silicon wafers, and copper antennas and circuit boards, all of which need to be etched – a subtractive process, which typically employs some nasty chemicals – organic semiconductors can be added cleanly to a substrate in order to build up the component. At least 200 companies are developing this new technology, including heavyweight names such as Samsung, Hewlett Packard, 3M, Sharp and IBM, and spin-outs and VC-funded developers such as Thin Film Electronics TFE and Plastic Logic. TFE is aiming for a one gigabyte memory on a few square centimeters of plastic film, but costing only a few cents in high volume. As soon as they can, such companies are co-depositing many components in one very low-cost structure.

The size of the industry will be impressive after a slow start. IDTechEx forecasts a $300bn industry in 2025 for printed electronics/electrics – more than the entire silicon industry today – but, then, this is a technology that will do more than silicon does. IDTechEx sees most of the printed electronics market consisting of new applications in the next two decades, such as the self-adjusting sell-by-date and flexible laminar lighting that doubles as signage, possibly over the whole of the outside and inside of the car. RFID will be fully printed but only to open up the enormous volume potential that silicon cannot touch in creating new markets.

Some aspects of the technology will take longer to realise than others however, but already a lot is happening now. For example, almost 70% of the flash memory based MP3 players use OLED screens rather than conventional LCDs; OLEDs offer better brightness and viewing angles. Samsung has developed 40-inch OLED TV displays, which will be available for sale from 2007. Not all of these are printed today but that is the end game that developers are working towards.

In contrast to these high-end displays, in 2003 Dow Chemical printed a very low cost electrochromic display onto a novelty card, where the display changed colour in sequence. Plastic Logic and Sony are working together to commercialise printed electrophoretic displays, printed organic transistor back-plane drivers for use in electronic books.

“Printed electronics is creating new electronic markets at price points that are way below anything that silicon proponents can dream of”

Despite these successes, an ongoing challenge is the optimal matching of the current performance of printed electronic devices to suitable markets. However, needs exist in healthcare, consumer goods and advertising. For example, disposable testers for blood, pregnancy and so on will have electronic displays in future, providing a considerable improvement in the human interface.

IDTechEx will host a Printed Electronics conference in Phoenix, US, on December 5-6, 2006. For more information, use www.idtechex.com

WIRELESS: transparently simple?

by Myk Dormer

"Something is coming out of the receive data pin, and on the scope it looks a bit like data, but if you turn your transmitter off then all hell breaks loose"

So you've decided that somewhere in your 'new product' a short range wireless interface would provide a great selling feature – maybe for a remote handset, or a short range interface to a diagnostic tool; or perhaps a sensor head or tool needs to operate without the awkward, trailing cables.

At the feasibility stage you just use a simple asynchronous serial data-stream, something like the good old RS232, but probably without the awkward voltage levels. Over the few meters of test cable it works just fine, but, now, you need to prove the radio link. So you look at your data rate, your budget and your available space and try to find a radio.

There are some excellent looking 'turnkey' radio modems in the market, most offering Hayes/AT modem emulation at 9600 baud or more. But those diecast boxes are as big as house bricks, the range extends over several miles (when you need 25m), and the price? – Hundreds of pounds or more.

Something much simpler is called for. So you get a pair of the numerous short range wideband transceivers (marketed by many firms and all much the same, in their neat little 33 x 25mm screen cans), add power supplies and aerials copied from the datasheet, connect your data stream and prey.

The specifications always state ranges of 50-250m (most use 1-10mW in the 433 or 868MHz unlicensed bands), for data rates upwards of 10kbit/s. So why doesn't it work?

Ah! 'Transmitter enable'. A bit like RTS, you need to provide this other signal line to tell the transceiver that a data burst is coming. And you need to assert this signal with enough time to let the unit power up and settle. So, you re-write your software to drive the line, being really careful with the timing (maybe you have to FIFO buffer the data-stream to allow for TX power-up times) and try again. Does it work properly? Nope!

Something is coming out of the receive data pin, and on the scope it looks a bit like data, but if you turn your transmitter off, or even stop sending data with the transmitter on, then all hell breaks loose. Random bytes and framing/overrun errors start spewing out of your UART. What's going on here?!

Believe it or not, it's quite normal. The output of any simple FM/FSK demodulator in the absence of a signal is high level white noise. And telling that from the wanted data is your problem. So, you re-write the software to add some sync and address bytes onto the data bursts, and maybe a checksum or CRC code too, so the, now quite complex, decoder routine has something to look for to discriminate between real data and noise, or interference.

Reliable data communications at last? Unlikely.

Data errors are appearing and they seem to depend on the actual composition of your data stream: Send random bytes, or streams of 'U' or '5' and things seem fine. Send 'space' characters, or include large gaps between bytes and nothing works at all.

Back at the datasheet, a subtle little detail raises its head: the transmission path of all these simple radios is AC-coupled (at the receive end), the response rarely falling below a few hundred Hz. An asynchronous data-stream requires a DC-coupled link, or the unbalance between high and low bit durations accumulates into a crippling mark-space distortion.

And so you re-write the software (again!). Long preamble sequences (of 101010 etc) are added to the transmit bursts to settle the receive end, and either careful byte coding and bit number balancing algorithms are included, or the whole asynchronous format is thrown out, along with the UARTS, and a biphase (Manchester) bit level coding scheme gets adopted.

Seems like a lot of work, when all you wanted to do was send a few bytes of data over a few yards of space. Isn't low power radio supposed to be simple to use?

Myk Dormer is Senior RF Design Engineer at Radiometrix Ltd,
www.radiometrix.com

The rule of THUMBS

Not having a pen, a calculator or even a fax machine are all omissions most of us could do without nowadays. Not having an agile pair of thumbs could prove costly, however. Juan Pablo Conti looks at how RIM is building its BlackBerry empire

The young Mike Lazaridis and Douglas Fregin were still at university when, in 1984, they decided to set up a business and call it Research in Motion (RIM). As ambitious as their idea of what they wanted to achieve might have been at the time, they could never have predicted the explosion of publicity that made of their company's flagship product the gadget that no self-respecting businessperson would dare say they don't own or need today.

The undisputed top-selling brand of what has become known as 'push-email' technology – BlackBerry – has already been deployed in more than 160 cellular networks in 60 countries. By March next year, RIM expects that another 150 operators will have launched their own BlackBerry service. More than six million users pay a subscription fee of between $40 and $50 every month to gain access to their email accounts while on the move using a BlackBerry (or BlackBerry-licensed) handheld device.

"I think they are certainly one of the most successful start-up companies around," said Ken Dulaney, vice president of mobile computing with market research firm Gartner. "Just like Palm did in the mid-nineties, they've brought about a revolution in mobility with wireless email. Their execution from top to bottom has been excellent, providing a very hot value proposition for those people who have purchased it. Today, no-one else has matched all the aspects of excellence of RIM, from the device to the way the email system works, to the relationships with the operators."

The Intricacies of Push Email

Ever since the world started to become so reliant on emails, the telecommunications industry knew that a potentially lucrative market would open up if companies were offered the chance to allow employees remote access to their inboxes via Internet protocol

Right and below: BlackBerry has also proved a popular gadget in Europe

networks. Remote corporate email did become a big business eventually, although the real players to cash in on this phenomenon initially weren't telecom carriers but software companies, especially Microsoft.

By developing the now widespread Microsoft Exchange Server program, Bill Gates's company and others helped establish the concept of remote email and calendar data access. However, these systems still require users to proactively find a spot with Internet connectivity, where they can hook up their computing devices and log on to their company's web-based email system.

Research in Motion is credited as the company that almost single-handedly took this concept a step further by combining the messaging possibilities of Microsoft Exchange and similar software with the widespread availability of cellular networks and users' familiarity with handheld devices, on the one hand, and QWERTY keyboards on the other. Rather than having to check for new messages, email is automatically, wirelessly forwarded (or 'pushed') to subscribers' handsets as it arrives to the office's server, as long as users are anywhere within the reach of their cellular operator's network (or one of its international roaming partners').

RIM uses a proprietary, Real-Time Streaming Protocol (RTSP) to synchronise data transmissions. For handsets to be able to receive the service, they need to be loaded with RIM's client access software. Original BlackBerry handheld devices manufactured by the vendor already come equipped with it. Competing device manufacturers such as Nokia, Motorola or Sony Ericsson are also welcomed to the BlackBerry ecosystem, courtesy of a licensing programme called BlackBerry Connect.

Meanwhile on the office side, RIM's push email platform requires a dedicated server, which also needs to be installed with proprietary middleware: the BES, or BlackBerry Enterprise Server program. It supports Microsoft Exchange, IBM Lotus Domino and Novel GroupWise personal information management systems. A network operations centre located in Canada retrieves email using triple DES encryption and forwards it to the required handset.

Three Revenue Streams

RIM's successful business formula can be described as a delicate cocktail made up of three key ingredients, with each of them generating revenue for the company: hardware, software and services.

The obvious hardware element consists of the BlackBerry handsets themselves. In RIM's corporate structure, they form an entire business unit, called 'Devices'. It's the most important of four divisions in terms of revenue, consistently producing around 70% of the firm's income. During fiscal 2006, RIM shipped some four million handsets.

These are not sold directly to end users, but through the powerful retail infrastructure of partnering mobile phone operators. The Canadian vendor – whose original expertise was actually in radio modems – has, therefore, to constantly keep an eye on new cellular radio technologies being adopted by the networks on which the various BlackBerry models operate. Currently, it supports GPRS, EDGE, CDMA, Ev-DO and Motorola's iDEN (the platform used by operator Nextel).

Competition is becoming a major worry for RIM. The type of handsets it makes, which can support voice but are primarily data communications devices, are catalogued as 'smart phones'. The smart phone market has traditionally been dominated by Nokia, with RIM occupying a distant second place. However, that is no longer the case according to research carried out by Canalys, which at the end of July discovered that RIM had lost its second-place spot to Motorola.

The rival US vendor is already reaping the rewards of what industry watchers are regarding as a very 'sexy' handset – the Q, a Razr lookalike, designed to make even the latest generation of BlackBerries look somewhat old-fashioned.

Samsung and other handset manufacturers are launching similar high-end products that will inevitably

The first BlackBerry was introduced in 1998, with the system taking a decade to develop

erode RIM's market share even further. But the company's chairman and co-CEO remains untroubled by this prospect: "There always has been competition in the wireless market and there always will be," says Jim Balsillie. "An important part of this (like the CEO of a major carrier in Europe recently told me) is that the data plan attach rate of these camera phones is less than 1%, when the incentive to the carrier is, in fact, having an extremely profitable account relationship, as they currently do with the BlackBerry franchises. So, it's not about the fancy devices for the sake of fancy devices; these are subsidised products through a carrier channel."

"There's a lot of competition out there but, then again, this sector is dramatically expanding. So, maybe our overall percentage market share may drop, but the overall market size would dramatically increase to way offset any potential share shift," added Balsillie.

Expensive Plans

The second most important ingredient in RIM's business cocktail is 'Services'. Also forming a separate business unit, last year it captured just over 18% of the company's revenues. The unit makes its living out of the monthly BlackBerry subscription plans, which again has a total base of around six million users. Of the money each BlackBerry subscriber pays each month, a large percentage goes to the mobile phone operator that signed the customer. But RIM still makes a healthy profit from each transaction.

And the good news for RIM is that demand for the service continues to grow exponentially. In only three months between March and May earlier this year, 38 mobile operators launched a BlackBerry service, announced plans to do it or launched a new BlackBerry handset for the service they are already offering. The list includes well-known names such as Sprint, T-Mobile, Vodafone, KPN, 3 and O2, but also carriers in countries such as Chile, Peru, Argentina, the United Arab Emirates, China, Korea, Hong Kong, Fiji, India, Singapore and Indonesia.

No doubt encouraged by such high level of interest, Balsillie sounds anything but cautious when he is questioned about how his company will manage to get to the 10 million subscriber milestone it recently set out to achieve: "I don't want to sound cavalier but, for us, [getting to the 10 million mark] is not about 'if' but about 'when'."

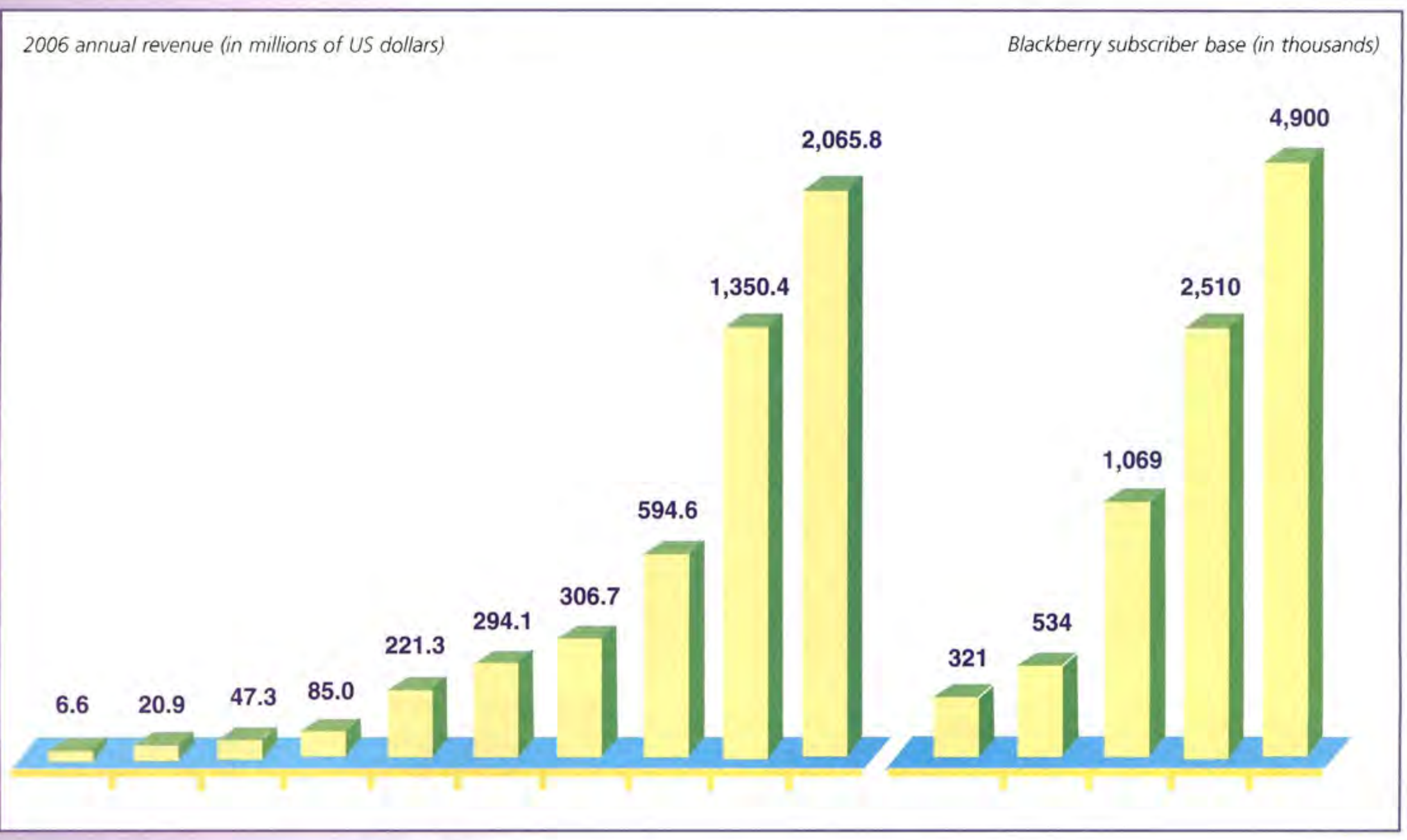
Gartner's Ken Dulaney is, however, a bit more cautious: "They've done a great job with a very tiny part of the eventual market. We believe that, in the next five to ten years, every single cellphone in the world will get wireless email. Email is probably more important than voice to most people today. So, to think that your mobile device wouldn't have email in the future just doesn't make sense to us."

"Given that there's two billion potential mobile email users out there today and given that we have only about 15 million push email users (mostly in the corporate sector and mostly in North America and Western Europe), the market has got a tremendous future in that most of the volume is yet to come. The question then becomes: can RIM capture any significant portion of that?" added Dulaney.

He thinks that, if the company is indeed to gain a sizeable advantage from this trend, it will need to address a series of difficult challenges. One of them has to do with the ability to satisfy the cutting-edge design requirements demanded by mass-market users, not just business customers. "And that, of course, means going up against Nokia and Motorola, among others."

The other major challenge RIM's got ahead of it is the perceived exorbitant cost of the BlackBerry service:

The much newer BlackBerry 8700c



"They will have to work with the operators to bring the prices down," warns Dulaney. "$40 or $50 per month is a very high price, there's no way you're going to capture the two-billion market with those kind of prices. They have to fight the operators who really aren't very good at sizing up the market. Worldwide, most operators have been really unimaginative, I would say. They just have not been successful on the data side, they're really voice carriers. So, RIM has to work with them."

Ironically, Dulaney notes that cellular operators are often reluctant to promote the adoption of wireless email. This is because, while they normally make around $250 per megabyte of transferred data on the much more primitive, SMS messaging technology, wireless email only yields $1 or $2 per megabyte. "So how do you get them to move people to the next step, when they are very interested in keeping the old system going, simply because of the profitability it brings to their company? This is just one of the issues with the operators that RIM is going to have to work hard to overcome," says the analyst.

The Shadow of Microsoft

The final component of RIM's successful push-email business formula is software. The vendor's aggressive licensing scheme means that a constant stream of revenue is derived from both, the BlackBerry Enterprise Server (BES) middleware and client access licences.

But industry experts believe the same server software strategy that helped cement RIM's firm grasp of the wireless email market may ultimately prove its Achilles heel. To sustain this argument, they point to Microsoft's increasing interest in this lucrative business, particularly signalled just over a year ago, when the Redmond-based software giant launched its Messaging and Security Feature Pack (MSFP) for Windows Mobile 5.0.

Essentially a free upgrade for Microsoft Exchange 2003 Server with Service Pack 2, the software crucially added support for the debuting Windows Mobile Direct Push Technology. For enterprise customers, this meant the automatic chance of wirelessly pushing all Outlook personal data (email, contacts and calendar) to associated Windows Mobile-powered smart phones, without having to install any additional servers.

The significance of the move is highlighted by the fact the BES software required to support BlackBerry services costs $4000 for 20 licences, or $3000 for just one user licence.

67.7% Devices
18.5% Service
7.6% Software
4.2% Other

Revenue mix fiscal 2006

Even while Microsoft is increasingly becoming the blackest cloud on RIM's horizon, a group of other players that includes Seven, Visto, Good Technology and Intellisync (now part of Nokia) is also pushing hard to steal a share of the market. And there is evidence they are doing just that. Strategy Analytics research shows that RIM's market share of global mobile email accounts fell by 5% during the first half of 2006. Still,

RIM IN BRIEF

Founded: 1984
Chairman and Co-CEO: Jim L. Balsillie
President and Co-CEO: Mike Lazaridis
Headquarters: Waterloo, Ontario (Canada)
Revenues: $2.07bn (fiscal year ended March 2006)
Net income: $382m (fiscal year ended March 2006)
Employees: 4784, distributed in North America, Europe and Asia
R&D team: 1000 employees/$157m budget
Listings: NASDAQ and the Toronto Stock Exchange

the Canadian firm continues to dominate comfortably with 59% of the market, while none of its trailing competitors (including Microsoft) has yet managed to reach even the 10% mark.

Perhaps the most dangerous threat to the long term sustainability of RIM's model is posed by mobile operators. A surprising new twist in this market emerged in June this year when operator 3, first, and Orange (a week later) unveiled their very own push-email systems. Based on France Telecom's proprietary technology, the Orange Mail Enterprise Service is being marketed to small and medium-sized businesses across the carrier's European operations. Compatible devices include four Orange own-brand SPV handheld devices, as well as Nokia and Sony Ericsson phones.

Interestingly, Orange's move into the new field of 'home-grown push email' comes after the network has been offering both RIM's and Microsoft's services. This would clearly indicate its intention to compete directly with its current suppliers.

Still blessed with an enviable majority of the nascent push email market, exponentially growing brand awareness and a proven track record to identify and deliver the solutions that users ask for, what lies ahead for RIM could actually be a treacherous path. As Ken Dulaney sums up, "right now, they are at the point where they could become either a very significant company or a good company that was around for ten or 15 years but never really made it for the long term".

The device now also works as a traditional mobile phone

LEGAL TROUBLES

There are few dates in Research in Motion's relatively short history that the company will remember as well as 24 February 2006. For that was the day the acclaimed BlackBerry operations came seriously close to being shut down in the US by a district court judge.

The judge was acting on an injunction to ban the service requested by patent holding company NTP, which had previously won a patent infringement suit against RIM. Eventually, he decided not to impose an immediate ban, although he did remind RIM that it had already been found guilty and warned that – should the two litigants not come to a mutual agreement soon – he would consider shutting down the network for good.

Exactly a week later, RIM announced that it had reached a settlement with NTP, after agreeing to pay $612.5m. RIM's co-CEO Jim Balsillie said the motivation to settle the case was not based on RIM finally accepting the patent rulings but because the dragging, high-profile, legal battle was starting to negatively impact the business. This was actually true. The vendor had recently been forced to lower its latest subscriber growth forecast. But, as soon as the settlement was announced, RIM's stock surged back and subscriber additions started to recover.

Then, two months later, another company filed a lawsuit against RIM: its competitor Visto. However, Gartner's Dulaney doesn't expect the new litigation to have much of an impact on RIM: "I think they are in a pretty good shape right now. Yes, they have a lawsuit filed against them by Visto, but Visto is suing a number of parties, and the last time we wrote something about it we thought that it wouldn't really matter until five years from now, if at all."

ELECTRONICA 2006 UK group directory

New concept membranes

IntraAction Europe Custom membrane switch panel

IntraAction Europe has introduced a new concept in the supply of quality custom designed membrane switch panels.

HMI membrane switch panels, keyboards and keypads are produced incorporating materials from approved suppliers and can incorporate real snap-action tactile feedback switching, embedded surface mount LEDs, clear or tinted display windows and other – all at very low cost.

IntraAction also offers to have a total front panel solution, by assembling the customer's complete HMI front – possibly incorporating a rigid metal or moulded support plate, with a sealed toughened glass display window.

Manufactuing takes place in IntraAction's new production facility in Gandhinagar, India. All pre-manufacturing, including design, configurations and quotations are coordinated by IntraAction Europe, which is the European technical and commercial headquarters for IntraAction Technology Pvt Ltd of India.

IntraAction Technology
Stand: C3-637

Thermacore goes 'cool' on export

Ashington-based electronics cooling and thermal management specialist Thermacore Europe won the Queen's Award for International Trade in the summer.

Export sales account for 83% of Thermacore's turnover, with customers in more than 25 countries.

Thermacore Europe received considerable help and advice from UK Trade and Investment expert export advisor Joyce Rawlings in developing its export strategy. "Becoming a successful exporter can have a significant, positive impact on a company's turnover and the region. [It helps] contribute to the £10bn plus of exports that leave the North East each year," said Rawlings.

The Queen's Award is held for a period of five years from the date of its announcement. However, winners can apply for further awards in different categories within this five-year period.

Thermacore specialist products are found in military, telecom, industrial and automotive applications. The firm is the electronics cooling division of Modine Manufacturing Company.

Thermacore Europe
Stand: C4-404

Tough RJ45 connectors: quick and easy to assemble

Amphenol's 'RJ Field' harsh-environment Ethernet connector system is now available from international assembling distributor PEI-Genesis too. It provides RJ45-style Cat 5/5e connections in a rugged, sealed and vibration-resistant housing.

The range is suitable for industrial, telecommunications, transport and military applications, as they use a one-step mating system that requires neither tooling nor time-consuming cable preparation and termination procedures. The plug connectors are designed to depress and protect the RJ45 plastic latch while capturing the complete RJ45 connector in a high-quality insulator. This insulator is then snapped into the plug housing and a simple plastic or metal gland cord grip is tightened on to the cable, providing an IP67 seal in the mated condition.

The range's operating temperature is between -40° and 85°C. The connectors can be specified in four versions offering MIL-C-26482 metallic shells with bayonet coupling, MIL-C-38999 Series III metallic shells with threaded coupling, circular composite shells with push-pull coupling or rectangular composite shells with a quick lever coupling mechanism.

A new range of RJ45 connectors

The connectors meet or exceed the requirements of 10 BaseT, 100 BaseTX and 1000 BaseT networks and are rated for a minimum of 500 mating cycles.

PEI Genesis
Stand: B4.637

ELECTRONICA 2006

Cyclops Group

Cyclops Electronics Ltd
Link Business Park, Osbaldwick
York, UK, YO10 3JB
Tel: +44 (0) 1904 415415
Fax: +44 (0) 1904 424424
Email: sales@cyclops-group.com
Web: www.needcomponents.com
Contact: Daniel Yodaiken

A Global Partner in Electronic Component Distribution, four Specialist Divisions, eight Offices Around the World, over 105,768 Line Items in Stock.... The four specialist areas in which you get a complete purchasing solution to fulfil your requirements....

- A stocking distributor, supplying and reducing lead times for companies that have urgent requirements of Day to Day, Shortage and Obsolete electronic components.
- Procurement, logistics and supply from Low Cost Areas. Specialists in finding quality world-wide suppliers for reduced manufacturing material costs.
- Excess Stock Management Program with over 105,768 different line items, over 600 million parts of active, passive and electro-mechanical components, having released capital from redundant stock worth over £160m.
- Asset Recovery and Recycling facility, which can provide disposal of electronic excess, and professionally prepare valuable components for, re-use.

Hall and Booth Location: A5. 175/1

Electronics Yorkshire

Airedale House, Clayton Wood Rise, West Park, Leeds LS16 6RF, West Yorkshire, UK
Tel: 0113 274 4270
Fax: 0113 274 4328
Email: info@electronicsyorkshire.org.uk
Contact: Dave Williams

Electronics Yorkshire is an IPC Training Centre, Technology Resource and Networking Organisation, with a Network Membership of nearly 400 Companies providing electronics solutions from Concept Design and Development to Prototyping, Assembly and Manufacture. Electronics Yorkshire, a not-for-profit organisation supported by Yorkshire Forward, is the one-stop access point to the electronics industry across the Yorkshire and Humber region of the UK.

Visitors will be provided with information about how international businesses can access this important region's electronics industry resource. They can talk directly with Member Companies who supply and distribute electronics equipment and provide manufacturing, testing and design and development solutions.

Hall and Booth Location: A5.175

Forge Europa

The Old Railway, Princes St
Ulverston, Cumbria, LA12 7NQ, UK
Tel: +44 (0)1229 580000
Contact: Ian Dixon, Sales Manager at the above address or to ian@forge-europa.co.uk or sales@forge-europa.co.uk

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We are experts in LED custom design, technical support and customer service. Visit our multilingual website at www.forge-europa.co.uk for full technical information.

Our extensive ranges include high power LEDs, aLED lighting assemblies, ultra bright LED lighting strips, SpectraLED high performance LEDs, white LEDs lamps and displays, seven segment and dot matrix displays, backlights, through hole LED lamps, SPLEDs (LED bulb replacements), fascia illumination, switch top illumination, and SMD LEDs including 4- and 6-pin RGB versions.

Hall and Booth Location: A5. 175/4

executive search for the semiconductor, mobile and broadcast industries

ICP Search,

Fourth Floor, 132 Queens Road, Brighton, East Sussex, BN1 3WB
Contact: John Monro

ICP Search is a specialist executive search organisation which focuses within the technology areas of Semiconductors, Mobile and Broadcast. Established in 2001, our goal was to provide a service that places our clients needs and our candidate's careers above everything else. Not simply providing an ad-hoc recruitment source, but a methodical and complete solution within our chosen technology sectors. Based on feedback from our clients and candidates, we have more than achieved our goal. Our phenomenal success has been complimented by our simple philosophy: To deliver the most efficient and ethical recruitment services for our clients and candidates alike.

Hall and Booth Location: A5. 175/7

Intellect

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10-12 Russell Square,
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Tel: +44 20 7331 2186
Email: louis.chan@intellectuk.org
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Contact: Louis Chan

Intellect is the UK trade association for the IT, telecoms and electronics industries. Its members account for over 80% of these markets and include blue-chip multina-tionals as well as early stage technology companies. These industries together generate around 10% of UK GDP and 15% of UK trade. For more information go to www.intellectuk.org

Hall and Booth Location: A5. 175

Nanotecture Ltd.

Epsilon House, Southampton Science Park
Southampton, SO16 7NS, UK
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Email: info@nanotecture.co.uk

Nanotecture's core technology is the design of materials that are templated onto low-cost liquid crystals or polymer dispersions. These materials contain regular arrays of well controlled nano-scale pores that significantly increase the surface area of the material. The size and structure of the pores

UK group directory

can be tailored to enhance the properties required for particular applications. These structures have unique properties which are different from bulk materials and importantly have characteristics not available from particle based nanomaterials.

Our principal target markets are batteries, supercapacitors, sensors and coatings.

Hall and Booth Location: A2. Micro-Nano World

PEI-Genesis UK Ltd

Unit 3 , The Trident Centre, Armstrong Road, Basingstoke, Hampshire, RG24 8NU, UK
Contact: Doug Mercer

PEI-Genesis is an international distributor and manufacturer of connectors for applications in the commercial, industrial, defence and aerospace sectors. As well as stocking piece-parts for a truly comprehensive range of connectors from leading manufacturers such as ITT Cannon, Amphenol,Glenair and Cinch, PEI-Genesis uses in-house developed automated assembly machines to enable it to offer an unrivalled 48-hour assembly service. The company's technical expertise is second to none, and its website (www.peigenesis.com) provides a wealth of useful resources for engineers and buyers alike.

Hall and Booth Location: B4.637

STONTRONICS
THE POWER TO SUPPLY

Stontronics Ltd

1 Arkwright Road, Reading, Berkshire, RG2 0LU, UK
Contact: Paul Branston and Martin Dodd

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Hall and Booth Location: B2, 160

TECAN

Tecan

Tecan Way, Granby Industrial Estate, Weymouth, Dorset, DT4 9TU, UK
Email: sales@tecan.co.uk
Website: www.tecan.co.uk

Tecan is a leading manufacturer of customised precision parts. A range of innovative, photolithography-based technologies enables highly accurate, burr and stress-free production.

Tecan manufactures parts and components for a wide range of electronics applications – from discrete component packages, to multi-level SMT stencils, through to advanced RFI/EMI screening enclosures.

Using advanced electroforming techniques in a class 1000 cleanroom environment, Tecan manufactures metal and hybrid multi-level micro-parts – from discrete parts used in MEM and MOEM systems through to micro-embossing tools used to produce micro-circuitry. Sub-micron feature sizes and tolerances are possible.

Hall and Booth Location: A2. 316

TEKNOflex

Teknoflex Limited

Terminus Road, Chichester, West Sussex, PO19 8UA, UK
Tel: 0044 1243 832800
Fax: 0044 1243 832832
Emails: ashorrock@teknoflex.com
Contact: Miss Andrea Shorrock

Teknoflex is the leading UK force in the design, the manufacture and the assembly of flexible printed circuit technologies.

Serving many of the multinational blue chip organisations operating across a wide range of market sectors and electronic applications, Teknoflex offers turnkey interconnection solutions.

From single or double-sided flex to multilayered, flex-rigid multilayered, Sculptured, Regal flex, Pinflex and high volume roll to roll flexible circuits Teknoflex has the capability to connect you.

Hall and Booth Location: B1. 655

THERMACORE
Electronics Cooling Division of Modine Manufacturing Company

Thermacore

12 Wansbeck Business Park, Ashington Northumberland, NE63 8QW, UK
Tel: 01670 859500
Email: info@thermacore.com
Contact: Mr John Broadbent

Showcasing its advanced range of Data Centre, Central Office, Military and Aerospace thermal solutions, Thermacore is the electronics cooling division of Modine; now the largest thermal company in the world.

Hall and Booth Location: C4. 404

WESTSIDE SUPPLIES LIMITED

Westside Supplies Limited

Durban Road, Bognor Regis
West Sussex, PO22 9NR, UK
Tel: +44-(0)1243-860626
Fax: +44-(0)1243-866626
Email: sales@westside-supplies.co.uk

Westside Supplies are specialists in supplying signal and power connectors and cables to manufacturers of electronic equipment. Our extensive range includes Audio, Video, Mains Power, DC Power and other Multipole Signal Connectors. In addition to our unique connector range, we also have significant expertise in supplying battery springs contacts and connectors for any size battery.

We have expertise in designing and manufacturing custom designed connectors, cables, battery holders and battery contacts and can offer a solution for all applications.

Our business has been successful based on our depth of knowledge, flexibility and support we offer our customers.

Hall and Booth Location: B3.108

A new kind of POWER AMPLIFIER

Douglas Self introduces the crossover displacement (Class-XD) principle by Cambridge Audio in its new Azur 840A amplifier, which bridges the divide between the Class-B and Class A solid-state amplifier technologies

The great divide in solid-state amplifier technology has always been between the efficient but imperfect Class-B approach and the beautifully linear but dishearteningly inefficient Class-A.

Many attempts have been made to combine the efficiency of the first with the performance of the second, with none of them being very satisfactory.

Class-B and Its Discontents

There is no doubt that Class-B linearity can be very good. Some time ago, I introduced the Blameless amplifier design methodology in this magazine (*"Distortion In Power Amplifiers"*, Aug 93-Mar 94), which gives very good linearity – typically below 0.001% at 1kHz. However, Class-B has inherent limitations as it generates crossover distortion and it does it at the zero-crossing, where it is always in evidence no matter how low the signal amplitude. At one unique value of quiescent current, the distortion produced is a minimum, which is what characterises optimal Class-B; however, at no value can it be made to disappear. It is inherent in the classical Class-B operation of a pair of output transistors.

Figure 1 shows a simulation of an output stage that illustrates the heart of the problem. The diagram plots the incremental gain of the output stage against output voltage; in other words, the gain for a very small signal. Both 8Ω and 4Ω loads are shown. It can be seen from the Y-axis that in the 8Ω case in particular, the gain variations are very small, with an inoffensive-looking gain ripple around the zero-crossing at 0V output. Unfortunately, this gain ripple generates high-order harmonics that are poorly linearised when the negative-feedback factor falls with increasing frequency, as it usually does.

There has always been a desire for a compromise between the efficiency of Class-B and the linearity of Class-A, and the most obvious way to make one is to turn up the

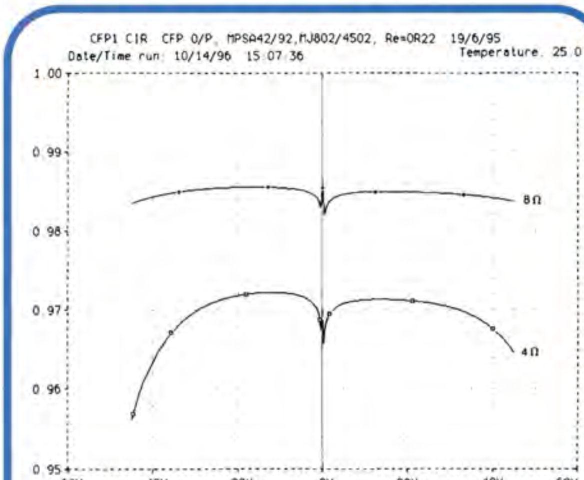


Figure 1: The incremental gain of a CFP output stage as output voltage changes. SPICE simulation for 8Ω and 4Ω loads

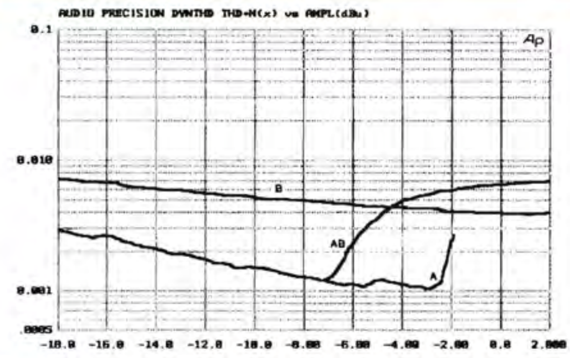


Figure 2: THD versus level for Classes B, A and AB. 0dB is 30W into 8Ω, so this graph runs from 500mW to 48W

quiescent current of a Class-B stage. As this is done, an area of Class-A operation, with both output transistors conducting, is created around the zero-crossing. This can have very low THD indeed, at less than 0.0006% up to 10kHz, as demonstrated in one of my previous articles in this magazine, entitled "*Trimodal Audio Power*" (June, July 1995).

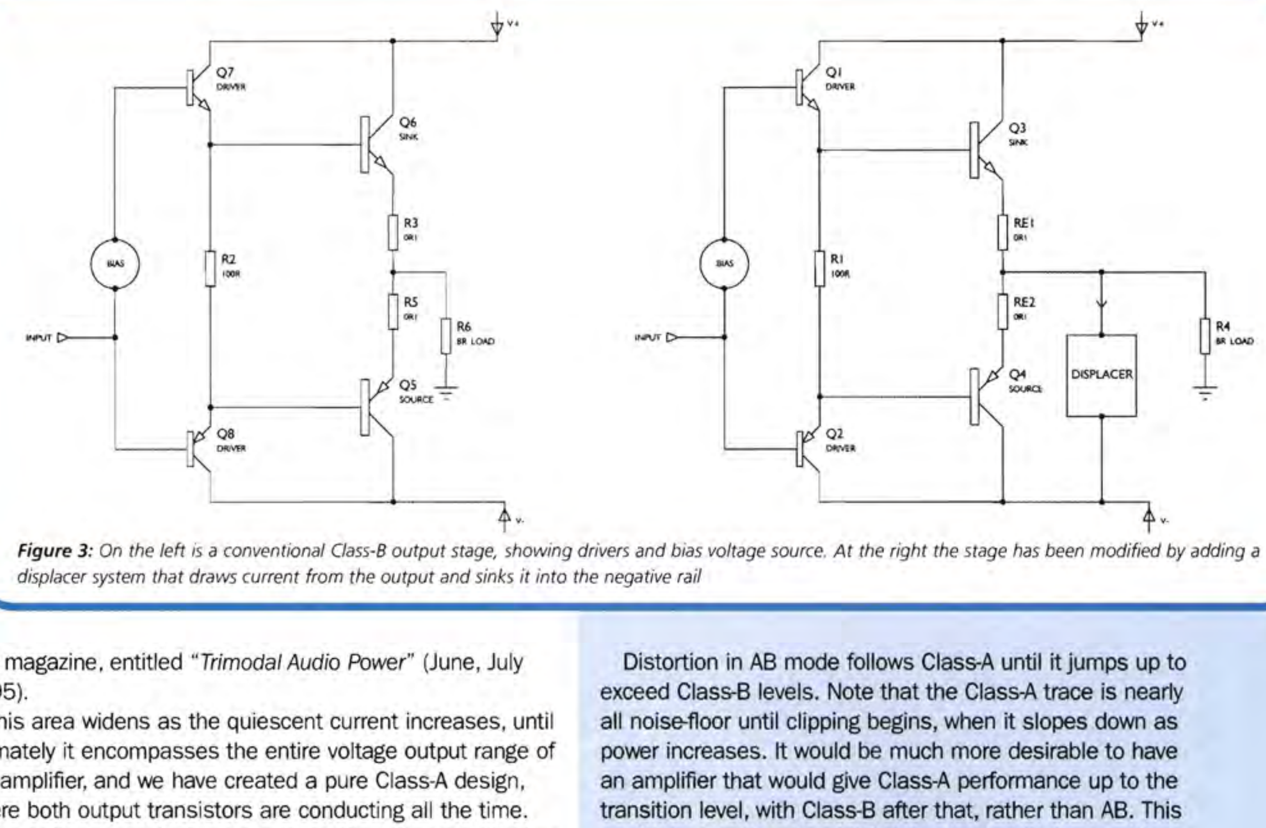


Figure 3: On the left is a conventional Class-B output stage, showing drivers and bias voltage source. At the right the stage has been modified by adding a displacer system that draws current from the output and sinks it into the negative rail

This area widens as the quiescent current increases, until ultimately it encompasses the entire voltage output range of the amplifier, and we have created a pure Class-A design, where both output transistors are conducting all the time. There is, thus, an infinite range of positions between the two extremes of Class-B and Class-A, and this mode of operation is referred to as Class-AB.

Unfortunately, while Class-AB is a compromise between Class-A and Class-B operation, it is not a very good one; once the signal exceeds the limits of the Class-A region, the THD worsens abruptly, due to the sudden gain changes when the output transistors turn on and off, and linearity is inferior not only to Class-A but also to optimally-biased Class-B. This effect is often called "gm-doubling". Class-AB distortion can be made very low by proper design, such as using the lowest possible emitter resistors, as outlined in my book "*Audio Power Amplifier Design Handbook*" (Newnes), but remains at least twice as high as in the equivalent Class-B situation. The bias control of a Class-B amplifier does not give a straightforward tradeoff between power dissipation and linearity at all levels, despite the constant repetition this notion receives in some parts of the audio press.

To demonstrate this, **Figure 2** shows THD plotted against output level for Classes B, A and AB. Measurements were done at 10kHz so the distortion was high enough to clear the noise floor.

Distortion in AB mode follows Class-A until it jumps up to exceed Class-B levels. Note that the Class-A trace is nearly all noise-floor until clipping begins, when it slopes down as power increases. It would be much more desirable to have an amplifier that would give Class-A performance up to the transition level, with Class-B after that, rather than AB. This would abolish the abrupt AB gain changes that cause the extra distortion. This article shows how crossover displacement does just that.

The Crossover Displacement Principle

In Class-B it would be better if the crossover region was anywhere else rather than where it is. If the crossover is displaced away from its zero-crossing position, then the amplifier output does not traverse it until the output reaches a certain voltage level. Below this transition point, the performance is pure Class-A; above it, the performance is normal Class-B.

The essence of the crossover displacement principle is the injection of extra current, either fixed or varying with the signal, into the output point of a conventional Class-B amplifier. This is shown in **Figure 3**. The technique is also called Class-XD.

For convenience I have called the current-injection subsystem the Displacer. Similarly, the upper transistor is the Source, while the lower is the Sink. The displacement current does not directly alter the voltage at the output; the output stage inherently has low output impedance and this is

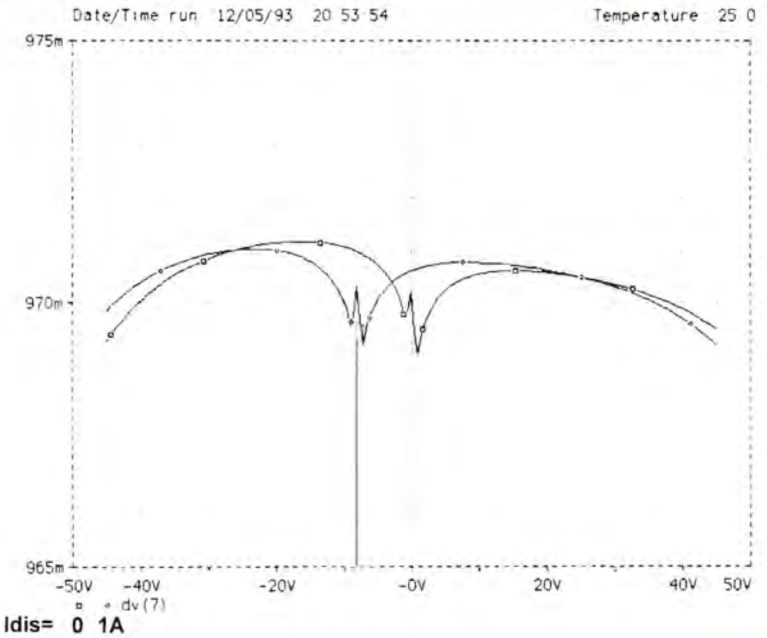


Figure 4: SPICE simulation of the output stage gain variation with and without a constant 1A of displacement current. The central peak is moved left from 0V to -8V

further lowered by the use of global negative feedback. What it does do is alter the pattern of current flowing in the output devices. The displacement current in the version shown here is sunk to V- from the output, rather than sourced from V+, so the crossover region is displaced downward rather than being pulled upwards. This is arbitrary as the direction of displacement makes no difference.

The extra current, therefore, flows through Re1, and the extra voltage drop across it means the output voltage must go negative before the current through Re1 stops and that in Re2 starts. In other words, the crossover point when Q3 hands over to Q4 has been moved to a point negative of the 0V rail; what I call the "transition point". For output levels below transition, no crossover distortion is generated. The resulting change in the incremental gain of the output stage is shown in **Figure 4**. The displacer current may be constant, or vary with the signal.

Realisation

There are several ways in which a suitable displacement current can be drawn from the main amplifier output node:

Resistive crossover displacement

The most straightforward way to implement crossover displacement is to simply connect a suitable power resistor between the output rail and a supply rail, as shown in **Figure 5**.

This method suffers from poor efficiency, as the resistance acts as another load on the amplifier output, effectively in parallel with the normal load. It also threatens ripple rejection problems as R is connected directly to a supply rail, which in most cases is unregulated and carrying substantial 100Hz ripple. The resistive system is inefficient because the displacement of the crossover region occurs when the output is negative of ground, but when the output is positive, the resistor is still connected and greater current is drawn from it as the voltage across it increases. This increasing current is of no use in the displacement process and simply results in increased power dissipation in the positive output half-cycles.

This method has the other drawback that the distortion performance of the basic amplifier will be worsened because of the heavier loading it sees, the resistor being connected to ground as far as AC signals are concerned.

Constant-current displacement

A much better solution is to use constant-current displacement, as shown in **Figure 6.** A constant-current source is connected between the output and negative rail.

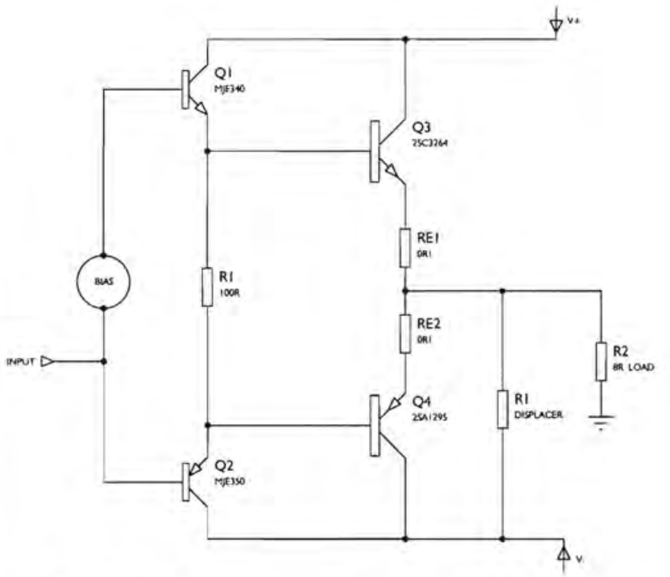


Figure 5: The concept of resistive crossover displacement. In and the following cases, the crossover point is displaced positively by sinking a current into the negative rail

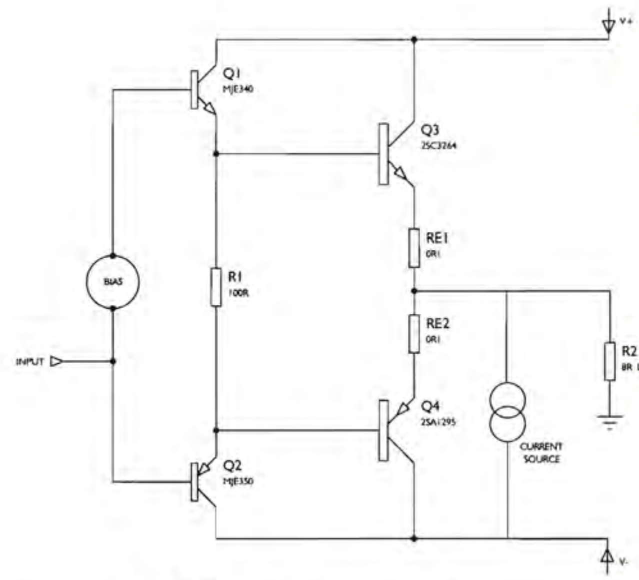


Figure 6: The concept of constant-current crossover displacement

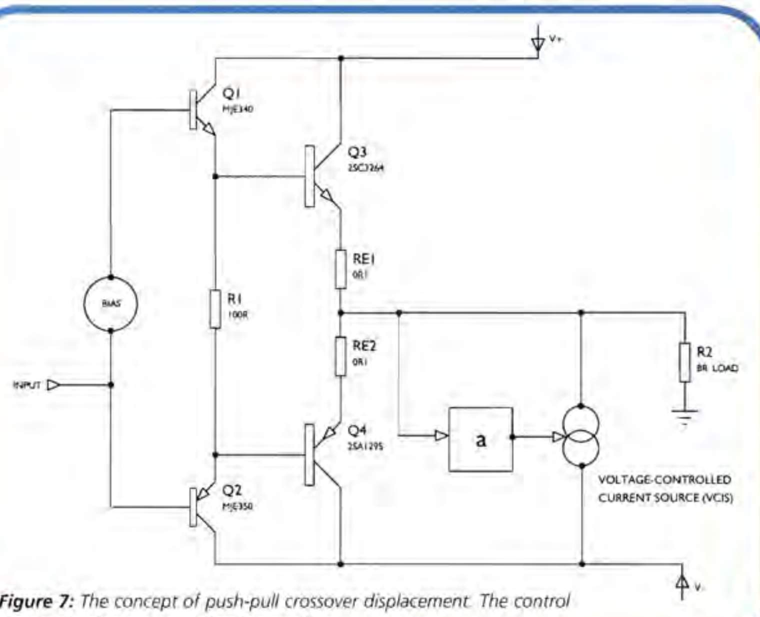


Figure 7: The concept of push-pull crossover displacement. The control circuitry implements a scaling factor of -a

Efficiency is better as no output power is wasted in the displacer due to the high dynamic impedance of the current source. Noise or ripple on the displacement current is greatly attenuated by the very low impedance of the basic power amplifier and its global negative feedback, so complex control circuitry is not required. The efficiency of this configuration is greater, because the output current of the displacer does not increase as the output moves more positive. The voltage across the current source increases, so its dissipation is still up, but by a lesser amount. Likewise, the source transistor is passing less current on positive excursions so its power dissipation is less.

Push-pull displacement

Having moved from a simple resistor displacer to a constant-current source, the next step is to move from a constant current to a voltage-controlled current source (VCIS), whose output is modulated by the signal to further improve efficiency. The most straightforward way to do this is to make the displacement current proportional to the output voltage. Thus, if the displacement current is 1A, with the output at quiescent at 0V, it is set to increase to 2A with the output fully negative, and to reduce to zero with the output fully positive. The displacer current is set by the equation:

$$Id = Iq\,(1 - Vout/Vrail)$$

where Iq is the quiescent displacement current (i.e. with the output at 0V) and Vrail is the bottom rail voltage.

Depending on the design of the VCIS, a scaling factor is required to drive it correctly; see **Figure 7.** Note that an inversion is necessary to get the correct sense of operation.

The push-pull displacement approach has another benefit; it reduces distortion when operating above transition in the Class-B mode. This is because the push-pull system acts to reduce the current swings in the output devices, as the displacement current varies. This is equivalent to a decrease in output stage loading; it is the exact inverse of what occurs with resistive displacement, which increases output loading. Lighter loading is known to make the current crossover between the output devices more gradual and so reduces the size of the gain wobble that causes crossover distortion. While the constant-current displacement method is simple and effective, the push-pull version of crossover displacement is to be preferred for the best linearity and efficiency; the extra control circuitry required is simple and works at low power, so it adds minimally to total amplifier cost.

Practical Circuit Technology

Figure 8 shows a push-pull displacer, with the associated Class-B output stage omitted. The basic problem is to apply a scaled and inverted version of the output voltage to the displacer. The signal must also have its reference transferred to the negative rail, which will carry mains ripple and distorted signal components. The reference is transferred by using the high-impedance output from transistor Q19 collector. Driver transistor Q15 is used to drive the Displacer Q14, so the control circuitry can work at low power levels.

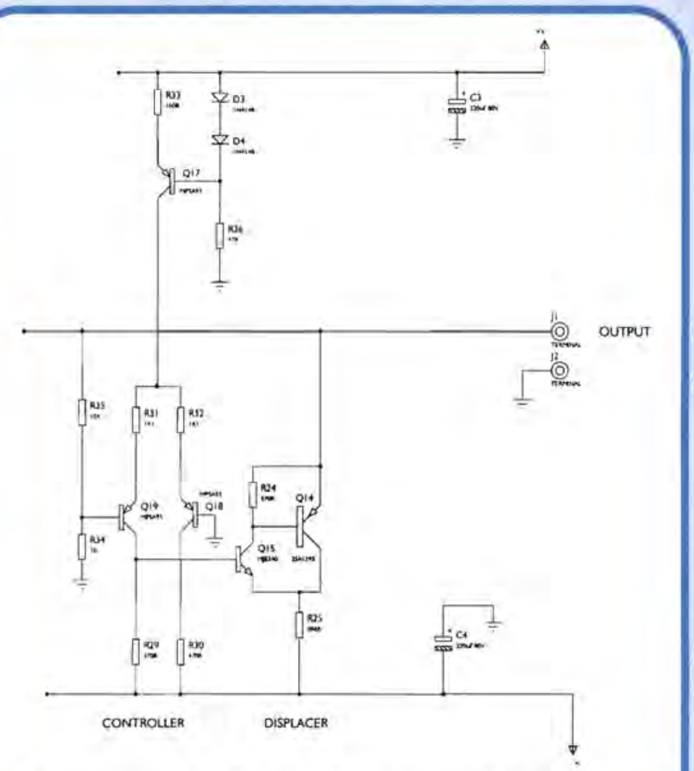


Figure 8: A practical push-pull displacer with complementary feedback pair structure

The controller is a differential pair of transistors with one input grounded and the other driven by the main amplifier output voltage, scaled down by R34, R35. The pair has heavy local feedback applied by emitter resistors R31, R32, to minimise distortion and define an accurate gain. The drive to the VCIS displacer is taken from collector load R29, to give the required phase inversion. R30 simply equalises the dissipation in the differential pair transistors to maintain balance.

The tail of the differential pair is fed by constant-current

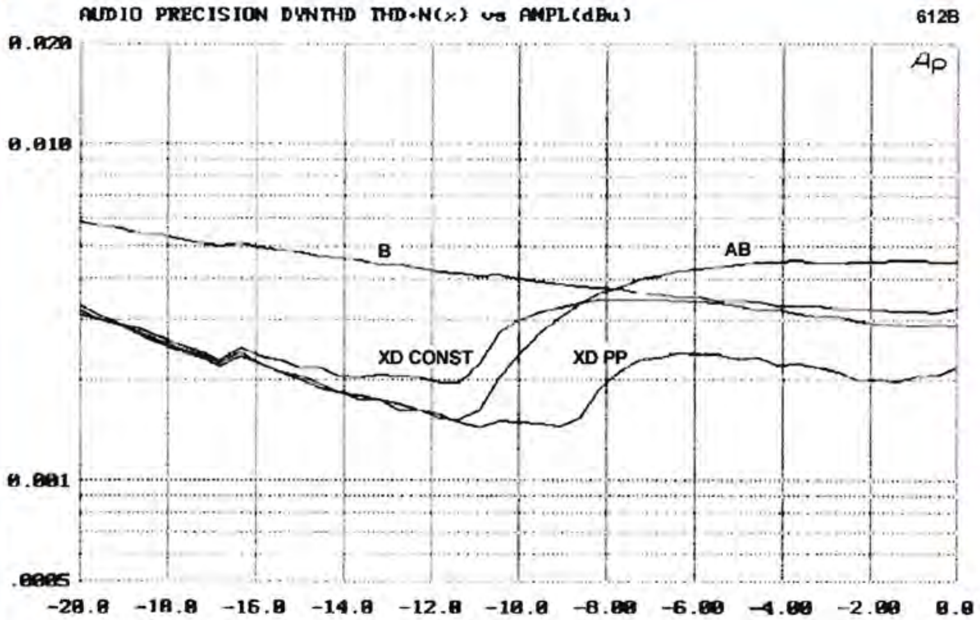


Figure 9: Both constant-current and push-pull crossover displacements give better linearity than Class-B and Class-AB. The push-pull version is much better (0dB is 30W into 8Ω)

source Q17. This gives good common-mode rejection, which prevents the significant ripple voltages on the supply rails from contaminating the control signal. Since half of the standing current through the differential pair flows through R29, the value of the tail current-source sets the quiescent displacement current.

Performance and Efficiency Of Class-Xd

Figure 9 shows how the crossover displacement principle reduces distortion in reality. The B and AB traces are the same as seen earlier in Figure 2.

The XD CONST trace demonstrates how a constant-current crossover displacement amplifier has the same superb linearity as Class-A up to an output of about –14dB, but distortion then rises to the Class-B level as the output begins to traverse the displaced crossover region.

The XD PP trace shows that push-pull crossover displacement gives markedly lower distortion than constant-current displacement. At -2dB, THD is very significantly lowered from 0.0036% to 0.0022% by the use of push-pull, as it reduces the magnitude of the current changes in the output transistors.

The crossover displacement technique increases the total power dissipated in the output stage. The dissipation in the source transistor is increased by the displacement current flowing through it, while that in the sink transistor is unchanged. There is also additional dissipation in the displacer itself, which is likely to be on the same heat sink as the main output devices.

When using crossover displacement, you must decide at the start just how much Class-A power you are prepared to pay for in terms of extra heat liberated, and what load impedance you intend to drive. For example, assume that 5W of Class-A operation into 8Ω is required from an amplifier with a full output of 50W. The crossover point is, therefore, displaced by the peak voltage corresponding to 5W, which is 8.9V. It is well-established that it takes about a 10dB increase in sound intensity to double subjective loudness, (see B J Moore's *"An Introduction to The Psychology of Hearing"*, Academic Press), which is a power ratio of ten times. Therefore, if there is only a doubling in loudness between the transition point into Class-B and full output, the amplifier will be in the Class-A region most of the time.

Table 1 shows the calculated efficiency for the various types of amplifier. "The calculations" were not the usual simple theoretical ones that ignore voltage drops in emitter resistors, transistor saturation voltages and so on, but a lengthy series of SPICE simulations of complete output stage circuits. Thus, the "classical" calculations for Class-B give a full power efficiency of 78%, with more detailed simulations showing that it is only 73% when typical losses are included.

The output stages were simulated using ±50V rails, giving a maximum power of about 135W into 8Ω. Displacement currents were set to give transition from Class A to B at 5W. All emitter resistors were 0.1Ω.

So, we have demonstrated that there is some penalty in efficiency when crossover displacement is used, but it

	Full output	Half power	1/10 power
Class B	74%	54%	23%
Class XD push-pull	66%	46%	14%
Class XD constant	57%	39%	11%
Class A	43%	23%	4%

Table 1: Efficiency of amplifier classes

The Cambridge Audio Azur 840a Amplifier

The Azur 840A is an integrated amplifier rated at 120W per channel into 8Ω. It uses a unique and patented power amplifier technology called Class-XD, but also offering some other features. An important facility is the relay-switched volume control, adjustable in 1dB steps from 0dB to -64dB, and in 2dB steps down to -76dB.

Precision resistors are used in the switched gain networks, giving extremely accurate channel balance.

Among its other features are the relay input selection, low-impedance pre-amplifier design to reduce noise, an RS232 control port and an interface to an ABUS multi-room audio system.

The Cambridge Audio Azur 840A integrated amplifier

MORE than a TEST

James Stanbridge, Sales Manager at JTAG Technologies, provides insight into the boundary-scan technology and its capabilities

Once considered to be something of a black art and solely an aid to manufacturing, boundary-scan is 'coming of age', thanks largely to the emergence of easy-to-use and highly automated tools for developing boundary-scan tests. What's more, boundary-scan is increasingly used as a means of in-system programming (ISP) of flash memory and programmable logic devices (PLDs) and, also, as a debug interface for microprocessors, DSPs and SOCs.

Encouragingly, boundary-scan is now a standard feature of most micros (processors and controllers) – 16-bit and above, such as Freescale's (formerly Motorola) QUICC, ColdFire and Dragonball series, Intel's Pentium and Xscale families, Renesas's (formerly Hitachi) SuperH and Texas Istruments's TMS320 series DSPs. You may also find it in modern variants of some 8-bit systems (see **Figure 1**).

An Unveiling

Boundary-scan is also known as JTAG, after the Joint Test Action Group that developed it. The technology has been around (conceptually) for 20 years. It was officially approved (as IEEE Std 1149.1) in 1990 so, as electronics 'standards' go, it is safe to call it a mature technology.

Even so, there remains a considerable thirst for knowledge of the fundamental 'nuts and bolts' of JTAG and how it can assist in, not only the post-manufacture testing of circuit boards for which was initially developed, but also a variety of board and system development applications.

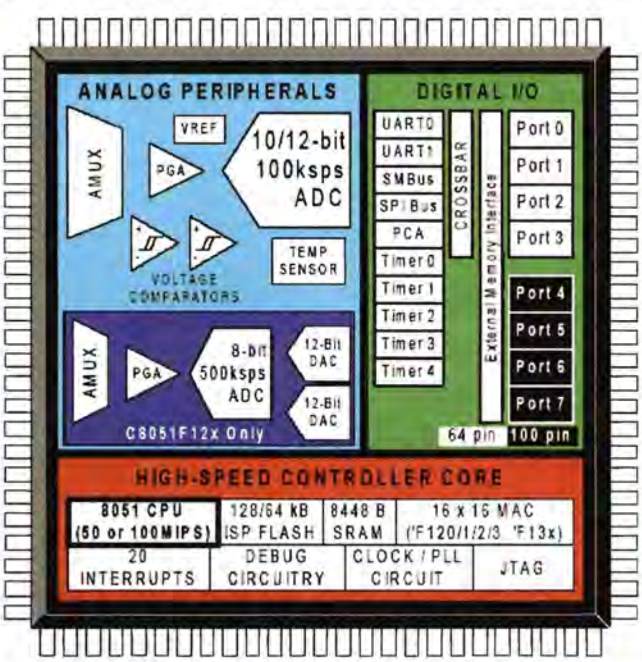


***Figure 1:** Block diagram of a modern micro-controller from SI Labs, featuring full JTAG IEEE Std 1149.1 compatible boundary-scan and embedded JTAG programmable flash memory [Diagram copyright SI Labs Inc]*

Where a boundary-scan version of a micro (or, indeed, any digital component) exists it will typically have four or five additional pins/pads, which together constitute the Test Access Port (TAP). Excluding the TAP and power/ground pins/pads, the devices' other digital pins/pads will usually each have a boundary-scan cell or cells that are 'transparent' during normal operation. It will also have three registers:

- Boundary-Scan Register (BSR);
- Instruction Register; and
- ID Register.

These registers, and the chain of boundary-scan cells, are accessed by the TAP. Data comes into the device on TDI (Test Data In) and exits on TDO (Test Data Out). Two control signals, TCK (Test Clock) and TMS (Test Mode Select) control the state machine with the TAP controller, which synthesises the switch and mode signals that select internal registers via multiplexers and latches.

As mentioned, a fifth pin/pad may be present on the micro. TRST offers an asynchronous reset capability to the TAP controller. However, device reset can also be achieved using a 'soft method', holding TMS high for five clock cycles.

Instructions

The above registers are mandatory (for a device to be IEEE Std. 1149.1 compliant). Also, a boundary-scan device must also accept three instructions.

- EXTEST, which allows external testing via the BSR;
- SAMPLE/PRELOAD, which can load or sample BSR cells without interference; and
- BYPASS, which selects bypass register and puts the device into normal operation.

Three optional instructions were also included in the original standard.

- INTEST, which allows internal [core logic] testing via the boundary-scan register;
- IDCODE, which scans out the ID register's contents (a 32-bit unique device code); and
- RUNBIST, which invokes device level BIST (e.g. using internal scan methods).

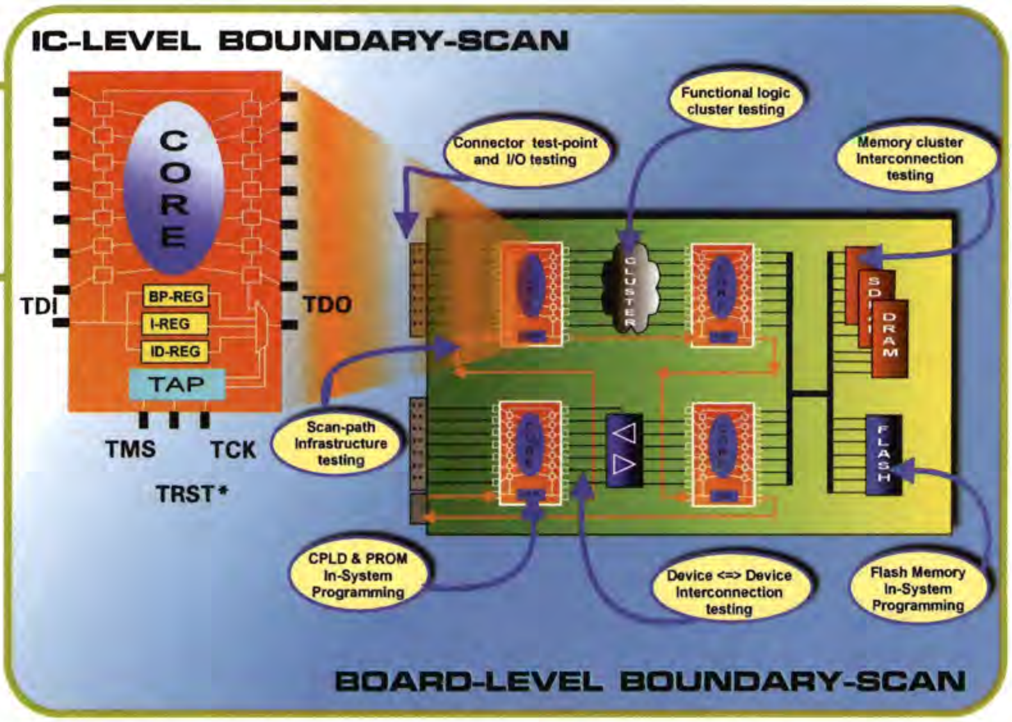


Figure 2: *Boundary-scan as implemented within a device and how boundary-scan components can be daisy chained together at the board level*

There are two more optional instructions in the 1992 IEEE 1149.1a addendum:

- HIGHZ, which selects bypass register – device tri-states all 3-state outputs; and
- CLAMP, which selects bypass register – device outputs set to defined state.

For every IEEE1149.1-compliant device, the manufacturer is obliged to produce a model for the boundary-scan logic known as the Boundary-Scan Description Language (BSDL) file. Close to VHDL in syntax, the BSDL includes a port (pin) description, pin name versus number mapping, supported instruction set and a BSR listing showing the scan cell to pin relationship. These can, typically, be downloaded from manufacturers' web sites.

Boundary-Scan In Action

For test purposes, the above instruction set has proved more than sufficient over the years, allowing the user to:

- **Check scan-path infrastructure and integrity.** This confirms the presence and location of the boundary-scan devices. The check is 'non-disruptive' and can be done whilst the circuit board is functioning normally.
- **Scan-pin to scan-pin interconnect test.** This is used as a post-manufacture assembly test and verifies the electrical connectivity of the nets between components accessible via boundary-scan (where 'accessible' does not necessarily mean that boundary-scan components can only test other boundary-scan components – see later).
- **Memory cluster tests.** Memory (read and write) test patterns can be applied to most memory devices and technologies.
- **Apply 'functional' test vectors (patterns) to non-scan logic elements.**

In addition, thoughtful use of test access provided by boundary-scan has enabled users to create flash ISP applications with relative ease.

Figure 2 illustrates how boundary-scan might be routed around a circuit board and 'zooms in' on a typical device to illustrate how boundary-scan is implemented within a component.

Historically, programmable logic vendors – such as Altera, Lattice, Xilinx and Cypress – were the early adopters of boundary-scan, even though not always in order to use its test features. The attraction of boundary-scan to these silicon vendors was as a programmer interface that could allow register accesses in order to program the EEPROM and/or flash memory that stored the macrocell and gate 'fuse maps'.

Of course, in the early days, each vendor devised its own schemes and instructions to implement this, adding so called PRIVATE [JTAG/boundary-scan] INSTRUCTIONS to those listed here. So, whilst the interface itself was a standard, the data formats and instruction codes were not. Indeed, several attempts were made by a few vendors to introduce 'industry standards' for the configuration codes and procedures (e.g. JAM, XSVF, etc).

By the late 1990s, however, a common PLD programming standard working group was established, which took input from test system developers such as JTAG Technologies, as well as the aforementioned CPLD vendors. By 2001, the new standard IEEE Std 1532 for In-System device Configuration (ISC) was approved.

This standard document had both, the approved data format and the extensions required for compliance to a new BSDL model format. Here, a new minimum set of ISC registers is defined, plus the minimum length for the JTAG instruction register (IR) is now set to 4 bits, in order to decode the 10 mandatory instructions for this standard.

Micros

Just as the PLD vendors used (and built on) the capabilities of boundary-scan for their needs, so too did the microprocessor vendors.

As had (and do) the PLD suppliers, the microprocessor vendors (and here I also include DSPs as processors) 'fitted' the basic boundary-scan functionality – allowing structural board tests to be performed prior to board and system-level functional tests. However, whereas the PLD vendors were focused on adding functions like ISP, the microcontroller vendors added emulator and debug functions – accessible via the standard JTAG/boundary-scan port.

In some instances (e.g. Motorola/Freescale PowerQUICC series) JTAG's TDI and TDO pins are actually multiplexed with the pins DSDI and DSDO (used for an embedded debug port and which allow a device to operate in 'Background Debug Mode').

In theory, this is a smart way to save on pin-count but in practice it requires some design effort to create a system

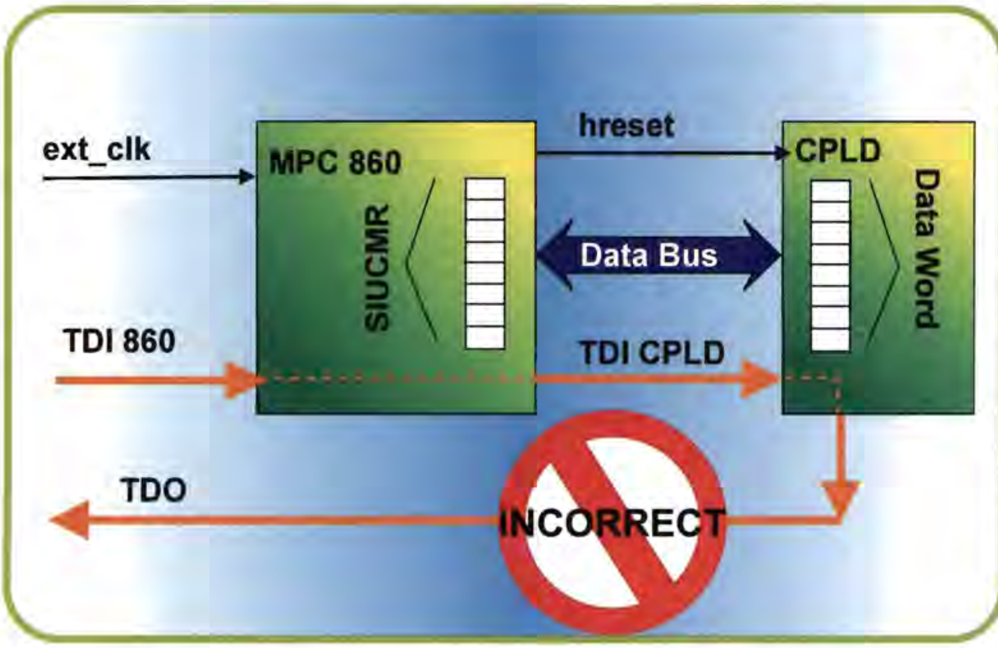


Figure 3: In the case of some devices, JTAG's TDI and TDO pins are multiplexed with the pins used to run 'Background Debug Mode'(BDM). But beware! Whilst the technique does save on pin count, with the set-up above a problem will result if the CPLD is assembled on the board in a blank state. With no config data word programmed, the MPC 860 cannot be switched into boundary-scan mode and the device becomes inaccessible. Only a fresh layout with a separate TAP for the CPLD could solve this problem

which can switch easily between the two modes, due to the convoluted method of reading a field data word into the set-up register (known as the SIUCMR), some 512 clock cycles after an asserted hard reset. See **Figure 3**.

Initially, JTAG/boundary-scan could only be found on larger, 'top-end' 32-bit (now 64-bit) microprocessors and a few 16-bit microcontrollers. However, many silicon companies are now implementing JTAG/boundary-scan across the board. SI Labs (formerly Cygnal) for example, offers an 8051 derivative microcontroller device C8051F120 with full boundary-scan and on-board JTAG debug, plus embedded flash which can also be programmed by register access from the JTAG port. This is offered along analogue inputs and DIO ports in a 64-pin package (see Figure 1).

Coming of Age

With this burgeoning availability of IEEE 1149.1-compliant devices in evidence, more and more engineers are harnessing the power of JTAG/boundary-scan – and employing formalised test techniques – for the first time.

Until recently, the available industry software tools for JTAG/boundary-scan application development have been at best esoteric and at worst long-winded, text-based systems requiring in-depth knowledge of programming syntax and the unit under test.

However, 'low-cost and easy-to-use' (a phrase not previously associated with JTAG/boundary-scan development tools) are now the watchwords of several newly launched development suites, the latest of which is JTAG ProVision from JTAG Technologies.

Clearly, because of the way boundary-scan works (controlling the I/O pins of JTAG-compliant devices on a powered board), it is important to consider what affect running the boundary-scan tests will have on non-boundary scan parts, often called 'clusters'. In the past, it has been necessary to craft the tests such that they do not risk damaging non-boundary-scan parts (which may share nets with boundary-scan devices), when performing interconnect tests.

Now though, tools like ProVision can automate JTAG/boundary-scan test generation, as models are provided (or can be built/requested) for all non-boundary scan compliant parts too. This is a major plus for engineers, in that it saves time and de-risks the tests.

Cluster models can not only be used to disable active parts, but also include the test patterns (or vectors) needed for functional checking. For example, it is possible to clock devices via boundary-scan to verify functional behaviour.

In addition to boundary-scan development tools (software), the associated hardware has also come a long way since the introduction of the standard. For example, controllers with multiple TAPs now allow engineers to design circuit boards with more than one boundary scan chain, thus giving the option for a dedicated chain for programming flash devices via a microcontroller.

Additional tester TAPs also make it easier to 'test through connectors', using a Digital I/O Scan (DIOS) hardware module and accessing the edge of the board and/or test points. Such modules contain JTAG/boundary-scan compliant parts that synchronise with those on the board – and the use of modules can lead to near 100% test coverage.

Lastly, with a modern high-performance JTAG/boundary-scan controller fitted with an internal memory, flash memory devices can be programmed with ease and at respectable speeds (typically 1-2Mbytes per minute).

An Important Role

JTAG/boundary-scan is playing an increasingly important role throughout products' life-cycles. So, whether the concerns are prototype debug, manufacturing process tuning or field service and firmware upgrades, JTAG/boundary-scan has a part to play. Moreover, as the technology disseminates through to all level of circuit board complexity, then more engineers will be exposed to this invaluable test and programming technique.

Also, whilst the (core) standard has evolved over the years, IEEE working groups have developed a number of enhancements, such as 1149.4 (analogue) and 1149.6 (high-speed digital) variants.

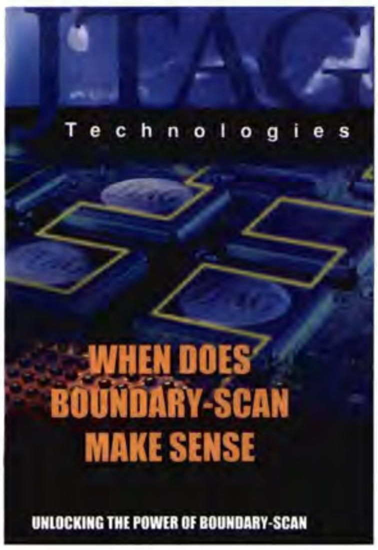
QuadPod is the standard interface hardware supplied with JTAG Technologies's DataBlaster series of boundary-scan controllers. This system operates at a maximum TCK of 40MHz and can be programmed for different voltage thresholds across each of its four synchronised TAPs.

All That Glitters...

Thankfully, now becoming a rarer occurrence is the device that features the 'IEEE Std 1149.1 compatible JTAG port'. This misleading statement may be added to the specification sheet of a device, which, on the face of it, has all the correct attributes to be tested by JTAG/boundary-scan. It has the TAP controller, the four (or five) TAP signals – TDI, TDO, TMS, TCK (TRST). In some cases, there may even exist Boundary-Scan Description Language (BSDL) models, even though, bizarrely, the devices may have no Boundary-Scan Registers (BSRs). With such devices, the TAP has been added purely to access emulator or debug functions, or in some instances, such as with early Altera MAX 7064S parts, ISP-only functions.

Examples of such "no BSR" microcontrollers include some devices that feature ARM RISC processor cores, such as Atmel AT90 series and some NetSilicon parts. Others include Hitachi H8, Freescale MAC 71xx, TI MSP 430 microcontroller and also some of Texas Instruments's DSP range.

If in doubt, ask your supplier to provide the BSDL model. If they cannot, then be suspicious. If they do supply the model then open it in a text editor and check the 'Port description' to see if all pins are assigned as 'linkage bits'. If they are, then this means no JTAG/boundary-scan access.



Further Reading

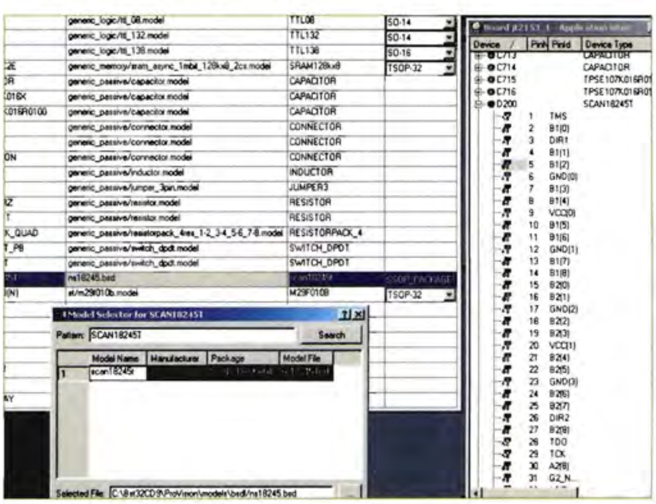
Copies of JTAG Technologies's Board DFT Guidelines and the accompanying overview booklet, *'When does boundary-scan make sense?'*, are available for free. Simply email JTAG Technologies at **info@jtag.com**, giving your name and full address and setting the Subject as 'Guidelines'.

Model Mapping

Model mapping is key to, not only developing boundary-scan tests, but also programming microcontrollers and other devices. As a minimum, the maps must contain the BSDL models of JTAG/boundary-scan compliant parts and intelligence of all non-1149.1 parts.

Thankfully, modern tools come with extensive libraries. For example, JTAG ProVision comes with a library of more than 5,000 models: and any models absent from the library can be created via a guided wizard built into the special editor. What's more, you can always ask your tool vendor to create new models as required.

Once mapped, any organisations can benefit from 'development re-use', by associating in-house device reference codes to library model names. For new projects, model maps need only be modified to include 'fresh' or updated device types, further adding to the simplicity of the operation.



REQUIREMENTS FOR a sensorless brushless

New electronic components that streamline the design of motor controllers are playing a key role in allowing engineers to evolve appliance designs to benefit from brushless motor operation. By **Sergio Biancifiori**, Technical Sales Manager at Future Electronics Europe (Italy)

Brushless motors are increasingly being designed into applications that have traditionally relied upon DC and asynchronous motors. The main benefits include generally lower unit costs for brushless motors and the ability to control speed and torque electronically. This not only saves mechanical design but also enables energy savings in domestic appliances, fans, compressors and industrial drives, which traditionally alternate between being switched off or operating wastefully at full speed.

Brushless motor control algorithms require rotor position data to calculate the PWM output, but the use of sensors such as Hall Effect devices to detect rotor position adds cost and complexity, and challenges reliability. Hence, designers are keen to achieve sensorless detection of rotor position.

To this end, the latest generation of microcontrollers with DSP capabilities provide sufficient computational power to support complex motor control strategies, including calculating speed and position information that must normally be collected by additional sensors. On the other hand, power modules are also available, which use smart power technologies to combine power MOSFETs or IGBTs with current measurement capabilities. These simplify power electronic design and enable a compact and self-contained solution that can be easily assembled into the end product.

Motor Types

Four core aspects can be highlighted in a motor control system. These are:

- **Control unit:** This executes the sophisticated position and speed estimation algorithms to control the motor, based on input signals and data from sensors. The control unit also manages system protection related to the motor.
- **Power converter:** This supplies power to drive the motor and is controlled by the DSP via a specific interface.
- **Sensor:** A sensor is traditionally used to feed back motor-position information, which will be used by the DSP to calculate the drive power required by the motor.
- **Auxiliary circuit:** System power supply and general protection circuitry complete the brushless motor controller design.

Broadly speaking, there are two types of brushless motors in common use. These are the Brushless DC (BLDC) motor and the brushless AC-motor, otherwise known as the Permanent Magnet Synchronous Motor (PMSM). Both types comprise a permanent

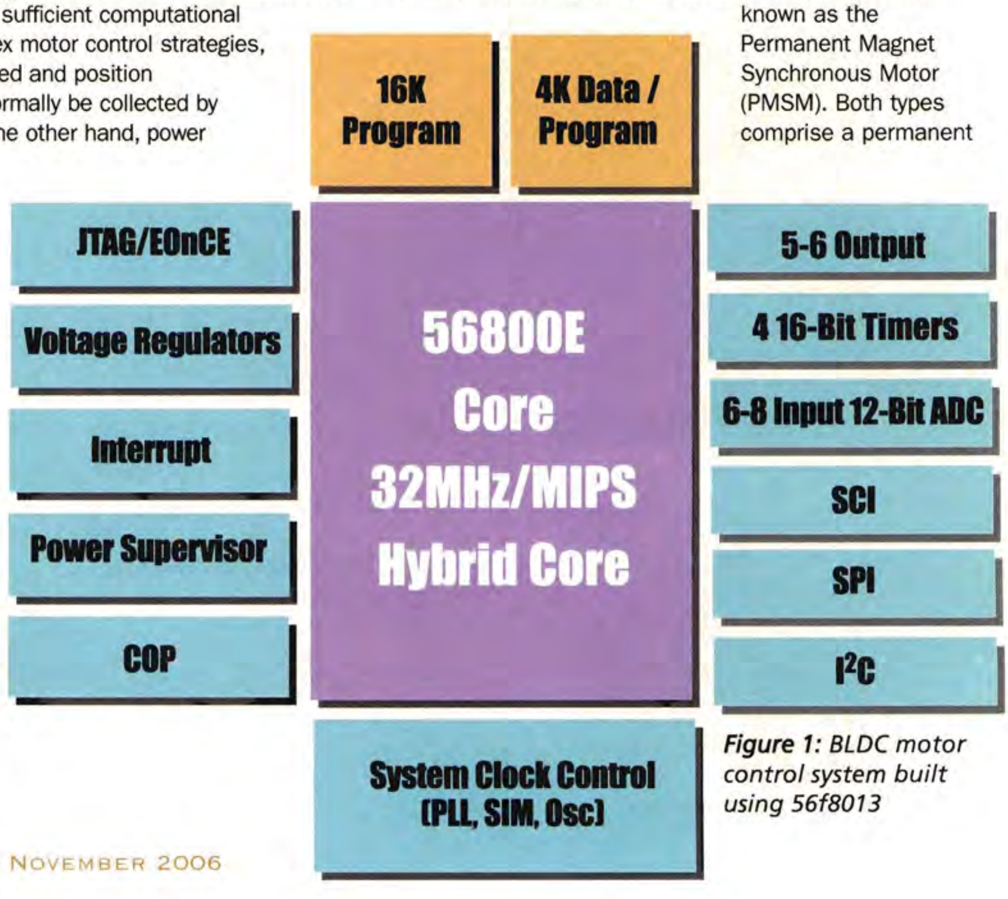


Figure 1: BLDC motor control system built using 56f8013

IMPLEMENTING motor control design

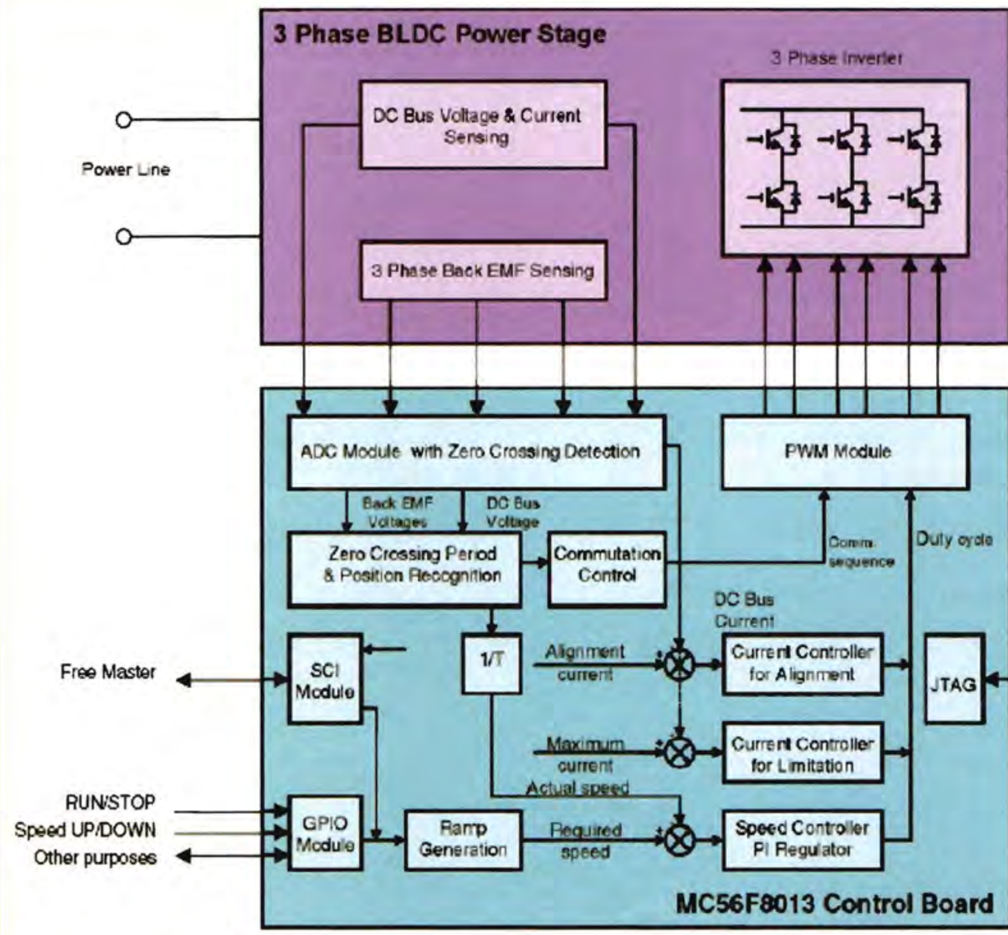


Figure 2: The 56F8013 DSC combines digital signal processing with dedicated motor control peripherals

magnet rotor that produces the excitation magnetic field, with stator windings arranged in either two or three phases. In BLDC motors the windings are arranged so that each phase generates a trapezoidal magnetic field at the air gap along the stator. In the PMSM, the rotating field is sinusoidal.

Working Principles

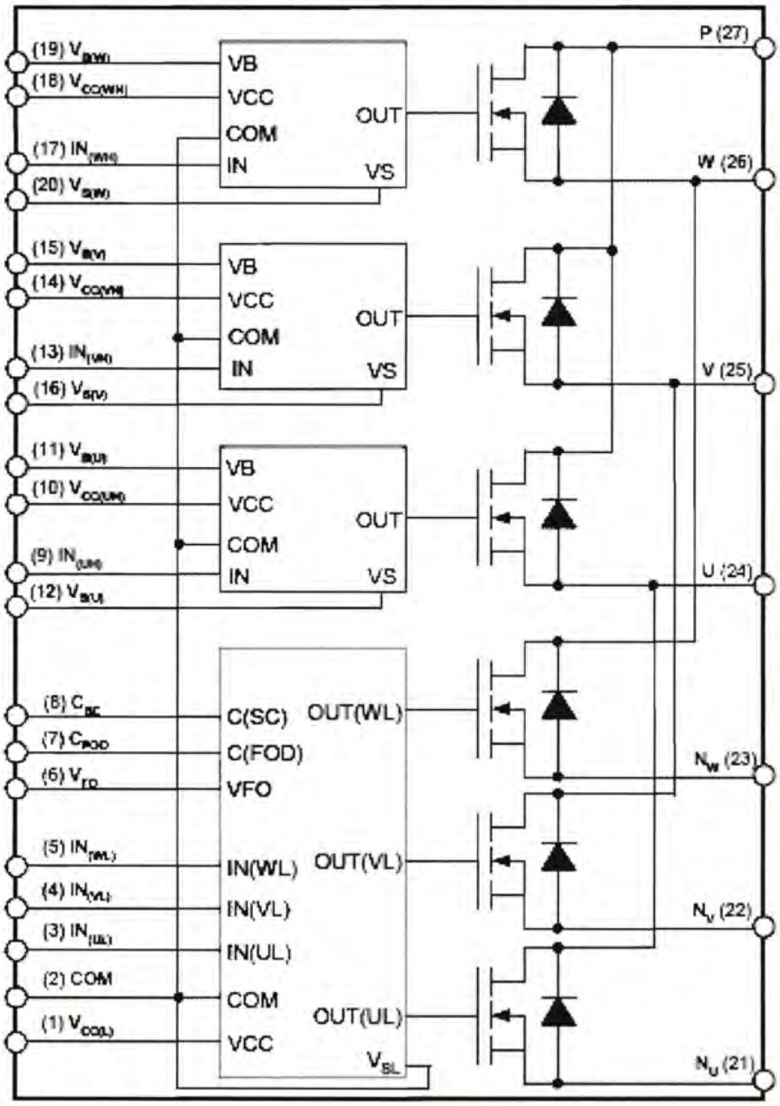
In a PMSM, a three-phase sinusoidal voltage system (120° shifted) is applied to the stator winding, which sets up a rotating magnetic field around the rotor. The rotor seeks to align itself with this rotating stator field, thereby creating a torque that is greatest when the stator and rotor flux are separated by 90°. The torque is zero when the fluxes are aligned. Finally, the rotor speed is equal to the stator frequency. For this reason, this type of motor is called synchronous. The motor speed can be controlled by adjusting the frequency of the three-phase power.

The PMSM has certain advantages over the BLDC, including lower torque ripple, lower audible noise and a better ability to operate at low speed. On the other hand, the motor construction tends to be more complex and a sophisticated control algorithm is required. The motors are normally equipped with a quadrature encoder to sense for rotor position and rotation speed feedback; sometimes Hall sensors are used to detect starting positions.

In a BLDC, the stator phases are fed with a sequence of trapezoidal shaped voltages, which combine to create a rotating magnetic field with a rectangular spatial distribution. The simplified two-pole model shown in **Figure 1** is a useful aid to understanding the basics of this type of motor.

Feeding coils U and W set up a magnetic field oriented as N' and S' in the figure. Hence, the rotor with its N-S orientation experiences a torque and begins to rotate; note that, initially, the two fields are 90° displaced. After 30° of rotation, the stator coils are commutated so that the new configuration will produce a stator field that is 120° displaced in respect to the rotor field. As explained, the rotor tends to follow the stator field, such that the displace-

Figure 3: *FCBS0550 550V MOSFET inverter module, with separate negative links supporting single leg current monitoring*



ment decreases to 60° again. A new commutation will be performed at this point and the situation continues to repeat itself so that a 360° rotation is achieved.

The correct time to commutate the power to the coil is determined by three Hall sensors, placed inside the motor. Hence, six different configurations are possible to produce maximum efficiency by causing the fields to operate always with displacement between 60 and 120°, with 90° as the medium. Remembering that maximum torque is obtained when stator and rotor field are 90° shifted, it is clear that the torque produced by a BLDC is characterised by appreciable ripple.

Fundamental to Operation

In both cases, rotor position sensing is fundamental to the operation of the motor and Hall sensors are the traditional solution. However, these add to the bill of materials, require extra wiring and represent an additional failure mechanism: a wire disconnection or a sensor failure causes the motor to stop. This is expensive in terms of maintenance and will result in generally poor market perception, as well as increased cost of ownership in industrial applications.

Another disadvantage is that, to produce precision speed control using Hall sensors, a more expensive quadrature encoder or a tachogenerator is usually required. Hence, creating a sensorless solution, thereby eliminating the need for Hall sensors and the associated circuitry, is desirable to reduce the cost and enhance the reliability and longevity of appliances featuring variable speed motor drives.

To perform sensorless control, the rotor position information must be derived indirectly from other measurements taken while the motor is running. For both motor types this requires measuring or estimating the back emf induced by the rotor in each stator phase. In BLDC motors, one phase is always unpowered. This allows back emf measurement and zero crossing detection to be used to calculate the correct switching time and configuration.

In a PMSM the back emf waveform must be estimated and rotor position information then extracted by means of inverse trigonometric function. In practice, a number of disturbance effects are also superimposed on the stator voltage waveforms, which must be filtered out before the data containing the rotor position information can be extracted.

DSP machines are an excellent choice to meet the high computational demands implicit in a practical implementation of sensorless motor control.

Digital Signal Controller

Freescale recently introduced the 56F8000 DSC (Digital Signal Controller) family, which combines DSP functions with microcontroller type management. The 56F8000 devices are based on a high performance 16-bit core capable of 32MIPS and are equipped with a large complement of peripherals serving applications, including motor control and many others. The 56F8013 shown in **Figure 2**, for example, is optimised for motor control applications with the inclusion of the following peripherals:

- A three-phase PWM module with a 15-bit resolution and a set of programmable faults and configurations.
- A 12-bit ADC that enables simultaneous conversion and, for example, zero crossing detection.
- Timer module with 16-bit resolution and a multi-channel structure that may be used for speed or time calculation.

For the BDLC the software incorporates:

- Motor control with closed loop speed and current limitation.
- Motor starting from any position, using an alignment procedure to enable known initial rotor position, required for correct feeding sequences.

- Back emf sensing, synchronised to PWM to minimise disturbances caused by PWM switching on the active phases, due to mutual inductance and capacitance.
- Commutation time is calculated and updated during the running process, allowing corrective actions in the event that zero crossing is not captured.
- Starting procedure for low speed, pre-defined, commutation timing; this is required, since at low speeds, for example when starting the motor, the back emf amplitude is too low to be sensed.

For the PMSM the software includes:

- Motor control based on FOC (Field Oriented Control), which is used to maintain stator and rotor flux in quadrature, to maximise torque efficiency.
- A back emf estimator, called SMO (Sliding Mode Observer), whose output is used to calculate rotor position and speed information.
- Speed and current closed loop for better speed and torque performance respectively.

Smart Power Module

In addition to implementing position estimation algorithms, designing the power stage of a motor controller presents another appreciable challenge to engineers seeking a fast and cost-effective solution. The power dissipation and disturbance effects associated with high current and high voltage operation in particular, require appreciable effort even from a skilled power designer, for example to optimise the layout in order to reduce the side effects of power switching. One of the more delicate parts is the layout of the driver for the power switches. These may be built using MOSFETs or IGBTs, depending on the voltage rating required.

To solve these challenges, some manufacturers offer a complete module, integrating the required power switches with drivers and interface circuits, requiring only the motor control input signals, as well as the power supply to drive the motor directly. Design is reduced to a simple process of dimensioning the heat sink to match the power rating. The layout is already optimised inside the module, to minimise trace lengths and to reduce power losses and capacitive/inductive side effects. Additionally, the power frame is reduced in size relative to a discrete solution, leading to a more compact overall design.

Fairchild, for example, has the FCBS family of Smart Power Modules comprising a 500V MOSFET inverter with integrated drive, protection and system control functions, as shown in **Figure 3.** HVIC technology enables single-supply MOSFET gate driving capability without requiring opto-couplers, contributing to an overall 20% board size reduction compared to a discrete implementation. The components are mounted on a low thermal resistance ceramic substrate to efficiently remove heat to the surface of the module, where a heat sink can be attached. Integrated protection includes under-voltage lockout and short circuit protection, while separate negative DC link terminals enable single leg current monitoring.

International Rectifier (IR) has solved the challenges of cost-effective brushless motor design with its IPM (Intelligent Power Module), featuring high integration and IR's proprietary three-phase gate driver and high efficiency trench IGBT technology, shown in **Figure 4**, in a single in-line package. One IPM replaces more than 20 discrete components and IR has used insulated metal substrate technology for high thermal performance and reduced EMI. This creates a complete power stage solution for energy-efficient appliances and light industrial equipment driven by variable speed motors. Available modules are optimised for power ratings from 400W up to 2500W.

As one example, the IRAMS06up60A is rated to 6A and integrates IGBTs and gate drivers, as well as temperature monitoring, over-current shutdown, under-voltage lockout and cross-conduction prevent logic. Other integrated features, such as bootstrap diodes for the high-side drive function and the single polarity power supply, simplify overall system design. No additional isolation is required, as the devices themselves achieve up to 2000Vrms/min. IR has also published a web design tool at www.irf.com/design-center/ipm to help designers build solutions using the IPM family with the IRMCK series of motor control ICs.

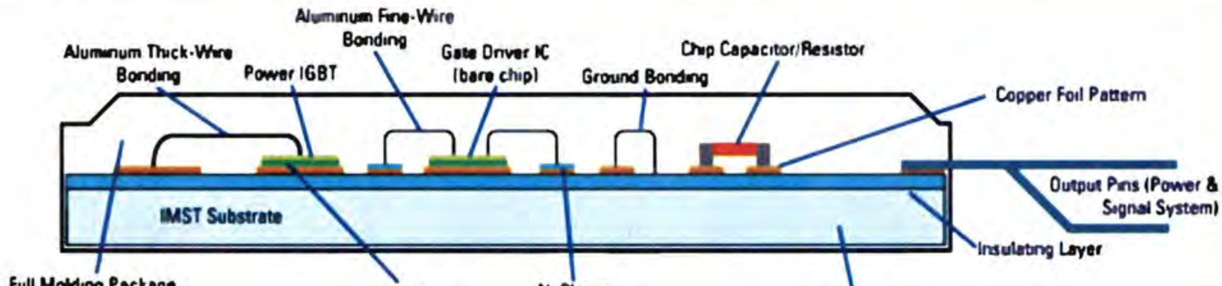


Figure 4: The International Rectifier IPM integrates digital circuitry with high power drivers

Accelerating COMPUTE INTENSIVE FUNCTIONS using C

Joe Hanson, business development director at Stretch, explores how to accelerate application processing using software configurable architecture to achieve hardware-accelerated performance with C, using the example of hardware accelerating a finite impulse response (FIR) filter

Today's electronics devices, whether for embedded, industrial, consumer, entertainment or communications applications, need to process more data in shorter periods of time. The flexibility of general purpose processors has made their architecture of choice for applications for a long time now, while digital signal processors (DSPs) are chosen for their computational capabilities. In many cases both features are needed.

While increasing the clock rate of a general purpose processor extends its performance capacity, it also increases cost and power consumption. To meet the compute requirements, hardware acceleration or specialised auxiliary components are added at the expense of increasing programming complexity.

Software Configurable Processors

Most high-performance markets are in a constant state of flux, chasing evolving standards and ever-changing system requirements. ASIC-based architectures, while offering the needed performance, cannot quickly or cost-effectively enough meet changing application specifications. As a result, many developers have begun to turn to software configurable architectures, which merge programmable logic with application processors.

The advantage of a software-configurable architecture is that programmable gates are organically integrated within the same pipeline as the application processor. This is in contrast to coprocessor-based architectures, which use an FPGA or ASSP to offload processing as a separate system component. The coprocessor approach introduces complex application partitioning and requires the application processor to stall or implement complex scheduling mechanisms while waiting for results. Additionally, designing for an FPGA requires a separate development environment from the application software and, often, a second development team as well.

Because software configurable processors implement programmable logic in the same pipeline as the application processor, it is possible for the compiler to manage partitioning of an algorithm into hardware and software, as well as manage any dependencies. In effect, developers can treat "hardware as software", writing application code in a single development environment that results in hardware and software optimised to work together.

Instead of spending significant development resources hand tuning application code, developers can highlight computational hotspots for the compiler to implement in hardware as extension instructions, which the application processor executes in the same pipeline as traditional instructions. The difference is that extension instructions represent hundreds to thousands of C instructions and computations executed in effectively a single cycle.

The Basic FIR Filter

FIR filters contain computational hotspots that lend themselves well to parallel implementations. While the following discussion focuses on how to hardware accelerate a C implementation of such a filter, the optimisation concepts are general enough to apply to any algorithm.

An FIR filter can be described using the following equation:

$$y(n) = \sum_{t=0}^{t=T-1} ((h(t) * x)(n-t)) \text{ for } n = 0,\ldots N-1$$

where x(n) is the input signal, y(n) is the output signal and h(t) the FIR filter coefficient. **Figure 1** shows a useful way of visualising the FIR function, with every dot on the grid representing the product of a coefficient h(t) and data point x(n-t), and every diagonal line all the products that must be added together to obtain the output y(n). **Listing 1** offers a straightforward C implementation of the FIR filter. A 64-tap filter using T=64 and N=80 would require approximately 27230 cycles to execute. Given its inherent parallel structure, it is an excellent candidate for hardware acceleration.

Key Acceleration Considerations

When determining how to exploit parallelism in an algorithm, it is important to consider several architectural characteristics:

- **Bus width:** How data is passed between the main CPU and accelerated implementation of the algorithm has a significant impact on overall efficiency and throughput. This is because the bus limits how quickly data can be transferred, both as input to the accelerator and as output. A bus that is too narrow or slow becomes a bottleneck; it doesn't matter how efficient the extension instruction is if it cannot be fed data fast enough to keep it fully utilised.

To increase overall throughput, some architectures offer multiple buses between the main CPU and accelerated hardware. For example, the software configurable processor from Stretch has three read and two write ports between the application processor and programmable fabric, each 128 bits wide and providing up to 384 read bits and 256 write bits per extension instruction issue. Efficient utilisation of these buses enables more efficient exploitation of parallelism.

It is important to be sure to include in bandwidth calculations the bandwidth required to transfer results back to the main CPU, as well as to handle intermediate results.

■ **State registers:** Accelerating a complex algorithm often calls for partitioning the algorithm in such a way that acceleration hardware computes only a portion of the result of each iteration. This means there are often intermediate results that must be passed on to the next call to the function. For example, in the initial C implementation of the FIR filter, a running sum must be maintained between each iteration. When more advanced optimisation techniques are applied, the number of intermediate results required increases.

To preserve intermediate results, the values are passed back over the data bus to the main CPU, which then sends them right back to the function for the next iteration. This process consumes not only limited bus bandwidth but also precious main CPU cycles, reducing overall processing efficiency.

Such inefficiencies can be avoided through the use of state registers. State registers provide a mechanism for storing intermediate results between function iterations without involving the main CPU or passing data over the bus. As a result, architectures that utilise state registers can increase overall parallelism more efficiently.

■ **Data Size:** Many architectures provide a limited subset of data width options. For example, a Boolean variable requires only a single bit but is often implemented as at least a byte in size. While this increases efficiency in general – the cost of masking for a single bit every time the value is needed exceeds the value of conserving seven bits – it introduces inefficiencies when passing data to an extension instruction if the CPU must strip and pack bits directly. Additionally, in order to conserve programmable logic resources, registers must be able to be defined as to eliminate unused bits.

Finally, bus bandwidth can also be maximised if unused bits are eliminated before they are passed to the bus. Ideally, these issues should be dealt with within the programmable logic, since requiring action from the CPU reduces the overall rate at which the CPU can issue extension instructions.

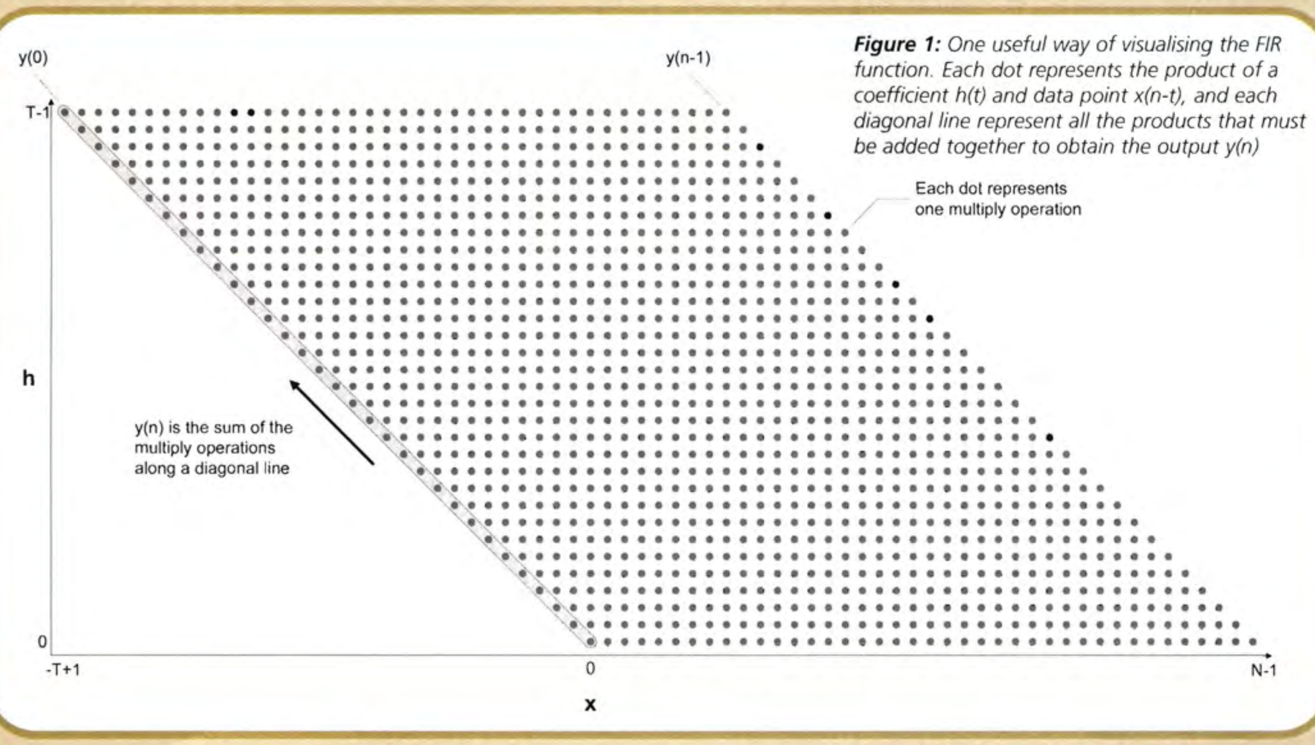


Figure 1: *One useful way of visualising the FIR function. Each dot represents the product of a coefficient h(t) and data point x(n-t), and each diagonal line represent all the products that must be added together to obtain the output y(n)*

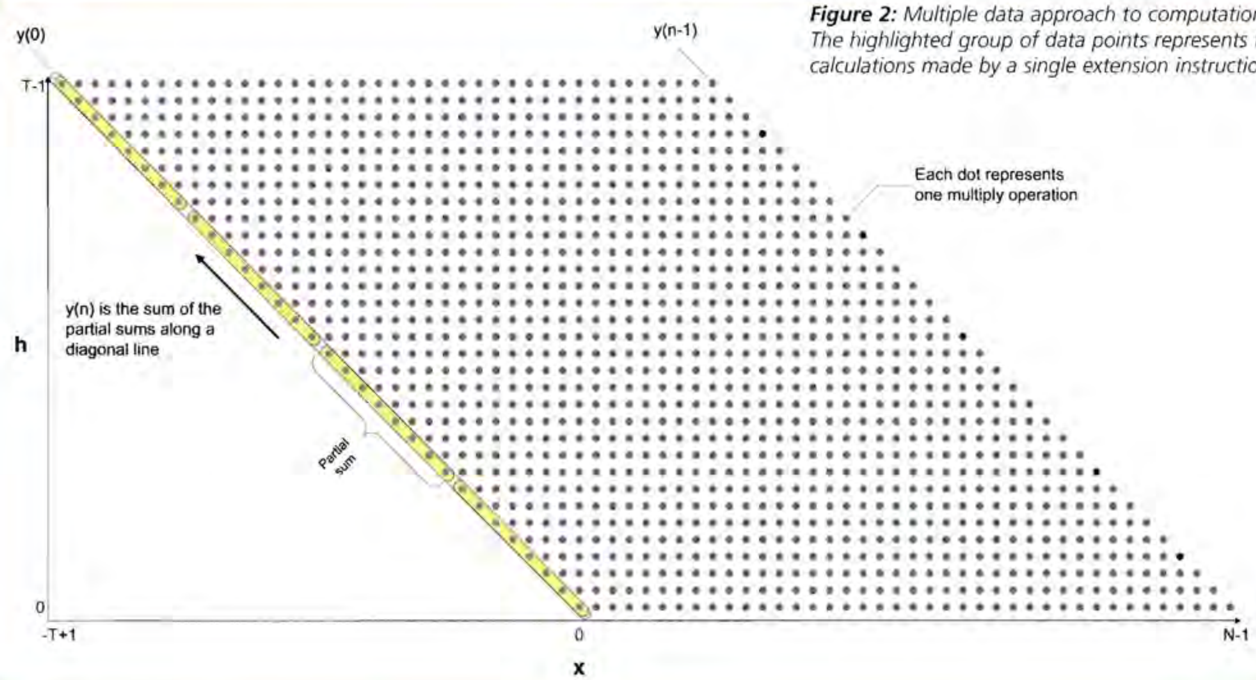


Figure 2: *Multiple data approach to computation. The highlighted group of data points represents the calculations made by a single extension instruction*

Parallel Computations

The first optimisation step is to determine the number of data points that the bus can efficiently pass. For example, an extension instruction performing eight multiplies and additions (MACs) would reduce the number of inner loop iterations by a factor of eight. Since each pipelined extension instruction executes in effectively a single cycle, there should be approximately an 8X boost in overall performance. Note that if a particular data set does not divide evenly by, in this case eight, it can be extended with nulls/zeros.

The multiple data approach is illustrated in **Figure 2**, where the highlighted group of data points represents the calculations made by a single extension instruction. Each execution of the extension instruction multiplies eight data values by the appropriate coefficients and accumulates all the products. The resulting partial sum is saved to a local state variable, thereby eliminating the need to pass the partial sum back to the CPU and then back to the extension instruction again.

Performing eight MACs per extension instruction reduces the theoretical minimum number of cycles required to execute the example FIR filter down to 1941. Compared to a straight C implementation, this is a performance gain of 15X.

The optimal number of simultaneous computations is dependent upon the number of programmable resources available. Conservation of programmable resources is critical as these resources are shared between all of the various extension instructions the CPU currently has access to. Therefore, it is important to reuse resources whenever possible.

The efficiency of reuse can be illustrated through the use of two extension instructions FIR_MUL and FIR_MAC (see **Listing 2**). The first time the FIR filter is called, the partial sum state register is reset; this is handled by FIR_MUL. In the case of a 64-tap filter, the next seven subsequent iterations call FIR_MAC, which uses the existing partial sum. The primary difference between FIR_MUL and FIR_MAC is captured in the line of code "acc = FIR_MUL ? sum : se_int<32>(sum + acc)", which effectively resets the partial sum if the extension instruction is called via FIR_MUL and uses the partial sum if called via FIR_MAC.

Instead of doubling up the resources required for these two extension instructions, the same programmable resources are shared. The trade-off is the use of the conditional resource and the associated latency of resolving the conditional which, in this case, has no material impact on performance. As a consequence, more resources are available to implement other extension instructions or to further optimise this instruction.

More Of The Good Thing

Because of the flexible implementation possible with integrated programmable logic, extension instructions can be revised to improve performance without substantial redesign. In contrast, ASIC- and FPGA-based architectures require that developers completely re-design, tune and debug modified implementations. ASIC and FPGA design takes place in a separate and distinctly different development environment requiring hardware expertise and, often, handled by a second development team. Therefore, a repartitioning or modification to accelerated hardware is met with resistance and must be justified before results can be accurately evaluated through actual implementation.

When hardware is abstracted as software, the same compiler that generates application code also generates the configuration for the programmable logic. In this way, the compiler is able to efficiently manage resources and dependencies, maximising throughput. Additionally, since the hardware implementation is automatically generated by the compiler, only a single development team is required. Not only does this eliminate the need for a second design team, it frees developers to evaluate multiple implementations, without having to invest significant development hours creating hand-optimised implementations.

For example, the FIR filter can be further optimised by

Figure 3: Illustration of 4 x 4 block of data points

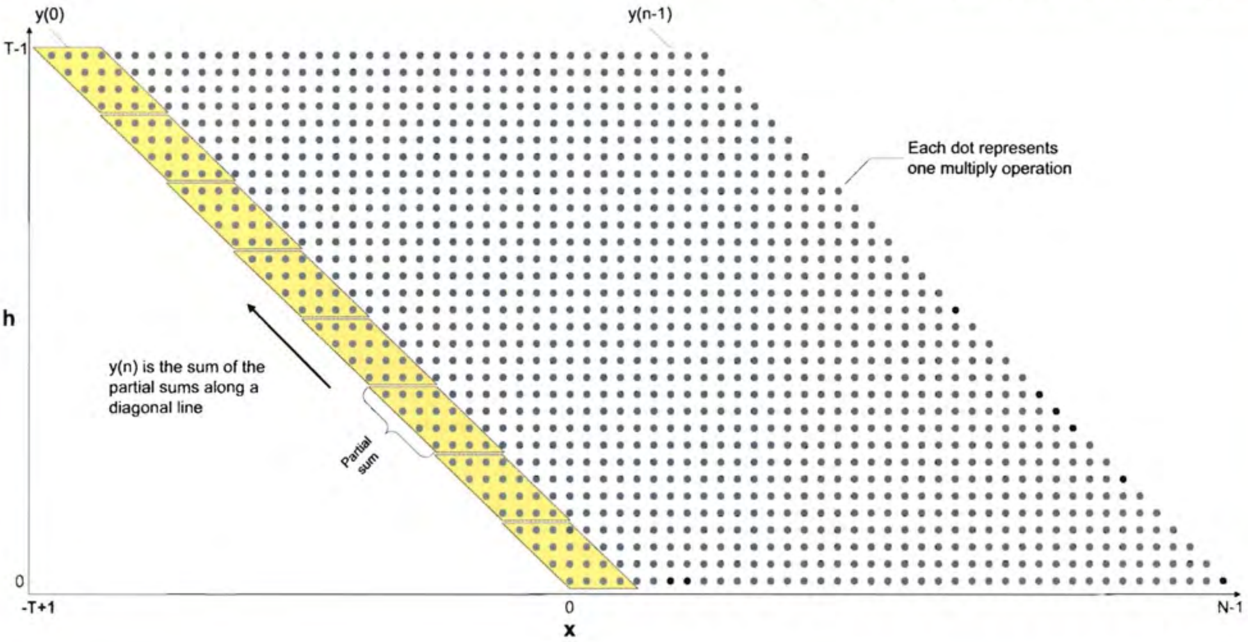
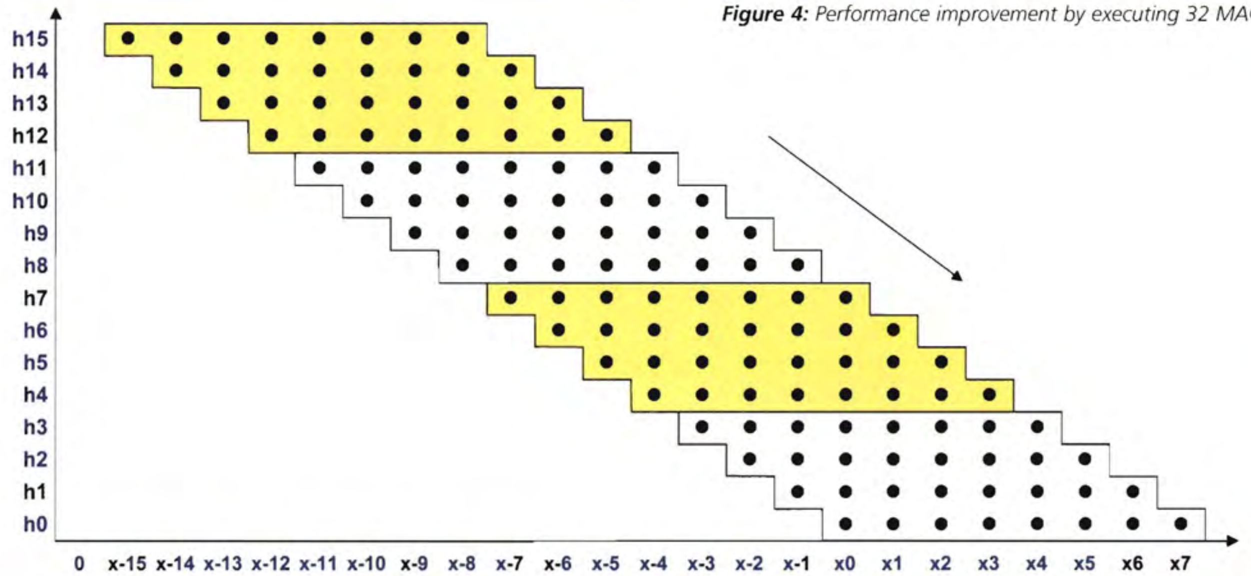


Figure 4: Performance improvement by executing 32 MACs



reducing the number of times the extension instruction must be invoked. Not only does this eliminate the headache of scheduling extension instructions, it also reduces the overall overhead associated with calling extension instructions.

Consider increasing performance by increasing the number of simultaneous MACs to 16 (**Figure 3** illustrates the 4 x 4 block of data points). Computing this block of data points requires only four coefficients and seven data points; compare this to 16 data points and 16 coefficients for the partial sum on a single diagonal line. This enables an efficient use of bus bandwidth as more computations can be made utilising less bandwidth. The primary tradeoff is that, now, four partial sums must be stored in state registers.

Moving to 16 MACs per extension instruction doubles performance, reducing the minimum number of cycles down to 981 for a 30X gain over an unaccelerated implementation. Further performance improvement is possible by executing 32 MACs (see **Figure 4**), which requires four coefficients, 11 data samples and eight partial sums. The theoretical minimum number of cycles for such an implementation is 501, approximately 58X more efficient than a straight C implementation.

Loop Optimisations

It is also possible to achieve substantial improvements through conventional loop optimisations. Consider, for example, the implementation of an FIR filter performing eight simultaneous computations – this example (see **Listing 3**) was chosen rather than the 32 simultaneous computations example to keep the inner loop code fairly simple, so as to better illustrate the optimisation techniques.

Source	Optimization	% of Cycles	# of Cycles	Performance Improvement over Straight C Code
fir0a	None	64.34	27230.60	–
fir8a	Separated inner loop into Extension Instruction	25.15	5065.00	>5x
fir8b	Shuffled Extension Instruction schedule	17.46	3189.00	>8x
fir8c	Manually unrolled loops	15.24	2711.40	>10x
fir16	Used 16 multipliers	6.96	1128	>24x
fir32	Used 32 multipliers	4.36	687	>39x

Table 1: *Performance results using an S5 software configurable processor to implement a 64-tap FIR filter with 80 data points, issue rate of 3 and an ISEF latency of 5*

```
void fir(short *X, short *H, short *Y, int N, int T)
{
    int n, t, acc;
    short *x, *h;
    /* Filter Input */
    for (n = 0; n < N; n++) {
        x = X;
        h = H;
        acc = (*x--) * (*h++);
        for(t = 1; t < T; t++) {
            acc += (*x--) * (*h++);
        }
        *Y = acc >> 14;
        X++;
        Y++;
    }
}
```

Listing1: *Straightforward C implementation of an FIR filter*

In this implementation, performance drops from 27,230 to 5065 cycles with no low-level assembly coding or significant modification to the structure of the original C source algorithm. However, there is inefficiency in the form of wasted cycles: after invoking the last FIR_MAC instruction for a given outer loop iteration, the processor must wait (the number of cycles is equal to the issue rate times the extension instruction latency) before results are available.

One way to recover wasted cycles is to begin computations for the next outer loop while waiting for the previous output. Since the number of processor cycles required to complete issuing of the extension instruction is greater than the number of cycles required to wait for the output, the CPU is guaranteed that, upon issuing the first extension instruction for the current samples, the output from previous samples will be available for use.

It is also possible to optimise between loop iterations. If the inner loop for a particular outer loop iteration is independent of the next or previous outer loop generation, it is possible to offset waiting for the result by issuing a new outer loop iteration. Consider that after the last FIR_MAC is issued for outer loop iteration 0, the CPU could begin the inner loop calculations for outer loop iteration 1, without waiting for outer loop iteration 0 to complete. In this implementation, the last FIR_MAC takes roughly 21 processor cycles before providing a result. By pipelining inner loop calculations in the outer loop, the number of processor cycles required for each iteration is reduced by 18. This drops the total number of cycles per call to 3189, down from 5065 (see **Listing 4**), for a further 8X improvement.

Another technique for improving performance is to manually unroll the inner loop. Because the inner loop is managed using a variable – the FIR macro is written for a

```
#include <stretch.h>

static se_sint<32> acc;

/* Performs 8 parallel MAC */
SE_FUNC void
firFunc(SE_INST FIR_MUL, SE_INST FIR_MAC, WR X, WR H, WR *Y)
{
    se_sint<16> x, h
    se_sint<32> sum ;
    int i ;

    sum = 0;

    for(i = 0; i < 128; i += 16) {
        h = H(i + 15, i);
        x = X(127-i, 112-i);
        sum += x * h ;
    }

    acc = FIR_MUL ? sum : se_sint<32>(sum + acc) ;

    *Y = acc >> 14 ;
}
```

Listing 2: *Illustration of the efficiency of reuse through the use of two extension instructions FIR_MUL and FIR_MAC*

```
#include "fir8.h"

#define       ST_DECR       1
#define       ST_INCR       0

void fir(short *X, short *H, short *Y, short N, short T)
{
  int n, t, t8;
  WR x, h, y;

  t8 = T/8;

  WRPUTINIT(ST_INCR, Y) ;

  for (n = 0; n < N; n++) {
      WRGET0INIT(ST_INCR, H) ;
      X++ ;
      WRGET1INIT(ST_DECR, X) ;

      WRGET0I( &h, 16 );
      WRGET1I( &x, 16);
      FIR_MUL(x, h, &y);

      for (t = 1; t < t8; t++) {
          WRGET0I(&h, 16);
          WRGET1I(&x, 16);
          FIR_MAC(x, h, &y);
      }

      WRPUTI(y, 2) ;
  }

  WRPUTFLUSH0() ;
  WRPUTFLUSH1() ;
}
```

Listing 3: Implementation of an FIR filter performing eight simultaneous computations

generic number of taps – the compiler cannot estimate the number of times the loop will be executed, so there will be conditionals within the inner loop which flush the processor pipeline, leading to processor stalling if the processor misses the cycle in which it can issue an extension instruction.

A 64-tap filter performing eight calculations per extension instruction needs to issue eight extension instructions per output; if the programmable resources are available, such a loop can be entirely unrolled. In addition, further optimisation is possible by loading registers well in advance of when they are needed to eliminate load penalties. Given that there are only 64 16-bit coefficients used by the FIR filter, these can all be preloaded and stored in state registers.

Implementing loop unrolling optimisations (see **Listing 5**) brings the total number of cycles down to 2711 per call, for an overall 10X improvement. Bringing all these techniques together using a 32-MAC extension instruction results in a function that executes in 687 cycles, over a 39x performance improvement over the original straight C code (see **Table 1**).

```
/* Include the Stretch Instruction Specific Header */
#include "fir8.h"
#define     ST_DECR     1       /* Decrement Indicator */
#define     ST_INCR     0       /* Increment Indicator */
/* define macro for the FIR ISEF instruction invocations */
#define     FIR(H, X, h, x, t8, y)          \
{                                           \
   int t8m1 = (t8)-1;                       \
                                            \
   WRGET0INIT(ST_INCR, (H)) ;               \
   (X)++ ;                                  \
   WRGET1INIT(ST_DECR, (X)) ;               \
                                            \
   WRGET0I( &(h), 8 * sizeof(short) ); \
   WRGET1I( &(x), 8 * sizeof(short) ); \
   FIR_MUL( (x), (h), &(y) );           \
                                            \
   for (t = 1; t < (t8m1); t++)         \
   {                                        \
      WRGET0I( &(h), 16 );              \
      WRGET1I( &(x), 16 );              \
      FIR_MAC( (x), (h), &(y) );        \
   }                                        \
   WRGET0I( &(h), 16 );                 \
   WRGET1I( &(x), 16 );                 \
   FIR_MAC( (x), (h), &(y) );           \
}
/*
* - FIR using 8 multipliers in ISEF
* - Loop optimized
*/
void fir(short *X, short *H, short *Y, short N, short T)
{
   int n, t, t8 ;
   WR x, h, y1, y2, y3, y4;
   t8 = T/8 ;
   WRPUTINIT(ST_INCR, Y) ;          /* init output stream */
   FIR (H, X, h, x, t8, y1) ;    /* x * h + y => y1 */
   /* loop ((N/2)-1) times */
   n = 0;
   do
   {
      FIR (H, X, h, x, t8, y2) ;  /* x * h + y => y2 */
      WRPUTI(y1, 2) ;               /* put (y1) result */
      FIR (H, X, h, x, t8, y1) ;  /* x * h + y => y1 */
      WRPUTI(y2, 2) ;               /* put (y2) result */
   } while ( ++n < ((N>>1)-1) );
   FIR (H, X, h, x, t8, y2) ;     /* x * h + y => y2 */
   WRPUTI(y1, 2) ;                /* put (y1) result */
   WRPUTI(y2, 2) ;                /* put (y2) result */
   WRPUTFLUSH0() ;                   /* flush output stream */
   WRPUTFLUSH1() ;                   /* flush output stream */
}
```

Listing 4: The total number of cycles per call drops to 3189, by pipelining inner loop calculations in the outer loop

Listing 5:
Implementing loop unrolling optimisations

```
/* Include the Stretch Instruction Specific Header */
#include "fir8.h"

#define      ST_DECR        1      /* Decrement Indicator */
#define      ST_INCR        0      /* Increment Indicator */
#define      FIR(h1, h2, h3, h4, h5, h6, h7, h8, x1, x2, y1, X)
{
    WRGET0I( &(h1), 8 * sizeof(short) );
    WRGET1I( &(x1), 16 );
    X++ ;
    WRGET0I( &(h2), 16 );
    WRGET1I( &(x2), 16 );
    FIR_MUL( (x1), (h1), &(y1) );

   WRGET0I( &(h3), 16 );
   WRGET1I( &(x1), 16 );
   FIR_MAC( (x2), (h2), &(y1) );
   WRGET0I( &(h4), 16 );
   WRGET1I( &(x2), 16 );
   FIR_MAC( (x1), (h3), &(y1) );
   WRGET0I( &(h5), 16 );
   WRGET1I( &(x1), 16 );
   FIR_MAC( (x2), (h4), &(y1) );
   WRGET0I( &(h6), 16 );
   WRGET1I( &(x2), 16 );
   FIR_MAC( (x1), (h5), &(y1) );
   WRGET0I( &(h7), 16 );
   WRGET1I( &(x1), 16 );
   FIR_MAC( (x2), (h6), &(y1) );
   WRGET0I( &(h8), 16 );
   WRGET1I( &(x2), 16 );
   FIR_MAC( (x1), (h7), &(y1) );
   WRGET1INIT(ST_DECR, X);
   FIR_MAC( (x2), (h8), &(y1) );
}
#define  FIR1(h1, h2, h3, h4, h5, h6, h7, h8, x1, x2, y1, y2, X) \
{
   WRGET1I( &(x1), 16 );
   FIR_MUL( (x1), (h1), &(y2) );
   WRGET1I( &(x1), 16 );
   FIR_MAC( (x1), (h2), &(y2) );
   WRGET1I( &(x1), 16 );
   FIR_MAC( (x1), (h3), &(y2) );
   WRGET1I( &(x1), 16 );
   FIR_MAC( (x1), (h4), &(y2) );
   WRGET1I( &(x1), 16 );
   X++ ;
   FIR_MAC( (x1), (h5), &(y2) );
   WRGET1I( &(x1), 16 );
   WRGET1I( &(x2), 16 );
   FIR_MAC( (x1), (h6), &(y2) );
   WRGET1I( &(x1), 16 );
   WRGET1INIT0(ST_DECR, X);
   FIR_MAC( (x2), (h7), &(y2) );
   WRGET1INIT1();
   WRPUTI(y1, 2);
   FIR_MAC( (x1), (h8), &(y2) );
}
#define FIR2(h1, h2, h3, h4, h5, h6, h7, h8, x1, x2, y1, y2, X)
{
   WRGET1I( &(x1), 16 );
   FIR_MUL( (x1), (h1), &(y1) );
   WRGET1I( &(x1), 16 );
   FIR_MAC( (x1), (h2), &(y1) );
   WRGET1I( &(x1), 16 );
   FIR_MAC( (x1), (h3), &(y1) );
   WRGET1I( &(x1), 16 );
   FIR_MAC( (x1), (h4), &(y1) );
   WRGET1I( &(x1), 16 );
   X++ ;
   FIR_MAC( (x1), (h5), &(y1) );
   WRGET1I( &(x1), 16 );
   WRGET1I( &(x2), 16 );
   FIR_MAC( (x1), (h6), &(y1) );
   WRGET1I( &(x1), 16 );
   WRGET1INIT0(ST_DECR, X) ;
   FIR_MAC( (x2), (h7), &(y1) );
   WRGET1INIT1();
   WRPUTI(y2, 2);
   FIR_MAC( (x1), (h8), &(y1) );
}
/*
 * - FIR using 8 multipliers in ISEF
 * - Loop optimized / Hand unrolled
 */
void fir(short *X, short *H, short *Y, short N, short T)
{
     int n, t, t8 ;
     WR  h1, h2, h3, h4, h5, h6, h7, h8 ;
     WR  x1, x2;
     WR  y1;
     WR  y2;
     // (these alternative "register" declarations make no difference:)
     //  register WR y1 SE_REG("wra1") ;
     //  register WR y2 SE_REG("wra2") ;

     WRPUTINIT(ST_INCR, Y);                       /* init output stream */

     WRGET0INIT(ST_INCR, H);                      /* init coefficient stream */
     X++ ;
     WRGET1INIT(ST_DECR, X);                      /* init input stream */

     /* compute Y[0] in y1 */
     FIR(h1, h2, h3, h4, h5, h6, h7, h8, x1, x2, y1, X) ;

     /* loop ((N/2)-1) times */
     for (n = 0; n < ((N>>1)-1); n++)
     {
```

```
/* FIR1 writes previous output (y1) and computes current output (y2) */
        FIR1(h1, h2, h3, h4, h5, h6, h7, h8, x1, x2, y1, y2, X) ;
/* FIR1 writes previous output (y2) and computes current output (y1) */
        FIR2(h1, h2, h3, h4, h5, h6, h7, h8, x1, x2, y1, y2, X) ;
    }
    /* compute Y[N-1] in y2 and write Y[N-2] from y1 */
    FIR1(h1, h2, h3, h4, h5, h6, h7, h8, x1, x2, y1, y2, X) ;
    WRPUTI(y2, 2) ;                              /* write U[N-1] */
    WRPUTFLUSH0() ;                                     /* flush output stream */
    WRPUTFLUSH1() ;                                     /* flush output stream */
}
```

By integrating programmable logic into an application processor and its pipeline, software configurable architectures are able to provide substantial hardware acceleration of computationally-intensive algorithms with little to no manual optimisation. By being able to design hardware as software, developers are able to avoid the complexities associated with partitioning an algorithm implementation between software and hardware. Because the complexities of the actual hardware implementation are handled by the compiler, developers are able to quickly and easily design complex algorithms and evaluate the efficiency of various implementations, in order to maximise performance and control cost.

CHALLENGING DEVELOPMENT ENVIRONMENT

Mike Lloyd, Managing Director of ML Electronics, discusses the challenges facing developers of electronic medical devices

The environment for creating medical electronic devices is an extremely challenging one. Devices need to undergo extensive regulatory approval processes, developers need to create perfect devices but at low cost; there are the matters of obsolescence, EMC and placement of components, restraining wiring and isolation for patient safety. On top of it all, space in the operating theatres and A&E is also at a premium. How can an engineer navigate around all these problems?

As a way of investigating some of these challenges let's consider a hypothetical device which has the following key elements (**Figure 1**):

It has to perform some kind of patient measurement using a disposable probe connected to the patient. It incorporates power actuators to stimulate the patient and a user interface to display to the nurse. It needs a reasonable degree of instrumentation and signal processing, some hardware interlocks and is powered by a mains power supply.

These blocks are very typical of most medical systems, so how can we address the technical solution to some of these blocks as individual problems?

In our example, a designer would immediately note that one would have to meet the requirements of ISO 60601. Typical design risk areas in this standard for this application would be an isolation barrier (6mm creepage) for safety between live mains (230V) and the patient side (probe connected to the patient). Also, any wiring would have to be physically tied down to prevent a loose wire touching any metal part of the patient side of the electronics.

EMC impacts on the patient leakage currents, which have to be less than several microamps. One could not use large EMC filters, as this would pass a large earth current, greater than the allowed amount, through the earth and, subsequently, through the patient. It is, therefore, essential to design a product that has extremely low EMC emissions by design (see later).

There is a need for intelligent control both on the patient side, to analyse the signal generated from the probe and also on the mains side, to ensure that the power is sequenced correctly and there is no inrush etc.

Exploring each of these three items would be a useful insight into medical design.

The first two points can be addressed simultaneously. In this design, let us imagine that the greater cause of the EMC is generated by the switched mode power supply that provides the power for the actuators, the instrumentation and control circuits. In this case we will assume for cost and obsolescence reasons that the decision has been made to design our own power supply. This now gives the designer the opportunity to control the EMC and the purchase of multi-source components.

By carefully accessing the characteristics of many power topologies, with the object of keeping the EMC to the required minimum, a semi-resonant phase shifted full bridge circuit would be used. This has the benefit of being easy to drive; there are control chips available to drive the bridge and the EMC generated by the switching is very low. Taking this approach, the designer uses one design to accomplish many different design objectives. The phase shifted full bridge (see Figure 1) is ideal in this situation as it uses a full bridge with two square waves applied to the two halves with a phase delay. If the square waves are in phase there is no output, if the two phases are 180-degree out, then the maximum output is delivered. The interesting point is that each half bridge sees only a 50% duty cycle, so there is plenty of time to resonate the edges of the switching waveform. This would give rise to very few EMC harmonics being generated and, hence, a very small EMC filter would be required. With skill, it is possible to create the resonant elements using the parasitic leakage inductance of the transformer and the switching devices. The high primary to secondary isolation needed in this application is ideal in creating the parasitic inductance in the transformer.

The third technical challenge benefits from the use of two embedded controllers with an optical interface across the isolation barrier. The patient-side unit can typically be a TMS320 DSP device with lots of efficient processing power and the primary device can be a PIC or MSP430 style device. By carefully choosing the hardware around these devices, with as much of the safety critical monitoring done in hardware, it is possible in many cases to reduce the level of risk (level of concern).

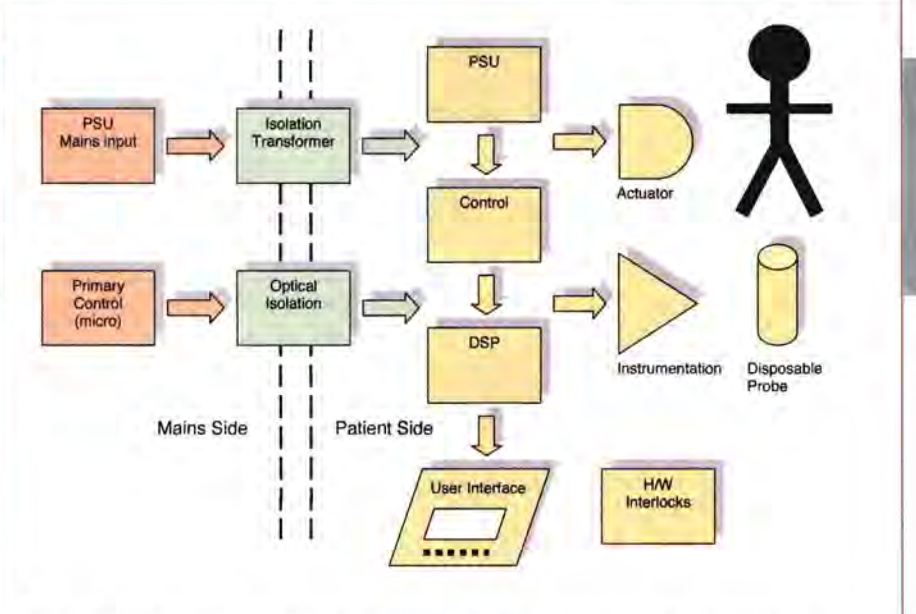


Figure 1: *Block diagram of a hypothetical medical product showing safety isolation*

The Development Process

In many medical designs the technical design of the electronics is fairly straightforward compared to the regulatory understanding that is needed. In addition, there are quality requirements including verification and validation of test plans and design history files that are required. In most situations all these aspects would be wrapped up in a 'Quality Plan', which would detail the test plans and compliance.

The design process is absolutely key to medical design (and any other design) and a formalised approach actually aids the creation of simple and concise solutions that are part of an elegant design. **Figure 2** shows an outline of the FDA and ISO design processes. Alongside these is an outline of a typical design process that covers these requirements.

The actual steps through the design process may differ according to whether the business is technology led or market led but, typically, this would consist of the following stages:

- Initial project set up to assign the team and kick start the project. The team needs to understand with clarity and focus the objectives in hand to prevent charging forward with typical engineering enthusiasm. These points go beyond the technical requirements and cover commercial, regulatory and quality implications. In addition, there will be roles and responsibilities assigned. In a typical successful company, key people would be selected for the team that possess specific character types as shown up by tests.
- The first development stage of a project should focus on how feasible the intended final product is. This is mainly about seeking answers to standard questions. For example, is it technically possible? Is it commercially viable? What are the risk areas and what options are available to reduce these risks? Which specific medical regulatory requirements need to be complied with?

During this stage of the development it is necessary to create a draft specification or basic requirements list, which allows good communications throughout all departments of the business. Priority should then be given to these using a weighting approach to define which are 'must haves' and which are 'wish list' items. This prevents too much work being conducted on unnecessary items.

From this the engineering team can create conceptual designs and assess what parts of the project are similar to previous projects. This provides two outcomes. One is a clear focus on the re-use of existing design modules and another is a clear understanding of the areas that are new. Listing these formally allows an easier review of design challenges and also creates the basis for the medical, commercial and technical risk assessment.

The output of this stage is theoretically based. It would normally be in the form of a report outlining the points raised for investigation; the options looked at along with the pros and cons of each option. Finally, it should conclude with recommended choices backed up with reasoning that are assessed during an Initial Design Review. This review provides an opportunity for all departments to sign off against decisions made and ensures that key design drivers, quality and regulatory aspects have been considered.

Figure 2: *Design process flowcharts*

The second stage of development would review risks identified by bench testing certain points in isolation. The intention here is to fully prove design concepts and gain confidence in the design as a whole, before committing to full system prototypes. This process may happen several times with the involvement of end users and marketing to explore how the technology/usability balance can be addressed. At this stage the project may be launched formally.

Completion of this stage is marked by another design review. At this stage it would be reasonable to have a very accurate statement of requirements or design input. This document would be signed off along with the quality plan and (essential for medical products) any changes to the design input would have to be rigorously recorded with issue control. Typically, this would happen within an ISO 9001 – 2000 or EN 13485 quality environment.

The third stage takes all the lessons learnt and confidence gained and brings the design together for the first time as a complete system. As with any engineering prototype, it is likely to need "engineering surgery" to correct mistakes and incorporate performance improvements. As such, it is usually a good idea to plan this as a non-deliverable item.

The third stage is completed with a Preliminary Design Review that includes the stakeholders and demonstrates the engineering prototype to assess operation and performance achieved so far. Is it going in the right direction? Have certain points been correctly interpreted and implemented?

The fourth stage of development is to typically create representative prototypes which should look like they are intended to as finished product.

The deliverable prototypes should be of a standard that is high enough and complete enough to allow any preliminary regulatory testing to take place. Full verification and validation needs to be conducted and it is the exhaustive testing that will take the bulk of the energy during this stage. Any anomalies found are discussed during a Critical Design Review. This is probably the most important review throughout the whole development process. The next units to be built are to be of pre-production standard, so any points, no matter how seemingly trivial, need to be carefully considered and dealt with.

From the perspective of the electronics team, the fifth stage for the development team is to run a production pilot run. The outcome here is to supply the units that can be used as final product. The production team is testing the build ease and documentation set to assess production release readiness before the final commitment to larger volume production. Final verification and validation generally takes place in parallel to this process before the final sign off is approved.

A final Post Project Review will look back at the whole project to assess what went well and what could have been done better. Post Project Reviews ought to be brought out during the very early stages of new projects as a means for continued improvement.

Need to Understand the Challenges

Whilst developing any product can prove a challenge, this article has shown some of the challenges that developers of medical devices often find themselves facing. The regulatory nature of the industry places additional pressure on designers to meet increasingly tight specifications. In the context of electronics this means designers need to be highly aware of these regulations and how an electronics design created with these in mind will make a device's approval process easier. As the industry moves towards a more collaborative development approach, device manufacturing companies need to be seeking development partners that have this understanding of the pressures of the industry and use design processes that cater for these.

The Medical Innovation Forum will take place at Olympia in London on 26th of October. Electronics World readers will receive a £100 discount of their participation fee. Please contact readeroffer@medical-innovation.net or see medical-innovation.net for more information.

UKDL COLUMN

Colourful DIFFERENCES

By Chris Williams, UKDL

There are two main ways of making colour in electronic displays: spatial colour and field sequential colour (see drawing below).

Spatial colour displays are the types that are seen in LCD laptop and desktop screens, and LCD and plasma TVs. To create an image, each display pixel is built up from at least three sub-pixels, shown here as 1 x blue, 1 x green and 1 x red. To create a colour pixel, each sub-pixel must be turned on for a varying amount of time, since the colour the eye sees will depend on how much red, green and blue light is mixed together at that pixel position.

The top three sub-pixels on the left hand side (see drawing) are on, so the eye will see (blue + green + red) light, which will be interpreted by the brain as 'white'. Similarly, in the middle three pixels on the left hand side, only the green is on, so the eye will see green at that pixel position; whilst in the lower three, the red and green are on so the eye will see yellow.

Note that with (at least) three pixels required to create a pixel group, the actual display resolution, in terms of number of switchable elements is at least 3 x the perceived resolution in one dimension. The XGA resolution screen on your laptop, with 1024 x 768 pixels, actually has (RGB) x 1024 x 768, i.e. it has 3072 x 768 switchable and controllable elements to create the image that we watch.

If the percentage of time for which each sub-pixel is switched on in a frame of information is varied, then grey scales can be implemented, with a resultant huge increase in the number of colours that can be shown on the screen. If we have 8-bit grey scale per colour, then we have 28 shades of grey for each colour – 256 shades for red, green and blue. The mathematical computation for number of possible colours combinations that can be shown on the screen will be 256 x 256 x 256 = 16.7 million! Absolute rubbish, of course – the screen technology is nowhere near good enough to accurately represent each of the grey scales of the three colours to properly generate so many unique colours, but it does make for great PR and it looks good in adverts.

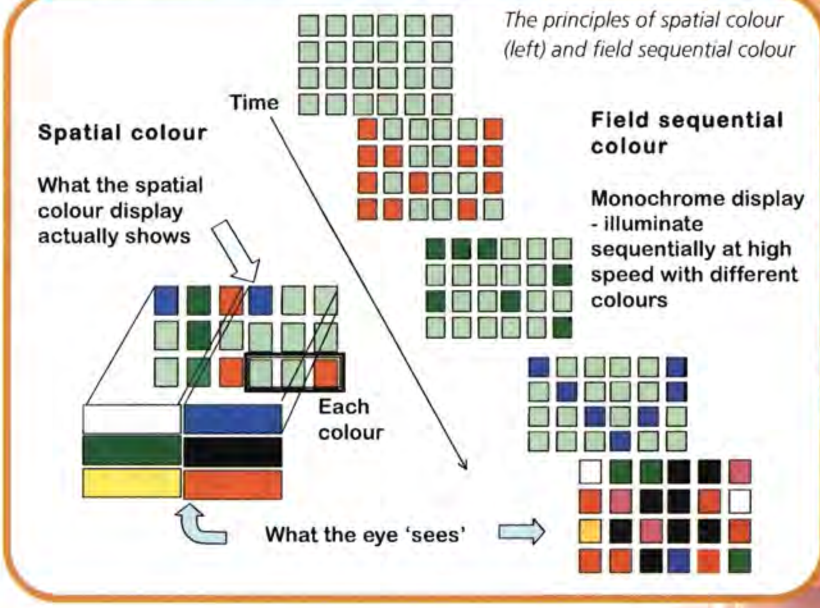
Field sequential colour is used in every one of the projection display systems based on the Texas Instruments DLP projector chip, and on various LCoS chips. It is also being used in small quantities in some 'direct view' displays – this display being one where the image seen is the same size as the display glass that creates it. In the projection system, the display glass is very much smaller than the final magnified image that is seen after it has passed through the projection optics.

In field sequential colour, a monochrome light modulator has sequential coloured lights shone onto it (or through it, in the case of transmissive elements), such that each coloured sub-frame forms part of a complete image. If the sequence is arranged such that multiple sub-frames are transmitted for each colour to allow grey scales to be created, then we also create variable amounts of red, green and grey at each position that are then seen by the eye when we view the image that is being written. The eye, being effectively an analogue device, will subconsciously integrate these different colour sub-frames and we will see variable colours at each pixel position.

The benefit of field sequential colour, if we can implement it in a direct view display, is that we only have one pixel on the display per pixel position that we see, so either we need 1/3rd as many pixels on a display as we do with spatial colour, or we could show 3 x as much information in the same footprint. The downside is that we now need a display that can update itself at least three times as fast as a display used in a spatial colour display, and the data rate that we need to supply information to the display system increases.

Which one will win: spatial or field sequential colour? There is room for both in the marketplace, but spatial colour has the biggest chunk of it by far, at present. It all comes down to the cost of manufacture and profit margins, and at the moment, spatial colour is easier and cheaper to implement as a system, but this may change over time.

Chris Williams is Network Director at UK Displays & Lighting KTN (Knowledge Transfer Network)



The principles of spatial colour (left) and field sequential colour

Living with RoHS – the big questions

Q: I've heard people are having problems with lead-free soldering of fine pitch components. Apparently, it's leading to tin whiskers? I thought this was rare.

A: Tin whiskers are still fairly rare but a number of cases have cropped up recently. Tin whiskers initially weren't that well understood. Even a year ago, "whisker resistant" tin coatings were not readily available. In most cases where there have been problems, companies have been the victims of changing to lead-free too early, before R&D was complete. The recently accepted exemption allowing tin/lead coatings on fine pitch components will help resolve concerns to some extent, but it is impossible to guarantee that incidents of tin whiskers will not occur. The best that can be done is to follow the whisker mitigation advice published by iNEMI:
http://thor.inemi.org/webdownload/projects/ese/tin_whiskers/User_Group_mitigation_May05.pdf

Q: Are evaluation boards in or out of the scope of RoHS and WEEE?

A: There has been a lot of discussion about this with many distributors and manufacturers surprised about the ruling on some evaluation boards. The National Weights and Measures Laboratory has stated that if they are a finished product they are within scope. However, their status depends on their function. If this is to write software then they should be regarded as Category 3 (within scope), but if their function is designing equipment and they have no IT function, then they are not in the 10 WEEE categories. There will be boards that are somewhere between these two extremes; deciding on their status is very difficult. My advice with products where the status is not clear is always work towards compliance, because the rules are still being decided and the authorities will eventually want to include more rather than less equipment in scope.

Q: Do you know when the Category 8/9 report is due?

A: A report was submitted to the EC in early August and this is now under review. I expect to see the final findings published on their website, hopefully, by October. Any implementation is, however, unlikely before 2010.

Q: What if the equipment I supply is a component of a larger infrastructure. Does it fall under RoHS then?

A: Much of the equipment in a large infrastructure, like an airport or railway station, is often interconnected and serves no function as separate items. The "product" is, therefore, the entire system. It would be reasonable to argue that, as the entire system's main function does not match any of the 10 WEEE categories, it is outside scope. However, in reality, the opinions of Member States will vary. Some will accept that these are excluded; others will insist that they are included. In some cases, it will depend on the equipment design and what is sold to the end-user. Equipment that is designed so that it could be used as a freestanding product may be in scope, whereas if it can be used only as part of the system, then it may be excluded. There is little logic with WEEE and RoHS and a situation could occur where individual items of equipment sold to end users will be included if they are in one of the categories. But, if the entire system is sold and the system does not match the categories, this could be excluded.

Q: Are power supplies covered by WEEE and RoHS?

A: There are still so many grey areas when it comes to exemptions. Power supplies are a big one. As finished products, these do not fit into any of the 10 WEEE categories, however, most are used as "part of" something else. A power supply module within a computer would have to comply with RoHS as it is a component in a Category 3 product. However, a bench power supply is probably excluded.

Gary Nevison is chairman of the AFDEC RoHS team, board director at Electronics Yorkshire and head of product market strategy at Farnell InOne. As such he is our industry expert who will try and answer any questions that you might have relating to the issues of RoHS and WEEE. Your questions will be published together with Gary's answers in the following issues of Electronics World. Please email your questions to EWeditor@nexusmedia.com, marking them as RoHS or WEEE.

Book Review

Practical Process Control for Engineers and Technicians
Wolfgang Altman
Wiley

I looked forward to receiving a copy of this book but what a disappointment. It became obvious after reading a few paragraphs that the work was no more than a set of course notes presented in a book form. The chapters and paragraphs are numbered in an "outline" format, which is a useful feature for course notes but, as the precedence of outline numbering sometimes lost its way, it tended – on occasions – to be confusing.

The book preface indicates that process control software is used in the course and is available by visiting IDC Technologies's website. I tried going on to this website, but could not find any reference to the software. I finally found that the name of the software file to download had no relationship with the book title.

The tome is divided into 14 chapters, 13 appendices and several working examples, each having a top level outline number.

Chapter 1 introduces various definitions and types of process control and includes process dynamics and time constants, basic definitions and terms used. The types and modes of operation of available control systems are also described. There is an introduction to closed loop controllers and process gain calculations for proportional, integral and derivative control modes, and an introduction to cascade control. This is a useful chapter as it defines the terminology of process control engineering.

Chapter 2 covers process measurement and transducers. It starts with a definition of transducers and sensors, followed by a listing of commonly measured variables. The common characteristics of several transducers are described with information on sensor dynamics and how to select these devices. There follows a description of temperature sensors, pressure transmitters, flow meters and level transmitters. Instrumentation and transducer selection considerations are discussed. The paragraph concludes with an introduction to the "Smart Transmitter".

Chapter 3 describes the basic principles of control valves and actuators, with an overview of eight of the most basic types together with their gain, distortion and range characteristics. The chapter concludes with a discussion on control valve actuators and "positioners" with a description of some mathematics involved.

Chapter 4 deals with the fundamentals of control systems and their stability. Chapter 5, a discussion on control modes in closed loops, is followed by a chapter on digital control principles. Chapter 7 describes real and ideal PID controllers and Chapter 8 deals with the tuning of PID controllers in both open and closed loop control systems.

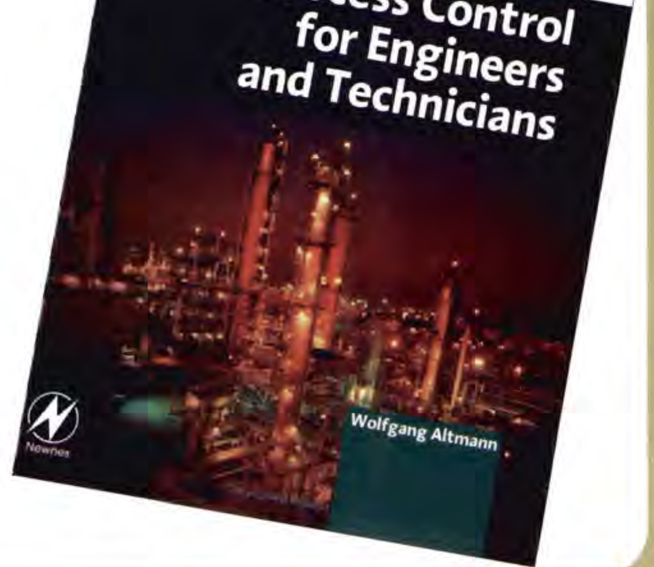
Chapter 9 describes controller output modes, operating equations and cascade control, and goes into some detail on controller output but, unfortunately, assumes that the reader is listening to the course presenter and that the software is up and running. Chapter 10 – concepts and applications of feed-forward control – is followed by a chapter on combined feedback and feed-forward control. Both of which are brief and not very useful.

Chapter 12 is another brief chapter discussing long process dead-time in closed loop control and the Smith Predictor. Chapter 13 gives a very basic introduction into the principles of fuzzy logic and neural networks are mentioned in passing. Chapter 14 gives some details on self-tuning intelligent control, whilst statistical process control is another chapter where the presence of the course lecturer is assumed. It goes into some depth but is hard to follow.

There's a set of Appendices, which deal mainly with how to set up, configure and run the software. The book concludes by providing a set of fifteen exercises illustrating and demonstrating the various control functions mentioned in it. The advertised software is used throughout. It is programmable by writing an external "script" file; each of the examples has its own script file.

Except for the definition of process control terminology and some detail on the various transducers available, this book has little to recommend it, except perhaps for someone who is expecting to attend the course, but even then not for the asking price posted on the website.

Michael B. Button



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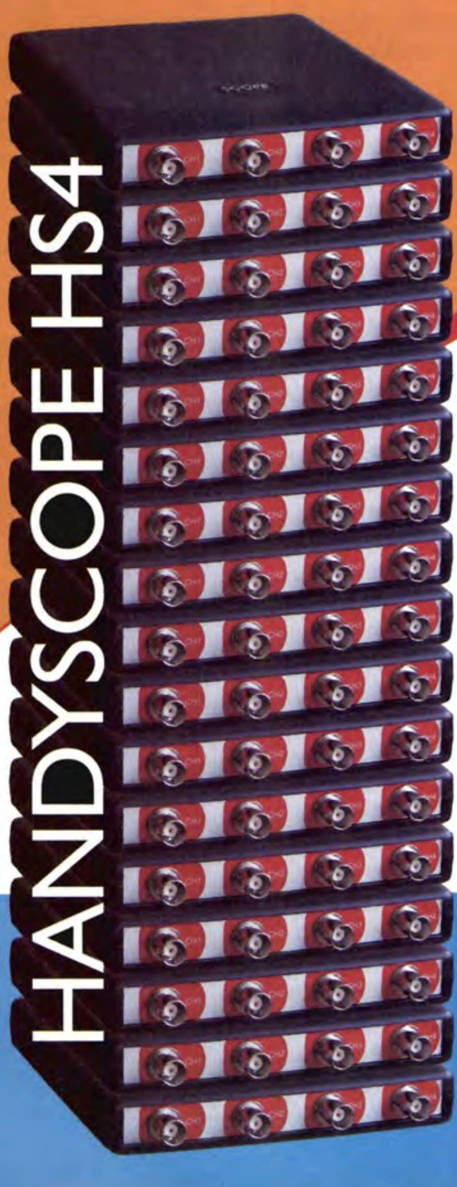

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- Auto disk function up to 1000 files
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- Auto trigger level and hysteresis setting
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Temperature-Stabilised, Constant-Current Source

Development of a constent-current source is not too heavy a problem. Engineers can use special ICs, operational amplifiers or voltage regulator ICs, such as LM317 (National Semiconductor, Motorola, Fairchild Semiconductor etc), which can be configured as a current regulator ("*LM317 Three-Terminal Adjustable Positive Voltage Regulator*", Motorola, data sheet in PDF)

It is suitable, but it will not be cheap or easy, because, for example, you don't have shutdown in the current regulator, which would be realised with the voltage regulator ICs – you will need additional electronic parts for it. This design solution will have some output residual voltage equal to the IC's internal reference voltage and, as such, residual current too.

An optimal solution is the well-known and old but modified one-transistor circuit (see **Figure 1**). However, it will need to be modified to reach our goal. We can use a Light Emission Diode (LED) as a reference voltage source.

This will allow stability, as the LED works as a voltage-reference diode with a low tolerance (see **Table 1**). This means that we will have a good thermal stability, as the temperature coefficient of the LED's voltage is a very close approximation to the transistor and has the same polarity.

Note that the temperature coefficient of the Zener diode voltage is a function of forward current. Also, the semiconductor junction of this device is a noise generator. Therefore, using an LED as the reference-voltage source will offer the simplest low-noise, temperature-stabilised, constant-current source, compared to that of the Zener diode. Effectively, this allows the simple turn-on of the current source, with the added bonus of the visual signal (see **Figure 2**).

However, what can be easier? The current of this current source can be calculated with: $I=(V_F - V_{EBO})/Re$ where, V_F is the LED forward voltage and V_{EBO} is the emitter-base voltage.
Hence, the current is approximately:
$I=(2-0.68)/Re=1.32/Re$
$V_{EBO} \approx 0.68$ V for usually used NPN general-purpose transistors.
$V_F \approx 2.0$ V for usually used red or green LED (see Table 1 below).

Table 1

Forward Current	Forward Voltage, V (experimental determination)			
mA	Red min	Red max	Green min	Green max
2.00	1.86	1.87	1.88	1.89
5.00	1.92	1.93	1.95	1.96
10.00	2.01	2.02	2.03	2.04

The necessary fine-tuning of the current can be performed by a change of value of the resistor Re.

The first time I used this temperature-stabilised, constant-current source as a collector load for the first transistor in a low-noise microcurrent amplifier (I needed a constant collector current 84μA in a wide range of operating ambient temperatures). I changed the high-resistance load and had a nice result (see **Figure 3**).

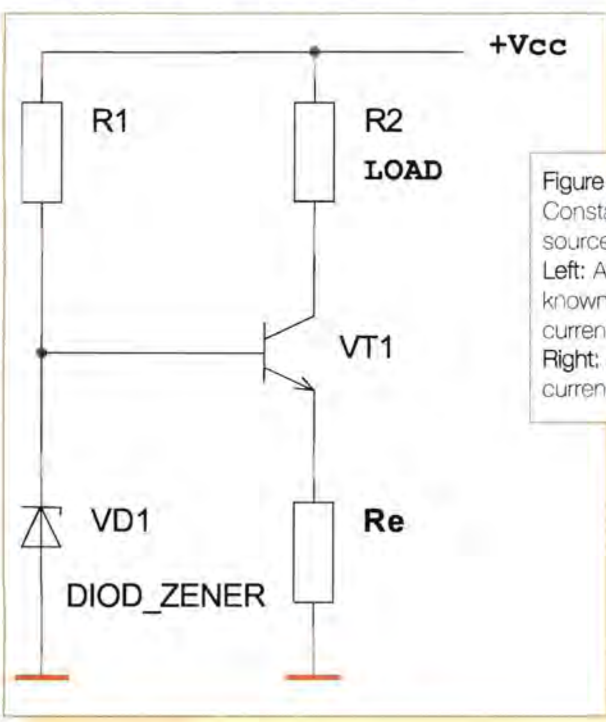
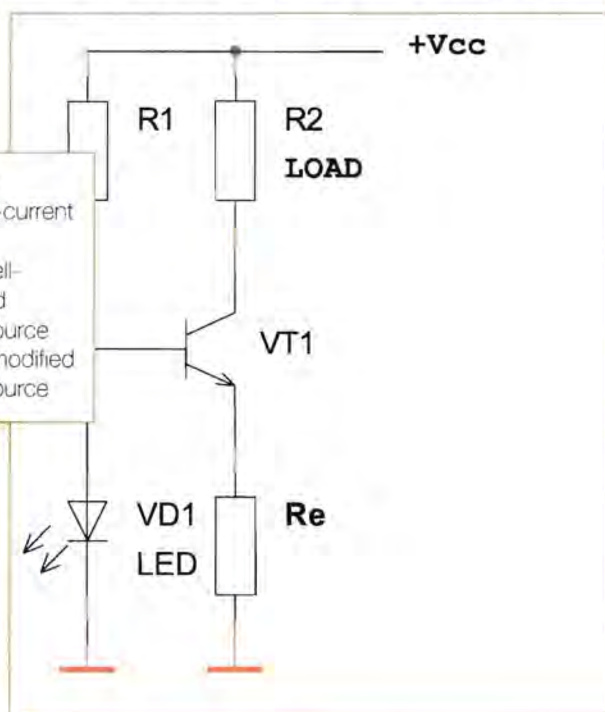


Figure 1: Constant-current source
Left: A well-known old current source
Right: A modified current source



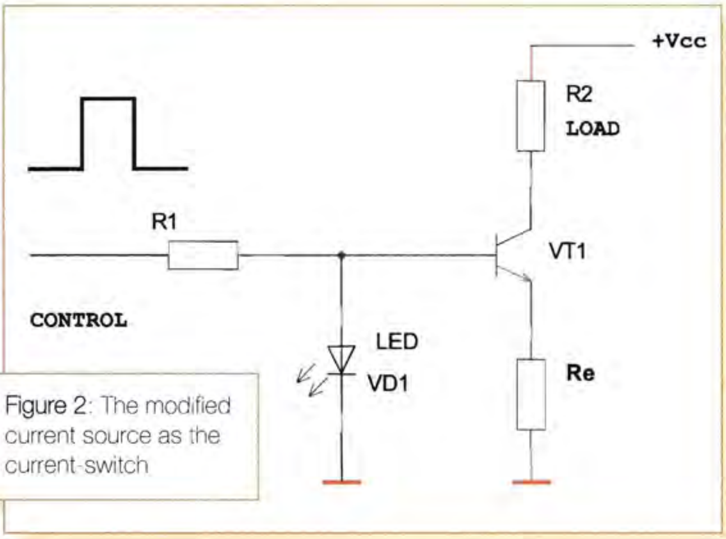


Figure 2: The modified current source as the current-switch

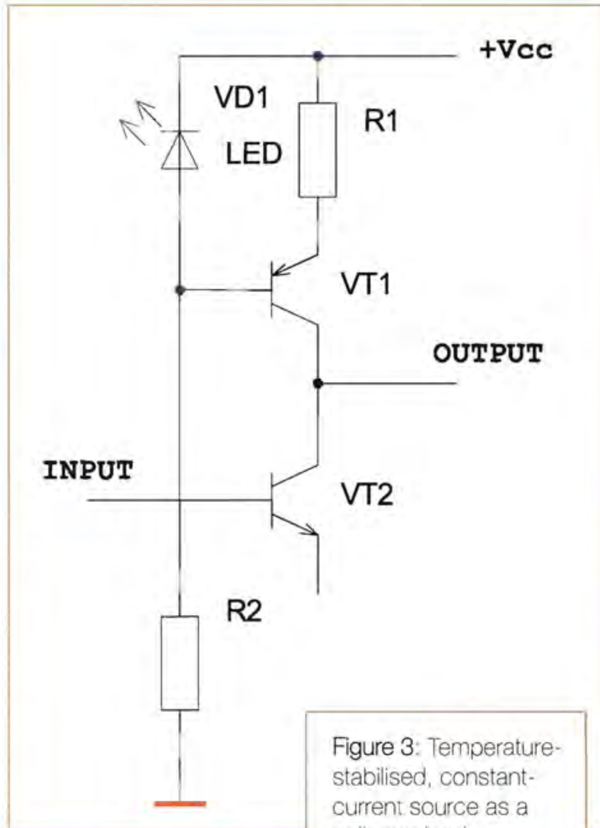


Figure 3: Temperature-stabilised, constant-current source as a collector load

I had a wider dynamic range and a better signal-to-noise ratio (up to 60dB under input signal 0.24mV).

Now, I use this simple circuit in IR-flash as background lighting, where a constant IR-flow is needed (see Figure 4).

The capacitor C1 is charged by a low current through resistor R1 (this can be a boost-converter or an additional current source). C1 gives its energy (as high current) via the temperature-stabilised, constant-current source to an infrared emitting diode VD2. So, the power supply unit (a battery) supplies the low current to C1 and temperature-stabilised, constant-current source supplies a constant, high current to VD2 and provides a constant IR flow.

R4=0 it is used as a "fuse" only. The diode VD1 flashes when the IR flash is flashing, too.

The solution has some disadvantages, naturally. You will need some additional voltage for the proper operation of this simple constant-current source. The minimum operation voltage is 0.8V. You will also need to check the power dissipation of the transistor.

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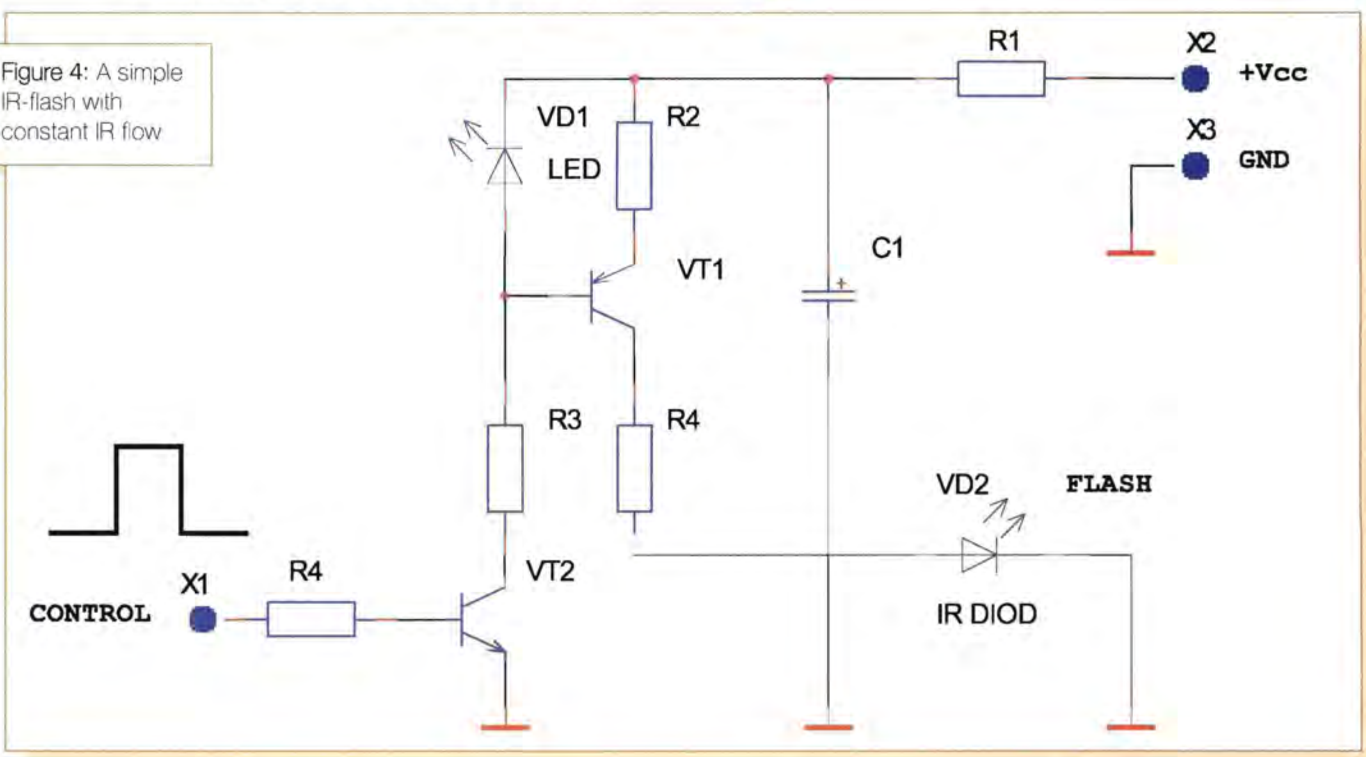


Figure 4: A simple IR-flash with constant IR flow

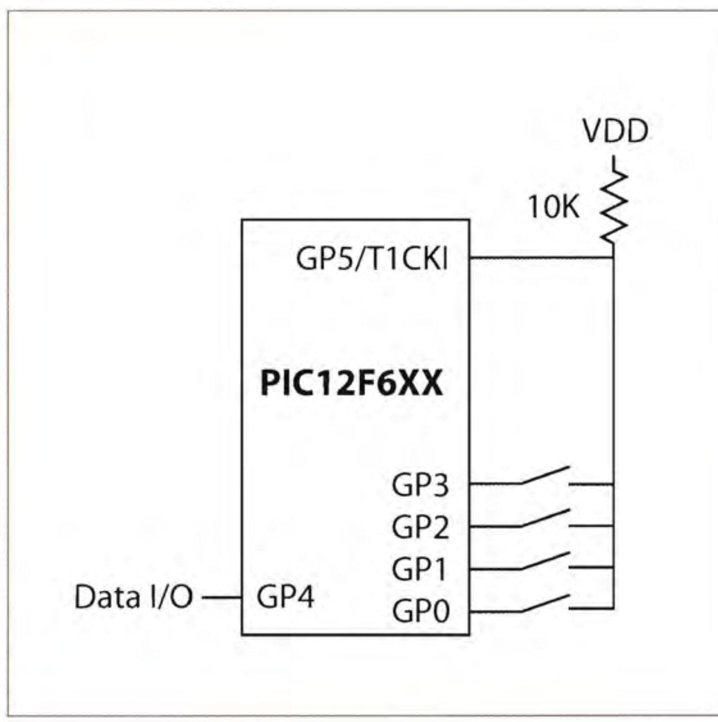
8-pin FLASH PICmicro Microcontrollers

TIP 1: READING DIP SWITCHES

The input of a timer can be used to test which switch(s) is closed. The input of Timer 1 is held high with a pull-up resistor. Sequentially, each switch I/O is set to input and Timer 1 is checked for an increment indicating the switch is closed.

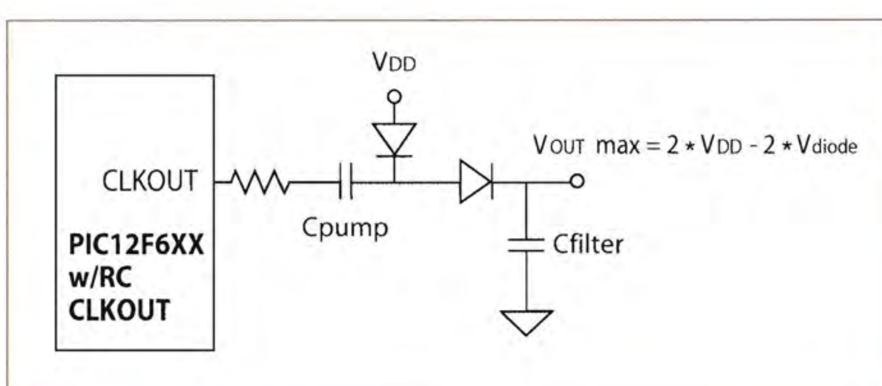
Each bit in the DP register represents its corresponding switch position. By setting Timer 1 to FFFFh and enabling its interrupt, an increment will cause a rollover and generate an interrupt. This will simplify the software by eliminating the bit test on the TMR1L register. Sequentially set each GPIO to an input and test for TMR1 increment (or 0 if standard I/O pin is used).

```
        movlw   b'11111111'
        movwf   TRISIO
        movwf   DIP
        movlw   b'00000111'
        movwf   T1CON
        movlw   b'11111110'
        movwf   Mask
        clrf    GPIO
LOOP
        clrf    TMR1L
        movf    Mask,W
        movwf   TRISIO
        btfsc   TMR1L,0
        andwf   DIP,F
        bsf     STATUS,C
        rlf     Mask,F
        btfsc   Mask,4
        goto    Loop
        retlw   0
```

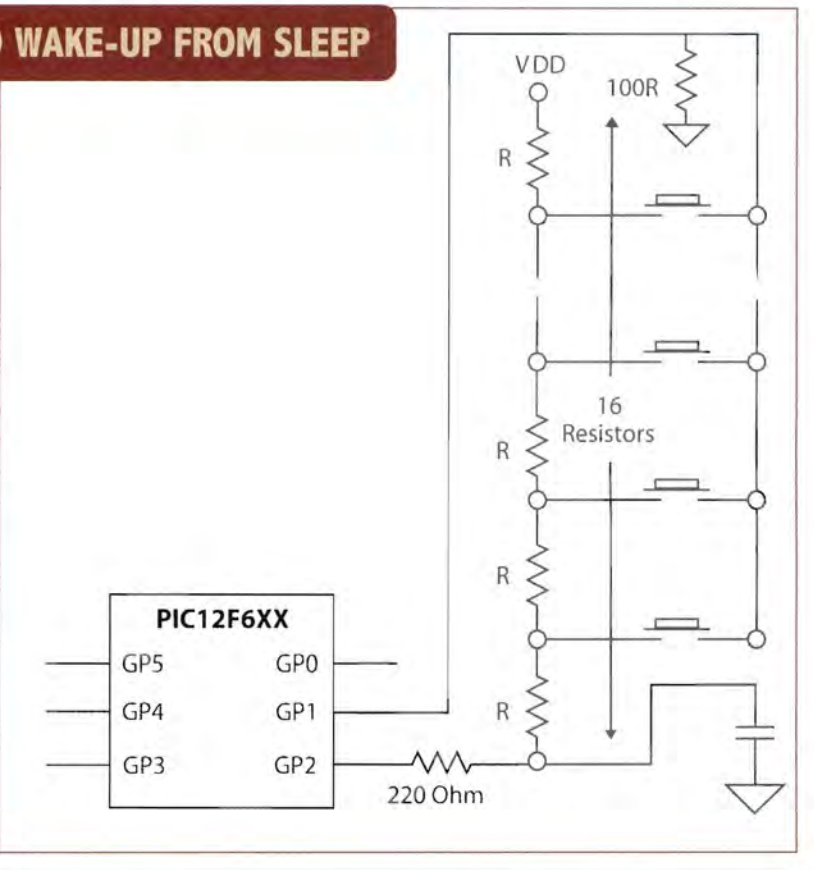


TIP 2: GENERATING HIGH VOLTAGES

Voltages greater than VDD can be generated using a toggling I/O. PIC MCUs CLKOUT/OSC2 pin toggles at one quarter the frequency of OSC1 when in external RC oscillator mode. When OSC2 is low, the VDD diode is forward biased and conducts current, thereby charging C_{pump}. After OSC2 is high, the other diode is forward biased, moving the charge to C_{filter}. The result is a charge equal to twice the VDD minus two diode drops. This can be used with a PWM, a toggling I/O or other toggling pin.



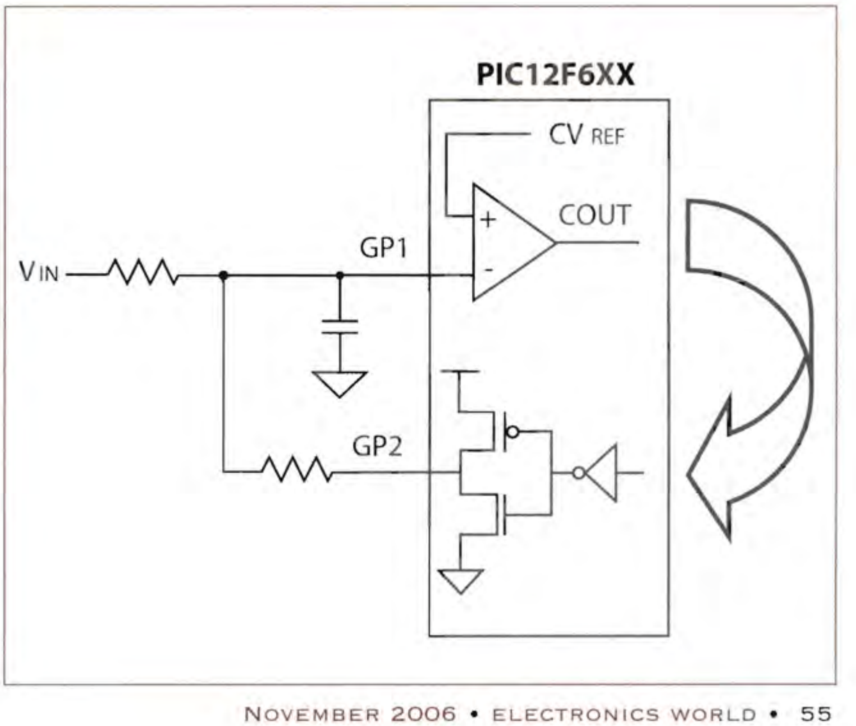
TiP 3: SCANNING MANY KEYS AND WAKE-UP FROM SLEEP



An additional I/O can be added to wake the part when a button is pressed. Prior to sleep, configure GP1 as an input with interrupt-on-change enabled and GP2 to output high. The pull-down resistor holds GP1 low until a button is pressed. GP1 is then pulled high via GP2 and VDD generating an interrupt. After wake-up, GP2 is configured to output low to discharge the capacitor through the 220 Ohm resistor. GP1 is set to output high and GP2 is set to an input to measure the capacitor charge time.

- GP1 pin connected to key common
- Enable wake-up on port change
- Set GP1 as input and GP2 high prior to sleep
- If key is pressed the PIC MCU wakes up, GP2 must be set low to discharge capacitor
- Set GP1 high upon wake-up to scan keystroke

TiP 4: DELTA SIGMA CONVERTER



The charge on the capacitor on GP1 is maintained about equal to the CVref by the MCU monitoring COUT and switching GP2 from input mode or output low appropriately. A timer is used to sample the COUT bit on a periodic basis. Each time GP2 is driven low, a counter is incremented. This counter value corresponds to the input voltage.

To minimise the affects of external component tolerances, temperature, etc, the circuit can be calibrated. Apply a known voltage to the input and allow the microcontroller to count samples until the expected result is calculated. By taking the same number of samples for subsequent measurements, they become calibrated measurements.

1. GP1 average voltage = CVref
2. Time base as sampling rate
3. At the end of each time base period:
   - If GP1 > CVref, then GP2 output low
   - If GP1 < CVref, then GP2 output high
4. Accumulate the GP2 lows over many samples
5. Number of samples determines resolution.

WIN A Microchip MPLAB ICD 2

Electronics World is offering its readers the chance to win an all-in-one, low-cost In-Circuit Debugger/ Programmer for Flash PICmicros

Microchip's MPLAB ICD 2 is an in-circuit debugger and programmer for their popular PICmicro micro-controllers. The PC based MPLAB ICD 2 supports Microchip's PIC16F and PIC18F Flash microcontrollers and dsPIC digital signal controllers. As new devices become available, users will be able to download new software code into the MPLAB ICD 2, at no cost, creating a highly adaptable tool that eliminates the expense of daughter board upgrades. The debugger supports real-time viewing of variables and registers. A single break point can be set and memory read/writes can also be accomplished. Additionally, the MPLAB ICD 2 can be used to program or reprogram the microcontroller on the product board. Other features include built-in over-voltage and short circuit monitors, support of 2 to 6 Volts operation, diagnostic LEDs, program memory space erasure with verification, and freeze-on-halt.

The MPLAB ICD 2 kit includes a demonstration board and samples of the PIC18F452 and PIC16F877 high-performance Flash micro-controllers. The demonstration board features a 2x16 LCD display, temperature sensor, EEPROM memory, LEDs, Piezo sounder, RS 232 interface. The kit also includes the MPLAB IDE (Interactive Development Environment) software.

For the chance to win a kit, log onto www.microchip-comp.com/eworld-icd2 and enter using the online entry form

AD INDEX

New 400W Laser Power Supply

UK Power supply specialist, Ferrus Power Ltd, has demonstrated its extensive design capability by developing a new 400W laser power source for a major OEM manufacturer of medical equipment.

Featuring a 60A constant current source and nominal voltage of 2Vdc, the product can drive up to 35W CW laser diodes. In addition, a TEC output rated at 250W/25Vdc is provided with reversible polarity for driving external peltier devices for diode cooling or heating.

Laser and TEC current is controlled via 0-10Vdc external programming in each case. Current monitoring for both laser and TEC is provided in 0-10Vdc format with voltage monitoring proportional to output. For safety purposes, a further laser interlock control offers beam attenuation and shuts down the laser output to meet the requirements of 21 CFR 1040.10. Signal and control connections are via 16W IDC, whilst laser and TEC are via high current screw terminal block.

The need for an external power supply to drive ancillary microprocessor control circuitry is removed as the product also features low voltage outputs of +5Vdc, ±15Vdc and 24Vdc via 6-way 0.156" header.

The product is suitable for worldwide applications and offers universal mains input operation of 90–264Vac with active power factor correction to meet the line harmonic distortion requirements of EN61000-3-2 class D. The product is currently undergoing medical approvals testing to EN60601-1.

Ferrus has the capability to design and manufacture similar products to suit the laser and opto-electronics industry and would welcome enquiries.

www.ferrus-power.co.uk

Precision Digital Multimeters

Fluke has introduced the new Fluke 8845A and 8846A Precision Digital Multimeters, featuring 6.5 digit resolution, a dual display that shows data in graphic or numeric formats, and multifunction measurement capability. These high-accuracy meters emulate several legacy bench DMMs, and are designed to provide industry-leading value for bench or systems applications including manufacturing test, research and development, and service.

The bench Fluke 8845A and 8846A Precision Digital Multimeters have 14 measurement functions, extending the capability of a standard DMM with wider ranges and features to easily measure temperature, capacitance, period and frequency. The 2x4 Ohms function uses patented split terminal jacks that allow users to perform 4-wire measure-ments using only two leads instead of four. The meters deliver best-in-class analogue performance, measuring DC volts with an accuracy of up to 0.0024 %, a voltage range of 100mV to 1000V with up to 100nV resolution, a current range of 100microA to 10A with up to 100pA resolution, and have a wide Ohms measurement range from 10 Ohms to 1 giga-Ohm with up to 10 micro-Ohms resolution.

www.fluke.co.uk

UHF ASK/FSK Receiver ICs

Atmel Corporation has made available its new ATA5745 and ATA5746 UHF ASK/FSK receiver ICs for automotive RF applications. The ATA5745 operates at 433-435MHz, whereas the ATA5746 covers the 313-315MHz frequency band for the standard automotive environment. These single-chip devices are manufactured using Atmel's new RF BiCMOS process UHF6S, enabling smaller designs. With a size of 5x5mm, they provide the industry's smallest footprints, a perfect fit for Remote Keyless Entry (RKE) and Tire Pressure Monitoring System (TPMS) applications.

These devices' fully-integrated filters provide the best combination of large bandwidth and excellent receiving selectivity.

The ICs' ability to change the modulation type between ASK and FSK, and between data rates without component changes, is important when receiving different RKE/TPMS modulation schemes and data rates. They can be operated in 1-20kbit/s Manchester FSK mode with four different baud rate ranges, selectable through the microcontroller without any hardware modification on board. The typical switching between modulation types ASK/FSK and different data rates is possible in less than 1ms.

These receiver ICs consist of an integrated IF filter, low phase-noise VCO, PLL and loop filter, without requiring any external parts for the functional blocks. The integrated RF circuits achieve an image rejection of typically 30dB. The ATA5745 and ATA5746 are transparent receivers and operate in combination with a separate microcontroller for bit check and polling modes.

www.atmel.com

New Series of Thermal Kiosk Printers

DED now has available the NP-3311 series of thermal printers from Nippon Primex. These printers are particularly suited for outdoor kiosk applications and offer features such as operating temperature of between -200ºC to +600ºC for both the printer and cutter assembly.

The series also offers vertical and horizontal options for paper roll mounting and positioning and is very flexible for kiosk integration.

The printing is at 250mm/s, 203dpi, on paper stock of 58mm or 80mm wide and up to 150gsm – perfectly suitable for applications where a thicker ticket is required. Thanks to the 150mm diameter paper roll, the NP-3311 series is ideal for ticketing applications where the kiosk is left unattended for long periods of time.

Flexibility with the NP-3311 series also comes in the form of a combined full or partial cutter, full speed USB2.0 or RS232C serial interface and Windows drivers for 2000 and XP.
www.ded.co.uk

Vinculum Family of USB Controllers

Future Technology Devices International (FTDI) has released its Vinculum family of embedded USB host controller devices. These ICs handle the USB host interface as well as data transfer functions. Owing to the inbuilt 8/32-bit MCU and embedded flash memory, Vinculum encapsulates the USB device classes as well. When interfacing to mass storage devices such as USB flash drives, Vinculum also transparently handles the FAT file structure communicating via UART, SPI or parallel FIFO interfaces via a simple to implement command set. Target pricing is $5 each at volumes of 10,000 units. The initial product member of the family is the VNC1L device, which features two USB ports which can be individually configured by firmware as host or slave ports.

Key VNC1L features include the 8/32-bit V-MCU core, dual DMA controllers for hardware acceleration, 64k embedded flash program memory, 4k internal data SRAM, 2 x USB 2.0 slow/full-speed host/slave ports, up to 28 GPIO pins, 3.3V operation with 5V safe inputs, low-power operation (25mA running/2mA standby)
www.vinculum.com

New SIC Digital Interface Card from Spellman

Spellman High Voltage Electronics Corporation announced the introduction of its new SIC standard digital interface control card. The SIC control card provides three types of communication interfaces: RS-232, Ethernet (10/100 Base-T) and USB (Universal Serial Bus).

Data acquisition and control capabilities are provided by three microprocessors: a 40MIPS digital signal processor, a network processor and a USB processor/controller. Interface functionality is achieved via fourteen channels of 12-bit analogue-to-digital converters, two additional analogue channels that monitor house-keeping power supply and ambient temperature, five digital output bits, eight digital input bits and three relay/interlock contacts.

The SIC digital interface card, along with a full compliment of software, provides easy, out-of-the-box functionality. A full featured GUI (graphical user interface), written in Visual Basic, allows for control of the power supply via any one of three interfaces. Additionally, a diagnostic web server can control and monitor any SIC equipped power supply from a web browser. Control, operational status and real-time configuration of the power supply can all be accomplished through the use of a provided control applet.
www.spellmanhv.com

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www.microrobotics.co.uk

Micro-Robotics is a Cambridge-based manufacturer of custom and off-the-shelf embedded control solutions and components. The company's VM-1 credit-card-sized control computer is ideal for a wide range of applications.

When used with the Micro-Robotics proprietary Venom-SC object-oriented programming language, the VM-1 controller can handle analogue and digital I/O, graphical user interfaces, communication protocols, data and text files and many other functions. This combination of powerful processor, easy to use application software and comprehensive I/O resources will make the VM-1 highly suitable for applications such as intelligent instruments, hand-held devices, industrial automation and process control systems, security systems and similar other applications.

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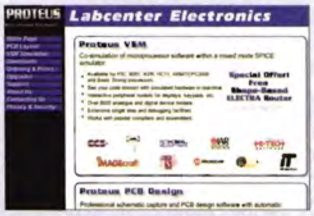

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www.spellmanhv.com

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