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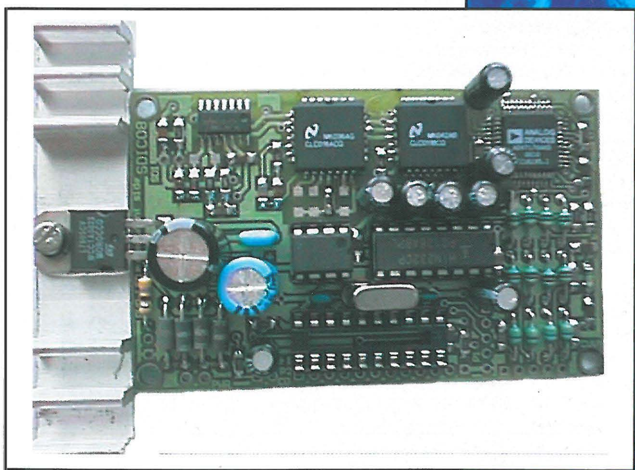
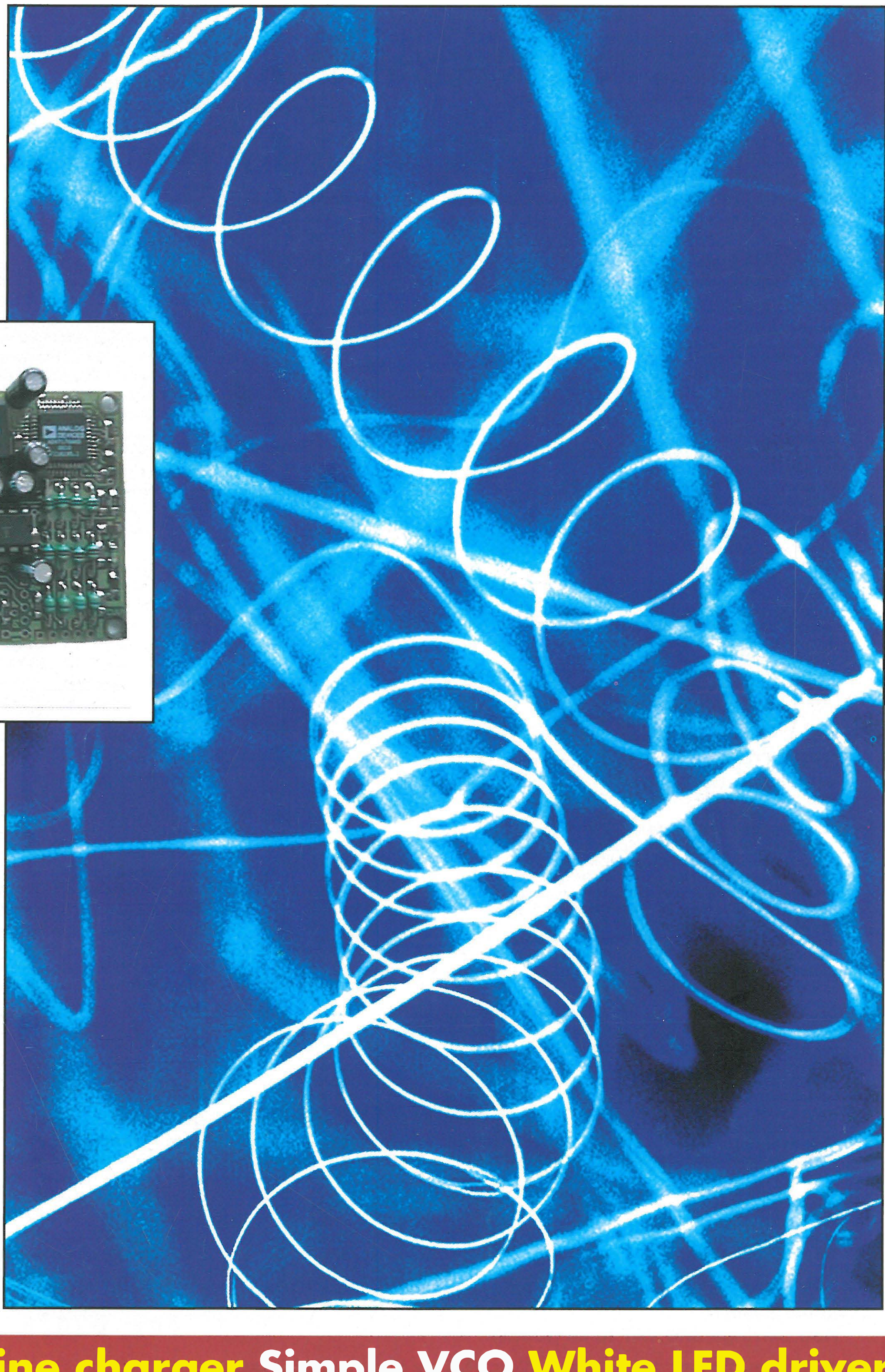
ELECTRONICS WORLD

FEBRUARY 2004 £3.25

SDI to analogue converter





Network analysis II

D. Self on analogue switching

Bluetooth

Circuit ideas: Alkaline charger Simple VCO White LED driver

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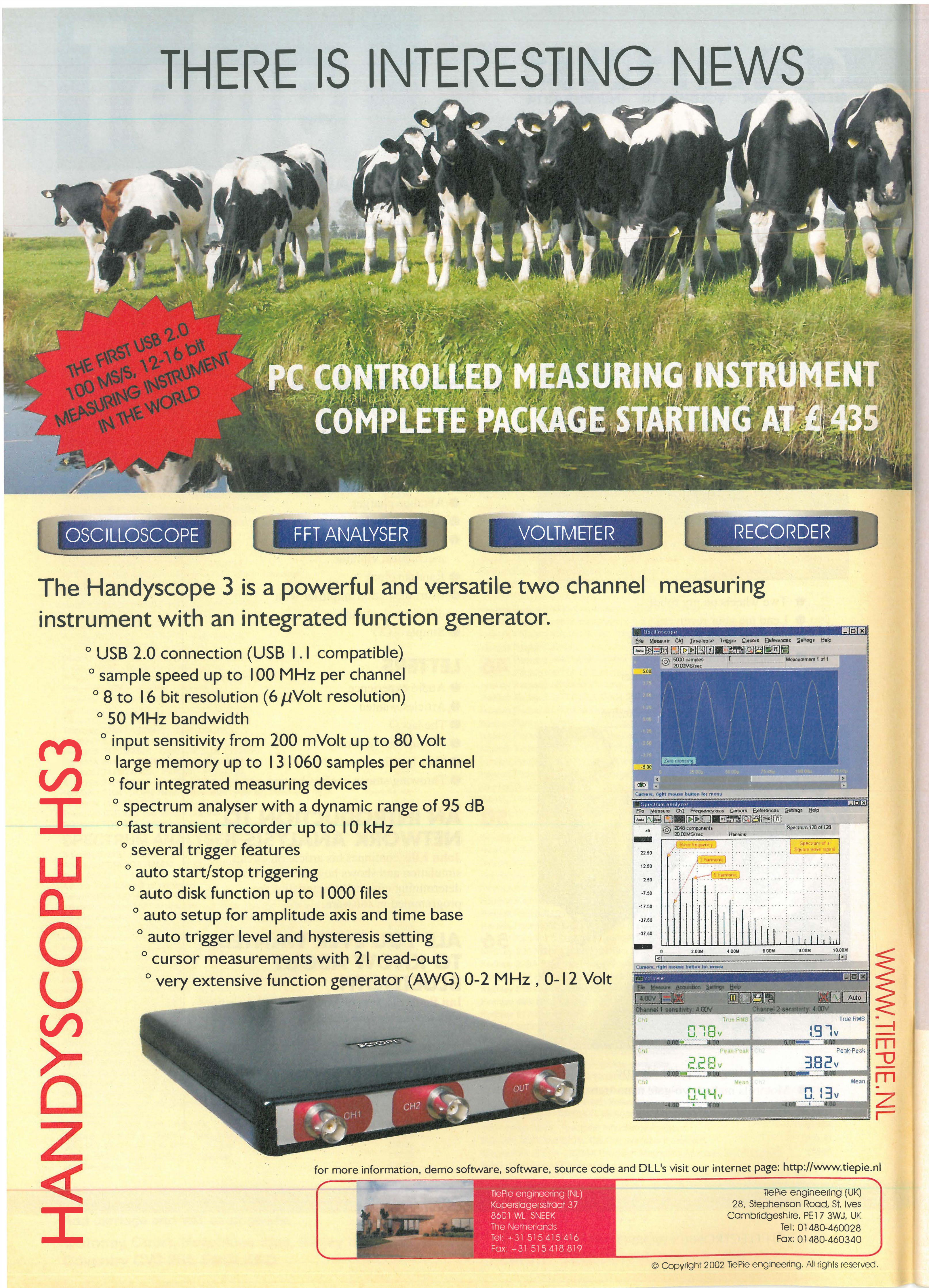

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Getting closer

Having been sitting in this seat now for about 18 months, I've decided that it's time to take stock of where *EW* is and where it is going. The last reader survey was a bit of jest – firstly, putting it in the magazine meant that only readers used it. What I need to know is why non-readers are non-readers. So any help from you the readers would be helpful. I need to contact people that have at least a passing interest in electronics and find out what they need from a magazine such as this. In this survey, we will also be asking advertisers what they think, so again any help here would be much appreciated.

This is your magazine and if I can increase circulation, I can increase the size and cover more topics. Which will probably increase circulation. If you, like me, hanker after the 'glory days' of *Wireless World* – then give me a hand.

Apologies to readers who tried to access our archive website (www.electronicsworld.co.uk) as advertised last month – but an incompetent IT department managed not to get the relevant domain registered. So, if you want to go to our archives go to: www.ewmag.co.uk. I must point out that this is actually part of Softcopy's web site, who look after our electronic archives. Between us we've managed to 'electrify' archives for the last five years, which are now available on separate CD ROMs. If you've got a computer, this is the way to keep your *EWs* archived. It takes up hardly any space, won't go gooey if you get it wet and the search engine makes it really easy to find those obscure articles, circuit ideas or letters. And there's a special offer for readers.

In the coming months we are going to expand the facilities by offering any code or lists in articles available for download and we are going to offer readers the chance to subscribe to an electronic (cheaper) version of *EW*, rather than paper. If anybody is interested in this idea (and I know some of you are) please get in touch.

Phil Reed

New editorial and advertising address

The Highbury Business Communications office previously at Cheam, Surrey has moved to Swanley in Kent. All correspondence intended for the editorial and advertising departments should be addressed to:

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Electronics World is published monthly. Orders, payments and general correspondence to **Caroline Fisher, Highbury Business Communications, Nexus House, Azalea Drive, Swanley, Kent, BR8 8HU**

Newstrade: Distributed by COMAG, Tavistock Road, West Drayton, Middlesex, UB7 7QE Tel 01895 444055.

Subscriptions: Wyvern Subscription Services, Link House, 8 Bartholomew's Walk, Ely Cambridge, CB7 4ZD. Telephone 01353 654431. Please notify change of address.

Subscription rates
1 year UK £38.95 O/S £64.50
US$100.62 Euro 102.55

USA mailing agents: Mercury Airfreight International Ltd Inc, 10(b) Englehard Ave, Avenel NJ 07001. Periodicals Postage Paid at Rahway NJ Postmaster. Send address changes to above.
Printed by Polestar (Colchester) Ltd,
Filmsetting by Impress Repro
A1 Parkway, Southgate Way, Orton Southgate, Peterborough, PE2 6YN

Transistor exceeds 500GHz

A transistor with a peak switching frequency of 509GHz has been fabricated by researchers from the University of Illinois at Urbana-Champaign.

The team used indium phosphide and indium gallium arsenide to make the device, which can support much higher current densities than silicon.

"The steady rise in the speed of bipolar transistors has relied largely on the vertical scaling of the epitaxial layer structure to reduce the carrier transit time," said Professor Milton Feng from Illinois.

"However, this comes at the cost of increasing the base-collector capacitance. To compensate for this unwanted effect, we have employed lateral scaling of both the emitter and the collector."

The 509GHz device has a collector width of 75nm and a base of 25nm.

"Further vertical scaling of the epitaxial structure, combined with lateral device scaling, should allow devices with even higher frequencies," Feng said. "Our ultimate goal is to make a terahertz transistor."

Laser comes out on top

Semiconductor lasers that emit from the surface of the material are crucial for lowering cost, so making a quantum cascade (QC) laser emit in this way is a significant step. Scientists at Bell Labs have managed this trick, by combining a photonic crystal structure into the QC laser.

QC lasers are made up from 30 or more very thin layers of semiconductor. Electrons are introduced into the top of the stack, and as they pass down the layers they liberate photons in a cascade.

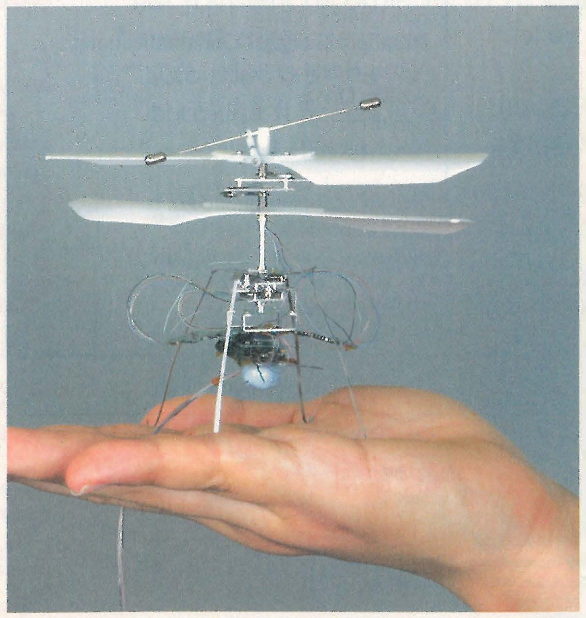
However, each layer emits its light from the sides, making it tricky to collect and launch the light in a useful way.

By etching a photonic crystal pattern through the layers of semiconductor, the laser light is diffracted and forced to travel up through the material, and out of the surface of the device.

Bell Labs' crystal is simply an array of holes etched in a hexagonal pattern, right through the layers and into the substrate.

The surface emitting QC laser could replace the industry workhorse - the vertical cavity surface emitting laser. The QC version is half the diameter at 50μm, and does not require the pair of complex distributed Bragg reflectors used by VCSELs.

The laser has a wavelength of 8μm, which would make it suitable for sensing gasses and chemicals by measuring molecular absorption lines.



Fly-weight robot

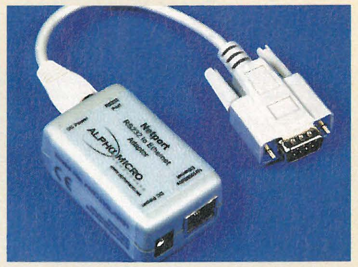
A flying robot weighing in at just nine grams has been developed by Seiko Epson in Japan.

In order to save weight, the μFR uses a 0.4mm thick ultrasonic motor to power its rotor blades. Ultrasonic motors are increasingly found in camera motor drives, mainly at the better quality end of the market.

Weight is further saved by using contra-rotating blades, which avoids the use of a tail rotor as the blades cancel out any torque reaction. The motor and blades generate around 13g of thrust, claimed Epson.

A weighted linear actuator is used to adjust the robot's centre of mass, which helps it maintain a level flight aspect.

Control signals are sent to the μFR via a Bluetooth wireless interface.



Basingstoke's Alpha Micro Components has developed a plug-and-play serial-to-Ethernet cable adaptor.

"It enables any device or machine with a serial port to become network and Internet-enabled in an instant," said Alpha.

NetPort, as it is called, is aimed at network routers, meter readers and point of sale terminals, as well as home entertainment systems, vending machines and security systems - particularly where adding Ethernet inside a product would mean re-qualification or re-testing.

The unit, slightly larger than a match box, has a separate power input and can hold around six Web pages; allowing it to act as a server even when its host is turned off.

A modem emulation mode is built-in to make use of existing modem-handling capability in the host. NetPort is available from www.nifty-gadgets.net and www.alphamicro.net

All-plastic CMOS steps closer

Philips researcher Eduard Meijer characterising the properties of polymer electronic circuits.

Scientists at Philips fabricated plastic field-effect transistors that conduct both holes and electrons within a single sheet of material.

"The discovery enables the design of robust digital circuits with low power dissipation and a high yield in their fabrication," said the firm - because CMOS requires both n and p-channel devices and the Philips development makes them both possible in a single, perhaps spin-coated, plastic substrate.

"Unfortunately, until now, organic semiconductors only showed the flow of one type of charge," said Philips. This is not an intrinsic property of these materials, but is caused by the occurrence of a high energy barrier for either electron or hole injection from the metal source and drain electrodes.

The company has actually made its transistors in two different ways.

In the first, a blend of p-type and n-type materials is used in combination with source and drain electrodes of gold. "The charge injection barrier problem is solved by mixing a material with a low energy barrier for electron injection, with a material with a low barrier for hole injection," said Philips.

In the second approach a *single* organic semiconductor was used. "For this purpose, organic semiconductors were chosen with a low bandgap, thus reducing the energy barrier at the source and drain electrodes for both electrons and holes," it said.

Inverter circuits made with the transistors showed good noise margins and high gain values, claimed the company.

Lend me your receivers

Rights to frequencies in the radio spectrum could be 'traded', if proposals from the Radiocommunications Agency and regulator Ofcom go ahead.

The two organisations have launched a consultation programme to look at the proposals. They would allow licences issued to broadcasters, mobile phone operators and others to be traded or sold.

"Spectrum trading will allow innovation and choice to shape the future allocation of spectrum, in place of the centrally planned, top-down approach of the past," said Ofcom's chief executive Stephen Carter.

The RA's responsibility for issuing non-military licences passed to Ofcom at the end of 2003.

"Our aim is to stimulate an environment in which the UK's communications industries flourish. The introduction of spectrum trading is a major component of that overarching policy objective," added Carter.

The Government is backing the proposals. Stephen Timms, minister for e-commerce, said: "This is key to the provision of new wireless services that underpin modern communications for business, entertainment and leisure, as well as for essential public services."

Ofcom reckons that opening up a market for spectrum trading will make it easier for companies to establish new wireless services.

Ofcom and the RA are seeking responses for the consultation document. Details can be found at www.ofcom.org.uk

Low cost storage uses plastic

Materials for a write-once, read-many (WORM) memory aimed at low cost archiving have been developed by researchers at HP Labs and Princeton University.

The single use memory card would be faster and easier to use than CDs, said the team, and would not feature any moving parts.

A paper published in Nature describes the basic organic material, which is already used in anti-static bags, electro-chromic windows and organic LEDs.

The HP Labs/Princeton team integrated an electro-chromic polymer with a thin-film silicon diode deposited onto a flexible metal foil substrate.

Using thin films deposited onto metal foil would satisfy the requirement for low cost.

Passports get their chips

Secure microcontroller developers are gearing themselves up for moves to add biometric identification to passports and national ID cards.

Europe's top three chip makers - Infineon Technologies, Philips Semiconductors and STMicroelectronics - along with Sharp Microelectronics have unveiled silicon with the necessary memory.

Sharp and ST, for example are integrating up to 1Mbyte of flash memory in a secure chip, with all the manufacturers integrating a 32-bit processor.

Reza Kazerounian, head of ST's smartcard chip division, said: "The ST22FJ1M was designed to allow developers to escape the current smart card software architecture limitations and hence to enable new applications for existing and emerging markets."

The chip makers are responding to moves by international and national authorities. The International Civil Aviation Organization, for example, has already outlined plans to add face recognition to all passports. Data, around 50kbyte for face recognition, would be passed to the reader through a wireless link.

Meanwhile the German Government said it would add some sort of biometric to its passports by 2007. The UK's plans for a national ID cards system has been delayed, but is likely to roll out in some form in the next ten years.

Two wheels on my robot

The Humanoid Robotics Group at MIT have modified a Segway self-balancing people transporter to be the 'legs' of a robot.

"The Segway's dynamic balancing on wheels provides us with the agility of a narrower wheel base in tandem with the facility of mounting torso, arms and robotic head at human-level height," said MIT's artificial intelligence lab.

So far, a simple one-armed robot with vision has been built that is capable of seeing a door, opening it, and passing through. "We are deriving our assessment via a prototype mobile humanoid robot with one arm," said MIT. "The goal of this robot, named Cardea, is to navigate using simple active vision and sensors while using its arm to reach out and interact with objects in compliant and safe ways."

Compliance - a bit of 'give' in the robot arm - is important to the project as rigid powerful arms are seen as a potential hazard amongst everyday objects and people. "Conventional robot manipulators are usually not safe to spontaneously interact with and are confined to environments such as factory floors," said researchers.

To add compliance, MIT has put a spring in series with the arm's actuator which "allows the forces interacting with the manipulator's axis to be sensed", said the lab, "Using this force information, a spring model can be used to control the manipulator - allowing the compliancy and responsiveness of a human arm that has muscles to be coarsely approximated."

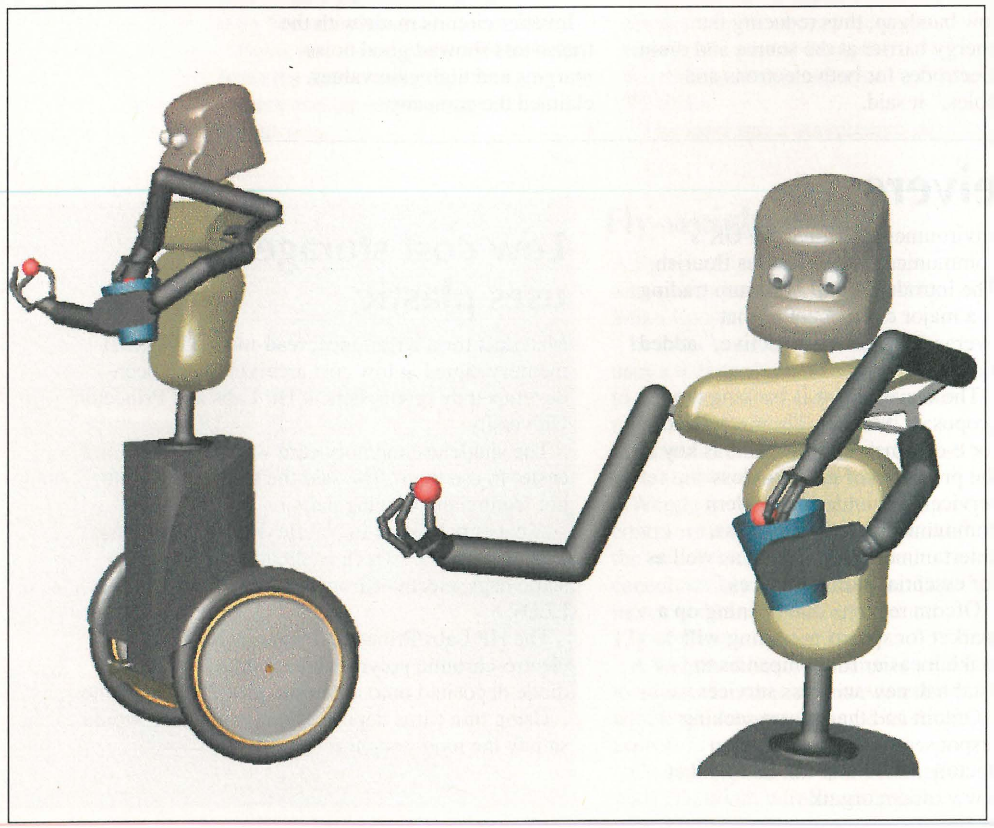
Unusually, Cardea will eventually have three arms, all different. "It will have the potential to carry something while unscrewing or opening it. Plus three arms provide three combinations of two arm pairs", said MIT. "Cardea can extend beyond the assumptions and conventions of the humanoid condition."

Each arm will have six degrees of freedom: three at the shoulder, one at the elbow and two at the wrist. The difference will be in the lengths and proportions of their joint segments. 'Hands' will be varied.

MIT's artificial intelligence lab is also responsible for Cog, a stationary robot which explores its surroundings. "Cog has a limited means of actively engaging the world. When Cog explores the world, we must bring the world to Cog," said the lab. "We envision that Cardea will actively seek objects and people, and use its mobility to go over and explore them."

Work done with Kismet, the lab's famous robot which makes facial expressions in response to human facial expressions, may also be rolled into the new machine. "Cardea will be outfitted with a head that, at the least, will serve two functions: it will be an active vision platform with human like visual properties such as cameras that act and move as its eyes, and, its face will provide it with social character and social inter-operability."

Cardea can be seen in action at: www.ai.mit.edu/projects/cardea



EU to force battery recycling

The European Commission is to issue a Battery Directive, which will mandate the collection and recycling of all batteries placed onto the European market.

The Commission aims to cut the practice of dumping spent batteries in landfill sites or into incinerators.

"Due to the metals they contain, batteries pose environmental concerns when they are incinerated or landfilled," said the EC.

Recycling the metals used should also help to save resources, it said.

"Discussions on a new Battery Directive have been on-going for several years and today we are presenting a concrete and well-balanced proposal," said Margot Wallström, commissioner for the environment. "Most importantly, consumers will have to contribute to environmental protection by bringing back their spent batteries to collection points."

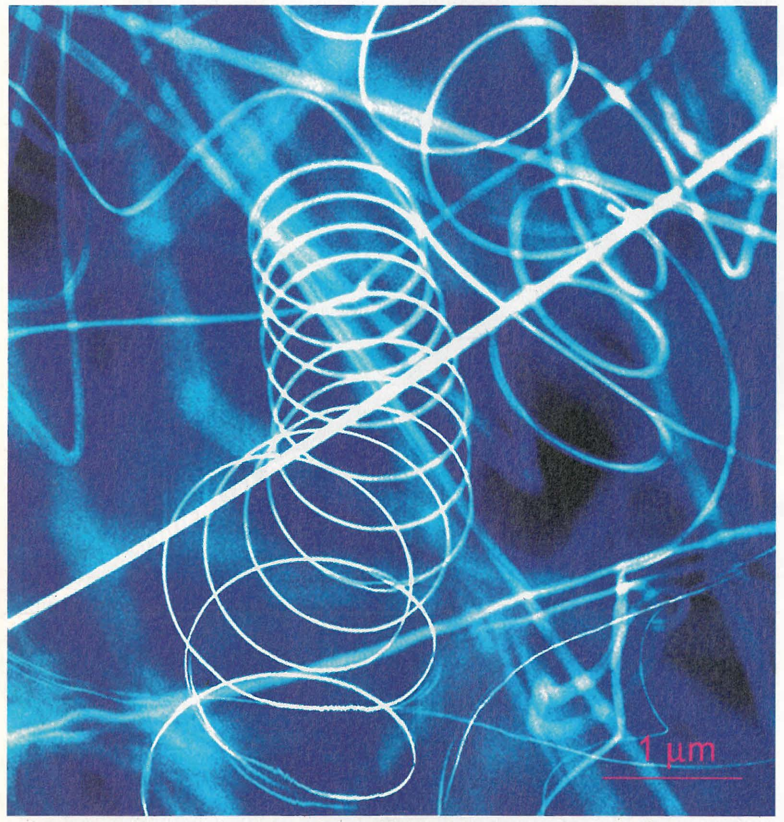
The Commission reckons 1.15 million tonnes of batteries are sold in the EU each year. Some 800,000 tonnes are automotive, 190,000 tonnes are industrial and 160,000 tonnes are for consumer use.

Mercury, lead and cadmium have been identified as the most dangerous substances to health contained in the batteries.

"Other metals used in batteries, such as zinc, copper, manganese, lithium and nickel may also constitute environmental hazards," said the EC.

Existing legislation only applies to batteries containing certain quantities of cadmium, mercury or lead and covers only seven per cent of all the portable batteries placed on the EU market annually.

The annual cost of recycling, paid for by producers and local authorities, would be under €2 per household per year, claimed the Commission.



Nano-springs are peizo-electric

Researchers at the Georgia Institute of Technology have made long ribbon-like single crystals of zinc oxide that spontaneously form helical shapes.

"Piezoelectric smart materials based on zinc oxide are important because they could be the transducers and actuators for future generations of nanoscale devices," said professor Zhong Wang, director of Georgia Tech's nanoscience centre. "You could use them to measure nano- or pico-newton forces."

The crystals are 10-60nm wide, 5-20nm thick, up to several millimetres long and form springs 500 to 800nm in diameter.

They also have a surface charge. "The polarised surfaces will attract different molecules with different charges, which would permit selectivity," Wang said.

Wang and collaborator Xiang Yang Kong fabricate the structures using a solid-vapour process. They formed on a cooler alumina substrate nearby zinc oxide powder evaporating at around 1,350°C.

PC robot ripe for experimentation

This is 912, a robot from Pennsylvania-based White Box Robotics. At its heart is a mini-ITX motherboard from Taiwanese PC component firm VIA which means it can run PC software and is suitable for robotic experimentation.

"Our nine series of robots allows anyone who can operate a PC the chance to own an attractive and functional personal robot," said Thomas Burick, president of White Box. "The 912 is designed with an industry standard approach to robot building. Almost all of the components used in the 912 are standard off-the-shelf computer parts. Any computer store in the world becomes your own personal robot parts bin."

912 is delivered able to move about the house and play MP3 files

www.whiteboxrobotics.com

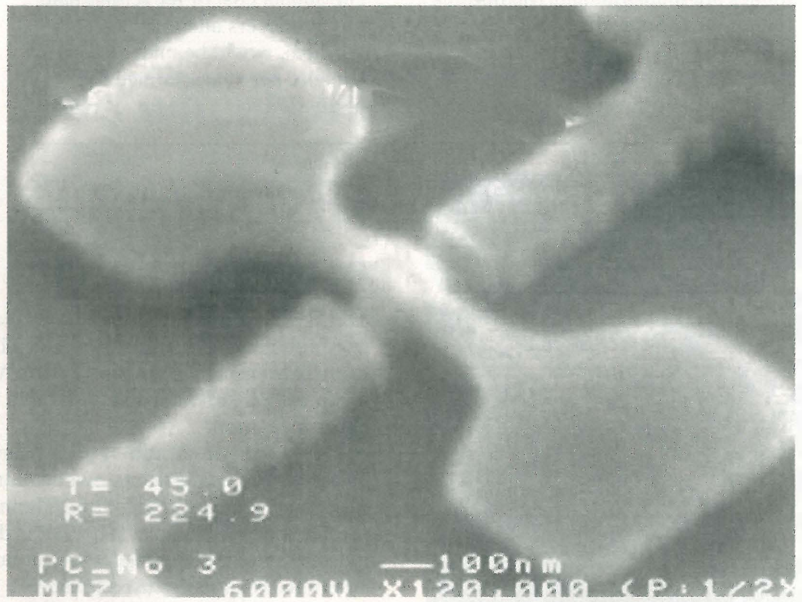
Motorola makes two-gate nano-transistor

Researchers at Motorola have created a nano-scale multiple independent gate Fet - a MIGFET.

Conventional mosfets have one gate deposited on top of a channel between the device's source and drain. A voltage on the gate controls the carriers in the channel and therefore the fet's resistance.

The fastest of today's research fets have a channel sitting on top of a substrate with a gate deposited on the channel's sides and top. With the gate on three sides of the channel, and a very thin channel, carriers can be affected extraordinarily quickly, resulting in multi-GHz operation.

If the top part of the gate can be removed, or not deposited, a two gate transistor is formed - with one gate on each side of the channel - but this has proved difficult to do, said Motorola: "Thus far, most of these experimental structures have been limited because the two gates are electrically linked. While these structures will offer additional performance improvements over existing planar devices, we have gone beyond forming a single gate on multiple sides of nanometer scale silicon."



The device in question has a silicon channel region of around 25nm wide and 100nm high formed on a silicon-on-insulator substrate. A 2.5nm later of oxide grown on the channel forms the gate insulator. Exactly how the firm manages to deposit the gate on the channel sides without getting it on top is still a secret. "The process keeps the structural integrity of the entire channel and gate structures intact, and allows the two gates to be perfectly self-aligned to each other," is all Motorola will say.

Two isolated gates 100nm long are formed.

With two gates, one gate can be used to adjust the threshold voltage of the transistor - trading operation speed against leakage current - while the other is used in the normal way. Also, two gates also mean the transistor can perform a logic function on its own. And finally, the two gates can be wired together for super-fast operation like other research fets.

This last configuration results in a high on/off current ratio with $I^{DSon}=10\mu A$ and $I^{DSoff}=1pA$.

Mosfet lowers resistance

Philips Semiconductors has demonstrated a Mosfet with under $1m\Omega$ on-resistance. The TO-220 package uses a copper plate to reduce resistance between die and circuit board.

The device is part of Philips' attempt to move further into the Mosfet market. The firm has also unveiled 20V p-channel Mosfets with $50m\Omega$ R^{DSon} in TSOP6 packages. Such devices are crucial as a switch in mobile phone handsets and other consumer products. The Mosfets are used to power down idle components, such as hard drives or displays, in order to conserve battery power. P-channel devices are easier to drive in 'floating' mode, where no connection to 0V is possible, said Philips.

Toshiba has launched 40Gbyte versions of its tiny 1.8-inch hard disk drives that fit inside type-II PC Cards.

The Japanese firm began making 1.8-inch drives in 2000, starting with a 2Gbyte capacity removable PC Card.

The latest 40Gbyte version fits in the standard 8mm high card and weighs just 62 grams. DMA transfer rate is 100Mbyte/s, while the mean time to failure is rated above 300,000 hours.

A 20Gbyte version fits in a 5mm height card.

SDI to analogue converter

Following on from last month's analogue to SDI converter – quite often you need to go back the other way for example for older equipment or displays. Emil Vladkov explains

The devices presented here are the partner devices to the CSDI10 decoder described in last month's article. Both of the units presented here do exactly the opposite to the CSDI10, namely they take the 270Mbps Serial Digital Interface signal according to SMPTE 259M and convert it to the analogue domain. One of the main strengths of the two encoders presented is the possibility to output different formats – the component YUV, the component RGB and the composite CVBS. You may ask yourself what is the intention for implementing such a converter, where can it be used? To provide an answer to this question lets examine the following situation: you have a modern studio infrastructure with the main distribution standard set to SDI. So you will probably have a SDI switcher, SDI distribution amplifiers, mixers with SDI inputs and outputs, recorders with SDI inputs and so on. Probably you will need to monitor the signal at some point of the distribution, let's say at the studio output. I know there are monitors with SDI inputs, but they are expensive. You may well want to use existing (analogue) professional monitors, which typically will have component inputs. So you will need to convert from SDI to YUV. This is only one possible example. Everywhere you have old component or composite input equipment that you wish to use in your SDI environment you will need a converter like the described here SDIC08 or SDIC10.

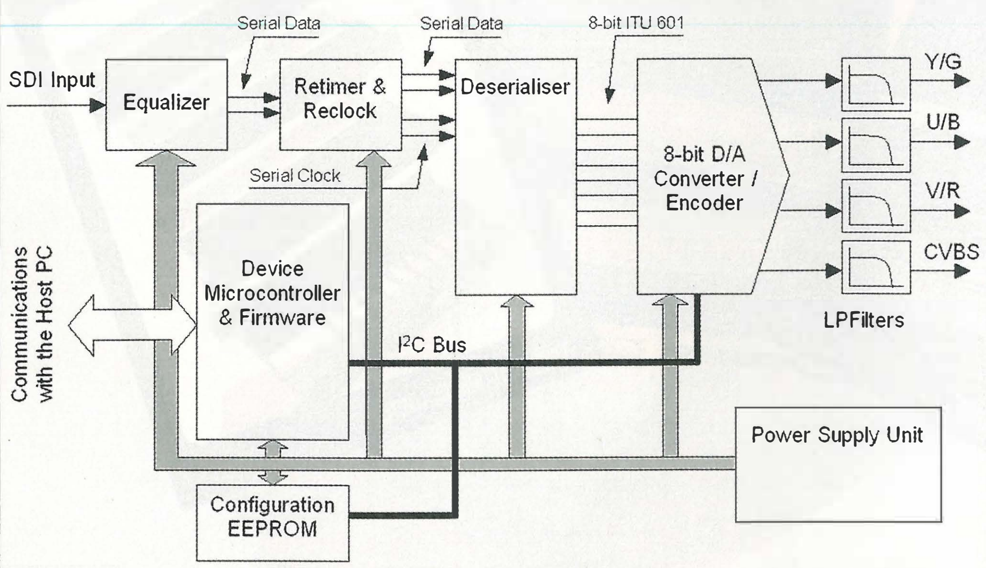


Fig. 1. Functional Block-Diagram of the 8-bit SDIC08 Encoder.

The difference between the units

The only difference is that the one device uses an 8-bit digital-to-analogue converter, while the other device uses a 10-bit D/A Converter. The input SDI data stream is deserialised in the encoders and converted to parallel 10-bit data words (the ITU 601/656 standard). The analogue video is usually digitised to 8-bits but newer equipment may also use 10-bit. For compatibility issues all deserialisers output full 10-bit word length with no regard to whether all 10 bits are used or not. The SDIC08 takes only the most significant 8-bits and encodes them. The SDIC10 takes all 10 bits. Of course there are some very important IC-dependent differences between the schematics of the two devices. The ADV7194 used in the SDIC10 has no output drivers so external OPAMP based drivers have to be arranged[2]. The simpler ADV7176A used in the SDIC08 has integrated cable drivers, so such external circuitry complication will not be needed[1]. Therefore the ADV7176 is a rather simple (very reliable) device with a limited set of signal processing functions. This is not the case with the ADV7194, which can control many of the video signal parameters (luma-chroma delay, pixel blocking artefacts, hue, saturation, contrast and so on). The functional block diagram structures of the SDIC08 and the SDIC10 are presented in **Fig.1** and **Fig.2** respectively.

Detailed schematic diagrams of the devices

Figure. 3. and **Fig. 4** represent detailed schematics of the SDIC08 and SDIC10. Let us begin with the description of the SDIC08 (Fig.3) which seems to be a little less complicated. The SDI input signal is fed to the unit at J1 BNC connector. The input is matched to the line with the R3 75Ω resistor. The line equalizer, which makes it possible to connect up to 300m of coaxial cable to the SDIC08, is IC1 – a National Semiconductor CLC014 IC[4]. This type of equalizer has differential inputs, so with a unipolar type of input some sort of balancing will be needed. This is accomplished through the R1, C1, R2, C2 and R5 components (R1 and R2 provide some kind of input isolation from the line). C6 sets the response time of the adaptive equalisation loop. The CLC014 provides a CD (Carrier Detect) output, which is used to drive the D2 LED (through IC2A inverting buffer). So the user is provided with a visual indication for valid signal presence at the device input. The equaliser has a differential output (DO, DO\) and the correct PECL levels on the internal signal paths are set through D1, R4 and R6. This provides some kind of trace line termination too. The unused parts of the IC2 buffer are tied to the supply voltage, so that they will not change state and cause noise in the circuit.

The differential output of the equaliser is fed to the IC3 (CLC016) National Semiconductor Retiming/Reclocking chip[5]. The last one is configured to restore the four different uncompressed video data rates – 143, 177, 270 and 360Mbps, which are set through resistors R15 – R17. Actually only the 270Mbps data rate is used, the others provided only for completeness. The D/A converter responds only to 4:2:2 uncompressed digital video, not to the digitised composite (PAL and NTSC) or the widescreen data formats. Therefore the re-timer is configured in manual data rate setting mode and the RD1/0 bus lines are hardwired to allow the retiming of the 270Mbps data rate only. The C8, C9 and R13 components represent the loop filter of the internal PLL of the re-timer. The CLC016 has two types of differential outputs – the Serial Data Outputs (SDO and SDO\) and the Serial Clock Outputs (SCO and SCO\). These outputs are set to the correct level and terminated through resistors R8 – R11.

The serial digital data stream and the serial digital clock are supplied to the serial digital deserialiser IC8 (CLC011), which descrambles and deserialises the SMPTE 259M video to parallel data words PD9-PD0 and produces the word-rate clock PCLK for clocking them into the encoder[6]. The CLC011 is wired so that the NRZI-to-NRZ conversion is performed (NRZI pin tied HIGH), the polynomial descrambling is conducted on the NRZ data (DESC pin tied HIGH) and the frame structure of the video signal including the Timing Reference Signal (TRS) is recognised (FE-pin tied HIGH). The EAV (End of Active Video), TRS (Timing Reference Signal) and NSP (New Sync Position) outputs are not implemented in this design.

A more detailed description of the Serial Digital Interface signal processing is given in an article of mine, published in *EW* and describing an SDI test pattern generator and receiver, so I will not go into detail here[7].

The video encoder used in the SDIC08 device is the ADV7176A professional converter/encoder, fed with CCIR 656 8-bit 4:2:2 parallel video with the luma and chroma information multiplexed[1]. The ADV7176 has the input option of accepting 16-bit non-multiplexed 4:2:2 video through the P15-P0 lines but this option is not used here as the deserialiser outputs multiplexed video format. The Teletext data inputs (TTX, TTXREQ) are not used in the design, but the user is encouraged to implement them in extensions of this project to feed teletext information in the analogue video signal. The CLOCK input has to be supplied with 27MHz clock signal to operate the device; in our case this clock signal is derived from the incoming data stream through the deserialiser (PCLK word-clock). The R27 resistor connected to the RSET pin is used to set the full-scale amplitude of the output signal. I have used the value proposed by the manufacturer to achieve standard levels. Reset is supplied to the encoder through the use of the R22-C26 group. One great advantage of this IC, compared to the far more powerful ADV7194, used in SDIC10, is that the component signals (YUV or RGB) and the composite signal (CVBS) are simultaneously available at its outputs. The four DAC-outputs DAC A, DAC B, DAC C and DAC D are biased with the 75Ω R28-R31 resistors to achieve correct signal levels. The supply to the encoder is derived from the on-board VCC +5V supply after filtering with the C27, C28 and L1 components.

The output filters of the 4 separate DACs are built around the LC-circuits L2-L12 and C31-C42. These filters are important to smooth the output analogue signals, especially if these will be subject to following ADC conversion or will be supplied to analogue TV monitor to prevent aliasing. The outputs of the device (component and composite) are available on the J3-J6 connectors.

The AT89C2051 microcontroller has 2K onboard EEPROM memory where the firmware resides. The micro is clocked from the crystal oscillator build around X1, C18 and C19 components. The configuration information of the whole device is stored in the IC7 EEPROM in a non-volatile way. Any change the user makes to the configuration is written

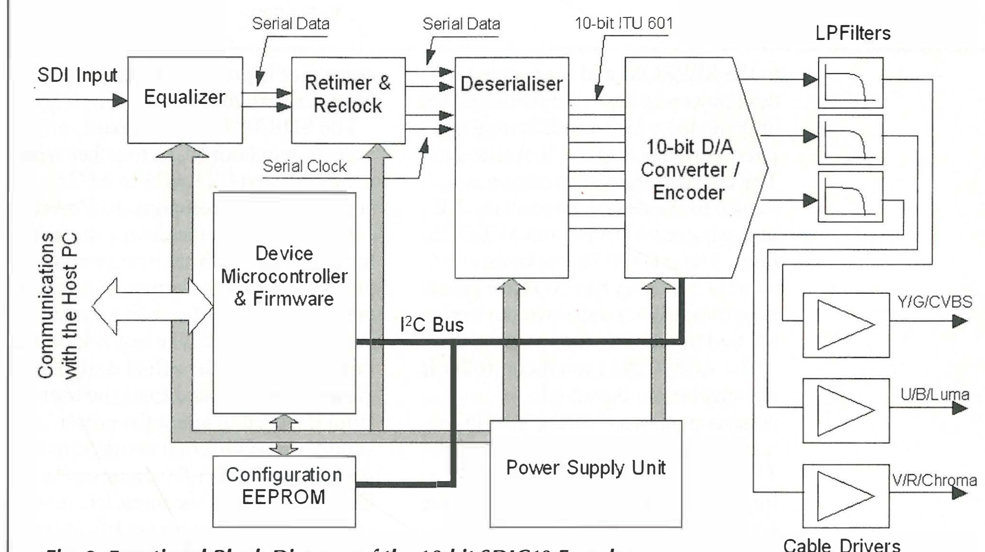


Fig. 2. Functional Block-Diagram of the 10-bit SDIC10 Encoder.

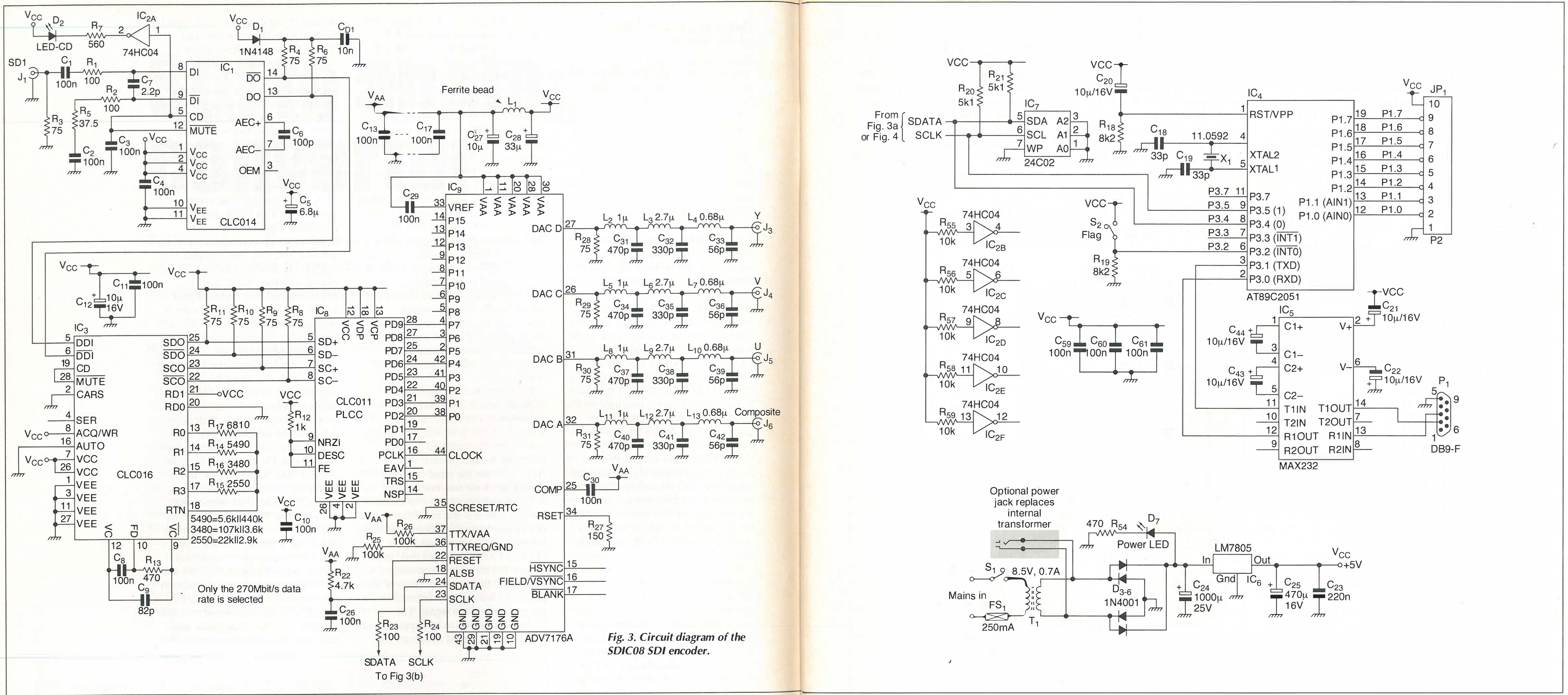


Fig. 3. Circuit diagram of the SDIC08 SDI encoder.

to the EEPROM and is executed at next power-up from the memory. The only device which needs setting up internal registers is the IC9 encoder. The configuration information is passed to the device through the I²C bus using the SDATA and SCLOCK lines. The ADV7176 responds to I²C address 54h. The EEPROM responds to address A0h, so the two devices are tied together to the common bus.

The AT89C2051 microcontroller is responsible for the serial communications with the host PC, needed for configuring the SDIC08. The IC5 interface circuit has the function of an interface driver for the serial RS232 interface, provided on the back panel of the casing as P1 Cannon DB-9 connector. The JP1 connector is provided for device hardware extensions.

The SDIC08 has an onboard voltage regulator (IC6) together with the associated C23, C24 and C25 supply filtering components. Power can be applied to the device in one of the two ways – through an internal power supply transformer or through the J2 power jack from an external wall cube adapter. The last solution is implemented in the actual design as it is more versatile and frees the user from the need to adapt the power supply to the different country mains standards. The D3-D6 diodes form a Graetz circuit, so the input DC power supply polarity has no significance on the correct operation of the device. The D7 diode provides indication that power is supplied to the unit.

The SW2 flag is the selection line for choosing one of the both component modes of operation of the SDIC08 device. When closed the RGB mode of operation is selected, when open the YUV standard is supported. Regardless of the switch position the composite video output (CVBS) is always produced from the encoder, which in my opinion is the greatest advantage of this device (SDIC08) over its sophisticated counterpart (SDIC10).

The schematic diagram of the advanced video encoder SDIC10 is presented in Fig. 4. The unit uses the professional extended 10-Bit video encoder with 54MHz oversampling ADV7194 (IC4)². The Serial Digital Interface signal traverses the same way as in the SDIC08. First it is equalised by the IC1 SDI equaliser, then it is reclocked and retimed in IC3 and last it is deserialised in IC8 to provide full 10-bit video resolution to the encoder. The encoder is configured from the onboard microcontroller through the I²C interface with the SCL and SDA lines. Again the encoder responds to the address 54h on the I²C bus where also the configuration EEPROM resides (IC7). Power supply and host PC communications do not differ from the simpler 8-bit case.

The ADV7194 encoder supports many input formats of the parallel video words, like 4:2:2 YCbCr format in 8-, 10-, 16- and 20-bits length. It also supports the 3x10bit progressive scan format implemented in some professional computer graphics stations. This explains the excessive number of inputs, which can be seen from Fig. 4. Besides the normal port inputs P19-P0 (from which only the 10-bit P9-P0 are used in the design) there are 10-bits wide Y-, Cb- and Cr- ports. Following the recommendations of the chip manufacturer (Analog Devices Inc.) the unused inputs are tied to ground. The Teletext input signals (TTX, TTXREQ) are not used in this implementation, but the reader should feel encouraged to use this advanced option of the integrated circuit to produce new more sophisticated designs. Reset to the circuit is applied through the R37-C39 components. There is a hardware option to select the output TV-standard (PAL_NTSC pin), which is easily overridden from the firmware setting up the correct values in the internal registers. The two resistors R18 and R19 connected to the RSET-pins determine the output voltage swings for the two halves of the output DACs (6 in this case: DACA, DACB, DAC C and DAC D, DAC E, DAC F). The outputs of all 6 DACs can only provide 4.33mA of output current, so some kind of buffering is mandatory in real world cable driving applications. The output buffering is provided for 3 of the D/A converters – DAC A, DAC B and DAC C. The single supply non-inverting AC-coupled 2x amplifier configuration based upon the use of Analog Devices AD8054 (IC10 A, B and C) video op-amps is implemented to provide buffering[3]. The outputs of the non-inverting 2x amplifiers are AC-coupled to the coaxial line through C42, C43, C46, C47 and C50, C51 and matched to the impedance with R36, R41 and R44 series matching resistors. The component/composite outputs (depending of the mode of operation, selected through SW2 and software) are provided on J5, J6 and J7. The outputs are filtered to remove the chance of aliasing prior to buffering with the filters build around the components L1-L6, C23-C28 and R23-R28. The filters are calculated for the 4x mode of oversampling the output signal. Implementing the filter in the 2x mode of oversampling proved not to have catastrophic consequences! As the output DACs are current mode, the R20-R25 resistors form a kind of current-to-voltage converter. The DAC D, DAC E and DAC F DACs are not buffered, but are routed on the PCBoard, so that they can be implemented in design modifications with no high current driving requirements.

The ADV7194 encoder has separate

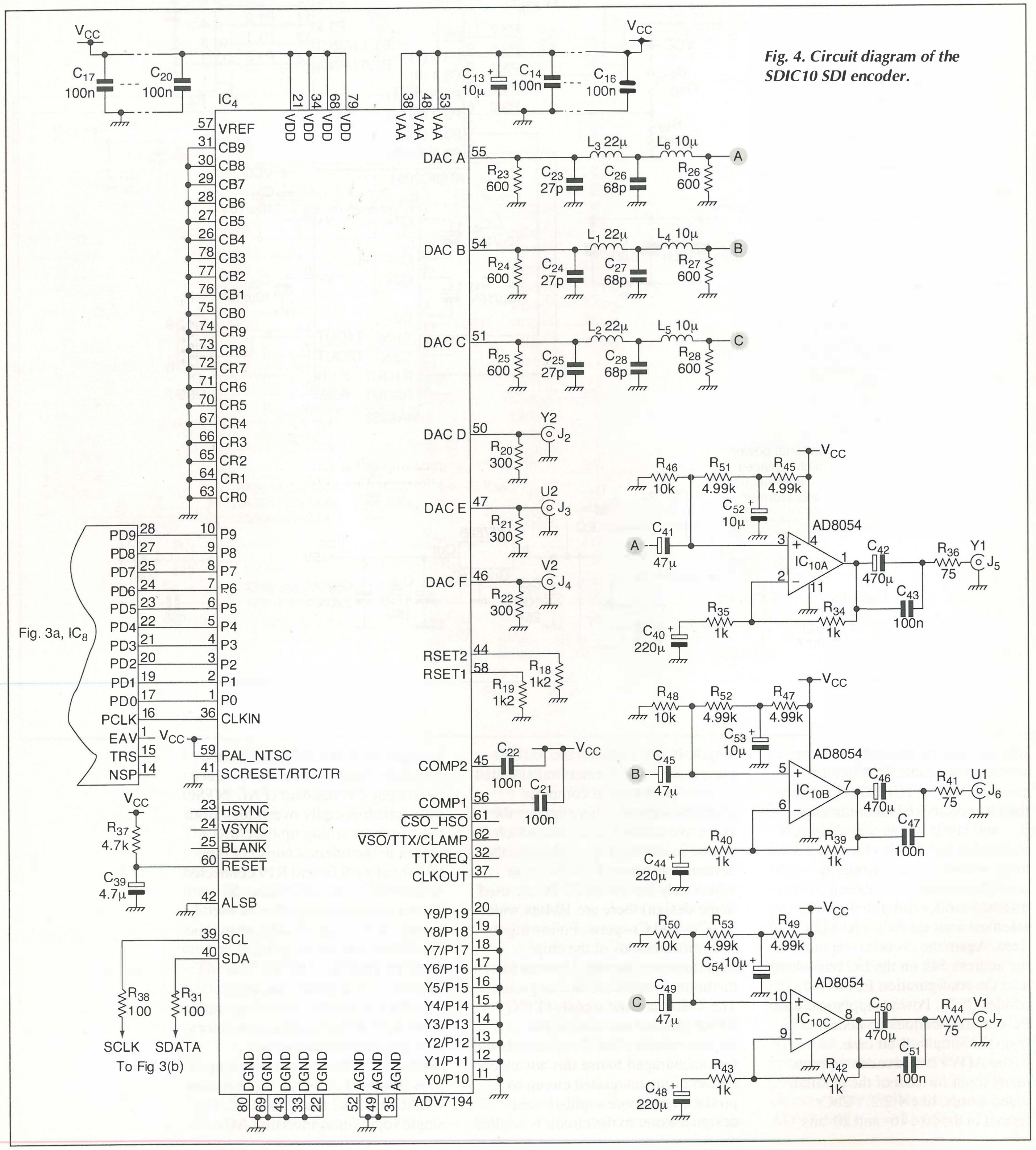


Fig. 4. Circuit diagram of the SDIC10 SDI encoder.

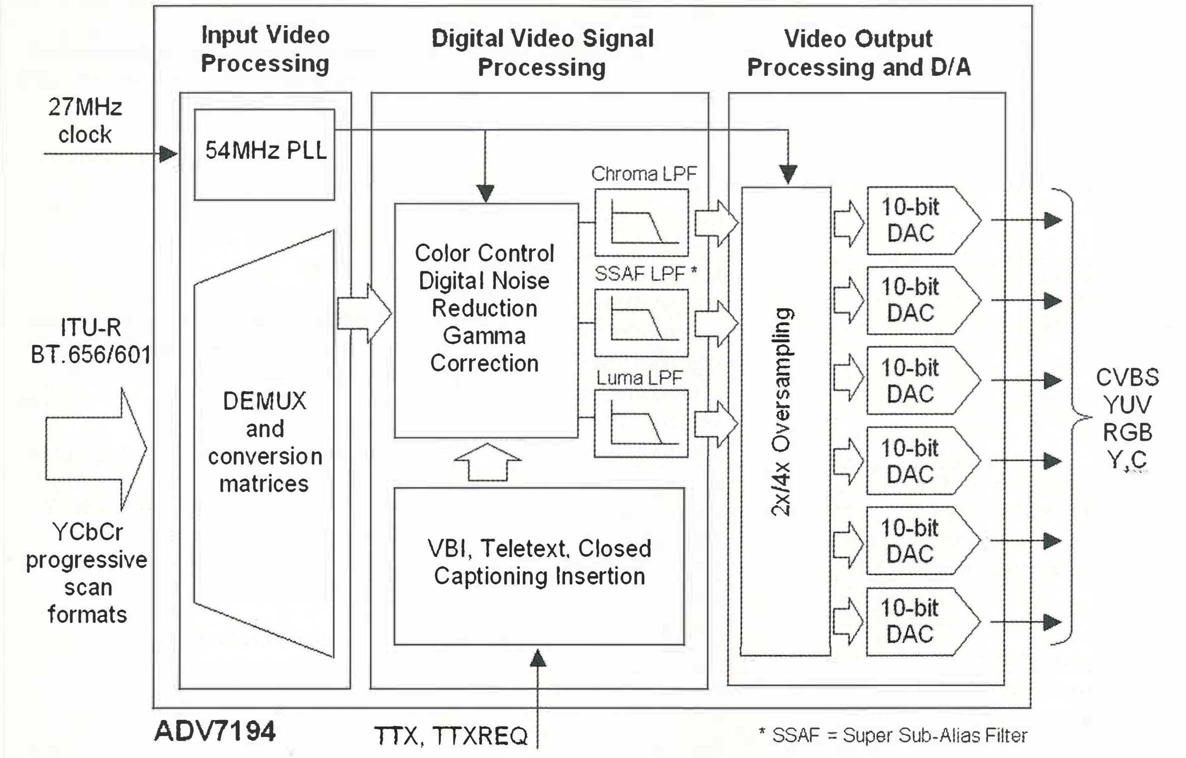


Fig. 5. Internal Structure of the ADV7194 advanced video encoder.

power supply pins for the analogue and digital ground and analogue and digital +3.3/+5V power supply. These are connected to the common power supply of the device with the aid of proper filtering achieved with C13-C20 power supply decoupling capacitors.

Main features of the ADV7194 extended encoder

The ADV7194, unlike the ADV7176 used in the SDIC08 device, has much more advanced features to allow for full user control over the characteristics of the output video signal. A simplified block diagram of the internal structure of the IC is provided in Fig. 5. I will try to summarise what the encoder chip can do without going down into detail, which will only distract the reader from the general idea of the project. If more detailed information should be obtained please refer to the manufacturers datasheet listed in the references[2].

Brightness detect: The ADV7194 can detect the average brightness of the video picture and this information is stored in its internal registers. Based on this information the user firmware (I encourage the readers to propose algorithms for making this strong feature useful) can adjust the saturation, contrast and brightness to compensate for very dark pictures automatically. In the design proposed this information is not used, but the hardware implementation will allow for firmware upgrades.

Chroma/Luma delay: The Luma pixel data can be delayed for maximum six clock cycles at 27MHz and the chroma information for maximum eight cycles. This feature can be programmed through the terminal interface of the device. The meaning of the term 'delay' of the corresponding video component becomes clear from the illustration (not to scale to an original video signal – provided only for simplification of the explanation), presented in **Fig. 6.**

Colour Bar Generator: The encoder chip has an internal 100/7.5/75/7.5 colour bar generator for NTSC and 100/0/75/0 colour bar generator for

Table 1. SDIC08 Encoder configuration command set

Command Group	Operation	Mnemonics
Default Configuration	Loads the factory preset configuration	DEFAULT
Standard Selection	PAL (BDGHI), sync on RGB (default)	R00D61, R02DCB, R03D8A, R04D09, R05D2A
	PAL (BDGHI), no sync on RGB	R00D41, R02DCB, R03D8A, R04D09, R05D2A
	NTSC, sync on RGB	R00D60, R02D16, R03D7C, R04DF0, R05D21
	NTSC, no sync on RGB	R00D40, R02D16, R03D7C, R04DF0, R05D21
Embedded Colour Bar Generator	Colour Bar Generator OFF (default)	R01D00
	Colour Bar Generator ON	R01D80
Luma Delay Control	0 ns delay on the luminance path (default)	R07D08
	74 ns delay on the luminance path	R07D18
	148 ns delay on the luminance path	R07D28
	222 ns delay on the luminance path	R07D38

Table 2. SDIC10 Encoder configuration command set

Command Group	Operation	Mnemonics
Default Configuration	Loads the factory preset configuration	DEFAULT
Standard Selection	Input Standard PAL (BGHID), (default)	R00D11 R0CDCB, R0DD8A, R0ED09, R0FD2A
	Input Standard NTSC (M)	R00D10 R0CD16, R0DD7C, R0EDF0, R0FD21
Luma Filter Selection	Low Pass PAL Notch PAL Low Pass NTSC Notch NTSC Extended Mode CIF QCIF	R00Dxxx001xx, R07D0F R00Dxxx011xx, R07D0F R00Dxxx000xx, R07D0F R00Dxxx010xx, R07D0F R00Dxxx100xx, R07D1F R00Dxxx101xx, R07D0F R00Dxxx110xx, R07D0F
Chroma Filter Selection	1.3MHz Low Pass Filter 0.65MHz Low Pass Filter 1.0MHz Low Pass Filter 2.0MHz Low Pass Filter CIF QCIF 3.0MHz Low Pass Filter	R00D000xxxxx R00D001xxxxx R00D010xxxxx R00D011xxxxx R00D101xxxxx R00D110xxxxx R00D111xxxxx
Oversampling Control	2x oversampling (default) 4x oversampling	R01D38 R01D78
Output Control	YUV Output (only if switch is set to YUV/RGB) RGB Output (only if switch is set to YUV/RGB)	R02D61 R02D60
Colour Bar Generator Control	Colour Bar Generator OFF (default) Colour Bar Generator ON	R04D00 R04D40
RGB Sync Control	Sync on all RGB-outputs (default) No Sync on RGB-outputs	R05D08 R05D00
Gamma, DNR, Resolution Control	Gamma Control	R08Dx0xx0100 – Gamma Correction OFF
		R08D01xx0100 – Gamma Curve A R08D11xx0100 – Gamma Curve B
	Digital Noise Reduction Control	R08Dxx0x0100 – DNR disable R08Dxx1x0100 – DNR enable
	Resolution Control	R08Dxxx00100 – 8-Bit Resolution R08Dxxx10100 – 10-Bit Resolution
Chroma Delay Control	Chroma Delay = 0ns	R09D0000xx00
	Chroma Delay = 148ns	R09D0001xx00
	Chroma Delay = 296ns	R09D0010xx00
Blackburst on Luma Control (in CVBS-mode)	Blackburst on Luma disabled Blackburst on Luma enabled	R09D00xx0x00 R09D00xx1x00
Blackburst on Y Control (in RGB/YUV-mode)	Blackburst on Y disabled Blackburst on Y enabled	R09D00xxx000 R09D00xxx100
Luma Delay Control	Luma Delay = 0ns (default)	R0AD08
	Luma Delay = 74ns	R0AD18
	Luma Delay = 148ns	R0AD28
	Luma Delay = 222ns	R0AD38
Contrast Control	Scaling of the Y-value Range = 0.0 – 1.5 XX = value x 128	R1DDXX R1DD80 (default) R1DD00 – contrast = 0 R1DDC0 – contrast = 1.5
Color Control	Scaling of the U-value U-register value XX = Scale Factor x 128, range = 0.0 - 2.0	R1EDXX R1ED80 (default)

PAL. The generator can be switched on and off through software (terminal program or GUI) when writing an appropriate value to a mode register (please refer to the command set table listed later in the article).

Chroma Burst switching ON/OFF: The chroma burst can be removed from the composite or chroma signal, which is again programmable in software.

Contrast Control: The Y-input data (luminance) can be scaled to influence the contrast of the picture between 0% and 100%.

Brightness Control: The brightness control is achieved through adding a programmable set-up level to the Y-data. The range for NTSC without pedestal and for PAL is between –7.5 and +15 IRE.

Colour Saturation: The colour information (U and V components) can be independently scaled by a factor, programmed in an internal device register and accessible through terminal commands. The range is between 0% and 200%.

Hue Adjust Control: Through shifting the phase of the video chroma information relative to the colour burst it is possible to control the hue of the signal in the range ±22°.

Digital Noise Reduction (DNR): This control works only on the luma information of the signal Y. The high-frequency, low-amplitude components of the signal are evaluated. They are compared to a programmable threshold value. Depending on the mode of operation selected – DNR Mode or DNR Sharpness Mode – a programmable amount is subtracted from all values under the threshold value to remove the noise or added to the values above threshold to sharpen the image. As in the most widely used configurations the input to the video encoder will come from an MPEG2 or MPEG1 decoder (providing SDI-output) the resulting video information will show the characteristic blockiness with the sizes 8x8 (MPEG2) or 16x16 (MPEG1). In this case the noise will be concentrated on the border areas between blocks and the DNR can be applied selectively in this region. It is possible to program through register access the size of the block, its position through pixel shift and the dimensions of the border area. This is a very powerful feature of the

	Scaling of the V-value V-register value XX = Scale Factor x 128, range = 0.0 - 2.0		R1FDXX R1FD80 (default)	
Hue Adjust Control	Hue Register Value = (value degree in decimal) / 0.17578125 +128 -> transform to hex to obtain XX Range: +/- 22.5° phase in 0.17578125° increments		R20DXX R20D80 (default)	
Brightness Control	0xxxxxxx = 7-bit brightness IRE value = |IRE_value| x 2.015631 > convert to hex, if negative two's complement Range: -7.5 IRE – 15 IRE		R21D0xxxxxxx R21D00 (default)	
Sharpness Control	(Value in dB + 4) x 1.5 -> convert to hex Range: -4dB - +4dB in 0.75dB steps		R22DXX R22D06 (default) R22D00 = -4dB R22D0C = +4dB	
Digital Noise Reduction	Mode (see DNR mode select)		Coring gain data	Coring gain border
	Sharpness	DNR	R23DxxxxX	R23DXxxxx
	0dB	0dB	R23D00	
	+1/16	-1/8	R23D11	
	+2/16	-2/8	R23D22	
	+3/16	-3/8	R23D33	
	+4/16	-4/8	R23D44	
	+5/16	-5/8	R23D55	
	+6/16	-6/8	R23D66	
	+7/16	-7/8	R23D77	
	+8/16	-1	R23D88	
Block Size Control	8 pixels (default)		R24D0xxxxxxx	
	16 pixels		R24D1xxxxxxx	
Border Area Control	Border Area = 2 pixels (default)		R24Dx0xxxxxx	
	Border Area = 4 pixels		R24Dx1xxxxxx	
DNR Threshold Control	Threshold = dddddd Range: 0 – 62 Default = 32		R24Dxxdddddd	
Block Offset Control	dddd=0000 -> 0 pixels offset .... dddd=1111 -> 15 pixels offset		R25Ddddxxxx	
DNR Mode Select	DNR mode		R25Dxxxx0xxx	
	Sharpness mode		R25Dxxxx1xxx	
DNR Input Filter Select Control	No filter (default)		R25Dxxxxx000	
	Filter A		R25Dxxxxx001	
	Filter B		R25Dxxxxx010	
	Filter C		R25Dxxxxx011	
	Filter D		R25Dxxxxx100	
Programmable Gamma Correction Control A-Curve Range: 0.3 – 1.8	Location (x input value)		RXXDYY, YY = Y value	
	32: Y=((16/224)^Gamma) x 224 +16		R26DYY, R26D20 (default)	
	64: Y=((48/224)^Gamma) x 224 +16		R27DYY, R27D40 (default)	
	96: Y=((80/224)^Gamma) x 224 +16		R28DYY, R28D60 (default)	
	128: Y=((112/224)^Gamma) x 224 +16		R29DYY, R29D80 (default)	
	160: Y=((144/224)^Gamma) x 224 +16		R2ADYY, R2ADA0 (default)	
	192: Y=((176/224)^Gamma) x 224 +16		R2BDYY, R2BDC0 (default)	
	224: Y=((208/224)^Gamma) x 224 +16		R2CDYY, R2CDE0 (default)	
Programmable Gamma Correction Control B-Curve Range: 0.3 – 1.8	Location (x input value)		RXXDYY, YY = Y value	
	32: Y=((16/224)^Gamma) x 224 +16		R2DDYY, R2DD20 (default)	
	64: Y=((48/224)^Gamma) x 224 +16		R2EDYY, R2ED40 (default)	
	96: Y=((80/224)^Gamma) x 224 +16		R2FDYY, R2FD60 (default)	
	128: Y=((112/224)^Gamma) x 224 +16		R30DYY, R30D80 (default)	
	160: Y=((144/224)^Gamma) x 224 +16		R31DYY, R31DA0 (default)	
	192: Y=((176/224)^Gamma) x 224 +16		R32DYY, R32DC0 (default)	
	224: Y=((208/224)^Gamma) x 224 +16		R33DYY, R33DE0 (default)	

ADV7194, which makes the device very useful as a noise reduction module in MPEG1/2 systems.

Gamma Correction Control: Gamma correction can be performed on the luma data and the user is allowed to program two independent Gamma-correction curves – curve A and curve B.

4x and 2x oversampling: All six DACs of the ADV7194 can work with a 27MHz sample clock, which is called 2x mode of operation. The IC incorporates an internal PLL, which when enabled will produce a 54MHz clock signal for the DACs and this mode of operation is called 4x mode. As the Nyquist sampling theorem states with increasing the sampling rate the aliased images in the output spectrum of the analogue video signal move further to the high frequency region. So it is usually easier to implement low-pass filtering on a higher sample rate reconstructed analogue signal. The output anti-image filter is a simpler one in 4x mode of operation. The 2x and 4x modes can be switched in software control through terminal commands. In **Fig. 7.** the function of (and requirements to) the output filters in both modes of operation (with and without oversampling) are presented.

Main features of the simpler ADV7176 encoder

The ADV7176 is a simpler video encoder compared to the ADV7194. Like the enhanced one it has an internal 32-bit DDS (Direct Digital Synthesis) synthesiser for the colour subcarrier. It has a build-in video pattern generator, which can be used for measurement tasks. The IC provides several low-pass, notch and extended filter responses, which can be applied on the luma information. Through the internal registers of the device VBI (Vertical Blank Interval) data can be inserted into the vertical sync corresponding data positions. From the signal processing functions specific to the ADV7194 only the programmable delay, which can be applied to the luma path, should be mentioned. Despite of the limited number of functions available to the user to control the output video signal, the ADV7176 proves to be a very reliable device, which is very easy to manage and very reliable to use. If a cheaper but reliable operation is the key factor for the choice between the SDIC08 and SDIC10 devices I would recommend the SDIC08. If many advanced

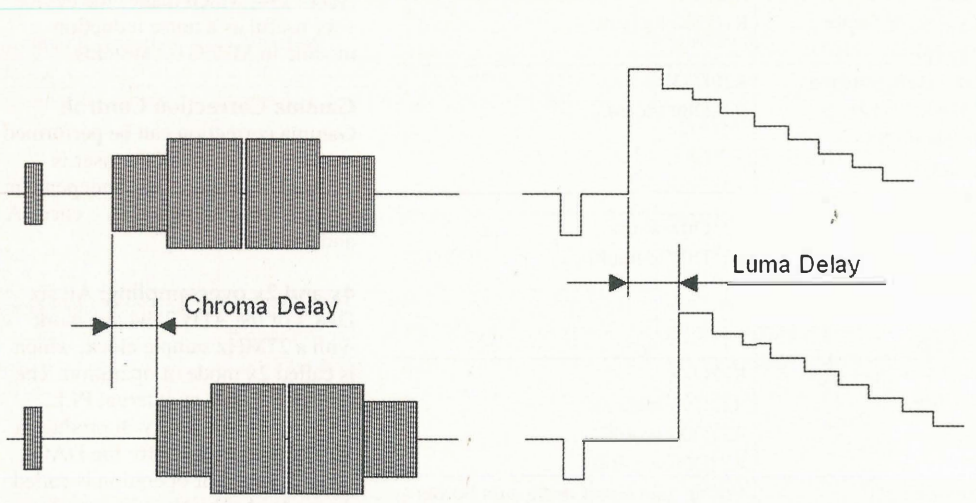


Fig. 6. Luma and Chroma Information delay programmable in software.

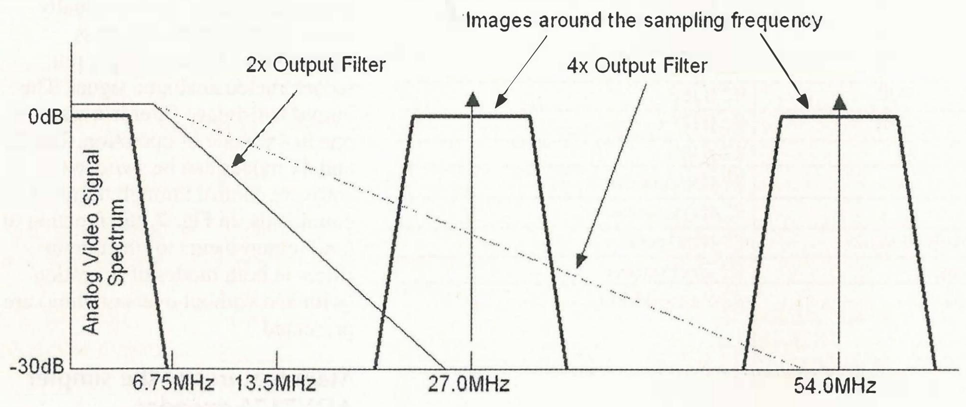


Fig. 7. Anti-imaging output filters function in 2x and 4x oversampled mode of operation.

Table 3: Luminance and Chrominance Filter Selections

Luminance Filter Specifications (4x oversampling)

Filter Type	Passband Ripple (dB)	3dB Bandwidth (MHz)
Low-Pass (NTSC)	0.16	4.24
Low-Pass (PAL)	0.1	4.81
Notch (NTSC)	0.09	2.3 / 4.9 / 6.6
Notch (PAL)	0.1	3.1 / 5.6 / 6.4
Extended (SSAF)	0.04	6.45
CIF	0.127	3.02
QCIF	Monotonic	1.5

Chrominance Filter Specifications (4x oversampling)

Filter Type	Passband Ripple (dB)	3dB Bandwidth (MHz)
1.3 MHz Low-Pass	0.09	1.395
0.65 MHz Low-Pass	Monotonic	0.65
1 MHz Low-Pass	Monotonic	1.0
2 MHz Low-Pass	0.048	2.2
3 MHz Low-Pass	Monotonic	3.2
CIF	Monotonic	0.65
QCIF	Monotonic	0.5

features of the ADV7194 are the goal of the application I will suggest the SDIC10. As with many other fields in life the decision depends upon what you want in your specific needs – what is absolutely necessary for one application may be treated as needless splendour in another not so demanding one. The internal structure of the ADV7176 encoder is depicted in **Fig. 8.** and this diagram provides far more detail than the diagram for the ADV7194 in Fig. 5[1]. It should be noted that this detailed structure is also inherent to the ADV7194 device, but is not presented due to lack of space, consumed by the other features of the enhanced encoder. From the structure in Fig. 8 the composition of the Composite Video Signal (CVBS) becomes very clear and also the colour subcarrier generation by the use of a Direct Digital Synthesis techniques (DDS) is visible.

How to configure the encoders

As with all other devices which I have recently published in *EW* there is a dedicated instruction set to control the devices through the serial interface (with the settings: 9600,8,N,1). In an earlier article about the CSDI10 decoder I described a very powerful concept, which allows the user to write to any register of the integral encoders in the units whatever value he/she finds appropriate. Despite of the fact that writing inappropriate values can result in a mis-configured or not working device (not permanently of course!), this idea allows for easy device upgrades and the implementation of new features of the integrated circuits without the need of modifying the hardware. This concept works for the two encoders SDIC08 and SDIC10 too. The general syntax of the commands is the same: first 'R' to indicate that the following ASCII-Hex value is the register subaddress in the IC and then 'D' to present the value to be written as the next ASCII-Hex value. So the command looks like: **RXXDXX** + Carriage Return + Line Feed. XX denotes an ASCII hex value – 7E for example. Of course also the salvage command 'DEFAULT' is presented in the command set, which returns the device to a factory preset condition after the user has changed so many registers in so many ways that everything refuses to work. Every command (strictly speaking every data value for the corresponding register subaddress) is not only executed (becomes active) but also is stored in the internal non-volatile memory to be executed at next start-up of the device. The power-on sequence of the devices involves outputting the active configuration on the serial communication port, so that the configuration can be identified and analysed with a simple terminal program. After the successful execution of every command the 'OK' message is returned from the encoders to the host PC. The command set for the SDIC08 is presented in **Table 1** and that of the SDIC10 encoder – in Table 2. The commands in **Table 2,** which incorporate strings like xxx001xx, are binary representations of the register values, as the x (lower case) are set by other commands. Please compile all x to a valid binary word and translate it to ASCII-hex before entering the command to the device. Obviously the commands for the SDIC10 are far more complicated and are often composed from many

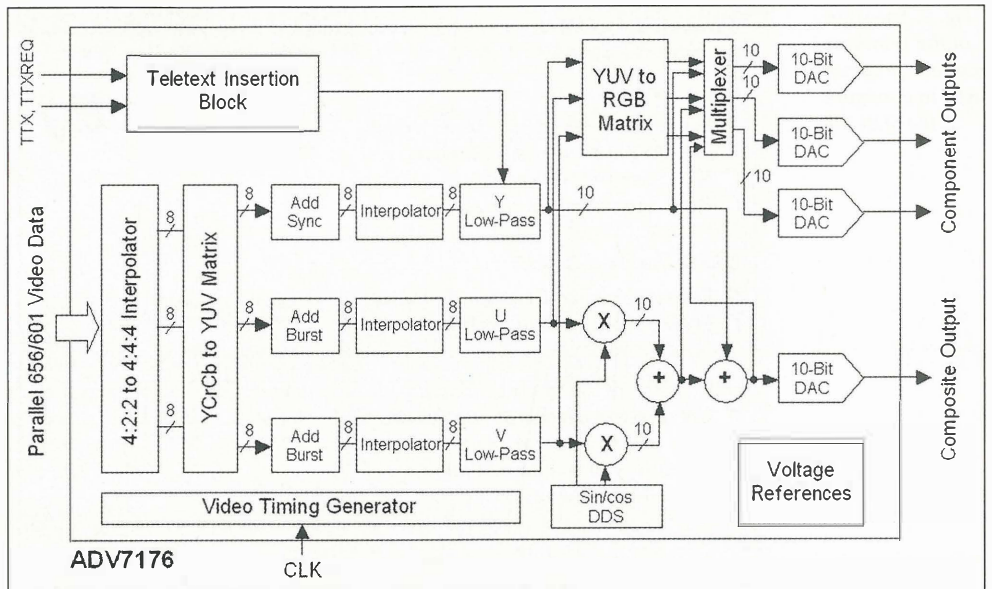


Fig. 8. Internal functional structure of the ADV7176 video encoder.

Technical specifications of the SDIC08 encoder

Main Features:

ITU-R BT601/656 YCrCb to PAL/NTSC Video Encoder;
High Quality 10-bit Video DACs, 70dB Video SNR;
32-bit Direct Digital Synthesizer for the Colour Subcarrier;
Multi-standard Video Output Support – Composite (CVBS), Component YUV and Component RGB;
Programmable Luma Filters (Low-Pass/Notch/Extended);
Programmable Luma Delay;
Input Equalizer with superior jitter performance – equalizes up to 300+ meters of Belden 8281 coaxial cable;
Data Retimer/Reclock PLL onboard – provides for removing of excessive jitter at the input SDI signal;
Carrier Detect Indicator on the Front/Back Panel;
Onboard Colour Bar Generator switchable through the Configuration RS-232 Interface;
Simple Reconfiguration through the integrated Serial RS-232 Interface and ASCII Terminal Commands / Configuration GUI;

Video Serial Digital Inputs

Applicable Standards	ITU-R BT.601/656
Format	EBU Tech 3267-E and SMPTE 259M-C
Number of Inputs	1 BNC
Input Impedance	75 Ω
Sampling	4:2:2, 8 bit
Line/field rate	525/60 and 625/50
Return Loss	>19dB, 5-270MHz
Cable Equalization	0-250m (Belden 8281)
Data Rate	270Mbps
Data jitter	180ps for 270Mbps data passed through 200m of Belden 8281 cable

Output Levels YUV (SMPTE/EBU)

Level Y	1V p-p
Level U,V	±350mV, 75% saturation

Output Levels RGB

RGB	700mV p-p non-composite
RGB	1V p-p composite (sync)

Output Standards

PAL-B, D, G, H, I, PAL-M, NTSC

Video Performance

Impedance	75Ω BNC
Return Loss	>35dB to 5.5MHz
Hue Accuracy	1.0 Degree
Colour Saturation Accuracy	1.2%
Luminance Nonlinearity	< 1.1%
S/N Ratio	> 68dB unweighted (10k-5MHz)
Differential Gain	0.4%
Differential Phase	0.4 Degree

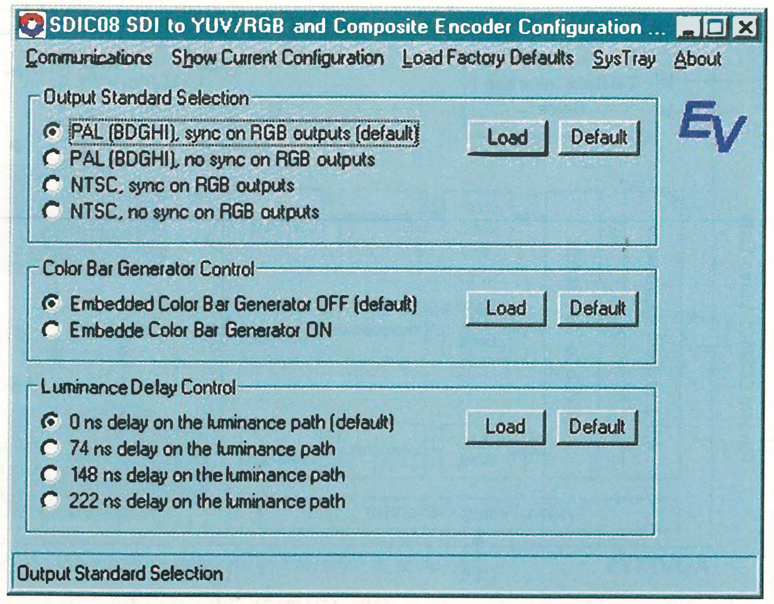
Frequency Response (PAL Mode)

Y Stopband Cutoff > 50dB Attenuation	7.4MHz
Y Passband Cutoff > 3dB Attenuation	5MHz
Chroma Stopband Cutoff > 40dB Attenuation	4MHz
Chroma Passband Cutoff > 3dB Attenuation	2.4MHz

Power Requirements

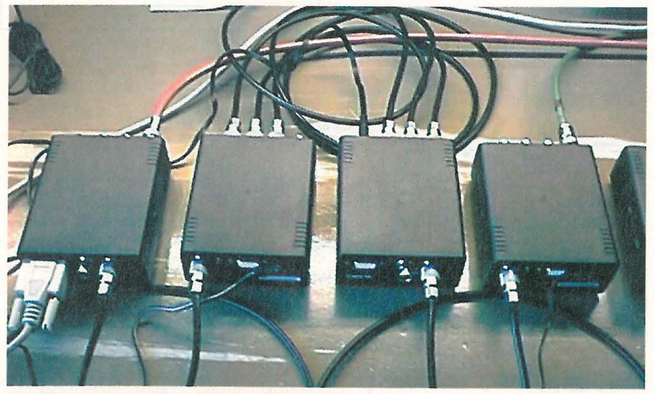
Power	9-12 VDC, 600mA
Mechanical & Climatic	
Height	45 mm (1.75 inches)
Width	90 mm (3.5 inches)
Depth	130 mm (5 inches)
Weight	0.2 Kg
Temperature	+5°C to +35° C
Humidity	96% maximum

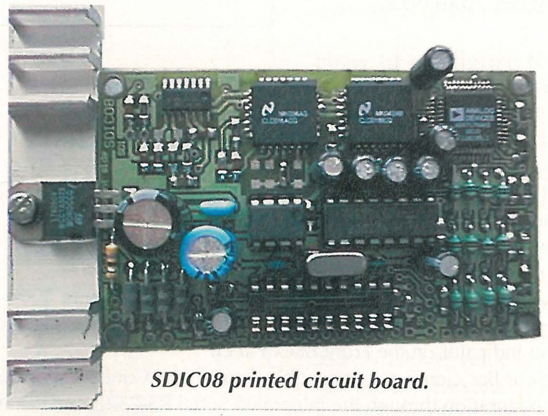
Fig. 9. Snapshot of the Windows interface program used to configure the SDIC08.



registers, controlling different functions of the device. The table lists all possible combinations but extreme care is advised when compiling valid commands from the individual register bits.

There is the option to control the SDIC08 device from a simple interface program running under Win9x on the host PC. A snapshot from this GUI program is provided in **Fig. 9.** It allows the user to change the output video signal standard, to control the internal video test pattern generator and to insert a delay in the luma path of the signal. I have not written an interface for the SDIC10 as it has so many options that such an interface in my opinion will look too crowded to be of any use. Of course the readers are encouraged to develop their own interfaces on the basis of


Cascaded operation of the encoders/decoders.


SDIC08 printed circuit board.

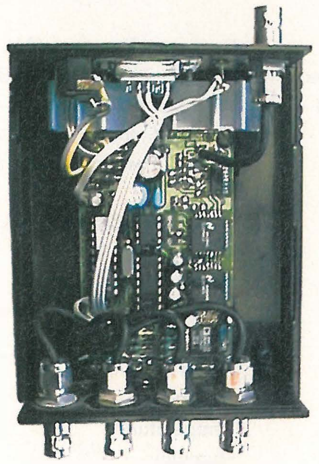
SDIC08 back panel view.

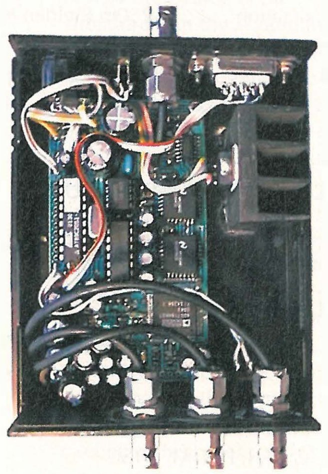
SDIC10 front panel view.

SDIC10 back panel view.

SDIC08 front panel view.

Fig. 10. Device photos.


SDIC08 open case.


SDIC10 open case.

Technical specifications of the SDIC10 encoder

Main Features:

ITU-R BT601/656 YCrCb to PAL/NTSC Video Encoder;
High Quality 10-bit Video DACs, 70dB Video SNR;
4 x Oversampling with Internal 54MHz PLL;
On-board Super Subalias Filter (SSAF);
Digital Noise Reduction for reducing MPEG-systems block artefacts;
32-bit Direct Digital Synthesizer for the Colour Subcarrier;
Multi-standard Video Output Support – Composite (CVBS), Component YUV, Component RGB, Luma and Chroma;
Multiple Luma and Chroma filters;
Programmable Luma and Chroma Delay;
Programmable Gamma Correction – 2 different user-defined Gamma Curves A and B selectable;
Brightness, Contrast, Colour, Hue and Sharpness Control;
Input Equalizer with superior jitter performance – equalizes up to 300+ meters of Belden 8281 coaxial cable;
Data Retimer/Reclock PLL onboard – provides for removing of excessive jitter at the input SDI signal;
Carrier Detect Indicator on the Front/Back Panel;
Onboard Colour Bar Generator switchable through the Configuration RS-232 Interface;
Simple Reconfiguration through the integrated Serial RS-232 Interface and ASCII Terminal Commands / Configuration GUI;

Table 3: Luminance and Chrominance Filter Selections

Luminance Filter Specifications (4x oversampling)

Filter Type	Passband Ripple (dB)	3dB Bandwidth (MHz)
Low-Pass (NTSC)	0.16	4.24
Low-Pass (PAL)	0.1	4.81
Notch (NTSC)	0.09	2.3 / 4.9 / 6.6
Notch (PAL)	0.1	3.1 / 5.6 / 6.4
Extended (SSAF)	0.04	6.45
CIF	0.127	3.02
QCIF	Monotonic	1.5

Chrominance Filter Specifications (4x oversampling)

Filter Type	Passband Ripple (dB)	3dB Bandwidth (MHz)
1.3 MHz Low-Pass	0.09	1.395
0.65 MHz Low-Pass	Monotonic	0.65
1 MHz Low-Pass	Monotonic	1.0
2 MHz Low-Pass	0.048	2.2
3 MHz Low-Pass	Monotonic	3.2
CIF	Monotonic	0.65
QCIF	Monotonic	0.5

Contrast Control Range:	0.0 ÷ 1.5
Colour Control Range (U-, V-scaling):	0.0 ÷ 2.0
Hue Adjust Control:	± 22.5°
Brightness Control:	-7.5 IRE ÷ 15 IRE
Sharpness Control: (applicable only if Luma filter is in Extended Mode)	-4dB ÷ +4dB
Luma Delay Control Range:	0 ns ÷ 222 ns
Chroma Delay Control Range:	0 ns ÷ 296 ns

Video Serial Digital Inputs

Applicable Standards	ITU-R BT.601/656
Format	EBU Tech 3267-E and SMPTE 259M-C
Number of Inputs	1 BNC
Input Impedance	75W
Sampling	4:2:2, 10 bit
Line/field rate	525/60 and 625/50
Return Loss	>19dB, 5-270MHz
Cable Equalization	0-250m (Belden 8281)
Data Rate	270Mbps
Data jitter	180ps for 270Mbps data passed through 200m of Belden 8281 cable

Output Levels YUV (SMPTE/EBU)

Level Y	1V p-p
Level U,V	±350mV, 75% saturation

Output Levels RGB

RGB	700mV p-p non-composite
RGB	1V p-p composite (sync)

Output Standards

PAL-B, D, G, H, I, PAL-N, NTSC-M, NTSC-N, PAL-60

Video Performance

Impedance	75Ω BNC
Return Loss	>35dB to 5.5MHz
Hue Accuracy	0.5 Degree
Colour Saturation Accuracy	0.7 %
Luminance Nonlinearity	< 0.6 %
S/N Ratio > 70dB unweighted	(10kHz - 5MHz)
Differential Gain	0.4%
Differential Phase	0.4 Degree
Chroma Nonlinear Gain	0.7%
Chroma Nonlinear Phase	0.5 Degree
Chroma AM noise	82dB
Chroma PM noise	72dB

Power Requirements

Power	9-12 VDC, 600mA

Mechanical & Climatic

Height	45mm (1.75 inches)
Width	90mm (3.5 inches)
Depth	130mm (5 inches)
Weight	0.225 Kg
Temperature	+5°C to +35° C
Humidity	96% maximum

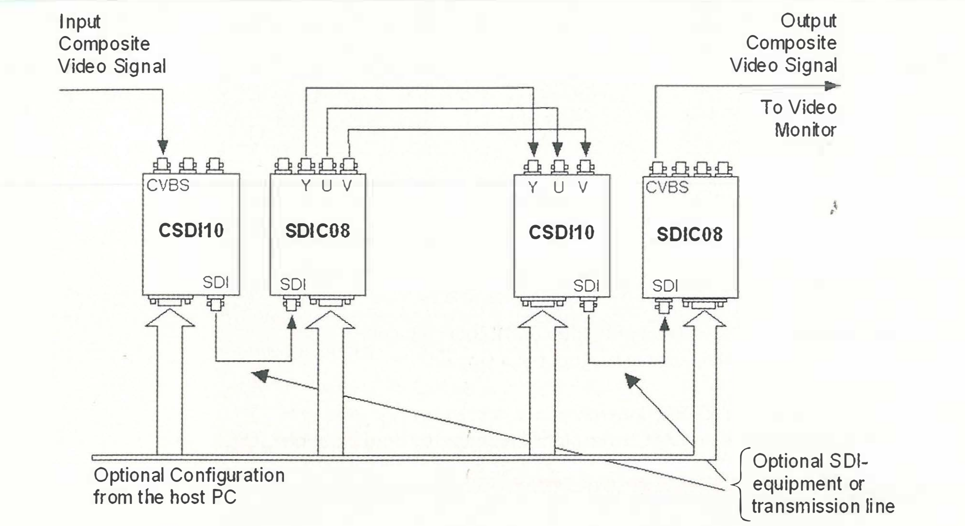


Fig. 11. Cascaded measurement set-up for the SDIC08 encoder and the CSDI10 decoder.

the provided detailed command set and possibly these programs will include only the commands which are suitable for the particular application of the encoder.

Firmware, Software and Printed Circuit Boards

The listings of the code residing inside the 89C2051 microcontrollers are long with detailed comments but unsuitable for publishing due to the large space they will occupy. Also I think they will not significantly contribute to the aim that the reader should obtain a generalised view of the device technology, applications and internal structure. Of course they are one of the most important parts of the design as the hardware will not work without the firmware covering the register access to the encoder integrated circuits, the serial communications with the host PC and the command translation from ASCII-hex format to I^{2}C-compatible register address and data format. The assembly code of the program, the object code or the microcontroller – EEPROM image (bin-representation of the content) can be obtained from the *EW* editorial office. The same is true for the GUI configuration program for the SDIC08 encoder.

I have prepared dedicated 2-layer PCBs for both devices. Actually it is impossible to build the project without such PCBs as the integrated circuits involved are SMD-technology components, some of them with 80-pins (the ADV7194 encoder for example). Soldering these tiny components on a piece of universal prototyping board is not advisable (if at all possible!). The PCBs can be obtained from the *EW* office for £50 each. Please allow four weeks for delivery if they run out of stock and need to be produced.

The SDIC08 and SDIC10 encoders are housed in a plastic case as can be seen from the pictures presented in **Fig. 10.** Of course if a more rugged or reliable operation is the goal then several such encoders (combined with the decoders CSDI10) can be mounted in a 19 inch 1RU metal unit case. In such a case the power supplies of several encoder/decoder modules can be merged and a switched mode power supply in the 19'' case can be used as the primary supply. This device-casing structure is suitable for the studio environment, where usually not a single but several encoders and decoders will be implemented.

Testing the encoders/decoders

To ensure that a signal processing system is a reliable and stable one, the measurement has to be done in the so called worst case conditions. Such a condition for a video processing facility is the process of several encoding/decoding sequences, which should show a possible generation loss of quality if such exists. With the uncompressed digital video represented by the SDI stream there are no expectations for any loss of quality. Because of the sampling characteristics of the systems involved aliasing phenomena could result, so the cascaded operation is a reasonable measurement method. The first photo in Fig. 10 shows the experimental set-up I have used. The same set-up is depicted as a signal flow chart in **Fig. 11.** The input CVBS (composite) analogue video signal is converted to SDI by the first CSDI10 decoder. The SDI can be passed through a SDI switcher or through a long transmission line (to degrade intentionally the digital signal). The second converter – an SDIC08 encoder converts the SDI stream to component video (YUV). This component video signal is applied to the second CSDI10, which works in component mode in this case. The resulting SDI signal can be passed through signal degrading equipment (such a long transmission line). The final step is the back-conversion of the SDI signal to an analogue composite signal performed by the second SDIC08 converter. So we have CVB-signal at the input and CVBS at the output too. The input signal can be sourced from a test pattern generator or it can be a live video signal (which on my opinion is the better way to stress the system and to test the subjective working of the devices). The output composite signal can be viewed on a oscilloscope or on a conventional video monitor. Using the proposed experimental set-up I could not observe a visible degradation of the video material with the exception of the degradation inherent to the component-to-composite conversion (the composite signal is always a lower quality one!). This last degradation is only a feasible one – I could not observe any degradation at all. So in conclusion I will say the proposed devices allow for professional signal processing and conversion of video signals from the digital to the analogue domain and reverse. ■

References

1. Analog Devices, 'ADV7175A/ADV7176A High Quality, 10-Bit, Digital CCIR-601 to PAL/NTSC Video Encoder', Rev. C, 12/2000.
2. Analog Devices, 'ADV7194 Professional Extended-10TM Video Encoder with 54MHz Oversampling', Rev. A, 02/2001.
2. Analog Devices, 'AD8051/AD8052/AD8054 Low Cost, High Speed Rail-to-Rail Amplifiers', Rev. D, 02/2003.
4. National Semiconductor, 'CLC014 Adaptive Cable Equalizer for High-Speed Data Recovery', June 1998.
5. National Semiconductor, 'CLC016 Data Retiming PLL with Automatic Rate Selection', July 1998.
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7. Vladkov, E., 'Analyse your SDI', Electronics World, February 2002, pp. 18-28.

Electronic analogue switching

Part 2: Discrete FETs

Having looked in detail at analogue switching using CMOS gates, and having seen how well they can be made to work, you might be puzzled as to why anyone should wish to perform the same function with discrete FETs. Douglas Self explains

There are at least two advantages in particular applications. Firstly, JFETs can handle the full output range of opamps working from maximum supply rails, so higher signal levels can often be switched directly without requiring opamps to convert between current and voltage mode.

Secondly, the direct access to the device gate allows relatively slow changes in attenuation (though still measured in milliseconds, for reasons that will emerge) rather than the rapid on-off action which CMOS gates give as a result of their internal control-voltage circuitry. This is vital in creating mute circuits that essentially implement a fast fade rather than a sharp cut, and so do not generate clicks and thumps by abruptly interrupting the signal.

The downside is that they require carefully-tailored voltages to drive the gates, and these cannot always be conveniently derived from the usual opamp supply rails.

Discrete FETs in voltage mode: The series JFET switch

The basic JFET series switching circuit is shown in **Fig 15.** With the switch open there is no other connection to the gate other than the bootstrap resistor, V_{gs} is zero, and so the FET is on. When the switch is closed, the gate is pulled down to a sufficiently negative voltage to ensure that the FET is biased off even when the input signal is at its negative limit.

The JFET types J111 and J112 are specially designed for analogue switching and pre-eminent for this application. The channel on-resistances are low and relatively linear. This is a depletion-mode FET, which requires a negative gate voltage to actively turn it off. The J111 requires a more negative V_{gs} to ensure it is off, but in return gives a lower $R_{ds(on)}$ which means lower distortion.

The J111, J112 (and J113) are members of the same family- in fact they are same the device, selected for gate/channel characteristics, unless I am much mistaken. Table 4 shows how the J111 may need 10V to turn it off, but gives a 30Ω on-resistance or $R_{ds(on)}$ with zero gate voltage. In contrast the J112 needs only 5.0V at most to turn it off, but has a higher $R_{ds(on)}$ of 50Ω. The trade-off is between ease of generating the gate control voltages, and linearity. The higher the $R_{ds(on)}$, the higher the distortion, as this is a non-linear resistance.

Table 4

	J111	J112	J113
$V_{gs(off)}$ min	–3.0	–1.0	–0.5V
$V_{gs(off)}$ max	–10	–5.0	–3.0V
$R_{ds(on)}$	30	50	100

FET tolerances are notoriously wide, and nothing varies more than the V_{gs} characteristic. It is essential to take the full range into account when designing the control circuitry.

Both the J111 and J112 are widely used for audio switching. The J111 has the advantage of the lowest distortion, but the J112 can be driven directly from 4000 series logic running from ±7.5V rails, which is often convenient. The J113 appears to have no advantage to set against its high $R_{ds(on)}$ and is rarely used - I have never even seen one.

The circuits below use either J111 or J112, as appropriate. The typical version used is shown, along with typical values for associated components. **Figure 15** has Source and Drain marked on the JFET. In fact these devices appear to be perfectly symmetrical, and it seems to make no difference which way round they are connected, so further diagrams omit this. As JFETs, in practical use they are not particularly static-sensitive.

The off voltage must be sufficiently negative to ensure that V_{gs} never becomes low enough to turn the JFET on. Since a J111 may require a V_{gs} of -10V to turn it off, the

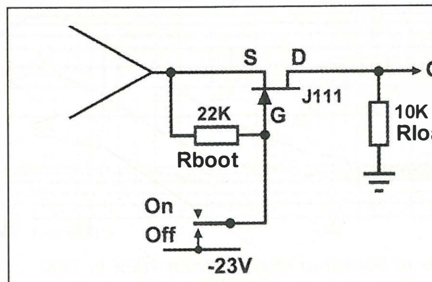


Fig. 15. The basic JFET switching circuit, with gate bootstrap resistor.

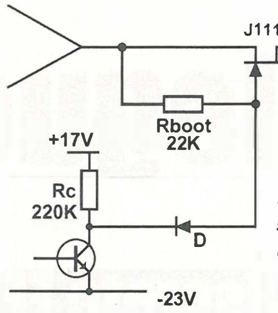


Fig. 16. The JFET switching circuit controlled by a transistor.

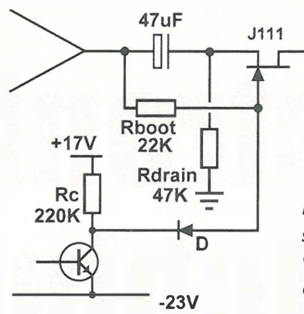


Fig. 17. The JFET switching circuit with a DC blocking capacitor.

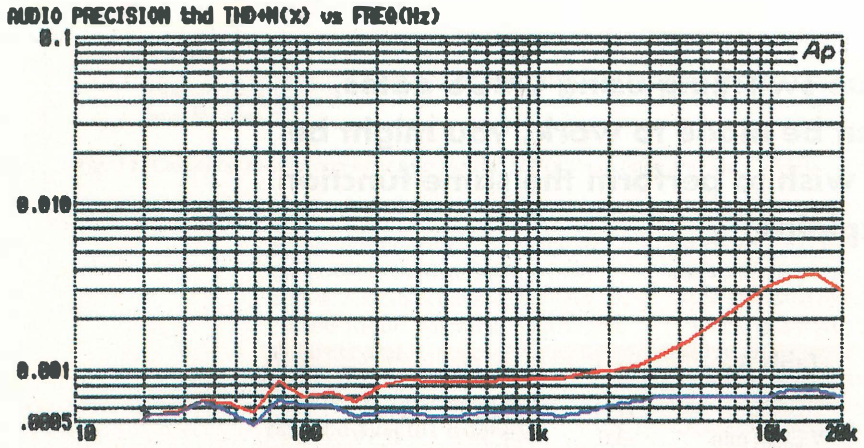


Fig 18 The JFET distortion performance with a load of 10K.

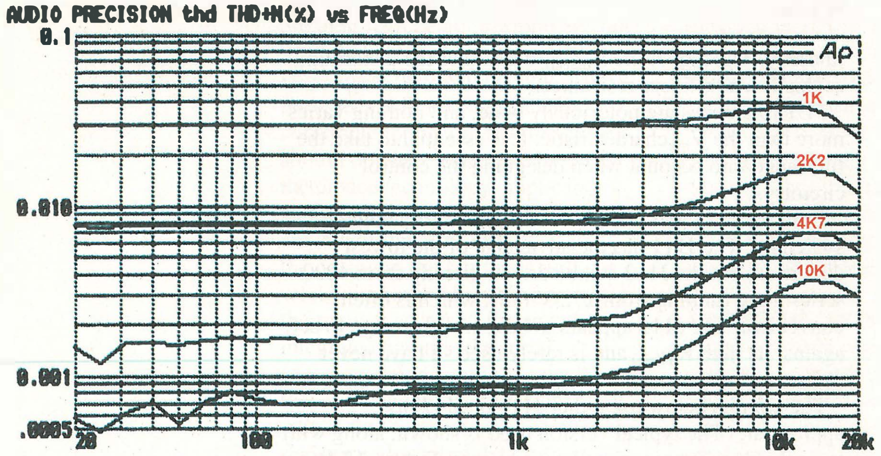


Fig. 19. The JFET THD with loads from 1K to 10K.

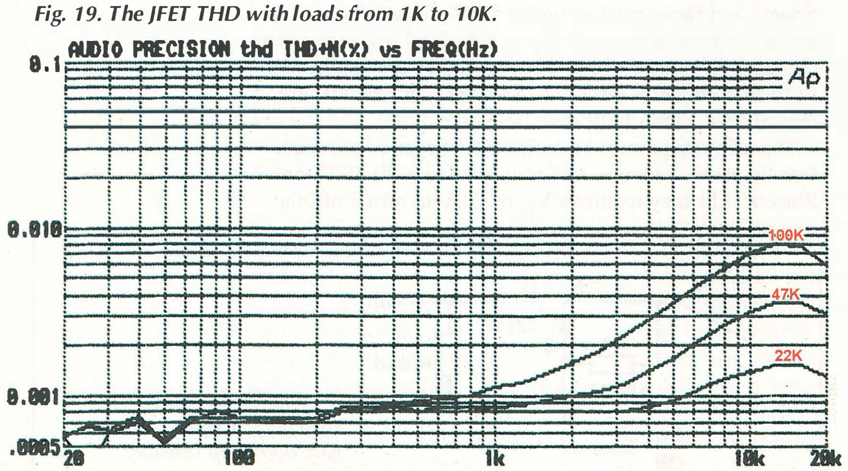


Fig. 20. The THD with different values of bootstrap resistors from 100K to 22K.

off voltage must be 10V below the negative saturation point of the driving opamp- hence the -23V rail. This is not exactly a convenient voltage, but the rail does not need to supply much current and the extra cost in something like a mixing console is relatively small. To turn a JFET on, the V_{gs} must be held at zero volts. That sounds simple enough, but it is actually the more difficult of the two states. Since the source is moving up and down with the signal, the gate must move up and down in exactly the same way to keep V_{gs} at zero. This is done by bootstrap resistor R_{boot} in Fig 15. When the JFET is off, DC flows through this resistor from the source; it is therefore essential that this path be DC-coupled and fed from a low impedance such as an opamp output, as shown in these diagrams. The relatively small DC current drawn from the opamp causes no problems.

Figure 16 is a more practical circuit using a driver transistor to control the JFET (if you had a switch contact, you would presumably use to control the audio directly). The pull-up resistor R_c keeps diode D reverse-biased when the JFET is on; this is its sole function, so the value is not critical. It is usually high to reduce power consumption. I have used anything between 47K and 680K with success.

Sometimes DC-blocking is necessary if the opamp output is not at a DC level of 0V. In this case the circuit of **Fig. 17.** is very useful; the audio path is DC-blocked but not the bootstrap resistor, which must always have a DC path to the opamp output. R_{drain} keeps the capacitor voltage at zero when the JFET is held off.

Figure 18 shows the distortion performance with a load of 10K. The lower curve is the distortion from the opamp alone; the low THD level should tell you immediately it was a 5532. The signal level was 7.75Vrms (+20dBu).

Figure 19 shows the distortion performance with heavier loading, from 10K down to 1K. As is usual in the world of electronics, heavier loading makes things worse. In this case, it is because the non-linear R_{on} becomes a more significant part of the total circuit resistance. The signal level was 7.75Vrms (+20dBu).

Figure 20 shows the distortion performance with different values of bootstrap resistor. The lower the value, the more accurately the drain follows the source at high audio frequencies, and so the lower the distortion. The signal level was 7.75Vrms (+20dBu) once again. There appears to be no disadvantage to using bootstrap resistor of 22K or so, except in in special circumstances, as explained below.

Two series JFET switches can be simply combined to make a changeover switch, as shown in **Fig. 21.** The valid states are A on, B on, or both off. Both on is not a good option because the two opamps will then be

driving each other's outputs through the JFETs.

It is possible to cascade FET switches, as in **Fig. 22.** which is taken from a real application. Here the main output is switched between A and B as before, but a second auxiliary output is switched between this selection and another input C by JFET3 and JFET 4. The current drawn by the second bootstrap resistor R_{boot2} must flow through the $R_{ds(on)}$ of the first FET, and will thus generate a small click. R_{boot2} is therefore made as high as possible to minimise this effect, accepting that the distortion performance of the JFET3 switch will be compromised at HF; this was acceptable in the application as the second output was not a major signal path. The bootstrap resistor of JFET4 can be the desirable lower value as this path is driven direct from an opamp.

The shunt JFET switch

The basic JFET shunt switching circuit is shown in **Fig 23.** Like the shunt analogue gate mute, it gives poor offness but good linearity in the ON state, so long as its gate voltage is controlled so it never allows the JFET to begin conducting. Its great advantage is that the depletion JFET will be in its low-resistance before and during circuit power-up, and can be used to mute switch-on transients. Switch-off transients can also be effectively muted if the drive circuitry is configured to turn on the shunt FETs as soon as the mains disappears, and keeps them on until the various supply rails have completely collapsed.

The circuit of **Fig. 23.** was used to mute the turn-on and turn-off transients of a hi-fi preamplifier. Since this is an output that is likely to drive a reasonable length of cable, with its attendant capacitance, it is important to keep R1 as low as possible, to minimise the possibility of a drooping treble response. This means that the $R_{ds(on)}$ of the JFET puts a limit on the offness possible. The output series resistor R1 is normally in the range 47-100Ω, when it has as its only job the isolation of the output opamp from cable capacitance. Here it has a value of 1K, which is a distinct compromise.

The muting obtained with 1K was not quite enough so two J11 1s were used in parallel, giving a further -6dB of attenuation, and yielding in total -33dB across the audio band, which was sufficient to render the transients inaudible. The offness is not frequency dependent as the impedances are all low and so stray capacitance is irrelevant.

Discrete FETs in current mode

JFETS can be used in the current mode, just as for analogue gates. **Figure 24** shows the basic muting circuit, with series FET switching only.

When switching audio signals, an instantaneous cut of the signal is sometimes not what is required. When a non-zero audio signal is abruptly interrupted there is bound to be a click. Perhaps surprisingly, clever schemes for making the instant of switching coincide with a zero-crossing give little improvement. There may no longer be a step-change in level, but there is still a step-change in slope and the ear once more interprets this discontinuity as a click.

What is really required is a fast-fade over about 10msec. This is long enough to prevent clicks, without being so slow that the timing of the event becomes sloppy. This is normally only an issue in mixing consoles, where it is necessary for things to happen in real time. Such fast-fade circuits are often called 'mute blocks' to emphasise that they are more than just simple on-off switches. Analogue gates cannot be slowly turned on and off due to their internal circuitry for control-voltage generation. Therefore discrete JFETS must be used. Custom chips to perform

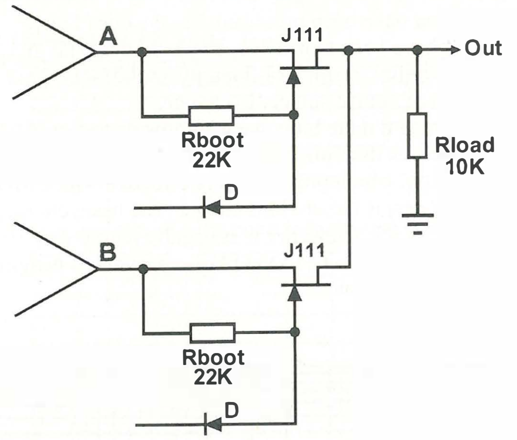


Fig. 21. The basic JFET changeover circuit.

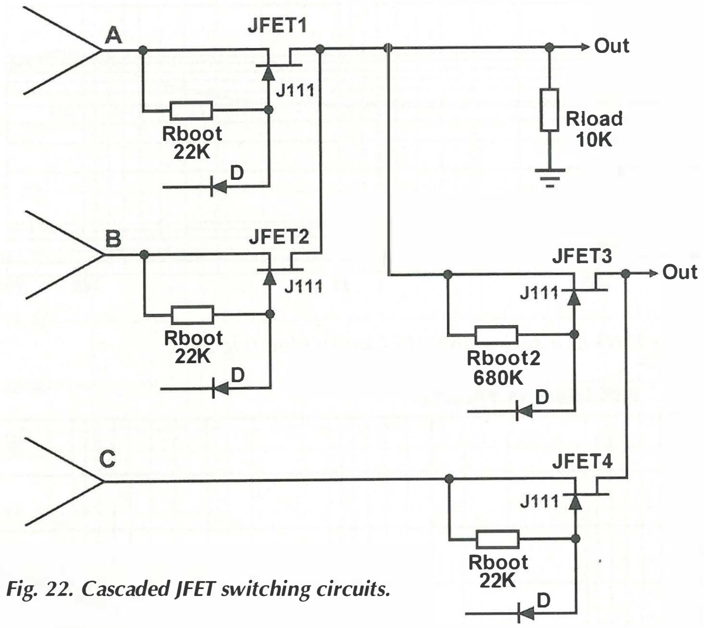


Fig. 22. Cascaded JFET switching circuits.

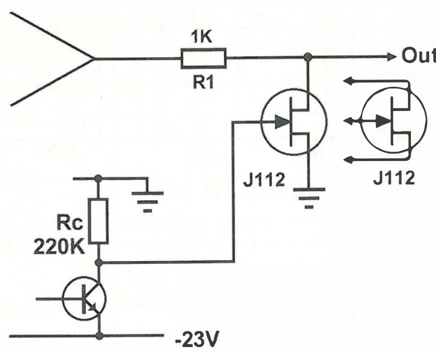


Fig. 23. The basic JFET shunt switching circuit. Adding more JFETs in parallel increases the offness, but each -6dB requires doubling the number.

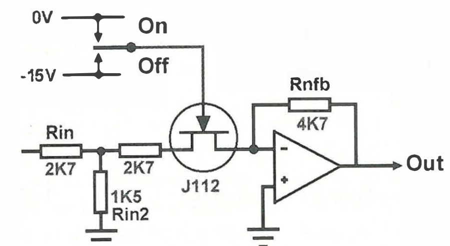


Fig. 24. Circuit of series-only JFET mute bloc. There is a crosstalk/linearity trade-off.

this function have been produced, but the ones I have evaluated have been expensive, single-source, and give less than startling results for linearity and offness. This situation is of course subject to change.

In designing a mute bloc, we want low distortion AND good offness at the same time, so the series-shunt configuration, which proved highly effective with CMOS analogue gates, is the obvious choice. The basic circuit is shown in **Fig. 27.** Capacitor C is usually required to ensure HF stability, due to the FET capacitances hanging on the summing node at D.

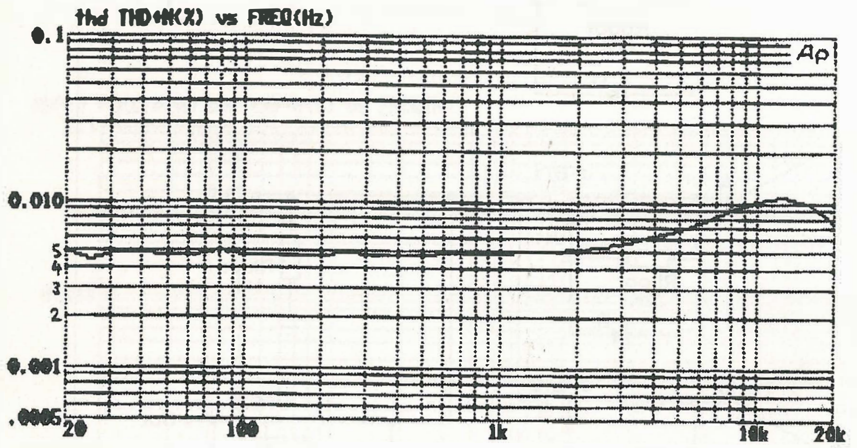


Fig. 25. The THD of a series-only JFET mute bloc (Fig 24).

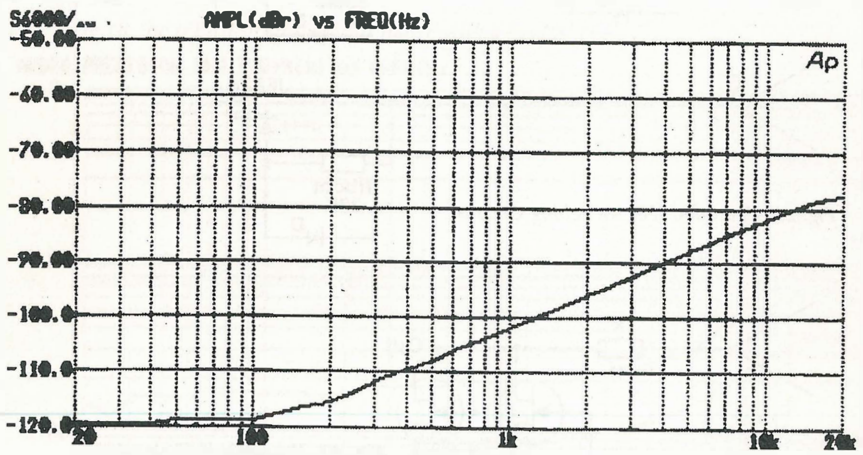


Fig. 26. Offness of a series-only mute circuit (Fig 24).

The control voltages to the series and shunt JFETs are complementary as before, but now they can be slowed down by RC networks to make the operation gradual, as shown in **Fig. 28.** The exact way in which the control voltages overlap is easy to control, but the V_{gs}/resistance law of the FET is not (and is about the most variable FET parameter there is) and so the overlap of FET conduction is rather variable. However, I should say at once that this system does work and works well enough to go in top-notch mixing consoles. As you go into the muted condition the series JFET turns off and the shunt JFET turns on, and if the overlap gets to be too much in error, the following bad things can happen:

1) If the shunt FET turns on too early, while the series JFET is still mostly on, a low-resistance path is established from the opamp VE point to ground, causing a large but brief rise in stage noise gain. This produces a 'chuff' of noise at the output as muting occurs.

2) If the shunt FET turns on too late, so the series JFET is mostly off, the large signal voltage presented to the series FET causes visibly serious distortion. I say 'visibly' because it is well-known that even quite severe distortion is not obtrusive if it occurs only briefly. The transition here is usually fast enough for this to be the case; it would not however be a practical way to generate a slow fade.

The drive circuitry

The mute bloc requires two complementary drive voltages, and these are most easily generated by 4000-series CMOS running from 7.5V rails. NAND gates are shown here as they are convenient for interfacing with other bits of control logic, but any standard CMOS output can be used. It is vital that the JFET gates get as close to 0V as possible, ensuring that the series gate can be fully on and give minimum distortion, so the best technique is to run the logic from these rails and use diodes to clamp the gates to 0V.

Thus, in Fig 28, when the mute bloc is passing signal, the signal from gate A is high, so D1 is reverse-biased and the series JFET TR1 gate is held at 0V by R1, keeping it on. (The role of R_p will be explained in a moment) Meanwhile, D2 is conducting as the NAND-gate output driving it is low, so the shunt JFET TR2 gate is at about -7V and it is firmly switched off. This voltage is more than enough to turn off a J112, but cannot be guaranteed to turn off a J111, which may require -10V (See **Table 5**). This is one reason why the J112 is more often used in this application - it is simpler to generate the control voltages. When the mute bloc is off, the

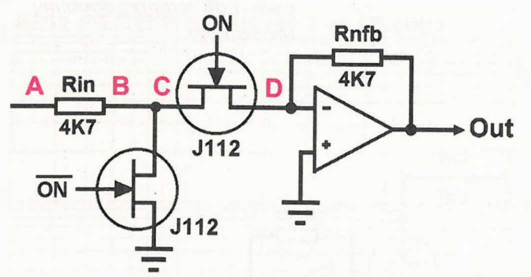


Fig. 27. Circuit of series-shunt JFET mute bloc.

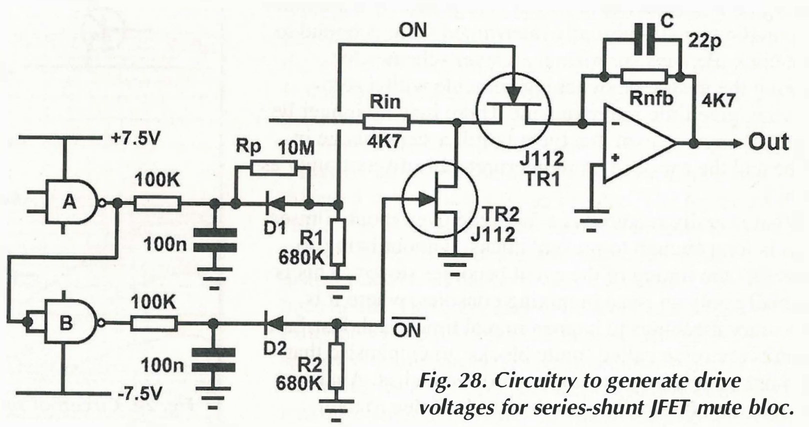


Fig. 28. Circuitry to generate drive voltages for series-shunt JFET mute bloc.

Table 5

	1kHz	10kHz	20kHz
THD dBu	0.0023%	0.0027%	0.0039%
Offness	–114dB	–109dB	–105dB

conditions are reversed, with the output of A low, turning off TR1, and the output of B high, turning on TR2 .

Reducing THD by on-biasing

The distortion generated by this circuit bloc is of considerable importance, because if the rest of the audio path is made up of 5532 opamps - which is likely in professional equipment - then this stage can generate more distortion than the rest of the signal path combined and dominate this aspect of the performance. It is therefore worth examining any way of increasing the linearity.

We have already noted that to minimise distortion, the series JFET should be turned on as fully as possible to minimise the value of the non-linear R_{ds}(on). When a JFET has a zero gate-source voltage, it is normally considered fully on. It is, however, possible to turn it even more on than this. The technique is to put a small positive voltage on the gate, say about 200 - 300mV. This further reduces the R_{ds}(on) in a smoothly continuous manner, without forward biasing the JFET gate junction and injecting DC into the signal path. This is accomplished in Fig 28 by the simple addition of R_p, which allows a small positive voltage to be set up across the 680K resistor R1. The value of R_p is usually in the 10-22 MΩ range, for the circuit values shown here.

Care is needed with this technique, because if temperatures rise the JFET gate diode may begin to conduct after all, and DC will leak into the signal path, causing thumps and bangs. In my experience 300mV is about the upper safe limit for equipment that gets reasonably warm internally, i.e. about 50°C. Caution is the watchword here, for unwanted transients are much less tolerable than slightly increased distortion.

As with analogue CMOS gates, the choice of the resistors R_{in} and R_{nfb} that define the magnitude of the signal currents is an important matter. **Figs. 30.** and **31.** examine how the offness of the circuit is affected by using values of 4K7 and 22K. Usually 4K7 would be the preferred value; choosing 22K as the value makes the noise floor higher, as well as the signal leakage. Values below 4K7 are not usual as distortion is likely to increase, as the JFET $R_{ds(on)}$ becomes a larger part of the total resistance in the circuit. The loading affect on the previous stage must also be considered.

Layout and offness

The offness of this circuit is extremely good, providing certain precautions are taken in the physical layout. In Fig 32 there are two possible crosstalk paths that can damage the offness. The path C-D, through the internal capacitances of the series JFET, is rendered innocuous as C is connected firmly to ground by the shunt JFET. However, point A is still alive with full amplitude signal, and it is the stray capacitance from A to D that defines the offness at high frequencies. Given the finite size of R_{in}, it is often necessary to extend the PCB track B-C to get A far enough from D. This is no problem if done with caution. Remember that the track B-C is at virtual earth when the mute bloc is on, and so vulnerable to capacitative crosstalk from other signals straying in to the area.

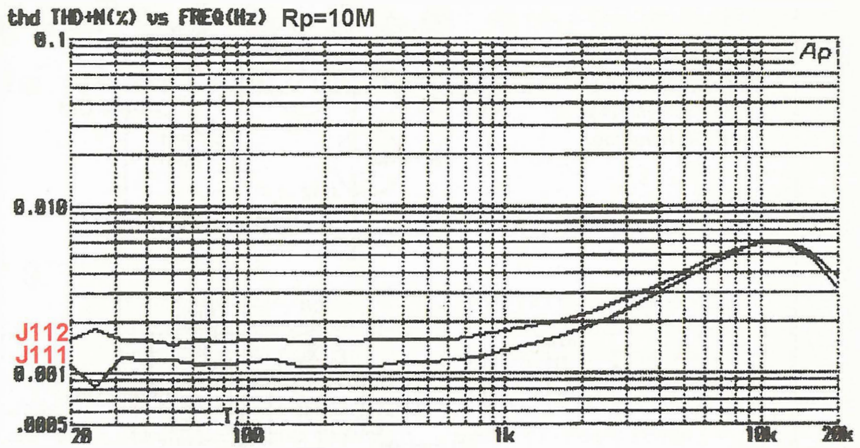


Fig. 29. The THD of the mute bloc in Fig. 27. The increase in FET distortion caused by using the J112 rather than J111 is shown.

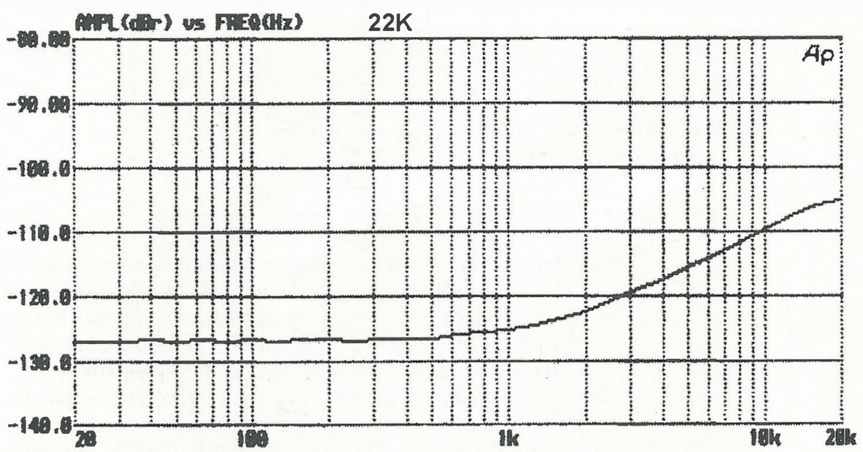


Fig. 30. The offness of a series-shunt JFET mute bloc with $R_{in} = R_{nfb} = 22K$.

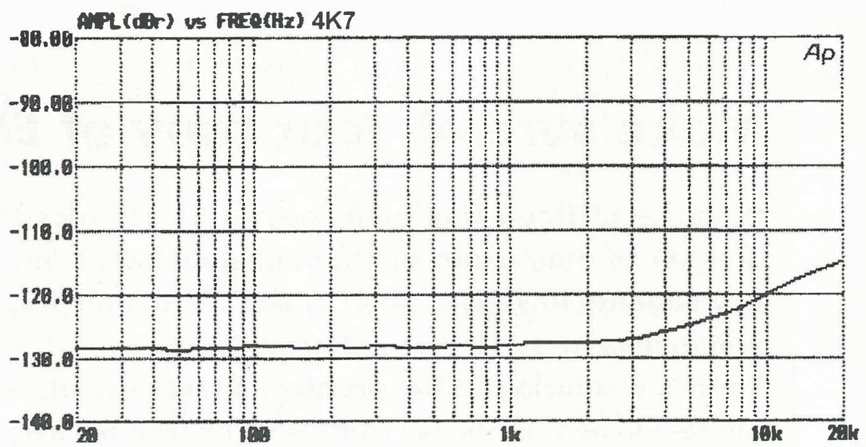


Fig. 31. The offness of a series-shunt JFET mute bloc with $R_{in} = R_{nfb} = 4K7$. Offness is better and the noise floor (the flat section below 2 kHz) has been lowered by about 2dB.

Dealing with the DC

The circuits shown so far have been stripped down to their bare essentials to get the basic principles across. In reality, things are (surprise) a little more complicated. Opamps have non-zero offset and bias voltages and currents and if not handled properly these will lead to thumps and bangs. There are several issues:

If there is any DC voltage at all passed on from the

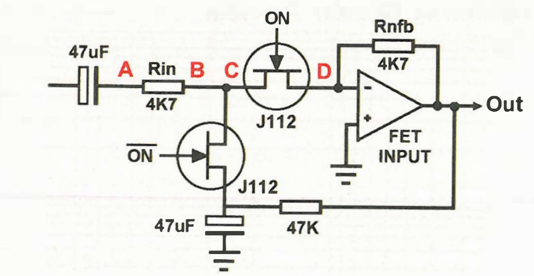


Fig. 32. Circuit of JFET mute showing stray capacitances and DC handling.

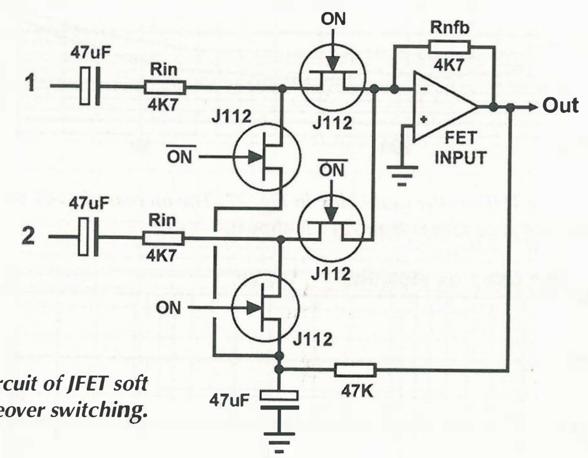


Fig. 33. Circuit of JFET soft changeover switching.

previous stage, this will be interrupted along with the signal, causing a click or thump. The foolproof answer is of course a DC blocking capacitor, but if you are aiming to remove all capacitors from the signal path, you may have a problem. DC servos can partly make up the lack, but since they are based on opamp integrators they are no more accurate than the opamp, while DC blocking is foolproof.

The offset voltage of the opamp. If the noise gain is changed when the mute operates (which it is) the changing amplification of this offset will change the DC level at the output. The answer is shown in **Fig 32.** The shunt FET is connected to ground via a blocking capacitor to prevent gain changes. This capacitor does not count as 'being in the signal path' as audio only goes through it when the circuit is muted. Feedback of the opamp offset voltage to this capacitor renders it innocuous.

The input bias and offset currents of the opamp. These are much more of a problem and are best dealt with by using JFET opamps such as the OPA2134, where the bias and offset currents are negligible at normal equipment temperatures

Soft changeover circuit

This circuit (**Fig 33**) is designed to give a soft changeover between two inputs - in effect a fast crossfade. It is just the mute block but with two separate inputs, either or both of which can be switched on. The performance at +20dBu in/out is summarised in Table 5.

The THD increase at 20kHz is due to the use of a TL072 as the opamp. J1 12 JFETs are used in all positions. This circuit is intended for soft-switching applications where the transition between states is fast enough for a burst of high distortion to go unnoticed. It is not suitable for generating slow crossfades in applications like disco mixers, as the exact crossfade law is not very predictable.

Control voltage feedthrough in JFETs

All discrete FETs have a small capacitance between the gate and the device channel, so changes in the gate voltage will therefore cause a charge to be transferred to the audio path, just as for CMOS analogue gates. As before, slowing down the control voltage change tends to give a thump rather than a click to a thump; the same amount of electric charge has been transferred to the audio path, but more slowly. Lowering the circuit impedances is effective in reducingcertainly reduces the effect of the feedthrough, butit is of limited effectiveness.use. Halving the impedance only reduces the amplitude by 6dB, and such a reduction is likely to increase distortion. ■

NEWPRODUCTS

Please quote *Electronics World* when seeking further information

Dual 1Gbit Ethernet board supports up to four devices

The MAT 1040 PICMG single board computer from Microbus combines a Pentium 4 with the Intel 845G chipset. Socket 478 Pentium 4 processors up to 3GHz and Celeron processors up to 2GHz are supported. Product features include support for two 10/100/1G Ethernet ports, DDR memory up to 2 Gbyte, and provision for CompactFlash type I and II. The board's ATA/100 interface allows support of up to four devices including hard disc, CD-ROM, LS and Zip drives. Other interfaces include two serial, one parallel, four USB, IrDA, keyboard and mouse ports. The 845G chipset features integrated graphics and video support, while additional AGP daughter cards add further graphics capability, ranging from nVidia GeForce2 MX 400, to an ADD card for DFP/LVDS panels, and an ATI Mobility Radeon flat panel controller.

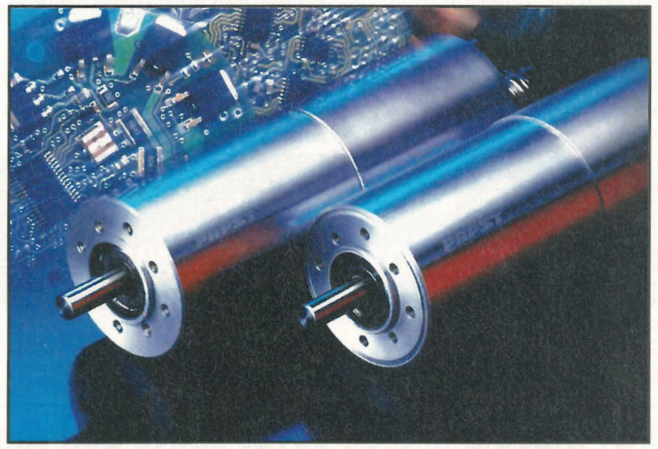
Microbus
www.microbus.com

Motor with integral electronics

Comprising motor plus integrated control electronics and network filter, Papst's 56mm EC motor operates from the standard industrial voltage of 18 to 28Vdc with a nominal current consumption of 5A. Utilising neodymium magnets, the motor attains an output of 90W and a torque of 29mNm at a rated speed of 3000rpm. Different types of gear units are available to expand the field use. The service life of the three phase, electronically commutated motor is over 20,000 hours. Dimensions of the drive are 56mm diameter and 140mm in length.

Microprocessor-based control electronics are used to carry out many functions of motor management. Three Hall sensors give the microcontroller position signals of the motor current. The four-quadrant controller is equipped with an end stage capable of over-current, and a protection function for other safety features such as stall protection and temperature monitoring. In order to keep within the limits for incoming and outgoing interference radiation, an efficient EMV network filter is integrated in the casing. The drive can be controlled via a standard interface, such as 0-10V signal or an optional frequency range signal of 0-400Hz. An actual value output and alarm output permit external monitoring of the drive.

Papst
www.papstplc.com



Mini ferrite chokes rated for 55A

A range of miniature high current ferrite common mode chokes from Steward are rated up to 55A of continuous operating current. Suitable for high- or low-frequency applications, the CM41 chokes are available in broadband and low frequency materials and are smaller and less suscepttible to the effects of vibration than more traditional wire-wound devices.

Steward
www.steward.com

Real-time radar processing platform in 6U VME

Pentek is offering developer-ready systems aimed at data acquisition, digital up- and down-conversion, processing, analysing, recording and synthesising signals. It is also offering RTS Turnkey Systems tailored for specific, high-end applications. To support the offering, the VME board firm has entered into a strategic alliance with a system integrator, DSPCon, which will come up with an integrated and tested commercial-off-the-shelf design with custom application code and a complete graphical user interface. The first platform offering in the series is the System RTS 2501, a real-time radar signal processor and recorder development platform, consisting of a 100MHz, 14-bit analogue front end, scalable from 2 to 80 channels. The system is delivered in a 6U VMEbus card cage pre-configured and tested, with all required cabling and software.

Pentek
www.pentek.com

Shielded M-12 Profibus connector

Harting has introduced a shielded M-12 profibus connector using the company's HARAX rapid termination technique. This technique eliminates soldering or screw terminations. The individual strands in a cable are inserted into a splicing ring and cut to length. The shield is attached to the metal housing via a sliding ring. The individual strands are then terminated securely using insulation displacement technology with the aid of a union nut. The connector is for use in harsh industrial environments and offers protection to IP67. It is rated at up to 32V and 4A, and designed for conductor sizes from AWG24 to AWG22.

Harting
www.harting.co.uk

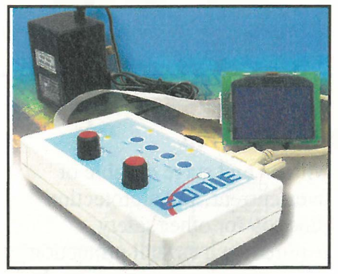
Tiger-SHARC board for military uses

BittWare has a TigerSHARC board support package for Gedae. Largely used in military applications, Gedae developed by Blue Horizon Software, is a development tool for signal processing algorithm design and implementation on real-time embedded multiprocessor systems. The approach is designed to allow developers to analyse the performance of the embedded implementation and optimise it to various hardware platforms. They can use Gedae to develop hardware-independent code in a graphical environment and then port their designs to any supported hardware. The EZ-TigerSHARC BSP for Gedae allows developers to port their designs to any of BittWare's ADSP-TS201 and ADSP-TS101 TigerSHARC platforms, providing all the TigerSHARC components required to tailor any Gedae design to BittWare hardware. It features cluster bus and link port communication methods in word, block, and DMA modes for extensive interprocessor communication capability. The memory handler offers full use of the TigerSHARC multi-memory block architecture and the external board memory.

BittWare
www.bittware.com

LCD developer kit

Intelligent display Solutions has launched an LCD development tool which is intended to simplify the design of user



interfaces. Called Eddie, it allows the user to create graphics and text in MSPaint, or any other suitable drawing program. The graphics are then loaded onto the display. Control for up-loading is managed by the hyperterminal software tool that is standard on all PCs. It requires no special software and connects to the PC via the RS232 port.

Intelligent Display Solutions
www.intelligentdisplay.com

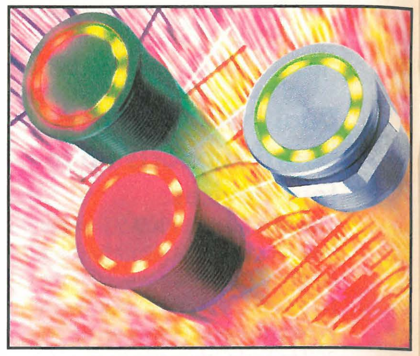
Multi-processor support device

Fujitsu has introduced an ARM9 multi-CPU evaluation device, the MB87Q1100, which implements the next-generation SoC platform, integrating ARM926EJ-S and ARM946E-S embeded macrocell cores. The external extension function of AHB-Lite, a subset of the AHB system bus, is incorporated. According to the supplier, this makes it possible for customers to design and verify modules in their Asic by connecting the master and slave module of AHB-Lite to the device. The device is available in an FBGA400 package.

Fujitsu
www.fme.fujitsu.com

Green light for touch switches

Schurter has launched a ring illuminated piezo switch, ideal for night use or to provide a simple on/off status display in a wide variety of applications.The device has a mounting diameter of 22mm and, unlike mechanical switches has no moving parts, and is less likely fail due to parts



wearing out. The PSE M22R series are specified with a 20 million lifecycle operation. The switch housing is made of anodized aluminium and is available in various colours. The ring illumination is available in red, green or a 2-colour red/green combination, the switches are rated to IP67. An O-ring is supplied to seal the front plate. The switches are supplied either ready to wire in directly, or alternatively, with a Molex type connector. The socket features a D-shaped area to allow for the correct positioning of marked switches.

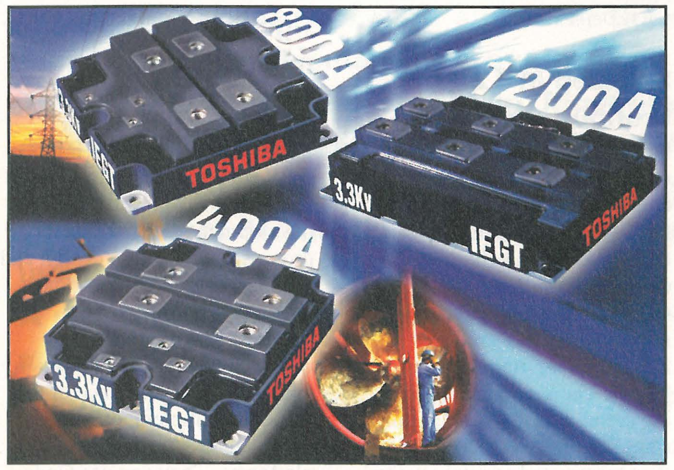
Schurter
www.schurter.com

Ultra miniature chip capacitors

Murata's smallest range of multi-layer ceramic capacitors (MLCCs) measure just 0.4x0.2x0.2mm. The 01005 size MLCC is already in volume production and the capacitance range of devices is from 2pF to 15pF for C0G dielectric types and from 1000pF to 10000pF for R characteristic capacitors. According to the supplier, to get an idea of the scale of these chips when compared to the current 0201 size (0.6x0.3x0.3mm) the 01005 size

IEGT module line-up saves space and simplifies cooling

Toshiba's latest 3.3kV IEGT (injection-enhanced gate transistor) module is designed to have reduced on-stage losses as well as offering a 30 per cent reduction of off-state losses when compared with conventional modules, said the supplier. Integrating multiple IEGT chips with fast recovery diodes (FRDs), the MG1200FXF1US53, MG800FXF1US53 and MG400FXF2YS53 IEGT modules have respective current ratings of 1200A, 800A, and 400A. Maximum junction to case R_{th} ratings for the transistor stages of the IEGT modules are as low as 8K/kW. Typical overall module R_{th} are 9K/kW for both the MG400 and MG800 falling to just 6K/kW in the case of the 1200A MG1200 module. An Aluminium Silicon Carbide (AlSic) base plate has been used to optimise thermal dissipation and to ensure high-reliability operation and extended lifetime characteristics. The modules are suitable for very high-power applications including large motor drives for locomotives, trams and other traction control systems, uninterruptible power supplies (UPS), power transmission and distribution designs. The 1200A and 800A modules are based on a 1-in-1 circuit configuration, while the 400A module incorporates a 2-in-1 circuit. All the modules have an isolation voltage rating of 6000Vac (for one minute) and can operate with junction temperatures of between –40 and 125°C. Minimum short circuit capability is rated at 2500V.



Toshiba
www.toshiba-europe.com

Please quote *Electronics World* when seeking further information

chip capacitor takes up approximately 50 per cent less board space. In addition, the shorter length has resulted in lower inductance.

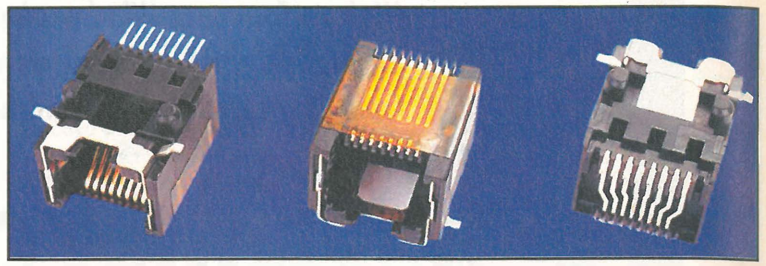
Murata
www.murata-europe.com

RTOS supports ARM development kit

Quadros Systems has announced that its real-time operating system supports the recently released CodeWarrior development suite for ARM-based processors. The combination of the RTXC Quadros RTOS and the new Code Warrior development suite offers customers tighter integration, shorter development times and enhanced visibility into their applications. The RTXC Quadros RTOS features a kernel awareness plug-in module for the Metrowerks development suite. The Metrowerks development suite includes a fast editor, award-winning debugger, a new Metrowerks compiler for ARM architectures, and an assembler and linker. The RTXC Quadros real-time operating system is a generation RTOS composed of two major architectural modules: a Single kernel and a Multi-stack kernel. The RTXC Quadros real-time operating system, with support for the new Metrowerks CodeWarrior development suite, is available immediately.

Quadros Systems
www.quadros.com

Jack connector increases EMI protection



A jack connector with a copper alloy shield within its plastic housing available from FCI is designed to provide increased protection against EMI when mated with shielded male connectors. The single port RJ45 right angle connector has 8 contact loaded positions and suits low profile network interface cards. Conforming to FCC Part68F and EIA Performance Category 3 specifications, the connector is compatible with standard industry parts. The connector offers gold plated mating contacts specified for up to 750 connection cycles and a lead free option using pure tin plating for the solder tail area. The jack connector is compatible with all vapour phase and reflow soldering processes and is provided in tray or tape and reel packaging.

FCI
www.fciconnect.com

Chip camera has 1,600x1,200 resolution

TDC has available the OV2610 CameraChip from OmniVision. Suitable for digital still image and video/still camera products, the device incorporates a 1,600x1,200 (UXGA) image array and on-chip 10-bit A/D converter capable of operating at up to 10frames/s with full resolution and 40frames/s at SVGA (800x600) resolution. There are fixed pattern noise cancellation algorithms to provide black level calibration for optimal colour performance. Other features include video or snapshot operation, programmable image windowing, variable frame rate control in addition to internal/external frame synchronisation.

TDC
www.tdc.co.uk

Decoders convert video formats

Texas Instruments has two mixed signal video decoders which convert NTSC, PAL and SECAM video into digital component video in applications such as personal video appliances, digital and mobile phone TVs. With power consumption at 115mW in typical operation, the TVP5150 and TVP5146 are high performance mixed-signal video decoders that convert base-band analogue NTSC, PAL and SECAM video into digital component video. The TVP5146 supports up to ten component video inputs.

Texas Instruments
www.ti.com

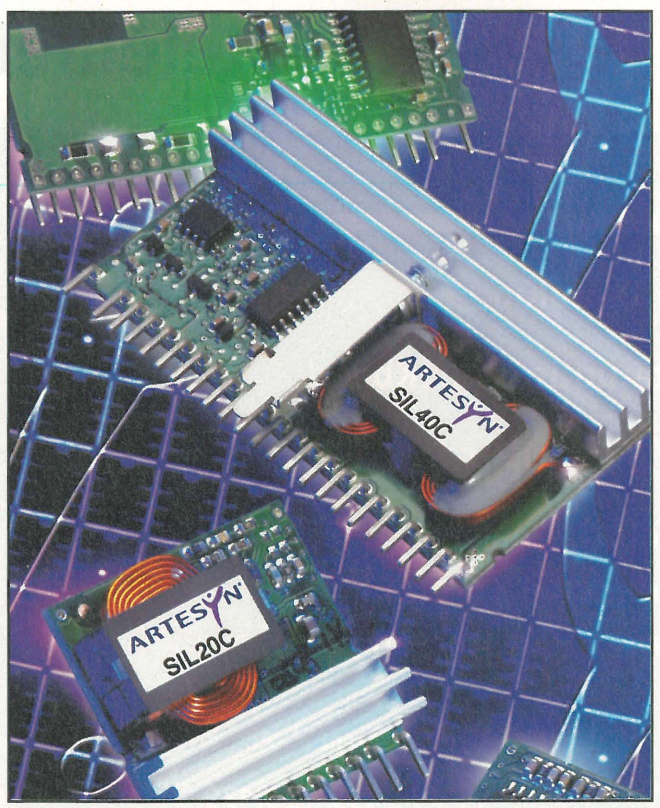
Linux support for comms board

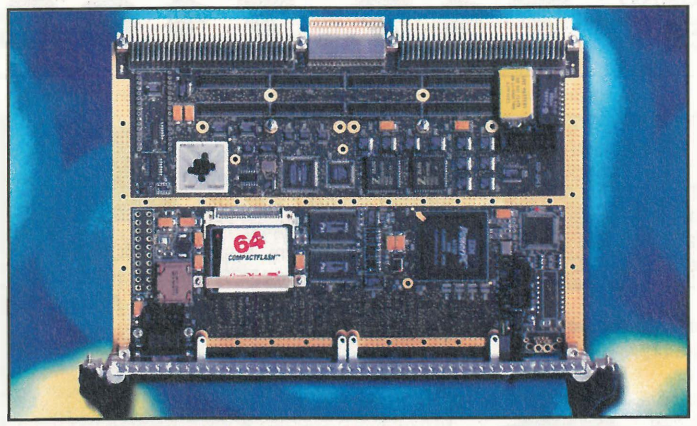
Thales Computers is supporting the Linux OS in its low-power (typically 6.5W) VCE405 comms board. According to the supplier it can reduce the need for heat sinks or cooling fans and has an operating range up to 85°C using convection cooling. The 6U VCE405, an off-the-

Converters support distributed power design

Artesyn Technologies has extended its point-of-load converter range with options offering a third more power, without any change to form-factor or footprint. The 'C-class' non-isolated DC-DC converters have an open-frame, single-board construction. The SIL20C and SIL40C have a single output adjustable from 0.9V to 5.0V at currents of up to 20 or 40A. Output voltage is set by an external resistor. Input voltage is either 12V or 5V to suit the different intermediate DC bus voltages used in computing and telecoms. The 5V input version is adjustable only up to 3.3V. Both converters are for through-hole board mounting, and offered in a choice of vertical or horizontal package orientations. Vertical models feature small-footprint, single-in-line connections.

Artesyn Technologies
www.artesyn.com

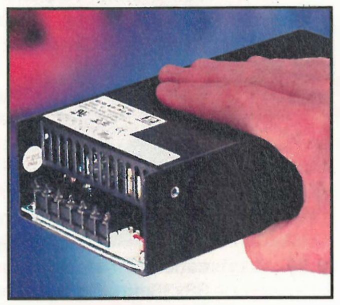




shelf connectivity engine based on the 400Dhrystone Mips 266MHz IBM PowerPC 405GP 32-bit Risc embedded controller, features dual PMC slots that support 64-bit PCI buses. The Linux board support package is based on a standard Linux 2.4 kernel compatible with the LynusWorks BlueCat 4 cross compiler and tools. The VCE405 is already available under VxWorks and LynxOS 4.0, which is the hard real-time Unix OS. With Linux ABI from LynuxWorks, the VCE405 is a certified reference platform for LinuxOS
Thales Computer
www.thalescomputers.com

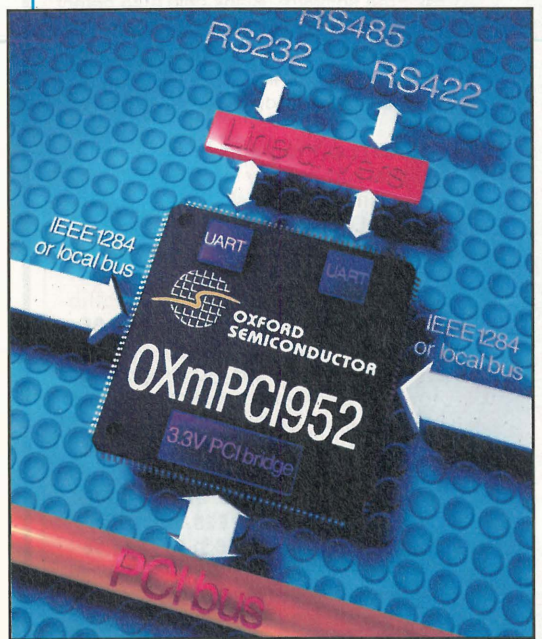
AC/DC power supplies shrink equipment size

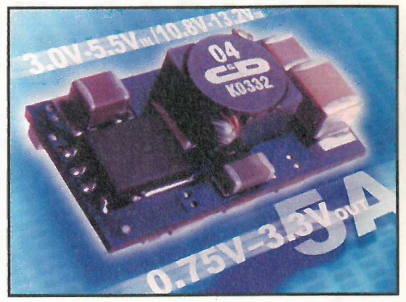
With power density of 6.25W/in^3, the SMQ 300 and SMQ400 AC/DC switch mode supplies from XP are designed to support peak loads at up to 2.3 times nominal output current ratings. The units, with internal cooling fans and over-current, over-voltage and over-temperature protection, provide single outputs between 12Vdc and 54Vdc from a universal AC input with efficiencies up to 85 per cent. The units also have remote sense, DC-OK and remote on/off functions. Battery charging versions suited to use in standby systems, are also available. The power supplies meet all relevant EMC specifications and have UL, CSA, EN and CE international safety approvals. Active power factor correction is built-in, giving a typical power factor of 0.99
XP
www.xpplc.com



Fast throughput from dual UART / PCI bridge chip

Integrating two high performance UARTs, a 3.3V PCI/mini PCI interface and a parallel port/localbus in a 160LQFP package, Oxford Semiconductor's latest UART offering provides a sustained data throughput of 60Mbit/s in isochronous mode and 15Mbit/s in asynchronous mode. According to the supplier, 128 byte transmit and receive FIFOs on each UART channel also enable the OXmPCI952 to reduce CPU interrupts and boost the speed of PCI and Mini PCI serial and parallel add-in cards. The UARTs are compatible with industry standard 16C550 devices and the PCI interface is also fully compliant with PCI bus version 3.0 and PCI power management version 1.1 specifications. The device has two operating modes: function 0 which offers the fast dual UART capability and function 1 which provides either an 8-bit local bus or a bi-directional IEEE1284 parallel port supporting SPP, PS2, EPP and ECP protocols. Serial card applications requiring more than two UART channels are also possible using the IC's 8-bit pass-through local bus option, which enables the chips to be cascaded to create up to 18 serial ports. The OXmPCI952 is supported by software drivers for Windows NT, XP and MacOSX, with Linux drivers available from third party sources. A PCI card design note, PCB schematics and application notes are also available.
Oxford Semiconductor
www.oxsemi.com





DC-DC converters can deliver up to 5A

C&D Technologies has announced two non-isolated DC-DC converters designed for use with nominal 3.0V to 5.5Vand 10.8V to 13.2V intermediate bus architectures. The NNL05S04 and NNL05S12 deliver a maximum 5.0A output current. Typical efficiency levels are up to 93 per cent. The converters offer user-selectable output voltages of between 0.75V and 3.3V and feature a low typical output ripple and noise rating of 24mV (peak-to-peak). Voltage accuracy is up to 0.3 per cent, while typical line regulation and load regulation are 0.76 and 0.52 per cent respectively.
C&D Technologies
www.cdpoweronline.com

SIM card controller has 256kbyte memory

Samsung is offering a 256kbyte version of its SIM card microcontroller series. Industry-standard security features common to all family members include built-in DES/T-DES hardware and SPA/DPA prevention circuitry. Samsung is targeting common criteria security certification, and has already received EAL4+ security certification for the 64KB controller. Common criteria has been adopted as ISO standard ISO/ISEC 15408.
Samsung
www.samsung.com

P-channel Mosfet is optimised for bucks

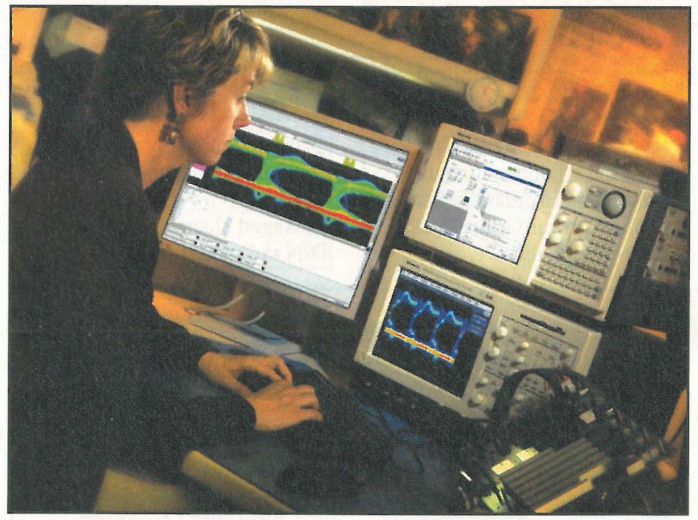
Vishay Siliconix claims to have the industry's first p-channel power Mosfet optimised for use in synchronous buck converters. Used on the synchronous buck high-side, a p-channel Mosfet can be turned on with a gate drive that is lower than the battery voltage. According to the supplier, this can potentially eliminate the need for extra bootstrap circuitry in DC-DC converter design. Combining on-resistance of 0.051Ω with a typical gate charge of 7nC, theSi3867DV delivers an on-resistance-times-gate-charge figure of merit of 0.36. The device has been designed to eliminate secondary turn-on effects
Vishay
www.vishay.com

More I/O for PC/104 computer boards

Ampro Computers has added extra I/O expansion capabilities for its Little Board and CoreModule single board computers and CPU modules. MiniModule products supplement the I/O found on EBX-form-factor SBCs such as the little Board 700 which features low-power Pentium 111 and Celeron processors, as well as PC/104- and PC/104-Plus-form-factor CPU modules and SBCs such as the 486-based CoreModule 400 and the CoreModule 410 and 600 products. The modules plug on top of the CPUs and SBCs using the industry-standard PCI and ISA buses in PC/104 and PC/104-Plus connectors. They plug in horizontally rather than vertically like slot cards, which reduces the height and mounting requirements of end systems.
Ampro
www.ampro.com

Advances in digital signal analysis

Tektronix has added multi-channel eye-diagram signal analysis capabilities to its TLA700 series logic analysers. It offers eye diagrams and mask testing for hundreds of signals instantaneously. As part of the iLink Tool set, iVerify provides multi-channel analysis and validation testing using powerful oscilloscope-generated eye diagrams. It joins iConnect (digital/analogue data acquisition through a single probe) and iView (time-correlated, digital/analogue/digital probing, acquisition, display and analysis.)
Tektronix
www.tektronix.com

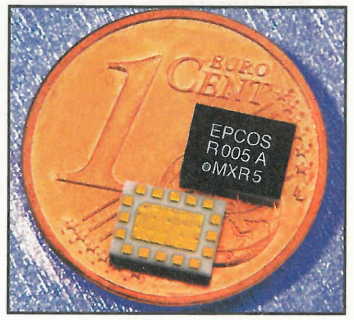


Embedded board spec combines next generation buses

Kontron has proposed a specification for embedded computers which integrates the latest interface technologies such as PCI Express, Serial ATA, Gigabit Ethernet, Dual Channel DDR and USB 2.0. Called ETXexpress, it will support 4 PCI Express x1 Lanes and PCI Express cards as well as established hardware based on current busses such as 32-bit PCI and ISA bus (via a LPG). A 10/100/1000Mbit Ethernet port provides fast connectivity to LAN/WAN and 6x USB 2.0 provide interfaces for external drives/flash, keyboard, mice and other peripherals. The new standard is planned to be initially offered in a 85mm x 125mm form factor. Signals are brought out via 160-pin SMT connectors that permit data transmission rates of up to 5GHz. Six mounting holes on the board provide resistance to shock and vibration. The thermal coupling system incorporates a standardized heat spreader, as is the case with ETX. The first Kontron ETXexpress modules will be based on 1.6GHz Intel Pentium M processors as well as the Intel 855 GME chipset.
Kontron
www.kontron.com

802.11b/g/a RF front-end module

Epcos is offering its first module to integrate the complete dual-band front-end circuitry for wireless LAN devices in a package measuring 5.4x4.0x1.4mm. The R005 module combines two duplexers,



DSP design with first power-over-Ethernet computer

DSP Design claims to have the first touch screen, flat panel computer to be powered over an Ethernet CAT5 cable. Known as POET 6000, it uses IEEE802.3af power-over-Ethernet technology to provide power and data over a single standard CAT5 cable. It includes a 12.1in TFT display fitted with an impact resistant, touch screen for user input and is available on a wall-mounted panel or as a desktop unit. Delivered with a pre-configured copy of Microsoft Windows XP Embedded, the enclosure has a standard RJ45 Ethernet connector and two USB connectors. Power-over-Ethernet allows IP telephones, wireless LAN access points and other appliances to receive power as well as data over existing LAN cabling.
DSP Design
www.dspdesign.com

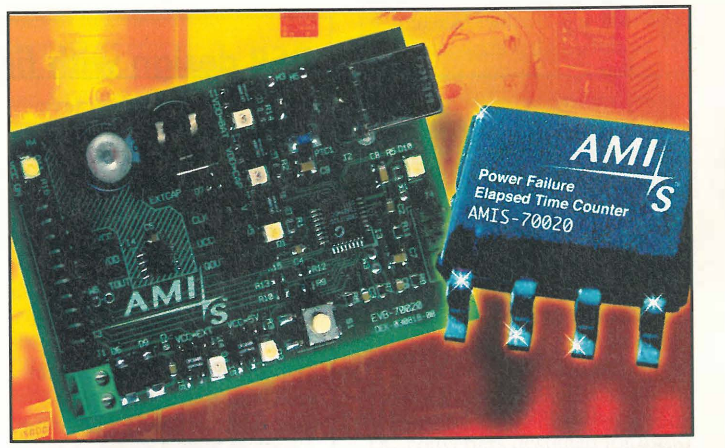
two receive filters, two transmit filters and an antenna diversity switch in a single component. It is for WLAN chipsets that conform to the IEEE 802.11 b/g/a standard, operating in the frequency bands from 2.4 to 2.5GHz and from 4.9 to 5.9GHz. The modules have footprints of 5.4x4mm.
EPCOS
www.epocs.com

Threaded probe for cable-harness and automotive testing

Peak Test Services has a threaded probe designed for use

in testing cable harnesses and automotive electrical systems. A small mounting diameter allows it to be used in applications where probes needed to be spaced at 2.2mm centres, said the supplier. It is also suited to applications involving 2.5mm centres where greater clearance between adjacent probes is required to allow for wider tolerance in test-fixture construction or to prevent electrical arcing. Two tip styles with a choice of two diameters for each are initially available from stock, with further variants being introduced in the near future. A choice of four spring pressures from 1N to 3N is available.
Peak Test Services
www.thepeakgroup.com

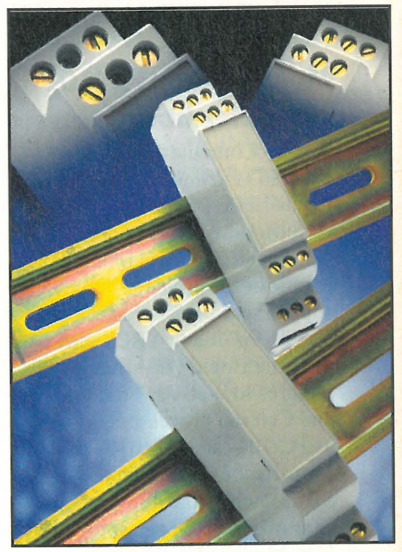
Plug-and-play evaluation kit



An evaluation kit is available from AMI Semiconductor for its recently launched AMIS-70020 'Power Failure Elapsed Time Counter' IC.
The kit allows designers to reduce the component count, cost and time-to-market for industrial power failure duration monitoring systems, typically used in applications where measuring power failure duration is needed for equipment and material protection.
The board allows users to evaluate the counter IC in a "stand alone IC evaluation-mode" or in a "system integration mode".
AMI Semiconductor
www.amis.com

DIN rail mounted module housings

Distributor Switchtec is offering electronic housings from Euroclamp for the production of packaged electronic modules for DIN rail mounting.



The housings can be supplied with up to 12 connections to the internal PCB (four 3-way terminal blocks). Although grey is the standard colour, other colours including red, green and black, can be provided for branding and identification purposes.
The units can also be supplied with a wide range of markings and graphics. The standard 1 DIN width of 17.5 mm is used to enable multiple device mounting on DIN rail and Euroclamp have designed a terminal block that allows the PCB to be vertically mounted within the housing.
DIN rail compatibility ensures that housed electronic devices can be quickly installed and replaced for maintenance purposes. The housings are made from self-extinguishing polyamide.
Switchtec
www.switchtec.co.uk

FCB colour block camera

Sony image sensors have announced the FCB-S300P colour block camera, the first FCB block to incorporate 3-CCD technology for picture quality and an integrated zoom lens. It offers a 16:9 aspect ratio as well as a high-speed serial interface, RS-232/TTL remote control, 12X optical zoom and slow shutter.
According to the supplier, likely applications include remote monitoring with plasma display, high-end video surveillance, broadcast and industrial applications where 16:9 modes are increasingly demanded. With a 3-chip Mega Pixel camera system derived from three, 1/4.7-type advanced HAD CCD sensors each with a total of 1,070,000 pixels. It is switchable between 16:9 and 4:3 modes, and features a x48 zoom ratio comprising x12 optical and x4 digital. A signal to noise ratio of more than 50dB is returned and the camera requires a minimum illumination of 15lux. A range of video outputs are provided comprising analogue composite, Y/C, or R/G/B/Sync. Size is 72(w)jx67(h)x105.5mm.
Sony
www.sonybiz.net

CIRCUIT IDEAS

Fact: most circuit ideas sent to *Electronics World* get published

The best circuit ideas are ones that save time or money, or stimulate the thought process.

This includes the odd solution looking for a problem – provided it has a degree of ingenuity.

Your submissions are judged mainly on their originality and usefulness. Interesting modifications to existing circuits are strong contenders too – provided that you clearly acknowledge the circuit you have modified. Never send us anything that you believe has been published before though.

Don't forget to say why you think your idea is worthy.

Clear hand-written notes on paper are a minimum requirement: disks with separate drawing and text files in a popular form are best – but please label the disk clearly. Where software or files are available from us, please email Caroline Fisher with the circuit idea name as the subject.

Send your ideas to: Phil Reed, Highbury Business Communications, Nexus House, Azalea Drive, Swanley, Kent, BR8 8HU *email ewcircuit@highburybiz.com*

Simple, low-power logic level to RS232 level conversion

With the proliferation of low-power, built-in-power-supplies RS232 driver ICs available these days, the need for this circuit is perhaps not too great. Still, it may come in handy if an IC happens to be unavailable. A PNP and an NPN general-purpose switch transistor performs the logic inversion and the unipolar logic level to bipolar RS232 level conversion, and vice versa.

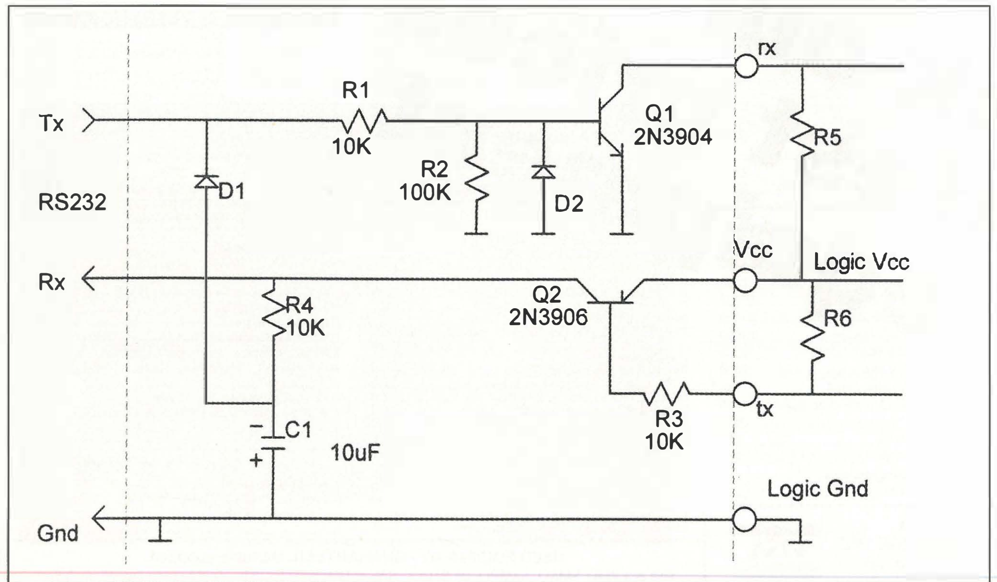
Q1 receives the RS232 transmitter signal and provides open-collector output. This output would typically be pulled to the logic Vcc supply as shown with R5. D2 protects Q 1 from the negative excursion of the RS232 signal that could be large enough to cause base-emitter breakdown.

Q2 receives the logic-level signal and drives the RS232 receiver between a positive voltage equal to the logic supply and the negative voltage at C1. Logic supplies down to 3.3V should still (barely) meet RS232 level specifications.

D1 and C1 steal negative voltage from the RS232 transmitter to pull the RS232 Rx line negative when Q2 is OFF. In other words, the RS232 transmitter drives the RS232 receiver input to the negative level. The size of Cl is not critical, it just needs to hold up during the positive time of a RS232 transmitted character, so its size depends on baud rate and receiver input impedance.

The interface circuit draws only leakage currents from the logic supply when the RS232 lines are disconnected or even if connected but inactive. The logic supply provides the base current for Q2 when the logic tx signal is low, but when the RS232 is idle, the Rx line should be negative and therefore Q2 should be OFF, so the logic level tx signal should be normally high. Similarly, the idle RS232 Tx line is negative, turning Ql OFF. When the RS232 Tx is active, Q1 switches ON, and the logic supply provides the Ql collector current via pullup resistor R5. R2 and R6 connect the base-emitter junctions of the transistors to assure they are off when the RS232 is idle or disconnected.

It is worth emphasising that the interface circuit ground is common to and connects the RS232 and logic circuit grounds.

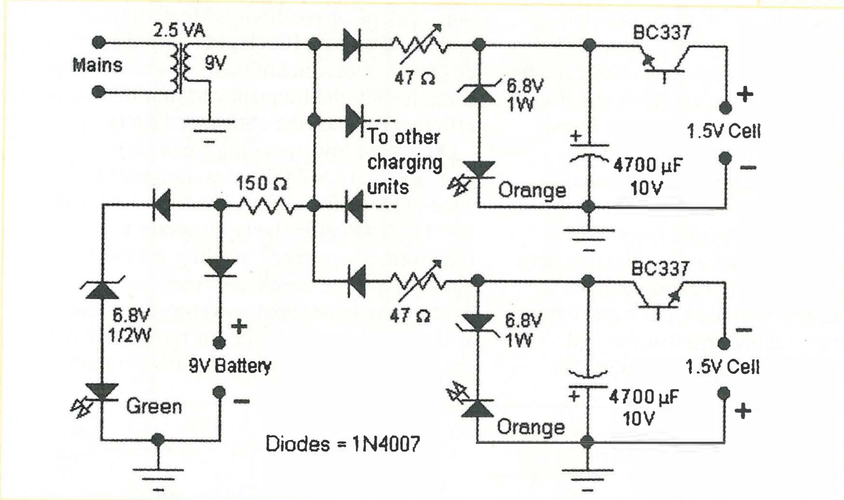


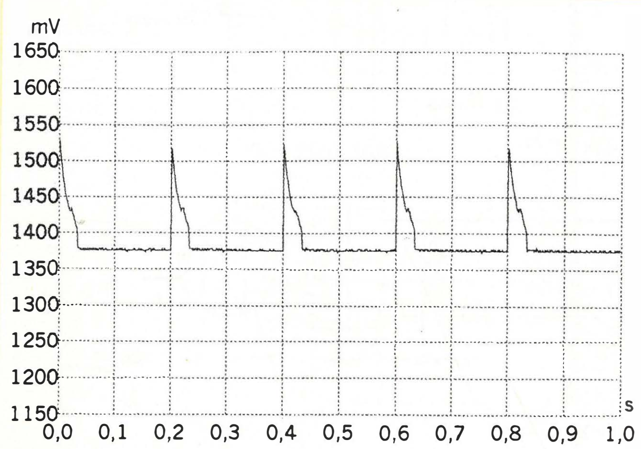
Joe Young
Victoria
British Columbia
Canada

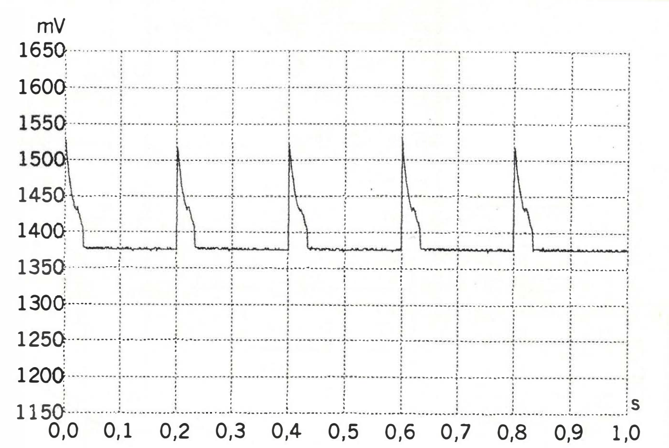
Alkaline charger

This circuit was specifically designed to recharge alkaline cells. The unusual connection of the transistor in each charging unit will cause it to oscillate, on and off, thus transferring the charge accumulated in the capacitor to the cell. The red LED will blink any time there is this transfer of charge, around five times a second for a 1.377V cell (see chart showing the voltage across an AA cell being charged). For a totally discharged cell the blinking is faster: up to nine times a second but it will decrease until it comes to a stop when the cell is charged. You may leave the cell in the charger as it will trickle charge and keep it at around 1.6V. To set the correct voltage you have to connect a fresh, unused cell and adjust the trimmer until oscillations set in, then go back a little until no oscillation is present and the circuit is ready to operate. You should use only the specified transistors, LED colours, zener voltage and power rating because they will set the final voltage across the cell. A simple 9V charging circuit was also included: it will charge up to around 9.3V and then keep it on a trickle charge: the green LED will be off while charging and will be fully on when the battery is close to its final voltage. A 2.5VA transformer will easily charge up to four cells at the same time although two only are shown in the schematic. You may add more charging circuits provided you increase the transformer power rating. In order to minimise interference from one circuit to the other they have nothing in common except the transformer and in order to show a balanced load to the transformer, half of the charging units will use the positive sine wave and the other half the negative sine wave. All types of alkaline cells can be recharged: it will take around 1 day for a discharged AA cell or 9V battery and up to several days for a large D type cell. The best practice is not to discharge completely the cell or battery but rather give it a short charge every so often although admittedly this is not easy to achieve. The circuit will endure temporary battery reversal, shorts and over voltages but do not recharge cells or batteries that show even a minimal damage, leakage, or have been kept discharged for a long time.

D. DiMario
Milan
Italy







16 channel selector

This circuit will allow push button control of 16 channels in any application. This circuit is an expansion of the 8-channel control published some time ago. As with the previous circuit it consists of 4 to 16 channel line decoders with diode feedback. To create an expansion to 16 channels, the outputs are controlled in groups of 4 outputs by CD4514 decoders. A fifth CD4514 is used as priority decoder. When a push button is pressed the feedback diodes maintain the selected input.

As the inputs are directly connected to priority encoder U1, it will select an output IC to control the output selected with the push button. By providing a priority function it is impossible to have more than one output selected. It is also excluded to have an output selected if more then one pushbutton is depressed. If this where the case, no outputs are enabled as this is prevented by the 4 to 16 channel line decoders. In this application the only outputs used of the decoders are those that have only one high level input.

An additional function of the priority decoder is to provide an output enable. As the enable input of the IC not only controls the outputs of the IC but also the outputs of the channel selectors U2-U5.

In the present circuit the output control relays with ULN power drivers. However the possibilities for output control are unlimited.

Bernard Van den Abeele
Evergem
Belgium

Electronic half bridge replaces mechanical vibrator in 6V to 12V conversion

A friend, currently engaged in rebuilding an American Ford Mercury of 1953 vintage, asked me to restore and convert the original valve car radio to 12V as the vehicle electrical system was being converted from 6V to 12V. The American vehicle voltage standard of the time was 6V and as a result the radio had no provision for conversion to 12V operation built-in. With eight octal valves, including twin 6V6GT valves operating in push-pull, this radio was capable of driving 10W+ into the speakers and drew a massive 8-10A from a 6V supply; a linear series regulator was therefore out of the question. The radio had to be converted to 'internal' 12V operation.

The first step, re-arranging the valve heaters in series-parallel was a trivial matter. However, some thought had to be given to the power supply; derived from a mechanical vibrator, centre-tapped transformer and 6X5GT HT rectifier valve. Replacing the transformer was out of the question and the only alternative that immediately sprang to mind was the use of a half or full bridge MOSFET driver circuit. As the half bridge was simpler, this was evaluated first and found to be perfectly adequate. A CMOS 4047 oscillator was used, its complementary outputs driving a pair of IRFIZ44 MOSFETs via a suitable drive circuit. Most vibrators operate at around 100Hz, but with the electronic replacement there was some scope for adjusting the frequency to improve efficiency, hence the choice of 170Hz.

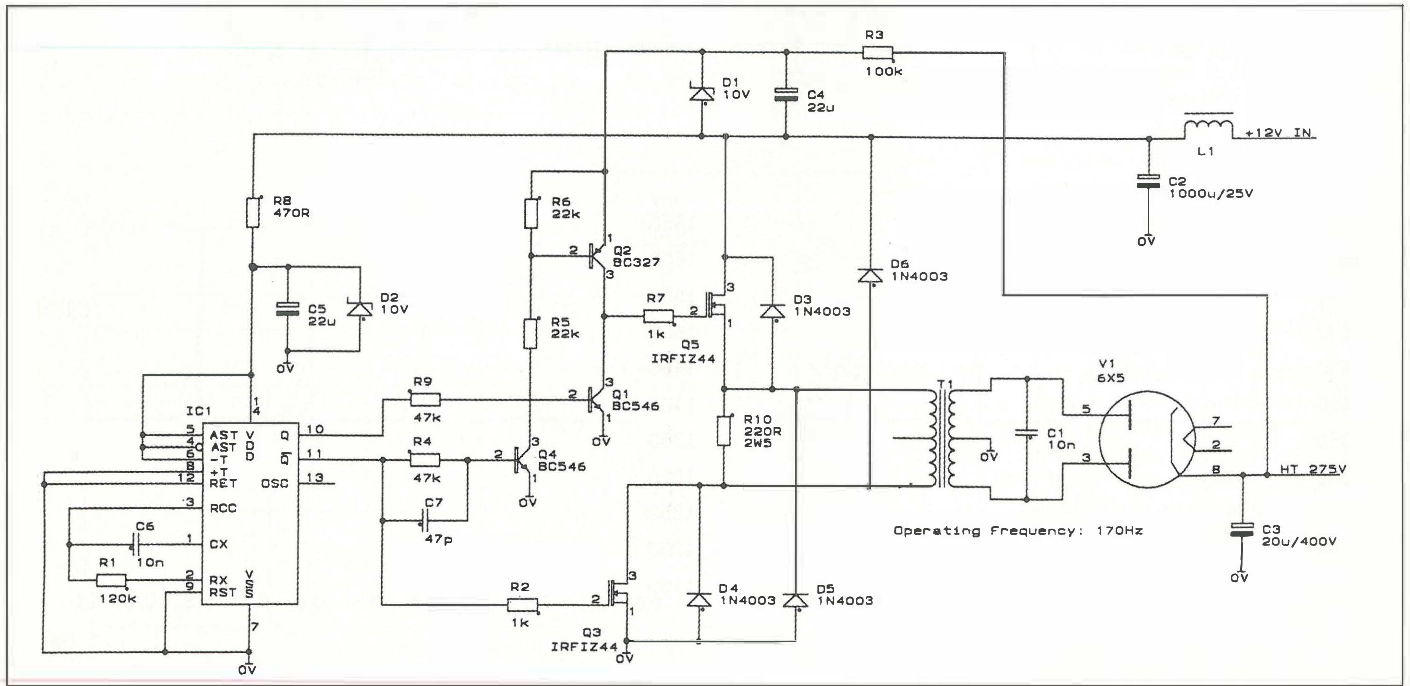
Due to the low operating frequency conventional 1N4000 series diodes can be used in the output stage. The four diodes D3, D4, D5 & D6 effectively constrain the transformer's primary winding within the supply rails and the transformer 'sees' exactly the same input waveform as it did with the mechanical vibrator running on 6V, the only difference being that the primary centre tap is left to float. R10 provides primary damping, smoothing out discontinuities at the switching points. With the diodes and R10 mounted on the vibrator base, the rest of the circuitry, built on a small PCB was mounted in the original vibrator can. Other points of note in this circuit:

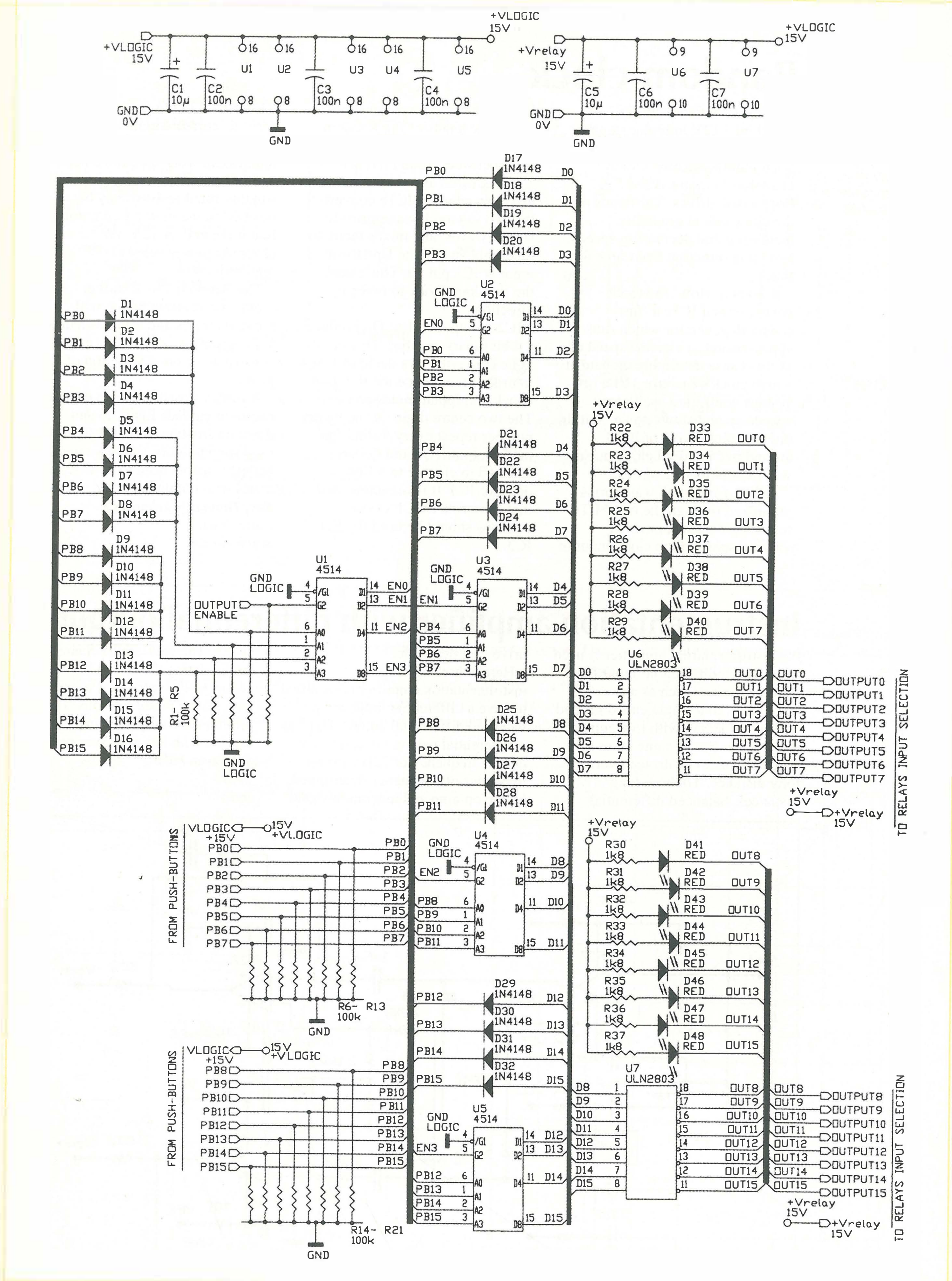
1) 'Boosted supply' for Q5 gate is developed from the supply via R3. This means that whilst V1 is warming up the bridge operates at a much reduced voltage thus limiting the peak voltages seen by T1 & tuning capacitor C1.

2) R7 & R2 are included to slow the switching of the MOSFETs and thus reduce interference.

3) Running at an input power of around 25W no heatsinks are required for Q3 & Q5.

Jeremy Stevens
Ealing
London
UK





Random clock

The Random Clock in Fig.1 is based on a 12V unipolar stepper motor operating in wave mode. Such motors are now widely available from discarded $5^{1}/_{4}$” floppy disk drives. The hands of the clock tick at gradually increasing and decreasing speeds, reversing direction from time to time.

IC1d is a ‘slow’ sawtooth generator and IC1c a ‘fast’ sawtooth generator which runs at approximately twice the speed of 1C1d. These determine the rate at which clock generator 1CI a (a voltage controlled oscillator) speeds up and slows down. Within one complete cycle of IC1d, around one hundred clock pulses will be sent to 1C2 pin 15.

The two sawtooth waveforms are mixed through the two FETs, to produce a clock pulse of varying speed at the clock input of IC2. This determines the speed at which the hands of the Random Clock move clockwise or anticlockwise around its face.

IC2 is wired as a 4 bit binary up-down counter. IC1b converts the two sawtooth waveforms to square waves, and mixes them, to randomly switch the Up/Down input at IC2 pin 10. This causes the Random Clock to reverse direction.

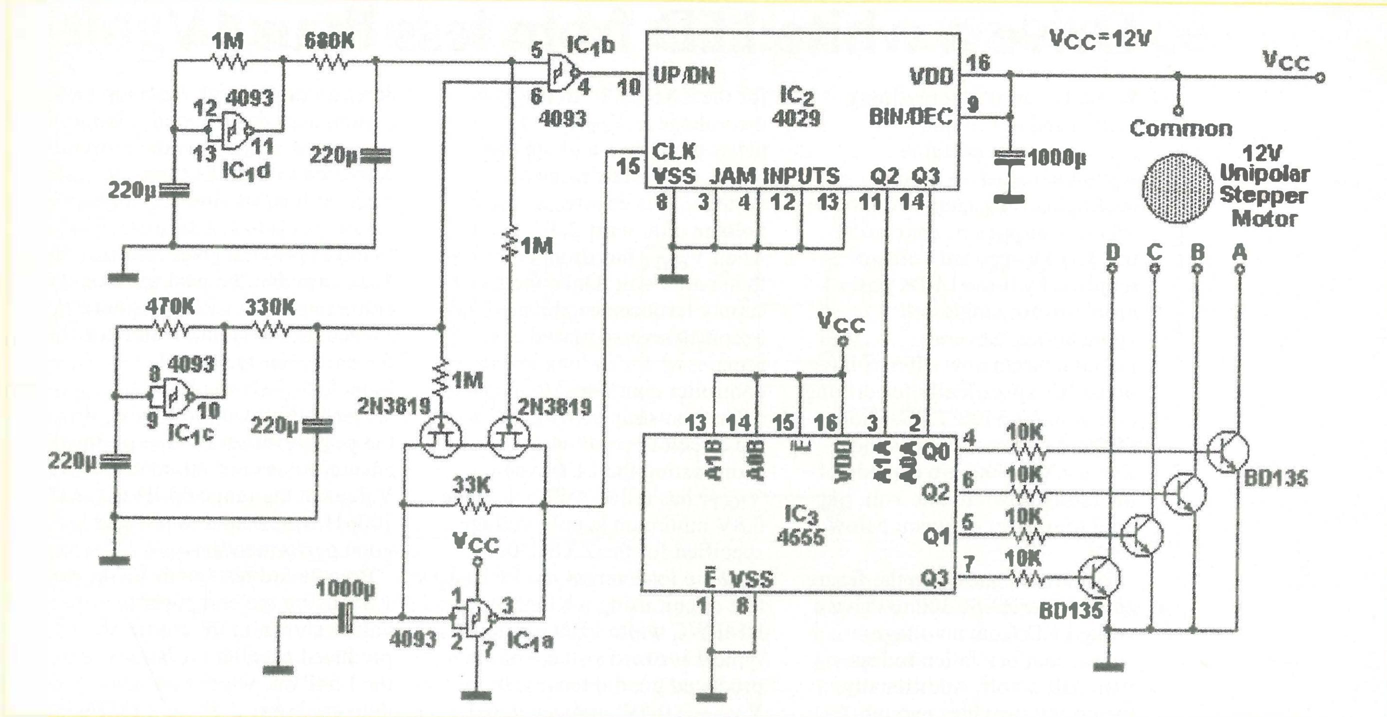
IC2’s outputs Q1 to Q4 produce a 4 bit binary number. This needs to be converted to a decimal 1 to 4 in order to sequence the Random Clock’s unipolar motor phases. The two centre digits of the binary number repeat every 4 steps, so these outputs (Q2 and Q3)are selected to clock 2 to 4 line decoder IC3. It is recommended that Motorola (MC1 xxxx) versions should be used for IC1-IC3.

Four BD135 power transistors serve as current amplifiers at the outputs of IC3. Since stepper motors can work up quite a heat, and full power is not required, a suitably rated resistor may be inserted in the motor’s common line if desired. A 12V 3W (250mA) power supply is required.

The Random Clock further requires a gearbox which will move its hours and minutes hands at different speeds. This is easily constructed from a selection of gears.

A further possibility is to use the circuit to cascade lights up and down a Christmas tree. If LEDs are used for the lights, suitably rated ballast resistors need to be wired in series with outputs A to D.

Rev. Thomas Scarborough
Cape Town
South Africa

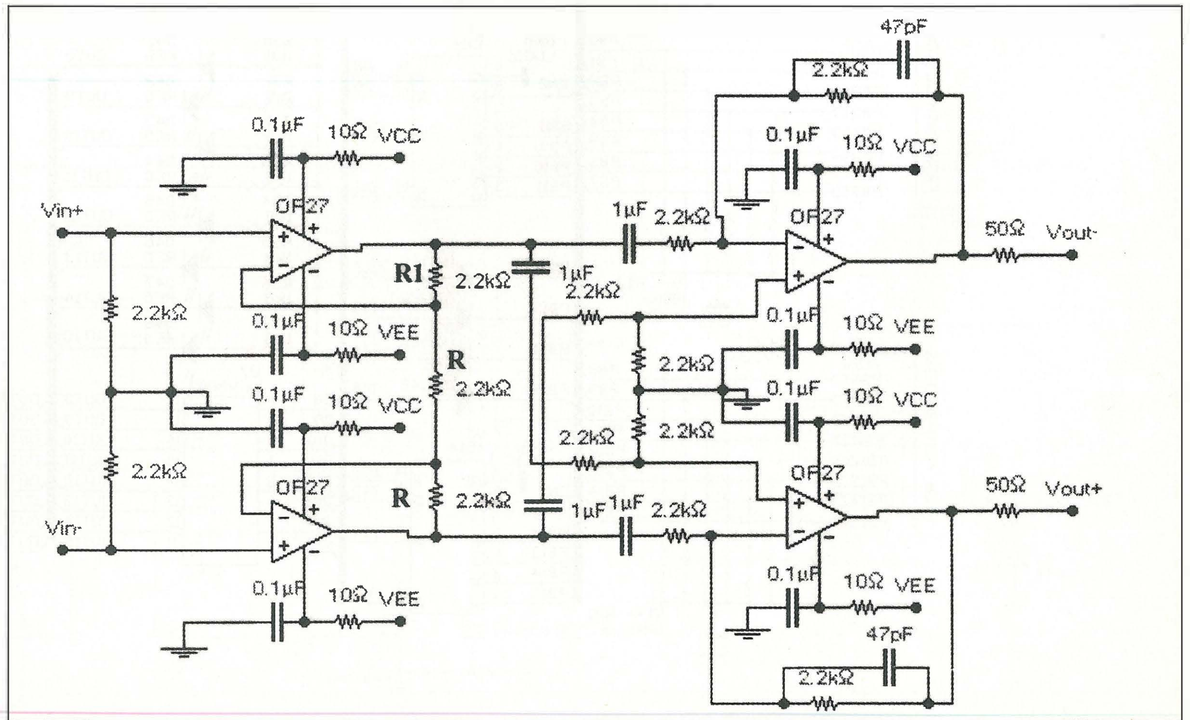


Instrumentation amplifier with differential output

An instrumentation amplifier is used to convert a differential input from a floating source, such as any transducer, to a single ended ground referenced signal with low output impedance. But in some cases this output needs to be driven over a long distance. To drive long distances, balanced differential drives are desirable.

Here a three op-amp instrumentation amplifier is modified to have a differential input and a balanced differential output. This has a differential gain of six and lower cut-off frequency of 72Hz and an upper cut-off frequency determined by the op-amp and maximum signal swing. The gain can be changed by manipulating the ratio a = R1/R - by changing the value of R alone the gain can be modified. This structure provides pre-amplification and driving with low source impedance.

S. Vijayan Pillai
Kerala
India

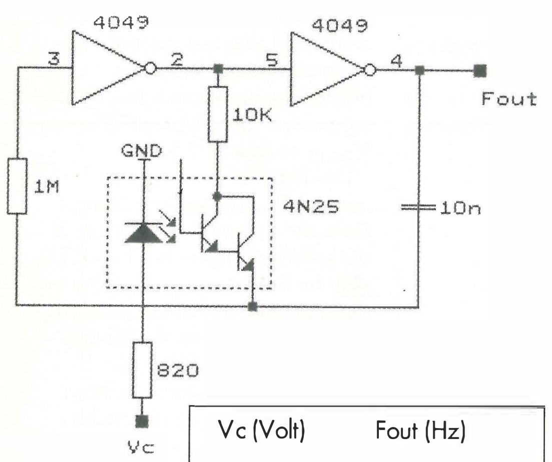


Simple VCO

A description is given of an oscillator of which the parts are floating and nevertheless whose frequency can be controlled by a grounded DC source (see schematic diagram). The oscillator consists of two inverters connected in a well-known way with the frequency determining capacitor and resistor. The resistor is replaced by a resistor in series with a Darlington transistor of an opto-coupler, of which the ‘resistance’ is controlled by the current through the diode.

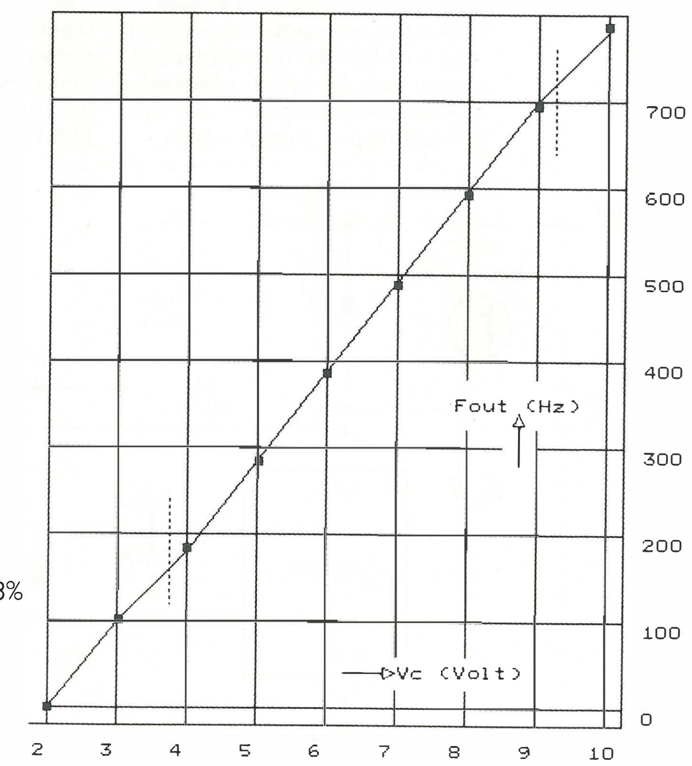
The relation between frequency and control voltage is reasonable linear (see table and graph).

W.E.C. Dijkstra
Waalre
The Netherlands



Vc (Volt)	Fout (Hz)
10	788.5
9	695.0
8	597.2
7	496.2
6	393.0
5	289.2
4	189.9
3	101.0
2	32.5

Linearity 3%



Drive a white LED from less than 1V

White LEDs are increasingly being used to provide illumination in portable equipment, such as display backlights for pagers and mobile 'phones. However, generating the 3 to 5V forward voltage required by these LEDs poses problems for single cell applications. Several manufacturers now offer voltage boost ICs specifically for driving one or more white LEDs. Some of these devices, such as the Zetex ZXSC300, are capable of operating down to one volt, but tend to run out of steam below 0.8V.

The circuit shown in the figure enables the ZXSC300 to drive a white LED from a voltage source that has fallen to less than half a volt. Additionally, the circuit provides enough power to supply over 3V to an external load.

On power up, the ZXSC300 receives supply current via D1 and starts to oscillate. The device functions as a PFM (Pulse Frequency Modulation) controller which steps up the battery voltage, V_{BATT}, using L1, TR2 and D3 in the familiar 'voltage boost' configuration. The voltage, V_{LED}, on C2 then rises to a level sufficient to forward bias the LED. At the same time, D2 becomes forward biased and provides a 'bootstrapped' supply voltage for the ZXSC300. In this way, the voltage at V_{CC} (pin 1) is never more than a diode drop below the LED's forward voltage. This ensures a supply voltage of at least 2.4V, even when V_{BATT} has dropped to less than half a volt. Once the LED supply has been established, D1 becomes reverse biased and remains so for as long as the controller continues to operate.

The bootstrap scheme allows the circuit to continue illuminating the LED when V_{BATT} has fallen well below the 0.8V minimum supply voltage specified for the ZXSC300. With no load across the LED, a test circuit using a Kingbright L54PWC white LED having a typical forward voltage of 3.6V produced good intensity at V_{BATT} = 0.5V, and generated reasonable light output with V_{BATT} as low as 0.3V.

Connecting a load, R_{LOAD}, across C2 steals power from the LED. However, provided the load is not excessive, the LED intensity remains acceptable allowing several milliwatts to be delivered to the load without dimming the LED.

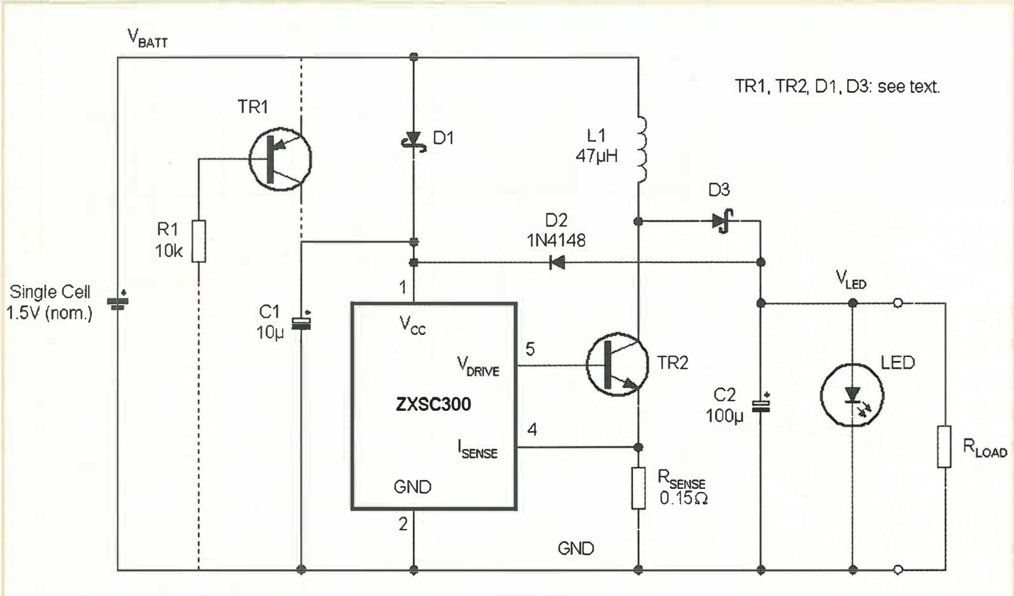
Circuit components should be chosen carefully. D1 and D3 should be low drop Schottkys, and switching transistor TR2 should be a low saturation device such as the ZTX689B or FMMT617. Resistor R_{SENSE} determines the peak inductor current and, consequently, has a significant bearing on the power delivered to the LED and external load (if fitted). Values around 0.1Ω to 0.22Ω were found to provide good results. Take care that the peak current delivered to the LED does not exceed the maximum value for the particular type used. Inductor L1 should have a current rating well in excess of the peak level set by R_{SENSE} to ensure it does not saturate. Values in the range 33μH to 100μH were found to provide good performance.

Breadboard tests with V_{BATT} = 1.0V using the component values shown in the figure produced excellent brightness in the L54PWC white LED and delivered over 3.3V to a 1kΩ load – more than enough to power a range of low power circuitry. With V_{BATT} reduced to 0.5V, V_{LED} was measured as 3.0V with R_{LOAD} = 1kΩ, and the LED intensity was fair.

The voltage to the external load can be increased by connecting a signal diode in series with the LED, or by connecting two or more LEDs in series. With no external load connected, the test circuit maintained reasonable brightness in two series-connected white LEDs with V_{BATT} as low as 0.65V.

Diode D2 is necessary to prevent R_{LOAD} stealing current from the supply on power up. If the external load is not fitted, D2 may be linked out and C1 can be omitted. The minimum power-up voltage depends on the diode type used for D1. Using a BAT49, the breadboard circuit started operating at just under 1.0V. This can be reduced still further by replacing D1 with TR1 and R1. If TR1 is a low saturation device, the minimum power-up voltage can be as low as 0.9V. The disadvantage, however, is that TR1's collector-base junction becomes forward biased by V_{LED}, resulting in wasted power in R1.

Anthony H. Smith
Biddenham
Bedfordshire UK



Using a parallel port to measure capacitance

This cost effective design solution measures the sample capacitance in laboratory experiments. Some of the samples, while in heat treatment, show changes in their capacitance. This can be measured using this simple circuit compatible with a PC's LPT port. A 555 timer IC wired in an astable mode generates a frequency output at its pin 3. The frequency of the multivibrator depends on the charging resistor R_A, discharging resistor R_B and the capacitor C. The resulting frequency = 1.414 / (R_A + 2 R_B) C. Instead of the fixed capacitor C, a sample which undergoes changes in capacitance value can be mounted and hence the frequency totally depends on the sample capacitance. The output of 555 timer pin 3 is wired to pin 10 of a PC's LPT1 port ('acknowledge' input in the status port 0x379) as an input signal. The control program can be written any language which has to monitor the number of changes of state per second i.e., frequency, and in turn the capacitance can be calculated from the formula given above. This design shown in fig.1 helps the experimentalist to go for phase transition measurements using simple interfacing with the parallel port.

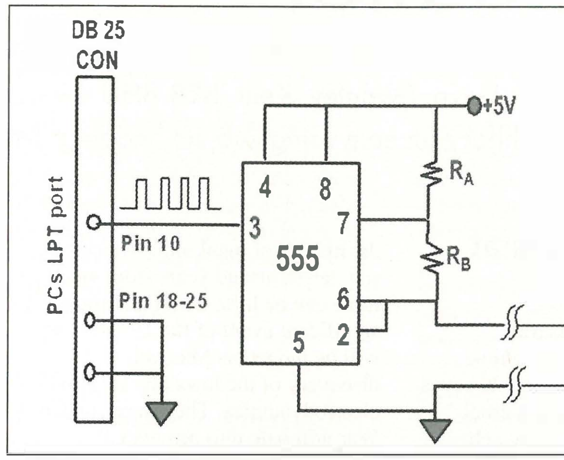


Fig.1. PC's LPT port measures samples capacitance.

J.Jayapandia
Tamil Nadu
India.

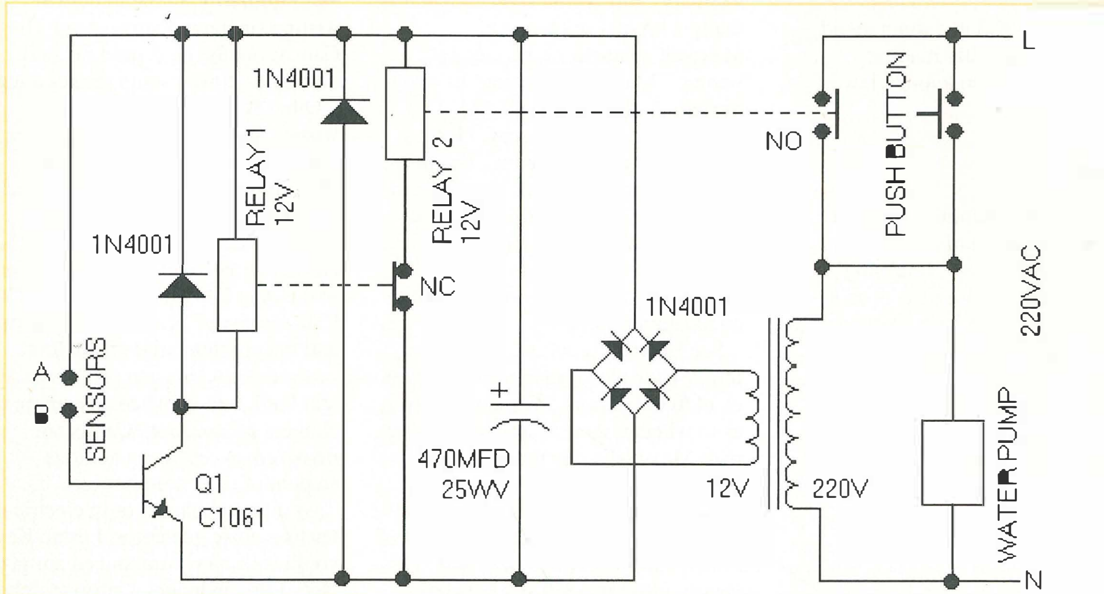
Electronic water level interlock

The circuit, which is basically an interlock, disconnects a water pump and itself from the mains as soon as the water rises to a predefined level and touches the sensors A and B. The sensors (common pins or iron nails) are held suspended in the tank at a level just below the water overflow outlet.

Pushing the push button energises the relay 2 and turns on mains AC supply to the pump and sensing circuit. As the water is still below the sensors A and B, Q1 is off and relay 1 is de-energised and is conducting. Relay 2 is energised thereby continuing the AC mains supply to both pump and sensing circuit.

Whenever the water touches the two sensors, Q1 turns on, energizing the relay 1 and de-energizing relay 2 and the mains is disconnected from the pump and sensing circuit. Pushing the push button again repeats the cycle.

Ejaz ur Rehman
Islamabad
Pakistan



LETTERS to the editor

Letters to "Electronics World" Highbury Business Communications, Nexus House, Azalea Drive, Swanley, Kent, BR8 8HU
e-mail EWletters@highburybiz.com using subject heading 'Letters'.

Throwing glasses at stone houses

I feel sad that my adversaries persistently lead with their chins. However, this one also keeps his eyes tight shut. A turkey shoot is cruel, and I do not feel proud of myself.

In his letter of December 2003, Kevin Aylward wrote; ".... There are also those that are prone to use such terms as .... intermixed with various .... technical terms in an effort to mislead or obscure the real issues, or because they do not actually understand the real significance of these terms .... those with only a passing acquaintance often misunderstand the finer and more subtle points being presented by individuals who do have such experience."

In his letter of January 2004, Kevin continued; ".... the best current and fully accepted theory of EM is Quantum Electrodynamics (QED) for which Richard Feynemann got the Nobel Prize. The theory explains EM .... Maxwell's equations are simply wrong. They cannot be used to explain all the results of EM. This was decisively proved in the early 1900s ....

What a pity Kevin did not avoid this gaffe by actually reading Feynemann; "From a long view of the history of mankind – seen from, say, ten thousand years from now – there can be little doubt that the most significant event of the 19th century will be judged as Maxwell's discovery of the laws of electrodynamics. The American Civil War will pale into provincial insignificance in comparison with this important scientific event of the same decade." – R.P. Feynman, R.B. Leighton, and M. Sands, *Feynman Lectures on Physics,* vol. 2, Addison-Wesley, London, 1964, c. 1, p. 11. (see http://www.ivorcatt.com/2804.htm)

It gets worse; "The special theory of relativity owes its origin to Maxwell's equations of the electromagnetic field." Einstein quoted in ed. Schilpp, P.A., "Albert Einstein, Philosopher – Scientist," *Library of Living Philosophers*, 1949, p62. (Perhaps Kevin should look for some different people to drool over.)

What a pity Kevin did not read anything about The Catt Anomaly either, but again relied on guesswork, guessing that there was a link between The Catt Anomaly and Maxwell's Equations, which there is not. ".... the so-called 'Catt anomaly', this whole subject matter is really a bit of a red herring. Maxwell's equations are simply wrong. They cannot be used to explain all the results of EM." - Kevin, letters, *EW* January. Here, Kevin is in good company. The only previous attempt to link The Catt Anomaly with Maxwell's equations was by Howie, Head of the Cavendish, see http://www.electromagnetism.demon.co.uk/stoppress.htm

See Howie's letter at http://www.electromagnetism.demon.co.uk/07091b.htm "The central issue as to whether there is anything wrong with Maxwell's equations is not I believe best resolved by a vote following some kind of public debate which might degenerate into a kind of Punch and Judy show.' - Howie. This clearly misrepresents my October 2001 letter .... Also note that the definitive statement of The Catt Anomaly, (at http://www.electromagnetism.demon.co.uk/catanoi.htm) and also on p3 of the book "The Catt Anomaly" http://www.ivorcatt.com/28anom.htm, which Howie says he received by recorded delivery, does not mention Maxwell's Equations. – (I Catt, 30th Oct 2001)"

As to Nobel Prizewinners, two so far have made fools of themselves over the Catt Anomaly; Salam in *Wireless World*, December 1982, and more recently Huxley, see http://www.ivorcatt.com/28anom.htm; "Dear Mr. Catt, I much enjoyed our conversation at dessert in Trinity a week ago....I confess that I find it unsatisfactory that you dismiss Pepper's discussion as "drivel" (p. 5, bottom) and make no attempt to explain what you think is wrong with it. An analogous situation exists in nerve conduction, the field in which I worked for many years with Alan Hodgkin. The best-understood nerve fibre ..... Yours sincerely, Andrew Huxley."

I know from personal experience that old boy Huxley was not gaga at the time. All the same, extraordinarily, in the middle of writing (incompetently) about The Catt Anomaly, he drifted off into discussing how a squid shakes a leg.

Other Nobel Prizewinners have wisely, and frustratingly, held their peace. At the next level, "Pepper FRS" (worth doing a Google search for) fell disastrously at the Catt Anomaly fence, as did Howie FRS. However, as Nigel Cook pointed out in the Aug 2003 EW Editorial, "The Catt Anomaly" is actually a question, and the problem arises from total contradiction between professors and text book writers when answering this elementary question. Catt is not involved, except as an anxious student of these luminaries.

As a Drivelmaster, or in electrical terms a noise generator, I think Kevin could well merge unnoticed among Nobel Prizewinners. Unfortunately he lacks the dynastic or patronage background. Trinity High Table is full of them. A Nobel Prize has to be proposed by an existing Nobel Prizewinner or some such. For some reason, despite all his social graces, they don't hand one to their buddy Ivor.

Ivor Catt
St. Albans
Hertfordshire
UK

Throwing stones in glass houses II

Thanks to Kevin Aylward (*EW*, Jan) for promoting quantum electrodynamics (QED) as the solution to the light speed of electricity, via 'virtual' photons. Perhaps Kevin missed my article on this subject, dealing with particle and force mechanisms? (*EW*, April 2003.)

Maxwell's equations can't be derived from QED at all, and efforts to derive them from superstring theory (general relativity tensors with 10 or more dimensions of space) spew out a welter of solutions and do not lead uniquely to Maxwell type equations, let alone Maxwell equations with the right constants!

The so-called virtual particles in QED only increase the magnetic moment of the electron by 0.115965 percent. It is this trivial number which has uniquely been computed to about 13 decimals. Dirac first claimed that the magnetic moment was exactly 1 unit, so I suppose that would be accuracy to an infinite number of decimals if it had been correct (1.0000...)!

Clever Feynman does actually admit, I find, in his book 'QED' that QED predicts the EM force to be 137 times too high; he says this is the 'greatest damn mystery'. On the contrary, it is actually the strong nuclear force, not EM! For EM you need what Kevin calls the 'wrong' Maxwell result that spinning charges radiate continuous (non-quantum) energy!

The continuous exchange of energy with surrounding particles causes EM forces with the correct strength as proven in the April EW article. By the way, the derivation of the equation curl E = curl (cB) = +/- c.curl B used in the April article is based upon the unique fact that both the EM vector field equation E =cB (derived from experimentally proven F = Bil = Eq = Bql/t = Bqc) and the definition of the curl vector operator both describing perpendicular fields, so c is just a vector multiplier.

Finally, the Chairman of the Nobel Prize is not God, but more like a sports referee: prizes are generally awarded for acknowledged races. In the absence of any intelligent competition, Ivor Catt has no motivation to use QED. Mendel's genetics were ignored during his lifetime, whereas Darwin had instant fame (too much for his liking!) because his work had a ready-made competitor (the Church). Success of IC's work after 30 years of being neglected thus relies on an urgent run-in with today's science bigots.

Nigel Cook
By email

Ooooo no

I've gone back to looking at the old devices and the crumbling data books and I'm quite sure that the first character in 'OC71' etc. is an O and not a 0.

Pro-Electron coding certainly applied before transistors, and the first letter was the code for either the heater voltage (e.g. 'E' = 6.3V) or current (e.g. U = '100mA'). So the most one could say is that O (not 0) is the code for zero voltage or current.

Incidentally, the US JETEC (not JEDEC - that came later) code has the first number for the approximate heater voltage (6 or 7 for 6.3V, for example). But the cold-cathode rectifier used in car radios was an OZ4 not a 0Z4.

Editors 1 Web sites 0.

However, the editorial in this issue doesn't score many Brownie points. EMC controls are NOT a conspiracy, and not worthless. If you look at the emission standards you will see that emissions are measured at a reasonable distance from the source - 3m, (in a few cases) 10m (for household use) or 30m (for industrial equipment). This is because it was realised a 'long' time ago that it's impracticable to demand emission levels and immunity levels for most equipment that ensure the absence of interference at much closer distances.

Your proposal that the regulations don't work or are not worth the paper they are printed on is a gross insult to me and my colleagues who work on these standards, and are paid by industry for doing so. Do you seriously imagine that we are employed by 'industry' (not Government) to waste everyone's time and money, especially that of those who pay us?

The point about electronic equipment on aircraft is two-fold. Much aircraft equipment was designed before carry-on electronics was present in large amounts, so it has never been tested for immunity to the emissions that may be produced. Furthermore, the details of those emissions are simply not known: there are millions of units of thousands of model numbers that may be present on an aircraft. So, it's a wise precaution to control the use of the equipment at critical times - take-off and landing. Mobile phones are a special case - if airborne at lowish levels (say below 2000m) they can communicate 'too well' with base stations over a wide area, and thus potentially disrupt the system.

Then you take an opposite stance on links between EM fields and cancer. The only reason that 'the jury is still out' is that some people have an anti-technology agenda and refuse to be convinced by the huge body of negative results of all the legitimate research. You can see how ludicrous some of this cultivated anxiety is: people are bamboozled into objecting to a cell-phone base station while living near a 5 MW TV transmitter and quite happily using their mobile phones, both of which give hundreds of times the field strength from the base station.

Finally, your observation in Rhodes is way off beam. You may be right about the feeder being suitable for 125 A, but why on earth should the purely British IEE Regs (BS 7671) apply in Greece? Quite apart from the fact that they don't apply to 'supplier's works' anyway! In any case, in southern European countries, there is no electrical heating load and household supplies are often not the 60A or 100A rated supplies we are used to here, but only 25A or so.

John Woodgate
By email

It was not my intention to insult those in the EMC fraternity who I'm sure generally do a good job. The point I'm making is how many of the regulations are actually needed? How much does it cost the industry and do the consumers get good value (since ultimately they pay for it)? Regarding the possibility of some 'bodies' wasting everybody's time and money – I think you will find this happens an awful lot in Brussels. And your last point about Rhodes – whilst I agree that the IEE have no jurisdiction down there – they surely have a similar body. And since there is no mains gas on the island, all apartments have water heaters of at least 2kW and this pole fed about 20 of them and a string of bars! But again, you missed my point. – Ed.

Articles wanted

Wanted badly (written well). A continuing series of Back to Basics to answer such question as: What is 'formatting' on digital discs; what does 'finalising' do; what does 'SIM card' stand for and what does it do; why do CD-R and CD-RW cause such amateur frustration in exchanging copies which don't work in players or PCs; and even more so on DVD+R AND +RW - the list is endless and causes glazed looks on the most informed of experts.

Never mind nanometric stuff we can't see, let's have someone knowledgeable to impart the gen!

Alan Watling
Colchester
Essex
UK

Ooooooooooo

In the words of 'Big John' alias 'The Duke', "never apologise - it shows weakness" (after all you may be right). The addition in brackets is mine.

Correspondent J.I. Anderson is only partially correct with reference to numeral 0 (zero) to indicate zero voltage. An example of this was the 0Z4, a rectifier, without a discrete heater, mainly used in car radios. This tied in with the widely used American system of identification for tubes which used 5 for 5 volts, 6 (and 7) for 6.3 volts, 35 for 35 volts and so on.

However, UK manufacturers such as Mullard adopted the European system of nomenclature in which the initial alphanumerics were letters and the first of these indicated the heater voltage (or current) for example D for 1.4 volts, E for 6.3 volts and U for 100 milliamps. Upper case letter O was adopted to indicate (logically but confusingly) zero volts. Thus we have OC (letters) indicating a transistor (C was used in the Mullard system to indicate a triode) and OA to indicate a semiconductor diode (A indicating a single diode).

If any doubts remain refer to, for example, the Mullard Maintenance Manual, Second Edition where it will be found that the semiconductors with a leading O lie in logical alphabetical sequence between MW and PC. The physical dimensions of the leading O and final 0 in, for example, the OC70 transistor (p.155) will be found to different also.

'Ed' keep up the good work, I have taken the WW and its descendants since 1949 and hope you have something better to publish than the antique garbage I have written above.

John Winterburn
By email

The last O

There seems to be some confusion and carelessness in some quarters over the use of '1', 'I', '0' and 'O' for numbering semiconductors. Before the Pro-Electron system came into use the situation was fairly chaotic but manufacturers in the Philips empire such as Mullard used the Philips valve coding system. One or two manufacturers such as Brush Crystal and, I think, BTH also followed Philips' example. The system had O (oh) = zero heater volts, A = single diode, C = triode, 6 and 7 = wire-ended devices. It soon ran out of options. To support the above statements I have attached a scan of a page from a Mullard 1956 valve data booklet and an image of an OC201 silicon transistor because I haven't an OC70 in my collection. Note that Philips' system was being modified by using 2 for silicon and leaving other numbers for germanium.

MULLARD

Valve Type		Mullard Direct Equivalent	Other Equivalent
OA81 ..	..	OA81	—
OC16 ..	..	OC16	—
OC44 ..	..	OC44	—
OC45 ..	..	OC45	—
OC65 ..	..	OC65	—
OC66 ..	..	OC66	—
OC70 ..	..	OC70	—
OC71 ..	..	OC71	—
OC72 ..	..	OC72	—
OM1 ..	..	CY31	—
OM3 ..	..	EB34	—
OM4 ..	..	EBC33	DH147
OM5 ..	..	EF36	OM5B
OM5A	..	EF37A	OM5B
OM5B	..	EF37A	—
OM6 ..	..	EF39	W147
OM7 ..	..	EF39	—
OM9 ..	..	EL32	—
OM10	..	CCH35 (a.c./d.c.) / ECH35 (a.c.)	X147
OP41	..	PENB4	AC4PEN
OP42	..	PENA4	AC2PEN, PT4(*F*)
P2 ..	..	—	—
P12-250	..	*	LP4, PP3/250, PX4
P27-500	..	—	PP5/400, PX25
P41 ..	..	—	—
P61 ..	..	—	—
P220(*T*)	..	—	—

The supporters of 0C71 are misguided in using valves 12AT7, 6J7 or 0C3 as examples because they represent the US numbering system where the first number is approximately the actual heater/filament voltage, the letter very roughly indicating the function, and the last number approximately the number of electrodes. Examples are 0C3: a gas-filled regulator diode with an extra internal connection, and 0Z4: an ionic heated full-wave rectifier in an earthed steel envelope.

I could rant on about the ignorant who referred to diodes as IN4148 instead of 1N4148, for example, but I won't.

Richard Hubbard,
Whitstable,
Kent
UK

How low do we need?

I've been intrigued by Cyril Bateman's articles about the measurement of very low levels of distortion which may be introduced by components in analogue circuits. Such low levels may well be of interest and concern in the design of high quality measuring instruments, but Cyril seems to suggest that the same precautions are relevant to ordinary audio equipment (the stuff that used to be called hi-fi?). I worked for Ampex for many years and was often involved with sound recording studios and broadcasters.

I cannot see that practical sources of audio can be "pure" to the extent that Cyril's measurements of very low distortion products are relevant. The heterogeneous collection of analogue boxes found in recording studios contributed 'their sound' to recordings made in the past. Those with 'golden ears' attributed a particular sound to each brand of (analogue) recording tape. Now we have 'digital', so the end-product may have been through several codecs, and then a compressor, to yield the popular MP3 recording format or DAB digital radio.

Lastly, to harmonise with the precision of Cyril's approach to distortion measurement, which I'm sure is very valuable in a relevant situation, I think the form of the trimming groove he refers to in film resistors is a helix and not a spiral. This confusion is encouraged by the common reference to spiral staircases, which are really helical!

Justin Underwood
Much Marcle
Herefordshire
UK

Audio experience

D. Lucas' assumptions concerning my age, knowledge and experience just make his letter (October) suffer from all the faults he sees in mine (July). So, as many writers of letters to *EW* currently do, I have to admit my age, 53 and say a bit about myself. I hope this will stop Mr. Lucas to consider contradictors as necessarily being kids.

Involved in electronics for more than 35 years, I have repaired, built and even conceived many electronic designs. Among the amplifiers I built, there are five different J. Linsley-Hood projects (including the class A in 1971 and the latest mosfet that D. Lucas has modified) and the first version of D. Self's blameless amplifier.

Already having the two compilations of *Wireless World, 'High fidelity Designs'*, I bought my first regular issue in December 1978. It contained major contributions by two 'giants': one by P. Baxandall titled *Audio power amplifier design* and the other by S. Linkwitz titled *Loudspeaker system design.* Could it be a better introduction to serious audio-related reading?

Since 1975, I've been passionately studying audio and particularly solid-state amp designs, collecting everything I could get on the subject. Among many articles, three studies had a great influence on my thinking. The first was the above Baxandall one, but it was unfortunately not completely published, as far I know.

In the eighties, in the French magazine *L'audiophile*, Hephaïstos published a very interesting series, unfinished, dealing with possible thermal and memory distortions: its experiments failed to prove them in conventional bipolar amplifiers with standard feedback structure.

The third study, by D. Self, starting in 1993 in *EW+WW*, is the most complete and very easy to read. It was wonderfully welcome because it had the virtues of answering many questions I had asked myself for a long time and that of unveiling some important distortion mechanisms, which were never addressed before, particularly by the subjectivist camp. During the years, I have been more and more intrigued by the debate about differences between amplifiers, which is far more raging than those between loudspeakers.

D. Lucas raises a fundamental question: from where does come the "emotion" he talks about? Till now, I have been aware of that emotion could be driven by electric currents in the brain but never in electronic circuits, as intellectually exciting as these can be. If emotion is in the input signal, what mechanism does remove it in a given amplifier and respect it in another one with lower specifications? I spent years asking myself similar questions.

As controversial it may sound, I have made up in my mind that what gives an apparently more detailed rendition is nothing else than a bit of distortion and noise, which are then not anymore considered as faults. The article 'Can noise improve your hearing?' *EW+WW*, Dec 1993, p 976 confirms this point of view, regarding noise.

I have numerous examples where audio circuits designed under 'careful listening conditions' leave some non-linearity to be dominant in the transfer of the signal. The result of such subjectivist approaches is the emergence of an enormous amount of unreliable and contradictory designing rules. The objectivist school feels better to obey to more firmly established guidelines, which nevertheless do not exclude controversies. It is a happy fact that a growing number of competent engineers, some under the banner of EW, are now fighting audio myths of subjectivist emanation with strong arguments. After my assertion about the appeal of distortion, T. Callegari (*letters*, November) asks: why should designers spend so many efforts to avoid it?

Let's have a look at the domain of photography: aberrations to optics are non-linearity to electronics. An engineer designing a lens will certainly try to get the best sharpness out of it. However there are some subjects (portraiture, for example) for whom a soft or foggy effect may be desired. The easiest way to get it is then to fit an adequate apparatus, some kind of smoothing filter, on the lens. But leaving this filter permanently in place would certainly make all the photos having the same boring style.

The situation is similar in amplifier design. An engineer will normally try to design the most accurate one. If a bit of non-linearity is a desired feature, the easiest way to introduce it is prior to the amp input, in a very controllable manner, by using some kind of "niceness" (D. Self's word) processor. Among these pages, Ian Hickman has shown how to generate various non-linearities. A very interesting figure, in *EW* March 1999 p 226, shows how to generate an "ideal" spectrum of regularly decaying harmonics. In combination with a bit of noise, a tailored bandwidth, and a blameless amplifier fitted with a few ohms resistor at its output, you can get the same transfer function as a famous SE tube amp: this procedure would be a perfect subject for a thesis.

Finally, contrarily to optics, amp designing for very high audio performances is not complex and does not cost more: the number of components is not great and good standard quality is sufficient to obtain reliable results. One can prefer having nicely distorting amplifiers but it is considering them as being musical instruments, just as do jazz and rock musicians. They are perfectly right to do it, but literally speaking, such amplification is not anymore in the territory of 'high fidelity'.

An example of the cascode connection that W. Cross (*letters*, October) seems to think of can be found in the Y. Ezkhov amplifier (*EW*, September 1999): the bias of the common-base transistors is floating, clamped to the tail of the input pair. Such connections are used in the OPA 627/637 or in some sophisticated circuits in Halcro, Lavardin-Hephaïstos or Sansui amplifiers, to name a few. I do not see great interest, at least for non-inverting amplifiers with a long tail pair input, in the popular cascode connexion where the bias is referenced to ground.

As long as no precise technical information is given to *EW* readers, D. Lucas's reference to Krell amplifiers comes only as a free advertisement and only indicates that audio designers can afford extravagances.

I find intellectually exciting the controversy among the writers of *EW* letters as far as it remains technical. But I cannot give any credit to people who seem to consider audio components as interpreters of music: I have seen criticisms about the 'excessive neutrality' of amplifiers! The aim of my previous and somewhat provocative letters was a prayer to *EW* to maintain its high standard regarding audio and avoiding recent attempts of intrusion of boring and peremptory claims about the subjective goodness of circuits and components.

EW is a technical magazine which has always published innovative articles with a minimum of subjectivity and which never the less had had a profound influence all over the world. The whole lot of recent articles, contrary to a few letters, proves that its traditional high standard for audio is intact. There are other magazines, with a far greater audience than *EW*, which perfectly entertain their readers with considerations full of emotion.

Concerning the current content of *EW*, my only regret is the disappearance of the nice illustrations.

Sébastien Veyrin-Forrer
Saint Chartres
France

Wheatstone accuracy

Referring to the letter 'Meaningless Algebra' in the November issue, I would query the statement that using 1% resistors in a Wheatstone bridge that you get 1% overall accuracy. Remembering that the balance conditions for a bridge are R1/R2 = R3/R4, then putting limit tolerances of 1% in the least favourable directions means that the overall accuracy tolerance is actually 3%, 1% being contributed by each of the three bridge resistors. Hence for a bridge to be accurate to 1% we need resistors in the bridge to have accuracies of 0.03% or better.

Arthur Bailey
Ilkley
West Yorkshire UK ■

An introduction to network analysis II

In his second article on circuit simulation, John Ellis explains how the equations for determining circuit characteristics are programmed in software, leading off with a discussion of how to program with complex numbers.

Some programming languages have complex numbers as a standard variable – others don't. Fortran is one of those that does. Equation 21 from the end of last month's article

$$V_{out}\left[-\left(\frac{1}{z_r}+\frac{1}{z_c}\right)\right]=\frac{-V_{in}}{z_r}$$

can be written in Fortran more or less as shown, where the variables z_r and z_c have been declared as complex along with V_{in} and V_{out} – even though V_{in} might have only a real term as the resistor did. A complex number in Fortran is declared thus:

```
complex (selected_real_kind (P=14, R=300)) :: zr,
zc, vin, vout
```

and each complex component defined as for example by:

```
zr = cmplx (R,0)                                  (22)
```

Unfortunately, C does not know about complex numbers by default. But C is able to have a structure defined, so it is possible to add complex numbers. Since C will not know how to multiply, divide, subtract or add complex numbers, the four basic mathematical operations will have to be added too, as functions.

A complex structure type can be defined with the following:

```
struct  complex {double re; double im;};
```

This declaration has to be first, so that complex functions may also be defined. Then, the complex maths routines are prototyped as functions returning a complex number as in **List 1**.

List 1. Complex maths routines are prototyped as functions returning a complex number.

```
struct   complex cxadd(struct complex z1, struct complex z2) ;
struct   complex cxsub(struct complex z1, struct complex z2) ;
struct   complex cxmul(struct complex z1, struct complex z2) ;
struct   complex cxdiv(struct complex z1, struct complex z2) ;
```

List 2. The four basic operations.

```
(A + jB) + (C + jD) = (A + C) + j (B +D)
(A + jB) – (C + jD) = (A – C) + j( B – D)
(A + jB) * (C + jD) = (AC – BD) + j(BC + AD)
(A + jB) / (C + jD) = ( (AC + BD) + j(BC – AD) )/(C*C + D*D)
```

The functions are written out, as usual, after the end of the main program and return the complex result. The four basic operations are shown in the **List 2**. Listings for these functions are available from the author via *EW*.

Even being able to define complex numbers in C, the use of them in a C program is cumbersome. Each expression has to be written in long hand. Thus, the expression involving the series combination of a resistor r and a capacitor c with equivalent complex impedances defined as

```
zr.re=r;
zr.im=0.0;
zc.re=0.0;
zc.im=–1.0/2/pi/f/c;
```

as defined by the complex definition, and where zr and zc have been declared as struct complex, would be written out as

```
zrc=cxadd(cxdiv(cx1,zr),cxdiv(cx1,zc)));      (23)
```

meaning `(1/zr+1/zc)`, and where `cx1` is a complex version of the real 1, i.e.

```
cx1.re=1.0;
cx1.im=0.0;
```

Writing expressions like this for each line of a calculation is a bit of a throwback to machine-code programming. They could be done as part of an automated procedure for translating circuits into models. Once this procedure was defined the scope for error would be greatly reduced. Of course, this is what commercial simulators will have done, and what one has to pay the money for.

I would not recommend C for this task – at least not for any large circuit, although it is capable of doing the job. It has to be added that C++ offers a solution to this problem.

As Fortran is geared to solving complex numbers and can handle them almost as easily as conventional numbers, I recommend that you use Fortran to write a linkable subroutine to the main simulator, which I would recommend is in C.

The reason I recommend C for the main structure of the simulator is that C is very good at handling text and i/o. The number of times I have tried to write a Fortran program to handle input files which may be ASCII but as a generic binary file, in case it wasn't, or to read and write lines of input or output which may be loosely or undefined – and therefore of indeterminate record length – until the problem is known, or found that Fortran really doesn't like characters outside it base set, a miserly sub-set of the eight-bit ASCII code, is too numerous to count.

Even the old VAX extension of Fortran, which allowed a length parameter to be passed to an output format descriptor, seems to have been excluded in F90. Invariably I have given up and used C. However, modern Fortran has pointers, too, just to point out that Fortran is still reasonably competitive.

The result of solving equation 21 for a frequency sweep from 1Hz to 100kHz for a resistor of 1kΩ and capacitor of 0.1μF is shown in **Fig. 1**. The ratio Vout/Vin is the final vector sum which is determined as follows:

Define gain as complex. Then

`gain=Vout/Vin` (using `gain=cxdiv(vout,vin)` in C) (24)
`amplitude=sqrt(gain.re*gain.re+gain.im*gain.im)` (25)
(a real number)

and

```
phase = atan (v/u)                                (26)
```

(also real)

Here, v (a real number) =gain.im and u (also real) =gain.re as was defined for C; or

```
phase = atan(imag(gain) / real(gain) )
```

in Fortran.

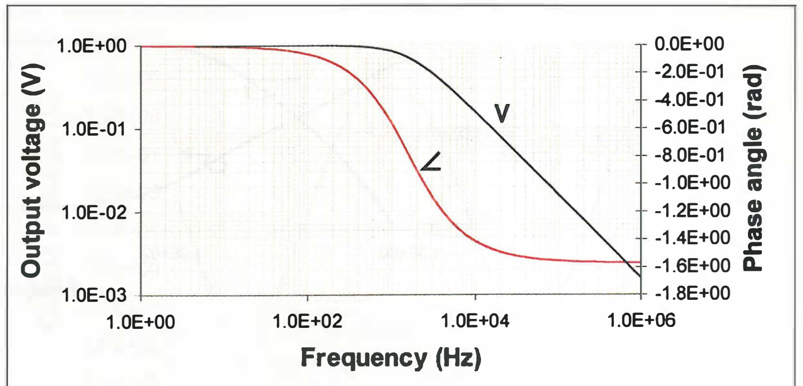


Fig. 1. Output voltage versus frequency for a low-pass filter, where V_{in}=1.0.

Simultaneous equations

A simple one-transistor circuit is shown in **Fig. 2**. It uses the standard four resistors for biasing, and coupling capacitors for the input and output, and a decoupling capacitor across the emitter resistor.

To simulate the small-signal characteristics of this circuit, the transistor is replaced by its equivalent circuit where the input and output impedances are shown by actual resistors based on the small signal values, as shown in **Fig. 3**.

Initially, a calculation is performed to determine the DC operating conditions, followed by a small perturbation to determine the small signal impedances. Thereafter, the

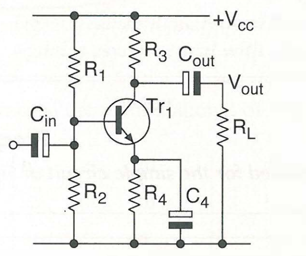


Fig. 2. Basic one-transistor amplifier. Note that C_4 is labelled to reflect its associated resistor.

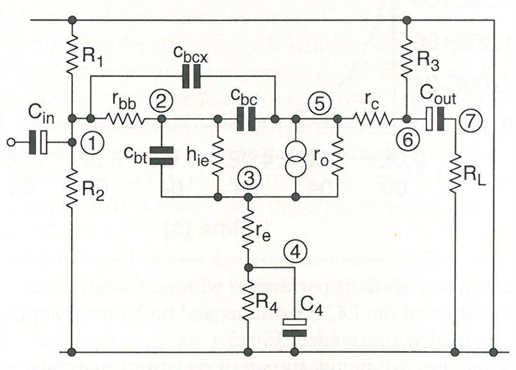


Fig. 3. Small-signal representation of Fig. 2 showing nodes.

$$\begin{array}{c}
\begin{array}{ccccccc} (1) & (2) & (3) & (4) & (5) & (6) & (7) \end{array} \\
\begin{bmatrix}
-\left(\frac{1}{zr1}+\frac{1}{zr2}+\frac{1}{zr3}+\frac{1}{zr4}+\frac{1}{zr5}\right) & \frac{1}{zrb} & 0 & 0 & \frac{1}{zcbcx} & 0 & 0 \\
\frac{1}{zrb} & -\left(\frac{1}{zrb}+\frac{1}{zrch}+\frac{1}{zcbc}\right) & \frac{1}{zrch} & 0 & \frac{1}{zcbc} & 0 & 0 \\
0 & \frac{1}{zrb}+zgm-\left(\frac{1}{zrch}+\frac{1}{zre}+\frac{1}{zro}+zgm\right) & & \frac{1}{zre} & \frac{1}{zro} & 0 & 0 \\
0 & 0 & \frac{1}{zre} & -\left(\frac{1}{zre}+\frac{1}{zrc4}\right) & 0 & 0 & 0 \\
\frac{1}{zcbcx} & \frac{1}{zcbc}-zgm & \frac{1}{zro}+zgm & 0 & -\left(\frac{1}{zrc}+\frac{1}{zro}+\frac{1}{zcbcx}+\frac{1}{zcbc}\right) & \frac{1}{zrc} & 0 \\
0 & 0 & 0 & 0 & \frac{1}{zrc} & -\left(\frac{1}{zrc}+\frac{1}{zr3}+\frac{1}{zc_{out}}\right) & \frac{1}{zc_{out}} \\
0 & 0 & 0 & 0 & 0 & \frac{1}{zc_{out}} & -\left(\frac{1}{zc_{out}}+\frac{1}{R_L}\right)
\end{bmatrix}
\end{array}
\begin{bmatrix} V1 \\ V2 \\ V3 \\ V4 \\ V5 \\ V6 \\ V7 \end{bmatrix}
=
\begin{bmatrix} -\frac{zV_{in}}{zC_{in}} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

Fig. 4. Full matrix expression for the one-transistor small-signal circuit. All values are complex, designated by 'z'. Some combinations have been used for simplification; zrch=1/(1/zcbt+1/zhie); zrc4=1/(1/zR$_4$+1/zC$_4$).

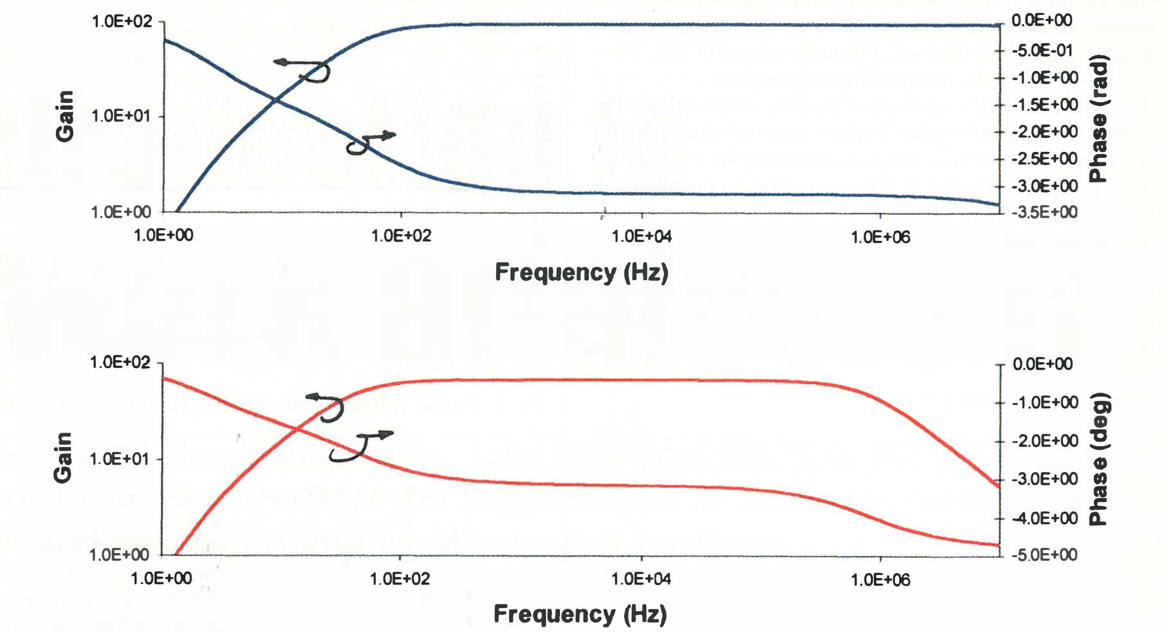


Fig. 5. Response as calculated for the simple circuit of Fig. 2.

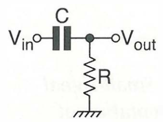
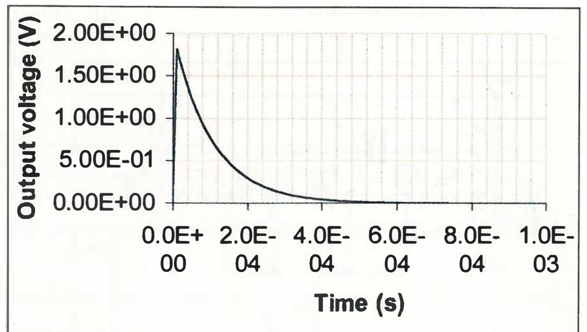


Fig. 6. Transient response of a capacitor/resistor network where steps of 1µs have been used.



small signal analysis is performed with no further consideration of the DC conditions and both power supply lines are in effect grounded, Fig. 3.

To simulate this circuit, the set of equations that must be solved is assembled into a matrix format. There are seven nodes, three additional nodes being included in the transistor equivalent circuit. For a seven-unknown node, the matrix comprises a seven-by-seven array of terms, or coefficients, describing the impedances on each node in terms of all of the others. This is multiplied by the unknown voltages written in a column vector, and the product is equated to the "right-hand side" quantities.

Figure 4 shows the matrix for the simple transistor circuit is shown in full. Note that only values that relate to components on the nodes are assigned values: where there is no component, the matrix entry is zero. There is only one right-hand side value representing V_{in}. The rest of the nodes, as we said earlier, sum to zero.

Although the matrix form may appear daunting, it is very straightforward to determine, and can be done by inspection. For each node, the main diagonal represents its "own voltage". This has a negative sign attached, and then all the impedances attached to it are summed, five components in the case of node 1.

The other nodes only have an impedance where there is a component attached to the node in question. For node 1, there are components attached at node 2 (through rbb) and node 5 (through cbcx). These entries are located so that they multiply by the relevant node voltage in the column vector.

Nodes that are not on the main diagonal all have positive signs. A fixed quantity which is transferred to the "right-hand side" vector of course changes sign as in any expression.

The only other consideration is where there is an internal generator such as the gain given by g_m and the base to emitter node voltage. To obtain the correct signs the direction of the current representing gm is drawn in, as in Fig. 7 from last month's article.

If gm is attached to a node such as 5 where the currents normally enter the node, but in this case exits, g_m takes a negative. For node 3, g_m "enters" and assumes a positive sign as any other current entering the node, and is added to the other impedances. Of course, the whole lot are negated when node 3 is considered on the main diagonal, but the relationship between gm and the other impedances has the same sign.

Note that the matrix here is a complex matrix, and that there are many zero entries, actually complex zeros or (0,0). Where there are more zeros than entries in a matrix, it is known as "sparse". Sparse matrices can be solved using a shorter algorithm, but with iteration.

For a three transistor circuit, 15 nodes were required, but by following the principles illustrated it is not actually necessary to write the full matrix out as it can be constructed directly into a program.

Solving matrices

Matrix operations are written in shorthand as

$$\mathbf{Mx=y} \tag{27}$$

where **M** represents the matrix of coefficients, **x** the set of unknowns – usually voltages or currents – and **y** the set of "right hand side" constants. We have to solve for **x** given **M** and **y.**

Many, if not all, mathematics textbooks which discuss matrices describe the standard inversion procedure which provides the inverse of **M** such that

$$\mathbf{M}^{-1}.\mathbf{y=x} \tag{28}$$

To obtain the inverse matrix $\mathbf{M}^{-1}$, the adjoint of **M** is divided by the determinant of **M**. The adjoint is the transposed matrix of the co-factors, obtained by cross-multiplying all the other row and column elements (minors) for a given element, having "crossed off" the row and column of that element.

The determinant is the number obtained by summing the multiplication of all the coefficients with their minors. The determinant and co-factor matrix involve a lot of calculations, and needs a sign rule attached to the coefficient matrix to preserve the correct signs. Despite being in nearly all maths textbooks this method is rarely used, if ever, in practice. To be fair, more recent maths books discuss better methods.

Perhaps the majority of commercial solvers today use a method of decomposition. A decomposition splits the matrix into two triangular matrices: a lower and upper triangular matrix. There are some variations on this where the matrix is symmetrical. This is true for many calculations involving electric current, heat flow, stress or electromagnetic effects for example.

One, named after Cholesky, obtains an upper and lower triangular matrices which are the transpose of each other. But in circuit simulations the matrices tend to be not quite symmetrical, (e.g. compare the coefficients on lines 2 and 3 above) and the Cholesky decomposition may not be usable.

For nearly symmetrical and other asymmetrical matrices the lower-upper triangular decomposition method (LU decomposition) works well providing that the matrix is soluble. Generally this means that the main diagonal must not contain any zeros, but also preferably that the main diagonal is dominant: that is, numerically larger than the other values.

Ideally the main diagonal should have a negative sign while all the other values are positive, and in general this is also true for circuits. Of course in many sets of equations the main diagonal is arranged to correspond with one of the unknowns, so is guaranteed to have a non-zero value.

Sparse matrices can be solved with the incomplete LU decomposition where only the elements of **L** and **U** are calculated where there is a non-zero value in **M**. This approach is approximate – the full decomposition is in principle accurate – and has to be iterated to improve the accuracy, but is often quicker than a full decomposition, particularly for large matrices. This is because the number of equations in a matrix is increasing faster than a square law for each point added.

The direct LU decomposition works as follows:

In matrix form

$$\mathbf{Mx=y} \tag{29}$$

Write **M** as an upper-lower triangular pair

$$\mathbf{M=LU} \tag{30}$$

Hence

$$\mathbf{LUx=y} \tag{31}$$

By writing

$$\mathbf{Ux=z} \tag{32}$$

we can solve

$$\mathbf{Lz=y} \tag{33}$$

by forward elimination for z. Then solve

$$\mathbf{Ux=z} \tag{32}$$

for x by back elimination.

The bulk of the work in LU decomposition is in splitting **M** into **L** and **U**. If **L** comprises the elements L_{ij} where i is the row and j the column for all rows and columns up to j=i, and the main diagonal of U is unity, then, for example,

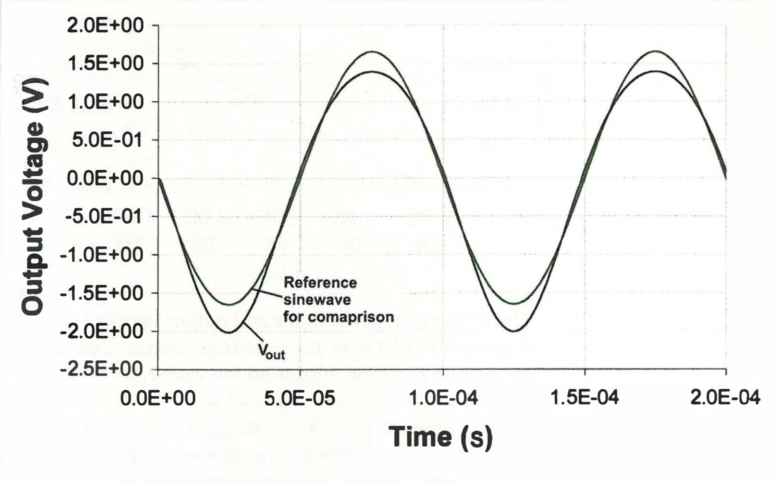


Fig. 7. Transient analysis of the one-transistor circuit. Note that the output signal is asymmetrical with about 20% distortion.

$$\begin{bmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{bmatrix} = \begin{bmatrix} l_{11} & 0 & 0 \\ l_{21} & l_{22} & 0 \\ l_{31} & l_{32} & l_{33} \end{bmatrix} x \begin{bmatrix} 1 & u_{12} & u_{13} \\ 0 & 1 & u_{23} \\ 0 & 0 & 1 \end{bmatrix} \tag{33}$$

Starting with l_{11} the sum of the multiplication of the first row of **L** with the first column of **U** gives $l_{11}=m_{11}$. Multiplying the first row of **L** with the second column of **U** gives $m_{12}=l_{11}.u_{12}$ or $u_{12}=m_{12}/l_{11}$. Similarly, u_{13} is calculated, and in general, for each row i, each element of **L** is calculated from l_{i1} to l_{ii}, then the rest of the 'u's are calculated from the ls on that row. Both **L** and **U** can be stored in one additional matrix the size of **M**, because the diagonal of **U** is known and therefore does not have to be stored.

The forward and backward eliminations follow a similar procedure but operating with **L** to obtain **z** from **y**, starting with the lowest number x_1, then on **U** and **z** to obtain **x**, starting with x_{max} and working backwards to give x_1.

This procedure is very easily adapted to a computer program, and is more straightforward than the classical inversion procedure. However, it involves about the same number of calculations.

This number increases rapidly with matrix size. For three unknowns the matrix is three-by-three; for six it is six-by-six. For each additional line, a set of calculations, or product terms, has to be determined that is of the same number as the order of the matrix. The total number of calculations therefore is roughly increasing as the cube of the number of unknowns.

For small problems, there is no difficulty in performing the complete decomposition. For large problems though, it is clear that the number of calculations may be prohibitive, as well as needing an M-array of the order of n^2 where n is the number of unknowns.

Thus for sparse arrays, the decomposition is limited only to those values where there is a non-zero entry in the M-array. This is not accurate, but successive iterations can be employed to reduce the error.

Even with iteration a limited decomposition is faster for large arrays than the full decomposition. As a guide to the effect of incomplete decomposition, in the limit the "L" array equates to the M-array, as is, while the 'U' array becomes M(i,j)/M(i,i). Hence incomplete decompositions are attractive for large matrices and are more accurate the sparser they are.

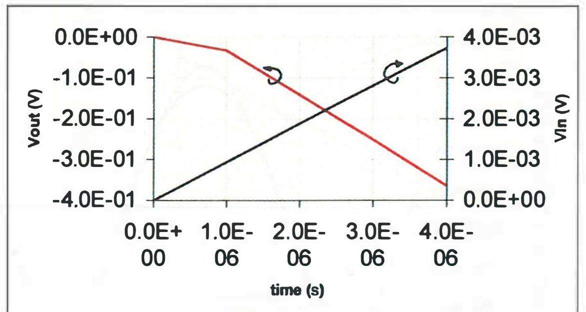


Fig. 8. Comparison of input and output signals. Transient model with 1µs time step. Output should be smooth but time resolution too coarse.

Figure 5 shows a plot of the frequency response for the one-transistor circuit of Fig. 2, as represented by Fig. 3 using the matrix of Fig. 4. It also shows full LU decomposition and a implementation of the SPICE model for the transistor. The gain is relative to the input.

As mentioned, because the equivalent impedances are fixed, there is no knowledge of distortion – small-signal means linear here – and the input voltage magnitude is irrelevant, within reason.

Points to note are that the low frequency gain roll-off begins at around 100Hz using an emitter decoupling capacitor of 220μF. It rolls off at a value of 18dB/octave – well in the 'unstable' region except that two time constants are external to the transistor – C_{in} and C_{out} – and would not cause a problem for feedback around the transistor only.

Neither of these time constants – the input formed from h_{ie}×C_{in} and the output R_{load}×C_{out} – is low enough to account for the 100Hz roll off. The roll off is controlled by something else, yet I have seen one text book state quite categorically that the low-frequency response is controlled by C_{in} and R_2.

In fact, the correct picture is that all time constants will affect the low frequency cut-off, but the shortest time constant will dominate.

Effective emitter-input impedance, or h_{ib}, is roughly V_{th}/I_c, or $25/I_c$ (mΩ). For a BC547, or similar, at 2mA this is 12.5Ω. This rather low value is the critical impedance that sets the time constant in conjunction with the emitter decoupling capacitor – not the emitter resistor R_4, nor the input resistor R_2. In fact the simulation gives a slightly higher value for hib than the nominal 12.5Ω.

For a low-impedance signal voltage, the upper cut-off frequency is around 10MHz. But if you were to use the transistor in an amplifier stage, you may find in practice that it has a much more limited open-loop bandwidth.

Because of the capacitance between the collector and base, a small input resistance will significantly alter the characteristics. The second curve shows the gain for the same amplifier but with a 1kΩ resistor in series with the input. The effect is quite remarkable, but is only the well-known Miller effect, shown in practice.

Given that volume controls of about 10kΩ are often used in real circuits, the open-loop performance could be changing dramatically with volume setting. With negative feedback this effect will be minimal, but could explain sensitivities in some designs that do not consider this, or in distortion figures that depend on the open-loop to closed-loop gain difference to reduce distortion.

Small-signal circuits are useful as checks to see whether there are peaks or dips in the frequency-response curve, or how fast a response may be tailing off at high or low frequencies, as this is a guide to potential instability. For a quantitative assessment of an amplifier's characteristics, a time-stepped solution is necessary.

Transient model

The circuit for a transient simulation is essentially the same as in Fig. 3, but with the ordinary SPICE model replacing the small-signal equivalent. The transient model preserves the operating voltages, and works on a time-stepped approach using the differential form of the capacitor equations.

A simple test is to consider an *RC* network again. Assume that a capacitor *C* is initially uncharged, and at time t_0 a voltage step is applied. The network has one unknown node – the junction between the resistor and capacitor. For each node – in this case just the one unknown – the various nodal elements of current are summed to zero.

The potentials are taken again where positive means "from there to here". Thus, in the case of the resistor, the current from the point of view from node 1

$$i_r = \frac{V_{gnd} - V_1}{R} \tag{1A}$$

but V_{gnd}=0. Whereas the capacitor current

$$i_c = -C.\frac{d(V_{in} - V_1)}{dt}$$

The node currents then sum to zero:

$$i_r + i_c = 0 \tag{34}$$

and the instantaneous capacitor current i_c is written in terms of current voltage and previous charge thus:

$$i_c = C\frac{(V_{in} - V_1)}{dt} - \frac{Q_{t-1}}{dt} \tag{35}$$

For this illustration, if a step function defined by V_{in}=0 up to t=t_0, then for t>t_0, V_{in}=2V is applied – the response for a 1kΩ resistor and 0.1μF capacitor is the exponential one would expect to see (Fig. 6).

The one limitation is that while time steps can be made short, this approach cannot resolve an 'infinitely short' step. This means that the output does not quite reach the peak input that would have been seen had the step been infinitely fast. However, the transient model does not 'know' about any voltages between the input time steps, and assumes a linear interpolation.

Considering the one-transistor circuit described earlier, the simulation requires the standard equivalent circuit instead of the small-signal circuit. Otherwise the circuit is the same.

Instead of using impedances for each capacitor, the differential version and previously stored charges are used. For node 1, for example, the currents feeding into it arise from the input via C_{in}, the bias resistors R_1 and R_2, the collector-to-base external resistance c_{bcx} and the base resistance r_{bb}, totalling five. The nodal equation becomes:

```
-(1.0/r1+1.0/r2+cin/dt+1.0/rbb+cbcx/dt)
.V1+1/rbb.V2+cbcx/dt.V5
=-vcc/r1-cin*vin/dt+qcin/dt+qcbcx/dt            (36)
```

Note that in general the impedance of a capacitor has been replaced with *C*/d*t*, and this time the current from a fixed v_{cc} in R_1 is required. The previous charges on the capacitor are now on the right to allow accurate calculation of d*Q*/d*t* written as *C*.d*V*/d*t*.

Capacitor charges are initially set to that of the DC bias conditions. After each time step, the new charge can be determined simply from the capacitance and terminal voltages rather than calculating from the change in current: this has to be multiplied by d*t*, having just divided by it, so the standard *Q*=*CV* is rather easier and more efficient.

When the set of equations is written out, some capacitor charges appear on more than one node. The charge will have been set in the direction 'there' to 'here' the first time a capacitor is encountered, and the charge from the previous iteration, subtracted on the left, is added on the right side of the equation to give a positive quantity.

The same charge applies to the node that was 'there' when that node is considered, but as the original node is now 'there' and the 'there' now 'here', the sign has changed.

For example, qcbcx is the charge on cbcx between nodes 1 and 5. When considering node 1, qcbcx is subtracted from node 1, but to use the same charge for node 5 requires a sign change.

For each node, if a capacitor is attached to that node and is seen for the first time, write the charge according to the point of view of that node. If, later, we get to the other side and see a capacitor we have seen before, use the charge previously calculated but reverse the sign.

The transient solution does not require complex numbers. Each variable is an ordinary real or floating point number. There is no strong language preference for solving this model.

To solve the transient response of the circuit, the DC operating point is again established. Then a pre-defined signal is applied to the input, and the output voltage is calculated. The solution for each time-step uses a relaxation approach as outlined for the DC case.

First, the matrix is solved for the given transistor characteristics – using primarily gain – which leads to a bias voltage on the transistor. The SPICE or other bipolar model equations are solved, returning currents, gains and capacitances which are used to prepare a new matrix set of constants.

Next, the sequence is iterated, alternately solving the matrix, then the SPICE model, updating the input parameters to each between each call. For signals that do not cause abrupt non-linearities – such as the transistor entering the saturation region – this approach is stable for smallish time steps. A resolution of 1μV is sufficient to determine convergence.

This relatively simple relaxation algorithm, iterating between the circuit matrix and the SPICE model, is not particularly robust under adverse conditions. If the matrix – or circuit – solution indicates that the transistor current should increase, yet the SPICE model shows that the transistor saturates and the gain collapses, the collector current should not increase, the subsequent circuit simulation will try to increase the collector voltage, leading to an unstable loop.

One partial solution to this difficulty is to reduce the time steps. This means that at the start of each loop, the previous successful solution is saved. If difficulties are encountered, indicated by a diverging voltage particularly on the collector, or a numerical overflow, the whole time step has to start again using the previous solution with a smaller time increment, until a solution is found.

Another approach is to use a more robust algorithm that calculates the differentials, and use these in a Newton type solution to try to achieve a more stable formulation. This approach, or in general, any more robust algorithm, will increase the coupling between the two models rather than leaving them entirely separate.

A crude fall-back solution that is not elegant is to perform a binary search on one model to force the result. This may work but would take more iterations than strictly necessary.

Finally, discrete time-stepping in this manner is a digital characterisation of an analogue system. Just like audio digitisation, there is no information regarding the output waveform between time steps, which is usually 'filled in' by a straight line. Therefore to assess a distortion figure, the time steps will have to be small enough that the digitisation errors do not contribute to the distortion figures requiring to be analysed.

In effect, this amounts to something like 1μs at the most. This is well below the CD digitisation frequency of 44kHz, but may still be too large to resolve high-frequency harmonics.

The result of applying a 20mV, 10kHz, sinewave signal to the transistor circuit of Fig. 2 using transient analysis is shown in **Fig. 7**. For reference, a sinewave has been included. You can see that the upper part of the output waveform is flattened (peak 1.4V), while the lower part of the waveform is peaked (trough –2V). Distortion levels of this are in the region of 20%.

The absolute values are more of a guide than the apparent shape of the waveform – it does seem that the eye is not a good judge of a waveform. The transient analysis will provide the time delay of the circuit. An enlarged scale of the initial part of the wave is shown in **Fig. 8**. This indicates that there is about 1μs at the most. This is well below the CD digitisation frequency of 44kHz, but may still be too large to resolve high frequency harmonics.

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The transient analysis provides the time delay of the circuit. An enlarged scale of the initial part of the wave is shown in Fig. 8. This indicates that there is about 1μs delay between the start of the input signal and the point where the output begins to follow it. (being an inverting stage of course the output is opposite to the input.) This occurs in one time step for the simulation, and is not resolved particularly well. A smaller time increment is really needed.

The use of these simulations becomes apparent when considering circuits with more transistors. I have used these approaches to investigate the use of the Miller capacitor in amplifier circuits compared with alternative stabilisation schemes.

The two-pole roll-off method discussed by Self[1] is particularly interesting and seems to have the capability of providing a high performance but is not without difficulties. The method used by Bailey[2] and Linsley-Hood[3] where the compensation capacitor is connected around both input and VAS stages is a possible alternative to the 'Miller' capacitor: it has some advantages but certainly is not as stable and will be discussed in a subsequent article. ■

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2. A. R. Bailey, "High Performance 30W Amplifier", *Wireless World*, May 1968
3. J. Linsley-Hood, "70W Audio Amplifier", *HiFi News and Record Review*, November 1972.

All you ever wanted to know about Bluetooth

The concept of a wireless society where different peripherals seamlessly connect together may appear to be a rose tinted view of the future, but this is what the aim of Bluetooth was when it was first conceived. Ian Poole tries to relieve 'Bluetoothache'

Today there are many Bluetooth devices on the market, and to some it is a real advantage, whilst others refer to it as Bluetoothache. Whatever one's view the technology is here to stay, with many mobile phones and other devices using it.

The technology traces its origins back to a concept that came out of Ericsson in 1994. The original intention was to make a wireless connection between something like an earphone and a cordless headset and the mobile phone. However the idea developed as the possibilities of interconnections with a variety of other peripherals such as computers, printers, phones and more were realised. Using this technology, the possibility of quick and easy connections between electronic devices should be possible.

In order that the technology could move forward and be accepted as an industry standard, Ericsson opened the technology up. As a result of this, in February 1998, five companies (Ericsson, Nokia, IBM, Toshiba and Intel) formed a Special Interest Group (SIG) to further advance the work that Ericsson had begun, hoping to develop an industry standard. The group consisted of market leaders in the fields of telephony and computing – the two main areas they wished to address. Then in May 1998, Bluetooth was publicly announced with the first specification following on with the first release of the standard in July 1999. Later more members were added to the group with four new companies, Motorola, Microsoft, Lucent and 3Com, joining the group. Since then more companies have joined and the specification has grown and is now used in a large variety of products.

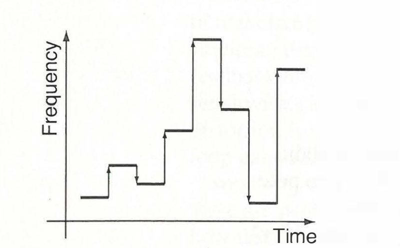

Fig. 1. Frequency hopping.

The name of the standard originates from the Danish king named Harald Blåtand who was king of Denmark between 940 and 981 AD. His name translates to be "Blue Tooth" and this was used as his nickname. A brave warrior, his main achievement was that of uniting Denmark under the banner of Christianity, and then joining it with Norway that he had conquered. The Bluetooth standard was named after him because it endeavours to unite personal computing and telecommunications devices.

Basic capabilities

Bluetooth is primarily a wireless data system and can carry data at speeds of up to 721 Kbps but it also offers up to three voice channels. The technology enables a user to replace cables between devices such as printers, fax machines, desktop computers and peripherals and a host of other digital devices. Furthermore, it can provide a connection between an ad hoc wireless network and existing wired data networks.

The technology is intended to be placed in a low cost module that can be easily incorporated into electronics devices of all sorts. It uses the licence free Industrial, Scientific and Medical (ISM) band and enables communications to be established between devices up to a maximum distance of 100 metres.

RF system

The system uses a low power frequency-hopping carrier that is modulated using Gaussian Frequency Shift Keying (GFSK).

With a hopping transmission, the carrier only remains on a given frequency for a short time and if any interference is present the data will be re-sent later, but on a different channel that is likely to be clear of other interfering signals. The standard uses a hopping rate of 1600 hops per second. These hops are spread over 79 fixed frequencies that are chosen in a pseudo-random sequence. The fixed frequencies occur at 2400 + n MHz where the value of n varies from 1 to 79. This gives frequencies of 2402, 2404 ….. 2480MHz. In some countries the ISM band allocation does not allow the full range of frequencies to be used. In France, Japan and Spain, the hop sequence has to be restricted to only 23 frequencies because the ISM band allocation is smaller.

The frequency hopping system was used rather than a direct sequence spread spectrum approach because it is able to operate over a greater dynamic range. If direct sequence spread spectrum techniques were used then other transmitters nearer to the receiver would block the required transmission if it is further away and weaker.

The way in which the data is modulated onto the carrier was also carefully chosen. As I mentioned earlier, a form of frequency shift keying known as Gaussian Frequency Shift Keying is employed. Here the frequency of the carrier is shifted to carry the modulation. A binary one is represented by a positive frequency deviation and a binary zero is represented by a negative frequency deviation. It is then filtered using a filter with a Gaussian response curve to ensure the sidebands do not extend too far either side of the main carrier. By doing this it achieves a bandwidth of 1MHz with stringent filter requirements to prevent interference on other channels. For correct operation the level of BT is set to 0.5 and the modulation index must be between 0.28 and 0.35.

The transmitter powers for Bluetooth are quite low, although there are three different classes of output dependent upon the anticipated use and the range required. Power Class 1 is designed for long range communications up to about 100m, and this has a maximum output power of 20dBm. Next is Power Class 2 which is used for what are termed ordinary range devices with a range up to about 10m, with a maximum output power of 4dBm. Finally there is Power Class 3 for short-range devices. This supports communication only to about 10cm and it has a maximum output power of 0dBm.

There are also some frequency accuracy requirements. The transmitted initial centre frequency must be within ±75kHz from the receiver centre frequency. The initial frequency accuracy is defined as being the frequency accuracy before any information is transmitted and as such any frequency drift requirement is not included.

In order to enable effective communications to take place in an environment where a number of devices may receive the signal, each device has its own identifier. This is provided by having a 48-bit hard-wired address identity giving a total of 2.815 x 10^{14} unique identifiers, which should be quite sufficient!

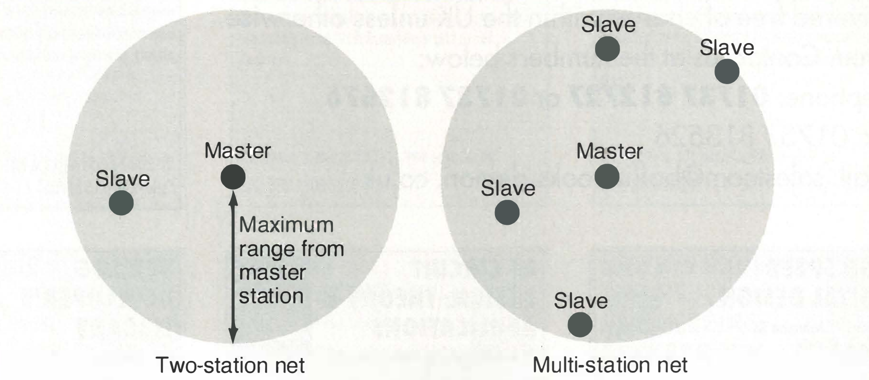

Fig. 2. Bluetooth nets.

Links

There are two main types of link used for data transfer. The first is the Asynchronous Connectionless Communications Link (ACL) and this is used for file and data transfers. A second form of link known as a Synchronous Connection-orientated Communications Link (SCL) is used for applications such as digital audio.

The asynchronous link supports a maximum data rate of 732.2 kbits/sec in an asymmetric mode, whereas in a symmetrical mode running the same data rate in both directions this rate is reduced to 433.9kbits/sec. The synchronous links support two bi-directional connections at a rate of 64kbits/sec. The data rates are adequate for audio and most file transfers. However the available data rate is insufficient for applications such as high rate DVDs that require 9.8Mbit/sec or for many other video applications including games spectacles.

Data is organised into packets to be sent across the link. The Bluetooth specification lists seventeen different formats that can be used dependent upon the requirements. They have options for elements such as forward error correction data and the like. However the standard packet consists of a 72-bit access code field, a 54-bit header field and then the data to be transmitted, which may be between 0 and 2745 bits. This data includes the 16-bit CRC if it is needed.

As it is likely that interference will cause errors, error handling is incorporated within the system. For asynchronous links, packet sequence numbers are transmitted. If an error is detected in a packet then the receiver can request it to be re-sent. Error coding using a 16-bit CRC is also available. For the synchronous links packets cannot be re-sent as there is unlikely to be sufficient bandwidth available to re-send data and 'catch up'. However it is possible to include some forward error control.

Nets

To communicate between different Bluetooth devices, they form small nets called 'piconets'. These comprise up to eight devices, of which one takes on the role of a master whilst all the others become slaves. If more than eight devices are within range, then they may remain in an inactive standby state and may be requested at a later time to join the net. Still further devices may be in a standby state.

When establishing a net, the master transmits an enquiry message every 1.28 seconds to discover whether there are any other devices within range. If replies are received then an invitation to join the net is transmitted to specific devices that might be in range. To set up the net the master allocates each device a member address and it then controls their transmissions.

All Bluetooth devices have a clock that runs at twice the hopping speed and this provides synchronisation to the whole net. The master transmits in the even numbered time slots whilst the slaves transmit in the odd numbered slots once they have been given permission to transmit.

As security is becoming an important issue, especially where links to computers are concerned, secure communications are possible over Bluetooth with the devices encrypting the data transmitted. A key up to 128 bits is used and it is claimed that the level of security provided is sufficient for financial transactions. However in some countries the length of the key is limited to enable the security agencies to gain access if required.

Summary

Recent reports indicate that Bluetooth is now well established in the market place. It is estimated that over 70 million items equipped with Bluetooth will be shipped this year. Next year this figure is expected to rise considerably as the technology becomes further embedded in today's systems and recognised as a standard means of communication.

This is a far cry from the early days of Bluetooth when, for example in 2001, only 10 million items were shipped. In fact the early days of Bluetooth saw relatively low levels of uptake. One of the major factors causing this was the interoperability problems that were encountered when setting up communications between devices made by different manufacturers. These are said to be something of the past now, although many Bluetooth users may choose to disagree. Nevertheless as the number of applications and the number of users increase the technology should mature still further and improvements in the way the different units inter-operate should improve.

For the future it is anticipated that the use of Bluetooth will grow, this growth fuelled not only by increasing the market penetration, but also by the new applications that will be discovered. The fact that there are no clear competitors in the personal sector of the wireless networking market is a clear advantage. Other possible competitors do not have the scope, or the maturity to take any significant element of the market. In view of this, it appears that Bluetooth will become a far more common feature on personal electronic devices from mobile phones to computers and many other devices that are in common use around the home and office.

Further information about radio and wireless technology can be found in Ian Poole's book entitled *Newnes Guide to Radio and Communications Technology* published by Newnes (2003) ISBN 0750656123 priced £16.99. It is available through the Electronics World bookshop (Boffin Books) page 58. ■

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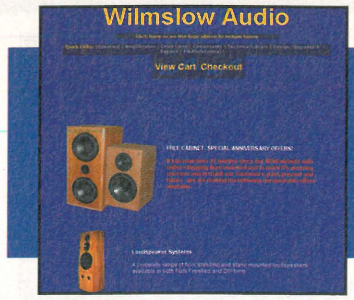

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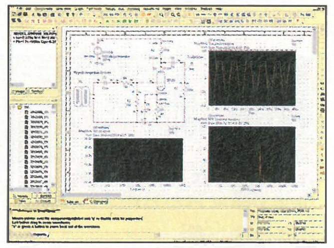

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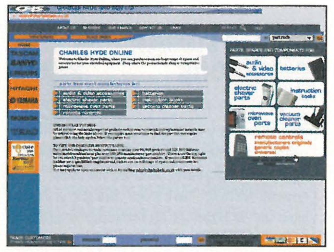

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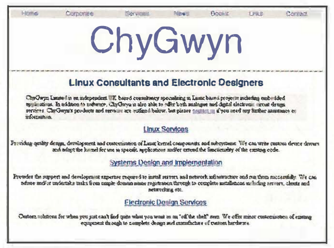

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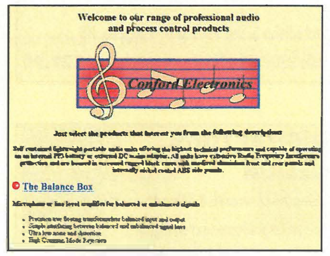

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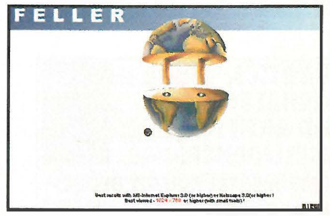

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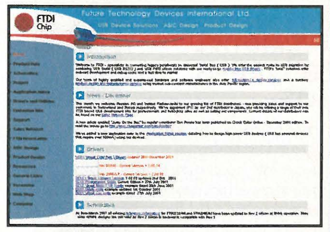

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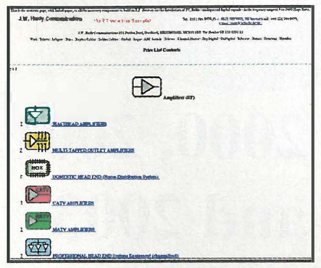

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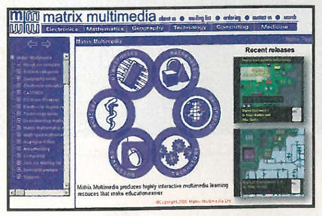

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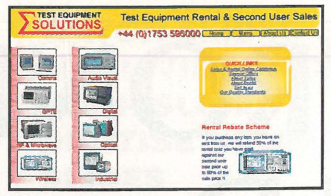

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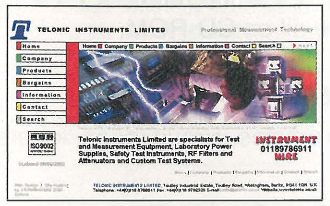

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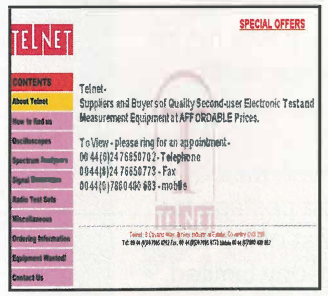

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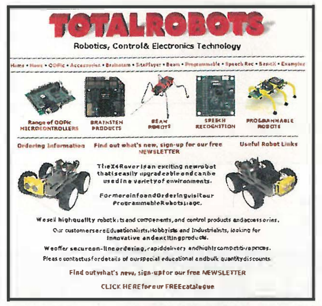

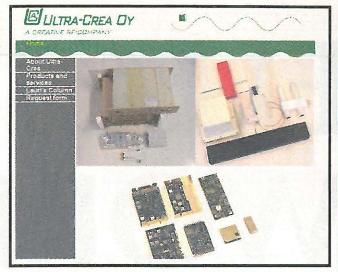

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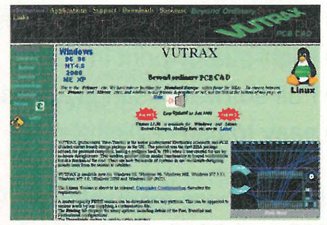

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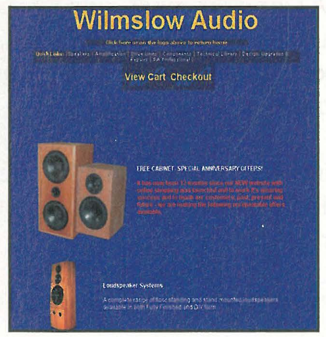

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