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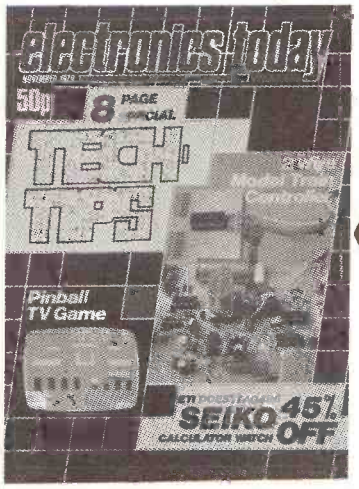

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magazines for enthusiasts, from enthusiasts.

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AUTUMN 1979

Introduction

Since ETI was originally launched in Britain in April 1972 we have published nearly 5000 pages of editorial matter; much of this has been devoted to electronic projects of course. In our history we have republished the best of these projects in Top Projects No 1-No 7, we have also reprinted the Tech-Tips and other circuits in Circuits Book No 1 and No 2 and our beginners series Electronics-It's-Easy is now on its third reprint.

We have not however, until now, brought together the best features dealing with electronic design. Nearly 1500 pages have been devoted to this in recent years and this special is the first of a series of three which will bring together the best 250-300 of these.

Although some features are from quite early issues they have only been included because we feel that 'age has not withered them'.

We hope that the contents help the reader understand at least some of the aspects of electronic circuit design.

Halvor Moorshead
Editorial Director — ETI

Contents

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CMOS

BY T. BAILEY

The availability of the CD4000 series of chips brings CMOS to the forefront of logic technology to rival TTL in many applications. CMOS is far less critical as regards power supplies and possesses high noise immunity as well as capabilities which are not offered by other logic families. In this article we shall give various circuits which illustrate the use of CMOS. Some of the circuitry, of course, is capable of realisation in a number of different logic families, so that, in these cases, we will merely be introducing equivalents of familiar devices. However, some of the applications we give show the revolutionary possibilities of CMOS.

HANDLING AND USE

Firstly we shall deal with the disadvantages of CMOS and get these behind us before we look more closely at some of the virtues. The first point is that these devices are very susceptible to surges of over-voltage from static electricity and unearthed test equipment. When you come to buy any of the ICs we will discuss you should find them with their leads buried in foam. This foam is conductive and protects the device so do not remove it until the IC is to be put in circuit. If you run out of foam for storing devices then stick them into a piece of soft balsa wood. Whatever else you do, you must not keep them in plastic containers or use ordinary plastic foam which may develop a great deal of static. It is in fact a good rule to keep the devices away from all plastics as much as possible including any nylon clothing. It is sensible to use IC sockets for the more expensive devices and also for any chip you may wish to re-use, but if you do solder them solder the V_{DD} pin first, then V_{SS} and then all the others. The reason for this is that the common ranges of CMOS have internal protection devices which operate fully only when the supply lines are connected. While we are on the subject of soldering, check that your iron and any other instruments you may use (meters, oscilloscopes, etc.) are all properly earthed.

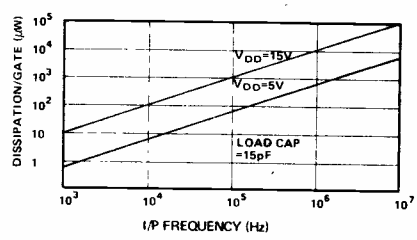
The only other real disadvantages of CMOS compared with TTL are that it is slower (typical gate rise time 25nS) and that a few operating precautions are necessary. Firstly, all unused inputs must go somewhere. The alternatives are tying unused inputs to used inputs, either supply line as appropriate, or to a supply line via a resistor (220kΩ is usually about right). The last solution is particularly helpful for inputs to which off-board connections are to be made. This avoids leaving the input "floating" until it is wired in. The other point is to ensure that the chips do not have signals at their inputs when the power supply is not on.

Now we shall consider a few of the advantages of CMOS. Most of these will come out more clearly later and so we shall just mention them briefly here. The principal virtue is the ease of choice of power supply which may be anywhere between three and fifteen volts at low current. The actual power required depends on operating frequency (see fig. 1) being comparable with TTL at ten megahertz but in the region of a few microwatts at sub-kilohertz speeds. Voltage regulation is not required but operating speed and current consumption rise with increasing supply voltage. For most practical purposes CMOS will run off a nine volt battery or the simplest of mains power supplies. Other advantages include high noise immunity and analogue possibilities. Before we proceed with some circuitry a table of operating conditions (table 1) has been given and these should be adhered to rigidly.

TABLE 1 CMOS OPERATING LIMITS.....CD4000A SERIES

STORAGE TEMPERATURE	−65 to +150°C
OPERATING TEMPERATURE	−40 to + 85°C
SUPPLY VOLTAGE LIMITS ($V_{DD}-V_{SS}$)	−0.5 to +15V
PACKAGE DISSIPATION	200mW max.
INPUT VOLTAGE	$V_{SS} \leq V_{in} \leq V_{DD}$
RECOMMENDED SUPPLY VOLTAGE ($V_{DD}-V_{SS}$)	+3V to +15V

Unused inputs should be tied to a supply line. No input should be present when the supply lines are off.



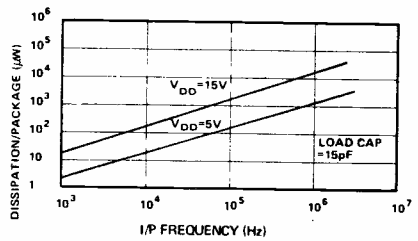


Fig.1. Power dissipation in CMOS as a function of frequency for a) a simple gate and b) an MSJ package.

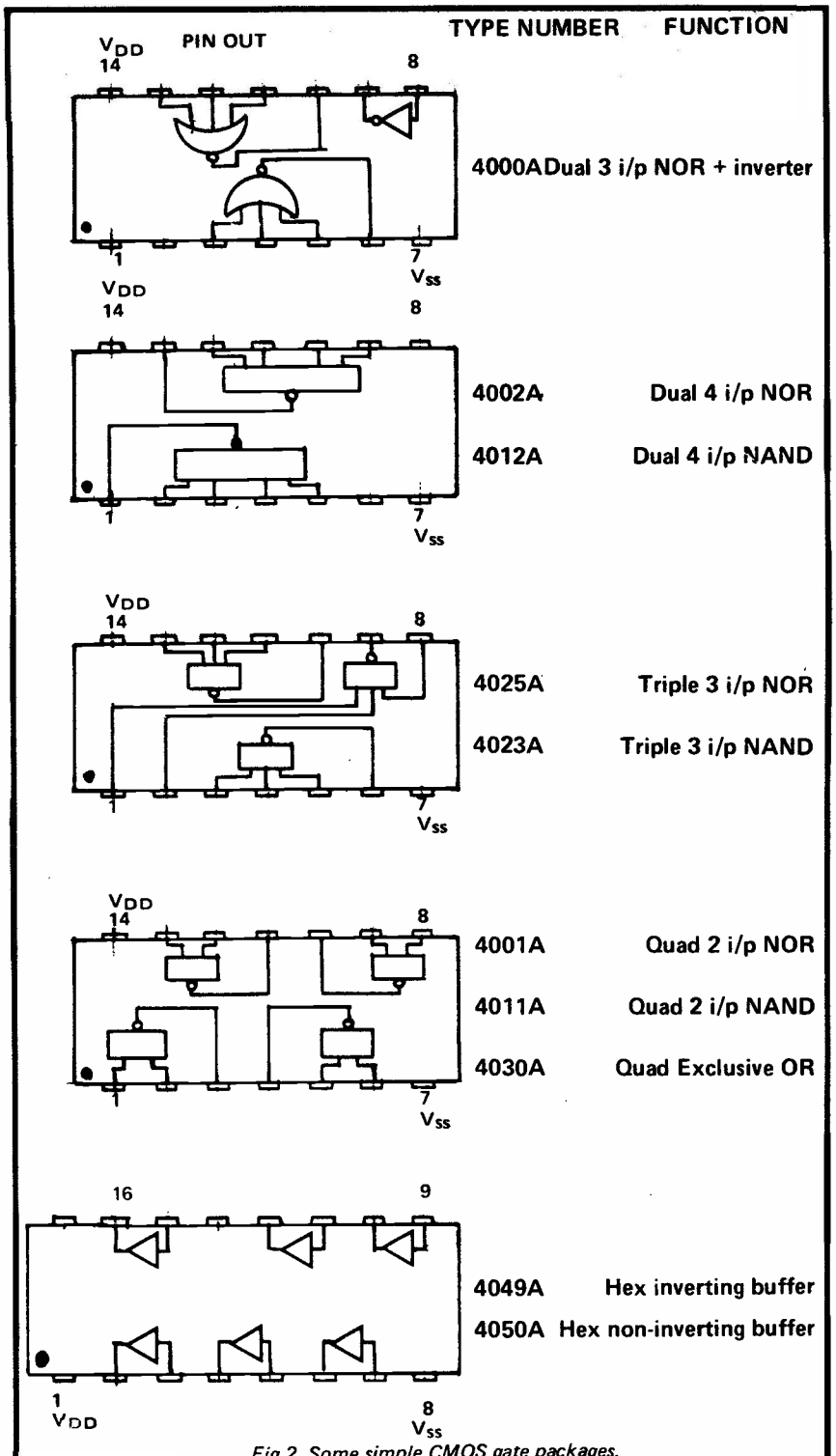


Fig.2. Some simple CMOS gate packages.

SIMPLE GATES

It is an unpleasant fact that it seems one must always start considering any subject at its least interesting parts and it is hardly surprising that the least interesting logic ICs are the simple gates.

We shall assume that the reader is familiar with the truth tables and terminology of the subject and consequently our discussion will mainly be on the subject of monostable and astable multivibrators. For ease of future reference a list of basic CMOS gates and their pin-outs is given in fig. 2. It is worth remembering that inverters may be realised by trying together all the inputs of a NAND or NOR gate, thus allowing a circuit requiring two NOR gates and two inverters to be constructed for a single type 4001A package.

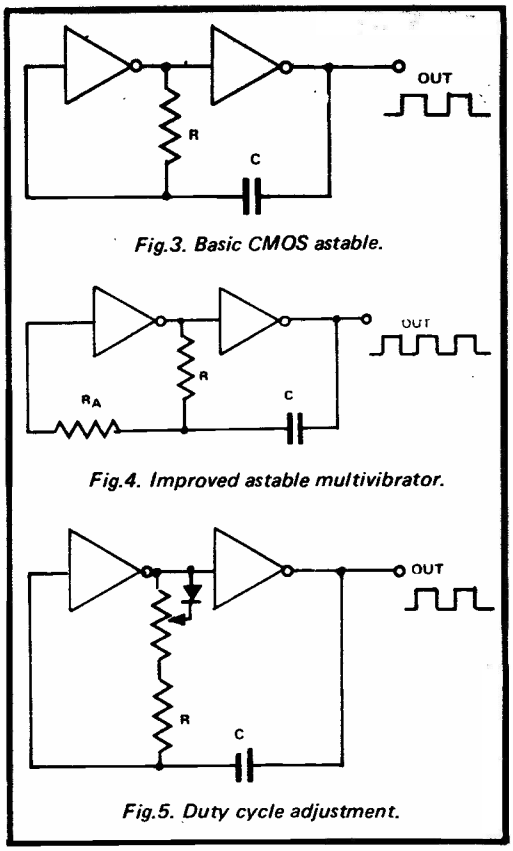


Fig.3. Basic CMOS astable.

Fig.4. Improved astable multivibrator.

Fig.5. Duty cycle adjustment.

ASTABLE MULTIVIBRATORS

The basic CMOS astable is shown in fig. 3. This could of course be built using any of the packages in fig. 2 with the exceptions of the 4030A and 4050A, indeed, the 4049A could produce three of these circuits simultaneously. The period is approximately 1.4RC (R in ohms, C in farads) and the waveform may have a non-unity mark-space ratio due to the voltage at which the inverters switch (called the transfer voltage—V_{tr}) not being exactly half way between V_{DD} and V_{SS}. The frequency is also dependent on the supply voltage. In keeping with normal practice, connections of the device to the supply voltage have not been shown.

The next few circuits will rectify some of the aberrations of the simple version. The addition in fig. 4 of R_A, which should be at least twice as large as R, makes the frequency almost independent of the supply voltage over a wide range. The frequency of any of the circuits may be made variable by making R a variable resistor.

Duty cycle adjustment may be achieved using the circuit in fig. 5. Altering the duty cycle will affect the frequency and the diode may have to be reversed to achieve the desired result.

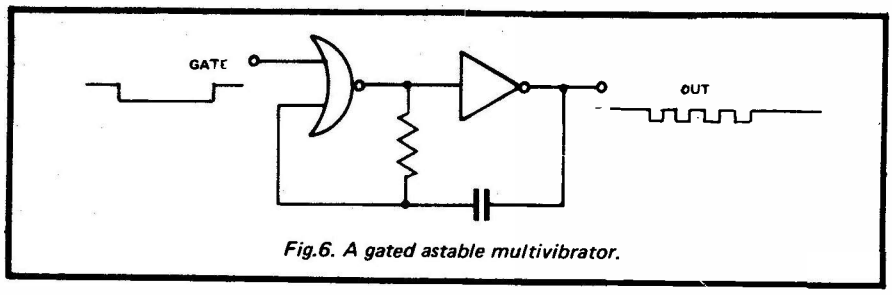


Fig.6. A gated astable multivibrator.

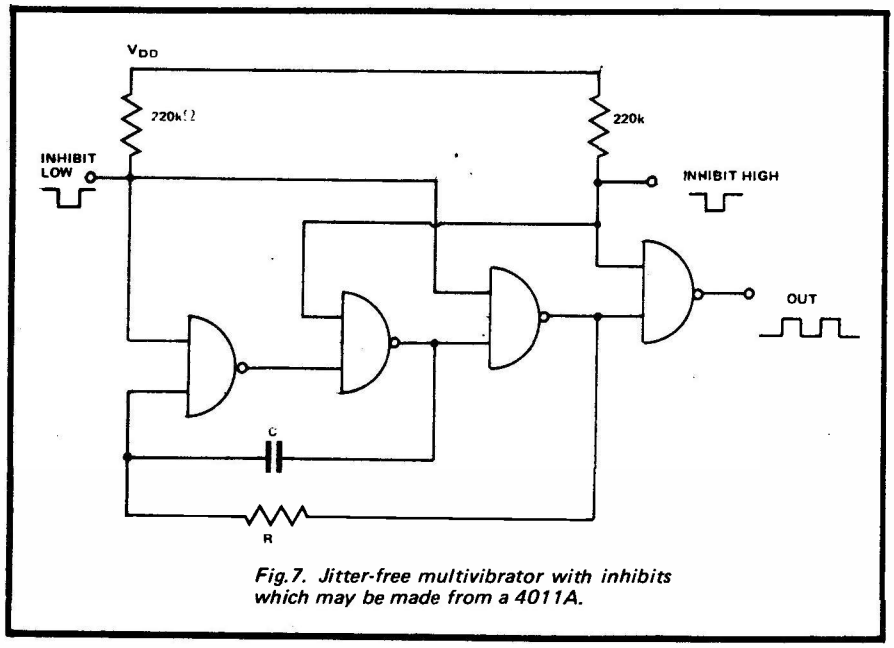


Fig.7. Jitter-free multivibrator with inhibits which may be made from a 4011A.

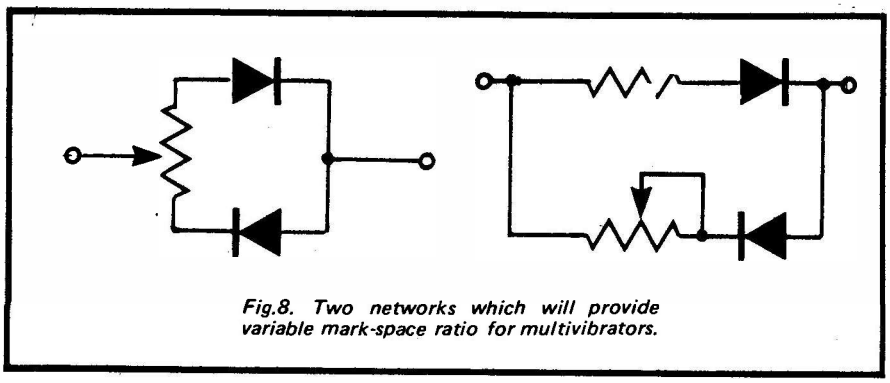


Fig.8. Two networks which will provide variable mark-space ratio for multivibrators.

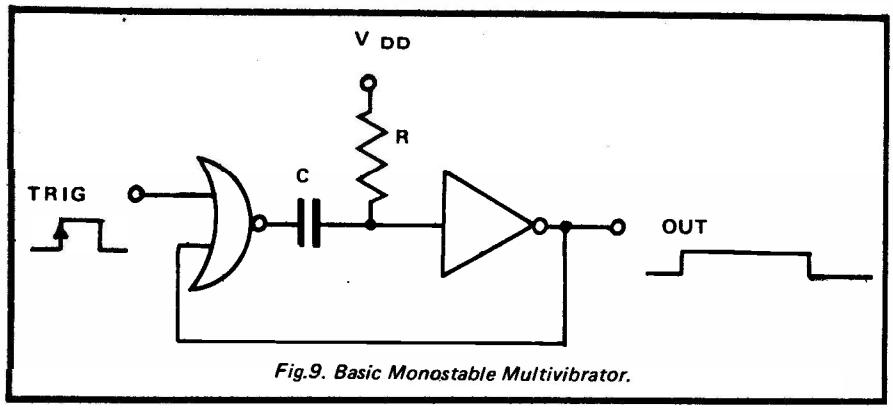


Fig.9. Basic Monostable Multivibrator.

GATING

A gated multivibrator is shown in fig. 6 where the oscillator only runs when the gate input is low, thus producing "bursts" of output in synchronism with the control signal. Using a NAND gate instead of the NOR would cause the circuit to run when the gate was high instead of low.

One of the huge advantages of CMOS is the exceedingly high input impedence. As a consequence of this the timing resistors can be very large and values in the hundred megohm region with capacitors of several microfarads can be a practical proposition.

Before we leave the astable multivibrator for a time we shall give one more circuit which corrects a tendency of all the preceding ones to "jitter" near the switching point. This requires an extra inverter and a fourth has been added as an output buffer. There are also two inhibit inputs which stop the circuit with the output high or low, depending on which is used. The theoretical diagram is shown in fig. 7. Another feature of this circuit, and indeed virtually all the others, is that the timing resistor may be substituted by one of the networks in fig. 8 to give a variable mark-space ratio. They work because the diodes effectively change the value of the timing resistor depending on whether the capacitor is charging or discharging and it is reported that values as large as 5000 : 1 may be achieved.

MONOSTABLE MULTIVIBRATORS

The basic CMOS monostable is shown in fig. 9. It is triggered by the input pulse's leading edge and produces a positive going output pulse. The period may vary by more than ± 50% with different devices due to the dependence of the circuit on the transfer voltage of the inverter.

Once again we shall improve on the basic circuit and also give several alternative versions. The circuit in fig. 10 operates in an interesting way. The quiescent state is with the first and second inverter outputs at "0" and "1" respectively. The falling edge of the triggering pulse makes the first inverter go high, C2 charges through the diode up to V_{DD} and the second inverter goes low thus initiating the output pulse. C1 recharges through R1 and crosses the transfer voltage of the first inverter which consequently goes

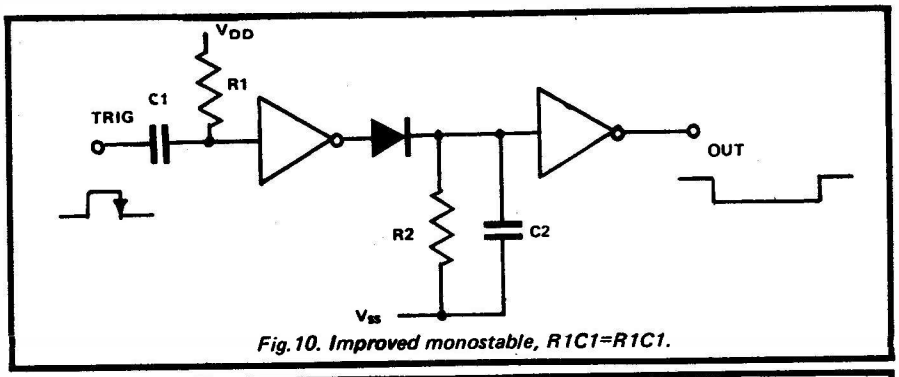


Fig.10. Improved monostable, R1C1=R1C1.

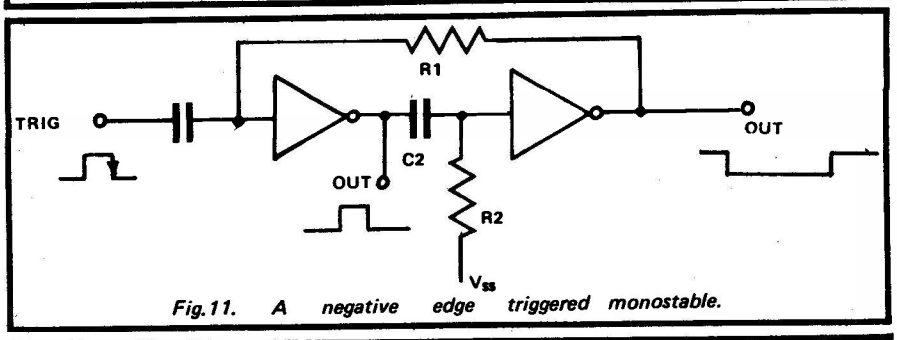


Fig.11. A negative edge triggered monostable.

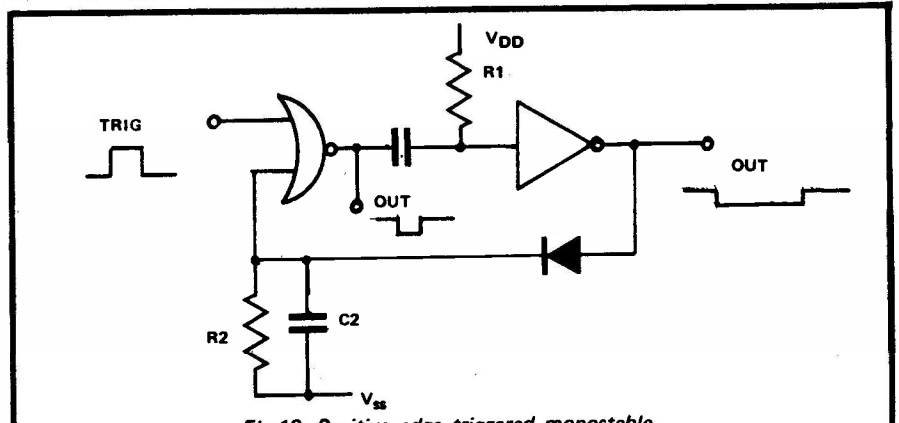


Fig.12. Positive edge triggered monostable.

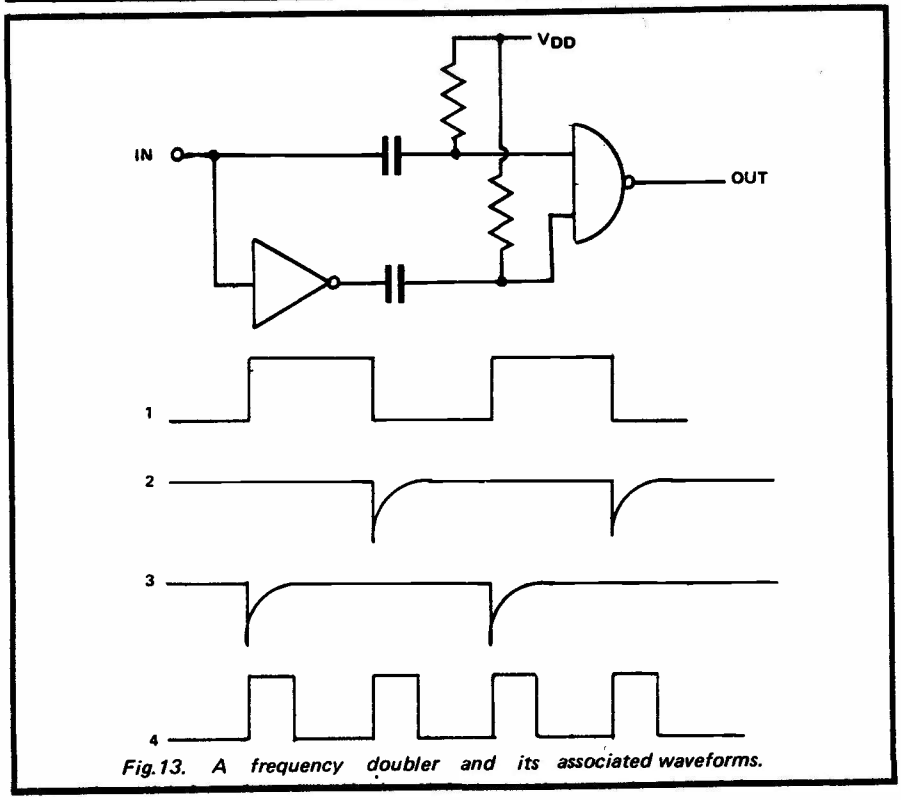


Fig.13. A frequency doubler and its associated waveforms.

low and is isolated from C2 by the now reverse biased diode. C2 then discharges through R2 and causes the second inverter to revert to its initial state thus completing the output pulse. The advantage of all this is that inverters fabricated on the same chip have similar transfer voltages and if the two time constants (R1C1 and R2C2) are made identical, errors cancel out and the period becomes well defined. It is in fact approximately equal to 1.4R1C1 (=1.4R2C2) and this circuit is capable of being retriggered during the output pulse.

Our last two monostables (figs. 11 & 12) are non-retriggerable and the two time constants should be made the same, as in the previous circuit. Fig. 12 is particularly interesting because the circuit isolates the trigger input during the output pulse as the charge on C2 holds one input to the NOR gate high, thus keeping the output low independently of the state of the trigger unput.

FREQUENCY DOUBLER

The frequency doubler shown in fig. 13 works by differentiating the leading and trailing edges of the waveform and applying the resulting pulses to the two inputs of a NAND gate. This produces a complete output pulse at both the rise and fall of the input signal. The values of the discrete components will depend on the desired frequency of operation.

THE 4007

The next device we are going to consider has no equivalent in other logic systems. It is described as a "dual complementary pair plus inverter" and its type number is 4007. It can perform several different functions and while we are discussing it we shall present a number of useful circuits and have the added advantage of learning a little about the internal operation of CMOS.

In CMOS there are two different types of field effect transistors, namely n-channel and p-channel enhancement mode devices (see fig. 14). What all this means is that when biased in the conventional manner (drain positive in n-channel devices but negative in p-channel devices), the n-type turns on when the gate becomes sufficiently positive with respect to the source and the p-type when it is sufficiently negative. A "turned on" device may be considered to have a resistance of the order of 500-1k-

between source and drain whereas the equivalent resistance when "off" is about $10^9\Omega$. The resistance at the gate is always very high ($>10^{12}\Omega$) regardless of the state of the device.

The working of the CMOS inverter (fig. 15) should now be fairly clear. When the input is

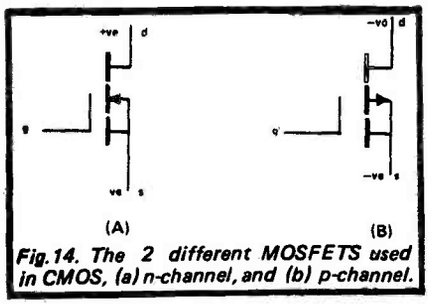


Fig.14. The 2 different MOSFETS used in CMOS, (a) n-channel, and (b) p-channel.

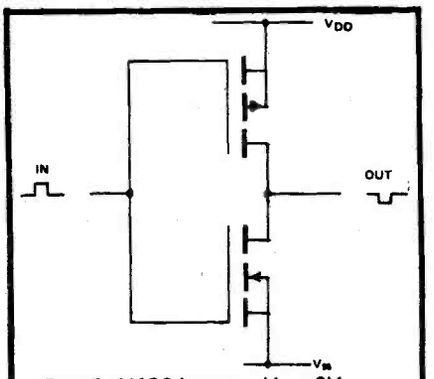


Fig.15. CMOS inverter, V_{SS}=0V, V_{DD}=+3–15V.

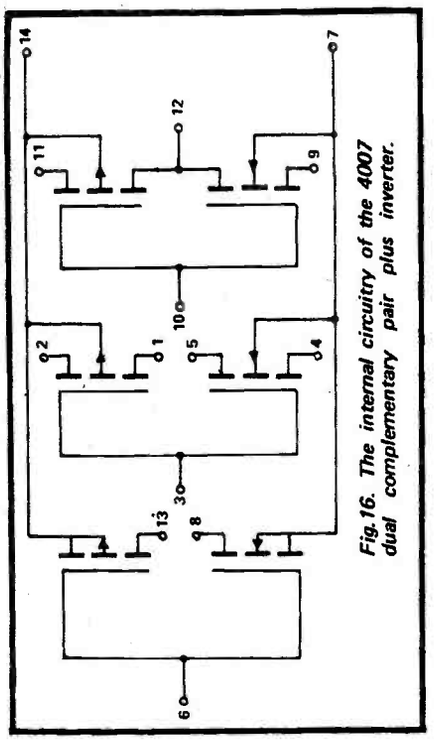


Fig.16. The internal circuitry of the 4007 dual complementary pair plus inverter.

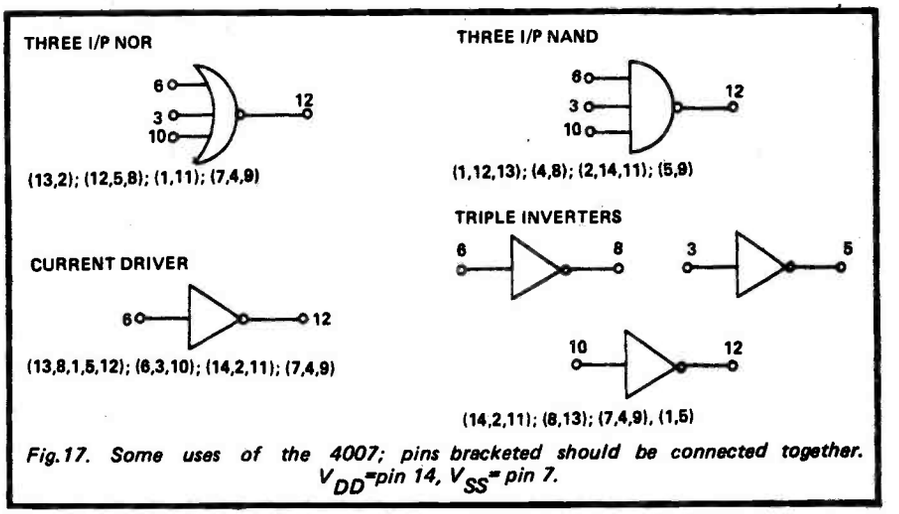


Fig.17. Some uses of the 4007; pins bracketed should be connected together. V_{DD}=pin 14, V_{SS}= pin 7.

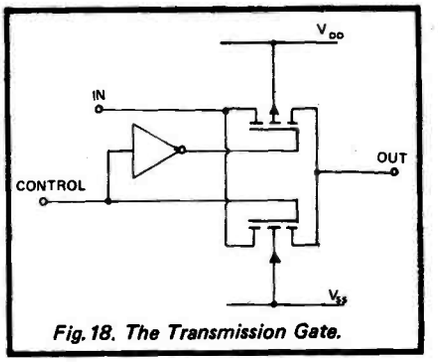


Fig.18. The Transmission Gate.

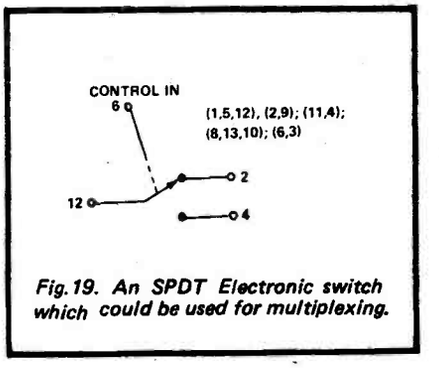


Fig.19. An SPDT Electronic switch which could be used for multiplexing.

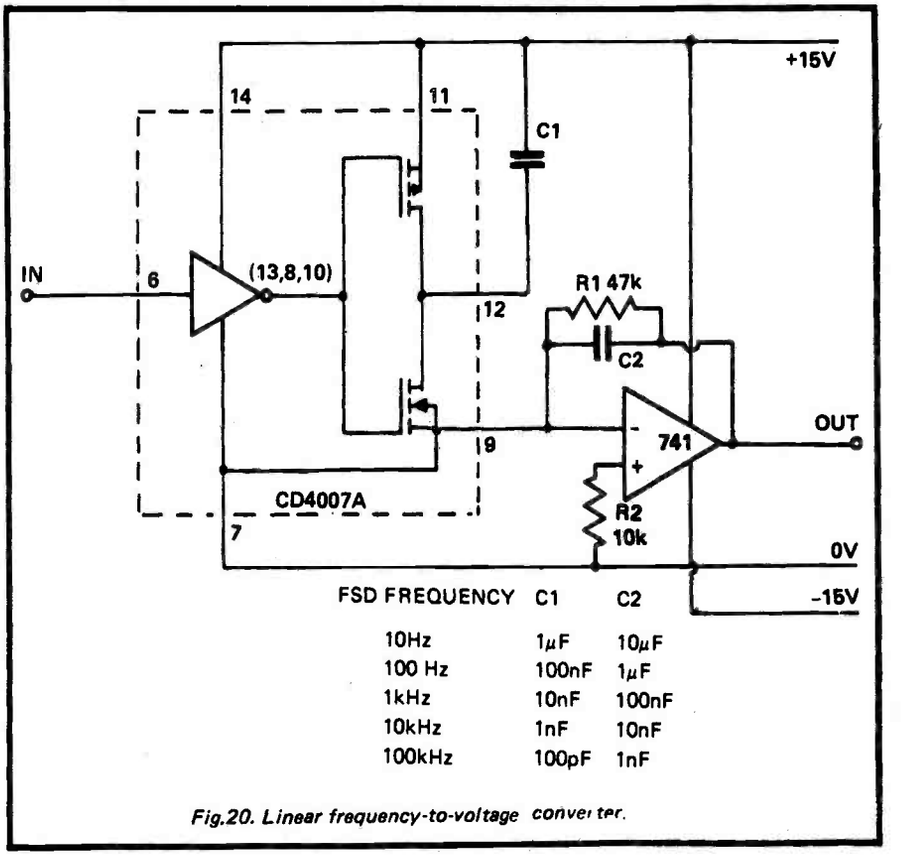


Fig.20. Linear frequency-to-voltage converter.

"high" the bottom FET is turned on and the top one off. Thus the output voltage is held very low. When the input is low the FETs reverse roles and the output is high. Now look at fig. 16 which shows the internal circuitry of the 4007. You should be able to see how joining a few pins together will allow three separate inverters to be produced. Reference to fig. 17 will reveal how several other gates may be produced and their mode of operation should be relatively easy to discern.

TRANSMISSION GATES

There is another way of connecting two FETS which produces a result unique to CMOS. This is the transmission gate (fig. 18). Here, due to the inverter, both FETS are either on or off simultaneously. When they are on, the path between input and output (they are interchangeable) may be regarded as a resistor of about 500-1kΩ whereas when they are off the equivalent value is about 1000MΩ.

Thus the device behaves as a switch capable of passing analogue signals with very little distortion provided that the load resistance is fairly high (≈100kΩ). We shall have more to say about these "bilateral switches" later but while we are dealing with the 4007 fig. 19 shows how to connect one as a single pole-double throw switch which will pass analogue signals in both directions.

Any of the three or less inverter circuits we have mentioned to date may be realised with a 4007, as may several more interesting designs. Fig. 22 shows a linear frequency to voltage converter which works by charging a capacitor up once for every input cycle, the charge to do so being passed by a MOSFET into a summing amplifier. The component values given are based on an approximate five volt output for the given frequency. The resistor R1 should be made a 100kΩ preset if it is required to set a range exactly. The capacitor C2 "smooths" the output and need not be changed from 10μF if fast response on the upper ranges is not needed. The linearity achieved on the top range will depend on the particular "741" used and if reliable operation is required a higher speed op-amp should be used.

Fig. 21 shows an alternative monostable multivibrator. We have already given a number of multivibrator circuits and so we shall say nothing more about this one except

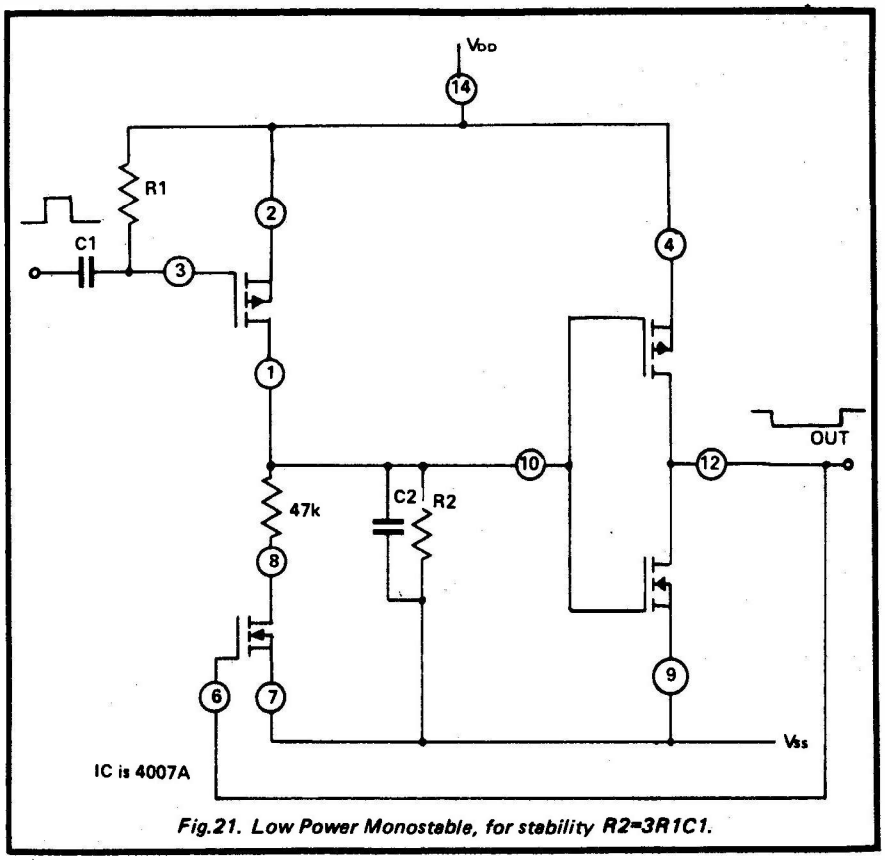


Fig.21. Low Power Monostable, for stability R2=3R1C1.

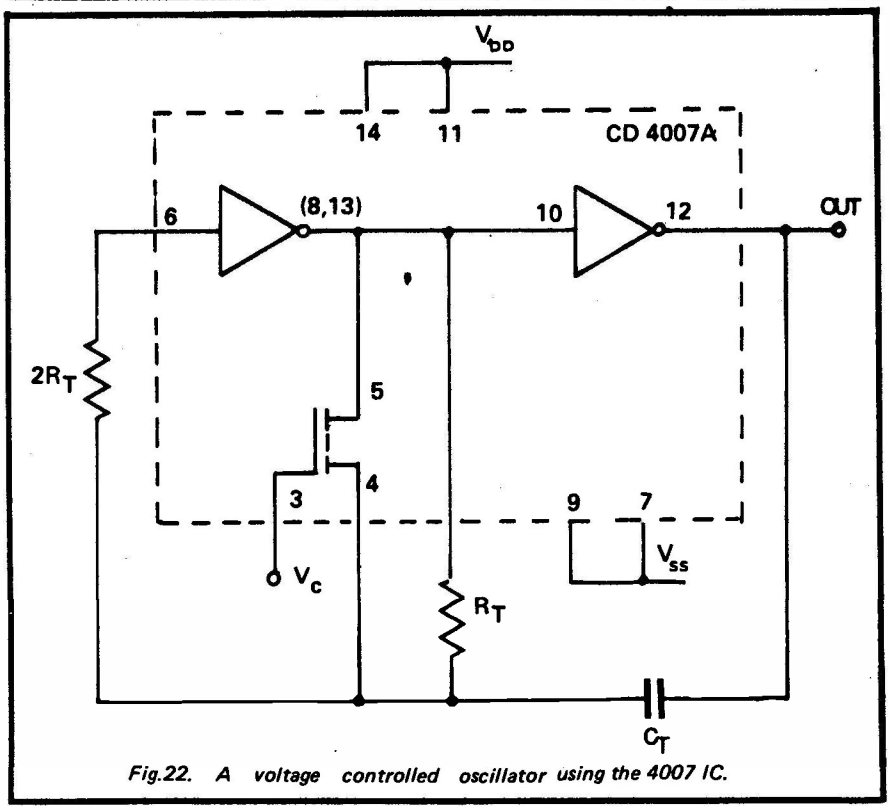


Fig.22. A voltage controlled oscillator using the 4007 IC.

that it has an extremely small power consumption. This is due to the feedback connection (pins 12-6) which turns off the n-channel MOSFET during the discharge of the time constant. This circuit is also an interesting demonstration of the use of components in the 4007 as discrete transistors.

A WIDE RANGE VCO

The voltage controlled oscillator depicted in fig. 24 uses two inverters as well as a separate transistor as a voltage controlled resistor. The inverters function as an astable multivibrator in the manner of Fig. 4 but the timing resistance is the parallel combination of R_T and

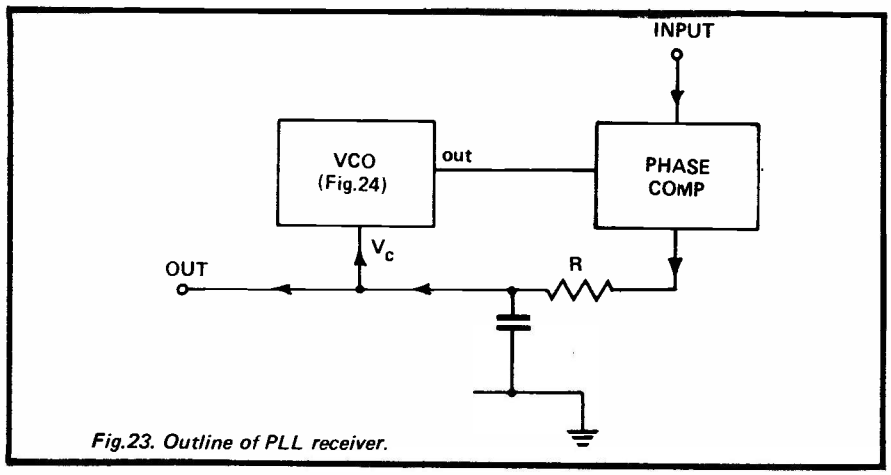


Fig.23. Outline of PLL receiver.

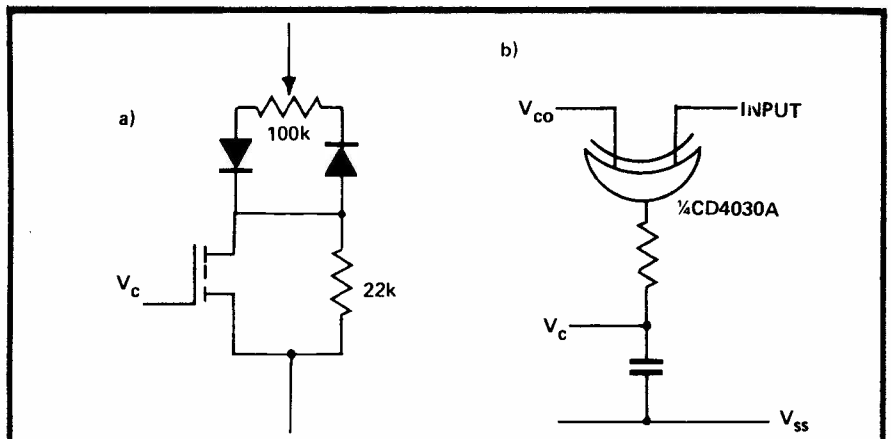
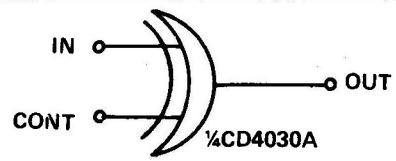


Fig.24. (a) Adjustable M–S ratio narrow range controller, (b) Exclusive–OR phase comparator.

Fig.25. Exclusive–OR gate used as a conditional inverter together with the device's truth table.

IN-1	IN-2	OUT
0	0	0
0	1	1
1	0	1
1	1	0



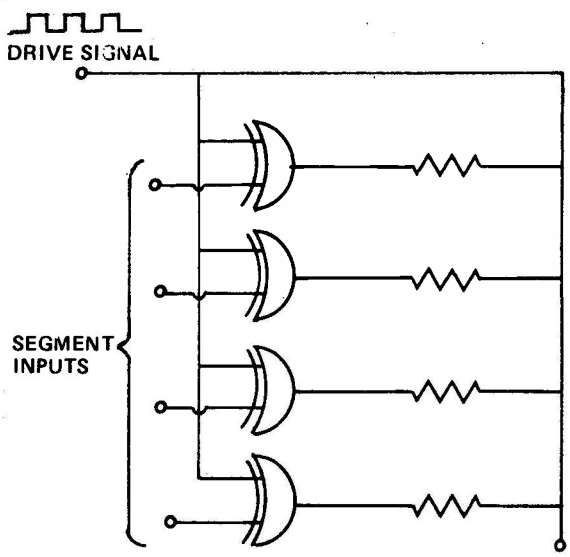


Fig.26. Exclusive–OR gates driving liquid crystal segments, represented by resistors.

the FET. As V_C varies between V_{DD} and V_{SS} so the resistance of the FET varies between about 1k and 1000MΩ. If the upper value is limited to 10MΩ by making R_T that value, then the circuit will sweep over a 10000 : 1 range in frequency. There would seem to be scope here for experimenting with a pulse frequency modulation communications system. One might produce an analogue system although distortion would probably be high due to mismatching. The transmitter could be the circuit in fig. 22 and the receiver a phase locked loop along similar lines (fig. 23) using some sort of phase comparator and a low-pass R-C filter.

EXCLUSIVE-OR GATES

Exclusive-or gates, for example the 4030 (see fig. 2) will function as phase comparators but they require a unity mark-space ratio to be effective. Perhaps a voltage controlled oscillator might be designed with a narrower range along the lines of fig. 24 for both transmitter and receiver, together with a phase comparator and low pass filter as shown in fig. 24. While we are on the subject of the exclusive-or function we shall consider two more uses of these devices. Fig. 25 shows the exclusive-or truth table and its use as a conditional inverter. This configuration causes the input signal to be inverted when the control input is high but not when it is low.

Liquid crystal displays are undoubtedly the readout devices of the future but they last longer in general if an a.c. drive is used. If then a square wave is applied to one end of a liquid crystal segment and also to the other connection via a conditional inverter (see fig. 26) then the control input will decide whether or not there is a net voltage across the segment.

CMOS and liquid crystal make an ideal combination for ultra-low power logic and display systems and so manufacturers have produced BCD to seven segment decoders and drivers specifically for this application. Their type numbers are 4054/5/6, the variations being due to the addition of latches and other refinements. These devices have too limited an appeal to justify a full description here and it is suggested that if it is intended to experiment with this technology, data sheets should be obtained from a manufacturer* or large distributor.

*e.g. RCA, Sunbury-on-Thames, Middlesex, for the "CD4054/5/6A" range. ●

CMOS Part 2

THE 4016A

The next device we are going to look at has already made a considerable impact on amateur electronics. The 4016A quad bilateral switch consists of four transmission gates each with its own control input. Each switch also has a signal input and output (although these are interchangeable). When the control input is held high the input to output path behaves like a pure resistance of about 300Ω but when it is low the equivalent value is of the order of $10^9\,\Omega$ at low supply voltages. It is impossible to give all the data which might be necessary for diverse applications here and data sheets from a manufacturer may be required by the more adventurous experimenters. In any case the pinout diagram in fig. 1 should now be self explanatory.

It should be appreciated that the output impedance of the switch is fairly high and so for low signal distortion, a load greater than 10kΩ is necessary. Using a high supply voltage (10-15V) also helps to achieve this end. The gates will pass signals above the 10MHz mark but as the frequency becomes higher, crosstalk between the switches and distortion will inevitably increase. It should be fairly clear how complicated switching systems may be realised but fig. 2 has been included to guide constructors along the right lines.

ANALOGUE APPLICATIONS

Many uses of this device in audio equipment have appeared in constructional articles in ETI magazine and so it is to two slightly less obvious applications that we shall turn now. Fig. 3 shows a sample and hold unit; when the control input is high the output tracks the input but when it goes low the output remains frozen at the value it was at the instant of transition. The operation of the circuit is generally self evident and it may be regarded as two voltage followers, one consisting of two op-amps with the output following the input, the other is just the second op-amp which "follows" the voltage stored on the capacitor. It is advisable to take care with the layout as with all op-amp circuits due to the huge open loop gain of these devices. The value chosen for C is a compromise between "slewing rate," that is the rate at which the circuit tracks a sudden change of input and "holding ability" which is the length of time the circuit will hold a signal without unreasonable decay. To give some sort of guide, for a 10kHz square wave to the control input, a 0.01μF capacitor seems to optimise the performance. The value of the resistors is also worth experimenting with.

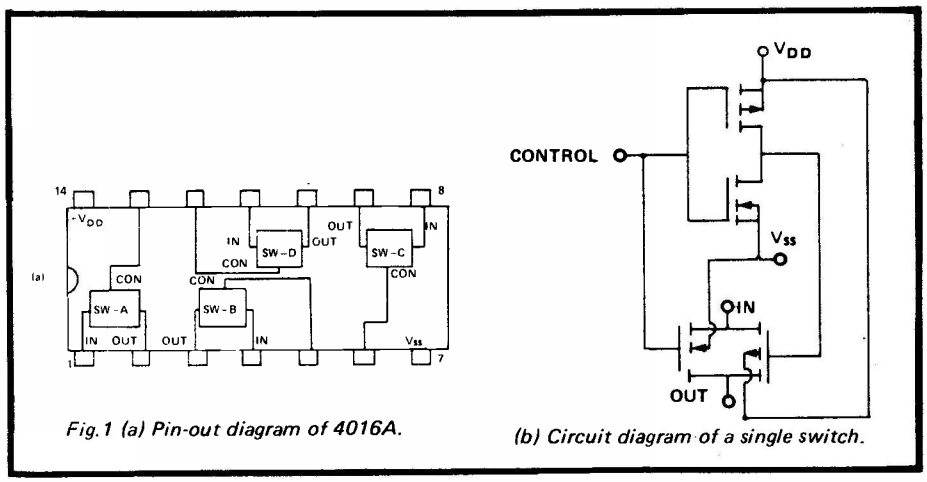


Fig.1 (a) Pin-out diagram of 4016A.

(b) Circuit diagram of a single switch.

An extension of the sample and hold concept is the analogue delay line which is shown in its basic form in fig. 4. The sequence of amplifiers and gates can be extended to any desired length to achieve a longer delay, the only limitation being that in extreme cases the control lines may need to be buffered. It should be observed that alternate stages of the circuit are driven by an identical clock waveform and so the circuit works by shifting the voltage on alternate capacitors during alternate clock phases. The value of the passive components and the clock frequency will have to be optimised for specific applications, low frequencies give long delays but high distortion.

DIGITAL COMPONENT SELECTION

There are a few fairly straight-forward uses of the 4016A in digital component selection which we will mention here because, in certain fields, they are very useful. Fig. 6 shows how to produce digitally controlled resistance and capacitance networks which will vary the magnitude of the quanity in question from its basic value up to 2^n-1 times that amount, where "n" is the number of gates and binary control bits. The resistor network can be used to produce a digitally gain controlled amplifier by placing it in the feedback loop of an op-amp and this can be used as a staircase generator as well as to produce more interesting waveforms. One application of the digital capacitor is to produce a digitally controlled sweep generator by using it as the capacitor in one of the multivibrators we discussed in the last part.

Clearly, any type of component may be switched in and out of circuit by the 4016A. One possibility that is useful in some circumstances is to use the information on filter design in "Electronics — it's easy" to produce digital filters of different descriptions. The main thing to remember when using all these ideas is that the impedance of the component that is being switched must, at the desired frequency of operation, be large compared to the 300Ω of the 4016A gates.

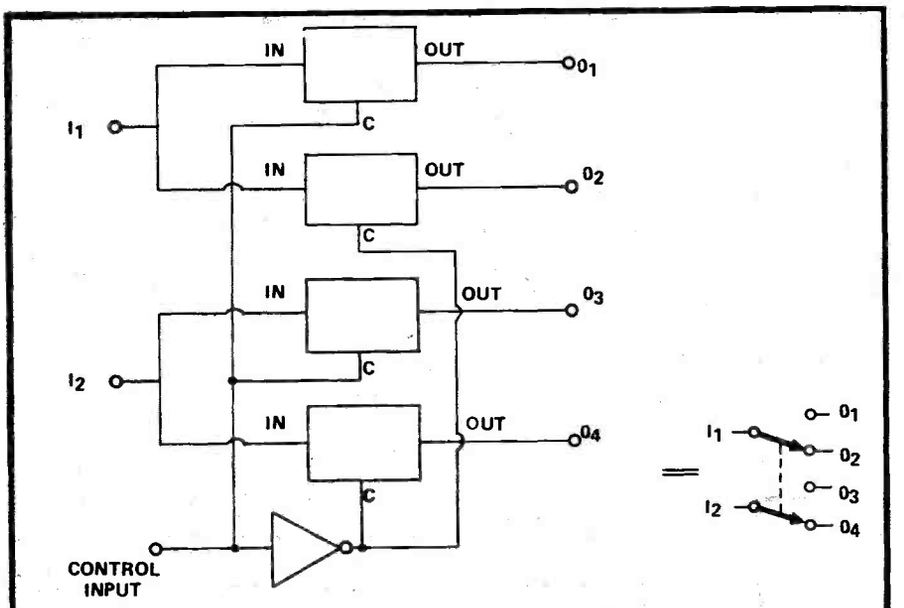


Fig. 2. DPDT electronic switch realised using a single 4016 and an inverter.

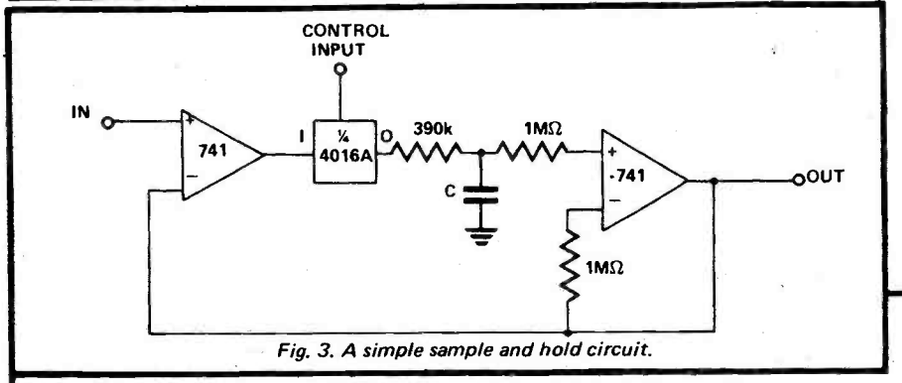


Fig. 3. A simple sample and hold circuit.

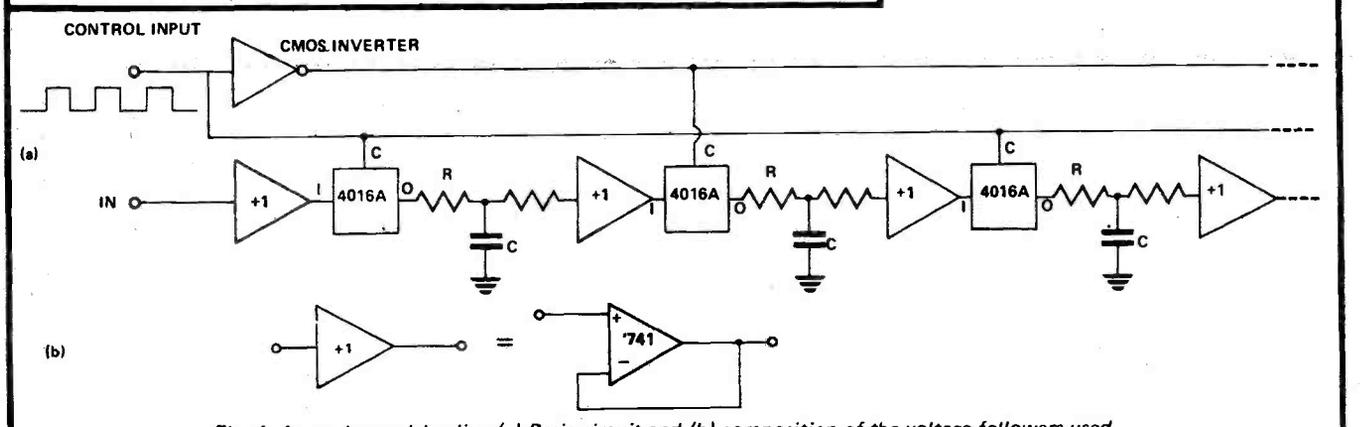


Fig. 4. An analogue delay line (a) Basic circuit and (b) composition of the voltage followers used.

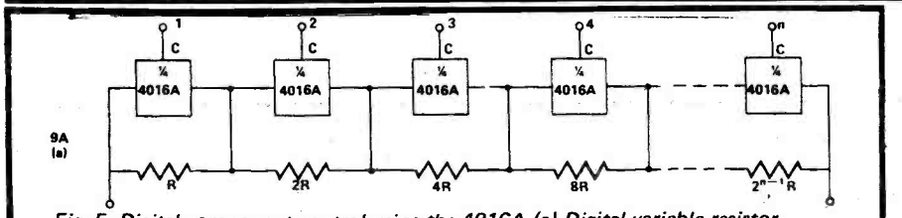
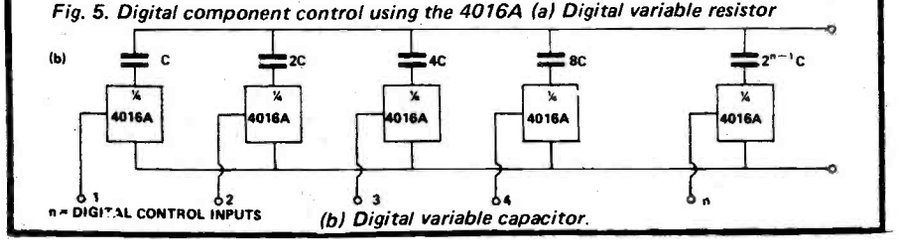


Fig. 5. Digital component control using the 4016A (a) Digital variable resistor



(b) Digital variable capacitor.

D-A AND A-D TECHNIQUES

The next use of the quad bilateral switch we are going to consider is in the field of digital to analogue conversion but first we are going to look at the subject of conversion on its own. Fig. 6 shows a D-A converter of the type known as a weighted resistor network. The working of this circuit is easy to see and the reason it is practical in so simple a form in CMOS is that the high and low output levels from a simple gate are within a few millivolts of the supply line thus providing accurate voltage levels to the summing resistors. This simple form has disadvantages, one of which will become immediately apparent if you consider the diversity of resistor values required for an eight or nine bit version. It is for this reason that the R — 2R network shown in fig. 7 is more popular for most applications. It is difficult to explain how this configuration works without becoming involved in mathematics but it becomes fairly clear if a three bit version is written down with the voltages in and analysed.

The basic idea for one sort of A-D converter or encoder as they are often called is shown in the block diagram of fig. 8. This variety is called a binary ramp encoder and is similar to the ramp integration method often encountered in modified form in digital measuring equipment. The principle of operation of our binary version is that a binary counter counts up from zero until it reaches the equivalent of the analogue input. Contrast this approach with the continuous counter method outlined in fig. 9. This provides a continous approximation to the input and is thus generally more useful for continuously monitoring a single channel

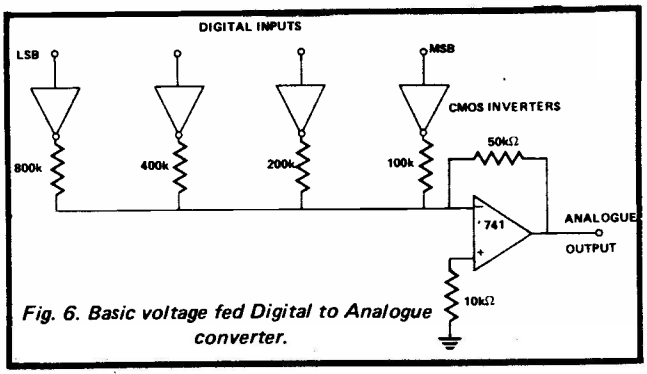


Fig. 6. Basic voltage fed Digital to Analogue converter.

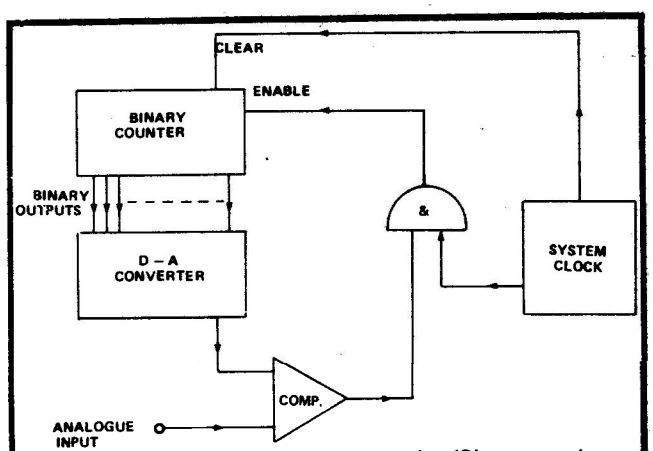


Fig.8. Outline of A-D converter using 'Binary ramp' method. The binary counter counts up to the required value so that the output is correct during only part of the cycle.

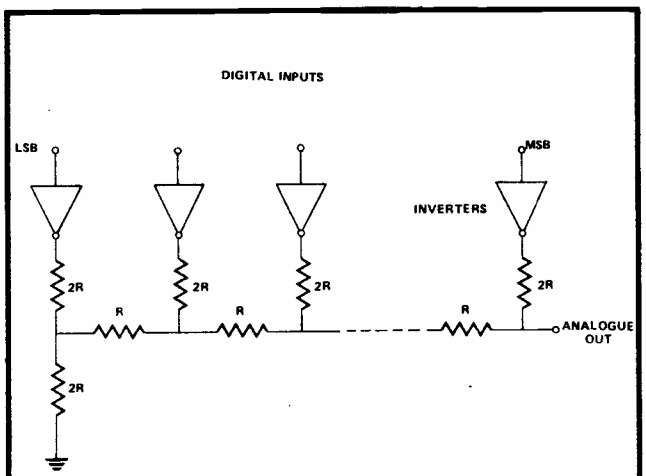


Fig. 7. The R–2R ladder network D–A converter.

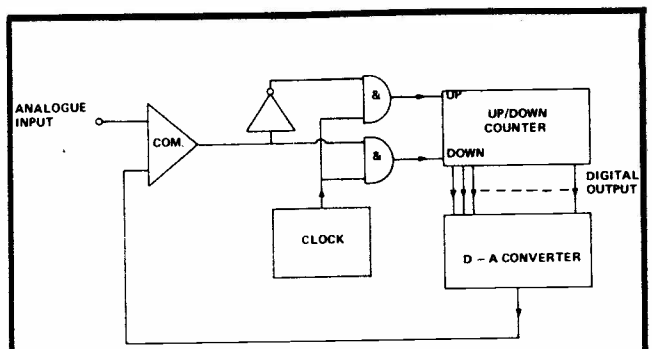


Fig. 9. A continuous counter type A–D converter. The clock just prevents the system oscillating at high frequency.

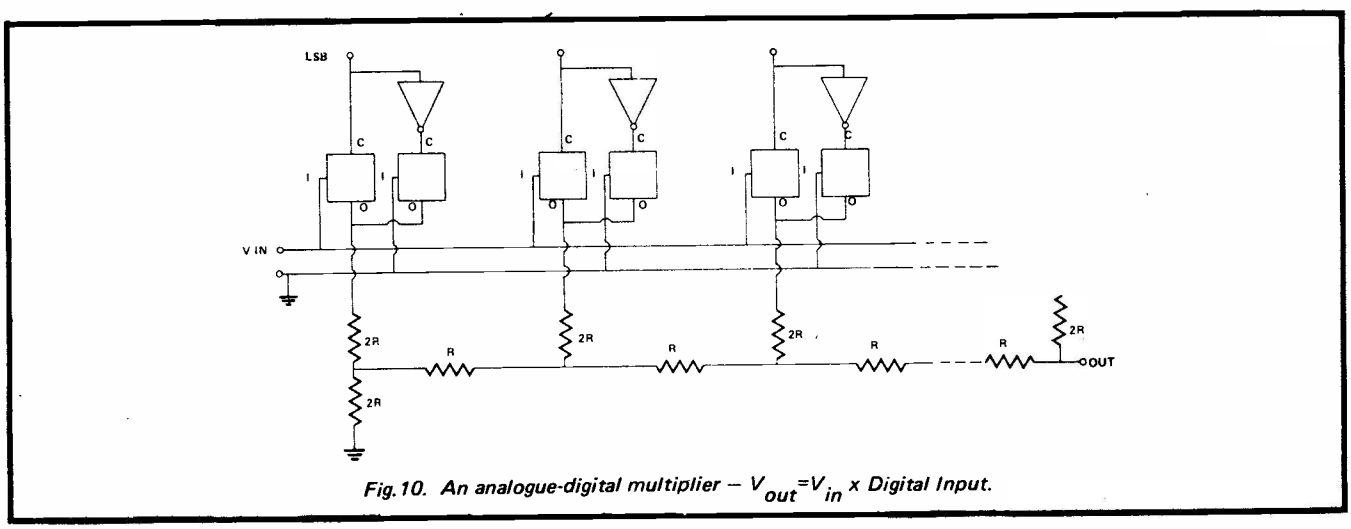


Fig.10. An analogue-digital multiplier – $V_{out}=V_{in}$ x Digital Input.

of information. It would be an advantage in many cases to have the counters working in BCD for ease of readout but this leads to complications which can not be gone into here. Finally on this subject it should be pointed out that these are circuits for experimentation and are unlikely to be directly applicable to any given situation. They have been included because of the ease with which they may be realised in CMOS compared, say, to TTL.

A-D MULTIPLIER

As far as digital to analogue conversion is concerned, using the 4016A we can take the idea a little further. What in fact we do (fig. 10) is to use an arbitary analogue voltage to feed the resistor ladder and so we multiply this input by the digital input and produce an analogue result. This "hybrid multiplier" is an interesting circuit, particularly because the analogue input voltage may be ac. thus producing several interesting waveforms and, on a more serious note, it may find application in hybrid computing experiments. We shall now leave the 4016A having, it is hoped, suggested some of the slightly less obvious uses of this versatile IC. ●

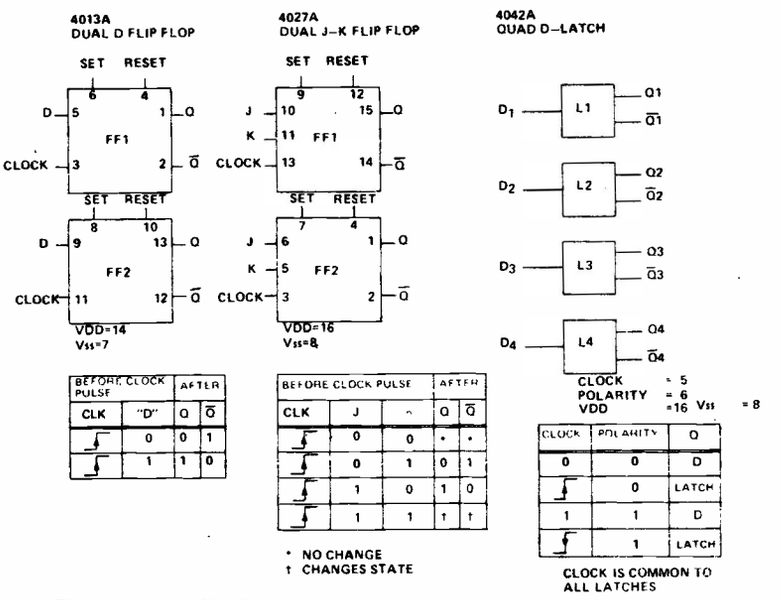
CMOS Part 3

FLIP-FLOPS

Our next subject is flip-flops — and we shall assume that the reader is familiar with the working of these devices and so the discussion will begin with the the pin-out diagrams in fig. 1. The first two are standard dual edge triggered devices with "D" and "J-K" type data inputs respectively. No doubt it is known that the "D" variety will divide the input frequency by two if "Q" is connected to "D" whereas the "J-K" type toggle, as this behaviour is called, when both "J" and "K" are held high. The set and reset inputs operate asynchronously (ie. independently of the clock) forcing the device into the "Q" = 1 and "Q" = 0 states respectively. These inputs operate when taken high in contrast to most TTL because TTL inputs rest high when disconnected whereas CMOS inputs must never be allowed to "float" anyway. Both the 4013A and the 4027A will operate up to about 8MHz.

The last device in fig. 1 (the 4042A) is a quad data latch of the sort often used for temporary storage of BCD digits in applications like frequency meter displays. If the polarity input is held low then the "Q" output follows the "D" input in each latch when the clock is also low but on the rising edge of the clock pulse the outputs are isolated and retain the data present at that moment. When the polarity input is high all this works the other way round. The clock inputs to all these devices should have rise times of 5μs or less (at V_{DD} = 10V).

Flip-flops on their own have uses in control circuitry and counters. If you wish to produce a counter to count through an odd sequence (a Gray code for example) it is advisable to find out about Karnaugh maps and associated techniques which aid the design process considerably. The standard form for such counters is a sequence of flip-flops whose inputs are derived from the outputs of the others by a few simple logic gates. As far as simple binary is concerned, the required set-up is shown in fig. 2 but we shall have a lot more to say on the subject of counters in general later.



BEFORE CLOCK PULSE		AFTER	
CLK	"D"	Q	$\bar{Q}$
⊓	0	0	1
⊓	1	1	0

BEFORE CLOCK PULSE			AFTER	
CLK	J	K	Q	$\bar{Q}$
⊓	0	0	*	*
⊓	0	1	0	1
⊓	1	0	1	0
⊓	1	1	†	†

* NO CHANGE
† CHANGES STATE

CLOCK	POLARITY	Q
0	0	D
⊓	0	LATCH
1	1	D
⊓	1	LATCH

Fig. 1. Three common flip-flop devices.

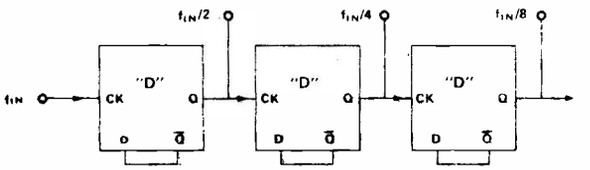


Fig. 2. Basic binary counting chain used for frequency division.

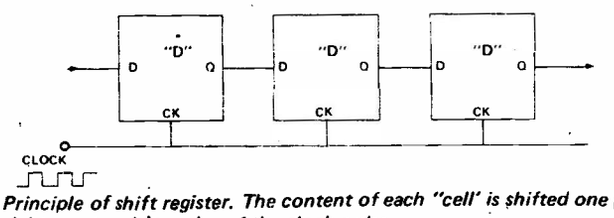


Fig. 3. Principle of shift register. The content of each "cell' is shifted one place to the right on the rising edge of the clock pulse.

The other main application of flip-flops is in shift registers. A shift register is a sequence of flip-flops so interconnected (see Fig. 3) that on a clock pulse the content of each device is transferred to the next one down the line. The register so formed is referred to as a static device because, unlike some MOS devices available, data is not lost if it is not shifted for some length of time. One modification to the basic device is to provide inputs and outputs to individual flip-flops in the chain and in this form, shift registers have many applications in serial to parallel and parallel to serial data conversion. This though is another subject which must wait until a little later in our discussions.

COUNTERS

Our main subject in this part is counters. It might well be true to say that the range available (compared to TTL) reflects the advances which have been made in other branches of electronics, particularly display technology. BCD counters are conspicuous by their absence as they have generally been replaced by seven segment decoded counters. One disadvantage is a need in many cases for external drivers for LED displays but this will be eliminated when Liquid Crystal technology is more advanced and, hopefully, cheaper.

BINARY COUNTERS

As usual we will start with the less glamorous devices in the range which, in the present instance, are the straight-forward binary counters. First we should mention the general operating conditions required for all CMOS counters. The clock input rise and fall times should be less than 5μS and the operating frequency limit is about 2.5MHz at V_{DD} = 5V rising to 5MHz at 10V. As far as the problem of drive current is concerned, it is advisable to consult the full data sheets for the device in question but it is reasonable to assume that no trouble is likely to be experienced if the requirement is less than 0.25mA with a 5V supply or 0.5mA with 10V.

Fig. 4 gives the pinout diagrams for CMOS seven, twelve and fourteen stage binary counters. The outputs are labelled B, with B_0 the most significant bit (i.e. giving greatest frequency division). It will be noted that three of the less significant bits are not available as outputs on the 4020A and this limits its usefullness in "divide by N" applications as we shall see later. The greatest division of the input frequency is 128 for the 4020A, 4096 for the 4040A and 16384 for the 4020A. In all cases the counters step on the negative transition of the clock pulse and the reset input sends all stages to logical zero independently of the clock when it is taken high. There is also a twenty-one stage counter (the 4045A) which produces two out-of-phase pulses at separate outputs for every 2097152 input pulses. It

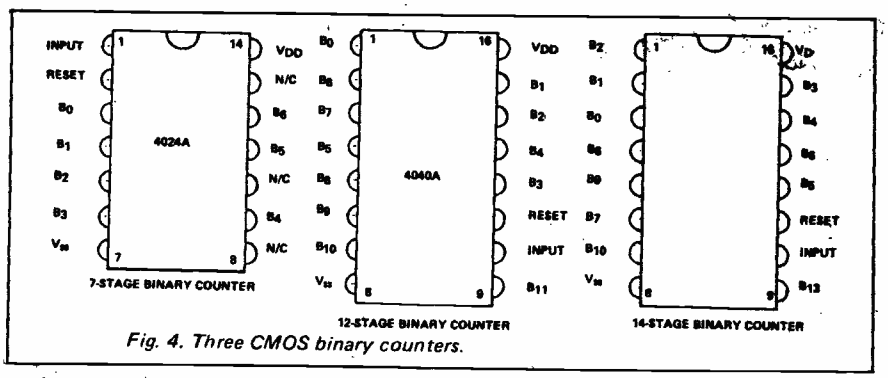


Fig. 4. Three CMOS binary counters.

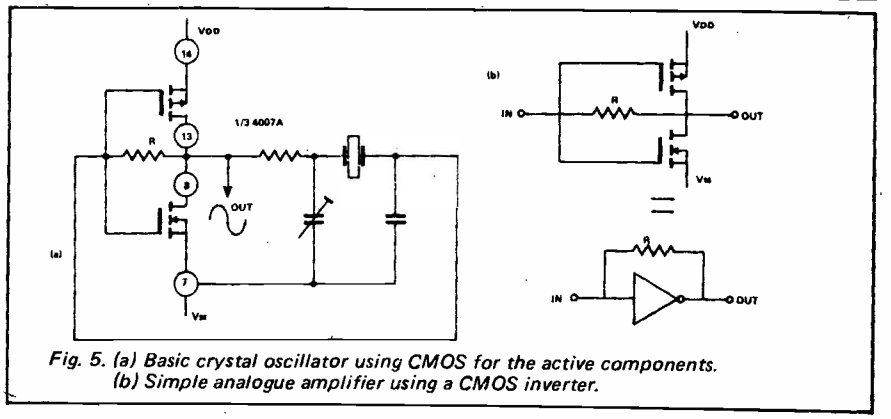


Fig. 5. (a) Basic crystal oscillator using CMOS for the active components. (b) Simple analogue amplifier using a CMOS inverter.

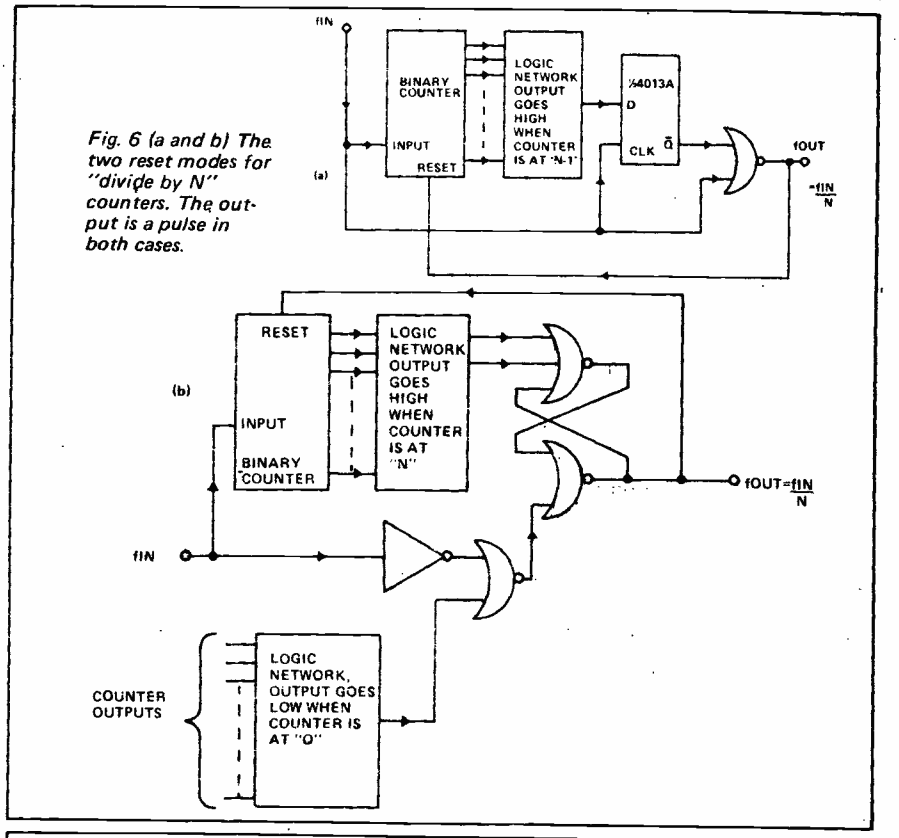


Fig. 6 (a and b) The two reset modes for "divide by N" counters. The output is a pulse in both cases.

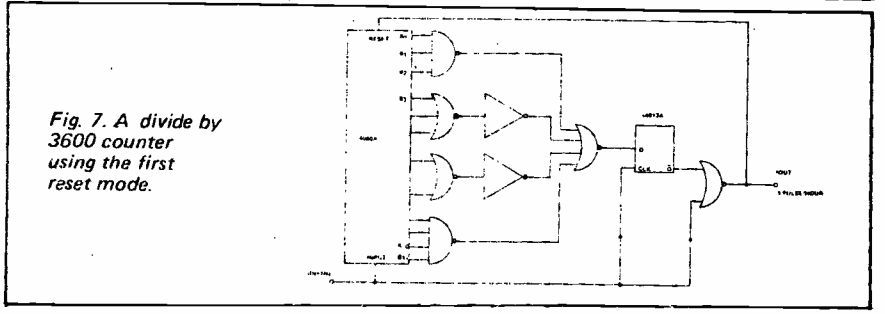


Fig. 7. A divide by 3600 counter using the first reset mode.

is intended for producing one second pulses from 2.097152 MHz crystals for driving clock circuitry and similar applications. Anyone interested in using this device should obtain data from a manufacturer.

While we are on the subject of huge frequency division chains perhaps we should consider crystal oscillators very briefly. Fig. 5(a) shows one common set-up and it is worth noting that the configuration in Fig. 5(b) is the standard way of producing a simple analogue amplifier from a CMOS inverter.

DIVIDE BY N COUNTERS

There are times when it is required to divide a signal by other than some power of two and by using a 4024A or 4040A we may divide by any number from 2 to 128 and 4096 respectively, althqugh extra components are required. Fig. 6 shows two ways of achieving this end. The circuit in (a) has the binary counter feeding a system of logic gates, the output of which goes high when the counter reaches N-1 (where N is the number the input frequency is to be divided by). This happens on the falling edge of the clock pulse because the counters are negative-edge triggered. On the next rising edge the flip-flop Q output goes low and when the clock goes low again the output goes high, generating a pulse of length equal to one half of the clock period which resets the counter. It is interesting to draw a timing diagram for this circuit and prove it works. It should be noted that although the actual output is a positive going pulse, a similar pulse of twice its length (i.e. one clock period) is available at the Q output of the 4013. A divide by 3600 counter which will provide one pulse an hour from a 1Hz input is shown in Fig. 7 as an example of the technique.

The second mode has the advantage that the "N" count and not the "N—1" count is detected, but two logic networks are required; one to decide when the counter has reached "N" and another to identify the "all zeroes" state and reset the output. It is also a disadvantage in some applications that the counter spends a brief period in the "N" state. It is again interesting to draw a timing diagram and it is worth noting the cross-coupled NOR gates used as an R-S flip-flop. As an example a divide by twenty four counter is shown in Fig. 8 to produce one pulse per day from the one per hour output of Fig 7. The circuit dissipation of both the counters would be very low (less than 1mW) at this low operating frequency and the only note of caution to be sounded is that the counter and flip-flop should not both be triggered from the same edge of the clock pulse (i.e. one should be positive and the other negative edge-triggered).

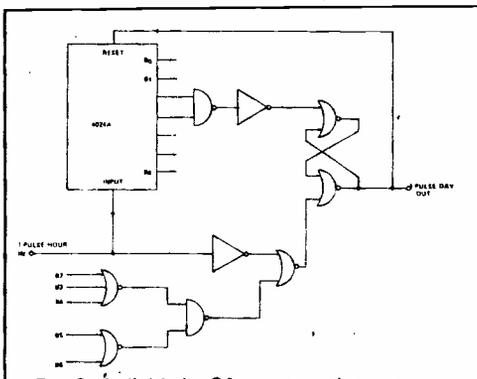


Fig. 8. A divide by 24 counter using reset mode two. Note the simplicity that may be achieved in the logic networks – one NAND gate serves to identify "24".

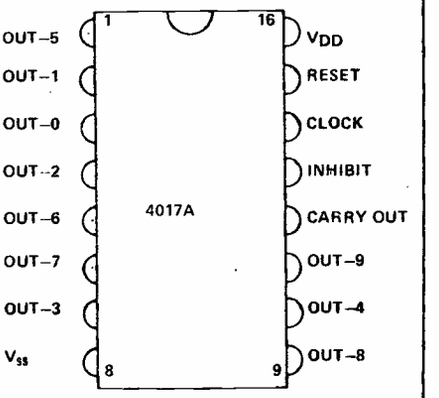


Fig. 9. Pin-out diagram of the 4017A decimally decoded decade counter.

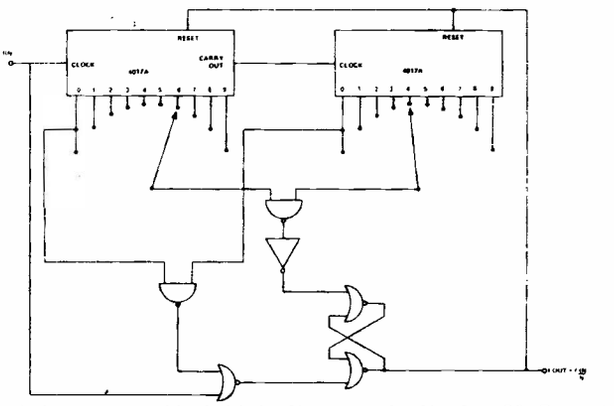


Fig. 10. A switch programmable divide by N counter for N = 2 to 99. Extension to higher N is obvious.

A DECIMAL-DECODED DECADE COUNTER

All the old hands at TTL will doubtless be familiar with the 7490 decade counter and 74141 decimal decoder driver. The 4017A combines the count and decode functions in a single package but has the disadvantage of low output drive capability. Buffering the outputs with 4049A inverters will raise the available output to about five or ten milliamps at supply voltages of five and ten volts respectively. The pin diagram is given in Fig. 9 and the counter advances one on the positive clock transition provided that the inhibit is held low. The reset operates asynchronously when taken high as usual. "Carry-out" may be used to clock the next stage in a multi-stage counter. This device has fairly obvious applications in controlling switches in multiplexing equipment as one and only one output is high at any one time. It is fairly clear also that we may extend the techniques of divide by N counters to cover these devices with the added bonus of them being switch programmable. Fig 10 shows this idea realised using reset mode two because of the ease of switching for N rather than N-1. This circuit has lost an inverter compared with Fig. 6b, this being the change necessary to adapt the circuit for counters and flip-flops which operate on the same clock transition. The sequence of counters could clearly be extended to any desired length and it is an interesting thought that seven of these counters (4017As) and the attendant gates could, when fed with a 1Hz input, generate pulses at any interval from two seconds to over three months! On a more practical note, used in a phase locked loop circuit a most versatile digital frequency synthesiser would result. Remember however that the output is a pulse and it would need squaring (one more flip-flop) before most phase comparators would accept it.

SEVEN SEGMENT DECODED COUNTERS

We mentioned earlier that CMOS IC design reflected the changes in display technology. Two particular examples of this phenomenon are the 4026A and 4033A decade counters with seven-segment outputs. The pin-out diagrams for these devices are shown in Fig 11 and, as one might guess, the counters are identical with the exception that the 4026A has a display enable function for use in multiplexing digits and an ungated C-segment output, whereas the 4033A has ripple blanking and a "lamp-test" facility. We shall consider the use of these special facilities when we have discussed the features common to both. The devices are positive edge triggered and advance only when the clock enable is low. The reset operates when taken high as usual and the segment outputs go high when they are active. Just as in the 4017A the signal at the "carry out" terminal may be used to clock the next stage in multi-decode applications.

In the same way as we have considered for other counters, the seven segment outputs may be identified by logic gates and the counters made to divide by any number. Fig. 12 gives the information necessary and it should be noted that the "N-1 and flip-flop" method is used because the other method does not count through zero. If anyone wants to strike a blow for freedom against LSI we have covered most of the devices necessary for designing a CMOS digital clock. Now we will have to consider the interfacing of displays with our seven segment counters. LEDs like the MAN-3 which have a low current will interface directly with the outputs of the 4026A or 4033A and give a tolerable brightness with the available drive current (about 5mA), provided that V_{DD} is more than 9V. If we drop the voltage down to between 4 and 9V then NPN transistors should be inserted as shown in Fig. 13a and if the supply drops even lower, the addition of inverting buffers is recommended. The seven transistors needed are generally the components of a single IC. The attention of the reader is drawn to the discussion on current limiting resistors to follow.

MULTIPLEXING

Life is never as simple as we might want and there are *two* reasons for complicating the circuitry by using digit multiplexing

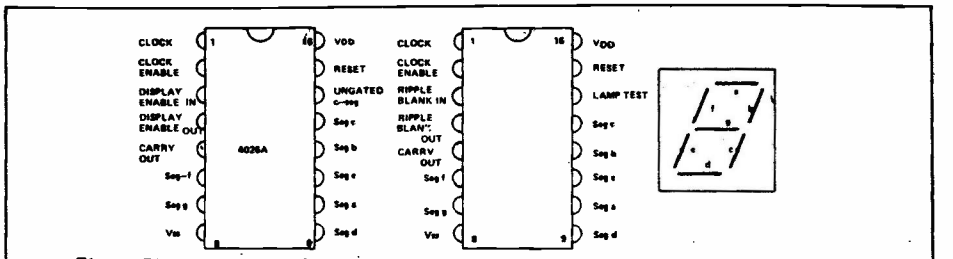


Fig. 11. Pin-out diagram for the 4026A and 4033A seven segment decoded decade counters. The labelling of the segments is also shown.

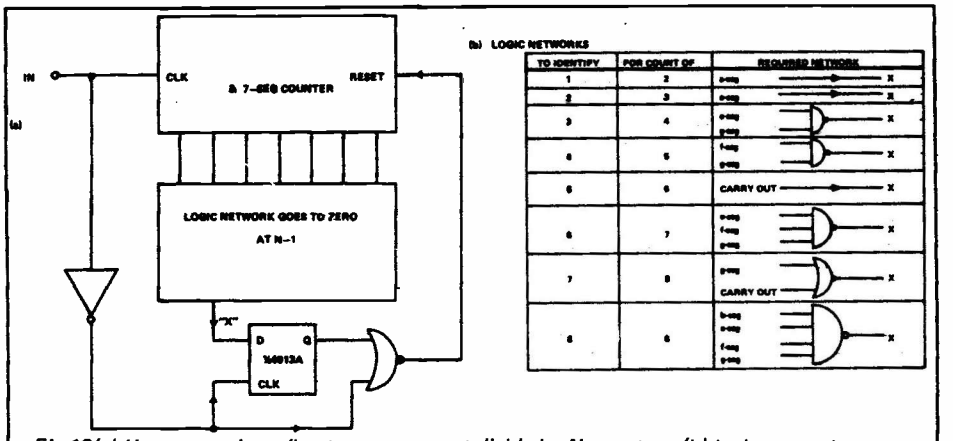


Fig. 12(a) How to produce direct seven segment divide by N counters, (b) logic networks to identify each digit. The extension to a multi-decade version is simple.

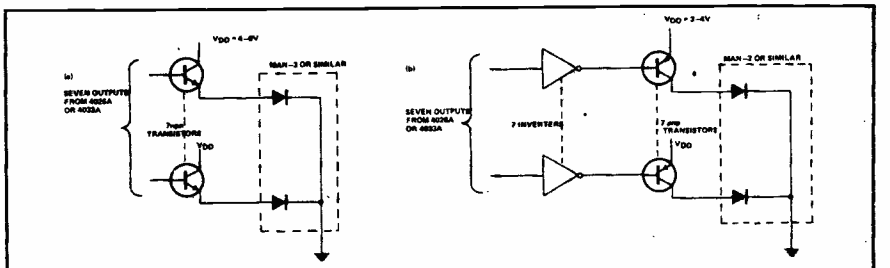


Fig. 13. Driving MAN-3 type displays (a) at intermediate supply voltages and, (b) at low voltage.

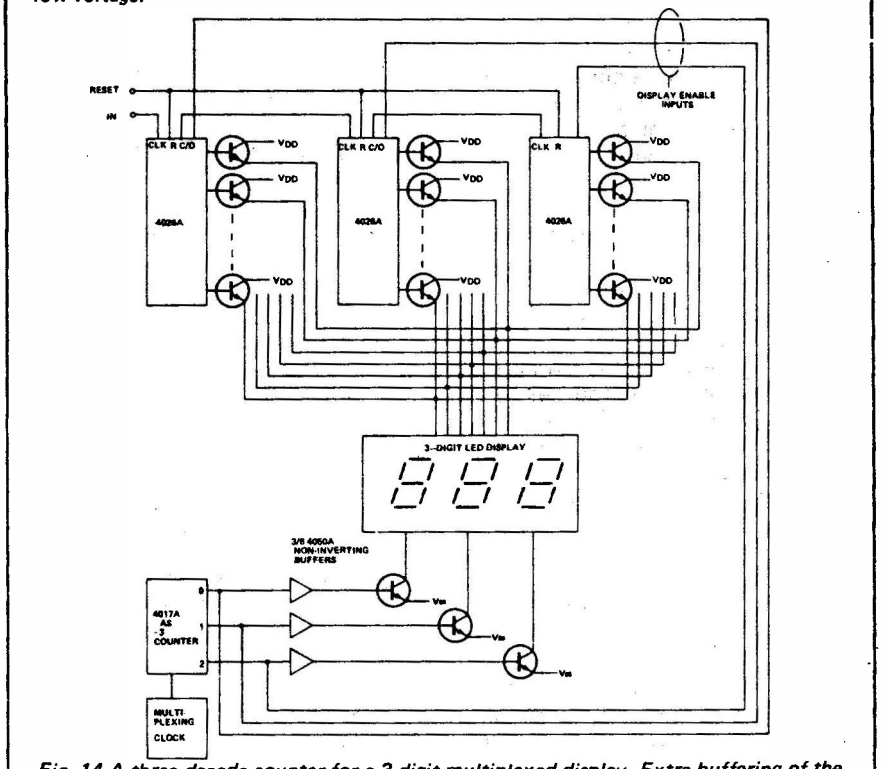


Fig. 14. A three decade counter for a 3-digit multiplexed display. Extra buffering of the digit lines may be necessary for some displays.

(ie each digit is displayed for a fixed period, usually between about 10 and 30% of the time). These are that to do so is more efficient in terms of power consumption and secondly that most multi-digit displays reduce the number of lead-outs (by giving just one set of seven segment drive lines for the complete display and one digit drive line for each digit).

This is the reason why the 4026A has a display enable input which, although the counter continues to function, cuts off the display when it is held low. The display enable output gives a replica of the input and may be used to enable other counters which are to be "on" during the same period. It also explains the presence of the "ungated C-segment" output which is used for producing some divide by "N" configurations which operate when the display is disabled. The basic arrangement of a three decade counter is shown in Fig. 14 and attention is drawn to the note that additional buffering may be necessary on the digit lines. It is also worth noting the use of a 4017 divide by three counter (using the flip-flop reset mode) to control the display.

Other sorts of displays which are often used are higher current LEDs such as the MAN-1 which is, in contrast to the MAN-3, a common anode device. This means it must be driven by inverting buffers as shown in Fig. 15a. We have been relying here on the output current limit of the CMOS chip to limit the forward current in the LEDs. Particularly when transistor drivers are employed it may be necessary to add current limiting resistors in the segment lines. The calculation of the value is simple given the required segment current and voltage drops (see Fig. 15(b)). In multiplexed displays the limiting resistors should, of course, be put in the common segment lines and it is worth noting that a considerable saving in resistors in non-mutliplexed displays may be achieved by putting a single resistor in the common line to each digit. The pay off is that the display brightness varies with the digit. Fig. 15(c) shows the technique for interfacing with "Numitron" and similar displays.

The ripple blanking facility is for blanking leading and trailing zeroes in the display and it works as follows. Take the ripple blanking input (RBI) of the most significant 4033A on the integer side of the display low. Then take the ripple blanking output (RBO) of the IC and connect it to the RBI of the next counter and so on until the position of the assumed decimal point is reached. Follow exactly the same procedure from the least significant counter in the fractional part of the display backwards to the decimal point (see Fig. 16(a)). Of course, if the assumed decimal point is at one end of the display then half the procedure would be unnecessary. If non-significant zeroes in the places either side of the decimal point are to be displayed (so that 7 and .6 appear as 7.0 and 0.6) then the RBI's of the two counters concerned should be taken to V_{DD} (as in Fig. 13(b)). Finally on these two ICs, the lamp-test facility on the 4033A just forces all segment outputs high when it is taken high.

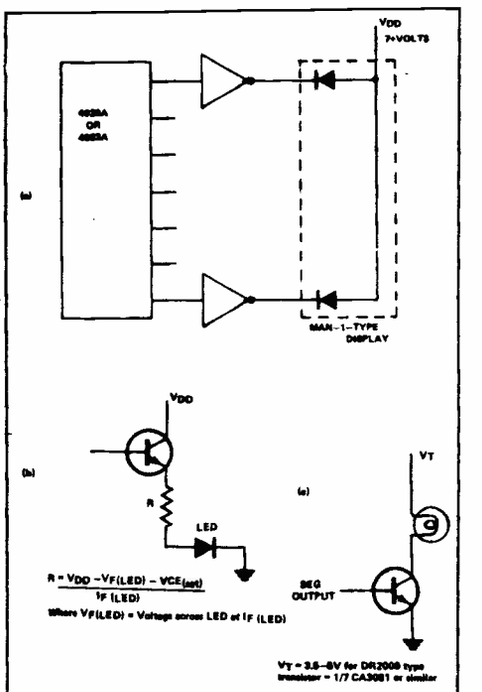


Fig. 15. Driving others displays:- (a) MAN-1 type (b) example of calculation of limiting resistor (c) Numitron type incandescent display.

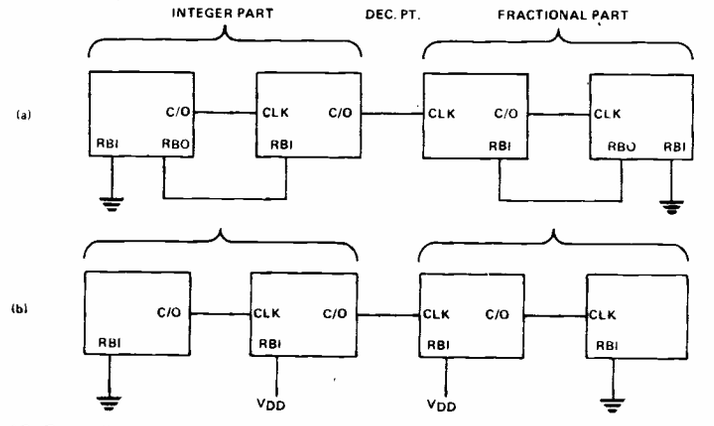


Fig. 16. Four digit counters using the 4033A with non-significant zero supression (a) in all positions (b) in first and last position only.

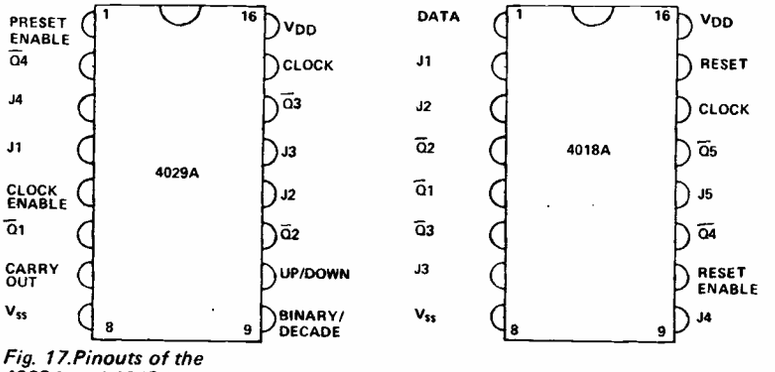
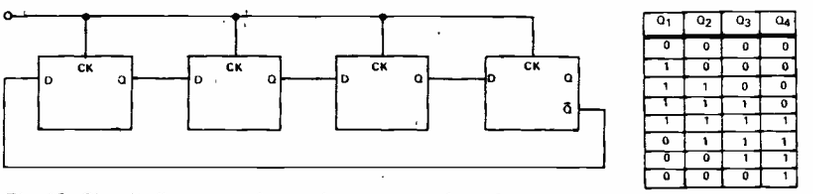


Fig. 17.Pinouts of the 4029A and 4018A.



Q_1	Q_2	Q_3	Q_4
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1

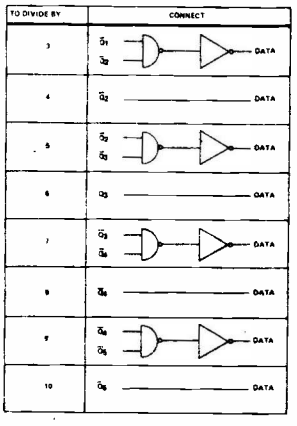
Fig. 18. Circuit diagram and counting sequence for a four stage Johnson or "twisted ring" counter.

THE 4029A AND 4081A

We shall conclude our discussion of counters by looking briefly at two more devices. The 4029A is a general purpose counter which, has most of the features of the more exotic TTL devices. Briefly, the device is positive edge triggered and advances when the clock and preset enables are both low. Furthermore it counts in binary when the Binary/decade input is high and BCD otherwise, a high signal at the up/down input persuades it to count up and a low input forces it to count down. As though this were not enough, when the preset enable input is high, the Q counter outputs are forced to follow the J ("Jam") inputs. The suffix "4" in both cases indicates the most significant digit. The pinout diagram is given in Fig. 17 along with that for the 4018A presettable divide by N counter.

There are two basic ways of producing counters. Firstly there is the chain of flip-flops each of which halves frequency produced by the one before it. This was the principle behind the binary counters, which we considered at the beginning of this part's discussion, and also of the 4029A. The second method is known as a Johnson counter and it is basically a shift register consisting of a chain of flip-flops (see p59) with the Q output of the last counter connected back to the data input. A little patience and a pencil and paper will soon show that such a counter will divide the input frequency by 2N where N is the number of stages. The counting sequence for a four stage counter is shown in Fig. 18 and the reader will notice that if the counter starts with contents not in the counting sequence (e.g. 1010) then the contents are always nonstandard thereafter. Thus some special gating is required. The simplified internal diagram of the 4018A in Fig. 19 is not complete. Also the Jam inputs and preset enable (which work in the same way as in the 4029A) together with the reset (which zeros all stages (Q1 — Q5 = 1) have been omitted for clarity. Fig. 20 shows the way to connect the 4018A to divide by all numbers from three to ten. Just as an example of how versatile this device is one application will be considered in a totally different field from counting. By disregarding the clock the Jam inputs and inverted data outputs (Q) can be used as a five data latch for temporary storage, the outputs being updated to the inputs while the present enable is high. ●

Fig. 20. Connection of the 4018A as a divide by "N" counter Input to clock, output waveform from DATA input is symmetric when N is even, almost so when N is odd.



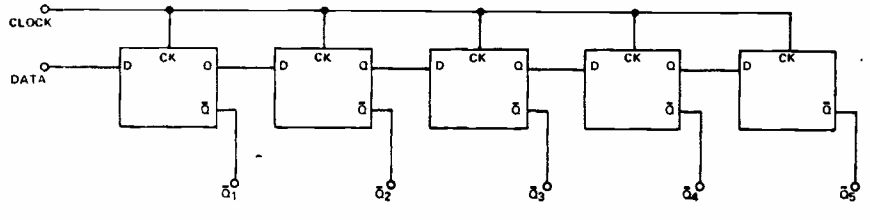


Fig. 19. Simplified internal diagram of the 4018A.

(ETI staff conference)

CMOS Part 4

We have already seen how flip-flops may be cascaded to form shift registers and, as you might guess, these are available already connected in a single IC. As usual we will start with some pin-out diagrams.

Referring to fig. 1 we start with the 4015A, a dual four stage serial input parallel output (SIPO) version. The two parts "A" and "B" are independent and each consists of four D-type flip-flops with outputs Q1-Q4 and data is transferred from each one to the next and from the data inputs to the first on the rising edge of the clock pulse. A high input to the reset clears all the outputs to zero.

The 4006A is an 18 stage device with the registers so arranged that 4, 5, 8, 9, 10, 12, 13, 14, 16, 17 and 18 stage registers may be produced. These are serial in-serial out (SISO) devices. It should be noted that the clock input is common to all the stage so that although two separate five stage registers could be produced they would have to share the same clock.

Finally in fig. 1 we have the 4014A and 4021A which are both eight bit registers with the same pin connections. The 4014A works as follows: On the rising edge of the clock pulse, the data is all shifted down and a new datum accepted from the serial input if the parallel/serial input is low. If instead it is high, no shift occurs and instead each stage of the register adopts the state present at the parallel inputs. The 4021A is similar in almost all respects except that when the Parallel/serial is taken high the stages are jammed asynchronously (i.e. it does not wait for the clock transition like the 4014A). We mentioned earlier that the 4042A quad D latch is often used for temporary storage but for many applications a shift register is superior, giving options of serial or parallel operation. As far as eight bit data manipulation is concerned, the ultimate shift register must surely be the 4034A whose pinout is given in fig. 2. It is described as a bi-directional bus register because the two data lines "A" and "B" are interchangeable in that if the A/B input is high the A lines are inputs and the B lines are outputs, whereas when A/B is held low the reverse applies. When the parallel/serial input is high then data is accepted from the parallel inputs (on the positive clock transition when Asynch / synch is low, asynchronously otherwise) whereas when parallel/serial is low data is accepted from the serial input and shifting is performed on the positive clock transition. The only other feature is the A-enable input which enables the A lines when it is high thus allowing several registers to feed a common bus. Designers of large digital processing systems will find many applications of this device.

Applications of shift registers in data storage and conversion are not really very interesting out of context and so we will look briefly at counters. The connection of shift registers (under the guise of a sequence of flip-flops), to form Johnson counters, has already been

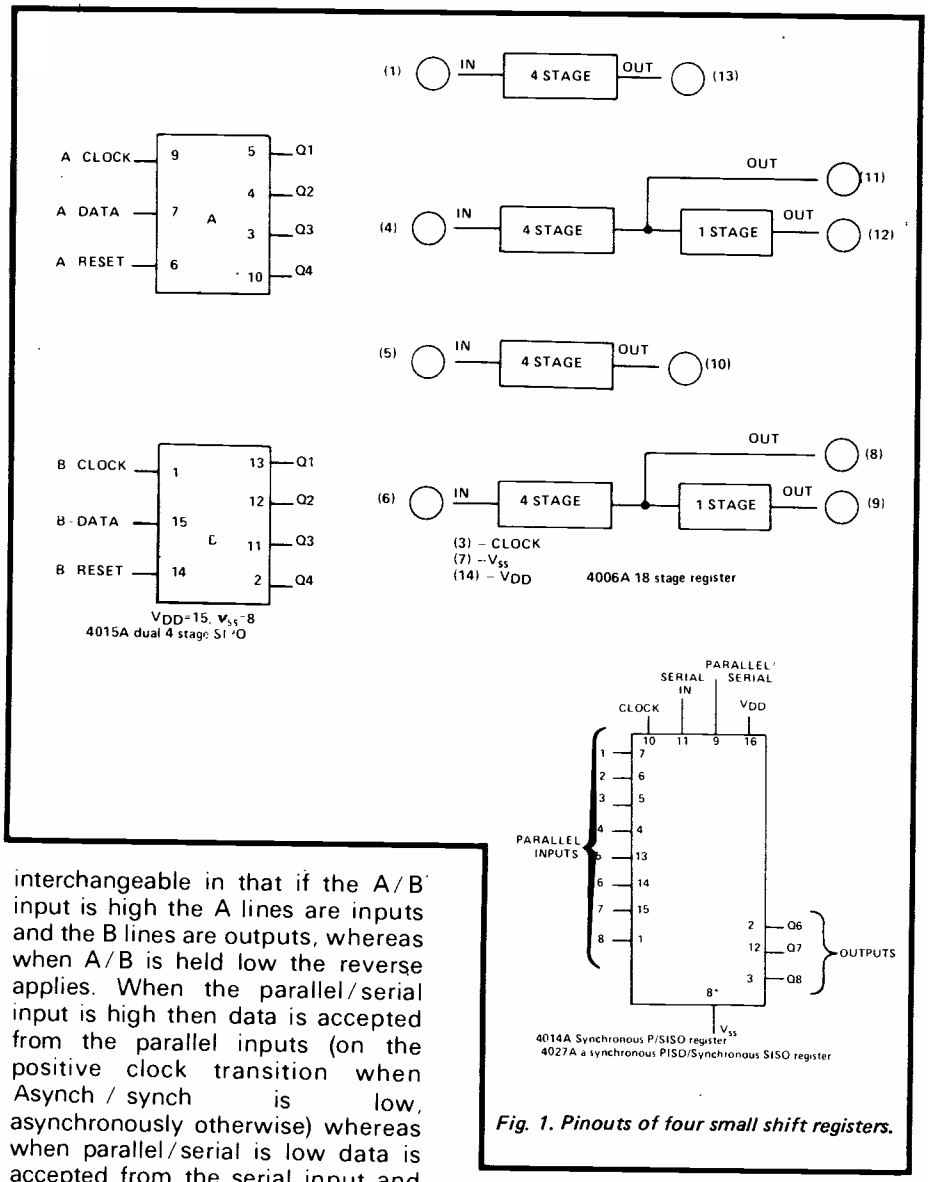


Fig. 1. Pinouts of four small shift registers.

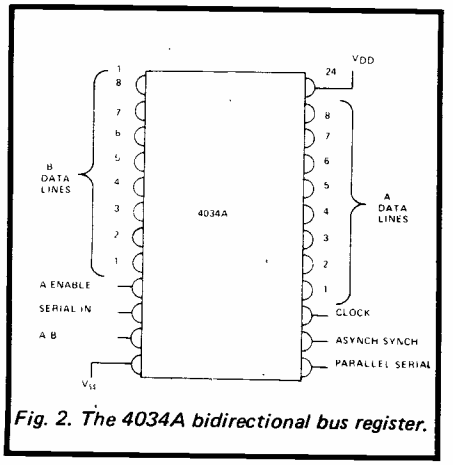
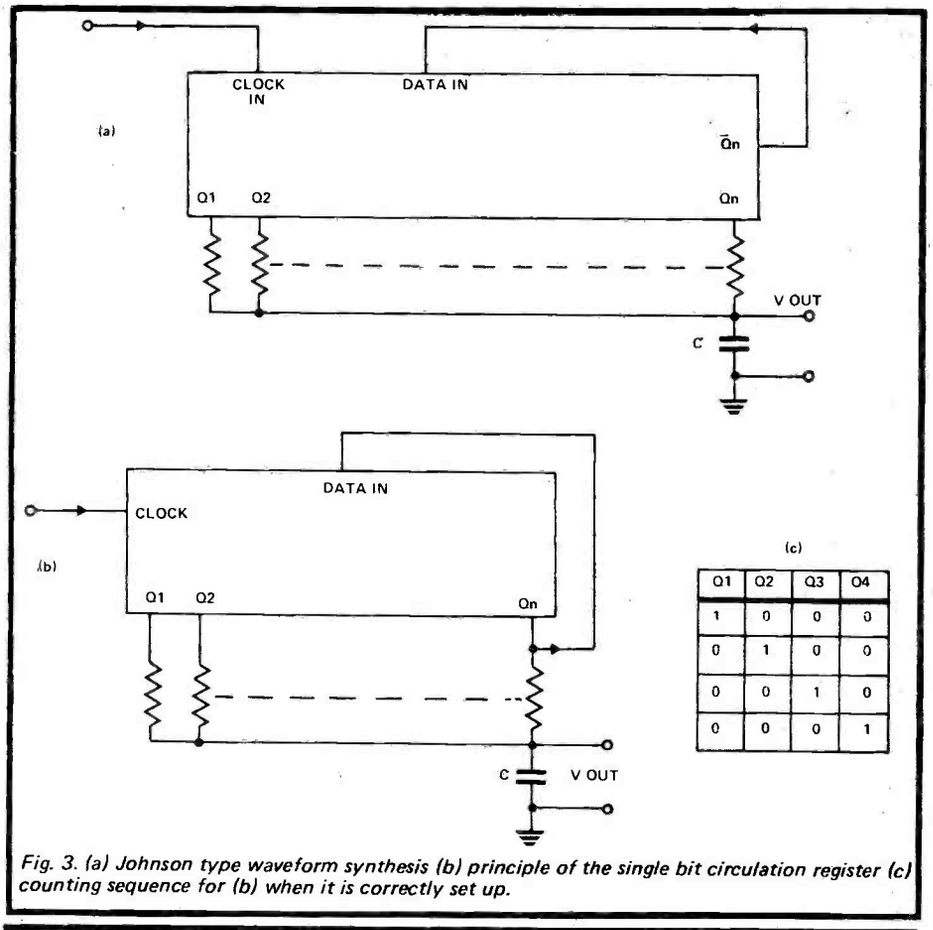


Fig. 2. The 4034A bidirectional bus register.

considered but it is worth noting that in the same way as we produced digital to analogue converters from counters we can also produce waveform synthesisers from Johnson counters (see fig. 3(a)). The calculation of the required value of each register is rather tedious because each is on for half a complete cycle. Nevertheless, an eight stage register gives sixteen separate values out but not all of these are independent. On occasions this method is superior to the single bit approach. The circuit in fig. 3(b) is not complete because the single bit must be inserted to start with. If the application will tolerate switches in the starting sequence it is a trivial design exercise but if complete auto-starting is required it becomes quite interesting.

These small registers we have been considering are by no means the top end of the range. Fig. 4 gives the pinouts for some high capacity registers. The 4031A is a single sixty-four stage shift register, the only addition being a $\bar{Q}$ output and mode and recirculation connections. When the mode control is low the recirculation input is inoperative and data accepted from the data input. When mode is high, however, data is accepted from the recirculation input instead. Thus if the Q output is connected to the recirculation input a register is formed with a control input which will either recirculate its contents continually or accept new data, depending on the control signal. You might well wonder why the recirculation input is not internally connected to the Q output. This is not done because it would generally reduce the versatility of the device and, more particularly, would prevent the formation of multi-chip recirculating registers like the one shown in fig. 5(a). The 4013A is positive edge triggered and it has also got a delayed clock output which, as the name implies is a replica of the clock signal delayed by several hundred nano-seconds so that the cascading method shown in fig. 5(b) may be used. The addition of the flip-flop if recirculation is required should be noted as without it this method will not work. The cascading method in Fig 5(a) must be used for highest speed operation although it requires higher clock drive.

Having said so much about the 4031A there is less to say about the next three devices. The 4517 is dual sixty-four bit register, the two devices being distinguished in the pin diagram by the suffices 'A'' and ''B''. During normal operation the device is positively edge triggered, data is entered at the data pin and outputs are available at Q16, Q32, Q48 and Q64. This is with the write enable low. When it is high however data is entered at the data, Q16, Q32 and Q48 pins (the Q16 pin acting as a data input to stage 17 etc) thus allowing complete filling of the device in sixteen clock periods.



Q1	Q2	Q3	Q4
1	0	0	0
0	1	0	0
0	0	1	0
0	0	0	1

Fig. 3. (a) Johnson type waveform synthesis (b) principle of the single bit circulation register (c) counting sequence for (b) when it is correctly set up.

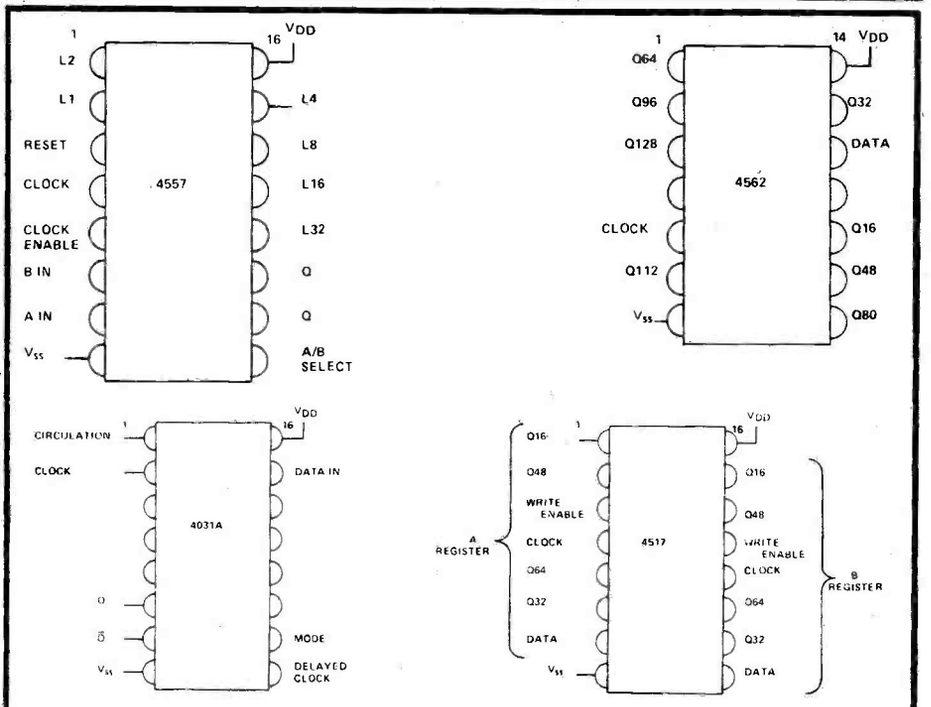


Fig. 4. Some larger shift registers.

The 4562 is a straight forward one hundred and twenty eight stage positive edge triggered device with no additions except outputs every sixteen stages throughout. The 4557 is an altogether more interesting device. Basically, the length of the shift register between the A and B inputs and the $\overline{Q}$ and $\overline{Q}$ outputs is equal to the sum of the L inputs which are high plus one. Thus if L32 and L4 are the only ones held high the shift register will be of length 32+4+1 = 37. The reset input clears all stages to zero when it is taken high. The A/B select input is used to decide whether the A or B inputs will be used as the data source, when it is low B is used, when it is high A is chosen instead. It should be clear from our previous discussion how a recirculating register could be formed. As for the clocking, when the clock enable is low the device behaves as a conventional positive edge triggered register, but if negative edge operation is required this can be achieved by holding the clock at logical one when a falling edge at the enable input will operate the device. Using this device as a Johnson counter would lead to an interesting binary programmable symmetric frequency divider. Before we leave the subject of shift registers we will point out that all those we have considered are static devices which means that they maintain their state even if they are not clocked for some time. A two hundred stage dynamic shift register is available but there is not really time to describe it here. Its type number is 4062A.

MEMORIES

Of course, a shift register can be used as a memory. The disadvantage is that it is a serial access device which means that a lot of unwanted information must often be passed by while the piece we require is arriving. Random access memories (RAMS) avoid this problem because access is by a set of address lines, the signal on which determines which bit of the memory is to be written to or read from. We intend here just to give brief details of one available device (see fig. 6). The 4061A two hundred and fifty six bit static RAM has been chosen as our example because it is simple enough for a brief description of its features to be given easily. A0 to A7 are the eight binary address lines necessary to specify any one bit and these should only be changed while the chip enable input is high. Only when the chip enable has returned to zero can read and write operations be performed, reading when "read/write" is low, writing otherwise. The buffering of the outputs is such that the data in line may be tied to either data out or data out if desired. It should also be noted that the V_{SS} and V_{DD} pins are unconventionally positioned so that the devices are compatible with other MOS memories. Of course, there are a few other pieces of timing protocol to be observed. For example, the chip enable signal should not go low too soon after an address change but we will not go into these here as anyone who uses this device in a system will doubtless be obtaining data sheets for other devices anyway.

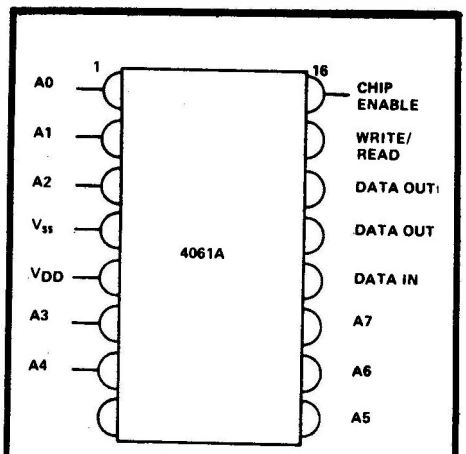


Fig. 6. The 4061A static 256 bit random access memory (RAM).

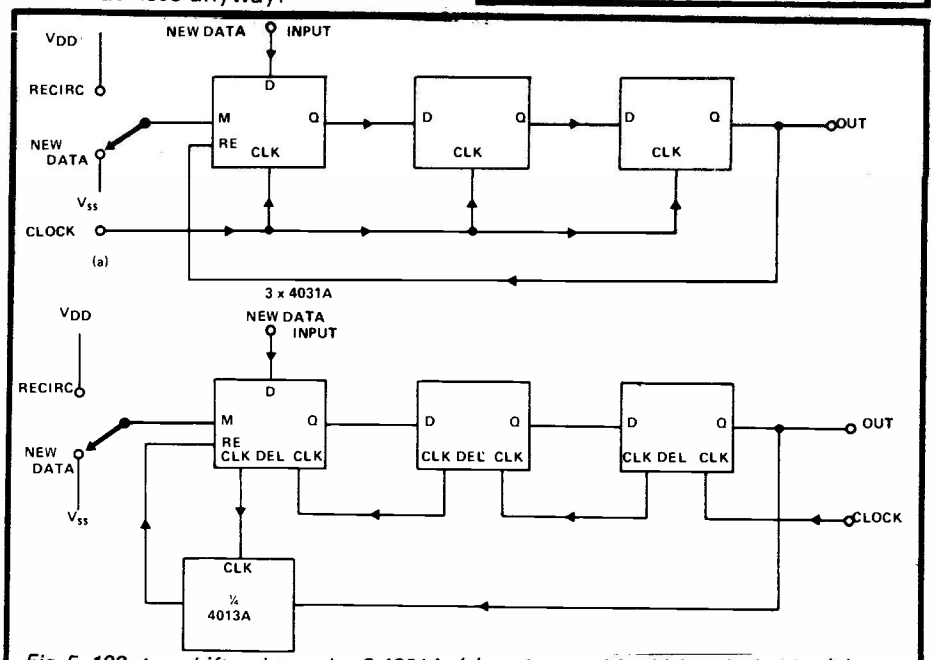
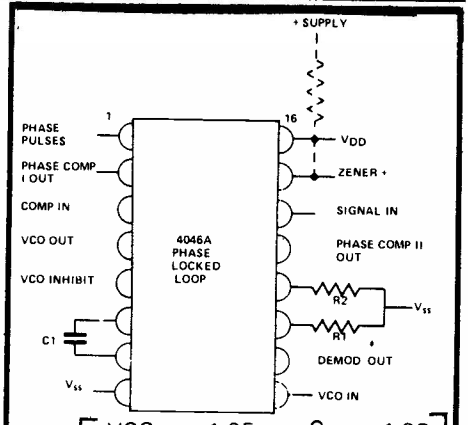


Fig. 5. 192 stage shift register using 3 4031A. (a) version requiring higher clock drive (b) version using delayed clock.

THE 4046A PHASE LOCKED LOOP

The possibilities of combining linear and digital circuitry on the same chip has made the fabrication of the 4046A phase locked loop possible in CMOS. As usual we will discuss this device with reference to its pin diagram which is given in fig. 7.

A zener diode of 5.2V is provided at pin 15 for supply regulation if required although the circuit will operate at any value of V_{DD} between five and fifteen volts. The chip contains two phase comparators with outputs at pins 2 and 13. The first of these is an exclusive — OR network which requires a 1:1 mark space ratio at the input to work effectively, will lock onto harmonics of the input frequency but makes up for a lot by having good noise rejection and it also leaves the



$$f = K\left[\frac{VCO_{IN} - 1{\cdot}65}{R1 \times (C1 + 32)} + \frac{C_{DD} - 1{\cdot}35}{R2 \times (V_{DD} + 1{\cdot}6)}\right]$$

K = 0·95, V_{DD} = 5, 10V

K = 1·08, V_{DD} = 15V

f is in MHz, R1, R2 in MΩ (≥ 5kΩ)

Cin pF (≥50pF)

$1{\cdot}65 \leqslant VCO_{IN} \leqslant V_{DD}$ Ω 1·35V

Fig. 7. The 4046A pinout and formula for determining frequency.

voltage controlled oscillator running in mid-range with no input connected. In contrast to this, phase comparator 2 can handle pulses and leaves the oscillator running at minimum frequency. The output from one of these phase comparators is generally connected via a low pass filter to the input of the V.C.O. In passing we will mention that when the first phase comparator is used, the capture range (that is the range of frequencies that will pull the loop into lock) can be made less than the lock range (the range over which the loop will follow an already locked input) by using an appropriate low pass filter. In the case of comparator 2 however, the lock and capture ranges are identical.

The frequency of the V.C.O. for given R1, R2 and C1 is given in fig. 7. The highest frequency attainable is over 1MHZ but the supply voltage may need to be a full fifteen volts to achieve this with the cheapest plastic encapsulated devices. For experimenting purposes this description of the oscillator is probably sufficient but if it is required to design for specific frequency ranges, the R.C.A. data sheet on the device gives graphs which are easier to use than the somewhat cumbersome formula. Basically the smaller R2 is, the smaller the range the VCO may be swept over. If pin 12 is left open, the frequency can be swept from a negligible value to a megahertz or over.

If the signal in is within CMOS logic levels ("0" $\leqslant 30\%V_{DD}$, "1" $\geqslant 70\%V_{DD}$) then it may be directly coupled to the signal input but if capacitive coupling is used signals at least as low as 1.5V p-p will be accepted. The inhibit input saves power by disenabling the VCO when it is taken high and the "DEMOD OUT" terminal provides a buffered copy of the "VCO IN" signal for use as an output in demodulation set-ups. If this is used a resistor of 10kΩ — 1MΩ should be connected between it and V_{SS}. Perhaps we can save time by giving one or two examples of the use of the 4046A rather than talking about it further. Fig. 8 shows an F.M. demodulator designed to operate with a centre frequency of 10kHz. It uses phase comparator 1 for good noise rejection and the formula for the capture range shows that the values used give ±400Hz. As R2 is infinite the circuit will track over a very wide range and the linearity obtainable is very high.

Fig. 9 shows the outline design of a frequency synthesiser. The second phase comparator is used because it will deal with non symmetric output from the divider and will not lock onto harmonics. The V.C.O. is set with the pin 12 resistor infinite for maximum range. Three to nine hundred and ninety nine kilohertz in one kilohertz steps can easily be achieved. The low pass filter should be optimised for minimum settling times. The divide by N counter has been shown as a block as these have been discussed at length previously. ●

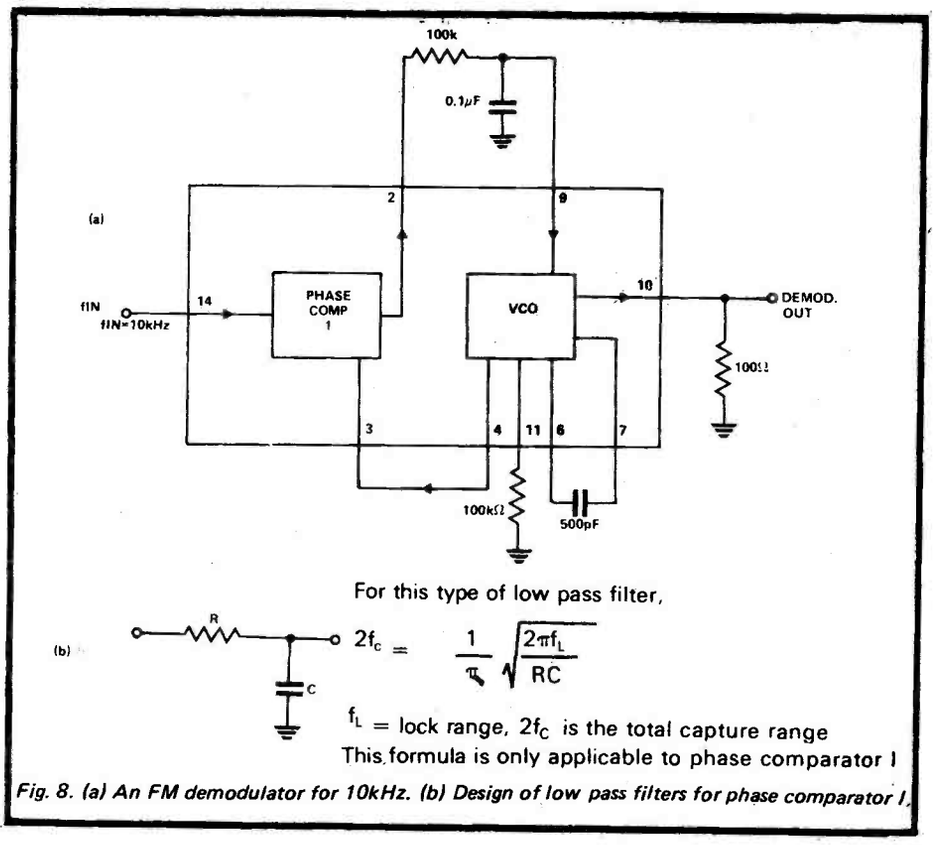


Fig. 8. (a) An FM demodulator for 10kHz. (b) Design of low pass filters for phase comparator I.

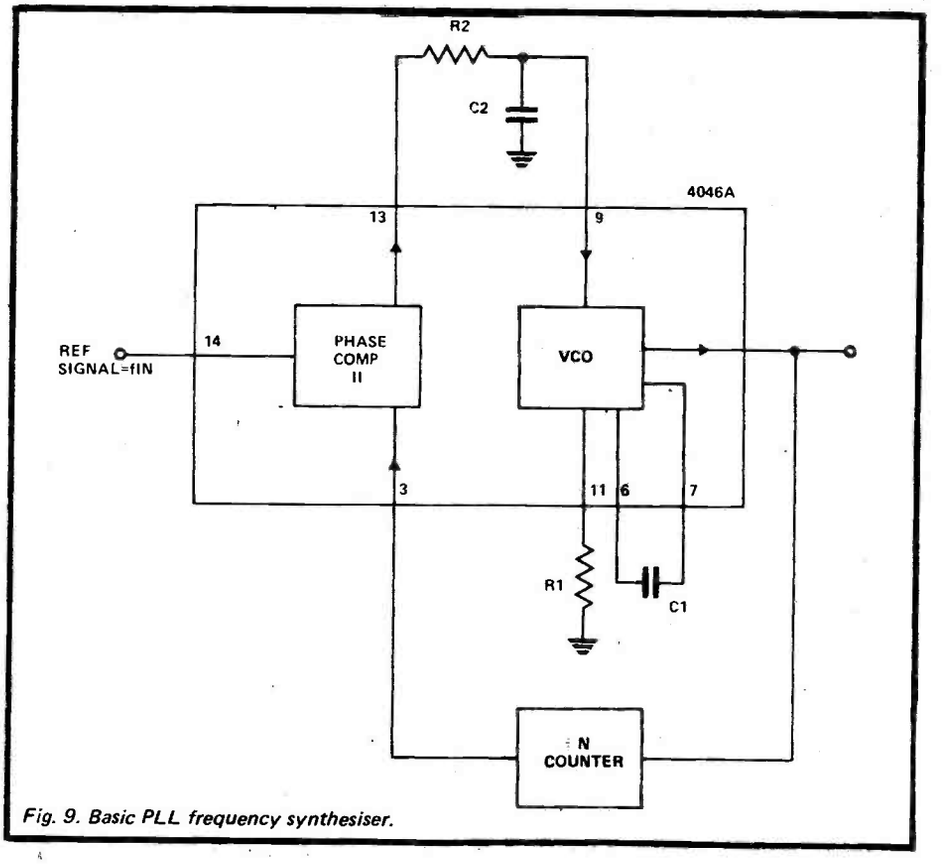


Fig. 9. Basic PLL frequency synthesiser.

CMOS Part 5

MULTI-STAGE COUNTERS

We will now begin a brief trip back through several of the topics we have already covered, looking at some more sophisticated IC's in each group.

The first two devices in fig. 1 share a common pin-out diagram. They are both dual counters (labelled "A" and "B") with reset operating when high. The 4518 operates in BCD and the 4520 works in binary. Both devices are capable of counting at at least 2.5MHz when V_{DD}= 10V. The clock and enable inputs are interchangeable in that a positive edge triggered counter may be realised by holding enable at "1" and using the clock input, or a negative edge triggered device may be obtained by holding the clock high and using the enable input.

The 4553 is altogether a more advanced I.C. It is a three stage decade counter with latches and it provides a multiplexed output. The counters advance on the trailing edge of the clock pulse providing that "disable" is low. It will also advance on the rising edge of a disable pulse if the clock is high. The outputs are multiplexed, which means that one digit is given at a time on the four BCD output lines. The three digit outputs show which digit is being presented (digit 1 is most significant). The BCD outputs are high when active, the digit select outputs are low. The multiplexing is driven by an internal oscillator whose frequency is determined by the value of capacitor (1000pF is about right) connected between pins 3 and 4. Alternatively, this can be overridden by leaving the capacitor out and driving the multiplexing by feeding pulses to pin 4. The carry out signal may be used to clock succeeding counters and in this case a capacitor may be used to control the multiplexing of the first counter and succeeding ones driven by connecting their pin 4 to pin 3 on the preceeding device. The reset input sets all the counters to zero and disables all the digit outputs hence blanking the display when it is taken high. The only other thing to note is the latch enable input. On the rising edge of the input to this pin the output from the counters is stored in latches and thus the conventional three decade counter ICs and three latch ICs are replaced by a single device. Use of this device is well illustrated by the ETI counter module and also by fig. 2 which shows a six decade version.

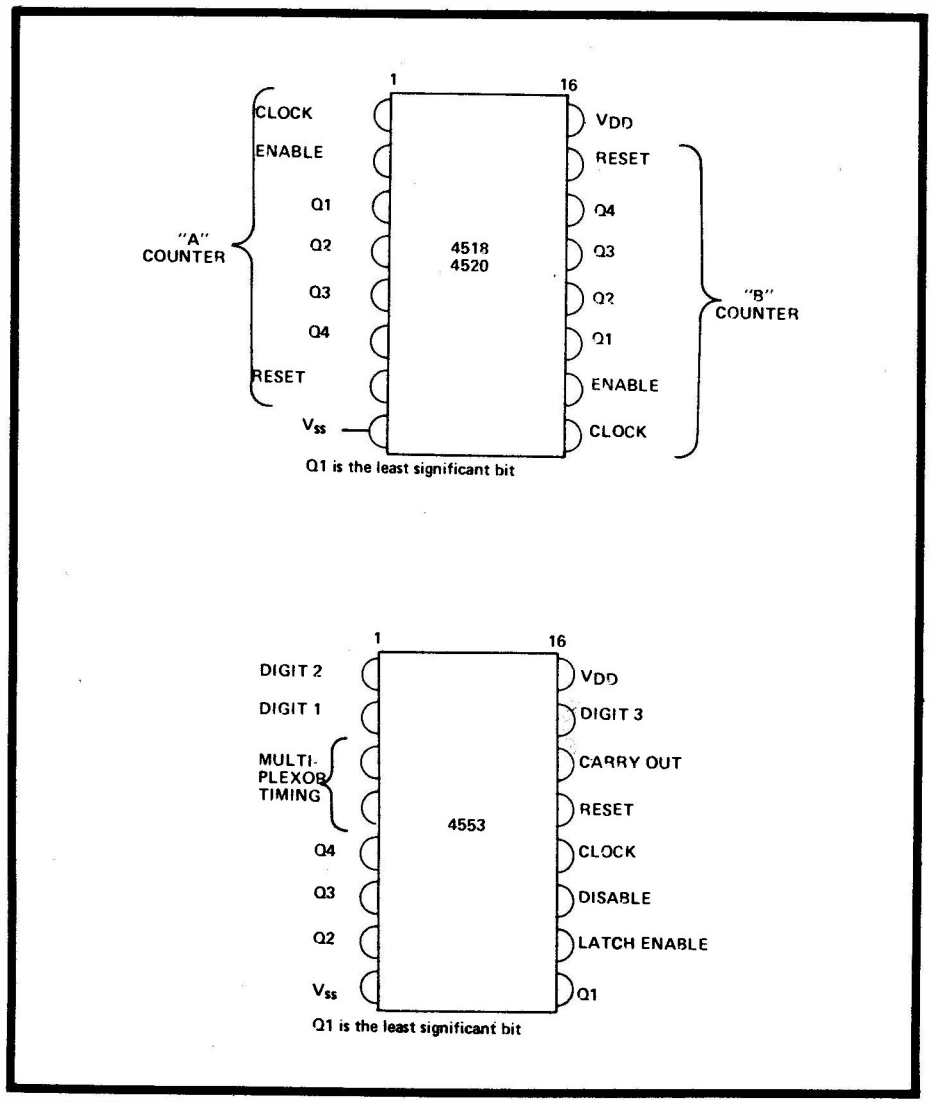


Fig. 1. Three multistage CMOS counters.

The two seven segment decoders used in these two counters, the 4543 and the 4511 have their pin-out given in fig. 3. The 4511 is a straightforward device with Q1-Q4 BCD inputs and a-g segment outputs. The three additional connections are simply a lamp test which lights all segments when it is taken low, a blanking input which turns off all segments when it is taken low (unless lamp test is low as well) and a latch which stores the current input when it is taken high. The segment outputs will source up to 25mA.

The 4543 is more advanced, the latch operates when taken low and the blanking operates when high. The device operates conventionally when the phase input is low (i.e. is suitable for directly driving common cathode L.E.D.s) but when phase is high, the outputs are all inverted which is useful for driving common anode L.E.D.s. If this input is fed

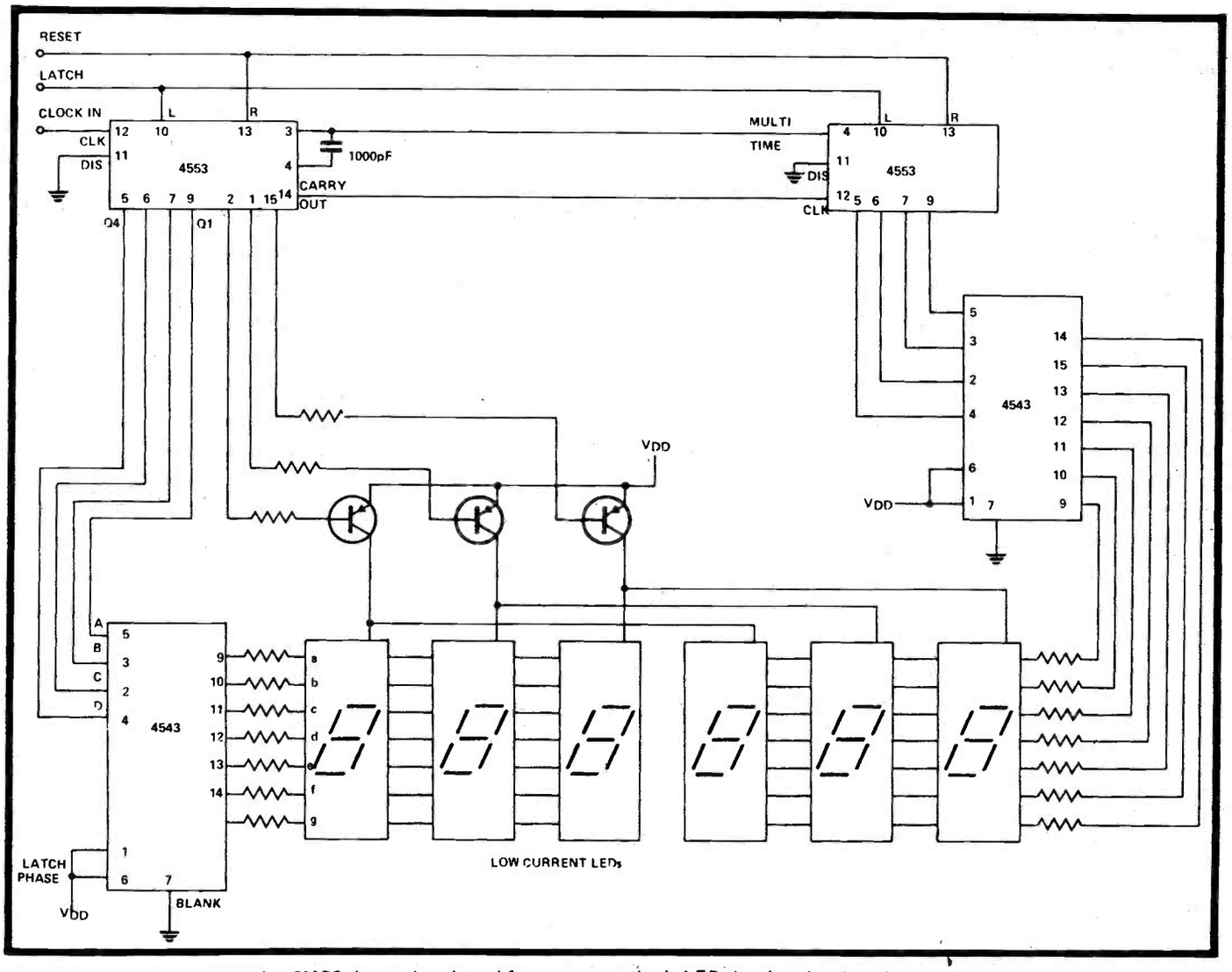


Fig. 2. A six decade counter using CMOS. It may be adapted for common cathode LEDs by changing the drivers and taking pin 6 on the 4543's to V_{ss}.

with a square wave which is also fed to the common connection of the segments, liquid crystal displays may be driven in the manner described in part one. The 4056A mentioned there is a pin for pin equivalent of this device except that the blanking is dispensed with and pin seven used as a second V_{ss} pin for the display output part of the circuitry. Thus pin 16 could be at OV, pin 8 at —3V and pin 7 at —15V giving maximum economy while still providing full drive at the output.

There is also a five decade counter of a similar type but there is not space to describe it here. Its type number is 4534 and it comes in a twenty-four pin DIL case.

MONOSTABLE MULTIVIBRATOR

The 4098B is a dual monostable multivibrator. Its pin diagram in fig. 4 is accompanied by a table showing the connections needed for every combination of edge triggering and retriggerability. The reset operates when low in this device whose period is, to a first approximation given by T=RC (ohms and Furads), where C is connected getween the RC and C pins and R is connected from RC to V_{DD}. The specification of the 4528 is similar except for minor details.

MORE GATES

We can now claim to have covered a fair cross-section of devices and so to conclude we shall say a little more on the subject which we started with, simple gates. As well as the NOR and NAND gates we mentioned at the time there is a range of AND and OR gates available at comparable prices. The 4071B, 4075B, 4072B are quad, triple and dual OR gates respectively with identical connections to the NOR gates (4001A, 4025A, 4002A) that were discussed in the first part. Similarly, the 4081B, 4085B, 4082B are the AND gates corresponding to the 4011A, 4023A, 4012A we mentioned then.

The 4030A quad exclusive-OR gate was also listed there and it is worth mentioning that types 4070B and 4077B are exclusive-OR and exclusive-NOR gates with identical pin connections. As the 4070B has slightly superior specification to the 4030A and is usually cheaper it may generally replace it. Also, for almost all purposes the 4507 is equivalent to the 4030A and 4070B.

The 4093B is a quad NAND Schmitt trigger with about 0.6 volts hysteresis (at V_{DD}= 5V) and a pin-out identical to the 4001A. The 4583 is a dual Schmitt trigger in which the hysteresis may be adjusted by

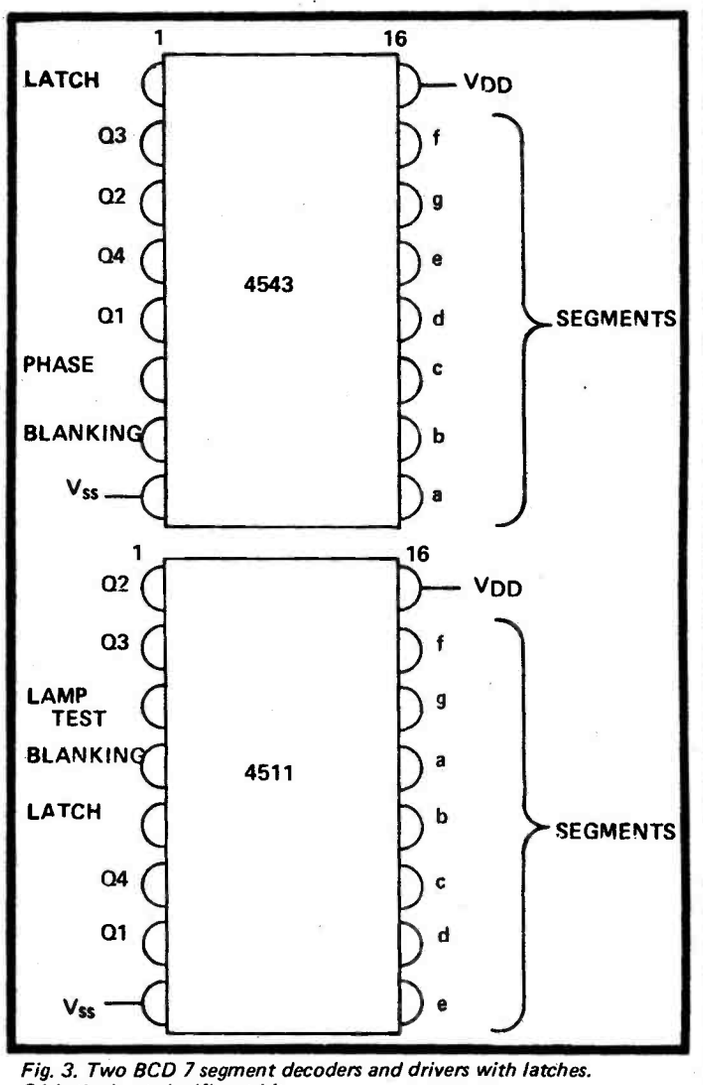
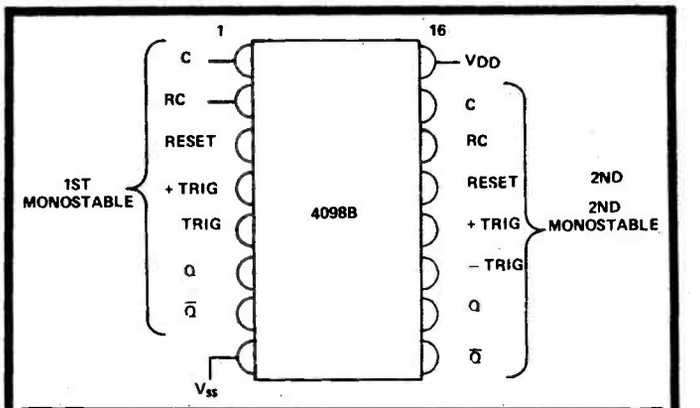


Fig. 3. Two BCD 7 segment decoders and drivers with latches. Q1 is the least significant bit.



MODE OF OPERATION	CONNECT TO VDD	CONNECT TO Vss	INPUT PULSE TO	OTHER CONNECTIONS
+EDGE TRIG RETRIG	–TRIG RESET	–	+TRIG	–
+EDGE TRIG NON-RETRIG	RESET	–	+TRIG	–TRIG TO Q̄
+EDGE TRIG RETRIG	RESET	+TRIG	–TRIG	–
–EDGE TRIG NON-RETRIG	RESET	–	–TRIG	+TRIG
UNUSED SECTION	–TRIG	RESET +TRIG	–	–

Fig. 4. The 4098B dual monostable multivibrator and method of achieving different modes of operation.

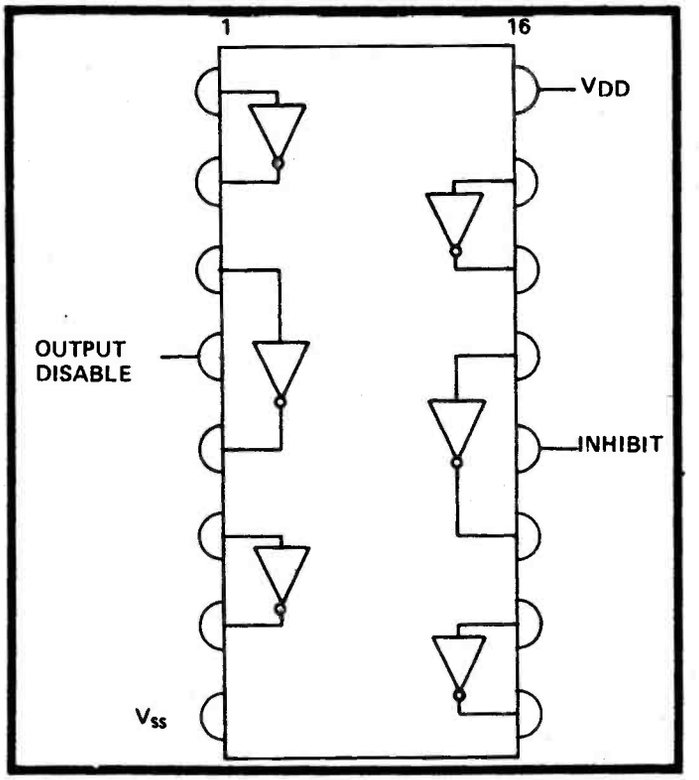


Fig. 5. Pinout of the 4502 strobed hex inverting buffer.

external resistors. There can be few uses for these which have not already been realised with the T.T.L. SN7413N but it is worth noting that larger time constants could be used on the inputs.

Fig. 5 shows a hexinverter and buffer with the extra options of an inhibit input which makes all the inverters have low outputs when it is taken high and an output disable which sets all the outputs in a high impedence state. This also operates when it is taken high. The chief use of these circuits is in applying one of two lines of data to an input. They are both wired in but only one disable is low at any one time. The disable overrides the inhibit.

RANGES OF CMOS

Throughout this article, devices have been known by a four digit code number beginning 40 and ending with A or B, or beginning 45 and possessing no suffix. Most of the devices beginning 40 are available from RCA in the CD range with a type number CD40xxAE or CD40xxBE. The A signifies that the maximum supply voltage is 15v, B signifies 18v. In general, A and B versions are not both provided. Most of this range is also available from Motorola as the MC140xxCP range which will tolerate up to sixteen volts. The 45 devices are often available only in the MC145xxCP range. In general other combinations of suffices indicate a ceramic packages or the like. Generally these are more expensive and have slightly superior specifications. ●

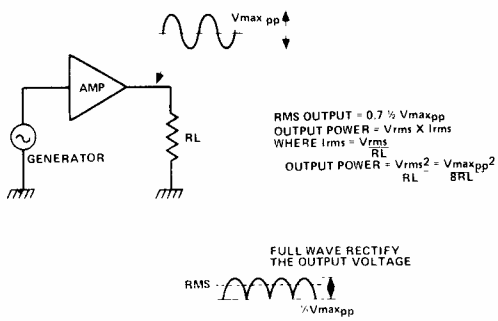
AUDIO AMPLIFIERS

Designing an amplifier is like re-inventing the wheel. There are thousands of published designs and possibly as many as a 100 different types of monolithic amplifiers as well as lots of off the shelf modules to choose from. If you design the amplifier yourself (or use someone elses design) you will probably encounter problems such as heat, noise, instability, distortion, power rating etc, etc. Tim Orr sets out to help you cope.

Power Rating

The power rating for an amplifier is *generally* considered to be the maximum RMS power that a sine wave can deliver to a load (Fig. 1). The RMS power is given by:

$$P_{(RMS)} = \frac{V_{pp}^2}{8RL}$$



Therefore if RL=8R and Vpp is 1V, $pP_{(RMS)}$ = 15.6mW.

For V_{pp} = 10 V $P_{(RMS)}$ = 1.56 W.
For V_{pp} = 100 V $P_{(RMS)}$ = 156 W.

So the RMS power goes up as a square of the output voltage. However our hearing does not respond linearly to power, and so the difference between a 10 W and 100 W amplifier is always disappointing.

Heat

Not surprisingly, power amplifiers get hot. When they are delivering power to a load, the amplifier is also dissapating a considerable amount of heat itself. A reasonable rule of thumb is that both the amplifier and the load dissipate the same power, except when there is no output signal. Then the amplifier is the only thing that is getting hot. To get a very low crossover distortion it is usually necessary to run the output transistors in an amplifier in class A or AB. This means that the transistors are biased on (or partly on for AB operation). Thus they consume lots of current and get hot. Therefore designing power amplifiers is a compromise between heat production and distortion. IC power amplifiers, because of their small size, go for low heat generation and hence higher crossover distortion. Discrete component power amplifiers can use large heat sinks sometimes with forced air cooling and thus obtain THD figures from 0.1% to 0.01%.

Some IC power amplifiers get rid of their heat down the IC legs to suitably large areas of copper on the printed circuit board. There are also 'Stick On' heat sinks dor DIL packages. Also, when the going gets a bit hot some amplifiers employ a thermal shutdown mechanism. Generally though, high temperature operation means that the device life time is greatly shortened. Thus it is not surprising that the components that fail most regularly are the power transistors in amplifiers and power supplies.

Stability

The only difference between amplifiers and oscillators is the phase of the feedback and so it is hardly surprising that a problem exists. When the phase of the feedback becomes positive then oscillation can occur, if the gain of the amplifier is then greater than unity. The gap between a good amplifier and an oscillator is known as the phase margin. When the phase margin is reduced to zero, oscillations will occur.

More feedback when the phase shift is positive will increase the risk of instability. Less feedback when the phase shift is positive will make the amplifier more stable.

However, less negative feedback means more distortion. It is a compromise between stability and distortion. It is possible to increase the phase margin and thus stabilise the amplifier with a suitably placed capacitor. However, in the IC (monolithic) design this is not possible because this capacitor would probably occupy

twice the area as the rest of the integrated circuit. So, the designers of IC power amplifiers usually make this stabilising capacitor small and set the amplifier gain high (less negative feedback).

You end up with a power amplifier that is only stable with high values of gain and which has a relatively high distortion. Even so, most monolithic designs need additional capacitors on their inputs and their outputs to maintain stable operation. Other stability problems are:

1) Amplifier gain and phase margin depend on power supply voltages. Thus, an amplifier may not be stable under varying conditions of supply voltage. During the power up, the amplifier may emit a squeak or a whoosh, due to high frequency instability.

2) Amplifier gain and phase margin depend on temperature. Thus as the amplifier warms up it may then become unstable, oscillate, the output transistors get very hot and the amplifier burn out.

Alternatively, the amplifier may be unstable only when cold. So you switch on and it squeaks (oscillates), warms up, stops oscillating, cools down, oscillates (squeaks), warms up, etc. etc. (Breaks the ice at parties!).

3) The load put on an amplifier will affect the phase margin. Designing an amplifier that will drive any load is difficult. Often a power amplifier will have a capacitor resistor network from its output to ground. This network is used to increase the phase margin.

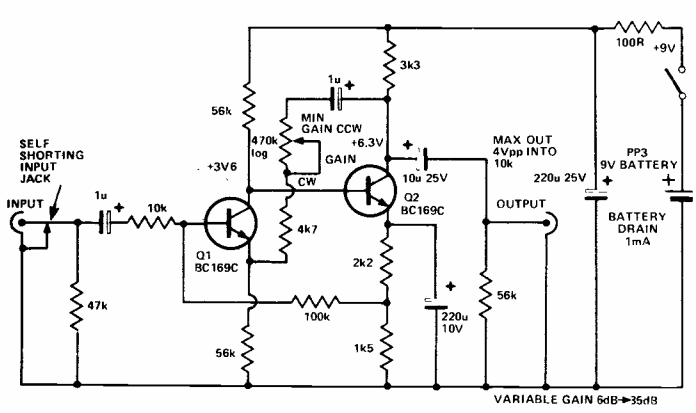
Distortion

If you put a pure sinewave into an amplifier and you get out of it the same sinewave plus some harmonics, then you have got distortion. Any other spurious signals are not distortion products and are not included in the THD calculations.

Crossover distortion is usually generated by the output transistor pair (Fig. 2). This is caused by one of the transistors switching off before the other one can switch on. The result is a 'lump' in the output waveform which gives the sound a 'buzzy' quality. The distortion can be reduced by turning the output transistors on a bit more, by biasing their bases further apart. This increases the quiescent current and thus more power is dissipated: Also, overall negative feedback can be used to iron out the kinks, but this will increase the chance of instability.

Another type of distortion is harmonic distortion. An amplifier, used in open loop is usually fairly non linear. This non-linearity will cause any signal passing through the amplifier to be distorted. Negative feedback is used to iron out the non-linearities and so reduce this source of harmonic distortion.

It is interesting to note that the hi-fi market wants low THD figures of 0.1% to 0.01% but the music market actually prefers (in some cases) higher figures of about 2%.

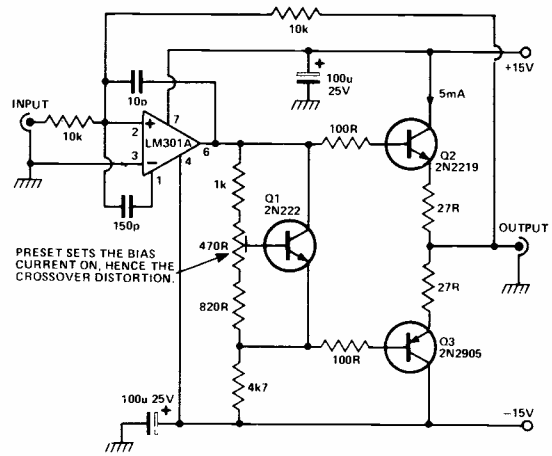


Mains hum is easily picked up with high impedance microphones, particularly if the microphone cable is long. Also, a treble cut occurs when using long cables. The output impedance of the microphone and the capacitance of the cable produces a low pass filter which cuts off the high frequencies, so that a high impedance microphone should only be used on a short cable.

For low impedance types, a low-noise high gain amplifier is needed, as output is much lower, and the circuit above is such an amplifier. The noise generated by transistors is a function of collector current. The current through Q1 has been optimised to give low noise operation.

The amplifier has an open loop gain of more than 60 dB. Negative feedback is applied, via a variable 470k pot, so that the closed loop gain is controllable from 6 dB to 35 dB. This allows the gain to be tailored to suit different types of microphone and hence get the best overload and S/N ratio conditions. A maximum signal output of 4 V into a 10k load is obtained and the current drain is 1 mA making it possible to run the amplifier from a PP3 9 V battery.

Unbalanced Line Driver



The high open loop gain of an op amp is combined with the power handling capabilities of descrete transistors to produce a line driver amplifier. The output driver stage (Q1, 2, 3) is included in the overall feedback, and acts as a power booster on the output of the op amp. Transistor Q1 is used as a VB_{BE} multiplier. That is, it sets up a voltage of about 1 V5 between its collector and emitter. The actual voltage can be set by the preset connected to its base. Thus the bases of Q2 and Q3 can be biased apart by a set amount, just sufficient to make them work in class B operation.

If there are any ambient temperature changes, Q1 automatically adjusts the bias voltages to Q2,3 to maintain a constant bias current. There is overall negative feedback from the output, providing a voltage gain of 0 dB (x1). The output is partly short circuit protected by the 27 ohm emitter resistors. This amplifier can deliver high level, low distortion signals into low impedance loads. It could be used as an output driver in an unbalanced audio mixer.

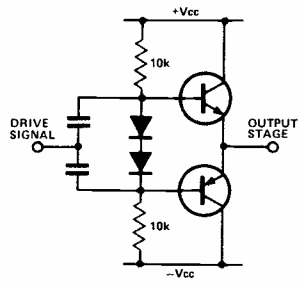
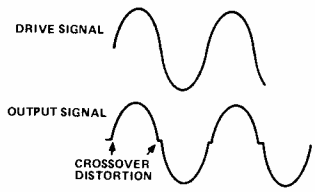


Fig 1 (above) is the classical output pair that produces the equally classical crossover distortion illustrated below. Careful biasing of the output pair can reduce the effect but it is usually present in most amplifiers of this type.



Noise

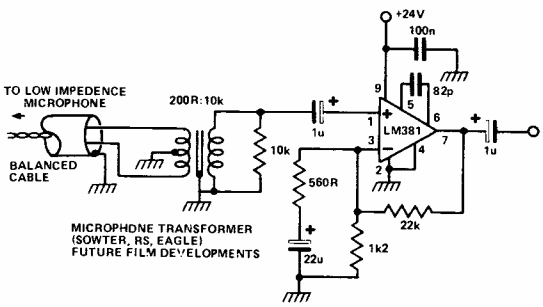
Noise is generally not a problem in power amplifiers but it is in the pre-amplifier stages of an audio system. An overall system signal to noise ratio of 70 dB (3 000 to 1), is quite good and not very difficult to achieve. Better than this is studio or professional quality. When amplifiers are used to reproduce stored signals, such as from a disc, radio or tape recorder, then an overall S/N ratio of 70dB is quite adequate. This is because the S/N ratio for these storage or transistor systems is quite low.

For example the best disc technology will only give us a 60 dB S/N ratio. The best studio quality tape recorder (unprocessed), will give 65 dB. Radio transmissions are about 50 dB on FM, and cheap cassette players only clock up 30 dB's.

As tapes and discs are used then their S/N ratio deteriorates. Also, most listening environments have a high background noise level (air conditioning, street noise, jets etc.).

The most demanding situations where the noise of a preamplifier will be important are in amplifying the signals from low impedance microphones, magnetic cartridges for record players and tape recorder pickup heads. In the following sections there are several examples of low noise pre-amplifier designs.

Balanced Microphone Preamplifier

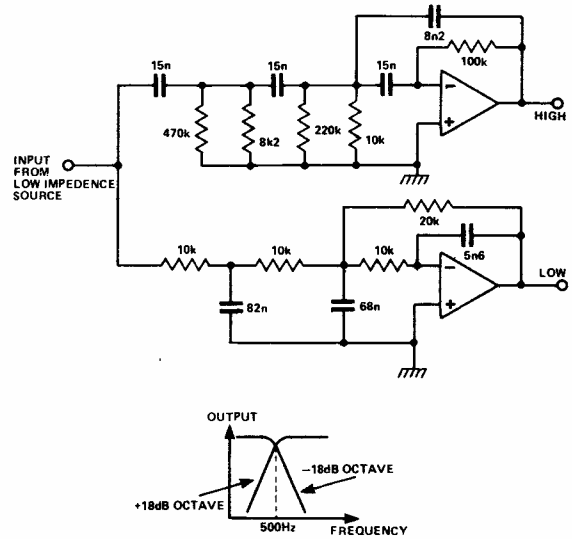


Professional audio equipment generally uses balanced inputs and outputs. This means that the inputs and outputs are differential, which is usually obtained by having balancing input and output transformers.

The advantage of using a balanced system is that any unit can be connected to any other unit without any ground loop problems. A balanced system eliminates these problems. Also, mains hum pick up is reduced. A balanced audio cable has an outer screen and a twisted pair of wires in the centre. Any mains hum (or other signal) which is picked up on the twisted pair will have the same amplitude on each of these central wires. This is a common mode signal. The microphone signal applied to these two wires is a differential signal. Thus, when the microphone signal plus mains hum is connected to the transformer, the differential signal appears at the output windings and the common mode signal is rejected. Thus the mains hum is suppressed.

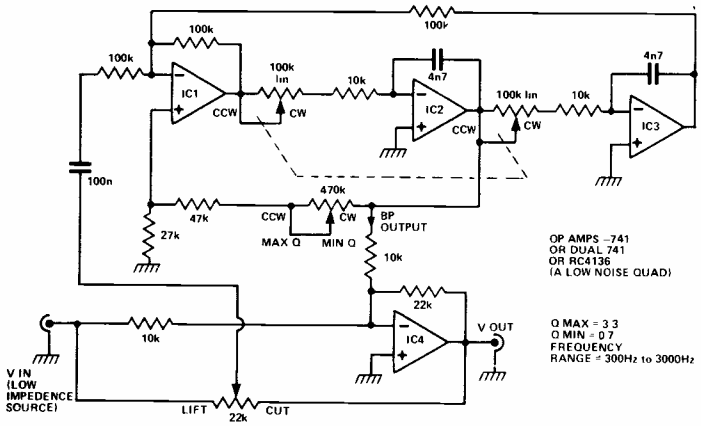
The transformer also provides a voltage gain, and the LM 381 provides a low noise amplification of about 32 dB (x40).

Active Crossover Unit



The circuit shown is for a two speaker system having a crossover frequency of 500 Hz. The filter structures are third order Butterworth multiple feedback, low pass and high pass. (Third order implies that roll off slopes of ±18 dB/octave are obtained.)

Parametric Equaliser

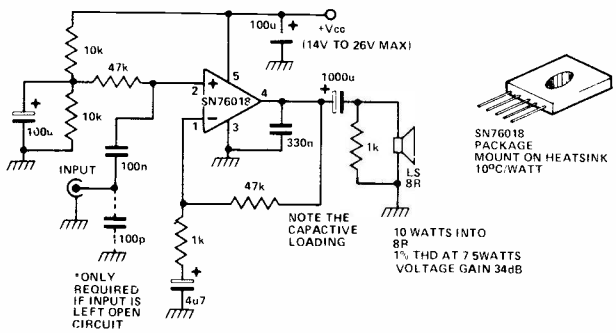


This is possibly the equaliser for the amplifier system that has everything. The parametric equaliser has got three controls. It is a bandpass filter which can have variable cut or lift, so that a particular frequency band can be enhanced or rejected. The resonance can also be controlled so that area of frequency affected can be broad or narrow. Also the centre frequency of the bandpass filter can be varied so that it can be tuned to operate at a particular frequency. The circuit operation is quite simple.

Op amps IC 1, 2, 3 form a state variable filter, the Q and centre frequency of which can be varied. Op amp IC4 is a virtual earth amplifier. When the equaliser is in the lift position, the signal is fed into the state variable filter. It then comes out of the bandpass output and into IC4. In this feed forward position the equaliser has got a peak (lift) in its response. When the equaliser is in its cut position, the bandpass filter is in the feedback loop of IC4 and so there is a notch in the frequency response.

Care must be taken not to cause overloading and clipping when using high Q lifts.

10 Watt Power Amplifier. (SN6018)



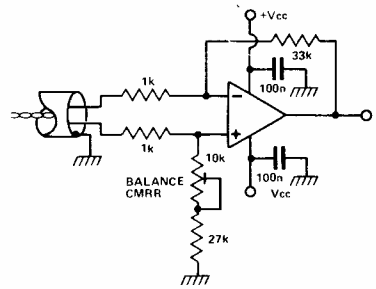
This is a very simple and inexpensive monolithic power amplifier made by Texas Instruments. It comes in a package that looks like a plastic power transistor with five legs.

Thus it can be screwed down to a heat sink without any problems. The THD specifications for this device are:

10 W at 10% THD (R1 = 8 ohm)
7.5 W at 1% THD (R1 = 8ohm)
0.05 W to 6.5 Watt at 0.2% THD (RL = 8ohm)

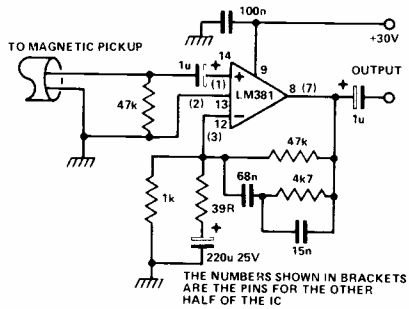
No isolation from the heat sink is required. It should be used in applications where high fidelity is not required. Note that it requires two stabilising capacitors.

Electronic Balanced Input Microphone Amplifier.



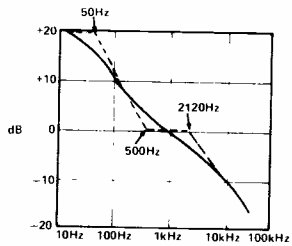
It is possible to simulate the balanced performance of a transformer electronically with a differential amplifier. By adjusting the presets the resistor ratior can be balanced so that the best CMRR is obtained. It is possible to get a better CMRR than the one you would obtain from a transformer. Also, a transformer can itself pick up mains hum, it is expensive and heavy. So, electronic balancing can be quite competitive. One problem is obtaining a truly differential low noise amplifier. I would suggest a RC4136 which is a quad low noise op amp.

Record Player — Magnetic Pickup



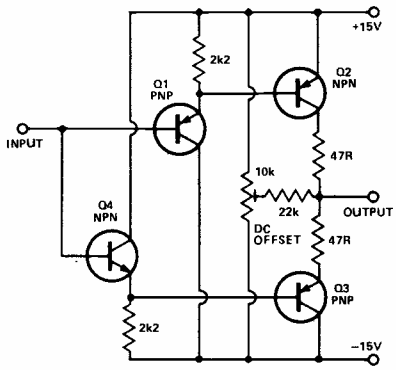
If you were to amplify the signal from a magnetic pickup on a record player and listen to it the sound would be terrible. It would be all treble and no bass. This is because the pickup is magnetic and gives an output voltage which is velocity sensitive. That is the faster the needle wiggles in the record groove, the larger the output voltage, or rather the output voltage (for the same amplitude of excursion) is proportional to frequency. To restore the natural sound, the signal must be equalised with a frequency response as specified by the RIAA.

This play back equalisation gives 20 dB lift at low frequencies and 20 dB attenuation at high frequencies and is 0 dB at 1 kHz. No equalisation is required if you use one of the cheaper ceramic pickups, which have a flat response.



Graph illustrating the non-ideal approximation to the ideal RIAA equalisation curve, the response flows smoothly unlike the 'defined' RIAA response.

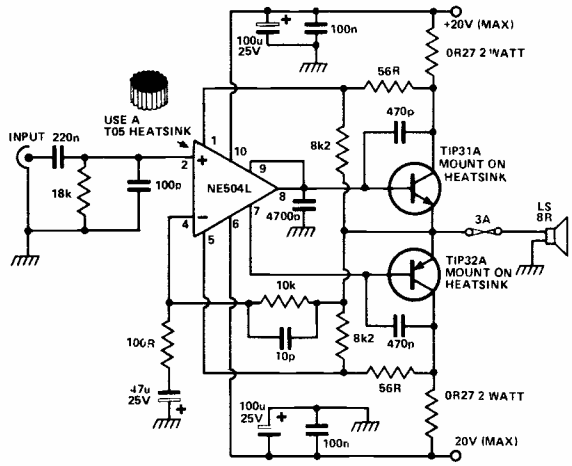
50 Ohm Driver



When you want to buffer a test generator to the outside world it is often very difficult to get an amplifier with sufficient bandwidth and power handling to do the job. The circuit is a very simple unity gain buffer. It has a fairly high input impedance, a 50 ohm output impedance, a wide bandwidth and high slew rate.

The circuit is simply two pairs of emitter followers. The base emitter voltages of Q1 and Q2 cancel out, and so do those of Q3 and Q4. The preset is used to zero out any small DC offsets due to mismatching in the transistors.

20 Watt Amplifier



An audio power amplifier can be constructed from a power driver op amp plus a pair of transistors. The power driver is a NE540 made by Signetics. It generates quite a bit of internal heat and so a TO5 heat sink is required. Note that this design uses five stabilising capacitors.

The amplifier works quite well once any stability problems have been sorted out and the power output is quite adequate for a domestic amplifier system.

POWER SUPPLIES

This series of articles by B. Doherty outlines the operation, performance, limitations and design aspects of the modern dc power supply.

The usual first stage in a dc power supply is the transformer which converts the ac at mains voltage to the (usually) lower voltage required for semi-conductor circuits. The transformer also isolates the circuit from the ac mains (Fig. 1).

The output of the transformer is still ac, so a rectifier is required to convert this to dc. (Fig. 2).

The dc output is, however, a fluctuating direct current, so a smoothing, or filter, circuit is required. (Fig. 3).

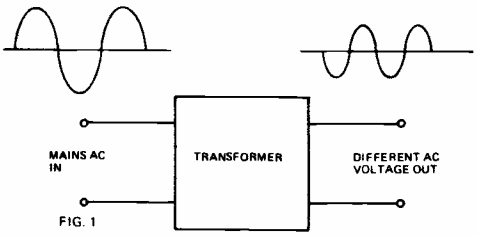


FIG. 1

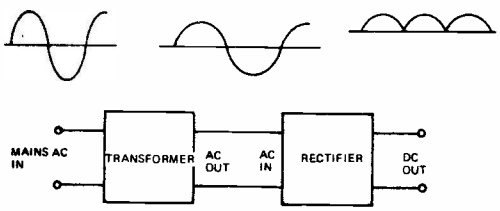


FIG. 2

This provides an almost steady dc, there remaining only the problem of being sure that the supply maintains a steady flow of power and does not allow fluctuations. For this, a control circuit is added to counteract fluctuations in supply or load.

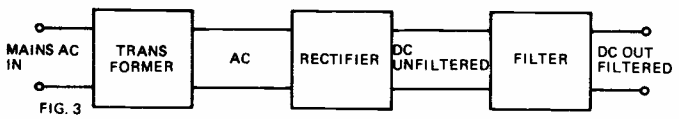


FIG. 3

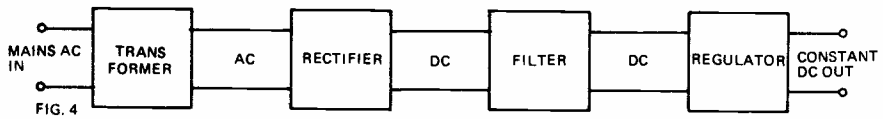
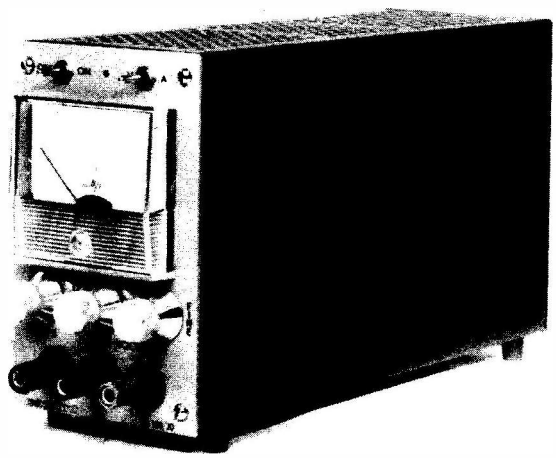


FIG. 4



Constant voltage power supply with variable current limiting and one meter to read both voltage and current (Coutant)

The block schematic of a complete power supply is shown in Fig. 4.

Power supplies may be required to supply either constant voltage or constant current.

A constant voltage power supply acts to maintain its output voltage constant, in spite of changes in load, line, temperature, etc. Thus for a change in load resistance, the output voltage of this type of supply remains constant while the output current changes by whatever amount is necessary to accomplish this.

A constant current power supply on the other hand, acts to maintain its output current constant in spite of changes in load, line and temperature. And thus for a change in load resistance, the output current remains constant while the output voltage changes by whatever amount is necessary to accomplish this.

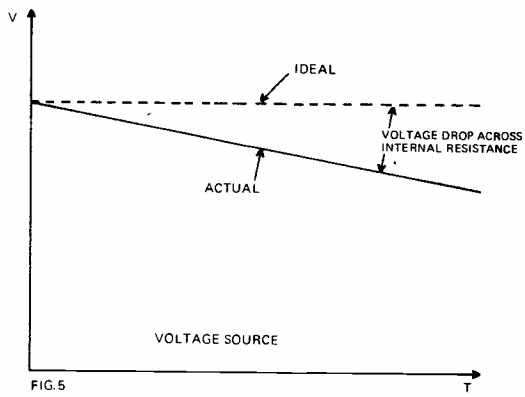


FIG.5

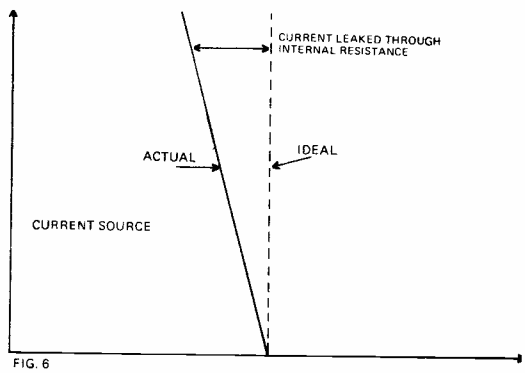


FIG. 6

The differences between the two types of power unit are shown graphically in Figs. 5 and 6.

The internal resistance of an ideal voltage source will be zero, so that there is no voltage drop across the internal resistance, and the internal resistance of an ideal current generator will be infinite, so that there is no current lost internally. This is perhaps clearer if we look at the circuit of practical voltage and current generators (Figs. 7 and 8).

In both cases the actual source consists of an ideal source (Fig. 7) with an internal resistor connected so as to introduce an imperfection before the terminals (Fig. 8).

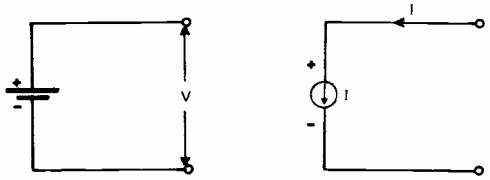


FIG. 7

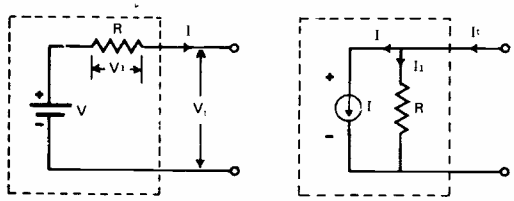


FIG. 8

THE TRANSFORMER

The transformer (Fig. 9) operates by creating a magnetic flux (ϕ) in the iron core by passing a current into the primary, then the passage of the magnetic flux through the secondary generates a voltage in the secondary (Faraday's law).

Note that the coupling between the primary and the secondary is magnetic only — there is no electrical coupling.

The ratio of primary and secondary quantities is determined by the turns ratio. Thus

$$\frac{V_2}{V_1} = \frac{N_2}{N_1}$$

$$\frac{I_2}{I_1} = \frac{N_1}{N_2}$$

Theoretically there is no power loss in the transformer, so the principle of conservation of energy, requires that the input power is equal to the output power

so $P_1 = P_2$

i.e. $V_1 I_1 = V_2 I_2$

It is from this product of $V_1 I_2 (= V_2 I_1)$ that the volts/amps of a transformer is derived.

In practice of course, there are losses in the transformer which mean that the power in the secondary is less than the power in the primary.

The relation between primary current and magnetic flux is as shown in Fig. 10.

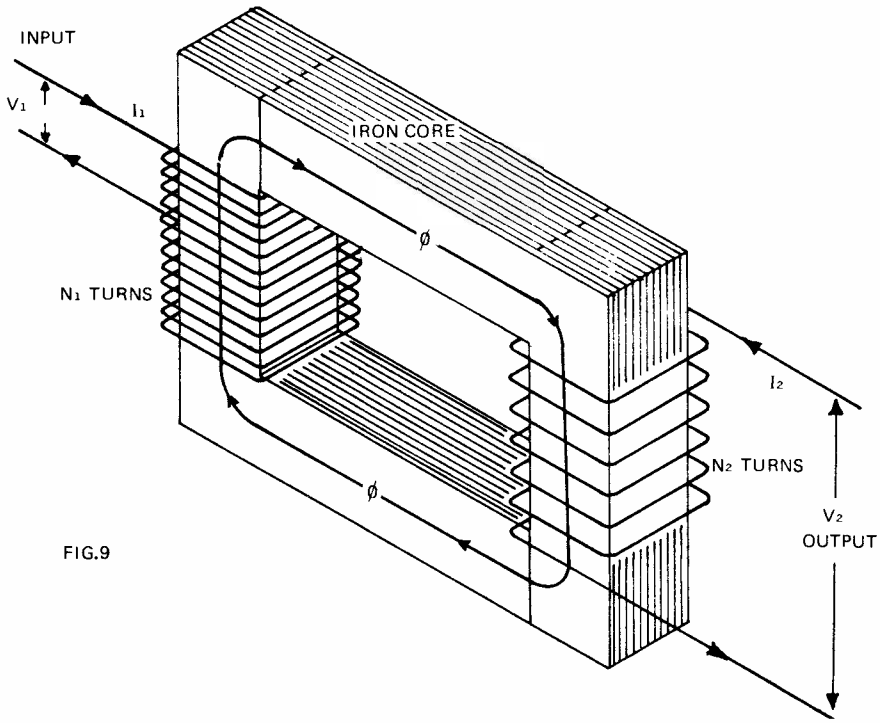


FIG.9

Note that the relation is linear from 0 to A, but after A no matter how much the current is increased the flux remains approximately the same. This phenomenon is called *saturation* (of the iron core) and occurs when the great majority of the magnetic dipoles in the iron have been aligned with the flux.

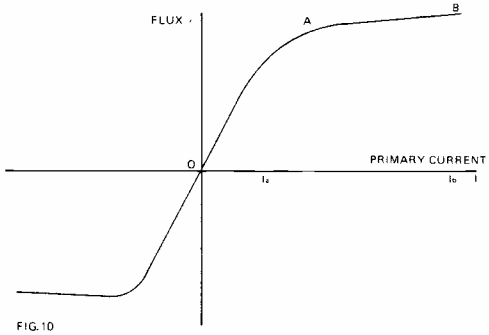


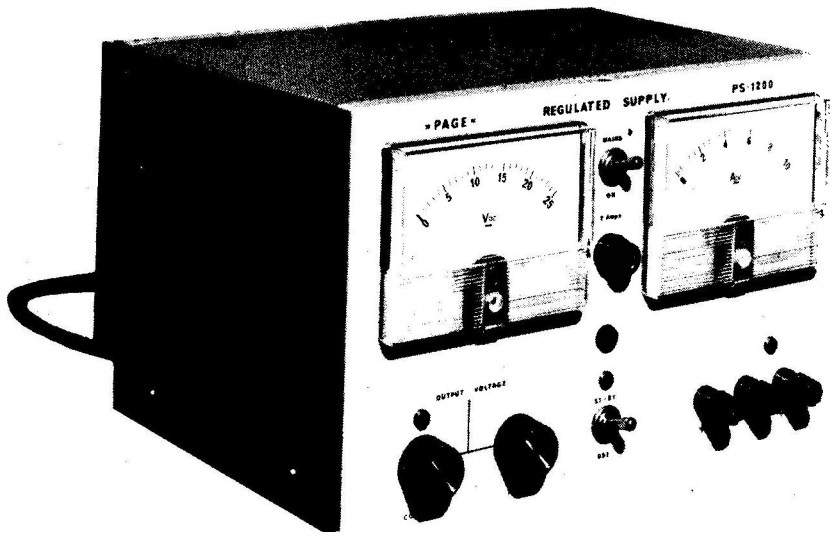
FIG.10

The segment AB is called the saturation region.

If the primary current is derived from the ac mains it will have a sinusoidal waveform. If the peak of the sinusoid is less than I_A, the flux produced will be an exact replica of the input current, because as current goes up, flux goes up and vice versa.

The secondary voltage will be approximately proportional to the flux, and will therefore also be sinusoidal.

There is however a renewal of interest in the type of transformer where the peak of the primary current moves well into the saturation region. In this type of transformer the peak primary current is I_B. The flux varies directly with primary current until A is reached, then it remains approximately constant over AB as the sinusoid rises to a peak then falls.



This regulated power supply provides outputs adjustable from 9 to 16 volts at currents of up to 15 amps.

When the primary current falls below A, the flux once again varies directly with primary current. The flux waveform is then as shown in Fig. 11, and since the secondary voltage is roughly proportional to the flux, the secondary voltage is as illustrated in Fig. 12.

(Note that transformers must be specially designed to operate in this mode.)

DIODES

The voltage/current graph for a typical diode is shown in Fig. 13. When a positive voltage is applied, the current is high and the forward voltage drop is less than 1 volt. When a negative voltage is applied, a negligible current flows.

The diode is eminently suitable for use as a rectifier because of its ability to pass current only in one direction.

BASIC RECTIFIER CIRCUITS

The simplest possible rectifier circuit is shown in Fig. 14.

The diode will pass only the positive half cycle of the secondary ac voltage, so the voltage across the load is as shown in Fig. 15. The output is a fluctuating direct current (since it moves always in the positive direction).

The circuit shown in Fig. 14 is a half-wave rectifier. As a source of direct current it is not very effective because of the large voltage fluctuations. The full-wave rectifier is a substantial improvement.

The two most common types of full-wave rectifier are the centre tapped (Fig. 16) and the bridge (Fig. 18) configurations.

The full-wave centre tapped secondary configuration is shown in Figs. 16 and 16a. On the positive half-cycle A is at +V, B at 0V, and C is at -V. Thus A is more positive than B, and diode D1 conducts via the load in the direction shown. Diode D2 has a negative voltage across it and does not conduct.

On the negative half-cycle, A is at -V, B is at 0V, and C at +V. Thus C is more positive than B_1, so diode D_2 conducts via the load in the direction shown. Note that it conducts in the same direction as did D_1. Diode D_1 now has a negative voltage across it and does not conduct.

The voltage applied to the load is therefore as shown in Fig. 17. The fluctuation is much less with this waveform. (Half as much as with the half-wave configuration.)

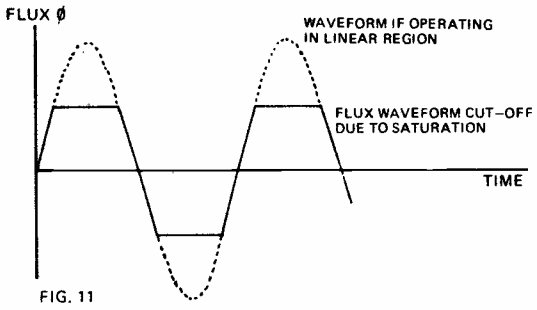


FIG. 11

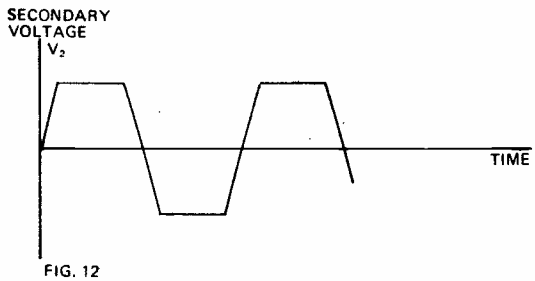


FIG. 12

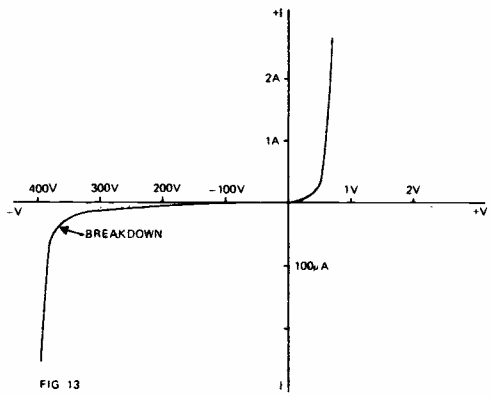


FIG 13

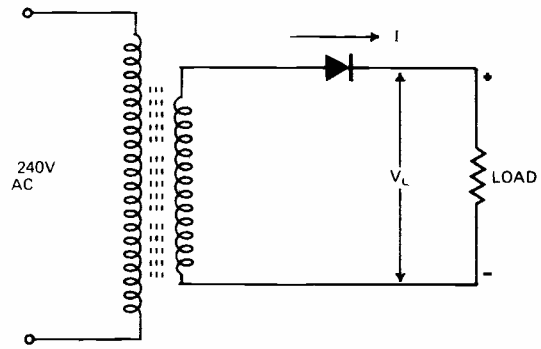


FIG. 14

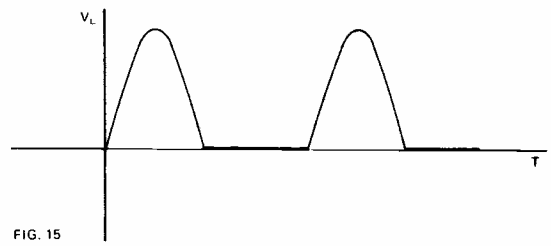


FIG. 15

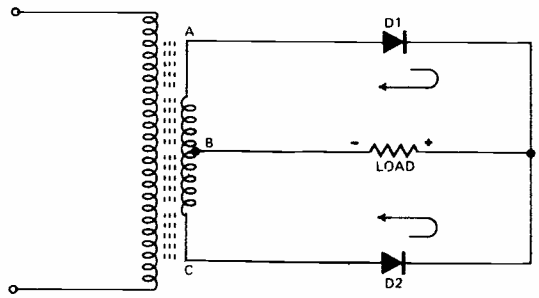


FIG. 16

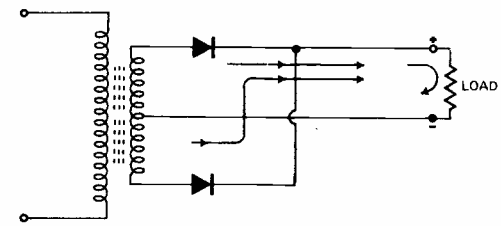


FIG.16A

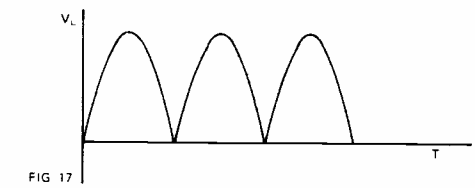


FIG 17

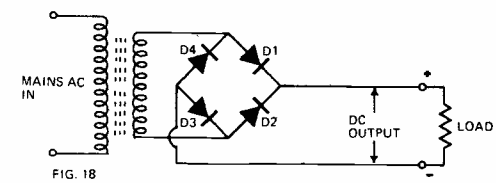


FIG. 18

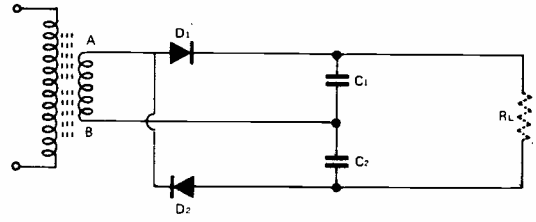


FIG.19

THE BRIDGE RECTIFIER

The second common type of rectifier is the bridge rectifier. (Fig. 18).

During the positive half-cycle, current flows from A to B through D1, through the load, and through D3. During the negative half-cycle, current flows from B to A through D2, *through the load in the same direction as before* and through D4.

The voltage applied to the load is, therefore, the same as in the centre-tapped circuit shown in Fig. 16 above.

VOLTAGE DOUBLERS

Another type of rectifier-filter commonly used in low power applications where the load is relatively constant is the voltage doubler (Fig. 19).

When A is at +V and B is at 0V, diode D1 conducts and charges C1 up to the peak of the ac voltage. Diode D2 has a negative voltage across it and does not conduct. When A is at -V and B is at 0V, diode D2 conducts and charges C2 to -V peak. Diode D1 has negative voltage across it and does not conduct.

Since capacitors C1 and C2 are in series, the voltage across them (off load) is twice the total peak ac voltage, hence the term voltage doubler.

When a load is applied to the voltage doubler circuit, the output voltage will be less than twice the peak voltage. The actual voltage will depend on the value of the capacitor and the load current drawn from the circuit.

VOLTAGE MULTIPLIERS

The voltage multiplier shown in Fig. 20 produces high voltage at lower power levels.

Off load, the output voltage of this configuration is twice the peak ac voltage multiplied by the number of stages used. Both diodes and capacitors must be rated as twice the peak ac input voltage.

DIODE SELECTION

The important factors in selecting suitable diodes are the current they must carry, both peak and average,

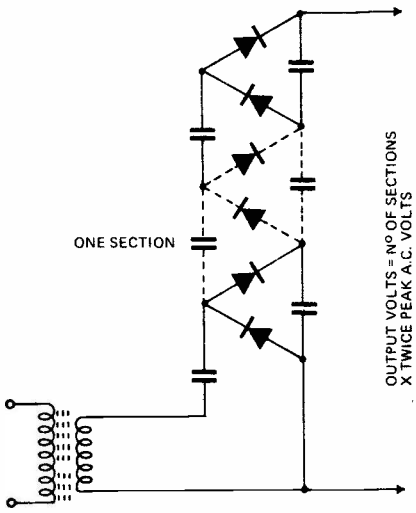


FIG.20 VOLTAGE MULTIPLIER

and the negative voltage which will appear across them when they are non-conducting. If the permissible maximum currents (as determined from the manufacturers' specifications) are exceeded for even a short time the diode will be destroyed, and if the negative voltage exceeds the Peak Inverse Voltage (P.I.V. – once again found from manufacturers' specifications) the diode will probably be destroyed by avalanche breakdown.

In the half-wave circuit the single diode must carry the full current and the full secondary voltage (the *peak*, not the rms which is normally specified at the secondary). For a sinusoid, the peak voltage = rms voltage x $\sqrt{2}$. If capacitors are used to filter the output, the diodes must be rated at twice peak voltage.

In the centre-tapped secondary or circuit, the voltage of the transformer is usually quoted as half the total voltage – 0 – half the total voltage; thus if the total output voltage is 650V, the transformer specification will be 825-0-325 volts.

The diodes must be rated for the peak of the *total* output voltage, and half the output current.

In the bridge rectifier the diodes are rated for the peak of the ac voltage and half of the full amount.

FILTER CIRCUITS FOR POWER SUPPLIES

A full-wave rectifier output may be shown to be equal to a constant voltage *plus* an alternating voltage, by the use of a Fourier series. Thus the output voltage is expressed by

$$V_o = \frac{2}{\pi} V_m + \frac{4}{3\pi} \cos 2wt + \text{negligible terms}$$

where Vo is the rectifier output voltage

V_m is the peak rectifier output voltage

w = $2\pi f = 2\pi \times 50$ Hz is the supply frequency in radian/sec.

The purpose of the filter circuit is to remove the ac component of the rectifier output but allow the dc component to pass through. The ac component is termed "ripple" (and in audio work "hum", from the 100 Hz signal produced in the speakers by the ripple voltage).

The ripple will be an important factor in deciding the performance of a power supply, so we must establish an accurate means of measuring and recording it. For this purpose we introduce the "ripple factor", which is defined by —

$$\text{ripple factor, r equals } \frac{\text{rms value of alternating components of output}}{\text{dc value of output}}$$

For a good power supply the alternating component is small in relation to the dc component, so the ripple factor will be small.

The dc and ac components may be measured quite readily using a dc reading meter for the dc component, and an rms reading meter (with a capacitor in series) for the ac component.

With a sinusoidal input, the ripple factor of a half-wave rectifier is 1.21, and for a full wave rectifier it is 0.482. In other words for a half-wave circuit the ac component is larger than the dc component by about 20%, while for a full-wave circuit the ac component is less than half the dc component. Thus full wave rectification clearly provides a substantial improvement in ripple factor, and hence it is almost always used where the quality of the dc supply is in any way important.

The simplest filter circuit is a choke or inductance connected in series with the output. The reactance of the choke is $2\pi fL$, where f is frequency (in Hz), and L the inductance of the choke (in Henrys). The ac component of the waveform sees this as a high impedance, but the dc component, having zero frequency, sees no impedance. Thus a high impedance is inserted for the ac component, but has no effect on the dc component. (In practice there will be a small dc resistance due to the copper wire used to wind the choke).

A typical circuit arrangement is shown in Fig. 21.

The ripple factor with a choke filter is approximately

$$r = \frac{1}{3\sqrt{2}} \quad \frac{R_L}{2\pi fL}$$

Thus ripple is increased as the load increases and as the current falls (Ohm's Law), i.e., low ripple at high currents.

A substantial improvement is obtained with the capacitor filter (Fig. 22). The capacitor value must be large

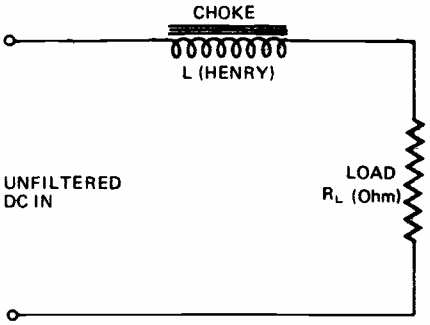


FIG. 21

to provide as low an impedance path around the load as is possible for the ac components. Of course, no dc passes through the capacitor.

The capacitor charges up to the peak of the unfiltered dc output, and when the output voltage falls, the capacitor discharges through the load, thus

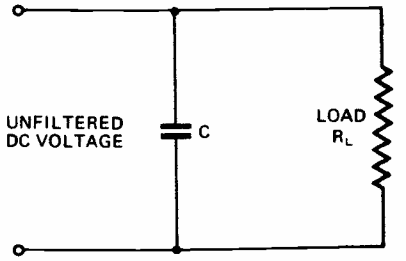


FIG. 22

tending to keep the voltage across the load up to its peak value.

The major drawback of the capacitor filter is that with each peak it recovers the lost energy, and this results in a high current inrush as the capacitor starts charging (Fig. 23). Because of the voltage stored on the capacitor the diode has only a positive voltage across it for the time periods shown in Fig. 23.

The peak diode current is

$$I_{peak} = V_m \sqrt{(2\pi f)^2 C^2 + \frac{1}{R_L^2}}$$

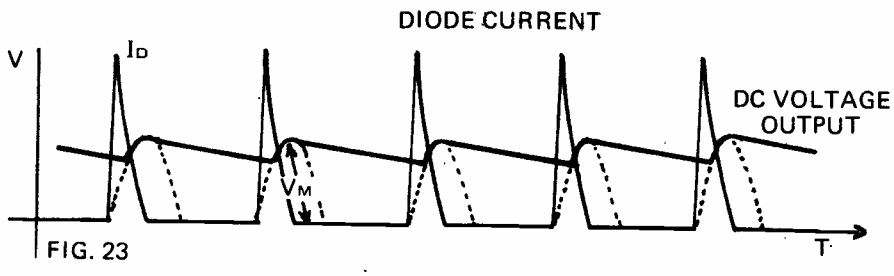


FIG. 23

This is the peak current which the diode will conduct on each fluctuation. The diode peak current rating must, therefore, be in excess of the value which is calculated from the above.

For a single capacitor filter the ripple factor is given by

$$r = \frac{I_{DC}}{4\sqrt{3}\ f\ C\ V_{DC}} = \frac{1}{4\sqrt{3}\ f\ C\ R_L}$$

A substantial improvement is obtained with one of the more commonly used circuits, the pi-section filter (Fig. 24).

The ripple factor for this circuit is

$$r = \sqrt{2}\ \frac{Xc}{R_L}\ \ \frac{Xc1}{X_L 1}$$

It is possible to replace the inductor with a low value resistor (with a sufficiently high wattage to allow it to carry the full load current).

The ripple factor is then

$$r = \sqrt{2}\ \frac{Xc}{R_L}\ \ \frac{Xc1}{R}$$

The use of the resistor in place of the choke is quite common because of the expense, weight, and bulk of the choke.

VOLTAGE STABILIZATION

There are three main factors which may cause the output voltage to vary. The ac supply may fluctuate by up to ± 10%, the load current may range from zero to the full load current, and the temperature may have a further effect, particularly with semi-conductor devices.

The main source of variation in output voltage is the variation with load current. This is because the resistance of the copper wire used in the transformer, the forward resistance of the diode, filter resistance, and the like, cause a voltage drop which is proportional to the load current.

It is possible to represent a voltage source by an ideal voltage source in series with the internal resistance (indicated above) as shown in Fig. 25. The voltage appearing across the load is then the voltage of the ideal voltage source *less* the voltage drop across the internal resistance.

i.e. $V = E - I\,Ri$

So as I increases, V falls.

The measure of the stability of the output voltage is the *regulation*, defined as

$$\text{per cent regulation} = \frac{\text{no load voltage} - \text{full load voltage}}{\text{no load voltage}} \times 100$$

Devices which stabilize the output voltage are, therefore, frequently called regulators.

Regulators fall into two categories. These are the shunt regulator (Fig. 26) and the series regulator (Fig. 27).

Both type utilize the fact that Vo = Vi = Vf. If Vi alters and Vf can be made to alter by an equal amount, then their difference (i.e. Vo) will be unchanged.

With the shunt regulator the output voltage is compared with a fixed reference voltage V_R, and a greater or lesser current is drawn by the regulator in proportion to the difference.

This either increases or decreases V_f depending on whether Vo has increased or decreased.

The series regulator has V_f dropped over the regulator itself and the voltage-drop over the regulator is made inversely proportional to current by comparison of Vo and V_R.

The second part of this article will consider actual regulator circuits, protection, transients, saturating core transformers, control of power flow, output voltage control, and cooling. ●

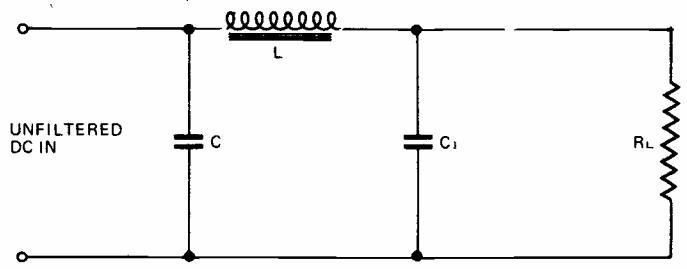


FIG. 24

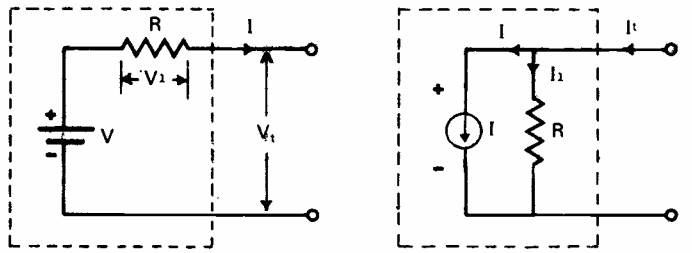


FIG. 25

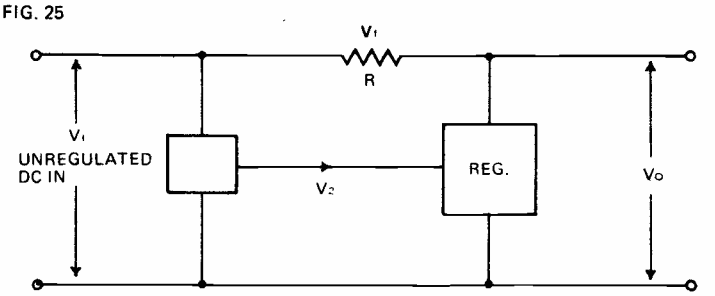


FIG. 26

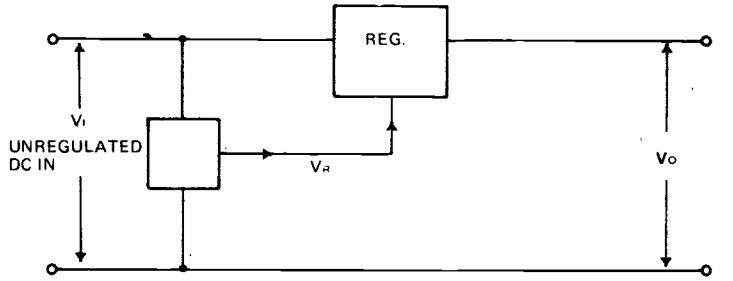


FIG. 27

POWER SUPPLIES Part 2

The output voltage from an unregulated supply may vary considerably with changes in input voltage, load current and ambient temperature.

This can be overcome by comparing the output voltage against a 'reference voltage' (that will remain constant despite external variations) and correcting accordingly.

The zener diode may be used as voltage reference source for just this purpose. It is simply a diode manufactured in such a way that it has the unique ability of maintaining a very high reverse resistance, until, at a certain critical voltage, the dynamic resistance falls to a very small value. In this region an essentially constant voltage will be maintained over a wide range of currents. This is shown graphically in Fig. 28.

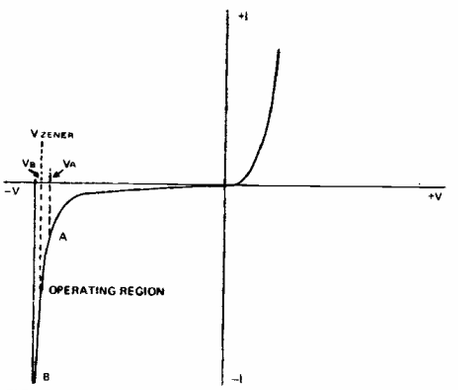


FIG 28

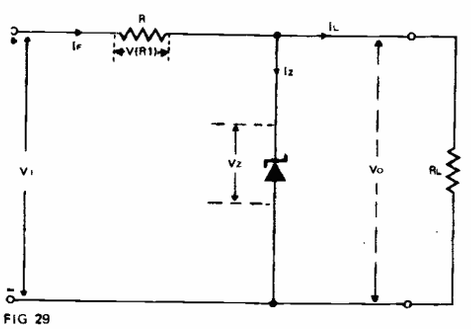
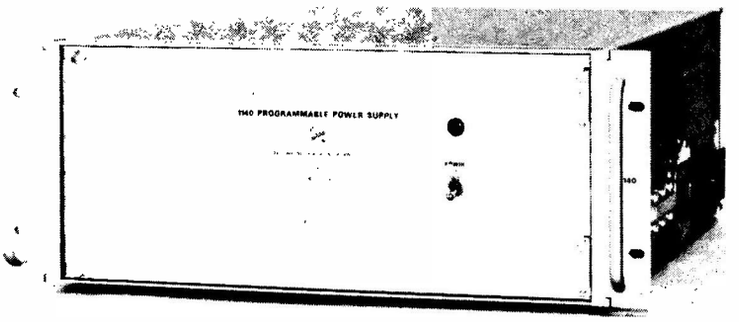


FIG 29



This unit from Tektronix contains three 40 volt supplies, one 100 volt supply, and one current supply. The power unit can be externally programmed.

Fig. 29 shows a zener diode used to produce a constant voltage despite varying load current and supply voltage. As these vary, the zener shunt element draws more or less current. The nett result is a substantially constant output voltage across R_L.

The series resistor R is selected so that the minimum current passing through the zener, lies beyond the knee of the curve shown in Fig. 28, but at the same time ensuring that the zener diode does not exceed its maximum specified power rating (which is at a maximum at zero load).

The design proceedure for the simple shunt regulator shown in Fig. 29 is:—

1. Specify maximum and minimum load current (I_L), say 10 mA and 0mA.

2. Specify the maximum supply voltage V_i that is likely to occur (say, 12 volts) but ensure that the minimum supply voltage will always be approximately 1.5 volts higher than the breakdown voltage of the zener to be used.

3. Thus at any time $V_i = V_z + V_{(R1)}$, where V_z is the breakdown voltage of the zener, $V_{(R1)}$ is the voltage across R_1. And $I_Z = I_Z (min) + I_L$, where I_L is the maximum load current required.

Assume that the required output voltage, and hence the zener voltage is 6.5 volts, and the specified minimum zener current is (I_z min) is 100 micro-amps.

Then the maximum I_z is 100 micro-amps + 10 mA which is 10.1 mA.

Thus the series resistor R1 must conduct 10.1 mA at the lowest input supply voltage: and so allowing 1.5 volts minimum drop across R1 (in other words $V_i - V_z$) then

$$R1 = \frac{1.5}{10.1 \times 10^{-3}}$$

$$= 148.5 \text{ ohms}$$

The value of R1 is thus 148.5 ohms, and the nearest preferred value to this is 150 ohms.

At the maximum supply voltage (12 volts) the voltage drop across R1 is $I_z R1$.

$$I_Z = \frac{(12 - 6.5)}{150} \text{ mA.}$$

$$= 36.7 \text{ mA.}$$

And this is the maximum current that will flow through the zener at any time, i.e., maximum input voltage and zero external load.

The power dissipated by the zener

under these conditions is

$$Pd = I_Z V_Z$$
$$= 6.5 \times 36mA$$
$$= 234\ mW.$$

This power dissipation is within the capabilities of most small zener diodes — which are rated at 400 mW min.

It should be noted that whilst the zener voltage should be equal to the desired dc output voltage, there is always a small tolerance on the nominal value of the voltage (typically ± 5%), and selection may be necessary in critical applications.

SHUNT REGULATORS

The regulation and power handling capability of a zener diode may be increased by using it as a voltage reference element in an amplifier circuit.

The simplest of these, the shunt regulator, is shown in Fig. 30.

Fig. 30 illustrates the way in which

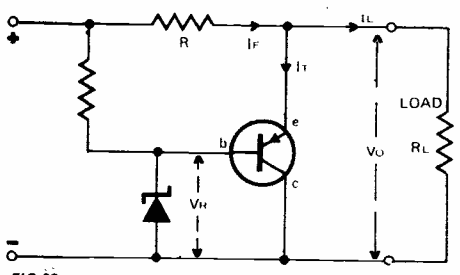


FIG 30

an amplifier is combined with a zener diode.

In this circuit arrangement the zener voltage is made nearly equal to the desired output voltage, and holds the base of the transistor fixed at voltage V_R. If V_o decreases, the voltage between the emitter and base of the transistor will decrease by the same amount, so reducing the emitter current I_T, and with it I_f ($I_f = I_T + I_L$), so tending to restore V_o by decreasing the voltage drop across R. All other variations are similarly accommodated.

The two main advantages of this type of circuit are that the power rating of a transistor is usually greater than that of a zener diode, and this allows a lower value of R to be used, thus improving the regulation of the circuit and secondly, the amplification introduced by the transistor increases the sensitivity of the circuit to much smaller changes in output voltage.

The shunt regulator is inherently short circuit proof, and because of this it is often used for simple power supplies intended for schools, and experimental use. The circuit is however, basically inefficient, and because of this, the series type of regulator is more commonly used.

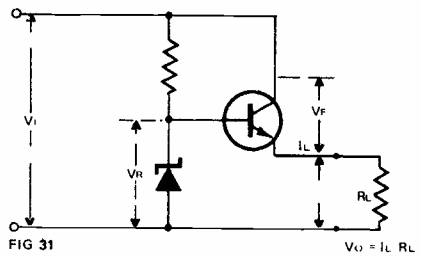


FIG 31 $V_O = I_L R_L$

SERIES REGULATORS

The basic series regulator circuit is shown in Fig. 31.

The voltage at the base of the transistor is held at a constant voltage, V_R, by the Zener diode. If the output voltage rises, a greater current may pass through the transistor (since $V_o = I_L R_L$). But this increase in V_o decreases the voltage between emitter and base of the transistor, so reducing the current which the transistor may pass. And since $V_f = V_i - I_L R_L$, increasing the collector to emitter voltage (V_f) reduces V_o back towards its previous value.

The main disadvantage of this circuit is that the regulating transistor is in series with the output, and because of this it must be capable of carrying the full load current; if a short circuit load is applied, the full dc voltage appears across the transistor.

REGULATORS — a more general view

Both the series and shunt transistor regulators described above measure the difference between a fixed reference voltage and the output voltage, and use this voltage difference to control the regulator. In other words the regulator compares output voltage to reference voltage and makes an adjustment in accordance with this difference.

All regulators use a comparator circuit, and this introduces the problem of providing a fixed reference suitable for both a non-variable voltage source and a variable voltage source, (which must of course have an adjustable reference).

A fixed standard voltage can be provided by using either a standard cell as a well defined known voltage; or a zener diode which, with proper circuitry, gives a fixed (but not necessarily accurately known) voltage.

The standard cell voltage reference will only remain accurate if negligible current, or at least a constant current is drawn from it, so that the internal voltage drop is constant. The main drawback of the standard cell is that it "goes flat", but if treated with due respect, it offers a very accurate reference, and in critical applications this disadvantage may be tolerable.

Loading on the cell can be prevented by using a buffer amplifier. The type of amplifier used will take the difference between two inputs and give an output proportional to this difference.

A simple buffer amplifier is shown in Fig. 32.

Terminal 1 is at zero potential and terminal 2 is at a potential $V_r - E_r$. The load current is supplied by the amplifier, not by the standard cell, which now serves only to maintain a fixed voltage difference across the amplifier. If the input resistance of the amplifier is high, the current drawn through the cell will be small. Ideally, the input resistance of the amplifier will be infinite, so that no current is drawn from the standard cell. This circuit allows a substantial current flow at the reference terminals without loading the standard cell.

The inconvenience of periodic cell replacement may be avoided by using a zener diode, although this results in a small sacrifice in accuracy.

A zener diode circuit can however be made extremely stable by maintaining a constant current in the zener (there being only one voltage on the characteristic curve corresponding to any one particular current). In order to maintain a constant current, the zener diode is connected across the terminals of a constant current generator as shown in Fig. 33.

In this circuit, (Fig. 33), terminal 1 is at zero potential and terminal 2 is at a potential Vr — Ez. The load current is supplied by the amplifier, not by the zener diode which now serves only to maintain a fixed voltage difference across the amplifier. If the input

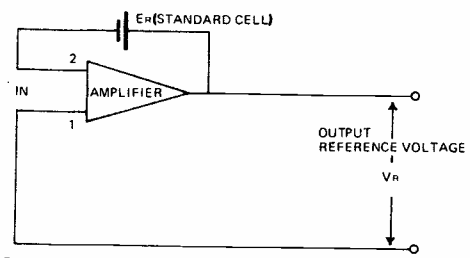


FIG 32

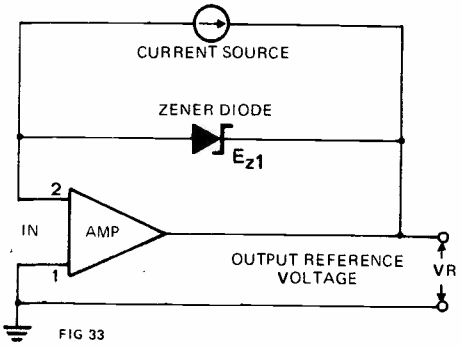


FIG 33

resistance of the amplifier is high, or at least constant, the current through the zener diode will be a constant value at all output load conditions.

An adjustable reference is provided by circuits of the basic type shown in Fig. 34.

Either a potentiometer or a stepped switch may be used to vary the potential input to the amplifier, and hence its output. There are many refinements to this circuit which can be readily seen in specific regulator circuits.

Since the regulator tends to counter any fluctuation in output voltage it will tend to reduce the effect of the ac component of the dc, thus assisting the filter circuit.

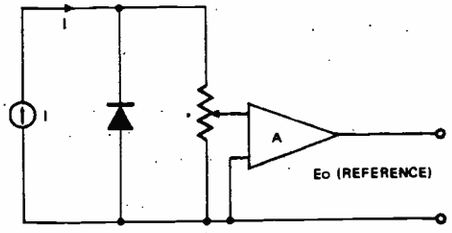


FIG 34

CONTROL OF POWER DISSIPATION AND VOLTAGE RANGING.

The regulator circuit must be capable of dissipating a good deal of power. For a shunt regulator with no load the full voltage is across the regulator, and for a fully loaded series regulator, the full current must flow through the series transistor. The power dissipated by the regulator is the product of voltage across it and current through it.

The series type regulator is generally preferred for high power application because the power dissipated is less than for the shunt type, and it is more suitable for use with pre-regulator circuits.

The pre-regulator circuit adjusts the output voltage of the transformer to a few volts above the desired dc output voltage, so that there need only be a low voltage across the series transistor, hence reducing its power dissipation.

There are two basic approaches to this. The first is to provide a variable transformer output voltage by having taps at various voltages on the secondary with a rotary switch to select the desired tap (a refinement of this being the continuously variable variac type transformer). The second is to use Silicon Controlled Rectifiers (SCRs) in the type of bridge rectifier circuit shown in Fig. 35, the output of

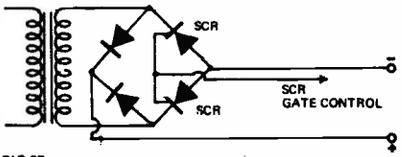


FIG 35

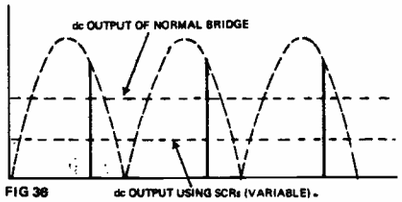


FIG 36

which is shown graphically in Fig. 36.

PROTECTION

The protection of a power supply involves protection of each of the main elements, (the transformer, the rectifier, and the regulator) from overpower, overcurrent, and overvoltage in both steady and transient form.

The simplest form of protection is the fuse, or in its more elaborate variant, the circuit breaker. The fuse uses the heat produced by the overload current to melt a fine piece of wire, which, on melting, produces a gap in the wire over which an arc will be struck until further melting increases the gap beyond the length that the arc can sustain. The break in the circuit is then complete.

The circuit breaker uses the overcurrent to operate an electromagnet which separates contacts to break the circuit. There is an arc drawn at the initial opening of the contacts, but this breaks before the opening is complete.

Both fuse and circuit breaker are quite adequate for protection of the transformer, but unless they are of special construction, have severe limitations if used for semi-conductor protection.

The transformer heats quite slowly because of the large masses of material used in its construction. The semi-conductor material however is only a fine chip, which will heat very quickly to its maximum allowable temperature (which is quite low).

A conventional fuse will not break the flow of current immediately. It must first be heated to its melting point. Typically, this will take about one second at twice normal current, 100 milliseconds at four times normal current and 10 milliseconds at 10 times normal current. A silicon diode will be destroyed, typically, after half a second at twice normal current, after 30 milliseconds at four times normal current, and after five milliseconds at 10 times normal current. Thus if the diode and fuse are rated for the same current the diode will protect the fuse.

A similar problem arises with a circuit breaker, which, because of its inductance, delays the current build up and requires a finite operating time for contact movement.

The conventional protective devices are, therefore, limited in their application, unless they are rated well below the diode current maximum. This, in fact, is the usual solution applied to "built-in" power supplies which have only to carry the load they are intended for.

A safe formula that will ensure that the diode is adequately protected by the fuse is

Diode max. current = 0.8 X short circuit current.

With present-day diodes this substantial over-rating can be achieved quite easily in most cases, and at moderate cost.

Another method is to use special types of fuse and circuit breaker that act much more rapidly than the conventional type, and are therefore, suitable for protection of semi-conductors. But care should be taken when considering the use of fast-action fuses, because of the possibility of someone inadvertently replacing them with conventional fuses.

In most cases using over-rated semi-conductors is better.

Clearly it will be desirable to limit the short circuit current to as low a value as possible. With a normal transformer the internal resistance of the transformer and diodes is the only limit on the short circuit current. But as we have already seen the higher the internal resistance the more difficult the problem of regulation, so there is an obvious need to compromise and it is usually towards a lower resistance to improve regulation and reduce transformer heating in regular service.

It is here that the self-regulating (saturating core) transformer possesses a marked advantage.

The currents in primary and secondary of the transformer are related so that if the secondary current increases, so does the primary current required to maintain the secondary current, and as the current increases so does the flux, which is the only link between primary and secondary. In a

conventional transformer this is so up to the full short circuit current, so the primary continues to supply the flux to support a high secondary current. But the self-regulating transformer saturates, i.e., the flux does not increase after a certain level, so there is no increased flux to support an increase in secondary current, thus the maximum current which can be supplied by the secondary is limited by the saturation of the transformer core.

The circuit is, therefore, self-limiting and theoretically has no need of any other protection provided that the rectifier and regulator can carry the maximum current which the secondary will deliver.

The simpler type protection described above is not always adequate and there are a range of electronic protective circuits which give better protection.

OVERCURRENT CONTROL

The basic method of current control is to insert a low value resistor in series with the output current and then utilize the voltage drop across this resistor in the same way that is done with a voltage control circuit. Thus a basic current limiting circuit is as shown in Fig. 37. Diodes D1 and D2 are non-conducting when the forward voltage drop across them is less than 0.25V for germanium diodes and 0.7V for silicon diodes. But if the volt drop across R_s exceeds this level, the diodes will conduct and provide negative feedback which reduces current through the transistor. If R_s is made variable, the short circuit current may be altered as desired.

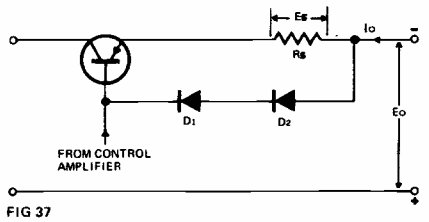


FIG 37

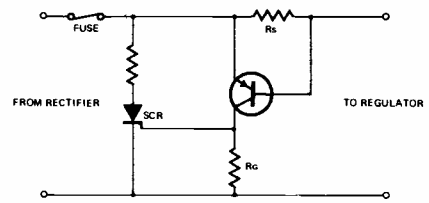
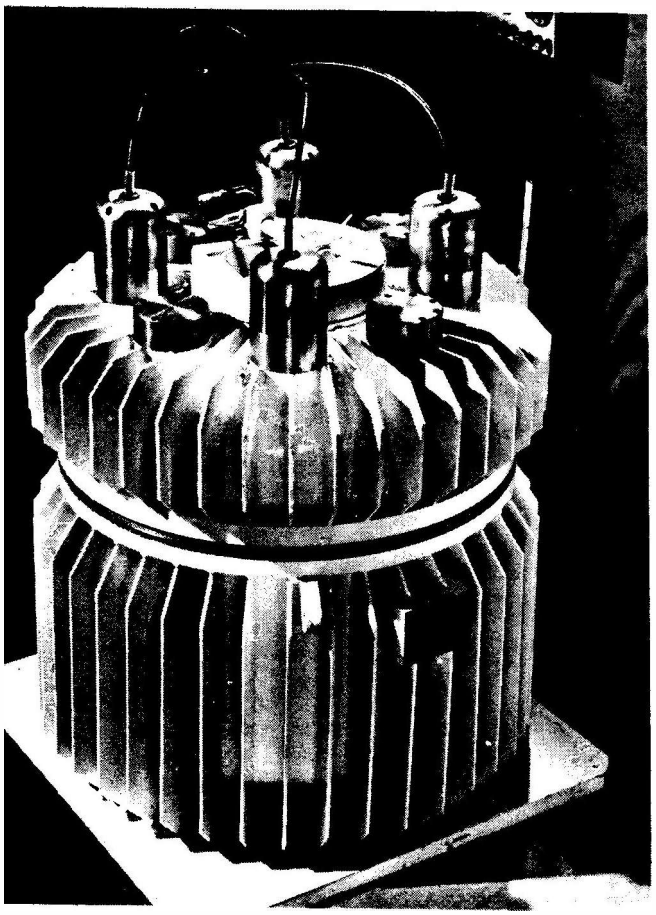


FIG 38

Another type of overcurrent protection that is quite commonly used is "crowbar" protection. (Fig. 38) In broad principle this consists of switching a short circuit across the output of supply and before the input of the circuit to be protected and then relying on the supply protection to operate. This is useful because the short circuit can be switched in very quickly, thus protecting following semi-conductors, and the fuses can then operate with their usual time lag without any danger to the remainder of the circuit.

The value of Rs is chosen so that normally the transistor is cut off and so, therefore, is the SCR, but if the current rises to an unsafe value the voltage across Rs will increase and turn the transistor on, producing a voltage across R_G and so triggering the SCR which will conduct heavily within about 20 microseconds, well before the one millisecond or so danger time for semi-conductors. The fuse will then blow after say 10 milliseconds. The main limitation of this type of circuit is that there may be some sharp transient effects produced by the rapid switching of the SCR. These may be sufficiently large to endanger the circuit which it is intended to protect.



This radio isotope powered generator provides electrical energy for a major marine navigational light.

OVERVOLTAGE PROTECTION

Wherever semi-conductors are used it is essential to safeguard against overvoltages which may breakdown the semi-conductor structure and allow excessive currents to flow.

There are various causes of overvoltages. The main ones are as follows:

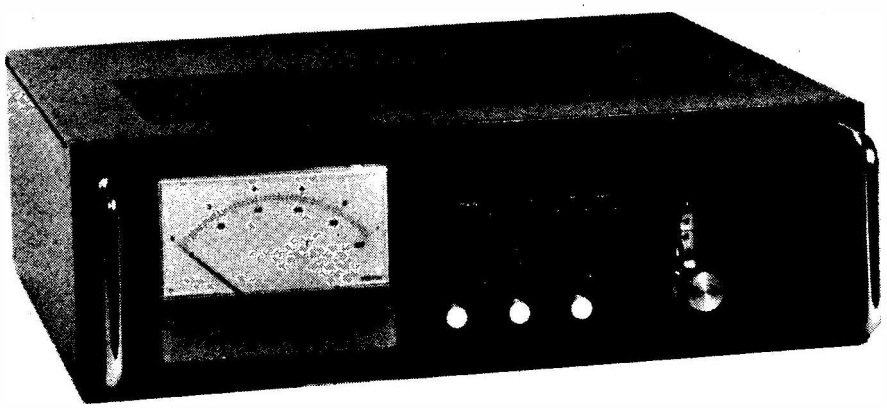
(i) Hole-storage effect. When a semi-conductor is switched on (or off) there is a time lag before the minority carriers move into (or from) the base region. This tends to act as a capacitor, giving a voltage spike on switch on (or off) This is normally reduced by connecting small capacitors across the line.

(ii) When a short circuit is interrupted by a fuse an overvoltage is developed the magnitude of which depends on the arc voltage and the circuit of the power supply.

(iii) Transient voltages are similarly produced when a circuit breaker opens.

(iv) If an unloaded rectifier is disconnected on the ac side, some of the magnetic energy stored in the core is converted to electrostatic energy in the winding and lead capacitance.

(v) Ac supply transients will be



Miles Hivolt's TH25/25 can be switched on/off locally or remotely, and the voltage controlled manually or, by a low-voltage input, remotely. DVM readout of voltage and current provides remote monitoring.

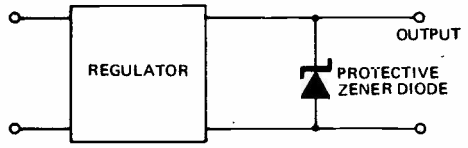


FIG 39

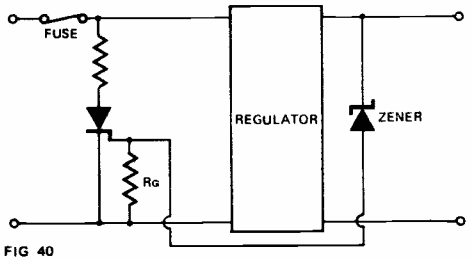


FIG 40

transmitted across the transformer. The usual protection for all these overvoltages is to use diodes with a voltage rating of at least one and a half times the peak inverse voltage.

All transient voltages may be reduced by connecting capacitors into the circuit which absorb the energy of the transient pulse (by charging up to the pulse voltage).

In many cases a more sophisticated form of overvoltage protection is desired, and this may be obtained either with a simple zener diode as shown in Fig. 39, or a crowbar circuit as shown in Fig. 40.

In Fig. 39, if the output voltage rises above the zener voltage the zener will conduct heavily, so shunting the output.

In Fig. 40, if the output voltage rises the zener diode will conduct and pass a current to the gate of the SCR thus triggering it. This places a short circuit across the supply and blows the fuse.

The circuit of Fig. 39 is self-restoring, while that of Fig. 40 is not. That is to say once the overvoltage has ceased to exist the circuit of Fig. 39 returns to normal operation, whereas the fuse must be replaced in the circuit of Fig. 40.

These circuits are usually only required for special applications, and for in-built supplies for various equipment it is usually sufficient to use conservatively rated diodes, and a capacitor or two.

OVERPOWER PROTECTION

Overpower protection is not used widely since it will usually be accompanied by overcurrent or overvoltage.

However, in some applications there may be a particularly expensive device, or some critical apparatus which must be protected from excessive power dissipation (with its consequent excessive heat build up).

One of the simpler techniques is to fix a thermistor to the heatsink of the component to be protected as shown in Fig. 41.

The potentiometer is adjusted so that at normal operating power the SCR is non-conducting, but if the power rises so does the temperature, thus lowering the thermistor resistance and increasing the SCR gate voltage. This type of circuit is not very accurate (±10°C approx.) but may be refined if need be, to give better sensitivity.

The methods of protection described above are by no means the only ones available, but are certainly the most widely used.

USE OF INTEGRATED CIRCUITS IN POWER SUPPLIES

Bridge rectifiers in integrated circuit form have been available for several years now. They consist of the four diodes of the bridge rectifier combined inside a single package with two ac terminals and a + and a— terminal.

More recently integrated circuit regulators have become available and there are also integrated crowbar circuits on the market. The main limitation of integrated circuits for power supply applications is their power ratings. Existing IC's cannot cope with the power which discrete devices can handle, at least at their present stage of development. Otherwise, integrated circuits give the same advantage in power supplies as in any other circuit.

The theoretical circuits considered so far require some additional components before they become useful practical circuits.

A PRACTICAL CIRCUIT EXPLAINED

The series regulated supply shown in Fig. 42 combines controlled voltage and current limiting and uses zener diode ZD1 as a reference source.

Reference diode ZD1, which is supplied by resistors R1 and R2, clamps the base of transistor Q4 at a fixed potentional. Capacitor C1 smooths out any 100 Hz ripple from the input.

The output voltage of the power unit is sampled by R6, RV1 and R7 and this is compared against the zener reference voltage by transistors Q4 and Q5. The voltage at the base of Q5 is the zener voltage minus the two base-emitter voltages, i.e. $V_z - 1.2V$. The output voltage is then this voltage multiplied by the ratio of the resistors in the divider chain.

The output of the comparator is taken via R5 to the output stage consisting of transistors Q2 and Q3.

The action of this part of the circuit is as follows, if the output voltage drops (because the load has increased) then the difference between the zener reference voltage and the divided output voltage will increase. And since this voltage appears across the base-emitters of Q4 and Q5, these

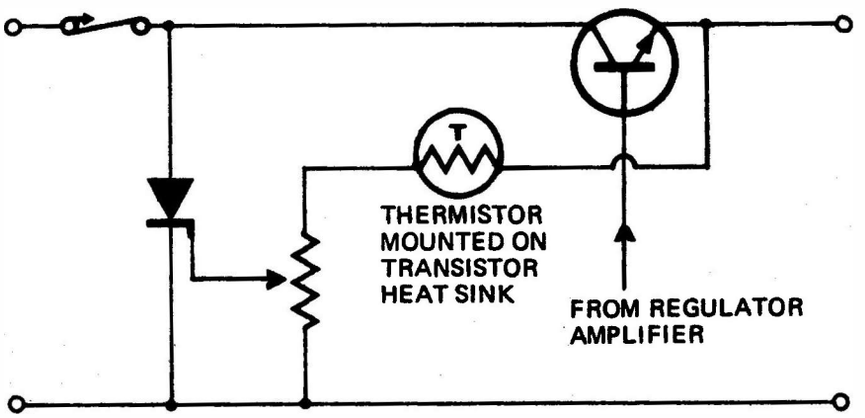


FIG 41

transistors will pass more current. This causes Q3 and Q2 to conduct more heavily, thus reducing the voltage drop across them and so allowing the output voltage to rise and compensate for the increased load; for every load there will be a stable output voltage the regulation of which is dependant on the gain of the comparator amplifier.

The second mode of operation is current limiting, and this is used to protect both the power unit and the load in the event of a short circuit or load that exceeds a predetermined level.

When the current increases beyond a predetermined level, the voltage drop across R3 is sufficient to bias transistor Q1 into conduction. When this occurs the output from the voltage comparator Q4, Q5 is progressively removed from the output transistors Q3 and Q2; these in turn reduce the excess current flowing into the load and an almost constant current is now supplied to the load regardless of any further load increase.

POWER SUPPLY PERFORMANCE CRITERIA

(i) **LOAD REGULATION**
Load regulation is a measure of the ability of a power supply to maintain a constant voltage at its terminals regardless of load variation. The regulation is normally specified as a percentage of the nominal output voltage for a fixed voltage supply or of the maximum voltage of a variable voltage supply. So if regulation of a 50V supply is given as say 0.01%, the terminal voltage will not fall below (50 -0.005)V or rise above (50 + 0.005)V.

(ii) **LINE REGULATION**
Line regulation is a measure of the ability of the power supply to absorb changes in the ac mains voltage while holding the output voltage steady. The ratio of the change in output voltage for a change in mains voltage multiplied by 100 gives the line regulation percentage.

(iii) **RIPPLE**
This may be measured with either a true rms reading meter or with a cathode ray oscilloscope. Then ripple is

$$r\% = \frac{\text{rms of ac component}}{\text{dc component}} \times 100$$

(iv) **TEMPERATURE STABILITY**
The output of a power supply should be constant, regardless of ambient or operating temperature. A performance figure is sometimes quoted in mV/°C.

(v) **CURRENT STABILITY**
The above four quantities may be evaluated for current stability by inserting a series resistor in the circuit so that the voltage produced across it is proportional to the current.

(vi) **TRANSIENT RECOVERY TIME**
In some applications it may be important that should the loading be sufficient to force the output outside the tolerance band set by the regulator, the supply will re-adjust itself swiftly. The transient recovery time gives a measure of the speed of re-adjustment.

(vii) **LONG TERM STABILITY**
There is some drift in the performance of a power supply if it is used continuously for say 8 hours. The % change in output voltage may be quoted per 8 hours, 12 hours, 24 hours or whatever the maker specifies.

In assessing the performance of a power supply note should also be taken of its overload protection facilities, and of any transients observable on switch on/off, or with operation of the protective circuits. ●

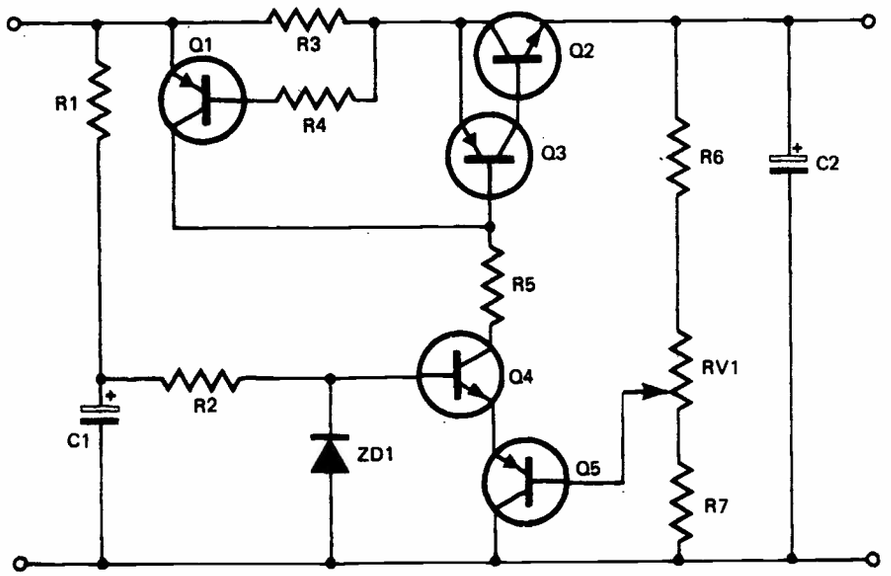
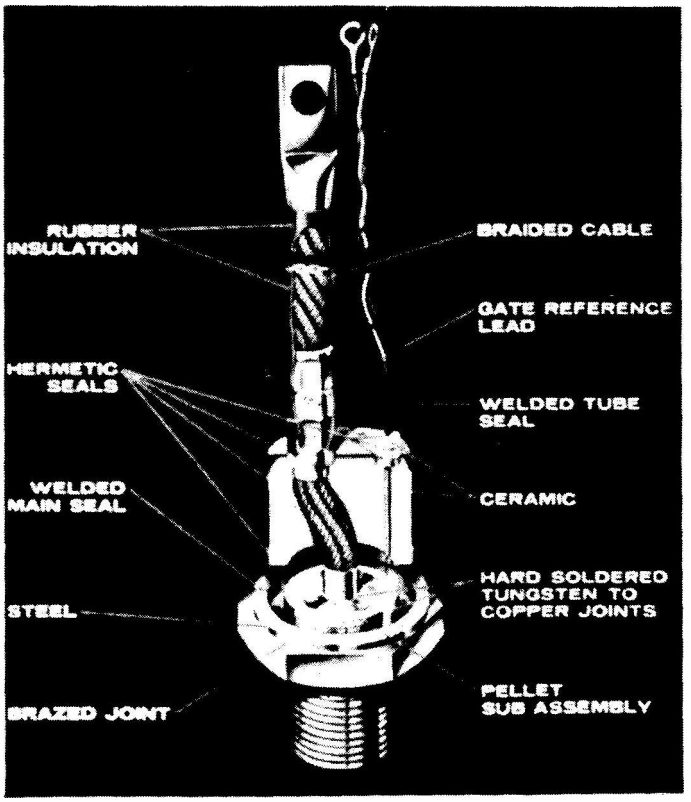


FIG 42

A PRACTICAL GUIDE TO SCR'S

Used in applications as diverse as switching 240 volts in a photographic timer to forming a major element in a 50,000 hp motor speed control system – the SCR is a simple device with a myriad of uses. Here, Collyn Rivers explains, simply and clearly, how to use this versatile circuit component.



The silicon controlled rectifier (or SCR as it is commonly called) is a rectifying device in as much that it can be *caused* to have a low resistance in the forward direction, but *always* has a high resistance in the reverse direction.

The device is called a silicon *controlled* rectifier since it can be switched from a very high forward resistance (its 'off-state') to a low forward resistance (its 'on-state'). And although silicon controlled rectifiers can cope with both high voltage and high current, they can be switched from the 'off-state' to the 'on-state' with very low levels of gate voltage, current and power.

Silicon controlled rectifiers are readily available in a wide variety of shapes, sizes and power handling capabilities. They may be encapsulated in plastic, encased in metal, and either air or water cooled. Voltage capabilities range from 12 volts to many thousands of volts, and current ratings from a few milliamps to several thousand amps. SCRs are surprisingly cheap, for example GE's C 106 (4 amps) can be bought in quantity for a few pence.

They are, in many respects, a solid-state equivalent of the gas-filled thyratron, and like the thyratron, once triggered into the 'on-state', SCRs can only be switched off again by breaking (or reversing) the flow of current through them.

The circuit symbol and schematic diagram of the silicon controlled rectifier is shown in Fig. 1.

THE SCR IN AC CIRCUITS

In ac circuits, the polarity of the voltage across the SCR is reversed on alternate half-cycles, and the resultant reverse voltage will cause the device to revert to the 'off-state', switching on again during the next positive half-cycle only if a triggering voltage exists at the gate. When used in this fashion, conduction may be initiated at the beginning of any positive half-cycle, thus providing a simple on-off control. Or conduction may be initiated at some later time in the positive half-cycle, thus varying the voltage impressed upon the load. This process is known as 'phase-control'.

Silicon controlled rectifiers may be used to control ac power by connecting them in inverse parallel so that one SCR conducts load current in one direction, while a second conducts in the opposite direction. The gate firing signal may be used to switch on the flow of current, and by using phase control, the average power applied to the load may be varied.

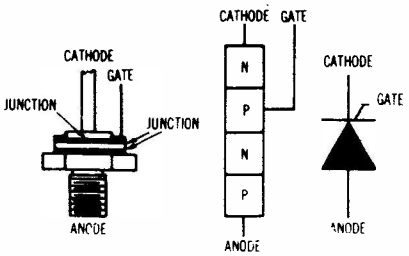


Fig. 1. Cross Section, Block Diagram, and Electrical Symbol of Silicon Controlled Rectifier.

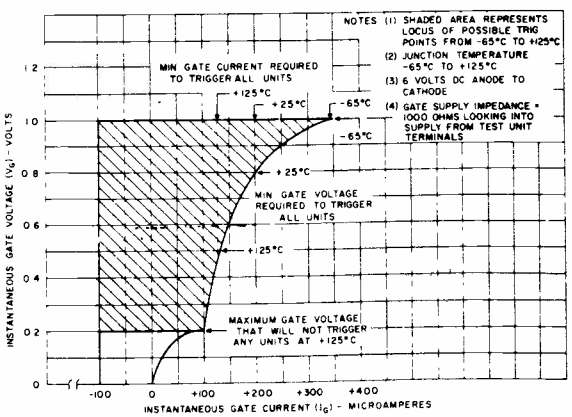


Fig. 2. This graph shows the triggering characteristics of the low-current type C106 SCR.

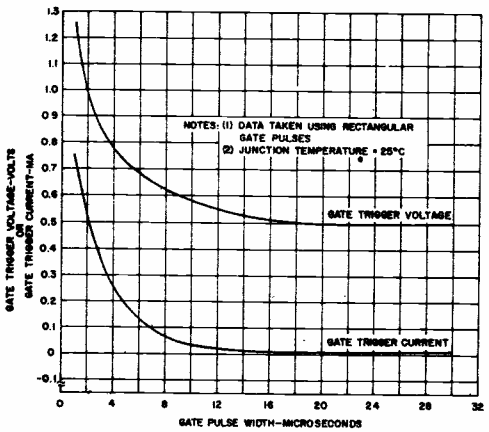


Fig. 3. Relationship between trigger pulse width and pulse magnitude (C106 SCR).

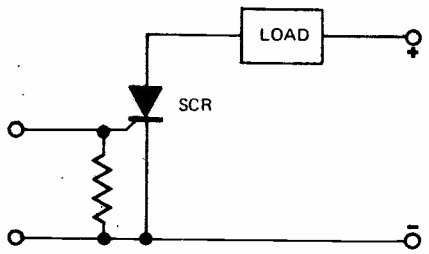


Fig. 4. A 1k bias resistor is connected between gate and cathode to provide operational stability.

THE SCR IN DC CIRCUITS

In dc circuits, where the voltage across the SCR does not reverse, the gate may be used to initiate current flow, but some specific means must be used to turn the SCR off again. This may take the form of a mechanical switch that interrupts the load current, or a more complex circuit in which firing a second SCR causes a break in load current or a momentary flow of reverse current through the first controlled rectifier, causing it to turn off. This latter process is called commutation and is the basis of operation of the SCR inverter.

TRIGGERING THE SCR

A silicon controlled rectifier is triggered into conduction by a positive pulse (or continuous dc voltage) applied to its gate terminal.

The level of voltage required varies from one type of SCR to another – and between individual SCRs of the same type. It is also affected by ambient temperature (voltage and current firing requirements decrease as temperature increases).

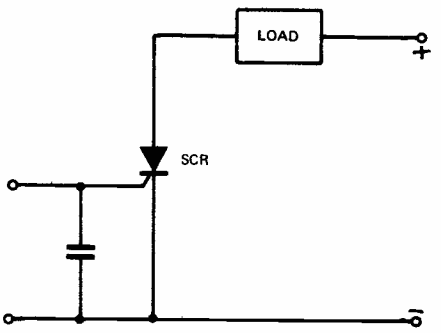


Fig. 5. Where dc triggering is used, a capacitor may be used in place of a bias resistor.

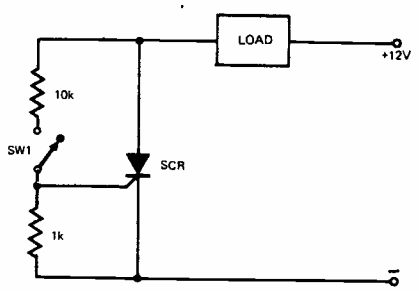


Fig. 6. Basic SCR switching circuit.

typical graph – showing firing requirements of the C106 series is shown in Fig. 2.

Manufacturers of SCRs publish specification sheets showing firing requirements in graphical form. A

The graph also shows the maximum gate voltage that will *not* trigger a C106. This knowledge is invaluable in applications where a small constant voltage may be impressed on the gate.

The graph shown in Fig. 2, and its counterparts for other SCRs, applies only when the SCR is being triggered from a dc gate source, or from a pulse source where the pulses are of relatively long duration. But if the width of the trigger pulse is reduced below about 20 micro-seconds, it is necessary to increase the magnitude of the triggering pulse above that shown for constant voltage triggering (in Fig. 2 etc.). The relationship between trigger pulse width and magnitude for the C106 is shown in Fig. 3.

BIASING

Many low-current SCRs are so sensitive that they require only a few micro-amps of gate current for reliable triggering. In fact, at high temperature, or with high voltage applied, the SCR's internal leakage may be sufficient to cause self-triggering. Similarly, in high frequency ac applications, or in dc circuits where anode voltage is suddenly applied, sufficient capacitive current may flow to trigger the SCR. In all applications where low-current SCRs are used, the possibility of spurious triggering must be eliminated by the provision of sufficient stabilizing gate bias.

In most applications the necessary gate bias can be readily obtained by connecting a resistor (of about 1k) between the gate and the cathode – as shown in Fig. 4. A bias resistor – *as such* is not always required, for in dc coupled gate circuits the output resistance of the trigger source (pulse transformer – or UJT base one resistor) will serve the same purpose. Again in many circuits where dc triggering is used, a capacitor may be used in place of the bias resistor (the optimum size will be somewhere between 0.1uf and 0.5uF.) Fig. 5 refers.

Generally it can be said that the stability of SCR circuits increases almost in proportion with decreasing bias resistance and that the maximum amount of bias (minimum resistance) should be used commensurate with the available triggering source. The lower limit of bias resistance is reached when the trigger source can only just supply sufficient current for the parallel combination of SCR gate and bias resistance.

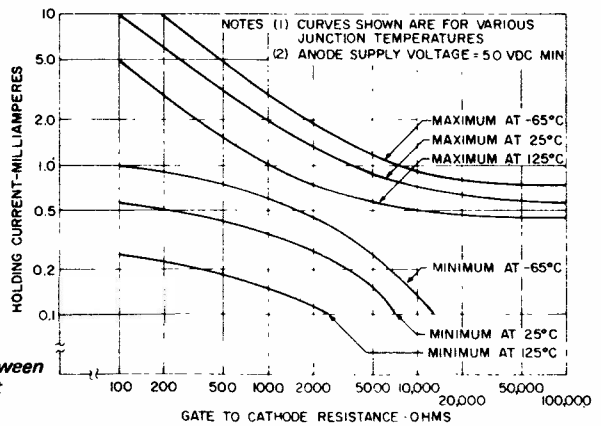


Fig. 7. Relationship between bias and holding current (C106).

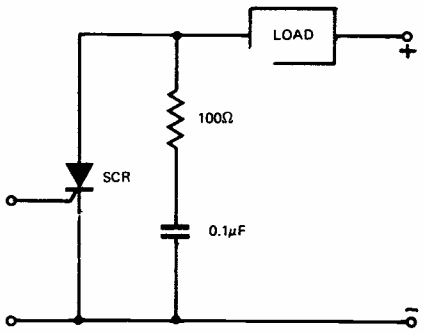


Fig. 8. Resistor/capacitor combination connected across the SCR provides dv/dt suppression (see main text).

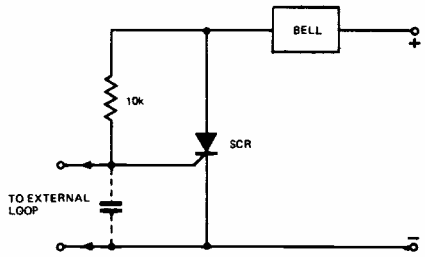


Fig. 9. This basic alarm circuit is in common use, but is prone to false triggering – see main text.

LATCHING

A basic SCR switching circuit is shown in Fig. 6. In this circuit the SCR is in series with the load. The SCR is normally non-conducting (i.e. no power is applied to the load), but if a positive potential is applied to its gate – for example by closing SW1 – the SCR will be switched on and the load energized. The SCR will then remain switched on, even if SW1 is subsequently reopened. This action is called 'latching'.

A certain minimum current must pass through the SCR for the device to switch to the 'on' state and to remain in the 'on' state (latched) after the cessation of a gate triggering pulse. But once latched, a somewhat lower level of current will suffice to prevent the SCR reverting to the 'off' state. This latter current level is called the 'holding' current.

The level of latching and holding currents vary from one type of SCR to another – and indeed between different SCRs of the same type. The current levels are also dependent upon ambient temperature and the value of the gate bias resistor. (Typical figures for the C106 range, at 25°C, are – holding current, 3.0 mA; latching current, 4.0 mA.)

The use of resistive bias also affects the level of latching and holding current required. The greater the amount of bias the higher the current required for reliable holding. Figure 7 shows the relationship between bias and holding current for a typical 4 amp SCR.

(Some difficulty may be experienced in obtaining reliable latching in circuits where the load is primarily inductive, as for example with relay coils, even though the steady state current exceeds the latching requirements. Here the remedy is to connect an appropriate resistor across the inductive load. The resistor should be selected to ensure that it alone can pass enough current to effect latching.)

FALSE TRIGGERING

In some SCR circuits the SCR will tend to 'switch on' the moment the dc supply voltage is applied, at the SCR's gate. This is because the SCR is sensitive to the rate at which the supply voltage is applied, and if this rate of rise exceeds a certain level, switch-on will occur. The effect may be eliminated by connecting a series resistor/capacitor combination across the SCR. This is known as dv/dt suppression and its effect is to slow down the rate of voltage rise. A diode, connected in the same effective polarity as the SCR, may be paralleled across the resistor for maximum effectiveness. In most applications the values shown in Fig. 8 will prove effective.

False triggering can also be caused by transients induced into the gate circuits. This is a very common problem with a number of burglar alarms – even commercially made ones from manufacturers who should know better.

The most commonly used SCR burglar alarm circuit is basically that shown in Fig. 9. In this configuration, the gate of the SCR is connected to the positive rail via a 10k resistor, but an external loop interconnecting a number of normally closed trip switches, effectively clamps the gate at zero potential. However if any switch is opened, or if the external loop is cut, the SCR will immediately be triggered into conduction, thus energizing a series connected bell.

The problem with this circuit is that although the gate of the SCR appears to be held very firmly at zero potential by the external loop, transient energy induced into the external loop by electro-magnetic phenomena (caused by lightning, arc welders, fluorescent lighting starters etc) can reach quite high voltage levels at the 'open' SCR end of the loop. And these levels are more than sufficient to trigger a sensitive SCR.

In some instances this type of false triggering can be overcome by connecting a 1.0uF capacitor between the SCR's gate and cathode but generally speaking it is bad practise to connect long 'aerials' directly to the gate circuit of an SCR.

A better solution is to use a UJT as a 'buffer stage' – as shown in Fig. 10. This will ensure that the gate circuit is totally immune from false triggering no matter how long the external circuit, (UJT and other triggering circuits will be described in greater detail in the second article in this series).

False triggering may also be caused by switching transients if long external leads are used in the anode or cathode circuit of the SCR. This sometimes occurs with burglar alarms and other control and warning systems if a bell (or other load) is located some distance away from the SCR.

This problem can almost invariably be overcome by using dv/dt suppression (as shown in Fig. 8). In extreme cases it may be necessary to use a 5uF capacitor and a 5k series resistor, but values of 1uf and 1k will generally suffice.

STATIC SWITCHING CIRCUITS

As may be seen from the examples shown so far, the SCR in a dc circuit is analogous to a static latching switch, making it an ideal replacement for relays, contactors, and other electromechanical devices. Where latching action is undesirable, latching may be eliminated by driving the SCR from an ac supply. In either case the SCR doubles as a power switch with all the advantages of a solid state component – small size, high speed, ruggedness and long life – and as a high gain amplifier. ●

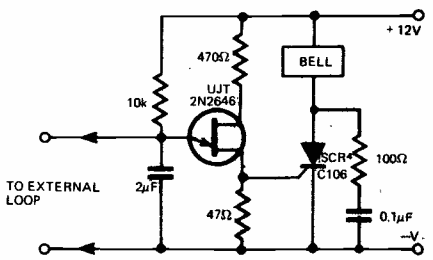


Fig. 10. This is a greatly improved version of the circuit shown in Fig. 9. The addition of the 2N2646 UJT effectively isolates the gate of the SCR from signal transients.

A PRACTICAL GUIDE TO SCR'S Part 2

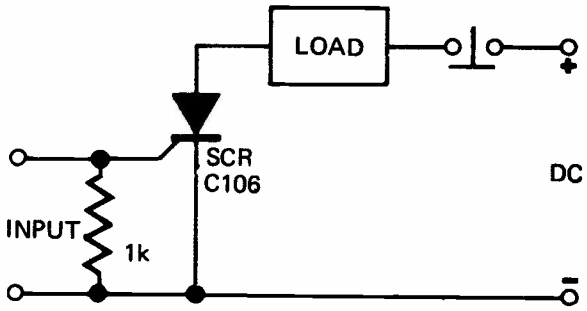
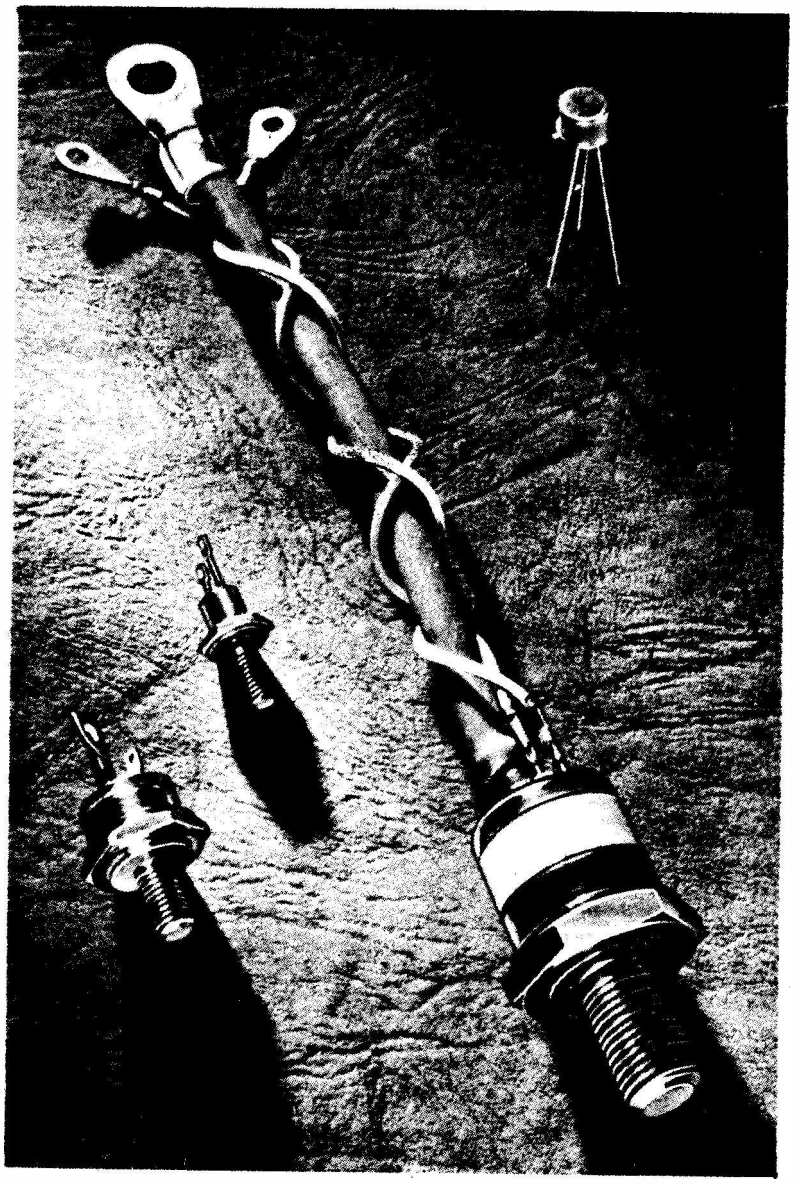


FIG. 1



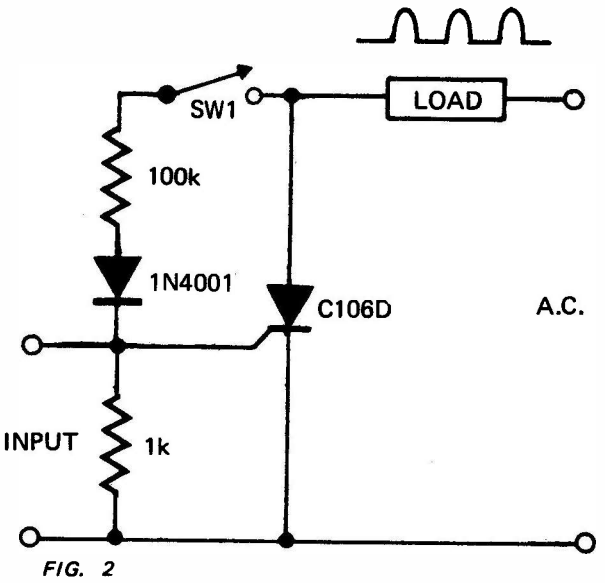


FIG. 2

SCR's may be used to simulate common relay configurations, Figs. 1 through 5 show how this can be done.

Figure 1 shows how an SCR can simulate a single pole single throw latching contact. A positive input to the gate of the SCR activates the load. The circuit is deactivated by the 'reset' switch.

An ac energized version of this circuit is shown in Fig. 2. Here, a positive input (or closure of SW1) will cause the load to be energized with half-wave rectified dc. Reset is automatic when the triggering signal is removed (or SW1 is opened).

The circuit shown in Fig. 3 is a 'normally closed' version of that shown in Fig. 2. Here a positive input to the gate of SCR1 shorts out the gate of SCR2, thus preventing it triggering. When the input signal is removed, SCR1 switches off and SCR2

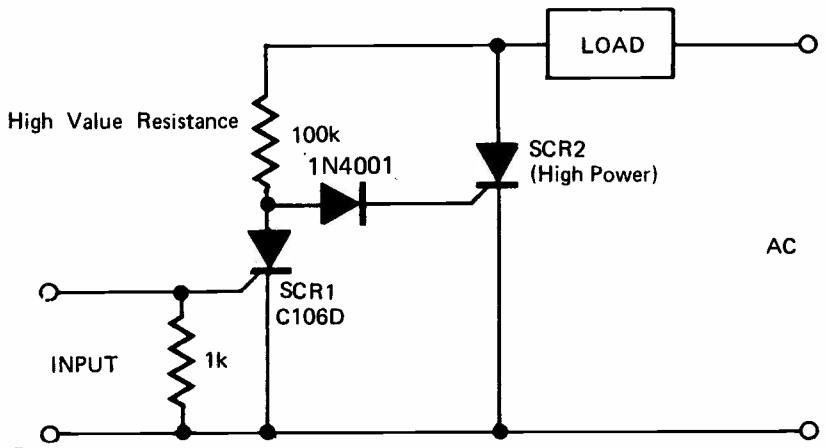


FIG. 3

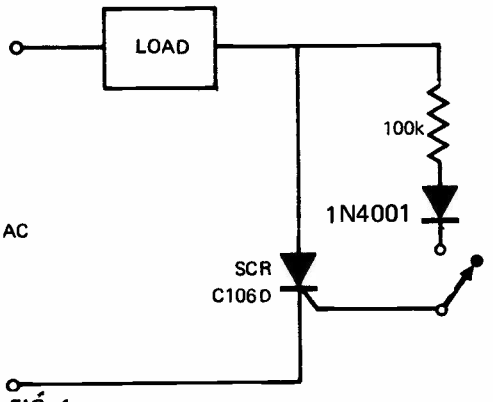


FIG. 4

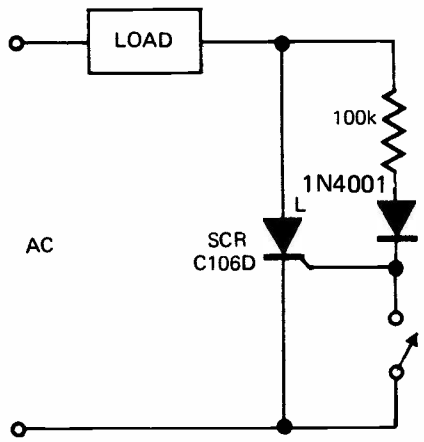


FIG. 5

is biased into conduction thus energizing the load. This circuit may also be triggered by a switching device – simply by the addition of the 100k resistor and 1N4001 diode shown in Fig. 2.

Figure 4 shows how an SCR may be triggered (via a switch) by energy derived from the ac supply. The circuit shown in Fig. 5 is a variation of Fig. 4, the difference being that the switch shown in Fig. 5 causes the SCR to switch 'off' when closed.

It is important to appreciate that the circuits shown in Figs. 2, 3, 4 and 5 will cause half-wave rectified dc to be supplied to the load.

Full-wave operation may be obtained by connecting the SCR's within a full-wave rectifier bridge as shown in Fig. 6. Both ac and dc loads may be switched using this type of circuit, but unless the circuit is being used to take advantage of the low gate current triggering capabilities of small SCR's, it is generally more satisfactory to use Triacs if full-wave switching is required.

LOGIC OPERATIONS

The 'on-off' (or binary) nature of the SCR makes it an ideal device for low-speed logic circuitry in applications where large power output is required. They may be used to drive high current relays, incandescent lamps, fractional horse-power motors etc.

Figure 7 shows how a pair of C106s may be used as an 'AND' circuit capable of switching up to four amps. In this circuit, unless inputs 1 and 2 occur simultaneously, no voltage can exist across the load.

An 'OR' gate, again using C106s, is shown in Fig. 8. Here, an input to either 1 or 2 will energize the load.

Figure 9 shows a triggered multivibrator – an input to 1 energizes load 1. A subsequent input to 2 energizes load 2, thus turning off SCR1 and de-energizing load 1.

The circuit shown in Fig. 10 is a 'one shot' or pulse generator. Here an incoming signal triggers the SCR and energizes the load. The load voltage energizes the UJT timing circuit. After a time determined by R1/C1, the UJT fires, and a pulse generated across R2 is coupled to the cathode of the SCR through D1 and C2. The SCR's cathode is momentarily lifted above the anode voltage and the SCR turns off.

A pulse generating circuit, suitable for use as a car, boat or warning flasher, is shown in Fig. 11.

This circuit will operate reliably from noisy or fluctuating power supplies – and unlike many multivibrator circuits – is inherently self-starting when power is applied. In this circuit unijunction transistor Q1 is used as a relaxation oscillator supplying a continuous train of pulses to the gates of the SCRs. Assume that SCR2 has been triggered into conduction and that lamp 2 is energized. The next trigger pulse from Q1 triggers SCR1, this discharges C2 and the resultant commutation pulse turns off SCR2. The resistor R2 in the anode of SCR1 is of a value high enough to prevent SCR1 from latching on. SCR2 is retriggered by the next triggering pulse from Q1. Using the component values shown, the flash rate of this circuit is adjustable – by R2 – from 35 to 150 flashes a minute.

TIMING CIRCUITS

The precision time delay circuit shown in Fig. 12 will provide accurate and repeatable time delays adjustable from a few milliseconds to a minute or two. This is a very flexible circuit in which the operating current and voltage depends only on the choice of SCR.

The timing sequence may be initiated either by applying power to the circuit – or by opening a shorting switch

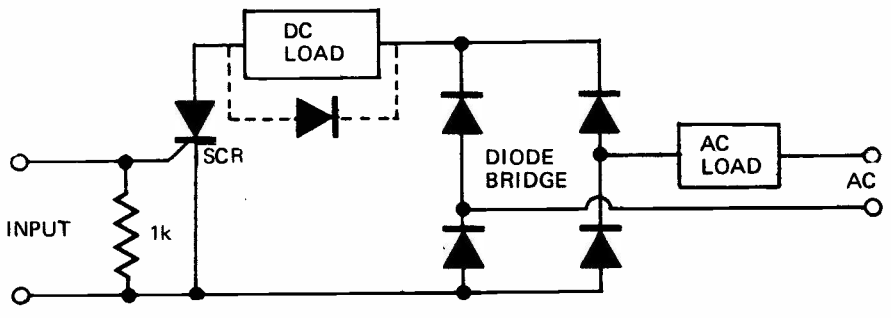


FIG. 6

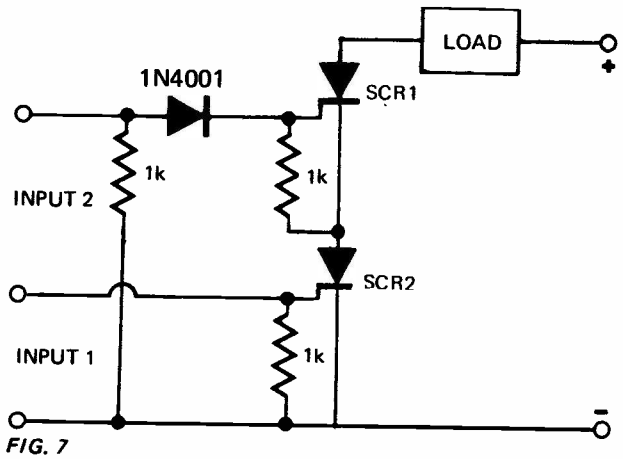


FIG. 7

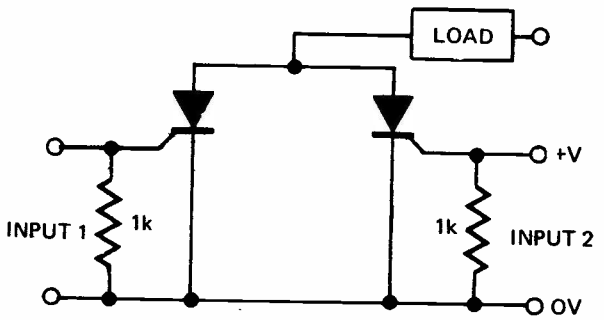


FIG. 8

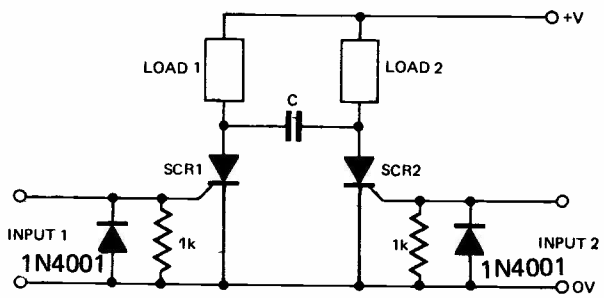


FIG. 9

wired across C1. Timing capacitor C1 is charged via R1 and R2 until the voltage across C1 reaches the peak point voltage of the UJT Q1. When this occurs, Q1 fires, generating a pulse across R4, triggering the SCR, and applying power to the load. Holding current for the SCR is provided via R5 and D1.

The circuit is reset by momentarily removing the supply voltage.

If the circuit is to be used in an application where both rapid cycling and accurate, repeatable timing is required – some provision must be made to ensure that C1 is discharged to zero before each timing sequence. This can most easily be done by interconnecting a pair of switch contacts with the reset system so as to momentarily short out C1 whenever the circuit is reset.

Temperature compensation for this circuit is provided by R3. Increasing the value of this resistor causes the circuit to have a positive temperature coefficient. It is possible to obtain zero coefficient over a small range of ambient temperatures by optimizing R3.

A simpler version of this time delay circuit is shown in Fig. 13. The supply voltage to the timing circuit is not Zener stabilized in this latter version, and because of this, repeatability is not as good.

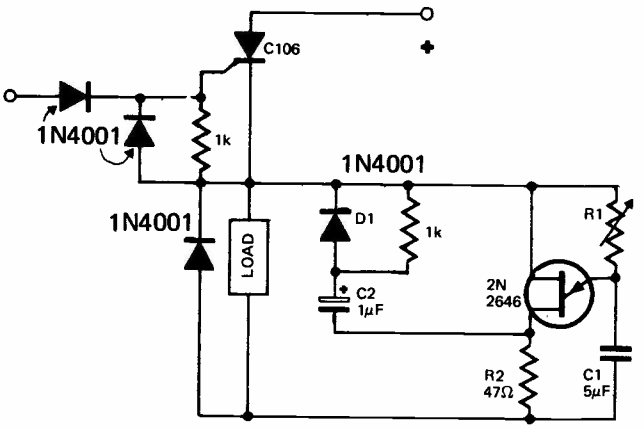


FIG. 10

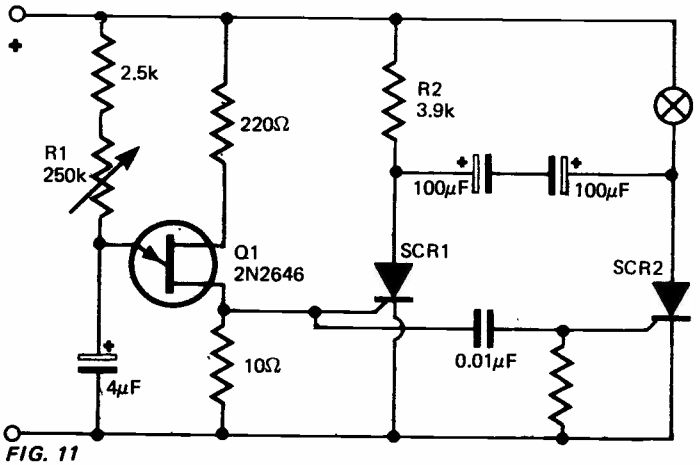


FIG. 11

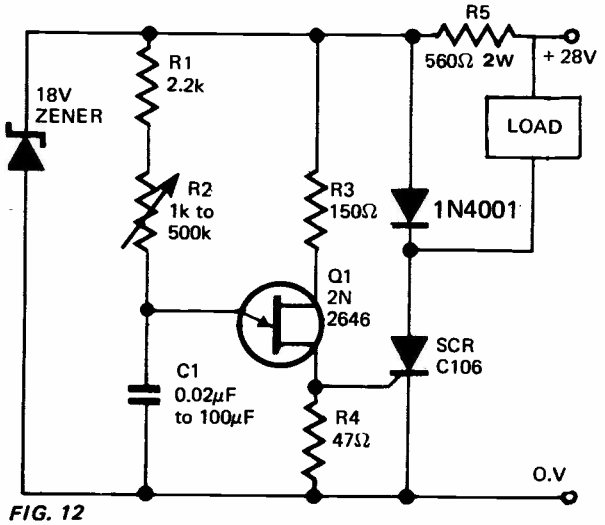


FIG. 12

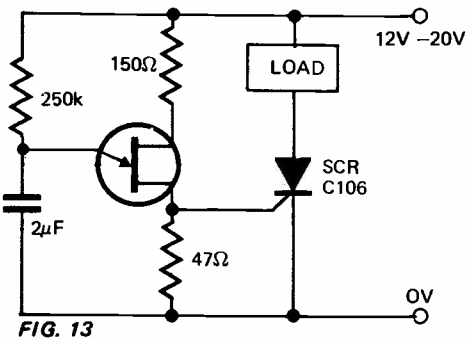


FIG. 13

The timing circuits shown above provide delays which may be adjusted from less than a millisecond to approximately one minute. The upper time limit is determined by the amount of leakage in the UJT timing capacitors. It is possible to use special large value low-leakage computer type capacitors, but a more satisfactory (and certainly cheaper) solution is to use a circuit such as that shown in Fig 14.

This circuit will provide precise time delays from about ½ millisecond to several minutes — in fact by using a 2μF mylar capacitor as C1 and a 2000 Megohm timing resistor as R1, the circuit will provide delays of well over one hour with excellent repeatibility.

In operation, the peak point requirement of UJT Q1 is reduced to about 1/1000 of its normal requirement by pulsing its upper base with a ¾ volt negative pulse derived from the free running oscillator UJT Q2. This regular pulse momentarily reduces the peak point voltage of Q1 and thus allows the peak point current to be supplied from C1 rather than R1, as it would be with the more conventional circuits of this type. The pulse rate of oscillator Q2 is not very critical but it should have a period that is less than one fiftieth of the overall time delay. Resistor R2 may be adjusted to provide optimum temperature stability.

An unusual timing circuit is that shown in Fig 15. This circuit is often used in electrically powered stapling machines, impulse hammers etc, and causes load current to flow through the load for one complete half-cycle of the ac supply whenever SW1 is actuated (i.e. moved from its normal position (1) to energise-load position (2)). The circuit is arranged so that the SCR is always triggered at the beginning of a positive half-cycle of the ac supply, even though the switch may be closed randomly at any time during the previous two preceding half-cycles.

Resistor R1 and capacitor C1 should be chosen so that their series combination supplies just sufficient holding current for the SCR for one complete half-cycle.

PHASE CONTROL

Phase control is a technique used for varying the effective power input to a load.

It is a process of rapid on-off switching in which the ac supply is connected to a load for a controlled (but adjustable) fraction of each cycle.

The simplest form of SCR phase control is shown in Fig. 16. This is a very basic circuit and provides control only from SCR full-on (100% of half-wave output) to SCR half-on (50% of half-wave output).

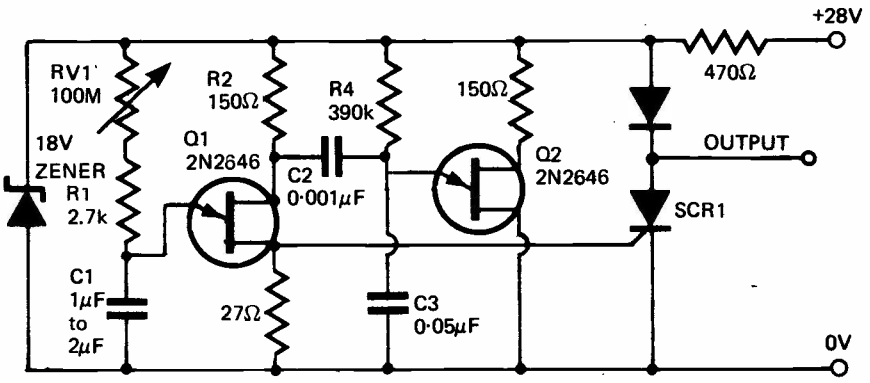


FIG 14

The addition of one capacitor and one more diode (Fig 17) extends the range of the basic phase control circuit from SCR full-on (100% half-wave output) to SCR off (0% half-wave output). In this circuit, the values of R1 and C1 must be chosen to suit the characteristics of the particular type of SCR that is used.

By wiring a diode across the SCR (Fig 18), the basic phase control circuit will provide a fixed half-cycle of power plus a variable half-cycle. Thus control can be obtained from full power to half power — but there will be a major dc component which will

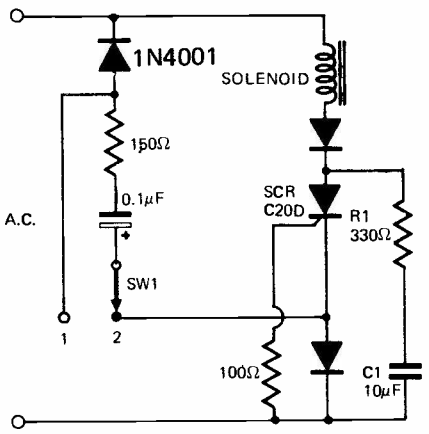


FIG 15

adversely affect many loads — especially inductive loads. In particular a half-wave control circuit should not be used to vary the power input to a transformer, variac, induction motor etc.

Full-wave control, over the full range from zero to maximum, may be obtained by connecting the basic control circuit inside a full-wave diode bridge. (Fig 19) This arrangement may be used to provide either controlled ac, or controlled and rectified dc. Losses in the rectifier bridge reduce the electrical efficiency of this circuit, and generally it is preferable to use Triacs rather than SCR's if full-wave control is required.

HALF-WAVE CONTROL FOR UNIVERSAL MOTORS

One of the most common applications for SCR phase control systems is speed control of commutator motors — such as those used for food mixers, sewing machines, pottery wheels etc.

However one of the disadvantages of controlling motor speed by varying input power is that as the effective power input is reduced to slow down the motor — the torque available is reduced as well.

This may be overcome by using a feedback signal to advance the firing

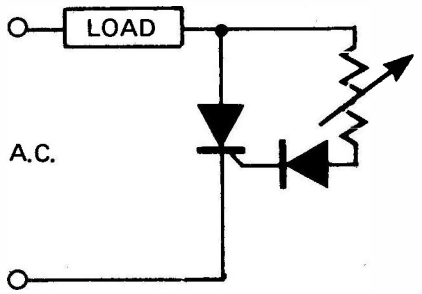


FIG. 16

angle in proportion to the load on the motor — thus increasing the power input if more torque is required.

The circuit shown in Fig 20 achieves this load compensating function by deriving a feedback signal from the armature back-emf (produced by the residual field of the motor). In this circuit, the SCR is triggered when the voltage on the wiper arm of potentiometer R2 rises to a high

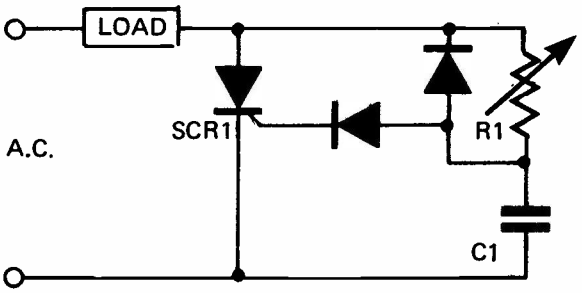


FIG 17

enough value to forward bias diode D2 – thus allowing gate current to flow. As the back emf tends to reverse bias D2, the firing point of the SCR depends largely upon the back emf and this in turn is a function of speed. If the motor is loaded, the speed reduces, thus also reducing the back emf – hence D2 becomes forward biased earlier in the cycle (triggering the SCR earlier in the cycle), and thereby supplying the motor with more power to offset the effect of the loading.

The component values shown in **Fig 20** are suitable for most fractional horsepower motors – for optimum results it will be necessary to adjust component values to suit the motor used.

The circuit described above will provide stepless speed control over a wide range of motor speed – but tends to cause jerky operation at low speeds.

This tendency can be almost entirely overcome by using the circuit shown in **Fig 21.** As may be seen from the circuit diagram, it is necessary to bring out separate connections from the armature and field windings. This is generally a simple operation and providing it can be done the circuit will provide stepless speed control down to virtual standstill. In this circuit the 20V zener diode provides a constant voltage for the discharge of C1. Capacitor C2 and resistor R4 are connected from gate to cathode of the SCR to stabilize the circuit by preventing the SCR from being triggered by extraneous signals.

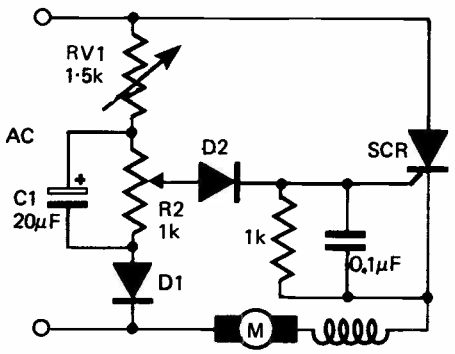


FIG 20

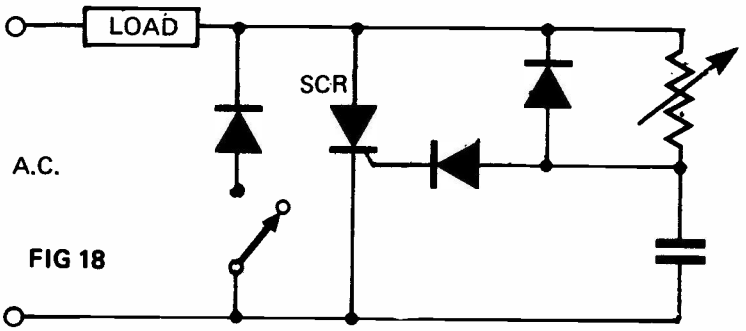


FIG 18

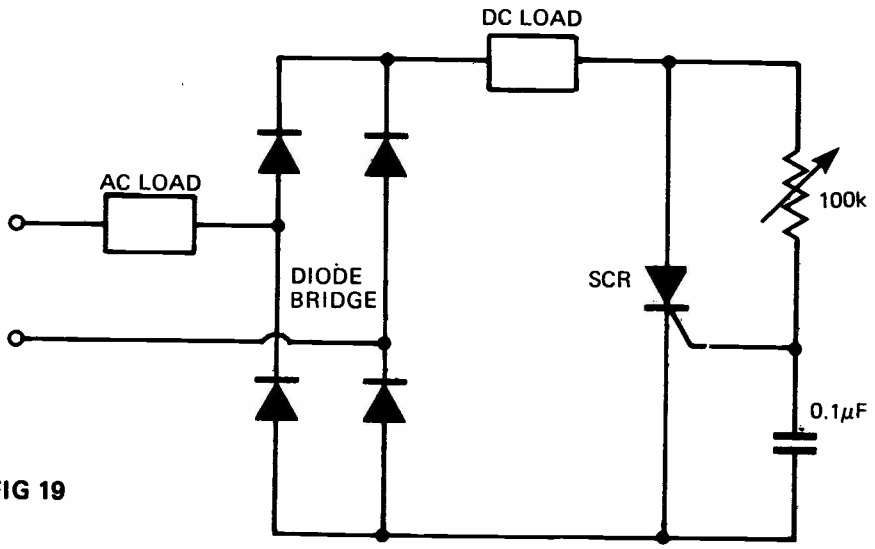


FIG 19

INDUSTRIAL APPLICATIONS

Silicon controlled rectifiers are in common use around the world for the control of very large dc motors – often using tachometer feedback control to provide speed regulation. These control systems are built in surprisingly large sizes and single units exceeding 50,000 h.p. are by no means uncommon.

Another common use for industrial SCR's is in the control of heating loads – and here again very large loads may be steplessly controlled. ●

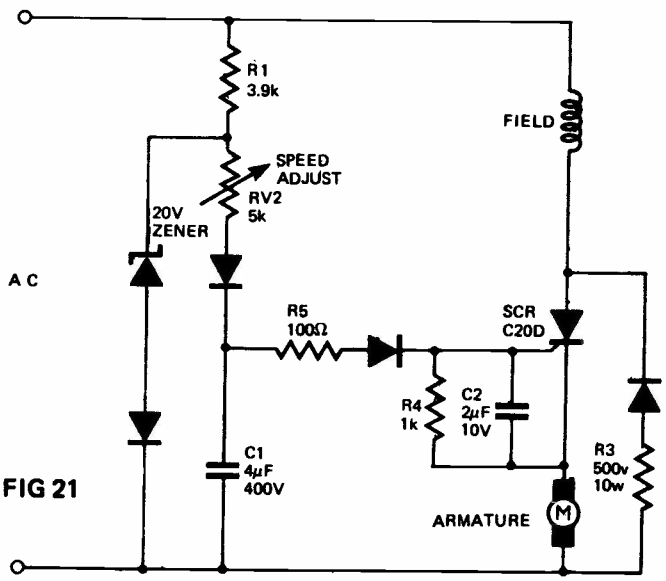


FIG 21

OP AMPS AND INTEGRATORS

Although we're dominantly digital these days, there are some applications where the trusty op amp is cheaper and easier — differentiating and integrating circuits, for instance. A. S. Lipson reveals all . . . .

Digital computers, folks, are not always fastest or cheapest. No, don't faint. No kidding — those amazing digital circuits we keep hearing about do not always get the job done first! They're fine, of course, as long as we stick to straightforward arithmetic, but unfortunately, there are occasions when we want to do other things (no, not that sort of thing . . .), such as integration or differentiation. Circuits performing these functions are not only of use in computers, however; they are of great use to those of us who are just simple mortals, as well. For instance, in function generators, a square wave may be changed to a triangular wave merely by integrating.

Now, while digital circuits can perform these functions, they do tend to get a bit bulky and expensive. It's very much easier to use analogue circuits. As it happens, we have very simple networks that make passable integrators and differentiators for very little money. They're capacitor-resistor series circuits, and their operation is quite easy to understand.

Differentiators

We can make quite a serviceable differentiator circuit from the series combination of resistor and capacitor shown in Fig. 1. Now from our original definition of capacitance, the current flowing through a capacitor is given by;

$$I_C = \frac{d\,V_C}{dt}$$

But, in the case where we are driving a load with very high input impedance, I_{OUT} will be negligible, and I_R will be very close to I_C. We can say, without too much inaccuracy, that $I_R = I_C$. I_R, however, is given by Ohm's law, $I_R = V_{OUT}/R$. Thus $V_{OUT} = RI_R$. Since I_R is the same as I_C, however, this gives;

$$V_{OUT} = RI_C = RC\frac{dV_C}{dt}$$

and so the output voltage is effectively the voltage across the capacitor, differentiated and then multiplied by a scale factor RC. If we don't want this scale factor, we can just arrange matters so that $RC = 1$.

The main problem with this circuit, of course, is that it is, indeed, the voltage across the capacitor, and not that across the input, which is differentiated. However, as long as we don't let the output voltage get too large, V_C will be very close to V_{IN}, and this error will not matter too much.

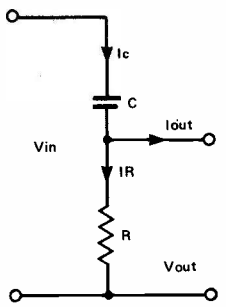


Fig. 1. Basic differentiator.

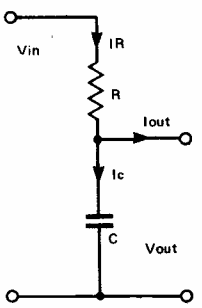


Fig. 2. Basic integrator.

Integrators

The basic integrator circuit is very similar to that of the differentiator — the resistor and capacitor just swap positions (Fig. 2). Now we can find the circuit's action in the same way as we did before;

$$I_C = C\frac{dV_{OUT}}{dt}.$$

Integrating both sides of the equation;

$$\int I_C dt = CV_{OUT}.$$

But I_C is the same as I_R, provided we are driving a load with high enough input impedance. From Ohm's law, we have $I_R = V_R/R$, and thus;

$$1/R \int V_R dt = CV_{OUT}.$$

Dividing both sides by C;

$$V_{OUT} = 1/RC \int V_R dt.$$

Again, the voltage being integrated is the voltage across only one of the components — the resistor — and not that across the entire circuit. However, as long as we again arrange that V_{OUT}, that is, V_C, never gets *too* large, V_R is very close to V_{IN}, and we have a fair approximation to an integrating circuit with a gain of $1/RC$. ▶

Bigger and Better

So far, the circuits we have looked at have had two main disadvantages; they are accurate only when driving circuits which have very high input impedances, and their output voltages cannot be allowed to become very large, or the difference between the input voltage and the voltage actually being acted on becomes too large to be ignored. (This in turn puts resistrictions on the allowable values of RC time constants and thus the components themselves, but we won't go into that.) How can these problems be solved? Did the man at the back mention op-amps? Dead right, friend. To see how they might be useful, however, let's do a quick bit of revision on them. (Those familiar with op-amps skip the next section.)

Op-Amps

Op-amps are famed for three major properties. The first of these is a very high input impedance, the second is a very low output impedance and the third is a gain so high that it may be approximated to infinity without too much innaccuracy for most purposes. It is this last property which leads to the 'virtual earth', a very useful concept in analysis of op-amp circuits.

The voltage gain of an amplifier is, by definition, the ratio of its output voltage to its input voltage. If the gain is m, then the output voltage V_{OUT} is mV_{IN}, or, if we are using the inverting input of an amplifier, $-mV_{IN}$. However, as we have stated, the gain of an op-amp is close to infinity. Thus, its output voltage is infinity times its input voltage, or, putting it another way, the input voltage is equal to the output voltage divided by infinity. Since the output voltage must be finite, the input voltage, or, more accurately, the difference in voltage between the inverting and non-inverting inputs, of an op-amp, must be zero. (Yes, I know it looks as though I've cheated somewhere, but I can assure you that it works.) Since this difference in voltage is zero, it follows that if we ground one input of an op-amp, the other input automatically goes to zero potential. This is not to say that it automatically gets shorted to earth — there is still a very high resistance between the two points — it just means that no voltage will be present; there is a 'virtual earth'. This concept, as has been stated, is a very useful one. Now we can apply it to our integrator and differentiator circuits.

The New Improved . . .

We saw in the last section that an op-amp has a very high input impedance and a very low output impedance. It was a very high input impedance, you will remember, that we needed for our basic circuits to drive, so suppose we put some sort of unity gain voltage amplifier on the outputs. It wouldn't affect the signal in any way, but it would mean that we could drive circuits with lower input impedances.

Well, using an op-amp, a unity gain voltage amplifier has a circuit something like that shown in Fig. 3. It's easy enough to understand; the output is shorted to the inverting input and so the voltage present at each is identical. However, the difference in voltage between the two inputs must be zero and so the same voltage is

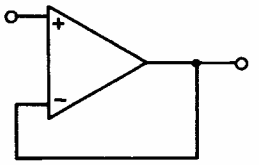


Fig. 3. Unity gain voltage amplifier.

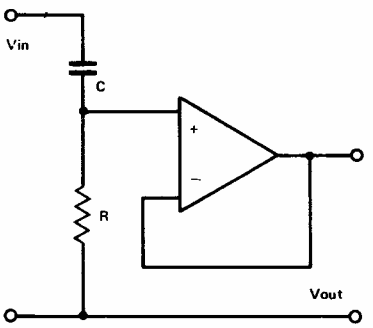
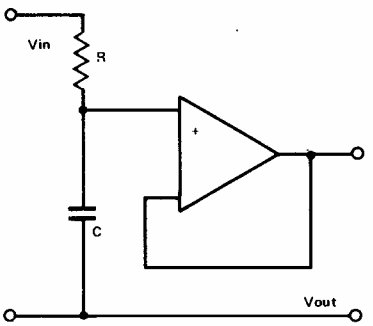


Fig. 4 a Differentiator with buffer.



b Integrator with buffer.

present at the input to the amplifier as is at the output. In practice, this means that the output voltage follows the input voltage. Amplifiers like this are often used as 'buffers' — allowing high output impedance circuits to drive low input impedance ones.

If we put one of these buffer amplifiers on the output of each of our circuits, we have the circuits shown in Fig. 4, and we have, indeed, solved one of our major problems; the circuits no longer need to drive into high impedances. The other problem is still present, however. Is it possible to improve our circuits again? Well, yes. (See, it was worth reading this far.)

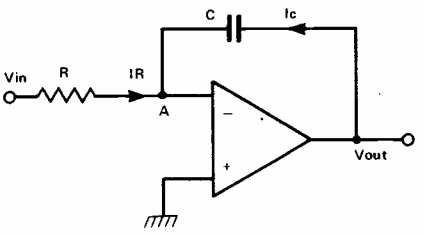
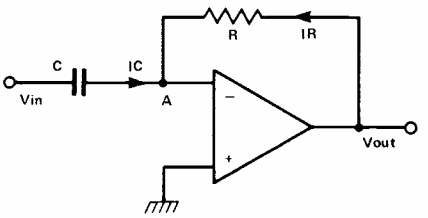


Fig. 5a (above) Integrator circuit using an op-amp and b (below) differentiator circuit using an op-amp.



At Last . . .

We'll look at the integrator first. The circuit is shown in Fig. 5a, and, unlike our last idea, does not use an op-amp tacked onto the end, but as an integral part of the circuit. (Yes, that's right, it's an integrated integrator . . . sorry, I just couldn't resist that. . .) It's action is as follows:

Since the input impedance of the op-amp is very high, it follows that the current actually flowing into it is very small, and hence, $I_R = -I_C$, to a first approximation, in order to keep the currents flowing into point A sum to zero. (Kirchhoff's first law — the algebraic sum of all the currents flowing into a point of a network is zero. This is the same as saying current in = current out.)

However, Ohm's law tells us that the current flowing through the resistor is given by the voltage across it, divided by the resistance. Now, the voltage at A is zero (virtual earth), so the current through the resistor is V_{IN}/R. The current through the capacitor is given by

$$I_C = C\frac{dV_{OUT}}{dt}$$

Hence, we have, since current through the resistor equals current through capacitor;

$$V_{IN}/R = -C\frac{dV_{OUT}}{dt}$$

$$\text{and so } V_{IN}/RC = -\frac{dV_{OUT}}{dt}$$

Integrating both sides of the equation, we obtain;

$$\frac{V_{IN}}{RC}dt = -V_{OUT} \text{ or } V_{OUT} = -1/RC \int V_{IN}dt.$$

Since R and C are constants, and can thus be moved out of the integration sign.

Hence we have effectively a circuit which integrates input voltage with respect to time, and which has, once again, a gain given by $-1/RC$. The integrating action may be seen if we apply a square wave to the input. We obtain a triangular wave as output, and one which compares very favourably with that obtained from our original circuit. (Fig. 6.)

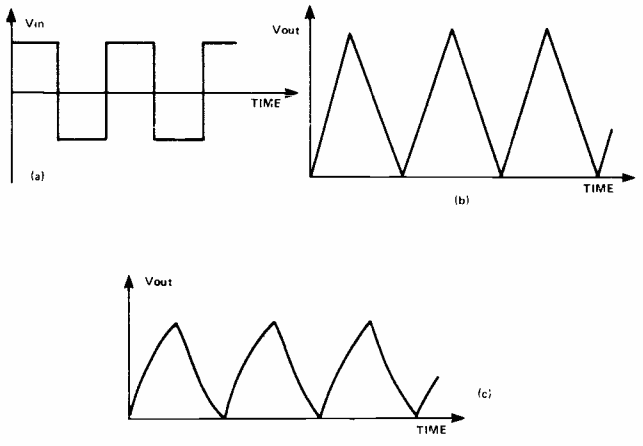


Fig. 6a Input square wave signal B output from op-amp circuit c output from original circuit.

Differentiator Mark 3

The action of the differentiator circuit (Fig. 5b) can be explained similarly. Again, current through the resistor is equal to that through the capacitor, because of the very high input impedance of the op-amp.

$$I_C = -I_R$$

But I_R is given by $(V_{OUT}-V_A)/R$ and V_A is zero (virtual earth again). Similarly, I_C is given by CdV_{IN}/dt. Therefore;

$$V_{OUT}/R = -C\frac{dV_{IN}}{dt}$$

multiplying both sides of the equation by R, we get;

$$V_{OUT} = -RC\frac{dV_{IN}}{dt}$$

And we have a differentiating circuit, the gain of which is given by —RC. We can see the differentiating action if we apply a square wave to the circuit as in Fig. 7.

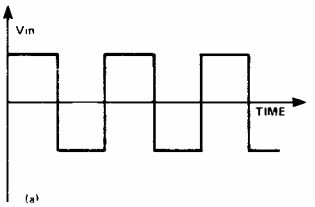
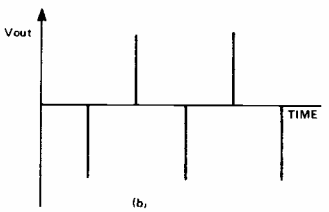


Fig. 7a (above) Input square wave signal and b (below) output from op-amp circuit.



Howzat!

With these two circuits we have overcome the difficulties experienced with our original RC combination series circuits. The voltage being acted on is the input voltage actually and, thanks to the low output impedance of the op-amp, we can use these circuits to drive many more circuits. The output voltage, which we were forced to restrict in our original circuits, for fear of affecting the action of the circuits, is now restricted only by the supply voltage to the op-amps.

The outputs of these circuits are, of course, inverted, as is shown by the minus signs in our equations. This is because of practical difficulties incurred when a non-inverting circuit is used, and can easily be solved by tacking a unity gain inverting voltage amplifier onto the output — surely a small price to pay for all the advantages that these circuits give us over the originals. ●

ELECTRONIC SPEED CONTROL FOR MOTORS

How various types of motor can be controlled in speed using semiconductor devices,

Applications Department, Motorola, Phoenix.

Speed control of motors in domestic appliances has been technically possible for a long time, but only recently has it become a good proposition economically.

Such diverse items as blenders, furnace blowers, clothes dryers, and food mixers can now use electronic controls. In this article, we review some of the common circuits being used today, and also describe some of the new circuits.

By far the easiest to control electronically are universal (or series-wound ac-dc) motors. Their characteristics and construction allow the use of a simple circuit to provide an electrical feedback so that speed is held relatively constant under varying load conditions.

Permanent-magnet motors are also easy to control. Perhaps surprisingly, the speed of several forms of induction motors may also be successfully controlled by electronic means – if these motors have a suitable load.

How AC power control

The most common method of electronic ac power control is called phase control.

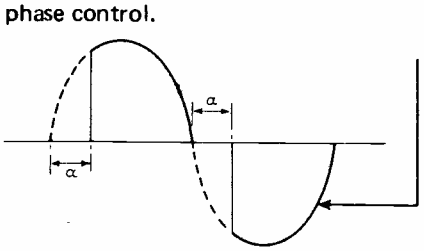


Fig.1. Illustrating the basic principles of phase control. The portion of the waveform applied to the load is shown shaded.

Figure 1 illustrates this concept. During the first portion of each half-cycle of the ac sine wave, an electronic switch is opened to block current flow. At some specific phase angle, *a*, this switch is closed to allow the full line voltage to be applied to the load for the remainder of that half-cycle. Varying *a* will control the portion of the total sine wave that is applied to the load (shaded area), and thereby regulate the power flow to the load.

The simplest circuit for accomplishing phase control is shown in Fig. 2. The electronic switch in this case is a triac *(Q)* which can be turned ON by a small current pulse to its gate. The triac turns OFF automatically when the current through it passes through zero.

In the circuit shown capacitor C_T is charged during each half-cycle by the current flowing through resistor R_T and the load. The fact that the load is in series with R_T during this portion of the cycle is of little consequence since the resistance of R_T is many times greater than that of the load. When the voltage across C_T reaches the breakdown voltage of the trigger diode (D), the energy stored in capacitor C_T is released. This energy produces a current pulse in the trigger diode, which flows through the gate of the triac and turns it ON. Since both the trigger diode and the triac are bidirectional devices, the values of R_T and C_T will determine the phase angle at which the triac will be triggered in both the positive and negative half-cycles of the ac sine wave.

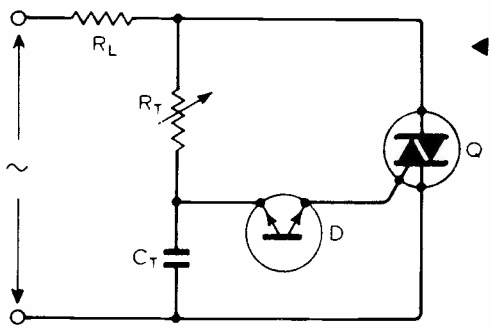


Fig.2. The simplest possible circuit for phase control. The load is represented by resistor R_L.

The wave form of the voltage across the capacitor for two typical control conditions (a = 90° and 150°) is shown in Fig. 3. If a silicon controlled rectifier is used in this circuit in place of the triac, only one half-cycle of the wave form will be controlled. The other half-cycle will be blocked, resulting in a pulsing dc output whose average value can be varied by adjusting R_T.

Characteristics of semiconductor switches

The silicon controlled rectifier (SCR) was the first of several thyristors developed for controlling electric power efficiently. It blocks current flow in both directions as long as no gate signal is applied and the applied voltage is below the rated breakover voltage. Exceeding the breakover voltage in the forward direction (with anode more positive than cathode) will cause the SCR to switch to its ON condition, in which the voltage from anode to cathode is approximately 1 V (and the current is limited only by the external circuitry). When the forward current is interrupted, the SCR recovers its blocking character.

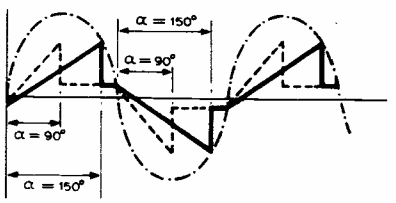


Fig.3. Waveforms across the capacitor at two different phase angles. The applied sine wave is shown dotted.

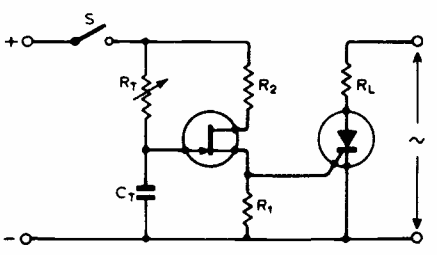


Fig.4. A typical phase control circuit using a unijunction transistor firing circuit.

Exceeding the reverse breakdown voltage of an SCR will destroy the device, most often causing a permanent short circuit.

Current flowing into the gate of an SCR will also cause it to turn ON when forward voltage is applied. Since the SCR is a regenerative device (that is, it remains in the ON condition as long as anode current is flowing), only a current pulse at the gate is necessary to effect switching. Thus, in the previously described circuits, a properly timed current pulse into the gate of an SCR can control average power flow to a load.

The triac is a bidirectional SCR. It is designed for use with alternating current, and functions the same way in both directions of applied voltage (as an SCR does in the forward direction). Its gate characteristics are different from that of an SCR in that gate current of either polarity will cause the triac to turn ON, with either polarity of applied anode voltage.

The trigger diode is a device designed specifically to provide current pulses to trigger SCR or triacs. In use, it acts much like a triac without a gate. That is, it will block current flow in either direction as long as the applied voltage is below the breakover voltage, which is generally between 16 and 36 V, depending on the device type. When the breakover voltage is exceeded, the device turns ON. In this state, the current is limited by the external circuitry, and the voltage drop across the diode is about 10 to 15 V. The trigger diode is most commonly used in circuits similar to the one shown in Fig. 2.

The unijunction transistor (UJT) is a three-terminal trigger device in which the characteristics of the emitter and base 1 are very much like those of the trigger diode. However, its breakover voltage can be controlled by the power supply voltage applied between base 1 and base 2. Since the UJT is a unidirectional device, unlike the bidirectional trigger diode, it requires a source of direct current for the interbase voltage as well as for the timing-circuit components, R_T and C_T. Figure 4 shows a UJT in a typical control circuit.

Because the breakover voltage of the UJT emitter is controlled by the interbase voltage, the unijunction transistor can be used for the timing circuit with a much lower source voltage than can be trigger diode, whose breakover voltage is controlled by the parameters of its structural materials. As a result, the UJT is quite popular for use with electronic control systems utilizing feedback.

In many applications it is desirable to vary motor speed in proportion to the magnitude of a change in a physical condition, such as a change in temperature. A furnace blower responding to the air temperature of a house is one example. Similarly, a control device can light a lamp in response to the fading twilight. Control of these circuits can be effected by resistors that change in value in response to a change in temperature or light intensity. A typical circuit using such a variable resistor is shown in Fig. 5. If motor speed is the quantity to be controlled, R_S may be a fixed resistor, and a direct-current tachometer generator may be inserted as shown. Only a few additional components are necessary to turn these elementary circuits into working modules.

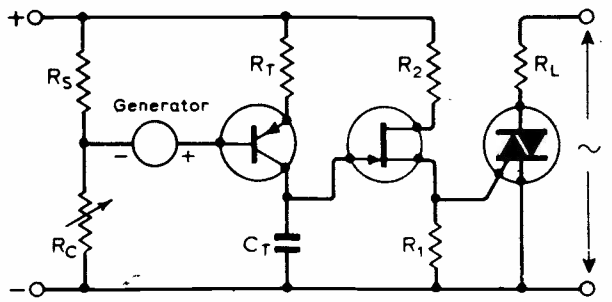


Fig. 5 Motor speed control with a unijunction transistor using feedback.

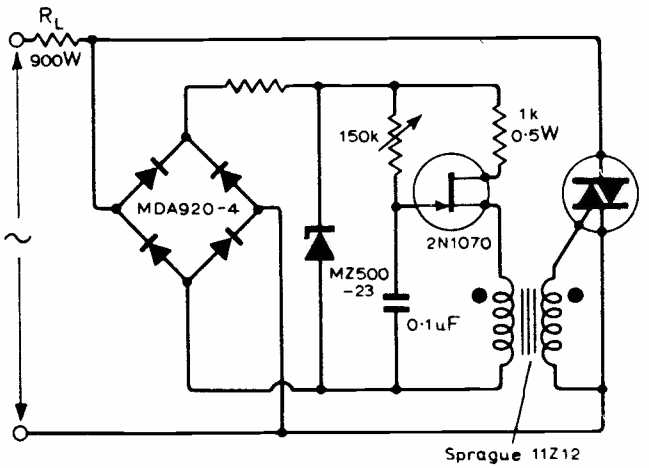


Fig. 6 Simple full-wave trigger circuit for a 900 W resistive load.

Figure 6 shows a simple full-wave trigger circuit for controlling a 900 W load. The additional components required are a full-wave bridge, a resistor, and a Zener diode, which make up the dc power supply, and a pulse transformer which provides the isolation between the UJT circuit and the power line, necessitated by the bridge rectifier. The feedback circuitry shown in Fig. 5 could also be added to this circuit.

Control of induction motors

Shaded-pole motors driving low-starting-torque loads such as fans and blowers may readily be controlled using any of the previously described full-wave circuits. One needs only to substitute the winding of the shaded-pole motor for the load resistor shown in the circuit diagrams.

Constant-torque loads or high-starting-torque loads are difficult, if not impossible, to control using the voltage controls described here. Figure 7 shows the effect of varying voltage on the speed-torque curve of a typical shaded-pole motor. A typical fan-load curve and a constant-torque-load curve have been superimposed upon this graph. It is not difficult to see that the torque developed by the motor is

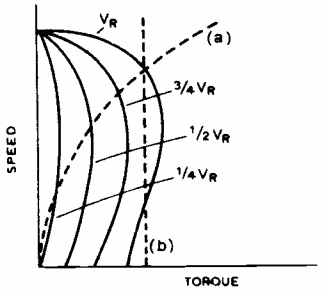


Fig. 7 Characteristics of a shaded pole motor at several voltages. V_R is the full rated voltage, (a) indicates a typical fan load and (b) shows a constant torque load.

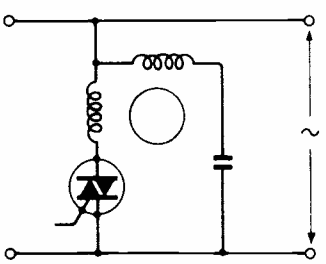


Fig. 8 Connection diagram for permanent split capacitor motors.

equal to the load torque at two different points on the constant-torque-load curve, giving two points of equilibrium and thus an ambiguity to the speed control. The equilibrium point at the lower speed is a condition of high motor current because of low counter emf and would result in burnout of the motor winding if the motor were left in this condition for any length of time. By contrast, the fan speed-torque curve crosses each of the motor speed-torque curves at only one point, therefore causing no ambiguities. In addition, the low-speed point is one of low voltage well within the motor winding's current-carrying capabilities.

Permanent-split-capacitor motors can also be controlled by any of these circuits, but more effective control is achieved if the motor is connected as shown in Fig. 8. Here only the main winding is controlled and the capacitor winding is continuously connected to the entire ac line voltage. This connection maintains the phase shift between the windings, which is lost if the capacitor phase is also controlled. Figure 9(a) shows the effect of voltage on the speed-torque characteristics of this motor and a superimposed fan-load curve.

Not all induction motors of either the shaded-pole or the permanent-split-capacitor types can be controlled effectively using these techniques, even with the proper loads.

Motors designed for the highest efficiences and, therefore, low slip also have a very low starting torque and may, under certain conditions, have a speed-torque characteristic that could be crossed twice by a specific fan-load speed-torque characteristic.

Figure 9(b) shows motor torque-speed characteristic curves upon which has been superimposed the curve of a fan with high starting torque. It is therefore desirable to use a motor whose squirrel-cage rotor is designed for medium-to-high impedance levels and, therefore, has a high starting torque. The slight loss in efficiency of such a motor at full rated speed and load is a small price to pay for the advantage of speed control.

A unique circuit for use with capacitor-start motors in explosive or highly corrosive atmospheres, in which the arcing or the corrosion of switch contacts is severe and undesirable, is shown in Fig. 10. Resistor R_1 is connected in series with the main running winding and is of such a resistance that the voltage drop under normal full-load conditions is approximately 0.2 V peak. Since starting currents on these motors are quite high, this peak voltage drop will exceed 1 V during starting conditions, triggering the triac, which will cause current to flow in the capacitor winding. When full speed is reached, the voltage across the main winding will decrease to about 0.2 V, which is insufficient to trigger the triac – thus the capacitor winding will no longer be energized. Resistor *R2* and capacitor C_2 form a dv/dt suppression network; this prevents the triac from turning on due to line transients and inductive switching transients.

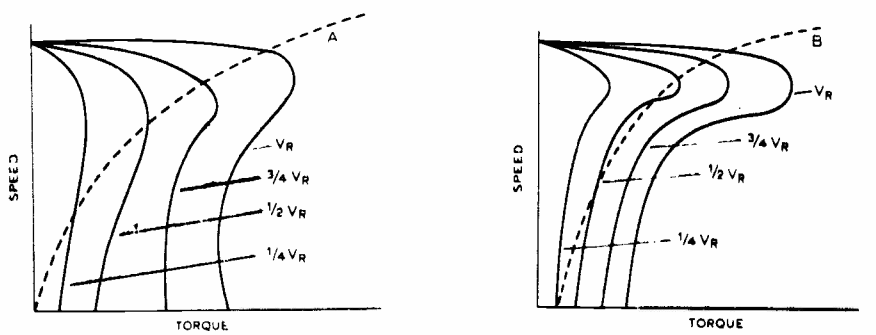


Fig. 9 Speed-torque curves for (A) high starting torque and (B) high efficiency permanent split capacitor motors at several voltages. The dotted line indicates a typical fan load and V_R is the full rated voltage.

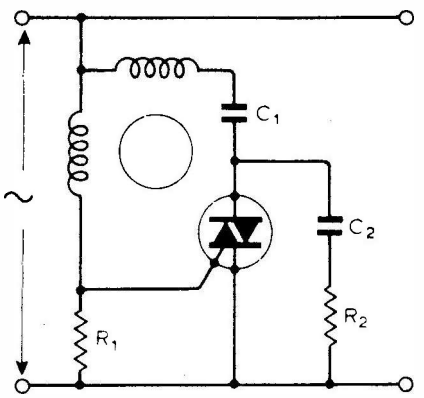


Fig. 10 Circuit diagram for a capacitor start motor.

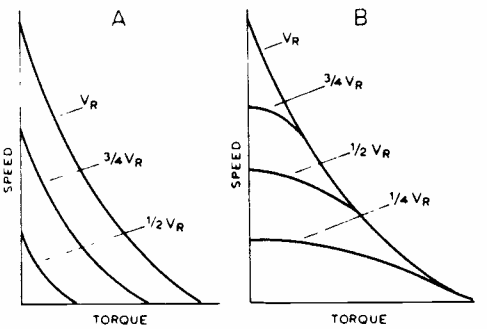


Fig. 11 Speed control, with (A), and without (B). feedback, compared.

Control of universal motors

Any of the half-wave or full-wave controls described previously can be used to control universal motors. Non feed-back, manual controls, such as those shown in Fig. 2, are simple and inexpensive, but they provide very little torque at low speeds. A comparison of typical speed torque curves using a control of this type with those of feedback control is shown in Fig. 11.

These motors have some unique characteristics which allow their speed to be controlled very easily and efficiently with a feedback circuit such as that shown in Fig.12. This circuit provides phase-controlled half-wave power to the motor: that is, on the negative half-cycle, the SCR blocks current flow in the negative direction causing the motor to be driven by a pulsating direct current whose amplitude is dependent on the phase control of the SCR.

The theory of operation of this control circuit is not at all difficult to understand. Assuming that the motor has been running, the voltage at point A in the circuit diagram (Fig.12) must be larger than the forward drop of diode D_1, the gate-to-cathode drop of the SCR, and the emf generated by the residual (magneto-motive force) in the motor, to get sufficient current flow to trigger the SCR.

The waveform at point A(V_A,) for one positive half-cycle is shown in Fig.13, along with the voltage levels of the SCR gate (V_{scr}), the diode drop (V_D), and the motor-generated emf (V_M). The phase angle (*a*) at which the SCR would trigger is shown by the vertical dotted line. Should the motor for any reason speed up so that the generated motor voltage would increase, the trigger point would move upward and to the right along the curve so that the SCR would trigger

later in the half-cycle and thus provide less power to the motor, causing it to slow down again.

Similarly, if the motor speed decreased, the trigger point would move to the left and down the curve, causing the triac to trigger earlier in the half-cycle providing more power to the motor, thereby speeding it up.

Resistors R_1, R_2 and R_3, along with diode D_2 and capacitor C_1 form the ramp-generator section of the circuit, as shown in the diagram in Fig.12. Capacitor C_1 is charged by the voltage divider R_1, $R2$ and R_3 during the positive half-cycle. Diode D_2 prevents negative current flow during the negative half-cycle, therefore C_1 discharges through only R_2 and R_3 during that half-cycle. Adjustment of R_3 controls the amount by which C_1 discharges during the negative half-cycle. Because the resistance of R_1 is very much larger than the ac impedance of capacitor C_1, the voltage waveform on C_1 approaches that of a perfect cosine wave with a dc component. As potentiometer R_2 is varied, both the dc and the ac voltages are divided, giving a family of curves as shown in Fig.14.

The gain of the system, that is, the ratio of the change of effective SCR output voltage to the change in generator emf is considerably greater at low speed settings than it is at high speed settings. This high gain coupled with a motor with a very low residual emf will cause a condition sometimes known as cycle skipping. In this mode of operation, the motor speed is controlled by skipping entire cycles or groups of cycles, then triggering one or two cycles early in the period to compensate for the loss in speed. Loading the motor would eliminate this condition; however, the undesirable sound and vibration of the motor necessitate that this condition be eliminated. This can be done in two ways.

The first method is used if the motor design is fixed and cannot be changed. In this case, the impedance level of the voltage divider R_1, R_2 and R_3 can be lowered so that C_1 will charge more rapidly, thus increasing the slope of the ramp and lowering the system gain. The second method, which will provide an overall benefit in improved circuit performance, involves a redesign of the motor so that the residual emf becomes greater. In general, this means using a lower grade of magnetic steel for the laminations. As a matter of fact, some people have found that ordinary cold-rolled steel used as rotor laminations makes a motor ideally suited for this type of electronic control.

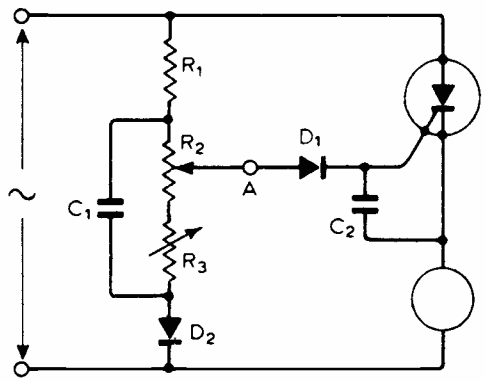


Fig. 12 Speed control scheme for universal motors.

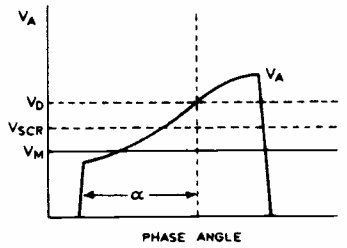


Fig. 13. Waveform for one positive half cycle in the circuit shown in Fig. 12.

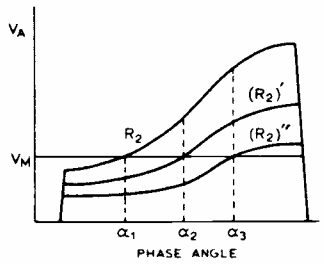


Fig. 14. Voltage waveform at point A (Fig. 12) for three different settings of R_2.

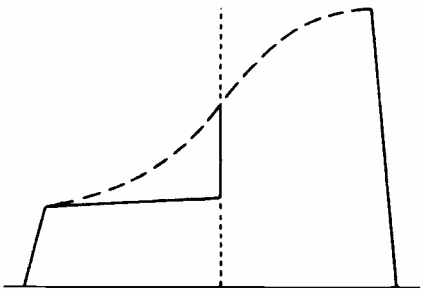


Fig. 15 When resistor R1 (Fig. 12) is too large, this voltage waveform appears at point. A. The dotted line is the unloaded waveform and the unbroken line is the actual waveform.

Another common problem encountered with this circuit is that of thermal runaway. With the speed control set at low or medium speed, at high ambient temperatures the speed may increase uncontrollably to its maximum value. This phenomenon is caused by an excessive impedance in the voltage divider chain for the SCR being triggered. If the voltage-divider current is too low, current will flow into the gate of the SCR without turning it on, causing the waveform at point A to be as shown in Fig.15. The flat portion of the waveform in the early part of the half-cycle is caused by the SCR gate current loading the voltage divider before the SCR is triggered. After the SCR is triggered, diode D_1 is back-biased and a load is no longer on the voltage divider so that it jumps up to its unloaded voltage. As the ambient temperature increases, the SCR becomes more sensitive, thereby requiring less gate current to trigger, and is triggered earlier in the half-cycles. This early triggering causes increased current in the SCR thereby heating the junction still further and increasing the sensitivity of the SCR until maximum speed has been reached.

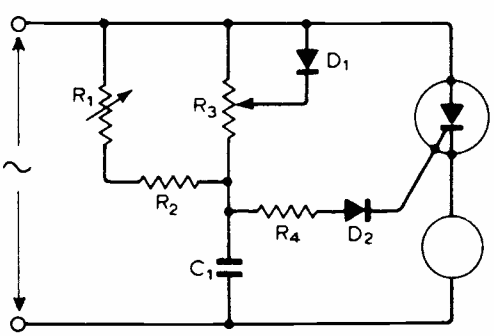


Fig. 16 Speed control of permanent magnet d.c. motors.

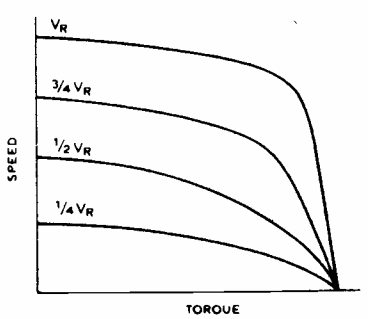


Fig. 17 Speed-torque characteristic of permanent magnet motors at various applied voltages.

The solutions to this problem are the use of the most sensitive SCR practical and a voltage divider network of sufficiently low impedance. As a rough rule of thumb, the average current through the voltage divider during the positive half-cycle should be approximately three times the current necessary to trigger the lowest sensitivity (highest gate current) SCR being used.

In addition to the type of steel used in the motor laminations, consideration should also be given to the design of motors used in this half-wave speed control. Since the maximum rms voltage available to the motor under half-wave conditions is less than for full-wave, the motor should be designed for use under these conditions to obtain maximum speed.

CONTROL OF PERMANENT MAGNET MOTORS

As a result of recent developments in ceramic permanent-magnet materials that can be easily moulded into complex shapes at low cost, the permanent-magnet motor has become increasingly attractive as an appliance component. Electronic control of this type of motor can be easily achieved using techniques similar to those just described for the universal motor. Figure 16 is a circuit diagram of a control system to control permanent-magnet motors presently being used in blenders. Potentiometer R_3 and diode D_1 form a dc charging path for capacitor C_1; variable resistor R_1 and resistor R_2 form an ac charging path which creates the ramp voltage on the capacitor. Resistor R_4 and diode D_2 serve to isolate the motor control circuit from the ramp generator during the positive and negative half-cycles, respectively.

A small amount of cycle skipping can be experienced at low speeds using this control, but not enough to necessitate further development work. Since the voltage generated during off time is very high, the thermal runaway problem does not appear at all.

HEATER CONTROL AND TIMERS

The circuit shown in Fig.2 or 3 could well be made to control heaters in domestic appliances without any modifications.

If the capacitor C_T in Fig.3 is made very large a timer results. The time delay is set by the value of C_T and the variable resistor R_T. ●

OP AMPS

In this down-to-earth series, J. T. Neil explains the basic theory and practical applications of op amps.

Operational amplifiers are small in size, provide very high, stable voltage gains, and are readily available at well under 50p each.

Unfortunately these immensely practicable devices tend to be described by their manufacturers and countless technical writers in terms that are virtually meaningless to the home constructor.

The purpose of this short series of three articles then, is to show, with the minimum of theory and mathematics, how to extract the essential information from data sheets and how to apply it to practical designs.

The units to be described, each using a single operational amplifier, are a compact sine-wave audio-signal generator, a high-impedance audio amplifier (with various switched frequency-responses available) and a dc amplifier to increase the effective sensitivity of an ordinary 1 mA meter to 10 μA fsd.

Each of these units can be run from batteries or any other suitable source; however, since operational amplifiers usually require dual supplies (which could become expensive if batteries were used for long) the first actual constructional project will be a power supply unit giving ± 12 V fully stabilised and short-circuit protected. This latter feature is rather important, for the operational amplifiers to be used have their lead out wires only 2.5 mm apart which, in experimental setups, will, sooner or later, lead to short circuits of the supply rails by solder blobs, touching wires etc.

Accordingly, a protected power supply, specifically designed for use with op amps and which automatically reverts to correct operation on removal of an unwanted short-circuit is essential.

WHAT IS AN OPERATIONAL AMPLIFIER?

Originally, the term was used to describe an amplifier suitable for performing mathematical operations in analogue computers. It has since come to include almost any high-gain dc amplifier capable of having its actual performance, in terms of gain, frequency response and input impedance, determined by external components arranged to provide feedback (usually negative feedback).

An *ideal* op. amp. has the following characteristics:–

1., Infinite gain
2. Infinite bandwidth
3. Infinite input impedance
4. Zero output impedance
5. Constant phase shift between input and output.

Obviously, such a device is impossible in the real world, but it *is* possible to manufacture amplifiers that have gains etc. So large, and output impedances so low, that any departures from the ideal have little effect in practical circuits.

For example, if a working gain of 100 is required and the op. amp. to be used has a gain (without feedback) of 50 000 then 50 000 ÷ 100 (500) is such a large margin that we can say that, for practical purposes, the reserves of gain available are so large that the gain is infinite. Similar reasoning applies to the other parameters whose ideal values were mentioned earlier.

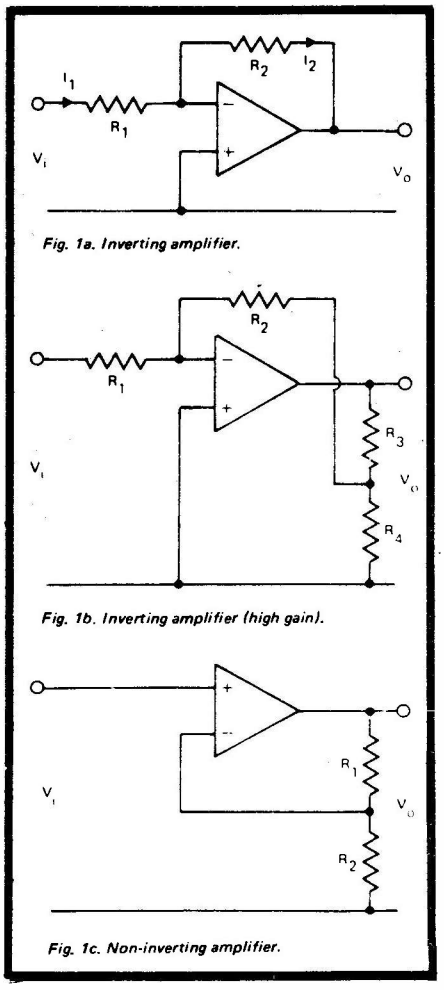


Fig. 1a. Inverting amplifier.

Fig. 1b. Inverting amplifier (high gain).

Fig. 1c. Non-inverting amplifier.

FEEDBACK

Operational amplifiers are most often arranged to function with negative feedback applied, although there are cases where either no feedback, or indeed *positive* feedback, is employed. The op. amps. we shall be considering have, in fact, two input terminals, and feedback is considered to be either negative or positive according to which of these inputs it is connected.

The two input terminals are arranged in the following manner. Consider that one input terminal is earthed; then if the application of a positive going signal to the other input results in a *positive* going output signal, then that latter input terminal is termed the "+ ve" input terminal. Conversely, again with one input earthed, if the application of a positive going signal to the other input results in a *negative* going output signal, then that latter input terminal is termed the "–ve" input terminal. Sometimes the +ve input is called the "non phase inverting" input and the –ve input is called the "phase inverting" input.

By convention, the op. amp. itself is shown as a triangle, with the output being taken from the righthand apex; the two inputs are on the left, one input being the –ve and the other the +ve.

The arrangement of Fig. 1a will result in a phase reversal of the signal, while that of Fig. 1c will not. Accordingly, the first configuration is called an "inverting amplifier" and the second a "non-inverting amplifier".

TERMINOLOGY

Op. Amps have their own terminology which need expanation. These are frequently used when dealing with op. amps and without explanation could cause confusion. The terms are necessary because these devices do not have the ideal characteristics referred to earlier.

Open loop gain is the voltage gain of the amplifier at low frequencies with no feedback applied, ie with the feedback loop open. The value of 50,000 used as an example earlier is the open loop gain of the amplifier discussed.

Closed loop gain is the voltage gain of the amplifier when negative feedback is applied, ie with the feedback loop completed. It is thus the gain of the whole circuit and is analogous to the stage gain of valve and discrete-transistor circuits. The value of x2 we use below is the closed loop gain in that case.

Input bias current is that current that must be fed into the input terminals in order to make the output voltage zero. The current is necessary since the input transistors of the op. amp require some base current, however small, in order for them to conduct and so amplify.

Input Offset Voltage is that voltage that must be applied across the input terminals to make the output voltage zero. It is not usually as important as input bias current in the type of application that we shall be considering.

Common Mode Rejection is a measure of how good the amplifier is in rejecting signals applied to both inputs together. Once again, we will not need to pay great attention to this characteristic in our applications.

Frequency Response is usually quoted by stating the frequency at which the voltage gain falls to unity; it is then normally assumed that, as the frequency is reduced, the gain rises at a rate of 20dB per decade (i.e. the voltage gain rises by a factor of 10 for a ten-fold change in frequency) until it reaches the open loop value. It is then possible, with a knowledge of the open loop gain, to sketch the frequency response, see Fig. 2. Operational amplifiers have a response down to zero frequency, that is, they are dc amplifiers.

Towards the top end of the frequency range, slewing rate becomes important.

Slewing rate is the fastest rate of change of output voltage that the op. amp. can generate. Provided that the output voltage swing is small, say 1V peak-to-peak, the slewing rate limitation is unlikely to be a problem, even at a frequency close to the op. amp's maximum. However, if a large output voltage swing is called for, say 20V peak-to-peak at the same frequency, then slewing rate limitation can give rise to distortion; for clearly, at the zero crossing a large-amplitude signal will be changing its voltage as a faster rate than a signal of smaller amplitude.

For example the popular 741 IC may have a bandwidth of 100kHz to a small signal but the maximum slew rate of 1 volt/microsecond will limit bandwidth to 10kHz, if an output swing of 20V peak-to-peak or more is required, or to 40kHz at four volts peak-to-peak.

Slew rate thus limits the ultimate output swing available at high frequencies and is also a source of high-frequency distortion at high output levels.

The use of negative feedback will not cure the distortion for it is inherent in the op. amp. itself.

Each configuration has its own properties, which we shall now consider.

INVERTING AMPLIFIERS

Referring to Fig. 1c, consider an input, V_i at, say 1 kHz. Imagine that the input resistance of the op. amp. itself is so large compared to the values of R_1 and R_2 that it can be said to be infinite. This will be the case if R_1 is, say, 1 k, for the input resistance of a typical op. amp. is 1 M. Imagine also that the gain of the op. amp. is very much larger than the final gain of the whole circuit. Once again this will be so, for the gain of a typical op. amp. is 50 000 and the overall gain of the whole circuit will be very much less than this extremely high value, as will be shown.

This latter assumption is very important, for it means that the actual level of signals at the –ve input terminal will be so close to nothing that we can consider it to be zero. By Ohm's Law

$$I_1 = \frac{V_1}{R_1} = I_2 = \frac{V_2}{R_2}$$

where

V_1 is voltage across R_1

V_2 is voltage across R_2

But with zero signal at the –ve input

$V_1 = V_i$ and $V_2 = V_o$

so that the gain, A, is

$$A = \frac{V_o}{V_i} = \frac{V_2}{V_i} = \frac{R_2}{R_1}$$

which is independent of the actual gain of the op. amp., provided that the latter is very much larger than the value of A – very likely in practice.

It will be instructive at this point to consider the level of signal actually present at the –ve input of the op. amp. With an input signal of 1 volt and a circuit gain of x2, there will be an output of 2 volts. If the op amp gain is 50 000, then the level at the –ve input must be

$$\frac{2}{50\,000} .1 = 40\ \mu V,$$

quite close to the zero level assumed.

Note that when the amplifier output is fed back to the –ve input, the output voltage adjusts itself to such a value that the actual voltage between the two inputs becomes so close to zero that the difference can be neglected. The greater the gain of the op amp itself, i.e. the better it approximates to the ideal of infinite gain, the less the voltage at the –ve input becomes.

Since the –ve input has such a low level signal present, it is virtually at earth potential, and consequently the input resistance of the whole circuit is equal to R_1. Such an arrangement as illustrated in Fig. 1a is sometimes called a "virtual earth amplifier".

If a very high value of gain is required, complications can arise if a high input impedance is called for at the same time, for if R_2/R_1 is large, either R_2 will need to be such a high value that it is impracticable or R_1 will be too low for the required input impedance.

In that case, the configuration of Fig. 1b can be used. An analysis of this circuit gives, for the voltage gain

$$A = \frac{R_2}{R_1} \cdot \frac{(R_3 + R_4)}{R_4}$$

provided that R_2 is large compared to R_4.

Now R_1 can be kept at a reasonably high value (to raise the input impedance) with R_3 and R_4 making up the gain to the required level).

NON-INVERTING AMPLIFIERS

Now consider the non-inverting amplifier of Fig. 1c. As before, imagine that, due to the high gain of the op. amp., there is virtually zero signal between the two inputs and that the input resistance of the amplifier is very much greater than either R_1 or R_2.

Then $V_2 = V_i$ where V_2 is the voltage across R_2

$$\text{But } V_2 = \frac{R_2}{(R_1 + R_2)} . V_o$$

$$\therefore V_o = \frac{R_1 + R_2}{R_2} \cdot V_2$$

so that gain A is

$$A = \frac{V_o}{V_i} = \frac{(R_1 + R_2)}{R_2} \cdot \frac{V_2}{V_2} = \frac{(R_1 + R_2)}{R_2}$$

which again is independent of the actual gain of the op. amp. itself.

The input resistance of a non-inverting amplifier is very high, being determined largely by the impedance from the two input terminals to earth. Typically, it is of the order of 200 – 400 M at low and medium gain levels. It is this extremely high value of resistance that makes the non-inverting amplifier so useful, although, of course, there are disadvantages. For example, it might appear that a non-inverting amplifier would be ideal to accept the output from a high resistance source, but in

that case the resistance seen by the op. amp +ve input would be that source resistance, while the resistance seen by the –ve input will be R_1 and R_2 in parallel (Fig. 1c). The input bias currents (see later) at each input would then give rise to a voltage difference across the inputs and hence, of course, unwanted voltage offset at the output.

These two circuit configurations, namely, the inverting and the non-inverting, form the basis of all op amp circuitry and are well worth remembering. In a number of uses, the simple resistors used in the examples quoted are replaced by complex impedances of one kind or another in order to modify the frequency response in some way. By such means it is possible to make op amps respond as frequency selective amplifiers, integrators etc.

Examples of this tailoring of frequency responses will arise in the case of the audio amplifier to be described in part 3.

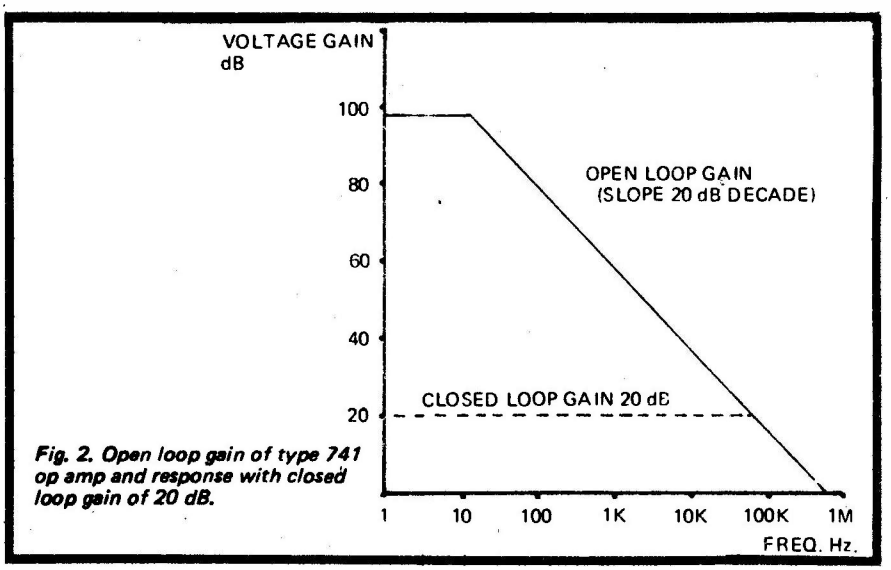
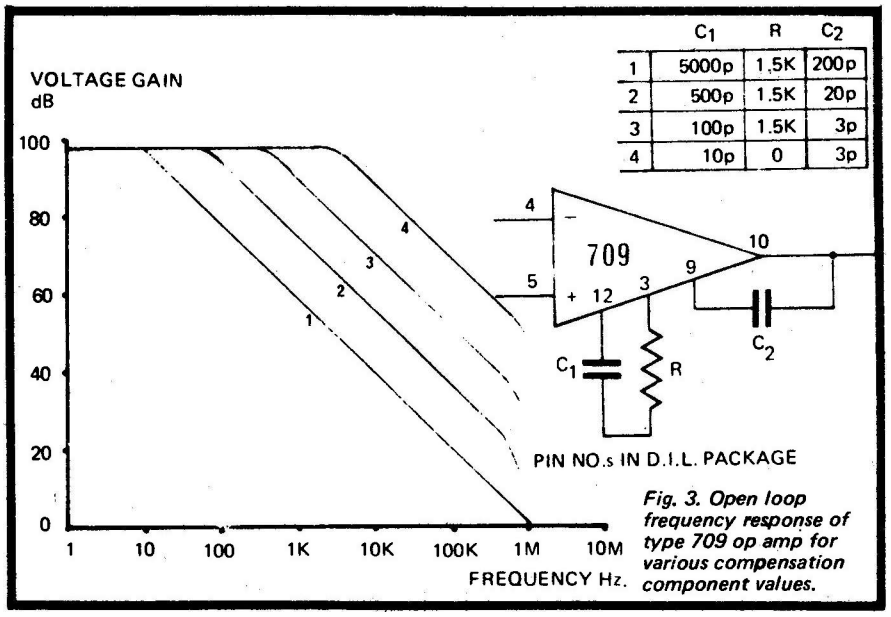


Fig. 2. Open loop gain of type 741 op amp and response with closed loop gain of 20 dB.



	C_1	R	C_2
1	5000p	1.5K	200p
2	500p	1.5K	20p
3	100p	1.5K	3p
4	10p	0	3p

Fig. 3. Open loop frequency response of type 709 op amp for various compensation component values.

FREQUENCY COMPENSATION

Figure 2 shows the frequency response of a type 741 op amp it can be seen that the open loop gain starts to fall at frequencies above about 10 Hz. This is not to say that at higher frequencies useful gain cannot be obtained – it most certainly can. At 100 kHz for example, a closed loop gain of 20 dB is possible. However, the response of the 741 can be a limitation in some applications and then the 709 type amplifier is possibly preferred. The 709 is *never* used without some form of frequency compensation – it readily oscillates at around 10 MHz if none is employed – but does have the advantage that the values of the components used can be varied to provide various bandwidths, (Fig. 3). In practice, the values of the frequency compensation components are chosen to give just sufficient bandwidth for the application being considered. There is no real objection to employing values to give a greater bandwidth, but instability probems may then arise, and the noise level is liable to be greater.

As a point of historical interest, the 709 came before the 741 (it was itself preceeded by other op amps of reduced performance) and the need for the provision of external components proved irksome. Advances in technology enabled manufacturers to incorporate capacitors on the ntegrated circuit chip itself and so ɔrovide an op amp that was stable vithout the need for large external components – thus the 741.

At the same time, the designers were able to provide protection at the input terminals, so that should either input have either supply rail connected to it (by a wiring error for example) no damage would be caused. The 709 in such circumstances, would have burned out its input transistors.

Further improvements were incorporated in the 748 op amp which is in some respects between the 709 and the 741, in that it requires one small external capacitor but provides a greater gain-bandwidth product than the 741.

With so many external connections – two supply rails, two inputs, one output and perhaps terminals for frequency compensation components – a special form of packaging was required and in fact there are two in common use. One, the T099, is similar to the common T05 transistor encapsulation in size of can but has eight lead-out wires. The other is the dual-in-line (DIL) package and it is recommended that the constructor uses this style, together with the appropriate holders. This will make it possible to check, to some extent, the dc conditions of the circuit when first wired up. This is done before the op amp itself is inserted thus perhaps preventing catastrophic failure of the device due to a wiring fault. Further, in those cases where a 709 is called for, it is possible to use a 741 for initial testing (although of course full performance in respect of frequency response might not then be obtained). Should an important wiring erroi have been made, damage is less likely to be caused to a 741 due to the built-in overload protection at its input terminals. ●

OP AMPS Part 2

Two practical projects aid understanding

THE POWER SUPPLY

The limitation when attempting to reduce the size of any small piece of equipment is, with the present state of the art, the dimensions of the mains operated power supply required to drive it. Thus although an oscillator can be constructed with one IC and a few passive components, the companion ac power supply, by comparison, is extremely bulky. Thus it is fairly pointless to attempt to construct the power supply in such a way as to minimize its total volume. This is not really a disadvantage, however, as the power supply can be used to power other circuits and the diminutive oscillator can, of course, be powered by separate, small, batteries when that is desirable.

Small size may not be a feature of the power supply, but it does have several important characteristics, namely, *automatic* short circuit protection and good voltage stabilisation. A brief specification is given in Table 1, while the full circuit diagram appears in Fig. 1.

Consider first that part of the circuit above the dotted line.

Diodes D1 and D2 full-wave rectify the transformer output and charge C1 positively. Capacitor C1 has a sufficiently large value to filter out nearly all the 100 Hz ripple component and provide a smooth dc to the regulator.

The constant potential across the Zener diode D3 maintains the base of Q1 similarly constant. Should the mains voltage vary, or the load current alter, then the output voltage will tend to change too; however, that voltage is fed, via the diode D4, to Q1 emitter, where it is compared with the Zener voltage at Q1 base. Thus, the collector current of Q1, and hence the base current of Q2, will alter, so effectively changing the emitter-collector impedance of Q2 in such a way as to correct for the original variation. The voltage drop across D4, D8 compensates for the drop across Q1 and Q3 thus ensuring the output voltage is the same as the zener voltage.

Such a configuration will give good load regulation but very large variations in mains voltage will not be counteracted as well as is done in some other circuit designs. This is because the Zener diode is fed from an unstabilised supply. Improvement in output voltage stability – by the order of a factor of five or so – can be achieved by modifying the circuit to drive the Zener from the output, rather than the input, of the regulator, but this would not permit the incorporation of short-circuit protection components, in an arrangement now to be described. Short circuit protection of the supply is vital in experimental work, especially on integrated circuits, where the small size and close spacing of the connecting leads printed circuit tracks can so easily result in unwanted shorts which may overload and possibly damage the power supply.

Consider what happens when the output of the voltage regulator is connected directly to the earth line. The germanium diode D4 is no longer forward biased, for its anode,

PARTS LIST — POWER SUPPLY

D1,2,5,6	Diode	IN4001
D3,7	"	BZ x 79 C12 or other 12 V Zener
D4,8	"	IN914
Q1	Transistor	BC547, BC107
Q2	"	BD140, BD136
Q3	"	BC177, BC557
Q4	"	BD139
R1,3	Resistor	1.5 k ¼W
R2,4	"	6.8 k ¼W
C1,4	Capacitor	1000μF 25 V electrolytic
C2,5	"	22μF 16 V electrolytic
C3,6	"	100μF 16 V electrolytic

Transformer 12 V — 0 12 V 100 mA

SW1 double-pole double throw

Die-cast box 165 x 114 x 51 mm

F1	Fuse	1 amp
Fuse holder		20 mm
Terminals (screw)		1 red, 1 black, 1 greer (earth 1 other)
Neon indicator		

Veroboard, 0.15" pitch 100 x 60 mm

TABLE 1

Input	220 – 240 V 50 Hz
Output voltage	1. –12 V and +12 V
or	2. –24 V
or	3. +24 V
Output current	100 mA maximum
Protection	Automatic constant current limiting (210 mA) on short circuit
Regulation	Better than 80 mV variation, no load to full load
Hum and noise	Less than 3 mV

TABLE 2

Frequency range	120 Hz – 1.2 kHz 1.2 kHz – 12 kHz
Output level	1 V rms maximum, continuously variable
Output impedance	70 ohms
Min. load at 1 Vrms	1.5 k
Power supply needed	3 mA at +12 V 2 mA at –12 V

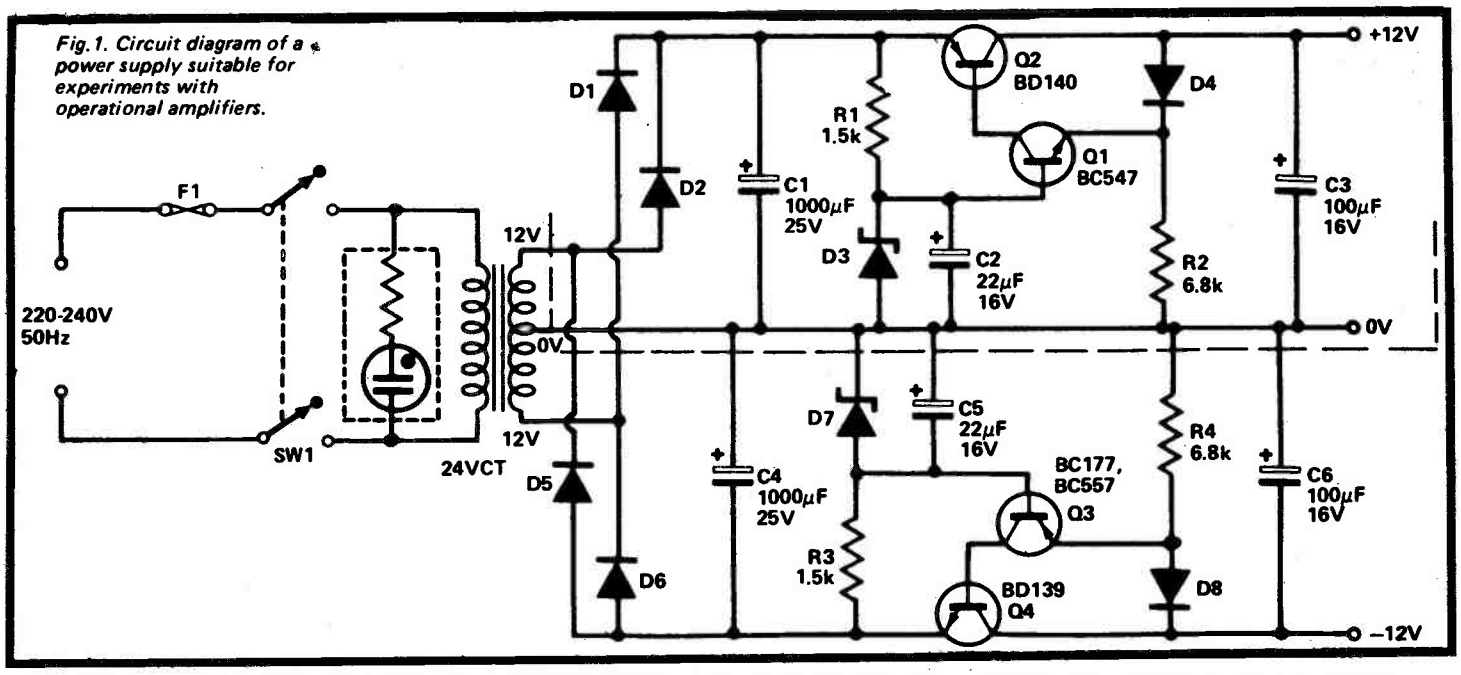


Fig. 1. Circuit diagram of a power supply suitable for experiments with operational amplifiers.

connected now to earth, is not more positive than its cathode; accordingly, D4 can be considered to be absent and the effective circuit arrangement is as in Fig. 2. The base voltage of Q1 is still fixed (by the voltage across the Zener) at 12 V with its emitter taking up a voltage about 0.7 V less. This fixed voltage appears across R2, which means that a fixed current flows through R2 and Q2 into the base of Q1 and hence, the emitter current of Q1 is fixed also. The emitter current of Q2 will be larger than its base current by a factor equal to the current gain of transistor Q2. The emitter current of Q2 is the load current however, so that it can be seen that, under short circuit conditions, a constant current of a magnitude determined by R2 flows into that short circuit.

A suitable value of R2 must be selected to obtain the desired short circuit current. Here, it is chosen so that 210 mA flows in short circuit conditions. It is under these conditions that the greatest power dissipation occurs in Q2 and accordingly it has been ensured that a continuous short circuit will not give rise to overheating of that transistor.

In point of fact, about 3.4 watts are then dissipated in Q2, a value well within the capability of the transistor type employed. It is bolted to, but insulated from, the die-cast box in which the power supply is housed, so that it is thereby provided with a very large heatsink. Accordingly, in normal use all components run with hardly any temperature rise, and even when running into a short circuit, the combination of current limiting and large heatsink ensures that the power supply is not damaged.

What has been discussed so far is a single power supply, giving an output of 12 V. The actual unit contains two such supplies, as Fig. 1 shows, of similar circuit configuration, but, in the second case, a PNP transistor is used instead of an NPN and vice versa, and with a negative supply voltage, derived from D5 and D6, fed to it. The Zener diode and its electrolytic capacitor, as well as the germanium diode, are all connected with the opposite polarity from before. Therefore, a stabilised and protected −12 volts appears at the output, relative to the centre supply terminal.

As quoted in the specification, this permits the output from the power supply unit to be connected in any one of three configurations:—

1. + 12 V and −12 V relative to earth
2. + 24 V relative to earth
3. −24 V relative to earth

This is achieved by connecting the two supplies in series, with the common point brought out as an external connection. Further, this common point is not earthed, but a separate earth terminal provided. The three different modes of operation are then obtained by means of the appropriate external connections — see Fig. 3.

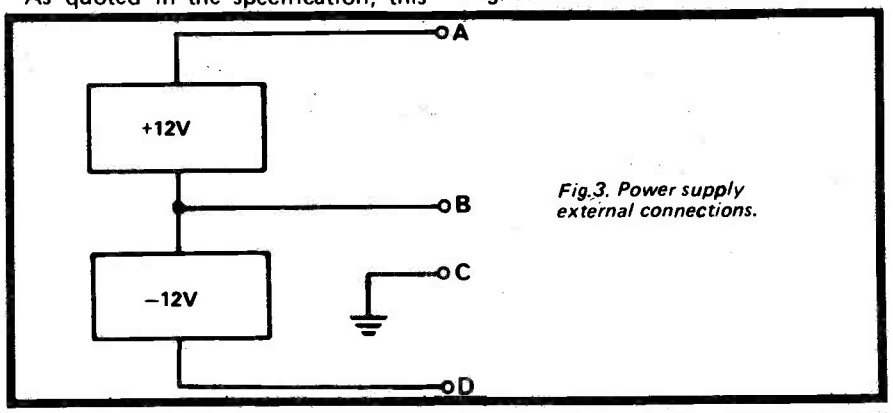


Fig.3. Power supply external connections.

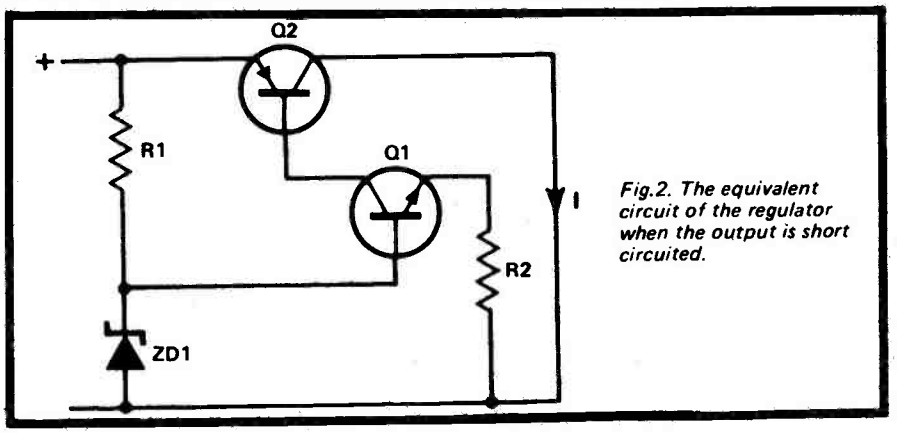


Fig.2. The equivalent circuit of the regulator when the output is short circuited.

For use with the type of operational amplifier dealt with here, the first mode i.e. ± 12 V will usually be employed.

The rated output, of 100 mA from either side, will be found to be more than adequate for the intended use, since type 709 and 741 op. amps. draw less than 5 mA each, unloaded.

A suggested layout and constructional technique for the dual power supply is given in Fig. 4, but the layout is by no means critical and the constructor may employ any alternative method. Nevertheless, a robust housing is required and the best is probably a die-cast box – any small extra expense incurred, to obtain such a convenient and easily worked case, is well worthwhile.

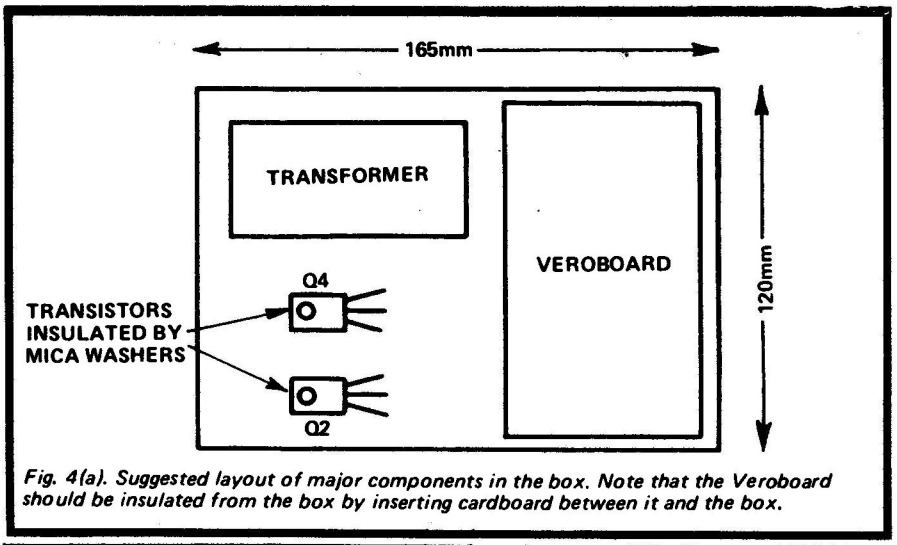


Fig. 4(a). Suggested layout of major components in the box. Note that the Veroboard should be insulated from the box by inserting cardboard between it and the box.

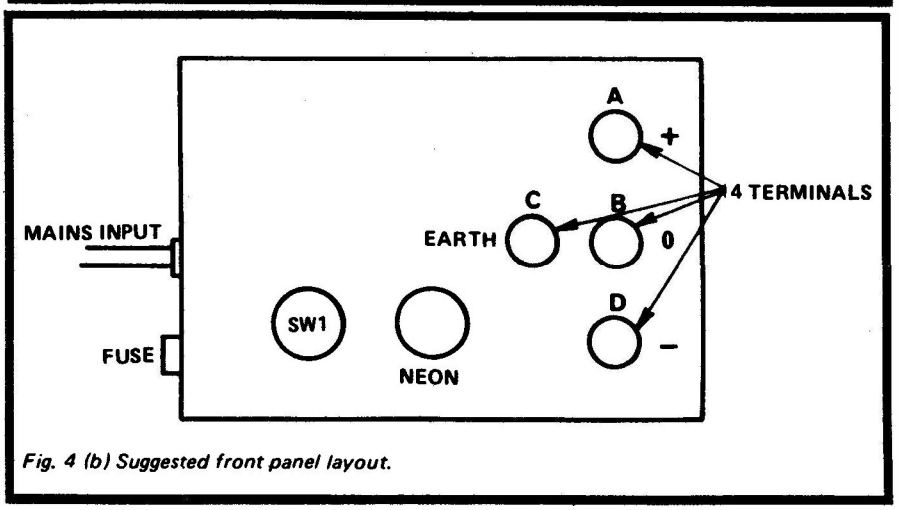


Fig. 4 (b) Suggested front panel layout.

THE OSCILLATOR

Now for the first constructional project using an operational amplifier. As mentioned earlier, this is a sine wave audio oscillator. The circuit is given in Fig. 5 and its specification in Table 2.

The oscillator makes use of the well known Wien-bridge network to set the frequency of operation. A resistor (in this case RV1a and R1) and a *parallel* capacitor (either C1 or C2) are connected to further resistors (RV1b, RV3 and R4) in *series* with a further capacitor (either C3 or C4). It is a property of the Wien network that the junction of the two RC arms, has, at a single frequency only, a voltage in phase with, but smaller than, that applied to the whole network. Since, in the oscillator, this in-phase voltage is fed to the non-inverting terminal of the op. amp. it constitutes positive feedback, and thus oscillations will occur and be maintained at one specific frequency – a frequency determined by the values of the resistors and capacitors employed in the Wien network.

So much for the frequency of oscillation. What of its amplitude?

Consider for a moment what would happen if, with the oscillator already giving a sine wave output, the output amplitude should increase for some reason. If it continues to do so, eventually the voltage will become so large that it will be limited by the supply rails and a clipped sine wave will result. Conversely, if the amplitude of oscillation should decrease, then oscillations will eventually die away to nothing.

Such variations in amplitude can easily arise due to temperature changes etc., and will in any case occur as the frequency is altered, due to tolerances in the capacitor values and tracking errors in the twin-gang potentiometer.

Thus, some means of automatic gain control is essential in order to maintain a constant output amplitude.

It will be recalled that the signal voltage applied to the op. amp. non-inverting input was smaller than the output voltage due to the attenuation in the Wien network. To maintain oscillation the op. amp. must have a gain equal or exceeding this attentuation – which is in fact x3. The desired gain is obtained by selecting the ratio of feedback resistance to input resistance of the inverting input (RV2 + R3)/R2.

If the overall gain, including feedback, exceeds unity the circuit will produce sine wave oscillation at a frequency set by the Wien network.

Stabilisation of the gain is brought about by the action of diodes D1 and D2.

When the instantaneous output voltage is close to zero, neither diode conducts, since even a germanium diode requires 0.4 volts or so forward voltage to bias it on. Consequently, the negative feedback loop is open (giving maximum gain) and, under the action of the positive feedback via the Wien network, oscillations build up rapidly. As soon as their amplitude is sufficient to bias on either D1 or D2 (depending on the polarity of the output voltage swing), then R2, R3 and RV2 provide negative feedback, so limiting oscillations to a convenient level.

Re-inforcement of such oscillations takes place close to each zero crossing when D1 and D2 are open i.e. non-conducting; the setting of RV2 determines the final amplitude.

This method of stabilisation does give rise to a very small amount of crossover distortion, but the effect of this can be minimised by setting VR2 for the largest possible sine wave without clipping. In any event, some distortion is a small price to pay for such a simple, easy-to-get-working sine wave oscillator and, further, it is a *low* level of distortion – some class B audio amplifiers are worse!

Range switching is confined to a choice of two ranges, in the interest of simplicity and cheapness, but more ranges could easily be provided if the constructor is so inclined.

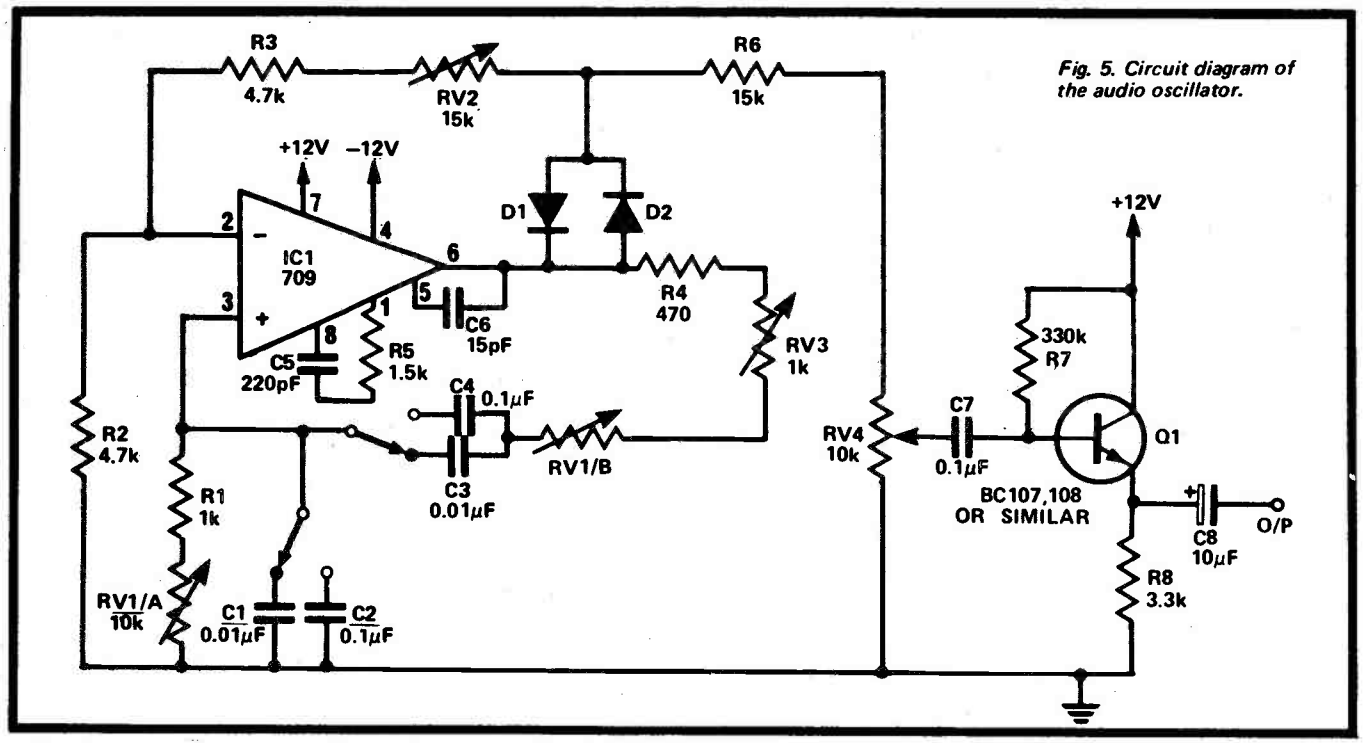


Fig. 5. Circuit diagram of the audio oscillator.

The frequency ranges mentioned in the specification are a little unusual, in that most audio generators provide ranges starting and ending at 1 kHz, 10 kHz and so on. However, in the present case, the selection of easily available components having standard values produced the ranges shown and these were, in fact, found to be convenient in practice.

A simple emitter-follower output stage completes the unit, with a logarithmic potentiometer as a level control, enabling the output to be set from 1 V rms down to 10 mV rms or so.

Suitable compensation components R5, C5 and C6 are required for the type 709 op. amp. A layout found suitable for the oscillator is given in Fig. 6. Notice that this calls for a box of only 100 x 75 x 30 mm, which, whilst making the oscillator quite small and neat, does not result in cramping of the layout, which is straightforward and easily followed.

With wiring up completed and thoroughly checked, switch on and, if possible, monitor the output on an oscilloscope. No 'scope? Then a pair of headphones, of reasonably high impedance, can be used instead. Set RV4 about half way, S1 to "low" and RV1 about half way. If there is no output, adjust RV2; clockwise rotation should give increased output.

With an ac meter, measure the signal level at the junction of D1, D2 and RV2. Adjust RV2 for 3 volts rms. This will ensure the highest output level (thus reducing the effect of crossover distortion) consistent with sine wave operation (no clipping). This should provide about one volt rms at the output.

It was found on the prototype that changing to higher frequency range gave a slightly reduced output – doubtless due to the use of 10% tolerance capacitors in the Wien network. Closer tolerance capacitors are, of course, more expensive but the amplitude difference may be overcome by adding small capacitors to either C1 and C3 or C2 and C4 whichever reduces the amplitude difference.

Variation of output level as RV1 is

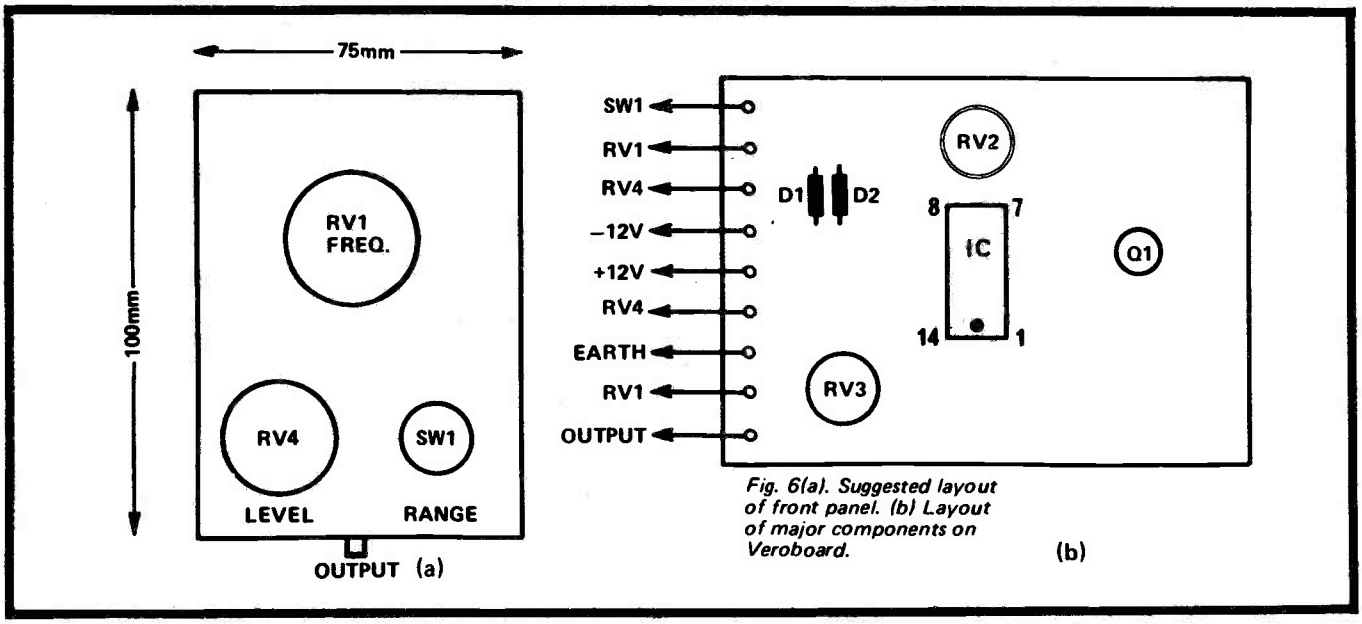


Fig. 6(a). Suggested layout of front panel. (b) Layout of major components on Veroboard.

PARTS LIST — AUDIO OSCILLATOR

IC1	Integrated Circuit	709
Q1	Transistor	BC107,108 or similar
D1,D2	Diode	OA95
R1	Resistor	1k 1/8W or 1/4W
R2,R3	"	4.7k
R4	"	470 1/8W
R5	"	1.5k "
R6	"	15k "
R7	"	330k "
R8	"	3.3k "
C1,C3	Capacitor	0.01μF polyester
C2,C4,C7	"	0.1μF polyester
C5	"	220pF "
C6	"	15pF "
C8	"	10μF electrolytic 16V
RV1	Potentiometer	10k + 10k ganged
VR2,RV2	"	5k pre-set (horizontal)
VR3,RV3	"	1k pre-set (horizontal)
VR4,RV4	"	10k logarithmic
S1	Switch	DPDT

Aluminium box 100 x 75 x 40 mm
Veroboard, 0.1" pitch 80 x 62 mm
8 pin IC holder
3.5 mm jack

rotated, due to tracking errors between RV1 sections, can be minimised by adjustment of RV3. To do this, set RV1 close to its high frequency end. Adjust RV3 to give about the same level of output as with RV1 at mid-travel. If the twin gang potentiometer RV1 is particularly poor in its tracking an alteration to the value of R4 may be called for.

Calibration of the frequency scale is always a problem with any home constructed audio equipment such as this oscillator. Comparison with other audio signals is one method, either by ear, oscilloscope or frequency counter. Ideally comparison with another oscillator will allow the frequency scale to be marked up accurately.

Regarding alternative components: a 741 in place of a 709 will function well, except for some slew rate limiting at the higher frequencies, leading to distortion. If a 741 is used delete C5, C6 and R5. A type 301 may also be used; in this case C5, C6 and R5 are deleted as before and a 10 pF capacitor is fitted between pins one and 8. Almost any silicon NPN transistor will be satisfactory for Q1, but some alteration in R7 value may be necessary. Silicon diodes for D1 and D2 give rise to much greater levels of crossover distortion, due to their greater forward voltage drop.

This little oscillator will be found to give a sufficiently pure sine wave to assist in the testing of almost any audio equipment, its restricted frequency range being no great drawback for that work.

A truly portable oscillator can be made by replacing the dual 12 volts batteries by two small nine volt batteries. If this is done, however, some re-adjustment of RV2 and a reduction in the value of R6 to give a sine wave free from clipping, will be required. ●

OPAMPS Part 3

In this down-to-earth series, J. T. Neil explains the basic theory and practical applications of op amps.

The sine wave oscillator described in the previous part was an example (albeit an extreme one) of how frequency selective feedback is used with operational amplifiers. We shall now go on to consider an amplifier employing non frequency-selective feedback and then amplifiers using feedback of such a nature as to produce two particular forms of frequency response. Then to conclude, there is a description of the use of an op. amp., as a dc amplifier, to increase the sensitivity of a moving coil meter — in this case the frequency is required to be limited to dc up to a few Hz only.

Figure 1 gives the circuit of a high input-impedance amplifier with a nominal voltage gain of 48 and a bandwidth of from 10 Hz to at least 50 kHz. In the prototype the measured value of input impedance was 10M Ω at 1 kHz. This value will vary slightly with frequency and with the particular layout employed, but in any case is likely to be as high as will normally be required for most applications.

As an ac connection, via a capacitor, is provided at the non-inverting input there would be no dc return for bias current, at that input, if R_3 were not present. The value of R_3 is 47 k however, bootstrapping is used to raise the apparent value of R_3 to the value of 10 megohm as quoted, in the following manner.

Due to the extremely high gain of the op. amp, and to the feedback between the output and the inverting input pin 2, there is very little difference in the signal levels at the +ve and –ve inputs, and, since C1 has a negligible reactance, there is similarly very little difference in signal voltage at either end of R_3. Accordingly, very little signal current can flow into R_3 from the signal input, thus R_3 appears, to the input signal, to be many times its actual value.

With the op. amp. arranged in the non-inverting configuration, the voltage gain is:

$$Av = \frac{R_1 + R_2}{R_1} = 48$$

This amplifier set-up is most likely to be used in the design of a pre-amplifier for an oscilloscope or millivoltmeter, where the high value of input impedance is necessary in order to load the circuit under test as little as possible.

In audio applications, a 'tailored' frequency response is often called for; for example, the output of a tape replay head should be fed to a stage with a gain rising at 6dB per octave below about 2.5 kHz, and a flat response above that frequency. (The actual value of the break frequency depends on the tape speed and the particular replay characteristic employed). Such a response is readily arrived at by replacing R_2 of Fig. 1 with the network shown in Fig. 2a.

At high frequencies C_5 has a reactance low compared to R_6 and hence it can be ignored. Thus the gain is determined by R_6 alone (although R_5 is in parallel its value is large enough to be disregarded). As the frequency is lowered, the reactance of C_5 rises and consequently the feedback is reduced, so giving the frequency response shown in Fig. 3a. Resistor R_5 provides a dc connection for the negative input of the op. amp. and limits the gain at very low frequencies.

The voltage gain of this circuit at high frequencies is about 16 times; this will make the tape head output comparable to that from a magnetic pick-up. If more gain is called for, this is best done by increasing the value of R_6 and reducing the value of C_5 in proportion.

What if a response suitable for pre-amplification of the output of magnetic pick-up is required? In this case the network of Fig. 2b is a suitable replacement for R_2 in the original circuit; the overall response of the stage is now as given in Fig. 3b.

Similar reasoning to that given for the tape head amplifier applies here also — the gain rises at lower frequencies as C_6 reactance becomes larger, falling at the higher frequencies as the reactance of C_6 and C_7 both fall. As before, R_7 sets the low-frequency gain.

These two latter configurations are good examples of the shaping of a frequency response to suit a particular need — as indeed was the audio oscillator of Part 2. Note that the response and the overall gain can be adjusted independently.

All the circuits given so far in Part 3 are intended to make use of type 709 op. amps., although a 741 or an LM301 could be used with the appropriate equalizing network changes as detailed in Part 2.

The amplifier configuration des-

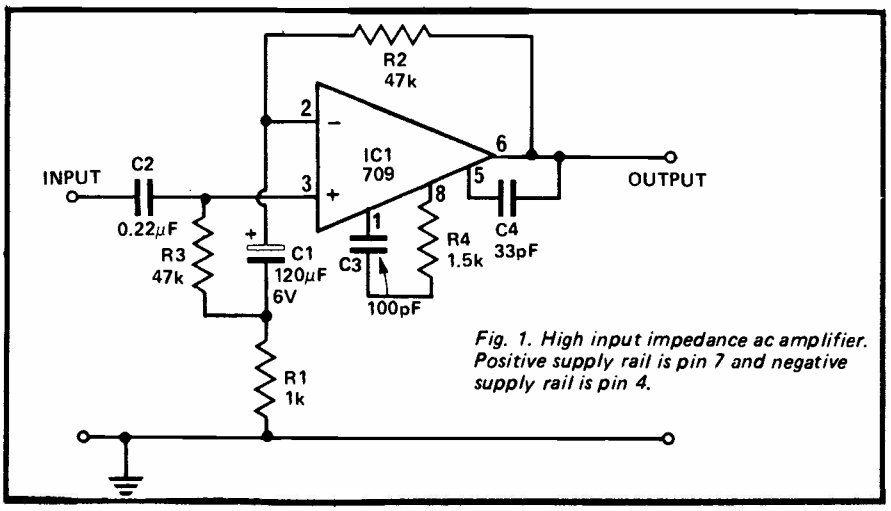


Fig. 1. High input impedance ac amplifier. Positive supply rail is pin 7 and negative supply rail is pin 4.

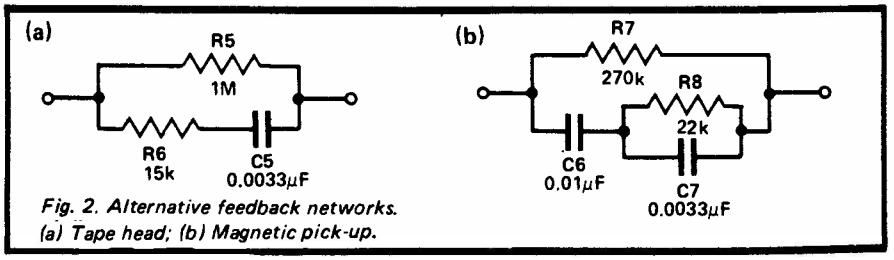


Fig. 2. Alternative feedback networks. (a) Tape head; (b) Magnetic pick-up.

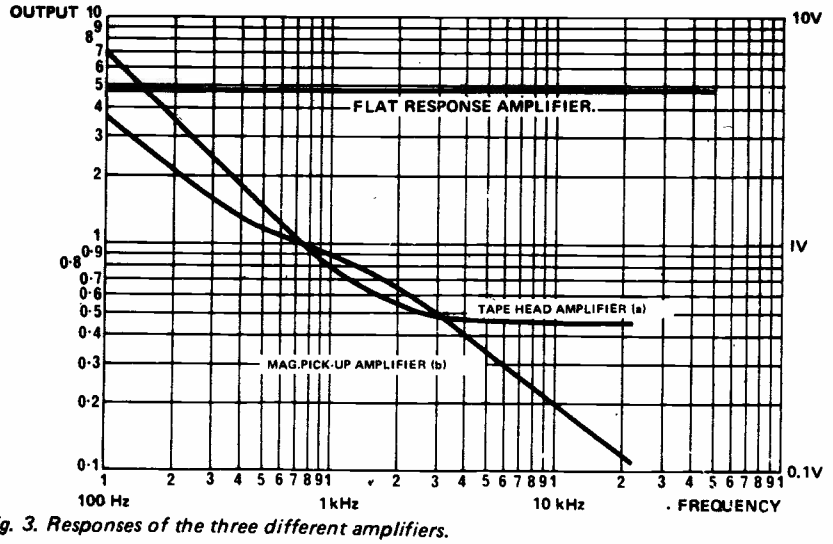


Fig. 3. Responses of the three different amplifiers.

cribed is an inherently stable one and almost any convenient layout can be employed. A small piece of Veroboard was used in the prototypes, with a dual-in-line IC holder soldered in place and the remaining components placed around it.

For convenience, it is best to build the whole amplifier in a small metal box, either mounting this in existing equipment or leaving it as a separate unit for greater flexibility. The box must be earthed to give a measure of screening to reduce hum pick-up. This is especially necessary if the feedback networks of Figs. 2a or 2b are employed as both of these provide considerable bass boost thus aggravating the hum problem.

METER AMPLIFIER

Now for the dc meter amplifier which uses a 741 type IC. The circuit is given in Fig. 4. The values shown give full scale deflection on a 1 mA meter with only 10μA flowing into the input.

Circuit function depends on there being negligible difference between the voltages at the two inputs of an op. amp. when arranged in a negative feedback configuration. Accordingly, whatever voltage is applied to the non-inverting terminal, that is, across R_1, will appear at the inverting terminal, that is, across R_3. However, R_3 is only 1/100th of the value of R_1, so that the current through R_3 must be 100 times larger than that through R_1. It is, of course, the current through R_3 that flows through the meter, and it is worth noting that the value of this current is not affected by resistor R_2 in series with the meter – provided of course that R_2 is not too large to allow the required meter current to flow. The value of R_2 is chosen here to limit meter current to about twice the FSD current, so providing a useful safety device should an unexpectedly high voltage be applied to the non-inverting terminal.

Thus we have a circuit incorporating a meter of 1 mA basic sensitivity but which appears to be a meter of 100 times that sensitivity.

Resistor R_4 is included to improve the performance with regard to drift, of the meter reading, as temperature changes cause changes in the op. amp. bias currents. It is best selected by experiment, although the value given was found to be satisfactory with

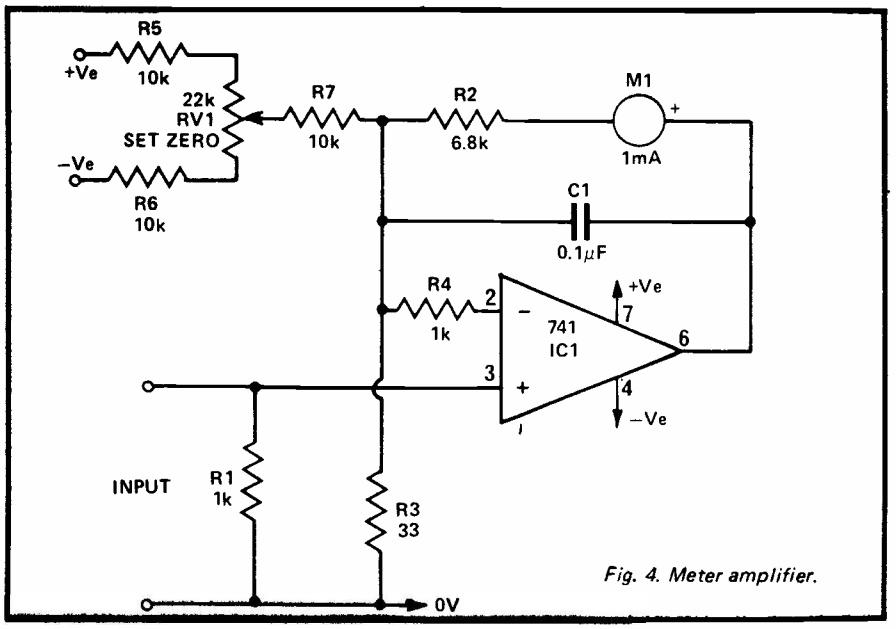


Fig. 4. Meter amplifier.

PARTS LIST

Flat response amplifier
IC1 Integrated Circuit 709 8 pin DIL
R1 Resistor 1k ¼ watt 5%
R2 " 47k " 5%
R3 " 47k " 5%
R4 " 1.5k " 5%
C1 Capacitor 120 μF 6V electro.
C2 " 0.22 μF polyester
C3 " 100 pF ceramic
C4 " 33 pF ceramic

Tape head network plus all of Fig. 1
R5 Resistor 1MΩ ¼ watt 5%
R8 " 15k " 5%
C5 Capacitor 3,300 pF polyester

Pick-up network plus all of Fig. 1
R7 Resistor 270k ¼ watt 5%
R8 " 22k " 5%
C6 Capacitor 0.01 μF polyester
C7 " 3,300 pF polyester

Meter amplifier
IC1 Integrated Circuit 741 8 pin DIL
R1 Resistor 1k ¼ watt 5%
R2 " 6.8k ¼ watt 5%
R3 " 33 ¼ watt 5%
R4 " 1k ¼ watt 5%
R5 " 10k ¼ watt 5%
R6 " 10k ¼ watt 5%
R7 " 10k ¼ watt 5%
RV1 Potentiometer 22k linear
C1 Capacitor 0.1 μF polyester
M1 Meter 1 mA movement

Miscellaneous
IC holders, Veroboard, small aluminium boxes etc.

three individual 741's.

The voltage at the slider of RV_1 is fed via R_7 to the inverting input to provide a means of setting the meter zero. It can, if desired, be used to give a centre zero, so producing a 5 μA–0–5 μA meter. The capacitor C_1 ensures that the gain falls at high frequencies.

With a basic sensitivity of 10 μA., this amplifier enables a dc voltmeter of 100 kohm per volt to be constructed, by connecting the appropriate resistor in series with the input. The value of the resistor is given by:

R = 100 V kilohms

where V is the input voltage required to give FSD.

Note that the basic meter of 1mA is a type of movement that is much more robust, and yet cheaper, than others of greater sensitivity.

The actual method of construction can be adapted to suit individual requirements. If a 1 mA meter is bought for the job, almost any housing capable of containing it will have room for the 741 and the few other components required, whilst only three short lengths of wire are required for connection to the power supply. The test-meter used in the prototype had a 1 mA range, so a small aluminium box was used for the circuitry, with two output terminals for the test-meter connections, and, again, three leads for the power supply.

As with the audio amplifier, it is best to use a small piece of Veroboard to mount the IC holder and components, and to bolt the board to the box with insulated spacers if required. ●

Back Numbers From HE

We regret to say that copies of the November, December and January issues of Hobby Electronics have sold out (we did warn you!) However Hobbyprints A B C, F and G are still available.

Shown here are most of the past issues with their major features and projects. The issues available are now priced £1.00 each including post and packing. Send your order to:

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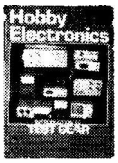
Shown next to each issue is the relevent code letter to use when ordering Hobbyprints. (See Hobbyprints ad. elsewhere in this issue.)

FEBRUARY 79 (Hobbyprint D)
Projects: Short Wave Radio, Sine/Square Generator Scratch/Rumble Filter, Car Alarm Project.
Features: Video Tape Recorders, Radioactivity, CA 3130 Circuits, Computer Glossary etc.



MARCH 79 (Hobbyprint E)
Projects: Light Chaser, Tone Controller, Photographic Timer, Cassanova's Candle.
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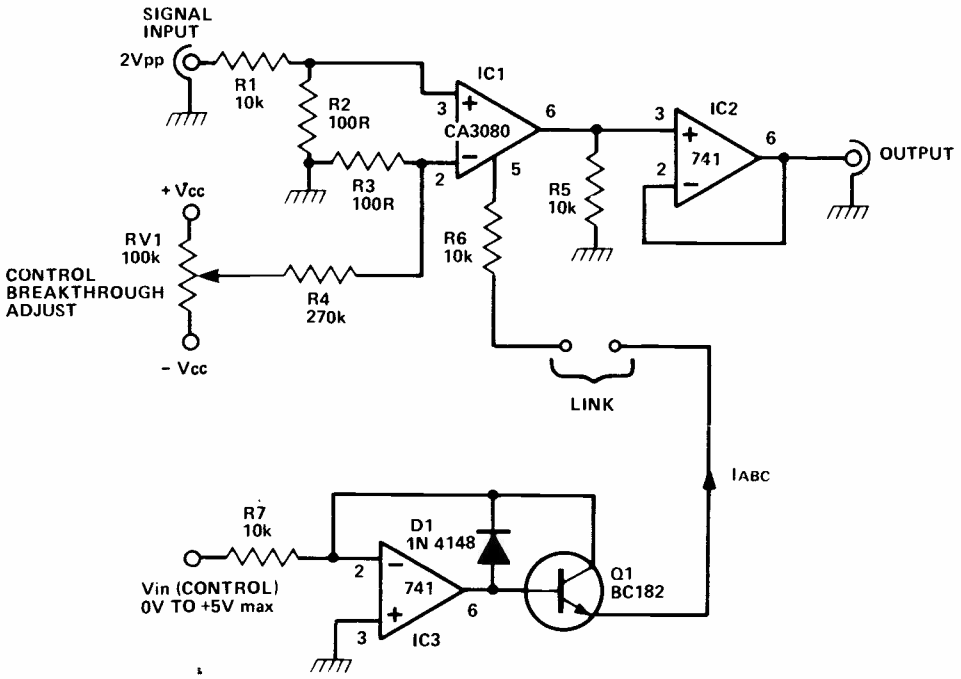
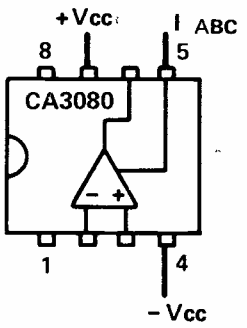
3080 CIRCUITS

The 3080 is not a run of the mill op amp. These ten circuits from Tim Orr show you why.

The CA3080 is known as an operational transconductance amplifier, (OTA). This is a type of op amp, the gain of which can be varied by use of a control current, (I_{ABC}). The device has a differential input, a control input known as the 'Amplifier bias input' and a current output. It differs in many respects from conventional op amps and it is these differences that can be used to realize many useful circuit blocks.

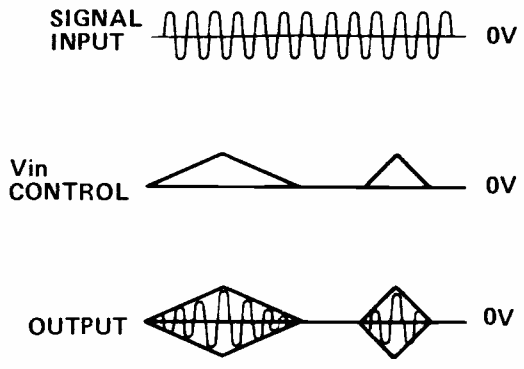




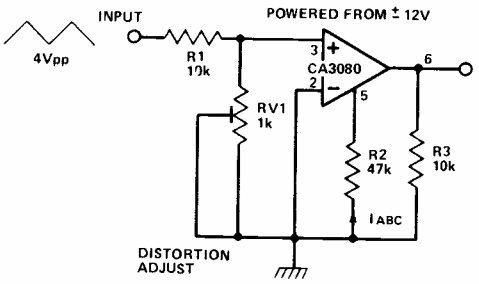
Voltage Controlled Amplifier

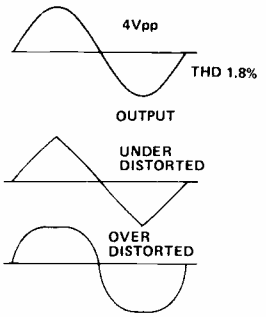
The CA3080 can be used as a gain controlling device. The input signal is attenuated by R1, R2 such that a 20 mVpp signal is applied to the input terminals. If this voltage is much larger, then significant distortion will occur at the output. In fact, this distortion is put to good use in the triangle-to-sinewave converter. The gain of the circuit is controlled by the magnitude of the current I_{ABC}. This current flows into the CA3080 at pin 5, which is held at one diode voltage drop above the -Vcc rail. If you connect pin 5 to 0 V, then this diode will get zapped, (and so will the IC)! The maximum value of I_{ABC} permitted is 1 mA and the device is 'linear' over 4 decades of this current. That is, the gain of the CA3080 is 'linearly' proportional to the magnitude of the I_{ABC} current over a range of 0.1uA to 1 mA. Thus, by controlling I_{ABC}, we can control the signal level at the output. The output is a current output which has to be 'dumped' into a resistive load (R5) to produce a voltage output. The output impedance seen at IC1 pin 6 is 10k (R5), but this is 'unloaded' by the voltage follower (IC2) to produce a low output impedance. The circuit around IC3 is a precision voltage-to-current converter and this can be used to generate I_{ABC}. When Vin (control) is positive, it linearly controls the gain of the circuit. When it is negative, I_{ABC} is zero and so the gain is zero.

This type of circuit is known by several names. It is a voltage controlled amplifier, (VCA), or an amplitude modulator, or a two quadrant multiplier.



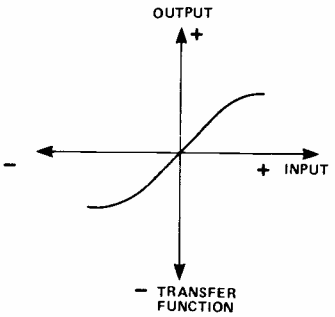
One problem that occurs with the CA3080 is that of the 'input offset voltage'. This is a small voltage offset between its input terminals. When there is no signal input and the control input is varied a voltage similar to the control input will appear at the output. By adjusting RV1 it is possible to null out most of this control breakthrough.

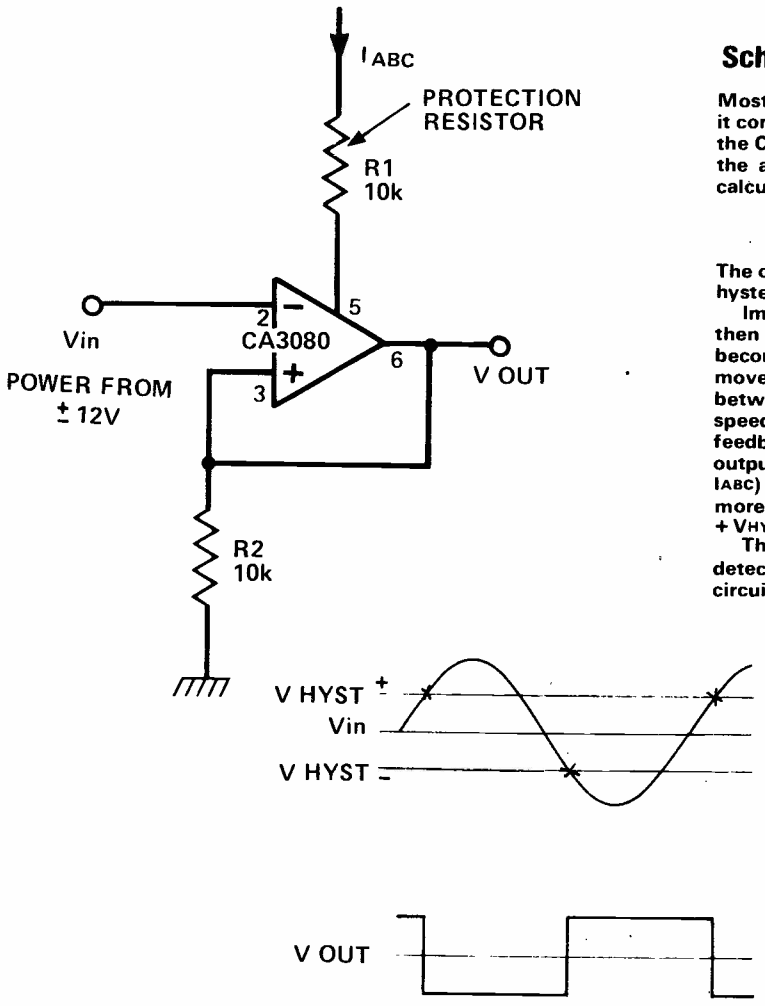




Triangle To Sinewave Converter

By overloading the input of a CA3080 it is possible to produce a 'sinusoidal' transfer function. That is, if a triangle waveform of the correct magnitude is applied to the CA3080 input, the output will be distorted in such a way as to produce a sinewave approximation. In the circuit shown, RV1 is adjusted so that the output waveform resembles a sinewave. I tested this circuit using an automatic distortion analyser and found the sinewave distortion to be only 1.8%, mostly third harmonic distortion, which, for such a simple arrangement, seems very reasonable indeed. This could be used to produce a sinewave output from a triangle/square wave oscillator.





Schmitt Trigger

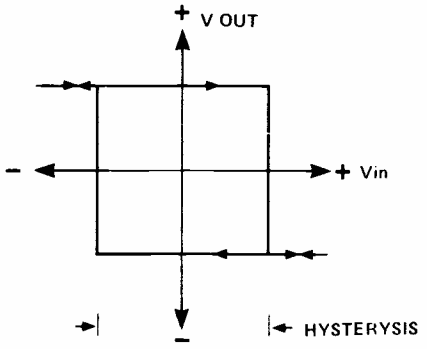
Most Schmitt trigger circuits prove to be very complicated when it comes to calculating the hysterysis levels. However, by using the CA 3080 these calculations are rendered trivial plus there is the added bonus of fast operation. The hysterysis levels are calculated from the simple equation,

$$V_{HYST} \approx \pm (I_{ABC} \times R2)$$

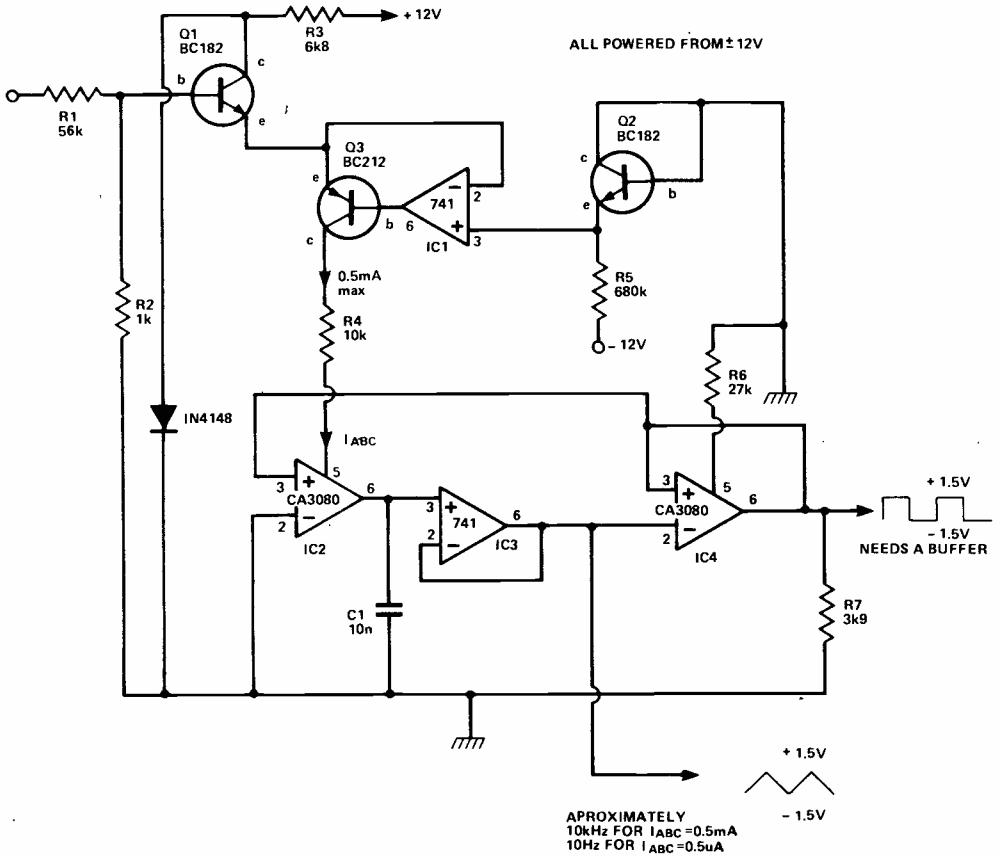
The output squarewave level is in fact equal in magnitude to the hysterysis levels. The circuit operation is as follows.

Imagine the output voltage is high. The output voltage will then be equal to (R2 × IABC) which we will call +VHYST. If VIN becomes more positive than +VHYST, the output will start to move in a negative direction, which will increase the voltage between the input terminals which will further accelerate the speed of the output movement. This is known as regenerative feedback and is responsible for the schmitt trigger action. The output snaps into a negative state, at a voltage equal to — (R2 × IABC) which is designated as —VHYST. Only when VIN becomes more negative than — VHYST will the output change back to the +VHYST state.

The Schmitt trigger is a very useful building block for detecting two descrete voltage levels and finds many uses in circuit designs. ▶



IABC CONTROLS HYSTERYSIS LEVELS AND OUTPUT LEVEL



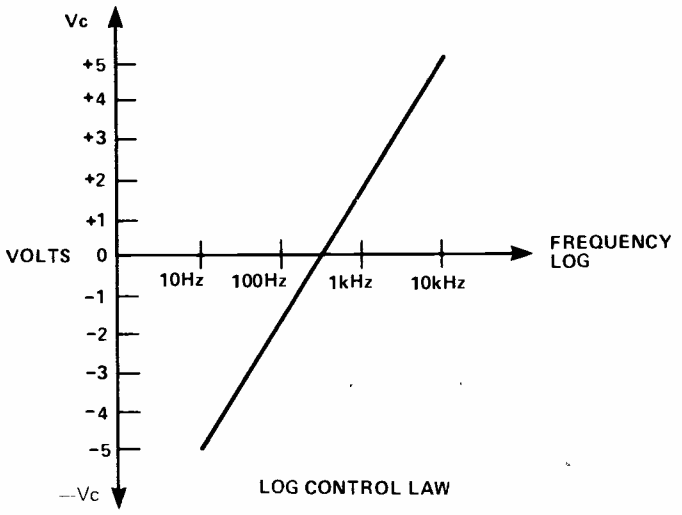
Voltage Controlled Oscillator

By using two CA3080's and some op amps it is possible to make an oscillator, the frequency of which is voltage controllable. This unit finds many applications in the field of electronic music production and test equipment. The circuit has been given a logarithmic control law, that is, the frequency of operation doubles for every volt increase in the control voltage. This makes it ideal for musical applications where linear control voltages need to be converted into musical intervals (which are logarithmically spaced) and also for audio testing where frequencies are generally measured as logarithmic functions.

IC2 is an integrator. The IABC current that drives this IC is used to either charge or discharge C1. This produces triangular waveforms which are buffered by IC3, which then drives the Schmitt trigger IC4. The hysterysis levels for this device are fixed at + 1.5V, being determined by R6, R7.

The output of the schmitt is fed back in such a way as to control the direction of motion of the integrator's output. If the Schmitt output is high, then the integrator will ramp upwards and vice versa. Imagine that the integrator is ramping upwards. When the integrators output reaches the positive hysterysis level, the Schmitt will flip into its low state, and the integrator will start to ramp downwards. When it reaches the low hysterysis level the Schmitt will flip back into its high state. Thus the integrator ramps up and down in between the two hysterysis levels. The speed at which it does this, and hence the oscillating frequency is determined by the value of IABC into IC2. The larger the current, the faster the capacitor is charged and discharged. Two outputs are produced, a triangle wave (buffered) from IC3 and a squarewave (unbuffered) from IC4. If the squarewave output is loaded then the oscillation frequency will change.

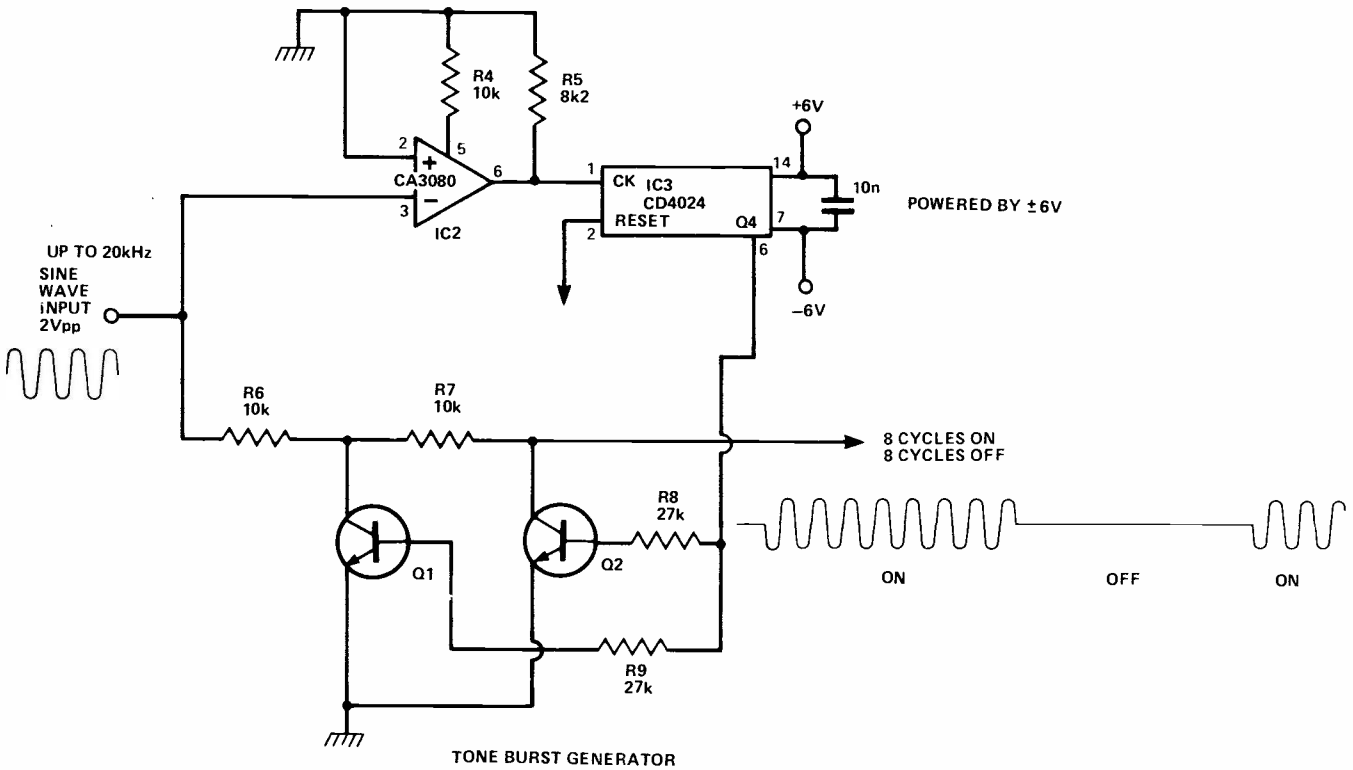
The log law generator is composed of Q1, 2, 3 and IC1. Transistors Q1 and Q2 should be matched so that their base emitter voltages (Vbe) are the same for the same emitter current, (50uA). Matching these devices to within 5 mV is satisfactory, although unmatched pairs could be used. When matching transistors take care not to touch them with your fingers. This will heat them up and produce erroneous measurements. Transistor Q2 is used to produce a reference voltage of about —OV6 which is connected to IC1 pin 3. This op amp and



Q3 is used to keep Q1 emitter at this same voltage of —OV6. The input control voltage is attenuated by R1, R2 such that a + 1 V increase at the input produces a change of only + 18 mV at the base of Q1. However the emitter of Q1 is fixed at —OV6, so the current through Q1 doubles. (It is a property of transistors that the collector current doubles for every 18 mV increase in Vbe).

The emitter current of Q1 flows through Q3 and into IC2 thus controlling the oscillator frequency. It is possible to get a control range of over 1000 to 1 using this circuit. With the values shown, operation from 10 Hz to 10 kHz is achieved. Reducing C1 to 1 n will increase the maximum frequency to 100 kHz, although the waveform quality may be somewhat degraded.

Changing C1 to 1uf (non-polarized) will give a minimum frequency of 0.1 Hz.

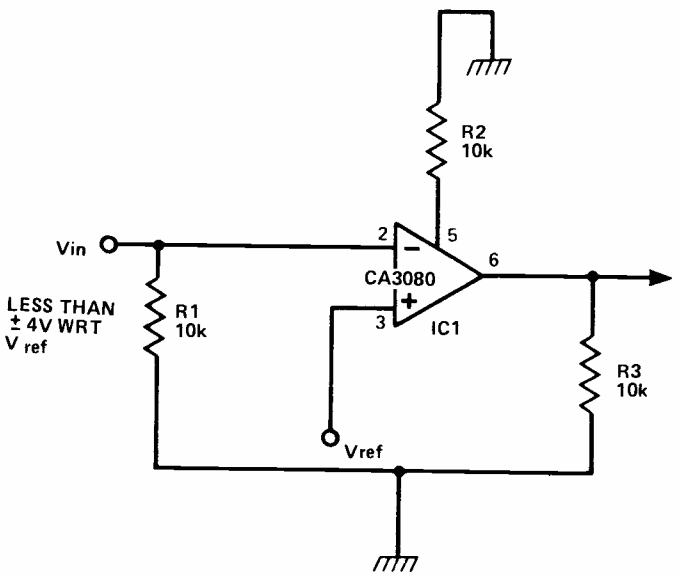


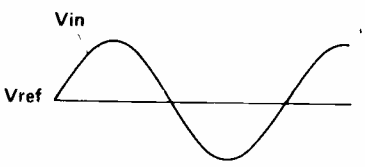
TONE BURST GENERATOR

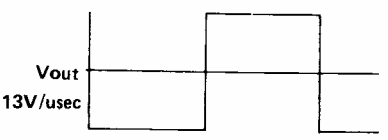
Fast Comparator

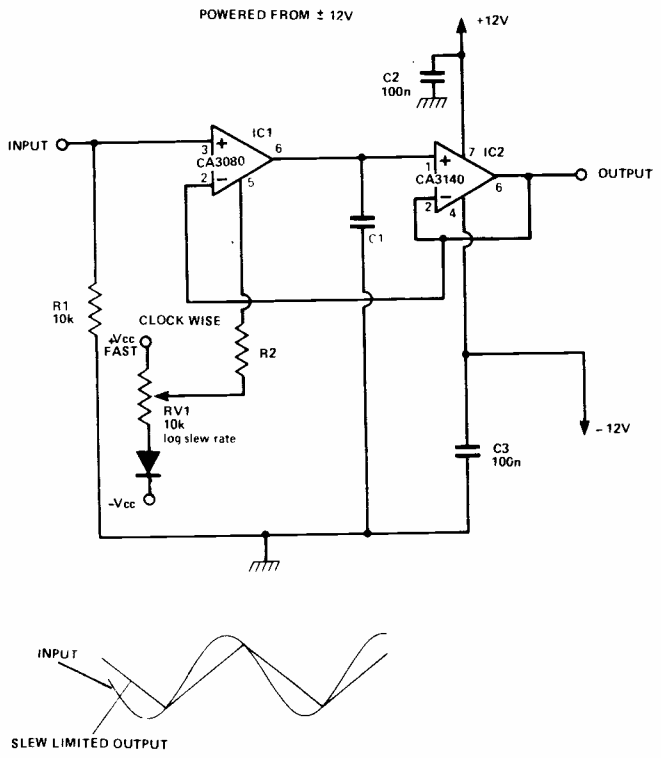
The high slew rate of the CA3080 makes it an excellent fast voltage comparator. When pin 2, IC1 is more positive than Vref the output of IC1 goes negative and vice versa. Vref can be moved around so that the point at which the output changes can be varied. As long as the input sinewave level is quite large (1 V say) then the output can be made to move at very fast rates indeed. However, care must be taken to avoid overloading the inputs. If the differential input voltage exceeds 5 V, then the input stage breaks down and may cause an undesired output to occur.

One use of a fast comparator is in a tone burst generator. This device produces bursts of sinewaves, the burst starting and finishing on axis crossings of the sinusoid. The comparator is used to detect these axis crossings and to produce a square wave output which then drives a binary divider (IC3). The divider produces a 'divide by sixteen' output which is high for eight sinewave cycles and then low for the next eight. This signal is then used to gate ON and OFF the sinewave. The gate mechanism is a pair of transistors which short the sinewave to ground when the divider output is high and let it pass when the divider output is low. The resulting output is a toneburst. However, if the comparator is not very fast, then there will be a delay in generating the gate and so the tone burst will not start or finish on axis crossings. Using the circuit shown, operation up to 20 kHz is obtainable.









Slew Limiter

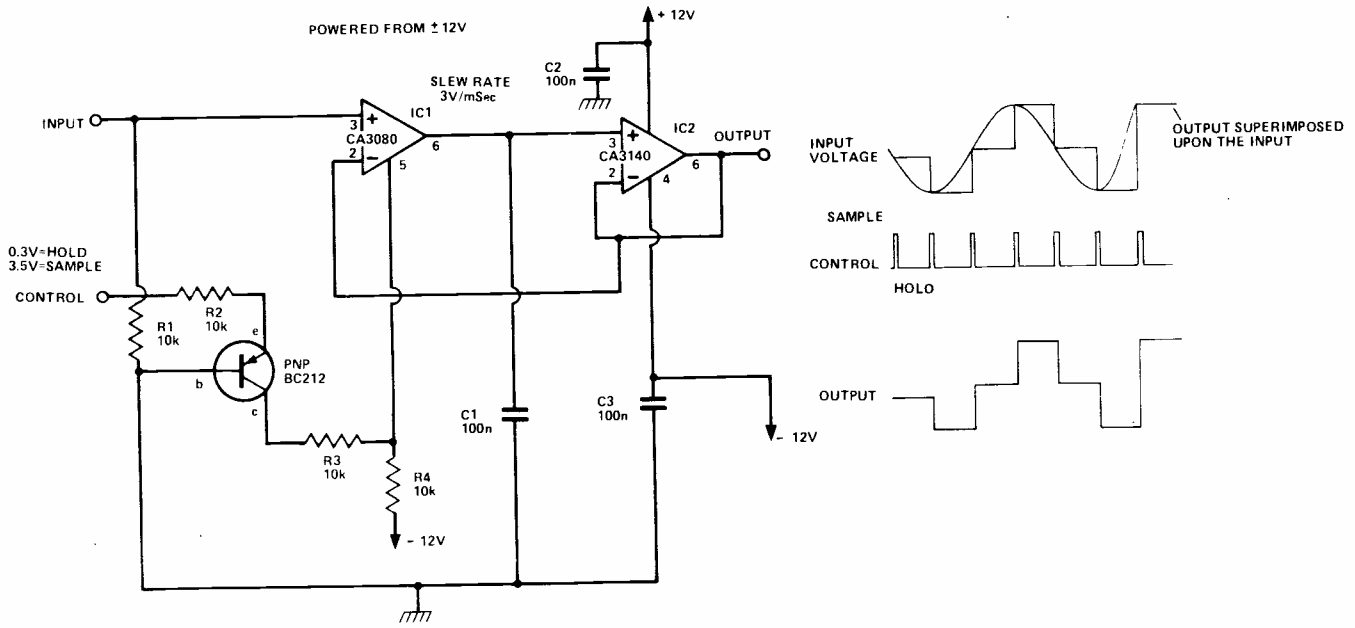
The current output of a CA3080 can be used to produce a controlled slew limiter. By connecting the output current to a capacitor, the output voltage cannot move faster than a rate given by

$$\text{slew rate} = \frac{I_{ABC}}{C1} \text{ Volts per sec.}$$

Note that I_{ABC} determines the slew rate and as I_{ABC} is a variable then so is the slew rate. The output voltage is buffered by a voltage follower, IC2. This is a MOSFET op amp which has a very high input impedance, which is necessary to minimise the loading on C1.

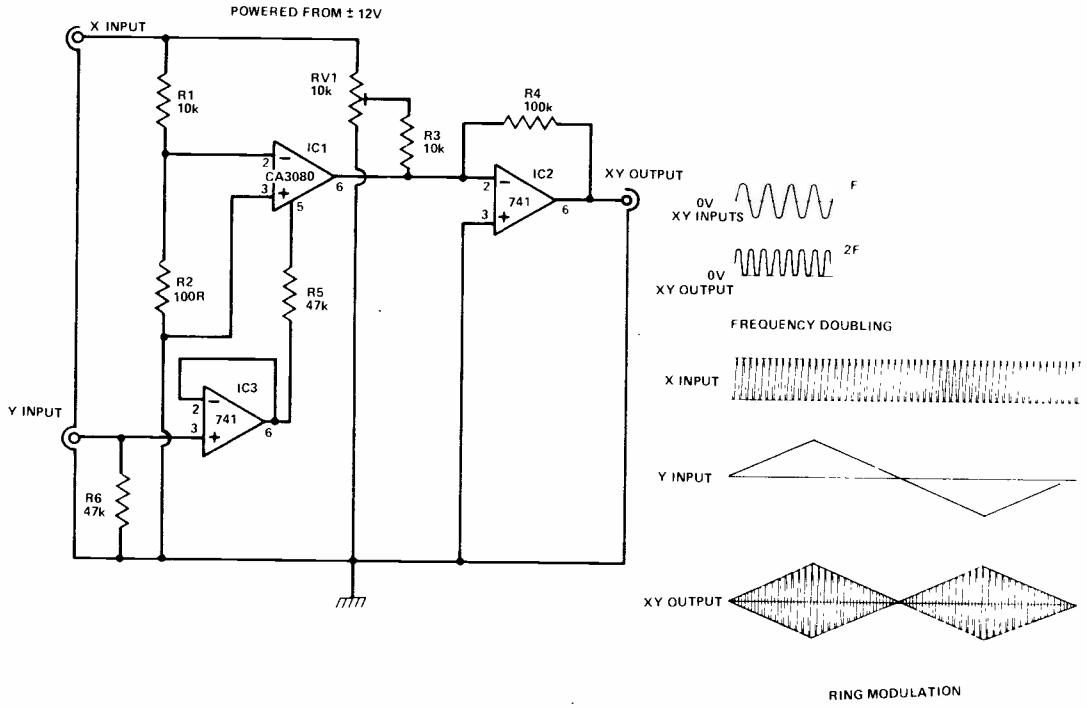
When an input signal is applied to IC1 the output tries to move towards this voltage but its speed is limited by the slew rate. Thus the output produces a linear ramp which stops when it reaches the input signal level.

R2	C1	FASTEST SLEW RATE
150k	100n	1.5V/mSec
150k	10n	15V/mSec
150k	1u0	0.15V/mSec
1M5	1u0	15V/Sec



Sample And Hold

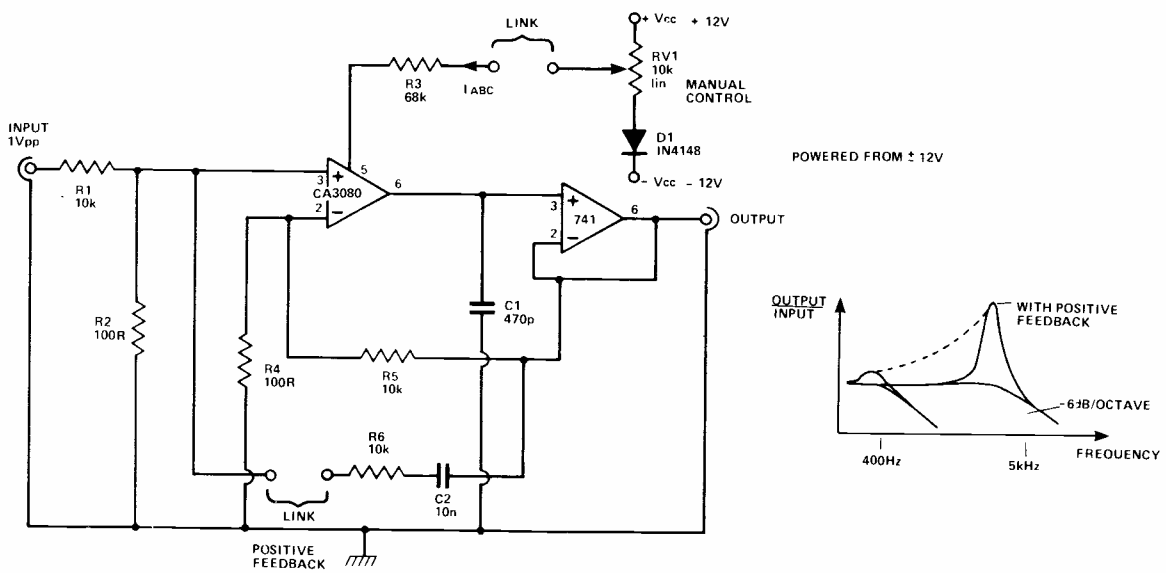
The slew limiter can be modified so that it becomes a sample and hold unit. In this circuit I_{ABC} is either hard ON (sample) or completely OFF (hold). In the sample mode, the output voltage quickly adjusts itself so that it equals the input voltage. This enables a short sample period to be used. In the HOLD mode, I_{ABC} is zero and so the voltage on C1 should remain fixed. The circuit is in fact an analogue memory. It is used in music synthesisers (to remember the pitch), in analogue to digital converters and many other circuits.



4 Quadrant Multiplier

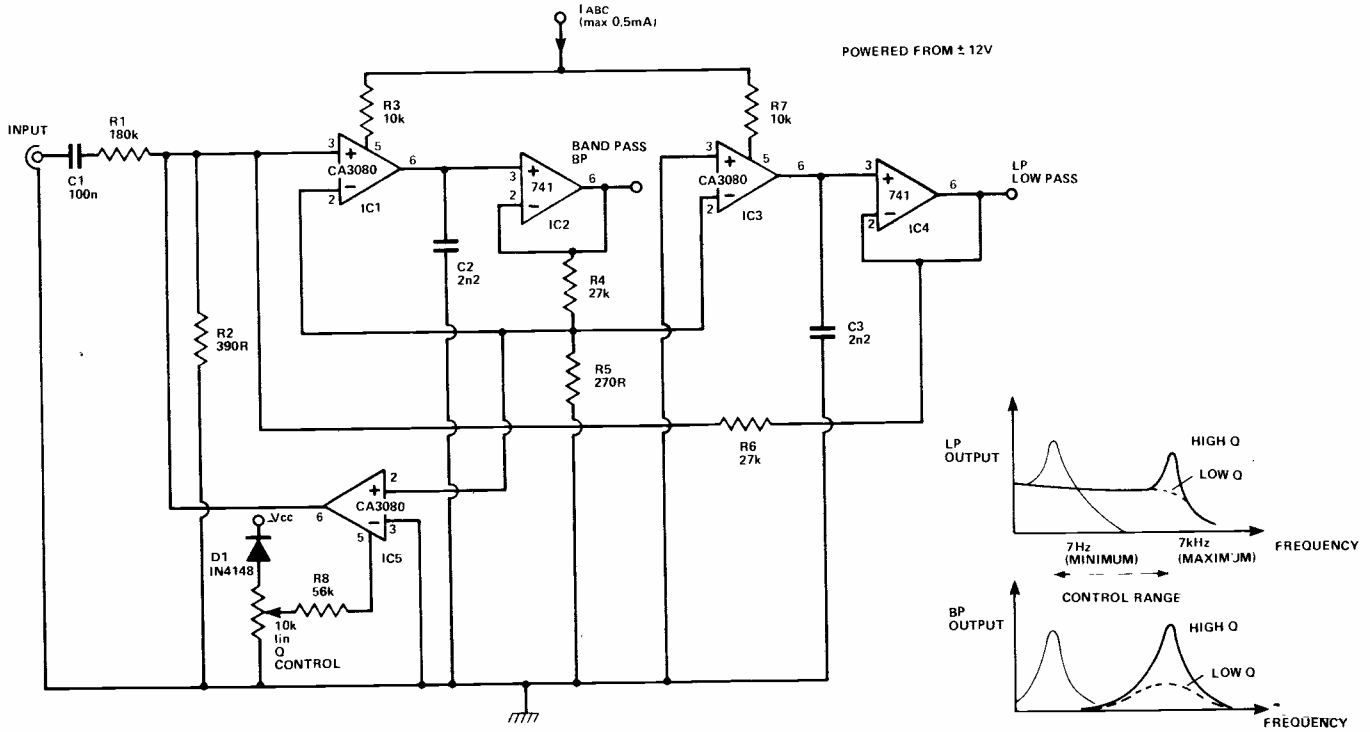
The CA3080 is a two quadrant multiplier but, with the addition of a few extra bits of electronics, it can be made into a four quadrant circuit. A two quadrant multiplier has two inputs, one can accept bipolar signals (the inverting or non inverting input) and one can only accept a unipolar signal, (the I_{ABC} current). However, a four quadrant multiplier can accept bipolar signals on both of its inputs which enables it to perform frequency doubling and ring modulation.

The circuit is fairly similar to that of the two quadrant multiplier described earlier except for two differences. IC3 is used to generate I_{ABC} in such a way that the Y input can go both positive and negative, thus the Y input is bipolar, when Y is at 0 V and there is a signal on the X input the desired output (X × Y) should be zero. This is achieved by adjusting RV1 so that the signal via IC1 (this is inverted) is exactly cancelled out by that via R3. Now, when Y is increased positively, a non-inverted value of X is produced at the output and, when Y is increased negatively, an inverted value of X is produced. When Y is zero, so is the output. This is known sometimes as ring modulation. If a speech signal is connected to the X input and a variable frequency oscillator to the Y input the resulting sound is that of a 'dalek'. Also, if a sinewave is connected to both the X and Y inputs, the XY product is a sinewave of twice the frequency. This is known as a frequency doubler, but it will only work with sinewaves.



Single Pole Filter

A singlepole lowpass filter can be constructed using a CA3080 as a current controlled resistor. The filter is, in fact, just a simple RC low pass section where the R, which is controllable, is constructed out of IC1, R4, R5. Varying I_{ABC} changes the amount of current drive to C1. This would normally make the circuit a slew limiter, but because the signal level that IC1 (pins 2 and 3) handles is so small, the CA3080 works in its linear mode. This enables it to look like a variable resistor. When this resistor is varied, the break frequency of the filter also varies. By applying some positive feedback around the filter (R6, C2) it is possible to produce a peaky filter response. The peak actually increases with frequency making the circuit useful as a guitar Wah Wah unit.



Voltage Controlled Filter

A standard dual integrator filter can be constructed using a few CA3080's. By varying IABC the resonant frequency can be swept over a 1000 to 1 range. IC1, 3 are two current controlled integrators. IC2, 4 are voltage followers which serve to buffer the high impedance outputs of the integrators. A third CA3080 (IC5) is used to control the Q factor of the filter. Q factors as high as 50 can be obtained. The resonant frequency of the filter is linearly proportional to IABC and hence this unit is very useful in electronic music production. There are two outputs produced, a low pass and a band pass response. ●

GEORGE HANSLIP SHOWS HOW TO INTERFACE

CMOS TO MAINS

The advantages of CMOS, namely low power consumption, high noise immunity, tolerance of wide power supply voltage variations, and the relatively higher level of integration, i.e. circuit functions per package, make it the obvious choice of logic to use in not only battery powered designs but also mains operated equipment. This is particularly so if power for the circuit is to be derived from the a.c. mains by means of a mains dropper resistor — a much cheaper solution than a mains transformer. With CMOS the total current consumption of the logic will probably be below 5mA as opposed to about 100mA for a comparable TTL design and, therefore, a low power mains dropper resistor will suffice.

Problems will, however, arise when the logic circuit has to interface with a high power a.c. load such as a mains lamp or motor. Here, two solutions are possible: a relay or a triac. The first device, a relay, uses a lot of power and currents of the order of tens of mA are required to keep the relay energised, which defeats the original object and prevents the use of a power mains dropper resistor.

TRIAC TRIGGERING

To investigate the possibilities of using CMOS to drive triacs it would be helpful to state the triggering requirements of these devices. Triacs may be triggered into conduction on both positive and negative mains half cycles, with either polarity of gate current. They are, however, more sensitive (i.e. require less gate current) to negative gate current. Triac triggering requirements are, in fact, normally specified for gate current polarities which are in phase with the main terminal voltage, i.e. main terminal voltage positive with positive gate current and main terminal voltage negative with negative gate current. These and the gate sensitivity for the case of main terminal voltage positive with a negative gate current are equal. Triacs are generally much less sensitive to positive gate current on negative mains half cycles (i.e. main terminal voltage negative) and need to be selected for applications which require this mode of triggering. The gate current may be d.c. or a pulse since the triac will remain on once it has been triggered, until the end of the mains half cycle.

The current required to trigger a triac will depend on the type of device used as well as the temperature. Higher power devices of 25A or greater rating may require up to 100mA to trigger while low power devices, 4A and less, may need only 10mA or less. Manufacturers generally state the maximum current required to trigger. Thus a triac type TAG250-400, for example, has a maximum gate current of 50mA and this is guaranteed to trigger all devices of this type. There will, of course, be many TAG250 devices which require a good deal less but unless the constructor has many such devices and can choose those with lower gate current, for good reliability he should aim to provide a current of 50mA.

Before gate current can flow, a certain voltage, the gate trigger voltage must be exceeded. This for the TAG250-400 is 2.5V maximum. Thus for a worst case device, the trigger circuit must provide a voltage of at least 2.5V plus the voltage required to drive 50mA through any reistance in series with the gate.

CMOS GATES AS DRIVERS

Unfortunately, CMOS gates, such as the 4001 or 4011, cannot provide anything like 50mA output current. The maximum current which can be supplied by CMOS devices is 10mA. Exceeding this limit will probably destroy the device. With a 5V supply, the output of a CMOS gate may drive a transistor base directly as the device will limit its output current to below 10mA, but above about 8V a current limiting resistor R will be required (see Figure 1).

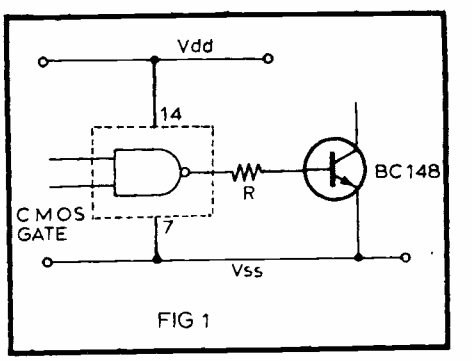


FIG 1

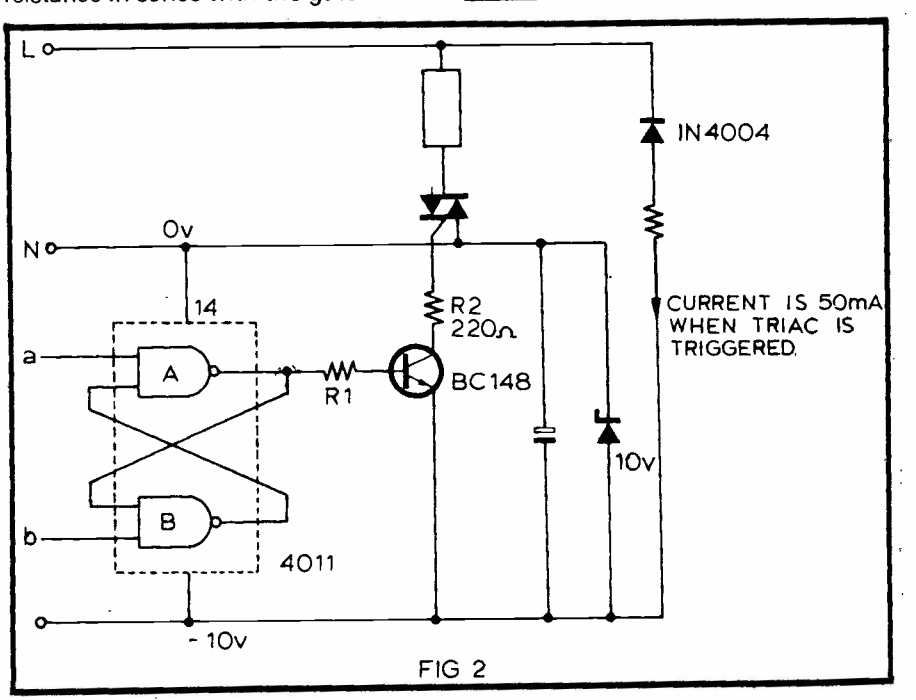


FIG 2

If the output of the gate is required to maintain a recognisable logic state when supplying output current, to drive another gate for example, then the current must be limited to below 1mA. Figure 2 shows a circuit for a bistable a.c. switch.

If input "a" is momentarily connected to logic 0 (negative supply rail) the transistor will turn on and trigger the triac, which will remain on until input "b" is connected to logic 0. Note that a negative supply is used to provide negative gate current for the triac. R2 is chosen to give the required 50mA gate current and R1 to give the required base current. Since gate A must drive both the transistor and present a defined logic level to gate B, the output current of gate A must be less than 1 mA giving R1 a minimum value of 10Kohm with a 10V supply. If the gain of the transistor is greater than 50, R1 may be increased in value, thus reducing further the current taken from the output of gate A.

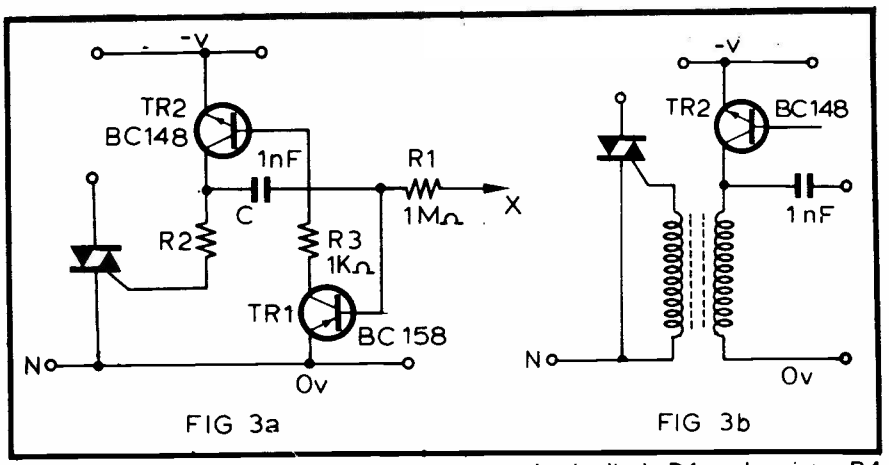
This type of circuit, however, still draws a large current from the supply when the transistor and hence the triac is on. This current, about 50mA must, of course, come through the mains dropper and defeats the object of low current consumption. We get round this by

PULSE TRIGGERING THE TRIAC

Use can be made of the fact that the triac will latch once it has been triggered. Thus the trigger current of 50mA pulses of short duration, the duty cycle of which may be such that the average current is only a few mA. The supply smoothing capacitor thus supplies the 50mA peak current while the mains dropper replaces the charge over a longer period and, therefore, needs to carry a current of only a few mA.

This is the principle behind the circuit shown in Figure 3. Transistors TR1 and TR2 form a circuit which oscillates at a frequency determined by C and R1 when point X is connected to the negative supply line. This can be done by a CMOS gate. The loading on the gate is minimal; about 10μA, but the circuit can supply 50mA pulses to the triac gate while keeping the total current consumption below 5mA.

The circuit has been used on a range of supplies from 3 to 15V with success, although, of course, less trigger current will be available with the lower supply voltages. It is, therefore advisable to use a supply voltage of at least 5V. The frequency of oscillation is also slightly dependent on the supply voltage but this is of little consequence.



When the circuit is not oscillating it draws very little current, and so stand-by power will be minimal.

In a circuit like this it is desirable that the frequency of the oscillator be at least 5KHz. This ensures that the triac is triggered as early as possible in each half cycle, minimising radio interference.

If isolation of the trigger circuit from the mains is required, then resistor R2 may be replaced by a transformer. This may be wound on a ⅜" diameter x 1¼" ferrite rod and consists of 10 turns of 28 swg wire for the primary and 10 turns for the secondary, insulated by a layer of PVC insulating tape.

Table 1 lists the supply current (Is) the gate current (Ig) and the frequency oscillation (F) for the circuit of Figure 3 supply as measured on a prototype when the supply voltage was varied between −3V and −15V, and no voltage applied to the triac. The two cases are R2 = 100 ohms and 47 ohms.

The circuit together with the CMOS gates thus forms a useful a.c. power switch as shown in Figure 4. When the ON button is pushed, the triac is turned on a supplies power to the load. Since the circuit latches, the triac will remain on until the OFF button is pushed.

The negative d.c. supply for the circuit is derived from the a.c. mains supply via diode D1 and resistor R4. The zener and capacitor stabilise and smooth the supply. The zener and capacitor stabilise and smooth the supply. The zener may have a breakdown voltage of anywhere between 5V and 15V. Since the current drawn by the circuit is only 1.5mA, R4 need only be a ¼ watt component.

If resistor R2 is replaced by a pulse transformer, then the current drawn by the circuit rises to about 2.5mA and resistor R4 may need to be reduced to 74Kohm.

APPLICATIONS OF THE CIRCUIT

The circuit of Figure 3 forms a low power trigger circuit for triacs and is, therefore, ideal for interfacing between these devices and CMOS digital integrated circuits. The cost of the extra transistor compared to that of Figure 2 is far outweighed by the reduced cost of the mains dropper. The difficulty of synchronising the circuit with the mains makes its use in phase control circuits (such as lamp dimmers) unattractive compared to programmable unijunction transistor (P.U.T.) trigger circuits, but in ON-OFF type switching applications it is superior.

By removing the push buttons and the 100Kohm resistors from the circuit of Figure 4, the load current may be switched on by a negative pulse to the input of gate A and off by a negative going pulse to the input of gate B. By suitably decoding the outputs of a digital clock and

TABLE 1

	Vs Volts	Is MA	Ig MA	Frequency KHz
R2=100Ω	3	0 15	20	5
	6	0 32	50	5
	9	0.45	70	5
	12	0.6	100	5.2
	15	0.85	120	6.25
R2=47Ω	3	0.25	35	5 3
	6	0 45	80	5.3
	9	0 6	140	5.3
	12	0 75	180	5 3
	15	1.0	200	6.0

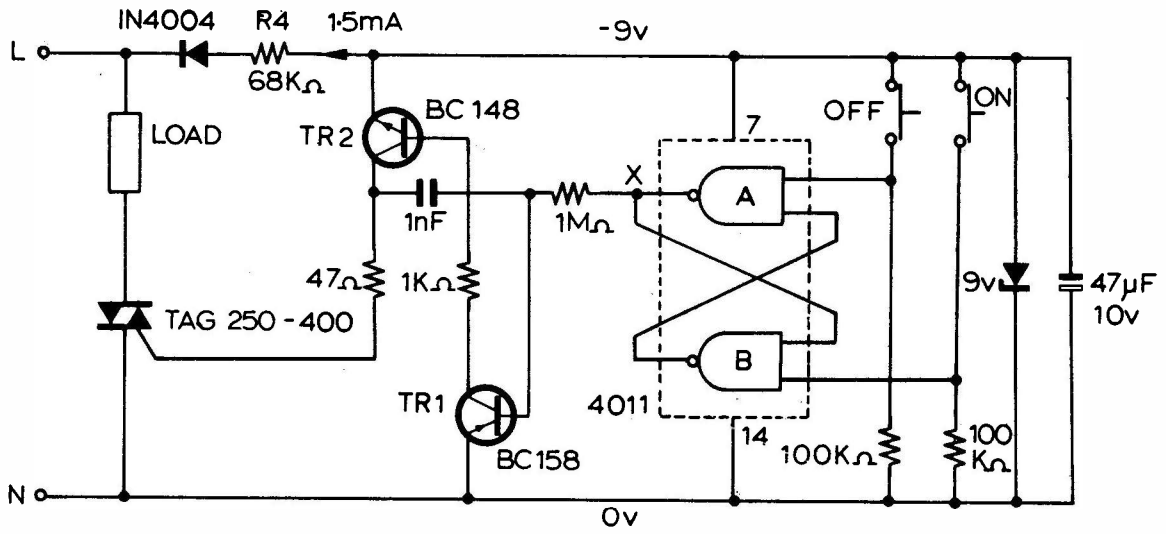


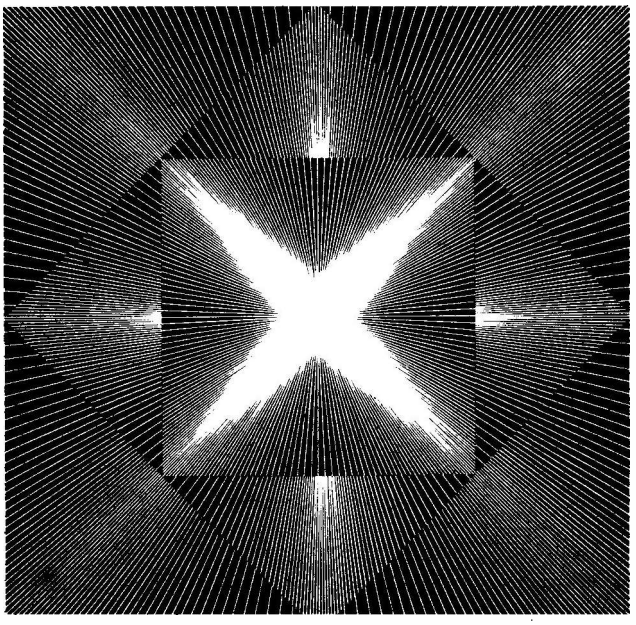
FIG 4

connecting these to gate A and B, the circuit could be used to switch mains and driven equipment such as lamps, tape recorders or central heating systems on and off at certain times. Power for the circuit could be obtained from the clock power supply line, as this would almost certainly be able to supply the small extra current required. The use of a pulse transformer (as shown in Figure 3b) would isolate the clock and decoding circuitry from mains.

Referring to figure 3, by making TR1 a BC148 (NPN) and TR2 a BC158 (PNP) and connecting the positive supply to the emitter of TR2 and negative to TR1 emitter, the circuit would produce positive going trigger pulses when X is connected to the positive line. The pulses applied to the triac gate could be made negative by correct phasing of the transformer windings. In this way the circuit may be used with a positive or a negative supply depending on which is available. ●

PRACTICAL GUIDE TO TEMPERATURE CONTROL

Temperature controlled systems are used throughout science and industry – in this series of articles Collyn Rivers explains how they work.



Accurate, repeatable temperature measurement and control is an essential requirement in many aspects of science and industry.

Many scientific experiments depend upon the maintenance of a stable temperature – often, as with pathological specimens, over long periods of time.

Even the cheapest usable laboratory ovens and water baths must therefore be capable of maintaining temperatures that are constant to within at least 1°C – in fact many will better this by a factor of at least two.

In the development of colour films on an industrial scale, large quantities of water must be held to close temperature limits, even in industries such as chicken hatching, large volumes of air must be maintained to astonishingly tight specifications.

THERMOSTATIC CONTROL

To various extents, all solids expand when heat is applied to them. Thus, when a metal rod is heated along its length, each unit of its length will become longer. This increase in length (per degree of temperature rise) is called the coefficient of linear expansion and has different values for different materials.

Table II shows the coefficient of expansion for various materials. The Table also shows the coefficient of volumetric expansion – which is roughly equivalent to three times the coefficient of linear expansion.

From Table II it can readily be seen that the volumetric expansion of mercury is over six times that of glass, and that the linear expansion of copper is considerably greater than that of say, invar, (invar is an alloy containing 36 percent nickel and 64 percent steel).

It is this difference between expansion rates that is exploited in devices such as thermometers and thermostats.

The simplest form of thermostat consists of a bimetal strip – usually invar and brass. As temperature rises, the brass expands more than the invar thus causing the strip to bend. This movement is used to open and close a pair of electrical contacts which in turn make and break the electrical energy supplied to the heating (or cooling load. (Fig. 1).

The thermostat is located within the area to be controlled – for example, in a laboratory water bath the thermostat will be immersed in the bottom of the bath.

A thermostat of any type is simply an 'on/off' device: it is either open or closed. This effect is shown diagrammatically in Fig. 2. Here the upper line represents the thermostat movement whilst the lower line shows the current flow through the heating element which is controlled by the thermostat. At the lowest temperature the bimetal strip is straight and the contacts are closed – hence current flows through the heating element and temperature begins to rise (T1). For a time, temperature rises and as it does so the bimetal strip begins to bend. At a certain temperature – determined by the characteristics of the bimetal strip

TABLE I

SCALE	MELTING POINT	BOILING POINT	SYMBOL
Celsius (Centigrade)	0	100	C
Fahrenheit	32	212	F
Reaumur	0	80	R
Absolute Celsius	273	373	K
Absolute Fahrenheit	492	672	–

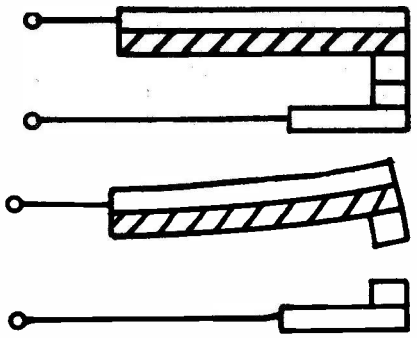


Fig. 1. Basic thermostat: when heated, brass (shaded) portion expands more than invar thus causing strip to bend and contact to open.

and the spacing of the electrical contacts – the bimetal strip bends sufficiently to open the contacts (T2) and the heating stops.

Thus the thermostat oscillates between maximum temperature (contacts open) and minimum temperature (contacts closed). This variation is known as the 'differential' of the thermostat, and in top quality units may be as little as ½°C.

It should however be clearly understood that the temperature differential described above is that achieved once the heated system has reached a state of equilibrium. During the initial process of coming up to the desired temperature, the system may well 'overshoot' by quite a substantial amount. This action may then be followed by several swings of temperature – diminishing in amplitude – above and below the required set point.

The amount of initial overshoot is a function of the design of the complete heating system – including the electrical size of heating elements, time taken for the thermostat to respond to temperature change etc. It may be reduced by careful design but can rarely be eliminated conpletely. Hence on/off control systems must only be used where these initial characteristics can be tolerated.

A further article in this series will describe various types of proportional controllers – which do not exhibit this overshoot characteristic.

Precision thermostats, such as those used for laboratory applications, whilst still exploiting the basic principle of different coefficients of linear expansion – do not use bending bimetal strips. Generally they use long rods of brass or copper located within an invar framework. One end of the rod is rigidly clamped to the invar frame and the other end is linked to electrical contacts via a lever mechanism that magnifies the relative movement between the two brass rod and the invar framework.

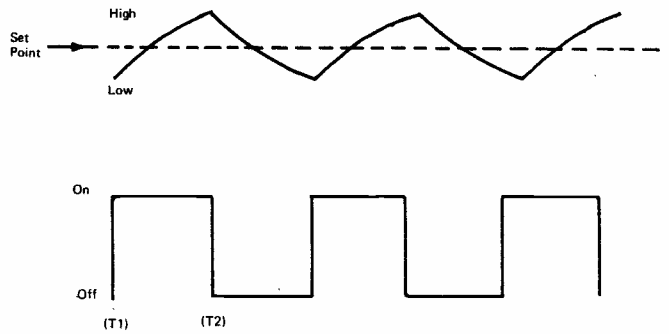


Fig. 2. Operation of thermostat above and below set point, upper curve shows temperature of load, lower curve shows heater being turned on and off.

This type of precision thermostat is necessarily large and is therefore only suitable for large ovens and water baths – or other applications where space is not at a premium. Nevertheless they can be very effective devices indeed and differentials of 0.1% have been achieved.

A major disadvantage of nearly all electric thermostats is that the contacts are used to interrupt the heating load current, which, in large ovens or water baths may be at least ten to fifteen amps.

This results in two problems – with a common cause.

Thermostat contact points open and close fairly slowly, and because of this a certain amount of arcing takes place. Unless the thermostat is very conservatively rated, the contact points become burnt and pitted and must be replaced at frequent intervals. Failure to do so may well result in the points welding together and thus supplying power continuously to the heating element. If the element is used to heat a pathological oven, months of research can literally be burnt up in less than half an hour. Many a tankful of tropical fish has perished for the same reason.

The second effect of point arcing is that the heat generated in the arc disorts or expands some parts of the thermostat, thus affecting its operating accuracy.

To overcome these problems, a few top quality ovens use the thermostat merely as a switching device to control a main power contactor.

Practically throughout science and industry, and shortly to become common useage elsewhere, temperature measurements are quoted in degrees Celsius.

Earlier, a centigrade scale was proposed by Celsius, a Swedish astronomer. This term was used extensively until 1948 when, at an international conference, the word 'Celsius' was adopted in place of 'centigrade' – a term which is also used to define one hundredth part of a grade (part of a European scale in which a circle is divided into 400 grades).

The Celsius scale has now been adopted by Standards Institutes worldwide for use in scientific work. Units are expressed in degrees Celsius – often abbreviated to °C.

An absolute Celsius scale (Kelvin scale) is also used in scientific calculations. In this system, zero degrees represents the total absence of heat. Units are expressed as degrees Kelvin – or °K.

The Fahrenheit scale is still used in some parts of the world in medicine, engineering, meterology, and for domestic purposes.

All conventional temperature measurements are based on two fixed reference points which are both stable and easily reproducible.

The lower of these two points, 0°C (273°K) is defined by the temperature of melting ice. This is measured at an external pressure of 760mm of mercury at sea level on latitude 45°.

The second point defines 100°C (373°K) and is based on the boiling point of water – measured under the same conditions.

Two further reference points are sometimes used. These are the boiling point of sulphur (444.6°C) and the melting point of gold (1063°C).

Relationships between these three scales are shown in Table 1 – which also includes the Reaumur scale. This latter scale is still used in parts of Europe for domestic temperature measurement.

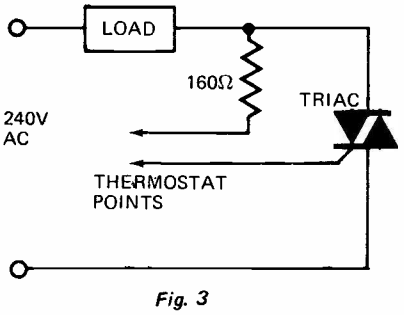


Fig. 3

This method is effective, but expensive and clumsy.

A far simpler method of overcoming the problem is to use the thermostat contacts in the gate circuit of a suitably rated Triac which in turn switches the heating load. This overcomes all the problems in one go and is both cheap and effective.

The writer of this article has modified several hundred laboratory heating systems in this way over the past eight years – and without exception none has since required any further attention to contact points. A further bonus is that the temperature regulation of the device is frequently improved – by as much as 50 to 75 percent.

Figure 3 shows how the modification is made. If installing this modification. bear in mind that the Triac assembly must be mounted in the coolest possible location and not within the heated part of the oven!

CONTACT THERMOMETERS

The construction and use of the mercury-in-glass thermometer is familiar to us all. The contact thermometer is in essence a standard thermometer of this type but modified to incorporate electrical contacts.

In its simplest form the contact thermometer is made to switch at a specified temperature. A typical example of this type of thermometer is shown in Fig. 4. Here, one wire is in permanent contact with the mercury pool in the thermometer bulb – a second wire is attached to the inner face of the tube and this is contacted by the mercury at the predetermined temperature.

An adjustable form of contact thermometer is shown in Fig. 5. In this device the leads enter the glass tube via a plastic cap. A magnet mounted on this cap is used to rotate an internal armature; this is attached to a fine threaded spindle terminating in a platinum contact, the operating temperature of which is read from a calibrated scale.

Although far more fragile than electro-mechanical thermostats, contact thermometers are simple devices capable of accurate, repeatable switching for millions of operations. The switching differential is largely a function of the range that must be covered – but accuracies of 0.1% and better are quite common; and thermometers with a differential of as low as 0.001% (over limited ranges) can be obtained.

Contact thermometers are less commonly used than they deserve to be – probably because they were developed many years before the introduction and commercial acceptance of cheap simple circuitry that was capable of exploiting their switching capabilities: for contact thermometers have what was at one time a major drawback – that is that they can only switch very low currents and voltages. This switching capability is limited to preferably less than five to ten volts – the lower the better within reason – and the current flow should be less than a few milliamps. If these limits are exceeded, changes within the mercury will shorten the unit's life quite drastically – and apart from this the heating effect of the current (which must inevitably pass through the mercury cloumn) will grossly affect the switching accuracy.

TABLE II
Coefficients of expansion (per $^{o}C \times 10^{-6}$)

SUBSTANCE	LINEAR	VOLUMETRIC
Aluminium	23	69
Brass	18.9	56.7
Copper	16.8	50.4
Glass	8.6	26.4
Pyrex glass	3.2	9.6
Invar	0.9	2.7
Quartz	9.4	1.2
Steel	10.7	32.1
Tungsten	4.5	13.5

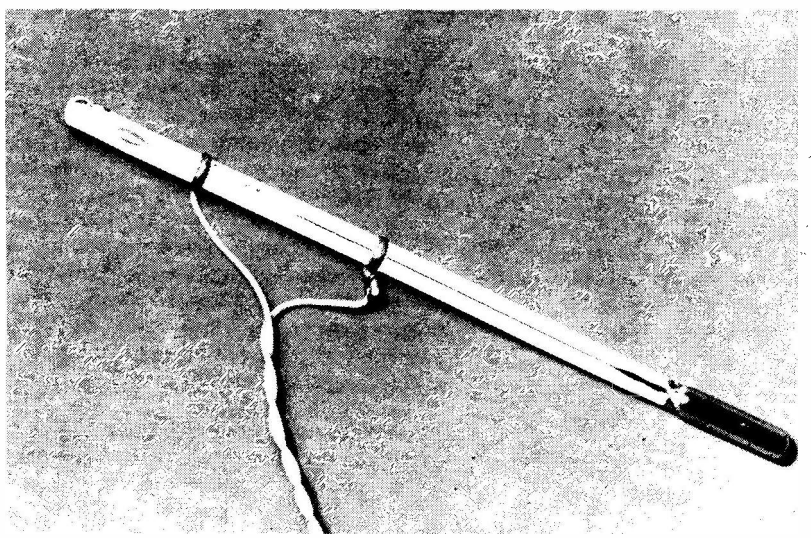


Fig. 4. Basic contact thermometer – designed to switch at 40°C. At that temperature, the expanding mercury touches the second contact point.

Originally, complex valve amplifiers were used to magnify the low acceptable switching currents to a level which could be used to drive a load contactor – these were clumsy and expensive – although incredibly enough, several companies still have such anachronisms in series production.

Unlike thermostats in which the contact points close as the temperature falls – and thus reapply power to the heating load – contact thermometers switch 'on' as the set point is reached. This is of course an ideal characteristic for refrigeration loads but is the opposite to that normally required for heating loads.

Nevertheless a Triac switching circuit may be used – switching the Triac 'off' as the desired temperature is achieved. One method of achieving this is shown in Fig. 6.

In operation, when the contact thermometer is 'open', the capacitor is charged via the 150k resistor until the breakover voltage of the trigger diode if reached – usually around 30 volts – the diode then breaks down triggering the triac into conduction.

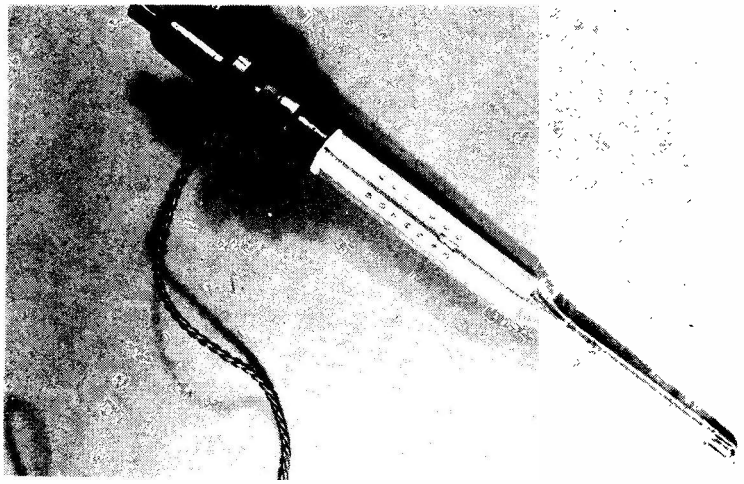


Fig. 5. Adjustable contact thermometer. Rotating upper magnet assembly (in top hat fitting) is used to adjust switching temperature — here set at 35°C.

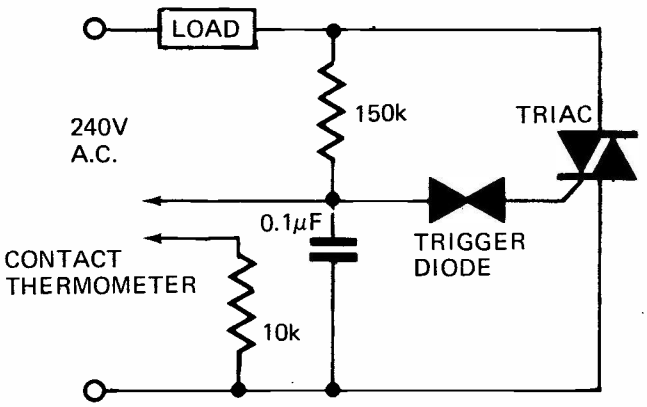


Fig. 6

The power loss caused by the minor phase shift is negligible).

Subsequently, when the contact thermometer 'closes', the capacitor is prevented from reaching the trigger diode breakover voltage and the triac is prevented from conducting.

In practice this circuit works very well indeed, although it may occasionally be necessary to select triacs capable of switching reliably at low trigger energy levels. The voltage applied across the contact thermometer is higher than desirable but in practice problems are rarely experienced.

A more elegant (but also more costly) version of this circuit is shown in Fig. 7. This latter circuit should preferably be used in critical applications. Both switching voltage and current is much lower than in the version shown in Fig. 6. In this circuit the contact thermometer is wired across the capacitor in a UJT firing circuit. When the contact thermometer is 'closed', the capacitor is prevented from reaching the UJT valley point (or 'firing') voltage and thus the triac is not triggered.

This is an excellent circuit for controlling laboratory water baths and ovens for applications where the characteristics inherent in 'on/off' control systems are acceptable.

Yet another method — originally developed by General Electric in the USA — uses an SCR connected within a full-wave bridge. (Fig. 8).

With the contact thermometer 'open', the SCR will trigger on each half cycle and deliver power to the heater load. When the contact thermometer 'closes', the gate of the SCR is effectively held at SCR cathode potential and is therefore prevented from triggering. Thus power is removed from the heating load. In this circuit the maximum current through the contact thermometer is about 250 uA.

This circuit (Fig. 8), whilst limited to switching loads of less than 150 watts or so, is reliable, cheap and simple. It is an excellent temperature control system for small fish tanks, or other similar applications where only low energy heating elements are used.

As with electro-mechanical thermostats, contact thermometers are strictly 'on/off' devices, and because of this the heating element that they control (and hence the controlled volume) will continuously cycle above and below the 'set point'.

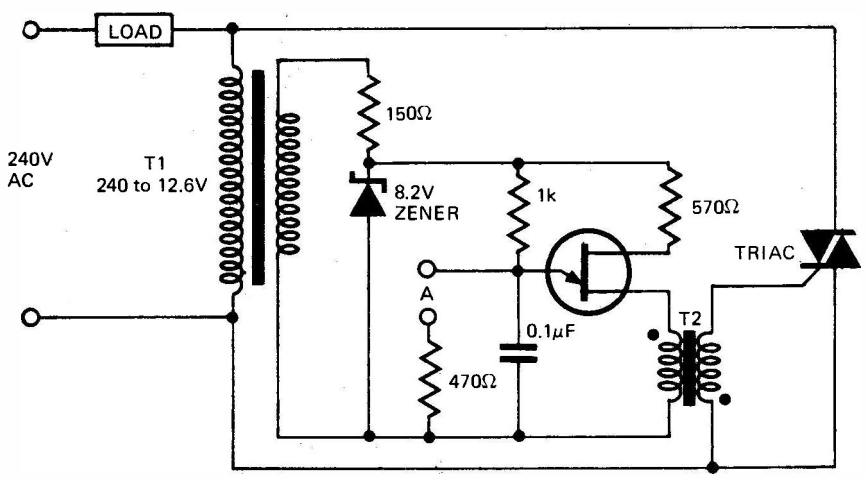
This characteristic in inherent in this — and other — types of control systems, but in a well designed system the variations may be well within the permissible limits. In fact using these techniques the writer has successfully designed laboratory water baths and ovens with an overall temperature diffentential of less than 0.1%. One small water bath was produced with a differential of less than 0.05%.

The following points should be noted by experimenters seeking to obtain optimum accuracy and long term stability when using contact thermometers.

a) The exposed glass column may be at a different temperature from the bulb. This may cause non-uniformity in the temperature of the mercury column. Where possible ensure that the whole thermometer is at the same temperature. If the thermometer is immersed in liquid, ensure that as much as the cc column as possible in immersed. If an immersion level is specified, ensure that is is maintained.

b) Glass is slightly plastic, and if the contact thermometer is changed from a high temperature to a low temperature there may be errors of up to 0.5°C until the glass returns to its original dimensions. This may take several weeks.

c) As the glass ages, there will be a slight decrease in the volume of the bulb. This may cause an error of up to 0.2% over a period of five to ten years.



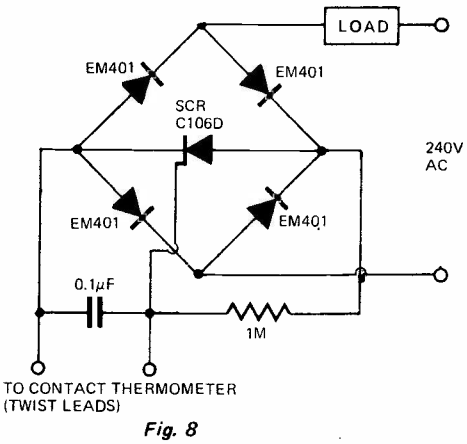


Fig. 8

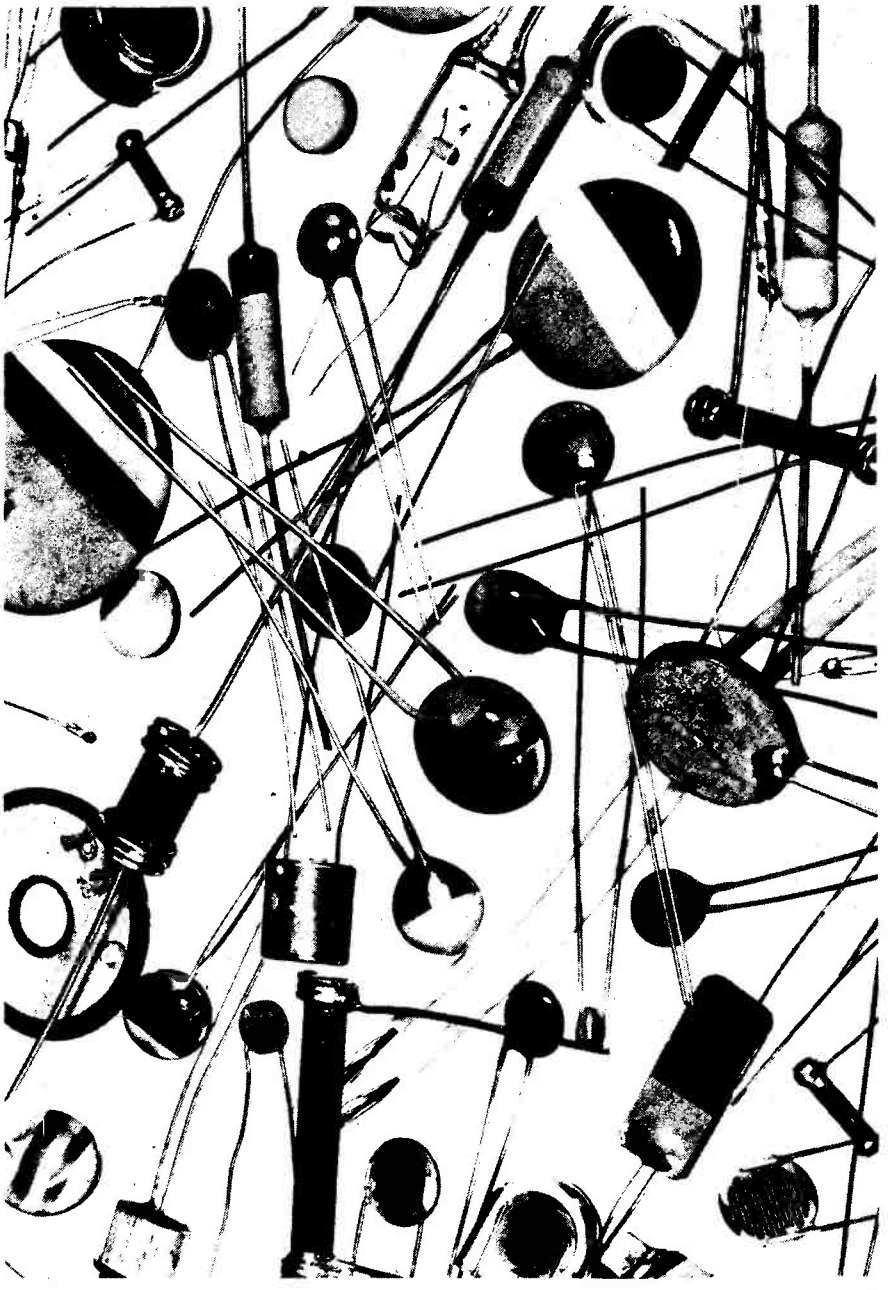
PRACTICAL GUIDE TO TEMPERATURE

In this article, Collyn Rivers shows how thermistors are used for temperature control.

Thermostats and contact thermometers – described in the first part of this series are essentially 'on/off' devices. They cycle continuously above and below the required temperature.

Their major limitation is that (with few exceptions) they can only control energy on an 'all or none' basis. It is because of this that the majority of heating systems controlled in this way are characterized by a large overshoot when initially coming up to the set temperature.

This problem is overcome by using sensing elements in which changing temperature causes linear changes in one or another electrical parameter. Of these, the most commonly used are thermistors, resistance thermometers, and thermocouples.



THERMISTORS

Thermistors are temperature-dependent resistors generally having a negative temperature coefficient. Thus, the resistance of a thermistor decreases as the temperature increases. This change in resistance is typically between 3% and 6% per degree Celsius at room temperatures.

In construction, thermistors are small, solid, semiconductors made of various metal oxides. They are produced in several shapes and sizes as rods, discs, beads, washers, and flakes.

For temperature control applications, the thermistor is located within the space to be controlled. A small current is caused to flow through the thermistor and the resultant voltage drop – which is proportional to temperature – is compared with a reference voltage. Any resulting difference voltage is used to control the energy applied to the heating elements.

Figure 1 shows the relationship between resistance and temperature for 14 different thermistors. Taking the lowest curve as an example, it can be seen at –25°C the resistance is 50k. This is reduced to approx 5k at 0°C and finally to around 40 ohms at 200°C. The resistance (4.7k) shown on the right side of the graph is the resistance at 25°C, and it is at this temperature that the 'resistance' of any specific thermistor is generally given. The graph shows thermistors in which the 25°C resistance may vary from as little as 4.7k to as high as 680k. Thermistors are available with 25°C values as low as 2 ohms.

The 25°C resistance value of a thermistor becomes stable after a thousand or so hours of use, but before this time has passed, quite considerable changes may take place. Figure 2 shows a plot of percentage change in resistance value against elapsed time for two commonly used thermistors. It is clear that for good

CONTROL Part 2

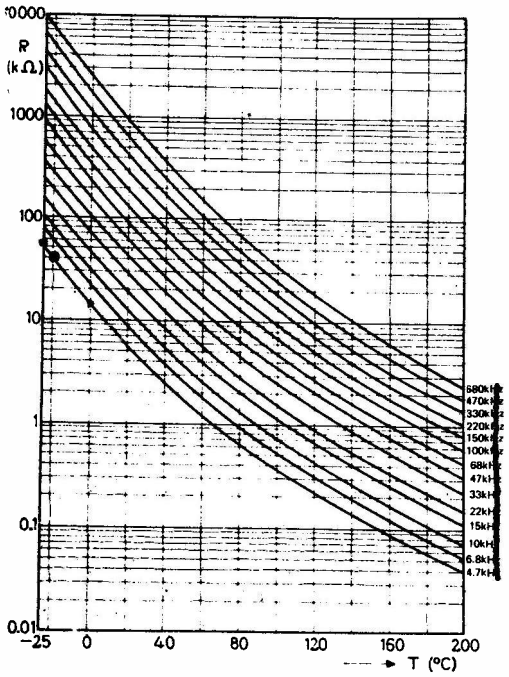


Fig. 1. Relationship between temperature and resistance for 14 different thermistors.

stability, thermistors must always be aged (at high temperature) before use in critical applications. Always so if they are to be used for temperature measurement.

Although as described earlier, thermistors enable control circuitry to be used in a manner other than straight 'on/off' control, many thermistor controlled circuits still have the basic 'on/off' characteristic. However as the response time of a thermistor may be much quicker than that of a thermostat or contact thermometer, 'on/off' thermistor controlled circuits generally have far less initial overshoot.

SIMPLE THERMISTOR CONTROL

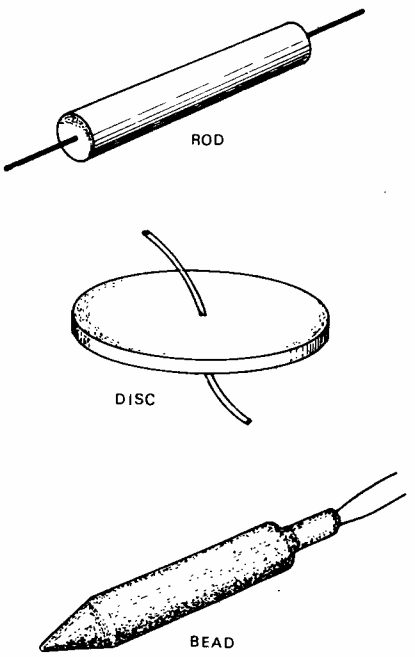
A relatively low cost on/off type thermistor controller is shown in Fig. 3.

This is a simple circuit ideal for controlling ovens, hot plates, soldering irons, water baths etc. The circuit will control the temperature to within one degree or less over a temperature range from 0°C to 100°C.

Transformer TI may be an old filament transformer having two secondary windings, each of 12.6 volts, 0.5 amps or so. Winding WI supplies energy to the relay RL1 through SCR1, the second winding (W2) supplies 12.6 volts ac to the bridge circuit of thermistor R1, resistors R2 and R3, and temperature setting potentiometer RV1.

Power is supplied to the heating element via the 'normally open' contacts of relay RL1. In other words power is applied to the load when the relay coil is energized.

When the heating load is colder than required, the resistance of the thermistor will be higher than that of potentiometer RV1 and this unbalances the bridge in such a way that a positive voltage is applied to the gate of SCR1 when its anode is positive. This causes it to trigger and, hence power is supplied to RL1. The contacts of RL1 close and power is applied to the heating elements of the load.



Construction of various types of thermistors

As temperature increases, the resistance of the thermistor decreases until eventually it becomes less than that of RV1. This unbalances the bridge in the opposite direction and now a negative signal is applied to the gate of SCR1 while the anode is positive.

The SCR now turns off, thus de-energizing RL1, and hence removing power from the load.

The type C106 SCR chosen for this circuit can handle relay coil operating currents up to a couple of amps. This

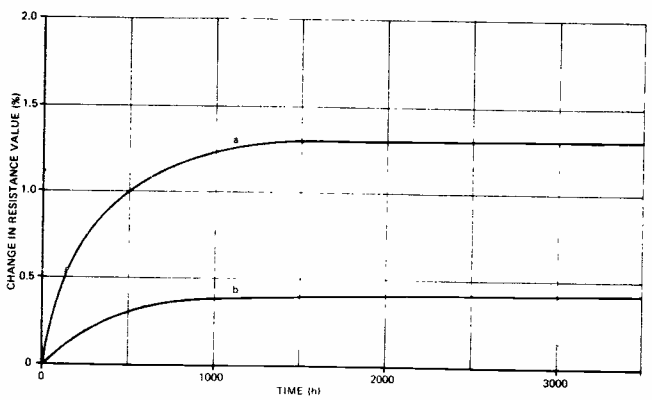


Fig. 2. How thermistors change characteristics during initial period of use. (a) Disc type thermistor with 1 watt load (b) Miniature bead type thermistor with 20mW load.

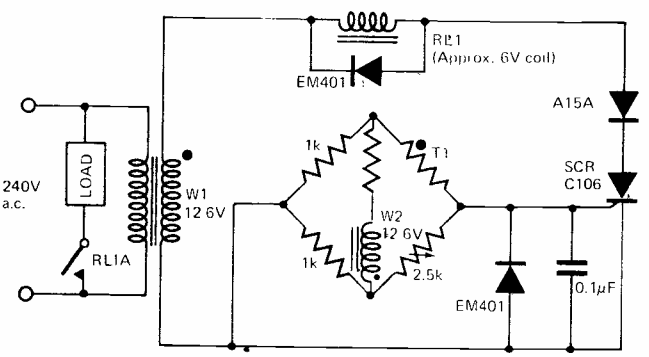
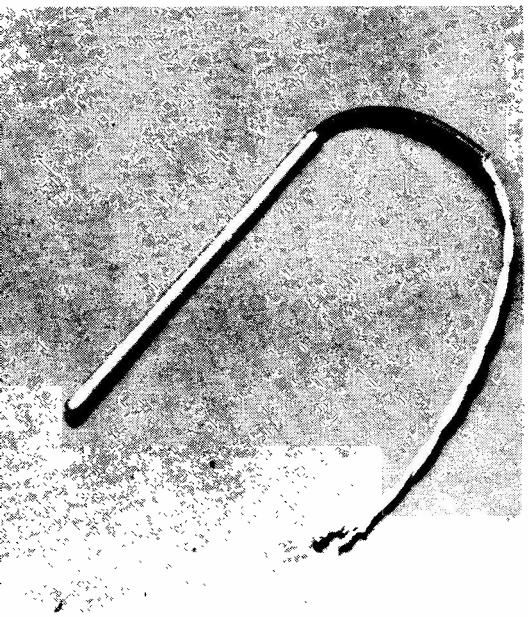


Fig. 3. Versatile low-cost controller.



Thermistor protected by metal sheath operates to 300°C.

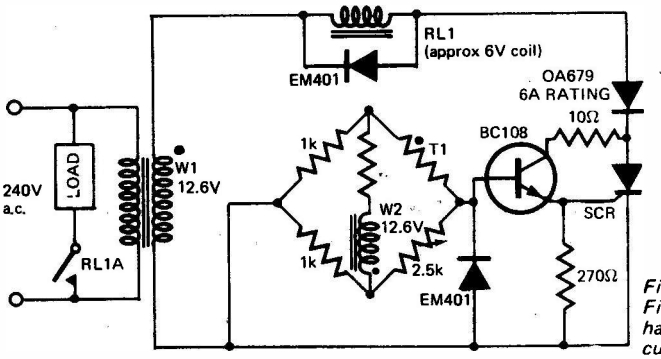


Fig. 4. Basically similar to Fig. 3, this circuit can handle relay operating coil currents of up to six amps.

is adequate for a fair sized relay capable of switching at least ten to fifteen amps. Heavier loads (including three-phase loads) can be handled either by using RL1 to energize a larger contactor or by modifying the circuit to obtain a larger triggering signal capable of controlling a heavy current SCR.

A circuit capable of switching six amp coil currents is shown in Fig. 4. Operation of the circuit is similar to that described for Fig. 3. except that transistor Q1 is used to amplify the bridge output signal.

Either of the circuits shown in Figs. 3 and 4 may also be used to control cooling loads — such as fans, refrigerators, air conditioners etc. The required 'opposite' operation can be achieved simply by connecting the load to a pair of normally closed contacts on RL1 — or by reversing the leads on the transformer secondary winding W2.

The thermistor chosen for the applications described above should have a resistance of approximately 1000 ohms at a temperature halfway up the control range required.

The circuits shown in Figs. 3 and 4 have very considerable operational flexibility, for within the triggering and current handling limits of the SCR, a relay may be chosen to suit the characteristics and size of the load. Thus either single or three-phase loads of practically any voltage and current may be catered for.

TOTALLY SOLID-STATE CONTROL

Although the circuits shown in Figs. 3 and 4 are extremely reliable there are many applications in which a totally solid-state system is to be preferred, for if correctly designed, a totally solid-state system is inherently more reliable and practically maintenance free.

Another major advantage of solid-state electronic control systems is that proportional control may readily be obtained.

Unlike the 'on/off' system in which full power is applied to the load until the required temperature is reached, proportional control continuously varies the power applied to the heating element in an amount depending upon the deviation between the actual temperature and the required temperature (Fig. 5).

Solid-state controllers — apart from having either 'on/off' or proportional control — may be categorized as using either phase control or zero voltage switching techniques.

Phase control is a technique used to control the effective power input to a load by a process of rapid on/off switching. In this the ac supply is connected to the load for a controlled (but variable) fraction of each half cycle.

This type of circuit, although inherently suitable for proportional control applications, generates large amount of radio interference, primarily at low and medium frequencies. It seriously affects reception of long and medium wave radio transmissions and may also interfere with audio equipment.

Whilst the extent of rfi may be reduced by filtering, the size of chokes required for large loads — such as heating systems — becomes excessive.

Phase control also introduces another problem — namely power factor. This is adversely affected and some power supply authorities object to this quite strongly.

Zero voltage switching overcomes most of the problems inherent in phase control systems.

The technique differs from phase control in that line voltage is switched

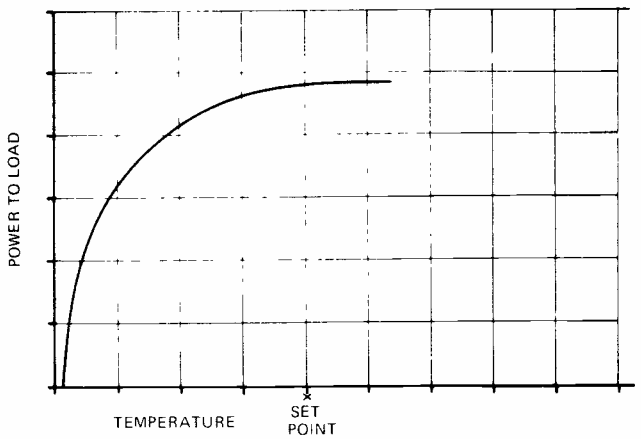


Fig. 5.

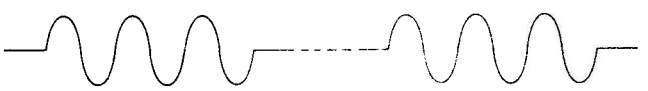


Fig. 6. Zero-voltage switching waveform

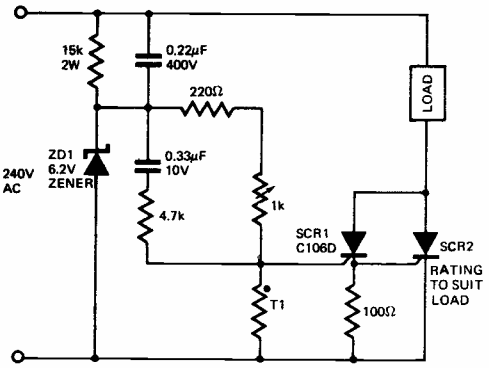


Fig. 7. Basic half-wave zero-voltage switching circuit.

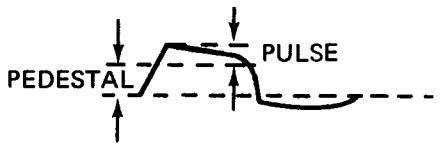


Fig. 8. Pulse and pedestal wave-form of circuit shown in Fig. 7.

'on' as well as 'off' only at the zero crossing points on the ac waveform. The power applied to the load is controlled by varying the ratio of time that power is applied, to the time that power is switched off.

At first sight this technique appears similar to the basic 'on/off' thermostat systems — and so to a point it is. The main difference is that power is switched only at zero crossing points of the ac waveform — apart from this the 'on/off' cycle may be very much quicker. For example, if only a small amount of power is required to maintain the set temperature, the circuit may pass only a few complete half-cycles and then remain switched off for a further twenty or thirty complete half-cycles before repeating the sequence (Fig. 6). A simple zero voltage switching circuit is shown in Fig. 7. In this circuit there is also a 'half power' mode within the temperature differential in which every second sine-wave is applied to the load.

The sensing differential of this circuit is approximately ±1/4°C about the set point and neither changes in ambient temperature not line input voltage degrade the accuracy.

The action of the circuit is as follows: Zener diode ZD1 forms a voltage pedestal of 6.2 volts (nominal) amplitude by clipping the incoming 240 volt ac supply. This pedestal is differentiated by capacitor C2 and resistor R2 to form a pedestal of reduced amplitude with a pulse superimposed on top of the pedestal (Fig. 8). This waveform is then applied to the gate of SCR1.

Zero voltage switching action is provided by the pulse (which is superimposed on the 'pedestal' at the beginning of the positive going line voltage) appearing at the anodes of SCR1 and SCR2. This pulse is shifted to the correct phase by C1 and R1.

As the controlled temperature approaches the set point, the decreasing resistance of the thermistor continuously decreases the height of the pedestal until the amplitude of the pulse plus pedestal is insufficient to trigger SCR1.

The lock-in configuration of SCR1 plus SCR2 virtually eliminates errors due to ambient temperature variations affecting SCR2 trigger voltage.

As the heating load of this circuit is in series with an SCR the power applied to the load will be half-wave. This may not necessarily be a severe limitation as many heating elements have more than sufficient heating capacity, and the inevitable loss when only halfwave power is applied may well be acceptable. If an element is being constructed specifically for the application then of course the element may be designed for half wave power.

The zero voltage switching action of this circuit eliminates the need for rfi filtering. Hence the cost is very much lower than a comparable phase control circuit in which rfi components would be necessary.

SIMPLE PHASE CONTROL

The zero voltage switching circuit shown in Fig. 7 should be compared with the phase control circuit shown in Fig. 9. This latter circuit has a very similar performance and — with the exception of rfi components — similar cost. It is commonly used to control the temperature of photo-developer baths. Again like the circuit shown in Fig. 7 it has half-wave output.

The 10 megohm potentiometer connected from the positive rail to the emitter of the unijunction controls the 'gain' of the circuit. In effect it controls the temperature range over which proportional action is obtained. It is not an essential feature of the design and may be omitted (or replaced by a suitable value fixed resistor if required).

Shown in Fig 10. is a full-wave version of the circuit described above. The basic operating principle is similar, the main difference being that a Triac is used in place of the SCR. The pulse transformer shown in this circuit consists of two windings, each of approximately 100 turns of 24G enamelled copper wire, on a ½" diameter ferrite rod. Each winding must be well insulated from the other, and from the ferrite rod. Construction of this pulse transformer is not at all critical and minor variations from the specification should not affect operation of the circuit.

It should be noted that both these phase control circuits result in ac potential being applied across the thermistor. This may be overcome in the latter circuit by supplying the firing circuit via an isolating transformer rather than via a dropping resistor. ●

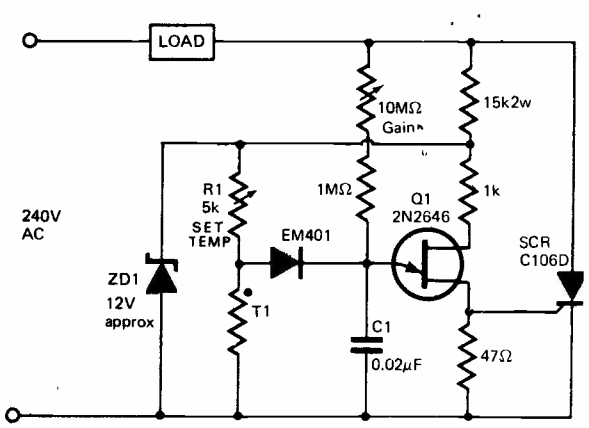


Fig. 9. Half-wave phase control system.

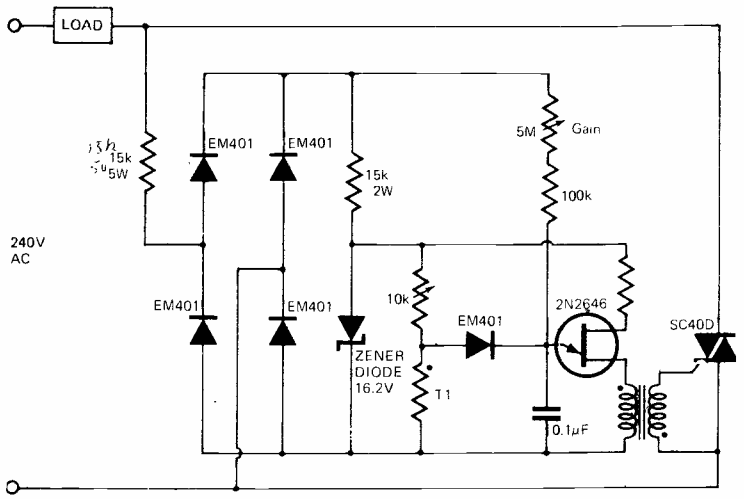


Fig. 10. Full-wave version of phase-shift controller shown in Fig. 9.

PRACTICAL GUIDE TO TEMPERATURE CONTROL Part 3

In this article Collyn Rivers explains how to obtain really precise temperature control.

The temperature control circuits described in parts one and two of this article are capable of maintaining temperatures to within ½% to 1% of the 'set' temperature.

A temperature differential of this magnitude is adequate for the vast majority of engineering and laboratory applications. Nevertheless there are some applications where a temperature differential of 0.1% or better is required. Here then are two circuits capable of maintaining temperatures within this level of accuracy – we have also included a simplified version of one of these circuits which can maintain temperatures within 0.15%.

All three circuits utilize the 'zero-voltage switching' technique in which the output Triac is switched on for entire cycles and off for entire cycles, control being achieved by varying the ratio of 'on' cycles to 'off' cycles.

The circuits shown in this article are all capable of 'slave-driving' a number of additional Triacs each supplying a separate heating element. Thus heating loads varying from a few watts to many thousands of watts may be controlled by selecting Triacs of the required ratings in suitable combinations. It must however be borne in mind that massive heating control systems are generally more economic to build using inverse-parallel SCR's.

Figure 1 shows a control circuit capable of maintaining a differential better than 0.1°C at temperatures between 10°C and 150°C.

In this circuit D1,R1,R2, and Zener diode ZD1 provide a regulated dc power supply for the sensing circuit consisting of the thermistor (Th), R3, D2 and 'temperature set' potentiometer RV1. Power is also supplied by this circuit to transistorQ1 and Q2.

A change in the resistance of the thermistor causes a change in the base current of Q1. This change is dc amplified and is then used to turn the SCR on or off. The SCR, in turn, synchronously clamps and unclamps the mains-derived trigger voltage to the

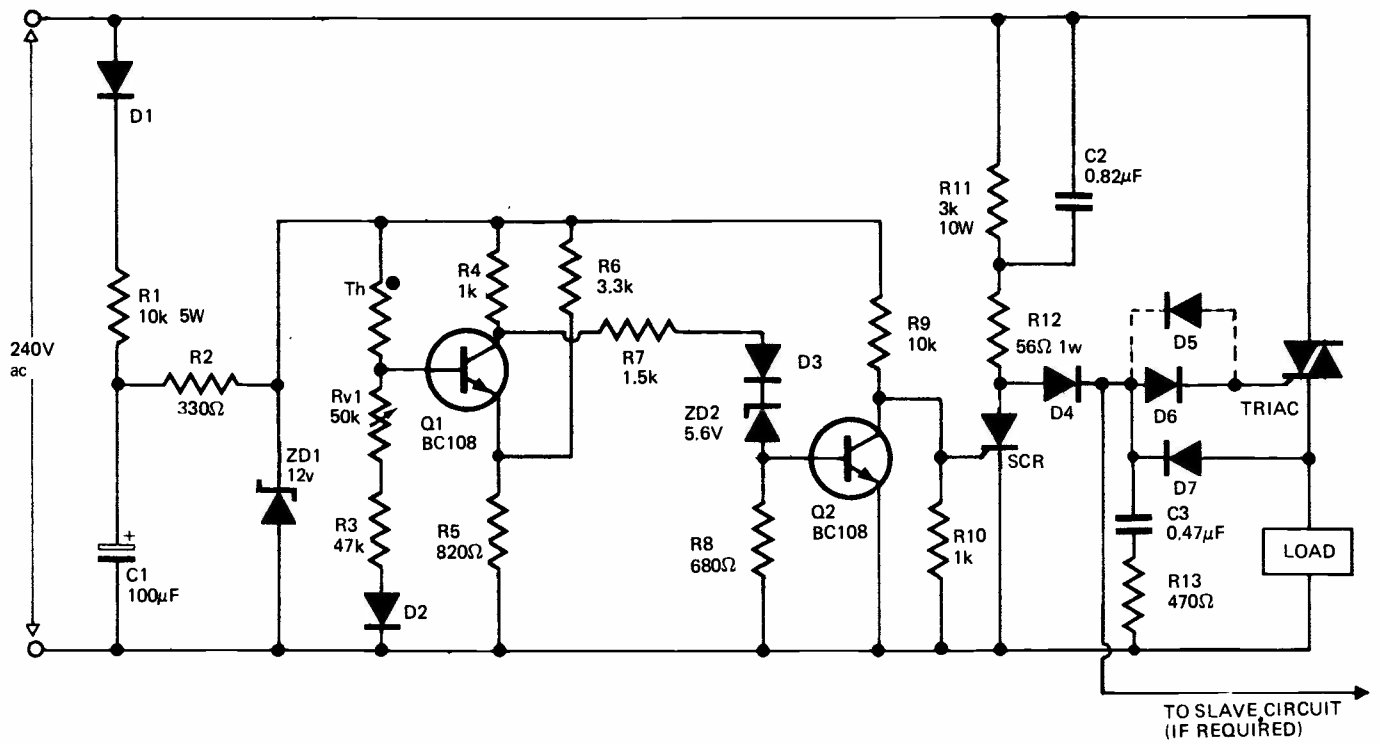


Fig. 1. Triac should be selected to suit the load, thermistor resistance should be approximately 100k at sensing temperature.

Triac.

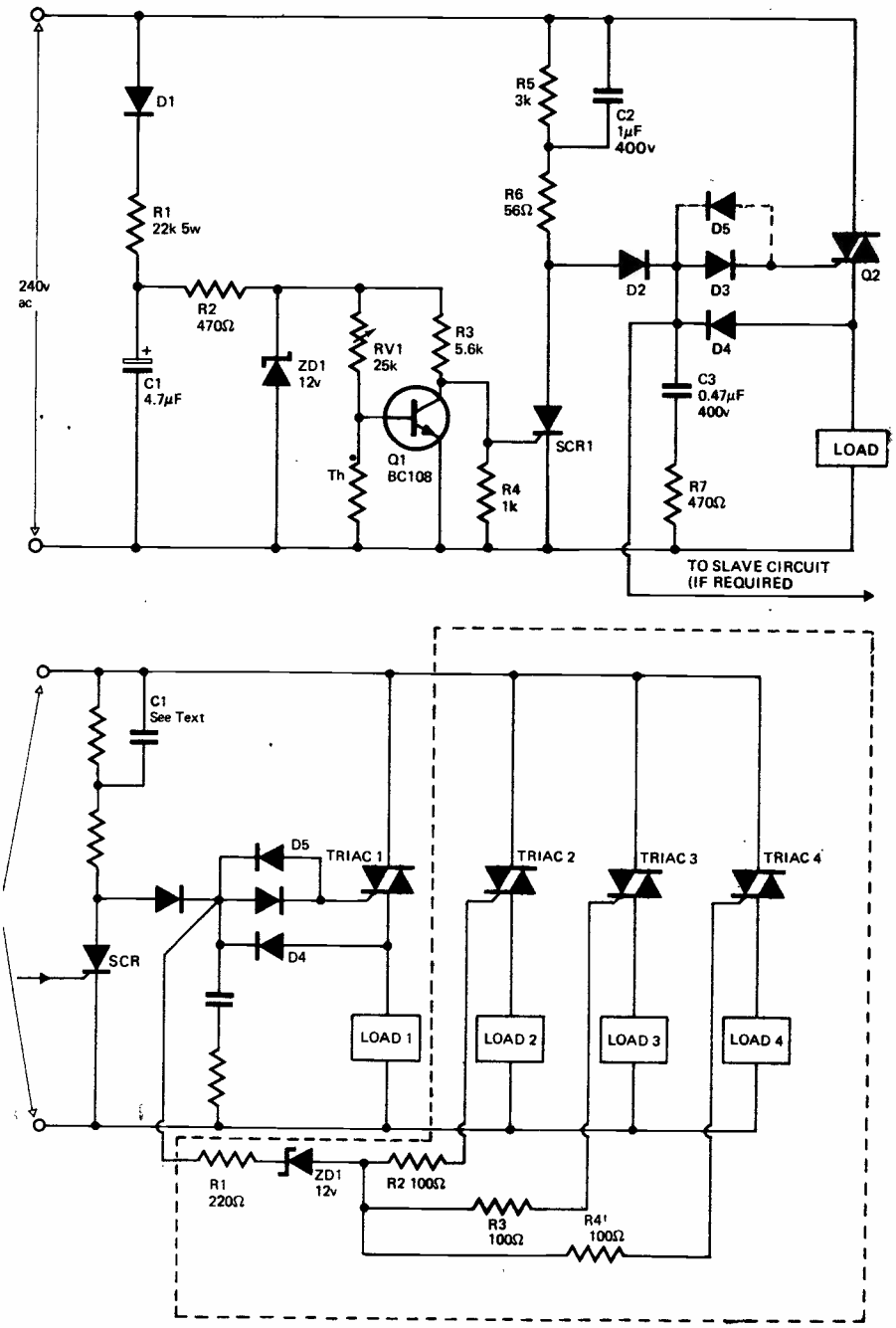
The triggering action is slightly more complex than at first it may appear. Assuming that the SCR is in the 'off' state, the Triac is triggered via R11, C2, R12, D4 and D6 during the initial period of the positive going sine-wave of the 240 volt line. As soon as line voltage appears across the load, capacitor C3 charges positively (relative to the low side). At the start of the negative-going part of the mains waveform, C3 (which still carries a positive charge), discharges via D6 thus triggering the Triac for the negative going half-cycle.

Diode D5 – shown dotted in Fig.1 – is used only when the circuit is used to slave-drive other Triacs. If only one Triac is used then D5 may be omitted.

Again, when only one Triac is used in this circuit, it may be necessary to increase the value of capacitor C2 in order to reduce the conductive RFI caused by a small notch formed at the beginning of the positive going waveform.

Figure 2 shows a simplified version of the above circuit. In this version, temperature may be controlled within 0.2°C between 10°C and 150°C.

Circuit operation is very similar to that of Fig.1, with the exception that only one transistor is used. The differential of this circuit is largely a function of the gain of the transistor (Q1). the higher the gain, the smaller



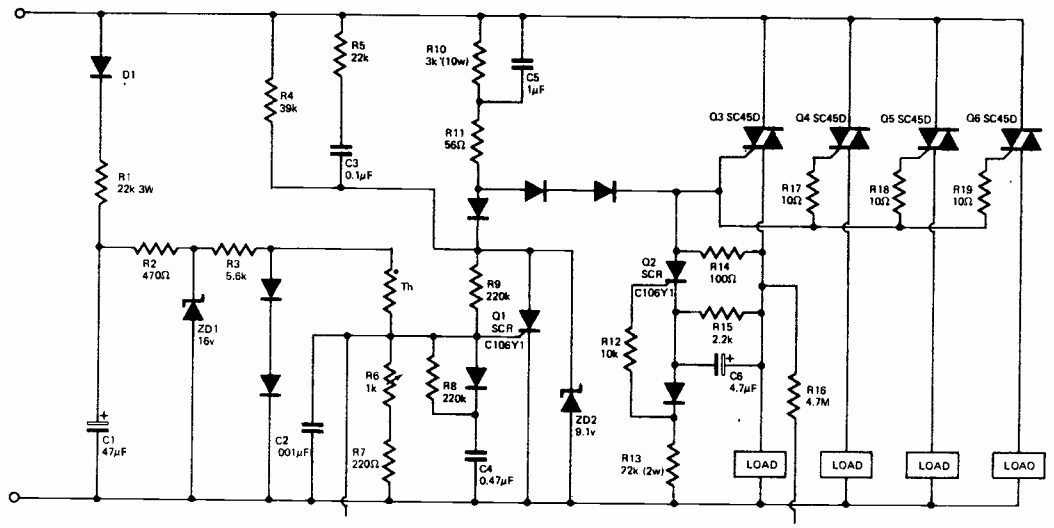


Fig. 2. (top) This circuit is a simplified version of that shown in Fig. 1. Thermistor resistance should be approximately 2k at sensing temperature.

Fig. 3. (centre) Slave circuit may be driven from either of the circuits shown as Fig. 1. and Fig. 2. Note – additional components are shown inside dotted lines.

Fig. 4. (right) This circuit may be used for either on/off or proportional operation.

the temperature differential If the smallest possible differential is required, than a BC108B or BC108C should be used for Q1. (It is not always realized that the BC108 transistor is manufactured in three different types — labelled BC108A, BC108B and BC108C in order of ascending gain).

SLAVE-DRIVE CIRCUITRY

Figure 3 shows the slave-drive circuit that may be used with Figs. 1 and 2. For clarity, the output stage of Figs. 1 and 2 has been shown — and the additional circuitry required for slave driving is that shown within the dotted lines.

In operation, as soon as Triac 1 conducts on the positive half-cycle of line voltage, gate currents are provided for the additional Triacs via parallel diodes D4 and D5, resistor R4 and Zener diode ZD1. The purpose of ZD1 is to act as a buffer between the master Triac (1) and the slaved Triacs.

Resistor R4 must be selected to suit the individual application. Its value depends on the size and number of the extra heating loads and the operating temperatures of the Triac junctions. For three slaved Triacs the value shown (220 ohms) will be about right, however this may need to be increased to 470 or 560 ohms if the loads or number of Triacs are increased. If this resistor is increased in value beyond 600 ohms or so, RFI may be become a problem. Capacitor C1 (shown as C2 in Figs 1 and 2) should be selected to provide optimum temperature differential combined with low RFI.

ON-OFF OR PROPORTIONAL OPERATION

The circuit shown in Fig. 4 is unusual in that it may readily be changed from 'on-off' to proportional operation — both modes nevertheless utilizing zero-voltage switching.

It is slightly less accurate than the circuits shown in Figs. 1 and 2 but nevertheless can maintain temperatures to within better than 0.4%.

As shown, the circuit operates in the proportional mode, 'on-off' operation is effected by deleting components R8, R9, C4 and D4.

The total heating load controllable by this circuit — using the components specified — is 9.6 kW. Naturally if smaller loads are used, then any or all of the slaved Triac stages (Q4, Q5 and Q6) may be omitted.

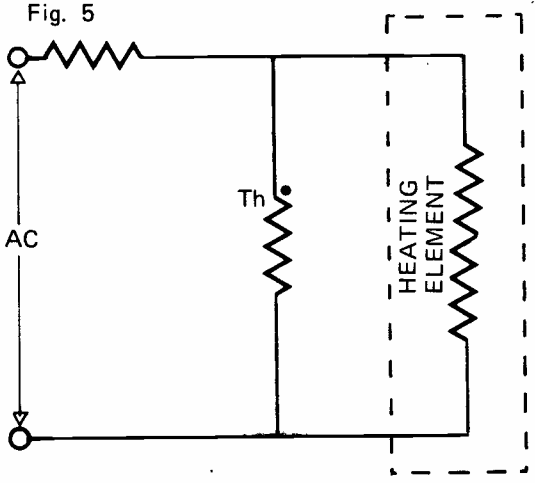
INTEGRATED CIRCUITS

The circuits described in this month's article have slightly complex control circuitry. They are capable of excellent performance and use components that are readily available.

Recently however, zero voltage switching integrated circuits have become commercially available and these in effect may be used to replace practically the entire control circuitry of the circuits shown in Figs 1 and 2. Circuits using this type of IC will be described in the next part of this continuing series — it is suggested that readers who are considering building high precision zero voltage switched controllers should wait until they have read this next article before commencing construction. ●

Fig. 5. Constant temperature control of small enclosure is achieved using this circuit.

Fig. 5



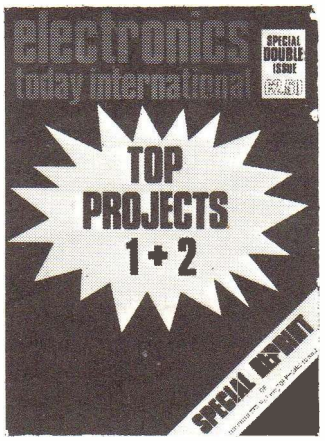
Several readers have asked us for a really simple circuit for maintaining a constant temperature inside a small enclosure.

The very simple circuit shown in Fig.5 is often used. Temperature differential is about 3°C.

In this circuit the thermistor is mounted outside the container but is connected in parallel with the heater. As ambient temperature rises, current through the thermistor will increase, hence decreasing current flow through the heating element.

The thermistor chosen must of course be large enough to dissipate the external current without excess heating.

SPECIALS



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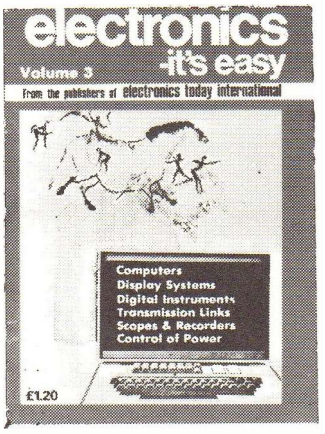

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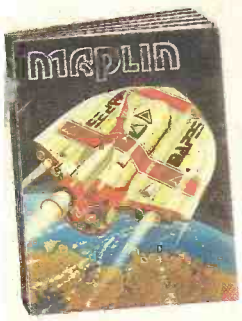

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