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THE ENGINEER: ON TAP OR ON TOP?

The Presidential Address of

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Presented after the Annual General Meeting of the Institution in London on 25th October 1973

It is customary on occasions such as this to look back over some great events in the history of our subject and to take a peep into the future. There is no shortage of compelling subject matter: the pioneering days of the wireless, the emergence of short waves, the evolution of television, the high drama of the role of radar during the war years, the arrival of microwave technology, the expansion of navigation aids to their present dominant role, the arrival of the computer, of semiconductors and of integrated circuits, of medical instrumentation and so on. I know of no other area of engineering which can point to so many changes of such magnitude in such a short time span—all within the professional lifetime of many of the members of this Institution. Nor can I think of one which is likely to see more rapid evolution in the next few decades than is likely to occur within the broad subject of electronics.

With such a surfeit of riches it should be an easy matter to select some particular theme and follow its history and to project somewhat into the future. I have decided, however, *not* to follow this tempting course but to take a more melancholy theme. It is this—where is the engineer going? Is his status in the community increasing or decreasing? Have the sustained endeavours of so many engineers in the various Professional Institutions—including the IERE—achieved the objective of elevating the engineer to the same standing in the public eyes as those in other professions?

I take this theme because I have become concerned at the signs I see of disenchantment with engineers and engineering, and, in some quarters, undisguised suspicion. The demand that the engineer should be 'on tap but never on top' seems to be stronger now than ever before—just at the very time when the engineering community is putting its house in order in terms of qualifications and professional code.

I would like therefore to take this very privileged opportunity to give my own analysis of the problems which beset the engineer in to-day's world and to give some suggestions for some of the measures necessary to correct them.

The Unhappy Past

Rich though the inheritance is from the past, there are a number of long shadows which hang over this nation's engineering which have led to the doubts I have described. In very recent times we have witnessed Rolls-Royce, surely one of the greatest names associated with engineering, brought to the humiliation of bankruptcy; a long chain of problems have assailed some of the newer nuclear power stations—with attendant time-delays and escalating costs; there have been some unhappy events in the world of civil engineering (roof collapses, bridge failures, etc.). Where investors have been persuaded to pledge their funds to some aspects of advanced technology they have found that the rewards were elusive. There were the over-publicized problems with the steam turbines of the *Queen Elizabeth II*.

Are there any lessons that can be drawn from some of these examples and are there ways which we as engineers can improve our performance? I believe there are!

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Appreciation of Cost

Possibly the most persistent defect has been the engineer's reluctance to take cost into consideration. This appears to be particularly true—but my view may be biased here—where the moneys come from the public purse. Every engineer is naturally dedicated to his particular design or invention and is reluctant to hear anything against it. Cost is essentially a negative score against any project and the engineer will naturally tend to diminish this in his own mind. In nearly every project with which I have had contact (a fair number by now) I have seen this unwillingness to face the full significance of costs and a realistic appraisal of what they may be. Let me immediately admit that I have been fully guilty of this type of blinkering in the days when I was fostering my own projects.

What form does this particular malaise take? I can identify the following in most of the projects that have run into some trouble. First there is the inability to appreciate the costs which *follow* the stage of invention or initial discovery. It is now widely accepted that if all of the research and initial development which leads to an invention costs one unit of money or effort, then it will take a further ten units to bring this to the market place.

This, however, is not the end of the story. If the product is accepted in the market place, there usually follows a third phase of rapid expansion to meet the demands. Failure to respond to this opportunity will only mean that a market has been created which an alert competitor will be able to occupy. This third (exploitation) phase may cost anything up to a hundred-fold more than the initial R and D investment. It will include expanded or modernized manufacturing plant, stockpiling of spares, creation of agencies, provision of leasing finance, extended credit, etc., etc.

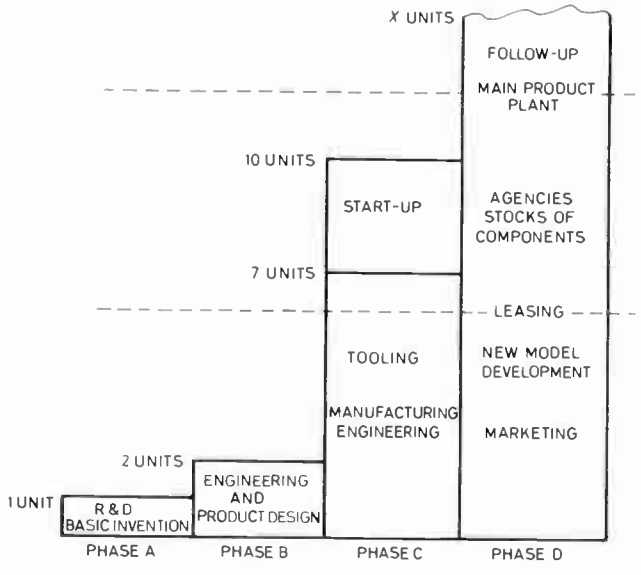

Fig. 1. Phases in the exploitation of an invention. (Source: 'Technological Innovation. Its Environment and Management'. US Department of Commerce, Washington DC, 1967.)

Figure 1 shows these three phases schematically. Let us suppose that our resources, either nationally or within a company, are limited as shown by the upper broken line. This would mean that the product could be taken right through to the market place but there would be insufficient resources to gain the full benefit. There are many cases of this.

If the resources available are even less, as indicated by the lower broken line, there will not even be enough to bring the product to the market place, let alone exploit its success. It is all too easy therefore to commit money to the initial R and D stage, only to find a multitude of projects clamouring for the limited funds available for the second and third stages. This leads inevitably to the agony stories about the brilliant inventions which the country or the company fails to exploit and the leadership which has been lost. It is necessary even at the early R and D stage to look forward to see whether the resources are going to be available to make exploitation possible. With very large projects, this will probably involve seeking international collaboration on a considerable scale, even though this means the loss of some sovereignty and a general move in this direction can now be seen emerging within the countries of the EEC.

Cost Escalation

The second major source of trouble is the inability of the engineer either to predict or to control his costs. A very few engineering projects stay within the cost forecasts, all too many greatly exceed them. The causes for this are numerous but most significant are:

Underestimation of the technical difficulties

Deliberate underestimating

Investment appraisal

Ignoring marketing.

Underestimation of the Technical Difficulties

All too often the engineer underestimates the difficulties which will arise as the scale of the project is expanded out of the laboratory or conceptual phase. Manufactured models turn out to perform differently from those carefully constructed in the laboratory, the scatter of performance is greater than was envisaged, the behaviour of components proves to be fickle, the yield of the production process is low or the product is inferior. This kind of erroneous technical forecasting is particularly noticeable where a great number of different disciplines have to be brought into play. The original inventor overlooks the extreme demands he may be making on the allied technologies which are frequently outside his knowledge and experience. All too often he dismisses them as 'mere engineering detail'.

To illustrate my general point about cost escalation I turn to one of the most publicized and best documented cases of cost escalation, the *Concorde*. In doing so, I must emphasize that this is *not* because *Concorde* is a special case, but rather because it has the characteristics of so many projects in advanced technologies. Here I must introduce a method which has been used within the DTI (it came initially from the former Ministry of

Aviation) to examine the cost escalation performance of projects. If the ratio 'current estimate of remaining cost' divided by 'initial estimate' is plotted against 'expenditure to date of estimate' divided by 'initial estimate' we get a form of presentation which very dramatically shows the way that the costs are moving. The effects of inflation must of course be removed and so the chart is presented at constant prices. In the ideal project, the locus of the two ratios should be a sloping line at 45° joining unity on the X scale to unity on the Y scale. Figure 2(a) shows what has happened in practice with *Concorde*. As the project moves forward, the estimates are constantly revised and the locus zig-zags up the chart rather than moves towards the Y axis. I have seen all too many examples of this 'walking up the page' type of phenomenon in a wide diversity of topics. If once a project starts to show this characteristic it is time to examine its future with a critical eye. This may well call for courageous decisions, which are certain to be unpopular in some quarters.

Figures 2(b) and (c) show two examples where the estimating has been fairly precise and in one case (the steam generating heavy water reactor) the final costs turned out to be below the initial estimate. It should also be noted that the revised estimates as time progressed produced a movement of the locus in both positive and negative directions.

There are now growing specific techniques of project appraisal and management which can markedly reduce these uncertainties even though they can never completely eliminate them. These methods need to be disseminated more widely.

Deliberate Underestimating

There are cases where the engineers involved are well aware of the uncertainties and the likelihood of cost escalation. In such a case the engineers should prudently make provision for a contingency margin to cover the expected increase. Alas, I have known engineers to argue that if their initial estimates were to include substantial (but realistic) contingencies the project would not be approved to begin with. There is an inverted logic in such a procedure. If a project is 'sold' to the customer on the basis of a probable underestimate of cost, it must be expected that the customer will be highly displeased as the true costs emerge and may be driven to cancel the project. The customer (particularly where this is Government) is also liable to be far more circumspect in examining future projects and is likely to add in contingencies of its own as an insurance. I see no justification whatsoever for this method of deliberate underbidding.

Investment Appraisal

Even where good cost estimates are achieved, it is surprising how many engineers fail to appreciate the basis on which investments are made—either in private industry or by Government. The whole purpose for making the investment is to achieve a commensurate benefit. In the majority of cases this benefit is quantifiable as *profit* and this profit must bear comparison

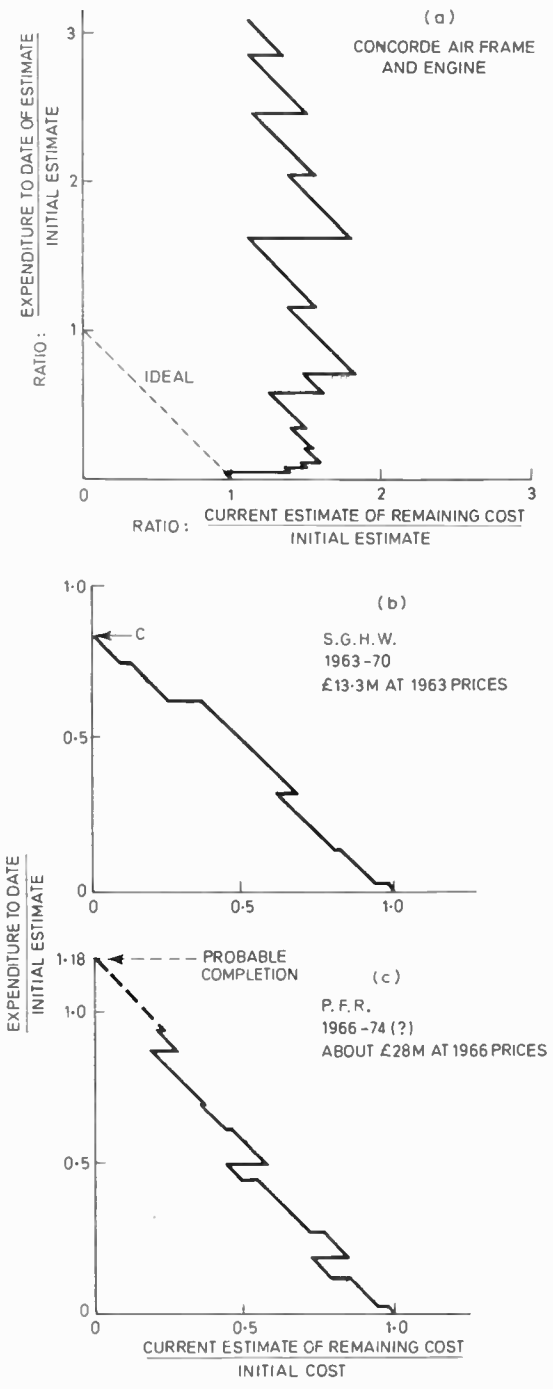

Fig. 2. Progressive costs of major capital projects. (At constant prices.)

(a) Concorde airframe and engines.

(b) Steam generating heavy water reactor.

(c) Pressurized fast reactor.

with the profits which can be made by alternative uses of the same money and resources. There are well-established methods for appraising these potential profits, the best known being that of predicted 'discounted cash flow'. Every engineer should be familiar with this method and use it in his own project analysis. Not only should an engineer be familiar with e.m.f., with s.i.c. and p.p.i., he must also be fluent in d.c.f.

There are also methods for evaluating the risks involved; in general the investor expects a higher potential return (or greater insurance) where higher risks obtain. The engineer should at least be aware of these methods and the ways that those responsible for funds have to consider the ways they are deployed.

Marketing

Let me immediately draw a distinction between marketing and 'selling'. Important though the latter most certainly is, it is only a component of the total activity known as marketing. This wider title involves all of those activities which lead to the right product being offered to the customer in the right way (price, delivery, service, etc.). It can mean a detailed technical appraisal of his needs, the study of alternative methods for achieving them, the seeking for an optimum package to satisfy him, and a close association with him after the sale. These elements are particularly relevant where the product is complex and the capital investment high (air traffic control, urban transport systems, power stations, telecommunications networks, broadcast systems and studios, navaids, computers, process control, etc.). Brilliant work in the R and D laboratory can be made valueless if this element of marketing is neglected. Contrary to being the haven for 'failed design engineers' technological marketing demands the very best qualities an engineer can possess—imagination, analysis and compromise. Yet how many of our engineering faculties give proper attention to this vital activity and indeed, how much attention do we give to it in our professional engineering institutions?

An important element in marketing is market research. In the field of advanced technology, market research is a very challenging task, calling for exceptional skills not only in the technology itself but also in the handling of statistics and probability theory. Not only does the changing pattern of the market place have to be forecast, but also the impact of alternative, rapidly moving, technologies have to be assessed. This is particularly difficult where long lead times are involved, such as usually occurs in the whole process of research, development, engineering and production of complex equipment such as air traffic control, broadcast systems, telecommunications networks or computers. The high quality effort which lies in the R and D and engineering departments must be matched with people of comparable quality and dedication in the market research section of the organization. Yet few of our academic institutions trouble to select and train talented engineers for this task and all too often the people who do this work have arrived through some 'accident' in their career.

Time Factor

Another particularly troublesome item is time factor. Because engineers are prone to underestimate the technical difficulties they consequently underestimate the time factors involved. Quite apart from the inevitable cost increase associated with time delay, there is the more serious danger of losing the 'opportunity window'. All technologies tend to increase in volume and complexity along an exponential curve which I show schematically in Fig. 3. When a company decides to market a particular product it inevitably inhibits its ability to continue to follow the further advancement of the technology. It will have to freeze designs, set up manufacturing facilities, train personnel, order components, etc. As time rolls on, the technology incorporated in the product or process will become outmoded. At some later date a competitor will introduce a new product, based on the advantages of a more advanced technology. This, in all probability, will then mean that the life of the original product will be curtailed and within a few years it will become obsolescent. The more powerful the technological push, the shorter will be the 'opportunity window' within which the product can enjoy an advantage in the market place. Once a product design has been frozen, any delay introduced by development, engineering, production or marketing will erode the profits which can be made and thus diminish the funds available for the next generation of product research, engineering, etc.

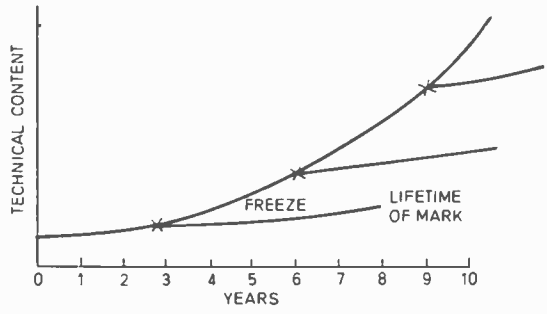

Fig. 3. Technological advance and exploitation showing the opportunity window.

Brilliant initial design will be of little value if the subsequent processes take too long to complete and the 'opportunity window' is missed. At this phase, time is a direct substitute for technological advance and it is frequently necessary to curb further technological ambitions in order to achieve the time-scale. It is here that the creative inventor can frequently become his own enemy, seeking to improve and refine his brainchild at peril of missing the market opportunity. One of the qualities needed in a powerful marketing and production system is the authority (and courage) to cut, if necessarily ruthlessly, the continuing dalliance with R and D and engineering.

I would like to illustrate the effect of time-scale by turning to another advanced technology industry—that of electrical generation. First, the chart (Fig. 4) shows the time slip of the Dungeness 'B' Nuclear Power Station. The method of presentation here is a variant on the one I used earlier. Here the ratio 'current estimate of total cost' divided by 'initial estimate' is compared to 'current estimate of remaining time to completion' divided by 'initial estimate of construction time'. In the ideal case the locus should be a horizontal straight line passing through the origin. Any movement upwards is a measure of shortfall in performance and the chart speaks for itself.

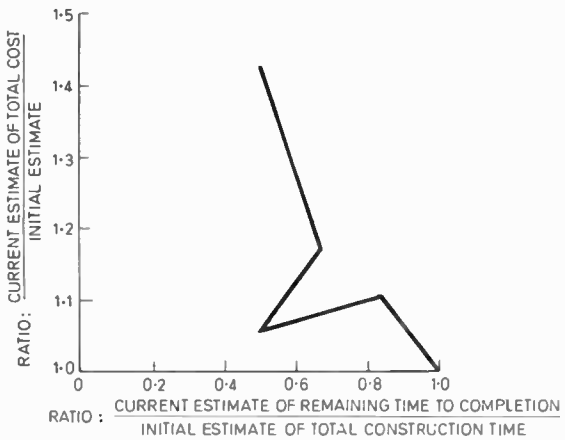

Fig. 4. Cost and time slip chart for Dungeness B Nuclear Power Station.

As a second example, Table 1 relates to the commissioning of generating units in the electrical power programme. Again the figures speak for themselves, but I emphasize that these delays mean very high costs, not only in terms of unproductive capital investment but also because older and less efficient stations have to be maintained in service for a much longer time.

Technological 'Sex Appeal'

In far too many cases engineers (and sometimes the public at large) are impressed by that element of their subject which is exciting and new at the cost of attention to those matters which may be dull but vital to success. We tend to regard 'originality' particularly in terms of new concepts as being the only worthy form of engineering and we neglect factors such as detail design, quality, reliability and maintenance. Here in the UK we are prone to remind ourselves of the original inventions and discoveries of the world which have been produced by our own engineers throughout history, yet at the same time we find our products surrendering to competition because of such defects as inferior quality, imperfections on delivery, unreliability and delays. On the other extreme we see Japan, whose contribution to the world's store of fundamental knowledge or engineering concepts has been very modest, achieving major successes in advanced technological products and processes. This has been achieved by great attention to the very things we tend to overlook—detail design, quality control, technological marketing and a willingness to adapt to the customers' needs.

Of particular danger here are the 'fashions' which tend to arise all over the world for a particular field or technique. How often do we hear the cry that 'we must do so and so because everyone else is doing it' without critically examining whether it is worth doing anyway or whether it is relevant to the particular company or country. I believe that as a country we are now less prone to fall into this trap than we were in earlier days, and we have learnt to view things more soberly and dispassionately. This calls for an interplay—which may sometimes lead to collision—between the enthusiasts and those who are uncommitted or even critical. It was this type of questioning challenge that Lord Rothschild was seeking when he proposed the customer/contractor relationship in Government funded research. This is now reflected in the Research Requirements Boards which have been established in the various Government Departments.

Multi-disciplines

It is a feature of most of to-day's technologies—whether it involves space flight or sewerage processing—that they call for a complex interplay between the various disciplines. It is not sufficient, therefore, for to-day's engineer to develop a mastery of one field of engineering (mechanical, civil, electrical, etc.), he must have some fluency in several fields which may be outside his own. For example, the mechanical engineer should certainly have some knowledge of electronics because he will be confronted more and more with numerical control, electronic sensors, electronic diagnostics, etc., in the practice of his subject. In his turn the electronic engineer will need to have a significant knowledge of advanced materials, of mechanical engineering and of computer-aided design. The engineer must be encouraged to accept new and unfamiliar disciplines and to learn to master these as they arise. Possibly those of us that grew up in the world of electronics are more willing than most to 'learn and re-learn' because our subject has changed so dramatically in the space of a few decades. This suggests that we should take the lead in encouraging other branches of engineering to widen their field and to espouse new forms of engineering.

The Status of the Engineer and the Role of the Engineering Institutions

Whilst the work which has been done and is being done to elevate and to formalize the qualifications which have to be achieved for registration as chartered engineers is vitally important, this in my view is not enough. It is only when the engineer himself demonstrates in all

Table 1

Analysis of delays in the commissioning of generating units.

	Delays in months								
	0–6	7–12	13–18	19–24	25–30	31–36	37–42	43–48	49–54
Number of units	12	14	11	7	6	7	2	2	1
Number of stations concerned	6	8	9	5	5	4	2	2	1

of the things he does a full awareness of those additional matters that I have mentioned will his status become automatically accepted. At the end of the day it is by performance that the engineer, like anyone else, will be evaluated. It is his skill in handling all of the factors which concern him that will win respect and here cost, quality, reliability, time delays, marketing and maintenance must not be ignored. We must regard those engineers who concern themselves wholly with one or other of these topics to be just as important as those who are in the laboratories, the experimental workshops or in design offices.

What role should an institution play? It is my view that one of its crucial roles is to foster the type and quality of engineer which the community needs to serve it. By its process of selection for membership, by its activities in lectures, conferences, seminars, and through its publications, it should not only keep its membership abreast of developments but steer them towards a proper balance between the exotic and the necessary. A ceaseless diet of the more advanced elements of the subject can lead the engineer to overlook those which are vital to success. We must avoid creating the impression that so many have, that it is only the 'original' or 'fundamental' engineer who is 'respectable'. I believe the IERE does better than most institutions in this regard and our activities in fostering the good health of technicians is very worthy but how often have even we discussed or highlighted the importance of cost, of marketing, of quality and of avoiding time delays? How many of our published papers even acknowledge that these mundane subjects are crucial, how many of our meetings are devoted to such topics? Should we not get into the habit of saying 'How much will it cost?' 'How long will it take?' 'Where is the market place? And how long will it exist?'

In what has preceded I have been critical and possibly destructive. Now let me be constructive. I suggest that we as an institution and as a member of the CEI should do the following things.

(1) So frame and implement our membership rules that those engineers who concern themselves with production, quality control, marketing and maintenance are just as welcome and just as privileged as those who engage in R and D, design engineering and other 'creative' activities.

(2) Make a place deliberately in our calendar of meetings, symposia and conferences for these essential but less glamorous topics to be discussed.

(3) Encourage more authors of papers to discuss such matters as cost, time-scale, and probable markets when they submit their manuscripts.

(4) Publish occasionally, in our journal, papers specifically concerned with marketing, market research, quality control and maintenance.

(5) Once a year to invite a speaker from a background different from our own but closely involved with it, to give a different viewpoint. I have in mind such people as accountants, financiers, public authority officials, exporters, etc., who can open our eyes to matters that concern them as the people who have to deal with us.

(6) Campaign for industry to make better use of its engineers and to play its part in encouraging the engineer to play a fuller part in the management decisions of the company.

(7) Exploit the existence of the CEI and our membership of it to promote a more multi-disciplined approach.

(8) Urge the academic and teaching world to place due emphasis on the less glamorous but vital aspects of engineering.

I return now to my title for this address and repeat the question 'is the engineer to be on tap or on top?' The answer to this can only come from the engineer himself, through his performance and his ability to meet the needs of his organization, his company or his country. It is by consistent success in meeting these needs within the resources available and to the time targets that have been set that he wins respect. The ability to do this is, in the long term, far more important than the constant striving after dazzling new concepts or products. This is an unattractive conclusion, but one which we must face.

I have no doubt that the way to the top is open to the engineer—but he (and we) must recognize the route that has to be followed.

Address No. 47

Guest Editorial

Tomorrow's Logic

Logical design as an area of study has been described as a triple point interface between physics, mathematics and electronics. The display techniques associated with digital circuitry depend on a variety of physical phenomena from incandescent filaments to light-emitting diodes and liquid crystals; the mathematics content owes much to the work of George Boole who published his method for solving problems in logic in 1854; and the electronics ingredient is evidenced by the wide variety of electronic systems of logical circuits.

One should not conclude that the ideas of two-state systems on which much of logic design depends is of recent date, or even that it dates from 1854. The history of logical systems can be traced back to Jevons' Logical Piano 1869, Babbage's Difference Engine 1823, and the Jacquard Loom of 1800 which used what must be supposed to be the first punched cards.

Readers may have heard that whilst Charles Babbage designed his machine to calculate, process statistics and even modify its actions as a result of the answers it was producing, he never actually got down to building it! There are a lot of Babbages around to-day—theorists who do an excellent job with brilliant new ideas but who never seem to meet the challenge of, 'Build it, prove it with hardware, and what's more, do it now'. Mathematicians, of course, feel that this is no part of their terms of reference. Hence they do not need to go through this exercise. But this is the commercial situation where industry must exploit ideas or bow to the competition. Although logic design is a fascinating academic exercise, its *raison d'être* lies, in the widest sense, in automation engineering.

Logic design has for so long been associated with computing that it might be argued that it is over-influenced by the technological demands of that industry. The electronic circuits in use to-day are those which are desirable commercially, and this has sometimes limited the thinking of designers who feel that they must of necessity work with the circuits which are available, at prices within their budget, especially where they are attempting to realize systems of substantial size. Others, not so inhibited, have had genuine practical difficulties in implementing their circuit designs, the initial cost of setting up a new silicon circuit layout being not the least of these. Thus whilst integrated electronics has materially contributed to reducing the price of digital circuitry, it has severely limited original circuit design to the point where practical large-scale circuit innovation at basic resistor-transistor component level is very much a minority exercise. The test is often, perhaps wrongly, applied to new developments in logic design that any new idea is suspect unless it is quickly implemented in m.s.i. or l.s.i. form.

The design of electronic systems has for a very long time been based on the manipulation of components. For the logic designer the basic components have been the combinational and sequential gate functions such as NAND and NOR gates and JK flip-flops. This has been so since the early 1950s when other engineers were thinking in terms of resistors and capacitors. Now with improved silicon technology these are being replaced by sub-systems as fundamental building blocks. Here again the digital electronics engineer is often still ahead of others in implementing new technology; for example, domestic radio receivers with integrated i.f. and audio amplifier circuits are only now coming into common use.

The introduction of sub-systems as logical components in digital equipment is a step for which our mathematical armament is inadequate. Can one, how does one produce a super-powerful system using say, several thousand central processor chips interconnected in some new way? What worthwhile function can be generated by doing so? How can we deduce these results mathematically? Questions like these indicate the limitations of our design capability. Whether this is all a mere pipe dream can only be resolved when we are able to manipulate complex functions such as central processors in some way analogous to that in which Boolean algebra enables us to handle the interconnexion of NAND gates. The situation with sequential functions is, if anything, worse! Now that we have component reliability which is so high, large systems are to-day viable which would previously have been dismissed out-of-hand as unrealistic. Mean time between failures is now measured in (at least) thousands of hours where previously it would have been expressed in minutes. Our design techniques are not yet geared to this situation.

This issue of *The Radio and Electronic Engineer* is not just an excuse to babble of Babbage or to bore with Boole, but is intended to present some cross-section of interest in logic design and some indication of where the frontiers of knowledge now lie, so that the specialist and generalist reader alike can weigh up what has been done and in what direction we should now be going. The limitations of logic design have been taken up by one author whilst others review topics of current interest or describe recent work which they have carried out. This is chiefly the concern of a few university departments. Whilst a much larger number are, of course, concerned with digital applications and there is a great deal of that kind of design work being done in British industry, it is perhaps significant that in UK at least, innovative research in logic design is slow to gain the wide acceptance that tomorrow's leadership in an increasingly digital electronics industry will demand.

K. J. DEAN

Contributors to this issue*

Professor Douglas W. Lewin (Member 1960, Graduate 1957) is Professor of Electronics at Brunel University. Prior to his present appointment in January 1972 he was a Senior Lecturer in the Department of Electronics at the University of Southampton. He has served as a member of the Southern Section Committee and has been a member of the Computer Group Committee since 1970 and of the Papers Committee since 1971; he has represented the Institution on the Organizing Committees for several joint Conferences. Last October Professor Lewin was elected a member of the Council. He has contributed papers to the *Journal* and is author of several books.

Mr. W. Swan (Member 1948) served as a Technical Officer in the Signals Branch of the Royal Air Force including four years at Air Ministry working on surface to air guided weapons systems, and he retired from the Service in 1961. He has attended university in London, Manitoba, and Calgary, obtaining a B.Sc. in mathematics and physics, and an M.Sc. in computing science. He held an instructor's post in the Department of Electronics at Southern Alberta Institute of Technology from 1965 to 1971, and he now lectures in the Department of Computing Science at the University of Calgary.

Mr. John Deverell received an honours B.Sc. degree in electrical engineering from Queen Mary College, University of London, in 1961. From 1961 to 1966 he was employed in Engineering Division of AERE, Harwell, first as a Graduate Apprentice, then as a Technical Assistant, and finally as an Engineer III. He was a Lecturer I at the School of Electronic Engineering, REME, Arborfield from 1966 to 1968, when he joined Twickenham College of Technology as a Lecturer II. He became a Senior Lecturer in 1971 and lectures in electronics on degree level courses in the Department of Engineering Technology. In addition to his research on cellular logic, he manages the College's Central Research Unit.

Dr. K. J. Dean (Fellow 1965, Member 1952), who has acted as Guest Editor for this issue on Logic Design, is Principal of South East London Technical College. A member of the Papers Committee, from 1964 until December 1973, he has been Chairman of the Computer Group Committee since 1971. A fuller note on his career was published in January 1973.

Dr. Igor Aleksander obtained his first degree in electrical engineering at the University of the Witwatersrand, and his doctorate at the University of London. In 1959 he joined STC at Footscray where he worked on the application of transistors and tunnel diodes to computer circuitry. Since 1962 he has been lecturing at the West Ham College of Technology, Queen Mary College (London University), and he is at present Director of the Computers and Cybernetics Research Laboratory at the University of Kent at Canterbury.

During this time Dr. Aleksander has pursued research on the electronics of artificial intelligence systems, switching theory, automata theory and control systems. He is the author of forty papers and two books on these subjects. In 1962 he was joint recipient of the IERE Charles Babbage Award, for a paper on the switching applications of tunnel diodes.

Mr. T. J. Stonham graduated with honours in electronics at the University of Kent where he also obtained his M.Sc. degree. During the last two years he has been sponsored by the Unilever Company on a research studentship. He is at present a Research Fellow at the University of Kent where he is carrying out research into the automatic recognition of mass spectral data.

Dr. Manissa Jill Dobrée Wilson was educated in France and graduated with honours in electronics at the University of Kent from which she also obtained her Ph.D. At present, she is a Science Research Council Research Fellow at the University of Kent where she is investigating the trainability of sequential adaptive logic circuits for artificially intelligent systems.

* See also pages 20, 38 and 49.

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Outstanding problems in logic design

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SUMMARY

Current problems in logic design, in particular those concerned with the design and implementation of digital systems using complex l.s.i. circuits, are discussed. It is argued that established switching theoretic methods, such as minimization, state-assignment etc., are no longer relevant, and that existing theory is inadequate for design at the sub-system level. The difficulties associated with the implementation of r.o.m. and multiplexer circuits are reviewed in detail and finally a summary is given of present day research in systems specification and design.

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1 Introduction

It has long been accepted practice to implement logic circuits by using basic gates, such as NAND/NOR units, and bistable elements. This has resulted in a design philosophy emphasizing the minimal number of gates and bistables required by the circuit. This technique, though of course still fundamentally sound, is nevertheless rapidly becoming obsolete due to the advances in i.c. technology. With modern l.s.i. and complex m.o.s. circuits the cost of saving a single gate, transistor or diode is almost insignificant. In some cases, however, a minimal solution is still relevant. For example, in l.s.i. circuit manufacture, circuit area and the interconnexion between gates and modules are important parameters. The number of interconnexions dictates to a large extent the size of the final module, while decreasing circuit area enhances the production yield. In both cases logic circuit minimization can result in worthwhile savings. Medium scale integrated circuits (m.s.i.) providing complex logic functions such as counters, shift registers, decoders, multiplexers, read-only memory (r.o.m.) etc., are now available very cheaply in standard dual-in-line packages. These devices enable many standard logic operations, such as binary decoding and encoding to be implemented directly using a single module. The availability of complex integrated circuit modules is inevitably beginning to influence the techniques of logic system design. In many cases it is better practice to utilize standard m.s.i. packages, even if this introduces redundant gates, then design optimized logic to be implemented at the gate level. Thus, the criteria for the economical implementation of logic systems has been raised to a higher sub-system level, and must now take into account the number of logic packages, and the cost of printed circuit boards and back wiring.

Another, and perhaps more important change, is that designers are using these complex elements as sub-system components and modifying their design by defining a data structure consisting of standard m.s.i. registers, arithmetic and logic units, highway gates, etc., with the overall operation being governed by a programmable r.o.m. control unit. Logic design is thus being elevated to a higher, sub-system, level where complex elements, rather than basic gates, are being interconnected to give the required system function. Moreover, in general we have a situation where the component manufacturers are providing modules (based on conventional logic functions) which are being imposed on the designers, rather than the system designers dictating what modules should be available. Consequently designers are being forced of necessity to work at an intuitive level with little or no theoretical basis. The reason for this is obvious—theory has not kept pace with practice. What is needed is a new theory of switching circuits at the sub-system level, rather than as we have it at present, at the logic gate level.

Another major problem is the inherent complexity of logical systems. The basic engineering design of digital systems has changed very little from the original techniques used for first-generation computers, though of course they have been considerably refined as a result of technological progress in components and devices.

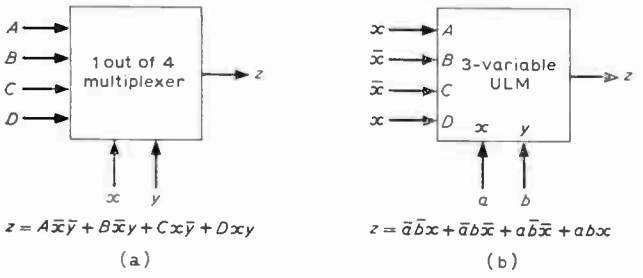

Fig. 1. Implementation using multiplexers.

Consequently we are rapidly reaching a situation where, unless something is done, the sheer intellectual effort required to develop, evaluate and test digital systems could establish a barrier to further progress. A partial solution to this problem has been the application of computers to the production phases of digital system designs.

Thus, computers have proved extremely effective in automating the layout and routing of printed circuit cards, back-plane wiring, testing and maintenance schedules etc.[1,2] However, the real problems are encountered in the initial design stages, that is at the conceptual level and the subsequent evaluation and implementation. The real requirement is for an interactive computer-assisted design scheme which allows the designer to specify and evaluate a system proposal and then proceed to implement the design using either hardware (or software) processes.[3] The output from such a system would be a logic diagram or flow-chart, or ideally if included in a comprehensive hardware c.a.d. scheme, placement and wiring diagrams. A design system of this sophistication requires a methodology for specifying the system both at the behavioural (information flow) and functional (data flow) levels. Moreover, in order to fully assist the designer in synthesizing and evaluating complex logical systems, it is essential to have a formalism in which the total system, both hardware and software, can be represented. Unfortunately a notational system which adequately fulfils this function does not exist at the present time.

2 Logic Design with Complex Integrated Circuits

The realization of logic circuits using m.s.i. circuits, such as multiplexers and r.o.m.s have had a marked effect on the traditional methods of implementation. In many cases it is no longer necessary to apply conventional minimization techniques and the designer can work with canonical expressions obtained directly from the truth-table. In particular the use of r.o.m. modules allows both combinational and sequential circuits to be economically implemented without recourse to sophisticated design techniques.

2.1 *Multiplexer Modules*

Multiplexer circuits are capable of generating Boolean functions and consequently may be used to implement combinational circuits.[4] For example, the 1-out-of-4 multiplexer circuit, shown in Fig. 1(a), can be considered as a 3-variable universal logic module (u.l.m.).[5] This is possible because in the general case any combination of the four possible variable values 0, 1, x and $\bar{x}$ can be connected directly to the multiplexed input lines which, with the control inputs (ab), gives $4^4 = 256$ different input combinations. Since this figure corresponds exactly to the number of different Boolean functions of 3 variables (that is 2^{2^n} where n is the number of variables) it follows that multiplexer circuit can be used to generate any 'random' switching function. For instance in Fig. 1(b) the expression

$$z = \bar{a}\bar{b}x + \bar{a}b\bar{x} + a\bar{b}\bar{x} + abx$$

has been implemented directly, where a and b are the control inputs and x the multiplexed variable.

The action of the multiplexer circuit may be expressed more formally by noting that any logic function $f(x_1, x_2 \ldots x_n)$ of n variables, where $n \geqslant 3$, can be expanded to the form:

$$f(x_1, x_2, \ldots x_n) = \bar{x}_1\,\bar{x}_2\,f(0, 0, x_3, \ldots x_n) + \bar{x}_1\,x_2\,f(0, 1, x_3, \ldots x_n) + x_1\,\bar{x}_2 f(1, 0, x_3, \ldots x_n) + x_1\,x_2\,f(1, 1, x_3, \ldots x_n). \quad (1)$$

For example, in the case of a function of 3 variables, i.e. $f(x, y, z)$, we have, by expanding with respect to the variables x and y, the following equation:

$$f(x, y, z) = \bar{x}\bar{y}\,f(0, 0, z) + \bar{x}y\,f(0, 1, z) + x\bar{y}\,f(1, 0, z) + xy\,f(1, 1, z)$$

where the residual functions, $f(0, 0, z)$, $f(0, 1, z)$, $f(1, 0, z)$ and $f(1, 1, z)$ are functions of z only, and each of these functions assumes one of the four values 0, 1, z or $\bar{z}$ Note that this equation describes the 1-of-4 data-selector described above, where x and y are the control lines. Moreover, it follows that Boolean functions may also be expanded with respect to any number of variables, for example expanding with respect to three variables results in the 1-of-16 data selector which enables all Boolean functions of 5 variables to be generated.

Though it will be obvious from the above that u.l.m.s handling any number of variables can be produced, the complexity of the circuits increases rapidly and from economical and maintenance considerations it is better to implement logic functions using a number of identical small variable u.l.m.s. This is possible by connecting multiplexers in arrays of two or more levels, corresponding to repeated expansion of the residue functions in equation (1) above until they are functions of the variable x_n only.

In multi-level implementation the selection of suitable control inputs at the first level is very important, since this can effect the number of multiplexers required in the second and subsequent levels. If possible the choice must be made so as to optimize the number of 0, 1 and common inputs (that is inputs which can be shared at the data inputs of the multiplexer). An alternative approach is to select variables for higher order levels that are either identical or the inverse of one another; this latter procedure is only applicable when the multiplexer has both true and complemented outputs. In all cases the objective is to reduce the number of multiplexers required in the higher order levels. The problem is further complicated

since there is no reason why the control inputs at higher order levels should all be the same (though in practice they often are); the use of individual control inputs can often lead to a reduction in the number of modules required in the preceding levels.

Though the cost of multiplexer units is some five times higher at the present time than basic gate packages, there is nevertheless considerable advantage to be gained from this method of implementation. The obvious gain if a single 1-of-16 multiplexer is used is the reduced cost of wiring and layout of printed circuit boards. Other considerations include the reduced number of spare packages that will be required and the ease of testing and maintenance. An obvious disadvantage in the case of cascaded modules is the increased propagation time through the circuits.

Multiplexer units are, on average, some 2 or 3 times slower than corresponding TTL NAND/NOR units; this difference balances itself out with single package multiplexer implementation since most practical logic circuits involve at least two gate levels. Unfortunately, there is as yet no formal design theory which can be directly applied to the implementation and minimization of cascaded multi-level multiplexer circuits. Note also that we have only considered the realization of single-output functions, multiple output circuits present yet another problem.

2.2 *R.o.m. Circuits*

Using r.o.m.s the implementation of combinational and sequential circuits becomes a relatively trivial operation.[6,7] There is no need to employ any of the conventional minimization techniques or to search for an economical state assignment, the designer can work directly from a truth-table or assigned state-table.

For example, to implement a combinational circuit the switching variables would be used as the address inputs to the r.o.m. with the required output values being stored in the contents of the r.o.m. words. Thus, when a particular input combination is presented to the r.o.m. the contents of the addressed word (i.e. the output values) are read down and appear at the output of the memory. It will be obvious that the r.o.m. is ideal for realizing multiple-output circuits, when each bit in the r.o.m. word corresponds to a particular output value.

The choice of r.o.m. is determined by the number of variables and output functions required. For example, a n-variable circuit will require 2^n words of r.o.m., with a wordlength directly proportional to the number of required outputs. If the number of minterms for a given function of n variables is greater than 2^{n-1}, it is often more convenient to program the complement of the function (equivalent to using maxterms) and invert the output of the r.o.m. Note that 'don't-care' input conditions are immaterial when implementing logic circuits using r.o.m.s, since the devices are only available in standard-sized modules and hence it is not possible to economize on the number of words required.

For large variable problems direct implementation using a single r.o.m. soon becomes impracticable since every additional switching variable doubles the number of words required in the memory. This limitation may be overcome in the majority of cases by employing smaller r.o.m.s in cascaded or multilevel circuits. Since it is always possible to connect r.o.m.s together to produce a larger sized store, for example two 32×8-bit word modules can be connected together to give a 64×8-bit word store, the techniques of cascading are effectively those of minimization at the sub-system (i.e. r.o.m.) level.

Table 1

Cascaded r.o.m. networks

(a) ON terms listing

Decimal form	Variables *AB*	*CDEF*
5	00	0101
15	00	1111
20	01	0100
29	01	1101
41	10	1001
42	10	1010
45	10	1101
47	10	1111
53	11	0101
58	11	1010
61	11	1101
63	11	1111

(b) Shared terms and coding

Variables *CDEF*	Coded form $Z_1Z_2Z_3$
0100	001
0101	010
1001	011
1010	100
1101	101
1111	110
other terms	000

(c) Layout of first-level r.o.m.

Input Variables *AB*	$Z_1Z_2Z_3$	Outputs $T_1T_2T_3T_4$
00	010	1000
00	110	1000
01	001	1000
01	101	1000
10	011	1000
10	100	1000
10	101	1000
10	110	1000
11	010	1000
11	110	1000
11	101	1000
11	110	1000

As an example of multilevel implementation consider the 6-variable switching function:

$$T = \sum(5, 15, 20, 29, 41, 42, 45, 47, 53, 58, 61, 63)$$

In order to realize the circuit as a cascaded r.o.m. network the variables must first be partitioned and then recoded to achieve the necessary data-compression. This is usually possible since in general the ON terms of a switching function contain common variables or minterms. For example, in Table 1, the variables are partitioned into the sets (AB) and ($CDEF$). Now since ($CDEF$) contains only six unique 4-tuples, i.e. 0100, 0101, 1001, 1010, 1101 and 1111, it is possible to replace these with a 3-bit code. Note however that the OFF terms and 'don't-cares' must also be coded, usually as an all zeros code. The cascaded circuit takes the form shown in Fig. 2 in which the variables $CDEF$ go to ROM 1, which generates the coded outputs Z_1 Z_2 Z_3, and this output together with the primary input variables AB go to ROM 2 which generates the final output functions.

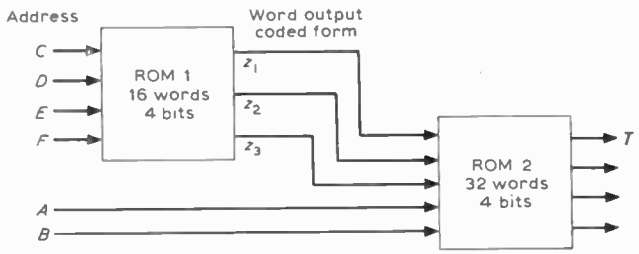

Fig. 2. Cascaded r.o.m. network.

Note that the circuit could have been implemented directly using four 16 × 4-bit words; using the cascaded method we have reduced the number of 16 word r.o.m.s to three.

The technique produces even greater savings when large variable functions are to be implemented. Unfortunately, no formal design algorithms exist for this technique and consequently the method is essentially heuristic in nature. Moreover, in a practical situation when multiple output circuits are required the problems encountered in heuristic design become severe. However, some work has been done by the semiconductor manufacturers, who have devised computer algorithms to determine the best partitioning and coding of the truth-table for the implementation of specialized r.o.m. networks.

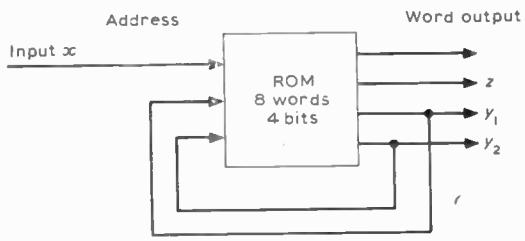

Fig. 3. Divide-by-two r.o.m. counter.

As we might suspect, r.o.m.s are also ideal devices for the realization of synchronous and asynchronous sequential circuits. Using r.o.m.s the initial conceptual design procedure remains unchanged, and the starting point for implementation is the assigned flow-table. Table 2 shows a typical assigned flow-table for a divide-by-two asynchronous counter stage; the transition table shows the required transitions from present to next states of the counter when the external input x is applied. The circuit is shown in Fig. 3, note that the $y_1 y_2$ outputs are fed directly back to the address input of the r.o.m. to give the required sequential, that is feedback, action. Note also that the circuit represents a Moore machine, the more general Mealy machine can easily be accommodated by allocating appropriate bits in the r.o.m. words to generate the output functions directly.

Table 2

R.o.m. implementation of binary counter stage

(a) Assigned flow-table

State variables	Input x		Output
$y_1 y_2$	0	1	Z
00	00	01	0
01	11	01	0
11	11	10	1
10	00	10	1

(b) Transition table

Address $x y_1 y_2$	Output word $y_1 y_2 z$
000	000
100	010
001	110
101	010
011	111
111	101
010	001
110	101

An implementation of this form is possible because the integrated circuit r.o.m. is constructed from active devices, which give the necessary gain round the feedback loop. The equivalent in the r.o.m. to an asynchronous stable-state condition is when the output word is used to address its own location—a form of dynamic loop. Thus, the r.o.m. circuit is directly analogous to the conventional NAND/NOR implementation of the excitation equations. However, in this case there is an added advantage in that there is no longer any need to examine and correct for static hazards. The occurrence of static hazards arises during the minimization procedures and since, when using r.o.m.s all the basic switching terms are effectively used, hazards of this type are eliminated.

Synchronous machines may be implemented using r.o.m.s in a similar manner, though in this case there is a timing problem to be considered. In some cases the

r.o.m. is provided with an enable or strobe line which can be used like a system clock, for instance, the outputs can be disabled until the transients on the input lines have died away. However, the required delay round the loop may be obtained by using external bistable devices (for example, m.s.i. D-type bistable latch units) to register (that is, delay) the outputs prior to returning them to the address inputs.

It is interesting to consider the effect that implementing sequential machines with r.o.m.s has on established logic design theory. It will be obvious that the need for minimization of the combinational circuitry (for instance, bistable input equations) no longer exists. For similar reasons minimal state-assignment procedures for synchronous machines are also irrelevant. However, state-reduction and row reduction (merging) procedures are still of moderate importance since these techniques can reduce the number of words required in the r.o.m. The size of the r.o.m. required to implement a sequential machine is determined by the fact that the sum of the number of bits used for the external input and state codes must be less than or equal to the address bits of the r.o.m. The wordlength of the r.o.m. is dictated by the total number of bits required for the state code and output functions.

Once again there is very little formal theory to assist the designer to implement sequential circuits using r.o.ms. This lack of theory could create real problems particularly since large systems must be cascaded to economize in r.o.m. storage. One theoretical concept which could prove useful in the design of r.o.m. systems is that concerned with the decomposition of large sequential machines into smaller machines, which can then be connected in serial-parallel configurations to give the same characteristics.[8] This work could be extended to r.o.m.s in order to reduce the amount of storage required for a given machine. Moreover the early work of Ashenhurst[9] could also be usefully re-evaluated in the context of cascaded r.o.m. implementation.

The economic advantage of r.o.m.s is not obviously apparent, for example, in the case of the sequential circuits discussed above the cost of the r.o.m.s would far exceed the cost of the logic packages required for a conventional design. However, if we consider not only the reduced cost of engineering a single package, but also the costs involved in design, testing, maintenance etc., there are considerable advantages. Nevertheless, at the present time one must consider carefully whether or not to use r.o.m.s (or for that matter m.s.i. in general). For small one-off systems logic packages are still the most economic method of realization, but for large quantity produced systems m.s.i. is far superior. One further advantage of using r.o.m.s is that many different functions can be obtained by simply re-programming the r.o.m. Thus, it is possible to have a basic circuit configuration, say for a sequential encoding circuit, in which the type of code can be changed by plugging in a new r.o.m. unit; this characteristic is sometimes referred to as a 'loadable personality'. This concept becomes very powerful when random access memory modules (r.a.m.s) are used since the 'personality' can then be changed dynamically. The natural extension of this philosophy is the adaptive logic systems described by Aleksander.[10]

3 Modular Realization of Digital Systems

Numerous attempts have been made to partition digital systems (in particular computers) into suitable basic modules which can take full advantage of l.s.i. technology. From the technology point of view the following properties are desirable for a logic systems module made in l.s.i.:

(a) high circuit density, that is a large number of gates.

(b) regular structure and interconnexion pattern.

(c) high circuit-to-edge-connector ratio,

(d) versatility in use,

(e) easily testable.

Though many of the modules suggested have been well suited for the technology, unfortunately due to a lack of a suitable system theory, they did not possess the universality required of such a device. In this Section we shall survey some of the more important sub-systems that have been proposed for systems realization.

Most of the work on digital sub-system components has been orientated towards the design of computers. One such system, described by Podraza, Gregg and Slager[11] uses four m.s.i. functional building blocks which are generally applicable to the design of parallel data-processing structures. Another way of attacking the problem has been to use cellular logic arrays, and considerable work has been done in this field.[12] Early work in cellular logic arrays was centred on the problem of developing algorithms that could be used to realize an arbitrary switching function in a given array, thereby showing that the array was a universal switching element. More recent work however, has concentrated on the use of special-purpose arrays, such as those proposed by Kautz,[13] Nicoud,[14] Dean[15] and the work of Deverell and others described in this issue.[16,17,18] Programmable cellular arrays have also been described by Jump and Fritsche[19] for use in implementing the control structure and micro-program for a digital computer. A somewhat similar solution to the problem of l.s.i. implementation, again using active cellular arrays, is the functional memory proposed by Gardner of IBM.[20] The system is based on an associative storage array composed of writable storage cells capable of holding three states. 0, 1 and 'don't-care' In this context the r.o.m. could be described as a cellular array; the chief advantage of the functional memory is that it allows the store size to be reduced by effectively storing prime implicant terms instead of canonical terms.

The l.s.i. modules described above are not commercially available to the logic designer but were discussed in order to indicate current trends in system design. Moreover, the majority of these systems have emanated from the computer industry and are orientated towards the specific problems (for example, control unit design) encountered in that field. At the present time no general-purpose sub-system modules, excluding r.o.m. and multiplexer which are really at a much lower system level, exist.

The only practical attempt to present a more generalized system of modular design is the PDP16 concept[21] which utilizes special register transfer modules (r.t.m.) to implement a digital system. The r.t.m. system consists of about 20 different p.c. board modules performing the basic functions of register processing and transfers, storage of data and control signals, control of processing operations, and interfacing with peripheral equipment. In use the designer constructs a data structure comprised of the appropriate r.t.m. modules, and then proceeds to specify, using a flow-chart technique, the required control and processing algorithms. The flow-chart devised in this way can be processed automatically to yield directly the wiring schedule for the control logic circuit.

To sum up then, at the present time there is no universal module at the sub-system level which can supersede the basic gate in digital system design. Walker[22] has proposed a system of node logic which satisfies many of the fundamental requirements, but it might be thought that the work still lacks a formal design procedure.

What is the reason for this state of affairs? Is it possible in fact to devise a universal systems module? The answer to these questions is contained in the fact that there is no formal systems theory. In order to evolve and use a specific module, a theoretical background must exist in order to generate a sound design procedure. The starting point for such a theory must be the specification and description of the system, leading to evaluation and design.

4 Representation of Digital Systems

The ideal methodology for representing logical structures in a c.a.d. environment should have the following characteristics:

(a) Capable of representing both hardware and software processes.

(b) Easily assimilated by the designer; simple to modify and edit.

(c) Unambiguous and concise descriptions, capable of serving as a means of communication between designers, implementers and users.

(d) Able to proceed from description to realization in either hardware or software form; should also give insight into the best method of implementation.

(e) Possible to handle parallel, that is concurrent operations, in synchronous and asynchronous modes.

(f) Must be possible to represent the information flow in large variable systems, that is at the macro or sub-system level rather than logic gate level.

(g) Systems evaluation performed by formal analysis at the behavioural level rather than by step-by-step simulation.

(h) Hierarchical, block structured format, capable of including pre-defined sub-systems.

Various techniques have been described in the literature for the description and design of digital systems; these methods may be generally classified into three basic areas, which are:

(1) *Functional descriptive programing languages*, such as register transfer languages, simulation languages, *APL*, etc.

(2) *Algorithmic techniques*, based on finite-state machine theory, such as state-tables, regular expressions, flow-charts, etc.

(3) *Directed graph techniques*, such as the use of state diagrams, Petri nets, etc.

Many of the required characteristics listed above for a specification and design system are present in one or other of these techniques, but in general most methods described to date fall short of the ideal methodology. For instance, procedure-orientated programing languages suffer from the inherent disadvantages that there is no formal mathematical structure. Consequently any design and evaluation procedure must take place as an exhaustive, sequential examination of all possible logic conditions. Moreover, this lack of formalism places large demands on the amount of storage space required. Of all the methods described two techniques, that of register transfer languages and Petri nets, have met with limited success. It is worthwhile describing these techniques in more detail.

4.1 *Register Transfer Languages*[23-25]

The intuitive design procedures used in computer systems engineering are normally centred around a predefined register configuration. The execution of a machine-code instruction set is then interpreted in terms of micro-order sequences (a set of which is called a microprogram) which control the required transfers and data processing operations between registers. These heuristic procedures have been semi-automated using a procedure orientated register transfer language (r.t.l.) to declare a proposed register structure and the required logical operations between them. Using this technique, micro-programs for a particular machine-code instruction set may be specified in a register transfer language as operational procedures, for example:

$$/C/ : T \leftarrow R+S \qquad (2)$$

indicates that when C = logic 1 the contents of register R are added to the contents of register S and the result placed in register T. In these procedures the contents of a register (the name and size of which must be initially declared in the program) are treated as a vector with n components: individual elements may be referred to by, for instance, using subscripts of the form:

$$T_{(5)} \leftarrow R_{(3)} \oplus S_{(2)}.$$

Various logical and arithmetical connectives, such as $+$, $\cdot$, $\oplus$ etc., are allowed in the language being applied component by component in the transfer operations. Essentially, register transfer languages are used to describe the parallel data paths and processing operations between registers. The control operations are implicitly specified by the ordering of the program statements (for synchronous systems) and by the use of various conditional relationships. For example, in equation (2) above, $/C/$ could be either a simple clock input (specified as

$/C_1/,/C_2/,/C_3/$ etc.) or a compound conditional of the form $/\bar{A}_1 A_3 \bar{A}_7 C_5 = 1/$. Timing and control in register transfer languages, particularly for asynchronous and parallel operations, can be a difficult problem.

Micro-programs (or logic systems in general) expressed in the form of register transfer language statements may be translated into a set of Boolean equations representing logic gate implementation of the system; unfortunately in most cases the resulting realization is grossly inefficient, requiring many more gates than conventional design methods. Register transfer languages may also be used for systems simulation and evaluation, and as a means of concisely documenting logic systems.

One language that has been used extensively (particularly by IBM) is the *APL* language based on the Iverson notation.[26,27] Iverson notation is essentially a general-purpose algorithmic language which provides compound and logical operations on binary vectors (registers) and arrays (store matrices) and allows the concise representation of complex sequential logic and inter-register transfers as micro-program statements. Iverson has been used to define a complete system[28] and as a logic design language in the ALERT system.[25] This design system was used to process a major part of the IBM 1800 computer; however, the resulting design required 160% more gates than the original system.

One of the major drawbacks of the r.t.l. technique is that the designer is constrained to think in terms of predetermined register structures with synchronous control; moreover, the r.t.l. approach is only applicable to hardware systems. The problem of designing the control part of a system using r.t.l. has been overcome to some extent by the work of Gerace[29] who showed how r.t.l. descriptions can be transformed into state-tables (for the operational and control functions of the system) which can then be manipulated using conventional switching theory. A similar procedure has been described by Stabler[30] which defines the control processes in terms of state-tables and uses r.t.l. statements for the operational logic; transformations between the two representations (indicating speed and hardware 'trade-offs') are also possible.

4.2 *Petri Networks*[31–33]

A more generalized solution to the problem of system specification and realization is based on the idea of Petri nets, which in principle are very similar to the state-diagram approach. The Petri net is basically a directed graph consisting of nodes and arcs (directed lines) which may be used to represent the control structure in a digital system. As illustrated in Fig. 4(a), the Petri net has two kinds of nodes: *places* drawn as circles, and *transitions* drawn as bars. Each directed line or arc, connects a place to a transition, or vice versa; in the former case the place is called an input place and in the latter an output place of the transition. Note that parallel, or concurrent, operations are easily represented on the Petri net.

The various paths through the Petri net can be simulated using a form of party game (first suggested by Holt) involving tokens, and the use of these for marking places in the net. Progress through the net, from one marking

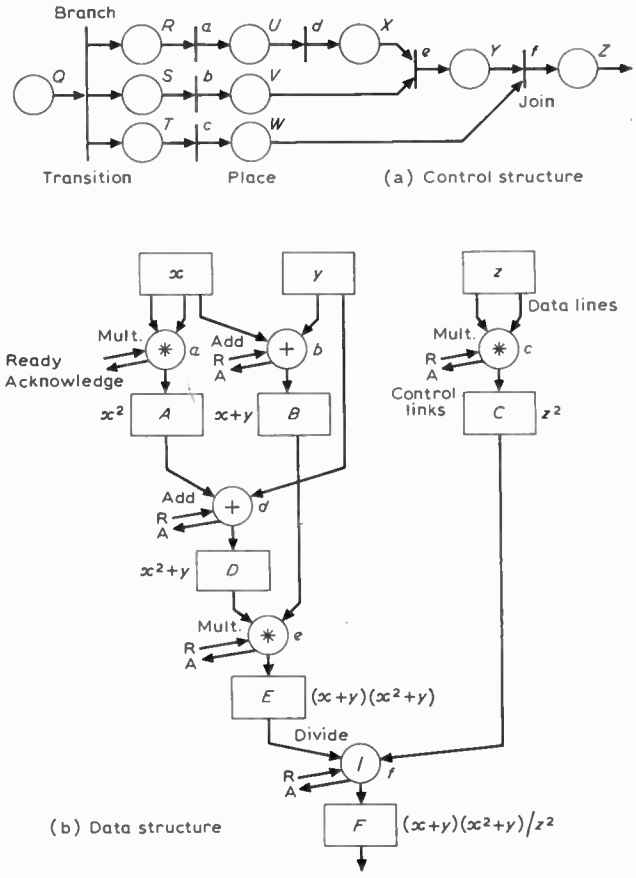

Fig. 4. Petri net structures.

to another, is determined by the *firing* of transitions according to the following rules:

(i) A transition is enabled if all of its input places hold a token.

(ii) Any enabled transition may be fired.

(iii) A transition is fired by transferring tokens from input places to output places.

When Petri nets are used to represent the control structures of digital systems asynchronous operation is assumed and control signals must be sent to and from the control and data structures. A ready signal is sent from the control structure to initiate operations in the data structure (such as addition, multiplication, etc.); the data processing unit replying with an acknowledge signal when the operation has been completed (the 'hand-shake' principle). The transition firing procedure for the Petri net is consequently modified to provide the basic steps:

(i) Remove tokens from input places.

(ii) Send a ready signal to the processing unit.

(iii) Wait for acknowledge signal.

(iv) Put token in output places.

Figure 4(b) shows the control and data structures for evaluating the expressions $(x+y)(x^2+y)/z^2$. The process is initiated by placing a token in place Q (equivalent to generating a ready signal) the data structure responding with an acknowledge signal when the registers x, y and z

are loaded. Then, applying the transition firing rules, as stated above, to the transitions *a*, *b* and *c*, the next stages of the process are initiated; this procedure is continued until the evaluation is complete, as indicated by a token in place *z*.

It is possible to replace the individual functions of a control network (for example: a place containing a token, branches, joins, etc.) by a hardware circuit. Using these components a direct translation from a Petri net into control logic may easily be accomplished.

These concepts have been employed in the LOGOS system[34] under development at Case Western Reserve University for the specification and realization of hardware/software processes. The LOGOS representational system divides a digital system (both hardware and software processes) into two directed graphs, one for data flow and the other for control. The data graph defines the algorithmic data structure and the transformations upon it, while the associated control graph sequences the transformations and defines its control flow. A hierarchical modular approach is adopted, where the final system is comprised of components specified at lower order levels. The control graphs can be directly implemented in terms of hardware, but it is not clear at the moment how the data graph may be realized. Considerable work has also been done on the derivation of analysis algorithms and simulation procedures.

There are many problems to be solved before an ideal design scheme can be developed. The register transfer language technique is adequate for the design of register structured systems, but it is specifically hardware orientated and analysis (as against simulation) algorithms have yet to be developed. Of all the methods described in this paper the LOGOS system, based on Petri nets, seems to be the most promising.

5 Conclusions

Integrated circuit technology has progressed rapidly over the last decade with the consequence that the original techniques of logic design using basic gate elements are rapidly becoming outdated. The current emphasis is on implementing digital systems using m.s.i. and l.s.i. modules performing sophisticated logical functions. Moreover, the proliferation of sub-system components which are becoming available on the market (such as micro-processor chips) is continually adding to the general complexity of logic systems design.

Unfortunately, theory has not kept pace with practice and we have now reached the stage when the lack of a suitable formal design theory at the sub-systems level is becoming a severe handicap. The logic systems of the future will be far too complex to design by intuitive methods alone.

It seems inevitable that computer assisted techniques must play a vital role in the design of the complex systems of the future. However at the present time there is no ideal specification, evaluation and design scheme available for logical systems. It is essential for the future development of digital systems that a suitable design methodology be established as soon as possible.

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STANDARD FREQUENCY TRANSMISSIONS— November 1973

(Communication from the National Physical Laboratory)

Nov. 1973	Deviation from nominal frequency in parts in 10^{10} (24-hour mean centred on 0300 UT)			Relative phase readings in microseconds NPL—Station (Readings at 1500 UT)		Nov. 1973	Deviation from nominal frequency in parts in 10^{10} (24-hour mean centred on 0300 UT)			Relative phase readings in microseconds NPL—Station (Readings at 1500 UT)	
	GBR 16 kHz	MSF 60 kHz	Droitwich 200 kHz	*GBR 16 kHz	†MSF 60 kHz		GBR 16 kHz	MSF 60 kHz	Droitwich 200 kHz	*GBR 16 kHz	†MSF 60 kHz
1	+0·2	0	0	688	603·3	17	0	−0·1	0	694	592·7
2	−0·1	0	0	689	603·4	18	+0·1	−0·1	0	693	593·7
3	+0·1	0	0	688	603·2	19	−0·1	0	0	694	593·7
4	−0·1	0	0	689	603·6	20	0	−0·1	+0·1	694	593·0
5	−0·1	0	0	690	603·7	21	+0·3	−0·1	+0·1	691	593·7
6	−0·1	0	+0·1	691	590·9	22	−0·3	0	0	694	593·9
7	0	−0·1	+0·1	691	591·8	23	0	−0·1	0	694	594·8
8	0	−0·1	+0·1	691	558·5	24	−0·1	−0·1	0	695	595·6
9	0	0	+0·1	691	589·4	25	−0·2	0	0	697	595·8
10	−0·1	−0·1	0	692	589·5	26	0	−0·2	0	697	597·4
11	0	−0·1	0	692	590·2	27	+0·2	−0·1	0	695	598·0
12	0	0	+0·1	692	590·5	28	−0·3	−0·1	0	698	598·5
13	−0·1	0	0	693	590·3	29	0	0	0	698	598·5
14	0	−0·1	0	693	591.2	30	−0·1	+0·1	0	699	597·7
15	0	−0·1	0	693	591·7	31					
16	−0·1	−0·1	0	694	592·2						

All measurements in terms of H-P Caesium Standard No. 334, which agrees with the NPL Caesium Standard to 1 part in 10^{11}.

* Relative to UTC Scale; $(UTC_{NPL} - Station) = +500$ at 1500 UT 31st December 1968.

† Relative to AT Scale; $(AT_{NPL} - Station) = +468{\cdot}6$ at 1500 UT 31st December 1968.

UDC 681.325.57

Cellular arrays for multiplication of signed binary numbers

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and
D. BASU, M.Tech.*

SUMMARY

Two cellular arrays for the multiplication of signed binary numbers using Robertson's algorithm have been described. It has been shown that this results in a considerable saving in hardware compared to previous schemes.

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1 Introduction

Methods for the implementation of multiplication of signed binary numbers using simple adder/no operation cells, arranged in an iterative array, have been proposed.[1,2] While Majithia and Kitai[2] have used Booth's algorithm,[5] starting the process of multiplication from the most significant bit(m.s.b.) and ending with the least significant bit(l.s.b.), Bandyopadhyay *et al.*[1] have shown that it is more economical to begin from the l.s.b. and end with the m.s.b. The cells used in both these arrays can be derived from the more basic cells suggested by Guild[3] for performing non-restoring division.

However these cells, used for multiplication,[1,2] are more complex, versatile and require more intercellular connexions because apart from the conditions of addition and subtraction the condition for doing no operation has been incorporated in them. It will be shown in this paper that using the same adder/no-operation cell suggested by Bandyopadhyay *et al.*,[1] considerable reduction in hardware can be achieved if Robertson's first method[4] is used. As in most of the computers using fixed point arithmetic, numbers are assumed to be fractional, and negative representation is in two's complement.

2 Robertson's First Algorithm

Let the two numbers to be multiplied be X and Y, where X is the multiplicand and Y is the multiplier. Then

$$X = X_0 + \sum_{i=1}^{n-1} X_i \cdot 2^{-i}, \qquad X_i = 0 \text{ or } 1$$

and

$$Y = Y_0 + \sum_{i=1}^{n-1} Y_i \cdot 2^{-i}, \qquad Y_i = 0 \text{ or } 1.$$

Here X_0 and Y_0 are the sign bits of the multiplicand and multiplier respectively.

According to Robertson's algorithm, the multiplier sign bit Y_0 is ignored at first and multiplication proceeds from the l.s.b. to the m.s.b., i.e. Y_1, according to the following simple rules:

(i) If $Y_i = 0$, shift the existing sum of partial products one bit to the right.

(ii) If $Y_i = 1$, add X to the existing sum of partial products and shift the new sum one bit to the right. Obviously, this result cannot be correct for negative multipliers and a correction is needed. This is easily done according to the following.

(iii) If $Y_0 = 0$, no correction is required.

(iv) If $Y_0 = 1$, i.e. the multiplier is negative, add the two's complement of X to the already formed sum of partial products to obtain the correct result.

3 The Realization

The algorithm can be easily realized by a cellular array using the same adder/no operation cell as suggested in Reference 1. The cell is shown in Fig. 1 and consists of

5 inputs and 5 outputs, governed by the following equations:

$$S = R \oplus C_{IN} \oplus Q\cdot(P \oplus X) \quad (1)$$

$$C_{OUT} = R\cdot C_{IN} + Q\cdot(P \oplus X)\cdot(R + C_{IN}) \quad (2)$$

where S = sum output of a cell,

R = input corresponding to the sum of partial products,

C_{IN} = carry input from the previous cell,

and C_{OUT} = carry output of a cell.

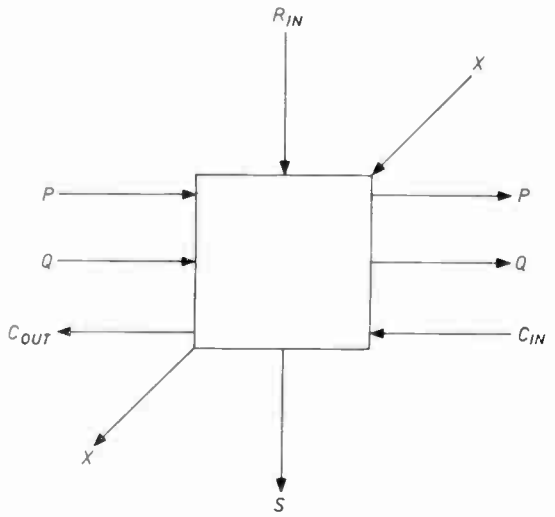

Fig. 1. The cell.

P and Q are the inputs controlling the mode of operation of the cell. The cellular array for the multiplication of two three-bit numbers is shown in Fig. 2. In the arrangement shown the Q inputs take up the values of the multiplier bits, with the l.s.b. connected to the cells in the first row, the next higher bit to the cells in the second row and so on. In this way, the Q-inputs to the cells in the last row correspond to the sign bit of the multiplier. The connexions to the P-inputs are done as follows. For all rows except the last row $P = 0$ and this corresponds to the condition of adding the true value of X. In the last row, $P = 1$ and the complement of X is added, effecting the required correction. The two's complement of X is formed by connecting Q to the carry input of the last cell in the row as shown in Fig. 2. It may be noted that if the multiplier is positive the Q-inputs to the cells in the last row are 0 and no correction takes place. This is evident from equations (1) and (2), because $Q = C_{IN} = 0$ gives the condition of no operation for any cell. Robertson's algorithm can result in overflow due to addition. This is taken care of by the arrangement shown in Fig. 2. When the multiplicand is shifted left (which is equivalent to shifting the partial product to the right), its sign bit is applied to the R input of the first cell in the next row. In this way, the sign of the partial product at each step is made equal to that of the multiplicand even though overflow might have occurred. It may be noted here that there can never be any overflow during the correction process as the two numbers being added are always of opposite signs.

4 Example

Let us assume that $X = 0{\cdot}11$ and $Y = 1{\cdot}11$.

Step 1. $Q = Y_2 = 1$, for the cells in the first row and X is added to 0·00 to obtain 0·11. This is shifted one bit to the right to give 0·011.

Step 2. $Q = Y_1 = 1$, for the cells in the second row and X is added to the partial product 0·011. This is an overflow condition and the result is 1·001. It is shifted right to obtain 0·1001.

Step 3. $Q = Y_0 = 1$, for the cells in the third and last row and the two's complement of X, i.e. 1·01 is added to 0·1001. The correct result is 1·1101.

5 Speed Considerations and a Faster Array

The speed of operation of the array shown in Fig. 2 is equal to $(3n-2)T$, where T is the delay of one cell. If one wants to have an increased speed of operation, one can have an arrangement of the cells as shown in Fig. 3, where Robertson's algorithm is carried out starting from the m.s.b. and ending with the l.s.b. The speed of operation in this case is equal to $(2n-1)T$ and is considerably faster.[2] The operation of the array is mostly self-explanatory and will not be described in detail here. The values of the multiplicand and multiplier have been chosen to be the same as those in the array of Fig. 2.

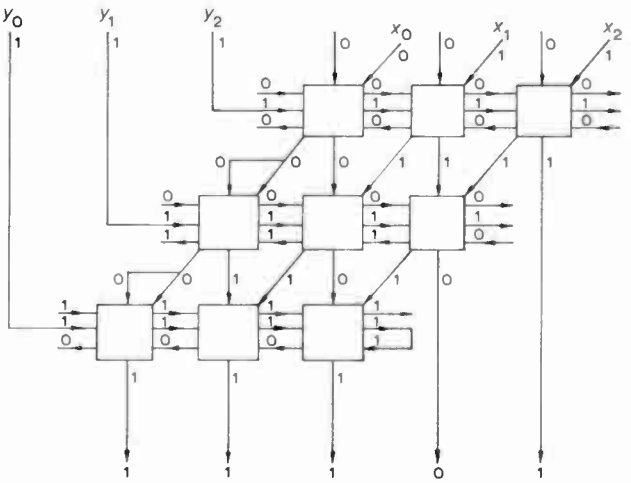

Fig. 2. Array for the implementation of Robertson's algorithm.

6 Conclusion

Two cellular arrays which permit the direct multiplication of two signed numbers (negative numbers being represented in two's complement) have been suggested. Both the schemes use Robertson's algorithm and for a given speed this results in a sizable reduction in hardware compared to any of the earlier methods. For instance, the speed of operation of the array of Fig. 2 is equal to that of the array suggested by Bandyopadhyay *et al.*[1] But, whereas the latter requires n^2 cells plus n EXCLUSIVE OR and n AND gates, the former requires only n^2 cells. Similarly, the array of Fig. 3 requires only $(3n^2-n)/2$ cells compared to the $(3n^2-n)/2$ cells and the n comparator cells of reference 2.

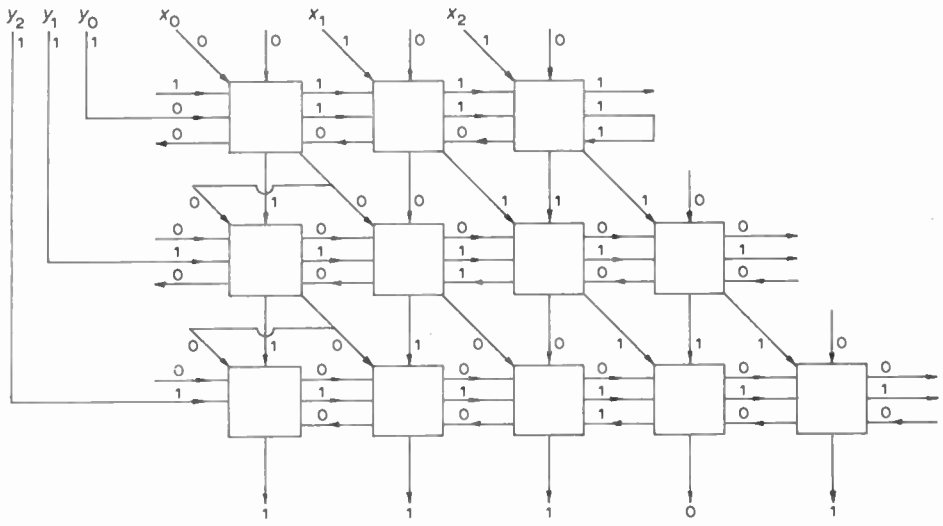

Fig. 3. Arrangement of the cells for faster operation.

7 Acknowledgment

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The design of cellular arrays for arithmetic

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SUMMARY

The past five years have seen the rapid development of iterative circuits performing many arithmetic functions. With the present state of l.s.i. technology in mind, this paper retraces the basic steps made in iterative circuit design and suggests that pipelined arrays are the most suitable for manufacture. The paper also suggests how general arithmetic arrays can be modified to perform non-arithmetical functions.

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1 Introduction

Recent large scale integration (l.s.i.) techniques such as collector diffusion isolation (c.d.i.) now enable circuits having up to 16×10^3 gates to be made on a single chip of silicon, 5 mm square. As c.d.i. is a bipolar process each gate is fast, about 4–5 ns. The process is therefore very suitable for the iterative circuits which have been designed over the past five years to give fast, parallel solutions to the basic arithmetic operations, multiplication, division, addition and subtraction. In a truly iterative array all cells are identical and each cell is connected only to adjacent cells. This paper briefly retraces the basic steps in the development of iterative circuits for multiplication and division. The paper then compares the general pipelined array with the unlatched equivalent and shows that not only is the pipelined array more efficient for general use, but also that it is the more suitable for manufacture at the present time. In the second part of the paper it is shown how a pipelined arithmetic array can be modified to act as a store or routing array. Another modification shows an array which can be used as a self-sorting file or as a pipelined arithmetic array.

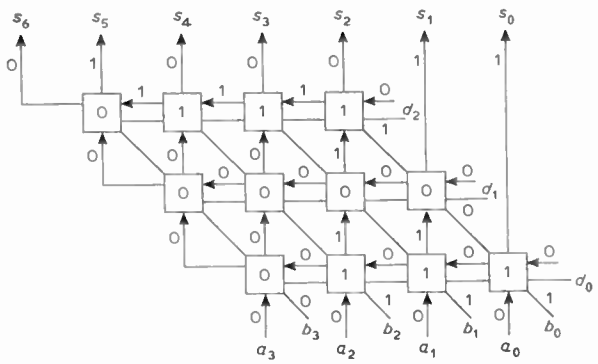

Fig. 1. Multiplying array using Hoffman cells.

2 Multiplication

Multiplication is a repetitive process whereby the multiplicand is successively shifted and added to itself, depending on the value of the multiplier. Pencil and paper multiplication illustrates the process. In Example 1, the multiplicand b = binary 0111 is multiplied by the

Example 1

b	0111
d	101
	0111
	0000
	0111
s	100011

multiplier, d = binary 101, to give product s = binary 100011, the partial products having been written down in the appropriate position and then added together. A cellular iterative multiplier follows a similar process. The array of cells is laid out as in Fig. 1, in a way suggested by Dean,[1] in order to give the spacial shift, the

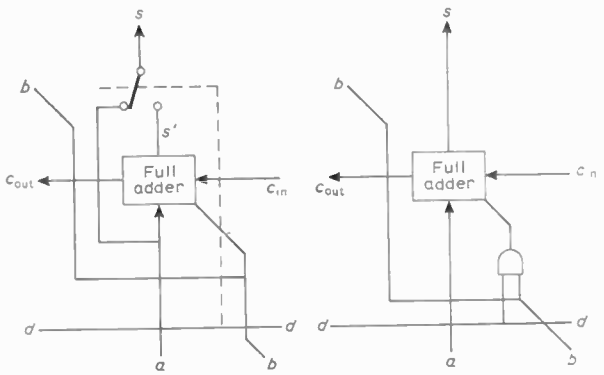

Fig. 2. Typical cells used for multiplication.

only difference being that the addition of the partial products occurs in a slightly different way. Each cell in the array of Fig. 1 adds its own partial product to the sum of partial products of cells vertically below it and also to any carry which may be present from the horizontally adjacent cell. Each cell therefore gives a sum output to the cell above and a carry output to the horizontally adjacent cell in the higher order column to its left. In Fig. 1, partial products are shown inside each cell.

Several different cells have been suggested. The two basic cells are the Hoffman switched full-adder cell[2] and the Guild gated full-adder cell.[3] Both cells are shown in Fig. 2. The Hoffman cell adds previous partial products a to the values of b and c_{in} to give s, but s' is only switched to S if d is at 1. If d is at 0 then a is routed to S. The Guild cell uses an AND gate to give the multiplication bd, then adds this to the previous partial products, a and input carries, c_{in}. The full function of the array in Fig. 1 is $S = (a+bd+c)$.

3 Division

The cellular logic approach for division again follows the pencil and paper method. Example 2 shows the

Example 2

```
      1.00011
      0.111
    ---------
1   | 0.00111
      .0111
    ---------
0   | 1.11001
    ---------
      .00111
    ---------
1   | 0.00000
    ---------
```

pencil and paper method of division, where a, binary 1.00011 is divided by b, binary 0.111. The divisor b is aligned with the dividend, a, so that the result of the first subtraction is less than 2. In the example, the first subtraction is successful as a positive remainder is obtained. The divisor, b, is then shifted one place to the right and another trial subtraction taken, which this time is unsuccessful because the remainder is negative, 1.11001. The quotient so far is 1.0. The divisor is shifted one place right again and subtracted from the previous remainder. This is seen to be exactly successful giving the quotient 1.01 and remainder 0.00000. The quotient is obtained by negating the sign bit of each remainder.

In order to simulate this process using a cellular circuit, Dean[4] devised the array of Fig. 3 which used switched full-subtractor cells. Each cell is similar to the Hoffman switched full-adder cell in that sum and difference have the same logical expression, but differ in that the borrow out c_{out}' is given by $c_{out}' = \bar{a}bc + \bar{a}b\bar{c} + abc$, whereas carry out c_{out} is $(ab+bc+ca)$. The same notation is used for both cells and arrays, except that for multiplication, the calculation propagates from bottom right to top left-hand corner of the array, and for division, the information passes row by row from top to bottom of the array. In Fig. 3, when a row subtraction has been successful, the final borrow is 0, setting the d line for the row to 0 and hence passing the remainder s' to S and hence to the a inputs of the next row. An unsuccessful subtraction gives a negative remainder, d is therefore 1 and the row's a input is switched to the next row's a inputs. Differences and borrows are shown inside each cell of Fig. 3.

This method has been chosen to illustrate division because it follows the pencil and paper method very closely and is therefore easy to understand. It is called restoring division because the remainder is repeated if a subtraction is unsuccessful. Another method of division, non-restoring division, has been thoroughly investigated by Guild[5] and is very suitable for use with his gated full-add/subtract type of cell.

4 Multiplication/Division Arrays

The structure of the arrays of Fig. 1 and Fig. 3 is similar, as are the cells, but propagation through these arrays is in opposite directions. However, the multiplication process can proceed in the same direction as division if a is first added to the top (bd_2) row. The sum $(a+bd_2)$ is then added to the bd_1 row and so on. As the most significant partial products are dealt with first, extra cells are required in the bottom row to ensure that all carries have been accounted for. The complete multiplication array is shown in Fig. 4 which is now

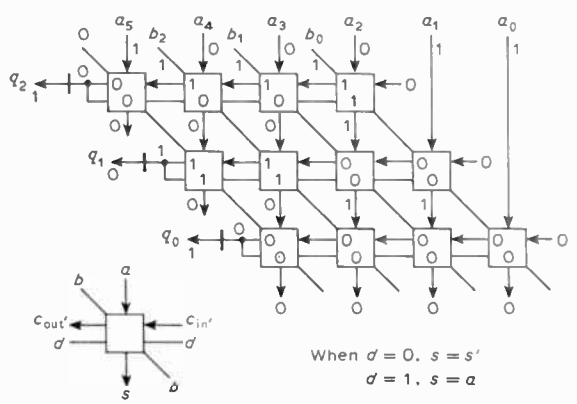

Fig. 3. Division array using switched full-subtractor cells.

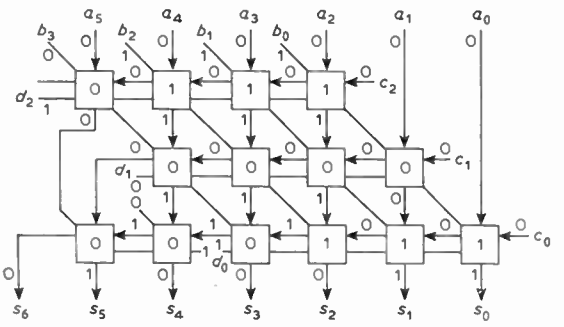

Fig. 4. Modified multiplication array.

similar in all important respects to the dividing array of Fig. 3.

The addition of control cells enables either multiplication or division to occur. The control cells decide whether the cell will act in switched full-adder or switched full-subtractor mode, with the aid of a control line to each cell; route input d to the array for multiplication, or accept output q for division; act as full-adders to cope with the extra carries generated by multiplication. The original idea of this array was due to Gex.[6] There have been several variations upon the basic idea.[7, 8, 9]

5 Pipeline Arrays

In the general arrays multiplication times are fast, being about $2n\tau$ for an array multiplying 2, n-bit numbers. τ is the propagation time for the sum and carry of each cell. Division is slow, about $n^2\tau$ as it is a row-by-row process. When asked to perform a variety of successive multiplications and divisions, a large general array would be fed with the input data at the speed of the slowest operation, division, and for a considerable portion of the operation cycle only a very small part of the array would be functioning at any one time. In other words, the bandwidth, the number of operations in a given time, would be poor.

In a pipelined array such as that shown in Fig. 5 each row is buffered from the next by the addition of D-type flip-flops, one to each of the b and a inputs of each cell. Each row performs multiplication or division on successive data as required and as directed by the control cells. A general pipelined array[10] which could calculate (ab/c) performed one such calculation with a maximum delay time of $2\tau(n^2+n)$, and performed m calculations in a delay time of $2n\tau(n+m)$. It is assumed that sum and carry propagation times for each cell are 2τ, the D-type flip-flops doubling the delay time, τ, of an unbuffered cell. Conventional arrays performing m similar calculations would take a delay time of $\tau nm(n+2)$. The pipeline method is always faster for more than two successive calculations and increases in effectiveness as n, the size of the array, increases.

In an analysis of pipeline methods for multiplication Hallin and Flynn[11] suggest that an Earle latch[12] would provide a very suitable way of buffering adjacent rows. It is simpler than a D-type flip-flop, using only five gates and having only two gate delays. Hallin and Flynn measured the effectiveness of pipelining a Guild multiplying array[4] and came to the conclusion that pipelining gave a 230% increase in efficiency if all rows were latched. This claim is rather optimistic, as the following section demonstrates, but in a more modest way the multiplier/divider is seen to be superior to its unlatched counterpart.

6 Efficiency of Pipelined Arrays

Efficiency is proportional to the array's bandwidth and inversely proportional to the amount of logic used in the array. It is easier to deal with a figure of merit, the reciprocal of efficiency, which is the product of the number of gates in the array, G and the maximum propagation delay, D. This gate-speed product should be as small as possible. The general pipeline multiplier/divider array will now be compared with the unlatched equivalent. Hoffman switched full add/subtract cells are used. Each of these cells has a minimum of 14 gates. Each cell in a pipeline array contains two Earle latches and has a total of 24 gates. Control cells are ignored as it is assumed that they are external to the iterative array.

For multiplication of n-bit inputs an unlatched array behaves in a similar way to the array of Fig. 1 which has $n(n+1)$ cells, a total gate count of $14n(n+1)$ gates, a delay time for one multiplication of $2n\tau$ and for m multiplications a delay time of $2mn\tau$. Thus

$$G.D = (14n(n+1))(2mn\tau).$$

In its dividing mode an unlatched general array has $14n(n+1)$ gates and a delay time for m divisions of $\tau n^2 m$, so

$$G.D = (14n(n+1))(mn^2\tau).$$

The latched array has $n(n+1)$ cells each with a gate count of 24 gates. In addition $n(n-1)$ latches are required so the array gate count is $(24n(n+1)+5n(n-1))$ gates. The delay time for one multiplication or division is $n\tau(n+2)$ and for m successive operations is $\tau(n+2)(m+n-1)$.

$$G.D = (n(29n+19))(\tau(n+2)(m+n-1)).$$

Table 1 shows the relative merits of each array for various values of m and using $n = 25$ bit wordlength.

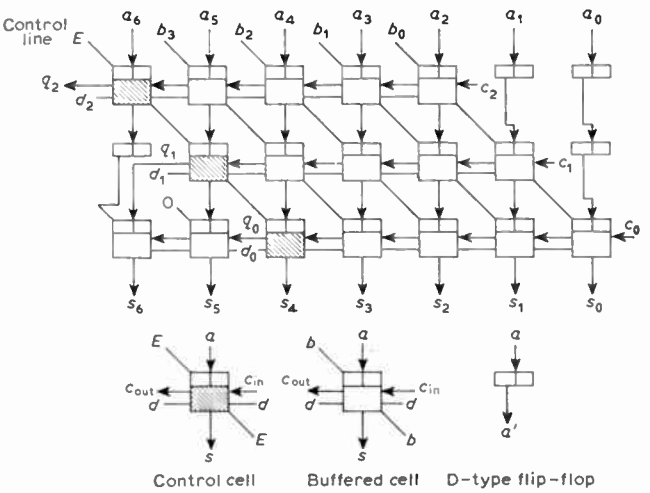

Fig. 5. General pipeline multiply/divide array.

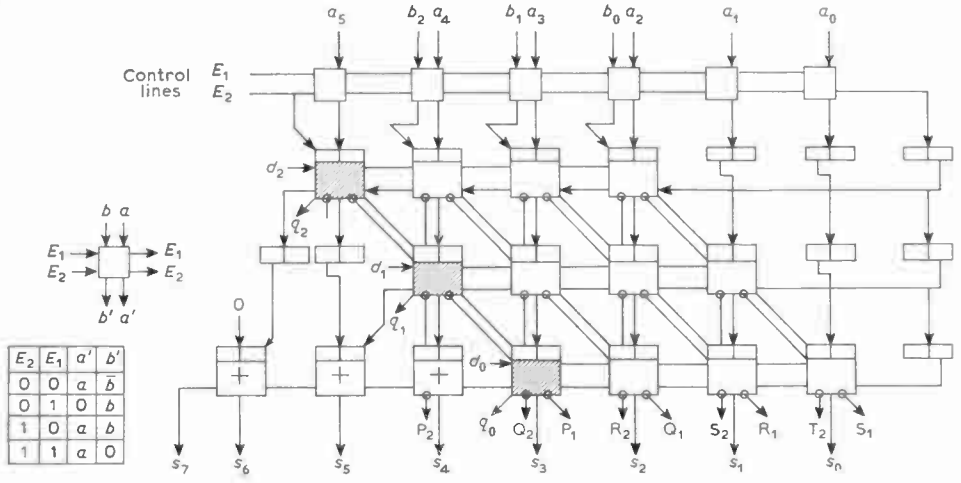

Fig. 6. General array for switching or arithmetic functions.

The array as an unlatched multiplier has been used as a base.

Table 1. Comparison of figures of merit of unlatched and latched arrays

		m				
		1	10	100	∞	$G.D.$
Unlatched array	As multiplier	1	1	1	1	$4{\cdot}55 \times 10^5 m\tau$
	As divider	12·5	12·5	12·5	12·5	$5{\cdot}69 \times 10^6 m\tau$
Latched array	As multiplier and divider	27·5	3·74	1·37	1·10	$5{\cdot}0 \times 10^5(m+24)\tau$

For a large number of successive multiplications and divisions the latched system is better by a factor of about 11, this being the ratio of latched to unlatched dividing $G.D$ products. This factor is dependent upon n. For arrays smaller than (5×5) there is little to choose between the two methods.

7 General Pipeline Arrays and Modern L.S.I. Technology

At present, l.s.i. technology is capable of producing circuits on chips 5 mm square, having about 16×10^3 gates per chip, with a delay of 4–5 ns per gate. Although c.d.i. and similar processes give smaller, faster bipolar transistors than before there are still problems with metalization and, most important of all, there are still problems with connexions to the chip. A typical number of connexions to a 5 mm square chip is 32. This severely limits the size of arrays that can be built at present, although large arrays could be made by connecting chips together on a thick film base.

A (4×4) array requires 32 leads if control cells are omitted. The omission of control cells from the general arrays during the manufacturing process is a logical step if the arrays are to be truly iterative and as versatile as possible. A (4×4) pipeline array has 20 latched cells and an additional 12 latches making a total of 540 gates. This leaves a lot of potential silicon area unused, so it would aid the manufacturing process if all the 12 latches were made as latched cells. An array capable of 4-bit multiplication would then be rectangular, a (4×8) array with 32 latched cells and 768 gates.

There is still plenty of scope for more complicated cells. One obvious improvement to performance of the general pipelined array would be the addition of carry-lookahead to each row. Alternatively, carry-save reduction with sign-bit lookahead could be used[13] which results in row propagation times proportional to $\log n$. Instead of improving performance, the versatility of the array may be increased. The remainder of this paper suggests two ways in which this may be done.

8 The Pipelined Arithmetic Array as a Storage and Routing Array

As this array performs such a multitude of functions it was called 'a general array'.[14] The addition of two gates per cell and additional control lines as in Figs. 6 and 7 make use of the storage properties of the array. Earle latches are no longer suitable, so two D-type flip-flops are used in each cell. The arithmetical properties of the array are as before. Figure 8 shows the relevant portions of the array which perform the storage and routing functions. When used as a store, parallel data are clocked

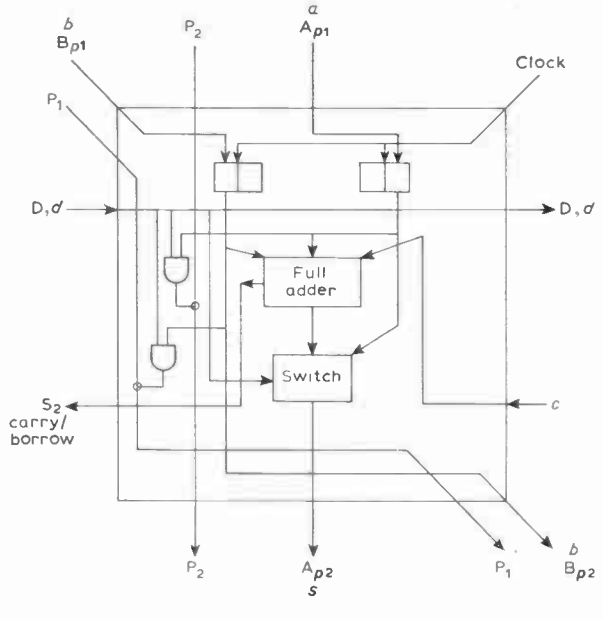

Fig. 7. General cell.

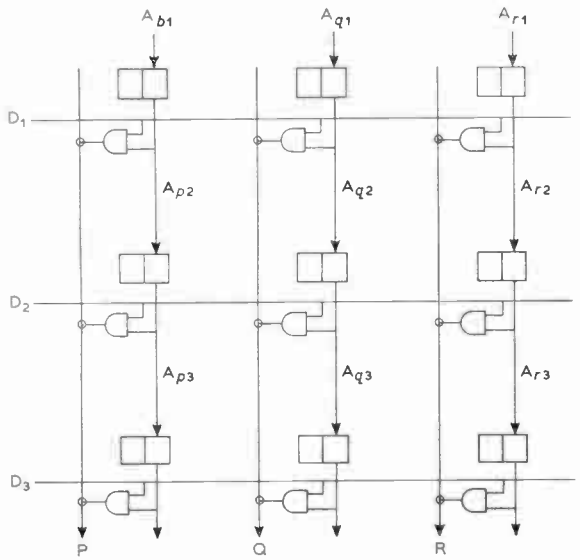

Fig. 8. Switching, storing and routing array.

into the array, each column acting as a shift register. Any row may be read out at P, Q and R by a 1 applied to the appropriate D input. Alternatively, parallel data may be presented at the parallel row (D) inputs and read out sequentially by clocking a 1 through the A_p, A_q or A_r columns as required. In a similar way, sequential data at each of the D inputs can be routed through the array to any of the outputs P, Q or R by programming the flip-flops appropriately.

9 Contents Addressed Memory/Arithmetic Array

Another common application of importance is sorting and contents addressed memories. Such devices, fabricated using l.s.i. techniques, are already available commercially, but perform only a limited set of operations. Iterative arrays to perform sorting have been previously described, especially by Kautz, who described an array possessing many of the desirable features of contents addressed memories.[15]

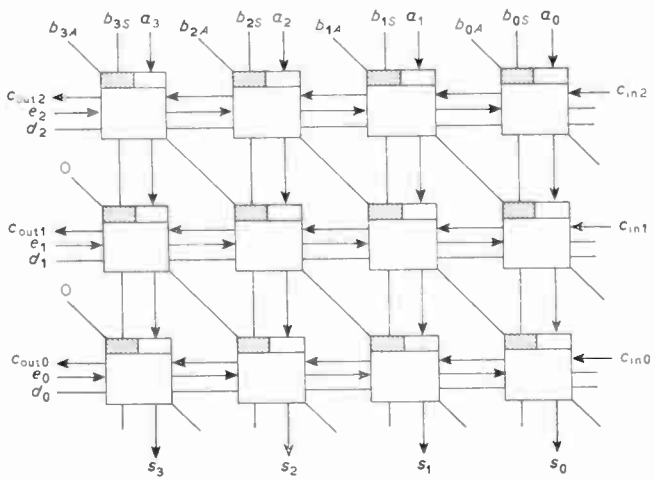

Fig. 9. Sorting/arithmetic array. (Clock and control line, M, not shown.)

A cell of the pipelined arithmetic array[10] already contains most of the properties required for searching ($B \leqslant A$ or $B \geqslant A$) and selection. The add/subtract circuitry of the Hoffman cell may be used to subtract B from A, the relative size of each word being indicated by the borrow output. The rectangular array shown in Fig. 9 can be used for either arithmetic functions such as multiply, divide, add and subtract or as a sorting array. The array has a completely iterative structure and uses a cell based on the Hoffman switched full add/subtract with storage. Only eight additional gates per cell are required to enable the array to perform both sorting and arithmetic operations. No control cells are shown in Fig. 9.

When used as an arithmetic array, the control line M is set to 1 so that the switches of Fig. 10, a schematic diagram of the sorting/arithmetic cell, are set in the positions shown. The full-adder/subtractor has its output S at either A or S′ depending on the state of d

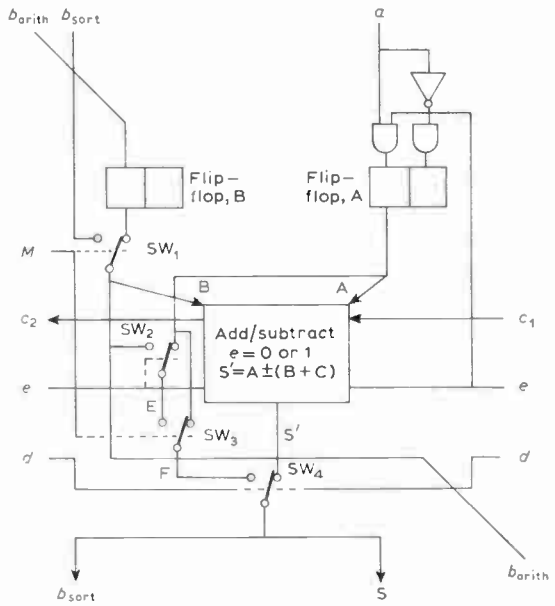

Fig. 10. Arithmetic/sorting cell.

and its inputs are A, B and C_1. Operation of the array is thus in the conventional pipeline manner, external control cells determining the arithmetic function to be carried out. Input and output registers have been omitted from Fig. 9. The usual requirement is for five registers to cope with input and output variables. The input registers B, D and C and the output register R for the quotient (a/b) are all n bits long. The output register, S, takes an m-bit word for the solution of $S = (bd+a+c)$. Input register A also has a length of m bits where $m = (2n-1)$. Of the $(m \times n)$ cells in the array only $n(n+1)$ are used for arithmetic. There is therefore a certain amount of redundancy in the array which is partially offset by the improvement in iterativeness.

The requirements for the sorting array's external circuitry are roughly the same as for arithmetic. The block diagram of Fig. 11 shows the $(m \times n)$ array with the control line M at 0 and the array therefore in the sorting mode. A sorted list of up to n words each of m bits

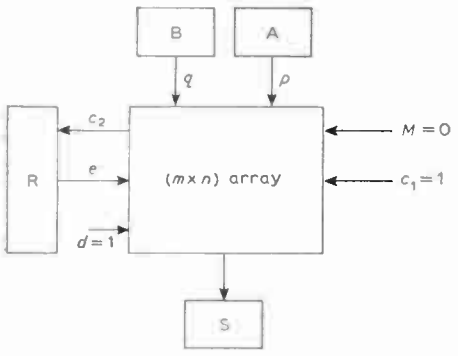

Fig. 11. Array used for sorting.

is fed to the array via the input register, A. Input register B stores the word which is to be added to the list. All flip-flops in the R register are initially set to 1 so that each cell is set to its subtract mode via the e control line. The word to be entered in the list, b, is subtracted from each of the words, a_n, in the stored list and the borrow output for each row appears at the input to the R register. Thus c_2 is 0 for each row where $a \geqslant b$ and 1 when $a < b$. This information is clocked into the R register. A further clock pulse to the A flip-flops of each cell will insert the new word, a, into the appropriate place, moving those words marked with a 1 down one row. The word in the lowest row m marked with a 1 will be copied into the output register, S. Words in rows marked with a 0 do not move.

Read-out is obtained by setting the most significant flip-flop of the R register to 1. With all the other flip-flops of this register at 0, the largest word, i.e. the word in the top row of the array, is routed to the S register. A sequence of 1's clocked down the R register will successively read the contents of the file into the S register in descending order of magnitude. Any read-out order may be chosen by programming the R register in the appropriate way.

Operation of the cell in the sorting mode is as follows. With $M = 0$, switches SW1 and SW3 change from the positions shown in Fig. 10. All d inputs are put to 1 so that F is connected to S. Initial conditions have e at 1 so the subtract mode is chosen and the B inputs at 0 so that each borrow output, c_2, is 0. As soon as the number to be read into the array, b, is applied to the b_{sort} inputs, subtraction occurs in each row of the array, the c_2 outputs going to 1 if $b > a$. Each c_2 output sets the R register, each output of which is connected to the e line of the same row. With e at 0 the gates at the inputs to the A flip-flop of each cell are inhibited and B is routed to S. When e is 1 the gates at the inputs of the A flip-flops are enabled and A is routed to S. Thus when all the A flip-flops are clocked, rows having their e lines at 0 retain the same word as before: the top row of those rows having their e line at 1 is filled by b via the b_{sort} inputs; all other rows having their e lines at 1 move down one row.

Circuitry in addition to the Hoffman cell with storage comprises two AND gates at the A flip-flop input and switches SW1, 2 and 3, which are

$$B = Mb_{arith} + \bar{M}b_{sort}$$
$$E = Be + A\bar{e}$$
$$F = EM + A\bar{M} \quad \text{respectively.}$$

The function E may be found in the add/subtract circuitry of the Hoffman cell. A total of eight additional 2-input gates are required to give the Hoffman cell with storage the capability of acting in a sorting capacity.

10 Conclusion

This paper has briefly outlined the progress made in the design of iterative cellular arrays for arithmetic, and has also shown how the pipeline array can be extended to perform non-arithmetic functions.

It will soon be possible to make iterative arrays on a commercial scale. It is necessary, then, to ensure that the arrays adopted for manufacture are those which are best suited to the state of l.s.i. technology. At present, with limitations to the number of connexions to the chip lagging behind the amount of logic that can be built on the chip, it is sensible to adopt arrays such as the pipeline array which have large cells. It has been shown that despite its relatively large cell the pipeline array is more efficient than its unlatched counterpart. As it also suits present technology better, it is therefore the most useful type of arithmetic array so far devised. It is also suggested that the user should provide his own control cells to define the functions he requires. The array may then be made completely iterative and of more general use.

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Design of NAND logic switching circuits

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SUMMARY

Problems in switching theory can be solved using universal NAND logic elements. The design of these circuits is optimized by using a factor procedure to ensure gate minimality with specified fan-in restrictions. The method suggested provides a means of obtaining hand solutions and can be suitably adapted for computer programming.

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List of Principal Symbols

I number of inverted literals present at even gate levels, or true literals present at odd levels
P number of products
P_B number of products in factored bracket
S number of sums
N number of NAND gates
N_1 number of NAND gates before factoring
N_2 number of NAND gates after factoring
ΔN change in NAND gate count
n number of terms being factored
i number of isolated inverted literals
t number of isolated true literals
ΔP number of additional products generated by factoring
ΔS number of additional sums generated by factoring
c.f. sum of products common factor
$G_{c.f.}$ number of gates required to realize a common factor
ΔZ_p change in fan-in requirement at second gate level
ΔZ_s change in fan-in requirement at first gate level

1 Introduction

Algorithmic methods have been developed to solve switching problems with the minimum number of NOR gates, for specified fan-in restrictions.[1] These methods were applied to NAND logic by the method of dualizing, thereby maintaining a strictly isomorphic relationship between the NOR and NAND solutions. This is not an entirely satisfactory procedure since NAND circuit solutions cannot be obtained directly, and the problem must first be related to the NOR circuit solution. This of course also presumes that the most economical NAND solution is the dual of the minimal NOR solution.

The writer has developed direct methods for solving switching problems, minimally, using NAND gates. This procedure entails factoring the Boolean function being realized, instead of using the duality property of NOR and NAND circuits as suggested by Zissos and Duncan.[2]

Factoring is first used to optimize 2-level sum of products functions. This procedure is referred to as first-order factoring. The terms thus obtained are again factored and the procedure then referred to as second order factoring. The 4-level sum of products function resulting from second-order factoring may again be factored, the final step being referred to as third-order factoring.

2 Objectives of Algebraic Reduction

A general transmission function written directly from a table of combinations will seldom result in the most economical circuit realization. These functions can, in most cases, be manipulated to reduce the number of gates required to realize the function. If fan-in restrictions are specified these must also be taken into account during the process of minimizing.

The immediate objective after extracting the standard sum function from a table of combinations is to reduce

the complexity of the function by algebraic methods. This is done by putting the function into a form in which the number of occurrences of the literals, which represent switching variables, is as small as possible. Each appearance of a literal in the function may correspond to a contact in a network so the number of physical contacts in a network is determined by the size of the function. All methods of algebraic reduction therefore have the common aim of eliminating, or reducing to a minimum, the occurrence of each literal present in the standard sum.[3] The minimum sum produced by algebraic (or graphical) methods contains no redundant terms, or redundant variables. Many functions may have more than one minimum sum. However, because the minimum sum is not always consistent with gate minimality, and because the number of terms in the minimum sum, or the number of literals in any term, may violate fan-in restrictions additional procedures must be introduced to enable the minimum sum form of a switching function to be changed to a form which will ensure optimal gate minimization.

3 Suggested Procedure for Optimal Realization of Minimal Boolean Functions using NAND Logic

The following procedure is suggested for obtaining the optimal solution of combinational switching problems using NAND logic:

(i) state the problem,

(ii) set up a table of combinations,

(iii) obtain the standard sum from the table of combinations,

(iv) use the Quine/McCluskey method to obtain a minimum sum-of-products,[4]

(v) Factor† the terms of the minimum sum to obtain gate minimality for specified gate fan-in restrictions.

Steps (i) to (iv) are well established and the minimum sum obtained in step (iv) therefore provides a starting point from which a factor algorithm can be developed.

4 Reducing the Gate Count in NAND Circuits

The number of NAND gates required to realize a switching function, with no fan-in restrictions can be denoted by the formula:

$$N = I+P+S.$$

For example, we can calculate the number of NAND gates required to realize the following functions:

(i) $A\bar{B}+C\bar{D}+XY$

$I = 2$ ($\bar{B}$, $\bar{D}$ present at second level)

$P = 3$

$S = 1$

$N = 2+3+1 = 6$

(ii) $A(\bar{B}+\bar{D})+XY$

$I = 0$ (inverted literals now at odd level)

$P = 2$

$S = 2$

$N = 0+2+2 = 4$

(iii) $(A+B)(X+C)(A\bar{Y}+D)$

The function has to be effectively OR'ed with 0. This entails using an additional gate, i.e.

$0+(A+B)(X+C)(A\bar{Y}+D)$

$I = 6$ (A, B, D, X, C at third level and $\bar{Y}$ at fourth level)

$P = 2$

$S = 4$

$N = 6+2+4 = 12.$

4.1 *Change in Gate Count Caused by Factoring*

If two or more products in a two-level sum of products are combined to form a single product with a common factor the gate count may be affected. If the change in gate count is signified by ΔN then

$$\Delta N = N_2 - N_1$$

where N_1 is the gate count before factoring.

N_2 is the gate count after factoring.

$$N_1 = I_1+P_1+S_1$$

and

$$I_1 = i$$
$$P_1 = n$$
$$S_1 = 1$$

so

$$N_1 = i+n+1$$
$$N_2 = I_2+P_2+S_2$$
$$I_2 = t$$
$$P_2 = P_B+1$$
$$S_2 = 2$$

so

$$N_2 = P_B+3+t$$
$$\Delta N = N_2-N_1$$
$$\Delta N = P_B-n+2+t-i \qquad (1)$$

Note: i only represents a gate saved if the variable to which it applies does not exist elsewhere as an isolated inverted literal or as a true literal in a product.

Similarly, t only represents an additional gate if the variable to which it applies does not appear as an isolated literal in some other factored bracket, or as an inverted literal in a product.

4.1.2 Maximum change in gate count

The maximum change in gate count is obtained as follows:

$$\Delta N = P_B-n+2+t-i$$

but

$$n = P_B+t+i$$

so

$$\Delta N = P_B-(P_B+t+i)+2+t-i$$
$$= 2-2i$$
$$\Delta N = 2(1-i).$$

† Factoring is a term used here to denote the process whereby two or more terms in a Boolean expression are combined into one term with a common factor. Factoring will therefore affect the fan-in requirement as well as the gate count in a switching function.

Table 1

ΔN for sums of products expression with varying fan-in restrictions

Function	Fan-in	Factors	Δn Eqn. (1)	Eqn. (2)	Eqn. (3)	Total
$\bar{A}BC+\bar{A}XY+\bar{A}W$	2	$\bar{A}(BC+[XY+W])$	2	–	2	4
$XY\bar{A}+XY\bar{Z}+XY\bar{W}$	2	$[XY](\bar{A}+[\bar{Z}+\bar{W}])$	−4	2	2	0
$ABCD+AX$	2	$A([BC]D+X)$	2	2	–	4
$abcde+abxy+g$	2	$[ab](c[de]+xy)+g$	2	4	–	6
$WXY\bar{Z}+WXY\bar{A}$	3	$[WXY](\bar{Z}+\bar{A})$	−2	2	–	0
$ABCDEFG+ABXYZ$	3	$AB(CD[EFG]+XYZ)$	2	2	–	4
$ABCDE+AWXYZ$	4	$A(BCDE+WXYZ)$	2	–	–	2

If only two terms are being factored then the maximum gate saving occurs when $i = 2$ and ΔN then becomes -2. On the other hand the maximum increase in gate count occurs when $i = 0$. This time ΔN becomes $+2$ and is independent of the number of terms.

5 Fan-In Restrictions in Two-Level (OR-AND) Circuits

5.1 *Meeting Fan-In Requirements at the 'AND' Level*

When a Boolean two-level sum of products function is factored there may be a resultant change in fan-in requirements. For example, if two terms are factored then the fan-in requirement for the 'sum' part of the factored expression is 2.

This does not benefit the designer however, unless the 'products' also meet the fan-in specification. For example, if we consider the sum of products:

$$S = (X_1 . X_2 \ldots X_m)+(X_1 . Y_1 . Y_2 \ldots Y_n);$$

after factoring:

$$S = X_1(X_2 . X_3 \ldots X_m+Y_1 . Y_2 \ldots Y_n).$$

If S is to meet a fan-in requirement of say, 2, then the products $X_2 . X_3 \ldots X_m$ and $Y_1 . Y_2 \ldots Y_n$ must now be factored, so that they will not violate this restriction. When this procedure is completed each additional product generated will increase the gate count by 2. Therefore,

$$\Delta N = 2\Delta P. \qquad (2)$$

For example, factoring the following expressions to meet a fan-in restriction of 2 results in the indicated changes in gate count. In example (iii) the 'sum' function still requires a fan-in of 3.

Function	Number of additional products generated	ΔN
(i) $\bar{A}BC$		
$\bar{A}(BC)$	1	2
(ii) $ABCD$		
$(AB)(CD)$	2	4
(iii) $ABC+DEFG+HIJKLM$		
$(AB)C+(DE)(FG)+(HI)(JK)[(LM)]$	7	14

5.2 *Meeting Fan-In Requirements at the 'OR' Level*

When fan-in restrictions are violated it may be necessary, in order to meet the fan-in specification, to combine two or more products which have no common factor. Each additional sum generated by this means increases the gate count by 2. For 'sum' functions then:

$$\Delta N = 2\Delta S. \qquad (3)$$

The following examples show the changes in gate count created when the terms, of sums of products functions, are grouped to meet a fan-in requirement of 2.

Function	Number of additional sums	ΔN
$AB+C\bar{D}+EF+GH$		
$(AB+C\bar{D})+(EF+GH)$	2	4
$AB+CD+EF+GH+KL+MN$		
$[(AB+CD)+(EF+GH)]+(KL+MN)$	4	8

6 Realizing Sum of Products OR/AND Expressions

Sums of products OR/AND expressions can now be factored for optimal realization to meet specified fan-in requirements. We refer to the procedure as first-order factoring. ΔN obtained for factoring some simple functions for specified fan-in requirements is shown in Table 1.

Equations (1), (2) and (3) are applied to each function and the results summed to give a final value for ΔN. When the parameters of ΔN sum to zero this signifies that the factoring procedure has not altered the gate count.

6.1 *Factoring Multi-term Functions*

When factoring functions with large numbers of terms the procedure can be facilitated by constructing a factor diagram, as illustrated in Table 2, for the function

$$S = DBC+ADB+ZBC+BC\bar{Y}+\bar{X}Y+\bar{A}Y.$$

The possible factors with ΔN in each case, is shown for each pair of terms, in the appropriate matrix element. The number of gates saved by using repeated sub-products is shown in the leading diagonal of the matrix.

6.1.1 Selecting the factors

If there are no fan-in restrictions then the factored

Table 2

Factoring diagram $\Delta N = t - i + P_B$

	DBC	ADB	ZBC	$BC\bar{Y}$	$\bar{X}Y$	$\bar{A}Y$
DBC	DB 0 *BC −1 DC 0	$DB(A+C)$ 2 $B(DC+DA)$ 2 $D(BC+AB)$ 2	$BC(Z+D)$ 2 $B(CD+CZ)$ 2 $C(BD+ZB)$ 2	$BC(D+\bar{Y})$ 0 $B(CD+C\bar{Y})$ 2 $C(BD+B\bar{Y})$ 2		
ADB		AD 0 DB 0 AB 0	$B(AD+ZC)$ 2	$B(AD+C\bar{Y})$ 2		
ZBC			ZB 0 *BC −1 ZC 0	$BC(Z+\bar{Y})$ 0 $B(CZ+C\bar{Y})$ 2 $C(BZ+B\bar{Y})$ 2		
$BC\bar{Y}$				*BC −1 $C\bar{Y}$ 0 $B\bar{Y}$ 0		
$\bar{X}Y$					$\bar{X}Y$ 0	$Y(\bar{A}+\bar{X})-2$
$\bar{A}Y$						$\bar{A}Y$ 0

* Note: BC is a repeated sub-product only if fan-in restriction is 2.

pairs are only selected if they result in gate reduction either by using equation 1 or by the use of repeated sub-products. In the example illustrated, if a fan-in of 3 is stipulated, the following solution is obtained directly from Table 2:

$$Y(\bar{A}+\bar{X})+BC(Z+\bar{Y})+D(BC+AB).$$

The first term is selected at the $\Delta N = -2$ level, the second at the $\Delta N = 0$ level and the last at the $\Delta N = 2$ level. The gate change for the complete transformation is

$\Delta N = -2+0+2$

$\Delta N = 0$ but the fan-in restriction is now 3 instead of 6.

The example is illustrated in Fig. 1.

If a fan-in of two is required the sum function at the first level is reduced by sub-dividing the expression to give

$$Y(\bar{A}+\bar{X})+[(BC)(Z+\bar{Y})+D(AB+BC)].$$

This alteration, which includes the bracketing of BC increases ΔN by 4. However one gate is saved because BC is now a repeated sub-product.

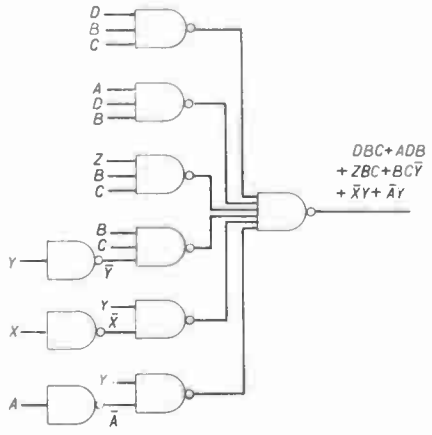
6.2 *Second-order Factoring*

Having optimized the two level sum of products function, the problem of factoring the four level sum of products function, created by this process, is now considered. This procedure is referred to as second order factoring.

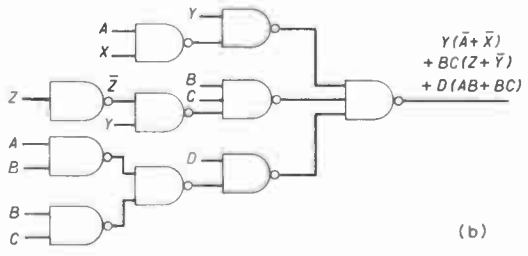
Functions containing elements of this type can be expressed as follows:

(i) $X_1(\text{c.f.})+X_2(\text{c.f.})+\ldots+X_n(\text{c.f.})$ (4a)

X_t is a Boolean product or literal



(a) Realization of $DBC+ADB+ZBC+BC\bar{Y}+\bar{X}Y+\bar{A}Y$
fan-in requirement = 6
number of gates = 10



(b) Realization of $Y(\bar{A}+\bar{X})+BC(Z+\bar{Y})+D(AB+BC)$
fan-in requirement = 3
number of gates = 10
ΔN = 0

Fig. 1.

or

(ii) $X_{c.f.1}(S_1)+X_{c.f.2}(S_2)+\ldots+X_{c.f.n}(S_n)$ (4b)

where $X_{c\ f.i} = X_i$(c.f.).

6.2.1 Change in gate count

If N_1 is the number of NAND gates required to realize expression (4a) before factoring then the gate count can be expressed as follows:

$$N_1 = I_1+P_1+S_1+G_{c.f.}$$

and $I_1 = i$

$P_1 = n$

$S_1 = 1$

so $N_1 = 1+i+n+G_{c.f.}$.

Factoring equation (4a) we obtain:

$$\text{c.f.}\,(X_1+X_2+\ldots+X_n).$$

If N_2 is the number of NAND gates required to realize the factored function then:

$$N_2 = I_2+P_2+S_2+G_{c.f.}$$

$I_2 = t$

$P_2 = P+1$

$S_2 = 2$

so $N_2 = t+P+3+G_{c.f.}$

but

$$\Delta N = N_2-N_1$$
$$= t+P+3+G_{c.f.}-(1+i+n+G_{c.f.})$$
$$\Delta N = t-i+P-n+2. \quad (5)$$

The common factor in this case has no affect on ΔN. If second-order factoring exists in the form of equation (4b) then:

$$\Delta N = 2(1-n).$$

We will see later that this is similar to third-order factoring.

6.2.2 Examples of second-order factoring

The application of equation (5) is clarified in the following examples. In each case second-order factoring is applied to illustrate the change in gate count

(i) $\bar{B}(DX+AY)+\bar{C}(DX+AY)$

factoring:

$(\bar{B}+\bar{C})(DX+AY)$

$\Delta N = 0-2+0-2+2$

$\Delta N = -2$

(ii) $B(AF+GD)+C(AF+GD)$

factoring:

$(B+C)(AF+GD)$

$\Delta N = 2-0+0-2+2$

$\Delta N = 2$

(iii) $BD(WX+YZ)+CD(WX+YZ)+XY(WX+YZ)$

factoring:

$(BD+CD+XY)(WX+YZ)$

$\Delta N = 0-0+3-3+2$

$\Delta N = 2.$

Example (iii) is illustrated in Fig. 2.

If second-order factoring is restricted to two terms at any one time then:

$$\Delta N = t-i+P-2+2$$

so $\Delta N = t-i+P.$

The limits of gate change are therefore:

$$\Delta N = \pm 2.$$

6.3 *Third-order Factoring*

Third-order factoring involves factoring a function created by second-order factoring. The general form of the function, in which factors are present, is:

$$S = (S_1)(\text{c.f.})+(S_2)(\text{c.f.})+\ldots+(S_n)(\text{c.f.})$$

where c.f. is a sum of products common factor.

S_i is a sum of terms in which the individual terms may be products or isolated literals.

When factoring at this level particular consideration must be given to the resulting changes in gate fan-in requirements.

If N_1 signifies the number of gates required to realize a function of this type before factoring, then:

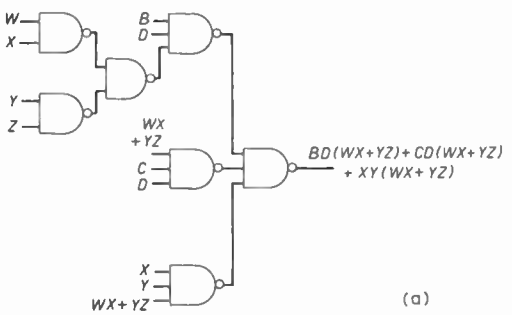
$$N_1 = I_1+P_1+S_1+G_{c.f.}$$

and $I_1 = i$

$P_1 = n+P$

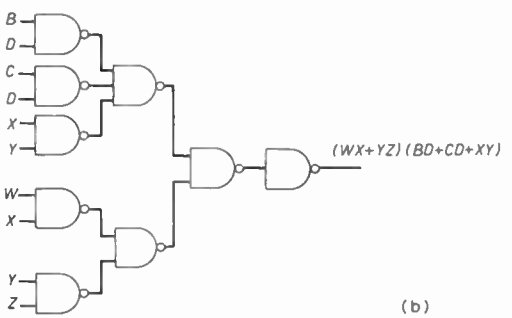
$S_1 = n+1$

so $N_1 = i+P+2n+1+G_{c.f.}$.



(a) Realization of $BD(WX+YZ)+CD(WX+YZ)+XY(WX+YZ)$

number of gates = 7



(b) Realization of $(WX+YZ)(BD+CD+XY)$

number of gates = 9

$\Delta N = +2$

Fig. 2.

Factoring such a function we have:

$$(S_1+S_2+\ldots+S_n)(\text{c.f.})$$

and N_2, the number of gates required to realize this function is given by:

$$N_2 = I_2+P_2+S_2+G_{\text{c.f.}}$$
$$I_2 = i$$
$$P_2 = 1+P$$
$$S_2 = 2$$

so $$N_2 = 3+P+i+G_{\text{c.f.}}$$

but

$$\Delta N = N_2-N_1$$
$$= 3+P+i+G_{\text{c.f.}}-(i+P+2n+1+G_{\text{c.f.}})$$
$$\Delta N = 2(1-n). \quad (6)$$

If only two terms are factored then ΔN is always -2.

6.3.1 Examples of third-order factoring

The constancy of ΔN for third-order factoring is shown in the following examples:

(i) $(B+C)(AF+GD)+(B+C)(XY+WZ)$

factoring:

$(B+C)(AF+GD+XY+WZ)$

from equation (6) $\Delta N = -2$

(ii) $(H+G)(A\bar{B}+BF+C)+(B\bar{D}+XY)(H+G)$

factoring:

$(H+G)(A\bar{B}+BF+C+B\bar{D}+XY)$

from equation (6) $\Delta N = -2$.

Note: ΔN is always -2 for third-order factoring.

6.4 *Effect of Factoring of Fan-In Requirement*

Multi-term functions can be systematically factored by combining terms in groups of 2. To simplify this operation the factor diagram can be used as previously illustrated. The effect of this procedure on the fan-in requirement is now considered.

For first-order factoring, the number of terms in a function S is reduced by X where X is the number of factored pairs in the function. Therefore

$$\Delta Z_s = -X. \quad (7)$$

If P_t denotes the number of literals in the largest product before factoring, and P_{ct} the number of literals in the common factor, then after factoring:

$$\Delta Z_p = (P_{ct}-P_t) \text{ or } -P_{ct} \text{ (whichever is the larger).} \quad (8)$$

For second-order factoring, the fan-in requirement at the first level will be reduced by one for each pair of terms factored. The size of the products are not affected by second-order factoring. Thus

$$\Delta Z_s = -X \quad (9)$$
$$\Delta Z_p = 0 \quad (10)$$

For third-order factoring, the number of sums is increased by the number of terms in the smaller of the two brackets being factored. Again, the product terms are not affected. Thus

$$\Delta Z_s = X_s \quad (11)$$
$$\Delta Z_p = 0 \quad (12)$$

where X_s is the number of terms in the smaller of the two brackets, or the number of terms in each bracket, if they contain the same number of terms.

In summary, for each pair of terms factored, the change in fan-in requirement is given by:

	ΔZ_s	ΔZ_p
first-order factoring	-1	$(P_{ct}-P_t)$ or $-P_{ct}$
second-order factoring	-1	0
third-order factoring	X_s	0

7 Conclusion

When optimizing Boolean functions for gate minimality any increase in gate fan-in requirements is undesirable. The chief advantage of this method is that ΔZ is never increased for first- and second-order factoring. The method guarantees an optimized result in terms of gate minimality for a specified fan-in restriction. A suitable program for computerized solutions is at present being tested at the University of Calgary.

Third-order factoring would only be used if the resultant increase in ΔZ_s did not cause a violation of gate fan-in requirements, if such a limit had been specified.

8 References

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Programmable shift registers for numerical multiplication

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SUMMARY

A programmable shift register using 'modulo 2' or (non-carrying) binary arithmetic is briefly described. The additional problems of making a programmable shift register for numerical binary arithmetic are examined in some detail. An experimental programmable shift register made from standard integrated circuits is described together with performance tests. Various uses of the device are suggested. Its use as a coefficient multiplier in a computer using serial digital techniques where analogue techniques were previously used is examined.

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1 Introduction

An electronically programmable shift register which can be used for binary multiplication has been described by Griffiths and Tomlinson.† Their principal interest was in 'modulo two' or 'non-carry' binary arithmetic. The advantages of few connexions and relatively fast multiplication are attractive to those concerned with digital computing techniques. The authors have therefore considered the practical details required to make a programmable shift register perform true binary arithmetic multiplication.

Although the full advantages of the technique will not be obtained until the device is constructed as a single integrated circuit, a model made up of standard logical elements has been designed, made and tested so that the device may be evaluated for various applications.

2 Serial Binary Multiplication

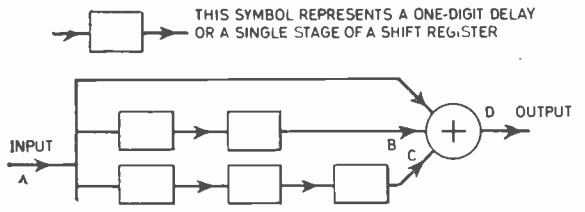
Binary numbers are usually represented in pulse trains with the least significant digit leading or occurring first in time. The significance, or the power of two, of each digit is determined by the time of arrival of a pulse relative to some clock controlling the system. Clearly if a pulse train is delayed by one pulse period the number represented by the pulse train is doubled. Multiplication by an exact power of two can therefore be achieved by a series of shift register stages which produce the appropriate delay.

Multiplying by a binary number other than an exact power of two can be achieved by splitting the multiplier into a number of exact powers of two; that is to say, dealing with each digit separately. In early serial computers it was usual to use three registers for multiplying, one of which had a single serial adder. The process was sometimes called 'halving and doubling' and was shown to one of the authors in the mid-thirties as a party trick under the name of 'Chinese multiplication'. If the multiplier is halved and the multiplicand doubled successively until the multiplier becomes unity then clearly the many times doubled multiplicand becomes the product. This can only work if the multiplier is an exact power of two but if the contents of the multiplicand or doubling register be added to a third product register, every time the multiplier or halving register contains an odd number the correct product is produced. Consider the process of multiplying 9 by 13 (see Table 1).

Table 1

Contents of multiplier register	Contents of multiplicand register	Contents of product register
13	9	0
6	18	9
3	36	9
1	72	45
0	—	117

† Griffiths, J. W. R. and Tomlinson, M., 'An electronically programmable shift register', *The Radio and Electronic Engineer*, **37**, No. 4, pp. 209–11, April 1970.



	1,	2,	4,	8,	16,	32,	64		
Pulse train at A	1	0	0	1				=	9
Pulse train at B	0	0	1	0	0	1		=	36
Pulse train at C	0	0	0	1	0	0	1	=	72
Pulse train at D	1	0	1	0	1	1	1	=	117

$9 \times 13 = 117$

Fig. 1. Schematic for multiplying a pulse train by 13.

This process, which successfully mystified children at a party, is easily explained in terms of the normal rules of multiplication for binary numbers. It lent itself very well to serial computing devices, especially where the registers were acoustic delay lines and access to the number was only possible at one point. The disadvantage was the time taken. The product was not available until after as many word times as there were binary digits in the multiplier. In processing serial numbers where the time for dealing with a word is necessarily longer than in parallel operations this disadvantage is particularly strong and a reasonably cheap method of multiplying in the same sort of time as adding is required. At first it appears that a very large number of delay stages are required. Figure 1 shows a system of multiplying serial pulse trains by 13 where the delays and additions are carried out in parallel instead of successively as in the doubling–halving system. The pulse trains show a train of pulses illustrating the operation by multiplying 9 by 13. All the pulse trains are written with the least significant digit on the *left* so that they correspond with the waveforms as they would be seen on a normal oscilloscope. Figure 2 shows how this system can be generalized for any multiplier. The AND-gates are controlled by the digits of the multiplier.

2.1 *Floating Point Multiplication*

As the example of Fig. 1 shows, a pulse train of n digits multiplied by a multiplier of m digits produces a product pulse train of $m+n$ digits. The least significant digit is produced at the same time as the least significant digit of the multiplicand arrives at the input. The most significant digit is produced m digit periods after the most significant digit of the multiplier arrives at the input. In most cases we are interested in the most significant part of the product and the systems can only handle pulse trains of a fixed length n. The product is therefore delayed by m digits and has m superfluous digits. These extra digits are frequently removed by gating and their existence ignored. This does not introduce any great error when the product is a large number but the error can be important when a system is set to follow a form of operations with many different multiplicands, some of which may be quite small. One method of avoiding these troubles is to use a 'floating point' system where all numbers are arranged in a standard form and a multiplying index of a power of two is calculated and stored in association with the number. This system has many advantages but is not appropriate to the device we are considering which is best discussed in fixed point terms.

In 'fixed point' systems some method other than truncation is usually adopted to deal with the superfluous product digits. The processes are generally called 'round-off'.

2.2 *Round-off*

The most usual method of dealing with 'round-off' is to add one digit into the most significant place of the superfluous digits and then truncate. It is easier to consider the process if we regard the truncated part as 'fractions' and the final train as 'whole numbers'. This may not be the case but the principle is always the same. A digit in the most significant part of the 'fractions' part represents $\frac{1}{2}$. If the fractions are less than a half there is no change in the 'whole number'. However, if the 'fractions' are greater than a half, the 'whole number' is increased by one.

This system is good enough for most purposes but there are occasions when the product is accumulated (for instance in an integration process) and an error can accumulate.

One method of avoiding cumulative error is to store the truncated 'fractions' part and add them to the 'fraction' part of the next product. A sum of the 'whole numbers' is therefore never more than '1' in error. Usually there is difficulty in storing the 'fractions' and in this case cumulative errors can be avoided by adding a random sequence to the 'fraction' part of the product before truncation. The effect is most easily understood by considering 'round-off' for one place of decimals. The analogous situation here is adding at random some number between 0 and 9 to the first place of decimals. On average a 'carry' will be generated into the 'whole number' position at a frequency proportional to the 'fraction'. For example, if the first place of decimals contained a 3, then three out of ten times a 'carry' would be produced into the 'whole number' position. It would probably not be acceptable to use the same random sequence for all multipliers in a large machine but having produced one random sequence it is easy to produce another by delaying the first by one digit period.

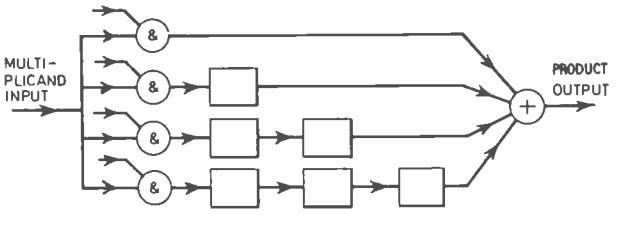


Fig. 2. Schematic for generalized multiplier.

All these methods have one common feature. They require provision in the multiplier for adding in an extra number to the product before truncation. In serial arithmetic devices this is a very low cost feature to realize. Normally the sequence generators and gating waveforms can be shared between many multipliers in a large system.

3 Programmable Shift Register Multiplier

The multiplier shown in Fig. 2 can be simplified to reduce the number of delay stages used and to substitute many 'add' units with two inputs for the one unit with many inputs. In practice the hardware content of the add units would be about the same so that savings on delay units are not in any way offset. Figure 3 shows the arrangement. The gates are controlled by the multiplier digits as before but the delay routes are shared between the digits, reducing the delay stages to a minimum.

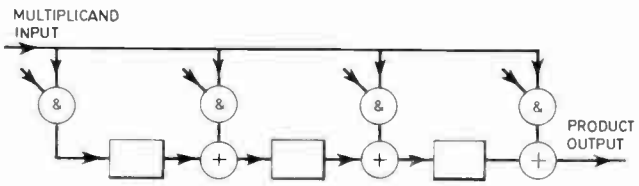


Fig. 3. Alternative generalized multiplier.

3.1 *Register Configuration*

Up to this stage the device has been identical to the device described by Griffiths and Tomlinson which uses non-carry or modulo-two arithmetic. The add units considered here will produce 'carrys'. The rules for a two-input binary adder (often called a half adder) are

0 + 0 gives 0 and no carry
1 + 0 „ 1 „ „ „
0 + 1 „ 1 „ „ „
1 + 1 „ 0 „ carry

The usual form of adder in serial arithmetic systems delays the 'carry' output pulse and adds it to the input pulse train with another half adder. The 'carry' outputs of both adders supply one delay stage through an OR-gate. Both half adders cannot produce a 'carry' output simultaneously since if the first one produces a 'carry' it must also produce a zero normal output so that the second cannot produce a 'carry' (see Fig. 4).

Frequently the two 'half adders' are combined into a 'full adder' which has three inputs (two normal, one for carry) a normal output and a 'carry' output. This may be used for serial addition in conjunction with a delay stage as shown in Fig. 5.

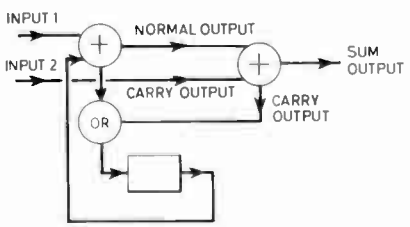


Fig. 4. A serial binary adder.

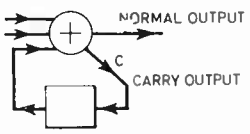


Fig. 5. Full adder for serial arithmetic.

In the multiplier the delay stages may be combined with the shift register stages as shown in Fig. 6. Also in Fig. 6 is shown the control shift register which holds the multiplier. The multiplier register is static during the multiplication process so that there is no need in principle for it to be a shift register. However, a shift register can be loaded via one input under the control of one clock input and therefore has the advantage of few connexions so necessary for integrated circuit realization.

Table 2 indicates the pulse trains which would result at the various points marked if the multiplier register

Table 2

		1	2	4	8	16	32	64	128
		2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7
	a	1	0	0	1	0	0	0	0
$2^3 = 8$	b	1	1	1	1	1	1	1	1
	c	1	0	0	1	0	0	0	0
	d	0	0	0	0	0	0	0	0
	e	1	0	0	1	0	0	0	0
$2^2 = 4$	f	1	1	1	1	1	1	1	1
	h	1	0	0	1	0	0	0	0
	j	0	1	0	0	1	0	0	0
	k	0	0	0	0	0	0	0	0
	l	1	1	0	1	1	0	0	0
$2^1 = 2$	m	0	0	0	0	0	0	0	0
	n	0	0	0	0	0	0	0	0
	o	0	1	1	0	1	1	0	0
	p	0	0	0	1	0	0	0	0
	q	0	1	1	1	1	1	0	0
$2^0 = 1$	r	1	1	1	1	1	1	1	1
	s	1	0	0	1	0	0	0	0
	t	0	0	1	1	1	1	1	0
	u	1	0	1	0	1	1	1	0

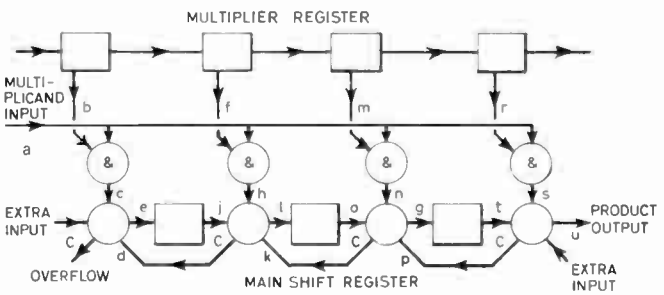


Fig. 6. The programmable shift register multiplier.

held the binary equivalent of 13 and the input stream represented 9. Once again the digit streams are written with the least significant digit leading.

Additional inputs and outputs are shown so that the devices could be joined together to form double length registers. The extra inputs could also be used for adding in round-off quantities. The extra output could be used as a product overflow indicator.

The number of connexions required for the device would be made up as follows:

power supplies, say	2 connexions
main register clock	1 „
multiplier register clock	1 „
multiplier input	1 „
multiplicand input	1 „
product output	1 „
minimum total	7 connexions

To increase the versatility of the unit additional connexions would be needed:

extra inputs	2 connexions
overflow carry output	1 „
multiplier register output	1 „
	4 connexions

grand total 4 + 7 = 11 connexions

This total will not be increased for any length of register so that a comparatively long register might be built as a single integrated circuit. A few further control connexions would not be impracticable.

3.2 *Operating Speed*

The speed at which the device would work is governed by the type of construction used. However, it is clear that the limit will be reached when a 'long carry' fails to reach the first adder in time (a 'long carry' is the condition when a 'carry' is generated in the least significant position which, in turn, generates 'carrys' at each stage until the most significant digit position). For a given technology the upper limit of operating frequency would be inversely proportional to the length of the register. This fact might limit the optimum length of register that should be produced for general application.

3.3 *Negative Numbers*

To be useful for general purposes a multiplier must deal with negative numbers. There are several conventions for dealing with negative numbers in binary computing systems. The most convenient one for the purposes of addition is to represent the number $-a$ by the binary equivalent of 2^n-a, where n is the number of binary digits in a word. Positive numbers must then be restricted to less than $2^{n-1}-1$. A digit in the most significant position then indicates a negative quantity. In the programmable shift register described, negative numbers would be dealt with correctly providing that the products were restricted to between $2^{n-1}-1$ and -2^{n-1}. Unfortunately we find that 'double length' products are necessary in most applications and considerable modifications to the device would be required.

The method used in the practical device that was tested was to change the convention for representing negative numbers. In the convention used, a negative number was represented in exactly the same way as a positive number except that a '1' was placed in the most significant digit position. In other words, $-a$ was represented as $2^{n-1}+a$. Once again numbers must be restricted, in this case to the range $\pm(2^{n-1}-1)$.

Besides being simple to implement, this convention has the advantage that the multiplicand input is always zero during the second part of a double length operation and so the multiplier could be shifted out and changed from the multiplier shift register during this time. Before choosing a final design for a programmable shift register it would be necessary to decide which convention of signs would be the most convenient for the entire system. The convention just described is admirable for multiplication but produces problems for addition.

4 Construction of Model

4.1 *Multiplier Design*

The model was designed around the 74 series of transistor-transistor-logic (TTL) integrated circuits due to their relatively high speed of operation, low cost and availability at the time. Figure 6 shows the form of the basic multiplier without gating for negative numbers, truncation or round-off. It can be seen that two shift register elements, a full adder and a two-input AND gate were required for each stage of the basic multiplier. Dual D-type flip-flops were used for the shift register elements whilst quad full adders were shared over four stages. The quad full adders were used since these contain four full adders with the 'carry lines' already connected internally and thus gave much lower propagation time for the 'ripple carry' than could have been obtained using less complex integrated circuits to build the adders. The quad full adder schematic is shown as Fig. 7. This required a multiplier which was some multiple of four stages in length and an eight stage was tested.

AND gates were achieved by using NOR gates with the inverted outputs of the multiplier register and having an invertor on the multiplicand input. This invertor would need to be a power gate to be capable of driving the many NOR gates in a large multiplier.

More complex integrated circuits could have been used in the model, such as the eight-bit shift register for use in the multiplier register and hex D-type flip-flops in the main register. Such integrated circuits would have reduced the size and interconnexion complexity of the model but at the time these were prohibited by cost.

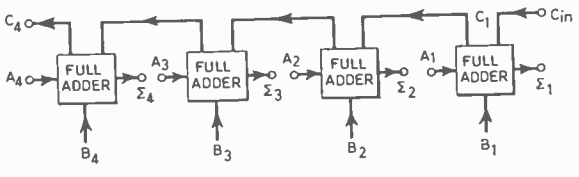


Fig. 7. Quad full adder.

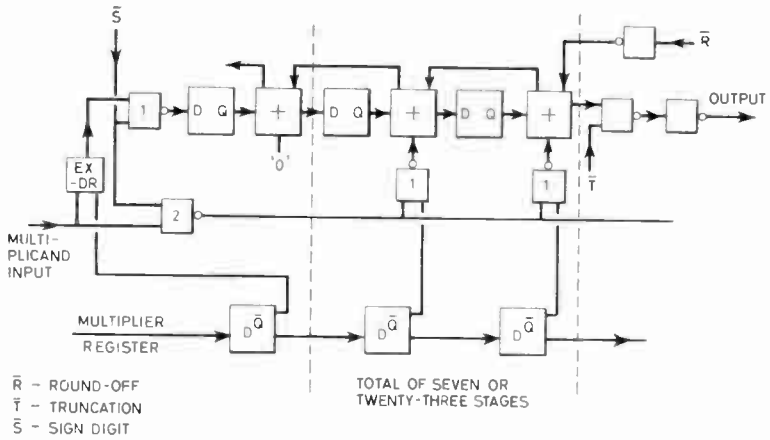


Fig. 8. Model programmable shift register.

Truncation was achieved by simple gating of the product output whilst for 'round-off' the extra input on the output full adder allowed for any technique such as a random sequence or a single pulse, as previously described, to be added to the least significant half of the product. The convention used for negative numbers required only recognition of the sign digits and implantation of the appropriate resulting sign, i.e. positive × negative = negative, negative × negative = positive, etc., which is an EX-OR function when using '0' for positive and '1' for negative.

The resultant device is shown in Fig. 8. Necessary control pulses were obtained from the test equipment for the negative number, truncation and round-off gating, the gates being chosen so that the basic multiplier would still operate with the control inputs unconnected, i.e. open circuited.

4.2 *Performance*

A multiplier with eight stages only was built and tested due to a cost limitation of the model and test equipment.

So that the product answer could be viewed on an ordinary oscilloscope, the test equipment repetitively generated any selected eight-digit serial binary number (seven plus sign digit) followed by an eight pulse zero. This generated number was the multiplicand, the multiplier having been loaded manually into the multiplier register via the available clear and preset inputs of each flip-flop instead of serially as would be required in the larger complete device.

The least significant half of the product output appears simultaneously with the inputting of the multiplicand and the most significant half during the eight-pulse zero period. With a normal oscilloscope the stream of digits was viewed with the least significant digit on the LEFT.

It was assumed that the only timing problem would be due to the propagation of the 'ripple carry' through the main register, i.e. the carry pulse not reaching the most significant full adder before the arrival of the next multiplicand digit. However, it became apparent that the timing of the clock and multiplicand digit edges was critical in order to prevent spurious outputs at the output full adder. Similarly, the timing of the control pulses for truncation, etc., had to be exact.

When all these had been corrected and the supply rails suitably decoupled to minimize the voltage spikes, the model was tested successfully up to a clock rate of 10 MHz which was the limit of the test equipment.

Due to a typical propagation time of 30 ns over four stages of ripple carry, a theoretical limit or around 16 MHz exists for the eight-stage device and a limit around 5 MHz for a twenty-four-stage device. Thus a complete multiplication of twenty-four bits times twenty-four bits including loading the multiplier register ought to be possible within 20 μs using TTL.

4.3 *High-speed Operation*

For a high operating speed TTL or even better ECL (emitter coupled logic) needs to be used but at the same time due to the large number of elements in the device it would be helpful to have the packing density offered by metal oxide semiconductors for large scale integration. M.o.s. would however present problems with the ripple-carry propagation time due to its slower switching speeds. Collector diffusion isolation (c.d.i.) would be a solution as it offers TTL operation at m.o.s. densities. On a printed circuit board it was possible to rearrange gates as required for various control functions but this would not be possible if the device were encapsulated in a single integrated circuit; thus a problem exists in deciding what additional gating to provide within so that the device can readily be used in other modes.

5 Applications

The arithmetic programmable shift register, unlike the modulo-two shift register, can only multiply. The authors cannot see any way of making the programmable shift register deal with the remainders which are invariably left in practical divisions. Where there is an exact division without remainder the technique described by Griffiths and Tomlinson will work. As this case is rare and unpredictable under practical conditions it has no practical use.

The use of programmable shift register multipliers which attracted the authors' attention was as a coefficient multiplier in a computer performing the functions of an

analogue computer but where serial pulse streams representing samples replace continuous analogue signals. The speed and potential cheapness of the device make such a computer possible with very high sampling rates.

The authors expect that, if the devices were available as an integrated circuit at a reasonable price, it could be used in signal processing pulse code modulated signals. It has been suggested that it would be particularly useful for adaptive detection processes. Where both the multiplier and the multiplicand are changing continuously a pair of multipliers might be required to achieve the maximum speed.

It is probable that additional features and controls would have to be added to make an integrated circuit version useful in many applications. In particular, it would be necessary to provide connexions so that registers could be joined up to form longer registers where required.

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Adaptive logic for artificially intelligent systems

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SUMMARY

The state-of-art of adaptive logic systems consisting of memory elements is surveyed with particular reference to three recent developments. The first introduces the concept of special-purpose structures of mixtures of memory elements and fixed circuitry for the implementation of several logic functions. The second discusses techniques developed for the automatic classification of patterns by means of randomly connected combinational networks and the optimization of performance through reconnexion of the network after training. The third topic describes the use of sequential systems for the computation of global properties of binary patterns.

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1 Introduction

Digital adaptive logic circuits were first introduced in 1968.[1] A circuit of this kind is an interconnexion of memory elements (MEs). The elements have a variable logic function by virtue of the fact that their stored content determines their response to an input pattern applied at their 'address' terminals. The circuit is adaptive in the sense that it is taught to perform desired functions 'by example' rather than by algorithm. The development and applications of such devices up to 1970 were summarized in a previous publication,[2] and it is the aim of this paper to present developments in this field which have taken place since the latter date, including the most recent advances.

After brief comments on the current state of device technology and the field of 'artificial intelligence', this paper devotes its attention to applications of two kinds: single-layer combinational networks and dynamic, sequential networks. Although both types of network contain memory elements and are therefore, strictly speaking, sequential, the distinction is made to separate their functions in use (i.e. after training) when the memory content does not change.

1.1 *The Technology of Memory Elements*

Work on adaptive logic systems has always taken it for granted that memory elements would be available in integrated-circuit form. At the outset (1965) no such devices were available and an element called the SLAM (Stored Logic Adaptive Microcircuit) was developed in conjunction with industry.[3] This type of element is now totally superseded by the bit-organized integrated-circuit Random Access Memory (r.a.m.). Except for a few minor details the two types of device are identical, and the r.a.m. may be considered as the basic element of an adaptive logic circuit. However, in the rest of this paper we shall refer to these devices as MEs: memory elements. The important terminals of an ME (shown in Fig. 1) are the inputs (addresses in a r.a.m.) and the output (data-out terminal), the latter performing a logic function of the former. The system is 'trained' by the application of a pattern at the input and the transmission of the 'desired' (or exemplary) output to a 'teach' (data-in) terminal. The moment of teaching is determined by the application of a pulse to the 'teach clock' (read/write) terminal.

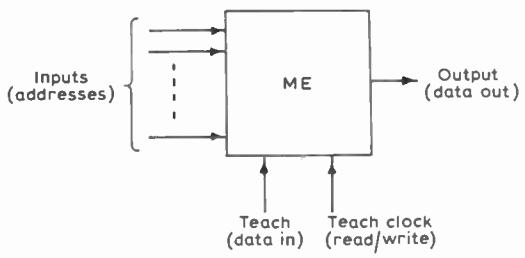


Fig. 1. The memory element.

In present day technology 11-address devices are available, while 12-address elements are at the development stage. Read and write times of the order of $\frac{1}{2}$ μs are

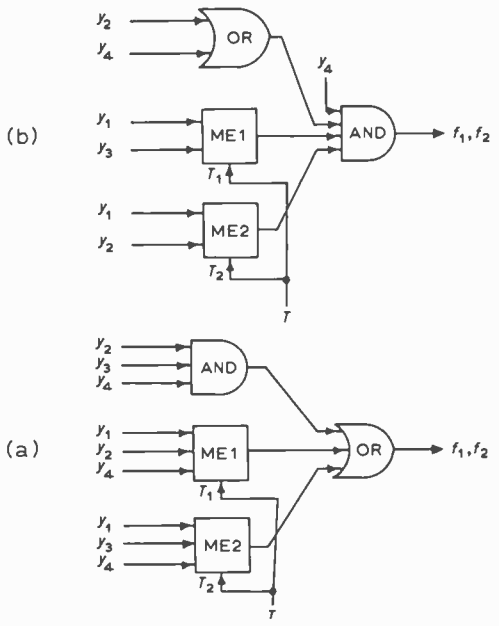


Fig. 2. Special-purpose adaptive circuits.

available for metal-oxide silicon devices. Much of the work reported here has been carried out with devices with a maximum of four address terminals. Such elements are relatively economical, making the design of adaptive logic circuits a present-day reality.

1.2 *Artificial Intelligence*

This title is generally given to the execution of computing tasks that prove to be 'difficult' for digital computers. Scene analysis, pattern recognition and robot control are the most often attempted problems in this area. Success is often hard to achieve for two fundamental reasons.[4] Even though programs may be statistical in nature they rely on exhaustive computations within the computer. This usually brings about a 'combinational explosion' of computational steps which allows one to consider only the most trivial problems even with large machines. Secondly, often programs based on numerical and linear techniques are used which fail when faced with non-linear and non-numerical tasks.

The adaptive network concept concentrates on the discovery of physical structures that, *as a basic property*, perform tasks desirable in the above fields. This is not only significant because it leads to 'buildable' machines which have some inherent artificial intelligence, but also because successful structures have successful non-numerical program counterparts.

2 Special-purpose Combinational Structures

Whereas most early work in this field has been concerned with randomly connected networks, recent effort has been devoted to the design of structures that perform a set of specific combinational tasks. Training is effected only to let the system know *which* of the tasks is required.

As an illustration of such work, consider a circuit which, at some time, has to perform the logic function:

$$f_1 = \bar{y}_1 y_2 y_4 + \bar{y}_1 y_3 y_4 + y_2 y_3 y_4,$$

and at some other time it has to perform another function:

$$f_2 = y_1 y_2 y_4 + y_2 y_3 y_4 + y_1 y_3 y_4.$$

It may be shown that the circuits in Fig. 2 can each achieve both of these two functions provided that some specific information may be entered into the MEs. In each case the fixed circuitry supplies the minterms (a) or maxterms (b) that are common to both functions. If we assume that the MEs are initially reset (i.e. they output a 0 irrespective of their input) then the systems are 'trained' by applying some patterns corresponding to the minterms of the desired functions at the inputs with a 1 at the common teach terminal T (this is called 1-training). In case (a) it may be shown[5,6] that it is merely necessary to 1-train with 0111 at the $y_1y_2y_3y_4$ terminals, respectively, to obtain f_1 or with 1111 to obtain f_2 (starting from the reset state in each case).†

Whereas, it may also be shown that circuit (b) must be trained on all four minterms of each function to perform as desired. Circuits with an output OR gate such as (a) are not always 1-trainable from a common teach wire as indicated. For example, for

$$f_3 = y_2 y_3 y_4 + \bar{y}_1 y_2 y_4 + y_1 y_3 y_4$$

there exist no suitable 1-training minterms even though the elements are potentially connected in the right way. On the other hand, it has been shown[5,6] that circuits such as (b) with an output AND gate can always be 1-trained. Converse results have also been obtained for 0-training (starting with all stores in the *set* state) and techniques for designing multi-level systems which guarantee an implementation (but do not guarantee trainability) have been developed.[6]

The trainability question is of vital importance in applications such as the design of digital learning controllers[6] which are trained by a human operator to control a dynamic system. A non-trainable system cannot accept raw 'desired output' information and consequently cannot be taught by example. Thus, only trainable systems are useful in this area of artificially intelligent machines.

3 Advances in Pattern Recognition Logic

3.1 *Automatic Recognition of Mass Spectra*

Effort has been devoted to the automatic recognition of mass spectra under an industrially-sponsored contract.[7] The first 256 mass values of the spectrum only are considered. A threshold is applied to the spectral lines and those exceeding it are mapped as 1's into a 256-bit vector while those below the threshold are mapped as 0's into the same vector. This vector is fed to a set of 28 discriminators each consisting of 64 4-input MEs. Each of the resulting 256 inputs of each discriminator is connected at random to one element of the above vector.

The object of the system is to classify spectra into 28 chemical groups (such as alkanes, primary alcohols, etc.). There is one discriminator per group. Training proceeds

† Clearly this particular problem could have been solved in many ways *not* involving MEs. Nevertheless, it was used to give a *simple* explanation of principles. More complex examples may be found in the references.

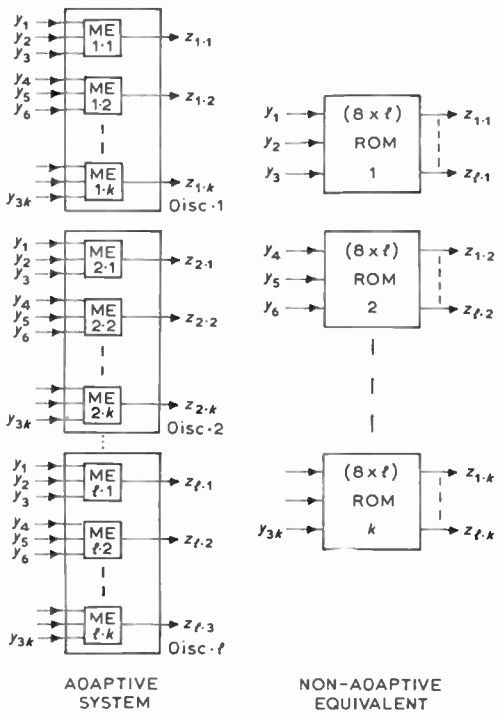


Fig. 3. ME-to-r.o.m. translation.

by the application of a known spectrum to the system and the transmission of 1's to the 'teach' inputs of all the memory elements of the appropriate discriminator. In use, the unknown spectrum is applied and classified according to the group of the discriminator with the highest response (number of output 1's).

The results of this work show that zero-error recognition may be obtained for a set of 440 spectra with about 75% training and a threshold which cuts off only those line intensities less than 1% in height of the maximum.†

Of interest in logic design is the way in which a successfully trained adaptive system of this kind may be transformed into a non-adaptive pattern recognizer composed of read-only-memories (r.o.m.s). It is seen, in Fig. 3, that the translation involves the following device changes. A k-discriminator adaptive system of n-input memory elements operating on an $(m \times n)$-bit vector, requires m r.o.m.s each word-organized to a k-bit word each having at least 2^n addresses. Thus, the above spectrum identification task could be carried out with about 256, (32×8) commercially available r.o.m.s. (Ideally, one would need 64, (16×28) r.o.m.s.)

3.2 *Connexion Optimization*

In conjunction with this work, some techniques for 'derandomizing' the discriminator connexions are being studied. These are best illustrated by referring to the following simple pattern recognition problem rather than the mass-spectrum recognizers. Assume that patterns of two basic classes appearing on a rectangular binary matrix are of interest. These patterns are either horizontal bars (Class H) or vertical bars (Class V) with a thickness of two binary elements. Consequently, there are *two* discriminators H and V. Consider three MEs each with three address inputs as shown in Fig. 4.

- ME1 has all three inputs in one horizontal line spaced by more than two binary elements.
- ME2 has two inputs connected to adjoining elements in the same horizontal line and the third input elsewhere, but further than two rows or columns from the other two.
- ME3 has its inputs scattered with more than two rows or columns between any two terminals.

Each of two discriminators contains these three MEs as described earlier. Assume that the system is trained (as described in the last section) on *all* possible 2-element-thick horizontal and vertical bars.

The following will be found on testing. For two horizontal bars ME1 in the H discriminator ($ME1_H$) will respond with a 1 while its twin ($ME1_V$) responds with a 0. This is a useful contribution towards making the correct decision. For all other horizontal bars $ME1_H$ and $ME1_V$ respond with 1's adding little to the recognition. For *six* vertical bars $ME1_V$ responds with a 1 while $ME1_H$ is at 0 which also is a useful response. We can, therefore, assign a figure of merit of 8 useful responses to the ME1 connexion. Similarly one can see that ME2 *never* responds usefully for horizontal bars but does so for two vertical bars earning a figure of merit of 2. Also, one sees that ME3 never gives a useful response.

Clearly, ME3 is a candidate for removal from both discriminators and possible reconnexion. ME2 is not quite as bad, while ME1 clearly performs a useful job.

The matter is a little more complex when more than two discriminators are used since a particular connexion may be useful for one *pair* of discriminators while it ought to be left out of others. The translation into r.o.m.s is an important characteristic of this work and the ease of translation, as in Fig. 3, is lost if discriminators have to be connected in different ways. Therefore, both methods of equal connexions and unequal connexions in discriminators are being studied. Also, techniques for assigning figures of merit and basing optimal connexions on these

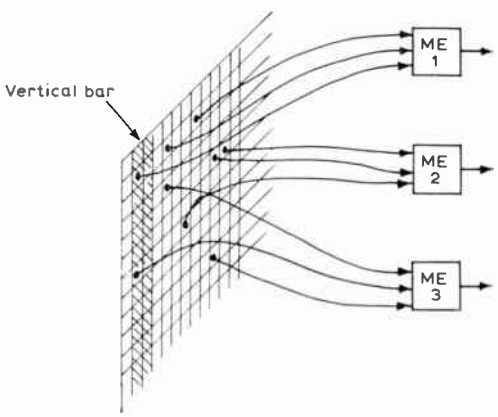
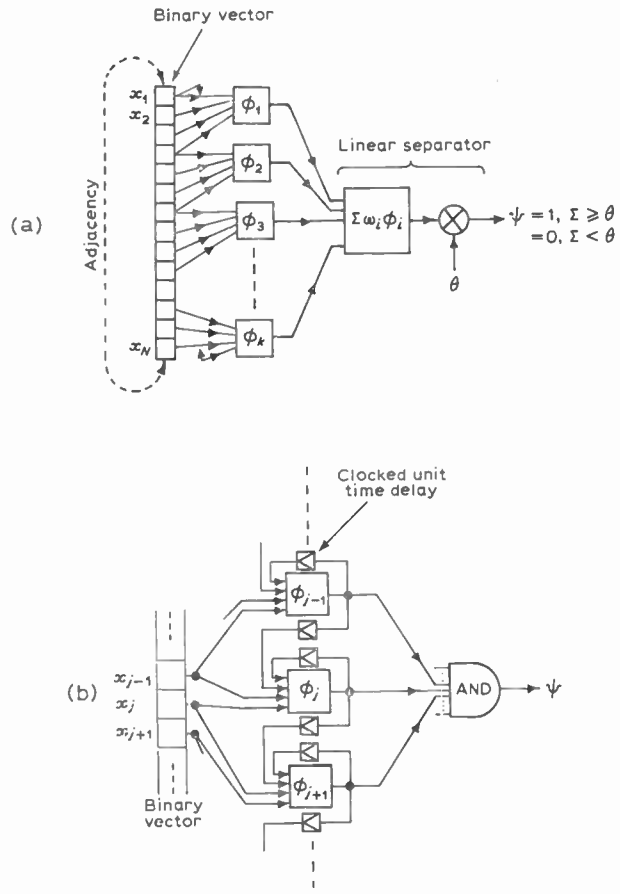


Fig. 4. Recognition of bar patterns.

† These results were obtained with a system similar to that described above, however, two discriminators were used for each chemical group.



(a) Static (no feedback) (b) Dynamic.

Fig. 5. Perceptron-like structures

figures are being researched at the present time and results will be presented in a future publication.

4 Sequential Systems

4.1 *Aims*

A sequential system implies that the networks of MES contain feedback connexions (usually assumed to be clocked). These systems have a major advantage over single-layer nets, not only in the sense that they can be sensitive to input *sequences*,[2] but also, and principally, because they have far greater discriminatory powers with respect to static input patterns. This is best seen as follows.

Imagine that two patterns differing in only one bit require a vastly different response from the system. A single-layer net can, at best, produce responses that differ in one bit at the output, as only one element is differently addressed. If a sequential system is used where the output of each element feeds one and only one input of another element and the input pattern is fed to the remaining inputs, a change of one bit in the input can, in the course of time, be propagated to all the elements and produce a maximum change in the output.

The above effect overcomes the inability of combinational networks of computing *global* properties of input patterns. This is the same defect as found in linear adaptive devices called Perceptrons.[8]

Although much work has been done in the past in showing general attributes of processing 'intelligence' in such systems[9,10,11] in this paper we shall describe one system that can compute important grobal properties of a binary vector.

4.2 *Some Global Properties of a Binary Vector*

Consider a binary vector of N bits $x_1,x_2,x_3 \ldots x_N$. We assume that the vector is circular in the sense that x_N and x_1 are *adjacent* in the same way as x_j and x_{j+1} for any j. Three global properties are defined as follows

(a) *Disparity*
The number of 1's in the vector is odd.

(b) *Uniqueness*
There is precisely one 1 in the vector.

(c) *Connectedness*
All the 1's in the vector are in adjacent bit positions and there is at least one 1.

According to Minsky and Papert,[8] a network connected to the vector is said to *compute* the predicate $\Psi_{\text{disparity}}$ (say) when its output is 1 if, and only if, the vector has the property of disparity. The 'ability to easily compute' again, according to Minsky and Papert, may be interpreted as follows, (see Fig. 5(a)). There must exist a 'layer' of K logic elements, each with less inputs than N, each of which performs a logic function ϕ_j, ($j = 1,2 \ldots K$). These functions feed a 'linear separator' which carries out the linear algebraic function

$$z = \sum_j w_j\phi_j$$

where w_j is a numerical 'weight' and ϕ_j the 0 or 1 coefficient as above. z is compared with a threshold θ and if this threshold is exceeded the predicate Ψ is defined as being *true*. This is said to be 'easily computable' because the ϕ_j computations are considered to be simple, particularly if the number of variables of each ϕ_j is low, and because the 'linear separation' is thought to be easily achieved. This is called the Perceptron structure which may be implemented both in software and hardware. In practice 'linear separations' are hard to achieve in hardware, and the system would be *easy to compute* if the $\sum_j w_j\phi_j > \theta$ operation could be replaced by one operator such as the AND (or the OR) function so that

$$\Psi = \phi_1.\phi_2 \ldots \phi_K$$
$$(\text{or } \Psi = \phi_1 + \phi_2 \ldots \phi_K).$$

This implies that a measure of 'ease of computation' is the number of inputs to each ϕ_j. In switching theory terms, a highly minimizable 2-level circuit is therefore more 'easily computed' than one which cannot be minimized. It is easily seen that properties (a), (b) and (c) all require ϕ_js with N inputs and are, therefore, not easily computed. It can also be shown that this is true for linear separators at the output. These properties are therefore only trivially within reach of Perceptron-like machines or MES. In the latter case one ME with N inputs would have to be used.

4.3 *Sequential Computation of Global Properties*

The machines described above are combinational and limited purely because, if the number of inputs of the

ϕ_js is less than N, the ϕ_js themselves have no 'knowledge' of the entire pattern. The feedback connexion as mentioned in 4.1 has the effect of making the output of each ϕ_j a function of the entire pattern *in the course of time*. To compute a global property with a sequential system of this kind it is, therefore, necessary that at some point in time *all* the ϕ_js should produce a 1 only if the input pattern has the desired property.

We will show that the system in Fig. 5(b) can compute the three predicates:

$$\Psi_{\text{disparity}},$$
$$\Psi_{\text{uniqueness}},$$
$$\Psi_{\text{connectedness}}.$$

Each ϕ_j at clock time t has the function

$$|\phi_j|_t = |f(\phi_j, \phi_{j-1}, x_j, x_{j-1})|_{t-1} \quad (1)$$

For convenience we write this as

$$|\phi_j|_t = |(\phi_j[j]\phi_{j-1})|_{t-1} \quad (2)$$

where $[j]$ is a binary function determined by the value of (x_j,x_{j-1}). To specify the operation of the system one must, therefore, specify four functions for $[j]$ one for each value of (x_j,x_{j-1}).

Since the global properties are position-invariant in the binary vector, each ϕ_j must perform the same four functions. Therefore, to prove our assertion that the system in Fig. 5(b) can compute the three desired global properties we need merely to show that there exist four functions for $[j]$ that satisfy the requirements. These can then be translated back into one function of type (1).

In general, one can develop equation (2) as follows

$$|\phi_j|_t = |((\phi_j[j]\phi_{j-1})[j](\phi_{j-1}[j-1]\phi_{j-2}))|_{t-2}$$

and so on for other, lower, values of t. It is assumed that all $|\phi_j|_{t=0} = 0$. The earliest time at which $|\phi_j|_t$ becomes a function of the entire $x_1 \ldots x_N$ vector is at $t = N$. Therefore, the existence of the four functions for $[j]$ has been sought so that at $t = N$ all ϕ_js output a 1 if and only if a pattern with the desired global property is input. The procedure for finding such functions is lengthy and consists of a tree-like search through all possible functions for a specific N. If functions are found their applicability to other values of N is checked. Details of this are considered to be beyond the scope of this paper and will be the subject of another publication.

We now consider the functions for the individual global properties.

(a) $\Psi_{\text{disparity}}$

The four functions are:

x_j	x_{j-1}	function type (2)
0	0	$\|\phi_j\|_t = \|\phi_{j-1}\|_{t-1}$
0	1	
1	0	$\|\phi_j\|_t = \|\bar{\phi}_{j-1}\|_{t-1}$
1	1	

Validity. The above functions are independent of x_{j-1} and $|\phi_j|_{t-1}$. This means that at $t = N$, $|\phi_j|_{t=N}$ is a function of the x_js and $|\phi_j|_{t=0}$. Effectively the system forms a 'ring' of N unit-time delay elements which *invert* if $x_j = 1$ and not otherwise. Thus, at $t = N$, $|\phi_j|_{t=N} = 0$ if the number of inversions is even and $|\phi_j|_{t=N} = 1$ if and only if the number of inversions is odd. This verifies the assertion and the type (1) equation for ϕ_j for $\Psi_{\text{disparity}}$ is given by:

$$|\phi_{j(\text{disparity})}|_t = |x_j\bar{\phi}_{j-1} + \bar{x}_j\phi_{j-1}|_{t-1} \quad (3)$$

(b) $\Psi_{\text{uniqueness}}$

Two sets of functions have been found which satisfy the requirements:

x_j	x_{j-1}	function type (2)
Set 1		
0	0	$\|\phi_j\|_t = \|\phi_{j-1}\|_{t-1}$
0	1	
1	0	$\|\phi_j\|_t = \|\bar{\phi}_j.\phi_{j-1}\|_{t-1}$
1	1	
Set 2		
0	0	$\|\phi_j\|_t = \|\phi_{j-1}\|_{t-1}$
0	1	
1	0	$\|\phi_j\|_t = \|\bar{\phi}_j+\bar{\phi}_{j-1}\|_{t-1}$
1	1	

Validity. This may be ascertained by evaluation of the type (2) equations at $t = 4$ and $N = 4$ (a very lengthy process even for small N). These equations are

Set 1

$$|\phi_{j(\text{uniqueness})}|_t = |\bar{x}_j.\bar{\phi}_{j-1} + x_j\bar{\phi}_j\phi_{j-1}|_{t-1} \quad (4a)$$

Set 2

$$|\phi_{j(\text{uniqueness})}|_t = |\bar{x}_j\phi_{j-1} + x_j(\bar{\phi}_j+\bar{\phi}_{j-1})|_{t-1} \quad (4b)$$

Here we merely give some typical responses at $t = 4$ for a system with $N = 4$.

				Set 1				*Set 2*			
x_1	x_2	x_3	x_4	$\|\phi_1$	ϕ_2	ϕ_3	$\phi_4\|_{t=N}$	$\|\phi_1$	ϕ_2	ϕ_3	$\phi_4\|_{t=N}$
0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1	1
1	1	0	0	0	0	0	0	1	1	0	1
1	0	1	0	0	1	0	1	0	1	0	1
1	1	1	0	1	0	1	1	0	1	1	0
1	1	1	1	0	0	0	0	0	0	0	0

It is seen that only the 'unique' input gives the all-'1' response.

These functions are not valid for all N. Indeed, one can easily show that it is *necessary* but not sufficient that N be even. Some even values of N are also not valid due to the fact that some non-unique inputs eventually and cyclically enter the 1111..1 state but not at $t = N$. For example, for $N = 4$ and set 1, 1010 enters 1111 at critical times $t_c = 2+3n, n = 0, 1, 2 \ldots$. This means that values of N *divisible* by $2+3n$ are not valid (e.g., $N = 8$, $n = 2$). An exhaustive computation has shown that the following *even* values of N between 0 and 100 are *not* valid with the above equations.

Set 1	*Set 2*
8	
14	8
20	14
24	20
26	26
32	32
38	38
44	44
48	48
50	50
56	54
62	56
64	62
68	64
74	68
80	74
84	76
86	80
92	86
98	92
	98

A detailed investigation regarding the nature of the above series is in progress at present. What is important is that the equations are valid for approximately 50% of all the possible even integer values of N up to 100. Further computations have shown that this proportion is maintained up to $N = 1000$.

(c) $\Psi_{\text{connectedness}}$

This makes use of two sets of $\Psi_{\text{uniqueness}}$ functions as follows

x_j	x_{j-1}	function type (2)
Set 1		
0	0	$\lvert\phi_j\rvert_t = \lvert\phi_{j-1}\rvert_{t-1}$
1	0	
1	1	
0	1	$\lvert\phi_j\rvert_t = \bar{\phi}_j.\phi_{j-1}\rvert_{t-1}$
Set 2		
0	0	$\lvert\phi_j\rvert_t = \lvert\phi_{j-1}\rvert_{t-1}$
1	0	
1	1	
0	1	$\lvert\phi_j\rvert_t = \lvert\bar{\phi}_j+\bar{\phi}_{j-1}\rvert_{t-1}$

Validity. The way in which the functions are arranged with respect to x_j and x_{j-1}, and from what is known of them as uniqueness detectors, it is seen that the predicate will be true if and only if there exists one and only one pair of inputs (x_j,x_{j-1}) of the form (0,1). This effectively detects the existence of the *edge* of a group of adjoining 1's in the input vector. If there is only one such edge it means that there is only one group of adjoining ones and therefore $\Psi_{\text{connectedness}}$ is computed for all values of N valid in $\Psi_{\text{uniqueness}}$. The type (1) equations are

Set 1

$$\lvert\phi_{j(\text{connectedness})}\rvert_t = \lvert(x_j+\bar{x}_{j-1})\bar{\phi}_{j-1}+(\bar{x}_j.x_{j-1})\bar{\phi}_j.\phi_{j-1}\rvert_{t-1}$$

Set 2

$$\lvert\phi_{j(\text{connectedness})}\rvert_t = \lvert(x_j+\bar{x}_{j-1})\phi_{j-1}+(\bar{x}_j.x_{j-1})(\bar{\phi}_j+\bar{\phi}_{j-1})\rvert_{t-1}$$

All that has been done in this section is to show that a system of MEs (as in Fig. 5(b)) can, at different times, compute disparity, uniqueness and connectedness. Clearly, there are trivial ways of training such a system 'off line' by direct insertion of the logic into the MEs. More sophisticated 'on-line' training techniques remain an open question and are the subject of present research.

5 Conclusions

Three recent studies in adaptive logic have been presented: (a) the application to special structures, (b) the application to the recognition of mass spectra and general circuit optimization for pattern recognition and (c) the computation of global pattern properties by means of sequential systems. The major reason for selecting these three topics amongst several others that are being studied in adaptive logic (mainly on the modelling of intelligent functions in living systems) is to make a contribution in the field of novel methods of logic design. It is hoped that the presentation of the above methods will also act as a stimulant for the imagination of others, as the commercial availability of MEs gives logic design an added dimension.

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The design of sequential logic circuits

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SUMMARY

The inadequacies of Combinational and Sequential Logic as circuit design techniques are pointed out; in particular, the Sequential Logic design technique due to Huffman has the disadvantage of leading to 'race' problems.

The work of Moore on Finite Machine Theory points the way to design based on a state graph and this technique is advocated. An illustrative example of this technique is adduced.

The case is made for the direct implementation of the state graph as a good design method and a novel logic element is proposed which is an analogue of a node on a state graph.

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1 Introduction: The Development of Sequential Logic Techniques

Combinational Logic is concerned only with logic circuits in their steady state. Since it is culled directly from Boolean Algebra it contains no considerations of time or sequence. George Boole did not postulate his algebra as an aid to circuit designers. Regrettably, Combinational Logic has advanced rather little beyond its original derivation and has many limitations: it does not, for instance, contain any major body of technique to deal with fan-in or gate delays, nor networks of more than two levels. Nevertheless, it is valuable; it is undoubtedly the best basic educational discipline for logic designers and contains the bones of an algebra which does much to facilitate logic circuit design and manipulation; but, as every practical circuit designer knows, it can only provide half the answer. This is more apparent today than it was when its techniques were pioneered; in those days logic was bulky and costly and generally designed, gate by gate, in small assemblies. Modern large logic assemblies have far outgrown the techniques of the original Boolean Algebra and those derived directly from it. It is dubious if Boolean Algebra or Combinational Logic can in themselves provide an adequate basis for the techniques now required. Probably the best formal methods of design yet postulated are those of Zissos,[1] in the form of algorithms. These include, as steps in the algorithms, all the conventional techniques but they have the added power of a carefully developed strategy of design and, surely, this is proper because engineering design should follow a strategy.

Sequential Logic grew out of the deficiencies of Combinational Logic with respect to time and sequence. It was pioneered by S. H. Caldwell[2] and D. A. Huffman.[3] It was natural for these two men and their immediate successors to base their work on the existing Combinational Logic techniques since in other respects they seemed adequate. Today most of the published work on Sequential Logic, both papers and text books, follows on from the work of Caldwell and Huffman. This, like the Combinational Logic of that time, was elegant and effective when applied to circuits and networks that today would be regarded as trivially small. It does not lend itself to the solution of practical problems of present day magnitude. It is a sad reflection that a large proportion of most books on Sequential Logic is devoted to ingenious work on how to detect and eliminate 'races' between bistable outputs. It is regrettable since these do not arise out of the problem itself but out of the method of solution. This method, due to Huffman, had the prime aim of reducing the number of secondary state *bistables* required; it was never shown that a minimal implementation arose from having the minimum number of bistables. In fact many examples are found to contradict this assumption.

At about the same time that Huffman was working at MIT, E. F. Moore was studying Automata Theory at Princeton. Moore's paper, 'Gedanken-experiments on sequential machines'[4] is a classic. In it he postulates valuable theorems on sequential 'machines' which, since 'machines' merely mean 'things that work', cover also sequential circuits. Mealy, of Bell Telephone, replied to

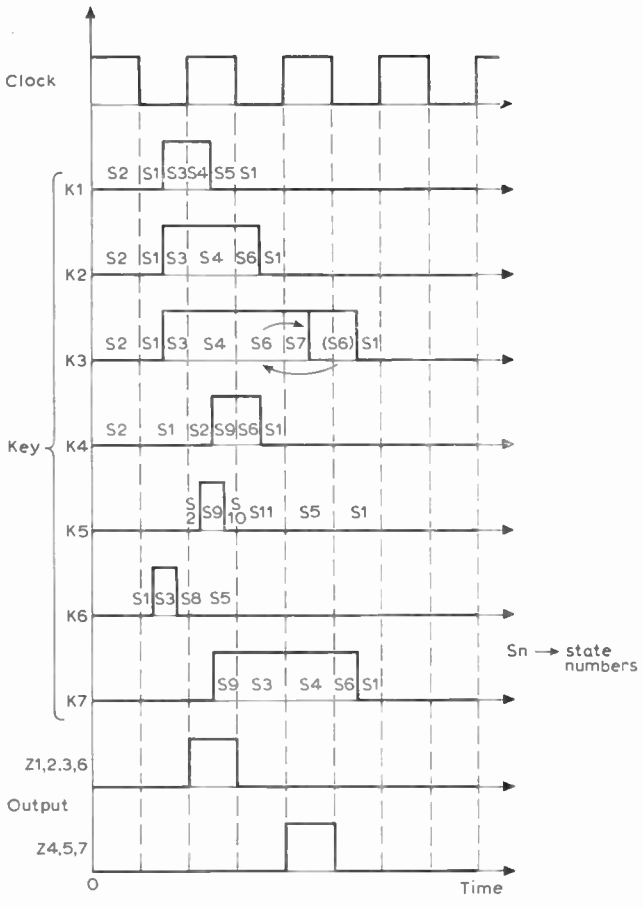

Fig. 1. 'One shot' timing diagram showing possible 'key' pulses and durations. Restriction: 'key' pulses no more often than 'clock' pulses.

Moore and extended some of his ideas in his paper 'A method of synthesizing sequential circuits'.[5] Both Moore and Mealy used a state graph to describe the sequential nature of their circuits or 'machines'. (Figure 4 shows an example of a state graph.) The 'rings' are called 'nodes', the transition lines 'arrows'; if a transition is shown as a loop, starting and ending on the same node, it is called a 'sling'.

2 The Description of a Sequential Circuit

A sequential circuit specification generally starts with a verbal description of what it does; for instance it is much easier to describe a shift register or counter or one-shot switch in words than as a mathematical formulation. Since a sequential circuit, by definition, follows a sequence of actions, the next stage in the specification is to explore the sequence, or sequences, that it is to follow and to list its actions against the steps or stages of each sequence. This can be done more or less equally easily by means of a state graph[4,5] or a flow table.[3] Suppose we consider a design problem, that of the 'one-shot' circuit. First we write down the verbal specification:

The network has two inputs C and K and one output. A square clock wave is applied to C; whenever a logic 1 is applied to K a single complete pulse of the square wave is emitted from the output.

This is necessarily a sequential circuit and certain problems are immediately apparent. If K goes to 1 while the square wave on C is 'down' then the following 'up' period, or pulse, of C is transmitted, but only one. If K goes to 1 while the clock pulse is up then it must be the next clock pulse that must be emitted since the 'present' one would be curtailed. There is no stipulation on the duration of the level applied to K; it might go up and down in the gap between clock pulses, or within a clock pulse, or stay up for many pulse times. Generally the conditions of circuit operation can be stipulated and this may well simplify the problem. It may be that the design permits the use of 'spikes' obtained from differentiation of pulse edges. In the general case no stipulations exist. We thus have to take all possibilities into account.

From the verbal description in this case we proceed to the 'timing diagram' shown in Fig. 1, or we go straight to the state graph. In this example the state graph is a complicated one and it pays instead to use a 'primitive flow table' as in Fig. 2. It will be seen that there are eleven possible states the system can assume; the state graph, if drawn, would have eleven interconnected nodes and it would be difficult to extract much useful information from it. The flow table is a useful complement to the state graph. It is of the same form as the 'crossbar chart' much loved by process plant engineers and others. It has the great advantage that every possibility must be examined to fill it in completely.

Moore's interests lay in Finite Automata Theory, which is a branch of mathematics, and it is well documented and contains some useful theorems; a number of these are concerned with reducing complex machines to simpler ones, particularly by removal of redundancy. This reduction means the reduction of the number of states; it must be noted that this reduction is of *states* and not bistables. Huffman's methods are aimed not only at reducing states in the first place but bistables as well and herein lies the weakness of his form of Sequential Logic.

	$\bar{K}\bar{C}$	$\bar{K}C$	KC	$K\bar{C}$	Z
S1	(1)	2	–	3	0
S2	1	(2)	9	–	0
S3	8	–	4	(3)	0
S4	–	5	(4)	6	1
S5	1	(5)	4	–	1
S6	1	–	7	(6)	0
S7	–	2	(7)	6	0
S8	(8)	5	–	3	0
S9	–	10	(9)	3	0
S10	11	(10)	9	–	0
S11	(11)	5	–	3	0

Fig. 2. Primitive flow table for ' one shot '.

		$\bar{K}\bar{C}$	$\bar{K}C$	KC	$K\bar{C}$	Z
(S1,S2)	S1	1	1	4	2	0
(S3,S8,S11)	S2	2	5	5	2	0
(S6,S7)	S3	1	1	3	3	0
(S9,S10)	S4	2	4	4	2	0
(S4,S5)	S5	1	5	5	3	1

Fig. 3. Reduced flow table showing critical races.

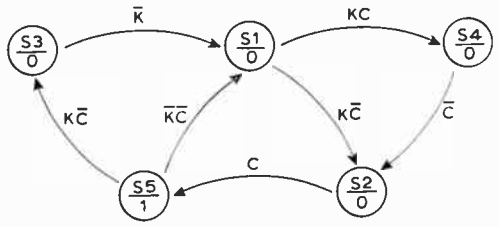

Fig. 4. State graph of 'one shot' circuit. Each node represents one of the five states and under the state number is shown the output of the circuit while in that state. This is a 'Moore machine' state graph. A 'Mealy' graph appends the outputs to the labels on the transitions.

Application of state reduction theorems to the primitive flow table of Fig. 2 leads to the reduced flow table of Fig. 3 and the state graph of Fig. 4. It now remains to implement the circuit from the state graph and this process is not easy to make into an algorithm. Huffman's method was to assign a binary code to each state of the system and to use a set of bistables to 'remember' the state assignment; that is, the states of the bistables indicate and control the state of the system. In this example since we have five states we need three bistables and we have discretion as to how we may assign them. Assignment methods form a major part of Sequential Logic texts since it is in this process of coding and assigning that 'races' are introduced. Consider our system in State 1, receiving the input combination $K = 1$; $C = 1$. The next state of the system is State 4. Suppose we had coded the states directly, say from zero to four in binary code; then starting in State 1 the bistables would all be reset, that is, at 000. Transition to State 4 would entail changing the bistable combination to 011, entailing the simultaneous change of two of them. Bistables being what they are, they would not in general change exactly simultaneously and in the transition would pass through or stick in states 001 or 010, both of which are in this case unwanted states and the system would malfunction. If care is taken with the assignment, often the numbering of states can be so arranged that no races occur over the *required* transitions of the system. If such a good assignment is not possible then there are a range of artifices which are possible, delays in setting the bistables, delaying the effect of their outputs or adding extra bistables. All this is amply covered in texts on Sequential Logic design.[6,7] But let us consider the practical aspects. In this problem, if we allocate one bistable to each state there can be no race problems and we need five instead of a minimum possible of three. In these days of cheap hardware for logic the cost of two bistables can easily be outweighed by advantages in simplicity, reliability, maintainability, design time or similar considerations. In a large system of many states this argument is manifestly harder to justify. But the design of a larger system is essentially a piecemeal job: the human designer cannot cope with complexity above a certain level. Thus a large system must generally be designed by partitioning it into smaller sub-systems; the concept of building a computer by supplying all the ingredients and parameters to a computer program and getting out the complete system in one mixing and baking is not really a good one. Even if it were possible the finished product would probably be incomprehensible to a human and would hardly inspire confidence.

If the concept of partitioning is accepted, then the state graph approach becomes preferable to the flow table or matrix approach. For a state graph has the quality that each of its nodes can represent a sub-system and the problem can be examined successively through coarse grain to fine. A whole computer may start as a state graph of three or four nodes, representing major states. These can be dissected or synthesized from smaller components piecemeal. The state graph interconnexions then define the interface signals and channels between the sub-systems.

3 Implementation from the State Graph

The state graph contains the essence of the sequential circuit and its abstract topology. The implementation is not constrained any more than it must be and this allows the designer the maximum freedom in the choice of devices to be used in the implementation. Generally, the problem of implementation reduces to the design of a transition mechanism from state to state as a result of the inputs to the system. Often, when such a mechanism has been designed once it can be used for all the transitions. There is one important point to note, however: a transition involves setting a new state but it also involves resetting and turning off the previous one. In a clocked or synchronous system this is usually a simple automatic process; in an asynchronous system it can be complicated. Typical of this technique are a set of circuit examples cited by Peatman,[8] using J K bistables and simple gating. These circuits are, in effect, node analogues in a network which is the analogue of the state graph.

The state graph has the virtue not only of being simple but also of being interdisciplinary. It is basic to the work on Finite Automata and logic design but it is also used widely in the fields of behavioural sciences, linguistics, operational research and management. Since it is a description of a sequential 'machine' in the widest sense and since the automation of 'machines' of all kinds is nowadays implemented by electronics, it seems good sense to design a logic element system which is as close as possible to being the exact analogue of the state graph. Work with this object has been carried out by the author, at Reading University with SRC support, over the past three years and a number of logic elements that are 'node analogues' have been designed. The obviously desirable properties of such an element are that it represents a node on the state graph, connected by wires to other nodes, in one-to-one correspondence

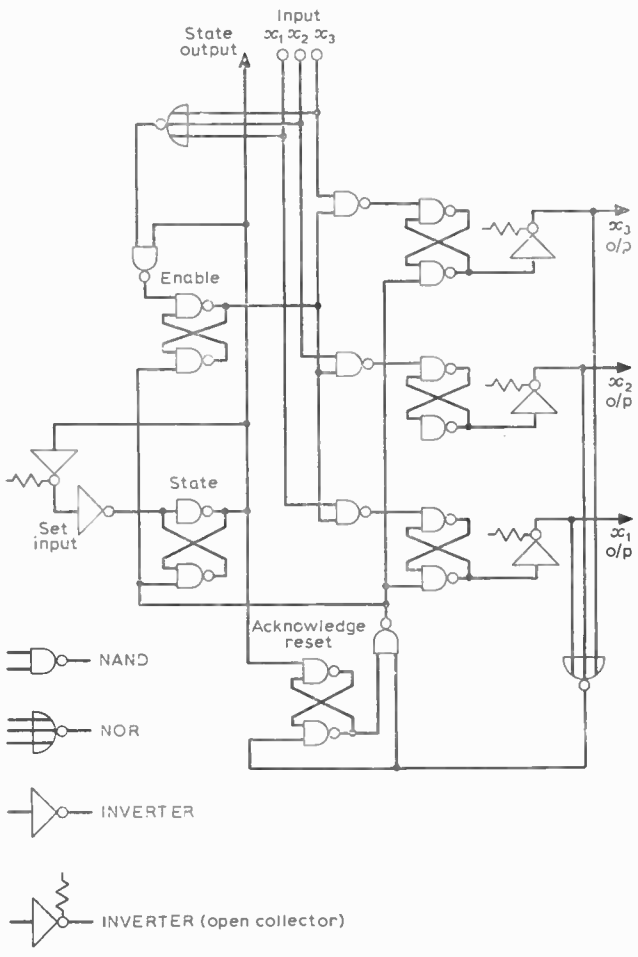

Fig. 5. TTL node element.

with the state graph arrows, and it indicates or 'remembers' the state of the represented system at any moment. On the face of it, these requirements can be fairly easily met; the element needs to be a bistable, to indicate its 'set' state; in the 'set' state it needs to be able to send, or route, setting signals to other nodes on receipt of the appropriate input signals. It also needs to become 'reset' when the state transition has been achieved. The circuits described by Peatman are manifestly capable of all these actions. On a state graph there is only one 'wire' from each state to the next; for a true analogue, a reset wire is undesirable, thus the node elements designed at Reading use a duplex system, that is, set and reset take place on the same wire. There are other considerations that are not so obvious, for instance the problem of 'ripple through'. Figure 5 shows the circuit of a node element implemented in transistor-transistor logic (TTL); it is somewhat more complicated than would be expected at first consideration. The following description of its operation indicates the reason for this complication.

4 A TTL Node Element

In the reset condition all inputs and outputs are at logic 0. A logic 1 on the input sets the 'state' bistable. The output of this going to logic 1 causes the input terminal to be pulled down to logic 0, by the open collector inverter directly connected to it. This arrangement allows the preceding node element to determine the status of its following element; it 'sees' a 0 when it sends its setting level, which takes the input terminal to 1. As soon as the receiving node becomes set, this 1 is taken off so that the setting node again 'sees' a zero. The 'acknowledge reset' bistable is used to detect this; when any output of the sending node goes to 1, this bistable becomes set, through the common NOR gate. When the output is pulled down to 0 (the 'acknowledgment' or 'hand-shake'), a reset signal is gated through the NAND gate, resetting the 'state' bistable, which in turn resets the 'acknowledge reset' bistable.

The 'enable' bistable serves to prevent any 'ripple through' malfunction. It can only be set by the 'state' bistable when all the input signal channels x_1 to x_3 are at 0. Thus if any input channel is active when the node is set it waits until the channel goes to zero before enabling the output. If it were not for this arrangement the system would respond in the same way to the two different sequences of inputs a–b–c and a–b–b–c.

In Finite Machine Theory we say that *if in a certain state the 'machine' receives a certain input* then it changes state in some defined way. The situation must not exist such that the machine changes state and an input is already there on the succeeding state. The reason for this is that if the input signal is already there then it must have entered the machine in some previous state and should have been dealt with in that state: if it was ignored then the machine does not 'respond' to that signal in that state and this should be specified as part of the requirement. The element illustrated conforms to this rule. If it is in fact required to cope with input signals that already exist they can be conveniently gated in under control of 'state output'.

The node element as illustrated is too complicated to be an economical proposition when built of discrete components or standard chips. As an element on a single chip or fabricated in arrays on m.s.i., for interconnexion by metal masking, it could make sequential design quick and almost foolproof. A circuit built of these elements would have the great advantages that it is already designed once the state graph is designed, and that the circuit could be easily understood by anyone who understood its function, without any particular competence in electronics.

5 Conclusion

Sequential Logic, like Combinational Logic, has not yet been developed as a complete design tool. There are techniques for doing all aspects of the design of sequential circuits but they are not all good ones and do not fit all circumstances. In the design, say, of a microcircuit on which the cost of a great deal of design time can be justified, in order to get an ultimately minimal configuration, then the complicated techniques of Sequential Logic may well be effective. They should be studied because they give a great deal of insight into the nature of sequential circuits.

For the general requirement of sequential circuit design the better approach is to use the state graph and

the relevant theorems of Finite Automata Theory. From the minimized state graph the designer should use his skill as an electronics designer or, if available, a specially designed element which implements the state graph as directly as possible.

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The Institution awards a prize for the most outstanding apprentice obtaining the highest aggregate marks in all subjects in each Entry at No. 1 Radio School, Royal Air Force, Locking. The prize for the 119th Entry has been won by Technician Apprentice J. R. Cruikshank who during his training gained an Ordinary National Certificate with four distinctions; he also received prizes given by the Royal Aeronautical Society and the Borough of Weston-super-Mare for the highest marks in technical and educational subjects, respectively.

The Engineer in Parliament

Parliament needs the advice and support of scientists and engineers, said Mr. Airey Neave, MP, at a lecture sponsored by the Thames Valley Local Committee of CEI on 9th November. Mr. Neave, who is Chairman of the Parliamentary Select Committee on Science and Technology, was speaking on 'Science and Technology and Parliament' before an audience of some 150 at Reading University. In outlining the role of his committee over the whole field of science and technology, Mr. Neave referred to its investigations into areas such as nuclear power, computers, high-speed transport and Government research and development policy. 'The value of this all-party committee', he said, 'is that we can get technical information not available to others, and being all-party it of course carries much more weight with Parliament.' It was important, he continued, to see that the Government was given the right advice on technical matters and he was concerned to see that they, in fact, received it. 'There should be a careful check on all future projects to see that they are commercially viable. With the EEC we are bound to get involved in bigger and bigger projects and it is important to see that these are correctly evaluated.'

In the discussion that followed, Mr. M. W. Leonard, Secretary of CEI, said that engineers welcomed the interest shown by Parliament in engineering and scientific matters. CEI and its Constituent Members supported the Parliamentary and Scientific Committee (a non-Party body formed with the object of providing a permanent liaison between scientific bodies and Parliament) which has become the centre for the consideration and discussion of scientific information bearing on current proceedings in Parliament. Chartered engineers were well represented amongst the officers of the Committee, and the IERE has been associated with the P&SC since its formation over 25 years ago.

Forum on Terotechnology

'We are beginning to succeed in putting across the message and I would like to congratulate Sir Leonard Atkinson and his Committee on Terotechnology on their work in this respect,' said Mr. Christopher Chataway, Minister for Industrial Development. Mr. Chataway was addressing a Forum on Terotechnology in London on 6th November at which Sir Leonard—CEI's Vice-Chairman and President of the IERE in 1968–70—took the chair.

'Today,' Mr. Chataway continued, 'plant and equipment are rarely the product of one discipline. The mechanical engineer needs to know something of electrical engineering and vice-versa as well as something of hydraulics and pneumatics. But it is not just the engineers who are concerned. All who are involved in the decision-making process, not least the accountant and others whose task is to advise management, must be deeply concerned. As yet, no attempt has been made to quantify the total cost to this country of the failure to appreciate the benefits to be derived from the application of terotechnological practices but it must be several times the figure produced by the original maintenance engineering survey.'

The concept of Terotechnology grew out of the survey on maintenance engineering published in 1970 which indicated that enormous savings could be achieved—£550M a year in the private sector alone—if industry paid more attention to plant maintenance.

Design Education

The best way of maintaining and creating a future supply of designers who understand the principles of engineering and of engineers who appreciate design concepts was the broad theme for discussion at a recent dinner given by CEI for the Design Council and the Society of Industrial Artists and Designers. The dinner was attended by nearly 80 leading engineering and design representatives, and was preceded by a session, under the chairmanship of Sir Angus Paton, at which three speakers briefly covered different aspects of engineering design. Professor Sir Misha Black, Professor of Industrial Design (Engineering), Royal College of Art, spoke on the importance of design as a concept; Mr. Hugh Conway, C.Eng., emphasized the engineering considerations involved; and Dr. A. H. Chilver, C.Eng., Vice Chancellor, Cranfield Institute of Technology, covered the question of design education.

Mr. Conway, who backed his points with slides showing well-designed and efficient products, said: 'We have tended to over-glamourize scientific research. We now need to get on and design better products. If we spent a small percentage of the money now being used for scientific research and used it for engineering design, we would be a great deal better off.'

Sir Paul Reilly, Director of the Design Council, summed up by suggesting that the Design Council and CEI might set up a working party 'to watch what is happening in designing as a whole'. Perhaps 1975/6 should be a Design Education Year, he continued, to give prominence to some of the matters raised during the wide-ranging discussion.

European Consultants Meeting

The International Association of Experts—INTER-EXPERT— recently met in Luxembourg when delegates from many countries of Europe discussed in great detail the standardardization of Consultancy procedure and the composition of Arbitration Tribunals within the European Community. Great Britain was represented by Mr. George R. Pontzen (Fellow), formerly with Lustraphone Ltd., and now an international consultant on electronics. The meeting established that Western European countries generally are not sufficiently informed about the potentialities and knowledge offered by experts in many fields. Information about Inter-Expert may be obtained from Mr. Pontzen whose address is 146 Elizabeth Avenue, Little Chalfont, Amersham, Buckinghamshire MP6 6RG, or from Union Internationale d'Experts, Pavillon Le Lys, Rue Charles Gounod, 67380 Strasbourg-Lingolsheim, France.

The End of the Physics Exhibition

It has been decided by the Council of The Institute of Physics that the Physics Exhibition should be discontinued. The next exhibition provisionally arranged for 1975 will not therefore take place. The exhibition was first held by The Physical Society in 1905, the last one in 1973 was the fifty-seventh in the series. A variety of venues in London were used including Imperial College, the Royal Horticultural Halls, Alexandra Palace, and, finally, Earls Court.

In recent years the number of exhibitors, particularly industrial firms, has fallen substantially as has the number of visitors. This gives confirmation of a widely held belief that generalized scientific exhibitions lacking a unifying theme are unattractive to both exhibitors and visitors. The considerable knowledge and expertise in the exhibition field which exists in the Institute will now be concentrated on smaller specialized exhibitions, largely held in conjunction with the Institute's extensive programme of conferences.

Trends in On-line Computer Control Systems

Organized by the Control and Automation Division of the Institution of Electrical Engineers in association with the IERE, the Institute of Mathematics and its Applications, the Institute of Measurement and Control, the Institute of Physics and the Institution of Chemical Engineers, this Conference will be held at the University of Sheffield from the 22nd to the 24th April 1975. Residential accommodation will be available at Ranmoor House, University of Sheffield.

The aim of the Conference is to present and highlight developments in control computers and their applications since the previous conference on this subject, held in April 1972. The Conference will provide an opportunity to identify new developments in both equipment and application areas, and thereby will interest equipment suppliers, systems analysts and end users.

Among the subject areas which it is intended to cover are:

The effect of large scale integration on central processing units, storage and peripherals.

Hardware microprogramming, intelligent peripherals and virtual storage.

The use of mini and special-purpose computer systems as control devices, including data concentrators and remote plant data multiplexers.

Interface systems and data links.

Solid state multiplexers and data highways.

Operator communication including use of visual display units, data input and control panels.

Systems arrangement including hierarchical and multi-processor computer configurations with special reference to inter-computer communication and dynamic task assignment, and high integrity computer systems including failure survival and self-diagnostic systems.

High level and interactive language developments.

The use of software simulator and host computers for program assembly and test.

Operating systems and real time executives.

Applications, with special reference to commissioning techniques, test specifications, off- and on-line testing and the measurement of system success and reliability, drawn from a wide variety of fields, such as: utilities systems; transport systems; marine applications; automated warehouses; laboratory automation.

The IERE representative on the Conference Organizing Committee is Mr. S. L. H. Clarke, B.A.(Fellow).

The Organizing Committee invite offers of contributions of not more than 2000–4000 words (8 A4 pages). It is the Committee's intention that this material should be published as interim papers for distribution prior to the Conference and that authors may provide additional material (2 A4 pages) at the Conference to up-date their work. Synopses of approximately 250 words should be submitted on or before 1st May 1974. A synopsis should include all the main points of the paper and, where possible, indicate where the emphasis will be placed and in which areas there are likely to be further developments which can be reported nearer the time of the Conference. The full typescripts for advance publication will be required for assessment by 1st November 1974.

Registration forms and further programme details will be available a few months before the event from the IEE Conference Department, Savoy Place, London WC2R 0BL, to which offers of papers should be sent.

Dinner of Council and Committees

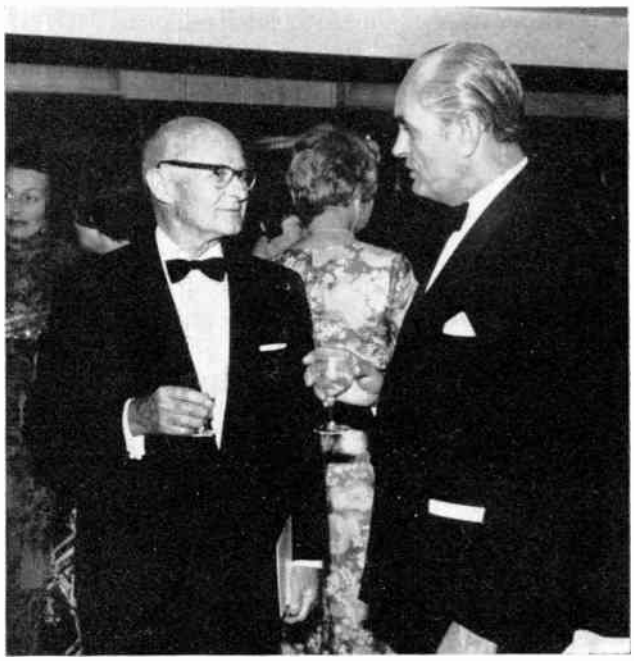
Savoy Hotel, London, 21st November 1973

The Institution's traditional Dinner at which the Immediate Past President and his lady are the guests of honour, was held under the chairmanship of Dr. Ieuan Maddock, F.R.S. Mr. and Mrs. A. A. Dyson were welcomed by the President who in his speech referred to his distinguished predecessor's service on the Council and its Committees since 1950. Dr. Maddock also proposed the Toast of the Guests, and said how very welcome ladies were at this particular occasion.

The President and Immediate Past President and their ladies wait to greet members and their guests.

The President and Mrs. Maddock with Mr. and Mrs. Denis Heightman.

The President then called upon Mr. Harvey Schwarz (Past President) to make presentations to Mr. and Mrs. Dyson on behalf of the Institution. In his own tribute Mr. Schwarz recalled that throughout his professional life Mr. Dyson had been concerned with the making of components—the little things that made big things work. He had also been active in promoting the exchange of technical ideas between this country and America, and as an American who had worked in Britain for 40 years, Mr. Schwarz welcomed the opportunity of saluting a professional colleague who was British by birth and had done much to promote good Anglo-American relationships.



During the reception Mr. Harvey Schwarz (Past President) talks with Dr. Percy Allaway (Vice President).

Mr. Schwarz then presented to Mrs. Dyson a painting of Berney Arms Mill by Stanley Orchard, a Norfolk artist, and to Mr. Dyson a small electronic calculator.

Replying, Mr. Dyson referred to the international character of the Institution and to some of the events during his period of office. He had particularly enjoyed the opportunity to visit several of the local sections as well as the many occasions on which he had represented the Institution at functions all over the country. The last two years had not been easy for the Institution but its many problems and increasing growth had been met by the cooperation which existed between members of Standing Committees and of the staff.

The evening was rounded off by a programme of songs from light opera and musical comedy.

Mr. Dyson replies to the Toast as Guest of Honour.

The Institution's Solicitor, Mr. Gray Hill, and Mr. and Mrs. George Taylor examine the guest list.

Past President Professor Emrys Williams is welcomed.

Obituary

The Council of the Institution has learned with regret of the deaths of the following members.

William George Gough (Member 1939) died on 30th May 1973, aged 76 years. He leaves a widow.

Mr. Gough received his early academic training at the Victoria Institute, Worcester, and during the first World War was trained as a Wireless Operator at the RAF Wireless School, Flowerdown. In 1930, after three years of part-time radio experimental work, he joined County Magneto, Worcester, as Assistant Manager of the Radio Service Department and was appointed Manager in 1935. During this period he wrote several articles for 'World Radio', notably on interference and early push-button domestic radio receivers.

In June 1941 Mr. Gough joined the BBC as a Maintenance Engineer at Wood Norton and was transferred as an Engineer in 1945 to Birmingham where he continued to serve until 1961 when he retired to live in Brixham.

William Arthur Penton (Member 1938) died in October last aged 62 years. He leaves a widow.

One of the Institution's first members in New Zealand, Mr. Penton spent the early years of his professional life in broadcasting. He joined the Auckland station of the Radio Broadcasting Company in 1928 and subsequently moved to the New Zealand Broadcasting Service where he was Station Engineer at Christchurch. After war service as a Lieutenant with the Royal Australian Navy Volunteer Reserve, he was appointed a radio and radar engineer with the New Zealand Department of Scientific and Industrial Research's Dominion Physical Laboratory, now known as the Physics and Engineering Laboratory, at Lower Hutt near Wellington. At the time of his premature retirement in February 1971 due to ill health originating from a war-time disability, Mr. Penton was a Senior Technical Officer.

The formation of the Wellington Section in 1946 was due in no small part to Mr. Penton's efforts. He was especially active in gaining recognition for the Institution by New Zealand Government departments.

Members' Appointments

NEW YEAR HONOURS

The Council has congratulated the following members of the Institution, whose names appear in Her Majesty's New Year Honours List, published on 1st January 1974.

Appointment to the Most Honourable Order of the Bath

AS AN ORDINARY MEMBER OF THE MILITARY DIVISION OF THE THIRD CLASS OR COMPANION (C.B.)

Rear Admiral Sir Peter Anson, Bt. (Fellow 1972)

Admiral Anson is Assistant Chief of the Defence Staff (Signals). He was promoted to Rear Admiral in July 1972 and his previous recent appointments include that of Commanding Officer of HM Signal School (HMS *Mercury*).

Appointments to the Most Excellent Order of the British Empire

AS AN ORDINARY COMMANDER OF THE CIVIL DIVISION (C.B.E.)

Timothy Arthur Cross (Fellow 1942)

Mr. Cross is Executive Vice-Chairman of Redifon Limited and a director of Rediffusion Limited. He has been with the Group for the whole of his professional career and, before appointment as Managing Director of Redifon in 1962, had been closely concerned with wire broadcasting and cable television developments in this country, Trinidad and Canada. He served on the Institution's Council from 1965 to 1968 and on the Finance Committee from 1964 to 1969.

AS ORDINARY OFFICERS OF THE MILITARY DIVISION (O.B.E.)

Lieutenant Colonel Gordon Arthur William Hickman, Royal Signals (Member 1965)

Prior to taking up his present appointment with the Signals Division of the Northern Army Group, Colonel Hickman was Officer Commanding, Trade Training School, 8th Signal Regiment at Catterick Camp.

Commander Ronald Walter Nickson, RN (Member 1966)

Commander Nickson is Director of Fleet Work Study and Management Services; before taking up this appointment in 1968 he was Air Engineer Officer at RN Air Station, Yeovilton.

AS AN ORDINARY OFFICER OF THE CIVIL DIVISION (O.B.E.)

John Stuart Sansom (Member 1959, Graduate 1954)

Mr. Sansom has been Technical Controller of Thames Television Ltd. since 1970; he was previously Chief Engineer of ABC Television.

AS AN ORDINARY MEMBER OF THE CIVIL DIVISION (M.B.E.)

Austin Egley (Member 1970)

Mr. Egley has been on the staff of the Sheffield Regional Hospital Board since 1956 and since 1969 he has held the post of Assistant Regional Engineer.

CORPORATE MEMBERS

Professor H. E. M. Barlow, D.Sc., F.R.S. (Honorary Fellow 1971) was elected to the Honorary Membership of the Japanese Society of Electronics and Communications Engineers (JSECE), during a recent tour of Japan. This is the first time that anyone from the United Kingdom has been so honoured, and in fact Professor Barlow is now the only living Honorary Member of the Society in Europe. The honour recognizes Professor Barlow's great contribution to microwave techniques and for the help he has given in translations for the Society and in the training of many Japanese students.

Professor Barlow has been a member of the IERE Council since 1972 and he represents the Institution on the Council for Environmental Science and Engineering.

Mr. R. I. T. Falkner (Fellow 1960, Member 1946) has been elected President of the Business Equipment Trade Association for the current year. Mr. Falkner is Managing Director of the Sperry Remington Division of Sperry Rand Limited.

Mr. E. W. J. Satchell (Fellow 1973) has been appointed Director of Engineering (Ships) in the Procurement Executive of the Ministry of Defence. Since graduating from the Royal Naval College, Greenwich, in 1939, he has been concerned with electrical installations in HM Ships as a member of the Royal Naval Engineering Service, and he was appointed Deputy Director of Engineering in 1970.

Mr. C. G. Beetham (Member 1972) has been granted three years' leave of absence from the Science Research Council's Daresbury Laboratory in order to supervise the timing system of the Super Proton Synchrotron at CERN, Geneva. He has been with the Laboratory since 1968 and holds the rank of Higher Scientific Officer.

Mr. W. S. Black (Member 1963, Graduate 1955) is now a Senior Design Engineer with Plessey Radar at Cowes, Isle of Wight. He was previously an Experimental Officer at the Atomic Energy Research Establishment.

Sqn. Ldr. J. L. Critchlow, RAF (Member 1971) has completed a course at the RAF Staff College and has taken up the appointment of Officer Commanding Ground Radio Installations Squadron with the Radio Installations Unit at RAF Henlow.

Wing Cdr. J. P. Downs, RAF (Member 1966, Graduate 1961) has been appointed to the staff of the Director of Engineering Policy, Ministry of Defence; since April 1972 he has been Officer Commanding Engineering Unit at RAF Marham.

Mr. R. C. Duffield (Member 1971, Graduate 1964) has been appointed Works Director of Grundy and Partners Limited, Stonehouse, Gloucestershire. He was previously with Marconi Space & Defence Systems Limited, Portsmouth, latterly as Quality Manager.

Dr. A. G. J. Holt (Member 1959, Graduate 1953) has been appointed to a Professorship in Electrical Engineering in the Department of Electrical and Electronic Engineering at the University of Newcastle Upon Tyne. Professor Holt went to the then King's College, University of Durham in 1957, after completing the Diploma Course in Electronics at the University of Southampton. He gained his Doctorate in 1957 for an investigation of methods for detecting small periodic changes in circuit conductance. His main teaching and research interests are in circuit and system studies, computer aided design and thin film devices; he has made a number of contributions in these fields, and is the author of numerous papers in the Institution's *Journal*.

Professor Holt is a member of the Components and Circuits Group Committee and of the North Eastern Section Committee.

Mr. C. H. J. Jones (Member 1969, Associate 1965) has been appointed to the Corporate Staff of the Plessey Company as Manpower Manager, Technology and Graduate Recruitment, and is based at Ilford. He was previously Manpower Manager, Research, with Plessey Telecommunications at Taplow. Mr. Jones is a member of the Education and Training Committee and was the Institution's Membership Officer from 1962 to 1967, prior to joining the Plessey Company.

Dr. C. A. F. Joslin, M.B., B.S. (Member 1955, Graduate 1950), who has been on the staff of the South Wales and Monmouthshire Radio Therapy Service at Velindre Hospital, Cardiff, since 1967, and is a clinical teacher in the Welsh National School of Medicine, has been appointed to the Chair of Radio Therapy at the University of Leeds; he will take up his appointment in May. Dr. Joslin was a member of the Medical and Biological Electronics Group Committee from its formation in 1959 until 1970 and was Chairman from 1963 to 1969. He served on the Council from 1967 to 1969.

Mr. Bernard O'Brien (Member 1966) has been appointed Engineer in Charge (Television) in the Educational Technology Unit of the University of the Witwatersrand, Johannesburg. He was previously Senior Television Engineer with Uganda Television which he joined in 1967 after working with the Independent Television Authority as Senior Maintenance Engineer.

Forthcoming Institution Meetings

London Meetings

Wednesday, 20th February

AEROSPACE, MARITIME AND MILITARY SYSTEMS GROUP

A Novel Radar Situation Display

By A. Harrison (*Kelvin Hughes*)

IERE Lecture Room, 6 p.m. (Tea 5.30 p.m.)

The use of an optical storage medium capable of retaining a radar picture for periods up to 15 or 30 minutes has led to the achievement of a mode of display of radar data on a moving ship, originally suggested many years ago but never successfully carried out. A simple ship's head-up relative display is optically projected on the image retaining panel, which is viewed by a closed-circuit television system. The panel is moved electro-mechanically to correspond to the ship's movements as indicated by log and gyro. The unique combination of electronic, optical, and electromagnetic techniques has produced a radar display with properties of real daylight viewing by more than one person, and the indication of position, course, and speed of other ships, in a manner extremely cost effective and operationally very attractive. Extracts from recordings of sea voyages will be shown.

Thursday, 21st February

JOINT IEE/IERE MEDICAL AND BIOLOGICAL ELECTRONICS GROUP

Colloquium on PHYSICAL TECHNIQUES IN BIOLOGICAL RESEARCH

IEE, Savoy Place, 2 p.m.

Further details and registration forms from the IEE, Savoy Place, WC2R 0BL

Tuesday, 26th February

JOINT MEETING WITH THE IEE AND RTS

The Long Playing Video Disk

By Dr. P. Kramer (*Philips, Eindhoven*)

IEE, Savoy Place, 5.30 p.m. (Tea 5 p.m.)

Tuesday, 26th February

JOINT IEE/IERE MEDICAL AND BIOLOGICAL ELECTRONICS GROUP AND IMPI-EUROPE

Discussion meeting—

The Measurement of Electromagnetic Radiation Hazards and their Biological Effects

IEE, Savoy Place, 2.15 p.m.

Wednesday, 27th February

COMMUNICATIONS GROUP

Data Communications—The Next Ten Years

By P. T. F. Kelly (*Post Office Telecommunications*)

IERE Lecture Room, 6 p.m. (Tea 5.30 p.m.)

Data communications is now just over 10 years old and there are now over 30 000 data terminals in the UK making use of data transmission facilities. Information is being obtained on likely growth patterns, data signalling rates requirement, and data traffic patterns, in order to assist in the planning of future Datel services. The next ten years could see the introduction of new point to point, multipoint and switched digital data services, perhaps initially on an experimental basis.

Wednesday, 6th March

EDUCATION AND TRAINING GROUP

The Future of Part-Time Study for Professional Engineers

Speaker to be announced

IERE Lecture Room, 6 p.m. (Tea 5.30 p.m.)

Wednesday, 13th March

AEROSPACE, MARITIME AND MILITARY SYSTEMS GROUP

New Displays for Old Radar

By T. W. Welch (*T. W. Welch and Partners*)

IERE Lecture Room, 6 p.m. (Tea 5.30 p.m.)

In 1970, following operational and feasibility studies, it was decided to begin the development of a Civil Air Traffic Control Radar Service by the employment of an up-to-date data extraction, transmission and display system to present, for the time being, information derived from an existing secondary radar system, operated by a different agency from the ATC Authority, at a land-line distance of some 35 miles. A supply contract was effected in 1971 and the display system was installed and commissioned in the summer of 1972. This paper discusses various interference design problems encountered before, during and since the installation and commissioning of the system and the solution found effective for each. The topics discussed include protection of the existing radar system from fault conditions in the new equipment, early difficulties encountered in passing data over the existing telephone circuits, malfunctions caused by harmonic content in the selsyn azimuth data and by departures from specification of the video output of the original radar and some s.s.r. siting lessons learned from the results obtained.

Friday, 15th March

JOINT IEE/IERE MEDICAL AND BIOLOGICAL ELECTRONICS GROUP

Some Recent Developments in Medical Ultrasonic Diagnostics

By Professor P. N. T. Wells (*Welsh National School of Medicine*)

IEE, Savoy Place, 5.30 p.m. (Tea 5 p.m.)

Wednesday, 20th March

JOINT MEETING WITH IEE

Colloquium on TELECOMMUNICATIONS TEST—Philosophy of Test and Maintenance Equipment in the Next Five Years for use in Telephone Systems

IEE, Savoy Place, 10.30 a.m.

Apply for further details and registration forms to IEE, Savoy Place, WC2R 0BL

Wednesday, 20th March

COMMUNICATIONS GROUP

Global Communications

MEETING POSTPONED

Wednesday, 27th March

AUTOMATION AND CONTROL SYSTEMS GROUP

The Engineering Approach to CAD of Avionic Control Systems

By P. J. Burt (*Marconi-Elliott Avionic Systems*)

IERE Lecture Room, 6 p.m. (Tea 5.30 p.m.)

Friday, 29th March

JOINT IEE/IERE COMPUTER GROUP

Colloquium on INFORMATION STRUCTURES AND STORE ORGANIZATION

IEE, Savoy Place.

Further details and registration forms from IEE, Savoy Place, WC2R 0BL

Kent Section

Thursday, 28th February

Multiphonic Organs

Lecture by J. H. Asbery

Demonstration by M. Knight

Lecture Theatre 18, Medway and Maidstone College of Technology, Chatham, Kent, 7 p.m.

The principle of the multimonophonic organ (usually abbreviated to multiphonic) involves the use of a small number of oscillators, the frequency of these being determined according to the keys pressed. Attention will be drawn to the relative advantages of a.c. resistive, a.c. capacitive and d.c. keyboard switching and to systems using the divider principle. Aperiodic frequency multipliers may be used as an alternative to dividers. Tone forming by use of non-linear elements and modulation of one footage by another will be mentioned. Some of the techniques can be used where a conventional melodic section is provided in a polyphonic organ. While the concept of the multiphonic organ is over a quarter of a century old, its commercial exploitation has hitherto been inhibited by lack of inexpensive components of sufficient stability.

Thursday, 21st March

ANNUAL GENERAL MEETING at 7 p.m.

Followed by

Modern Railway Signalling Systems

By R. M. Bell and P. M. Flook (*British Rail*)

Lecture Theatre 18, Medway and Maidstone College of Technology, Maidstone Road, Chatham.

The feature of the lecture is an hour-long sound film, made by the authors, 'First of

the Thirteen', and is a documentary of the British Rail, Southern Region North Kent Lines resignalling scheme. The introduction will describe the events leading up to the scheme, the making of the film and Southern Region's 'Thirteen signal box plan'. After the film the present London Bridge resignalling scheme will be introduced briefly, pointing out the similarities and variations with the North Kent scheme, together with novel features at present being developed. The presentation is the basis for a future lecture on the use of electronics on the London Bridge scheme.

Thames Valley Section

Thursday, 14th February

Mini Computers—Wherever Next?

By M. Judd (*Data General*)

J. J. Thomson Physical Laboratory, University of Reading, Whiteknights Park, Reading, 7.30 p.m.

A critical review of the development of mini-computers covering the main technological advances which have brought about the current range of machines will be given. Extrapolation of present trends in both hardware and software will be given to predict the architecture of the next generation of machines, with particular emphasis on new applications.

Thursday, 14th March

Recent Advances in Radio Navigation

By J. E. Viles (*Marconi Avionic Systems*)

J. J. Thomson Physical Laboratory, University of Reading, Whiteknights Park, Reading, 7.30 p.m.

A general survey will be given of new navigational aids such as Omega and aircraft microwave landing systems and the integration of aids in area navigation and mixed systems, with reference to some modern techniques which have helped these advances in the airborne equipment field.

Thursday, 4th April

ANNUAL GENERAL MEETING at 7 p.m.

Followed by **C-MOS and its Applications**

By W. G. Saich (*National Semiconductors UK*)

J. J. Thomson Physical Laboratory, University of Reading, Whiteknights Park, Reading.

East Anglian Section

Wednesday, 13th February

JOINT MEETING WITH IEE

Digital Measurement of Television Waveforms

By R. Vivian (*IBA*)

Ipswich Civic College, 6.30 p.m. (Tea 6 p.m.)

The ability of an equipment of channel to transmit faithfully a video signal appearing at its input terminal may be investigated in many ways. One of the most obvious would be to apply audio testing techniques and plot amplitude and phase responses against frequency.

However, the results of this simple if tedious process cannot always be related easily to subjective assessments of visual impairments. Early attempts at resolving these difficulties resulted in the practice of supplementing the frequency domain information with transient response curves, but as the applied waveforms often contain frequency components outside the normal passband, the interpretation was still not as straightforward as might have been supposed originally.

Further efforts to improve the correlation between measured and subjective degradations focused attention on measurements in the time domain, using waveforms whose frequency distributions were well defined. Much of the success in quantifying measurements made according to this technique has been due to the work of Dr. N. W. Lewis.

Thursday, 21st February

JOINT MEETING WITH IEE

Flight Simulators

By A. M. Spooner (*Redifon Flight Simulators*)

University Engineering Laboratories, Trumpington Street, Cambridge, 6.30 p.m. (Tea 6 p.m.).

Wednesday, 6th March

JOINT MEETING WITH IEE

Digital Computers: A Survey of the Art and Future Developments

By J. Carter (*Eastern Electricity*) and L. Forth (*University of Essex*)

The Computer Centre, University of East Anglia, Norwich, at 7 p.m.

(Refreshments served at 8 p.m.)

Southern Section

Wednesday, 13th February

Submillimetre Waves

By Professor D. Harris (*Portsmouth Polytechnic*)

Portsmouth Polytechnic, Anglesea Road, 6.30 p.m.

The wavelength from about 1 mm to 0·1 mm is now being explored. The lecture will outline the development of this region, present the state of the art so far as generation, detection and modulation devices are concerned, consider the properties of materials and the atmosphere at these wavelengths, and discuss the possibility of low-loss waveguides for submillimetre operation. Applications, including special purpose communications and image forming systems, will be discussed and possible developments outlined. A demonstration of submillimetre lasers, techniques and waveguides will be given after the lecture.

Tuesday, 19th February

Project Management in the 1970s

By R. H. Bradnam (*Urwick Technology Management*)

Bournemouth College of Technology, 7 p.m. (Refreshments in Refectory 6.30 p.m.).

The paper will describe the factors involved in setting up a 'new project', and will review current practices and procedures of project management. The problems associated with running a project will be discussed.

Thursday, 7th March

This meeting will only be held if the current fuel restrictions are terminated.

Electronic Aids to Position Fixing

By D. J. Phipps (*Decca Survey*)

South Dorset Technical College, Weymouth, 6.30 p.m.

During the past decade, we have seen a large expansion in the use of electronics for position measurement on the surface of the earth. This presentation deals with one widely accepted method of operation: namely, time shared, differential phase measurement of radio frequencies. In particular, the design philosophy, problems and engineering details that led to the development of the recently announced HIFIX/6 system.

Wednesday, 13th March

ANNUAL GENERAL MEETING at 6.30 p.m. Followed by

The History of some Major Inventions and Concepts in Electrical Communications

By Professor D. G. Tucker (*University of Birmingham*)

Lanchester Theatre, Southampton University. (Tea in Senior Common Room from 5.45 p.m.)

Many of the basic concepts in electrical communications today have a surprisingly early origin in the nineteenth century, although they were often not understood and were often misunderstood. The lecture will examine some of these origins with particular reference to ideas and methods of multiplex telephony for both line and radio, including frequency-division and time-division multiplex, and of amplitude and frequency modulations; it will conclude with a consideration of the influence of the thermionic valve and positive and negative feedback.

Wednesday, 20th March

JOINT MEETING WITH IEE

Colloquium—ENERGY IN THE 80s

Three lectures will be presented by G. N. Stone (*CEGB, Bristol*), Dr. I. Fells (*University of Newcastle Upon Tyne*) and P. T. Cast (*Shell Mex and BP*)

Registration not necessary; visitors welcome. Lanchester 'A' Lecture Theatre, Southampton University, 4 p.m.

Wednesday, 27th March

JOINT MEETING WITH IEE

Multi-channel U.H.F. Reception on Naval Ships

By H. P. Mason (*ASWE*)

HMS *Collingwood*, Fareham, 6.30 p.m.

Tuesday, 2nd April

Charge Coupled Devices

By J. D. E. Beynon (*University of Southampton*)

Brighton Technical College, Pelham Road, 6.30 p.m. (Tea in Refectory)

Although the charge-coupled device was conceived only three years ago it is already

challenging many conventional integrated circuit techniques, particularly in the memory and solid state imaging field. This is because of the device's extreme simplicity which is leading to circuits having high packed density, low power dissipation and low cost per function. The lecturer will explain the operation of the charge-coupled device and describe some of the techniques used for fabricating c.c.d. circuits. Some of the c.c.d.'s many present and future applications will be discussed.

Yorkshire Section

Thursday, 21st February

JOINT MEETING WITH IEE

Mini-Computers and Their Application

By N. Emslie (*Hewlett Packard*)

Leeds University, 7 p.m. (Refreshments 6.30 p.m.)

The first part of the presentation will explain to an engineering audience the principles of operation of mini-computers with emphasis given to the important architectural features which influence the performance of complete systems. This will be followed by a brief review of the concepts of software and comparison between scientific programming languages. Examples will be shown of the applications in engineering and science where mini-computers have made major contributions.

Thursday, 14th March

The Use of Circuit Blocks in Digital Systems

By J. M. Reid (*South Yorkshire Automatic Control Engineering*)

University of Leeds, 7 p.m. (Refreshments 6.30 p.m.)

A survey of discrete component circuit blocks available at the present time and the detailed application of one product range in an industrial system will be given. The challenge from various integrated circuit families will be discussed and probable developments outlined.

Friday, 26th April

ANNUAL GENERAL MEETING

Leeds University, 7 p.m.

West Midland Section

Thursday, 28th February

JOINT MEETING WITH IEE AND IPOEE

Low Frequency Navigational Aids

By A. Brooker-Carey (*Decca Navigator Co.*)

Post Office Training College, Stone, Staffs, 7 p.m.

Monday, 25th March

IEE MEETING

Radio Telemetry Network for the Retrieval of Seismic Signals

By Z. E. Jaworski (*City of Birmingham Polytechnic*)

M.E.B. Offices, Summer Lane, Birmingham. at 6 p.m.

Wednesday, 3rd April

ANNUAL GENERAL MEETING at 7 p.m. Followed by

Recognizing Musical Instruments

By K. A. Macfadyen (*University of Birmingham*)

The Polytechnic, Wolverhampton.

East Midland Section

Wednesday, 13th February

Opto-Electronics

Speaker from Texas Instruments

Lecture Theatre 'A', Physics Block, Leicester University, 7 p.m. (Tea 6.30 p.m.)

Tuesday, 5th March

JOINT MEETING WITH IEE

Synthesis of Digital Logic Systems using ROMs

By M. E. Woodward (*Nottingham University*)

Edward Herbert Building, Loughborough University of Technology, 7 p.m. (Tea 6.30 p.m.)

The talks will be concerned with the synthesis of combinational and segmental logic systems using r.o.m.s (Read Only Memories). Particular reference will be made to the large reduction in memory size made possible by decomposing complex systems into a number of smaller interconnected sub-systems.

Wednesday, 27th March

ANNUAL GENERAL MEETING

Leicester Polytechnic, 7.30 p.m.

South Midland Section

Tuesday, 19th February

Integrated Circuits for Radio Receivers

By J. Bryant (*Plessey Semiconductors*)

B.B.C. Club, Evesham 7.30 p.m.

Thursday, 21st March

Fibre Optic Communications

By Professor W. A. Gambling (*Southampton University*)

G.C.H.Q., Oakley, Cheltenham, 7.30 p.m.

Wednesday, 24th April

Developments in Electronics for Motor Vehicles

Speaker to be announced

To be followed by

ANNUAL GENERAL MEETING

The Foley Arms, Malvern, 7 p.m.

South Western Section

Wednesday, 27th February

JOINT MEETING WITH IEE AND RAES

Digital Instrumentation

By A. R. Owens (*University of Wales, Bangor*)

Queen's Building, University of Bristol, 6 p.m. (Tea 5.45 p.m.)

Wednesday, 20th March

JOINT MEETING WITH IEE

Aphid Numerical Control for Printed Circuit Card Layouts

By G. Skidmore (*British Aircraft Corporation*)

Lecture Room 2E3.1, University of Bath, 7 p.m. (Tea 6.45 p.m.)

Wednesday, 3rd April

Electronics in Support of the Police

Speaker to be announced

Lecture Room, 2E3.1, University of Bath, 7 p.m. (Tea 6.45 p.m.)

Monday, 6th May

ANNUAL GENERAL MEETING

The Royal Hotel, College Green, Bristol, 7 p.m.

North Eastern Section

Wednesday, 13th March

Electrical Filters

By Professor A. G. J. Holt (*University of Newcastle Upon Tyne*)

The Main Lecture Theatre, Ellison Building, Newcastle Upon Tyne Polytechnic, Ellison Place, Newcastle Upon Tyne, 6 p.m. (Refreshments in Staff Refectory 5.30 p.m.)

Wednesday, 10th April

Communication with Light

By Professor W. A. Gambling (*University of Southampton*)

Followed by ANNUAL GENERAL MEETING

The Main Lecture Theatre, Ellison Building, Newcastle Upon Tyne Polytechnic, Ellison Place, Newcastle Upon Tyne, 6 p.m. (Refreshments in Staff Refectory 5.30 p.m.)

North Western Section

Wednesday, 27th February

JOINT MEETING WITH IEE

Data Transmission—Present and Future

By Messrs. Brenton and Wright (*Post Office*)

Lecture Theatre R/H10, Renold Building, UMIST, 6.15 p.m. (Tea 5.45 p.m.)

The lecture will comprise an introduction to data transmission, a section on modem design and the prospects for future development.

Thursday, 21st March

Machine Tool Control. The Interfacing of NC to the Machine Tool

By R. W. Prew (*Plessey Numerical Controls*)

Lecture Theatre R/H10, Renold Building, UMIST, 6.15 p.m. (Tea 5.45 p.m.)

The paper will cover the evaluation of the interface from the Ferranti Mark IV equipments up to present soft wired developments.

Thursday, 9th May

ANNUAL GENERAL MEETING

Lecture Theatre R/H10, Renold Building, UMIST, 6.15 p.m. (Tea 5.45 p.m.)

Merseyside Section

Wednesday, 13th February

Digital Systems Technology: Its Influence on Modern Electronic Systems

By A. K. Porter (*Liverpool Polytechnic*)

Department of Electrical Engineering and Electronics, University of Liverpool, 7 p.m. (Tea 6.30 p.m.)

The paper appraises the revolution which has occurred in the past decade in the use of digital technology in electronic systems. Applications in instrumentation, communications, and computer technology are reviewed with an indication of trends in the development of new components and design techniques.

Wednesday, 13th March

Magnetic Bubbles and their Applications

By P. J. Banks (*Liverpool Polytechnic*)

Department of Electrical Engineering, and Electronics, University of Liverpool, 7 p.m. (Tea 6.30 p.m.)

Magnetic bubbles are cylindrical magnetic domains which are formed in films of suitable materials by applying a bias field normal to the plane of the film. The bubble domains can represent a bit of information, and thus can be used both for the storage and the manipulation of digital data. Work has been done on them by several manufacturers interested in computer applications.

An explanation of the basic requirements for the formation of bubbles will be given as well as descriptions of some of the methods proposed for generating, moving and detecting them.

Wednesday, 24th April

ANNUAL GENERAL MEETING at 7 p.m. Followed by

Wide Ranging Applications of Metal Oxide Semiconductors

By J. A. Everist (*ITT Semiconductors*)

Department of Electrical Engineering and Electronics, University of Liverpool, 7 p.m. (Tea 6.30 p.m.)

Northern Ireland Section

Wednesday, 13th February

The Ergonomics of Electronic Equipment

By G. R. Dickson

The Polytechnic, Jordanstown, 7 p.m.

Wednesday, 13th March

Megaw Memorial Lectures

The Main Lecture Theatre, Ashby Institute, 6.30 p.m.

The Megaw Memorial Award is given annually for the most outstanding paper presented at a meeting of the Institution's Northern Ireland Section by a final-year student of Electrical Engineering at the Queen's University of Belfast.

Wednesday, 3rd April

Please Note Change of Date

Making Good Television

By W. Woods (*B.B.C.*)

Cregagh Technical College, 7 p.m.

South Wales Section

Wednesday, 13th February

ANNUAL GENERAL MEETING at 6 p.m. Followed by

Electronic Music

By K. Winter (*University College, Cardiff*)

Large Shandon Lecture Theatre, University College, Cardiff.

Long before the advent of so-called electronic music, apparently non-musical sounds had been employed in various works. Today tape recorders and synthesizers have expanded the available range of sounds to such an extent that composers are no longer content with traditional orchestration. They demand an expansion of instrumental possibilities. It is this interaction between live performer and tape/synthesizer in the concert hall or on another level between composer and machine which is stimulating much new music today.

Monday, 18th March

JOINT MEETING WITH IEE

Automobile Electronics

By C. S. Rayner (*Lucas Electrical*)

Department of Applied Physics, UWIST, Cardiff, 6 p.m. (Tea in College Refectory from 5.30 p.m.)

Thursday, 11th April

JOINT MEETING WITH IEE

Quadrophonics

By K. Barker (*University of Sheffield*)

University College, Swansea, 6.15 p.m.

Scottish Section

JOINT MEETINGS WITH IEE

Concorde Electronics

By H. Hill (*BAC*)

Monday, 11th February

Room 406, James Weir Buildings, University of Strathclyde, Glasgow, 6 p.m.

Tuesday, 12th February

South of Scotland Electricity Board Showrooms, 130 George Street, Edinburgh, 6 p.m.

JOINT MEETINGS WITH IEE

Some Military Applications of Lasers

By S. Lazenby (*Ferranti*)

Wednesday, 6th March

Napier College of Science and Technology, Colinton Road, Edinburgh EH10 5DT, 7 p.m.

Thursday, 7th March

Glasgow College of Technology, Hanover Street, Glasgow, 7 p.m.

APPLICANTS FOR ELECTION AND TRANSFER *(continued from opposite page)*

OVERSEAS

CORPORATE MEMBERS

Transfer from Graduate to Member

ASHIE, Winns Major. *Accra, Ghana.*
BASSEY, David Andrew. *Calabar, Nigeria.*
BEHRENS, Roy William, Flight Lieutenant. *R.A.F. Rheindahlen, BFPO 40.*
BURTON, Roger John. *Sydney, N.S.W. Australia.*
FERGUSON, Anthony Malcolm, Flight Lieutenant. *R.A.F. Episkopl, BFPO 53.*
HOCTOR, Bernard Paul, Flight Lieutenant. *R.A.F. Luqua, Malta, BFPO 51.*
MACKENZIE, Ian James, Flight Lieutenant. *R.A.F. Episkopl, BFPO 53.*
ONUKVUBE, Lawrence Chilaka. *Enugu, Nigeria.*
POOLEY, Anthony Richard. *Quebec, Canada.*
SHAH, Khaliq Nawaz. *Ontarlo, Canada.*
SHARMA, Rejendra Kumar. *Kota 5, Rajasthan, India.*
SIMS, Michael Stroud. *Ottawa, Canada.*

Direct Election to Member

RAMSBOTTOM, Thomas Anthony, Flight Lieutenant. *R.A.F. Episkopl. BFPO 53.*

NON-CORPORATE MEMBERS

Transfer from Student to Graduate

BANDYOPADHYAY, Gayatri (Mrs). *Bangalore 1, India.*

Direct Election to Graduate

BALASUBRAMANYAM, Lakkaralli Seshanginhas. *Bangalore 22, India.*
OYEMI, Thomas Gregory. *Benln, Nigeria.*
TANG, Kwok Kwong. *Kowloon, Hong Kong.*

STUDENTS REGISTERED

FONG, Chin On. *Pahang, Kuantan, W. Malaysia.*
YING, Siew Wai. *Singapore 12.*

Notice is hereby given that the elections and transfers shown on Lists 169 and 170 have now been confirmed by the Council.

INSTITUTION OF ELECTRONIC AND RADIO ENGINEERS

Applicants for Election and Transfer

THE MEMBERSHIP COMMITTEE at its meetings on 4th and 18th December 1973 recommended to the Council the election and transfer of 95 candidates to Corporate Membership of the Institution and the election and transfer of 18 candidates to Graduateship and Associateship. In accordance with Bye-law 21, the Council has directed that the names of the following candidates shall be published under the grade of membership to which election or transfer is proposed by the Council. Any communications from Corporate Members concerning these proposed elections must be addressed by letter to the Secretary within twenty-eight days after the publication of these details.

Meeting: 4th December 1973 (Membership Approval List No. 171)

GREAT BRITAIN AND IRELAND

CORPORATE MEMBERS

Transfer from Graduate to Member

BACKHOUSE, Robert. *Cheadle, Cheshire.*
CATT, Brian Richard Lewis. *Sutton, Surrey.*
COBB, Alan George. *Ilford, Essex.*
COLE, Christopher Brian. *Cheltenham, Gloucestershire.*
HARTLEY, William. *Winchester, Hampshire.*
HENERY, Albert Briggs. *St. Heller, Jersey, Channel Islands.*
HENSON, John Anthony. *Lenton, Nottingham.*
JENKINS, Colin Henry. *Farnborough, Hampshire.*
KING, Dennis. *Burnley, Lancashire.*
KING, Donald Terence. *Sallsbury, Wiltshire.*
LAID, Christopher John Caton. *London, S.E. 25.*
LEVER, Ian Reginald. *Andover, Hampshire.*
McKAY, Graham. *Biggleswade, Bedfordshire.*
MACKINNON, Douglas Charles. *East Kilbride, Lanarkshire.*
MACSWEENEY, Seamus Joseph. *Dundrum, Dublin* 14.
MASLIN, Thomas Douglas. *Cheltenham, Gloucestershire.*
MAWBY, Roger Bernard Graeme. *Fleet, Hampshire.*
MOH, John Ifeatu. *London, S.W. 11.*
MOSS, Peter Richard. *Chipstead, Surrey.*
NEIL, William. *Teddington, Middlesex.*
NOBLE, James. *Rutherglen, Glasgow.*
NUTH, Victor Raymond. *Hayes, Middlesex.*
OXLEY, George. *Evesham, Worcestershire.*
PAIN, John George. *Chelmsford, Essex.*
PANNELL, Keith. *Ascot, Berkshire.*
PEARCE, Richard John. *Leiston, Suffolk.*
PEMBER, William John. *Waltham Abbey, Essex.*
PENDER, William Gerard. *Bromley, Kent.*
PLUNKETT, George. *Dunnington, York.*
PRICE, Barry Kenneth. *Liverpool, Lancashire.*
PUNWANI, Sunder Chandumal. *London, N.W.2.*
RABE, Arthur Guenter. *Poole, Dorset.*
REYNOLDS, George William. *Harrow, Middlesex.*
RHODES, Anthony. *Woking, Surrey.*
SMITH, David George. *Southampton, Hampshire.*
VAUDREY, Stuart. *Oldham, Lancashire.*
WASHBOURN, Leslie Henry. *Woking, Surrey.*

Direct Election to Member

COX, John Arthur. *Cardiff, Glamorgan.*
HOWELLS, Malcolm Richard, B.A., Ph.D. *Hale, Cheshire.*
KERR, Andrew. *Bishopbriggs, Glasgow.*
JONES, Anthony Glanville. *Penzance, Cornwall.*

NON-CORPORATE MEMBERS

Transfer from Student to Graduate

PENDLEBURY, Barry Keith. *Whitefield, Lancashire.*

Direct Election to Graduate

AYUB, Mohammad. *London, W.1.*
CARTER, Michael Humphrey. *Overton, Yorkshire.*
FENEMORE, Kenneth James. *Birmingham.*
MORCOM, Christopher John. *Gt. Shelford, Cambridge.*
WATSON, William. *London, W.4.*

STUDENTS REGISTERED

HEPWORTH, Lawrence. *London, S.W.13.*
CHAUDHARY, Zahid Hussain. *Bristol.*
HUME, Terence Arthur. *London, N.3.*
MERALI, Mehboob. *London, N.W.10.*
TYNDALE, Adrian James. *Mitcham, Surrey.*

OVERSEAS

CORPORATE MEMBERS

Transfer from Graduate to Member

CORNISH, John Alfred. *Wellington, New Zealand.*
MAOR, Pinchas. *Haifa, Israel.*
MEBUDE, Abiodun Hazaaz Abdul. *Lagos, Nigeria.*
ONIANWA, Agboso. *Lagos, Nigeria.*
OSHOKO, Festus Folusho. *Jos, Benue Plateau, Nigeria.*
QUADRI, Syed Peer Badshah, *Qatar, Arabian Gulf.*

NON-CORPORATE MEMBERS

Transfer from Student to Graduate

LIM, Peng Hor. *Kuala Lumpur, Malaysia.*

Direct Election to Graduate

CHEUNG, Ming Kay (Miss). *Hong Kong.*

STUDENTS REGISTERED

CHENG, Siu Ming. *Kowloon, Hong Kong.*
CHOI, Chung Hong. *Kowloon, Hong Kong.*
CHUNG, Chun Man. *Tsuen Wan, Hong Kong.*
HO, Chung Hong. *Kowloon, Hong Kong.*
KWAN, Yuk Tak. *Kowloon, Hong Kong.*
KWONG, Chung Ping. *Northpoint, Hong Kong.*
LAM, Ar Fu, Peter. *Kowloon, Hong Kong.*
LAU, Fung Chun. *Northpoint, Hong Kong.*
LAU, Hing Tung. *Kowloon, Hong Kong.*
LEE, Chun Ho. *Kowloon, Hong Kong.*
LEE, Nga Yin. *Hong Kong.*
LEE, Sai Keung. *Kowloon, Hong Kong.*
LEUNG, Fu Yee. *Hong Kong.*
LEUNG, Tai Ming. *Kowloon, Hong Kong.*
LEUNG, Wai Boon. *Kowloon, Hong Kong.*
POON, Hing Wai. *Hong Kong.*
WONG, Hon Shu. *Kowloon, Hong Kong.*
WONG, Kee Lam. *Kowloon, Hong Kong.*
WONG, Yan Kwai. *Wanchai, Hong Kong.*
YUNG, Kwok Tai. *Northpoint, Hong Kong.*
YU, Kai Wing. *Hong Kong.*

Meeting: 18th December 1973 (Membership Approval List No. 172)

GREAT BRITAIN AND IRELAND

CORPORATE MEMBERS

Transfer from Graduate to Fellow

MOODY, George Walter. *East Grinstead, Sussex.*

Transfer from Graduate to Member

AGNEW, David Skelton. *Bradford-on-Avon, Wiltshire.*
CUMMING, John. *High Wycombe, Buckinghamshire.*
FOLLAND, Edward Philip. *Bletchley, Milton Keynes.*
LIGHT, Thomas. *Walton-on-Thames, Surrey.*
LONGMAN, Brian David. *Hawarden, Deeside, Flintshire.*
MacDONALD, Alexander. *Bearsden, Glasgow,*
MANKU, Harbans Singh. *Uckfield, Sussex.*
MARIS, John Anthony. *West Drayton, Middlesex.*
MASON, Joseph. *Northallerton, Yorkshire.*
MAY, Colin Paul. *Marlow, Buckinghamshire.*
MOORE, Antony Bernard. *Pinner, Middlesex.*
MOORE, Kevin Malcolm. *Chippenham, Wiltshire.*
MORTLEY, Robert Anthony. *Chatham, Kent.*
MUNROE, Rodney Arthur. *Rayleigh, Essex.*
OLSSON, Geoffrey Peter. *Basingstoke, Hampshire.*
PIPER, Stephen George. *Cowes, Isle of Wight.*
PLANT, Robert John. *Maidenhead, Berkshire.*
POWERS, Ian Edward. *Upton, Wirral.*
PRICE, Nigel Francis, Flight Lieutenant. *Tattershall, Lincoln.*
PYNE, Roger Michael. *Southampton, Hampshire.*
ROLPH, Denis Dumas. *Marlow, Buckinghamshire.*
SAUNDERS, Anthony. *Plymouth, Devon.*
SCOTT, Ronald James Alexander. *Hitchin, Hertfordshire.*
SCOTT, Stephen Anthony. *Bedford, Bedfordshire.*
SEABURNE-MAY, Jerome Roger. *Portsmouth, Hampshire.*
SHARP, David Walter. *Hoddesdon, Hertfordshire.*
SHARPE, Brian Allan John. *Ryde, Isle of Wight.*
SHARPE, Paul Roger. *Broxted, Essex.*
SHAWO, Gilbert. *Ilford, Essex.*
SHAND, David Ian. *Poole, Dorset.*
SKINNER, Richard Lee Hayward. *Binley, Coventry.*

Direct Election to Member

GOVE, George Yule. *Weymouth, Dorset.*
LEFEVER, James Charles. *Ongar, Essex.*
SANDS, Martin, Commander R.N. *London, S.E.10.*

NON-CORPORATE MEMBERS

Transfer from Student to Graduate

DAINTY, Stephen Frank. *Leigh, Lancashire.*

Direct Election to Graduate.

AHMED, Shafiq, B.Sc. *London, N.15.*
BHATTI, Muhammad Yaqub. *Slough, Buckinghamshire.*
CORNER, Geoffrey Seddon. *Farnborough, Hampshire.*
MERRELL, David, Squadron Leader, B.Sc. *High Wycombe, Buckinghamshire.*
SWINN, Christopher James, B.Sc. *Moseley, Birmingham* 13.

STUDENTS REGISTERED

JIBOWU, Olubunmi Mofo. *Roath Park, Cardiff.*
LEE, Dominic Savid Kin-Ip. *Birmingham.*
LILLEY, Robert Mark. *Guildford, Surrey.*
MAX-MACARTHY, William Ekundayo. *Bolton, Lancashire.*
OVERTON, Gary Charles. *Loughborough, Leicestershire.*
SHAW, Patrick Frank. *Desford, Leicester.*
SWAILE, Henry Barry. *London, N.9.*
YOUNG, Derek Ronald. *Rickmansworth, Hertfordshire.*
YOUNGMAN, Stephen Nicholas. *Botley, Oxford.*

(Continued on opposite page)

Technical News

Miniature Solid-state Television Camera

An all solid-state television camera, little larger than a cigarette packet and weighing only 170 g (6 oz), has been demonstrated in the United States by the Space and Defence Systems Division of Fairchild Camera and Instrument Corporation. Stated to operate in conditions ranging from bright sunshine to subdued room lighting, the new camera, Model MV-100, uses no conventional vidicon tube. It is the first in a series employing charge-coupled device sensors, the present model using an array of 10 000 photosensors assembled on a 24-pin dual-in-line package. Size of the camera is $9 \times 3{\cdot}8 \times 5{\cdot}6$ cm ($3\frac{1}{2} \times 1\frac{1}{2} \times 2\frac{1}{4}$ in) and power consumption is about 1 W.

Charge coupled device sensors are basically bulk silicon that releases charge carriers in proportion to the amount of light reflected from the scene. These charge carriers are transferred by a clocking system and transmitted to a receiver as standard television signals. Although television receivers must be slightly modified for use with the MV-100, videotape recorders need not be changed.

Television in The Netherlands and other Countries

In 1969, when the market for black and white television sets was close to a saturation point, only 45 000 colour sets were sold in The Netherlands. In 1970 the number of colour sets sold had risen to 70 000, a number that was doubled again in 1971, when more than 150 000 colour sets were sold. At the end of 1972 already more than half a million colour sets had been sold. The total number of television sets in The Netherlands, both black and white and colour, is estimated at more than 3 million. These are some of the data from a market report published recently by the Amsterdam Market Survey Bureau Ecoplan, and which contains data on the Dutch market for audio and visual appliances.

At the end of 1972 almost 35% of American families owned a colour set, whereas at that time even more than half of all Japanese families owned a colour set. The total number of television sets in use in all countries of the world (mid-1972) is estimated at 45 million. According to the Ecoplan research team, The Netherlands are holding the fourth position in the present nine EEC countries as to ownership of television sets. The first three places are taken by the United Kingdom, the German Federal Republic, and Denmark respectively.

Video cassette recorders (v.c.r.) have been on the market for some time, Philips starting large-scale production of v.c.r.s. in 1972. The first model put on the market was the N1500 for the PAL-system, with tuner, u.h.f.-modulator and time-switch. The modulator is for play-back of recorded programmes using the aerial terminals of the television set. Recording both in black and white and in colour is possible. Telefunken colour sets are now produced completely ready for video, one of the buttons of the channel-selector being intended for video-appliances, for instance the v.c.r. or video-record. However, prerecorded v.c.r. tapes are not yet of importance from the marketing point of view.

This report may be obtained from Ecoplan B.V., Sarphatistraat 58, Amsterdam, price HFL 75.

British Electronics Industry in Europe

The computer peripherals and recording heads manufacturer, Data Recording Instrument Company Limited has formed a subsidiary company in West Germany, which it has found to be a fast-expanding market place for its products and where it expects to achieve sales in excess of £1M in the next 12 months. The new company, Data Recording Instrument GmbH, is located at Düsseldorf, and will be mainly concerned with disk drives, tape transports and other peripheral equipment in Germany, Holland and Austria. The company's product range is being increased with the introduction of two new devices, a 'floppy' disk drive and a matrix printer.

Coutant Electronics Ltd, who specialize in power supply technology, have formed a wholly-owned French subsidiary company—Coutant Electronique SA—based in Paris. The new company will be concentrating initially on marketing the standard ranges of Coutant's modular and variable power supplies, and it has a projected sales turnover of over two million French francs during its first year of operation.

Data Recognition Ltd, a Reading-based British company specializing in optical mark recognition computer peripherals and systems, have announced the formation of a wholly-owned subsidiary company in the Federal Republic of Germany. Located in Frankfurt, the new company—called Data Recognition GmbH—will be operated as an entirely autonomous organization, staffed by German nationals, although initially it will be drawing on the technical resources and services of its parent. A substantial amount of the funding for setting up the new company had been contributed by the National Research Development Corporation.

CAA's Plans for Air Traffic Services

A comprehensive record of the economic and safety regulation of British civil aviation in 1972/3, and of the work of the air traffic services, is given by the Civil Aviation Authority in its first Annual Report.* The year was a significant one for the National Air Traffic Services which embarked on a massive re-equipment programme including the acquisition of a new Flight Data Processing System and Radar Data Processing System which will automate many tasks currently undertaken by controllers.

Other major developments include:

The dual installation of a long-range radar together with secondary radar equipment at Burrington, Devon, which provide controllers with clear displays and additional information as well as providing radar coverage over the South West approaches.

The improvement of 'labels' identifying aircraft and height shown on radar displays at ATC Centres.

First orders for new technology Doppler v.h.f. omni-directional range beacons which will facilitate greater accuracy in navigation and eventually enable a greater traffic flow to be achieved.

Further developments in the automatic landing programme to facilitate safe landings in poor weather by installing improved Instrument Landing Systems and associated equipment at major aerodromes. Related to this was the introduction of British instrumented runway visual range measurement installations at Heathrow, Gatwick and Manchester airports for the measurement of visibility in poor weather conditions.

* Civil Aviation Authority, Annual Report and Accounts 1972/3, price £3.30, CAA Printing and Publication Services, P.O. Box 41, Cheltenham.