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Commonwealth Engineering Conference 1969

ON 3rd November next the Seventh Meeting of the Commonwealth Engineering Conference will open in New Delhi. The four-day meeting, to be held for the first time in India, will enable representatives of the participating national institutions to discuss common professional engineering problems, in particular the world-wide demand for more qualified engineers and the consequent need to promote technical training. This in turn could lead to agreement in equating professional engineering qualifications.

The Conference will also provide opportunity for discussing the ways in which all the Institutions may play their part in increasing the engineering effort through 'learned society' activities, conference proceedings, publications, etc. Closer collaboration between institutions will undoubtedly be the underlying theme since any measure of agreement in the Commonwealth will be a factor in the deliberations of similar organizations, such as the European Federation of National Associations of Engineers (F.E.A.N.I.) and, of course, the World Federation of Engineering Organisations.

The significance of Commonwealth links is shown by the extensive Commonwealth membership of the British Chartered institutions. Each of the fourteen Chartered Engineering Institutions sponsors or joins in activities promoted by national bodies in various Commonwealth countries. A recent survey has shown that over 72,000 members of British Institutions reside outside Great Britain. The I.E.R.E., for instance, has over 3,000 of its members overseas—about a third of these being in India, where a flourishing Division issues 'Proceedings', holds meetings, and generally fosters the advancement of electronics and thereby the professional interests of its members on the sub-continent.

Indeed, in its own branch of the engineering profession, the I.E.R.E. has already demonstrated in India and elsewhere the advantages of collaborative effort, as shown by the success of the Institution's Conventions in India, the last of which was held in Delhi in September 1968 with the theme of 'Electronics in Industry'.

The Commonwealth Engineering Conference will now not only be concerned with discussing the general administration of professional engineering activities throughout the Commonwealth, but will also have a technical programme of especial interest to the host country. The Institution of Engineers (India) is organizing a technical programme on 'Priorities in Public Works in Developing Countries' which will obviously be of considerable relevance to many member countries.

The proceedings, both 'administrative' and 'technical', of this Conference will undoubtedly arouse great interest among engineers throughout the World. Such a Conference, attended by engineers from all countries of the Commonwealth, will substantially contribute to the first aim of the Conference which is almost word for word that of the principal object of the I.E.R.E., namely 'the advancement of engineering science and practice for the benefit of mankind'.

As is the case with many international conferences, it is unrealistic to expect immediate achievements. The justification for holding such a conference is to promote better understanding among its members. Without understanding, especially in science and engineering, there is little hope of improving the lot of man.

G. D. C.

INSTITUTION NOTICES

London Engineering Congress 1970

The Council of Engineering Institutions (C.E.I.), federal body for the fourteen British Chartered Engineering Institutions, is organizing a major congress in London in Spring of 1970. Stimulating papers designed to attract engineers from all over the world will be presented by eminent U.K. engineers, who will also chair discussions on provocative subjects. The theme of the Congress is 'The Challenges facing the Profession in its Services to the Community' and participants will not only be reviewing current developments but also taking critical stock of the position of their profession in society and considering means by which the growing interdependence of different engineering disciplines on each other may best be developed to the National advantage.

The Congress opens at the Royal Festival Hall, London, on 4th May 1970. During the conference period individual Institutions will provide the venues for discussions and there will be a joint final session at the Central Hall, Westminster, on 7th May. H.M. Government has indicated its support. Further information will be published as it becomes available.

The Norman W. V. Hayes Memorial Award

The Institution of Radio and Electronics Engineers Australia has announced that its Norman W. V. Hayes Memorial Award for 1968 will be made to Mr. T. A. Pascoe for his paper 'A Sweep Technique for Group Delay Measurements on Television Receivers' which was published in the October 1967 issue of the Australian Institution's *Proceedings*.

The Award was made on the recommendation of the I.E.R.E. who act as adjudicators in alternate years with the American Institute of Electrical and Electronics Engineers. It is expected that it will be presented on the occasion of the official opening ceremony of the I.R.E.E. 1969 Convention at Sydney in May. The I.E.R.E. is being represented at the Convention by Dr. F. E. Jones, F.R.S., (Fellow).

Members will be interested to learn that Mr. Pascoe, who is a design engineer with Philips Electrical Pty. Ltd., Adelaide, is a Member of the I.E.R.E., and was from 1956 to 1958 at Mullard Research Laboratories, Redhill, Surrey.

New Institution Tie

A new design of the Institution's tie has been produced in which the coat of arms forms a motif reproduced three times down the centre of the tie. This tie is available with a dark blue or wine background. Both colours are made in terylene at 18s. 6d. each and the dark blue only in silk, price 26s. 0d. Institution ties can of course be worn only by members, and are to be obtained from 9 Bedford Square, London, W.C.1.

Exchange of Programme Cards

Members of the Institution resident in the South East of England are being sent, with this issue of the *Journal*, a copy of the programme of London Meetings of the Institution of Electrical Engineers. A cordial invitation has been extended by the I.E.E. to members of the I.E.R.E. to attend any of these meetings without formality. At the same time, copies of the I.E.R.E. Programme Card and a corresponding invitation have been sent to I.E.E. members in the London region.

C.E.I. Chairman to Visit Australia

Sir Leonard Drucquer, C.Eng., F.I.E.E., Chairman of the Council of Engineering Institutions, is to visit Australia at the invitation of the Institution of Engineers, Australia.

He will be accompanied by Lady Drucquer and they will attend the jubilee conference of the Australian Institution of Engineers to be held in Sydney from 14th to 19th April 1969. An extensive programme for this jubilee has been planned and in addition to an exhibition of Australian engineering achievements, a number of technical sessions and tours are being arranged.

Sir Leonard will be representing the fourteen U.K. Chartered Engineering Institutions comprising C.E.I. and will also visit the U.S.A. and South Africa for discussions with Institutions and learned societies in those countries on engineering problems of mutual and international interest.

'Guidance for Authors'

Members and others who are contemplating writing papers for *The Radio and Electronic Engineer* are reminded that the Institution has published a leaflet with the above title which may be obtained on application to the Secretary of the Programme and Papers Committee. The leaflet contains information on the requirements of style and presentation of papers, and advice on the preparation of illustrations.

Indications are also given regarding abbreviations; letter symbols and units.

In this last connection additional information on future Institution practice was given in the article 'The Use of S.I. Units' on pages 61 to 64 of the July 1966 issue of the *Journal*.

It is helpful if an intending author first submits a synopsis of his paper to the Committee as this enables the contents of the paper to be discussed in advance of carrying out detailed preparation.

Authors are asked to submit at least two copies of their papers (with prints of the illustrations) in order that the process of consideration by the Papers Committee's referees (normally two in number) can be completed with the least possible delay.

U.D.C. 621.382: 681.32

The Development of Large Scale Integration

By

K. J. DEAN, M.Sc., F.Inst.P., C.Eng., F.I.E.E., F.I.E.R.E.†

An Address given at the Inaugural Meeting of the Institution's Components and Circuits Group in London on 9th October 1968.

Summary: Large scale integration (l.s.i.) presents the opportunity of putting more circuitry on a single silicon chip than ever before, so making possible much more complex digital systems. However, it challenges us to decide which groups of circuits will be logically and economically viable as system components. The development of integrated circuits is traced from the introduction of the planar process and some suggestions are made of the types of networks which are likely to prove attractive in l.s.i. systems. Some of the implications of l.s.i. are discussed, and in particular the educational problems involved.

1. Introduction

Surely, the inaugural meeting of the Components and Circuits Group is as good a time as any to attempt to define what is meant by *components* and *circuits.* It has been said that a circuit is a collection of circuit elements—resistors, capacitors, transistors, diodes and so on—and that a circuit functions in a way which depends on the circuit elements of which it consists. On the other hand, a component has been described as that basic part of a circuit which can be regarded as an entity in itself from the points of view of manufacture and maintenance. Now an integrated circuit fulfils both these sets of conditions. Is this device then a component or a circuit or both?[1] Perhaps this argument shows that our notion of a component must not be static. In the past a component has been part of a circuit. In fact, the terms *component* and *circuit element* were very nearly synonymous. At the present time there are some components which are themselves circuits. Large scale integration (l.s.i.) is today leading us to a position where the majority of components are made up of circuits. These circuits, acting together, can be regarded as a single item, that is, a component. A component, in this modern usage, is not *necessarily* a fractional part of a circuit, or even of a simple sub-system. Hence an electronic component may be better defined as that part of a system which can be regarded as a basic entity for manufacture or maintenance and may itself consist of a group of circuits, or a circuit, or a part of a circuit.

2. The Development of Microelectronics

Any assessment one might make about present trends in microelectronics must be based on one's experience of past trends. An important milestone in the history of electronics was the introduction in 1959 of the planar process for the manufacture of transistors. Using this process, large numbers of transistors could be manufactured on a single slice, with closely-matched characteristics. As experience of the process was acquired, the characteristics of the devices became more predictable and the surface area per device became smaller. It was not long before dual transistors became available, and using triple diffusion, electrically-isolated transistors with similar thermal characteristics were also being manufactured. It was then only a step, using these diffusions, to producing isolated regions of uniform resistance so that resistive networks could be included with the active devices. With the addition of evaporated aluminium conductor patterns, integrated circuits had arrived!

Those early circuits were primarily logic gates, usually 2-, 3- or 4-input resistor-transistor logic gates. They first appeared in 1960 and the first advertisements for them in this country were in the summer of 1962. These RTL gates were designed on the basis of the input current causing the transistor to saturate and were typically 1 mm square. Logic gates were the natural choice for the early integrated circuits since diffusion methods could not be controlled with sufficient certainty to make the design of worthwhile linear circuits a commercial proposition. These followed later. Hence the concept of the circuit (a 2-input gate) as a component is reinforced by the parallel idea of a logic gate as a good basic unit for design purposes; an idea which computer engineers had accepted 15 years earlier.

There is an interesting history to the development of integrated circuits. At first it was said that they were small. At that time, this did not impress engineers who had barely recovered from the size reduction which accompanied the use of transistors, and in any case they could usually put the required circuitry into the instrument cabinets which were available. It was chiefly in the military field that specifications became more and more demanding and the opportunity of using small component size to increase system complexity was seized. A walkie-talkie is a

† Vice-Principal, Twickenham College of Technology.

typical self-contained system. The weight which could be carried by a soldier in the field dictated the system weight, whilst the complexity depended on the components which were available. It was only later that it was generally appreciated that the size of an instrument is more or less constant and that its complexity rises as the component size falls.[2]

Secondly, it was argued that integrated circuits were reliable, since wiring and soldered joints were minimized. (This was only really true of monolithic construction, and multi-chip circuits were then fashionable.) Again, engineers were not impressed unless they were designing satellites or missiles. It was only when enough was known about the technology to build up a quantity production of circuits that the third argument, 'integrated circuits are cheaper' really rang true. At the same time the number of circuit elements per circuit was continually rising.

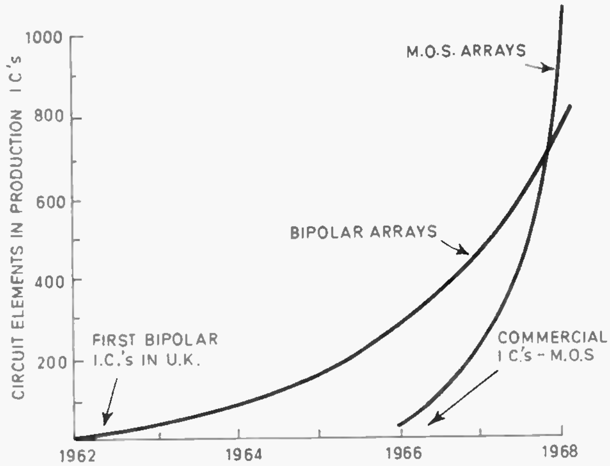


Fig. 1. Graph showing typical complexity of production integrated circuits during the period 1962–1968.

On the one hand there was the pressure to increase production yield so that profits increased, and on the other hand to increase component density on the chip so that function complexity kept ahead of commercial competition. It is this continuing battle with its inevitable compromises which is so fascinating for the electronics engineer.

Since 1962, function complexity has continually increased. There have been faster systems of logic such as DTL, TTL and ECL, which involve more complex circuitry, leading eventually to reliable non-saturating forms of nanosecond logic. (The first circuits were advertised as operating at a 1 MHz clock rate.) There have been dual gates, quad gates and hex inverters. It should be noticed that the gate is still the basic design unit. Since about 1963 the flip-flop in integrated form has been available also, together with half-adders and equivalence functions, but these can still be appreciated as collections of gates, just as now manufacturers still attempt to describe more complex integrated circuits as collections of transistors, diodes and resistors. How much longer can this traditional viewpoint last?

1966 saw commercial production of small shift registers and counters, often decade counters. It also saw a determined onslaught on the surface problems of metal oxide semiconductors. These problems were due in part to sodium ion contamination causing a shift in threshold voltage and an increase in leakage current; m.o.s. integrated circuits are now in production on a large scale and surface contamination problems are to a large extent things of the past. Long term stability has been assured by surface passivation with a layer of silicon nitride. These devices bring fresh advantages of high input impedance and hence large fan-out within the system. These unipolar circuits are still not as fast as otherwise comparable bipolar circuits and precautions need to be taken at the interface between m.o.s. circuitry and 'the outside world'. However, they are less complex to manufacture and one sees in this an argument for increasing the complexity of m.o.s. circuitry so that any interface problem is minimized.

Throughout the development of silicon chip circuits there have been parallel interests in thin film and thick film circuits. At times this has been distinctively competitive, and the development of flip-chip transistors was an attempt to design circuits using these transistors together with the cheap manufacturing techniques of passive elements (resistors and capacitors). Of course, the design philosophies are quite different. Thick film circuit design will tend to maximize the use of passive elements in relation to active ones, as did discrete component technology, but silicon chip circuit design tends to favour active elements since these take up so much less space than resistors on the chip. Capacitors on integrated circuits usually involve a prohibitive amount of surface area. However, thick film circuits have survived and flip-chip methods are now possible for integrated circuits as well as for single transistors.

The production yield of silicon integrated circuits[3] depends primarily on the size of the chip and on the surface density of the interconnection pattern rather than on the density of surface elements. This is one of the main reasons why a number of manufacturers have hurried into using two-layer interconnection patterns. These effectively reduce the surface density of interconnections in each layer, so that the overall production yield may thus be increased. Clearly, as chips become more complex, the use of multi-layer interconnections becomes inevitable.

It was at this point[4,5] that the use of beam leads was introduced into the United Kingdom in an attempt to raise reliability yet more. This was possible because beam leads eliminated one of the major sources of unreliability, namely, the bond between the chip and the connecting lead. Beam leads are produced by multiple deposition, usually of platinum and gold, to extend the conductors beyond the edge of each chip, so that when the semiconductor is etched away from the edge of the chip, they protrude beyond the edges and can be used for bonding on to a thick film in a way similar to that of the flip-chip. Thus a new form of hybrid multi-chip circuit has been developed with beam leads or wired leads connecting silicon integrated circuits to a thick film pattern of conductors and resistors on a common substrate.

The following points summarize the developments which have been discussed. These trends have a definite bearing on the move towards l.s.i.

(i) Our notion of what is meant by a component is undergoing considerable change. Components are becoming more complex.

(ii) The logic gate has been the basic design-unit of digital systems. Present chips contain very many logic gates.

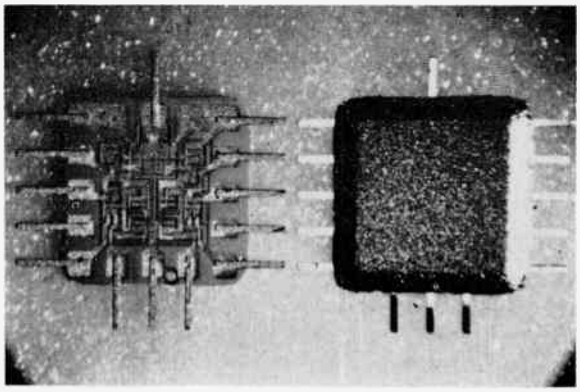


Fig. 2. Integrated circuit showing beam leads. The reverse side of the chip is also shown (*Marconi-Elliott Microelectronics Ltd*).

(iii) The potential market for integrated circuits is enormous since unit price can now be an order less than for some discrete circuits.

(iv) Improvements in manufacturing techniques lead to more complex chips and this leads to more complicated equipment replacing less complex equipment of about the same order of bulk.

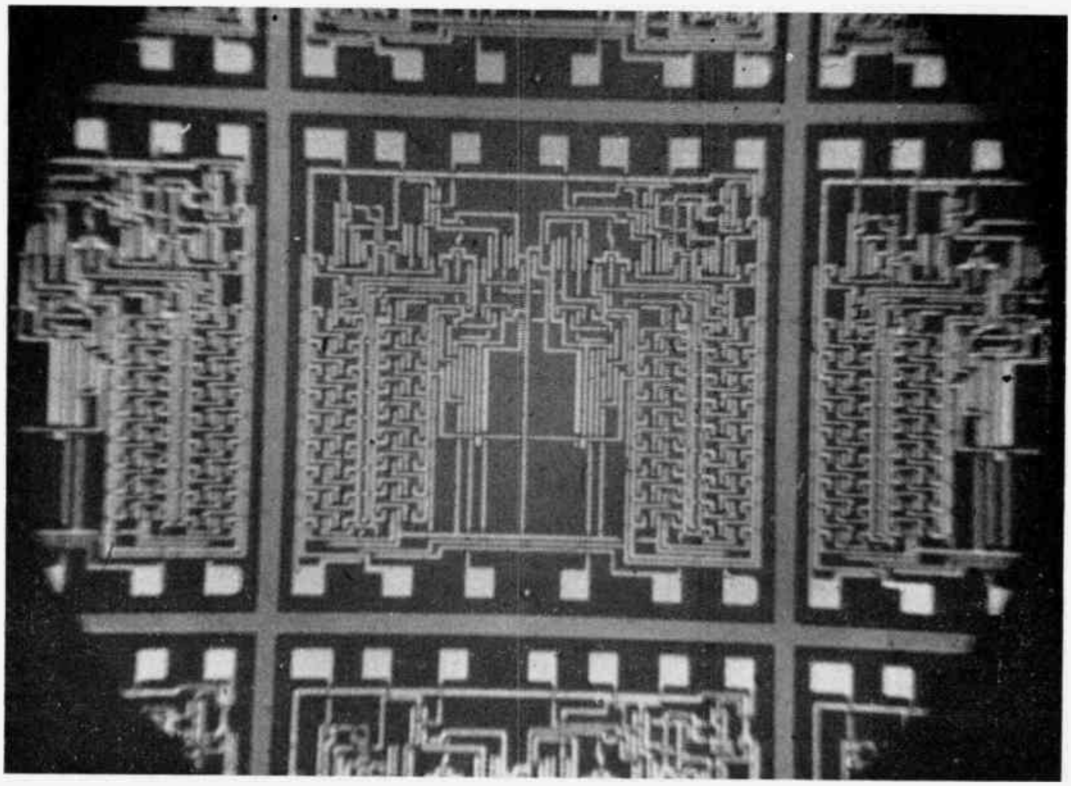


Fig. 3. Dual 20-bit shift register (*Marconi-Elliott Microelectronics Ltd.*).

3. The Present State of Microelectronics

Digital circuits are now being produced which are very much more complex than a few years ago. These include multi-bit shift registers, counters and code converters. Frequently, the implementation of such functions are examples of unipolar circuits (that is, m.o.s. arrays[6]). One of the problems associated with these complex chips is to find a system with relatively few external leads. For example, some companies† are manufacturing a chip which is a 4-bit b.c.d. counter (i.e. a decade counter), a second chip which is a 4-bit storage register into which the count at any time can

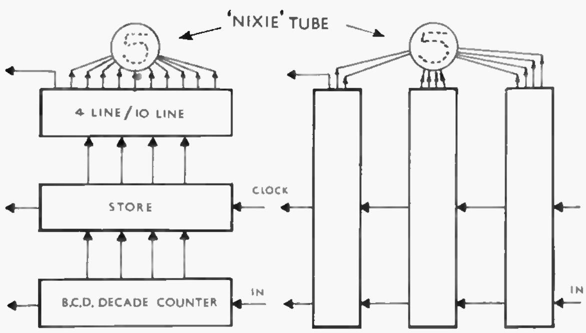


Fig. 4. Diagram showing how it is possible to redesign a system which includes counter, store and decoder-driver.

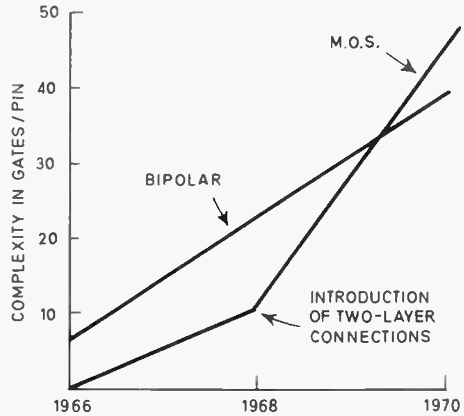


Fig. 5. Graph showing the complexity of integrated circuits, measured in gates/pin, during the period 1966–1970.

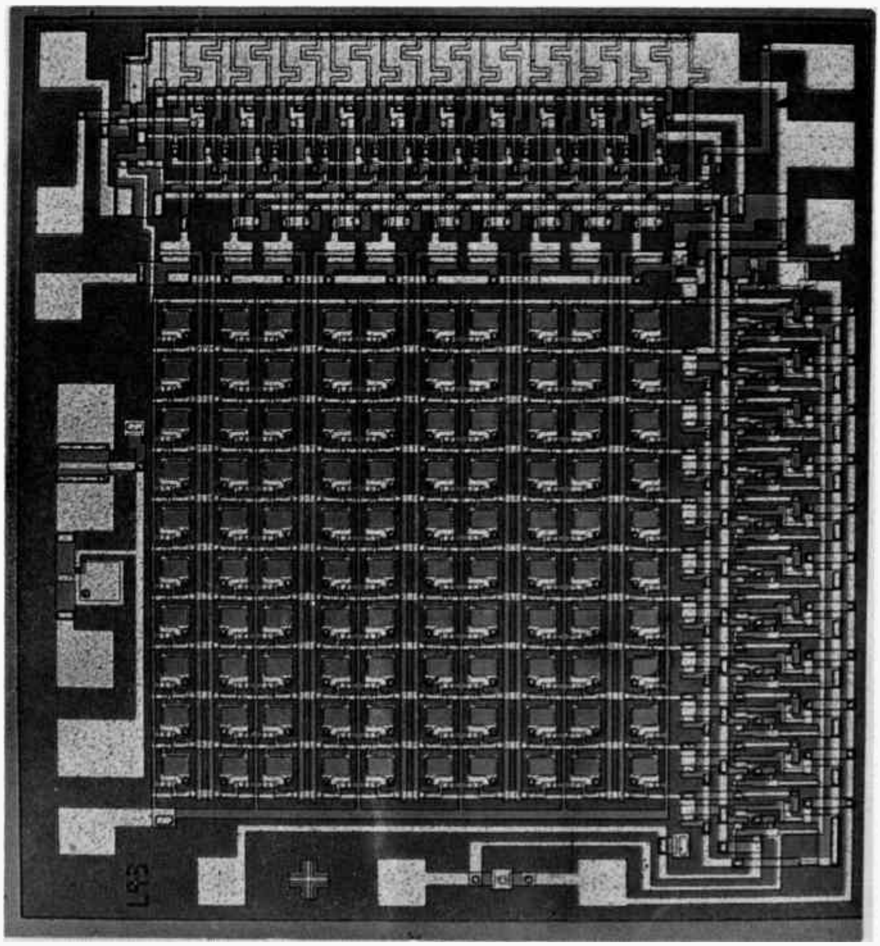


Fig. 6. The chip contains an array of 10×10 photodiodes, together with two decoding shift registers (*The Plessey Company Ltd.*).

† CμL 9958/59/60 and SN 7441/75/90 N.

be shifted and stored, and a third chip which contains a code converter changing the binary-decimal code of the counter and store into a 10-line code and providing drive circuits for a numerical indicator tube. It might be better to redesign these chips not on the basis of their separate functions, but in order to minimize the connections to each chip. Alternatively, all these functions might be contained on only one chip.

Nowadays one talks of 40-, 100-, and 200-lead packages. The cost of packaging is a significant fraction of the overall cost of the device. The use of multi-layer interconnections has already been mentioned. This technique has done much to influence the compromise between the number of pin connections and the complexity of the array, both when using m.o.s. arrays and when using bipolar circuits. Perhaps the ideal situation is one in which there is a single input and a single output, and a vast array of complex logic on the chip, but such a solution is seldom possible. For example, a scratch pad memory is an attractive integrated circuit which must, of necessity, have multiple inputs and outputs. The same comments can be made of a 100-bit photodiode array which can be used for character recognition or as a crude television camera. However, in this case the array is accompanied by two shift registers which are used to scan the contents of the array and serialize the video output from it. Without these registers a much larger number of interconnections would have been required. This could have been done with the memory chip also, but this would have increased the access time to the memory to an extent which might well have been unacceptable.

To summarize the present position then, the following points indicate current trends.

(i) Technological developments have made it possible to make much more complex chips than before. One is now losing sight of the circuit elements in the chip when one wishes to describe its function.

(ii) There is the problem of the number of pin connections. This number must be kept small even though the system is complex.

(iii) One should notice that there is a symmetry in the layout of the chip. Symmetrical groups of circuits are to be preferred, since a regular structure in the layout of the chip aids in the design of the masks which will have to be used.

(iv) In explaining the logical operation of the chip the logic gate is not used as the basic unit of design as much as previously.

(v) Design techniques must favour serial systems in which the parallel (and hence complex) aspects of the system are all contained within a chip. However, speed requirements may insist on parallel systems.

(vi) Many engineers who would formerly have called themselves circuit engineers are now finding that their work has become chiefly concerned with system design.[7] In fact, it is rather strange, if not to be deplored, that the majority of our courses in universities and colleges assume that circuit design is still the main function of the practising engineer.

4. The Future of Microelectronics

Before going any further one ought to define the terms *medium scale integration* and *large scale integration*. The first is said to be what we have today and the second is what we hope for tomorrow. Each manufacturer has his own definitions and perhaps like our definition of *component* they alter with time under the influence of developments in technology. Some dismiss l.s.i. as 'large scale insanity' and say that we shall never see it. It might be better to say that it will be a long time before complex systems only are manufactured and not simple gates also. At the present time four classes of digital chips may be distinguished:

(1) Gates, e.g. quad 2-input gates, etc.

(2) Complex functions such as the J–K flip-flop or the dual half adder, equivalent to not more than about 20 gates.

(3) Medium scale integration including dynamic shift registers and some counters. Here the equivalent of 20–50 gates might be involved, and two-layer interconnections are used on the chip.

(4) Large scale integration where in excess of 50 gates are employed. Here there will be at least two layers of interconnections and the chip layout will be produced by computer-aided design. More and more, l.s.i. will involve a complete slice (of perhaps 50 mm diameter) laid out as a single chip.

These are definitions with which not everyone will agree. There will be some anomalies also. It is suggested that these differences of opinion are due to each engineer in the manufacturing industry having an eye on his company's nomenclature[8] and progress.

It is always difficult to predict the future, and such predictions often make strange reading in retrospect, but some manufacturers are now producing chips with one layer of metallization and permitting customers to specify their own second layer. A glance at a chip of this sort shows that here again there is a symmetry about the cells of these arrays. The recent announcement[9] of advanced diffusion techniques permitting element spacings of about 3 μm and circuit element density of $1{\cdot}5 \times 10^5$ per cm^2 also

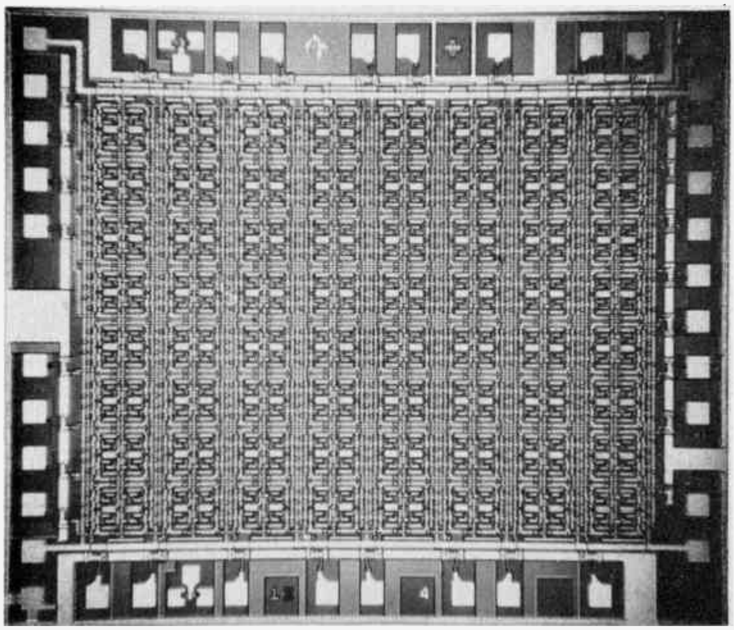


Fig. 7. A dual 60-bit m.o.s. shift register (*Texas Instruments Ltd.*).

shows that manufacturers are able to control the technology more precisely than before. Perhaps there will be larger shift registers, more programmable counters, multiplex switches and decoders, and so forth. But how many people need a 200-bit shift register? It seems that l.s.i. has presented us with a new problem which may be expressed thus:

(i) What system is there which is so complex that it needs a large scale integrated chip to contain it, but is so general that it is a commercial proposition to manufacture it?

(ii) How can such a system be designed to minimize the number of connections to it, without detracting from its usefulness (e.g. its speed or its flexibility)?

(iii) Can the logic be designed in a symmetrical way so that the pattern produced aids the layout of the chip?

Some believe that no viable solution to these questions can be found, so one must rely solely on customer-designed interconnection patterns.[10] Thus the onus is put on the customer to optimize his interconnection pattern to suit the requirements of l.s.i.

This may be only partly true, an alternative approach being to use arrays of interconnected cells in which the cells are all identical. In the short history of integrated circuits (it is only about seven years) the emphasis has been on symmetry of circuitry and a high complexity-to-pin ratio. One of the advantages claimed for microcellular systems is that they involve higher complexity than for other similar or even smaller systems. Recently, research papers[11,12] have drawn attention to the use of cellular arrays for a particular digital application, that of arithmetic. These arrays are highly symmetrical and typically have in excess of ten gates for each external connection to the array. It may well be that if our experience with cellular arrays keeps pace with l.s.i.

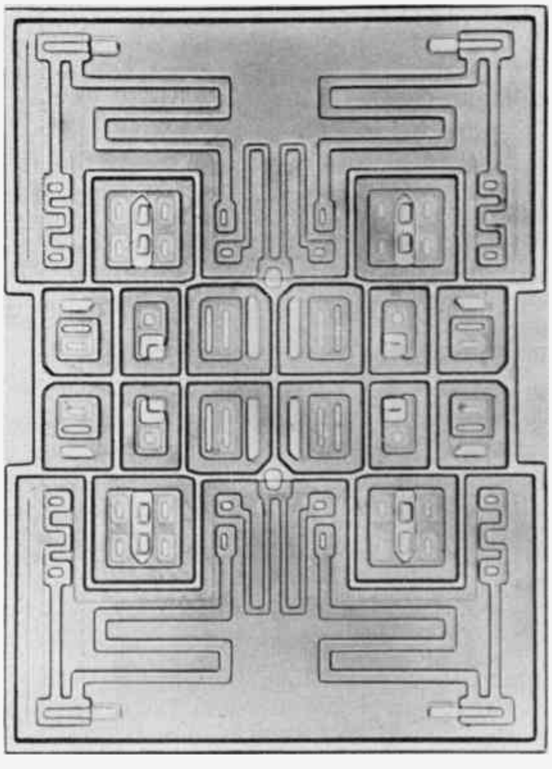


Fig. 8. A single cell of a micromatrix array (*SGS (United Kingdom) Ltd.*).

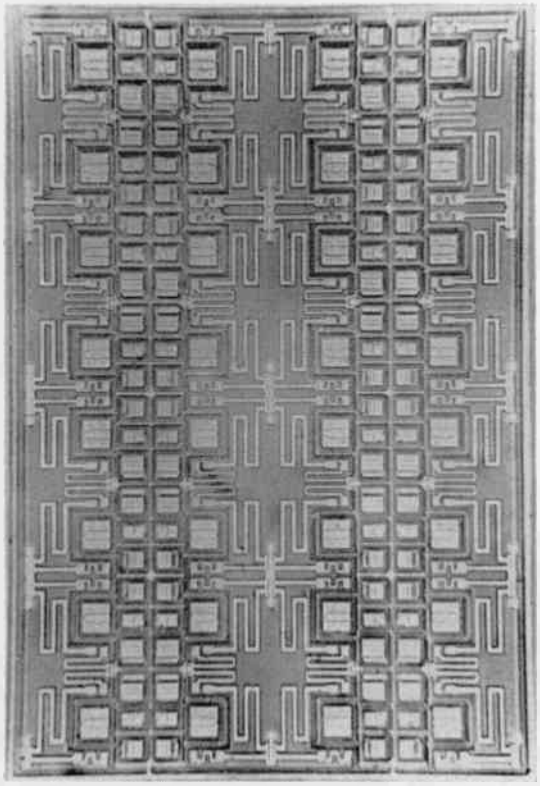
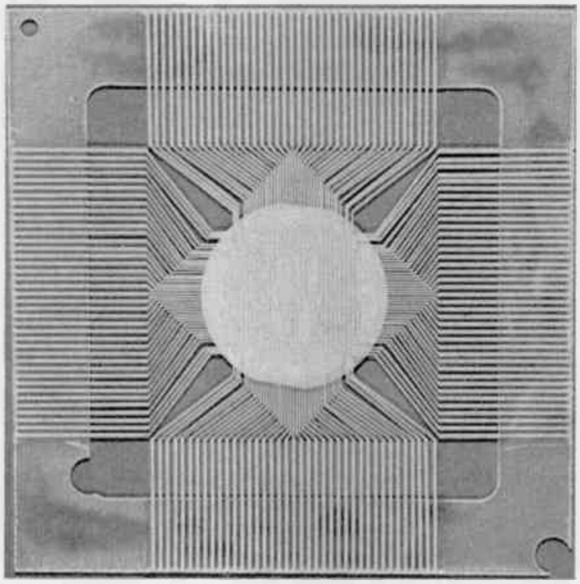


Fig. 9. A complete chip containing eight identical cells of a micromatrix array (*SGS* (*United Kingdom*) *Ltd.*).

capability we shall come to regard these arrays as normal building blocks for use in complex logical systems.

One hears a great deal about computer-aided design, firstly for the layout of masks in making integrated circuits[13] and secondly to permit discretionary use of parts of the slice and even parts of l.s.i. chips. Perhaps this last application will become less important only when optimum yield points have become sufficiently high to make it untenable. However, it will be some time yet before all aspects of logic design are computer controlled. These arrays which have been mentioned have been iteratively connected, and because of their highly regular structure these seem most suitable for l.s.i., although non-iterative arrays are also being developed in this country.



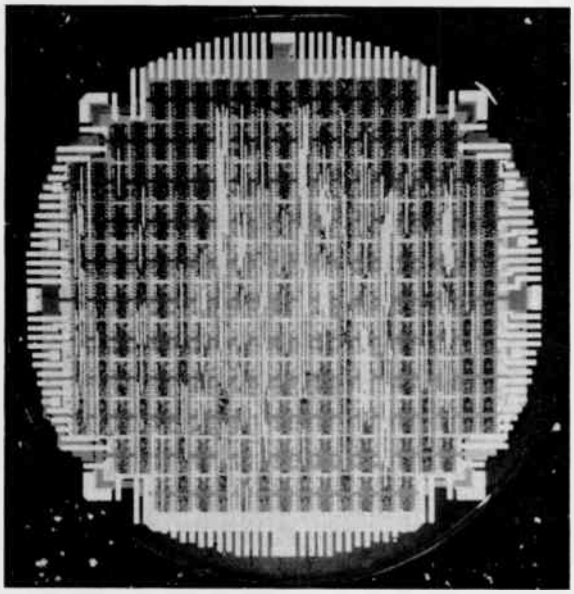


Fig. 10. L.s.i. slice showing discretionary wiring (*Texas Instruments Ltd.*).

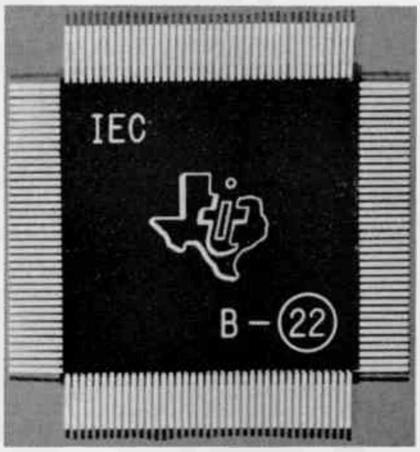


Fig. 11. 156-pin lead frame with slice and encapsulated array (*Texas Instruments Ltd.*).

Beyond this all is pure speculation. A computer on a chip was once the stated goal of one American organization. Perhaps when it comes (if it is a worthwhile computer) it will be using organic semiconductors. By then, however, the aim will be *a computer in a molecule* or is that what that celebrated organic semiconductor, DNA, really is?

5. Conclusion

These then are some of the trends which, as an educationalist, one sees looking back over seven years. These are factors which must influence logic design, and also the way in which electronics, in general, must be taught in the future. These changes in device technology have altered the course of electronics, and where its mainstream is likely to flow profitably in the next few years. The state has been reached with l.s.i., and logic design in particular, where one has long lost sight of the circuit elements in the system and where even gates are too small as units in which to visualize design problems. To what extent does it remain justifiable to explain hardware in terms of circuit element parameters when our components contain many thousands of these elements arranged in vast arrays of regular patterns of a customer's own choosing? Perhaps at the end of another seven years the new achievements will no longer be at the interface between physics and engineering, but 'old-style' electronics engineers will all be back at college reading *the new biology* to become 'Organic Electronics Engineers.'

6. Acknowledgments

The author wishes to record his thanks for the unstinted co-operation he has received from many friends in the microelectronics industry, and for permission to reproduce the illustrations to this paper.

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Electrical Efficiency of an Acousto-electric Oscillator

By

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AND

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Summary: A theoretical analysis of the electrical behaviour of an acousto-electric oscillator is presented. Expressions are derived for the electric field distribution in the crystal and for the electrical power output. Numerical calculations are made for cadmium sulphide crystals and the results indicate a possible power output in the range of microwatts with an efficiency of about 10^{-6}.

1. Introduction

Thin samples of photo-conducting cadmium sulphide crystals have been found to oscillate on the application of electric fields for which the drift velocity of the charge carriers exceeds the sound velocity.[1-3] The oscillations have been explained to be due to the building up of noise vibrations as a result of the round-trip acousto-electric gain.[4] In general, multi-mode oscillations are excited at frequencies corresponding to the resonant frequencies of the resonator formed by the crystal. However, very recently it has been observed that single-mode operation may be obtained by applying steady electric fields.[5] In such an oscillating crystal, the current also oscillates and the crystal generates a.c. electrical energy, though a significant part of the energy supplied by the driving source is converted into acoustic vibrations. The device may, therefore, find applications as an electrical oscillator as well as an acoustic generator. In the present paper the electrical behaviour of the oscillator is theoretically analysed by considering a homogeneous crystal having variation of fields in one direction only.

In Section 2, expressions are given for the acoustic displacement in a sample executing steady oscillations. The electric field distribution associated with the acoustic vibration is obtained in Section 3. In Section 4 the output impedance and the electrical power output of the oscillator are studied. Estimates of the voltage and power output for a CdS crystal of conductivity $10^{-2}\,\Omega^{-1}\,\text{cm}^{-1}$ and thickness 0·05 cm for a frequency of 100 MHz, are given in Section 5.

2. Acoustic Displacement in an Oscillating Crystal

The stationary acoustic wave in an oscillating crystal consists of two components—one propagating in the direction of the electric field and the other in the opposite direction. Hence, the particle displacement at a distance x from the cathode end, at any instant t may be expressed as

$$u(x,t) = u_{0+}\exp\{j(\omega t - k_+ x)\} + u_{0-}\exp\{j(\omega t + k_- x)\} \qquad \ldots\ldots(1)$$

where u_{0+} and u_{0-} are the amplitudes of the forward and backward waves at $x = 0$; k_+ and k_- are the respective propagation constants.

For the sustenance of a stationary acoustic wave within the crystal, the particle displacement at any point should be identical in phase and amplitude after each round-trip through the crystal. This consideration leads to the following condition for steady, self-sustained acoustic oscillations:

$$\exp\{j(k_+ + k_-)L\} = \frac{1}{\gamma^2} \qquad \ldots\ldots(2)$$

The reflection coefficients of the two end-faces of the crystal have been assumed to be identical and given by γ.

Putting

$$jk_+ = \alpha_+ + j\beta_+, \quad jk_- = \alpha_- + j\beta_-$$

and

$$\gamma = |\gamma|\exp(j\theta)$$

in eqn. (2) we obtain

$$\exp\{-(\alpha_+ + \alpha_-)L\} = \frac{1}{|\gamma|^2} \qquad \ldots\ldots(3)$$

and

$$(\beta_+ + \beta_-)L = m\pi + \theta \qquad \ldots\ldots(4)$$

where m is any integer. Equations (3) and (4) give respectively the amplitude and phase conditions to be satisfied by the forward and backward acoustic waves for the sustenance of a stationary acoustic wave within the crystal.

Using the above conditions we obtain for the particle displacement in the crystal

$$u(x,t) = u_{0+}\left\{\exp(-jk_+ x) + \frac{1}{\gamma}\exp(jk_- x)\right\}\exp(j\omega t) \qquad \ldots\ldots(5)$$

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3. Electric Field Distribution

The elastic strain produced by the stationary sound wave at any point x is

$$S(x,t) = \frac{\partial u(x,t)}{\partial x}$$
$$= \mathrm{j}u_{0+}\left\{-k_+ \exp(-\mathrm{j}k_+ x) + \frac{1}{\gamma} k_- \exp(\mathrm{j}k_- x)\right\} \times \exp(\mathrm{j}\omega t) \quad \ldots\ldots(6)$$

Due to the piezo-electric coupling this strain in the crystal produces electrical displacement which in turn produces spatial variation of the charge carrier density. The spatial variation of the carrier density is again associated with a varying electric field, since the current density through the crystal must be continuous.

Let us denote the varying components of conduction current, electrical displacement and carrier density respectively by J_{c_1}, D_1 and n_s. These variables are related with the total conduction current J_c and the initial carrier density n_0 by the following equations[4]:

$$J_c(x,t) = e\mu[n_0 + fn_s(x,t)][E_0 + E_1(x,t)] + $$
$$+ eD_n \frac{\partial}{\partial x}[n_0 + fn_s(x,t)] \quad \ldots\ldots(7)$$

$$D_1(x,t) = \varepsilon E_1(x,t) + pS(x,t) \quad \ldots\ldots(8)$$

where ε and p are respectively the permittivity and the piezoelectric coefficient of the crystal.

The d.c. electric field, E_0, is such that the electron drift velocity exceeds the sound velocity. However, the sound velocity being much smaller than the thermal velocity of the electrons at room temperature, the electron temperature may be assumed to be unaltered by the field. The mobility μ and the diffusion constant D_n may, therefore, be taken to be the same as at low fields.

The excitation of the acoustic flux may affect the electric field E_0 due to acousto-electric interaction.[6] We shall assume a low level of acoustic flux and neglect the possible spatial variation of E_0.

We also note that en_s represents the space charge produced to ensure charge continuity. A part of this charge may arise from the trapped charges. The trapping factor is assumed to be f and fn_s, therefore, represents the mobile charges available for conduction. We shall assume that f is independent of x. It may depend on the frequency of oscillations, if the frequency is comparable to the time constant for trapping. The factor f in eqn. (7) would then represent its value at the frequency of operation.

Separating eqn. (7) into the d.c. and a.c. parts neglecting the harmonic components, combining the resulting equations with eqn. (8) and Poisson's equation

$$\frac{\partial D_1(x)}{\partial x} = -en_s(x)$$

and using the continuity condition for the total alternating current density J, we obtain for the a.c. electric field,

$$D_n \frac{\partial^2 E_1(x)}{\partial x^2} + \frac{fJ_0}{en_0}\frac{\partial E_1(x)}{\partial x} - \frac{1}{\varepsilon}(\sigma_0 + \mathrm{j}\omega\varepsilon)E_1(x)$$
$$= -\frac{\mathrm{j}pk_+ u_{0+}}{\varepsilon}\exp(-\mathrm{j}k_+ x) \times$$
$$\times\left(\mathrm{j}\omega + \mathrm{j}k_+ \frac{fJ_0}{en_0} + k_+^2 D_n\right) +$$
$$+ \frac{\mathrm{j}pk_- u_{0+}}{\varepsilon\gamma}\exp(\mathrm{j}k_- x) \times$$
$$\times\left(\mathrm{j}\omega - \mathrm{j}k_- \frac{fJ_0}{en_0} + k_-^2 D_n\right) - \frac{1}{\varepsilon}J \quad \ldots\ldots(9)$$

where $\sigma_0 (= n_0 e\mu)$ is the d.c. conductivity of the crystal and J_0 the d.c. component of conduction current.

Solution of eqn. (9) gives

$$E_1(x) = C_1 \exp(m_1 x) + C_2 \exp(m_2 x) +$$
$$+ \frac{J}{\sigma_0 + \mathrm{j}\omega\varepsilon} + A_1 \exp(-\mathrm{j}k_+ x) +$$
$$+ B_1 \exp(\mathrm{j}k_- x) \quad \ldots\ldots(10)$$

where

$$A_1 = \frac{\mathrm{j}pk_+ u_{0+}}{\varepsilon} \cdot \frac{\mathrm{j}\omega + \mathrm{j}k_+ \frac{fJ_0}{en_0} + k_+^2 D_n}{k_+^2 D_n + \mathrm{j}k_+ \frac{fJ_0}{en_0} + \frac{1}{\varepsilon}(\sigma_0 + j\omega\varepsilon)}$$

$$B_1 = -\mathrm{j}p\frac{1}{\gamma}\frac{k_- u_{0+}}{\varepsilon} \cdot \frac{\mathrm{j}\omega - \mathrm{j}k_- \frac{fJ_0}{en_0} + k_-^2 D_n}{k_-^2 D_n - \mathrm{j}k_- \frac{fJ_0}{en_0} + \frac{1}{\varepsilon}(\sigma_0 + \mathrm{j}\omega\varepsilon)}$$

$$m_1, m_2 = \frac{-f\mu E_0 \pm \sqrt{f^2\mu^2 E_0^2 + \frac{4D_n}{\varepsilon}(\sigma_0 + \mathrm{j}\omega\varepsilon)}}{2D_n}$$

C_1 and C_2 are two arbitrary constants.

4. Electrical Power Output and Impedance

The arbitrary constants C_1 and C_2 in eqn. (10) are to be evaluated so as to fit the boundary conditions for $E_1(x)$. The boundary conditions are determined by the state of the surface and the contacts on the sample. In some analyses of similar problems it has been assumed that for an ohmic contact, the a.c. electric field may be taken to be zero at the ends.[7] We shall use the same condition in the following analysis. It should be noted that this assumption would also mean that there is variation in the steady field at the ends. However, the variation would be confined to a very small region of the order of a Debye length (less than 5 μm for experimental samples) and should not affect much the results derived here assuming a constant d.c. field. Using these boundary conditions one obtains for C_1 and C_2

$$C_1 = \frac{\dfrac{J}{\sigma_0 + j\omega\varepsilon} + A_1 \exp(-jk_+ L) + B_1 \exp(jk_- L) - \exp(m_2 L)\left(\dfrac{J}{\sigma_0 + j\omega\varepsilon} + A_1 + B_1\right)}{\exp(m_2 L) - \exp(m_1 L)} \qquad \ldots\ldots(11)$$

$$C_2 = \frac{\left(\dfrac{J}{\sigma_0 + j\omega\varepsilon} + A_1 + B_1\right)\exp(m_1 L) - \left\{\dfrac{J}{\sigma_0 + j\omega\varepsilon} + A_1 \exp(-jk_+ L) + B_1 \exp(jk_- L)\right\}}{\exp(m_2 L) - \exp(m_1 L)} \qquad \ldots\ldots(12)$$

If Z_1 be the external load impedance connected across the crystal, we have

$$\int_0^L E_1(x)\mathrm{d}x = -Z_1 J s \qquad \ldots\ldots(13)$$

where s is the cross-sectional area of the crystal.

Using eqn. (13) and replacing C_1 and C_2 by (11) and (12) in eqn. (10) we get for the total a.c. component of the current in the crystal

$$I = \frac{|v| \exp(j\phi)}{Z_1 + Z_s(1-\delta)} \qquad \ldots\ldots(14)$$

where

$$|v| \exp(j\phi) = \frac{1}{\exp(m_2 L) - \exp(m_1 L)} \Bigg[\Bigg\{\left(\frac{i}{m_1} - \frac{1}{m_2}\right) + \left(\frac{\exp(m_2 L)}{m_2} - \frac{\exp(m_1 L)}{m_1}\right) \times$$

$$\{A_1 \exp(-jk_+ L) + B_1 \exp(jk_- L)\} +$$

$$+\Bigg\{\left(\frac{\exp(m_1 L)}{m_2} - \frac{\exp(m_2 L)}{m_1}\right) + \exp((m_1 + m_2)L)\left(\frac{1}{m_1} - \frac{1}{m_2}\Bigg\{\Bigg((A_1 + B_1) +\right.$$

$$+\{\exp(m_2 L) - \exp(m_1 L)\}\left\{\frac{A_1}{-jk_+}(1 - \exp(-jk_+ L)) + \frac{B_1}{jk_-}(1 - \exp(jk_- L))\right\}\Bigg]$$

$$Z_s = \frac{1}{\sigma_0 \dfrac{s}{L} + j\omega\varepsilon \dfrac{s}{L}}$$

$$\delta = \frac{1}{L}\left(\frac{1}{m_1} - \frac{1}{m_2}\right) \frac{(1 - \exp(m_1 L))(1 - \exp(m_2 L))}{\exp(m_2 L) - \exp(m_1 L)}$$

$|v| \exp(j\phi)$ represents the alternating e.m.f. generated in the crystal and $Z_s(1-\delta)$ is the output impedance.

The evaluation of $|v|$, ϕ and δ of eqn. (14), for the general case, involves complex expressions. The qualitative behaviour of the oscillator may, however, be discussed with the following simplifying assumptions:

(i) The two ends of the crystal are kept completely free for vibrations and $\gamma = 1$.

(ii) The phase constants for the acoustic wave, β_+ and β_- in the two directions are equal.

(iii) The conductivity of the crystal is such that $\sigma_0 \gg \omega\varepsilon$.

For these assumptions we get

$$I = \frac{V_1 + jV_2}{Z_1 + Z_s\left(1 + \dfrac{\psi_4}{\psi_3}\dfrac{\sigma_0}{L}\right)} \qquad \ldots\ldots(15)$$

where

$$V_1 = \frac{1}{\psi_3}\left[(-1)^m \exp(g_+ L)(\psi_1 X - \psi_3 X') + \psi_2 X + \psi_3 X'\right]$$

$$V_2 = \frac{1}{\psi_3}\left[(-1)^m \exp(g_+ L)(\psi_1 Y - \psi_3 Y') + \psi_2 Y + \psi_3 Y'\right]$$

$$\psi_1 = \frac{\varepsilon}{\sigma_0}\left[a - \exp\left(-\frac{f\mu E_0}{2D_n}L\right)\left\{f\mu E_0 \sinh\left(\frac{a}{2D_n}L\right) + a\cosh\left(\frac{a}{2D_n}L\right)\right\}\right]$$

$$\psi_2 = \frac{\varepsilon}{\sigma_0}\left[\exp\left(-\frac{f\mu E_0}{2D_n}L\right)\left\{f\mu E_0 \sinh\left(\frac{a}{2D_n}L\right) - a\cosh\left(\frac{a}{2D_n}L\right)\right\} + a\exp\left(-\frac{f\mu E_0}{D_n}L\right)\right]$$

$$\psi_3 = -2\exp\left(-\frac{f\mu E_0}{2D_n}L\right)\sinh\left(\frac{a}{2D_n}L\right)$$

$$\psi_4 = -\frac{\varepsilon}{\sigma_0^2}a\left\{1 - 2\exp\left(-\frac{f\mu E_0}{2D_n}L\right)\cosh\left(\frac{a}{2D_n}L\right) + \exp\left(-\frac{f\mu E_0}{D_n}L\right)\right\}$$

$$X = -\frac{2pu_{0+}}{\varepsilon}\cdot\frac{1}{\left(P+\frac{\sigma_0}{\varepsilon}\right)^2 + Q^2}\left\{g_+\left(P^2+Q^2+P\frac{\sigma_0}{\varepsilon}\right) + Q\beta_+\frac{\sigma_0}{\varepsilon}\right\}$$

$$Y = \frac{2pu_{0+}}{\varepsilon}\cdot\frac{1}{\left(P+\frac{\sigma_0}{\varepsilon}\right)^2 + Q}\left\{Q\beta_+\omega - g_+\omega\left(P+\frac{\sigma_0}{\varepsilon}\right)\right\}$$

$$X' = -\frac{2pu_{0+}}{\varepsilon}\cdot\frac{1}{\left(P+\frac{\delta_0}{\varepsilon}\right)^2 + Q^2}\left(P^2+Q^2+P\frac{\sigma_0}{\varepsilon}\right)$$

$$Y' = -\frac{2pu_{0+}}{\varepsilon}\cdot\frac{1}{\left(P+\frac{\delta_0}{\varepsilon}\right)^2 + Q^2}\,\omega\left(P+\frac{\sigma_0}{\varepsilon}\right)$$

$$P = (\beta_+^2 - g_+^2)D_n - g_+\frac{fJ_0}{en_0}$$

$$Q = \beta_+\frac{fJ_0}{en_0} + 2g_+\beta_+ D_n$$

$$a = \sqrt{f^2\mu^2 E_0^2 + 4D_n\frac{\sigma_0}{\varepsilon}}$$

$g_+(=-\alpha_+)$ is the gain in the forward direction; $R_s(=1/G_s)$ is the d.c. resistance of the crystal.

On considering the expressions for m_1 and m_2 we find that m_1 is positive and m_2 is negative. Also, ψ_4 is positive, while ψ_3 is negative. Hence, the resistance of the crystal in the oscillating condition is, in general, less than its d.c. value.

The output power will be a maximum when the load Z_1 is a pure resistance equal to the self-resistance of the crystal and the magnitude of this maximum power is given by

$$W_{max} = \frac{1}{8}\frac{|v|^2}{R_s\left(1+\frac{\psi_4}{\psi_3}\frac{\sigma_0}{L}\right)} \qquad \ldots\ldots(16)$$

5. Discussion

We shall use the expressions deduced in the preceding sections to calculate the electrical power generated by a thin Cadmium Sulphide crystal of conductivity $\sigma_0 = 10^{-2}\,\Omega^{-1}\,\text{cm}^{-1}$.

Since $\varepsilon = 9{\cdot}5\,\varepsilon_0$ for CdS, we find that σ_0 is some twenty times larger than $\omega\varepsilon$ for $\omega = 2\pi\times10^8$ rad/s. Thus the condition $\sigma_0 \gg \omega\varepsilon$ is valid in this case. Taking $L = 0{\cdot}05$ cm, the simplified equations give a value of the internal impedance of the crystal equal to $R_s\,(1-1\times10^{-3})$, which indicates that the presence of the acoustic wave does not change the crystal impedance by an appreciable amount, for crystals of fairly large conductivities.

Furthermore, in order to evaluate the order of $|v|$, the e.m.f. of the oscillating crystal, we are required to know the attenuation characteristic of the crystal. We have seen that the condition of sustenance of acoustic oscillation in the crystal is that the total gain in the forward direction is equal to the attenuation in the reverse direction. Though the value of the attenuation constant α_- depends to some extent on the applied electric field and also on the various non-linear mechanisms occurring in the crystal, we may take its value roughly equal to that of the attenuation constant in the absence of any electric field. The attenuation constant[8] is approximately of the order of 2 nepers/cm (N/cm) in the frequency range 10 to 200 MHz. Thus, in the oscillating condition we have

$$g_+ = -\alpha_+ = \alpha_- = 2 \text{ N/cm}.$$

Further, we assume that the frequency of the acoustic oscillation is of the order of 100 MHz. The sound velocity for longitudinal waves in CdS may be taken as $4{\cdot}47 \times 10^5$ cm/s. Under this condition $\beta_+ \gg g_+$.

The voltage required to be applied for producing electron velocities exceeding the sound velocity is about 70 V for electron mobility of 300 cm^2/Vs. The efficiency of the oscillator as an electrical generator is thus of the order of 10^{-6}. One may hence conclude that an acousto-electric oscillator of dimensions and parameter values as considered here would have very limited applicability as an electrical power source.

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When the above-mentioned simplifying conditions are applied to eqn. (15), we obtain

$$|v| = \frac{2u_{0+}\,p}{\sigma_0}\left[\frac{\omega^4}{v_s^4}\{\exp(g_+L)-1\}^2\left(\mu^2E_0^2+D_n\frac{\sigma_0}{\varepsilon}\right)^2\frac{\varepsilon^2}{\sigma_0^2}+\right.$$
$$+\frac{\omega^4}{v_s^4}\frac{\varepsilon^2}{\sigma_0^2}\left(\mu^2E_0^2+4D_n\frac{\sigma_0}{\varepsilon}\right)\mu^2E_0^2-$$
$$-2\frac{\omega^4}{v_s^4}\{\exp(g_+L)-1\}\frac{\varepsilon^2}{\sigma_0^2}\left(\mu^2E_0^2+D_n\frac{\sigma_0}{\varepsilon}\right)\left(\mu^2E_0^2+4D_n\frac{\sigma_0}{\varepsilon}\right)^{\frac{1}{2}}f\mu E_0+$$
$$\left.+\omega^2\{\exp(g_+L)-1\}^2\right]^{\frac{1}{2}}$$

We have taken $f = 1$. The e.m.f. of the acousto-electric oscillator thus depends in a complex manner on the physical constants σ_0, μ, ε, p and v_s, the oscillation frequency ω and the applied field E_0, but it varies directly as the acoustic displacement u_{0+}.

Taking the value of the drift velocity μE_0 to be equal to the sound velocity and using $p = 0{\cdot}2$ coulomb/metre^2 (C/m^2), we obtain for the electrical voltage for an amplitude of acoustic vibration of u_{0+} metres

$$|v| = 2{\cdot}6\times10^7\,u_{0+} \text{ volts}$$

For an acoustic displacement of the order of 10 Å, $|v| \simeq 26$ mV.

We also find that the maximum output power is

$$W_{\max} = \frac{1}{8R_s}\times 6{\cdot}76\times10^{14}\,u_{0+}^2$$

$W_{\max}$ is in watts for R_s in ohms and u_{0+} in metres. Thus, for a crystal of dimensions 2 mm × 2 mm × 0·5 mm, the power output for acoustic vibration of an amplitude of 10 Å is 1 µW.

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New British Satellite Communications Earth Station

The Post Office has brought a new aerial system into service at its Goonhilly Earth Station to work with the new *Intelsat III* satellite, less than seven years after Goonhilly 1's first experiments with *Telstar*. The new installation, Goonhilly 2, will be the main Post Office Earth station in the expanding system of global communications via *Intelsat III* satellites in synchronous orbits over the Pacific, Atlantic and Indian Oceans. Goonhilly 1 is being re-equipped to communicate with countries to the East and will come back into service as soon as an *Intelsat III* satellite is available over the Indian Ocean. Meanwhile the new aerial will cater for a further expansion of the transatlantic service. This has become possible because an *Intelsat III* satellite has been substituted for *Early Bird* over the Atlantic Ocean. Whereas *Early Bird* is capable of linking together only two Earth stations and handling no more than 240 telephone conversations or one television programme, the *Intelsat III* satellites have facilities which provide flexible interconnections between a multiplicity of Earth stations, as required. Each satellite can carry a total of 1000 telephone conversations and relay one colour-television programme simultaneously. Initially, Goonhilly will operate telephony circuits to only the U.S.A. and Canada but as more Earth stations become operational the system will expand until, by 1971, Goonhilly is expected to be working to twenty countries.

The new installation at Goonhilly, which meets the technical requirements of the International Telecommunications Satellite Consortium (INTELSAT), has been built to a Post Office specification and installed at a total cost, including roads, buildings, etc., of approximately £2 million. The Marconi Company were the main contractors. Threshold extension demodulators and certain other equipment have been supplied and installed by G.E.C.–A.E.I. (Electronics) Ltd. The 90-ft diameter aerial built by The Marconi Company and based upon a design commissioned by the Post Office from their consulting engineers, Husband and Company, is the largest and most expensive item. The present aerial follows the pattern established by the first Goonhilly installation of dispensing with a radome. This practice has since been followed by most other Earth station designers.

The aerial makes use of a Cassegrain configuration with a spinning horn at the apex of the main reflector. The spinning feed-horn is a feature of Marconi's 'mode conversion scanning system' of aerial steering. It introduces a conical scan of the aerial beam only at the frequency of the satellite beacon signal. Thus it avoids unwanted amplitude modulation of the communication carriers or significant degradation of aerial efficiency for either direction of transmission. By this means auto-tracking can be achieved either by servo control of the main reflector mounting or, within a range of about ± 20 minutes of arc, by deflection of the sub-reflector. Provision has also been made for control of the aerial manually and for the addition of tape control facilities later, if required. Motor-driven bogies running on a circular track rotate the whole aerial about a central pivot and tilting of the reflector about its low-level elevation axis is controlled by a single horizontal screw and cross-head linked by a massive connecting rod to the upper part of the strong back of the reflector. Both driving mechanisms are powered by duplicated thyristor-controlled d.c. motors operating via differential gearboxes.

The aerial and telecommunications equipment are controlled and monitored from a suite of consoles in the central building. Each carrier, which may transmit up to 132 telephony channels, is monitored separately and reserve equipment is switched into use automatically if a disabling fault condition arises.

A microwave radio link from Goonhilly extends the satellite circuits to the International Telephone Services Centre in London. In the central building at Goonhilly, the circuits are rearranged at baseband frequencies into units of 24, 60 or 132 channels as dictated by traffic requirements. Each baseband unit then modulates an intermediate frequency of 70 MHz in the modulator section of the equipment. Inter-site coaxial cables transmit the modulated i.f. carriers to the equipment on the aerial where they are converted individually to their assigned radio frequencies. All carriers are then combined at low power level before amplification, in two stages, by common wideband travelling-wave-tube amplifiers. The output stage has a maximum c.w. capability of 8–10 kW but in order to restrict the power of unwanted intermodulation products it will not normally be loaded above 1·5 kW. A second transmitter which serves as a reserve for the telephony system, can be used alternatively for television transmissions. With the exception of the two travelling-wave tube amplifiers, solid-state circuits are employed throughout the transmitting system.

The very weak signals from the satellite in the 4 GHz band are amplified by a three-stage parametric amplifier, cooled to 160°K in a closed-circuit, gaseous-helium refrigeration system. The parametric amplifier consists of three identical gallium arsenide varactor diode stages connected in cascade. Each of these three stages is pumped by a klystron source connected through a three-way passive splitter. These klystrons provide 30 mW of pump power at 34 GHz. Except for these klystron-stages, the rest of the receiving system employs all solid-state circuits. A low-noise tunnel diode amplifier stage which is also contained in the same cryogenic package follows the three-stage parametric amplifier. The four stages have an overall gain of 40 dB over the 500 MHz frequency band assigned for the down path from the satellite. The effective noise temperature of the amplifier, referred to its input, is less than 20°K. At the output of the common amplifier the individual carriers are separated by a selective branching network, converted in frequency to 70 MHz and extended individually by coaxial cables to the f.m. feedback demodulators in the main building. Here, supervision is effected by monitoring the synchronizing pulses. The receiver covers the complete satellite communications band from 3700 MHz to 4200 MHz including all possible channels from both the *Intelsat II* and *III* type satellites, as well as from the *Early Bird* satellite.

Extensive provision of switched redundant equipment in the system and the comprehensive control facilities will ensure a high standard of reliability and enable maximum economy of operational manpower to be achieved.

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Flashover in Picture Tubes and Methods of Protection

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Summary: The aim of this paper is to bring forward and analyse phenomena occurring in a television receiver as a result of a flashover inside a picture tube, and to evolve a systematic approach to a method of protection. The paper first reviews the behaviour of a picture tube under flashover conditions, its effect on receiver circuitry, and a suggestion is made for a possible equivalent circuit. It then establishes a comprehensive method of protection against the large transients generated by a flashover which affect primarily a portion of the receiver directly connected to the base of the picture tube. This protection consists of a separate path for flashover currents, which is switched into circuit for the duration of flashover by means of spark-gaps assisted by series resistors. It is connected in such a way as to provide a minimum disturbance to the rest of the receiver. Further, the paper considers overloads imposed on the e.h.t. generator as a result of discharge of the e.h.t. capacitor by a flashover of the picture tube or other agency. Proposals are made for suitable limiters to protect the output transistor. Finally, a description of some measuring techniques of particular interest in flashover work is given.

1. Introduction

In the realm of side-effect problems with which a television designer has to cope nowadays, the flashover in the picture tube assumes ever-increasing importance. It is not because the performance of picture tubes has suddenly deteriorated; on the contrary, there has been a steady and continuous improvement. However, with increase of size of the picture tubes, there is a need for higher operating voltages and currents, the latter requiring a larger value of e.h.t. capacitor. Thus, while the tube technology kept pace with the increase in voltage, the increase in stored energy has to be accepted as a law of nature.

The flashover phenomena have existed in early television receivers, but only in the last few years has their effect been felt. No doubt the increase in energy has been a contributing factor, but so has been also the use of more advanced devices, more compact designs, chassisless construction and so on. More recently, introduction of semiconductors created, in a way, an incompatible situation—devices inherently sensitive to over-voltage are operated in a situation potentially prone to produce high voltage.

As to the need for flashover protection, there seems to be a whole spectrum of opinions, ranging from 'no difficulties ever encountered' at one end, to a plain statement that 'one would never dare to produce an all-transistor receiver' at the other. Strange as it seems, both extremes are right in their particular settings. However, in the majority of cases this arises from a conglomeration of fortuitous circumstances. The object of this paper is to analyse the problem, and, by design, to create a situation which will provide a full and consistent flashover protection.

2. A Brief Description of the Phenomenon and its Effects

A photograph of the picture-tube neck at the instant of flashover is shown in Fig. 1. In this picture, the tube is positioned vertically with the base pointing downwards. A bright spot visible between the focus electrode and the second anode is the discharge. The waveform of current flowing through the picture-tube during such a discharge is shown in Fig. 3. It is of the familiar shape associated with damped oscillations; the only point of interest is its maximum amplitude of about 700 A.

A sketch of the picture tube with the minimum amount of circuitry is shown in Fig. 6, and a simple equivalent circuit in Fig. 7. Logically the latter can be divided into two parts:

(i) Charging circuit, consisting of e.h.t. supply V of internal impedance R_i and picture-tube capacitance C.

(ii) Discharging circuit, consisting of capacitance C, total inductance L, total resistance R and a spark-gap G representing the interelectrode spacing of the gun structure.

The charging circuit is formed from the elements of the e.h.t. supply; its operational characteristic is

† Mullard Ltd., Central Application Laboratory, Mitcham, Surrey.

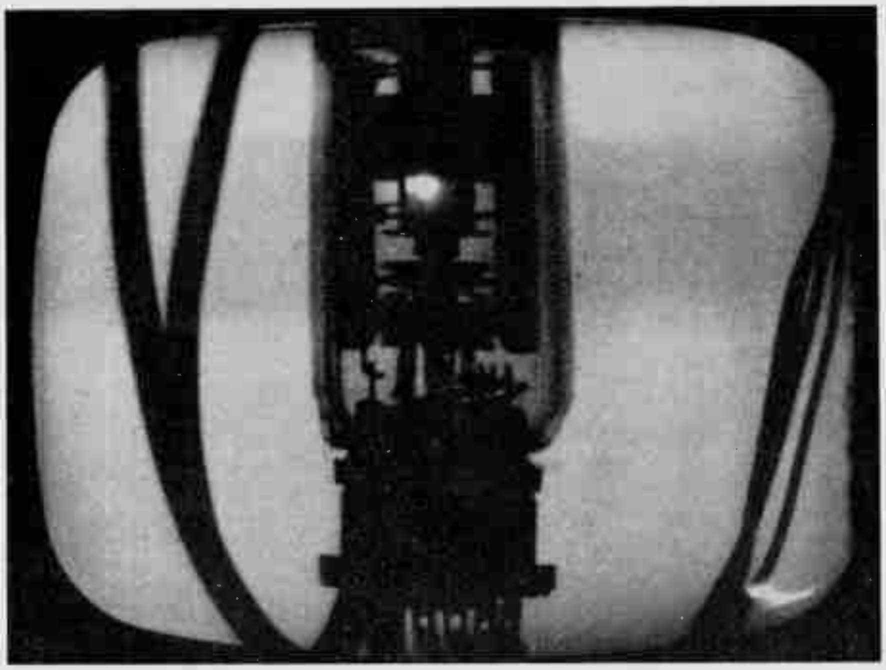


Fig. 1. Photograph of picture-tube gun at the instant of flashover (after Oxenham[1]).

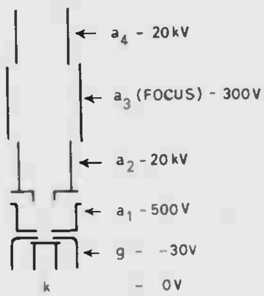


Fig. 2. A sketch of picture-tube gun.

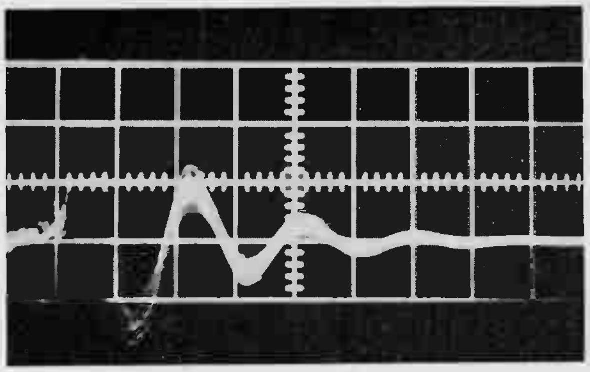


Fig. 3. Waveform of flashover current. $i = 200$ A/div; $t = 0{\cdot}1$ μs/div.

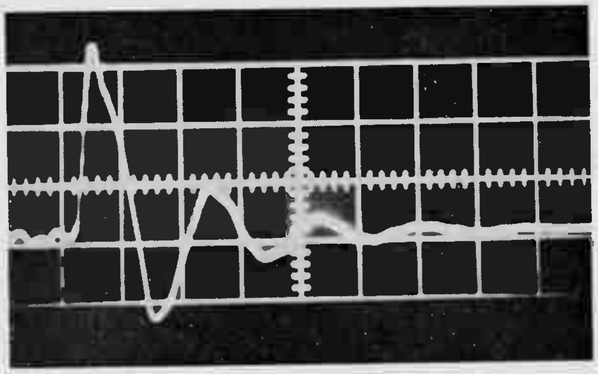


Fig. 4. Waveform of current produced by the flashover generator. $i = 200$ A/div; $t = 0{\cdot}1$ μs/div.

limited to d.c. and low frequencies; it is in action all the time the receiver is switched on. On the other hand, the discharging circuit is completed only for the duration of flashover when an arc develops across gap G. It is essentially of an oscillatory nature. In this circuit, the e.h.t. capacitor forms a large store of energy and the e.m.f. is that of the e.h.t. supply. Thus, large voltages and currents can be expected. Since the external circuitry forms a part of the oscillatory circuit, these voltages and currents appear across various components which, as a rule, are not designed to cope with them. A waveform of voltage appearing across 25 cm of wire connected between the tube base and the external conductive tube coating ('Aquadag'†) is shown in Fig. 5.

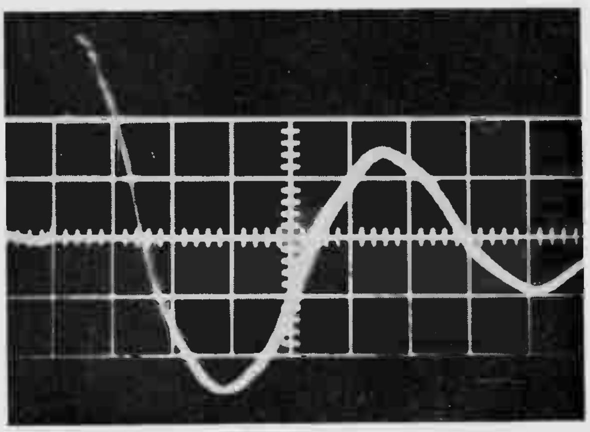


Fig. 5. Voltage developed across 25 cm of wire connected between the tube base and external coating. $v = 2$kV/div; $t = 30$ ns/div.

† Aquadag: aqua-deflocculated Acheson graphite.

In a system with a fixed gap spacing, the only way an arc can be terminated is by self-extinction; that is, when the current falls below a value sufficient to sustain the arc. In the case under discussion, this implies that the voltage across capacitor C must fall to practically zero and the capacitor itself must be nearly completely discharged.

Thus the effects of flashovers on the circuitry of a television receiver can be divided into two groups:

(i) Injection of transient energy into the circuits connected to the low voltage electrodes of the picture tube.

(ii) Overload of the e.h.t. generating circuits during the recharging of the e.h.t. capacitor discharged by a flashover (or any other agency).

This is only a rough division; the transients can penetrate right into the line time-base circuits, causing damage there, and equally other supplies (particularly the a_1 and focus) may suffer from overloads produced by recharging of the output capacitors. In addition, large currents may circulate in the chassis and the resulting potential differences can alter significantly the operating conditions of transistors in various parts of the receiver.

3. Flashover Behaviour of Picture Tubes

3.1. *Breakdown Mechanism*

Picture tubes, in common with other high-vacuum devices, are prone to internal flashover. As yet, there is no generally agreed theory which explains the mechanism producing the high temperature required for generation of vapour in which the arc is formed. It is likely that under the influence of electrostatic forces minute particles are detached and transported across the interelectrode spacing; the energy released on impact may set off a chain of events leading to formation of the arc. Random occurrences of flashovers and a return to normal operation after only one discharge seem to support this theory.

3.2. *Flashover Paths*

A sketch of the picture-tube gun structure with a unipotential lens is shown in Fig. 2. There are three electrode spacings with a potential difference of practically full e.h.t. value: a_4 to a_3, a_3 to a_2 and a_2 to a_1. Each of them is a possible path for flashover currents. The focus electrode, with high-potential gaps at both ends, is particularly exposed to flashover. A discharge of this type is shown in Fig. 1.

A flashover can also occur along the structures supporting the electrodes. Perhaps contrary to expectation, in such cases the discharge does not terminate at the neighbouring electrode but travels the length of the structure and unloads itself into one of the pins on the foot of the picture-tube.

On rare occasions, a flashover may travel along the glass surface inside the neck. Again it is usual for the discharge to terminate at the foot of the tube.

Thus, by means of one or more of these routes, a flashover may reach every pin on the tube base. While the number of discharges received varies from electrode to electrode, none of them is completely free from flashover.

In spite of a plurality of paths, the e.h.t. capacitor is the only source of energy. A discharge across one of the paths automatically removes the potential difference from the remainder. This is a fortunate situation, for there is some evidence to indicate that a flashover across one of the gun spacings lowers the breakdown voltage across the other spacings.

3.3. *Frequency of Occurrence*

With production samples of picture tubes, flashovers occur at random intervals and are well separated in time. In fact, this property is a serious obstacle in the development of an improved product. The only meaningful approach is on the basis of statistical analysis, and this calls for a large number of samples each time a new approach is tried.

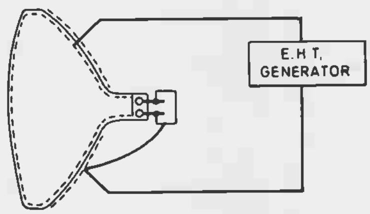


Fig. 6. A sketch of a picture tube with minimum of external circuitry.

However, there are some patterns of behaviour. A tube taken fresh from stock may produce a few discharges at first, but it soon settles down. There is a general tendency towards longer intervals as the life progresses. An exception is a tube with a cracked rod, or 'soft'—but such faults are rare nowadays.

A reduction in e.h.t. below the specified value for the tube will reduce the number of discharges; the converse is also true. Rapid changes in the e.h.t. potential, or mechanical shock, can induce a flashover.

With modern picture tubes the frequency of flashover is sufficiently low to pass unnoticed by the viewer; the problem, however, is of vital importance to circuit designers, particularly when semiconductor devices are involved.

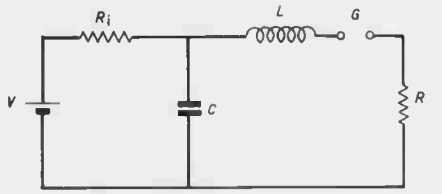


Fig. 7. A simple equivalent circuit of a picture tube under flashover conditions.

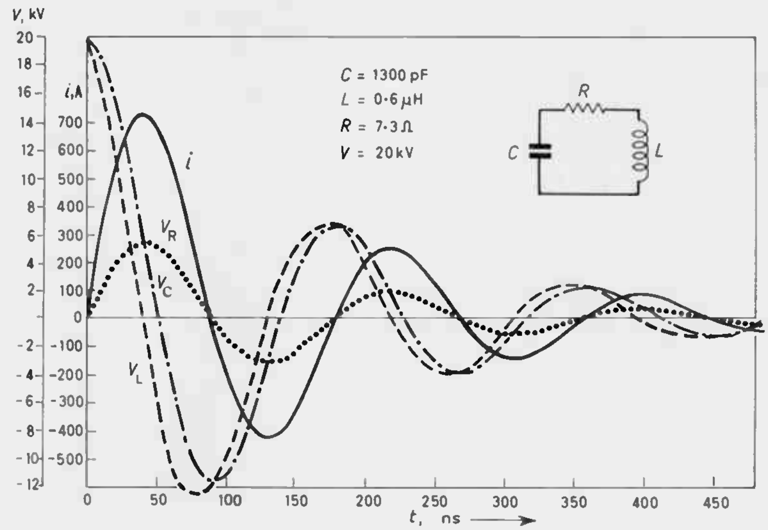


Fig. 8. Waveforms of the simple equivalent circuit.

3.4. *Consequences*

As a consequence of flashover, a receiver may suffer damage ranging from nil to a complete disablement, and there is even a remote possibility of fire. Fortunately, a receiver without any protection has a host of incidental spark-gaps such as spacing between pins of the tube or a valve, tagboards, neighbouring conductors, and so on. In the presence of high voltages generated by flashover, a breakdown occurs across one or more of them and thus a discharge path is established to the external coating of the tube. With receivers fitted with valves, a flashover in such a situation is harmless in most cases. However, with repeated discharges, some components may be weakened, leakage paths can develop and the performance of the receiver may suffer. In exceptional circumstances an arc generated by a flashover can bridge a gap across a store of high energy such as the smoothing capacitor of the h.t. supply. A repeated flashover of this nature can cause mechanical damage by distorting or evaporating conductors, charring insulators and so on.

While incidental spark-gaps contribute to the safety of a receiver, their performance is unpredictable and may vary considerably even between samples of the same model. A slight change during a production run can cause considerable deviations. In order to introduce some organization into this uncontrolled situation, a design was evolved which ensures that the flashover currents are directed back to the external conductive tube coating along well-defined paths and with minimum disturbance to the rest of the circuitry. The solution developed in this paper may be of some benefit to receivers fitted with valves, but it is of particular interest for receivers using semiconductor devices.

3.5. *Equivalent Circuit*

3.5.1. Analysis of the simple equivalent circuit

A better understanding of flashover problems may be gained from the analysis of the simple equivalent circuit shown in Fig. 7. Of primary importance in this consideration is the discharging portion. In most cases the function of capacitance C is served by the picture tube capacitance formed by the internal conductive layer and the outside conductive layer, with the glass of the cone serving as a dielectric. The value of the capacitance so formed is a function of the picture tube size and the energy stored depends also on the operating potential. The relevant data for two monochrome and two colour picture tubes currently in use are given in Table 1.

Table 1

Tube capacitance, charge and energy stored for several current types of picture tubes

Tube type	V kV	C nF	Q μC	E J	Metal band C_b pF
A47-11W	20	1—1·5	20—30	0·2—0·3	250
A59-11W	20	1·7—2·5	34—50	0·34—0·5	350
A49-11X	25	1·5—2·0	37·5—50	0·47—0·62	300
A63-11X	25	2·0—2·5	50—62·5	0·62—0·78	500

Every time there is a flashover the picture tube is practically completely discharged: while the value of peak current is a function of external circuitry, the charge transferred and the energy involved must be the same.

Since the capacitance C is an integral part of the tube, the amount of associated inductance and resistance is small. For the A47-11W tube, the following circuit constants were established: $C_p = 1{\cdot}3$ nF, $L_p = 0{\cdot}38\ \mu$H, $R_p = 6{\cdot}3\ \Omega$.

In order to complete the discharge circuit it is necessary to provide an external connection between the tube base and the outer coating. Because of the physical distances involved, the connecting wire can seldom be less than 25 cm, and its self-inductance between 0·2 and 0·25 μH. Assuming a current sampling resistor of 1 Ω, the electrical constants of the discharge portion of the circuit in Fig. 7 are as follows: $C = 1{\cdot}3$ nF, $L = 0{\cdot}6\ \mu$H, $R = 7{\cdot}3\ \Omega$.

The discharge loop is described by the following differential equation:

$$Ri + L\frac{di}{dt} + \frac{1}{C}\int i\,dt = 0 \qquad \ldots\ldots(1)$$

In the case under consideration

$$\frac{1}{LC} > \frac{R^2}{4L^2}$$

and the complete solution is:

$$i = \frac{V}{\omega' L} e^{mt} \sin \omega' t \qquad \ldots\ldots(2)$$

where

$$m = -\frac{R}{2L} \quad \text{and} \quad \omega' = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}$$

The peak values of current occur at

$$t_{i\,pk} = \frac{\tan^{-1}\left(-\dfrac{\omega'}{m}\right)}{\omega'} + n\frac{\pi}{\omega'} \qquad \ldots\ldots(3)$$

Substituting in eqn. (2) for t, the maximum values of current may be found. For the circuit considered the highest current value is 730 A. A graph of the current waveform and the associated voltage waveforms is shown in Fig. 8. Since this is a series circuit, the same current is flowing through the picture tube and the external wiring. With such a large value of current even a small value of resistance will produce a large voltage drop.

With reference to eqn. (1) and Fig. 7, at $t = 0$ $i = 0$, hence:

$$L\frac{di}{dt} = \frac{1}{C}\int i\,dt = V \quad ; \quad \frac{di}{dt} = \frac{V}{L}$$

Substituting for V and L, the initial rate of change of current is 3×10^{10} A/s. The equation also indicates that initially all the voltage appears across the inductive portion of the circuit. The voltage on the external circuit is a function of the ratio of the external inductance L' to the total inductance, that is:

$$v' = V\frac{L'}{L}$$

Even for the shortest connection between the tube base and the outer coating, $L'/L = \frac{1}{3}$, therefore a large proportion of the e.h.t. voltage will be present in the external circuit.

If it so happens that a capacitor C' is connected in series with the external circuit, then at the end of the transient period the charge stored in the tube capacitance will be shared, resulting in the final voltage across C' of:

$$v' = V\frac{C}{C+C'}$$

For $C' \ll C$, practically full e.h.t. voltage will appear on C'.

The natural frequency of the discharge circuit is 5·7 MHz, which falls just outside the video frequency range. For larger tube sizes or where the connection to the outer coating is long, it falls within the video frequency band.

Insertion of a resistor in series with the external connection will produce a drop in the peak current, but the duration of the transient will be lengthened to allow for practically total discharge of the e.h.t. capacitor.

In this case

$$\frac{1}{LC} < \frac{R^2}{4L^2}$$

and the solution for current is:

$$i = \frac{V}{R\beta}\left[e^{(1-\beta)mt} - e^{(1+\beta)mt}\right] \qquad \ldots\ldots(4)$$

where

$$\beta = \sqrt{1-\left(\frac{\omega_0}{m}\right)^2} \quad \text{and} \quad \omega_0 = \sqrt{\frac{1}{LC}}$$

and the maximum current occurs at

$$t_{i\,max} = -\frac{\log_e \dfrac{1+\beta}{1-\beta}}{2m\beta} \qquad \ldots\ldots(5)$$

If

$$\frac{1}{LC} \ll \frac{R^2}{4L_2}$$

then

$$\beta = 1 - \frac{1}{2}\left(\frac{\omega_0}{m}\right)^2 \simeq 1$$

In this situation

$$(1-\beta)mt = -\frac{t}{CR}$$

and

$$(1+\beta)mt = -\frac{R}{L}t$$

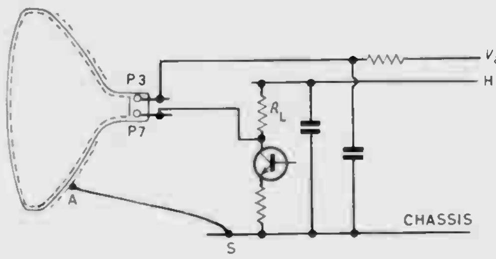


Fig. 9. Layout of picture-tube and some components on the chassis.

Substituting in eqn. (4)

$$i=\frac{V}{R}\left[e^{-\frac{t}{CR}}-e^{\frac{Rt}{L}}\right] \qquad \ldots\ldots(6)$$

Since

$$\frac{1}{LC} \ll \frac{R^2}{4L^2}$$

then

$$CR \gg \frac{L}{R}$$

Therefore, the build-up of current is controlled by the time-constant L/R and can be written as

$$i_b=\frac{V}{R}\left(1-e^{\frac{-Rt}{L}}\right) \qquad \ldots\ldots(7)$$

Similarly, the decay of current is controlled by the time-constant RC and can be expressed as:

$$i_d=\frac{V}{R}e^{-\frac{t}{CR}} \qquad \ldots\ldots(8)$$

Under these conditions the maximum current is simply

$$i_{max}=\frac{V}{R}$$

and the time at which it occurs is

$$t_{i\,max}=2{\cdot}3\frac{L}{R}\log\frac{C}{L}R^2$$

With an increase in R, the ratio L/R varies much faster than log R^2, therefore there is a reduction in time within which the maximum current occurs.

3.5.2. Further development

A lay-out of a picture tube with some representative components on the chassis is shown in Fig. 9. An equivalent circuit using discrete components is presented in Fig. 10. A clear distinction is made between the components belonging to the e.h.t. generator, the tube itself, and the circuitry connected to the tube base. In the latter section connecting leads are shown as inductances. Pins P3 and P7 represent pins of the picture tube (monochrome) which are connected to a_1 and cathode respectively. All the components connected to a given pin bear the same number as the pin. The point of contact with the external tube coating is represented by A and the point on the chassis from which connection is taken to the coating by S; the connection itself is L_a.

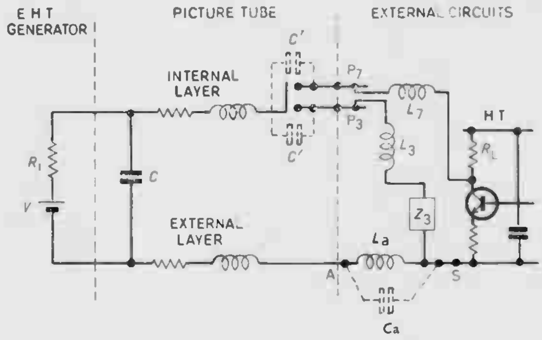


Fig. 10. Equivalent circuit—discrete components.

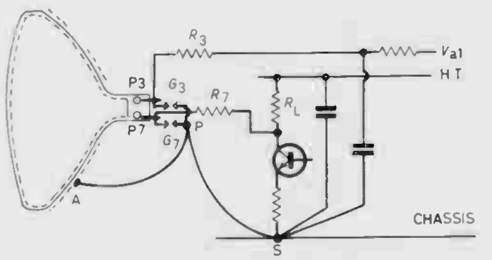


Fig. 11. Basic flashover protection circuit.

The equivalent diagram shows a new component, C_a, which represents capacitance between the outer coating and the chassis. In monochrome receivers it was found to be between 15 and 25 pF.

4. Flashover Protection of Low-voltage Circuits

4.1. *Principles of the Protection Circuit*

A transistor operating in a video output stage is shown in Fig. 9. It has a direct connection to the cathode-pin of the picture tube. In the event of a flash-over inside the tube to the cathode the resulting arc provides a direct connection between the collector and the e.h.t. line. Both the voltage and the energy impressed upon the transistor are outside its limits and a failure is inevitable.

While it is possible to devise some methods of protection around the transistor, there is always a danger that the flashover transient may get into the wiring of the receiver and cause damage to other components. For this reason, it is prudent to apply protective measures directly at the tube-base. An obvious choice is a separate flashover by-pass path connected between pin 7 and the outer coating. If it is made as short as possible, its impedance should be much smaller than the impedance of the path via the transistor and the current reaching the transistor will be correspondingly reduced.

For such a by-pass path to be a workable proposition, it is necessary to provide a device which, in the event of flashover, will automatically switch pin 7 from the transistor to the by-pass connection. Unfortunately, such a change-over switch is not feasible at present and the nearest other choice is a spark-gap connected in series with the lead from P7 to the external tube coating.

It is well known that the action of any spark-gap can be speeded-up by application of overvoltage. The necessary potential difference can be produced by the insertion of a resistor in series with the lead to pin 7. In the initial stages of flashover, the current will flow through the resistor (and transistor) producing a large voltage across the spark-gap. Once an arc is established, the bulk of the current will pass through the spark-gap.

As a result of a large current flowing through the by-pass path, a large voltage will appear across it. With a conventional connection between the chassis and the external tube coating (Fig. 9, points S and A), this voltage will be impressed on the receiver circuitry. A considerable improvement can be effected by taking the connection from the chassis to the tube-base (point P in Fig. 11). With the rearrangement (and in the presence of connection PA), there is still a d.c. path to the outer coating, but the voltage appearing on the flashover by-pass connection PA is eliminated from the receiver circuitry. In fact, the effectiveness of this connection is lessened by the stray capacitance between coating and chassis. Nevertheless, a useful improvement can be ensured under practical conditions.

Thus, the constituent components of the flashover protection circuit are: a short connection between the tube-base and the outer coating, a spark-gap, a resistor in series with the supply lead to the pin, and routing of connection from the chassis to the tube-base, point P, instead of directly to the coating. The circuit diagram embodying these components is shown in Fig. 11. In practice, every pin of the tube-base should be protected, but for the sake of simplicity only two pins are shown. In order to ensure the speed of operation, resistors R and spark-gaps G should be mounted close to the tube socket; all the spark-gaps should be returned to point P, which should also be located close to the tube socket.

It will be noted that only one connection is used between the tube-base and the outer coating. A flashover passing through any pin will produce a large potential across this connection, and normally, there would be a danger of secondary discharges in the neighbouring spark-gaps. However, with connection SP between the chassis and the tube-base, as shown, this possibility is avoided.

4.2. *Characteristics of Spark-gaps*

Spark-gaps for flashover protection should have a hold-off voltage well in excess of d.c. potential at which the electrodes of the picture-tube are working. In practice, the same spark-gaps are used for all electrodes of monochrome and colour tubes, with the exception of the focus electrode of the colour tube. Taking into account mechanical tolerances, and the need to guard against a possibility of a leakage developing with time, the electrode spacing of a spark-gap normally used is between 0·3 and 0·5 mm. This results in a d.c. breakdown voltage of 2 to 3 kV. A spark-gap for the focus electrode of a colour tube may have a spacing of 5 to 6 mm, and a d.c. breakdown voltage between 6 and 8 kV. Under pulse conditions, the breakdown voltages are much higher than at d.c., and typical characteristics are shown in Fig. 12.[2]

The breakdown voltage of a spark-gap is a function of atmospheric conditions and the state of electrode surfaces. With a moderate value of the series resistor, a large over-voltage is produced and consequently the

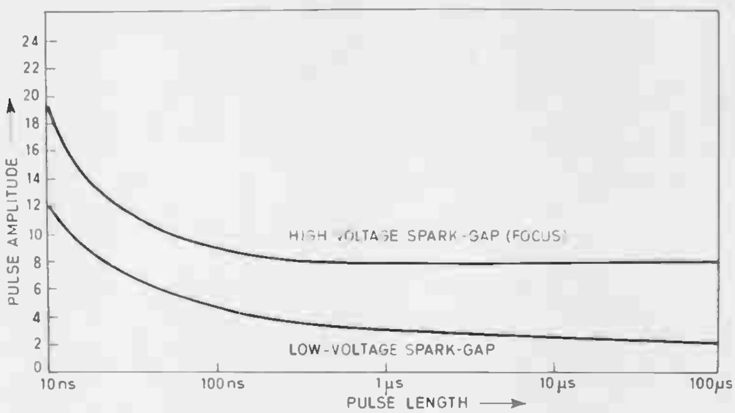
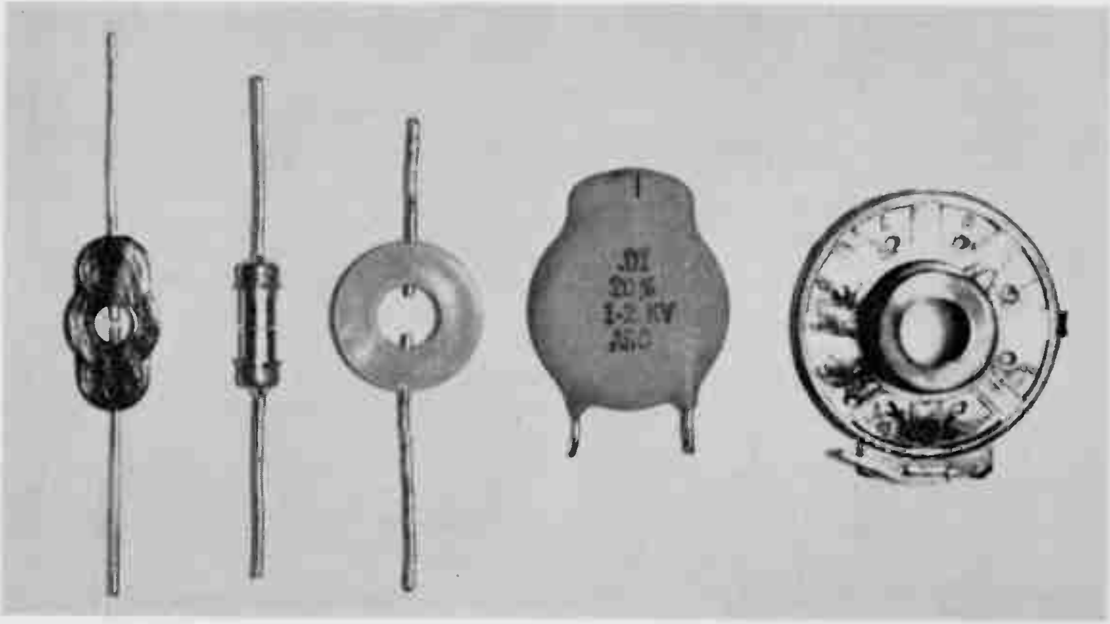
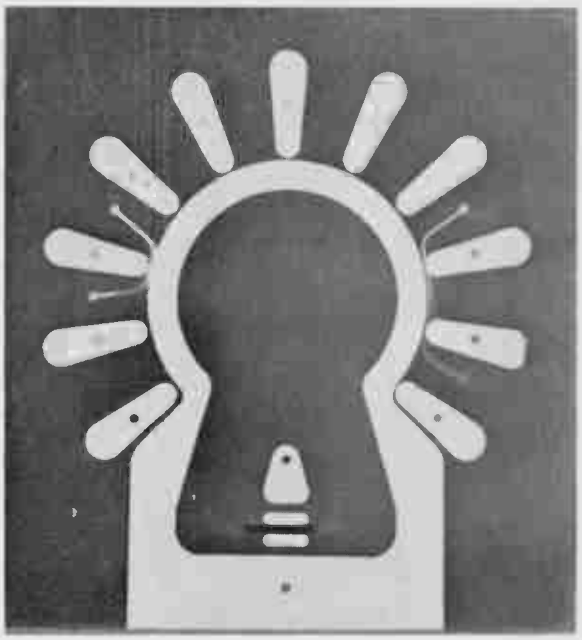


Fig. 12. Breakdown characteristics of spark-gaps.
Pulse amplitude (in kV) vs. pulse length.



(a) (b) (c) (d) (e)

(a, b) Low-voltage spark-gaps. (c) High-voltage spark-gap. (d) 'Cap-Gap'. (e) 'Sparkguard' base.



(f) Printed spark-gap for colour tube.

(g) 'Ring-trap' base.

Fig. 13. Spark-gaps used for flashover protection.

circuit is reasonably tolerant of variation in the performance of the spark-gaps. In practice, there is no need to take special precautions, apart from some protection against accumulation of dust or other deposits. A spark-gap designed for operation in air should not be enclosed in an airtight compartment. Nitrous products formed in the presence of an arc, if not dispersed, can affect performance. Similarly, a printed spark-gap should not be covered by lacquers or soldering resins.

A spark-gap should be able to handle flashover currents without a change in its characteristic. The state of the spark-gap after 1000 discharges under operating conditions can be taken as a measure of its suitability. Parameters to be checked are: d.c. breakdown and insulation resistance.

Several types of spark-gaps already in use in television receivers are shown in Fig. 13. The first two are low-voltage spark-gaps; the one shown in Fig. 13(a) consists simply of two pieces of wire held in a plastic mount, and Fig. 13(b) is two cylinders pushed on to a ceramic tube. In Fig. 13(c) is shown a spark-gap for protection of the focus electrode of colour tubes. A combination of a spark-gap and a capacitor ('Cap-Gap') is shown in Fig. 13(d).

In most cases, spark-gaps used in the television industry are operated in free air. Occasionally, one finds some enclosed in an inert atmosphere. There is a whole range of sophisticated devices used in industrial applications which would be ideally suited for television receivers were it not for their cost.

A multiple printed circuit spark-gap designed for colour tubes is shown in Fig. 13(f). The large common electrode is easily recognizable, and so is the electrode for the focus pin, by its special isolation from the rest. The operating condition of the latter is rather finely balanced; it must have a high d.c. breakdown voltage and yet the available potential difference during the initial breakdown stages is the lowest ($V_{\rm eht} - V_{\rm foc}$). To speed up its action, two isolated electrodes are provided (de-ion principle). Spacing of the main electrodes is 6 mm and a d.c. breakdown 7 kV. For the remaining spark-gaps 0·3 mm spacing is used with a d.c. breakdown of 3 kV. Note the slits cut into the supporting base between electrodes of focus and first anode spark-gaps in order to remove any possibility of leakage developing with time.

There is an obvious advantage in having a picture tube provided with the necessary spark-gaps. Unfortunately, the same mechanism which makes a picture tube unpredictable in respect of flashover would still be operative in the case of any spark-gap enclosed in vacuum. Thus an integral spark-gap has to be located outside the envelope, and the obvious choice is the base. A base of this type, incorporated into monochrome tubes, is shown in Fig. 13(e). It has a piece of metal inserted into the space between pins 3 and 4 (first anode and focus). The metal strip forms a common electrode and the pins themselves the other two electrodes. On the outside, the metal strip is bent at right angles and follows the contour of the base in order to allow an unobstructed passage for deflection coils. There it is formed into a flat pin so that a push-on contact can be used to provide a connection to the external tube coating. This base, when used with a suitable circuit, provides an effective flashover protection for discharges appearing on pins 3 and 4.

Another approach to the multiple spark-gap system integral with the picture tube is the 'ring-trap' base shown in Fig. 13(g). The portion facing the reader is the underside of the base, which covers the foot of the tube and normally is not visible to the user. In the centre of it can be seen a piece of wire shaped into practically a complete circle. One end of it is bent to a right angle and passed through a vacant hole No. 5 in the base to form an additional pin. The assembly is pressed into the recess around the space provided for the tube exhaust seal. When the base is fitted on to the foot of the tube, the pins occupy their normal places and form seven spark-gaps with the wire serving as a common electrode.

The spacing between the common electrode and the pins is governed primarily by the distance between the pins and the recess—the tolerance of the wire is of no importance; any small variation in the diameter of the ring is taken up by the elasticity of the wire. The original base had to be modified to give the required spacing of 0·5 mm. Provision was made to hold the wire in position by means of three prongs. Some material between the pins and wire was removed to ensure an unobstructed air space around the areas in which the arc is expected to form. Due cognizance was taken of the fact that the majority of discharges occur to the focus electrode and the first anode by bending the wire in the direction of those pins (4 and 3). With the base fitted on the foot of the tube there is enough space to allow circulation of free air, but there is some shielding against ingress of dust. Close location to the heater of the tube provides for a dry atmosphere.

4.3. *The Series Resistor*

In addition to providing favourable conditions for the breakdown of a spark-gap, the series resistor performs other useful functions. During the pre-breakdown moments it limits the amount of current flowing into the portion of receiver circuitry connected to the pin. A further limitation of transients reaching the receiver is obtained by the action of the resistor in conjunction with any capacitance (stray capacitance, output capacitance of a valve or a transistor) as a low-pass filter. Once the spark-gap is conductive, it represents a low-impedance path not only for flashover currents, but also to the supply feeding the electrode. The series resistor limits the amount of current flowing out of the supply.

As a result of transient currents flowing out of the pin, voltages are built up not only across the resistor but also on any series impedances. Thus, they can appear in various places in the receiver. To guard against such a contingency it is advantageous, where-ever possible, to provide some decoupling after the series resistor (see Fig. 11).

The maximum value of the series resistor is limited by such considerations as the bandwidth requirements, maximum permissible electrode impedance and so on, and the minimum value by the need to provide sufficient protection to the devices in the receiver, and to ensure a self-quenching action for the energy flowing from the supply to the pin. The resistor, and its mounting, must be able to handle high voltages without a breakdown or a reduction in the value of resistance. Satisfactory results were obtained with carbon composition resistors.

4.4. *Evaluation of Breakdown Voltage*

In the initial stages of flashover, the current is flowing through the series resistor via the rest of the circuitry and back to the outer conductive coating. Thus, the path taken (in its simple form) can be compared with a series resonant circuit. In this circuit, the resistor represents the largest resistive component, let it be 1 kΩ. For a monochrome tube, the other components can be taken as $L = 1$ μH, $C = 1300$ pF, $V = 20$ kV. The current flowing in such a circuit is given by eqn. (6), and the voltage across the resistor is obtained by multiplying it by R, that is:

$$v_R = V\left[e^{-\frac{t}{CR}} - e^{-\frac{Rt}{L}}\right] \qquad \ldots\ldots(9)$$

With the values assumed, $L/R = 1$ ns and $CR = 1{\cdot}3$ μs.

A plot of this equation together with spark-gap characteristics is shown in Fig. 14. With a logarithmic time-scale it represents a rather unfamiliar shape.

Considering this curve and the breakdown characteristic of the low-voltage spark-gap, it is obvious that the ignition of the spark-gap cannot occur any earlier than about 6·8 ns. At that time, the voltage dwell across the spark-gap at the 20 kV level is zero. An arbitrary value of $t = 10$ ns gives a voltage dwell time at 20 kV of $10-6{\cdot}8 = 3{\cdot}2$ ns, which is too short, and at 18 kV of $10-2{\cdot}3 = 7{\cdot}7$ ns, which is too long in comparison with the required voltage dwell of 7 ns at 18 kV.

Selecting now a shorter time, say 9 ns, we have:

Voltage, kV	20	19	18	17	16	14	12	10
Time of dwell, ns	2·2	5·9	6·7	7·1	7·4	7·8	8·1	8·3

The time of dwell is shown in Fig. 14 by means of a dotted curve. This curve is coincident with the spark-gap characteristic at about 16 kV. Therefore, it suggests that the breakdown occurs at 9 ns and 16 kV.

Obviously, this is rather an oversimplified view of a complex problem. However, spark-gap characteristics are often published in terms of breakdown voltage as a function of time and this approach allows some tentative assessment.

Using this method, it can be shown that the breakdown voltage for the high-voltage spark-gap of Fig. 13(f) is 19 kV and it occurs at 13 ns. If the voltage applied to the picture tube is reduced to 10 kV, the low-voltage spark-gap fires at 9 kV after 17 ns, and the high-voltage spark-gap at 9 kV after 100 ns. Note the increase in the time at which the breakdown occurs.

With a reduction in the value of series resistance, there is a slowdown in the rate of voltage build-up and a faster decay. Therefore, smaller values of R need more accurately designed spark-gaps.

Another store of energy is the capacitance between the deflection coils and the internal conductive layer of the picture-tube. It would be desirable for one end of the line deflection coils to be directly connected to chassis. However, the need to reduce r.f. radiation may dictate a balanced connection to the line output transformer. In such a case, the best that can be done is to provide a low-impedance path via the shortest possible route to the outer conductive coating.

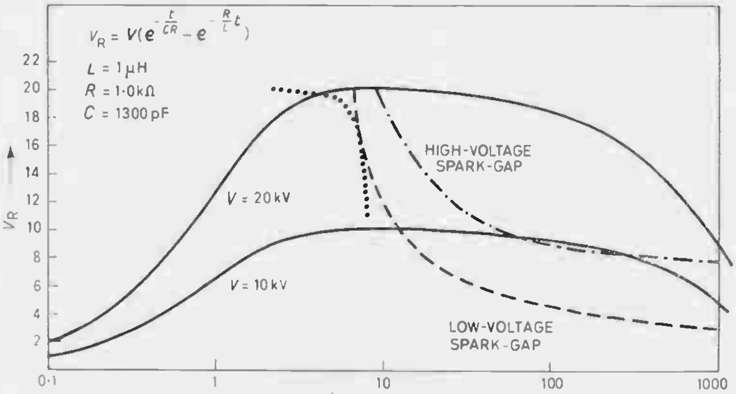


Fig. 14. Evaluation of breakdown voltage. V_R (in kV) vs time (in ns).

4.5. *Protective Measures and Semiconductor Devices*

An unprotected semiconductor device (a diode or a transistor) supplying one of the pins on the tube base is bound to be damaged by a flashover, unless it is specifically designed for operation at high voltages. If it is a diode, the failure will occur irrespective of the polarity of connection. The situation is altered considerably when a resistor is connected in series with it. If the resistor is of a moderate value (several kilohms), most of the voltage will be developed across it and it will consume most of the energy. When the diode is forward biased by the flashover current, the voltage drop across it will be much smaller than when the diode is connected in the reverse direction. This is the reason why the flashover protection of a reverse biased junction is so difficult.

Given a series resistor of sufficiently high value, it should be possible to protect any junction. Such a resistor may not be acceptable on the grounds of bandwidth requirements, or may be too high for the picture tube to operate satisfactorily. Even if it is acceptable, it solves only part of the problem since the resulting high voltages will try to find another outlet.

In Fig. 15 is shown the characteristic of a video transistor and a load line of the series resistor. The voltage v, varies with time as shown in Fig. 16, and is given approximately by eqn. (9) (and also Fig. 14). Its peak value is equal to the e.h.t. value. When the flashover protection is augmented by a spark-gap, the voltage assumes the waveform represented in Fig. 16 by a thick line. Note the reduction in duration of the voltage obtained by the action of the spark-gap, and the corresponding fall in dissipation. Furthermore, since the duration of voltage transient is very short, the filtering action of the resistor and self-capacitance of the transistor is effective. Consequently, the voltage reaching the device may be only a fraction of the voltage applied to the resistor.

Thus for the same degree of protection, the presence of the spark-gap permits a reduction in the value of series resistor (by about one order of magnitude).

Note a negative overswing in the waveform. With the complexities of practical circuits, such an overswing is bound to appear at the collector. Reverse voltage at the collector produces a forward bias on the collector-base junction. If the impedance between base and emitter is high, the resulting voltage can be high enough to damage the base-emitter junction. Alternatively, the voltage can travel to the preceding transistor and cause damage there. This is one of the reasons for keeping the base-emitter impedance low (another is the fact that for a video transistor, $V_{CBO} > V_{CEO}$).

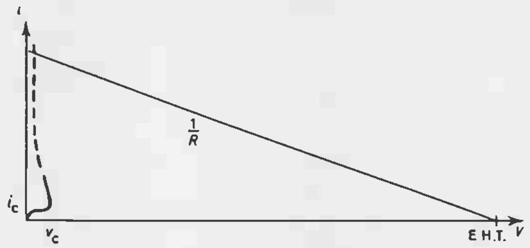


Fig. 15. Transistor characteristic and load line of the series resistor.

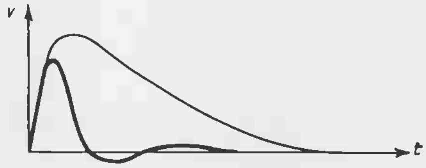


Fig. 16. Voltage waveforms applied to the resistor.

4.6. *Effects of Flashover Protection on Picture Tube*

The described method of protection directs the bulk of flashover current into the by-pass path. Under these circumstances, the amount of connection between the tube base and the tube coating is reduced to a minimum. Most of the voltage and practically all the energy is dissipated within the tube itself. Since the value of the series resistance is low, high peak currents are produced. In fact, the picture tube is subjected to the greatest possible stresses—a situation which does not occur in an unprotected receiver. For this reason, it was necessary to conduct life tests, and these showed that the picture tube can handle the additional burden without deterioration of life or performance.

4.7. *Other Sources of Disturbance*

An appreciable capacitance exists between the metal mounting band of the picture-tube and the internal conductive coating, as shown in Table 1. The majority of television receivers in this country are connected directly to the mains and there is a chance that the chassis can be live. For this reason, the metal band is connected to the rest of the receiver via an isolating network. It is good practice to return this network to the common contact on the outer coating. Large voltages are present on this band during flashover, therefore it is necessary to ensure that a suitable insulation exists to the rest of the receiver.

In a receiver provided with a double-wound mains transformer, there is no need for the isolating network, and the metal band can be connected directly to the common point on the external tube coating. However, there is still a need for good insulation to the rest of the receiver.

Often the line flyback pulses are taken to various parts of the receiver. In order to ensure freedom from breakdown, these pulses should not be taken from the same winding as the deflection coils, but from a separate winding well insulated from the rest.

Many unexplained difficulties in a television receiver can be attributed to circulating currents in the chassis generated by a picture-tube flashover. They enter the chassis through a connection to the tube base such as heater wiring, video amplifier, a_1 supply and so on, and via the stray capacitance between the tube and the outer coating. Obviously, the presence of resistors in series with the supply leads is a help. A further improvement can be produced by grouping all the components feeding the tube around point S from which a connection is taken to the tube-base, point P. Steps can be taken to keep the capacitance to the coating to a minimum; if possible, any large screening panels should be earthed at point S.

There is a limit to these reductions and a certain amount of chassis currents must be accepted. The main concern is the potential differences these currents cause. They can assume a sufficiently high value to modify operating conditions of transistors, particularly when remotely placed portions of circuits are interconnected. An example may be the a.g.c. system. In this particular case, it is fortunate that only d.c. voltages are involved. Most of the difficulties may be resolved by a capacitive decoupling close to the transistors supplied with a.g.c. An additional decoupling may be required to protect the devices generating the a.g.c.

During a picture-tube flashover, currents flowing in the outer coating generate an appreciable potential difference. For this reason, there should be only one point of contact between the coating and the receiver itself. In fact, the rest of the receiver should be well insulated from the coating. This particularly applies to the type of connection used in the circuit for flashover protection. Here the insulation must be capable of withstanding not only the voltages on the coating, but also on connection PA between the tube-base and the coating. Making allowances for a fault developing at the point of contact to the coating, the insulation has to handle peak voltages up to full e.h.t. value. At first sight, this may appear a stringent requirement; in fact, tests made on several existing receivers showed that the degree of insulation was sufficient and no modifications were needed.

The contact to the outer coating deserves some attention. In its execution it is necessary to bear in mind that a connection is made from a wire to a thin and brittle conductive layer. In order not to exceed the current-carrying capacity of the conductive coating it is necessary to make the contact over a large area. A minimum requirement is a copper braid extended diagonally across the coating, with a connection at the centre for the lead to the tube-base. A further improvement would be two diagonal braids joined at the centre. Occasionally an elaborate harness is used. A good contact to the coating provides not only trouble-free operation in the presence of flashover, but also reduces voltage drop across the coating. Additionally there is a reduction in r.f. interference radiated by the receiver during normal operation.

4.8. *Examples of Flashover Protection Design*

4.8.1. Flashover protection of monochrome receivers using the 'ring-trap' tubes

The 'ring-trap' tube is provided with spark-gaps to all electrodes, therefore the only other components to be added to the tube-socket are the series resistors. A possible arrangement of flashover protection is shown in Fig. 17. The drawing shows a vertical chassis with a cut-out for the tube. Four series resistors are grouped around the tube socket. The resistor in the cathode lead is 1·5 kΩ—this is the value considered at present as safe for protection of the video transistor. In the published data for picture-tubes, it is recommended that an un-bypassed resistor of 10 kΩ be used in series with the control grid in order to limit its excursion into grid current. Since a 1·5 kΩ resistor is already provided in the cathode lead, a 8·2 kΩ resistor can be used in series with the control grid for flashover protection. Higher values of resistors should be used for protection on the focus electrode and the first anode—22 kΩ are shown. If potentials for these electrodes are derived by means of semiconductor diodes, it may be necessary to verify whether these resistors provide a sufficient degree of protection.

To prevent the flashover currents meandering in the chassis, the video amplifier and circuits for focus, a_1 and control grid are mounted close to the tube-socket. In this vicinity, anchorage is made for the lead from the chassis, point S, to pin 5 on the tube-base (common electrode for all the spark-gaps). The heater connection to tube (pin 8) is also taken from point S.

The connection between the tube-base and the outer coating should be as short as possible. A short connection not only reduces self-inductance, but materially assists in keeping the wire apart from the rest of the receiver wiring and thus prevents a possibility of magnetic coupling.

In some receivers, a heater of a valve, or a power supply for transistor circuits may be inserted between the tube heater and the chassis. Such configuration requires a decoupling capacitor of 0·1 μF from at least one heater lead to point S, preferably from both leads.

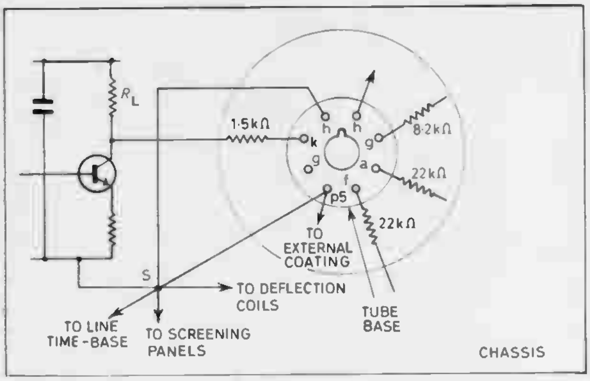


Fig. 17. Execution of flashover protection using 'ring-trap' tube.

As stated before, it is essential that the outer conductive coating and the metal band be insulated from the rest of the receiver for peak voltages approaching the e.h.t. value.

The protection described above can be applied to other tubes by providing the necessary spark-gaps. One side of each spark-gap should be returned to a common point P on the tube-socket. This point would serve the same function as pin 5 of the 'ring-trap' tube.

The described measures provide full flashover protection which is needed with transistor television receivers. 'Ring-trap' tubes can be used in receivers not requiring such a degree of protection. However, in such cases, it is necessary to connect pin 5 directly to the outer coating and it must be ensured that if a supply to any pin is taken directly from a high energy source, such as the h.t. line, a series resistor is provided (a few kilohms). In return for these provisions, the 'ring-trap' base will remove the possibility of arc formation anywhere in the wiring, due to picture tube flashover.

4.8.2. Flashover protection of colour receivers

A circuit diagram of a colour picture tube with flashover protection is shown in Fig. 18. The positioning of spark-gaps and resistors is clearly indicated; the common connection to all the spark-gaps is shown by means of a thicker line. Both the resistors and the spark-gaps should be mounted as close as possible to the pins of the tube, and the wiring to the common connection, point P, ought to be short. The take-off wire to the external tube coating should be connected opposite the focus pin (9). In view of the large number of components involved, a printed circuit spark-gap shown in Fig. 13(f) may be used as the basis of a panel to be mounted on the tube socket.

The values of series resistors shown in the circuit diagram follow the same lines as for the monochrome

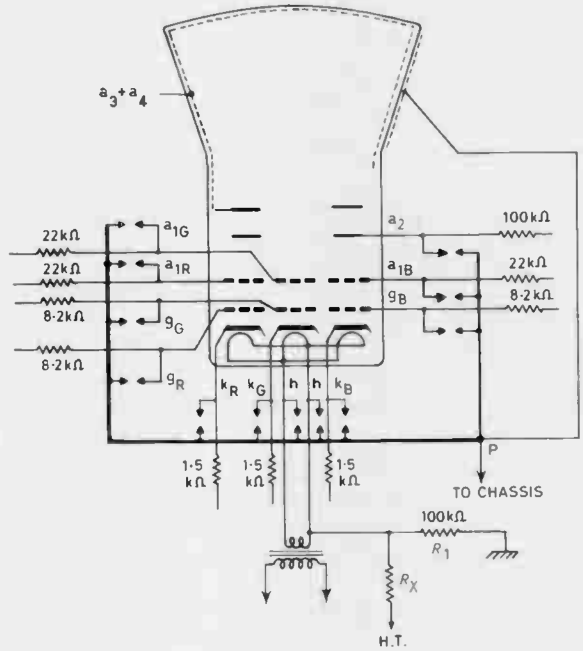


Fig. 18. Flashover protection of colour receiver.

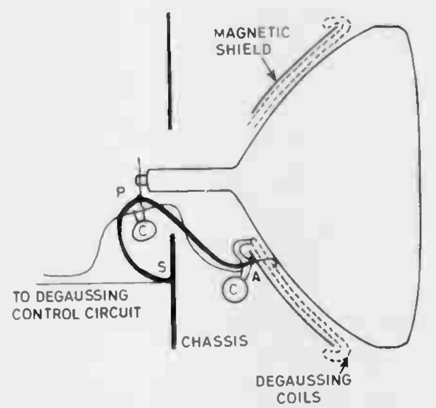


Fig. 19. Suggested arrangement of supply leads to degaussing coils.

tube. The only exception is the focus electrode, where, in view of higher operating voltage, a resistor of 100 kΩ is suggested. In receivers with a_1 potentials reaching 1 kV, it may be advisable to increase the series resistors to 33 kΩ in order to ensure a self-quenching action.

The heater of the picture tube is shown as being supplied from a separate winding on the transformer. Resistors R_X and R_1 may be used as a potential divider to reduce the heater-cathode potential of the tube. Their presence ensures a full flashover protection for the heater circuit.

Insulation of degaussing coils, commonly used in colour receivers, may prove a problem. Two alternatives are possible—either they are insulated for peak voltages of e.h.t. amplitude, or they are fed through bifilar leads as shown in Fig. 19. One of the leads is, in fact, the flashover by-pass connection, the other is specially provided for this purpose; the leads should be held closely together. At the tube socket side and at the conductive coating side, potentials on the leads are equalized by means of 1 to 2 nF capacitors capable of handling mains voltages.

4.9. *Warning*

A flashover between h.t. line and chassis will inject a large amount of current into the chassis and thus invalidate some of the protective measures. Furthermore, repeated discharges may lead to damage of the inside coating of the tube around the e.h.t. connector. For these reasons, every effort should be made to prevent such occurrences. Should this not be possible, a resistor of 10 kΩ should be connected close to the e.h.t. contact of the tube. The resistor, and its mounting, should be able to handle peak voltages of e.h.t amplitude.

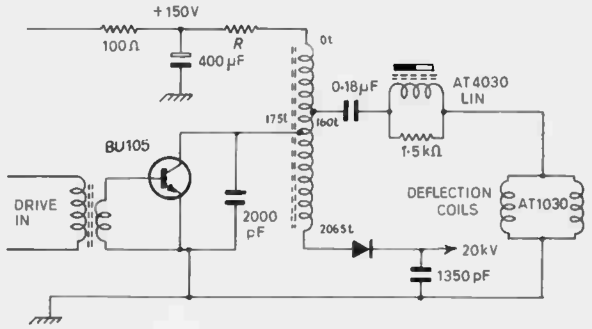


Fig. 20. Experimental line output stage.

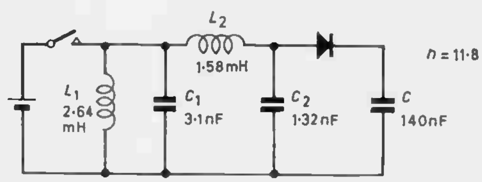


Fig. 21. Simplified equivalent circuit of third harmonic tuned transformer.

5. Protection of the E.H.T. Generator

5.1. *Description of the Phenomenon*

During the recharging period of the e.h.t. capacitor, unloaded by any agency (internal flashover of the picture tube, flashover from the e.h.t. line and so on), a severe overload is imposed on the e.h.t. generator. With circuits employing energy recovery, there is a disorganization of circuit functions. Valve circuits could handle such occurrences with impunity, but semiconductor devices require some protection.

5.2. *Effects on the Line Time-base*

5.2.1. E.h.t. recovery

A monochrome picture-tube, such as A47-11W, has a minimum external capacitance of 1 nF. At 20 kV a deflection current of 2·1 A peak-to-peak is required through a total inductance of 2·5 mH (coils and transformer primary).

Energy stored in picture-tube capacitance

$$= \tfrac{1}{2} CV^2 = \frac{1}{2}\,\frac{4\times 10^8}{10^9} = 0{\cdot}2\ \mathrm{J}$$

Energy stored in the line time-base

$$= \tfrac{1}{8} Li^2 = \frac{1}{8}\,\frac{2{\cdot}5}{10^3}\,2{\cdot}1^{\,2} = 1{\cdot}4\,\mathrm{mJ}$$

The ratio of these two sets of energy is 143. Although this simple calculation does not take into account several other effects, it shows that many cycles of the line time-base are needed to recharge the e.h.t. capacitor. The collapse and recovery of the e.h.t. is shown in Fig. 24. The photographs of oscilloscope displays described in this section of the paper were taken from an experimental line time-base shown in Fig. 20. In this circuit no energy recovery diode is shown; its function is performed by the collector-base junction of the output transistor BU105.

5.2.2. Reduction in fly-back time

The network analysis of the line output stage with third harmonic tuning has been published by several workers. In a simplified form, the equivalent circuit is as shown in Fig. 21. The nomenclature employed is as follows:

- C_1—combined capacitance of tuning capacitor, self-capacitance of deflection coils and of primary winding of the line output transformer
- L_1—combined inductance of scanning coils and primary inductance of the transformer
- L_2—leakage inductance between primary and secondary (e.h.t.) windings
- C_2—self-capacitance of e.h.t. winding and stray capacitance
- C—tube capacitance

All the values are referred to the primary of the transformer. Bate[3] showed that the fly-back time is given approximately by:

$$\tau_f = \sqrt{3}\,\pi (L_1 C_1 L_2 C_2)^{\frac{1}{4}} \qquad \ldots\ldots(10)$$

and for the condition of minimum voltage on the collector (double humped waveform):

$$\frac{C_2}{C_1} = \frac{5}{12} \quad \text{and} \quad \frac{L_2}{L_1} = \frac{3}{5}$$

Substituting in eqn. (10):

$$\tau_f = 3{\cdot}8\sqrt{L_1 C_1}$$

After a flashover, the tube capacitance C is discharged. Even if the internal impedance of the e.h.t. rectifier were zero, the line time-base does not have enough energy to recharge the capacitor. For this reason, when the first fly-back pulse occurs after the flashover, C_2 behaves as a short-circuit and L_2 appears in parallel with L_1. Disregarding the effects of e.h.t. rectifier impedance, the fly-back time is:

$$\tau_f' = \pi\sqrt{\frac{L_1 C_1}{L_1+L_2} C_1} \qquad \ldots\ldots(11)$$

The ratio of fly-back time before and after the flashover is:

$$\frac{\tau_f}{\tau_f'} = \frac{3{\cdot}8}{\pi}\sqrt{1+\frac{L_1}{L_2}} = \frac{3{\cdot}8}{\pi}\sqrt{1+\frac{5}{3}} = 2 \qquad \ldots\ldots(12)$$

This has been confirmed experimentally as shown in Fig. 25.

5.2.3. Increase in collector voltage

Fly-back voltage before flashover:

$$v_f = v_s \pi \frac{\tau_s}{\tau_f}$$

Fly-back voltage after flashover:

$$v_f' = v_s \pi \frac{\tau_s'}{\tau_f'}$$

The scan voltage v_s is the same, assuming the transistor remains bottomed:

$$\frac{v_f'}{v_f} = \frac{\tau_f}{\tau_f'}\,\frac{\tau_s'}{\tau_s} = 2\frac{\tau_s'}{\tau_s}$$

Since, from eqn. (12)

$$\tau_f = 2\,\tau_f'$$

$$\tau_s' = \tau_s + \tau_f'$$

Therefore

$$\frac{v_f'}{v_f} = 2\left(\frac{\tau_s+\tau_f'}{\tau_s}\right) = 2\left(1+\frac{\tau_f'}{\tau_s}\right) = 2\left(1+\frac{\tau_f}{2\tau_s}\right). \qquad \ldots\ldots(13)$$

In practice,

$$\frac{\tau_f}{\tau_s} = 0{\cdot}22$$

which gives

$$\frac{v_f'}{v_f} = 2(1+0{\cdot}11) = 2{\cdot}22$$

The above arguments do not take into consideration the reduction in the peak collector voltage due to third harmonic tuning (about 15%). If this is taken into account, the possible increase in the collector voltage may be 2·5 times. However, in practice these increases are associated with a large increase in the collector current. Normally, there will not be enough base drive to support these currents and the transistor will come out of bottoming, causing a drop in the peak collector voltage. This situation can be observed in Fig. 25.

5.2.4. Increase in the collector current

An idealized diagram of transistor and efficiency diode current waveforms is shown in Fig. 22. During the scan period the e.h.t. rectifier is not conducting,

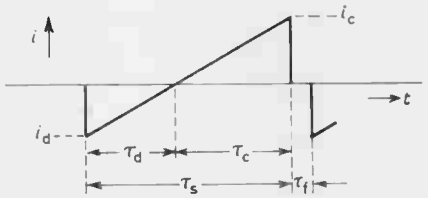


Fig. 22. Idealized current waveforms.

hence the shunting effect of leakage inductance, so important in the case of the peak collector voltage, is absent.

It is common to express

$$\frac{i_d}{i_c} = \sqrt{\eta}$$

The peak-to-peak current is:

$$\alpha = i_c - (-i_d) = i_c + i_c\sqrt{\eta}$$

Thus,

$$i_c = \frac{\alpha}{1+\sqrt{\eta}} \qquad \ldots\ldots(14)$$

average current of the transistor:

$$I_t = \tfrac{1}{2}\, i_c \frac{\tau_c}{\tau}$$

average current of the diode:

$$I_d = -\tfrac{1}{2}\, i_d \frac{\tau_d}{\tau}$$

average current flowing through the transformer:

$$I = I_t + I_d = \frac{1}{2\tau}(i_c\tau_c - i_d\tau_d)$$

Substituting for

$$i_d = i_c\sqrt{\eta}, \quad \tau_d = \tau_c\sqrt{\eta} \quad \text{and} \quad i_c$$

$$I = \frac{1}{2}\frac{\tau_c}{\tau}\alpha(1-\sqrt{\eta}) \qquad \ldots\ldots(15)$$

After a flashover, the e.h.t. capacitor is discharged and when the next fly-back pulse arrives, all the energy goes into the capacitor. For this reason, there is very little energy left for the recovery. For the sake of simplicity, let us assume that, under these conditions, the efficiency diode is not conducting. In order to keep the line output transistor bottomed, the inductive voltage drop $L\mathrm{d}i/\mathrm{d}t$ must remain unchanged. This can be satisfied provided $\mathrm{d}i/\mathrm{d}t$ remains constant. The peak current to be supplied by the transistor will depend on the length of the driving pulse applied to the base. As extremes of possible situations, two cases are considered: transistor driven for the whole scan period τ_s and the drive limited only to the conduction time of the transistor τ_c.

Case 1. Transistor driven during the whole scan period.

In this situation, the transistor must supply the whole current α, therefore

$$i'_c = \alpha$$

The average current is also the only current in the transformer, and is:

$$I' = \tfrac{1}{2}\alpha \frac{\tau_s}{\tau}$$

The increase in the peak collector current is:

$$\frac{i'_c}{i_c} = 1+\sqrt{\eta}$$

The increase in the average transformer current is:

$$\frac{I'}{I} = \frac{\tau_s}{\tau_c(1+\sqrt{\eta})}$$

Since

$$\tau_s = \tau_c(1+\sqrt{\eta})$$

$$\frac{I'}{I} = \frac{1+\sqrt{\eta}}{1-\sqrt{\eta}} \qquad \text{......(16)}$$

Taking $\sqrt{\eta} = 0{\cdot}8$, the increase in the peak collector current is 1·8 times and in the average current 9 times.

Case 2. Transistor open for the duration τ_c.

After a flashover, the peak collector current remains unchanged, and the average current is:

$$I'' = \tfrac{1}{2} i_c \frac{\tau_c}{\tau}$$

Substituting for

$$i_c = \frac{\alpha}{1+\sqrt{\eta}}$$

$$I'' = \frac{1}{2}\frac{\alpha}{1+\sqrt{\eta}}\frac{\tau_c}{\tau}$$

The increase in the average current is:

$$\frac{I''}{I} = \frac{1}{1-\eta} \qquad \text{......(17)}$$

Again, taking $\sqrt{\eta} = 0{\cdot}8$, the increase is 2·8 times.

In practice, the conduction time of the transistor is somewhere in between these two cases; let it be $\tau_t, \tau_t > \tau_c$. Using the same arguments, it is possible to show that:

the increase in the peak collector current is

$$\frac{\tau_t}{\tau_c} \qquad \text{......(18)}$$

the increase in the average current is

$$\frac{1}{1-\eta}\left(\frac{\tau_t}{\tau_c}\right)^2 \qquad \text{......(19)}$$

In Fig. 26 are shown waveforms of the collector voltage and the collector current before and after a flashover. The maximum increase in the peak collector current is over four times. Yet eqn. (18) indicates only an increase of 1·35 times (since measured $\tau_t/\tau_c = 1{\cdot}35$). The corresponding increase in the average current is 5 times. Obviously, there is another contributory cause.

5.2.5. Increase in the magnetic flux density

The diagram in Fig. 22 shows idealized current waveforms of the transistor and the efficiency diode. Inspection of the circuit diagram in Fig. 20 shows that the transformer has to handle the total direct current, but only a fraction of the alternating current. In a well-designed transformer, about 90% of the alternating current is directed into the deflection coils. Thus, the peak magnetizing current can be written:

$$i_m = \tfrac{1}{10}(i_c - I) + I \qquad \text{......(20)}$$

Substituting for i_c and I (eqns. (14) and (15)),

$$i_m = \frac{1}{10}\left[\frac{\alpha}{1+\sqrt{\eta}} - \frac{1}{2}\frac{\tau_c}{\tau}\alpha(1-\sqrt{\eta})\right] + \frac{1}{2}\frac{\tau_c}{\tau}\alpha(1-\sqrt{\eta})$$

Taking

$$\sqrt{\eta} = 0{\cdot}8 \quad \text{and} \quad \frac{\tau_s}{\tau} = 0{\cdot}82$$

$$i_m = 0{\cdot}051\alpha + 0{\cdot}0455\alpha = 0{\cdot}0965\alpha \qquad \text{......(21)}$$

In the above equation, the first term represents the a.c. component and the other the d.c. component. The equation shows them to be of about the same magnitude.

A similar equation can be derived for Case 1, where the transistor is driven for the whole scan period:

$$i'_m = 0{\cdot}1\alpha + 0{\cdot}378\alpha = 0{\cdot}478\alpha \qquad \text{......(22)}$$

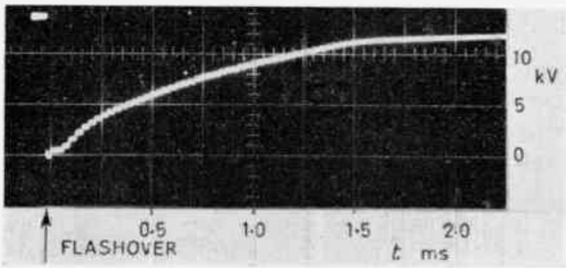


Fig. 24. Recovery of e.h.t. voltage.

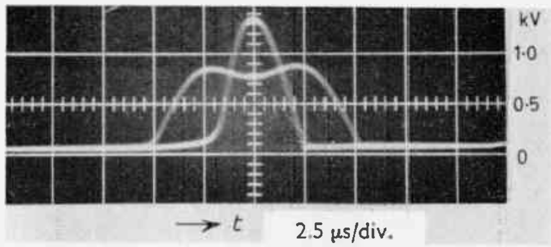


Fig. 25. Comparison of fly-back waveforms before and after flashover.

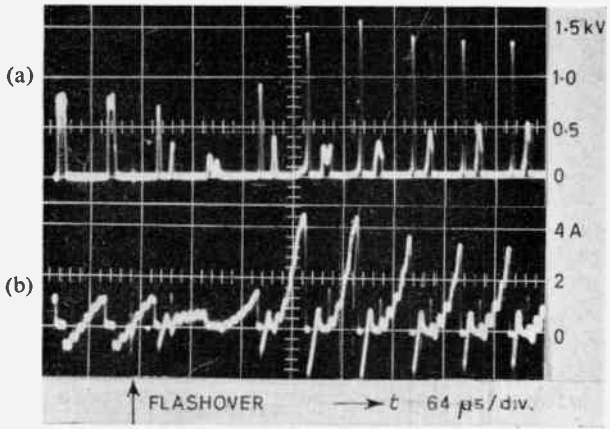


Fig. 26. Waveforms of collector voltage and current. (a) Collector voltage; (b) Collector current.

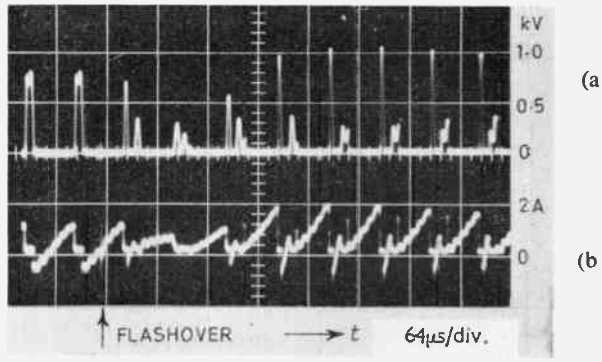


Fig. 27. Effect of 56Ω resistor in series with h.t. to line output transformer. (a) Collector voltage; (b) Collector current.

Therefore,

$$\frac{i'_m}{i_m} = 5$$

For Case 2, when the transistor is driven only during τ_c,

$$i''_m = 0{\cdot}0428\alpha + 0{\cdot}127\alpha = 0{\cdot}17\alpha \quad \text{......(23)}$$

$$\frac{i''_m}{i_m} = 1{\cdot}8$$

Thus the increase in the peak magnetizing current can vary between 1·8 and 5 times. For the waveforms shown in Fig. 26, the corresponding equation is:

$$0{\cdot}052\alpha + 0{\cdot}23\alpha = 0{\cdot}282\alpha \quad \text{......(24)}$$

and the increase is 2·9 times.

A transformer is seldom designed with such a margin of safety, and saturation of the core is inevitable. This leads to an increase in the current drawn by the transistor and further saturation of the core.

Inspection of Fig. 26 shows that the increase in the peak collector voltage and current occurs a few cycles after the flashover (and sometimes later than that, depending on circuit arrangements). In fact, with the flashover in the middle of the scan period, there is no change in operation until the next fly-back pulse. This is followed by several cycles when the circuit re-organizes itself and after that there is an increase in the peak collector current and voltage.

5.3. *Flashover across the E.H.T. Rectifier*

The picture tube capacitance can also be discharged by a flashover across the e.h.t. rectifier. In this case there is, in addition to the effects described above, a large amount of energy injected into the line timebase circuit. In order to obtain some magnitude of the resulting currents and voltages, let us disregard all the resistive components and assume the line output transistor is not conducting (this is actually the case, since usually a flashover occurs shortly after the fly-back when the inverse voltage is enhanced by rings). With reference to Fig. 21, an arc across the rectifier will connect C across C_2. Since $C_2 \ll C$, C_2 can be disregarded, and the circuit configuration considered as shown in Fig. 23. It is assumed that at $t = 0$, $i_1 = 0$, $V_{c1} = 0$ and $V_c = V$. The differential equation for the circuit can be written as:

$$\frac{d^4 i_1}{dt^4} + a\frac{d^2 i_1}{dt^2} + b i_1 = 0 \quad \text{......(25)}$$

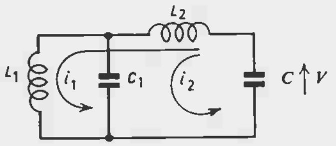


Fig. 23. Simplified circuit diagram for calculation of effects of flashover across e.h.t. rectifier.

where

$$a = \frac{L_1 C + L_2 C + L_1 C_1}{L_1 C_1 L_2 C} \quad \text{and} \quad b = \frac{1}{L_1 C_1 L_2 C}$$

Writing

$$p_1 = \tfrac{1}{2}(-a+\sqrt{a^2-4b}); \quad p_1 = \pm j\omega_1$$

$$p_2 = \tfrac{1}{2}(-a-\sqrt{a^2-4b}); \quad p_2 = \pm j\omega_2$$

the solution is:

$$i_1 = \mathrm{A}e^{p_1 t} + \mathrm{B}e^{-p_1 t} + \mathrm{C}e^{p_2 t} + \mathrm{D}e^{-p_2 t} \qquad \ldots\ldots(26)$$

From the initial conditions:

$$\mathrm{A} = \frac{\omega_2}{\omega_1}\mathrm{D}, \quad B = -\frac{\omega_2}{\omega_1}\mathrm{D}, \quad C = -\mathrm{D},$$

and

$$\mathrm{D} = \frac{-V}{2L_1 C_1 L_2 p_2(p_1^2 - p_2^2)}$$

Substituting and rearranging:

$$i_1 = \frac{-V}{L_1 C_1 L_2 \omega_2 (p_1^2 - p_2^2)}\left(\frac{\omega_2}{\omega_1}\sin\omega_1 t - \sin\omega_2 t\right) \qquad \ldots\ldots(27)$$

The voltage across L_1 (and C_1) is:

$$v = \frac{-V}{L_2 C_1 (p_1^2 - p_2^2)}(\cos\omega_1 t - \cos\omega_2 t) \qquad \ldots\ldots(28)$$

Substituting for the values of components from Fig. 23, the peak values are:

$$i_1 = 10\ \mathrm{A}; \quad v = 2{\cdot}1\ \mathrm{kV}$$

In this particular time-base, to generate the e.h.t. of 20 kV, the peak voltage on the transistor was 1·3 kV, and the peak collector current 1·5 A.

A simulated flashover across the e.h.t. rectifier produced failure of the line output transistor at the first attempt.

5.4. *Protective Measures*

In a transistor line time-base, the peak collector voltage and current are proportional to the applied h.t. voltage. Thus, insertion of a resistor in series with the h.t. supply to the line output transformer (resistor *R* in Fig. 20) can provide the required degree of protection. To be fully effective, it must be un-bypassed to ensure a quick response. With modern circuits, the line output transformers carry only a small fraction of alternating current; hence the amount of ripple developed across the resistor should be small. Furthermore, Martin[4] suggested that if the deflection coils are suitably tapped on to the transformer by taking into account shunt inductance losses, the bulk of the transformer winding (n_{0-160}) is free from alternating current.

The effectiveness of the resistor is illustrated in Fig 27, which was taken under the same conditions as Fig. 26, and with $R = 56\Omega$. There is a very useful reduction in the peak collector voltage and a most significant reduction in the peak collector current. However, presence of the resistor produces an increase in the e.h.t. regulation (0·9 MΩ measured).

It is suggested that a suitable compromise between the voltage derating of the transistor for flashover contingency and the increase in the e.h.t. regulation may be obtained if the value of the resistor is chosen to give a 20% increase in the peak collector voltage after flashover.

Since most of the increase in the collector current as a result of flashover is due to saturation of the transformer, a desaturated line output transformer is a possible solution. However, additional steps are needed to deal with the increase in the peak collector voltage. Fortunately, such a design involves some form of a.c. coupling, and a reduction is possible by using a small coupling capacitor. This approach was tried by modifying the circuit in Fig. 20 as follows: the h.t. line to the line output transformer was disconnected at point 0t and fed to the collector via a 28 mH inductor; a capacitor of 10 nF was connected between the h.t. line and the start of the transformer winding. The results were similar to the case of resistance in series with the h.t. line.

Occasionally, difficulties are experienced with transient pulses appearing on the base drive waveform during fly-back due to collector-base capacitance of the line output transistor. A capacitor connected between the base and emitter should provide an effective solution.

In view of the severity of disturbance due to the flashover across the e.h.t. rectifier, it may be difficult to develop an effective method of protection. It was felt that with line output stages using transistors, semiconductor e.h.t. rectifiers will be used. In contrast with thermionic valve rectifiers, they could be free from internal flashovers. Attention should be paid to stability of these devices with time and temperature. Encapsulation of rectifying elements should ensure freedom from external arcing.

6. Notes on Measuring Techniques

6.1. *Oscilloscope Measurements*

Flashovers of picture tubes are essentially non-repetitive events of short duration. This imposes severe demands on oscilloscopes in terms of writing-speed and accuracy of synchronization. With high-grade laboratory instruments, it is still necessary to rely on dark-adaptation of the eye in order to discern faster waveforms. Photography of displays is even more difficult; often, with the fastest materials available, it is necessary to use multiple exposures.

A flashover produces severe electrical interferences which reach the measuring oscilloscopes via earth leads and by direct radiation. Unless great care is taken, the display does not bear any relation to the signal under examination. Many solutions have been tried in order to overcome these difficulties: special oscilloscopes were constructed for this purpose, elaborate screening of input probes was used, input stages of standard instruments were by-passed, and so on. The author made extensive use of direct signal injection to the Y-deflection plates of the oscilloscope tube via a long coaxial cable properly terminated at both ends. The cable acted as a signal delay and the triggering was carried out via the normal channels. Probes were prepared to measure both voltages and currents.

6.2. *Flashover Generator*

In view of the unpredictable nature of flashovers generated by the picture-tube, there was a need for a piece of equipment to produce the required discharges at command. Such equipment was constructed using the simplified equivalent circuit shown in Fig. 7. The e.h.t. generator was replaced by a variable e.h.t. supply and a series resistor of 100 MΩ, and the tube capacitance by high-voltage capacitors specially selected for low internal impedance. The spark-gap was constructed of two aluminium balls, 1·5 cm in diameter. One of the balls was permanently fixed, while the other was mounted on a threaded bolt, made of perspex, so that the separation between the balls could be varied from zero to about 2 cm. A resistance of 2Ω was inserted in series with the spark-gap to make up the internal losses to the same value as in the picture-tube. A photograph of discharge current produced by this equipment is shown in Fig. 4.

In many experiments on line time-bases and television receivers, all the components of the flashover generator are already available with the exception of the spark-gap. A simple spark-gap cannot be used since there is no mechanism to control the discharges. For these applications a triggered spark-gap was constructed as shown in Fig. 28. Its main feature is an auxiliary spark-gap built into one of the electrodes. It is formed by a mushroom-shaped central core with a cylindrical outer shell. A machined piece of perspex provides a rigid spacing between the two portions; the gap itself is in air. The auxiliary spark-gap is supplied from a high voltage transformer wound on a ferroxcube core of the type used in line output transformers. The windings are well insulated from the core and from each other—up to 30 kV pulses or d.c.

Triggering of the auxiliary spark-gap is by means of a positive-going pulse, of about 80 μs duration, applied to the base of the BFY50. A single pulse can be initiated manually, or pulses can be produced electronically at a desired repetition frequency. For investigation of line time-bases, equipment was designed to produce pulses synchronized with the line time-base and also providing sync. pulses to the oscilloscope. In this way, it is possible to observe the behaviour of the time-base just prior to the flashover, and for a desired time afterwards. The flashover itself can be positioned at a desired portion of the line time-base cycle. Photographs shown in Figs. 24, 25 and 26 were taken using this equipment.

The action of the triggered spark-gap is based on the principle that the breakdown within the auxiliary gap lowers the breakdown voltage of the main gap. With a suitable spacing of the main gap, a breakdown can be produced every time an arc is formed within the auxiliary gap.

The triggered spark-gap can be used in the applications listed above or in the flashover generator. While it forms a very convenient means of producing an accurately-timed breakdown, it has its own dangers. A fair amount of energy is available at the auxiliary spark-gap and it is important to ensure that it is not injected into the circuit under examination. For this reason, it is desirable to limit this energy to a level just sufficient for reliable operation. A degree of isolation may be obtained by inserting 1·5 kΩ resistors in the leads feeding the spark-gap.

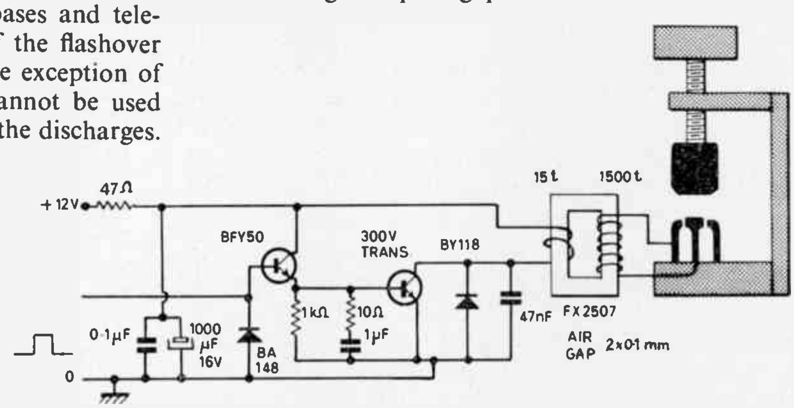


Fig. 28. Triggered spark-gap.

The generator can be used for many experiments on flashover problems. However, there are situations where the physical configuration of the picture tube plays an important role—such as presence of capacitance between chassis and the outer conductive coating. For these problems the capacitors of the generator must be replaced by the tube capacitance. Unfortunately, with repeated flashovers, there is a degradation in the quality of contact between the internal conductive coating and the e.h.t. connector. This leads to a reduction in the peak current delivered by the equipment.

6.3. *Receiver Testing*

In the method adopted by the author, a triggered spark-gap is used. One terminal is connected to the e.h.t. contact of the picture tube and the other to a flying-lead. The receiver is operated at nominal mains voltage increased by 10%. The test is commenced by connecting the flying-lead to the focus pin of the picture-tube and operating the spark-gap at a rate of about one breakdown in three seconds. After about a hundred discharges, the lead is transferred to the first anode, then to the grid and so on. At each stage observations are made of the occurrences on the tube socket, receiver wiring and general behaviour of the set. Every effort is exerted to trace the path taken by the flashover currents, occasionally removing any unintended spark-gaps within the chassis. When a flashover inside the tube is suspected, the relevant pin is isolated from the circuitry by means of series resistors.

Tests on line time-bases are made using a special synchronizing unit to operate the triggered spark-gap. This arrangement allows the production of the flashover at any desired portion of the line time-base cycle, and enables observations to be made of the behaviour of the circuit prior to the discharge and for any length of time afterwards.

7. Conclusions

A picture tube, in common with other high-voltage vacuum devices, is prone to internal flashover. With the product available at present, the number of flashovers is so low as to pass completely unnoticed by the viewer, but there is a potential hazard to semiconductors and other devices in the television receiver. It seems unlikely that a flashover can be eliminated entirely, and for this reason, measures must be applied to protect the devices and hence the receiver.

As a result of picture-tube flashover, high-energy transients are generated which primarily affect circuits with direct connection to the tube base. A further consequence is the discharge of the capacitor in the e.h.t. supply (usually the line time-base). While the voltage on the capacitor is recovering, the output stage is subjected to considerable overloads in terms of high peak current and voltage. The same effects can be produced by discharges in various parts of the e.h.t. generator, including a breakdown across the e.h.t. rectifier. With the latter there is additionally an injection of a large amount of energy into the e.h.t. system.

The protection against the transients consists of provision of a separate connection between the tube base and the external coating. By means of spark-gaps and resistors (in series with the leads to the tube-base) high-amplitude flashover currents are diverted from the receiver circuitry and are directed into the flashover by-pass connection.

A required degree of protection of the e.h.t. generator may be obtained by insertion of a resistor between the h.t. line and the output transformer. In order to keep the resulting increase in the internal impedance of the e.h.t. generator within acceptable limits, it is suggested that the resistor should be so proportioned that the increase in the collector voltage of the output transistor during the overloads does not exceed 20%. In deriving nominal operating conditions of the transistor from its absolute ratings this derating should be taken into account.

The same degree of protection can be obtained with the output transformer operated in the saturated mode, provided a small coupling capacitor is used.

It may be difficult to provide an efficient protection against flashover of the e.h.t. rectifier. It is believed that with transistor equipment semiconductor e.h.t. rectifiers will be used. These can be produced to be free from internal flashover.

8. Acknowledgments

The contents of this paper cover many areas of interest and provide interaction of many ideas. Whenever possible acknowledgments have been made directly in the text, but in addition the author wishes to express his gratitude to all workers in this field. His thanks are also due to many colleagues for endless discussions, encouragement and for valuable suggestions, and particularly to Mr. F. Majkut for a multitude of experiments. The author also wishes to thank the Directors of Mullard Ltd. for permission to publish this paper.

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A Stored Microprogram Control Unit Using Tunnel Diodes

By

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AND

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Summary: This paper is an account of an attempt to perform logic at very high speed (250 MHz) using tunnel diodes. The basic circuit, a derivative of the Goto pair, is described and the rather limited logic power of such an element defined. An account is given of a suitable application for a small amount of very high speed logic, namely a variable microprogram control unit for a transistor digital computer. A brief description of the incorporation of the tunnel diodes in the machine follows.

The microwave diodes used were found to be too unreliable for large-scale use in a digital computer. By careful selection from a large number (5000) of diodes, 700 logic elements were constructed and interconnected, to confirm the circuit analysis and logic rules. It is concluded that in the event of reliable microwave tunnel diodes becoming available in large numbers they could be used in the described manner to perform logic at 250–300 megabit rates and 1 ns stage delays.

1. The Basic Circuit

After investigating a number of tunnel diode circuits, a modified version of the Goto pair was adopted for use in the machine. Several appraisals of the Goto pair have been published[1, 2] and it is not proposed to give a detailed analysis here, but a few comments will not be out of place. The performance of the basic circuit is, almost entirely, limited by stray reactance. Diodes capable of operation at frequencies up to several gigahertz can be made successfully (although we have found most of them thermally unstable and mechanically frail!). However, even using the modified Goto pair (as described by Wiseman[3]) great difficulties are encountered in achieving a physical construction which has stray capacitances low enough to permit reliable operation at speeds above about 500 MHz. Extensive computer simulation studies of the circuit have been carried out[4] and the parameters chosen for the circuit described below were considered to represent a good compromise between manufacturing difficulty, stability and performance. The authors were led to believe, incorrectly as it turned out, that diodes having suitable characteristics were available from several sources at reasonable prices.

The same element is used throughout the system and was made, in this Laboratory, by soldering pill packaged tunnel diodes on to an evaporated thin film circuit. These circuits consisted of borosilicate glass substrates 6·4 × 15·2 × 5·1 mm (0·25 × 0·6 × 0·02 in) on which the network of resistors (nichrome sealed with silicon monoxide) and conductors (copper on nichrome) were deposited during a single pump-down cycle by sequential evaporation through two out-of-contact masks. The nichrome source, which must be well controlled and uniform in emission was heated by electron bombardment, the copper and silicon monoxide sources were resistance-heated boats. A second pump-down was used to deposit an earth plane on the backs of the substrates. The resistance was measured during evaporation on a separate monitor slide and

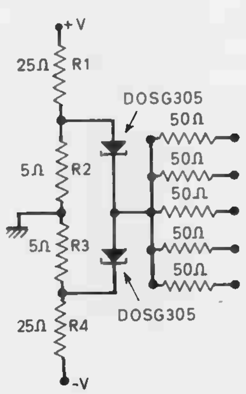

Fig. 1. The basic circuit.

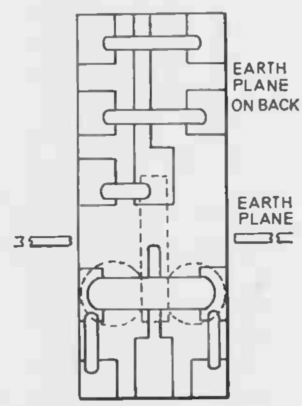

Fig. 2. The circuit layout.

twenty-four substrates were processed simultaneously. The circuit is shown in Fig. 1, the layout in Fig. 2. The resistor chain R1, R2, R3, R4 is of most concern, and the absolute values of these resistors are held to $\pm 12\%$. Due to the method of manufacture, the ratios of resistors are easily made to be more accurate than the absolute values, and the ratios R1 : R2 and R3 : R4 are held to within 3% of each other. The summing and output resistors are held to $\pm 12\%$.

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A yield of 30% good substrates was achieved while the masks, fabricated from 0·025 mm (0·001 in) molybdenum sheet, were in new condition, but eventually distortions produced by evaporated deposits and mechanical damage reduced this to 20%. Even so one man was able to produce 1200 satisfactory substrates from the one set of masks. Unsatisfactory substrates were chemically cleaned and reprocessed. The principal reasons for out of range resistors were unclean substrates, asymmetrical nichrome source, and masks being too far from the substrates (they swung upwards into position in the mask-changer and if greater than 5 mm from the substrate the copper spread into the resistor area).

The germanium tunnel diodes (type DOSG305) are packaged in a microwave pill 3·05 mm (0·12 in) in diameter by 1·52 mm (0·06 in) high, with the actual diode being a small chip 0·013 × 0·125 mm (0·005 × 0·01 in) connected by fine wires to the case. Peak current is 10 mA ± 10%. Barrier capacitance, nominally less than 10 pF, is generally spread from ½ pF to 15 pF, and diodes were selected to be from 1½ pF to 10 pF. The series inductance of a pill diode is 0·5 nH.

Tunnel diodes were batched roughly by capacitance (within 1½ pF) and then matched in pairs as exactly as possible (within 100 μA, i.e. 1%) by peak current. They were then soldered to the substrates with very low melting point (80°C) solder, making sure that the diodes never exceeded 100°C, their nominal maximum operating temperature. The centre point of the diodes was bridged with a large piece of copper foil which was then soldered with ordinary solder to the centre point of the summing resistors. The critical loop had an inductance which was largely the series inductance of the diodes themselves and those packages made from the low capacitance diodes (< 2 pF) failed from inductive effects at above about 320 MHz. The inductance effects were just beginning to appear at 250 MHz but not enough to be significant, at the chosen pump voltages. Packages made from diodes greater than 10 pF were discarded as too slow in switching.

The yield on diodes was very poor and since they eventually ceased to become available, the completion of the machine became impossible. In all 4800 diodes were handled and only 700 packages (using 1400 diodes) could be made. The diodes were of epitaxial unetched construction but although they were mechanically very strong (a previous serious weakness of tunnel diodes), many were unstable with respect to both temperature and time. Eventually the diodes were 'baked' at 80°C for 15 minutes after measuring and before installing and this eliminated most of the diodes that would have open-circuited or drifted on installation. The diodes were delivered in batches of 300 spaced several weeks apart, and some batches yielded very well, say 70%, whilst other batches were virtually a total loss. Although nominally the same diodes, the spread in I_p and C_b, the proportion drifting and the proportion failing on heating to 80°C, all varied so widely from batch to batch that practically no two batches were the same. These were the first epitaxial diodes that became available, and it was fully expected that, as with transistors, they would be a considerable improvement on the alloy-diffused diodes previously made. In fact they are, if anything, even less reliable and though the wide variation between batches would indicate that the difficulty probably lies in the manufacturing methods, rather than being inherent in the device, the authors have concluded that no high-speed tunnel diodes that they have examined are suitable for large-scale incorporation in a digital computer. This will not necessarily remain so as only a very small amount of development work has been done on the epitaxial tunnel diode compared with that done on the epitaxial transistor.

Most of the package failures were due to I_p drifting, but a few (less than 20) were due to unequal series resistances of the tunnel diodes, a parameter not checked before construction since it is strongly correlated to I_p and C_b. No other failure reasons could be found apart from occasional accidental breakages of the substrates.

After construction the packages were tested for switching speed and out-of-balance current in the fully loaded condition, a full load being a total fan power of four. A calculated waveform is shown in Fig. 3, and an oscilloscope trace for a 2 pF pair is shown in Fig. 4; a typical pulse train is also shown in Fig. 5. Interconnection between packages is by 50 Ω transmission line with a 50 Ω resistor at the sending end, and ending in a 50 Ω summing resistor at the receiving package (Fig. 6). Thus a single load looks

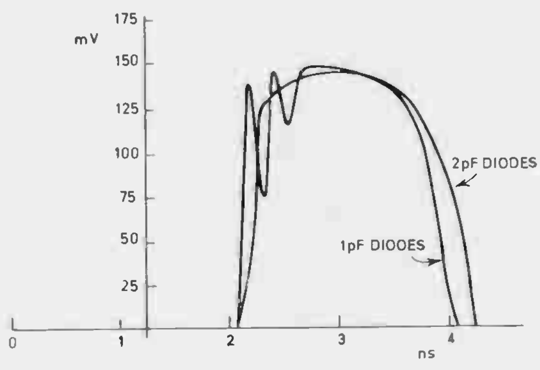

Fig. 3. A calculated waveform.

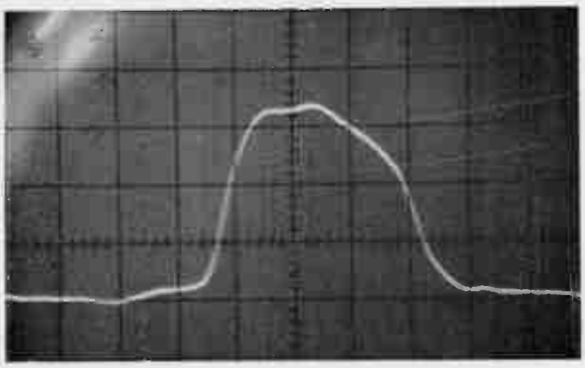

Fig. 4. An oscilloscope waveform; horizontal scale: 500 ps/cm; vertical scale: 50 mV/cm.

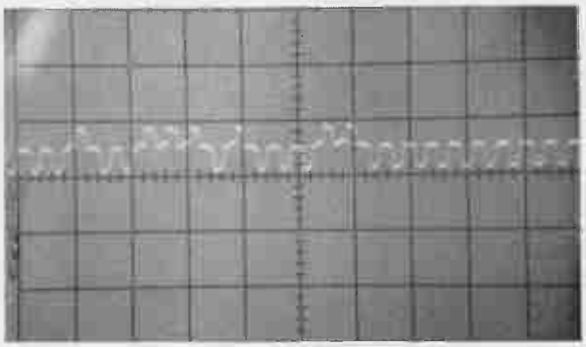

Fig. 5. A typical pulse train; horizontal scale: 10 ns/cm; vertical scale: 50 mV/cm.

like 100 Ω to the sending package whether it is an input or an output. The signals are inherently unbalanced with respect to earth but the transmission line is balanced, consisting of a bifilar pair of lacquered wires 0·25 mm (0·01 in) in diameter. Normal interconnections are less than 7·6 cm (3 in) long which is $\lambda/8$, and no trouble was experienced with such short lengths. Long wires, which are greater than 25 cm (10 in), however, must be threaded several times through a ferrite toroid. Earthing the correct one of the balanced pair then restores the signal to the fully unbalanced state, and any common mode currents are rendered negligible by the large common mode inductance presented by the toroid.

2. The Logical Performance of the Circuit Element

Logically the Goto pair forms a majority element without isolation between output and input. In fact the same resistors are used for either outputs or inputs as required. The lack of isolation necessitates a system of phased pumps and by a symmetry argument it is evident that more than two pumps are essential, if they are equally spaced. Three or four pumps are both possible and show their peculiar advantages and disadvantages. From the majority element, a 2-input AND and a 2-input OR may be constructed but, unless a two-wire system is used, inversion is also required. This can be done by differentiating the output and feeding the trailing edge spike into a suitably phased package as a following amplifier. The modified interconnection is shown in Fig. 7. Two packages are required and must be close to each other, within 13 mm ($\frac{1}{2}$ in), with a phase difference of 240° between them. The 8 pF capacitor and the total series resistance of 75 Ω form a differentiating circuit of 600 ps time constant. Thus a current spike of initial value 2 mA, time-constant 600 ps is available on the short transmission line into the amplifying package which inverts the original signal by sensing only the trailing edge spike. Other schemes

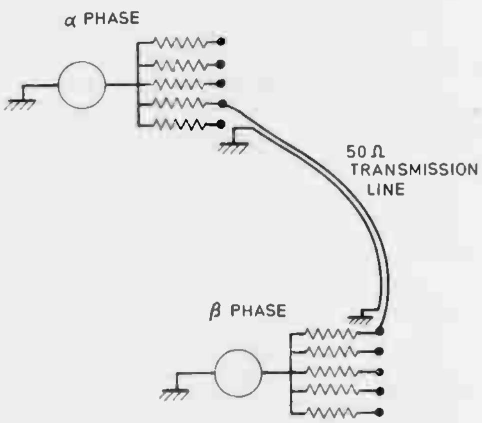

Fig. 6. The standard interconnection.

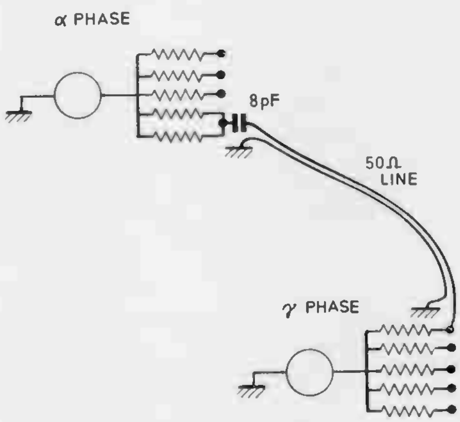

Fig. 7. The inverting interconnection.

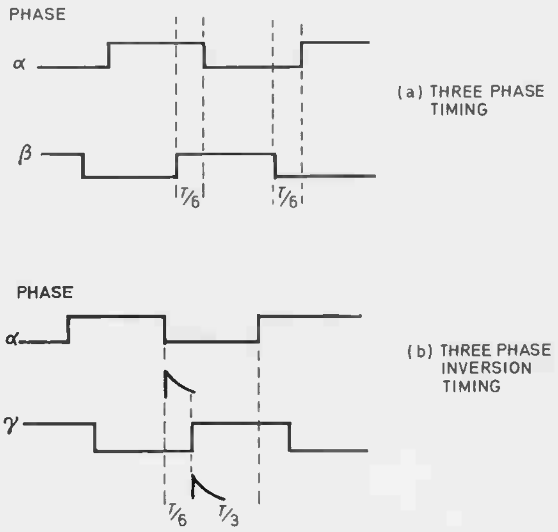

Fig. 8. Three-phase operation.

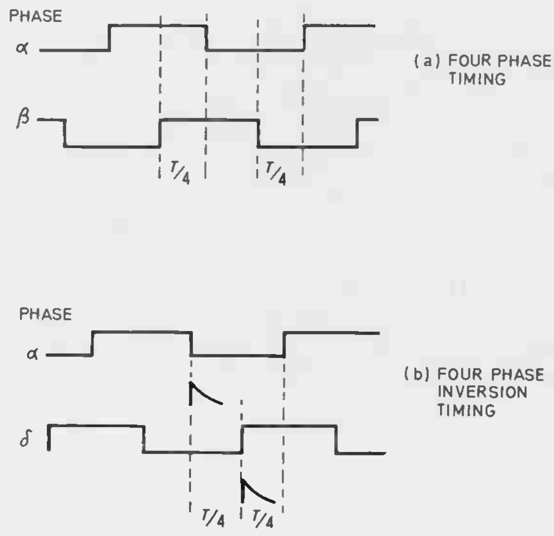

Fig. 9. Four-phase operation.

were considered, principally using transformers, but they were found to be sensitive to the duty cycle, or unduly sensitive to earth currents.

When deciding the number of phases two points are particularly relevant from the point of view of the correct operation of the packages. First, the prevention of back-writing currents from occurring through delays in signal wires and pump distributions; second, the minimizing of back-writing currents affecting the inverters.

Assuming a 1 : 1 mark space ratio, the idealized three-phase situation is illustrated in Fig. 8, the four-phase in Fig. 9. It is seen that there is a tolerance of $T/6$ in the three-phase case, but one of $T/4$ in the four-phase case, in each case for both writing and back-writing. This tolerance is a fundamental limitation and must cover delays in the interconnection, delays down the pump distribution, tolerance on pump phases, tolerance in mark/space ratio, and variations in rise-times.

Examining the inversion situation, in the three-phase case the forward writing transfer requires the spike to hold up for $T/6$, and in back-writing it has $T/3$ to die away in. In the four-phase case the times are both $T/4$, which is significantly worse, permitting no differentiation between forwards and backwards transfer. In the end it was felt that using three phases was the more practicable.

The pump is distributed on a set of lines 6·4 mm ($\frac{1}{4}$ in) apart, the packages being spaced 9·3 mm ($\frac{3}{8}$ in) apart down the lines. The pump moves down the lines at a speed of 15·2 cm/ns (6 in/ns), which is the same propagation speed as the interconnecting transmission lines. Thus the packages occupy a matrix being 9·3 mm ($\frac{3}{8}$ in) apart up and down the pump and 6·4 mm ($\frac{1}{4}$ in) apart across the pump. Considering Fig. 8 again, since the delay along the interconnection is always positive, it will be seen that the worst condition is the back-writing failure of a connection travelling with the pump, i.e. in the figure β is delayed on α, and the critical back edge is delayed by the length of the interconnection towards the reset sensitive edge of α. Thus if the delay in the interconnection is D, this also equals the delay down the pump. Therefore for no back-writing, if the worst tolerance on each pump is ε,

$$2D+2\varepsilon < T/6$$

It was decided that the shortest maximum interconnection which could be allowed must be four packages, i.e. 3·75 mm ($1\frac{1}{2}$ in) or $\frac{1}{4}$ ns. T is 4 ns.

Therefore, $\varepsilon < 1/12$ ns or $T/48$, corresponding to a phase accuracy on pumps of $\pm 8^\circ$.

During the construction of the module each component was tested, at 250 MHz, on a transmission line for input impedance, insertion loss, and phase delay, and the components were selected until the phase accuracy necessary was achieved. The absolute values of the alternating voltages on the line are relatively unimportant and were held to $\pm 15\%$, over the whole module. The balance down each line was a little more important and was held to $\pm 8\%$. The pumps on a line must be accurately in antiphase and there was never more than 5° between them. A good deal of power was lost and just under half the generated a.c. power ended on the packages, most losses being due to standing waves in the $\lambda/4$ transformers. The direct voltages which largely determine the mark/space ratio of the packages, were in fact selected to give a

45 : 55 ratio, which gave an added safety to the above back-writing calculation of about 0·1 ns, corresponding to a useful 12·5 mm ($\frac{1}{2}$ in).

The complete performance of this type of logic may now be defined. A package may be converted to an AND or OR circuit by injecting a direct current from a long tail (1 kΩ) without affecting the loading. Therefore, the following configurations are allowed:

(1) Two-input, two-output AND.

(2) Two-input, two-output OR.

(3) Three-input, one-output MAJORITY.

(4) One-input, three-output amplifier.

(5) One-input amplifier with one non-inverted output and one differentiating output driving an amplifier with two outputs (inversions of the original signal).

Configurations (1)–(4) have a delay of $T/3$, configuration (5) has the non-inverted output after $T/3$, and the inverted outputs after T. In addition, one phase may be skipped with a $T/3$ delay line giving a standard output with which logic may be performed. A $2T/3$ delay is, of course, of no use, as two phases cannot be skipped without losing the directionality of the pump system, $3T/3$, $4T/3$ and $6T/3$ delays are available but dispersion reduces the signals so that logic cannot be performed with the outputs and only circuits (4) and (5) can be driven. Maximum interconnection lengths between neighbouring phases may be deduced from Fig. 8. Down the pump system, interconnections can be only four packages long: across the system, 10 packages may be crossed: against the pump system, eight packages are permissible as there is no back-writing problem.

3. Outline of the System

The circuit and assembly technique described above was considered to be suitable for use in a relatively small digital system employing up to around 2000 gates. A detailed paper study[6] of a machine embodying a tunnel diode processor revealed the need for a high degree of sophistication in order to achieve any sort of match with the speed of available main memory and no hope whatever of making a sensible computer with only 2000 tunnel diode circuits (around 12 000 circuits were considered necessary). The decision was finally reached to construct the control unit for an otherwise conventional computer and to utilize the high-speed capability of the tunnel diode circuits to achieve a new degree of flexibility by providing the control unit with a stored microprogram. The control unit has then many of the properties of a tiny computer and in fact has come to be called the 'microcomputer' at Cambridge.

It may be of interest to review the essential functions of a control unit before discussing the action of our microcomputer. To be specific we shall postulate the control for a simple machine with a one-address instruction format. In general, instructions are carried out in two distinct phases, FETCH and EXECUTE. The FETCH phase has to do with determining the address of the next instruction to be obeyed and obtaining it from main memory. In the EXECUTE phase the operand (if any) is obtained from memory and some operation (such as add to accumulator) specified by the instruction code, is carried out. Each phase comprises a sequence of elementary operations, known as microsteps, suitably spaced in time to allow the circuits

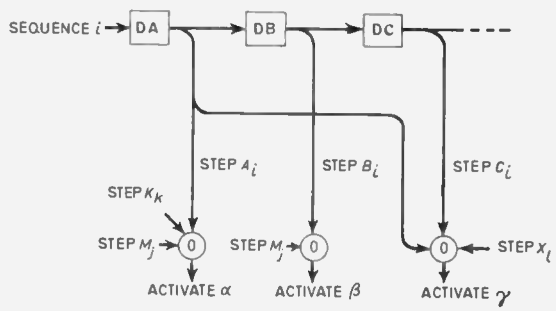

Fig. 10. Simple control sequence.

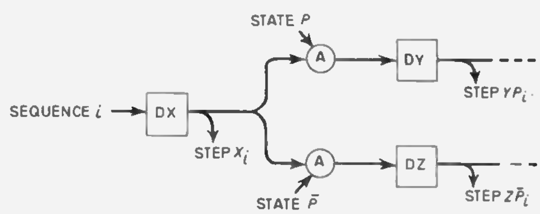

Fig. 11. Branching on control state P.

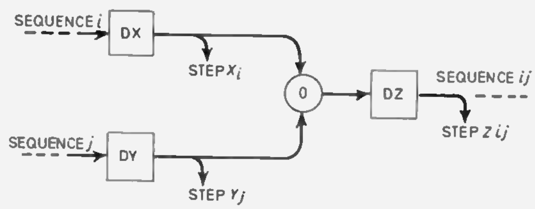

Fig. 12. Merging of two sequences.

activated on each microstep to settle by the time they are next used. A number of circuits may be activated in unison on each step and any given circuit may be activated from a number of different microsteps. An example of a stylized circuit for generating control activations is shown in Fig. 10. Sequence i is generated by a chain of delay elements DA_i, DB_i, etc., providing successive signals $stepA_i$, $stepB_i$, etc. The activation signals are generated by OR-ing together the appropriate step signals. Thus B is activated on step B in sequence i and on step M in sequence j. We can imagine the injection of a pulse into such an arrangement as initiating a chain of events, each event being provoked by a pattern of pulses which emerge on the activation wires. Sequences can be arranged which branch on the condition of a control state (Fig. 11) or merge into a common route (Fig. 12).

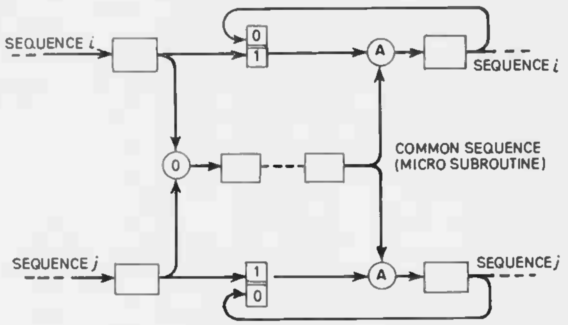

Fig. 13. Entering and leaving a micro-subroutine.

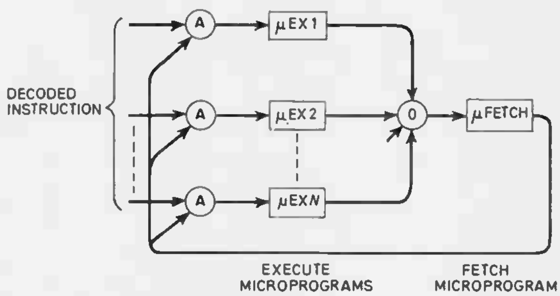

Fig. 14. Microprogram sequencing.

A group of connected sequences which controls the execute phase for a single instruction is known as the 'microprogram' for that instruction.[7] Simple extensions can be devised which permit 'micro-subroutines' to be implemented for those sequences which are common to a number of different microprograms. Figure 13, for example, shows a sequence forming a micro-subroutine called from two microprograms. At the end of each EXECUTE microprogram the FETCH microprogram is entered to extract and decode the next instruction. The decoded instruction then causes the appropriate execute microprogram to be entered after which the process repeats (Fig. 14). Control units are not, of course, normally constructed in quite this way (particularly as regards the delay elements) but the illustrations are useful in relating the behaviour required of a control unit with the facilities provided by the microcomputer.

It is interesting to note that the control sequences described so far are totally sequential and bear a close resemblance to a conventional (single-processor) program—hence the term micro-programming. We can in fact devise a very simple extension, illustrated in Fig. 15, which has an analogy with parallel (multiprocessor) programming. A control sequence i is shown stimulating a number of sequences $i1$, $i2$, $i3$ in unison, each sequence operating independently of the others. The problem of synchronizing events between the various microprograms is similar to the problem of co-ordinating the activities of co-operative parallel

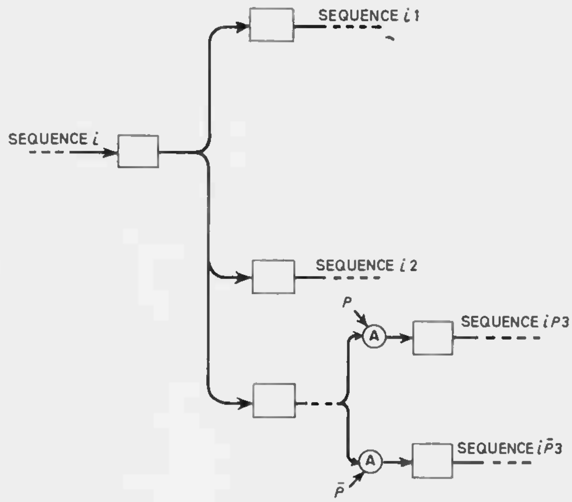

Fig. 15. Parallel microprograms.

programs. (See for example Dijkstra.[8]) Existing microprogrammed computers do not utilize parallel microprograms, probably because the sort of read-only memory in which microprograms are usually stored does not permit more than one access at a time. The tunnel diode microcomputer described below could be readily extended to execute parallel microprograms but a detailed design of such a system has not been carried out.

The tunnel diode microcomputer employs a serial-parallel delay line memory, holding 512 words of 6 bits. Six identical lines each comprising 16 sections of 128 ns are arranged as shown in Fig. 16. Any of the 16 regenerating stages can be selected as a read station and 6-bit words then flow out to the output register at a rate of one word every 4 ns (corresponding with the 250 MHz pump frequency). By selecting the 'nearest' read station any address in memory can be read with an access time of 128 ns or less (average 64 ns) but, since only one write station is provided, the write access time may be up to 2048 ns. The property of a long average access time coupled with a high word-rate after access is exploited to model control sequences as follows. Words which flow on to the output registers are regarded as 6-bit names of activation signals. A burst of these names is decoded and stretched in time to generate the activations required on a given microstep, after which the outputs are shut off and a new address is set up on the microstore. The access time to this address is used to provide the delay required before the next burst of gate names occurs on the next microstep. A number of features are provided to give some measure of control over this delay and to permit branching and merging of sequences and the use of micro-subroutines. The major units of the microcomputer are shown in Fig. 17. The machine operates in one of two modes, RUN or CONTROL. In RUN mode the 6-bit words issuing from the microstore pass through SBR and into the decoder (at 250 MHz) to generate activation signals on one out of 62 of the 64 decoder output wires. When either of the remaining outputs of the decoder is stimulated the gates from the microstore are shut off and the machine switches to CONTROL mode. By the time this can be done two further word times have elapsed and these words are staticized in SBR to control the further action of the machine. In one case (word = 000001) an immediate reversion to RUN mode occurs. The effect is simply that the store loses and then regains synchronism, causing the selected read station to advance by one, introducing a delay of 128 ns before the stream of words from the microstore is reconnected to the decoder. In the other case (word = 000000) the contents of SBR is interpreted as a 12-bit instruction which is executed before RUN mode is again selected. The format of the 12-bit

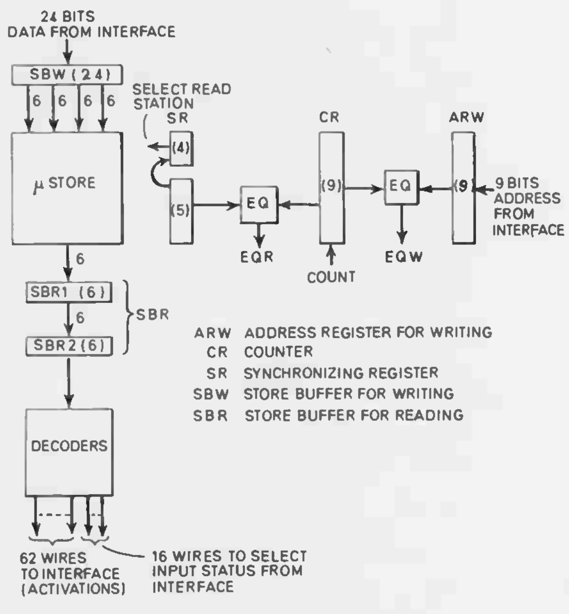

Fig. 17. The microcomputer.

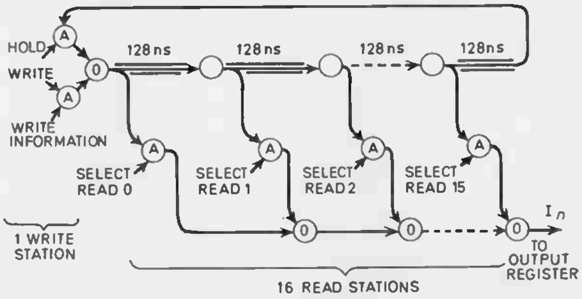

Fig. 16. The microstore; arrangement of 512-bit lines.

CONTROL mode instruction is shown below:

First two bits 00, 01, or 10

(3)	(9)
3-bit operation code	9-bit address

First two bits 11

(2)	(4)	(6)
2-bit operation code	4-bit input status address	6-bit relative address

First 3 bits	*Mnemonic*	*Action*
000	WRR	Write from reader and jump to absolute address.
001	WRC	Write from core and jump to absolute address.
010	JMS	Jump to subroutine at absolute address (enter). Put link in ARW.
011	JME	Jump from subroutine (exit). Take link from ARW.
100	JMP	Jump to absolute address.
101	JMM	Jump to absolute address in ARW.
11X	JMR	Relative jump ($\pm$ 5 bits) if selected status line is 0 (not set).

The microcomputer communicates with the outside world via interface circuits which match the tunnel diode circuits with conventional 10 MHz transistor logic. Four nanosecond pulses emitted from the decoder are stretched in the interface to 50 ns, so that the succession of 4 ns pulses issued to the interface in RUN mode produce overlapping activation signals to the controlled circuits. A simple paper tape reader may be connected to the interface for loading the microstore initially. A stream of zero words (000000) issuing from the microstore then causes the loading of words directly from the reader. The ARW and SBW registers are loaded by the reader logic and a busy signal generated by the reader inhibits RUN mode while the reader is stepping.

4. The Machine Construction

The packages fit into six modules, each module carrying 312 packages. A module consists basically of a copper earth plane, pierced with 312 slots, through which project the top 1·2 cm (0·25 in) of the substrates carrying the summing resistors of the packages. Thus on one side of the plane lie all the interconnecting wires, on the other side the pump distribution. The latter consists of 24 tapered balanced transmission lines matched into the 25 Ω input impedances of the packages, there being 13 packages to a line. Each line is driven by a bifilar transmission line transformer (see Ruthroff [5]), which restores balance and produces the two antiphase pumps. Direct current is added at two flip-chip capacitors at the earthy ends of the windings. The input impedance of a line is 3·5 Ω and the transformers, being mismatched to the lines, appear inductive to the source. The inductance is tuned out by lumped capacitors, which also block d.c. from the rest of the a.c. system, to give a final input impedance of 220 Ω to the line of 13 packages. Eight lines are then connected in parallel to a distributing transmission line fed by a $\lambda/4$ transformer to present an input impedance of 100 Ω to each of three phases, the three phases being produced by 100 Ω delay lines, matched with another $\lambda/4$ transformer into 80 Ω balanced feeder. Apart from the bifilar transformers, short connecting links of bifilar 100 Ω line between boards, and the very first $\lambda/4$ transformer, the distribution transmission lines are etched from glass-fibre printed circuit board, and consist of balanced conductors between earth planes.

One cabinet was designed to hold the six tunnel diode modules, their ancillary a.c. and d.c. power supplies, a cooling system, the delay lines for the microstore, and the interface circuits linking the tunnel diode signals with standard transistor circuits. The six modules fit on to a single panel so that all the interconnections are accessible from the front and lie in one plane. These modules are cooled by cold water from a thermo-electric module mounted on a chassis at the top of the cabinet. This chassis also holds conventional d.c. supplies for the modules and a valve oscillator to supply the 250 MHz power supply. Below the modules is a small control panel and then two boxes of interface circuits. Behind the modules are the cables for the delay line store. These cables are wound into four drums, each drum, holding 24 cables, measures 30 cm (12 in) diameter by 15 cm (6 in) deep. The cables consist of mineral-filled coaxial cable, which is semi-flexible, and is of sufficiently low dispersion to allow 31 bits to be stored in each. The characteristic impedance was found to be 33 Ω and the lines are matched into the tunnel diode packages with 33 Ω bifilar wire via a 192-way coaxial plug and socket. The lines were measured by a simple reflection method and were easily made accurate to 100 ps. As shown in Fig. 16, they are used in a non-reflection mode, which is extravagant of cable but economical of packages, since only one write-station per bit is required, instead of one per cable, as would be necessary if a reflection mode were used.

Since a sufficient number of satisfactory tunnel diodes were not delivered, only a representative part of the machine could be made. This included the following:

- 512 3-bit words of microstore.
- Address decode tree to select reading stations.
- Single-shot writing circuit to load store.
- Nine-stage binary counter.
- Four-bit full adder.
- Data transfer between modules.
- Data transfer from transistor circuits to tunnel diode circuits.
- Data transfer from tunnel diode circuits to transistor circuits.

No great difficulty was experienced in mechanizing the required logic, and apart from the use of the majority element, the logical design was quite conventional based mainly on a two-wire system using AND or OR gates. Inverters were not often used inside a block of logic, mainly owing to the extra delay, but once a function had been made it was very convenient to invert it in order to provide the complement for the next block of logic, rather than make the complement

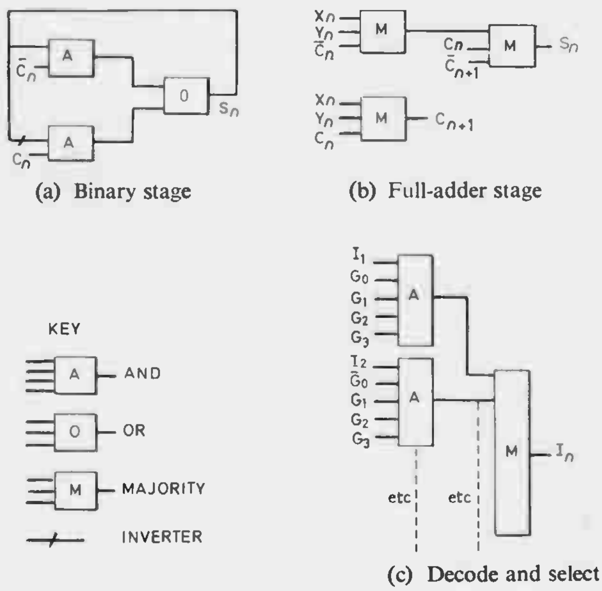

Fig. 18. Typical logic diagrams.

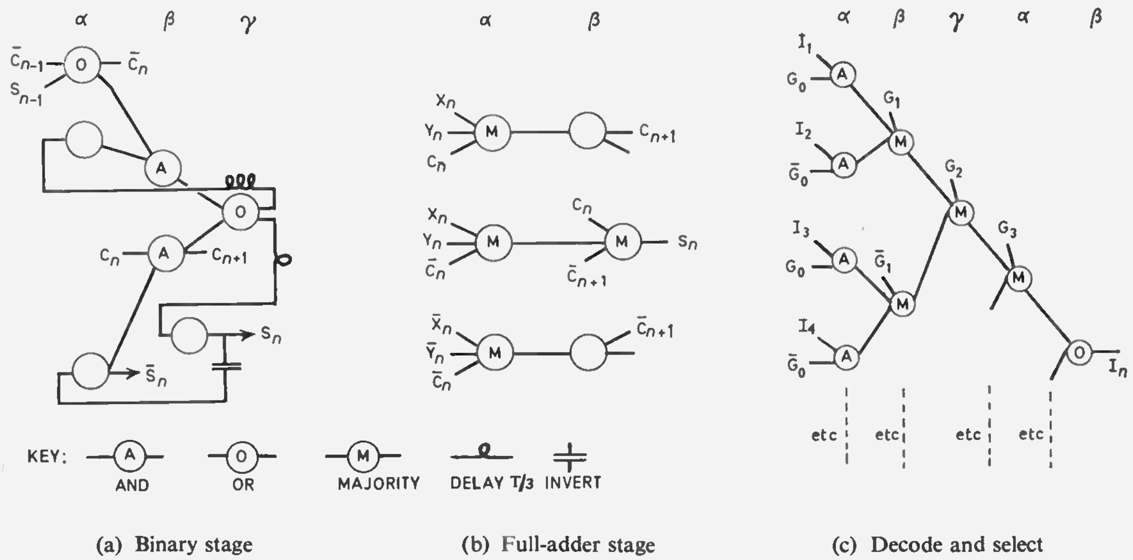

Fig. 19. Mechanization of Fig. 18.

from the two wire inputs. In Fig. 18 are shown conventional logic diagrams of a binary stage, a full adder stage, and a stage of decoding for address selection. Actual mechanization of these three circuits in terms of packages is shown in Fig. 19.

5. General Comments

A substantial part of the microcomputer has been built and operated. It is probably the largest array of digital logic which has been demonstrated working at speeds of around 250 MHz. In this section we discuss some of the conclusions we have drawn regarding experiments of this sort and what we consider to be the future prospects for machines like the microcomputer.

The tunnel diode technology we have developed has, of course, been outmoded in a number of ways by modern integrated circuit technology. The development of tunnel diodes, and particularly of integrated circuits employing tunnel diodes, has not been pursued with intensity by the device makers, with the result that many of the problems associated with the use of these devices in large-scale systems (e.g. stability, fragility, cost) have not been solved. We have been hampered by poor quality diodes since the project began and the present situation is clearly such as to preclude the use of tunnel diodes in large-scale systems. However, many of the circuit techniques developed for the microcomputer project are not peculiar to the use of tunnel diodes and may find a wider field of application. Indeed, even tunnel-diode logic, similar to that we describe, may find application in those special areas where a sufficiently high processing speed cannot be obtained simply by adopting more and more parallelism. Such problems, which demand a high bit rate per circuit, may be solved by a small-scale tunnel diode array—a system employing some 200 to 300 gates would not, we believe, introduce serious problems with reliability, etc., compared with the remainder of a typical currently available large system.

Machines employing a variable microprogram (stored logic it is sometimes called) are not (yet) common, for two main reasons:

(1) There is ordinarily a very large speed penalty, usually because the microprogram store is slow compared with the basic circuits or because the machine has no parallel microprogramming capability.

(2) The increasing use of high-level languages has reduced the user's awareness of the detailed structure of the machine and hence his capacity to design machine codes for special applications.

We believe that each of these difficulties is being slowly eroded by the improvements which are occurring in device technology and by the tremendous increases taking place in system program sophistication. As examples in each of these areas consider

(a) In the last five years core speeds have increased roughly by a factor of 4 and cheapened by a factor of 2 or 3. Logic circuits have in the same time increased in speed by a factor of 10 and cheapened by a factor of 20 or more. Thus the cost in both money and speed of using stored logic is falling dramatically.

(b) With the introduction of machine description languages, such as Schorr's register transfer language[9] it is becoming easy to write microprograms for a given machine to administer some complex function. For example, the page turning algorithm for a big multi-programmed machine or an interrupt unscrambler for a medium-size machine could profitably be tailored according to the application, loading and configuration. If, say, one (of several) disk channels should break down then a new microprogram could be called to administer the remaining channels in the best possible way. The development of supervisor systems would involve the design of both programs and microprograms and since such systems normally continue to evolve throughout the life of the computer ('bugs' are being removed and improvements are being added) the need for *stored* microprograms is clear.

6. Acknowledgments

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STANDARD FREQUENCY TRANSMISSIONS—February 1969

(Communication from the National Physical Laboratory)

February 1969	Deviation from nominal frequency in parts in 10^{10} (24-hour mean centred on 0300 UT)			Relative phase readings in microseconds N.P.L.—Station (Readings at 1500 UT)	
	GBR 16 kHz	MSF 60 kHz	Droitwich 200 kHz	*GBR 16 kHz	†MSF 60 kHz
1	− 299·9	+ 0·1	0	522	456·9
2	− 300·1	0	0	523	455·9
3	− 299·7	0	+ 0·1	520	456·0
4	− 299·4	0	+ 0·1	515	456·0
5	− 299·9	+ 0·1	+ 0·1	514	454·8
6	− 300·0	0	+ 0·1	514	457·8
7	− 300·0	0	0	514	457·5
8	− 299·8	− 0·1	+ 0·1	512	458·4
9	− 299·7	+ 0·1	+ 0·1	509	457·0
10	− 299·6	+ 0·1	+ 0·1	505	455·8
11	− 300·1	− 0·1	+ 0·1	506	433·5
12	− 300·2	− 0·2	0	508	435·6
13	− 300·2	− 0·1	0	510	436·6
14	− 300·1	− 0·2	0	511	438·4

February 1969	Deviation from nominal frequency in parts in 10^{10} (24-hour mean centred on 0300 UT)			Relative phase readings in microseconds N.P.L.—Station (Readings at 1500 UT)	
	GBR 16 kHz	MSF 60 kHz	Droitwich 200 kHz	*GBR 16 kHz	†MSF 60 kHz
15	− 300·2	− 0·1	+ 0·1	513	439·3
16	− 300·1	0	+ 0·1	514	422·5
17	− 300·2	− 0·2	+ 0·1	516	424·3
18	− 300·1	− 0·2	0	517	435·8
19	− 300·1	− 0·1	0	518	436·6
20	− 300·2	− 0·1	0	520	—
21	− 300·2	− 0·2	0	522	—
22	− 300·1	− 0·1	0	523	437·9
23	− 300·1	0	0	524	437·9
24	− 300·0	− 0·1	0	524	439·3
25	− 300·0	0	0	524	439·6
26	− 300·1	− 0·1	+ 0·1	526	440·3
27	− 300·0	0	+ 0·1	526	439·9
28	− 300·0	0	+ 0·1	526	439·8

All measurements in terms of H.P. Caesium Standard No. 334, which agrees with the N.P.L. Caesium Standard to 1 part in 10^{11}.
* Relative to UTC Scale; (UTC_{NPL} — Station) = +500 at 1500 UT 31st December 1968.
† Relative to AT Scale; (AT_{NPL} — Station) = +468·6 at 1500 UT 31st December 1968.

Of Current Interest

New Radio Telescope for Cambridge Astronomers

A new aperture synthesis radio telescope, to be known as the 'Five-kilometre Radio Telescope', is to be built at the Mullard Radio Astronomy Observatory of the Cavendish Laboratory, Cambridge, at a cost of about £2M provided by the Science Research Council. The Observatory was recently in the news with the discovery of the remarkable regularly-pulsating radio sources which have become known as pulsars.

The technique of aperture synthesis pioneered by Professor Sir Martin Ryle, F.R.S., and the Radio Astronomy Group at Cambridge and used in the present and proposed instruments, involves repeated scanning of the sky with the telescope aerials spaced at various positions along a rail in order to provide data which is progressively built up in a computer to form a map of the sky. For the new '5 km telescope' the maps will be as detailed as if a huge radio telescope dish 5 km in diameter had been used.

The 'Five-kilometre telescope' has been designed to extend one of the programmes now being carried out with the 'One-mile' instrument which is aimed at understanding the physical mechanisms occurring within quasi-stellar radio sources (quasars) and radio galaxies. With the 'One-mile telescope' it has been possible to obtain maps with a resolution of about 20 seconds of arc, but these maps have shown that many of the sources have considerable complexity in their structure which is below the present limits of resolution. The new instrument is intended to provide the increased resolution necessary to investigate structure as fine as 1–2 seconds of arc.

A disused railway track runs almost due east-west for about three miles (5 km) and provides an excellent site for the new instrument which will consist of an array of 8 paraboloid steerable aerials, four fixed and four movable on rails. The aerials will be modified versions of the 42 ft dish developed by The Marconi Company for the overseas satellite communications stations. The whole telescope array will be under the control of a Marconi *Myriad* computer.

A Federation of Science and Technology Institutes

A Council of Science and Technology Institutes (C.S.T.I.) is being formed by the Institute of Biology, the Royal Institute of Chemistry, the Institute of Mathematics and its Applications, the Institution of Metallurgists, and the Institute of Physics and the Physical Society. Its objects will be:

To make known as widely as possible the part that science and technology play in a modern community and to represent and enhance the contribution of the scientist and technologist to the well-being of every citizen.

To be a channel for the communication of common views of the member societies to Government departments, to industry and to other organizations (in particular the Royal Society and the Council of Engineering Institutions).

To make available to members of all the constituent bodies the privilege of attending meetings arranged by any one body at the same rate as charged to members of that body.

To provide joint services for members.

To aim at the adoption of common, easily understood terminology indicating levels of qualifications.

To collaborate on matters of educational policy, especially recruitment to the professions.

Membership of the Council will, at least initially, be confined to the five bodies named above. If, in the future, application were made by any other organization to join this would be considered on its merits but membership would be confined to those institutions requiring a university degree or its equivalent as a necessary standard of attainment by members eligible to have full voting rights, and organizations which covered a general field rather than those allied to particular industries or techniques.

The secretariat of the Council will be provided in turn by the constituent bodies, normally for a four-year period. Initially, the Secretary of the Institute of Physics and the Physical Society, Dr. L. Cohen, will be the Secretary of the federation. The first Chairman will be the President of the Institute of Mathematics and its Applications, Dr. P. G. Wakely.

Engineers in Canadian Armed Forces

In reply to a question in the House of Commons in Ottawa, the Canadian Minister of National Defence stated that on 1st January 1968 the Armed Services included the following number of technical officers:

	R.C.N.	*C.A.(R)*	*R.C.A.F.*	*Total*
Technical Officers	544	891	1623	3058
No. holding Engineering degrees	117	186	138	441
No. holding Science degrees	14	267	535	816
No. holding other degrees	27	34	62	123

The term technical officer covers the following: R.C.N.—officers in marine engineering, naval architecture, armaments, electrical, air engineering, construction engineering; C.A.(R)—officers serving in R.C.E., R.C. Sigs., R.C.E.M.E.; R.C.A.F.—officers serving in photography, telecommunications, armament, aeronautical engineering, mobile support equipment, construction engineering.

This compares with 393 medical doctors, 53 lawyers and 162 dentists.

Letters to the Editor

Experiences with Tropospheric Scatter Propagation Experiments

SIR,

We agree whole-heartedly with Mitchell and Fitzsimons' comments[1] that skilled effort has to be concentrated on the analysis of recorded data. Although we have collected signal strength data on a routine basis on operational links, for manpower reasons these data have been reduced only in small sections to resolve some specific point. The data are in the form of one inch/hour chart records of the continuous pen or 'Rustrak' type. Hourly medians can be estimated, but fine structure information is lost. Refractivity information has not been collated. To enable automatic analysis of the data, a system using on-site analogue-to-digital conversion and a paper-type punch is being assembled.

It should perhaps be pointed out that by far the majority of the 367 links listed by Gunther[2] are military links and certain information on these links would be classified.

We would be pleased to make available unreduced data to research workers in the field.

A. H. J. KNIGHT, B.Sc.

Cable and Wireless Ltd.,
Mercury House, Theobalds Road,
London, W.C.1. *12th February 1969.*

SIR,

The timely letter by Messrs. Mitchell and Fitzsimons[1] highlights a problem which has been awaiting a solution for a considerable time. I would like to draw attention to other aspects of this problem of interest to users of mobile tropospheric scatter equipment. Here there is concern about: (a) the standard deviation of observed transmission loss about the predicted value for a given reliability; (b) the effect of the terrain or path profile when the terminal is operating primarily in the diffraction mode.

Though a variety of prediction methods exists, suppliers of troposcatter equipment are inclined to use N.B.S. Technical Note 101[3] or C.C.I.R. Report 244–1[4] as the prediction procedure mainly in order to achieve international acceptance of their products. Hence any data obtained from the experiments suggested by the authors should ideally be co-ordinated under the auspices of a committee from one of these agencies.

The primary problem with regard to troposcatter path loss prediction is that the accuracy of prediction is heavily dependent on the data sample selected. For example, N.B.S. Technical Note 101[3] quotes a standard deviation of 3·57 dB for the difference between observed and predicted (N.B.S. method) values of long-term median path loss. Hence if the user requires a 99% service probability, a transmission loss margin as high as 9·4 dB has to be allowed. Larsen[5] on the other hand quotes an r.m.s. deviation of 8·1 dB for the N.B.S. method based on results on 15 links, which is even more pessimistic. These and other questions may not be properly resolved unless a certain amount of additional experimentation using mobile troposcatter terminals are performed.

These experiments may be necessary for the following reasons:

(a) As Mr. Fitzsimons suggested in an earlier paper,[6] most existing prediction methods are based on measurements performed at frequencies below 1 GHz. Due to the need for greater traffic capacity and consequent problems of spectrum occupancy, increasing use is being made of the bands above 3 GHz. At these frequencies the number of links currently in operation is insufficient to provide meaningful statistical data for estimating standard deviation of prediction errors. Therefore, experiments with mobile terminals under varying conditions could provide much valuable data for improving N.B.S. and/or C.C.I.R.[4] methods.

(b) The increasing use of tropospheric scatter for digital communications creates a requirement for more experimental data on the effects of multi-path differential delay. It would be difficult to measure such parameters as inter-symbol interference and pulse spreading on commercial links without disrupting communications.

In conclusion, a standard set of experiments (with a few additions to account for terrain and multi-path differential delay) on the lines suggested by Messrs. Mitchell and Fitzsimons would considerably improve prediction methods. However, it is considered that utilizing existing links alone for this purpose may not provide sufficient data to be of equipment design value in time to meet market demands. If complementary experiments using mobile terminals are performed mainly for the purpose of reducing the standard deviation of predicted errors in the N.B.S. or C.C.I.R. methods, a considerable amount of information useful to both suppliers and users of troposcatter equipment would be obtained.

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New Barnet, Hertfordshire. *20th February 1969.*

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Paper Transistors: the Foil Technique for Printed Circuits

SIR,

I have read with interest the recent article entitled 'Paper Transistors'[1] which summarized a paper given by Dr. T. P. Brody of the Westinghouse Electric Corporation at the recent International Conference on Solid State Devices in Manchester.

The vision to which the report leads up is that of 'the "printing" of complete electronic integrated circuits on a continuous tape . . . circuits on data cards, documents and credit cards to facilitate electronic processing: teaching manuals with working circuits printed in them, pads of tear-off circuits for laboratory experiments . . .'

The work on which this vision is based is the development of a technique of 'printing' of transistors on paper, plastic films or aluminium foil through depositing on these sheet materials vapours of metal and glass. Quoting again from the article: 'The transistors are about the size of the crossbar on this printed letter "T" and much thinner than the layer of ink used to print it. They can be bent, twisted and coiled—a property unique among electronic devices. The process departs completely from the idea that thin-film devices can only be fabricated on expensive, ultra-smooth and rigid insulating materials such as sapphire, quartz and glass.'

No doubt we have here an exciting development and a new emphasis on the merits of ultra-miniaturization. The main result of the development brings us back into the direction of progress for which I worked from 1940 to 1954 and which I sketched out in the early days of printed circuits (see 'Technology of Printed Circuits',[2] Chapter 20, and Ref. 3). Then, soon after World War II during which I had developed the foil technique of printed circuits to almost the identical stage at which it is still today proving the basic production process of the electronic industry, I analysed the future possibilities of integrated circuits and the form they would take. I concluded that the bulk of these circuits would be produced from flexible material and would take the form of traditional printed matter, i.e. the form of a 'loose leaf folder adapted for experimental equipment, the book form for general use and the framed picture for radio and television receivers. These and other traditional forms of printed products may be expected to appear as serious electronic devices'.[3]

I see the significance of the Westinghouse development in the approach it makes towards these time-honoured forms in which print has served mankind. The fundamental divergence of the Westinghouse process, however, is the use of a positive processing method to achieve this goal.

The Westinghouse paper transistors are made by evaporating in vacuum and depositing their component materials (tellurium, gold, silica and aluminium) and we are led to assume the same process to be adapted for the other components and connections of the integrated circuit. This adaption appears facilitated by the departure 'from the usual in-vacuum fabrication of thin-film devices a single layer at a time, with the vacuum chamber being pumped down after each layer is deposited. Instead, with a single pump-down a roll of paper or foil is passed through a "printer" one full frame at a time'.[1]

Nevertheless, and notwithstanding the appreciation of this perfection of the vacuum deposition method, the positive character of such production method is in my opinion a cardinal error of methodological approach if the method aims at the highest goal of the printed circuit technique. This error does not mean that the method is—so to speak—technically at fault or incapable of producing perfectly good integrated circuits, or that this Westinghouse method is not ideally suited to the requirements of giant electronic firms which are geared to production of identical circuits in enormous quantity. Giant firms indeed tend to favour such a positive method as they are basically interested in production facilities not suitable for small firms. Their own monopoly of the market is thereby consolidated.

But the error does mean that the method cannot help to fail in providing for electronics through the printed circuit an equivalent—however rudimentary—to what the invention of printing has provided for the whole cultural development of mankind in all the spheres which the printed word has influenced in the last five hundred years. The importance of the methodological approach cannot therefore be overstressed and it formed the basis of the paper on the foil technique, the principal negative processing method, which I read before the British Institution of Radio Engineers over fifteen years ago.[4]†

The argument is one of fundamental principle. It has become almost the cliché of a self-evident belief to expect electronic devices to carry out control functions in a myriad of production, administrative, scientific, educational, medical and numerous other branches of our life—exceeding, replacing or assisting human activities.

If only a limited number of such circuits but an enormous quantity of each were required—as is the case with present mass-produced military and entertainment equipment—the problem would not be so critical, and various methods of production may be feasible. However, this is not the problem. Any methods restricting electronic production to such limitations negate the promise which the printing of complex electronic circuits holds for the employment of electronic devices to replace, improve and extend human control and nervous functions in innumerable fields of our life.

That task entails the use of millions of different circuits, most of them only in relatively small quantities. Competition with the faculties of the human brain with its vastly superior level of competence will impose an ever-increasing complexity on these circuits and the high degree of reliability required necessitates integrated circuits consisting essentially of surface elements as distinct from body elements. Each individual task may require special circuits. Only a 'negative' production method can solve this problem.

The familiar foil technique of printed circuits which I originally developed for the interconnections of the terminals of the components of an electronic circuit is an example of a simple negative production method. Here the basis is the availability to the printer of a foil-clad

† *Editorial note.*—Dr. Eisler received the Institution's Marconi Award for his paper, considered to be the outstanding engineering contribution published in the *Journal* in 1953.

laminate, which already has—in testable form—all qualities the connecting links are desired to possess because the links are produced by printing their shapes on to the foil in an (etch) resist and removing the superfluous foil by etching or by an equivalent removal agent (e.g. heat, abrasion). The producer of these 'simple' electronic circuits has one task only, namely, to print and thereby to reproduce the shape of the conductor pattern exactly; all other requirements for the conductors have already been met by the specification of the chosen foil-clad laminate; the thickness and homogeneity of the copper foil, its bond strength, solderability, etc. Several positive methods leading to a similar end-product have been shown to be technically possible but they require more than one simple task to be achieved by the production process, e.g. the patterning and the homogeneity and thickness of the conductors. The 'negative' method of removal of unwanted material leaves the wanted product untouched as long as it is precisely outlined during the process by effective protecting means. As such patterning can be done economically, and with more or less equal perfection for small quantities or large ones, by small or by large organizations, with primitive means or automatically, it has remained the fundamental production method for connecting networks in the electronics industry since its delayed acceptance in the early fifties.

If integrated circuits are to become almost as readily producible as the printed circuits of today, the negative method of printing transistors and most other components of the electronic devices must be developed. I have described one such method twenty years ago in patents (e.g. British Patent 690,691), in articles and then in my book,[2] but it has still not been developed to its full potentiality. This method uses a thin-film multi-layer material instead of just a foil-clad insulator and from this prefabricated marketable 'raw material' not only the desired network of connections but also components of the circuit can be produced by a differential printing and etching or other subtractive technique which leaves the components patterned from their respective film layer and conductively interconnected.

If the Westinghouse achievement of multi-layer film production were to be used, not to print transistors as described by Dr. T. P. Brody, but to produce a multi-layer raw material available to the trade, as copper foil clad laminates are today, the printing of innumerable types of integrated flexible miniaturized circuits by a multitude of organizations would be an important stage nearer.

PAUL EISLER, DR.-ING., C.ENG., F.I.E.R.E.

57 Exeter Road,
London, N.W.2.

27th January 1969.

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Contributors to this Issue

Kenneth John Dean (F. 1968, A.M. 1952, A. 1946) was appointed Vice-Principal of Twickenham College of Technology in January of this year. Previously he was Head of the Department of Science and Electrical Engineering at Letchworth College of Technology. He is a graduate of London University and gained his Master's degree in 1967. His research interests are in logic design and special purpose computing and he has written numerous books, papers and articles on circuit theory and techniques (including integrated circuits) and on digital instruments. Mr. Dean is Chairman of the Institution's Components and Circuits Group Committee and his inaugural address to the Group, on Large Scale Integration, appears in this issue. He is also Chairman of the Organizing Committee for the Joint Conference on Digital Methods of Measurement and is a member of the Institution's Programme and Papers Committee.

Professor Biswaranjan Nag (*left*), is on the teaching staff of the Institute of Radio Physics and Electronics, University of Calcutta. After obtaining the degree of B.Sc. in 1951 and M.Sc.(Tech.) in 1954 from Calcutta University, he studied at the University of Wisconsin obtaining the M.S. degree in 1960. He was awarded the D.Phil. of Calcutta University in 1961, his thesis being 'Studies on Non-linear Phenomena in Electronic Oscillators'. Dr. Nag's other research interests have been electronic computers and phenomena of ionized media under hot-electron conditions and he is author of about 60 papers on these subjects.

S. K. Lahiri (*right*), is a graduate of Calcutta University, holding its B.Sc., B.Tech., and M.Tech. degrees. He joined the Solid State Electronics Laboratory of the Institute of Radio Physics and Electronics in 1967 where he now holds a Senior Research Fellowship in the Council of Scientific and Industrial Research, Government of India. He is working on acousto-electric instabilities in piezoelectric semiconductors.

Professor Nag and Mr. Lahiri's joint paper on 'Electrical Efficiency of an Acousto-electric Oscillator' is on page 143.

U.D.C. 621.372.57

Sensitivities of Six R-C Active Circuits

By

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AND

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Summary: The R-C active filters investigated use operational amplifiers as the active element and are capable of realizing second-order network functions with no finite transmission zeros. One of the networks uses positive feedback; another uses negative feedback (from an amplifier of nominally infinite gain); two use both positive and negative feedback (from a paraphase amplifier of nominally infinite gain); the fifth uses a combination of three amplifiers all of nominally infinite gain; the sixth uses a four-amplifier realization of a gyrator, again all of nominally infinite gain.

Expressions are given for the sensitivity of the Q-factor and frequency of location of the 'peak' to variations in the ratios of the passive elements and to gain. Also the effects on the Q-factor of finite gain and phase shift in the amplifier are observed.

The operational amplifiers are assumed to be of infinite input impedance and zero output impedance and to have a gain which is approximated to a first-order lag.

List of Symbols

A	open loop gain
$N(p)$	transfer function
a, b, c	coefficients of transfer function
K	defined gain of an amplifier
ω_0	undamped frequency of oscillation
ω_A	actual undamped frequency of oscillation due to finite gain of the amplifier
Q_0	Q-factor of desired response
Q_A	actual Q-factor obtained by circuit owing to finite gain of the amplifier
$N(j\omega)\|_{max}$	maximum point of magnitude response of transfer function $N(p)$ with a sinusoidal excitation
$\|N(0)\|$	magnitude response of $N(p)$ at zero frequency
ω_Q	angular frequency at which $\|N(j\omega)\|_{max}$ is located
ω_{Q_A}	actual angular frequency at which $\|N(j\omega)\|_{max}$ is located due to finite gain of the amplifier
H	term establishing d.c. conditions
$n, m, l, d, e, f, g, h, k, \alpha, \beta$	component ratios
T	time-constant, equals $R \times C$ or C/Y
S_q^Q	sensitivity of Q with respect to variations in any parameter q.
S_q^ω	sensitivity of ω_Q or ω_{Q_A} with respect to variations in any parameter q.
S_T^Q	total Q-sensitivity for a circuit
Q_τ	'predicted' Q-factor due to finite gain and phase shift in the amplifier
Q_ε	Q-factor with $\varepsilon \neq 0$
ε	$\frac{3}{2} - \frac{1}{\alpha} + \frac{1}{\beta}$

† Department of Electrical Engineering, The University of Newcastle-upon-Tyne

1. Introduction

It is well known that R-C active circuits may be employed to obtain responses of the same form as those of inductor-capacitor filters. One important matter in the design of R-C active networks is their sensitivity to variations in the values of active and passive elements. A response of particular interest is the second-order all-pole network function which may be written as:

$$N(p) = \frac{H}{ap^2 + bp + c} \qquad \ldots\ldots(1)$$

where the factor H dictates d.c. conditions. Higher-order all-pole network functions may be realized by first reducing the function to second-order factors of the form of eqn. (1) and realizing each factor with a simple circuit. The authors have realized Bessel responses of up to 8th order by this method. It would appear that any of a number of simple networks may be used to realize the second-order factors and the designer has a wide array of possible circuits from which to choose.

A Q-factor may be defined by comparing eqn. (1) with the following:

$$N(p) = \frac{H}{p^2 + \frac{\omega_0}{Q} p + \omega_0^2} \qquad \text{......(2)}$$

where ω_0, the undamped frequency of oscillation, and Q are given by:

$$Q = \frac{\sqrt{ac}}{b} \qquad \text{......(3)}$$

$$\omega_0 = \sqrt{\frac{c}{a}} \qquad \text{......(4)}$$

It is clear that the Q-factor is determined by the location of the pole-pair $p_1 p_2$ in the complex $p = \sigma + j\omega$ plane, as shown in Fig. 1(a), and as the poles approach the imaginary axis Q is increased. The higher the Q-factor required the greater is the peak of response shown in Fig. 1(b) and the greater the sensitivity of the circuit to component error. In this paper sensitivity is related to Q-factor and frequency of location of the peak for six simple circuits each capable of realizing the second-order all-pole response.

This enables the sensitivity of the circuits to be found at their most sensitive point, which is when $|N(j\omega)|$ is a maximum. This occurs at an angular frequency ω_Q where

$$\omega_Q^2 = \frac{c}{a} - \frac{b^2}{2a} \qquad \text{......(5)}$$

$$= \omega_0^2 \left[1 - \frac{1}{2Q^2}\right] \qquad \text{......(6)}$$

and $|N(j\omega)|_{\max}$ may be written in terms of the Q-factor as

$$|N(j\omega)|_{\max} = \frac{Q.H/c}{\sqrt{1 - \frac{1}{4Q^2}}} \qquad \text{......(7)}$$

but $\frac{H}{c} = |N(0)|$, the d.c. gain.

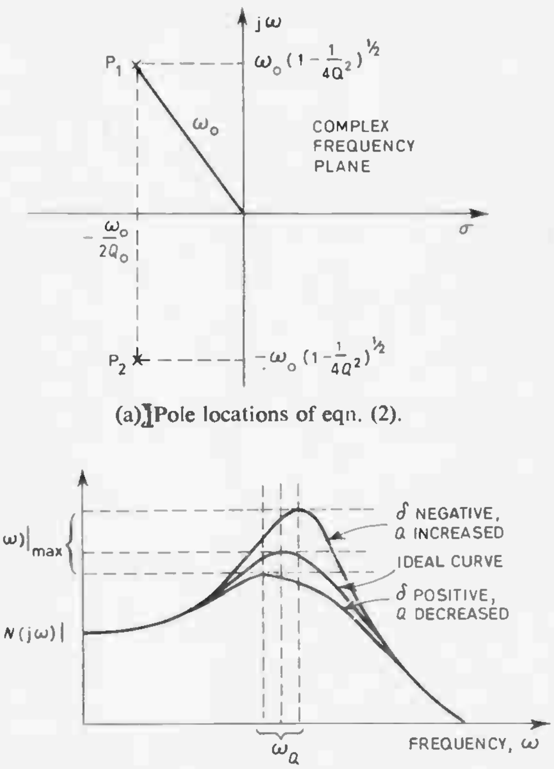
Therefore $\quad \frac{|N(j\omega)|_{\max}}{|N(0)|} \simeq Q \quad$ when $Q^2 \gg \frac{1}{4}$

The importance of the Q-factor, as a parameter of a circuit is now readily seen since both the 'frequency of the location of the peak' of the magnitude response and the 'peak' of the magnitude response itself are dependent upon its value.

The sensitivity of Q to any parameter q may be defined as

$$S_q^Q = \frac{\partial Q/Q}{\partial q/q} \qquad \text{......(8)}$$

$$S_q^Q = \frac{\partial Q}{\partial q} \cdot \frac{q}{Q} \qquad \text{......(9)}$$



(a) Pole locations of eqn. (2).

(b) Effect of variation in Q-factor.

Fig. 1.

Similarly, the sensitivity of ω_Q to variations in any parameter q is defined as

$$S_q^\omega = \frac{\partial \omega_Q}{\partial q} \cdot \frac{q}{\omega_Q} \qquad \text{......(10)}$$

Using the coefficients of eqn. (1), the following general expressions for Q and ω_Q sensitivity are obtained:

$$S_q^Q = \frac{q}{2c} \cdot \frac{\partial c}{\partial q} + \frac{q}{2a} \cdot \frac{\partial a}{\partial q} - \frac{q}{b} \cdot \frac{\partial b}{\partial q} \qquad \text{......(11)}$$

$$S_q^\omega = \frac{q}{2}\left\{\frac{1}{c} \cdot \frac{\partial c}{\partial q} - \frac{1}{a} \cdot \frac{\partial a}{\partial q} - \frac{1}{2Q^2 - 1} \times \right.$$
$$\left. \times \left(\frac{2Q}{a\omega_0} \cdot \frac{\partial b}{\partial q} - \frac{1}{c} \cdot \frac{\partial c}{\partial q} - \frac{1}{a} \cdot \frac{\partial a}{\partial q}\right)\right\} \qquad (12)$$

In general, the actual or experimental Q-factor a response exhibits will be different from the ideal Q-factor due to changes in the component values whether active or passive. The actual Q-factor Q_A may be related to the ideal Q_0 in the following way.

$$Q_A = Q_0(1 - \delta) \qquad \text{......(13)}$$

where δ is the fractional change in Q_0. This change will consequently affect the magnitude and frequency of location of the peak of the magnitude response according to the relation:

Actual magnitude of peak

$$|N(j\omega)|_{\max} \simeq Q_0(1-\delta) \qquad \ldots\ldots(14)$$

Actual frequency of location of peak

$$\omega_{QA}^2 = \omega_A^2\left[1-\frac{1}{2Q_0^2(1-\delta)^2}\right] \qquad \ldots\ldots(15)$$

Since δ may be either positive or negative this gives rise to two possible new curves as shown in Fig. 1(b).

By setting accurately the values of the passive components the effect on Q of finite gain and phase shift in the amplifier may be investigated. The transfer function of the operational amplifiers assuming infinite input impedance and zero output impedance used in these circuits may be approximated to a first-order lag having the form:

$$N(p) = \frac{A}{1+p\tau} \qquad \ldots\ldots(16)$$

In the experimental work the values of A and τ were found to be 20 000 and 0·001 respectively for the amplifiers used.

2. Sensitivity and Effects of Finite Amplifier Gain and Phase Shift for Certain R-C Active Filters

2.1. *Circuit (1): Positive Feedback (as shown in Fig. 2), with an Amplifier of Finite Voltage Gain K*

This circuit (Fig. 2) has the voltage transfer ratio

$$\frac{V_0}{V_i} = \frac{K}{p^2T^2\dfrac{m}{l} + pT\left[\dfrac{m+l+1}{l} - K\right] + 1} \qquad \ldots(17)$$

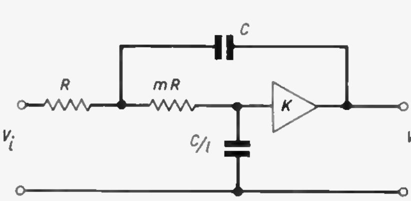


Fig. 2. Circuit (1)—Positive feedback.

2.1.1. Sensitivity

The expression for the Q-factor obtained using this circuit is

$$Q = \frac{\sqrt{lm}}{l+m+1-lK} \qquad \ldots\ldots(18)$$

The sensitivity of Q and ω_Q as realized by this circuit to variations in m, l and K may be found by using eqns. (11), (12) and (17), and are given in Tables 1 and 2 respectively.

An optimization of sensitivity to Q is considered here[1] as the 'p' term in eqn. (17) is produced by the difference between two large quantities, arising from the use of a finite gain positive feedback amplifier. By comparing coefficients of eqns. (2) and (17),

$$T^2\frac{m}{l} = \frac{1}{\omega_0^2} \qquad \ldots\ldots(19)$$

$$T\frac{m}{l} + T + \frac{T}{l} - KT = \frac{1}{Q\omega_0} \qquad \ldots\ldots(20)$$

Let $$\frac{m}{l} = x \qquad \ldots\ldots(21)$$

The optimization of sensitivity is based on the minimization of the following expression:

$$h_K|S_K^Q| + h_m|S_m^Q| + h_l|S_l^Q| \qquad \ldots\ldots(22)$$

where h_K, h_m and h_l are weighting factors and may be considered as being proportional to the tolerances in setting the gain of the amplifier and component ratios. From Table 1, using eqns. (19) and (21)

$$\left.\begin{aligned} S_K^Q &= \frac{KQ}{\sqrt{x}} \\ S_m^Q &= \tfrac{1}{2} - Q\sqrt{x} \\ S_l^Q &= -\tfrac{1}{2} + Q\sqrt{x}\left(1+\frac{1}{m}\right) \end{aligned}\right\} \qquad \ldots\ldots(23)$$

But in order to take into account that T/l must be positive, K must be greater than $1+x-(\sqrt{x}/Q)$. Therefore, set z such that

$$K = z\left(1+x-\frac{\sqrt{x}}{Q}\right) \qquad \ldots\ldots(24)$$

where z is always greater than unity. This gives

$$\left.\begin{aligned} S_K^Q &= z\left(\frac{Q}{\sqrt{x}} + Q\sqrt{x} - 1\right) \\ \text{and} \quad S_l^Q &= \tfrac{1}{2} - \frac{Q}{\sqrt{x}} + z\left(\frac{Q}{\sqrt{x}} + Q\sqrt{x} - 1\right) \end{aligned}\right\} \qquad \ldots\ldots(25)$$

Expression (22) now has a minimum when

$$x = \frac{z(h_K+h_l)-h_l}{z(h_K+h_l)+h_m} \qquad \ldots\ldots(26)$$

Consider the following two examples...

Firstly, an optimization of S_K^Q alone[2] with $h_m = h_l = 0$, yields $x = 1$ and $K = z(2-1/Q)$, where, although the sensitivity to K is a minimum, the sensitivities to the passive elements are high. Secondly, with $h_K = h_m = h_l = 1$, and assuming z to be not much greater than unity,

$$x = \frac{2z-1}{2z+1} \simeq \tfrac{1}{3} \qquad \ldots\ldots(27)$$

then $$K \simeq \frac{4}{3} - \frac{1}{Q\sqrt{3}} \qquad \ldots\ldots(28)$$

A result similar to this one has been found by Saraga,[3] through a different approach.

In general, the value of finite gain which gives the optimum overall sensitivity will be in the range z to $z(2-1/Q)$ and depends on the assignment of values to h_K, h_m and h_l.

Since a positive gain amplifier is used, the condition when the circuit becomes unstable is of great importance. The ideal value of gain, K_0 say, may be different from the actual value of gain, K_A due to tolerances in component values. It is found that if the actual value of gain exceeds the ideal value by an amount equal to or greater than $1/Q$ the circuit will oscillate, i.e. it will oscillate if

$$K_A \geqslant \frac{1}{Q} + K_0$$

2.1.2. Effects of finite amplifier gain and phase shift in the amplifier

The positive gain amplifier used here consists of two operational amplifiers with negative feedback,

Table 1

Sensitivity of Q to variations in active and passive elements

Circuit (1) Positive feedback	Circuit (2) Negative feedback
$S^Q_m = \frac{1}{2} - \frac{Q}{\omega_0 T}$	$S^Q_m = \frac{1}{2} - \frac{Q_A(n+1)}{\omega_A T n}$
$S^Q_l = -\frac{1}{2} + \frac{Q(m+1)}{\omega_0 T m}$	$S^Q_n = -\frac{1}{2} \cdot \frac{1}{1+\frac{n}{A+1}} \left\{1 - 2Q_A \omega_A T \frac{m}{l}\right\}$
$S^Q_K = Q \omega_0 T K$	$S^Q_l = -\frac{1}{2} + \frac{Q_A}{\omega_A T}\left(1 + \frac{1}{m} + \frac{1}{n}\right)$
	$S^Q_A = -\frac{1}{2} \cdot \frac{A}{(A+1)^2} \cdot \frac{n}{1+\frac{n}{A+1}} (1 - 2Q_A \omega_A T)$

Circuit (3) Positive and negative feedback	Circuit (4) Positive and negative feedback
$S^Q_m = \frac{1}{2}\left\{1 + \frac{l}{\omega_A^2 T^2 n}\right\} - \frac{Q_A}{\omega_A T} \cdot \frac{n+l}{n}$	$S^Q_m = \frac{1}{2} - \frac{Q_A(n+1)}{\omega_A T n}$
$S^Q_n = -\frac{1}{2} \cdot \frac{m+1}{m+1+\frac{n}{A_2+1}} \left\{1 - 2Q_A \omega_A T \frac{m}{m+1}\right\}$	$S^Q_n = -\frac{1}{2} \cdot \frac{1}{1+\frac{n}{A_2+1}} \left\{1 - 2Q_A \omega_A T \frac{m}{l}\right\}$
$S^Q_l = -\frac{1}{2} + \frac{Q_A(m+1)}{\omega_A T m}$	$S^Q_l = -\frac{1}{2} + \frac{Q_A}{\omega_A T}\left\{1 + \frac{1}{m} + \frac{1}{n}\right\}$
$S^Q_{A_1} = \frac{A_1}{A_2+1} \cdot \frac{Q_A l}{\omega_A T m}$	$S^Q_{A_1} = \frac{A_1}{A_2+1} \cdot \frac{Q_A l}{\omega_A T m}$
$S^Q_{A_2} = -\frac{1}{2} \cdot \frac{A_2}{(A_2+1)^2} \times \frac{n}{m+1+\frac{n}{A_2+1}} \{1 + 2Q_A \omega_A T(A_1 - 1)\}$	$S^Q_{A_2} = -\frac{1}{2} \cdot \frac{A_2}{(A_2+1)^2} \times \frac{n}{1+\frac{n}{A_2+1}} \{1 + 2Q_A \omega_A T(A_1 - 1)\}$

Table 1 (*continued*)

CIRCUIT (5)	Approximate expressions
$S_d^Q = \frac{1}{2}\left\{1+\frac{1}{\omega_A^2 T^2 efg(A_3+1)}\right\} - \frac{Q_A}{\omega_A T}\left\{\frac{1}{e}+\frac{1}{fg(A_3+1)}\right\}$	$-\frac{1}{2}$
$S_e^Q = \frac{Q_A}{\omega_A Te} - \frac{1}{2\omega_A^2 T^2 efg(A_3+1)}$	1
$S_f^Q = \frac{1}{2} - \frac{Q_A}{\omega_A T}\left\{\frac{1}{e}+\frac{1}{d(A_2+1)}\right\}$	$-\frac{1}{2}$
$S_g^Q = \frac{1}{2} - \frac{Q_A}{\omega_A T}\left\{\frac{1}{e}+\frac{1}{d(A_2+1)}\right\}$	$-\frac{1}{2}$
$S_h^Q = -\frac{1}{2} - \frac{k/h}{A_1+1+k+k/h}$	$-\frac{1}{2}$
$S_k^Q = \frac{1}{2} - \frac{1}{2}\cdot\frac{k+k/h}{A_1+1+k+k/h}$	$\frac{1}{2}$
$S_{A_1}^Q = \frac{1}{2} - \frac{1}{2}\cdot\frac{A_1}{A_1+1+k+k/h}$	0
$S_{A_2}^Q = \frac{1}{2}\cdot\frac{A_2}{(A_2+1)^2}\left\{\frac{2Q_A}{\omega_A Td}+\frac{1}{\omega_A^2 T^2 dfg}\left[\frac{kA_1A_3}{h(A_1+1+k+k/h)(A_2+1)(A_3+1)}-\frac{1}{(A_2+1)(A_3+1)}\right]\right\}$	0
$S_{A_3}^Q = \frac{1}{2}\cdot\frac{A_3}{(A_3+1)^2}\left\{\frac{2Q_A}{\omega_A Tfg}+\frac{1}{\omega_A^2 T^2 dfg}\left[\frac{kA_1A_2}{h(A_1+1+k+k/h)(A_2+1)(A_3+1)}-\frac{1}{(A_2+1)(A_3+1)}-\frac{d}{e(A_3+1)}\right]\right\}$	0

CIRCUIT (6)	Approximate expressions
$\varepsilon = \frac{3}{2} - \frac{1}{\alpha} + \frac{1}{\beta} = 0$	$\varepsilon \neq 0$
$S_m^Q = -\frac{1}{2(m+1)} + \frac{l}{mn^2\alpha^2+l}$	$S_m^Q = \frac{1}{2} + \frac{l\varepsilon}{4\omega_0 T}\left\{\frac{1}{Q_0}+\frac{1}{lQ_0}+\frac{\varepsilon}{\omega_0 T}\right\}$
$S_n^Q = \frac{l-mn^2\alpha^2}{l+mn^2\alpha^2}$	$S_n^Q = \frac{(1-l)\varepsilon}{4Q_0\omega_0 T} + \frac{l\varepsilon^2}{2\omega_0^2 T^2}$
$S_l^Q = -\frac{1}{2} + \frac{mn^2\alpha^2}{mn^2\alpha^2+l}$	$S_l^Q = \frac{Q_0\varepsilon}{\omega_0 T}$
$S_\alpha^Q = \frac{1}{2\alpha}\left\{\frac{1}{n(m+1)}+\alpha^2-\frac{2n\alpha^2(lm+l+m)}{mn^2\alpha^2+l}-1+\frac{2l}{mn^2\alpha^2+l}\right\}$	$S_\alpha^Q = -Q_0\left\{\sqrt{l}+\frac{1}{\sqrt{l}}\right\}$
$S_\beta^Q = -\frac{1}{2\beta}\left\{\frac{1}{n(m+1)}+\alpha^2-\frac{2n\alpha^2(lm+l+m)}{mn^2\alpha^2+l}\right\}$	$S_\beta^Q = Q_0\left\{\sqrt{l}+\frac{1}{\sqrt{l}}\right\}+\frac{3Q_0(l+1)}{2\omega_0 T}$

Table 2

Sensitivity of ω_Q to variations in active and passive elements

CIRCUIT (1) Positive feedback	CIRCUIT (2) Negative feedback
$S_m^\omega = -\frac{1}{2} - \frac{1}{2Q^2-1}\left\{\frac{Q}{\omega_0 T} - \frac{1}{2}\right\}$	$S_m^\omega = -\frac{1}{2} - \frac{1}{2Q_A^2-1}\left\{\frac{Q_A(n+1)}{\omega_A Tn} - \frac{1}{2}\right\}$
	$S_n^\omega = -\frac{1}{2}\cdot\frac{1}{1+\frac{n}{A+1}}\left\{1 - \frac{1}{2Q_A^2-1}\left(\frac{2Q_A\omega_A Tm}{l} - 1\right)\right\}$
$S_l^\omega = \frac{1}{2} + \frac{1}{2Q^2-1}\left\{\frac{Q(m+1)}{\omega_0 Tm} - \frac{1}{2}\right\}$	$S_l^\omega = \frac{1}{2} + \frac{1}{2Q_A^2-1}\left\{\frac{Q_A}{\omega_A T}\left(1+\frac{1}{m}+\frac{1}{n}\right) - \frac{1}{2}\right\}$
$S_K^\omega = \frac{Q\omega_0 TK}{2Q^2-1}$	$S_A^\omega = -\frac{1}{2}\cdot\frac{A}{(A+1)^2}\cdot\frac{n}{1+\frac{n}{A+1}}\left\{1 - \frac{2Q_A\omega_A T-1}{2Q_A^2-1}\right\}$

CIRCUIT (3) Positive and negative feedback	CIRCUIT (4) Positive and negative feedback
$S_m^\omega = -\frac{1}{2}\frac{1+\frac{n}{A_2+1}}{m+1+\frac{n}{A_2+1}}\left\{1+\frac{1}{2Q_A^2-1}\times\left[\frac{2Q_A\omega_A Tm}{A_2+1+n}\left(\frac{A_2+1}{n}+A_1+\frac{n}{l}\right)-1\right]\right\}$	$S_m^\omega = -\frac{1}{2} - \frac{1}{2Q_A^2-1}\left\{\frac{Q_A(n+1)}{\omega_A Tn} - \frac{1}{2}\right\}$
$S_n^\omega = -\frac{1}{2}\frac{m+1}{m+1+\frac{n}{A_2+1}}\times\left\{1-\frac{1}{2Q_A^2-1}\left(\frac{2Q_A\omega_A Tm}{m+1}-1\right)\right\}$	$S_n^\omega = -\frac{1}{2}\cdot\frac{1}{1+\frac{n}{A_2+1}}\times\left\{1-\frac{1}{2Q_A^2-1}\left(\frac{2Q_A\omega_A Tm}{l}-1\right)\right\}$
$S_l^\omega = \frac{1}{2} + \frac{1}{2Q_A^2-1}\left\{\frac{Q_A(m+1)}{\omega_A Tm} - \frac{1}{2}\right\}$	$S_l^\omega = \frac{1}{2} + \frac{1}{2Q_A^2-1}\left\{\frac{Q_A}{\omega_A T}\left(1+\frac{1}{m}+\frac{1}{n}\right) - \frac{1}{2}\right\}$
$S_{A_1}^\omega = \frac{A_1}{A_2+1}\cdot\frac{1}{2Q_A^2-1}\cdot\frac{Q_A l}{\omega_A Tm}$	$S_{A_1}^\omega = \frac{A_1}{A_2+1}\cdot\frac{1}{2Q_A^2-1}\cdot\frac{Q_A l}{\omega_A Tm}$
$S_{A_2}^\omega = -\frac{1}{2}\cdot\frac{A_2}{(A_2+1)^2}\cdot\frac{n}{m+1+\frac{n}{A_2+1}}\times\left\{1+\frac{2Q_A\omega_A T(A_1-1)+1}{2Q_A^2-1}\right\}$	$S_{A_2}^\omega = -\frac{1}{2}\cdot\frac{A_2}{(A_2+1)^2}\cdot\frac{n}{1+\frac{n}{A_2+1}}\times\left\{1+\frac{2Q_A\omega_A T(A_1-1)+1}{2Q_A^2-1}\right\}$

Table 2 (*continued*)

CIRCUIT (5)	Approximate expressions
$S_d^\omega = -\frac{1}{2} + \frac{1}{2\omega_A^2 T^2 efg(A_3+1)} - \frac{1}{2Q_A^2-1} \times \left\{\frac{Q_A}{\omega_A T}\left[\frac{1}{e} + \frac{1}{fg(A_3+1)}\right] - \frac{1}{2\omega_A^2 T^2 efg(A_3+1)} - \frac{1}{2}\right\}$	$-\frac{1}{2} - \frac{1}{2Q^2-1}$
$S_e^\omega = -\frac{1}{2\omega_A^2 T^2}\left\{\frac{1}{efg(A_3+1)} - \frac{1}{2Q_A^2-1}\left[\frac{2Q_A\omega_A T}{e} - \frac{1}{efg(A_3+1)}\right]\right\}$	$-\frac{1}{2Q^2-1}$
$S_f^\omega = -\frac{1}{2} - \frac{1}{2Q_A^2-1}\left\{\frac{Q_A}{\omega_A T}\left[\frac{1}{e} + \frac{1}{d(A_2+1)}\right] - \frac{1}{2}\right\}$	$-\frac{1}{2} - \frac{1}{2Q^2-1}$
$S_g^\omega = -\frac{1}{2} - \frac{1}{2Q_A^2-1}\left\{\frac{Q_A}{\omega_A T}\left[\frac{1}{e} + \frac{1}{d(A_2+1)}\right] - \frac{1}{2}\right\}$	$-\frac{1}{2} - \frac{1}{2Q^2-1}$
$S_h^\omega = -\frac{1}{2Q_A^2-1}\left\{\frac{1}{2} - \frac{k/h}{A_1+1+k+k/h}\right\}$	$-\frac{1}{2}\cdot\frac{1}{2Q^2-1}$
$S_k^\omega = \frac{1}{2}\cdot\frac{1}{2Q_A^2-1}\left\{1 - \frac{k+k/h}{A_1+1+k+k/h}\right\}$	$\frac{1}{2}\cdot\frac{1}{2Q^2-1}$
$S_{A_1}^\omega = \frac{1}{2}\cdot\frac{1}{2Q_A^2-1}\left\{\frac{1+k+k/h}{A_1+1+k+k/h}\right\}$	0
$S_{A_2}^\omega \simeq \frac{k}{2\omega_A^2 T^2 dfgh(A_2+1)} + \frac{1}{2Q_A^2-1}\left\{\frac{Q_A}{\omega_A T d(A_2+1)} + \frac{k}{2\omega_A^2 T^2 dfgh(A_2+1)}\right\}$	0
$S_{A_3}^\omega \simeq \frac{k-dh}{2\omega_A^2 T^2 dfgh(A_3+1)} + \frac{1}{2Q_A^2-1}\cdot\frac{1}{\omega_A Tfg(A_3+1)}\left\{Q_A + \frac{1}{2\omega_A T}\left(\frac{k}{dh} - 1\right)\right\}$	0

CIRCUIT (6)	Approximate expressions
$\varepsilon = \frac{3}{2} - \frac{1}{\alpha} + \frac{1}{\beta} = 0$	$\varepsilon \neq 0$
$S_m^\omega = \frac{1}{2(m+1)}\left\{1 - \frac{1}{2Q_0^2-1}\left[\frac{2Q_0 l}{\omega_0 T n\alpha^2} - 1\right]\right\}$	$S_m^\omega = -\frac{1}{4Q_0 \quad 2} + \frac{\varepsilon}{4Q_0\omega_0 T}$
$S_n^\omega = \frac{1}{2Q_0^2-1}\cdot\frac{l-mn^2\alpha^2}{l+mn^2\alpha^2}$	$S_n^\omega = -\frac{\varepsilon(l+1)}{4Q_0\omega_0 T}$
$S_l^\omega = \frac{1}{2} - \frac{1}{2Q_0^2-1}\left\{\frac{Q_0 mn}{\omega_0 T(m+1)} - \frac{1}{2}\right\}$	$S_l^\omega = \frac{1}{2} - \frac{\varepsilon}{2Q_0\omega_0 T}$
$S_\alpha^\omega = \frac{-lm}{2\alpha(m+1)}\left\{\frac{1}{\omega_0^2 T^2}\left(n - \frac{2}{\alpha}\right) - \frac{1}{lmn} - \frac{1}{2Q_0^2-1} \times \left[\frac{2Q_0}{\omega_0 T}\left(1 + \frac{1}{l} + \frac{1}{m} - \frac{2}{mn\alpha}\right) - \frac{1}{lmn} - \frac{1}{\omega_0^2 T^2}\left(n - \frac{2}{\alpha}\right)\right]\right\}$	$S_\alpha^\omega = 1 + \frac{\varepsilon\sqrt{l}}{\omega_0 T} + \frac{1}{4Q_0}\left(3\sqrt{l} + \frac{1}{\sqrt{l}}\right)$
$S_\beta^\omega = \frac{lm}{2\beta(m+1)}\left\{\frac{n}{\omega_0^2 T^2} - \frac{1}{lmn} - \frac{1}{2Q_0^2-1} \times \left[\frac{2Q_0}{\omega_0 T}\left(1 + \frac{1}{l} + \frac{1}{m}\right) - \frac{1}{lmn} - \frac{1}{\omega_0^2 T^2}\right]\right\}$	$S_\beta^\omega = \left\{\frac{\varepsilon\sqrt{l}}{\omega_0 T} - \frac{1}{4Q_0}\left(\sqrt{l} + \frac{1}{3\sqrt{l}}\right)\right\}\left\{1 - \frac{3\sqrt{l}}{\omega_0 T}\right\}$

connected in cascade and using the experimental values, has the voltage transfer ratio

$$\frac{V_{out}}{V_{in}} \simeq \frac{2}{1+p2{\cdot}5\times10^{-6}} \qquad \ldots\ldots(29)$$

If K in the voltage transfer ratio equation (17) is replaced by $K_A/(1+p\tau')$, neglecting the p^3 term, the following expression for 'predicted' Q-factor, Q_τ, may be obtained and its value is given in Table 3. The effects of phase shift dominate and using values of K_A and τ' given in eqn. (29) it can be shown that the maximum values of Q-factor (Q_τ) attainable when $\omega_0 = 10^3$, 10^4 and 10^5 radians per second are 400, 41 and 4·9 respectively.

2.2. *Circuit (2): Negative Feedback (as shown in Fig. 3)*

The voltage transfer ratio for this circuit (Fig. 3) if the active element is of finite gain, is

$$\frac{V_0}{V_i} = \frac{-\dfrac{A}{A+1}}{p^2T^2\dfrac{m}{l} + pT\left[\dfrac{m}{ln}+\dfrac{1}{l}+\dfrac{m}{l}+\dfrac{1}{A+1}\right]+\dfrac{1}{n}+\dfrac{1}{A+1}} \qquad \ldots\ldots(30)$$

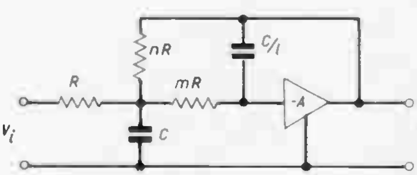


Fig. 3. Circuit (2)—Negative feedback.

2.2.1 Sensitivity

The Q-factor obtained by this circuit, assuming the amplifier to have finite gain, is

$$Q_A = \frac{\sqrt{lmn}\sqrt{1+\dfrac{n}{A+1}}}{m+n+mn+\dfrac{ln}{A+1}} \qquad \ldots\ldots(31)$$

The sensitivities of Q_A and ω_{Q_A} to variations in m, n, l and A are given in Tables 1 and 2 respectively. Foss and Green[4] have shown a relationship between circuits (1) and (2), but since the comparison assumes the use of ideal amplifiers an optimization of Q to the amplifier gain does not logically follow.

2.2.2. Effects of finite amplifier gain and phase shift in the amplifier

The expression for 'predicted' Q-factor, Q_τ is obtained by substitution of $A/(1+p\tau)$ for A into eqn. (30) and neglecting the p^3 term, its value being given in Table 3.

Note that Q_τ is approximately of the form

$$Q_\tau \simeq \frac{1}{\dfrac{1}{Q_0}+\dfrac{uQ_0}{A+1}} \qquad \ldots\ldots(32)$$

where $u = 1+(n/m)+n$. Its value will be a maximum when $Q_0 = \sqrt{(A+1)/u}$ and therefore the maximum Q_τ attainable is given by

$$Q_{\tau_{max}} \simeq \frac{A+1}{2\sqrt{u(A+1)}+\tau\omega_0(n+1)} \qquad \ldots\ldots(33)$$

It may now be seen that the value of ideal Q-factor, Q_0 for which Q_τ is a maximum, is about twice the value of Q_τ. Also since u will always be somewhat greater than unity, the attainable Q-factor is somewhat less than $\sqrt{(A+1)/2}$.

2.3. *Circuit (3): Positive and Negative Feedback Combined (as shown in Fig. 4)*

The voltage transfer ratio for this circuit (Fig. 4) which uses a paraphase active element is given by

$$\frac{V_0}{V_i} = \frac{-\dfrac{A_2}{A_2+1}}{p^2T^2\dfrac{m}{l}+pT\left[\dfrac{m}{n}+\dfrac{1}{l}+\dfrac{m}{l}-\dfrac{A_1-1}{A_2+1}\right]+\dfrac{1}{n}+\dfrac{1}{m}+\dfrac{1}{A_2+1}} \qquad \ldots\ldots(34)$$

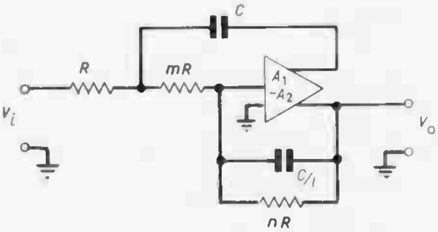


Fig. 4. Circuit (3)—Positive and negative feedback.

2.3.1 Sensitivity

Assuming the amplifier to have finite gain, the Q-factor obtained is

$$Q_A = \frac{\sqrt{lmn}\sqrt{m+1+\dfrac{n}{A_2+1}}}{ml+mn+n-\dfrac{ln(A_1-1)}{A_2+1}} \qquad \ldots\ldots(35)$$

The sensitivities of Q_A and ω_{Q_A} to variations in m, n, l, A_1 and A_2 are given in Tables 1 and 2 respectively.

Table 3
'Predicted' Q-factor, Q_τ

Circuit number	Value of Q_τ
(1)	$\dfrac{\sqrt{1+\tau\omega_0\left(K+\dfrac{1}{Q_0}\right)}}{\dfrac{1}{Q_0}+K-K_A+\tau\omega_0}$
(2)	$\dfrac{\sqrt{1+\dfrac{n}{A+1}}\sqrt{1+\dfrac{\tau\omega_0 T}{A+1}\left(\dfrac{1}{Q_0}+n\omega_0\right)}}{\dfrac{1}{Q_0}+\dfrac{\tau\omega_0}{A+1}(n+1)+\dfrac{Q_0}{A+1}\left(1+\dfrac{n}{m}+n\right)}$
(3)	$\dfrac{\sqrt{1+\dfrac{n}{m+1}\cdot\dfrac{1}{A_2+1}}\sqrt{1+\dfrac{\tau\omega_0}{A_2+1}\left(\dfrac{1}{Q_0}+\dfrac{2\omega_0 Tn}{m+1}\right)}}{\dfrac{1}{Q_0}+\dfrac{\tau\omega_0}{A_2+1}\left(1+\dfrac{n}{m+1}\right)+\dfrac{\omega_0 Tn}{m+1}\left(\dfrac{A_2-A_1+2}{A_2+1}\right)}$
(4)	$\dfrac{\sqrt{1+\dfrac{n}{A_2+1}}\sqrt{1+\dfrac{\tau\omega_0}{A_2+1}\left(\dfrac{1}{Q_0}+2\omega_0 Tn\right)}}{\dfrac{1}{Q_0}+\dfrac{\tau\omega_0}{A_2+1}(1+n)+\omega_0 Tn\left(\dfrac{A_2-A_1+2}{A_2+1}\right)}$
(5)	$\dfrac{\sqrt{1+\dfrac{dh}{Aek}}\sqrt{1+\dfrac{1}{A}\left\{\left(1+\dfrac{\tau\omega_0}{Q_0}\right)\left(k+\dfrac{k}{h}+3\right)+\dfrac{\tau\omega_0 e}{Q_0}\left(\dfrac{1}{d}+\dfrac{1}{fg}\right)\right\}}}{\dfrac{1}{Q_0}+\dfrac{1}{AQ_0}\left\{k+\dfrac{k}{h}+3+\dfrac{e}{d}+\dfrac{e}{fg}+\dfrac{\tau\omega_0}{Q_0}\cdot\dfrac{e}{fg}\right\}}$
(6)	$\dfrac{\sqrt{1-\dfrac{10}{A}+\dfrac{12\alpha n}{A}}\sqrt{1+\dfrac{12}{\alpha An(m+1)}+\alpha\tau\omega_0\sqrt{l}\left\{\dfrac{12}{\alpha A}\left(1+\dfrac{1}{l}+\dfrac{1}{m}\right)-\dfrac{10}{A}\right\}}}{\dfrac{1}{Q_0}+\dfrac{12\sqrt{l}}{A}\left(1+\dfrac{1}{l}+\dfrac{1}{m}\right)-\dfrac{10\sqrt{l}}{\alpha Amn}+\dfrac{\alpha\tau\omega_0 12n}{A}-\dfrac{10\tau\omega_0}{A}}$

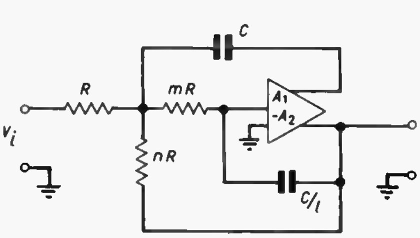


Fig. 5.
Circuit (4)—Positive and negative feedback.

2.3.2. Effects of finite amplifier gain and phase shift in the amplifier

The expression for 'predicted' Q-factor is obtained by substitution of $A_1/(1+p\tau)$ for A_1 and $A_2/(1+p\tau)$ for A_2 into eqn. (34) and neglecting the p^3 term, its value being given in Table 3.

2.4. *Circuit (4): Positive and Negative Feedback Combined (as shown in Fig. 5)*

The voltage transfer ratio for this circuit (Fig. 5) is given by

$$\frac{V_0}{V_i} = \frac{-\dfrac{A_2}{A_2+1}}{p^2T^2\dfrac{m}{l} + pT\left[\dfrac{m}{ln} + \dfrac{m}{l} + \dfrac{1}{l} - \dfrac{A_1-1}{A_2+1}\right] + \dfrac{1}{n} + \dfrac{1}{A_2+1}} \qquad \ldots\ldots(36)$$

2.4.1. Sensitivity

Assuming the amplifiers to have finite gain, the Q-factor obtained is

$$Q_A = \frac{\sqrt{lmn}\sqrt{1+\dfrac{n}{A_2+1}}}{m+mn+n-\dfrac{ln(A_1-1)}{A_2+1}} \qquad \ldots\ldots(37)$$

The sensitivities of Q_A and ω_{Q_A} to variations in m, n, l, A_1 and A_2 are given in Tables 1 and 2 respectively.

2.4.2. Effects of finite amplifier gain and phase shift in the amplifier

In a way similar to that described in Section 2.3, but by using eqn. (36), the expression for predicted Q-factor may be found (see Table 3).

2.5. *Circuit* (5) (*Fig. 6*)

This circuit (Fig. 6) has the voltage transfer ratio

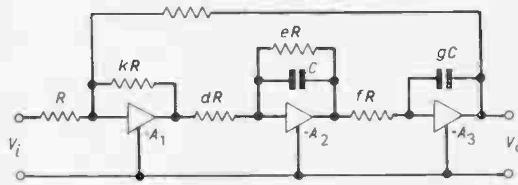


Fig. 6. Circuit (5).

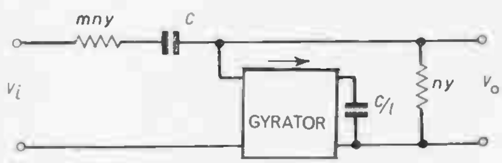


Fig. 7. Circuit (6)—Gyrator high-pass filter.

$$\frac{V_0}{V_i} = \frac{-\dfrac{A_1A_2A_3k}{(A_1+1+k+k/h)(A_2+1)(A_3+1)}}{p^2T^2dfg + pT\left[\dfrac{dfg}{e} + \dfrac{d}{A_3+1} + \dfrac{fg}{A_2+1}\right] + \dfrac{1}{(A_2+1)(A_3+1)} + \dfrac{d}{e(A_3+1)} + \dfrac{A_1A_2A_3k}{h(A_1+1+k+k/h)(A_2+1)(A_3+1)}} \qquad \ldots\ldots(38)$$

2.5.1. Sensitivity

Assuming the amplifiers to be of finite gain, the Q-factor is given by

$$Q_A = \frac{\sqrt{\dfrac{A_1A_2A_3}{h(A_1+1+k+k/h)(A_2+1)(A_3+1)} + \dfrac{d}{ek(A_3+1)} + \dfrac{1}{k(A_2+1)(A_3+1)}}}{\dfrac{1}{e}\sqrt{\dfrac{dfg}{k}} + \sqrt{\dfrac{d}{fgk}}\cdot\dfrac{1}{A_3+1} + \sqrt{\dfrac{fg}{dk}}\cdot\dfrac{1}{A_2+1}} \qquad \ldots\ldots(39$$

Both accurate and approximate expressions for the sensitivities of Q_A and ω_{Q_A} to variations in d, e, f, g, h, A_1, A_2 and A_3 are given in Tables 1 and 2 respectively.

2.5.2. Effects of finite amplifier gain and phase shift in the amplifier

If in eqn. (38), A_1, A_2 and A_3 are replaced by $A/(1+p\tau)$ and by neglecting the terms of order $1/A^2$ and $1/A^3$, and p^3 terms, an approximate expression for 'predicted' Q-factor may be found and its value is given in Table 3.

2.6. *Circuit* (6): *A Second-order Gyrator High-pass Filter* (*Fig. 7*)

The high-pass filter arrangement is realized here because of the difficulties in obtaining an ungrounded gyrator. The problem can be overcome by using two gyrators[5] but for the purposes of this investigation the high-pass case is preferred since the number of operational amplifiers required is kept low.

The gyrator is realized by the parallel connection of two ideal voltage-controlled current sources, and the circuit configuration used here is one suggested by Morse and Huelsman[6] using four operational amplifiers of the same type as in the previous circuits. The gyrator circuit is given in Fig. 8, and assuming the amplifier gains are finite, has the following nodal admittance matrix:

$$\begin{vmatrix} y\left\{\frac{3}{2}+\frac{1}{\alpha}+\frac{1}{\beta}-\frac{2}{\alpha}\cdot\frac{1}{1+4/A_1}\cdot\frac{1}{1+2/A_3}-\frac{2}{A_1(1+4/A_1)}-\frac{1}{2A_4(1+3/A_4)}\right\} & -y\left\{\frac{1}{\alpha}\cdot\frac{1}{1+4/A_1}\cdot\frac{1}{1+2/A_2}-\frac{1}{A_1(1+4/A_1)}-\frac{1}{A_4(1+3/A_4)(1+3/A_3)}\right\} \\ y\left\{\frac{1}{\alpha}\cdot\frac{1}{1+3/A_4}-\frac{1}{A_1(1+4/A_1)}\right\} & y\left\{\frac{3}{2}+\frac{1}{\alpha}+\frac{1}{\beta}-\frac{2}{\alpha}\cdot\frac{1}{1+3/A_3}\cdot\frac{1}{1+3/A_4}-\frac{2}{A_3(1+3/A_3)}-\frac{1}{2A_1(1+4/A_1)}\right\} \end{vmatrix} \quad \text{......(40)}$$

Assuming the amplifiers to be of infinite gain, the voltage transfer ratio is given by:

$$\frac{V_0}{V_i}=-\frac{p^2\frac{T^2}{l}+pT\varepsilon}{p^2\frac{T^2}{l}\left(1+\frac{1}{m}+\frac{\varepsilon}{mn}\right)+pT\left[\frac{n}{l}+\frac{1}{mn\alpha^2}+\varepsilon\left(1+\frac{1}{l}+\frac{1}{m}+\frac{\varepsilon}{mn}\right)\right]+\frac{1}{\alpha^2}+n\varepsilon+\varepsilon^2} \quad \text{......(41)}$$

where $\varepsilon=\frac{3}{2}-\frac{1}{\alpha}+\frac{1}{\beta}$ and is usually made equal to zero.

2.6.1. Sensitivity

The sensitivities of Q_0 and ω_Q to variations in m, n, l, α and β, with ε zero, are given in Tables 1 and 2 respectively.

The ideal Q-factor is given by

$$Q_0=\frac{\sqrt{m(m+1)}}{\frac{mn\alpha}{\sqrt{l}}+\frac{\sqrt{l}}{n\alpha}} \quad \text{......(42)}$$

The value of Q_0 has a maximum when

$$mn\alpha^2=l \quad \text{......(43)}$$

and its value is

$$Q_0=\frac{\sqrt{m+1}}{2} \quad \text{......(44)}$$

For high Q-factors

$$Q_0\simeq\frac{\sqrt{m}}{2}=\frac{\sqrt{l}}{2n\alpha} \quad \text{......(45)}$$

Using eqns. (43) and (45), and assuming ε is not equal to zero, the approximate expressions for sensitivities of Q_0 and ω_Q are given in Tables 1 and 2 respectively.

2.6.2. Effects of finite amplifier gain and phase shift in the amplifier

By replacing A_1, A_2, A_3 and A_4 in the admittance matrix (40), by $A/(1+p\tau)$ and neglecting terms of greater order than $1/A$ the following Y-matrix is

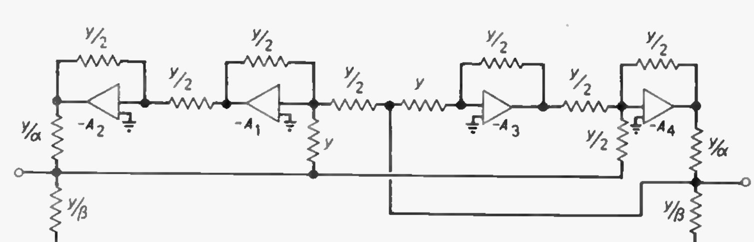


Fig. 8. Circuit of a gyrator (after Morse and Huelsman[6]).

produced:

$$\begin{vmatrix} \frac{y}{A}\left[\frac{12}{\alpha}-2{\cdot}5+\left(\frac{12}{\alpha}-2{\cdot}5\right)p\tau\right] & -y\left[\frac{1}{\alpha}-\frac{7}{\alpha A}(1+p\tau)\right] \\ y\left[\frac{1}{\alpha}-\frac{1}{A}\left(\frac{3}{\alpha}+1+\frac{3p\tau}{\alpha}+p\tau\right)\right] & \frac{y}{A}\left[\frac{12}{\alpha}-2{\cdot}5+\left(\frac{12}{\alpha}-2{\cdot}5\right)p\tau\right] \end{vmatrix} \quad \ldots\ldots(46)$$

For small values of α, this is of the form

$$\begin{vmatrix} \frac{12y}{\alpha A}(1+p\tau) & -\frac{y}{\alpha}+\frac{7y}{\alpha A}(1+p\tau) \\ \frac{y}{\alpha}-\frac{3y}{\alpha A}(1+p\tau) & \frac{12y}{\alpha A}(1+p\tau) \end{vmatrix} \quad \ldots(47)$$

From matrix (47) the value of predicted Q-factor may be found and is given in Table 3.

Considering the transfer voltage ratio in the more general form, eqn. (41), the actual Q-factor obtained is

$$Q_\varepsilon = \frac{Q_0\sqrt{1+\dfrac{\varepsilon}{n(m+1)}}\sqrt{1+\alpha^2\varepsilon(n+\varepsilon)}}{1+Q_0\alpha\sqrt{l\varepsilon}\left(1+\dfrac{1}{l}+\dfrac{1}{m}+\dfrac{\varepsilon}{mn}\right)} \quad \ldots(48)$$

In experimental work, there are several ways of obtaining different Q-factors for one particular frequency. Considering varying the resistance ratio m, the Q-factor is approximately given by

$$Q_\varepsilon \simeq \frac{Q_0}{1+Q_0\dfrac{12}{A}\left(\sqrt{l}+\dfrac{1}{\sqrt{l}}\right)} \quad \ldots\ldots(49)$$

Alternatively, variation in capacitor ratio l, produces the following Q-factor

$$Q_\varepsilon \simeq \frac{Q_0}{1+\dfrac{\varepsilon}{2n}+Q_0^2 2\alpha^2 n\varepsilon} \quad \ldots\ldots(50)$$

The interesting point to note is that in this circuit these curves, (49) and (50), are considerably different and intersect at a value of Q_0 given by

$$Q_0' = \frac{1}{4\alpha n}\left[\left(\sqrt{l}+\frac{1}{\sqrt{l}}\right)\pm\sqrt{l\left(1+\frac{1}{l}\right)^2-4}\right] \quad \ldots(51)$$

It will be noticed that eqn. (50) exhibits a maximum and its value is given by:

$$Q_{\varepsilon_{\max}} \simeq \frac{1}{2\sqrt{\alpha n}}\sqrt{\frac{A}{24}} \quad \ldots\ldots(52)$$

This illustrates the limitations upon the value of Q attainable as a result of finite gain in the amplifier.

3. Conclusions and Remarks

For any particular problem in hand, the designer must, from a large selection of possible circuits, be able to pick the circuit best suited to his needs. He will therefore consider such properties as stability, reliability, sensitivity, and other non-ideal effects which certain circuits exhibit. From these considerations some sort of design criterion must be formulated in order to show which properties take priority.

Six simple circuits have been presented and some comparison is made, by means of tables, concerning the aspect of sensitivity and its relationship to Q-factor. An expression for total sensitivity to Q may be defined in the following way:

$$S_T^Q = \sum_{q=1}^{n} |S_q^Q|$$

where n is the number of active and passive elements in the circuit. The general qualitative result which is reached, is that circuits (2) and (5), using purely negative feedback are the least sensitive. More specific comparisons cannot be made unless particular component values are allocated. However, it will be seen that, although the sensitivity of circuit (2) is low, the effect of phase shift and finite gain of the active element limits the applications of the circuit. In the case of circuit (5) there is the additional advantage that the Q-factor and centre frequency location can be selected independently by, for example, changing e and C respectively.

The effect of finite gain and phase shift in the amplifier on the Q-factor obtained is most marked in the case in which a single active element is employed. For example, circuit (5) which has gain distributed throughout the network is able to realize considerably higher Q-factors than either circuit (1) or (2). It may therefore be thought that the gyrator filter, circuit (6) should be capable of yielding even higher Q-factors. However, the results given in eqns. (49) and (50) prove to the contrary. A further disadvantage of this gyrator filter is the large number of components necessary and tolerance effects on the gyration resistance. It can also be shown that phase shift in the amplifiers introduces an uncontrollable amount of Q-enhancement due to the $10\tau\omega_0/A$ term in the expression for Q_τ.

The Q-factor depends only upon the ratio of component values of the circuit whereas the frequency of location of the 'peak' of the magnitude response which is given by eqn. (6) depends upon the Q-factor and the absolute value of the time-constant T. Consequently the accuracy of obtaining a certain Q and then locating the response (in frequency) is different. This may be of importance in thin film or integrated circuit application of active filters.

For many applications, circuit (5) or the gyrator are likely to be the most satisfactory, particularly when high Q responses are required. However, when selecting a circuit it must be borne in mind that if many filters are to be employed the power dissipation in the amplifiers must not be excessive. One possible way of overcoming this problem is to approximate the required response by cascading two stages of the type shown in Fig. 3. Use of only two amplifiers instead of three reduces the power dissipation. Obviously, the cost of the filter is also reduced.

The analysis above does not take account of amplifier input and output impedances. High input impedance can be obtained by the use of m.o.s. transistors in the amplifier input stage while emitter-follower output will give low output impedance. Stray capacitance effects are also ignored in the analysis. Stray capacitance can lead to instability if suitable compensation procedures are not adopted.

The effect of phase shifts in this and other gyrator circuits may be compensated to extend the frequency range before the Q becomes infinite. However, it can be shown that in order to avoid instability it may be necessary to make this phase compensation exceedingly accurate. It may be difficult to maintain the compensation against variations of supply voltage and temperature for a wide range of frequencies.

4. Acknowledgments

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Forthcoming Conferences

Organization and Management of R. & D.

The External and Professional Matters Sub-Committee of the Institute of Physics and The Physical Society is arranging a Conference on 'The Organization and Management of Research and Development' to be held at the Institution of Electrical Engineers, Savoy Place, London, W.C.2, on Monday, 5th May 1969.

There are many problems in the organization and management of research and development, not the least of which is that many young scientists find themselves having to assume positions of managerial responsibility without having received adequate training. Current annual expenditure on R. & D. in the United Kingdom is about £1000M. The Conference is intended to give guidance on the techniques of research organization and management and their use, and on sources of further information and training in these techniques. It should, therefore, be of interest to all concerned now, or likely to be concerned in the future, with the management of research and development, whether as group leaders, project leaders or research managers and directors. After the conference an assessment will be made of the desirability of further meetings on other aspects of the organization of scientific research and development.

Members of the I.E.R.E. may register to take part in this Conference at the same rate as members of the Institute of Physics and the Physical Society.

Further information about the Conference may be obtained from the Meetings Officer, Institute of Physics and The Physical Society, 47 Belgrave Square, London, S.W.1.

Solid-State Devices

The Institute of Physics and The Physical Society, in collaboration with the I.E.E., the I.E.R.E. and the I.E.E.E. (United Kingdom and Republic of Ireland Section), is arranging a third conference on 'Solid State Devices', to be held at the University of Exeter from 16th to 19th September 1969. The conference will follow the same general pattern as previously and the object will again be to provide a forum for the presentation of applied research in the physics and characterization of solid-state devices and associated technologies.

Keynote papers will be given, but contributions on the following subjects are invited:

New devices needed (also new device concepts, device physics, device modelling, device characterization); large scale integration—two approaches; semiconducting ferromagnetics; semiconducting ferro-electrics; physics of Schottky barriers; physics of silicon–silicon dioxide interface; novel circuit elements used in s.i.c. design; semiconductor detectors of visible and i.r. radiation; modern microwave techniques; reliability physics; and silicon technology.

Contributions should be of about 15 minutes' presentation time and intending authors should submit two copies of abstracts (about 350–400 words), to Dr. P. C. Newman, Allen Clark Research Centre, Caswell, Towcester, Northamptonshire. The final date for consideration of contributions will be 27th June 1969, but late-news papers may be accepted up to 29th August 1969.

It is also hoped to organize, during the Conference, information discussion seminars on 'High power devices' and 'Alternative high frequency active devices'.

Further information may be obtained on application to the Meetings Officer, Institute of Physics and The Physical Society, 47 Belgrave Square, London, S.W.1.

I.F.A.C. 1970

At the invitation of the Association Française de Cybernetique Economique et Technique and the Conseil d'Administration des Journées d'Electronique de Toulouse, the third Symposium on Automatic Control in Space will be held in Toulouse, France, from 2nd to 6th March 1970. The following topics for contributed papers have been proposed:

Space vehicle systems; Trajectory control, including problems of rendezvous; Components of space systems and space digital computers; Environmental systems; Underwater and underground systems; Space navigation; Biological aspects and control of human biological functions; Man-machine problems in space; Automatic steering of vehicles on the surface of the planets.

Abstracts of papers should be submitted to Professor J. Lagasse, Laboratoire d'Automatique et de ses Applications Spatiales du CNRS, B.P. 4036, 31 Toulouse 04. Full text of accepted papers will be required before 1st September 1969.

Further information and details regarding the Symposium Programme will be announced in the *Journal* as soon as they become known.

Education and Training Technology International Convention

The Educational and Training Technology International Convention (ETTIC 69) planned for the 2nd to 6th September 1969 at Grosvenor House, London, has been postponed.