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"To promote the advancement of radio. electronics and kindred subjects by the exchange of information in these branches of engineering."

THE RADIO AND ELECTRONIC ENGINEER

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The National Electronics Council

THE announcement made in the House of Commons on 24th January of this year by the Minister of Technology (see page 82 of this *Journal*) regarding the wider function of the National Electronics Research Council, is of interest to all members, especially in those Commonwealth countries which have established links with N.E.R.C.

By the terms of the Royal Charter granted to the Institution in 1961, it was declared that the object and purpose for which the Institution is constituted is to promote the general advancement of radio science and engineering including . . . 'the theory, science, and practice of electronics and all kindred subjects and their applications'. One method of fulfilling this particular object was to support the National Electronics Research Council in its purpose of bringing closer together the three main groups concerned with research in electronics: namely, government, industry, and the universities.

The formation of such a Council was recommended in 1961 by the Institution's Charter President, Admiral of the Fleet the Earl Mountbatten of Burma, in a speech to the radio and electronics industry. At his request, the Institution's Research Committee compiled and published a report on 'Radio and Electronics Research in Great Britain'.† Lord Mountbatten was then invited to become the Chairman of the National Electronics Research Council, which was subsequently incorporated under the Companies Act in July 1964, comprising representatives of government departments, the electronics industry, universities, and the learned and professional bodies.

Within the last two years N.E.R.C. has completed a preliminary design study demonstrating the feasibility of a British system for the selective dissemination of information to scientists and engineers concerned with electronics. In this project emphasis has been laid on the need to give scientists and research workers an immediate service of current awareness designed to help to avoid unnecessary duplication of research and indicate preferable fields of British endeavour. The original features of this system have been acknowledged by experts in the U.S.A. and Russia. The work has now been transferred to the Institution of Electrical Engineers‡ and it will provide a valuable complementary function to the computer-aided information retrieval system operated in conjunction with *Science Abstracts*. The whole of this work is under the sponsorship of the Department of Education and Science through its office for Scientific and Technical Information.

The National Electronics Council—successor to N.E.R.C.—will be under the aegis of the Ministry of Technology but will retain its legal status as an incorporated body. The Council will advise the Government on matters affecting the application of electronics to the national life. Association will continue with such organizations as the White Fish Authority in jointly examining the application of electronics to the fishing industry, and the Medical Research Council in the application of electronics in the medical field. The continuation of Commonwealth links is especially welcomed.

The role of the Institution in supporting and encouraging N.E.R.C.—both actively through members taking part, as they have in many capacities, in its work, and through financial contributions—has been well justified: the new N.E.C. has a sound foundation for working towards the stated aim of the old N.E.R.C., of improving the national economy by promoting applications of electronic devices and the application of new electronic ideas to industry generally.

F. W. S.

† *Proc. Brit.I.R.E.*, **1**, No. 5, pp. 113–141, July–August 1963.

‡ 'Britain's S.D.I. Project', *The Radio and Electronic Engineer*, **32**, No. 6, p. 329, December 1966.

INSTITUTION NOTICES

President to Visit India

The President of the Institution, Professor Emrys Williams, has accepted an invitation from the Indian Divisional Council to visit India at the beginning of March this year. He will travel to the main centres of Institution activity—Delhi, Bombay, Calcutta, Madras and Bangalore—and address meetings of members and give a number of lectures at universities and other establishments. Professor Williams will be accompanied by the Secretary of the Institution, Mr. Graham D. Clifford. They will visit the Institution's Section in Israel before returning to England.

Proceedings of I.E.R.E. Symposia

The following sets of reprints of papers, presented at Radar and Navigational Aids Group Symposia, held in London and recently published in *The Radio and Electronic Engineer*, are now available.

'I.L.S. Ground Equipment for Automatic Landing': Six papers and associated Discussion. *Price 21s.*

'Reliability of Marine Radar Equipment.' Four papers and associated Discussion. *Price 15s.*

Orders, together with remittance, should be sent to the I.E.R.E., 8–9 Bedford Square, London, W.C.1.

Information on Institution Conferences

Further information and registration forms relating to the Conferences on 'The Integration of Design and Production in the Electronics Industry', and 'R.F. Measurements and Standards', may be requested, using the application forms on page xvi of this issue. Attention is drawn to the fact that offers of papers for the latter Conference are invited.

World Congress of Engineers and Architects in Israel

The Association of Engineers and Architects, Israel (A.E.A.I.) is holding a Congress on the theme 'The Technological and Engineering Challenge of Israel's Development' between June 20th and 27th, 1967. Based on Tel-Aviv, but including a three-day tour of Israel, the Congress participants will divide into Discussion Groups. These will include 'Industrial Development' and 'Space Research Technology'.

Further information on the programme, registration and travel arrangements may be obtained from A.E.A.I., P.O. Box 3082, Tel-Aviv, Israel, or from the I.E.R.E., 8–9 Bedford Square, London, W.C.1.

New Role for National Electronics Research Council

In a written reply to a parliamentary question by Mr. H. D. Brown (Glasgow, Provan) on 24th January, the Minister of Technology, Mr. Anthony Wedgwood Benn, made the following statement:

'The National Electronics Research Council, an independent non-governmental organization, was set up in July 1964 under the chairmanship of Earl Mountbatten of Burma, in the belief that there was an urgent need to co-ordinate pure and applied research in electronics, and with the intention that it should indicate gaps in research, suggest priorities and prevent unnecessary duplication of effort.

'Since then, however, the Government has made new central arrangements for dealing with questions of science and technology. In particular the Ministry of Technology has become the sponsoring Department for the electronics industry. With the imminent transfer to it of the present functions of the Ministry of Aviation, its research stations with an interest in electronics will be further augmented by the inclusion of the Royal Radar Establishment and the Royal Aircraft Establishment. Responsibility for civil scientific policy and questions relating to basic scientific research lies with the Department of Education and Science and the Science Research Council.

'These developments have profoundly affected the role of the National Electronics Research Council. In future its research role will be continued under different arrangements. The Government has therefore proposed, with Lord Mountbatten's agreement, that the Council should accept a new and wider function under the aegis of the Ministry of Technology.

'The change would be reflected by an alteration in the title to the National Electronics Council (N.E.C.). The new Council would, in place of a more limited interest in research, assume responsibility that would embrace the impact of major developments in electronics on society. It will consider and advise the Government on the application of electronics to the national life. If it sees the need to promote research or encourage other specific action it will take the appropriate initiative either directly with the Ministry of Technology or through the various existing bodies operating in the electronics field. The new Council will continue to develop the valuable contacts which its predecessor had established with Commonwealth countries.

'There will be an appropriate widening of the membership of the governing body of the Council to reflect its new role. Also, as from the date at which this new arrangement takes effect, the Secretariat will be provided by the Ministry of Technology.

'I believe that the new Council has a very important job to do and am looking forward to working with it.'

U.D.C. 621.385.833:621.9

Design and Control of a High Precision Electron Beam Machine

By

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AND

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Summary: A two-lens electron beam machine is designed to give maximum power density in spot diameters ranging from 1·5 μm to 10 μm. The beam is deflected in a raster and modulated by a simple pattern generator. The design and performance of the electron optical system and the present control equipment are discussed together with a proposal for an on-line computer control system.

List of Symbols

Unless otherwise defined, the subscripts 'C' and 'O' and '1' and '2' will be used to refer quantities to the condenser and objective lens respectively.

C_s	spherical aberration coefficient (cm)
C_s^*	modified spherical aberration coefficient
D	average lens bore diameter. For asymmetrical lenses, D_1 and D_2 are used to distinguish the polepieces
D'	diameter of polepiece at the air-gap
D''	maximum diameter of polepiece
d	diameter of aberrated spot (cm)
f	focal length
k	Boltzmann's constant $= 8{\cdot}6 \times 10^{-5}$ eV/degK
l_1	electron gun to condenser lens distance
l_2	condenser lens to objective lens distance
l_3	objective lens to workpiece distance
M	electron optical magnification
M_x, M_y, n	registers
NI	lens excitation in ampere turns
R	average lens bore radius $= D/2$
r	radius of disk of confusion
r_x	radius of disk of confusion referred to the gun crossover
S	polepiece separation
T	absolute temperature
ΔT	temperature rise
t_B	thickness of lens bottom plate
t_s	thickness of lens shell
u, du	program co-ordinate variables
u'	object distance from lens
V	accelerating voltage (volts)
v, dv	program co-ordinate variables
v'	image distance from lens
v_{r1-6}	reference voltages
W	beam power density (W/cm^2)
x, dx, y, dy	registers
γ	beam semi-angle (radians)
ρ_c	cathode current density (A/cm^2)

1. Introduction

A focused electron beam provides a small intense heat source which appears well suited to the fabrication of miniature components.[1] The ease with which the beam can be deflected and modulated makes electron beam machining amenable to automation; however, a versatile machine and complex control equipment must be used to take full advantage of the process. This paper first describes the design and construction of a variable spot diameter machine and shows some initial machining using a novel pattern generator. Then, a proposed on-line computer control system to fully-automate the machine is discussed.

2. The Electron Beam Column

The electron beam column consists of an electron gun and magnetic lenses which focus the electrons from the gun into a spot on the workpiece as shown in Fig. 1. The spot size can be varied by changing the position and focal lengths of the lenses but the

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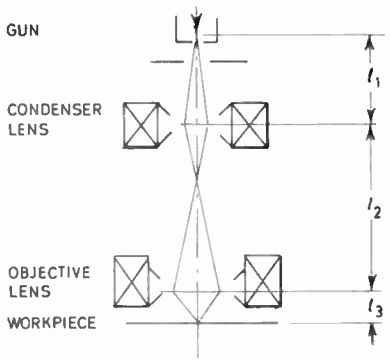
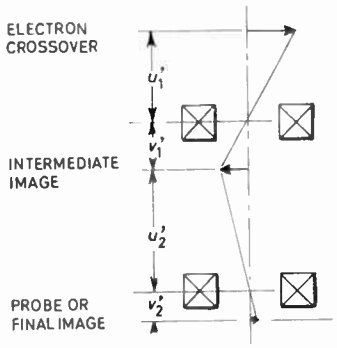


(a) Location of lenses.



(b) Location of images.

Fig. 1. The electron beam column.

power density will vary as well. The spot diameter chosen for each machining operation must therefore be a compromise between accuracy and power, and a versatile electron beam machine should provide a variable magnification. The range of spot sizes needed can be estimated by calculating the power and heating effect of different beams.

2.1. *Heating Effect of an Electron Beam*

The power density in a spot of given size is a function of the beam brightness and the spherical aberration of the optics. Einstein[2] has shown this power density to have a maximum value,

$$W = \frac{0{\cdot}34\,\rho_c V^2}{kT}\left(\frac{d}{C_s}\right)^{\frac{2}{3}} \qquad \text{.....(1)}$$

when an aperture is used to constrain the beam to an optimum semi-angle of convergence given by

$$\gamma_{opt} = \left(\frac{2}{3}\frac{d}{C_s}\right)^{\frac{1}{3}} \qquad \text{.....(2)}$$

where W = power density (watts/cm^2), ρ_c = cathode current density (A/cm^2), V = accelerating voltage, k = Boltzmann's constant, T = cathode temperature (°K), C_s = spherical aberration coefficient (cm), d = diameter of aberrated spot (cm) and γ = beam semi-angle (radians).

Using the correct aperture, the spot diameter is increased 50% due to spherical aberration. For smaller apertures, the beam current is reduced and for larger apertures, the current increase is offset by the increase in spot size due to spherical aberration.

Equation (1), which assumes that the gun delivers a current at theoretical brightness, is valid for small spots and currents. For larger spots, the total gun current reaches the spot and the power density in the spot is given by

$$W = \frac{\rho_c}{M^2} V \qquad \text{.....(3)}$$

where M = column magnification.

The localized heating of different materials by an electron beam allowing for penetration and backscatter has been studied by Vine and Einstein.[3] From their data, the temperature rise of the hottest point in targets of copper and iron has been calculated and the results for different spot diameters are shown in

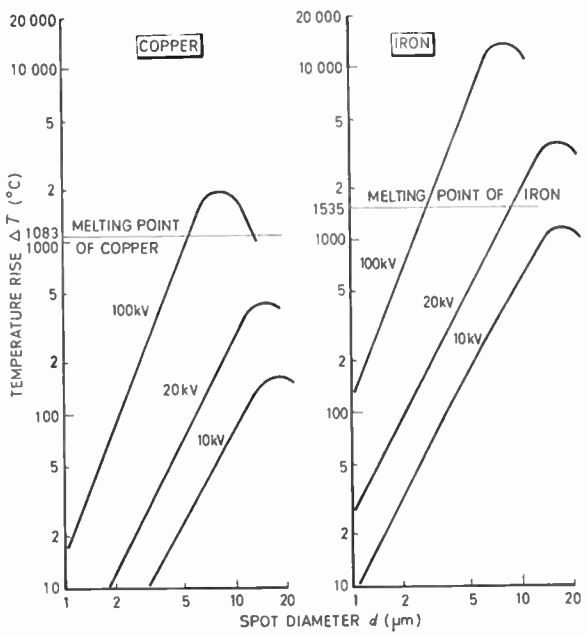


Fig. 2. Theoretical heating of copper and iron targets by the electron beam, C_s = 3 cm, ρ_c = 2A/cm^2.

Fig. 2. Typical values of ρ_c = 2 A/cm^2 and C_s = 3 cm were assumed and the maximum current from the 0·005 in diameter hairpin filament in the gun was taken as 500 μA. The temperature rises sharply with increasing spot diameter until the gun current

limit is reached. For low voltages, maximum temperature is reached for spots about 15 μm diameter.

2.2. *Machine requirements*

It is now possible to state the voltage, magnification and physical size requirements needed for the electron-optical design of the column. High beam voltages are useful for their power but low voltages are also needed for thin film machining where excessive penetration is harmful. It was assumed for the design that the voltage would be variable between 10 kV and 100 kV. The spot diameter range was fixed at 2 μm to 15 μm. Figure 2 shows 15 μm to be the largest useful diameter and 2 μm appears to be the smallest useful spot for thermal machining of thin films.[1] Since the electron source at the gun varies from 30 μm to 60 μm,[2,4] the electron optics, allowing for the 50% spherical aberration increase, must provide variable magnification from 1/3 to 1/50, and for high power, spherical aberration must be kept at a minimum over this range. Finally, the column diameter is limited to 16·5 cm by the availability of high purity iron for the lens polepieces and the maximum column length is chosen as 50 cm to allow easy handling and assembly.

2.3. *Electron Optical Configuration*

The two-lens configuration of Fig. 1 was chosen as the most suitable. The magnification can be changed electrically by varying the lens currents and the spherical aberration remains approximately constant over the spot size range. A single-lens system could be used, moving the workpiece to change the spot size but the spherical aberration increases with spot size.[2] Since no design criterion could be found in the literature for the choice of the spacings l_1, l_2 and l_3 between the gun, lenses and workpiece, the effect of each on the column performance was considered.

2.3.1. Objective lens to workpiece spacing, l_3

The working distance l_3 has a strong effect on the spherical aberration. The focal length f of the lens is approximately equal to l_3, for small values of l_3, and the spherical aberration coefficient C_s is proportional to f (eqn. 6). Therefore l_3 should be made small but a lower limit is imposed by the thickness of the bottom polepiece t_B (Fig. 16b). As l_3 is decreased, the lens gap S decreases in proportion and since the ampere-turn excitation is kept high for low aberration (Appendix, Section 7.1), the flux density increases and tends to saturate the iron polepiece. For short working distances, the value of t_B required to keep the iron unsaturated is appreciable and the electron spot is focused inside the polepiece. Trial designs lead to $l_3 = 1{\cdot}5$ cm to give about 0·5 cm clearance between the polepiece and the workpiece.

2.3.2. Inter-lens spacing, l_2

The effect of l_2 on the column performance was evaluated by calculating the parameters of both lenses for seven values of $l_2 = 5, 15, 25, 35, 45, 75$ and ∞ cm. The gun distance l_1 was arbitrarily chosen as 25 cm and l_3 was kept at 1·5 cm. In each case, the intermediate image position was found graphically for $M = 1/3$ and $M = 1/50$. The lens dimensions, focal lengths and spherical aberration coefficients in each case were calculated as shown in Appendix, Section 7.1. The results are shown in Table 1. To allow comparison of the spherical aberration of both lenses, the modified coefficients C_s^* have been used and are both referred to the final spot (Appendix, Section 7.2). An increase in l_2 reduces the spherical aberration of the objective lens and lessens the effect of condenser-lens aberration on the final spot.

Table 1

Effect of objective to condenser-lens spacing l_2 on spherical aberration and condenser-lens size

l_2 cm	$M = \frac{1}{3}$		$M = \frac{1}{50}$		$(S + D)$ cm
	C_{so}^* cm	$M^4 C_{si}^*$ cm	C_{si}^* cm	$M^4 C_{sc}^*$ cm	
5	32	460	10	210 × 10^{-4}	3·9
15	5·1	31	3·1	15 × 10^{-4}	11
25	3·3	9·0	2·6	4·2 × 10^{-4}	16
35	2·5	4·4	2·4	2·0 × 10^{-4}	21
45	2·1	2·8	2·0	1·1 × 10^{-4}	25
75	1·8	1·6	1·7	0·42 × 10^{-4}	35
∞	1·2	0·25	1·2	0·03 × 10^{-4}	81

where M = column magnification

$C_{so}^*, M^4 C_{sc}^*$ = modified spherical aberration coefficients referred to final spot for objective and condenser lenses.

S = condenser-lens gap

D = condenser-lens bore

$l_1 = 25$ cm

$l_3 = 1{\cdot}5$ cm

However, the condenser lens turns out to be quite large. An estimate of its size can be made from $(S+D)$, where S = lens polepiece gap and D = bore diameter (Fig. 16). Roughly, $(S+D)$ is the minimum diameter of the lens polepiece (eqn. 6) and should be about half the lens diameter or at most 10 cm for this design. Table 1 shows that $(S+D)$ increases with l_2 and that for $l_2 = 25$ cm, $(S+D) = 16$ cm or almost the full lens diameter.

There are two possible ways to reduce this lens size:

(*a*) by reducing the excitation and $(S+D)$, keeping the focal length constant;

(*b*) by reducing the gun to condenser-lens distance, l_1, and hence the required focal length.

Reducing the excitation would increase the spherical aberration and since the aberration is already large, a smaller value of l_1 must be used instead.

2.3.3. Gun to condenser-lens spacing, l_1

To determine the effect of l_1, the properties of several lens combinations were calculated for values of l_1 between 0·75 cm and 45 cm and l_2 between 5 cm and 75 cm. Three factors were selected as indices of performance of each configuration:

(i) maximum value of objective-lens spherical aberration C_{so}^*;

(ii) dominance of objective or condenser-lens spherical aberration;

(iii) condenser-lens size represented by $(S+D)$.

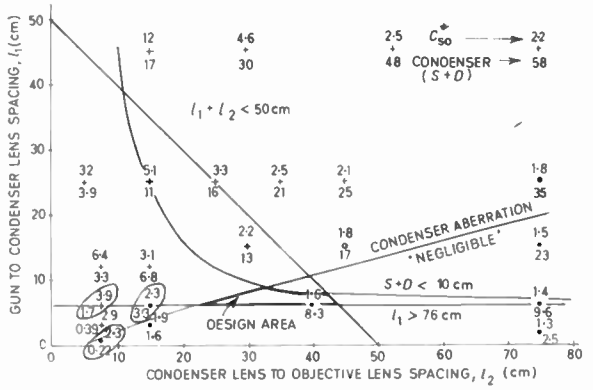


Fig. 3. Design graph for lens spacings: + condenser-lens aberration is dominant; ○ objective-lens aberration is dominant; ● condenser-lens aberration is negligible.

The results are set out on a design graph (Fig. 3) with l_1 and l_2 as the variables. For each configuration, a point has been put down with the value of C_{so}^* above it and $(S+D)$ below it. The symbol at the point shows which lens aberration is dominant and whether the condenser-lens aberration can be neglected, arbitrarily $M^4 C_{sc}^* < \frac{1}{2} C_{so}^*$ (Appendix, Section 7.2). This graph shows that a decrease in l_1 is beneficial to all factors: C_{so}^* and $(S+D)$ decrease and the condenser-lens aberration becomes negligible. The size of l_1, however, is limited to 6 cm by the dimensions of the electron gun.

2.3.4. Selection of spacings

Contour lines have been drawn on Fig. 3 to enforce design requirements and the following spacings were chosen:

$$l_1 = 6\text{ cm}, \quad l_2 = 40\text{ cm}, \quad l_3 = 1{\cdot}5\text{ cm},$$

for which the condenser $(S+D) = 8{\cdot}3$ cm and $C_{so}^* = 1{\cdot}6$ cm. The total length requirement $l_1 + l_2 \leq 50$ cm is the most arbitrary, but doubling the length would increase the condenser-lens size and only reduce C_{so}^* by 13%

It appears that the best performance for the column is achieved by making l_1 and l_3 as small as possible and increasing l_2 until the condenser-lens size becomes important.

2.4. *Lens Design*

The design of the lenses follows an established procedure which is summarized in Appendix, Section 7.1. The objective lens must have a long working distance with a small magnetic field at the workpiece. The diameter of the upper bore must be large enough to accommodate deflection coils. Trial designs lead to $S/D = 0{\cdot}5$ and $D_1/D_2 = 2$ and the excitation must be reduced with some increase in spherical aberration to give sufficient working distance. The condenser lens has no special requirements and is made symmetrical with $S = D_1 = D_2$.

The lens data are as follows:

Objective lens

$D_1 = 2{\cdot}54$ cm

$D_2 = 1{\cdot}27$ cm

$S = 0{\cdot}952$ cm

$V/(NI)^2 = 0{\cdot}015$ minimum

$C_s^* = 2{\cdot}99$ cm for $M = 1/50$

$C_s^* = 3{\cdot}28$ cm for $M = 1/3$

$f_{min} = 1{\cdot}05$ cm

Condenser lens

$D_1 = D_2 = S = 2{\cdot}03$ cm

$f_{min} = 1{\cdot}2$ cm.

2.5. *Constructional Details*

A section drawing of the column is shown in Fig. 4. The gun (1), taken from an EM-6 microscope, has a conventional triode structure capable of operation up to 100 kV. Though the whole machine has been designed for 100 kV, at present only a 50 kV generator with stabilized heater and grid supplies has been used. Beam tilt due to filament misalignment can be corrected by de-centering the anode (2) slightly with X and Y pushrods. Though Fig. 4 shows the gun solidly bolted to the condenser lens (3), it is now free to slide so that the beam and condenser-lens axes can be centralized. There is also an alignment stage (5) between the condenser lens and objective lens (6). These three adjustments allow exact alignment of all parts of the column (Ref. 4, p. 189).

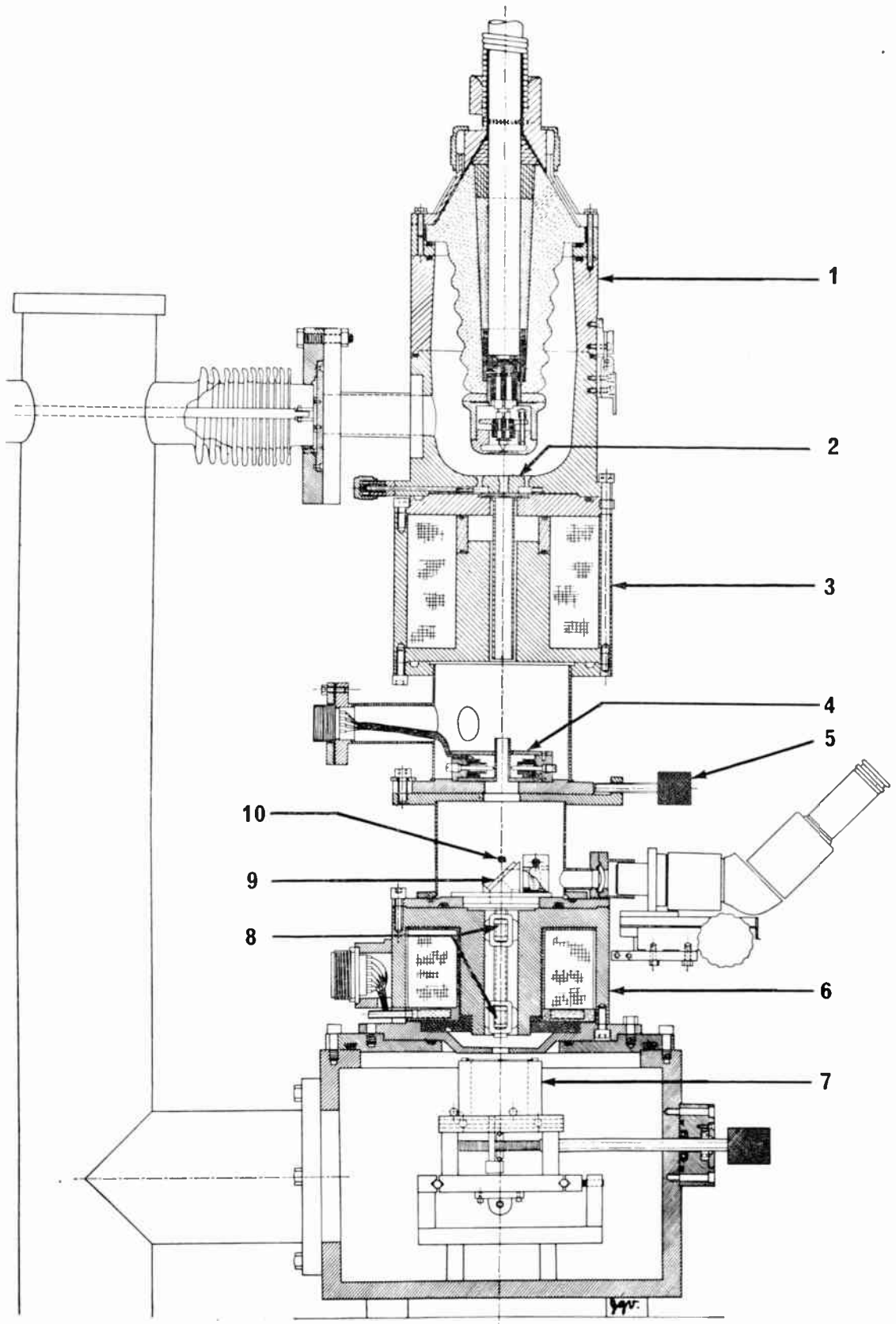


Fig. 4. Cross-section of the electron beam machine.

To reduce astigmatism arising from asymmetry, the lenses are made from vacuum-smelted low carbon steel, first rough machined to 1/32 in and then annealed before final machining.

Double deflection coils (8) to deflect the beam over a 1 mm square have been placed in the bore of the objective lens. Mechanical movement of the workpiece (7) extends the machining area to a 2-inch square. A 45° mirror (9) concentric with the beam allows top-side viewing of the workpiece through the centre of the coils. An aperture holder (10) above the mirror enables five different apertures to be selected. Further up the column, a magnetic octopole astigmatic corrector (4) is used to correct a small amount of astigmatism visible in the spot.

A 4-in diffusion pump is used with Apiezon B oil to reduce build-up of insulating films. Welded stainless steel construction has been used for all parts of the vacuum system except the lenses. Lead shielding around the aperture stage was found necessary to reduce radiation at 50 kV below the background level.

2.6. *Measurement of Spot Size and Power*

The beam is deflected across a horizontal knife edge above a Faraday cage and the current waveform is displayed on an oscilloscope. This signal is also taken through a differentiator to give a spot profile. The width at half-height is taken as the spot size.

The spot size is mainly dependent on the condenser-lens excitation. The objective-lens current to keep the spot in focus varies only slightly but must be capable of adjustment and be stable to 1 part in 10^4.

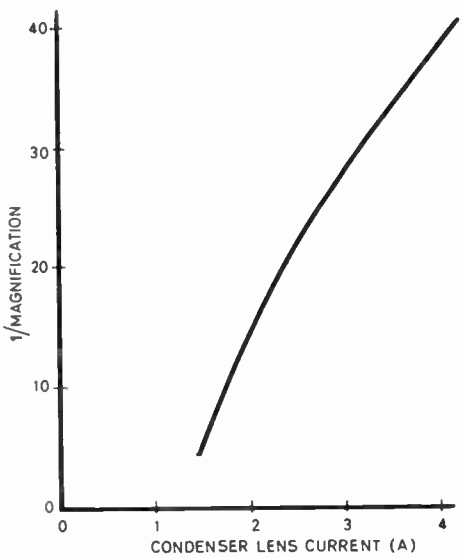


Fig. 5. Variation of column magnification with condenser-lens current. (Lens coil is tapped to give 335, 473 and 749 turns at 10 kV, 20 kV and 50 kV respectively.)

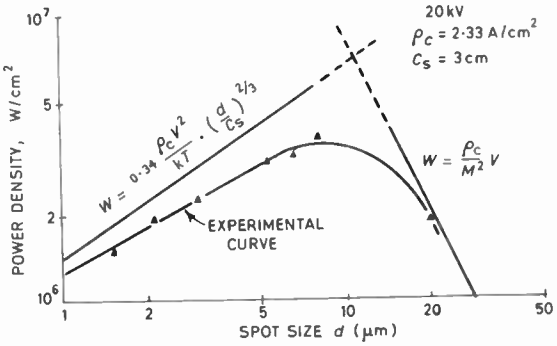


Fig. 6. Spot power density.

Beam currents and spot sizes were measured at 20 kV for various condenser-lens currents and beam apertures. The column magnification as a function of condenser-lens current is shown in Fig. 5. The variation of power density with spot size is compared to the theoretical curves in Fig. 6. The value of ρ_c used in calculating the theoretical power density was estimated by measuring the beam brightness at its peak value. At peak brightness, the filament current was 330 μA and the source diameter was 87 μm. For lower currents the source diameter is reduced to 48 μm.

The agreement is as good as can be expected from the simple theory. The power density for large spots is limited by the gun current. Spots as small as 0·5 μm have been obtained by using low currents and small apertures but maximum power density cannot then be expected.

2.7. *Conclusions*

A two-lens electron beam machine can be designed to give low, constant spherical aberration over a range of spot sizes. The condenser and objective lenses should be placed close to the gun and workpiece respectively and the inter-lens distance increased until the condenser lens size becomes important. For large spots, the gun current limits the beam power.

On this basis, an electron beam machine has been designed which approaches the maximum theoretical power density over the range of spot sizes from 1·5 μm to 10 μm.

3. Control Equipment

There are many parameters in the electron beam system which must be controlled, but in the absence of a computing machine, only a few can be controlled automatically. For the machining of simple straight-

lined patterns, some parameters can be manually pre-set while a digitized pattern generator is used to deflect the beam in x and y directions automatically, and pulse the beam 'on' over selected areas.

3.1. *The Digitized Pattern Generator*[5]

The pattern generator provides:

(i) the signals for deflecting the beam in a raster-form, the raster containing up to 1024 lines, and

(ii) the bright-up signal to turn the beam on and off as required to cut the pattern.

3.1.1. Pattern formation

Figure 7 shows how a pattern is formed. The pattern area is divided into 5 separate horizontal bars (Fig. 7(a)) and on each of these horizontal bars up to 2 bright-up segments may be placed (Fig. 7(b)). These segments are variable in position and length along the horizontal bar, and constitute the pattern. The upper and lower limits of each bar are variable over a small range so that the segments can be made to overlap (Fig. 7(c)). The bright-up signal can be inverted to make the negative of the pattern (Fig. 7(d)). More horizontal bars and segments can be added, but it is felt that the equipment is flexible enough not to warrant the increase in complexity of the electronics.

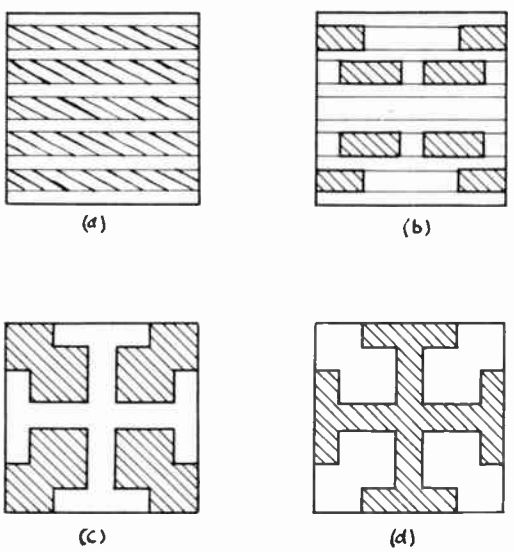


Fig. 7. Formation of the pattern.

A raster is scanned electronically over the pattern and the electron beam is turned on when the raster is scanning over a segment so that the workpiece is machined in that segment. A pattern made with a 64-line raster is shown in Fig. 8, as displayed on a monitor screen.

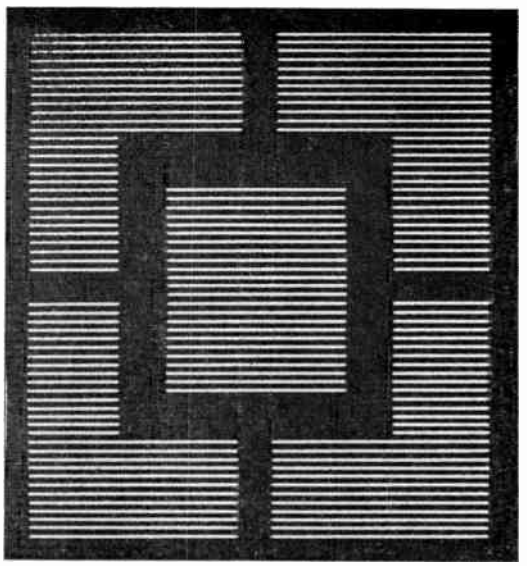


Fig. 8. Typical pattern as viewed on the monitor screen.

3.1.2. Raster generation

The raster is generated by a linear ramp in the x direction and a synchronized staircase waveform in the y direction. The master oscillator (Fig. 9) triggers a bootstrap sweep generator producing the x ramp deflection and also steps the binary counter by one count during the x ramp flyback. The required number of binary counter outputs are fed into the digital-to-analogue converter by a 10-pole switch, so that the number of steps on the y staircase waveform can be varied up to 1024 in powers of 2. The x ramp and y staircase waveforms are fed to the bright-up circuits, to a monitor oscilloscope and to the electron beam deflection coil amplifiers.

3.1.3. Bright-up logic

To produce the bright-up signal, the logic must decide first whether the raster is scanning within a horizontal bar, and then whether it is scanning a segment within that bar. The decision is made by the use of comparator amplifiers (Fig. 9), which compare the x and y sweep voltages with reference voltages (v_{r1-6}) set up by front panel controls. The comparator amplifiers give a positive output if the sweep voltage is greater than the reference voltage, so that, as positive logic is used, the waveform at A is positive only when the instantaneous y sweep voltage is between v_{r1} and v_{r2}. To eliminate spurious triggering the waveform at A is sampled during the x flyback time and held on a bistable circuit, the output being

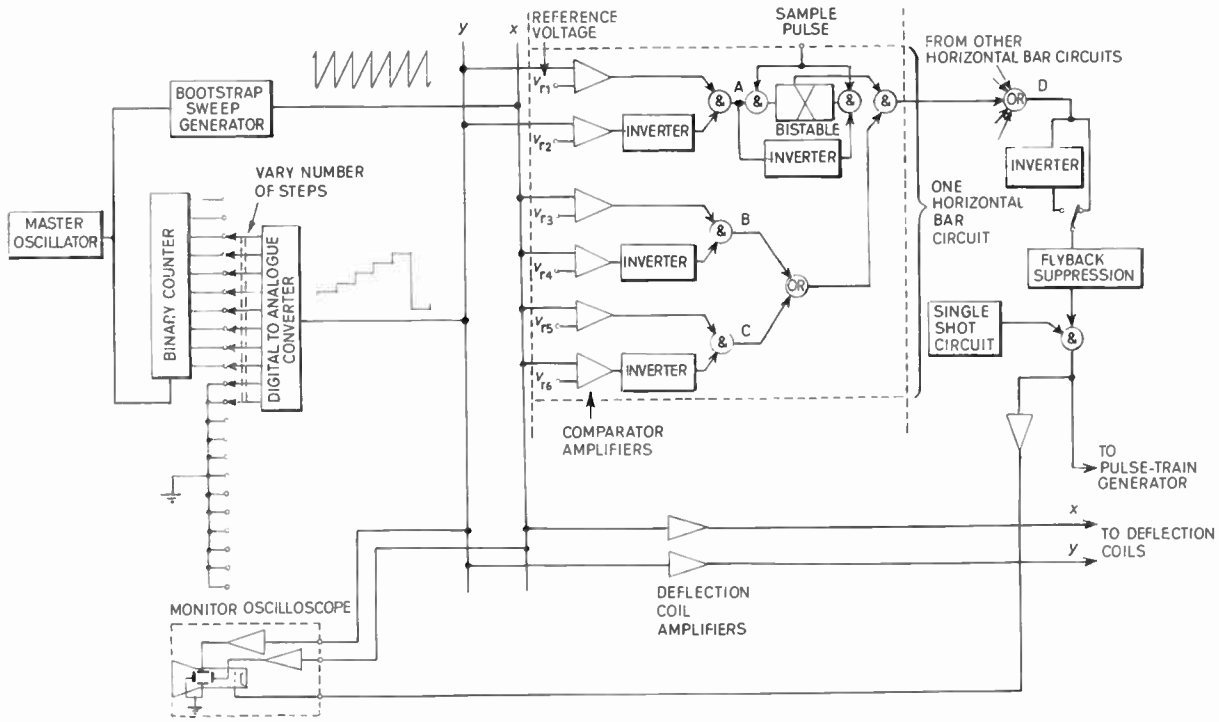


Fig. 9. Block diagram of the pattern generator.

positive during the time that the raster is scanning the appropriate horizontal bar. Similarly, the waveforms at B and C are positive only during the segment of x sweep when the instantaneous x sweep voltage is between v_{r3} and v_{r4}, and v_{r5} and v_{r6} respectively. If v_{r3} is greater than v_{r4} that particular segment will not be generated, so that all the segments available do not have to be used. After the subsequent logical gating, the bright-up signal is generated at D, whereafter it can be inverted if required (to make the negative of the pattern). The output waveform modulates the monitor oscilloscope to enable the pattern to be observed and adjusted before machining.

The stability of the pattern is mainly dependent upon the stability of the comparator amplifiers, and on a raster of 1024 lines they are stable to ± 1 line over a short time and ± 2 lines over 30 minutes, or $\frac{1}{3}\%$ to $\frac{1}{2}\%$ of the raster width.

3.2. *Beam Pulsing*

The cutting rate of an electron beam process is very dependent upon the temperature of the work-piece.[6] For the same average beam power, a higher spot temperature and lower temperature of the surrounding material is obtained if the beam is pulsed, so that the cutting rate is increased and the edge of the cut is sharper.

3.2.1. Pulse-train generator

The bright-up signal gates a pulse-train generator which generates a train of pulses of independently variable mark and space times. In anticipation of a computing machine both the time intervals are selected by 3 digital control lines so that timing varies in powers of two from 2 μs to 256 μs for the 'mark' time and from 4 μs to 512 μs for the 'space' time.

3.2.2. Pulsing equipment

A voltage swing of up to 300 volts with respect to the filament is needed on the electron-gun grid to turn the electron beam 'on' and 'off'. A current of

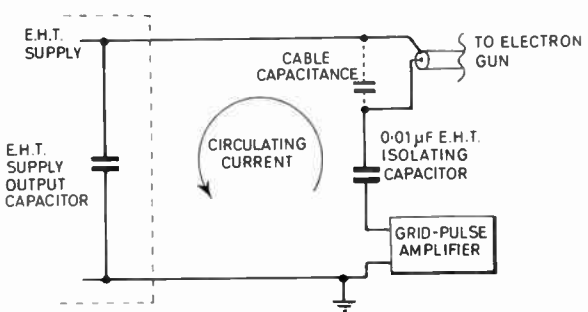


Fig. 10. Circulating current loop.

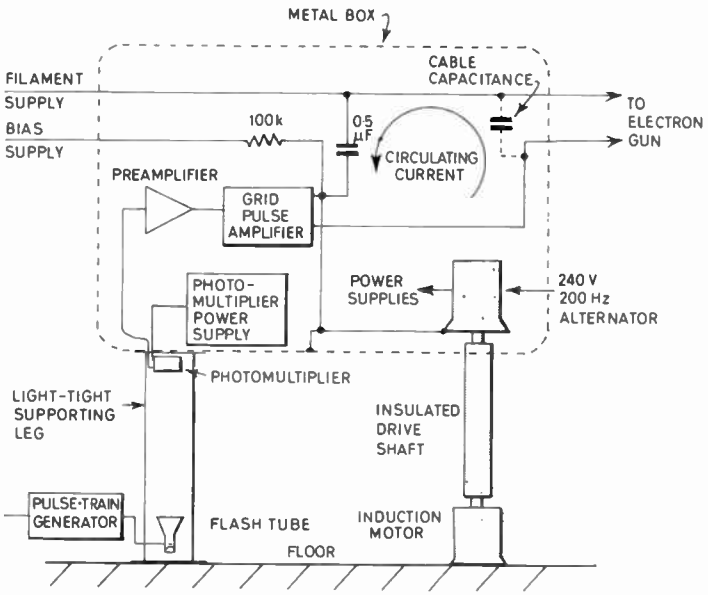


Fig. 11. Grid pulsing equipment.

about 1 A is needed to charge the filament-grid cable capacitance in 0·5 μs and if the grid pulse amplifier were at earth potential (Fig. 10), this high circulating current would pass through the e.h.t. supply (which can only supply 5 mA peak current). The e.h.t. supply output capacitor cannot be increased because if the electron-gun were to break down to earth, the high stored charge would damage the gun. This difficulty is overcome by mounting the grid pulse amplifier at e.h.t. potential in an insulated metal box (Fig. 11). One of the insulated supporting legs contains a flash-tube and photomultiplier to provide communication from the pattern generator at earth potential to the grid pulse amplifier at e.h.t. potential. A motor-alternator set with an insulated drive shaft is used to provide 2 kVA of power for the equipment in the box, and enables an oscilloscope to be mounted and used at the e.h.t. potential.

The pulse-train generator drives the flash-tube grid directly and the delay at the grid pulse amplifier is 380 ns on the rising edge and 220 ns on the falling edge. These delay times are mainly determined by the photomultiplier transit-time and grid pulse amplifier delay-time. The rise- and fall-times are mainly determined by the speed at which the circulating current can charge the cable capacitance, and for a 300 volt swing the rise and fall times are 500 ns.

3.3. *Conclusions*

Equipment to provide signals for the electron beam machining of simple patterns 1 mm square has been described. Two examples of some initial machining are shown (Fig. 12). One is a general pattern as might be used for interconnections and the other indicates how a meander resistor could be formed using two superimposed patterns.

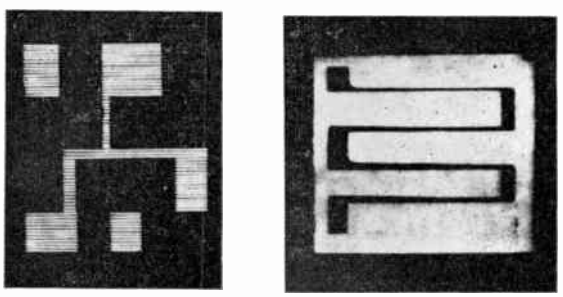


Fig. 12. Initial machining of 750 Å tantalum film on Pyrex glass. Patterns were machined in a 1 mm square by a 3 μm spot with 2 μA at 20 kV swept at 80 mm/s.

4. Computer Control

To obtain the flexibility required for machining thin films, a higher degree of control than given by the simple pattern generator is necessary. This section describes a proposal for automating the electron beam machine using a small on-line computer control system. The times estimated assume that an *Argus 400* is used.

4.1. *Electron Beam Parameters*

The control parameters of the proposed on-line computer control system are shown at the top of

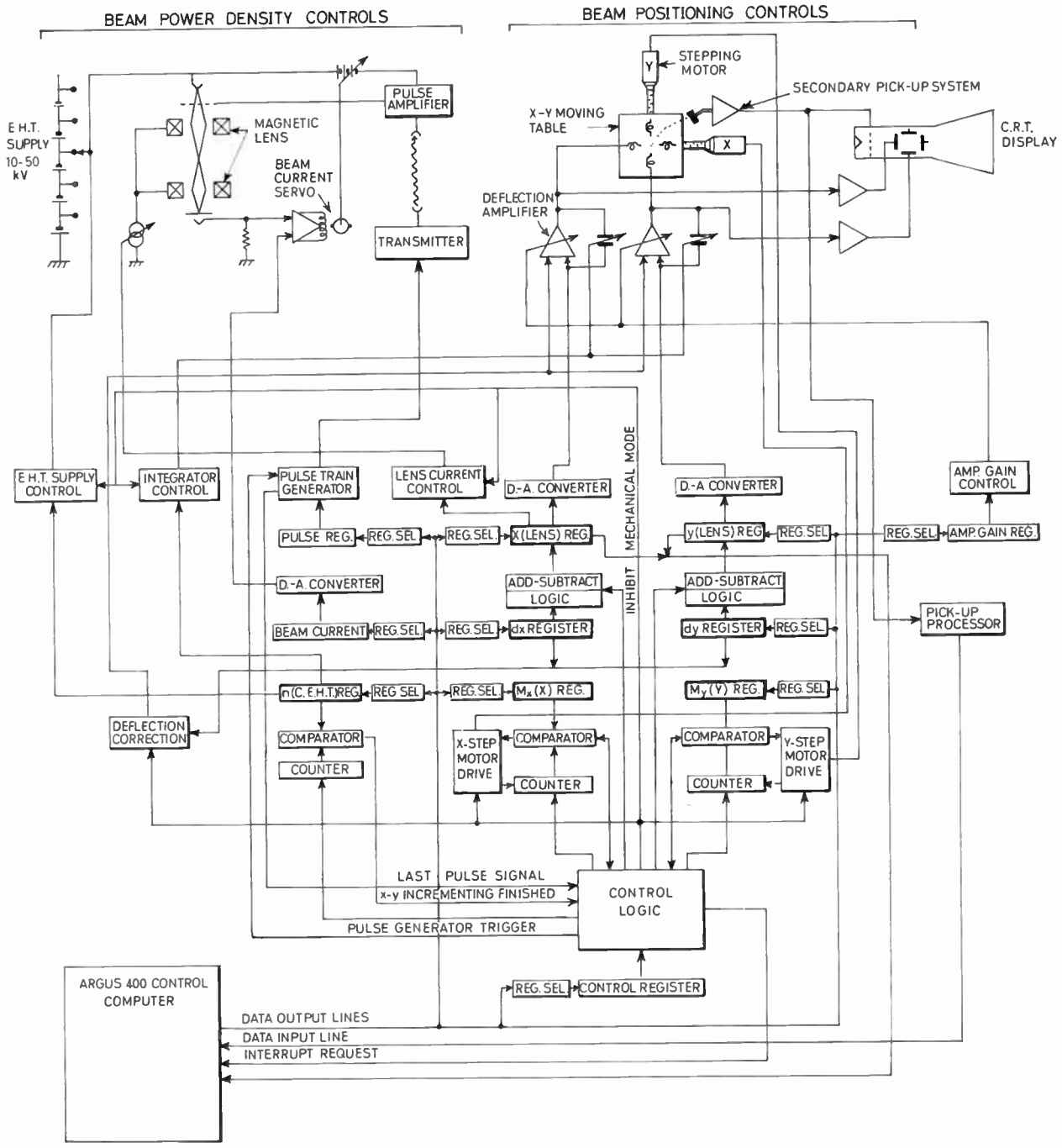


Fig. 13. Proposed control system for the electron beam machine.

Fig. 13. The parameters can be divided into two classes, those concerned with beam power density and those concerned with beam position. The e.h.t., lens currents, and grid bias control the beam power density. The pulse amplifier, isolated from earth by a light path, modulates the beam current as described in Section 3.2. The spot is positioned by deflection amplifiers which move it over a 1 mm square area. The amplifiers will be driven by 12-bit digital-to-analogue converters, making it possible to move in 0·25 μm steps. A moving table, driven by stepping motors under digital control, will permit the machining area to be extended over a 3 cm square. Scanning electron microscope facilities are added to monitor machining and to enable the workpiece to be re-located.

4.2. *Computer-Electron Beam Interface*

The complexity of the interface shown in Fig. 13 is largely due to the difference in speed between the computer and the deflection system. The deflection system can accept new information every microsecond, whereas the computer can provide new information approximately every 300 μs. To bridge the gap, it is necessary to have some automatic control external to the computer. With the interface logic shown, it is possible to machine in the x or y direction automatically, a line up to 1 mm in length or a rectangle up to 1 mm square, with all the information needed held in external registers. Since the computing time required to specify a line or a rectangle is approximately the same as that for a single point, a 1 mm line can be cut in 4 ms instead of 1·2 s, if every point were computed.

The x and y registers of Fig. 13 define the starting co-ordinate of the line or rectangle to be machined.† dx and dy determine the size of the increments in the x and y directions, while M_x and M_y hold the number of increments in each direction. Using the n register and the associated counters a complete rectangle can be defined.

4.3. *Non-linear Correction*

The same registers can also be used in another mode of operation, this is concerned with the non-linearities of the deflection system. If the distortion caused by the non-linearities is measured, this information can be stored in the computer and used to correct this distortion. The use of a highly accurate interpolation formula is impracticable because of the excessive time needed for computation. A simple linear interpolation formula is used which requires about 1·6 ms on the *Argus 400* to specify a complete line.

† The brackets in the registers of Fig. 13 indicate that the registers are also used in setting the control parameters shown in the brackets.

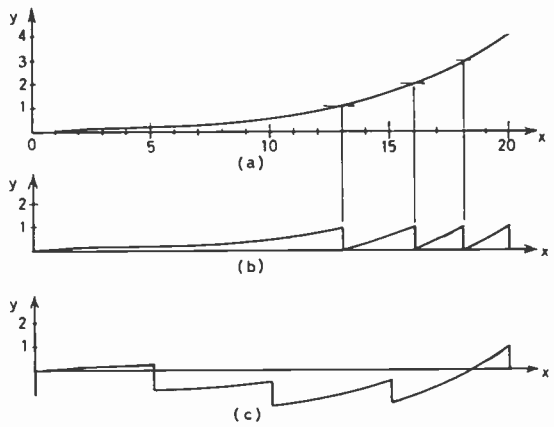


Fig. 14. Non-linear deflection correction.

Figure 14(a) illustrates the deflection distortion which may be present when moving from co-ordinates 0, 0 to 20, 0. The beam has moved four units in the y direction while moving 20 units in the x direction. The ideal method of compensating for this would be to deflect as in Fig. 14(b) where a move in the negative y direction is made whenever the error exceeds one unit. The time-consuming iterative interpolation procedure needed to find the x co-ordinate of the compensating y shift makes this procedure impracticable. An approximate method, which is faster to calculate and more amenable to automation, is shown in Fig. 14(c). Making the intervals between the y correction shifts equal allows the existing registers to cut a line automatically. The x and y registers hold the starting co-ordinates ($x = 0$, $y = 0$), dx and dy define the increments and the direction (d$x = +1$, d$y = -1$), M_x contains the number of dx steps before a change in the y co-ordinate ($M_x = 5$), n defines the number of times cutting alternates between x and y ($n = 4$).

4.4. *Re-positioning Error*

If the electron beam is to be useful in making integrated and thin film circuits, it is necessary to be able to re-locate the workpiece relative to its previous position. The rotational and translational errors introduced when re-positioning will be detected using the scanning electron microscope facilities. A co-ordinate system of fiducial marks, initially machined on the substrate, will be located with the electron microscope and their new position fed back to the computer. The computer could either compute the correction for each set of co-ordinates or set up an analogue device to compensate these errors. If the corrections are computed, machining would be difficult because the interface is not designed to machine automatically lines which lie at an angle to the co-ordinate system. Analogue compensation,

on the other hand, requires set-up time when the table is moved, but this is offset by the reduction in computing time and the more effective use of automatic machining.

4.5. *Simplified Pattern Description*

One disadvantage in using the computer to control the machining, is the difficulty in describing a pattern in machine language. A special pattern description language, similar to an autocode, was developed to make this task easier. Some features of this language are shown in Fig. 15.

Patterns are described by the end points of straight line segments defining the boundary, the necessary detail to cut inside will be calculated by the computer. The language was designed to minimize the redundant information in describing a pattern. The pattern of Fig. 15(a) which is symmetrical about the x and y axes, is described by listing the co-ordinates of a quarter of the boundary and stating that symmetry exists, e.g.

pattern 1
x and y symmetry
0, 0 0, 3 1, 3 1, 1 3, 1 3, 0

The instruction, 'x and y symmetry', completes the rest of the pattern automatically. If a pattern has repetitive detail, as in Fig. 15(b), it can be specified by a cycle repeat instruction which is designed to repeat the part of the pattern bounded by the instructions. The following program describes Fig. 15(b):

pattern 2
0, 0 3, 0
cycle 3
0, −1 −1, −1 −1, −2 0, −2
repeat
3, −7 0, −7

Using variable co-ordinates, the geometry of the pattern can be varied. The pattern routine describing Fig. 15(c) would be:

pattern 3
0, 0 1, 0 1, $-y_1$ 0, $-y_2$

Lines and rectangles are best described by standard routines which make it necessary to define only the width and path of a line or the dimensions of a rectangle. The rectangle of Fig. 15(d) is called by the instruction, 'rectangle (4, 6)'. The line of Fig. 15(e) is defined as follows:

line (2)
0, 0 3, 0 3, −2 6, −2

To machine an area as in Fig. 15(f), which is inside the rectangle and not inside the cross, the 'and not' instruction is used, e.g. rectangle (8, 8) and not pattern 1.

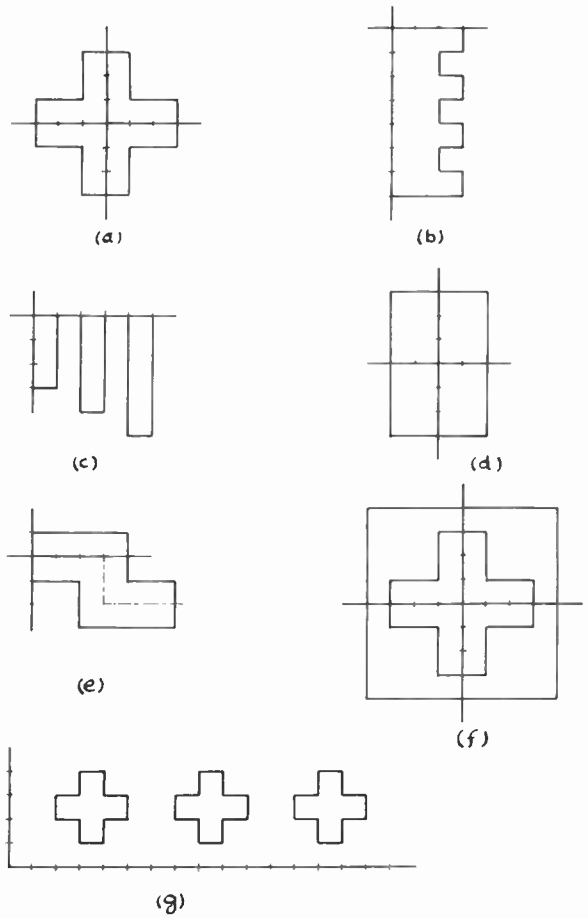


Fig. 15. Patterns described by computer language.

The cycle-repeat instructions, together with the co-ordinate parameters u, v, du, and dv make it convenient to specify arrays of patterns. The array in Fig. 15(g) would be described as follows:

$u = 7$
$v = 5$
cycle 3
pattern 1
du = 10
repeat

u and v set the initial co-ordinates so that when the pattern is called, the present value of u and v will be the (0, 0) co-ordinates of the pattern. du and dv are used to move the pattern incrementally in the u and v directions.

4.6. *Programming*

A program describing the machining in the simplified form described above will be read into the computer and compiled into a control program on

paper tape. This tape will be read into the computer when machining is to begin. The nature of the control program and the program which compiles it, is determined largely by speed considerations. Machining would be too slow, if the descriptive language were used to control it directly. On the other hand, a control program could be generated, which required the computer to act merely as a buffer and to direct data to the proper register. This program would be limited by the rate at which information can be read into the computer and the practical limit on the amount of information stored on paper tape. It is clear that control program which makes efficient use of the input control data, must be used.

The compiling program will edit the descriptive language providing address information, locating routines and variables. The boundaries of the patterns containing symmetry, repetitive detail, etc., will be completed and the co-ordinates of the path the electron beam will take inside the pattern will be calculated. The co-ordinates of the patterns will be left local to the routines. When machining, the computer will generate the absolute co-ordinates of the pattern in the millimetre square and if the non-linear correction is to be applied, the co-ordinates will then be modified. The calibration data will be held in store as 1000 24-bit words. Because of the automatic facilities of the interface, machining of the pattern and computing will take place simultaneously. When the interface requires new data, computing will be halted, using the interrupt channel of the computer, and new information, if available, will be transferred. When the instruction to move the table occurs, the computer and the scanning electron microscope facilities will be used to find the new fiducial marks and make adjustment as described in Section 4.4.

4.7. *Conclusions*

With a computer used as a general pattern generator and using the descriptive language described, the patterns can be easily specified and modified. On-line computer control would enable information about the position and condition of the workpiece to be fed back to the computer, thus increasing the machine's versatility and eliminating the need for a highly accurate moving table and measuring device. The system would be independent of any other computing installation and if the facilities of a large computer are needed, connection could be made using magnetic tape or paper tape.

5. Acknowledgment

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7. Appendix

7.1. *Magnetic Lens Design*

A typical lens is shown in Fig. 16. It consists of a coil set in soft iron polepieces to produce a strong well-defined magnetic field. The focal length and spherical aberration of such a lens are given by Liebmann's curves[7] drawn in Fig. 17 as a function of $V/(NI)^2$ and $(S+D)$, where V = beam voltage, NI = lens excitation, D = average polepiece diameter and S = polepiece separation. For large values of excitation NI, the focus moves into the lens field and the beam is focused after the focal point. For imaging

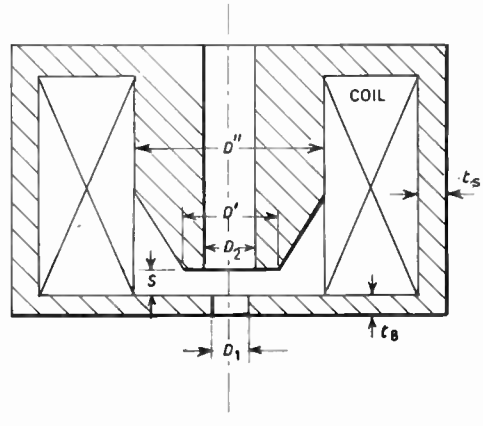

Fig. 16. Magnetic lens construction.

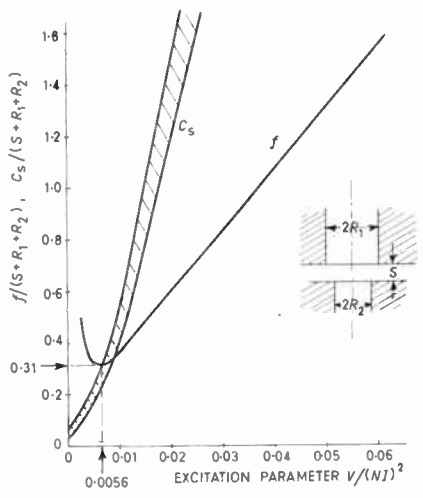

Fig. 17. Liebmann's unified design curves.

lenses where the object is not at the focus, the focal length will increase as shown in Fig. 17 and the minimum focal length is obtained for $V/(NI)^2 = 0{\cdot}0056$. The curve for C_s applies to an object at the focus, for imaging lenses its minimum is probably also for $V/(NI)^2 = 0{\cdot}0056$.

The following equations approximate Liebmann's curves:

$$\frac{f}{(S+D)} = 25\frac{V}{(NI)^2} \qquad \text{.....(4)}$$

$$C_s = 5\frac{f^3}{(S+D)^2} = 3130f\left\{\frac{V}{(NI)^2}\right\}^2 \qquad \text{.....(5)}$$

In a simple design, $V/(NI)^2 = 0{\cdot}0056$ is used and the required focal length determines $(S+D)$. The polepiece dimensions are then found by taking $S = D_1 = D_2$ for minimum aberration. If necessary, the proportions may be altered so that $S \neq D_1 \neq D_2$ and Fig. 17 can still be used taking $(S+R_1+R_2)$ instead of $(S+D)$.

The outside diameter of the polepiece D' is taken as

$$D' = D+2S \qquad \text{.....(6)}$$

so that the fringing field does not affect the field in the gap. The other lens dimensions are calculated by following Mulvey's design procedure[8] to keep the flux density below saturation.

7.2. *Spherical Aberration*

Spherical aberration in magnetic lenses causes a point image at the focus to be spread into a disk of confusion of radius r given by

$$r = C_s\gamma^3 \qquad \text{.....(7)}$$

where γ = beam half-angle at the image and C_s is a constant known as the spherical aberration coefficient.

Equation (7) refers only to an image at the focus, but Petrie[9] has shown that the aberration disk for an image distance v' is given by:

$$r = C_s\left(\frac{v'}{f}\right)^4\gamma^3 \qquad \text{.....(8)}$$

Using subscripts 1 and 2 for the object and the image respectively,

$$r_2 = C_s\left(\frac{v'}{f}\right)^4\gamma_2^3 = C_s\left(\frac{u'}{f}\right)^4\left(\frac{v'}{u'}\right)^4\gamma_2^3$$

where u' = object distance.

Introducing the magnification, M, so that

$$M = \frac{v'}{u'} = \frac{\gamma_1}{\gamma_2},$$

the radius of the disk of confusion at the image,

$$r_2 = M\,C_s\left(\frac{u'}{f}\right)^4\gamma_1^3$$

$$= Mr_1$$

The aberration disk is magnified in the same ratio as the image and Petrie's formula (eqn. (8)) may be applied either to the image or the object.

To compare the relative aberrations of the condenser and the objective in the electron beam machine, a modified spherical aberration coefficient C_s^*, which applies to one particular image at v', is found useful where

$$C_s^* = C_s\left(\frac{v'}{f}\right)^4 \qquad \text{.....(9)}$$

The increase in spot size due to the objective lens will be

$$r_o = C_{so}^*\gamma_2^3 \qquad \text{.....(10)}$$

and the increase caused by the condenser lens, referred to the gun cross-over will be,

$$r_{cx} = C_{sc}^*\gamma_1^3$$

This increase is magnified by the two lenses and results in an increase in final spot size,

$$r_c = Mr_{cx} = MC_{sc}^*\gamma_1^3$$

But

$$\gamma_1 = M\gamma_2$$

Therefore

$$r_c = M^4C_{sc}^*\gamma_2^3. \qquad \text{.....(11)}$$

The resulting total aberration can be found by combining r_c and r_o in quadrature.[10] If

$$M^4C_{sc}^* \leq 2C_{so}^* \qquad \text{.....(12)}$$

the resulting aberration will be increased by less than 11% over that due to the objective alone and will be considered negligible.

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Characteristics of Varactor Diodes at Low Temperatures

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Summary: An experimental investigation of varactor diode junction properties at low temperatures has been performed. Both elemental and compound type diodes have been examined, including two silicon varactors produced by different doping techniques and a diffused mesa-type gallium arsenide varactor. The diode spreading resistance is calculated from *Q*-factor measurements with an appropriate correction applied for the loss in the measuring line.

List of Principal Symbols

α	rate of change of diode contact potential with temperature
ρ	charge density of the depletion layer
ψ	electrostatic potential
ε	permittivity of the semiconductor material
$C_J(v)$	voltage dependent junction capacitance
σ	conductivity of semiconductor material
μ	electron mobility
N_D	donor concentration
N_A	acceptor concentration
b	ratio of electron mobility to hole mobility
c	ratio of electron concentration to hole concentration
$f_c(v)$	diode cut-off frequency at v volt bias
f_m	measuring frequency
$Q(v)$	diode quality factor at v volt bias
P	measuring-line loss
R_s	diode spreading resistance
Z_o	characteristic impedance of the measuring line

1. Introduction

A reverse-biased semiconductor diode can be used as a capacitor having a linearly graded junction. Diodes specially prepared to make use of this effect are termed 'varactor diodes' and have found applications in parametric amplifiers and frequency multipliers up to microwave frequencies.

Parametric amplifiers using varactor diodes as the non-linear element are not subject to the main sources of noise encountered in amplifiers using thermionic valves and thus are useful where low-noise amplification is necessary. If the diode is biased beyond forward conduction, no current flows and shot noise will be absent. However, due to the inevitable losses in the diode and the associated amplifier circuits some thermal noise is always introduced; this may be reduced by cooling the amplifier. Cooled parametric amplifiers are suitable for use in satellite communications and in radio astronomy. A simple calculation of noise temperature[2] for an amplifier cooled in liquid helium suggests that the noise performance should be comparable with that of a maser. However, in practice the noise temperature available from a helium-cooled varactor-diode parametric amplifier is somewhat higher than the calculated value. This increase may in part be attributed to anomalous behaviour of the diode at low temperatures. This paper describes attempts made to determine experimentally the performances of three typical varactor diodes namely (a) a short diffused silicon varactor, (b) a prolonged diffused silicon varactor[10] and (c) a diffused junction mesa-type gallium arsenide varactor.

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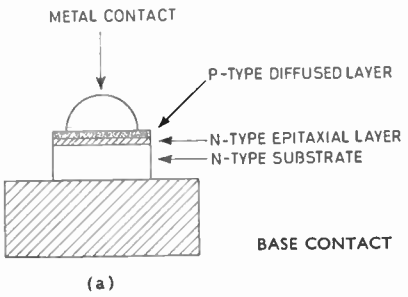
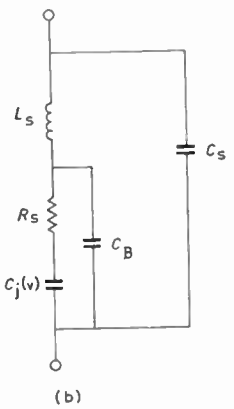
2. Theoretical Considerations

Figure 1(a) shows a typical varactor diode construction.

The a.c. small signal equivalent circuit normally used to represent such a varactor diode is shown in Fig. 1(b), where $C_J(v)$ is the voltage dependent junction capacitance and R_s is the series (spreading) resistance. Because the latter is mainly due to the resistivity of the bulk of the semiconductor material, the value of R_s is dependent on the conductivity of the semiconductor material. L_s is the series inductance within the diode encapsulation, C_s is the capacitance introduced by the case and C_B is the stray capacitance across the junction. The variation of $C_J(v)$ and R_s as functions of temperature must be examined. Because the principal source of noise within the amplifier is the series resistance R_s, the experimental measurements must be arranged to determine the changes which occur in R_s as the diode is cooled. It is shown by Uenohara and Wolfe[12] that some diodes show large increases in R_s as liquid helium temperatures are reached.



(a) Typical construction of a varactor diode.



(b) Varactor diode equivalent circuit.

Fig. 1.

The change in $C_J(v)$ at low temperatures will be small, and as the approximate variation of contact-potential with temperature for gallium arsenide and silicon is known, it is possible to calculate the change to be expected in $C_J(v)$. If this change in $C_J(v)$ is calculated and the change in diode Q-factor is measured as a function of temperature, the relevant change in spreading resistance with ambient temperature can then be determined.

In order to calculate $C_J(v)$ as a function of temperature, it will be assumed that the diode has a linearly graded junction[2], where the net impurity concentration varies linearly across the diode in the vicinity of the junction and that the resultant space-charge due to the ionized donor and acceptor impurities is also distributed linearly over the depletion layer, extending from $-d/2$ to $+d/2$. Then the charge density of the depletion layer, ρ, is given by:

$$\rho = (N_D - N_A)q$$
$$= kqx; \; -\frac{d}{2} < x < \frac{d}{2} \qquad \text{.....(1)}$$

In these equations, q is the elementary charge, N_D and N_A are respectively the excess donor and acceptor concentrations on either side of the junction.

Poisson's equation within the depletion layer is then

$$\frac{d^2\psi}{dx^2} = \frac{-\rho}{\varepsilon} = \frac{qkx}{\varepsilon} \qquad \text{.....(2)}$$

where ψ is the electrical potential and ε is the permittivity of the semiconducting material of the diode.

Equation (2) is integrated twice, and the following boundary conditions applied:

$$\begin{cases} \dfrac{d\psi}{dx} = 0 \text{ at } x = \dfrac{d}{2}; \; -\dfrac{d}{2} \\ \psi = 0 \text{ at } x = 0 \end{cases}$$

This gives the solution

$$\psi = \frac{qkx}{2\varepsilon}\left(\frac{x^2}{3} - \frac{d^2}{4}\right)$$

The potentials at the edges of the depletion layer are obtained by substituting $x = -d/2; \; +d/2$, and the potential difference between the two boundaries of the layer is thus obtained. The value is $qkd^3/12\varepsilon$, and this must be equal to the sum of the (negative) applied bias, v, and the contact potential, ϕ.

$$(\phi - v) = \frac{qkd^3}{12\varepsilon} \qquad \text{.....(3)}$$

Hence the depletion layer thickness d is given by

$$d = \left(\frac{12\varepsilon(\phi - v)}{qk}\right)^{\frac{1}{3}}$$

Integrating eqn. (1) from $-d/2$ to 0 gives the total charge on either side of the origin

$$Q = \frac{qd^2k}{8} = \frac{qk}{8}\left(\frac{12\varepsilon(\phi - v)}{kq}\right)^{\frac{2}{3}}$$

and differentiating with respect to the total potential across the diode, $(\phi - v)$ gives the capacitance

$$C_J(v) = \left(\frac{kq\varepsilon^2}{12\phi}\right)^{\frac{1}{3}}\left(\frac{1}{1 - \dfrac{v}{\phi}}\right)^{\frac{1}{3}} \qquad \text{.....(4)}$$

The temperature dependence of capacitance is due to the variations of the contact potential, and this may be written

$$\phi = \phi_{25} + \alpha(T - 25); \; T \text{ in degrees Celsius} \qquad \text{.....(5)}$$

where α is approximately -2mV/deg C for silicon and gallium arsenide.[10]

If we write

$$\left(\frac{kq\varepsilon^2}{12\phi_{25}}\right)^{\frac{1}{3}} = C_J(0)_{25},$$

the zero-volt junction capacitance at 25°C, then

$$C_J(v)_T = \frac{C_J(0)_{25}}{\left[1 - \left\{\dfrac{v - \alpha(T - 25)}{\phi_{25}}\right\}\right]^{\frac{1}{3}}} \qquad \text{.....(6)}$$

and this equation will be used in computing the diode

resistance from the measured values of Q. The equation is plotted in Fig. 2 using the parameters which apply to the three diodes under examination.

The diode spreading resistance is inversely proportional to the conductivity (σ) of the semiconductor material and hence the conductivity at low temperatures must be considered. For purer semiconductors and assuming electrons are the majority charge carriers the following relationship holds:

$$R_s = \frac{t}{A\sigma} \qquad \text{.....(7a)}$$

$$\sigma = e\mu n \qquad \text{.....(7b)}$$

where e is the electronic charge, μ is the electron mobility, n is the effective carrier density, t is thickness of the base material and A is the area of the junction (assuming electrons are the only charge carrier).

When both electrons and holes contribute significantly to conduction, eqn. (7b) must be considerably modified, to become:

$$\sigma \simeq \mu e n_i \frac{(1+bc)}{b\sqrt{c}} \qquad \text{.....(8)}$$

where $b(>1)$ is the ratio of electron mobility to hole mobility, c is the ratio of electron concentration to hole concentration and n_i is the intrinsic carrier concentration. The quantity c is temperature variant and N_A the acceptor concentration is temperature invariant under fully ionized condition and the relationship of N_A, c and n_i is as follows:

$$n_i = \frac{N_A\sqrt{c}}{(1-c)} \qquad \text{.....(9)}$$

Substituting the value of n_i in (8):

$$\sigma = \mu e N_A \frac{(1+bc)}{b(1-c)} \qquad \text{.....(10)}$$

For specific samples b and c can be estimated for a particular temperature, and if the added impurity

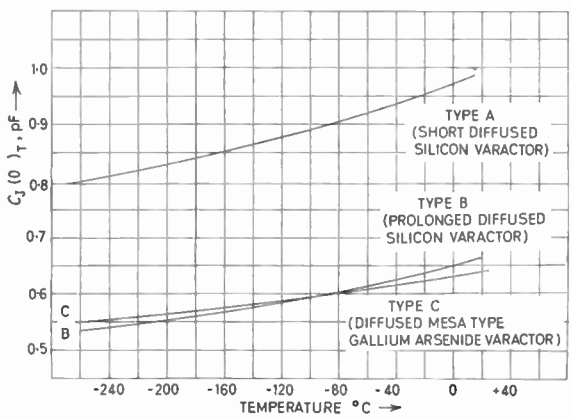


Fig. 2. Curves for zero bias capacitance against temperature.

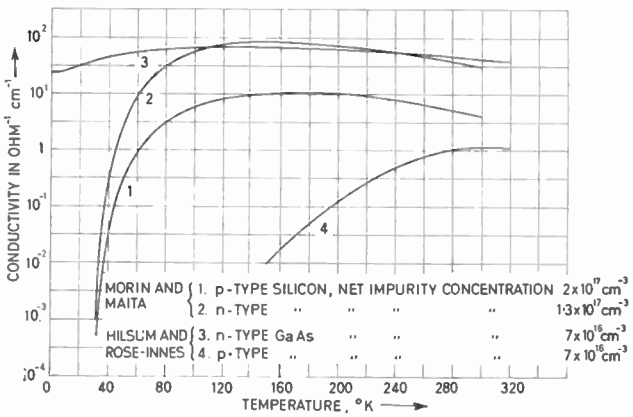


Fig. 3. Curves showing the variation of conductivity with temperature.

concentration is known σ can be estimated from eqn. (10) provided that μ remains at its ambient temperature value. At low temperatures the electron mobility is, however, perturbed by various scattering processes. The most important types of scattering which affect the mobility of electrons through crystals are lattice scattering, impurity scattering and carrier-carrier scattering. At low temperatures the predominant scattering in varactor diode p-n junctions is the impurity scattering and at low temperature some of the impurities are ionized giving rise to charged impurity centres, with a corresponding increase in resistivity. Although theoretical calculations have been made,[4] the results are very approximate and do not correlate well with the experimental results. Some experimental measurements on resistivity at low temperatures have been published and values are plotted in Fig. 3. These refer to some of the results obtained by Morin and Maita[3] on the p- and n-type silicon semiconductors, together with the results outlined by Hilsum and Rose-Innes[4] on the p- and n-type gallium arsenide semiconductors. The conductivity of both p- and n-type silicon semiconductors follows smooth curves down to about 80°K and tends to become almost asymptotic at about 30°K. On the other hand the n-type gallium arsenide sample follows a smooth curve with temperature and starts a gentle slope at about 80°K and thereafter the conductivity decreases slowly down to 10°K. Beyond that, the graph is extrapolated. The p-type gallium arsenide is a high resistivity sample and is therefore not relevant to varactor diodes.

3. Varactor Measurements

In the design of low-noise parametric amplifiers for use at microwave frequencies, measurements at low frequencies are not suitable and microwave techniques must be used to determine the characteristics

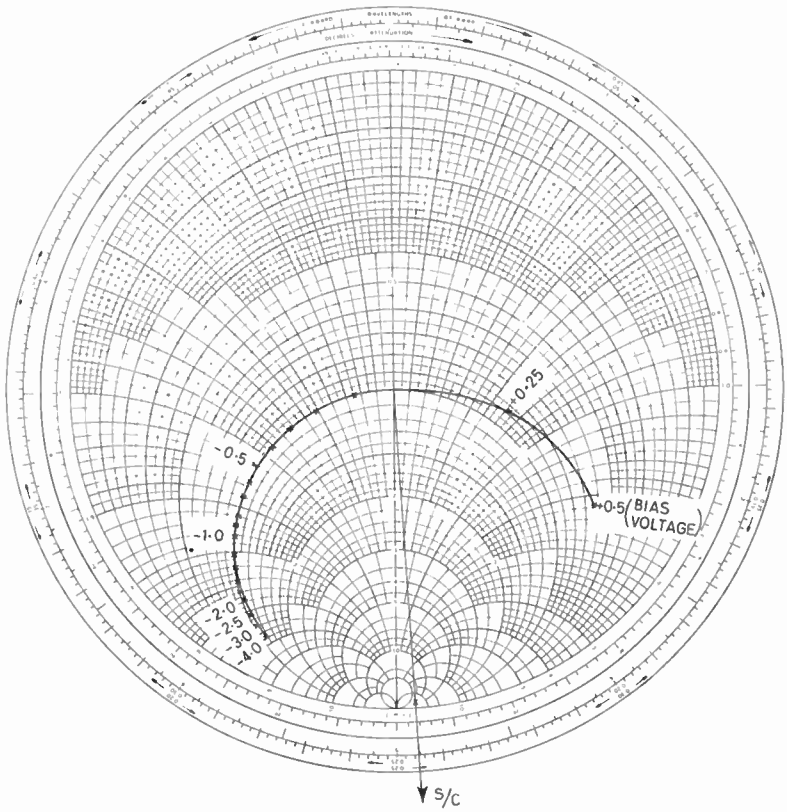


Fig. 4. Diode impedance plot derived by Harrison's method (gallium arsenide varactor).

of diodes at their operating frequencies. Such methods usually give a direct measure of the Q-factor of the diode. The component values can then be deduced from the following relationship:

$$Q(v) = \frac{1}{2\pi f_m C_J(v) R_s} = \frac{f_c(v)}{f_m} \qquad \text{.....(11)}$$

where $Q(v)$ is the diode quality factor at v volt bias, f_m is the measuring frequency and $f_c(v)$ is the cut-off frequency at v volt bias.

There are several methods of determining the Q-factor of varactor diodes, but for the present purposes, those methods using mounts with resonant tuning elements are unsuitable for measurement of diodes at cryogenic temperatures. The methods of Waltz[5], Houlding,[6] Roberts[7] and Harrison,[8] are all suitable for the measurement of diodes at microwave frequencies but the method used by Harrison is simple and has been found to be particularly suitable for the present measurements. The experimental arrangement is shown in Fig. 6, and consists basically of a low-loss coaxial line connecting the diode mount to a variable impedance waveguide-to-coaxial transformer. A reference impedance can be provided by replacing the diode by a short circuit 'dummy' diode. Measurements are then made of the diode impedance at various bias values, the results being plotted on a Smith chart. A series of bias voltages is chosen, the effective capacitive reactances are determined and on division by the real part of the complex impedances these yield the Q-factors for the respective bias voltages. The analysis of Harrison's method is given in the Appendix.

Since the technique is based upon a matched system, the resultant plot will be of a unit circle on a normalized chart, if R_s is constant for all bias values and if there is negligible attenuation between the point of measurement and the diode. As an example Fig. 4 shows the results for one of the varactor diodes under examination, made at a frequency of 4·170 GHz where the Q-factor is 33 and the cut-off frequency is 138 GHz. These measurements were confirmed by the use of a General Radio transfer function and admittance bridge type 1607 A. This however, gives the effective total series resistance and reactance at the diode terminals which must then be resolved into the

intrinsic parameters R_s and $C_J(v)$. Figure 5 shows the results obtained by machine computation from measurements made using the bridge at a frequency of 1 GHz. The bias voltage dependence of R_s is shown, for the short diffused silicon varactor and the diffused junction mesa type GaAs varactor where the values deduced from Harrison's method are also shown for the GaAs varactor. The value of R_s, therefore, can be taken as approximately independent of v.

In order to measure the varactors when cooled, they were mounted on a length of coaxial line, the end of which could be inserted into a Dewar of refrigerants; usually liquid nitrogen or helium. The coaxial line must be of low loss and yet be of low thermal conductivity, which leads to a compromise. Low thermal conductivity was achieved by the use of stainless steel and the attenuation was minimized by copper plating the inner surface of the line.

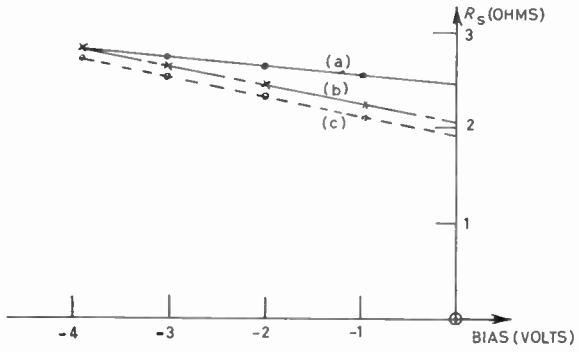


Fig. 5. Variation of R_s with bias for:
(a) short diffused silicon varactor,
(b) diffused junction mesa GaAs varactor, } 1 GHz Bridge
(c) as for (b), derived from Harrison's method.

When measurements are made using Harrison's method it is possible to correct for the finite but low value of attenuation as shown by Hyde and Smith.[9] It is possible to determine the value of Q-factor at room temperature and then at the required temperature, but this necessitates prolonged operation under cooled conditions and the value of R_s can only be deduced by using eqn. (6) in the computation. Because the short circuit reference must be accurately measured for each case, the diode and dummy must be repeatedly interchanged and this is a major source of error due to the slight variations in the repositioning of the component. Corrections for line loss must be applied which involves a further set of measurements.

However, the process may be simplified by lowering the diode mount and the line carefully into a Dewar already filled with liquid coolant and then matching the system with the diode in place under cooled conditions. The complete line and diode mount are then allowed to reach room temperature; taking care to avoid ice forming in the system when the line is withdrawn. Diode impedance measurements are then made at various bias voltages. If a plot were constructed for the low temperature condition it would approximate to the unit circle because the system is matched at the required temperature; the second plot for a higher temperature will not follow the unit circle since both R_s and $C_J(v)$ have changed, but the value of R_s will still be constant for all bias values so that the measurements should fit some other constant resistance circle on the Smith chart. The ratio of these normalized resistance values may then be used to show the effect of cooling the diode upon R_s. Of course it is still necessary to assess the line loss under all conditions and make the appropriate corrections but the technique does avoid the necessity of critical measurements at low temperatures.

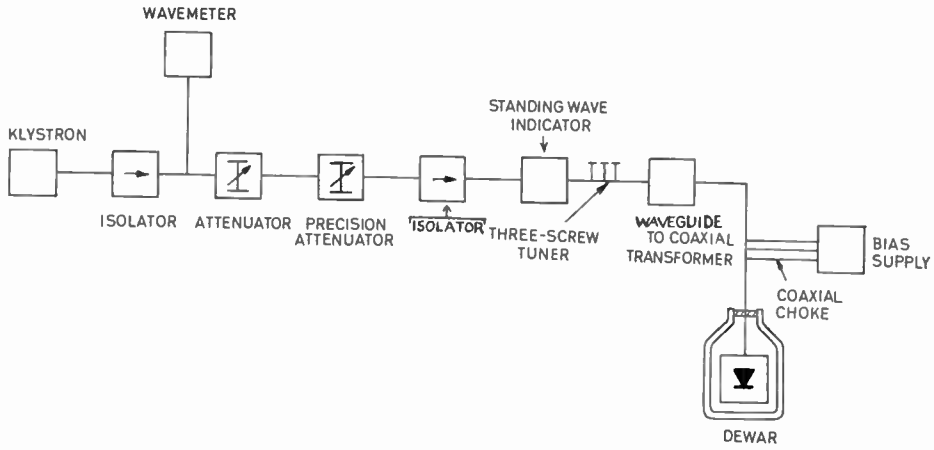


Fig. 6. Block diagram of measuring apparatus.

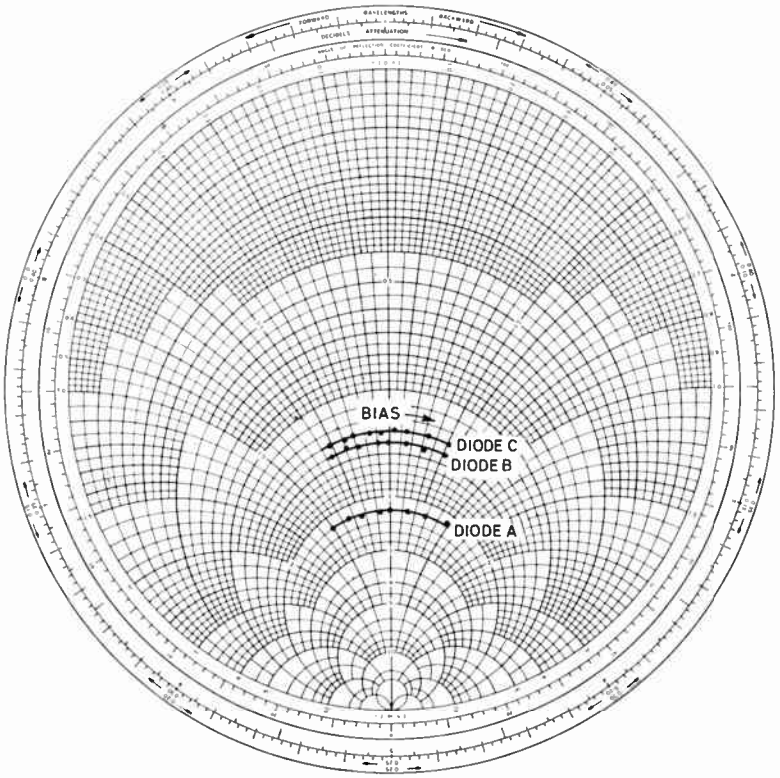


Fig. 7. Loci of spreading resistance (R_s) normalized to R_s at 77°K, for bias 0–3V.

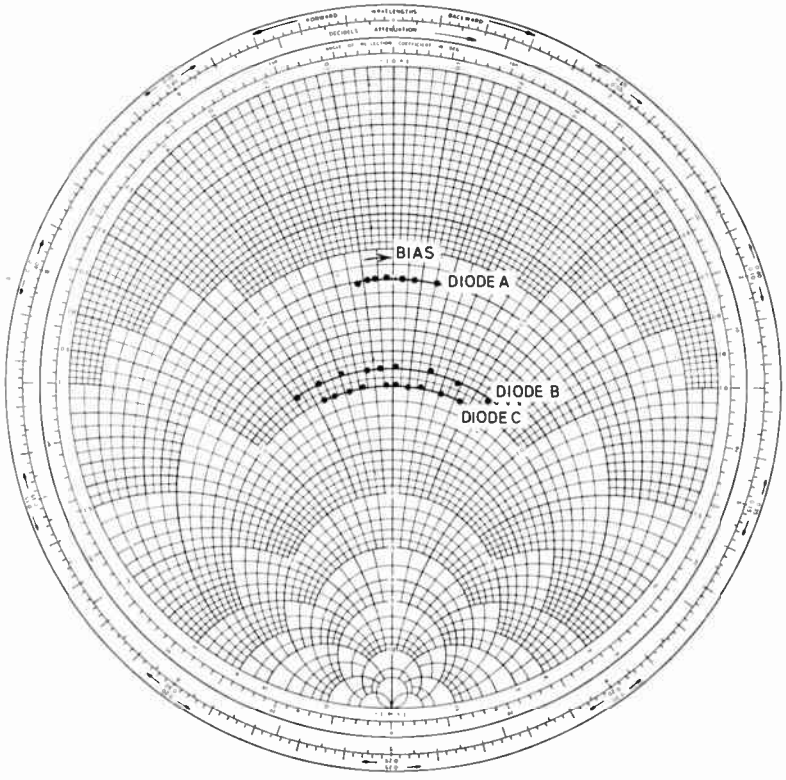


Fig. 8. Loci of spreading resistance (R_s) normalized to R_s at 4°K, for bias range 0–3V.

Table 1

Diode parameters at room temperature

Diode	Measured $Q_D(0)$ at 4·17 GHz	$R_s(\Omega)$	$C_J(0)$ (pF) at 1 GHz	ϕ(V)	C_s(pF)	L_s(nH)
Type A—short diffused silicon	13	2·6	1·00	0·6	0·30	0·45
Type B—prolonged diffused silicon	23	2·5	0·67	0·6	0·19	0·40
Type C—diffused junction mesa gallium arsenide	33	2·0	0·64	1·0	0·19	0·40

4. Diode Performance

Table 1 shows the values of the diode quality factor at zero bias $Q_D(0)$, the spreading resistance and the junction capacitance measured for the three diodes at room temperature. For reference, the additional parameters ϕ, C_s and L_s from the manufacturers' data are also included.

Application of the technique outlined above produced the Smith chart plots shown in Figs. 7 and 8 for operating temperatures of 77°K and 4°K respectively. These plots yield the uncorrected relationship between R_{300}, the value of R_s at room temperature and R, the value at the operating temperature. If the loss of the connecting line is known, it is possible to apply a correction as described by Hyde and Smith.

The measured and corrected values are related by the equation (12) and are set out in Table 2.

$$\left(\frac{R}{R_{300}}\right)_{\text{measured}} = \frac{R\left[1+P_2\left(\frac{R}{Z_0}+\frac{Z_0}{R}+\frac{X_2^2}{Z_0R}\right)\right]}{R_{300}\left[1+P_1\left(\frac{R_{300}}{Z_0}+\frac{Z_0}{R_{300}}+\frac{X_1^2}{Z_0R_{300}}\right)\right]} \quad \ldots\ldots(12)$$

where the values of R and R_{300} on the right of the equation are the actual values.

The other quantities are as follows:

Z_0 = characteristic impedance of the line

X_1 = reactance due to $C_J(0)$ at room temperature

X_2 = reactance due to $C_J(0)$ at the operating temperature as deduced from eqn. (6)

P_1 = transmission loss in nepers at room temperature

P_2 = transmission loss in nepers at operating temperature

The corrections applied are in accordance with eqn. (12) where the line loss was carefully measured independently at the various temperatures. It is estimated that the errors involved in arriving at the above values do not exceed 20%.

Table 2

Measured and corrected values of R/R_{300} for the three diodes

Diode	Measured values		Corrected values	
	R/R_{300} at 77°K	R/R_{300} at 4°K	R/R_{300} at 77°K	R/R_{300} at 4°K
Type A	0·45	2·00	0·33	2·90
Type B	0·72	1·11	0·69	1·45
Type C	0·78	1·00	0·76	0·70

5. Comment on the Results

The measuring techniques based on Harrison's method have proved to be simple and consistent in the measurement of varactor diodes at low temperatures. The results demonstrate that of the diodes tested, the silicon varactors are not suitable for helium operation due to increased resistivity and consequent degradation in the diode quality factor. Prolonged diffusion as predicted by Benny[10] improves the performance of silicon varactor down to nitrogen temperature and it can be anticipated that proper diffusion over a prolonged period would compensate the resistivity profile of the silicon varactor which may prove successful even at helium temperature.

6. Conclusions

The gallium arsenide varactor tested in these experiments is suitable for operation at liquid helium temperature, although allowance must be made for an increase in Q-factor. The diode should therefore be suitable for use in a helium cooled parametric amplifier.

7. Acknowledgment

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9. Appendix

9.1. *Theory of Harrison's method of Q_D measurement*

For a four terminal lossless network, such as a section of transmission line, the input and output impedances Z_{in} and Z_{out} are related by

$$Z_{in} = \frac{AZ_{out}+B}{CZ_{out}+D} \qquad \text{.....(13)}$$

where A and D are real and B and C are imaginary. If a diode with spreading resistance R_s is connected across a section of transmission line of characteristic impedance R_0 and if the condition of conjugate matching is attained, eqn. (13) becomes

$$R_0 = \frac{AR_s+B}{CR_s+D} \qquad \text{.....(14)}$$

If the diode is now replaced by a short circuit, Z_{out} becomes equal to zero and Z_{in} will then become equal to B/D. As this is purely imaginary, Z_{in} now represents a reactance, with a value lying between plus and minus infinity depending upon the choice of input reference plane. If the position of this plane is chosen to be where $Z_{in} = 0$, then the value of B must also be zero. For the right-hand side of eqn. (14) to be real when $B = 0$, it follows that C must also be zero for this reference plane.

Thus, if the short circuit is now replaced by the diode, eqn. (14) becomes

$$R_0 = \frac{AR_s}{D}$$

If the diode reactance is altered by changing the bias, the impedance at the reference plane is given by:

$$\begin{aligned} Z_{in} = \frac{AZ_{out}}{D} &= \frac{R_0}{R_s} Z_{out} \\ &= R_0\left(1+j\frac{\Delta X_D}{R_s}\right) \\ &= R_0(1-j\Delta Q) \end{aligned}$$

and the measured values will lie on a unit circle where

$$\frac{X}{R_0} = \frac{X_D}{R_s} = -Q_D$$

X_D is the diode reactance and R_s is constant.

The Q-factor at zero bias can be determined from the input impedance at the reference plane corresponding to a short circuit in place of the diode, when:

$$\frac{Z_{in}}{R_0} = -\frac{jX_{D0}}{R_s} = +jQ_{D(0)}$$

X_{D0} is the value of X_D at zero bias.

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Phase-shifting Networks using Field Effect Transistors

By

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Summary: The use of the field effect transistor in the below pinch-off mode as a variable resistor permits a wide range of phase shifting networks, filters and variable frequency oscillators to be constructed. The technique is fully compatible with integrated circuit technology and the properties of the circuits so produced are only moderately temperature-dependent.

1. Introduction

The field effect transistor (f.e.t.) is receiving[1-3] considerable attention in applications in which it is used as an amplifier or a switch because of its very favourable properties, included amongst which are very high power gain and input impedance, low noise, extreme speed and, as a switch, zero voltage offset. However, the field effect transistor has a further property which is almost unparalleled in other circuit devices. Operated under suitable conditions it can exhibit the properties of an ohmic resistor so far as the circuit between source and drain terminals is concerned, but the value of the resistance is electrically controlled, being determined by the potential difference between the source and gate terminals. The exploitation of this variable resistance property in circuit applications has already been the subject of publications,[4,5] and there can be little doubt that it will play a significant role in the future development of electronic circuit technology, not least because it is the only variable linear passive element available for use in microcircuits.

In order that a f.e.t. shall behave like an ohmic resistor two conditions must be fulfilled:

(a) the potential difference between the gate region and the conducting channel must be such that no significant gate current flows (this condition does not, of course, apply to insulated gate devices), and

(b) the depletion region of the reverse-biased gate to channel p-n junction must at no point along the axis of the channel extend so far as to close or 'pinch-off' the channel.

If these two conditions are met then the source-to-drain channel will show approximately ohmic properties, although there will be some departure from a linear voltage-current relationship as circuit conditions approach those at which pinch-off occurs. The value of resistance measured between drain and source will depend upon the voltage between gate and source terminals of the device, increasing with the reverse bias applied to the gate junction due to the increasing penetration of the depletion region into the conducting channel, and hence the reduction of its effective cross-sectional area. The exact law of dependence of resistance on gate control voltage depends critically on the structural details of the device considered. Usually there is an approximately exponential increase in resistance as reverse gate bias increases, followed by a much sharper increase in resistance as pinch-off conditions are approached. The later effect is rather undesirable, since it occurs at a gate voltage which varies widely from unit to unit. It also results in a marked increase in control sensitivity which may complicate design and sets a limit to the resistance variation range which can be used. Development of transistor structures for variable resistance use will probably aim at 'remote pinch-off' types having an extended range of near exponential dependence of resistance on control voltage. This matter has been discussed by the present author, in connection with the design of electrically controlled variable attenuators,[6] and a structure which goes some way to meeting these requirements has been described. Further developments in this sphere can be expected.

For the present an exponential dependence of drain–source resistance on gate–source voltage will be assumed, that is,

$$R_{DS} = R_0 \exp(\lambda V_{GS}) \qquad \ldots\ldots(1)$$

where R_{DS}, V_{GS} are the drain–source resistance and gate–source voltage respectively, and R_0 and λ are constants characteristic of the transistor concerned, the sign of λ being such that λV_{GS} is positive.

A plot of R_{DS} versus V_{GS} for a commercial transistor type having remote pinch-off properties is given in Fig. 1, and shows that the relationship assumed is not an unreasonable approximation over the range of

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these experimental results. R_{DS} was measured using small alternating voltages, to avoid non-ohmic effects. Where appropriate, the effect on circuit behaviour of the rather more rapid variation of R_{DS} with V_{GS} as pinch-off is approached will be indicated.

It will also be convenient to ignore the distortion of a.c. signals in the networks to be described due to the small non-linearities in the current-voltage relationship for the source-drain circuit which still exist even when pinch-off effects are avoided. This distortion can be very small, harmonic power being as low as 0·01% of fundamental under favourable conditions, and has in any case been treated in considerable detail in the publication on attenuators.[6] Thus, provided that the sum of the direct control voltage applied to the gate and the peak value of any waveform applied to either of the other terminals is not sufficient (either in magnitude of sign) either to cause gate conduction or channel pinch-off, it will be assumed that for practical purposes the device is ohmic. Figure 2 shows the limit on peak values of V_{DS}. The devices will behave in an ohmic manner only below the contours shown. The superior signal handling capacity of high pinch-off voltage (V_p) devices is evident.

Another effect to be neglected in what follows will be the introduction of noise into the circuit by the f.e.t. The noise introduced by such a device is slightly greater than that which would result from an ideal resistor in its place. However, the difference is very small, amounting in favourable cases to only a small fraction of a decibel, and, particularly since the device is capable of operation at quite high signal levels, it is almost invariably possible to neglect the problem of noise in considering f.e.t. phase shifting circuits.

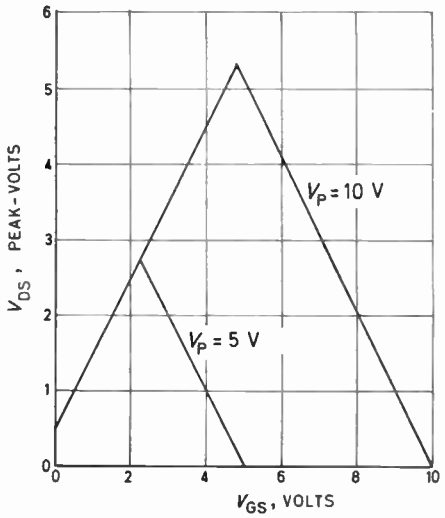


Fig. 2. Permitted operating regions for ohmic behaviour. The device behaves as an ohmic variable resistor provided that the peak drain voltage is such that the working point is within the triangle appropriate to the pinch-off voltage of the device in use.

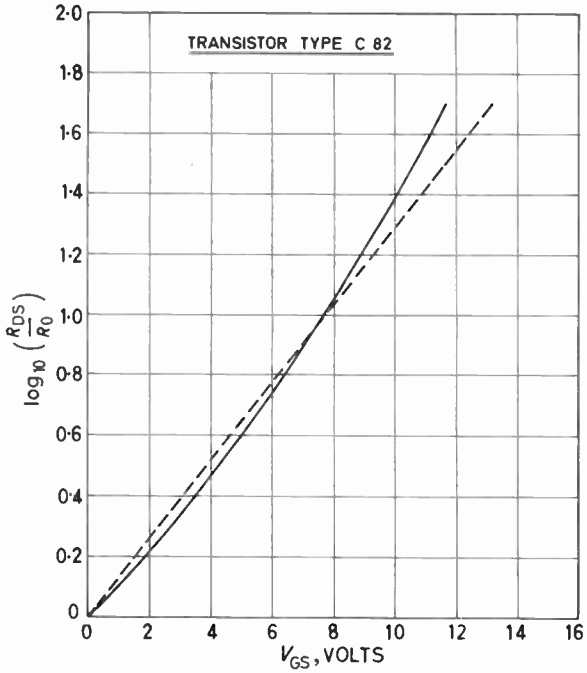


Fig. 1. Resistance versus control voltage characteristic for a 'remote pinch-off' f.e.t.

2. Simple Phase-shift Networks

A particularly simple class of phase-shifting network consists of a resistor and either a capacitor or an inductor. Due to technological problems associated with the use of inductive components, consideration will here be limited to circuits composed of a f.e.t., acting as a variable resistor, and a capacitor. Simple lead and lag circuits thus appear as in Figs. 3(a) and 3(b). Alternative forms are possible, as in Fig. 3(c) where the signal source is a current generator.

For the lead-network of Fig. 3(a) the ratio of output voltage to input voltage is

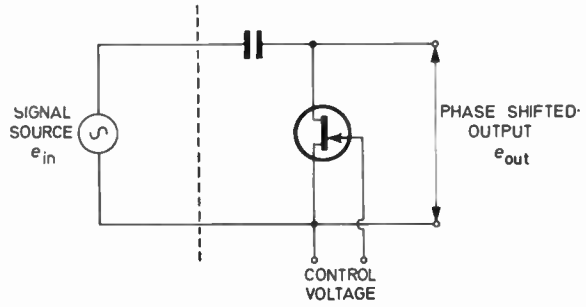
$$\frac{e_{out}}{e_{in}} = \frac{R_{DS}}{R_{DS}+(1/j\omega C)} \qquad \ldots\ldots(2)$$

where ω is the angular frequency of the signal, and C is the value of the capacitor.

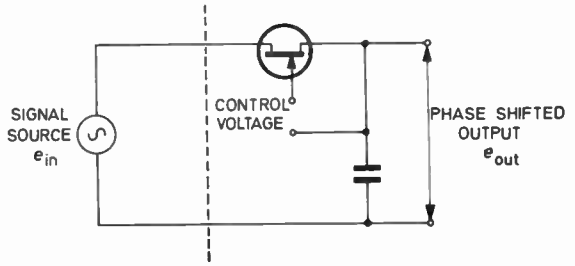
Hence the phase shift ϕ given by the network is

$$\phi = \arctan\left\{\frac{1}{\omega C R_{DS}}\right\} \qquad \ldots\ldots(3)$$

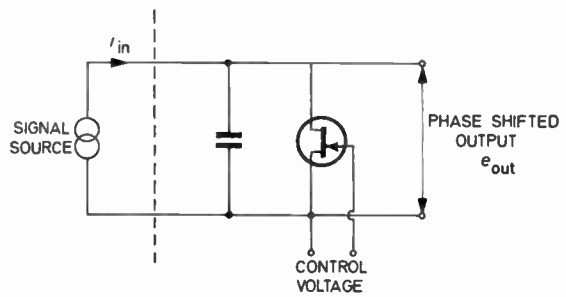
$$= \arctan\left\{\frac{1}{\omega C R_0}\exp\left(-\lambda V_{GS}\right)\right\} \qquad \ldots\ldots(4)$$



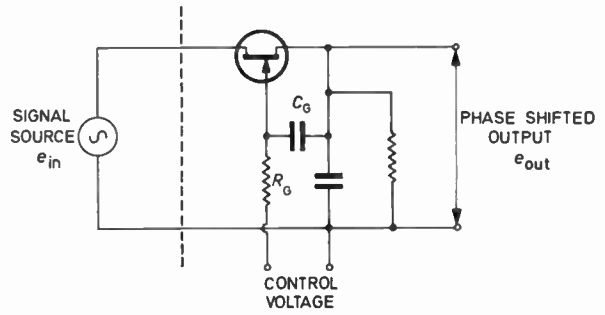
(a) A phase advance network.



(b) A phase retard network.



(c) An alternative phase retard network.



(d) A variant of (b) in which the control voltage is not 'floating' relative to earth.

Fig. 3. Simple phase-shift networks using f.e.t.'s.

assuming that the value of R_{DS} may be obtained from eqn. (1). By suitable choice of C the phase advance at zero gate bias may be set at any required value greater than zero and less than 90°. When a reverse bias is applied to the f.e.t. gate the phase lead is reduced, falling to a low non-zero value as the bias approaches the pinch-off value. Figure 4 shows a series of graphs of ϕ against V_{GS} for a number of different values of initial phase shift. For small angles of phase shift the dependence is initially linear, but becomes less rapid as the phase shift is reduced below approximately one-third of its initial value, and in this region the divergence between experimental results and the predictions of eqn. (4) become significant. As the phase shift is varied there is also a change in magnitude of the output voltage from the circuit, in fact, taking the modulus of both sides of eqn. (2) and using eqn. (3)

$$\frac{|e_{out}|}{|e_{in}|} = \cos\phi \qquad \text{.....(5)}$$

The corresponding lag network (Fig. 3(b)) has closely similar properties, the angle of lag being given by

$$\phi' = -\arctan(\omega C R_{DS}) \qquad \text{.....(6)}$$

$$= -\arctan\{\omega C R_0 \exp(\lambda V_{GS})\} \qquad \text{.....(7)}$$

This circuit is, however, occasionally inconvenient in use because the common terminal of the input and output ports of the network is usually required to be earthed, whilst the control voltage is also usually most conveniently available relative to earth (or some other fixed) potential. This is incompatible with the circuit of Fig. 3(b), which requires the control voltage to be floating with regard to the earth line. Although as shown in Fig. 3(d), this difficulty is quite easily overcome, it may be more convenient to use a different lag circuit if the signal can be derived from a source of high internal impedance, essentially a current generator. In this case the circuit of Fig. 3(c) can be used, the values of lag angle given in eqns. (6) and (7) still applying. The main difference between the two circuits, apart from the greater convenience of applying control voltage in the second, is that whereas for the first the magnitude of the voltage transfer ratio

$$\frac{|e_{out}|}{|e_{in}|} = \frac{1}{(1+\omega^2 C^2 R_{DS}^2)^{\frac{1}{2}}} = \cos\phi \qquad \text{.....(8)}$$

as in the case of the lead network, for the second circuit the ratio of output voltage to input current (the transfer impedance) is equal in magnitude to

$$\frac{|e_{out}|}{|i_{in}|} = \frac{R_{DS}}{(1+\omega^2 C^2 R_{DS}^2)^{\frac{1}{2}}} = R_{DS}\cos\phi \qquad \text{.....(9)}$$

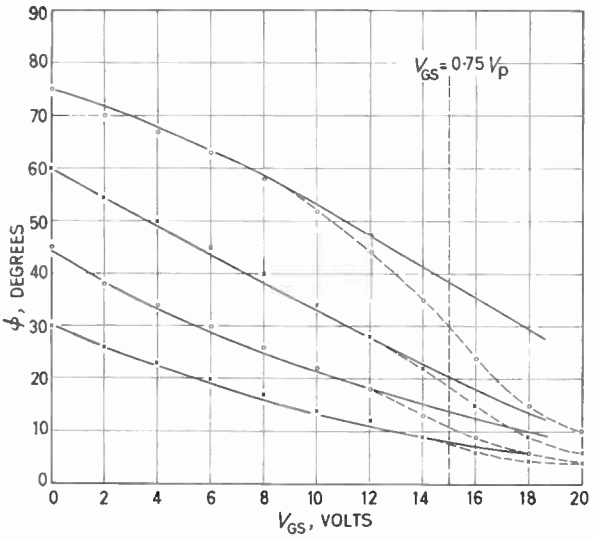


Fig. 4. Characteristics obtained with the network of Fig. 3(a). Points and broken line: experimental results. Full line: values predicted by eqn. (4).

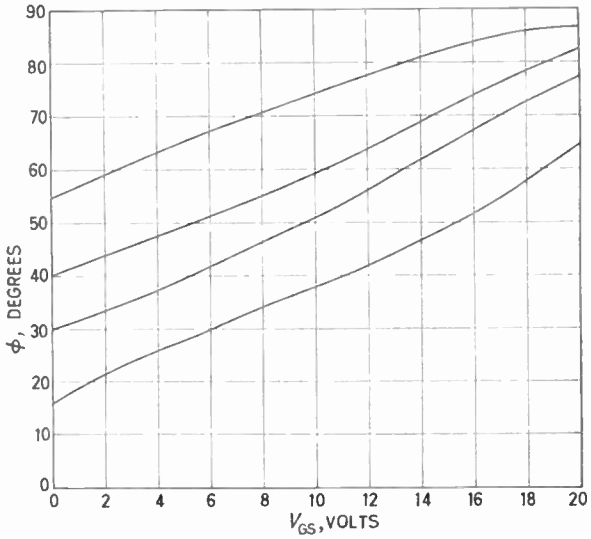


Fig. 5. Experimental results obtained with the network of Fig. 3(d).

This dependence of output voltage on R_{DS} is a disadvantage for certain applications, as will appear below. Figure 5 shows the variation of ϕ' with V_{GS} obtained experimentally with the circuit of Fig. 3(d)).

Experimentally the results shown in eqns. (4) and (7) are well reproduced, subject to two limitations. The f.e.t. drain–source circuit has been represented by a pure resistance, R_{DS}. In fact it is shunted by a stray capacitance which may be in the range from a picofarad to a few tens of picofarads, depending on the details of device design. Thus the results quoted are inaccurate if the value of the capacitor C is not large compared with this stray capacitance, particularly when R_{DS} takes on large values. This effect is most serious at high frequencies where low values of C are used to obtain a given phase shift. Maximum frequency of operation is obtained with transistors having low values of stray capacitance or low values of R_{DS} (permitting higher values of C). At present diffused devices are commercially available having values of R_{DS} as low as 50 ohms, combined with a shunt stray capacitance of only 10 pF, permitting operation up to about 3 MHz without significant change in performance. The circuit of Fig. 3(c) might seem to be advantageous in this respect, since in this case the capacitor C is in parallel with the f.e.t. channel, and thus the stray capacitance only has the effect of modifying the value of C slightly. However, it is not easy to achieve a truly constant current source in aperiodic circuits at megahertz frequencies and above, and in practice it becomes necessary to limit the impedance of the phase-shift circuit so that it shall remain low compared with the internal impedance of the signal source. It should be noted that the stray capacitance shunting the drain–source resistance of the f.e.t. is partly due to end-to-end capacitance of the conducting channel, but a major part is the capacitance of the p-n gate channel junction, since the gate is at a fixed potential relative to the source. For this reason it falls as the reverse gate–source bias is increased.

The second factor limiting the accuracy of the agreement between predicted and experimentally observed variation of phase shift with V_{GS} is due to failure of the channel resistance to obey the simple law of eqn. (1) as assumed. This is particularly obvious (as in Fig. 4) at higher values of V_{GS} where the channel begins to pinch-off and its resistance increases much more rapidly than predicted. For double diffused and epitaxial diffused structures having a sharp pinch-off this effect becomes apparent at values of λV_{GS} of about 1·5, whereas for the remote pinch-off structures, such as the etched alloyed type, the effect is not marked until λV_{GS} exceeds about 2. Consideration of Fig. 4 shows that, since phase-shift networks will usually operate primarily over the initial linear regions of the curves, the effect is small in sharp pinch-off devices and negligible for f.e.t.'s having remote pinch-off, provided that the maximum value of phase shift is not more than about 60 degrees per section.

The simple phase-shift networks described may be used by themselves, or may be combined in various ways to produce more complicated networks having a variety of applications. Some of these applications will now be described.

3. Cascaded Networks

The range of phase shift at a single frequency which can be conveniently obtained with the simple networks so far described is not more than 70° (i.e. 10° to 80°). Where the phase angle is required to vary over a larger range (assuming constant signal frequency) several similar circuits may be cascaded. The phase shift of a series of cascaded networks is not simply the sum of that which they would have produced separately, due to the effect of loading on earlier networks by those following. For example, in the case of a phase-advance network having two identical cascaded sections

$$\frac{e_{out}}{e_{in}} = \frac{j\omega CR_{DS}\left\{\dfrac{j\omega CR_{DS}(1+j\omega CR_{DS})}{1+2j\omega CR_{DS}}\right\}}{\left\{1+\dfrac{j\omega CR_{DS}(1+j\omega CR_{DS})}{1+j\omega CR_{DS}}\right\}\{1+j\omega CR_{DS}\}} \quad \ldots\ldots(10)$$

From this expression the phase shift at a given frequency can be calculated if C and R_{DS} are known. For this particular network the effects of loading are zero when the nominal phase shift per section is 0°, 45° or 90° and rises to maxima of about 11½° midway between these points. The loading effect has been shown[7] (to good approximation) for the case of two identical sections to give a total phase shift equal to θ, where

$$\theta = 2\arctan\left(\frac{1}{\omega CR}\right) + 11{\cdot}5\sin\left\{4\arctan\left(\frac{1}{\omega CR}\right)\right\} \text{ in degrees} \quad \ldots\ldots(11)$$

The effect of loading is seen to be small, and it may be still further reduced by using a sequence of networks in which the value of capacitor is successively reduced, however, at the cost of reducing the total range of phase shift available. In some applications, for example where signal levels are rather small, buffer amplifiers may be interspersed between successive phase shift networks, and in this case the effect of loading is eliminated. The current driven lag-network of Fig. 3(c) cannot be cascaded without the use of buffer amplifiers.

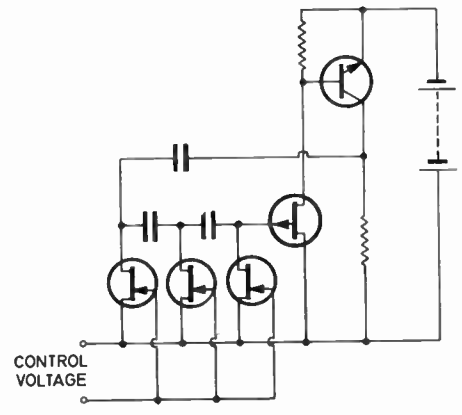


Fig. 7. A voltage-controlled variable frequency oscillator.

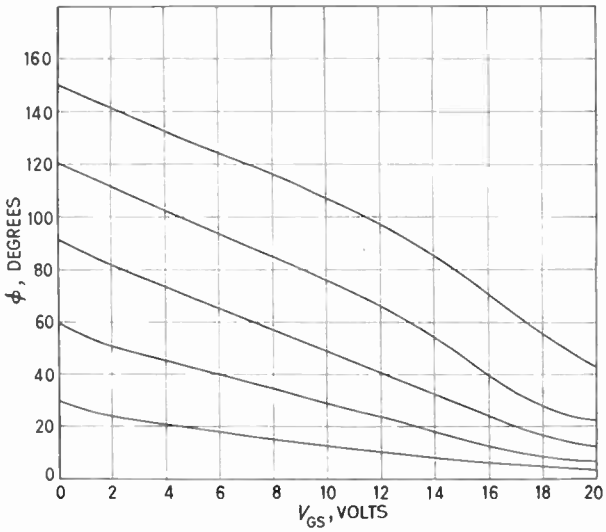


Fig. 6. Experimental results obtained with a two-section phase advance network.

Among applications of cascaded phase-shift networks which have been investigated, a voltage-controlled variable frequency oscillator will be described. Phase shift obtained experimentally with a two-stage phase advance circuit is shown in Fig. 6.

3.1. *A Phase-shift Oscillator*

A simple phase-shift oscillator may be constructed using three cascaded lead-networks to produce a phase shift of 180° and which thus permit oscillation when connected as a feedback loop over an amplifier which produces phase inversion. In this case the total phase shift to be produced is constant and variation of bias applied to the field effect transistor varies the frequency at which oscillation occurs.

For a three-mesh oscillator of this type the oscillation frequency is given by

$$f = \frac{1}{2\pi\sqrt{6}CR_{DS}} = \frac{\exp(-\lambda V_{GS})}{2\pi\sqrt{6}CR_0} \quad \ldots\ldots(12)$$

where the symbols are as above, and subject to the condition that the forward path voltage gain of the amplifier must be not less than 29. A suitable circuit is shown in Fig. 7. This very simple circuit achieves a frequency range of 30 : 1 with good agreement with eqn. (12) over the upper decade of the frequency range. With the f.e.t.'s used in the variable resistance mode in this case (type C85) the lower decade of frequency variation was more rapid than predicted

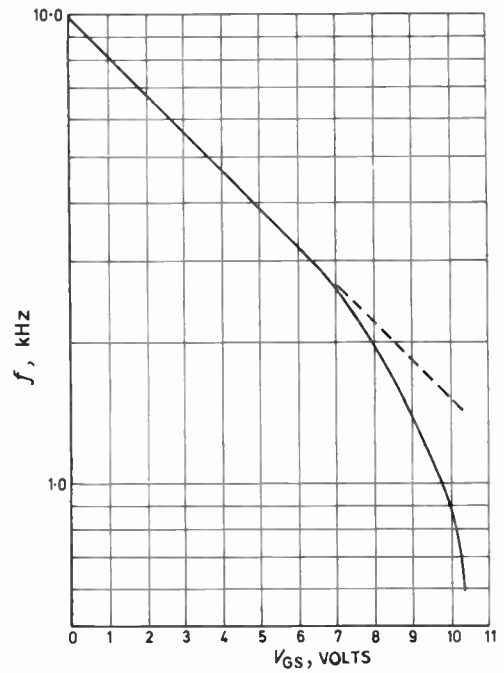


Fig. 8. Frequency versus control voltage plot for the circuit of Fig. 7.

by eqn. (12), due to the onset of pinch-off effects (Fig. 8). Provided that the loop gain is set sufficiently low, good waveform may be obtained, however a practical oscillator would embody some form of a.g.c. to adjust the loop gain, and maintain stable, relatively distortion free, oscillations. With modern transistor structures, having low R_0, there seems to be no reason in principle why oscillators of this type should not operate well above the audio range. An attractive feature of the design is that in the range in which eqn. (12) is a valid approximation the incremental tuning sensitivity (percent frequency change for a given control voltage change) is independent of frequency and is given by

$$\frac{\Delta f}{f} = \lambda \Delta V_{GS} \qquad \text{.....(13)}$$

This feature may be particularly valuable if the oscillator is to be incorporated in a.f.c. systems. The circuit is also one of the few tunable oscillators suitable for direct incorporation in microcircuits.

4. Cascaded Lead and Lag Networks

The lead- and lag-networks described may be cascaded to produce a network which has zero phase shift at a unique frequency. Circuits of this kind are widely used in active filters. There is, however, an important difference between networks produced using a phase-advance network as in Fig. 3(a) and a lag-network of either the form shown in Fig. 3(b) or 3(c). In the former case (assuming that a buffer amplifier is interposed between the sections so that loading effects may be neglected) the voltage transference ratio

$$\frac{e_{out}}{e_{in}} = \frac{j\omega CR_{DS}}{1+j\omega CR_{DS}} \cdot \frac{A}{1+j\omega CR_{DS}}$$

where A is the voltage gain of the buffer amplifier. The imaginary part of the right-hand side of this equation becomes zero, indicating zero phase shift, when

$$1-\omega^2 C^2 R_{DS}^2 = 0 \qquad \text{.....(14)}$$

in which case

$$\frac{|e_{out}|}{|e_{in}|} = \frac{A}{2} \qquad \text{.....(15)}$$

However, if the lag-section were of the shunt type (Fig. 3(c)) the voltage transference (again assuming a buffer amplifier between sections) is

$$\frac{|e_{out}|}{|e_{in}|} = \frac{j\omega CR_{DS}}{1+j\omega CR_{DS}} \cdot \frac{G_f \omega R_{DS}}{1+j\omega CR_{DS}}$$

where G_f is the forward transfer-conductance of the buffer amplifier. The condition for zero phase-shift is given by eqn. (14) as before but this time the transference of the network at zero phase-shift is

$$\frac{|e_{out}|}{|e_{in}|} = \frac{G_f R_{DS}}{2} \qquad \text{.....(16)}$$

and thus depends upon R_{DS}.

It will be seen that for a lead-lag network of the first form the frequency of zero phase-shift can be altered by changing R_{DS} without changing the voltage transfer ratio at zero phase-shift, but that this is not possible with the second form.

5. Frequency Independent Phase-shift

In all the above networks the phase shift has been calculated as a function of frequency. Many systems operate on fixed frequencies and in this case the simple networks described will yield fixed values of phase shift. There is, however, an important field of application for networks which yield a constant phase-shift irrespective of frequency. This result can be achieved, using field effect transistors, over a limited frequency range.[8] Consider the circuit shown in Fig. 9. The system will automatically adjust the value of resistance of the f.e.t. so that the rectified value of the signal voltage obtained from the phase-advance network is almost equal to V_{ref}, which is assumed smaller than the magnitude of the input signal. Thus, assuming that the peak value of the input signal (assumed sinusoidal) is V, then the phase-shift will be

$$\phi''' = \arccos\left\{\frac{V_{ref}}{V}\right\} \text{ assuming } V_{ref} < V \qquad \text{.....(17)}$$

This is unsatisfactory as it stands, because the phase shift obtained is dependent on V.

However, V_{ref} may itself be derived by means of a resistive potential divider and rectifier from the input signal, in which case

$$\phi''' = \arccos(a) \qquad \text{.....(18)}$$

where a (less than unity) is the voltage division ratio (assuming perfect rectification). Thus the phase shift of the network is constant, independent of frequency, and is set by a simple resistive network.

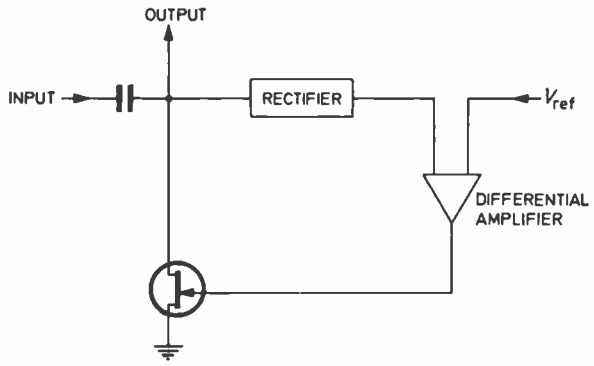


Fig. 9. A system which produces constant phase shift of a sinusoid.

In practical terms, the properties of the circuit are fairly complex, partly because the assumptions made are too simple. Thus the phase shift obtained is not constant, but depends upon a number of factors. However, by careful design, a close approach to constancy can be made which would be sufficient to render the circuit useful in a variety of applications.

6. Temperature Dependence of Phase-shift Networks

All of the circuits described produce phase shift by the use of capacitors and f.e.t.'s, the latter operating as variable resistors. The channel resistance, R_{DS}, is temperature dependent (assuming constant gate–source voltage) for two reasons:

(i) Variation of contact potential between gate and channel. This effect is equivalent to a change in the effective voltage applied to the gate terminal, is of such a sense as to cause a decrease in channel resistance with increasing temperature, and is equal in magnitude to a little over 2 mV/degC, for a silicon junction-gate unit.

(ii) Variations of carrier mobility. The mobility of charge carriers falls with increasing temperature, causing an increase in the magnitude of channel resistance. In silicon junction f.e.t.'s the effect varies between about 0·5 and 0·7% per degC.

To derive an expression for the variation of applied gate–source voltage needed to offset the effects of temperature, eqn. (1) must be rewritten in a form which explicitly includes contact potential. Writing Φ for the latter, eqn. (1) may be amended to

$$R_{DS} = R_0 \exp(\lambda[V_{GS}+\Phi]) \qquad \text{.....(19)}$$

The theory of phase-shifting networks derived in preceding sections was based on eqn. (1) rather than the more precise form of eqn. (19). However Φ is only a fraction of a volt and the magnitude of λ, for the type of f.e.t. best suited to these circuits, is 0·1 or less, so that the consequent error is very small.

By differentiation of eqn. (19) R_{DS} will not vary with temperature if

$$0 = \frac{\delta R_0}{\delta T}\exp(\lambda[V_{GS}+\Phi]) + \\ + \lambda R_0\left(\frac{dV_{GS}}{\delta T}+\frac{\delta\Phi}{\delta T}\right)\exp(\lambda[V_{GS}+\Phi])$$

or, expressed as a condition on the rate of change of the magnitude of the gate bias with temperature,

$$\left|\frac{\delta V_{GS}}{\delta T}\right| = \frac{\alpha}{\lambda}+\frac{\delta\Phi}{\delta T} \qquad \text{.....(20)}$$

where

$$\alpha = \frac{1}{R_0}\cdot\frac{\delta R_0}{\delta T}$$

Practically, the reverse gate bias will need to decrease in magnitude by an amount varying between zero and a few tens of millivolts per degree. Note that whilst α is always positive, for an N-channel device λ is negative and $\delta\Phi/\delta T$ (since the voltage Φ is of such sense as to make the channel more negative than the gate) is positive. The two terms in eqn. (20) are thus of opposite sense, the first predominating for normal values of λ.

Rate of change of gate voltage needed to keep the phase shift constant despite temperature changes is the most convenient mode for expressing drift magnitude in cases where the gate voltage can be adjusted by a feedback system, however, in other cases the gate voltage remains constant and the phase-shift changes. Under these circumstances the drift rate is more conveniently expressed as $(\delta\phi/\delta T)_{V_{GS}}$ where ϕ is the phase shift. Since

$$\left(\frac{\partial V_{GS}}{\partial T}\right)_{\phi}\left(\frac{\partial\phi}{\partial V_{GS}}\right)_{T}\left(\frac{\partial T}{\partial\phi}\right)_{V_{GS}} = -1$$

and from eqn. (4) for a phase-lead network of one section

$$\left(\frac{\partial\phi}{\partial V_{GS}}\right)_{T} = \frac{\lambda}{2}\sin(2\phi),$$

it follows that for a network of this type

$$\left(\frac{\partial\phi}{\partial T}\right)_{V_{GS}} = \left(\frac{\alpha}{\lambda} + \frac{\partial\Phi}{\partial T}\right)\frac{\lambda}{2}\sin(2\phi) \quad \ldots\ldots(21)$$

Similar expressions can be obtained for other phase shifting networks. Typical drift values range from zero up to a small fraction of a degree of angle per degC.

The temperature dependence of R_{DS} can be reduced by, for example, connecting the f.e.t. in series or in parallel (or both) with resistors of lower temperature sensitivity.[5] Dependence of the resistance of the network on control voltage is reduced by the same factor as dependence on temperature and the range of possible resistance variation is reduced. The method is useful primarily in applications where only a modest range of phase shift (or frequency variation for a given phase shift) is required, but where significant temperature dependence cannot be tolerated.

7. Acknowledgments

The author wishes to acknowledge helpful discussions with his colleague, Dr. J. Watson, and assistance with experimental work by Mr. J. Gionis.

8. References

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I.E.R.E. Graduateship Examination, November 1966—Pass Lists

The following candidates who sat the November 1966 examination at centres outside Great Britain and Ireland succeeded in the sections indicated. The examination, which was conducted at 64 centres throughout the world, attracted entries from 376 candidates. Of these, 173 sat the examination at centres in Great Britain and Ireland and 203 sat the examination at centres overseas. The names of successful candidates resident in Great Britain and Ireland will be published in the January–February issue of the *Proceedings* of the I.E.R.E.

	Candidates appearing	*Pass*	*Fail*	*Refer*
Section A: Great Britain	91	36	43	12
Overseas	101	18	80	3
Section B: Great Britain	82	25	40	17
Overseas	102	14	74	14

OVERSEAS

The following candidates have now completed the Graduateship Examination and thus qualify for transfer or election to Graduate or a higher grade of membership.

AGARWAL, R. N. *Delhi, India.*
ANDREWS, A. *Hong Kong.*
D'CRUZ, W. V. (S) *Bombay, India.*
JAGADISH, S. (S) *Bangalore, India.*
JAGANNATH, Y. G. *Bangalore, India.*
KOHLI, M. S. *Delhi, India.*
MUNDAY, J. D. *Nairobi, Kenya.*
PRABHU, R. C. V. K. (S) *Bangalore, India.*
PURUSHOTHAMAN, M. (S) *Delhi, India.*
SANKARA-RAO, N. (S) *Madras, India.*
SANSOM, D. J. (S) *Salisbury, Rhodesia.*
SINGH, D. (S) *Delhi, India.*
WONG, Wing-Cheung *Hong Kong.*
*GREEN, R. F. D. *Sydney, Australia.*

* *Given special permission to sit certain papers.*

The following candidates have now satisfied the requirements of Section A of the Graduateship Examination

DE GROOT, K. *Holland*
GRACE, J. I. *Bermuda*
HALLOUMA, K. R. *Kaduna, Nigeria.*
JARIWALA, S. T. (S) *Bombay, India.*
JUNAIDI, S. R. H. (S) *Hyderabad, India.*
LEE, R. K. K. (S) *Malaysia.*
LIM SENG TECK *Singapore.*
MENSAH, D. K. *Accra, Ghana.*
MORDI, H. U. *Lagos, Nigeria.*
MOUNT, A. E. (S) *Victoria, Australia.*
PAKIANATHAN, T. C. (S) *Malaysia.*
RAJI, Y. A. (S) *Lagos, Nigeria.*
RANAWEERA, G. H. (S) *Ceylon.*
SHARMA, S. P. (S) *Bombay, India.*
SIVABALAN, S. (S) *Colombo, Ceylon.*
SIVAPRAKASAM, N. *Hyderabad, India.*
SNG HONG POH *Singapore.*
SPRUYT, H. J. N. (S) *Holland.*

(S) denotes a Registered Student.

U.D.C. 621.385.833.2: 621.9: 681.32

Computer Control of the Manufacture of Electron Beam Processed Microelectronic Modules

By

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AND

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Presented at a Joint I.E.R.E.-I.E.E. Computer Groups' Symposium on 'Computer Control in Industry: Equipment Design and Application Engineering', held in London on 26th March 1966.

Summary: The characteristics of the electron-beam machine as a welding and cutting tool lend themselves to computer-controlled operation. The paper describes such a combination used to produce a specially-designed microelectronic package. The aim of the system design was to allow the package to be made precisely to the user's requirements by merely reprogramming the computer.

Electron-beam techniques are discussed in relation to the micromodule concept, the machine functions which need to be controlled and the other control elements required are described and the computer input–output and interface characteristics are discussed. Programming aspects are also described. Finally, reference is made to future developments that are thought desirable.

1. Introduction

Computer-controlled processes are commonly associated with bulk product manufacture such as those found in the oil, chemical and power industry. The application to be described in this paper, however, is concerned with high-speed repetitive piece-part production in the factory, where the conditions are more akin to those of a machine tool environment. Computer application to this purpose was inspired by a combination of the characteristics of the electron beam machine, and the need for a fast and flexible system for producing microelectronic components and electronic packages.

The engineer and designer has a continuing problem of finding the most suitable package for his application, whilst the package manufacturer faces the dilemma of trying to accommodate most engineers in this respect in order to make his sales justify the outlay on plant and tooling. The ideal, therefore, is to conceive a process that will allow a large economic production rate, whilst permitting the introduction of package design-change in minimum time and at minimum cost.

2. The Micromodule Concept—Electron Beam Application

The particular micromodule package with which we are concerned is shown in Fig. 1, and an 'exploded' view is shown in Fig. 2. It comprises a stack of square alumina wafers to which are allotted the func-

† Formerly with Hawker Siddeley Dynamics Ltd., Hatfield, Herts; now with S. G. Brown Ltd., Watford, Herts.

‡ Formerly with Hawker Siddeley Dynamics Ltd., Hatfield, Herts; now with The Plessey Co., Swindon, Wiltshire.

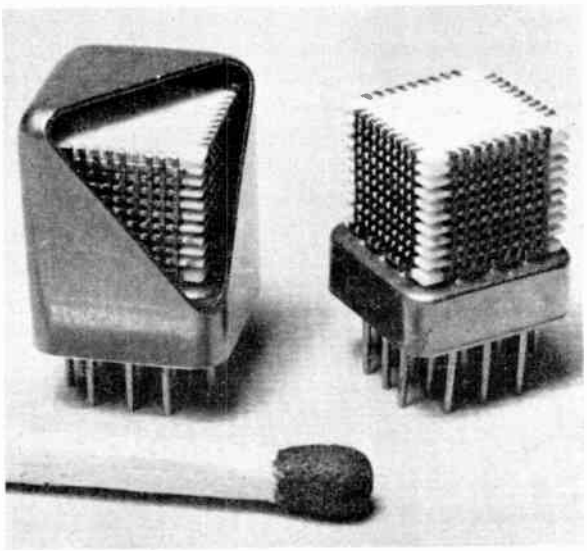

Fig. 1. The microelectronic module.

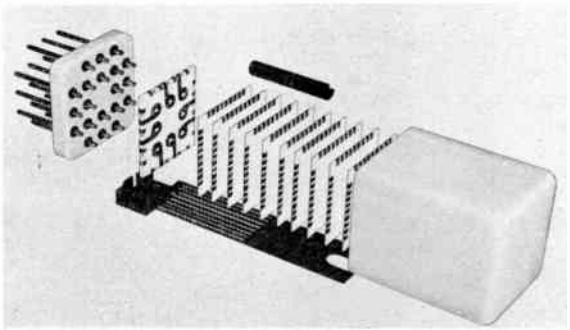

Fig. 2. Module piece parts.

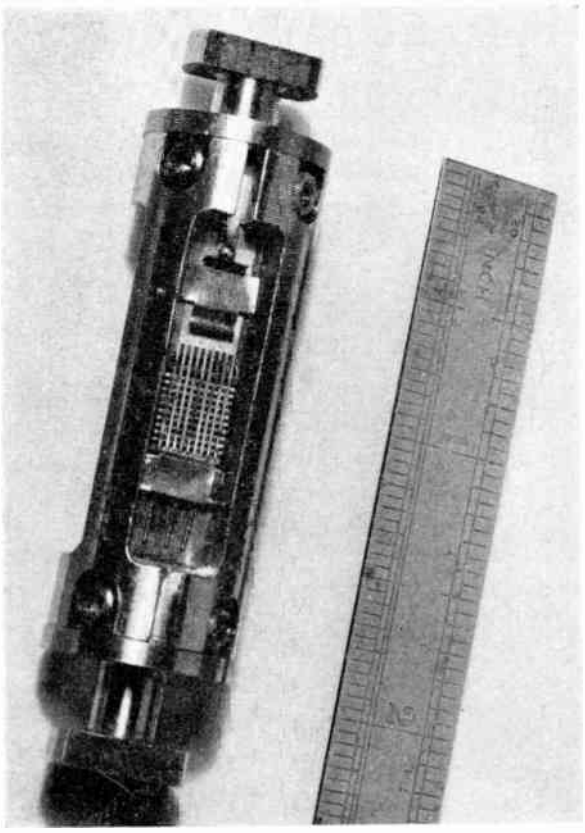

Fig. 3. Cartridge containing a module stack.

tion of semiconductor, capacitor or resistor mounting substrate. The component terminations are brought out to the edges of the wafers by normal thin film and plating techniques to provide nine wrap-round 0·012 in wide terminations per edge. The corresponding terminations on each of the wafers are interconnected by a set of riser wires and the leads to be brought outside the module are connected to the header. The header-stack assembly is mounted in a cartridge (Fig. 3) which is brought on its side under the electron beam whose deflection and pulsing are then programmed to spot weld the riser wire matrix of the stack to the wafer edges of one stack face. Typically, this comprises 99 connections. After successive rotations of the stack, a total of 396 welds are thus made. It is important to note here that the actual weld time is in the region of 10 ms per connection.

After the wafers in the stack have been interconnected, the whole assembly is slid into a can which is a push fit on the header. The second use of the beam welder is then to join the can hermetically to the header—again by programmed deflection and beam current control. The tooling needed to hold and feed the modules to the beam is shown in Fig. 4.

The third electron-beam usage is the most complex, and makes use of the ability of the machine to scribe

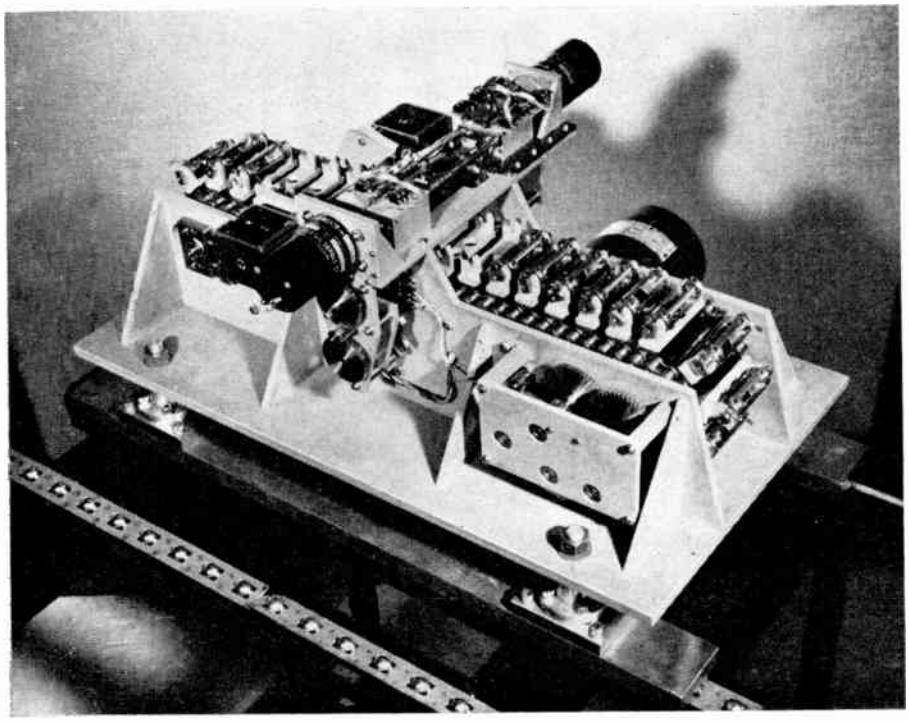

Fig. 4. Weld tooling.

through thin metal films. A pattern is cut in a resistive film which initially overlaps all 36 terminations on the wafer, so that up to six resistors appear between pairs of the terminations, while the other terminations are isolated. The value of each resistor is determined by the length and width of the resistive path that is formed between the relevant terminations. The most convenient pattern is a rectangular meander with constant path width. This is also the best for programming simplicity and heat distribution in the finished resistor.

The variation of sheet resistivity of resistor thin films is invariably wide and since close tolerances of resistor values are required it is not sufficient merely to program a fixed resistance path length. The resistor being scribed is monitored between scribe pulses and when it reaches its correct value, an override signal turns off the beam and stops the generation of that particular pattern. This method enables resistor accuracies of better than 1% absolute to be achieved, over the range 100 ohm–100 kilohms.

The sequence is shown in Fig. 5. In Fig. 5(a), the initial cuts have been made between terminals on a 'blank' wafer. In Fig. 5(b), the areas allocated to each resistor are defined. In Fig. 5(c), the complete patterns are shown. Figure 5(d) shows a typical result, with the patterns shown as having ceased before completion, with the resistors on value. It is, of course, necessary to program the complete pattern to give the correct resistor value assuming a film resistivity

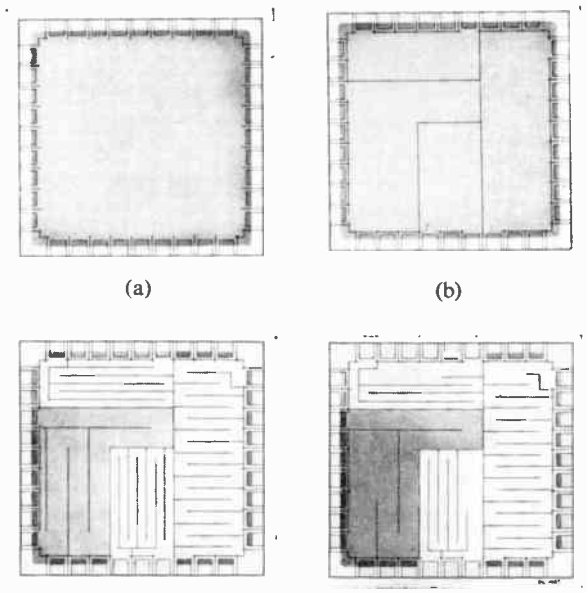

Fig. 5. The scribing sequence.

less than the smallest expected. Figure 6 shows the tooling which carries two magazines each of which can be loaded with 210 wafers. This unit is capable of being mounted in the chamber, fully loaded in 30 minutes, after which only about 15 minutes is necessary to evacuate the chamber. Outgassing of tooling has not been found to affect this time significantly.

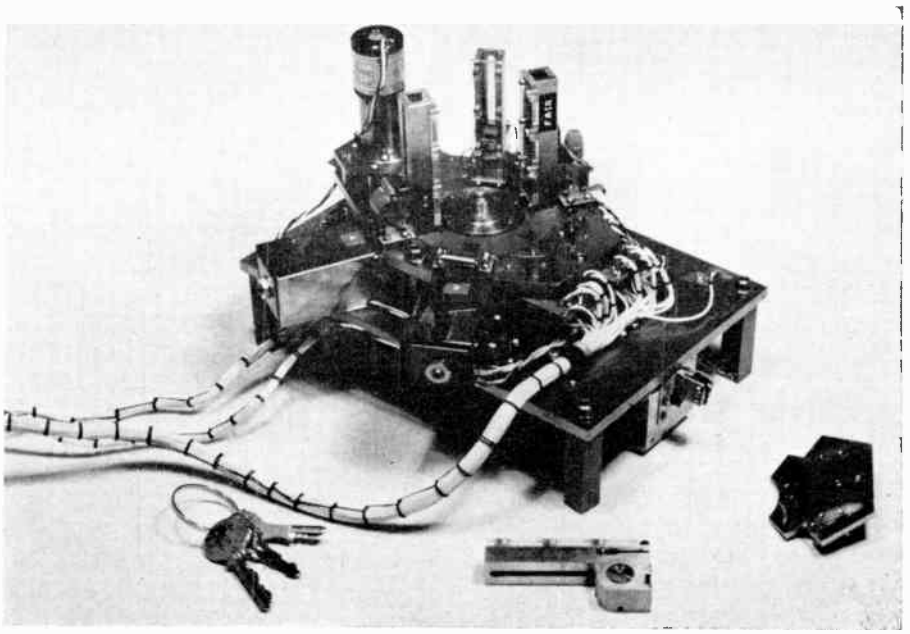

Fig. 6. Scribe tooling.

3. The Electron Beam Machine

The machine used is shown in Fig. 7, and Fig. 8 gives an outline of the electron optical system. It is in effect a cathode-ray tube with an angle of scan of 5° at up to 150 kV e.h.t. but facilities for opening and closing the bulb, and mounting the workpiece as the target in place of the fluorescent screen.

A maximum beam power of 150 W is available when the beam current is 1 mA and with a spot size that gives a puncture diameter of 0·0005 inch, this may be said to represent an average power density of about 50 MW/in^2.

The filament is maintained at between -50 kV and -150 kV with respect to the target and anode which are both at 'earth' potential. This dictates the need for a bias voltage control system, since the signals to pulse the beam must originate at around earth potential. This particular machine uses a 27 MHz carrier signal to carry the bias modulation waveforms.

4. The Control System

Figure 9 shows the block diagram of the control system. On the right-hand side is the electron beam machine. The controlled parameters associated with the machine and the contents of its work chamber

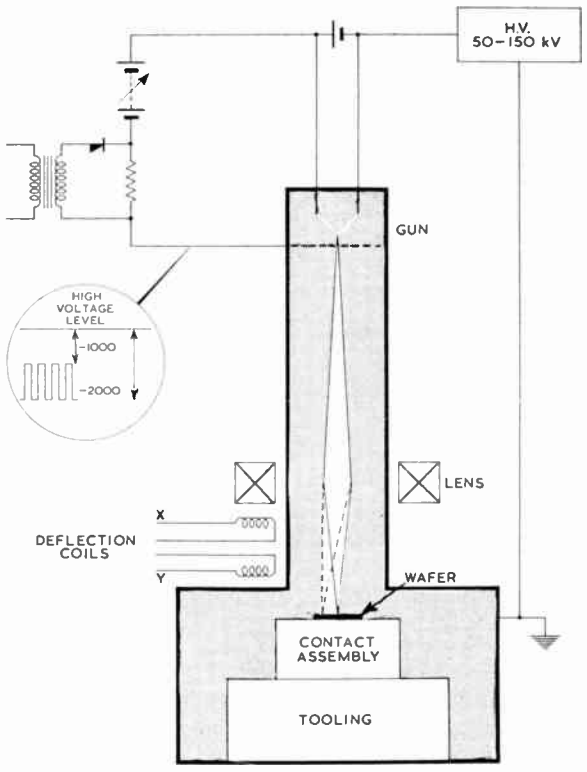

Fig. 8. Block diagram of a CW-1 and the electron optical system.

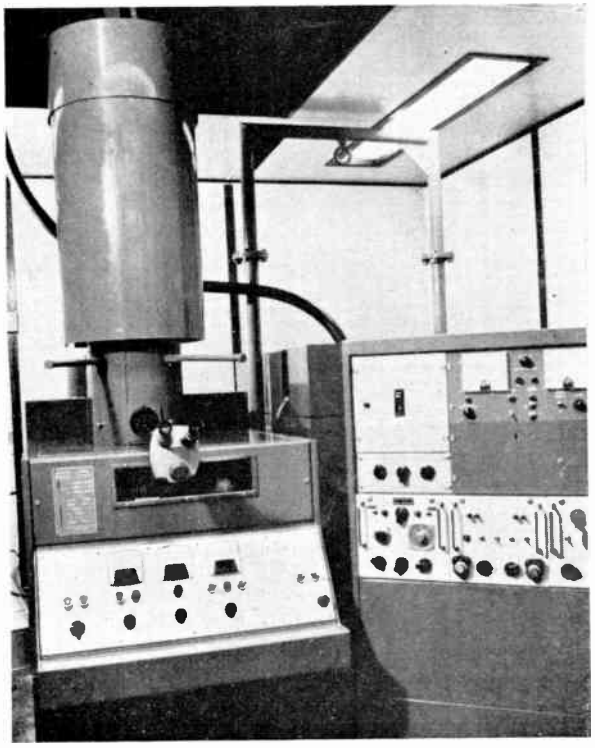

Fig. 7. CW-1 cutter-welder.

are:

(*a*) Beam deflection position,
(*b*) Beam deflection rate,
(*c*) Beam on/off gating,
(*d*) Indexing and control of weld tooling, and
(*e*) Indexing and control of scribe tooling.

The monitoring lines from the machine are simply those from tooling microswitches and those associated with the scribing process.

4.1. *The Computer*

The machine chosen was a Digital Equipment Corporation PDP8, which is a small, fast computer with a basic store of 4096 12-bit words and a cycle time of 1·5 μs. The major programmed arithmetic and logic operations are performed in or via the accumulator and there is a link bit extension to the accumulator which may be separately set or cleared. There are 5 prewired memory processing instructions, and about 40 prewired instructions which manipulate and take decisions on the contents of the single working register, comprising the accumulator and link.

In our system three highways emanate from the computer, namely,

(1) Buffered accumulator (BAC 0–11)
(2) Memory buffer (MB 3–8 and their complements)
(3) Three input/output pulse lines (IOP 1, 2 & 4)

To output an accumulator word to a peripheral device all three highways are used, the accumulator presenting the information, the memory buffer the destination code, and the input/output pulses the command to transfer the word to the device buffer register. The de-coding of the memory buffer contents takes place in device selectors which route the input/output pulses to the relevant device.

Three further highways are involved for transfer of information into the computer. These are:

Accumulator input (AC 0–11)
Skip bus (SKP)
Program interrupt bus (PI)

In order for a word to enter the computer from the accumulator input highway, the memory buffer is used to determine the source of the information in the manner just described, the input/output pulse highway carries the gating command, and the information is then read direct into the accumulator from the device.

Instruction skip, and program interrupt are initiated by driving their respective buses to ground. If a program interrupt is called up, the computer enters a subroutine which will enquire the origin of the interrupt and deal with it accordingly.

The basic input-output highways and controlled functions are shown in Fig. 9.

4.2. *The Interface*

It was decided at the outset to build a significant amount of logic into the interface, since in this type of process the computer works in relatively short bursts of continuous activity, taking decisions on the result of a previous operation and initiating the next one, then having to wait possibly in a time-wasting loop until the operation finishes. These waiting periods may occupy up to 90% of the total process time. Extensive use of the program interrupt facility enables all this 'waiting' time to be used for such purposes as:

(i) Housekeeping routines (e.g. loading a working storage block with a new set of parameters).
(ii) Type-out of information (e.g. so many off part No. ABC0001 complete).
(iii) Reading-in of more data.
(iv) Processing of data which may have been read in decimal form or even plain language before final storage as working information.
(v) Time-sharing with a completely unrelated program.

The design that was evolved is shown in block diagram form on Fig. 10. Here the device selection is shown to be in effect a three-pole multiway switch whose position is selected by a 6-bit plus complements code from the memory buffer. 'Devices' in this application range from the up-down counters used to control beam position, to bistables used to switch tooling solenoids.

Dealing first with the control of the electron beam machine itself, it is necessary to pulse-modulate the gun bias voltage with pulse widths varying from a few microseconds upwards depending on the process function being carried out.

The welding pulse widths are governed by preset monostables in the beam on/off control logic, selected by relevant input/output pulses and buffered accumulator codes, whereas the scribing pulse is produced by a separate gated clock, non-synchronous with the computer clock. This is an external pulse generator

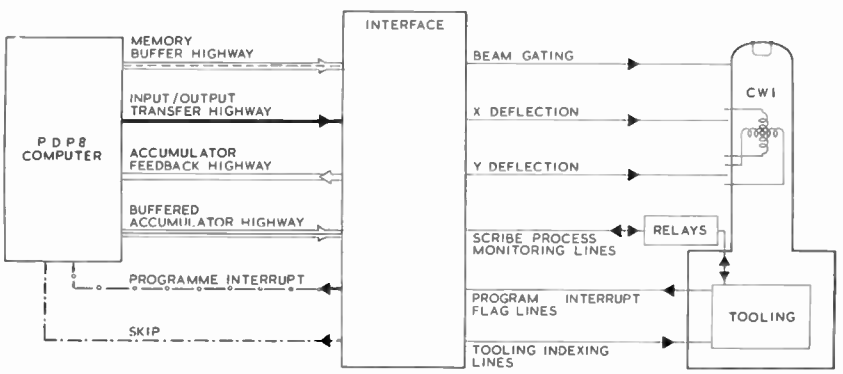

Fig. 9. Block diagram of the system.

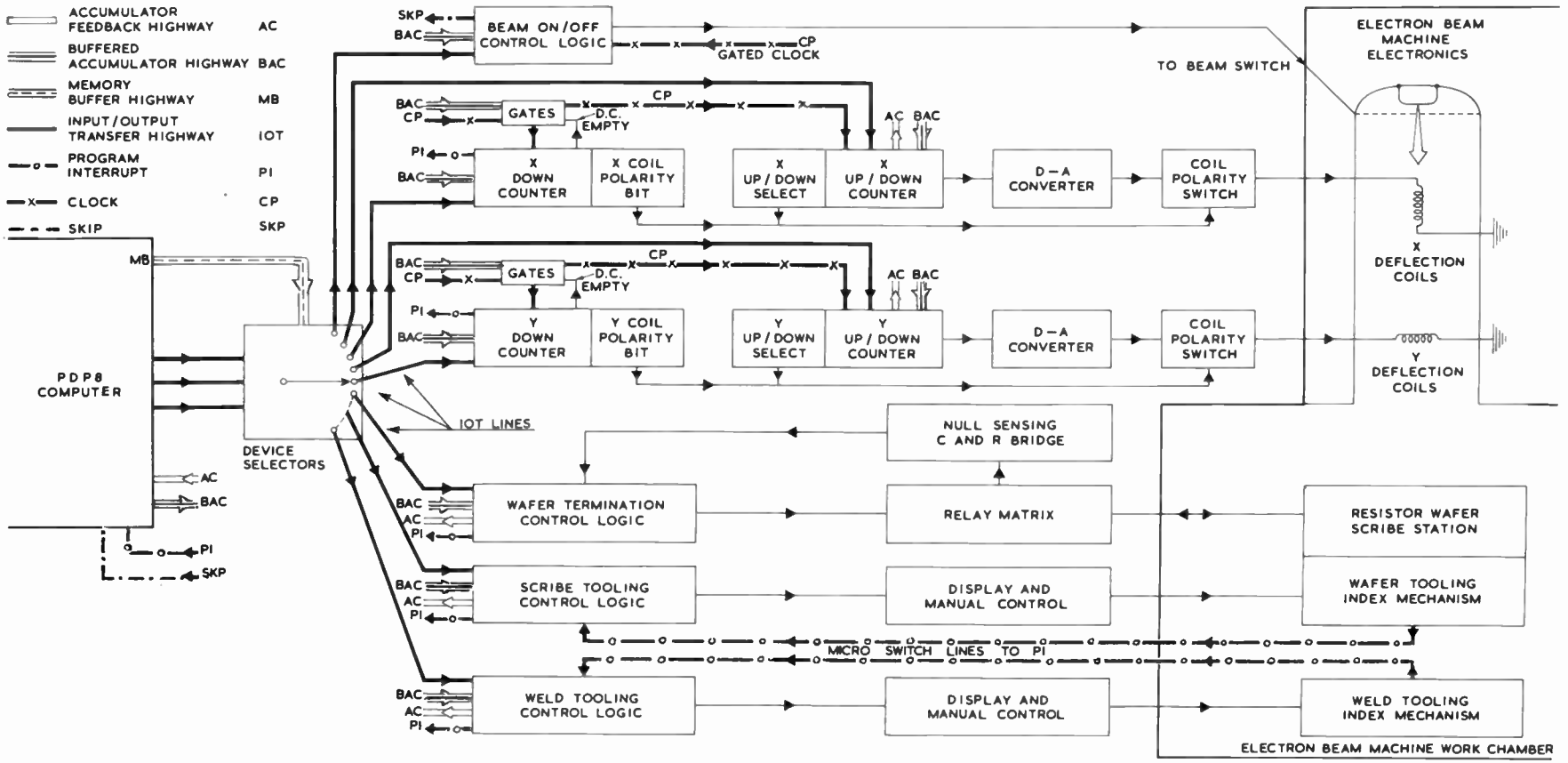

Fig. 10. Block diagram of the interface.

able to give a variable repetition rate and pulse width. The interface thus provides suitably shaped pulses to the electron beam machine's standard electronics. This external clock normally runs at a frequency considerably lower than that of the computer.

The deflection of the electron beam is achieved by driving the standard machine coils from a set of constant-current sources whose current values are determined by the states of the X and Y 10-bit up-down counters, i.e. the most significant bit of the counter turns on $\frac{1}{2}$ maximum deflection current, the next bit $\frac{1}{4}$, etc.

To use the minimum deflection and thus achieve minimum linearity error, the tooling is positioned so that the undeflected condition of the beam is such that it resides roughly over the centre of the work. Deflection is therefore required in all four quadrants, and this is achieved by including solid-state coil polarity switching in the digital-analogue converter output.

The states of the up-down counters and the coil polarity switches thus define the position of the spot in any quadrant, and this position may be preset by feeding a suitable code from the computer along the buffered accumulator output highway followed by the relevant input-output pulses. Movement of the spot is achieved by gating the external clock into the desired up-down counter. The deflection magnitudes are determined by the numbers set into the X and Y up-down counters and the direction of the spot excursion by the state of the up-down selection bit. It is then arranged that as pulses from the external clock change the condition of the up-down counters to move the spot, they simultaneously count the down counter to zero. When the down counters are empty a gate prevents further clock pulses from reaching the counters, thus halting the beam. It is clear that the rate of movement as well as the rate of beam pulsing is governed by the rate of the external clock and this is continuously variable from single step to 1 MHz by the operator. This means that each element of cut track receives the same amount of energy irrespective of pulse rate; were this not so the operator could not vary the pulse rate independently of beam current without affecting the cutting process.

The sequence of events is then, on the command 'start scribe or weld', the down counters count to zero at the external clock rate (of say 30 kHz), whilst the clock is simultaneously reading into the relevant up-down counters and pulsing the electron beam for a period determined by the setting of the external pulse generator which is variable at will by the operator. The scribing process is thus extremely flexible with all the variables independent. The interface is wired so that when an up-down counter passes through zero (i.e. X or Y deflection passes through zero axis) both the coil polarity and sign of count will change, causing the beam to continue along the same path.

The process of scribing the resistor films uses both these beam modulation and deflection facilities but introduces problems not associated with the welding aspect.

Assuming that the tooling has presented a film covered resistor wafer to the scribing station at the electron beam axis, it is first necessary to determine that all the contact fingers are making with the terminations, otherwise all measurements will be meaningless. (A test for this will of course also reject wafers with open circuit films at the same time.)

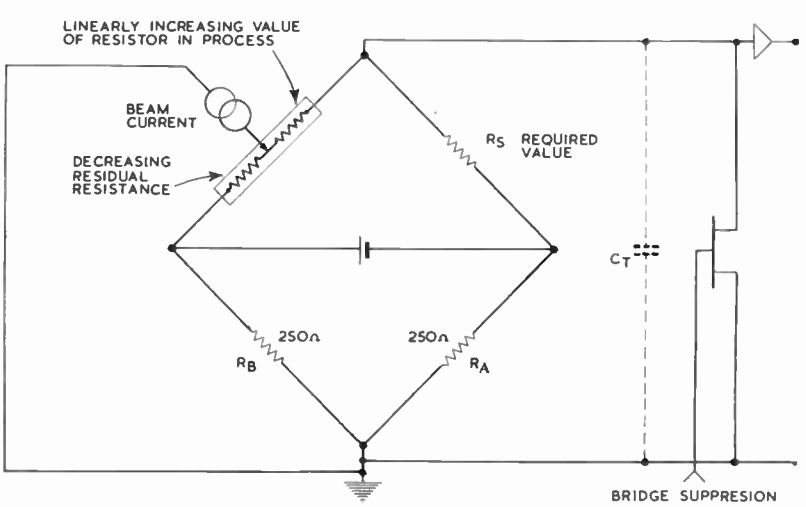

Fig. 11. The bridge circuit configuration.

The selection of the terminations for the operations already described and shown in Fig. 5 is via banks of reed switches which are selected through the interface by the computer program. During the final resistor defining period the two relevant terminals for the resistor being cut are connected to a resistance bridge.

Figure 11 shows the bridge configuration and highlights a serious problem inherent in the technique. The pulse height of the beam current is about 100 μA during scribing and this current divides, part flowing to earth through a bridge arm, and part charging the circuit stray capacitance.

Both these currents seriously limit the bridge accuracy and their effects must be reduced. This is achieved in the system not only by keeping bridge-to-earth impedance as low as possible but by short-circuiting the bridge output during the scribing pulse and for a short period following this pulse.

The bridge sensing amplifier is then allowed to normalize before a sampling pulse reads the state of an 'at balance' Schmitt trigger circuit driven from the bridge amplifier. A short sampling pulse is utilized to help eliminate the possibility of reading coincident noise pulses and three consecutive readings must be present before the computer is permitted to receive an interrupt signal. Two further Schmitt trigger circuits fed from the bridge amplifier give outputs (i) at '5% low' to reduce the scribing rate by dividing the external clock rate by 8 in the interface, and (ii) at +1% high for overvalue interrupt.

All these timing and sampling pulses are initiated by the interface beam pulser.

Tooling control is fairly straightforward and needs no further comment other than that flag signal shapers and solenoid drivers are housed in the interface and manual control is available for system fault finding, maintenance and experimental purposes. Figure 12 shows the construction of the present system.

5. System Engineering

It was recognized at the outset that serious interaction problems could arise through the interconnection of so many separate units each with its own method of earthing, some capable of drawing significant surge currents. Further, the introduction of different tooling units into the electron beam machine work chamber at different stages in the process could give a variable earth loop geometry.

Attention to overall interconnection at an early stage in design, and the use of separately generated supplies has been justified, in that spurious electrical disturbance has given very little concern. The design of the tooling has required particular care both to obviate the disastrous effects associated with sliding surfaces under vacuum, and to prevent static charge

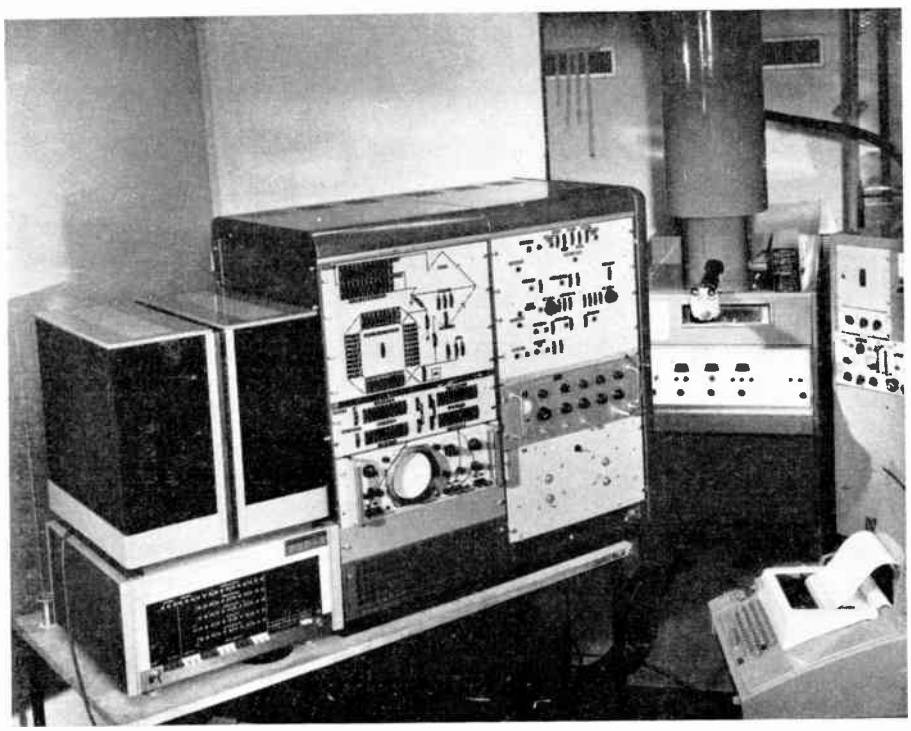

Fig. 12. The complete electron beam machining system.

on any of its parts, which could sufficiently modify the deflection pattern to allow the electron beam to ruin the tooling.

Further, since the actual weld, scribe and measurement times were so short, the demands were for rapid indexing. The tooling is still a limiting factor in this respect.

6. Programming

Having obtained a controllable machine, the apparatus with which to control it, and sufficient feedback functions to close all essential loops, one must aim at programming methods that make the most of the system.

We have endeavoured to satisfy the following requirements:

(i) Data fed into the computer must be concise but in a form easily recognizable by the operator and compiler.

(ii) Process 'setting up' must be made as near foolproof as possible by the type-out of instructions to the operator; such as 'line-up beam', 'adjust beam off-set', etc.

(iii) The program must be extremely flexible. Should the dimensional tolerances and the beam drift combine unfavourably, it may be necessary to adjust the positional relationship of the beam zero and the work in order, say, to ensure isolation between terminals on a resistor wafer, or get a spot weld on the desired place.

(iv) Communication with the computer must not interfere with the operation of the process. Type-in, read-in, print-out, etc., should all be possible concurrently with the main program. Thus the interrupt servicing routine must be prepared for anything, and be adaptable by the program or the operator to circumstances.

(v) There must be plenty of opportunity for alteration or improvement to the program. It turns out in practice that the more easy and flexible in operation a program is, the longer and more involved it gets.

(vi) For development, check-out and demonstration purposes, all processes must be capable of repetition in whole or in part at speeds varying from single step to full speed. There must be easy choice of the presence or absence of beam pulsing and tooling movement, and of whether notice is taken of process monitoring.

(vii) On completion of a successful batch or sub-batch, print-out must take place to make a record for production control and inspection purposes. Print-out should take place on detection of an error.

(viii) The program must be able to enter a 'manual' step mode, so that if there is a fault in the automatic control logic, the process can still be carried on with the computer giving typed instructions to the operator.

7. Future Developments

The control system described closes all the essential control loops in the process for which it was designed. However, as the demand rises for much faster and even more reliable operation, certain other functions need to have feed-back to the control system. These are beam current and absolute position.

7.1. *Beam Current*

It will be remembered that the bias voltage on the gun is of the order of 1000 V. Since the mutual conductance of the gun is about 10 μA per volt, either a highly accurate and stable variable supply is required, or the current must be continually adjusted for drift. Again, the beam current is very critically dependent on filament temperature which is controlled very indirectly. A sub-routine is therefore necessary whereby the beam is deflected into a current collector which is connected, say, to a go/no-go array of Schmitt trigger circuits. The output from these causes a decision to be taken which adjusts the filament current; this is the easiest method to restore the desired beam current since the alignment of the beam and its focus change with bias voltage. This loop cannot be permanently closed but a check can be made as often as required.

7.2. *Absolute Position*

There are several ways in which information about where the beam is striking can be obtained. There is the beam current itself whose path to earth can be detected, or the side effects of electron bombardment such as fluorescence, x-ray emission or secondary electron emission may be monitored. The most fruitful line to pursue appears to be the last. Secondary electron emission depends on the bombarding energy, the material bombarded, its potential with respect to its surroundings, and the nature of its surface. This phenomenon seems to give the most information, although it requires much computation for its analysis.

Secondary electron and x-ray techniques, where the emission is displayed on an oscilloscope which is scanned in synchronism with the beam, are well proved, although conversion of the information into a form suitable for positional control has not yet been attempted. But it must be obvious that with the beam 'finding' both the work (say a wire to be welded) and

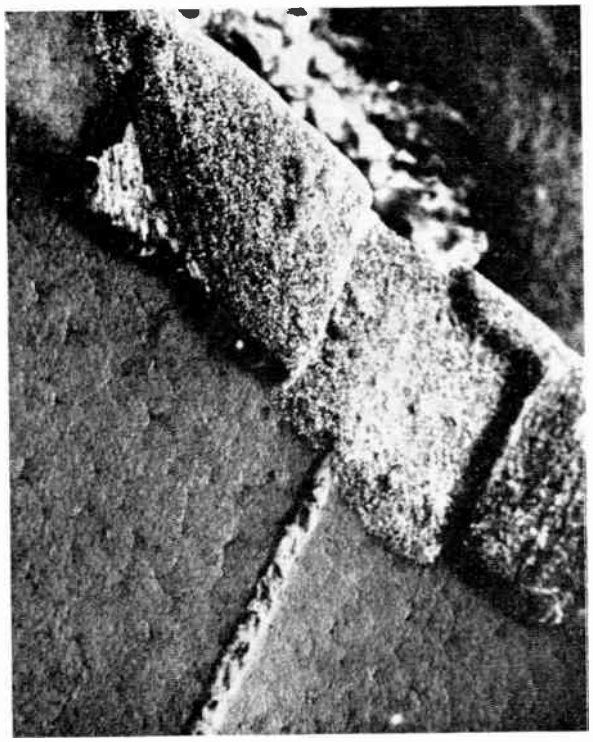

Fig. 13. Scanning microscope picture of a wafer.

the tool (a holding-down device), the control system can position these exactly with respect to one another and then form the weld on precisely the right spot. With this arrangement, mechanical movement can be faster and needs to be less intrinsically accurate and reproducible, thus reducing tooling cost, and enhancing reliability.

Figure 13 shows a scanning electron micrograph of part of a scribed resistor wafer; this demonstrates the feasibility of the technique. An x-ray micrograph would be similar and in both cases particular intensities and energy levels could be selected from the video signal.

8. Conclusion

An attempt has been made to show that on-line computer production systems need not always be very large or very costly, and that the versatility and scope for information feedback inherent in the concept avoids costly design and manufacturing effort.

It has been shown that the electron beam machine is feasible as a production tool and a number of new applications will no doubt appear. The system described can cope equally well with a 6 kW welding machine or a high resolution electron probe device.

9. Acknowledgment

Thanks are due to the Directors of Hawker Siddeley Dynamics Ltd. for permission to present this paper and to the staff of the Microelectronics Division at Hatfield for realizing the project.

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A Precision Voltage-controlled Time Delay Circuit

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Summary: A transistor circuit is described in which the time delay between a trigger pulse and the output pulse, is directly proportional to a control voltage over a 100 : 1 range.

The delay circuit is synthesized from circuits performing the functions of ramp generation, voltage comparison and switching. The circuit uses matched dual planar transistors to achieve a temperature coefficient of 0·0025% per deg C, for temperatures between 20°C and 100°C.

List of Symbols

C_R	ramp capacitor
E	ramp aiming voltage
α	transistor common-base current gain
β	transistor common-emitter current gain
I_B	transistor base current
I_{CBO}	transistor collector–base leakage current
I_{CC}	output of constant-current generator
I_E	transistor emitter current
K	Boltzmann's constant
q	charge on the electron
r_b	transistor base resistance
r_e	transistor emitter resistance
r_c	transistor collector resistance
R_b	base resistor
R_e	emitter resistor
R_o	output resistance of constant-current generator
t	time
T_k	absolute temperature
V_{BE}	base-emitter voltage of transistor
V_c	time delay control voltage
V_{CC}	supply voltage
V_{EE}	emitter–emitter saturation voltage
V_e	ramp voltage at maximum error
V_m	maximum ramp voltage
V_0	ramp voltage at zero error
V_r	ramp voltage

1. Introduction

Many electronic systems require a stable circuit which will produce a pulse delayed with respect to a trigger pulse, the time delay being voltage-controlled. Voltage-controlled time delay circuits can be formed from a linear ramp generator and an accurate voltage comparator, the delay beginning at the commencement of the ramp and terminating when the ramp voltage is equal to the control voltage.[1]

The paper describes a voltage-controlled time delay circuit with particularly good thermal stability. The availability of matched planar transistors, with good tracking of thermally-variant parameters, allows compensation techniques to be fully exploited.

2. The Basic Circuit

The block diagram of the circuit is shown in Fig. 1.

The operation of the basic circuit may be explained by considering the sequence of events during one delay period.

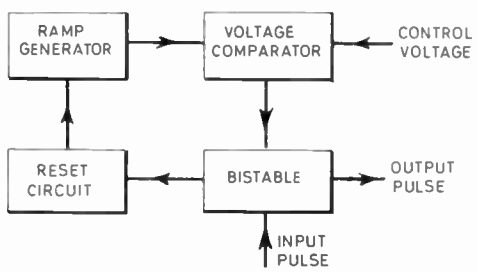

Fig. 1. Block diagram of time delay circuit.

An input pulse starts the delay period by changing the state of the bistable, which operates the reset circuit and allows the ramp to start. The ramp voltage rises until it is equal to the control voltage; the voltage comparator then produces an output which changes the state of the bistable. The bistable terminates the delay by operating the reset circuit and producing an output pulse.

The bistable is a conventional multivibrator followed by an amplifying stage. The reset circuit is a single, symmetrical alloy, transistor switch. The voltage comparator is a long-tailed pair circuit, with the addition of a further stage to give high sensitivity.

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The ramp generator is a temperature-compensated constant-current generator feeding a capacitor with one side earthed. This arrangement gives adequate linearity and good thermal stability. Where the delay is to be voltage-controlled the overall circuit is simplified if the ramp is reset to earth.

3. The Ramp Generator

The basic constant-current generator shown in Fig. 2(a) has poor stability due to the variation of V_{BE}, β and I_{CBO} with temperature.

The new constant-current generator circuit shown in Fig. 2(b) has excellent thermal stability and is used in the ramp generator.

3.1. *Ramp Stability*

Assuming the capacitor C_R has negligible leakage and change of value with temperature then the thermal stability of the ramp slope depends solely upon the stability of the constant-current generator.

In the circuit of Fig. 2(b), matched dual transistors are used to compensate for variation of transistor emitter–base voltage and leakage current with temperature.

The output of the constant-current generator (Appendix 2) is given by:

$$I_{CC} = \frac{\beta_2}{R_5(1+\beta_2)+R_4}\left[V_{CC} - V_{BE2} - \right.$$
$$- \frac{R_4\beta_1[R_2V_{CC} + R_1R_2I_{CBO1} - V_{BE1}(R_1+R_2)]}{R_3(R_1+R_2)(1+\beta_1)+R_1R_2} +$$
$$\left. + R_4(I_{CBO2} - I_{CBO1})\right] + I_{CBO2} \qquad \text{.....(1)}$$

The transistors are matched for V_{BE} and V_{BE} temperature coefficient. Differentiating I_{CC} with respect to V_{BE} and equating to zero gives the condition for stable current I_{CC}, for change of V_{BE} with temperature.

$$\frac{\delta I_{CC}}{\delta V_{BE}} = \frac{\beta_1\beta_2R_4(R_1+R_2)}{[R_3(R_1+R_2)(1+\beta_2)+R_1R_2][R_5(1+\beta_2)+R_4]}$$
$$- \frac{\beta_2}{R_5(1+\beta_2)+R_4} = 0 \qquad \text{.....(2)}$$

For matched transistors $\beta_1 = \beta_2 = \beta$. Assuming $\beta \gg 1$, eqn. (2) may be simplified to:

$$R_3 = R_4 \qquad \text{.....(3)}$$

Although the dual transistors are not matched for leakage current it is likely that the collector leakage currents will be similar. By differentiating eqn. (1) with respect to I_{CBO} the optimum circuit condition with the assumption of eqn. (3) is found to be:

$$\frac{R_1R_2}{R_1+R_2} = R_5 \qquad \text{.....(4)}$$

Substituting the relationship established by eqn. (3) the output of the constant-current generator may be determined from the approximate expression:

$$I_{CC} \simeq \frac{V_{CC}}{R_5}\left(1 - \frac{R_2}{R_1+R_2}\right) \qquad \text{.....(5)}$$

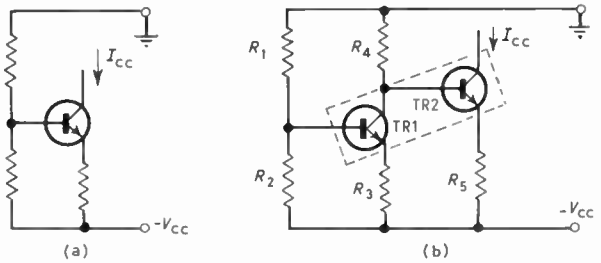

Fig. 2.
(a) Basic constant-current generator.
(b) Temperature-compensated constant-current generator.

3.2. *Ramp Linearity*

For the purpose of determining output resistance, the circuits of Figs. 3(a) and 2(b) are equivalent if R_b is made equal to R_4. The use of small signal parameters is sufficiently accurate when the practical values of the circuit components are taken into account; the values shown in Fig. 7 are typical. For more accurate work the output resistance should be measured with large signals, i.e. a collector voltage swing of V_m. The results of such a measurement are shown in Fig. 6.

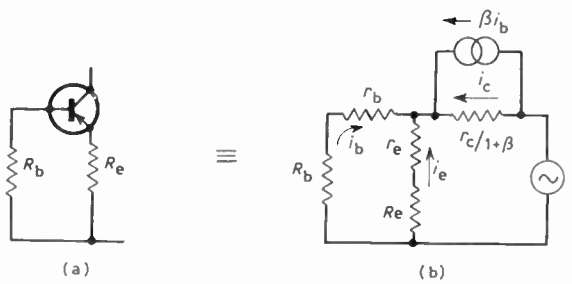

Fig. 3. Circuits for determination of output resistance.

The output resistance of the circuit of Fig. 3(a) is given by:[2]

$$R_o = \frac{R_b + r_b + \frac{r_c}{1+\beta}\left[1+\beta+\frac{R_b+r_b}{R_e+r_e}\right]}{1+(R_b+r_b)/(R_e+r_e)} \qquad \text{.....(6)}$$

The collector resistance is a function of current; a typical plot of R_o against collector current is shown

in Fig. 6. A simple equivalent circuit that can be used to determine the linearity of the voltage ramp is shown in Fig. 4. The parameter used to calculate

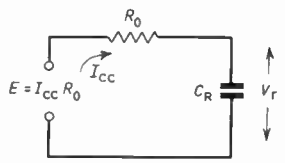

Fig. 4. Circuit for determination of ramp linearity.

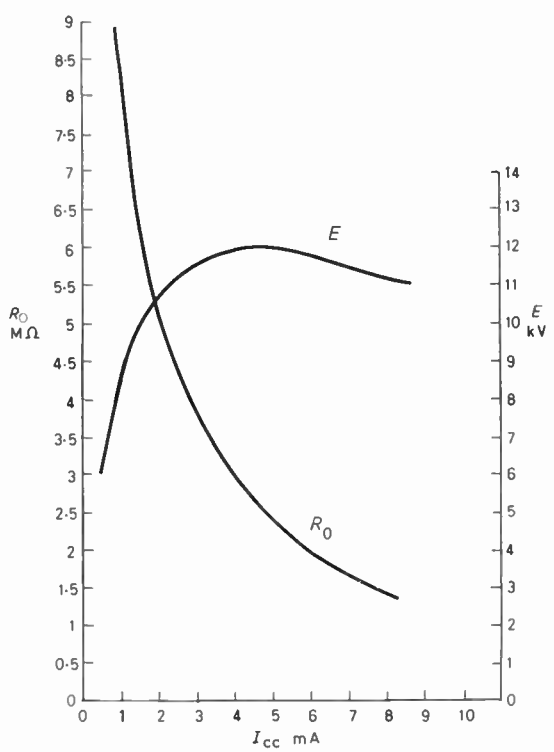

Fig. 6. Collector output resistance R_0, and aiming voltage E, where $E = I_{cc}R_0$. Transistor (half) 2N2060. Measured under large signal conditions with $R_b = R_e = 10\,k\Omega$.

ramp linearity is the effective aiming voltage E; the variation of E with collector current, for a typical circuit, is shown in Fig. 6.

For a given maximum ramp voltage V_m the departure from linearity is minimized by operating at a high value of E.

In Appendix 1 it is shown that the calculated linearity error can be reduced by choosing the time-constant R_0C_R to give a 'best fit' to the ideal ramp. Expressions are derived for the best fit exponential, for the error zero point and for the maximum linearity error. Some useful values are given in Table 1.

A further linearity error is caused by the change of transistor output capacitance C_{ob} with collector-base voltage. If the change in capacitance is ΔC_{ob} the percentage linearity error is given, for small errors, by:

$$\text{error} = \frac{\Delta C_{ob} \times 50}{C_R}\ \% \qquad \text{.....(7)}$$

4. Voltage Comparator

The voltage comparator uses matched dual transistors in the long-tailed pair configuration of Fig. 5. To maintain good ramp linearity the input current to the comparator is held constant, for changes of control voltage, by supplying the emitters from a constant-current generator.

The thermal stability of the time delay is affected by changes of base-emitter voltage and collector-base leakage current. The variation of base-emitter differential voltage is minimized by using matched dual transistors, and the effect of leakage current is reduced by operating the ramp constant-current generator at a current much greater than the comparator leakage current.

The switching sensitivity of the voltage comparator is increased by the regenerative feedback loop consisting of transistors TR2 and TR4, capacitor C_1 and resistor R_1.

Since the delay period terminates when the ramp voltage equals the control voltage the delay time may be determined by substituting V_c for V_r and $E = I_{cc}R_0$ into eqn. (14).

$$t = \frac{V_C C_R}{I_{CC}} \qquad \text{.....(8)}$$

Equation (8) neglects ramp starting delay and linearity errors.

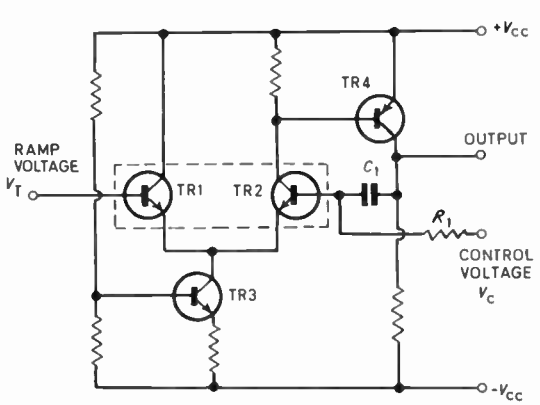

Fig. 5. Simplified voltage comparator circuit.

5. Reset Circuit

At the end of a timing period the reset circuit is operated to discharge the ramp capacitor, C_R, and return the ramp to its starting level. Ideally the reset circuit should take no current during the timing cycle, and during the reset period it should clamp the ramp capacitor to zero volts. This ideal is closely approached by using a symmetrical silicon alloy transistor as a switch.[3]

Symmetrical transistors are made with two emitters, either may be used as the collector. The low emitter-emitter saturation voltage of the symmetrical transistor is a result of the close matching of the common-emitter current gains of the transistor, irrespective of which emitter is used as the collector. The emitter-emitter saturation voltage, neglecting leakage current, is given by[4]

$$V_{EE} = \frac{KT_k}{q} \ln \frac{\alpha_1\left[1-(I_{E1}/I_B)\left(\frac{1-\alpha_2}{\alpha_2}\right)\right]}{1+(I_{E1}/I_B)(1-\alpha_1)} + \\ + r_{ev1}.I_{E1} + r_{ev2}.I_{E2} \qquad \text{.....(9)}$$

where r_{ev} is the volume resistance of the emitter region and emitter 1 is used as the collector. For a symmetrical transistor where $\beta_1 = \beta_2 = \beta$ and $\beta \gg 1$, and $I_{E1} = I_{E2} = I_E$.

$$V_{EE} \simeq \frac{KT_k}{q} \ln \left[\frac{\beta - I_E/I_B}{\beta + I_E/I_B}\right] \qquad \text{.....(10)}$$

For operation at low emitter currents the emitter resistance may be neglected.

6. Design Considerations

6.1. *Constant-current Generator*

The value of the constant current I_{CC} should be made large compared to the leakage currents into the reset circuit and the voltage comparator. The emitter currents in TR1 and TR2 (Fig. 7) should be equal, to preserve the base–emitter voltage matching. The resistors should be precision wire-wound types with low temperature coefficients. The differential temperature coefficients of the resistor pairs R_1, R_2 and R_3, R_4 is more important than the absolute temperature coefficient.

The error in using the approximate eqn. (5) for I_{cc} will give an error of less than 0·5% for $\beta \geq 40$.

In calculating the effective value of R_o due consideration should be given to the shunt effect of the voltage comparator and reset circuit.

6.2. *Reset Circuit*

The resetting transistor TR3 (Fig. 7) should be operated with equal emitter currents for a low temperature coefficient of V_{EE}, i.e. $I_B = 2I_{CC}$, giving a typical temperature coefficient of 10 μV/deg C. In the off condition the reverse base voltage should be just sufficient to reverse-bias the most positive emitter.

7. Performance

The performance was measured with the circuit and component values shown in Fig. 7

The value of I_{CC} calculated from eqn. 1 is 1·009 mA, the value calculated using the approximate eqn. (5) is 1·006 mA, and the measured value was 1·009 mA ± 0·1%. The measured temperature coefficient of I_{CC} was −0·0018% per deg C, for temperatures between 20°C and 100°C.

The calculated output resistance, for a typical r_c of 8 MΩ, is 5 MΩ. The loading of the voltage comparator and the reset circuit reduce the effective output resistance to approximately 2·5 MΩ, giving an aiming voltage of 2500 V. If V_m is limited to 5 volts

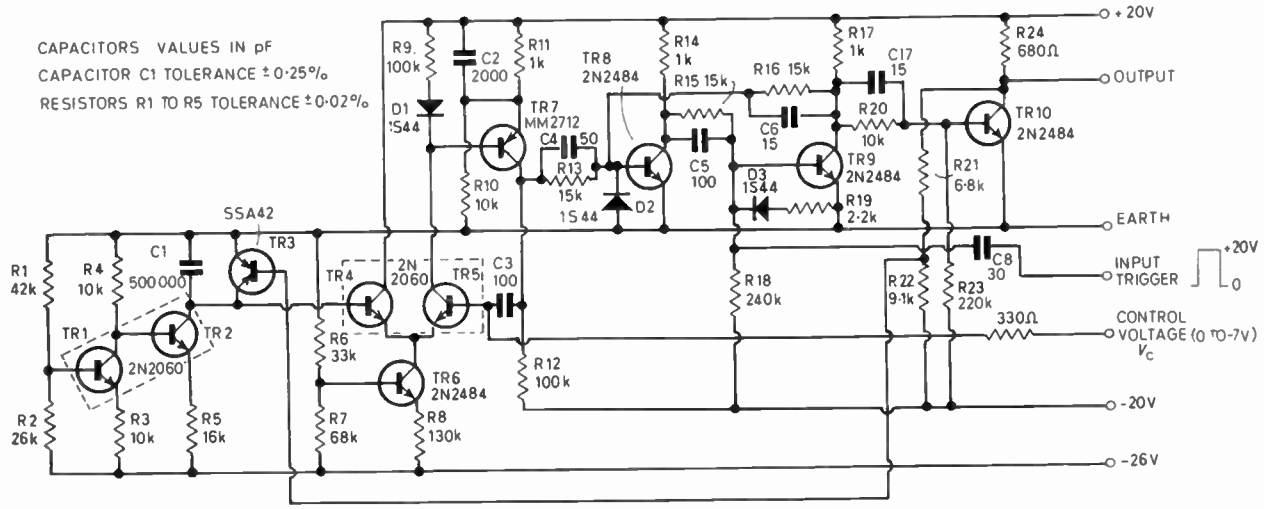

Fig. 7. Circuit diagram.

then $V_m/E = 0{\cdot}002$, and from Table 1 the linearity error is $\pm$ 0·017% of full scale. The finite switching times of the transistors will introduce further linearity errors at the commencement and termination of the ramp. The overall linearity of the time delay circuit was within the measurement resolution of $\pm$ 0·1% over a range of 100 : 1, and the circuit operated with reduced linearity over a range of 350 : 1. The slope of the *delay time to control voltage* graph was calculated to be 495·5 μs/V $\pm$ 0·35%, from eqn. (8), and the measured value was 496·7 μs/V $\pm$ 0·1%. The switching characteristics of the transistors combine to give an intercept on the V_C axis (extrapolated) of 38 mV at $t = 0$.

The symmetrical transistor used for resetting the ramp had a V_{EE} of 9·8 mV at 20°C which increased by 1·5 mV at 100°C.

The temperature coefficient of the delay time was measured for temperatures between 20°C and 100°C and was less than +0·0025% per deg C, percentage of the set delay time, the temperature error increasing linearly with temperature. The thermal drift was measured with the ramp capacitor (C_R) external to the oven, since the unpredictable change of a nominally zero temperature coefficient capacitor would mask the true drift of the circuit.

The control voltage was derived directly from the ramp generator supply voltage, the −26 V supply of Fig. 7. For this condition the change of delay with variation of the supply was 0·026% per volt.

The circuit recovery time was 7%, when set to give maximum delay, and the jitter was less than 1 part in 60 000.

8. Conclusions

A voltage-controlled time delay circuit has been described and simple design equations have been obtained.

The circuit which was built to verify the design had a linearity error less than 0·1% of full scale over a 100 : 1 delay range.

The circuit had excellent thermal stability with a temperature coefficient of delay time less than 0·0025% per deg C over the total delay range.

The time delay range could easily be changed by changing the value of the ramp capacitor C_R.

9. References

1. C. K. Friend and S. Udalov, 'Stabilized delay circuit provides high accuracy', *Electronics*, **34**, No. 15, pp. 78–80, April 1961.
2. H. C. Bertoya, 'High resistance transistor circuits', *The Radio and Electronic Engineer*, **26**, pp. 13–24, July 1963.
3. J. F. O. Evans, D. A. Gill and B. R. Moffitt, 'Symmetrical transistors as a.c. or d.c. switches and their applications in modulator and demodulator circuits', *J. Brit. Instn Radio Engrs*, **21**, pp. 143–9, February 1961.
4. J. J. Ebers and J. L. Moll, 'Large-signal behaviour of junction transistors', *Proc. Inst. Radio Engrs*, **42**, pp. 1761–71, December 1954.

10. Appendix 1

The voltage developed across the capacitor C_R, of Fig. 4, is given by:

$$V_r = E(1 - e^{-t/T_1}) \qquad \text{.....(11)}$$

where $T_1 = R_0 C_R$.

Using the exponential series

$$V \simeq E\left(\frac{t}{T_1} - \frac{t^2}{2T_1^2}\right), \qquad \text{.....(12)}$$

for $V_r \ll E$ sufficient accuracy may be obtained by terminating the series at the squared term.

Rearranging eqn. (12)

$$t = T_1\left(1 - \sqrt{1 - \frac{2V_r}{E}}\right) \qquad \text{.....(13)}$$

For an ideal voltage ramp

$$t = \frac{V_r T_2}{E} \qquad \text{.....(14)}$$

where T_2 is the ramp time-constant.

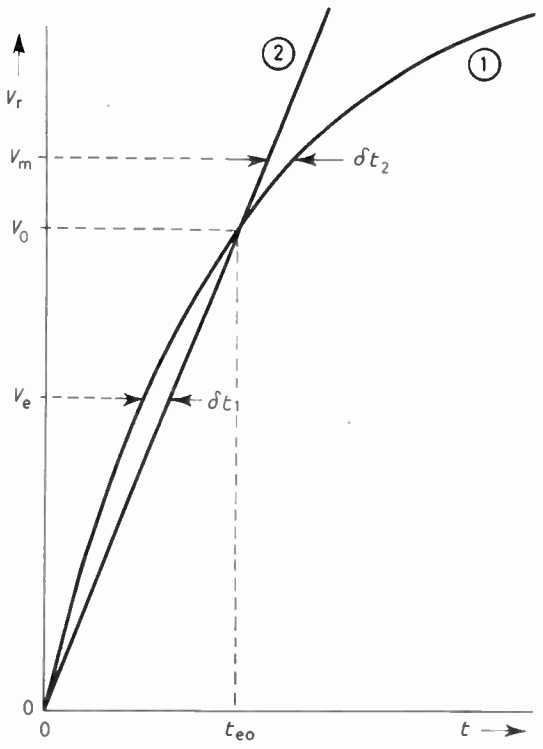

Fig. 8. Ramp linearity.

(1) Approximate, exponential, $E\left(\frac{t}{T_1} - \frac{t^2}{2T_1^2}\right)$

(2) Ideal ramp, Et/T_2.

Table 1

Ramp parameters

V_m/E	T_1/T_2	V_0/E	Percentage error
0·0005	0·9998	0·0004	±0·004
0·001	0·9996	0·0008	±0·008
0·002	0·9992	0·0016	±0·017
0·005	0·9979	0·0041	±0·043
0·010	0·9958	0·0083	±0·087
0·020	0·9916	0·0166	±0·175
0·050	0·9787	0·0416	±0·455
0·100	0·9563	0·0836	±0·969

To minimize the *calculated* linearity error it is desirable to have a method of determining a 'best fit' of the actual exponential to the ideal ramp, as shown in Fig. 8.

For a ramp which is terminated at V_m a 'best fit' is obtained when $\delta t_1 = \delta t_2$.

Now

$$\delta t_1 = \frac{V_e T_2}{E} - T_1\left(1-\sqrt{1-\frac{2V_e}{E}}\right) \qquad \text{.....(15)}$$

By differentiating eqn. (15) with respect to V_e and equating to zero, the value of V_e for a maximum value of δt_1 is found, i.e.

$$V_e = \frac{E}{2}(1-T^2) \qquad \text{.....(16)}$$

where

$$T = \frac{T_1}{T_2}$$

Substituting eqn. (16) into eqn. (15) gives

$$\delta t_1 = \frac{T_2}{2}(1-T^2) - T_1(1-T) \qquad \text{.....(17)}$$

Similarly

$$\delta t_2 = T_1\left[1-\sqrt{1-\frac{2V_m}{E}}\right] - \frac{V_m T_2}{E} \qquad \text{.....(18)}$$

Putting $\delta t_1 = \delta t_2$

$$T = 2-\sqrt{1-\frac{2V_m}{E}} - 2\sqrt{1-\frac{V_m}{E}-\sqrt{1-\frac{2V_m}{E}}} \qquad \text{.....(19)}$$

The error zero voltage V_0 is found by equating (13) and (14):

$$V_0 = 2ET(1-T) \qquad \text{.....(20)}$$

The error zero voltage is useful where some adjustment of capacitor C_R is possible, i.e. V_r is set to V_0 and the required value of t is given by:

$$t_{eo} = \frac{V_0 T_2}{E} \simeq \frac{V_0 C_R}{I_{CC}} \qquad \text{.....(21)}$$

The maximum value of the time error between the ideal ramp and the actual exponential is given by:

$$t_e = T_2\left[\frac{V_e}{E} - T\ln\left(\frac{E}{E-V_e}\right)\right] \qquad \text{.....(22)}$$

Table 1 contains a range of normalized parameters, which should be useful for any ramp generator.

11. Appendix 2

Derivation of Equation for Output of Compensated Current Generator

Consider the emitter current of transistor TR1, in Fig. 9.

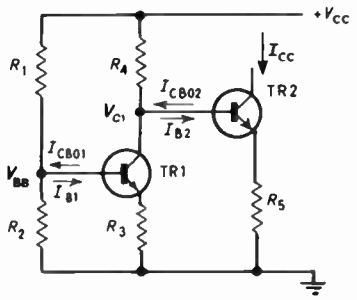

Fig. 9. Compensated constant current generator.

$$I_{E1} = \frac{V_{BB}-V_{BE1}}{R_3} \qquad \text{.....(23)}$$

where

$$V_{BB} = \frac{R_2}{R_1+R_3}\{V_{CC}-R_1[I_{B1}-I_{CBO1}]-V_{BE1}\} \qquad \text{.....(24)}$$

Making the usual substitutions, one obtains

$$I_{C1} = \frac{\beta_1[R_2V_{CC}+R_1R_2I_{CBO1}-V_{BE1}(R_1+R_2)]}{R_3(R_1+R_2)(1+\beta_1)+R_1R_2} + \\ + I_{CBO1} \qquad \text{.....(25)}$$

and similarly,

$$I_{E2} = \frac{V_{C1}-V_{BE2}}{R_5} \qquad \text{.....(26)}$$

$$I_{CC} = \frac{\beta_2}{R_5(1+\beta_2)+R_4}\Bigg\{V_{CC}-V_{BE2}- \\ -\frac{R_4\beta_1[R_2V_{CC}+R_1R_2I_{CBO1}-V_{BE1}(R_1+R_2)]}{R_3(R_1+R_2)(1+\beta_1)+R_1R_2} + \\ +R_4(I_{CBO2}-I_{CBO1})\Bigg\}+I_{CBO2} \qquad \text{.....(27)}$$

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The *UK-3* Satellite and its Ground Check-out Equipment

By

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Presented at an Institution meeting held in London on 27th April 1966.

Summary: An outline of the electrical design of the *UK-3* satellite is followed by a statement of the philosophy governing the design of the ground check-out equipment. The principal functions of the latter are described under the general headings of:

(1) Test equipment for use close to the satellite.

(2) The trailer-mounted data processing and recording station.

Among the units specially developed for *UK-3*, and described, are a 365-day clock and commutator unit employing integrated circuits, and a self-checking off-limit detector.

1. The *UK-3* Satellite

UK-3 is the third in the series of Anglo-American co-operative satellites and the first to be wholly designed and manufactured in Britain. It is scheduled to be launched from the Western Test Range in California from a *Scout* rocket early in 1967. Its orbit will be circular and near-polar at a height of 550 km approximately. Five scientific experiments are carried.

The satellite structure and the ground check-out equipment are designed and manufactured by the British Aircraft Corporation, Guided Weapons Division, under the Design Authority of the Royal Aircraft Establishment, Farnborough. The satellite power supplies, data handling and telemetry systems are likewise dealt with by the General Electric Company (Applied Electronics Laboratories). The reception and data processing of signals from the satellite in orbit will be the responsibility of the U.S. National Aeronautics and Space Administration.

1.1. *Experiments*

The scientific experiments (Fig. 1) carried by the satellite are as follows:

1. Birmingham University (Department of Electron Physics)—Measurement of electron temperature and concentration in the ionosphere above F2 maximum.
2. Manchester University (Jodrell Bank)—Reception of galactic noise in the band 2–5 MHz.
3. Sheffield University (Department of Physics)—Study of propagation of very-low-frequency signals in the band 3–16 kHz.
4. Radio and Space Research Station (R.S.R.S.)—Measurement of naturally occurring terrestrial noise in the band 5–15 MHz.
5. Meteorological Office—Measurement of the density of molecular oxygen in the upper atmosphere.

It will be seen that experiments 2, 3 and 4 embody radio receivers working from loop aerials. Overall testing is therefore performed by coupling signals at the appropriate frequency into the loop. Items 1 and 5 require special-purpose simulation equipment.

The satellite encoders pass control pulses to the experiments so that their operation may be synchronized with that of the data handling system.

The construction of the satellite is profoundly influenced by the requirements of certain of the experiments. For example, Jodrell Bank need a loop aerial aperture of at least 1 square metre. The satellite must therefore carry some structure to enable the

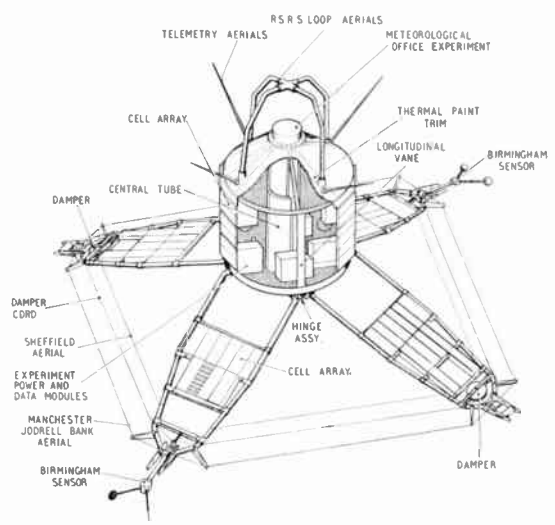


Fig. 1. *UK-3* satellite with experiment sensors.

† British Aircraft Corporation, Stevenage, Hertfordshire.

loop to be folded away in the rocket nose cone during launch and later deployed in orbit. This is achieved by hinging four booms to the body, with the loop strung around their tips. They erect under the action of centrifugal forces while injection into orbit takes place.

Birmingham University require adequate separation between the electron temperature and density probes and the satellite body so that the electron distribution in the vicinity of the probes is not disturbed. The Birmingham sensors are therefore mounted on opposite boom tips. It is necessary to expose a projected area of satellite of at least 2500 cm^2 in order to collect positive ions from the local plasma. For this reason, most of the outside surfaces have to be plated with gold to ensure an oxide-free conducting finish.

R.S.R.S. and Sheffield University would prefer their aerial systems to be maintained in a relatively constant attitude for reasonable periods of measurement. The Meteorological Office wish their sensor look-out angle to the sun to remain fairly stable. This imposes a stability requirement which is met by spinning the satellite about its longitudinal axis at an initial rate of approximately 30 rev/min.

Several experimenters need to know the attitude of the satellite as it precesses slowly under the influence of aerodynamic and geomagnetic forces. Attitude sensors are fitted to determine the angle of the sun with respect to the satellite spin-axis. These have a look-out angle of about 115° and comprise stacks of photo-sensitive cells giving an angular measurement to within approximately 3°.

Fuller discussions of these topics have been given elsewhere.[1,2]

1.2. *Solar Cell Arrays*

The control and distribution of power within the satellite is covered in a companion paper.[3] The characteristics of, and measurement techniques for, the solar cell power sources have also been described.[4]

The following method was employed to determine the number of solar cells to be fixed to the booms (both sides) and to the body in two equal electrical arrays which supply the load and charge the battery. First, the voltage and current requirements for the equipment load were found and allowance made for losses in converters and regulators. The charging requirements of the battery for typical orbits were likewise determined. A basic cell tray comprising 40 or 48 cells in five or six parallel 'strings' of eight series-connected cells was found to give the best compromise between reliability and lightness. An allowance was made for radiation damage which reduces output power. The power output is now dependent on the angle of incident illumination and on the area of the array unshadowed. Shadowing was determined by photographing a scale model of *UK-3* from many different angles. A computer analysis was performed to predict the power available for any satellite attitude. This enabled the boom geometry to be decided and the number of cells finalized at nearly 7400. These give an output of between 15 V and 30 V at around 500 mW per array.

1.3. *Thermal Balance*

The thermal control technique for *UK-3* employs paint patterns to control the emissivity and absorptivity of the outside surfaces. It is calculated[5] that the temperature of installed equipment can be controlled within a range of about 0°C to 40°C. Proof of this estimate was obtained when the satellite was tested in the thermal vacuum chamber at the Royal Aircraft Establishment, Farnborough.

1.4. *Magnetic Moment*

The interaction of the earth's magnetic field with the combined magnetic moment of the satellite will cause the satellite to experience torques leading to unwanted changes of attitude.[6] The use of magnetic materials in construction has been avoided as far as possible, and care has been taken to prevent circulating currents from flowing by insulating sections of the structure from the rest.

Such techniques are not always compatible with electrostatic and magnetic screening requirements and there has been a recent tendency for the magnetic moment to increase. Special equipment has been constructed by the Royal Aircraft Establishment to enable accurate measurements to be made on complete satellites.

1.5. *Interconnections*

To standardize manufacture, to simplify the task of integrating installed equipment on an extended time-scale, and to allow for the quick replacement of faulty sub-units, it was decided to make all electrical interconnections by means of a single cable-form with plug/socket terminations (Fig. 2). Most of the materials (e.g. insulated wire and connectors) are purchased from the U.S.A. from types which have been certified by N.A.S.A. for space use.

The wires are crimped to the connector pins; a high degree of redundancy is employed in both wires and pins. Shrinkable plastic sleeves are used to protect the cable/connector joints, and to give them mechanical strength.

1.6. *Power Supply and Telemetry Systems*

These are described in the companion paper.[3]

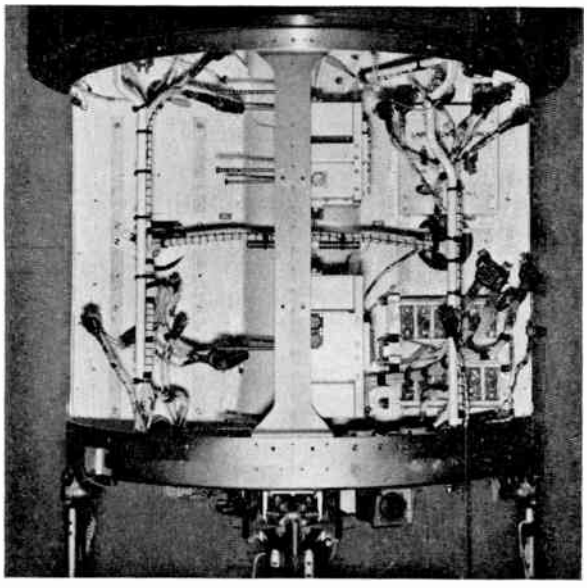


Fig. 2. Satellite cableform.

2. Principal Functions of Ground Check-out Equipment

The functions of the ground equipment may be summarized as follows:

(1) Supply of external power to satellite, including battery charging facilities.

(2) Provision of facilities to enable satellite sub-systems to be controlled and tested, and the simulation of ground commands.

(3) Monitoring and recording of satellite outputs. This includes the reception and processing of signals received by telemetry r.f. link as well as via a direct link; and the selection of individual channels for measurement and data storage.

(4) Generation of N.A.S.A. 365-day standard time code for insertion into printed records.

(5) Display of direct and recorded data in a variety of forms.

(6) Provision of equipments for testing sub-systems separated from the satellite and for general purpose testing.

2.1. *Ground Check-out Philosophy*

The configuration and content of the equipment has been based largely on the experience gained by the Americans in testing and firing the *UK-2* satellite, which was successfully launched into orbit in 1964. It will be realized that the ground equipment has to provide a service for satellites undergoing environmental and other tests at various locations before being taken to the launching range. In the case of *UK-3*, these tests include trials of the satellite structure and mechanics under simulated launch conditions, extended thermal vacuum chamber trials to simulate the orbital environment, radio frequency interference checks and compatibility tests of each item of installed satellite equipment with respect to the others.

The more important design requirements for the *UK-3* check-out equipment were:

(*a*) *Rapid Access to Data*

Tests should be applied and the results read out from a number of diagnostic points in a readily understandable form. This 'quick look' capacity enables the testing staff to take immediate decisions while tests are in progress and is obviously an important factor in reducing delays both during the test phase and final count-down.

(*b*) *Closeness to Satellite*

Small groups of control and monitoring equipment should be arranged to accompany the satellite as it moves to the various test areas. The equipment, in the form of mobile racks, should be sufficiently flexible to meet the requirements of different trials. Furthermore, it is found to be of great benefit at the launching site to have equipment which can give an immediate indication of the condition of the satellite under the direct eye of the block-house controller near the launch tower. More comprehensive test gear cannot usually be accommodated at a distance of less than one mile from the launch pad.

(*c*) *Simplicity*

Efforts should be made on grounds of reliability and reduction of crosstalk to use the minimum number of connections to the satellite.

(*d*) *Information Storage*

The check-out equipment should be capable of recording the signals received from the satellite in a number of ways. A history can thus be compiled and later used for comparison with current performance. The benefits of this during a programme lasting several years are obvious.

(*e*) *Spare Equipment*

Duplication of all equipment is needed, both to enable faulty units to be replaced at once, and to meet the programme requirement for trials to be carried out simultaneously at different establishments.

2.2. *Equipment Complex*

The realization of the above principles results in the provision of two complete sets of ground check-

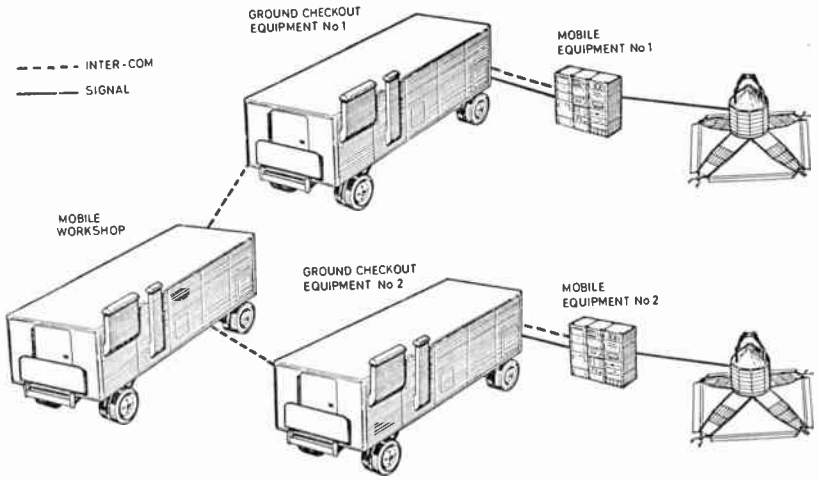


Fig. 3. *UK-3* ground equipment complex.

out equipment. Each consists of a comprehensive data processing and recording station mounted in a trailer, and a mobile satellite check-out control station. The trailers also carry instruments to enable the individual experiments to be tested, together with a selection of standard electronic test gear.

Intercommunication facilities are provided between all vehicles and equipment in the form of loudspeakers and hand microphones. A single workshop trailer has also been fitted out to enable limited repairs to be performed at short notice.

It may be of interest to note that the trailers were acquired at a nominal price from the Royal Air Force *Thor* Stations after the weapons were withdrawn from service. Most of the original equipment has been taken out and replaced with *UK-3* check-out and data recording equipment. The air-conditioning systems are being supplemented with cooling units to improve working conditions while in the U.S.A. The complex is shown diagrammatically in Fig. 3.

3. Mobile Check-out and Control Equipment

The mobile check-out equipment is designed to operate close to the satellite and to be easily portable so that it may be set up in any area where a satellite is undergoing test. Its principal functions are as follows:

(1) Supply of external power to the satellite to enable equipment to be operated and batteries to be recharged. Monitoring of current and voltage inputs.

(2) Control of certain data handling functions in the satellite.

(3) Simulation of ground commands by r.f. link.

(4) The injection of test signals, the calibration of sub-systems and the monitoring and recording of direct outputs.

(5) The reception, decommutation and display of selected telemetry channels.

The equipment is housed in three 19-in racks (Fig. 4). Individual units and instruments may be removed and remounted in, for example, the block-

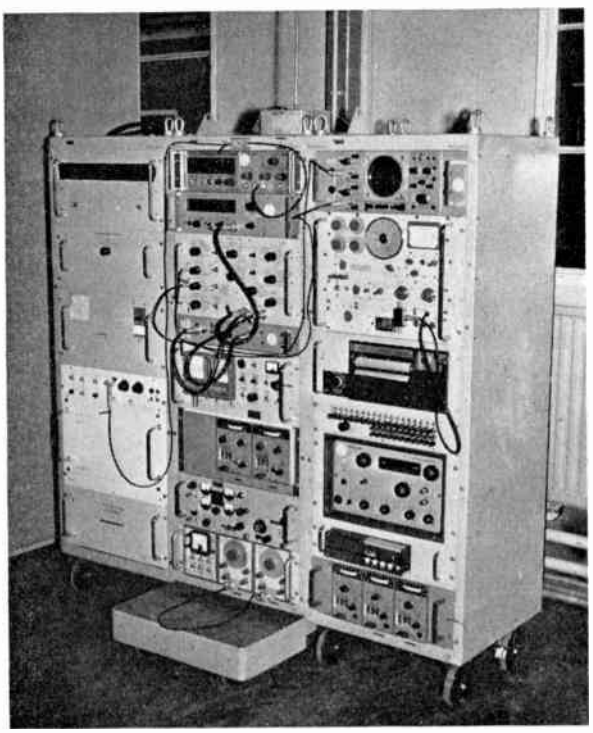


Fig. 4. Mobile check-out station.

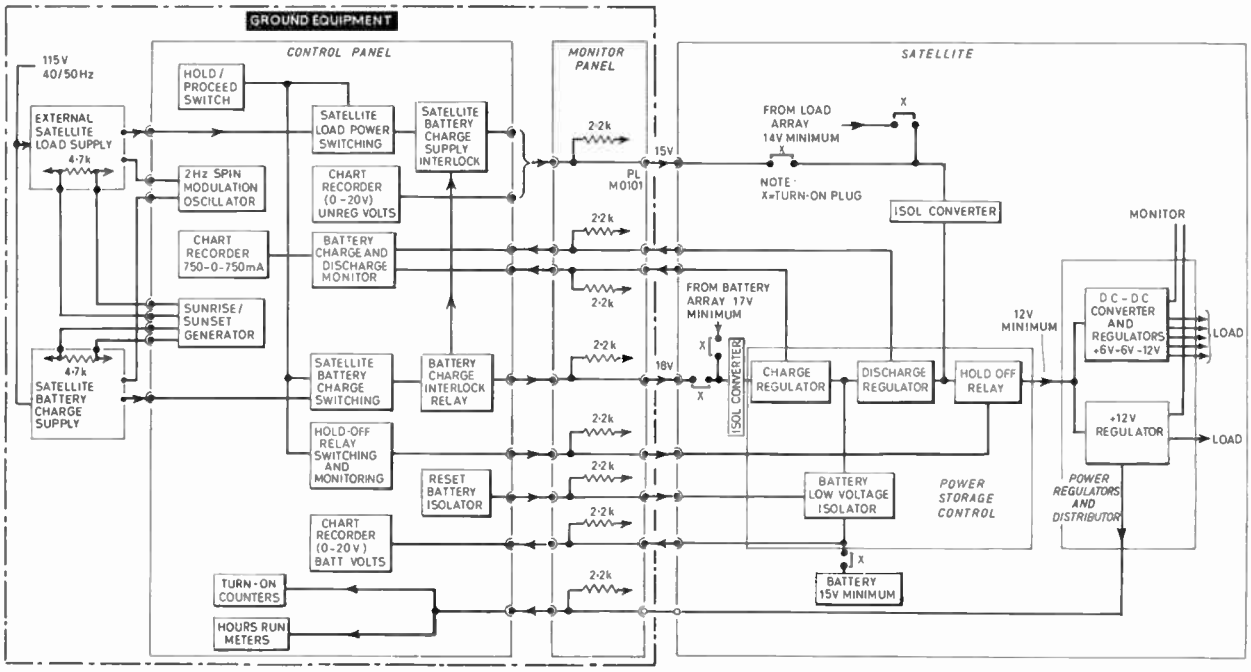


Fig. 5. Block schematic of the external power supply to satellite.

house console at the range. For long-distance transit the three racks and their equipment are stowed in the trailer.

The design philosophy has been to use proprietary British test equipment where possible. Where this was not possible, design and manufacture has generally been undertaken in the U.K. either by B.A.C. or its sub-contractors. It has not, however, proved economical to do this in every case, and a number of important instruments have been purchased from the U.S.A.

3.1. *External Power Supply to Satellite*

A block diagram is shown in Fig. 5.

The variable-voltage, variable-current power units simulating the battery and load arrays are switched from a control panel and their outputs are routed through a monitor panel into which suitable recording instruments may be patched. From here power is fed through the umbilical cable to the satellite. A battery charge interlock in the control panel ensures that the 18V charging supply is always present before application of the 15V load external supply. If it were not the reverse voltage across the discharge regulator might damage its power transistors.

The HOLD/PROCEED switch is used to cut off both external supplies from the satellite. In the HOLD position it also energizes a hold-off relay. This additional safeguard disconnects the satellite loads from the power storage control system. Thus by switching to HOLD all active sources are isolated and the satellite battery prevented from discharging.

A further safeguard is the provision on the satellite of a turn-on plug. This may be removed manually while working on the satellite; it disconnects all satellite sub-systems from sources of supply.

The sunrise/sunset generator simulates the transfer of power in orbit between battery and solar cell supplies. It applies ramp voltages to the current limiting circuits of the two external supply units so as to bring one into operation while the other is gradually inhibited.

The power ripple caused by the spin of the satellite is simulated by the 2 Hz spin modulation oscillator which superimposes a voltage of up to 10V peak-to-peak on the external supplies.

The monitoring and recording functions will be clear from the block diagram.

3.2. *Satellite Control and Experiment Test*

A 250 mW command transmitter is provided in the mobile ground equipment to initiate satellite tape recorder playback and to transfer the recording of low-speed data from Mode 1 to Mode 2. The transmitter is modulated by address and execute audio frequency tones in a simple code and radiates in the 140–150 MHz band. Alternatively, the r.f. signal may be fed to the satellite by coaxial cable.

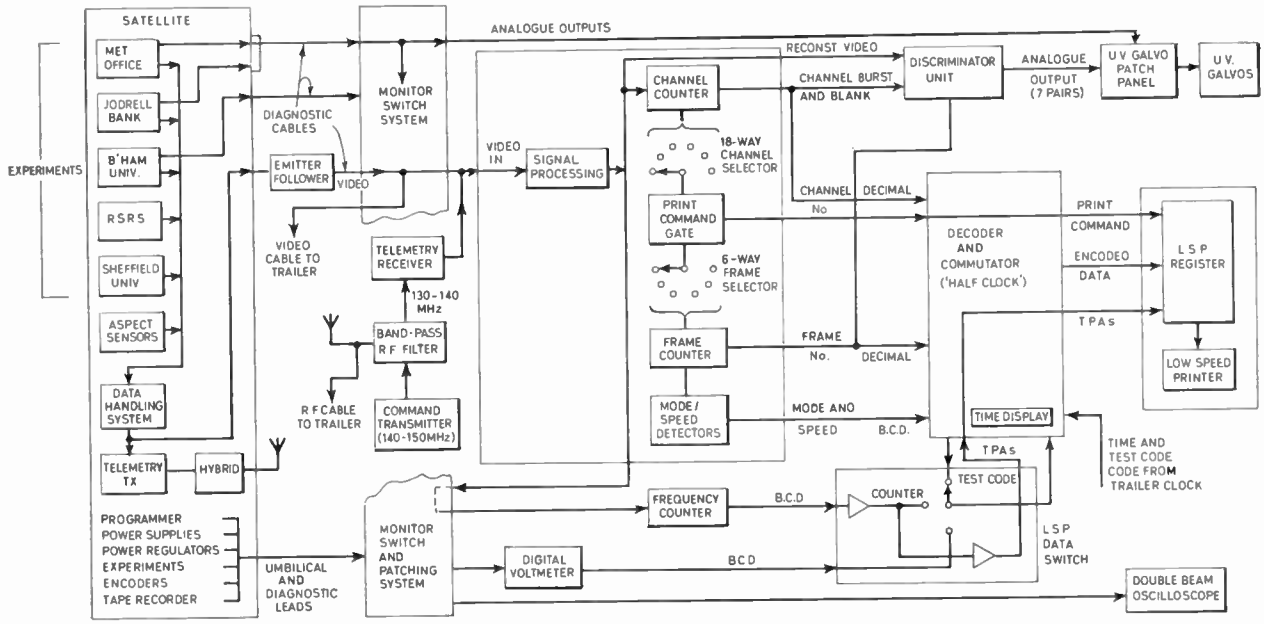


Fig. 6. Block schematic of the data extraction in mobile check-out equipment.

The tape recorder may also be commanded to replay by means of a direct voltage generated in the control panel and fed by direct link to the satellite programmer. A two-minute gate controls the replay time.

The check-out equipment includes a variety of stimulation sources for calibrating and testing individual satellite experiments and sub-systems. Among these are r.f. and a.f. general-purpose signal generators and a tape recorder. The latter is intended to provide a v.l.f. signal programme to the Sheffield experiment. Stimulation is applied to the satellite via three multi-core diagnostic cables and the direct outputs from sub-systems are brought back along the same cables. Distribution in the check-out equipment takes place in the monitor panel where selector switches enable connections to be made to the various items of display equipment described in Section 4. It should be noted that the diagnostic cables cannot be used when the satellite is installed in the launching rocket. The umbilical cable which carries external power and a small selection of satellite monitors is the only line connection under these circumstances.

3.3. *Data Extraction and Display*

The signals emanating from the satellite may be grouped as follows:

(1) Analogue voltages representing telemetry inputs.

(2) Actual voltages and frequencies at measurement sites.

(3) The composite video signal.

The signal sources in the satellite and the processing arrangements in the ground check-out equipment are shown in Fig. 6.

3.4. *Analogue Voltage Recording*

The outputs of certain experiments in the range 0–5 volts d.c. are fed via the diagnostic cables to the monitor panel. From there they may be patched to an 18-channel ultra-violet recording galvanometer of U.S. manufacture. This instrument provides an accurate 'quick-look' facility and a record of experiment performance but its time-marker trace is not linked to the telemetry system.

3.5. *Real Voltage and Frequency Recording*

The measurement and recording of real voltages and frequencies is performed by a digital voltmeter, in conjunction with an a.c. converter, a counter and a numeric printer known as the low-speed printer (l.s.p.). Signals are distributed from the monitor panel either by switches or by jumpers so that any satellite quantity may be recorded on the appropriate instrument.

The digital voltmeter has a four-digit measurement capability. It provides a front-panel decimal display as well as a digital output in 1248 binary-coded-decimal (b.c.d.) form. The frequency counter, which has an 8-digit capability, provides a similarly coded output and display.

The low-speed printer data switch selects one output or the other, or a test code, for printing out.

The signal is routed to the low-speed commutator in the unit known as the 'half-clock' and thence to a proprietary paper tape register and printer. Further details of this process are given in the next section.

4. Reception and Selection of Telemetry Data

The satellite telemetry output in the 130–140 MHz band is demodulated by the telemetry receiver and the video signal passed to the decommutator. A low-pass r.f. filter prevents the 140–150 MHz signal from the command transmitter from reaching the receiver and enables a common receiving/transmitting aerial to be used.

A direct video signal from the satellite data handling system may also be fed to the decommutator via on-line emitter followers in the diagnostic cables and through the monitor panel. From the latter a video connection is made to the trailer equipment for recording on magnetic tape or for high speed print-out. The magnetically recorded signal in the trailer may also be fed to the decommutator.

A feature not shown on the block diagram is the possibility of building up a synthetic telemetry signal for testing the receiver. This is done by taking the satellite data handling system video output to a standard signal generator in the mobile ground equipment where a phase-modulated v.h.f. signal may be produced.

4.1. *Decommutation*

The incoming pulsed frequency modulation (p.f.m.) signal may have suffered degradation during transmission and reception. It is therefore first passed through amplifying, limiting and signal conditioning stages in the decommutator to form a reconstituted signal whose envelope is used for gating purposes.

The p.f.m. signal format may have been derived from either the satellite high-speed real-time transmission or from the low-speed recorded data, the latter being in one of two alternative modes. The decommutator identifies the low-speed signal by the presence of a 15·7 kHz reference frequency inserted in the blank intervals between bursts. One channel in the low-speed format also carries an identification frequency to enable the decommutator to recognize the mode.

Solid-state counters and diode matrices connected to selector switches on the front panel enable any channel of any frame to be gated out for printing or display. The necessary command to the low-speed printer to commence printing at the correct point in the complex format is also generated in the decommutator. The following outputs are provided:

(1) P.f.m. bursts for all channels to discriminators.

(2) The channel number and frame number in decimal form and the speed and mode in b.c.d. form for acceptance by the low-speed printer.

(3) Processed video to the frequency counter.

4.2. *Discriminators*

Seven frequency discriminators are associated with the decommutator. These are individually patched into selected channels at the decommutator unit. Gating signals allow each discriminator to select one channel for a given frame or alternatively the same channel for all frames.

The discriminators convert the incoming burst frequencies into voltages proportional to the applied frequency. These levels are held for just less than one frame period, after which the output resets to zero level in readiness for the next burst. The discriminator analogue outputs are routed to the ultra-violet oscillograph for recording.

4.3. *Frequency Counter*

This high-speed counter accepts the reconstituted p.f.m. signal from the decommutator. It times the duration of ten consecutive cycles from each channel burst, the reset occurring during each intervening blank period. Thus the incoming data frequencies in the range 5–15 kHz appear as counts between 660 and 2200 ms. These data are displayed visually and the state of each decade of the display is encoded to 1248 b.c.d. form and passed via the l.s.p. data switch amplifier and half-clock to the low-speed printer.

4.4. *Low-speed Printer Data Switch*

The functions of this unit have been referred to above. It is worth noting, however, that the assembly houses 52 buffer amplifiers which amplify and limit the b.c.d. outputs from the counters. Each amplifier consists of two d.c.-coupled transistor stages with saturation characteristics which give the necessary degree of limiting.

4.5. *Half Clock*

This unit processes the data into a suitable form for driving the low-speed printer. Its decoding and decommutating functions are duplicated in the 'full-clock' in the trailer-born station which also generates the timing code.

It will therefore be convenient to describe the unit in the section dealing with the trailer (Section 5).

4.6. *Low-speed Printer and Register*

This proprietary electro-mechanical paper tape printer provides a fourteen-column print-out at a maximum rate of 15 lines per second. It finds its

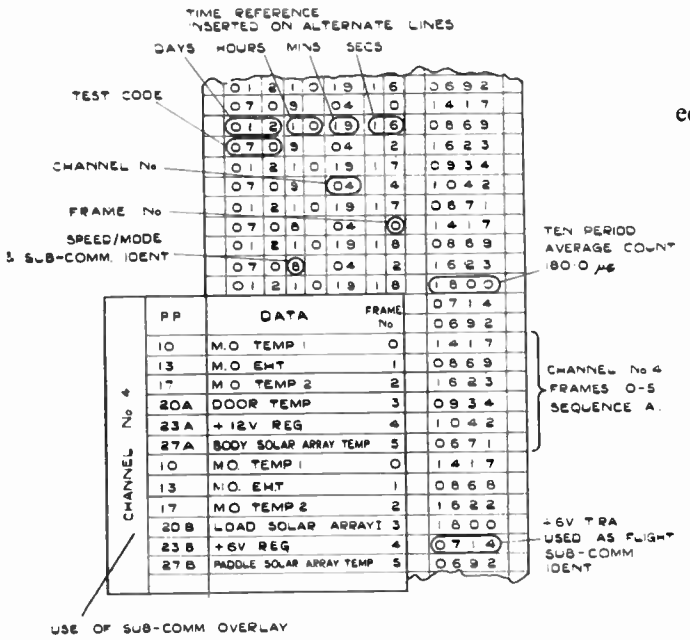


Fig. 7. Typical low-speed print-out.

most frequent use in printing out selected channel ten-period averages under control of the print command from the decommutator. It can, however, print any data derived by direct line from the frequency counter and digital voltmeter in 1248 b.c.d. form.

Figure 7 shows the format of a typical low-speed print-out. An overlay card may be prepared to assist in interpreting the data.

5. Trailer Mounted Data Recording and Processing Station

The principal functions of the trailer-mounted equipment may be summarized as follows:

(1) To provide immediate test information in readily understandable form to satellite designers and test co-ordinators.

(2) To record telemetry transmissions made during test phases so that detailed assessments may be made later.

(3) To give the block-house launch controller immediate information on the condition of the satellite during count down.

(4) To give experimenters immediate information during count-down.

(5) To make limited functional tests on sub-assemblies removed from satellites.

(6) To record the satellite telemetry transmissions for a limited period after launch.

The trailers are some 20 ft long and 7 ft 8 in wide internally. All equipment with the exception of the tape recorder and a few proprietary instruments is accommodated in six 19-in racks.

The vehicle services (mains power, air conditioning, etc.) are built into the trailers and have not been disturbed except to carry out such modifications as were necessary to fit the *UK-3* test equipment. In particular, transformers have been fitted to enable equipment to be supplied from 115V single-phase or

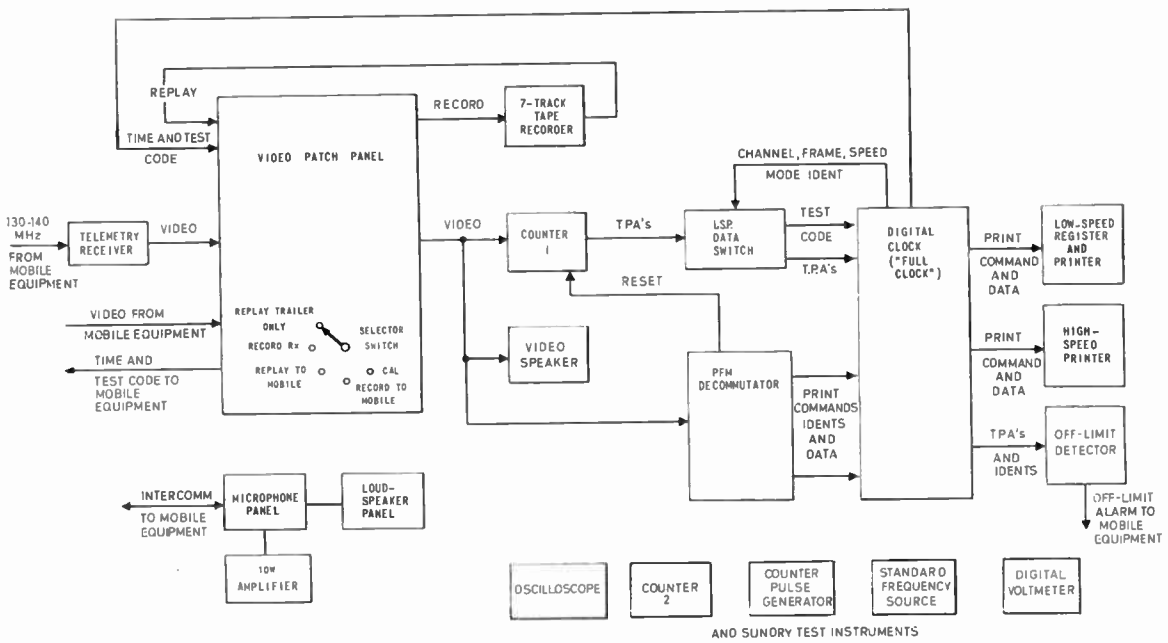


Fig. 8 Block schematic of the trailer-borne receiving and data processing station.

415V three-phase mains. All installed instruments are capable of operating from 50 Hz or 60 Hz supplies.

Two air-cooling units are fitted to each trailer to supplement the built-in personnel heaters. Another addition was the fitting of roof-mounted gantries whose prime purpose is to lift the mobile racks into the trailers where they are stowed for shipment.

A block diagram of the data recording and processing equipment is shown in Fig. 8. It will be seen that several of the units are common to the mobile equipment. This duplication provides a ready back-up in case of faults.

A photograph of the trailer internal arrangement is shown in Fig. 9.

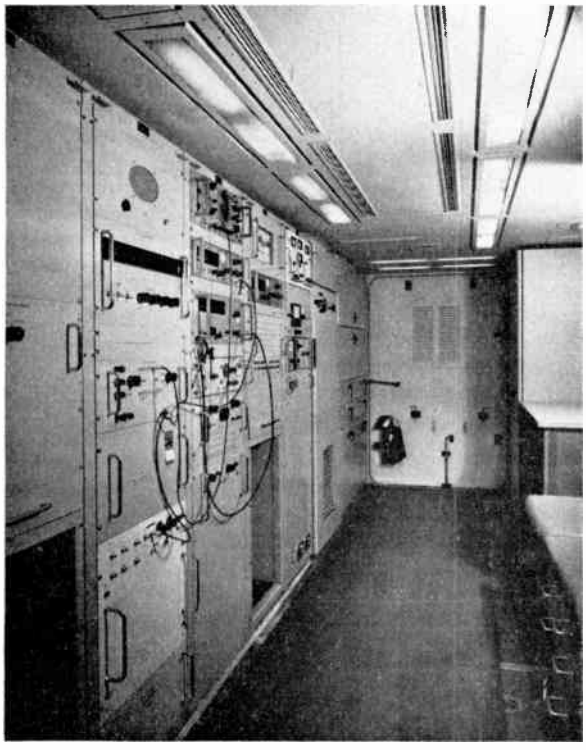


Fig. 9. Equipment in trailer.

5.1. *Video Inputs*

The p.f.m. video signal is either received direct from the mobile equipment on coaxial cable, or is transmitted as r.f. in the 130–140 MHz band along a similar cable fed by the aerial on the mobile equipment. The provision of a receiving aerial on the trailer is under consideration.

To meet the last two conditions a telemetry receiver is installed. It is a double superheterodyne with 30 MHz and 10 MHz intermediate frequencies. In the first oscillator either a b.f.o. or a crystal-controlled stage may be used. The crystal stability is 0·005%. The second i.f. amplifier has bandwidth of 40 kHz between 1 dB points and precedes the phase demodulator.

5.2. *Video Patch Panel*

This unit selects the video signal and distributes it, with the test number and the time code, to processing equipment selected by a switch. The following combinations are possible:

(1) RECORD TO MOBILE. Selected parts of the satellite telemetry transmission are printed out in the trailer with local identification added. This takes the form of a test number and continuously up-dated time code generated in the digital clock. The identification is fed to the mobile station for simultaneous insertion in print-outs there.

(2) REPLAY TO MOBILE. Selected parts of a magnetic recording may be played back and printed out in the trailer, while the recording is also played back to the mobile station for selection and print-out there.

(3) RECORD RX. As for (1) except that the video is derived from the telemetry receiver instead of from the satellite by line.

(4) REPLAY TRAILER ONLY. Selected parts of a recording are played back and are printed out in the trailer with local identification. The test number and time code is transmitted to the mobile station so that selected parts of a current telemetry transmission may be printed out there with local identification data. There can, of course, be no tape record of these transmissions.

(5) CALIBRATION. Injection of calibrating signals on to the tape recorder tracks.

5.3. *Tape Recorder and Video Speaker*

The tape recorder is a seven-track proprietary machine with a.m./f.m. record inputs. Normally three-track inputs are used at 7½ in/s recording speed. 7200 ft of 0·001 in or 5000 ft of 0·0015 in tape may be carried.

A loudspeaker is fitted to give aural monitoring of the video signal being processed. It is found that operators become skilled in recognizing unusual or fault conditions merely by listening to the 'chirp'.

5.4. *Low-speed Print-out*

The extraction of the low-speed signal in the trailer is basically the same as in the mobile equipment. The ten-period averages of the frequency bursts corresponding to each channel are measured in counter 1 and transmitted in 1248 b.c.d. form to the l.s.p. data switch. After amplification they are routed to the low-speed printer register via the

digital clock. Recognition of the channel, frame, speed, mode and format is accomplished by the p.f.m. decommutator and the appropriate decimal and b.c.d. numbers fed to the clock where test code identification is added. These numbers are now passed through the l.s.p. data switch and returned to the low-speed commutator in the digital clock for conversion into the format necessary to drive the low-speed register and printer.

In the trailer no use is made of the COUNTER and digital voltmeter switch positions on the l.s.p. data switch.

5.5. *High-speed Printer*

This instrument, of American manufacture, consists of a numeric pattern generator which writes numerals on a cathode-ray tube. A quartz fibre optical system projects the pattern on to the face of a moving sensitized paper strip. The resultant image is latensified by an ultra-violet light source.

Thirty-two columns are printed to the format shown in Fig. 10. A maximum printing speed of 3200 characters per second is possible, the paper feed being 20 inches per second in this case.

5.6. *Digital Clock*

A block diagram of the full clock is shown in Fig. 11. It should be noted that the sub-units comprising the half clock are contained in the dotted outline. These are essentially the circuits required to encode and commutate information for the low-speed printer, together with the time and test code decoder and a standard time indicator.

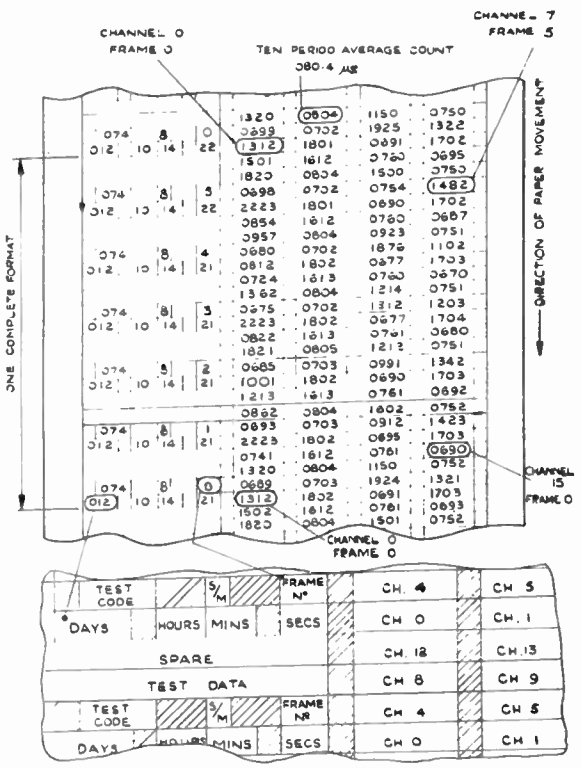


Fig. 10. Typical high-speed print-out.

The full clock includes a high-speed commutator for driving the high-speed printer; it also generates the master time code for insertion into high speed and low-speed records. The half clock in the mobile equipment receives the master time code from the full clock in the trailer, having no facilities for generating it internally.

The logic circuits of the clock make extensive use of Texas Instruments micrologic modules. These are welded to fibre glass printed circuit boards to which are added other components. The use of integrated circuits is expected to maintain a high level of reliability, as well as effecting a considerable reduction in volume and power requirements.

The general construction of the unit is seen in Fig. 12.

The time code source is a 1 MHz oscillator whose crystal is contained in a temperature-stabilized oven. The overall accuracy is of the order of ± 1 second in 11 days. The output is amplified and successively divided by ten to produce a 100 pulses/second input to the encoder. An intermediate frequency of 10 000 p/s is extracted for time-base control of counter 1; a 1000 Hz sine-wave carrier is also extracted for subsequent modulation by the time code.

The 100 p/s output is further divided by binary counters in the encoder to 1 p/s. This signal is fed to a series of nine counters which change state at each decimal interval up to 999 days 23 hours 59 minutes 59 seconds. A test number, between 000 and 999, is selected by three switch banks and passed to the matrix together with the parallel outputs from the counters. The matrix is scanned 100 times per second to give a serial pulse code output. The 1 kHz carrier is then pulse-width modulated to give a 48 bit signal carrying the time and test code numbers. The time frame for this code is 1 second, the p.r.f. is 100 p/s, and 2 ms and 6 ms pulses correspond to binary 0 and binary 1 respectively.

The encoder matrix may alternatively be synchronized to an external time source, the crystal oscillator input being inhibited. A time-set facility enables the matrix to be driven from a variable-speed multivibrator.

The decoder receives the modulated carrier either direct from the encoder or from the tape recorder via switch SW5 in Fig. 11. The carrier is demodulated and the time and test number reconstituted as parallel outputs in 1248 b.c.d. form. Binaries are used to store this information, updating occurring with each change of time or test code number. The time is indicated in

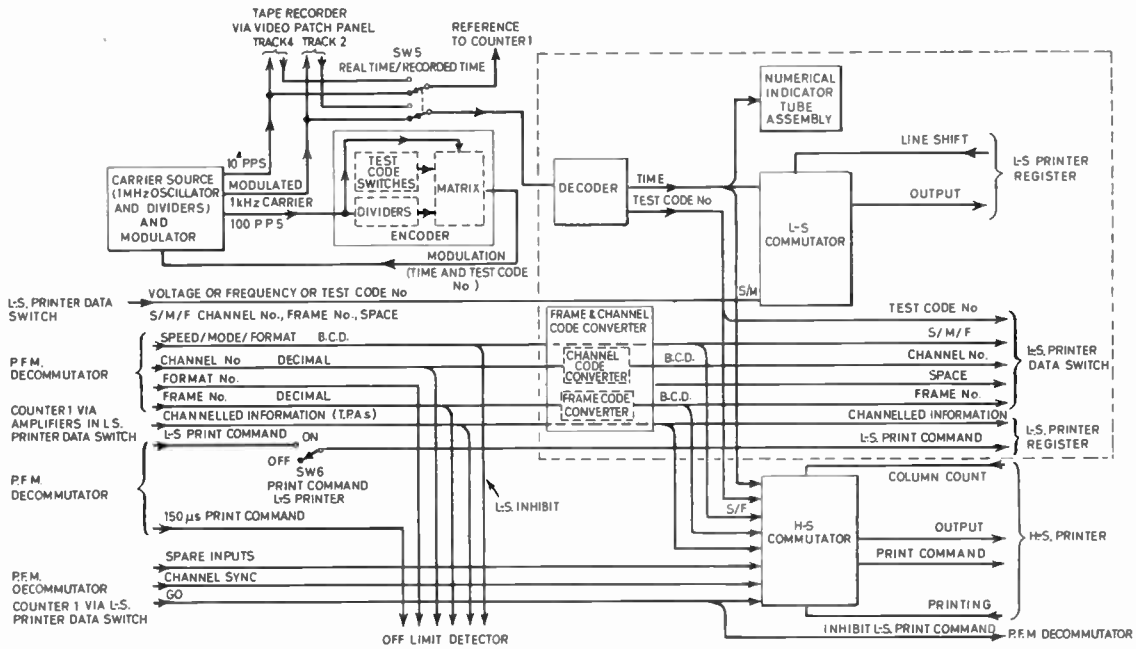
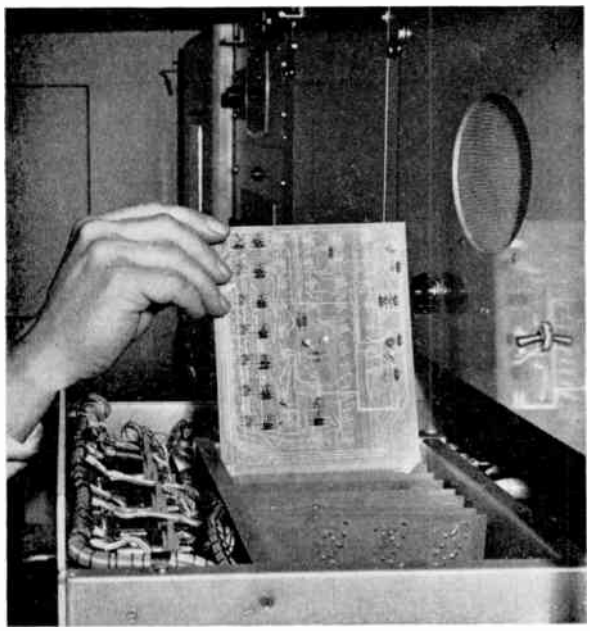
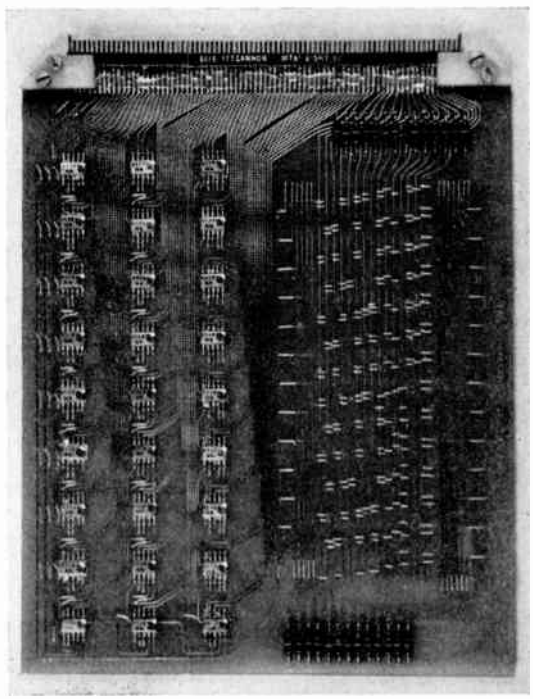


Fig. 11. Block schematic of digital clocks.



(a) Clock chassis.



(b) Clock integrated circuit board.

Fig. 12.

days, hours, minutes and seconds on a set of numeral indicators on the front panel. Each indicator tube incorporates a b.c.d.–decimal converter of the diode matrix type.

The time and test code number are also routed to the high-speed and low-speed commutators. The signals reaching the high-speed commutator comprise ten period channel averages (t.p.a.) derived from counter 1, b.c.d. numbers representing channel and frame numbers (after decimal-binary conversion), speed, mode and format numbers and the time and test code as described above. The commutator

organizes the information into the 32 columns required by the high-speed printer. It also provides the print command pulse required for each character. The pulse is initiated when the following two events occur:

(1) counter 1 completes measurement of each t.p.a.,

(2) printer signals that printing cycle is complete.

The low-speed commutator does not process the t.p.a., which are fed direct to the l.s.p. register. It does, however, gate the identification data and time code to the l.s.p. register. Instead of identification numbers it may be fed with direct voltage or frequency measurements.

5.7. *Miscellaneous Equipment*

Any of the major sub-units or experiments may be removed from the satellite and tested in the trailer which is fitted with a selection of high grade instruments for this purpose. A control pulse generator has been developed to simulate the action of the satellite programmer in initiating and controlling equipment operation.

These test instruments are also used to calibrate the ground check-out equipment itself.

5.8. *Off-limit Detector*

A block diagram of one channel of the unit is shown in Fig. 13. The signal circuits use transistors mounted on printed circuit boards which plug into a single chassis.

The function of the detector is to provide an audible and visual indication of the departure from tolerance of a high-speed p.f.m. telemetry quantity being measured in the trailer. Up to ten channels may be monitored simultaneously between limits pre-set to an accuracy of four significant figures.

The channel, frame and format pulses, and the low-speed inhibit and print command pulses from the clock, are brought to a common amplitude and polarity in the level converter and buffer stages. Each sample selector has two manual channel selector switches (one for each decade), a frame and a format selector. These allow the appropriate line to be connected to an AND gate and buffer which sends a sample command signal when the four input pulses are coincident. The sample command allows the pre-determined limits to be loaded into the comparator, and also initiates the comparison via the AND/OR gate.

The upper and lower limit manual switches select two 4-digit numbers which are routed in 1248 b.c.d. form to the comparator via the limit gates. The AND/OR gate opens to trigger the monostable when:

(1) sample command is present,

(2) high-speed signal is present,

(3) counter has finished counting (print command),

(4) no fault is being signalled from the self-check unit.

The start and inhibit monostables allow the comparison to proceed for 1 ms and control the transfer of the result during the succeeding 1 ms to the indicator system. The comparator consists of 14 bits operating in series, each bit corresponding to one character of the b.c.d. code, so enabling t.p.a.'s between 0000 and 2999 μs to be compared. The comparison, which takes about 4 μs per bit, is performed by logical networks until a GO, NO-GO HIGH or NO-GO LOW verdict is signalled to the appropriate lamps and alarms.

An important feature of the off-limit detector is its self-check system which prevents a fault condition from giving misleading limits indications. Fourteen

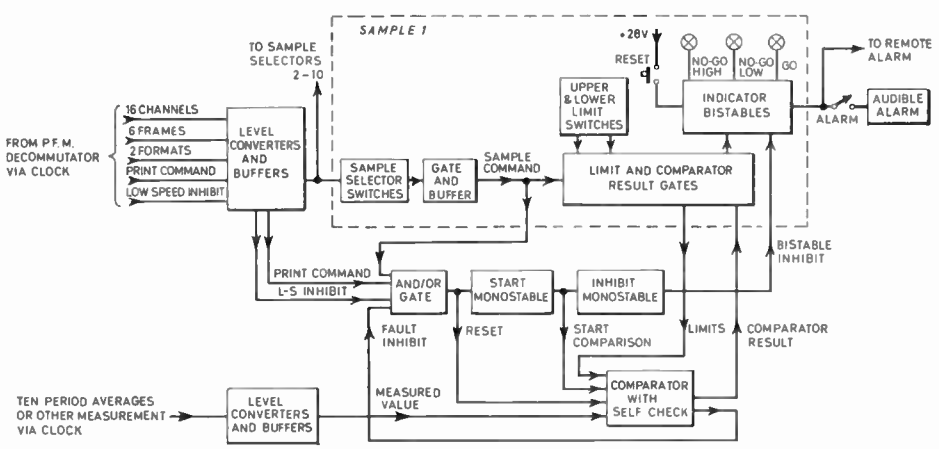


Fig. 13. Block schematic of the off-limit detector.

digital threshold gates monitor the outputs of the comparator bits. These four-input gates require at least two inputs to go to the '1' state to give a '1' output. It is arranged that fault conditions occurring in the comparator bits will cause two or more '1's to be fed to the threshold gates. A '1' output from the latter will light a fault lamp; a locator enables the fault to be isolated to a particular comparator. In addition, the AND/OR gate is prevented from triggering the start monostable so that further comparison is inhibited until the fault is cleared.

6. Conclusion

The ground equipment is complete and both sets are operational. One set has been in continuous use since June 1965 and the other since January 1966. They have seen the D.2 electrical test satellite through its lengthy integration and compatibility trials, and the prototype and flight models through all their environmental and qualification tests.[7] Only minor modifications to the check-out equipment have been found necessary.

When environmental trials of the flight and prototype satellites in the U.K. were completed, both sets of ground equipment were shipped to the Western Test Range, California, for launch operations.

7. Acknowledgment

This paper is presented by kind permission of the Guided Weapons Division, British Aircraft Corporation, Stevenage, and of the Ministry of Aviation.

8. References

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Manuscript received by the Institution on 30th March 1966. (*Paper No. 1100.*)

STANDARD FREQUENCY TRANSMISSIONS

(Communication from the National Physical Laboratory)

Deviations, in parts in 10^{10}, from nominal frequency for **January 1967**

January 1967	24 hour mean centred on 0300 UT		January 1967	24 hour mean centred on 0300 UT	
	MSF 60 kHz and GBR 16 kHz	Droitwich 200 kHz		MSF 60 kHz and GBR 16 kHz	Droitwich 200 kHz
1	— 300·4	— 0·4	17	— 299·7	+ 0·1
2	— 300·1	— 0·2	18	— 299·9	+ 0·1
3	— 300·2	— 0·2	19	— 300·2	— 0·2
4	— 300·2	— 0·1	20	— 299·9	— 0·5
5	— 300·2	+ 0·4	21	— 299·5	— 0·9
6	— 300·6	0	22	— 299·0	— 0·4
7	— 300·5	— 0·1	23	— 299·5	— 0·4
8	— 300·1	— 0·3	24	— 300·2	— 0·7
9	— 300·4	— 0·1	25	— 299·7	— 0·9
10	— 300·7	0	26	— 299·3	— 1·0
11	— 301·2	— 0·4	27	— 298·4	— 0·1
12	— 300·7	— 0·9	28	— 299·7	— 0·5
13	— 300·3	— 1·3	29	— 299·9	— 1·3
14	— 300·3	— 0·8	30	— 299·5	— 1·3
15	— 300·3	— 0·2	31	— 298·9	— 2·5
16	— 300·4	0			

Nominal frequency corresponds to a value of 9 192 631 770·0 Hz for the caesium F,m (4,0)–F,m (3,0) transition at zero field.

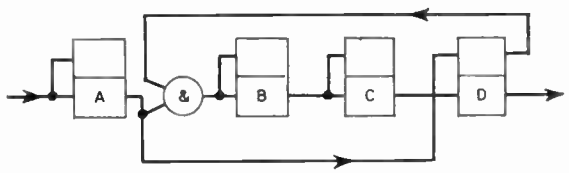
Letters to the Editor

SIR,

The Karnaugh Map and Counting Circuits

With regard to a recent paper by Mr. K. J. Dean† in which he described the design of different counting circuits using Karnaugh maps, I do not think that it is generally known that these methods may be extended to include the design of the decoding matrix required for any such counter. The method, which involves the introduction of the principle of immaterial states, is shown below.

The logic required for ten-line read-out can easily be obtained in the canonical form from the truth table of the particular counter concerned; the difficulty usually arises when minimizing the expressions in order to produce the most economical array of diodes which uniquely define the ten states. Consider as an example the well-known 8 4 2 1 binary coded decimal (Fig. A):



State	A	B	C	D	Logic
0	0	0	0	0	$\bar{A}.\bar{B}.\bar{C}.\bar{D}.$
1	1	0	0	0	$A.\bar{B}.\bar{C}.\bar{D}.$
2	0	1	0	0	$\bar{A}.B.\bar{C}.\bar{D}.$
3	1	1	0	0	$A.B.\bar{C}.\bar{D}.$
4	0	0	1	0	$\bar{A}.\bar{B}.C.\bar{D}.$
5	1	0	1	0	$A.\bar{B}.C.\bar{D}.$
6	0	1	1	0	$\bar{A}.B.C.\bar{D}.$
7	1	1	1	0	$A.B.C.\bar{D}.$
8	0	0	0	1	$\bar{A}.\bar{B}.\bar{C}.D.$
9	1	0	0	1	$A.\bar{B}.\bar{C}.D.$

Fig. A.

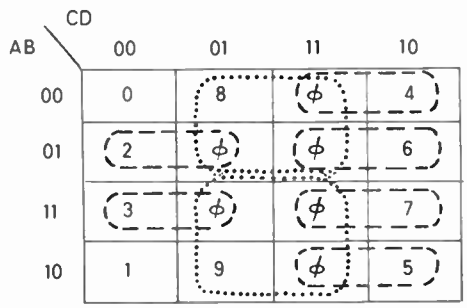


Fig. B.

Having determined the logic for the ten required states, it is then entered on a Karnaugh map, but not as usual by placing a 1, the appropriate decimal digit being used instead. This latter point is a considerable help when reading the map after the minimization has been carried out. The map is now completed with 'don't cares' (immaterial states), represented by ϕ, as shown in Fig. B.

Since ten separate outputs are required, the normal Karnaugh looping process cannot be carried out, as this would merely yield the logic for the counter to be in any b.c.d. state; i.e. a 0 would show that the counter had gone wrong. The 'don't cares' however, represent the states that never exist if the counter is working correctly, so we can eliminate any independent factors between the required outputs and adjacent 'don't cares'. The looping process is then carried out in the usual fashion for a Karnaugh map, as shown above. The matrix logic for each decimal digit may now be read from the Karnaugh map, one variable being eliminated for a loop of two and two variables for a loop of four. The advantage, when reading the map, of having entered the decimal digits will now become quite obvious as each digit may be picked out in turn and the appropriate logic tabulated. Finally, as shown in Fig. C, a matrix diagram may be constructed.

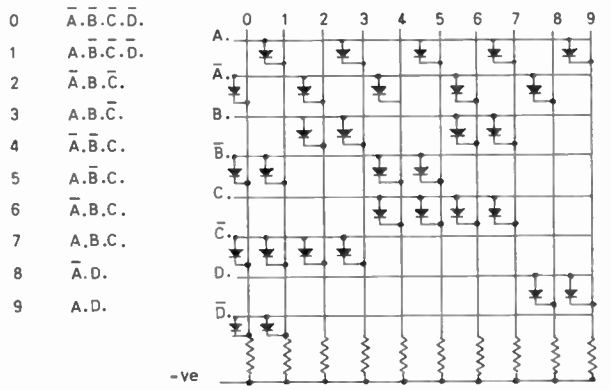


Fig. C.

The matrix shown assumes negative logic, i.e. the most negative state of the output is 1 and the most positive state is 0.

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† 'The design of parallel counters using the map method', *The Radio and Electronic Engineer*, **32**, No. 3, p. 159, September 1966.

SIR,

I would like to thank Mr. Cobham for bringing these points to the notice of readers. It is true that he has quoted a very obvious example, the solution of which is familiar to many people. It is when this method to which he has drawn our attention is applied to reversible counters, for example, which may count up in one code and count down in another, that its benefits become most obvious.

The map method is extremely powerful, and this application, among others, is discussed elsewhere in more detail.†

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† K. J. Dean, 'Integrated Electronics' (Chapman & Hall, London, 1967).

SIR,

Graphical Derivation of Trajectories for Simple R-C Networks containing a Non-Linear Resistance Element with a Negative Resistance Region

The recent publication of papers on graphical derivations of trajectories of logic circuits suggests that the subject is of interest and that some further information may be useful to readers.

Negative resistance oscillators, toggle circuits and other active circuits using tunnel diodes or transistors can be analysed by graphical methods. Usually, these methods enable trajectories of the operating point to be constructed. The papers in *The Radio and Electronic Engineer* by H. Madani[1] and by M. Nalinimohan Rao[2] describe trajectories of the operating point in tunnel diode circuits.

The references contained in these papers go back to a paper by M. Shuleykin published in 1939. A. Lienard had already published in 1928 the basic theory and construction of trajectories for the analysis of such non-linear circuits.[3]

In 1955 I used Lienard's construction for the analysis of transistor oscillators in an article,[4] in which I developed a graphical method, based on Lienard's construction, which not only gives the shape of the trajectories but also allows the speed of movement of the operating point along the trajectory to be determined graphically. The detailed analysis given in this article may be found useful.

A brief description of graphical methods from a practical rather than an academic point of view is contained in the chapter 'Graphical analysis of non-linear oscillation' in the 'Electronic Engineers Reference Book'.[5] My method was also used for the analysis of a Class-B oscillator as part of a paper[6] in which use was made of graphical calibration of the trajectory and limit-cycle in units of time, and a good prediction of actual wave shapes was obtained.

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2nd January 1967.

References

1. 'Graphical derivation of trajectories for transistor-tunnel diode logic circuits', *The Radio and Electronic Engineer*, **32**, No. 4, p. 255, October 1966.
2. 'Trajectory of the operating point in a binary circuit using one tunnel diode', *The Radio and Electronic Engineer*, **32**, No. 5, p. 281, November 1966.
3. 'Étude des oscillations entretenus', *Revue General d'Electricité*, **23**, p. 901, 1928.
4. 'Isocline diagrams for transistor circuits', *Electronic Engng*, **26**, No. 329, p. 312, July 1955.
(Note: This article contains some minor errors: Fig. 9 is printed upside down and there is an error contained in equations (19) to (22). See Correspondence column, p. 461, of *Electronic Engng*, October 1955 issue.)
5. 'Electronic Engineers Reference Book', L. E. C. Hughes (Ed.), Article 914. (Heywood, London, 1958.)
6. 'Design considerations of junction transistor oscillators for the conversion of power from direct to alternating current', *Proc. Instn Elect. Engrs*, **104**, Part B, No. 15, p. 307, May 1957.

Correspondence of a technical nature is welcomed by the Editor for consideration for publication in *The Radio and Electronic Engineer*. Writers may put forward new ideas, which perhaps are not sufficiently advanced or are too brief to form the basis of a paper or short contribution, or they may comment on papers already published, i.e. as 'written discussion'.

Radio Engineering Overseas . . .

The following abstracts are taken from Commonwealth, European and Asian journals received by the Institution's Library. Abstracts of papers published in American journals are not included because they are available in many other publications. Members who wish to consult any of the papers quoted should apply to the Librarian giving full bibliographical details, i.e. title, author, journal and date, of the paper required. All papers are in the language of the country of origin of the journal unless otherwise stated. Translations cannot be supplied.

IMPROVEMENT OF SIGNAL/NOISE RATIO FOR ECHO-RANGING SONAR

Among the correlation methods of improving signal/noise ratios, the polarity coincidence correlation (p.c.c.) system, which considers the polarity only of the input signal, has recently been studied with keen interest. The author of a Japanese paper begins with an analysis of the characteristics of the signal/noise ratio improvement in echo-ranging sonar using the p.c.c. system. Further, the design standards for the p.c.c. system and the effect of improvement of the signal/noise ratio are investigated, comparing the experimental results with the analytical results.

'Improvement of signal/noise ratio for echo-ranging sonar by the system of polarity coincidence correlation', Tetsuro Ichikawa, *Electronics and Communications in Japan* (English edition of *Denki Tsushin Gakkai Zasshi*), **48**, No. 12, pp. 19–28, December 1965.

INTERFERENCE ON SATELLITE COMMUNICATION LINKS

Cosmic noise sources, such as the Sun, can cause considerable interference on communication links via satellites, especially when the antenna is pointing simultaneously to both the Sun and the satellite. Under these circumstances the maximum permissible noise power in speech channels will be exceeded. The time of the event and the duration of the interference can be predicted in the case of a synchronous satellite such as *Early Bird*.

A German paper describes the results of an experiment carried out at Raisting in Germany, using an antenna 82 ft in height. The maximum interference periods in Raisting were in March and October each year and lasted for about $5\frac{1}{2}$ minutes on three successive days.

'Interference on communication links via satellites caused by the Sun', G. Erler and M. Schönfeld, *Nachrichtentechnische Zeitschrift*, **19**, No. 11, pp. 653–58, November 1966.

AUTOMATIC CONTROL OF GROUP-DELAY IN F.M. LINKS

A large part of the signal distortion in f.m. links is due to the frequency dependent characteristics of the group-delay. In addition to correctors with passive circuit elements, electronically-controlled correctors are also used for reducing such distortion. Automatic adjustment of the controlled corrector characteristic seems worth having, especially at unattended repeater stations.

A Soviet paper describes a new system for automatic group-delay control in broadband f.m. links. The error signal for the corrector is obtained by phase demodulation of the sub-carrier signal. The automatic corrector is easily installed on existing links. The circuit of the new system and results of measurements obtained with Hungarian link apparatus are given.

'Automatic group-delay control in link circuits', T. Sharkan, *Telecommunications and Radio Engineering* (English edition of *Elektrosvyaz* and *Radiotekhnika*), **20**, No. 6, pp. 50–56, June 1966.

COMPUTER APPLICATION FOR METEOROLOGICAL DATA

Study of the radio refractive index of the atmosphere and its variation with height in the troposphere is assuming increased importance in recent years in view of the applications in the fields of tropospheric communication systems and precision radar-tracking work. Propagation of radio waves in the u.h.f. and microwave regions is mainly controlled by the refractive index structure of the atmosphere. The refractive index of the atmospheric air is a function of the pressure, temperature and partial pressure of the water vapour in the air, and is relatively independent of frequency over the entire radio spectrum.

An Indian paper describes a simple electrical circuit analogue which has been designed to simplify the conversion of meteorological data to refractive indices.

'A simple radio refractive computer', M. S. V. Gopal Rao, *Journal of the Institution of Telecommunication Engineers*, **12**, No. 5, pp. 315–17, May 1966.

CROSS MODULATION IN TELEVISION RECEIVERS

Adjacent channel reception in television receivers gives rise to interference, which may be reduced by the use of suitable traps in the i.f. circuit of the receiver. Where such traps are used, cross modulation occurring in the tuner is observable.

An Australian paper discusses the problem of cross modulation in v.h.f. tuners with particular reference to the mixer valve as the source of non-linearity giving rise to cross modulation.

A mathematical analysis is given for three r.f. voltages applied to the mixer grid. The importance of low frequency and d.c. voltages applied to the grid is discussed. The mathematics is based on a precise current-voltage relationship for the transfer function of the valve.

'Cross modulation in t.v. tuner mixer stage', H. Wigg and B. H. Sheehan, *Proceedings of the Institution of Radio and Electronics Engineers Australia*, **27**, No. 10, pp. 271–79, October 1966.