A Practical Introduction to Digital IC's

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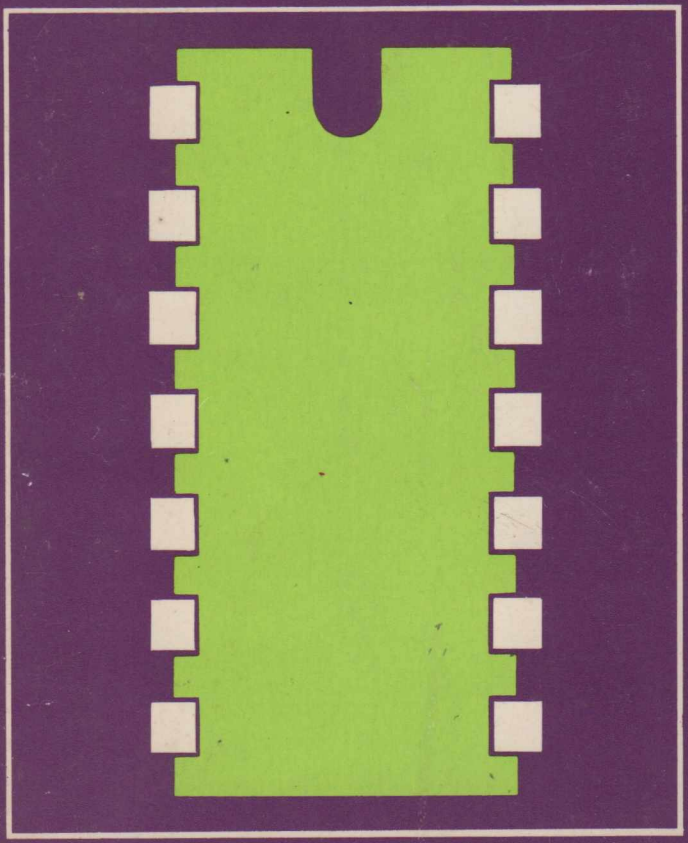

A PRACTICAL INTRODUCTION TO DIGITAL IC's

by

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Chapter 1

AN INTRODUCTION TO DIGITAL INTEGRATED CIRCUITS

Digital ICs, which have been used by computer engineers for many years, are now available to experimenters at home and in schools. Besides having obvious uses in electronic timers, counters, digital voltmeters and other instruments, they are now to be found in a wide range of equipment including model control and fascinating toys and games.

This book is mainly concerned with Transistor-Transistor-Logic (TTL) such as the 7400 series. The range is wide and covers many different types of device. It is also cheap, and readily interfaces with other IC series. Various circuit configurations are available which may be directly interconnected to create a single complex system.

The ICs come in two packaging styles, dual-in-line and flat-pack. The first type is the one generally available and discussed here. The number of pins or contacts depend on the complexity of the device. Simple devices have 14 pins (7 per side), others have 16 pins (8 per side), and a few have

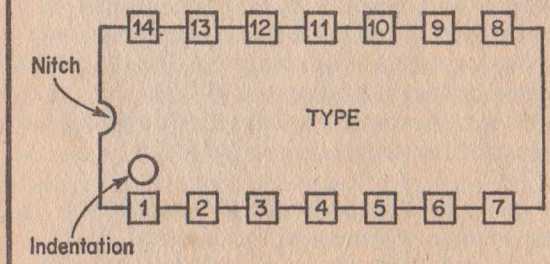


FIG. 1-1. DIL PIN IDENTIFICATION

24 pins (12 per side). Pin spacing is 0.1 inches between centres so that the IC readily fits 0.1 inch matrix Veroboard. As seen in Figure 1-1, pin number 1 is identified by a nitch or small indentation in the top of the moulding. The numbering then runs down one side and back up the other, with the highest pin number always opposite to number 1.

Power supplies for digital ICs are fairly critical. The devices are easily damaged by excessive signal or supply potentials which, unless otherwise stated, must not be allowed to exceed a nominal 5 volts (5.2V max). On the other hand, for reliable operation the supply should not fall below 4.5 volts. When several devices are operating at different frequencies, as in a dividing or counting chain, say, excessive noise or ripple on the supply rail may cause circuit malfunction. It will be realised, therefore, that a precise and well regulated power supply is very desirable. It is also advisable to decouple every five to ten packages with a capacitor having a value in the order of 0.01 to 0.1 microfarads.

Digital circuits employ binary signals having two possible logic states:–

Logic "hi" (high)	4 volts ± 1V
Logic "lo" (low)	zero to about 0.5 volts.

When discussing positive logic, "1" is the same as "hi", and "0" is the same as "lo". Negative logic reverses this convention but is rarely used. It is important for the transition time between the two logic states to be very short. This can cause problems when connecting TTL to non-TTL circuits and switches, but is usually overcome by using the Schmitt-trigger or anti-bounce circuits described later in the book.

Truth Tables are a method of showing the relationship between signal states at different parts of a circuit, or at different times; e.g. between the input or output, or before and after the clock-pulse. The practical examples shown in this book will assist the reader in using and testing the devices concerned.

Fan-Out is the maximum number of unit loads which can be connected across the output of a circuit. Usually every TTL input represents one unit load, although some devices have a higher rating. Sometimes it is required to connect several inputs of a multi-input gate together when the value of the common input will equal the sum of the unit values; e.g. two one-unit inputs connected in parallel represent a load of two units.

Unused inputs can generally be dealt with as follows:—

1. Connect them to the 5 volt power supply via a 1,000 ohm resistor. Several inputs may be connected to the same resistor.

2. Connect the unused input in parallel with a used input on the same gate, provided that the maximum fan-out of the preceeding circuit is not exceeded.

3. Leave the inputs floating (unconnected), when they may be regarded as being "hi". Under certain conditions this may cause the circuit to malfunction.

The inputs of completely unconnected gates may be taken to ground for minimum power dissipation, or left floating unconnected.

As already stated, digital ICs are easily damaged by excessive voltage. High voltages can sometimes occur accidentally from electrical equipment such as test instruments and soldering irons. If possible the cases and metal work of instruments and electrical tools should be earthed or made completely non-conductive. Soldering irons having a ceramic body are suitable. Inductors such as relay coils can also produce high peak voltages and should normally be shunted by a suitable diode or capacitor. High voltage transients frequently occur at the terminals of signal generators and oscilloscopes, and some ohmmeters employ fairly large potentials which appear across the input terminals. Suitable protection circuits for TTL are discussed in Chapter 4.

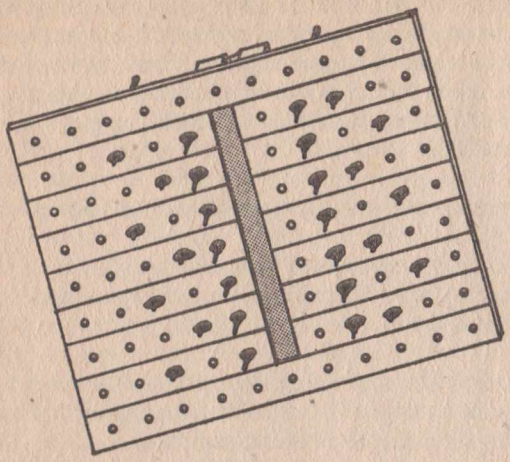


FIG. 1-2. UNDERSIDE OF VEROBOARD SHOWING I.C. PINS AND VEROPINS. NOTICE INTERRUPTED STRIPS.

The high circuit density and small packaging of digital ICs make it necessary for the inexperienced experimenter to acquire new skills. The techniques used by the writer are illustrated in Figures 1-2 and 1-3. The devices are mounted directly onto circuit boards or via special holders. Copper stripped Veroboard having a 0.1 inch matrix is ideal for prototype and "one-off" construction, although it is necessary to interrupt the strips at appropriate points to prevent unwanted connections. This is achieved by using a countersink drill or specially designed spot face cutter obtained from Veroboard stockists. Wire links are used for cross connections. Single strand insulated instrument wire may be used. The writer obtained a good supply by stripping down a length of multicore cable. Good joints are made by firmly hooking the wires around the pins before soldering. It is a good idea to carefully examine each joint area through a magnifying glass to ensure that neither pins or copper strips have been inadvertently bridged by solder or wire particles.

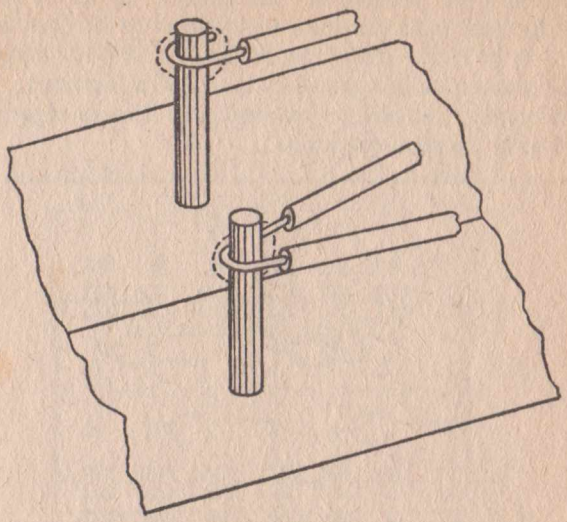
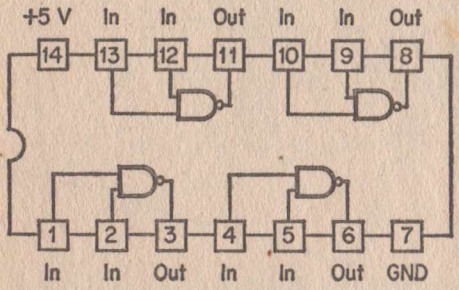


FIG. 1–3. METHOD OF FITTING CONNECTING WIRES TO VEROPINS OR I.C. PINS

The neatest arrangement is to mount all the components on the insulated side of the board, and complete the wiring on the stripped side. It should be remembered that the IC pin numbering seen below the device is a mirror image of that usually shown in diagrams and data sheets. This problem can be avoided by using veropins to bring the connections up to the insulated side of the board so that wiring and components share the same face, when the data-sheet viewpoint is obtained.

The six digital ICs now to be described are employed throughout this book in various projects. It should be noted, however, that they represent a very small sample of the types currently available, and for which data sheets are usually obtainable from the suppliers.

The Quad 2-Input NAND Gate type SN7400 shown in Figure 1-4 contains four independent gate circuits. It will be seen from the truth table that both inputs must be "hi" for the output to be "lo". The output is "hi" for all other input combinations. NAND gates can be wired as inverters, multivibrators, anti-bounce switches and Schmitt-triggers, as well as in the usual gate mode.

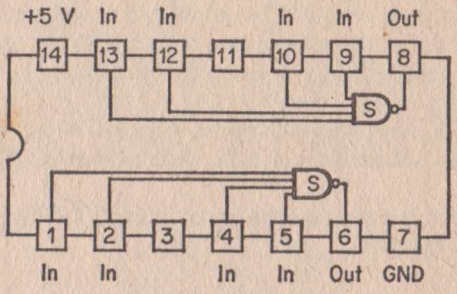


TRUTH TABLE		
EACH GATE		
IN	IN	OUT
hi	hi	lo
lo	hi	hi
hi	lo	hi
lo	lo	hi

Fan-out = 10 each output

FIG. 1-4. SN7400 QUAD 2-INPUT NAND GATES

The Dual 4-Input Schmitt-Triggered NAND Gate type SN7413 shown in Figure 1-5 contains two independent circuits. Logically each circuit functions as a 4-Input NAND gate so that all inputs must be "hi" for the output to be "lo". All



TRUTH TABLE				
EACH SCHMITT GATE				
In 1	In 2	In 3	In 4	Out
hi	hi	hi	hi	lo
lo	lo	lo	lo	hi
lo	hi	hi	hi	hi
hi	lo	hi	hi	hi
and etc.				hi

Positive threshold 1·7 typical
Negative threshold 1·1 typical
Hystersis 0·8 V typical
Fan-out = 10 each output

FIG. 1-5. SN7413 DUAL SCHMITT TRIGGERED NAND GATE

other input combinations make the output "hi". The device has the special characteristic of producing a very good rectangular output pulse irrespective of the input waveshape, thus making it a useful input stage to TTL or other logic families which require good clean pulses with short transition time for stable operation. The significant parameter here is the hysterisis or potential difference between the positive and negative threshold values. The output will undergo an almost instantaneous transition from one logic state to the other for an input potential change of the order of 0.7 volts.

The Dual J-K Master-Slave Flip-Flop type SN7476 (Figure 1-6) contains two independent circuits, each behaving as follows:–

1. Output Q is always opposite to output $\overline{Q}$. When Q is "hi", Q is "lo".

2. If clock pulses are applied and all other inputs are "hi" or disconnected, the circuit will function as a divide-by-two counter. Output Q will go from "lo" to "hi" or "hi" to "lo" at the moment when the clock pulse goes from "hi" to "lo" (negative going pulse edge-operated).

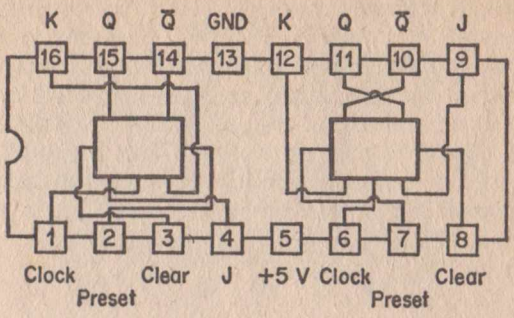
3. Except when clock pulses are applied, inputs J and K will not affect Q.

4. When J is "lo", once the clock pulse has driven Q "lo" it will remain there irrespective of further clock pulses until J goes "hi".

5. When K is "lo", once the clock pulse has driven Q "hi" it will remain there irrespective of further clock pulses until K goes "hi".

6. When the Preset goes "lo" it will over-ride all other inputs and make Q "hi".

7. When the Clear goes "lo" it will over-ride all inputs except the Preset and make Q "lo".

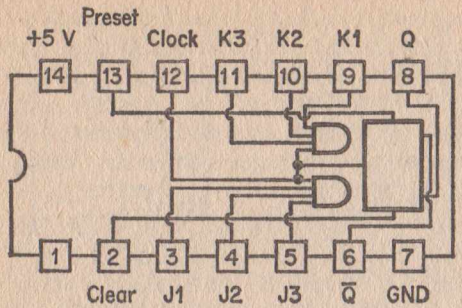


TRUTH TABLE		
EACH FLIP–FLOP		
tn		tn + 1
J	K	Q
lo	lo	Qn
lo	hi	lo
hi	lo	hi
hi	hi	$\overline{Q}$n

tn = Input before clock pulse
tn + 1 = Output after clock pulse
Fan-out = 10 each output

FIG. 1–6 SN7476 DUAL J-K MASTER-SLAVE FLIP-FLOP

The J-K Master-Slave Flip-Flop with AND gate entry type SN7472 (Figure 1-7) is a single circuit which behaves similarly to a circuit in the SN7476, except that the J and K inputs are operated through AND gates so that the three inputs to each AND gate must be "lo" for the function to operate.



TRUTH TABLE AS FIG. 1-5
J = J1, J2, J3
K = K1, K2, K3
Fan-out = 10

FIG. 1-7. SN7472 J-K MASTER-SLAVE FLIP-FLOP

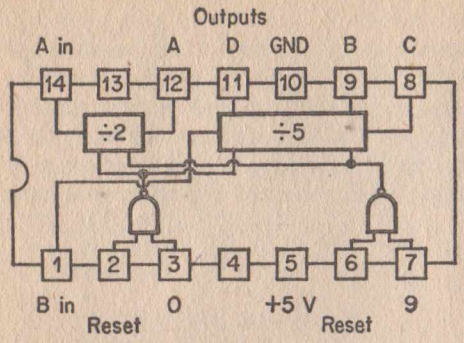
The Decade-Counter type SN7490 shown in Figure 1-8 contains four dual-rank master-slave flip-flops internally connected to provide separate divide-by-two and divide-by-five counters. Gated reset connections are provided to inhibit count inputs and return all outputs to Binary-Coded-Decimal (BCD) zero or nine. Three divider modes are possible:—

1. Completely separate and independent divide-by-two and divide-by-five counters (except for the reset function).

2. BCD output. Both counters in series with the divide-by-two counter at the input end. This mode is used to drive the decoder-driver type SN74141.

3. Divide-by-ten with symetrical square wave output. Both counters in series with the divide-by-five counter at the input end.

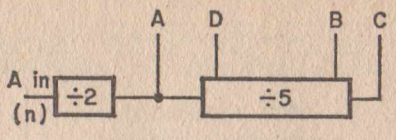
The BCD-To-Decimal Decoder-driver type SN74141 shown in Figure 1-9 will directly drive a gas-filled cold-cathode indicator tube (Nixi) from a BCD input such as that provided by the SN7490 just described. Up to 70 volt protection is provided at the outputs going to the indicator tube, although the nominal 5 volt limit still applies to other connections. The indicator tube supply should exceed the tube starting voltage but not be greater than 70 volts above the tube running voltage. For tubes which ionise at 180 volts and run at 140 volts, a power supply in the order of 190 volts is satisfactory.



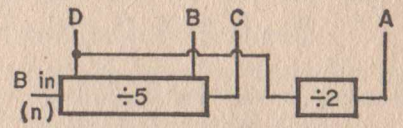
Fan-out = 10 each output
Resets must be 'lo' for counter to operate
n = clock or counter input

TRUTH TABLE				
BCD MODE				
n	A	B	C	D
0	lo	lo	lo	lo
1	hi	lo	lo	lo
2	lo	hi	lo	lo
3	hi	hi	lo	lo
4	lo	lo	hi	lo
5	hi	lo	hi	lo
6	lo	hi	hi	lo
7	hi	hi	hi	lo
8	lo	lo	lo	hi
9	hi	lo	lo	hi

FIG. 1-8. SN7490 DECADE COUNTER

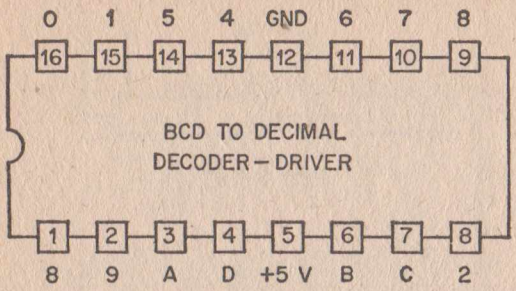


BCD MODE



SYMMETRICAL MODE

TRUTH TABLE				
SYMMETRICAL MODE				
n	B	C	D	A
0	lo	lo	lo	lo
1	hi	lo	lo	lo
2	lo	hi	lo	lo
3	hi	hi	lo	lo
4	lo	lo	hi	lo
5	hi	lo	lo	hi
6	lo	lo	lo	hi
7	hi	hi	lo	hi
8	lo	hi	lo	hi
9	hi	lo	hi	hi



Selected output sinks to near ground potential for directly driving gas-filled indicator tubes.

TRUTH TABLE				
INPUTS				OUTPUTS
A	B	C	D	ON = lo
lo	lo	lo	lo	0
hi	lo	lo	lo	1
lo	hi	lo	lo	2
hi	hi	lo	lo	3
lo	lo	hi	lo	4
hi	lo	hi	lo	5
lo	hi	hi	lo	6
hi	hi	hi	lo	7
lo	lo	lo	hi	8
hi	lo	lo	hi	9
OTHER COMBINATIONS				NONE

FIG. 1-9. SN74141 BCD TO DECIMAL DECODER – DRIVER

Chapter 2

A LOGIC CIRCUIT TEST SET

The experimenter who starts using digital ICs faces three basic problems:—

1. How to demonstrate the device in order to understand what it does, the input required, and the output obtained.

2. How to test a new or suspect device.

3. How to power and stimulate an experimental "hook-up" containing one or more digital ICs.

The unit to be described is one possible solution. It is designed mainly to cover the requirements of the TTL range but is generally suitable for other series.

It will be apparent from the foregoing chapter that an important requirement for the test set is a precise and well regulated power supply. Because accidents can happen, especially with temporary "hook-ups", short circuit protection is also desirable.

A second requirement is some form of logic stimulus as even the most simple logic circuit requires some form of input. A decision has to be made regarding the number of logic outputs to be provided. Circuits to be catered for include gates with 8 inputs, master-slave J-K flip-flops with five, and other circuits with four BCD inputs. After much thought it was decided to provide eight fixed outputs (four "hi" and four "lo") and two outputs which can be switched either "hi" or "lo". Special design was necessary to ensure that only one logic "hi" and logic "lo" state occurs for every cycle of the switch. This is very important when testing counting circuits.

Finally, the experimenter often wants to know the output state of the circuit under test. In this design one lamp is provided which lights for logic "hi" or "lo" depending on the terminal used. Some constructors may wish to provide additional lamps so that more than one output can be observed at the same time. This would be particularly useful when the device being checked has a BCD output. There is no reason why additional lamp circuits cannot be fitted, except that each lamp dissipates 60 mA when lit, thus limiting the power available to the system under test. Also there is the cost of the extra lamps, holders and driver transistors to be considered. Unlike the input, where stimuli may have to be applied to several points simultaneously, the output state can be checked sequentially.

The circuit for the test set is shown in Figure 2-1. It will be seen that the mains is brought in via a fused three pin mains plug and double-pole ON-OFF switch to the primary of the mains transformer. The centre tapped 9–0–9 volt rms secondary drives the full wave rectifier diodes D1 and D2. An alternative arrangement would be a single 9 volt winding driving a bridge rectifier. Direct current from the rectifier is smoothed by electrolytic capacitor C2 before being fed to the voltage regulator IC2. This little device contains a Zener diode voltage reference, error amplifier, series regulator, and short circuit protection, all in one package. In the event of a short circuit, current overload or overheating, the output voltage falls to nearly zero. The pilot lamp LP2 wired directly across the output of IC2 gives ample warning of something wrong.

Fixed "hi" logic is derived from the 5 V rail via separate current limiting resistors R3, R4, R5 and R6. The earthed or GND rail provides the fixed "lo" logic. Switched logic is taken from the outputs of IC1.

Theoretically it would seem that the switched logic could be taken direct from a simple changeover switch selecting either the 5 volt supply through a current limiting resistor, or

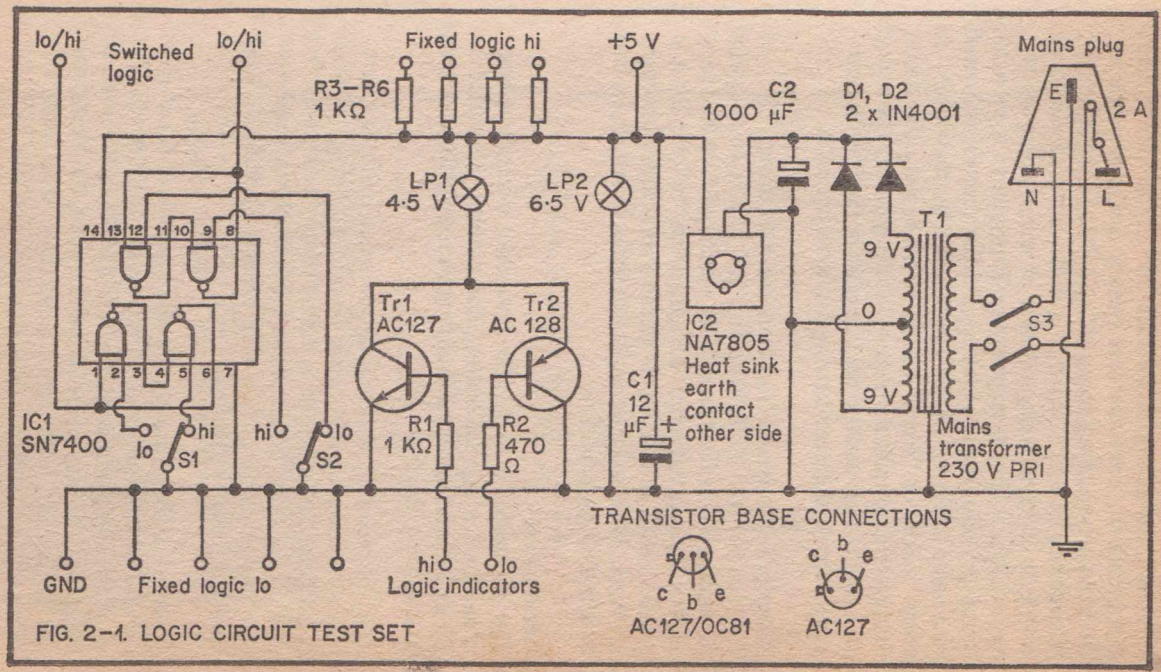


FIG. 2–1. LOGIC CIRCUIT TEST SET

"ground", depending on whether "hi" or "lo" is required. Unfortunately, even the best quality switches produce electrical noise at the instant of "make" and "break". The characteristic "click" heard in a radio when an electrical switch is operated really consists of many pulses which modern digital circuits respond to. The problem is overcome by using gates wired as bistable multivibrators which immediately latch in favour of the gate selected by the switch. A noisy "make" or "break" has no effect because the circuit remains latched until the switch positively selects the opposite gate. Since there are two pairs of gates in the SN7400 integrated circuit, there are two logic outputs available.

Indicator LP1 operates from both the NPN driver TR1, and PNP driver TR2. To light-up for "hi", the input is applied via resistor R1 to the base of TR1 which conducts and passes current through the lamp. To light-up for "lo", the input is applied via R2 to TR2 which will also pass current through the lamp. With no input applied to either terminal, the lamp remains extinguished.

Construction

The instrument is housed in a standard aluminium box measuring 7 x 5 x 2½ inches. The layout is illustrated in Figure 2-2, and the internal arrangement including the wiring (not to scale) in Figure 2-3.

It will be seen that the terminals, switches, indicator lamps, mains transformer and circuit board containing the other components, are mounted in the lid which becomes the front panel. The circuit board can be 0.1 inch matrix Veroboard, with copper strips on one side suitably "doctored", and Veropins fitted as required.

A precise drilling template for the front panel is not given because the dimensions and positions of the holes will depend on the actual components used. Once the holes have been drilled and the burr cleared from the edges, the front panel can be covered with self-adhesive vinyl sheet such as "Contact" or "Fablon". This provides a suitable background

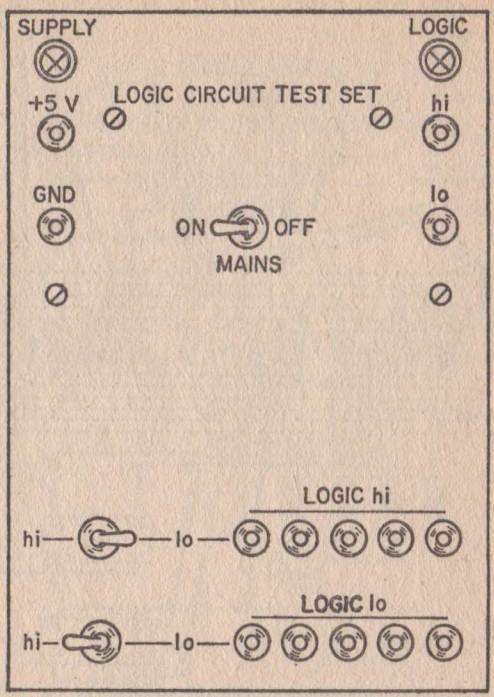


FIG. 2–2. FRONT PANEL LAYOUT

for transfer dry-print lettering, such as "Blick", which may be used for the terminal and switch legends. The lettering should be applied after the components are mounted, and then protected by a coat of varnish. Clear fingernail varnish is ideal.

The voltage regulator IC2 should be fitted with a heat sink made from about 1½ square inches of 18 gauge metal bent "U" shape. This is held in place by the same 6BA bolt as that which secures the IC to the circuit board. Examination of the IC will show that metal is exposed on one side, and this should make a firm clean contact with the heat sink. Heat conduction

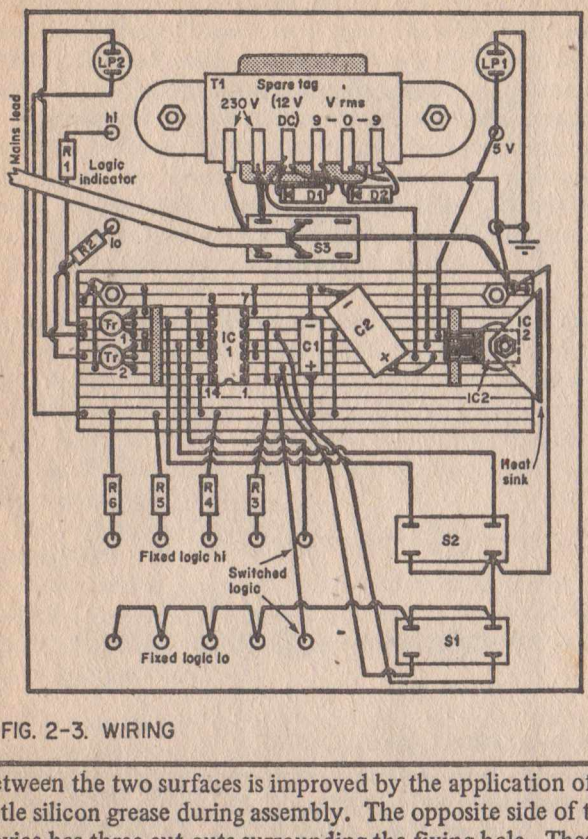
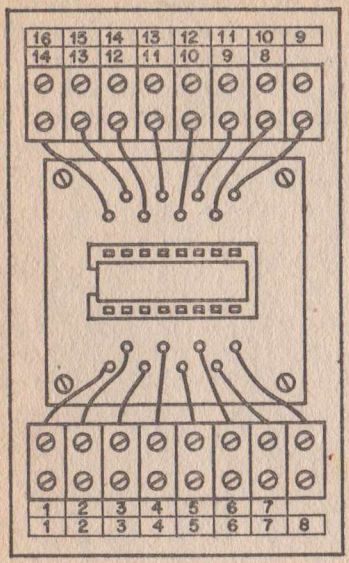


FIG. 2-3. WIRING

between the two surfaces is improved by the application of a little silicon grease during assembly. The opposite side of the device has three cut-outs surrounding the fixing hole. These are relevant to identifying the connect tags as shown in Figures 2-1 and 2-3.

The wiring is straightforward and should cause no problems but, for safety reasons, it is essential that the conductors carrying mains voltages are well insulated. The writer used plastic covered mains flex for the mains and transformer primary connections, and single-strand plastic-covered tinned-copper wire for the low voltage circuits.

When the wiring is completed the unit may be tested. The 5 volt supply should remain constant to within ± 0.2 volts for loads ranging from zero to 500 milliamperes. This can be checked by applying a suitable 10 ohm load across the terminals. Any sudden fall in output over a reasonably short period is probably due to an insufficient heat sink for IC2. The logic circuits are checked by linking the outputs to the logic indicator input terminals.



SIDE ELEVATION

FIG. 3-1. TEST BOARD

Chapter 3

TESTING AND IDENTIFYING DIGITAL INTEGRATED CIRCUITS

The testboard shown in Figure 3-1 enables ICs to be rapidly checked using the logic test set just described. It consists of a 16 pin IC holder secured to a small strip of Veroboard which in turn is mounted on a block of wood fitted with terminals. A 16 pin holder is chosen because it will also accept the 14 pin package, and so cater for nearly all TTL ICs currently available.

Veropins act as soldering posts for the connecting leads which go to terminal strips. The strips used by the writer are obtainable from nearly all chain stores and electrical dealers. They are usually supplied in 12 way strips but can be cut down to 8 way using a small hacksaw. It was found that if the wire gripping screws are slackened off down one side, the strip comfortably "mates" with standard wander-plugs. Consequently, the leads between the board and test-set have plugs at each end in preference to using capitive leads with plugs at one end only.

It is proposed to discuss in detail the method of logic-testing. Manufacturers tests do, of course, cover a much wider range of parameters but these are outside the scope of this book. It is often taken for granted that if the logic is correct the other parameters are probably satisfactory. This is not true, but if the logic is correct it is probably worth trying the device under working conditions.

In all cases the specified logic response assumes that the device is correctly powered, with the GND (ground) connections made, and 5 volts applied to the Vcc pin. When the device contains a number of independent circuits, such as the Quad NAND gate type SN7400, each circuit should be checked separately.

Type SN7400 in Figure 1-4 is checked by simultaneously applying logic to both inputs of the gate under test and ensuring that the output is in the mode specified by the truth table. That is when both inputs are "hi" the output is "lo". All other input combinations make the output "hi".

Type SN7413 in Figure 1-5 is similarly checked. This time all four inputs must have logic applied. If all inputs are "hi" theoutput should be "lo". All other input combinations should make the output "hi".

Type SN7476 shown in Figure 1-6 is checked by applying switched logic to the clock input and fixed logic to the J, K, Preset and Clear inputs. The circuit should function in accordance with the truth table and description given in Chapter 1. The same applies for the type SN7472 shown in Figure 1-7.

Type SN7490 is best checked as follows:—

1. Switched logic to the divide-by-two input (pin 14).

2. Connect counters in the BCD mode by linking pins 1 and 12.

3. Switched logic (set to "lo") to the reset-to-zero (pin 2).

4. Fixed logic "hi" to pin 3.

5. Reset-to-nine function inhibited by connecting pins 6 and 7 to fixed logic "lo".

6. Refer to the truth table for the BCD mode. The count should be zero. Use the logic indicator "hi" terminal to check outputs A, B, C, D (pins 12, 9, 8, 11). These should all be at logic "lo" and the lamp should not light.

7. Set the switched logic going to pin 2 to "lo" to inhibit the reset-to-zero function.

8. Operate the switched logic going to pin 14 through one full cycle. That is from "hi" to "lo" and back to "hi"

9. Check the logic at outputs A, B, C, D. Only "A" should be "hi" and light the lamp (see the truth table for a count of "1").

10. Sequentially cycle the switched logic going to pin 14, and after each cycle check the output logic at A, B, C, D to ensure that results agree with the truth table.

11. Check the reset functions by making pins 2, 6, 3, 7 "hi" and then "lo" in turn. Note that A, B, C, D outputs give BCD readings of 0, 9, 0, 9.

Type SN74141 in Figure 1-9 is checked by applying fixed logic to the A, B, C, D inputs at pins 3, 6, 7, 4 in the order given by the truth table. In this case the correct output can be ascertained by using the logic indicator "lo" terminal to detect the active output pin.

Identifying Digital ICs

An equivalents chart covering most common TTL codes is given in Figure 3-2. The suffix shown against some first numbers may also apply to other numbers in the same range and simply indicates a dual-in-line package.

Some numbers have the letter "H" following the "74" digits; e.g. SN74H00. The logic is similar but high speed performance is better. Alternatively the letter "L" may be used in the same place to indicate a device dissipating less power than the standard type. Also produced is a range of devices having the digits "54" instead of "74"; e.g. SN5400. Again the logic is the same as for the SN7400, but this time the specified temperature limits are much wider (–55°C to 125°C) instead of the usual 0°C to 70°C).

Occasionally the experimenter is faced with the almost impossible task of identifying a device having a code which has been defaced or completely obliterated. This can happen

EQUIVALENTS CHART

Texas	Ferranti	Fairchild or ITT	Motorola	
SN7400	ZN7400	9002	MC7400	
SN7401	ZN7401		MC7401	
SN7402	ZN7402		MC7402	
SN7403				
SN7404	ZN7404	9016	MC7404	
SN7405	ZN7405			
SN7410	ZN7410	9003	MC7410	
SN7420	ZN7420	9004	MC7420	
SN7430	ZN7430		MC7430	
SN7440	ZN7440	9009	MC7440	
SN7441A	ZN7441A			
SN7442				
SN7450	ZN7450	9005	MC7450	
SN7451	ZN7451		MC7451	
SN7453	ZN7453	9008	MC7453	
SN7454	ZN7454		MC7454	
SN7460	ZN7460	9006	MC7460	
SN7470	ZN7470			
SN7472	ZN7472		MC7472	
SN7473	ZN7473		MC7473	
SN7474	ZN7474		MC7474	
SN7475	ZN7475		MC7475	
SN7476	ZN7476		MC7476	
SN7483				
SN7486				
SN7490	ZN7490			
SN7491A	ZN7491			
SN7492	ZN7492			
SN7493	ZN7493		MC7493	
SN7495				
SN74107	ZN74107			

Figure 3–2

Mullard	Siemans	National Semiconductor	
		Old Series	New Series
FJH131	FLH101	DM8000	DM7400
FJH231	FLH201	DM8001	DM7401
FJH221	FLH191	DM8002	DM7402
FJH291	FLH291	DM8003	DM7403
FJH241	FLH211	DM8004	DM7404
FJH251	FLH271	DM8005	DM7405
FJH121	FLH111	DM8010	DM7410
FJH111	FLH121	DM8020	DM7420
FJH101	FLH131	DM8030	DM7430
FJH141	FLH141	DM8040	DM7440
FJL101	FLL101	DM8840	DM7441
FJH261	FLH281	DM8842	DM7442
FJH151	FLH151	DM8050	DM7450
FJH161	FLH161	DM8051	DM7451
FJH171	FLH171	DM8053	DM7453
FJH181	FLH181	DM8054	DM7454
FJY101	FLY101	DM8060	DM7460
FJJ101	FLJ101		
FJJ111	FLJ111	DM8540	DM7472
FJJ121	FLJ121	DM8501	DM7473
FJJ131	FLJ141	DM8510	DM7474
FJJ181	FLJ151	DM8550	DM7475
FJJ191	FLJ131	DM8500	DM7476
	FLH241	DM8283	DM7483
	FLH341	DM8086	DM7486
FJJ141	FLJ161	DM8530	DM7490
FJJ151	FLJ221		
FJJ251	FLJ171	DM8532	DM7492
FJJ211	FLJ181	DM8533	DM7493
	FLJ191	DM8580	DM7495
FJJ261	FLJ271	DM8502	DM74107

in the case of "bargain buys", manufacturers "throw-outs", or ICs salvaged from old printed circuit boards. With a little detective work and the application of "logic!!" it is sometimes possible to identify unmarked digital ICs. Proceed as follows:—

1. If the IC has a number or a part of a number, can it be identified from the chart shown in Figure 3-2?

2. Has the supplier marked the IC with a special code which can be identified from an advertisement or data sheet?

3. If the device was removed from a circuit board, can it be identified by the circuit configuration? This is sometimes possible with easily recognised circuits such as counters.

4. Perhaps the board from which the IC was removed has some legend or marking which will assist identification. At least the supply connections can be traced because they usually go to common lines. Mark these pins before removing the IC from the board.

5. How many pins does the IC have? The following statistics were derived from a review of manufacturers data sheets:—

   14 pin ICs
   85% Vcc=pin 14; GND=pin 7; (gates & inverters)
   12% Vcc=pin 5; GND=pin 10; (counters etc.)
   3% Vcc=pin 4; GND=pin 11; (arithmetic ICs)

   16 pin ICs
   58% Vcc=pin 16; GND=pin 8; (decoders)
   34% Vcc=pin 5; GND=pin 12; (decoders & arithmetic)
   8% Vcc=pin 5; GND=pin 13; (SN7476 flip-flop)

6. Try powering the device. Digital ICs are rarely damaged by incorrect power connections unless the voltage limits are exceeded. Does the power dissipated by the IC come within the normally expected range of 4 to 100 mA?

7. With the device powered, use a voltmeter to detect the potential at each pin. If Vcc or GND connections are incorrect there will either by very low voltage detected at all inputs except that connected to the 5 volt supply, or nearly 5 volts at all pins except that connected to the GND return.

8. If the Vcc and GND connections are correct, the input pins will be approximately 1 to 2 volts, although clock connections to multivibrators and counters can be higher. Outputs will either by "hi" (nearly 5 volts) or "lo" depending on the circuit mode at switch-on.

9. From the data derived from the voltage tests, sketch the base diagram and insert the values and probable base connection. Try to match this with the base connection detail given in data sheets. See Figure 3-3 for an example.

10. Finally, make a full logic check along the lines already discussed. Do not forget to mark the device with the probable code number.

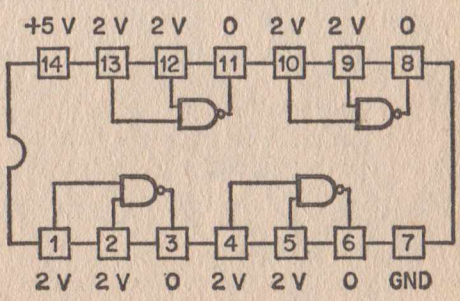


FIG. 3-3. IDENTIFICATION TEST VOLTAGES

Before throwing out faulty ICs, it is a good idea to check whether any serviceable sections remain. For example, the SN7413 contains two Schmitt-triggered NAND gates; perhaps only one of these circuits is faulty. Partly serviceable devices are always handy for experimental work, and it is a good plan to mark them so that the good sections are easily identified. Coloured fingernail varnish is ideal for this purpose. It comes in bottles complete with a little brush for immediate use, and quickly dries.

Chapter 4

SIMPLE PROJECTS USING DIGITAL ICs

Although this chapter deals with simple systems, it does point the way to more ambitious projects.

Figure 4-1 illustrates a method of "breadboard" construction used by the writer. It is really an adaption of the IC testboard already described in Chapter 3. A block of wood has two strips on which to mount Veroboards, and is fitted with a simple front panel to accommodate switches and controls as required. The assembly is completed by a multiway connector block.

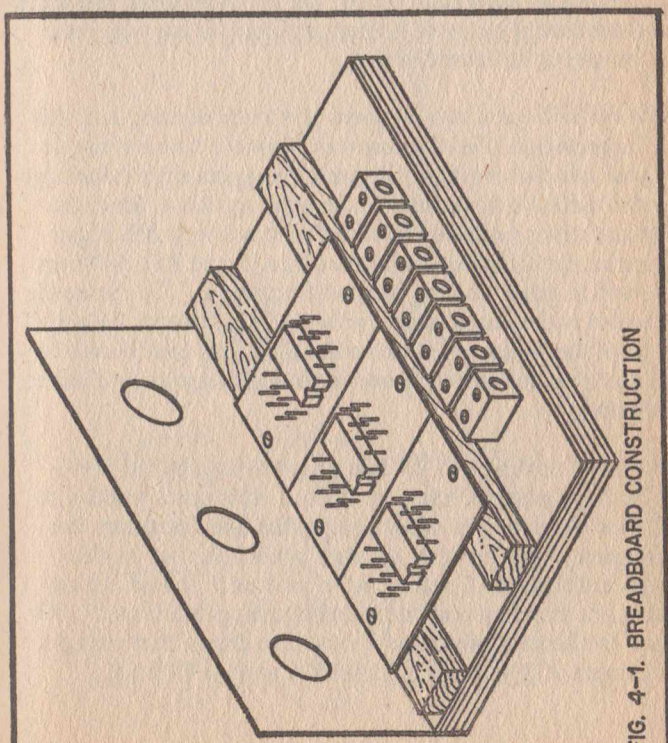


FIG. 4–1. BREADBOARD CONSTRUCTION

Standard 2½ x 1 inch copper stripped Veroboards having a 0.1 inch matrix comfortably take single 14 pin or 16 pin integrated circuits mounted direct or via holders. Veropins, suitably staggered, are used to provide connecting posts. The boards are secured to the two strips by small wood screws or captive nuts and bolts. Whatever method is adopted, the object is to be able to mount, remove or replace the boards easily.

The question arises of whether to fit the IC directly onto the Veroboard or via a holder. If the IC is a basic gate or device frequently used for experimental purposes, it is worth mounting it direct because the holder costs more than the and probably more than the IC. On the other hand, it is useful to have several mounted holders available for use with more expensive or little used devices.

Two NAND gates can be wired as a multivibrator, and this arrangement is ideal for many applications where a simple signal source is required. Figure 4-2 suggests a typical arrangement used as a signal injector for radio servicing. Since the square waves produced by the circuit are very rich in harmonics, the signal can be injected into IF and RF amplifiers as well as those working at lower frequencies. The method is to start at the output stage and work back towards the aerial end of the receiver. At each point the 1 kHz tone should be detected at the output, otherwise the last stage to be checked is suspect.

It will be noticed that the two gates not used by the multivibrator circuit are wired as buffers. It is good practice to buffer oscillators in order to stabilise the frequency the frequency and produce a better waveform, but in this application stages 3 and 4 can be omitted if desired. In any case, the isolation and protection circuit, comprising C3, R3 and the Zener diode, should be used to ensure that voltages in excess of 5 V are not accidentally applied to the IC.

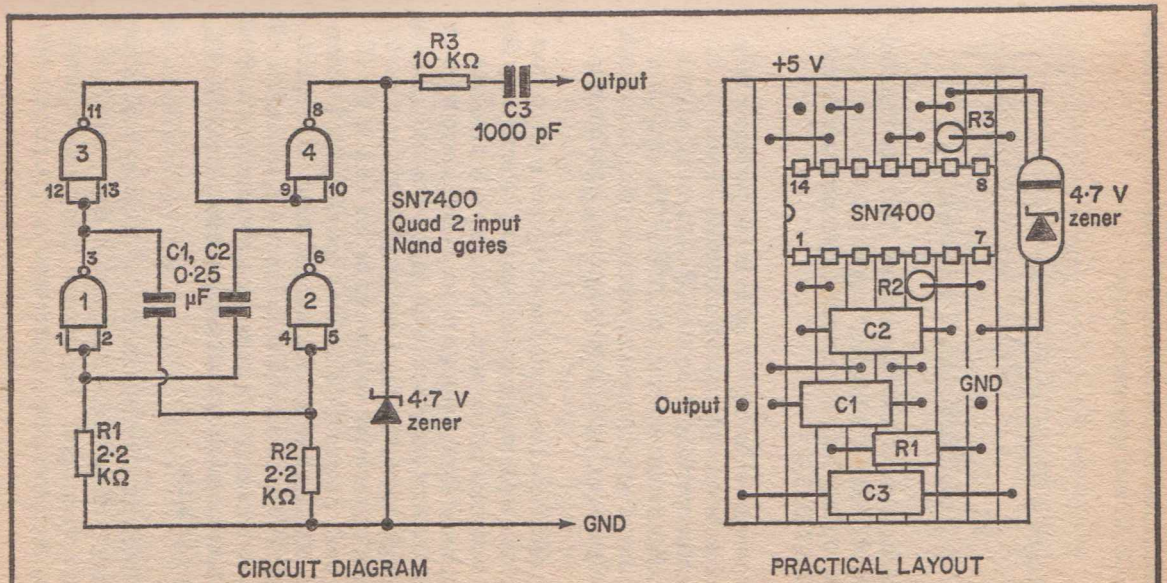


FIG. 4–2. SIGNAL INJECTOR USING A NAND GATE MULTIVIBRATOR

The multivibrator frequency mainly depends on the values of R1, R2, C1, C2 and approximates to:–

$$\text{frequency (Hz)} = \frac{10^6}{(C1\ R1) + (C2\ R2) \times 0.9}$$

where C is in microfarads and R is in ohms.

The formula does not take into account other factors including external loads. If a precise frequency is required, it is advisable to make both or one resistor variable within the range 2.2 kΩ ± 25%.

The convenience of having four gates in one package is fully exploited in the tone generator illustrated in Figure 4-3. A multivibrator operating at about 800 Hz is switched by a second multivibrator operating at 22 Hz. The result is a combination of both frequencies producing the characteristic high pitched "burr" used in telephone and intercom sets.

It will be seen from the circuit that the output is taken from across R4 to a high impedance loudspeaker. Alternatively the telephone earpiece can be used. This normally produces sufficient sound for the average room. If the intercom has an amplifier, the tone can be fed to the input, thus making use of the existing loudspeaker. Once again care should be taken to ensure that no excessive voltage can be fed back to the IC. This can easily happen if the device is operating into a system using inductors such as transformers and relays. If in doubt, use the protection circuit shown in Figure 4-2, although it will probably be necessary to increase the series capacitor to about 10 microfarads, and decrease the series resistor to a value not less than 470 ohms.

The multivibrator is just one method of obtaining a rectangular waveform. Sometimes it is required to derive this shape from some other signal. For instance, many low-frequency sine-wave oscillators have a square-wave output facility, but

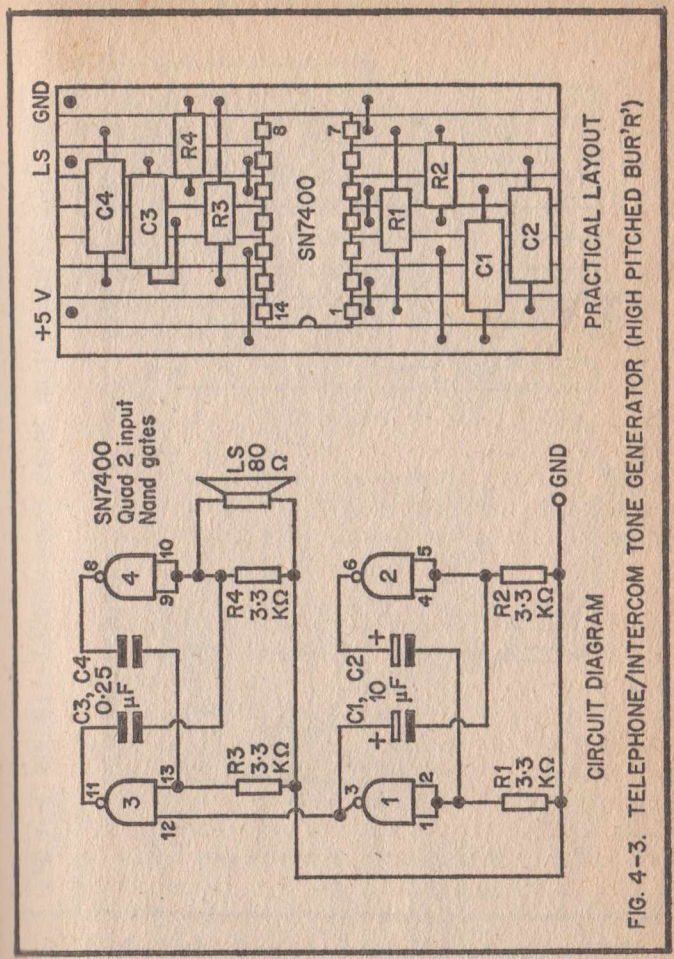


FIG. 4–3. TELEPHONE/INTERCOM TONE GENERATOR (HIGH PITCHED BUR'R')

the waveform is not good enough to drive a TTL system. The circuit shown in Figure 4-4 produces a good rectangular waveform from virtually any signal and makes the ideal input interface for TTL.

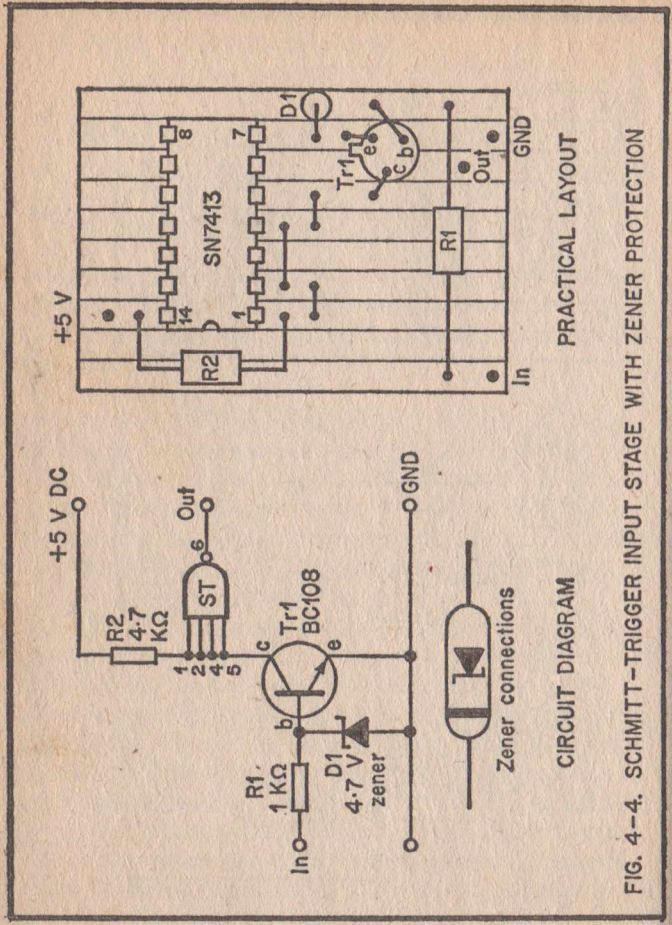
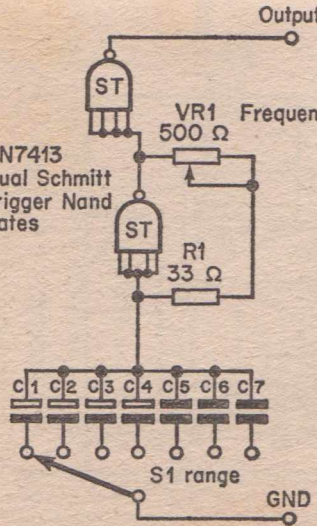


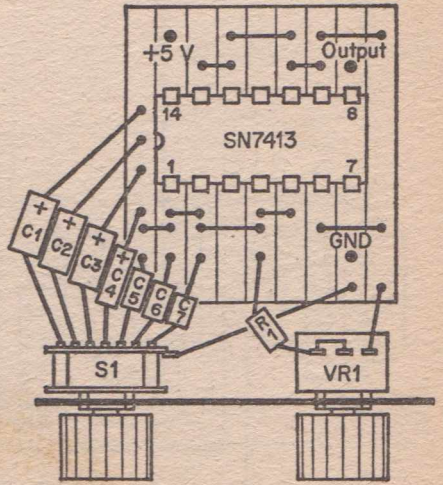
FIG. 4–4. SCHMITT–TRIGGER INPUT STAGE WITH ZENER PROTECTION

It will be seen that an input transistor is used to hold the Schmitt-triggered NAND gate at the required level and, with R1 and a zener diode, protect the IC against excessive input signals. If the device is to be used to feed circuits using high voltages, it will be desirable to provide output protection as well, and the arrangements discussed for the previous two circuits will normally be satisfactory.



CIRCUIT

FREQUENCY RANGE			
C	µF	F(low)	F(high)
1	1000	1 Hz	10 Hz
2	100	10 Hz	100 Hz
3	10	100 Hz	1 KHz
4	1	1 KHz	10 KHz
5	0·1	10 KHz	100 KHz
6	0·01	100 KHz	1 MHz
7	0·001	1 MHz	>5 MHz



PRACTICAL LAYOUT

FIG. 4-5. MULTIRANGE PULSE GENERATOR

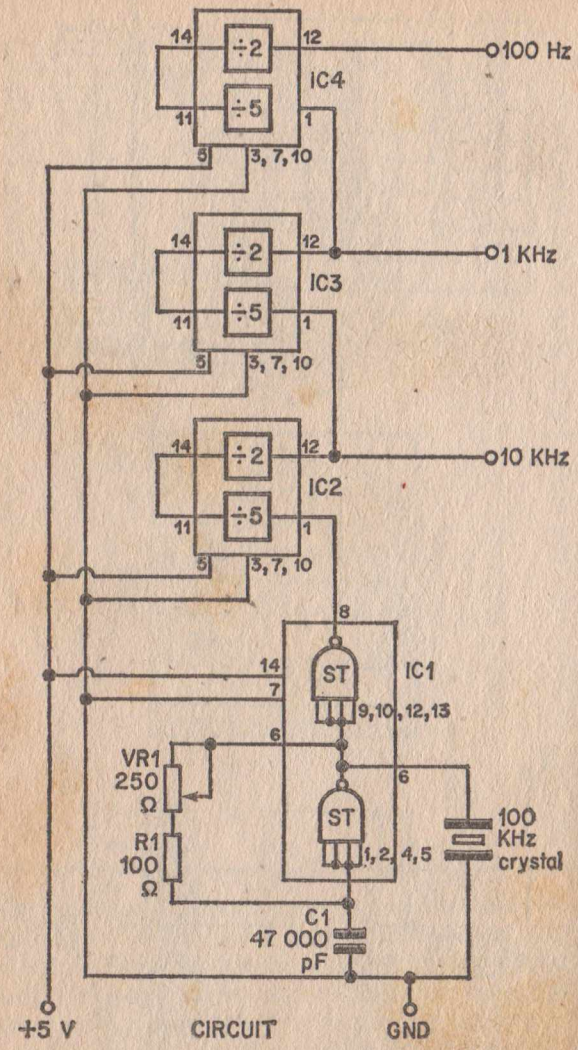
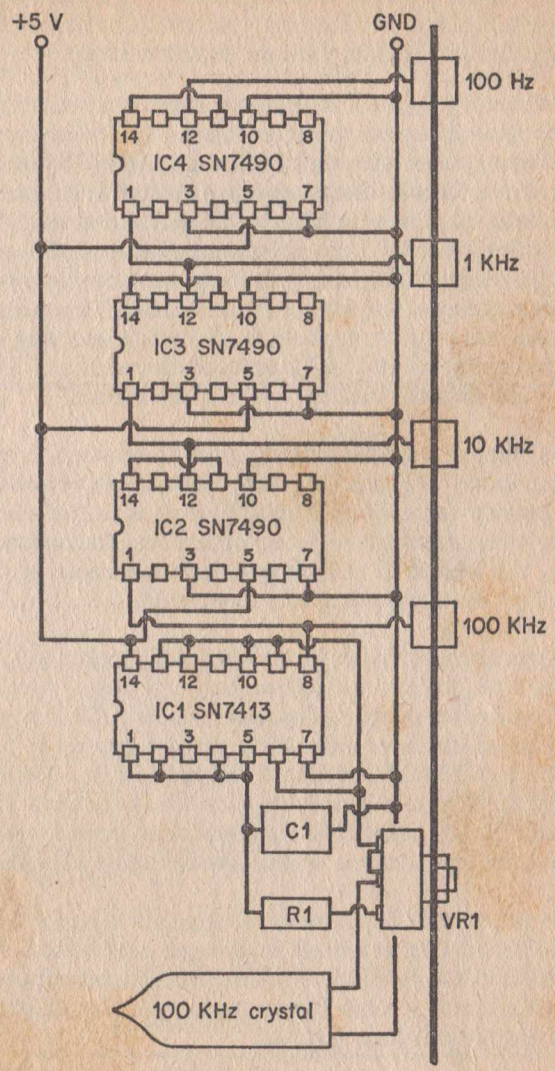


FIG. 4–6. CRYSTAL CONTROLLED FREQUENCY REFERENCE



PRACTICAL LAYOUT

Construction is straightforward, with a 2½ x 1 inch Veroboard again being used, but this time a second break is made in the copper strips to isolate the input transistor stage.

The Schmitt-triggered NAND-gate is also used in the multi-range pulse generator shown in Figure 4-5. The advantage of this arrangement over the circuit using a NAND-gate multi-vibrator is the wide frequency range obtainable from only one CR network. From the table it will be seen that the 500 ohm variable resistor VR1 gives a frequency swing of 10:1 on all ranges except the highest, so that seven switched ranges give continuous coverage from 1 Hz to 5 MHz. The circuit can actually be made to oscillate at 15 MHz by reducing the capacitor to about 47 pF, although the setting of VR1 becomes critical if oscillation is to be maintained. .

Construction is simple, with the layout following the arrangement shown in Figure 4-1. Once again it will be necessary to provide output protection if the unit is to feed circuits employing potentials in excess of 5 volts. The constructor may also wish to fit a simple output potentiometer, although for logic circuits this is usually unnecessary.

The oscillator just described can be readily locked to a quartz crystal to provide a stable frequency reference. A suitable arrangement is shown in Figure 4-6, where a 100 kHz crystal controlled oscillator drives three decade counters to provide outputs of 100 kHz, 10 kHz, 1 kHz and 100 Hz. Since these outputs are rich in harmonics, they are an excellent signal source for the calibration of communication receivers and RF signal generators as well as low frequency equipment.

The system may be constructed onto four separate 2½ x 1 inch Veroboards, or a single larger board can be used. In the latter case it is necessary to interrupt the copper stips between the ICs as well as below them in order to isolate the stages and prevent the pins from shorting.

The frequency of the oscillator has to be adjusted until it locks onto the crystal. The best way to do this is to arrange for the 100 kHz output lead to be near a radio receiver tuned to BBC Radio 2 on 1500 meters long wave. This is 200 kHz and a second harmonic to the required frequency. As VR1 on the reference oscillator is adjusted, the frequency will suddenly lock onto the 100 kHz crystal and its second harmonic will distort the radio signal. The frequency will then stay locked over a relatively wide variation of VR1, which should then be centred between the two non-lock points. The setting should be tested by switching the unit off and on several times to ensure that it always locks onto the crystal very quickly after switch-on.

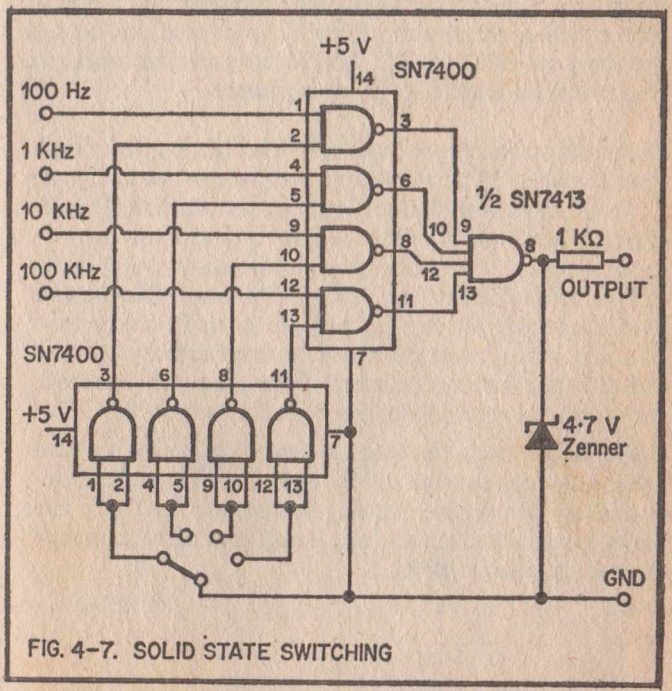
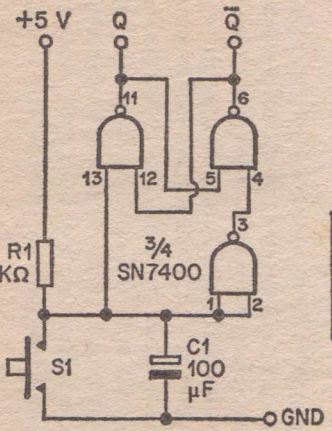


FIG. 4–7. SOLID STATE SWITCHING

If it is considered necessary to provide output protection, isolation can be provided by buffers, such as the four gates in a SN7400 package followed by the usual series resistor and Zener diode.

Some constructors may prefer to switch the different frequencies to a single output terminal. One method is illustrated in Figure 4-7. It will be seen that the four outputs are routed through NAND gates to the four inputs of the second Schmitt-triggered NAND gate. A further four gates, wired as inverters, are used as inhibitors. When their input is "hi", their output is "lo", and no signal may pass through the associated gate. The required frequency is selected by making the input of the appropriate inhibitor "lo". Solid-state switching allows a simple switch to be used, and because switching potentials are DC, there are no problems relating to long switch leads and high frequency losses.

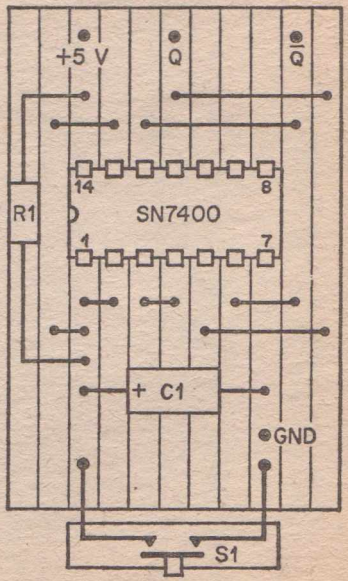
The problems relating to switch noise is high frequency logic circuits such as TTL have already been referred to in Chapter 2. It will be recalled that the logic test set uses a single-pole changeover switch to latch a bistable multivibrator in the required mode. The anti-bounce button pulser circuit shown in Figure 4-8 is derived from this arrangement. The circuit is particularly suitable for use with cheap single-pole press-button switches, or simple slow-speed mechanically operated switches used for model control. When the switch is closed, the circuit very quickly latches with the output "hi". On releasing the switch, the time constant C1.R2 holds the latch sufficiently long enough for the switch contact to become completely clear before allowing the output to go "lo". Thus, the effect of switch noise is completely eliminated, although the time constant is critical.



CIRCUIT

TRUTH TABLE

OUTPUT	NORMAL	S1 CLOSED
Q	lo	lo
$\bar{Q}$	hi	hi



PRACTICAL LAYOUT

FIG. 4–8. BUTTON PULSER

Chapter 5

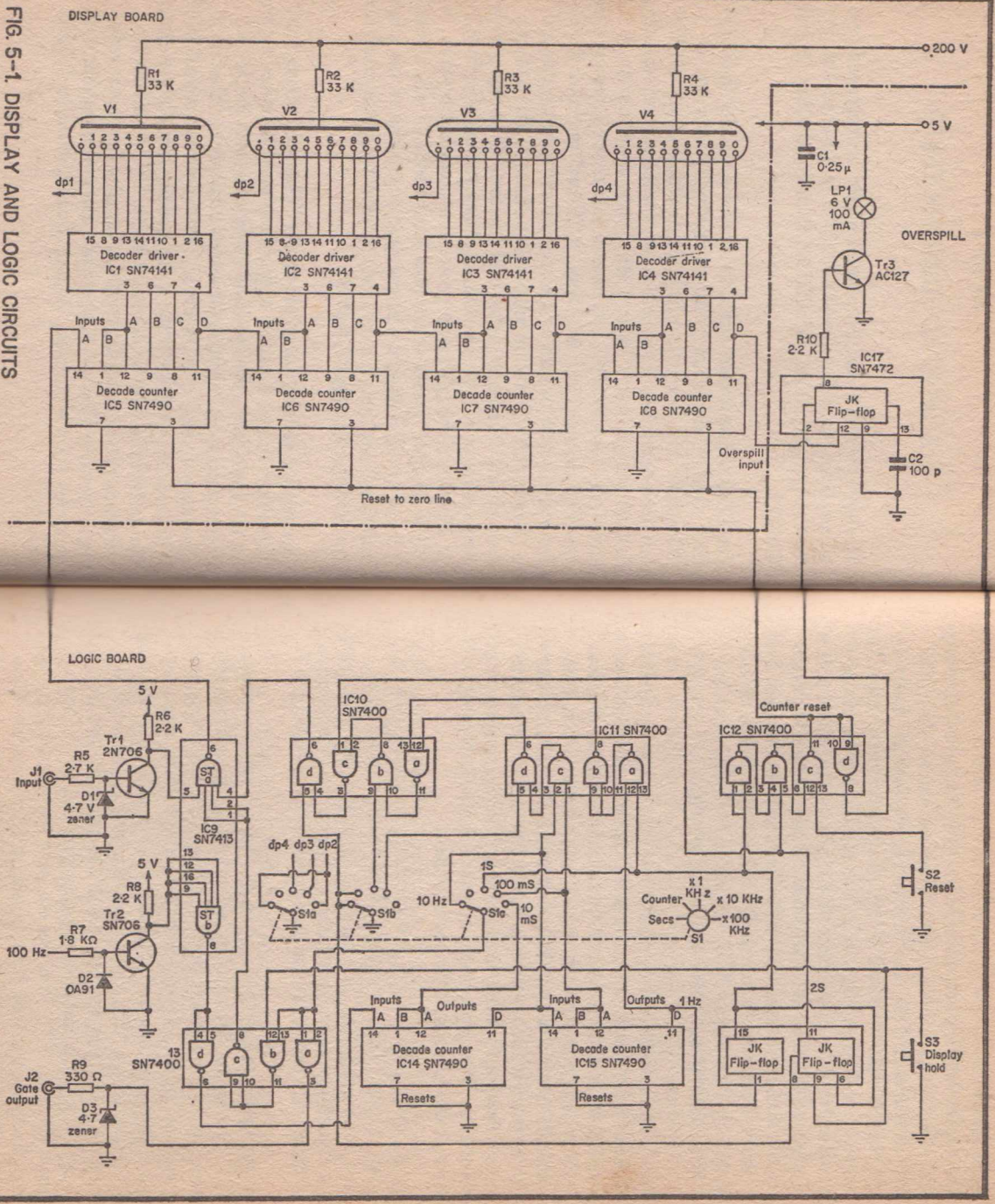
A DIGITAL COUNTER-TIMER

The low cost unit to be described is simple in design and easy to construct. It makes a useful addition to the experimenter's workshop and an ideal introduction to more advanced digital systems.

Gas-filled cold-cathode indicator tubes are used for the four-digit display which has switched decimal points and an "Overspill" lamp to warn when the maximum count of 9999 has been exceeded. A single five-way switch covers frequency in three ranges from 1 Hz to 1 MHz, pulse count unrelated to time from zero to 9999, and time in 0.1 second increments up to 999.9 seconds (16.6 minutes). A "Reset" button is fitted for manual reset to zero of the counter and time ranges, and a "Display-Hold" button enables the timer to be used as a stop watch. The input circuit will comfortably accept a wide range of input waveforms with amplitudes nominally from 2 to 20 volts, although circuit protection exceeds this value. A "Gate Output" socket is provided from which 10 mS, 100 mS, 1 S and 10 Hz pulses may be obtained depending on the range switch setting; thus, the unit may be used as a pulse generator for driving other digital circuits.

Accuracy is generally absolute on the "Counter" range, but is dependent on the timebase trigger frequency for other ranges. In the basic form, the timebase is triggered from the 50 Hz mains supply, and although it is not unknown for the mains frequency to vary by as much as 2 Hz from the nominal 50 Hz (4% variation), this situation is fortunately rare. In practice, the variation is more likely to be within 1%. An alternative arrangement is to use the crystal controlled frequency reference shown in Figure 4-6, and space and power supplies are provided for this purpose. Accuracy can then better 0.1% ± one digit.

FIG. 5-1. DISPLAY AND LOGIC CIRCUITS



The Circuit

The display and logic circuits are shown in Figure 5-1. Starting from the input J1, the signal is applied via resistor R5 to the base of transistor TR1, which, with Zener diode D1, isolates and protects the integrated circuits from excessive voltage. The transistor is followed by one of the Schmitt-trigger circuits contained in IC9. This "gates" the input, and produces pulses of precise amplitude and shape suitable for driving the counting circuits. A chain of four SN7490 decade-counters are used to cover units, tens, hundreds and thousands. These are connected by their 4-wire BCD outputs to SN74141 decoder-drivers which in turn drive the indicator tubes.

The indicator tubes are operated by maintaining a potential between anode and numeral-shaped cathode sufficient to ionise the gas and produce the characteristic cathode glow. The anode is positive with respect to ground, so that the required numeral is illuminated simply by grounding the appropriate cathode. Because the decimal points are a function of the range setting, they are controlled by range-switch wafer S1a. The anode resistors are to limit the current through the tubes once the gas is ionised.

Before every pulse count, it is necessary to set all indicator tubes to zero. This is accomplished by making pin 3 of all four decade counters "hi", although they must be "lo" during the counting process. Incidentally, the reset-to-nine function of the decade counters is made inoperative by earthing pin 7.

As each pulse arrives at pin 14 of the "units" decade-counter IC5, the number displayed by indicator-tube V1 increases by one digit. At the tenth pulse the display reverts to zero, and the output at pin 11 goes from "hi", where it had been since the eighth count, to "lo"; thereby activating IC6 and changing V2 from zero to "1". The overall display now reads "0010". As these operations are repeated, V2 increases by one digit for every ten input pulses until it passes nine and reverts to zero, when V3 reads "1". This goes on, with V3 increasing by one digit for every hundred input pulses, and V4 for every thousand until, finally, V4 passes nine and all tubes revert to zero.

Further pulses will produce an incorrect reading, because the counting chain is going round for the second time but lacks a "ten-thousand" digit. It is necessary, therefore, to warn the operator by lighting the "Overspill" lamp at the moment when all tubes revert to zero. Furthermore, the lamp must stay on until the counting chain is deliberately reset by the operator, or that he knows resetting has occurred. This is the job of C17, which is reset with the decade-counters to make pin 8 "lo" until the count of ten-thousand, when it latches "hi" and activates the lamp driver TR3.

Frequency is measured by allowing the pulse count to take place for a precise period only. This period is defined by the width of gate pulse applied to pins 1 and 2 of IC9. With a one-second pulse width, the readout is pulses-per-second or Hz. A full display reads 9999 Hz, or with the decimal point inserted, 9.999 kHz. The effective frequency range can be increased by reducing the gate width to 100 mS, because 9999 pulses in 0.1 seconds is equivalent to 99990 pulses in one second, or 99.99 kHz. Similarly, with a 10 mS gate, the full display reads 999.9 kHz.

Time is measured by applying a 10 Hz clock-pulse to the counter input also via pins 1 and 2 of IC9. This produces one count every 0.1 seconds, but with the decimal point in front of the first digit, the display actually reads seconds to the nearest tenth of a second.

Gate or clock pulses are derived from a special timebase circuit triggered by a 100 Hz signal, obtained either from the 50 Hz mains via the power unit, or from the crystal controlled frequency reference shown in Figure 4-6. The appropriate gate or clock pulse is selected by switch-wafer S1c and passed through the "Display-Hold" gate and inverter IC13 before being applied to pins 1 and 2 of IC9. Provision is made to access the pulses via an isolating gate in IC13, protection network R9 D3, and output socket J2.

The shortest gate period required by the unit is 10 mS, which is equivalent to one half cycle of a 50 Hz squarewave. To obtain a precise 1:1 mark-space ratio, however, it is necessary to start with a higher frequency and divide down. Hence the 100 Hz signal, which is processed by diode D2, transistor TR2, the second Schmitt-trigger in IC9, inverter in IC13, decade-counters IC14 and IC15, and double flip-flop IC16, to provide all the intermediate frequencies and timing periods down to 0.25 Hz required by the unit.

When frequency is being measured, it is usually necessary to repeat the reading several times in order to detect drift or observe the result of some adjustment to the unit under test. Control logic is derived from the timebase which, automatically resets the counter to zero, allows the count to occur, holds the display for two seconds so that the operator can read it, then repeats the operation. All this is achieved by combining different pulses from the timebase in the correct sequence and phase using the NAND gates IC10 and IC11.

Automatic reset is obtained by combining the 0.5 Hz and 0.25 Hz squarewaves in IC12 in such a way that a one-second reset pulse occurs every four seconds. Both "hi" and "lo" pulses are generated simultaneously in order to reset the decade-counters and overspill circuit. The manual "Reset" button operates by grounding pin 13 of IC12.

The control logic previously discussed is set by range switch-wafer S1b. In the "Counter" and "Secs" positions, pin 5 of IC10 is grounded to keep pin 4 of IC9 "hi", thereby admitting input and clock pulses. At the same time, automatic reset is inhibited by grounding pin 8 of IC16. As the range switch is moved through the frequency ranges from "X1" through to "X100", more blanking waveforms are combined to produce a "window" in the four-second cycle sufficient for only one gate pulse. The "Display-Hold" button S3 operates by earthing pin 12 of IC13, and pin 9 of IC16, to stop pulse counting and automatic reset.

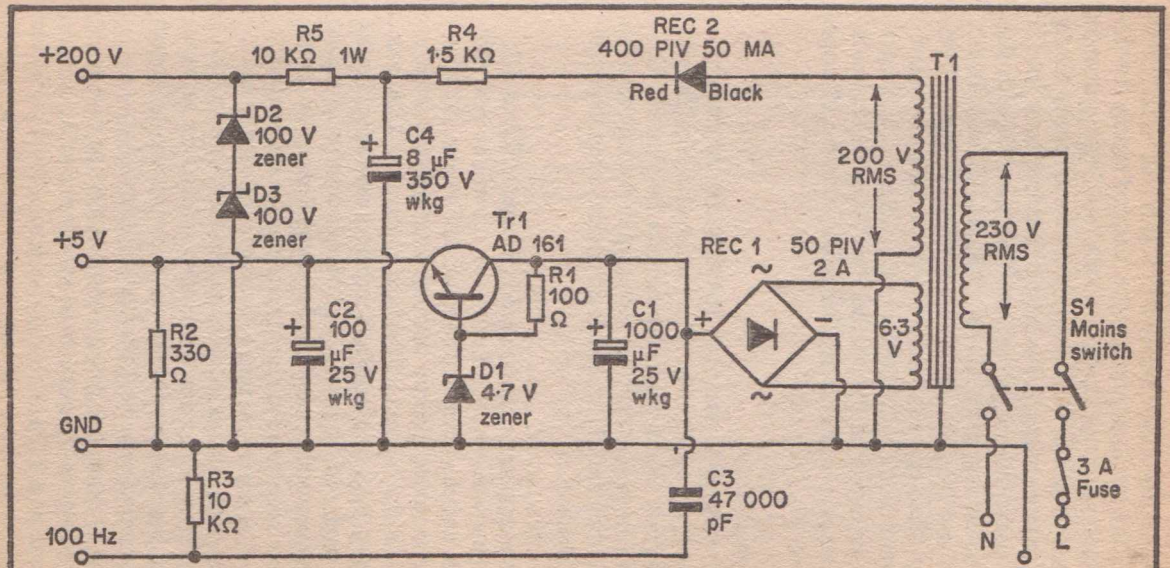


FIG. 5–2. POWER SUPPLY UNIT

The power supply circuit is shown in Figure 5-2. Mains transformer T1 is a small instrument type designed mainly for valve circuits, but in this case the 6.3 V heater winding is connected to a full-wave rectifier D5 to provide the 5 volt supply through a simple series regulator. The high voltage indicator tube supply consists of a simple half-wave rectifier D3, with the smoothing and regulating network R3, R4, C2, and Zener diodes D1 and D2. The 100 Hz timing signal is derived from the unsmoothed output of the full-wave rectifier via C4 and R2. No pilot lamp is fitted because the indicator tubes light up immediately the unit is switched on. Mains protection is by the 2 ampere (or 3 ampere) fuse mounted in the 13 ampere mains plug.

Construction

The instrument is housed in a standard aluminium box measuring 8 x 6 x 3 inches. The display and logic circuits are mounted in the lid which becomes the front panel. The power supply components are mounted in the box so as to be well clear of the display and logic circuits when the front panel is fitted.

The power supply circuit diagram is shown in Figure 5-2, and the practical layout in Figure 5-3. It will be seen that the mains switch, mains transformer and power circuit board are mounted directly into the box with the latter spaced from the bottom of the box by two full 4BA nuts. Plain unclad 0.15 inch matrix Veroboard measuring 5 x 2½ inches is used, with Veropins inserted as necessary. A simple "U" shape heat sink made from 3 square inches of 18 gauge aluminium is mounted on the power board to accommodate the AD161 regulator transistor. It was found convenient to mount the high voltage rectifier on the transformer shroud, otherwise there is room in the bottom of the box between the circuit board and mains switch. Wiring is straightforward with the connections clearly shown in Figure 5-3.

If the crystal controlled frequency reference is to be used, it should be mounted on a circuit board not exceeding 2½ x 4 inches, and inserted in the box at the place shown in Figure 5-3. The counter-timer will only require the 100 Hz output,

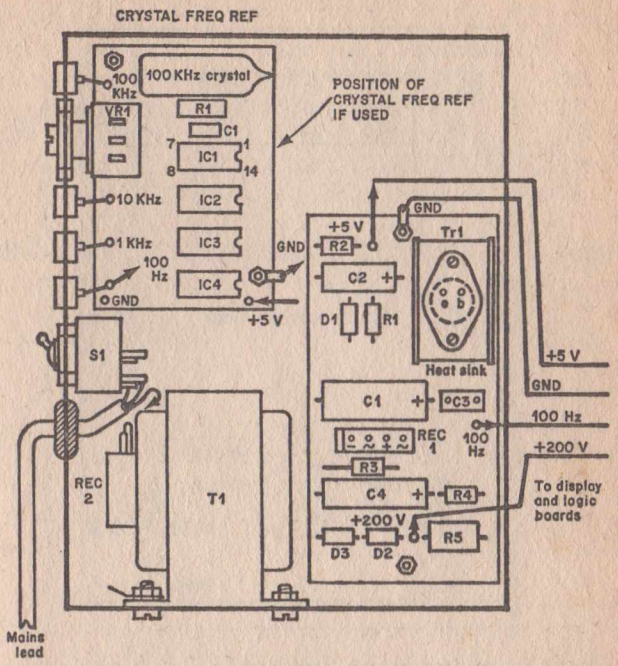


FIG. 5-3. POWER UNIT LAYOUT

but the higher frequency outputs can be made available via wander sockets let into the adjacent side of the box, along with the frequency adjustment potentiometer which should be protected by a suitable cover or locking device.

The front panel layout, drilling template, and relative positions of the circuit boards and indicator tubes, are shown in Figure 5-4 and Figure 5-5. Once the panel is drilled, it may be covered with self-adhesive vinyl sheet. Next, the display window is "glazed" with red acetate sheet, cut 3/8 inch all round larger than the window to provide a gluing edge. Finally, the switches, sockets and "Overspill" indicator lamp are fitted.

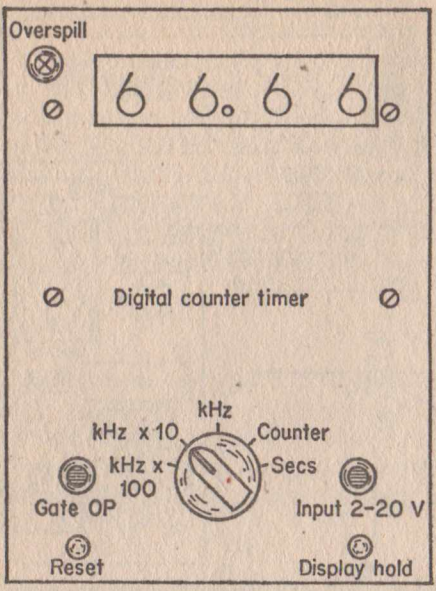
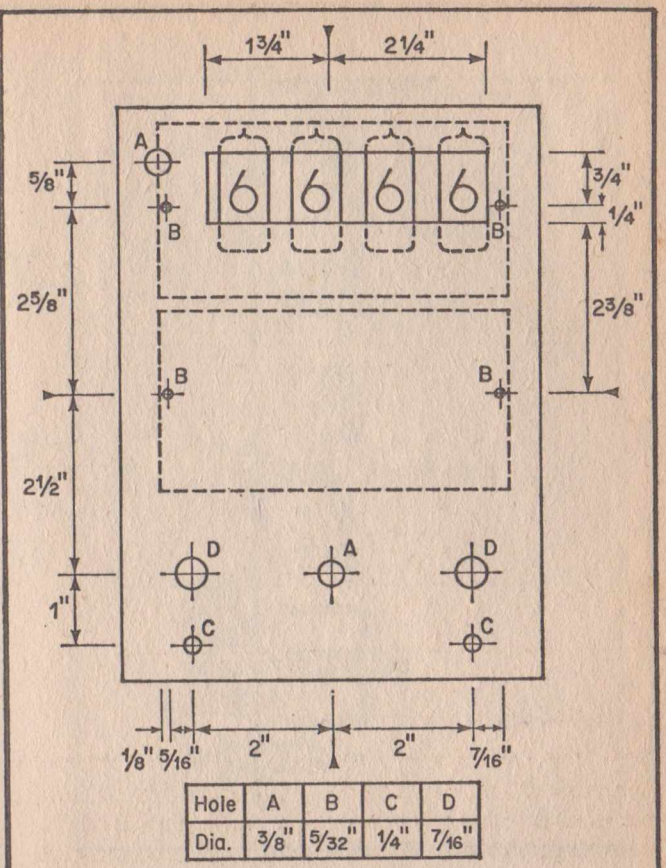


FIG. 5–4. FRONT PANEL LAYOUT

Separate 0.1 inch matrix Veroboards measuring 5 x 2½ inches are used for the display and logic boards. The method of mounting is shown in Figure 5-6, and it will be seen that the copper strips are uppermost when the front panel is laid face downwards. The components, including the ICs, are mounted on the insulated side before the boards are fitted to the front panel. This method leaves the stripped side accessible for wiring and testing. Before mounting the components, however, the copper strips must be interrupted at appropriate points to prevent unwanted connections (see Chapter 1). Also, holes are required to accommodate the fixing bolts and indicator tube connecting leads. Remember that these leads will have to be covered by plastic sleeving.



Hole	A	B	C	D
Dia.	3/8"	5/32"	1/4"	7/16"

FIG. 5-5. FRONT PANEL TEMPLATE

The indicator tubes are secured to the display board by their leads and a simple wire twist around the top pinch. It is well to identify and mark the leads at this stage. The order of the connections is shown in Figure 5-7. Start by first identifying the lead to numeral "6" which is visible through the face of the tube. The IC pin numbers shown in Figure 5-7 are a mirror image of those normally seen in data sheets because

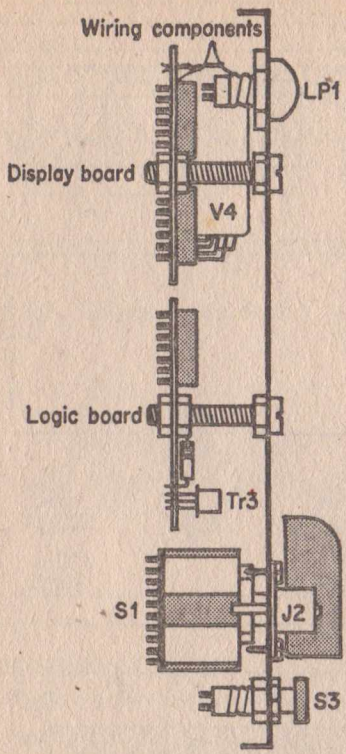


FIG. 5-6. FRONT PANEL SIDE VIEW

the pins in this case are being viewed from below the device. The other components are shown conventionally.

With all their components mounted and the connections clearly identified, the boards can be mounted to the front panel. One inch 4BA bolts are used with spacer nuts arranged so that sufficient room is left between the boards and front panel to accommodate the indicator tubes. Note that the two centre strips are at ground potential and coincide with the fixing nuts and bolts.

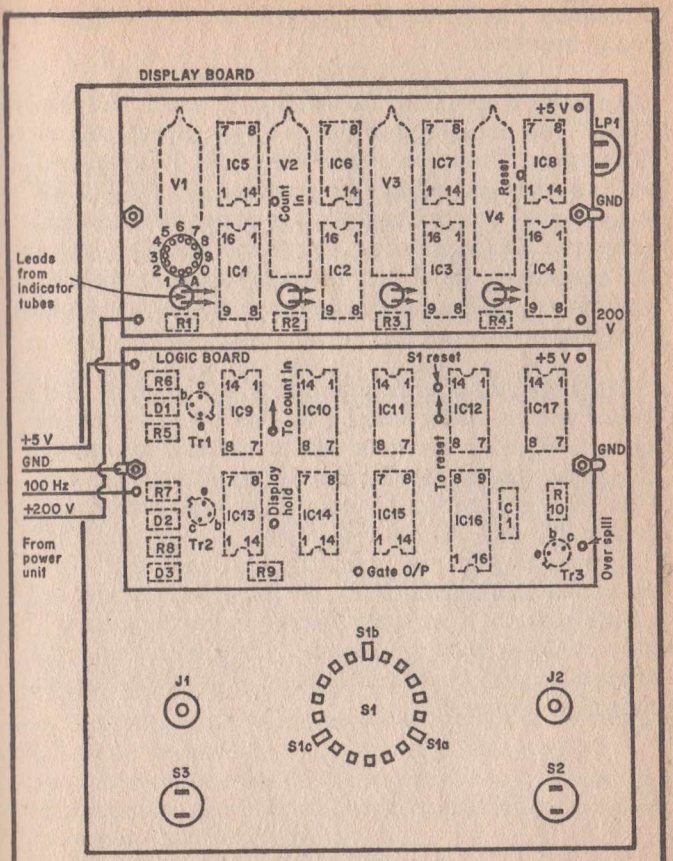


FIG. 5-7. REAR VIEW OF FRONT PANEL

It is impracticable to provide a full wiring diagram, but the information given in Figures 5-1 and 5-7 should be sufficient. Interconnecting links are by single-strand plastic-covered tinned-copper wire. Unless Veropins are used, it is easier to solder the links direct to the component leads and pins rather than via the copper strips. Connections to the range switch are shown by Figure 5-7 in simplified form. If a multiwafer switch is used, care should be taken to identify the correct

switch tag. Finally, the power, ground and 100 Hz signal rails can be connected.

Once wiring is completed the unit may be tested. Switched to "SECS", the display should change by one decimal digit every 0.1 seconds. The action of the "Reset" and "Display-Hold" buttons are best checked on this range. The "COUNTER" range may be checked by feeding in pulses from a suitable pulse generator, logic test set, or a simple DC supply such as a 3 volt battery. Finally, the frequency ranges can be checked against a reliable frequency source such as a crystal controlled oscillator.

Fault finding is not difficult provided it is approached in a logical fashion. After ensuring that the power supplies are correct, all other functions can be checked separately. Remember that for NAND gates to open all inputs must be "hi". For instance, if the counter function does not operate, it is possible that the potential on pins 1, 2, 4 of IC9 is "lo". Try connecting the pins in turn to the 5 volt rail ("hi") to determine the incorrect circuit. By using this technique and a little patience, it is usually possible to locate incorrect connections or faulty components. Take care, however, not to introduce test signals greater than 5 volts DC or AC peak, other than through J1.

Chapter 6

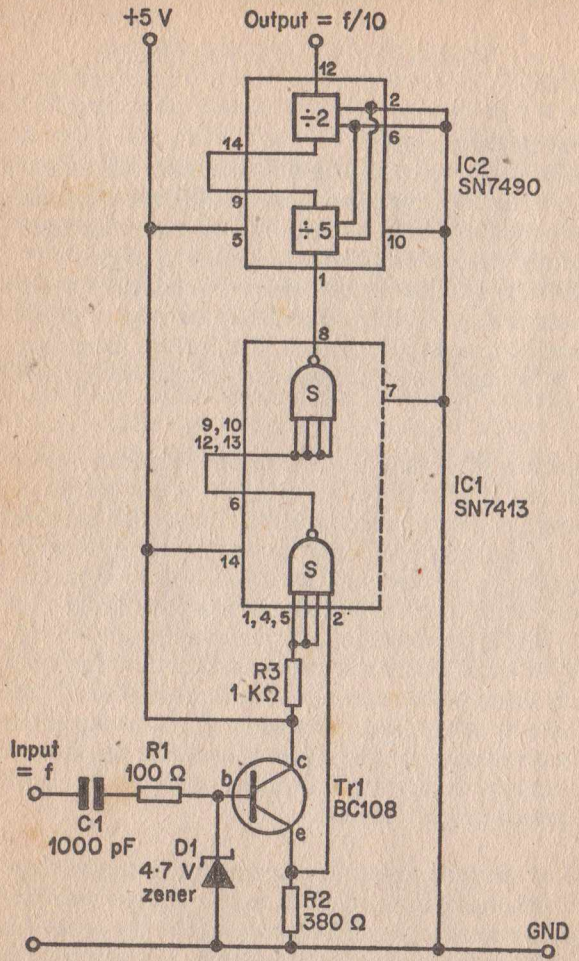
USING THE COUNTER-TIMER

Frequency Measurements

The highest frequency indicated by the counter-timer is 1 MHz. That is when the reading just exceeds 999.9 kHz and settles at 000.0 with the "Overspill" lamp lit. Of course the same indication will occur at 2 MHz, 3 MHz, etc. so that it is theoretically possible to determine with reasonable accuracy frequencies above 1 MHz provided that the order of the frequency being measured is known. The limiting factor, however, is the input stage gain which is virtually useless above 3 MHz.

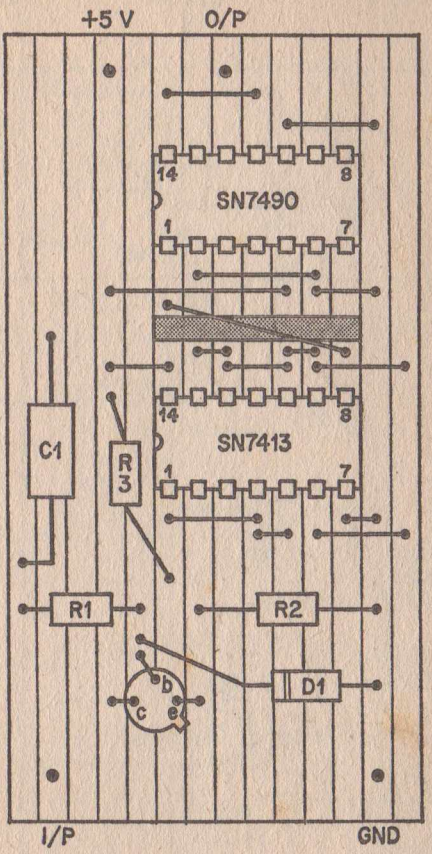
The adaptor shown in Figure 6-1 enables frequencies between 1 MHz and 10 MHz to be measured with greater confidence. It consists of an isolating capacitor C1, protection network R1 and D1, and emitter-follower transistor feeding a double Schmitt-trigger in cascade. This is followed by a decade-counter which divides the input frequency by ten so that 9.999 MHz is presented to the counter-timer as 999.9 kHz. It may be considered worthwhile to include this as an input stage in the main instrument, in which case suitable switching will have to be provided. Alternatively, if it is required to frequently monitor a high frequency oscillator say, the oscillator can have the adaptor built-in and connected to a suitable "Frequency Check" terminal.

Some of the more expensive communication receivers are fitted with digital tuning dials. Normally it is not practicable to directly measure signal frequency and so the counter is connected to the receiver local oscillator. This relates to the signal but with a displacement depending on the receiver i.f. The problem may be overcome by starting the count, not from zero, but from a figure representative of either the i.f. or its complement, depending on whether the receiver local oscillator frequency is below or above that of the signal. Unfor-

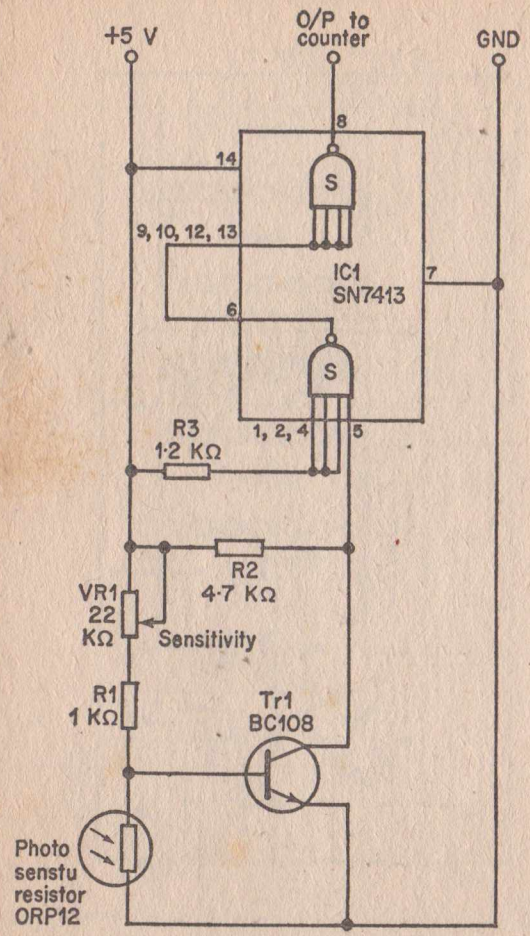


CIRCUIT DIAGRAM

FIG. 6–1. ADAPTOR TO EXTEND THE COUNTER–TIMER TO 10 MHz

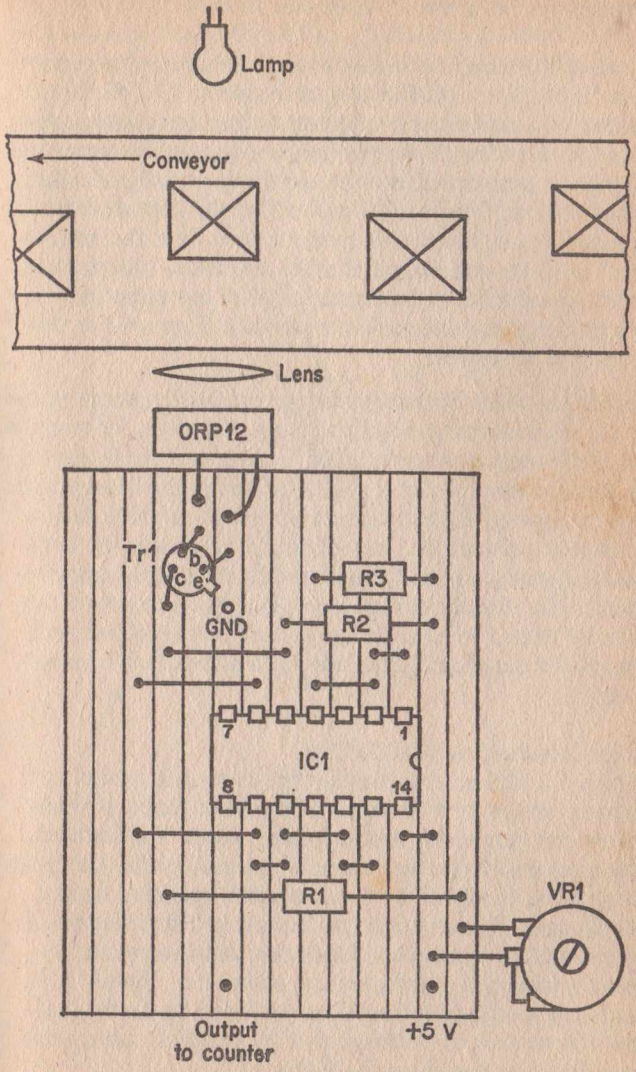


PRACTICAL LAYOUT



CIRCUIT

FIG. 6-2. OPTO-COUNTER ADAPTOR



PRACTICAL LAYOUT

tunately, this technique is difficult to arrange with the counter-timer described in this book.

A possible alternative to direct receiver frequency measurement is to use a digital hetrodyne wavemeter. This simply consists of a stable oscillator connected to the counter, and tuned so as to "beat" with the received signal. The wavemeter frequency is measured, and hence, that of the signal. Care must be taken, however, to ensure that the measurement is not confused by harmonics, spurious beats from the receiver local oscillator and second channel detection. The method and its drawbacks can be demonstrated at low radio frequencies by using the pulse generator shown in Figure 4-5 as the hetrodyne wavemeter.

A problem which does arise when measuring frequency relates to the signal waveshape and amplitude. Suppose, for example, that it is required to measure the frequency of ripple appearing on top of a low frequency pulse. Unless the ripple amplitude is comparatively large, the counter tends to measure the low frequency pulse only. One solution is to display the composite signal on an oscilloscope and use the counter-timer to measure the timebase frequency. The timebase period can then be related to the relevant part of the waveform with reasonable accuracy. Alternatively, a high-pass filter may be tried.

Pulse-Counter Unrelated To Time

Figure 6-2 illustrates a simple opto-electronic set-up for counting items on a conveyor belt. Other forms of transducers can be used for similar measurements. For instance, the number of revolutions made by a wheel can be determined from pulses produced by a microswitch operating from a simple cam. Sometimes it can be arranged that the wheel revolutions are related to distance so that the counter is actually displaying yards, metres, miles, etc. Usually it is necessary to clean up the pulses produced by mechanical transducers such as microswitches by using an anti-bounce circuit such as that shown in Figure 4-8.

Revs-Per-Minute

The techniques just described can be used to measure rpm by simply noting the number of pulses counted in one minute. This can be tedious, and so another approach is to make the rotor produce 60 pulses during one revolution, when rpm also becomes pulses-per-second and can be measured as frequency. This has the advantage of speeding up the measurement period so that the effect of any adjustment can be quickly noted. A

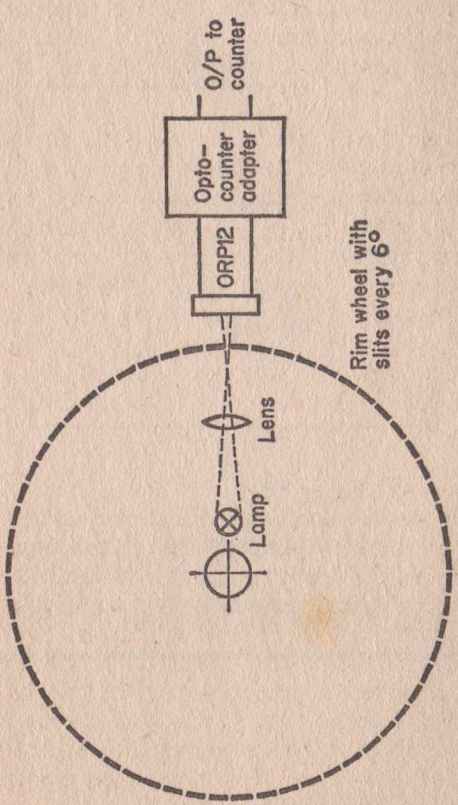
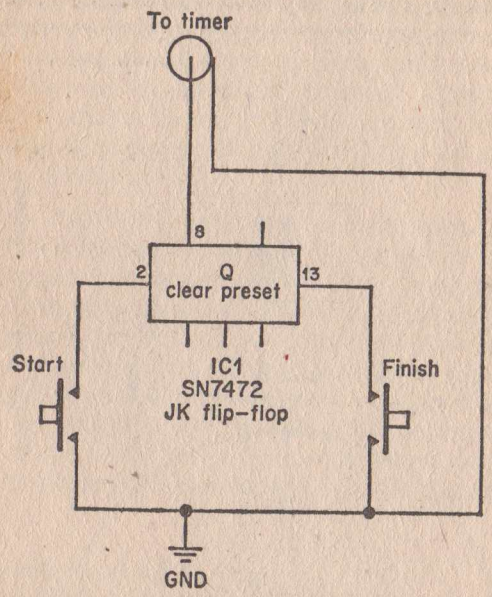
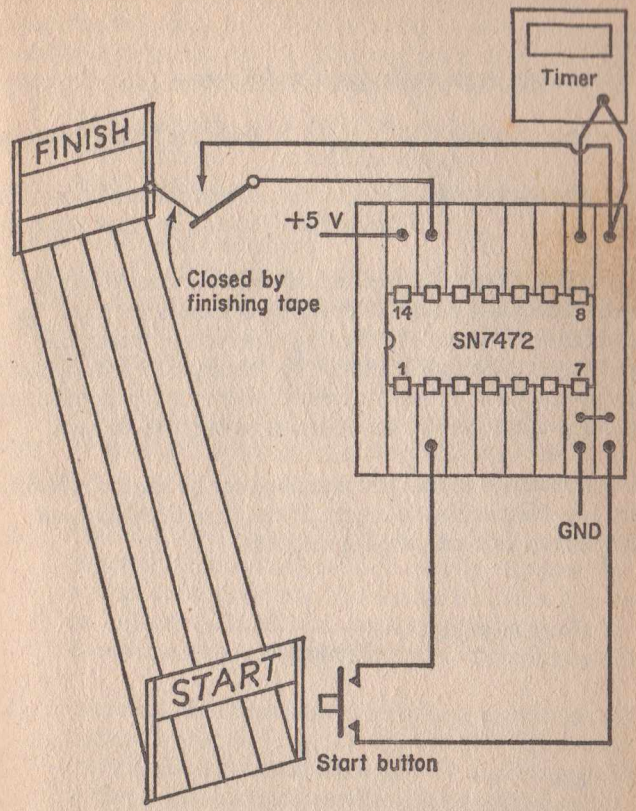


FIG. 6-3. REV-COUNTER



CIRCUIT

FIG. 6-4. REMOTE CONTROL OF TIMER



PRACTICAL LAYOUT

suitable system is illustrated in Figure 6-3, with the photo-cell connected to an input circuit similar to that shown in Figure 6-2.

Timer

Processes can be manually timed as follows:—

1. Process starts ..... Press the "Reset" button.

2. Process completed..... Press and hold down the "Display-Hold" button and read the time.

Figure 6-4 illustrates a method of remotely controlling the timer. The J-K flip-flop is latched so as to hold the input "hi" and inhibit the timer. At this stage the counter is manually reset to zero. Timing is initiated by pressing S1. This latches the flip-flop "lo" until S2 is pressed, when the flip-flop latches "hi" and again inhibits the timer, allowing it to be read.

Similar methods to that just described can be used to measure very low frequencies and rpm. If the time taken for one complete cycle is measured in seconds:—

$$\text{Frequency (Hz)} = \frac{1}{\text{Time (Secs)}}$$

$$\text{rpm} = \frac{60}{\text{Time (Secs)}}$$

The measurements just described require the timer to be manually reset to zero before making the next measurement. A remote reset facility can easily be provided by simply fitting suitable terminals across the "Reset" button (S2 in Figure 5-1).

Some experimenters may wish to extend the timer facilities by providing two extra ranges. The unit as shown in Figure 5-1 uses switch-wafer S1c to select 10 Hz from pin 11 of IC14 to

provide 0.1S pulses. 1S pulses can be similarly obtained from pin 11 of IC15, and 0.01S pulses from pin 14 of IC14. In the latter case, it is desirable to arrange for switch-wafer S1a to select decimal point dp3. Both new ranges will require switch-wafer S1b to ground pin 5 of IC10 and pin 8 of IC16. The maximum display reading for each range will then be:–

99.99 Seconds	in 0.01S increments
999.9 Seconds	in 0.1S increments
9999 Seconds	in 1S increments.

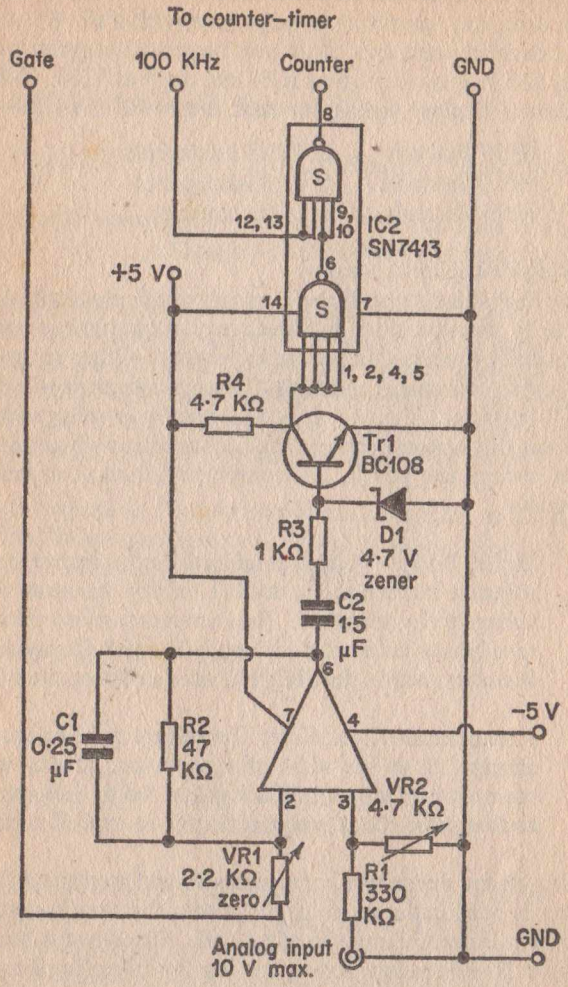
Analog-To-Digital Converters

Basic digital instruments are counters which can easily be made to measure time and frequency because these are electrically processed in precise increments. Other parameters are not so convenient and normally require an analog-to-digital (AD) converter. The analog input is usually in voltage form, because this is readily derived from quantities such as resistance, current and power. AD converters fall into two main groups:–

1. Digital Bridge: Voltage produced by the instrument is adjusted incrementally until it exactly balances the voltage to be measured. The increments relate directly to a binary code which is applied to the display via decoders such as the SN74141 used in the counter-timer.

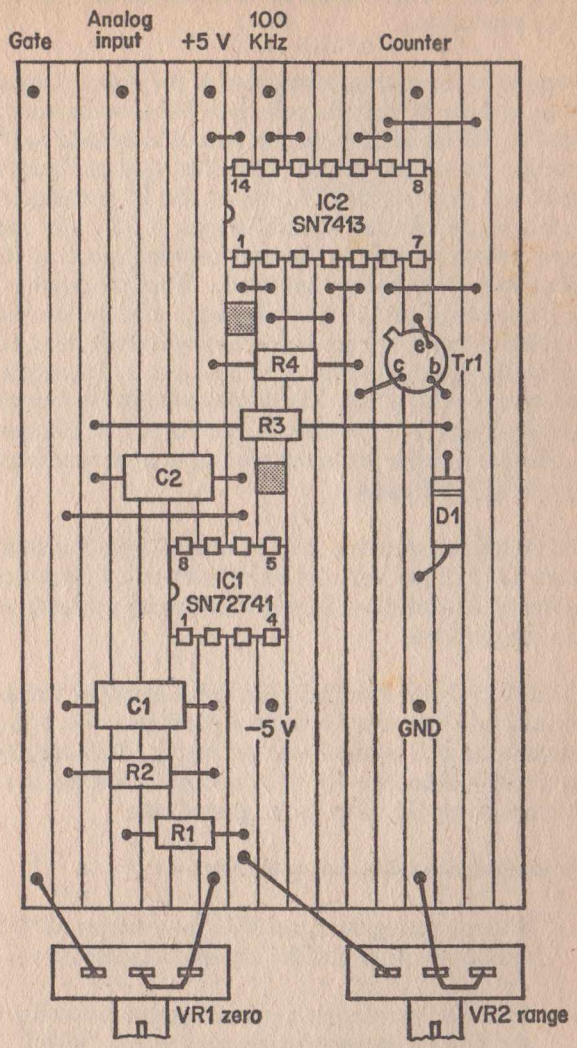
2. Proportionate Clock Gate: The voltage to be measured is arranged to set the width of a gate pulse. This in turn controls the number of clock pulses fed to the counter, so that pulse count is proportionate to applied voltage.

Although the design of a comprehensive and accurate AD converter is outside the scope of this book, the simple circuit shown in Figure 6-5 may be of interest. Fitted to the timer-counter it will produce a two digit display indicating 0 to +5 volts in 0.1V increments. This could be increased to three digits and 0.01V increments by injecting 100 kHz clock-pulses into IC2 instead of the 10 kHz shown, but then the decimal point would be in the wrong place. In any case, the linearity



CIRCUIT

FIG. 6–5. A SIMPLE A–D CONVERTER



PRACTICAL LAYOUT

and accuracy of the circuit are not compatible with three figure resolution.

To operate, the counter is switched to the highest frequency range so that a 10 mS gate pulse is available to the inverted input of IC1 via VR1. Here, the pulse is integrated by C1 to produce the wedged shaped pulse illustrated in Figure 6-5 insert, and then fed via TR1 inverter, and D1 protection and dc restorer, to the first Schmitt-trigger in IC2. The analog input voltage applied to the non-inverting input of IC1 effectively sets the wedge amplitude. When the input is low, only the narrow part of the wedge projects above the Schmitt threshold potential to produce a narrow output pulse, but as the analog input is increased, so does the wedge amplitude and output pulse width. The output pulse fed to the second Schmitt-trigger in IC2 is used to gate the 10 kHz clock-pulses, causing the number fed to the counter to be proportionate to the analog input voltage.

The 10 kHz clock-pulses may be derived from the counter-timer if it is fitted with the crystal controlled frequency reference illustrated in Figure 4-6; otherwise a separate source must be provided.

The SN72741 is a standard operational amplifier which is obtainable in several styles as shown in Figure 6-5. It requires a negative as well as positive power supply. Both supplies can be obtained from two 4.5 volt batteries connected in series with the centre tap taken to the ground rail.

The converter is calibrated as follows:—

1. With no analog input, set VR1 for a display of "000.1", then back off so that the display just reads zero.

2. With a known analog input voltage not exceeding +5V, set VR2 for the appropriate reading, e.g. "004.5" (4.5V).

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