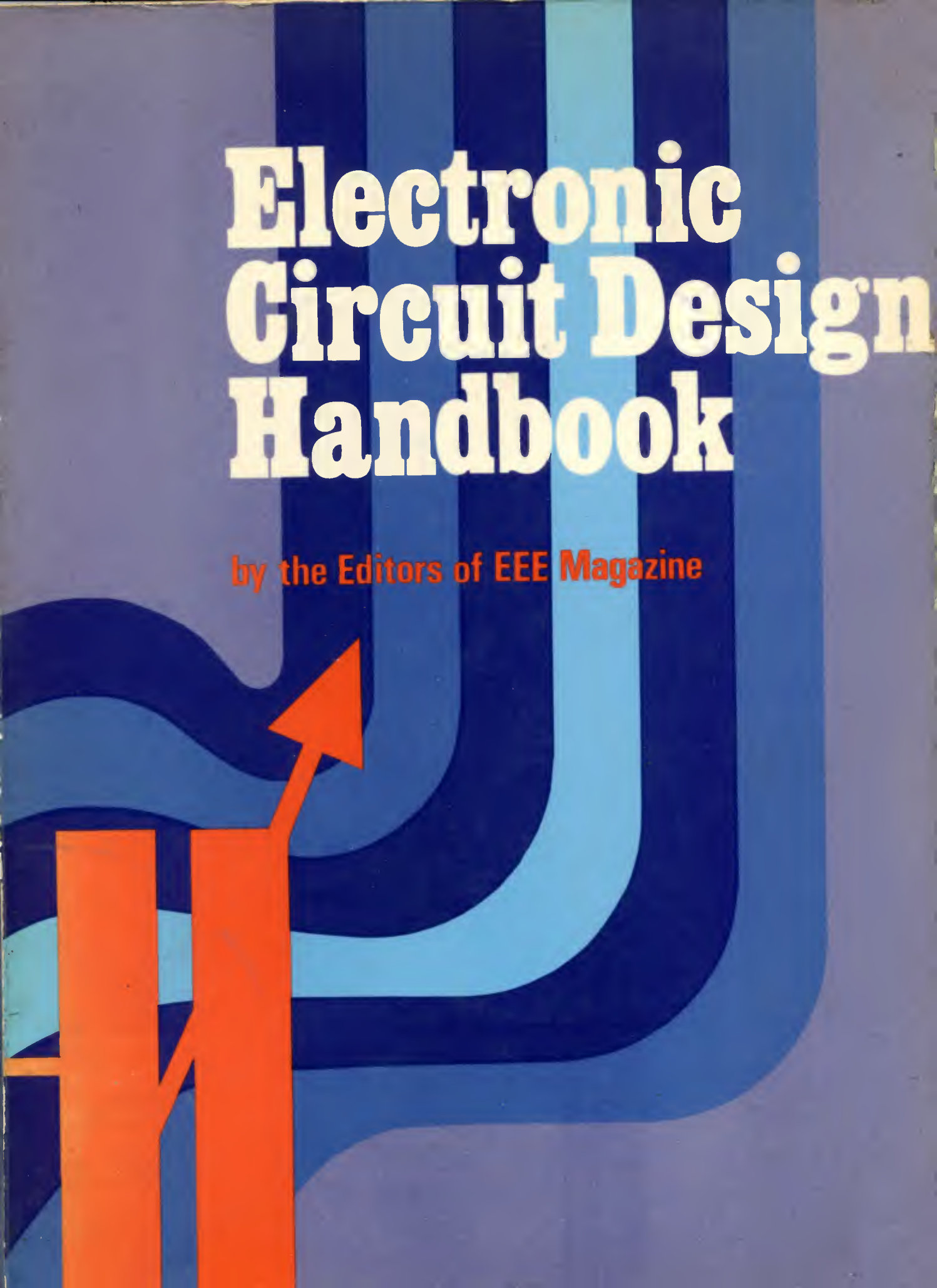
Electronic Circuit Design Handbook

by the Editors of EEE Magazine



Some notes about this scanned book.

1.
Due to poor print quality of the original diagrams, scanning proved difficult and the following four diagrams have been redrawn using EasyPC CAD software.
They are to be used in conjunction with the original associated text.

2.
In the main body of the book.
A few scanned pages have annotations added to help with reading circuit values etc.

No guarantees can be given to the accuracy of these annotations due to poor original print quality.

3.
Use of the zoom facility available in most Acrobat .pdf document readers will help to view component values.

4.
A small number of original pages had print quality too poor to make out the values.
Any suggested values are left to the reader to try out or pick a value they think works best.

Page 111.
Fig. 2.
Full range PWM circuit uses UJT combined with standard S-R flip flop.

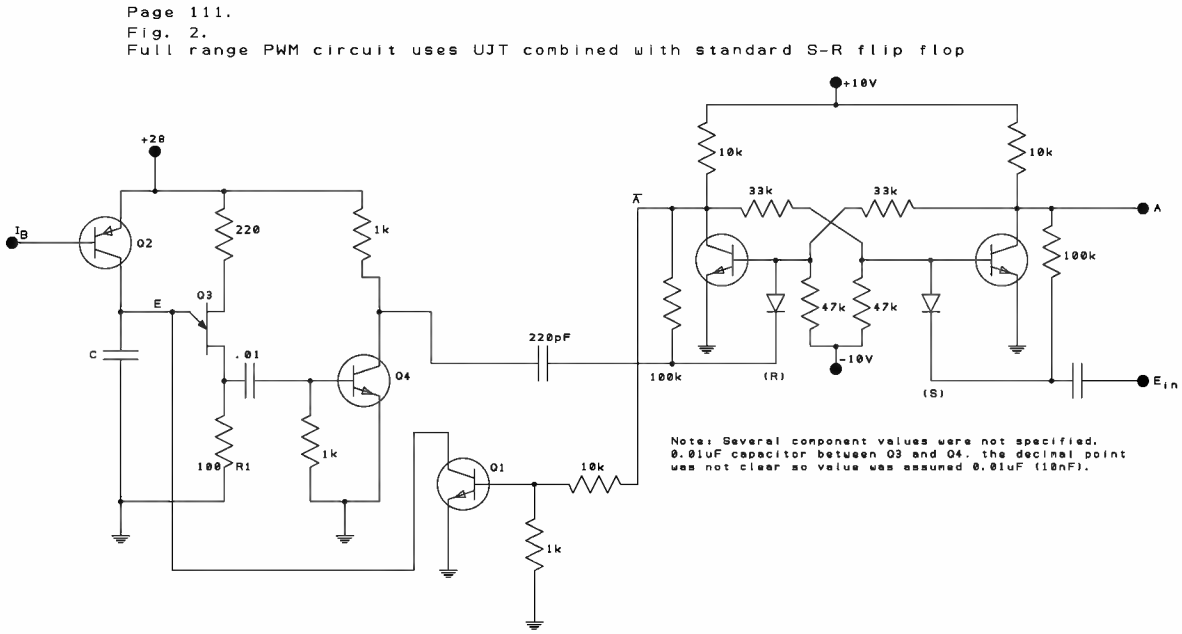


Fig. 2. Full-range PWM circuit uses UJT combined with standard S-R flip flop.

Page. 111
Fig. 1.
Trigger Circuit Gives Less Pdiss, More Vout.

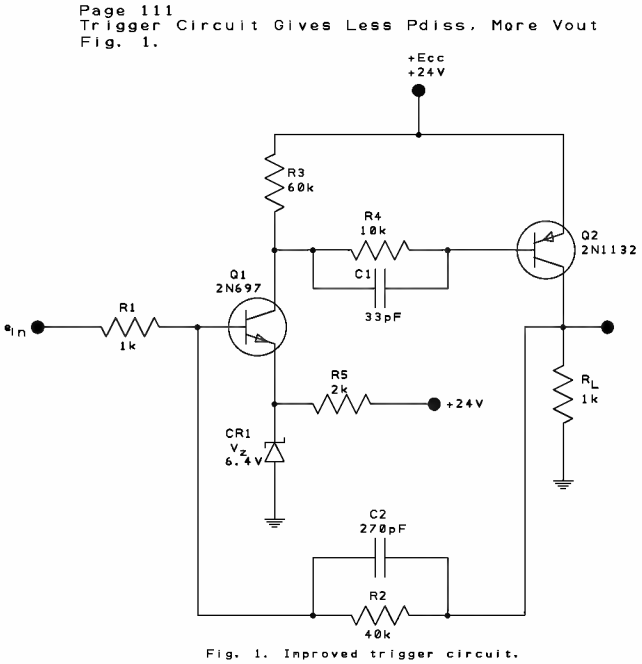


Fig. 1. Improved trigger circuit.

Page 331.
Figure 1.
Relay BCD – to – decimal converter

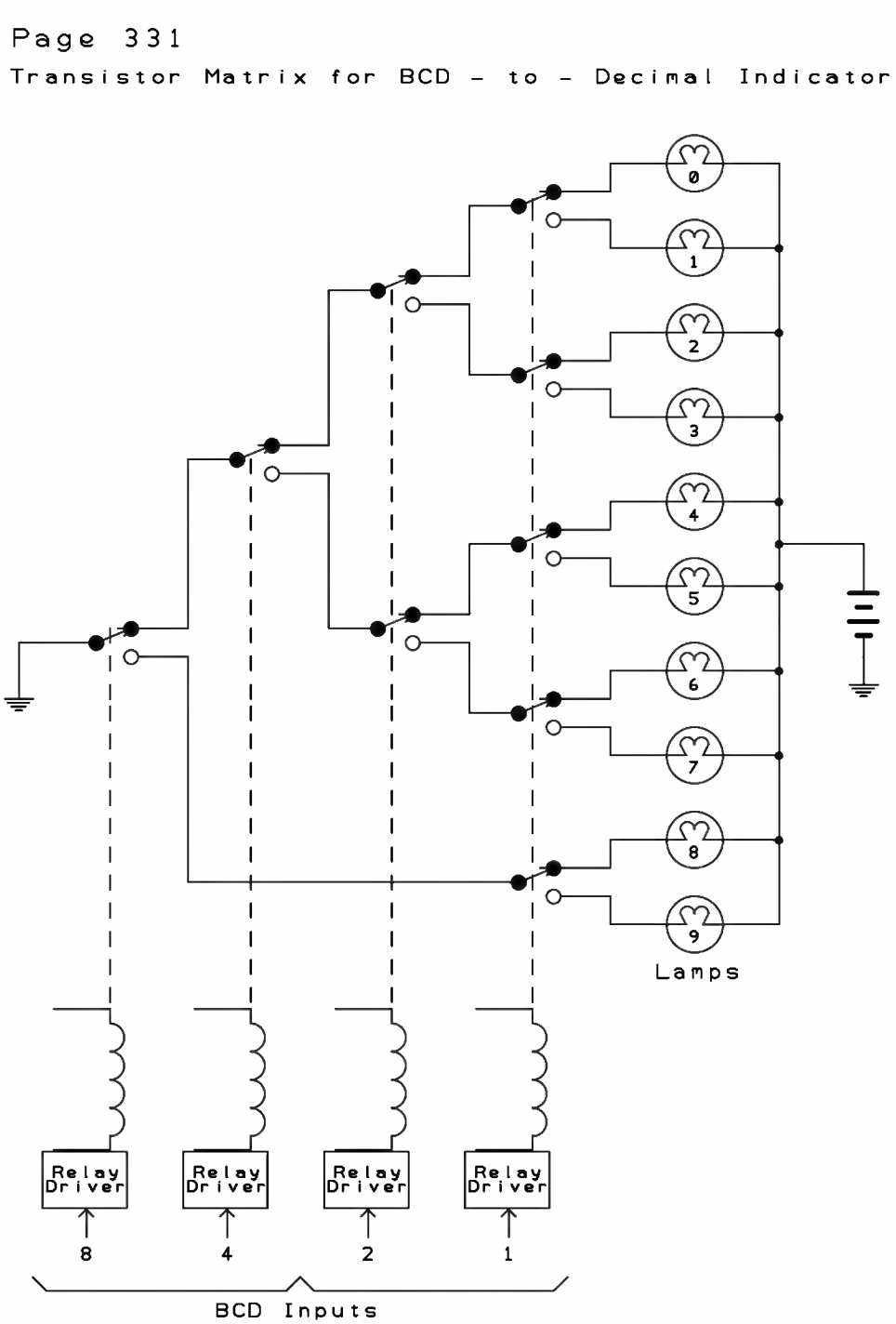


Fig. 1. Relay BCD-to-decimal converter.

PAGE 406

Pulse-height Modulator multiplies voltage by frequency

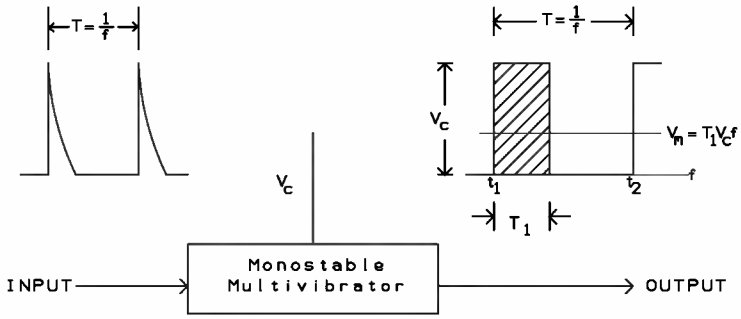


Fig. 1. Voltage-controlled one-shot multivibrator gives output pulses of constant width and variable height. Total period T is the reciprocal of input frequency, threfore mean output voltageis proportional to the product of f and Vc.

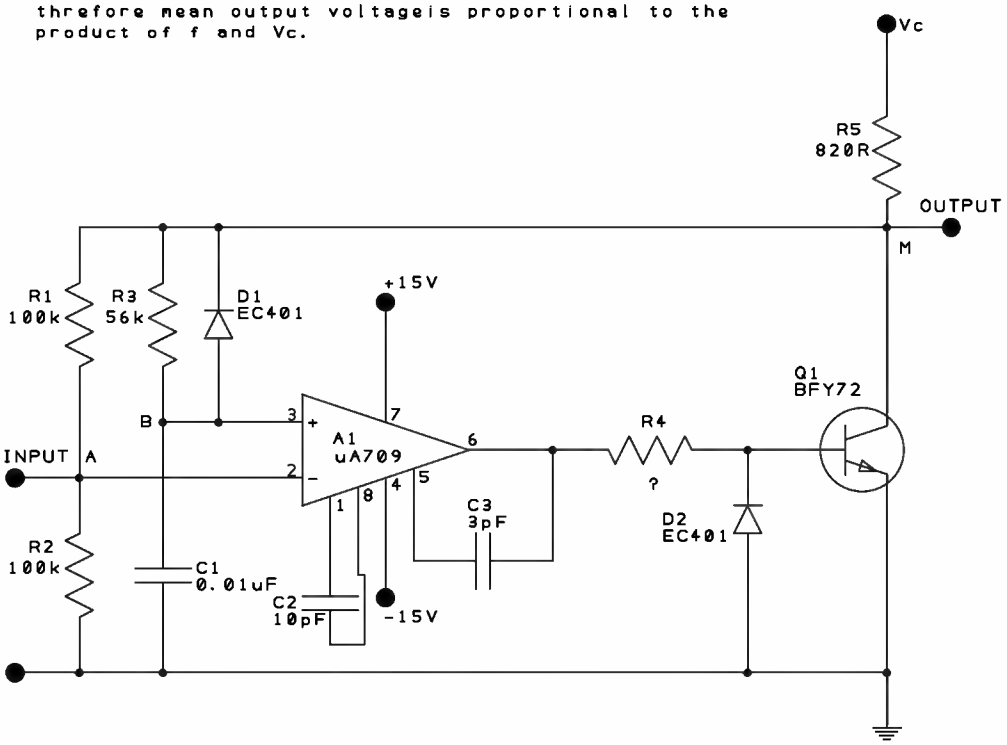


Fig. 2 This practical circuit accepts input frequencies from 1Hz to 1kHz and control voltages from 0.1 to 15 V. Note that voltage balance between points A and B doesn't depend on Vc.
Therefore pulse widthdepends only on the values of R3 and C1.

Page 406: Pulse-height modulator multiplies voltage by frequency
The value for R4 was not specified.
Data sheet for EC401 diodes not found, probably not critical.
The NTE116 diode may be a substitute (600V 1Amp diode).
Many other silicon rectifier type diodes should substitute OK.

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With a specially written chapter for the guidance of the English reader by W. Oliver

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The colour coding of American mains leads, for instance, is quite different from our own; and if you are involved in the use of these, you must make sure by checking both ends of the leads from an appliance to identify each lead beyond all possible doubt before connection is made or the plug inserted into the mains outlet point or socket.

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Moreover, sticking too slavishly to working drawings or detailed layout designs may tend to handicap the beginner by discouraging initiative and the ambition to plan his own designs. Using a book such as the present one compels the beginner to think and plan for himself where practical construction is concerned; and this, in the long run, is of the utmost value—though, in the early stages, it may occasionally cause some delays, disappointments or even minor disasters, through learning the hard way!

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through placing any components which are vulnerable to these effects in too close proximity to one another, or incorrectly orientated; and risk of overheating through lack of adequate spacing or ventilation for certain components which tend to run warm or even hot.

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The question of safety looms large where beginners are involved. With projects powered entirely by low-voltage dry batteries (an inherently safe form of energy), no problem is likely to arise. But mains-powered projects are in a different category altogether. With mains there is always, lurking in the background, some element of danger. It can be a slight potential risk in cases where every reasonable precaution is taken; or it can be a downright lethal hazard if anyone goes to the opposite extreme and is utterly foolhardy. In general, although (contrary to popular belief) it is current rather than voltage which kills, the two are so inseparable that, in actual practice, one must act on the assumption that the higher the voltage the greater the risk, in most cases.

For this reason, and one or two others, British mains (running at 240 VAC 50 Hz) must be treated as more dangerous than American mains (usually running at 110–120 VAC 60 Hz, but with an alternative supply in some cases which offers twice that voltage).

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Preface

While many of us may be reluctant to admit it, most modern electronic circuits are patterned after existing designs. A generation ago the minds of men like Eccles and Jordan, Wheeler, Hazeltine, Black, Schmitt, Hartley, Armstrong, and others developed the basic designs for many of today's circuits. Yet, even today, truly original circuits, bearing almost no resemblance to anything previously developed, occasionally reach the light of day. For the most part, however, the majority of new circuits are modifications of previous designs.

It is indeed fortunate that we do not slavishly worship a cult of originality simply for the sake of originalty. How wasteful it would be of our nation's engineering talent if we repeatedly re-invented the Schmitt trigger, the blocking oscillator, or the flip-flop. In truth, our progress can be measured in how successfully we can stand on each other's shoulders. Previously designed circuits are continually modified, refined, and improved as engineers adapt them to their specific needs. This is genuine progress.

This volume is a collection of circuits originally published in EEE magazine. The circuits were selected for their originality, novelty, or sophistication—but most of all, they were selected for their usefulness. These award-winning circuits can be used as building blocks in designing circuit configurations best suited to your needs. Most importantly, however, these circuits will serve as imagination triggers, stimulating you to think of more efficient designs for specific applications.

In this expanded Fourth Edition, 639 individual circuit designs are included, arranged as much as possible by function and applications. Of course, many circuits serve a multitude of functions and can serve in a myriad of applications. Some control circuits, for example, can also be classed as sensing or detection circuits. Many multivibrators described in the Pulse Circuits Section are also oscillator circuits. Thus, when seeking a circuit for a specific function, you'll find scanning the Contents pages the easiest way to locate the most applicable designs.

This book is the answer to the long-felt need for a one-source handbook of tried-and-tested circuits. It is also the answer to thousands of requests from readers of EEE, who virtually demanded that these circuits be published in book form.

The Editors

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Section 1
CONTROL CIRCUITS

A Reliable Open Loop Amplifier

BY REPLACING the conventional closed loop with a semi-open loop configuration, the reliability of this differential dc amplifier has been greatly increased. In a semi-open loop approach, the active elements of the circuit are controlled by individual closed loops, permitting the gain characteristics to be determined by passive elements. Further improvement in reliability has been accomplished by reducing the number of components normally required for circuitry to provide the operating characteristics of this type of instrument.

The semi-open loop approach provides important features not possible with the closed loop method: isolation of the input from the output and a higher degree of filtering. The isolation of the input from the output offers several advantages including constant impedance level independent of the slewing rate of the amplifier and the absence of a unidirectional input current. Multipole filters with limiting slopes greater than 12 db per octave can be inserted internal to the amplifier and are completely isolated from the signal source and load effects.

The amplifier circuitry involved in the semi-open loop approach is shown in block diagram form in Fig. 1.

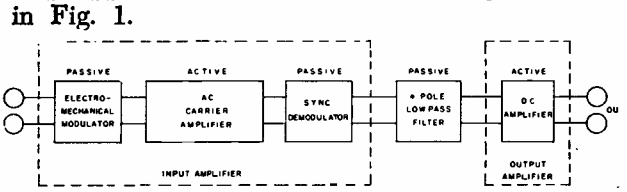


FIG. 1—Arrangement of stages of open loop amplifier.

As shown in Fig. 2, input switch S_{101} is driven at a sampling rate of 400 cps. The input signal is impressed between the switch arm and the center tap of the input transformer. The modulated input signal is magnetically coupled to the ac carrier amplifier by the secondary of T_{101}, and is referenced to the amplifier common. Isolation necessary to achieve high common mode rejection is established at the input by transformer coupling and electrostatic shielding.

The unity gain amplifier Q_{101}, Q_{102}, effects a high impedance transformation ratio to prevent loading of the input transformer, and provides a low source impedance to the gain attenuator S_{102}.

The loading of the unity gain amplifier, referred to the primary of the input transformer, is negligible; therefore, the input impedance of the total amplifier is determined by the half-primary impedance of the input transformer at the carrier frequency of 400 cps. This value is always greater than one megohm and is independent of the amplifier's operating condition. Thus, the input circuitry provides a well isolated true differential input at a constant impedance level.

The gain attenuator S_{102} varies the overall gain of the instrument in fixed steps. Stability is assured by precision wire wound resistors.

A fixed gain amplifier (Q_{103}-Q_{108}) is completely enclosed in feedback to insure gain stability.

A multi-turn, high resolution trimming potentiometer R_{159} is provided in the feedback network to serve as a fine gain vernier. This control is accessible through the front panel for screwdriver adjustment and allows the user to trim the amplifier gain to a high degree of precision. The output of the fixed gain amplifier is transformer coupled to the second section of switch S_{101} to achieve synchronous demodulation. The demodulated signal is presented to an appropriate filter and appears at the filter output as an accurate reproduction of the input signal. This signal is presented to the dc amplifier to terminate the filter and provide ample power gain and output characteristics consistent with the loads commonly incurred in data acquisition systems.

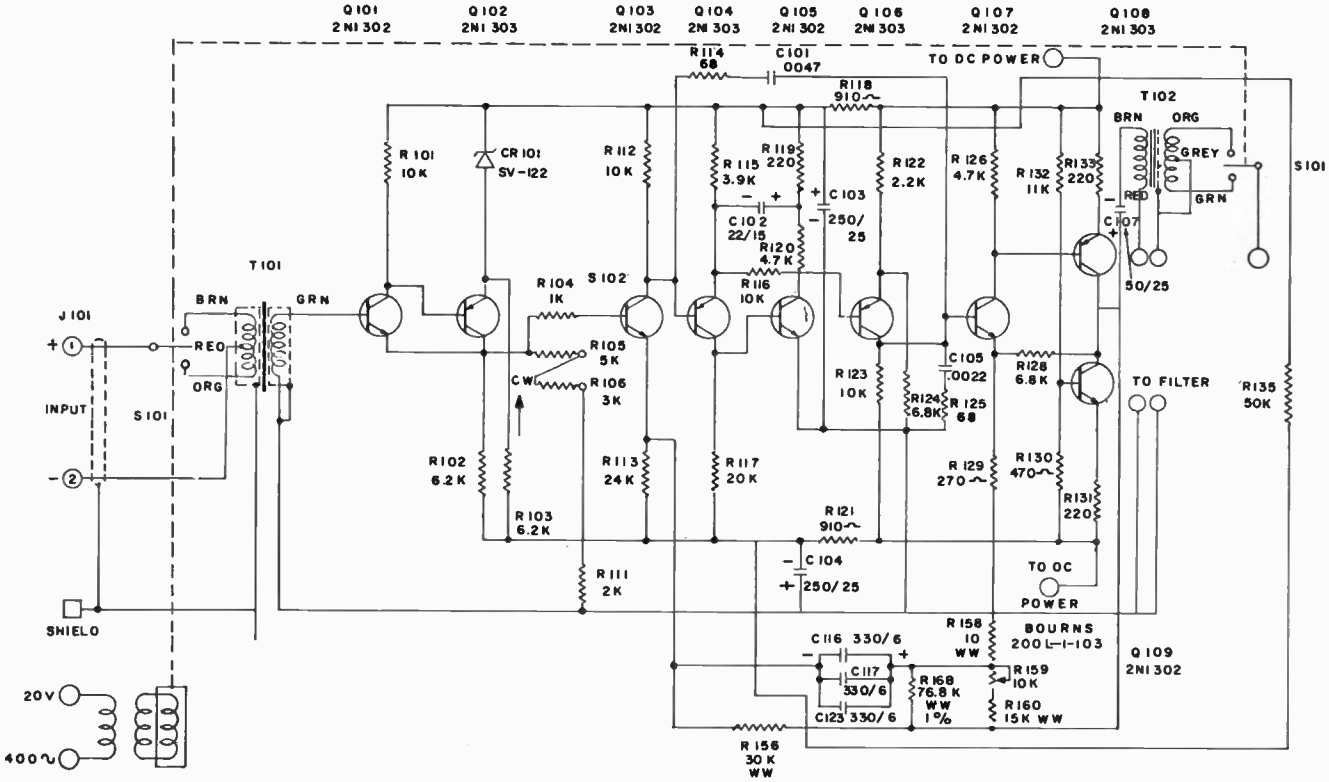
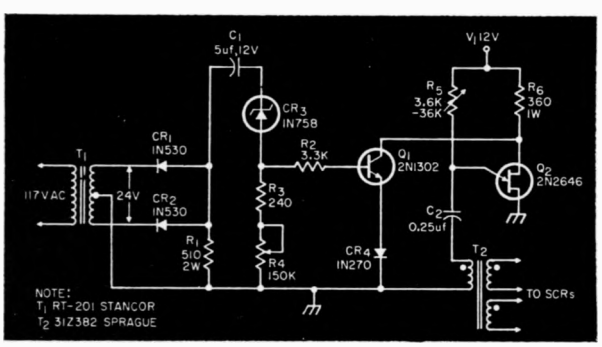


FIG. 2.—Complete circuit of open loop amplifier.

Zero-Crossing Sync Circuit For SCRs

WHEN SCRs are used to control the ac power delivered to a load it is necessary to fire the SCRs at some selected point on the input sine wave. To do this, the SCR firing circuit must be synchronized with the zero crossing points of the sine wave to initiate a new timing cycle at each zero crossing. This synchronization can be done with the circuit shown.



Zero-crossing sync circuit.

C_2, Q_2, R_5, R_6, and T_2 comprise the usual SCR firing circuit. Resistor R_5 may be any control device, from a simple potentiometer to a servo control system.

To synchronize Q_2's timing cycle so that it will start from each zero crossing, capacitor C_2 must be discharged at each crossing. This is achieved as follows. Transformer T_1 and rectifiers CR_1 and CR_2 form the zero-crossing reference by doubling the 60-cps line frequency to 120-cps pulsating dc. C_1 differentiates this reference voltage and R_1 discharges C_1 at the end of each cycle. Zener diode CR_3 conducts in the forward direction during the negative portion of the differentiated reference cycle, reverse biasing Q_1. As long as Q_1 is reverse biased its effect on the UJT circuit is negligible, allowing Q_2 to cycle at a frequency determined by its circuit values.

However, when the differentiated reference voltage starts to swing positive, CR_3 ceases to conduct and then supplies a positive pulse when its zener voltage is reached. At this point Q_1 becomes forward biased thus effectively shorting Q_2's bases. This causes Q_2 to fire (regardless of the amount of accumulated charge on C_2) thus discharging C_2. R_4 is adjusted so that the breakover point of CR_3 is at the peak of the reference voltage (zero crossing point of the ac sine wave).

The polarities of CR_1 and CR_2 are so arranged that the sharp peaks of the reference voltage are positive after being differentiated by C_1. This provides a precise zero crossing sync pulse at each crossing. R_3 serves as a current limiting resistor to protect CR_3 and CR_4 provides a small emitter bias so that Q_1 will remain in its cut-off state until CR_3 conducts in its reverse direction.

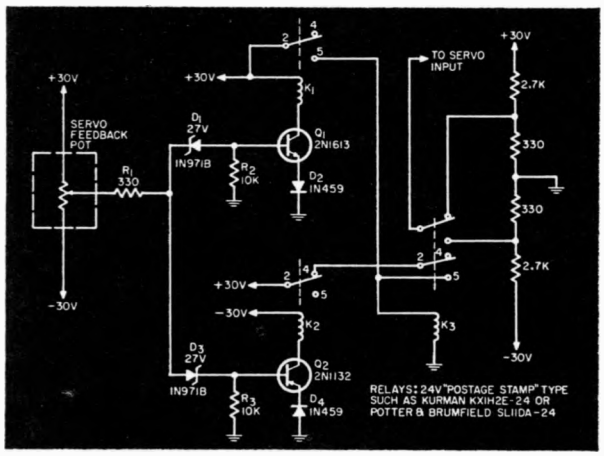
In a temperature control system, this circuit maintained the temperature of a liquid within 0.001°C of the set point within a range of ambient to 100°C. ◆◆

Instrument Servo Cycling Circuit

IT OFTEN IS DESIRABLE to cycle servo units from stop to stop for extended lengths of time to determine such things as wear characteristics and friction level changes. Limit stop switches can be incorporated on larger units, but on instrument servos, this is not practical. However, most of these servos use a potentiometer as the feedback element, and this can be utilized, as shown, to supply the required reversing signal.

With the servo positioned midway between its stops, motor drive is applied so that the pot arm is driven toward +30 v. When the breakdown voltage of D_1 (27 v) is exceeded, it conducts, turning on Q_1. K_1 pulls in, energizing

K_3, and the motor drive reverses. As the pot arm travels toward −30 v, Q_1 turns off, and K_1 drops out, but K_3 remains energized through holding voltage applied to contacts *2* and *5*. As −30 v is approached by the pot wiper arm, D_3 conducts and turns on Q_2. K_2 pulls in, de-energizing K_3, and motor drive again reverses. As the pot arm moves back toward +30 v, Q_2 turns off, K_2 drops out, and the cycle repeats.



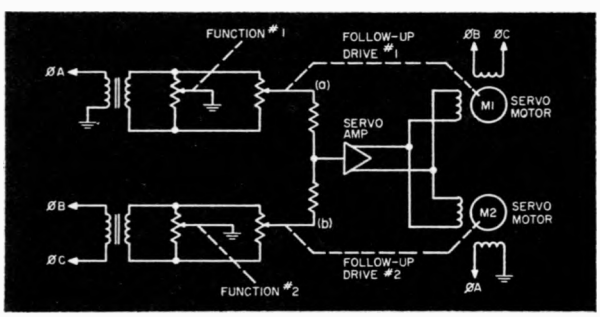
Instrument-servo cycling circuit.

As shown, relay K_3 reverses a dc servo input signal, but it could just as easily reverse the actual motor drive if desired. Similarly, the use of variable supplies and/or zeners with different breakdown voltages allows one to cycle the servo over any portion of its travel continuously. ◆◆

Double-Channel Servo Controls Two Motors

WITH ONLY ONE servo amplifier driving two channels of servo control, the number of electronic parts can be reduced 50 percent. In the block diagram, if the shaft position representing the first signal changes, then a difference will occur between the signal position and its follow-up position. This difference will appear as a voltage at point (a) which is in phase with ϕ_A. This signal voltage will be amplified and appear across the control windings of both M_1 and M_2. However, since M_2 has its fixed-phase excitation from phase *A*, it will not respond to the signal. M_1, however, is referenced to ϕ_B and ϕ_C which is 90 degrees out of phase with the signal. The two-phase servo motor M_1 will, therefore, respond to the signal while M_2 will not. In a similar manner, M_2 will respond only to signals generated at (b) by the second signal circuit because of the phase relationships.

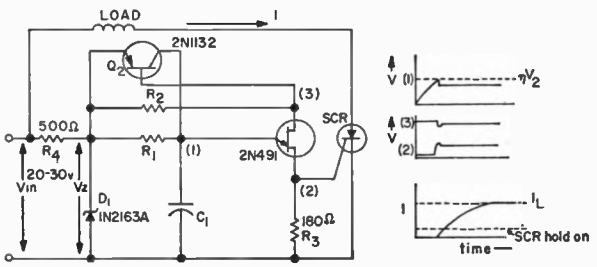
This system serves best for servo loops with low dynamic response since some quadrature voltage is generated in the amplifier when one channel is disturbed. This quadrature voltage, if large enough, can cause a slight shift in the null position of the other channel during the disturbance. In a servo loop with low dynamic response this quadrature voltage is negligible. ◆◆



Two-channel servo system.

Unijunction Latchup for SCR's Driving Inductive Loads

WHEN AN SCR, controlled by a unijunction transistor, is driving an inductive load, it may not turn on. When the unijunction fires, a pulse appearing at the scr gate begins to turn it on. The rate of current rise through the scr is limited by the inductance of the load so there is the possibility that the pulse at the gate may disappear before the load current rises above the hold-on current level of the scr. If this happens, the scr will never turn on.



The unijunction latchup circuit for scr's turning on inductive loads and circuit waveforms.

A resistor across the inductor can eliminate the problem but this wastes power and it may call for a larger scr. A better circuit appears in the figure. When voltage is applied to the circuit, C_1, begins to charge through R_1. When the voltage at the emitter of the unijunction (point *1*) reaches ηV_z (where η is the intrinsic standoff ratio of the unijunction and V_z is the Zener voltage), the emitter is forward biased and C_1 discharges into R_3. The unijunction turns on and the voltage at the base of Q_2 (point *3*) drops instantaneously.

This change in potential turns Q_2 on, forcing a large current into the unijunction emitter. This action holds the unijunction in saturation, causing the voltage at the gate of the scr to be continuous rather than pulsating. R_1 and C_1 are chosen to give the desired time delay from

$$f \approx \frac{1}{R_1 C_1 \ln\left(\frac{1}{1-\eta}\right)}$$

R_2 depends on the desired temperature compensation. It is approximately $0.4\ V_{bb}/\eta V_z$, where V_{bb} is the initial voltage between points *2* and *3*.

Simple Intervalometer

AN INTERVALOMETER, as applied to the control of aerial cameras, generates pulses which cycle the camera at a rate such that the terrain is photographed with a constant overlap. The expression which defines the re-

quired rate is as follows:

$$\text{Rate} = 1.69\ V/H \frac{f}{F} \times \frac{1}{1\text{-}0.01\ (\text{overlap})} \quad ;$$

where, V = velocity of aircraft in knots; H = altitude in feet; f = lens focal length in inches; F = format size in inches; and overlap is in percent.

Although there are several techniques which could be utilized to produce the pulses, it was found that a simple relaxation oscillator would generate the required pulse rate over a wide range to an accuracy of better than 3 percent.

The basic circuit is shown in Fig. 1. The circuit as applied to aerial photography is shown in Fig. 2. A

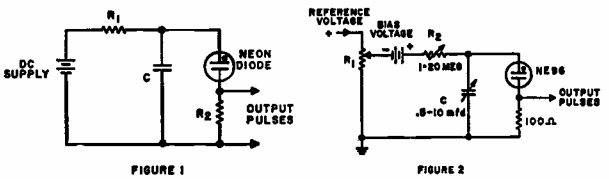


Fig. 1. Basic pulse circuit.
Fig. 2. Actual circuit employed for aerial photography.

dc reference voltage is applied to a potentiometer whose arm would be rotated proportionately to the V/H ratio of the aircraft. This voltage is then added to a bias voltage which is set at just below the minimum firing level of the diode. Resistor R_2 is made inversely proportional to the ratio of f/F, and C is set as a direct function of the factor: 1-0.01 (overlap).

The values given in Fig. 2 for R_2 and C are the ranges within which reliable operation is assured. The magnitude of the reference voltage can be changed to set the scaling of the circuit.

The following experimental data is useful in working out the initial design of this type of intervalometer for a specific application: At a total input of 300 v, an R of 1 meg, and a C of 1 μf, the pulse rate was found to be 3 cps. The frequency change as a function of the input voltage was 0.0133 cps/v. Based on the above data, the following equation for pulse rate is obtained:

$$\text{Rate} = 0.0143 \frac{V\text{-}V_o}{RC} \text{pulses/sec};$$

where, R = resistance in ohms; C = capacitance in farads; V = total input voltage; and V_o = bias voltage (approx. 140 for the NE96).

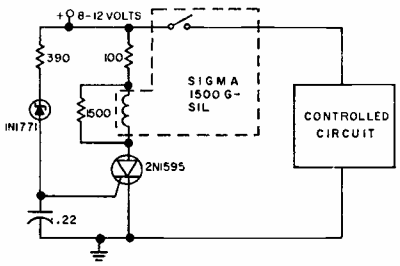
SCR-Zener Combination Senses Voltage Limits

HERE IS A CIRCUIT that can be used when an automatic switch is required to turn a circuit on or off as a result of changes in supply voltage above or below a predetermined value.

The circuit shown turns on at 12 v and turns off at 8 v. When the supply voltage reaches 12 v, the zener diode goes into its avalanche region, and the SCR receives gate power to turn on. The relay then is energized, providing on-off control for the circuit connected through the relay contacts.

When the supply voltage goes down to 8 v, the zener draws only leakage current, which is not sufficient to turn on the SCR. Also, the current through the SCR is below its holding current, and, consequently, the SCR is non-conducting. The relay is thus de-energized, turning the controlled circuit off. Rectifiers can be used for isolation between two controlled circuits.

This circuit is versatile and has many uses. The controlled circuit might be a battery charger which is automatically connected to the supply battery when the battery voltage drops to 8 v and is disconnected when the battery voltage reaches 12 v.



Voltage-limit sensing circuit.

The circuit can be adapted to suit any supply and controlled-circuit voltages within the limits of semiconductor devices, and can be made to sense supply voltage changes as low as 0.5 v. To change the operating point of the circuit it is only necessary to use a different zener diode.

Transistorized Phase Shifter

OFTEN IN SERVOS or other systems employing phase sensitive detectors or phase relationships to convey intelligence, a method of bucking out residual phase shift of the associated circuitry is required. In this circuit we have a simple, straight forward method of continual phase adjustment through nearly 180 deg. (in this case, greater than 170 deg). The transistor acts only as a phase splitter, offering complementary outputs. Phase shift at point *A* is 180 deg., at point *B*—0 deg. By adjusting R_1 through its range, proportional amounts of *A* and *B* are offered at the out-

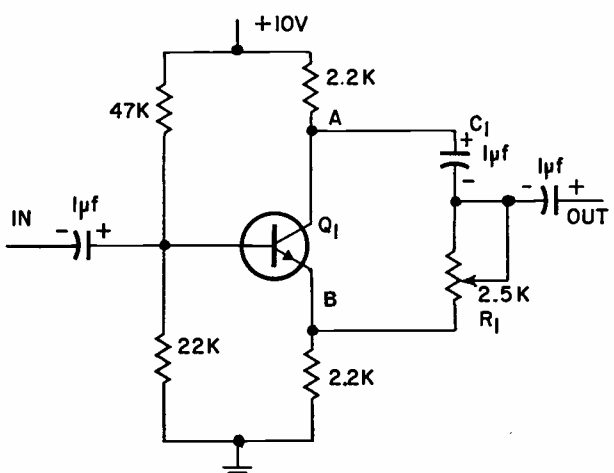


FIG. 1—Simple transistorized phase shifter, 0 - 180 deg. continuous.

put, determined by the specific setting of R_1, and the phase of the output relative to input is approximately in proportion to these relative amplitudes.

This particular circuit is optimized in the range of 1.0 kc and operates satisfactorily from 600 cps to 4.0 kc. An adjustment of C_1/R_1 ratio will shift this range. The transistor is a TI 2N1306.

SCR Voltage Sensitive Time Delay Switch

OFTEN, IN MISSILE circuit applications, a designer is required to mechanize a series of switched events initiated by a reference voltage level and separated by accurate time delays. A device for this purpose—simple, yet reliable, is presented here. The circuit in Fig. 1 can best be described as a voltage sensitive trigger which initiates sequenced thermal time delay relays. The relays used are Network Electronics' type M779, available normally open or normally closed, single-pole-single-throw, which operate on the fuse burnout principle. That is, when sufficient current passes through the relay fuse to burn it open, a spring loaded plunger is released which performs the required switching action. The time delay between rectifier firing and switch actuation is controlled by the resistance value (R_3, R_4, *or* R_5) in series with each separate relay fuse. The smaller the resistance, the shorter the delay time. Delays from 10 msec to 1.0 sec. ± 10 per cent are readily obtainable with high reliability.

Applied voltage, E_e, is exponential and can be obtained from a standard type capacitor charging circuit. When voltage at point *A* reaches 22 v, the Zener diode conducts and applies the triggering "signal" to the silicon controlled rectifier (*SCR*), CR_1, which "fires" and increases the currents through thermal elements of S_1, S_2 and S_3. Resistors R_3, R_4 *and* R_5, in this example, are chosen such that S_1 closes 100 msec after CR_1 fires, S_2 at 200 msec and S_3 at 300 msec. As the last fuse burns open, power is removed from the circuit thus eliminating unnecessary load on the missile power supply. The sequence of events is shown in Fig. 2.

Although, in the circuit shown, 22v at point *A* causes breakdown of the Zener diode, this voltage for breakdown can be varied along the exponential curve of Fig. 2 as long as there is sufficient power available at the *SCR* gate for firing. The resistance values in voltage divider $R_2/R_1 + R_2$ are selected to insure necessary gate voltage and gate current to fire the *SCR* at lowest and highest temperature extremes. Actually, in the example given, the anode-to-cathode saturation voltage of the *SCR* is practically independent of ambient temperature at the operating current level. Thus, the voltage across the three relays will be essentially constant. This constant voltage with temperature is reflected in extremely accurate time delays from −65 to +100 C.

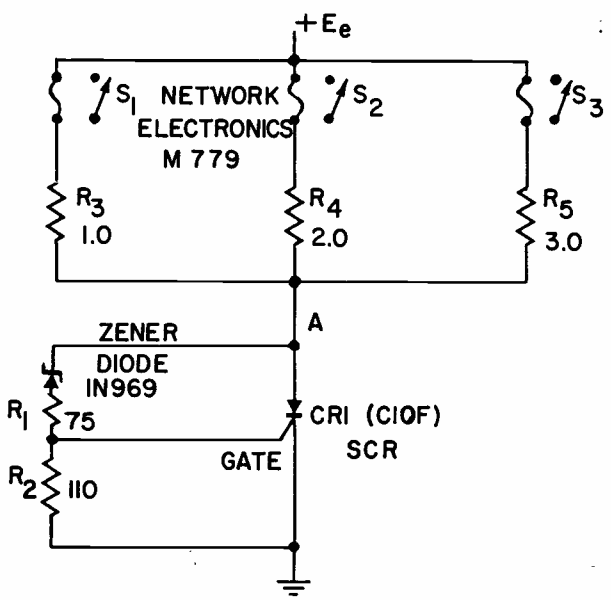


FIG. 1—Voltage sensitive trigger circuit initiates sequenced time delays.

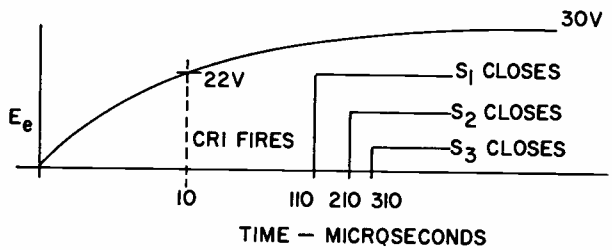


FIG. 2—Timing sequence as applied voltage, E_e, builds up. CR_1 fires after 10 msec. S_1, S_2 and S_3 close at 100 msec intervals thereafter.

Transistorized Motor Switching Circuit

THE CIRCUIT SHOWN in Fig. 1 was developed as a pulsed motor control circuit. This circuit offers the advantage of requiring only one voltage source, and eliminates non-simultaneous contact closing problems of dpdt relays.

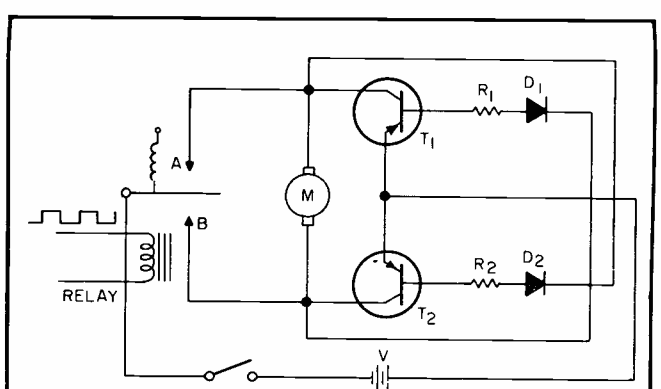


Fig. 1. Transistorized motor switching service.

Assume the relay is pulled in at position B when the circuit is in operation. This places $-v$ volts on one side of dc motor, M, and heavily forward-biases transistor T_1. As a result V-V_{sat} goes to the other side of the motor. The preceding causes the motor to rotate in one direction. When the relay drops out to position A, T_2 turns on, reversing the polarity at the motor and the direction of rotation.

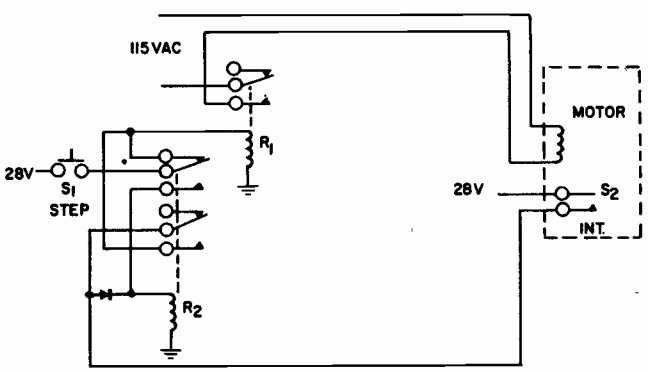
V_{sat} of the on transistor appears as forward-bias at the base of the off transistor. Diodes D_1 and D_2 act as nonlinear resistors effectively lowering the value of the off transistor base current. Resistors R_1 and R_2 together with diodes D_1 and D_2 determine the value of turn-on base current. Circuit betas, β_C, from 10 to 25 work well.

Step Control for Motor-Driven Selector Switch

IN DESIGN of a test unit, the use of a motor-driven rotary selector switch was incorporated. The requirement of the switch was that it be operated as a single step per pushbutton actuation. The switch is a rotary selector switch driven by a 72-rpm motor and contains a cam-operated sensitive switch interrupter.

The operator depresses and holds pushbutton S_1, energizing relay R_1 and applying 115-vac to the motor run winding. The motor starts running, driving the cam to a point to close the N.O. contacts of the interrupter switch. The interrupter switch energizes relay R_2, disconnecting switch S_1 from relay R_1, locking R_1, and locking R_2 through switch S_1. The motor of S_2 continues to drive until the interrupter switch is opened by the cam, de-energizing relay R_1, and stopping the motor.

Relay R_2 remains locked in until switch S_1 is released, releasing S_1 then permits the switch to be recycled. The instant starting and stopping characteristics of the motor eliminate any necessity for mechanical indexing of the selector switch.



Circuit for step control of motor-driven switch.

Beam Switching Tube Reset

THE RESET CIRCUIT shown below the dashed lines of Fig. 1 was developed to reset several beam switching tubes at one time.

Prior to this design, a thyratron was used to reset beam swiching tubes. In general, a single thyratron could only reset two or three beam switching tubes. The noise generation from the thyratron discharge was extremely objectionable. Where several thyratrons are used to reset several beam switching tubes in a chain, the noise frequently prevents stable reseting.

Figure 2 shows the resulting waveforms generated by the reset circuit. Waveform B is placed on all spades except the zero spade at time t_1. At the same time waveform C is placed on the zero spade. As all the spades go negative, the beam is cleared

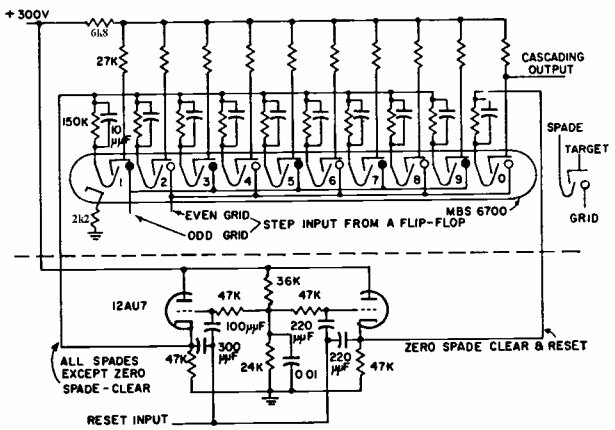


FIG. 1—Reset and MBS tube circuit.

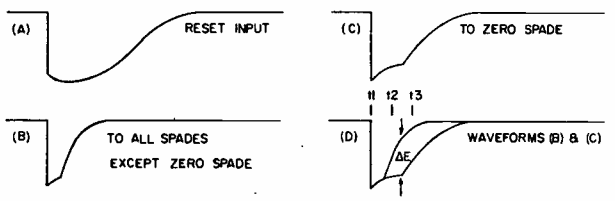


FIG. 2—Waveforms produced by reset circuit.

from the beam switching tube.

At the end of waveform B, at time t_2, all spades return to their normal voltage except the zero spade. This differential ΔE as shown at waveform D reforms the beam to the zero spade. When waveform C returns to the normal spade bias level, at time t_3, the beam switching tube is ready to be stepped. The pulse widtht difference, $t_3 - t_2$ is generated by the different RC time constants of the grid circuits. The cathode speed-up capacitors are used to discharge the beam switching tube spade capacity for fast reset.

When not resetting, the circuit supplies a regulated voltage to the spades for more reliable operation. A single tube will reset 10 cascaded beam switching tubes in twenty microseconds without failure.

Gain Control

A SIMPLE circuit for adjusting the gain of a transistor amplifier over a large frequency range without changing the dc bias is illustrated. The bias current, and hence the operating point, is maintained by the overall resistance, R_e, in the emitter circuit. The ac gain, however, is determined by that fraction of the emitter resistance bypassed to ground by the capacitor.

The relationship between the gain, G, and the unbypassed fraction of the emitter resistor, R_x, *is*

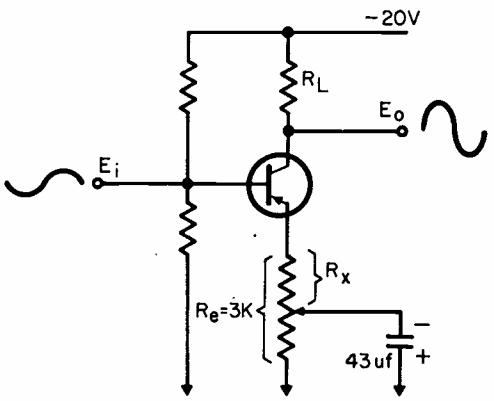
$$G = \frac{\beta R_L}{r_b - R_x\beta}$$

where

G = gain of stage E_o/E_i
r_b = effective base resistance
β = common emitter current gain of transistor for $\beta R_x >> r_b$

$$G = \frac{R_L}{R_x}$$

Hence, for a large range of potentiometer settings, the gain is inversely proportional to the variable R_x.



Transistor amplifier stage allows gain to be changed over a large frequency variation without effecting the dc bias.

Supervisory and Protective Relay Control

IT IS SOMETIMES necessary that any one of a number of operators of an equipment shall, once he has gained control of a remote equipment, be guaranteed uninterrupted control until he voluntarily and positively relinquishes his control. Such a requirement was encountered during the design of control circuits for an airborne wideband instrumentation magnetic tape recorder, calling for protection of the track recorded on the tape against interruption or erasure.

The circuit shown in Fig. 1 provides this type of control by means of a push-for-control pushbutton, a control relay and a transfer or dumping relay, with a floating ground line between stations. Any number of identical control stations can be connected.

Equipment control is obtained by actuating two relays, the control relay K_{111} and the transfer relay K_{112}, by means of a double-pole momentary-contact pushbutton switch S_8. The transfer relay is actuated only as long as the pushbutton switch is depressed and supplies 28 vdc to the control relay which has a hold-in circuit. When the push-for-control switch is released, the transfer relay opens removing the direct 28 vdc connection from the control relay which is, however, held in at reduced voltage, obtained by dropping the 28 vdc supply through two 75-ohm resistors in series. The station having control may now depress the record pushbutton causing the record relay to close, thereby gaining absolute control of the equipment. With the machine in the record mode no other position may gain control because the push-for-control ground return (floating ground line) is opened by contacts on the record relay. Consequently there can be no interruption to the record mode until the station having control pushes the stop switch, which stops the record mode by opening the 28 v supply to the record relays. This closes the contacts reinstating all push-for-control pushbutton switches. When this is done the transfer relay, at the station wishing control, shorts to ground the "hot" side of control

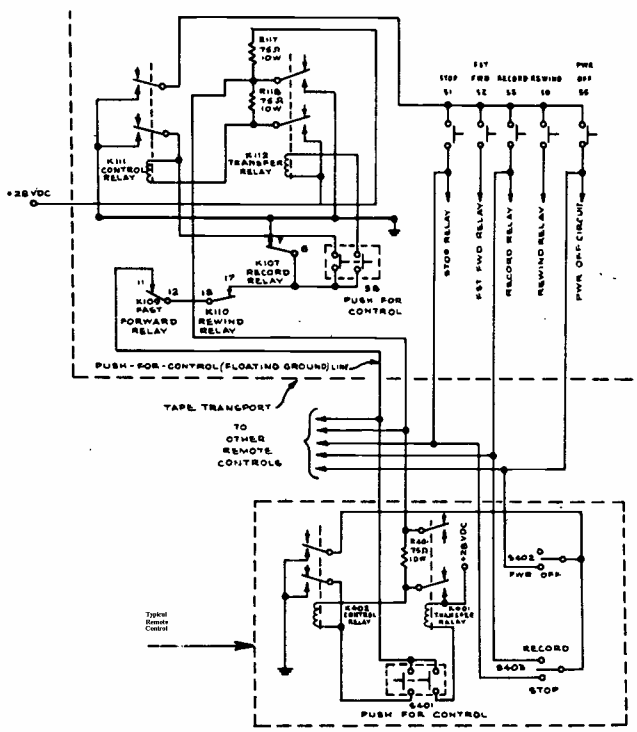


FIG. 1—Protective system prevents other remote stations from interrupting during recording process.

relay of the station relinquishing control, which, opens because there is now no voltage across the coil. The 28 volt source is protected by the series resistor R_{117}.

When the transport control unit has control its operator may initiate the rewind or fast forward modes as well as the record mode with absolute control. While the transport is in any of these modes no other position can get control and protection of recorded information is insured.

Variable Transistorized Phase Shifter

THIS UNIQUE application describes a simple 10-kc phase shifting network integrated with an active device with power and impedance matching features.

Most single-phase shifting networks are readily controlled by use of an a-c bridge circuit (such as the Wheatstone type).

Figure 1 shows one of the basic arrangements

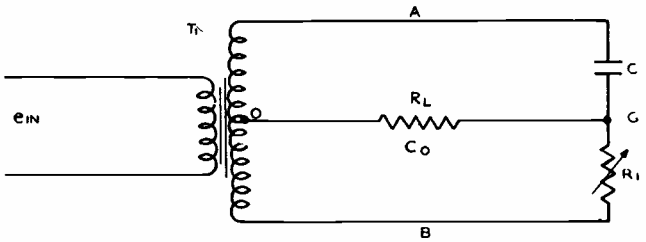


FIG. 1—Basic phase shifter circuit.

incorporating a center-tapped transformer secondary to form two bridge arms. *O-A* and *O-B*, both having equal induced voltages. The remaining two arms of the bridge are usually composed of two passive components, i.e. an inductor or capacitor in series with a variable resistor R_1. The phase shift voltage appears across the desired load at the points, *O-G*.

More often than not, it is assumed that no appreciable current will be drawn by the load selected. If so, then two distinct disadvantages will occur; excessive source power may be necessary; and reflected impedance variations will occur when adjusting phase control.

These problems can be resolved by the approach shown in Fig. 2. This features a similar bridge design, only the center tap is in the transformer's primary side with the common-collector configuration supplying the power. By reversing the bridge procedure and feeding the input signal being shifted into the center of the bridge arrangement, it is possible to balance the vectors across C_2 and L_1. Consequently a 90-degree phase shift signal appears across the transformer's primary winding, which is inductively coupled to the load via the secondary winding. This utilizes the common-collector's natural advantages; power gain, impedance matching properties, and little or no phase reversal.

The circuit provides a constant signal voltage (±5 percent) with a variable phase feature (90±15 degrees) while eliminating the standard phase-shifter disadvantages. Other advantages for this circuit include: low harmonic distortion, increased reliability through simplicity, and compact packaging.

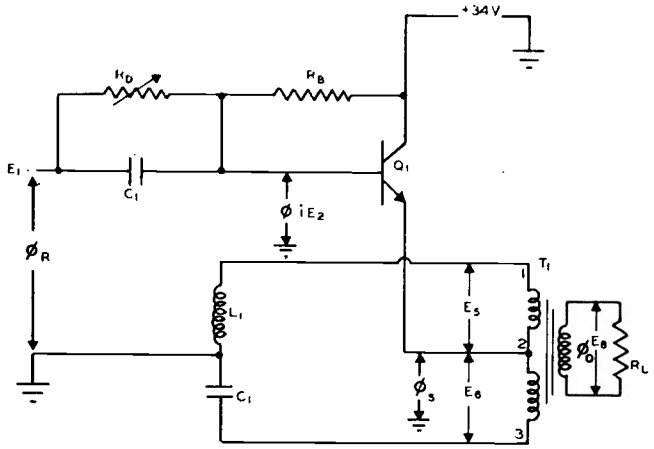


FIG. 2—Suggested values: R_D = 100K; R_B = 18K; C_1 = 1500 μμf; C_2 = .047 μf; Q_1 = TI2N1050; T_1 = 1:1.4, 10 kc; L_1 = 2-4 mh in series.

Because of component flexibility, almost any audio frequencies and/or input signal magnitudes can be handled. Initial design considerations for transistor selection would center around the critical parameters; maximum alpha cutoff frequency, and allowable emitter-base junction voltage (higher the better). Fixed bias is secured for the common-collector stage by R_B connected from the collector to base. This establishes the dc quiescent point for base current selected; with the series dc resistance of the inductor and half of the primary winding serving as the dc load line for transistor Q_1. Superimposed upon this dc load line of approximately 20 ohms is the 600-ohm ac load reflected from the secondary. Manipulation for a desired phase position

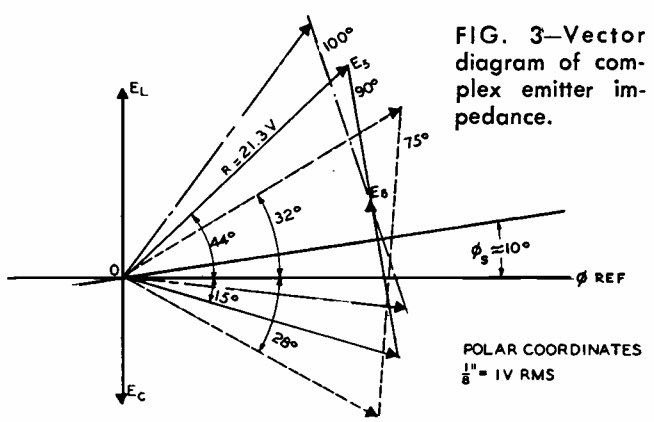


FIG. 3—Vector diagram of complex emitter impedance.

is possible by adjustment of R_D in shunt with C_1. At precisely a phase shift of 90 degrees, this value was 21 kilohms.

The transformer must be of a fairly good quality. The unit in conjunction with the emitter-follower stage developed a slight phase angle to the real audio transformer was available with nearly equal primary windings, turns ratio of 1:1.4, and was capable of handling the 200-ma dc unbalanced primary current through taps 1-2. This was required to maintain the correct dc bias for class A operation of the emitter-follower power stage. Analysis of the

phase rotation through 90 degrees reveals how the shifter functions (see Fig. 3).

Circuit applications for such a simple phase shifter include industrial areas for phase control of thyratron tube conduction, or possibly for correcting systems involving control synchro and resolver phase drift or shift, and demodulator reference signals.

Blower Delay Circuit

A SITUATION often arises in electronic equipment where it is desirable to have a blower or some other cooling device remain activated for perhaps n seconds after the removal of the primary power source. This delay is necessary in equipment where because of weight or space limitation the cooling equipment is designed to maintain the equipment just below some critical temperature while operating. However, when the equipment is turned off

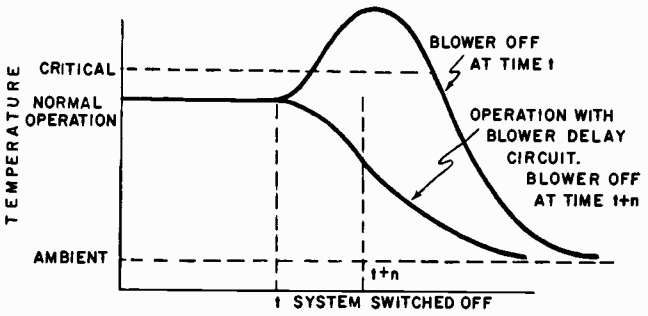


FIG. 1—Temperature versus time for a typical system at shutdown.

the temperature in the device as a function of time actually follows a curve similar to that shown in Fig. 1. In one particular system the increase in ambient exceeded the safe allowed seal temperature for a magnetron causing eventual failure and replacement of an expensive device.

There have been a number of circuits designed to keep cooling equipment activated for some additional incremental time but most of these devices require a small but constant primary power drain or utilize complex and expensive mechanical timers. The switching circuit shown in Fig. 2 performs the desired function with a high degree of reliability at a minimum cost while maintaining circuit simplicity. This circuit has been built and performs very satisfactorily.

The operation of the circuit is as follows:

A dpdt Switch, S_1, is shown in the normally off position and since relay A is deactivated, contact A_2 is open, and no power is applied to the n second timer B or the system. The circuit is activated by throwing S_1 into the on position thus applying power to the system, relay A and the blower.

By activating relay A, contact A_1 and the normally closed contact of the n second timer form a holding contact on relay A. Thus when contact X on S_1 is broken, relay A and the blower remain on while

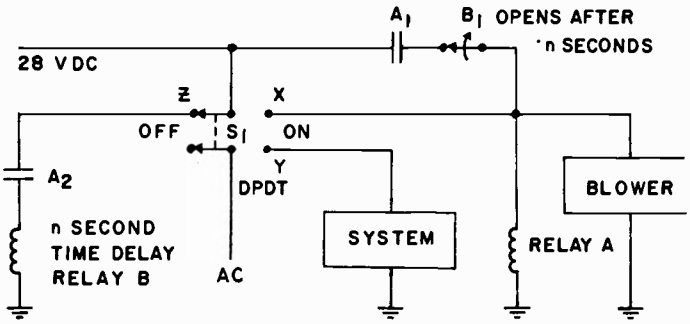


FIG. 2—Blower delay switching circuit.

primary power to the system through contact Y on S_1 is removed.

When S_1 snaps into its off position, contact Z then supplies 28 volt power through closed contact A_2 to the time delay relay or timer B. After n seconds elapse the normally closed contact of B opens momentarily causing relay A to loose its holding contact which in turn opens contact A_2; thus, the timer is once again de-energized and the cycle is completed.

Advantages of this circuit are that the timer contact need carry only the line current of the blower and relay A rather than the load current of the entire system. Further, since the time n is not critical in most practical cases the timer is a relatively inexpensive device. No primary power is drawn by the system after n seconds and the contacts on relay A handle only the blower current and the timer current which is very much less than the system load current; therefore, a rather inexpensive relay may be used.

Low Cost Servo Motor Control

THIS SYSTEM was developed to meet a need for a low cost, photoelectric cell controlled servo motor.

The 10-watt servo motor is a two-phase type with one 110v ac winding and a center-tapped high impedance winding for use with vacuum tubes. The amplifier consists of two symmetrical channels to supply control voltage to the high impedance winding of the motor. The input to the amplifier is a d-c signal proportional to the illumination of the photocell. The first stage of the amplifier proper is cross connected to reduce the effects of drift in the dc sec-

tion of the system and effects of tube variations.

The requirements of a two-phase motor are that the control windings must be supplied a voltage 90 degrees out of phase with the line winding. The output of the photocell is a dc voltage which always exists in the same polarity with only ampl tude variations. In order to eliminate a chopper a simple method of simulating chopper action was required.

Phase shift can be obtained by use of a resistance and capacitance in series, however, to obtain considerable shift, high resistance and capacitance values (with respect to the frequency of operation) must be employed. Also the voltage appearing across the capacitance is comparatively low. It is possible to obtain a phase-shifted current by use of a resistance and inductance in series. This method was utilized in the system designed. The 24-ohm resistor in series with the output winding of a small audio output transformer causes a phase-shifted voltage to appear across the secondary (original input of the transformer). This voltage is further corrected by use of the capacitor in parallel with the winding, also correcting some loss in waveform occurring in the transformer. The total output was in excess of the value required for application to the first amplifier, therefore the output was taken from the center tap of the transformer winding and loaded to ground by the 100-ohm resistor.

This phase-shifted voltage is applied to the grids of the first stage of the amplifier in ac parallel through the coupling capacitors. It is additionally amplified and applied to the control winding of the servo motor. Being of equal values at the motor and supplied in opposition, no resultant motor rotation occurs. Some additional phase correction is obtained through the addition of the capacitors in parallel with the grids of the second stage of the amplifier and in parallel with the motor control windings.

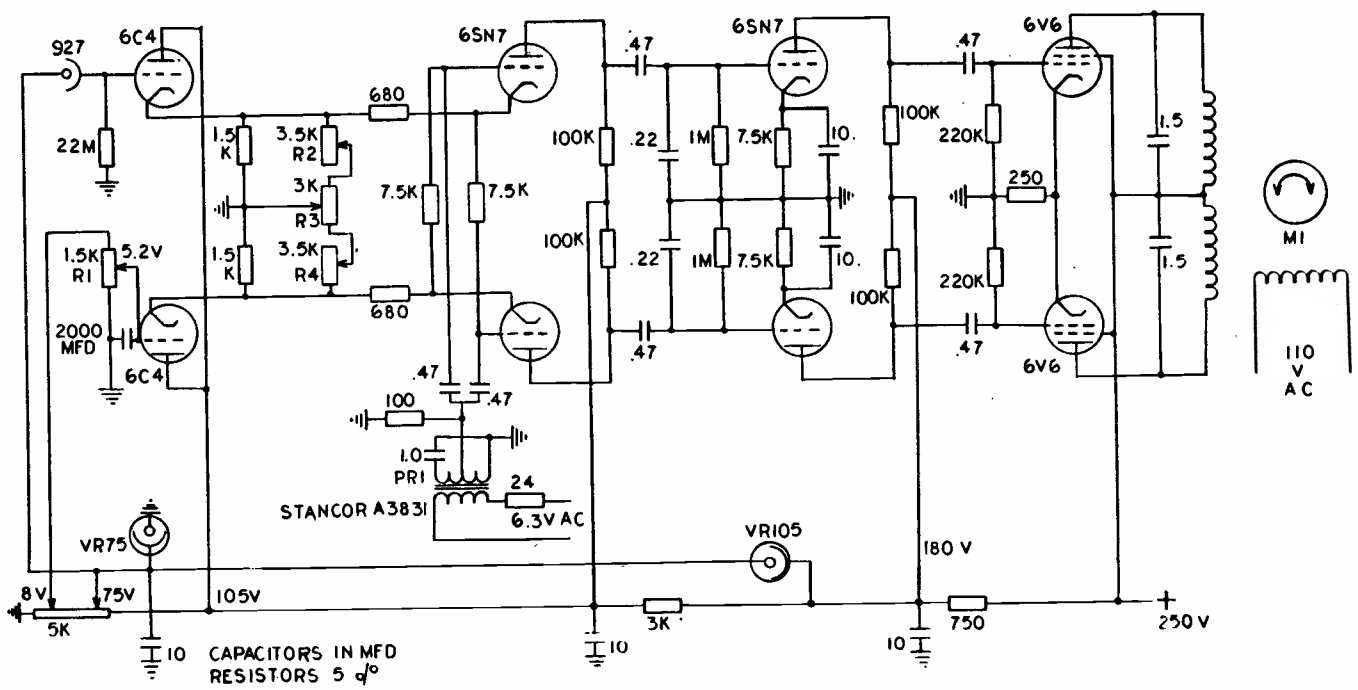
Because of the connection of the first stage of the amplifier, in which the grid resistor of one tube returns to the cathode resistor of the opposite tube, a change in operating point of a given tube results in a correction being automatically applied to the other tube. The cathode-follower photocell amplifier, the dc level control tube and the first amplifier stage are connected through a common cathode circuit.

Resistors R_2 and R_4 are mechanically connected with proper ratio gearing to the servo motor and serve as position feedback control. Resistor R_3 is utilized as a zero-center control.

The servo motor may be connected to a shutter in such a manner as to produce a given output from the photocell at the control point center of the operation being controlled. This might be a bin or hopper containing opaque material and being fed automatically by the servo system. As the contents increased above a given level, the illumination of the photocell would produce a signal such as to cause the servo motor to reduce the opening of a filler valve. With a reduction of the contents, the control valve would be opened.

In adjustment of the system, the shutter would be positioned at the proper level and with the correct filling of the container. The drive motor would then be disconnected and resistor R_1 adjusted to produce equal voltages at the cathodes of the first amplifier stage. With the drive motor reconnected, resistor R_3 is adjusted to balance the system about the control point.

This system was designed some years ago, as evidenced by the components called out. Replacement of tube types with more modern units would probably improve the reliability. The power supply



Low cost servo system is controlled by photoelectric tube.

divider system and the 8 volts supplied to the dc level control tube could also be modernized.

This system may be utilized in connection with any type of sensing device whose output is an amplitude modulated dc signal. The feedback control system shown may also be included more directly into the sensor output or the dc level control tube.

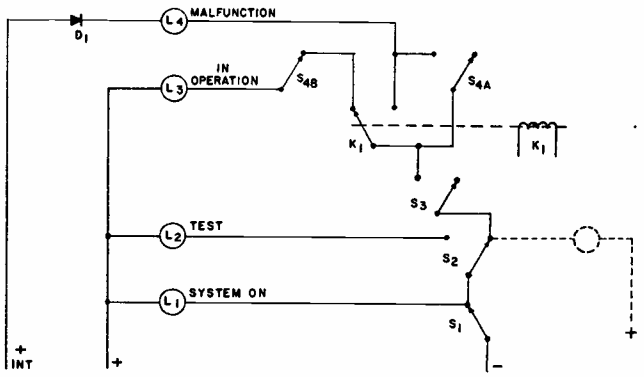
Control Switching Circuit

THE CIRCUIT shown prevents an operator from progressing to a new switch position without returning the previous switch or switches to a specified position.

Such a circuit may be used with lamps as shown for supervisory control or the lamps may be replaced with relays for actual control of operations. This circuit also contains a warning indication or cutoff, not under the control of the operator.

In the circuit, switch S_1 and lamp L_1 are the ON or SYSTEM ASSIGNED unit: L_2 is for TEST or ADJUST indication; L_3 is for the IN OPERATION indication and L_4 is for WARNING, MALFUNCTION or CUTOFF. Any number of L_2 components may be connected in the series. If it is desired that L_4 be supplied with an intermittent voltage to provide a flashing signal, it is necessary to insert a diode as shown to prevent a phantom circuit when a number of these systems are operated from the same power source.

In actual use, closing switch one (possibly remotely located and controlled by the supervisor), will start the operation or advise the operator that the controlled device is assigned for use. During the period necessary to setup, calibrate, or adjust



Supervisory control switching system

the device, the operator will close switch two, giving this indication and preventing the third unit from operating. After the necessary operation in position two, the operator turns off the unit two switch and then may turn on the unit three switch, placing the device being controlled in the desired condition (or giving indication of such).

If during the progress of the operation in a normal manner, the operator detects some undesirable occurrence he may close the switch of unit four, which in the supervisory system shown will not stop the operation but will give the supervisor indication that a malfunction has occurred.

The relay contacts shown are part of a relay which may be connected to the device in an appropriate manner to give the same indication automatically. The contacts of the relay may be connected into the circuit shown as either normally closed or normally open, depending upon the nature of the voltage available to the relay coil under non-failure conditions of the controlled device. It should be also noted that when unit two is operated, a failure signal from unit four cannot be generated, since during setup operations it may be normal to have a condition which might be abnormal in the operating condition.

An additional indication which might be of value can be obtained by connecting a lamp or relay as shown dotted at unit two. This lamp of course, indicates the alternate position of the switch to which it may be connected.

Remote Controlled Rotary Switch

REMOTE control of a distant rotary switch or stepping relay, is important in many applications. It is always possible to pulse a connecting wire, thus presenting a known number of pulses to this distant rotary switch and stepping it a known number of steps, but this is not a particularly accurate method. It is also possible to have the distant switch search for a particular marked contact, but in this case it is necessary to have a multiplicity of wires between the rotary switch and the control console. It would be advantageous to have a distant rotary switch find a particular marked contact, and have all marking for up to ten contacts accomplished over one wire. The device described here provides a means for so controlling a distant rotary switch.

The detector portion of this device consists basically of a balanced bridge circuit as in Fig. 1. Two legs of this bridge are composed of the resistors associated with the controlling wafer switch, R_1, and a 7500 ohm resistor, R_2. The other two legs of the bridge are composed of the resistors associated with the controlled rotary switch, R_3, and another 7500 ohm resistor, R_4.

If the resistors set in the rotary switch are the same as the resistors set in the wafer switch then the bridge is balanced and there is no voltage between points A and B. If the wafer switch is now moved the resistance of R_1 is changed, and there is a voltage difference between points A and B. This voltage causes a current to flow in the rectifying diode bridge, producing a current in the transistor base leads. Note that whether the potential of A

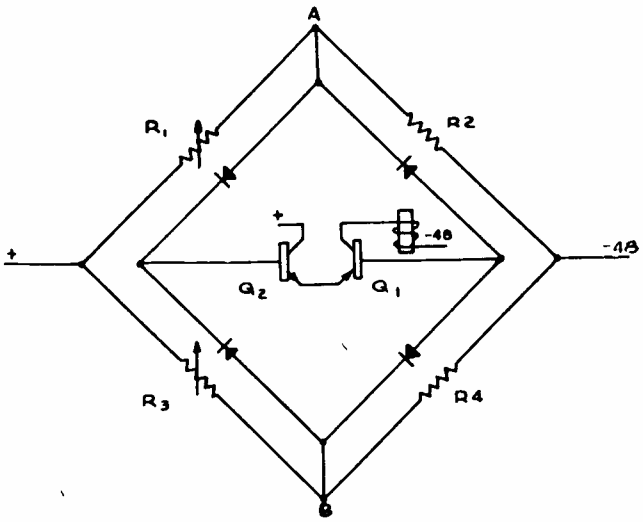


FIG. 1—Bridge circuit used to detect signal for activation of rotary switch.

bridge either increases or decreases, until eventually the correct contact is reached. When this occurs the bridge is balanced, and all relay current is stopped.

It is possible, as shown in Fig. 2, to make adjustments for line resistance between the remote wafer switch and the rotary switch apparatus. The 300-ohm resistor shown as being variable may be adjusted such that the resistance of this resistor plus the combined resistance of the control wire and the ground wire equals 300 ohms.

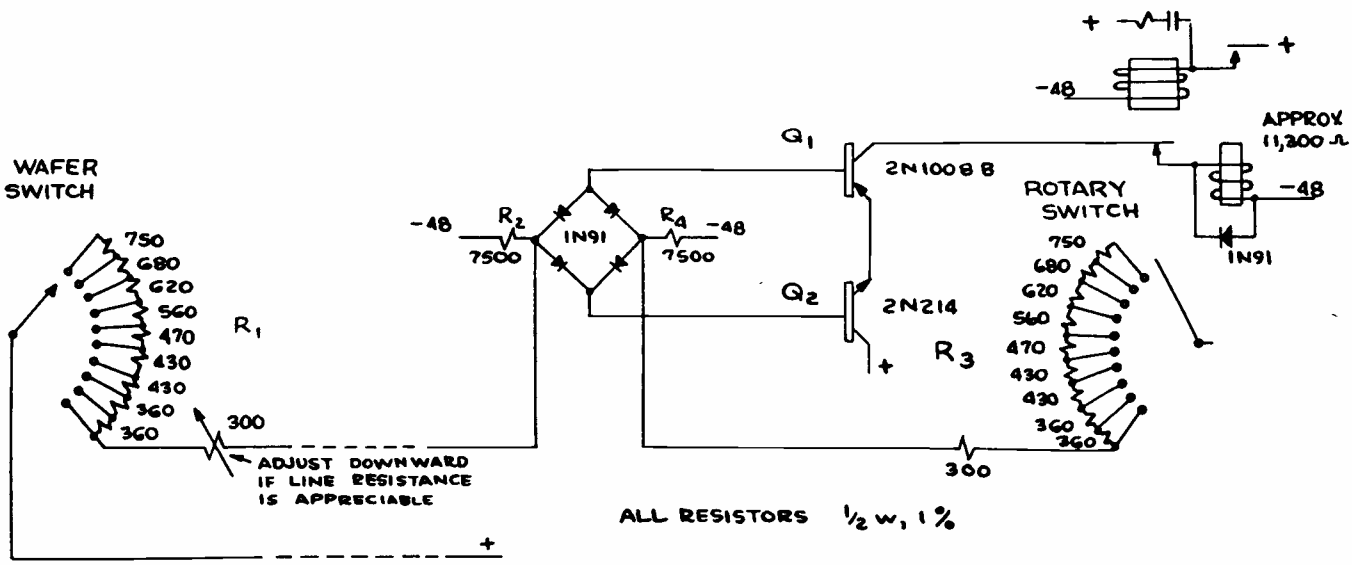


FIG. 2—Remote rotary switch steps to match resistor values at control position.

is higher or lower than that of B (caused by a larger or smaller R_1), the direction of current is the same.

This current is amplified in transistor Q_2, which is an npn transistor, and Q_1, which is a pnp transistor. The amplified current from these transistors operates the relay.

Figure 2 shows the connections of the relay, wafer switch, rotary switch, and transistors. The wafer switch can be located some distance from the remainder of the equipment, and perform all necessary control over one wire plus ground.

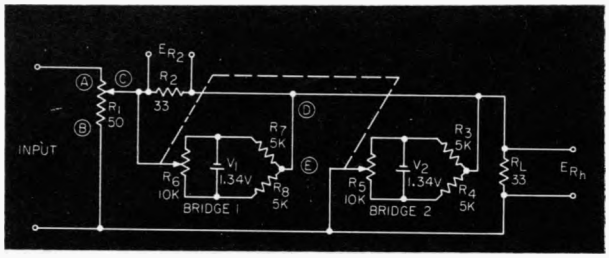
As shown here the relay, in operating, energizes the rotary switch. As the rotary switch cocks it breaks the circuit to the relay, causing the relay to release. This in turn breaks the circuit to the rotary switch, which falls back and steps, thus changing the resistance of R_3. As the rotary switch steps the current resulting from the unbalanced

Non-Interacting Positioning and Attenuating Controls

THIS CIRCUIT adds a dc positioning voltage to an input signal that is to be applied to a recording galvanometer. The major feature of the circuit is that the magnitude of both the input and the positioning voltages can be controlled independently, without interaction between the two controls. The total output voltage is equal to the sum of the positioning voltage and the attenuated signal voltage.

In the circuit, bridge 2 adds the dc offset to the output voltage, while bridge 1 sets up an equal voltage of opposite polarity across R_2. The ganging of R_6 and R_5 maintains the off-balancing of the bridges equal. There is no flow of current back through R_1 from the positioning bridge circuits because the two voltages cancel at points B and C of R_1. Therefore, there is no voltage feedback to the input and adjustment of R_1 will have no effect on the positioning circuits.

At the output, the maximum signal is reduced by the



Non-interacting position and attenuating controls.

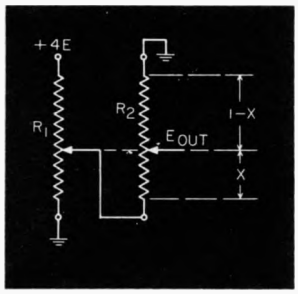
voltage-divider factor $R_L/(R_L \div R_2)$, which in the basic circuit is 50 percent. This shortcoming can be overcome by decreasing R_2. However, to maintain the effects of the two bridges equal, V_1 must be increased by the same factor by which R_2 was decreased and a resistor must be added between points D and E whose value is the difference between the new R_2 and the old R_2. For example, if R_2 were decreased to 11 ohms to make the maximum output voltage 75 percent of the input, then V_1 should be increased to 4.02 v and a resistor of 22 ohms added between D and E.

Dual Linear Pot Approximates Sine Pot

IN MANY CONTROL AND COMPUTER SYSTEMS, an analog output is required that is equal to the input multiplied by the sine or cosine of the angle on a controlled shaft. Although sine-cosine pots have been manufactured to perform this function, their cost often is too high to allow use in systems where a high degree of accuracy is not needed. A more economical method is shown.

A dual pot is connected as in Fig. 1. If R_2 is much

Fig. 1. Two linear pots connected to approximate a half-sine wave.



greater than R_1 (i.e. R_2 does not load R_1), it can be shown that $E_{out} = 4X(1 - X)E$, where X is the fraction rotated by the wipers. This parabolic function approximates one-half of a sine wave with a maximum error of $0.056E$ at 21 deg and 159 deg, as may be seen in Fig. 2.

A practical circuit which generates the positive and negative halves of a sine wave is shown in Fig. 3. This circuit approximates a sine function with a maximum error less than 10 percent. The error can be reduced by placing a buffer stage between the two pots and/or by using pots of better linearity.

Fig. 2. Comparison between pot approximation and sine function.

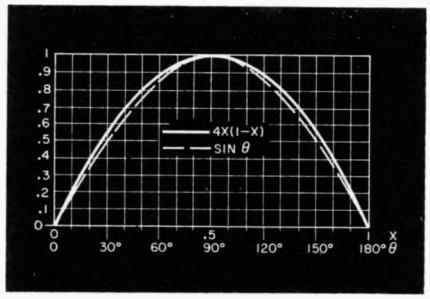
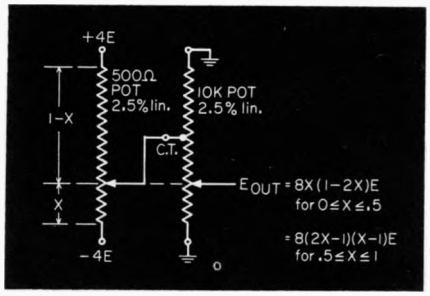


Fig. 3. Practical circuit for approximating complete sine function.



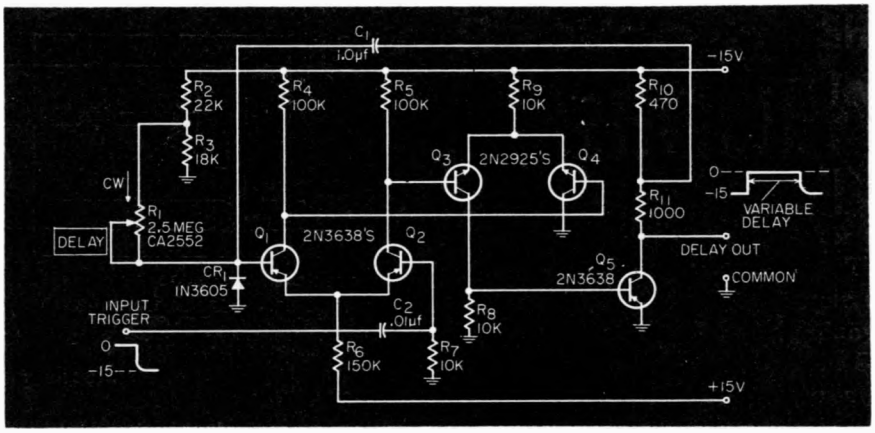
Wide-Range Variable Delay Circuit

THIS CIRCUIT was designed to provide a continuously variable delay from less than 10 msec to greater than 1 sec. The delay can be varied with good setability over the entire range due to the use of a single log tapered pot, R_1. The circuit was originally designed to delay a negative-going waveform in a negative true-logic system. The circuit is quite economical since it utilizes inexpensive commercial grade epoxy encapsulated silicon transistors.

The output stage Q_5 is a saturated pnp switch, driven by a two-stage non-saturating differential amplifier (Q_1, Q_2, Q_3, Q_4). A slight imbalance in the input stage Q_1 and Q_2 will drive Q_5 entirely on or off. The R-C time constant is provided by C_1 and R_1. Voltage divider R_2 and R_3 is used to allow the use of a 2.5-meg pot (a 5-meg pot is not commonly available in a log taper). Q_1 is the "normally on" side of the input amplifier; its on current is provided by R_1. This on current varies from approximately 3 to 700 μA.

When a negative triggering pulse is applied to the base of Q_2, Q_1 is driven off regeneratively by Q_5, which is driven on, pulling the junction of R_{10} and R_{11} from -15 V to -10 V. The voltage divider R_{10} and R_{11} is added to restrict this voltage excursion to 5 V to protect Q_1 from excessive reverse V_{BE}.

At the end of the delay, Q_5 turns off and C_1 is recharged to -15 V through R_{10} and CR_1. CR_1 clamps the base of Q_1 to -0.6 V during this recovery time. CR_1 also clamps the base voltage of Q_1 during the quiescient interval when the hold-on current provided by R_1 could pull the Q_1 base



Wide-range, continuously variable delay is set by log-taper pot R_1.

voltage negative by several volts depending on the setting of R_1.

The range of delay realized is typically from 6 msec to 1.5 sec, insuring that with a ±20 percent pot tolerance and ±10 percent capacitor tolerance the desired 100:1 range is still achieved.

Peak-Hold Circuit

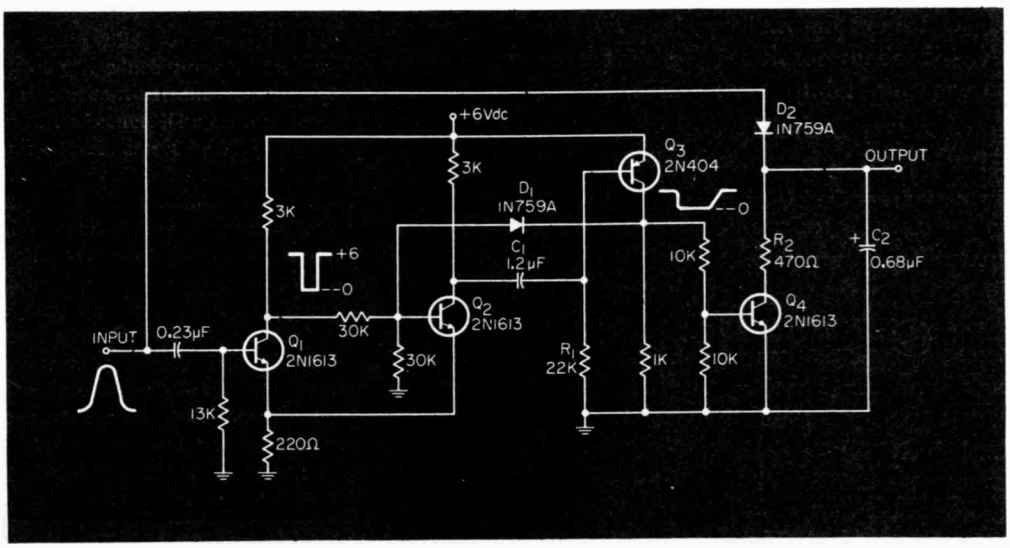


Fig. 1. Simple circuit holds the peak voltage of a short-duration input signal. Storage period is determined by the value of C_1.

IN CONTROL systems and instrumentation, it's often necessary to hold the peak voltage of a short-duration analog signal for a longer period of time. For example, mechanical indicators such as pen recorders have slow response but will measure the peak value of short-duration signals if used with a suitable peak-hold circuit.

The circuit shown in Fig. 1 receives a short-duration analog voltage as input and holds the peak magnitude of the input for any required period up to several-hundred milliseconds. Fig. 2 shows the input and output waveforms.

Transistors Q_1, Q_2 and Q_3 (any normal switching transistors) form a combined Schmitt-trigger and one-shot circuit. Normally, transistor Q_1 is cut off while Q_2 and Q_3 are turned on. Diode D_1 is then in the reverse-biased condition. When the short-duration analog signal appears at the input, the Schmitt-trigger action of transistors Q_1 and Q_2 shapes the signal and turns off Q_3. During the "off" time of Q_3 (controlled by the R_1C_1 time constant), diode D_2 is forward biased thus forcing Q_4 to be cut off regardless of the state of transistor Q_1. Because Q_4 is cut off, capacitor C_2 charges to the peak value of the analog input less the voltage drop of diode D_2. The capacitor holds the peak voltage until Q_3 is again turned on.

To avoid shunting capacitor C_2, an emitter follower can be added as an input buffer. The value of C_2 determines the discharge time for the next input peak. The value of C_1 determines the "hold" time of the circuit.

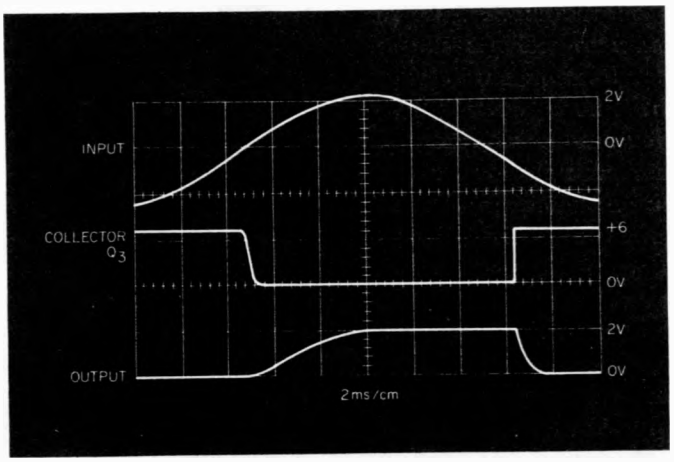


Fig. 2. Typical waveforms for the peak-hold circuit using component values shown in Fig. 1.

Modified Limiter With Improved Accuracy

THE CONVENTIONAL limiter circuit of Fig. 1 has two basic disadvantages: The rounded "knee" of the diode D_1 causes changes in limiting level for different input voltages. Current in the potentiometer causes further changes in limiting level. Because part of the diode current goes through each section of the potentiometer, the voltage drop changes with the position of the potentiometer slider.

The modified circuit of Fig. 2 overcomes these disadvantages. Voltage gain between E_{out} and point B is about 100. Transistor Q_1 operates as a common-base amplifier. Thus only a small change of E_{out} is required to turn the diode full on and to overcome any voltage change due to diode current. The knee voltage of D_2 and the V_{BE} of transistor Q_1 do not subtract from this action, since both are "on" before limiting occurs.

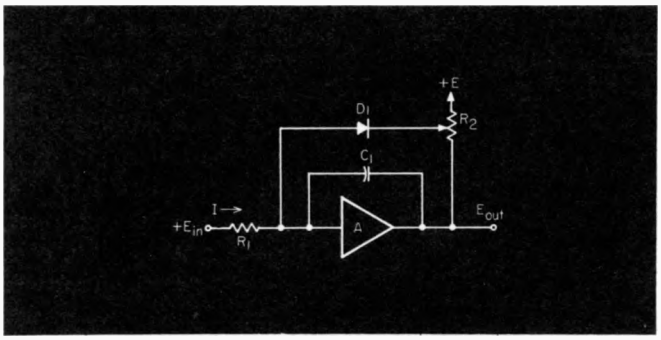


Fig. 1. This commonly-used limiter circuit for integrators has the disadvantage that calibration varies with input level.

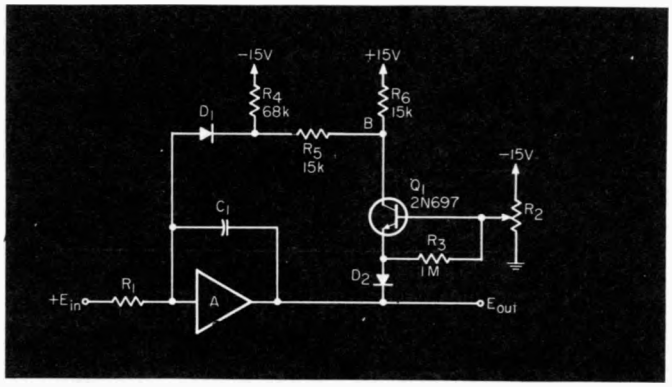


Fig. 2. Modified circuit gives improved accuracy because of the gain of grounded-base amplifier Q_1.

As the base current of Q_1 is very small, this current causes no detectable change of potentiometer voltage at any setting.

Resistor R_3 and diode D_2 protect Q_1 from reverse voltage at the base emitter junction. Resistors R_4 and R_5 provide bias for D_1.

Transistor Q_1 should have high gain, while diodes D_1 and D_2 should be silicon types with high back resistance.

This circuit was used with an integrator to limit at levels up to 10 V, with inputs from 0 to 10 V. Calibration was maintained within 0.1 percent.

Signal-powered dc voltage sensor controls ac loads

A FOUR-LAYER breakover diode simplifies the design of a voltage sensor that needs no external power other than the sensed voltage.

The circuit shown in Fig. 1 can be used to control various types of loads such as an ac relay, a lamp or an alarm horn. Fig. 2 shows how the sensor circuit is simply connected like a switch in series with the load, across a 115-volt ac line.

The load current should be sufficient to provide holding current for the SCR (typically 4 mA). The maximum current is restricted by the rating of the SCR. With the components specified, and with suitable heat sinking of the SCR, the allowable load current is around 1.5 amps.

With the component values shown in Fig. 1, the input trigger level is approximately 9.3 volts. So the circuit will respond to any input voltage above about 10 V. An internal limiting circuit prevents damage due to excessive input voltage. Hysteresis of the circuit is around 100 millivolts.

The circuit works as follows. Breakover diode D_2, capacitor C_1, resistor R_2 and pulse transformer T_1 together form a simple relaxation oscillator. Whenever the input voltage exceeds the breakover voltage of D_2, a train of pulses appears at the secondary of T_1. These pulses then gate the SCR output switch.

The pulse train is rapid enough to ensure almost full firing of the SCR during each cycle of the 60-hertz ac applied to the load through the switch. The SCR is operated

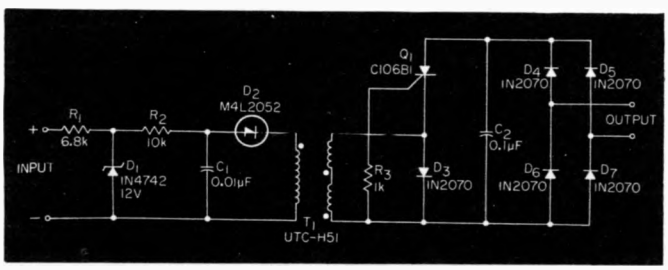


Fig. 1. Simple voltage sensor with threshold voltage determined by four layer diode D_2. The pulse transformer isolates the sensing circuit from the load circuit.

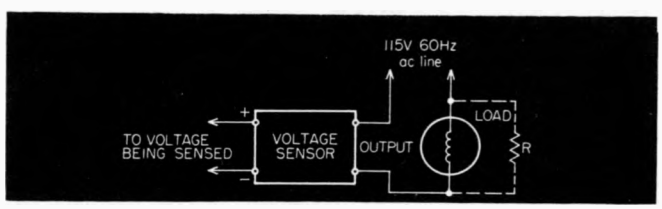


Fig. 2. The voltage sensor is used like a simple switch connected in series with the load. If load current is insufficient to hold the SCR in conduction, the load must be shunted by a resistor R.

in a bridge circuit configuration. Components R_3, C_2 and D_3 suppress transients and rate effect (false triggering that occurs when the ac line is turned on near the peak of a cycle).

Because the input circuit derives its power from the voltage being sensed, input impedance is necessarily rather low. But it has been found to be adequate in most applications.

For inputs below the breakover voltage of D_2, the input impedance is essentially the parallel leakage of C_1, D_1 and D_2. This is typically several megohms.

When the input voltage exceeds the breakover voltage of D_2, the impedance fluctuates because of the charging and discharging of C_1. In this mode, the minimum input impedance is 17 kilohms.

Zener diode D_1 prevents the breakover diode D_2 from reaching its holding current when the input voltage exceeds the trigger voltage. As the input voltage increases beyond that required for triggering, the pulse rate increases until a point is reached where the zener diode prevents further increase. The repetition rate, for input voltages above this level, depends on C_1, R_2 and the zener voltage. This rate must be sufficiently high to ensure a large conduction angle for the SCR. If the repetition rate is too low, it could cause a relay load to chatter.

Motorola's M4L series of four-layer diodes covers the range 8 to 12 volts. Other manufacturers offer diodes suitable for different voltages.

Simple modification prevents single-cycling with SCR motor drive.

A COMMON disadvantage of SCR phase-control circuits for ac motors is that the motor may run in a single-phase mode when continuous power is applied. This is because the inductance of the motor winding causes the motor current to lag motor voltage. However, a few extra components, added to the basic circuit, can eliminate the problem.

Let's look first at the conventional circuit. Fig. 1 shows a popular method of motor-speed control using SCR switches. In this full-wave circuit, SCR_1 applies power during the negative half cycle and SCR_2 applies power during the positive half cycle. Motor speed is proportional to conduction angle, which is the same for each half cycle.

Figure 2 shows the waveforms for motor-current I_M and motor-voltage V_M. The motor-current I_M lags V_M by an angle α, which is a function of the applied power and the Q of the overall load circuit.

In case (a), the motor fixing angle ϕ_a (which defines conduction angle β) is greater than α_a. Thus the fixing angle controls the applied voltage for each half cycle, resulting in smooth control of motor speed.

But in case (b), the fixing angle has been decreased to ϕb in an attempt to increase the motor speed. This increases α to α_b, which is greater than ϕb. Under these conditions, the motor current doesn't return to zero before SCR_1 (which controls the negative conduction cycle) receives its turn-on pulse V_{G1}. Thus V_{G1} occurs before SCR_2 has turned off. This puts a reverse bias

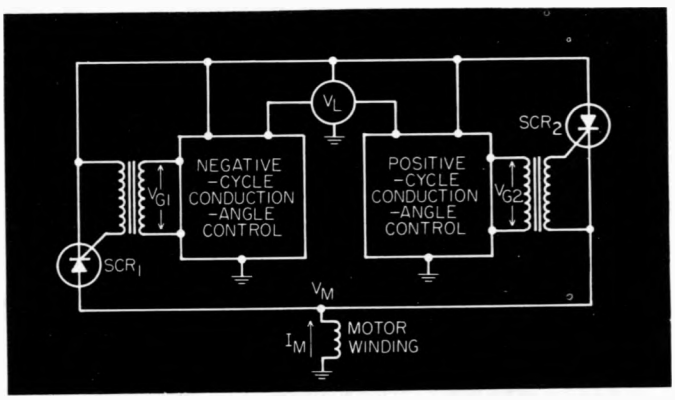
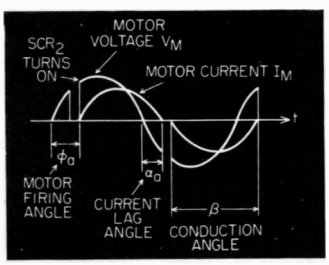


Fig. 1. Conventional full-wave phase-control circuit has the disadvantage that the motor may "single cycle" with low firing angles.



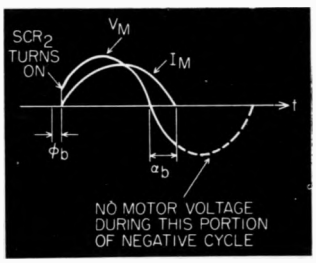


Fig. 2 a (left) In this example, the firing angle ϕ is greater than the current-lag angle α so single-cycling is not a problem.

Fig 2 b (right) In this example, however, ϕ_b is less than α_b so there is no motor voltage during the latter part of the negative half cycle.

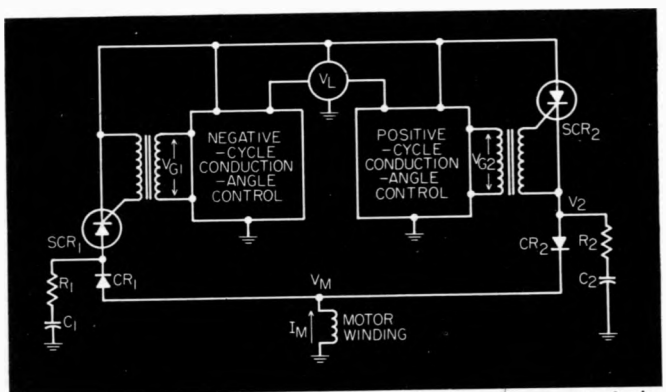


Fig. 3 An improved version of the full-wave phase-control circuit, in which the added diodes and RC networks eliminate the single-cycling problem.

across SCR_1 when its turn-on pulse occurs. Consequently, the SCR doesn't turn on and the motor voltage isn't reapplied during the negative half cycle. This condition is known as single cycling.

The only known method for preventing single cycling is changing the SCR triggering mode from transient to steady state. In applications where this is impossible or uneconomical, the fixing angle ϕ must be maintained greater than α, using some sort of limiting circuit.

Figure 3 shows a simple circuit modification that prevents single cycling. Assume that SCR_1 and CR_1 are conducting. Then CR_2 and R_2 allow C_2 to charge to the negative peak of V_M. When V_M starts its upward slope, CR_2 becomes reverse-biased and C_2 retains the negative peak. Now, when SCR_2 receives its trigger pulse V_{G2}, it can turn on because its cathode is at a low negative voltage.

When I_M finally goes to zero, at some point into the positive half cycle, SCR_1 will turn off, CR_2 will become forward-biased, and SCR_2 will apply V_L to V_M which will continue uninterrupted.

Resistor R_2 must be small enough to provide the minimum turn-on holding current required by SCR_2. The network R_1, C_1, and CR_1 performs the same function as described for its counterpart—but at the end of the positive half cycle.

Reference

1. F.W. Gutziwiller, "G.E. SCR Manual, 4th Edition," General Electric Company, 1967, p. 173.

High-voltage triacs reverse capacitor motor

Two TRIACS and two capacitors are the essential components for a simple bridge circuit that can control rotation-direction of a fractional-horsepower, capacitor-start, motor. With a suitable trigger circuit, also described here, motor direction can be controlled by IC logic voltages.

Figure 1 shows the bridge circuit, and Fig. 2 shows a suitable trigger circuit together with its power supply. The bridge and trigger circuit are coupled together by transformers T_1 and T_2. No external power supply is needed, other than the 115-Vac supply for the motor.

Low-level logic, from an IC flip-flop, forward-biases either Q_1 or Q_2 at points L or R respectively; resulting in either "left" or "right" motor drive.

Unijunction oscillator Q_6 provides pulsed emitter current which is conducted by either Q_1 or Q_2 depending on the input logic. One of the two pulse transformers then couples the pulsating signal to the corresponding triac Q_3 or Q_4. Triac conduction determines the phase of the capacitor winding relative to the main winding. This, in turn, determines the direction of rotation.

Pulsed output from Q_6 is synchronous with the ac line, because the supply voltage for the unijunction is full-wave clipped ac derived from the combination of transformers, rectifiers and zener. Of course, the pulse train ceases each time the line voltage crosses the zero axis. There is a short delay before the unijunction oscillator can restart with a new line-voltage cycle. This is because the timing capacitor must recharge to the firing voltage of Q_5. Delay is sufficient to allow the voltage to build up across the triac, thus ensuring reliable triggering.

The 75-ohm resistor, shown in series with the main winding, allows motor direction to be reversed while the motor is running. This resistor is not required if the motor need only be reversed from standstill rather than while running. Also, the resistor is not needed if the motor is always heavily loaded. Use of a series resistor causes a sight reduction of starting torque.

A disadvantage of the simple two-triac controller is that it doesn't allow phase control of the motor — to vary the starting torque. This is because the nonconducting triac sees an extremely high voltage across the near-resonant motor-and-capacitor circuit. Though the 400-volt triacs used here are adequately rated for full-phase running, they would not be able to withstand the dV/dt conditions encountered with delayed triggering. If phase control is needed, a third triac in the main winding could be phase-controlled from a separate trigger source.

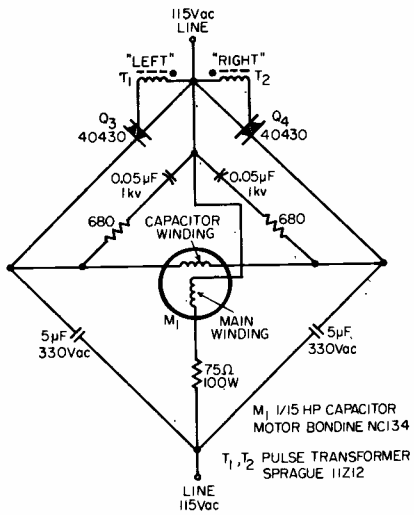


Fig. 1. Simple triac bridge controls direction of rotation of capacitor-type motor.

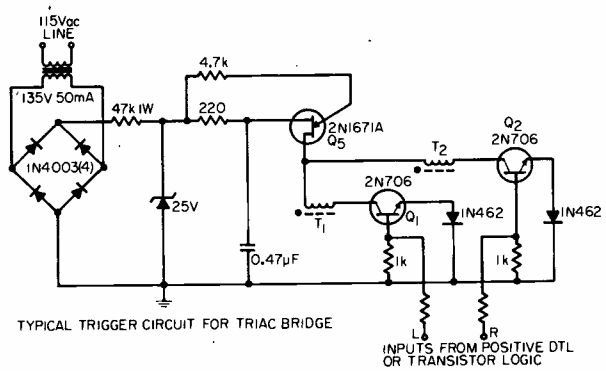


Fig. 2. Control circuit for the motor controller. Depending on the input logic, pulses from the unijunction oscillator are transformer - coupled to one of the two triacs in Fig. 1.

The two-triac controller is foolproof. Simultaneous triac triggering, or a shorted triac, will stall the motor — which then draws about two-thirds of its normal running current. With the specified motor, current in the capacitor winding ranges from 500 mA rms at idling speed, down to 300 mA with both triacs shorted. Current in the main winding is 1.6-A idling and 500-mA stalled.

RC networks across each triac minimize the possibility of unwanted dV/dt triggering. The values depend on the inductance and back emf of the particular motor used.[1] With

the motor specified here, the no-load back emf is about 800 V, resulting in dV/dt of 2 V/μs.

The same basic circuit can be used to control motors other than the one specified. Larger motors would probably increase the dissipation of the conducting triac, necessitating a heat sink. Very small motors could be controlled by a simpler circuit with a triac connected from one winding or the other, directly to the line.

Reference

1. "G.E. SCR Manual, 4th Edition," General Electric Co., 1967, p. 136.

Variable control for automobile windshield wiper

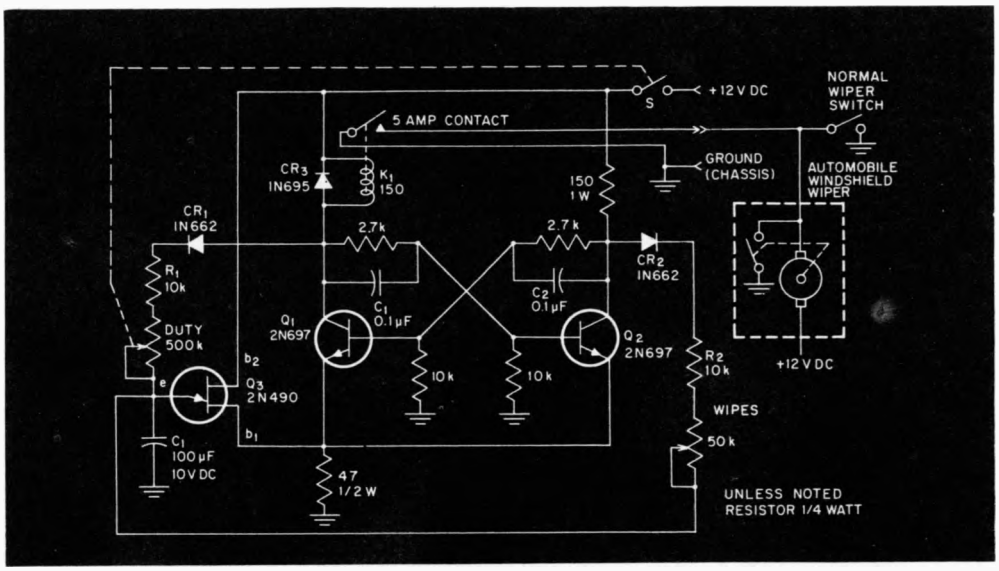


Fig. 1. Flip-flop circuit acts as a driver for windshield wipers and provides variable control.

WHEN DRIVING a motor vehicle in very light rain, it is often desirable to operate the windshield wipers at infrequent intervals — say, for example, every 30 seconds. Depending on the condition of the rubber blades, it may be necessary to allow one or more wiping actions across the windshield for proper cleaning. The circuit described allows independent control of both frequency and interval, while still allowing the blade to run at its normal speed while wiping.

The circuit shown in Fig. 1 consists of a flip-flop, a unijunction timer driven by the flip-flop, and a relay which drives the wiper motor. When the windshield control switch S_1 is turned on, +12 Vdc is applied to the driver and either Q_1 or Q_2 turns on. Assuming that Q_2 is on, then capacitor C_1 is then charged through the coil K_1, and via CR_1 R_1 and the *DUTY* adjust resistor. Depending on the setting of the *DUTY* pot., unijunction transistor Q_3 will be activated in about one to 80 seconds, and the flip-flop, consisting of transistors Q_1, Q_2 and associated circuitry, will be switched. This allows Q_1 to turn on and Q_2 to turn off, thereby causing K_1 to close and supply power to the windshield wiper motor through the relay ground. Depending on the setting of the *WIPES* pot, control capacitor C_1 will be charged through CR_1 and R_2 in about one to eight seconds, and the flip-flop will be switched back to its former position. The *WIPES* control will usually be set for about one second for a single wiping action, however, this depends to some extent on the speed of the individual wiper motor. Thereafter, the cycle repeats at the time interval determined by the *DUTY* control.

Diode CR_3 suppresses transients that are produced when the relay coil is interrupted. Speedup capacitors C_1 and C_2 ensure proper flip-flop switching action. A separate ground wire should be used for the relay, since the motor current through this lead could produce a significant voltage drop and upset the flip-flop operation.

Section 2
REGULATOR CIRCUITS

A Time-Variant Attenuator

OCCASIONALLY it is necessary to measure a signal which has a greater dynamic range than the instrument available for recording the measurement. If the signal changes in a predictable fashion with respect to time, an automatic gain changing network can be used such that the signal to the recorder always lies within its dynamic range.

The circuit to be described accepts an input signal which changes over a range of 60 db and provides an output to the recorder within 20-db limits. The gain is changed by attenuating the signal in three discrete steps, which eliminates any ambiguity in knowing the over all transfer function at any given time during the test. Thus, calibration is not affected and known scale factors may be applied during data reduction.

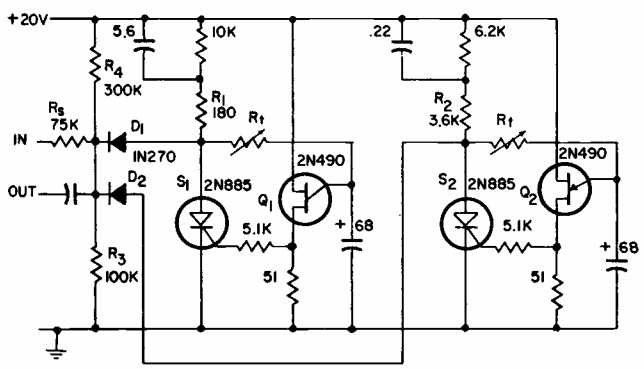


FIG. 1—In the time variant attenuator, Bourns type 3250L-1-502 pots are used to vary the timing of the unijunction circuits. The silicon controlled switches are miniature units made by Solid State Products.

The circuit shown in Fig. 1 is based upon the voltage divider equation, $e_{out} = e_{in} R_p/(R_s + R_p)$, where R_p is caused to change through the action of two time delay switches. When the circuit is first actuated, both diodes are conducting and their dynamic impedance is quite low. In this case, R_p is equal to the parallel resistance of R_1 plus the dynamic impedance of D_1, R_2 with its diode, R_3, and R_4. As the series resistance of R_1 and D_1 is about 300 ohms, it is this value which sets the initial attenuation and causes the input signal to be divided by 200.

Applying power to the circuit has started the timing sequence by energizing the standard RC unijunction transistor time delay circuits, and when Q_1, the first unijunction to fire, triggers its associated silicon controlled switch S_1, D_1 becomes back-biased, essentially removing R_1 from the input circuitry. Now it is the parallel combination of R_2 and its diode impedance, R_3, and R_4 which makes up R_p and R_2 is chosen such that now the circuit divides by 20. When the second scs is triggered by Q_2, D_2 becomes back-biased and now only R_3 and R_4 make up R_p. The attenuator divides by 2 in this case and consists of only the three input resistors.

In setting up the circuit, the input impedance of the amplifier or recording device must be accounted for in selecting R_3 and R_4 as the attenuator cannot be loaded without changing the transfer function.

Because only passive devices are used to determine the attenuation factors, good stability is achieved and there is less than 3 per cent variation at any time over the temperature range of —50 C to 75 C. The noise characteristics are also quite good in that no noise could be measured with the instruments available.

As the attenuation is changed, there is a switching transient, during which data is lost, of about 30 milliseconds. The timing of the changes can be varied independently from less than a second to as much as a minute by selecting R_t, and the time stability is about 5 per cent over the above temperature range.

Servo-motor Winding Stabilizes Power Amplifier Operating Point

THE MAJORITY of transistorized servo-amplifiers employ class AB power stages in the common emitter configuration to realize the maximum power gain. (See Fig. 1). The quiescent current of these stages must be stabilized at a suitable small-signal gain level. A common emitter resistor used for this purpose will set the total emitter current but it will not correct unequal current sharing due to different base-emitter voltages. Furthermore, the resistor seriously reduces available output power for large input signals.

An improvement can be realized with the common collector configuration shown in Fig. 2. When driving a low-impedance load, such as a servo motor, the power gain is only slightly less than other configurations, and the output voltage is limited only by the saturation resistance of the output transistors.

The grounded collector circuit has certain advantages. First, a fact which does not appear to have been used previously, the motor control winding placed in the emitter circuit provides through its positive temperature coefficient a compensation for the negative temperature coefficient of the base-emitter voltage. Second, the winding will conveniently provide the proper separate emitter resistances necessary to equalize quiescent current sharing.

Either pnp or npn transistors can be used with this circuit. With npn transistors and a negative supply or pnp transistors and a positive supply, the collectors may be directly grounded for better heat dissipation.

The control winding impedance can be selected for maximum power output for a given supply voltage and transistor saturation resistance with the aid of the following relationship:

$$Z_m = \frac{2V_{cc}\left(V_{cc} \pm \sqrt{V_{cc}^2 - 8W_m R_s}\right) - 4W_m R_s}{W_m}$$

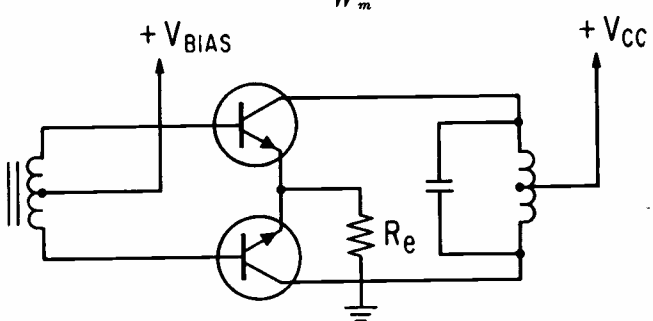


FIG. 1—Conventional circuit for driving servo motors.

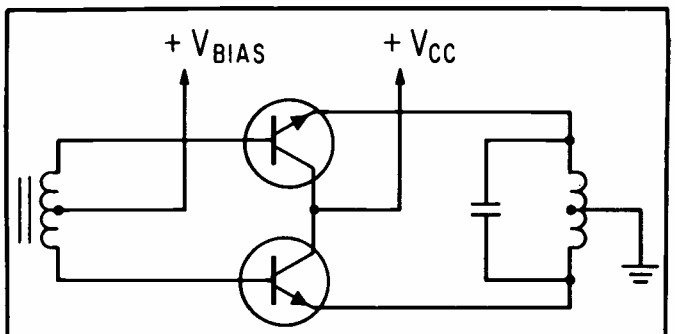


FIG. 2—Better current balance and temperature stability result with grounded collector circuit.

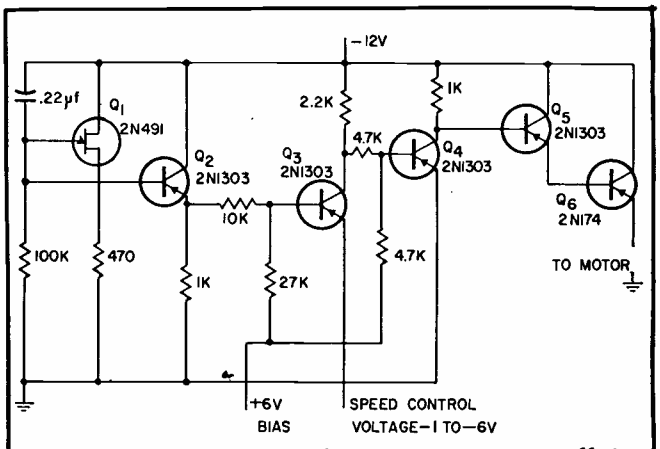
where W_m = motor watts, V_{cc} = collector supply voltage, R_s = saturation resistance of output transistor, and Z_m = control winding impedance.

Motor Speed Control

REGULATION of speed of a small dc motor is difficult, especially over a wide range, and when the driven load is subject to change. Also, the starting friction requires more voltage to overcome than that required to maintain rotation. The following circuit is capable of driving a small pm motor at speeds of less than one rpm up to full speed in direct proportion to the control voltage. For all practical purposes it eliminates the problems caused by starting friction.

The principle employed is to always apply full voltage, 12 volts in this case, to the motor. The speed is regulated by interrupting the voltage at a fixed frequency and controlling the on-time to off-time ratio.

Transistor Q_1 is used in a conventional saw-tooth generator circuit. The output is —4 volts to —10 volts at a frequency of approximately 50 cycles.



Speed regulator circuit for dc motor varies on to off time of pulses.

This frequency was chosen because it gives optimum motor performance. Q_2 couples the generator to the detector Q_3 through a biasing network. Q_3 will conduct only when that portion of the sawtooth wave which is more negative than the emitter, is applied to the base. Therefore, by varying the emitter voltage, the ratio of on to off time can be controlled. The ratio is in direct proportion to the control voltage, which is —1 to —6 volts. Q_4 amplifies and squares the output of Q_3 by going from cutoff to a saturated condition. A Schmitt trigger circuit is not used due to its hysteresis properties. Q_5 and Q_6 are emitter followers to provide the power to drive the motor. An output rating of one ampere is quite conservative for the unit.

Zener Diode Regulator

A SIMPLE REGULATOR, continuously variable between 0 and 30 volts, is useful for bias and transistor testing applications. The design of such a regulator poses several knotty problems, however. As an example, the two-transistor feedback regulator (Fig. 1) suffers from poor regulation near full output. For this condition the ratio of R_1/R_2 must be large to cut off the control transistor. The error signal is also divided by the ratio R_1/R_2. Further, the usual transistor regulator circuit does not go to zero for the control transistor requires forward bias (obtained from the output) to cut off the current passing transistor.

A circuit for circumventing this problem is shown in Fig. 2. The zener diode, in addition to performing a function as reference element, will provide a reduction in dc without attenuating the control or error signal. In the regulator circuit shown, 40 volts dc is applied to the load through the regulator transistor Q_1 and a 10-volt zener diode Z_2. Connected in this manner the emitter of Q_1 will always be 10 volts more negative than the output terminal, providing the bias voltage and error signal for transistor Q_2.

For zero output voltage the potentiometer arm is moved toward the Z_2 end, causing diode Z_1 to avalanche. The voltage appearing across resistor R_2 biases the control transistor, greatly reducing the junction resistance. Resistor R_1 and transistor Q_2 form a voltage divider to reduce the bias on the current passing transistor, Q_1. Under these conditions the emitter to positive terminal potential will be approximately 8.4 volts. Since this is less than the breakdown voltage of Z_2, no potential appears across the output terminals.

To obtain output voltage the potentiometer is rotated toward the R_3 end. This reduces the bias on Q_2, decreasing the junction resistance of the regulator transistor Q_1.

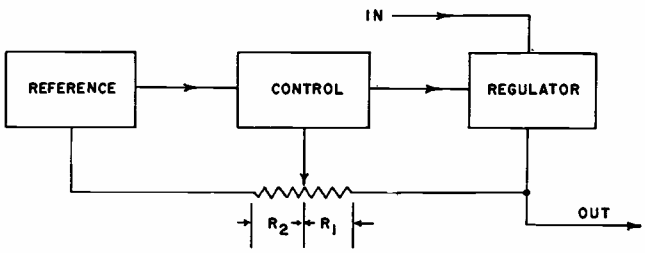


FIG. 1—Conventional two-transistor regulator.

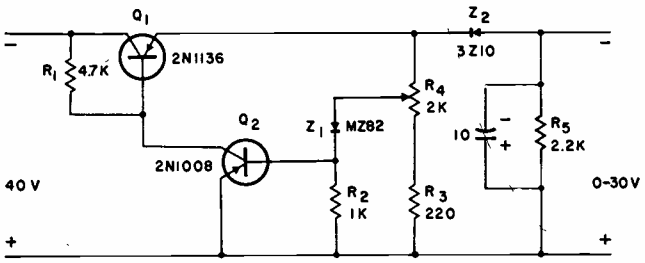


FIG. 2—Simple regulator provides zero to 30 volts output.

The use of a diode in series with the error signal reduces R_1/R_2 ratio and improves the regulation at all voltage settings. Series-connected diode Z_2 permits the output voltage to be reduced to zero. Both diodes are International Rectifier types.

For best regulation both diodes are selected in the avalanche region, well past the zener knee. If more output voltage is required, and a small minimum voltage can be tolerated, diode Z_1 may be replaced with an MZ-3.9 and Z_2 can be eliminated. With these changes it will not be possible to reduce the output below 4 volts.

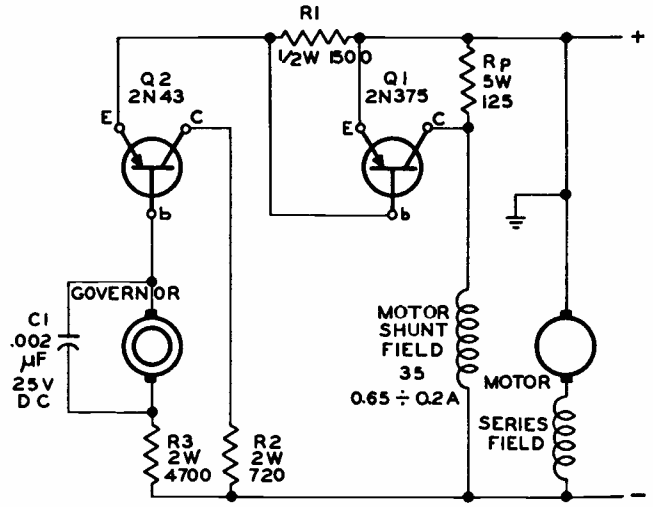
Transistorized Speed Regulator

CONVENTIONAL centrifugal governors for speed control of dc motors are widely applied. The limitations of this type of control include the handling capabilities of the contact fingers, the violent changes of instantaneous speed rates caused by the governor contacts switching on and off a major part of the field power, the regulation drift due to contacts arcing and pitting, and the regulation accuracy.

A transistorized speed regulator, where the centrifugal governor is used only as an error detector loaded very lightly (microwatts), where the problem of arcing and pitting does not exist. where the drift is minimum and where the regulation is better than $\pm 1/4$ percent will be described.

The speed regulator is designed for a 1/2 H.P. dc motor operated from 24 vdc supply. The anticipated input voltage range is between 20 v to 30 vdc, and rated motor speed is 6000 rpm.

A two-transistor amplifier is connected across the



Governor contacts handle only a few microwatts of power.

Table I. Test Data

Input Voltage VDC	Load Percent	Speed RPM
20	0	5995
20	100	5986
24	0	6000
24	100	5995
30	0	6010
30	100	6010

minimum field resistor. No separate source of power is necessary for the amplifier. The only input is the 24-vdc bus.

The amplifier consists of a preamplifier transistor (Q_2) and a power transistor (Q_1). The centrifugal governor controls the signal current flow between emitter and base of the preamplifier. The signal current is a few microamperes. The signal power that the governor is required to handle is in the range of microwatts. The amplifier sensitivity is adjustable. The governor may be as small as desired, consistent with mechanical requirements.

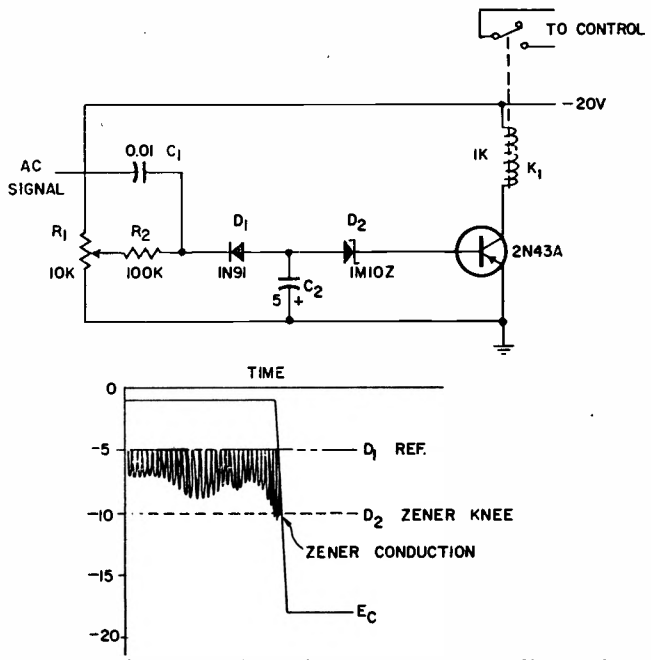
Table I shows readings taken with varying conditions of input voltage and load.

Snap Action Level Switch

PRESET AUDIO POWER level indicators find many applications in the field of electronics. Circuits of this type are usually unreliable because in the ac to dc conversion the velocity component is lost. Therefore, if the integrated dc voltage is used to control a transistor-relay combination, the I_{co} and temperature effects on the transistor render the unit unrepeatable.

In the circuit shown here, a zener diode, with a zener knee of 10 v, was employed to allow the integrated voltage to reach a relatively high point. The instant the zener breaks from nonconduction to conduction, the control transistor is forward biased. The transistor goes from cutoff to saturation in a snap-like action, thus actuating the relay. Level of operation is controlled by the adjustment of potentiometer R_1.

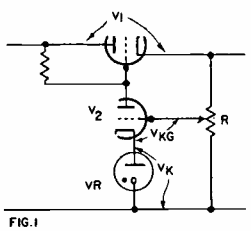
This circuit could also be used as a gating circuit if K_1, was replaced by a suitable transistor and load resistor combination.



Level switch circuit (top) has snap action effect when ac signal goes over zener conduction point (bottom).

Low-Voltage Transistor Series Regulator

UNLIKE a vacuum tube circuit, a low voltage transistor regulator does not require a reference voltage because of the difference in biasing between tubes and transistors. In Fig. 1, tube V_2 must be biased for Class A operation (no grid current) to regulate properly. Therefore the grid of V_2 must be negative with respect to its cathode. This can be accomplished by the VR tube which contributes to regulation by holding V_K constant.



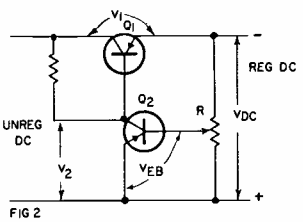


FIG. 1—Tube regulator using VR tube as reference.

FIG. 2—Transistor series regulator for low voltage.

Transistors, however, must draw base current for class A operation. Using the circuit of Fig. 2, it is unnecessary to insert a reference diode at the

emitter of Q_2. In fact, when the emitter of Q_2 is grounded, emitter ground becomes the reference of Q_2. As V_{DC} increases, so does V_{EB}, I_B, while V_2 decreases and V_1 increases, thereby decreasing or regulating V_{DC}.

Naturally, better regulation is obtained if V_{EB}/V_{DC} is larger. This should be the reason for inserting a reference in the emitter leg of Q_2 because the base of Q_2 can be applied to a higher point on R, thereby applying a greater portion of the output voltage change to the base of Q_2. This improvement is limited to the reduction of voltage across V_1 (V_{EC}) due to the reference.

However, as mentioned previously, for low voltage regulators, V_{EB}/V_{DC} will be sufficiently large for most applications.

Whether or not a reference diode is used, V_{EB} can still vary with temperature. It is possible to use a silicon transistor for Q_2 to minimize this effect. In addition V_{EB} can be larger for silicon than for germanium, resulting in a larger V_{EB}/V_{DC} ratio.

Blanking Circuit Clamps to DC Level

THIS BLANKING CIRCUIT clamps a linear amplifier's output to its dc operating level during the time the blanking signal is present. The necessary blanking signal is a negative rectangular pulse.

During blanking, Q_1 and Q_2 are saturated. Resistors R_5 and R_6 then form a voltage divider between E (−20 v) and ground. If V is the operating level of the amplifier, the values of R_5 and R_6 should be chosen such that

$$\frac{R_6}{R_5 + R_6} \cdot E + 0.3 = V$$

The emitter resistor R_7 of emitter follower Q_3 is returned to ground through Q_2. Since Q_1 is saturated, the source impedance of Q_3 is low and Q_3 therefore has a low output impedance. The current flowing through Q_3 should be sufficient so that Q_3 can act both as a source and as a sink for the amplifier Q_4; hence the amplifier output is clamped to the voltage V.

To ensure clamping of all signal magnitudes,

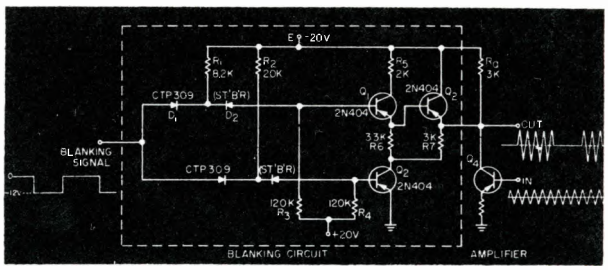
$$R_7 < R_a \frac{V}{E - V}$$

In the circuit shown, this means that $R_7 < 4.5$ K.

In the absence of the blanking signal, Q_1 and Q_2 are off. Emitter follower Q_3 has an extremely high source impedance, namely the parallel combination of the reverse biased base-emitter diode of Q_1 and the output impedance of $Q_2(r_e/\beta)$. This source impedance divided by the beta of Q_3 is the load for the amplifier during the positive-going excursion of the signal.

When the signal is negative-going, the amplifier is loaded by the parallel combination of the reverse biased base-emitter diode of Q_3 and the output impedance of Q_2. In both cases this load is sufficiently small so that it can be ignored. ◆ ◆

Poor original image. R1 may be 82k
in value, the D.P. if valid was badly printed
Point E badly printed, had to assume -20V



Blanking circuit (Q_1, Q_2 and Q_3) controls output of linear amplifier Q_4.

Non-Attenuating Voltage-Control Circuits

THESE CIRCUITS shift the dc level of a signal without attenuating the ac signal voltage. The basic dc-level-setting component in each circuit is a zener diode.

In Fig. 1, the zener diode sets an exact voltage across resistor R, which does not change as the input voltage changes. However, the voltage above ground at the potentiometer slider varies directly with the input signal. Fig. 1 shows a circuit that transposes a zero dc voltage from a high impedance source to a low-impedance source in which the output can be set to exactly zero volts.

Figures 2a and 2b show other possible arrangements. These circuits transpose to a more negative dc voltage. If the zener diodes and supply voltages are reversed and pnp transistors used, the circuits can be used to transpose to a more positive dc voltage.

The actual component values depend on the voltages to be transposed, but care should always be taken to draw enough bias current through the zener diode. ◆ ◆

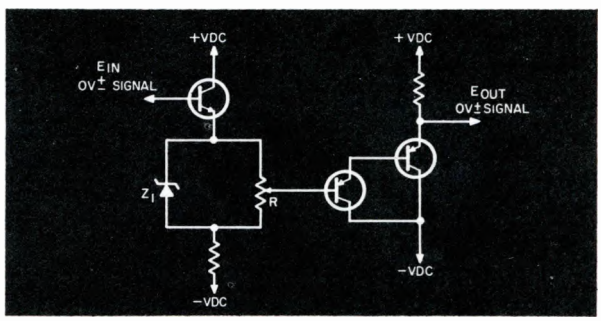


Fig. 1. Basic voltage-control circuit.

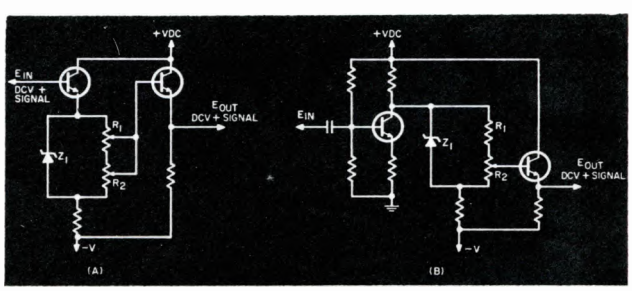


Fig. 2. Voltage-control circuits for shifting to a more negative dc voltage.

Temperature-Stabilized Darlington

USE OF DARLINGTON or beta-squaring circuits leads to severe offset-voltage changes as a function of temperature. If the ΔV_{be} figure is about 2 mv per deg C, a 25 C temperature change can give an output change of 50 mv per stage which can represent a 50 percent (or more) change in quiescent output.

Here are two circuit variations for minimizing or eliminating this temperature effect. Fig. 1a shows a typical Darlington while Fig. 1b shows a modification that includes a pair of diodes and an additional resistor. In these circuits quiescent levels are assumed for silicon transistors at temperatures of 0 C and 50 C, and it is assumed that I_{c2} is about 10 ma and I_{c1} about 0.1 ma. Values of V_{be} as a function of I_c and temperature are manufacturer's specs for the 2N930 but they are typical for silicons.

Fig. 1 The Darlington circuit (a) and a modified version (b) offering temperature compensation.

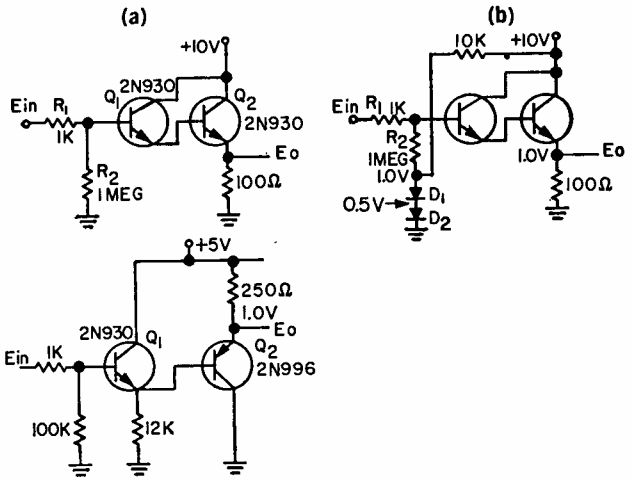


Fig. 2. Use of complementary transistors reduces offset voltages by cancellation.

Table 1

	Basic Ckt.		Modified Ckt.	
	0 C	50 C	0 C	50 C
V_{b1}	2.35	2.35	2.35	2.15
V_{b2}	1.75	1.85	1.75	1.65
V_{be1}	0.6	0.5	0.6	0.5
V_{be2}	0.75	0.65	0.75	0.65
V_{d1}	—	—	0.6	0.5
V_{d2}	—	—	0.6	0.5
E_o	1.0	1.2	1.0	1.0

Table 2

	0 C	50 C
V_{b1}	.85	.85
V_{b2}	.25	.35
V_{be1}	.6	.5
V_{be2}	.75	.65
E_o	1.0	1.0

Table 1. Voltage Levels in the Basic and Modified Darlington.

Table 2. Voltage Levels in the Complementary Circuit

Table 1 shows the effect on the output voltage of the temperature change. In the basic circuit, the 20 percent change in output could well have been a 100 percent change had the quiescent output been 0.2 v. Note how, in the modified circuit, the effect of ΔV_{be} of Q_1 and Q_2 on E_0 caused by temperature change is offset by identical changes in V_{d1} and V_{d2}.

A second approach to controlling the effect of V_{be} changes with temperature involves the use of complementary transistors as in Fig. 2. It is perhaps more subtle in that it virtually eliminates V_{be} offset voltages by cancellation.

If we assume the same quiescent voltages in Fig. 2 (Table 2) as in Fig. 1, then, at 0 C, $V_{be2} = 0.75$ v and $V_{be1} = 0.6$ v. But in Fig. 2, these voltages are of opposite polarity so the total offset voltage is the difference (0.15 v) rather than the sum (1.35 v), an improvement of nearly an order of magnitude.

At 50 C, $V_{be1} = 0.5$ v and $V_{be2} = 0.65$ v and, in Fig. 2, the total offset voltage is still 0.15 v rather than the 1.15 v of Fig. 1.

Though silicon transistors and diodes are used in these circuits, germaniums could be used just as well.

Low Cost Transistor Voltage Regulator

MANY APPLICATIONS REQUIRE an inexpensive, constant source of low voltage dc. Such a regulator, costing 5 to 7 times less than a zener diode, and having the same power rating, is given here. A further advantage is realized in that it can be set at the precise value of the voltage required, whereas the zener is purchased with a tolerance of 5 or 10 per cent.

This regulator was designed around a very inexpensive power transistor, the 2N554. By using a minimum of parts, and a silicon diode (1N462) for reference as opposed to a zener diode, the regulator was produced (in quantity) for less than two dollars.

The forward characteristic of the general purpose silicon diode was used rather than the back characteristic of a zener diode. A 2N404 transistor was chosen as a feedback amplifier because of its reliability, uniformity, and low cost. In addition, a 10 ohm thermistor was added to make the circuit perform at any temperature within the −55 to 71 C range. The input voltage source to this regulator is a sea water activated battery which has a voltage which varies from 12.5 to 14.7 v depending on salinity and temperature. The output voltage of this regulator, with design load of 600 ma, varies from 6.3 to 6.4 v over the voltage input and temperature ranges indicated.

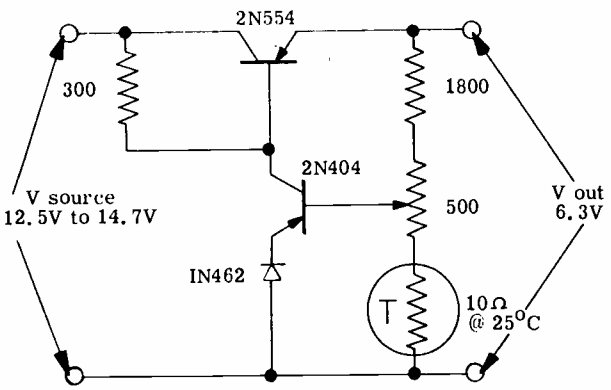


Fig. 1 Low cost transistor voltage regulator.

Transistor Voltage Regulator

IN THE CIRCUIT SHOWN, voltage V_z of reference diode D_1 causes a current I_1 to flow in the collector of Q_1. The current kI_1 flows through R_2 and $(1\text{-}k)I_1$ flows into the base of Q_2. The constant k will be a value equal to or greater than α_2 of Q_2. Current $(1\text{-}k)I_1$ causes a current β_2 $(1\text{-}k)I_1$ to flow through the reference diode.

Advantages of this circuit are: 1. High voltage operation. The only restriction is that $E_{cc} - V_z$ does not exceed the reverse break-down voltage of Q_1 or Q_2. 2. The output voltage is referred directly to a reference diode, and the output of this diode is stabilized by constant bias current which results from the constant reference voltage. Thus, the reference diode regulates its own bias current to a constant value.

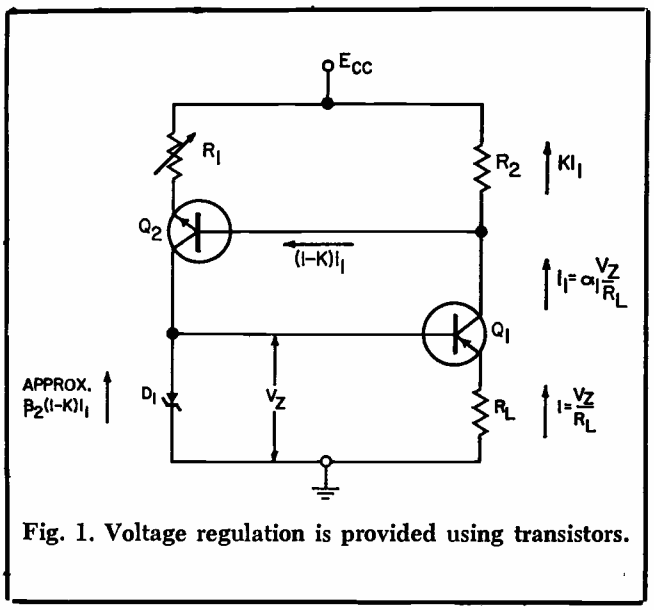


Fig. 1. Voltage regulation is provided using transistors.

Extentions of this circuit are possible. For instance, R_2 may be replaced by a low voltage zener. This will cause the effect of the load current on the reference diode bias current to be reduced by r/R_2, where r is the reference diode impedance.

Also, the regulator may be decoupled from the load by an isolation amplifier (series regulator amplifier), as shown in Fig. 2. This will further reduce the effect of the load current on the bias current.

Experimental values were found to be:
$V_z = -275$ v
$E_{cc} = -300$ v
$R_1 = 25$ K (adjusted for approximately ½ ma current to zener).

$Q_1 = 2N526$
$Q_2 = 2N335$
$R_L = 130$ K (2w)
$R_L = 20$ K (5w)
$R_L =$ (See Fig. 2)
$R_2 = 6.2$ K
R_2 replace by 10 v zener diode.
$R_2 = 6.2$ K

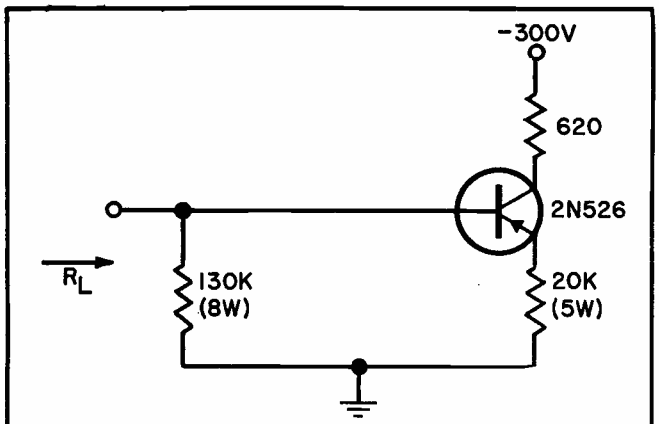


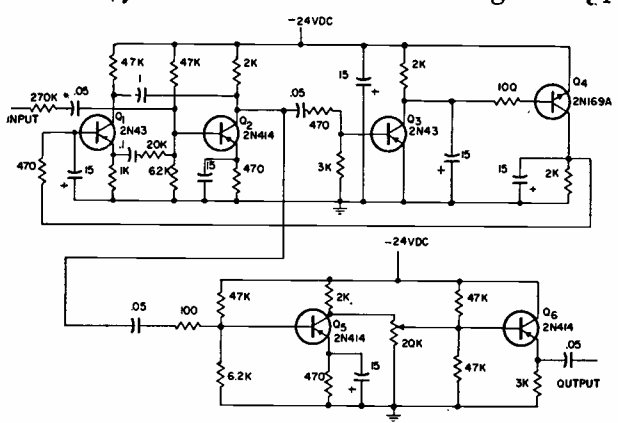
Fig. 2. Amplifier accomplishes good isolation.

AGC Amplifier

MANY APPLICATIONS require a constant output voltage over a considerable range of input variation. This circuit was designed for such an application. The input may be varied from 2 to 15 volts peak to peak with output variation from 8 to 10 volts peak to peak. This performance was adequate for our use, but an extension of the design can control more closely.

The conventional method of agc which controls gain by varying the current through an amplifier has a number of deficiencies. It is undesirable to change the operating point because of possible distortion. Transistors in general vary in gain by a useful amount only at low collector currents. This brings to mind the desirability of varying gain with a feedback loop. The accompanying circuit uses this principle.

Transistor Q_2 is the controlled amplifier, with Q_1 in a feedback path from collector to base. A bias variation on Q_1 will vary its resistance and hence vary the feedback. Control voltage for Q_1 is derived from the output of Q_2 by detection and a dc amplifier. Any variation of the output of Q_2 is reflected in a variation in the output of the dc amplifier. This changes the resistance of Q_1 in the feedback loop which varies the gain



Wide range of input voltage is handled by this agc amplifier.

of Q_2. An amplifier is shown after Q_2 to bring the output voltage to the desired level. The operating frequency of this circuit is 20 kc for our application, but it will operate from approximately 5 to 100 kc as shown, and any range desired with suitable component changes. Output variations may be reduced by a higher gain dc amplifier in the control portion of the circuit. Smaller capacitors in the dc amplifier will provide a faster response time to input variation, if desired for the application.

High Frequency DC Restoration with Gain

THE RETENTION of a fixed dc reference potential in association with a rectifier requires clamping. Basic circuits that perform clamping are shown in Fig. 1.

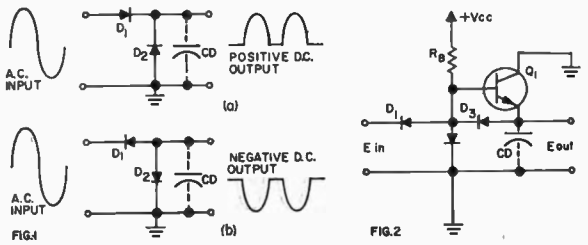


Fig. 1. Basic clamping circuits.

Fig. 2. Modified clamping circuit gives gain.

Diode $D2$ provides effective clamping at audio and low radio frequencies, but at higher frequencies the effects of distributed capacitance make the clamp unsatisfactory. The higher the input frequency, the greater the charge across C_D. This will, in effect, backbias diodes $D1$ and $D2$ and prevent complete restoration of the reference potential.

The difficulty can be resolved by the addition of a few components which use this reverse bias to effective advantage. The modified circuit, shown in Fig. 2, uses the reverse voltage developed across $D3$ to turn on transistor $Q1$ to provide a low impedance path to ground, hence giving effective clamping.

The circuit in Fig. 3 illustrates how the modified clamp is used with 500-kc sine wave input and 1-mc

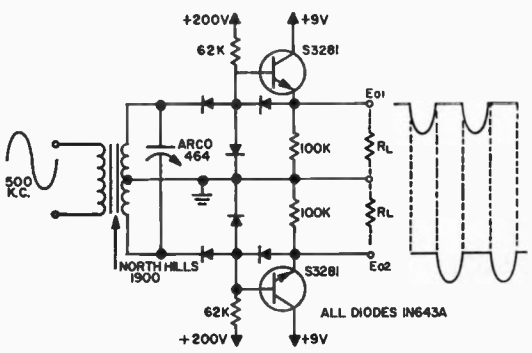


Fig. 3. Practical circuit for 500-kc-to-1-mc operation.

half-wave output. The transistor collectors are returned to a slight positive potential because of the large signal and supply voltages involved.

Zero Impedance Voltage Regulator

DESCRIBED is a zero output resistance voltage regulator using two transistors and controlled positive feedback.

A basic emitter-follower type voltage regulator, using a complementary compound connection, is shown in Fig. 1a. The raw dc input voltage, E_i, is pre-regulated by zener diode, Z, to a voltage level, E_z. The output voltage, E_o, is clamped to the zener voltage, E_z, through the base-to-emitter junction potential, V_{BE}, of transistor T_1. The output voltage, E_o, is

$$E_o = E_z - V_{BE} \tag{1}$$

The output resistance is essentially

$$R_o = \frac{r_e}{\beta_2} + \frac{r_b + r_z}{\beta_1 \beta_2}, \tag{2}$$

where r_b and r_e are the intrinsic r parameters of the base and emitter of T_1 respectively; β_1 and β_2 are the base-to-collector current gains of T_1 and T_2 respectively; and, r_z is the dynamic resistance of Z.

A method of reducing the output resistance to zero is shown in Fig. 1b. Most of the output load current, I_o, is sensed by sensing resistor, R_s. The voltage, V_s, thus developed is fed back through resistor R_f to the base of T_1. The feedback is positive; because, as output voltage E_o starts to drop due to a decrease in load resistance, the resultant increase in load current develops an increasing voltage, V_s, which when fed back to the base of T_1 through variable resistor R_f tends to

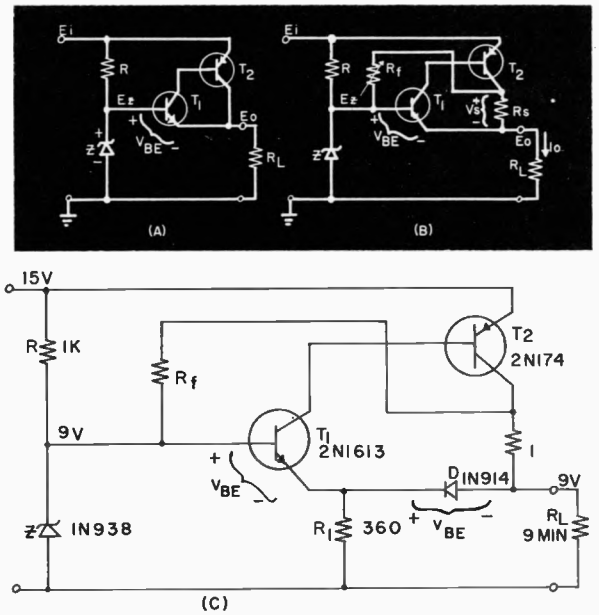


Fig. 1. Two-transistor voltage regulator; a. without feedback; b. with positive feedback; c. with positive feedback and temperature compensation.

raise E_o. A proper adjustment of R_f results in zero change in E_o as the load resistance is varied. The condition which must be satisfied is:

$$R_f = \frac{r_z}{R_o}(R_s - R_o), \qquad (3)$$

where R_o is given by Eq. 2. Hence, in order for R_f to be positive (real), R_s must be greater than R_o—the output resistance without feedback. Once R_f is properly adjusted to satisfy Eq. 3, it may be replaced with a fixed resistor of the same value.

Change in V_{BE} with temperature, resulting in output voltage drift, is a major disadvantage of the circuit in Fig. 1b. Positive feedback aggravates the condition. The circuit of Fig. 1c incorporates a temperature compensating diode, D, placed in opposite polarity but in series with the base-to-emitter junction of T_1. Ideally, the junction voltage of the diode matches the junction voltage of the transistor with variations in temperature. The output voltage then remains unaffected. For the diode to remain biased "on," the following condition must be satisfied:

$$R_1 < \beta_2 R_L \, . \qquad (4)$$

A measure of current overload protection is also offered by this circuit. The maximum load current that can flow ($R_L = 0$) is given by

$$I_o max = \beta_2 \frac{(E_z - V_{BE})}{R_1} \, . \qquad (5)$$

The component selection shown in Fig. 1c is for a nominal 9 v, 1 a supply. By placing a 50 ohm potentiometer between the emitter of T_1 and the cathode of diode D, with the wiper arm connected to R_1, the output voltage can be adjusted over a 1 v range.

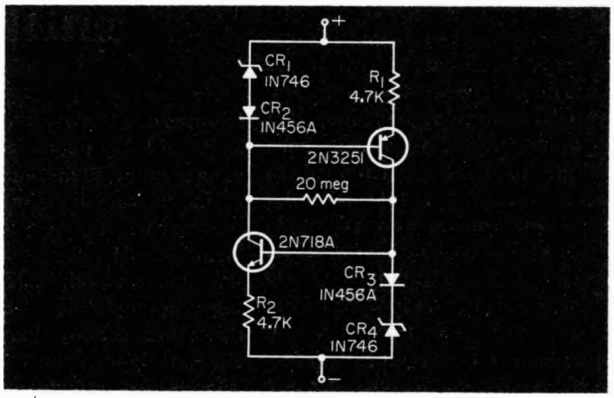
Two-Terminal Constant-Current Device

THIS CIRCUIT is unique in that it can be encapsulated and used as a single component in a circuit to achieve a constant current in the same manner that a zener diode is used to achieve a constant voltage.

The circuit consists of a pnp and an npn current source connected in such a manner that each regulates the other's reference. Another feature is that the current through the compensating diodes CR_2 and CR_3 is the same as the current through the base-emitter junctions, which improves tracking with temperature. The circuit is efficient in that no additional current is required to bias the reference as in a conventional current source.

Values given are for 1-ma current R_1 and R_2 can be changed for other currents. The circuit requires at least 8 v for proper operation. Maximum voltage is determined by transistor ratings.

The purpose of R_3 is to provide the initial turn-on of the circuit. The source of current for the zener diodes is the collector current of the transistor that feeds it. At first turn-on of the circuit, there is zero drop across the zener and visa versa (a bootstrap condition). The circuit will not start until a leakage current is provided. Once it is started, R_3 contributes nothing except its current, which is added to the total. It could, in fact, be disconnected.



Constant-current source.

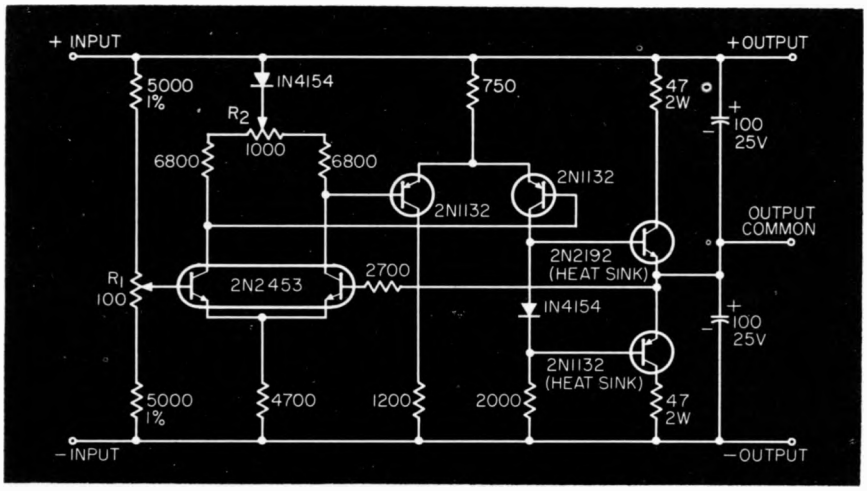
The compensating diodes compensate for changes in V_{be} with temperature. The temperature characteristics of a diode vary with currents hence the drop across the base-emitter diode and the compensating diode will more nearly track if the currents are the same.

Regulator Makes Two Power Supplies Out of One

CIRCUIT DEVELOPMENT work often requires a dual power supply with equal positive and negative voltages about a common bus. Use of two separate supplies is undesirable both because of the perpetual shortage of power supplies in a development laboratory and because of the need to use a differential voltmeter to measure and set each voltage to get good tracking between the two supplies. The circuit shown here permits a conventional power supply to be converted to a dual supply with precisely matched positive and negative outputs.

The circuit is constructed in a small box which plugs into the output terminals of a conventional supply and which has available binding posts for the positive, negative, and common outputs. In use the conventional supply is set to twice the required voltage. Once the circuit has been adjusted initially, the positive and negative voltages will track within several millivolts without any further adjustments.

The circuit as shown is a unity gain follower with the input referenced to a precision divider connected between the positive and negative inputs. With 20 V at the input, the open loop voltage gain of the amplifier is about 4000 and the closed loop output impedance is less than 0.05 ohms. The output current will be limited to about 150 mA by the beta of the output transistors or to a lower value, depending on the power dissipation of the output transistors. The circuit normally is used with output voltages between 5 and 25 V (input voltage between 10 and 50 V) with output currents of 100 mA or less. Note that the output current flowing in the positive and negative supplies can be much higher than 100 mA.



The initial adjustment of the circuit is made by comparing the output voltage with a precision voltage divider connected between the positive and negative inputs. Potentiometer R_1 is adjusted to balance the output voltage and potentiometer R_2 is adjusted to give good tracking of the output voltage with a precision voltage divider convoltage.

Equal positive and negative voltages generated from single polarity powerr supply.

An efficient focus-current regulator using the LM300

OTHER CIRCUIT designers have shown[1] how IC voltage regulators can be used in a wide range of applications — to regulate current as well as voltage. National Semiconductor's LM-300 is especially suitable for use as a current regulator, because it needs a low reference voltage of only 1.8 volts. This allows efficient operation, because only a minimum of voltage need be dropped across the current-sensing resistor.

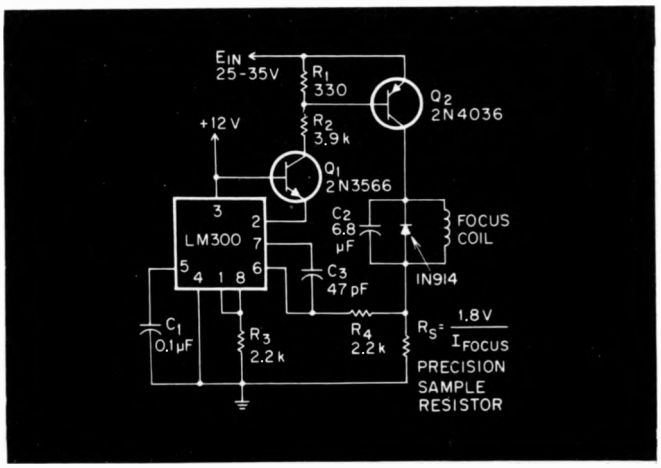
The circuit described here regulates the control current through a CRT focus coil. Unlike other focus-current regulators that use ICs, this circuit has separate supply voltages for the focus coil and for the IC. Thus the unregulated input voltage is not restricted by the maximum allowable input (30 volts) for the LM300. The entire input voltage, less the saturation voltage of Q_2 and the drop across the sensing resistor, is available to drive the load.

Output from the booster terminal (pin 2) of the LM300 drives Q_1 which is a common-base level-shifting stage. This in turn controls the pass transistor Q_2. Current through R_5 generates the comparison voltage which is fed back to the LM300 input (pin 6). Resistor R_4 provides the optimum source resistance for the feedback terminal of the IC. With a 2.2-kilohm source resistance, thermal drift is minimized and frequency compensation is satisfactory.

Capacitor C_3 provides frequency compensation for the LM300, while C_1 filters noise at the reference terminal (pin 5). The diode across the focus coil damps inductive kickback during turnoff. Capacitor C_2 filters sweep-induced transients. Resistor R_5 merely minimizes the dissipation in Q_1, and is not essential to the circuit action.

Circuit performance is excellent. Here is a summary of measured performance:

- Line regulation : <0.02% (ΔE_{in} = 25 to 35 V, I_o = 50 mA, R_L = 400 Ω).
- Load regulation : <0.05% (ΔR_L = 300 to 500 Ω, E_{in} = 30 V, I_o = 50 mA).
- Rejection of +12V : <0.1% (Δ12V = ±10%, I_o = 50 mA, E_{in} = 30 V, R_L = 400 Ω).
- Temperature stability : ≃ 0.3% (0 to +70°C).



In this precision focus-current regulator, the focus coil and the IC regulator are fed from separate voltage sources. Thus the unregulated input voltage can exceed the allowable maximum for the IC.

Temperature performance is primarily determined by the IC, so the manufacturer's data should be used instead of the measured value to determine worst-case performance. In critical applications, other IC types (for example, the LM-100) can be substituted for the LM300 to give improved temperature stability.

The circuit as shown will handle focus-coil resistances of 400 ohms, ±10 percent, at temperatures up to 50 degrees C — with a 30-volt supply and a maximum load current of 50 milliamps. Higher currents can be controlled if Q_2 is replaced by a higher-power transistor such as the 2N3740.

Reference

1. R. J. Widlar, "New Uses for the LM100 Regulator," *Application Note AN-8*, National Semiconductor Corp., June 1968.

CRD simplifies design of voltage regulators

A RELATIVELY new device, the field-effect current-regulator diode, can replace four discrete components in conventional voltage-regulator circuits. Thus it reduces the size and cost of these circuits and improves their reliability.

Current-regulator diodes (CRDs) are available from two manufacturers, Motorola and Siliconix. Basically, the devices can be regarded as n-channel FETs with an internal short from gate to source. Fig. 1 shows the equivalent circuit and the conventional symbol for a CRD.

The diodes are normally operated above pinch-off on the $V_{gs} = O$ curves, as shown in Fig. 2. At voltages higher than V_P, changes in drain-source voltage (V_d) result in very small changes of drain current (I_d). Thus, above pinch-off, the current through the device remains essentially at I_P, and the CRD functions as a constant-current source. Note the duality of the CRD with the zener diode which is, of course, a constant-voltage source.

The dynamic impedance $\Delta V_{ds}/\Delta I_d$ of CRDs is normally very large. Motorola's diodes

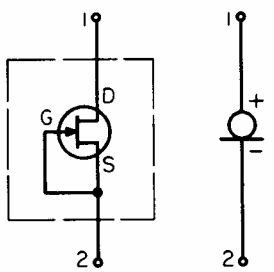


Fig. 1. A current-regulator diode behaves like an unbiased n-channel FET. The device is normally represented by the symbol shown right.

(1N5283-1N5314) have minimum dynamic impedances ranging from 235 kΩ to 25 MΩ, depending on the value of I_P. Available pinch-off currents range from 0.22 to 4.7 mA.

In a conventional feedback voltage regulator, shown in Fig. 3, the output voltage of the error amplifier should result only from the difference between the sampled output voltage and the reference voltage. Unfortunately, unwanted error-amplifier signals can be produced by changes in bias voltage. The error amplifier derives its bias from the unregulated input voltage which may have ac ripple and dc level shifts superimposed on it. To eliminate the effect of input variations on the bias voltage, a preregulator stage is normally connected as shown.

Figure 4 compares a conventional transistor preregulator with the simpler approach using a single CRD. Both circuits give about the same performance, but the CRD circuit costs less. At present, the cost advantage is only about $1.00, but the gap should eventually widen when increased demand lowers the cost of CRDs.

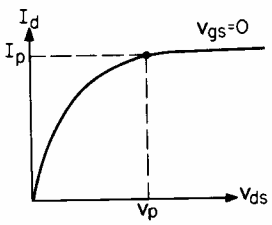


Fig. 2. When biased above the pinch-off voltage V_P, the CRD forms a constant-current source.

A complete voltage regulator, using a CRD prereg, is shown in Fig. 5. This circuit delivers up to 200 mA at 10 V. Load regulation is 0.1% (zero to full load), and line regulation is 0.02% (for 2 Vrms input ripple at 400 Hz).

In choosing the right CRD for use as a preregulator, the circuit designer should consider the following interrelated factors:

- Temperature coefficient of the CRD.
- Quiescent operating point of the error amplifier.
- Maximum output current of the regulator circuit.

Current through the CRD is temperature dependent. The direction and magnitude of the tempco depends on the pinch-off current. Because variations in CRD current can cause variations in output voltage of the regulator circuit, one should estimate the allowable drift before specifying the diode. One should then select a CRD whose pinch-off current falls within the range that gives acceptable tempco.

The exact pinch-off current is dictated by the design of the error amplifier. The amplifier should be biased to give high gain and low temperature drift. For example, in Fig. 5, the RA1 error amplifier is specified by GE to give minimum drift at a bias current of 0.5 mA. Thus, a CRD (1N5291) with a nominal I_P of 0.504 mA was chosen.

One should check to see that, when multiplied by the current gain of the series control elements, the CRD's current rating exceeds the maximum expected load current.

One should also check that the rated dissipation of the CRD won't be exceeded. Motorola's CRDs have an allowable dissipation of 600 mW.

Of course, for constant-current operation, the applied voltage should be greater than V_P. Also, to avoid avalanche breakdown, the applied voltage should be below the rated V_{max}. For Motorola's CRDs this figure is 100 V.

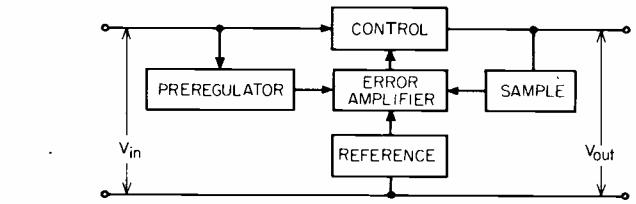


Fig. 3. Simplified block diagram of feedback voltage regulator. Prereg circuit biases the error amplifier.

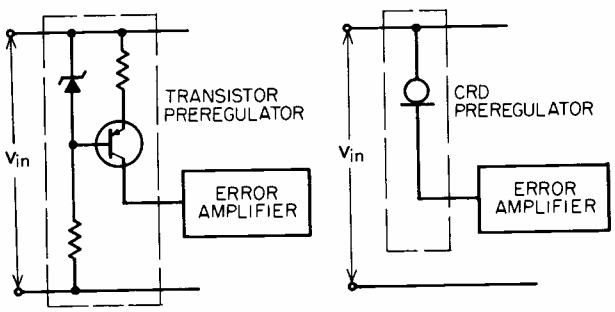


Fig. 4. Conventional transistor prereg with four discrete components can be replaced by a single CRD.

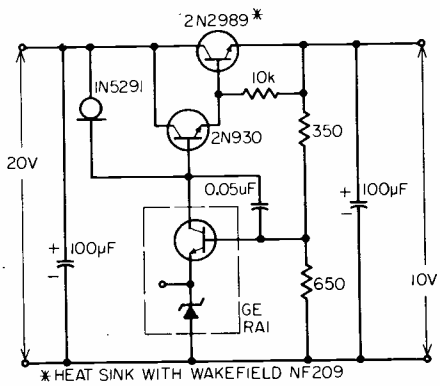


Fig. 5. Complete voltage regulator using a CRD prereg. Circuit is designed for a load current of 200 mA.

FET improves voltage regulation and allows current limiting

IN THE OTHERWISE conventional regulator circuit of Fig. 1, a FET constant-current source has been used instead of a resistor to provide current for zener diode CR_1. This arrangement makes the feedback amplifier less dependent on regulator input voltage and load current. Thus it improves the voltage regulation. As a bonus, the circuit shown also provides automatic current limiting.

The constant-current source is shown inside the dashed-line rectangle. Resistor R_S is selected to bias the FET at a drain current I_D of approximately 4.5 mA. This current is sufficient to supply the collector of Q_2 and to bias CR_1.

Zener voltage V_z provides a near-constant voltage across R_3, regardless of the setting of R_1 (or output voltage V_o). Choice of input voltage V_{in} is restricted by the following relationship $V_{in} \geq V_{o\ max} + V_z + V_{po}$, where V_{po} is the pinch-off voltage of the FET. The circuit shown was designed for an input of +45 V. With a 10-kΩ potentiometer for R_1, output is adjustable from approximately +6.5 V to +35 V.

Network, Q_4 and R_4, provides automatic current limiting. When load current reaches the predetermined limiting value, voltage drop across R_4 biases Q_4 into conduction. Because the transistor bypasses CR_1, bias voltage V_z is removed and, hence, voltage across R_3 is reduced. When this occurs, there is no longer sufficient base current to Q_5 (and hence Q_6) to allow further increase in load current. Current in R_4 can no longer increase because any increase would only tend to back-bias Q_6 still further.

Figure 2 shows typical output characteristics for two nominal voltages, 30 V and 10 V. Also shown are curves of percent regulation versus load current for the same two nominal output voltages. Note that load current is limited to just over 40 mA. At normal load currents, regulation is better than 0.1 percent.

The circuit shown is merely one example of the technique. The same constant-current source can be used in a variety of regulator circuits. This circuit could possibly be further improved by replacing R_7 with a constant-current source also.

Another possible circuit improvement would be to connect the collector of Q_4 to the base of Q_5. This would have little effect on regulation but could improve the current limiting. With the alternative arrangement, Q_4 would need to absorb only the current given up by Q_2 during current limiting. With component values shown, this current is about 3 mA. Thus Q_4 would dissipate less power.

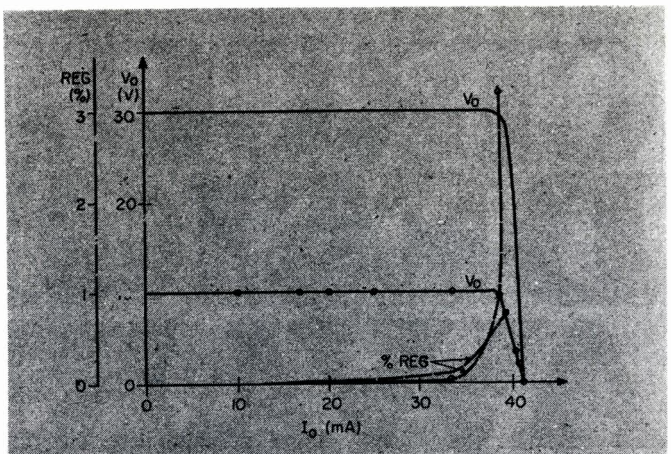


Fig. 2. Typical output characteristics and regulation characteristics for nominal output voltages of 30 V and 10 V. Note the current limiting at around 40-mA load current.

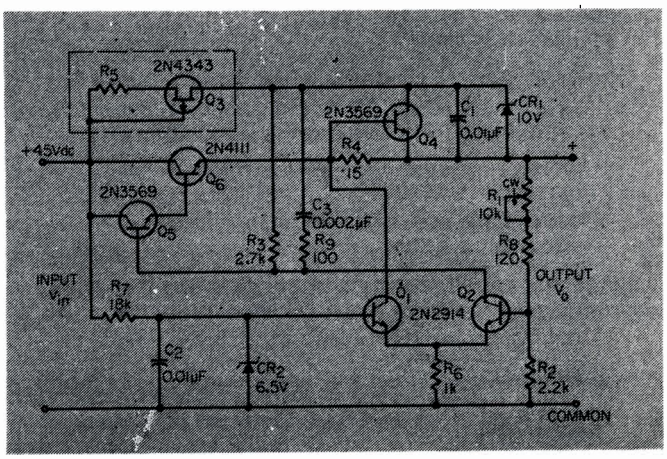


Fig. 1. In this voltage regulator, the FET constant-current source (inside the dashed rectangle) provides improved regulation, because current through CR_1 is independent of input and output voltages.

Temperature-stabilized constant-current source

By careful design, one can greatly improve the temperature stability of a conventional common-base current source. Using an extra transistor, and matched components, the modified circuit gives an output current that's extremely stable over a wide range of ambient temperatures.

Let's look first at the conventional circuit shown in Fig. 1. It works as follows: Diode D_1 provides a constant-voltage source for the base of Q_1. Because the base-to-ground potential is fixed, emitter current is essentially determined by R_e. Then,

$$I_e = \frac{V_b - V_{be}}{R_e} \qquad (1)$$

But the V_{be} term can become quite significant, especially at low zener voltages. However, we would like to operate at these lower voltages so that less power will be dissipated in the regulating transistor Q_1.

One solution to the problem is to choose a zener diode such that its net TC is approximately equal to the TC of Q_1's base-emitter junction. (This is about −2 mV/°C.) Then we have a combination which is

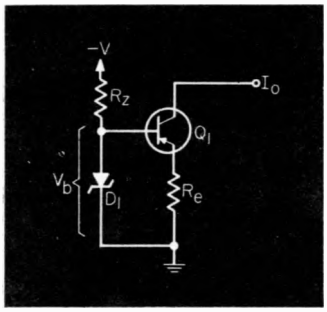


Fig. 1. A conventional grounded-base current source has the disadvantage of poor temperature stability.

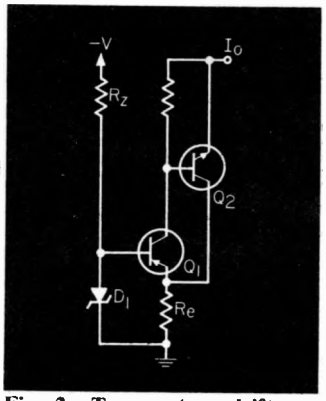


Fig. 2. Temperature drift can be minimized by matching the TCs of D_1 and Q_1's V_{be}. There is little internal temperature rise in Q_1, because Q_2 handles the bulk of the load current.

temperature-compensated, assuming that D_1 and Q_1 track reasonably well with temperature. A typical 4.3 - volt zener diode has a nominal TC of 0.037%/°C. This works out to 1.6 mV/°C, which is a fairly close match to the TC of Q_1's base-emitter junction.

To ensure that Q_1 and D_1 will accurately track, in a practical circuit, we must hold their relative temperature constant. But, of course, if Q_1 has to handle emitter currents larger than a few milliamps, the dissipation will cause an internal temperature rise in the transistor.

Figure 2 shows how we can overcome the dissipation problem. The added transistor Q_2 carries the major portion of the load current; Q_1 merely supplies base drive for Q_2. The load current still flows through R_e, so the regulating property of the circuit is unchanged.

In the complete working circuit of Fig. 3, the emitter resistance is adjustable, so that the load current can be set to the required value. A bypass capacitor minimizes noise voltages across the zener. The 390-ohm resistor biases the zener to around 20 milliamps, thus providing a low-impedance source at Q_1 base.

With the components specified in Fig. 3, the load current changes less than 0.5 percent with ambient temperatures in the range 0 to +70°C. With a 400-ohm load, the circuit shown will deliver 50 mA.

If the higher currents are needed, a third transistor can be Darlington-connected to Q_2, with its collector returned to R_e. Of course, the value of R_e will need to be reduced. Its value can be calculated by dividing I_e into V_e. Then,

$$R_e = \frac{V_{D1} - V_{be}\ (Q_1)}{I_e}$$

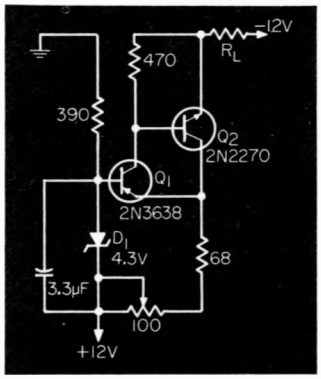


Fig. 3. In this practical circuit, the emitter resistance can be adjusted to set the load current. The zener is bypassed to minimize noise.

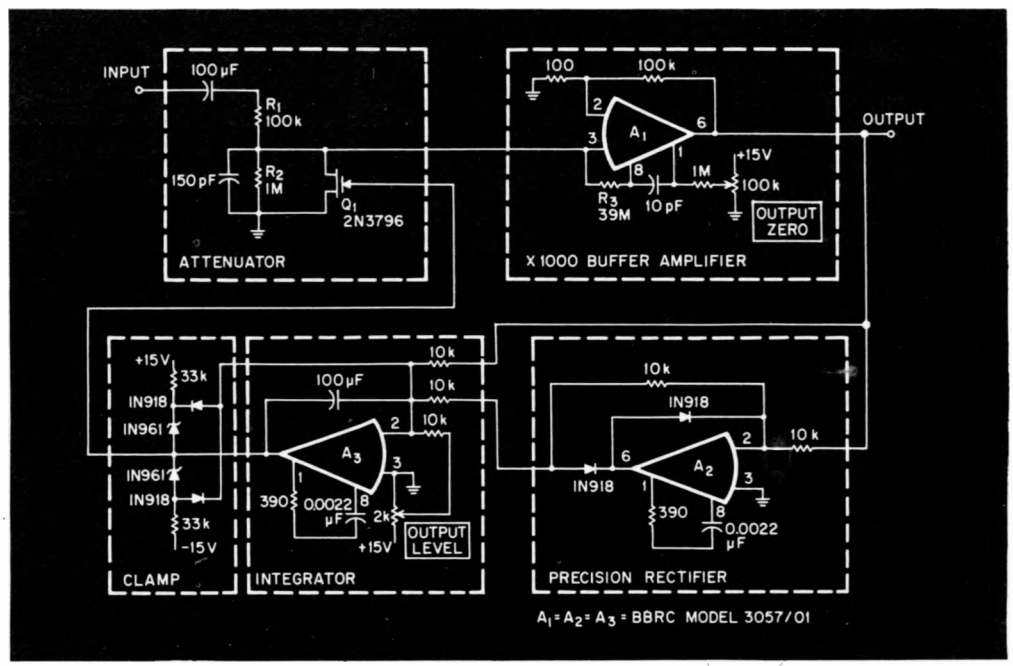
With a 4.3-volt zener, this reduces to $R_e = 3.7/I_e$.

A stable constant-current source lends itself to many circuit applications. Some obvious applications include differential amplifiers, timing generators, long-tailed emitter followers and FET stabilizers.

MOS-FET provides 60-dB dynamic range low-frequency AGC circuit

CONVENTIONAL transistor AGC circuits vary the gain by controlling the base bias current. The ratio of the range of transductances available between saturation and cutoff is about 40 to 1 (32 dB). This defines the range of automatic-gain control possible with conventional circuits.

The circuit in the figure uses an insulated-gate FET to increase the controlled gain range to about 1000 to 1 (60 dB). The ratio of the off resistance to the on resistance of the FET sets the theoretical limit of the range. However, the input impedance of the



Schematic of MOS-FET AGC circuit.

associated buffer amplifier as well as noise pickup limit the practical off resistance.

R_1, R_2 and Q_1 form a variable attenuator which is controlled by the output of amplifier A_3. The attenuation can vary from 0.9 to 0.0009. Amplifier A_1 is set at a gain of 1000 and is operated non-inverting to prevent loading of the attenuator. The output is full-wave rectified by A_2 and fed to amplifier A_3 along with a reference from the 2-kΩ output-level potentiometer. Amplifier A_3 integrates this sum and applies it to Q_1 to complete the feedback loop. The clamp circuit is placed around A_3 to prevent saturation with zero or overload input signals. R_3 is used to compensate the bias current of A_1. Both R_3 and the zero control can be omitted if amplifiers A_2 and A_3 are capacitively coupled from the output. ■

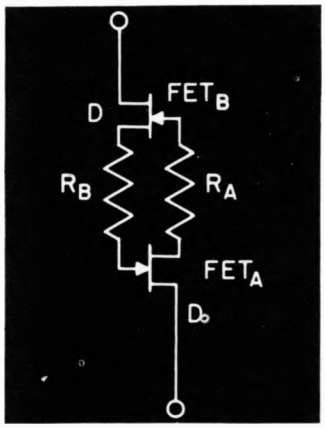
An inexpensive bipolar current limiter

WE OFTEN need a bipolar current-limiting diode. For this, two commercially-available diodes must be placed in an opposing-series connection. The circuit shown uses two similar FETs and two resistors to create the same function at a cost below that of one current-limiting diode.

The circuit is a straightforward FET current source, using source resistance to establish the current level. One FET operates in the normal sense while the other has a forward-biased gate to complete the current path. The forward-biased FET channel resistance connects the gate of the operating FET.

Making the two resistors R_A and R_B variable allows unequal currents for the two polarities. Making one resistor fixed and the other variable allows close matching of the two current levels.

Good results have been obtained with the low cost 2N3819 FETs, or with a matched dual FET, such as the 2N5199. Use 5% resistors for relatively well-matched currents. ■



Low cost method to obtain variable bipolar current limiting.

High-efficiency series regulator

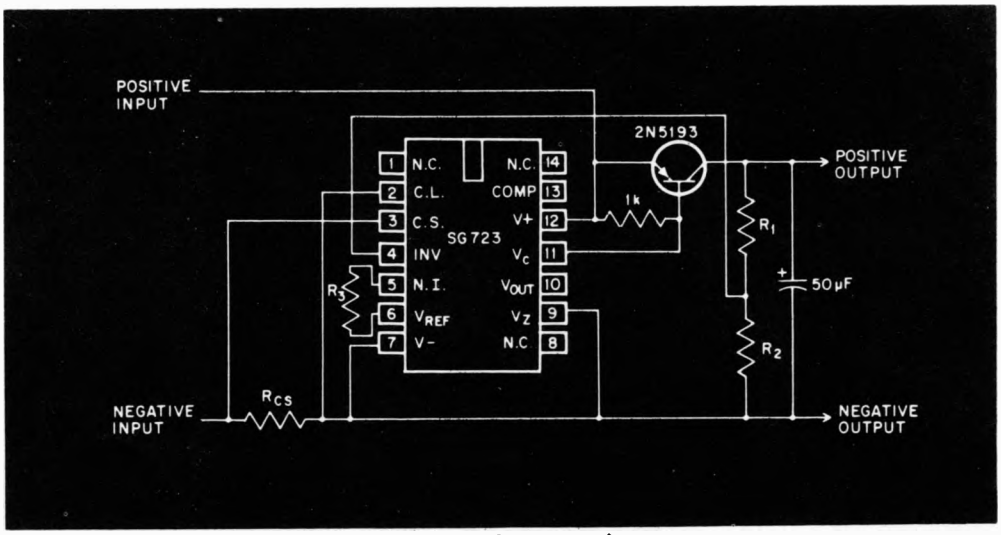
THE MAJOR FACTOR limiting efficiency in a series regulator is the minimum input-output voltage differential required for proper operation. Today's monolithic regulators require two to three volts, depending on supply current, to keep the output in regulation. Using the SG723 in the configuration shown reduces this differential to 0.5 V, even for an output current of several amps.

A series-pass transistor internal to the SG723 is used as a grounded-emitter amplifier to drive an external pnp power transistor. This modification, shown in the figure, allows the pnp transistor to be driven into saturation while providing proper biasing for the rest of the circuitry.

This circuit has excellent regulation due to the two additional stages of voltage gain. The added gain can cause stability problems but the large output capacitor (50 μF) acts as a brute-force stabilizer.

Current limiting using the internal shut-down transistor must be done in the negative line. This is necessary because the collector of the transistor tied to the compensation terminal is at a voltage lower than the output.

The normal divider equations for the basic regulator apply. Note that the V_Z terminal is used (available only in the N package), although an external 6.3-V zener could be used at the V_{out} terminal. ■



Positive high-efficiency regulator uses an external pnp transistor. Minimum $V_{in} = V_{out} + 0.5\ V = R_{cs}\ I_{L^*}$ Output = 7 to 37 V.

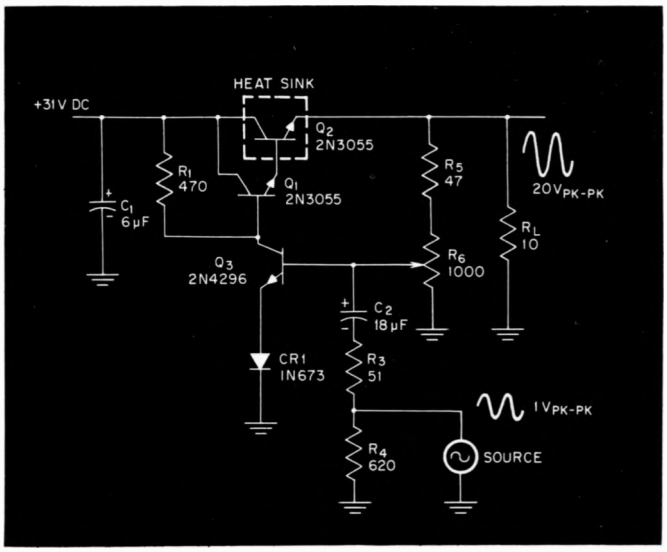
Modulated dc voltage regulator

A SERIES regulator, normally used to regulate the dc output of a power supply, can be amplitude modulated to produce an ac output across a low impedance (10 ohms). This allows the regulator to be used as a power amplifier having high gain and good efficiency.

In the circuit, C_2, R_3 and R_4, and a 600-Ω ac source have been added to modulate the regulator. A sine wave applied to the base of Q_3 through C_2 causes the output across R_L to vary at the same rate. Increasing the amplitude of the applied sine wave increases the output amplitude. R_6, which normally controls the dc output, can be adjusted to set the operating point of the regulator to obtain maximum ac swing across R_L.

The response of the circuit is flat from 1 kHz to 20 kHz at 20 V pk-pk into the 10-Ω load. Below 1 kHz the frequency response falls off due to coupling capacitor C_2. The low end can be extended to dc if R_3 is made larger and C_2 shorted. Under these conditions a larger modulating voltage is necessary for the base drive to Q_3.

Using the forward drop of a silicon diode (1N673) as the reference, one can obtain an undistorted output of 27 V pk-pk across R_L. If the input to the base of Q_3 is overdriven by the modulating signal, a clipped sine wave of 29.5 V pk-pk into the 10-Ω load can be obtained.



Modification of a conventional dc series regulator yields a low-impedance, high-output audio source.

The power transistors used for Q_1 and Q_2 have a cutoff frequency of 20 kHz. With better transistors one can extend the upper limit of the frequency response. ■

High-efficiency series regulator

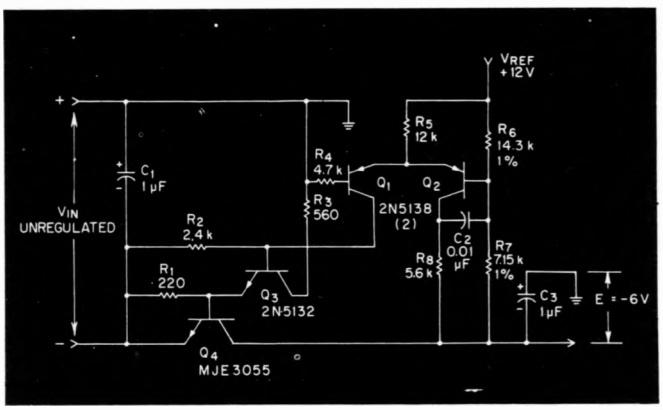
A BASIC problem in low-voltage (5-6 V) power supplies for ICs is efficiency, as quite commonly the regulated output is a small percentage of the input voltage. So the voltage drop across the series-pass transistor can approach the magnitude of the voltage delivered to the load, particularly at high ac-line inputs. As a consequence, reducing the minimum input-output differential of the regulator can substantially reduce series-transistor dissipation and thus greatly enhance efficiency.

A direct approach to reducing the series-transistor bias requirement is to arrange the circuit so that no device junction(s) appear in series with the output. As a result no operating bias (various V_{be}'s) can subtract from the available output and the minimum input voltage required for regulation is reduced to the output voltage plus the pass transistor's V_{ce}(sat).

A practical example is shown in the figure where a pnp differential pair (Q_1-Q_2) drives a pseudo-Darlington combination (Q_3-Q_4). An auxiliary bias supply is used both to supply regulated emitter current to the differential amplifier and to establish a voltage reference for output comparison.

The key to the low input-regulation threshold is the drive connection of Q_4. With Q_3's collector current derived from the positive input leg (rather than Q_4's collector as in a conventional Darlington) Q_4 can operate down to a minimum V_{ce} approaching saturation — while Q_3 is still supplying active base drive, and can do so until Q_4 is hard into saturation and the regulator loses control. An additional virtue of this connection is the ability to limit output current by forcing Q_3 to saturate (via the voltage developed across R_3) and limit Q_4's base drive to a safe maximum under short-circuit conditions.

The rest of the circuit is straightforward. R_8 and C_2 frequency compensate the differential amplifier Q_1-Q_2. The scaling output divider (R_6-R_7) compares the −6-V output to the +12-V reference at one input of the diff amp. The opposite input is ground referenced through a resistance equivalent to the divider's dc impedance. The tantalum input and output capacitors (C_1 and C_3) are typical solutions to the stability problems associated with normal connections to sources and loads.



Low-cost voltage regulator provides high efficiency by reducing the required input voltage.

This particular circuit handles loads up to 300 mAdc with load regulation of 1% (or an R_o of 20 mΩ). Line regulation, due to the low output conductance of Q_1, measures less than 0.5 mV/V of input change (or 66 dB of rejection to input changes). The input-output differential is directly proportional to the saturation characteristics of Q_4 and the output-current level. The device used in the figure requires only 370 mV of V_{ce} across Q_4 to sustain regulation at 300 mA.

These characteristics are obtained quite economically, as all active elements are inexpensive plastic devices. Of the passive elements, only the tantalum capacitors are costly. The total component cost is about $2. ■

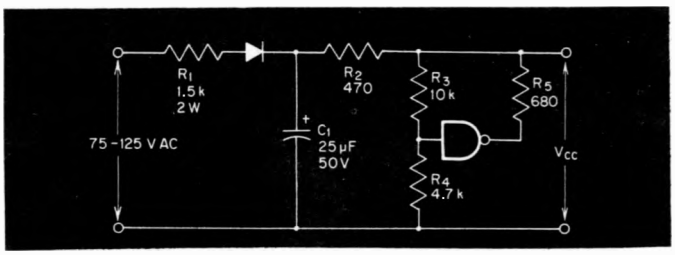
Spare IC gate serves as regulator

AN UNUSED gate in a multiple-gate IC can serve as a zener regulator. In one case, it was necessary to derive 12 Vdc (for a digital IC and a reed relay) from an ac line that varied from 75 to 125 V. To cut costs, the 12-V supply was developed from the ac line by a half-wave rectifier and a line-dropping resistor.

But the wide variation in line voltage and variable demands of the load required some kind of regulator and a zener would have been too costly.

In the circuit shown, an unused gate in an Amelco 303CJ (a quad 2-input NAND buffer capable of sinking 60 mA), was used as an active regulator. The input switching level in the 303CJ is quite constant from one IC to another and also very temperature stable. Other NAND or NOR gates could be used as well.

In the circuit, R_3 and R_4 bias the gate in its active region while R_5 reduces power dissipation in the output transistor. If V_{cc} tries to rise, the gate input rises. This makes the output go lower, thereby drawing more current through R_2, which causes V_{cc} to decrease.



This simple circuit uses a spare IC gate from an Amelco 303CJ to regulate a +12-V supply derived from a widely varyiug acliue voltage.

The circuit supplies 6 to 10 mA and V_{cc} varies from 11.4 to 11.5 V as the line varies from 75 to 125 V. The circuit works well from 0 to 75°C.

The circuit can be used, too, where the supply voltage is constant, but load current changes. It is then necessary to change values of R_1, R_2, R_5 and C_1. Supply cost, excluding the gate, is about $2 in single quantities, $1 in 100-up. ■

Short-protected current limiter ignores inrush currents

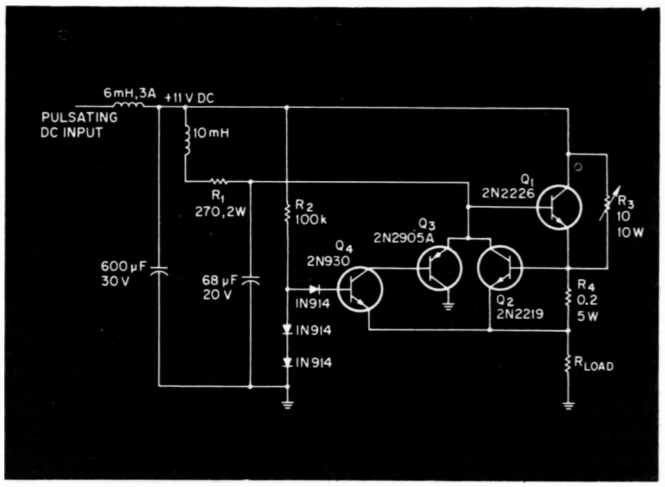
THE SIMPLE CURRENT limiter in the figure protects itself from overdissipation in case of a shorted output. It also distinguishes between a shorted output and capacitive or cold-filament loads which can momentarily look like shorts.

As soon as the current in the circuit exceeds the limit value, 3 A in this case, the voltage drop across the current-sensing resistor R_2 exceeds the cut-in voltage for the emitter-base junction of Q_2. This causes Q_2 to conduct, thereby limiting the base drive to Q_1.

If the load resistance is reduced to zero, Q_4 conducts and Q_3 saturates, thereby turning Q_1 off, and the current is limited by R_3 in series with R_2.

If the load is a filament, R_3 is necessary to allow the circuit to operate. If R_3 is omitted, then when power is applied, Q_4 conducts and Q_1 saturates, keeping Q_1 off. If R_3 is added, a "starting" current flows through R_3 and R_2 to the load.

R_3 is adjusted so the starting current is large enough to begin heating a cold filament. As the filament voltage increases to about 100 mV, Q_4 and Q_3 turn off, allowing the load current to rise to the 3-A limiting value. ■



Though protected against short circuits, this current limiter will deliver momentary high current to uncharged capacitors or cold filameuts.

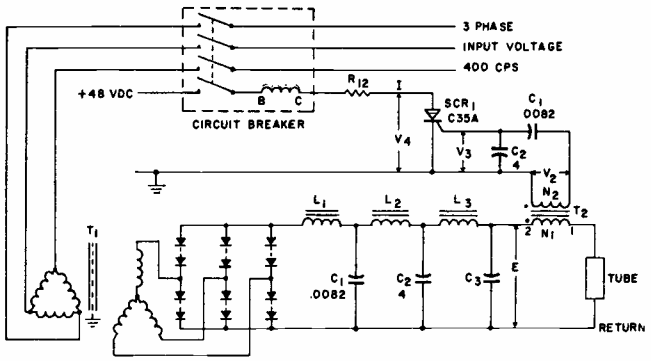
Section 3
PROTECTION CIRCUITS

High Voltage Power Supply Protective Circuit

WHEN a high voltage power supply is used to operate a klystron power amplifier there should be a means of protecting the high voltage power supply from damage due to excessive current drain. The most common cause of excessive current drain is a short circuit in the power amplifier. One approach to the problem is to remove line voltage from the power supply when a short circuit occurs at the load. To provide adequate protection the protective circuit must be extremely fast acting.

The circuit described here and shown in Fig. 1 consists of a high voltage power supply with an efficient protective circuit. This circuit can remove primary power from the power supply within a period of 8 to 15 msec after a malfunction has occurred at the load. The power supply illustrated is operated from three phase 440 volts at 400 cps and delivers 15 kv dc to the load. The protective circuit consists of pulse transformer T_2, a silicon controlled rectifier, and a circuit breaker.

The primary winding of T_2 is connected in series with the load at the output of the power supply. Voltage drop across this winding is negligible so the full power supply potential is applied to the load. When the load becomes short circuited, the primary winding of T_2 takes the place of the load across the power supply output so the potential between terminals 1 and 2 of T_2 is equal to the power supply voltage. This voltage requires a few microseconds to develop due to stray capacitance in the primary winding of T_2. At the same time a pulse is induced in the secondary of T_2. The pulse amplitude is determined by the power supply voltage, E, times



the ratio of secondary turns to primary turns of T_2, or $N2E/N1$. This pulse is coupled through capacitor C_1 to the gate of silicon controlled rectifier SCR_1. The voltage, V_3, applied between the gate and cathode of SCR_1 is determined by the following equation; $V_3 = C_1/(C1 + C_2) \cdot N_2/N_1 \cdot E$.

When SCR_1 is triggered by the pulse, it conducts, drawing current through the trip coil of the circuit breaker and R. Current I increases rapidly to its maximum value of 48-1/R and the voltage applied between anode and cathode of SCR_1 drops from $R/48$ v to one dc. Current flowing through the trip coil opens the circuit breaker removing line voltage and the anode voltage applied to SCR_1. The circuit breaker is reset manually after the load has been repaired or replaced. Time required for this circuit to turn off power is within 8 to 15 msec which is sudden enough to protect components of the power supply from damage.

Care must be taken to apply a pulse of correct amplitude to the gate of SCR_1. If the pulse is too great, SCR_1 will be damaged and too small a pulse will not trigger SCR_1. Switching time for the C35A is 2.5 μsec when current flow is 4 amps dc. Faster switching time could not be achieved with higher values of I. Values of C_1 and C_2 were obtained by trial and error to reach the correct value of V_3.

The trip coil of the circuit breaker was designed for a current value of one fifth of that used. The principles involved in this protective circuit can be used with any power supply where rapid turn off is required for protection due to a sudden fault at the load.

Automatic Overload Circuit

THE CIRCUIT described is an overload sensing device which will interrupt an applied voltage in the event of an overload, and sample at approximately one second intervals to ascertain whether or not the overload still exists. If the overload is removed, normal voltage will be restored; however, if the overload continues to exist the circuit will cycle, continuing to monitor the load until the overload is removed.

The circuit operates as follows: R_1, R_2, R_3, and Q_1 comprise the current sensing network. R_1 is chosen to keep its voltage drop constant at 0.60 v when the desired rated current is drawn (in this case, approximately 2.3 a). This drop is sufficient to forward bias the emitter-base-junction of Q_1 and cause it to conduct. The collector of Q_1 then swings from ground potential to +v. This positive going voltage is then applied to the base of Q_2 via R_4 and C_1. Potentiometer R_3 permits current trip adjustment of approximately ±20 per cent to be made.

Transistors Q_2 and Q_3 comprise a one-shot multivibrator which has a period of approximately 500 ms and is triggered by the output of the current sensor portion. The operation of this multivibrator is straightforward. Briefly, Q_2 receives a trigger at its base which causes it to go into forward conduction, bringing its collector to ground potential. This negative-going voltage is coupled to the base of Q_3 through C_2, causing the base drive to Q_2 to be interrupted with subsequent turn-off of Q_2. This causes the collector of Q_2 to go to approximately supply potential and in turn supply base drive Q_4 directly through R_8. Q_2 is held in the "on" state for the duration of the period of the multivibrator.

Transistors Q_4 and Q_5 are connected in a time stretch and recovery circuit. Transistor Q_4 is an emitter follower current amplifier which transforms a high impedance drive from the output of the multivibrator to a low impedance in order to facilitate rapid charge of C_3 through CR_1. Diode CR_1 also prevents rapid discharge of C_3 by R_9 upon completion of the period of the multivibrator. A dc return for the base of Q_5 is provided by R_{10}. Capacitor C_3 functions as a time stretch and reverse integrator which performs two distinct operations simultaneously: 1. The time stretch serves to allow sufficient time for the multivibrator to recover in case of a repeat cycle; 2. **The reverse integrator** permits the voltage to be gradually reapplied to the load instead of a step function. This prevents high surge currents and serves to protect regulator and associated power supply components.

Transistor Q_5 is connected as an emitter follower which presents a high impedance to the time stretch and recovery circuit so as to minimize loading. The output of this emitter follower drives the base of Q_6 which is connected for operation as a switch. The collector of Q_6 is connected to the base of Q_7. Potentiometer R_{13} allows the ouput voltage to be adjusted to the desired level. In the event of overload, the previously described circuits go into operation and Q_6 shorts the base of Q_7 to ground thus removing the voltage from the output.

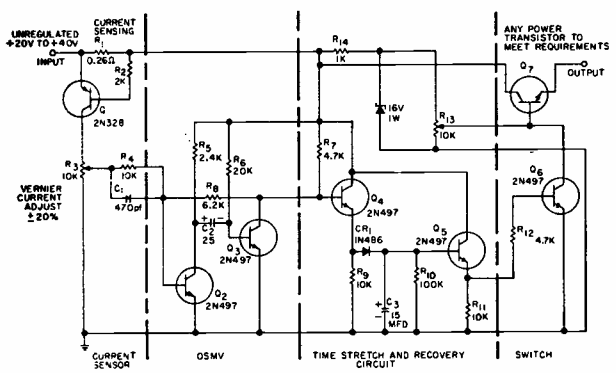
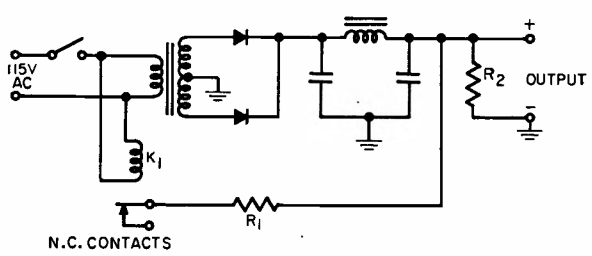


Fig. 1—Overload sensing and control circuit.

Capacitor Discharger

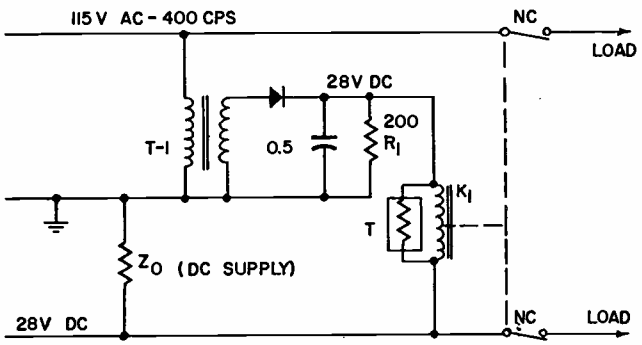


Relay discharges power supply capacitors rapidly and safely.

THE RESIDUAL charge on power supply capacitors maintains an output voltage for a considerable time after shutting off the input power. This is objectionable for the testing of computer flip-flop modules, where a zero starting voltage is required.

Reducing the ohmic value of bleeder resistor R_2 will reduce the discharge time, but this also lowers the output voltage and wastes power. An effective solution is shown in the diagram. When power is turned on, the normally-closed contacts of relay K_1 open up, shutting off input power, de-energizing K_1, and causes its contacts to close. This, in turn, discharges the filter capacitors C_1 and C_2 through resistor R_1. Resistor R_1 is a low-ohmage (25 to 50 ohms), high-wattage, current-limiting element which permits rapid discharge at a rate low enough to prevent burning of the relay contacts.

Differential Voltage Circuit Protector



Differential relay circuit provides over and under voltage protection.

THE CIRCUIT described has the unique feature of offering undervoltage, overvoltage and ac or dc failure protection for equipment being life tested or running for long periods unattended. In military aircraft equipment operating from 28 v dc with cooling fans operating on 115 v ac, failure of the ac line and subsequent loss of cooling can cause rapid deterioration of the circuits. When either the ac or dc power fails the relay circuit shown here operates to open its normally closed contacts to the load circuits. By selection of a relay with a low pull-in voltage the circuit can be made to operate in such a way as to open the load circuits when the ac or dc voltage falls below or goes above a certain value. Transformer T_1 provides isolation and step-down of the 115 v line to match the 28 v at the other end of relay K_1. If K_1 were selected to operate on 6 v any change in ac or dc resulting in the 6 v difference would actuate the relay and open the power to the load. If desired, a third set of contacts can provide an alarm indication. Resistor R_1 will provide current limiting for the relay when the ac line fails completely. A dc line failure will allow the relay to operate through the normally low output impedance of the power supply while the additional parallel load of the relay coil resistance serves to lower the dc voltage from the poorly regulated half-wave power supply. Ultimate heat rise protection for the relay itself can be provided by a thermistor in contact with the body of the relay and offering a shunt path for excess current during periods of all-out ac or dc line failure.

A circuit of this type has application in the field of military designs where the specifications for the equipment itself often call for undervoltage and overvoltage protection with resumption of normal operation when the voltages are restored to their normal values.

Typical values for C and R_1 are shown. The relay resistance will determine the value of the thermistor chosen and it in turn depends on the degree of protection desired. Where only protection against either line failing is required this can be a standard 28 v type.

An Electronic Circuit Protector

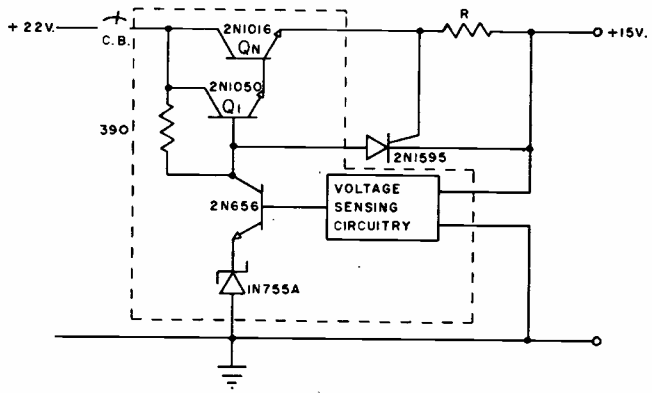
THE PROBLEM often arises of how to protect a transistorized, regulated power supply and the circuitry which it supplies.

It is usually desired that the circuit protecting device must tolerate transient overloads of the same magnitude which under continuous overload conditions it cannot tolerate. At the same time, the device must stop transient overloads above a given value and short circuits.

The circuit protector shown accomplishes these conditions. Within the dotted lines in the circuit is a common voltage regulator, using a series power transistor Q_n, and driver transistor Q_1.

Under heavy load conditions, the base to emitter voltage of Q_n will be about 1.5 volts. Each driver transistor will have about 0.7 volt from base to emitter. If a silicon controlled rectifier is added to the circuit as shown, with the gate and cathode connected across a current sensing resistor and the anode connected to the base of the first driver transistor, it is ready to perform the function of protection against harmfully large transient currents and short circuits.

If the current through the current sensing re-



Transistor protection circuit for regulated power supply.

sistor is large enough to develop the necessary gate potential (about 0.7 volt for a 2N1595), the scr will conduct. During conduction, an scr will have a maximum of about 0.8 volt from anode to cathode, which is not sufficient to allow the driver and series power transistors to remain in conduction and the circuit is protected from the overload. The current sensing resistor is determined by the formula, $R = V_G/I_{trip}$, where V_G is the necessary gate to cathode potential to fire the scr.

The mechanical circuit breaker is used to protect against continuous overloads.

Short-Circuit Protection of Regulated Power Supply

THE CIRCUIT of Fig. 1 provides a practical solution to the problem of protecting series regulator transistors, during short circuit loading.

The series transistors are Q_1 and Q_2. When a short circuit appears across A_1 and A_2, Q_1 and Q_2 are in danger of being destroyed because of the time lag in F_1. Q_{10}, Q_3, Q_1 Q_2 make up the basic unprotected regulator. Q_8 and Q_9 are the protective circuit. E_1 is an unfused, low current, rectified supply that comes on as soon as the primary power is applied to the power supply.

Assume that A_2 has been connected to chassis and R_1 has been adjusted for —17 volts output at A_1. The base of Q_8 is now at —17 volts. The emitter of Q_8 is held at —6 due to the D_{14} regulator diode. Q_8 is in the off condition. The +10 volt power supply, E_1, applies power to the base of Q_9 through R_{17} and R_{16}. Because Q_8 is off the voltage appearing at Q_9 base is +10 volts.

The emitter of Q_9 is in series with a three-volt regulator diode D_{15}. Any tendency for Q_9 to conduct under the preceding conditions is inhibited

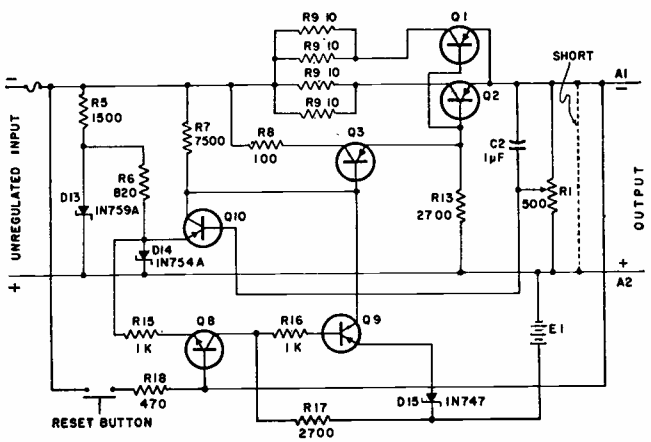


FIG. 1—Transistors Q_8 and Q_9 protect the power supply until the circuit is reset.

by D_{15}. (Making the emitter more negative than the base.) The regulator under these conditions is functioning normally.

If a short circuit (dotted line) occurs between A_1 and A_2 the base voltage of Q_8 goes to zero volts while the emitter remains at —6. Q_8 conducts heavily dropping the voltage at the junction of R_{16} and R_{17} from +10 volts to approximately —3 volts. This causes Q_9 to conduct heavily. The impedance of Q_9 drops to a low value causing its collector to assume a positive voltage of approximately +7 volts. This causes Q_3 to go into a high-impedance condition which prevents power from reaching the bases of Q_1 and Q_2.

Making the bases of Q_1 and Q_2 positive places them in a high-impedance state preventing power from being delivered to the short-circuit load. This condition is self-maintaining and will remain until the reset button is pressed. If the short has been removed, pressing the reset button will place a sufficiently high cut-off voltage on the base of Q_8. The output will build up to —17 and the reset button can be released.

If the reset button is pressed while the short circuit is across the output, all of the cut-off voltage is dropped across R_{18} and Q_8 remains conducting. The regulator cannot be reset until the short is cleared.

Cathode-Ray Tube Grid Protection Circuit

ONE PROBLEM associated with operation of most cathode ray tubes is that of transients when the tube is turned on or off. The effects of transients when the tube is turned on are generally observed as short duration blooms.

In the case of storage tubes of the direct view, high intensity type, blooming caused by transients of turning the tube on are highly undesirable since in many cases its duration is prolonged by the storage action of the tube. Transient blooms are in a long run detrimental to the operation and life of the tube.

Transient problems exist only with those tubes which are operated with a relatively high negative voltage on their cathodes with respect to ground, and where grid coupling capacitors have one side connected to a low voltage level signal source. Most electrostatically deflected tubes are operated with a basic circuit configuration due to the desirability of operating the deflection plates at relatively low B+ voltages. The characteristics of the tube dictate the high negative voltage on the cathode.

The negative source is generally of a moderately high voltage and for discussion will be assumed to be —1700 volts. See Fig. 1. Capacitor C will be assumed to be 0.1 μf and R equal to 500,000 ohms. When the tube is off, capacitor C has no charge and the negative supply voltage is zero.

When the tube is turned on, the negative voltage of —1700 volts appears almost instantly at point A. (Point X is connected to a low voltage level, low impedance, signal source.) The grid of the tube is reluctant to change its voltage level from a value of ground potential. The grid will obtain its proper potential only after coupling capacitor C has had time to charge to the potential Z on the negative bleeder circuit.

There are two paths through which the capacitor may charge. One path is through resistor R and the second is from the cathode through the control grid. Due to the diode action of the control grid and cathode, the impedance of this path is much smaller

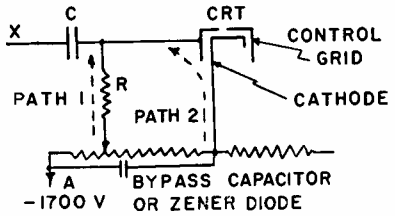


FIG. 1—Charging paths for grid coupling capacitor.

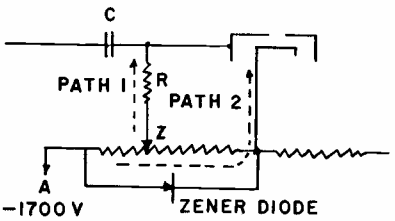


FIG. 2—Transient current paths in a c-r tube.

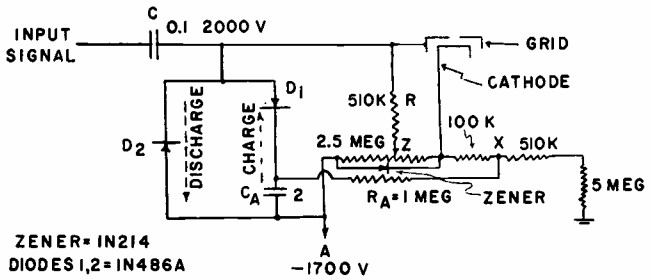


FIG. 3—Circuit designed for protecting grid of c-r tube.

than R and the greatest portion of the current required to charge the capacitor will flow through the grid.

After a fraction of a second, the current through the grid decreases to zero and the capacitor arrives at its final value of potential at Z by charging through resistor R.

The current drawn through the grid-cathode circuit is relatively large and tends to cause a large bundle of electrons to flow toward the tube screen with resultant blooming. Another way of looking at it is that during the capacitor charging period through the grid there is a positive grid to cathode voltage developed.

When the tube is turned off, the large negative voltage across the capacitor tends to hold the grid at its negative value and a large negative grid to cathode voltage momentarily occurs. This causes no blooming effects on the screen of the tube, but is not in its best interests. Grid to cathode voltage breakdown may occur. The only path in this instance for the capacitor to discharge through is resistor R.

When a zener diode is used to stabilize the voltage across the grid bias portion of the negative bleeder as shown in Fig. 2 a large current flows momentarily through the zener to the cathode and grid and may be capable of destroying the unit.

The circuit of Fig. 3 was designed as an answer.

Diode 1, Diode 2, C_A and R_A constitute the added components necessary to completely protect a cathode ray tube from transients.

When the tube is first turned on, capacitor C is charged through diode 1 and C_A. A small voltage due to the transient appears across the capacitor C_A. The voltage across C_A, if the power supply came on instantly, would be $C/C_A + C$ (—1700). This voltage should be lower than the voltage difference between the supply and that normally appearing at point Z during normal operation.

After the transient charging of C has occurred, C_A continues to charge above the grid bias level Z to the value at X through R_A. Resistor R_A charging capacitor C_A to a value of voltage more positive than the grid assures that diode 1 will not clip or limit any incoming video signal. In most cases positive grid to cathode signal operation is avoided, therefore R_A may be tied to the cathode with no interference with incoming video signals resulting. The time constant of R_A and C_A made equal to 1 to 2 seconds should give satisfactory operation for most applications. Diode 2 is ineffective in the circuit in any way during the on transient and will not limit or clip the video signal in a properly designed circuit. The voltage level difference between the supply and point Z must be greater then the most negative pulse expected in order to prevent diode 2 interference. This condition may be readily met in circuit design.

When the tube is turned off, the negative supply rapidly approaches zero. Diode 2 conducts assuring that capacitor C will not maintain a large negative voltage on the tube grid. The grid can never become more negative than the supply voltage since diode 2 will conduct to prevent such an action. The inclusion of diode 2 assures that a large negative voltage will not occur across diode 1 as well as the grid. Neither diode need have a large inverse voltage rating. Resistor R_A rapidly discharges C_A when the tube is turned on.

The circuit has no inherent long time lags to be effective. It is ready to operate again almost immediately after turn off. Small crystal diodes are used, which need not have high inverse voltage ratings. The circuit was found to be effective in preventing blooming and the destruction of reference diodes.

PTC Thermistors Trip 50 Amp Contact at Limiting Temp.

POSITIVE TEMPERATURE COEFFICIENT ptc thermistors provides over-temperature protection when used to actuate the standard magnetc ac circuit breaker shown in Fig. 1. This *ptc* thermistor has a constant resistance of about 60 ohms over a range of temperatures and an abrupt rapidly increasing resistance after a prede-

termined temperature level is reached. The resistance versus temperature curves are shown for a family of *ptcs* in Fig. 2. A *ptc* can carry a continuous current of 70 ma in air without self-heating.

Small inexpensive single pole magnetic circuit breakers with 50 a contacts and toggle type on-off handles

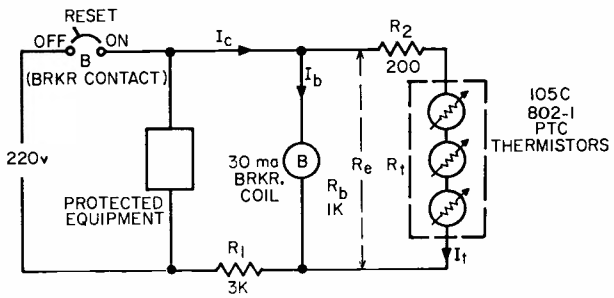


Fig. 1. PTC thermistors used to trip 50 a contact at limiting temperature.

are available with coil ratings as desired from 0.015 to 50 a.

From one to six *ptc* thermistors wired in series and located as temperature protection sensors may be used. Standard fixed resistors are used in a voltage bridge to limit current through the thermistors and the breaker

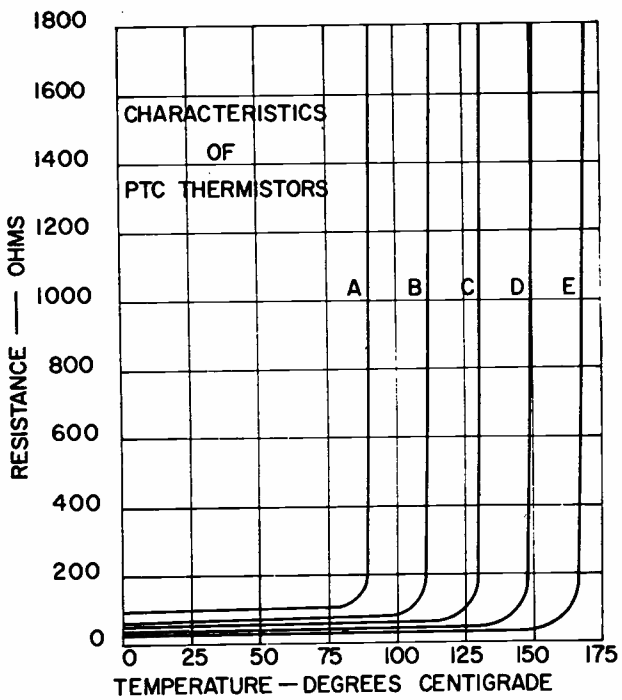


Fig. 2. Family of curves for several PTC thermistors showing resistance versus temperature.

coil. Calculation with components for a 220 v supply are attached. An increase of thermistor resistance to 1220 ohms will trip the breaker. The resistance decreases with temperature reduction and the breaker may be reclosed.

Power to a 3-phase induction motor such as shown in Fig. 3, is furnished by a standard 3-pole contactor whose magnetic coil *M* is actuated by switch S. Circuit breaker *B* is used as the maintained contact switch and turns the control circuit on and off manually. One *ptc* thermistor is embedded in each phase of the winding end turns. With the breaker closed, the motor will normally cycle on and off as controlled by S. In the event of over-temperature in any one or all phases of the winding the breaker will immediately trip, shutting down the motor, and its handle will go to the off

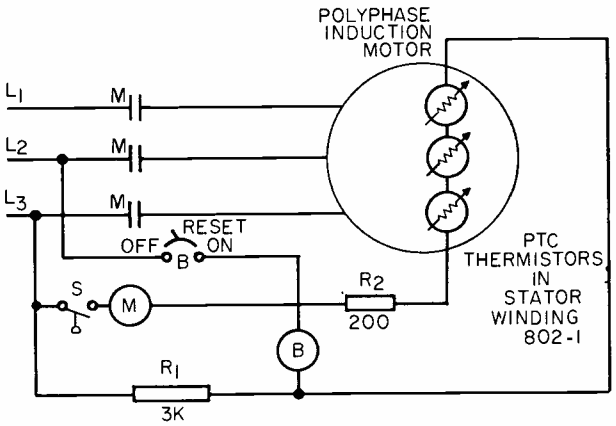


Fig. 3. PTC used with a 3-phase induction motor.

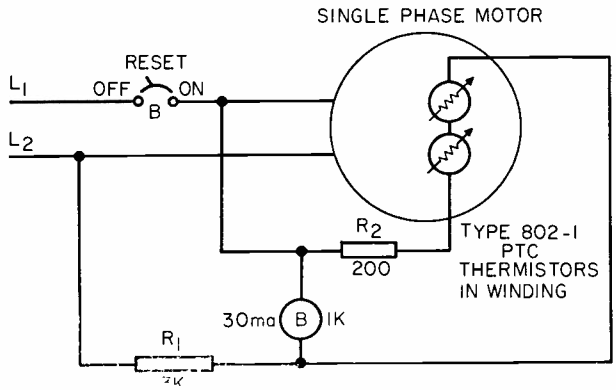


Fig. 4. PTC used with a single-phase motor.

position as an indication. With an 802-1 thermistor, this occurs at 105 to 110 C, a proper limiting temperature for general purpose motor windings. The motor cannot restart until manually reset after cooling.

The breaker is used as a manual control in Fig. 4 for starting and stopping a single-phase motor. One *ptc* thermistor is placed in the main winding to protect for running over-loads and one thermistor is in the starting winding to protect against a faulty acceleration such as centrifugal switch failure. Motor over temperature trips the power. The circuit is satisfactory for ± 10 per cent of the rated voltage.

Calculations:

Thermistors (in equipment) at normal temperatures:

$$R_e = \frac{(R_t + R_2)(R_b)}{R_t + R_2 + R_b} = \frac{(180 + 200)\,1000}{1380}$$

$$= 275 \text{ ohms}$$

or,
$$R_t = \frac{R_b\,(R_e)}{R_b - R_e} - R_e$$

$$V_b = \frac{R_e}{(R_1 + R_e)}(220) = \frac{(275)(220)}{3000 + 275}$$

$$= 18.5 \text{ volts}$$

And,
$$R_e = \frac{V_b R_1}{220 - V_b}$$

$$I_b = \frac{18.5}{1000} = 18.5 \text{ ma};$$

$$I_t = \frac{18.5}{380} = 48.7 \text{ ma};$$

$$I_c = \frac{220}{3275} = 67.2 \text{ ma}$$

Thermistors in equipment at trip temperature (V_b = 36 v)

$$R_c = \frac{V_b R_1}{220 - V_b} = \frac{(36)(3000)}{220 - 36} = 587 \text{ ohms}$$

$$R_t = \frac{R_b R_c}{R_b - R_c} - R_2 = \frac{(1000)(587)}{1000 - 587} - 200$$

$$= 1220 \text{ ohms}$$

For R_1 use a 15 watt resistor.
For R_2 use a 2 watt resistor.

A Novel Magnetron Protection Circuit

THE CIRCUIT of Fig. 1 uses avalanche diodes in a protection circuit for sparking magnetrons. An audio oscillator feeds an auto-transformer which is used to step up the audio voltage to the point where the negative swing of the audio sine wave fires avalanche diode D_1. The characteristic curve of this diode is shown in Fig. 2. The 0.03 μf capacitor then discharges through the avalanche diode and the transformer, rapidly reversing the flux direction in the winding. This flux reversal generates a voltage pulse across the winding which is coupled out through the 0.002 μf capacitor to fire the 4C35A hydrogen thyratron in a line-type modulator feeding a magnetron. After the discharge the avalanche diode recovers because it cannot draw enough sustaining current through R_1. The 0.03 μf capacitor then is free to recharge from the 4 μf capacitor. This portion of the circuit forms the drive pulse generator driven by the audio oscillator.

To obtain protection, either the magnetron pulse current or the inverse diode current can be monitored if the modulator is a line type with usual

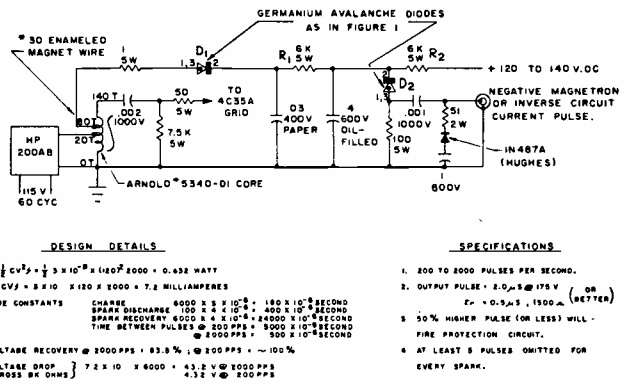


FIG. 1—Trigger circuit for modulator with spark protection and automatic threshhold adjustment.

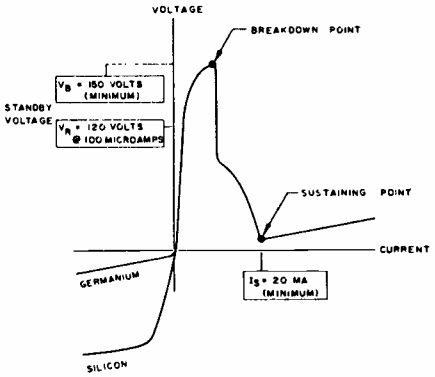


FIG. 2—Avalanche diode characteristic curve.

circuitry. When the monitored pulse is of negative polarity the configuration used on the right hand side of Fig. 1 works quite well. The 51 ohm resistor in series with the 1N487A diode and the 1-μf capacitor is a diode peak voltmeter which relies on the small back conductance of the 1N487A and the low source resistance for slow discharge when the current pulse amplitude is reduced. The 1-μf capacitor charges up to the peak value of the monitored pulse train. From then on little current passes through the 51 ohm resistor until an oversize pulse (caused by a magnetron spark, for instance) comes along. If this oversize pulse is of sufficient amplitude (as it will be with a spark) the voltage spike developed across the 51 ohm resistor will fire the avalanche diode through the 0.001 μf coupling capacitor. The 4 μf power supply capacitor now discharges through avalanche diode D_2 and the 100-ohm resistor. Since resistor R_2 will not maintain sustaining current through the diode, this diode recovers and the 4-μf capacitor recharges. During the time that the 4-μf capacitor is not charged to its normal voltage the drive pulse generator is inoperative.

The net result is that several pulses are omitted every time the magnetron sparks. If the magnetron should spark on every pulse, the effect is a reduction in repetition rate which greatly reduces the average power flow into the magnetron and limits damage.

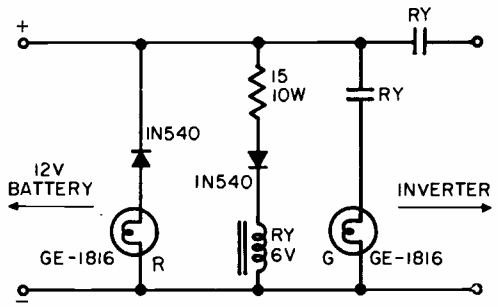
Inverter Control

CONNECTING the wrong battery polarity to an inverter can destroy its power transistors. This circuit provides built-in protection to transistorized inverters operating from a 12 v battery and providing 115 v, 60 cps output.

The relay is energized through the 15 ohm resistor and series diode when the positive and negative terminals of the inverter are respectively connected to the positive and negative sides of the battery. This action closes both contacts, lights a green bulb, and places the inverter in service. If incorrectly connected to the battery the relay fails to operate. Under this latter condition a red bulb lights implying error.

The complete circuit shown consists of two general purpose diodes, one 6 v dc relay, one resistor and two

GE-1816 pilot lamps. For just a few dollars this circuit provides protection for equipment worth much more.



Control protects transistorized inverters from being incorrectly polarized.

Low-Voltage Cutoff Circuit

THE CIRCUIT PRESENTED HERE is designed to prevent failure in a satellite's electronic system due to low battery voltage. This design was developed for the Army Signal Corps' Courier Communications Satellite. Its function is to return the satellite from an active to a standby condition if the battery voltage falls below a pre-determined level.

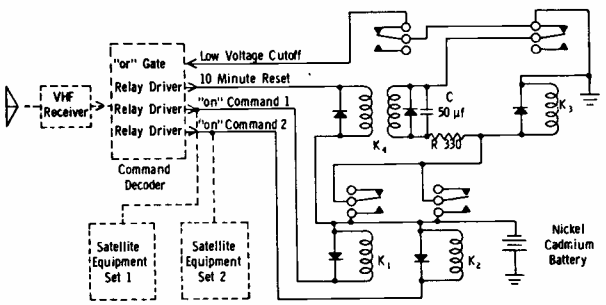


FIG. 1—Low-voltage de-energizer.

Fig. 1 shows the low-voltage cutoff circuit as it is used in the Courier system. Relays K_1 and K_2 are Potter Brumfield SC11's; K_4 is a Potter Brumfield SL11 and K_3 is the relay portion of a line-voltage sensor (Model 9760) made by Tempo Instrument, Inc. The sensor is designed to energize or de-energize the relay when the voltage across the coil is 24 volts ± 1 percent.

The cutoff circuit works in the following manner. When the satellite equipment is turned on by a signal from the ground station, either relay K_1 or K_2 (depending upon which command is given) is also energized by a relay driver in the command decoder. Operation of either relay in turn causes a voltage to be applied across the coils of K_3 and K_4; however, the RC time delay across K_4 results in K_3 being energized first, which removes the voltage from K_4 thereby preventing it from being energized. The circuit remains in this condition for normal active operation of the satellite.

If the battery, which has a nominal working voltage of 27 v, becomes discharged down to 24 v, K_3 is automatically de-energized and this action applies a voltage across the coil of K_4. Operation of K_4 removes the ground from an OR gate in the command decoder which in turn de-energizes power-control relays in the remaining satellite equipment, including K_1 or K_2. Thus, the satellite is returned to standby condition, allowing the batteries to be recharged by the solar cells.

Relay K_4 is of the latching type and remains energized until it receives a signal from the command decoder, which is automatically generated every ten minutes. After this relay is reset and the batteries are recharged, the satellite is again ready to receive a command from the ground station to activate the system.

Overload Protection

THIS CIRCUIT gives fast, automatic protection with an adjustable trip level. The sample circuit shows it as it would be applied to a lab power supply.

Other fast automatic-protection devices usually have one or more of the following faults: not adjustable, poor regulation as load current approaches overload limit, load-limit setting varies with transistor changes, complexity, and output voltage might not go to zero when tripped. This circuit avoids these faults. It is quite simple, has a wide-range adjustment of the trip current, is insensitive to changes of transistor characteristics, and the adjustable trip level can be set close to the operating current level.

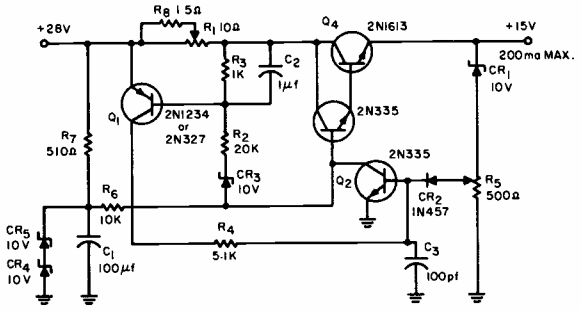
The automatic overload-protection circuit is shown incorporated into a conventional regulator. The protection circuit consists of resistors R_1, R_2, R_3, and R_4; capacitor, C_2; diodes CR_3 and CR_2, and transistor Q_1, operating in conjunction with the existing regulator circuitry.

In normal operation (load current less than the trip level) R_2, R_3, and CR_3 are selected so that the drop across R_3 is much less than 0.6 volts (silicon transistors assumed).

$$R_3(V_S - V_L - V_{CR3} - 1.2)/R_2 + R_3 << 0.6 \text{ v}$$

where V_S is the source voltage, V_L is the output voltage, V_{CR3} is the zener voltage of CR_3, 1.2 v is the base-to-emitter drop of Q_3 and Q_4 in series and 0.6 v is the base-to-emitter drop of Q_1.

Therefore Q_1 is cut off and the regulator operates as though the protection were not present.



Overload cut-out current level is adjustable with R_1.

When the load current reaches the preset trip level, the drop across R_1 becomes great enough to turn on Q_1. The trip-current is given by:

$$R_1 I_L > I_{b2} R_3/\beta_1 + 0.6$$

where β_1 is beta for Q_1, R_1 is adjustable to set desired I_L, I_L is the load current at trip level, and I_{b2} is the base

current to saturate Q_2. When Q_1 turns on, it saturates Q_2, dropping Q_2's collector voltage to approximately zero. The current through R_3 increases. A second condition on R_2, R_3, and CR_3 is that under these conditions the drop across R_3 is sufficient to turn on Q_1, which will saturate Q_2.

$$\frac{\beta_1}{R_3}\left[\frac{R_3(V_B - V_{CR3})}{R_2 + R_3}\right] - 0.6 > \text{Base current to saturate } Q_2$$

This holds Q_2 in saturation which cuts off the regulator string Q_3 and Q_4, thereby protecting these transistors and reducing the output voltage to zero.

The turn-off switching is regenerative and fast. To reset the regulator the supply voltage is switched off and then back on.

Capacitor C_2 prevents turn-on transients from triggering the protection circuit. Diode CR_2 blocks the switching current from R_5. Resistor R_4 limits the base current to Q_2. ◆◆

Lifesaver Circuit

It is often desirable in line-operated, power-transformerless equipment to connect the chassis to the grounded side of the power line. While use of polarized receptacles affords a degree of protection, wiring reversals are common and the chassis may be placed at full line potential with respect to ground. In addition, use of polarized receptacles does not protect against an inadvertent "floating" neutral. Elaborate protective measures are then required to prevent personnel from coming in contact with the chassis.

The device described here uses the Underwriters Laboratories parallel blade connector with ground lug in conjunction with special circuitry to minimize the possibility of the chassis being "alive." The 115 v relays must find the proper relationship of voltage between the "hot," neutral, and ground terminals in order for power to be applied to the equipment. A fuse is used to provide the usual circuit protection.

The circuit can be housed in a small metal box on the connector end of the three conductor power cord. The black terminal of the line is normally routed to the fuse or circuit breaker of the branch circuit while the white is connected to the system neutral which is in turn grounded. The ground lug of the receptacle is connected to the grounded conduit system or, if nonmetallic sheathed cable is used, to a separate lead which is returned to the building ground.

When power is applied to the circuit, an undesired potential between the neutral and ground terminals causes fast acting relay K_1 to be energized thus opening the normally closed contacts. This prevents operation of K_2 so that power is not delivered to the load. If the desired connection exists, K_1 will not operate; thus K_2 will be connected between the "hot" and ground terminals of the connector and will supply power to the load. Contacts on K_2 are adjusted so that the ground contacts close first and release last.

The only limitation of this circuit is that it does not protect against the condition where both the neutral terminal and the conduit ground system are at line potential with respect to earth ground. Such a fault is rare and unlikely to occur.

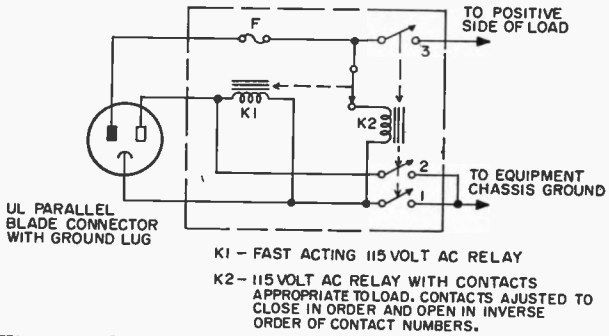


Fig. 1—Lifesaver circuit.

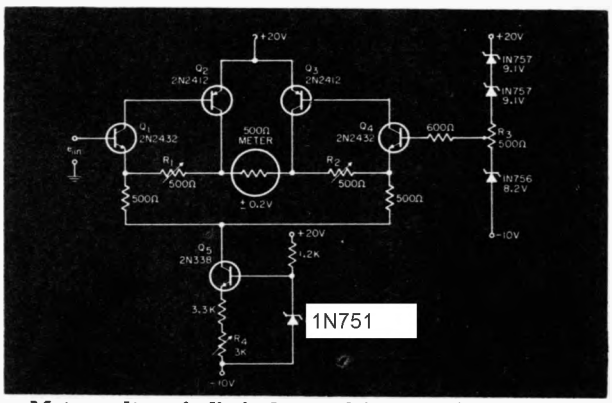
High Input Impedance Meter-Protection Circuit

It often is necessary to provide overload protection and an effective increase in impedance for a meter movement while at the same time preserving the linearity of the meter. The circuit shown meets these requirements with a linear response from −0.2 to +0.2 volts across a 500-ohm meter and limits the meter voltage to these maximum values for input swings up to ±15 volts. Two complementary amplifiers are used differentially to allow bi-polar inputs.

High input overloads (±15 volts) are possible because of the high BV_{EBO} of Q_1, which protects the circuit, and also because of constant-current source Q_5, which provides protection to the meter. The current level in Q_5 (and thus the clipping level) is set by R_4.

With the input shorted, Q_5 supplies equal current to Q_1 and Q_4 and to Q_2 and Q_3. While the input is increasing in a positive direction, Q_1 and Q_2 are turning on and Q_3 and Q_4 are turning off. When e_{in} becomes greater than +0.2 volts, Q_5 is supplying all of its current to Q_1 and Q_2 while Q_3 and Q_4 are turned off. As the input voltage is further increased to +15 volts, the collector voltage of Q_5 increases at the same rate. This keeps a constant voltage across the emitter resistors of Q_1, thus limiting the current through the meter. R_3 sets the dc level at 0 volts across the meter with the input shorted.

One method of setting the clipping level is to supply a low-frequency sine wave at the input and observe on a



Meter voltage is limited to ±0.2 v and is linear in its active region.

scope the voltage across a 500-ohm load while adjusting R_1 and R_2 until the clipping level is greater than ±0.2 volts. Input impedance is greater than 1 meg for all input voltage.

Although the circuit was designed for a 500-ohm meter, minor circuit modifications will adapt it to other meters. Silicon planar transistors can be used for low leakage at high temperatures. ◆◆

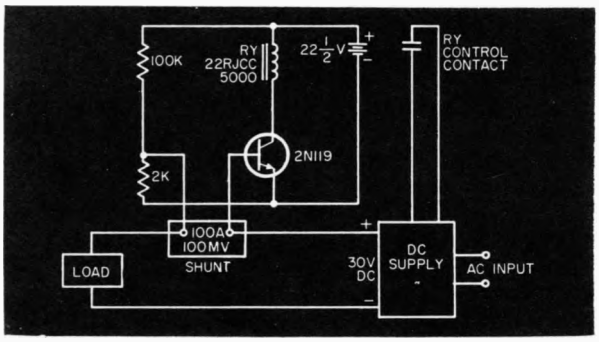
Single-Transistor Short-Circuit Detector

THE CURRENT-AMPLIFICATION FEATURE of a transistor lends itself nicely to the protection of dc power circuits. Most dc power sources have millivolt shunts which are used in metering. This shunt (or an equivalent length of wire) can be used to drive the base of the transistor to indicate overloads.

Almost all dc supplies can develop up to ten times normal load current on a bolted short circuit. This usually is far too much current.

In the circuit shown, a 400-mv signal (4 times overload) at the base shunt causes a base current of 0.060 ma and a collector current of 2.3 ma at room temperature. The relay will operate when 2 ma flows in the collector. This gives a transistor beta of 38.3 (2.3/0.06 = 38.3).

Therefore the circuit will disconnect the dc power when



Single-transistor short-circuit detector.

four times normal current is reached. The operating point should be designed to override normal load and switching surges and still be below maximum short circuit current. Four or five times normal seems reasonable. ◆◆

Inexpensive Short-Proof Voltage Regulator

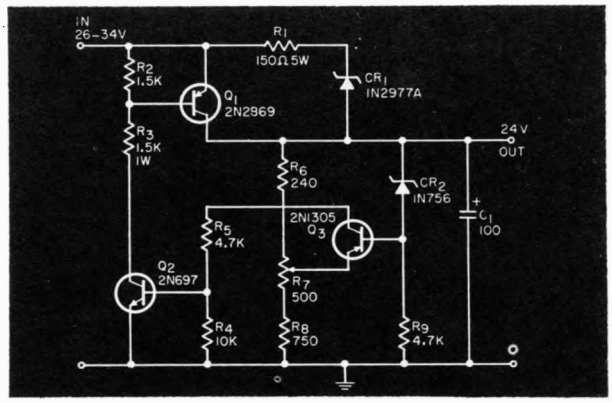
DESIGNED TO PROVIDE a constant 24 v at currents up to 500 ma, this voltage regulator turns itself off when its load is short-circuited. Restarting is automatic when the short is removed. Regulation is within 1 percent for currents from no load to 500 ma and with input voltages from 26 to 34 v.

As the load current increases, all three transistors conduct more heavily until, at a collector current of about 20 ma, Q_2 becomes saturated, and the base current of Q_1 is thereby limited. The maximum output current in milliamps is approximately 20 times the beta of Q_1. If the load resistance is sufficiently low, the output voltage will become too small to maintain conduction in Q_3, thus turning the regulator off. The short-circuit output current is about 100 ma, supplied through R_1 and CR_1. Under normal operation no current flows through R_1 or CR_1 except during starting, unless the input voltage exceeds about 37 v.

If manual starting is desired, R_1 and CR_1 may be replaced with a 3900-ohm resistor. The short-circuit in this case will be only about 10 ma. Starting is accomplished by a switch which momentarily disconnects the load from the regulator.

Q_1 and CR_1 may be mounted on the same small heat sink. A 3-inch square piece of aluminum is sufficient, since it is only necessary to dissipate about 2 w.

Total parts cost is less than $16.00 for the automatically



Inexpensive short-proof voltage regulator.

started regulator, and less than $10.00 for the manually started version. ◆◆

Reduced-Power Overload Protection

THIS CIRCUIT features a minimum number of components to accomplish overload protection of a series-regulated power supply. The output current decreases as the load resistance decreases above the set value.

The circuit was developed to reduce power dissipation of the series transistors under overload or short circuit conditions. Most power supply protection circuits under overload conditions go into a constant-current regulating mode, requiring high power dissipating capabilities under short circuit conditions.

A typical power-supply schematic is shown in Fig. 1 with the overload protection circuitry enclosed by dashed lines. Zener diode, CR_1, resistors R_1 and R_2 and transistor Q_3

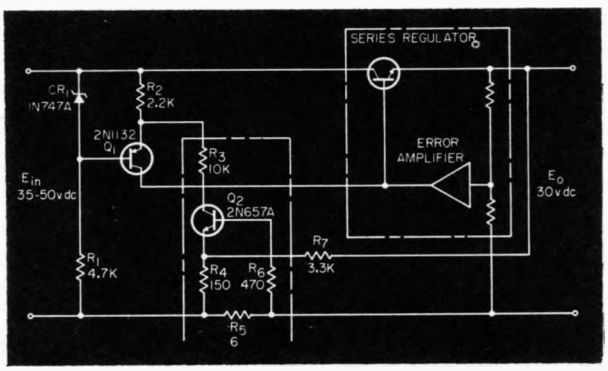


Fig. 1. Low-power overload protection circuit.

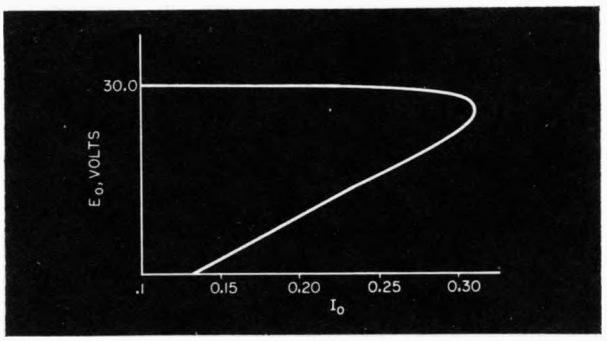


Fig. 2. Output characteristic.

provide a constant-current source to the series regulator.

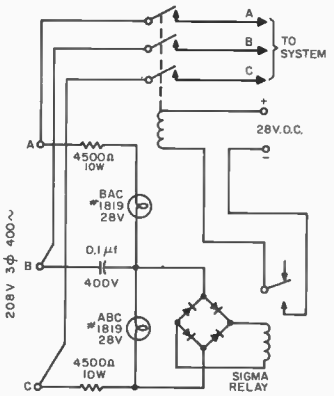
Transistor Q_2 and resistors R_3 — R_7 comprise the overload-protection circuitry. Typical values are shown for a 30-vdc, 0.25-amp supply with current limiting to start at 0.31 amp.

The curve in Fig. 2 indicates the negative resistance effect due to the positive feedback through R_7. As the load current increases, the voltage across R_5 increases until Q_2 is biased into conduction.

The emitter voltage of Q_1 then increases until Q_1 is cut off which causes the output voltage to start decreasing. The voltage feedback from R_7 then causes the emitter voltage of Q_2 to decrease and Q_2 further conducts, causing Q_1 to cut off completely.

A direct short across the output actually causes the output current to drop to less than half nominal current.

The important feature is that under short circuit conditions power dissipation is actually decreased in the series regulation transistors.



The proper phase rotation is indicated by lamp ABC, which is paralleled with a full-wave bridge and relay circuit to connect the source to the system.

Simple Reverse-Phase Protection

NAVIGATION SYSTEMS can be seriously damaged if the phase rotation is reversed by careless or accidental power transfers. This circuit protects the system and determines phase rotation on initial startup or installation.

A full-wave bridge and sensitive relay are added to the existing phase rotation indicator as shown.

If proper rotation is connected, the ABC lamp will light and the Sigma relay will close the control circuit and allow operation. With reverse phase rotation, lamp BAC will light up and the relay will fail to close the control circuit and prevent operation.

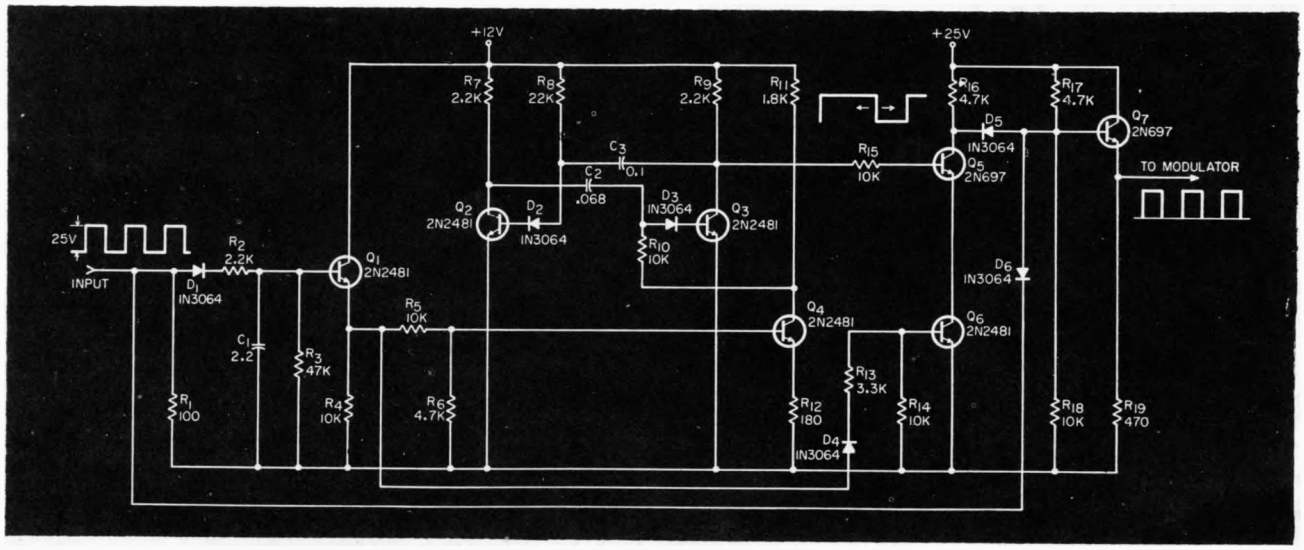
The principal components added are a 22RJCC Sigma relay with a 2500 ohm coil, four general purpose diodes and a conventional 28 vdc three-pole relay.

Duty-Cycle Limiter

IT IS SOMETIMES NECESSARY to limit the duty cycle of pulse modulated transmitters below a certain level. The circuit shown passes a modulation signal without limiting until a duty cycle of 1 percent is reached. Thereafter countdown begins and the duty cycle is held at approximately 1 percent but never exceeds it.

Components C_1 and R_2 integrate the pulsed signal and establish an average dc level proportional to duty cycle. This dc level is coupled through emitter follower Q_1 to a voltage-controlled astable multivibrator consisting of Q_2, Q_3, and Q_4 and associated components. This multivibrator, which runs unsynchronized with the PRF of the input signal, has its duty cycle controlled by the base voltage of Q_4. Its output is direct coupled to a tandem AND gate Q_5 and Q_6.

A continuous output from diode AND gate D_5 and D_6 is obtained when Q_5 and Q_6 are cut off and a signal is applied to D_6. Divider network R_{13} and R_{14} allows tandem gate Q_5 and Q_6 to be switched on after a 1-percent duty cycle has been reached. The signal is then counted down at a rate determined by the duty cycle of the astable multivibrator. Q_7 is an emitter follower used as a modulator driver.

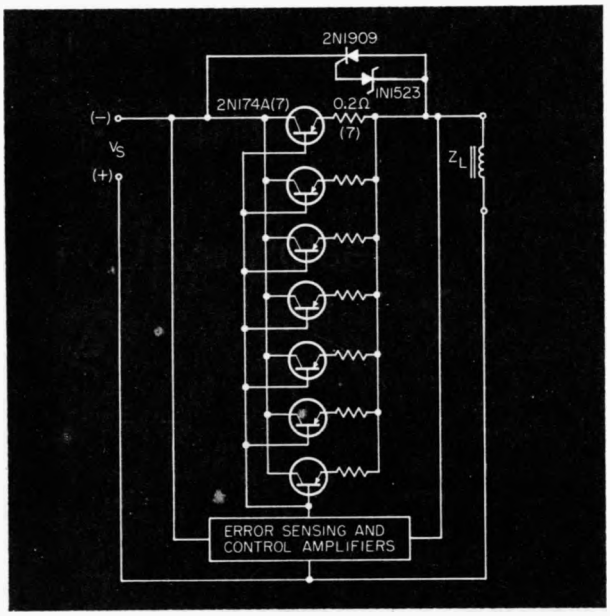


Zener-Gated SCR Protection for Power Transistors

HERE IS A RELATIVELY inexpensive and reliable way to protect power transistors from excessive dissipation due to over-voltage. In the original application, seven 2N174As were paralleled to serve as the pass stage of a constant-current dc power supply. Current regulation was required under doubly adverse conditions of changing source voltage and changing load values.

The equipment was designed for operation by relatively inexperienced personnel, and the SCR protective circuitry was included to prevent transistor damage by remote-control selection of 20-A load current with the source voltage set at the 40-V level. If this occurred, the product of the collector-to-emitter voltage and the collector current would exceed the transistor dissipation rating and transistor burn-out would occur in a very short time, even though properly heat-sinked.

A 2N1909 SCR was used as a controllable "short circuit" across the 2N174As. Since the current-regulator control amplifier requires about a 5-Vdc compliance voltage across the 2N174As, the SCR gate was referenced to a 10-V zener



SCR protection for seven paralleled power transistors.

diode (1N1523), so that if the collector-to-emitter voltage of the 2N174As equalled or exceeded the zener voltage, the SCR gate was permitted to draw triggering current through the zener diode.

The 2N1909 has a turn-on time of a few microseconds when gated by a steep wavefront, or step function, which is much faster than needed to protect against junction overheating in power transistors.

The virtual shorting effect of emitter to collector by SCR conduction is permissible in this application. The desired result is effected by the regulator losing control. The 2N174As are turned off, and load current flows through the SCR. Turn-off of the SCR is accomplished by reducing the source voltage to the SCR extinguish level. Upon increasing source voltage, the current regulator once again assumes control.

The zener-controlled gate has a further excellent characteristic in that a "soft-drive killer*" design deficiency does not exist. The SCR turn-on time is defined by the sum of the zener diode turn-on time and the turn-on characteristic of the SCR in use. Typical turn-on time for the 2N1909 is about 2 μsec. The zener blocking-switching action, then, serves to prevent a constant flow of SCR gate current at levels below the SCR triggering level. Zener diode leakage current flows in the gate lead, but this amount of current is far less than a damaging amount.

Zener Stabilizes Phase-Shift Oscillator

A LOW-VOLTAGE ZENER DIODE has a rounded knee characteristic that makes it an excellent current-variable resistor for AGC purposes, since it permits operation with larger signal levels than possible with ordinary diodes. Typical

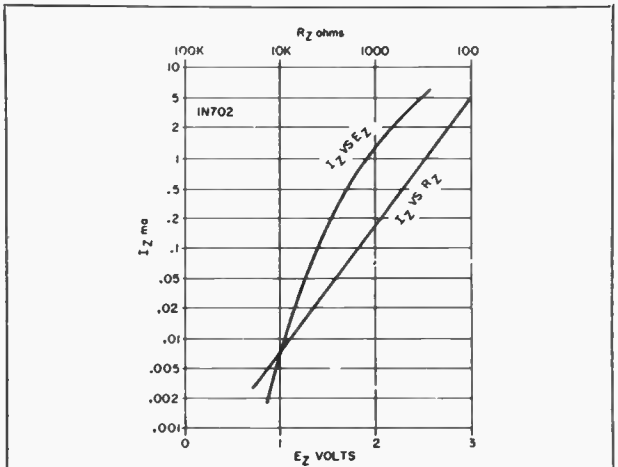


Fig. 1. Characteristics for 1N702.

characteristics of the 1N702 are shown in Fig. 1, while Fig. 2 shows a phase-shift oscillator (Q_1) in which the gain is controlled by coupling a 1N702 zener diode, CR_1, across the emitter resistor. (C_5, C_6, R_7 is a non-polar capacitor combination.)

The phase-shift oscillator consists of the oscillator proper, Q_1, the AGC amplifier Q_2, and a complementary emitter follower Q_4, Q_5, with a driver stage Q_3.

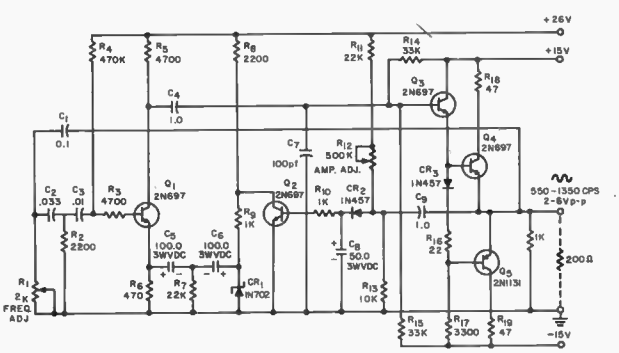


Fig. 2. Stabilized phase-shift oscillator.

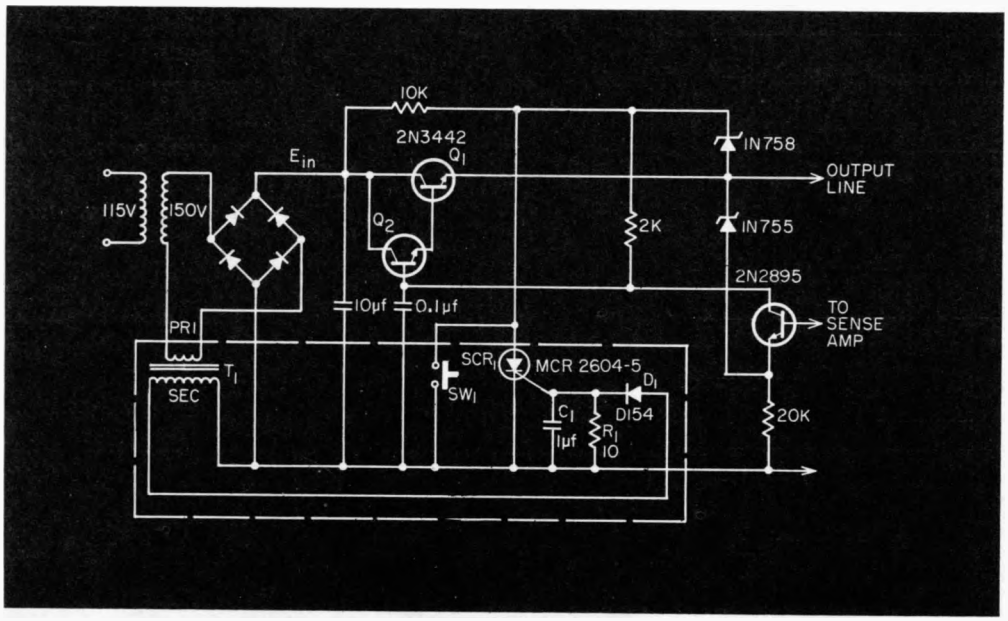
The input capacitor to the phase-shift network is connected to the circuit output rather than the collector of Q_1. In this way, the feedback overcomes the zero crossover distortion of the complementary emitter follower. At the collector of Q_1 there is a compensatory fast rise and fall at these points. CR_3 and R_{16} minimize crossover effects. Phase-shift resistor R_3 is connected to the base of Q_1 instead of to ground. All the signal current therefore flows into the transistor, and the relatively small input impedance is in series with R_3 instead of shunting it.

Diode CR_2 detects the output amplitude, and the resulting current, plus the bias current through R_{12}, is amplified by Q_2, which upon excessive input current reduces current through CR_1 by reducing the potential at the tie-point of R_8 and R_9. The dynamic impedance goes up, decreasing the gain of Q_1, and output amplitude is lowered. Output dc level is such as to keep Q_5 conducting, thereby maintaining a self-starting capability.

Current Transformer Gives Fast Overload Protection

IN HIGH-VOLTAGE transistorized power supplies, current limiting as a means of short-circuit protection is often inadequate. Large values of current and voltage will quickly exceed the control transistor's power rating. If a current transformer is used to sample overloads, a fast and effective short-circuit protection can be obtained that will reduce the power expended in the control transistor during overloads to a negligible level.

The current transformer T_1 samples the current supplied to the voltage regulator. Diode D_1 rectifies the sampled current and a voltage drop is produced across resistor R_1. R_1 is selected to trigger the silicon-controlled rectifier SRC_1, when a predetermined value of overload current is reached. Capacitor C_1 serves as a filter for the rectified signal.



Fast reacting overload protection circuit uses current transformer to sense current to voltage regulator.

When a current overload occurs, additional voltage is generated across R_1 which triggers SCR_1 on. With SCR_1 on, no base current is available to the control transistors Q_1 and Q_2, and these transistors are turned off. With Q_1 off, the transistor is required to sustain only the unregulated voltage E_{in}, thereby reducing its expended power to a negligible amount.

The circuit can be reset by removing the input voltage or by providing a manual reset switch SW_1 to eliminate the holding current of the SCR.

The current transformer used in the circuit shown was wound on an EI-187 core with an 8-turn primary and a 120-turn secondary.

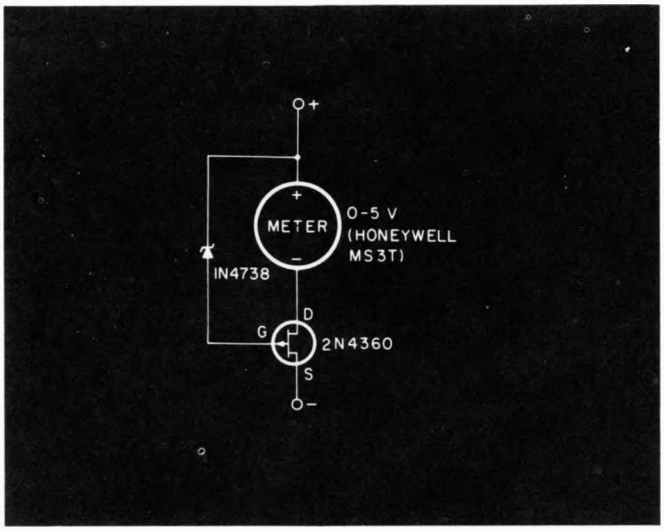
FET provides automatic meter protection

MOST METER-PROTECTION circuits use some sort of nonlinear device to shunt the meter and thus divert high currents. Though these circuits do protect the meter, many of them have the disadvantage that they also load down the external circuitry, causing errors. Errors can be minimized by using a series resistor and by recalibrating the meter together with its protection circuit. But, of course, this increases the cost.

Other protection circuits employ fuses or circuit breakers, but these are often slow and must be manually replaced or reset after each overload.

The circuit shown here has none of the drawbacks mentioned, yet it requires only two inexpensive components. It was developed for an application where the usual voltages of interest were in the range 2 to 3 volts, but where accidental overload voltages up to 14 volts could occasionally occur. With the components shown,, there is no noticeable effect or meter accuracy with voltages to full scale. Yet with 16 volts applied, only 6.7 volts appear across the meter.

Maximum allowable voltage depends on the breakdown voltage of the FET. Circuit action is such that, below the onset of conduction in the zener diode, only the FET "on" resistance is in series with the



meter. This resistance is negligible compared to the meter resistance. When the zener diode conducts, it applies gate voltage to the FET, cutting it off and preventing excessive meter current.

This simple and effective meter-protection circuit uses only two inexpensive components.

Solid-state relay/circuit breaker

THE CIRCUIT in Fig. 1 provides on-off power control with fault and overload protection. It eliminates the need for a mechanical circuit breaker (which is too slow to protect semiconductors) or fuse (which cannot be reset).

Power is supplied to the load when a logical "1" (5.0 Vdc) is applied to terminal *1*. With transister Q_3 biased on, capacitor C_1 starts charging toward the value of the supply voltage through resistor R_2 and transistor Q_2. Up to rated load, the potential at point *A* is greater than the reference voltage established by zener RD_1, and transistor Q_3 is biased on. This shunts C_1 and holds Q_2 and Q_1 on.

In the event of an overload or fault, the potential at *A* falls below the established reference voltage, whereupon RD_1 becomes non-conductive and a trip cycle is initiated. Transistor Q_3 is turned off causing C_1 to start charging toward the supply voltage. The time constant established by R_2 and C_1 prevents tripping by transient overloads such as caused by incandescent lamps. However, if the overload or fault continues beyond the duration of the time delay, the charged capacitor halts current flow and causes Q_2 and Q_1 to turn off.

To reset the circuit, a logical "1" applied to terminal *2* turns Q_2 on, thereby discharging C_1. If the overload persists, the trip cycle is repeated.

Capacitor C_2 prevents maintaining the circuit closed on an overload or fault with a continuous reset signal. The time constant of C_2 and R_9 allows capacitor C_1 to discharge fully. Diodes D_1 and D_2 isolate the power circuit from the reset circuit.

The allowable range of load current for the circuit shown in Fig. 1 is 0 to 5.0 A. The circuit will limit current to a shorted output to approximately 7.0 A. Overload trip point can be adjusted up or down by raising or lowering the reference voltage at point *A*. This is done by selecting the proper zener voltage for RD_1. Load-current rating of the circuit is controlled by R_2.

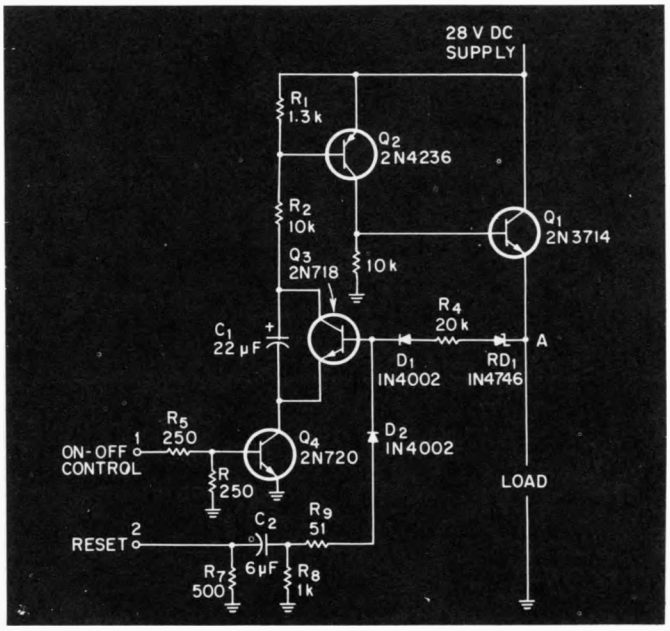


Fig. 1. This solid-state relay provides on-off power control with fault and overload protection. It obviates circuit breakers and fuses.

Overvoltage-protection circuit for IC power supplies

MANY CIRCUIT designers use series voltage regulators to power linear ICs, because, with many types of ICs, gain depends on supply voltage. To maximize the open-loop gain of IC op amps, supply voltage should be as high as possible. But there is then a danger of damaging the ICs if the series-regulator fails or becomes shorted. Over-voltage protection is therefore essential.

Figure 1 shows how a simple protection circuit can be added to an otherwise conventional series regulator. The added components are Q_1, Q_2 and R_1. If Q_3 becomes shorted, the protection circuit reduces the output current to a very low value.

The circuit is designed such that, with normal load currents, I_{E1} is sufficient to hold Q_2 in saturation. Resistor R_1 is chosen to maintain a suitable(V_{CE3} - V_{BE1}) with the predetermined value of I_{E1}. Transistor Q_1's collector current I_{C1} provides base drive for Q_2.

If Q_3 saturates or becomes shorted, V_{BE1} approaches zero and I_{C1} decreases due to back biasing of Q_1's base-emitter junction. With a reduced value of I_{C1}, V_{CE2} increases, thus causing the output voltage to fall.

Negative supplies can, of course, be protected by a similar technique. Transistor Q_1 should then be NPN and Q_2 should be PNP. Fig. 2 shows a dual supply that provides ±15 volts for IC op amps.

In general, switching-type transistors should be used for this circuit to provide fast response. Transistor Q_2 should be chosen to have suitable $V_{CE\ SAT}$ and V_{CEO}. For Q_1, V_{CB} should be greater than the sum of V_{CE3} and E_o.

Interaction of the protection circuit with the regulator circuit is not serious. Current I_{E1} depends on the unregulated input voltage but, provided the regulator has sufficient gain to correct for variations in the impedance of Q_2, input variations have little effect on output voltage.

Of course, if the total load current is less than I_{E1} the regulator won't work. Therefore, the output divider network should draw all of I_{E1} plus whatever minimum current is needed by the regulator.

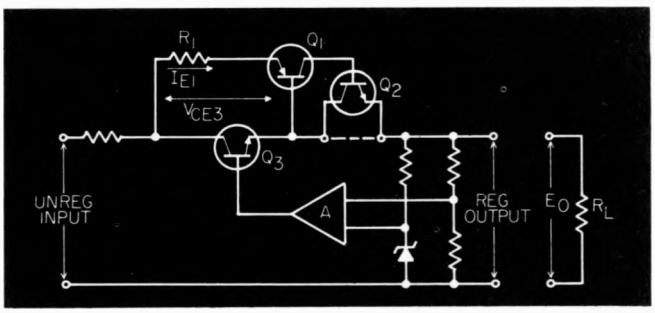


Fig. 1. Simple overvoltage-protection circuit (R_1, Q_1, Q_2) can be added to any conventional series regulator.

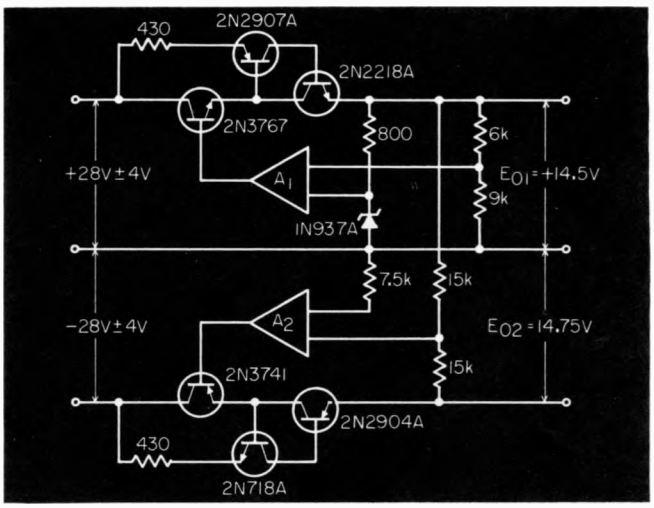


Fig. 2. Complete dual 15-volt power supply for IC op amps has protection circuits in each line.

Adjustable-overvoltage circuit breaker

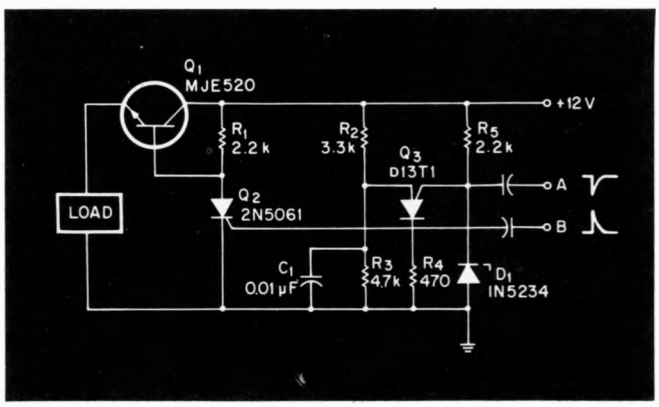
THIS CIRCUIT serves as an overvoltage protector and, at the same time, generates trigger pulses for an alarm or other functions.

The pass transistor, Q_1, is normally on; it is turned off when SCR Q_2 fires. Zener D_1 keeps the gate of the programmable unijunction Q_3 at a constant voltage. Q_3's anode voltage is kept below the zener voltage. Where the supply voltage rises and Q_3's anode voltage exceeds the gate voltage, Q_3 fires, turning on Q_2, which cuts off Q_1 and the load.

By selecting a suitable R_2/R_3 ratio, one can set Q_3's anode voltage and thus, the voltage at which the circuit will trip. When Q_3 fires, it generates complementary pulses A and B which can be used to trigger other circuitry.

After the circuit trips it stays off until the supply voltage is shut off, at which time Q_2 commutates and resets the circuit.

In many cases, it may be desirable to actuate a relay or lamp without controlling a load. In these applications, one can eliminate Q_1 and the load, substitute a relay or lamp for R_1 and use more than one circuit to trip at different levels. ■



The R2/R3 ratio determines the trip point of this overvoltage protector.

Modified 710 maintains accuracy at high input voltages

IT IS OFTEN NECESSARY to protect the inputs of comparators (μA710) against excessive voltage inputs. A typical application would be a zero-crossing detector placed at the output of an op amp with amplifier output swinging ±10 volts. The usual over-voltage protection circuit resembles the circuitry of Fig. 1. In this circuit, R_S is made relatively high to limit the drive current required of amplifier A_1. This resistor reduces the accuracy of comparison by $I_{off}\ R_s$ where I_{off} is the offset current of the 710.

The circuit of Fig. 2 overcomes this problem. When V_{in} is more positive than V_{p1} (Pinch-off voltage of Q_1), Q_1 is off and Q_2 is on since CR_2 is back biased. Thus the gate of Q_2 is allowed to float and assumes the same potential as the source with the result that Q_2 is on. When V_{in} is more negative than V_{p2}, Q_2 is off and Q_1 is on. In either case, the impedance seen by V_{in} is approximately $R_a + R_b$ and the input voltage of the comparator is $(V_{in})\ (R_b)/(r_a + r_b)$. The voltage and the pinch-off voltages should be chosen to be less than the input and differential voltage ratings of the comparator (5 volts for the μA710).

Only when the difference between V_1 and ground is less than the pinch-off voltages, do both FETs conduct resulting in a low impedance path to the 710's input. Maximum conductance (Gds in Fig. 3) is obtained only near the comparison point where $V_{GS} = V_1 - \text{ground} = 0$. ■

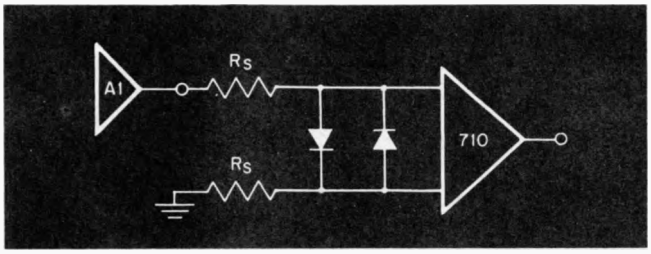


Fig. 1. Usual comparator protection circuit which introduces an error of $I_{off}\ R_s$.

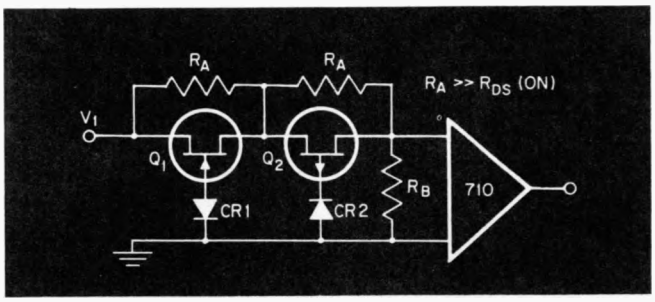


Fig. 2. New comparator protection circuit extends differential and input voltage ranges while maintaining accuracy.

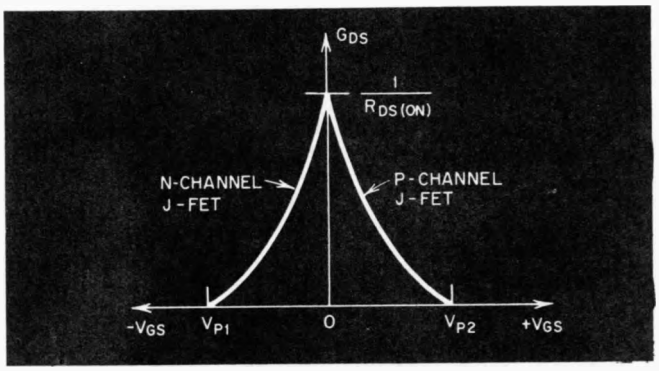


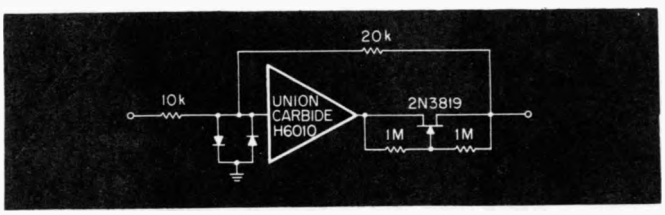
Fig. 3. Graph of FET conductance versus comparison points.

FET protection for op amps

HERE'S a circuit to protect op amps from destruction due to the application of a voltage source at the output — even momentarily. The amplifier shown, designed to operate from ±15 V, has survived, without damage, the application of 40 V to its output, when this circuit was used.

The protection comes from an inexpensive, plastic-cased JFET, the 2N3819, which has an I_{DSS} of 10 mA, an on resistance of 200 Ω and a breakdown voltage exceeding 50 V. Enclosed in the loop of the op-amp circuit, designed to deliver 5 mA, the FET has almost negligible effect on performance. The two 1-MΩ resistors keep the FET fully on.

If a low-impedance voltage source is connected to the output, the FET permits only 10 mA to flow from the amplifier. The excess voltage is developed across the FET and the 20-kΩ feedback resistor. Diodes can be used at the op amp's input to protect against too high input voltages. ■



A junction FET at the output protects an op amp from the inadvertent application of a voltage source there, while diodes at the input protect against excessive input voltages.

Section 4
FILTER & SUPPRESSION CIRCUITS

Directional Frequency Splitter Filter

THE FILTER to be described was designed to allow simultaneous transmission of tv and fm frequencies (54-220 mc) in one direction and sub-frequencies (0-39 mc) in the opposite direction in community or closed circuit tv systems. This feature can be utilized for broadcasting live community tv shows of local interest such as news or sports, or for two-way tv communication in schools, military bases or hospitals.

A modified repeater amplifier station is shown in Fig. 1 for two-way tv communication. As indicated in Fig. 1, the directional frequency splitter consists of two low pass filters to pass signals from 0-39 mc and two high pass filters to pass signals from 54-220 mc.

The main difficulty encountered in the design of the composite filter was obtaining sufficient rejection and isolation of undesired signals with a reasonably sized package. A standard five-inch rack mounted panel was decided upon. The high pass filters attenuate the low-frequencies at least 75 db,

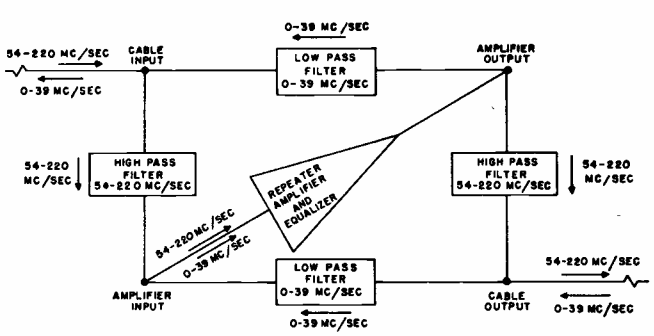


FIG. 1—Modified repeater station.

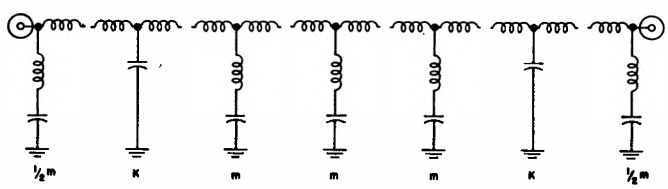
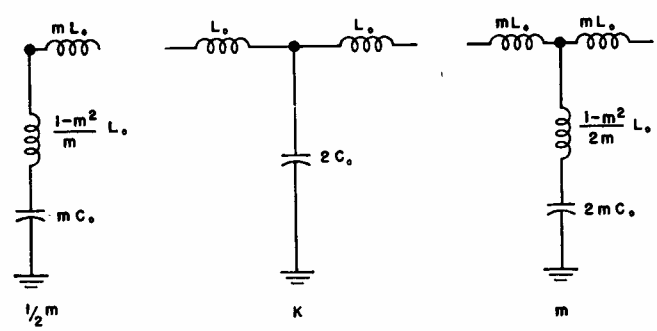


FIG. 2—Low pass filter.

and the low pass filters attenuate the high frequencies at least 75 db. All filters have a maximum vswr of 1.2 over their pass band.

Another important requirement is that the attenuation of frequencies between 39 and 54 mc should be at least 40 db between the amplifier input and output terminals with the amplifier removed and the cable input and output terminals terminated in 75 ohms, the characteristic terminating impedance of the filter. This provides sufficient gain margin at the critical crossover frequency to pre-



f_0 = CUTOFF FREQUENCY OF FILTER.

f_∞ = TRAP FREQUENCY OF m SECTIONS = $\frac{f_0}{\sqrt{1-m^2}}$

R_n = NOMINAL FILTER IMPEDANCE = $\frac{1}{2\pi f_0 \sqrt{L_0 C_0}}$

$L_0 = \frac{R_n}{2\pi f_0}$

$C_0 = \frac{1}{R_n 2\pi f_0}$

FIG. 3—Design equations for low pass filter.

vent unwanted oscillations in the circuit.

The original design was based on Tchebycheff equal ripple behavior in the stop band by proper selection of the m and k values of the many sections of filters required for rejection specifications of 75 db minimum. It was found to be expedient and resulted in a less complex filter to deviate slightly from pure Tchebycheff design to eliminate inadequate rejection between amplifier input and output terminals. This was experienced originally since a

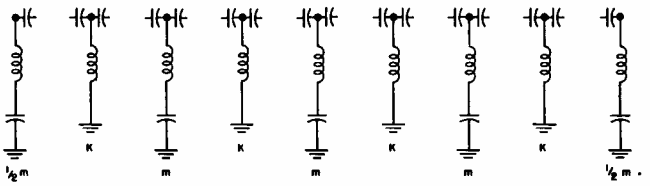


FIG. 4—High pass filter.

common cutoff frequency was chosen for the low pass and high pass filters to provide both satisfactory pass band vswr and adequate stop band attenuation with minimum components. Deviation also permitted meeting all specifications utilizing standard stocked values of capacitors (all coils being adjustable).

Each low pass filter consists of two m derived terminating half sections, three m derived full sections and two constant k full sections as shown in Fig. 2. Figure 3 gives equations for the various type low pass sections.

Each high pass filter consists of two m derived terminating half sections, three m derived full sections and four constant k full sections as shown in Fig. 4. Figure 5 gives equations for the various type high pass sections.

When the high pass and low pass filters are connected in parallel at one end, the shunt legs of the terminating m half sections can be eliminated if the terminating half sections have equal m values

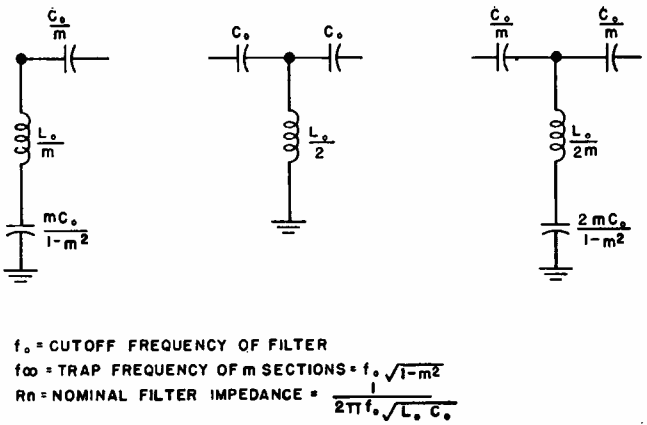


FIG. 5—High pass filter design equations.

and the product of the cutoff frequencies equals the product of the highest useful frequency of the low pass filter and the lowest useful frequency of the high pass filter.

The complete circuit with trap frequencies and component values is shown in Fig. 6. Since all inductors are variable and vary from theoretical

Table I — Coil Data

	Turns
L1, L3, L5, L7, L10, L23, L26, L28, L30, L32	5
L12, L13, L20, L21	7
L11, L22	9
L2, L4, L29, L31	10
L15, L18	11
L9, L24	14
L14, L19	15
L6, L27	17

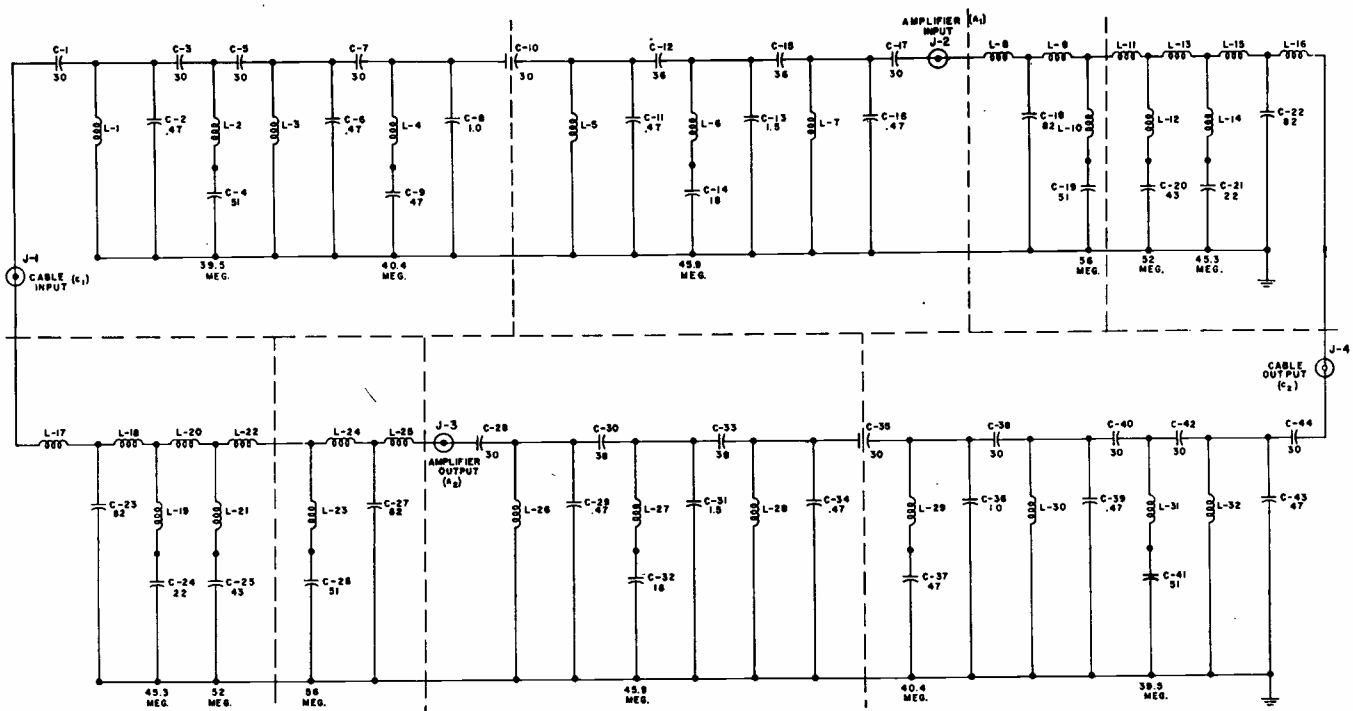


FIG. 6—Complete circuit of frequency splitter. All capacitor values are in μμf.

values due to coupling, stray capacitance and inductance of tie points, the number of turns is listed which will give a convenient adjustment. The low value capacitors in the high pass filter sections are compensating capacitors for the unavoidable (for practical manufacturing considerations) series lead inductance of the series high pass capacitors. The trap sections are first adjusted to their proper frequency indicated in Fig. 6, and all remaining inductors are then adjusted for best pass band vswr.

All coils are air wound on a 0.25 inch diameter. The ten 5-turn coils have No. 22 polyurethane insulated wire. All other coils are No. 20 polyurethane. Table I gives the numbers of turns for all coils.

Muting System for Motor-Tuned Receivers

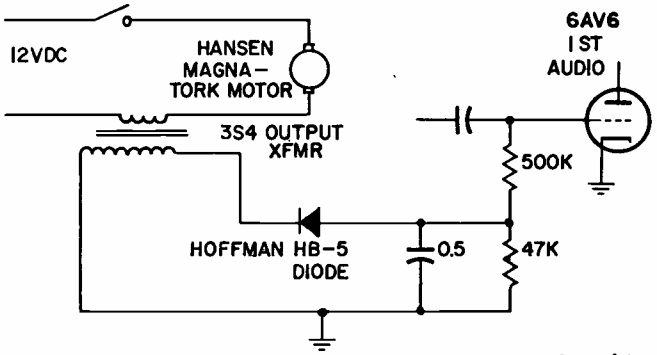
USE of fractional horsepower dc motors for remote tuning or channel changing of marine, communications, and television receivers has become widespread. Since this type of motor is a prolific source of electrical noise, its use entails the employment of some system of noise suppression. The obvious and conventional method is to use a muting relay, which means additional power consumption and possible space problems.

The muting system described herein was developed for use in conjunction with a retrofit channel-changing system for an eight-channel marine radio. Instead of a muting relay, the circuit utilizes four components whose total cost is less than that of a single relay. Operation is dependent upon the fact that the input current to a commutator-type motor is full of spikes and fluctuations.

Application of power to the motor causes an immediate surge of noise current through the primary of the transformer. The resultant high voltage appearing across the secondary is rectified and filtered, and then applied to the first audio stage as cutoff bias. As long as the motor continues to run, the noise currents will keep the audio system effectively silenced.

A convenient feature of this system is that no components of critical value are required. The transformer can be an output transformer with a turns ratio of around 50:1, and since the noise currents contain no low-frequency components, only a very small core size is necessary.

The rectifier can be any diode having an inverse voltage rating of 100 volts or more. The resistor should be a small fraction (less than one-tenth) of the audio grid resistor, and the capacitor is chosen for the desired muting hold time, or the time the audio is disabled after the motor stops. In the circuit shown, the audio amplifier remains cut off for



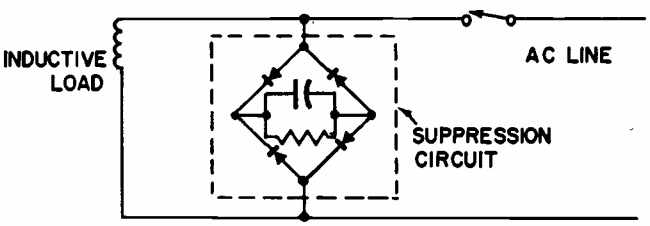
Noise pulses from motor are rectified and used to bias audio stage to cutoff.

approximately 0.25 second after power is removed from the motor. The author developed this circuit while employed at Pearce-Simpson, Inc., Miami, Fla.

Transient Suppressor for AC Circuits

SUPPRESSING the kickback of inductive loads, such as relays, solenoids, etc., when the power is interrupted is usually done by connecting a nonlinear circuit element across the load. Such nonlinear elements are zener diodes, selenium arc suppressors and others. The difficulty is that they must have their voltage characteristic tailored very carefully to suit the particular operating voltage of the system. Also, the sharp breakdown needed for fully effective suppression is difficult to obtain at a reasonable cost.

The circuit shown is composed of inexpensive



Capacitor fed by bridge rectifer forms transient suppressor of inductive kickback.

components and has the interesting feature that it can operate over a voltage range limited only by the voltage ratings of the diodes and capacitor, and yet the clamp voltage is always very sharp and adjusts itself to be equal to the peak line voltage. This is ideal for most applications.

The diodes form a full-wave bridge rectifier which has a resistor and capacitor across its output. The resistor is large and serves only to discharge the capacitor after the power is turned off. The capacitor is made as large as practical. When power

is first applied, the diode bridge immediately charges the capacitor to the peak line voltage. Once charged, the capacitor floats across the line. When power is interrupted, the high-voltage kickback exceeds the peak line voltage and the diode bridge conducts the transient into the capacitor, and the energy of the transient is dissipated in trying to charge the capacitor to a higher voltage. If the capacitor is large enough, the voltage across it will not increase significantly. No danger of ringing exists because the diodes will interrupt a reversal of current. The diodes need not be large since they only conduct surges of short duration.

Active Second Order Filter

IT IS often desirable to use active filters to overcome difficulties of simple passive filtering. The following filter provides low phase shift and a near flat response to its corner frequency with a minimum number of components. The circuit of Fig. 1 consists of a simple second-order filter combined with a transistor emitter follower which provides the necessary positive feedback.

The emitter follower provides sufficient feedback

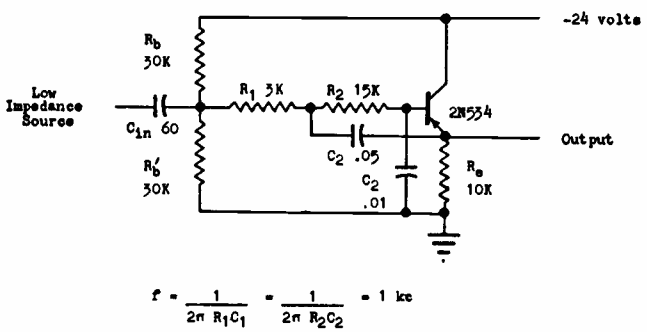


FIG. 1—Circuit of active low pass filter.

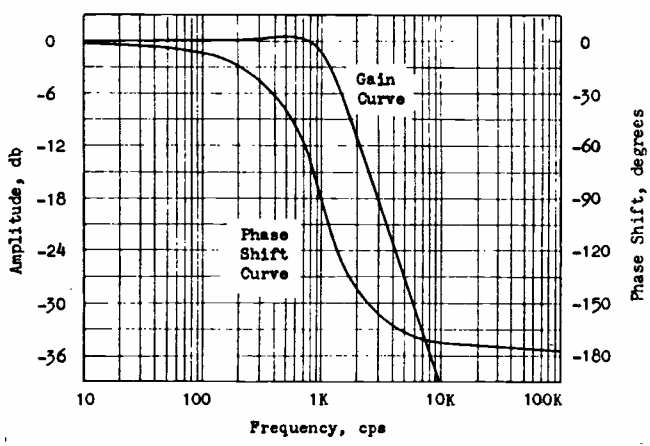


FIG. 2—Response of low pass filter.

to produce a damping ratio of 0.6, however, since the feedback can never exceed unity, the circuit is unconditionally stable. The time constants of R_1C_1 and R_2C_2 are made approximately equal, however, the impedance of R_2C_2 should be about five times that of R_1C_1 so that loading of the first filter section by the second is negligible. Typical circuit values for a 1-kc low pass filter are included in Fig. 1. The frequency and phase characteristics of this filter are presented in Fig. 2.

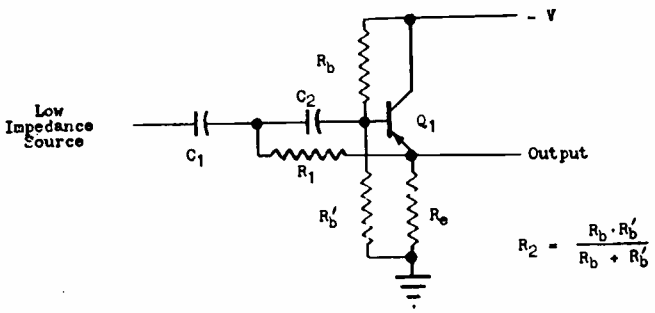


FIG. 3—Active high pass filter.

The R's and C's may be interchanged as shown in Fig. 3 to provide an active high pass filter. In this form of the circuit the bias divider resistors, R_b and R_b', also function as R_2.

The input to the low pass filter may be direct coupled (eliminating C_{in}, R_b and R_b' of the low pass) to the output of a high pass filter to form an active band pass filter. The output impedance of the active filters is low and performance is relatively insensitive to loading. The filter insertion loss is close to zero db.

Variable Rejection Band Filter

VOLTAGE SENSITIVE band-pass filter circuits have been used in equipment for re-creating speech or vocal sounds by selecting appropriate audio frequencies from a noise signal source containing a wide range of frequencies in response to a control voltage developed from a sampling of frequencies in the original spoken words.

An amplifier is arranged to pass selective bands of frequencies in response to a control voltage which acts to change the parameters of a parallel-T band rejection filter connected in a negative feedback path of the amplifier. The band rejection characteristics of the filter are varied by changing the impedance value of resistors *12*, *13* and *14* in Fig. 1. As shown in Fig. 2 each of the resistors comprise a plurality of resistors which may be selectively connected in parallel by a sequence of relays *15*, *16*, *17* and *18* which are activated by the control voltage appearing at an input terminal.

The amplifier circuit of Fig. 1 uses a triode fed by the noise signal. The cathode of the triode may

be biased somewhat above ground potential by a bypassed cathode resistor. Output signals are developed across a plate load resistor and appear at the output terminals.

Negative feedback path is provided between plate and grid through capacitor *36*, resistor *37* and the parallel-T band rejection filter network. The grid may be biased by grid leak resistor *38* which is coupled through resistor *37* and the filter network. The grid resistor is effectively connected in series with the filter network, rather than in parallel at the filter network output, and therefore will not impair the action of the filter.

The twin-T filter comprises a high-pass T section including a pair of series connected capacitors *39* and *40* and resistor *14* and a low-pass T section including the series resistors *12* and *13* and the capacitor *41*.

By varying resistors *12, 13* and *14*, the rejected band of frequencies may be shifted, these frequencies becoming the new pass bands of the amplifier. If the values of capacitors *39, 40* and *41* and resistors *12, 13* and *14* are properly chosen, the rejection bands and pass bands may be maintained at very closely the same width in cycles and may be evenly spaced along the frequency spectrum.

In the speech re-creation application, the spectrum assigned to the speech was approximately from 100 to 6000 cycles. This primary audio spectrum was divided into three major sub-bands of approximately 100 to 1500 cycles, 1500 to 3000 cycles and 3000 to 6000 cycles. In addition, the 100 to 1500 cycle major sub-band was operated on in a special manner to identify the pitch information. This resulted in a fourth sub-band in the 100 to 300 cycle range.

A voltage sensitive bandpass filter, of the type described here, was assigned to each of these major sub-bands. The filter selected a minor sub-band within the major sub-band. Because of the wide range of frequencies to be covered, optimum circuit constants were not necessarily the same in corresponding position in filters operating in different major sub-bands.

The various pass bands can be made the same width in cycles, which, of course, requires a changing Q of the filter with frequency. Some filters have been built with matching Q and reactance curves to give this constant width in cycles, but these filters are by contrast very complicated.

In the time domain of speech, the 5-millisecond delay due to the relays was completely insignificant.

The filter is electrically noisy when the contacts change and transients are introduced. This was anticipated and the effect was actually enhanced for the following reasons: During relatively steady state speech sounds, such as vowel sounds, the relays were relatively inactive and the noise injected was negligible. However, when some of the fast

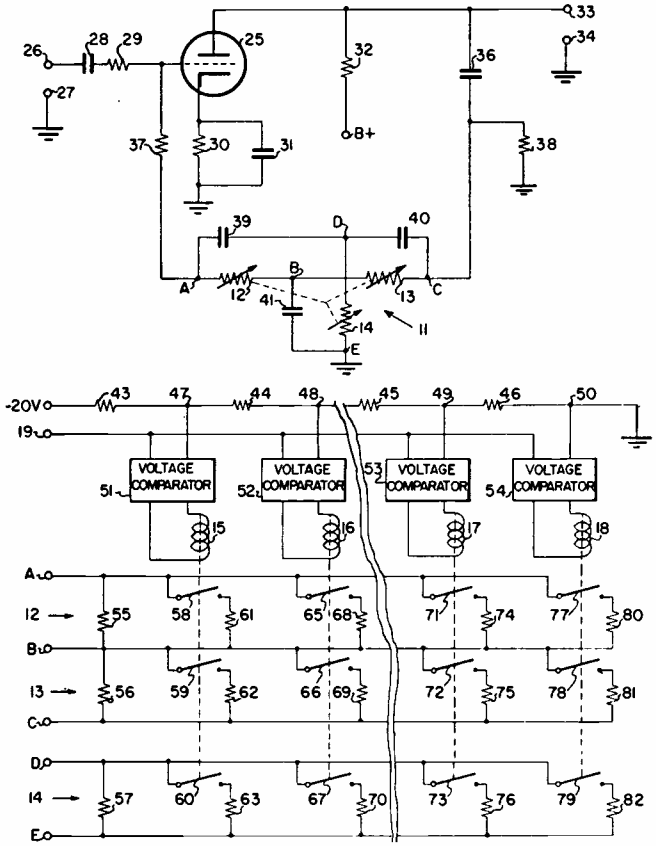


FIG. 1 Selection of resistors for filter is done by voltage comparators controlling relays.

Table of Values

Major sub-band	100 to 1500 cycles
Number of minor sub-bands	7
Capacitors *39* and *40*	0.006 microfarad
Capacitor *41*	0.012 microfarad
Bandwidth	200 cycles approximately

Minor sub-band Center Frequency	R_{12}, R_{13} Nominal Values	R_{14} Nominal Values
200	110,000 ohms	25,000 ohms
400	64,000 ohms	15,000 ohms
600	44,000 ohms	10,000 ohms
800	35,000 ohms	7,500 ohms
1000	30,000 ohms	5,100 ohms
1200	25,000 ohms	4,500 ohms
1400	20,000 ohms	3,500 ohms

speech transients were formed, such as the explosive sounds T, P, B, etc., the relays were very active and introduced a great deal of noise. Since the speech sounds themselves were noisy, the filter noise was believed to enhance the efficiency of the job the filter was supposed to perform.

By way of example, the following table of typical values is given for the major sub-band of 100 to 1500 cycles. For simplicity, resistor *37* is considered a constant, although in actual practice it was incrementally adjusted to make the output minor sub-bands of equal amplitude.

Low-Pass Filters for Wide-Band Harmonic Suppression

SIGNAL GENERATORS and other signal sources, no matter how precise, always produce harmonics and spurious signals along with the desired signal. For some applications this is of no importance. For many others, these spurious signals can be extremely annoying. For example, when making slotted line measurements, the presence of even a small amount of harmonic signal can affect the measured vswr seriously. In measuring the selectivity and interference rejection of a receiver, the signal source must be "clean."

Ideally, an extra tuned circuit after the output attenuator would solve the problem. This is impossible from a practical viewpoint due to the tracking problem. A low-pass filter will often serve the same purpose but is useful over a range of less than one octave. If the desired signal is lower in frequency than 1/2 of the filter cut-off, second harmonics will be passed. If the signal is higher than cut-off, it, too, will be attenuated. Thus the less-than-octave limitation.

If a series of low-pass filters is used, a wide range of frequencies can be accommodated. An analysis shows that if the cut-off frequencies of the various filters were spaced by a ratio of 1.6 to 1, the widest frequency range could be covered with a limited number of filters and still produce satisfactory rejection of second harmonics and all higher spurious signals. For example, if the lowest filter cut-off is chosen to be 1000 mc, this filter can be used for frequencies from about 650 mc to 1000 mc. Then,

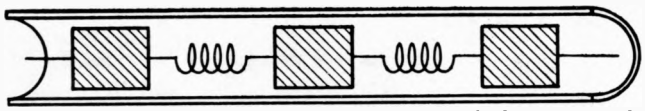


FIG. 1—Filters consists of inductance and shunt capacitance.

by using filters with cut-offs of 1600, 2500, 4000, 6500, and 10,000 mc, a frequency range of 650 mc to 10,000 mc is covered with just six low-pass filters.

However, it is not convenient to be constantly changing filters in coaxial circuits. Screw-on type of connectors are slow to attach and disconnect. Bayonet types are not very satisfactory for leakage and stability. To make the use of a series of filters convenient, it was necessary to develop a switching mechanism.

For many years there has existed a good coaxial switch which was developed and used for coaxial attenuators. This switch works on a pull-turn-push principle to disengage and engage the coaxial connectors at each end of the attenuator. Once the attenuator is disengaged, it is only necessary to rotate the desired attenuator into position with a standard turret mechanism.

To use this switch for coaxial filters, it was necessary to develop a line of filters of identical length covering the entire frequency range. This was done using a combination of lumped-constant and transmission line techniques. In Fig. 1, a cross section of the filter is shown. The series inductance is a coil of the appropriate inductance, while the shunt capacitance is a section of low characteristic impedance line. The combination can be used to produce

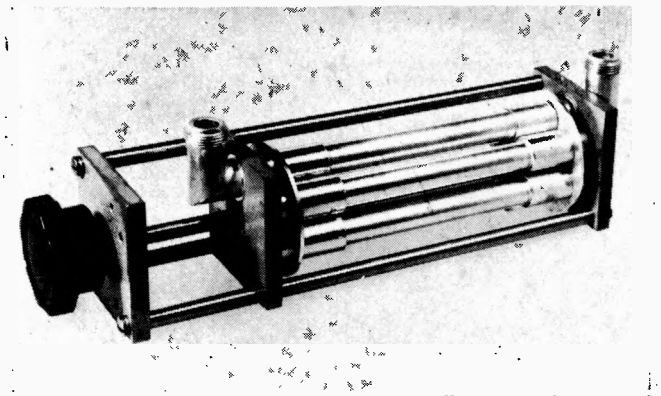


FIG. 2—Filters are combined with pull-turn-push coaxial switch.

excellent low-pass filters, over a very wide frequency range.

By using these filters and the turret switch, it was possible to develop a turret filter which would pass fundamental frequencies over a range of almost 20 to 1 and still have 40-to-60 db attenuation on all harmonics. For one application, a unit was built with the filters mentioned above to cover the frequency range from 650 to 10,000 mc. For another application, cut-off frequencies of 200, 320, 500, 800, 1300, and 2000 mc were used to cover the range from 120 to 2000 mc. A patent application has been filed on the device, shown in Fig. 2.

Transistors As Reactive Filter Elements

A TRANSISTOR may appear as capacitive or inductive to a circuit if the transistor is used in a Miller amplifier configuration. Inductances as high as 20 henrys and capacitances as large as 100 μf can be simulated using these circuits.

In Fig. 1A the transistor is used as an inductive reactance. If an ac signal is applied across collector to ground the voltage across C will lag the current. The base current I_b, of the transistor will change in proportion to the voltage variation across C. The output of the transistor will be a current which lags the voltage of the applied ac, giving an inductive effect. The inductive reactance will be equal to the X_c minus RC phase losses multiplied by the beta of the transistor. An emitter follower circuit is used to increase the input impedance of the tran-

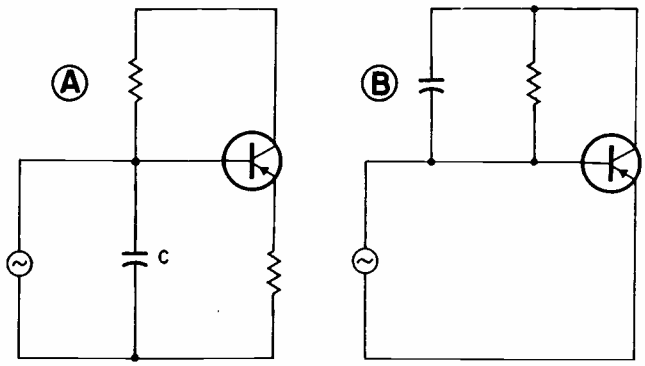


FIG. 1—Equivalent circuits for inductive (A) and capacitive (B) transistor circuits.

sistor. If not, the capacitor would discharge through the base emitter junction and exhibit a very low cross-over point.

In Fig. 1B the transistor is used as a capacitive

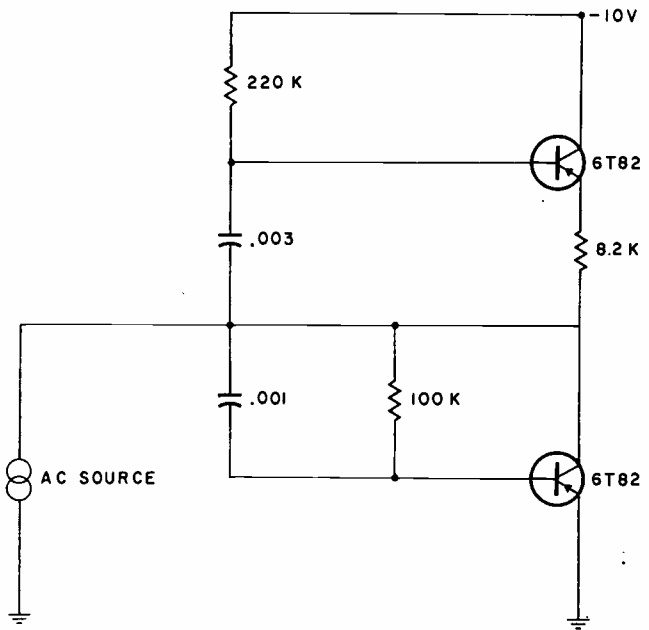


FIG. 2—Parallel-tuned circuit resonant at about 1 kc.

reactance. Here the current through C passes directly into the base. The capacitive output of the transistor is approximately equal to h_{fe} times X_c minus RC phasing losses.

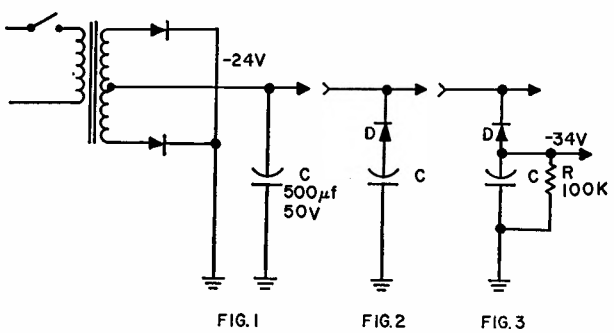
In Fig. 2, the Circuit of Fig. 1A and B are connected in series to form a parallel-tuned circuit. They resonate at approximately 1 kc and exhibit a Q of approximately 7. The inductive reactance is equivalent to a 200 mh choke across a 0.1 μf capacitor.

Rectifier Transient Protection Circuit

TRANSIENTS created by the collapse of a transformer magnetic field or inductive devices switched in and out of a power supply load can be absorbed in many ways.

A large electrolytic capacitor across the load, Fig. 1, appears to be the best "absorber"; however, this condenser filter creates poor regulation that may not be tolerable. By adding a diode in series with the capacitor as shown in Fig. 2, C will charge to the peak of the ac cycle, then uncouple until a higher pulse comes along. Repetition of pulses will gradually increase the charge across C, and a bleeder resistor R may be used as shown in Fig. 3 to counteract this rise.

Transients in the load of opposite polarity will be shunted to ground by conduction of the rectifiers. Transients from the transformer side will be coupled to the electrolytic by the transformer center tap (or by a conducting rectifier in other circuits); thus, this circuit affords protection from both directions.



Devices requiring pure dc, such as transistor amplifiers, can be run off the same supply by attaching the load to C.

Output Stage With Active Filtering

MANY APPLICATIONS require that the output stage match a high-impedance amplifier to a low-impedance load and also attenuate unwanted noise outside the useful bandwidth. The circuit, Fig. 1, combines all of these features without the use of bulky inductors. The frequency response is that of a low-pass L-C network with a coefficient of damping (c/c_o) ranging from 0.4 to 2. The network can be made maximally flat by proper selection of the ratio R_3/R_4. Experiments and calculations show this to be approximately 0.8, but it de-

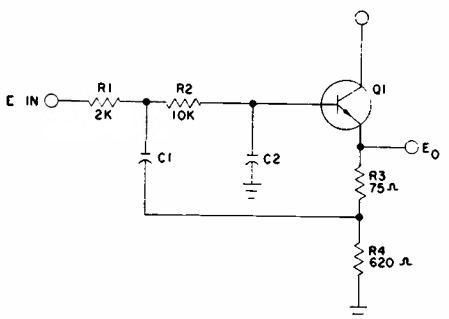


Fig. 1. Active filter output stage.

pends on some transistor parameters such as r_e, β, and the location of the poles determined by R_1C_1 and R_2C_2.

The R_1C_1 time constant is determined by the cut-off frequency desired. R_2C_2 has the same time constant, but R_2 is made five times R_1 to prevent loading of the first network. The emitter resistance, $R_3 + R_4$, should be as low as possible especially if transients are anticipated.

Rigorous analytical means can be used to describe the operation, but a brief summary is that real roots of R_1C_1 and R_2C_2, located on the real axis of the complex S-plane, can be made to become complex conjugate with the application of feedback, thereby simulating an L-C network.

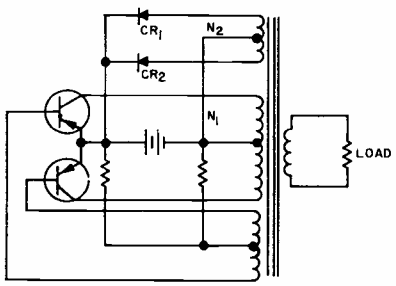
Spike Suppressor for Power Converters

ALTHOUGH it is possible to design and manufacture power-converter transformers with very low leakage reactance, such transformers usually are expensive, particularly if high power levels are involved. A tape wound core of 50-50 nickel-iron alloy often is used, but hand-winding of the primary may be necessary if bifilar winding is to be used.

In many cases, the cost of such construction prohibits its use. A more economical method is shown.

An additional winding is placed on the transformer. The number of turns in this winding is made slightly (about 5 percent) less than the number of turns on the primary winding. The diodes can then conduct only during the time when a spike voltage appears at the transistor collectors which exceeds the supply voltage by about 5 percent plus the forward drop of the diodes. In a typical 12-v design very inexpensive diodes can be used. The spike-suppression winding will carry very little average current and the wire size can be chosen on the basis of the allowable voltage drop.

One difficulty will be apparent in the design as shown: leakage reactance between the primary winding and the spike-suppression winding will tend to nullify the advantages gained. This problem can be minimized by merely tapping the primary winding at about 95 percent of its turns.



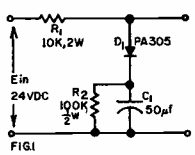
Extra winding for CR1 and CR2 suppresses transients.

One of the greatest advantages to this circuit, in addition to its cost saving features, is the fact that unlike most transient clippers, this design does not divert the spike energy into a dissipative element. The energy is returned to the input power source, thereby actually improving the efficiency!

Surge-Current Limiter Gives Fast Turn-Off

THE SURGE CURRENT that flows during turn-on of a non-linear device such as a motor or incandescent lamp can be destructive to the transistors or SCRs used for control purposes. In a motor, the initial current is limited only by the armature current; in a lamp, the cold resistance is about 20 times less than the operating resistance. Thus if full signal is applied when the equipment is turned on, the limited current rating of the control device can easily be exceeded.

The obvious solution is to use a delay network so that the applied voltage builds up slowly. A simple RC circuit provides a delay at turn-on, but also delays turn-off. This second delay is undesirable in most cases. The solution then is to make the network unilateral.



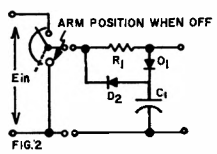


Fig. 1. Diode decreases turn-off time.

Fig. 2. Shunt resistor might be eliminated and another diode added.

The diode in the circuit allows the capacitor to charge slowly to provide the necessary turn-on delay, but prevents capacitor discharge current from flowing through the load. Turn-off thus is instantaneous. Resistor R_2 can be eliminated, as in Fig. 2, thus reducing operating drain when the signal source has a low output impedance. Another diode, $D2$, can be added to insure fast decay by bypassing R_1.

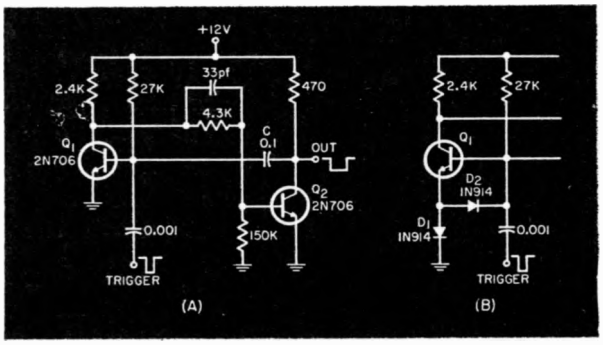
Base-Emitter Protection in Monostable Multivibrators

A COMMONLY OVERLOOKED PHENOMENON in transistor monostable multivibrators is the excessive transient base-to-emitter voltage caused by the discharging coupling capacitor. This voltage often surpasses the maximum specified V_{BE} of the device. This is particularly troublesome with high-speed transistors, where the V_{BE} ratings are generally low.

The source of trouble is capacitor C, which commences to discharge when the triggering pulse turns Q_1 off, (see Fig. 1a), effectively applying a negative voltage on the

base of Q_1, which, initially, is very close to the value of the supply voltage.

This undesirable effect can be alleviated with two diodes, as shown in Fig. 1b. When Q_1 is on, diode D_1 is conducting and the forward-bias voltage on the base of Q_1 is isolated by diode D_2. When Q_1 is off, the negative discharge voltage on its base is now applied also to the



Typical monostable multivibrator (A) and improved circuit with diodes (B).

emitter via diode D_2, causing low V_{BE}. D_1 isolates the discharge voltage until its value reaches the critical point, causing Q_1 to turn on.

The circuit shown produces a pulse width of 200 μsec. ◆◆

The FET as a Voltage-Controlled Resistor

THE UNIQUE PROPERTIES of the field-effect transistor can be used to make an excellent voltage-controlled resistor, both for dc and for ac.

One example is a high-impedance (100-K or more) dropping resistor, working into an audio-frequency anti-resonant filter (Fig. 1). Since the iron-cored inductors of the filter are sensitive to signal amplitude, a constant voltage must be delivered to the filter when the input varies.

The circuit of Fig. 2 performs the desired functions. Since the input is ac, the drain-source voltage is alternately positive and negative. Due to the bi-directional characteristic of the drain-source channel, *either end* may be used as the source.

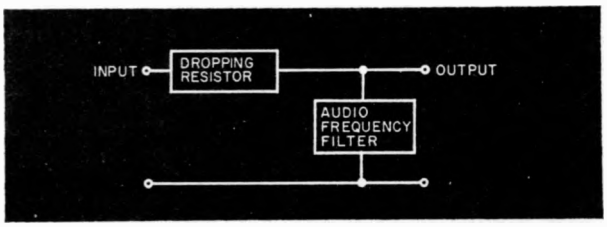


Fig. 1. Voltage control for audio-frequency filter.

When the input is positive, terminal A serves as the source and B as the drain, and when the input is negative, terminal A serves as the drain and B as the source. In either case, CR_1 and CR_2 insure that the gate is reverse-biased with respect to the terminal which serves as the source.

Self-bias is developed across R_1 or R_2 (depending on input polarity). With low input (low bias), the drain-source

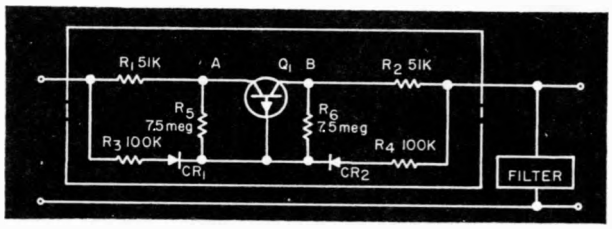


Fig. 2. FET voltage-controlled resistor.

resistance is a few hundred ohms. As the input, and consequently the bias, increases, the drain-source resistance increases to several hundred thousand ohms.

The FET used in this case is the 2N2386. With a 100-K resistor in place of the filter, the output increases with input up to approximately 10 v peak to peak, and stays constant with inputs over 50 v peak to peak. Without R_5 and R_6, the output limits at less than 10 v peak to peak, and actually decreases with increasing input; however, some distortion is introduced. ◆◆

Delay Line Output Amplitude Equalizer

THE CIRCUIT shown in Fig. 1 was developed to provide a pulse train from a delay line without the use of amplifiers for each delay line tap.

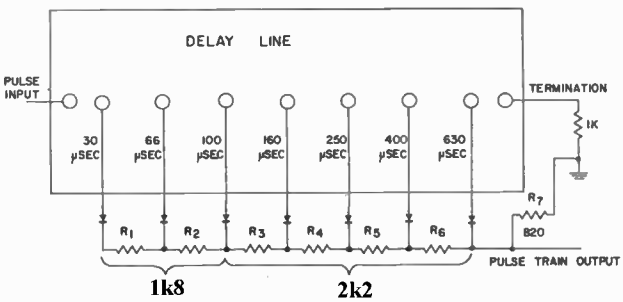


FIG. 1—Delay line output amplitude equalizer.

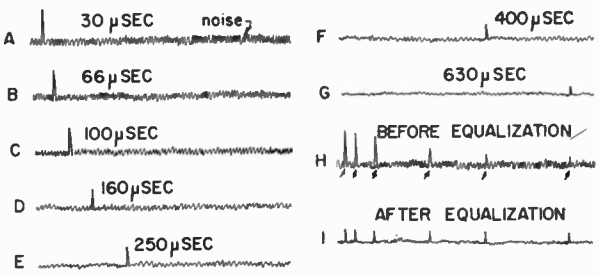


FIG. 2—Waveforms at points identified in text.

As shown in Fig. 2, waveforms A through G, the signal to noise ratio at all taps is approximately the same, however the noise output from the first tap, at 30 microseconds, is about the same amplitude as the desired signal output from the last tap, 630 microseconds. When the signals are added together without equalization, wave-

form H results. As can be seen, the 400 and 630 microsecond delayed pulses are lost in the noise from the first taps.

In the circuit shown, R_1 through R_6 attenuate the signal and the noise by varying amounts for each tap. The output pulse train waveforms are shown at I. A single amplifier is used where desirable to amplify the signals. If the difference in the desired alternation at adjacent taps is not great, some of the alternation resistors R_1 through R_6 may be eliminated by increasing the value of the others.

Transient Load With Exponential Decay

A CAPACITOR IS OFTEN USED as a transient load with exponential decay. However, for heavy load or wide range requirements, use of a capacitor is not feasible due to size and range limitation.

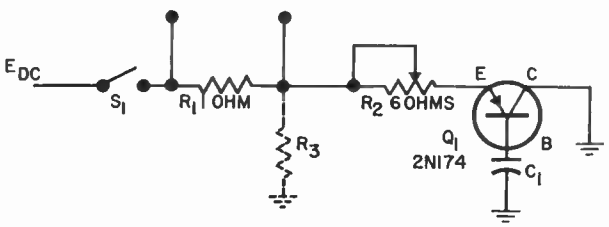


Fig. 1a. Circuit monitor provides transient load with exponential decay.

Illustrated in Fig. 1A is a circuit which has wide application as an exponential decay transient load that is compact in size and is of extended range. When a voltage E_{dc} is applied by the closing of switch S_1, base B of transistor Q_1 is initially at ground potential due to capacitive action of C_1; thus, Q_1 conducts most heavily. As C_1 charges, the conduction of Q_1 decreases. Maximum load current I_1 is established by adjusting resistors R_2 and R_1 (Fig. 1B). Time duration, t, is established by the product values of C_1 and the sum

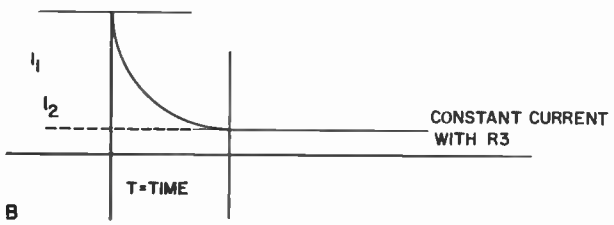


Fig. 1b. Output waveshape shows exponential decay for current with time.

of R_2 and R_1 (Fig. 1C). Insertion of resistor R_3, permits a constant current I_2 level of operation. Use of the 1 ohm resistor R_1, provides a current monitoring device. The current may be displayed directly on an oscilloscope. The circuit is useful in applications that require simulation of a transient load with an exponential decay.

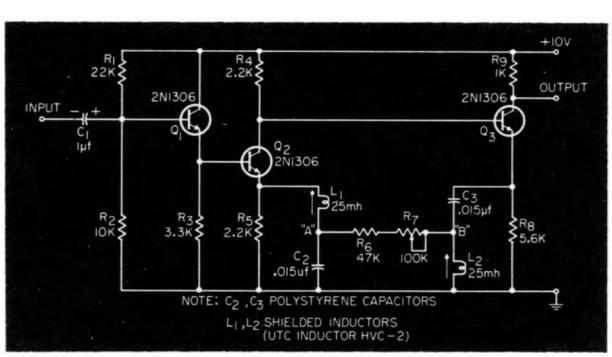
VDC	R_3	I_2	C_1	t	I_1	R_2
32	—	—	50MFD	50MS	18.7a	0.7
32	—	—	100MFD	1SEC	6.3a	4.1
32	—	—	70MFD	300MS	8.0a	3.0
32	28	1.1	70MFD	100MS	21.5a	0.5
32	200	0.16	70MFD	300MS	7.0a	3.6

Fig. 1c. Time durations for various combinations of C_1 ($R_1 + R_2$).

Stable Q Multiplier

THIS CIRCUIT FULFILLS A NEED for a high-selectivity, single-frequency tone filter that often is required in simple telemetry systems. In the audio frequency range, physically small high-Q inductors are unavailable. To obtain high selectivity (Q of about 200) with compact inductors requires a Q multiplier stable over a wide temperature range, such as the circuit shown.

Transistors Q_2 and Q_3 form a two-stage amplifier. The emitter resistors R_5 and R_8 are bypassed at the required tone frequency by the respective series-tuned resonant circuits L_1, C_2 and L_2, C_3. This basic circuit is a bandpass amplifier with peak response at the tone frequency, but rather broad in bandwidth. However, because of the bypass configuration, points A and B are exactly in phase at the resonant (tone) frequency. Inserting a small conductance (R_6 and R_7) between these points allows positive feedback at this frequency. The amount of feedback is varied by R_7; decreasing the resistance of R_7 increases selectivity. At resonance, the driving impedance into the base of Q_2 becomes very low, and thus an emitter follower Q_1 is used to increase the input impedance.



Stable Q multiplier.

In a typical application the circuit was adjusted for a center response frequency of 8 kc and bandwidth of 40 cps. The tone output remained constant within 2 db over a temperature range of 0°C to 55°C.

Active bandpass filter with adjustable center frequency and constant bandwidth

ACTIVE FILTERS are becoming more and more popular now that low-cost op amps and linear ICs are widely available. The simple bandpass filter, shown here, needs just an op amp plus a few discrete components.

In this circuit, a single resistor controls the center frequency without changing the bandwidth or the gain.

With the component values shown, center frequency can be shifted from 1.6 kHz to 2.4 kHz by changing R_c from 1100 ohms to 406 ohms. The 3-dB bandwidth remains constant at 260 Hz. Center-frequency gain varies only ±0.5 dB from the nominal 26 dB. Bandwidth at the −10 dB points is 775 Hz.

Filters can be designed for a wide range of parameter values. Here is a simple step-by-step procedure for calculating the component values from specified values of bandwidth, gain and range of center-frequency adjustment:

Step 1. Choose values for mid-frequency f (Hz), nominal voltage gain G, and 3-dB bandwidth Δ (Hz).

Step 2. Select a convenient Value C for the capacitors.

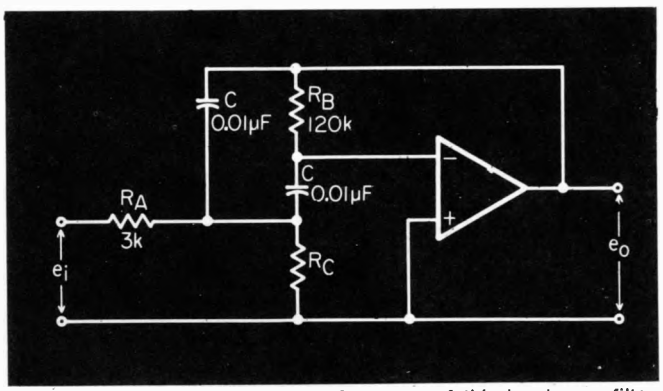
Step 3. Calculate the required resistor values from the following equations:

$$R_A = \frac{1}{2\pi \Delta GC} \quad (1)$$

$$R_B = \frac{1}{\pi \Delta C} \quad (2)$$

$$R_C = \sqrt{\frac{1}{2\pi C\left[(2f^2/\Delta) - \Delta G\right]}} \quad (3)$$

Circuits, designed by this technique, can be used singly as tunable filters; or they can be used in multiple combinations to form a comb filter in which each section can be individually adjusted to an exact frequency.



Value of Rc determines the center frequency of this band pass filter. Adjustment has no effect on bandwidth.

Optimum zener decoupling

DECOUPLING capacitors are often used across zeners, as in Fig. 1a, to filter out conducted interference. Because the zener's internal resistance R_z is small compared to the bias resistor R_s, the value of R_z determines the filtering, as shown in the equivalent circuit of Fig. 1b. The effective filter cutoff frequency f_c equals $1/(2\pi R_z C_p)$.

The small change in Fig. 2a can improve performance significantly. The dc regulation remains the same but, for decoupling, the value of R_z is negligible and the network, whose equivalent circuit appears in Fig. 2b, has the maximum possible value of series resistance, $R_s/4$. The cutoff frequency, now equal to $4/(2\pi R_s C_p')$ is reduced by a factor of $R_s/4\ R_z$ for circuits with $C_p = C_p'$.

As an example, let's assume a 6.2-V zener regulator operates from a 29-V supply with conductive interference up to 1000 Hz. A 3-kΩ resistor R_s provides 7.5-mA bias current to the 5-Ω zener. For the shunt capacitor of Fig. 1a we need

$$C_p' = \frac{1}{2\pi \times 1000 \times 5} = 31.8\ \mu F$$

For the revised circuit, however, we can use

$$C_p = \frac{1}{2\pi \times 1000 \times 750} = 0.21\ \mu F$$

for a reduction in capacitor size by more than two orders of magnitude.

The proposed circuit would use two ⅛-watt resistors and a 0.2-μF capacitor operating at about 18 V. The less effective network has a ¼-watt resistor and a 30-μF capacitor operating at 6.2 V. The component trade-off favors the newer circuit.

Load circuits with internally generated noise may still require the conventional decoupling. In that case, the proposed circuit, if used with a capacitor across the zener, effectively decouples residual noise from the power line.

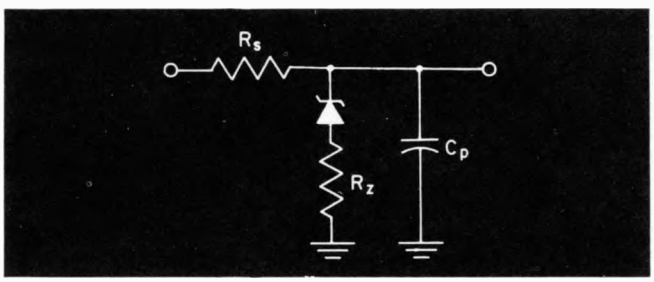


Fig. 1a. Basic circuit of zener shunted by decoupling capacitor used to filter out conducted interference.

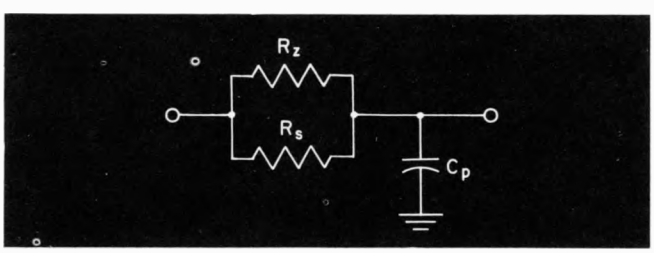


Fig. 1b. Equivalent circuit of Fig. 1a.

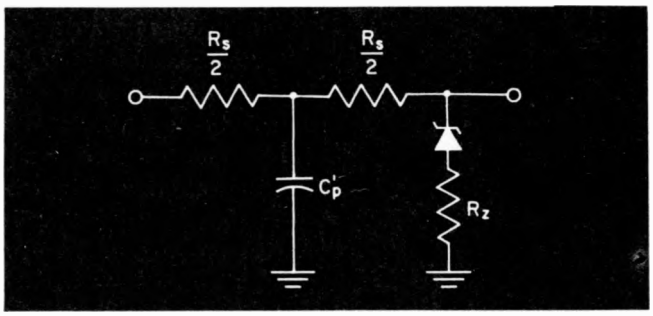


Fig. 2a. Slight modification of earlier circuit gives significant improvement.

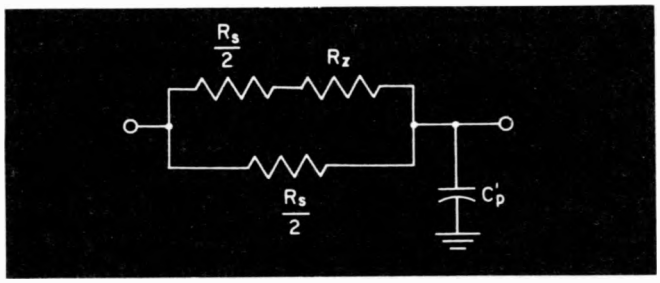


Fig. 2b. Equivalent circuit of Fig. 2a.

Digital ICs serve as audio filters

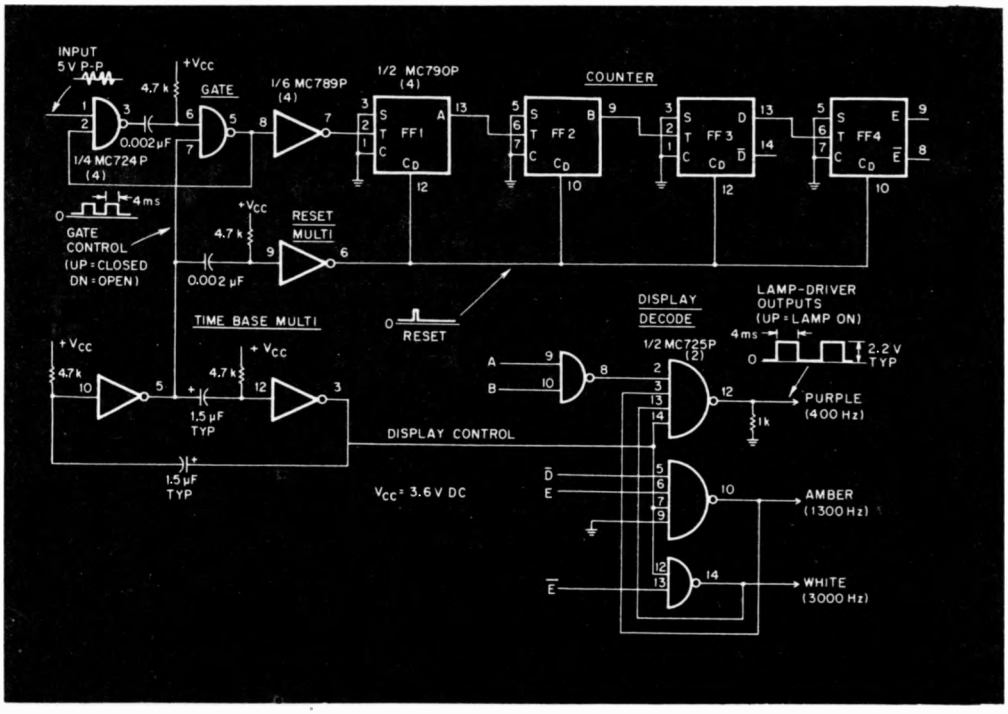


Fig. 1. A digital-IC frequency counter selects the proper coded audio signals for driving the proper display lamps.

In most conventional marker beacon receivers, coded audio frequencies (400, 1300 or 3000 Hz) associated with particular indicator lamps are selected by LC tuned circuits. Since the tuned circuits operate at audio frequencies, they are large and heavy. Other components sometimes used to obtain the required audio selectivity, such as RC notch filters, are cumbersome and often unreliable since tight component tolerances and typical long-term instability leave much to be desired.

In the alternate system shown in Fig. 1, the more conventional filter circuitry is replaced entirely by digital ICs. The arrangement shown is actually a simple, low-frequency counter. Since the counter capability required for effective audio-frequency selectivity is low, the time-base frequency can be selected such that it may vary as widely as 25% from its initial nominal value. Reliable long-term operation is thus assured and, of course, no periodic tuning is required.

Operation of the counting circuit is conventional, with counting and display periods of approximately 4 ms each. When the gate-control line is positive, the gate is closed, and the previous count is displayed. At the instant the gate-control line goes low, the counter flip-flops are reset, and the gate (which also serves as part of the monostable multi that shapes the input-signal waveform) is enabled, allowing the counter to accumulate one count for each input cycle that occurs while the gate is open.

Input Freq (Hz)	Cycles in typical 4-ms count	Lamp activated	Nominal lamp modulation
100-250	0	None	None
250-1000	1, 2 or 3	Purple	400 Hz
1000-2000	4-7 inclusive	Amber	1300 Hz
2000-4000	8-15 inclusive	White	3000 Hz

Fig. 2. Typical lamp states as a function of input frequency.

After the gate closes, the accumulated count is displayed. Since the duration of the count cycle (which is determined by the time-base period) is constant, or nearly so, then the count that is accumulated and subsequently displayed is proportional to the frequency being counted. With the values given, each of three frequencies of interest will light an associated lamp.

A tabulation of the lamp-display output states as a function of input frequency over the range of 100-4000 Hz, the normal marker beacon receiver audio-frequency bandwidth, is shown in Fig. 2. The tabulation is for illustration only. It does not consider the normal ±1-count ambiguity. Any degree of audio selectivity can be provided at the cost of added circuit complexity. The principal aim here is to provide a minimum reliable realization of the required function.

The indicator lamps are disabled during the counting period to prevent display-lamp flicker. The system is extremely immune to noise-induced false-count displays since a fresh count is made and displayed every 8 milliseconds.

The use of inexpensive plastic-package RTL, like the MC-700P series, is quite suitable if extreme temperature range is not a problem. Five chips are required to implement the design as shown.

Simple solid-state noise filter for industrial logic systems

THIS CIRCUIT provides a useful interface between a noisy outside world and the necessary quiet of timing and logic circuits associated with electromechanical controls.

Even with 24-volt logic circuits, noise is often a serious problem in situations where control lines may be extremely long, and where there may be considerable 60-hertz radiation — for example, with installations such as SCR mill drives. Buffer relays are often used for logic interface in high-noise environments; but these are slow, expensive and bulky. Passive filter networks provide another possible answer; but these are also expensive, they cannot filter out dc level shifts, and they adversely affect the rise and fall times of the logic signals.

Though the circuit described here is relatively crude, it is simple and effective. It has none of the disadvantages associated with relays or passive filters. It is a three-terminal active network; and needs no external power other than the input logic.

The circuit works like a Schmitt trigger. There is no output until the input voltage exceeds the breakover voltage of the 4-layer diode D_1. When D_1 switches to the "on" state, the output jumps to the zener voltage of D_2. Level fluctuations and noise at the input are taken up by R_1.

With the specified components, input "on" and "off" levels are 9.1 volts and 5.6 volts respectively. Noise immunity is 6 volts ac with the input dc level at zero. With the input dc level at 24 volts, the output will not switch with ac inputs of up to 12 volts. The table shows dc switching levels and ripple at various noise frequencies.

During turnoff, the output remains in the "on" state until the current in D_1 decreases below its holding value. The following equations will allow the circuit designer to select component values to suit his needs.

For output "on,"

$$V_{in} \geq V_{(BR)F} \quad (1)$$

For output "off,"

$$V_{in} \leq I_H R_1 + V_z \quad (2)$$

and,

$$R_1 < (V_{(BR)F} - V_z)/I_H \quad (3)$$

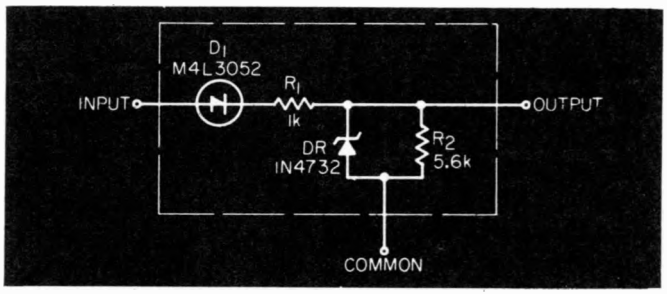
Resistor R_2 provides a current path for D_1 at the time when the diode begins to trigger. Without R_2, triggering would be poor because of the high impedance of the zener below its knee. The value of R_2 must be low enough to aid turn-on of D_1, but not so low as to cause the output voltage to drop significantly while the input decreases.

$$R_2 > V_z/I_H \quad (4)$$

Typical rise and fall times for this circuit are 20 microseconds and 8 microseconds respectively. One further advantage of the circuit is that diodes D_1 and D_2 can easily be inverted to provide the same circuit action for negative logic voltages. ■

RIPPLE REDUCTION FOR VARIOUS NOISE FREQUENCIES

RIPPLE ON ZERO VOLTS dc OUTPUT	INPUT (ac)		INPUT (dc) VOLTS
	VOLTAGE	FREQUENCY	
10 mV	6V	100Hz	0
50 mV	6V	1 KHz	0
400 mV	6V	10 KHz	0



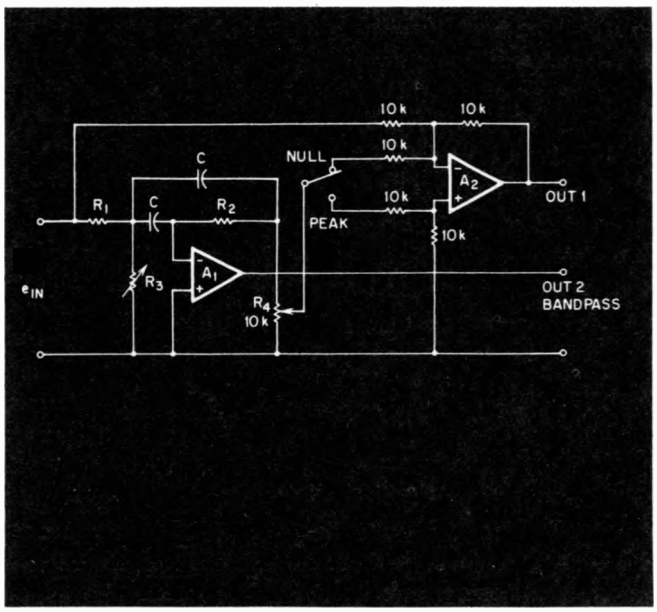
Simple, three-terminal active filter works like a Schmitt trigger, yet needs no external dc supply.

A novel active filter

A SIMPLE modification of a multiple inverse feedback filter gives either constructive or destructive interference at a selected frequency. The filter (A_1) both shifts the signal phase by 180° and gives unity voltage gain at the tunable center frequency f_o. The filter output is either added to the original signal for a null, or is subtracted for a peak in summing amplifier A_2. The amount of filter output used determines the depth of the null or the height of the peak. With the switch in the null position, the null is complete at the maximum setting of R_4. With the switch in the peak position, the peak is up by 6 dB at the maximum setting of the potentiometer. In addition, the bandpass response of the filter is available at output 2.

Three-dB bandwidth and midband voltage gain are independent of frequency control R_3. The feedback filter works best for Q values less than 10 and has reasonable component values down to low audio. In terms of f_o, the center frequency, and Δ, the 3-dB bandwidth in Hz, the time constants for the filter are: $R_1C = 1/2\pi\Delta$, $R_2C = 1/\pi\Delta$ and $R_3C = 1/2\pi\Delta\ (2f^2/\Delta^2 - 1)$.

Typical values for $f_o = 1000$ Hz and $\Delta = 232$ Hz are: $C = 0.005\ \mu$F, $R_1 = 138$ k, $R_2 = 275$ k and $R_3 = 5$ k. ■



This active filter provides bandpass, band-reject and band enhance responses.

High-efficiency, miniature decoupler

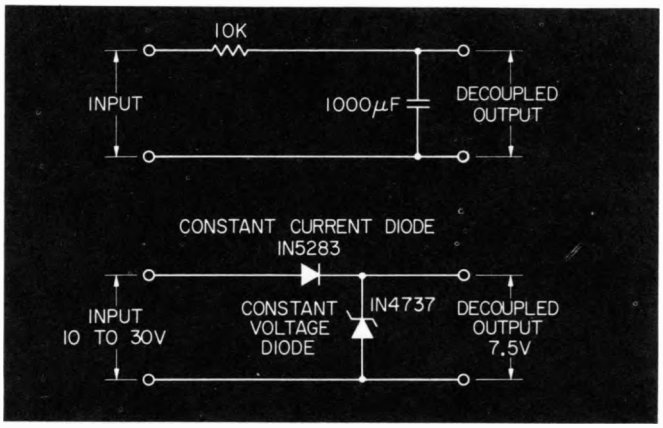
IT'S USUALLY NECESSARY to decouple the power supplies used with high-gain amplifiers to prevent oscillation due to feedback through the power lines. A disadvantage of the conventional network at the top of the figure is that decoupling is not very effective at low frequencies where good decoupling is often very important.

For example, a 1000-μF capacitor has a reactance of 160Ω at 1 Hz, so 1-Hz ripple is attenuated by a factor of only about 60. It is at frequencies of about 1 Hz that motor-boating oscillation occurs. Further disadvantages of this circuit are that it introduces phase shift, increasing the possibility of oscillation, and it requires physically large components.

The lower circuit in the figure overcomes all these disadvantages. The 1N5283 is a current-regulator diode, which is a two-terminal field-effect device with common source and gate as one terminal and drain as the other. The 1N4737 is a conventional regulator diode.

When used with a load requiring almost zero current, the attenuation of this circuit at 1 Hz exceeds 50,000 to 1 from dc to many kilohertz. The fact that attenuation is maintained down to dc is a significant advantage in preventing low-frequency oscillation. The circuit also uses small components.

Excellent decoupling from dc to very high frequencies can be achieved by adding an rf choke in series with the input to the 1N5283 and a capacitor across the decoupled output. Decoupling can be maintained for load currents that aren't negligible compared to the zener current by using an appropriate emitter-follower circuit as a buffer. ■



The conventional decoupling circuit at the top uses large components, yet it's not effective at low frequencies; it introduces phase shift and increases the possibility of low-frequency oscillation. The bottom circuit eliminates these problems, offering high attenuation from dc to high frequencies.

Section 5
PULSE CIRCUITS

Fast Recovery Monostable Multivibrator

THE CIRCUIT shown in Fig. 1 requires fewer components than a standard one-shot multivibrator and it has a fast recovery, usually on the order of 1/100 of its period. It may be triggered with either positive or negative pulses.

Initially both transistors are conducting. Base current is supplied to Q_2 thru R_3 which keeps it in saturation. Since Q_2 is saturated, base current is supplied through R_2 to saturate Q_1. In this state capacitor C has a charge of almost V volts.

With the circuit in this stable state it may be triggered into the unstable state by a positive pulse at the base of Q_1 or a negative pulse at the base of Q_2. In either case the net result of the trigger is to turn off Q_2 thus allowing its collector to go positive, this turns off Q_1 and its collector goes to ground. In this way both transistors are cut off.

The timing is done in much the same way as in a conventional one-shot, the base of Q_2 is initially at approximately V volts and it is charging toward $+V$ volts. When the base voltage reaches zero volts Q_2 will conduct which turns Q_1 back on. Note that transistor Q_1 can supply large collector currents to recharge C to its original voltage very rapidly.

The period of the one-shot is given approximately by:

$$\tau = 0.69\ (R_1 + R_3)\,C$$

The recharge time constant is given by:

$$\tau_{Rch} \approx R_3 C/\beta_1$$

The diodes CR_1 and CR_2 are used to protect the base to emitter junction from excessive voltages,

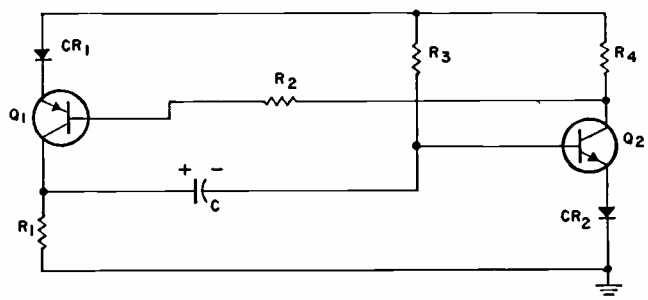


FIG. 1—Circuit of fast recovery monostable multivibrator.

if however transistors with a high inverse V_{BE} rating are used, these diodes may be omitted.

Typical values for resistors R_1 and R_4 would be 1000 ohms; for R_2 and R_3, 10 K; and capacitor C to suit. Transistor Q_1 can be a 2N1132 or 2N1259; Transistor Q_2 can be a 2N697 or a 2N706. The diodes can be 2N663 or equivalent.

Fast Monostable Multivibrator

DELAY WAVEFORMS of short duration and fast rise and fall times may be obtained using current switching techniques. Nonsaturating circuitry and drift transistors are used in the circuit shown in Fig. 1.

In the stable state T_2 is on and T_1 is off. The base of T_2 is returned to the negative supply through R_3 holding T_2 on. The voltage at the base is clamped to approximately —0.5 v (the on voltage of silicon diode D_1) so that the emitter of T_2 is slightly negative. This means that the emitter base junction of T_1 is reverse biased, holding T_1 off. The current through T_2 is determined by E_1 and R_1 so T_2 is held out of saturation by picking R_4 sufficiently small.

When an impulse of current is applied to the base of T_2, the voltage there becomes positive to the point where D_2 conducts and clamps the base voltage to +0.5 v. The emitters of T_1 and T_2 try to follow the base voltage of T_2 but when the emitters become positive, the emitter base junction of T_1 becomes forward biased and T_1 turns on, turning T_2 off. Thus, during this transient condition the common emitter current is switched from T_2 to T_1.

This current, now flowing in the collector circuit of T_1, tries to raise the collector potential toward ground. This is prevented initially by the capacitor since the voltage across it cannot change instantaneously and the potential at the other end of the capacitor is clamped by D_2. Therefore none of the current switched through T_1 passes through R_2 but rather through the capacitor into the junction of D_1, D_2, and R_3, and the base of T_2. This current is in the same direction as the trigger pulse, and thus holds T_2 off.

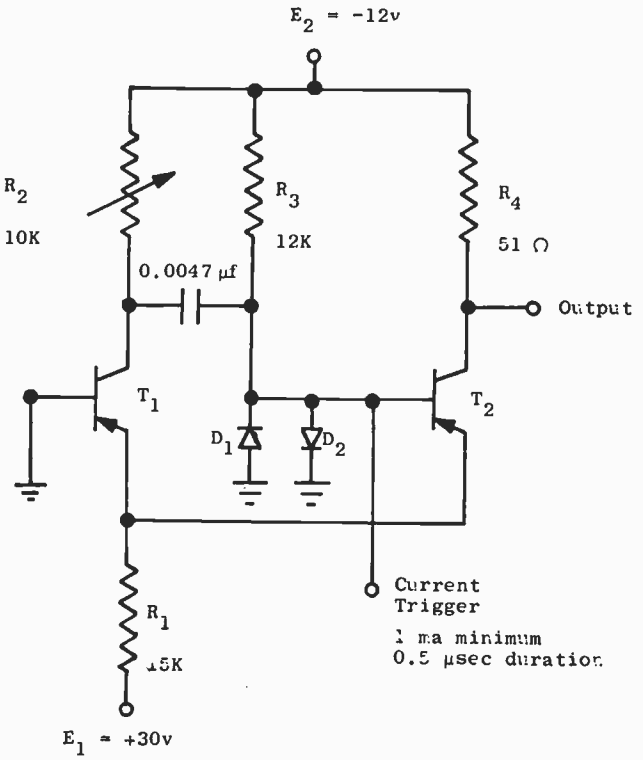


FIG. 1—Current switching monostable multivibrator uses two 1N266G silicon diodes and two 2N384 transistors.

The collector current in T_1 charges the capacitor and consequently the current builds up in R_2 at the expense of the current in the capacitor. When the current through the capacitor decreases to E_2/R_3, the base of T_2 is zero and is going negative, turning T_2 back on. The current in T_1 starts to decrease which causes the current in the capacitor to decrease more rapidly, causing even more current to flow through T_2. This regenerative action causes the common-emitter current to switch rapidly back to T_2.

With the values shown, the common emitter current is 2 ma and the current through R_3 is 1 ma. Thus, when the capacitor charging current falls to 1 ma, the circuit returns to its stable state. Then the time of the delay pulse is 0.69 R_2C. Delay times of 1 to 25 µsec result when R_2 is varied over its range, with the capacitor value shown. Longer delays may be obtained by using a larger value capacitor.

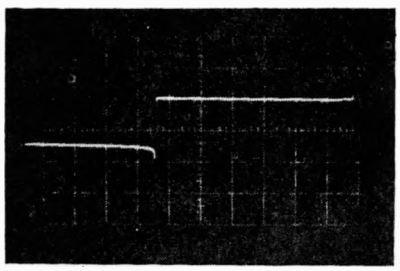


FIG. 2—Multivibrator output waveform.

The 51-ohm resistor in the collector of T_2 develops 0.1 v across it due to the 2-ma current. If a larger output voltage is required, it may be obtained by increasing the common emitter current or increasing the collector impedance. The particular value used is of a proper value to drive a coaxial cable. Figure 2 shows an oscilloscope trace of the output waveform. The particular waveform shown has a duration of 6.4 µsec and a rise time limited by the oscilloscope used. The actual rise time of the circuit is approximately 15 mµsec.

Current Switching Astable Multivibrator

A SIMPLE 10-mc pulse generator was recently required. Conventional saturating astable multivibrators were difficult to design at frequencies greater than 1 to 5 mc. The storage and switching times were great enough fractions of the half-period that the cross-coupling capacitors were discharged before the conducting transistors were turned off, and the circuits would not operate. Conventional methods of preventing saturation, such as shunting excess base current through the collector of the conducting transistor with a diode, were not attractive because of the extra parts required. The circuit which was finally developed uses a very simple principle to prevent saturation, and presented some extra advantages in addition.

The circuit, shown in Fig. 1, uses the principle of injecting a known current into the emitter of the transistor and clamping its base to a known voltage. Assume Q_1 is initially conducting and Q_2 is nonconducting. Capacitor C is being charged by current I so that the emitter voltage of Q_2 is decreasing. The base of Q_2 is clamped to a voltage determined by R_{c1}, R_b, and the collector current of Q_1. When the emitter voltage of Q_2 becomes low enough that

Q_2 begins to conduct current, the emitter current of Q_1 decreases, increasing the base voltage of Q_2, which turns off Q_1.

Now Q_2 is conducting, Q_1 is nonconducting, and current K_1I is charging C so that the emitter voltage of Q_1 is decreasing. Eventually Q_1 will begin to conduct again, the collector of Q_1 will decrease the base voltage of Q_2, and Q_2 will turn off. Now Q_1 is conducting, Q_2 is nonconducting, and the cycle will repeat.

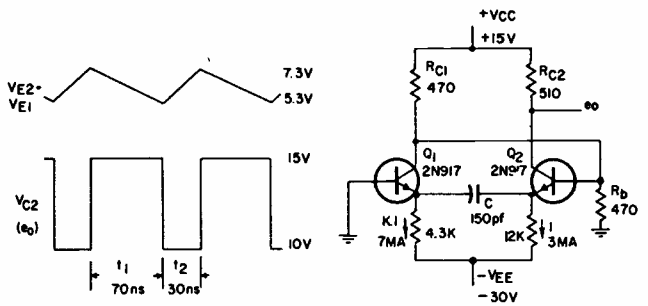


FIG. 1—Current switching astable multivibrator and its waveforms.

The following equations are easily derived once the operation is understood:

$$R_{c1} = \frac{V_{cc} - (1+k_2)\,V_{cb}}{(1+k_1)\,I}$$

$$C = \frac{k_1\,I}{(1+k_1)\,f\Delta V}$$

(When switching time is small fraction of $1/f$)

$$\Delta V = R_{c1}\,I\,\frac{1+k_1}{1+k_2} - 2\,(V_{be} - V_j)$$

$$e_o = \Delta V_{c2} = R_{c2}\,I\,(1+k_1)$$

where $k_1 = t_1\,t_2$; t_1 = time Q_1 conducts; t_2 = time Q_2 conducts; $k_2 = R_{c1}/R_b$ = degree of freedom in choosing parameters; V_{cb} = reverse bias on collector-base junction of Q_1 when Q_1 conducts; ΔV = change in voltage across C during half-period; V_{be} = base-emitter voltage of Q_1 or Q_2 when conducting; V_j = base-emitter voltage of Q_1 or Q_2 just before conducting, and f = frequency.

It is simple to pick values of V_{cc}, R_{c1}, and R_{c2} so that neither transistor saturates. The collector voltage rise time of neither transistor is limited by a cross-coupling capacitor, so the output is a good square wave. The frequency is more stable than that of the conventional multivibrator. If the equations for C and V are combined, it is seen that the frequency is approximately independent of V_{cc} and I, and is not sensitive to changes in V_{be} as is the conventional multivibrator.

Only one capacitor is required. At low and medium frequencies the capacitor is the largest component in the circuit, so this circuit will be smaller. Polarized capacitors may be used if extremely low frequencies are desired, since the emitter voltage of Q_2 is always positive with respect to the emitter voltage of Q_1.

Current Fall Time Control

IN MANY memory circuits such as inhibit drivers, word drivers, etc., the load for the output transistor consists of a series RL circuit to a supply voltage. The rise time in such a circuit is therefore 2.2 L/R measured from 10 to 90 per cent. Timing allowance is made for this rather slow transient.

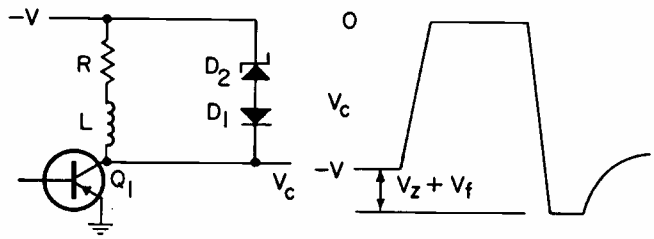


Fig. 1—Circuit with controlled fall time.

To protect the transistor at turn-off from the energy stored in the inductance, a diode clamp is generally used between the collector and the supply voltage. The fall time is therefore only slightly faster than the rise time, speeded up only by the help from the added forward voltage of the diode.

When the inductance is appreciable, as in an inhibit winding for a coincident current memory, the fall time is so long that it limits the memory cycle time, adding dead time before a subsequent read operation may be performed. It was found desirable to have a faster fall time than rise time, which was realized conveniently by the circuit of Fig. 1.

In the circuit, diode D_2 is a zener diode and diode D_1 is conventional to prevent forward current in D_2. When transistor Q_1 is turned on, the current rise time is 2.2 L/R as before. When the transistor is turned off, the collector is clamped to a voltage consisting of the sum of the series zener voltage and forward voltage of diode D_1, superimposed on supply voltage V. The fall time from 100 per cent to O is calculated from the equation $t_f = L/R\,[ln\ (k/k-1)]$ where $k = (V_{zener} + V_{f(D_1)} + V)/V$; $k > 1$

An advantage of this circuit, in addition to the faster fall time, is the fact that there is a sharp break at zero current rather than the exponential decay toward zero of a simple diode clamp; the sharpness of the zero current point is a result of an exponential decay toward a negative current equal to $(V_z + V_f)/R$ but cut off at zero when the diodes stop conducting.

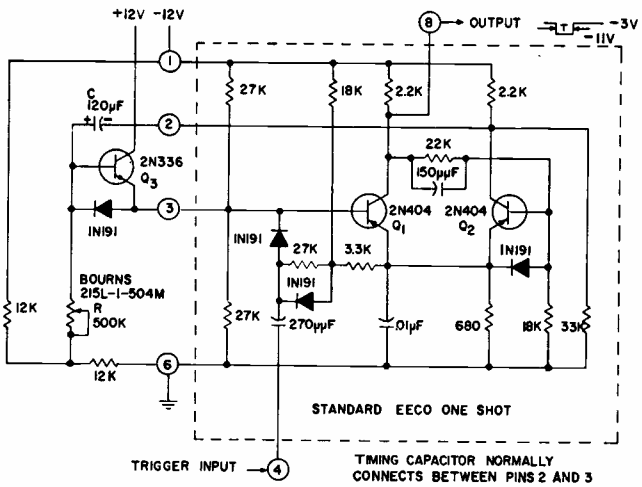
In the application for which the circuit was de-

signed, the fall time was decreased from 0.80 microsecond to 0.32 microsecond. For this application V was 20; R, 73 ohms; D_2, 1N764: D_1, 1N690; and Q_1, 2N1384.

Variable One-Shot for Counter Display Time

A VARIABLE pulse width of up to one-minute duration was required to control the display time of a digital counter. A standard one-shot multivibrator was modified by inserting in the timing capacitor feedback path a high-gain low-leakage silicon transistor for high input impedance. This allowed the use of a smaller capacitor than would otherwise have been required, and the use of a variable resistor which could be made large without being appreciably influenced by the temperature dependent parameters (leakage and current gain) of the transistors.

With a 500K-ohm potentiometer R and a 120-μf capacitor C, the output pulse width at pin 8 is variable from 1 second to 1 minute. Stability is very good over moderate temperature and supply voltage variations.



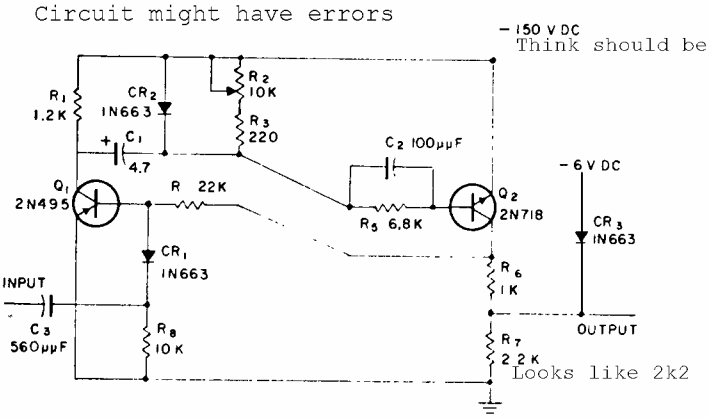
Output pulse width of one-shot mv is variable from one second to one minute.

The voltage level at pin 8 is normally —3 volts. Upon application of a positive input pulse, transistor Q_1 is turned off and Q_2 is turned on; pin 8 swings to —11 volts and pin 2 swings from —11 volts to —3 volts. Capacitor C couples an 8-volt positive pulse to the base of Q_3 which is initially at —3 volts. The emitter of Q_3 (pin 3) then swings from —3 volts to +5 volts and maintains Q_1 in the off state after the input positive pulse is gone. After C has discharged sufficiently to cause the emitter voltage of Q_3 to decay from +5 volts to —3 volts, Q_1 turns on and Q_2 turns off. The discharge slope at pin 3 is quite steep at —3 volts because the point is seeking —6 volts; thus, turn-on of Q_1 is sharply defined. The net result is a negative 8-volt pulse at pin 8 whose duration is determined almost completely by the values chosen for C and R.

Monostable 50-Millisecond Multivibrator

THIS complementary type 50-millisecond pulse width monostable multivibrator is designed to have both transistors in a nonconducting state until the circuit is triggered into operation with a negative going pulse of 2 volts or more. The introduction of such a pulse into the input causes Q_1 to be driven into saturation.

Circuit might have errors



Neither transistor of this monostable multivibrator conducts until an input pulse is applied.

Capacitor C_1 charges to —15 volts through R_2-R_3 and R_5-BE junction of Q_2, driving Q_2 into saturation. It also applies base drive to Q_1 thru R_4, holding Q_1 in a conducting state until C_1 has completed charging. Q_2 ceases to conduct and removes the base drive from Q_1. CR_2 functions as a discharge path for the charge on C_1 when Q_1 stops conduction, allowing the circuit to recover within 20 per cent of the pulse period. CR_3 is a clamp diode, for a 0 to —6-volt output pulse.

High Square, Variable Frequency Multivibrator

PREVIOUSLY PUBLISHED circuits for achieving improved rise and fall times in astable multivibrators have resorted to the use of additional transistors and voltage clamps with attendant cost increase and marginal improvement. The circuit described here combines fall time of 75 nanosec using inexpensive audio transistors and general purpose diodes with frequency range adjustment using a single control element.

The circuit requirements were for a frequency

range of 4 to 15 kc with a minimum squareness of 1500 at 4kc, which represented a fall time of 83 nanosec. This was to be done without resort to any exotic (i.e., relatively high priced) components.

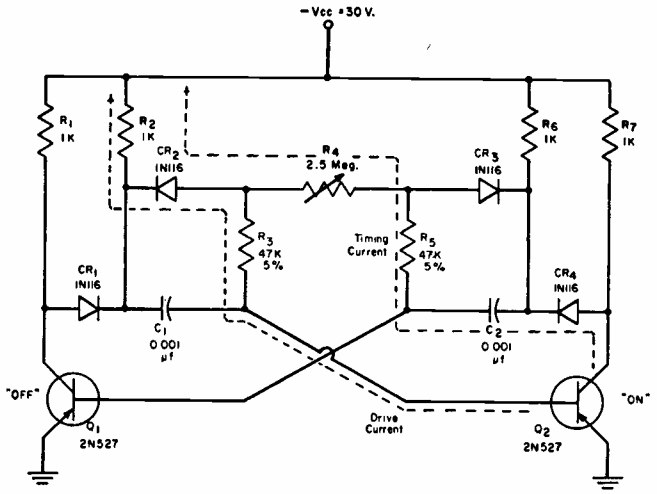


FIG. 1—Squareness of 1670 at 4 kc is provided by circuit composed of two audio transistors and four diodes.

Assume the situation in Fig. 1 of Q_2 in the on condition and Q_1 in the off condition. Collector load resistor R_7 is paralleled with R_6 since CR_4 is forward biased. Discharge current for C_2 flows through the series combination of R_2, R_4, and R_5. This is possible because with Q_2 on, CR_2 is forward biased with its cathode connected to a negative source through R_2. CR_3 is reverse biased since its cathode is essentially at ground potential.

When C_2 has completed discharging, the base-emitter junction of Q_1 will be forward biased, and the transistor will turn on. The collector of Q_1 will rise toward ground, forward biasing CR_1 and causing C_1 to discharge through Q_1. This will turn Q_2 off and reverse bias CR_4. Thus the collector voltage of Q_2 can approach V_{cc} as fast as the time consta of R_7 and the transistor diode capacitances will allow, since the charging current path for C_2 is now through R_6.

It should be noted that only the timing current flows through the variable frequency control R_4, preventing any change in bias condition. The duty cycle should remain reasonably constant provided R_3 and R_5 are matched within 5 per cent. Any high back resistance diode with low junction capacitance may be used for CR_1-CR_4. The diodes used here were low cost 60-v germanium units.

Should Q_1 and Q_2 attempt to simultaneously turn on, sufficient base drive can not be obtained through CR_2 and CR_3 for sustained operation, consequently both Q_1 and Q_2 will turn off. The circuit is self-starting.

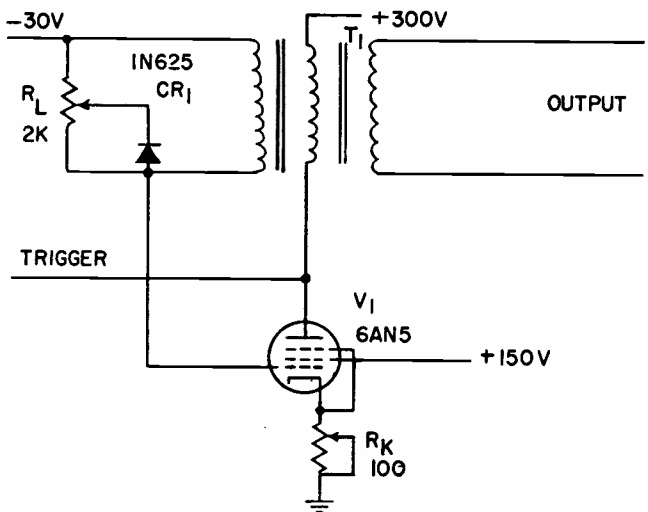
The circuit has a frequency range of 4 to 15 kc with adequate margin; the fall time is 75 nanosec, giving a squareness of 1670 at 4kc. The circuit requirements were met using two audio transistors. Four general purpose diodes and one resistor were the only additional components required over the number in a classical multivibrator.

Magnetic Control of Pulse Width

DESIGN ENGINEERS often have need for a reliable and simple linear pulse width control for use in equipment design or as test equipment in the laboratory. Such a requirement appeared on a product improvement program for a portable radar test set. Additional restrictions imposed on the device were light weight, small size, and low cost.

Several methods of obtaining the variable pulse were considered including a triggered monostable multivibrator and a variable delay line. The multivibrator was tried and abandoned because of its marginal operation with the short pulse widths and short rise times required. A variable delay line was considered and discarded due to physical size and mechanical problems.

The schematic shows the circuit configuration of the pulse width control selected as most economical and most reliable. Blocking oscillator transformer T_1 has a normal (unloaded) pulse width of about two microseconds which is narrowed as required by the adjustment of R_L and the rectifying action of CR_1 which introduces a dc component in the transformer winding and tends to saturate the core.



Pulse width can be varied over a range of four to one by adjusting the diode current.

Cathode resistor R_K is adjusted to compensate for manufacturing tolerances in blocking oscillator transformers and vacuum tubes. The circuit provides a pulse output with variable width over a range of four to one. It has been used for pulse durations in the one-microsecond range and will probably work for several hundred microseconds

depending on the transformer used.

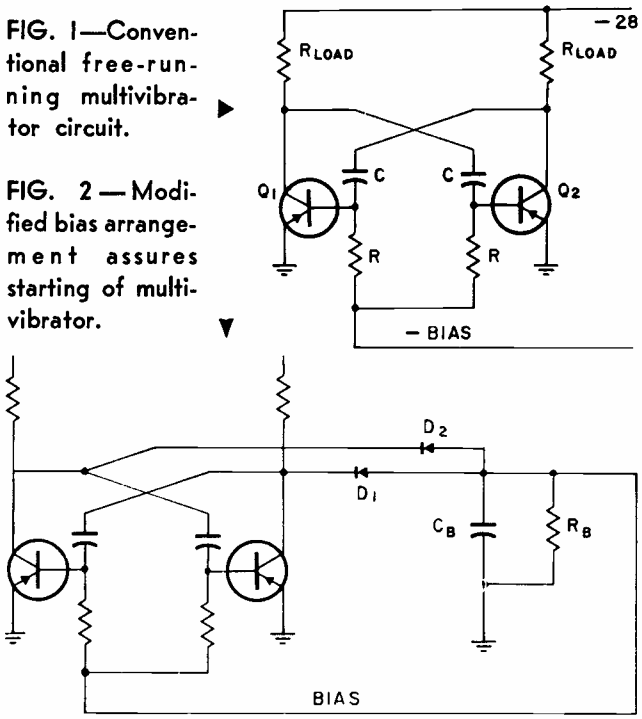
The concept is applicable to transistor blocking oscillators as well as vacuum tube circuits where wide range control of pulse width is required. Transistor circuits utilizing this principle have been built with good results.

Self-Starting Multivibrator

IN A CONVENTIONAL application of a free-running multivibrator, difficulty is often encountered in self-starting. The conventional multivibrator is shown in Fig. 1. On initial turn on, or if in use with test equipment, both capacitors are switched simultaneously, and conditions may arise in which both Q_1 and Q_2 will be fully conducting. (Amount of saturation is determined by R and the negative bias voltage.) With both Q_1 and Q_2 saturated, their incremental gain is low. Loop gain may not be sufficient to ensure oscillation.

FIG. 1—Conventional free-running multivibrator circuit. ▶

FIG. 2—Modified bias arrangement assures starting of multivibrator. ▼



A solution to this problem is shown in Fig. 2. The bias bus is derived from a full-wave rectifier circuit, D_1, D_2, R_B and C_B. If both Q_1 and Q_2 are drawing current, no bias voltage will be formed. Loop gain will be high enough to allow starting.

Noise-Free Pulser

A CONVENTIONAL transistor monostable multivibrator (Fig. 1) is very noise sensitive. The transistor is forward biased through resistor R_B. This resistor is usually picked to provide just enough current to saturate the transistor. This current is a function of the load resistor R_L and the beta of the transistor. A voltage swing at the input is transmitted through capacitor C to the base of the transistor, causing it to shut off. The pulse width is equal to $RC\ ln\ (V_{in} + 10)/10$. Unfortunately any voltage swing at the input can cause the transistor to shut off. Thus, a small noise pulse at the input can be amplified in the one shot.

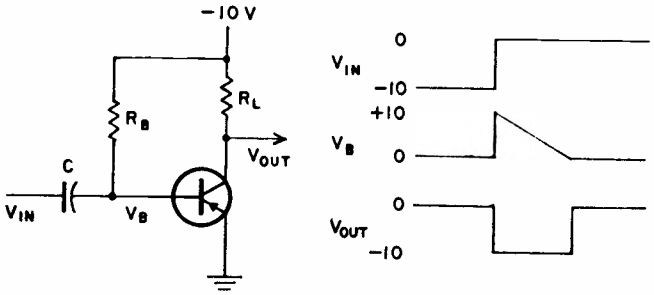


FIG. 1—Small noise pulses are amplified in a conventional multivibrator.

A desensitized monostable multivibrator is shown in Fig. 2.

During steady-state conditions V_2 is at —1.89 volts.

When an input voltage is applied to C, point V_1 rises. However, no "off" current is transmitted through diode D_1, until point V_1 rises more than 1.89 volts. Thus, the voltage at V_2 is that shown in Fig. 2. The peak swing is 1.89 volts less than that of the input signal. The pulse width is

$$T = RC\ ln\ (V_{in} + 8.1)/10$$

This is less than the pulse width of the original circuit but has one distinct advantage. No pulse output is generated unless the input voltage is greater than 1.89 volts. Some rejection of unwanted noise spikes has been obtained.

Diode D_2 is used to provide isolation between the input voltage and the voltage divider R_1, R_2. This diode also enables quick recharge of capacitor C when the input signal goes negative.

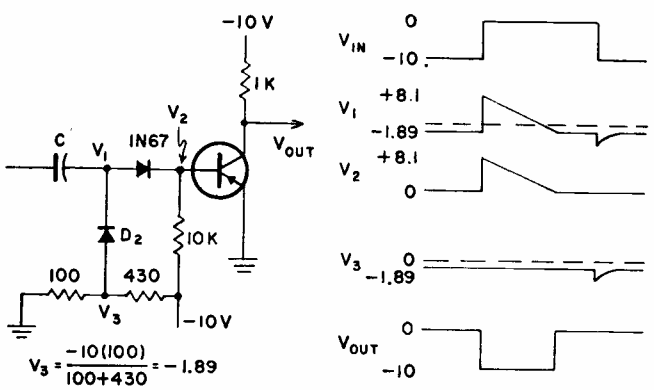


FIG. 2—Noise rejection provided by one diode in this circuit can be adjusted to a desired level.

Noise rejection is controlled by the voltage divider R_1, R_2. This can be set at any desired level.

The greater the noise rejection amplitude the less the pulse width, all other factors being equal. The circuit described was used with a 10-volt input swing.

Simple Intervalometer

MANY APPLICATIONS arise where a repetitive pulse train is required with wide tolerances in repetition rate and pulse duration allowed. The pulses may be used to actuate cameras, counters, stepping switches and similar devices. Figure 1 shows the circuit diagram of the intervalometer. The only components required are one relay, one capacitor, and two resistors. The circuit takes advantage of the fact that the pull-in voltage of a relay is higher than the drop-out voltage.

When a voltage V1 is applied, the voltage across the relay starts to rise at a rate determined by the R_1-C_1 time constant. When the pull-in voltage is reached, the relay energizes closing the control contacts. C_1 then begins to discharge through R_2 and the relay. When its drop-out voltage is reached, the relay reenergizes and the control contacts open. C_1 will again start rising and the cycle continues until V_1 is removed. The result is that the control contacts will open and close alternatively.

The repetition rate is determined by R_1 and C_1. Repetition rates from 0.1 to 20 pulses per second are practical. The pulse duration is determined by R_2, C_1 and the relay. Durations of 10 milliseconds to 5 seconds are feasible. Values shown are for a 28-volt pulse train with a repetition rate of approximately 5 pulses per second and a pulse duration of 50 msec.

Design values are chosen according to the best compromise in terms of keeping V_1 and C_1 relatively small and maintaining compatibility with the pulse requirements. V_1 must be high enough so that the voltage divider action of the relay, R_2 and R_1 will allow the relay to reach its pull-in voltage and allow the use of a relatively small capacitor for a given repetition rate. The pulse duration is limited by the size of C_1 and the relay resistance.

For variable repetition rates and pulse durations, potentiometers may be used for R_1 and R_2.

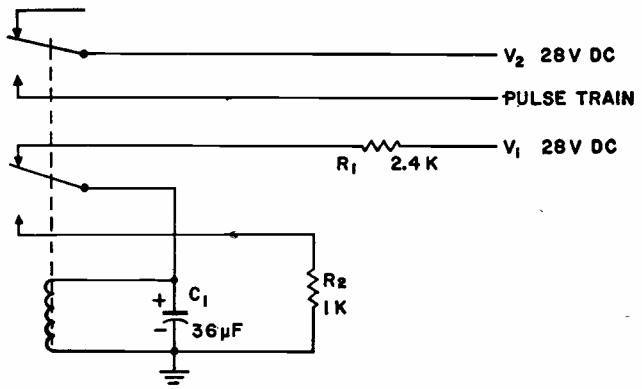


FIG. 1 — A Sigma 8000 G or equivalent is used in the intervalometer.

Free-Running Transistor Multivibrator

THE ORDINARY free-running multivibrator consists of two inverters cross ac coupled and biased on with resistance to a negative voltage. This circuit has the disadvantage of unreliable starting, since, if both transistors are saturated and in a quiescent state, the loop gain may be less than unity, and an external signal is required to start oscillation.

Reliable starting is frequently achieved by using a common emitter resistance which is made sufficiently large so that both transistors cannot be saturated simultaneously. Use of the common emitter resistance has the disadvantage that the output signal does not return to ground, and is therefore not compatible with other logic circuits without buffering or ac coupling.

If no emitter resistance is used, and the biasing resistors of the ordinary free-running multivibrator are returned to their respective collectors instead of a negative supply, as shown in Fig. 1, then the transistors cannot be saturated in the quiescent state and reliable starting is achieved. Furthermore the signal returns to ground, so that it may drive inverter stages directly.

The frequency is varied by changing either or

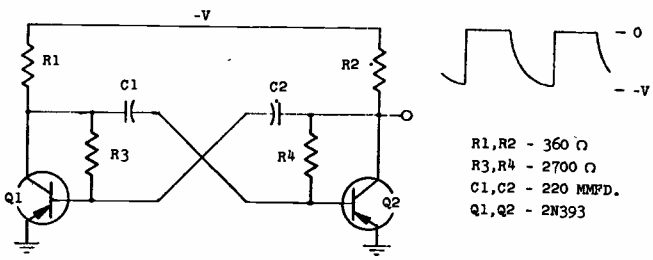


FIG. 1—Signal returns to ground in this free-running multivibrator circuit.

both of the capacitors, as in the conventional multivibrator. With the values shown, the frequency of oscillation is approximately one megacycle. The corresponding waveform is shown. Any supply voltage not exceeding the transistor rating may be used.

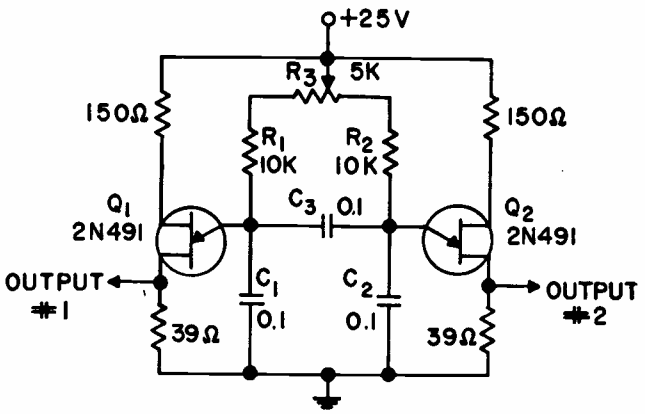
SCR Parallel Inverters in Correct Timing Sequence

FOR APPLICATIONS such as triggering silicon controlled rectifier parallel inverters, a pulse generator is required which produces high energy pulses alternately from two separate outputs. It is necessary that the pulses occur in the correct timing sequence from the instant that the supply voltage is switched on, otherwise the inverter circuit will fail.

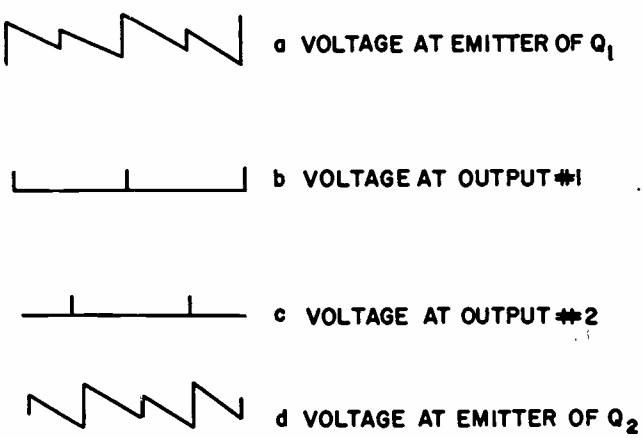
The unijunction transistors in the circuit shown

will generate pulses alternately from outputs 1 and 2 and will start in the correct timing sequence when the supply voltage is applied. This circuit consists of two relaxation oscillators which are synchronized by capacitor C_3 connected between the two emitters. This method of synchronization is unique and depends on the nonlinear charging characteristics of capacitors C_1 and C_2.

Potentiometer R_3 is used to adjust the time interval between the pulses from the two outputs. The range over which this time interval may be varied is determined by the value of C_3 (the smaller the value of C_3, the greater the possible range of the time interval). In the circuit as shown, synchroniza-



Double-output pulse generator consists of two relaxation oscillators synchronized by capacitance.



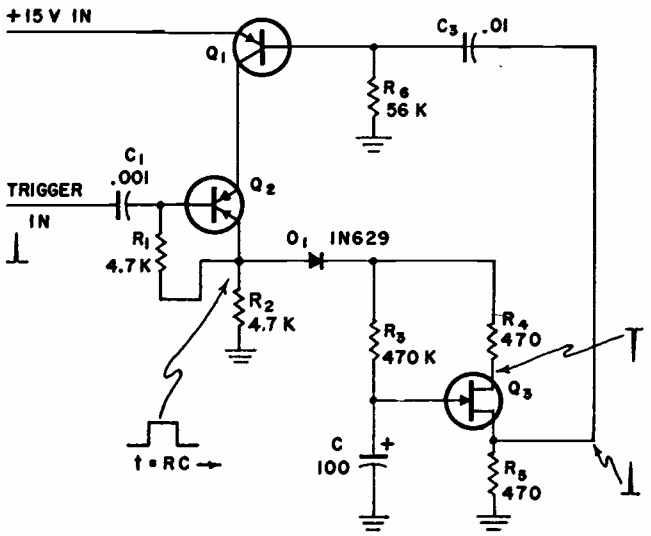
SCALE: VERTICAL—VOLTAGE (5 VOLTS/DIV.)
HORIZONTAL—TIME, RIGHT TO LEFT
(0.5 MS/DIV.)

Waveforms at emitters and outputs of scr parallel inverter.

tion is achieved with values of C_3, as low as 0.001 μf.

Negative pulse outputs can be obtained with this circuit by adding small values of resistance between ground and the lower ends of C_1 and C_2. This circuit can also be used in variable duty cycle power control circuits by adding a npn control transistor in shunt with C_1 or C_2.

Ultra-Long Monostable Multivibrator



Generator of long-time pulse draws no current while quiescent. Transistor Q_1 is a 2N1442, scr Q_2 a 2N1595 or 3A31, and unijunction Q_3 a 2N489.

THERE are three major disadvantages for the generation of a long-time pulse when employing the conventional monostable or one-shot multivibrator. One transistor stage is always turned on and thus draws current in the quiescent mode.

For the generation of a long-time pulse or gate, the designer is limited in his selection of the time constant in that for values above 100 K, a free-running mode may result under temperature variation. Therefore, his only choice is that of a higher value of C, which may be impracticable. He is also limited by loading effects which do not allow the time constant to approach the full value of RC.

For long-time generation, poor leading or trailing edges of the output gate are inherent when taken from either collector.

The circuit to be described has a quiescent power drain of zero. Because of the circuit isolation, high values of R (up to 1 megohm) may be used to achieve a long time generation.

The circuit generates a step function gate with good leading and trailing edges as well as providing a delayed pulse of either polarity (positive or negative going) which may be used for triggering cascaded circuits.

A conventional pnp transistor (Q_1) is normally in the on condition (forward bias of R_6) and thus is conducting and applies B+ to Q_2 (a silicon-controlled rectifier). Q_2 is in the off condition until a positive trigger pulse is applied to its base. Q_2 now conducts and the step voltage appearing across R_2 also energizes the unijunction circuit (Q_3) The capacitor starts charging and when the breakdown

voltage for Q_3 is reached, Q_3 fires giving positive and negative pulses. The positive pulse is coupled back to the base of Q_1 which drives Q_1 out of conduction thus opening up the B+ supply to Q_2. Q_2 thus is reset to the quiescent mode.

The values shown for R_3 and C_2 give a pulse duration of 50 seconds. The circuit has an accuracy of 8 per cent over a temperature range of +60 to —10 C and can easily be compensated for better accuracy.

Square Wave Chopper

IT IS OFTEN NECESSARY to generate asynchronous square waves with, or in between, regular system clock pulses. Some logical or analog functions may also require that this square wave be interrupted, or chopped, at certain specified times. If the square wave interruptions are accomplished directly by logical gating, the rise and fall times of the square waves will be increased. A circuit satisfying this criteria appears in Fig. 1. This circuit is used to generate unblanking signals without rise time deterioration. The result intensifies sine and cosine waves thus producing the type of

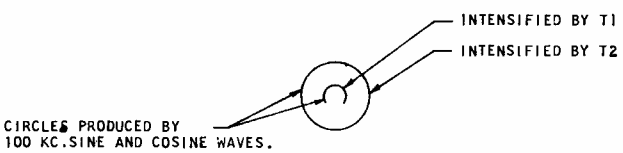


Fig. 1A. Circles produced by 100 Kc sine and cosine waves.

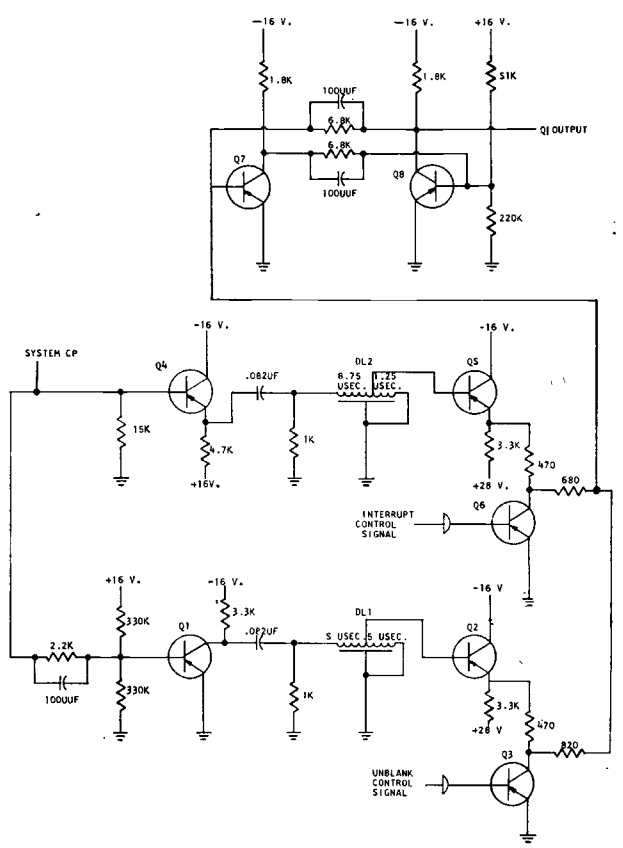


Fig. 1B. Transistorized circuit produces square wave output.

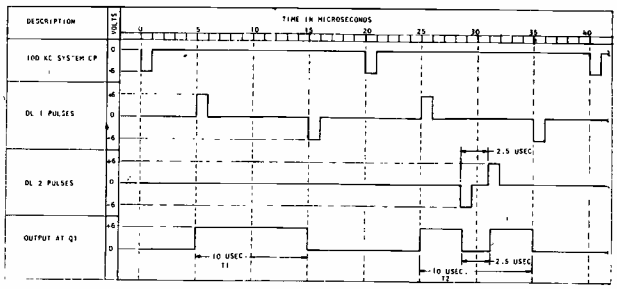


Fig. 2. Waveshaper for input and output of square wave chopper.

radar display console symbol illustrated in Fig. 1.

T_1 and T_2 represent the unblanked signals intensifies the larger and smaller symbol rings respectively. The interruption of T_2 causes the smaller symbol ring to open. The Circuitry which changes the sine and cosine wave amplitudes for the smaller symbol will not be discussed.

System clock pulses are applied to the bases of Q_1 and Q_4. Q_1 inverts the negative pulse and applies it to DL_1. DL_1 is a delay line with its output terminal shorted to ground. Assume DL_1 equals 10 μsec and is tapped at 5 μsec. The positive pulse will be transmitted through Q_2, and if Q_3 is back-biased, to the base of Q_7 in the flip-flop. Thus Q_7 will be turned off. Meanwhile, the positive pulse continued through the delay line until it reaches the shorted end. There the pulse is reflected with a polarity reversal, thus resetting the flip-flop.

If the interrupt control signal turns Q_6 off, additional pulses will be applied to the flip-flop. The negative pulse through Q_4 is not inverted and resets the flip-flop 3.75 μsec after the pulse passed through DL_1. The reflected pulse in DL_2 is positive and turns Q_7 off 2.5 μsec later. The interruption has now been completed, and the negative pulse from DL_1 resets the flip-flop.

Redundant MSMV Retrigger Any Time

A CIRCUIT DESIGN problem called for an extremely reliable msmv that could be retriggered at any time. The output pulse would then remain in the high state for a predetermined time. This means that if the trigger pulses are closer together than the time constant of the circuit a positive dc output will result. If the trigger pulses are further apart than the time constant, normal msmv action will take place and the output will be a pulse of fixed width.

The circuit in Fig. 1 is made up of four identical legs placed in a series-parallel configuration and can withstand any one component failure without loss or degradation of the output and up to three failures if they occur in the proper modes. The probability that the redundant configuration will operate successfully for one year is 0.99989. A corresponding nonredundant circuit has a probability of success for the same time interval of 0.9915. One hundred such redundant

circuits in series have a probability of success for one year of 0.989. One hundred nonredundant circuits would have a probability of success for one year of 0.43.

In describing the circuit, only one leg will be considered (Fig. 2). All legs work in the same manner and one leg could be used alone if redundant operation were not required.

Transistor Q_2 is normally in the saturated state. The potential at point A is approximately 1.3 v (two energy gaps above ground). When a positive going pulse appears at the input, it is differentiated and a positive

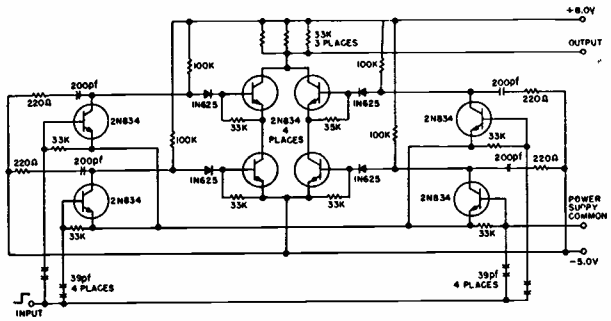


Fig. 1—Redundant msmv circuit.

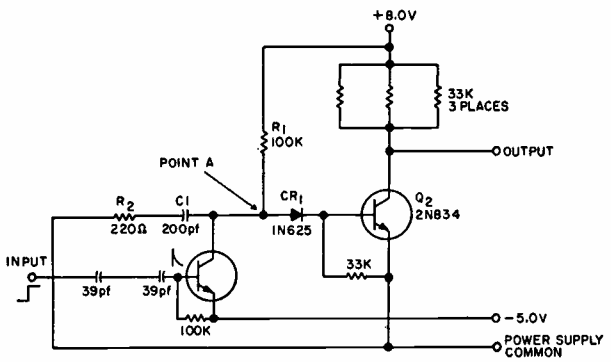


Fig. 2—One leg of circuit.

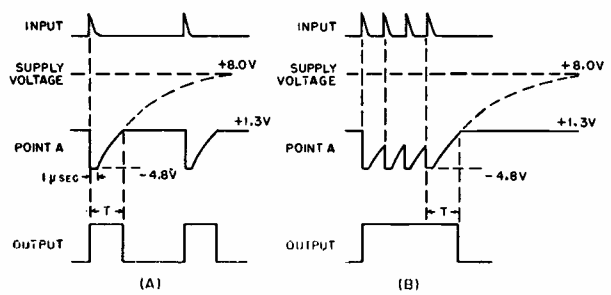


Fig. 3—Waveforms.

spike appears on the base of Q_1. Transistor Q_1 saturates and point A is pulled down to $-5v + V_{CE(SAT)}$ or about -4.8 v. This turns off Q_2.

Transistor Q_1 turns off, and the potential at point A begins to rise exponentially toward $+8.0$ v. When the potential at point A reaches 1.3 v, Q_2 again turns on and the cycle is complete.

The time constant is formed by R_1 and C_1. Resistor R_2 is small compared to R_1 and has negligible effect on the time constant. Resistor R_2 is placed in series with the capacitor to limit the maximum collector current of Q_1. Resistor R_1 must be small enough to supply enough base current to saturate Q_2. Transistor Q_2 must be a fast high beta device.

Diodes are inserted in the base circuits of the second transistors to insure that BV_{EBO} is not exceeded.

The equation for the output pulse width is easily derived if the waveforms shown in Fig. 3 are studied.

$$v = V_1 - (V_1 - V_2)\, e^{-t/R_1C_1}$$ (the exponential potential rise of point A)

$$e^{t/R_1C_1} = \frac{V_1 - V_2}{V - v}$$

$$t = R_1C_1 \ln \frac{V_1 - V_2}{V_1 - v}$$

Since Q_1 conducts for a finite amount of time (1 μsec) as shown in Fig. 3, this factor must be included in the calculation of the time constant. Also, since transistor Q_2 again conducts when v 1.3 v, this value should be substituted in the expression.

The equation for the period in μsec now becomes:

$$T = R_1C_1 \ln \frac{V_1 - V_2}{V_1 - 1.3} + 1$$

For the circuit shown:

$$V_1 = +8 \text{ v}$$
$$V_2 = -4.8 \text{ v}$$
$$T = 13.84 \approx 14 \text{ μsec}$$

The tolerance on the output pulse can be made as tight as desired by making R_1 and C_1 precision components and limiting voltage variations.

Tunnel Diode Trigger

IN MANY SATELLITE APPLICATIONS it is desirable to switch high-speed binary-counter stages using input voltages having unpredictable rise times.

The circuits of Fig. 1a and Fig. 2a are pulse-conditioning circuits. They accept input signals with rise times ranging from a slow-changing dc variation, to a steep pulse with a rise time of a fraction of a microsecond. From this wide input range, these circuits generate triggers that are suitable for switching high-speed binary-counter stages. Two variations of the pulse-conditioning circuit are shown. Both are for positive going input signals, but Fig. 1a shows the design for a negative-supply at the binary stage. In both diagrams Q_1 and Q_2 are silicon transistors, and the 1N2939 tunnel diode is of germanium. Both circuits have operated satisfactorily over the temperature range of -50 to $+100$ C.

Circuit operation hinges on the presence of the 1N2939 tunnel diode in series with Q_1, and the bias arrangement at Q_2. In Fig. 1a, Q_1 is cut off in the steady-stage condition, and Q_2 is conducting as an emitter-follower stage. Base current from Q_2 flows in the reverse direction through the tunnel diode. The collector of Q_2 is at 2.5 v positive. When the input signal voltage applied to the base of Q_1 (Fig. 1b) reaches approximately 2 v, the emitter current of Q_1 rises to about 1 ma. The peak current of the tunnel diode is 1 ma; therefore, when the input reaches the 2 v level, the tunnel diode will instantaneously switch to the high voltage state. This produces a positive step

voltage of about 0.5 v across the terminals of the diode (Fig. 1c). The rise time of the step voltage is steep enough to drive a high-speed binary-counter stage, but the amplitude is too small for reliable triggering. The step-voltage is, therefore, applied to the base of Q_2, which in the steady-state condition is operating as an emitter-following biased on. When the step voltage is applied to the base of Q_2, the base voltage rises immediately, but the capacitor across the emitter resistor of Q_2 prevents the emitter dc voltage from instantaneously following the base. Q_2 then acts as a grounded-emitter amplifier. The transistor saturates, and the collector goes to near ground potential (Fig. 1d), thus providing sufficient voltage swing at the junction of the 1N252 diodes to switch the state of the binary-counter stage.

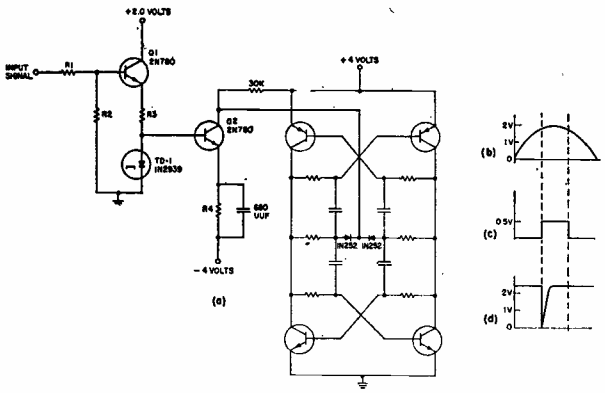


Fig. 1.
(a) Pulse conditioning circuit with positive supply.
(b) Input signal.
(c) Output at diode terminals.
(d) Transistor output.

The circuit of Fig. 2a has the tunnel diode placed in the collector circuit of Q_1. Because this circuit is designed for use with binary stages of negative supply voltage, the tunnel diode must be in the collector circuit to produce the proper polarity step voltage when Q_1 conducts. Q_2 is a PNP transistor with a positive emitter supply. The pulse produced at the collector is positive which is the correct polarity to switch the negative voltage supply binary-counter stage. Figs. 2b, 2c, and 2d show waveform data analogous to that shown in Fig. 1.

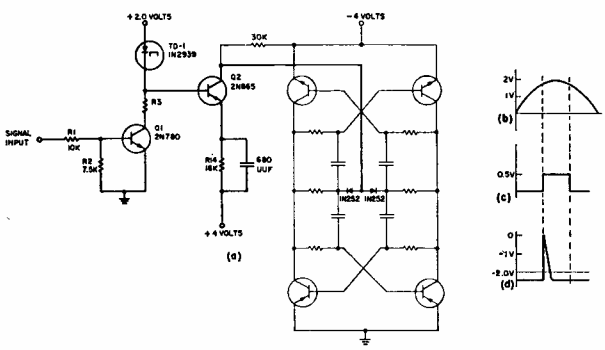


Fig. 2
(a) Pulse conditioning circuit with negative supply.
(b) Input signal.
(c) Output at diode terminals.
(d) Transistor output.

Fast Turnoff Monostable Multivibrator

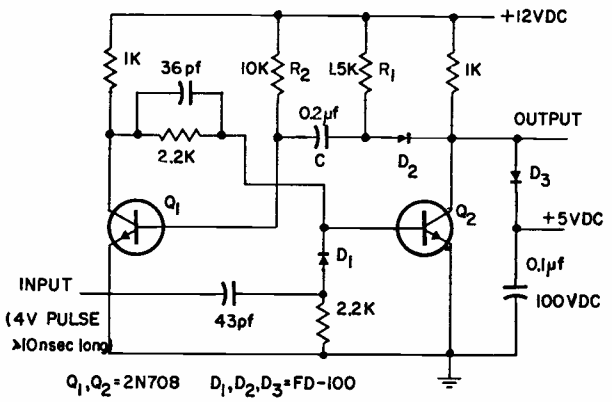


FIG. 1—Monostable multivibrator circuit designed for fast turnoff.

A CIRCUIT of a monostable multivibrator with a long delay time and yet fast rise and fall times is shown in Fig. 1.

In this circuit, diode D_2 decouples the charging capacitor, C, from the transistor Q_2, allowing it to recover rapidly. Capacitor C is charged by resistor R_1. The monostable pulse width, $\tau_{PW} \cong R_2C$, which in this circuit is 1 millisecond. The unloaded rise and fall times are each 30 nanoseconds. Pulse amplitude is clamped at 5 volts.

Positive Pulser

A SIMPLE CIRCUIT which produces a positive output pulse on both the leading and lagging edges of an input pulse should find many applications. Such a circuit is shown in Fig. 1.

With the input at ground, Q will be off and the

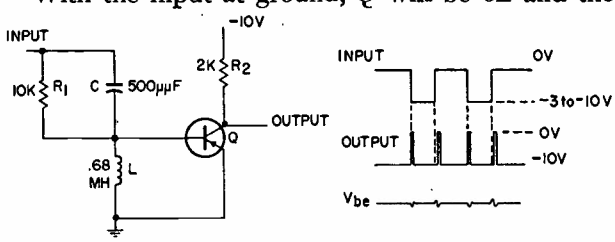


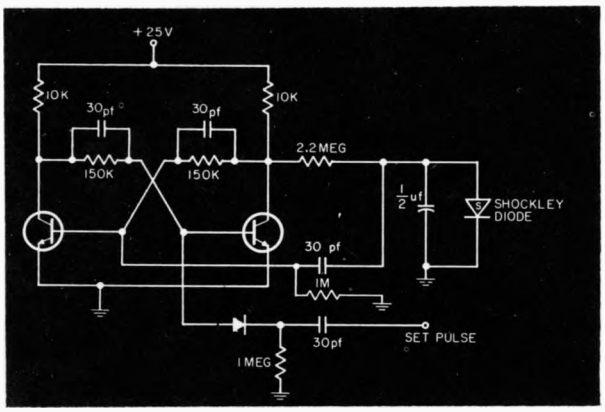
FIG. 1—This circuit produces a positive pulse for every transition of the square wave input.

output will be at approximately −10 volts. When the input is negative, R_1 and L provide a dc path which clamps the base of Q to ground, therefore the output is again at −10 volts. During the leading or lagging edge of the input waveform, the RLC circuit will resonate producing a positive and negative going waveform at the base of Q. The negative portion of this waveform will drive Q into saturation and the output will switch to ground. The result, then, is a positive output pulse, ten volts in amplitude, for every transition of the input waveform.

An analysis of the unloaded *RLC* circuit shows that the voltage developed across the inductor will be an underdamped oscillation for a step function input when $1/LC - 1/(2R_1C)^2 > 0$. A figure for *LC* may thus be obtained by using this expression. Any reasonable values of *L* and *C*, giving the proper product, may be used. With the base of *Q* connected to the output of this *RLC* circuit only one negative oscillation will occur, since the low input impedance of *Q*, as it is driven into saturation, shunts *L*. Thus the base waveform appears as shown in Fig. 1.

With the component values shown, a ten-volt pulse is produced at the output for every transition of an input square wave greater than three volts in amplitude. The output pulse resulting from the positive rise of the input will be slightly delayed since the base waveform goes positive before it goes negative for a positive input transition. The output pulse width is a function of how hard *Q* is driven into saturation, and therefore is dependent on the input pulse amplitude and the type of transistor used.

High-Duty Cycle Monostable Multi



High-duty cycle monostable multi.

A CAPACITOR discharging through a Shockley diode can be used to quickly turn off a monostable multivibrator to make ready for the next pulse.

In the circuit shown, the set pulse causes the flip-flop to change state. This starts an exponential voltage rise across the 1/2-μf timing capacitor. When the timing voltage rises sufficiently, the Shockley diode, type 4E 20-8, breaks down, discharging the capacitor very rapidly. The negative discharge pulse is used to re-set the flip-flop through the 30-pf capacitor. The flip-flop then is ready for the next trigger pulse.

This method allows triggering within .25 μsec after termination of a 2-sec output pulse. ◆◆

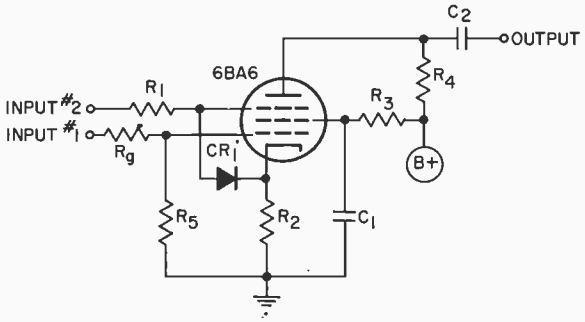
Electronic Chopper

THIS CIRCUIT can be used in all of the usual chopper applications; it was originally assembled for use as the first stage of a wide band (dc up to several kc) amplifier.

Input 1 is the signal to be amplified; R_g is optional and is for protection of V_1. Input 2 is a square wave of frequency several times (say 10) higher than the highest frequency of input 1. The high voltage supply must be very stable, as it is the reference, or zero level of the output; i.e., with no input at 1, $B+$ and $R_4\ I_p$ determine the output. R_4 is limited by the input impedance of the next stage. and the upper frequency limit desired.

R_1 and CR_1 insure that grid G_3, will not go positive, and make the input 2 amplitude requirements less severe. The transconductance of G_3 is apparently not very closely controlled, and a large amplitude square wave must be available if tube selection is not possible, as the square wave must cut off the tube. According to the manual, typical operation is characterized by $E_{Plate} = 100\text{ v} = E_{g2}$; $R_2 = 68$ (this may be increased to provide degeneration; 100 ohms was chosen for use); $I_{g2} = 4.0$ ma, $I_p = 10$ ma.

With a plate supply of 150 v, $R_4 = 150 - 100/10 \times 10^{-3} = 50/10 \times 10^{-3} = 5$ K. $R_3 = 150 - 100/4.4 = 50/4.4 = 13$ K. This may present a problem if the lowest frequency is dc, because this value cannot be bypassed. The μ of this tube is $(g_m\ r_2) = 0.25 \times 10^6 \times 4300 \times 10^{-6}$ is approximately $1/4 \times 4400$ or 1100. Since degeneration at the cathode for a given resistor is μ times that at the screen for the same resistor, an R_3 of 110 R_2 or 110 K will result in the same degeneration as will result from 100 ohms for R_2. For $R_3 = 13$ K, the equivalent $R_2 = 13 \times 10^3/1.1 \times 10^3$ or about 10 ohms. There is roughly 10 per cent degeneration at the screen for these values; if this



Electronic chopper

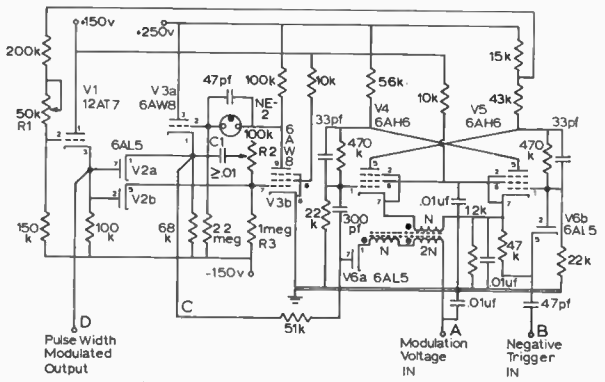
is too much distortion R_2 can be raised, although an adjustment of R_4 may be necessary.

C_1 is chosen on the basis of the lowest frequency to be amplified. If this frequency is very low, C_1 can be omitted subject to the discusion above. R_g and R_5 were arbitrarily chosen at 1 K and 1 M. R_1 depends on *CR*1. With a 1N34A diode, $R_1 = 15$ K is satisfactory although larger values are permissible. Depending on the end use of the signal, a filter to remove the square wave may be used. Further use of the basic circuit can be obtained by having the $B+$ controlled from some other source: this area was not investigated.

A Pulse Width Modulator

MOST PULSE WIDTH modulators are one of two types, the conventional voltage modulated monostable multivibrator, or the voltage controlled phantastron. Both suffer from the disadvantage that they cannot be modu-

lated over a very large range with tolerable linearity. The phantastron is the better of the two, but even at best it is only capable of a maximum pulse length to minimum pulse length ratio of 10:1, and with poor linearity. The circuit to be described is good for up to 350:1 ratio with nearly perfect linearity.



Pulse width modulator circuit.

The circuit works as follows. Tubes *V*4 and *V*5 comprise a bistable multivibrator. Initially *V*5 is conducting and *V*4 is cut off. A moduation voltage between zero and +175 v is applied at point *A*. Any time after this a negative trigger voltage is applied to point *B*. *V*5 cuts off, *V*4 conducts and the drop in *V*4 plate voltage is coupled, via cathode follower *V*1, to the disconnect diodes *V*2a and *V*2b. Thus, point *C* of the Miller integrator *V*3a and *V*3b starts to rise from zero volts dc at a linear rate. If unchecked it could rise to +175 v. V4, in addition to being part of a bistable multivibrator is also a cathode coupled blocking oscillator. That is, it would be a blocking oscillator except for the reversed biased diode, *V*6a, in its grid circuit. The cathode of this diode is connected, via the pulse transformer, to the modulation voltage. Its plate is being gradually raised towards the level of the modulation voltage by the miller integrator output. When the integrator output exceeds the modulation voltage the diode conducts, the blocking oscillator grid circuit is completed and the circuit delivers one pulse. This pulse flips the bistable. The plate of *V*4 then goes positive and turns on the disconnect diodes *V*2a and *V*2b, resetting the integrator in preparation for the next trigger pulse. Since the integrator output can only rise to the value of the modulation voltage before reset occurs the on period of the integrator is controlled by the modulation voltage and is directly proportional to same. The pulse width modulated output is shown at point D, but could also have been taken from either plate of the bistable.

The rate of rise of the miller integrator is determined by C_1, R_3, the voltage at the grid of *V*3b during the sweep, and the-150 v power supply; and equals, in volts per second, $\frac{144}{R_3\ C_1}$ Output pulse length then equals $\frac{R_3\ C_{1\cdot Emod\cdot}}{144}$. Keeping R_3 at 1M, the minimum value of C_1 works out empirically to be 0.01μf. This results in a maximum pulse length of 12.2 msec for a modulation voltage of +175 v, and a minimum pulse length of 70μsec for a modulation voltage of +1 v. With larger values of C_1 the dynamic range is better, and with C_1 equal to 0.05μf, the limits of modulation voltage are +175 v and +0.5 v for pulse lengths of 61 msec and 173μsec respectively.

R_1 adjusts the dc level of the waveform to the disconnect diodes and is used to set the base line of the sawtooth output at point *C* to zero volts during the quiescent condition of the circuit. R_2, a calibration adjustment, sets the value of an initial voltage step at the beginning of the sawtooth. This step may be positive, negative, or non-existent depending on the setting of R_2. To calibrate the circuit apply a modulation voltage of +100 v and provide a source of triggering voltage of at least 20 v peak to peak at a slow repetition rate. (The circuit has a maximum duty cycle of about 70 per cent.) Measure the output pulse length. Then decrease the modulation voltage to +1.0 v. Set R_2 to cause the output pulse length to be $\frac{1}{100}$ of the previously measured value. Repeat both steps once. The circuit will now accept any value of modulation voltage between +0.5 v and +175 v.

The bistable was necessarily designed to switch on very low values of trigger voltages. This insures the blocking oscillator-voltage comparator of working with only one output pulse from the blocking oscillator.

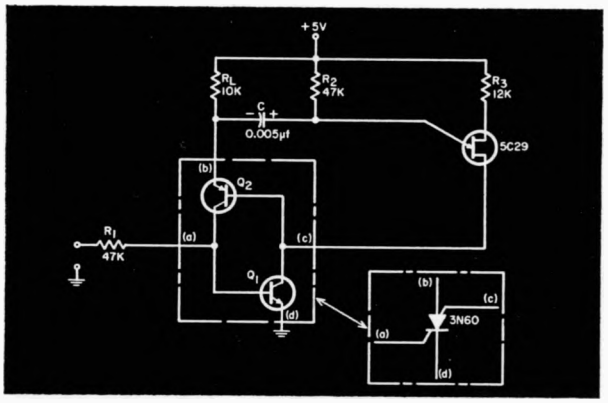
Self-Resetting Pulse Stretcher

THE PURPOSE of this circuit is to detect a 20-μsec, 5-v pulse or group of pulses and produce an output pulse which persists for a designated period of time after the last input pulse disappears. The circuit is self-resetting to its quiescent state and draws no current in the quiescent state.

The circuit is designed to be simple, and, with the exception of the charging capacitor, lends itself to microcircuit fabrication techniques.

In the circuit shown, an input pulse of at least 20-μsec width and 5-v amplitude turns Q_1 on, which in turn causes Q_2 to conduct thus locking Q_1 on, independent of the presence of an input pulse.

With Q_1 and Q_2 conducting, the output voltage drops to about 0.6 v and capacitor *C* charges toward the supply voltage through R_2. When the voltage at point *A* rises sufficiently, the unijunction is triggered on, supplying a positive turn-off pulse to the base of Q_2 which in turn causes Q_1 to



Self-resetting pulse stretcher. Gate turn-off SCR can be used instead of two transistors.

cease conducting, and the output voltage returns to its quiescent value.

In the final circuit, a gate turn-off SCR is used to replace Q_1 and Q_2, as shown.

The following are the test results for values shown:

Minimum Detectable Pulse Width	20 μsec
Minimum Detectable Pulse Amplitude	1.6 v
Turn-on Delay	0.6 μsec
Delay (C = 0.005 μf)	55 μsec
Maximum PRF	10 kc
Turn-off Fall Time	1.5 μ sec

A One Microsecond Delay

A CIRCUIT using four components can be constructed to deliver a good, solid pulse in the region of one microsecond. The circuit which is especially useful to a designer who needs a short pulse from a longer input is shown in Fig. 1. Output waveforms from positive and negative going input pulses are shown in Fig. 2.

Transistor Q is normally on and in saturation. During this time a quiescent output level of 0 v is provided. Any positive transient at the input is commutated through capacitor C and drives the base of the transistor positive, cutting it off. The transistor remains off with the output at $-V$ for a time determined by R and C. When the voltage at the base returns to approximately −0.1 v, the transistor once again conducts returning the output to 0 v.

Where the rise time of the positive going transient of the input is much less than the desired pulse widths, the output pulse width ≃0.7RC; slower rise times add to the pulse width.

Fig. 1

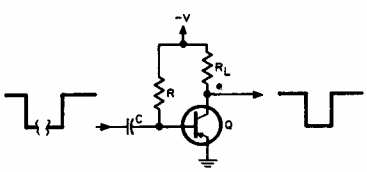
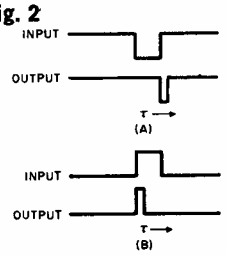


Fig. 2



Q = 2N396 R_L = 1K R = 10K C = 150 pf

Fig. 1. A delay of 1 μsec can be obtained with the circuit shown.

Fig. 2. Output waveforms compared with input signals.

Monostable Circuit with Negative Recovery Time

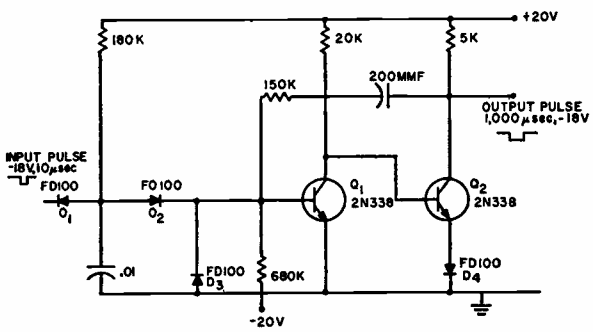
ONE DISADVANTAGE of most monostable pulse generating circuits is the fact that they have a finite recovery time. During this dead time following each output pulse, the typical circuit will not respond to an input trigger pulse. Hence, any input pulses which occur during the recovery period are lost. The circuit shown here completely overcomes this difficulty. It will respond to an input pulse immediately after the end of its output pulse. Moreover, it will also respond to input pulses which occur *before* the end of its output pulse. Thus, it may be said to have negative recovery time. For example, assume a trigger pulse is received and the circuit begins its normal 1000 μsec cycle. Suppose, then, that another trigger pulse is received after 500 μsec. In this case, the output pulse will last 1500 μsec, which is 500 μsec longer than usual. In general, the output pulse will continue until 1000 μsec after the last trigger pulse.

The operation of the circuit is straight forward. Under normal conditions the current through the 180 K resistor forward-biases Q_1 to saturation. Q_2 is hence biased at cutoff. The 0.01 capacitor is thus charged to about +1 v. The trigger pulse discharges the 0.01 capacitor down to about −17 v, thus turning off Q_1 and turning Q_2 on to saturation. Current through the 180 K resistor gradually recharges the 0.01 capacitor. After 1000 μsec the capacitor reaches normal +1 v, and the transistors revert to normal conditions. The 150 K resistor and 200 pf capacitor constitute a feedback network which insures that the output pulse will have fast rise and fall times. Diode D_1 prevents the 0.01 capacitor from being recharged by the input driving source. Diode D_2 protects the base-emitter junction of Q_1 from excessive reverse bias. Diode D_3 and the 680 K resistor provide stable cutoff bias for Q_1. Diode D_4 provides some bias to insure that Q_2 remains fully cutoff.

Several application precautions should be observed. One is that the input pulses should be of standardized voltage and of sufficient length to fully discharge the 0.01 capacitor. Otherwise, the length of the output pulse will vary as a function of trigger pulse duration and amplitude. Secondly, the output should be direct coupled; because, if the input prf is great enough, the output pulses will merge into a dc voltage.

The length of the output pulse may be made either longer or shorter by changing the 0.01 capacitor or the standard trigger pulse voltage. The length of the output pulse will be directly proportional to either of these. The base line of the trigger pulse should be slightly positive so as to reverse-bias diode D_1.

In general, this circuit may be regarded as a monostable multivibrator wherein the normally conducting transistor is determined by whether the diode, D_2, is forward or reverse biased.



Monostable circuit with less than zero recovery time.

Double Pulsed Sine Wave Circuit

IN MANY APPLICATIONS it is necessary to generate a pulsed sine wave signal. Other applications require generation of a pulsed sine wave signal that can be adjusted to either build up or die out in amplitude with succeeding sine wave cycles.

Figure 1 shows a double pulsed sine wave circuit of tremendous versatility. Output 1 of this circuit gives a pulsed fixed-frequency sine wave whose amplitude with succeeding sine wave cycles can be adjusted to either build up, die out or remain constant. Output 2 of this circuit gives a pulsed-variable frequency sine wave whose amplitude with succeeding sine wave cycles remains constant.

The portion of the circuit comprising Q_1 and Q_2 is a free-running multivibrator. The frequency of this free-running multivibrator is set by the circuit components to be approximately 333 cps. This multivibrator is unsymmetrical and the circuit components were selected to make one semiperiod of the circuit to be twice as long as the other semiperiod. Further adjustment on semiperiod duration is accomplished by adjustment of the 20-K pot.

The output of the multivibrator is fed through a coupling and speed up circuit to a transistor switch circuit whose emitter returns to ground through the parallel resonance tank circuit of a Colpitts type oscillator.

The operation of this portion of the circuit is as follows: During the semiperiod of the free-running multivibrator when the base of transistor Q_3 is made negative compared to its emitter, current flow in the emitter of transistor Q_3 passes through the parallel resonance circuit and prevents it from oscillating. During the other semiperiod of the free-running multivibrator, when the base of transistor Q_3 is not negative compared to its emitter, current does not flow in the emitter of transistor Q_3 and the tank circuit oscillates at its natural frequency.

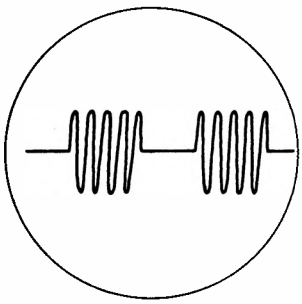


FIG. 2—Waveform of pulsed signal output when feedback is correct.

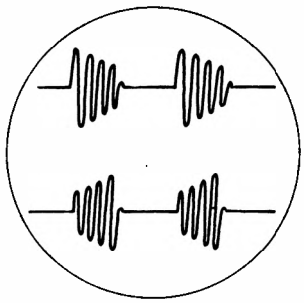


FIG. 3—Excessive or insufficient feedback produces waveforms shown.

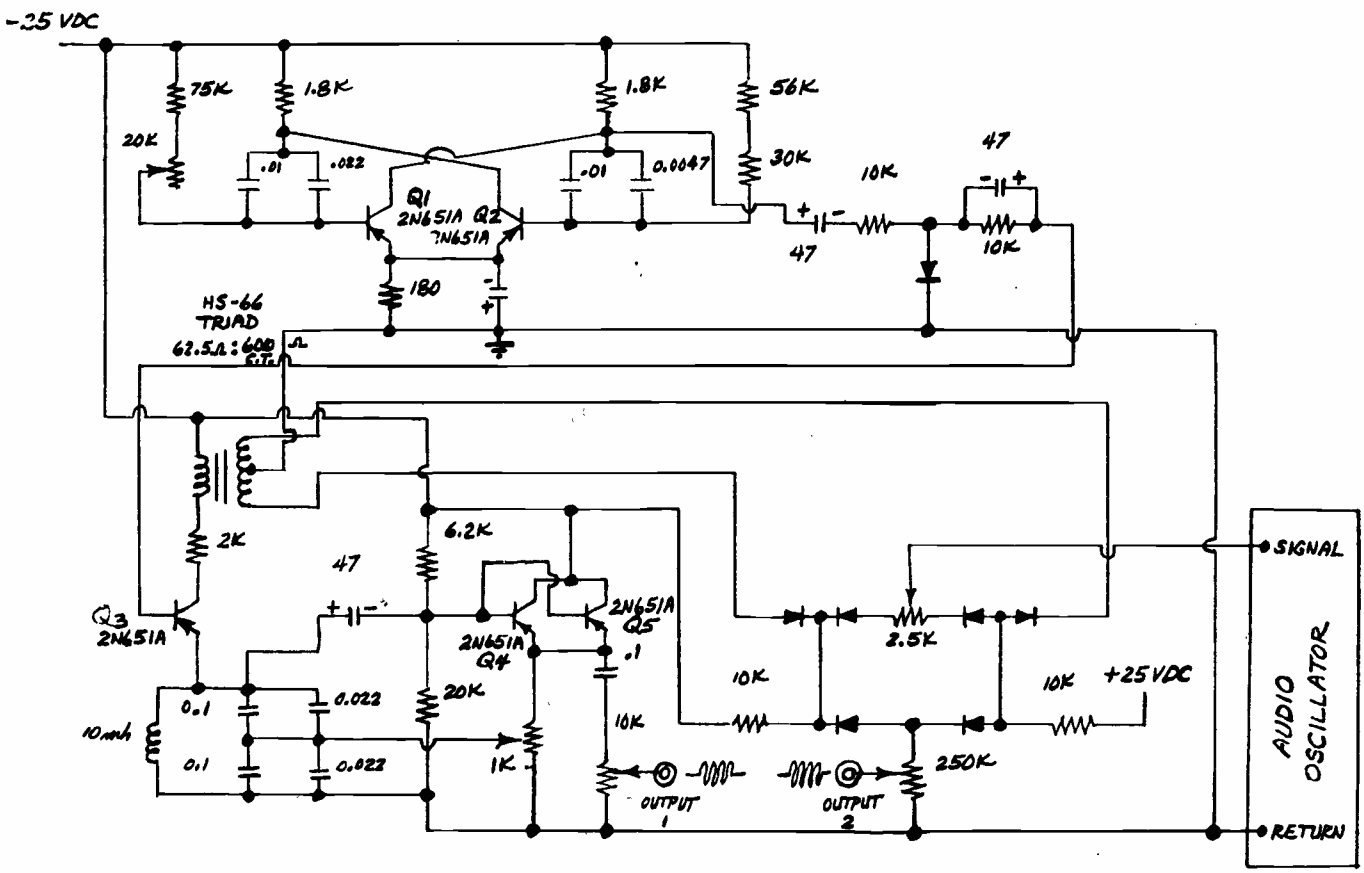


FIG. 1—All diodes are 1N645A and all transistors are Motorola 2N651A. Type 236S-1-203 Bourns Trimpot was used for the 20K pot at top left, 224S-1-252 for the 2.5K pot, and 224S-1-102 for the 1K pot at O

Feedback to the tank circuit is accomplished by adjustment of the 1-K pot. If the feedback is insufficient to sustain oscillations, the pulsed signal at Output 1 will slant downwards (as shown in Fig. 3) and appear to die out.

If the feedback to the tank circuit is more than enough to sustain oscillation, the pulsed signal at Output 1 will slant upwards (also in Fig. 3) and appear to build up. The pulsed signal at Output 1 will appear as shown in Fig 2 when the feedback to the tank circuit is exactly the proper amount to sustain oscillations. Circuit components in the Colpitts oscillator were chosen to make the resonance frequency 6.4 kilocycles per second.

The 10K pot in the emitter circuit of Q_5 adjusts the amplitude of the signal of Output 1 as desired. Transistors Q_4 and Q_5 were paralleled to get more current output. A single transistor with more current handling capability could be substituted for Q_4 and Q_5.

The transformer in the collector circuit of transistor Q_3 passes the semiperiod square waves that originated in the free-running multivibrator to act as control voltages for a six-diode gate. (Equations and explanation of operation of this six-diode gate are given in detail in "Pulse and Digital Circuits" by Millman and Taub pp 445-447.) The pulsed signal at Output 2 will appear as shown in Fig. 2. The sine wave frequency of the pulsed output signal can be selected as desired by the audio oscillator shown in Fig. 1. The 250K pot adjusts the amplitude of the signal of Output 2.

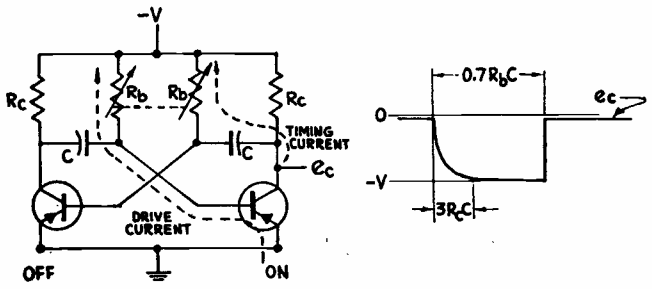
Wide-Range Constant Symmetry Multivibrator

OFTEN it is desired to have a square-wave signal source which is variable over a wide range of frequencies. Further, it is desirable that the symmetry, or duty cycle, of the wave remain constant. Conventional multivibrator circuits for accomplishing this suffer from limited frequency range, and the symmetry is dependent upon the tracking of two ganged potentiometers (see Fig. 1). Resistors R_b determine both the base drive in the on transistor and the rate of discharge of capacitor C, which is holding the other transistor off. The frequency range possible with this technique is limited by the range of base currents which will allow successful switching of the transistors.

A range of from 5 to 10 is about the limit of this method. Further, the squareness of the wave shape, that is the ratio of the half-period to the full-time is determined by:

$$\text{Sq.} = \text{Half-Period/Fall-Time}$$
$$= 0.7\ R_bC/3\ R_cC = 1/[4.3\,(R_b/R_c)\,]$$

But the maximum value of the ratio of R_b and R_c is determined by the dc beta of the transistors,



MULTIVIBRATOR CIRCUIT COLLECTOR WAVEFORM

FIG. 1—Classical multivibrator circuit and its output waveform.

that is:

$$\text{Sq.} = (R_b/R_c)/4.3 = dc\ beta/4.3$$

For present-day transistors, this means that the squareness is limited to about 10 to 20.

The conventional circuit suffers finally from one more point. If both transistors are on, the state is stable. That is to say, the circuit is not inherently self-starting.

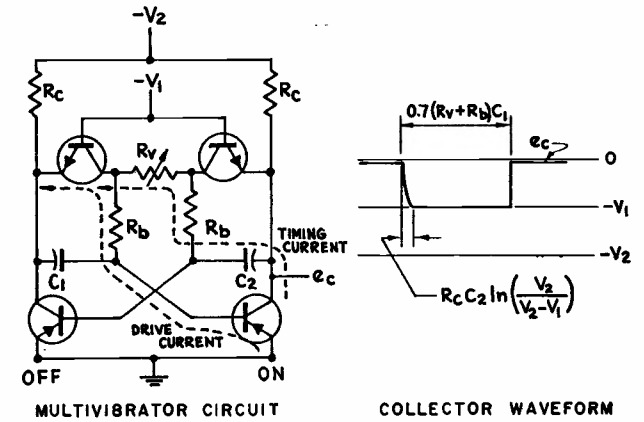
In the new circuit, Fig. 2, two pairs of transistors are employed, one pair of each polarity type. Base drive and timing current flow paths for a typical quasi-stable state are shown. Notice that the base drive to the on transistor is determined by a fixed resistor R_b, and that the discharge of capacitor C_1 is determined by $R_b + R_v$. The timing currents for the other quasi-stable state will also flow through R_v. The one resistor will determine the frequency, so the symmetry will remain essentially constant if the R_b resistors are a good match. No accurately tracking, ganged pots are necessary.

The period of the square-wave will increase linearly with R_v, which may be varied from a short-circuit to an open-circuit without upsetting the bias conditions of the transistors. When R_v is zero, the period will be determined by R_b; if R_v is made infinite, the period will be limited by the leakage of the circuit elements (in particular, by the I_{ebo} of the pnp transistors and I_{cbo} of the npn transistors).

The npn transistors will clamp the output wave at V_1, increasing its squareness by about two to four, depending on the ratio of V_1 and V_2. Further, the squareness is now limited by the ratio of R_v and R_c and can be made quite high. A squareness of 2-300 is readily attainable. (If this is not a high enough value of squareness, a resistor, R, of value $R = R_cV_1/(V_2—V_1)$ can be inserted in series with the capacitors. The fall-time of the circuit will them be independent of the capacitor recharge and depend on the transistor hole storage only. The author has attained square waves of two-three seconds duration with 30 μsec fall time . . . a squareness of 10^8.)

If both pnp transistors try to turn on, both npn transistors will turn off, turning off the pnp transistors. The circuit is inherently self-starting.

Since supply V_1 is used as a clamp, it is always receiving power, and any small battery can be used. Or, alternately, since the load to V_1 is constant, a



MULTIVIBRATOR CIRCUIT COLLECTOR WAVEFORM

FIG. 2—New mv circuit and its collector waveform.

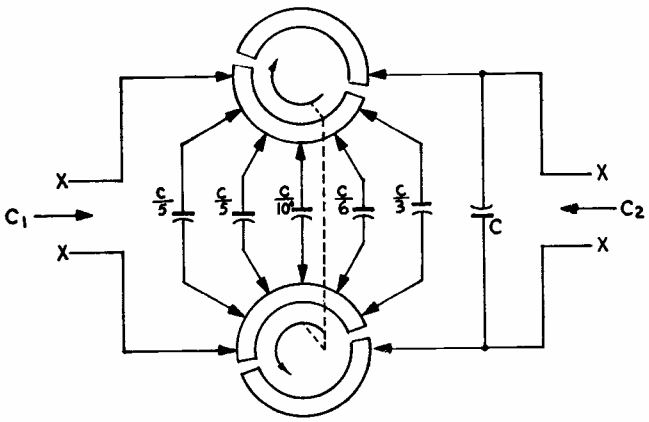


FIG. 3—Switching circuit to vary symmetry.

suitable resistor to ground bypassed with a capacitor can be used.

It is useful to be able to change symmetry on duty cycle without changing the frequency. This can be accomplished by using the switching circuit in Fig. 3 instead of C_1 and C_2. The values shown will give duty cycles of 50, 33-1/3, 25, 20, and 10 per cent.

The new circuit uses two more transistors than the classical approach but these more than earn their keep by providing fast fall-times, wide range with a single control element, and self-starting.

Pulse Generator for High-Speed Computers

IN SOME large high-speed computers, timing considerations make it prohibitive to propagate pulses from a central unit over long distances. These pulses, which are the basic timing signals of the computer, would be severely attenuated and distorted by the transmission line. The dc levels, on the other hand, may be propagated without serious deterioration, suffering only in the way of rise and fall times. For this reason, in a computer which requires high pulse repetition rates, it is sometimes necessary to transport a level over the distance and then convert to pulse form in the proximity of the recipient device.

To convert the level to a pulse, a transistor switch is turned off by the positive going wavefront, energizing a ringing circuit. To make the circuit operation independent of the level waveform, direct coupling is maintained at the input to the ringing stage. The input triggering of this stage is accomplished when a definite threshold level is exceeded. A pulse generator which performs the level-to-pulse conversion for a computer is shown in Fig. 1.

A pulse generator of this ringing type will be inherently prf sensitive. This sensitivity is seen by the degradation of the ringing amplitude as the frequency limit is reached. However, a positive biased emitter configuration will permit reliable, insensitive operation at frequencies well above that of a conventional grounded emitter circuit. For example, the circuit of Fig. 1 is capable of reliable operation for frequencies four times its grounded emitter capability. The increase in operating frequency is attributed to a larger inductor charging voltage, therefore, it will be shown that the input frequency limit is a function of e_L.

Assume the input of Q_1 is at its minus level, Q_1 is saturated, L_1 is fully charged, and D_1 is back-biased. The circuit will remain in this quiescent state until the input goes in a positive direction to cut off Q_1. When Q_1 goes active and toward cutoff, the collector current decreases causing the inductor field to collapse, and the familiar LC ring results. The initial ringing excursion is in the negative direction and is critically damped to zero volts by damping resistor R_5. This damping assures the generation of only one negative pulse for each positive transient at the input of Q_1. The output pulse width is dependent upon the values of L_1 and C_3 in the relation

$$PW = \pi\sqrt{L_1C_3}$$

Transistor Q_2 is always in dc cutoff. It is normally off while Q_1 is on and is held in cutoff by the forward drop of D_1 while Q_1 is off. It is desirable that D_1 have a low forward voltage to afford a better

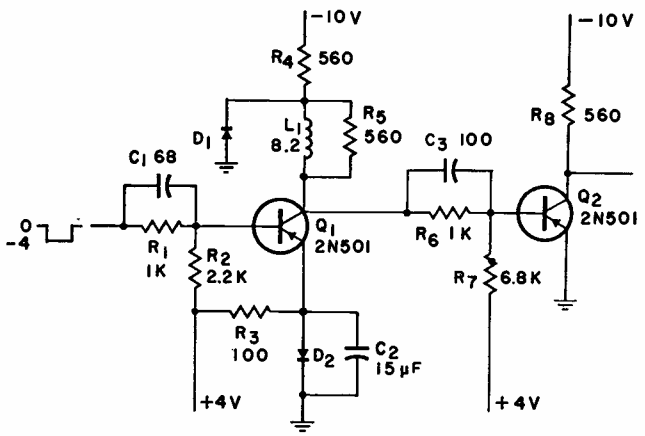


FIG. 1—Ringing type of pulse generator.

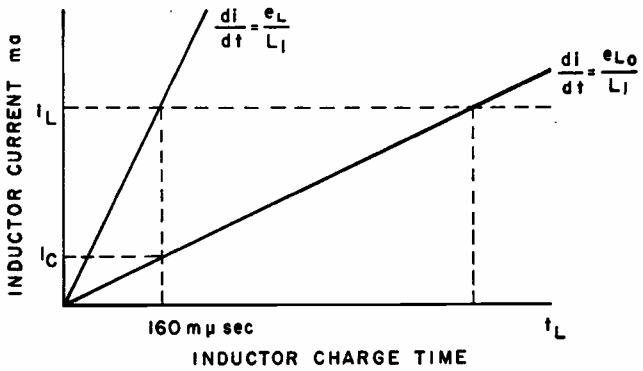


FIG. 2—Graph shows advantages of positive emitter circuit.

noise rejection at the base of Q_2. The base capacitor of Q_2 (C_3) will be driven by a pulse of amplitude.

$$v_p\, 2/\pi\, i_o \sqrt{L_1/C_3}$$

where i_o = the instantaneous inductor current when Q_1 comes out of saturation.

After the pulse is terminated, Q_1 will remain quiescently off until its base input goes negative, at which time D_1 is still conducting and L_1 begins to charge. Since the voltage across the inductor is

$$e_L = L_1\, di/dt,$$

the inductor will charge only during the time of changing collector current.

During this time D_1 is conducting and clamps the upper end of the inductor to the diode voltage V_f. If, then, the emitter is grounded, the voltage across the inductor is $e_{Lo} = V_f - V_{CE}$. Therefore, the value of e_L limits the charging rate of the inductor since $di/dt = e_{Lo}/L_1$. Consequently, if the input repetition rate is too fast, the circuit will be caused to ring before the quiescent collector current I_c is attained; and a less than standard voltage pulse results. To obtain the full pulse amplitude, the inductor must be allowed a charging time

$$t_L \geqslant I_c/di/dt \text{ or } t_L \geqslant I_c L_1/e_L$$

and since the input period T must be $T \geqslant 2t_L$ (50% duty cycle), then

$$T \geqslant 2I_c L_1/e_L$$

or

$$f \leqslant e_L/2I_c L_1.$$

Therefore, the dependence of the input frequency upon the inductor charging voltage is seen in this last expression.

To obtain a larger e_L, the emitter of Q_1 is raised above ground by a positive voltage reference using the stabistor D_2 (SG 22 or 1N816). The positive emitter voltage is limited by the stable off state of Q_1. The designer must effect a compromise between the maximum input frequency and the stable dc operation of the input circuit.

Figure 2 is a graph showing the relation between the inductor current and the inductor charging time for a grounded emitter and a positive referenced emitter for Q_1. The value of t_L at 160 mμsec on the graph is the inductor charge time required for the positive emitter case as given in Fig. 1.

Of the two co-ordinates on the graph, if first t_L = 160 mμsec is chosen as the starting point, note the serious reduction in current output for the grounded emitter case (e_{Lo}/L_1). Secondly, if we start with the collector current I_c, note the much larger charging time required, which limits the input repetition rate. Hence, the positive emitter circuit allows a four-to-one advantage over the grounded emitter configuration.

Results of bench tests verified the predictions as to the improvement in frequencies attained by the positive emitter versus the grounded emitter configurations with everything else unchanged. Input frequencies up to four mc were achieved with the positive emitter circuit while the same circuit with the emitter grounded became prf sensitive slightly above one mc.

Double Pulser

IN DIGITAL applications, it is often necessary to sense a change in state or to trigger a pulse on the leading and trailing edge of an input waveform (See Fig. 1). A simple one-transistor device to do this might be called a double pulser.

The circuit in Fig. 2 is essentially an amplifier

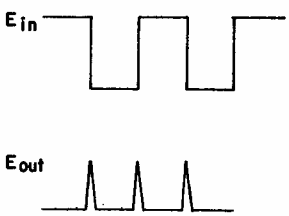


FIG. 1 — Two pulses form square wave.

with emitter resistor biasing. For small input voltages (negative with respect to ground for a pnp transistor), this is a linear network. An equivalent circuit for this amplifier is shown in Fig. 3.

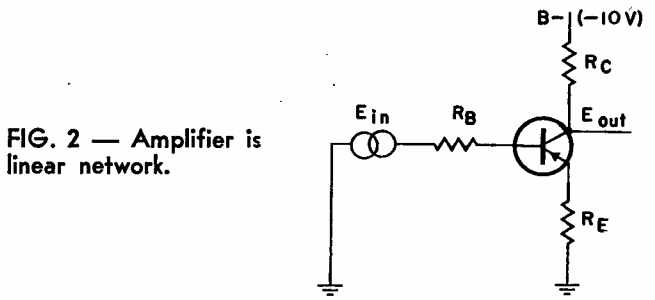


FIG. 2 — Amplifier is linear network.

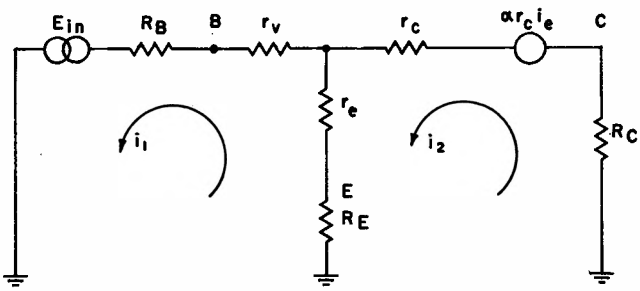


FIG. 3—Equivalent circuit showing current loops.

Assuming small signal linear analysis, we can find

the input impedance of this device.

Solving loop equations,

$$l_1 = [(E_{in}/R_B + r_b + r_e + R_E) - (r_e + R_E)\ (r_e + R_E - \alpha r_c)/ R_E + r_e + r_c\ (1-\alpha) + R_c]$$

The input impedance is given by:

$$l_1 = E_{in}/R_B + R_{in} \text{ or } R_{in} = E_{in}/l_1 - R_B$$

This is after combining terms:

$$R_{in} = r_b + (R_E + r_e)\ (r_c + R_c)/ R_E + r_e + R_c + r_c\ (1-\alpha)$$

assuming:

$r_c >> R_c$

$r_c\ (1-\alpha) >> R_c + r_e + R_E$

$R_E >> r_e$

we get:

$$R_{in} \sim r_b + (R_E + r_e)/(1-\alpha) \sim BR_E$$

This analysis is very approximate but it can give some idea of the circuit characteristics involved.

The current in the base is:

$$i_b = E_{in}/R_B + BR_E$$

Collector current is:

$$i_c = -BE_{in}/R_B + BR_E$$

Voltage out is:

$$E_{out} \simeq -10 - BE_{in}\ R_c/R_B + BR_E$$

$$\text{if } BR_E >> R_B$$

$$E_{out} \simeq -10 - E_{in}\ R_c/R_E$$

This is a very approximate relationship between E_{in} and E_{out}. It is a straight line over the linear region (Fig. 4—Curve 1).

The linear characteristic of this circuit breaks down when the transistor saturates. This occurs when: $|E_{in}| \geqslant |-10\ R_E/R_E + R_c|$

When the transistor saturates, it looks like a low-impedance passive device and the equivalent circuit is shown in Fig. 5.

$$E_{out} = [(E_{in}/R_B + -10/R_c)/(1/R_B + 1/R_E + 1/R_c)]$$

This is a straight line shown in Fig. 4—Curve 2.

The composite approximate E_{out} versus E_{in} characteristic of this circuit is shown as the crossed line in Fig. 4.

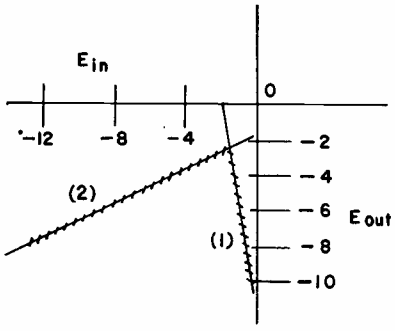


FIG. 4 — Approximate values of output versus input voltage.

Investigating this characteristic, when $E_{in} = 0$, E_{out} is —10v because the transistor is cut off. When E_{in} is very negative, E_{out} is also negative.

A practical example shows the use of this circuit. Let R_B be 100 ohms, R_c 5000 and R_E 1000.

$$V_{SAT} = -|10\ (1)^k/(1+5)^k| = -1.67 \text{ volts}$$

For the linear region $E_{out} \simeq -5\ E_{in} - 10$ and for the non-linear region $E_{out} = 0.975\ E_{in} - 1.95 \simeq E_{in} - 2$.

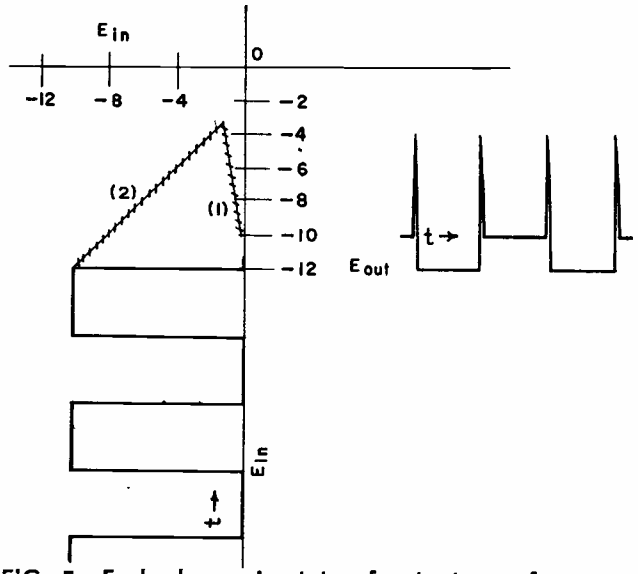


FIG. 5—Each change in state of output waveform provides a positive pulse.

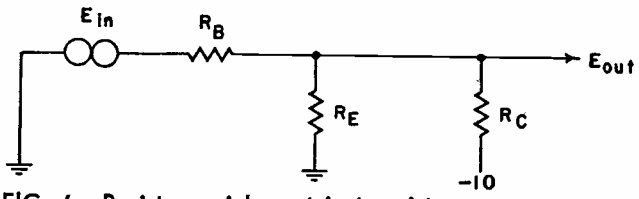


FIG. 6—Resistance inherent in transistor.

The characteristic is shown in Fig. 5. From this characteristic, for an input pulse going from 0 to —10 volts, the output will be negative for both of these states and will only go positive during the transition.

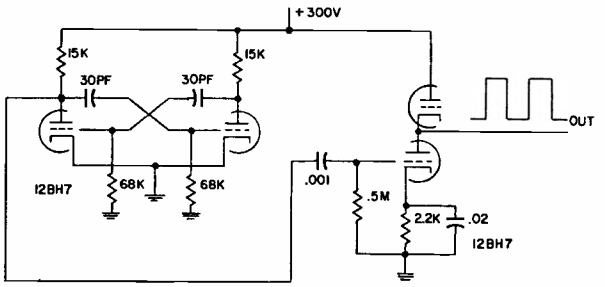
Therefore, we have a monostable device that nominally rests at —10 volts and produces a positive pulse every time the input waveform changes state (Fig. 5).

When this circuit was hooked up, results very much as predicted were attained. Hysteresis effects in the transistor causing unequal pulse amplitudes, and a slope less than unity for the saturated region were the main departures from the theoretical predictions. This latter occurrence is understandable when the transistor resistances involved, Fig. 6, are considered.

Low-Impedance Multivibrator Output Circuit

ADVANTAGE is taken of the push-pull feature of a multivibrator in the circuit shown to drive a stacked triode combination. This arrangement overcomes the usual disadvantage of an ordinary cathode follower which has unequal output impedances for fast rise and fall time signals.

In operation, starting with a positive-going signal out, the upper triode of the stack behaves



Stacked triodes provide constant output impedance.

as an ordinary cathode follower with an output impedance of approximately

$$[(r_p R_K) / (r_p + R_K)] R_K$$

Then R_K is the lower section resistance, and it is cut off by the negative-going signal from the multivibrator. This would make R_K very high and the output impedance is then r_p. On the next half cycle the upper triode would tend to be cut off and the lower triode grid driven positive, causing it to conduct. The output impedance is again r_p instead of R_K as in an ordinary cathode follower. The resulting output impedance is constant and very low, about 2000 ohms.

Blanking Pulse Generator With Linear Pulse Width Control

The circuit described provides a blanking signal starting with an input pulse and remaining on for some nominal portion of the pulse period regardless of drop outs due to noise in the triggering pulse. Information of the approximate input pulse frequency was obtainable from the rotational position of a shaft, the shaft position being linearly proportional to the frequency over each decade of a one cps to 10 kc range.

The functional elements of the circuit shown in Fig. 1 are transistors Q_1 and Q_2 forming a flip-flop, a dc level inverter comprised of zener diode D_3 and transistor Q_3, unijunction transistor Q_4 in a timing circuit, and transistor Q_5 pulse amplifier. Unijunction timing circuits operated in the manner shown, with transistor flip-flops, essentially form hybrid one-shot networks recognized for their excellent pulse shape and high duty cycle capability.

The stable state of the network when ready to recognize an input pulse has Q_1 and Q_2 collectors at 0 and −9 v respectively. With this condition, zener diode D_3 is in its low conductance region thereby providing no bias current to transistor Q_3. Q_3 collector is then at −10 v as is the emitter and base 1 terminals of unijunction Q_4. An input pulse causes Q_1 and Q_2 collector voltages to interchange value. The increased effective supply voltage to the zener diode now exceeds the zener potential of this device resulting in a heavy bias current which saturates Q_3. Capacitor C_5 starts charging

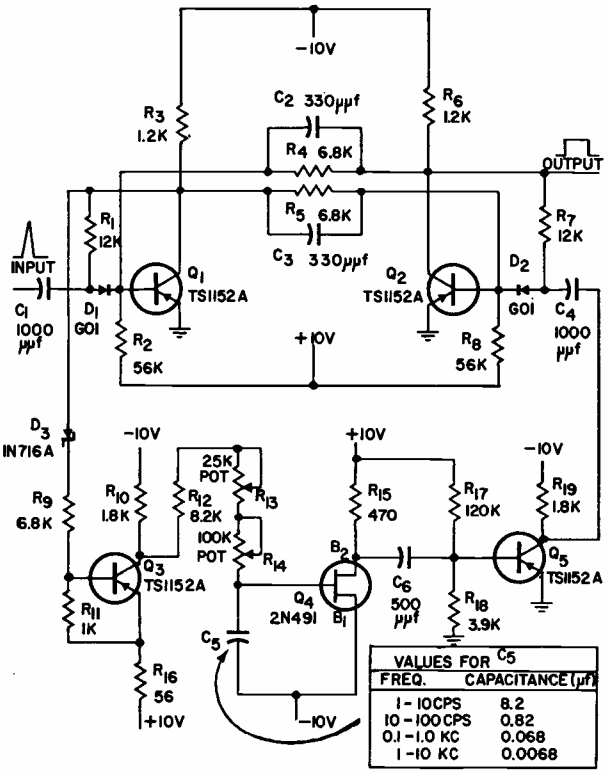


FIG. 1—Blanking pulse generator.

exponentially to the 10 v potential of Q_3 collector. When the capacitor charges to the peak point emitter voltage of the unijunction, a narrow negative pulse appearing at base 2 is amplified by Q_5. This latter pulse resets the flip-flop returning the network to its original state to await the arrival of a new input pulse.

A cycle of operation is initiated by the leading edge of a positive input pulse, setting the flip-flop. With the blanking pulse width exceeding the input pulse width, drop outs will have no effect since they would only attempt to cause set action to a flip-flop already in the set state.

In the particular application for which the circuit was designed, the input pulses had a maximum 50 percent duty cycle. The blanking pulse width was selected as 70 percent of the period of the input. Blanking period in the unijunction timing circuit is proportional to the product of R and C_5, where R is the sum of R_{12} and the unshunted portion of potentiometers R_{13} and R_{14}, these potentiometers being ganged to the shaft containing the input frequency information. Since the shaft position was directly proportional to frequency, and the blanking pulse had to be inversely proportional to frequency, it was necessary that R be inversely proportional to per-cent shaft rotation over 10:1 ranges of frequency. The proper variation of R with shaft position was obtained by using a 25K linear taper pot with clock-wise rotation in series with a 100K logarithmic taper pot of counter clock-wise rotation.

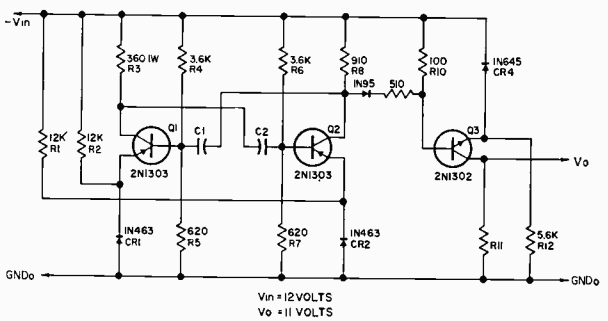
Very satisfactory results were obtained with this blanking pulse generator even when tested with a modulated cw signal to simulate a worst case

noise condition. The network demonstrated better than a 99 percent duty cycle capability over the entire frequency range. The choice of potentiometer tapers resulted in a maximum 5 percent tracking error from the nominal duty cycle selected.

Square Wave Generator with Variable On and Off Times

THIS SIMPLE SQUARE WAVE GENERATOR may be used to drive relays, flash lamps, drive computer gates, and other applications. Output is adjustable from 0.5 cps to 60 kc at currents up to 150 ma without appreciable waveform corner rounding.

The basic operation of the circuit is as follows: When current is first applied to the circuit, Q_1 begins to conduct, causing the potential of its collector to rise. This action charges capacitor, C_2, through resistor, R_6, which brings transistor, Q_2, into the cutoff state. With Q_2 cut off, its collector becomes more negative. Thus, a negative charge is placed across C_2, which speeds up the on time for Q_3. When the charge across C_2 is equal to 0.63 of the power supply voltage, C_2 discharges through the low impedance of Q_1 and the second half of the cycle begins. The circuit combinations of R_2, R_3 and CR_1, R_1, R_7 and CR_2 and R_{10}, R_{12} and CR_4 provide a reverse base drive, decreasing the turn-off time of Q_1, Q_2, and Q_3, respectively. CR_3 acts as a single and gate controlling amplifier Q_3.



Square wave generator for variable pulse widths and variable interval between pulses.

The calculations for C_1 and C_2 are:

$$C_1 = \frac{\Delta I_1 \, \Delta T_1}{(0.63)\, E} \; ; \quad C_2 = \frac{\Delta I_2 \, \Delta T_2}{(0.63)\, E}$$

where:

V = 11 volts

I_2 = Q_2 collector current = 0.0317 a

I_1 = Q_1 collector current = 0.0306 a

T_1 = Interval between pulses in sec.

T_2 = Pulse width in sec.

R_{11} is made equal to

$$R_{11} = \frac{V_o}{(0.15 - I_L)}$$

where

V_0 = 11 volts

0.15 = max. collector current of Q_3

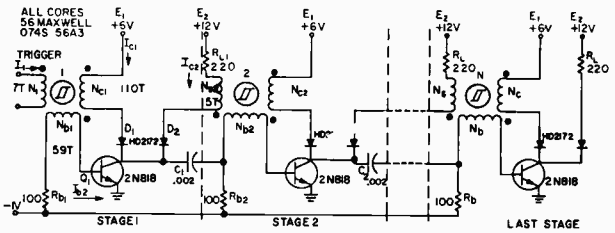
I_1 = load current

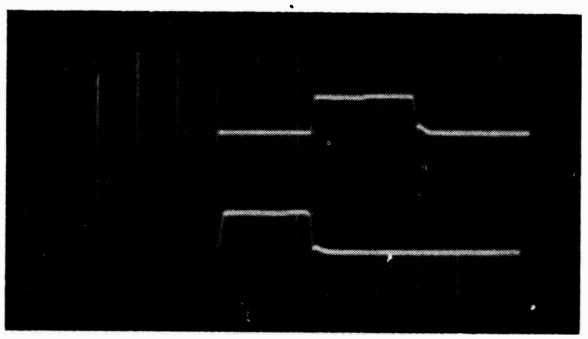
If a relay is connected directly across the output, it may be necessary to add a resistor in parallel with the coil. This reduces the inductive voltage created by the coil and prevents damage to the transistor.

Magnetic-Core Sequential Pulser

THIS CIRCUIT, when triggered, provides high power, electrically isolated, sequential pulses. The number of pulses is determined by the number of stages.

With core 1 in a "one" state and all other cores in a "zero" state, the trigger pulse (40 ma for 1 μsec) causes a regenerative action between N_{c1} *and* N_{b1}. Transistor Q1 saturates and a large current I_{c2} (output pulse) flows in the N_{S2} winding on core 2. I_{c2} sets core 2 to a "one" state. When the output of stage 1 falls to zero, C_1 charges through R_{L1}, D_2 and R_{b2}. The initial charging-current spike triggers stage 2. Stage 2 resets and its output sets core 3. This action continues for the number of stages used.





A single trigger pulse is transmitted from stage to stage, saturating each transistor and then turning the transistor off as the induced voltage drops to zero. Adjacent-stage outputs are shown (50 ma/div vert. and 5 μsec/div hor).

The output pulse width is determined by:

$$T_{sw} = \frac{N_c \phi}{E}$$

where T_{sw} = output pulse width or switching time of the core

N_c = number of turns in the collector winding

ϕ = switchable flux of the core

E = supply voltage (E_1) minus volt-

drops V_{ce} and V_{D1}

It is desirable to use a high voltage for E_2 so that the back emf, generated in N_{S2} when core 2 is set, will not distort the leading edge of the output pulse.

In order to minimize the number of turns required for N_c, E_1 must be small. These requirements are met by having two supply levels (E_1 and E_2). D_1 and D_2 prevent current flow between the supply levels. The output pulse amplitude can be varied by changing R_L.

The component values shown will generate a 11.5-μsec pulse. Stages using 123-maxwell cores have been used to obtain pulse widths of 40 μsec. By returning the last stage to the first, a ring counter (which would require no drive pulse) can be built.

Transient-Protection Of Monostable Multivibrators

THE SIMPLICITY and reliability of the monostable multivibrator makes it a logical choice for a multitude of timing applications. Unfortunately, its susceptibility to triggering as a result of power supply transients may severely restrict its practical use. The circuit shown in Fig. 1 is a monostable multivibrator which is totally insensitive to power supply transients.

To fully understand its operation, consider the mechanics of supply transient triggering. The coupling between the cut-off collector and saturated base is shown in Fig. 2A. Assuming the circuit in equilibrium, then the coupling capacitor, C_c, is charged to nearly

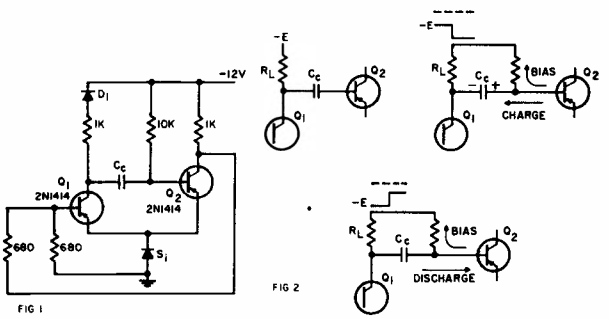


Fig. 1. A monostable multivibrator insensitive to power supply transients.

Fig. 2. (A) Coupling between the cut-off collector and base; (B) Step increase in supply voltage causes a charging current to flow; (C) Step decrease in supply voltage causes C_C to discharge through R_L and the base of the conducting transistor.

full supply voltage. A step increase in supply voltage will cause a charging current to flow, as shown in Fig. 2B, which aids the saturation bias. A step decrease in supply voltage will cause C_c to discharge through the load resistor R_L, and the base of the conducting transistor, as shown in Fig. 2C. The discharge current opposes the saturation bias and is approximately 1 ma/volt step for $R_L = 1$ K. In the majority of circuits this is more than sufficient to completely reverse bias the saturated transistor.

The addition of the diode in series with the cut-off collector load is the key to transient protection. Any step decrease in supply voltage will cause the diode D_1 to be reverse biased. Assuming a minimum back resistance of 1 M, the discharge current of C_c will now be limited to the order of 1μa./volt step, and in most circuits even an instantaneous loss of battery will not produce false triggering.

It should be noted that the addition of the diode in no way alters the normal triggering of the cut-off side, since in this case, the discharge path of C_c is provided by forcing the cut-off side into conduction.

Stable-Fast Recovery Transistorized Multivibrator

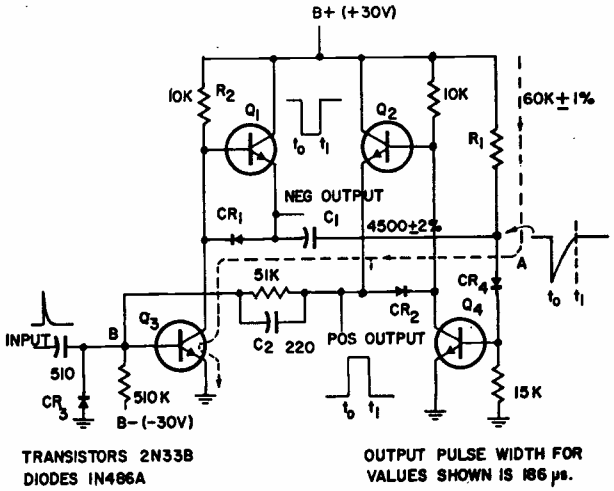


FIG. 1—Stable fast-recovery multivibrator.

THE UNIQUE MONOSTABLE MULTIVIBRATOR shown has the following highly desirable features:

- Output pulse width stability of better than 1 percent over the temperature range—55 to 85C when using mica condensers and wire wound resistors for the timing components R_1 and C_1.
- Ability to reset and trigger again at a duty cycle of 95 percent or more with less than a 1 percent shrinkage of the output pulse width from a value measured at a low duty cycle operation.
- Excellent squareness of both the positive and negative output pulses.
- Built-in emitter follower output transistors which provide low output impedances both for heavy current flow out of and also back into the multivibrator.
- These desirable features, especially that of the squareness of the output pulses with a circuit which has a very low current drain off the power supply.
- The output pulse width is independent of interchange of transistors and is unaffected by loading.
- For a 50 percent change in B+ the output pulse width changes less than 1%.

These outstanding features are gained at the expense of adding two additional transistors and

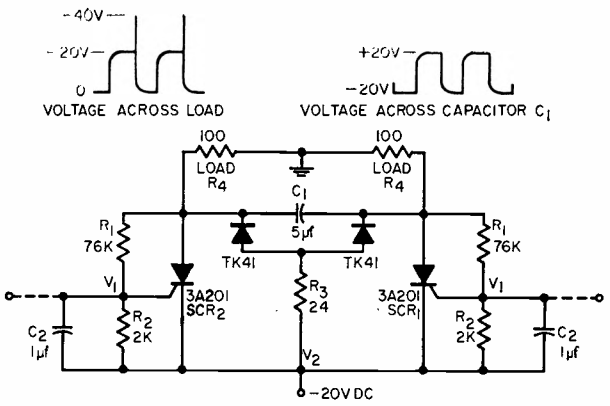
diodes (Q_1 and Q_2, CR_1 and CR_2) to the normal monostable multivibrator configuration. Transistor Q_1 reduces the recovery time associated with capacitor C_1 and the normal collector load resistor R_2 by a factor of β, which for high gain transistors can give an improvement factor of better than one hundred. Transistor Q_2 serves a similar function in connection with capacitor C_2 and its recovery time. The improvement in circuit performance with the addition of Q_2 is not as marked as that with the addition of Q_1 due to C_1 generally being one or two orders of magnitude larger in value than C_2. However, the fourth transistor Q_2, when added to the circuit, does improve all the former mentioned characteristics somewhat.

In order to reduce the current drain on the B+ supply, diodes CR_1 and CR_2 are added to the circuit. These diodes provide the dc return path for the capacitors C_1 and C_2. For example, when Q_3, the normally off transistor, is triggered on, its collector voltage drops rapidly toward ground. However, capacitor C_1 will hold the voltage at the emitter of Q_1 positive until CR_1 goes into forward conduction. With CR_1 in forward conduction, the driving impedance to bring the voltage at the base of Q_1 to ground becomes that of two forward conducting diodes (CR_1 and the saturated transistor Q_3). The path for current flow during the off time of Q_4 (time T_0 to T_1) is as shown in the Fig. 1. This unusual technique for providing a dc return path for C_1, renders a significant improvement in performance over similar circuits using low resistances from the emitters of Q_1 and Q_2 to a B— supply. This improvement is due to two factors: It greatly reduces the current load on the supplies; and it provides a lower drive impedance at the emitters of Q_1 and Q_2, thereby coupling the important wave-forms through to Points *A* and *B* more reliably than can be done with resistors to a B— supply. Diodes CR_3 and CR_4 are added to the circuit to prevent back breakdown of the base to emitter junction of Q_3 and Q_4.

Patent (No. 2,976,432) has been assigned to the Government with a free non-exclusive license to Westinghouse Electric Corporation.

Astable High Power Multivibrator

MANY ARTICLES have been written about flip-flops using silicon controlled rectifiers *scr*'s. All of these circuits required external triggers for operation. A common or representative application for this type of flip-flop is in converter power supplies. Here the high current carrying capability of the *scr* is used to provide an efficient conversion of dc to ac on a transformer primary. For applications of this nature it is desirable to eliminate the external trigger circuit to minimize components. A simple astable circuit design is shown. The voltage dividers R_1 and R_2 provide the gate voltage for the *scr*'s. When the power is first applied to the circuit, both voltage dividers will start charging the associated capacitors C_2 until one *scr* breaks down. This initiates the oscillation which is typical of this type circuit. If



Astable multivibrator

SCR_1 fires first the anode of SCR_2 is driven to 20 v momentarily. The charging of C_1 then begins until the gate voltage of SCR_2 is reached which then reverses the cycle. The time constant on the gate circuits R_2C_2 must be large compared to other circuit time constants $R_4\,C_1$, $R_3\,C_1$ to realize efficiency of operation and steep waveforms. Thus, frequency control is a function of the *RC* value in the *scr* gate circuits.

This circuit design required only the addition of six inexpensive components to accomplish astable operation. This results in considerable savings by eliminating the driving trigger circuit requirement. By varying the value of R_3 this circuit can be made to operate as a monostable or bistable flip-flop also, but in this case some low level external triggering is necessary. If the gate voltage, V_1, never reaches triggering potential neither *scr* will trigger on. By supplying an external trigger to either *scr* that *scr* will switch on and remain on. A trigger at the other *scr* gate will cause the circuit to switch to its other stable state; bistable operation has been obtained by increasing the value of both 76 K resistors.

Increasing the value of just one of the 76 K resistors will cause the circuit to be monostable. By supplying a trigger to the *scr* biased off that *scr* can be switched on forcing the circuit to go to an unstable state. After a given time approximately, 3 R_2 C_2 the circuit will return to its one stable state automatically.

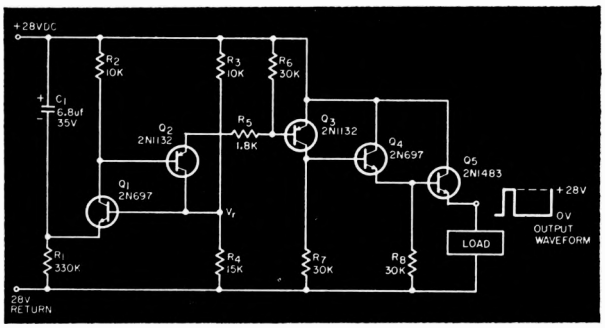
Pulse Generator Low-Frequency

THIS PULSE GENERATOR uses a two-transistor equivalent circuit for a double-base diode, providing better reliability and more uniform performance. Applications for this circuit are in recycling timers, indicator readout devices and switching regulators.

The circuit, as shown, will produce positive pulses at frequencies from as low as .05 cps to over 10 kc, depending on the values chosen for the circuit parameters. The frequency is variable over a wide range by varying C_1 and R_1 and the pulse width may be adjusted by varying R_5. With the

values shown. the frequency is about 1 cps and the pulse width is about 30 msec.

When power is applied, C_1 starts charging toward ground potential until it reaches a voltage, V_r, established by the voltage divider consisting of R_3 and R_r plus the base-emitter conduction voltage of Q_1. At this time the regenerative combination of Q_1 and Q_2 is actuated and they both go into saturation. C_1 discharges through the saturated transistors Q_1, Q_2, and Q_3 and the resistors R_2, R_3, R_5 and R_6. Transistor Q_3 is turned on by the discharge current through R_5 and a very high current gain is obtained through the compounded connection of Q_3, Q_4 and Q_5. This high current gain provides the capability of delivering up to several amperes to a load. For applications requiring less load power,



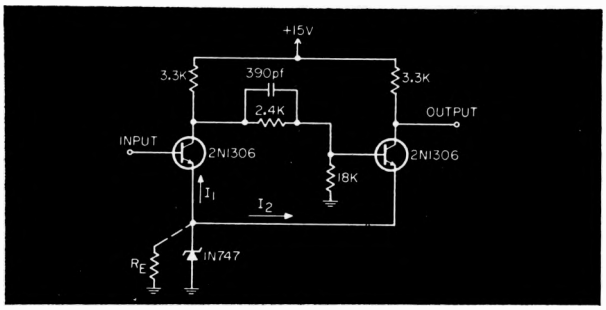
Low-frequency pulse generator.

Q_5 may be omitted and the output taken from the collector Q_4.

After the pulse is initiated, the reference voltage, V_r, takes on a new value due to the shunting of R_3 by R_5 in series with R_6 and Q_3. As the voltage on C_1 approaches this new value of V_r, Q_1 becomes biased off and all of the transistors are abruptly cut off. The circuit uses little power between pulses since all transistors are in the "off" state. ◆◆

Zero-Hysteresis Schmitt Trigger

IN A SCHMITT TRIGGER CIRCUIT, hysteresis is essentially caused by differences in I_1 and I_2, and hysteresis limits can normally be defined as $I_1R_E - I_2R_E$. There would be zero hysteresis if either of two conditions were met: $I_1 - I_2 = 0$ or $R_{E-} = 0$. The first is difficult to achieve, usually requiring matched transistors and matched collector load



Zero-hysteresis Schmitt trigger.

resistors. The second condition, $R_E = 0$, cannot be met because the Schmitt trigger requires an emitter resistor for regenerative feedback used in the switching action.

One other way of reducing the hysteresis to zero is to simply set $I_1R_E - I_2R_E$ equal to zero by replacing R_E with a constant voltage source, such as a zener diode. Small variations in I_Z do not affect the zener voltage, hence zero hysteresis. ◆◆

Voltage-Controlled Ramp/Trigger Generator

THIS CIRCUIT provides a voltage ramp and/or positive and negative trigger pulses with approximately a 6:1 linear range of frequency control. Frequency is controlled with a dc signal at the base of transistor Q_1.

The circuit consists of a constant-current source Q_1 in series with charging capacitor C. The voltage across C rises linearly with time until the firing potential of unijunction Q_2 is reached, at which time C discharges rapidly through R_2. Varying the operating point of Q_1 sets the magnitude of the charging current, which in turn controls the time required for Q_2 to fire. The frequency is given approximately by

$$f_o \approx \frac{2}{t}\left(1 - \frac{V_{co}}{V}\right)$$

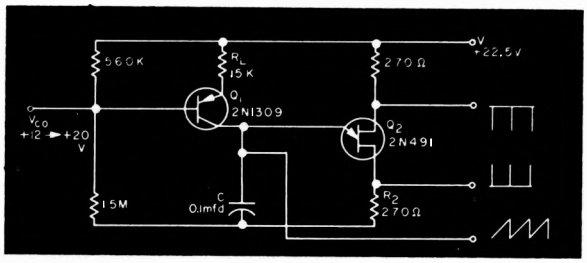
where $t = R_LC$

V_{co} = dc control voltage

V = supply voltage

For C ranging from 0.001 to 10 μf, the frequency ranges from below 10 cps to well beyond 20 kc.

The circuit has several other desirable features. The



Wide-range, voltage-controlled ramp/trigger generator. Charging current for timing capacitor C_1 is set by the operating point of Q_1.

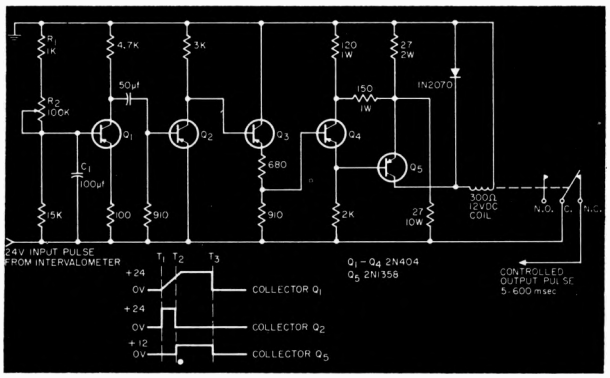
input impedance is quite high (approximately 250 K for the values shown) due to the common-collector configuration of Q_1. The trigger output impedance can be made quite low to obtain either maximum power or voltage gain. The ramp linearity is within ±5 percent over the working range. However, to preserve linearity and control range, the output should be coupled through a buffer stage or emitter follower. The circuit also is relatively insensitive to power supply variation and temperature effects. ◆◆

Low-Cost Pulse-Length Controller

AIRBORNE STRIP-CHART CAMERAS generally are controlled by an electro-mechanical intervalometer. However, the pulse length put out by most intervalometers is often too long. Since the intervalometer is often needed for other functions it cannot be eliminated. Here, therefore, is an inexpensive device that can reduce the duration of the intervalometer pulse without affecting its operation with other apparatus.

In one application, the minimum pulse length available from the intervalometer was 400 msec; the maximum pulse duration needed was only 100 msec. In the circuit shown the incoming pulse is applied to the normally common side

of the circuit and the supply or V_{cc} side is grounded. When power is applied, C_1 charges through R_1 and R_2. As C_1 charges, it puts reverse bias on Q_1, generating a ramp waveshape at the collector. This waveshape is then R-C coupled to Q_2, which acts like a Schmitt trigger by detecting a preset voltage level and then turning off completely, thus generating a square wave whose pulse length is controlled by



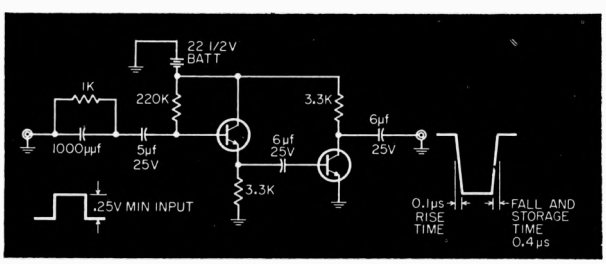
Low-cost pulse-length controller.

R_2 and can vary from 5 to 600 msec. Q_3 and Q_4 are modified emitter followers which provide isolation and prevent loading of the timing transistors, Q_1 and Q_2. Q_5 is the power switch which turns on as Q_2 turns off. A high-speed mercury wetted relay was used as the load for Q_5, giving still further isolation from load variations. All components, excluding the relay, came to less than $20.00. ◆◆

Scope-Trace Intensification Converter

TO INTENSIFY A TRACE such as an A-Scope radar presentation on a commercial scope, such as Tektronix's 535 or 545, a negative-going pulse, 15-v minimum amplitude, is required on the cathode of the scope circuit to do an acceptable job. The problem is, invariably, the pulse to be intensified is positive-going and seldom in the 15-v amplitude region. This pulse must therefore be processed before application to the cathode of the scope circuit.

This circuit was designed as the means of processing a positive pulse with a minimum amplitude of 250 mv for application to the cathode of the scope circuit. A 250-mv



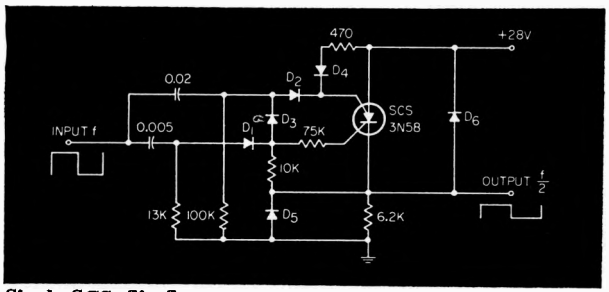
Scope-trace intensification converter.

signal drives the amplifier to saturation and a negative-going replica, 22 v in amplitude, appears across the collector load. The 1-K resistor in the base prevents oscillation and prevents excessive storage time. The 1000-pf capacity prevents deterioration of base from high dc voltages and is large enough to carry a long pulse with negligible sloping. Since the transistor only draws current when pulsed, the battery may be left connected. Its service life is almost equal to its shelf life. ◆◆

Single-SCS Flip-Flop

THIS CIRCUIT uses only one silicon controlled switch, a 3N58, to perform a flip-flop function over a wide temperature range.

In the circuit, differentiated positive pulses are applied to the cathode gate and anode gate alternately to turn the SCS on and off. When the SCS is off, the steering diode D_3 and rectifying diode D_2 are reverse-biased so that the pulse is applied only to the cathode gate to turn the SCS on. When the SCS is turned on, D_1 is reverse-biased while the reverse bias on D_2 is removed by D_3 and therefore the pulse is applied to anode gate to turn the SCS off.



Single-SCS flip-flop.

The diode D_4 is inserted so that the 470-ohm resistor does not load the positive pulse applied to the anode gate. The diode D_6 is placed so that the turn-off pulse will not appear at output. Diode D_5 prevents the differentiated negative pulse from appearing through D_3 at the output while the SCS is off.

If the anode gate and cathode gate are brought out separately, the circuit can be used as set-reset flip-flop with appropriate signal.

The circuit operates satisfactorily over the temperature range of −55°C to +100°C. ◆◆

Variable Time, Power One-Shot Multivibrator

THIS ONE-SHOT MULTIVIBRATOR switches load currents of a few milliamps to over 1 amp for a precise time interval ranging from a few milliseconds up to a minute. It requires minimal power in the "off" position and is not affected by repeated operation.

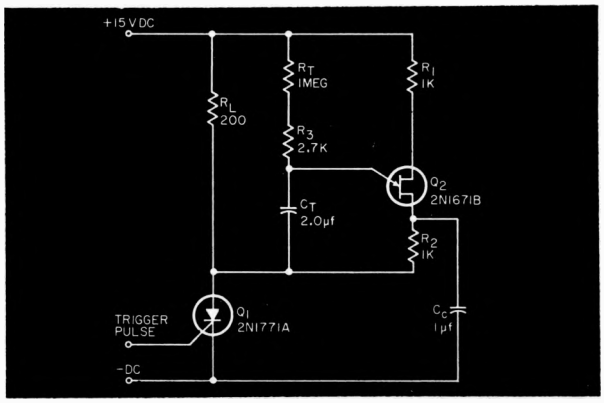
It is an excellent solid state substitute for slug relays, dash pots, and thermal timers. Several stages can be cascaded to establish a sequence of timed operations. Relay coils shunted with diodes can readily be used as loads to give multiple independent contact closures.

In the circuit's quiescent stage, the power supply drain is in the microamp range. A positive input trigger pulse fires SCR Q_1, and starts two circuit actions: load current through R_L and charging of C_T through R_T and R_3. After the desired time interval the voltage on C_T becomes equal to a critical level (roughly one-half the dc supply voltage) and the emitter-to-base-1 resistance of unijunction transistor Q_2 suddenly falls to a low value which, in effect, places the voltage on C_T from anode to cathode of Q_1 via C_C so as to drive Q_1 to an "off" condition. With Q_1 "off," the circuit is back in its quiescent state and ready for repetition of the cycle.

With the values shown in the circuit and R_T set at 680 K, a 1-volt trigger pulse initiates a 1-sec "on" period, during which a load current of 70 ma is delivered to the 200-ohm resistor (R_L). The "on" period is reproducible to within 5

parts per thousand when the circuit is triggered once each second.

In a high-current application, dc voltage = 30 v, $R_L = 21$ ohms, $C_T = 6.8$ μf, $C_C = 6.8$ μf, and $R_T = 750$ K, a load



High-power one-shot multivibrator.

current of 1.3 amp flows for 15 msec with R_T set at minimum and for 7 sec with R_T set at 1 meg.

The "on" time for the circuit can be calculated from:

$$t_{on} = \frac{(R_T + R_3)\, C_T}{0.43} \cdot \log\left(\frac{1}{1-n}\right)$$

where n = UJT intrinsic stand-off ratio. ◆◆

Astable Multi Has Microsecond Fall

ALTHOUGH the free-running multi can be easily designed to give microsecond rise times, the fall times are generally too slow to be of use in a triggering application. If the application calls for microsecond rise *and* fall times, the following technique may be used.

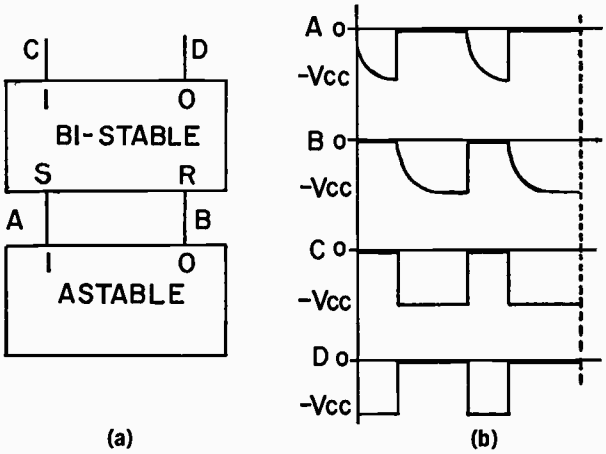


Fig. 1. (a) Astable sets and resets bistable; (b) resulting waveforms.

The fast rise times of the astable multi are used to alternately set and reset a bi-stable flip flop as shown in Fig. 1 (a). This results in the output waveform of the bi-stable following the astable with the important exception that the fall times are fast, being limited mainly by the transistor parameters and loading. See Fig. 1 (b). In practice, microsecond rise and fall times are easily obtained.

The circuit in Fig. 2 is a typical application which required a 5 cps square wave with microsecond rise and fall times.

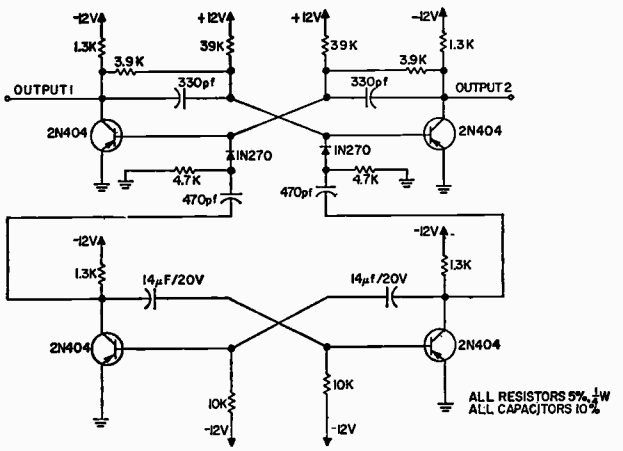


Fig. 2. Symmetrical 5 cps astable multi with flip flop waveform squaring.

Unijunction Adds PWM Mode to S-R Flip Flop

IN MANY pulse-width-modulation applications the designer will attempt to use a standard monostable multivibrator and adjust the RC time constant for the desired modulation. Usually the resistance is adjusted by replacing it with a transistor used as a constant-current source as in Fig. 1. This technique will work, but only over a limited modulation range, typically 40 to 60 percent. This limited range is due to the variation in base bias current (I_B) in the "on" transistor with variation of the resistance in the RC combination. At the extremes of modulation, the "on" transistor is either in heavy saturation with small R (large base drive) or barely in saturation with large values of R (small base drive).

The circuit shown in Fig. 2 combines a standard set-reset flip flop with a unijunction transistor to produce a PWM output which is linearly adjustable from 0 to 100 percent. The operation of this circuit does not involve variation of circuit parameters but obtains PWM action by variation of the charging rate of capacitor C.

Output A of the set-reset flip flop goes high when negative input E_{in} is applied to the set input. As A goes high, A goes low and inverter Q_1 is turned off. This releases the

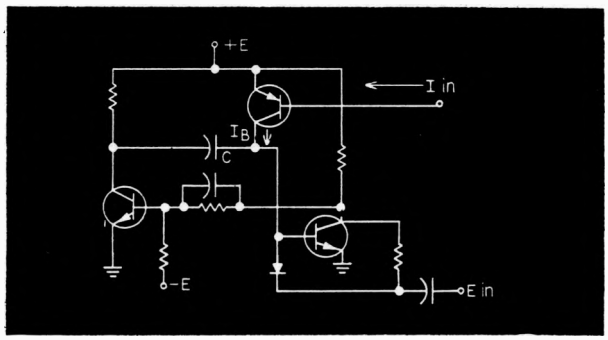


Fig. 1. Limited-range PWM circuit.

emitter E of UJT Q_3 from its clamp to ground and capacitor C begins charging towards +28 v through constant-current source Q_2. When Q_3 fires, the positive pulse generated

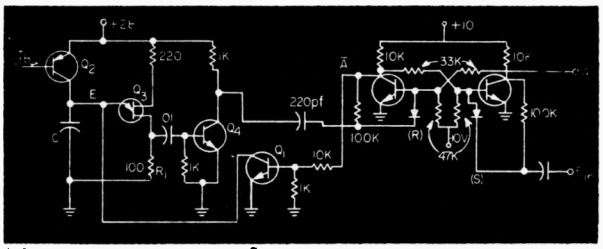


Fig. 2. Full-range PWM circuit uses UJT combined with standard S-R flip flop.

across R_1 (in base 1 of Q_3) is inverted by Q_4 and a negative pulse is applied to the reset side of the SR flip flop returning it to its original state. The pulse width of the output at A is, of course, defined by the base current I_B of Q_2.

Trigger Circuit Gives Less P_{diss}, More V_{out}

HERE IS AN IMPROVED TRIGGER CIRCUIT with regenerative switching action similar to the conventional Schmitt trigger circuit. Basically, the improved circuit consists of an npn common-emitter stage followed by a pnp stage and a selected amount of positive feedback.

The emitter of the npn stage, Fig. 1, is referenced to a voltage source, V_Z. When the input voltage is low, the output is low. When the input voltage exceeds the turn-on threshold, the regeneration provides a rapid transition of the output voltage from low to high. Likewise when the input voltage drops below some sustaining level, the output voltage rapidly returns to low. R_1 is the

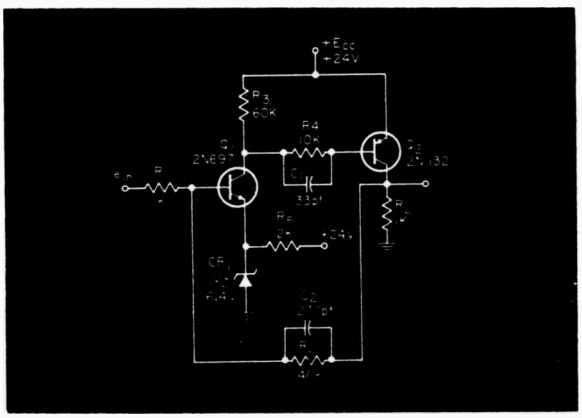


Fig. 1. Improved trigger circuit.

mixing resistor for the input signal and R_2 is the mixing resistor for the feedback signal. With $R_2 >> R_1$, as will generally be true, the turn-on threshold is approximately 0.5 volts greater than V_Z. R_5 establishes the operating point of CR_1. Turn-off input voltage is determined by the percentage of feedback used, and by the loading caused by the base input resistance of Q_1. R_3 and R_4 reference the base of Q_2 to $+E_{cc}$ when Q_1 is off, which prevents conduction of Q_2. When Q_1 is on, R_4 limits the base current of Q_2 to some desired value.

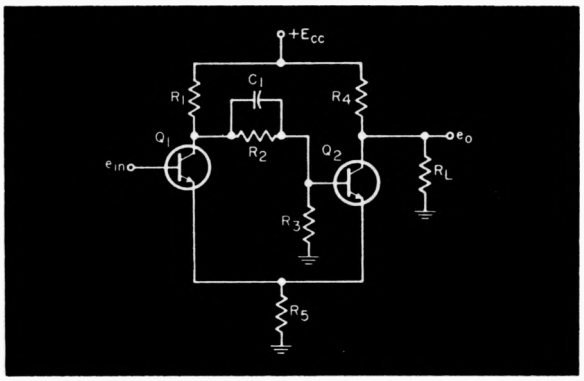


Fig. 2. Conventional Schmitt trigger circuit.

C_1 and C_2 are speed-up capacitors which insure high loop gain for transients, and consequently, fast rise and fall times.

The improved trigger circuit in Fig. 1 has the following advantages over the conventional Schmitt trigger circuit shown in Fig. 2:

- Reduced power consumption, since in the "off" state neither transistor is conducting.
- Full-range output voltage swing. The output voltage of the improved trigger switches from 0 to E_{cc}. The baseline output voltage of the conventional Schmitt trigger is determined primarily by the divider effect of R_4 and R_5.
- Low output impedance. When on, the output impedance of the improved trigger is limited only by the low saturation resistance of the pnp transistor. The output impedance of the conventional trigger is equal to R_4. Lower output impedance in the conventional circuit is achieved at the cost of additional standby power dissipation, because of a lower value of R_4.

Disadvantages of the improved circuit are:

- More parts required. The improved circuit requires a zener diode and one additional capacitor more than the conventional circuit. However, for a turn-on threshold of +0.5 v, the diode and one resistor are eliminated.
- Some input signal appears in the output. A small amount of input signal is coupled to R_L through R_1 and and R_2 when the trigger circuit is off. If this effect is objectional, a diode in series with R_2 would prevent positive inputs from reaching R_L; a diode in series with R_1 would prevent negative inputs from reaching R_L.

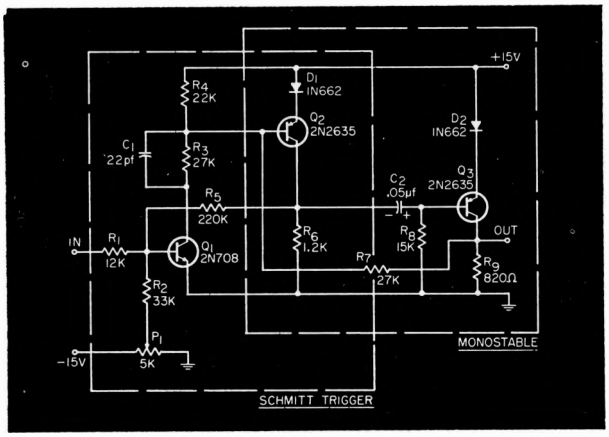
The circuit shown in Fig. 1 was tested at room temperature. Both the rise and fall time (10 to 90 percent) measured 0.15 μsec. With R_2 = 40 K, turn-on voltage is 6.97 v and turn-off voltage is 6.49 v.

Combination Schmitt Trigger-Monostable Multivibrator

THREE TRANSISTORS in a complementary configuration combine the function of a Schmitt trigger and a monostable multivibrator.

The advantages of the circuit are two-fold: the triggering level is accurately controlled and the output pulse width is independent of input drop-out since the circuit is regenerative.

In the circuit, as soon as the input level crosses a threshold established by P_1, then Q_1 and Q_2 turn on. R_5 increases



Schmitt trigger, (Q_1, Q_2) aud monostable multi (Q_2, Q_3).

the regeneration of the circuit by providing additional turn-on current to Q_1. Q_3 is normally on and Q_2 normally off; therefore, C_2 is charged as shown in the figure. As soon as Q_2 turns on, the positive step through C_2 turns off Q_3. Positive feedback from Q_3 through R_7 back to the base of Q_2 insures that if the level at the input drops below the triggering level of Q_1, then Q_2 will still remain turned on. C_2 discharges through R_8 until Q_3 turns on, thus terminating the cycle.

The figure shows the Schmitt trigger to be made up of Q_1 and Q_2, and the monostable of Q_2 and Q_3.

Delayed Pulse Generator

THIS CIRCUIT generates an output pulse delayed in time relative to an input pulse. Only three transistors are used rather than the four that would be needed in the more conventional method for generating a delayed pulse, a pair of "one-shots."

Before the circuit is pulsed, Q_1 is off, and Q_2 and Q_3 are on. The input pulse turns on Q_1, and through the action of C_1, turns off Q_2. This state remains intact for a time determined by C_1, R_3, and R_4. C_1 charges through R_3 and R_4 and eventually turns Q_2 back on, thereby turning Q_1 back off. When Q_2 turns on, Q_3 turns off due to the action of C_2. Q_3 remains off for a time determined by C_2, R_6, and R_7. C_2 charges through R_6 and R_7, thus turning Q_3 back

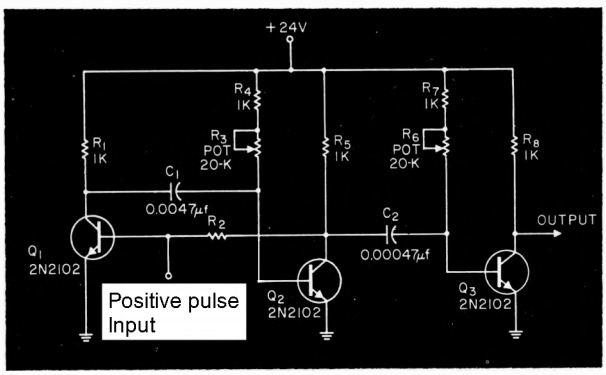


Fig. 1. Delayed pulse generator.
R2 poor print, thought to be 12k

on. The result is a delayed pulse at the collector of Q_3.

Fig. 2 shows how various waveforms are time-related to each other. The delay time, t_1, can be adjusted with the

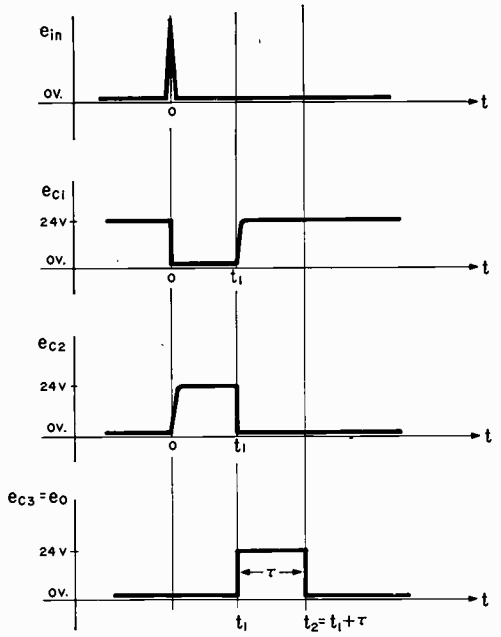


Fig. 2. Circuit waveforms.

potentiometer R_3. For the values shown, this is of the order of 10 μsec. The pulse width, τ, can be adjusted with the potentiometer R_6. This time is also about 10 μsec. The rise and fall times of the output pulse are less than 0.5 μsec.

Frequency Divider With Independent Pulse-Width Control

IN MANY pulse-frequency division circuits, additional circuitry is often required to reshape the pulses. For example, if a standard one-shot multivibrator is used as the divider, the width of the pulse is increased as shown in Fig. 1. However, pulses of the desired width, as in Fig. 2, may be obtained as the division is being accomplished with the circuit of Fig. 3.

In the circuit, Q_1 is normally off and the collector of Q_1

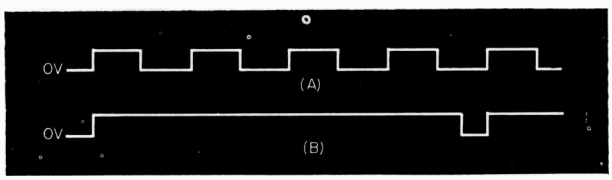


Fig. 1. Input (A) and output (B) from standard multi.

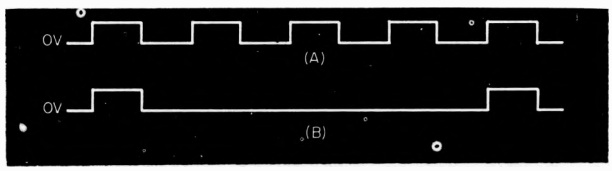


Fig. 2 Input (A) and output (B) from frequency-divider circuit.

at +12 v. Q_2 is on and its collector is at approximately 0 v. The first positive pulse will turn Q_1 on and Q_2 off. The time duration that Q_2 remains off is determined by R_1 and C_1. When Q_2 is off, C_2 charges toward +12 v through

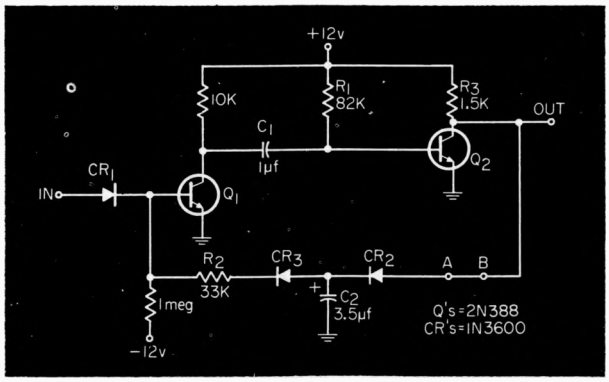


Fig. 3. Frequency-divider circuit.

R_3 and CR_2. As C_2 charges, some of its current flows through CR_3 and R_2 to insure that Q_1 remains on. The time constant of R_2 and C_2 must be greater than that of R_1 and C_1.

When the charge on C_1 allows Q_2 to turn on, its collector will return to 0 v. CR_2 is now back-biased and will prevent the discharging of C_2 by Q_2. C_2, which was charged through a low impedance, will discharge through R_2 thus holding Q_1 on. Q_1 will ignore any additional pulses until C_2 has discharged. R_1 and C_1 control pulse width, and R_2 and C_2 control the time between output pulses.

The components shown divide 50-msec pulses by 5 without changing the pulse width. However, a great variety of outputs may be achieved by changing the circuit time constants. Pulse risetimes may be improved and the range of operation can be extended by adding an emitter follower between points A and B in Fig. 3.

PW Modulator as Multiplier and Bang-Bang Amplifier

THE CIRCUIT OF FIG. 1 is a relatively simple pulse-width modulator with a couple of interesting applications. The circuit combines an astable (Q_1, Q_2) and a differential (Q_3, Q_4) circuit. The differential circuit will keep the sum of the base currents of Q_1, Q_2 constant such that the basic carrier frequency remains fairly constant. The pulse width, however, will depend on the division of the total base current as determined by the input signal to the differential.

It takes only a simple RC averaging network to detect the pulse-width modulated output. A 100-mv swing at the input produces a 20-v demodulated output swing, linear to within 5 percent. The gain of 200 can be used to increase the linearity by feedback. In the circuit of Fig. 2 the demodulated output will follow the input within 5 percent/200 = 0.025 percent.

A relatively simple analog multiplier is possible by applying the output to a switching circuit in which the collector supply, and therefore, the pulse amplitude, is proportional to the other factor, y, in Fig. 3. The demodulated output will be proportional to the product xy.

Finally, the pulse-width modulator may be used as a bang-bang audio amplifier, Fig. 4. A small transformer

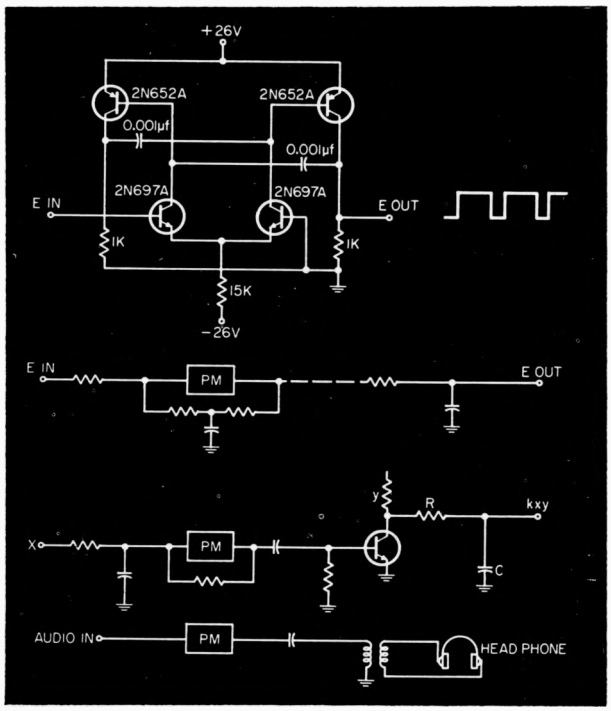


Fig. 1. Basic pulse-width modulator circuit.

Fig. 2. As an accurate information carrier.

Fig. 3. As an analog multiplier.

Fig. 4. As a bang-bang audio amplifier.

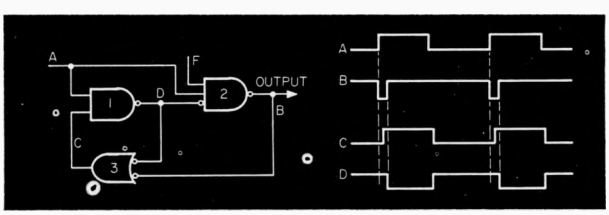
may be used if the carrier frequency is high. Earphones connected to the secondary will do the averaging and demodulation directly. A buffer stage may be necessary. Because of the bang-bang operation, a minimum of heat is dissipated.

Narrow Pulses with DTL Integrated Modules

WHEN DESIGNING LOGIC, it frequently becomes necessary to obtain narrow pulses corresponding to the leading edge of a signal. With standard circuits this is not a problem since the signal can be differentiated with a capacitor-resistor-diode combination. But if DTL integrated circuits are being used, this cannot be done since the input to the DTL circuit is a diode AND gate.

The logic circuit shown can be used to generate pulses approximately 60 nsec wide corresponding to the leading edge of a pulse. It has been found that the addition of only one module to the system is usually needed since gate 2 is normally present and 1 and 3 are in a single module.

The input pulse is applied at point A and is passed through gate 2 since point C is normally high. The output at B then goes low, forcing the output of the OR gate high.



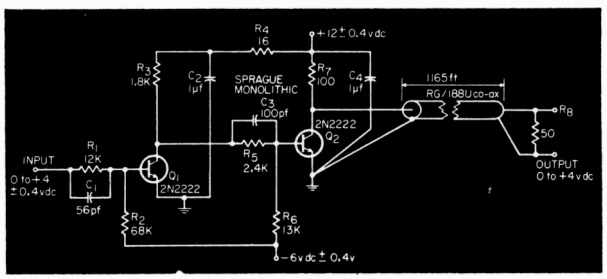
Integrated circuits provide narrow pulses on leading edge.

Gate 1 now has two high signals so its output, point D, goes low inhibiting Gate 2 and forcing point B back to a high level. The circuit will then stay latched in this position until cleared by A going low, allowing point D to go high. The circuit is now ready for another cycle.

The width of the pulse is only dependent upon the propagation delay of the modules and may be made wider by placing a capacitor from point C to ground if necessary. Note that gate 2 may have more than one input. That is, it may be used to perform a normal AND function by applying a signal to point F.

Coaxial Cable Driver Circuit

HERE IS A CIRCUIT that can drive digital information through long lengths of coaxial cable. Pulses of 30-nsec rise and fall time have been sent through 1155 ft of 50-ohm co-ax (RG/188U), and through 650 ft of 93-ohm co-ax (RG/62U). Since risetime (τ_r) can be related to frequency (f) by the equation $f = 0.352/\tau_r$, a risetime of 30 nsec means that a frequency of 10 to 20 mc is coupled into the supply and ground leads. R_4, C_2, and C_4 comprise a decoupling circuit which eliminates this. These capacitors, C_2 and C_4, must be good quality, high-frequency units. Since tantalytic and electrolytic capacitors become inductive in this frequency range, they must not be used here. Sprague monolithic capacitors were found to be suitable. Also, great care must be used in laying out this circuit—the power and ground leads as well as input and output leads, must



Coaxial cable driver circuit.

be as short as possible.

For use with a different characteristic-impedance co-ax, merely replace R_8 with the characteristic impedance of the co-ax selected. The output level, of course, will change. This can be easily calculated.

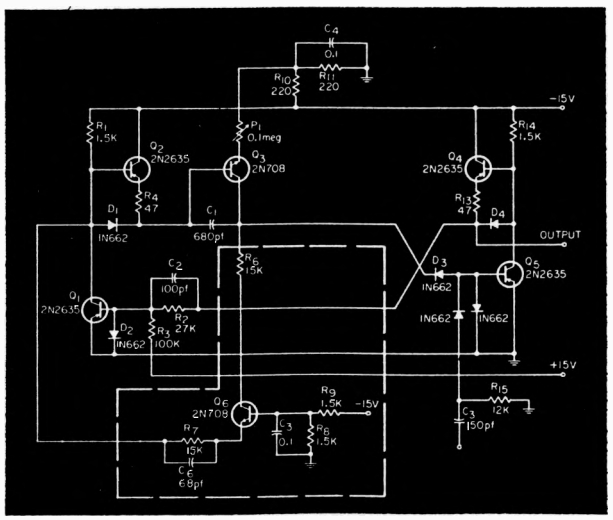
There is no noticeable deterioration in the wave shape (input to co-ax vs. output) with a ±20 percent variation in R_8.

Wide Range Monostable Multivibrator

THE ADDITION of one transistor to a linear one-shot increases the range through a ratio of 150 to 1. In the circuit shown, Q_6 is the extra transistor. Its associated circuitry is shown within the dashed lines.

Q_5 is normally on, Q_1 and Q_3 are off. Q_6 is forward-biased and therefore provides a steady base current to Q_5. A positive pulse coming in through C_5 cuts off Q_5 and turns on Q_1 and Q_3. This positive step is transmitted through C_1, which was charged to approximately −15 v and maintains Q_5 off during the one-shot timing cycle. C_1 charges through constant-current source Q_3 at a rate determined by the setting of P_1 and the voltage across it, approximately 5.7 v. When the voltage at the collector of Q_3 has reached −1 v, Q_5 starts turning on, Q_1 begins to turn off, Q_6 starts conducting, turning Q_5 on harder. This cycle of events is regenerative so that Q_5 rapidly saturates and cuts off Q_1 which in turn cuts off Q_3.

The circuit effectively separates the charging current through C_1, which varies the timing of the one shot, from the biasing current turning on Q_5, which should be constant. The current through Q_3 has to be only sufficient to set Q_5 into the active region and thus start regenerative action.



Added transistor Q_6 increases range of monostable.

Fast-Recovery One-Shot Multi Gives 10:1 Width Control

MOST ONE-SHOT multivibrator circuits that have short recovery time compared with the output pulse width use additional transistors and diodes to provide a discharge current that is much greater than the charging (timing) current. This disadvantage of extra components is not present in the circuit shown here, which is currently in use in a commercial radar range unit and a pulse analyzer.

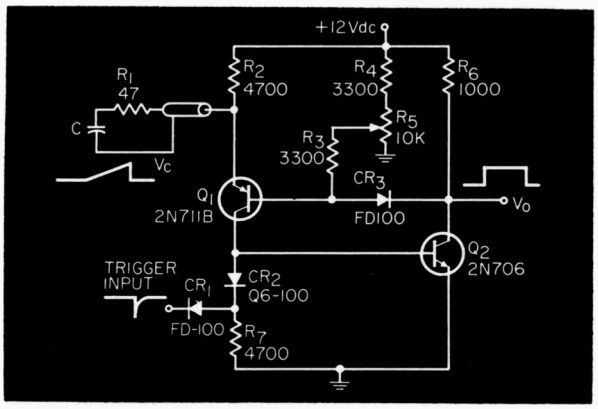
The pulse width can be readily varied from 0.1 μsec to 10 msec in decade ranges by using appropriate timing capacitors. Risetime of the output pulse is essentially constant at about 10 nsec over the entire width control range. Further, very high duty factors (90 percent for shorter widths and 97 percent for maximum widths) can be realized because the recovery time is nearly a constant fraction of the pulse width.

With an npn and a pnp transistor, both transistors in the multivibrator are simultaneously on or off, as contrasted with the usual case in which one transistor is on while the other is off. In the circuit shown, Q_1 and Q_2 are off during the pulse-width period, the longest time interval in the circuit. In addition to achieving high duty factors, use of the npn and pnp configuration provides a large discharge current path for the timing capacitor, C, without the requirement for additional components.

A negative-going trigger is applied to the base of Q_2 via CR_1 and CR_2 to turn Q_2 off. The resulting positive change at the collector of Q_2 appears at the base of Q_1 to quickly

cut off Q_1, and the emitter of Q_1 is restrained from following the base of Q_1 by timing capacitor C. Thus, Q_1 remains in the cutoff state and regeneratively completes turning off the base of Q_2. Both Q_1 and Q_2 remain off until C charges to the voltage level present at the base of Q_1. This level is set by R_5, the width control, to determine the time required for the emitter and base voltages of Q_1 to equalize.

When the emitter and base voltages of Q_1 are equal, Q_1 and Q_2 conduct as heavily as they can (limited primarily by their internal resistances) to discharge C to its quiescent voltage level. Timing resistor R_2 functions to maintain sufficient current in the emitter of Q_1 so that the circuit remains on over the entire range of R_5 after the heavy discharge current dies out. CR_3, a disconnect diode, permits the output at the collector of Q_2 to swing a full 12 V regardless of the setting of R_5.



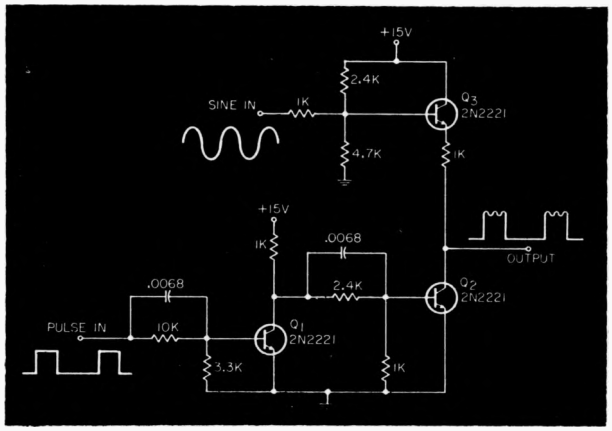
Opposite polarity transistors allow fast recovery with broad width control.

With the exception of timing capacitor C, component values are as indicated on the schematic. The value of C is determined from the following relationship: C (pf) = Maximum Pulse Width (μsec) $\times$ 10^2. The value of C for a decade range of 1 to 10 μsec, for example, is 1000 pf.

In addition to having a fast recovery time, this circuit exhibits several other features: essentially constant trigger sensitivity over the complete width range (a pulse width of many milliseconds can be generated with a trigger width of 50 nsec); only one power supply is required; no large recharge current flows through the power supply to cause transients; a width control range of 10:1 is readily obtained with a remote (up to 10 ft) control; and timing capacitors that determine the decades over which the pulse width is variable can be remotely (up to 10 ft) located on a range switch by using coaxial cable with the shield grounded at the circuit but not at the switch.

Pulse Amplitude Modulator

IT IS OFTEN DESIRABLE to amplitude modulate a pulse train with an audio signal or some other input, such as noise. This circuit will satisfactorily perform this function over an audio signal range of 0 to approximately 200 kHz with input pulses over 1 μsec in duration. The maximum attainable percent modulation is dependent on the modulation frequency with approximately 80-percent modulation available at frequencies up to 3 kHz decreasing to 30 percent at an audio input of 200 kHz.



Pulse-amplitude modulator.

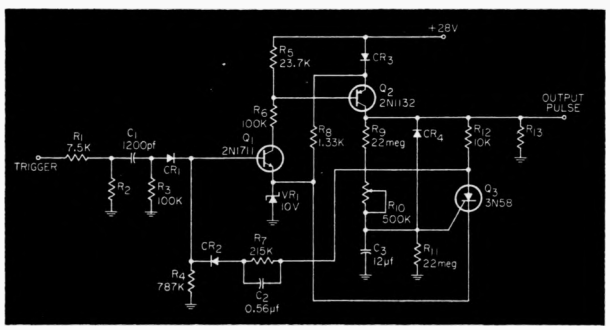
The circuit consists of an emitter follower which determines the collector voltage for a saturated pulse amplifier Q_2. Amplifier Q_1 serves as an inverter to make the pulse input positive-going. Q_1 may, of course, be omitted if the input pulse train is negative-going (input at ground during pulse and positive between pulses). An emitter follower may also be added, if desired, in order to drive low impedance loads.

High-Gain, Long-Pulse Monostable

THIS ONE-SHOT has the following advantages over more conventional types: high current gain, long pulse width with relatively small timing capacitance and low dissipation in the off state.

The trigger pulse turns on Q_1 and Q_2. Transistor Q_2, besides supplying load current, provides lock-up drive to Q_1 through R_{12}, R_7 and CR_2. Capacitor C_3 charges toward Q_2's collector voltage through R_9 and R_{10}. When the charge on C_3 reaches the sum of the voltage on zener VR_1 plus the gate-to-cathode firing voltage of Q_3, Q_3 turns on. The voltage on the anode of Q_3 drops to nearly the VR_1 voltage and the left side of C_2 is pulled considerably negative to insure turn-off of Q_1 and hence, Q_2. The base of Q_1 doesn't go negative but is grounded through R_4. Diode CR_2 is included to prevent destruction of Q_1 by exceeding its BV_{ebo} rating.

The maximum pulse length obtainable for a given value of C_3 is limited by the I_{ago} of Q_3 (which determines the maximum value of R_{11}), the leakage resistance of



High-gain, long-pulse monostable.

C_3 and the gate firing current required for Q_3.

Resistors R_2 and R_{13} are optional in that reset time

specification may be met through the effect of source and load impedances. Diode CR_4 allows C_3 through R_{13} or the load.

The circuit shown is adjusted for a pulse width of 11 sec and drive a 19.6-K load. Transistor Q_2 must be saturated in order to provide maximum output and a definite charging voltage ($V_{c_{43}}$) for C_3.

Wide-Range Monostable, PRF Discriminator

THE MONOSTABLE CIRCUIT of Fig. 1 can be electronically adjusted to vary its output pulse width from several seconds to 0.2 μsec. With the feedback path shown in dashed lines, it performs as a PRF discriminator with output dc voltage as a function of frequency from below 3 Hz to 300 kHz.

The input pulse, which should be of uniform amplitude and width, is applied to diode CR_1 and charges capacitor C_1 up to peak amplitude. Transistor Q_2 is immediately cut off, Q_3 conducts, and Q_4 is shut off. The output at the collector of Q_4 rises to power supply level in about 0.1 μsec.

The charge on C_1 leaks off through Q_1. The amount of leakage current is determined by the input control voltage applied to the base of Q_1. When the potential on C_1 is sufficiently low, Q_2 clamps the base of Q_3 to ground, shutting Q_3 off, and Q_4 conducts again, pulling down the collector potential with a speed which is about 1/1000th of the pulse width at the wide end, and 0.1 μsec at the narrow end.

Any monostable and an averaging network constitute a PRF discriminator. In the present circuit the range of such a configuration is extended by feeding back from the averaging network R_4, C_2 a voltage which will, as the frequency goes up, narrow the pulse width to make it possible to go to still higher frequencies. This voltage is fed to the pulse-width controlling transistor Q_1 through resistor R_5. A bias input through R_6 assures that, at low frequencies there

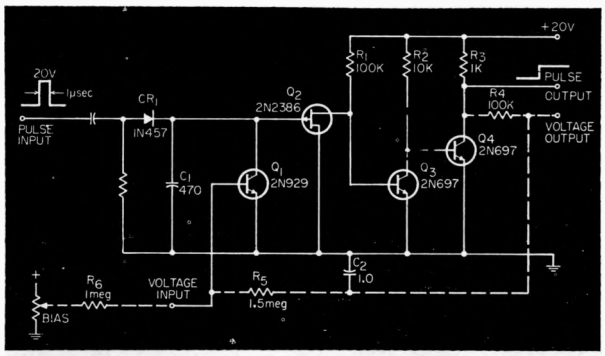


Fig. 1. Electronically-adjustable monostable.

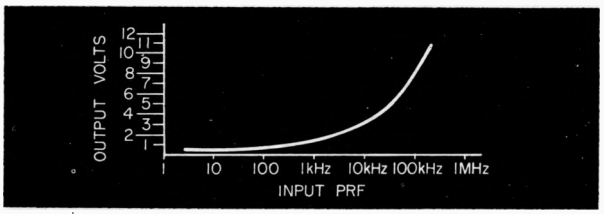


Fig. 2. Frequency characteristic.

is a finite pulse width (5 μsec) to give a finite output and feedback action.

Figure 2 shows a plot of input frequency versus output voltage. The high end can be extended by using a narrower input pulse. Conversely, the low range can have better definition by using a wider input pulse at the expense of high frequency response. The response curve can be modified, of course, by including a shaping network in the feedback path.

Improved One-Shot Output Circuit

IT IS SOMETIMES NECESSARY to take the output of a one-shot from the timing side to obtain the correct polarity output pulse. This is normally accomplished with a resistive divider (R_1, R_2) and capacitive speed-up as shown in Fig. 1. A serious limitation of this circuit is the large variation in output pulse width resulting from the use of Q_1's collector voltage to drive the output amplifier. Because of the limited current available to recharge C_1, the trailing edge of Q_1's collector voltage pulse is a ramp. The point on the ramp where Q_3 turns on, and hence the output pulse width, is a function of the divider accuracy, the supply voltages, the beta of Q_3, and the load.

In the improved circuit, Fig. 2, the timing current serves to discharge C_1 during the active timing period and supplies base drive to the output amplifier during the recovery period. This is accomplished by replacing the clamp diode on the right side (CR_2 in Fig. 1) with the base-emitter junction of the output amplifier.

Transistors Q_1 and Q_2 form an astable multivibrator with Q_2 normally biased on. Transistor Q_3 is also normally turned on by the current through R_4. The positive-going leading edge of the input pulse, differentiated by C_1, turns on Q_1. The resulting negative-going pulse at the collector of Q_1, coupled through the timing capacitor, C_2, turns off Q_3 and holds off Q_2. Resistor R_4 discharges C_2, turning off Q_2 at the end of the active timing period. As Q_2 turns

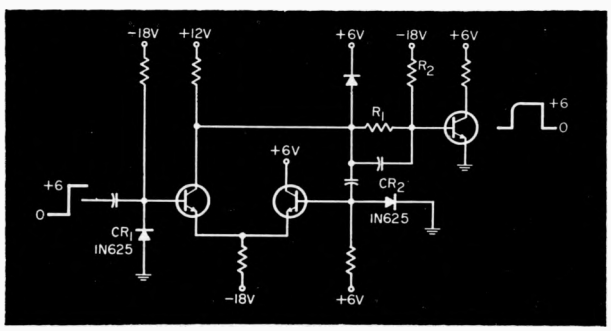


Fig. 1. Basic one-shot output circuit.

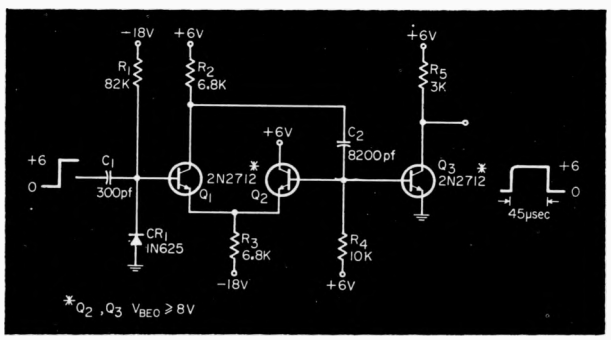


Fig. 2. Improved one-shot output circuit.

on, Q_1 turns off. The positive-going pulse at Q_1's collector, coupled by C_1, turns Q_2 off harder and supplies speed-up drive to turn on Q_3. Transistor Q_3 is now held on by the current through R_4, and C_2 is recharged through the base emitter junction of Q_3 by R_2.

For the power supply voltages and component values shown, the active timing period is:

$$T_a = R_4 C_2 \ln \frac{6.6}{12.6} = 0.646 R_4 C_2$$

The recovery period is:

$$T_r = 5 R_2 C_2$$

If Q_3 is a low-leakage silicon transistor, the timing performance will not be affected.

The improved circuit, besides using less power, gives improved timing accuracy with the use of fewer components.

Eliminating False Triggering in Monostable Multis

THE ADDITION OF three diodes and one resistor to a conventional monostable multivibrator permits an increase in the timing resistor, R_t, without making the circuit susceptible to false triggering.

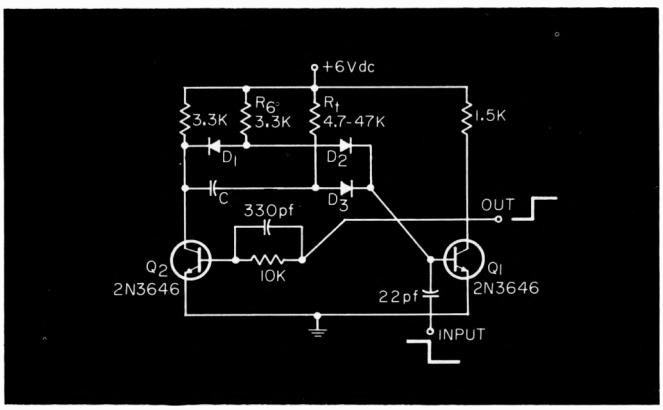
The monostable should be able to accommodate large timing resistors for two reasons: a wider variation of pulse width can be achieved without changing C, and larger R/C ratios can be used, thereby increasing the duty cycle.

In the conventional monostable, large values of R_t cannot supply enough base drive to Q_1 to provide adequate noise immunity when the monostable is in the quiescent state, making the circuit susceptible to false triggering.

In the modified monostable shown, substantial base drive is supplied by R_b when in the quiescent state. A negative-going trigger step at the input turns Q_1 off, driving Q_2 into saturation and diverts Q_1 base current through D_1. At this time the junction between C and D_3 goes negative. Both D_2 and D_3 are now cut off. C must now charge through R_t to V_{be} of Q_1 before Q_1 can turn on.

When Q_1 turns on, Q_2 cuts off, allowing R_b to supply hard base drive to Q_1. The monostable will stay in this state until intentionally triggered.

The maximum value of R_t depends on the β of Q_1. The value of R_t may be extended by using a high-β Q_1 or by driving Q_1 with an emitter follower.



Extra components allow better triggering operation in mono stable multi.

Pulse-Width Discriminator

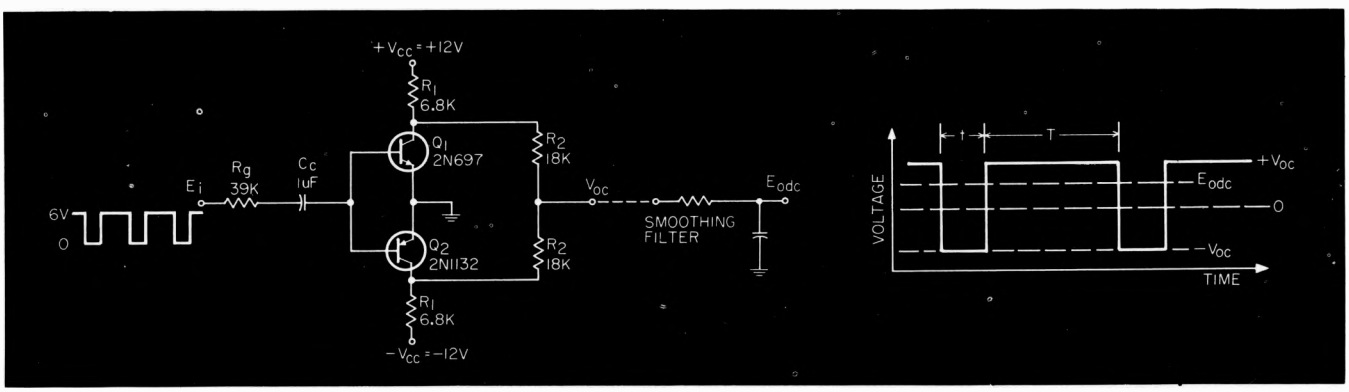


Fig. 1. Duty-cycle of input signal determines the output voltage of this discriminator.

Fig. 2. Output waveform of discriminator is filtered to give the average level E_{odc}.

THE SIMPLE pulse-width discriminator shown in Fig. 1 gives linear changes in output voltage for changes in input duty-cycle. The rectangular input signal can vary in amplitude without affecting the output, because Q_1 and Q_2 are operated in the switching mode. This discriminator was used in a self-balancing servo loop in which R_2 was a potentiometer geared to a servomotor:

The time constant R_2C_c must be large relative to the period of the input waveform. This gives constant-current base drive to the "On" transistor. The current must be sufficient to cause saturation. The base of the "Off" transistor is returned to ground and reverse-biased by the emitter junction of the "On" transistor.

Since the transistors operate in the switching mode, the output voltage will swing between fixed positive and negative voltages, with the average value dependent on the duty cycle as shown in Fig. 2. The dc output voltage is given by

$$E_o = V_{oc}\left[1 - 2\,\frac{t}{T}\right]$$

where t/T is the duty cycle and V_{oc} is the open-circuit voltage seen looking into the output terminals.

$$V_{oc} = \frac{R_2\,(V_{CC})}{R_1 + 2\,R_2}$$

Neglecting the filter network, the impedance seen looking into the output terminals is is simply R_2 in parallel with the series combination of R_1 and R_2.

Offset, due to unequal saturation voltages, is not a problem when the detector is used in a low-gain loop. For high-gain applications, offset can be minimized by operating the transistors in the inverted mode. The circuit will require increased drive in this mode.

Pulse integrator gives constant slopes

THE PULSE-INTEGRATOR circuit shown in Fig. 1 provides constant slope outputs controlled by two input pulses. Negative-going pulses at the base of Q_1, charge capacitor C_1. Positive-going pulses at the base of Q_2 discharge the capacitor.

During both charge and discharge, the current is constant. So the output voltage changes linearly for the duration of an input pulse. When there is no input pulse, the output level remains constant because of the charge on C_1.

Circuit equations are derived[1] as follows:

Normally the base of Q_1 is at V_{cc}, and the transistor is biased off. When an input pulse appears at the base, the base voltage drops to V_1. This turns on Q_1 and the emitter current provides a constant-current charging source for C_1. This charging current is,

$$i_{E1} = \frac{V_{cc} - (V_1 + V_{BE1})}{R_1} = \frac{V_p = -V_{BE1}}{R_1} \qquad (1)$$

Therefore

$$C\frac{dV}{dt} = \frac{V_p = -V_{BE1}}{R_1}$$

or

$$dV = dt\left(\frac{V_p - V_{BE1}}{R_1C_1}\right) \qquad (2)$$

Where dt is the time during which Q_1 is on.

Transistor Q_2 is normally off. If an input pulse is applied to the base of Q_2, the base rises to the new voltage V_2. This turns on the transistor, and its emitter current is,

$$i_{E2} = \frac{V_2 - V_{BE2}}{R_2} \qquad (3)$$

As before, the current is constant. But this current discharges capacitor C_1. The change in capacitor voltage is derived in the same way as for the charging case above.

Then

$$dV = dt\left(\frac{V_2 - V_{BE2}}{R_2C_1}\right) \qquad (4)$$

So the net voltage on the capacitor, caused by a charging pulse and a discharge pulse is,

$$V_x = V_x' + T_1\,(K_c) - T_2(K_d) \qquad (5)$$

where constants K_c and K_d are values calculated from the expressions in parentheses in Eq. 2 and 4. V_x is the new voltage on C_1 and V_x' is the preceding voltage.

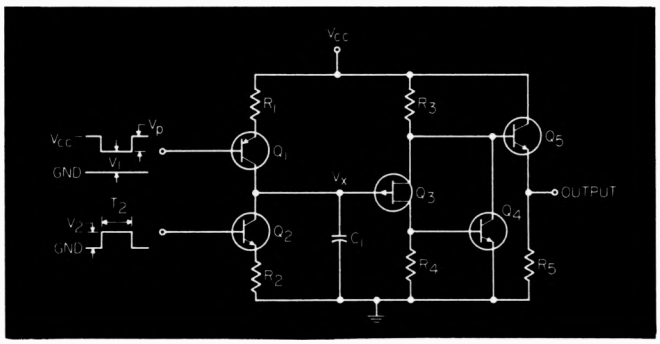


Fig. 1. Constant-current charge and discharge circuit integrates pulses.

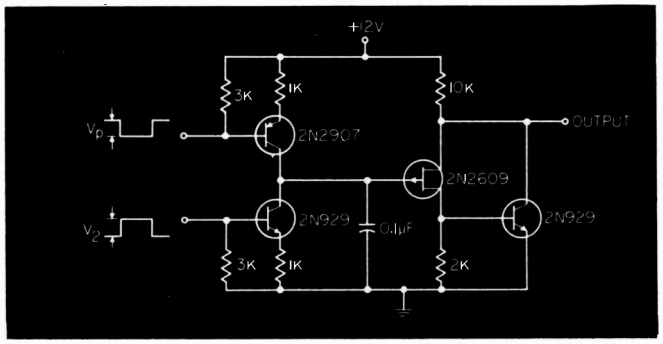


Fig. 2. Simplified pulse integrator with typical component values.

Now, because transistors Q_1 and Q_2 saturate during conduction,

$$V_x(max) \approx V_1$$

and

$$V_x(min) \approx V_2$$

Transistors Q_3 and Q_4 provide unity gain and present a

high shunt impedance across C_1. Equations for the gain and output impedance of FET amplifiers are given in many textbooks and application notes.[2] Emitter-follower stage Q_3 gives a further reduction in output impedance.

Typical component values for the charge-discharge circuit are shown in Fig. 2. For simplicity, the output stage is omitted in this figure. Typical input and output waveforms are shown in Fig. 3, for the circuit of Fig. 2. Note that the rise and fall time

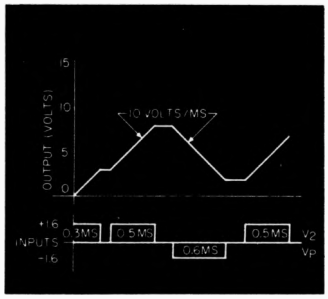


Fig. 3. Typical output waveform for the circuit shown in Fig. 2. Note that charge and discharge time constants are both 10 V/ms.

constants are identical, and all output changes are linear ramps.

The slopes of the charge and discharge ramps in Fig. 3 are calculated using the component values of Fig. 2 and assuming $V_p = V_2 = 1.6$ V, and $V_{BE1} = V_{BE2} \simeq 0.6$ V. Then

$$\left.\frac{dV}{dt}\right|_{\text{charge}} = \frac{V_p - V_{BE1}}{R_1 C_1}$$

$$= \frac{1.6 - 0.6}{0.1 \times 10^{-3}}$$

$$= 10 \text{ V/ms.}$$

Similarly

$$\left.\frac{dV}{dt}\right|_{\text{discharge}} = 10 \text{ V/ms.}$$

References

1. Richard S. Hughes, "Selected Semiconductor Circuits," *NAVWEPS Report 9039 (NOTS TP 4038)*, July 1966.
2. "High-Input-Impedance UNIFET Amplifiers," *Siliconix Application Note*, February 1963.

Improved monostable multivibrator allows wide range of pulse-width control

Conventional monostable multivibrators allow only a limited range of pulse-width control. This is because the resistive element of the RC timing network also supplies bias for the "on" transistor. So any attempt to vary the resistance over a wide range will upset the trigger conditions of the circuit.

With the modified one-shot circuit of Fig. 1, however, pulse width can be adjusted over a range of 100-to-1 or more without any change in bias level or output amplitude. Pulse width can be set with a potentiometer as shown, or externally controlled by a dc voltage or an ac modulation signal.

In the circuit shown, diode CR_1 isolates the timing capacitor C from the collector of Q_2 during the "off" period. Thus the charging potential for the capacitor is defined by potentiometer R_2. But the capacitor's discharge path is the same as with a conventional one-shot. When the circuit is triggered, the positive end of the capacitor is grounded via CR_1 and Q_2. The capacitor then starts to charge exponentially in the reverse direction towards V_{CC}, its previous charge being dissipated in the timing resistor R. But the capacitor voltage is limited by the base potential of Q_1 when the transistor starts to conduct. The interval between the arrival of a trigger pulse and the time at which Q_1 base becomes forward-biased determines the period of the one-shot.

Theoretically, the "on" time τ is adjustable from zero to 0.69 RC. Resistor R_4, necessary to limit the current of Q_2, determines the maximum practical value of τ. The "on" time can be calculated as follows:

$$\tau \approx RC \times \ln\left(\frac{V_{CC} - V_{on(Q1)} + V_C}{V_{CC} - V_{on(Q1)}}\right) \quad (1)$$

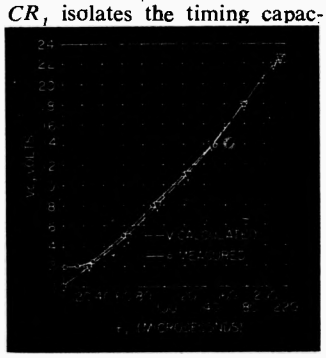


Fig. 2. Multivibrator pulse duration as a function of control potential.

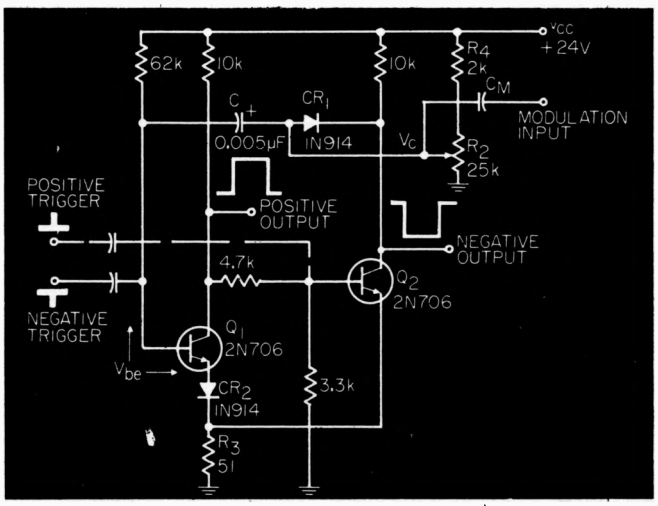


Fig. 1. This voltage-controlled monostable can be pulse-width modulated over a 100-to-1 range without change in amplitude or sensitivity.

where, $V_{on(Q1)} = V_{be(on)} + V_{CR2} + V_{R3}$ (2)

The circuit gives good linearity for small changes of V_C. Fig. 2 shows the measured and calculated values of τ plotted as a function of control voltage.

Control ratio is governed by the value of the timing capacitor C. This is because τ_{min} is fixed while τ_{max} depends on C. With suitable choice of components, large control ratios are possible.

For external modulation, one can set V_C to a voltage that gives half the maximum required τ. Then symmetrical modulation can be applied via isolation capacitor C_M. Of course, one can also offset V_C to allow asymmetrical modulation.

Sensistor stabilizes pulse width of monostable multivibrator

SOME CIRCUIT DESIGNERS have shown how dual-gate ICs can easily be converted into one-shot multivibrators, merely by the addition of a few discrete components.[1] This approach eliminates the need for special IC one-shots, thus reducing the number of different IC types required in a complete equipment.

But, modified gates usually give poor temperature stability. Pulse width of a monostable can vary by as much as ±10 to ±20% over a −55 to +125°C temperature range. The simple circuit, shown in Fig. 1, uses a Sensistor to improve the temperature stability. This technique confines variations of pulse width to within a much smaller range of around 3%.

With these component values, the circuit gives a 4-ms output pulse width. Output-pulse amplitude is approximately 1 V. The circuit requires an input drive pulse having an amplitude of 2 V and a width of 0.5 μs.

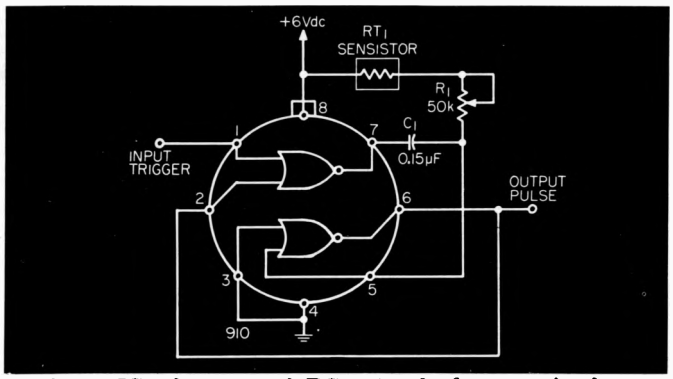
With a 50-kΩ pot, as shown in the schematic, the pulse width can be adjusted over a ten-to-one range with a maximum width of 5 ms. The Sensistor shown has been selected for optimum temperature stability of pulse widths in the range 3 to 5 ms. Other pulse widths will require different Sensistor values for optimum tempco. Suitable values are shown in the table. Still greater stability can be achieved using series or parallel combinations of Sensistors.

Maximum operating frequency for the circuit is approximately,

$$f = \frac{1}{P_W + (5 \times 10^{-4})} \text{ pps} \quad (1)$$

where P_W is the pulse width in milliseconds.

Of course, the recovery time of the circuit depends on the value of C_1. The equation shown is only valid for the specified capacitance. The Sensistor values, for optimum stability, were determined empirically using a polycarbonate capacitor for C_1. Sensistors were selected from the TI, TM-⅛ series.



Dual-gate IC, plus external RC network, forms a simple one-shot. Temperature stability can be improved by using a Sensistor as shown.

SENSISTOR VALUES FOR OPTIMUM STABILITY

Pulse width (ms)	Sensistor resistance (ohms)
5	2.2 k
3	2.2 k
2	1.5 k
1	1.0 k
0.5	1.0 k

Reference

1. Donald Femling, "One-Shot Multivibrator Kills Switch Bounce," ...

Tunnel diode speeds word-line driver

THIS HIGH-SPEED, high-power, driver circuit can deliver 220 milliamps to a 160-ohm load. Delay time is 5 ns, and rise and fall times are each 4 ns. Nominal output-pulse width is 18 ns.

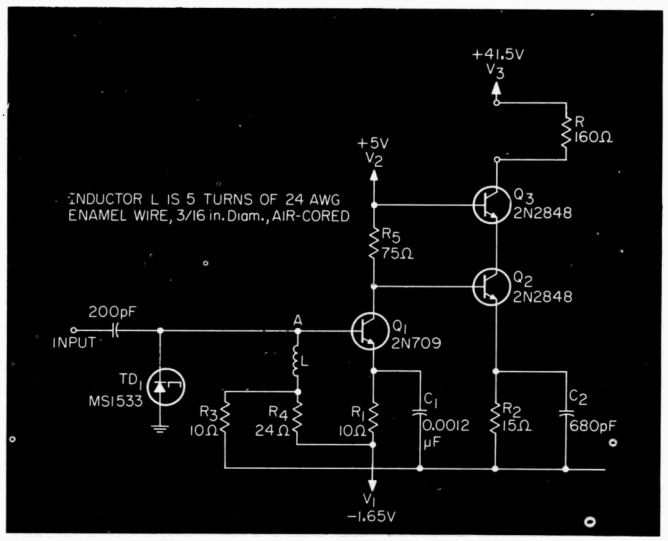
All parameters of the output pulse (for example, peak current, delay time, rise and fall times and pulse width) are independent of repetition rate. Pulse width is easily adjustable.

The circuit comprises a tunnel diode TD_1 and three transistors. The tunnel diode operates monostably. It improves switching time and controls the duration of the output pulse to the load. In the original application, the load R was a balun connected to a word drive line in a computer memory circuit.

When there is no input pulse, Q_1 is saturated and Q_2 and Q_3 are cut off. A negative input pulse triggers TD_1 from a low voltage to a high-voltage state. This produces a negative pulse at point A which drives Q_1 from saturation to cutoff. This, in turn, drives Q_2 and Q_3 to saturation, thus energizing the load R with a negative pulse.

Note that, because all three transistors are normally cut off or saturated, total power dissipation is a minimum.

Current-feedback resistors R_1 and R_2 compensate for temperature effects and unit-to-unit variations in performance of Q_1 and Q_2. Bypass capacitors C_1 and C_2 boost the ac gain and improve the switching time of the circuit. Time constants R_1C_1 and R_2C_2 are both smaller than the minimum cycle time needed to maintain a con-



Tunnel diode TD_1, in this simple word-line driver, acts as a one-shot to give fast switching speed and adjustable recovery time.

stant dc output level that does not shift with variations in repetition rate. Voltage levels at the emitters of Q_1 and Q_2 recover within the minimum cycle time.

Width of the output pulses is easily adjusted over the range 15 to 22 ns without disturbing the switching speed. This is done by merely stretching or compressing the turns of inductor L. Recovery time of the tunnel-diode circuit, which is very short, is determined by R_3, R_4, L and V_1.

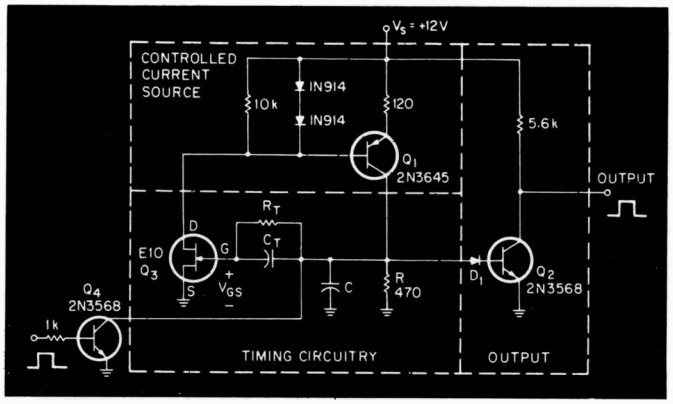
Current source improves immunity of one-shot

ONE-SHOT multivibrators with long time constants tend to be susceptible to false triggering from power supply line noise. This problem can be overcome by using a current source to isolate line noise from the timing circuitry.

Transistor Q_1 is a current source that supplies current to transistor Q_2 and resistor R. The voltage across R is held at 1.2 volts by diode D_1 and the V_{BE} drop of Q_2. Transistor Q_3 is a low-pinch-off FET (-0.3 volt for pinch off) and is normally conducting (V_{GS} = $+0.4$ volt) to keep the current source on. When a positive trigger pulse arrives at the input of Q_4, V_{GS} is driven negative to approximately -1.0 volt and the FET is nonconducting. Q_1 is thus turned off, and this turns off Q_2. Resistor R holds the timing line at low potential while Q_1 is nonconducting. When V_{GS} of the FET reaches about -0.3 volt due to the discharge of C_T, Q_3 conducts and turns on the current source. The circuit is now back in its steady-state condition, ready for another trigger pulse.

Capacitor C is needed to prevent misfiring from high-frequency noise spikes on the supply line. A value of 0.01 μF is sufficient for most purposes. Resistor R_T should be much larger than R, for proper operation. A minimum value for R_T is around 10 k. Because of this limitation, the one-shot is not capable of short-duration pulses (less than 50 μs). However, long-duration pulses can be obtained with relatively small capacitors. A time duration of 1 hour is obtained with R_T = 10 M, C_T = 330 μF.

This one-shot will operate over a wide power-supply voltage range. With the transistors shown, V_S may be as high as 40 volts or as low as 2 volts. If V_S changes from 40 to 4 volts, the timing period varies only 10 percent. Operating at a supply voltage of 20 volts, the circuit is unaffected by 15-volt noise spikes on the power supply line.



In this unusual one-shot, transistor Q_1 and capacitor C isolate the timing circuitry from transients on the dc line.

Simplified Schmitt yields fast rise time

THE BASIC Schmitt trigger seems such a straightforward circuit that one might ask how it could possibly be made any simpler. But for some applications, the component count can be further reduced to give improved results.

All capacitors can be eliminated, leaving a circuit with excellent performance at minimal cost. The circuit shown in Fig. 1 covers a frequency range of 10 Hz to over 100 kHz without adjustment of component values. Waveform is excellent at all frequencies, and both rise and fall times are less than 12 ns.

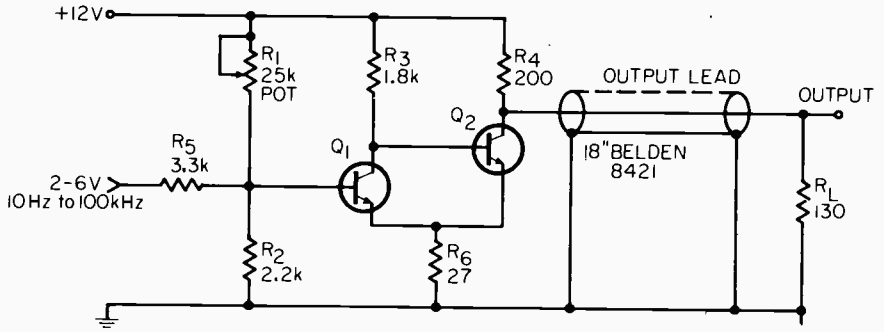


Fig. 1. Speed-up capacitors aren't necessary in this simplified Schmitt trigger that converts sine waves to clean square waves.

One practical application for the circuit is sine-to-square wave conversion. Used in conjunction with a low-cost audio generator, the circuit provides a wide-range square-wave signal source.

The speed-up capacitors, that are commonly used in Schmitt triggers, offer both advantages and disadvantages. They are useful in logic systems because they reduce the storage time of the semiconductor components. So they can provide increased switching speed in applications where speed would otherwise be limited by the transistors.

But speed-up capacitors do not alter the inherent rise and fall times of the circuit and its external impedances. In fact, they make it increasingly difficult to obtain good waveforms over a wide frequency range.

Elimination of capacitors in

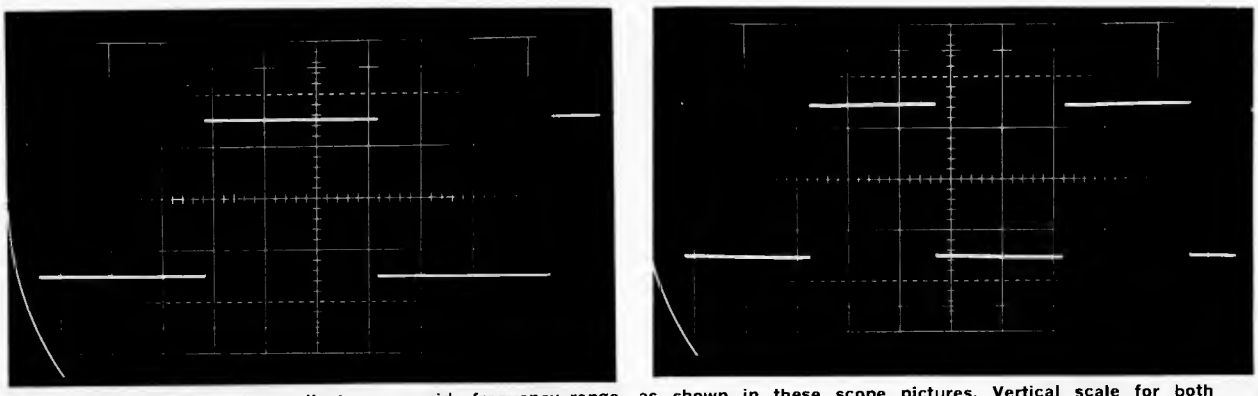


Fig. 2. Output waveform is excellent over a wide frequency range, as shown in these scope pictures. Vertical scale for both waveforms is 1 V/cm. Frequencies are 30 Hz (left) and 100 kHz (right). Horizontal scales are 5 ms/cm and 2 μs/cm respectively.

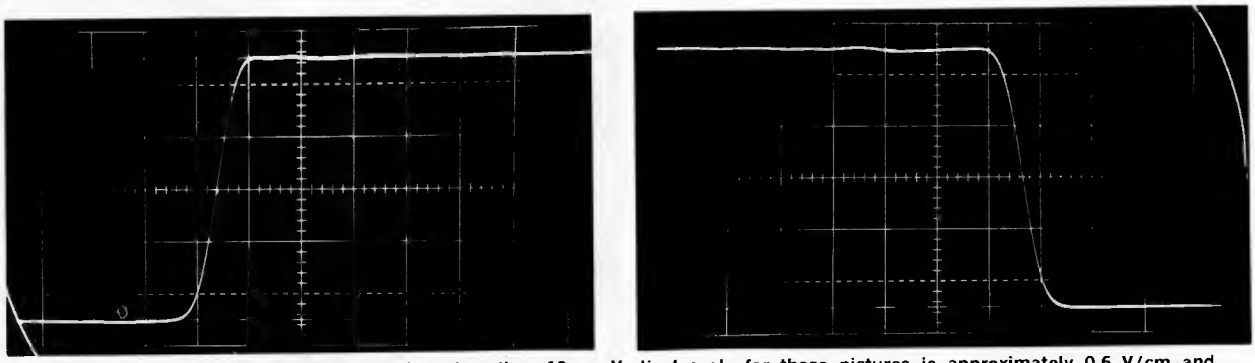


Fig. 3. At 100 kHz, rise and fall times are both less than 12 ns. Vertical scale for these pictures is approximately 0.6 V/cm and horizontal scale is 20 ns/cm. Rise and fall times are each 15 ns gross or 11 ns net (adjusting for scope response).

the circuit gives near-perfect waveforms over a wide range. Figure 2 shows the output square wave at 30 Hz and at 100 kHz. Fig. 3 shows expanded views of the leading and trailing edge of a 100-kHz output signal.

One other unusual feature of the circuit shown in Fig. 1 is that the load resistor is connected at the end of the output cable. This connection gives better results than the conventional approach. The Belden cable is specified because this has lower capacitance than most widely-available flexible cables. Length should not exceed eighteen inches, but this is probably adequate for most test-bench applications.

Lead dress and layout aren't very critical but output-cable length is critical. After the cable has been cut, the exact values of R_L and R_s should be determined for optimum fall time. The value of R_s is then chosen for optimum rise time. This resistor should be a 1-watt noninductive (composition) type.

Finally R_l is adjusted to give symmetrical square waves. Usually, no further adjustment is needed unless the input voltages are changed. Lower input voltages give faster rise times, and can be used when lower outputs are acceptable.

The transistors aren't too critical and low-cost types are usually adequate. Recommended types include TI 2N4418, TIS 48 or TIS 49; Fairchild 2N4275 or EN2369A; Motorola MPS2369. These are all epoxy equivalents of the 2N-2369.

Resonant clock-line driver for MOS ICs

THE CIRCUIT shown in Fig. 1 provides an efficient and economical way of delivering fast pulses to large capacitive loads. One useful application for the circuit is to provide clock pulses for cascaded MOS shift registers.

Circuit designers often need to connect a large number of MOS shift registers in series —to form delay circuits, for example. But a typical MOS register may need clock pulses of, say, 0.5 μs duration, with peak amplitudes up to 26 V. And the clock-line impedance is primarily capacitive. So, if one has, say, thirty cascaded registers with their clock lines in parallel, the total load capacitance for the clock driver may be as high as 2700 pF. This means that peak currents of up to 350 mA will be needed to generate a rise time of around 200 ns.

Complementary emitter-followers are commonly used as output stages for clock-line drivers. But these circuits can-

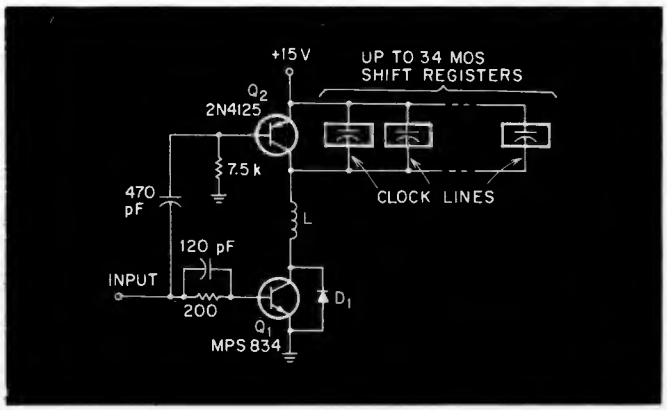


Fig. 1. In this unusual clock-line driver, inductor L forms a series-resonant circuit together with the load capacitance.

not work into large capacitive loads, because the transistors

are forced to operate continuously within their linear regions—thus the dissipation becomes excessive.

The circuit of Fig. 1, however, actually takes advantage of the load capacitance. Basically, the circuit consists of an inductor and a switch, connected in series with the clock line to form a series-resonant tank circuit. The switch is closed long enough to allow one half-sinusoid to be induced across the load; then it is opened, and another switch is closed, across the load, to terminate the half-sinusoid and prevent further oscillation.

Figure 2 shows the input and output voltage waveforms, and the current waveform. At time T_1, an input pulse turns on Q_1 and turns off Q_2. Current flows first down through the load, via the inductor and Q_1. Then the current reverses and flows back through diode D_1. At time T_2, the trailing edge of input pulse turns off Q_1 and turns Q_2 back on; this completes the output pulse and clamps the output to +15 V.

The input pulse width, or the value of the inductor, should be adjusted so that pulse duration is equal to the resonant half-period of the tank circuit.

$$T = \pi\sqrt{LC}_{load} \qquad (1)$$

Theoretically, the peak voltage across the load is 30 V, *i.e.*, twice the B+ voltage. But circuit losses prevent the output amplitude from achieving the full theoretical value. Typically, the output pulse has an amplitude of 25 V as shown in Fig. 2.

With the component values shown in Fig. 1, and with L = 6.8 μH, a total of 34 256-bit MOS registers have been operated at a clock frequency of 620 kHz. If the capacitive load is reduced, the clock frequency can be increased. For example, eight 128-bit registers have been operated reliably with a clock frequency of 4 MHz. In the latter case a 1-μH inductor was used.

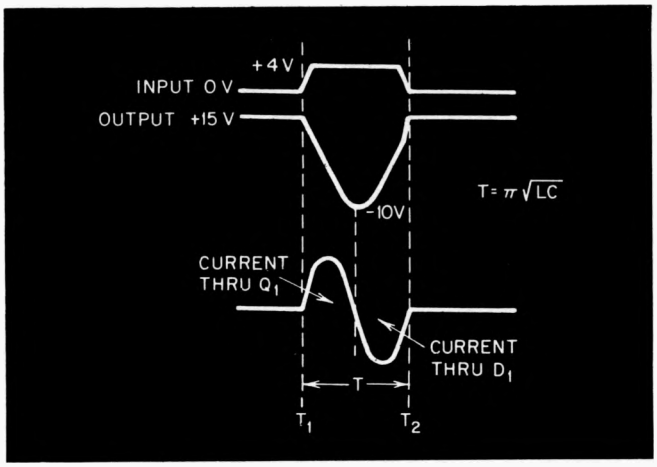


Fig. 2. Typical waveforms for the resonant line driver. During the positive half-cycle current flows through Q_1, and during the negative half cycle it returns via D_1.

High speed saturated-mode one-shot

THIS CIRCUIT offers better performance than currently-available IC one-shots which give minimum pulse widths of around 100 ns. An improved input-trigger circuit allows output pulse widths of less than 30 ns. Pulse width doesn't depend on the duration and amplitude of the trigger pulse.

With the components shown in Fig. 1, the circuit maintains a pulse width of 30 ns ± 5 ns over a temperature range of —55 to +80°C. For pulse widths greater than 200 ns, the variation is less than 1 percent over the same temperature range.

The circuit works as follows: Initially Q_1, Q_2, Q_4, and G_1 are all "on" and Q_3 is "off." A negative-going transition at the input then turns off Q_1. Since Q_2 emitter is now open-circuited, Q_2 turns off. This then turns off Q_4 and G_1, and turns on Q_3.

As Q_3 turns on, C_2 commutates and holds off Q_2 while the capacitor discharges through R_2. When the voltage at Q_2 base reaches the threshold level of the transistor, Q_2 turns on. The collector voltage of Q_2 then turns off Q_3 and turns on Q_4 and G_1.

Note that Q_1 turns on again before Q_2 does. Note also that C_1 is rapidly charged by an active pull-up TTL input. When Q_4 turns on, C_2 is rapidly charged by Q_4 thus providing fast recovery.

In designing this type of circuit, one should make sure that R_1C_1 is less than R_2C_2. The latter time-constant will then control the pulse width. Diode D_1 lowers the initial voltage across C_2 so that Q_2's base-emitter junction won't break down. (For the 2N2784, BV_{EBO} = 4 V.) The diode also compensates for the change in initial voltage across C_2 caused by the temperature drift of Q_2's base emitter "on" voltage.

Other one-shot circuits that are triggered by negative-going inputs, have the disadvantage that diodes and an extra capacitor must be included in the base circuit of Q_2. With these types of circuits, the

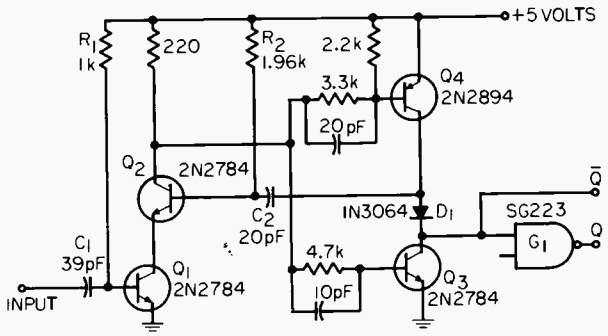


Fig. 1. The push-pull action of Q_3 and Q_4, and the unusual trigger circuit (Q_1, R_1, C_1), allows this one-shot to generate extremely fast pulses.

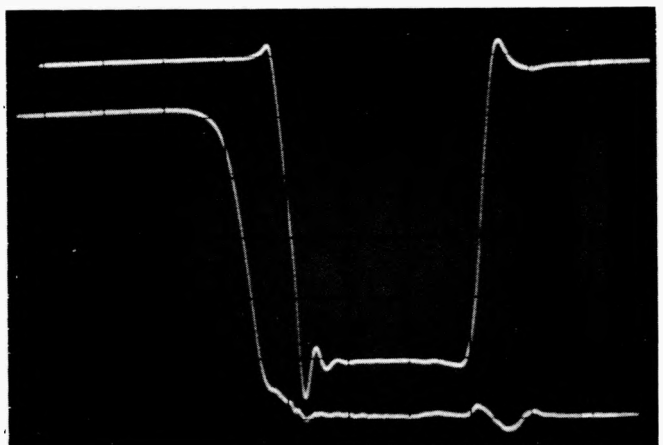


Fig. 2. Typical input (bottom) and output (top) waveforms for the circuit of Fig. 1. Horizontal scale is 10 ns/div. and vertical scale is 1 V/div.

trigger capacitor tends to partially discharge the timing capacitor, giving an output pulse whose width depends on the amplitude and duration of the trigger pulse.

With the arrangement shown here, however, the trigger circuitry (Q_1, R_1 and C_1) does not interact with the timing elements (R_2 and C_2).

Transistors Q_3 and Q_4 operate in push-pull so that the transistor turning on tends to pull the saturated transistor into its linear region. This arrangement minimizes storage time and provides a high-speed TTL-compatible output. Typical input and output waveforms are shown in Fig. 2.

The relationship between pulse width (in ns) and the value of C_2 (in pF) is given approximately by the following equation:

$$C_2 = \frac{\text{Pulse width}}{0.7\ R_2}$$

(where R_2 is expressed in kΩ).

Though described here as a discrete-component circuit, the high-speed one-shot can also be built as a hybrid or monolithic IC. Note, though, that Q_4 is a pnp transistor, so it wouldn't be economically feasible to include it on the same monolithic chip.

Two-Pulse Monostable

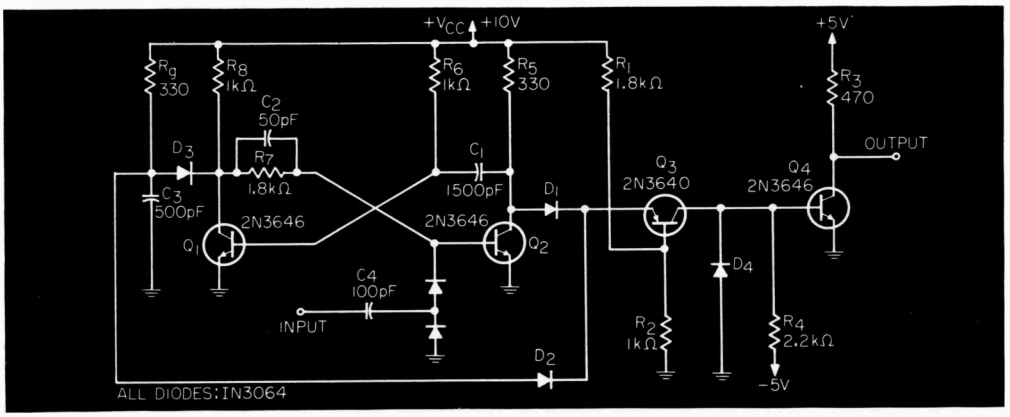


Fig. 1. Modified monostable gives two pulses for each input trigger pulse.

THE MODIFIED monostable shown in Fig. 1 gives two pulses instead of one. The duration of the pulses and the interval between them are all independently adjustable. Fig. 2 shows the output waveform. The first output pulse is triggered by the input pulse, and T_1, T_2 and T_3 are adjustable. The circuit shown is much simpler than the conventional approach, which would require three one-shots to generate the same output.

Initially Q_1, Q_3 and Q_4 are "on" and Q_2 is "off." Capacitor C_1 is fully charged and C_3 is discharged. Transistor Q_3 clamps the collector of Q_2 via D_1.

When the input pulse triggers the monostable, Q_2 turns "on" thus turning Q_1 "off." But until C_3 charges, both inputs to D_1 and D_2 are below the threshold of Q_3 set by the divider R_1 and R_2. Thus Q_3 and Q_4 turn "off."

Capacitor C_3 now charges until it is clamped by Q_3, turning Q_3 and Q_4 "on." When the monostable "times out" it regenerates to its initial state with Q_1 "on" and Q_2 "off." This discharges C_3 and turns Q_3 and Q_4 "off" again.

Capacitor C_1 now recovers through R_5 until the threshold of Q_3 is exceeded. This again turns on Q_3 and Q_4, clamping the collector of Q_2.

Thus two pulses are generated from a single one-shot. Components R_6 and C_1 determine T_3, recovery of C_1 through R_5 determines T_2, and the charge time of C_3 through R_9 determines T_1. Equations 1, 2 and 3 give the values of T_1, T_2 and T_3 respectively.

Diodes D_1 and D_2 isolate the collectors of Q_1 and Q_2. Resistor R_4 provides a reverse current to speed the turnoff of Q_4. Diode D_4 provides a protective clamp to limit the reverse bias applied to Q_4.

$$T_1 = R_9 C_3 \ln\left[\frac{V_{cc}}{\frac{V_{cc}R_1}{R_1+R_2} - V_{BE3} - V_D}\right] \simeq R_9 C_3 \left[\frac{R_1+R_2}{R_1}\right] \quad (1)$$

$$T_2 = R_5 C_1 \ln\left[\frac{V_{cc}}{\frac{V_{cc}R_1}{R_1+R_2} - V_{BE3} - V_D}\right] \simeq R_5 C_1 \ln\left[\frac{R_1+R_2}{R_1}\right] \quad (2)$$

$$T_3 = R_4 C_1 \ln\left[\frac{\left(\frac{2R_2+R_1}{R_1+R_2}\right)V_{cc} + V_D}{V_{cc} - V_{BE(Thres)}}\right] \simeq R_4 C_1 \ln\left(\frac{2R_2+R_1}{R_1+R_2}\right) \quad (3)$$

Where $V_D = D_1$ or D_2 "on" voltage drop.

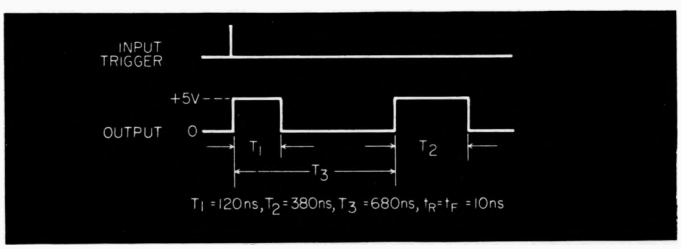


Fig. 2. Each of the durations T_1, T_2 and T_3 is adjustable. Typical times are shown, using the component values of Fig. 1.

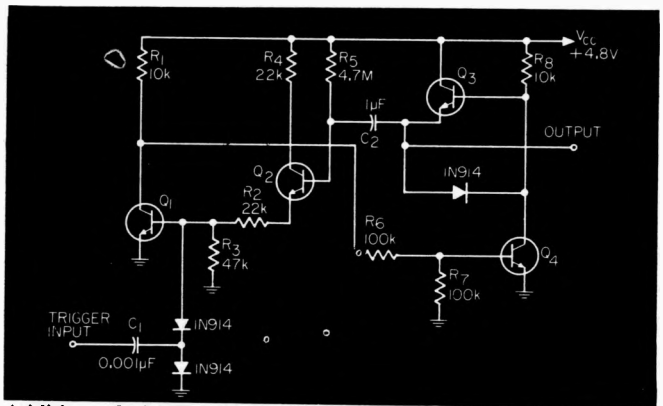
Extra transistor provides noise immunity for monostable multi-vibrator

THIS CIRCUIT is a conventional one-shot multivibrator with some added components. These components (Q_2, R_2 and R_4) eliminate one of the major disadvantages of the conventional circuit.

First, imagine that C_2 and R_5 are connected directly to the base of Q_1 in the usual way. Then, since Q_1 is normally saturated, negative-going pulses are required for triggering. They are usually applied to Q_1 base. The circuit is then very susceptible to triggering by negative-going pulses which may be coupled to Q_3 emitter either from the V_{cc} line or directly from the output.

But, with the improved circuit, Q_2 emitter is operated above ground to give noise immunity at Q_3 emitter. The steady gate-emitter voltage of Q_2 is that needed to saturate Q_1, plus the desired noise immunity. With the component values shown for R_2, R_3 and R_4, noise immunity at Q_3 emitter is 0.5 V. The corresponding trigger voltage, for the conventional circuit, at the same point is about 0.01 V. Though the modification raises the required trigger level at Q_3 emitter, it causes no change in the input-trigger sensitivity.

Addition of Q_2 gives an added bonus. Because of the current gain of Q_2, the maximum value of R_5, to allow complete saturation of Q_1, is much larger. Thus the output-pulse width can be much greater, with a given practical capacitor. Pulse width is approximately equal to $0.7 \times R_5 \times C_2$. With the values shown, pulse width is about 3 seconds.



Addition of Q_2, R_2 and R_4 to a conventional monostable multivibrator raises the noise immunity without affecting input sensitivity.

Zero (quiescent) power one-shot

THE ONE-SHOT in Fig. 1a, unlike the conventional text-book circuit, draws no standby current in the normal or off mode. This zero-power one-shot uses the holding-current technique for turning off an SCR.

When either a dc level or an ac-coupled pulse turns on SCR, CR_1, an exponentially decaying current I_B flows. This sustains $\beta I_B = I_0$ collector current which is designed to be greater than the SCR holding current. As I_B becomes smaller than the SCR holding current, the regenerative action cannot be sustained and the SCR turns off. Resister R_c limits I_1 to less than the SCR holding current. R_3, R_4 are leakage-protection resistors. Capacitor C_2 protects the SCR gate from noise spikes.

The on time of the one-shot is a function of the β of Q_1, and the holding current of the SCR, CR_1. Table 1 shows typical on time versus τ, (R_1C_1).

Advantages of this one shot are:

1) Addition of a resistor and a diode will provide a very fast rising edge at point A in addition to the fast falling edge at point B for signal purposes (see Fig. 1b).

2) Longer on time is possible because the on time is proportional to n where n can be designed greater than 2 instead of the conventional 0.69.

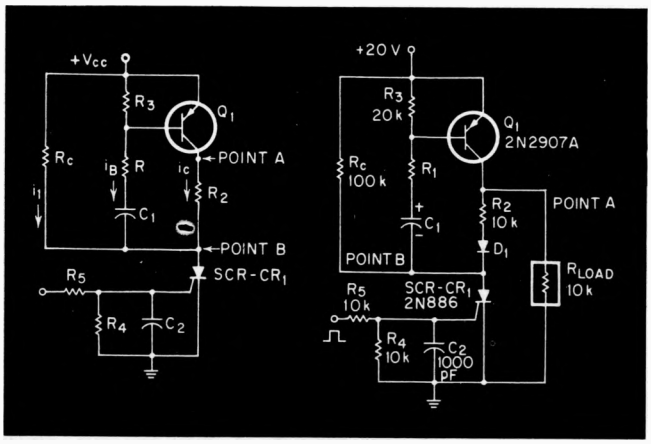
3) $+V_{cc}$ is not a limitation in this circuit because of V_{BE} reverse breakdown.

4) There is an inherent lockout feature. Trigger pulses can occur and not affect the on time of the one shot because of the latched-on SCR.

5) The circuit can be used as signal one shot or power one shot by driving a load off the collector of Q_1 as in Fig. 1b. If the load on time is required to be T seconds then the one-shot time constant should be $3T$ or $4T$ so that Q_1 can be assured of saturation for the first time constant.

Table 1. τ vs. measured on time

τ	R_1	C_1	Measured On Time
100 ms	10 k	10 uF	270 ms
10 ms	10 k	1 uF	27 ms
1 ms	10 k	.1 uF	2.7 ms
100 ms	5 k	20 uF	370 ms
10 ms	5 k	2 uF	.37 ms
1 ms	5 k	.2 uF	3.7 ms
100 ms	1.k	100 uF	550 ms
10 ms	1 k	10 uF	55 ms
1 ms	1 k	1 uF	5.5 ms



Zero standby current one-shot in signal (a) or power (b) configurations.

IC one-shot needs no external resistors or capacitors

WHEN MONOSTABLE multivibrators are needed in an IC system, circuit designers usually add an RC feedback network to a clocked flip-flop to achieve the necessary delay. But if only short pulses are required (for example, when strobes are generated from logic-level transitions), cascaded inverters can be used instead of resistors and capacitors. The advantage of the latter approach is that it employs ICs instead of discrete components. Thus it simplifies packaging.

Economical multi-gate ICs (such as hex inverters) are ideal for this approach. Both RTL and DTL circuits are suitable; the circuit of Fig. 1 uses DTL. The number of inverters cascaded in the path from the input to the flip-flop's direct-set terminal must be even for DTL and odd for RTL.

In Fig. 1, the steering inputs to the clocked flip-flop (which can be J-K or R-S) are so arranged that the flip-flop will assume the zero state t_{pdf} seconds after a negative clock transition. With the DTL flip-flop shown, this time is 15 to 55 ns for the negative transition at $\overline{Q}$ output and 25 to 75 ns for the positive transition at the Q output.

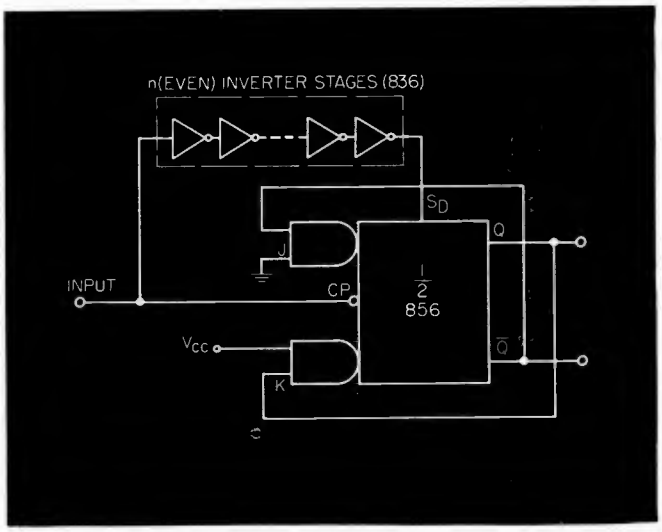


Fig. 1. This simple one-shot uses the propagation delay of cascaded inverters, instead of an RC network, to define its recovery time.

After a negative clock transition, the direct set terminal S_D of the flip-flop stays high for t_{pdi} seconds. This period is the overall propagation delay through n cascaded inverters. At the end of the delay, the voltage at S_D goes low, forcing the flip-flop into the "1" state where it will remain until the next negative clock transition.

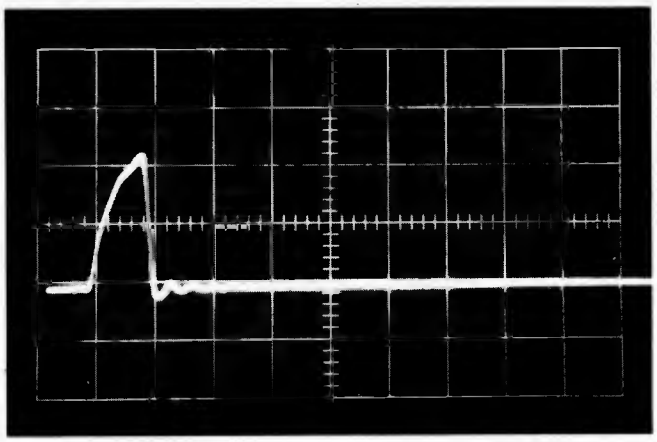
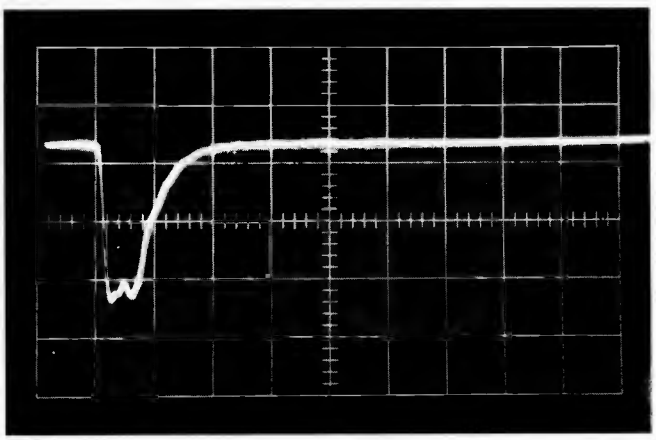


Fig. 2. Typical output waveforms from the $\overline{Q}$ terminal (top) and the Q terminal (bottom). Vertical scale is 2 V/div and horizontal scale is 100 ns/div.



Obviously one should use enough inverters to ensure that the total delay t_{pdi} is greater than t_{pdf}, the delay through the flip-flop. For example, in the DTL circuit shown, where inverter propagation delay is between 25 and 80 ns per stage, a minimum of six inverter stages would be required to produce a pulse from both outputs of the flip-flop under worst-case conditions. In practice, however, 50-100 ns pulses at repetition rates from zero to 9 MHz have been obtained with as few as two inverters.

Figure 2 shows typical output waveforms for the circuit of Fig. 1. For the test, four inverters were connected between the clock input and the direct set terminal of the flip-flop. ■

An inexpensive frequency doubler

THE STANDARD transition detector (Fig. 1), which detects pulse transitions in only one direction, can be made into a frequency doubler. This change can be instrumented by changing the NAND gate at the output of Fig. 1 to an exclusive OR gate (Fig. 2). This modification allows the new circuit to detect pulse transitions in either direction. The width of the output pulse is determined by the delay in the inverters. If longer pulse widths are desired, a feedback capacitor (shown by the dotted lines in

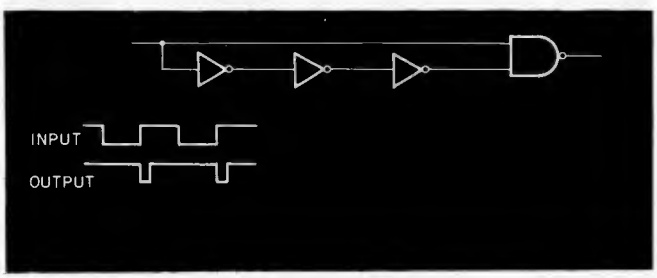


Fig. 1. This is the circuit of a transition detector using IC logic gates.

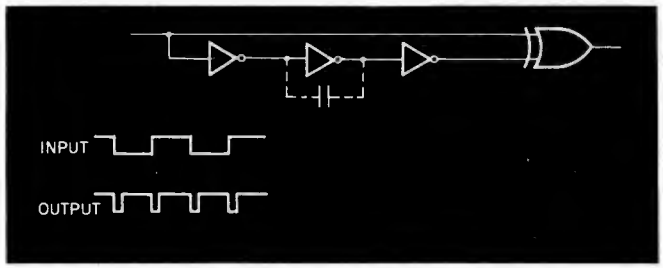


Fig. 2. Changing the output NAND to an exclusive OR converts the circuit to a frequency doubler.

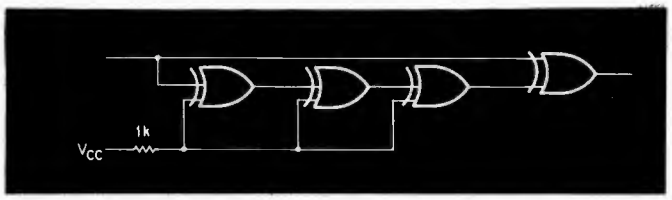


Fig. 3. The circuit of Fig. 2 can be instrumented in a single quad-exclusive OR IC.

Fig. 2) may be added. The availability of quad-exclusive OR gates enables the designer to implement the frequency doubler in one package as shown in Fig. 3. These gates are available in both TTL and DTL. ■

Single NAND package improves one-shot

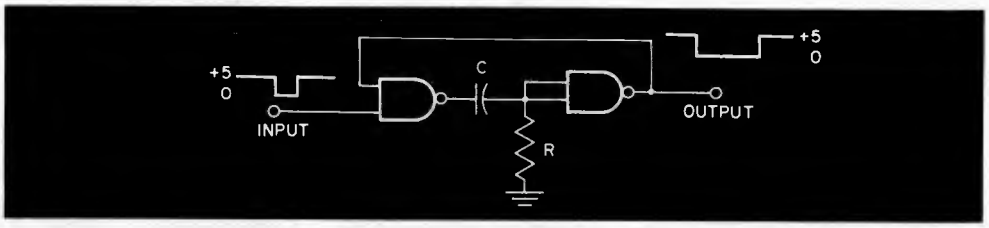


Fig. 1. The typical NAND one-shot suffers the likelihood of output instability and oscillation.

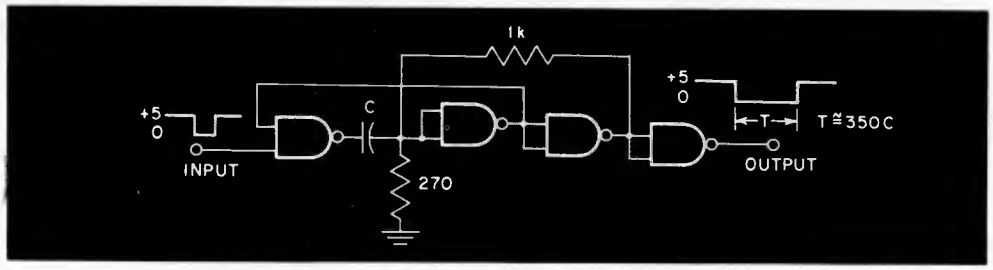


Fig. 2. Improved NAND one-shot provides cleaner, more stable output.

THE OUTPUT PULSE of the typical NAND one-shot of Fig. 1 is often subject to oscillation and pulse-width instability. Further, the range of pulse widths is sometimes quite limited.

The NAND one-shot in Fig. 2 overcomes these difficulties. The 1- kΩ feedback resistor eliminates the tendency to oscillate and the additional output gate provides more squaring of the output pulse.

All four NAND gates are part of a TI SN7400 package. With these gates, the output width, T, equals 1.3 RC and, with $R = 270\Omega$, this simplifies to $T = 350\ C$.

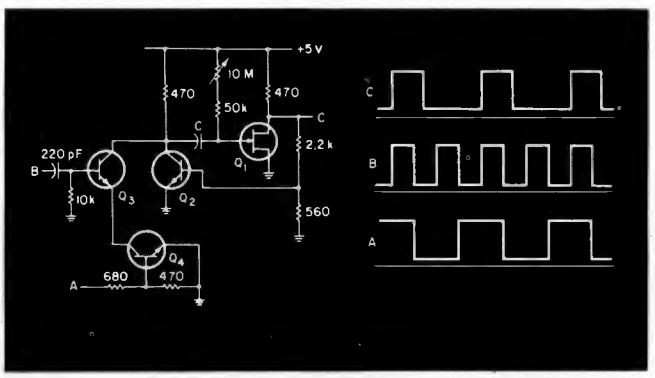
Input pulse widths longer than 30 ns can initiate an output. Timing capacitors ranging from 100 pF to 100 μF have been used successfully. ■

Versatile one-shot

THIS CIRCUIT uses standard digital-IC voltage levels as inputs and can be inhibited or enabled at any time without causing an output. Duty cycle approaches 98 percent at trigger rates of 500 kHz.

Comparable IC monostables are limited to 50 percent duty cycle and are noise sensitive during long pulse times. Also, IC monostables may trigger on an inhibit command unless the inhibit occurs during the one-shot period.

The input gate (Q_3 and Q_4) is enabled with a logical 1 at point A and inhibited with a 0 at the same point. If the inhibiting function is not needed, the emitter of Q_3 should be grounded and Q_4 omitted. A logical 1 at point B starts a timing cycle. Q_1 is a 2N3819 JFET while all other transistors are 2N3704s. ■



Versatile one-shot mono may be enabled or inhibited at any time without a false output.

Simple one shot has complementary outputs

THE CIRCUIT SHOWN in Fig. 1 is a one-shot multi that is capable of being pulse-width modulated. The circuit is actuated by a strobe input to G_1 which drives the output of G_1 to binary 0. This level turns Q_1 off and allows the voltage across C_1 to build up according to $V_{C1} = it/C_1$. At a specified time, unijunction Q_3 will fire discharging C_1. The output of the UJT drives the output of G_2 to binary 0. Fig. 2 is a timing diagram of circuit operation.

Q_2 is a linear current source to charge C_1. Since Q_1 is normally on, the current of Q_2 is bypassed to ground thru Q_1. V_C determines the amount of current delivered to C_1. Linearity of 0.1% has been achieved with this circuit. Replacing the current source with an op-amp single-ended current pump increases the linearity to 0.02%.

The duty cycle (not repetition rate) is determined by the speed of the logic used and the saturation storage time of Q_1. Q_1 may be replaced by an hex inverter with an uncommitted collector (SN7405N-J) for increased speed. The control voltage V_C, determines the amount of current to C_1 and therefore controls the output pulse width. The scale factor of supply voltage V_C is controlled by resistors R_3 and R_2. ■

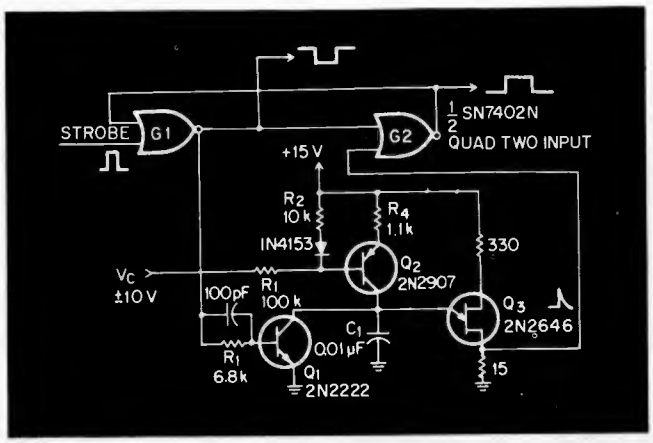


Fig. 1. This one shot is capable of being pulse-width modulated by V_c. It is capable of high duty cycles and can supply complementary outputs.

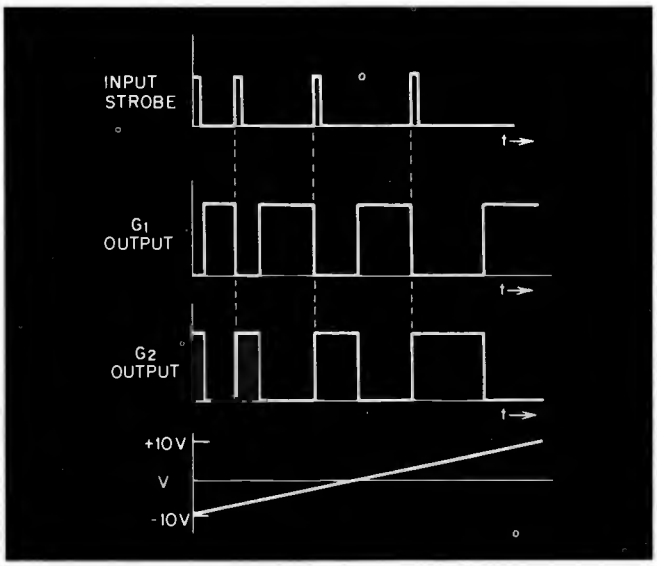


Fig. 2. Timing diagram of circuit operation. Note that the control voltage is bipolar.

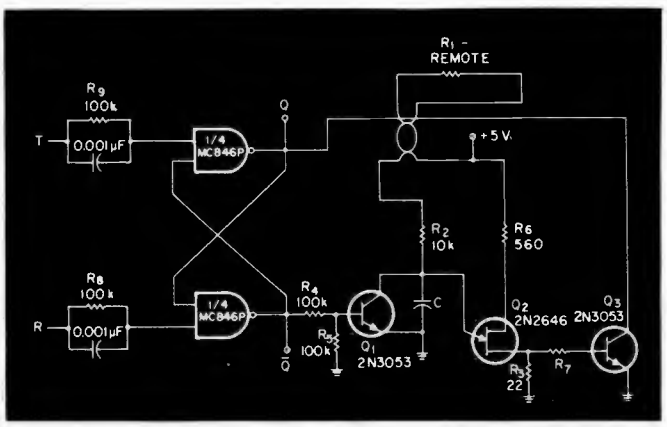
Resettable one-shot with high noise immunity

IT'S OFTEN necessary to vary the firing time of a one-shot from a remote point. In conventional one-shot circuits, if an external timing resistor is more than a few inches from the card rack, random noise can fire the circuit. In the circuit shown here, noise won't fire the one-shot, even with the timing resistor several feet from the logic chassis. Noise immunity is equal to that of a flip-flop.

If one wants to reset this one-shot during its firing cycle, it is merely necessary to apply a logic 0 to the reset input.

If we assume the flip-flop, made of two NAND gates, is in its reset state, Q is at logic 0 and $\overline{Q}$ is at 1. The 1 from $\overline{Q}$ holds Q_1 on, which holds R_1, R_2 and C at ground, thus preventing Q_2 from firing. When a 0 pulse is applied to the trigger input, the flip-flop changes state and $\overline{Q}$ goes to 0 and Q changes to a 1. With $\overline{Q}$ at a 0, Q_1 is turned off.

C charges through R_1 and R_2. When C charges to a voltage set by the intrinsic standoff ratio of the unijunction transistor, Q_2, it fires. A voltage is developed across R_3, turning Q_3 on for approximately 500 μs. This brings the Q output of NAND 1 to ground, thus resetting the flip-flop. The Q returns to a 0 and $\overline{Q}$ returns to a 1. The length of firing time may be computed from $T = C(R_1 + R_2)$. ■



The timing resistor for this resettable one-shot can be several feet away from the circuit without allowing noise to fire the circuit.

Ultralow-duty-cycle pulser

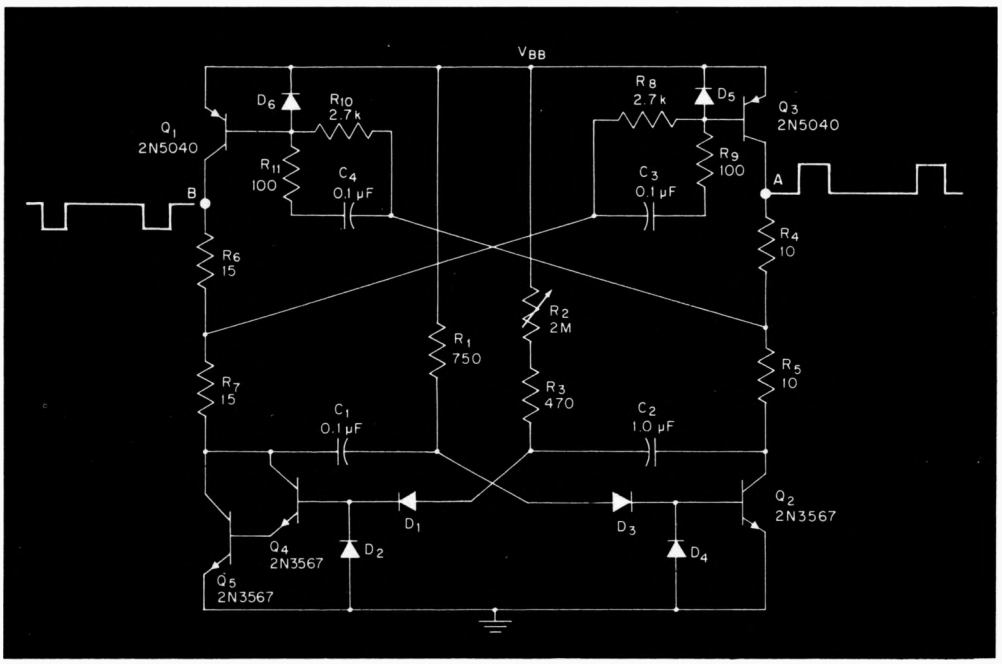
IT'S OFTEN necessary to generate a fast-rise pulse (or a train of pulses) whose width is very short relative to the overall period or rep rate. The circuit shown provides a period-to-pulse ratio of 30,000 to 1.

The timing circuits R_1, C_1 and R_2, R_3, C_2, are those of a standard multivibrator. Resistors R_4, R_5, R_6, and R_7 limit the current during the switching period and must be divided as shown for controlling the base drive of Q_1 and Q_3. R_9, C_3 and R_{11}, C_4 are speed-up circuits to enhance switching and provide drive for the heavy currents through Q_3 and Q_1 during the switching interval. Q_4 is required in a Darlington arrangement with Q_5 only because of the high resistance of R_2. With low-leakage transistors, a third transistor may be added and R_2 increased to 10 megohms to provide period-to-pulse width ratios as high as 100,000:1.

During operation, Q_1 and Q_2 are simultaneously in either the on or off state, with Q_3, Q_4 and Q_5 all in the state opposite to that of Q_1 and Q_2. Thus as Q_4 and Q_5 start to turn on, Q_2 is turned off and Q_3 is turned on, turning Q_1 off. It is not necessary to have D_6, R_{11} and C_4 in the circuit if an output is required only at A. If V_{BB} is equal to or less than the transistor base-emitter breakdown voltage, all diodes can be eliminated.

This circuit can be used as an astable, monostable, or bistable multivibrator by making R_1 a potentiometer. This also allows variation of pulse width. For the circuit shown, the pulse width is 50 microseconds, with a rise time of 200 nanoseconds, a fall time of 20 nanoseconds and periods ranging from 500 microseconds to 1.5 seconds. The pulse width and period can be scaled up or down while still realizing ratios of 10,000 or more.

The versatility of the circuit allows extremely low impedance drive for the complementary outputs at points A and B, while maintaining very low power consumption. If Darlington connections are made at all four corners of the circuit, the current required can be less than 1 mA. ■



This circuit generates fast-rise pulses with widths very short relative to periods. All diodes are 1N4148.

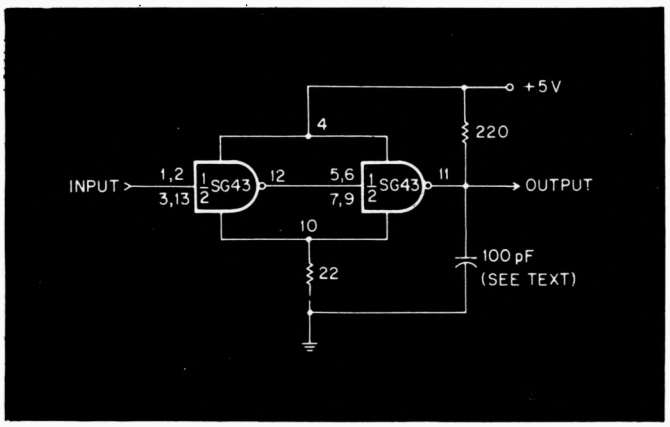
Schmitt trigger uses two logic gates

TWO TTL INVERTERS and a few components are used in the figure to form a Schmitt trigger. The gates may be any type of TTL inverter. They are connected in series with a small-value feedback resistor in the common power-supply ground lead.

The cascade connection of the gates causes them to always be in opposing logical states. This causes a constant voltage drop across the 22-Ω resistor. This drop results in a constant offset voltage. The addition of a second resistor at the output terminal corrects this situation. The extra current drawn through the output resistor, when the second gate is in the zero state, causes an increase in the feedback voltage. This enhances the switching speed of the first gate.

With the values shown, the circuit has a positive-going threshold of 2.4 V and a negative-going threshold of 2.0 V. Threshold values and hysteresis can be changed slightly by varying the external resistors.

The normal load capacitance at the output results in ac feedback. If the actual application does not provide sufficient output capacitance, it may be necessary to add a 100 pF from output to ground. ■



This Schmitt trigger is made from two TTL gates.

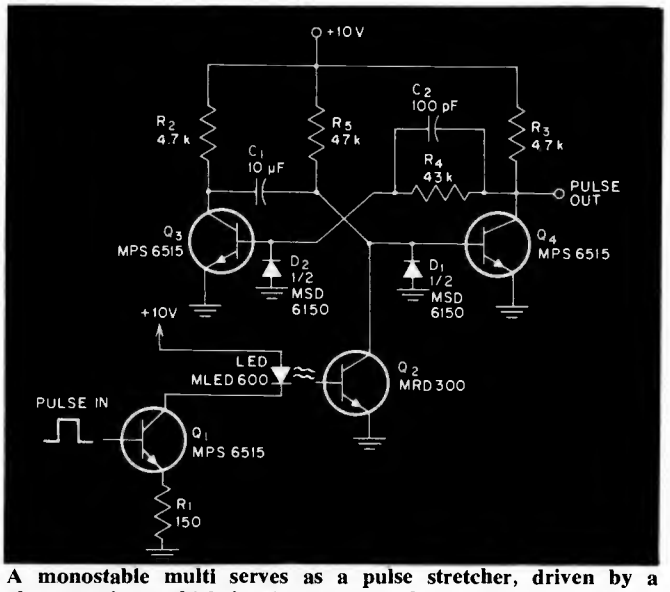
Optically driven pulse stretcher

A LIGHT-EMITTING diode and a phototransistor can be used to drive a pulse stretcher, as in Fig. 1. In this circuit, Q_4 is the normally-on transistor in a monostable multi.

When an input pulse drives the LED, phototransistor Q_2, which is photon coupled to the LED, causes Q_4 to turn off and Q_3 to turn on.

The base of Q_1 is held to $V_{CE(SAT)}$ of the phototransistor until the input pulse drops to zero. At this time C_1 begins to change toward +10 V. When the base of Q_4 reaches about 0.6 V, the circuit resets and Q_4 comes on while Q_3 goes off. The delay, or "stretch" time, after the trailing edge of the input pulse is a function of the R_5C_1 time constant, the supply voltage, the phototransistor saturation voltage and the turn-on voltage of Q_4.

For the values shown, a 3-μs input pulse creates a 55-ms output pulse with an amplitude from $V_{CE(SAT)}$ to V_{CC}. ■

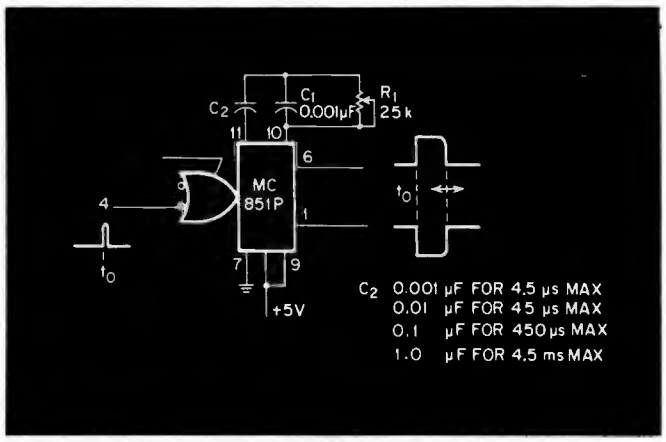


A monostable multi serves as a pulse stretcher, driven by a phototransistor which is triggered by light coupled from a LED.

Wide-range variable pulse-width monostable

A SLIGHT CHANGE in the external circuitry of the Motorola MC851P monostable permits wide-range continuous operation. The unmodified MC851P gives complementary output pulses that can be adjusted by the addition of external capacitors. The use of the recommended range of external variable resistor permits a pulse-length adjustment of only ±15%. This new circuit variation considerably extends this range (4.5 μs - 4.5 ms).

The change, as indicated on the circuit diagram, permits operation over a continuously variable range. C_2 is varied in order to cover a wide range of pulse widths. C_1 prevents rounding off of the trailing edge of the pulse as R_1 is increased. With the value of C_1 shown (0.001 μF), minimum pulse length is 4.5 μs. Rise and fall times of the output pulse are better than 100 μs. ■



A simple modification of the MC851P monostable extends output pulse widths from 4.5 μs to 4.5 ms.

High-speed, one-IC one-shot

USING a single, DTL or TTL quad 2-input gate, the circuit in Fig. 1 generates a short-duration pulse that can be extremely useful as a strobe or reset signal. It's a modified set-reset latch that generates a pulse that lasts slightly longer than three propagation times, typically 40 to 70 ns.

A single pulse is generated each time a command is given, regardless of its duration. The width of the output pulse can be extended up to 500 ns by adding a capacitor, C_x, at terminal Q. ■

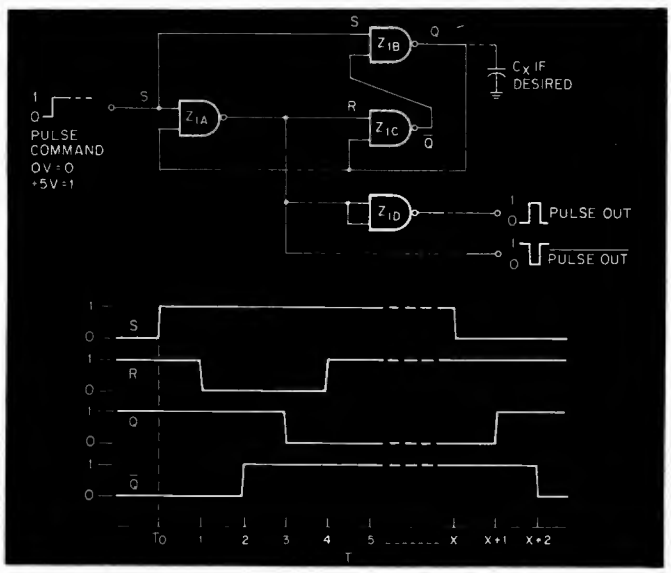


Fig. 1. (Top) An input command of any duration generates a single output pulse.
Fig. 2. Timing diagram shows pulse widths, which depend on propagation delays of the individual gates. Widths can be extended by adding a capacitor. Timing is expressed in propagation times.

Section 6
COMPARISON CIRCUITS

Transistor Go-No Go Voltage Comparator

MANY APPLICATIONS arise where an unknown voltage must be compared to a standard voltage within certain preset voltage limits. The accompaning schematic shows a go-no go transistorized voltage comparator that will perform this function.

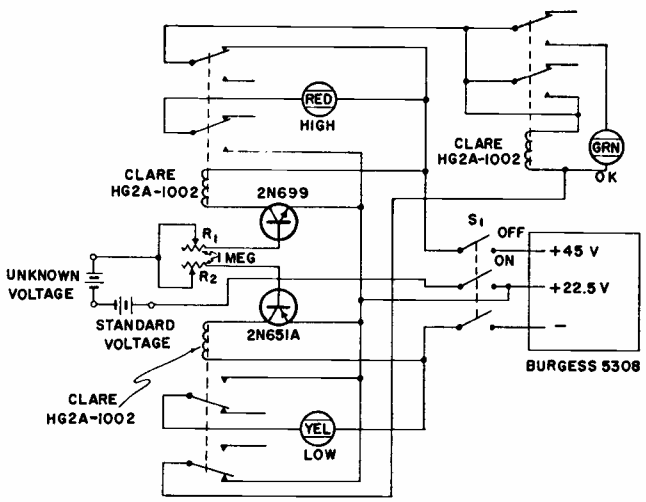
This circuit contains few components and is relatively inexpensive to build. The entire circuit contains only transistors, two potentiometers, three relays, three indicator lamps, a triple-pole double-throw switch and a battery.

Each transistor is forward biased so that 1 ma of base-to-emitter current will drive the transistor into saturation, closing the relay in the collector circuit to light an indicator light.

Potentiometers R_1 and R_2 are adjusted to allow 1 ma of base-to-emitter current to flow in both transistors at the preselected high and low limits that the unknown voltage may differ from the standard voltage.

The "O.K." indicator lamp is wired to light when switch S_1 is closed and less than 1 ma of base-to-emitter current flows in either transistor. When switch S_1 is closed one of the three indicator lamps should always light thus indicating that the battery is in good condition.

In the circuit that was constructed the voltage comparator was found to be sensitive enough to detect as low as 0.5 v difference between the standard and unknown voltage. Better sensitivity can be obtained if a germanium npn transistor with a low base-to-emitter voltage drop is used instead of the silicon 2N699 transistor.



Go-no go voltage comparator circuit. Transistors must be mounted on heat sink.

A Phase Discriminator

THE CIRCUIT illustrated in Fig. 1 will deliver half-wave pulses to only one of the two loads as determined by in-phase or 180-degree phase difference between the input signal and the reference source. This circuit is useful where different devices, such as heating and cooling equipment, are to be actuated upon a change of signal phase. The components are not critical, being limited only by their maximum ratings. The particular choices in Fig. 1 were made purely on the basis of availability. The waveforms are shown in Fig. 2, while the rms voltages are given in Fig. 1.

For in-phase signals, the voltage at the collector is clamped to ground for the positive signal half-cycle, and no signal appears at either load. During

the negative half-cycle the emitter-base junction of the transistor is reverse biased, unclamping the collector. Thus the negative signal half-cycle, passed by D_2, appears across R_{L2}.

For out-of-phase signals, both the collector and emitter junctions are forward biased during the negative half-cycle of the signal, thus clamping collector to ground. During the positive half-cycle of the signal the reverse biased emitter junction allows the signal to remain un-clamped. Diode D_1 conducts and the positive half-cycle appears across R_{L1}.

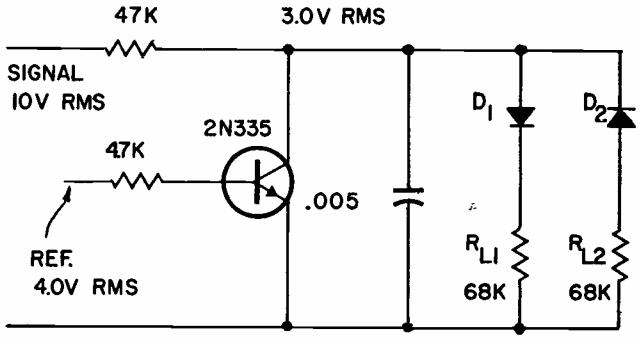


FIG. 1—Voltage appears across either of the two load resistors depending upon polarity of input signal.

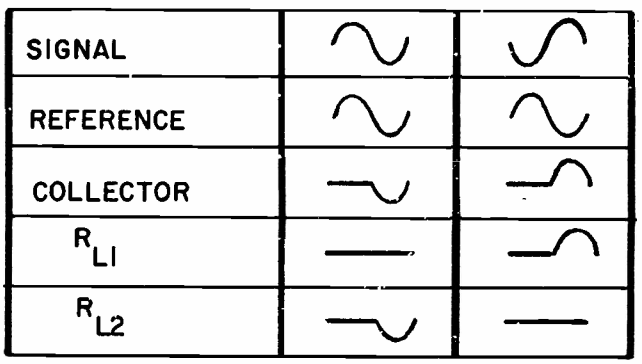


FIG. 2—Waveforms at various points of phase discriminator circuit.

The capacitor has been added to smooth out the small transient spikes during the switching periods.

Pulse Amplitude Evaluator

THE CIRCUIT shown in Fig. 1 was devised to locate pulses falling within a given range of amplitudes, rejecting all others falling above or below the preset limits of acceptance. The evaluation may be performed at any required level, with the upper and lower limits of acceptance variable to the desired range.

Unless the input is derived from a dc amplifier, it is necessary to restore the base line to a fixed reference, in this case, +12 v. A common-base transistor configuration, Q_1, is employed for this purpose rather than the more conventional junction-diode clamp. The impedance looking into the emitter of Q_1 will be less than the forward resistance of a diode by a factor of approximately $(1 - \alpha)$, allowing more complete clamping action and minimum base-line drift with large signal, high duty-ratio pulse trains.

The signal is then fed to the unity-gain phase splitter Q_2, resulting in equal amplitude, opposite polarity pulses at the collector and emitter. Diode D_1 at the collector is reverse biased by the voltage divider R_4, R_6, and the input impedance of Q_3. In this case the latter is quite small compared to R_6,

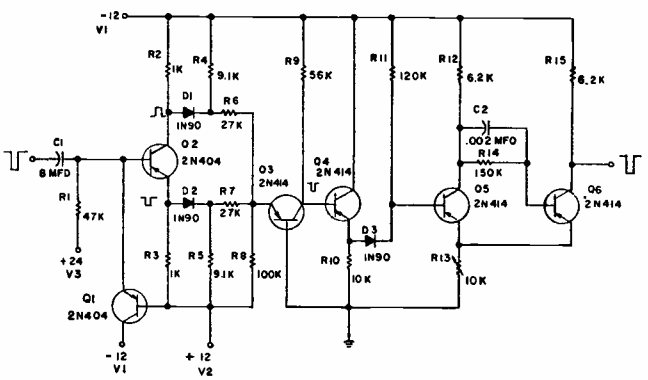


FIG. 1—Circuit of pulse amplitude evaluator.

(less than 150 ohms), and may be neglected. The value of R_4 may be calculated by:

$$R_4 = R_6\left(\frac{V_e}{V_1 - V_e}\right)$$

Where: V_e = amplitude at the midpoint of the acceptance range.

Thus, the cathode of D_1 is clamped at V_e until the input rises beyond V_e, when D_1 becomes forward biased, and the cathode is allowed to follow the input signal.

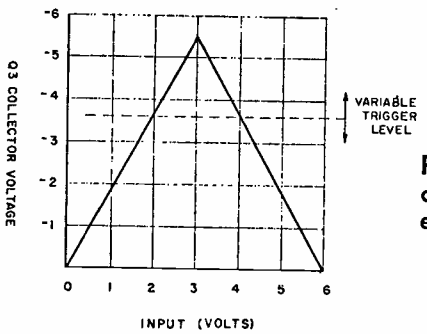


FIG. 2 — Transfer characteristic of evaluator.

Conversely, D_2 is forward biased by the voltage divider R_5, R_7, and the input impedance of Q_3, which may again be ignored. Resistor R_5 may be calculated by:

$$R_5 = R_7\left(\frac{V_e}{V_2 - V_e}\right)$$

Unlike D_1, the voltage at the cathode of D_2 will

follow the input signal until the threshold point V_e is reached, at which time D_2 is reverse biased and the cathode is held at V_e as the input continues to increase.

The resulting pulses at R_6 and R_7 are then added algebraically and amplified in Q_3. The transfer characteristic of this portion of the circuit is shown in Fig. 2. In this application, V_e was set to 3 v.

From this point the pulses are fed to emitter follower Q_4 and Schmitt trigger Q_5—Q_6 where acceptance levels are set by adjusting R_{13}. Thus, the trigger circuit will fire only when the pulses appearing at the input are within the desired latitude of peak amplitude.

If it is desired to retain the original amplitude information, the Schmitt output can be used to enable an AND gate as shown in Fig. 3.

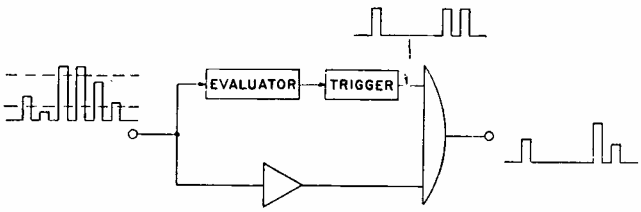


FIG. 3—Technique for retaining original pulse information using pulse evaluator to enable an AND gate.

Frequency Comparator Detects Coincidence Within 10^{-6}

THIS CIRCUIT is designed to detect frequency differences, to an accuracy of one part per million, between two separately derived signals of the same frequency. The frequencies that can be compared range from 60 kc: 60 kc to 1.2 mc: 1.2 mc. This is by no means a limiting range, but merely represents the range tested.

The frequency difference can be measured in any one of two ways, depending on equipment available. The first method is indicated by the block diagram of Fig. 1A where the time interval between one cycle of the difference frequency is counted. The second method is indicated by the block diagram of Fig. 1B, where the meter will deflect each time the difference frequency begins a cycle. A stop watch can be used to measure the time between deflections, the time being = period of the difference frequency.

The circuit operation for the first method does not require any circuitry to the right of dashed line *a.a* in Fig. 2. Its operation is as follows: Q_1 is used to modulate f_2 by f_1 to obtain a beat note between f_1 and f_2. The amplitude of $f_1 = f_2 = 0.75$v rms. Beat note f_d is detected at point *c* by the *LC* network which is a low pass 1-kc filter.

Q_2 and Q_3 provide dc amplification for f_d. During the positive half cycle of f_d, Q_2 is biased so that it will be saturated and Q_3 is biased so that it will

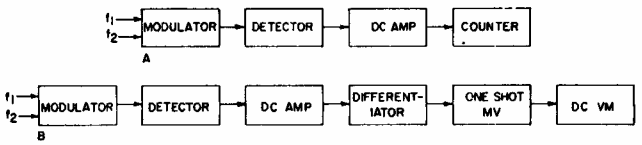


FIG. 1—Two arrangements for measuring frequency difference to one part per million.

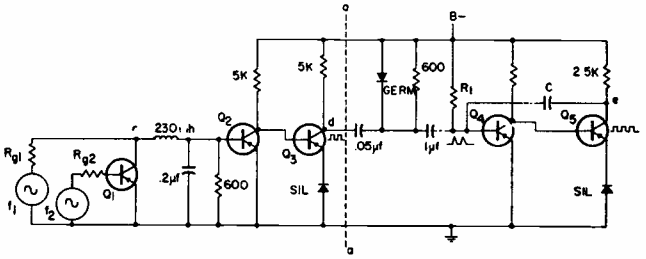


FIG. 2—Circuit to left of dashed line is used for method shown in Fig. 1A, complete circuit is needed for second method, in Fig. 1B. Collector resistor for Q_4 is 2.5K.

be held off; thus, point *d* is held at *B*—. During the negative half cycle of f_d, Q_2 will be held off and Q_3 will then saturate driving point *d* to ground. Therefore, a square wave of peak-peak voltage = *B*— is developed across point *d* to ground.

The developed square wave is then fed into the common input of the start and stop inputs of a counter having a Time Interval function. The Start Input can be set to trigger when point *d* goes to *B*—, and the Stop Input can be triggered at the same point of the cycle one period later.

To use the second method for measuring f_d, the circuitry to the right of dashed line *a.a* is also required. The object of the rest of this circuit is to provide square pulses of a frequency = f_d and of such a width as to be able to be properly integrated by a dc voltmeter. The width must be adjusted so that its time constant is somewhat larger than the voltmeter time constant.

To obtain the desired pulse, the square wave across point *d* is differentiated by the series *RC* network. The resulting spikes are rectified by the germanium diode, and the remaining positive spikes turn Q_4 off; Q_4 is a normally saturated transistor. When Q_4 is shut off, Q_5 will then saturate due to the change in the collector voltage of Q_4. Q_5 will remain on until Q_4 is turned back on, an event determined by the time required for *C* to discharge. *C* will discharge through *R* until the base of Q_4 goes slightly negative. As the base of Q_4 goes negative, Q_4 will again saturate and Q_5 will shut off. Thus a pulse of a height = *B*— and a width = R_1C is developed and can be used to deflect a dc voltmeter.

A supply of 20 volts, and five pnp switching transistors were used during the circuit test.

Phase-Sensitive Demodulator with Pulse Reference

PHASE-SENSITIVE demodulators are often very important in ac servos for stabilization, as they allow the use of dc phase-shift networks. This application is shown in the block diagram of Fig. 1. The ac from the preamplifier is applied to the phase-sensitive demodulator. The output is phase-shifted by the proper amount in a lead network, and then

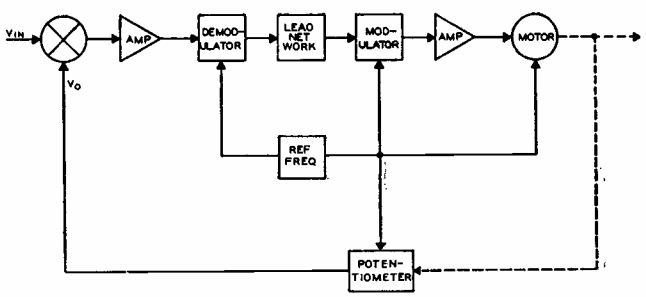


FIG. 1—Servo using demodulator and lead network stabilization.

modulated with the ac reference for application to an ac servo motor.

The demodulator described in this article uses a pulse reference, rather than a sine wave or square wave. The use of a pulse reference allows conduction only at the peaks of the carrier signal. The output is applied to a capacitor which holds its voltage in between pulses. This circuit has an inherently good discrimination against any quadrature component of the signal. The ripple voltage for a constant amplitude input is practically zero, while in conventional demodulators there is a ripple voltage under these conditions. It can be shown that the ripple amplitude for the pulsed demodulator with a sine wave input is $(2f_s/f_c)$ cos $\omega_s t$, while the ripple amplitude of a conventional demodulator with a shunt RC load is $(2f_s/f_c)$ cos $\omega_s t + (1/\pi f_c RC)$ sin $\omega_s t$. This second term could theoretically be reduced by making RC large, but in practice it is difficult to reduce.

The time constant of the pulsed demodulator is $1/(2f_c)$ since no output is obtained until the peak of the carrier is reached. However, the time constant of the conventional demodulator is essentially the same. A disadvantage of this circuit is that it has a high output impedance, and therefore must be fed into a circuit with a high input impedance, such as an emitter follower.

Figure 2 shows the pulse reference and demodulator circuit. A sinusoidal reference voltage of about 100 volts rms is applied at the 100K resistor. The two IR MZ 5.6 zener diodes give a square wave of 12 volts peak-to-peak. This is applied to a differentiating circuit, giving a pulse output as shown on the diagram. The time constant of this circuit is $0.0015 \times 10^4 = 15$ microseconds. For a 400-cps carrier, the period is 2500 microseconds, and therefore the differentiating circuit will produce a good pulse for this frequency and for frequencies as high as 6000 cps. An emitter follower is used to allow the differentiating circuit to feed into a high impedance.

A full-wave demodulator is used, and therefore it is necessary to have a pulse for each half-cycle of the carrier frequency. Thus, the output of the emitter followed is applied to a transformer giving a center-tapped high impedance output. This is applied to transistors which are negatively biased at the emitter so that only sharp positive pulses will appear at the output.

The collectors of these transistors are connected to transformers. The secondary of each transformer has a 1N91 diode across it to short out positive pulses that would normally appear there. A 1.2K resistor across the primary of each transformer reduces nonlinear loading effects due to the diode. The output of the transformer is applied through a large capacitor to the bases of the demodulator transistors to give a positive voltage during the time when there is no pulse. This assures that the transistors will not conduct during this time, and will only conduct when a pulse is applied.

The input signal is applied to a transformer with a center-tapped secondary. The center tap is grounded, and each end is connected to two transistors with collectors tied together for each pair. When a negative pulse is applied to the transistor base, the pair conduct whatever voltage is on the transformer at the time.

For the arrangement shown, the pulses are such that one pair of transistors conducts during the positive half cycle of the carrier, and the other pair conducts during the negative half cycle, sending current in the same direction into the 1-μf capacitor. Full-wave demodulation reduces the magnitude of high frequency in the output, and in addition, this high frequency is double the carrier frequency making the filtering problem much easier.

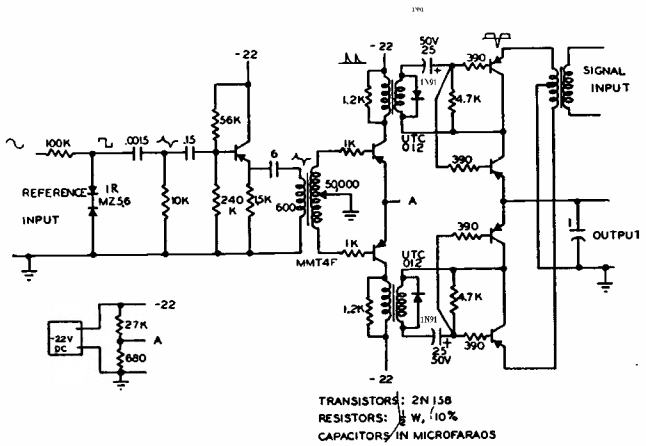


FIG 2—Circuit of pulse demodulator with pulse reference.

Comparator Uses Bilateral Transistor

ALTHOUGH bilateral transistors have been available for sometime, very little has appeared in the literature concerning unique uses for these devices.

A comparator circuit has been developed which depends upon bilateral transistor action as the basis of its operation. The circuit shown in Fig. 1 can be used as a voltage comparator by connecting one input to some reference level and allowing the second input to vary. Assume that input B is referenced to —5 volts. Its emitter to base junction is, therefore, back biased. However, diode D_2 will conduct causing base current to flow in Q_1, holding Q_2 on. Since Q_1 is bilateral, a similar condition prevails if the inputs are reversed. When the voltage levels at inputs A and B become equal (—5 volts), there is no base current flowing in Q_1. This causes Q_2 to cut off and the output rises to $+V_{CC}$.

The circuit is also capable of functioning as a digital comparator. In a digital computer, it is frequently necessary to ascertain when two numbers become equal. The circuit is capable of comparing the two numbers in the following manner: it gives a pulse output when there is a difference between the two numbers and a dc level ($+V_{CC}$) when and only when the two numbers become equal. Figure 2 shows a typical system application and the output waveforms for the conditions when the two numbers are equal and unequal.

Other possible uses for bilateral transistors include multiplexing, intercom and two-way telephone communication systems.

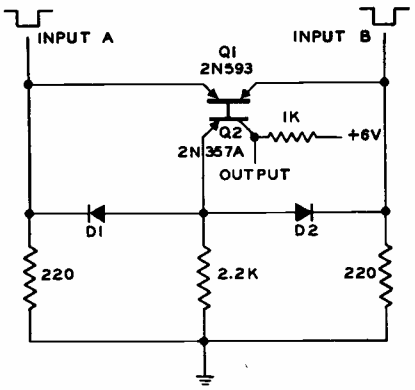


FIG. 1 — For computer use, digital comparator circuit gives pulse output when there is a difference between two numbers.

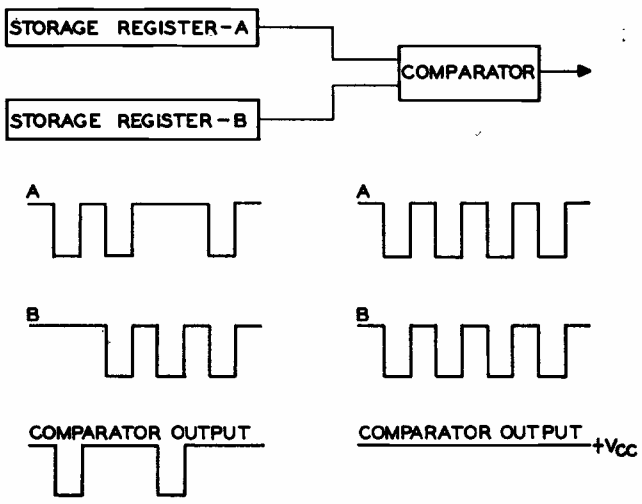


FIG. 2—Output waveforms when two numbers are equal or unequal.

Differential Voltage Comparator

THIS DIFFERENTIAL voltage comparator was developed to provide a "go-no-go" indication when two input signals are compared. If the two signals are within a preset differential voltage, the relay is not actuated and a "go" indication is provided. When the two signals differ by more than a preset differential voltage, the relay is actuated and a "no-go" indication is provided. The circuit operates if the signal on terminal 1 is either positive or negative with respect to terminal 2. A balance control is provided to adjust the circuit balance through a relay actuated with an equal positive and negative differential voltage. The sensitivity control

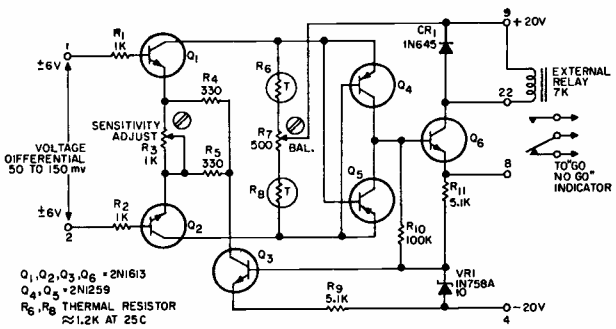


Fig. 1 Voltage comparator.

adjusts the differential voltage over a range of 50 to 150 mv. The input voltage to terminals 1 and 2 may vary over a range of —6 to 6 v. Transistor Q_3 serves as a constant current source for transistors Q_1 and Q_2 and simultaneously provides a high impedance between their common emitters and the power supply. In this manner a high common mode rejuection is provided which keeps the differential voltage sensitivity from varying more than 1 per cent over an input signal range of —6 to + 6 v. The thermal resistors consist of a thermistor in parallel with a fixed 1.5 K resistor and provides temperature compensation for the variation in the base-to-emitter voltage of Q_4 and Q_5. The circuit exhibits a hysteresis of not more than one to two per cent.

To explain the operation of the circuit, assume terminal 2 is at zero volts. If terminal 1 is also at zero volts, the current will be the same in Q_1 and Q_2, therefore, the voltage at the bases and emitters of Q_4 and Q_5 will be the same an dthey will be cut off. Consequently, Q_2 will also be cut off and the relay will not be actuated.

If the voltage on terminal 1 is now made more positive by 100mv, Q_1 will draw more current than Q_2 thus the emitter of Q_5 will be positive with respect to its base and will conduct. The collector current of Q_5 causes Q_6 to conduct and actuates the relay. The conduction point of Q_5 is critical when the base-to-emitter voltage is about 0.7 v. The operation is similar if terminal 1 is made negative. Under this condition Q_4 conducts instead of Q_5.

Sensitivity is quite independent of power supply votages and will work from 20 to 24 v without readjustment. The circuit was designed to operate over a temperature range of 0 to 50 C.

This circuit was developed for and used in a test console for comparing telemetered data received from a MIDAS satellite vehicle. When the received data was not within 100 mv of the data transmitted, a "no-go" indicator would be actuated.

Variable Schmitt, Amplitude Comparator

THE CIRCUIT SHOWN can be used either as a Schmitt trigger with a variable trigger voltage (where V_B determines the trigger voltage), or as an amplitude comparator (where the amplitude of V_A is compared with the amplitude of V_B). These functions are obtained by using a minimum-hysteresis Schmitt trigger[1] and applying the voltage V_B to the base of Q_2 through R_B.

Features of the circuit are:

☐ A variable trigger voltage is readily obtained without changing the load on the input signal.

☐ A regenerative comparator is obtained having negligible hysteresis.

☐ The circuit is simple and inexpensive, and its operation is readily predictable.

☐ The circuit readily provides high speed operation.

Formulas for the resistor values can be found in the reference. The parameters used were:

$V_T = 7.0$ V, $V_c = 7.0$ V, $V_{s1} = 24$ V. $V_{s2} = 0$ V, $R_E = 1$ K and $R_B = 6$ K.

The resistor values shown are within 2 percent of the calculated values; 1-percent resistor tolerance was used throughout.

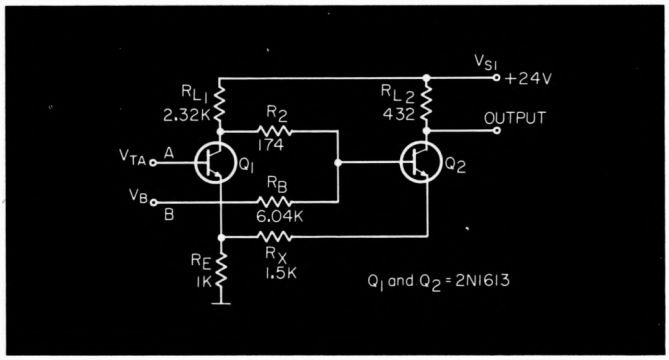
The voltage comparator formula giving the trigger voltage at point A (V_{TA}) as a function *of* V_B is linear:

$$V_{TA} = V_T + \frac{R_E}{R_E + R_X} \cdot \frac{R_T}{R_T + R_B} V_B$$

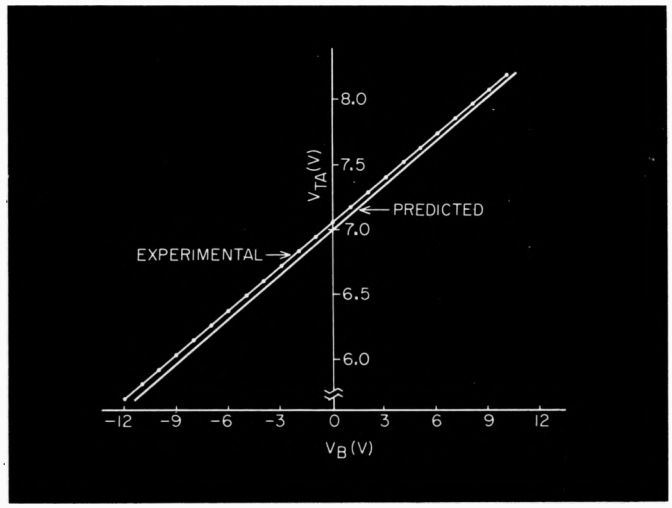
where V_T is the trigger voltage with $V_B = 0$ and R_T is the parallel combination of $(R_L + R_2)$ and $[(\beta_2 + 1)(R_E + R_X)]$. This reduces to:

$V_{TA} = 7.000 + 0.116\ V_B$

for the values shown. The curve shows the experimental plot of V_{TA} vs. V_B to be in excellent agreement with that predicted by the formula. The hysteresis for the circuit shown was 30 mV.



Variable Schmitt trigger, amplitude comparator in which V_B controls trigger level or is compared with V_{TA}. Comparison of calculated and experimental triggering points (below).



Reference:

1. William E. Zrubek, "Minimum-Predictable-Hysteresis Schmitt Trigger," EEE, Dec. 1963, pp. 40-43.

Frequency Comparator Uses ICs

THE CIRCUIT shown in in Fig. 1 can be used as a control circuit for VCOs, as a go-no-go frequency comparator, or as a frequency discriminator. There are two inputs to the circuit, a standard frequency and an unknown frequency (labeled *TACH* in the diagram). If the unknown frequency is less than the standard, then the output dc level is low. If the unknown frequency is higher than the reference frequency, then the output dc level is high.

When the two input fre-

quencies are identical, the circuit behaves as a linear phase discriminator. Unlike frequency discriminators that use tuned circuits, this digital discriminator has no humps in its characteristic curve.

The circuit shown in Fig. 1 was originally part of a larger circuit which included oscillators and VCOs. The dual NOR gate IC_6 is not really a part of the frequency comparator circuit, so for the purpose of this analysis it can be ignored. In the original application, IC_6 gave the correct levels, rise time and fanout for driving the comparator circuit.

Assume that the inputs are at points S and T in the diagram. Assume also that the first incoming pulse is on the S line. Then, this pulse sets the A output of IC_2 to "low" and simultaneously sets the B output to "high." (Note that the gates of IC_2 and IC_3 are cross-coupled to form flip-flops.)

The next S pulse propagates through gate B of IC_4 to set the B output of IC_5 to "low," with the A output "high." These outputs are connected to Q_1 and Q_2. Therefore Q_1 collector goes "low" and Q_2 goes "high."

Because Q_2 collector is "high" it disables the B gates of IC_1 and IC_3, allowing no change for further incoming S pulses.

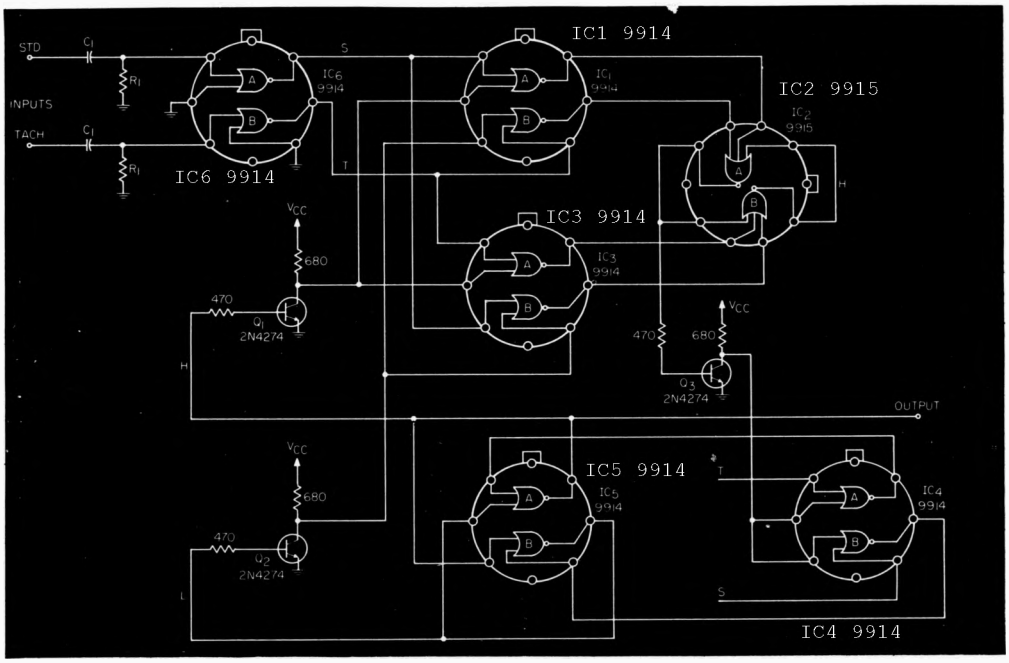


Fig. 1. Digital frequency comparator uses no tuned circuits.

Now, when the first T pulse arrives after a series of S pulses, it propagates through gate A of IC_3 to set gates B and A of IC_2, "low" and "high" respectively. This drives the collector of Q_3 "low," thus enabling gates A and B of IC_4. After this occurs, the next T pulse will then propagate through gate A of IC_4 to set gate A of IC_5 "high." As the circuit condition has not been reversed, any number of T pulses in a row, without an additional S pulse, will cause no further changes in output level. This will be seen more clearly, if the reader compares Fig. 2 with the above description.

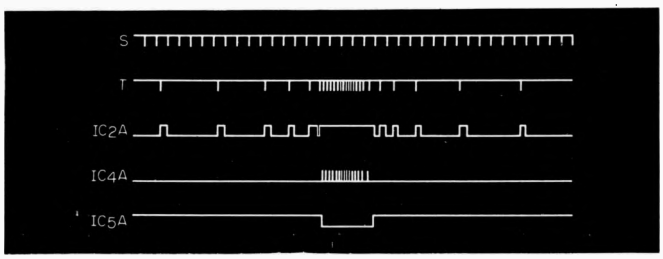


Fig. 2. Timing diagram shows the effects of T frequencies higher and lower than the S frequency.

The output can be selected to be of either polarity, for a given frequency relationship, by selecting the appropriate output of IC_5.

IC voltage comparator with adjustable threshold and hysteresis

THE CIRCUIT SHOWN in Fig. 1 has many of the properties of a conventional Schmitt trigger. But the improved circuit offers greater flexibility. Threshold and hysteresis are both adjustable. Two potentiometers determine the upper and lower trigger levels. These preset reference voltages are switched in or out of the circuit, depending upon the input signal level.

In Fig. 1, differential amplifier A_1 is biased by zener diodes CR_1 and CR_2. Buffer amplifier Q_1 couples the output signal from A_1 to gate G_1 of the triple-gate driver A_2. The remaining two gates, G_2 and G_3, alternately switch pots R_5 and R_1 into the reference node formed at pin 7 of A_1. Gate G_1 produces an IC-compatible output with suitable fan-out.

Initially, input voltage V_{in} is at zero. The pin-7 input to A_1 is then more positive than pin 1; thus Q_1 is held off because its base is at V_{cc}. Gates G_1 and G_2 are connected to the collector of Q_1, so these are also held off. But gate G_3 conducts, holding one end of R_7 at ground potential. Because the gates of SUHL driver A_2 have no pull-up resistors, R_6 is effectively out of the circuit. Thus the ratio of R_3 and R_7 alone determines the reference voltage at pin 7 of A_1.

As V_{in} increases, it eventually exceeds the preset reference voltage at pin 7. When the input voltage exceeds this "upper trip level" by about 25 mV, Q_1 conducts and turns on gates G_1 and G_2. Output voltage V_{out} then drops to the low state and gate G_3 turns off This disconnects R_7 from the circuit and introduces R_6. Provided R_6 has been previously set correctly, the reference level now abruptly drops to a lower voltage. This new voltage, set by the ratio of R_3 and R_6, is the "lower trip level."

If V_{in} decreases and falls below the lower trip level by

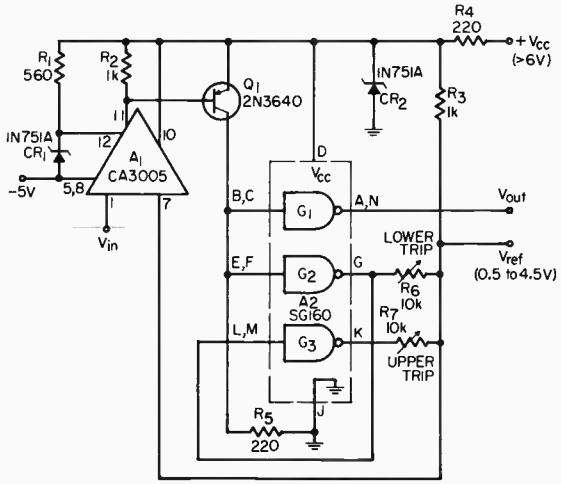


Fig. 1. This circuit can replace the simple Schmitt trigger in applications where both trigger levels must be adjustable. R_6 sets the lower trip point and R_7 sets the upper trip point.

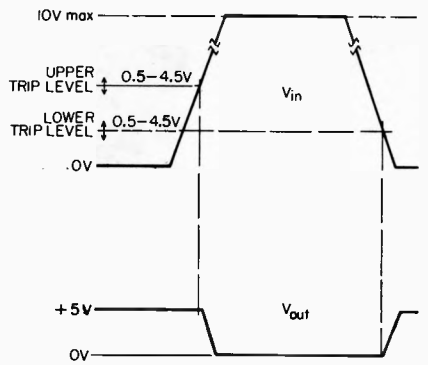


Fig. 2. When the input voltage exceeds the upper trip level, the output voltage drops to its low state. Later, when the input voltage falls below the lower trip point, the output voltage is restored to its high state.

at least 25 mV, Q_1 will turn off, again turning off gates G_1 and G_2. This restores V_{out} to a high level and places R_7 back in the circuit to reset the upper trip level for the next cycle, as shown in Fig. 2.

Because of the good temperature stability of the CA3005, threshold voltage of this circuit varies very little with temperature. Only small currents are needed to hold R_6 and R_7 at ground, so variations in gate-saturation drops can be neglected. Stability primarily depends on the stability of the reference voltages. If necessary, CR_2 can be replaced by a temperature-compensated zener.

Voltage comparator with visual readout

THE CIRCUIT shown in Fig. 1 provides visual indication of circuit continuities. It does this by comparing system voltages with a reference voltage.

With no voltage applied to the switch, V_{in} is zero. An external 28-volt reference voltage applied to D_3 causes it to conduct. And with lamps DS_1 and DS_2 off, the base of Q_1 is at ground potential. The transistor becomes forward-biased, shunting R_2 so that no current flows through the resistor. Current then flows from the 28-volt supply through lamps DS_3 and DS_4 turning them on.

If a voltage V_2 (28 V for the circuit shown) is applied through the switch, D_1 conducts, lighting DS_1 and DS_2, and extinguishing DS_3 and DS_4. This is because the Q_1 is cut off by the input voltage, thus causing D_2 to conduct, and D_3 to be turned off.

Input resistor R_1 limits the starting current to the lamps to increase their life. If more accurate comparison is needed, R_1 could be eliminated.

The circuit acts as a go-no-go indicator. The lamps DS_1 and DS_2 give a circuit continuity indication while DS_3 and DS_4 give an open circuit indication. Note that the lamps are paired, with one redundant lamp in each pair. Thus if a lamp fails, the circuit will still give an unambiguous indication.

In the original application for this circuit, the system voltage was 28 Vdc. The circuit can easily be modified for other supply voltages.

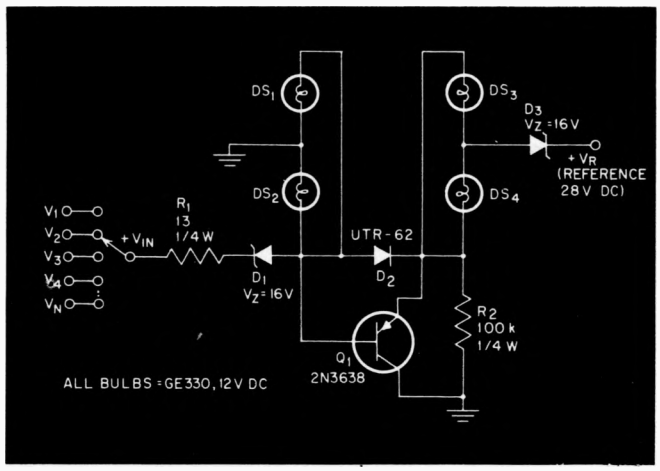


Fig. 1. Simple go-no-go indicator monitors circuit continuity of electronic systems.

Op-amp comparator with latching function

BY ADDING just a few components to an operational amplifier comparator, one can obtain a latching function. The circuit compares an input signal against a reference voltage, and when the reference voltage is exceeded the output switches and the comparator latches up. This circuit is the electronic equivalent of a latching relay. Resetting is accomplished manually or electronically. Input impedance and trip point are independent of the input level E_1.

In the figure, the input signal and reference level are summed together through R_1 and R_2. If E_o is positive, then Q_1 will be saturated and D_5 will block the 60 mV of Q_1 saturation voltage from the summing junction of the operational amplifier. When the input level goes more positive than $-E_R$, the output of the op amp will swing negative to about -1.6V and Q_1 will switch off. With Q_1 off, approximately $+2.5$ mA will flow into the summing junction through R_3 and R_4.

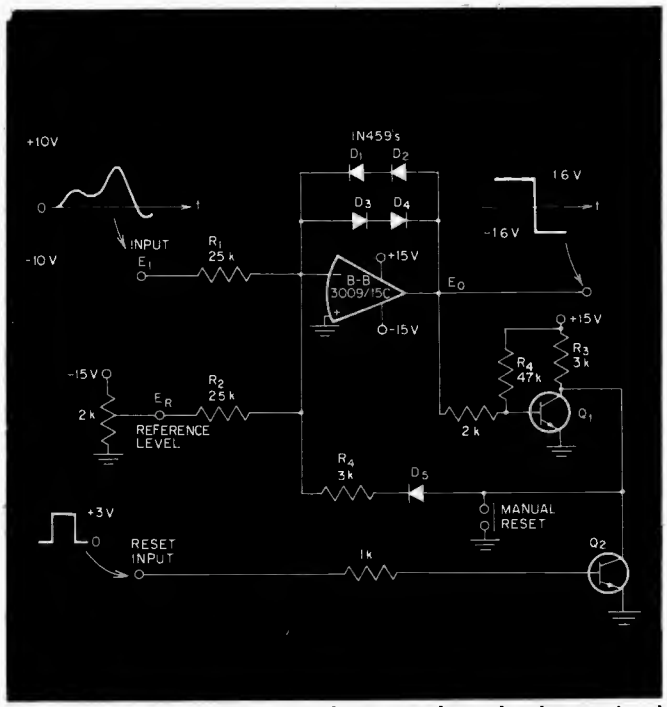
The latching operation is regenerative and analogous to the operation of a flip-flop. The amplifier will remain latched up with its output negative because

$$\frac{+15V}{R_3 + R_4} > \left| \frac{E_1}{R_1} + \frac{E_2}{R_2} \right|$$

with any combination of input voltages.

Resetting may be accomplished by several means, one of which is to short the collector of Q_1 to the common. A manual pushbutton can do the job, or an extra transistor Q_2 can be used if a logic signal is available.

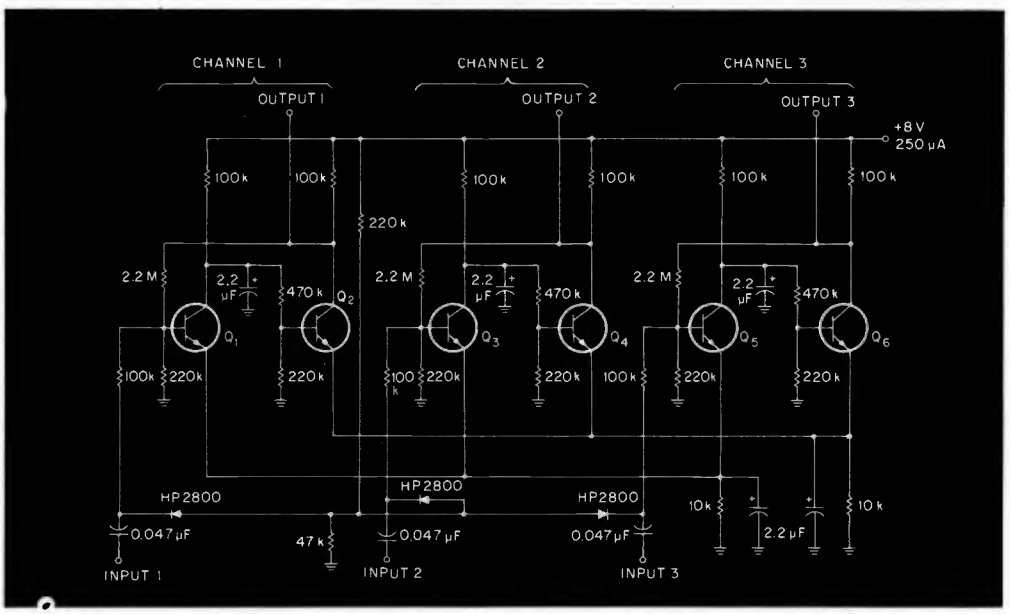
Accuracy of the circuit depends almost entirely on the match between R_1 and R_2. The latching-circuit sensitivity can be varied somewhat by varying the bias on Q_1 through the resistor R_4. The choice of op amp is not critical and most IC or inexpensive discrete units will perform well. ■



This op-amp comparator latches up when the input signal exceeds the reference.

Low-power, multiple-input comparator for ac/dc inputs

THREE or more ac or dc inputs can be compared directly with the comparator shown in the figure. The input with the largest amplitude yields a positive output state. The circuit consumes very little power — only 2 mW for the 3-input example shown, an audio-frequency voltage comparator. Each input is rectified and applied to the base of a transistor which forms one side of a Schmitt trigger. Both sides of each section are coupled to the emitters of the corresponding transistors in the other sections. Bias voltages are chosen so that only one input



This 3-input amplitude comparator is based on repetitive 2-transistor sections that lend themselves to construction of an n-input comparator. The transistors are 2N4286.

transistor can be on, and two output transistors must be on. Thus, one output transistor must be off, providing one high output at +7 V. This high output will always be from the section having the highest input amplitude.

Circuit operation is very similar to that of a two-transistor Schmitt trigger. Suppose that *Input 1* has the largest amplitude. Q_1 will be held on by the input signal, and Q_2 will be off. Because of the Q_1 emitter current in the 10-kΩ emitter resistor, Q_3 and Q_5 are biased off, holding Q_4 and Q_6 on. Now, suppose that the *Input 2* amplitude increases. As Q_3 begins to turn on, Q_4 is biased off by the coupling from the Q_2 collector. Q_1 must turn off because of the increased emitter voltage as Q_3 turns on, and Q_2 must turn on because of coupling from the Q_1 collector ■

Low-component-count digital comparators

THE MOST STRAIGHTFORWARD method of comparing the state of a counter with a number selected by thumbwheel switches is to compare the outputs of counter flip-flops and digital switches with an Exclusive-OR, as in Fig. 1. This approach is adequate if the number of switches is small. But as the quantity goes up, the logic becomes more complex since each switch requires a comparator.

A simpler solution is to add diodes to the thumbwheel switches to form an AND gate and drive this configuration with the flip-flops of the counter (Fig. 2). The output will be high (+5 V) only when the counter matches the setting of the switch (count 8 in the example). As long as there is a mismatch, at least one diode will provide a path to ground, keeping the output low.

While there is a mismatch, the output (*A* in Fig. 2) will be about ±1 V. That's the low output of the IC, typically 0.4 V, plus the forward drop of the diode. This exceeds the highest "0" that most ICs will tolerate (+0.8 V typ).

To avoid erroneous circuit operation, one should place a voltage comparator in the line and use a reference of 2 to 3 Vdc. The comparator output will then be high only when the output is at +5 V.

If many decade switches are used, each decade is driven by the corresponding counter decade and the commons tied together to form one output. ■

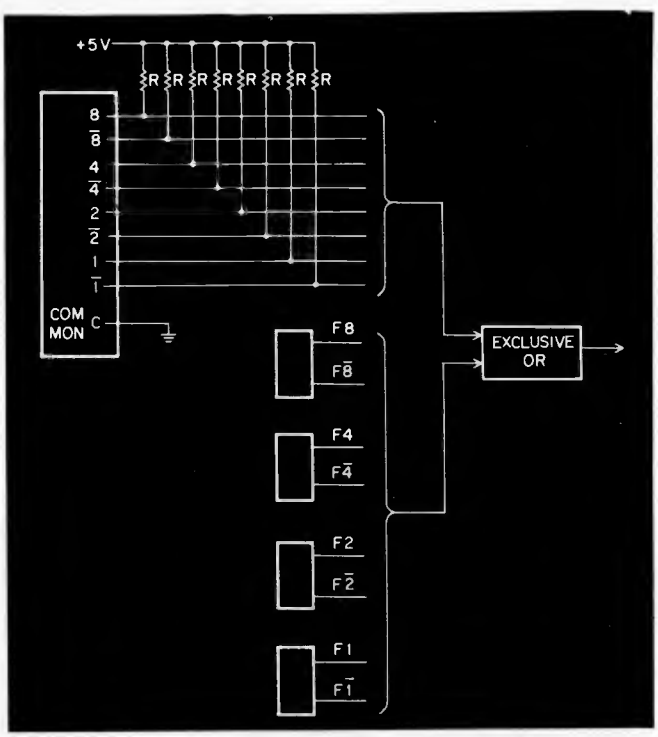


Fig. 1. The Exclusive-OR approach is the most direct one for comparing the output of a digital switch with that of counter flip-flops. But when several switches are used, each requires a comparator.

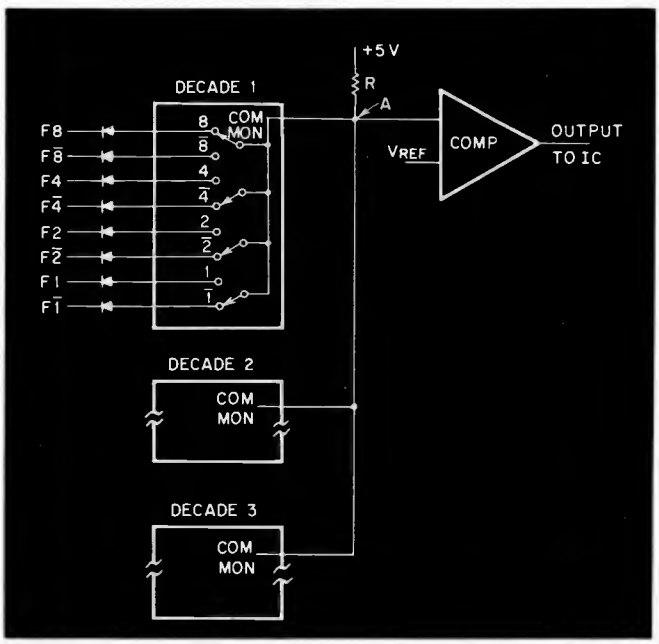


Fig. 2. In this approach, AND-gate diodes, driven by counter flip-flops, perform the comparisons

Section 7
AMPLIFIER CIRCUITS

"Power-Less" Pulse Amplifier

IT IS POSSIBLE to construct pulse amplifiers which draw very little quiescent current. Indeed, if the duty cycle is relatively low, the operating current differs very little from its quiescent value.

By merely alternating pnp and npn common emitter stages, and by returning the base resistor of each stage to its emitter, all stages are cut off (See Fig. 1).

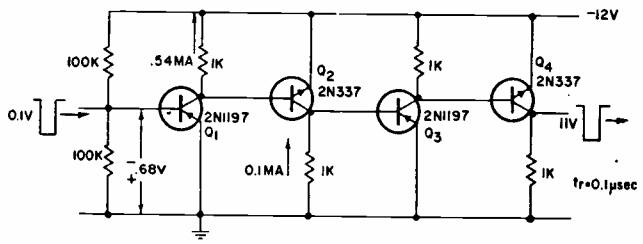


FIG. 1—Direct coupling and use of complementary transistors produces pulse amplifier chary of quiescent current.

It is interesting to observe that all stages are directly coupled, obviating the need for interstage capacitors. In addition, input and output stages are essentially at ground potential. Since the input pulse amplitude of 0.1 volt was below that necessary to overcome the input contact potential of the first transistor stage, it was necessary to cause Q_1 to conduct slightly. However, the total current was still only 0.7 ma.

By choosing the proper pnp-npn combination of common emitter and common base configurations and by selecting the appropriate supply voltage polarity, one can obtain any input and output pulse polarity while still maintaining all the desirable features already stated.

Hybrid Tube–Transistor Amplifier

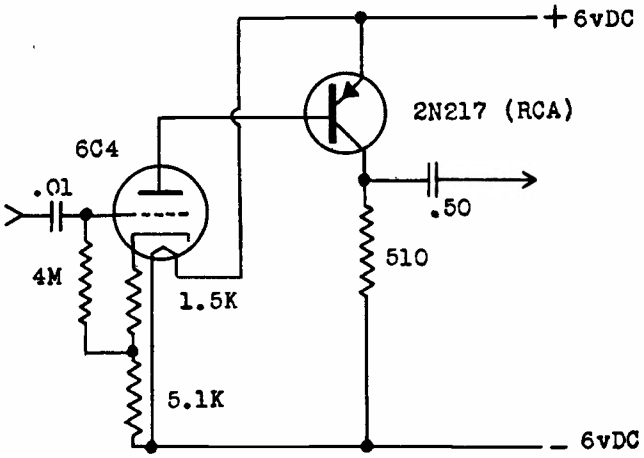
HIGH INPUT IMPEDANCE into a transistor amplifier was obtained by using the circuit shown in the diagram. A device was desired to take the output of a photomultiplier tube and convert it to a low impedance and at the same time it was desirable to have some voltage gain. It was also desirable to operate the circuit from the same 6v dc supply that was used on the remainder on the amplifier.

The circuit illustrated is a combination of vacuum tube and transistor circuitry. The vacuum tube portion of the circuit is basically a cathode-follower connected triode, to provide the desired high input impedance. The coupling to the transistor, however, does not come from the cathode as it normally would. The base of the transistor is connected directly to the plate of the tube, thus making the base current the same as the plate current; also, any variations in the plate current appear as changes in the base current of the transistor.

The transistor portion for the circuit consists of a pnp large signal audio transistor connected in common emitter configuration. No dc bias feedback was used on the model built, however, by adding a resistor from emitter to base and another from collector to base, the temperature stability will be greatly increased with a sacrifice of gain.

The voltage gain of the circuit is about three times, without dc feedback; a gain of about one or slightly higher is possible with dc feedback. The maximum voltage out is about 1v rms; this can be increased by increasing the supply voltage. The gain of the circuit does not vary greatly with changes in the supply voltage, (heater excepted). When the

supply voltage was changed from 6v dc to 12v dc the gain of the overall circuit changed only 10 per cent. The power requirements of the circuit are



Hybrid circuit provides high input impedance, low output impedance with voltage gain.

small, the total current, not including the heater, is only about 5 ma. The output impedance is low and can be connected to a long cable for remote indication purposes.

Driver Amplifier for 3½ and 6-Watt Servo Motors

A DETAILED CIRCUIT is presented in Fig. 1 for a high-performance servo-motor-driver amplifier. The characteristics of the amplifier are as follows: gain 30 db, ± 0.5 db variation including all temperature, all beta, and all component tolerance changes; input impedance 400 K ohms; output impedance 400 ohms.

To achieve such desirable characteristics, three important features are incorporated in the design.

A ± 25 volt well-regulated supply is used. Thus, stabilization of the operating points of the input stage is easily achieved, while maintaining an adequate output-voltage swing under adverse temperature and component tolerance conditions.

An npn-pnp feedback-amplifier pair is used in the input stage. This configuration has a voltage gain which can be reliably stabilized against beta variations, while providing a high input impedance. Close control of the stage gain is important, since overall feedback is used over two transformer stages.

An output transformer is used to couple the output transistors to the servo motor. The reason for using an output transformer instead of directly driving 28-volt servo motors is two fold: By proper design an optimum match can be made, resulting in the use of the smallest possible transistors in the

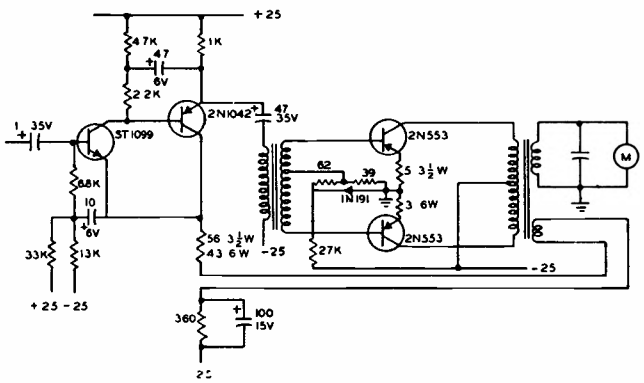


FIG. 1—Motor driver amplifier circuit was developed for the Radan-500 system.

output stage. A negative feedback winding is easily obtained and is used to provide tight feedback from both halves of the output stage. Such a feedback winding will reduce cross-over transients and increase the input impedance of the amplifier.

The interstage transformer is ac coupled, since any dc biasing current would necessite a large iron core if a high primary inductance is desired. Its turns ratio is 1:1 overall.

The output transformer has a turns ratio of 1:3.34 overall primary to 115-volt secondary. The feedback winding has 2.5 per cent of the secondary turns.

The development work was done while the author was Group Leader, Circuit Design, Radar Dept., General Precision Laboratory.

Hybrid Amplifier

HERE is an amplifier that makes use of the advantages of tubes and transistors in a manner that lowers cost and saves power.

It is simpler and less expensive to design an amplifier with an input impedance of one or two hundred thousand ohms or higher using a vacuum tube than with a transistor, and it is not as temperature sensitive as a transistor. On the other hand, to design an output stage with an output impedance less than about 100 ohms requires a vacuum tube cathode follower with a g_m of approximately 10,000 micromhos, and such a tube usually draws fairly large heater and plate currents. A transistor connected grounded collector can give an output impedance well under 100 ohms with less power consumption and circuit complexity without difficult temperature stability problems.

The amplifier schematic in Fig. 1 embodies the principles mentioned. The overall voltage gain is approximately 95 with a frequency response that is ±0.5 db from 1 kc to over 50 kc. The total harmonic distortion is 0.5 percent or less at an output

of 8.5 volts peak-to-peak across a 500-ohm load. The output impedance of the amplifier is less than 75 ohms. The total B drain is only 15 ma.

In Fig. 2a is a block diagram showing each stage function as far as the signal is concerned. The first and second stages are the two halves of a 12AT7 connected in cascade. The output stage is a 2N1123 (stud-mounted equivalent of 2N597) connected in the emitter follower configuration.

The output impedance of an emitter follower is approximately $Z_o = Z_s/\beta$ where Z_s is the source impedance seen by the base. For the 2N1123 and

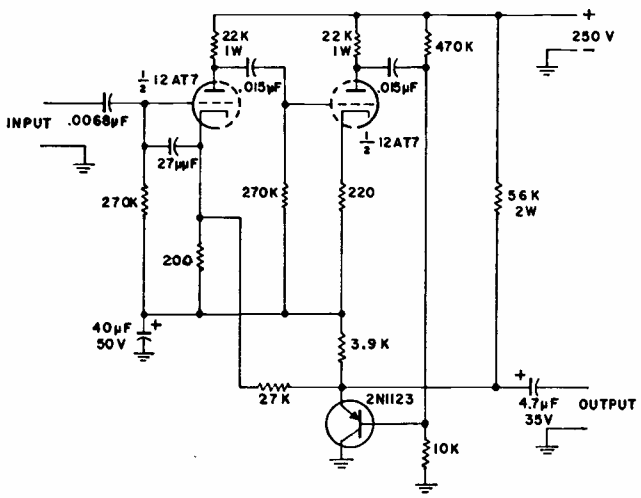


FIG. 1—Hybrid amplifier has gain of 95 from 1 kc to 50 kc.

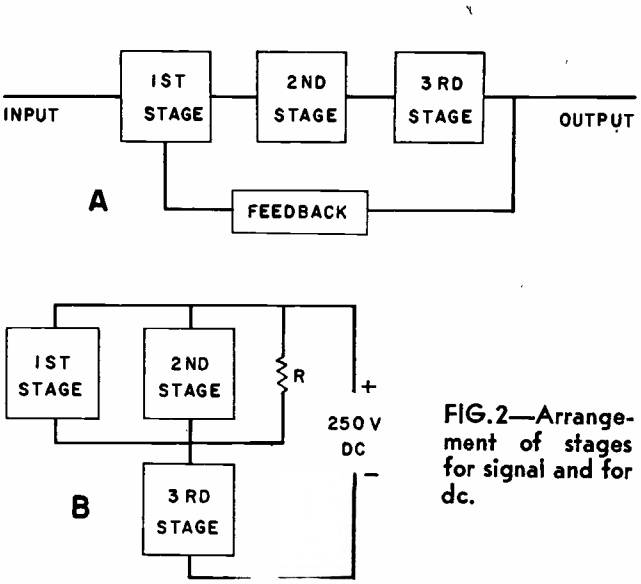


FIG. 2—Arrangement of stages for signal and for dc.

$Z_o = 75$, $Z_s = 4{,}500$ ohms. This means that the parallel impedance of the two base resistors, the preceding plate load resistor, and the preceding plate resistance should not be more than 4,500 ohms.

The gain obtained from this stage for a given tube will be limited by the maximum plate load resistor consistent with a value of 4,500 ohms for Z_s. It remains for the first stage to provide the rest of the gain needed to obtain the overall amplification required. The maximum gain that can be obtained in this stage is limited by the fact that if the plate load resistor is made too large the shunt capacitance will cause a loss of gain at the higher frequencies.

To obtain the required low harmonic distortion and also stabilize gain with changes in tubes, etc., inverse feedback was required. Lowest distortion and a saving in parts was obtained by overall voltage feedback around the three stages as well as individual stage feedback on the 12AT7 tube.

Figure 2b is a block diagram showing the amplifier configuration from the d-c standpoint. In this application the desired transistor emitter current was not a great deal larger than the combined plate currents of the two halves of the 12AT7. A supply of 250 volts (and 6.3 v, ac) was available. It appeared convenient to put the transistor in series with the two paralleled halves of the 12AT7. In this way the only wasted power was in a resistor (R in Fig. 2b) shunting the lower current device, the 12AT7. Despite the series-parallel connection, an open in either triode or the transistor will not cause damage to the other two, nor will a short circuit in any of these three elements cause damage to the other two.

Referring to Fig. 1, the cathode bias resistors for both triodes are unbypassed, constituting single stage feedback around each triode. For the first stage $Z_L = 22$K ohms and the gain is 40 without feedback. For the second stage, Z_L equals the parallel combination of 22K, 10K, 470K, and the input impedance of the 2N1123. This impedance is given approximately by β times the amplifier load impedance and is 27K ohms. This gives 18 for the second stage gain.

The feedback factors, β', for these two stages are 0.01 and 0.04, giving stage gains of 28 and 11 respectively. The 27K-ohm resistor from the emitter of the 2N1123 to the cathode of the first stage forms an inverse feedback path around all three stages. Without this feedback, the voltage gain of the complete amplifier is approximately 270. The feedback factor equals 0.014 giving a closed-loop voltage gain of 95. The use of inverse feedback in this manner also lowers the output impedance of the amplifier below the value of 75 ohms calculated for the 2N1123 alone.

Using the same tube and transistor a frequency response up to at least 100 kc and greater gain or a lower output impedance can be obtained. An amplifier with an output impedance of 15 ohms with the same output voltage across a load of 120 ohms has been built using the same circuit.

Constant Output AC Amplifier

THE CIRCUIT presented will maintain a nearly constant (±5 percent) ac output for a 10:1 change in input. This phenomenon is achieved by using the variable gain characteristic of a tetrode transistor in conjunction with dc feedback which is proportional to the ac output.

The gain of a tetrode may be varied by either of two methods. One method uses a reverse bias between one of the bases and the emitter while the other base is forward biased. The second method uses a transverse bias between the two bases. Of the two methods of gain contol, the second method was selected because it has less effect upon the common emitter input impedance of the tetrode.

The basic relationship between common base gain and common emitter gain is given by

$$H_{FE}=H_{FB}/1-H_{FB} \qquad (1)$$

when H_{FB} in the common base dc gain and H_{FE} is the common emitter dc gain. As a result of this relationship, a small change in H_{FB} will result in a relatively large change in H_{FE}. It follows from this that the ac configuration should be common emitter to take advantage of the maximum gain change and the dc configuration should be common base to keep the variation in dc operating point (quiescent current level) as small as possible. These two factors are incorporated in the basic circuit of Fig. 1.

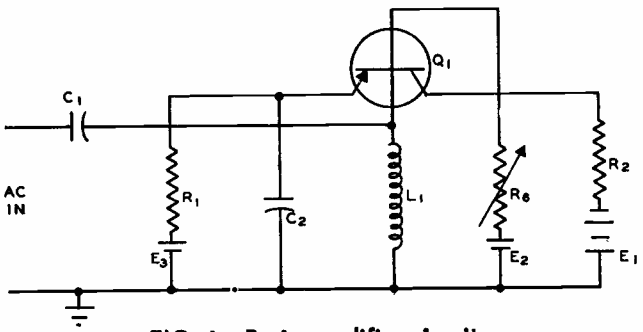


FIG. 1—Basic amplifier circuit.

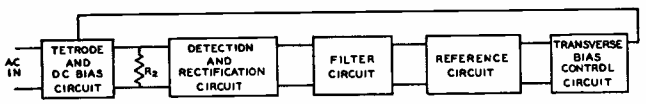


FIG. 2—Stages of practical circuit.

In the basic circuit, E_3 and R_1, in conjunction with the relatively low dc resistance of L_1, form a dc common base circuit. The combination of L_1 and C_2 results in an ac common emitter circuit which is the desired result. This combination resulted in a change in H_{FE} (ac common emitter current gain) of 15:1, while H_{FB} (dc common base current gain) changed only 25 percent (4:3).

If variable resistor R_6 in series with E_2 in Fig. 1 were replaced by a transistor, we now have a means of controlling the gain of the tetrode transistor by a small dc signal. For the complete circuit, it is only necessary to rectify a sample of the ac output, compare it to a reference, and then apply the error signal to the transistor which controls the transverse bias of the tetrode. The system is shown in the block diagram of Fig. 2.

The final complete circuit is shown in Fig. 3. In this circuit C_3, T_2, D_1, D_2, R_3, and Q_2 comprise the rectification and detection portion of the circuit. C_3 is a dc blocking capacitor. T_2 permits full wave rectification and acts as a high impedance paralleling the ac load. D_1 and D_2 are for full wave rectification. Q_2 amplifies the rectified signal and R_3 causes Q_2 to have a high input impedance. The combination of transformer and two diodes may be replaced by a bridge rectifier in most applications.

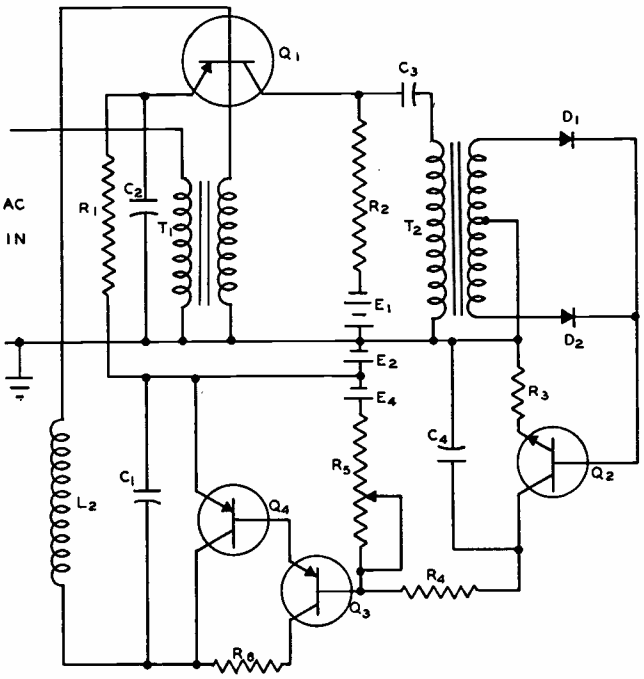


FIG. 3—Complete circuit contains amplifier for the difference signal.

Capacitor C_4 and resistor R_4 form a filtering circuit for the output of Q_2. R_4 also acts as a further current limiting resistor for Q_2 (along with R_3).

The combination of E_4 and R_5 determines the reference level for the output. Since I_{C2} (Q_2 collector current) is proportional to the ac output, when $[I_{C2} + I_{CBO3}\ (Q_3)] \times R_5 > E_4$, Q_3 will be turned on. If less than E_4, Q_3 will be reverse biased. The reference level for control is therefore determined by E_4, R_5 and I_{CBO3}.

Transistors Q_3 and Q_4 are a two-stage amplifier for the difference signal between the ac output and the reference. The output of these two transistors is the transverse bias of tetrode Q_1. In the circuit, R_6 is a current limiting resistor for Q_3. Inductor L_2 and C_5 insure that the transverse bias control (Q_3 and Q_4) is isolated from the ac signal being

applied to base 2 of the tetrode transistor Q_1.

The circuit of Fig. 3 was assembled with materials readily available in the lab, and therefore the transformers and chokes are not optimum. The circuit will operate satisfactorily as shown. The 3N45 tetrode transistors were used at a level far below their power capabilities because a particular application was in mind during the design of the circuit.

The circuit may be made more versatile by using another stage of controlled gain amplification in series with the stage shown. Both stages could be controlled by one feedback circuit if care is taken to split the output of Q_4 between the two stages being controlled. Closer control may be obtained if there is further amplification between the controlled tetrode and the output or if another stage is added in the control circuit.

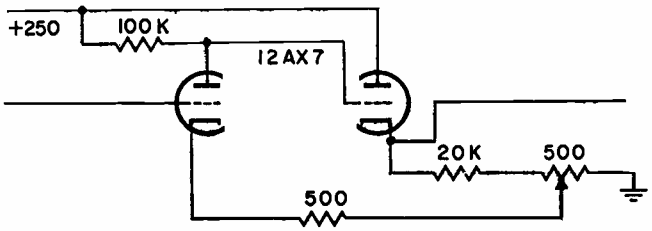
Since the circuit uses dc as a feedback control, the number of stages of amplification between the controlled tetrode and the output is entirely up to the designer. There is no phase shift problem in the feedback control. The control should also have very little dependence upon the frequency of operation within practical limits. Another advantage is that the control system will not increase distortion of the ac signal but rather will tend to decrease the distortion (a normal phenomenon of transverse biased tetrodes).

Additional Gain Circuit

IN THE CIRCUIT shown in Fig. 1 the system is a simple amplifier with cathode follower loading and output when the potentiometer arm is set at ground level. As the arm is raised above ground the gain of the amplifier can be raised to any desired value, 10 thousand being used in one case without reaching the maximum. This is a positive feedback circuit similar to the Q multiplier. It is a particularly convenient and stable way to trade bandwidth for gain, for with the potentiometer arm at ground the additional gain circuit effectively isn't there. With the pot arm raised so as to square the or ginal gain (effectively two stages in cascade) the phase shift of the single stage will have been multiplied by two, as it would by two stages in cascade. Thus, although the amplifier being loaded only by a cathode follower will perform better than two stages in cascade, the output impedance is low, and the second stage is very simple.

However, the virtue of this circuit is that the gain can be set at whatever level is desired and if less than the square of the original gain is desired, the phase shift added is proportionately small. If only a little more gain is needed, very little extra phase shift is added to the output of the circuit.

The circuit as shown will reach infinite gain when the feedback signal is sufficient to replace the input, or when the resistance below the pot arm is equal to the total cathode resistance divided by the



Additional gain circuit is similar to Q multiplier.

original gain of the amplifier. In this case the amplifier's gain would be about 50, so that for high gain the pot arm would be raised to nearly 400 ohms.

One of the drawbacks of this circuit is Miller effect. For high gain the amplifier should be a pentode to reduce C_{gp}. However, C_{gk} is also multiplied by the additional gain so that for a high-impedance input this might limit performance. However, when used only for limited additional gain, the added Miller effect is usually negligible. Note that if a pentode amplifier is used it will be capable of giving high gain simply because it is cathode follower loaded, permitting doubling of the plate load resistor, or if the same load resistor is used, additional bandwidth is obtained which this circuit can convert to gain.

The principle described will also work in transistors, but three gain stages are required so as to have enough gain to make the resistance below the potentiometer arm negligible when inserted in the emitter leg of the first gain stage. Emitter bypass capacitors can be omitted with the resultant gain loss and improved linearity. Gain can then be made up by the additional gain circuit.

Grouping Amplifier

COMBINING several frequencies on one output, as required in frequency multiplexing systems, is done by the circuit shown. It permits connection of several high impedance sources to a low impedance as in an operational amplifier adder arrangement. The low input impedance is obtained in the first stage by operating it in the grounded base configuration.

Greater than 40 db isolation between inputs is provided and all spurious signal outputs are 40 db below any single desired signal in the composite output when each input is held below 0.25 v, rms.

Resistors R_{25}, R_{26} and C_4, C_5 are power supply decoupling nets which may be varied according to specific requirements. R_{21}, R_{22} and R_{27}, R_{28} are conventional biasing networks and work in conjunction with R_{23}, R_{24} and R_{29}, R_{30} respectively to maintain proper transistor biasing for a maximum of dynamic range within the circuit.

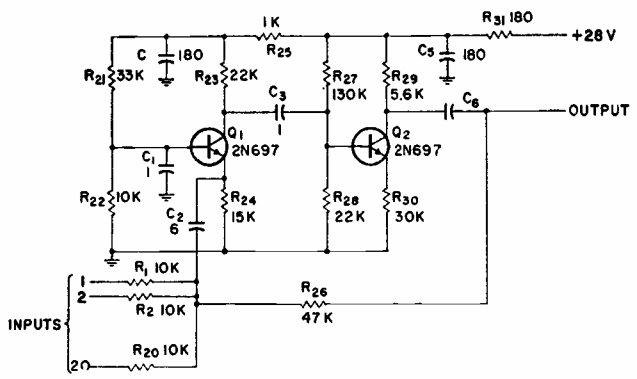
Capacitor C_1 holds the base of Q_1 at signal ground; C_3 is a conventional coupling capacitor. C_2 is an in-

put coupling capacitor and must be chosen large enough to present a negligible impedance compared to the input impedance at the emitter of Q_1 (approximately 50 ohms) plus the parallel source impedance of all inputs each in series with 10K. R_1 through R_{20} are input resistors which insure high isolation betwees any two input signals. The gain of the amplifier for any one input is nearly proportional to the value of these resistors, and the value may be varied according to application depending on desired gain and input source impedance.

The gain of the circuit from any one input to output may be approximated closely as follows: Since the emitter of Q_1 is very nearly at signal ground potential, a 1-volt signal at input 1 causes 0.1 ma in R_1. Practically all this current flows into the emitter Q_1 ($Z_{in} = 50$) and appears at the collector. At the collector the current divides into three paths of interest, R_{23}, R_{28} (in parallel with R_{27}) and the base of Q_2.

The input impedance to Q_2 is approximately h_{fe} times 1K or say 44K. Thus the 0.1 ma at the collector of Q_1 divides into 0.04 ma to R_{23}, 0.04 ma to R_{28}, and 0.02 ma to the base of Q_2. This last current causes h_{fe} times 0.02 ma to flow in the collector of Q_2. Thus without the negative feedback resistor R_{26}, the output voltage is approximately $44 \times 0.02 \times 5.6K = 5$ volts. The gain of the circuit without feedback is therefore 5. With no external load, $5.6/47 = \frac{1}{8}$ the output current returns to the input. The transfer gain, K, is then $K = A/[1 + A(\frac{1}{8})] = 3$.

The small amount of negative feedback was found to greatly improve linearity at high output levels. It may be determined statistically that with 20 inputs each at 0.5 v rms and with a transfer gain of 3 the output voltage will exceed peaks of plus and minus 13.5 volts five per cent of the time; this assumes a Gaussian voltage distribution. Clearly the preservation of linearity at high output levels is necessary if many inputs are used each at a convenient level. Since the circuit is unconditionally stable, R_{26} can be chosen according to application to vary gain, output impedance, etc.

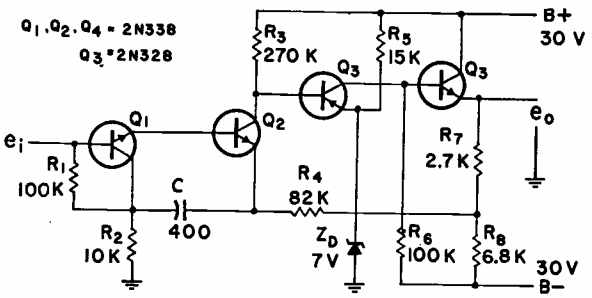


Up to 20 inputs can be handled by grouping amplifier.

High-Impedance Preamplifier

PREDICTABLE performance and reliability over extremes of temperature and variations of transistor characteristics are features of the circuit shown. The measured input impedance over a temperature range of 30 C to 95 C is 32 megohms.

The input impedance is a function of two negative feedback loops. The minor loop couples the signal



Gain of the high-impedance input amplifier is 13 and output impedance is 20 ohms. Frequency response ranges from 0.5 cycle to 20 kc.

at the emitter of Q_2 back to the collector of Q_1. The major feedback path samples a portion of the output signal at the junction of R_7, R_8, R_4 and couples it to the emitter of Q_2. The gain of the amplifier is determined by the ratio of R_4 to R_8. The major feedback loop also controls the dc voltage level at the emitter of Q_4, keeping it constant.

For example, if the dc voltage at the emitter of Q_4 tends to change in a negative direction, then a fraction of this change is observed at the junction of R_4, R_7, and R_8. Current flow into Q_2 will increase, and the base of Q_3 will become less positive. This change is then compared to the zener diode potential and the difference is amplified by Q_3 and Q_4.

This action continues until the dc voltage at the emitter of Q_4 stabilizes at its previous level.

DC Amplifier Has Infinite Input Impedance and 80 db Power Gain

THE amplifying system shown in Fig. 1 exhibits a power gain in one stage which approaches three times the maximum power gain of any other semiconductor device. Its input impedance is much greater than any known semiconductor circuit and much higher than any tube circuit, except an electrometer tube.

The system consists of an input signal which frequency modulates a Hartley type oscillator, and a detector for the modulated signal. A change in

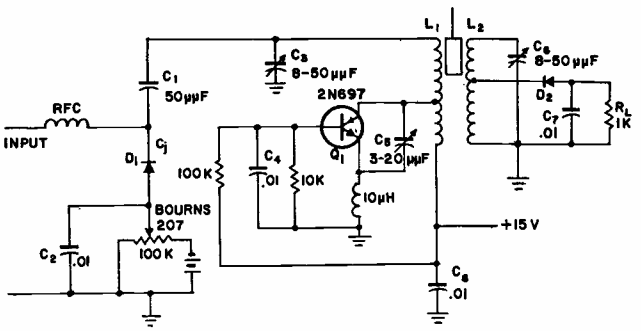


FIG. 1 — Frequency-modulated oscillator and slope detector provide high-gain dc amplifier.

the dc voltage applied to the input will change the oscillator frequency and the slope-detected output. It is, therefore, a dc amplifying device.

The oscillator acts as a power source which feeds the detector. The slope detector responds only to a change of frequency, delta, which it converts to a change of output. The conversion efficiency is determined by the portion of the slope used and the Q of the characteristic curve. The delta power-out is a function of the delta frequency and the oscillator power.

The delta frequency is also a function of the signal input. Increasing the oscillator power increases the gain, therefore the gain is variable and can be designed for any value required. Since output loading has no effect on input signal, it is a purely unilateral device.

Referring to the circuit diagram: a dc voltage impressed on the input terminals would be impressed in series with the bias path. The dc resistance of the diode is 1,000 megohms or 10^9. With one volt applied, the power input will be 10^{-9} watts. If we can get 10^{-3} watts at the output, we have realized a 69-db gain. In an experimental model, a diode of 2.4×10^{11} ohms was used to give a one-milliwatt output. Calculated power gain was 80 db.

If an ac signal is applied, the signal sees the junction capacitance C_j in parallel with C_1 to ground since L_1 represents no reactance until the rf frequencies are approached. The Z_{input} is, therefore, capacitive and can be designed to a small value.

In the experimental model the input capacitance C_j plus C_1 was 70 μμf, with an oscillator frequency of 30 mc. There is a good argument for a higher oscillator frequency, which would allow much lower C_j plus C_1. If a unit could be designed with C_j plus C_1 of 1 μμf, the Z_{in} at 10 kc would equal 15 megohms.

It must be noted that the dc return path for the diode bias voltage is through the input terminals. The signal source must have a dc path through it, but the resistance of this path may be as high as 500 meg without disturbing the circuit.

The frequency response of the device is in the audio range and though this represents a limitation to the circuit, it can be improved with further design. A patent is pending.

Failure-Proof Amplifier

THIS circuit was developed as part of a highly reliable military communications system. In several locations in this system it is necessary to provide dual circuitry for all transistor networks, since these networks are the most prone to failure. The most common network is an amplifier, and the following circuit provides for the interconnection of two identical amplifiers such that a failure of any transistor in either amplifier results in no change in output power.

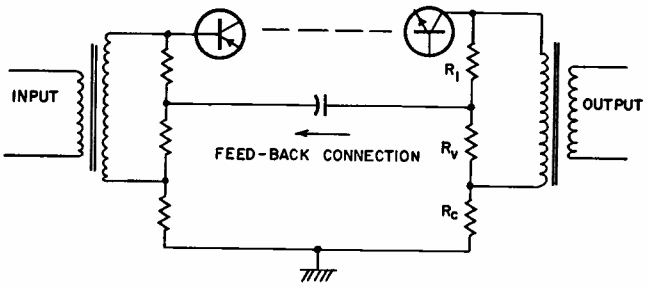


FIG. 1—Simplified schematic of bridge feedback amplifier.

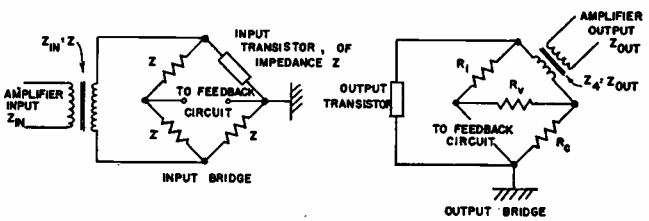


FIG. 2—Input impedance equals transistor input impedance when feedback is divided equally between series and shunt with the input, as shown. Output impedance is controlled by derivation of feedback voltage from current and voltage of the output.

All major amplifiers in the system use a bridge feedback arrangement which provides close control over input and output impedances and gain response, this being conducive with the system's high quality performance. A simplified schematic of a bridge feedback amplifier is shown in Fig. 1.

A voltage is developed across R_c which is proportional to the current in the load, and the voltage across R_v *is* proportional to the voltage across the load. The addition of these voltages is fed back to a bridge in the input circuit. The input bridge is balanced to divide the feedback voltage into series and shunt with the input signal.

Figure 2 shows the input and output bridge redrawn to indicate the balance conditions used in the application. The output bridge controls the output impedance, and the input bridge controls the input impedance. As stated, two amplifiers were paralleled to maintain a through circuit should one amplifier fail.

Figure 3 shows how the input signal is divided to feed both amplifiers by using separate windings on the input transformer. Combination of the outputs is achieved through a two-core hybrid arrangement, the need for this hybrid will be explained later.

The trick in this circuit is the common feedback path to the input of both amplifiers. Consider the case when both amplifiers are identical, both having the same open-loop gain and phase. Note the polarities at the output from each amplifier, points *a* and *b* are at the same potential. It would therefore be possible to connect the feedback lines at *XX*, instead of returning individual feedback voltages to their respective amplifiers, i.e. *a* to c and *b* to *d*, with no change in output level.

If, with the common feedback we fail one amplifier, by removing a transistor for example in amplifier *B*, then the voltage developed at *a* would see an identical feedback circuit consisting of the input and output bridge of the failed amplifier connected across its own bridge circuits. The voltage at *a* is therefore reduced to one half its former value resulting in 6

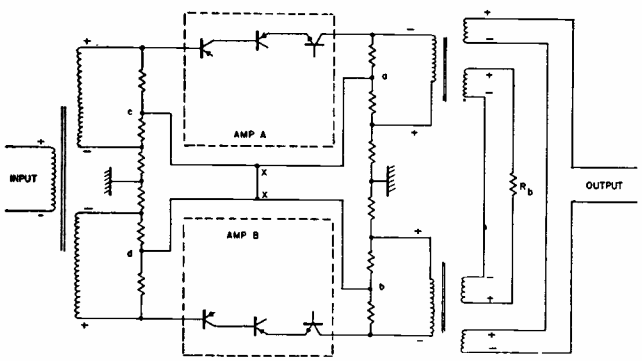


FIG. 3—Failure-proof amplifier showing common feedback connection.

db less feedback, or 6 db more gain in *A*.

This extra power from *A* is divided equally between the hybrid balance resistor R_b and the output, thereby maintaining an output level at the value held before transistor failure. Without the hybrid and its balance resistor we would not be able to maintain an unchanged output level.

It is common that the individual amplifiers may have different open-loop gain responses and one amplifier may gradually deteriorate due to ageing of transistor parameters, for example. Under these conditions the common feedback connection serves to select the amplifier having the highest open-loop gain, and hence better distortion and level stability, to do more work in a ratio greater than that of the open-loop gain differences. The better amplifier will develop a larger feedback voltage, a voltage higher than that required by the poorer amplifier will have its gain suppressed still further than if its own feedback voltage was operating alone.

As stated previously, the balance resistor, R_b, receives the same power as is delivered to the load under extreme conditions where one amplifier is failed. When both amplifiers have the same gain response then no power is delivered to the resistor as can be seen by inspecting the phasing of the hybrid windings. However, the probability of having two identical amplifiers is slight, so a voltage will usually appear across R_b due to the gain differential. Accordingly it is convenient to establish a maximum allowable gain differential between amplifiers and to monitor the voltage developed across R_b. By this means a failing amplifier may be located in service and replaced with no interruption of system operation.

Degradation of transistor parameters or removal of any transistor is completely protected with respect to output level and reflection coefficients at both input and output of the amplifier. If a short-circuit occurs within the transistor, then impedance changes may result, depending upon where the short is placed.

Any configuration of amplifiers can be used, provided the phasing is arranged to be as shown in the diagram. The configuration shown has been used in our own application with success.

Adjustable Temperature Compensation

A FAIRLY COMMON REQUIREMENT is a wide band operational or integrating amplifier with good dc stability. Rise time and overload considerations force a choice of transistor and operating point for the input stage which makes reduction of the net input current difficult. In an extreme case, an adjustable base current supply with adjustable temperature coefficient becomes necessary. An example of such a design is shown in Fig. 1.

The 1N754A and 1N758A Zener diodes were used to gain some immunity from supply voltage change, and have no further significance. Pot R_4 is a voltage zero adjustment with a range of about ± 0.1 v. No temperature compensation is provided here, as 2N706's selected for roughly equal base currents at 1-ma emitter current usually have base-emitter voltage drops that track within a few microvolts per degree.

The network on the left-hand side is designed to provide the base current required by an average 2N706 operating at 1.1-ma emitter current. This is about 30 μa at room temperature, decreasing at

about 0.3%/°C, or about 18 μa over 60C. Transistors with $20<I_B<40$ μa are selected for the stage, as accommodation of a larger range yields difficulties with potentiometer resolution. R_2 is adjusted for zero volts on its arm at 25C. This voltage decreases about 3.5 mv/°C due to the coefficient of the 1N276's, providing by way of R_3 the required temperature dependent part of the base current. R_1 and the selected resistor provide the remaining base current.

Operation of the circuit is most easily described by outlining the adjustment procedure. The complete amplifier is connected as shown in Fig. 2, where V_2 provides an easy measurement of net input current $I_{in} = /V/100K$. R_3 is set at its open spot or disconnected. R_1 and the selected resistor are adjusted for $V_2 = 0$. R_4 is set for $V_1 = 0$. R_3 is then set to about mid-range, and R_2 set for $V_2 = 0$. It should now be possible to rotate R_3, which controls temperature coefficient, over its entire range without affecting V_2. These operations are comparable to balancing a bridge to the end that the temperature coefficient adjustment will have no effect at room temperature. The temperature is then shifted to, say, +50C, and R_3 adjusted for $V_2 = 0$. The remaining coefficient varies slightly with temperature, and an optimum adjustment will require a plot over the working range with a second compromise adjustment of R_3. A plot of a typical amplifier after final adjustment is shown in Fig. 2.

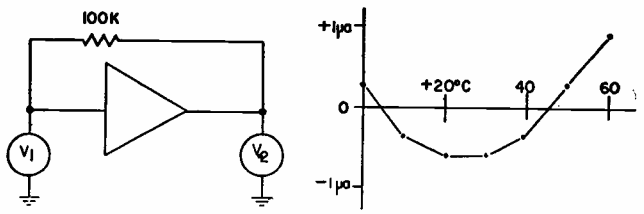


FIG. 2—Measurement setup and plot of temperature

As a matter of interest, a second order, or curvature, correction could probably be made with a thermistor. At about this point, a chopper stabilizing scheme seems a more sensible approach.

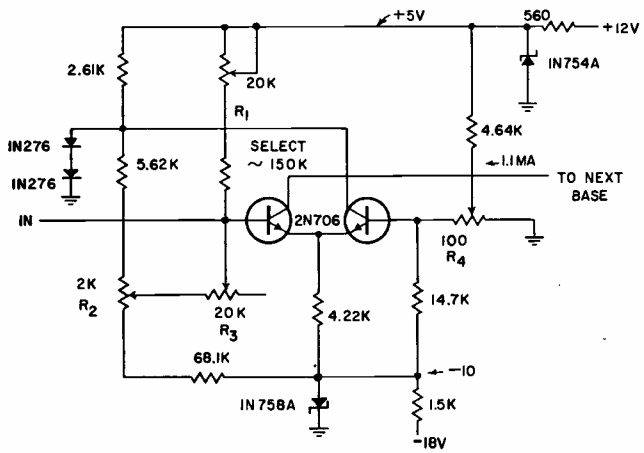


FIG. 1—Temperature coefficient is controlled by R_3.

Simplified Operational Amplifier

IN-FLIGHT analog computers frequently require single-ended operational amplifiers with reasonable drift requirements and few components. Typical specifications include an open-loop voltage gain of greater than 72 db with a closed-loop bandwidth to 1 kc. Output swing should be two-thirds of B+ into a 200-milliwatt load. The input should draw negligible amounts of power from the summing network.

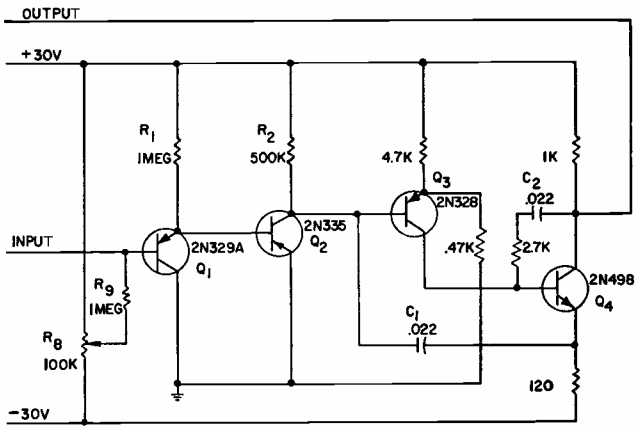
Design specifications require three direct coupled inversion stages (Q_2, Q_3, and Q_4) for high gain and phase inversion and an emiter follower input stage (Q_1) to obtain the high input impedance. Drift stabilization is performed by the unique common mode operation of Q_1 and Q_2. The output stage Q_4 is of high voltage, medium power design for output requirements. High frequency stabilization is obtained through C_1 and C_2, their associated resistors and the intrinsic collector capacitance of the transistors. An offset bias network is provided by R_8 and R_9.

Precise selection of the transistors simplified the circuitry besides considerably assisting the drift and stability problems.

Silicon transistors were used throughout to minimize drift. The reasoning behind the choice and circuitry of Q_1 and Q_2 is observed from a form of the well-known transistor collector current equation:

$$\Delta_T I_c = -\alpha_N I_{co}(e^{qV_e/k\Delta T}-1) + I_{co}(e^{qV_c/k\Delta T}-1)$$

From this equation it is observed that the change in collector current due to change in temperature is minimized if the emiter and collector voltages are made small. This was done by operating Q_1 and Q_2 at low collector currents and arranging their collector voltages to be small. The pnp to npn choice



Schematic of simplified transistor operational amplifier.

of Q_1 and Q_2 was to obtain the input potential near zero volts and provide a common mode cancellation of V_{be}. The final selection of R_1 and R_2 is a matter of inverse temperature curve matching to cancel the effects of V_{be} on Q_1 and Q_2 and to minimize the drift of succeeding stages in the circuit. The starved operation of the first stages is also advantageous in that little current is drawn from the input network and they operate at low internal power. The production drift tolerance curve is presented on Fig. 1.

Specific transistor characteristics are also used in eliminating multiple stabilization networks. The Miller Integrator effect was used in conjunction with transistors Q_3 and Q_4 to minimize the size of

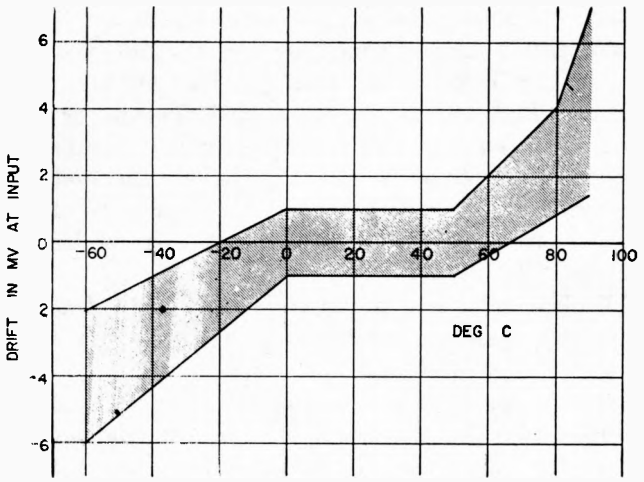


FIG. 1—Temperature-drift range of operational amplifier.

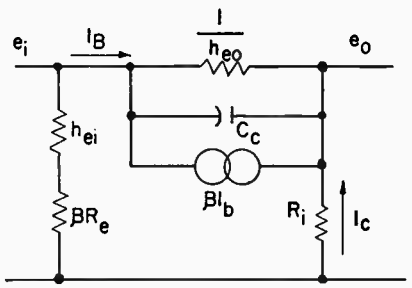


FIG. 2—Transistor equivalent circuit.

C_1 and C_2 which were used in the first two roll-off networks. The third, fourth and fifth lead-lag networks are the transistors Q_3, Q_1 and Q_2 respectively. The equivalent circuit used for the transistor network is given in Fig. 2. From this the individual transistor transfer function is derived. In practical form this transfer function is

$$\frac{e_o}{e_i} \cong \frac{-\beta R_L}{(h_{ei}+\beta R_e)} \left[\frac{(h_{ei}+\beta R_e)\ C_c\, s+1}{\beta R_L\ C_c\, s+1} \right]$$

From this equation, the lead and lag time constants can be manipulated by variation of R_e (emitter resistance) and R_L (load resistance). The total

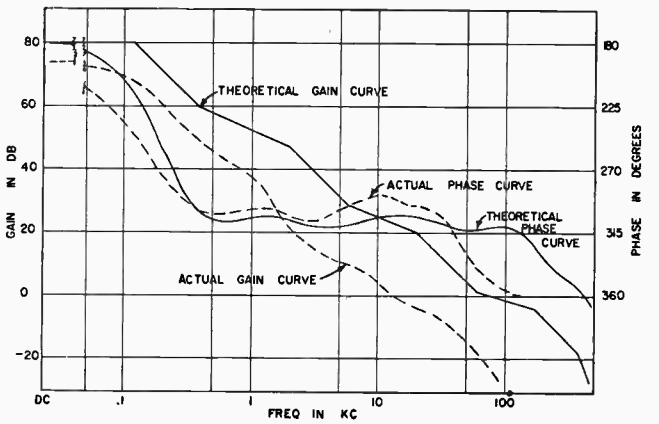


FIG. 3—Phase-gain characteristic of operational amplifier.

transfer function is a multiplication of the transistor transfer functions with the additional network functions. The total phase-gain plot for the theoretical and for the actual design is given in Fig. 3.

Because of Q_1 and Q_2 input circuitry, only B+ had to be stabilized and then only to 1 per cent. Due to power dissipation from the input network, summing components of less than 200K are preferred.

The circuit met and in most cases far exceeded the original requirements.

Sensitive Relay Control Amplifier

A REFLEX CIRCUIT is employed to ensure full use of the available gain of a two-stage relay control amplifier. In a conventional amplifier, the tube which controls the relay in its plate circuit acts only as a dc amplifier. In the circuit of Fig. 1, the same tube is also used as an ac amplifier, thereby increasing the overall sensitivity by a factor approximately equal to this ac gain.

The arrangement is especially useful in cases where there is insufficient space for more than one tube envelope. A high conductance twin triode, a 12AT7, provides a relay control triode of good sensitivity while the mu of 50 is sufficiently high to ensure gain stability in the degenerative amplifier of V_1.

Best results are obtained at high signal frequencies (400 cps or more) where advantage can be taken of the relay inductance providing a higher ac impedance to V_2 resulting in increased gain. The input signal is applied through the transformer which may be of any ratio provided that the secondary resistance is low. One 0.5 μf capacitor acts both as an insulator and dc filter forming a smoothing network in conjunction with the 100K resistor and 0.5μf reservoir capacitor. The amplified signal at V_2 plate is applied to the grid of V_1. The output of V_1 is rectified in a voltage-doubler circuit and the

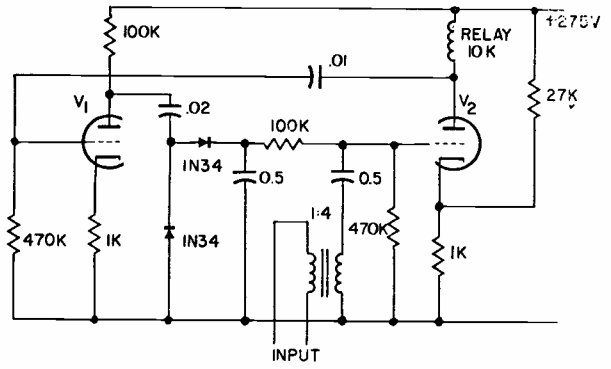


FIG. 1—A 10-mv rms 60-cps signal to this sensitive amplifier energizes the relay.

resulting positive dc potential controls the grid of V_2 and hence the condition of the relay. In the absence of a signal, the relay is held off by the cathode bias provided by the 1K and 27K resistors (about 9 volts).

Time Amplifier

A SIMPLE CIRCUIT to amplify time generates an output pulse width that's a linear function of an input pulse width. The circuit is stable, easy to calibrate, and adaptable to a wide range of time-amplification factors and pulse widths. With two stages, the circuit can amplify nanosecond pulse widths to seconds.

Operation of the circuit is based on the fact that the voltage across a capacitor charged from a constant-current source is directly proportional to the value of current and the length of time the current is applied. When a constant current charges the capacitor for a length of time, the time required to return the capacitor to its original voltage with another constant current of opposite polarity will be a linear function of the ratio of the two currents (Fig. 1). Linearity of the function depends on the capacitance, voltage change, and current ratio. Accuracy of time amplification depends only on the accuracy of the two currents.

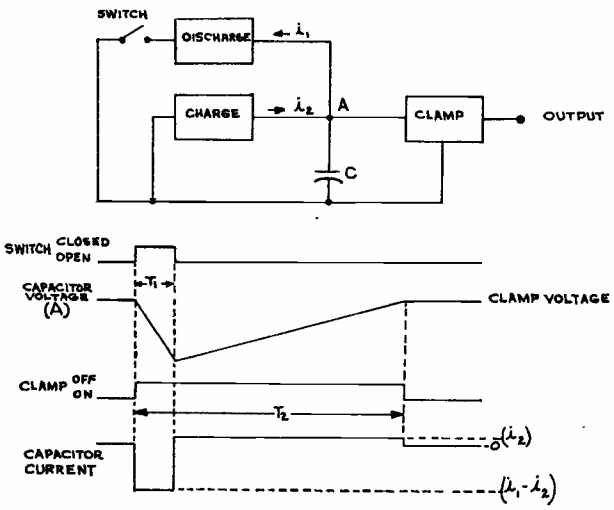


Fig. 1. Block diagram of the time amplifier and timing waveforms.

The circuit (Fig. 2) includes an input switch, a constant-current discharge load, a constant-current charge generator, and a voltage clamp. The input switch Q_1 turns on the constant-current discharge circuit for the duration of the input pulse. Q_2, R_1, and voltage reference V_1 form the constant-current-discharge load. Emitter resistor R_1 provides a feedback path for collector current and thereby generates a constant current discharge approximately equal to V_1/R_1.

Voltage source V_3 and R_2 form a simple constant-current charge generator. This current remains on at all times. It is switched between capacitor and voltage source V_2 by the base-to-emitter junction of clamp transistor Q_3, whose collector circuit generates the output pulse.

During static conditions, the charge current is switched through the clamp, thereby providing an output voltage equal to V_2. When a pulse is applied to the input switch, the capacitor starts discharging at a constant rate. At the same time, the voltage change across the capacitor back biases the clamp transistor and the collector switches to V_1. The actual capacitor current is now the difference between the discharge and charge currents. When the input pulse is removed, the capacitor starts to recharge and continues until the capacitor voltage reaches approximately V_2. Then the clamp transistor switches on, stopping the capacitor charge and switching the output voltage back to V_2.

After the clamp has switched, another input pulse may be applied. If several input pulses are applied during one cycle, the circuit will add and amplify the total time of the input pulses.

Most of the circuit's components are not critical. The only strict requirements are for the current-determining resistor and power supplies. The simplest design approach is to determine the discharge current first. It is limited by the rating of the input switch and discharge transistor. The duty cycle and input pulse width are also determining factors.

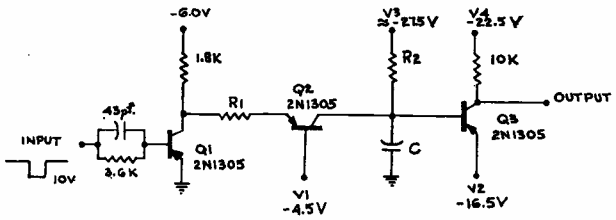


Fig. 2. The time amplifier.

Input Microseconds	R_1	C_1	R_2	Output Milliseconds
0.1- 1.0	51Ω	8200pf	3.2M	0.1- 1.0
1.0- 10.0	51Ω	.082μf	3.2M	1.0-10.0
10.0- 100	510Ω	.082μf	3.2M	1.0-10.0
100 -1000	510Ω	.82μf	320K	1.0-10.0

Component Values for Several Time Amplifications.

After the current has been chosen, the capacitor value can be calculated from the maximum input pulse width and allowable voltage swing (less than $V_2 - V_1$). The charge-current circuit values can be calculated from the discharge current and the required amplification. A few values are shown in the table.

The remaining components are determined from requirements for back biasing and signal-level control. The charge current must be large compared to the collector leakage of the discharge transistor and emitter-to-base leakage of the clamp transistors. If leakages were constant, they could be calculated into the circuit.

High Input-Impedance, Unity-Gain FET Amplifier

TELEMETRY DATA-PROCESSING applications frequently require unity-gain amplifiers with a dc input impedance approaching that of an electrometer tube, and a performance level approaching that of a chopper-stabilized potentiometric amplifier. Common applications would be for sample-and-hold demodulation, and active filters.

The design is based on a field-effect transistor driving a compound emitter-follower buffer. The compound emitter-follower performance is typically at current gain of 2500 and a voltage gain of 0.995. Output voltage from the compound emitter follower fed back to the field-effect transistor does two things: it multiplies the naturally high input impedance of the field-effect transistor by a factor of about 200; and it linearizes the operation of the field-effect transistor by keeping its current or voltage supply very nearly constant.

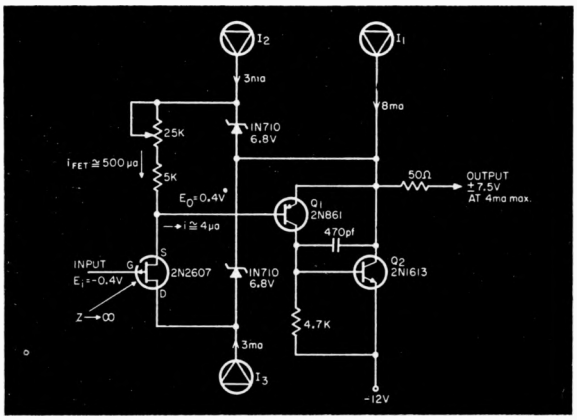


Fig. 1. High input-impedance, unity-gain amplifier. Three constant-current sources supply the circuit, composed of a p-channel field-effect transistor driving a compound emitter follower.

Power for the field-effect transistor is derived from the compound emitter-follower output via two positive-feedback (boot-strapped) voltage sources (See Fig 1). Complementary voltage cancellation is achieved with a Siliconix p-channel field-effect transistor driving a 2N861 pnp silicon-alloy transistor. Adjustment of the potentiometer in the field-effect transistor source supply permits the output voltage (E_o) to be the same as the input voltage (E_i). In practice, E_i can be grounded with a clip lead and the potentiometer adjusted until E_o is at ground level. At this point, the gate-source bias voltage of the 2N2607 equals the base-emitter voltage of the 2N861. This set-up procedure automatically establishes an optimum point of high transconductance for the field-effect transistor.

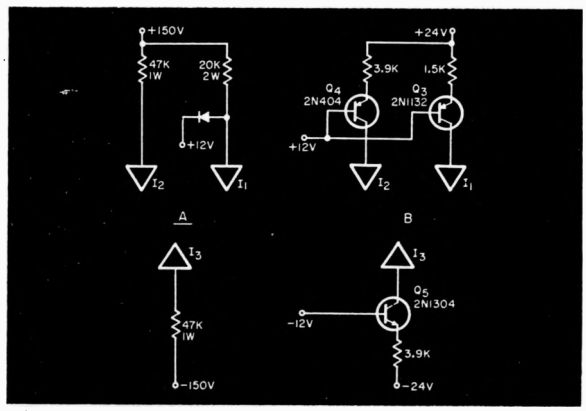


Fig. 2. Constant-current sources.

Two current sources are shown in Fig. 2. Current source *A* is very simple, but requires 150 v. This supply does not have to be a highly regulated voltage. Current source *B* is very effective, but requires 3 additional transistors. For single units, the zener diode boot-strap voltages could be replaced with isolated power supplies or batteries.

DC Drift Voltages Reduced With Ungrounded Supply

ALTHOUGH DIFFERENTIAL AMPLIFIERS can be used to reduce drift voltages. they have the disadvantage that one side of the input and output cannot be simultaneously grounded. However, if the power supply is allowed to float with respect to ground, the drift voltages

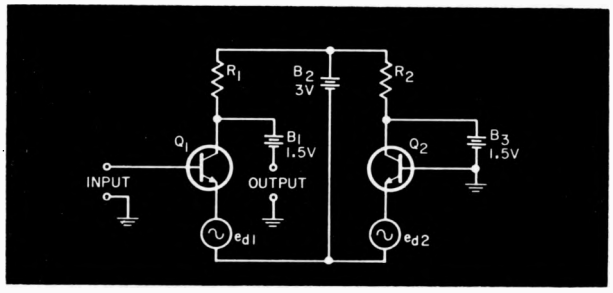


Fig. 1. Simplified circuit showing floating power supply.

can be cancelled and the amplifier can be made single-ended.

Figure 1 shows a simplified amplifier circuit of this type. In this circuit the drift voltages are shown as e_{d1} and e_{d2}, which we assume equal. The 1.5-volt battery B_2 fixes the collector-to-base voltage of the non-signal carrying transistor Q_2, and the other voltages adjust for this particular base-to-collector voltage.

Let us assume that the drift voltages e_{d1} and e_{d2} are external to the transistors and that, because e_{d2} is small compared with the supply voltage B_2, the current through Q_2 is constant. Then it follows that the bias voltage for Q_2 must also be constant. The emitter of Q_2 as shown

in Fig. 1 is thus at a fixed voltage with respect to ground. The negative terminal of B_2, however, moves with respect to ground by the amount of variable voltage e_{d2}. The emitter of Q_1, however, does not move with respect to ground because it differs from the voltage at the negative end of B_2 by e_{d1} which equals and cancels e_{d2}.

If Q_1 and Q_2 are identical and if negligible base currents flow and if no output load is present, then the voltage at the collector of Q_1 will be the same as at the collector of Q_2, because the circuit is symmetrical. Also, since B_1 is the same voltage as B_3, the output voltage is the same as the negative terminal of B_3, namely ground potential. If an input signal is introduced and if the base currents still are negligible and no output load is present, Q_1 will operate as a normal amplifier since its emitter is fixed with respect to ground. We now have an amplifier stage, the output voltage of which is centered about zero, having one side of both input and output grounded, and with drift voltage cancelled out.

In an actual amplifier the results differ slightly from an ideal amplifier because of base current flow and because of the output load. Most of the drift voltage originates inside the transistor instead of outside as shown, but the results are as described. Drift voltage is, of course, not entirely cancelled, but is greatly reduced.

Figure 2 shows a practical two-stage preamplifier,

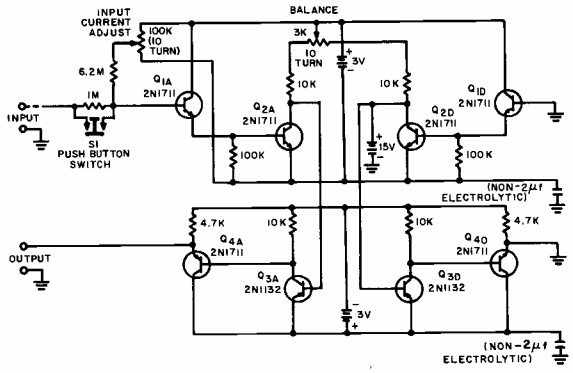


Fig. 2. Practical two-stage preamplifier.

which uses emitter followers at the input to increase the input impedance to about 1 meg and also uses emitter followers at the output to decrease the output impedance to less than 1000 ohms. Note that with pnp and npn transistors one battery can be eliminated (B_1 of Fig. 1). Each signal-carrying transistor, such as Q_{1A}, and its associated drift-cancelling companion, such as Q_{1D}, should have a common heat sink. Voltage gain is about 200. Steady-state current drawn by the input circuit may be reduced to zero by first shorting the input and then adjusting the input current control until the output voltage does not change when S_1 is opened. ◆◆

Amplifier with DC Controlled Gain

IN CERTAIN circuit applications it is desired to control the gain of a small signal amplifier by means of a dc voltage. By so doing, the adjustment potentiometer (if one is used) does not carry signal current, and remote control is easy. In order to obtain dc-controlled gain, an element must be used whose impedance is a

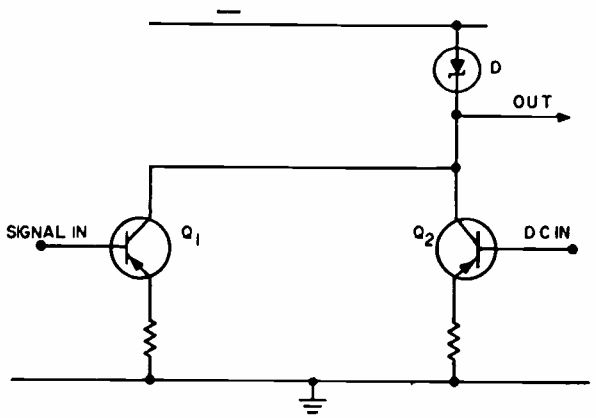


Fig. 1. Basic circuit of amplifier with dc controlled gain.

function of the current passing through it or of the voltage across it. In the circuit shown, a Zener diode is the element which controls the gain of the amplifier.

The basic circuit is shown in Fig. 1. Q_2 is a dc current generator whose current is controlled by the base voltage. This current passes through Zener diode D. This Zener is the collector impedance of linear amplifier Q_1. The high output impedance of Q_2 is seen by Q_1 in parallel with Z_d and can be ignored.

When the input signal is large, the diode current will vary with the signal and distortion will occur. Small input signals are therefore necessary; and, if

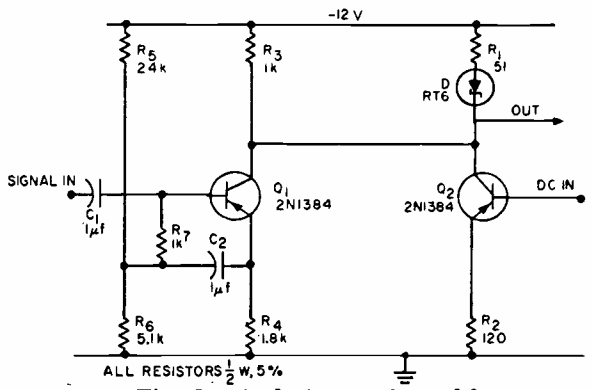


Fig. 2. Final circuit of amplifier.

needed, a suitable attenuator can precede Q_2 so that the input signal will be sufficiently small.

The complete circuit is shown in Fig. 2. The Zener diode is an RT 6 which has a nominal breakdown of 6 v. Zeners with breakdown voltages of 6 v and higher have dynamic impedances which are quite independent of temperature variations.

Resistor R_1 is in series with D so that the output signal will not be too small when the current is set for maximum value. Resistor R_3 limits the maximum gain to some reasonable value and prevents saturation of Q_1. The input of Q_1 is bootstrapped to obtain a large value for the input impedance with relatively small values of divider resistances. The input impedance is approximately the parallel combination of βR_4 and $R_4 R_7 / r_e$; where $r_e = 25/i_e$. Here βR_4 is about 90 k and $r_e = 25$ ohms, so that the input impedance is about 40 k.

The expression for the gain is

$$K = \frac{R_3 (R_1 + Z_d)}{R_1 + R_3 + Z_d} \left(\frac{1}{R_s}\right),$$

where

$$\frac{1}{R_s} = \frac{1}{R_4} + \frac{1}{R_5} + \frac{1}{R_6}.$$

With the values shown, this becomes

$$K = 0.8 \frac{Z_d + .05}{Z_d + 1.05};$$

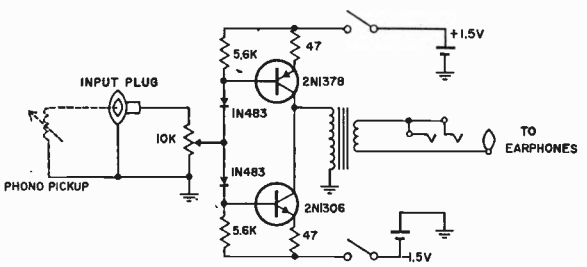
from which follows $K_{min} \cong 0.04$ (when $Z_d = 0$)
$K_{max} \cong 0.80$ (when $Z_d = \infty$).

In the circuit of Fig. 2 the control voltage is limited to −4 v. Thus, the gain is adjustable between 0.04 and 0.70, a range of 1 to 18. The input signal is a sine wave of 1 v p-p, and the output shows negligible distortion and negligible variation with temperature variations.

One application for the circuit is the automatic volume control of radio circuits. Also, a constant amplitude signal generator can be developed from this circuit. Other possible applications are in waveform generating circuits.

Opposed Collector Audio Amplifier

THE AMPLIFIER SHOWN is of interest because of the opposed collector method of achieving high gain. Presently the unit uses standard large size components, two pen cells for power, and is constructed in a 1-1/4 x 2-1/2 x 3-3/4 in. plastic case.



Opposed collector audio amplifier.

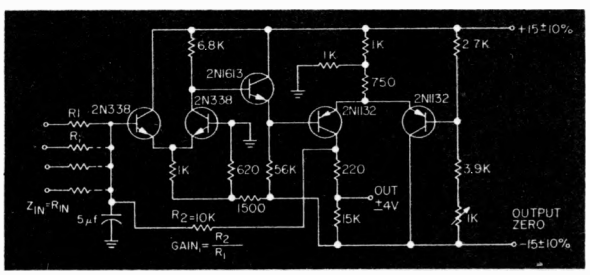
The basic circuit is an adaptation of a push-pull outage stage. 1N483 silicon diodes (similar types can be substituted) provide the proper dc bias levels. High beta germanium transistors and small emitter resistors supply a large current swing to the output, transformer with only millivolts of input.

The advantage of the opposed collector connection is that although the transistors are drawing nearly 13 ma, the currents balance closely and little resulting current flows in the collector load. Further, since the beta of these transistors is near 100, the transferred emitter impedance is not excessively low for most magnetic pickups. Too, the dc base current tends to flow out of the base of one transistor and into the other, again minimizing the resultant dc through potentiometer and pickup. Finally, because of these balanced conditions and the known high impedance of an open collector, voltage gain is proportional to collector load impedance up to gains of over a thousand. Gains of this magnitude are obtained with larger batteries, zeners instead of diodes in the input path, and a 100 K collector load impedance. Also, adjustment of the emitter impedances may be necessary to balance the two opposed currents. The circuit can then be used as a low level dc comparator or a sine wave clipping circuit with sensitivity of a few millivolts. Substitution of two parallel, oppositely polarized silicon diodes for the collector load further improves the wave squaring characteristics of this circuit. Gain achieved this way instead of with cascaded stages actually uses less package space because no coupling or bypass capacitors are needed at all.

This omission of capacitors plus pickup loading probably account for the frequency response of the unit into dynamic speaker earphones despite the fact that no recording characteristic compensation was used. High impedance magnetic earphones will not give good results due to their very limited bass response. High fidelity pickups having 10 mv output at standard stylus velocities will have very good listening volume, and pickup having output above 3 mv will be satisfactory. For low impedance stero-phones (both sides driven in parallel) a 5 K to 4 ohm or a 2.5 K to 1.8 ohm transformer is best and easily obtainable. High impedance (two thousand ohms) phones can be connected directly in place of the transformer primary if their dc resistance isn't too high, 400 ohms being a practical limit, and lower R being preferable.

Minimum-Interaction Summing Amplifier

THIS IS AN OPERATIONAL-TYPE amplifier that uses current-summing to hold the voltage at the input node, point *A*,



Minimum-interaction summing amplifier. Feedback through R_2 maintains point A at zero volts.

at zero volts. If more than one input is used, there will be an exact summation of the inputs, with no interaction between inputs.

This is accomplished as follows: A positive signal at the input will cause a current AV/R_i to flow into the node. The output causes a current of AV/R_2 to flow out of the node, and since $A = R_2/R_i$, the node voltage is held at exactly zero volts.

The gain from any input to the output is merely the ratio or R_2/R_i, where R_i is the series resistor at that par-

ticular input. Any gain from 0.01 to 1000 is possible.

The 5-μf input capacitor prevents oscillation and removes noise from the input. At first it may seem to limit the amplifier to dc summing, but since the input node is always at zero volts, the input capacitor does not degrade frequency response.

As a sine-wave amplifier with a gain of 1000, the bandwidth is dc to 20 kc, and this may be increased to 5 mc with better transistors. ◆◆

High-Level Wide-Band Video Amplifier

THIS CIRCUIT was developed to drive an 8 v pulse into a 100 ohm load. The circuit uses emitter degeneration in the first stage and negative feedback in the second stage.

The frequency response of the amplifier is from 5 cps to 30 mc. The voltage gain is 26 db, and the undistorted sine wave output is 10 v p-p into a 100 ohm load. The circuit gives good linearity and has good stability.

Frequency response can be increased to 50 mc by adjusting the bypass capacitor, C_2, of Q_1 and by adjusting the bias.

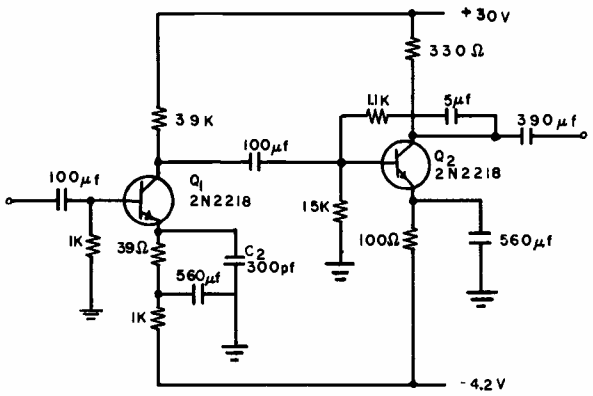


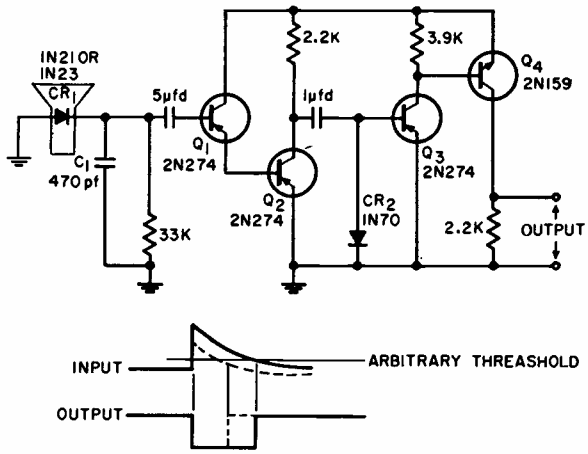
Fig. 1. Wide-band video amplifier.

Logarithmic Amplifier for Radar Signals

THE CIRCUIT shown in Fig. 1 has highly linear log output over a 30 db dynamic range, and has been used in obtaining antenna patterns on an operating radar system. Its output current is directly proportional to the pulse repetition frequency and log of the peak rf pulse power.

The underlying principle is based on the fact that the time required for an exponential discharge to reach an arbitrary constant value is proportional to the log of the starting voltage. The 470 μf capacitor, C_1, is charged by CR_1 to a value that is a function of the power into the detector mount. At the end of the radar transmit pulse, the voltage across C_1 drops exponentially toward zero. This exponential waveform is amplified in a Darlington amplifier containing Q_1 and Q_2. Some clipping takes place in this Darlington stage for high level input signals.

The positive going input to Q_3 is clamped at ground



Logarithmic amplifier for radar signals

potential by CR_2 and further amplified and clipped by the remaining two stages. The output of the final stage is a negative rectangular pulse of constant amplitude whose duration is proportional to the log of the peak pulse power into the detector mount. This output is suitable for driving an oscillograph.

Starved DC Amplifier Has Low Noise, High Z

TRANSISTORIZED low noise, high input-impedance ac amplifiers often are considered difficult to design—and with good reasons. To optimize the first stage, a careful compromise must be made among transistor parameters: V_{ce}, I_c, h_{FE}, semiconductor material, and base resistance. But if ac amplifier design is obtuse, the problems encountered in dc input stages are multiplied tenfold.

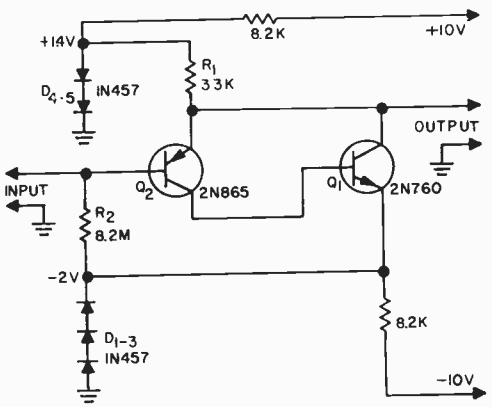
Fortunately the parameters that lead to low noise in a dc input stage, namely starved currents and reduced voltages, also lead to a high input impedance. Actually the term "input impedance" becomes "base current" when referring to dc amplifiers.

A wideband transistor input stage was needed for a chopper stabilized amplifier intended to resolve 10 microvolts. The maximum permissible base current was 10 nanoamps.

The first decision was to use an emitter follower, since wide bandwidth and low noise tend to be contradictory requirements in a voltage-gain stage. Secondly, the low noise figure and minute input-current requirement dictated what has been termed a "squarved" condition (squashed and starved V_{ce} and I_c).

To maintain this condition, forward-biased silicon diodes D_{1-3} and D_{4-5} regulate and decouple the negative and positive power supplies, respectively. Tran-

sistors Q_1, Q_2, form an npn-pnp gain-multiplication pair. The transistors are chosen for low noise, wide bandwidth, and substantial h_{FE} at low collector current. Resistor R_1, a critical factor in deciding noise factor, sets the transistor currents and provides ample drive for the next stage. Resistor R_2 almost completely cancels the base drive current, thereby raising the effective input impedance.



Starved low-uoise amplifier input stage. Emitter follower has wide bandwidth, and input curreut less than 10 ua.

The dc amplifier, when constructed, had a bandwidth of 100 kc, an equivalent input noise less than 10 microvolts rms (neglecting dc drift, which is compensated for by the chopper), and an input current of about 8 nanoamps. Two units can be used differentially to compensate for temperature and power supply changes, resulting in a highly reliable amplifier, or a precision voltage-regulator front-end stage. An additional attractive feature of the design is its high-speed recovery from overload.

Amplifier with Remote Gain Control

WITH THIS CIRCUIT, an operator at a console 1000 feet away can control a wide-band amplifier's gain from maximum to zero with a simple two-wire, low-voltage dc connection.

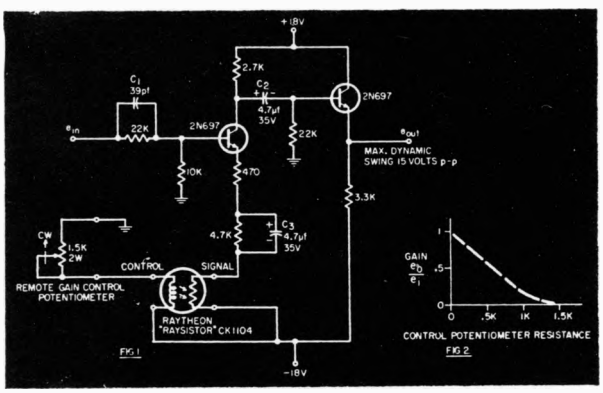


Fig. 1. Remote-gain control operates through Raysistor.

Fig. 2. Gain control characteristic.

The advantages of this circuit are its complete isolation between control and signal circuits; its linear gain control relationship over most of the control potentiometer's range; and its capability for supplying a large-amplitude, undistorted output signal. The circuit in Fig. 1 has a maximum output of 15 volts peak-to-peak. Distortion is low because of the large emitter resistances.

The basic component is a Raytheon Raysistor connected in the emitter lead of a common-emitter transistor amplifier. The photoconductive element of the Raysistor is used as an unbypassed variable emitter resistor. This resistance varies from over 1 meg down to about 600 ohms as the control current to the lamp element changes from 0 to 30 ma.

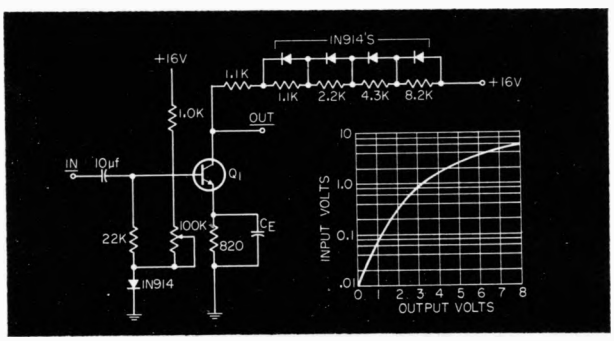
Two methods of gain control are at work. One is simply that the amplifier gain is inversely proportional to the unbypassed emitter resistance; as a rule of thumb, gain equals collector resistance divided by unbypassed emitter resistance. The second is that as emitter resistance increases, emitter current decreases, causing transistor beta to decrease (the effect used in reverse AGC circuits).

The change in Raysistor signal resistance with control current is roughly logarithmic in nature. Beta decrease with decreasing current also is logarithmic. This circuit cancels one logarithmic effect against the other, thus achieving a linear gain control relationship. Figure 2 shows the measured gain control characteristic.

The component values were chosen to satisfy particular requirements, i.e., a maximum gain of 1, a low output impedance, and a certain frequency response.

One Transistor, 50-db Dynamic Range Compression Amplifier

NON-SATURATING AMPLIFICATION of widely ranging video signals often is difficult to achieve in transistor circuits. The amplifier shown provides a minimum output signal level of 1.0 v with an input of 20 mv, but does not saturate with a 5 to 6 v input. In the actual application, the signal is later processed for risetime and duration information.



Wide dynamic range compression amplifier with voltage transfer function.

The circuit provides a minimum gain of 1 and a maximum gain of 15. The diodes across the collector load resistors change the stage gain and impedance by shunting the resistors, one by one, as signal input is increased. The 100-K pot is initially adjusted with zero signal to provide about 50 μa collector current. Q_1 must be a high beta at low current transistor such as a 2N336A. Capacitor C_E is selected for proper frequency response. The voltage transfer function for the circuit is shown in the accompanying curve.

In actual application, two such circuits are cascaded.

The second amplifier provides a maximum gain of 5 and minimum gain of 1. Overall input-output characteristics are 20 mv to 5 v input with 1.5 to 8 v output. By selecting load resistors and diodes, the gain characteristic can be made to follow many curves.

For Class A amplification, the ac-coupled dynamic load is similar except that two diodes are connected in opposite polarity in parallel with the various load resistors and the biasing circuit is altered.

Non-Inverting Pulse Amplifier Uses One Power Supply

THIS PULSE AMPLIFIER increases the amplitude of 1-pps pulses from +12 v to +28 v and also decreases rise and fall times. See Fig. 1. This circuit should also work well up to 50 meg pps with component value adjustments.

Q_1 is initially held off due to the saturation of the previous stage. R_6 provides a leakage path to ground for I_{cbo} and prevents turn-on (in the absence of a pulse input) of Q_1 even at elevated temperatures. R_1 is a current-limiting resistor and C_1 is selected to minimize storage (t_s) and fall (t_f) times. A positive-going pulse impressed at the base of Q_1 turns Q_1 on and the collector of Q_1 drops from +35 v to approximately zero. This negative-going pulse is applied to the base of the pnp transistor Q_2. Q_2, which is initially held off due to the +35 v on its base, now turns on and the output at its collector (point A) is again inverted to a positive-going pulse. R_2 and R_3 are selected to give the required base drive to turn on Q_2 with a signal applied at the input.

Rise and fall times, at the output, are lowered considerably because of the speed-up capacitor C_1 and the complementary scheme of Q_1 and Q_2. Q_1, due to the presence of C_1, provides an overdriven (spiked) pulse at the trailing

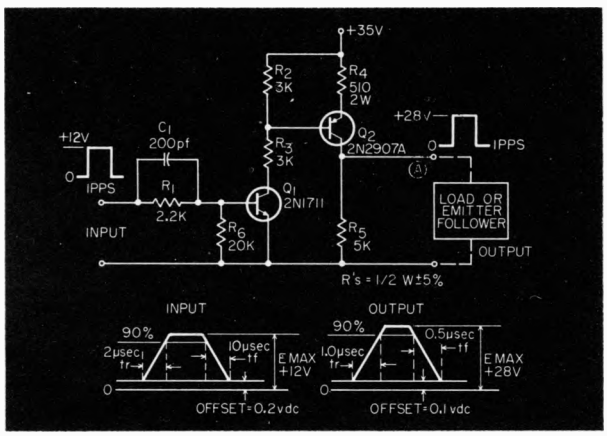


Fig. 1. Single power supply pulse amplifier.

Fig. 2. Input and output waveforms.

edge of its output. This pulse (at the base of Q_2) turns off Q_2 harder and provides a sink for the stored charge in the base of Q_2. Thus, the output pulse's trailing edge (fall time) is approved.

A 5-K potentiometer may be substituted for R_5 to give an adjustable pulse output from 0 to +28 v. An emitter-follower can be added at point A if a low impedance drive is required.

Operational Amplifier Gain Control from Zero to Infinity

THE USE OF OPERATIONAL AMPLIFIERS in analog computers, servo amplifiers, or any other electronic systems requires a practical adjustable gain control.

Two general methods of gain control for the operational

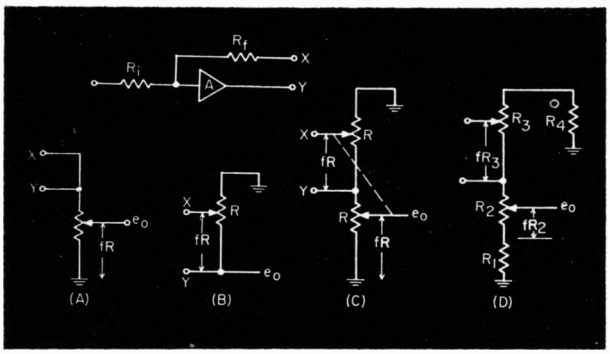


Fig. 1. Four methods of gain control. Method shown in 1d is most practical method for control from zero to infinity.

amplifier circuit are in common use. In the first method, Fig. 1a, the voltage gain is:

$$\frac{e_o}{e_i} = f\frac{R_f}{R_i}$$

where f is the fractional resistance of potentiometer R.

The gain of this circuit varies from zero to R_f/R_i.

The second method is used when more gain is desired. For Fig. 1b the gain is:

$$\frac{e_o}{e_i} = \left(\frac{1}{1-f}\right)\frac{R_f}{R_i}$$

The minimum gain of this circuit is unity times the ratio of R_f to R_i. The maximum theoretical gain is infinity; the maximum practical gain, obviously, is less.

Each of these two circuits has its uses and limitations.

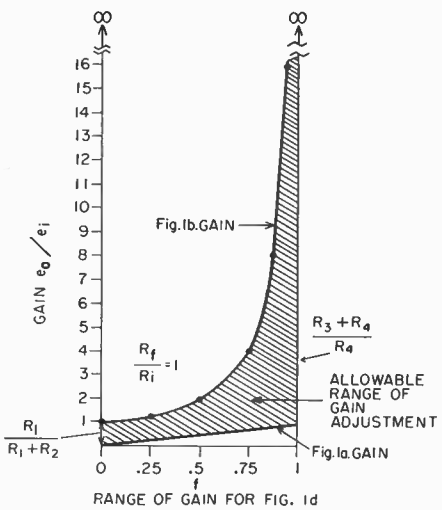


Fig. 2. Range of gain for control circuit of Fig. 1d.

A more useful circuit combines the above two circuits with a dual potentiometer.

Here,

$$\frac{e_o}{e_i} = \left(\frac{f}{1-f}\right)\frac{R_f}{R_i}$$

The gain moves from zero to infinity. A still more general approach is shown in Fig. 1d, where

$$\frac{e_o}{e_i} = \left[\frac{R_3+R_4}{(1-f)\,R_3+R_4}\right]\left[\frac{f\,R_2+R_1}{R_1+R_2}\right]\frac{R_f}{R_i}$$

To rapidly calculate the beginning and ending points for a desired gain characteristic use the following:

For $f = 0$

$$\frac{e_o}{e_i} = \left(\frac{R_1}{R_1+R_2}\right)\frac{R_f}{R_i}$$

For $f = 1$

$$\frac{e_o}{e_i} = \left(\frac{R_3+R_4}{R_4}\right)\frac{R_f}{R_i}$$

Or:

$$0 \leqslant \frac{R_1}{R_1+R_2} \leqslant 1 \leqslant \frac{R_3+R_4}{R_4} \leqslant \infty$$

The gain must start less than unity and terminates between unity and infinity. Obviously, infinite gain is impractical. The maximum gain achievable is dependent on the characteristics of the operational amplifier.

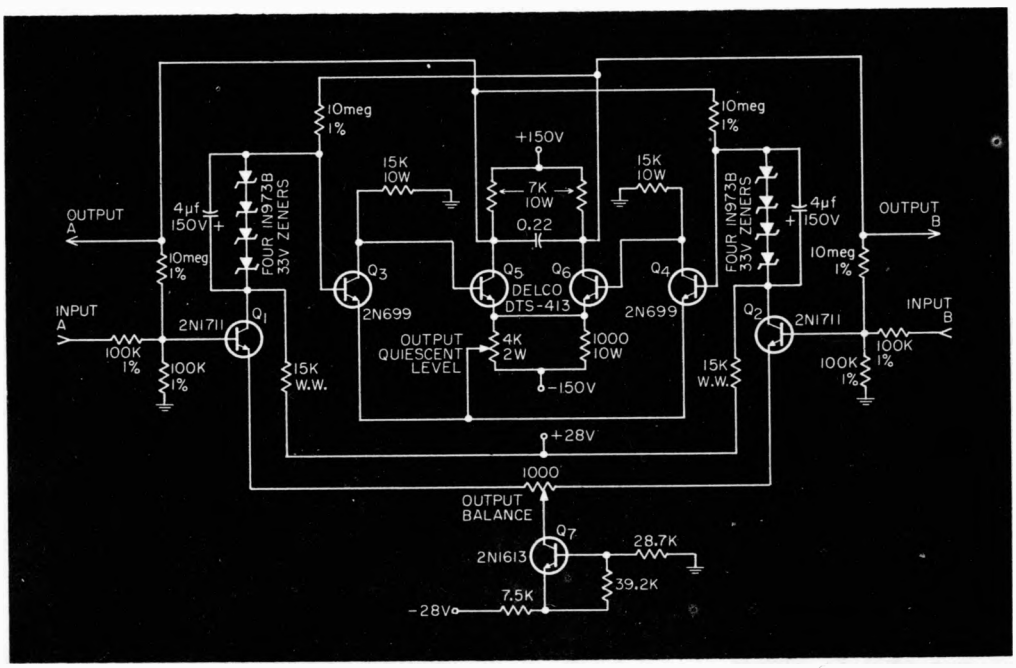
400-Volt Output Transistor Amplifier

HERE IS A differential voltage amplifier capable of swinging more than 400 V line-to-line. A gain of 100X can easily be obtained and the output quiescent level is at O V to ground. The operating voltages can be obtained from tube-type supply busses, with the drain from the 150-V supplies about 60 mA.

The power transistors can be purchased for less than $10 total. While the circuit was constructed of on-hand components and transistors, certain obvious substitutions can be made such as pnp's for Q_5 and Q_6. The power transistors are mounted on IERC #UP2-TOV-7 separate heat sinks.

The input and driver stages employ small back-to-back type heat sinks. The zeners can be mounted side by side, in a row, with silicone grease impressed between them for thermal linking. A 0.01-μF disc capacitor can be connected across the Q_5, Q_6 bases for reduced noise and increased feedback stability. In layout, sufficient insulation resistance should be maintained between the high-level output and the feedback junction points.

The circuit was constructed for use as a low frequency oscilloscope amplifier for a special application. No attempt was made to optimize this circuit beyond the requirements of 400 V peak swing, drift less than ± 1 V over normal room temperature range a 5-kHz bandwidth and a peak noise level of 3 V. The amplifier is quite forgiving for a shorted output, supply voltages applied in any sequence, or burnout from overdrive.



Direct-coupled differential amplifier provides 400-V output swing.

Photocell Threshold Circuit

THIS VARIABLE-threshold photocell amplifier draws negligible current in the quiescent state. When the incident light reaches the predetermined threshold level, the circuit switches rapidly from 12-V to zero output. These output voltages are standard logic levels. The low current-drain allows battery operation of the circuit.

The original application for this circuit was to detect day or nighttime conditions, and thus select the best operating frequency for a transmitter.

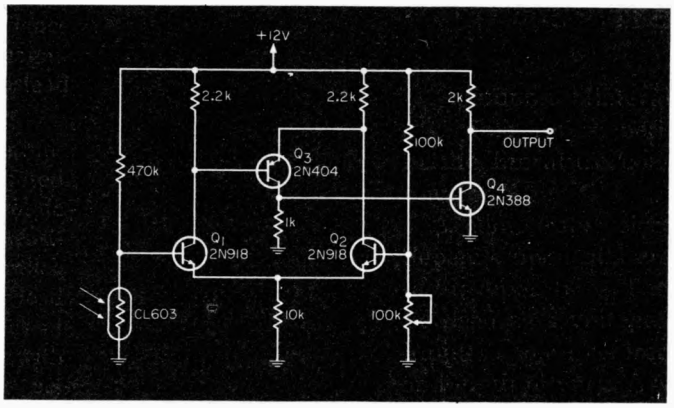
The threshold level had to be variable to compensate for photocell variations and also to allow the frequency change-over point to be advanced or retarded.

The circuit works with any resistive detecting device such as a thermistor or humidity sensor, as well as with the photocell shown here. Other resistance values can be accommodated by changing the 470-kΩ resistor in series with the detector.

Transistors Q_1 and Q_2 form a differential amplifier, with the reference voltage at the base of Q_2 set by the voltage-divider adjustment. As Q_2 is normally on and Q_1 is off, the base-emitter junction of Q_3 is back-biased. When the light input causes the photocell resistance to increase, Q_1 turns on and Q_2 turns off. Thus Q_3 is forward-biased and current flows into the base of Q_4 to saturate that stage.

The collector of Q_4 switches rapidly from +12 V to zero, giving an output compatible with standard logic.

Note that all transistors, except Q_2, are off in the quiescent state, thereby lowering the power drain.



Light-activated switching circuit uses a resistive photocell.

Low-Noise Preamplifier

Uses FET

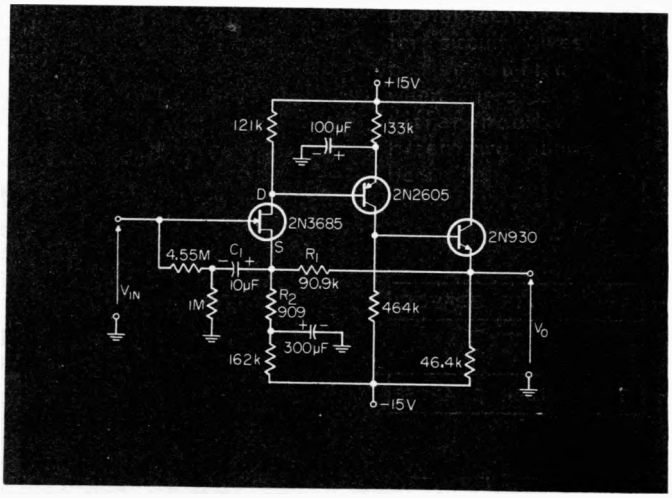
IF THE SOURCE impedance is high, a FET gives less noise than a bipolar transistor, even at frequencies as low as 10 Hz. Thus, for an amplifier to be used with a high-impedance transducer, a FET provides the best input circuit.

The preamplifier shown here, was designed for use with a 330 pF hydrophone over the frequency range 10 Hz to 10 kHz.

Positive feedback through C_1 reduces the shunting effect of the source impedance. The hydrophone has an impedance of approximately 48 MΩ at 10 Hz. The voltage gain of the FET stage is 20 dB. This stage gain reduces the effective noise contributed by subsequent transistors. Resistor R_1 provides 40-dB negative feedback, giving a closed loop gain of 40 dB for the complete preamplifier. This resistor also provides dc feedback which stabilizes the bias conditions over a wide range of operating temperature.

Measured voltage gain of this amplifier varies from 40.2 dB to 40.5 dB over the stated frequency range. Measured equivalent-input-noise voltage is −113 dBV at 10 Hz and −157 dBV at 10 kHz.

Voltage gain can be increased to 60 dB by reducing R_1 to 90.9 ohms, with little effect on noise. But this will reduce the 3-dB bandwidth. ■



Low-noise preamplifier for low-capacitance transducer.

Current sources improve amplifier slew rate

DIFFERENTIAL AMPLIFIERS SUFFER from slew-rate slow down when driving capacitive loads. This effect is due to the RC-time of their collector networks. By replacing the resistive collector network with a constant current source, a substantial improvement in slew rate is realized. Fig. 1 illustrates a typical improvement. The circuit illustrated in Fig. 2 demonstrates the use of a npn constant-current network in a typical deflection amplifier.

From Fig. 2, we see that

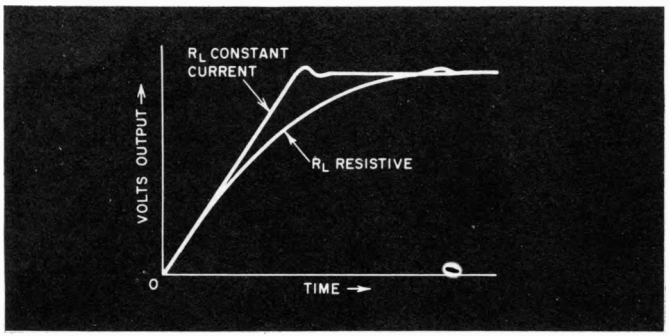


Fig. 1. This graph shows the transient response of the differential amplifier with and without the constant-current load.

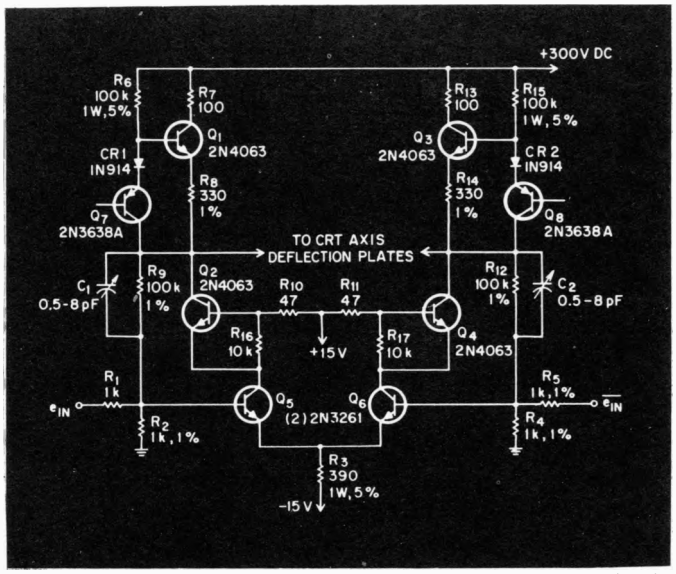


Fig. 2. This is the circuit of a high-voltage deflection circuit with current sources as output collector loads.

the circuit is a symmetrical differential amplifier, Q_1 and Q_3 are identical current sources. The network forming Q_1's current source is Q_1, CR_1, Q_7, R_6 and R_8. Transistor Q_7 is used as a 6.2 V zener diode. This equivalent zener has an extremely low impedance and will maintain 6.2 V with only a few μA of current. CR_1 compensates for V_{BE} drifts of Q_1, therefore, the voltage drop across R_8 is essentially 6.2 V. R_6 supplies the current for Q_7 and base drive for Q_1.

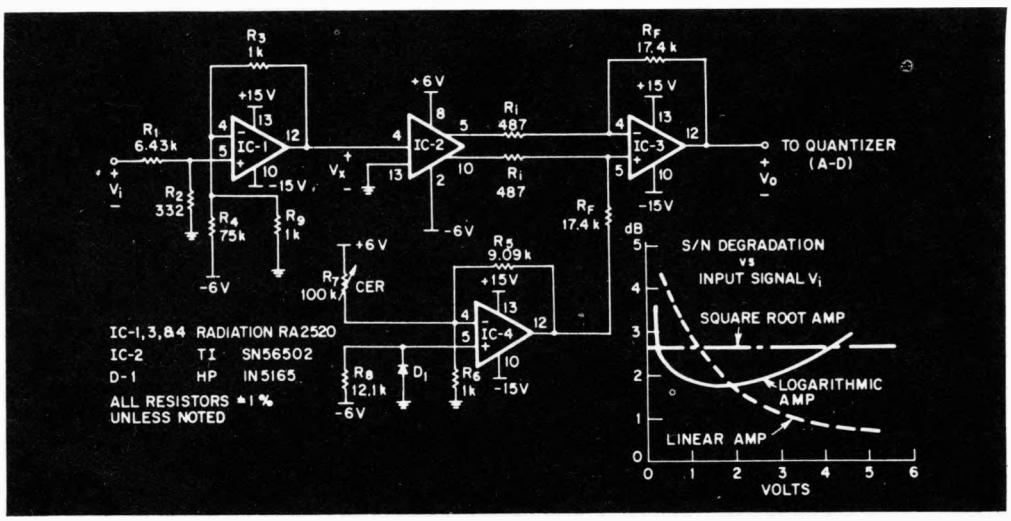
Under large output conditions the current variation through R_6 is maximum, since the entire signal appears across R_6. However, Q_7 maintains a 6.2-V constant drop due to its low dynamic impedance. Since this voltage appears across R_8, the current through R_8 is a constant. The only dynamic current variation under large-signal conditions is the current through R_6. The output impedance into the collector of Q_2 is close to 100 k. ■

Non-linear function amplifier

PROCESSING VIDEO signals with a linear quantization method is inefficient because too many levels exist for small signals and too few exist for large signals. In order to achieve economy in the use of quantized bits without changing the quantam level, it is necessary to pass the noise and signal through a non-linear function amplifier to make the rms voltage constant. The circuit shown improves system efficiency for signals of greatest occuring frequency.

This circuit uses a monolithic log amplifier in order to get the desired compression before a 6-bit A-D conversion. V_i is attenuated by −20 dB and level shifted by IC_1. Log amplifier IC_2 compresses the attenuated signal V_x. The output of IC_2 is amplified by IC_3 to a voltage range equivalent to V_i. IC_4 acts as a temperature compensator and output level shifter. Small output offsets may be nulled with R_7. The output transfer function is; Vo = 2.5 Log_{10} (V_i + 1). Temperature stability is within 1% for a −10 to 100°C range.

The transfer curve's shape may easily be altered by changing either the function's scale factor or constant. Adjusting the closed-loop gain of IC_1 varies the curve's order while adjusting IC_3's gain varies the scale factor. ■



This non-linear amplifier, made with IC op amps, synthesizes Vo = 2.5 Log_{10} (V_i + 1).

Higher speed, gain, output from IC diff amp

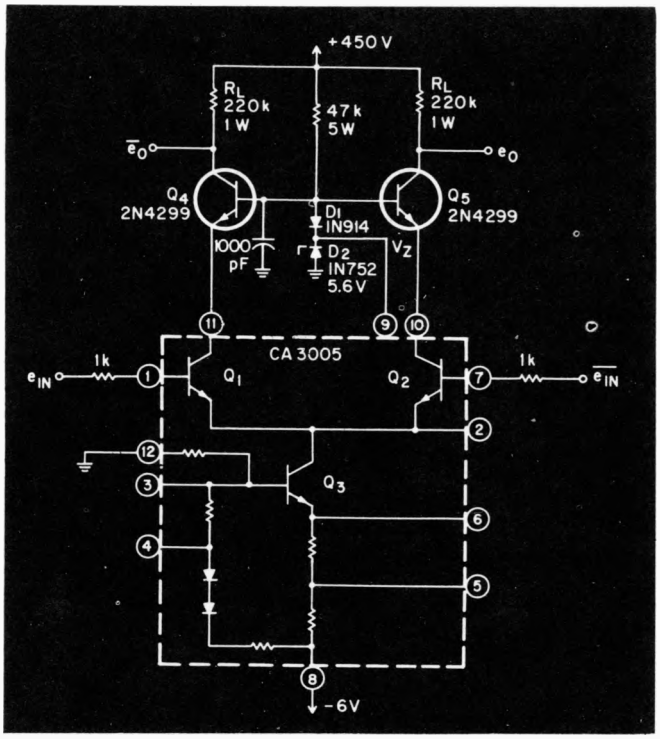
MONOLITHIC differential amplifiers are extremely attractive for dc and wideband amplifiers but the low operating-voltage requirements limit their applications to only low-level circuitry. With a hybrid combination of discrete components and an IC diff amp, we can greatly improve performance. The figure shows how we can minimize the number of external components while yielding a substantial increase in circuit capability.

The speed of the CA-3005 is limited by the collector-to-base capacitance of Q_1 and Q_2. By limiting the apparent dynamic voltage swing across this capacitance, we can reduce the degenerative ac feedback and boost speed. The dynamic levels of the IC collectors are clamped to the zener voltage so the maximum dynamic voltage swing appearing across the collector-to-base junction is e_{in}.

The gain of Q_1 and Q_2 is a function of collector supply voltage. By maintaining this voltage at V_Z, we avoid dynamic gain variations with varied input levels.

Transistors Q_4 and Q_5 operate in a common-base configuration since their emitters see a high-impedance drive. A common-base configuration can be viewed as delivering the greatest possible speed for a given transistor type, so Q_4 and Q_5 are extremely fast. The common-base configuration also allows operation from a high supply voltage since BV_{CEO} is no longer the significant breakdown parameter. Instead, BV_{CBO} now becomes the limit. For the 2N4299, BV_{CEO} is 400 Vdc, but BV_{CBO} is 500 V.

By allowing a greater voltage swing across the active device, we realize increased gain. Gain for the diff amp is directly proportional to R_L/R_e, where R_e is the intrinsic resistance of Q_1 and Q_2. Since we can now increase R_L, we boost circuit gain proportionally. ■



By operating discrete transistors in a common-base configuration we can boost an IC diff amp's gain, speed and output voltage.

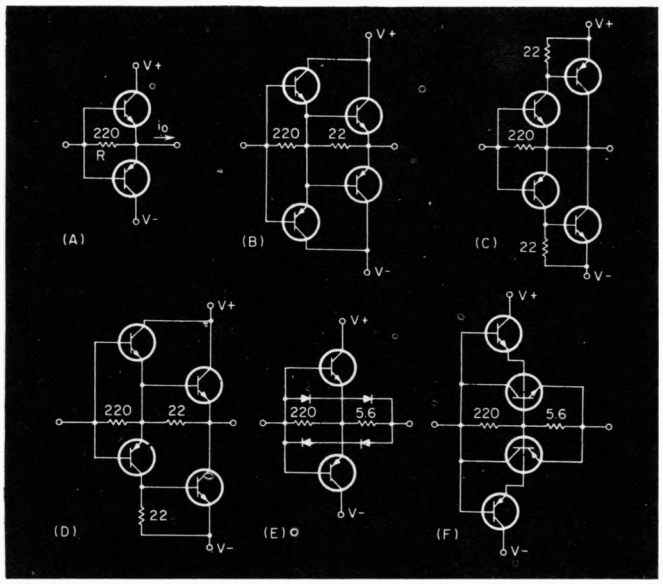
Current boosters for IC op amps

ASIDE FROM the matter of cost, there's an important functional limitation to increasing the current output from IC op amps: thermal feedback to the input circuitry causes voltage offsets. The best way to overcome the problem is to use a physically separate current booster.

The figure shows (A) a 100-mA booster with zero quiescent current. It uses the full output current of a preceding op amp (typically 5 or 10 mA). If the output current level is less than V_{BE}/R_e, the entire output current is supplied by the amplifier itself. Currents above V_{BE}/R_e are supplied by the complementary emitter followers.

We can extend the output to the 1-A range by cascading a similar booster (B in the figures), by adding complementary transistors (C) or by combining both (D). And if we want to limit short-circuit currents, we can use the popular circuits (E,F).

Diode types are not critical and the transistors are chosen to satisfy power and bandwidth requirements. ■



Various schemes for boosting current from IC op amps to 100 mA (A) and to 1 A (B,C,D) and for limiting short-circuit current (E,F).

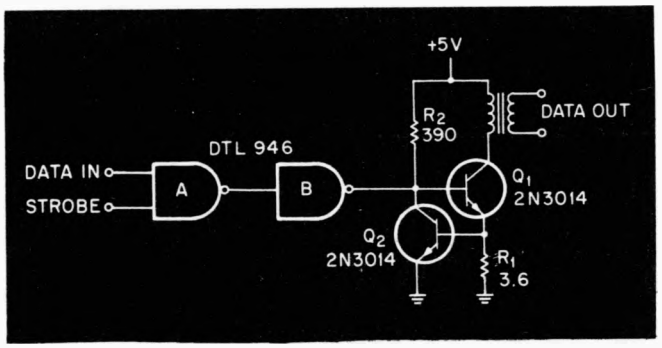
Isolated line driver with short protection

WHEN IT'S NECESSARY to transmit digital data over a transmission line while maintaining isolated signal returns at opposite ends of line, the driver circuit shown can be used to advantage. The circuit, compatible with TTL and DTL logic, is powered by a +5-V supply, and has short-circuit protection.

The pulse transformer is driven by transistor Q_1 whose base drive is provided by resistor R_2 when gate B is cut off. Current limiting is provided by the combination Q_2 and R_1. This current limiting protects Q_1 from high collector currents caused either by an inadvertent short across the transformer secondary winding or transformer saturation.

When the voltage drop across R_1 reaches approximately 0.7 V, transistor Q_2 begins to turn on, thus limiting the base drive to Q_1 and consequently limiting its collector current. With the value of R_1 as shown, the current is limited to 200 mA.

The circuit was used to transmit data with a pulse width of 300 ns over a 75-ohm transmission line at a rate of 600 kHz. A much higher frequency could be used, but the duty cycle must be kept small enough so the power dissipation of Q_1 is not excessive with the output shorted. ■



This line-driver circuit offers simplicity with current limiting and signal-return isolation. Any DTL or TTL NAND gates can be used at the input.

Gain-programmable amplifier

THE CIRCUIT in Fig. 1 enables the gain of a non-inverting op amp to be changed externally. The control device is a FET, which shorts feedback resistor R_3 to ground. Additional gain variation could be obtained by dividing R_3 into smaller increments and shunting each segment to ground with its own control FET. With the "digital input" at zero volts, Q_1 turns on but is held out of saturation by Schottky diode D_2. Q_1 then injects current into the gate of Q_2 through the reverse capacitance of D_3. Q_2 turns on, making its drain-to-source resistance about 10 ohms. This value is negligible compared to feedback resistors R_1 and R_2. The resulting op-amp gain is Eo/Ei = $(R_1+R_2)/R_2$. If R_2 is 1.13 kΩ and R_1 is 10 kΩ, the resulting gain is 10.

When the "digital input" is 5 volts, Q_1 is off and the gate of Q_2 is driven to −15 V. This negative gate bias causes the drain-to-source impedance of Q_2 to approach an open circuit. Now the gain becomes Eo/Ei = $(R_1+R_2+R_3)/(R_2+R_3)$. If R_1 and R_2 are still at 10 kΩ and 1.13 kΩ, respectively, and if R_3 is 8.87 kΩ, the resulting gain is 2. Fig. 2 shows the variation of the analog output as a function of the digital control signal. ■

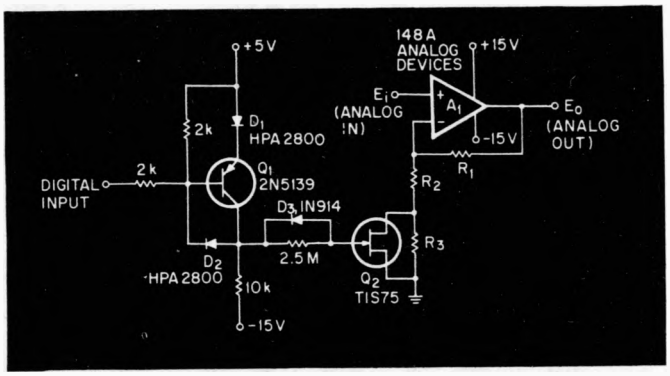


Fig. 1. This circuit's gain is programmable with standard logic levels.

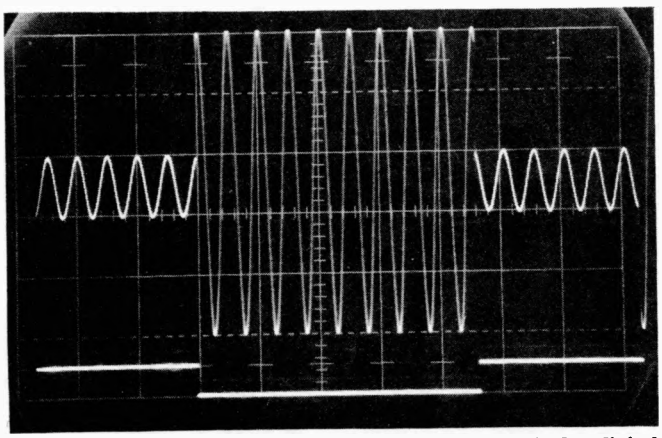


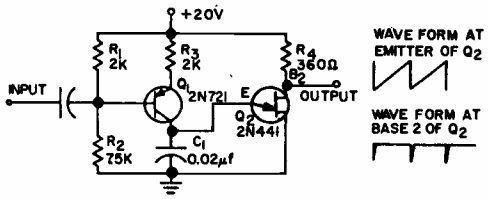
Fig. 2. Output voltage variation as a function of the digital control signal. Analog output voltage scale is 1 V/cm and the digital input voltage scale is 10 V/cm. The time scale is 200 μs/cm.

Section 8
OSCILLATOR CIRCUITS

Voltage Controlled Oscillator

HERE IS A SIMPLE voltage-controlled oscillator that basically consists of a variable current source (Q_1 and its bias circuit), a capacitor and a voltage-controlled switch (unijunction transistor Q_2). The output signal can be used to trigger a bistable flip-flop.

With no input signal, Q_1 acts as a constant-current source whose current is determined by R_1, R_2 and R_3. Q_1 will charge C_1 linearly and Q_2 fires when the voltage across C_1 reaches Q_2's emitter peak-point voltage. The unijunction transistor then discharges C_1, causing a negative spike at B_2. With the component values shown, the oscillator center frequency was 8 kc. The period is determined by the equation,



The output frequency is determined by the time needed for constant-current source Q_1 to charge C_1 to the peak-point voltage of UJT Q_2.

$$T = \frac{V_p C_1}{i}$$

where:

V_p = UJT emitter peak-point voltage
C_1 = capacitor value
i = current thru Q_1
T = period between pulses

When an input signal is applied to the base of Q_1 the current flowing through Q_1 is varied, thus varying the time required to charge C_1 up to Q_2's emitter peak-point voltage. Due to the phase inversion in Q_1, the output frequency is 180 degrees out of phase with the input voltage.

The circuit was temperature tested using a polystyrene capacitor for C_1. The frequency varied 3 percent between $-50°F$ and $+150°F$. Most of this variation occurred at the low temperatures, so that it is reasonable to speculate that the frequency could be held to ± 0.3 percent by placing the circuit in a temperature-controlled oven.

Wide Range Variable Multivibrator

THE HYBIRD astable and monostable multivibrators described in the literature have shown good stability and an improved range of continuous frequency variation over the conventional circuit configurations. (The hybrid circuits have exhibited a range of frequency change of up to 30:1.) This has been achieved at the price of adding another active semiconductor device, usually a unijunction transistor. The circuit of Fig. 1 reverts to the more conventional astable form, and is a

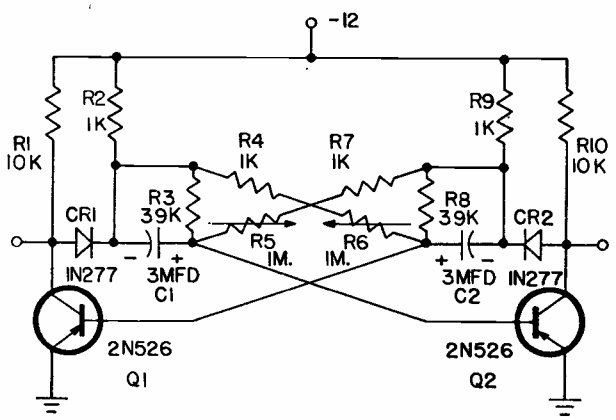


Fig. 1. Modified astable multivibrator.

variation of a circuit described earlier.[1] The modified astable shown has a frequency change ratio of 120:1 at

50 percent duty cycle, with symmetry variable by ±97.5 percent. The frequency range for the values shown is from 5 msec to 600 msec (t_1+t_2).

Among the many applications for a circuit with this capability is as a pattern source for generating keyed dc or keyed tone signals for testing digital communications and data processing equipment. For example, a four bit digital word has sixteen possible values; eight of these values can be programmed using this circuit. Six standard seven unit teletype characters can be generated, making the circuit an inexpensive baud

(Continued on page 40)

[1]Mattox, William J., "High Square, Variable Frequency Multivibrator", *Electronic Equipment Engineering*, July, 1961.

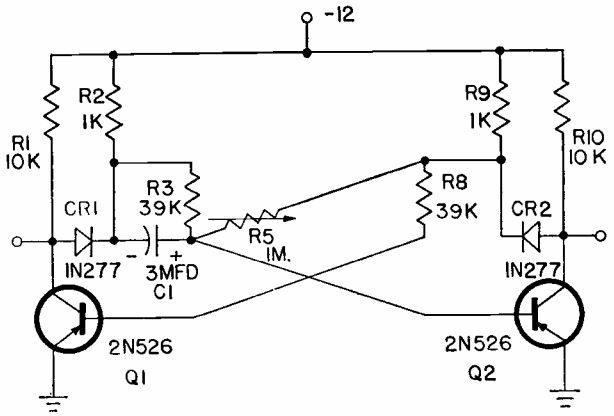


Fig. 2. Converted circuit of Fig. 1 to monostable multivibrator operation.

generator for testing communication circuits. With the symmetry and frequency range available, digital words up to 40 bits in length may be simulated. This is not to imply that all combinations are possible, but by proper adjustment of the timing, certain discreet values can be programmed.

The circuit of Fig. 1 operates in the conventional astable manner, with R1 and R2, and R9 and R10 forming the collector loads for Q1 and Q2. R3 and R8 are the base drive limiting resistors, while diodes CR1 and CR2 isolate the output terminals from the charging circuits for C1 and C2, thus providing an extremely square output waveform. Note that for all practical purposes the base drive and timing circuits are independent, an advantage not found when attempting to vary the frequency of a standard astable circuit. To prevent a ramp from appearing at the leading edge of the positive going waveform, R2 should equal R4, and R7 should equal R9. Also R3>>R2 and R8>>R9.

For digital or other type systems where the basic circuitry is repeated many times, the circuit of Fig. 1 can be converted to a monostable multivibrator by the omission of R4, R6, R7, and C2. No other changes are necessary, and with a suitable trigger a one-shot is available. This is shown schematically in Fig. 2. For the values given in Fig. 2, the output pulse width at the collector of Q2 can be varied from 0.25 msec to 300 msec, a ratio of 1200:1. This rather wide range should make the circuit attractive for a variety of uses. A waveform with good squareness can also be obtained from the collector of Q1 through the isolating action of CR1 as explained above.

Stable Oscillator Circuit

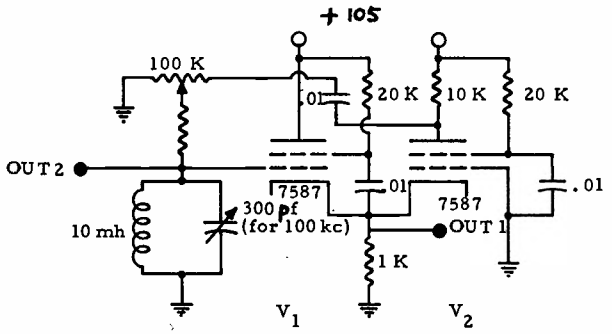
THIS CIRCUIT achieves excellent frequency and amplitude stability; accomplished by eliminating all grid current in the tank circuit, and by isolating the tank from the driving tube by the use of resistive degeneration.

Unlike most oscillators which limit by forcing the grid positive, drawing current into the tank coil, this circuit limits by forcing the grid of V_1 negative; therefore greatly reducing the g_m of the tube. Thus, no dc ever flows in the tank coil.

Tube V_1 is a tetrode cathode follower with the screen driven by the cathode, thus its input impedance as seen by the tank is very high, and changes of tube parameter will affect the resonance only slightly.

The driver circuit, V_2, is cathode driven with a grounded grid. This both maintains the cathode voltage, allowing the negative swing limited by V_1, and preserves the zero phase shift which is a characteristic of this circuit. The plate of V_2 is coupled to a potentiometer which regulates the positive feedback necessary for oscillations. Use of "Nuvistor" tetrodes makes this circuit economical on power, and reduces temperature drift.

For nonsinusoidal low impedance output, couple to the cathode resistor. If a very pure sine wave is de-desired, couple with a high impedance load to the grid of V_1. Be careful that this circuit is an equivalent constant resistance, as either reactive or variable loads will reduce stability, By proper compromise in the feedback pot setting, both excellent stability and near constant amplitude over a wide tuning range may be achieved.



Resistive degeneration allows isolation of the tank circuit from the driving tube while eliminating all grid current from the tank.

Low-Frequency C-Coupled Oscillator

THE SIMPLE and inexpensive oscillator in Fig. 1 is designed for frequencies from 5 cps to 300 kc but its advantages are more obvious at low frequencies. The frequency is quite stable over a wide range of temperature and dc-voltage changes.

Conventional configurations like the Clapp or Hartley require dual inductors or capacitors and, even with

tank circuits, another capacitor is required for coupling to the next stage. For low frequencies, these extra components are large and costly. For operation over wide frequency ranges, ac coupling introduces additional problems because loop gains decrease with frequency.

The oscillator in Fig. 1 overcomes these problems by using the tank not only to control frequency but

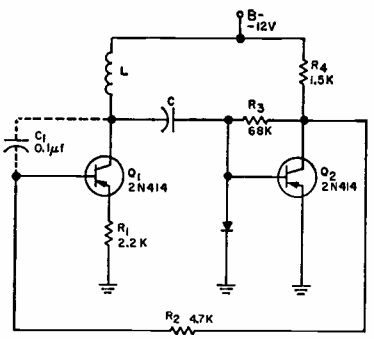


FIG. 1

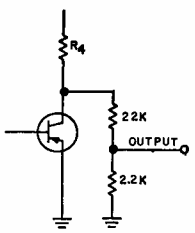


FIG. 2

Fig. 1. A stable low-frequency oscillator.

Fig. 2. A coupling circuit useful for driving varying loads.

also to couple the signal to the next stage. The diode at the base of Q_2 provides an ac ground from the tank capacitor for positive voltage swings, while Q_2's base emitter junction provides the ac ground for negative swings. There is a small discontinuity in the ac-grounding circuit when V_{be} of Q_2 is with 0.1 v for a germanium transistor and diode and within 0.6 v for silicons.

The resulting waveshape discontinuity at the collector of Q_1 can be smoothed by C_1. This capacitor produces degenerative feedback which will reduce all high-frequency changes at the collector. It will also limit the maximum frequency of operation.

Tests showed that with $L = 2$ hy and $C = 28$ μf, the circuit could oscillate below 4.6 cps. Dc biasing of the capacitor allowed the use of electrolytics. At frequencies around 100 cps, frequency stability with respect to supply-voltage changes of 20 percent was within 0.1 percent. Drift was 0.2 percent from 25 to 100 C.

Loading the circuit with a 22 K resistor from collector to ground lowered the frequency by 0.5 percent. The coupling circuit in Fig 2 can be used to eliminate this frequency change when the oscillator is used to drive a Schmitt trigger or other varying load.

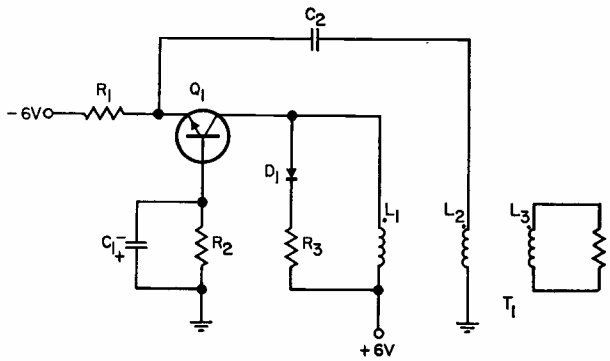
R_1 can be reduced if greater loop gain is required for low h_{fe} transistors and R_2 can be replaced by a crystal for tighter frequency control.

Even Duty Cycle Blocking Oscillator

THE DESIGN of a free-running blocking oscillator may prove to be a problem when the duty cycle is 50/50. This problem may be alleviated by the insertion of capacitor, C_1, across resistor R_2, as shown in the figure. The R_2C_1 time constant is adjusted so that $t = 10\ RC$, where $t = 1/2f_o$, and f_o is the frequency in question. The circuit was designed for operation at 400kc.

Since the on time is essentially controlled by the magnetizing inductance determined by values of L_2C_2, and the off time by time constant R_1C_2, R_1 must be made excessively small to insure that C_2 can discharge in a short period of time to a point where transistor Q_1 turns on. After Q_1 switches on C_1 is charged as shown. Thus, C_2, is required to discharge to a point where the base-to-emitter voltage V_{BE}, becomes positive instead of ground potential. The circuit then generates another pulse.

$R_1 = 300$	$R_4 = 1.0$ K	$Q_1 = 2N708$
$R_2 = 2.0$ K	$C_1 = 62$ pf	$D_1 = FD\ 126$
$R_3 = 470$	$C_2 = .01$μfd	$T_1 =$ AE 441-3 (MCI)



Blocking oscillator provides even duty cycle.

A Synchronized Oscillator Circuit

A SYNCHRONIZED OSCILLATOR circuit was required for a timing operation with a variable synchronized signal whose nominal frequency is in the order of 1/170 of the oscillator frequency. No integral relationship existed between synchronizing signal and oscillator signal frequencies. The best available scheme was synchronization of an oscillator by interrupting a current of known magnitude and direction in a coil (usually an element of the oscillator). However, delays existed in this scheme between the end of the synchronized interval and the start of oscillations of the order of 0.3 microseconds which was unsatisfactory.

Thus, a synchronized oscillator was devised using an astable multivibrator as the basic electronic circuit. The frequency stability could be made 1 part in 4000 using temperature stable elements (film resistors, etc.). This oscillator is shown in Fig. 1. Transistors Q_1 and Q_2 constitute a conventional astable oscillator pair. Diodes CR_1 and CR_2 prevent the large negative potential that appears between base and emitter of Q_1 and Q_2 from breaking down the base-emitter junction of these transistors.

The synchronizing pulse is applied to the cathode of diode CR_3, thus cutting Q_2 off and forcing Q_1 to saturate in the normal astable manner. When the synchronizing pulse passes, oscillations begin with Q_2

saturating first. The oscillations happen as a result of a slight positive spike created by the stray capacity across CR_3 which causes Q_2 to conduct. A capacitor of 20 micro-micro farads placed across CR_3 assures that this transition occurs with negligible delay from

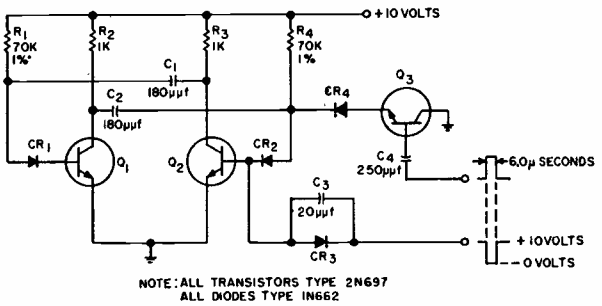


Fig. 1—Synchronized oscillator.

the termination of the synchronizing signal.

One situation which occurs and must be remedied is described here. If the synchronizing signal occurs at a time when Q_2 is cut off, as a result of the natural oscillation mode, then the synchronizing signal will not disturb the natural oscillation until Q_2 tries to return to the saturated state. This might be as long as a half clock interval. A transistor switch was inserted which is closed by a positive signal occurring at the same instant as the synchronizing signal. If Q_2 is off, at the arrival of the synchronized signal C_1 is charging and has not yet reached its final state. Transistor switch Q_3 quickly discharges capacitor C_1 to the ground potential, thus assuring that during the synchronizing interval the oscillator will be forced into the condition where Q_2 is nonconducting and Q_1 is in the conducting mode. The pertinent waveshapes are shown in Fig. 2.

For this application the synchronized signal had a width of 6.0 micro-seconds. However, the circuit would operate properly with a minimum synchronized signal of 2.0 microseconds. The oscillator frequency was 68.4 kc and the synchronizing signal 400 cps.

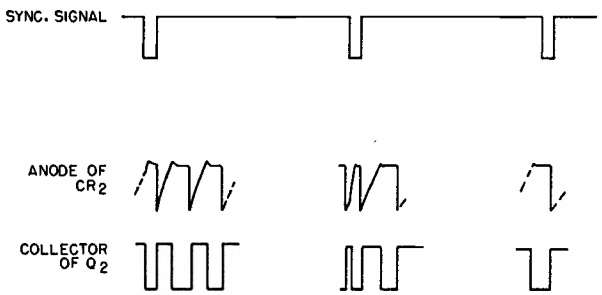


Fig. 2—Timing Waveforms

A 0.01 Microwatt Multivibrator

THE BASIC MULTIVIBRATOR consists of two amplifying devices which alternately conduct and cut-off as the multivibrator switches from one state to the other. Therefore one device is always conducting.

By making one device a pnp transistor and the other an npn transistor, both can be made to conduct at the same time for part of the cycle, and both can be made to cut-off the remainder of the cycle. If the conducting time is made very short compared to the non-conducting time, the average power used is very much less than when one is always conducting.

Such a multivibrator is shown in Fig. 1 and has a frequency of about 40 cps. It operates at 0.6 supply voltage at a current of about 0.015 μa, and has a total power consumption of 0.009 μw.

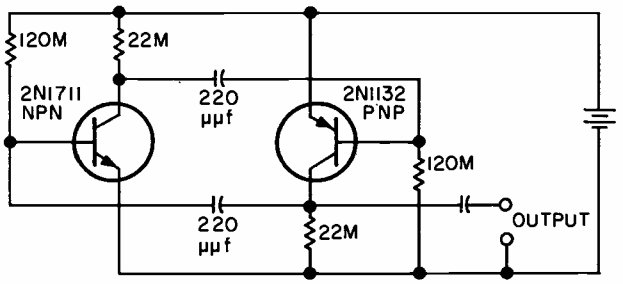


Fig. 1 Multivibrator having extremely low power consumption.

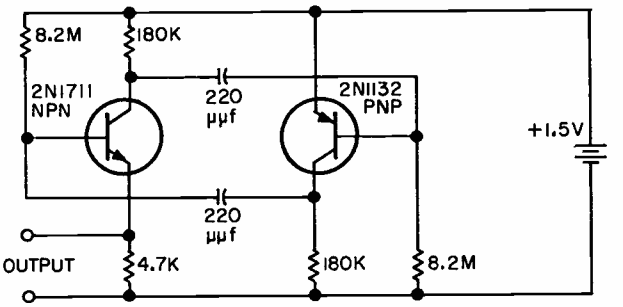


Fig. 2 Multivibrator with low output impedance.

As the frequency is increased, more power is required. For comparison, a higher frequency circuit, Fig. 2, is shown. This circuit oscillates at 840 cps and draws 1.6 μa. It differs from Fig. 1 in that a resistor is added in the emitter circuit of the 2N1711 transistor. A triangular pulse, about 10 μsec wide at the base, appears across this resistor. The pulse is surprisingly large, about 0.4 v, and because of the low impedance of the circuit, is useful in driving additional circuits.

Complementary symmetry allows flexibility in the polarity of the output pulses. This is because the output can be across either, or both, collector resistors, or across a resistor in either, or both, emitter circuits. Frequency can be controlled by varying the capacitance, the base resistance, or the base-bias. For example, a temperature-to-frequency conversion can be made by simply replacing one base resistor with a very high resistance theirmister. (The circuit will not operate unless the base resistances are very high). Alternate transistors which have been used are 2N338 or 2N697 for the npn and 2N495 for the pnp.

Wide—Range, Voltage-Controlled Oscillator

THIS TRANSISTORIZED BUTLER OSCILLATOR was designed to provide a 70 per cent frequency deviation. Placement of a series-tuned circuit in the feedback path between emitters of Q_1 and Q_2 makes the frequency relatively independent of transistor parameters. L_1, which is adjusted for a loop gain just sufficient for sinusoidal oscillation, also provides shunt peaking to stabilize the output amplitude over the range of control.

By adjusting L_2 the circuit shown was tuned to 2 Mc with a 1 v control. The frequency deviation from this point was minus 205 kc at 0 v to plus 1,289 kc at 20 v.

The frequency deviation is not linearly proportional to the control voltage in the lower half of the voltage range. Therefore, a requirement for linear deviation will necessitate a shaped control characteristic.

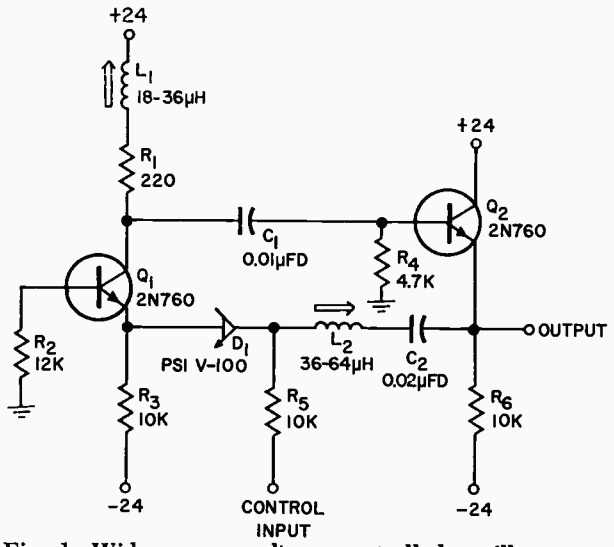
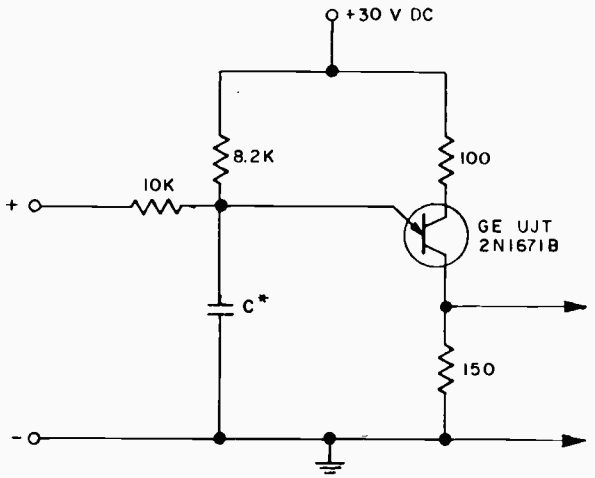


Fig. 1. Wide range, voltage controlled oscillator.

Voltage-Controlled Variable-Frequency Oscillator

THIS CIRCUIT WAS DESIGNED as a voltage-controlled variable-frequency oscillator. Without the 10 K resistor, the circuit is the well known unijunction transistor ujt oscillator. The voltage toward which the capacitor charges is controlled by the incoming dc voltage when the 10 K resistor is included. A low input voltage makes the capacitor charge towards a lower voltage, which means that it takes longer for the capacitor to charge up to the breakdown voltage of the ujt. This gives a slow pulse repetition frequency prf.

Conversely, a high input voltage allows the capacitor to charge towards a higher input voltage. Thus, the time it takes the capacitor voltage to reach the breakdown voltage of the ujt is reduced and the prf increases. It should be noted that this circuit is not meant for use where linearity is important.



Voltage controlled variable frequency oscillator.

Output, in pulses per second, for two values of C

C 0.68 μfd ±10%		C 0.2 μfd ±20%	
IN (vdc)	OUT (pps)	IN (vdc)	OUT (pps)
0	670	0	220
5	1700	5	530
10	2300	10	720
15	3000	15	870
20	3700	20	1100
25	4000	25	1230
30	4550	30	1400

Inductor Raises Useful Sawtooth Frequency

THE NOVELTY of this circuit consists of adding an inductor to cause ringing and thereby extend the operation of a sawtooth oscillator, notably a four-layer diode, to higher frequencies. The technique is also applicable to other, similar negative-resistance devices.

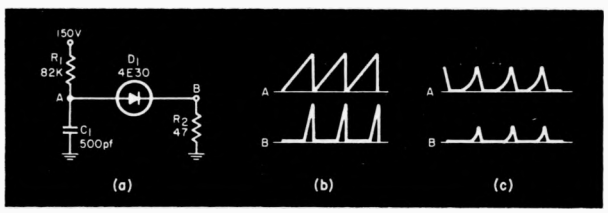


Fig. 1. Basic negative-resistance sawtooth oscillator with associated waveforms.

Consider the simple sawtooth oscillator in Fig. 1a, consisting of resistors R_1, R_2, capacitors C_1 and four-layer diode D_1. The waveforms for normal circuit operation are shown in Fig. 1b. For higher frequencies, the resistor R_1 is reduced or the voltage V_1 is increased. The waveforms, however, degenerate to those shown in Fig. 1c. The problem is that the capacitor charging current carried by the negative-resistance device is close to or above the valley current on the negative-resistance characteristic. Therefore

the diode tends to latch up in the conducting state. In one application, this caused a circuit not to operate satisfactorily above 10 kc for reasonable values of capacitance, about 500 pf.

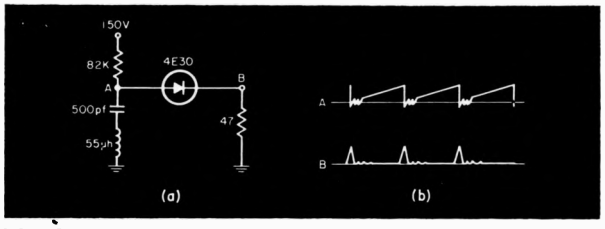


Fig. 2. Improved circuit with necessary ringing evident in sawtooth waveforms.

The solution is to add a choke coil in series with the capacitor C_1. Thus the capacitor discharge through the diode excites the *LC* circuit and the resulting rings cut off the four-layer diode. The modified circuit was thus capable of operating well above 100 kc with no tendency toward instability. The waveforms are shown in Fig. 2b. ◆◆

Transistor Mixer Crystal Oscillators

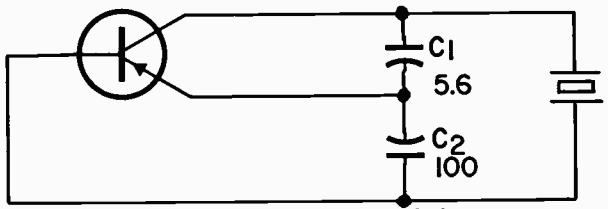


FIG. 1—Basic oscillator circuit—a Colpitts.

A CIRCUIT which will allow one transistor to do the work of two will not only save the price of a transistor but will generally effect a saving in space and other component parts. Three mixer crystal oscillator combinations based on this philosophy are shown in Figs. 2 to 4.

Oscillator-Mixer A (Fig. 2)

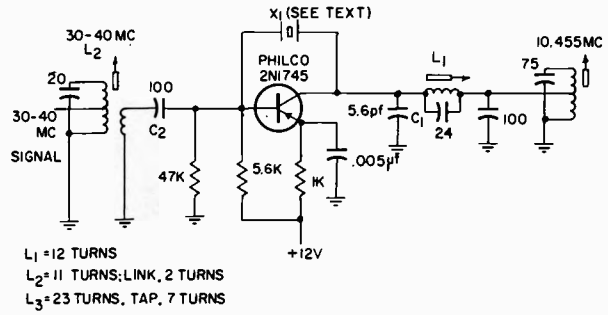


FIG. 2—Mixer-oscillator combination A.

Characteristics of this circuit are: Frequency—input 30-40 mc; output (i.f.), 10.455 mc; crystal, third overtone operating 10.455 mc lower than the signal frequency.

It will be observed that the oscillator configuration is the familiar Colpitts circuit, shown basically in Fig. 1. Capacitors C_1 and C_2 should be chosen carefully for correct operation. In parallel with C_1 and C_2 are the transistor capacitances—the collector-to-base and the base-to-emitter capacitances, respectively.

As a mixer, the transistor is operated in the grounded emitter configuration. Tuned circuit L_1, Fig. 2, has a low impedance to the i.f. frequency but a high impedance to the crystal frequency. L_1 and its associated capacitor should be tuned to the overtone crystal frequency.

The values of the various components have been compromised. They are not particularly critical within reasonable limits.

Oscillator-Mixer B (Fig. 3)

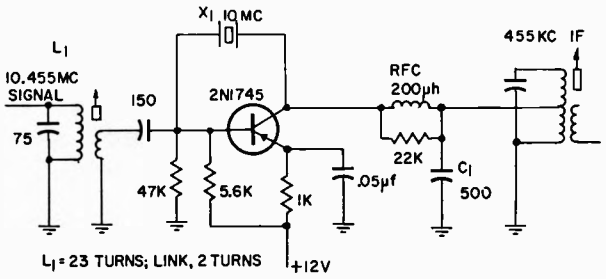


FIG. 3—Mixer-oscillator combination B.

Characteristics of this circuit are: Frequency—input 10.455 mc; output (i.f.) 455 kc; crystal frequency, 10 mc.

Although the transistor is a Philco type, others such as the TI S054A will give excellent performance at the frequencies concerned.

The 200 μh choke is used in lieu of a tuned circuit normally resonant at the crystal frequency. The oscillator is operated at the fundamental frequency of the crystal. The 22,000 ohm resistor is paralleled with the r.f. choke to damp out spurious oscillations which tend to occur at a frequency determined by the choke and associated capacitances.

Capacitor C_1 insures a low impedance for the signal to ground but is part of the i.f. tuned circuit at the i.f. frequency. As a mixer, the values of the various componentes are not overly critical.

Oscillator-Mixer C (Fig. 4)

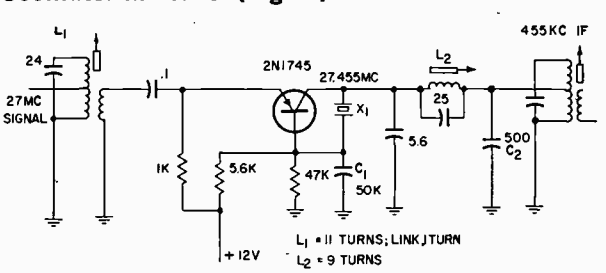


FIG. 4—Mixer-oscillator combination C.

Characteristics of this circuit are: Frequency—input 27 mc; output (i.f.) 455 kc; crystal frequency, 455 kc higher than the received frequency.

The transistor used is a Philco 2N1745, although others may give similar performance.

The tuned circuit in the collector lead is adjusted to the frequency of the crystal. As a mixer the transistor is operated grounded base. Ground-

ed base configuration has been found preferable to grounded emitter connection when the crystal frequency is near the signal frequency. The coupling between the link and L_1 should be adjusted so that the tuned circuit does not pull the crystal out of oscillation. The correct amount of coupling coincides with good selectivity requirements.

Components are somewhat more critical than those associated with the two oscillators previously described. The mixer is more critical of over-injection, and L_2 should be adjusted for maximum gain rather than for maximum oscillator output. Generally, L_2 is tuned slightly lower in frequency than the frequency of the crystal.

The 500 pf capacitor, C_2, creates a low impedance to ground for the oscillator but is absorbed in the i.f. tuned circuit at the i.f. frequency.

Feedback may be adjusted by varying the value of C_1. This capacitance is effectively in series with signal and should be as large as possible consistent with reliable oscillator operation.

RC Plate-Tuned Oscillator

A SPECIAL variety of the Wien-Bridge audio frequency oscillator as shown in Fig. 1 was constructed to generate a useful source of signal voltage by a one-stage instead of a two-stage regenerative amplifier. In addition, it makes a signal voltage available directly from an impedance matching transformer instead of a buffer amplifier for isolation purposes.

The oscillator tube is a triode-connected beam power 35A5; however, other power triodes can be operated satisfactorily. The Wien Bridge forms the plate load of the tube, and its reactive components determine the resonant frequency of operation as expressed by the relation: $F_o = 1/2\pi\sqrt{R_1C_1R_2C_2}$ cps.

One end of the matching transformer primary is connected to the midpoint of the bridge reactive components: the other end is connected to the grid leak of the tube. An intermediate tap on the primary is grounded. The cathode lead is tied either slightly above or below the grounded tap. The degree of amplifier gain and regenerative action is regulated by the position of the cathode in the feedback loop of the transformer. The grid-leak time constant should be equal or greater than ten times the period of oscillation, and is given by the following relation: $R_gC_g = 10\ T_o$ where $T_o = 1/F_o$. The signal output is obtained from the transformer secondary.

Consider that a steady current flows in the tube circuit. Assume a small momentary increase in plate current occurs due to some transient effect. The plate voltage will decrease. Since the voltages across the Wien-bridge capacitors cannot instantly follow the plate change, the midpoint of this RC network will drop below ground potential. Current from ground consequently flows through the transformer primary and induces a positive voltage on the grid. Accordingly, the original increase in plate current will continue until limited by the rise in grid-leak bias.

At this time, the bridge capacitors have been overcharged through the B supply, and this causes the midpoint of the RC network to go above ground potential. Current then flows to ground through the transformer primary, and induces a negative voltage which adds to the grid-leak bias, thereby tending to cut-off the plate current. As the cut-off point is reached, the induced negative voltage is lifted from the grid-leak. The amount of grid-leak bias only does not hold the tube at cut-off; hence, the plate current is allowed to increase. This cycle is repeated at a frequency given in the formula.

This oscillator can be operated as a self-modulated signal source. For example, when the primary of

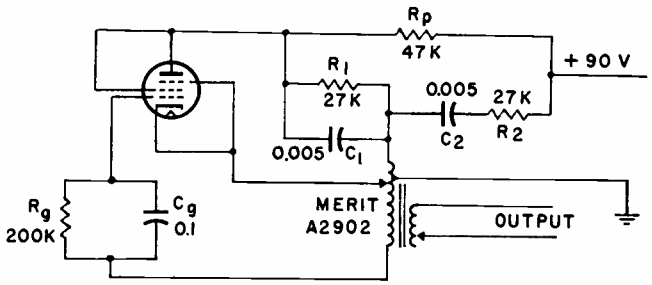


FIG. 1—Plate-tuned RC oscillator circuit for 1000 cps.

the matching transformer is connected in parallel with a capacitor, its resonant frequency will be modulated by the Wien-bridge selective frequency network.

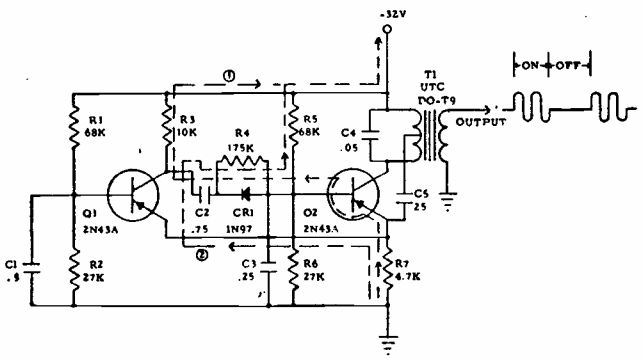
Using the values shown in Fig. 1 for R and C, the frequency is about 1000 cps. For higher frequencies, capacitors C_1 and C_2 could be of the dual-section type with common rotor drive for ease of frequency range control.

Pulsed Audio Oscillator

REPETITION rate, duty cycle, and frequency can be easily varied for the pulsed audio oscillator shown in the diagram. Transistors Q_1 and Q_2, together, form an emitter coupled multivibrator circuit, and Q_2 is a grounded base audio oscillator. Once each cycle, the multivibrator action shuts off the normally free-running audio oscillator. The oscillator output is thus pulsed as shown in the diagram.

The oscillator ON time is controlled by the RC time constant in series with the charge path 1 in the figure. Charge path 2 establishes the oscillator OFF time. It was desired to have a small duty cycle, ON time much less than OFF time. This action was accomplished by the addition of diode CR_1. The

diode conducts during the oscillator ON time and effectively shorts R_4. During the OFF time R_4 is in the circuit, hence the OFF time is greater than the ON time. Resistor R_4 controls the OFF time independent of the ON time. Resistor R_3 can be adjusted



Diode provides small duty cycle of pulsed audio oscillator.

to control the ON time but it will also effect the OFF time in the same direction.

The collector of Q_2 must not employ a series dropping resistor or saturation will take place and the oscillator action will be destroyed. Capacitor C_4 together with the transformer's primary inductance set the oscillator frequency. For the component values specified, the oscillator frequency is 920 cycles, the ON time is 0.07 second, and the OFF time is 0.27 second.

The circuit is designed for good bias stability and it is not very voltage sensitive. The 32-volt supply gives a secondary output of 21 volts, rms.

Unusual Emitter Follower RC Oscillator

VOLTAGE GAIN of an RC network can be arranged to be greater than unity with zero phase shift at a particular frequency. If this is used as a feedback element with an emitter follower amplifier, oscillation will result provided the loop voltage gain is greater than unity.

This technique gives a simple one-transistor RC oscillator of high stability, predictable performance, large output voltage, and low distortion. Because the emitter follower connection gives relatively high input impedance and low output impedance, the RC network may be severely mismatched to the amplifier, and thus the frequency determining parameters may be made independent of the transistor. The frequency may be adjusted over a wide range by simultaneous adjustment of the capacitors, or over a narrower range by adjustment of only one capacitor, (C of Fig. 3), which may be a varicap.

Suitable circuits may be derived from 180-degree phase shift networks. Figure 1 shows a generalized three-terminal network giving such phase shift. It is seen that the voltage of terminal 3 with respect to terminal 2 is greater in magnitude than the input voltage. If the terminals are interchanged as in Fig. 2, terminal 2 being grounded, the output voltage will be greater than the input voltage, and in phase with it. As the network is passive, there cannot be power gain; the output impedance is higher than the input impedance.

Many networks of this type are suitable as oscillators. One useful version is shown on Fig. 3. The gain of this circuit at $W_o = G/C$ is

$$\left(\frac{e_i}{e_o}\right)_{W_o} = \frac{n(1+m+n)}{1+m+mn+n^2}$$

This is maximum for a given value of m if $n = (1 + m)(1 + \sqrt{2})$, when

$$\left(\frac{e_i}{e_o}\right)_{W_o} = \frac{4+3\sqrt{2}}{4+2\sqrt{2}+m(1+\sqrt{2})}$$

This reaches its maximum value at $m = 0$, and drops to unity at $m = \sqrt{2}$.

The input and output impedances are

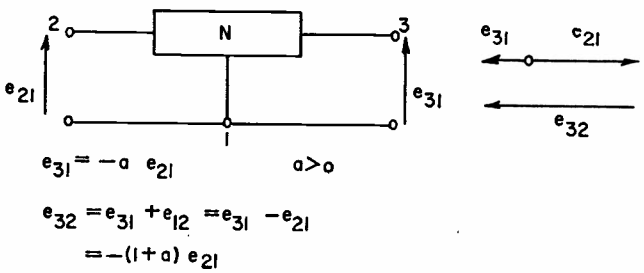


FIG. 1—Three-terminal network provides 180-deg phase shift.

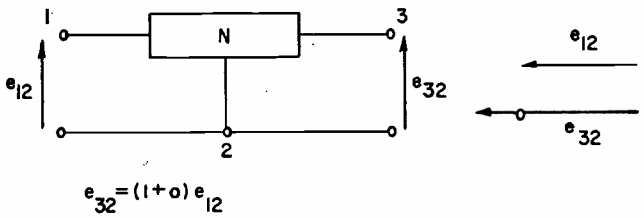


FIG. 2—Network with terminals transposed.

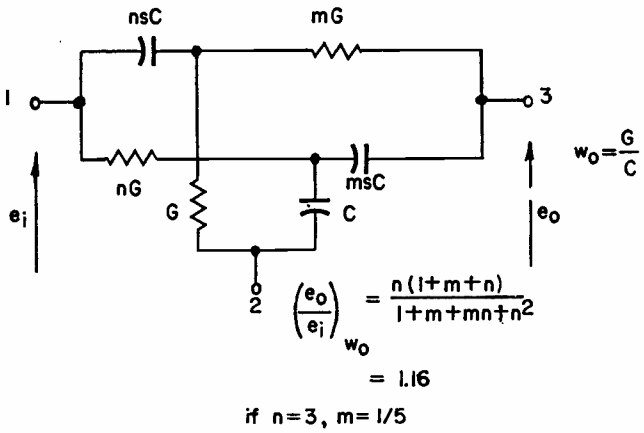


FIG. 3—Oscillator circuit formed from network.

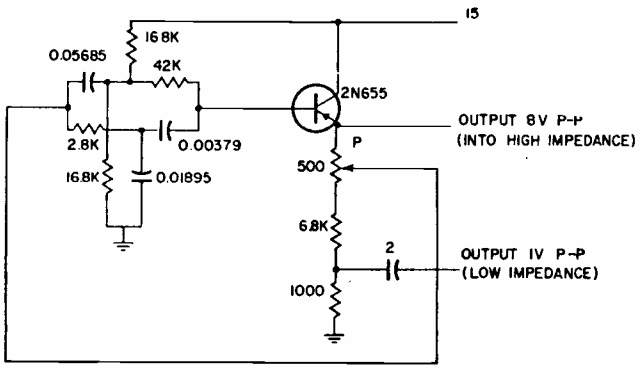


FIG. 4—Emitter follower oscillator has high stability and output.

$$\frac{1-j}{2G}\ \frac{1+m+mn+n^2}{m^2+n+n^2}$$

$$Z_o = \frac{1-j}{2G}\ \frac{n(1+m)\ \ (1+m+n)}{m(m^2+n+n^2)}$$

Suitable practical values are $m = 1/5$, $n = 3$ giving a gain of 1.16, when $Z_i = 0.64R$, $Z_o = 4.44R$, where $R = 1/G$.

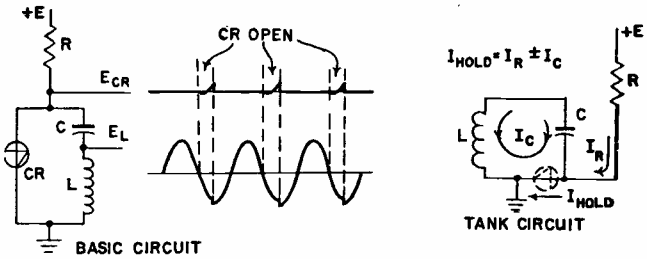
A suitable 1-kc oscillator circuit is shown in Fig. 4, using only one power supply. Potentiometer P sets the gain to achieve low distortion. An output voltage of about 8 volts p-p may be obtained with a 15-volt power supply. The load must be large enough to keep the gain above 0.862. If the load is tapped down on the emitter resistor, as indicated, the oscillator will be immune to load variations, even a dead short circuit. The effective source impedance will be somewhat less than 1000 ohms with the values indicated.

Current analogs of these circuits using the common base connection may also be built. Mismatch between amplifier and network is in this case easier to achieve, but the waveform is generally not as good, unless more complex amplitude control elements are used.

Quasi-Sinusoidal Relaxation Oscillator

RELAXATION OSCILLATORS are usually associated with sawtooth waveforms and neon glow tubes; however, this relaxation oscillator generates a sinusoidal output and uses a 4-layer (or Shockley) diode. Only four parts are required: the diode, a resistor, a capacitor, and an inductor (which can be the primary winding of a transformer).

Basically, the circuit is an oscillating tank circuit which is periodically re-energized by a relaxation type of operation. When E is first applied current will flow into the series LCR circuit and the voltage across the diode will begin to rise. In the "open" state the megohm impedance of the diode will have little effect on the LCR circuit hence it may be neglected; however when diode voltage reaches the critical or firing voltage, the diode will suddenly become a low impedance of a few ohms. With the diode fired, the circuit becomes the LC tank circuit shown. The diode will remain fired until the circulating tank current reduces the resistor current below the holding current of the diode. When the diode opens, the series circuit will be formed again and one cycle of operation will be complete.



Waveforms and tank circuit action in quasi-sinusoidal relaxation oscillator circuit.

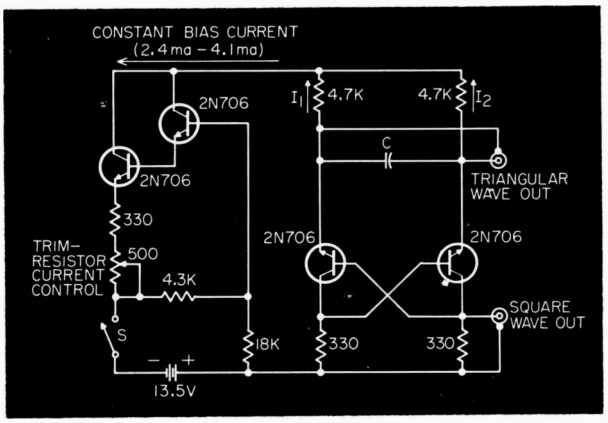
Component values of L and C will depend upon the desired frequency of operation; the 4-layer diode must have a firing voltage less than the applied voltage, other characteristics, (recovery time, holding current, etc.) will depend upon the application. The exact value of R can best be obtained experimentally, by adjusting for the minimum resistance required to maintain oscillation (this also provides the most sinusodial output waveform). Normally, the resistor value will be less than the product of the holding current and firing voltage; this is due to the addition of the circulating current in the LC tank circuit to the resistor current. Hence the Q of the LC circuit and output loading are compensated for by the proper value of R. It is noted that R does have a minimum value (when the resistor current exceeds the sum of the holding current and circulating current) which will cause the diode to remain fired continuously.

Frequencies from 15 kc to 175 kc have been generated using standard 4-layer diodes. Typical values for 120 kc unit using a 30-volt diode are: $E = 45$ volts, $C = 0.0003$ μf, $L = 25$ mh, $R = 2.6K$,

Improved Multi With Continuously Variable Rep Rate

THE BASIC MULTIVIBRATOR shown has a square wave output across the collector resistor and a triangular wave output across the capacitor. (See Circuit Design No. 56, EEE, Oct., 1964 by Peter Lefferts.) When this circuit is biased from a constant-current source, the tops of the square wave

become flat. and the triangular wave becomes linear. When the current source is made variable, the repetition rate becomes variable.



Improved multi with continuously variable rep rate.

The expression describing this variation of the period with current is:

$$T \propto \frac{C(I_1 + I_2)}{I_1 I_2}$$

In a symmetrical arrangement $I_1 = I_2$.

$$T \propto \frac{2C}{I_1}$$

The repetition rate thus varies directly with the magnitude of the constant biasing current.

Capacitance Value-C		Repetition Rate—Continuous Variation
100	µf	5.6 cps to 10 cps
10	µf	56 cps to 100 cps
1	µf	560 cps to 1 kc
0.1	µf	5.6 kc to 10 kc
0.01	µf	56 kc to 100 kc
0.001	µf	560 kc to 1 mc
330	pf	1.55 mc to 2.68 mc

Therefore, by using a variable current control resistor, one multivibrator can be used over a very wide range of repetition rates with few components, as is shown in the table. For this circuit the repetition rate may be varied by more than 70 percent. If an analog waveform is impressed on the current biasing transistor, voltage-to-frequency conversion results.

Because the amplitudes of both the square wave and the triangular wave are fixed by the transistor internal voltage drops, these amplitudes remain fairly constant over the full frequency range.

High Efficiency Relaxation Oscillator

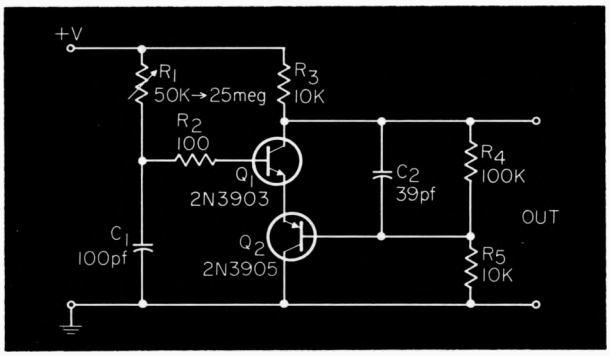
THIS CIRCUIT was developed for use as a voltage-controlled oscillator in a high efficiency switching regulator. It is a relaxation-type oscillator which provides short, fast pulses to trigger a multivibrator. It has many advantages over the common unijunction relaxation oscillator, such as: higher power output, lower power consumption, faster pulse rise-time, higher maximum operating frequency, higher reliability, and, with the new plastic-case transistors, lower cost.

The oscillator consists of a simple *R-C* ramp generator coupled to a high efficiency trigger circuit. In the circuit, Q_1 is initially off if the voltage at its base is less than:

$$V_{B1} = \frac{V R_3}{R_3 + R_4 + R_5} + V_{BE1} + V_{BE2}$$

Timing capacitor C_1 will charge up via control resistor R_1 until its voltage reaches the point at which Q_1 begins to conduct. If resistor R_1 can supply enough current (about 1/2 µa) Q_1 turns on. As Q_1 turns on its collector voltage falls, driving the base of Q_2 negatively, causing Q_2 and thus Q_1 to conduct more. Both Q_1 and Q_2 will be driven into saturation by the charge in C_1 and C_2. The base current of Q_1 in saturation will discharge C_1 through limiting resistor R_2; and if resistor R_1 cannot supply enough current to keep Q_1 in saturation (about 0.5 ma), the trigger will turn back off by the same regenerative action that turned it on.

Using the parts values shown, the permissible range of values for R_1 is found to be between 50 K and 25 meg. With R_1 set at 1 meg the oscillator operates at about 75 kHz putting out 10-v negative-going pulses with risetimes



Relaxation oscillator composed of ramp generator driving a trigger circuit.

of 10 nsec and fall times of 1 µsec. Power consumption is 1.5 mw.

With R_3 at 10 K the upper operating frequency is about 1 MHz, limited by the recharge time of C_2 through R_3 and R_5. Pulse width is about 0.5 µsec but can be lengthened by increasing C_1 and/or R_2. For example, with $C_1 = 100$ µf, $R_1 = 1$ meg, the pulse width is 25 msec and the frequency is 0.25 Hz.

Supply voltage and temperature affect the frequency since they set the charging rate of C_1 and the triggering voltage. In a closed loop feedback system, with R_1 replaced by a control transistor, the effects of supply voltage and temperature on the frequency will be compensated for by the feedback.

Costs might be estimated as follows: Q_1 and Q_2: \$0.50 each; R_1 to R_5: \$0.05 each; and C_1 and C_2: \$0.23 each, for a total component cost of \$1.71.

Voltage-Controlled Oscillators

THE USUAL LOW-FREQUENCY voltage-controlled oscillator is a relaxation oscillator delivering a rectangular or pulse waveform controlled by a dc voltage, with frequency dependent upon the magnitude of this dc control voltage. The circuit in Fig. 1, however, produces an excellent sine wave with very good linearity over the indicated 1000-cps range.

This circuit is basically a resistance-controlled three-section phase-shift oscillator. The frequency of the circuit,

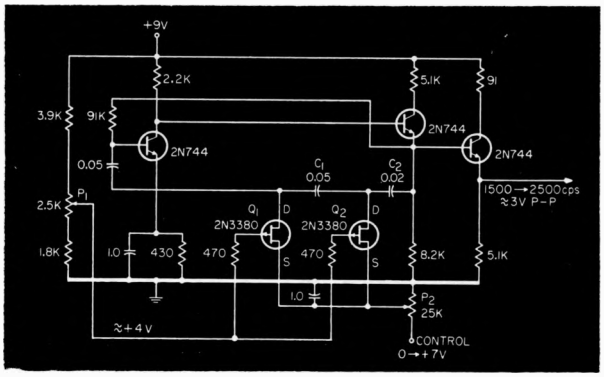


Fig. 1. Voltage-controlled oscillator using FETs.

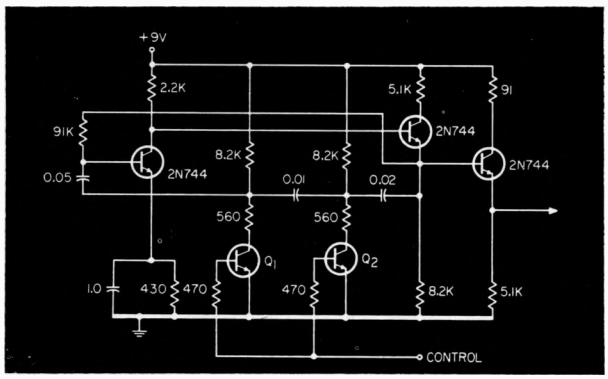


Fig. 2. Voltage-controlled oscillator using conventional transistors in place of FETs.

using untapered sections, is determined from:

$$f \simeq \tfrac{1}{2}\sqrt{6}\ \Pi\ RC.$$

In this oscillator, field effect transistors Q_1 and Q_2 appear as linear voltage-variable resistors controlled by 0-7v.

The circuit in Fig. 2 uses conventional transistors in place of the FETs. Linear frequency response with respect to the contol voltage, does not exist in the circuit since Q_1 and Q_2 are operated in the knee region. However, lack of linearity when the control voltage is servo'ed may not be a disadvantage. Note that in each circuit an increasing voltage increases frequency.

Modified UJT Oscillator Has No Timing Error

WHEN POWER is applied to a conventional unijunction oscillator circuit (Fig. 1), the capacitor C must charge from zero volts to the peak-point voltage V_P before the first pulse occurs at B_1. For succeeding pulses, C charges from $V_{E(SAT)}$ to V_P. This causes a difference between the period of the first cycle and that for succeeding cycles, as shown in Fig. 1b. The error may be serious in some applications. It can be eliminated by a simple circuit modification.

Fig. 2a shows a method requiring one extra transistor and two resistors. When power is applied, Q_2 saturates and rapidly charges C to $V_{E(SAT)}$. The voltage at point A is equal to $V_{E(SAT)} + V_{BE}$, Q_2 is cut off and no current can flow into C except through the timing resistor R_T.

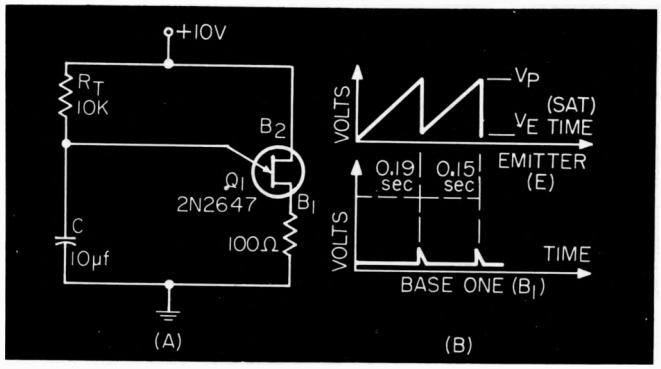


Fig. 1. Basic UJT oscillator (A) with waveforms (B). This circuit has timing error, due to time taken to charge capacitor to V_p during first cycle.

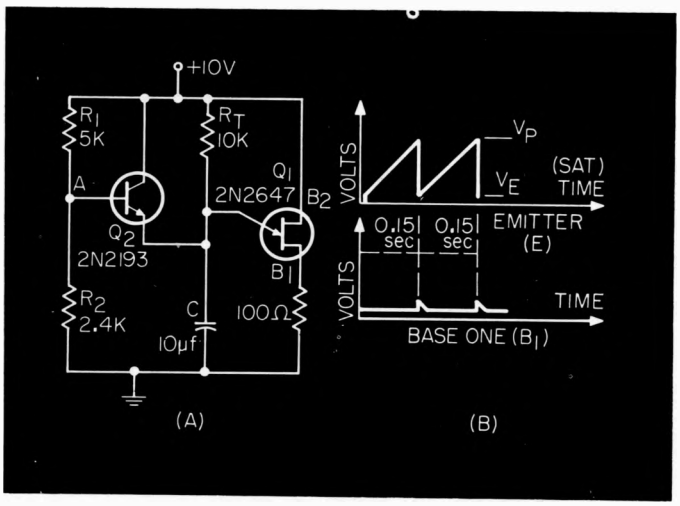


Fig. 2. Modified circuit has no error because capacitor is initially charged by transistor Q_2.

Modified Unijunction Oscillator Reaches 500 kHz

THE BASIC unijunction transistor relaxation-oscillator circuit of Fig. 1a is limited to approximately 70 kHz. However, by adding a transistor and resistor as shown in Fig. 1b the frequency range can be extended to 500 kHz.

For the basic circuit to oscillate, the load line formed by charging resistor R_T and supply voltage V_1 must intersect the UJT characteristic curve in the negative-resistance region to the left of the valley point as shown by line A in Fig. 2. The minimum value of R_T is, therefore, restricted by this point. Reducing the value of C_T can also increase

the frequency of oscillation, but its minimum value is restricted by the inherent characteristics of the UJT. Therefore C_T will be treated as a constant.

With the addition of Q_2 and R_2 (Fig. 1b), the value of R_T can be reduced so that the static load line is as represented by line B in Fig. 2. The circuit oscillates because the dynamic load line is actually as shown by line C.

In the modified circuit, transistor Q_2 is normally cut off and the charge current for C_T is $(V_1-V_E)/R_T$. When Q_1 fires, Q_2 goes into saturation, and the charge current

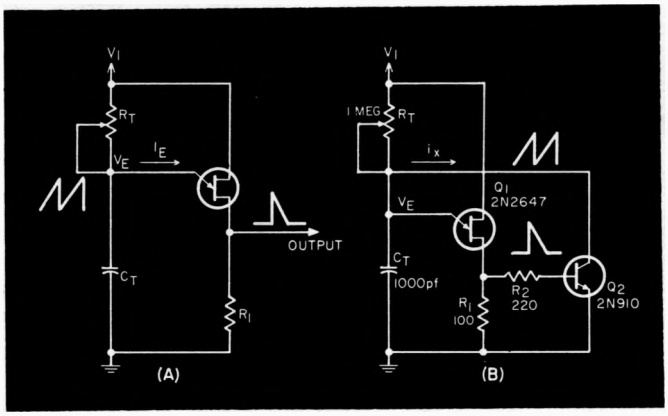


Fig. 1. Basic unijunction relaxation oscillator (a) is limited to frequencies below 70 kHz. By adding transistor Q_2, this range can be extended to 500 kHz.

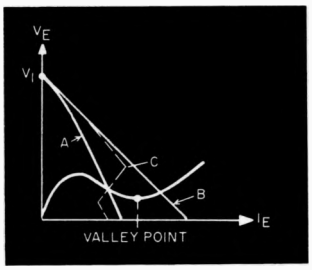


Fig. 2. Characteristic curves for basic and modified relaxation oscillator circuits.

i_x flows into the collector of Q_2. The resultant decrease in Q_1 emitter current shifts the load line into the negative-resistance region of the characteristic curve and oscillation is sustained.

Simplified one-shot multivibrator

COMPLEMENTARY SWITCHING transistors simplify the design of a one-shot multivibrator. The resulting circuit has the advantage that quiescent current is negligible.

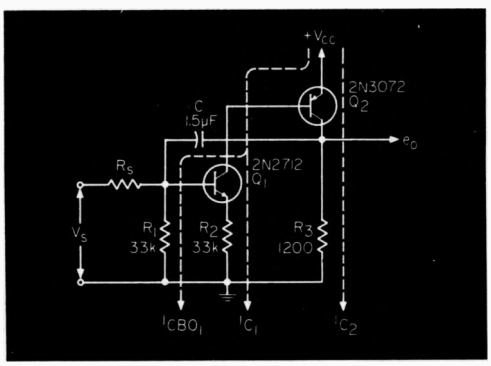
The circuit is extremely versatile. With minor changes in component values it will also work as a free-running multivibrator or as a trigger circuit.

Let's look first at the one-shot mode. The circuit is shown in Fig. 1, with typical component values for one-shot operation.

When the circuit is dormant, Q_1 and Q_2 are both inactive and there is no charge on the capacitor. When a positive pulse is applied to the base of Q_1, both transistors turn on and drive one side of the capacitor positive. Regenerative feedback then causes Q_2 to saturate. This places the circuit in the steady-state "on" condition and puts almost the entire supply voltage across C.

The circuit remains "on" until the capacitor discharges through base resistor R_1. After this discharge period (determined by time constant R_1C) the circuit returns to the initial state.

Current flow, for the one-shot



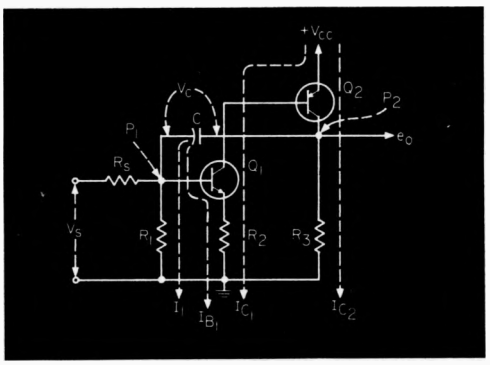


Fig. 1. (left) Complementary transistors simplify design of one-shot multivibrator. Current flow paths are shown for the quiescent "off" state. Fig. 2. (right) One-shot circuit redrawn to show current flow after triggering. With modification of component values, the same basic circuit becomes a free-running multivibrator.

circuit in the "off" condition, is shown in Fig. 1. The currents are the leakage current of Q_1 and the low collector currents of Q_1 and Q_2. Using the well-known relationships between these currents, we find that for the stable state,

$$I_{cbo1}R_1 < \beta_1 R_2 I_{cbo1} + V_{be1} \quad (1a)$$

or

$$R_1 < \beta_1 R_2 + (V_{be1}/I_{cbo1}) \quad (1b)$$

We can see, therefore, that the voltage required to turn on Q_1 is as shown in Eq. 2.

The circuit will become a free-running multivibrator if the component values are such that the relationship of Eq. 1 changes to that shown in Eq. 3.

Further, if the relationship of Eq. 1 is reversed, the circuit becomes a trigger circuit with a stable "on" state that can be triggered off with a negative input pulse.

For the normal one-shot mode, we can derive the circuit equations as follows: If the circuit has been activated by a positive pulse it is in its metastable state and current flow is as shown in Fig. 2. The input level returns to zero at the end of the input pulse, and the capacitor charges to a voltage V_c given by Eq. 4. We can express the collector current in terms of V_{cc} and R_1. This modifies the expression for capacitor voltage to give Eq. 5.

The capacitor then starts to discharge through R_1 and R_2, producing a voltage at Q_1 base

$$V_T = I_{cbo1}\,(\beta_1 R_2 - R_1) + V_{be1} \quad (2)$$

$$V_{be1} = I_{cbo1}\,(\beta_1 R_2 - R_1) \quad (3)$$

$$V_{co} = V_{cc} - V_{sat2} - I_{c2}R_2\left(\frac{\beta_1 + \beta_2}{\beta_1\beta_2}\right) \quad (4)$$

$$V_{co} = (V_{cc} - V_{sat2})\left(\frac{R_3\beta_1\beta_2 - R_2\,(\beta_1 + \beta_2)}{R_3\beta_1\beta_2}\right) \quad (5)$$

$$V_{b1} = V_{co}\exp\left(-\frac{R_1 + R_2}{R_1 R_2 C}\,t\right) \quad (6)$$

$$V_t = V_{be} + \frac{R_2\,(\beta_1 + 1)}{R_3\beta_1\beta_2}\,(V_{cc} - V_{sat2}) \quad (7)$$

$$T_1 = \frac{R_1R_2C}{R_1 + R_2} \times \left[\frac{(V_{cc} - V_{sat2})\,[\beta_1\beta_2R_3 - R_2\,(\beta_1 + \beta_2)]}{V_{be}R_3\beta_1\beta_2 + R_2\,(\beta_1 + 1)\,(V_{cc} - V_{sat2})}\right] \quad (8)$$

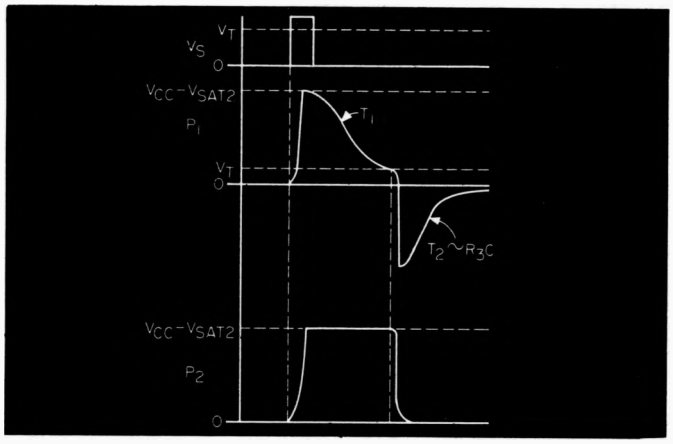


Fig. 3. Typical voltage waveforms for the circuit of Fig. 2. operating in the one-shot mode.

given by Eq. 6. This voltage turns off Q_1 when it decreases to the value given by Eq. 7. Therefore the total "on" time for Q_1 is given by Eq. 8.

Typical waveforms for the one-shot multivibrator are shown in Fig. 3.

Cascade UJT oscillator generates linear frequency sweeps

THIS SWEEP OSCILLATOR consists of two stages, shown separated by the dotted line in Fig. 1. The first stage generates a low-frequency sawtooth signal that controls the higher-frequency sawtooth generator of stage two. Both stages are simple relaxation oscillators using unijunction transistors.

The first stage determines the repetition rate and frequency range of the swept output. The second stage generates the output sawtooth waveform and determines the amplitude.

Figure 2 shows the emitter-voltage waveform of Q_1. The amplitude of this signal determines the frequency range of the sweep, while the frequency determines the repetition rate of the sweep.

When the first-stage output voltage is applied to the second stage via buffer-amplifier Q_2 the second stage oscillation frequency increases as the control voltage rises. Output frequency can be calculated from the following equation:

Figure 3 shows the relationship between V_{E2} and the output frequency. Fig. 4 lists the effects of the various components that control the performance of the generator.

Of course, the maximum operating frequencies are restricted by the characteristics of the unijunction transistors. Also, the frequency of the second stage must be higher than the frequency of the first stage. Usually, a ratio of ten or more is acceptable.

Both oscillators in this circuit have better linearity than standard unijunction oscillators. This is because the capacitor charging voltages are greater

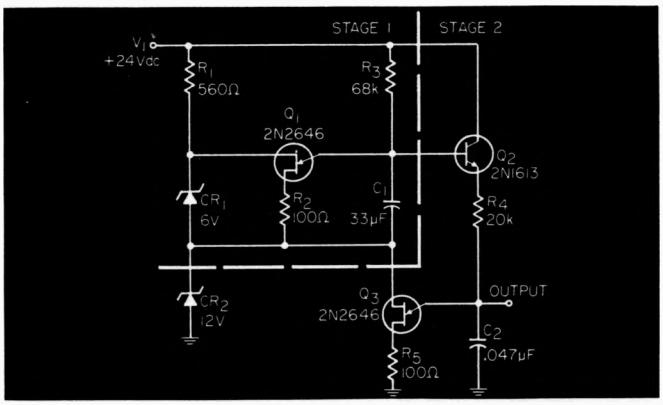


Fig. 1. Simple sweep-frequency generator consists of two cascaded unijunction oscillators.

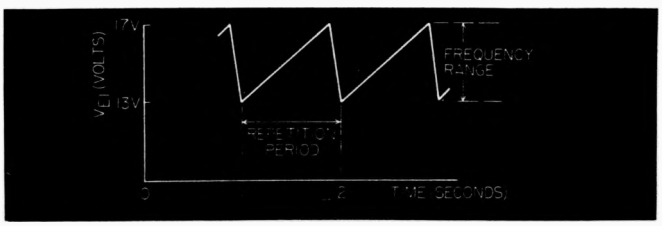


Fig. 2. Waveform of the first unijunction oscillator determines the repetition rate and frequency range of the swept output.

than the corresponding interbase voltages of the unijunctions. Sweep linearity can be further improved by replacing R_3 with a constant-current source.

In the original application, the sweep generator output was passed through a narrow bandpass filter to produce a short-duration signal. Figs. 1, 2 and 3 show component values and performance for the circuit that was built and tested for this application.

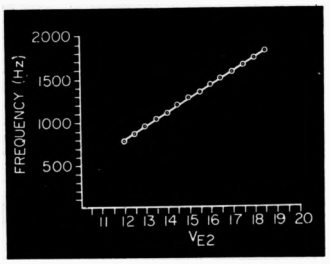


Fig. 3. Output frequency of the second stage is a linear function of the emitter voltage of Q_2.

$$f = \frac{1}{R_4C_2 \ln\left(\frac{VE_{E2} - V_{E3}\ (min)}{V_{E2} - V_{E3}\ (max)}\right) + t_r} \qquad (1)$$

where V_{E3} (max) = V_P = emitter peak-point voltage and t_r = emitter-voltage fall time

Fig. 4. Circuit parameters can be varied independently by changing component values as shown in this table.

	Adjust	To Increase	To Decrease
Freq range	CR_1	Increase V_{CR1}	Decrease V_{CR1}
Rep rate	$T_{C1} - R_3C_1$	Decrease T_{C1}	Increase T_{C1}
Freq output	$T_{C2} = R_4C_2$	Decrease T_{C2}	Increase T_{C2}

Linear VCO generates sawtooth and square waveforms

USING IC OP AMPS, one can design an inexpensive voltage-controlled oscillator having better than 0.5-percent linearity over a freqency range of almost an octave. Component cost for the complete circuit shown in Fig. 1 is less than $40.00. Though other VCO circuits can be built at lower cost, they do not have the performance of the circuit shown here. For example, neither biased astable multivibrators nor unijunction-transistor oscillators can approach the linearity of this circuit.

With the component values shown in Fig. 1, the output frequency covers the range 40 to 70 kHz, when the input voltage is varied from 4 to 7 Vdc. The center frequency depends on the value of capacitor, C_1. Center frequencies, from 30 Hz to 750 kHz, can be achieved simply by changing C_1 from 2 μF to 60 pF.

Frequency stability is good. During tests on the prototype circuit at constant ambient temperature and with constant input voltage, the output frequency changed less than 0.1 percent in two hours after a 45-minute warmup. A 60°F increase in ambient from normal room temperature increased the output frequency by four percent. Heat sinks on the op amps aid temperature stabilization and were used for the circuit tested.

The circuit simultaneously produces both sawtooth and square wave outputs. Phase of these output signals is synchronized as shown in Fig. 2. The square wave has a rise time of 100 ns from 0 to ±0.6 V. This output is suitable for direct coupling to some types of IC logic circuits. Of course, the sawtooth wave can be easily filtered to give a sine wave if desired.

The circuit works as follows: A dc input voltage and its inverse generated by amplifier A_1, are applied alternately through diodes D_9, D_{10}, to the op-amp integrator A_2. When the output voltage of A_2 reaches one of two threshold levels, V_{T1} or V_{T2}, it triggers the multivibrator circuit A_3. The following equations define the threshold levels V_{T1} (for positive-going charge) and V_{T2} (for negative-going charge):

$$V_{T1} = \frac{R_3 + R_4}{R_2} \times (12 - E_D) \qquad (1)$$

$$V_{T2} = \frac{R_3 + R_4}{R_1} \times (12 + E_D) \qquad (2)$$

(where E_D is "on" voltage of a single diode).

Because the output of the multivibrator is connected to the diode bridge, the network D_7 through D_{10} periodically reverses the direction of charge current to A_2 and, therefore, periodically changes the polarity of the ramp voltage at the output of A_2.

The sawtooth, generated at the output of A_2, has voltage limits determined by Eqs. 1 and 2. If $R_1 = R_2$, and $R_5 = R_6$, the output from A_3 is a square wave having an amplitude of approximately 3 V. The trailing edge is rounded as shown in Fig. 2. The period T of the square wave is given by Eq. 3

$$T = \frac{C_1(V_{T1} - V_{T2})\ (R_5 + R_6)}{V_{in} - E_D} \qquad (3)$$

Note that the multivibrator A_3 is never allowed to saturate.

To operate the VCO at frequencies below 10 kHz, the circuit designer should add a resistor in parallel with C_1. This will prevent A_2 from integrating its offset current. The total time constant of the added resistor and C_1, should be much longer than the period of the VCO output.

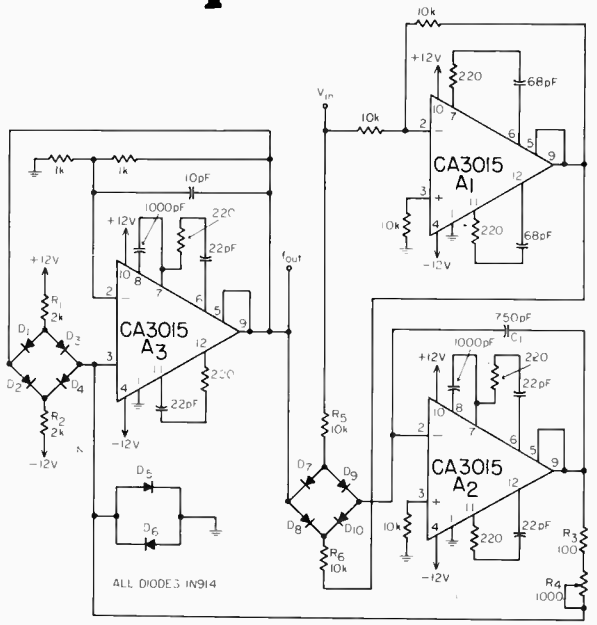
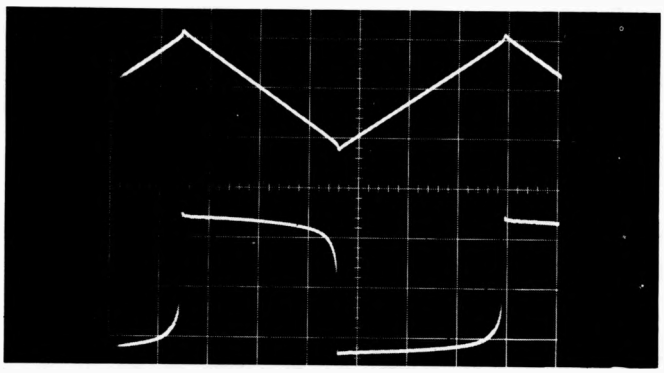


Fig. 1. IC op amps simplify the design of this VCO which gives a triangular wave at the output of A_2 and a square wave at the output of A_3.

Fig. 2. Typical output waveforms for the circuit of Fig. 1. Vertical scales are 2 V/div for the triangular wave and 1 V/div for the square wave. Horizontal scale is 2 μs/div.



Wide Range VCO Uses IC

ADDING TWO resistors and two capacitors will convert a $3 IC logic element into a miniature voltage-controlled oscillator. The complete low-cost VCO is useful as an fm generator, phase-locked loop reference, or analog-to-digital converter.

The MECL MC359 dual NOR gate is cross-coupled with C_1 and C_2 to form an astable multivibrator. The following equation determines the frequency of oscillation:

$$f = \frac{1}{R_1C_1 + R_2C_2} \times \frac{1}{\ln \frac{e_1 - e_2}{e_1 - e_3}}$$

Where e_1 is the control voltage, $e_2 = -1.2$ V and $e_3 = -0.9$ V for the MC359.

Minimum Frequency Versus Capacitance, with Zero Control Voltage.

C_1, C_2	Frequency
100 μF	0.5 Hz
10 μF	6.3 Hz
4700 pF	20 kHz
110 pF	757 kHz

The circuit shown in Fig. 1 has a linearity of ±5% over a frequency deviation of ±55% of center frequency. Sensitivity is greater than 24% of center frequency per volt. Fig. 2 shows a typical response for a center frequency of 112 kHz.

Measured temperature stability is 0.08%/°C. Maximum frequency of oscillation is above 2 MHz and the minimum frequency is limited only by the size of the components, as shown in the table.

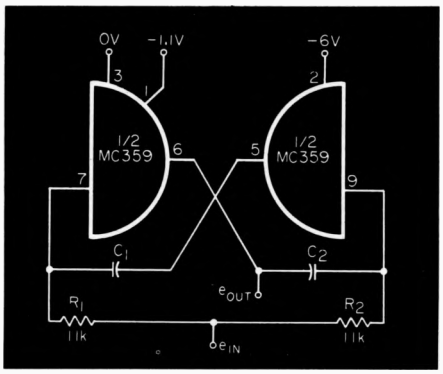


Fig. 1. Cross-coupled NOR gate provides sensitive low-cost VCO.

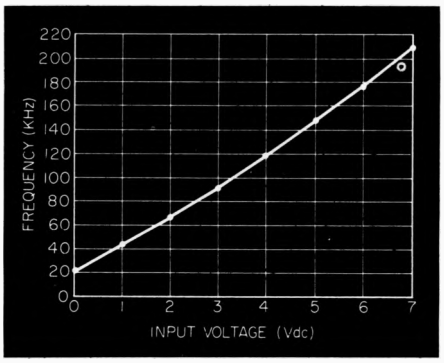


Fig. 2. Variation of frequency with control voltage is linear within ±5%.

FET controls crystal oscillator

CHANNEL RESISTANCE of a FET is voltage dependent. When operated without drain bias, the N-channel depletion-type junction FET, specified here, acts as a linear resistor for ac signals up to about 1 V pk-pk. The voltage-dependent resistance can be used to vary the effective tuning capacitance of a crystal and, thus, the frequency of a crystal oscillator. The oscillator described was used in a phase-locked loop as a 3.58-MHz subcarrier oscillator for color television.

Figure 1 shows the relationship between drain current and drain voltage when small positive and negative drain-source voltages are applied to a 2N5163 FET. Note that, over the range shown, each current - voltage characteristic is like that of a resistor whose value is determined by gate-source voltage. Though the curve is shown only for V_{DS} up to ± 50 mV, the relationship is, in fact, linear for higher values of V_{DS} to about ± 0.5 V. Thus ac signals of up to 1 V pk-pk can be handled without distortion.

In. Fig. 2, we can see more clearly how drain-source impedance varies with the applied gate-source voltage. Note that the reactive component is almost constant and that resistance varies substantially. This suggests that the device can be useful as a voltage - controlled resistor for small ac signals.

But, FETs have one major disadvantage for many circuit applications. There are wide variations in I_{DSS} ("on" current) and g_m (forward transconductance) due to production spreads and the effects of temperature. Usually this means that devices must be carefully selected or that the circuit must have "set-up" controls or considerable negative feedback.

However, in the case of zero drain-source bias (i.e. ac coupling), I_{DSS} has little effect and no correction for its variation is needed. Furthermore, as the oscillator described here is intended for use in a phase-locked loop, variations in g_m can also be ignored, as long as we provide the minimum necessary loop gain. In this application, the FET offers the additional advantage of high input impedance. Thus it easily interfaces with a simple phase detector.

Figure 3 shows the equivalent

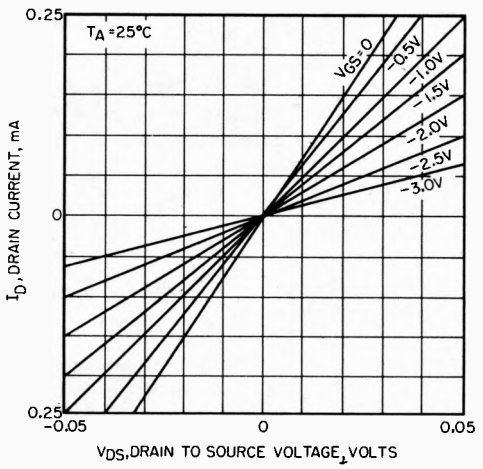


Fig. 1. For small values of V_{DS}, the 2N5163 FET behaves like a resistor with value determined by V_{GS}.

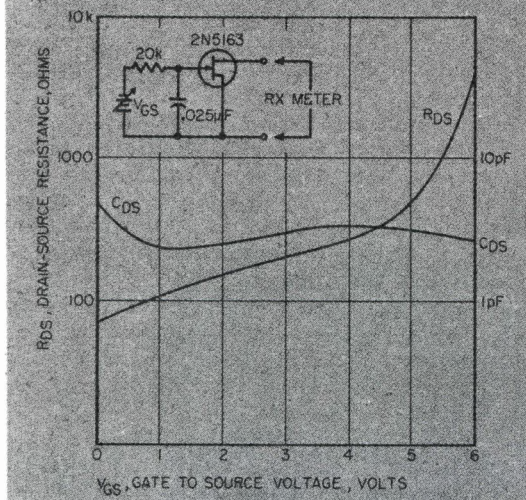


Fig. 2. The capacitive component of the FET output impedance varies little with changes of V_{GS}.

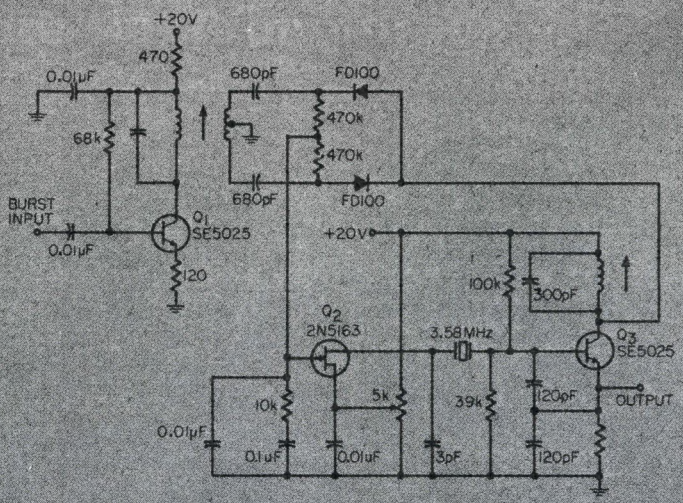


Fig. 6. Complete phase-locked oscillator loop. The FET presents a high input impedance to the output of the phase detector.

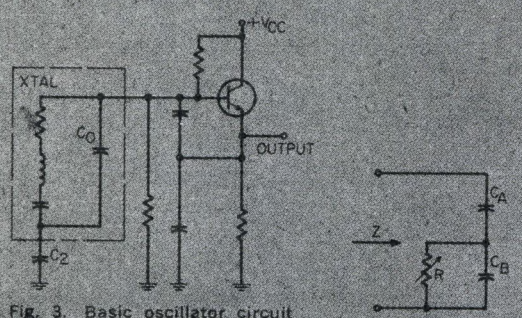
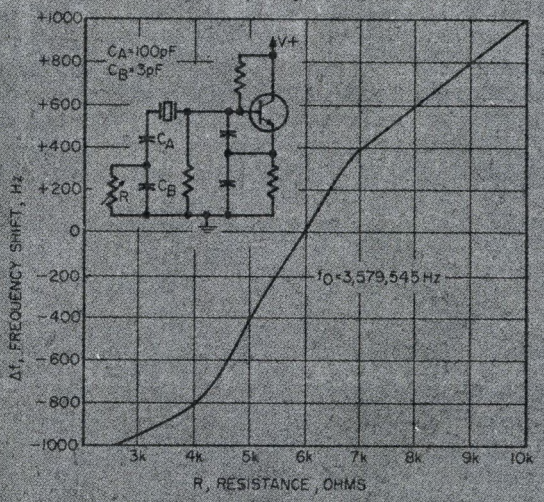


Fig. 3. Basic oscillator circuit showing the equivalent circuit for the crystal.

Fig. 4. Effective capacitance of this simple network can be varied by adjusting resistor R.

Fig. 5. Capacitor C_2 (Fig. 3), can be replaced by an RC network (Fig. 4) to achieve frequency control. Curve shows relationship between frequency and the value of R.



circuit of the basic crystal oscillator without FET control. Oscillation frequency is given by Eq. 1.

$$\frac{f_o - f_r}{f_r} = \frac{1}{2\left(\frac{C_o}{C_1}\right)\left(1+\frac{C_m}{C_o}\right)} \quad (1)$$

where f_r is series—resonant crystal frequency
f_o is oscillating frequency
C_m is effective circuit capacitance seen by crystal
C_o is shunt capacitance of crystal
C_1 is equivalent series capacitance.

Also,

$$C_1 = \frac{2C_2\,\Delta f}{f_r} \quad (2)$$

where C_2 is series capacitance required to produce frequency change Δf when oscillator frequency is f_r.
Therefore,

$$f_o = f_r - \frac{\Delta f}{(C_o + C_m)} \times C_2 \quad (3)$$

To see how we can vary effective capacitance with a voltage-controlled resistor, let's look first at the simple RC circuit of Fig. 4. The impedance of this network is given by Eq. 4.

$$Z = -j\left(\frac{1}{\omega C_A} + \frac{1}{\omega C_B + \frac{1}{\omega C_B R^2}}\right) + \frac{R}{1+\omega^2 C_B{}^2 R^2} \quad (4)$$

So, as R goes from zero to infinity, capacitance of the network goes from

$$C_A \text{ to } \frac{C_A C_B}{C_A + C_B}$$

If, now, we substitute this network for the tuning capacitor C_2 in the crystal-oscillator circuit of Fig. 3, we will be able to control the oscillating frequency f_o by varying the resistance R. Fig. 5 shows the frequency control achieved with this technique.

In the complete circuit, shown in Fig. 6, R is replaced by a FET circuit. Given the crystal parameters and the desired control range for the oscillator, one can easily determine the FET operating point, and derive the necessary values for C_A and C_B in a practical circuit. Also shown in Fig. 6 is the phase detector that completes the phase-lock loop. In the original application, fine adjustment of a color-TV sub-carrier oscillator allowed accurate control of picture tint.

FET and IC make syncable oscillator

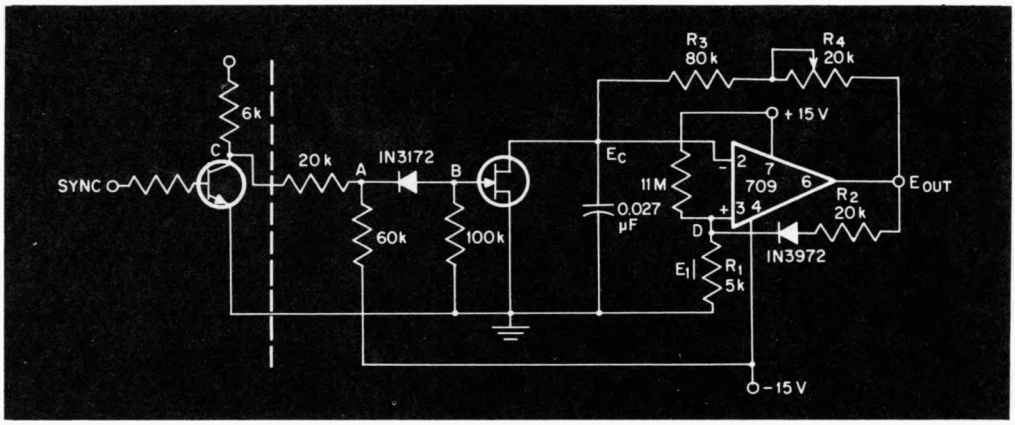


Fig. 1. This square-wave oscillator can be synchronized at frequencies up to 60 kHz.

FIGURE 1 shows a 1-kHz oscillator that can be synchronized over a wide frequency range. Using temperature-compensated resistors (R_1, R_2, R_3, R_4) and a capacitor one can hold the free-running frequency to 1% accuracy from 0° to 60°C.

The output regularly shifts between positive and negative saturation, thus producing a square wave with 50% duty cycle. The frequency is determined by the RC time constant and the voltage divider.

$$f = \frac{1}{2T} = \frac{E_o}{2E_1\ RC}$$

$$E_1 = \frac{1}{RC}\int_0^T E_o\ dt$$

If the output has just switched to positive saturation (+15 V), the capacitor starts charging to +15 V through R_1. But as soon as the voltage level at point D (established by the R_1-R_2 voltage divider), the output switches to negative saturation. Immediately after this transition the capacitor starts discharging towards −15 V. When the capacitor voltage reaches zero, the output switches to positive saturation and the process repeats.

If it weren't for the 11-MΩ resistor, the voltage at point D during negative saturation would be slightly below ground. With the 11-MΩ resistor, point D is 0.7 mV above ground. The capacitor thus normally swings from +0.7 mV to +3 V.

When a sync pulse is received and the output is in negative saturation, point D is at 0.7 mV. When the capacitor discharges to ground the output goes to positive saturation because D is slightly above ground. If the output is in positive saturation when a sync pulse arrives, the output stays in positive saturation. Thus, whenever a sync pulse arrives the output remains in or switches to positive saturation.

The FET used in the circuit is a 2N3972, with a pinch-off voltage of −0.5 to −3 V. The syncing source is an IC gate with a 6-kΩ load. Circuit values are determined as follows:

With the sync amplitude low, there is 20 V across 6 kΩ + 20 kΩ + 60 kΩ.

$$I_x = \frac{20\ \text{V}}{86\ \text{k}} = 0.23\ \text{mA}$$

$I_x \times 60\ \text{k}\Omega = 14$ V. Point A is at −1 V and B is at −0.3 V. The FET shorts the capacitor and thus synchronizes the oscillator.

When sync amplitude is high, point C is at ground and the 20 kΩ is in parallel with the 100 kΩ. Then,

$$I_x = \frac{15\ \text{V}}{20\ \text{k} + 60\ \text{k}} = 1.88\ \text{mA}$$

$I_x \times 60\ \text{k} = 11$ V

Point A is at −15 + 11 V = −4 V. Point B is at −4 + 0.7 V = −3.3 V.

With B at −3.3 V, the FET is cut off and the oscillator functions normally.

The IC, a μA709, operates satisfactorily from 0 to 60 kHz. At higher frequencies, bandwidth limitation causes distortion. For higher frequencies, use a μA702 or μA710.

For large values of C and high frequencies, the capacitor may not fully discharge during the sync pulse. Also, for large values of R offset currents of the operational amplifier tend to cause errors.

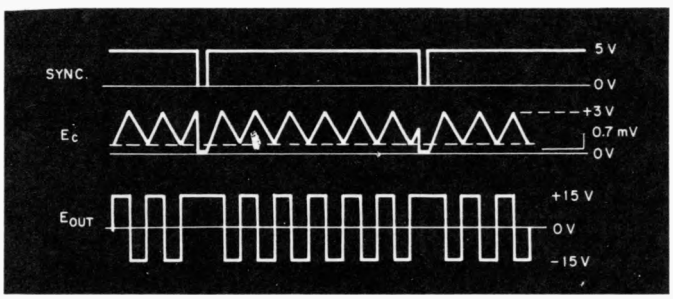


Fig. 2. Capacitor voltage and output waveform in response to sync pulses.

Higher-efficiency chokeless vertical sweep

THE ADVANTAGE of a chokeless vertical deflection circuit for small-screen B&W TV is well known—the elimination of costly copper for choke windings. But the sweep circuit with a choke tends to be about three times more efficient. Its efficiency is typically 25% compared with a bit better than 8% for the chokeless system.

The chokeless circuit of Fig. 1 can be modified to improve the efficiency. In this self-oscillating circuit, feedback from the collector of Q_2 (or from the yoke) to the base of Q_1 and direct connection of Q_2's base to Q_1's collector insure positive feedback. When the supply is turned on, current flows through R_1 and R_2 creating a positive ramp voltage across C_2.

This voltage causes the collector voltage of Q_2 to fall and induces a negative voltage at the base of Q_1, via C_1, thus holding Q_1 off. The emitter voltage of Q_2 also rises as its base voltage rises. This emitter voltage can be fed back to the base of Q_1, tending to charge C_1 such that the base of Q_1 goes positive.

When this happens, Q_1 conducts and turns Q_2 off. The rapid rise of the voltage at Q_2's collector keeps Q_1 conducting for the duration of the retrace period. Retrace time is here controlled by the R_3C_1 time constant which determines the time required for the current to decay to a value such that Q_1 cannot continue to conduct. When Q_2 stops conducting, C_1 starts charging again, repeating the cycle.

Q_2 and Q_3 constitute a totem pole output. As the current in Q_2 rises, the voltage across R_6 rises. The forward-biased diodes D_1 and D_2 couple this voltage back to the base of Q_3, reducing the conduction of Q_3. During retrace, when Q_1 conducts, Q_2 turns off and Q_3 saturates, recharging C_3.

The constant-voltage forward characteristic of the diodes shifts the dc level and couples the voltage across R_6 back to the base of Q_3 without attenuating the ac component.

We can improve the efficiency of this system if we can achieve part of the yoke-current reversal by resonating the yoke with a capacitor and isolating the yoke for the portion of the retrace pulse that exceeds B+. This is done in Fig. 2.

Now let us replace the integrator capacitor C_2 of Fig. 1 with C_4 and C_5 as in Fig. 3, the final circuit. The voltage at the emitter of Q_2 can then be integrated and fed back to provide some linearity correction. Also, C_5 is returned to the yoke to provide overall Miller feedback. C_5 also bootstraps the yoke to the emitter-follower (Q_3) part of the circuit. The size of C_5 affects retrace time. C_9 prevents spurious oscillation.

The final circuit generates a yoke current of 0.6 A pk-pk in a 25-mH, 10-Ω yoke from an 18-V supply. Retrace time is 1.35 ms.

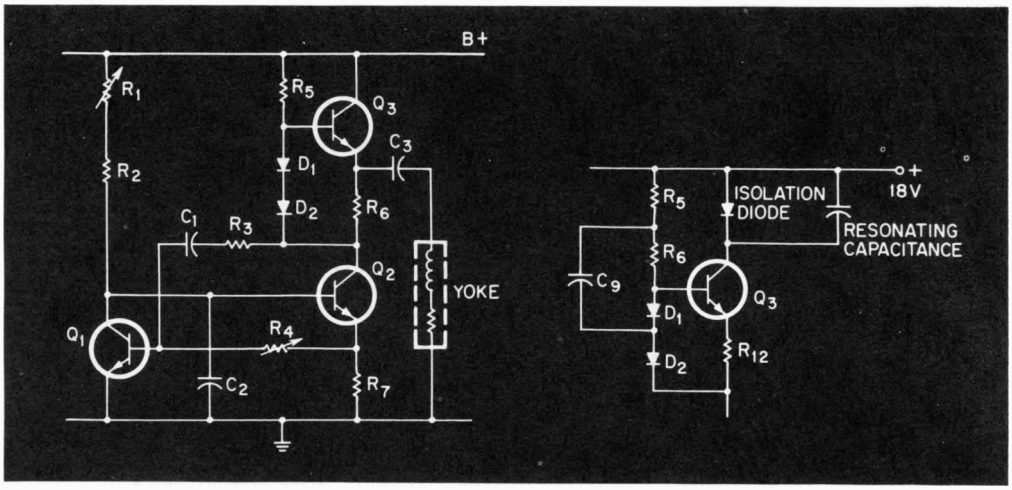


Fig. 1. This self-oscillating vertical-deflection circuit for small-screen black-and-white TV requires no choke. But it is quite inefficient.

Fig. 2. A resonating capacitor improves the efficiency of the sweep circuit.

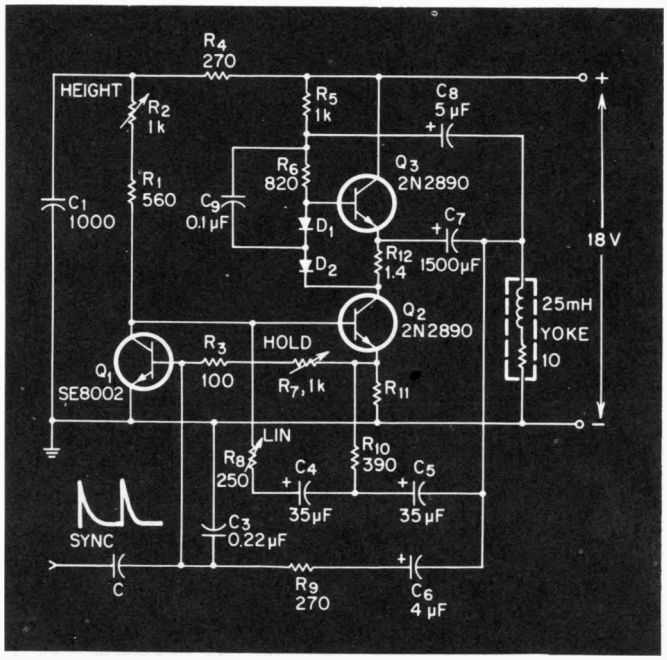


Fig. 3. Further improvements and necessary controls complete the chokeless sweep circuit.

Improved VCO uses TTL IC

OTHER CIRCUIT designers have shown how IC gates can be cross-coupled to form a multivibrator. They have also shown how this type of circuit can be used as a linear VCO[1]. By careful design, using a TTL IC, this type of circuit can be operated at much higher frequencies than before.

With the component values shown, the circuit of Fig. 1 gives a center frequency of 7 MHz, with low and high frequency limits of 3 MHz and 11 MHz respectively. As shown in Fig. 2, the linearity is better than 5 percent of full-scale over the whole range.

The maximum possible frequency for this type of circuit is determined by the practical size of the components in the RC timing networks. Of course, the actual value of the timing capacitance includes stray capacitance and the value of the timing resistance includes loading effects.

At the higher frequency limit, capacitor size can only be reduced to the point where

internal and stray capacitances become significant. Similarly, the size of the timing resistor cannot be reduced past the point where the IC devices saturate and where power-dissipation limits may, possibly, be exceeded.

To overcome these limitations, there is little that can be done about stray and internal capacitance. However, the timing resistor can be replaced by an active device. This active device will then provide a low-impedance resistive element for the timing network. In practice, we achieve this by selecting an IC from the TTL family. The low-impedance source provided by the specified IC gives a maximum oscillation frequency of 25 MHz when used in conjunction with an 18 pF timing capacitor.

Frequency control is achieved by varying the supply voltage which, in turn, controls the charge current. Output waveform is square with fast rise and fall times (typically less than 5 ns). One disadvantage of the circuit is that output amplitude varies with the control voltage. This limitation can be overcome by feeding the output to another gate or buffer.

The diode network provides sink current when the gate inputs are "low." Base current returns through the diode and resistor to the output. Thus the diode provides the correct output conditions, as though the gates were terminated with other gates.

It was found, experimentally, that silicon planar diodes give best performance in this application. So far, this phenomenon has not been fully explained. The diode interacts with the IC in some way; possibly the diode capacitance cancels the internal capacitances of the gates.

Reference

1. Edward S. Donn, "Wide Range VCO Uses IC," *EEE*, May, 1967 p. 182.

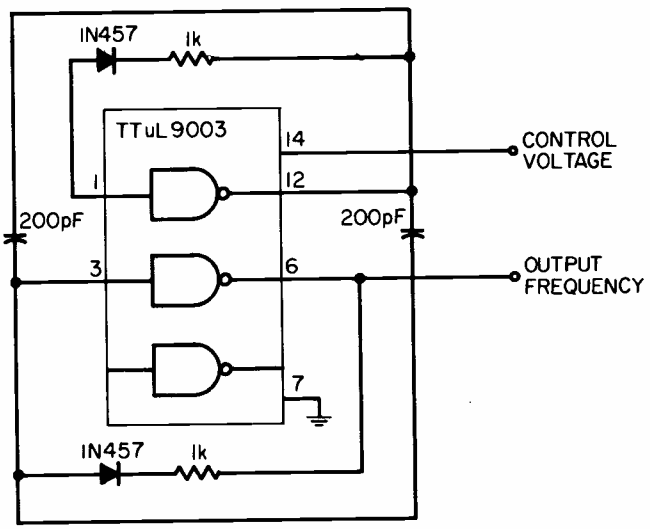


Fig. 1. High-frequency VCO uses cross-coupled IC gates. TTL logic allows oscillation frequencies of 25 MHz or higher.

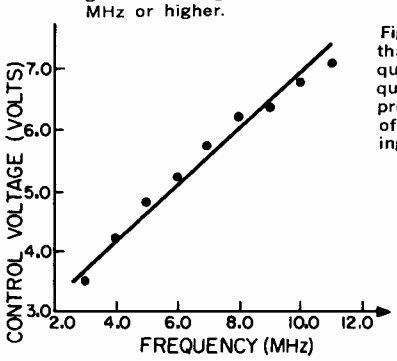


Fig. 2. Linearity is better than 5% of full-scale frequency. Above 5 MHz, frequency is approximately proportional to the product of control voltage and timing capacitance.

Gated delay-line oscillator eliminates range error

CONVENTIONAL CRYSTAL-CONTROLLED clock oscillators have the disadvantage that their outputs can't easily be synchonized with turn-on gate pulses. At the instant of turn on, the phase relationship, between clock signal and gate pulse, is indeterminate. In ranging applications, this uncertainty causes a possible range error of plus or minus one count..

A delay-line oscillator, as shown in Fig. 1, avoids this problem. Clock pulses always start in phase with the leading edge of the gate pulse and stop with the trailing edge. Output is thus coherent with the gate signal. Clock frequency depends on the delay line, and is given by the relationship,

$$f = 1/2d \quad \cdot (1)$$

where f is the frequency in MHz and d is the delay of the line in μs.

Experimental delay-line oscillators have been operated at frequencies as high as 22 MHz. Possibly, operating frequency could be extended to 30 or 40 MHz, but at these frequencies the delay line becomes very short and the values of discrete components start to become very small. With the components shown in Fig. 1, frequency is 5 MHz.

Another advantage of the delay-line oscillator is that it gives a squarewave output. In Fig. 2, the 5-MHz output oscillations are shown at the top and the bottom trace is a negative-going gate signal.

Operation of the circuit is quite simple. As Q_1 is turned on, a negative pulse at the collector travels down the delay line to turn off the base of Q_1. Then, when Q_1 turns off, a positive pulse from the collector travels down the delay line to turn Q_1 back on. Transistor Q_2 provides gating. This stage is normally biased on, to keep the oscillator off. A negative input pulse at the base of Q_2 cuts off the transistor, allowing the oscillator to start.

The delay line for the circuit of Fig 1 is a commercial unit

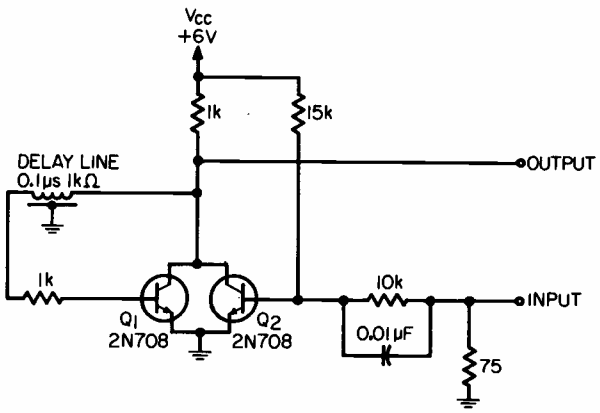


Fig. 1 Simple delay-line oscillator has the advantage that output clock signal always starts in phase with the input gate signal.

manufactured by PCA Electronics. The type DL-1000-0.1-2289 has an impedance of 1 kΩ and a delay of 100 ns. Of course, discrete-component delay lines can be used instead of packaged lines. For a test at 20 MHz, a four-section line was constructed using 2.2 μH series inductors and 3-pF shunt capacitors.

The RC network in the gate circuit is selected to give reliable triggering. With V_{cc} of +10 V, and with the 15-kΩ and 10-kΩ resistors shown, a negative 5-V gate pulse can just turn off Q_2 (or turn on the oscillator). The base resistor is shunted with a capacitor for speed up. This helps Q_2 to switch rapidly. Of course, though the circuit is designed for a 5-V gate pulse, higher voltages can be used.

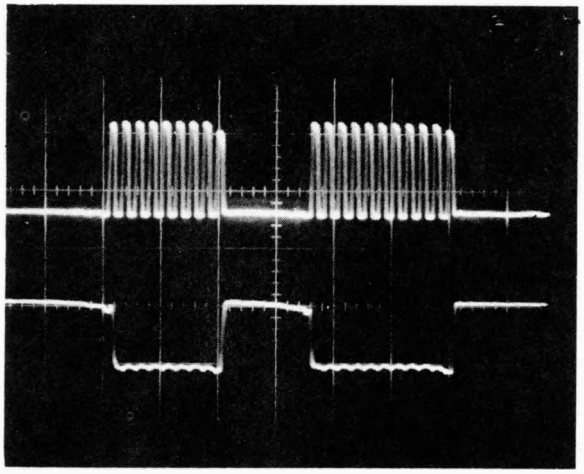


Fig. 2. Typical output (top) and input (bottom) waveforms for a 5-MHz gated oscillator. Horizontal scale is 1 μs/div. Vertical scales are 2 V/div (top) and 5 V/div (bottom).

Improved one-shot multivibrator using ICs only

A PREVIOUSLY published circuit[1] showed how flip-flop ICs could be connected with external gates to form a one-shot multivibrator. But the circuit had a disadvantage. If the time delay through the gates were insufficient, triggering of the flip-flop could be unreliable. An improved circuit shown in Fig. 1 eliminates this problem.

This circuit uses one flip-flop and one or more gates. A falling clock pulse sets the flip-flop after a short internal propagation delay. When the Q output of the flip-flop reaches about 1.5 volts, the gate threshold is reached. After a propagation delay, the gate's output falls, thus resetting the flip-flop. The gate propagation delay allows adequate time for the flip-flop to complete its "set" transition which is already well under way when the Q output reaches 1.5 V.

As shown in Figures 2 and 3, the output pulse of $\overline{Q}$ is narrower than Q. This is a characteristic of the flip-flop circuitry. The $\overline{Q}$ is set directly by the falling voltage on R_D. This setting of the $\overline{Q}$ output is internally coupled to the Q output of the flip-flop to cause it to reset. The time lag required for the Q output to reset after $\overline{Q}$ has set is equivalent to one gate delay. Hence the Q output pulse is the widest.

This circuit will work with flip-flops and gates of most logic families. If, for some reason, the resulting output pulse is not wide enough for the application, width can be increased by adding gates in series with the single gate shown. If an even number of gates is required, then the $\overline{Q}$ output should be used to drive the gates.

Reference

1. Theodore Shepertycki, "IC one-shot needs no external resistors or capacitors," *EEE*, December 1968, p. 102.

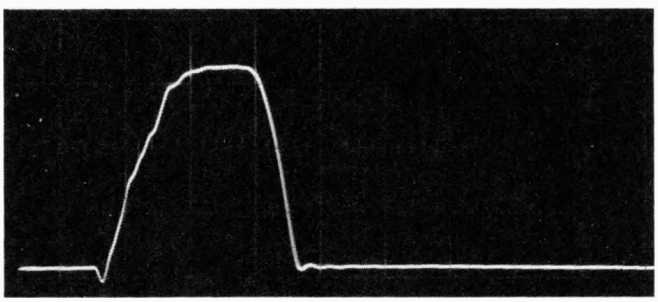


Fig. 2. The Q output of the flip-flop. (Vert. = 1.0 V/cm, horiz. = 50 ns/cm, Vcc = 4.0 V.)

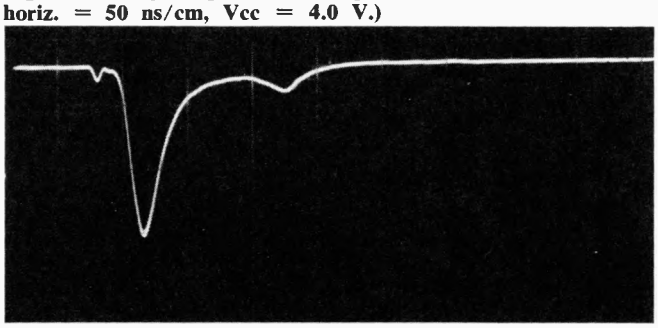


Fig. 3. The Q output of the flip-flop. (same scale as Fig. 2.)

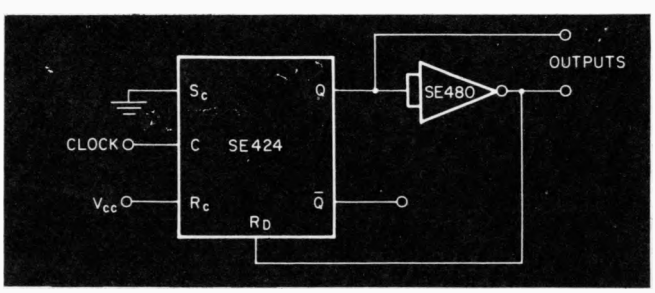


Fig. 1. One-shot circuit uses just one flip-flop and one gate. Circuit triggers reliably for a wide range of gate delays.

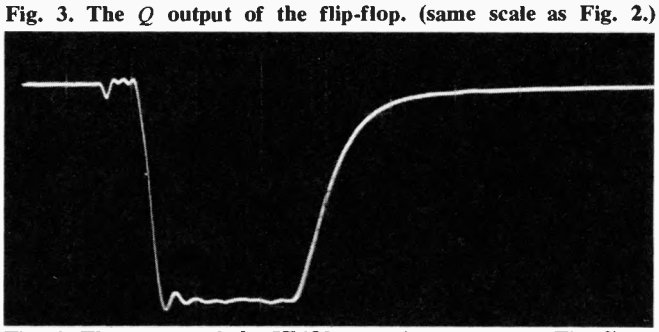


Fig. 4. The output of the SE480 gate. (same scale as Fig. 2)

Low-cost audio oscillator with stable amplitude

A BIFET AMPLIFIER, with a FET and a bipolar transistor in a single package, can be used to build a simple audio oscillator. Because the BIFET provides constant-current output (beyond pinch off), the oscillator has good amplitude stability over a wide range of supply voltages. Changing the supply voltage by 25% or so causes no measurable change in output amplitude.

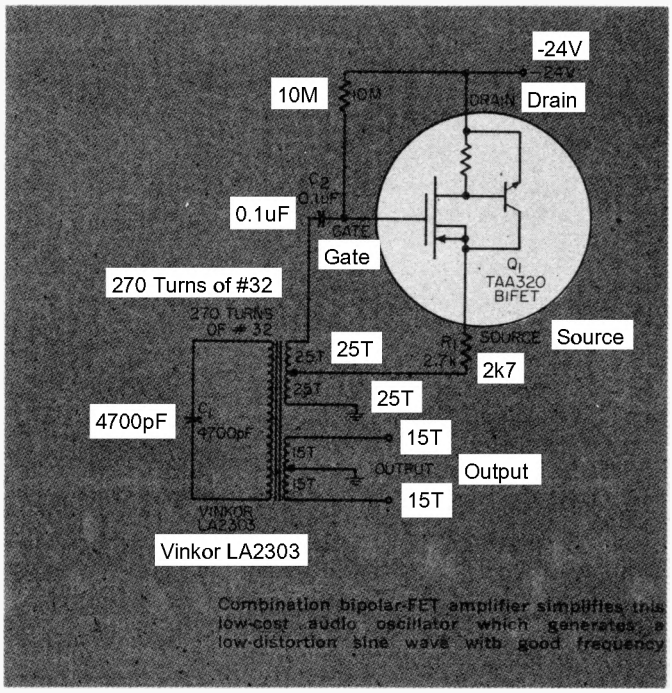
The high gate impedance allows the use of a high-Q tank circuit. Thus output distortion can be extremely low. Output waveform is sinusoidal and, with the 10-kHz circuit shown, harmonic distortion is about 0.1 percent. With a 24-volt power supply, oscillator output amplitude is 1.5 Vrms into a 3 kilohm load.

The Mullard Vinkor assembly is capable of providing Q's of 400 or more. With the specified core and windings, the compact transformer has a tuning range of 10 percent. The oscillator is intended for fixed frequency operation and the transformer is adjusted to compensate for capacitor and core tolerances.

For a practical design, the tank circuit should have a Q of at least 10 and must be tapped to provide some voltage gain between the source and gate of Q_1. Resistor R_1 limits the current through the device. It can be bypassed, though in most cases this is unnecessary.

An attempt was made to measure the temperature coefficient of the amplifier and it appears that for reasonably high-Q circuits it can be ignored.

Possible applications for this circuit include master oscillators and tone generators in electronic organs, or local oscillators for broadcast receivers. The circuit costs more than say a unijunction oscillator, but where a sine wave with good amplitude and frequency stability is required it would seem to be the best choice.



Text states:
Combination bipolar-FET amplifier simplifies this low cost audio oscillator which generates a low distortion sine wave with good frequency

UJT oscillator reconstructs clock signals

THIS CIRCUIT reconstructs a clock signal from data, such as an NRZ signal, that has no accompanying clock. Basically, the circuit consists of a unijunction-transistor oscillator triggered by a monostable multivibrator.

IC NAND gates G_1, G_2 and G_3, plus transistor Q_2, comprise the one-shot. Total cost of these components, together with the timing elements R_3 and C_1 is less than $5. Thus the approach is cheaper than using a packaged IC one-shot. For example, when this circuit was designed, Fairchild's DT-μL951 IC one-shot was selling for around $50. If required, further cost savings could be achieved by replacing the input amplifier (Q_1, R_1, R_2) with the unused gate of the DT-μL946.

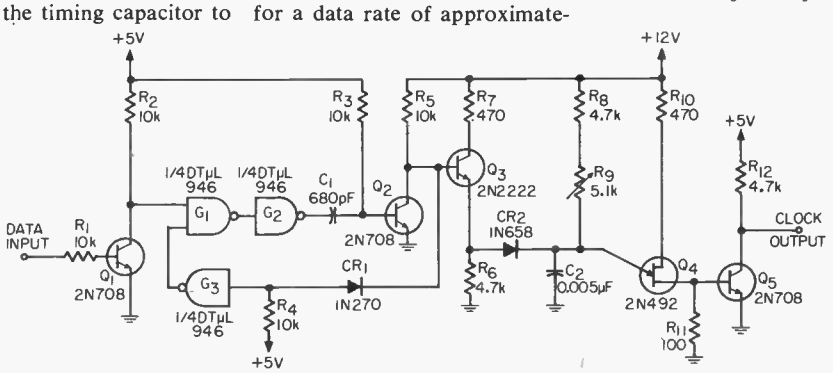
The circuit shown works as follows: A positive-going input pulse saturates Q_1 which fires the one-shot. The output from Q_2 drives emitter-follower Q_3 which charges C_2 to the firing point of the UJT. When Q_4 fires, Q_5 saturates and provides an output clock pulse.

Note that the oscillator is synchronized by charging the timing capacitor. Other circuits achieve synchronization by shorting the timing capacitor to ground; but the method causes timing errors. The effect is different because the period, when charging from ground to the UJT firing point, is not the same as that for the free-running oscillator.

Diode D_1 provides overvoltage protection for NAND-gate G_3. Resistor R_9 should be adjusted to give a frequency slightly below the data rate. The circuit shown was designed for a data rate of approximately 30 kHz.

With the given component values, maximum operating frequency is around 50 kHz. However, maximum clock frequency is determined by the UJT and by the values of the timing elements R_8, R_9 and C_2. Operating frequency can be increased by choosing a different type of UJT and by using a smaller time constant:

$$T = (R_8 + R_9)\, C_2$$



Clock resynchronizer consists of a UJT osillator (Q_4) triggered by a one-shot multivibrator (Q_2, G_1, G_2 and G_3).

Low-frequency sine-wave oscillator

It is often difficult to build low-frequency sine-wave oscillators because of the problem of regulating the amplitude. Shown in Fig. 1, however, is a simple one-hertz oscillator with stable amplitude and low distortion.

The twin-tee network is a one-hertz bandpass filter with approximately unity gain at the center frequency (James J. Murphy, "Electronics," September 16, 1968). Its output is fed through a high-impedance buffer amplifier, A_1, to its input. The gain of A_1 can be chosen so that the amplitude of oscillation is constant (zero damping), or decreases or increases exponentially (positive or negative damping). The gain setting for zero damping is extremely critical.

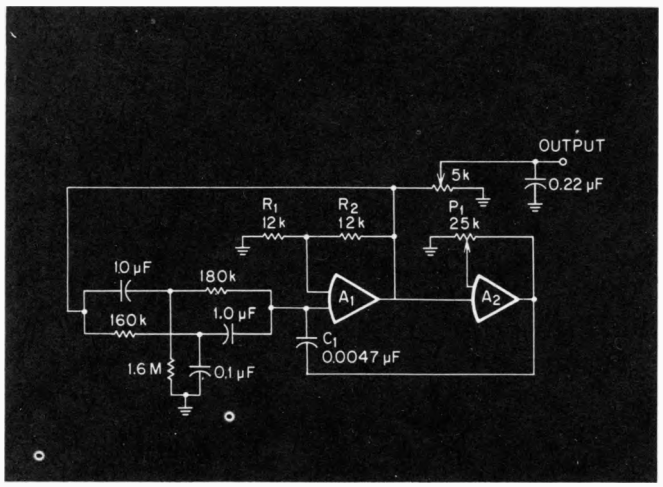


Fig. 1. This 1-Hz oscillator provides high stability, low distortion. The R_1/R_2 ratio must be selected to provide a small amount of positive damping.

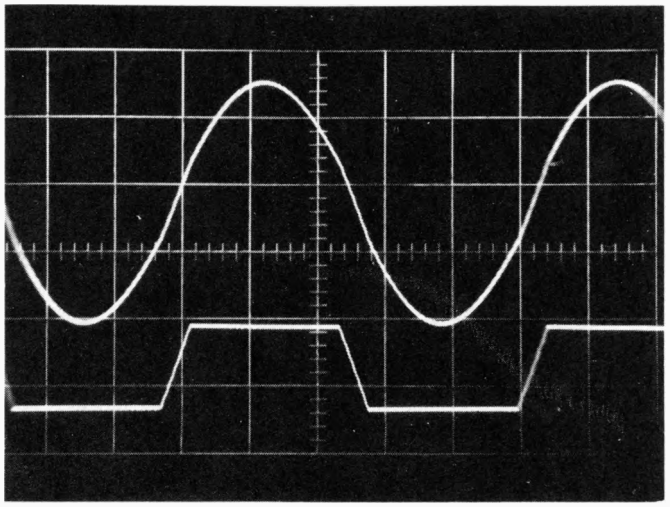


Fig. 2. Waveforms at the output of A (top, 5 V/div) and at the output of A_2 (20 V/div).

This is the usual source of trouble in this type of circuit.

In the circuit shown, the gain of A_1 is adjusted by the ratio R_1/R_2, so the circuit has small positive damping. The oscillations are amplified and clipped by A_2 and fed through a small capacitor, C_1, to the input of A_1. As the output voltage of the oscillator passes upward through zero, the oscillator is given a positive impulse by the leading edge of the clipped sine wave, and similarly a negative impulse is given at the negative zero crossing. Thus the oscillator runs free for most of each cycle, but is "pushed" for a short time each cycle, much like the balance wheel of a watch.

The twin-tee filter must work into a high impedance, so the reactance of C_1 at 1 Hz is made to keep loading negligible. Potentiometer P_1 determines the risetime of the clipped sine wave and hence the magnitude of the impulse to the oscillator and the amplitude of oscillation. ■

A 5000:1 frequency - range oscillator

The common NPN—PNP regenerative-relaxation oscillator (Fig. 1) can be converted into a very-wide frequency-range oscillator (Fig. 2). If R (Fig. 1) is a variable resistor used to continuously change the frequency of oscillation, the range will be limited to one to one and a half orders of magnitude. Q_1 and Q_2 will be forced to stay on if R is made small enough to maintain the required base current in Q_1.

Two different circuits are used to show the flexibility of the design.

By returning the resistor to the collector of Q_1 (Fig. 2) the transistor draws base current from only the timing capacitor C_t. C_t recharges when the transistors are off, to a voltage equal to E_1 plus the base emitter drops of Q_1 and Q_2. The transistors then start into conduction. The transition

(Continued on next page)

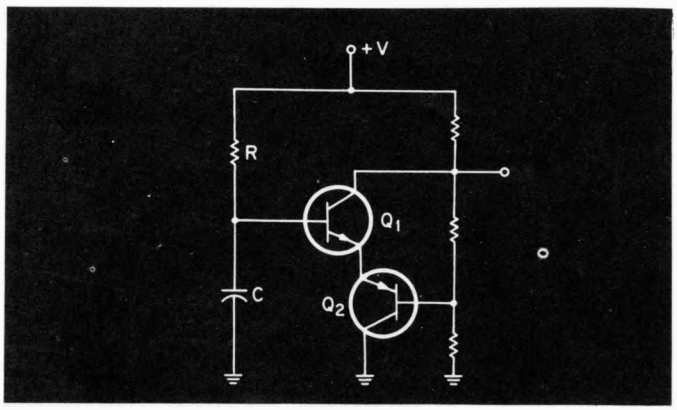


Fig. 1. The basic circuit for a popular relaxation oscillator.

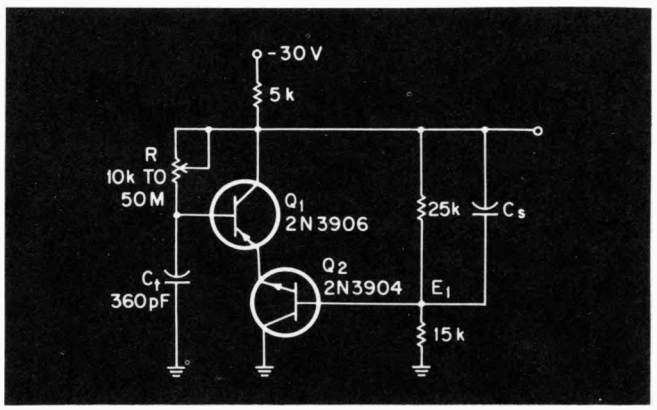


Fig. 2. One modification of Fig. 1 permits a very wide frequency range.

is helped by the speed-up capacitor, C_s. Table 1 shows the period of oscillation for a range of values for R.

R	1/f	E_{out}
10 kΩ	2.6 μs	−21 V
100 kΩ	23 μs	−26 V
1 MΩ	210 μs	−26 V
10 MΩ	2 ms	−26 V
50 MΩ	9.5 ms	−26 V

Table 1. Oscillation period and output voltage for various values of R in Fig. 2.

In the next diagram (Fig. 3), the discharge time of C_s is increased, by placing R_1 in series with the base of Q_1. The 5 to 10% temperature derived instability that is inherent in this modification is quite adequate for many applications. The frequency of oscillation is 2Hz with a 20% duty cycle. The addition of CR_1 allows a higher bias voltage between the base of Q_2 and C_t keeping the size and cost of C_t down. A larger value of R would normally be used but high humidity conditions can affect a conventional 20 or 30-MΩ resistor. ■

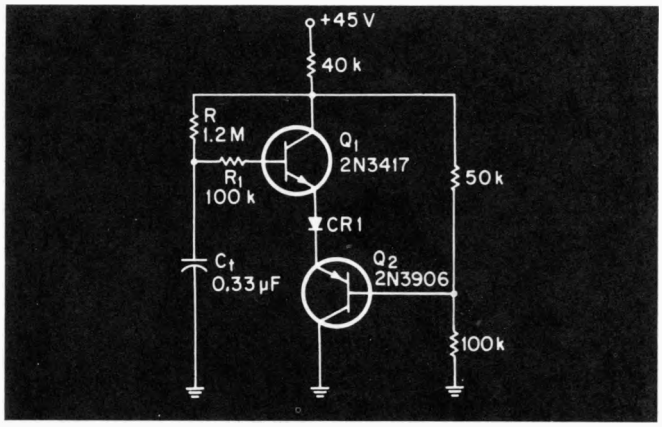


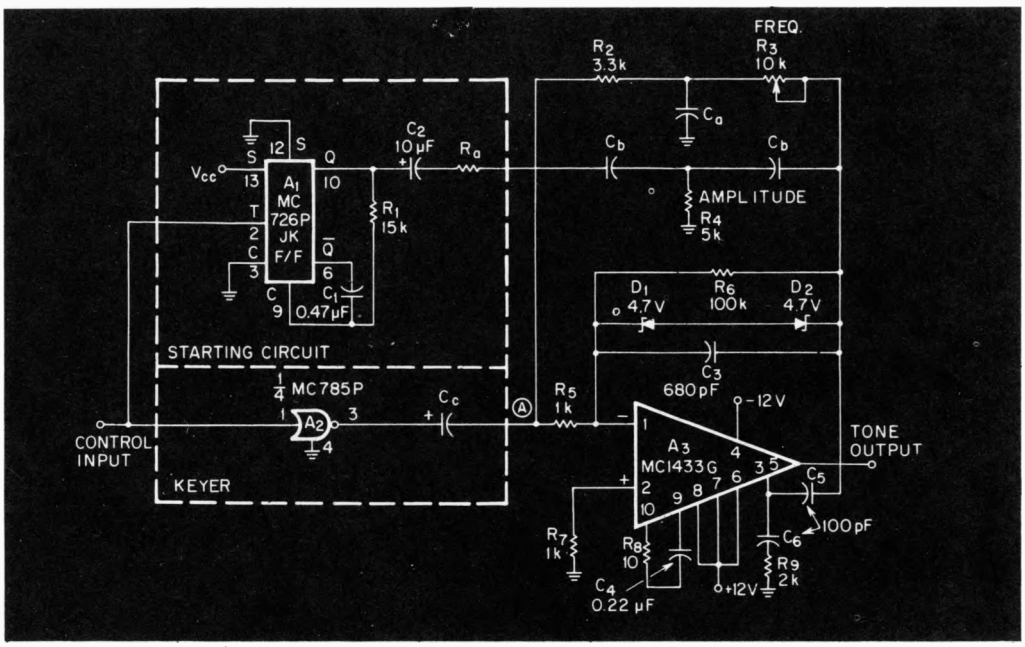
Fig. 3. Another modification of Fig. 1 allows one to generate very low frequencies but sacrifices temperature stability.

LF oscillator with direct digital control

A SUBSONIC telemetry system uses oscillators to generate four tones which are to produce 200-ms bursts under direct digital control. The circuit shown produces low distortion tones at a level of 3 Vrms, developing full amplitude in the first half cycle after turn-on, and producing no transients when starting or stopping.

There are three sections. The oscillator itself consists of an operational amplifier and a twin-T feedback network. The MC785P AND-expander section functions as a keyer, stopping and enabling the oscillator. The MC726P J-K flip-flop functions as a monostable with a 7-ms period and acts as a starter to produce full output, immediately after the oscillator is turned on, by applying a positive pulse to point A.

When oscillating, the twin-T network consisting of R_2, R_3, R_4, C_a and C_b, serves as the feedback network for the op amp. Frequencies are determined by C_a and C_b as listed in the table and R_3 provides precise frequency control. Amplitude is adjusted with R_4 and is set so that zeners D_1 and D_2 are just conducting on peaks. Distortion is slight and output level is stabilized. R_7, R_8, R_9, C_4, C_5 and C_6 are stabilizing components for the op amp.



This oscillator generates a choice of four low-frequency tone bursts under direct digital control. Tones are turned on or off rapidly, with no transients.

Freq. determining components

	C_a (μF)	C_b (μF)	C_c (μF)	R_a (kΩ)
20 Hz	5.6	2.2	100	5.2
28 Hz	3.3	2.2	50	5.6
36 Hz	3.3	1.5	50	10
44 Hz	2.2	1.0	40	12

If the control input goes high, the impedance of the MC785P AND-expander collector goes low, effectively acgrounding point A. The twin-T is then effectively shunted to ground, and replaced by R_3 and R_5 which become input and feedback impedances for the amplifier, producing a voltage gain of 100 but with input grounded. Oscillation dies out within a half cycle. C_c prevents dc offsets from being coupled from the AND-expander to the amplifier input.

If the control input goes low, the AND-expander collector impedance goes high, and oscillation can commence. Without the starting circuit, oscillation builds over a period of a few cycles. The starting circuit, however, applies a positive pulse to point A through C_2 and R_a of approximately 7 ms or 1/4 period of the oscillator frequency. This added energy brings the first half-cycle up to full amplitude. R_a must be adjusted with change in frequency according to the table, as the Q of the twin-T decreases with frequency and therefore the amount of pulse current required to develop full ampli-

tude decreases as frequency is increased.

The flip-flop, C_1 and R_1 form a monostable multivibrator. Prior to a negative-going pulse from the control input to the clock lead, the driving C_D negative. Current flip-flop is cleared and C_1 is charged to approximately 3 V. When the control input goes low, Q goes high, $\overline{Q}$ goes low, from Q through R_1 discharges C_1 through 0 V and continues till C_D is positive, clearing the flip-flop. ■

Crystal oscillator uses logic gates

THE CRYSTAL OSCILLATOR in the figure is simple and stable. Since it uses no reactive-component resonators, it's physically small and easily packaged.

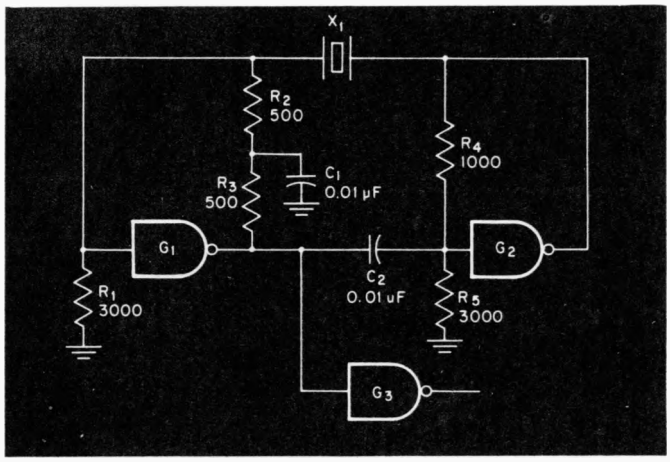
The circuit has two logic gates, G_1 and G_2, biased approximately in their linear region and connected through the crystal to form a positive-feedback loop. A third gate, G_3, buffers the loop signal and delivers the output, which is approximately a square wave with a duty cycle of about 40 percent.

Any of the DTL/TTL families can be used, but the particular gate used should be a buffer type with low output impedance in the high or low state. A 932 buffer was used in the circuit shown.

Frequency stability is essentially that of the crystal, which operates in the series mode on the fundamental frequency (1 to 3 MHz in this circuit). The circuit sees the crystal's series resistance so, at the frequency of interest, the resistance should be low compared with that at spurious frequencies.

The feedback resistors should be chosen to bias the gate input to the approximate center of its 1/0 swing. Over the voltage and temperature range that a particular logic family will see, the feedback should be chosen so that a "1" output results in a "0" input and vice versa, making certain that input-impedance effects are not neglected. The crystal should work into a relatively high impedance, but if R_1, R_2 and R_3 are too large, the gate output can no longer feed back a proper bias to its input and a "1" output can no longer drive the input to "0" or near "0."

Capacitor C_1 eliminates ac from G_1's negative-feedback path while C_2 isolates the G_1 and G_2 dc-bias loops, the ac output impedance of G_1 effectively eliminating ac feedback from G_2's input. ■



This entire crystal oscillator is powered by the nominal 5 V used by the logic gates, but it starts and runs reliably with voltages from 3.8 V to 7 V over −55 to +125°C.

Section 9
INDICATOR & ALARM CIRCUITS

Missing Pulse Detector

AT THIS laboratory there are many different timing pulses and gates in use, all recurring at a 20 pps rate but of durations ranging from 2 μsec triggers to 30 msec gate signals. At times, certain of these are suspected of "skipping" occasionally. A skipped pulse can result in overcurrents and automatic shutdown of large equipment. The cause of the overcurrent remains unknown but if one happens to be watching an oscilloscope presentation of the pulse at the time it skips the occurrence may be seen. Even though it is not too difficult to determine a single skipped pulse from a cathode-ray tube presentation, watching an oscilloscope for such an event becomes quite tedious after a few minutes.

The circuit described herein was designed to accept any of the signals above, without requiring adjustment, and provide a visual alarm if the pulse being monitored is absent for one or more periods ecifically, if the interval between any two pulses eeds 75 msec, the warning light appears and remains on until reset by the push-button switch. For satifactory operation, the input must be a rectangular, positive-going signal of amplitude 10 v or greater. Duration of the signal can be as little as 2 μsec or as much as 40 msec.

Operation of the circuit is as follows: Q_1 is an emitter-follower current amplifier which provides several milliamperes base drive to Q_2 without loading the input signal appreciably. A positive pulse at the input will cause C_1 to discharge through Q_2 and CR_1; when the input pulse terminates, C_1 begins to charge through R_1 and the base of Q_3. Transistor Q_3 discharges C_2, which after a millisecond begins to charge through R_2. The voltage across C_2 continues to rise until it is once more discharged by Q_3; the peak voltage attained by C_2 is hence a measure of the interval between input pulses.

Transistors Q_4 and Q_5 comprise a two-transistor equivalent of the pnpn triode, which has the characteristics of a thyratron. When the voltage across C_2 exceeds 5 volts, Q_4 and Q_5 are turned on and remain on until the emitter circuit of Q_5 is momentarily interrupted by the reset pushbutton switch. The value of R_2 is chosen so that the peak voltage across C_2 is just sufficient to fire Q_4-Q_5 for input pulses spaced 75 msec. The circuit is readily adaptable to other pulse repetition rates by a suitable choice of time constant R_2C_2.

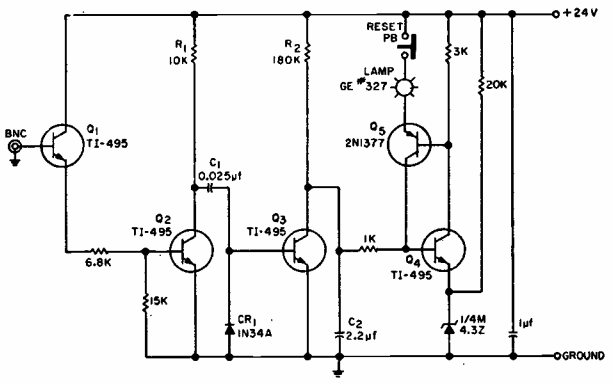


Fig. 1—Detector for giving visual alarm when pulse skips.

Malfunction Indicator

THIS CIRCUIT has been designed to indicate malfunctions, such as high and low line potentials and excessive voltage nulls. It has a sensitivity of 0.5 v over a temperature range of −55 to 125 C.

The indicator, I, is connected so as to show a malfunction under "no-power" condition. Each half cycle, the silicon control switch (scs) anode current is reduced below its holding current, making it insensitive to extraneous firing transients. Thermistor T_1 provides bias temperature stability, and thermistor T_2 compensates the anode firing voltage. Zener 1N966 compensates the cathode firing voltage and allows the scs to be operated with a 0.5 v change in line. D_2 prevents current from flowing through the scs during its "off"

period. All points can be monitored without interference from each other, and the potentials can be either dc or ac of any phase or frequency. D_1 and the 4 μf capacitor can be eliminated, if a dc supply is monitored instead of the ac line.

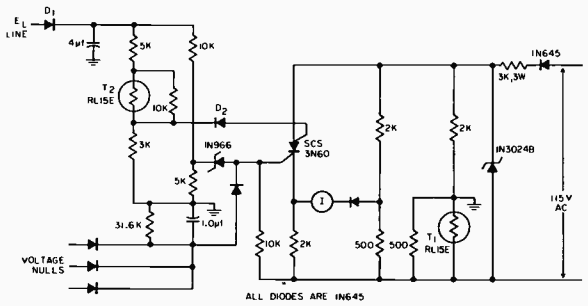
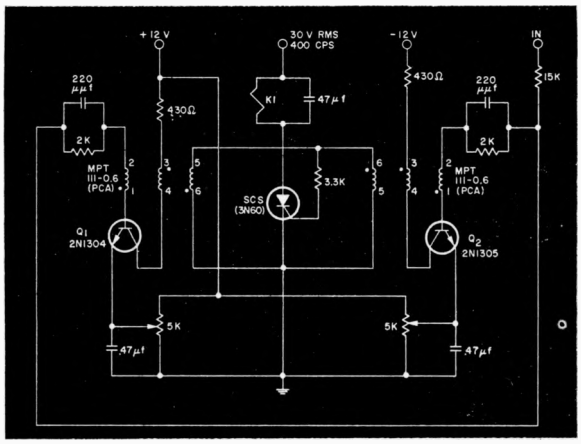


Fig. 1. Malfunction indicator.

High-Impedance Voltage Monitoring Circuit



Complementary transistors Q_1 and Q_2 provide high input impedance for this voltage-monitoring circuit.

in a blocking oscillator circuit with a high input impedance and low hysteresis at the switching limits.

When the input voltage is inside the preset limits, both transistors are back-biased and cut off. The input impedance is then determined by the quality of the base-emitter diode of the transistors. This circuit's input impedance is higher than 5 meg. Silicon transistors would allow a much higher value.

Resistor R_1 is adjusted to allow npn transistor Q_1 to be forward-biased at the desired high-voltage limit. R_2 is adjusted to allow pnp transistor Q_2 to be forward-biased at the desired low-voltage limit.

If the input voltage is outside these preset limits, one transistor will start blocking-oscillator action and provide input signals to the silicon-controlled switch (SCS). This will energize relay K_1 and provide an output indication through its contacts. If a visual indication is adequate, an indicator lamp can replace the relay and capacitor.

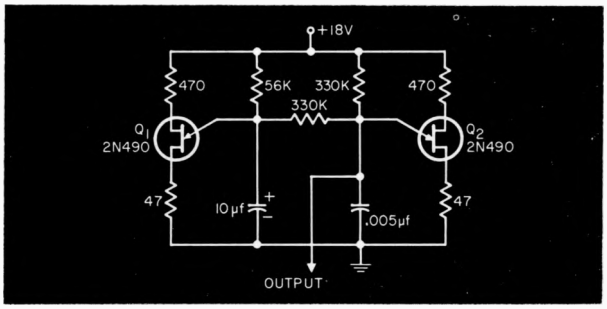
The circuit can be used to monitor a wide range of voltages if collector and bias voltages are chosen to match the input voltage range.

The circuit values and voltages shown here allow monitoring of voltages in the +1-to-6-volt range. At constant ambient temperature, the error is a few millivolts and hysteresis is negligible. For use over an extended temperature range, the base-emitter voltage changes should be compensated. ◆◆

Varying-Frequency Warning Alarm

A VARIABLE-TONE ALARM GENERATOR can be heard easily in noise environments where a single-tone or even an amplitude-modulated tone would not be heard. Here is an oscillator circuit whose output frequency changes continuously.

The low-frequency sawtooth wave on the emitter of unijunction transistor Q_1 is fed through R to the emitter of Q_2 where it modulates the higher frequency oscillator Q_2 and its associated timing capacitor C. The frequency modulation is accomplished by changing the charging current to capacitor C. The varying-frequency tone taken from the



Varying-frequency warning alarm.

emitter of Q_2 can then be amplified and used as an alarm by providing suitable external gating. ◆◆

Pulse-Peak Indicator

THIS CIRCUIT indicates the peak of a fast voltage pulse to within one of several predetermined voltage ranges. These ranges are established by tunnel-diode level-sensing circuits and indicated by a series of "exclusive-or" dual-coil reed relays.

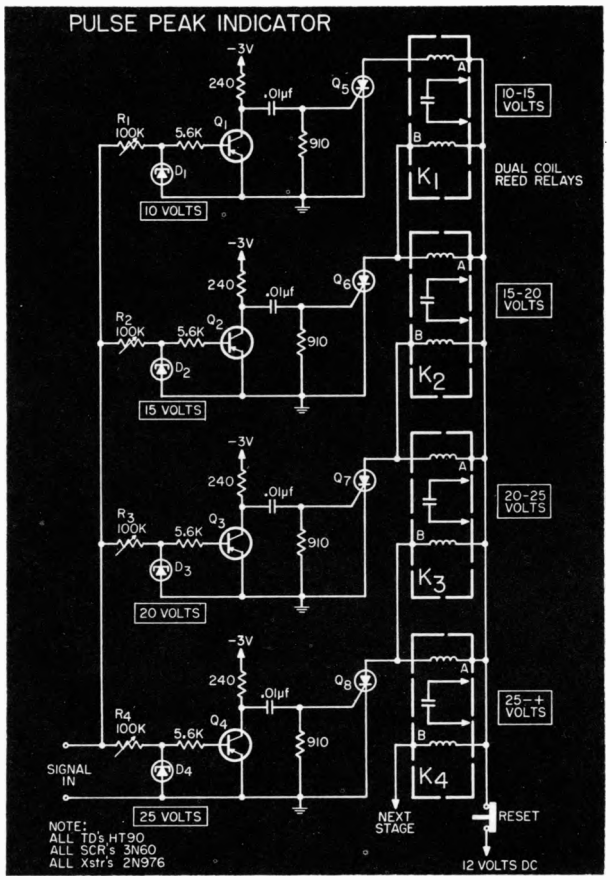
The circuit shown indicates the peak of an incoming negative voltage pulse within one of the following ranges: 10-15 volts, 15-20 volts, 20-25, and 25 volts and above. Minimum switching voltage is 2 v. The circuit is divided into four similar channels.

Assume that an 18-v voltage pulse is applied. The signal is large enough to momentarily switch tunnel diodes D_1 and D_2 to a high-voltage state, but not large enough to switch D_3 and D_4. Hence, Q_5 and Q_6 will be latched "ON."

The contacts of K_1 will be open because both coil A and coil B of K_1 will be carrying current and the coils are arranged so that their magnetic fields are in opposition. The contacts of K_2 will be the only ones closed because only coil A of K_2 is carrying current, but not coil B; hence, no flux cancellation. The contacts of K_3 and K_4 will be open because neither coil A or B in K_3 or K_4 will be carrying current. The reset switch must be operated to turn all silicon controlled switches "OFF" before the next pulse can be measured. The circuit operation is similar for other voltage levels.

The number of ranges may be increased by adding additional channels. The voltage range of one channel can be narrowed by appropriate adjustment of the tunnel-diode level sensing potentiometers. Polarity reversal can be obtained by reversing the tunnel diode, changing to an npn

transistor, and coupling to the anode gate of the silicon controlled switch. Multiple contacts could be incorporated in the reed relay assembly or the single reed relay contact could be used to energize a multiple contact relay.



Pulse-peak indicator circuit.

The tunnel-diode level sensing circuits have functioned satisfactorily to detect the peak of pulses resembling half sine-wave shapes having a 1-μsec width at 50-percent amplitude points. The level adjustment has remained constant to within ± 2 parts per thousand at room temperature for several weeks. ◆◆

Phase Indicator

THIS CIRCUIT provides a simple means of determining the succession of phases of a 3-phase 120-v source used in synchro work. Terminals *A*, *B*, *C* are connected to the three terminals of the source to be checked. If the neon bulb lights, interchange any two leads; the light then extinguishes and **A, B, C** indicate the correct sequence.

If power on any one line is lost, the neon bulb will light. This feature may be useful for monitoring purposes.

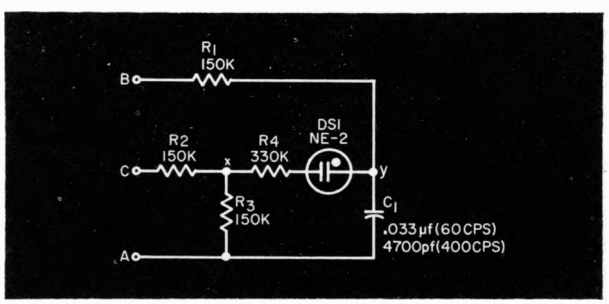


Fig. 1. Phase indicator circuit.

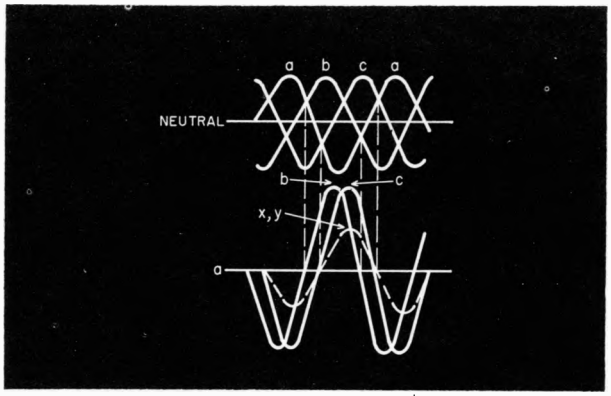


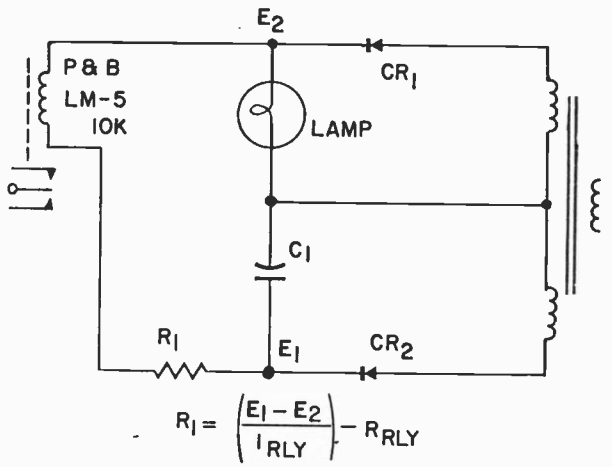
Fig. 2. Three-phase waveforms with phase sequence for lighting neon lamp.

Figure 2 shows the three phases *a*, *b*, *c* with respect to a neutral point. From these waveforms the subjacent waveforms *b* and *c* with respect to *a* are derived. These two waves are seen to be 60 deg out of phase with each other.

If terminals *A*, *B*, *C* of the circuit in Fig. 1 are connected respectively to terminals *a*, *b*, *c*, it will be seen that phase *b*, through 60-deg lag network R_1, C_1, assumes the dashed waveform of Fig. 2 at point *y*, and phase *c*, through attenuation network R_2 R_3, assumes the identical waveform at point *x*, hence there is no potential difference across the neon bulb, which stays unlit. However, if terminals *B* and *C* are interchanged, sine waves at *x* and *y* will be 120 deg apart, and the neon bulb will light. ◆◆

Exciter Lamp Failure Indicator

ON RAPIDLY moving conveyor belts and similar applications employing photoelectric counting or sorting devices, considerable time is lost if the photocell exciter lamp should fail without detection. Many methods of detection of such failure have been developed but the circuit shown is simple, easy to install, reliable, and adaptable to existing circuit configurations.



Circuit for indicating lamp failure of photoelectric system.

A good exciter lamp provides continuity through its filament to hold relay RL_1 closed. Upon failure of the exciter lamp, however, the continuity is

lost through the exciter lamp filament and CR_1 further prevents continuity through the transformer winding. The relay de-energizes and drops out. Suitable devices connected to the relay can serve to warn the operator, stop the operation, or both. Diode CR_2 and C_1 serve as a dc source for the relay. Resistor R_1 limits current through the relay coil.

Tone Decoder, Pulse Discriminating

THIS DECODER is designed to mute a receiver until a continuous 10 sec tone is received, at which time the speaker and a call light will be turned on. The speaker will remain alive and the light on until a reset switch is operated. A short discharge feature is included so that the unit will not respond to a tone interrupted

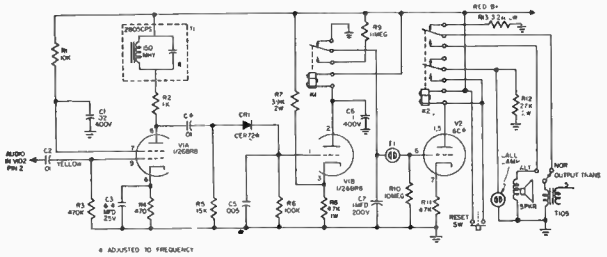


Fig. 1. Pulse discriminating tone decoder.

by dial pulses. This will permit the alerting of a special group of receivers by use of a long uninterrupted tone from standard secode type of equipment. Provision is included to monitor the channel while still allowing the call light feature to be operative. Tone frequency is 2805 cps.

Theory of operation: The decoder must respond to a 10 sec pulse of the proper frequency and discriminate against a series of shorter pulses. Any time the tone is interrupted the time required for the decoder to respond is reset. A series of pulses will not cause the circuit to function. The operation of the circuit is as follows:

Audio is fed to V_{1A}, which is a tuned amplifier. The L-C circuit is resonated at the required frequency. Output of the tuned amplifier is fed to a rectifier which converts the enhanced tone to a dc voltage. This voltage is introduced to the grid of V_{1B}. A tone at the correct frequency will generate enough positive voltage to cause the tube to conduct and activate relay K_1 in the plate circuit.

When K_1 is activated, capacitor C_7 will charge through R_9. Any interruption of the tone will cause K_1 to drop out, discharging C_7, thus returning the charging circuit to zero condition. When the voltage across C_7 reaches the ignition point of the neon bulb, it will fire and place a positive voltage on the grid of V_2. This will cause current to flow in the plate circuit of this tube, activating relay K_2, connected so that it will latch in the "on" condition until manually reset. Reset is accomplished by shorting the coil of K_2, causing it to drop out.

The audio output transformer, T105, is connected to a load resistor in the standby condition. When K_2 is activated, the audio is transferred to the speaker. A monitor switch duplicates the above function so that the receiver may be used normally. The call light will function normally during the time the switch is in the monitor position. The lamp will indicate that a coded signal has been received.

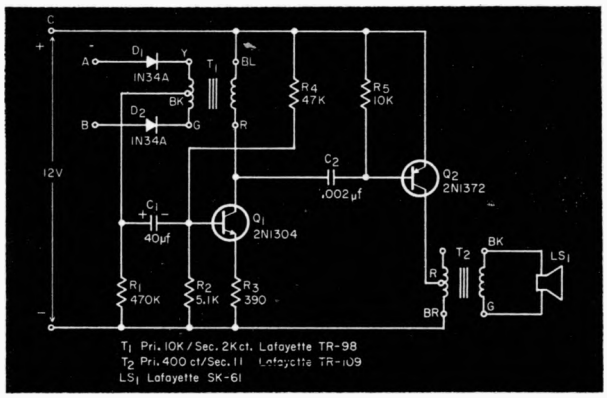
Differential-Voltage or Current Alarm Circuit

HERE IS A DETECTOR CIRCUIT with high sensitivity and stability, followed by an audio amplifier, to serve as a differential voltage or current alarm. The input may be either dc or low frequency ac. The output is a distinctive series of audio beeps or a continuous tone, and occurs only when a selected polarity unbalance is present at the input.

The input stage Q_1 is a squegging blocking oscillator. Under quiescent conditions there is both degenerative feedback through the N winding and regenerative feedback through the P winding, and no oscillations occur. If point B is made positive with respect to point A, diode D_2 is closed and D_1 is open, increasing the degenerative coupling. However, if point A is made positive with respect to point B, diode D_1 is closed and D_2 is open. Under these conditions the net feedback is regenerative, and the stage breaks into oscillation.

The oscillation frequency is determined by the components used, and is about 2 kc for those shown. Capacitor C_1 serves both to isolate the input signal from the remainder of the alarm circuitry and as a base-leak bias capacitor for the blocking oscillator. Its very large value here ensures squegged oscillations at the rate of about 2 bursts/sec. Reduction of the value of C_1 causes Q_1 to operate in the non-squegging mode.

The signal at the collector of Q_1 is coupled to the base of



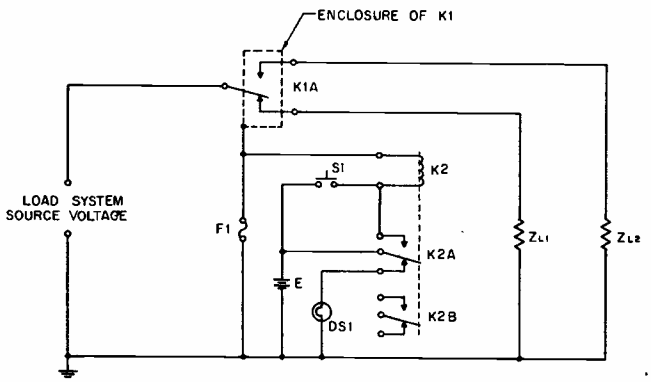
Differential-voltage or current alarm circuit.

Q_2 by C_2. This stage operated approximately class B to minimize Q_2 collector dissipation and maximize loudspeaker output. Under these bias conditions Q_2 tends to squelch output due to common-mode input at D_1 and D_2. The short time-constant of C_2 and R_5 is also helpful in this respect. The direction of the unbalance between points A and B causes the alarm output. This may be reversed by interchanging the input signals applied. The circuit becomes a sensitive current alarm if points A and B are connected across an appropriately small value current-sensing resistance. The differential sensitivity and temperature stability are mainly dependent upon the degree of balance between the characteristics of D_1 and D_2, and the windings of T_1. ◆◆

Relay Arc Failure Detector

CERTAIN RELAY DESIGN configurations, particularly those of the subminiature military type, are susceptible to failure when load current is interrupted and when a potential difference simultaneously exists between the relay frame or enclosure and its contacts. A common application condition satisfying this requirement would be a power control relay with its enclosure electrically connected to the load system ground or neutral. The manifestation of failure is a transient arc discharge between the contacts and grounded parts of the relay, e.g., its header.

In the case of the subminiature military type relays referenced, a 2 amp, 115v rms, 60 or 400 cps resistive load is representative of the type of circuit in which failure may occur. Depending on the degree of load circuit protection, the effect of this phenomenon may range from simple actuation of an overload protection device to complete destruction of the relay. These failures are attributed to random or undertermined causes because of the general lack of recognition of the mode of failure. The circuit shown here provides a positive means of detecting this type of failure.



Relay arcing to case is detected by test fixture.

The Form-C contact K_{1A} and its load circuitry Z_{L1} and Z_{L2} represent a spdt relay under test. Its coil circuit and cycling means are not shown. The enclosure of K_1 is returned to the load system ground through fuse F_1. Detector relay K_2 is a sensitive dpdt relay, chosen such that its coil current is small compared to the rating of F_1. When the spst momentary switch S_1 is closed, K_2 pulls in and is held in by means of the normally open contact of K_{2A}. The battery, E, represents a dc source for the coil of K_2, independent of the load circuit source for K_{1A}, but with a common ground point.

When failure occurs, F_1 opens, de-energizing K_2. The normally closed contact of K_{2A} closes, lighting DS_1, a failure indicating lamp. Auxiliary control of the life test circuitry, such as interrupting cycling and opening the load supply line may be accomplished by means of K_{2B}. With such an arrangement, the test cannot be resumed until F_1 is replaced and S_1 is again depressed.

The circuit shown is for testing only one relay. Multiple testing requires a detector circuit for each relay under test and a suitable arrangement of the auxiliary control contacts such that any one failure will result in the desired control function.

Target Bearing Indicator

A SIMPLE visual indicator device was desired which could be synchronized with a rotating, directional, underwater acoustic transducer to indicate the relative bearing at which the transducer was pointing when a target signal was received. The detecting device provided an ac output of considerable amplitude when a signal was received, which could be used to operate the indicator. Also the transducer drive mechanism had available a synchro output proportional to bearing. This output was used to drive a small servo motor, the shaft of which was directly coupled to the shaft of a standard four-tap sine-cosine potentiometer (Fig. 1).

The detector output was applied directly across the pot, and the four vector voltage (sin, cos, —sin, and —cos) were connected to the four deflection plates of a cathode-ray tube. If the voltage applied to the spot were a dc voltage, the spot would traverse a circular pattern with a radius proportional to the applied voltage.

An ac voltage produces a rotating bar crossing

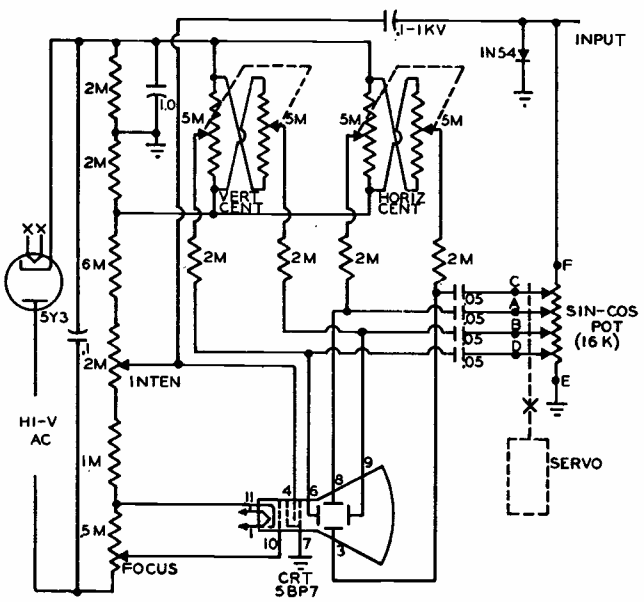


FIG. 1—Servo motor is coupled to sine-cosine potentiometer for target bearing indicator.

the center of the scope, and by diode clipping one half the signal, a pointer emanating from the center can be produced. In operation the spot is adjusted, with no signal, to rest at the center of the screen. With a signal present the signal amplitude is adjusted to produce a line from the center to the

edge of the screen. A further improvement in signal discrimination was effected by using a long persistance (P7) phosphor screen, and coupling the signal to the intensity control grid, an integration of reoccurring signals at the same bearing are more obvious than those signals caused by random noise.

The indicator required was constructed quickly and inexpensively by modifying a standard oscilloscope. The standard mask was replaced by one made of plexiglass having the bearing calibrations engraved around the outer rim. Edge lighting made the calibrations show up quite well.

Overvoltage Indicator

IN AN INDUSTRIAL test system, voltages from zero to 1,500 volts appear on a line. The line is connected to two black boxes, one of which handles voltages from 0 to 150 v, and the other handles voltages in excess of 150 v. It therefore is desired to route the voltages appearing on the line automatically to the black box which is designed to handle it.

The system is shown in Fig. 1. Applying 152 v of any frequency to the line, the pot is set so that the neon bulb fires. This applies a high negative voltage to the grid of the tube which deenergizes K_1 which in turn deenergizes K_2. When the system is off, the high voltage box is connected to the line. After the

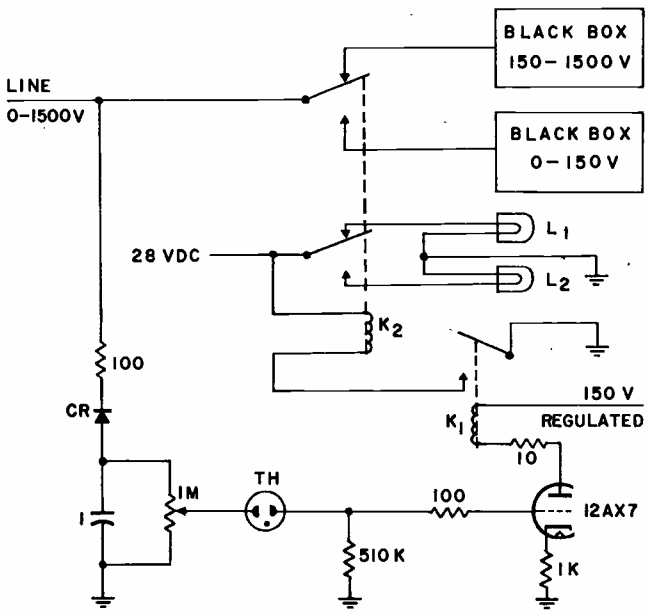


FIG. 1—Circuit for switching voltages from an industrial test line.

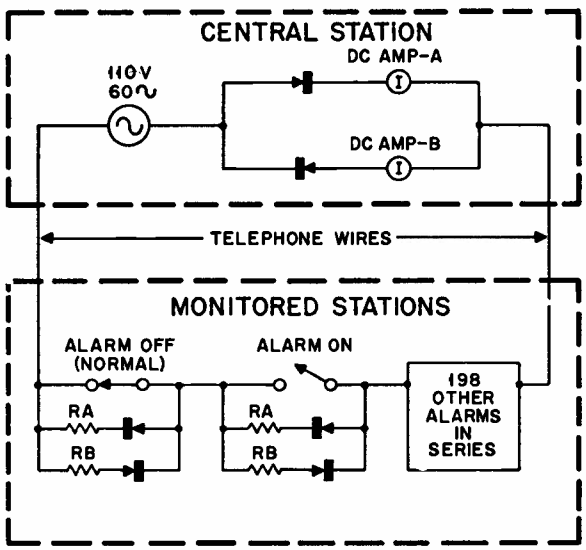
tube is warmed up it switches to the low voltage box, and switches to the high voltage box only when a high voltage appears on the line. If the tube fails, the high voltage box is connected.

This circuit also can be used as an excellent overvoltage protector and indicator.

Rectifier *CR* is a Sarkes Tarzian 126-100-H-Q but any 2000-v low-current rectifier will do. Relay K_1 is a Sigma 4a10,000S. Glow lamp *TH*, an NE68, must be installed in a lightproof box. Alternately, an NE2 or similar type can be used if suitably aged.

Multiple Station Diode Detection System

THIS DESIGN was applied when a night watch service company wanted to monitor distant stations over a limited number of telephone wires. The objective was 200 stations per wire pair. The problem was to detect which particular station was in the



RA AND RB: 200,300,400,600,800
1000,1200,1500,2000
2500,3000,4000,5000
6000, OR 7500Ω

FIG. 1—Use of diodes at central station and monitored stations allows detection of the one of 200 that is in the alarm state.

alarm state. The system did not have to detect more than one alarm at a time since this is a rare situation.

The alarms are all in series and are activated by opening the normally closed switch. A simple approach would have been to place a different resistor in shunt with each switch and have central station note the change in resistance on the outgoing pair of wires. This, however, would require 200 different resistance values. Since there is some variation in the telephone line itself, the method was too critical.

The problem was solved by using only 15 different resistance values. These were connected as shown in the diagram. R_A and R_B could be any one of the 15 values which permits 225 combinations (15×15). The alternating current goes through dc ammeter—*A* and R_A of the *Alarm-On* circuit during one half of the cycle and through dc ammeter —*B* and R_B during the other half cycle. Therefore each ammeter responds to its corresponding resist-

ance and reads one of 15 discrete values during the alarm condition. By checking the combination of readings against a wall chart, the operator at the central station immediately knows which of the 200 stations is activated.

The technique is also applicable to digital transmission over wires. For example, if 10 resistance values were used (instead of 15), then any one of 100 numbers could be transmitted with non-critical automatic equipment detecting and processing this at the central station.

Flying Spot Scanner Sweep Alarm

A RELIABLE system for detecting the lack (or presence) of sweep, intended to prevent burning of a flying spot scanner face phosphor in the event of loss of sweep, is shown in the block diagram of Fig. 1. The system consists of a differentiator-amplifier, a high and low level detector, an inverter, and a summing and blanking generator.

Circuit action is as follows (see Fig. 2). Yoke current variation is differentiated R_1, C_1 or C_2 and the resultant square wave B is fed to Q_1—Q_2—Q_3 amplifier, whose quiescent (zero input) output is adjusted to 10.0 volts by R_2. With any changing yoke current, Q_2 and Q_3 are either saturated or cut off. R_3 adjusts the high Schmitt to pull in when C is greater than 15 volts and R_4 adjusts the low Schmitt to drop out when C is below 5.0 volts. These outputs are summed at F, and amplified and inverted at F' for blanking pulses.

The wave form analysis shows normal (changing) yoke current from t_1 to t_2, yoke current stopping t_2 — t_3, and a blanking pulse rising at t_3.

Gain of Q_1, Q_2 must be increased if R_1, C_1 — C_2 T is decreased to insure reliability at faster alarm times. Alarm time = R_1 C_1 or R_1 C_2 = 10×10^3 $2 \times 10^{-6} = 20$ milliseconds.

All circuits designed at minimum β. Circuit proved stable at temperatures to 50 C. Although higher temperatures were not tested, dc stabilization is more than generous throughout. Note $Q_9 + Q_{10}$ held off by —15, drawing minimum —1b* until driven on by Q_6 or Q_8 R_L. (* — 150 μa).

Input A voltages in the order of +5v, —5v triangular wave were tested but differentiating any slope (with sufficient gain Q_1, Q_2) will cause either saturation or cut off of Q_2, Q_3.

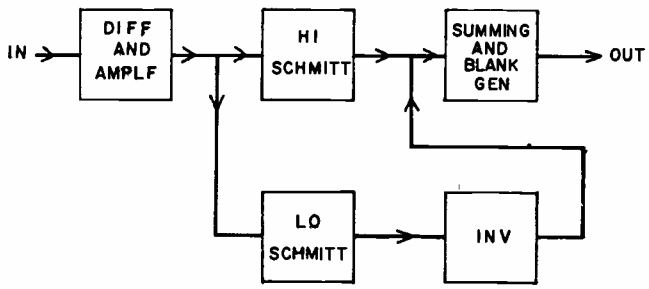


FIG. 1—Block diagram of sweep alarm system.

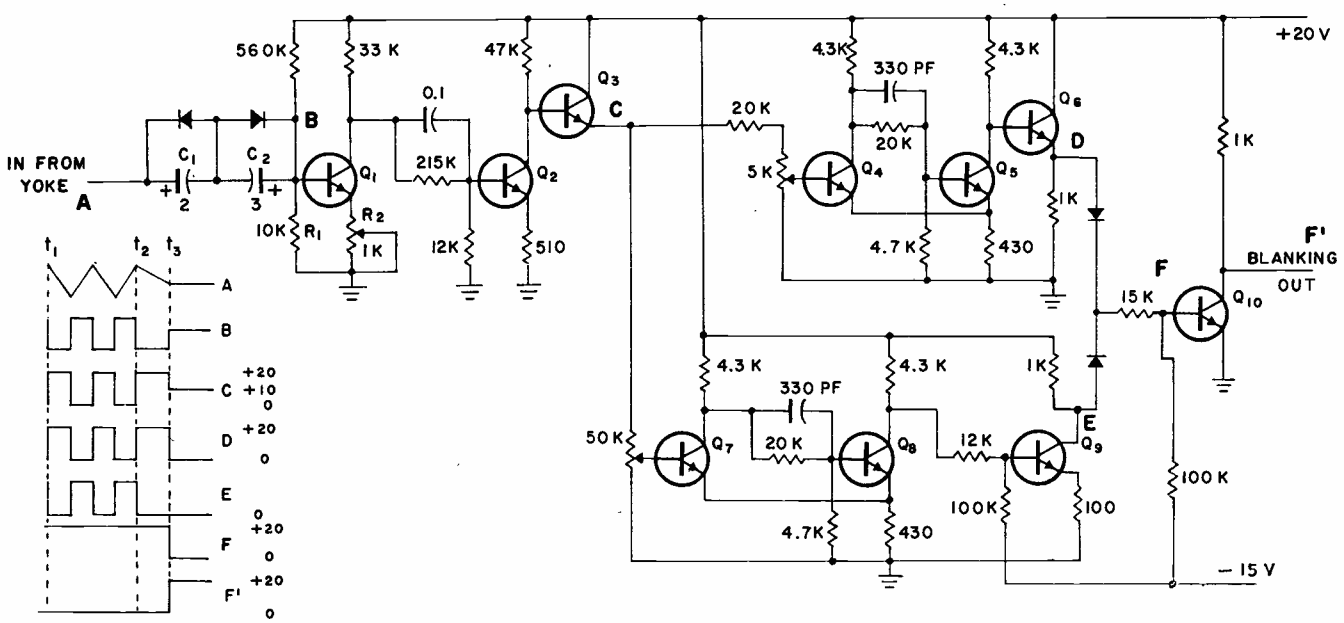


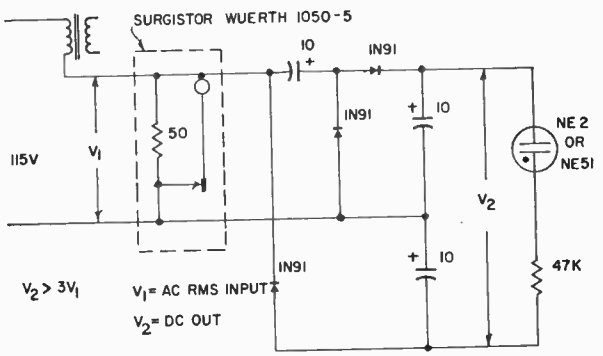
FIG. 2—All transistors of the sweep alarm are type 2N1302 and all diodes are type 1N497. R_2, R_3, R_4 are Bourns 275 Trimits.

Neon Indicator for Surgistor Points

IN A POWER SUPPLY using a protective surgistor there is no way of knowing when the surgistor points are open or closed. This is important since the surgistor may drop as high as 40 volts rms when in series with the power transformer primary.

To indicate whether the points are open or closed, some type of circuit is needed that draws negligible current and gives some indication that the surgistor is dropping line voltage. Another problem is that the surgistor resistance is not constant but changes as it heats.

The circuit shown does the job adequately by indicating with a neon tube when the points are open. This is accomplished by using a voltage tripler to give the neon firing voltage required. Although this circuit has poor voltage regulation, the small current drawn by a neon tube will not affect firing voltage. A series resistor of 47K was chosen for this application; however, this may be altered to compensate for different load conditions of the power transformer. The circuit shown will



Drop of 25 volts in primary circuit actuates neon lamp.

work for a range of V_1 from about 25 to 40 volts rms input which is sufficient for most vacuum tube circuits.

Photocell Lamp Burnout Warning Circuit

THE CIRCUIT ILLUSTRATED in Fig. 1 can be used when photocells are employed to indicate a bad-spot, end-of-tape, or load-point, on a magnetic tape. It should be understood that the tape is processed by a computer via a magnetic tape handler. The photocell watches the tape, and when a mark (reflective spot, hole, etc.) appears, the photocell signals back to the computer indicating the condition or position of the tape. If the photocell lamp burns out, this signal can no longer reach the computer, therefore troubles can develop.

The lamp is rated at 6 v, and is a G.E. type 328 bulb. It can also be operated at 5.3 v to improve life. A dropping resistor can be used by operating from an available 6.3 v ac source. The voltage drop across this

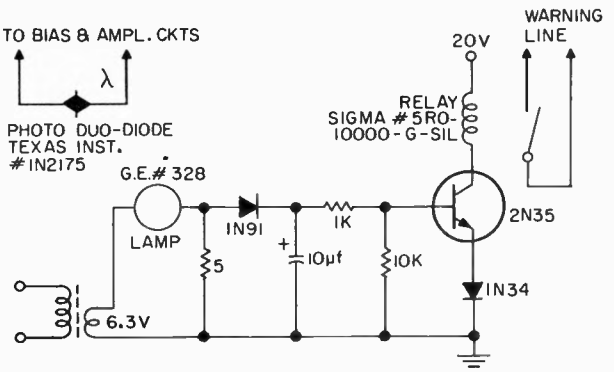


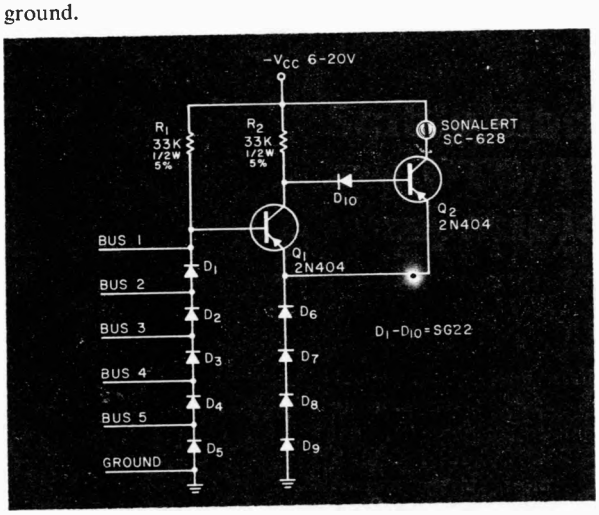
Fig. 1 Photocell lamp burnout warning circuit.

resistor (1.0 v) is rectified, filtered, and is used to drive the base of a transistor. The transistor energizes a relay whose contacts control a warning line. Thus, when a lamp burns out, the transistor can no longer energize the relay and the relay contact gives a warning signal to the computer.

Maximum operating temperature is 65 C.

Short-Circuit Alarm

DURING THE WIRING of today's complicated backplane for computers, where point to point wiring is used, short circuits between voltage buses or a voltage bus shorted to ground because of wiring errors or solder splashes are commonplace. If these shorts are not detected and removed as soon as they occur and are left in the computer to be found after the wiring is completed, many hours of debugging time could result. The circuit described here sounds an alarm as soon as a short occurs between any two of five different voltage buses or any one of the voltage buses to ground.



Short-circuit alarm.

The circuit uses a model SC-628 Sonalert device for the alarm, which oscillates at 2.5 kHz when the circuit is activated due to a short. These units can be obtained in a variety of frequencies.

Proper circuit operation is made possible by the use of the SG22 stabistors. The consistent EI curves for these devices are essential for proper stabilization.

While no shorts occur, Q_1 conducts and Q_2 is off. As soon as a short occurs between any two of the six input lines, Q_1 will shut off and Q_2 will conduct. This causes the alarm to sound until the short is removed.

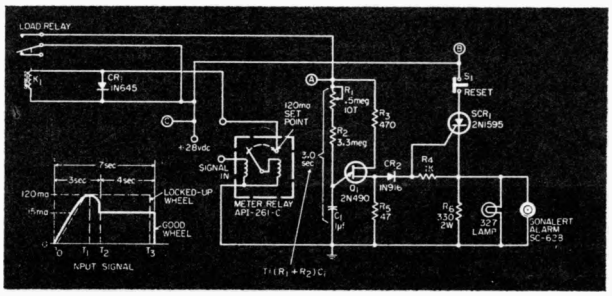
The supply can be any voltage between −6 and −20 v. The higher the voltage, the louder will be the alarm.

With 20 volts for $-V_{cc}$, the current when an alarm is obtained is only 8 ma, which makes this alarm circuit suitable for battery operation. The standby current is about 1 ma.

The alarm circuit cannot be used unless the voltage buses are floating. This does not present a problem because the power supplies do not get installed until after the rack wiring is complete.

Pulse-Level Discriminator and Fault Indicator

THIS CIRCUIT was devised to monitor and indicate gyro-wheel output faults. It sounds an alarm if the gyro wheel is locked up, as indicated by an input signal that remains at a high current (or voltage) level for a period of time longer than a preset interval. The meter-relay upper "set point" is adjusted to 120 ma (the meter relay is a non-locking type). As the input signal reaches 120 ma, (t_1), the meter relay latches and K_1 is pulled in. Plus 28 volts is applied to point A. SCR_1 is held off because its minimum breakover voltage (V_{BO}) is 50 v. Capacitor C_1 charges toward +28 v. If the input drops to 95 ma (good wheel curve), after 3 sec (t_2), the meter relay will move off the set point and K_1 will be de-energized, removing +28 v from point A. The unijunction transistor (Q_1) has not been gated on because the RC time constant, determined by R_1, R_2 and C_1, has been set to 3 sec.



Pulse-height discriminator.

If, however, the wheel locks up, the input signal remains at 120 ma and now is present at point A for a a period long enough (3 sec) to permit capacitor C_1 to charge enough to fire the unijunction Q_1. The SCR will now be gated on by the output from Q_1 and the alarm circuit actuated. At t_3, where the input signal goes to zero, the dc voltage is again removed from point A. The alarm current can now be turned off by pushing reset switch S_1.

Automatic indication of a fault and resetting of the alarm circuit for continuous signal pulses can be achieved by removing the wire from B to C and connecting points A and B together.

Gated Filter and Sample-Hold Circuit

THE BASIC circuit shown in Fig. 1 is a gated low-pass filter. If R_6 is removed, it becomes a sample-hold circuit. In the filter mode, it functions as a unity-gain amplifier with two alternative time constants. These are selected by opening or grounding the gate terminal. In the sample-hold mode it functions as an amplifier, as long as the gate is grounded. If the gate is opened, the output will no longer follow the input, but will be held at the last voltage level. Gating does not cause transients at the output.

Normally, for both circuits, the gate terminal is grounded. Thus Q_5, D_5 and D_6 are biased off. The push-pull pair Q_3 and Q_4 alternately charge and

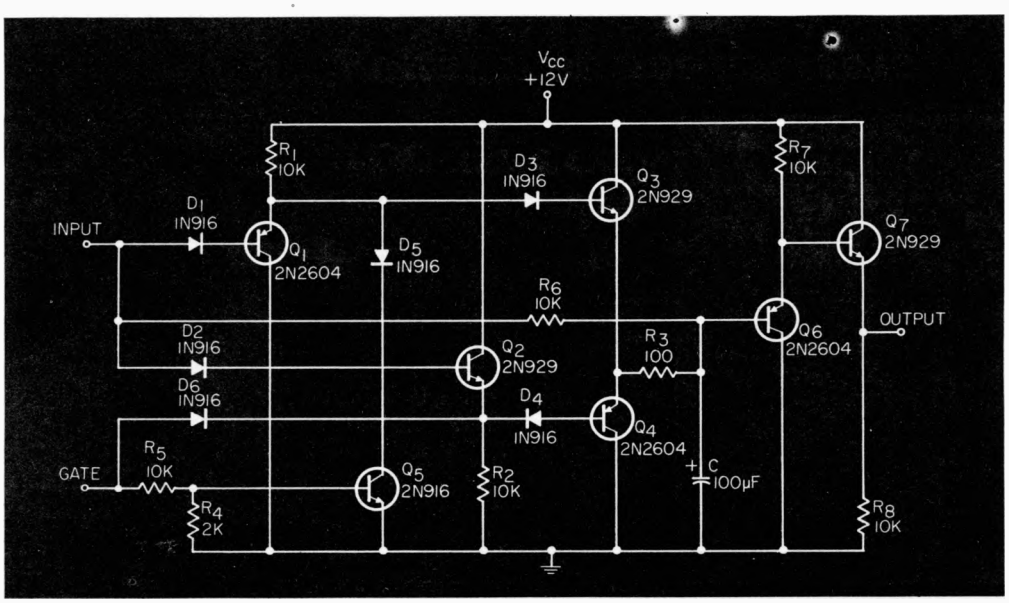


Fig. 1. Basic circuit of gated low-pass filter with two alternative time constants. Removing R_6 gives a sample-hold circuit.

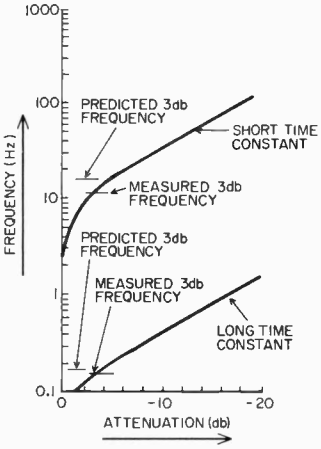


Fig. 2. Frequency response of filter with short time constant (gate grounded) and long time constant (gate open).

discharge capacitor C. The driving impedance caused by these transistors is quite small and the time constant will be almost entirely due to R_3 (assuming $R_6 >> R_3$). The dc level at the emitters of Q_3 and Q_4 is almost equal to the input level since the diode drops of D_1 and D_2 cancel those of D_3 and D_4. Also the base-emitter drops of Q_1 and Q_2 cancel those of Q_3 and Q_4.

When the gate voltage goes positive, Q_5 is turned on, grounding Q_1 emitter and back-biasing Q_3. Thus the emitter of Q_2 is driven positive, back-biasing Q_4. Transistors Q_1 and Q_2 are also turned off. With transistors Q_1, Q_2, Q_3 and Q_4 electrically removed from the circuit, the capacitor is now charged and discharged by R_6.

Normally R_3 is small (fast filter response) and R_6 is large (slow response). Note also that the input impedance of Q_6 should be much larger than R_6. If R_6 is very large (> 20 K) it will be necessary to replace the Darlington circuit Q_6 and Q_7 with a FET circuit to achieve the required impedance at this point.

The frequency responses for the two filter time constants are shown in Fig. 2. The cutoff frequencies are determined by the following equations:

For the short time-constant ($R_6 >> R_3$),

$$f_{3\,dB} = \frac{1}{2\pi}\left(\frac{1}{R_3 C}\right)$$

(assuming that the input impedance of Q_6 is much greater than R_3).

For the long time-constant (R_3 gated out),

$$f_{3\,dB} = \frac{1}{2\pi}\left(\frac{1}{R_6 C}\right)$$

Combination lamp driver and failure indicator

WHEN INSTRUMENT panels display critical information, some sort of failure indication is often needed — to show if information is missing due to lamp failures. The circuit of Fig. 1 provides automatic indication of lamp failures. It consists of a two-stage Darlington amplifier with a lamp as a load at the collector of the output transistor. Directly across the incandescent lamp is a neon indicator. If the lamp fails, the neon indicator is no longer shorted by the lamp filament and will therefore fire. Holding current for the neon indicator is supplied by a separate 60-volt line via R_2. Diode CR_1 isolates the neon voltage supply from the one lamp driver drives several lamps.

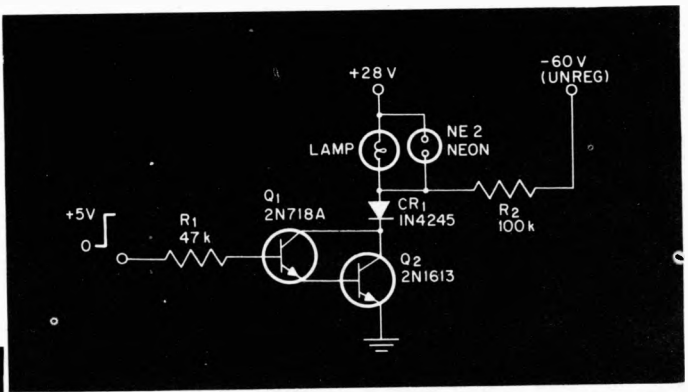


Fig. 1. In this simple lamp driver, the neon indicator provides failure indication for the incandescent lamp.

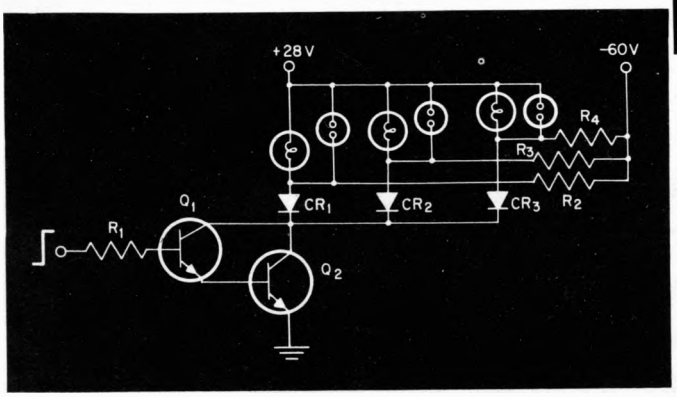


Fig. 2. The same basic circuit can provide independent failure indication for several lamps as shown here.

The component values for the circuits are quite flexible and mainly depend on the line driver.

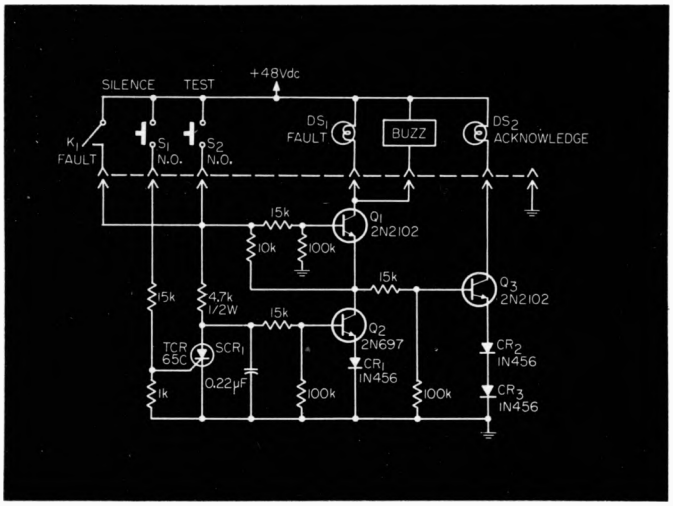
An extension of the same circuit, as shown in Fig. 2, can provide independent failure indication in situations where current ratings of the lamps. The values shown will handle almost all 28 V lamps and can be readily adapted to lamps of other ratings.

Fault Alarm Circuit

TO BE TRULY comprehensive, a failure indicator should give audible as well as visual alarm. The operator must be able to silence the alarm manually.

The circuit shown performs all these functions. When the buzzer is silenced, a second lamp lights to "acknowledge" the operation and confirm that the fault condition still exists. The input to this circuit is a pair of normally-open relay contacts, which close in the event of equipment failure.

The circuit works as follows: Initially all transistors are "off" until a fault occurs and contact K_1 closes. This turns on Q_1 and Q_2. Transistor Q_2 may



conduct momentarily, but not long enough to light the "acknowledge" lamp. The collector voltage of Q_2 reverse-biases Q_3 to hold it "off." The voltage drops of diodes CR_1, CR_2 and CR_3 give suitable bias conditions for Q_2 and Q_3. Both the "fault" lamp and the buzzer remain energized until the fault is removed or the "silence" switch is actuated.

The SCR is ready to be fired since anode voltage is present but not gate voltage. Closing the "silence" switch fires the SCR. This turns off Q_2, silencing the buzzer and turning off the "fault" lamp. Transistor Q_3 now conducts, lighting the "acknowledge" lamp. This lamp remains on until the fault is cleared.

Fault alarm circuit has buzzer and lamp. Switch S_1 silences the buzzer and transfers indication from DS_1 to DS_2.

Low voltage transistors drive neon indicators

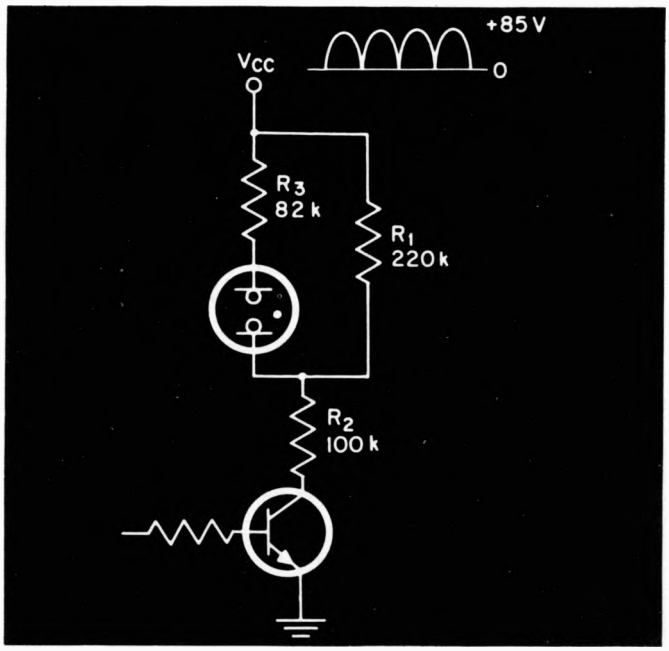
WITH TWO resistors added to a neon-drive circuit, inexpensive low-voltage silicon transistors can be used to light neon indicators. Neons are long-lived and inexpensive, requiring far less power than incandescent lamps and generating less heat. The high voltage required by the neons does not pose a problem when the associated equipment is line-operated.

In the circuit shown in the figure, R_1 and R_2 are selected so the drop across R_2 is within the Vcb rating of the transistor. The drop across R_1 is less than the striking voltage of the neon.

With the base of Q_1 at ground, Q_1 and the neon are off. A positive potential applied to the base saturates Q_1 and effectively grounds point A, turning on the neon. Collector current will be small, and determined by R_1, R_3 and Vcc. An ideal supply for use as Vcc is a full-wave rectified but unfiltered dc. The return to zero of Vcc twice each period will insure turn-off of the neon.

The supply is 85 volts peak derived from 120 volt center-tapped transformer. With the circuit values as shown the maximum collector voltage is 27.5 volts. The 82-kΩ resistor gives fair brightness for an NE2E bulb.

Any transistor with a collector rating of 25 volts will be adequate at Q_1. In fact, transistors with 15 volt ratings have been used quite successfully for Q_1. If the transistor suffers breakdown, the large collector impedance limits the current. Since the supply voltage is pulsating, the condition will be removed 120 times a second.



Low-cost, low-power neon indicator drive circuitry.

There is no reason this circuit can not be used to drive Nixies or other commercial neon type displays. The transistor input is compatible with most IC logic levels.

Automatic back-up lamp circuit

A WIDE variety of equipment depends upon a light source for operation. If the lamp fails, damage can occur. Such equipment usually provides lamp failure circuits, which may activate a buzzer or alarm to notify the operator of the failure, and indicate that replacement of the lamp is warranted.

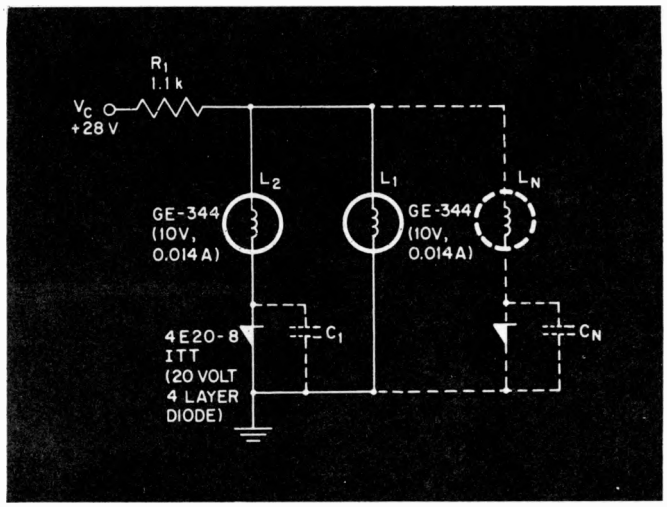
The circuit in the figure provides for an automatic switch-over to a backup lamp; letting the system operate normally if a lamp failure occurs during operation.

The lamp L_1 is activated when power (+28 V) is applied. Lamp L_1 is activated first because of its low cold resistance to ground as compared to the resistance path of L_2 and the 4-layer diode D_1. In this way resistor R_1 has a voltage drop across it of 18 volts and the voltage across L_1 is 10 volts, well below the 4-layer diode threshold.

If L_1 burns out, the circuit current flow is interrupted and the voltage goes toward +28 V, the 4-layer diode breaks-down through the resistance of L_2. D_1 latches because of the sufficient holding current due to the current path completed through the diode, and L_2 lights with approximately the same intensity as L_1. The location of the lamps is such that L_2 provides the circuit functions of L_1. When L_1 is replaced it again assumes control.

The same technique, shown dashed, can be used to provide multiple redundancy to such circuits. More lamps and 4-layer diodes can be added as required. For independent operation of such multiple circuits, a small capacitor may be included across the 4-layer diodes. In any case, the inherent differences in each diode device would probably avoid the necessity for additional capacitors.

The circuit can be adapted to operate with other (different rated) bulbs, or with multiple filament lamps using common electrode connectors in the same glass enclosure. ■



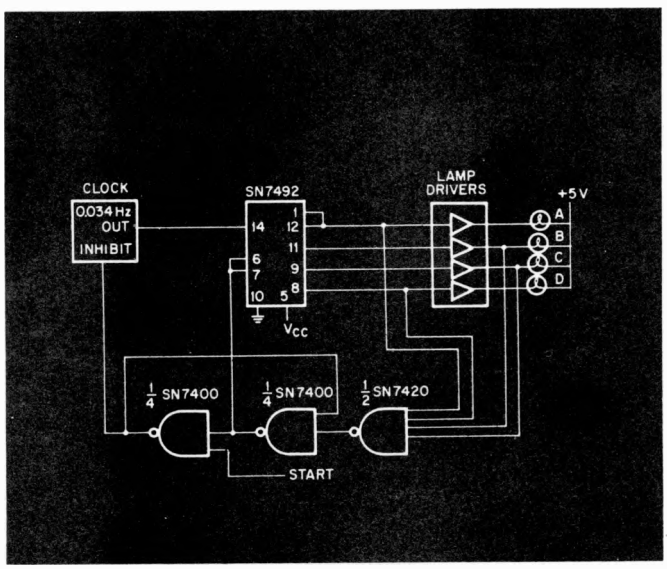
Automatic lamp back-up circuit using 4 layer diodes.

Simple, low-cost time indicator

A SIMPLE, low-cost time indicator can be obtained using four lamps, a slow rep-rate clock, lamp drivers and TTL decoding logic.

In the circuit shown, lamp D lights three minutes after a negative pulse is applied to the "start" lead. This lamp stays lit for 30 seconds. Lamps A, B and C light during the three-minute time cycle in a binary sequence and are used as an indication of total cycle time.

When a negative pulse occurs at "start" the TTL flip-flop removes ground from the 0.034 Hz (30 sec) clock and grounds the reset of the SN-7492. Every 30 seconds the clock fires, making a change occur at the lamps. When the SN7492 goes to a seven count, the TTL logic resets the flip-flop inhibiting the clock. This event lets the counter-reset go high, thus resetting all the lamps. Note that the seven count occurs so rapidly that it is not seen on the lamps. The binary sequence could be decoded but its direct usage provides circuit simplicity, a greater number of lamp changes and a valuable attention-getting feature. ■



In this circuit, lamps A, B and C light in a binary sequence during a three-minute time cycle.

Section 10
COUNTING & TIMING CIRCUITS

Transistorized Intervalometer

DURING a development program for rocket borne instrumentation, it became necessary to produce a signal delayed from an initiating signal. Space for the device was limited and stability over a wide environmental range was required.

Acceleration and shock loads of at least 50 G were anticipated, with temperature ranges of minus 10 degrees F to at least plus 120 degrees. Supply voltage variations of plus or minus 25 percent would be encountered. An output signal of a minimum of 10 milliseconds capable of supplying 20 amperes to a very low resistance load was specified.

Immediate considerations indicated that a transistorized monostable multivibrator (or Schmidt trigger type) would require the minimum of components.

A basic concept of the system is shown in Fig. 1

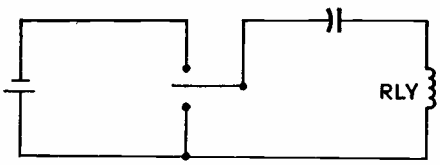


FIG. 1 — Basic circuit for switching polarized relay.

and consists of a power source, a two-position switch, a capacitor, and a polarized relay. With the switch in the upper position, the capacitor is charged through the relay coil resistance, however, the relay does not operate since the charging current is chosen to be improper polarity.

Moving the switch arm to the lower position discharges the capacitor through the relay causing it to operate for a period of time dependent upon the capacitor's value and the voltage of the power source. Extension of this concept replaces the switch and relay with transistors and adds biasing and a feedback path to reset the circuit following an input pulse. Voltage regulating and clamping circuits complete the design.

Figure 2A shows the final circuit of the delay section. Transistors Q_1 and Q_3 are npn types 2N78 and Q_2 is a pnp type 2N44. D_1 and D_2 are 5-volt zener diodes and D_3 is a 9-volt zener. The power source is a battery of ten HR-1 Silvercells, whose nominal voltage, after charging, is approximately 18.7 v.

Capacitor C_1 and resistor R_5 provide the delay determining components and the output pulse is derived from the circuit by differentiating the trailing edge of the pulse at the collector of Q_1.

Three points exist at which the circuit may be conveniently triggered. As is common with monostable systems, each has a minimum triggering level. At the base of Q_1 an input signal of about 0.25 volt positive will trigger the circuit. At the collector of Q_1, a somewhat larger signal is required, while at the collector of Q_3, still a larger signal must be applied. The trigger point at Q_3 was chosen for the circuit, due to the relatively low apparent impedance and the higher trigger level, which must be above that maintained by D_3. In the triggering system, resistor R_9 serves to prevent C_2 from holding a charge of such polarity as to prevent repetitive triggering. R_8 limits the current through the combination when the switch is closed.

In the untriggered state, transistors Q_1 and Q_2 are nonconducting, and Q_3 is conducting to the limit allowed by resistor R_6, because of the positive bias applied by R_5. Diode D_2 and resistor R_4, adjusted for about five ma through D_2, serve to regulate the bias level applied to the base of Q_3 to a greater degree than that afforded by D_3 alone. Capacitor C_1 is raised to the voltage level set by the parallel leakage path of Q_2 collector-emitter and D_1, its

other terminal being near ground through the base-emitter of Q_3.

Upon being triggered, Q_1 conducts heavily, being limited by R_1, thus grounding the base of Q_2 causing it also to conduct heavily. This switches the positive lead of C_1 to ground, as in Fig. 1, in turn biasing Q_3 off. The voltage at the collector of Q_3 rises to near the regulated supply level, a portion of the rise being coupled to the base of Q_1, thus holding the entire circuit in a stable condition until sufficient of the charge on C_1 has leaked off to permit the positive bias to again cause Q_3 to conduct.

In a circuit depending on the time constant of a capacitor and resistor, it is important to maintain the charging levels and charging and discharging resistances to maintain repeatability. Ideally these resistances would be zero or at least remain constant, placing the majority of the repeatability figure in the stability of the prime time determining components. When transistors are incorporated in such a circuit, a large part of the possible variation, with specific transistors, is due to the I_{cbo} change due to temperature. In the particular circuit, with D_1 removed, this I_{cbo} change in Q_2 causes sufficient variation in the charge on C_1 to place operation outside the specified limits. Since the collector-emitter of Q_2 is in series with R_2 and I_{cbo} changes appear as voltage changes applied to D_1, its regulation action effectively swamps I_{cbo} variations. Additionally,

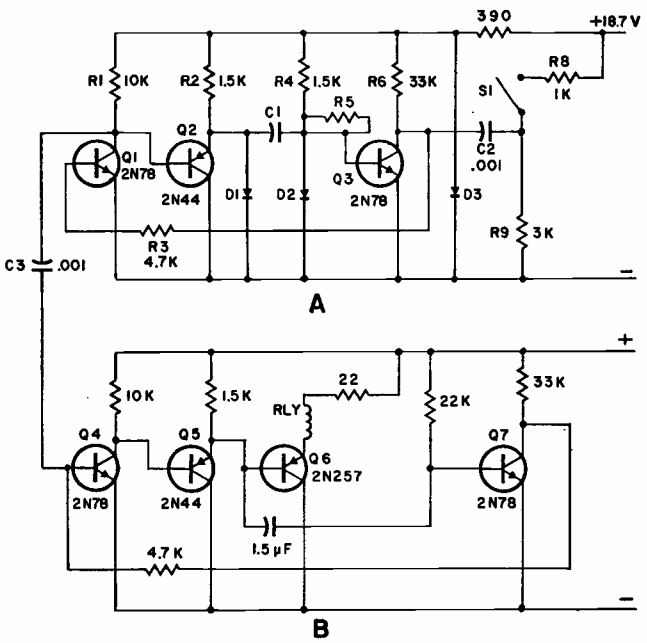


FIG. 2—Complete circuit of transistorized intervalometer.

since Q_2 conducts heavily, several milliamperes, the load swings primarily to D_2 during Q_2 cutoff, relieving D_3 of wide load changes. The collector circuit of Q_1 provides an area of additional temperature compensation if desired, by inserting a Fenwal RB 33L1 thermistor in series with approximately 5000 ohms resistance, in parallel with R_1. As temperature increases, reducing thermistor resistance, an increased positive bias is applied to the base of Q_2, lowering the effects of I_{cbo}.

Capacitor C_1 has demonstrated relatively insignificant effects on the performance with changes in temperature. High quality Mylar 5-µf 10-v capacitors have been incorporated as well as solid tantalytic units with no degradation within the limits of the tests performed. No resistor in the units manufactured (more than a dozen) was chosen beyond the ten-percent stock unit. With C_1 of 5 µf and R_5 approximately 80 kilohms, a time delay of about 200 millisec is obtained. Increasing R_5 to about 300 kilohms increases the time interval to about one second. Considerably longer intervals have been obtained using as high as 300 µf for C_1. It is not possible to increase R_5 to much above 470 kilohms due to malfunctioning of the system.

Switch selected resistors may be assembled for obtaining a number of prechosen time delays. A trimming potentiometer should be included in series, to effect time interval correction at the shortest period of time interval. A one-megohm pot in parallel with C_1 provides a satisfactory high end trimming control.

Use of a pot in parallel with a high quality capacitor may appear to degrade the performance of the capacitor, but explains the lack of significant difference in performance with capacitor types, since variations in leakage resistance with temperature govern the time interval to a greater extent than changes in absolute capacitance.

The basic circuit was modified as shown in Fig. 2B. to provide a means of obtaining the required high current and output pulse duration. Since the requirements specified only a minimum duration of output pulse, a time interval of about 35 millisec was chosen and all temperature compensation dispensed with.

Not having a relay of suitable sensitivity at hand, transistor Q_6 was added as an emitter follower to drive the relay. The relay used was a P and B SC11D type, with a 33-ohm coil resistance, and the 22-ohm resistor in series with the coil was utilized to limit the maximum current through the coil. For lower current requirements, the load could be connected directly in place of the relay coil. While this relay is overloaded, tests showed that it would interrupt a 35-ampere load, at an application period of 75 millisec for at least 50 operations.

The final assembly group of units were thoroughly tested for conformance to the requirements. Pulse to pulse repeatability was normally within five parts in 10,000 and day to day repeatability was easily within the limits of plus or minus one per cent of the selected time interval. All units were expended in the program.

The basic circuit generates pedestals of good rec-

tangular configuration at various points, which may be utilized as gates in other applications. A series of the basic units could be connected as frequency dividers, by adjusting sequential units for a time duration of one count less than the division period required, since no output can be obtained following the initial input pulse, until the circuit has reset.

Counter Uses Complementary Transistors

DESIGNED for switching at a 1-mc rate, the counter shown in Fig. 1 uses transistors in complementary pairs so that only one stage draws current from the power supply. The reason for this is that the ON

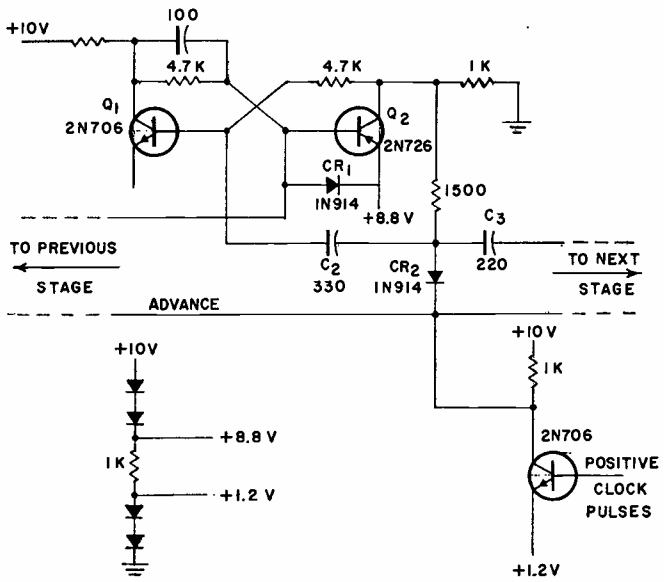


FIG. 1—One-mc counter with complementary transistors.

stage has both transistors conducting; the OFF stages have both transistors cut off. In an application where the ON state is caused to move from stage to stage, the average power dissipated by the counter is that of a single conducting stage, and is independent of the number of stages.

Another unique feature of the circuit is that it prefers the OFF state. When the supply voltage is turned on, both transistors are biased off and remain off until the stage is turned on by the advance pulse. There is then no transient overload on the power supply resulting from clearing the counter.

In the OFF state, no current flows in the circuit, and point 1 in Fig. 1 is at zero volts. The advance pulse is negative, dropping from +10 volts to approximately +1.2 volts, when the trigger amplifier is pulsed into saturation. Diode CR_2 remains reverse biased and inhibits transmission of the advance pulse.

In the ON state, Q_1 and Q_2 are both in saturation, and point 1 is at approximately +8.8 volts. During the advance pulse, CR_2 conducts and current flows through the triggering capacitors C_2 and C_3. The

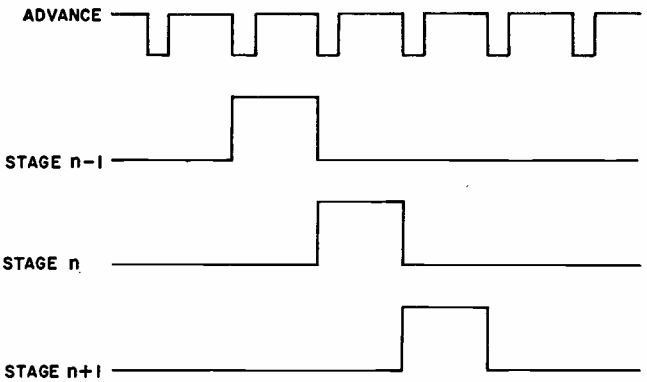


FIG. 2—Outputs of adjacent stages are shown with reference to the advance or shift pulses.

npn Q_1 is turned off, and the pnp Q_2 of the next stage is turned on. The switching is regenerative in both stages, and as shown in Fig. 2, results in a shifting of the ON state down the counter with each advance pulse.

The circuit rise time is less than 0.02 microsecond; fall time is 0.03 microsecond. The circuit was designed and tested to operate over the ambient temperature range of —55C to +150C.

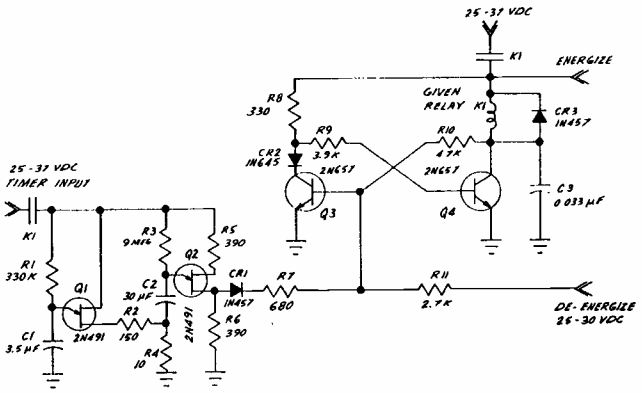
Transistor Time Delay Switch

THIS transistor switch is designed to operate a given missile-borne, 4-pdt, dc relay with the following requirements. The initially energized relay is to be de-energized four minutes after voltage appears at the output of a sensor device. The relay has two spare sets of contacts, a coil resistance of 350 ohms, and controls a 25-ampere circuit. The control unit for the relay is to operate from a voltage source of 25 to 37 volts dc and consume no power after relay drop out. The control circuit may be considered in two sections: a medium-power transistor switch consisting of Q_3 and Q_4, and a four-minute timer of Q_1 and Q_2.

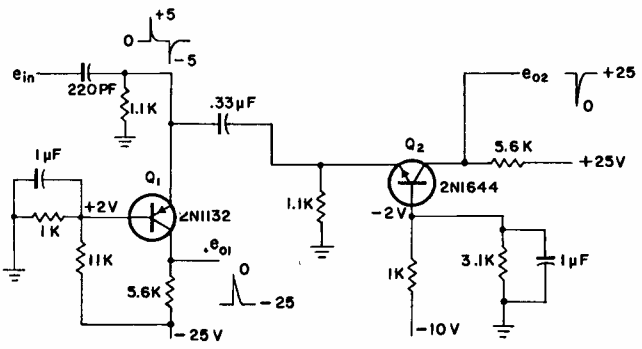
Initially, voltage is applied to the ENERGIZE terminal of the switch section. Current is withheld from the base of transistor Q_3 by the relay inductance and the capacitance of C_3. Current flows through resistors R_8 and R_9 to the base of Q_4, switching the transistor and energizing the relay. Transistor Q_3 remains off because the low emitter voltage of Q_4 is too low to supply much base current to Q_3 through R_{10}.

When the timer supplies a current pulse to the base of Q_3, the transistor saturates and its low emitter voltage then reduces the current through R_9 to Q_4. Transistor Q_4 turns off and the voltage across the relay is reduced below the minimum hold-in voltage.

Power is removed from the circuit by normally-



Circuit of transistor time delay switch.



Differentiating circuit for narrow pulses.

open contacts of relay K_1. This transistor switch is unique in that the relay coil is an integral part of a flip-flop and the inductance provides turn-on of the proper transistor. Turn-off is accomplished by a current pulse from the timer section.

Time delay is provided by the unijunction transistor circuit of R_3, C_2, and Q_2. To obtain the four-minute delay without using an extremely large capacitance value for C_2, the resistance of R_3 is too large to supply the required peak-point emitter current of transistor Q_2.

For the circuit to function, the peak-point emitter current value must be exceeded to trigger Q_2 to the negative resistance region of the emitter voltage versus emitter current characteristic curve. However, a unique innovation is employed which enables one to use the extremely large resistance value of R_3.

By adding the pulser circuit of transistor Q_1, a low frequency voltage pulse is developed across resistor R_4 which is in series with the timer capacitor C_2. When C_2 is charged to the peak-point emitter voltage, transistor Q_2 is triggered by a voltage pulse on R_4. Capacitor C_2 then discharges a current pulse to transistor Q_3 which trips the switch as described earlier.

Differentiating Clipper Circuit

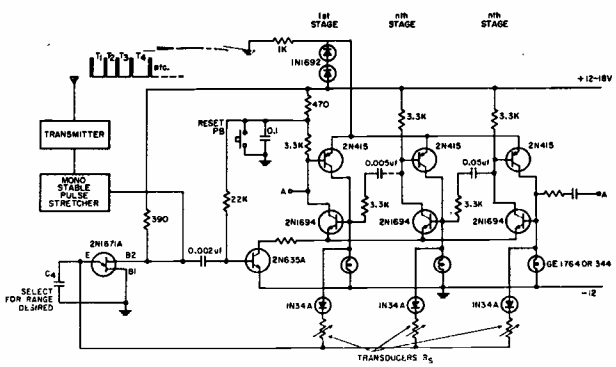
IN MANY TIMING applications, differentiating a narrow pulse in the order of 0.1 μsec presents the problem of admitting into the circuit hash and random noise impulses. The circuit shown eliminates this difficulty, using relatively few, inexpensive parts. In addition, the leading and lagging edges of the incoming pulses are separated and may be used to set the timing of logic circuits or pulse width discriminators.

The circuit is composed of two transistors, Q_1 and Q_2, which are reverse biased through bleeder networks according to their respective pnp or npn configuration. Transistor Q_1, which has the differential input applied to its emitter, is biased at the base with +2 volts, thus preventing negative spikes from passing. At the same time it allows only pulses greater than 2 volts to be conducted, keeping noise and other pulses of smaller magnitude out. The threshold level may be set as high as the reverse bias for the transistor will permit (for 2N1132 $V_{BER} = 5$ volts). A positive pulse of 5 volts at the input results in a voltage swing of nearly 25 volts at the collector.

Transistor Q_2 works similarly but in the negative direction. This transistor, a 2N1644 common base configuration, is biased at —2 volts, thus permitting only pulses more negative than 2 volts to pass. The pulse width obtained from a 0.1 μsec pulse will be 50 nsec because of the differentiator action.

Inexpensive Pulse-Time Telemeter

THIS CIRCUIT telemeters the output of a resistive transducer. Two basic circuits, a unijunction pulse generator, and a multistage ring counter are used in the manner described. The resistive transducers are sequentially switched into the pulse generator through steering diodes from the collectors of the pnp transistors of the ring counter. Each time the unijunction fires, the ring counter advances one step thus placing the next transducer and the fixed timing capacitor. The pulses from the unijunction are stretched to a suitable value for modulation of a transmitter. The data



Pulse-time telemeter.

are thus transmitted as a pulse train with spacing between pulse proportional to transducer R values.

Light bulbs are used as collector loads to provide a visual inspection of the circuit operation. A reset button turns the system on. This circuit has been bench tested and will be used on a high altitude balloon flight in the near future for telemetry of ambient pressure, differential pressure, and various temperatures.

Sample and Hold Circuit with Bilateral Charging

IN PROCESSING PAM data it is often necessary to increase the energy content of a series of low-duty-cycle, amplitude-modulated pulses that result from demultiplexing a particular channel of a PAM pulse train. To accomplish this, a sample and hold circuit with bilateral charging has been designed. This circuit (Fig. 1) was designed specifically for sampling and holding 0- to 5-volt information received via a sampled-data telemetry link, and it is currently in use in PAM-FM and PAM-FM-FM ground stations.

Upon command, the sample and hold circuit charges the holding capacitor to the value of the input data on pin 18. The voltage on the capacitor is then held until the next sample, at which time the holding capacitor is charged to the new value of the input data. This process repeats for every command received on pin 13 and the output data is taken from the holding capacitor via an isolation amplifier. In this manner the circuit functions as a demultiplexing gate and as an amplifier.

To prevent source loading, the input impedance at pin 18 is relatively high, approximately 100K ohms, in the off state. In normal operation many of these units are connected in parallel, allowing a large number of channels to be demultiplexed simultaneously. The input impedance of the unit in the on state is somewhat lower than 100K ohms; however, this presents no problem because normally only one unit is in the on condition at a given time.

The output impedance of the bilateral charging circuit in the off state is approximately 1 megohm minimum without the selection of matched transistors for Q_7 and Q_8. Selecting transistors Q_7 and Q_8 results in an extremely high output impedance, thus large discharge time-constant of the holding capacitor, because their leakage currents can ideally cancel each other and none would flow into or out of the holding capacitor.

The unit has high peak charging current capabil-

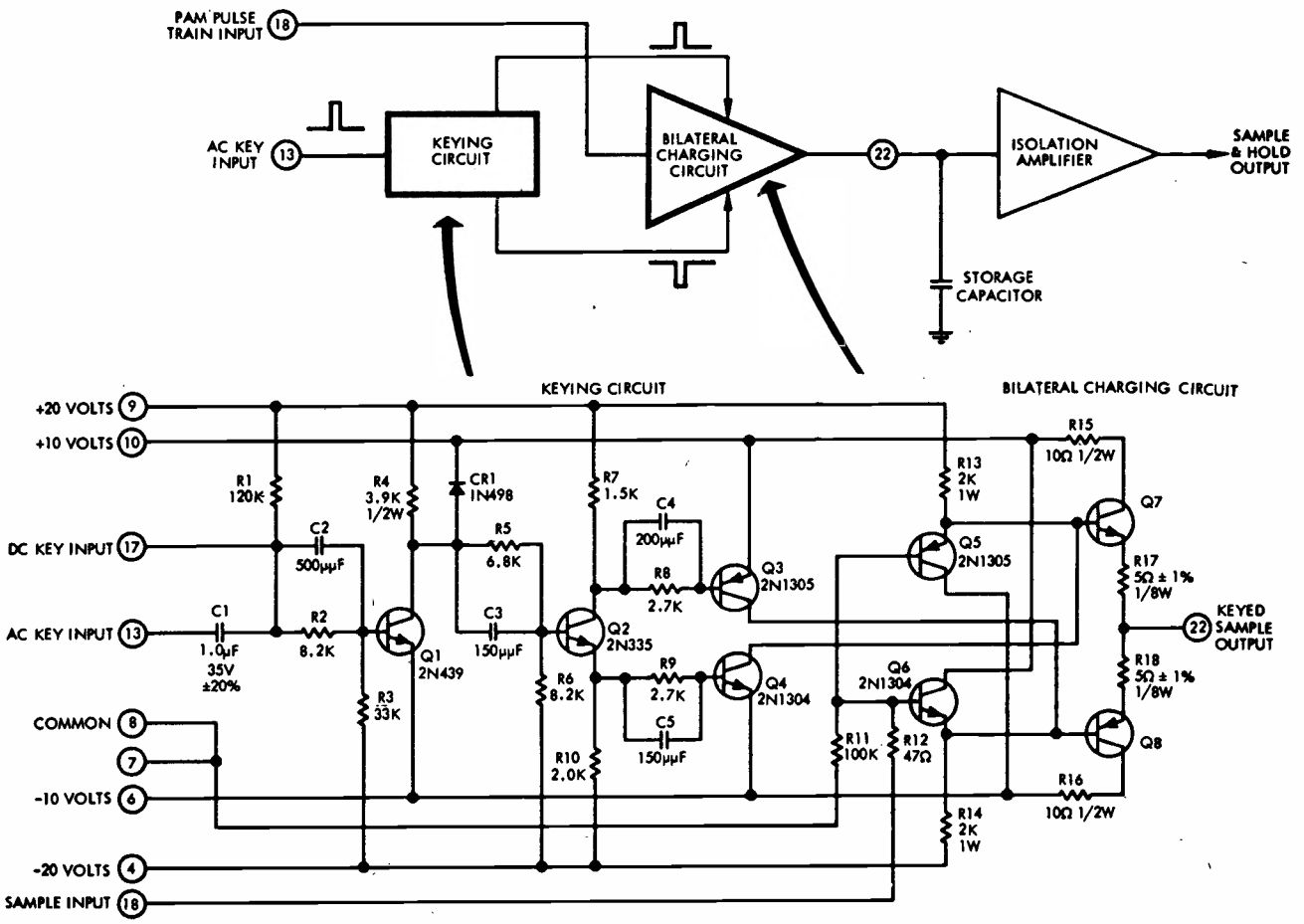


FIG. 1—Sample and hold circuit with bilateral charging. Transistor Q_7 is a 2N1304 and Q_8 is a 2N1305.

ities, in the order of 200 ma, and essentially all of the current is supplied by the 10-volt supplies. This puts hardly any current requirements on the source and it is effectively used only to catch the voltage on the holding capacitor through a near unity voltage gain, high current gain amplifier.

The main advantage of this charging circuit is that it is bilateral and can deliver peak currents of 200 ma to the holding capacitor or accept peak currents of 200 ma from the holding capacitor. In this manner the voltage on the capacitor can be changed rapidly in the positive or negative direction, thus eliminating the conventional dump circuit and making it possible to generate a true non-return-to-zero waveform.

In the charging, or on, state, the input data to be sampled on pin 18 is transferred by the two emitter follower transistors Q_5 and Q_6 to the output bilateral charging transistors Q_7 and Q_8. After the holding capacitor has been charged, the bilateral charging circuit is in a balanced state.

The voltage rise from base to emitter of Q_5 equals the voltage drop across R_{17} and the base to emitter voltage drop of Q_7. Also, the voltage drop from base to emitter of Q_6 equals the voltage rise across R_{18} and the base to emitter voltage rise of Q_8. In this balanced state a small bias current is allowed to flow through Q_7 and Q_8, thus eliminating any dead zone of the circuit and helping to keep the dc offset from input to output, pin 18 to pin 22, equal to zero or very nearly zero if the four transistors are not exactly matched. In this balanced bilateral arrangement, rapidly changing data in the range of —5 volts to +5 volts can be stored on the holding capacitor. Transistor Q_7 will be turned on hard while it is charging the capacitor in the positive direction and transistor Q_8 will be turned on hard while it is discharging the holding capacitor in the negative direction.

To deactivate the bilateral charging circuit, the keying circuit provides two low-impedance paths to the 10-volt supplies. A normal dc key input voltage on pin 17 would be —10 volts for the off state and zero volts with respect to common for the on state. If the ac key input is being used on pin 13, a 10-volt positive pulse will suffice for the on state and an absence of a pulse keeps the bilateral charging circuit in the off state.

In the off state, Q_1 of the keying circuit is turned off due to the bias on its base. The off condition of Q_1 allows base current to flow into Q_2 via R_4 and R_5, thus saturating Q_2. The saturated condition of the phase splitter allows both Q_3 and Q_4 to saturate, since the emitter of Q_2 is more positive than the base of Q_4 and the collector of Q_2 is more negative than the base of Q_3. The low-impedance paths to the 10-volt supplies are provided by the saturated transistors, Q_3 and Q_4, that actually deactivate the bilateral charging circuit. When Q_3 saturates, the base of Q_8 and the emitter of Q_6 are pulled to +10 volts, thus back-biasing the base to emitter junction of both Q_6 and Q_8. Similarly, when Q_4 saturates, the base of Q_7 and the emitter of Q_5 are pulled to —10 volts, back-biasing the base to emitter junction of both Q_5 and Q_8. In this manner all four transistors of the bilateral charging circuit are turned off, providing a long discharge time-constant for the holding capacitor and a high input impedance in the off state.

Some of the numerous applications for this circuit are a sample and hold circuit to sample and hold analog data that is to be digitized, a high current capability data gate feeding a resistive or reactive load, and a keyed dc restorer with high current capability, as shown in Fig. 2.

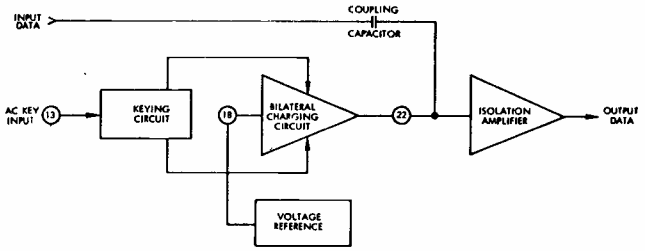


FIG. 2—Bilateral charging circuit used in dc restoration.

In this circuit the input data is fed through to the output via the coupling capacitor and the isolation amplifier. Upon command, the coupling capacitor is effectively shorted to the same potential as the voltage reference. This allows the coupling capacitor to be charged to a potential that is the difference between the input data at the particular command time and the voltage reference. In the off state, the circuit presents a high impedance to the coupling capacitor and thus the correct dc component can be inserted quickly and retained for a relatively long time.

By utilizing the bilateral charging circuit in this application, the dc voltage on the coupling capacitor can be changed quickly in either direction and the impedance of the voltage reference can be relatively high because the amount of current required from the voltage reference is very low.

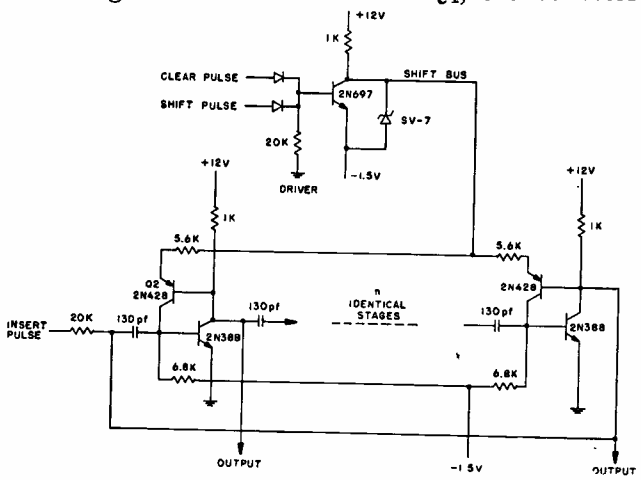
Low Power Binistor Action Ring Counter

THE BINISTOR action ring counter was designed for low cost, high reliability and minimum power dissipation. This ring counter application is extremely useful in digital devices as a time distributor and commutator. The maximum clock rate of the counter is well over 100 kc and it will operate over a temperature range of +70 C to —60 C.

Bistability is achieved by interconnecting a pnp (Q_2) and npn (Q_1) as diagrammed. When base current is supplied to Q_1, its collector voltage decreases until it exceeds the emitter bias of Q_2.

When this occurs, Q_2 is driven into conduction which further drives Q_1 into conduction and this regenerative action continues until Q_1 and Q_2 are in a saturated state. Parallel outputs are taken from the collector of Q_1. Turn on time for a "one" is typically .3 microseconds and its output level is the V_{CE} drop of Q_1.

When the emitter of Q_2 is triggered by a pulse more negative than the base of Q_1, the collector



In ring counter schematic, parallel outputs are taken from Q_1, 2N388 at lower left.

current of Q_2 is reduced, thus decreasing the base current of Q_1 which in turn limits the collector current of Q_1 and further cuts off Q_2. This regenerative action results in both Q_1 and Q_2 returning to the cutoff condition. This "zero" state transition or "turn off" time is typically 0.5 microseconds and its output level is the collector bias supply of Q_1.

The "one" is shifted through the ring counter by capacitively coupling successive stages. The positive transition of a preceding stage couples a positive pulse to the base of the following stage causing it to saturate. The shift pulse must be of shorter duration than the time constant of the coupled stages. By this method the "one" is shifted through the counter.

Prior to start a "clear" pulse is required to reset all stages to the cutoff or zero condition. The "clear" pulse must be of such duration to mask the coupling pulse between stages. A five microsecond pulse was used. An "insert" or read-in pulse is also required to set a "one" in the first stage. The insert pulse can be derived from the trailing edge of the clear pulse or any external source but must occur after the clear pulse. The shift pulse is "OR'ed" with the clear pulse and used to trigger the driver which supplies the proper shift pulses and bias to the stages of the ring counter.

Each stage is temperature stabilized by reverse biasing the stage of Q_1. As in binistors the betas of Q_1 and Q_2 do not appear in the leakage current equations at the node formed by the base of Q_1 and the collector Q_2. The equation for the leakage current of the "off" stages is $I_{CO1} + I_{EO2} + I_{CO2}$. The ring counter as shown can compensate for approximately 220 microamperes leakage current.

Since one stage only is conducting at any time the dissipation of the ring counter proper is only 150 milliwatts, thus making it suitable for low level operation.

Stable, Sensitive Pulse Height Discriminator

CIRCUITS WHICH TRIGGER when an input signal reaches a well defined threshold play a vital part in nuclear and spectrometry counting experiments. A circuit such as this is used when it is desired to exclude unwanted noise or other small pulses from signals being counted. Many trigger circuits have been designed to perform this function; however, they lack the stability or sensitivity required in many cases especially if supply voltage and temperature variations are encountered. The following circuit was developed for use in satellite and rocket applications, but should be applicable to laboratory experiments as well.

Shown in Fig. 1 is the new discriminator circuit using a 1 ma silicon tunnel diode, CR_1, as the amplitude sensing element. This is coupled to a transistor stage, Q_1, for amplification and feedback to obtain a monostable characteristic. Input pulses are coupled across the tunnel diode through a backward diode, CR_2, for isolation.

Operation may best be described by following through a typical triggering sequence and referring to the curves of Fig. 2. These curves represent the actual volt-amp characteristics of the diodes and transistor base-emitter junction. In addition, two composite curves, shown dotted, were plotted by adding corresponding current or voltage points.

Prior to receiving any input signal, a 0.7 ma bias for the tunnel diode is supplied through R_4 which is regulated through the low dc resistance of the delay line, DL_1, by the 7 zener diode, CR_3. This is shown as point 1 on the intersection of the tunnel diode curve and the R_4 load line. An input pulse exceeding approximately 180 mv coupled through CR_1 will trigger the tunnel diode into the high voltage

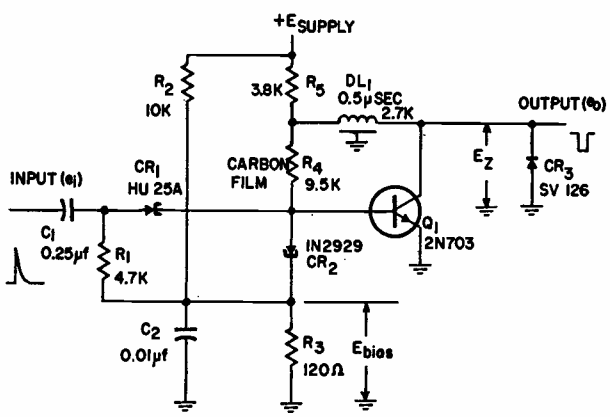


FIG. 1—Discriminator Circuit.

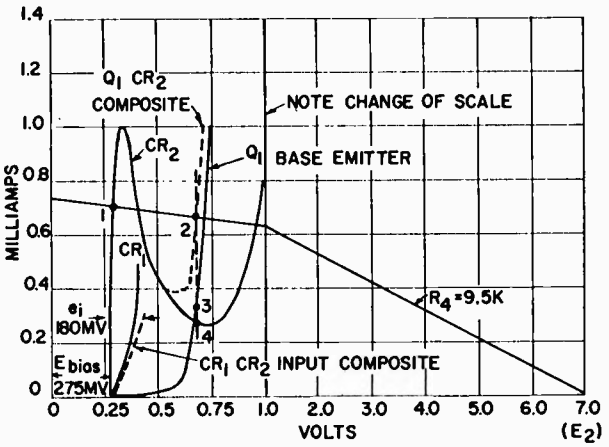


FIG. 2—Graphical Operation of Circuit.

state designated as point 2 on the composite plot. The bias current is now shared almost equally between the tunnel diode and the transistor base-emitter junction shown by points 3 and 4. This amount of base current causes Q_1 to saturate, reducing the voltage across the zener diode close to zero. This drop in potential is propagated through the delay line and appears as a loss of hold bias on the tunnel diode after a one-half microsecond delay. With no bias, the tunnel diode switches back to its low voltage state, cutting off the base current to Q_1. The transistor then switches off and reestablishes the zener regulated potential, E_z. After another half microsecond delay, the 0.7 ma bias is restored (point 1 again) readying the circuit for the next pulse. Theoretically the resolution time of the discriminator is equal to twice the delay line propagation time, 1 microsecond. Actual measurements indicate 1.4 microseconds to be typical, due to the significant junction capacitance of CR_3. Each time the discriminator is triggered a 7-v, 0.8 microsecond pulse is generated, suitable for driving directly binary counters or other digital logic. The output waveform is shown in Fig. 3.

A small bias, established by the voltage divider R_2, R_3, is used in series with CR_2 since the voltage

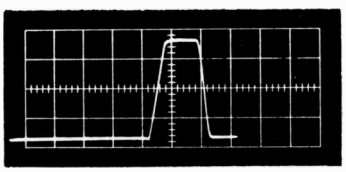


FIG. 3—Output Waveform

swing across the diode alone is insufficient to cause Q_1 to switch fully on. The backward diode, CR_1, isolates low impedance sources from shunting the negative resistance region of CR_2. If a high impedance current source is used to drive the discriminator, CR_1 and R_1 could be omitted. The circuit would then trigger on a 0.3 ma pulse.

The zener diode CR_3 serves to limit the output pulse amplitude in addition to regulating the tunnel diode bias through the 45 ohm dc resistance of the delay line. This regulation is imperfect, however, and almost exactly compensates for variations in the small bias voltage developed across R_3. The resulting bias current through CR_2 remains essentially constant in spite of changes in supply voltage, thereby maintaining threshold stability.

Temperature stability of the threshold is determined by the balance between the positive temperature coefficient of the zener diode, CR_3 and the negative coefficients of the two diodes, CR_1 and CR_2, and the carbon-film resistor R_4.

Over an ambient temperature range of −20 C to +60 C and supply voltage range of 12 to 20 v, a threshold stability of 1 percent is maintained. Furthermore, the potential speed of the tunnel diode produces a threshold almost completely independent of input pulse rise time.

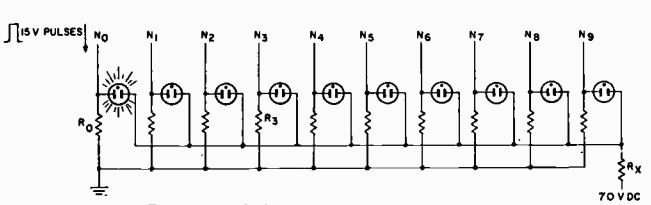
Digital Memory Display

MANY DISPLAY devices require auxiliary storage units such as relays for holding information after pulsed readout, or for converting the signals from low-level transistor circuits to high level display needs. Significant overall equipment cost savings could result from a transistor-compatible display which is self-storing in response to pulsed digital readout. Such a self-storing display should also provide automatic reset upon receipt of a new signal. In some applications, an auxiliary static readout of stored numbers is very important.

These features are realized by an application of neon tubes in a storage-type display device. Using this technique, a typical decimal indicator requires ten neon bulbs and eleven resistors as shown in the circuit diagram on page 38.

The property of neon tubes which requires a definite firing potential level above that potential required to hold them in conducting position is used in operation of this storage-indicator. The dc potential is chosen above the firing potential level. Assume that a typical neon tube fires at 60 volts, and maintains discharge at 50 volts. With the 70 volt dc level, twenty volts is dropped across resistors R_0 and R_x when the 0 indicator is fired. With an R_0 to R_x ratio of 1 to 3, then 5 volts will appear across R_0 and 15 volts across R_x. Thus, the potential on all tubes except N_0 is held to 55 volts, under the firing level, and only tube N_0 will be fired. A dc potential across resistor R_0 of 5 volts is produced, which can be used for static memory output to drive transistorized or tube operated circuits as desired.

Now assume a 15 volt input pulse at tube N_3.



Circuit of digital readout system.

This exceeds firing potential by driving tube N_3 to 70 volts. Current flow through resistor R_x will approximately double momentarily with two tubes

fired, and the 30 volt drop will cause tube N_o potential to drop to 40 volts, well under extinction potential. This is the self-resetting action desirable for a storage type display. After N_o becomes extinguished, the input pulse may be removed, and N_3 will remain fired in the same manner as for N_o.

Because of the low power, low potential input pulses, readout from transistorized circuits is entirely feasible.

Universal N-Bit Shift Register Uses N-Plus-2 Two-Pole Relays

THIS VERSATILE and economical shift register is capable of speeds of up to fifty operations per second. It features parallel or serial read-in, serial read-in from left or right, parallel and serial read-out, shifts right or left, circulating or non-circulating. Output is contact closure to ground for lamp or other read-out. It is non-volatile, retains information indefinitely if power is off, and uses one relay per stage, plus two common control relays. The relays are all standard dual-coil magnetic latching type.

Upon closure of "shift command" contact, relay K_x operates to "set" position. Contact K_xA then energizes the "reset" coils of relays K_1 through K_n resetting them to the "0" state. After several milliseconds delay, relay K_y operates to "set" position and contact K_yB enables the "set" coils of relays K_1 through K_n.

Contact K_yA resets relay K_x to initial condition, and contact K_xA resets relay K_y to initial condition.

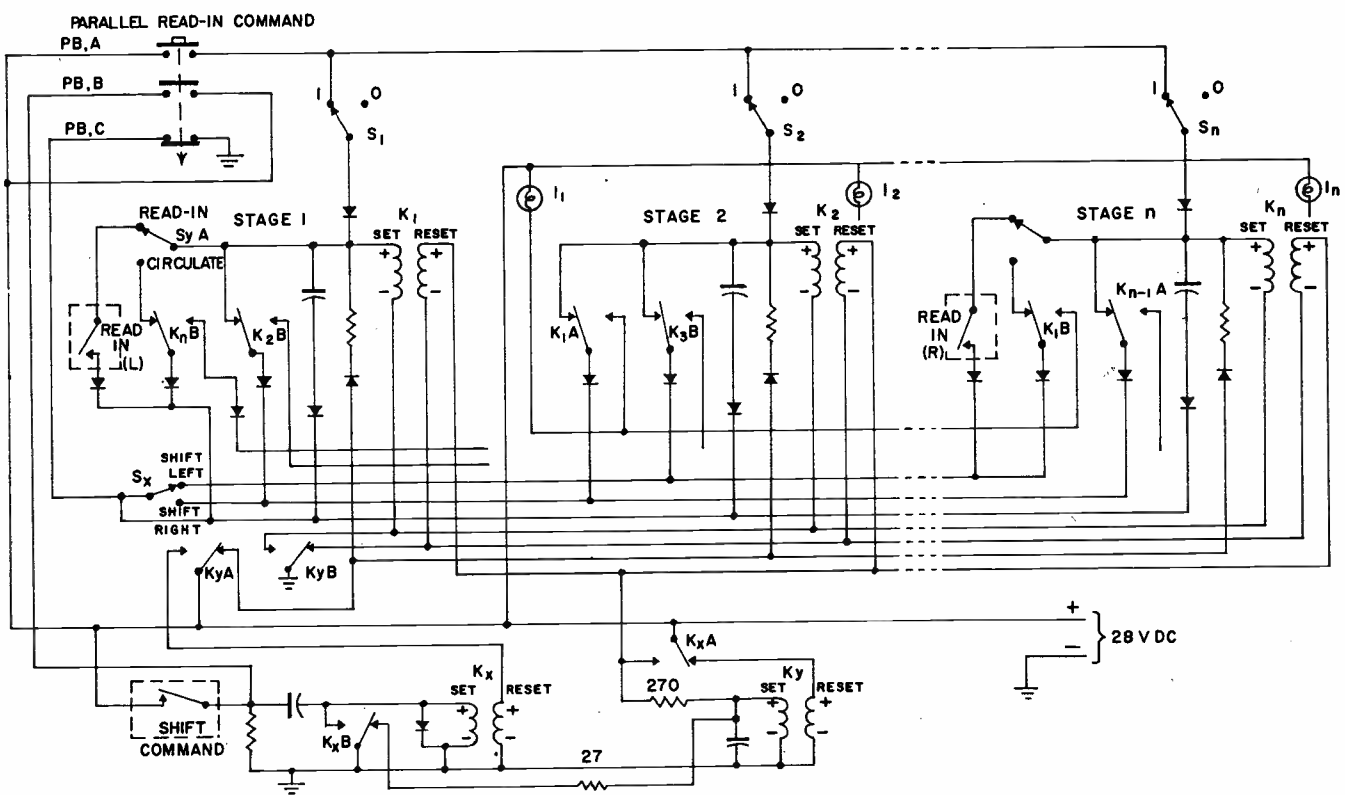
When relays K_1 through K_n are enabled, the capacitor in each stage is given a discharge path through the "set" coil, and to ground via contact K_yB. The capacitor may or may not be charged. If it is charged, it energizes the relay to the "set" or "1" condition. If the capacitor does not happen to be charged, the relay remains reset in the "0" condition.

The capacitor is charged if the previous stage is in a "1" condition, and not charged if the previous stage is in a "0" condition, thereby propagating ones and zeroes along the shift register.

The normally-closed contacts of relays K_1 through K_n short-circuit the capacitor if the previous stage is in the "0" condition, or these contacts open and permit the capacitor to charge through its charging resistor, if the previous stage is in the "1" condition.

For parallel read-in, switches S_1 through S_n are set up as desired, and then pushbutton switch PB_1 is operated. This enters the information in parallel into the shift register.

For serial read-in, switch S_y must be in "read-in" position, and the information is entered from left by closure of "read-in (L)" contact if switch S_x is in "right shift" position, or information is entered from right by closure of "read-in (R)" contact



In the shift register, all A and B normally open contacts of relays K_1 through K_n are tied together and go to readout indicators I_1 through I_n. Capacitors are 8 μf and diodes are 1N537. Unmarked resistors are 250-ohm, 5-watt.

if switch S_x is in "left shift" position.

The "shift command" contact must be closed momentarily once for each shift.

The read-out for all stages are lamps I_1 through I_n, which are lighted to indicate a "1" and dark to indicate a "0". Other loads such as recorders etc. may be put in parallel with lamps.

Stepping-Switch Decimal Counter

THE circuit of Fig. 1 is intended to cause a series of stepping switches to act as a decimal counter to count the number of cards passing through an IBM type 523 punch. In the original application, the stepping-switch bank contacts caused the count to be punched into the cards and performed other control actions not shown in this diagram. The auxiliary relays insure proper action of the stepping switches by stretching the 13-msec pulses from the punch and they also generate alarm signals in case the stepping switches fail to advance.

The circuit is arranged so that the bank contacts of the stepping switch never carry current while they are moving; all making or breaking of current is performed by the auxiliary relays or by the interrupter contacts on the stepping switches. The interruptor contacts, which are intended for just this service, open when the stepping switch coil is energized and close after it is de-energized. The bank contacts move ahead by spring action when the coil is de-energized.

The SET pushbuttons allow a desired count to be set up by advancing each switch one position each time the button is pressed. The RESET pushbutton, through the action of interrupter contacts A causes all switches to step automatically to the home position where action is stopped by the opening of the OFF-NORMAL contacts *ON*. In order that counting will start with the count of one rather than the count of zero, the home position is the ONE position on the units-count switch; on all other switches, the home position is the ZERO pesition.

Automatic counting of the cards starts with a 13-msec 40-v signal which, acting through the contacts of relay K_7, closes relay K_3 which locks itself up through its own B contacts and the B contact of relay K_5. As relay K_3 closes, it energizes the coil of stepping switch K_1. About 170 msec later, a 13-msec pulse from the punch is applied to one side of the coil of relay K_6. Since the stepping switch K_1 has now had some 150 msec to set, its B contacts should be open, and relay K_6 should not be actuated. If for some reason, the stepping switch has not been energized, relay K_6 will close, activating the error alarm flip-flop. The next signal from the punch is

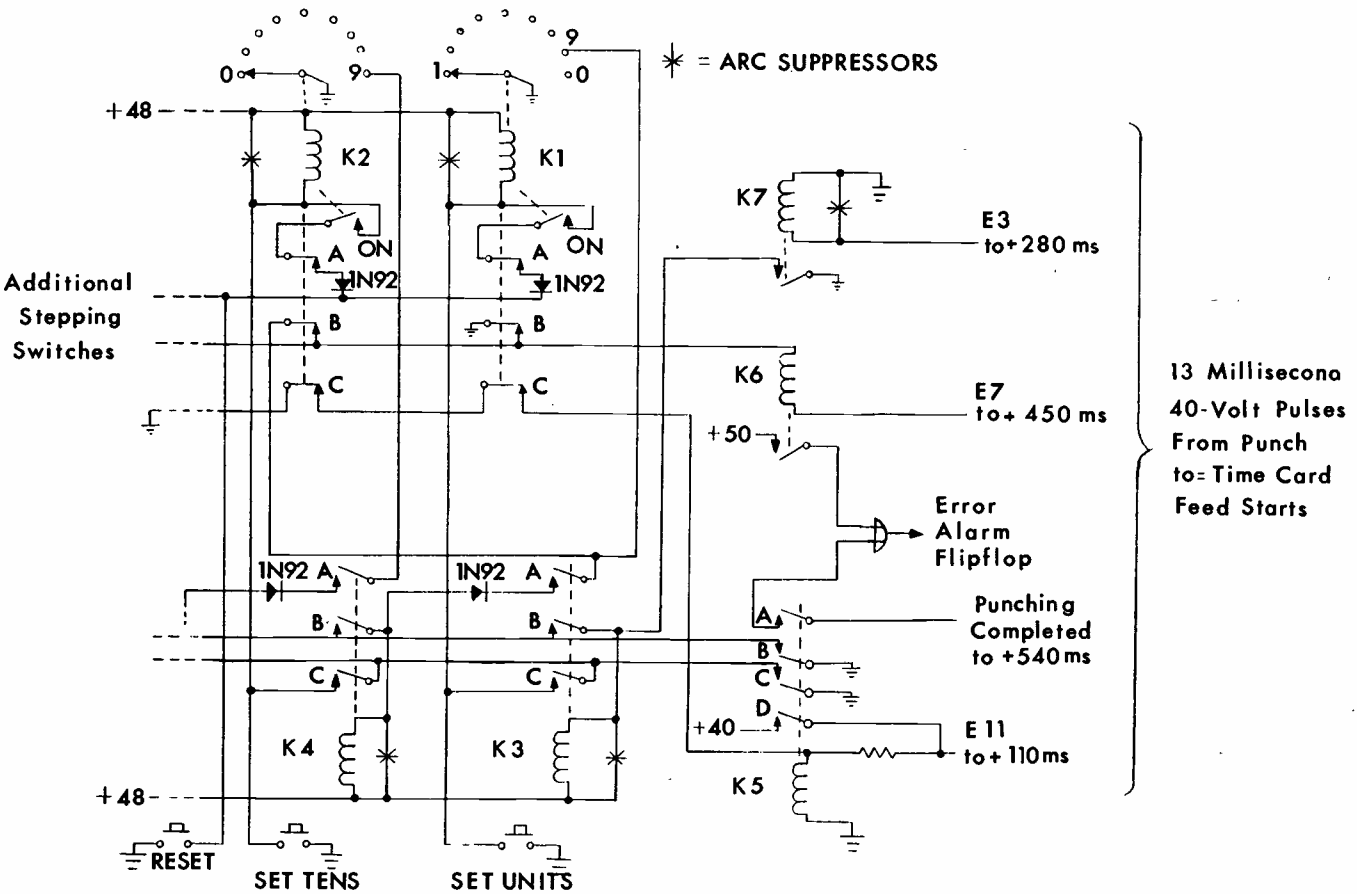


FIG. 1—Counter circuit using stepping switches.

a 20-msec "punch-completed" pulse which energizes relay K_5 and causes it to lock in through its own D contacts. At the same time, the B and C contacts of relay K_5 release relay K_3 and stepping switch K_1 respectively, allowing the stepping switch to advance one count. As switch K_1 is de-energized, its C contacts short out relay K_5, dropping it out. As the next card starts through the machine, a pulse which occurs about 65 msec after the action described above, is applied to the A contact of relay K_5. If the relay is still energized, indicating that one of the stepping switches has failed to advance, this pulse will pass through the closed contacts to activate the alarm flip-flop. About 170 msec after this test, relay K_7 is activated to start the next count cycle.

This counter uses a set-on-nine carry scheme rather than a ripple-down carry on zero. When stepping switch K_1 is in the NINE position, the closing of relay K_3 to energize switch K_1 also acts through the A contacts of K_3 to energize relay K_4 which, in turn, through its C contacts, energizes the coil of the tens stepping switch K_2. When relay K_5 opens its B and C contacts, both stepping switches move ahead; the units switch to zero, the ten switch to one. This carry action can be extended to any number of digits.

The stepping switches are Clare Type 20 with 48-volt coils. The relays are Clare Type J. Relays K_3 and K_4 have 48-volt coils; K_6 and K_7 have 40-volt coils and K_5 has a 24-volt coil with a series resistor to allow it to operate from a 40-volt pulse.

The circuit gives the stepping switches about 150 msec to energize their coils, about 150 msec to step ahead after the coils are de-energized, and provides a check on each operation. All contacts are protected against arcing by back-to-back selenium diodes across coils to limit back voltage and the bank contacts never make or break current. These precautions may seem rather elaborate, but they do give a highly reliable counting system.

Time Delay Relay

RELAY. K in Fig. 1 is a standard 2-pole type with coil resistance of 420 ohms. The 4D50M is a four-layer diode (Shockley) which starts conducting at 50 volts ±4 volts. Potentiometer R_1 (Bourns Trimpot) may be 20K ohm and resistor R_2 about 27K. C is 6 μf.

With these values a delayed energizing time of approximately 400 milliseconds is obtained.

When switch S is closed, C starts to charge to the negative potential (—28vdc) When the charge reaches approximately 20 volts, the four-layer diode breaks down and conducts causing relay K to become energized. K is now kept in the energized

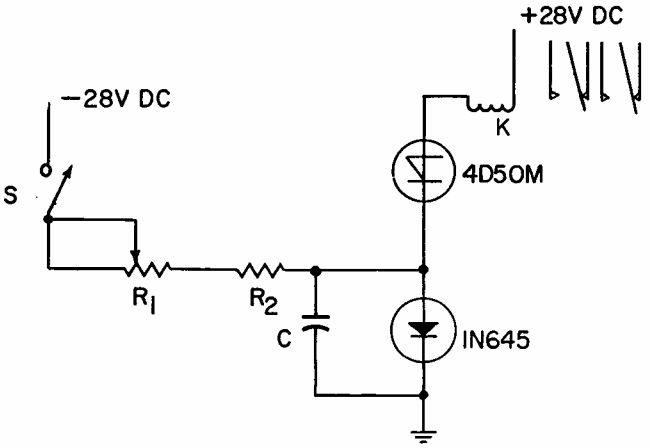


FIG. 1—Simple time delay circuit uses four-layer diode.

state by the four-layer diode thus the relay does not need to utilize a set of its contacts to hold it energized. To de-energize the relay, a switch or other controlling device may be inserted in series with the ground return.

Delay durations from 50 milliseconds up to 5 minutes were obtained by varying the RC time constant.

Sample and Hold Circuit with Long Memory

THIS CIRCUIT is used to sample and hold the value of a varying input voltage at a time controlled by a key pulse. The secondary of pulse transformer T_1 supplies enough current through diodes CR_1, CR_2, CR_3, and CR_4 to effectively connect the input to the memory capacitor during the key pulse interval. During the off time, the diodes CR_1, CR_2, CR_3, and CR_4 isolate the input from the memory capacitor regardless of input polarity, except for any conduction path through the pulse transformer secondary

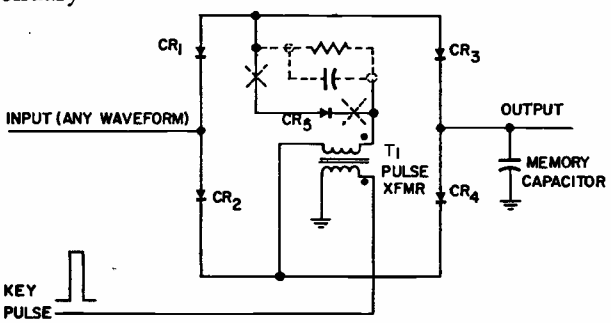


FIG 1—Sample and hold circuit.

Usually, a blocking capacitor (shown in dotted lines) which is small relative to the memory capacitor is placed in series with the transformer secondary. However, it must be shunted with a resistance to prevent its charging until no further diode conduction occurs. The capacitor value and shunt resistance must be chosen carefully, based

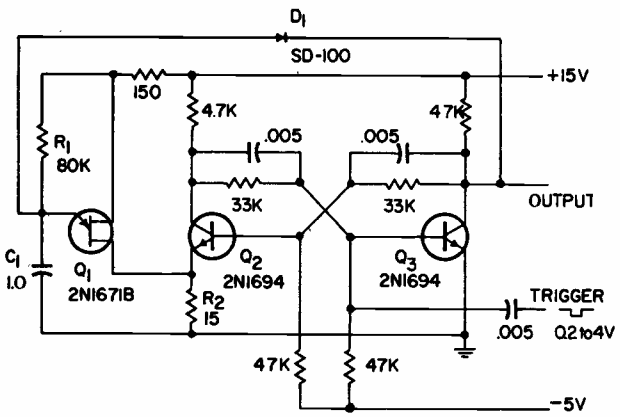
on the range of sampling rates over which the circuit must operate. At best, the circuit is usually a compromise.

By using the Zener diode CR_5 shown in this circuit, leakage through the transformer secondary is reduced to that of the diode. The Zener diode is chosen to have a breakdown voltage greater than the maximum difference between input and output. Thus, the circuit can be made to operate over a wide range of sampling rates, with improved sampling accuracy, shorter key pulses and longer memory.

Wide Range Timing Circuit

SIGNIFICANT advantages in applications where long timing intervals and good temperature stability are required can be provided by the timing circuit shown. It is similar to the hybrid one-shot multivibrator circuits described in the literature, but offers improvements in operating margins, recovery time, and temperature stability.

Transistors Q_2 and Q_3 are low leakage germanium npn transistors which form a flip-flop designed for operation at ambient temperatures up to 80C. The unijunction transistor, Q_1, is a low-leakage, high-sensitivity type which is used in a simple relaxation oscillator circuit to perform the timing function. In the quiescent condition Q_3 is conducting and the emitter of Q_1 is clamped to a low voltage by diode D_1. Timing is initiated by a negative trigger pulse at the base of Q_3 which turns Q_3 off and Q_2 on. The clamping diode, D_1, is then reverse biased and C_1 is allowed to charge through R_1.



Timing interval of this circuit can be varied from 10 millisec to 0.3 second.

After a period of approximately 0.8 R_1C_1 the voltage across C_1 exceeds the peak point voltage of the unijunction transistor causing it to fire. The discharge current of C_1 generates a positive pulse across R_2 triggering the flip-flop back to its quiescent state. When this triggering action occurs, C_1 partially discharges through the emitter of Q_1 and is then completely and rapidly discharged through D_1 and the collector of Q_3. This action establishes the initial voltage on C_1 and thus serves to reduce the variation of timing interval with temperature and duty cycle.

Operating tests on the circuit have demonstrated a high degree of accuracy over a wide range of temperature, duty cycle and trigger amplitude. Testing to extreme temperatures indicated that the circuit could operate up to 105 C which was well above both the design temperature limit and the maximum rated operating temperature of the germanium transistors.

The time interval changed by less than 0.4 per cent over an ambient temperature range of 25 C to 80 C and by less than 0.7 per cent over a range of duty cycle from 1 to 95 per cent. The circuit was triggered reliably by pulses having a width of 2 μsec or greater and an amplitude from 0.2 to 4 volts. The timing interval, nominally 60 milliseconds, can be varied over a range from 10 milliseconds to 0.3 second by suitable choice of R_1. Other timing ranges can be achieved by changing the value of C_1.

Relay Binary Counter Module

CONVENTIONAL double-pole relays may be employed to produce modular stages of a binary counter. Each module requires two relays, two resistors and two diodes. n modules may be cascaded to yield a counter of 2^n-1 total count.

The basic module circuit is shown in Fig. 1. Relay A coil actuates contacts a_1 and a_2. Similarly for relay B. Inputs are applied to relay K coil whose contact is labelled k. All relays are shown in the de-energized state.

When a pulse is applied to the coil of pulse repeater relay K, the relay pulls in and relay A coil becomes energized by application of voltage through normally open contact k and normally closed contact b_1, to the high side of coil A. Relay A pulls in and locks up through normally open contact a_2.

After the pulse input to relay K collapses, relay K drops out. Relay B coil now become energized by application of voltage through normally closed contact k and normally open contact a_1 to the high side of coil B. Relay B pulls in and locks up through normally open contact b_2.

Upon receipt of a second pulse, relay K again closes and relay A *is* forced to drop out by application of voltage through normally open contact k and normally open contact b_1 to the low side of coil A.

Upon collapse of the pulse input to relay K, relay K drops out and relay B is forced to drop out by application of voltage through normally closed contact k and normally closed contact a_1.

The circuit is now in the same state as prior to

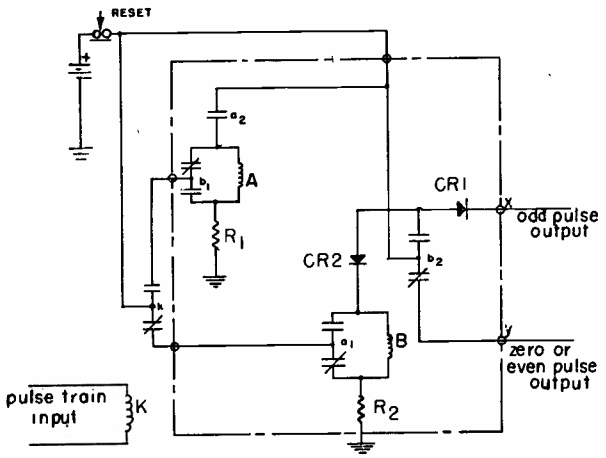


FIG. 1—Schematic of module.

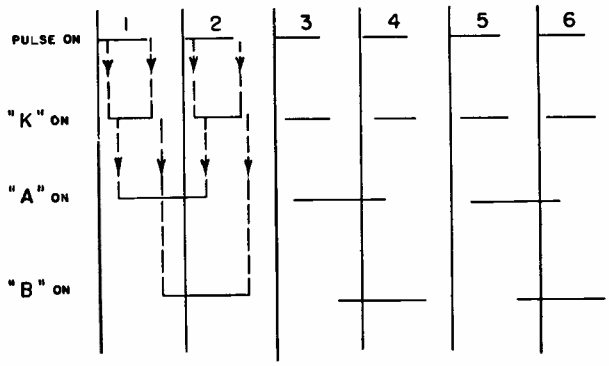


FIG. 2—Module cycle sequence.

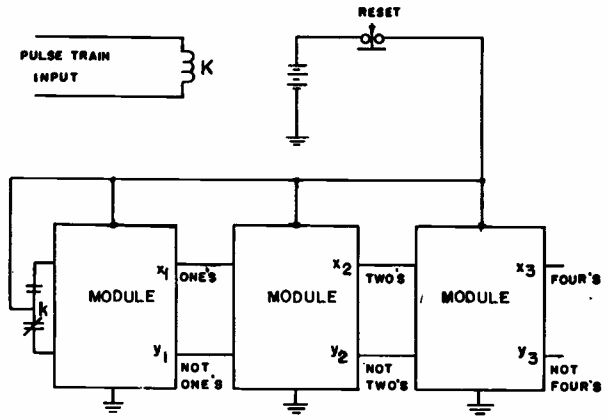


FIG. 3—Three-stage binary counter.

receipt of the first pulse, namely all relays deenergized, and the application of further pulse inputs to relay K produces the same cycle of events as described above. Figure 2 illustrates the cycling sequence.

The b_2 contacts of relay B provide readout and output from the circuit. Odd pulses produce output on terminal X, even pulses or no pulse input produces output on terminal Y. Diodes CR_1 and CR_2 provide isolation between the relay module and output circuitry.

Cascading of modules identical to that of Fig. 1 can produce an n stage binary counter. A 3-stage counter is shown in Fig. 3. Readouts can be both direct binary or binary complemented from full count of the n stage counter.

Simple Current Integrator

VOLTAGE developed across a capacitor may be utilized to measure the time integral of current (accumulated charge) regardless of the form in which it arrives at the capacitor. However, the total charge that can be measured accurately is limited by the available capacitance. If a trigger mechanism is arranged to discharge the capacitor and operate a register after a preset level is reached, the cycle may be repeated many times and the total accumulated charge measured as a digital output.

A meter relay coupled to an electrometer tube can provide a simple trigger system that does not suffer the instabilities of a gas thyratron trigger or the complexities of the tachometer type integrators.

A model of the current integrator described here has been in daily use for more than 2 years as an x-ray beam current integrator. Other than a

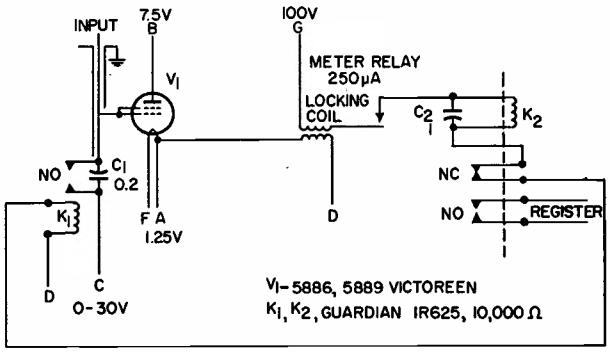


FIG. 1—Circuit of current integrator. Lettered leads connect to power supply leads of Fig. 2.

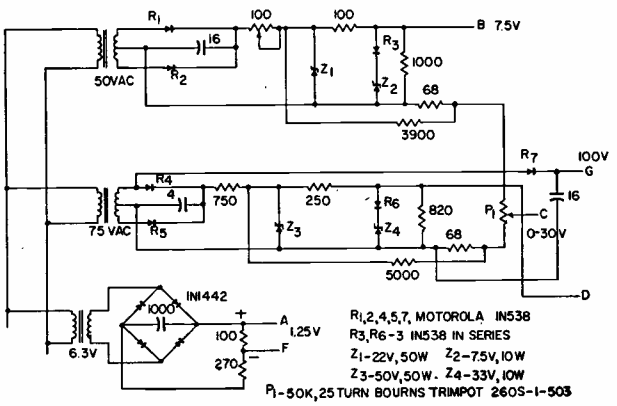


FIG. 2—Rectifiers R3 and R6 each consist of three in series.

weekly check on its accuracy, resulting in occasional adjustment, it has not required servicing.

As current flows to C_1 (Fig. 1) the grid of the electrometer tube begins an exponential rise from a negative voltage and approaches 0 volts. As the grid voltage approaches zero, electrometer current flows. When the current reaches a value that has been preset on the meter relay, the con-

tact close, causing the locking coil to be energized. At the same time the two relays in series with the locking coil are energized. One of these relays has a set of normally open contacts across C_1. The movable arm of this relay has been replaced with an arm made of Teflon with the contact point connected to the high impedance end of C_1, thus providing a very high impedance path for the input circuit. This relay, when energized, discharges the capacitor. The discharge time is short (10 millisec) compared to the average cycle time (10 seconds). Therefore, the integrator presents a "dead condition" for only 0.1 per cent of the cycle.

Relay K_2 energizes a mechanical register by which a visual indication of the number of completed cycles is given, and de-energizes the meter relay locking coil so that all relays can return to the de-energized state. The mechanical register can be of the preset-count type, equipped with an end-limit switch to terminate measurements when the desired integral has been reached.

The cleanliness of the high impedance components is essential, as is the light shielding of the electrometer tube. Capacitor C_1 is a Glassmike type and is washed thoroughly in petroleum ether to eliminate all traces of grease film. The electrometer tube, C_1 and K_1, are installed in a light-tight, hermetically-sealed box. With a clean, properly working circuit, a small charge placed on C_1 will neither leak off nor gain over a period of days.

Figure 2 shows the power supply, which is voltage regulated as well as temperature compensated in the plate and bias sections.

Line voltage variations of 10 per cent change the output voltages by only 0.0001 per cent[1]. The temperature stability of the series-connected rectifiers R_3 and R_6 and zener diodes Z_2 and Z_4 is 0.004%/°C.

Sensitivity of the circuit can be varied by changing the value of C_1, the bias voltage C, and by the adjustable scale contact of the meter relay.

With a bias voltage of −30 volts and an input current of 10^{-8} amp, a range in triggering time of approximately 1 second to more than 1 minute is available.

Other possible applications of the integrator are densitometry, average computing, power totalizing, and radiation alarm systems.

Zero-Order Data Hold

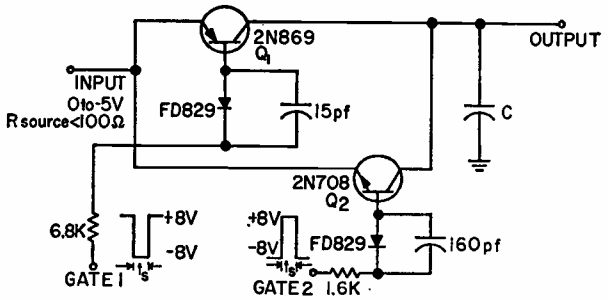
A ZERO-ORDER data hold circuit is required in some sampled-data systems and analog-to-digital converters. This circuit is one that samples an analog signal and then holds that sample value for a period of time much longer than the sampling aperture.

The circuit in the figure has been used to sample inputs with an accuracy of 0.1 percent of full scale using a sampling aperture of 1.25 μsec or longer. The holding accuracy, of course, depends on the input resistance of the following stage. Operating into a 2 meg load, the voltage deviation can be kept to less than 0.1 percent of full scale if the ratio of holding time to sampling time is 10 or less.

Q_1 and Q_2 provide a switch that is essentially bilateral since the voltage across the capacitor C can make a full-scale transition in either a positive or negative direction during one sampling aperture. The diode-capacitor combination in the base of the switching transistors insures that the base-to-emitter breakdown voltage is not exceeded since the back resistance of the diode is much greater than that of the base-emitter junction. The value of C required for 0.1 percent sampling accuracy can be determined from

$$C = \frac{t_s}{6.91\,R}$$

where t_s = sampling aperture and R = resistance in charge and discharge path of C.



Sample-and-hold circuit.

Precision Solid-State Delay Circuit

THIS CIRCUIT gives time delays of over three minutes without the usual tantalum or electrolytic capacitor. The low leakage requirement for the timing capacitor, C_1, is easily obtained with a mylar capacitor.

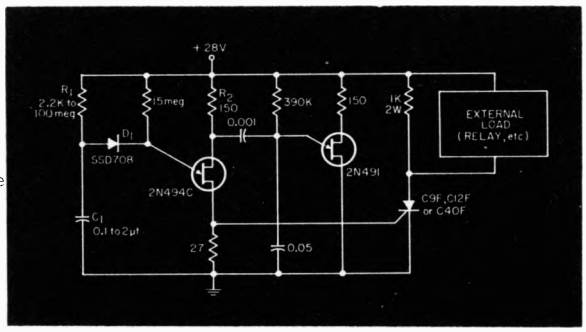
The timing interval is initiated by applying power to the circuit. At the end of the timing interval, which is determined by R_1C_1, the 2N494C fires the SCR. This places the supply voltage, less about 1 volt, across the load. Load current is limited only by the rating of the SCR, which is from 1 amp to 25 amp for the types specified in the circuit. A calibrated potentiometer can be used in place of R_1 to permit setting a predetermined time delay after one initial calibration.

The charging resistor, R_1, must be small enough to supply the minimum firing current (peak point current, I_p) of the UJT plus the leakage current of the capacitor when the UJT emitter is biased at its peak-point voltage. The 2N494C requires a minimum I_p of 2.0 μa. This places a limit of 3 meg for R_1 and permits time delays to 6 sec ($C_1 = 2$ μf) without using the additional 2N491 relaxation oscillator.

The circuit, as shown, effectively reduces the minimum I_p requirement by a factor of 1000 by pulsing the upper base of the 2N494C with a 3/4-volt negative pulse. This

negative pulse rate is not critical but it should have a period that is less than 0.02 R_1C_1. The negative pulse causes the peak point voltage to drop slightly and if the voltage level at C_1 is greater than this, the unijunction will fire with the necessary I_p supplied from C_1. With this technique, this circuit gives time delays of about one hour with 2000 meg at R_1 and 2 μf at C_1. The repeat-

R1 2k2 to 100M
D1 SSD708
Resistor D1 cathode 15M



Delay is set by R_1C_1 time constant.

ability of the time delay from one day to the next is within 0.15 per cent. R_2 can be adjusted or selected for best stabilization of the firing point over the required temperature range.

A pulse transformer can be used in place of the 27-ohm resistor if it is necessary to have the timing circuit isolated from the power switching (controlled rectifier) circuit which, for instance, mght be connected to the ac line.

The input impedance of the unijunction transistor is greater than 1500 meg before it is fired. The maximum time delay is mainly dependent upon the maximum values of R_1 and C_1 consistent with the low leakage requirement.

The diode D_1 allows higher values for R_1. For example, with an accuracy of 1/2 percent at 25°C and 5 percent at 55°C, without D_1, R_1 is limited to 15 meg, but with D_1, R_1 can be increased to 10,000 meg. ◆◆

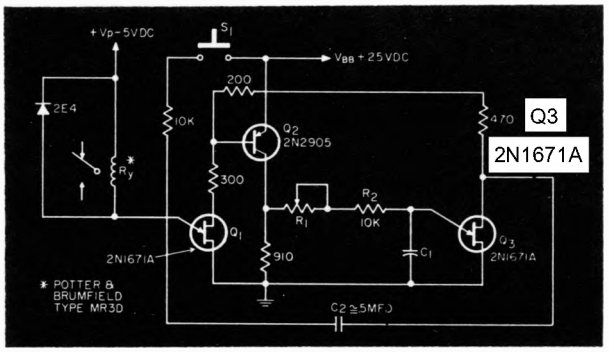
Interval Timer

INEXPENSIVE RELAYS can be used to provide excellent timing accuracies with high isolation in this unijunction-transistor timing circuit. The circuit uses the power gain of the emitter junction of UJT Q_1.

In the "off" state, the power dissipated in the relay is less than 10^{-9} watts and in the "on" state the power dissipated can approach 1.5 watts, depending on the relay coil resistance.

Depression of S_1 produces sufficient firing voltage for UJT Q_1. This causes emitter-current modulation, which results in actuation of R_y. Upon conduction of Q_1, the base of transistor Q_2 is switched from a cutoff to a saturation state. This results in the voltage $V_{bb} - V_{ce(SAT)}$ being applied to the timing network of R_1, R_2, and C_1.

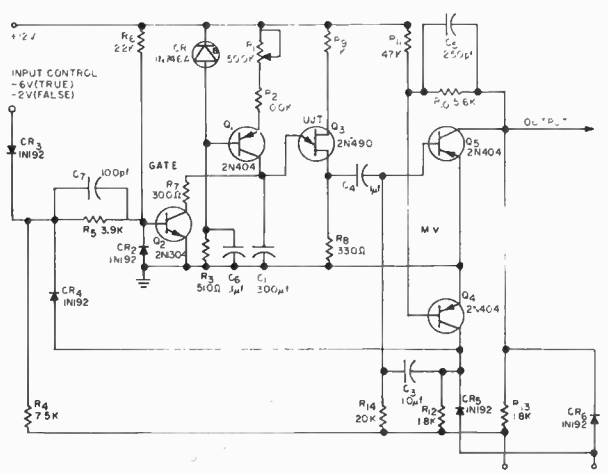
When C_1 charges to the peak firing voltage of UJT Q_3, a negative pulse is generated at its base 2 element. This pulse is fed back through C_2 to the emitter of Q_1 which results in operation on the unstable (negative resistance) portion of the emitter characteristic curve. This causes Q_1 to switch to a nonconductive state and completes the cycle. The timing constant of R_1 and R_2 and C_2 is determined by the formula $T = -(R_1 + R_2)\ (C_1)\ ln\ (1\text{-}n)$ where n is the intrinsic stand-off ratio.



Interval timer.

Accurate Time Delays up to Four Minutes

ACCURATE TIME DELAYS greater than one minute are difficult to achieve using conventional methods. However, with a unijunction transistor as the switch, an accuracy of ±1% at 25°C ±10°C for time delays between one and four minutes can be achieved.



Four-minute timing circuit.

Although the circuitry in Fig. 1 was designed for a controlled environment, the temperature range can be extended by including a thermistor temperature-compensating network in the constant-current configuration Q1.

In the circuit shown, the input AND gate is enabled by a −6-v input. This negative voltage cuts the gated clamp Q2 off and allows the timing capacitor C_1 to charge linearly through the constant-current generator Q1.

When the charge across the timing capacitor C_1 reaches the peak-point emitter voltage of 6.4 v, unijunction Q3 fires and the 1-v positive pulse developed across R_8 triggers the 80-msec one-shot multivibrator composed of Q4 and Q5.

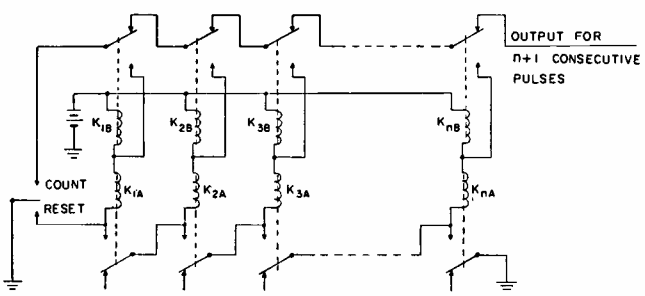
In the quiescent state, the 80-msec one-shot multivibrator provides one enabling input to the two-input AND gate. However, the triggering of the one-shot

multivibrator inhibits the input control AND gate and re-enables the gated clamp $Q2$. The saturation voltage V_{esat} ($Q3$) stored by C_1 is discharged through $Q2$ to ground. This action allows the full amplitude of the charging ramp voltage to be utilized and extends the time duration appreciably.

The complementary output of the one-shot multivibrator provides True or False output logic levels for associated circuitry. Adjustable time delays between one and four minutes are possible by varying trimmer potentiometer $R1$.

Relay Chain Counts Consecutive Pulses

THIS RELAY CIRCUIT is designed to provide an output pulse if, and only if, a given number of input counting pulses are received consecutively



Counter relay chain provides low-cost fail-safe operation.

If the counting pulses are interrupted by a reset pulse, the entire consecutive count starts over again from zero. As a secondary feature, all relays are normally energized so that coil failure or power failure can result in a premature output, but never an overcount.

At the beginning of a count all relays are energized and held-in through the contacts of the A relays. As the COUNT contacts close, K_{1A} is shunted and drops-out, but K_{1B} is held-in through its own contacts in series with the contacts of the COUNT switch. As the COUNT contacts reopen, signifying the completion of the first pulse, K_{1B} drops-out. The second count pulse will drop-out K_{2A} on make and K_{2B} on break, and so on down the line until pulse n drops-out K_{nA} and K_{nB}. The $(n + 1)$ pulse will pass straight through to the output. A reset pulse at any time will re-energize all dropped-out relays. The minimum duration of the reset pulse must be equal to the pull-in time of the type of relay used, multiplied by the number of pairs of relays in the chain.

A typical circuit for counting three consecutive pulses may use four relatively inexpensive spdt relays.

Relay Counters

COUNTERS which count in accordance with the binary cyclic code can be constructed to operate reliably using relays with double-throw contacts. In the circuits to be described, a counter with 2^n stable states requires n relays and a total of n^2 contacts.

A counter with four stable states is shown in Fig. 1. This counter uses two relays and four contacts. Relay A is made up of the coil labelled A and the contacts labelled A_1 and A_2. Similarly for Relay B. Both relays are shown in the deenergized state.

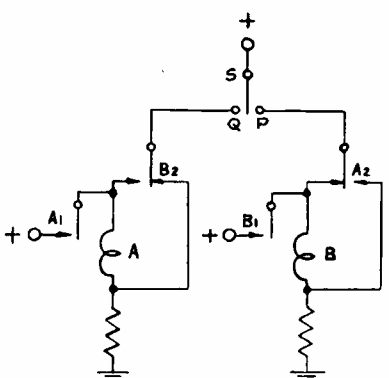
Table 1 describes the stable states through which this counter progresses as switch S is alternated between positions P and Q. A zero represents the deenergized state of a relay; a one represents the energized state.

TABLE I—Stable States of Two-Stage Counter

Stable State	Relay A	Relay B
1	0	0
2	0	1
3	1	1
4	1	0

Figures 2, 3, and 4 show counters having 8, 16, and 32 stable states, respectively. Table 2 lists the 32 stable states through which the last counter progresses. Portions of this describe the stable states of the smaller counters. Stable states 1 through 8, and columns C, D, and E describe the operation of a three-stage counter. Stable states 1 through 16, and columns B, C, D, and E describe the operation of a four-stage counter.

FIG. 1 — Two-stage counter.



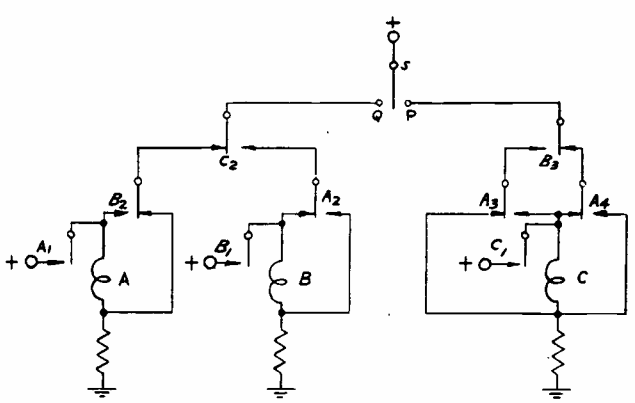


FIG. 2—Three-stage counter.

Circuits for counters with more than five relays can be obtained by extrapolating from the figures shown.

The author expresses his thanks to Sidney M.

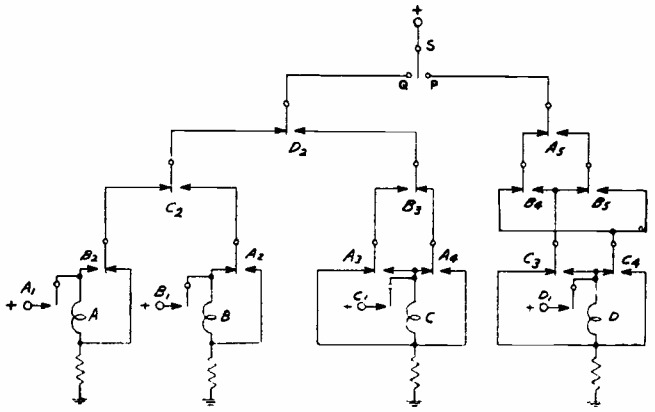


FIG. 3—Four-stage counter.

Stone for the experimental verification of these circuits.

TABLE II—Stable States of Five-Stage Counter

Stable State	Relay				
	A	B	C	D	E
1	0	0	0	0	0
2	0	0	0	0	1
3	0	0	0	1	0
4	0	0	0	1	0
5	0	0	1	1	0
6	0	0	1	1	1
7	0	0	1	0	1
8	0	0	1	0	0
9	0	1	1	0	0
10	0	1	1	0	1
11	0	1	1	1	1
12	0	1	1	1	0
13	0	1	0	1	0
14	0	1	0	1	1
15	0	1	0	0	1
16	0	1	0	0	0
17	1	1	0	0	0
18	1	1	0	0	1
19	1	1	0	1	1
20	1	1	0	1	0
21	1	1	1	1	0
22	1	1	1	1	1
23	1	1	1	0	1
24	1	1	1	0	0
25	1	0	1	0	0
26	1	0	1	0	1
27	1	0	1	1	1
28	1	0	1	1	0
29	1	0	0	1	0
30	1	0	0	1	1
31	1	0	0	0	1
32	1	0	0	0	0

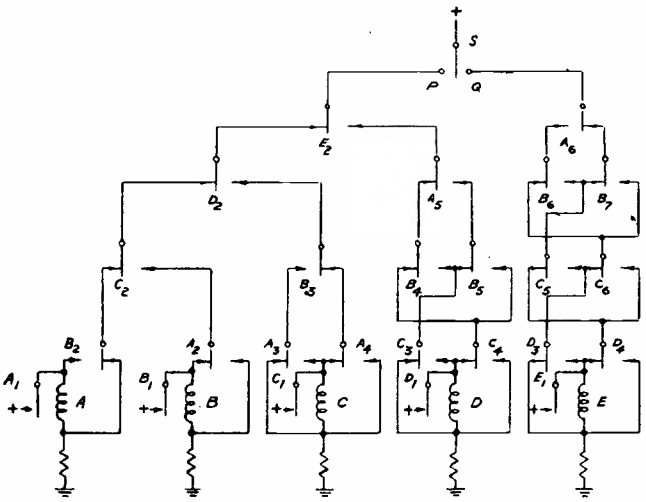
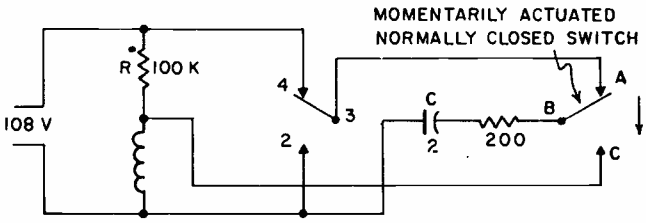


FIG. 4—Five-stage counter.

Relay Flip Flop

DESIGNED for use with an automatic machine tool, the circuit shown in the illustration functions as a binary counter. The system has proven reliable where slow-speed counting or sequence switching is required.

Normal resting position of relay contacts and the momentary contact sensitive switch are as shown in the schematic. The 108-v supply was taken from the existing equipment.



Switch actuated by machine tool operates binary counter relay.

Capacitor *C* charges to 108 v through relay contacts 4-3, and sensitive switch contacts *A*-*B*. A holding current of 1 ma flows through the relay coil. This magnitude of current is insufficient to close the relay.

When the normally-closed, momentary contact, sensitive switch is actuated, the charged capacitor *C* is switched across the relay coil resulting in a large current flow actuating the relay contacts. The 1-ma holding current flowing through *B* is ample to hold the relay closed when the switch returns to the normally open position. Capacitor *C* will now discharge through relay contacts 3-2 and sensitive switch contacts *A*-*B*.

Another actuation of the normally closed sensitive switch connects the discharged capacitor *C* across the relay coil where it appears as a virtual short circuit, de-energizing the relay and allowing the relay contacts to return to the original position.

Low-Frequency Stairstep Generator and Timing Circuit

A STAIRSTEP generator that will accept pulse inputs, either random or evenly spaced, and produce an output after a fixed number of inputs is often useful in measuring and recording low-frequency data. The circuit shown in Fig. 1A is capable of accepting pulses having any fixed width from a millisecond to several hundred milliseconds and producing a stairstep output having any number of steps from two to one thousand.

Transistor Q_1 with R_1, R_2, R_3 and zener diode D_1 form a constant current generator. Capacitor C_1 acts as a storage reservoir for the current output at the collector of Q_1. Resistor R_1 is adjusted to cancel out the leakage current occurring in C_1, R_5, and Q_2 when C_1 is half charged. With this adjustment, leakage can be controlled close enough so that an error due to leakage is less than one percent if a pulse input is more frequent than one every twenty seconds. Unijunction transistor Q_2 triggers at a fixed value of emitter voltage. The point at which Q_2 triggers is fixed by the voltage across zener diode D_2.

When Q_2 starts to discharge, a positive pulse is fed through C_2 and turns on the controlled rectifier Q_3, which in turn discharges C_1 essentially to zero. Then Q_3 recovers and presents a high impedance to current flow as soon as the voltage across C_1 falls to zero, as there is not a high enough current output from Q_1 to sustain conduction.

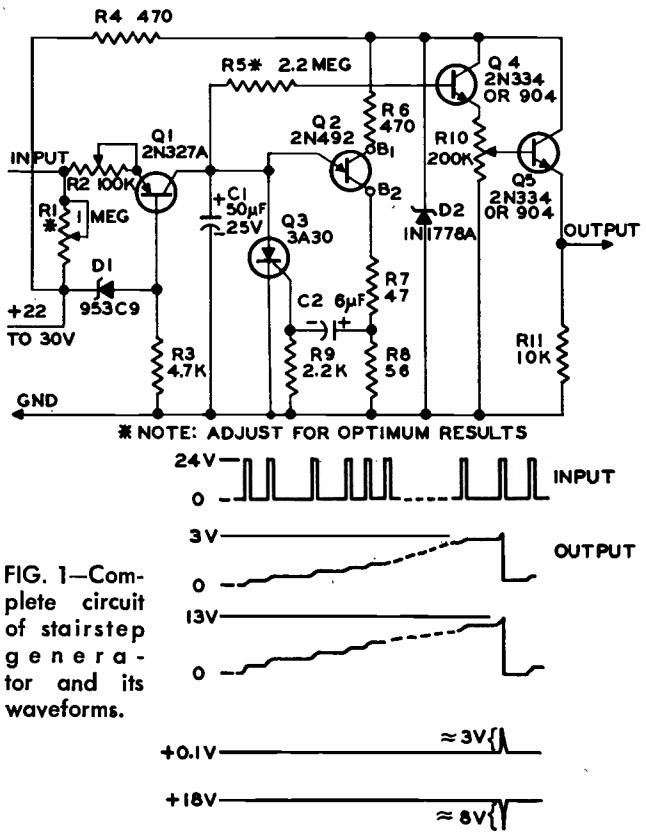


FIG. 1—Complete circuit of stairstep generator and its waveforms.

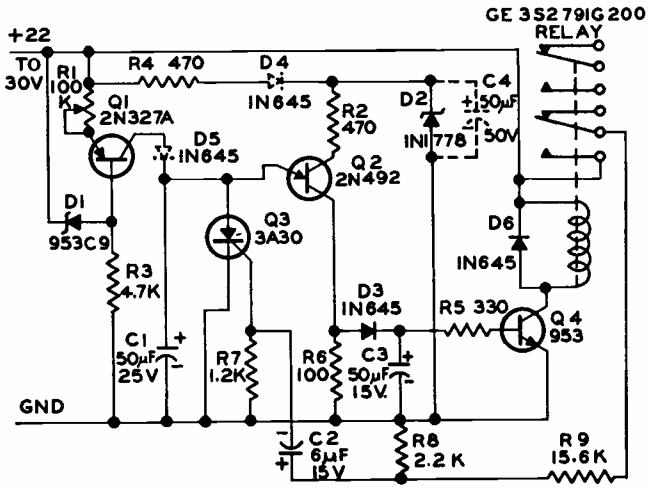


FIG. 2—Repeat cycle timer results by revising basic circuit shown in Fig. 1.

Adjustment of R_2 provides the desired amount of input current during a step input to fix the number of pulses in one group of steps.

An impedance matching amplifier, Q_4 and Q_5, is capable of driving a relatively low-impedance load. With the proper balance of R_5 and setting of R_{10}, the output can be adjusted to provide an output of 0 to 3 volts.

Figure 1B shows the waveforms obtained in the circuit. By changing R_1 to a smaller value and eliminating R_2, the output is a sawtooth with a linearity of one percent. The quality of the capacitor used for C_1 is important for linearity. The period of the sawtooth is variable from 10 milliseconds to 15 minutes, depending on the value of C_1 and R_1. The circuit has performed satisfactorily with a value of 600 µf for C_1. The only criterion for reliability is that Q_3 be capable of handling the high pulse current during discharge of C_1.

By modifying the circuit to that of Fig. 2, a repeat cycle timer is constructed capable of providing output pulses over a dynamic range of several thousand. In this circuit Q_3 is fired through the second pair of relay contacts to insure that sufficient current is passed to C_3 to provide a positive and consistent period of relay closure. The time that the relay remains closed is determined by size of C_3 and R_5.

The biggest advantage of this type circuit other than the wide dynamic range it covers is the large amount of ripple it will tolerate from the prime power source. If diodes D_4 and D_5 are added, as shown in dotted lines in Fig. 2, along with C_4, the unit will tolerate transients of as high as ±100 percent of the supply voltage and of several microseconds duration.

Simple FET Timer

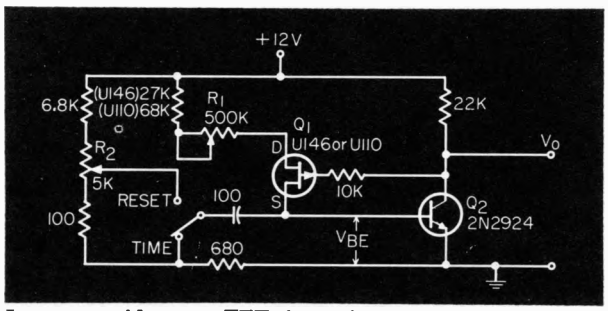
THIS SOLID-STATE TIMER uses a FET constant-current source to eliminate time-period errors due to unregulated power supplies and line transients.

In the "reset" switch position, the timing capacitor charges to the pre-set positive voltage on the divider network. The timing cycle begins when the switch is moved to the "time" position. The positive capacitor plate then is grounded and a negative voltage equal to the original positive capacitor charge is transferred to the base of bipolar transistor Q_2. The output voltage v_o rises to +12 V.

The FET, connected as a self-biased constant-current supply, now begins to linearly remove this negative charge in a time $t = CV/I_D$, where C = capacitance, V = reset voltage + $V_{BE(SAT)}$, and I_D = FET constant drain current.

The timing cycle ends when Q_2 turns on, and drops the output voltage v_o to $V_{CE(SAT)}$. Sharp turn-on action is provided by a regenerative action increasing available FET constant current as Q_2 turns on.

To achieve overall zero or near zero temperature coefficient for the timer, the FET constant drain current is set by R_1 to the FET nominal zero T.C. drain current, about −10 μA. Operated thus, the timer shown has a time period approximately 0.1—50 sec controlled by R_2.



Low-cost, wide-range FET timer circuit.

Total component cost for the circuit using a U-110 FET is estimated at $12.76 in small quantities and $9.97 in 100 and up quantities. With a lower cost, lower g_m U-146 FET, component costs are $10.76 in small quantity and $7.42 for 100 and up.

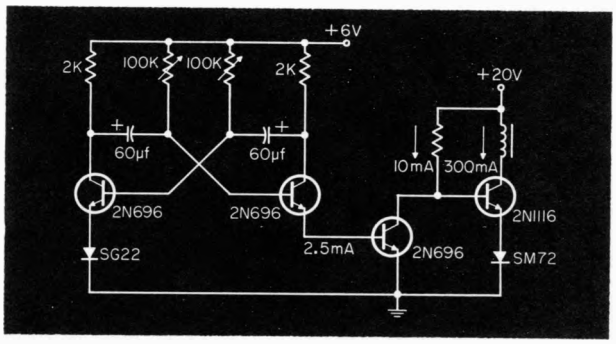
Recycling Timing With Variable Duty-Cycle

THIS CIRCUIT was designed to offer, at low temperatures, a variable recycling time delay with adjustable time-on, time-off.

In the circuit, the 100-K variable resistors control on and off times. Some refinements are necessary to make the circuit operational down to −65°C (a minimum beta of 20 at this temperature is required). For −50°C, an unselected transistor will perform well with 300 ma load.

If a small current is used, 50 ma or so, the second transistor could be eliminated, as could SM 72 as long as the emitter current of the trigger is increased, by changing the bias, to about 3.5 ma.

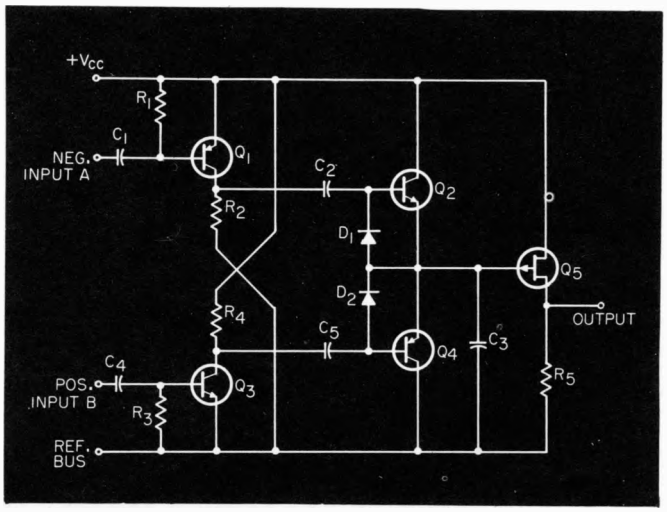
The circuit as shown has a time delay of 0.300 sec to 6 sec. Care should be taken when the 300 msec level is set because the base bias, i.e., 100 K, may now be almost as low in value as the load resistance, and the multi will not start.



Recycling timer with variable duty-cycle.

Reversible Linear Counter

THIS CIRCUIT provides uniform discrete steps in output voltage for pulses at the input terminals. Negative pulses at A cause positive steps in the output voltage. If terminals A and B are joined, positive pulses will cause negative steps, and negative pulses will cause positive steps in the output voltage. The input pulses, however, must be short and of small enough amplitude so that overshoot of the trailing edge will not drive the counter in reverse.



Counter circuit in which negative pulses at A give positive steps in output voltage. Counting is reversed by applying positive pulses at B.

Operation is as follows: initially the voltage between the base of Q_2 and the reference bus, will be the voltage across C_3 ± 0.7 volts (conducting potentials of diode D_1 and the base-emitter diode of Q_2). The voltage at the collector of Q_1 will be zero, since Q_1 is not conducting.

A negative pulse into terminal A will cause Q_1 to conduct, and the collector voltage will approach V_{CC}. Capacitors C_2 and C_3 form capacitive voltage-divider, but C_3 apparent = C_3 actual $(\beta + 1)$, where β is the current amplification factor of Q_2. The charge which

flows into C_3 is $(\beta + 1)$ times the charge which flows out of C_2. When the input pulse is removed, the collector voltage of Q_1 returns to zero in a time determined by R_2. The charge which must flow back into C_2 flows from C_3 through D_1 and is approximately equal to the charge which was forced into the base of Q_2. The net charge left in C_3 is β times the charge from C_2.

Assuming that the voltage step across C_3 is small compared to supply voltage, this voltage increase,

$$E_{step} = \frac{\beta \times C_2 \times V_{CC}}{C_3}$$

$C_2 \times V_{CC}$. This relationship holds for all values of voltage across C_3 until the voltage across Q_2 is less than 1 V.

Positive pulses into terminal B cause exactly the same action, via Q_3, C_5 and Q_4, but in the opposite direction. Coincident pulses cancel, so this counter can add and subtract simultaneously. FET Q_5, is an emitter follower, which prevents loading of C_3.

The counter can be reset to zero by clamping the base of Q_2 to the positive supply bus, or the base of Q_4 to the reference bus. This circuit can also be used as a net frequency indicator by shunting C_3 with a resistor. The average output voltage will then be proportional to the frequency of pulses at A less the frequency at B.

Inexpensive UJT-SCR Intervalometer

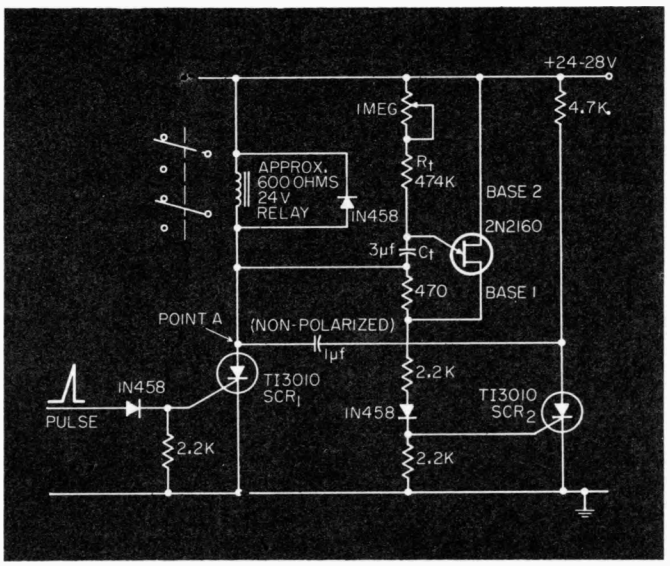
OFTEN A CIRCUIT is required that operates at the end of a pre-determined period for a second pre-determined period (unlike the time delay relay, which merely switches on or off). A monostable multivibrator will do this, but for time periods more than about 4 sec the timing capacitor becomes bulky, since it is not feasible circuit-wise to have the timing resistor large in transistor MV circuits.

A transistor MV, for 5 sec, requires about 500 μf. The circuit shown, however, works with small values of timing capacitor, here 3 μf, low standby current (5 mA) and with the values of R_t shown, gives time periods from below 5 to near 10 sec. Longer periods are easily obtainable.

Circuit operation is based on the familiar SCR with commutator capacitor for switching "other off" connected anode-to-anode. When power is first applied, SCR_2 is switched to conduction by the voltage-divider action of the relay coil through the 2.2-K resistors to ground. The voltage at the gate is about 0.75 V. The unijunction base 1 is at nearly the same potential as base 2, since point A is near supply potential. Thus, the unijunction does not conduct.

When a trigger pulse is fed to the SCR_1 gate, it is turned on and commutates SCR_2 off. The unijunction base-1 circuitry is now near ground potential. SCR_2 loses its 0.75-V gate signal since point A is near ground. The unijunction now functions as a familiar pulse generator.

The first pulse triggers SCR_2, which commutates SCR_1 off, and the circuit is once again in standby, awaiting the next signal pulse. Other uses can be obtained by replacing the relay coil with a different type of load. Total cost of the SCRs and UJT shown is $4.95.



Low-cost intervalometer using unijunction transistor and two SCRs.

Stable clock oscillators are DTL/TTL compatible

THESE TWO crystal oscillators provide stable clock sources that are completely compatible with DTL and TTL ICs. The circuits operate from a single +5 Vdc power line and have a minimum number of component parts. Over the temperature range 0 to +70°C, frequency stability of each circuit approaches that of the crystal alone.

The circuit shown in Fig. 1 generates a 1-MHz clock signal, while that shown in Fig. 2 is designed for 100-kHz operation. Fig. 3 shows the temperature drifts of both oscil-

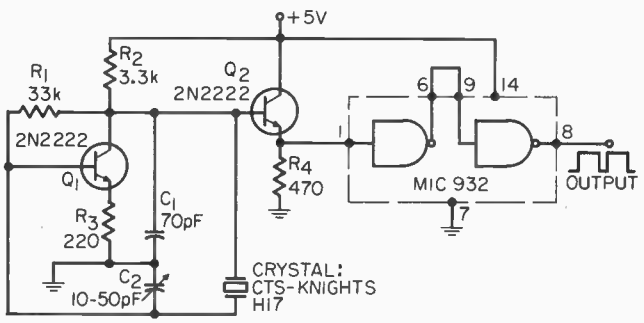


Fig. 1. Simple 1-MHz clock oscillator operates from +5 V supply and gives output levels compatible with digital ICs.

lators. Drift is well within the ±50 ppm expected from the specified crystals. Supply-voltage susceptibility is good too. Changing the supply voltage from 4.5 to 5.5 V produces a frequency change of less than ±3 ppm at all temperatures.

Both circuits use a Colpitts type feedback configuration that doesn't need inductors. The circuits are designed for parallel-resonant crystals that require 32-pF nominal shunt capacitance.

In the 1-MHz circuit, feedback capacitors C_1 and C_2 provide the necessary shunt capacitance. In the 100-kHz circuit, on the other hand, the values of C_1 and C_2 needed for oscillation are much higher. So an extra capacitor C_3 is added to give the necessary shunt capacitance.

Emitter follower stage Q_2 and a 932 DTL buffer gate complete the circuit. The wavform at Q_2 emitter is a sine wave with the bottom clipped. The two buffer gates, in series, amplify and clip the signal to produce a square wave with rise and fall times of less than 50 ns.

Some adjustment of R_3 may be necessary to achieve a symmetrical output square wave. With the specified IC gate, the circuit will drive up to 25 DTL loads or 12 TTL loads.

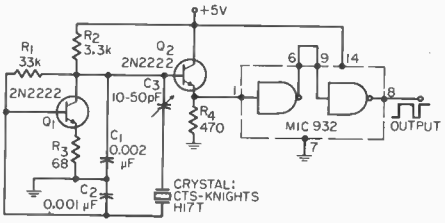


Fig. 2. For lower frequencies, as in this 100-kHz circuit, an additional capacitor C_3 is needed to provide the correct shunt capacitance for the crystal.

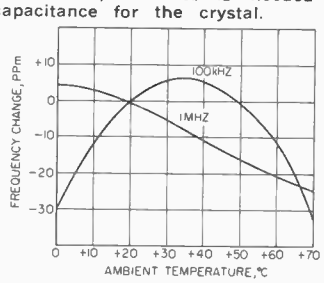


Fig. 3. Frequency varies less than ± 30 ppm over the temperature range 0 to +70°C. Stability is determined primarily by the crystal.

Low-power timer drives stepping relay

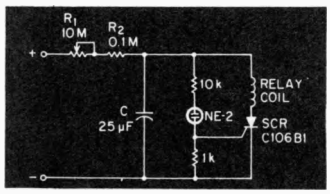
THE EXTREMELY low forward-blocking current of some SCRs (for example, GE's C106B, with $I_{fx} \simeq 0.1\ \mu A$) allows the design of inexpensive timing circuits which can drive inductive loads (such as stepping relays), yet which require a minimum of continuous power.

The circuit shown has a current drain of only 25 µA when cycling at 1 pulse/min. This allows battery operation in portable applications. For dc operation, a 90-V battery is suitable. Alternatively. the circuit will work directly from rectified ac (half-wave or full-wave), using a 110-V line.

Timing depends on the supply voltage as well as on the RC time-constant. With the component values shown (R = 10 MΩ, C = 25 µF), the circuit cycles at 5-minute intervals using a 90-V battery, or at 10-minute intervals using half-wave rectified ac. For optimum efficiency and timing accuracy, a low-leakage capacitor should be used.

Circuit operation is extremely simple. Capacitor C charges from the supply line via resistors R_1 and R_2. When the capacitor has charged to around 65 V, the neon fires and triggers the SCR. The charge on the capacitor is dumped through the relay coil, activating the relay. The discharged capacitor then starts to recharge, commencing a new cycle. Resistor R_1 allows adjustment of the cycling rate, while resistor R_2 determines the minimum cycle period.

In addition to its efficiency, the circuit has other advantages. the SCR is self-commuting — no special turnoff circuitry is needed. The circuit reliably drives inductive loads



This timing and driver circuit for stepping relays offers high efficiency, provided a low-leakage capacitor and SCR are used.

— the trigger signal is present until the SCR is fully conducting. Recycle time can be very short — the capacitor is discharged through the SCR and not through the neon or through a resistor.

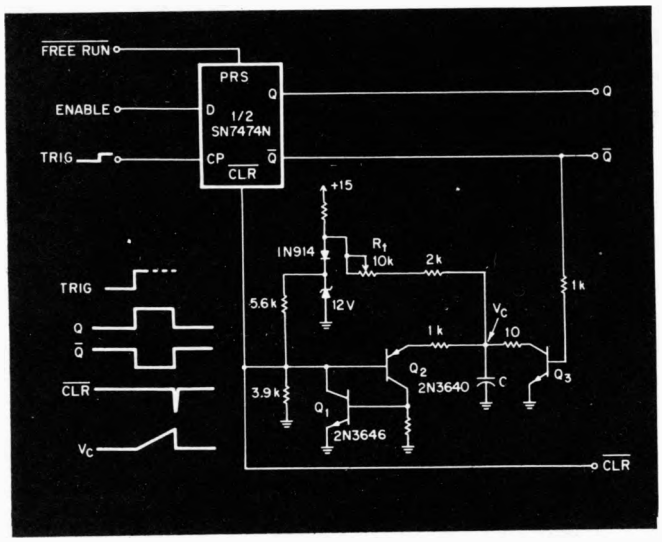
Versatile timer

THE CIRCUIT shown functions as a one-shot, variable pulse delay or oscillator. Stability with temperature and supply-voltage variations is excellent. Recovery time is extremely short, allowing duty cycles to about 98%.

For one-shot action the D and *PRESET* inputs of the integrated flip-flop are held at logic 1. A positive-going edge at the *CP* input triggers it to the set state. When the timing capacitor C charges sufficiently to turn on Q_2, Q_1 and Q_2 switch on, clearing the flip-flop. This turns on Q_3 which discharges C and holds it at 0 V until the flip-flop is again triggered.

The clear pulse or "Time Out Pulse" at the collector of Q_1 is useful since it occurs at the trailing edge of the output pulse. The circuit is thus useful for pulse delay. One-shot action is disabled if the D input is held at logic O. R_f allows a 4-to-1 adjustment of output pulse width.

With R_f set at mid-range, the

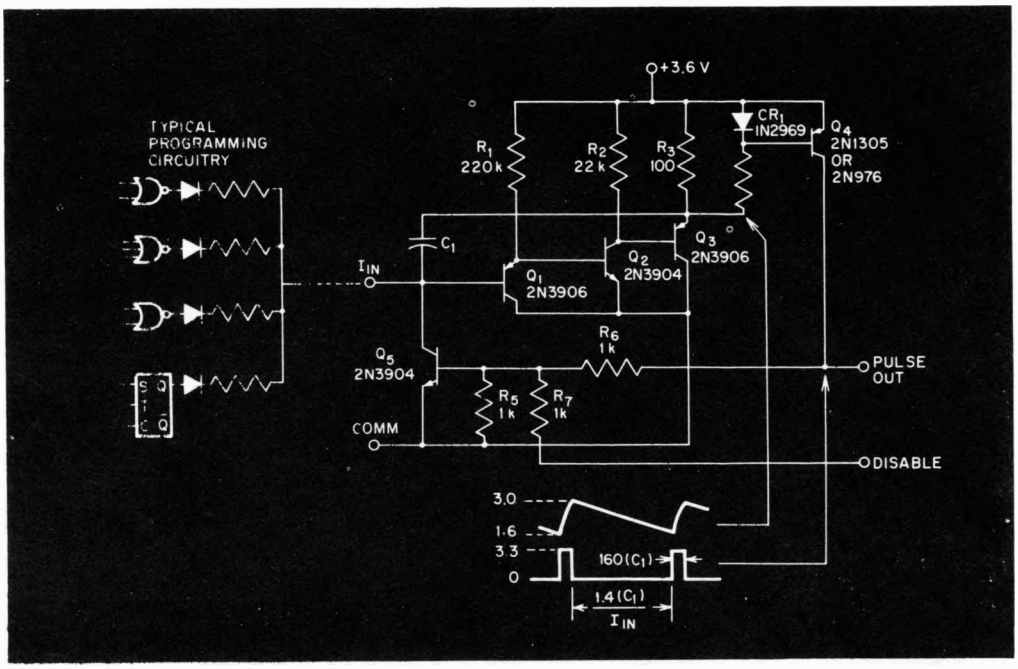


This highly stable circuit can be used as a one-shot, variable pulse delay or oscillator.

time-out period t equals $3.4 \times 10^{3}C$. Conversely, $C = 0.29 \times 10^{-3}t$.

If the *PRESET* input is held at logic *0*, the circuit free-runs, making it useful as an oscillator. The zener assures good stability with supply-voltage variations. The series diode compensates the effects of temperature on V_{BE} of Q_2. The zener and diode with series resistor supply four complete timing circuits.

Wide-range programmable clock for low-voltage logic



This timing generator, operating at RTL levels, can be current programmed over a wide range.

INPUT-CURRENT changes can program the rep rate of this timing generator over four decades. Timing can be provided from less than one microsecond to more than a minute with a single capacitor change. The generator works with RTL (3.6-V) logic.

A positive input current from the programming logic is integrated by the integrator in the figure ($Q_1Q_2Q_3$). A negative ramp appears across C_1.

When sufficient current has been integrated, the current through R_4 switches tunnel diode CR_1 to its high state and turns on Q_4. The output pulse generated by this turn-on drives Q_5 deep into saturation.

The timing capacitor C_1 now recharges through Q_5 and R_3R_4 until the tunnel diode returns to its low state. At this time, both Q_4 and Q_5 turn off and a new integration cycle starts.

The period between pulses is determined by the input-current integrated by C_1 and the output pulse width is primarily determined by the R_3C_1 time constant.

The generator free runs at a slow rate from the effect of input offset current (about 0.2 μA). Free running can be stopped by either opposing the offset current with a negative current of larger value or supplying a disable input to the reset transistor. For time-delay applications, either the input current can be switched on or the disable removed. The magnitude of offset current is of little consequence if the generator is free running. The input-voltage offset is about 60 mV. Both offset current and voltage remain constant during the integration cycle.

The rise and fall time of the ouput pulse is independent of the timing selected. They are determined by the switching characteristics of Q_4. The output pulse width is also independent of input current. In applications which do not require wide rate range (less than 3 decades), the circuit can be simplified by deleting Q_3, R_3, R_2, changing R_1 to 47 kΩ, and connecting R_4-C_1 to Q_2's collector. Power consumption of this version is about 4 mW.

This circuit was used for a system clock which operated at several rates between 2Hz and 10 kHz as determined by logic

programming. This rate variation was obtained with a 47 nF capacitor for C_1 and various resistances (2.7 kΩ to 50 MΩ) and series diodes switched by logic elements. The circuit was also used with a 47-μF capacitor to generate one-minute time pulses and with a 47-pF capacitor for a 2-MHz conversion oscillator for a pulse-width ADC.

Preliminary tests indicate about 1% linearity of current-to-frequency conversion from 0.1 to 100 μA which suggests additional applications as a ramp generator and current-to-frequency converter.

Single capacitor converts TTL gates into one-shot

DIGITAL SYSTEMS, with TTL ICs, frequently require fixed delay elements. Often, delay lines are impractical because they are too bulky, or because they don't give the necessary fine increments. In these cases a one-shot multivibrator can be used, provided it doesn't need too many discrete components. The circuit shown in Fig. 1 uses only two IC packages and a discrete timing capacitor to produce a versatile one-shot.

Sylvania's SG120- series SUHL gates have an additional output lead for use with gate expanders. Turn-on delay of the gate depends on the capacitance between the expander terminal and ground. According to the manufacturer's data sheet, delay varies over a range of 125 ns for a capacitance change of 30 pF.

In the one-shot circuit of Fig. 1, capacitor C_T loads terminal m of gate A_3 to give the required delay. Gates A_1 and A_2 are cross-coupled to form a simple S-R flip-flop, capable of being set by a negative pulse or step at the input. The steady-state condition is with the input high. Then gate A_2 is low and gates A_3 and A_1 are high.

When the flip-flop is set by a negative-going input, A_2 goes to the high state thus forcing A_1 low and allowing C_T to begin charging. Gate A_3 is still high. When C_T charges to approximately twice the base-emitter drop of the gate junctions, A_3 goes low, causing the output of A_1 to return to the high state.

The flip-flop will not reset until the input has returned to the high state. However, provided the input is a narrow pulse that returns to the high state during the timing interval, the flip-flop will reset as soon as A_3 goes to the low state. In Fig. 2, the solid lines show the normal mode of operation and the dashed lines show what would happen if the input remained low after completion of the one-shot period.

When the input returns to the high state, the flip-flop resets, discharging C_T in preparation for the next cycle. Recovery time depends on this discharge, thus it is proportional to the value of C_T.

For proper circuit operation, the input must remain negative long enough to set the flip-flop (at least 20 ns). Also, A_1 must not be too heavily loaded or the circuit will not reset. For greater versatility, the two unused gates in the SG143 can be connected in series to buffer the output of the one-shot. This arrangement will produce push-pull positive and negative outputs and will avoid loading problems.

Delay period can be adjusted by varying either C_T or the charging current. To vary the current, one can either adjust the supply voltage to A_3, or one can add a resistor (at least 1 kΩ) from pin-I to pin-D of A_3.

The circuit has the disadvantages that period depends on supply voltage and ambient temperature. For precise fixed delays, it will be necessary to use a well regulated power supply and possibly some form of temperature control too.

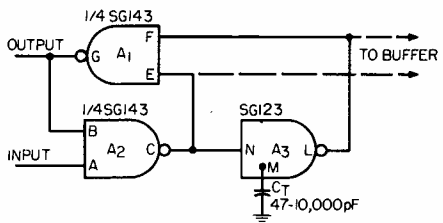


Fig. 1. Unusual one-shot multivibrator exploits the inherent delay of a SUHL SG120-series gate when its expander terminal is capacitively loaded.

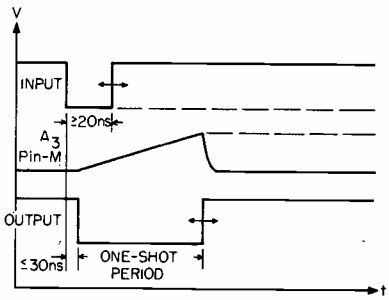


Fig. 2. The input pulse must return to the high state before completion of the delay period. If it does not, the capacitor won't be discharged in preparation for a new cycle.

Simple analog delay

A SINGLE low-Q inductor can provide long delays of analog signals, retaining amplitude information, where the bandwidth requirement is small. The patented circuit, in Fig. 1, uses a buffer-driven, tuned, RLC network.

A positive input excursion causes the tuned circuit to produce a positive voltage recovery swing the moment the input voltage returns to zero. The RLC network is sufficiently damped to provide only one significant recovery transient. The first recovery tends to be a function of LC network's center frequency.

The resonant frequency of the network can be determined from

$$f = \frac{\sqrt{\frac{1}{LC} - \frac{1}{4R^2C^2}}}{2\pi}$$

The procedure is to establish the R at a value sufficiently above the value $\sqrt{L/4C}$ to give a substantial first-recovery swing, but sufficiently close to damp out all the subsequent transients.

The output of the tuned network is amplified through a non-inverting amplifier. An adaptive clamp removes unwanted excursions from the output and enhances the dynamic range. The adaptive

clamp anticipates the first positive recovery amplitude since the negatively driven pulse discharges C_2, thereby lowering the negative clamping level. Changes in clamping also tend to vary the width of the output pulse. With longer-duration inputs the output pulse tends to lengthen, helping to improve frequency response.

The time constant of the clamp is about equal to twice the reciprocal of the center frequency of the RLC network. The circuit has a dynamic range over which the output amplitude follows the input amplitude linearly of about 30 dB. A greater range is possible

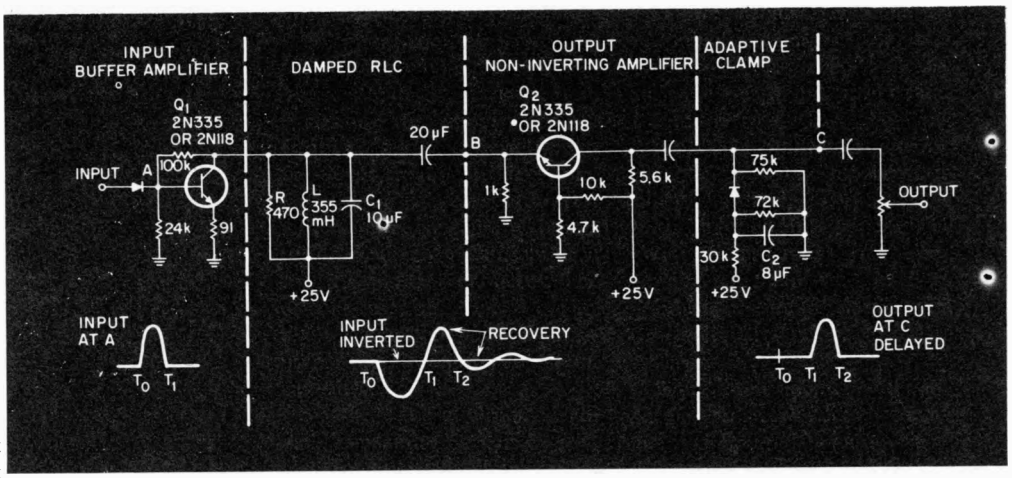


Fig. 1. With the component values shown, this circuit (positive-input version) provides 6-ms delay over a 25 to 150-Hz frequency range. The output follows the input over a 30-dB range.

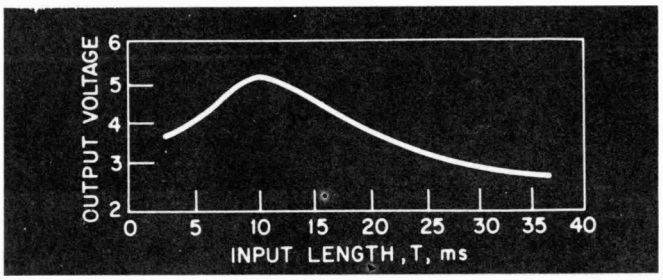


Fig. 2. Typical delay-circuit output as a function of input pulse length

direction so the output is like with some distortion. Delay is about 6 ms.

The output is within the 3-dB points over a range from 25 to 150 Hz. Fig. 2 shows the output response as a function of the input signal length.

The delay circuit is unipolar; it accepts inputs of only one that of a half-wave rectifier. A full-wave delay requires two units with some provision for 180° phase inversion.

The circuit can be stacked in series to provide longer delays and taps can be provided to select delay points.

Voltage- or pot-variable 400-Hz delay

THE CIRCUIT in Fig. 1 provides delays variable from 0 to 2.5 ms as a function of control voltage or potentiometer adjustment. The delay is controlled by the R_1-R_7 divider or by a dc control voltage in its place.

The circuit senses and delays the positive excursion of an input 400-Hz square wave. The delayed signal triggers a 1.25-ms one-shot so the output looks like the original square wave, delayed.

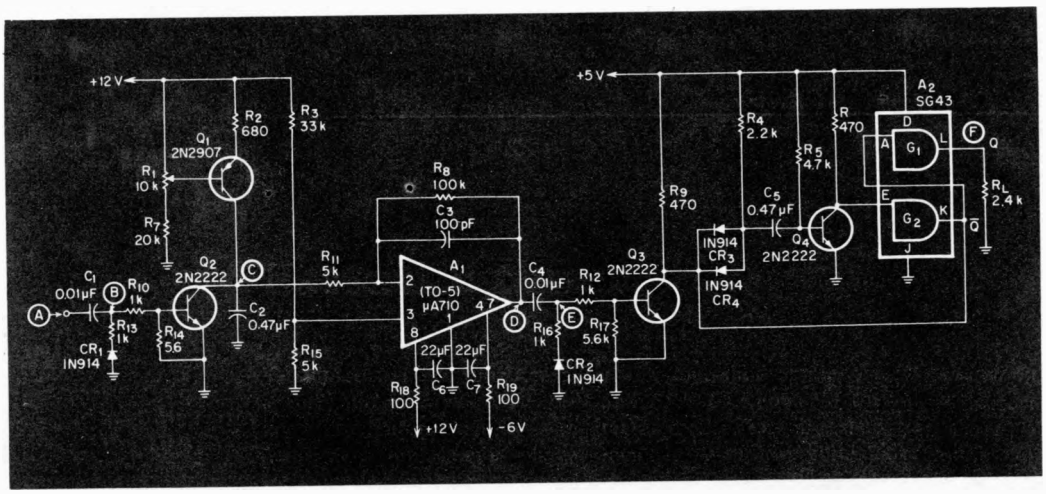


Fig. 1. This circuit provides variable apparent delay for a 400-Hz square wave, but it actually "reconstructs" the square wave.

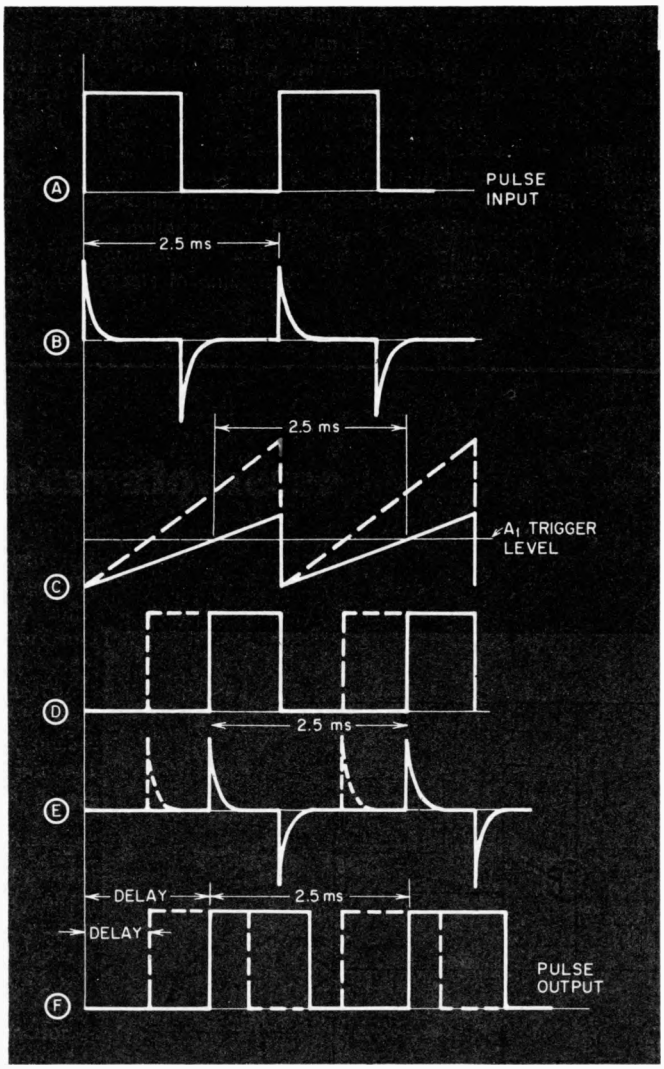


Fig. 2. Waveforms at key points in the delay circuit

When the input goes positive, Q_2 turns on and discharges C_2. Negative excursions are bypassed by CR_1. When the input goes low at the end of the positive excursion, voltage comparator A_1 senses the low voltage and its output goes low. C_2 begins to charge through the variable current source ($R_1R_7R_2Q_1$), which determines the slope of the charging curve.

When the voltage across C_2 reaches the trigger level of A_1, its output goes high. The high-going signal turns on Q_3, which triggers the 1.25-ms one-shot.

The same cycle is repeated, producing an apparent delay of the input signal. The transistors used are fast switches. The μA710 is a differential comparator with fast response and high accuracy. The one-shot uses standard SUHL gates.

Modulo -4 or -10 counter

A MODULO-10 asynchronous counter can be built with four JK flip-flops and two gates as shown in the figure (neglecting the dashed lines). The counter counts in a normal BCD fashion as shown in Table 1. If the frequency of the incoming clock is f_1, flip-flop FF_4 counts at $f_1/10$ and provides the carry input to the next stage of a counter, if required.

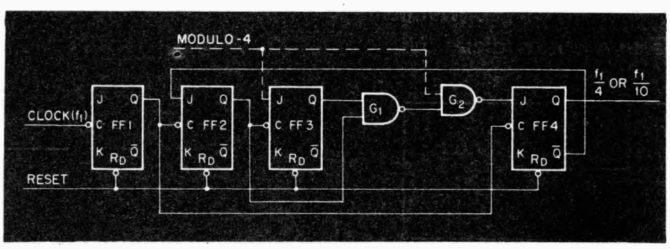
Table 1. Flip-flop counting states when the wires shown in dashed lines in the figure are removed or when a "1" is applied to the "Modulo-4" input.

FF1	FF2	FF3	FF4
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
1	0	0	1
0	0	0	0

Table 2. Counting states when a "0" is applied to the "Modulo-4" input.

FF1	FF2	FF3	FF4
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	1
0	0	0	0

However, by adding two wires (dashed lines), we get either a modulo-4 or -10 depending on the level of a control signal designated *Modulo-4*. If the *Modulo-4* signal is at a logic "0" level, the modulo is 4, as in Table 2, which shows the counting pattern when the *Modulo-4* signal is logic "0." When the *Modulo-4* signal is "1," the modulo is 10.



This is a modulo-10 counter when a "1" signal is applied to the "Modulo-4" input, and a modulo-4 counter when a "O" is applied there.

If the *Modulo-4* signal = "0," FF_3 is inhibited from toggling to the Q = "1" state. Also, since the output of G_2 = "1" in this configuration, FF_4 becomes merely a toggle flip-flop. Since FF_4's clock is FF_1 ($=f_1/2$), flip-flop FF_4 counts at $f_1/4$.

Whether the counter is modulo-4 or -10, FF_4 is the carry to the next stage of a counter. Also, since FF_3 does not count in the modulo-4 condition, the modulo of the counter can be logically switched each cycle (4 or 10 counts) without requiring clocks to resync the counter. ■

Combined shift-register clock driver and power supply

In systems using a small number of MOS-shift registers, in conjunction with TTL or DTL logic, the shift registers may be the only components requiring a negative supply and a 2-phase clock. The cost of this extra supply may be saved by using the pulse-transformer clock driver shown in Fig. 1.

In Fig. 1, both clock phases, ϕ_1 and ϕ_2, and the negative supply for the shift register, V_{DD}, are generated by an external TTL or DTL clock. The clock-driver power supply operates from a 5 V supply.

For phase 1 clock pulses, Q_1 is driven into conduction. Q_2, normally held on by R_2, is cut off by the signal coupled through C_1. At the same time, a negative pulse from the transformer (T_1) secondary drives clock line ϕ_1, negative via diode D_1. When the output of the TTL gate driving Q_1 goes low, Q_1 is cut off and Q_2 is turned on by C_1. This sequence causes the clock line (ϕ_1) to be returned to +5 V and completes a ϕ_1-clock pulse cycle. At the same time the clock pulse is generated, D_2 charges C_3 producing the negative supply voltage V_{DD}.

The ϕ_2 circuit consisting of Q_3, Q_4, T_2, D_3 and D_4 is identical to the ϕ_1-clock section. The ϕ_2 circuit also contributes to V_{DD}.

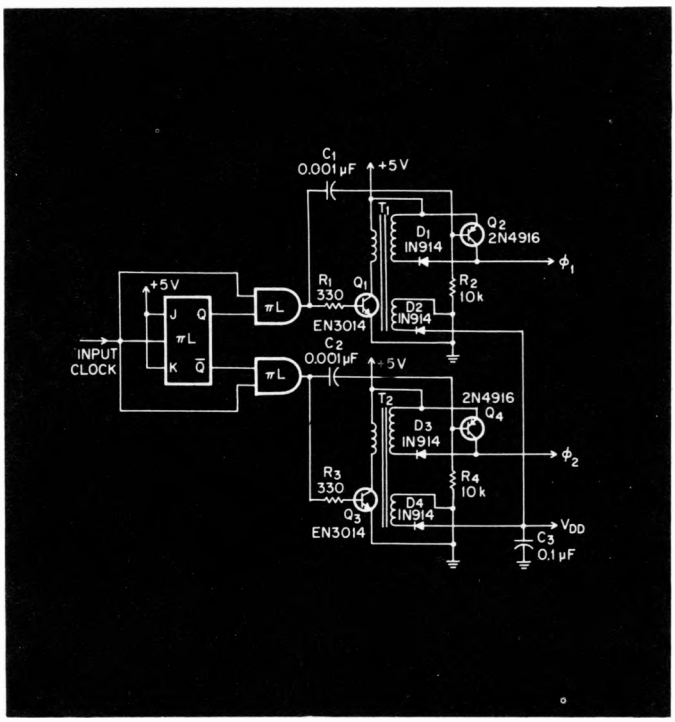


Fig. 1. This circuit supplies a two-phase clock voltage and a negative supply for MOS-shift registers. It interfaces with DTL-TTL logic and only requires +5 V.

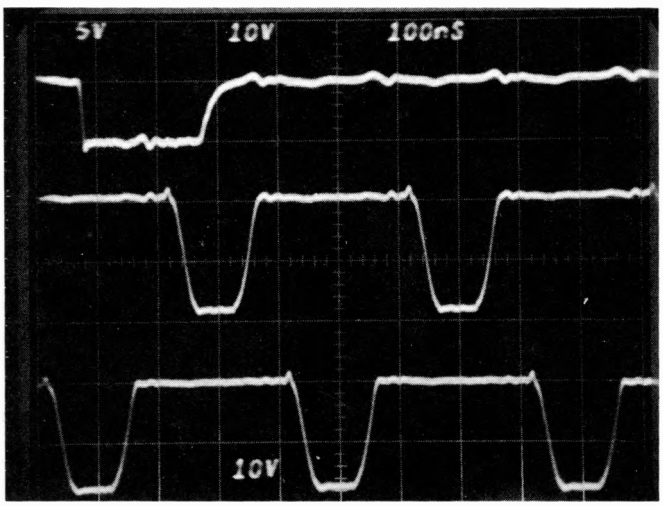


Fig. 2. In the photo, the top trace is data output and the next two traces are the two-phase clock signals. Data rate is 5 MHz and clock rate is 2.5 MHz.

For the widest frequency of operation, no loads other than shift registers (MOS) should be operated from V_{DD}. Shift registers draw current only during clock pulses, so that effective loading of each clock pulse remains independent of frequency.

This circuit has been operated without change of pulse width from a 40-Hz to 5-MHz data rate (clock rates of 20 Hz to 2.5 MHz). without loss of stored data. Fig. 2 is a photograph of waveforms in a typical circuit for driving two Intel 1402-type shift registers.

Each transformer consists of a 5-turn primary, a 15-turn secondary (V_{DD}) and a 8-turn secondary (V_{DD}) wound on a Magnetic Inc. D41408-UGX73 cup core.

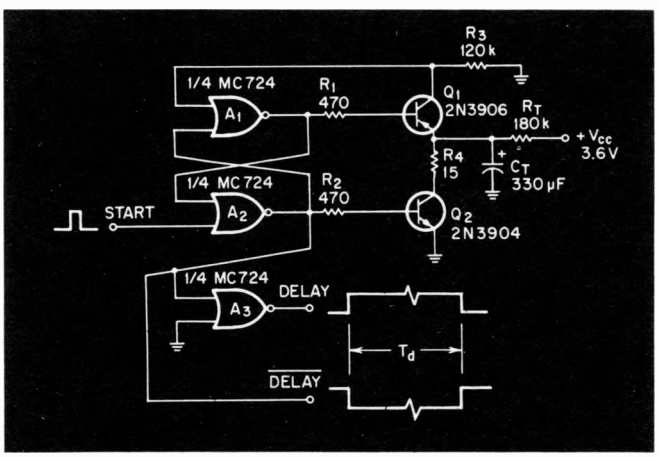
Long-delay timer

Producing long delays using the low voltage from which ICs operate can be difficult. The circuit shown provides delays up to more than one minute.

The delay period commences when a start pulse is applied to the R-S flip-flop formed by A_1 and A_2. Q_2 turns off, allowing R_T to provide charging current for the timing capacitor C_T. When the voltage across C_T exceeds the V_{be} of Q_1 plus the level set at its base by the IC, Q_1 turns on, resetting the flip-flop, and terminating the delay period.

With a V_{cc} of 3.6 V the delay time $T_d = R_T C_T$ and, with the values given, T_d equals 60 seconds. Resistor R_3 is used to provide some noise immunity, but it may be omitted if noise is not a problem. If used, R_3 should equal 0.7 R_T to guarantee proper reset action.

Since loading A_1's output will greatly affect the delay period, A_3 is used to provide a buffered complementary output. ■



This circuit provides long delays, even with the low voltages used for ICs.

Section 11

TEST & MEASUREMENT CIRCUITS

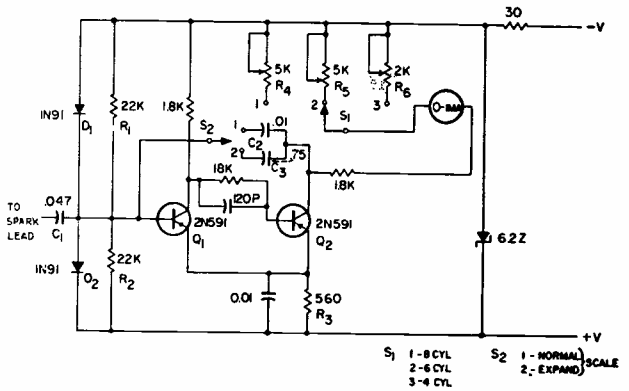
Accurate Engine Tachometer

THIS HIGHLY stable accurate tachometer is designed for use with engines using any battery voltage may have 4, 6, or 8 cylinders.

The circuit is basically a single-shot multivibrator with a meter movement in the collector circuit of the normally-off transistor. Diodes D_1 and D_2 clamp the input voltages to the battery supply to prevent input voltage spikes from harming transistor Q_1. Resistors R_1 and R_2 form a bias network to keep transistor Q_1 turned on. When Q_1 is in conduction, a voltage is produced across R_3 which keeps Q_2 cut off. Any input pulse will be passed through C_1 which establishes an ac reference point and the positive component of this pulse will cut off transistor Q_1. This, in turn, turns on the transistor Q_2 for a time determined by the value of C_2 or C_3 and R_2. A single pole double throw momentary switch allows the meter scale to be expanded by a factor of 10, and inertia of the meter movement allows the pulsing dc current to be averaged. Switch S_1, a single-pole three-contact rotary, is used to switch the meter movement through one of three calibration potentiometers corresponding to 4, 6, or 8 cylinders. A 10 w, 6.2 v zener diode regulates collector supply voltage so that meter readings will be independent of supply voltage.

A clip lead connected to C_1 is attached to the center high-voltage lead of the distributor, and the battery connected to the plus and minus supply leads. Care must be exercised that no direct connection is made to the high voltage but merely a capacitive coupling is achieved.

The meter used can be marked off in any suitable scale divisions from 0 to 3,000 rpm, or 0 to 10,000 rpm. A linear scale is used for this purpose. The author used a 0-1 ma movement and retained the



Circuit of expanded scale tachometer.

original scale markings to indicate 0 to 10,000 rpm. Calibration of the meter can be obtained on each scale by attaching a 60 cps, 110 v signal across the input and adjusting calibration resistor R_4 (8 cyl) for a meter reading of 900 rpm (the scale expansion switch may be used for this purpose), adjusting calibration resistor R_5 (6 cyl) for a meter reading of 1200 rpm, and R_6 (4 cyl) for a meter reading of 1800 rpm.

A 1 K resistor can be used in place of R_5 for use with 2 cyl. outboard engines and a flashlight battery supply may be used as a power supply. Calibration for this engine using 60 cps would be 1800 rpm.

Direct-Reading DC Beta Tester

THE INSTRUMENT here described gives a direct reading of the dc current amplification factor of the transistor (just saturated) being tested.

The transistor operates in the antisaturation circuit of Fig. 1. When the transistor is saturated, or near saturated, the voltage drop from collector to emitter will be less than the voltage drop over D_2

plus the emitter-base diode of the transistor, and a current will flow via D_1, until the base current is just great enough to keep the transistor so near bottoming, that the voltage drop over D_1 plus collector to emitter equals that of D_2 plus emitter-base.

Figure 2 shows the tester circuit used in our laboratory. It shows beta in the range 9-100 at a collector current of 10-11 ma. The meter will show full-scale reading if beta is 9 or less, and zero if the beta is 100 or higher.

Resistor R_3 is added to give the upper limit of beta. It adds a base current which does not flow through the meter, but which is great enough to saturate the transistor if beta is 100 or higher. It also reduces the influence of the I_{cbo} of the transistor, so that I_{cbo} of 10 μa only gives an error of 10 per cent if beta is 100 (or 1 per cent if beta is 10).

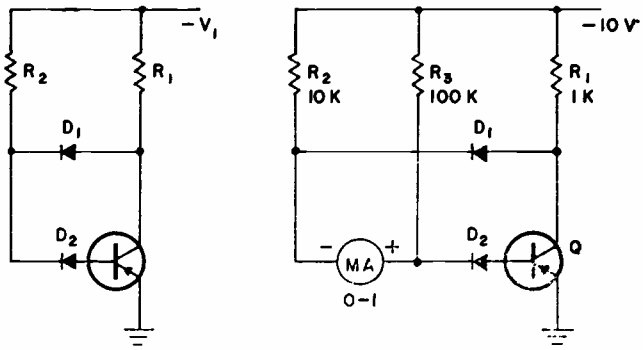


FIG. 1—Antisaturation circuit and Fig. 2 (right) complete circuit of beta tester. A Philips goldbonded Ge OA5 is used for D_1 and a Philips Si OA200 for D_2.

Between the outer limits beta can be calculated from the following formula

$$\text{Beta} = \frac{1/R_1 + (1-M)/R_2}{M/R_2 + 1/R_3}$$

Where M is the meter reading 0 to 1.
Or the meter may be calibrated to show beta directly by this formula. If a linear scale of beta is wanted, it is necessary to use an instrument which is most sensitive at small currents.

Checking Tracking of Stereo Controls

A STEREO loudness or volume control is usually a tandem control which consists of two controls ganged together and operated by a common shaft. Manufacturers of stereo equipment have suggested standards for db tracking of stereo loudness controls. The most liberal of these specifications is 5-db tracking between the front and rear controls at the —55 db down position. The most difficult specification is 2-db tracking between the front and rear section from 0 to —50 db and 4-db tracking from —50 to —60 db.

Designing a circuit to measure the difference in attenuation in db's between two controls involves many things. The dc could be applied to the two controls and the output voltages measured on vtvm's, but ratios would have to be calculated and converted to db's. The easiest method was to use an audio signal input and measure the output with an audio vtvm. To get the db difference in attenuation it was only necessary to subtract one meter reading from the other. The Ballantine audio vtvm (with 10 megohms input impedance) with direct reading scales of 0 to 20 db was found to be convenient for this test.

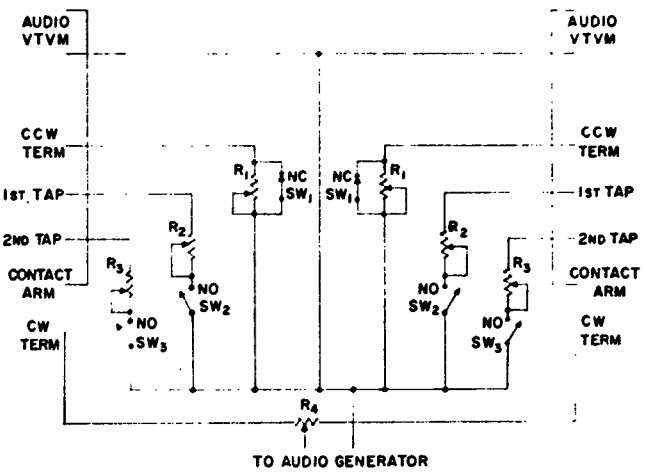


FIG. 1—Basic circuit for measuring tracking of stereo controls.

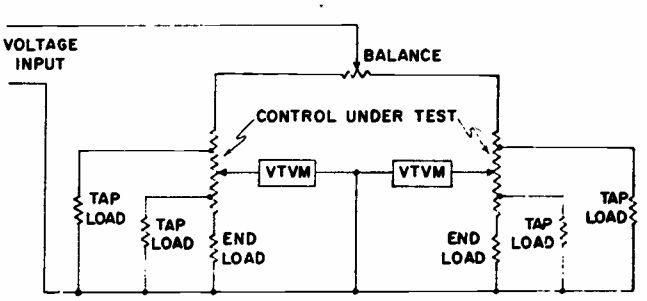


FIG. 2—Final circuit for measuring difference in attenuation between two tandem controls.

Another point to consider is end loading and tap loading of the controls. On a single tap control the usual tap load is 15 per cent of the overall resistance and on a double-tap control the tap loads are 5 and 15 per cent of the overall resistance. End loading, when specified, is usually 0.1 of 1 per cent of the overall resistance.

Figure 1 shows the basic circuit suggested by makers and users of stereo loudness controls. Figure 2 shows the actual circuit used in one laboratory for measuring the difference in attenuation in db's between two tandem mounted controls. If end load-

ing is desired SW_1 is opened and R_1 is adjusted to the desired value. If the 31 per cent tap is to be loaded, SW_2 is closed and R_2 is adjusted to the proper value. If the 69 percent tap is to be loaded, SW_3 is closed and R_3 is adjusted to the proper value.

The control under test is connected and the output of the audio generator is adjusted until the vtvm's read 10 volts. If it is desired to match the controls at the tap, R_4 is used to make the vtvm's read the same value, when the contact arms are set at the taps. The controls are then rotated from the clockwise to the counterclockwise and the readings are taken from the two vtvm's.

The readings are subtracted one from the other and the difference reading in db indicates how well the two controls are tracking. By adding db's as the attenuator switch is turned on the vtvm's, it is easy to find the —50 db and —60 db down points.

Relay Life Tests Monitored With Magnetic Amplifiers

MILITARY Specification MIL-R-5757 C, Paragraph 3.8.1, states in part, "Following the life test, the voltage drop shall not exceed 200 millivolts except that for contacts rated at 2 amperes or less, the contact resistance shall not exceed 0.10 ohm."

To automatically monitor the contact voltage drop of a relay during life test, the monitoring device must have an output (indicate contact failures) when its input is 200 mv or more. When its input is less than 200, the monitoring device must not have an output. In addition, the monitoring device must not have an output during the half cycle when the contacts of the relay under test are normally open. At that time, the contact voltage drop would normally be equal to the applied voltage; but the monitoring device must not indicate a failure of the contacts for this condition.

The requirements were met, through use of the circuit shown in Fig. 1, for a spdt relay. The principles involved can be extended to the testing of relays which contain more than one pole by duplicating the circuit shown for each additional pole.

The monitoring device was composed of a magnetic amplifier (Acromag type 761); an output relay (Potter & Brumfield, model PW5LS); and a means for calibrating and adjusting the device. The device was so adjusted that, with less than 200 mv input, the contacts of the output relay would be open (no output). With 200 mv input, the contacts of the output relay would close, and the output would be recorded to indicate a failure of the relay under test.

During normal operation the self-test-switch was set on position 2. The cam-operated switch, in series with the test relay coil, cycled the test relay with equal on and off pulses at a rate of 10 to 12 cycles per minute, as required by MIL-R-5757 C, Paragraph 4.6.15.

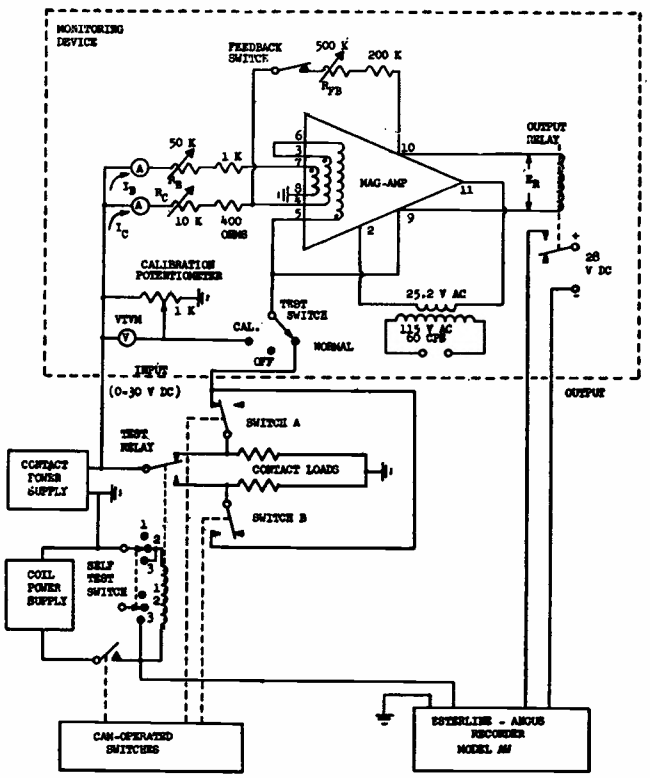


FIG. 1—Circuit for automatic monitoring of relay life tests.

Two other cam-operated switches, A and B, were used to switch the monitoring device from one set of contacts on the test relay to the other set at the proper time. These cams were adjusted such that switch B would close just after the test relay was energized and would open just before the test relay was de-energized. At all other times switch B was open. Switch A was operated in a similar manner.

With the self-test-switch set on position 1 and the cam-operated switches cycling on and off, a failure of the test relay was simulated on the normally open contacts. With the self-test-switch set on position 3, a failure was simulated on the normally closed contacts. This was done to check the monitoring device for proper operation.

The monitoring device was calibrated by turning off the test switch and adjusting the contact power supply to the rated voltage for the test relay. The calibration potentiometer was then adjusted to give a reading of 200 mv on the vtvm. The feedback switch was opened and variable resistors R_{FB}, R_B, and R_C were each adjusted to maximum value.

At this time the output from the monitoring device was 28 v, dc. R_B was decreased slowly until the output switched to zero. The feedback switch was then closed and R_{FB} was decreased slowly until the output switched back to 28 volts. R_{FB} was slowly increased until the output switched back again to zero.

The test switch was set at the calibrate position and R_C was slowly decreased until the output once more switched to 28 volts. The calibration potentio-

meter was then adjusted to give a reading of 190 mv on the vtvm. This caused the output to switch to zero. The calibration potentiometer was adjusted for a reading of 200 mv on the vtvm and the output switched back to 28 v, dc.

This completed the calibration of the monitoring device, and the test switch was set to normal. The self test switch was set to position 2; the coil power supply and the recorder were turned on; and the cam-operated switches were set in operation. The life test was underway. At regular intervals during the life test the monitoring device was checked for proper operation by setting the self-test-switch to position 1 or 3 in order to induce a failure indication as described.

Typical values for the variable resistors R_B, R_{FB}, R_C follow: $R_B = 15{,}000$, $R_{FB} = 130{,}000$, $R_C = 8{,}100$ ohms.

With the test switch in the calibrate position and the calibration potentiometer adjusted to give various vtvm readings, the values of control current (I_C), and of the voltage applied to the coil of the output relay (E_R) were as follows:

VTVM Reading	I_C	E_R DC
0	0	4 volts
190 mv	20 μa	4 volts
200 mv	23 μa	14 volts
30 volts	3.3 ma	18 volts

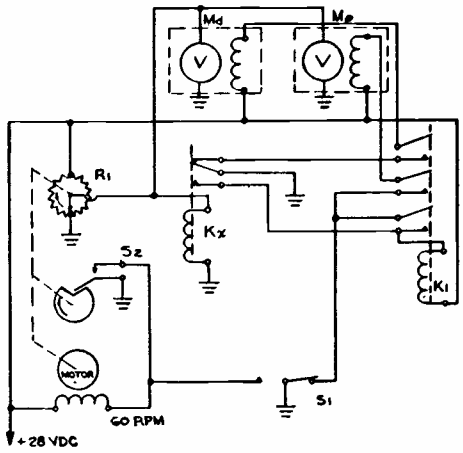
Since the coil of the output relay is rated at 14 v, dc, it will pull-in when the input to the monitoring device rises to 200 millivolts.

When it is desired to monitor contact resistance of contacts rated at 2 amperes or less, the circuit described may be used if the rated current is multiplied by the maximum allowable resistance (0.10 ohm) to obtain the maximum allowable voltage drop. The monitoring device must be calibrated to give an output when the contact voltage drop (input to the monitoring device) exceeds the specified limit.

Since the two control windings in the mag-amp contain a total of approximately 470 ohms, and the control windings will withstand a current of 50 ma; if the input voltage is limited to 30 volts maximum only 130 ohms are required in series with these windings. This gives a total of 600 ohms in the control circuit. Since approximately 23 μa control current is required to cause an output from the monitoring device, relays with contact ratings as low as 138 milliamperes can be monitored.

Relay Tester

IN any reliability program, one of the essential requirements of a relay tester is to determine the pick-up and drop-out voltages. This system was designed to afford a quantitative analysis of these two conditions in a matter of seconds. Repeatability characteristics are quickly and easily observed by this method.



Complete circuit of relay tester.

The schematic shows a motor-driven 360 degree continuous potentiometer, R_1, and K_x is the relay under test. The meters are memory type which use special solenoid-actuated mechanisms to permit the retention of a reading taken at any desired instant.

When S_1 is closed (momentary contact), the motor starts and the cam and microswitch S_2 keep the paralleled contact closed so that the motor will make one single revolution and stop. The potentiometer turns and varies the voltage applied to the relay coil, from zero through 28 volts and back down to zero. Both meters will follow the voltage variations.

Relay K_x will be energized at some given voltage, e.g. 14 volts. When K_1 is energized by the closing of K_x contacts, the holding coil of meter M_p is energized and the pick-up voltage reading is maintained.

Meter M_d continues to read up scale as the voltage increases to 28 volts and then starts down scale as the potentiometer goes through 180 degrees. When the drop-out voltage, e.g. 6 volts, is reached K_x drops out and since K_1 was latched-in by its own contacts, it does not open any circuits but provides the ground return for the holding coil of M_d which then maintains its readings.

Note that M_d was not actuated when the voltage originally went through the 6-volt point due to the fact that K_x had not as yet been energized.

These readings may be checked for repeatability by again closing S_1 or a new relay may be inserted for testing. Each time S_1 is pressed, K_1 is de-energized and reset.

Relay Chatter Detector

IMPORTANCE of reliable chatter-free relays in airborne electronic equipment is often overlooked. In most situations, current from primary power supplies must pass through at least one set of relay contacts before it reaches an electronic subsystem.

Chattering of these relay contacts can have serious

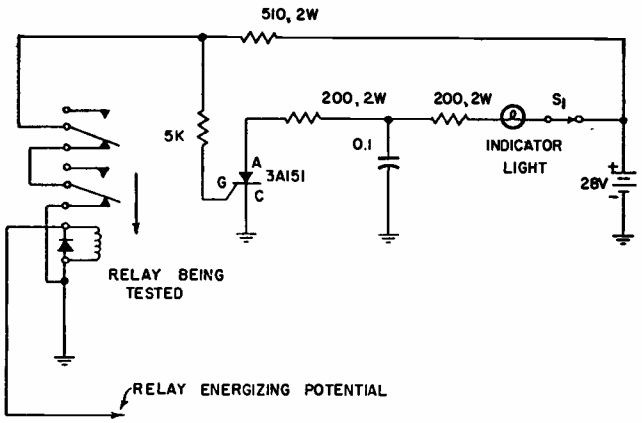


FIG. 1—Lamp lights if any relay contact opens for 0.1 microsecond.

consequences since many electronic circuits are sensitive to power supply fluctuations and transients.

False triggering of electronic switches and keying of transmitters are two examples of what relay chatter can do. Relay chatter can also produce large amounts of rf noise when the load is partially inductive.

To preclude having these chatter problems, relays can be tested under simulated flight conditions, and the inferior relays can be detected. A relay being tested is mounted on a mechanical vibrator and the circuit shown in Fig. 1 monitors the contacts for chatter if one contact opens for as long as 0.1μ sec, the 3A151 controlled rectifier is gated, causing the indicator light to come on.

Normally, the 3A151 gate-cathode junction has zero bias because it is shunted by the relay contacts. However, when one contact opens. the gate-cathode junction is forwarded biased by the 28-volt supply, causing the device to turn on ($t_{on}<0.1\mu$ sec). Once the 3A151 is on, the only way to turn it off is to interrupt its anode current; therefore, switch S_1 is provided to reset the monitoring circuit. A 3A151 is extremely sensitive, and it can be gated by applying its B+ through a switch as well as by an actual gating signal. To prevent this anode triggering, an RC filter consisting of a 200-ohm resistor and a 0.1-μ f capacitor is used to dampen switching transients. The other 200-ohm resistor's only function is limiting current.

This chatter monitoring technique has the advantages of fast response and explicit indication.

Fast Acting Subaudio Frequency Meter

A FREQUENCY MEASURING device was required that would provide a meter indication of frequencies in a range from 0.2 to 10 cps. In addition, the meter had to respond rapidly (preferably within 1 cycle) to changes in input frequency and without "bobbing" at low frequencies.

In the circuit developed to solve this problem, the input signal is fed through a conventional limiting and differentiating network and a bistable flip-flop so that it is converted into a square wave.

The instrument measures the period of the square wave, and this is indicated on a meter which is calibrated in units of frequency (such as pulses per minute).

Time interval is measured by measuring the voltage to which a capacitor charges during one-half cycle of the square wave.

By alternately charging each one of a pair of

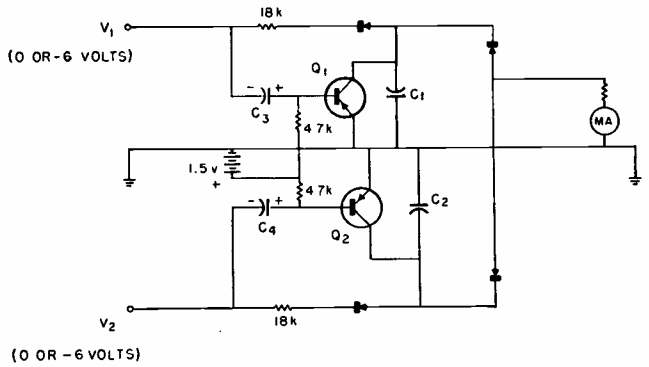


FIG. 1—Basic frequency measuring circuit.

capacitors, a steady voltage is maintained on the one which is connected to the meter while the other is charging. The means by which this is accomplished is as follows:

As shown in Fig. 1, two separate charge-discharge circuits are used, and the meter is connected to these through diodes so that it indicates the highest voltage of the two. This involves no time constants and insures rapid rise or fall of the meter reading if the rate should change.

Consider the circuit of Fig. 1, and the voltage waveforms of Fig. 2. Suppose initially that capacitor C_1 and C_2 are discharged, that V_1 is zero, and that C_3 is charged to 1.5 v in the polarity shown.

If then, V_1 is switched to —6 volts, C_3 rapidly charges to 6 volts through the emitter circuit of Q_1, and then continues to charge more slowly through the 4.7K resistor to 7.5 v cutting off tran-

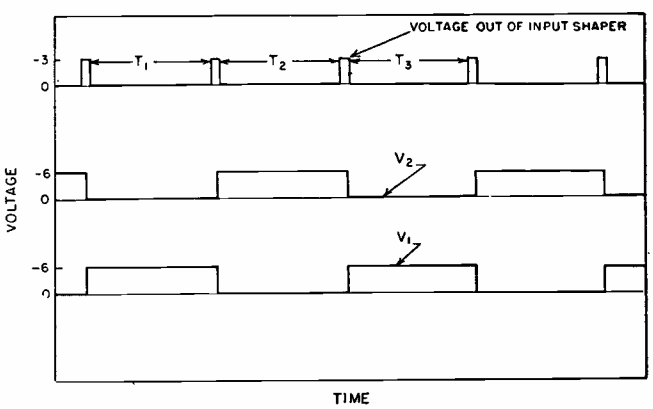


FIG. 2—Waveforms in frequency measuring circuits.

sistor Q_1.

As soon as Q_1 becomes cut off, C_1 begins to charge slowly through the 18K resistor, reaching a value v_1 depending on the time interval T_1. Voltage v_1 will then be indicated on the meter.

As the second pulse operates the flip-flop, V_1 becomes zero and V_2 is —6 volts charging C_2 to v_1 during T_2. During T_3 the meter reads the voltage across C_2 while C_1 is discharged by Q_1 and again charges to v_1.

Since each of the capacitors C_1 and C_2 is discharged by its shunting transistor at alternate states of the flip-flop, the voltage to which the capacitor is charged is dependent only on the present charging time and not on the previous one.

Fig. 3 shows a more complete circuit diagram with component values. With the values shown, the meter will provide a useful indication of frequency over the range from 0.2 to 10 cps. The frequency range can be changed by changing the time constant in the charging and discharging networks. An instrument built according to the circuit diagram of Fig. 4 was easily fitted into a standard meter case with its own battery supply. It will operate on pulsed or square wave inputs covering the range of 1 to 10 volts peak-to-peak. Increased accuracy and improved linearity can be obtained at the expense of additional circuit complexity.

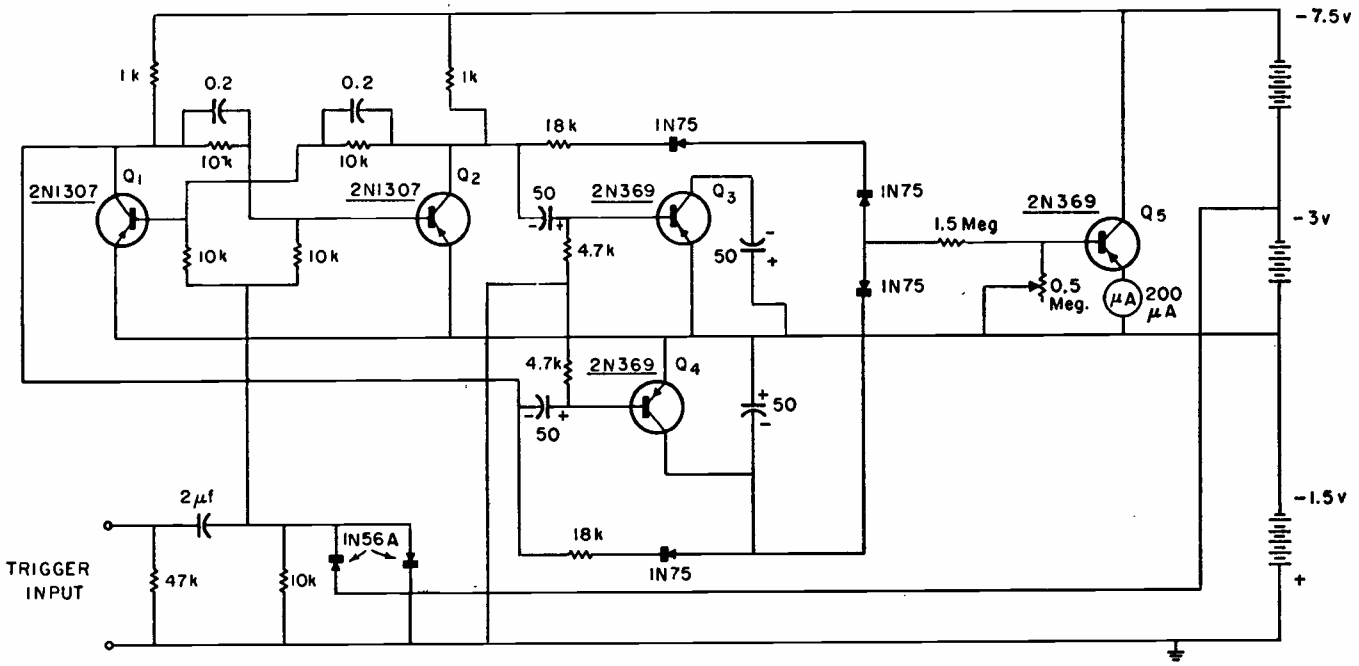


FIG. 3—Complete circuit for frequency meter for 0.2 to 10 cps.

Beta Tester

THE CIRCUITS shown in Fig. 1 and 2 are useful for measuring dc beta, or h_{FE}. The first finds its best application at low currents, where the effects of heating are negligible. The second is used at higher currents, where the use of short pulses keeps the power dissipation low.

The advantages of the two circuits are that they are very simple, accurate, easy to design, and give direct automatic read-out, due to feedback action.

Usually it is desired to know the base current at a given collector current and voltage. Of the three parameters, the accuracy to which the voltage is known is least important.

The current through R_2 is applied to the base of the first of the two amplifier transistors, in the Darlington compound configuration. This is amplified and finally applied, as I_B, to the base of the test transistor, T_t, which is driven on hard. However, T_t cannot saturate because of the voltage drop through the bases in series, and especially through the zener diode. That is, feedback action takes place such that if the test transistor were to tend towards saturation, this would tend to cut off the amplifier and reduce I_B, thus restoring the original condition. Finally a stable collector voltage is reached; this is given by:

$$V_{CE} = V_{BE(t)} + V_Z + V_{BE(1)} + V_{BE(2)}$$

It is apparent from this that since these voltages are a slight function of current, these components and their operating points must be chosen to keep this effect to a minimum.

For the currents, the following equations apply:

(1) $I_B = I_1[\alpha_1 + \alpha_2 - \alpha_1\alpha_2]$

$I_B = I_1[\alpha(2-\alpha)]$, for $\alpha_1 = \alpha_2$

$I_B \simeq I_1$ (within 1 percent, for α as low as 0.90)

or $I_B \simeq V_1/R_1$

(2) $I_O = I_2\,(1 - 1/\beta_1\,\beta_2\,\beta_3)$

$I_O = I_2\,(1 - 1/\beta^3)$ for $\beta_1 = \beta_2 = \beta_3$

$I_O \simeq I_2$ (within 0.1 percent for β as low as 10)

or $I_C \simeq (V_P - V_{CE})/R_2$
then $h_{FE} = I_C/I_B \simeq I_2/I_1$
min $h_{FE} \simeq R_1/R_2$

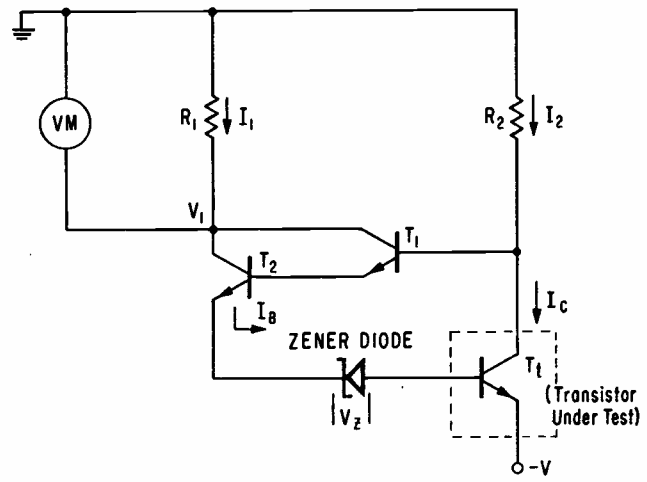


FIG. 1—Circuit for measuring dc beta at low current.

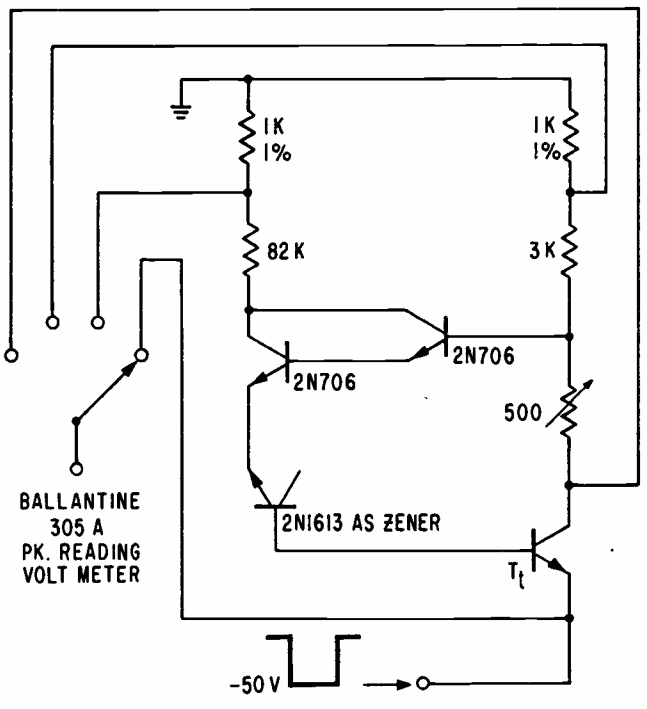


FIG. 2—Pulses permit measurements at higher current.

Figure 2 shows an actual design that has been found to operate quite satisfactorily. It is designed to test h_{FE} under the conditions V_{CE} = 10v, I_C = 10 ma.

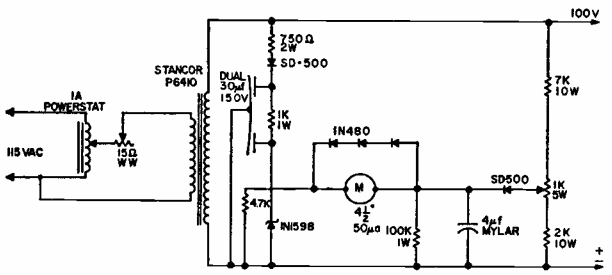
In practice, one plugs in a transistor and reads I_B. V_{CE} can be trimmed up with the 500-ohm pot for the first reading, and afterwards will remain constant with ± 5 percent. Note that if β is less than 20 the voltmeter will go no higher, since T_1 and T_2 saturate. This feature can be adapted to go-no-go testing.

The accuracy of h_{FE} measurement has been found to better than 5 percent for h_{FE} between 20 and 200. Since the accuracy of the peak reading meter was ± 5 percent, this was felt to be quite good.

Standardized AC Voltage Reference Source

THE ASSOCIATED circuit was developed to meet the need for an accurate 100 v ac rms source as the reference voltage for a divider to correlate vacuum tube voltmeters. A 4-1/2 in. 50 μa meter was mechanically made zero center and the scale numbering removed by erasure, after which − and + symbols were added with India ink to indicate voltages either side of 100.00.

The dc voltage on one side of the meter is held constant by a Zener diode, and is compared with voltage at the other terminal (+) which is obtained by divider action without stabilization protection. A diode rectifier and high quality Mylar capacitors insure consistent peak dc voltage to the meter. Initial output voltage standardization is done by adjusting the two input controls for an exact 100.00 v circuit output as determined with a reference standard. The 1000 ohm po-



100 vac reference supply.

tentiometer is then adjusted for zero center scale meter reading. Circuit sensitivity is such that a change of 1.825 v produces full scale deflection (25 divisions), which is the equivalent of 0.075 v per division and 0.075 percent. A low distortion line voltage regulator must be used to take full advantage of the circuit capabilities. The three diodes across the meter do not interfere with normal operation, but protect it against damage when the unit is turned on. The relatively low resistance across the Zener diodes performs a similar function when the unit is turned off. The 100 K resistor across the Mylar capacitors is the meter return to common when the output voltage is less than 100 v, since under this condition the more positive Zener voltage will not flow through the high reverse resistance of the meter diode. Wire wound resistors are used in the output voltage divider for stability.

Cable Harness Tester

THIS TEST SET will test continuity of wiring, connections to proper terminations, and shorting or shielding to any wiring. The test set is self testing and will also indicate the fault of any defective cable harness (does its own trouble shooting).

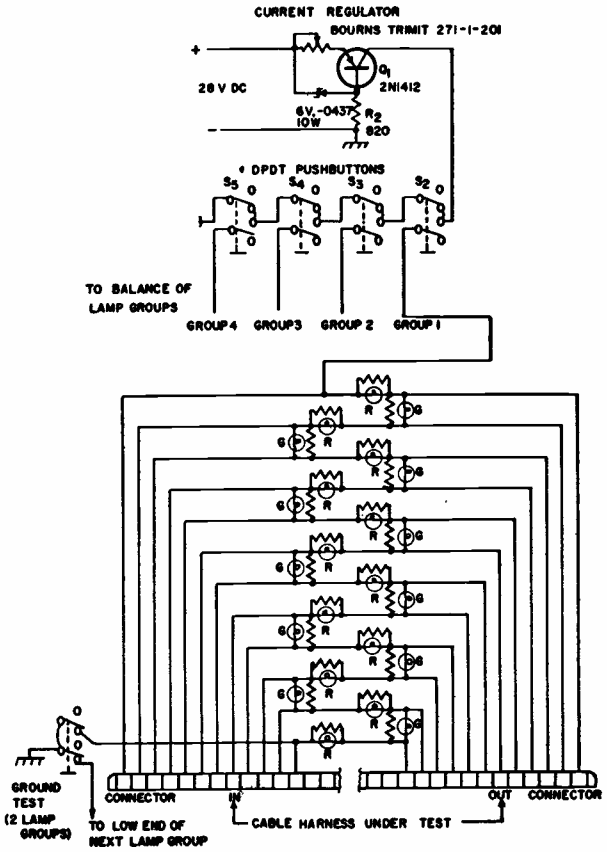


FIG. 1—Cable Harness.

The maximum number of lamps in one group is shown in the schematic, Fig. 1. One push button switch actuates one group of lamps. If more than one button is pressed, the group of lamps will be actuated by the button wired closest to the current regulator. It is impossible to operate more than one group of lamps at a time.

The current regulator limits the lamp current through the string should there be an error on the cable being tested causing most of the lamps to be shorted out. The ground test button switch opens the return to the chasses to determine if the wire shielding is touching any of the wires.

With the test specimen disconnected, press group 1 push button switch. All the lamps (red and green) in that group should light up. Then repeat with group 2 and so on. Any lamps which do not light at all indicate burnout and should be replaced. A short between lamp groups will cause lamps to light in the group where the short is present. The cable may contain an infinite number of wires. Sufficient lamp groups will be needed for additional wiring. The terminations (cable connector and terminal identification) should be marked on the panel next to each red and green lamp.

With the test specimen connected and the proper group of lamps actuated, a good cable will cause all the green lamps to light and all red lights to be off. A red light on will indicate an open wire or connection. Several lights off will indicate a short between the off lights (check panel marking for short identification).

Corrections:

1. The Bourns Trimpot to be a 10 ohm #236S-1-100.
2. The 6 v zener diode to be replaced with a 1N540 diode (cathode-to-base of transistor).
3. The resistor from base of transistor to ground to be 560 ohm 2 w.

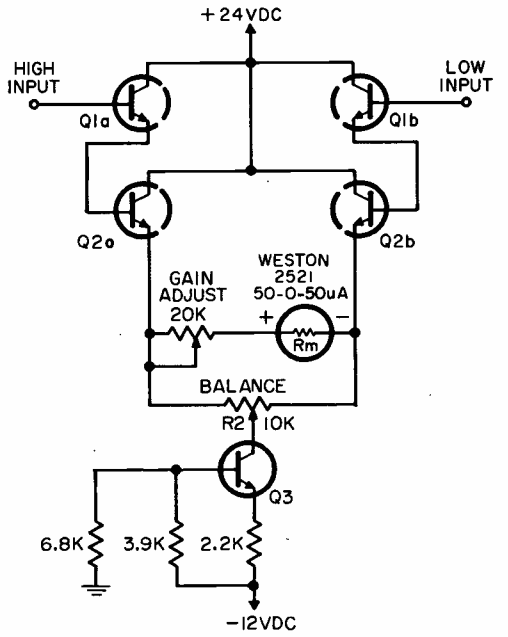
The above change were made to allow 25 v to appear across the lamp strings so that the 23 bulbs can light up satisfactorily.

A High-Stability Differential Voltmeter

THE HIGH-IMPEDANCE, differential-input, transistorized panel voltmeter shown produces zero-point accuracy from −40 to 85 C. A stable zero-point eliminates the need for an undesirable zero-control. As a comparitor device, the meter compares the voltage under test with a known Zener-regulated reference voltage.

This circuit is a differential, Darlington-connected emitter-follower, employing a pair of 2N2060's with an unusually high degree of parametric symmetry. The bias point is stabilized by using a constant current sink connected to a 2N1613 transistor and biased at 2 ma I_e. Residual unbalance is trimmed by R_2, and the gain which is limited by R_m to about 50 μv full scale, may be further reduced to 0.5 v full scale by R_1. Circuit power consumption is 72 mw. Zero-point drift is unreadable from −50 to 125 C. Input impedance is about 1 Meg.

Accuracy is limited by source impedance matching, and to keep it down to 1 percent, unmatched source impedance should be less than 10 K. Thus, when using the unit to accurately compare a test voltage to a reference, both should have the same source impedance. Common mode limits are approximately 5

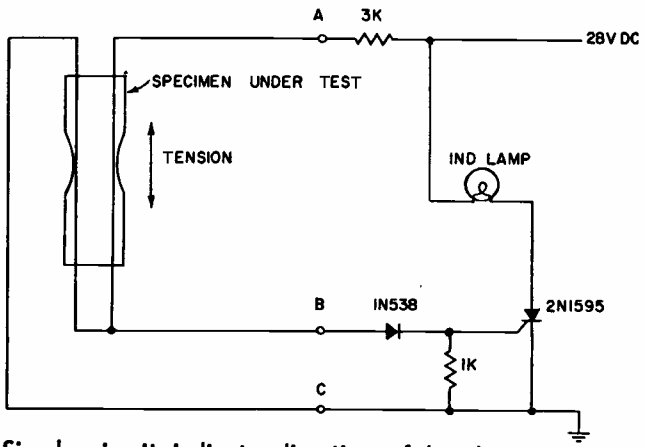


Differential voltmeter with a high degree of stability.

vdc. Trimmer potentiometers are used for R_1 and R_2 since no adjustments are necessary after balance and gain have been adjusted. Normal precautions should be taken as with all high impedance devices, i.e., keep

away from rf fields, moisture, and any other source of unbalance.

Anti-Coincident Detector



Simple circuit indicate direction of break in specimen under test.

FAILURES in structural test specimens occuring in two microseconds or slower can be detected for direction of failure with the simple circuit shown. One mil wires *AB* and *CB* are glued to the test specimen with one end of each connected together at point *B* and the other end of one wire is connected to ground and the other wire to 28 v dc through a 3K resistor. If the failure occurs from left to right, wire *CB* will open first and permit the scr to be triggered through wire *AB* and the lamp will burn. If the failure occurs from right to left, wire *AB* will open first and the scr will not be triggered and the lamp will remain off. Diode in the gate circuit is used to prevent inadvertant triggering of the scr as a result of the standing voltage at point *B* due to the resistance in wire *CB*.

Transistorized Tachometer

TECUMSEH Products Co. had a use for a tachometer that could be connected and disconnected from an engine quickly enough to allow production line speed adjustments. An instrument was designed whose input was a pulse from the high voltage ignition lead.

The pulse is picked up by a probe which has a flexible hook on its end. The hook is looped over the ignition cable in use and is just pulled away after the engine speed is set. The capacitance between the probe tip and ignition wire and the capacitance in the probe cable act as a voltage divider.

The probe is made from RG 58A/U coaxial cable. Approximately one inch of the shield is removed from the cable for coupling to the ignition wire. This capacitance is enough to produce a pulse width of a few tens of microseconds and about 1 volt high in the cable. The 1K resistor provides a termination for the cable and produces a better trigger pulse.

The pulse is fed through a capacitor and a diode to Q_1, the first stage of the mono-stable multivibrator (hereafter referred to as the multi). The diode isolates the multi from the probe except when the multi is being triggered. The capacitor provides dc isolation at the transistor base.

Since the transistors are npn type, the positive ignition pulse from the probe will make Q_1, which is held off by voltage divider resistors R_1 & R_2, conduct. The multi then switches states and produces a positive pulse at the collector of Q_2.

This voltage pulse, of constant height and width, has a frequency that is equal to the engine spark frequency. The pulse is direct coupled to an emitter follower circuit which isolates the indicating milliameter from the multi. The emitter is biased positive by R_3 & R_4. Thus the emitter follower will be cut off, keeping current from flowing in the meter except when the multi is putting out a pulse.

Thus the meter gets a current pulse whenever there is a spark. The average value of current is then proportional to the rpm of the engine. The mechanical damping of the meter is enough to damp the meter well down to speeds of 1000 rpm. A capacitor could be used for further damping.

A calibration signal is provided by passing line voltage through a diode clipping network. The output of the network is differentiated by C_1 and the resulting pulse triggers the multi on negative slope (since this signal is coupled to the collector). Since the engines that these tachometers were designed for gave one spark per revolution, the calibration signal calibrates the meter at 3600 rpm. Calibration is accomplished by adjustment of the 500-ohm pot and R_5. The latter is used to initially calibrate the milliammeter and calibrate out the effects of pulse length.

Capacitor C_2 and resistor R_6 adjust the pulse length. The values were chosen so that with an engine speed of 4000 rpm (full-scale reading), the pulse length is about 75 per cent of the period between pulses. As transistors vary in leakage current and the capacitors used were of 20 per cent tolerance, the pulse length varies within these limits. In the ten instruments that were built, the value of R_5 varied from 0 to 1000 ohms.

Because the output pulse height of the multi also determines the current through the meter and because this he ght is determined by the supply voltage, a regulated supply is necessary. This is accomplished by V_1 which regulates the rectified voltage before the divider resistors which reduce the voltage to 13 v.

There was considerable trouble encountered in getting a pulse from the ignition wire that would reliably trigger the multi. This problem was complicated by lack of a good oscilloscope plus the fact

that the instrument would be used near other engines that would interfere with its operation by giv ng spurious triggers. It was determined that much of the interference of false triggering was caused by pulses put out by a meter into the power line and hence picked up by a second meter. After shielding the line cord and putting filter capacitors across the line both in the plug and in the tachometer, the instruments could be operated near other engines and other meters and still give a reliable reading for engine to which attached.

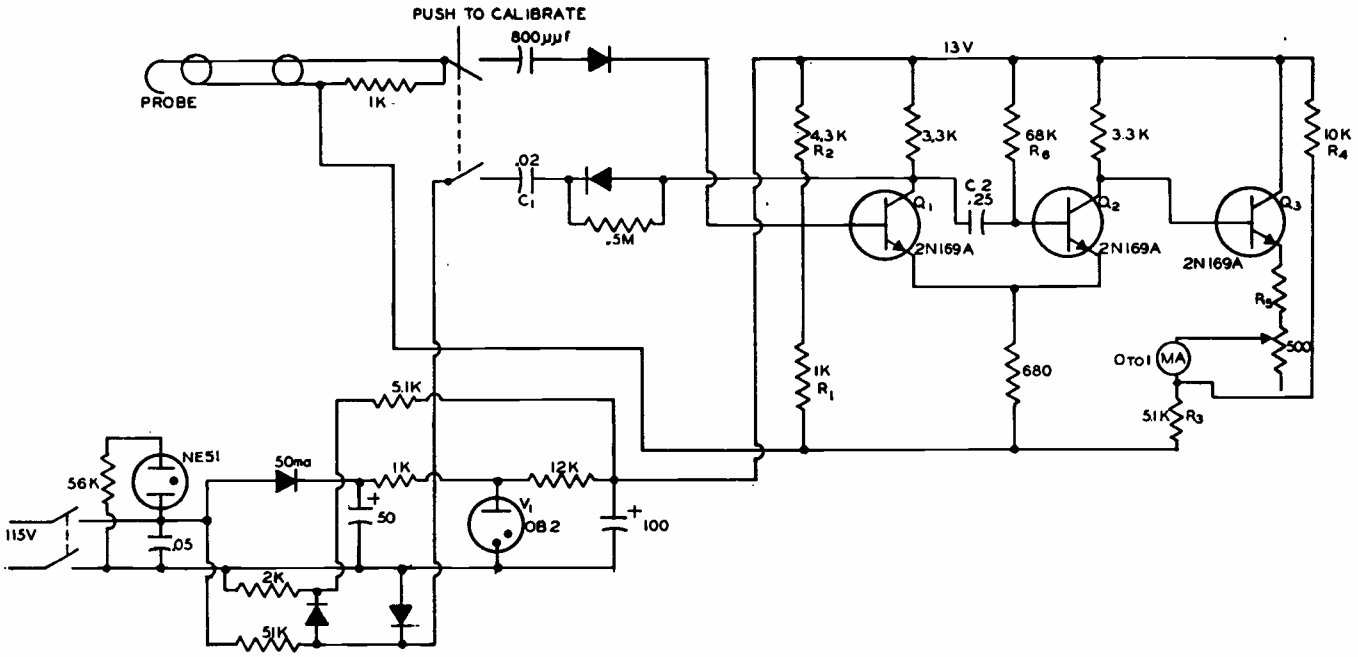


FIG 1—Tachometer couples to high-voltage lead of engine with quick-disconnect cable.

Relay Life Failure Indicator

MANY MONITORS have been devised for the purpose of detecting relay failures under resistive load conditions. These units contain expensive multi-tube, transistor or magnetic amplifier devices which sample at the correct cycle time the voltage drop across the closed test contacts. This voltage is amplified and sent to a trip or counter circuit.

Although these devices may be necessary in the low dry circuit area, Fig. 1 shows a monitor using only one tube which can be used on contact loads as low as one milliwatt. No voltage amplification

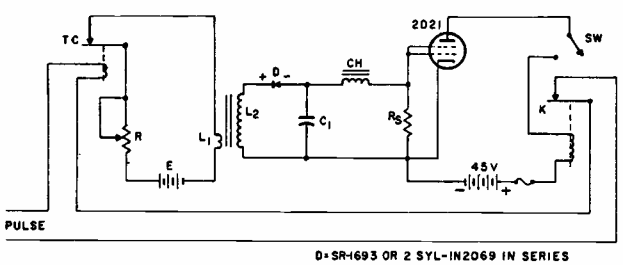


FIG. 1—Circuit of relay under test is isolated from monitor circuit.

takes place in the tube and its response time can be varied from 100 milliseconds to many seconds. Since there is no direct or physical connection to the test circuit, it offers safety where high voltage loads are encountered.

The test relay is pulsed at a rate of 5-20 pulses per second. Source E and resistor R supply the correct power to the test contacts. A non-inductive type resistance is used at R.

The pulse power flows through L_1, a coil of 3 to 6 turns of No. 18 wire, therefore the inductive power is coupled to L_2, a coil of about 200 to 500 ohms and many turns of wire. The L_2 output is rectified by D_1 and placed across C_1. Capacitor C_1 builds up this charge to many volts as long as the test contacts continue to pulse.

The charge cannot leak off fast because of the back resistance of D_1, therefore a negative charge is placed on the tube grid which prevents it from firing. Failure of the test relay contacts allows this charge to leak off at a time rate controlled by R_S (20 to 100 meg). The tube will then fire, pulling up relay K which shuts off the pulsing circuit.

A Variable Beta Transistor

ONE VITAL component needed for transistor circuit development and circuit reliability testing work is a low-limit beta transistor. If one also wants to simulate low-temperature beta in the circuit, the desired minimum beta will be lower than the manufacturer's limit. Occasionally, after much use (or

abuse), a transistor will have the desired low beta, but this cannot be depended upon. Besides, if an individual has acquired such a gem, it's sure to have been borrowed whenever it is needed.

At a particular collector current, the nominal beta transistor requires a particular base current, but a low-beta transistor will require proportionally more. Additional base current can be drawn by a shunt element, but its properties should resemble a forward-biased diode. Therefore, a shunt element composed of a series resistor and a diode (forward conducting) of the same type of semiconductor (silicon, germanium, etc.) would simulate the base-emitter junction in bypassing part of the base current. Figure 1 shows an npn circuit and Fig. 2 the pnp equivalent. If the resistance is variable, a circuit consisting of transistor, variable resistor, and a diode can constitute an effectively variable beta transistor.

By using the circuit described with a very high beta transistor, a circuit being developed can be tested quickly for the effect of beta variation due

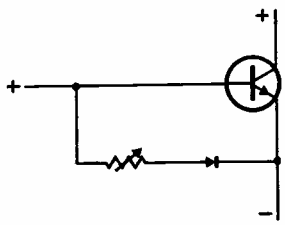


FIG. 1—An npn variable beta device.

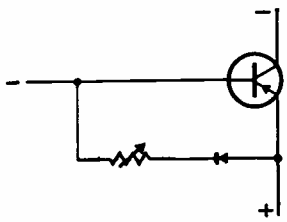


FIG. 2— A pnp variable beta unit.

to manufacturing tolerance, high and low temperature, and aging with the twist of a knob. Alternately, this circuit can be used for gain control. At high frequencies, the possible difference in junction capacitance between the transistor base-emitter junction and diode junction may cause problems.

For a specific example, the 2N697 npn silicon transistor has a specified beta range from 45 to about 120. The bulk of the transistors received from a particular manufacturer had betas around 80, but it is possible to receive transistors with betas at the lower limit. With 10 ma collector current, the beta

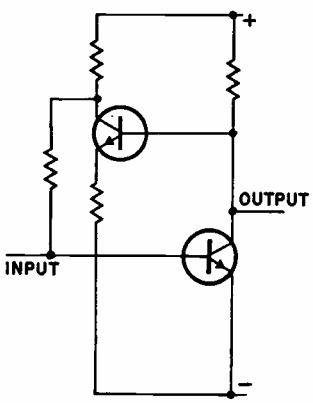


FIG. 3—Gain augmentation circuit.

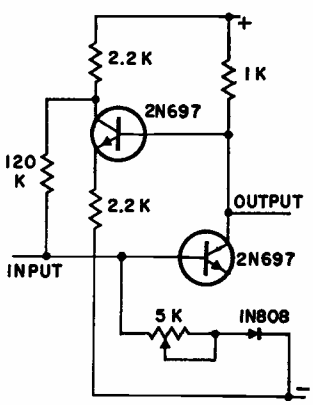


FIG. 4 — Variable gain augmentation circuit.

of a low limit transistor will drop to about 30 at —60 C. Low temperature testing of a circuit can be simulated by use of the proper value of beta without the delay and inconvenience of using an environmental chamber. At a stage where design is very fluid or for reliability testing, such a circuit can be used to great advantage.

The graph of Fig. 5 shows the variation of effective current gain for a 2N697 transistor with a

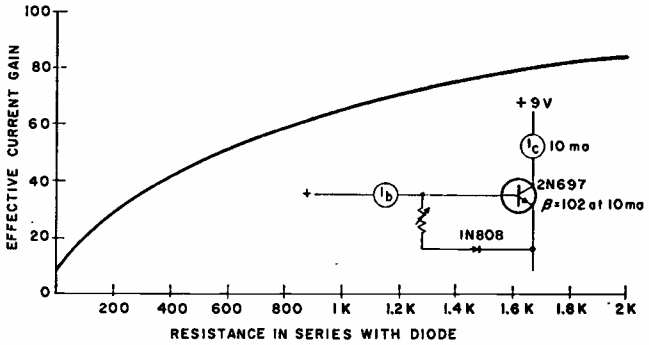


FIG. 5—Variable beta characteristic of a 2N697.

beta of 102 at 10 ma, versus the value of the resistance in series with the 1N808 silicon diode. The 1N808 diode has a low forward resistance. A diode having a higher forward resistance would have a curve intersecting the B axis at a higher value, and would be more nearly linear.

For a given type of transistor and diode, a set of curves for various unshunted betas and collector currents could be developed. From such a set of curves, a resistor-diode shunt element could be picked which would simulate a desired beta.

Conversely, of course, a high-beta transistor can be simulated by use of two low-beta transistors, connected as shown in Fig. 4 or Fig. 5. Actually, an infinite gain can be achieved when the base current feed-back becomes equal to the input signal. This is the 'potentiometric' amplifier sometimes used in servo work. By use of a potentiometric feedback circuit and the shunt circuit, an equivalent transistor with a gain variable from high to low limits can be designed for limit testing of circuits, etc. Unfortunately, a universal, calibrated version of Fig. 5 cannot be built because dc levels vary with supply voltages and collector currents. However, for any given set of circuit conditions (transistor type, supply voltage, load resistor) a 'variable beta transistor' can be quickly devised which will simulate the gamut of possible betas.

A Go No-Go Vacuum Tube Voltmeter

THE VOLTMETER, described here is designed for applications in which a specified voltage with a specified tolerance must be accurately monitored by unskilled personnel. It provides an indication to its operator by three lights which indicate that the unknown voltage is "low", "go", or "high" with re-

spect to the preset upper and lower "go" limits. A "go" band as narrow as 0.1 volt can be obtained.

Although the high and low limits may be quickly and easily adjusted to any desired values within the range of the instrument, the primary usefulness is in applications involving production testing, acceptance testing, military or commercial inspection, quality control and other tests involving large batch sampling or 100 per cent testing of a given component on the production line.

Its chief advantage is that its readout is rapid and foolproof. No judgment or meter reading ability is required of the operator. In this respect, it is readily adaptable to automation or automatic factory concepts.

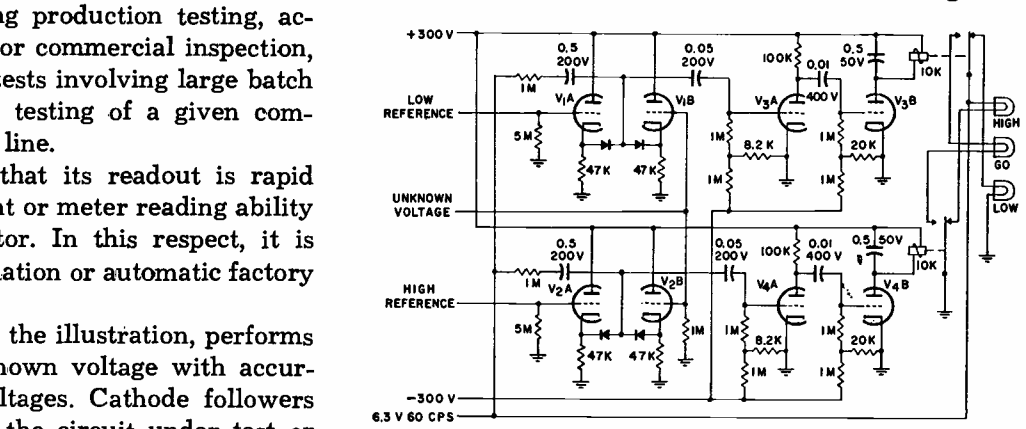
The circuit, as shown in the illustration, performs a comparison of the unknown voltage with accurately preset reference voltages. Cathode followers prevent loading of either the circuit under test or the reference voltages. Since the unknown voltage is applied directly to the grids of vacuum tubes, the input resistance may be made as high as other vtvm's. Circuitry consists essentially of two comparison circuits: one to compare the unknown to the lower reference voltage, and one to compare it with the upper reference voltage. An ac voltage, 6.3 volts at 60 cps, is applied through a high impedance to both comparison circuits, and also to the inputs of high gain ac amplifiers. Comparison circuits act as parallel switches or gates across the amplifier inputs. That is, the diodes and cathode followers modulate the ac supply, so that the ac inputs to the amplifiers are proportional to the differences between the unknown voltage and the reference voltages, provided the diodes are biased in the reverse direction. If the diodes are forward biased, they effectively shunt the signal to ac ground.

Relays in the plate circuits of the amplifiers are arranged in a logical manner, so that the "high" lamp is lit by the "high" relay when the unknown voltage is higher than the high reference.

When both relays are energized, the "go" light is turned on, indicating that the unknown voltage is within the predetermined pass band.

The reference voltage can be set with extreme accuracy without the use of a meter, by connecting a ten-turn linear potentiometer with a vernier dial or digital reading dial across well-regulated voltage source.

The instrument as built covers a basic range of 0 to + 100 volts. However, this range can be extended indefinitely with dividers. Also, the circuit can be modified to read negative voltages by returning the 47K cathode resistors to a negative



Circuit of go no-go vacuum-tube voltmeter. Tubes are all type 12AX7, diodes 1N69.

supply instead of to ground, and using a negative reference voltage. Rectifiers could be used to adapt the circuit to ac measurements.

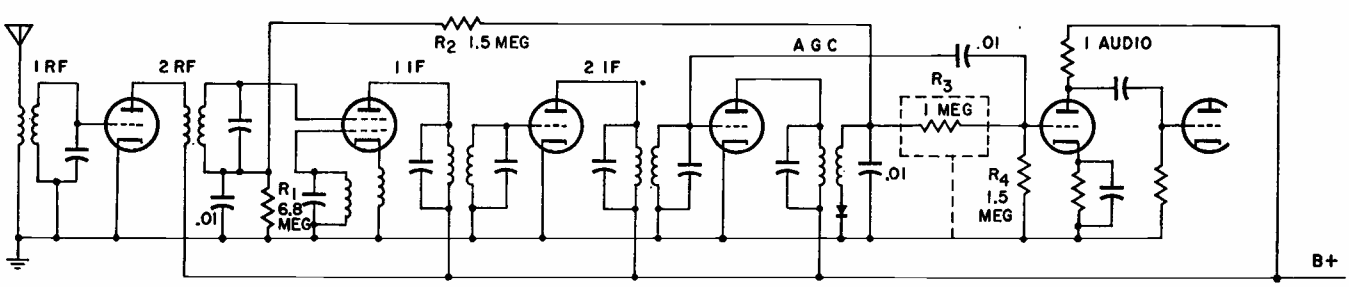
Errors due to variations of tubes T_1 and T_2 are extremely small because a cathode follower has 100 per cent negative feedback. Its small signal gain is as follows:

$$A = \frac{R_k}{R_k\left(\frac{u+1}{\mu}\right)+\frac{1}{g_m}} = \frac{1}{\left(\frac{\mu+1}{\mu}\right)+\frac{1}{g_m}\cdot\frac{1}{R_k}}$$

The formula indicates that gain is affected only to a very small degree by variations in R_k, μ or g_m, provided μ is high, and R_k is large compared to $1/g_m$. These conditions are fulfilled in the circuitry.

In addition, the reference-voltage cathode follower and the test-voltage cathode follower are the two halves of a dual triode; hence, any changes of gain due to filament voltage variation, plate supply voltage variation, aging, ambient temperature variation, etc., are negligible because the changes occur simultaneously and in the same direction in both triodes and thus tend to cancel out.

Errors due to variations of tubes T_3 and T_4 are also extremely small because there is no requirement for these tubes to have an exact gain. A great excess of gain necessary to operate the relays is



Circuit of modified agc system.

provided and considerable reduction of tube gains do not change the circuit operation.

Feedback Method of Checking Tracking of Dual Potentiometers

THE METHOD to be presented is especially useful whenever the tracking specifications specify that the ratio of the two output voltages, or resistances, lies within certain limits, usually specified in db. The two sections of the dual potentiometer need not be of the same resistance value.

As a typical example, consider a stereo volume control. These are usually used in conjunction with a balance control. Typical specifications require that after balancing at maximum loudness, one output voltage should be within 3 db of the other output voltage from 0 to —50 db and within 5 db from —50 to —60 db.

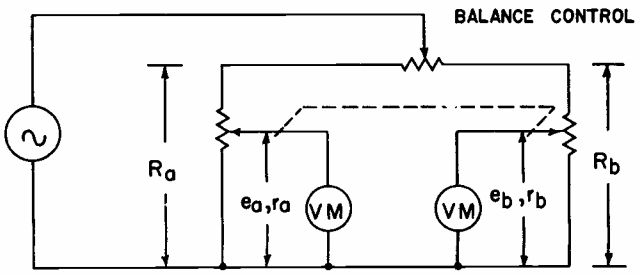


FIG 1

Two methods of checking tracking of dual pots.

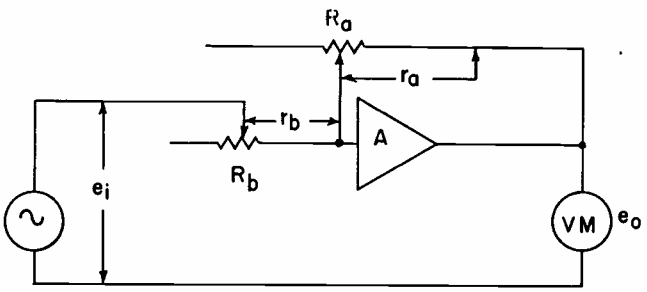


FIG 2

The simplest method of checking is shown in Fig. 1. The use of voltmeters calibrated in db permits the direct subtraction of readings to determine db difference. The ratio of the output voltages is $e_a/e_b = (r_a/r_{amax})/(r_b/r_{bmax})$ since the balance pot is adjusted for equal output voltages when the dual pot under test is at maximum output. Tap loading and end loading resistors can easily be connected in the circuit when required.

Note that R_a is equal to or greater than r_a maximum since there may be some resistance between the brush and outside terminal when the pot is at maximum. Similarly, r_a minimum may not equal zero ohms.

Although this method is simple, it is time consuming to read two meters and subtract their difference at several discrete points throughout the rotation of the dual pot. Meter ranges will have to be changed several times. In addition, the accuracy, depending on the type of meter and the portion of scale used, is affected by the subtraction process.

To obtain a faster, more accurate, and continuous method of checking dual pots, the following method was devised using an operational amplifier principle as shown in Fig. 2. The amplifier used is a Philbrick K2-W. If the gain, A, of any conventional amplifier, is large enough the gain with feedback is $A_f = e_o/e_i = r_a/r_b$.

The procedure to be followed is:

1. Turn dual pot to maximum
2. Set output voltage, e_o, to some convenient level by varying the input voltage, e_i (15.8 mv or —34 dbm is used in our tester). The input voltage is then

$$e_i = \frac{e_o}{A_f} = \frac{r_{b\,max}}{r_{a\,max}} e_o$$

3. Slowly rotate the dual pot throughout its range. The output voltage at any pot setting (e_o'), is

$$e_o' = \frac{r_a}{r_b} e_i = \frac{r_a}{r_b} \quad \frac{r_{b\,max}}{r_{a\,max}} e_o$$

$$\frac{e_o'}{e_o} = \frac{r_a/r_{a\,max}}{r_b/r_{b\,max}} = \frac{e_a}{e_b} \text{ (in Fig. 1).}$$

Thus the output voltage compares to the reference voltage in the same proportion as the ratio of the two output voltages of Fig. 1. This ratio can be read directly in db or converted to voltage readings, depending on the type meter available.

4. The determination of the —50 and —60 db points is not necessary unless the tracking exceeds the 3 db limits. This is done by switching the pot into the circuit of Fig. 1 and measuring the output voltage with a known input voltage. A judicious choice of the input voltage eliminates the need for changing meter scales.

Dual pots from 2.0 megohms to 20K ohms have been tested in this maner. The minimum value of r_a that can be tested depends on the output impedance, current capability of the amplifier and the reference voltage, e_o. This minimum value is 20 ohms in our case, with the following amplifier and generator characteristics.

$A = 15{,}000$ $\quad$ $Z_g = 0.1$ ohm
$Z_o = 1{,}000$ ohms $\quad$ $f = 100$ cycles
$I_o = 2$ ma

This method is very flexible and can be easily modified to test dual pots under different specifications.

To test dual pots where no balancing control is used, simply perform step 2 using the outside terminals, instead of turning the pot to maximum and using the center terminal. In this case, $e_o'/e_o = (r_a/R_A)/(r_b/R_B)$ To check the normalized resistance ratio between center and outside terminal, simply substitute accurate known resistance when performing step 2. In this case, $e_o'/e_o = (r_a/R_{A\ standard})/(r_b/R_{B\ standard})$.

Low Current Transistor Beta Checker

A USEFUL PARAMETER for evaluating a transistor is beta or h_{fe} and typical transistors have values of approximately 10 to well over 200. As shown by the curve of Fig. 1, the slope decreases with increasing collector current, showing that beta decreases proportionally. For small current transistors this slope does not greatly change, resulting in a fairly constant beta, but on high power or high current transistors it can decrease by as much as 50 per cent.

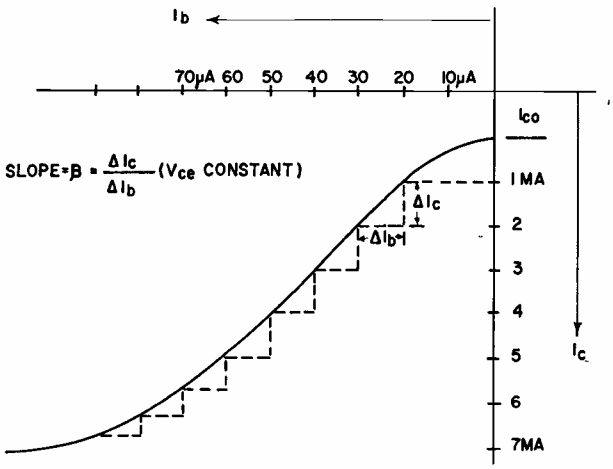


FIG. 1—Beta curve on which tester is designed.

A simple tester that measures beta under low current conditions would serve as a quick evaluation of most transistors. The transistor beta checker to be described will perform this function with an accuracy proportional to its initial calibration. Zener diodes are used to maintain a constant voltage source for accuracy.

On the low leakage range, the meter is in a bridge circuit for zero reference, Fig. 2. On the high leakage range, the meter is back biased with a zener diode of approximately 6.2 v. These steps are necessary to oppose any collector leakage current through the meter for zero reference.

One leakage range takes care of current up to and slightly over 1 ma and the other handles up to 10 ma. This balancing is done with the base of transistor under test open. Then an incremental base current of 10 μa is applied to the base and the collector current read on the meter.

The meter is calibrated from the formula, beta $= \Delta I_c/\Delta I_b$ with V_{ce} constant, and in this case with a 1-ma meter full-scale beta will read 100. The meter can be shunted for higher ranges.

It would be useful to know how much collector leakage current is present in the transistor under test. This can be found by measuring the back biasing of the meter. This value corresponds to the leakage current. By inserting a milliameter in series with the beta meter, and first on the high leakage range, calibrate R_{10} (6 K) directly with the reading of the meter. This is done without using a transistor in the test socket. The same could be done on the low range, although it is not necessary. It may be necessary to vary R_9, R_{11} and R_{13} to get the required ranges with particular meters used.

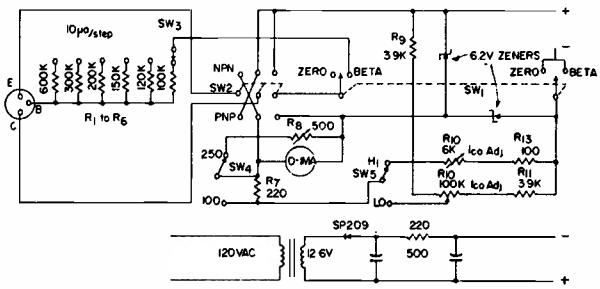


FIG. 2—Circuit of transistor beta checker.

The base current now has to be set. Assuming that approximately 6.2 v is applied to the transistor under test and that the average base to emitter bias is approximately 0.2 v, this leaves 6 v to be applied to the base through R_1, giving 10 μa of base current. A more accurate method could be used by making R_1 variable and, with the transistor removed, connecting a microammeter between the base and emitter while depressing the beta switch. Set R_1 for 10 μa of current to establish the proper current required for given meter and beta range.

In the model constructed, the base current was stepped in increments of 10 μa so that a beta curve could be plotted with base steps up to 60 μa. This method is very useful with transistors that start out with very low beta.

To adjust meter shunt R_8, get a high beta reading on the low range and adjust R_8 for the same reading on the high range. R_7 may have to be chosen so that the zener will always see a constant impedance when switching from one range to the other. By applying an ohmmeter across the meter and R_7, check that the resistance remains constant from one range to the other.

Insert a transistor in the test socket and set polarity switch 2 depending on the transistor being checked. Depress switch 1 to the zero position and rotate appropriate R_{10}.

Rotating R_{10} balanced out the leakage current so that the meter reads zero. Depress switch 1 to read beta. While it is depressed, zero the meter with R_{10} and change SW_3 to the next position. This gives a new reading of beta for another

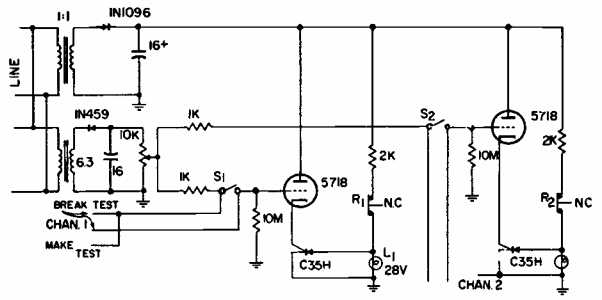
increment of 10-μa base current. If the beta curve is linear, beta will remain constant. The procedure is repeated up to the sixth position, giving an overall beta reading. Caution must be exercised while stepping higher increments of base current which could result in overloading the zener diodes.

Component Vibration Test Monitor

VISUAL INDICATION of momentary contact malfunctions occurring in components during vibration testing is accomplished by the circuit shown. It also indicates a permanently opened or shorted condition of a component being vibration tested. The nature of the fault can be determined by a reset switch. Two channels enable the monitoring of several components simultaneously. Operating time is approximately 25 microseconds. This allows the detection of faults which occur below a cutoff frequency of 40 kilocycles.

The component or components are connected in the grid circuit of a 5718 triode so that the grid bias of the tube is lost if a malfunction occurs. This allows the tube to be driven to saturation. This saturation current acts as a gating current to a silicon controlled rectifier in the cathode circuit of the tube. Upon application of the gate current, the scr extinguishes an indicating light, connected in parallel with it. This is accomplished by replacing the normally high forward impedance, presented by the scr in the unfired condition, with the very low forward impedance of the scr in the fired condition.

After the gate signal has been applied, the scr will conduct in the forward direction, even after the gate signal has been removed. To reset the scr after it has been fired, it is necessary to reduce the anode voltage to zero for a short interval of time. This is accomplished by depressing a normally closed reset switch.



Circuit of vibration test monitor for components.

The resets also provide a means of determining the nature of the malfunction. For example, in testing of devices having normally closed contacts, such as a relay, the lamp should go on initially. During the vibration test, the lamp would go out if the contacts open momentarily. To detect whether a momentary or permanent short has occurred, the associated reset switch is depressed and released. If the lamp remains on, the open was momentary. If it goes out on release, the open is permanent. Proper selection of test terminals provides testing of normally open contacts.

Electronic Squib Simulator

PROPELLANT ACTUATED FASTENERS, fired by electrical detonation, are widely used in missiles, boosters, and space systems to effect vehicle separation. These devices are invariably of the one-shot variety. They have very low impedance prior to firing and act as an infinite impedance after firing.

The circuit described simulates the electrical characteristics of a primer or squib. It is useful in testing the firing circuits which actuate the vehicle fasteners in that the electrical load and duration may be varied over wide limits.

Two power sources are required for operation. The squib firing source is E_1. A second power source, E_2, of higher voltage than E_1, is used to reverse bias Q_1, and switch off E_1.

Application of E_1, forward biases Q_1 and Q_2. The base currents are de ermined by R_1 and R_2, which are sized for saturation of each transistor. Current flows through the emitter-collector of Q_1 and R_L, with almost the full value of current flowing through R_L.

Capacitor C_1, begins charging through R_5. The charge then becomes proportional to the time constant R_5C_1, and causes sufficient voltage to appear at the gate of SCR_1. Hence, the SCR_1 conducts. Firing of the SCR_1 applies a reverse bias to the emitter-base junctions of Q_1 and Q_2 causing them to cut-off.

Diode D_1 permits E_1 to forward bias Q_2 causing it to initially conduct, but E_2 reverse biases Q_1 after the SCR_1 fires. Dicde D_2 prevents E_1 from reverse biasing the SCR_1 prior to firing.

Switch S_2 provides reset capability for the circuit. The maximum value of load current is determined by selection of R_L. If a silicon controlled rectifier with lower sensitivity is used instead of the 2N1872, typical values of R_5 and C_1 are 1 K and 10 μfd.

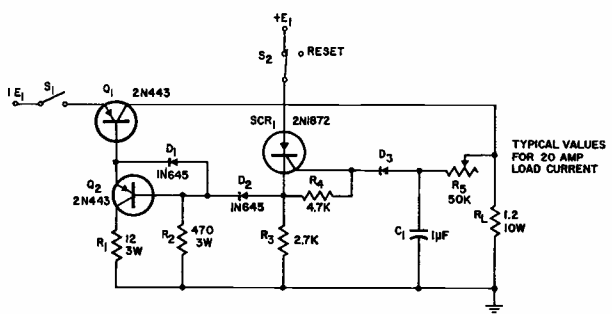


Fig. 1—Electronic Squib Simulator.

Engine Tachometer

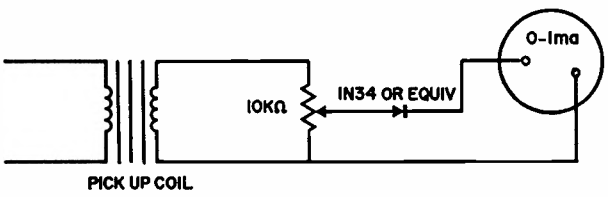
THE CIRCUIT SHOWN was conceived after many hours of experimentation. It was desirable to have a tachometer suitable for use where no battery or power source were available. Once the tachometer was installed, a minimum amount of maintenance would be required.

The coil is a relay field coil. A coil from a Potter and Broomfield KCP-11 10 K relay was used. The coil bobbin fits nicely on a 7/16 in. bolt used for mounting. In the case of an outboard motor, the pickup coil should be mounted near the rotating magnets of the flywheel. Where a separate magneto is used, as in the case of some stationary and aircraft engines, the pickup coil is mounted on the side of the magneto case. The mounting should be as close to the rotating magnets as possible. On most automotive engines, where no such rotating magnets are available, a variable reluctance pickup is used. This involves use of a magnetized core for the coil. It is easily accomplished by obtaining a small permanent magnet from an old speaker, gluing it to the head of the steel bolt, and using it as the core of the pickup coil. The assembly is mounted over the fan blades of the generator with the permanent magnet opposite the coil.

It is important that the coil mountings be firm, rigid, and made of aluminum to maintain calibration.

Calibration is accomplished by comparing the tachometer reading on the installation to a known standard. Most garages have a tachometer available for such a purpose.

Several units have been built at a cost of about $5.00 each.



SIMPLIFIED TACHOMETER

Fig. 1—Simplified tachometer.

Simple Transistor Tester

A CIRCUIT WHICH CHECKS a transistor for damage, wide ranges of h_{FE} I_{EO}, I_{CES}, and I_{CZO} is shown in the figure. In addition, this circuit can be used to check diode forward and leakage current.

To measure I_{CO} switch S_1, is set to position 1, switch S_2, is set to the proper position for the type of transistor under test; current I_{CO}, can then be read from the meter.

To measure h_{FE}, first set S_1 to position 2, and switch S_4, to position 4. Adjust resistor R_4, until meter M, indicates a predetermined constant value V_{IB}. Then S_4 is switched to position 3 and contact S_3, is depressed; M will indicate h_{FE} directly.

Resistor R_4, is large enough to provide a voltage reading from M without drawing current from I_{CO}. With S_4 at position 4, the voltage V_{IB}, indicated by the meter, is given by the relationship

$$V_{IB} = \frac{I_B R_2}{R_4 + R_2 + R_m} R_m$$

where I_B is the base current.

With S_4 at position 3, the voltage indicated by M when S_3 is depressed, is

$$V_{IC} = \frac{I_C R_2}{R_4 + R_2 + R_m} R_m$$

Where I_C is the collector current.

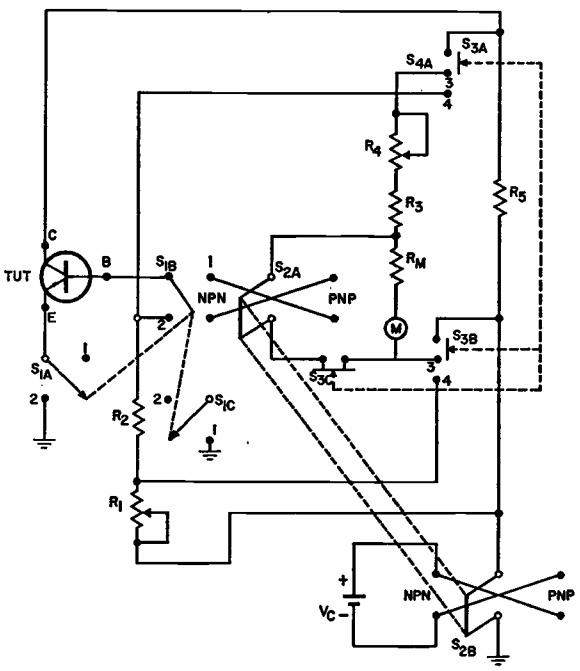
Thus,

$$\frac{V_{IC}}{V_{IB}} = \frac{I_C R_5}{I_B R_2}$$

Let $N = R_2/V_{IB}R_5$ be a normalizing factor. By choosing N properly, one makes the meter read h_{FE} directly. The value of V_{IB} determined here will be the predetermined constant mentioned before for adjusting R_4.

The function of S_{3C} is to prevent short circuit of the power supply V_c, in the event S_{3C} is closed accidentally during the measurement of I_{CO}.

If $V_c = 12$ v, $R_5 = 1K$, $R_2 = 50K$, and $R_1 = 100K$ the normalizing factor can be easily set to be unit, and the range of h_{FE} over 100 can be read.



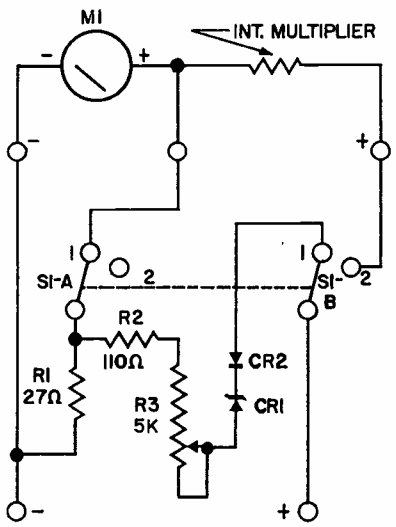
Transistor tester.

S_1 = 3P2 position
S_2 = 2PDT
S_3 = 3P push button, S_{3A} = S_{3B} normally open, S_{3C} normally closed.
S_4 = 2P2 position
M = 100 μa full scale
R_m = meter resistance
R_1 = Resistance for varying I_B to get h_{fe} of different type of transistors.

Dual Range DC Voltmeter

THIS DESIGN WAS CONCEIVED by the author and is in use at present in factory checkout test equipment. The requirement was for a meter to measure dc voltages within a range of 18 to 38 v and be able to measure 30 v dc ± 0.1 v at which amplitude a relay was to actuate. Both requirements were satisfactorily met with by a single meter, a 2 pole-2 position rotary switch, and a few additional components as shown in the figure.

Fig. 1. Dual range voltmeter.



***M* 1 = 50 mv, 1 ma, basic movement Unimeter.**
***R_1* = 27 ohm, ± 5 %, ½ w resistor.**
***R_2* = 110 ohm ± 5 %, ½ w resistor.**
***R_3* = 5 K Potentiometer**
***CR1* = Zener diode, 27 v, 1 w.**
***CR2* = Diode 1N540.**
***S1-A, S1-B* = Rotary switch**

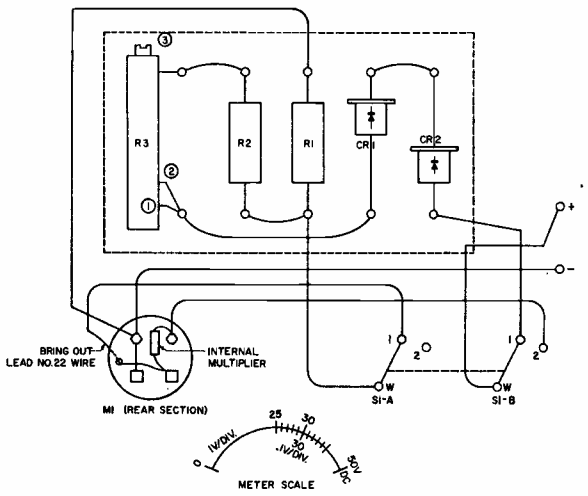


Fig. 2. Rear view of dual range voltmeter.

With the switch in position 2, the meter and multiplier resistor are connected as a standard 0-50 vdc voltmeter. With the switch in position 1 the multiplier resistor is disconnected, and R_1 is shunted across the meter to allow ≅ 3 ma through the zener diode *CR1*. The *CR2* diode is for temperature compensation. Approximately 27 v is then held across *CR1* and *CR2* and the meter becomes ≅ 27 (low end of scale) to ≅ 32 v (high end of scale) voltmeter thereby changing sensitivity to 0.1 vdc/division. Potentiometer R_3, is used for exact 30 vdc calibration.

The two ranges of the meter are as follows:
Range 1—0-50 VDC, 1v/div. Range 2—Expanded scale at 30 vdc, 0.1v/div.

Frequency Meter-Tachometer Amplifier

THE UNIJUNCTION TRANSISTOR can be used for a simple, inexpensive tachometer amplifier or frequency meter as shown in the circuit of Fig. 1. In this circuit the potentiometer is adjusted to give a steady-state emitter voltage, below the peak point voltage, by an amount determined by the desired input pulse sensitivity. Each time a negative pulse of sufficient amplitude occurs at the input the ujt is triggered and the 1μfd capacitor is discharged through the ujt. The capacitor is then recharged through the potentiometer and the dc ammeter. The current through the meter has a sawtooth waveform rather than a pulse waveform. Thus, this circuit shows less tendency for flutter at low input frequencies than conventional tachometer amplifiers.

The meter reads the average capacitor charging current which is promotional to the frequency of the input pulses as expressed by,

$$I = [V_1 - 0.5\,V_{B(sat)}]fc$$

where V_1 is the steady state voltage across the capacitor; $V_{B(sat)}$ is the emitter saturation voltage of the ujt; and f is the pulse frequency. A variable resistor can be used in parallel with the meter, for accurate calibration. To obtain good linearity the capacitor should be fully charged before a pulse occurs. A fully charged capacitor limits the maximum input frequency of the

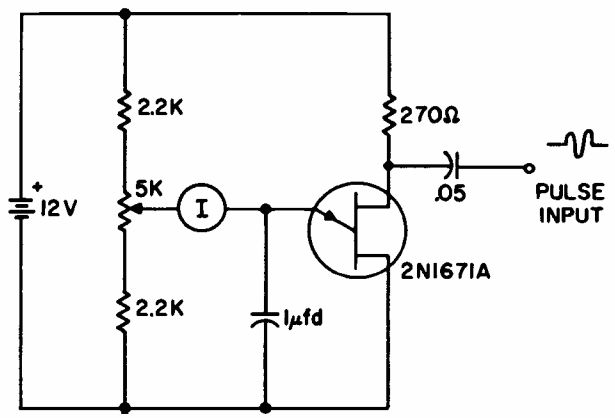


Fig. 1 Frequency meter Tachometer Amplifier.

circuit. The output resistance from the center arm of the potentiometer should be low making possible a high operating frequency, but high enough to prevent the ujt from being bistable. Generally, a value of 3.3 K is adequate to fulfill the latter requirement. In critical cases, the resistance can be reduced appreciably by adding a small inductor (10-100 mh) in series with the meter. This inductor acts to limit the current to the ujt during the switching interval without limiting the available current for recharging the capacitor. The size of the inductor should be chosen to give a critically damped waveform, i.e. there should be no appreciable overshot on the capacitor charging waveform.

Simple Scope Setup Measures Differential Microvolts

THE NEED to calculate microvoltage arises when attempting to measure low level differential or single-ended ac signals on an oscilloscope. A resolution of better than a trace width was required. The problem can be solved by using a 50 microvolts/centimeter differential plug-in connector in conjunction with an rms millivoltmeter connected to the "Vertical Output" terminal of the scope (see figure).

Three precautions should be observed. First, the sensitivity to common mode voltages can be minimized by injecting a 1 volt 60 cycle sine wave at point "A" and adjusting the "Differential Balance" control for minimum reading on the vtvm.

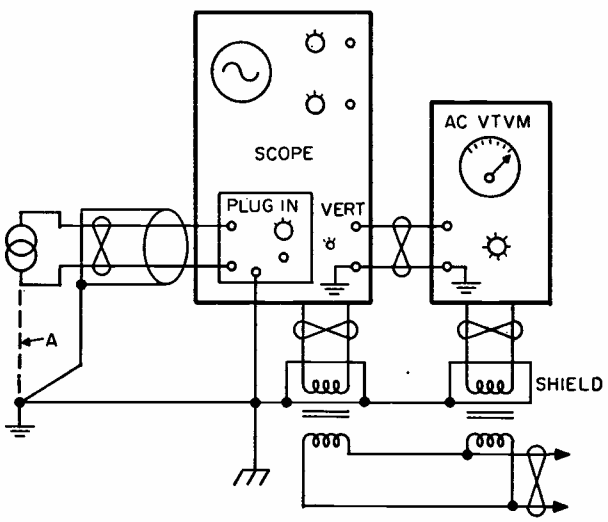
Second, the scope-millivoltmeter combination may be calibrated from the scope "Calibrate" reference, remembering that a given trace pattern results in the same vertical output on all scope sensitivity ranges. This reference voltage is square; therefore, the rms conversion appropriate to the signal waveform should be applied, namely:
Rms voltage reading equals one half the peak to peak calibration square wave.

Third, a short circuit input noise calibration is necessary if very low levels are to be measured. This calibration depends on the plug-in bandwidth settings.

Suppose the rms noise voltage is V, and the measured signal plus noise rms voltage is E, then the true rms signal voltage is very nearly $(E^2 - V^2)^{1/2}$.

Good low noise and grounding techniques, as shown in the figure have enabled a few microvolts to be measured without difficulty. The grounding techniques include low capacity isolation power transformers for both scope and millivoltmeter, and a single large copper ground conductor.

The measurement procedure outlined has proved valuable for noise checking of thousands of low level analog instrument cables associated with computer-controlled industrial processes.

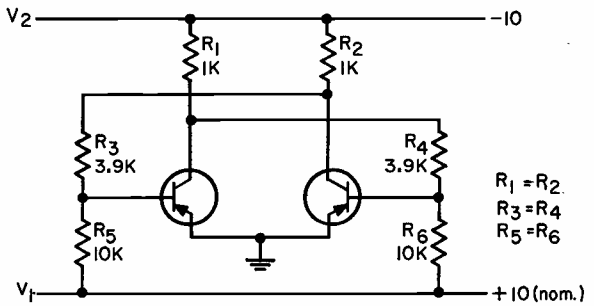


For preferred low level signal measurement: isolation power transformers, short twisted shielded cables, and single point grounding are emphasized.

Simple Test Anticipates Transistor Failures In Complex Equipment

AS THE COMPLEXITY of equipment using transitors has increased, the problem of obtaining some indication of transistor failure in advance of actual breakdown has become one of vital importance. It simply is not possible to test each of 1000 or more transistors which may be in one piece of equipment.

There are two parameters which, when checked, provide a fairly accurate picture of a transistor's condition, there are beta and I_{co}. If all the transitors can be checked for these parameters and found to be within design limits, the equipment may be reasonably expected to be in good condition as far as transistors are concerned.



Tester anticipates failures in complex equipment transistors.

These parameters may be checked by making the bias power supply variable, in a system which has been designed to accommodate such a test. Beta of the transistors may be checked by increasing the bias

to the point where the base drive to the transistors is barely sufficient to overcome the bias and still drive the transistor. Any transistor with a low beta will not receive enough drive and will be found when the circuit fails to operate. The I_{co} may be checked by lowering the bias to the point where an excessive leakage current will cause a faulty transistor to turn on and, as with the beta test, be found when the circuit fails. These are not absolute tests, but they are simple to employ and can perform a valuable service. The voltage excursions to be used must be calculated by the designer for each piece of equipment. An example is now shown.

Example

$$V_1\,(max) = R_5\left(\frac{V_3}{R_2 + R_3} - \frac{V_2}{\beta_{min}\,R_2}\right)$$

$$V_1\,(min) = (R_5)\,I_{co}\,(max)$$

(approximate equations)

Design Values $\beta = 10$ (min)

$I_{co} = 0.25ma$ (max)

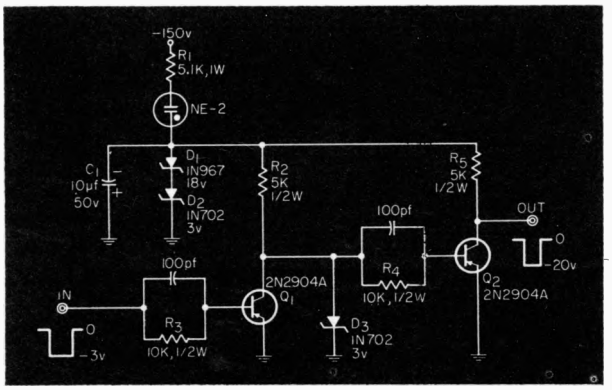
The test values to be used for V_1 are +2.5 v and +15 v.

Pulse Amplifier for Beam Intensity Modulation

THIS PULSE AMPLIFIER is a suggested modification to a Tektronix oscilloscope, to allow CRT beam intensity modulation from 3-v logic levels.

The output is connected to the external CRT cathode terminal through a short piece of coaxial cable. Rise and falltimes of 100 nsec result. If a variable pulse amplitude is desired, R_5 could be replaced with a potentiometer with the output taken from the wiper. The shift in dc level is unimportant since the signal is ac coupled to the cathode.

The only power supply used is the internal −150 v. Current drain on the supply is about 10 ma. No temperature compensation is needed due to the low leakage current (0.01 μa at V_{cb} max) of the transistor used.



Z-axis modulation circuit.

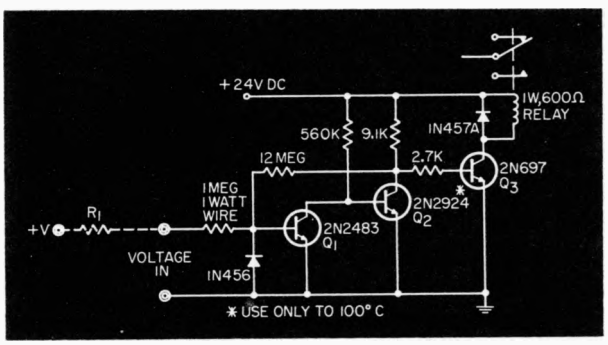
Schmitt Triggers on Nanoamp Inputs

HERE IS A HIGH-RELIABILITY Go, No-Go test circuit that cannot be damaged or even affected by overloads of 1000 V or more at the input. The circuit's major application is in leakage testing components such as capacitors, diodes and insulation up to 150°C ambient.

An input of less than 300 nA triggers the output relay. With R_I the test resistance (such as cable insulation), a 1000-V test potential will cause relay triggering if R_I falls below 3000 meg. However, if R_I fails and shorts over, the Schmitt is completely protected. Only a 1-mA input current flows under this fault condition. Therefore, if a wirewound input resistor is used as shown, 1000 V can be sustained and 2000 V handled for a short period. At voltages below 400 V or so, a film or even carbon input resistor can be used.

Bipolar transistors were used in the circuit instead of FETs since the transistor version was judged cheaper, simpler and easier to protect against high voltages.

Circuit operation is straightforward. Q_1 and Q_2 form a direct-coupled Schmitt with positive feedback occurring through the 12-meg resistor instead of through common-emitter coupling. It is important to note that the 2N2483 transistor is a low-saturation (switching) transistor with other characteristics similar to the standard low-level type 2N929. It is this characteristic that allows Q_1 to pull its collector



Low-level current-detector Schmitt circuit.

voltage low enough to completely turn off Q_2. This also explains why Q_2 can be successfully switched off despite leakage current that may occur in an economy transistor at high temperatures.

The Q_1—Q_2 Schmitt is coupled to a relay-driving transistor through a 2.7-K resistor. This resistance is low enough to allow proper saturation to cut-off operation of the 2N697 but still allows enough voltage swing (about 5.4 V) to the 12-meg resistor to cause proper positive feedback to the Q_1 stage.

Typical performance is as follows: pull-in, 0.59 V; drop-out, 0.32 V; hysteresis, 0.27 V or about 270 nA. The trigger points shift less than 200 mV with temperature increase to 85° C, and hysteresis increases only about 10 percent with temperature.

Parallel-Path Continuity-Checking Circuit

THIS CIRCUIT WAS REQUIRED for accurate continuity checking in automatic test equipment, where nonseparable, parallel paths were to be monitored within the equipment under test. The circuit operates over a temperature range of +40° to 125°F and is independent of power supply voltage variations.

The current flowing through the circuit being checked is limited so as to prevent damage to low-power circuits. Resistance levels for continuity checks are set at 5, 20, 100 and 1000 ohms.

The basic checking circuit consists of a voltage-divider input network, a differential-amplifier comparator, two emitter followers for isolation of the differential-amplifier inputs, a reference voltage and a level detector.

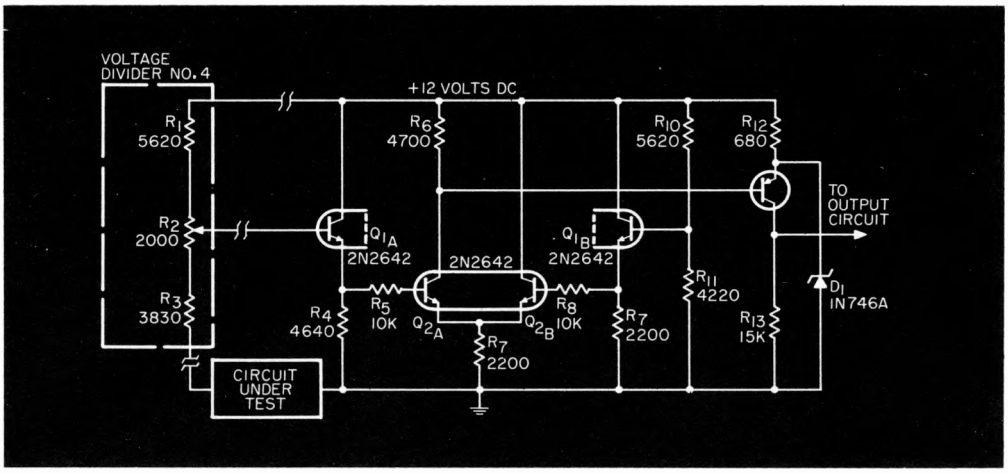
The input network consists of R_1, R_2, and R_3 and the circuit under test. This network provides at the base of Q_{1A}, an input voltage whose level depends on the value of resistance of the circuit under test. The output of emitter follower Q_{1A} applied to one side of the differential amplifier, is compared with a reference voltage generated by R_{10} and R_{11} and isolated from the differential-amplifier transistor Q_{2B} by emitter-follower Q_{1B}.

The differential amplifier output at the collector of Q_{2A} is used to drive a level detector, Q_3. The detector reference voltage level is held constant by zener diode D_1. When the resistance under test is greater than the nominal value, the output at the collector of Q_3 is a positive voltage. If it is less than nominal, the output is ground.

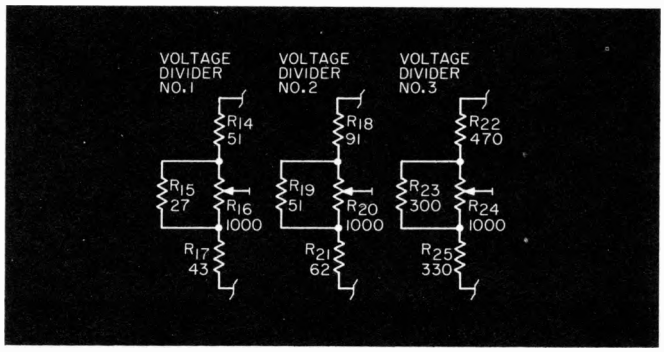
The level detector is used to drive an output circuit (not shown) giving visual indication and to supply a logic signal to the system within which the checker is used. The circuit operates without adverse effect from power supply variation because of the high common-mode rejection provided by this configuration.

Several voltage dividers may be used, depending on the desired continuity resistance level. Voltage divider No. 4 is used for performing the 1000-ohm test. Voltage dividers Nos. 1, 2 and 3 may be used to replace No. 4 for monitoring 5, 20 and 100 ohm levels, respectively. These ranges were selected within the automatic test equipment using relay switching circuits.

The test accuracies for the 1000-ohm continuity test were within 10 ohms, for the 100-ohm test within 1 ohm, for the 20-ohm test within 0.2 ohm, and for the 5-ohm test within 0.1 ohm. Accuracies could be improved, if desired, by increasing the current through the voltage dividers.



Continuity-checking circuit handles parallel paths.



Voltage dividers for various continuity resistance levels.

Automatic Scaling Circuit Uses ICs

WHEN USING a voltmeter or similar indicator to measure a wide range of voltages, it is normal to have a manual range-selector switch.

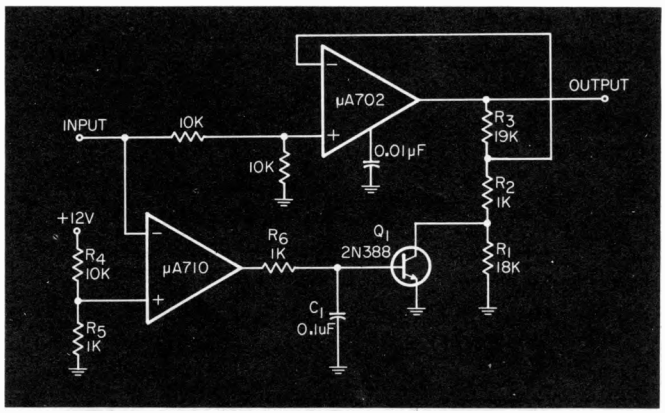
The circuit shown here provides automatic range selection. With these typical component values the circuit has two ranges, 0-1 V and 0-10 V fs. Similar circuits have been built with up to four different ranges.

The μA710 amplifier and transistor Q_1 comprise the electronic range switch. The input to this amplifier is compared with a fixed reference, derived from the divider network R_4 and R_5. The μA702 amplifier has variable gain, controlled by the feedback network R_1, R_2 and R_3. The ratio of this network is switched by transistor Q_1.

The gain of the μA702 amplifier is given by the formula

$$E_{out} = (1 + n)\, E_{in}$$

where $n = \dfrac{R_3}{R_1 + R_2}$



Automatic scaling circuit gives two meter ranges. With values shown here, scales are 1 V and 10 V fsd.

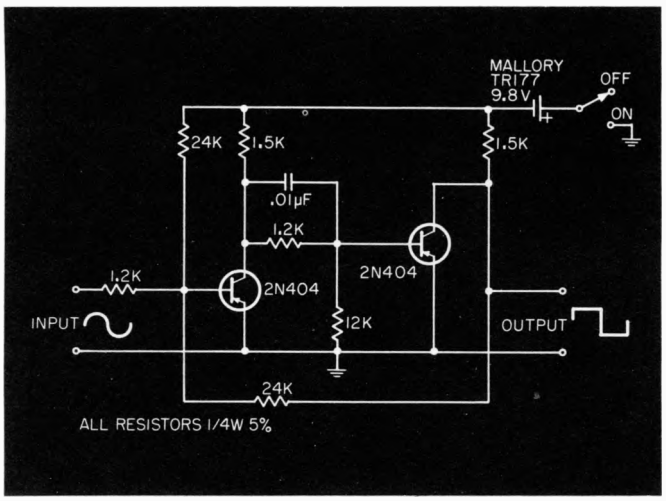
It can be seen from this equation that because Q_1 shorts R_1, the switching circuit will control the output voltage of the μA702 amplifier.

Normally, when the input voltage is less than the reference voltage set by divider R_4 and R_5, the output of the μA710 is positive and turns on Q_1, thus shorting R_1. This allows maximum gain of the μA702.

When the input voltage rises above the reference voltage, the output of the μA710 goes negative thus shutting off Q_1 and decreasing the gain. The capacitor provides damping for smooth crossover of scales. Note that, using an isolation diode, Q_1 can drive a scale indicator. This will show which range has been selected.

With the circuit shown there is an offset in the output, on the 10-V scale, due to V_{CE} of Q_1. If this is undesirable, it can be reduced by using a FET or by operating Q_1 in the inverted mode to give lower V_{CE}.

Plug-In Squaring-Unit for Signal Generator



Schmitt trigger circuit which shapes the output of a sine-wave generator.

A SQUARE-WAVE generator is often required for the design and test of digital equipment. This simple circuit will increase the versatility of existing test-equipment by converting sine waves into square waves. It is suitable for use with any sine-wave generator having a 600-ohm output and an output-level control.

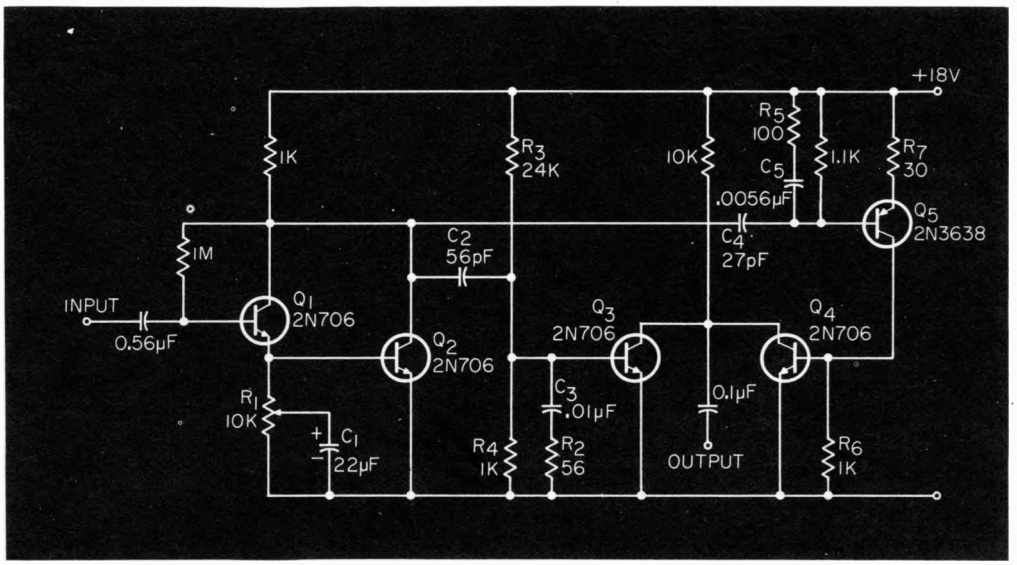
The basic circuit used is a schmitt trigger which is constructed on perforated epoxy-paper board and mounted along with the input/output connectors, on/off switch and a mercury battery in a small box. This results in a self-powered plug-in unit which is compatible with most audio generators having a GR-type connector for the output terminals.

The symmetry of the output square-wave is adjusted using the output-level control on the sine-wave generator. With the circuit shown, the battery life is limited, but could be increased by raising the values of the collector-load resistors of the two transistors. Other types of battery may also give longer life.

Differentiating Amplifier Intensifies Scope Trace

THIS CIRCUIT automatically corrects the intensity of an oscilloscope trace for variations in vertical writing speed. It is assumed that the intensity will be initially set by the user, with no vertical input to the scope, and that increased intensity will be required as the input-signal frequency increases. The gain control allows the intensity to be balanced for vertical and horizontal deflections. The output of the circuit is connected to the cathode of the CRT. Trace intensity is practically constant, for rise times ranging from very-slow to 0.01 μsec.

With an input of 50-mV rms, the output is 17-V peak at 100 MHz and above. For



Differentiating circuit gives increased gaiu at high freqnencies to compensate for loss of brightness in CRT.

frequencies below 100 MHz, output voltage is directional proportional to input frequency. The circuit will work with input levels as low as 10 mV. Input impedance is approximately 20 K when the gain control is set to maximum. Thus, for most applications, the input to this circuit can be paralleled with the input of an existing scope amplifier.

The circuit is so designed that positive and negative input pulses will give the same trace intensity, assuming that rise times are identical. This is achieved by having separate differentiating stages for positive and negative signals. Transistor Q_3 amplifies only positive-going voltages and Q_5 amplifies negative-going voltages. Both these stages are normally cut off.

Emitter follower Q_1 is direct-coupled to amplifier Q_2. Gain control is provided by capacitor C_1 which shunts the base of Q_2, as determined by R_1. This arrangement is used, instead of a conventional gain control, so that dc conditions will not change with gain.

Positive signals at Q_2 collector are differentiated by C_2 and R_4 to drive Q_3. Negative signals from Q_2 are differentiated by C_4 and R_5 to drive Q_5. Both of these circuits have the same time constant.

Transistor Q_3 is slightly forward-biased by R_3 and R_4 to compensate for the base-emitter drop. The gain of amplifier Q_5 is unity, defined by the emitter degeneration of R_7 and the collector shunting of R_6. Thus for a symmetrical input signal, the voltages at the base of Q_3 and Q_4 are of equal amplitude and opposite polarity. These signals are recombined at the output because Q_3 and Q_4 share the same collector resistor.

Pulse-catching probe

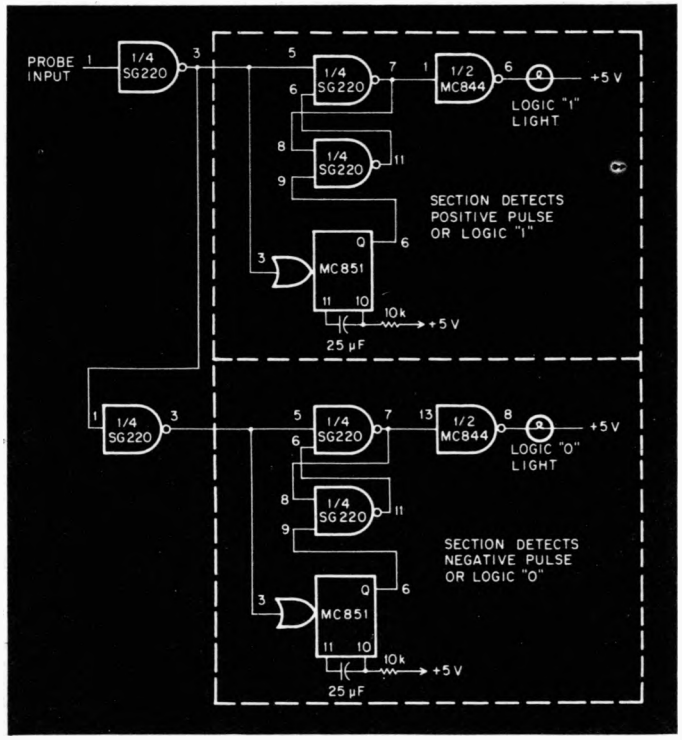
THE PROBE in the figure detects and displays four conditions in DTL and TTL circuitry. If the input is open or at logic "1," the logic *1* light will be on continuously. If in the logic "1" state a negative-going pulse is detected, the logic "0" light flashes on then off, indicating that a negative-going pulse had been present.

If the input is at logic "0," the logic *0* light will be on continuously. If in the logic "0" state a positive-going pulse is detected, the logic *1* light flashes on then off, indicating that a positive-going pulse had been present.

A continuous pulse train causes both lights to be on. At low repetition rates, the duty cycle of the pulse train can be estimated from the light brightness ratio. The duration of the flash is controlled by the one shots and can be adjusted. A duration of about 0.3 second works nicely.

The probe uses TTL gates and detects pulses as narrow as 10 ns. If this speed is not required, DTL gates can be substituted. The input buffer gate minimizes loading on the circuitry being tested. Discrete components can be used for an input buffer to provide overvoltage protection.

The two sections of the circuitry work the same way. When a logic "1" to logic "0" transition occurs at the input of a section, the one-shot is triggered and outputs a logic "1" for 0.3 second. The logic "0" state will set the RS flip-flop and cause the lamp driver to light the lamp. If the logic "0" is still present when the one-shot has timed out, the RS flip-flop still outputs a "1" until the logic "1" state is again present at the input. The logic "1" at the input then allows the reset of the flip-flop and extinguishes the light. If a negative-going pulse triggers the one-shot, the RS flip-flop remains set until the one-shot has timed out. ■



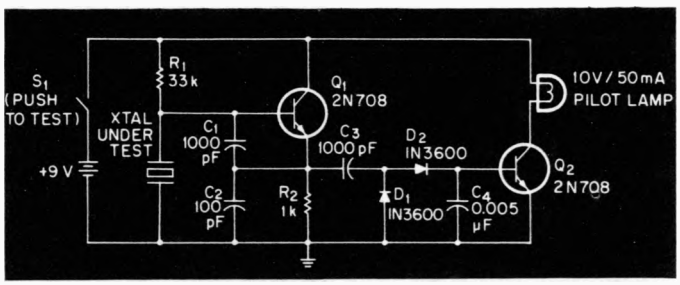
This versatile logic probe detects and defines pulses.

Self-contained crystal tester

TWO TRANSISTORS and a handful of components combine to produce a crystal tester. The crystal to be tested is inserted into a test socket and switch S_1 depressed. If the crystal is good (i.e., if it oscillates) the pilot lamp glows; if the crystal is bad the pilot lamp remains off. The entire unit can be battery operated and will fit into a 2 × 4 × 1½-in. package.

Transistor Q_1 and associated components form an untuned Colpitts oscillator which can oscillate over a wide range of crystal frequencies. When a good crystal is being tested, several volts pk-pk appear across R_2. This ac voltage is level shifted by C_3-D_1, peak detected by C_4-D_2 and the resultant dc voltage used to turn on Q_2 which turns on the pilot lamp. A non-oscillating crystal produces no drive to Q_2 and the lamp remains off.

This unit has been used to test crystals ranging from 3.5 to 90 MHz. Crystals which fail the test generally have broken leads or dirty contacts. ■



This simple go/no-go tester checks crystals over a frequency range of 3.5 MHz to 90 MHz.

Direct reading period meter

THE PERIOD of a repetitive waveform can be read directly on an ordinary milliammeter or voltmeter with the circuit shown. The readout is linear with period and allows any standard linear scale to be used.

The circuit in Fig. 1 consists of a constant-current source formed by Q_1, Q_2, and R_1 that charges C_1 when switch Q_3 is turned off. The flip-flop switches on alternate cycles of the input waveform, thus C_1 is allowed to charge during one cycle and forced to discharge the following cycle. Amplitude of the ramp voltage appearing on C_1 depends on the period p of the input signal. The peak voltage is

$$V_p = \frac{pI}{C}$$

The average voltage is

$$V_{av} = \frac{\frac{pV_p}{2}}{2p} = \frac{pI}{4C}$$

The average voltage on C_1 is directly proportional to the period of the input signal. Q_4 is an emitter follower to reduce the loading on the constant-current source. CR_1 keeps Q_4 from reverse biasing and acting like a rectifier when C_1 is discharged. CR_2 prevents C_1 from discharging completely so that Q_3 is in its linear region when the ramp starts.

R_2 and C_2 combined with the inertia of the meter movement form an integrator so that the meter will show a steady reading proportion to V_{av} and to period p.

A Motorola MC779P, multifunction integrated circuit, contains the flip-flop, two buffers and an expander to form the trigger circuit shown in Fig. 1. The trigger-level control allows the period of almost any waveform to be measured. Q_5 and C_3 force the flip-flop to reset after the input signal has been removed long enough for C_3 to charge to about one volt. This prevents the meter from pinning.

Meter readings over a decade are quite linear. Supply voltages are not critical and need not be closely regulated. The charging capacitor C_1 can be switched to make a multi-range instrument. ■

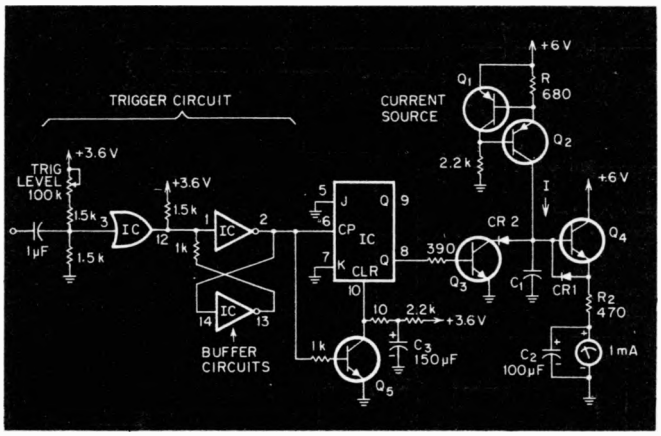


Fig. 1. The direct-reading period-meter circuit uses a Motorola MC779P as well as discretes.

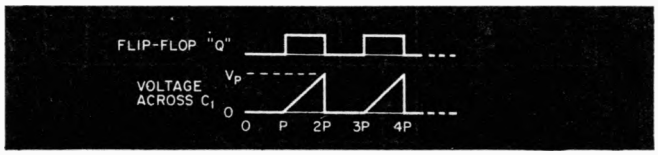


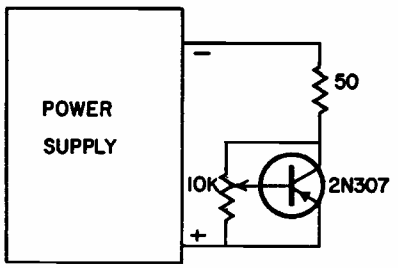
Fig. 2. Waveforms of the circuit in Fig. 1.

Section 12
GENERATOR & SIMULATOR CIRCUITS

Inexpensive Load Simulator

WHEN TESTING semiconductor power supplies for ripple attenuation and output impedance it is necessary that measurements be made at different values of load current. A large rheostat may be used to simulate a variable load. A more economical solution is to use an inexpensive, readily available power transistor.

The circuit shown in the diagram was intended to present a variable load to a 30 v supply rated at 0.6 amp max. With the center arm of the pot at the collector end, V_{cb} equals zero and the transistor



Transistor load simulator for testing power supplies.

is in saturation. The load current is therefore established by R_1 at 30 $V/50$ ohms or 0.6 amp. As the pot arm is turned down towards the emitter the transistor comes out of saturation and the load current decreases. With the base shorted to the emitter the collector current is some small value essentially equal to $I_{co}/(1-\alpha_n\alpha_i)$. At 30 v this may be about 10 ma in germanium and less in silicon.

Ultra Linear Ramp Generator

THIS CIRCUIT was designed to fill the need for an ultra linear ramp in a high accuracy, low speed, voltage to pulse width converter. Using the circuit, a plot was made showing departure of the ramp from a straight line between the 10 and 90 per cent points of the ramp. Linearity measured was better than 0.02 per cent and was limited somewhat by the measuring method and equipment.

The circuit shown is for a very long ramp but the principle can be used for many speeds and the relay can be replaced by two switching transistors for high-speed use. Of course the transistors introduce an error into the starting voltage of the ramp not found with the relay.

The circuit combines a transistor constant current source and a correcting circuit to compensate for the slight droop in slope near the end of the ramp (probably due to decrease in beta as collector voltage decreases with charging of C_1). As long as the voltage across the capacitor is less than about 8 volts, the 2N329 transistor keeps a constant voltage across its emitter resistors since the transistor's base is also kept at a constant voltage by the Zener referenced back to the +20-volt supply. Thus a constant emitter current flows, and the transistor having a reasonably high beta has a very similar current flowing from its collector to charge the capacitor. Leakage in a good pnp alloy transistor is an extremely small part of the total current and has little effect.

Varying junction drop with temperature can be compensated by putting a conducting diode, of characteristics similar to the transistor base-emitter diode, in series with the Zener diode.

Even with this constant current set-up there is a small decrease in collector current as C_1 charges, amounting to between 0.1 and 0.25 per cent nonlinearity. If a properly timed decreasing voltage can be inserted at point A in series with the constant current emitter resistor, this will slightly increase drop across the emitter resistor, and increase emitter current sufficiently to bring the transistor's

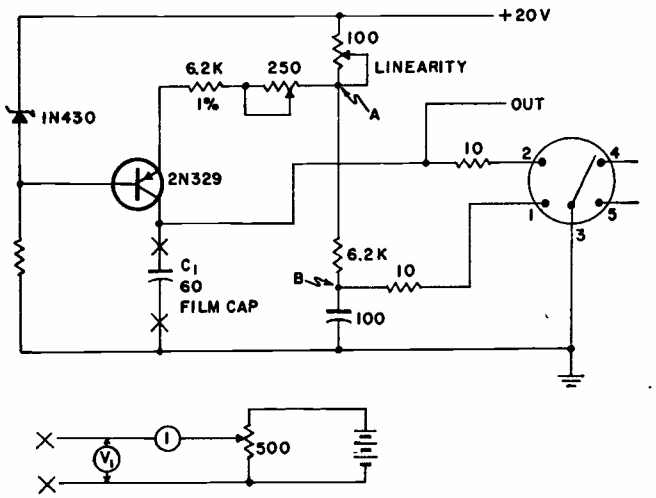
collector current back to a true constant value. As the correction needed is small (about 20 mv), a crude approximation to a decreasing voltage drop will be sufficient. A second ramp at point *B*, a standard exponential charging curve, does the job.

As the 100 μf electrolytic charges and its voltage increases toward plus 20 volts, the current drawn decreases. This current decrease shows up as a small voltage change across the linearity adjusting pot common to both ramp circuits. Proper adjustment of this control results in just enough decrease to compensate the other errors.

No ramp type bootstrap was used since it was discovered that any reasonable transistor amplifier drew enough current to add more than 0.1 per cent nonlinearity. In use, this ramp was loaded only with an ultra low leakage biased-off transistor in the input of a voltage comparator which drew current only at the moment of comparison.

It is interesting to see that a very large changing voltage injected at *A* can over compensate and give a positive exponential waveform output which is the reverse of the negative exponential charging curve.

Ramp linearity measurements are most easily



Test circuit at bottom is substituted for C_1 during adjustment of linearity control of ramp generator.

made with a precision voltage source, a time interval meter, and a high sensitivity dc voltage comparator. By measuring the time between relay contact opening and comparator firing time when the ramp reaches a known voltage, a plot of voltages vs. time can be made. A precision time interval meter timed with a stable crystal oscillator should be used to make measurements comparable with the accuracy of the ramp.

Adjusting the linearity control can be done as follows. Substitute the test circuit shown for the film capacitor. Also substitute a small divider and pot on a floating battery for the linearity control, so the voltage between plus 20v and *A* can be adjusted between zero and plus a couple of hundred millivolts. Start with V_1 on the meter at zero and note with maximum possible precision the milliammeter reading. Increase V_1 to the desired maximum voltage the ramp will reach in operation. Next increase *A* voltage until the meter returns to its original reading. This will have to be done several times with a very good meter, correction for parallax, etc. since the changes in current are very small. Note the dc value of the voltage between plus 20 v and *A* needed.

Constant Amplitude Sine Wave Source

NEED for a small battery operated, fixed frequency sine-wave calibration source, operating between 0 and +70 C, having less than 1 per cent harmonic distortion, and constant in output amplitude to within ±1 per cent, fostered the design of the circuitry shown in Fig. 1. Basically, the circuit generates a constant amplitude square wave and hen filters this square wave in a low pass network.

The circuit consists of a free-running multivibrator Q_3 and Q_4, switching transistor Q_2, constant current regulator Q_1, zener diode D_2, and low pass filter F_1. The free-running multivibrator Q_3 and Q_4 alternately turns the associated switching transistor Q_2 off and on. The coupling used betwen the multivibrator and Q_2 is shown in Fig. 2. A 10-ma constant current set by Q_1, D_1, and R_1, flows through Q_2 when Q_2 is on and through zener diode, D_2, when Q_2 is off.

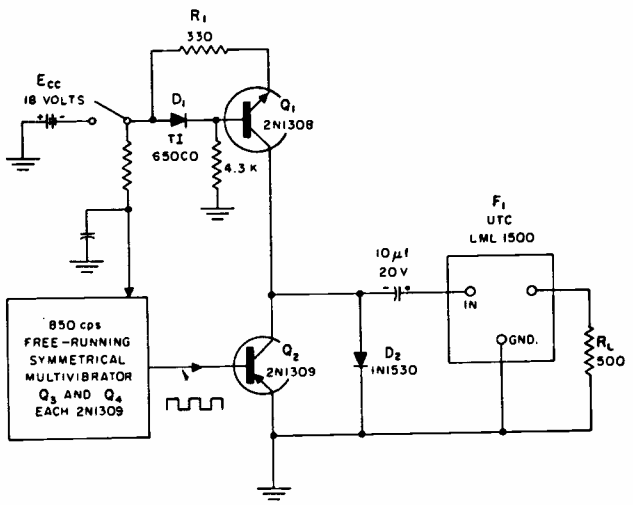


FIG. 1—Circuit for generating constant amplitude sine waves.

Thus, the square wave amplitude across D_2 is determined on the negative half cycle (Q_2 off) by the voltage developed from the constant current through D_2, and on the positive half cycle (Q_2 on) by the collector-emitter saturation voltage of Q_2. Over the operating temperature range, zener diode

D_2 maintains a constant voltage to within 0.14 per cent, and the change in Q_2 sautration voltage is less than 0.33 per cent of the square-wave amplitude.

This constant amplitude square wave is then

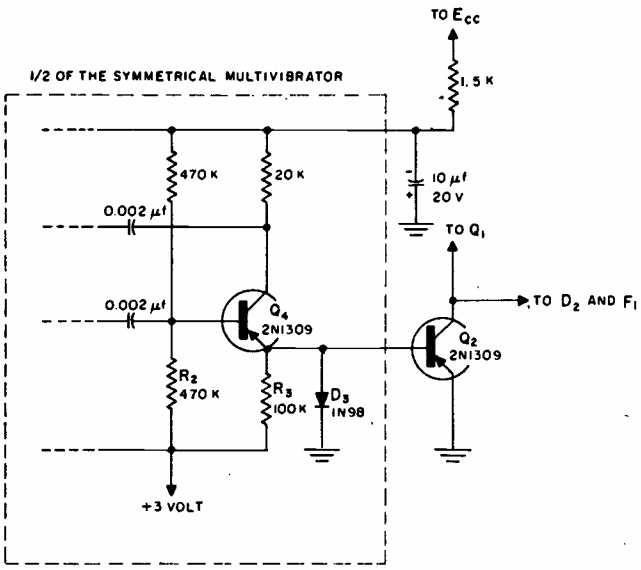


FIG. 2—Multivibrator and Q_2 coupling.

passed to F_1, a 1500-cps cut-off, low pass filter, where ideally, only the fundamental frequency component of the input square wave appears as a sine wave across the filter load R_L. Constant amplitude and minimum distortion of the sine wave output is achieved by operating the multivibrator at approximately 850 cps. At this input frequency the transfer characteristics of the low pass filter F_1 are high attenuation to second and higher order harmonics, and constant output for small variations in multivibrator frequency due to temperature effects.

High-temperature starting of the multivibrator is insured by the +3 volt bias supply and the associated resistors R_2, R_3 and diode D_3 shown in Fig. 2.

The frequency stability is 4 per cent from 0 to 70 C at —18 volts. At this voltage, battery drain is 13 ma. The 3-volt battery supplies 60 microamperes. Distortion is less than 1 per cent and output voltage is approximately 3 volts rms. The actual value depends upon the 1N1530 chosen, resistance of R_L, etc.

Simple Triangular Waveform Generator

THE CIRCUIT shown in Fig. 1 will provide a triangular waveform with essentially linear ramps having equal rise and fall times.

Operation of the circuit is as follows: Capacitor C_1 charges thru R_1 to the point where the Zener voltage of ZR_1 is overcome, then C_2 also begins to charge thru R_1, CR_1, and ZR_1. When the voltage across C_1 reaches the breakdown potential of the Shockley diode SR_1, C_1 begins to discharge rapidly thru SR_1 and R_2. This sudden discharge of C_1 causes CR_1 to become reverse biased preventing the charge on C_2 from following the path taken by C_1, thus C_2 must discharge thru R_3. The result of this series of events is a triangular waveform across R_3, as shown by Fig. 2A. Resistor R_2 serves to limit the current thru SR_1, and is assumed to be equal to zero for this discussion.

To obtain a linear output, the breakdown voltage of the Shockley diode must be small compared to the applied voltage E. The ratio should be in the order of 4-to-1 or greater. Linearity is equally dependent on $V_{z/a}$, the charge left on C_2 when ZR_1 closes being no less than ¾ V_z. In order for the output to have equal rise and fall times these two conditions must be met:

$$\frac{R_3 C_2}{R_1 (C_1+C_2)} = \frac{1}{4}$$

$$C_1 = C_2$$

From the above it is obvious $R_1 = 2R_3$

With the above conditions in mind the rise and fall times of the output are approximated by:

$$T_f = R_3 C_2 \left[\ln V_z - \ln \frac{V_z}{a} \right]$$

$$T_r = R_1 (C_1+C_2) \left[\ln \left(E - V_z - \frac{V_z}{a} \right) - \ln \left(E - V_s \right) \right]$$

Where:

V_z = The breakdown voltage of ZR_1
V_s = The breakdown voltage of SR_1
a = a number $1 > a > 4/3$ determined by the degree of linearity desired.
E = the applied voltage.

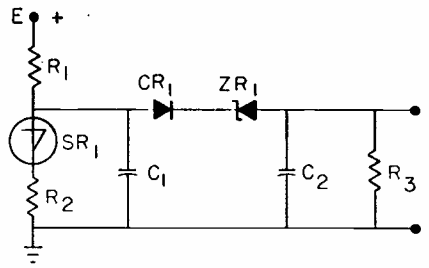


FIG. 1. Diode circuit provides triangular waveform.

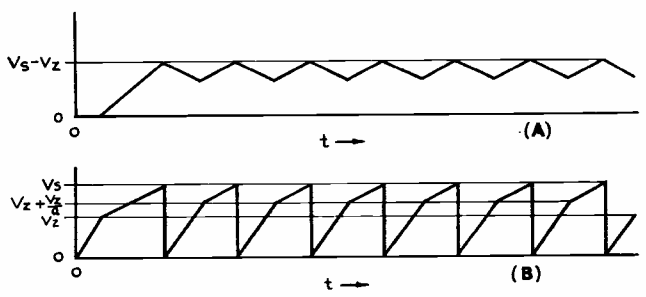


FIG. 2. Output of waveform generator (A) and waveform across C_1 (B)

It is interesting to note the waveform across C_1 is that of a double ramp as shown by Fig. 2B. Because V_s is small compared to E, the most linear portion of the charge curve of R_1 C_1 and R_1 $(C_1 + C_2)$ is used to obtain the double ramp. For this reason the two ramps are considered practically to be straight lines with slopes as follows:

The slope in volts per sec of the first ramp is:

$$S_1 = \frac{aV_z + V_z}{(a)\ (T_s)}$$

Where:

$$T_s = R_1 C_1 \left[\ln E - \ln \left(E - V_z - \frac{V_z}{a} \right) \right]$$

The slope in volts per sec of the second ramp is:

$$S_2 = a \frac{(V_s - V_z) - V_z}{(a)\ (T_r)}$$

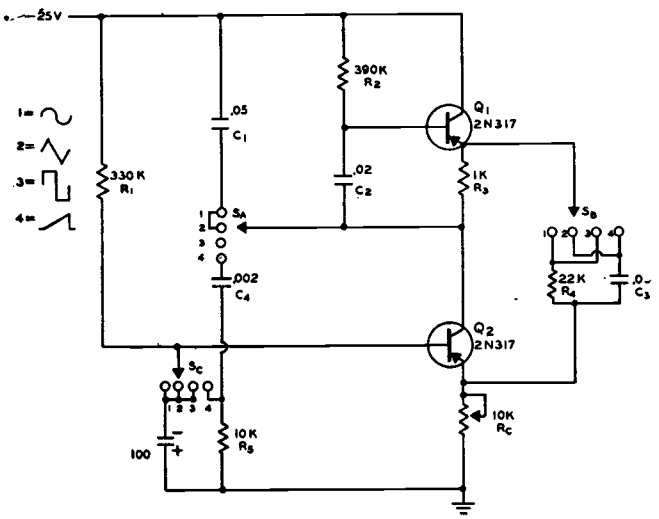


FIG 1—Two-transistor circuit provides choice of four different wave shapes.

Transistorized All-Waveform Generator

WAVEFORM generators are commonly called upon to deliver the following outputs: sine, triangular, square, and sawtooth.

A single circuit capable of delivering all these waveforms has, up to this point, involved a great deal of complexity.

A two-transistor circuit capable of generating all four waveforms is shown in Fig. 1. The function selector is a switch which accomplishes minor circuit modifications which control the shape of the output waveform. The circuit is essentially a common base amplifier in series with a Miller reactance transistor. The reactance transistor simulates an inductance of approximately 20 henrys.

In switch position 1 the circuit is a sine wave oscillator where Q_1, the effective inductive reactance, is shunted by capacitor C_1 to act as a tuned circuit. The feedback is from the emitter of Q_1 to the emitter of Q_2 and is resistance coupled. The emitter of Q_1 is used as the take off point for the feedback loop, producing the effect of a Hartley tapped coil. Resistor R_6 is adjustable, and acts as a feedback control. Frequency is 450 cycles per second with a total distortion of 0.8 percent.

A triangular wave is provided in switch position 2. No components have been changed except in the feedback loop where R_4 has been replaced by C_3. This adds capacitive phase shift back into Q_2 causing it to act as an oscillator and Miller integrator at the same time. The Miller integrator linearizes the sine wave output of the tank circuit, generating triangular wave form.

A square wave results with switch position 3. The feedback is again resistive. Here an LR feedback oscillator is formed where Q_2 is fired on and off by the LR time constant. The switching time is dependent on the circuit constants and the transistor characteristics.

In switch position 4, C_1 is out of the circuit, and sawtooth waves are produced. The feedback is capacitive, and a Miller integrator capacitor C_4 and load resistor R_5 are switched into the base of Q_2. Here the square wave circuit with a Miller integrator feeds the base of Q_2 from the collector of Q_2. This causes the square to ramp to its maximum voltage which produces a linear sawtooth waveform.

The circuit is quite versatile in generating well defined waveforms. It is suitable for applications in which fixed or limited ranges of repetition rates are required.

Triggered Sawtooth Generator

IT WAS FOUND that by connecting the Shockley 4-layer diode with a transistorized integrating circuit a free-running sawtooth generator could be made (Fig. 1). With the addition of a capacitor and a supply voltage change it was found that the sawtooth generator could be triggered into operation and the triggered sawtooth generator (Fig. 2) was conceived.

The wave shape generated by the triggered sawtooth generator is different from most sawtooth generators in that the ramp starts from the steady state condition with a quick drop after which the ramp rises back to the steady state condition. In the conventional sawtooth generator, the ramp starts from the steady state condition and rises to a maximum and then there is a quick drop back to the steady condition.

The supply voltage of the triggered sawtooth generator was set at 18 volts dc, but this was not enough to cause the circuit to run free. The collector of transistor Q_1 is then setting at 18 volt dc. If a

positive pulse of 10 volts is then applied to the collector, the potential between collector and base will be nearly 28 volts and is sufficient to break down the 4-layer diode to a low-resistance path between collector and base. With the collector voltage ap-

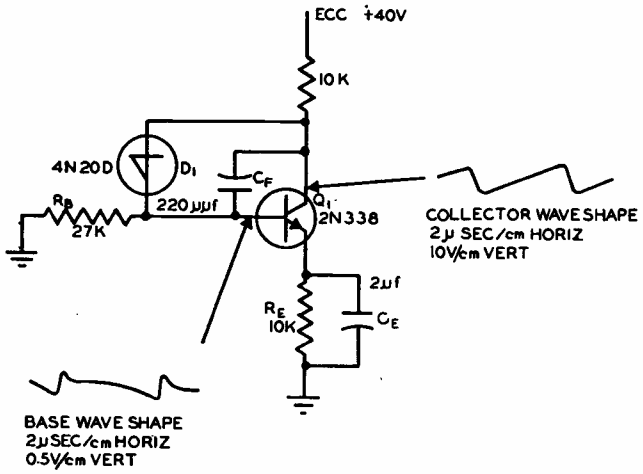


FIG. 1—Free-running sawtooth generator.

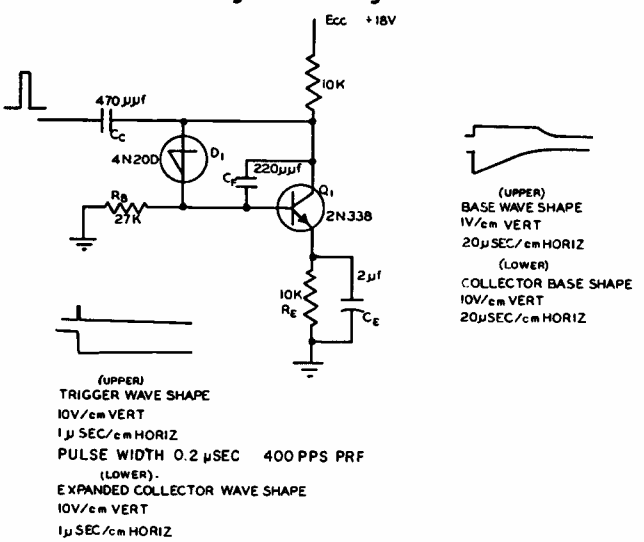


FIG. 2—Triggered sawtooth generator.

plied to the base, the transistor will then pass current and thus the collector voltage will drop.

When the drop between collector and base is down to about one volt, the 4-layer diode will return to a high resistance path and the collector voltage is no longer applied to the base. The voltage on the base, stored in capacitor C_F (about 0.8 v), begins to leak off through R_B and the base to emitter resistance of the transistor. The current through the transistor will start to decrease and thus cause the voltage on the collectory to increase.

The increase in voltage on the collector is fed back to the base through C_F and tends to buck the decrease in base voltage to a much slower rate. The result is a gradual increase of voltage on the collector or a ramp. As the collector voltage rises it eventually reaches the supply voltage of E_{cc} and the ramp stops until the circuit is triggered again.

The free-running sawtooth generator of Fig. 1 operates in the same manner as the triggered sawtooth generator except that the supply voltage is made higher than the breakdown voltage of the 4-layer diode on the free-running circuit. The wave shape seemed to be much better with E_{cc} of 40 volts rather than an E_{cc} of 20 volts which was just enough for oscillation.

Temperature-Compensated Constant Current Generator

IN A VCO application, requiring a constant current source, the wide range of temperatures experienced, —55C to +125C, affected the linearity of the oscillator.

As shown in Fig. 1, the reverse voltage charac-

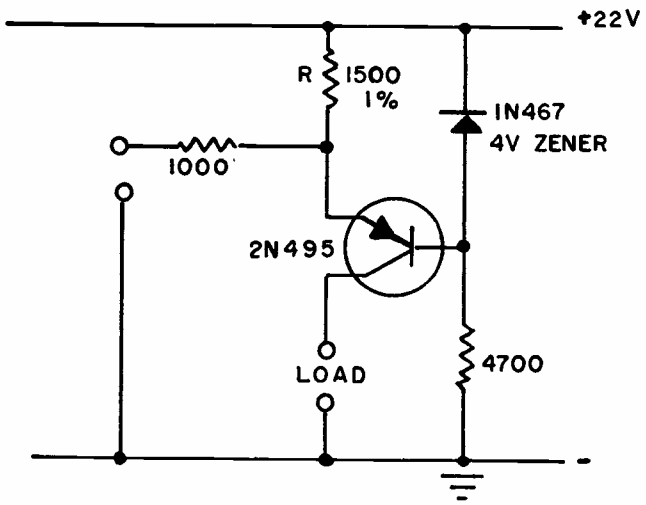


FIG. 1—Constant-current generator is temperature compensated.

teristic of the diode, in conjunction with the base-emitter characteristic of the transistor, stabilizes the collector current by maintaining a constant voltage across resistor R.

The V_{be}, of the 2N495 transistor selected, exhibits a temperature coefficient of —2 mv/C°, and dictated a similar coefficient for the zener diode. The 1N467 was found to have this property.

A similar arrangement may be devised using an npn type of transistor. Both circuits may be used together to provide a bipolar current source.

A more satisfactory type of transistor temperature compensation is thus provided than can be normally attained using conventional non-linear components.

Linear Sweep Generator

THE CIRCUIT shown in Fig. 1, generates linear sawtooth voltages over the range of 100 μsec to, and above 10 seconds, of constant amplitude. It offers interesting possibilities as a gated or free-

running sweep circuit.

The basis of operation is Miller type feedback with T_4 as amplifier, C_T and R_T the timing network and T_3 a gate. Transistors T_1 and T_2 provide an impedance changer to match the low input impedance of T_4.

In the steady state, transistor T_3 is cut off, T_4 is on, its current supplied through R_6. The base of T_4 is held positive by returning R_T to the supply voltage E_{cc}.

A positive gate on the base of T_3 drops the collector voltage e_c. This change occurs across timing capacitor C_T and is transmitted through the impedance changer to the base of T_4 cutting it off. Next follows the linear rundown at the collector of T_3, characteristic of phantastron type circuits.

The approximate relationship between the supply voltage and the timing network is

$$e_c = E_{cc}(1 - t/R_t C_t)$$

This was found to hold true for R_T in the order of 1 megohm. For R_T above that value, shunting effects of the impedance changer have to be considered. The slope of the sawtooth varies linearly with changes of C_T. Sweeps of 100 μsec to 10 seconds were consistent with capacitance variation from 0.0001 μf to 1 μf. The amplitude remained constant over entire range. Output waveforms are in Fig. 2.

An attempt to make the circuit free running was also successful. This was done by introducing positive feedback from the collector of T_2 to the base of T_3 through a 330K resistor (between points C and A in Fig. 1). Other ways of accomplishing the same are still being investigated.

This circuit will perform equally well with npn and pnp germanium transistors. 2N388 and 2N396 were tested (reversed power supplies) without change in performance. With silicon transistors (2N118), small circuit modifications were necessary, mainly due to the higher saturation resistance of T_1 and T_2. Nevertheless, there seems to be no major limitation in that respect.

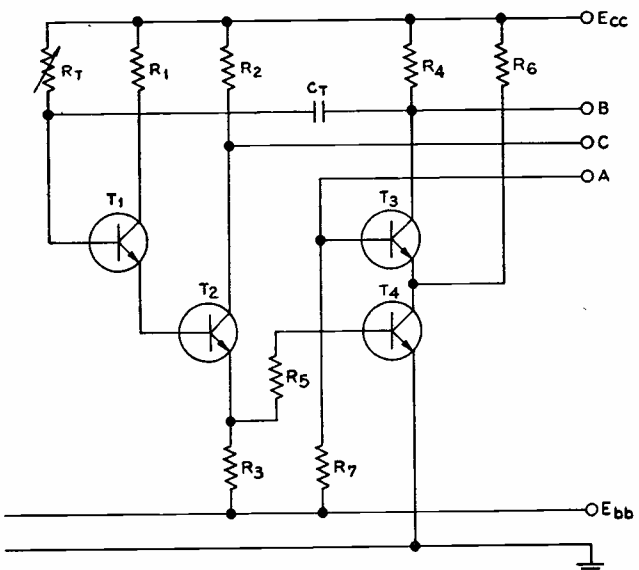


FIG. 1—Ohmic values of resistors follow: R_1 and R_5 —100; R_2 —2700; R_3, R_4 and R_6 —4700; R_7 —100K. All transistors are 2N388 and E_{cc} is —22v, and E_{bb} is —6v.

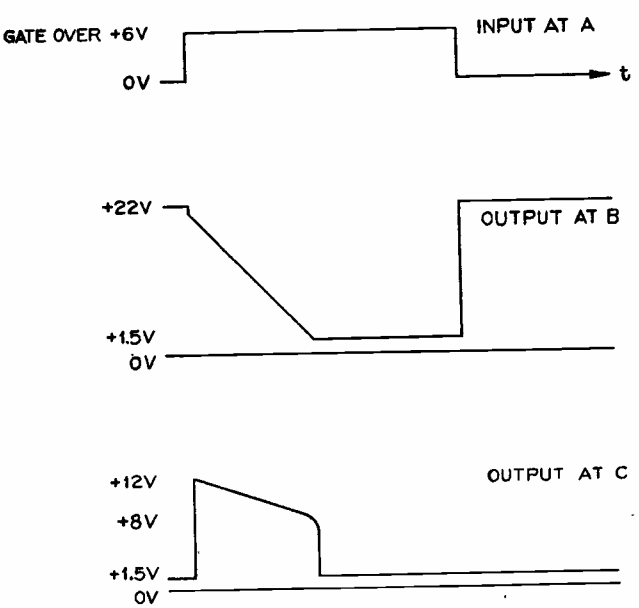


FIG. 2—Output waveform at designated points of linear sweep generator circuit.

Radar Target Acceleration Simulator

IN TESTING radar range tracking systems, it is often desirable to provide a target with a controlled acceleration. A rather elemental method for providing such a target is to use a phantastron delay circuit modified by the addition of a synchronous motor driven capacitor in the feedback loop.

A pulse used to trigger the phantastron is considered the radar transmitted pulse, and a second pulse, triggered by the trailing edge of the phantastron square wave, the radar echo. Time between pulses, or range, can be set to desired values by combinations of resistance between a positive supply and grid, and capacitance between plate and grid of the tube used in a phantastron circuit. Capacity variations produce essentially linear delay var-

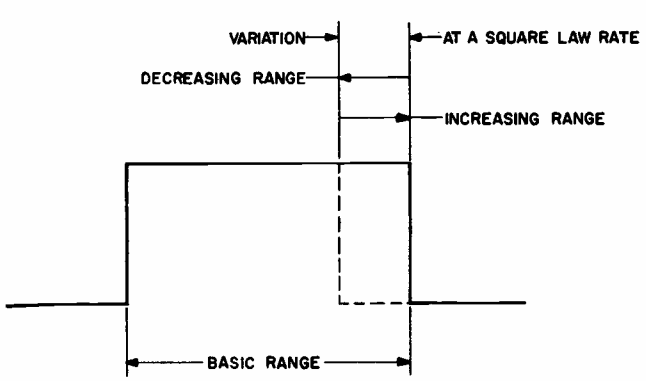


FIG. 1—Square law function is desirable.

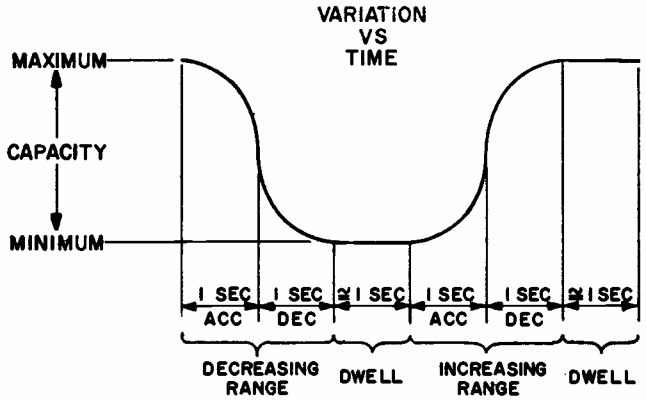


FIG 2—Graphical representation of capacitor.

iations. Therefore, a variable capacitor having a square law characteristic, driven at constant velocity will, when used in this circuit, cause the trailing edge to move in time at a square law rate. This in conformance with the standard acceleration

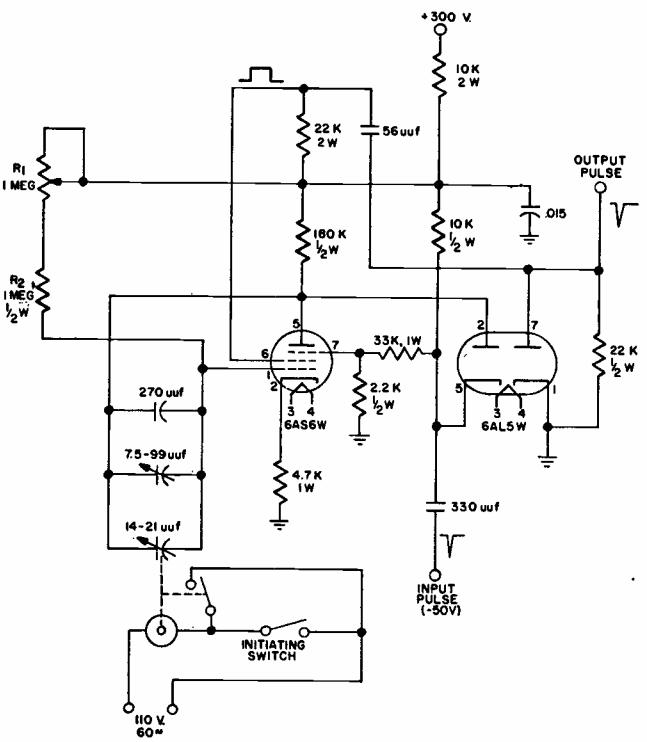


FIG 3—Circuit for simulating acceleration.

formula, $S = (at^2)/2$ which is a square law function. See Fig. 1.

Straight line frequency capacitor plate design is applicable or the procedures outlined in the article "Designing Variable Capacitors for Function Generators", page 131 of the March 1960 issue of ELECTRONIC Equipment ENGINEERING can be used. If acceleration and deceleration are desired, in decreasing and increasing range, capacity variation will be as shown in Fig. 2. A no change or dwell position is desirable if single functional cycles are desired. During this period, an auxiliary cam may be used to operate a stopping limit switch. An overriding switch initiates the action.

This capacitor is designed to function as follows: 1. Decrease capacity at a square law rate for one second. 2. Continue capacity decrease, but at a decreasing square law rate for one second. 3. Dwell for a period at minimum capacity. 4. Increase capacity at a square law rate for one second. 5. Continue capacity increase, but at a decreasing square law rate. 6. Dwell for a period at maximum capacity.

The moving plates will be cardioid shaped, formed

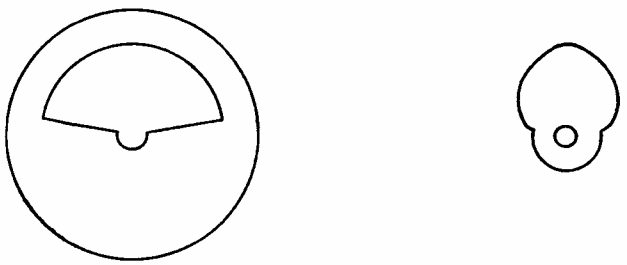


FIG 4—Configuration of capacitor plates.

by a straight line frequency plate folded back on itself. The fixed plates will be round with straight entering edges. Attention must be made to provide a standard minimum to avoid discontinuities, and to keep capacity to ground very low. To determine the amount of capacitor variation necessary, the following procedure is used. For example, say 200 G acceleration is desired, in one second:

$200\ G = 200 \times 32.2\ \text{ft/sec/sec} = 6440\ \text{ft/sec/sec}$

direct radar range $\cong$ 1000 ft per μsec

then, $200\ G = 6.44\ \mu\text{sec/sec/sec}$

and, $S = 3.22\ \mu\text{sec}$.

Therefore, during a period of one second, the shift of the target echo pulse amounts to 3.22 μsec, and the capacitor is designed to provide this.

Some adjustment of acceleration is possible with this unit. See Fig. 3. Components R_1, R_2, C_1, C_2 and C_3 determine the length of square wave. Values are chosen to the range desired. Capacitors C_1 and C_3 being normally fixed, adjusting R_1 to a small value, and C_2 to a large value to obtain the required range, will have the effect of decreasing the acceleration caused by operating C_1, since it will be a smaller proportion of the total capacitance in the RC circuit determining the length of square wave.

Conversely, adjusting R_1 to a large value and C_2 to a small value to obtain the required range, will have the effect of increasing the acceleration caused by operating C_1, since it will be a larger proportion of the total capacitance in the RC circuit determining the length of square wave, or range.

Circuit values shown result in a transmitted to echo pulse of approximately 230 μsec and adjustable acceleration. This can be changed to suit particular applications by changing the timing constants in the phantastron circuit. Figure 4 illustrates one capacitor design that was used with success.

Efficient Even Harmonic Generator

FREQUENCY multiplication may be performed either by class C operation of amplifiers or by use of a rectifier with both types requiring high Q filters. In either case, the efficiency is extremely low and additional amplification and filter stages are necessary. The combination of the rectifier followed by an amplifier is the preferred choice for maximum efficiency. Such circuits have been discussed in the literature and proposals made which increase the efficiency by using the dc from the rectifier to operate the following amplifier. A still further improvement is obtained by the circuit to be described which employs a ring modulator in place of the rectifier multiplier for the production of even harmonics.

The maximum conversion gain of the rectifier-multipler alone is $G_c = 1/n^2$ where n is the harmonic number. With the following amplifier a transistor of high power gain, the overall conversion gain will still be less than unity with a typical value being 0.9. Note that it is no longer a truly passive device.

Figure 1 gives the circuit of the passive multiplier. No special effort was made to obtain good balance. Tests were made with the fundamental frequency

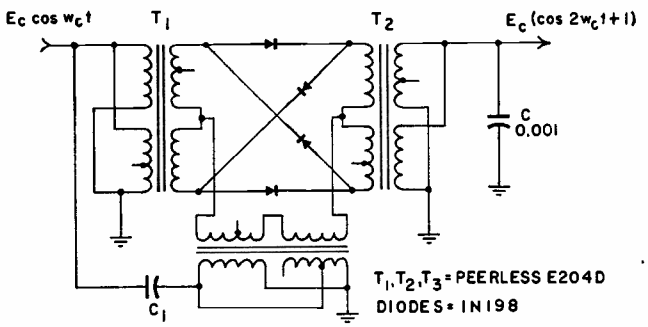


FIG. 1—Passive efficient even harmonic generator.

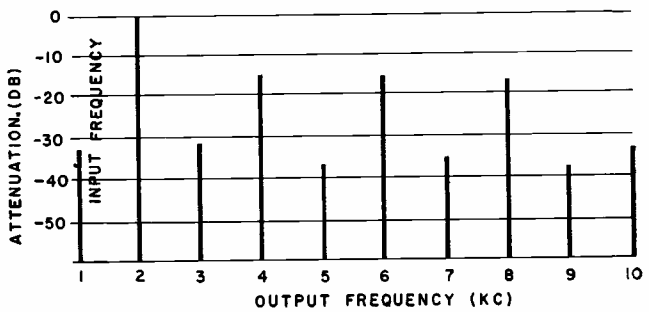


FIG. 2—Harmonic generator outputs.

of 1 kc. At 2 kc, the conversion gain was 0.76 and at 4 kc, it was 0.14. That is, the conversion gain was approximately 3 times the maximum gain of a rectifier multiplier. At the second harmonic, an insertion loss of only 3 db makes an amplifier not essential except where large amounts of power are required. The output at other harmonics is of interest. This is depicted in Fig. 2 as the wave analyzer readings for the laboratory model of Fig. 1. The conversion gain for the fourth, sixth and eighth harmonics is essentially the same. All the odd harmonics and the even ones above the eighth can be considered as balanced out since all fall below the 30-db attenuation level as does the fundamental. The rejection of the fundamental is a highly desirable feature of this multiplier.

Theoretical analysis of the circuit is derived from the output of an ideal balanced modulator which is

$$e_o = E_m \cos(w_c + w_m)t + E_m \cos(w_c + w_m)t$$

Where w_c equals w_m and E_m equals E_c, this becomes

$$e_o = E_c(\cos 2w_c t + 1)$$

thus indicating the predominace of the even harmonics. Further description of the outputs for this special case can be obtained from the knowledge that less than 60 db attenuation will occur for the following,

nf_c
$(2n + 1)f_c \pm f_c$
$(2m + 1)f_c \pm (2n + 1)f_c$
$2mf_c + 2nf_c$
$(2m + 1)f_c \pm 2nf_c$

Capacitor C in Fig. 1 was chosen to reject all unwanted harmonics. Better tuning of the output than was attempted in this model can considerably improve the conversion gain and spurious rejection. Practical conversion gains at the second harmonic can approach 0.9.

Capacitor C_1, experimentally selected, can be used to reduce the phase shift introduced by the multiplier where this is of interest. It is not essential to the operation of the harmonic generator.

4-Layer Diode Sweep (Synchronous)

THE CIRCUIT in Fig. 1 produces a linear 20-volt sawtooth with few components. With adjustment of component values its maximum sweep rate can reach 100 kc. Besides simplicity and a wide latitude of sweep rates, this circuit features synchronous operation and very fast retrace.

Since the ratio of off to on resistance is about one million to one in the 4-layer diode D_1, the sawtooth as shown in Fig. 2 has good linearity and very fast retrace. This fast retrace eliminates the need for blanking in oscilloscope applications.

The use of diode D_2 in the sweep circuit allows synchronous operation over a large range of signal amplitudes. Thus, in oscilloscope applications R_1 will not require additional adjustment after once set for minimum signal. Synchronous switching occurs because diode D_2 is open and the voltage across D_1 is greater than sweep voltage, when the signal voltage is negative.

The sweep voltage and synchronizing signal cause

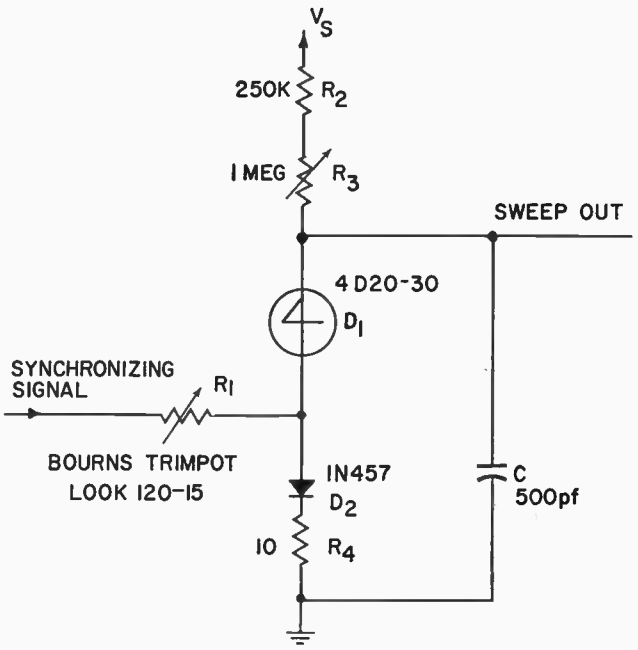
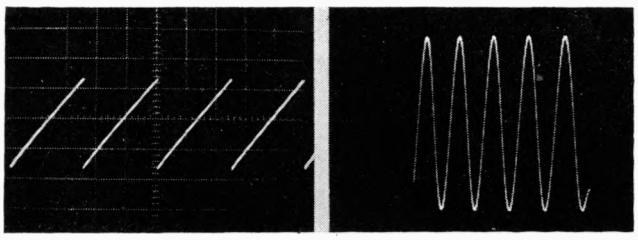


FIG. 1—Resistors of the synchronous sweep circuit are noninductive types.



Linearity of the sweep waveform is apparent in Fig. 2, left. Some 10-kc sine waves using the four-layer diode for sweep are shown in Fig. 3, right.

the voltage across D_1 to obtain the 4-layer switching voltage and capacitor C discharges through D_1 and D_2. The discharge current decreases to a value less than the 4-layer holding current and D_1 opens. Resistor R_4 serves as a current limiter to protect the diodes.

The approximate frequency of operation is given by

$$f \simeq \frac{V_s}{V_{D_1}(R_2 + R_3)C}$$

where V_{D_1} is the switching voltage.

Figure 3 shows an unblanked oscilloscope trace of a 10-kc sine wave using this oscillator for sweep.

Fast-Rise, Long-Width Pulse Generator

THE CIRCUIT shown in Fig. 1 was developed to provide a variable, long-width pulse with fast rise and fall times. Although the width in our application needed only to be as long as 20 msec, the principle of operation will allow a 1 min pulse to be generated with rise and fall times of 1 μsec or less.

The initial conditions are Q_1, Q_2, Q_4 off, Q_3 on, and CR_1 held in its low voltage state by current

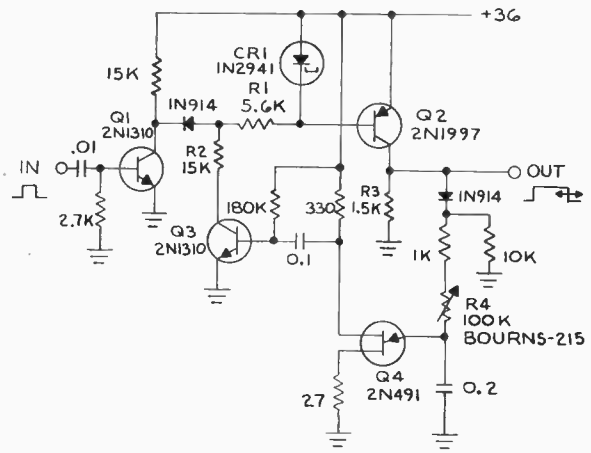


Fig. 1. Pulse generator.

through R_1 and R_2. A positive input pulse turns Q_1 on briefly, allowing sufficient current to flow through R_1 and the tunnel diode, CR_1, so that it sets to its high voltage state. This action turns on Q_2 and is the start of the pulse. Output voltage will remain across R_3 until the tunnel diode is returned to its low voltage state.

The output voltage is fed through an R-C integrator to the emitter of Q_4, a unijunction transistor. When the peak-point emitter voltage is exceeded, Q_4 fires. The resulting negative pulse turns off Q_3. As Q_1 is also off at this time, the reduced current through CR_1 allows it to reset to its low voltage state. Q_2 now turns off, and the pulse is complete.

Pulse width is adjusted by R_4. Rise and fall times are determined primarily by the switching characteristics of CR_1 and Q_2.

Variable Pulse Generator

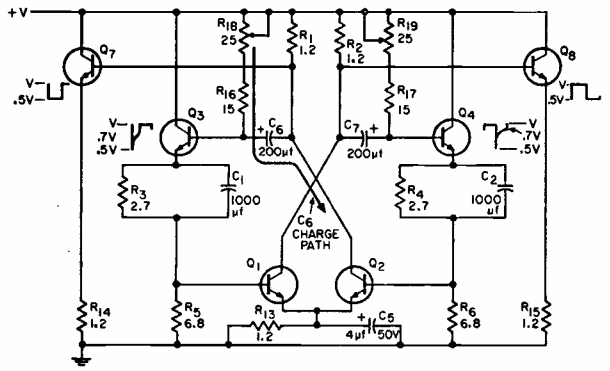
THIS CIRCUIT is a variable frequency generator of low impedance pulses. It operates with any power supply voltage from 1.5 to 20 v, and will generate symmetrical or nonsymmetrical pulses at rates from less than ½ ppm to more than 200,000 pps.

The capacity values chosen for C_6 and C_7 determine the center frequency of operation. Controls R_{18} and R_{19} provide a frequency adjustment of ½ to double the center frequency. These controls may also be used to individually adjust up and down pulse durations.

When operating with a 12 v power supply, values for C_6 and C_7 of 200 pf were found to give a center frequency of 100 Kpps; values of 1,000 μf gave a center frequency of 1 ppm.

Basic circuit operation is as follows: At any instant either Q_1 or Q_2 is saturated and the other of the pair is cut-off. The voltage at the collector of the cut-off transistor is approximately the supply voltage; the voltage at the collector of the saturated transistor is approximately ½ the supply voltage. These two levels are provided as reciprocal low impedance (700 ohms)

output signals via emitter followers Q_7 and Q_8.



Pulse generator provides variable frequencies from low impedance pulses. All resistors are in kilohms, 10 percent, ½ w; all transistors are 2N35 or similar; all unmarked capacitors are in picofarads.

Transition of the output signals from one state to the other occurs when the cut-off transistor comes into saturation. For example, assume Q_2 had been cut off and just came into saturation; this causes a negative spike to pass via C_6, Q_3 and R_3 (by-passed by C_1) to the base of Q_1, thereby cutting Q_1 off. Q_1 will now remain off until the voltage at the Q_1 base reaches ½ the supply voltage. This occurs when C_6 has been sufficiently charged through R_{18} and R_{16} to bring the voltage at the base of Q_3 up to 7/10 of the supply voltage. When this happens Q_1, coming back into saturation, sends a negative spike through C_7 causing Q_2 to cut-off. Now the duration of this state is determined by the chosen values of C_7, R_{19} and R_{17}.

This circuit, feeding into a Schmitt circuit, has been in use for controlling repetitive operation of certain analog computers. It has also been used as a source for the checkout of digital circuits. Further utility may be gained at larger potentials by using higher voltage transistors.

Unexplored but potentially useful applications of this circuit, may be discovered by substituting an information source for the supply voltage thereby obtaining modulated information as the output signals for Q_7 and Q_8.

Rectangular Waveform Generator

THE CIRCUIT shown in Fig. 1 is capable of generating rectangular waveforms of variable frequency and symmetry without interaction of the functions. Closer observation of Fig. 1 reveals that the network consists of conventional circuits coupled together to obtain the desired results and can be used to modulate a small transmitter for remote control purposes. At a receiver, the signal is decoded, thus separating the frequency and symmetry components which are used for two remote functions.

The generator consists of three well known circuits whose functions are presented here. Q_1 is a standard blocking oscillator. Q_2 acts as a constant current source which allows C_1 to discharge linearly over the frequency range determined by proper choice of C_1. R_1 controls the fine frequency adjustment by forward biasing transistor Q_2. As Q_2 becomes biased into conduction, the collector-emitter junction resistance becomes lower, allowing C_1 to be discharged sooner, thus increasing the frequency [Ed. note: $f = 1/2\pi r_c c_1$]. The output waveform at the collector of Q_2 is a linear ramp or sawtooth wave.

Transistor Q_3 is connected as an emitter follower

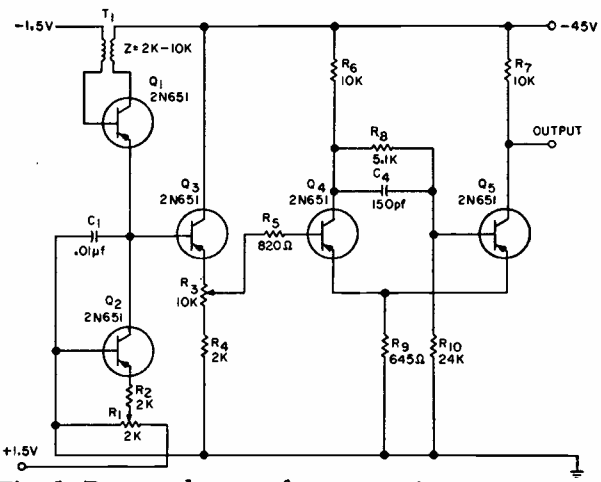


Fig. 1—Rectangular waveform generator.

which allows some isolation between the sawtooth generator and the following circuit. Potentiometer R_3 controls the symmetry of output waveform.

Transistors Q_4 and Q_5 form a conventional Schmitt Trigger with the trip point set at approximately −2 v. Varying this trip point will affect the symmetry range

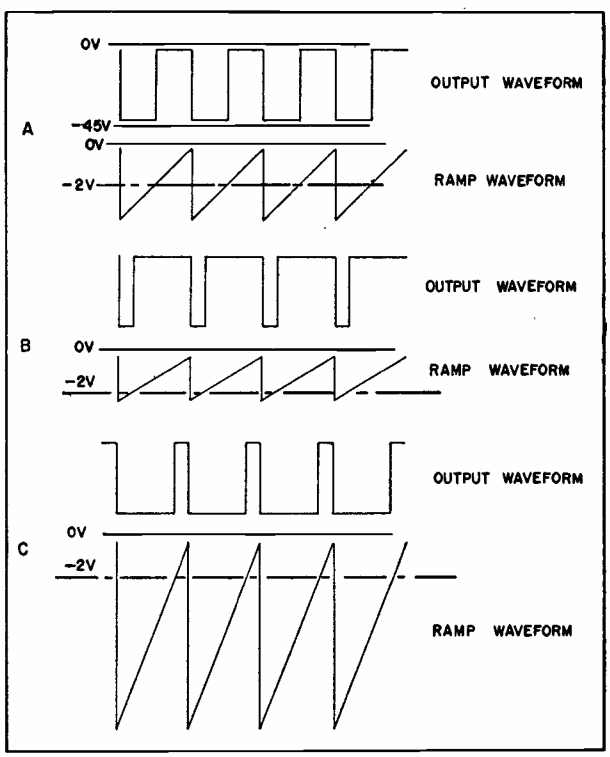


Fig. 2—Waveforms showing how output wave varies with amplitude of ramp voltage (setting of R_3). At A, symmetrical wave results. See text for conditions that cause waveforms at B and C.

attainable.

A symmetrical waveform is obtained (Fig. 2A) as follows: R_3 controls the amplitude of the ramp voltage applied to the base of Q_4. As the ramp voltage begins to rise, it reaches the −2 v trip point of the Schmitt Trigger. Transistor Q_5 turns on and remains on until the ramp voltage drops rapidly below the lower trip point of the Schmitt Trigger. Since the output waveform is symmetrical, the trip point is reached at the center of the rising ramp voltage. For other than symmetrical waveforms the ramp voltages is varied so that Q_5 remains on for a shorter (Fig. 2B) or longer (Fig. 2C) time depending on the setting of R_3.

Low priced components are used throughout the circuit, and almost any type of pnp transistor can be used with excellent results. The circuit operates normally over a wide voltage range (approximately −15 v to −45 v) supply. With a 0.01μf capacitor for C_1, the frequency range is variable from 60 cps to 7 kc.

Gated-Beam Tube Square-Wave Generator

With numerous solid-state/semiconductor designs and applications appearing lately, perhaps it would be technically refreshing to present a four-stage tube design reminiscent of the good old days.

This useful design was conceived to develop a square-wave generator unit or instrument capable of amplifying frequencies without attenuation to—at a minimum—the tenth harmonic of the square-wave fundamental, from which a signal output starting below 50 to 500,000 pulses/second could be adjusted over a desirable range without waveform distortion.

This is achieved by employing a twin-triode 12AU7 as a symmetrical multivibrator, using a 6BN6 as the gated-beam tube, a 6AN6 as a wide-band amplifier stage, and a 6AG7 tube as a cathode follower output. Separate frequencies of operation are provided by changing the grid-plate R-C networks by means of switching S_1 and S_2. (See Fig.1

The non-sinusoidal signal appearing across plate load R_2 is applied through C_{11} to the gated-beam clipper, V_2. Both plate and screen voltages on this tube must be kept low for good clipping.

A square-wave signal appears across plate load R_{20} and is applied via C_{15} to the cathode follower output stage which permits a low impedance output. Small value plate load resistors were selected for each amplifier stage to provide wide frequency response and to minimize distributed capacitance effects. This is desirable so that the final square wave signal would be free of overshoots, damped ringing, and/or high frequency phase shift problems.

Output signal level may be adjusted by means of R_{27} from approximately 0.8 to 8 volts peak to peak. R_{26} and R_{28} were added later to prevent over-adjusting the control to extremes. Rise time is good and for the 500-kc signal is better than 0.07 microsecond.

Since a square-wave signal is satisfactory for checking an amplifier to at least the tenth harmonic of its fundamental repetition ratio, it is not necessary to provide continuous frequency coverage in a square-wave generator such as this. Hence, four or five separate frequencies were chosen as useful in normal occasions. For these reasons repetition rates selected were 50, 1K, 10K, 100K and 500K pps (position A of switch). These were applied with equal versatility to the design applications and testing of various audio, pulse, and video amplifier designs.

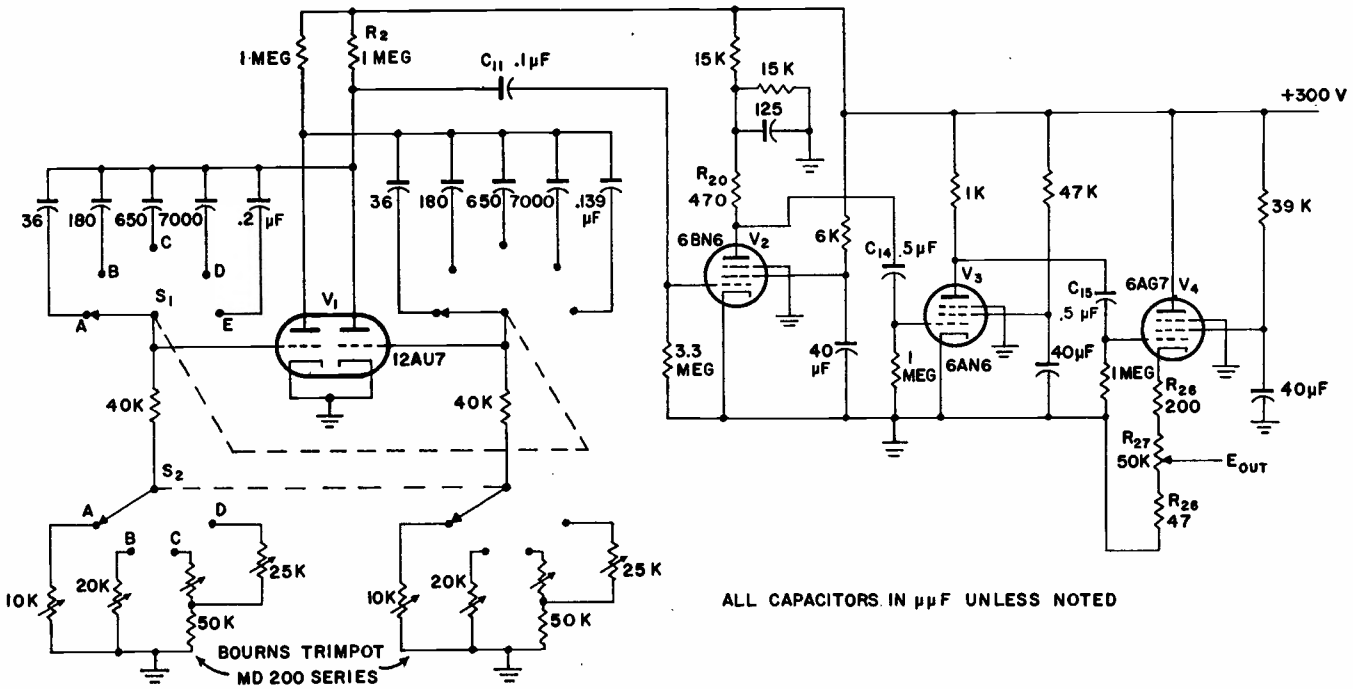


FIG. 1—Test generator using gated-beam concept.

Transistorized 15 Watt 60 Megacycle Generator

RECENT ADVANCES in the field of VHF power transistors have resulted in applications that were not possible a short time ago. Such an application is the 15 watt 60 megacycle generator which is described here.

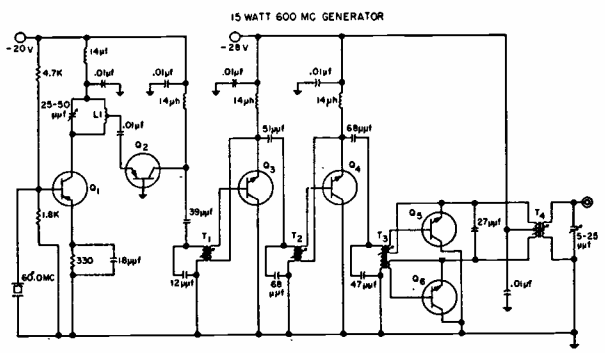


Fig. 1–15 WATT 600 Mc Generator

NOTES:

1—ALL RESISTANCE IN OHMS K = 1000

2—ALL TRANSFORMERS ARE #22 WIRE, BIFILAR WOUND ON CTC LS6-0-2C4L FORMS

3—Q_1, Q_2 = 2N1143 (TI)
Q_3 = 2N1505 (PSI)
Q_4, Q_5, Q_6 = PT613 (PSI)

4—L1 = 5 TURNS #18 WIRE, ⅜" DIAMETER

5—T_1 { PRIMARY = 7 TURNS; SECONDARY = 2 TURNS
T_2 { PRIMARY = 4 TURNS; SECONDARY = 2 TURNS
T_3 { PRIMARY = 4 TURNS; SECONDARY$_1$ = 2 TURNS; SECONDARY$_2$ = 2 TURNS
T_4 { PRIMARY = 5 TURNS (CENTER TAPPED); SECONDARY = 4 TURNS

The output of such a generator was checked with a wattmeter which indicated an output of 15 watts. A sampling scope displayed a visual clean waveform and a spectrum analyzer showed all unwanted harmonics to be down 40 db or more.

The bandwith of this circuit is slightly greater than 6 mc and is symmetrical around the fundamental frequency. This generator is transformer coupled rather than most transistorized power amplifiers, which usually contain "pi" or "T" coupling. Various coupling methods were tried in this circuit, but none work as well as the transformer coupled circuits. Too, transformer coupling showed no more loss than other methods and was not as critical to tune.

Q_1 is a common oscillator circuit using the collector to emitter capacitance of the device as a feedback loop. If necessary, a small shunt capacitance may be added. This method works well above 50 megacycles for most transistors. However, for frequencies below 50 megacycles, the phase shift in such a circuit may not be adequate to provide efficient operation. When working in the megacycle range, stray capacity may be a serious problem. Therefore, it may be necessary to tap the feedback capacity on the collector tank circuit to obtain the proper value of capacitance. However, oscillators at 30 megacycles have been constructed in which this was not necessary when used with the transistor shown in the figure.

Q_2 is operated in the common-base configuration to permit ac coupling to the oscillator, while still providing sufficient oscillator-to-load isolation.

Q_3, Q_4, Q_5 and Q_6 are all power amplifiers with Q_5 and Q_6 operating in the push-pull mode. All of the stages are operated with grounded-collector configurations to obtain maximum power dissipation. The collector leads are tied to the transistor case and the transistors are heat sinked. Any low frequency oscillations that may occur in the power stages can be minimized by placing 100 micro-henry chokes in series with the emitters. This, however, is usually not necessary.

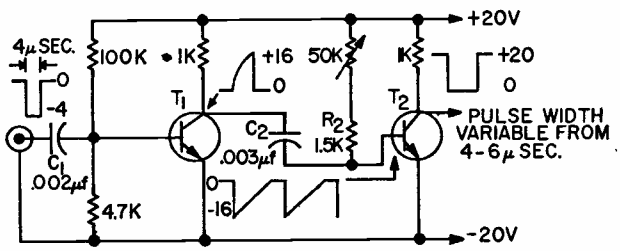
When terminated by a 50 ohm load, the power output in succeeding stages is approximately 100 milliwatts from Q_2, 1 watt from Q_3, 3 watts from Q_4 and 15 watts at the output. By operating Q_5 and Q_6 at 40 volts dc, a power output of better than 20 watts is obtained. However, to operate continuously at this level would require some type of cooling device or a heat sink of almost infinite size. All of the power stages in either case operate at greater than 50 per cent efficiency.

High-Duty-Cycle Pulse-Width Generator

THIS CIRCUIT generates a stable and variable pulse width from a fixed pulse-width input. The generator uses two 2N1308's. It accepts a negative pulse at the input. A positive-pulse input can be applied by changing T_1 and T_2 to type 2N1309 and reversing their collector voltages.

The generator, though simple and stable, has a maximum duty cycle as high as 93 percent. The output voltage is 20 v peak-to-peak into an open circuit and the output impedance is 1000 ohms. When terminated in a 1000-ohm load, the output voltage is 10 v peak-to-peak. The circuit operates as follows:

A 4-v negative pulse is applied to the base of T_1, an amplifier-inverter. Capacitor C_2, resistors R_1, R_2 and the input base resistance of T_2 differentiate the waveform at the collector of T_1 into a 16-v sawtooth which is negative in polarity. R_1 changes the bias of T_2 allowing its quiescent state to vary over the slope of the sawtooth. T_2 saturates with only a few tenths of a volt, so the waveform at the collector of T_2 will be a square wave, the width of which is controlled by potentiometer R_1.



Variable-pulse-width generator provides very high duty cycle.

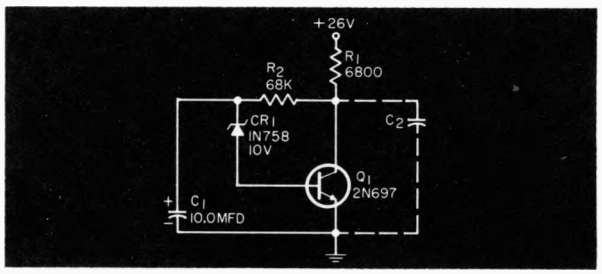
The pulse generator has been operated with repeti-

tion rates as low as 30 cps and as high as 2 mc, with pulse widths of 600 μsec to 100 nsec, respectively.

With the input and circuit values as shown in the schematic, the output is as shown and the maximum duty cycle is 92 percent with a 63-μsec input rep rate. For a 4-v peak-to-peak input, 600-μsec wide, with a 16,666-μsec rep rate, C_1 should be 0.33 μf and C_2 should be 1 μf. Then the output would be 20 v peak-to-peak, with pulse width variable from 600 to 16,200 μsec and maximum duty cycle 93 percent.

One-Stage Semiconductor Noise Generator

THE CONVENTIONAL WAY to design a semiconductor noise generator is to amplify the noise voltage developed across a conducting zener diode. However, note that if the noise level is 1.5 mv, a gain of 80 db is required to produce 15 volts, which means at least 3 stages of amplification are needed. But since the transistor is primarily a current-amplifying device, and the noise current of a zener diode is about 1.5 mv/50 ohms or 30 μa (where 50 ohms is the dynamic impedance of the zener diode), a much more efficient design is possible.



One-stage semiconductor noise generator.

The figure shows a circuit in which the zener current is fed to the base of transistor, which has a nominal current gain of 75. The zener diode serves two purposes: it produces a noise signal current, and it stabilizes the collector operating point. The drop across R_2 is about 2 volts. The load resistor R_1 determines indirectly the zener current. Noise signal across R_1 is 15 volts peak to peak. If C_2 is added to filter out the high frequency end, the amplitude drops (for $C_2 = 0.1$ μf, $e_{out} = 0.5$ v). ◆◆

Improving Linearity in Transistorized Horizontal Sweeps

CONVENTIONAL TECHNIQUES for linearizing horizontal TV sweeps are not practical in transistorized systems because of the every narrow dynamic range of the damper diode and the switching characteristic of the driver transistor. The method to be described here, however, provides better than ±0.5 percent linearity, referred to the displacement error from a theoretical straight line. Flatface correction is also employed so that the linearity figure is as observed on the kinescope.

The technique consists of placing a transformer in the yoke circuit as shown in Fig 1. The current I is adjusted to be about 10 percent greater than I_L by adjusting L, and

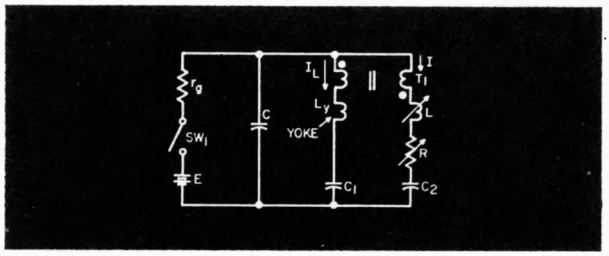


Fig. 1. Equivalent circuit.

is shaped by R to compensate for the second-order component of the sweep current due to yoke resistance and switch losses. The correcting voltage is applied to the yoke leg of the circuit through transformer T_1 which consists of two tightly coupled windings on a powdered iron core.

A practical circuit, shown in Fig. 2, uses this technique to deflect a 16-in. CRT employing a 52-deg deflection angle and 15-Kv acceleration voltage. The line rate was 28.35 kc, 945 lines. Linearity was better than ±0.25 percent on the breadboard. The supply voltage can be varied to vary the width or amplitude of the sweep. C can be increased for deflection at the standard 525-line rate.
Practical circuit coil data:

L_1: 150 turns No. 30 enameled wire on No. 187EI4914 core (Magnetic Metals Co.)

T_1: Primary and secondary both 7 turns No. 24 wire on powdered iron core. Use bifilar windings.

T_2: Primary: 150 Turns No. 30 wire.
Secondary: 30 Turns No. 26 wire.
Core: No. 187EI4914.

Yoke, Ly: Syntronics Y62-BB8P C3431-3-6, 160μh total.

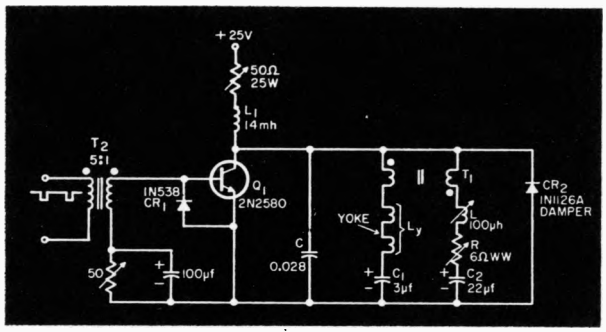


Fig. 2 Practical deflection circuit.

Unijunction Triangular Wave Generator

IN THIS CIRCUIT two current generators produce a triangular wave by alternately charging and discharging a capacitor. A unijunction transistor and diode function together as a switch to reverse the slope of the ramp.

Transistor Q_1 acts as a current generator supplying I_1, and transistor Q_2 acts as a current generator for I_2. ($I_1 > I_2$.)

Let us assume that Q_3 is off and the emitter voltage of Q_3 is V_1 at $t = t_o$. (See Figs. 1a and 1b.) The diode D_1 is forward biased and C_1 is being charged by the current ($I_1 - I_2$). The emitter voltage, v_E, also is rising; when $v_E = V_p$ at time t_1, Q_3 fires, causing v_E to fall to V_1 along the path indicated in Fig. 1c. The diode is now reverse-biased, and Q_2 begins to discharge C_1 with the current I_2. When the capacitor discharges to V_1, the diode becomes forward-biased. The current generators produce a net current (I_1

$- I_2$), and C_1 holds $v_E = V_1$, but this point is below the emitter characteristic of Q_3, so Q_3 turns off to complete the cycle.

The value of the positive slope is given by $(I_1 - I_2)/C$ and the value of the negative slope is given by $-I_2/C$. The peak-to-peak voltage of the wave is $(V_p - V_1)$.

The potentiometer is used to adjust the wave's symmetry. An emitter follower or similar high-impedance stage can be used to take the output directly from the collector of Q_2.

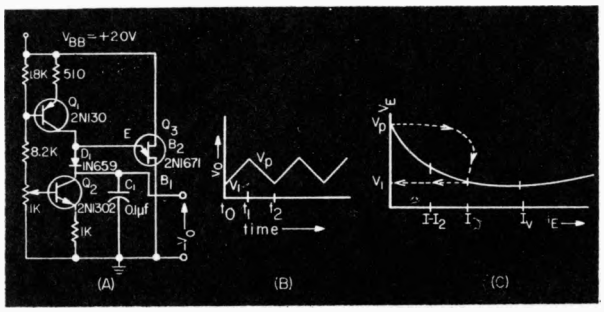


Fig. 1. UJT triangular wave generator (1a) with output wave (1b) and UJT switching path (1c).

The design criteria for the circuit are: $I_1 \leqslant 2/3\ I_v$; $I_2 \leqslant 2/3\ I_1$; $V_{B2} < V_1$; $V_{B1} > V_p + V_D$; and $C_t > C_{cr}$, where I_v is the UJT's valley current, V_{B1} and V_{B2} are the dc emitter voltages at the emitters of Q_1 and Q_2, V_P is the UJT's peak voltage, V_D is diode D_1's threshold voltage, and C_{cr} is the critical capacitance that will just sustain oscillation in the UJT. The factor 2/3 in the first two criteria is a rule of thumb which is not hard and fast.

I_1 and I_2 in Fig. 1a were set at 6 and 3 ma respectively to be compatible with the 8-ma minimum valley current of the 2N1671; V_{B2} is held at about 3 v maximum. The currents I_1 and I_2 and the value of C_1 may be easily changed to obtain variations in symmetry, slope and frequency. With the values shown, the frequency is about 2.5 kc. ◆◆

Synthesis of Ignition Noise in the VHF Band

IN DESIGN of mobile communications receivers it is often advantageous to have a laboratory source of simulated ignition noise for purposes of research and development.

Ignition noise, as generated by internal combustion engines, consists of high level, short duration pulses of unpredictable wave shape. The pulse repetition frequency of these pulses is dependent on engine speed. The problem of synthesizing ignition noise is primarily that of generating a wave shape which has the highest average noise value in the frequency band desired. The frequency band in this case is 132 to 165 mc.

Consider first a repeated triangular pulse which is possibly the closest approximation to the actual wave shape of ignition noise pulses (Fig. 1).

The spectral distribution of this wave shape is of the form $(\sin x/x)^2$ where $x = n\pi t_o/T$.[1] A plot of the function is shown in Fig. 2.

The value of the nth harmonic in the Fourier series expansion for a repeated triangular pulse is given by

$$C_n = 2A_{avg}\left[\frac{\text{Sin } n\pi\ t_o/T}{n\pi\ t_o/T}\right]^2 \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

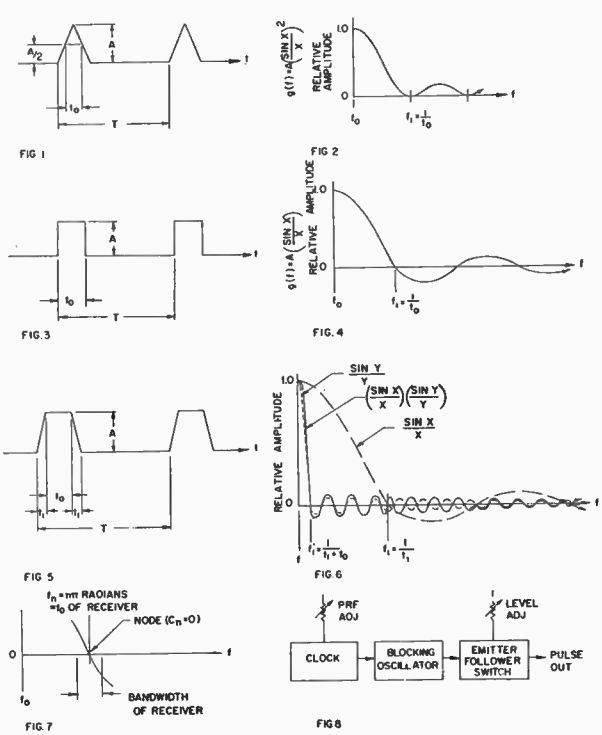
Consider now a repeated square pulse (Fig. 3) which has a spectral distribution of the form $\sin x/x$ where $x = n\pi t_o/T$.[1] A plot of this function is given in Fig. 4.

The value of the nth harmonic of the Fourier series expansion for a repeated square pulse is given by

$$C_n = 2A_{avg}\left[\frac{\text{Sin } n\pi\ t_o/T}{n\pi\ t_o/T}\right] \quad \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

By comparing Eq. 1 and 2 it is obvious that C_n for a repeated square pulse is larger than C_n for a repeated triangular pulse. It is apparent therefore that, for application in a broad band noise generator, a repeated square pulse is more desirable than a repeated triangular pulse.

As it is impossible to develop a pulse generator with zero rise time, the actual pulse shape that can be generated is closely approximated by a repeated symmetrical trapezoidal wave, as shown in Fig. 5.



This wave shape has a spectral distribution of the form $(\text{Sin } x/x)\ (\text{Sin } y/y)$ where $x = n\pi t_1/T$ and $y = n\pi(t_1 + t_o/T)$. A plot of this function in x and y is shown in Fig. 6.

Figures 2, 4 and 6 show that there are frequencies at which $C_n = 0$. These occur at all points where $(nt_o)/T$ is a whole number, that is, at π, 2π 3π, . . . $n\pi$, radians. Figure 7 shows an expanded view of a typical frequency at which $C_n = 0$.

If the center frequency, f_o, of the receiver is such that it falls directly on a node, noise is always present, since there is always a finite bandwidth in a receiver. The amount of noise present is dependent upon the actual bandwidth in question.

On the basis of this analysis, a reliable, relatively inexpensive pulse generator was developed, the prime design goal being the fastest rise time possible with a low overall cost and a minimum of components. A block diagram of the generator is shown in Fig. 8.

Figure 9 shows the complete schematic of the ignition noise simulator. The variable prf clock circuit utilizes a 2N491 unijunction transistor. The prf of the clock is determined by the RC network of $R_1 + R_2$ and C_1. The prf is adjustable from 100 to 1,000 cps to match various engine speeds by adjusting R_2. By using low temperature coefficient components, the clock is quite stable over a wide temperature range.

The blocking oscillator circuit is of conventional design, the choice of pulse transformer and transistor being dictated by the pulse width and rise time desired.

An emitter follower output is desirable for low output impedance and high impedance transfer

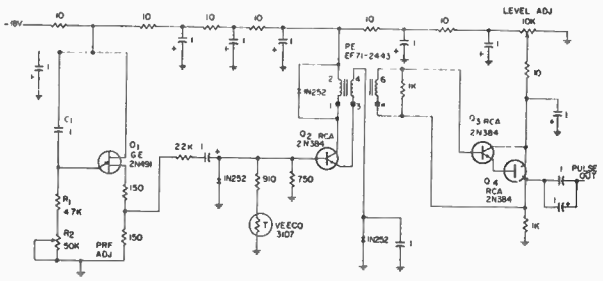


FIG. 9—Circuit of ignition noise simulator.

into the collector circuit of the blocking oscillator. Because a standard emitter follower circuit would tend to reduce, or at best match, the rise time of the pulse from the blocking oscillator, the tertiary of the pulse transformer is connected to the base and emitter of the equivalent output transistor. This creates an emitter follower switch. This switch improves the rise time by approximately 20 per cent. By connecting Q_3 and Q_4 in a conventional "Super Beta" compound connection, it is possible to drive into a low impedance with little or no loading on the blocking oscillator.

Using a prf of 250cps, pulse width of 1.5 micro seconds, rise time of 55 nanoseconds and driving into a 25-ohm load, the noise level achieved is approximately 50 micro-volts at 150 mc in a 100-kc bandwidth.

The generator material cost is less than $30.00. It has a power drain of less than 100 mw, and is stable over a temperature range of −20C to +55C.

Portable Pulse Generator

IN MANY INSTANCES there arises a need for a pulse generator for calibration of certain electronic devices. One such need is for calibrating a scaler such as is used in nuclear counting systems. Most scalers have built-in test generators which develop pulses at line frequency. This will not satisfy the needs of the technician when trouble develops at higher counting rates. It was with this requirement in mind that the following pulser was constructed.

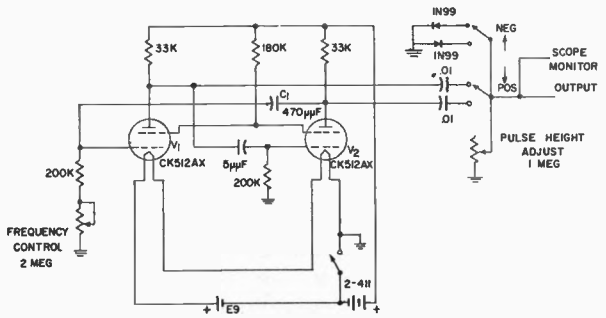
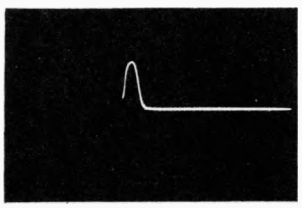


FIG. 1—Portable generator provides pulses up to 900,000 per minute.

The circuit shown in Fig. 1 is a basic multivibrator employing two subminiature tetrodes. Pulse repetition is variable from 180,000 to 900,000 per minute. Pulse size may be varied from 0 to 4 volts, positive or negative, and pulse duration is 10 microseconds. The frequency of the multivibrator is controlled by a 2-megohm potentiometer. This varies the discharge time of C_1, the feedback capacitor from the plate of V_2. The two diodes in the output are pulse shaping devices, passing positive overshoot during negative output and reversing the situation with positive output. A one-meghom control is used across the output to vary the pulse height. This is advantageous in working with discriminator circuits.

Photos of both positive and negative outputs are shown in Fig. 2 and 3. These photos were taken



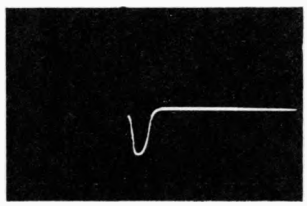


FIG. 2—Positive output. FIG. 3—Negative output. Vertical setting at 2 volts per cm and horizontal at 10 microsec per cm.

from a Tektronics 545 oscilloscope. Power requirements for the units are 3 ma at 30 volts plate supply, and 40 ma at 1.4 volts for the filament supply. Under these conditions reasonably long battery life can be expected.

The entire unit is housed in an aluminum box 6 x 4 x 3 inches with room to spare. The cost of the unit is under $20 and it can be constructed in two hours. This has proved to be a most valuable piece of test equipment.

Transistorized Linear Staircase Generator

IN COMPUTER or display electronics there is often a need for a long duration (> .5 min), many (>10) step, staircase generator.

Counter and ladder-adder arrangements find limits in this range in uniformity of step size and

in dc stability of step level.

Utilizing a high (1000) gain, high Z_{in} (>1 meg. ohm) operational amplifier, and charging C_2 with a reset pulse at A, we were able to generate a 600-step, 5-volt, 5-minute staircase with less than .5 mv difference in step size and less than one per-cent slope in step level.

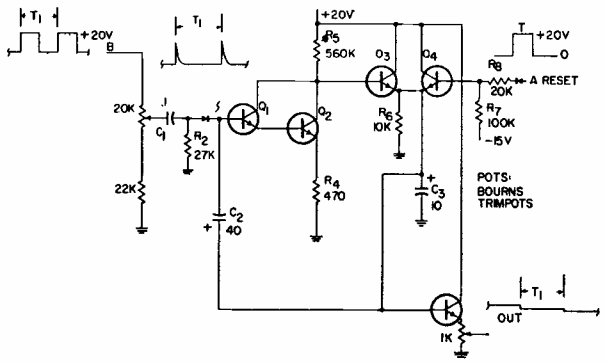
A reset pulse at A will charge C_3 and C_2 to a level corresponding to the duration and amplitude of the reset pulse.

The output will remain stable in that the discharge time for C_2 is 40 sec. While any incoming pulse at B is differentiated in C_1R_2 and the positive pulse fed to discharge C_2 and base of Q_1. For incoming pulse deviation, discharge time for C_2 is 40 mil sec, therefore any incoming positive pulse will be integrated for its duration. By feeding a "comb" in at B, each spike will cause a step in the output, whose amplitude is a function of spike amplitude and duration.

The 20K pot at B serves as a step size control while the 1000-ohm pot at the output serves to adjust output level.

The TI 495 commercial silicon transistors were selected for high β (100). The IN457A diodes were selected for low leakage (.025 μa).

The −15v and 100K-ohm resistor at the base of Q_4 merely serve to handle I_{co} in reset device.

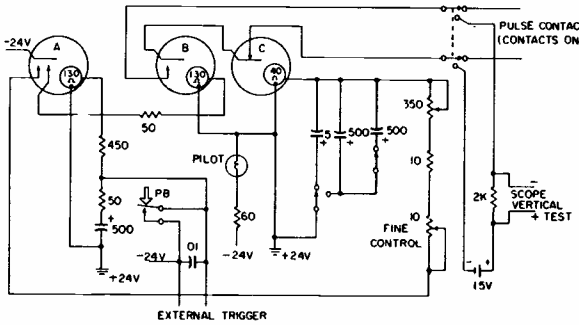


High-gain amplifier circuit used in linear staircase generator.

Single Shot Square Wave Pulse Generator

FREQUENTLY there occurs the need for a pulse generator capable of single shot operation in the micro or millisecond range capable of large current and voltage dissipation. Such a circuit could be done with a multivibrator transistor circuit or such a circuit driving a relay. Transistors alone will provide adequate pulse range but no actual open circuit exists at any time, furthermore, inductive circuits may damage such units. When transistors drive a relay the lower pulse range is limited to the operate time of the relay.

The circuit shown avoids both these limitations to a large degree by taking the difference of operate times between two relays. Mercury wetted contact relays were chosen for their lack of electrical contact bounce, stability and current capabilities.



Circuit produces pulses from 10 microsec to 200 msec in length.

Relay A, operated by means of a pushbutton, in turn closes the circuit to relay B and C. Relay B closes the circuit path through B and C, however, C operates at a later time, thereby opening the circuit path. This time delay is determined by the values of capacitance and the 350-ohm potentiometer. This circuit is capable of excellent pulse accuracy being ±1 per cent from 100 microseconds up. Below 100 microseconds ±6 per cent was observed, however it is believed this could be improved by better quality components.

A One Transistor Saw-tooth Generator

OPERATION of this generator relies upon transistor delay for resetting of the circuit.

Consider the instant when the transistor begins conducting. Point B is at $-v$ volts, it then rises positively until the transistor saturates. The silicon diode D_2 is reversed during this period and point A charges towards ground at a rate determined by CR_2. Point A will continue going positive so that D_1 conducts and reverse-biases the transistor until it falls out of saturation. The time taken for the transistor to again become forward-biased and for the collector current to rise to: $(V-v)/R_3$, allows adequate time for point B (and therefore A) to fall to $-v$ volts, thus completing the cycle.

The design considerations are as follows: For the transistor to saturate: $R_1 < \beta R_3$.

For the transistor to turn off: $R_2 < R_1$.

B must rise more rapidly than A. The circuit at B must discharge capacitor C more quickly than the transistor turns on.

The approximate charge time of A is:

$$t_r = \frac{C \cdot v \cdot R_2}{V+v/2}$$

The approximate discharge time of A and B is:

$$t_f = \frac{C \cdot v}{\frac{V-v/2}{R_3} - \frac{V+v/2}{R_2}}$$

Consider the case where $V = 2v$, $R_1 = 50R_3$, $R_2 = 25R_3$.
then, $t_r = CR_2/3$; $t_f = CR_2/24$.

The formula relating the collector current I_c and the base current I_b during turn-on, with a transistor of cut-off frequency $f\alpha$ is:

$$I_c = I_b\,(1 - e^{-\omega t})$$

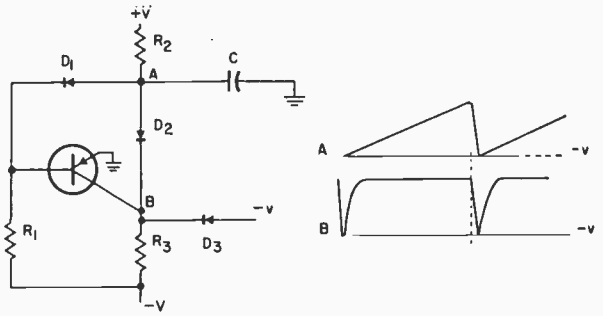
Making the asumption that the delay, before I_c exceeds $(V\text{-}v)/R_3$ approximates to the turn-on time, the following conditions must be met:

$1.6/\omega < t_r$ (neglecting collector and stray capacitance)

$2.3/\omega > t_f$

i.e. $0.8/CR_2 < f\alpha < 8\,8/CR_2$

The linearity of the waveform may be improved by replacing R_2 with a current generator or by making V/v large. A higher current gain allows the circuit to be designed for a wider range of frequency. The latter may also be attained by strapping a suitable tunnel diode between the base and emitter.



Single-transistor generator employs germanium diodes at D_1 and D_3, and a silicon type at D_2. Waveforms shown occur at points A and B.

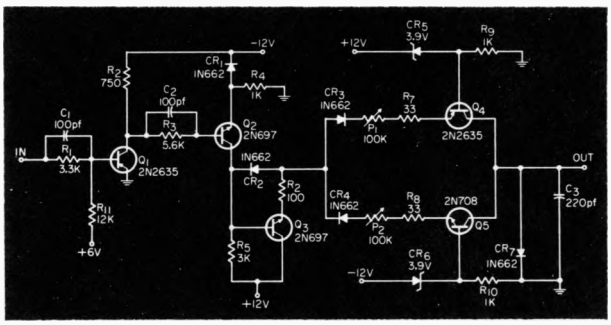
The circuit may be synchronized by applying a positive pulse to the base of the transistor.

Good results have been obtained using a 4-mc germanium alloy-junction transistor. The transistor cut-off frequency may be effectively degenerated by connecting a capacitor between base and ground.

Positive or Negative Slope Generator

THIS CIRCUIT GENERATES linear ramps, either negative or positive, by switching on and off two current sources charging a capacitor.

A negative gate into the base of Q_1 turns on Q_1, which turns on Q_2, and the emitter of Q_3 therefore sits at -12 v, thus turning on Q_5 and turning off Q_4. The constant current furnished by Q_5 will charge C_3 in the negative direction until clamped by the base-collector junction of Q_5. When Q_2 turns off, the emitter of Q_3 will be at about $+12$ v. Q_4 turns on and Q_5 turns off. The capacitor charges in the positive direction until clamped by the base-collector junction of Q_4. The purpose of Q_3 is to present an equal



Positive or negative slope geuerator.

low impedance either at $+12$ v or at -12 v to each of the current sources.

Wide-Range Voltage-Controlled Pulse Generator

WITH A CHANGE in input of only 0.5 v, the pulse generator in Fig. 1 will change frequency by a factor of more than 1 to 10,000,000.

The frequency is determined by the time it takes the charge on capacitor C_1 to leak off through transistor Q_1, which has a collector cutoff current in the order of milli microamperes. When the potential on C_1 approaches ground, it triggers Schmitt trigger Q_3, Q_4 through the action of buffer stage Q_2. Q_3 becomes non-conducting and recharges C_1 through diode CR_1 and resistor R_2.

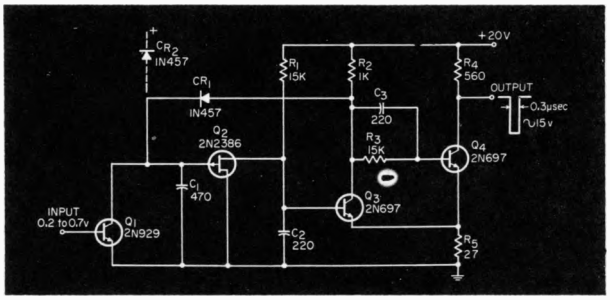


Fig. 1. Frequency of voltage-controlled pulse geuerator is determined by discharge time of C_1.

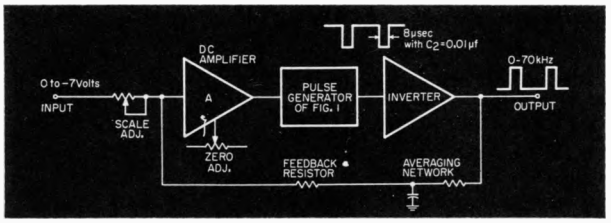


Fig. 2. Linear voltage-controlled frequency circuit.

Field-effect transistor Q_2 is cut off again, but lag network R_1, C_2 delays the resetting of the Schmitt trigger until C_1

is sufficiently charged. After reset, the collector potential of Q_3 drops down to its previous level and back-biases CR_1.

Sufficient hysteresis and regenerative action is built into the Schmitt trigger and Q_4 acts also as an output amplifier.

The output pulse is about 1/3 μsec wide with rise and fall times in the order of 20 nsec, except in the megaHertz range where they are 50-100 nsec.

The low-frequency end can be extended below 0.05 pps by adding back biased diode CR_2. Leakage through CR_1 and Q_2 to ground is balanced and compensated for by seepage through CR_2 from the power supply. Resistance through CR_1 and Q_2 to ground at room temperature is in the order of 10 gigaohms. When Q_2 clamps C_2 to ground it acts as a "source follower."

The output frequency increases by a decade for every 60-mv input increment. A linear function can be obtained by using feedback as shown in Fig. 2, assuming that the output of an averaging network varies linearly with frequency when pulse width is constant.

For example, with amplifier A in Fig. 2 consisting of a single transistor and the time constant of the averaging network being 1 msec, a linear response within 350 Hz was obtained from 0 to 70 kHz. This may be improved considerably by making amplifier A a high-gain amplifier.

MOS FETs Give Long Time-Constant Ramps

MANY TIMES the need arises for a very slow rate-of-rise linear ramp generator (less than 0.1 v/sec). Conventional transistor ramp generators require a very large integrating capacitor for slowly rising ramps, since the capacitor charging current must be large to minimize the loading effect and leakage current of the pick-off transistor.

The metal-oxide-silicon field-effect transistor, with a typical leakage resistance of 10^{13} ohms, virtually eliminates the effect of loading and leakage on the integrating capacitor when it is used as the pick-off device. This permits a drastic reduction in the value of capacitor charging current and thus a reduction in the value of integrating capacitor.

A source follower can be constructed using a MOS FET in which the source voltage will be typically 5 to 6 v greater than the gate voltage. Moreover the potential between the source and gate will remain almost constant for a wide range of drain-to-source voltage. This is true providing the drain current I_d is held constant (see Fig. 1). It is this

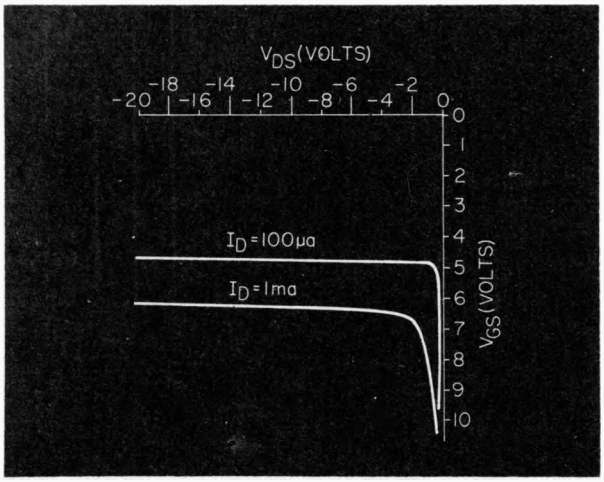


Fig. 1. Typical characteristics for MOS FET type 1004.

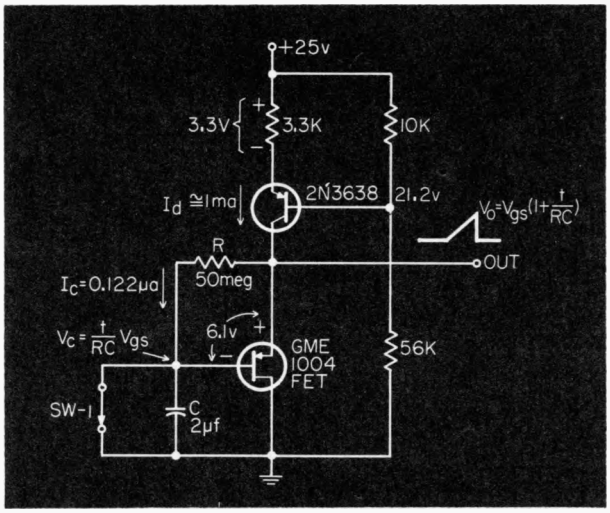
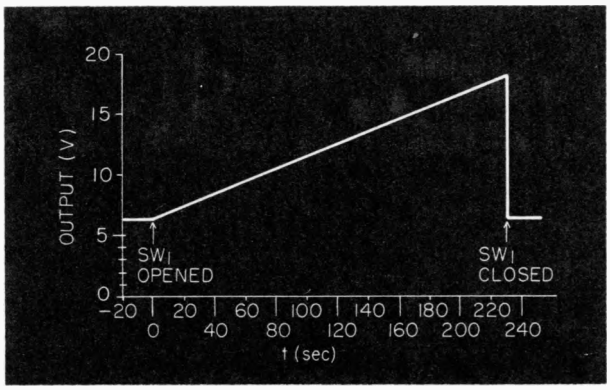


Fig. 2. Ramp generator circuit.

Fig. 3. Ramp output waveform.



property combined with the high input resistance which makes possible a simple ramp generator such as the one in Fig. 2.

In the circuit, when switch 1 is opened, the 2-μf capacitor starts to charge. The capacitor charging current is determined by the current through the 50-meg resistor. The value of this current is $I_c = V_{gs}/R = 0.122\ 10^{-6}$ amp. V_{gs} is 6.1 v for this particular FET when the drain current is held constant at 1 ma.

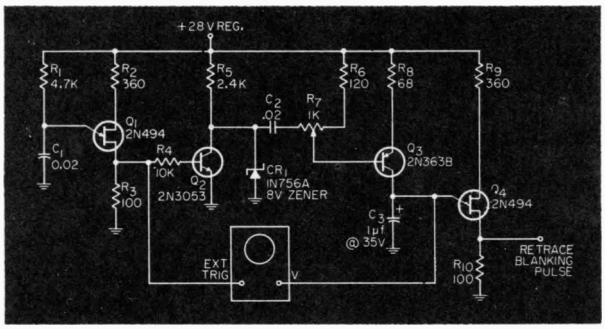
The source will follow the gate voltage as the capacitor charges, but the source-to-gate voltage will remain a constant 6.1 v. Therefore the capacitor charging current will remain constant. The result is a very linear ramp function with better than 1-percent linearity for an output of 6.1 to 18 v and a rate of rise of 0.061 v/sec (see Fig. 3).

Ramp functions of much longer durations can be generated using larger values of R and C; however, care must be taken to select a capacitor with very low leakage.

Low-Cost UJT Raster Generator

THIS CIRCUIT ANSWERED the need for a simple, low-cost, stable raster generator for use in a breadboard transistorized flying-spot scanner. It could be adapted for similar use in closed-circuit television cameras and monitors.

Unijunction transistor Q_1 is a relaxation oscillator at approximately 10 kHz, the frequency chosen as the horizontal



Unijunction transistor serves as relaxation oscillatnr at horizontal sweep frequency.

sweep rate. Positive pulses at base 1 of the UJT serve two purposes: they are used as the sync pulses for horizontal sweep and as the drive to the vertical waveform generating circuitry.

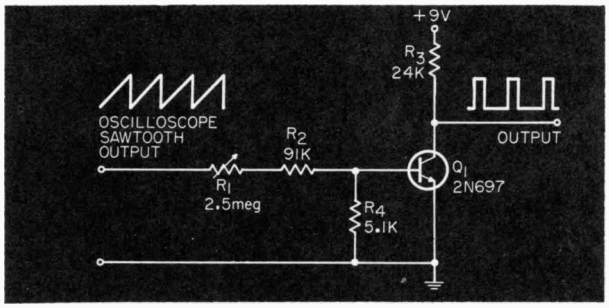
The pulses are amplified by Q_2, which operates into saturation, and clamped by CR_1 to 8 v. Thus, uniformity of pulse shape is assured. They are then ac-coupled into Q_3, which serves as a source of constant-current pulses for a UJT staircase generator stage. The staircase waveform across capacitor C_3 is applied to the vertical input of the scope and the sweep rate is adjusted so that each step on the waveform is slightly longer than one sweep of the trace. Potentiometer R_7 adjusts the current per pulse into Q_3 and therefore the voltage per step across the capacitor.

Since the UJT fires and discharges C_3 at a voltage equal to the intrinsic standoff ratio of Q_4 times the supply voltage, adjusting R_7 effectively determines the number of steps on the staircase. Because the number of steps per cycle is the number of lines per field, and also a stable integral multiple of the pulse repetition rate of Q_1, interlaced scanning is easily and reliably achieved. Since the field retrace time is the time during which C_3 discharges through Q_4 into R_{10}, the positive pulse available across R_{10} is conveniently used for retrace blanking.

Simple Variable Width, PRR Pulse Generator

FEW COMMERCIAL pulse generators produce pulses that are sufficiently variable in width to provide a large duty cycle. The simple ancillary circuit shown here gives a wide range of control over pulse width and pulse-repetition rate while maintaining oscilloscope synchronization.

Several oscilloscopes, such as the Textronix 531, have output jacks for a high-voltage sawtooth-wave whose frequency corresponds to the sweep rate. When this circuit is attached to the output jacks, variable resistor R_1 controls the amplitude of the sawtooth wave, which is applied to the base of Q_1. When the value of R_1 is increased to allow only the peak of the sawtooth wave to supply base current to Q_1, a narrow pulse appears at the collector of Q_1. If R_1 is decreased to a minimum, Q_1 will be maintained in an on state for sufficiently long periods to approach a 100-percent duty cycle. The output pulse may be monitored by the oscilloscope and will appear in synchronization with its sweep.



Simple pulse source uses scope output.

A small module, complete with a 9-v transistor-radio type battery and R_1 can be constructed with banana plugs so that it can be plugged directly into the sawtooth output jacks. Another transistor switch or a Schmitt trigger could be built into the same module to improve waveform.

Variable-Voltage Current Sink

A SILCON planar transistor operated in the second breakdown mode, provides an excellent high-current, short-duration pulse generator. This approach is simpler and cheaper than others using devices such as SCRs or avalanche transistors.

Second breakdown in transistors can be destructive, because the emitter current is concentrated in local hot spots and will eventually melt the silicon if sustained. But carefully designed pulse generators, using this mode of operation, are reliable because the cycle is completed before thermal buildup becomes excessive.

With the components shown, this circuit gives 30-A

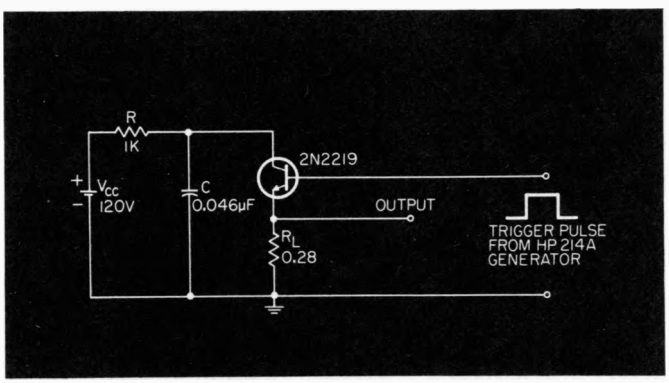


Fig. 1. Switching circuit with transistor driven into second breakdown to give 40-nsec pulses at 30-A peak.

pulses of 40-nsec duration. Generators using this circuit have been operated continuously at 130 kHz repetition rate, with no apparent deterioration in performance.

The capacitor charges to BV_{CEO} of the transistor, and the base of the transistor is pulsed with enough current to drive the transistor into second breakdown. For the transistor shown, this occurs with $I_B = 40$ mA. The capacitor voltage is monitored to detect switching. Any switching that occurs is certain to be in the second breakdown mode because normal switching would require a transistor current gain of 750 to give 30-A pulses.

During conduction in the second breakdown mode, the transistor voltage is low (approximately 10 V). Current is limited by the load resistance and the internal resistance of the transistor. Rise time of the output pulse is typically less than 10 nsecs. Pulse duration is determined by the RC time constant and by stray circuit inductance.

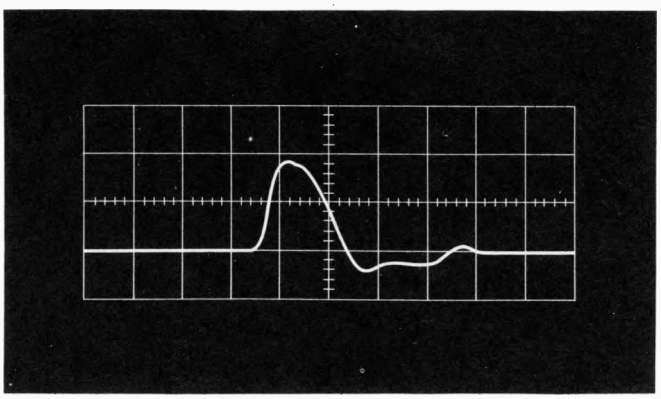


Fig. 2. Typical output pulse for the circuit shown in Fig. 1. Horizontal scale is 20 nsec/div and vertical scale is 5/div (18 A/div).

Improved Circuit for Constant-Current Source

THE CONVENTIONAL CURRENT source circuit shown in Fig. 1 has the disadvantage that there is considerable variation in output current I_o with variations in supply voltage E. This is because the zener diode has internal resistance. A solution to the problem is to add the resistor R_2 shown dotted in the figure.

Using the Thevenin equivalent circuit, the circuit can be represented as shown in Fig. 2, where R_2 and R_3 have been replaced by a generator and an equivalent emitter resistance R_E. Assuming $I_z >> I_b$ and $\alpha = 1$, adding voltages around the base-emitter loop gives

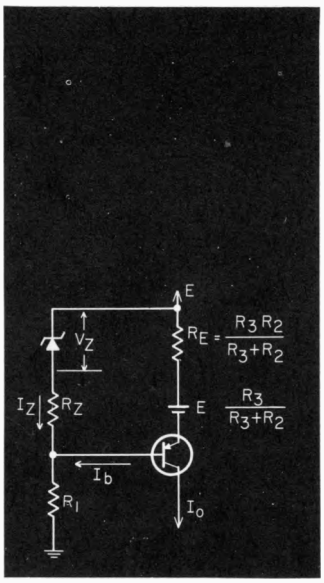


Fig. 2. To simplify the analysis, the circuit of Fig. 1 has been redrawn to show the Thevenin-equivalent generator and impedance in the emitter circuit.

$$V_z + I_z R_z - V_{BE} - \frac{E R_3}{R_3 + R_2} - I_o R_E = 0 \qquad (1)$$

Where $I_z \quad \dfrac{E - V_z}{R_z + R_1}$

Therefore

$$I_o = \frac{V_z}{R_E} + \frac{(E - V_z) R_z}{(R_z + R_1) R_E} - \frac{V_{BE}}{R_E} - \frac{E R_3}{R_E (R_3 + R_2)} \qquad (2)$$

Then, for changes in load current I_o due to supply voltage changes

$$\frac{dI_o}{dE} = \frac{R_z}{(R_z + R_1) R_E} - \frac{R_3}{(R_3 + R_2) R_E} \qquad (3)$$

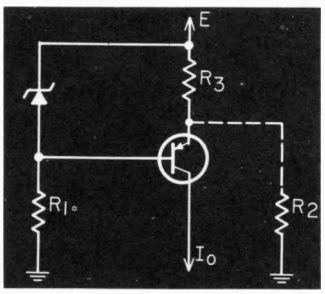


Fig. 1. The performance of this current source circuit can be improved by adding the resistor shown dotted.

From which, for no change in output current with variations in supply voltage

$$\frac{R_z}{R_z + R_1} = \frac{R_3}{R_3 + R_2} \qquad (4)$$

The optimum value for R_2 can be determined from equation 4 if R_1, R_z and R_3 are known. Also it is possible to design current sources in which the output current varies directly or inversely with variations in supply voltage in any required ratio.

Trigger Generator Sweeps from Audio-Frequency to dc

A CIRCUIT USED universally to provide a swept audio frequency is the voltage-controlled oscillator. However, when the desired frequency change is large with respect to the terminal frequency, or when the frequency is required to sweep to dc, other methods must be used. A common technique is the use of the difference signal between a fixed frequency and the output of a VCO.

The circuit shown here provides another way of approach without the complications of frequency mixing. The basic circuit element is an operational amplifier connected as an integrator. The transfer func-

tion for such an integrator is, ideally,

$$-\frac{e_o}{e_i} = \frac{t}{RC}$$

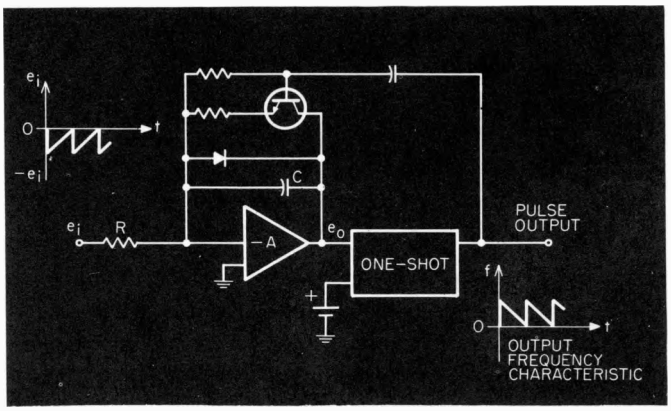
In terms of input voltage, this equation becomes

$$e_i = \frac{1}{t}(-e_o RC)$$

If the integrating capacitor, C is instantaneously discharged each time the output voltage, e_o, reaches some fixed value, the resulting circuit is a ramp generator having a frequency $(1/t)$ directly proportional to the input voltage, e_i.

When e_i is a ramp that crosses through zero volts, the generator frequency will also go to zero. The circuit shown will work only for negative e_i because of the type of capacitor discharge circuit chosen. A one-shot circuit, biased to trigger at the desired e_o, provides the discharge and the output pulse.

Many integrated-circuit operational amplifiers are ideally suited to this circuit because of their wide frequency response and because drift and gain requirements will not, as a rule, be demanding.



One-shot multivibrator, in trigger generator circuit, provides pulses which discharge capacitor in feedback circuit of operational amplifier. Output frequency is swept linearly by the input voltage.

Seesaw Circuit Gives Sine-Wave Power

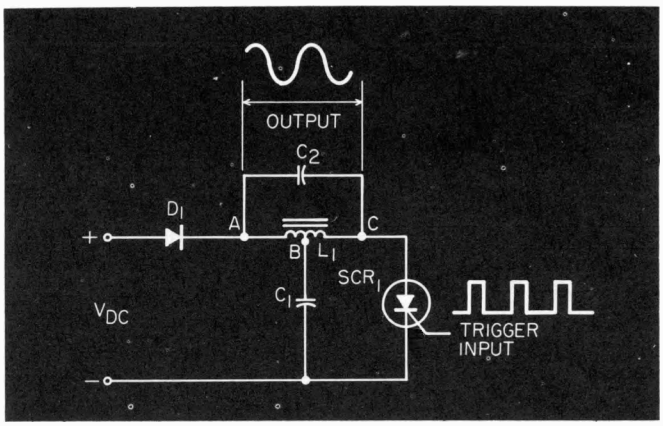
USING ONLY one active device, an SCR, this circuit provides an efficient way to generate sine-wave power. It is triggered by an external pulse generator which can be a simple multivibrator or UJT oscillator. One interesting application for the circuit is an ultrasonic generator. The circuit can be powered by 60-Hz line voltage instead of dc, to give bursts of ultrasonic power.

The operation of the circuit is analogous to a seesaw, where C_1 is the pivot and the resonant circuit L_1, C_2, is the board. The repetition frequency of the trigger pulses is chosen to coincide with the resonant frequency of L_1, C_2. The output voltage is developed across L_1. A secondary winding can be added to this inductor to match the load.

When supply voltage is applied, capacitor C_1 charges and points A, B and C approach the potential of the supply. If the SCR is triggered by an external pulse, it conducts and point C moves toward ground potential. Capacitor C_1 is made large so that current will flow out of it through the right half of L_1, without appreciably changing the the voltage at B. This current induces a voltage at point A which is higher than the supply voltage. Diode D_1 is therefore reverse-biased and the circuit is cut off from the supply voltage. The current stored in L_1 also induces a negative voltage at point C and starts charging C_2. The SCR cuts off due to the negative anode voltage, and when C_2 is fully charged, current through L_1 ceases and the potential at points C starts to move upward.

At the same time, the potential at A moves downward and when it drops below the supply voltage, current flows into the circuit to start a new cycle. The next pulse then arrives at the gate of the SCR to trigger it again.

Using this circuit, sine waves in the frequency range 1-20 KHz have been generated at powers up to 100 W. Harmonic distortion was approximately 20%, and efficiency was better than 90%.



The SCR is the only active device in this circuit. Efficiency is better than 90%.

Crystal controls rep rate of simple IC pulse generator

TO GENERATE continuous pulse trains, circuit designers generally employ circuits like blocking oscillators, or sine oscillators followed by clipping or shaping circuits. Fig. 1 shows a much simpler approach that needs only one TTL IC, a quartz crystal, and an RC network. The crystal controls the repetition rate and the RC network determines the pulse width.

But the RC network can't be chosen arbitrarily to give any required pulse width. Because of the higher switching speeds of TTL ICs, the RC network must also act as a filter to prevent high-frequency instability. Also, the resistor must limit the drive current to the crystal.

The lower limits for the values of R and C depend on the speed of the IC. The low-pass filter combination suppresses the closed-loop natural frequency of the IC. The upper

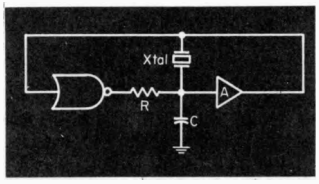


Fig. 1. Basic circuit of simple crystal-controlled pulse generator.

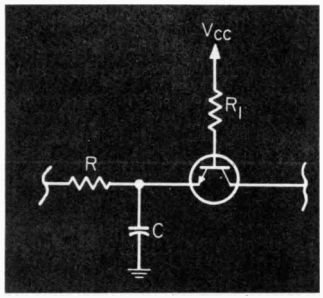


Fig. 2. Section of complete circuit shows how resistor R affects the input circuit of the IC gate.

limit of resistance for R is determined by the input circuit and threshold voltage of the IC.

For practical circuits, we replace the lumped amplifier of Fig. 1 with additional gates as shown in Fig. 3. This reduces the physical size of the circuitry, because we can use a multi-gate IC instead of separate gates and amplifiers.

Figure 2 shows the RC network and the input circuit of the second gate. To ensure that this gate switches properly, the maximum value of resistor R must satisfy the following equation:

$$R = \left(\frac{V_T}{V_{cc} - V_{be} - V_S - V_T} \right) \times R_1 \quad (1)$$

After finding an allowable value for R, we can select a suitable value for C. The value of C should be low enough to allow sufficient gain and feedback for oscillation. This sets an upper limit to the value. Provided the value is below the upper limit, C can be selected to give the required pulse width.

The practical circuit, shown in Fig. 3, uses a single Transitron TNG 3442, quad 2-input, gate. Crystal frequency is 4 MHz. In this circuit the fourth gate provides output isolation. Depending on the required output polarity, the fourth gate can either be connected as shown, or it can precede the third gate to reverse the pulse. Fig. 4 shows the output waveform for this circuit. The spare input of the first gate can be used as a stop/start switch.

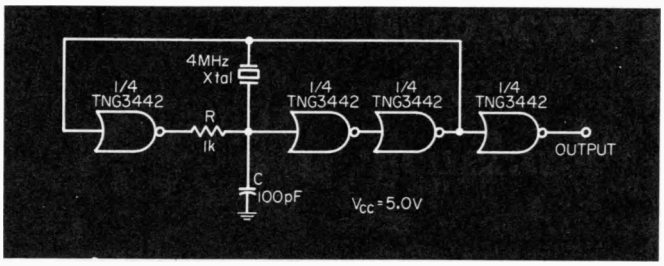


Fig. 3. Practical circuit for 4-MHz pulse generator, using quad 2-input gate. Spare input to the first gate can be used for stop/start control.

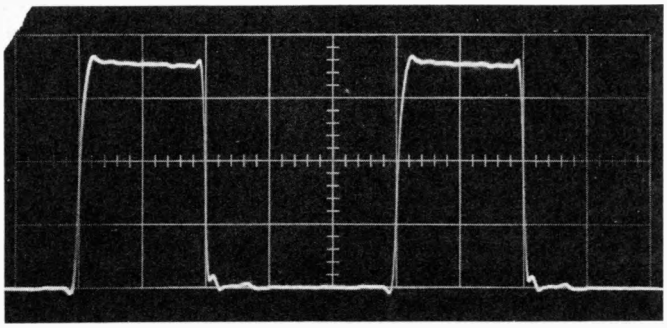


Fig. 4. Output waveform for the circuit shown in Fig. 3. Vertical scale is 1 V/cm and horizontal scale is 50 ns/cm.

With suitable component values, the basic circuit can accommodate a wide range of crystal frequencies from 10 kHz to around 10 MHz. Frequency stability depends primarily on the stability of the crystal. The circuit is insensitive to variations in crystal series impedance. Within the temperature range of the IC, the circuit shown in Fig. 3 has better than 0.02% stability.

Unijunction transistor simplifies trigger sweep generator

THIS SOLID-STATE sweep circuit delivers a linear ramp voltage whose amplitude is unaffected by variations in sweep duration. The circuit also provides positive and negative blanking pulses that are synchronized with the sawtooth output. Reliable triggering is achieved for sweep durations ranging from 2 μs to 10 s.

Sweep amplitude is almost 6 V pk-pk. This amplitude will vary slightly from circuit to circuit due to variations in the peak-point voltage of unijunction transistor Q_1. Sweep linearity is better than 1 percent (i.e. sweep voltage departs from a straight line by less than 1 percent of maximum sweep amplitude).

Maximum repetition rate is about 500 kHz, with a 7-V trigger pulse required at C_3. With suitable adjustment of the coarse-speed capacitor C_1, available sweep frequencies range from 0.1 Hz to 500 Hz.

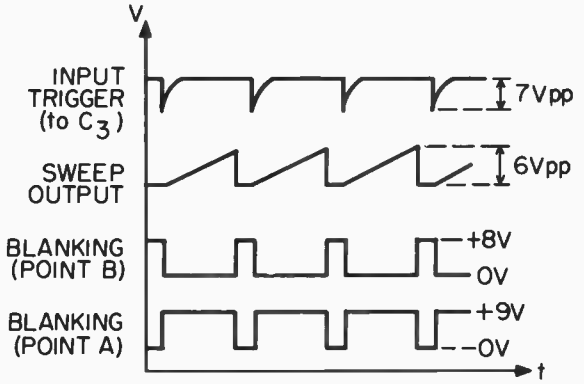


Fig. 2. Typical waveforms for the circuit of Fig. 1. The amplitude of the linear ramp output is unaffected by variations in sweep duration.

The basic sweep-generating circuit (see Fig. 1) consists of transistors Q_1 and Q_3, and unijunction transistor Q_2. At the start of a sweep cycle, Q_1 acts as a current source to charge the timing capacitor C_1 at a constant rate. Transistor Q_3 buffers the timing capacitor and provides the linear output voltage.

When the voltage across C_1 becomes equal to the peak-point voltage of Q_2, it forward biases the emitter-to-base-1 junction of Q_2. The unijunction then rapidly discharges C_1. With C_1 discharged, a new sweep cycle can be initiated.

Triggered sweep is achieved by using an R-S flip-flop (Q_4 and Q_5) in conjunction with the basic sweep circuit. The flip-flop allows a single sweep to occur for each input trigger.

When a trigger pulse is applied to C_3, transistor Q_4 turns off and C_1 is allowed to charge via Q_1. Upon completion of the sweep cycle, conduction of unijunction Q_2 causes a negative-going pulse at base-2. This resets Q_5. With Q_5 turned off, Q_4 clamps Q_1, thus preventing further sweep action until receipt of the next trigger pulse.

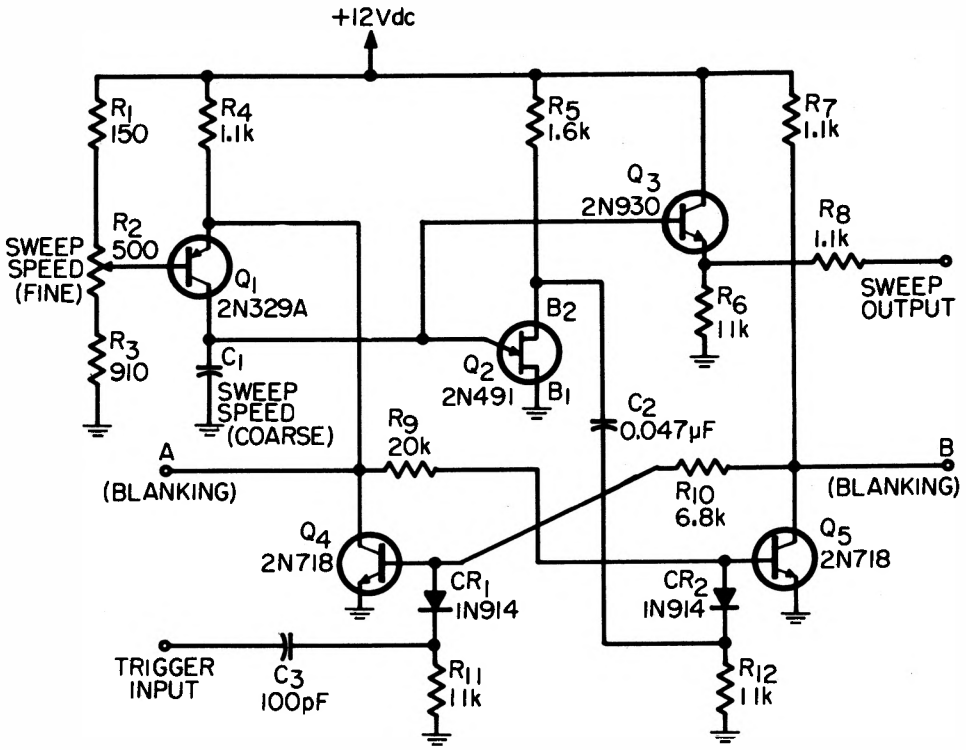


Fig. 1. Flip-flop (Q_4, Q_5) in this sweep generator allows a single sweep output for each trigger pulse. Positive and negative blanking pulses are generated at points A and B respectively.

If free-running operation is needed, point B can be grounded, thus removing the clamp provided by Q_4. Blanking for free-running operation can then be obtained from base-2 of Q_2.

Coarse sweep speed is determined by selection of timing capacitor C_1, while potentiometer R_2 provides a vernier adjustment of sweep rate. Transistor parameters aren't too critical, but Q_1 should be selected to withstand a reverse base-emitter bias of nearly 12 volts.

IC one shot generates short-duration pulses and eliminates switch noise

A PREVIOUSLY-PUBLISHED circuit ("One-Shot Multivibrator Kills Switch Bounce," *EEE*, June 1967, pp. 137-8), satisfactorily eliminates the effects of switch bounce on logic-system command signals. But the circuit has two disadvantages:

- It has an inherent 10-ms delay.
- It cannot generate noise-free pulses of less than 5-ms duration.

An improved circuit, shown in Fig. 1, overcomes the disadvantages of the earlier circuit. With the component values shown, the new circuit generates a noise-free output pulse of 1-μs duration. Rise

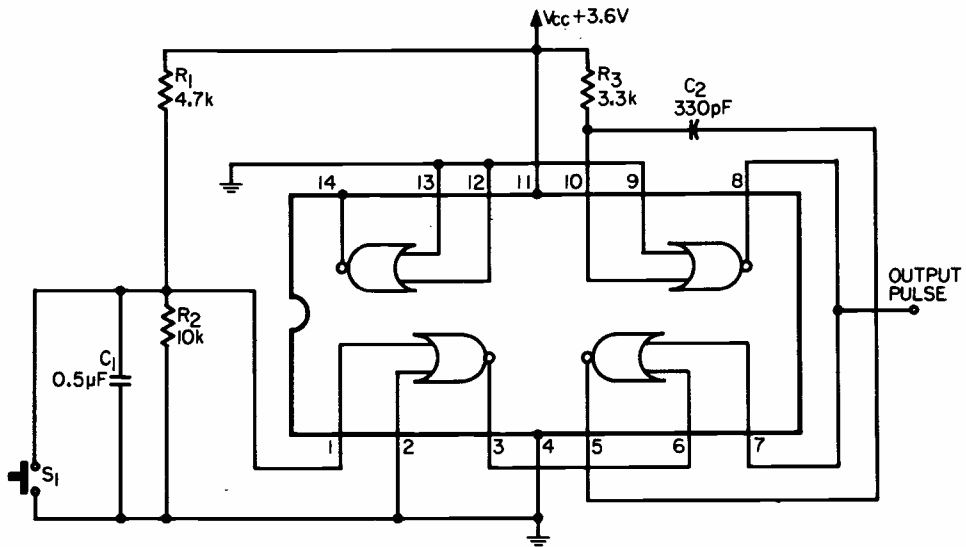


Fig. 1. Because swtich S_1 is shunted by C_1 and has one side grounded, noise generated by the switch is normally below the threshold of the IC. The circuit generates output pulses from 1 μs to 80 ms, wide depending on the value of C_2.

and fall times are around 30 ns.

The circuit is built around a single RTL IC 4-gate NOR unit. It consists of a 1-μs one-shot multivibrator driven by an inverter.

Before the switch is depressed, the inverter input (pin 1) is high, giving a low inverter output (pin 3). The one-shot output (pin 8) is normally low.

When the switch is momentarily closed, capacitor C_1 discharges, pulling the inverter output (pin 3) high. This signal then triggers the one-shot which generates a 1-μs output pulse.

Switch noise is below the noise threshold of the IC, so the one-shot sees a clean fast trigger signal. The switch is shunted by capacitor C_1 and one side of the combination is grounded. Therefore the switch noise is near ground level, instead of near V_{EE} as with the earlier circuit. The output pulse cannot be made narrower than about 0.5 μs because, during this period, switch noise will be above the threshold level of the IC.

The upper limit of output-pulse duration depends on the time constant of the RC network, C_2, R_3. Pulse widths from 1 μs to 80 ms can be obtained with capacitors ranging from 330 pF to 47 μF, with R_3 held constant. The value of R_3 cannot be increased much, above the value shown, otherwise the IC will be current starved.

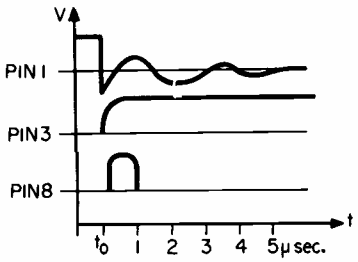


Fig. 2. Switch bounce at pin 1 has no effect on the inverted signal at pin 3. This signal then triggers the one-shot circuit to give a 1-μs output pulse at pin 8.

Trigger-diode simplifies efficient generation of sawtooths and pulses

USE OF A low-voltage regenerative trigger device in a relaxation oscillator allows the use of relatively low supply voltages. This reduces the circuit dissipation and required voltage rating for the capacitor.

The circuit can be very efficient because as much as 70 percent of the stored energy is available to the load. This contrasts with circuits using three-layer triggers and neon glow tubes, which typically deliver only 2 to 15 percent of the stored energy.

Figure 1 shows how the trigger diode, in conjunction with a low-current SCR, forms a simple relaxation oscillation. Pulse repetition frequency, obtainable with this circuit, extends from less than one pulse per minute to beyond 100 kHz. With the component values shown, operating frequency is approximately 10 kHz.

The circuit works as follows. When a supply voltage V_{AA} is applied, capacitor C_1 commences charging via R_1. When the capacitor voltage reaches the breakover voltage of the trigger diode, the diode switches and presents a low-impedance discharge path for the capacitor. The discharge current flows via the SCR gate and R_3, thus turning on the SCR.

When the voltage across the capacitor has decayed to a sufficiently low value, the saturation voltage of the SCR causes the trigger diode to cease conducting. The capacitor then continues discharging via the SCR until the SCR current falls below the holding current level. At this point, the combined current from C_1 and from V_{AA} via R_1 is insufficient to maintain conduction of the SCR. The SCR turns off and the cycle is repeated, creating a repetitive function.

From the above description, we can see that operation of the oscillator requires an SCR holding current greater than the current available from the supply through R_1. If we shunt the SCR, between gate and cathode, with a resistor R_2, we can increase the effective value of the holding current, thus allowing the use of low values for R_1. This enhances high-frequency operation of the circuit.

One disadvantage of shunting the gate to boost holding current is that this technique limits the minimum possible value for C_1, and therefore the maximum possible frequency. However, using an SCR with sensitive gate characteristics, frequencies up to 250 kHz are possible at room temperature.

Maximum operating frequency is determined by the gate sensitivity of the SCR, while the low-frequency limit is set by the switching current of the trigger diode.

The oscillator frequency can be synchronized with an external reference frequency. This is done by feeding positive synchronizing pulses directly to the gate of the trigger diode. Note that the external reference frequency must be slightly higher than the natural frequency of the circuit, otherwise synchronization won't occur.

We can calculate the natural frequency by taking the reciprocal of the sum of the calculated charge and discharge times for the capacitor. To calculate the respective charge and discharge times, we first need the following device and component characteristics:

- **SCR data**

I_{FX} — Rated blocking current (with gate-cathode resistor connected).

I_{HX} — Holding current (with gate-cathode resistor connected).

V_{FH} — Forward "on" voltage at selected holding current.

- **Trigger-diode data**

V_{SW} — Forward switching voltage.

I_{SW} — Forward switching current.

- **Capacitor data**

I_{LC} — Leakage current.

Figure 2 shows the capacitor voltage during the charging portion of the cycle. Expressed mathematically, this voltage is,

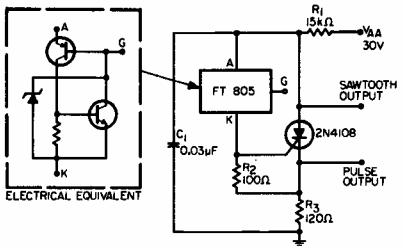


Fig. 1. Simple waveform generator for high efficiency. (Inset shows equivalent circuit of the regenerative trigger diode).

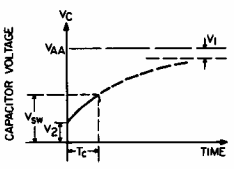


Fig. 2. Voltage waveform across capacitor C_1 while charging.

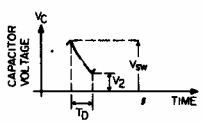


Fig. 3. Voltage waveform across capacitor during discharge.

$$V_C = (V_{AA} - V_1 - V_2)\,(1 - e^{-t/R_1C_1}) + V_2 \qquad (1)$$

This is a simple exponentially-rising voltage, starting at V_2 and aiming towards the value $V_{AA} - V_1$. Voltage V_2 is the potential across the capacitor after it has discharged. It is the sum of SCR forward drop and voltage across R_3 when the SCR anode current is equal to the holding current.

That is,

$$V_2 = V_{FH} + I_{HX} \times R_3$$

Also, in Eq. 1, voltage V_1 is the drop across charging resistor R_1 due to the combination of switching current required by the trigger diode, leakage current through the SCR, and leakage current through the capacitor. That is,

$$V_1 = R_1\,(I_{SW} + I_{FX} + I_{LC})$$

Rearranging Eq. 1 to solve for time t, we get,

$$t = R_1C_1 \times \ln\left(\frac{V_{AA} - V_1 - V_2}{V_{AA} - V_1 - v_C}\right) \qquad (2)$$

Now, the charging time is the time required for the capacitor voltage to reach the breakover voltage V_{SW} of the trigger diode. Therefore,

$$T_C = R_1C_1 \times \ln\left(\frac{V_{AA} - V_1 - V_2}{V_{AA} - V_1 - V_{SW}}\right) \qquad (3)$$

Discharge of the capacitor occurs when the capacitor potential reaches the breakover voltage of the trigger diode. Fig. 3 shows the capacitor-voltage waveform after the trigger diode has switched. This voltage is given by the equation,

$$V_C = V_{SW}\, e^{-t/R_3C_1} \qquad (4)$$

Rearranging Eq. 4 and solving for time t, we get

$$t = R_3C_1 \ln\left(\frac{V_{SW}}{v_c}\right) \qquad (5)$$

When the SCR stops conducting, the capacitor voltage has fallen to the previously defined value of V_2.

Therefore the discharge time is,

$$T_D = R_3C_1 \ln\left(\frac{V_{SW}}{V_2}\right) \qquad (6)$$

The frequency of oscillation is simply,

$$f = \frac{1}{T_C + T_D} \qquad (7)$$

This leads to the complete expression for oscillation frequency, given in Eq. 8.

$$1/f = C_1\left[R_1 \ln\left(\frac{V_{AA} - V_1 - V_2}{V_{AA} - V_1 - V_{SW}}\right) + R_3 \ln\left(\frac{V_{SW}}{V_1}\right)\right] \qquad (8)$$

Sequential bipolar multivibrator

A SINGLE circuit can replace cascaded one-shot multivibrators that are often employed to generate a delayed pulse or a pair of sequential pulses. The circuit, shown in Fig. 1, provides two sequential pulses of opposite polarities, with the duration of each pulse independently adjustable over a wide range.

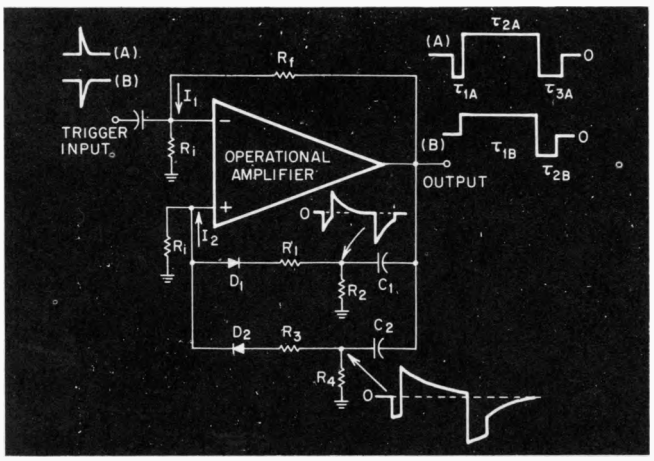
Other versions of the circuit can provide two short pulses separated by a long pulse of the opposite polarity, or allow independent triggering of the positive and negative pulses (*i.e.*, with the pulses not automatically sequential but mutually exclusive in time).

The basic circuit of Fig. 1 works as follows: Initially, I_1 and I_2 are both zero. When a positive trigger pulse is applied, the output swings negative. The negative pulse is coupled through capacitor C_1 causing D_1 to conduct. We choose $R_i < R_f$ so that, at first, I_2 is greater than I_1. Then, as C_1 charges, $|I_2|$ decreases until it is equal to $|I_1|$ and the circuit switches back to the quiescent zero state. This switching transient is coupled by the capacitance of diode D_2 and causes the output to swing positive, which turns on diode D_2. The same process is then repeated for the positive pulse.

If the first time-constant is short compared to the second, capacitor C_1 charges to the output voltage during time τ_{2A}. Therefore, when the output returns to zero, the voltage across C_1 is sufficient to turn on diode D_1. Thus a second negative pulse is generated. This pulse is longer than τ_1 because of the higher initial charge across C_1. Capacitor C_2 does not fully discharge during τ_1, and, when the output returns to zero, diode D_2 remains sufficiently back-biased to keep the circuit from switching positive.

If a negative trigger pulse is applied (situation (B) in the diagram), the sequence starts with the positive pulse. Subsequent operation is then the same as described for a positive input. The diode, of course, can be reversed to give opposite-polarity pulses.

Figure 2 shows a practical circuit that generates a 2-μs negative pulse followed by a 16-ms positive pulse. The diode across the 200-pF capacitor prevents reverse charging of the capacitor during the posi-



Design Equations for Fig. 1.

$$\frac{R_f}{R_i} = A > 1$$

$$R_1 < R_f > R_3$$

$$\tau_{1A} \simeq \left[\frac{R_2 + (R_1 + R_i)}{R_2 + R_1 + R_i}\right] C_1 \ln\left[\frac{R_f + R_i}{R_1 + R_i}\right]$$

$$\tau_{1B} = \tau_{2A} \simeq \left[\frac{R_4\,(R_3 + R_i)}{R_4 + R_3 + R_i}\right] C_2 \ln\left[\frac{R_f + R_i}{R_3 + R_i}\right]$$

and, (if $\tau_{2A} \gg \tau_{1A}$)

$$\tau_{2B} = \tau_{3A} \simeq \left[\frac{R_2\,(R_1 + R_i)}{R_2 + R_1 + R_i}\right] C_1 \ln\left[\frac{2\,(R_f + R_i)}{R_1 + R_i}\right]$$

Fig. 1. Bipolar multivibrator is similar to a one-shot, but it generates a sequential pair of pulses of opposing polarities.

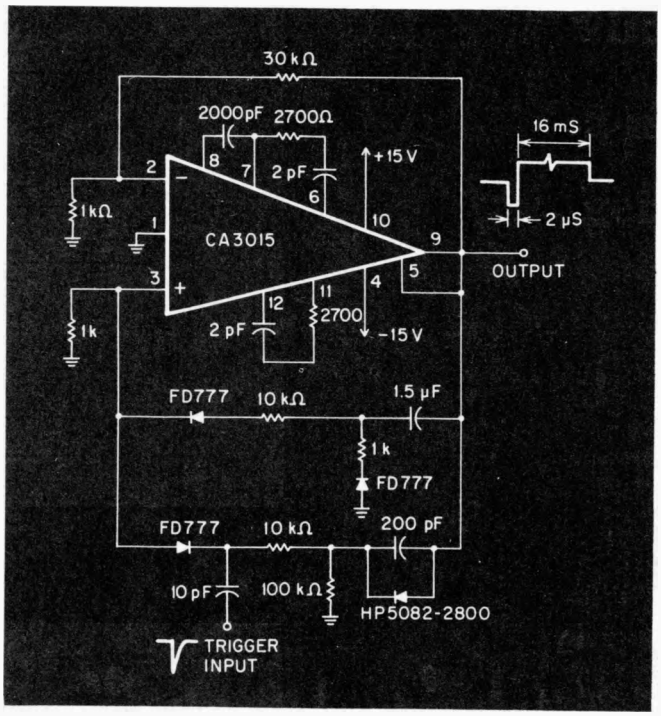


Fig. 2. This practical version of the bipolar multivibrator gives a 2-μs negative pulse and a 16 ms positive pulse.

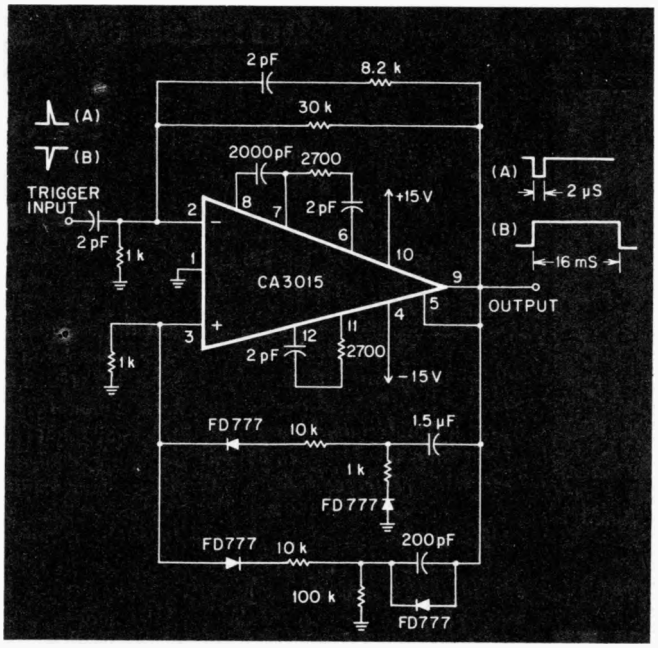


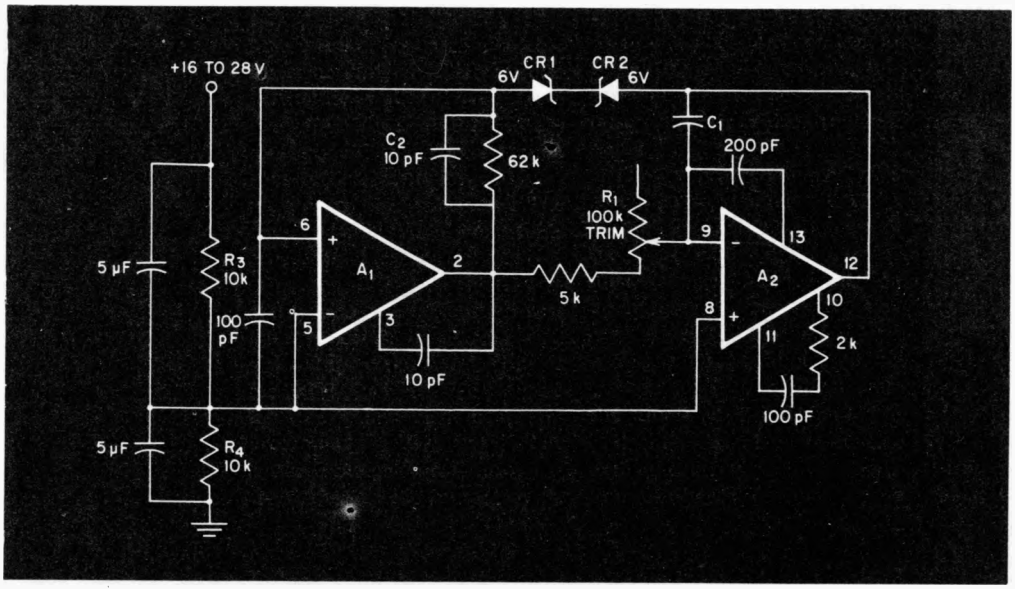
Fig. 3. The circuit can be modified, as shown here, to suppress the sequential action. Output is either a positive or a negative pulse, depending on the polarity of the input pulse.

tive portion of the cycle. Note that the triggering point has been relocated to allow negative triggering. The 10-pF coupling capacitor couples the trigger pulse and suppresses the transient during turnoff of the positive cycle. With this circuit there is no second negative pulse generated after the positive pulse.

The 1kΩ resistor, in series with the diode connected to the 1.5-μF capacitor, provides a fast discharge path for the capacitor after the positive cycle. This gives the longest possible time-constant during the positive cycle (when the diode is reverse-biased) and the shortest possible recovery time. The circuit can be triggered as often as once every 20 ms. Amplitude of the output pulse is −7 and +7 V.

Figure 3 shows how the circuit can be modified to supress the sequential action. With the trigger applied to the negative input of the operational amplifier, a positive trigger will yield a negative pulse and a negative trigger a positive pulse, with both pulse durations independently adjustable and mutually exclusive in time.

Single IC forms wide-range triangle/square-wave generator



Circuit diagram of a wide-range triangle/square-wave generator.

THE CIRCUIT in the figure takes advantage of a dual 1709 op-amp package MC1437P, with one amplifier serving as a level detecting switch to produce a square wave and the other amplifier as an integrator to produce a triangular wave of excellent linearity. The output signal is constant in amplitude to over 50 kHz, with a 5% increase over 100 kHz depending on the individual amplifier used.

The lower frequencies are limited only by the observer's

patience. Capacitor C_1 determines the frequency range available. The range is approximately 8 kHz to 120 kHz with the value of C_1 at 500 pF, 400 Hz to 10 kHz with C_1 at 0.01 μF, and 20 Hz with a 0.2-μF capacitor. A value of 250 μF will permit 1 cycle per minute. All measurments were made with B+ at 24 volts and with a 20,000-ohm load.

The switching amplifier, A_1, requires a 10-pF capacitor on pin *3* for transient suppression and 100 pF on pin *6* to prevent false triggering at high frequencies. The integrating amplifier, A_2, requires a standard compensation network of 100 pF and 2000 ohms. A 200-pF capacitor from pin *13* to pin *9* suppresses ringing. R_3 and R_4, with filter capacitors, provide minpoint-reference voltage and determine symmetry of waveform.

Assuming the output signal of A_1 is negative, resistor R_1 with a 10-pF speed-up capacitor, C_2, provides positive feedback to latch the amplifier. This voltage is applied to A through frequency-trim resistor, R_2, which allows a 20:1 variation in frequency. The integrator output then begins its positive-going ramp. When the ramp reaches 6.8 V above the reference voltage on the inverting input of A_1, zener CR_1 will conduct, overcoming the positive feedback and causing A_1 to switch to its positive state. A_2 will integrate, going negative until zener CR_2 conducts, completing the cycle. If desired a 12-volt zener may be placed on the output pin of A_1 to make the frequency and the square-wave amplitude immune to B+ variations.

Keyed multivibrator produces symmetrical ac output

SOMETIMES, THE circuit designer needs to generate a keyed tone or pulse train using a compact low-cost circuit. Conventional keyed multivibrators are suitable, but they have the disadvantage that their output contains a dc level shift which causes severe distortion in an ac-coupled load. Fig. 1 shows a typical output waveform for a conventional circuit.

The improved circuit of Fig. 2, however, has an added transistor Q_3 which removes the level shift from the output. Also, this circuit starts instantly with a full-width first pulse.

In the circuit, transistors Q_1 and Q_2 are connected as a conventional astable multivibrator. This is keyed by switching the charging voltage for Q_1's base coupling capacitor. With values shown, the multivibrator oscillates at about 3 KHz when the gate input is +4 volts, and is turned off when the gate input is below 1 volt.

When the circuit is free running, the collector of Q_2 alternates between 0.1 volt and 4.8 volts. The junction of R_7 and R_8 alternates between about 2.4 volts and 4.8 volts, producing an open-circuit output of 2.4 volts peak-to-peak.

When the gate pulse returns to less than 1 volt, Q_1 is held off and Q_2 is held on by current through R_5. Normally, of course, the junction of R_7 and R_8 would fall to 2.4 volts. But with this modified circuit, Q_3 is also turned on. This places R_{11} in parallel with R_7 so that the junction of R_7 and R_8 is pulled up to about 3.6 volts.

With the improved circuit, the positive and negative excursions of the output pulses are symmetrical about the mean level of 3.6 volts. Therefore the output can be ac coupled without introducing low-frequency level-shift distortion.

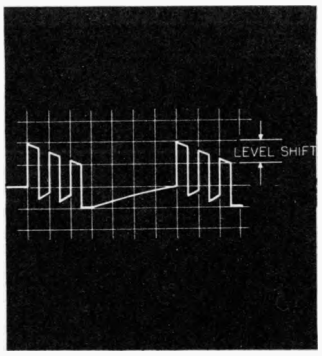


Fig. 1. Level shift at the output of conventional keyed multivibrators causes distortion when the load is ac coupled.

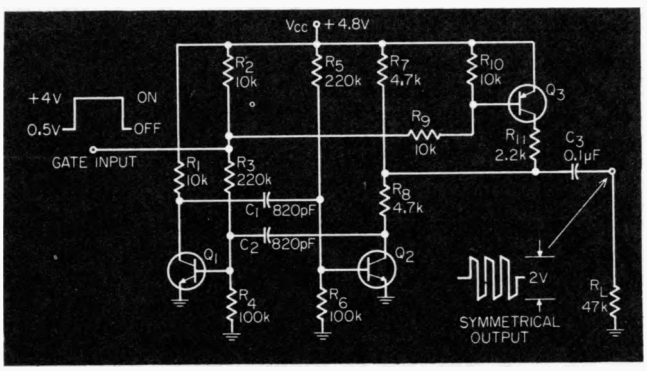
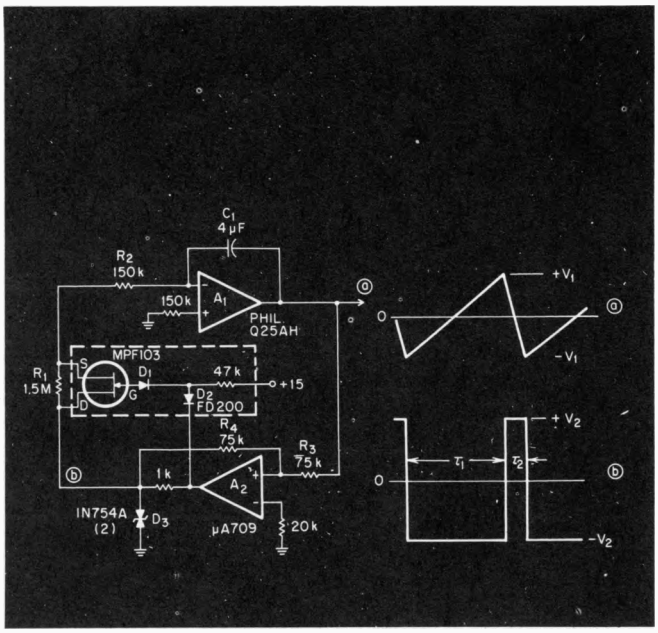


Fig. 2. This improved keyed multivibrator overcomes the level-shift problem. Added transistor Q_3 restores the output dc level to the mean value when the gate signal is low.

FET converts a triangle generator to a sawtooth generator

TWO OPERATIONAL amplifiers are often interconnected to create a triangular wave source. This circuit can be converted to a sawtooth generator by the addition of a general purpose junction FET, two diodes, and a resistor as shown within the dotted lines on the accompanying figure.

FET Q_1 is used as a switch to short the large integrating resistor which sets the long time constant. The large control signal required by the FET is derived directly from the saturating output of the Schmitt trigger, A_2. When the output of A_2 is negative, −15 volts is coupled via diodes D_1 and



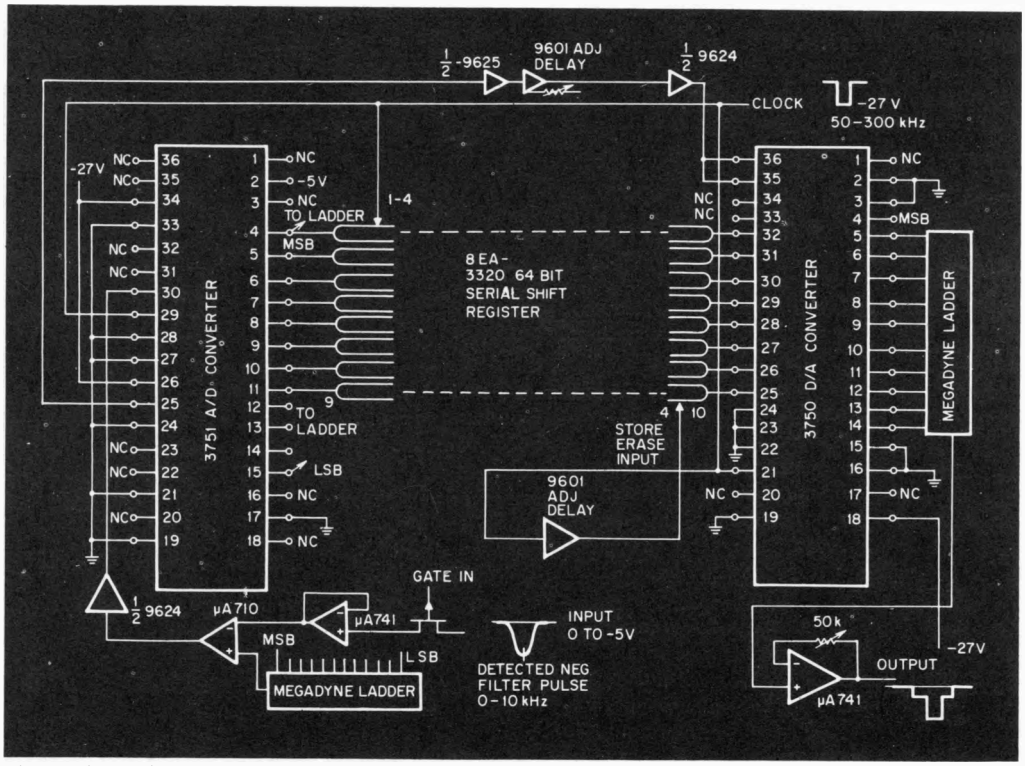
D_2 to the gate of the FET, pinching off the source-gate junction. The time constant during this part of the cycle is $(R_1 + R_2)\ C_1$. C_1 charges until the output of A_1 reaches the positive trip level of the Schmitt trigger. When this occurs, A_2 saturates positive, and D_1 and D_2 become reverse biased. The FET is turned on and shorts resistor R_1. The time constant during this part of the cycle is $(R_2 + R_{DS})\ C_1$ where R_{DS} equals on the "on" resistance of the FET.

Two diodes, a resistor and a FET convert a triangle-wave generator to a sawtooth generator with symmetrical output.

A digital boxcar generator

MOS TECHNOLOGY HAS made possible monolithic A/D and D/A converters and serial or dynamic memories. These LSI type ICs with their small size and low power, are used here in a precision digital boxcar generator. The conversion time of this circuit is in the medium to slow speed range but its accuracy is much greater than corresponding analog types.

The schematic shows a digital sampler using a Fairchild 3751 A/D, A Fairchild 3750 D/A, and a Fairchild 3320 64 bit circulating shift register. In addition to the shift register, the 3320 contains logic for loading, recirculating or erasing its information. A parallel stack of eight 3320s is used to store 64 × 8 bits in the memory mode. Any one of the 8 bit levels may be selected for readout by proper clock domain selection. In the same manner, the recirculating loop can be opened momentarily for erasure of some or all of the information.



The 3751 A/D samples the analog input continuously and feeds a digitized output to the 3320 serial memory.

The holding registers of the 3750 D/A are gated by the delayed end of conversion pulse of the 3751 A/D. By extending this delay, storage capabilities can be increased by adding additional serial registers. ■

Digital ramp generator

RAMP GENERATORS are usually designed by controlling charging rate on a timing capacitor. The capacitor has a large value and leaks charge under temperature extremes. All these difficulties are eliminated by using the digital approach of Fig. 1.

This ramp generator is based on digital-to-analog techniques. The circuit of Fig. 1 uses a single RCA COS/MOS device. The IC (CD4004T) is internally connected as a ripple counter. The respective flip-flop outputs indicate the number of binary bits loaded into the single rail input. The counter operates from dc to 2.5 MHz, therefore it is ideal for low-frequency operation. If a R-2R ladder is connected to the flip-flop outputs and a fixed-frequency square wave is fed into pin 1, a digitally stepped ramp will appear on the ladder output.

In actual operation, the symmetry of the input squarewave is immaterial. If the input frequency is F, the output ramp frequency will be $F/128$. The output impedance of the ramp generator is 51 k ±5%. $R7$ compensates for flip-flop output impedance. ■

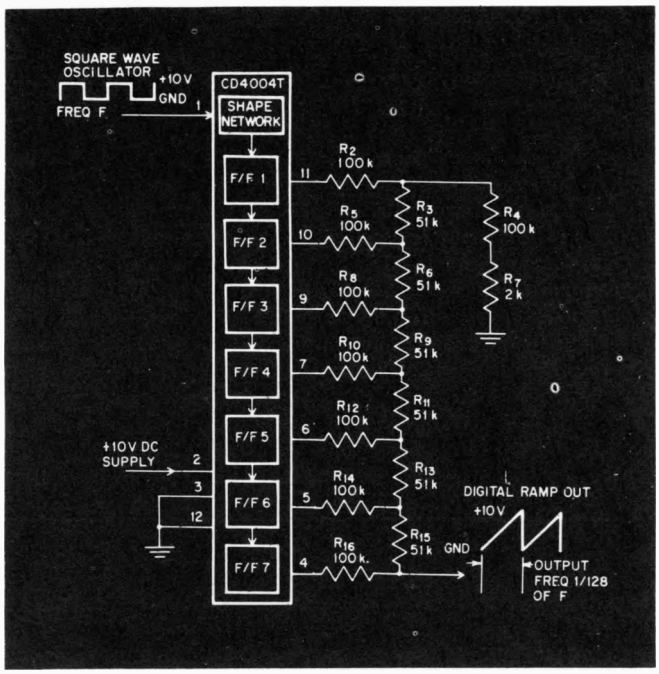


Fig. 1. This digital ramp generator eliminates the normal charging capacitor. Output frequency is 1/128 of input frequency.

Long duration variable linearity ramp generator

The circuit is an inexpensive and stable means of generating a ramp function. The shape of the ramp may be a changed to meet different requirements, from concave up through linear, to concave down. With different values of R_1 and C_1, ramp durations of 0.1 μs to several hours may be obtained.

With C_1 shorted by means of a relay, the source of buffer amplifier Q_1, is at .1.5 to 2 volts. Inverter amplifier Q_2 is biased almost off and Q_3 is conducting.

Speaking in general, when the short is removed from C_1, the voltage at the source of Q_1 rises with the charge on the capacitor and turns on Q_2. Transistor Q_3 in turn conducts less, holding the drop across R_1 constant. This is the way the current through C_1 is held constant and the capacitor charges at a linear rate.

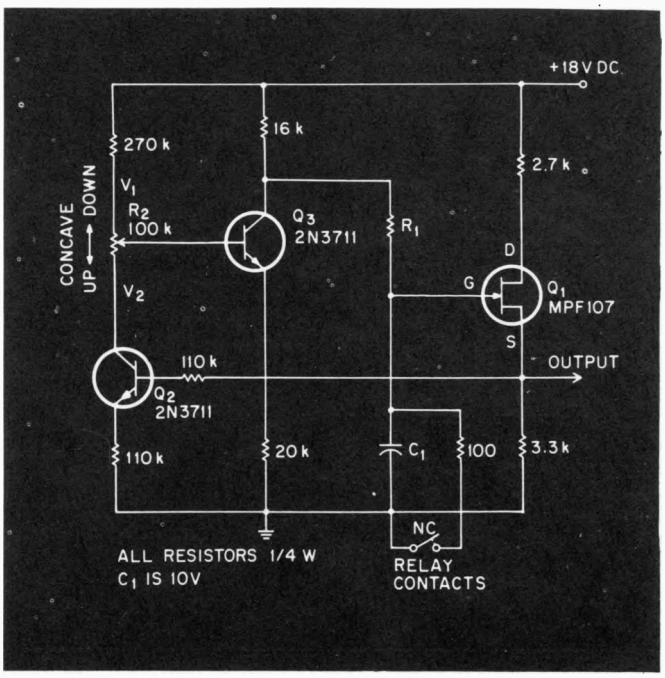
More specifically, potentiometer R_2 controls the shape of the ramp. Placing the wiper of potentiometer R_2 in the concave down position, at V_1, transistor Q_2 has little control over either Q_3 or the charge rate of C_1. At this setting the output resembles that of a simple RC circuit.

With the wiper of R_2 in the concave down position, V_2, Q_2 overcontrols Q_3 and causes an increasing charge rate for C_1 over the ramp duration, resulting in a concave up output with an initially lower slope. The linear position is simply the midpoint between V_1 and V_2.

Calibration of the device is achieved by using small increments for R_1 or C_1 and observing the output on an oscilloscope.

Once the desired linearity is set, the output is perfectly reproducible within the tolerance limits of R_1 and C_1. Increasing temperature will cause the starting point to rise slightly.

Both large value electrolytics and small value mica capacitors may be used for C_1. R_1 should be larger than 160 kΩ. The time duration of the ramp, D, may be approximated by $D = 5.9\ R_1C_1$. ■



The relay contacts shown may be replaced by a transistor to make an all solid-state variable linearity ramp generator.

Step-servo motor slew generator

THE VARIABLE UJT oscillator shown in this schematic, operates a step-servo motor in either a slow or fast mode. The motor requires a pulse generator capable of providing a train of pulses at a slow rate, a fast (slew) rate and a variable rate providing a smooth transition between the two extremes. The smooth transition is required to prevent motor stall. This circuit meets all three requirements and has a transition time of 1.5 seconds. The input is compatible with standard-digital logic levels.

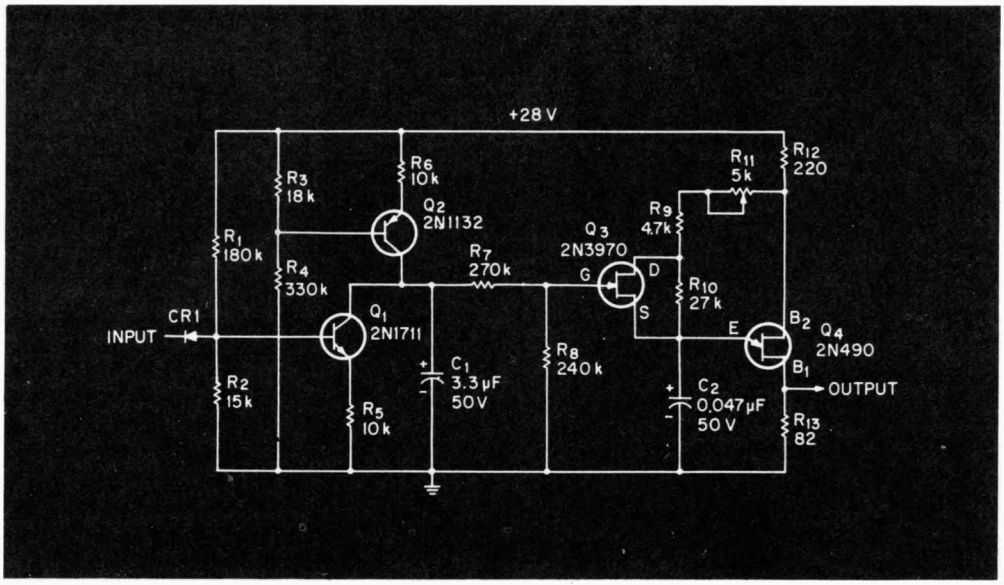
Q_1 and Q_2 are constant-current sources with Q_1 having twice the capacity of Q_2. Q . a JFET, acts as a voltage-controlled variable resistor in parallel with R_{10}. The FET's resistance varies inversely with the charge on C_1. R_{11}, R_9, C_2 and the equivalent parallel resistance of Q_3 and R_{10} determine the repetition rate of UJT oscillator Q_4.

In the steady state condition with a 1 at the input, Q_1 passes all the current generated by Q_2, C_1 is discharged and Q_3 is off. These factors cause Q_4 to generate its low frequency pulse rate (1000 pps).

When the 1 at the input is changed to 0, Q_1 cuts off. This causes Q_2 to charge C_1 at a uniform rate, which gradually reduces the source to drain resistance of Q_3. This in turn increases the pulse rate of Q_4.

With a steady state 0 at the input, Q_1 is off and Q_2 maintains the charge on C_1. Therefore, Q_3 is full on and oscillator Q_4 generates its highest rate (4400 pps).

When the "0" at the input is changed to a "1," Q_1 passes all of Q_2's current plus the discharge current of C_1. C_1 discharges at a uniform rate thus increasing the equivalent resistance of Q_3. This causes Q_4 to gradually decrease its pulse rate. ■



Wide range square-wave generator uses one IC

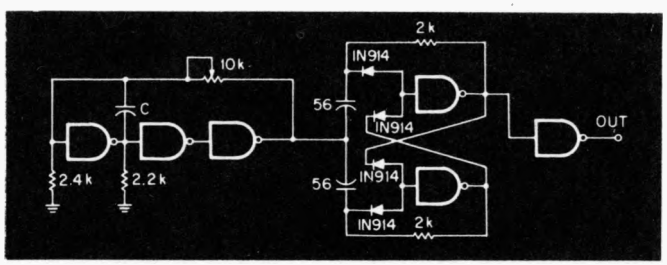
HERE IS AN INEXPENSIVE square-wave generator potentially useful for digital work. A three-inverter oscillator, a two-inverter R-S flip-flop, and an inverter used as a wave shaper-buffer, make up the circuit. The schematic shown, uses a Fairchild F9935 hex inverter (without input diodes).

The 10 kilohm potentiometer provides a frequency adjustment for the oscillator. The RS flip-flop changes state with each oscillator pulse and gives a square-wave output. The final inverter is necessary for good output buffering capability.

C μF	Freq lower	Freq upper
.01	7.4 μs	1.5 μs
.1	660 μs	54 μs
1	0.9 ms	13 ms
30	340 ms	19 ms
150	960 ms	70 ms
500	4.7 sec	330 ms

Vcc = + 5.0 V

Table of capacitance versus upper and lower frequeucy values.



A single IC is used to form a wide range, buffered, square-wave geuerator.

The upper frequency limit is about 660 kHz (C = 0.01 μF) and the lower limit is dependent on C. The chart of Fig. 2 tabulates approximate frequency ranges versus different capacitor values. ■

Simple, wideband a-m noise generator

A DIODE and an unijunction transistor provide a source of amplitude-modulated rf noise at frequencies extending from audio through uhf. The frequencies over which the noise power is useful depend on the type of diode and its bias.

The base-to-emitter diode of a 2N918 provides noise power over a broad range of frequencies from 0.5 to 500 MHz. A 2N3483 unijunction, used as a relaxation oscillator, provides a modulating frequency that depends on the choice of R_1 and C_1 in the equation

$$f = \frac{1}{R_1 C_1 \ln\left(\frac{1}{1-n}\right)}$$

where n is the intrinsic standoff ratio of the UJT.

The emitter voltage, V_e, of the UJT T_1 varies between the saturation voltage, V_s, and the peak-point voltage, V_p, which is typically 4 to 22 V. When V_e reaches the diode breakdown voltage, V_R, about 6 V for D_1, the diode begins to conduct. When V_e reaches V_p the peak diode current is

$$I_{Dp} = \frac{V_p - V_R}{R_2}$$

As shown in Fig. 2, the noise power from the diode increases monotonically with increasing bias current up to I_{D1}, which is about 20 μA in the 2N918.

By choosing R_2 to make I_{Dp} equal I_{D1}, we can vary I_D from 0 to 20 μA at the audio rate of the relaxation oscillator. The noise from the diode thus varies from minimum to maximum output, producing amplitude-modulated rf noise.

Amplitude is sufficient in the hf and vhf bands to check the operation of an a-m receiver on any channel, without bandswitching or tuning, simply by connecting the generator output to the receiver's input. ■

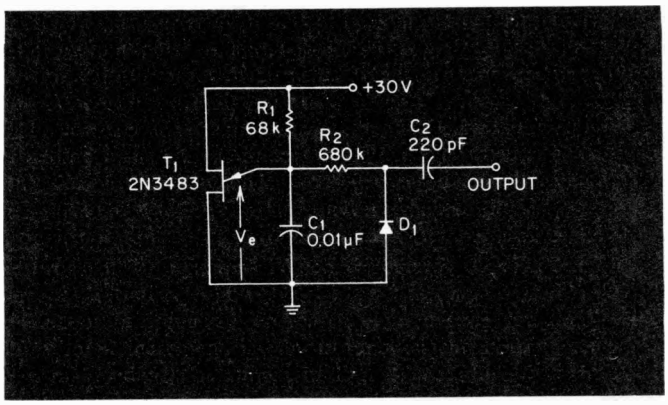


Fig. 1. This amplitude-modulated rf noise generator serves as a handy receiver tester.

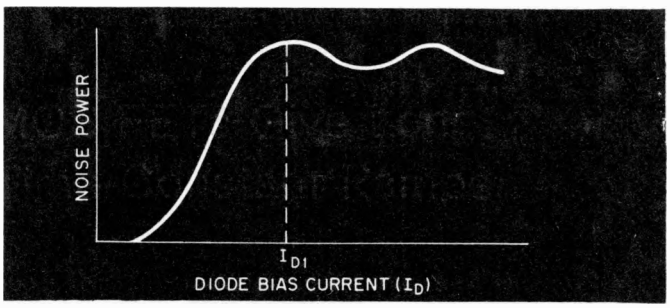


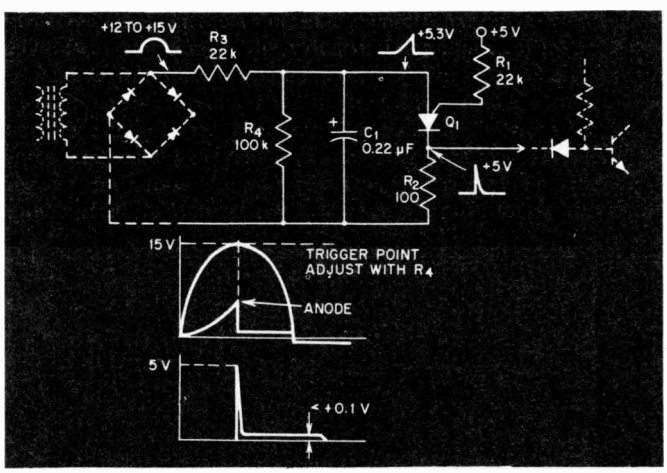
Fig. 2. Noise power is a function of diode bias current.

Low-cost 60-Hz sync

MANY CIRCUITS are available for generating a reliable pulse or square wave derived from the 60-Hz line. But most are too expensive for production runs or subject to false triggering due to line transients. The circuit here, based on GE's programmable unijunction transistor, offers complete reliability and a total cost of less than 70 cents.

In the circuit, R_1 biases the PUT gate to +5 V and sets the valley current to approximately 100 μA. The anode voltage must now exceed the gate voltage by a small amount (typically 0.3 V) before the PUT will turn on. R_3 and R_4 serve as a voltage divider with R_3 set to supply a minimum of 100 μA with approximately 3 V applied at its input. The time constant of R_3 and C_1 is about 4 ms, thus eliminating the possibility of false triggering due to transients.

The applied voltage must reach approximately +12 V before the anode voltage exceeds the gate voltage. At this time, Q_1 goes into conduction, discharging C_1 across R_2, thus generating a +5-V pulse with a rise time of about 80 ns. Q_1 continues to conduct until the anode supply drops below 2 V, then assumes a reset state until the next positive excursion of the 60-Hz line ■



This simple and inexpensive circuit provides a reliable sync pulse from the 60-Hz power line.

Section 13

CONVERTOR & INVERTER CIRCUITS

Mag-Amp Regulates Static Converter

PRACTICAL situations facing the engineer very often call for conversion of dc power from one voltage level to another or to ac with as little loss of power as possible.

Best approach to the problem is obtained by utilization of the transistorized-magnetic coupled multivibrator. The basic circuitry of this type of converter has been covered extensively. However, the converter is not inherently regulated and any change of input voltage is reflected in the output. Aircraft, missile and industrial dc sources fluctuate over a wide range. Variation of ± 20 per cent (a band of 40 per cent) is to be expected in missilery. If failure of the primary regulator occurs even wider fluctuations may be expected. Thus, a regulated converter becomes mandatory to assure continuous safe operation of the equipment.

In many cases cost and weight advantage are gained by making the primary regulator simple and designing it to more relaxed specifications which are sufficient for the bulk of the power equipment. The sensitive portion of the equipment, which in most cases forms just part of the demand, is then connected to the regulated converter with all the advantages of matching the voltages in the most desirable form possible.

Reliability and ruggedness are enhanced by util-

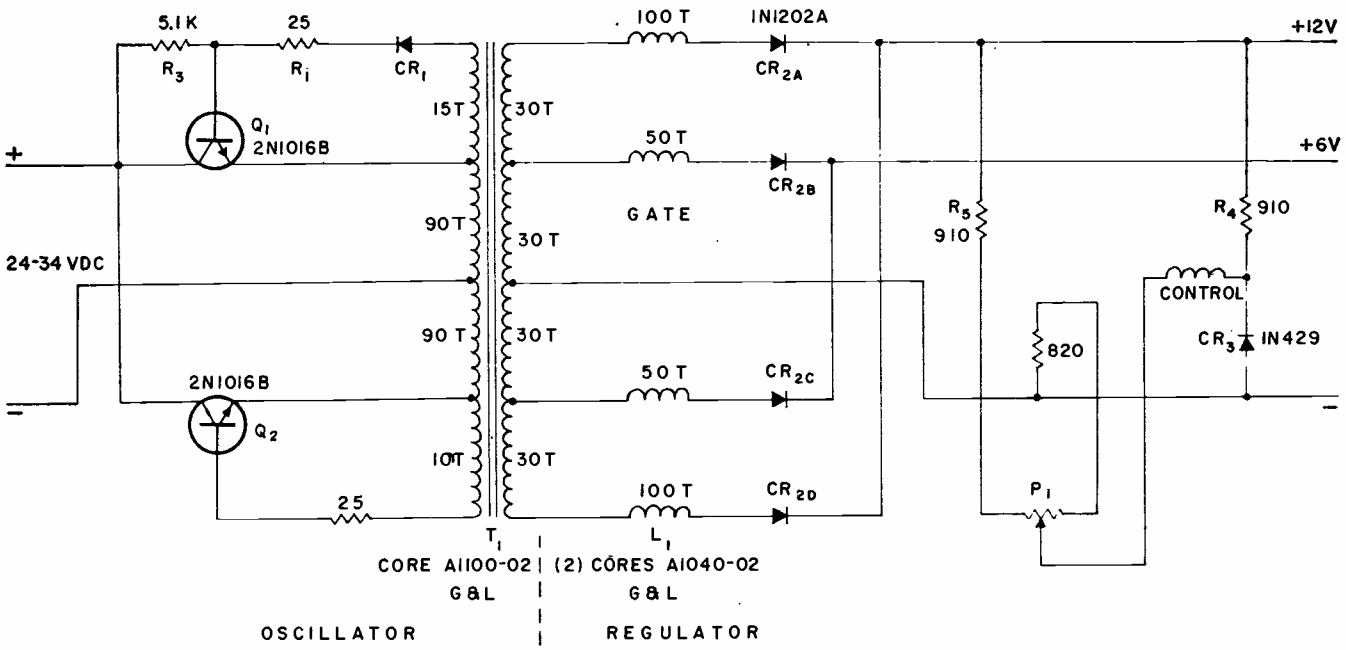


FIG. 1—Regulation of ±1 per cent is provided by mag-amp control of output of transistor oscillator.

ization of magnetic amplifiers in the regulating portion. The oscillator section is operated at a frequency which is high enough to allow the mag-amp to be small and lightweight, consistent with good efficiency. In this case 1000 cps nominal frequency is used. Fig. 1 shows the simplicity of circuitry and low number of components required for obtaining a tight regulation of ± 1 per cent, when the input changes about ± 20 per cent and the temperature goes from —28C to +71C. The circuit shown is designed for 30-watt output at 71C, under the most severe of the combinations called for in the specifications.

Transistors Q_1 and Q_2 operate in the switching mode. Diode CR_1 and resistor R_3 insure the start of oscillations under all conditions. Square wave ac output appears at the T_1 terminals. Any number of voltages, stepped up or stepped down, may now be obtained from one secondary winding provided they all have common ground. If floating ground is desired, another isolated winding is possible.

Rectifiers CR_2A-D convert ac to dc while performing the dual function of self saturation in the magnetic amplifier L_1. Reference voltage is obtained from zener diode CR_3, which forms one leg of a detecting bridge made of R_4, R_5, R_6 and P_1. For pot P_1, a Bourns Trimpot 224L-1-50 (Milliseal) allows adjustment of the outputs to the desired precise level. The circuit shown is representative of many. Negative outputs can be obtained by reversal of rectifiers $CR_{2A\text{-}D}$ and insuring the proper magnetic amplifier winding polarity.

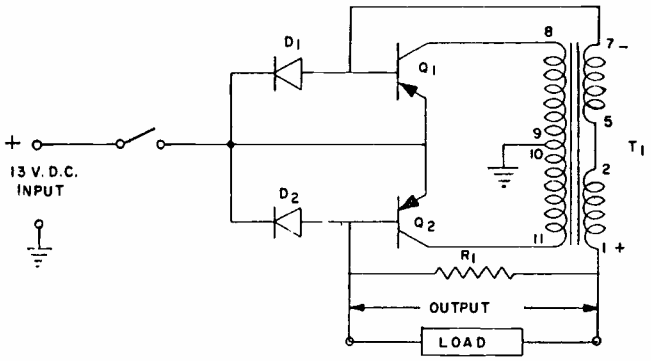
60-Cycle Inverter

THE ENGINEER has many occasions wherein an ac power supply is needed and only a 12-volt battery is available. If the frequency and waveform of this supply is not critical, the circuit shown can supply up to 100 watts output.

When power is initially switched on, a slight unbalance in transistor Q_1 and Q_2 will allow a voltage to be induced into secondary T_1. To trace this operation, assume Q_1 is slightly more conductive than Q_2. In this case, the polarity of voltage induced at terminals 7-1 of transformer T_1 will be negative. This polarity will tend to bias Q_2 in a reverse direction and also will bias Q_1 to become progressively more conductive until it is fully saturated. This process requires only a fraction of a millisecond at which time the dc supply voltage is effectively applied to terminals 8-9 of the transformer primary.

Approximately 120 volts then exists at the secondary terminals. Secondary current will flow through the base emitter junction of transistor Q_1 since it is forward biased. However, the base emitter junction of Q_2 presents a high impedance to current flow and forces current to take the shunt path afforded by diode D_2. Current flow returns to the secondary through the parallel combination of R_1 and the external load.

The primary sustains the applied voltage for a period of time which is governed by the transformer



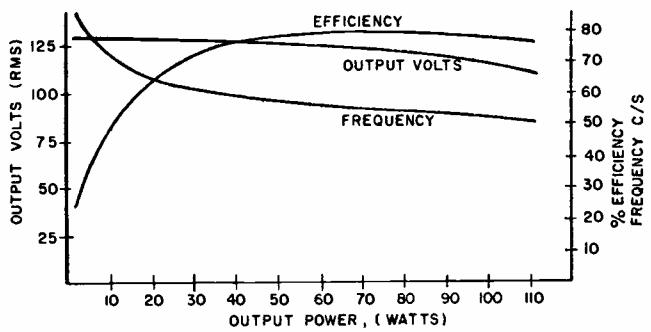
Complete circuit of simple 60-cycle inverter.

parameters. At the end of this time, the saturation flux level is reached and the primary can no longer sustain the applied voltage. The induced voltage rapidly decreases and reduces the base drive current to Q_1. The transistor is then forced to come out of saturation. The subsequent rapid decrease of current flow into the primary causes the transformer flux to decay which then induces a voltage of the opposite polarity in the secondary winding of the transformer. This polarity of voltage causes transistor Q_2 to be forward biased. In a similar manner, Q_2 proceeds to full conduction while Q_1 becomes cut off. The cycle of operation repeats in an alternating fashion yielding a square-wave output voltage whose frequency is governed by the following relation:

$$f = \frac{E_{bb} \times 10^8}{4 \times B_S \times A \times N}$$

where: E_{bb} is the dc supply voltage; N is one-half the number of primary turns of T_2; B_S is the saturation flux density in lines per square inch; and A is the effective core area in inches.

Resistor R_1 permits sufficient current flow to



Performance characteristics of simple inverter.

allow oscillation at light loads. The diode rectifiers are required to provide a shunt path for load current to flow. They also perform the function of limiting the amount of reverse voltage applied to each transistor its non-conducting half cycle.

This inverter circuit has the advantage of pro-

viding base drive current in proportion to the load power output. This causes the efficiency curve to be fairly uniform over the range of output power as shown in the performance characteristics. This variation in base drive indirectly causes a wider excursion of the frequency of oscillation than is observed in a more conventional circuit. For many applications, this variation in frequency is of little importance.

The transistors are Delco 2N442 types mounted on a finned aluminum heat sink of 80 sq. in. The thermal resistance of the sink should be better than 2.1 deg C/watt. This will permit operation in ambient temperatures up to 71 C. The diodes are Sarkes Tarzian type M500 and T_1 can be a Stancor RT204 or a Thordarson 24V62. The resistor is a 10K ohm, 1 watt.

Positive Square Wave to Negative Spike Converter

CAPACITIVE-DIFFERENTIATION systems employing a series RC circuit can be used to convert a positive square wave to a positive spike. However, if a negative spike is desired with zero volts as a starting and ending point for the negative spike, a transistor must be used with precision resistors and precision power supply.

The accompanying schematic diagram shows a positive square wave to negative spike converter with zero volts as a starting and ending point for the negative spike. Five-percent resistors may be used throughout the circuit.

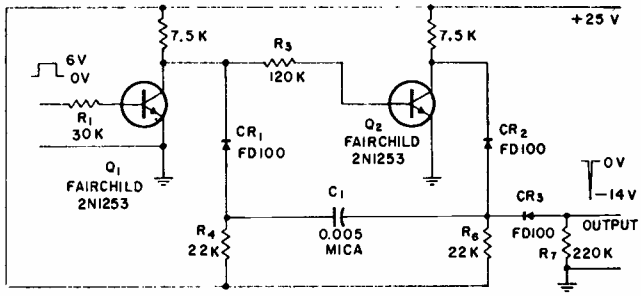
When the input voltage is zero volts, transistor Q_1 does not conduct, however transistor Q_2 does conduct. The conduction path through Q_2, CR_2, C_1 and R_4 charges capacitor C_1 to about 24 volts.

When the input voltage changes to six volts the following sequence of events takes place. Transistor Q_1 conducts and transistor Q_2 cuts off. When transistor Q_1 conducts, the junction point between CR_1 and C_1 is approximately zero volts and capacitor C_1 discharges around two paths exponentially.

The path of capacitor discharge which gives the negative voltage output spike is through CR_3, R_7, transistor Q_1 and CR_1. When the capacitor has discharged to the extent that the junction of $CR2$, CR_3 and R_6 is zero volts, diodes CR_3 ceases to conduct and the output voltage wave form is as shown.

The negative pulse width is 73.4 microseconds and the time required for capacitor charge is 406 microseconds. The maximum usable frequency for symmetrical square wave input is 1.23 kc.

At first glance it appears that the peak output voltage of the negative spike should be 24 volts. However, the peak voltage obtained with the actual circuit was 14 volts. A possible explanation is that the capacitor used had an internal series resistance which dropped some of the output voltage.



Circuit is noncritical and requires no precision power supply yet it converts square waves to negative spikes.

DC to Frequency Converter

THE CIRCUIT SHOWN in Fig. 1 converts a dc voltage

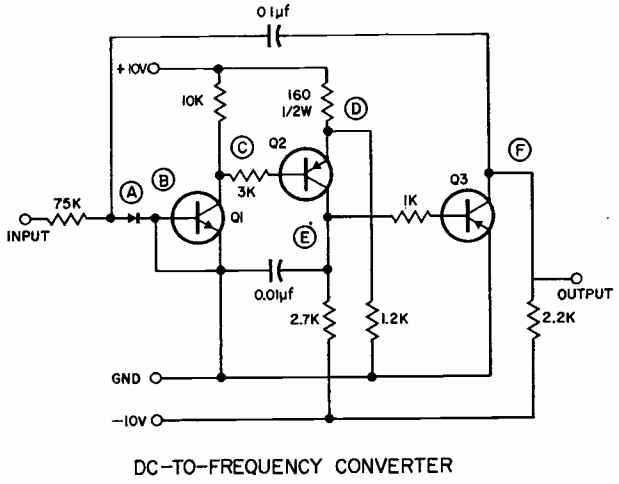


Fig. 1. DC-to-Frequency Converter.

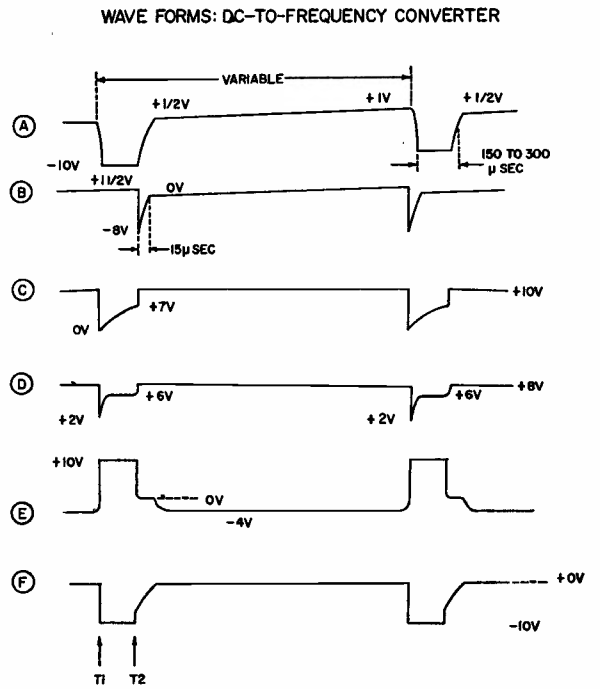


Fig. 2. Waveforms for DC-to-Frequency converter.

input to an audio frequency output. The operation of the circuit is most easily explained with reference to the waveforms shown in Fig. 2.

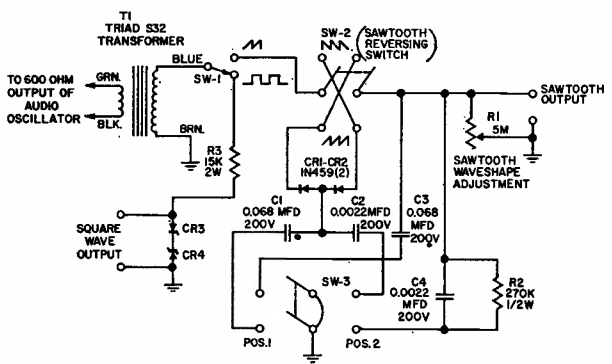
Before time t_1, transistors Q_1, and Q_2, are off and transistor Q_3, is on. At time t_1, point A reaches 1 v. Q_1 and Q_2 go into conduction and Q_3 goes off. A positive step appears at point E. The 0.01 μf capacitor charges through the 160 resistor, Q_2, and the emitter of Q_1. The 0.1 μf capacitor discharges via the 75 K and the collector resistor of Q_3. At time t_2, point C becomes more positive than point D and Q_2 turns off, while Q_3 turns on, and a negative step through the small capacitor turns off Q_1; the smaller capacitor discharges through the diode into the larger one. The large capacitor slowly charges up via the 75 K resistor, and the cycle is repeated. The period between pulses at point F is variable, depending upon the voltage at the input. The frequency response of the dc to frequency converter is given in the table.

Frequency Response Data

Input Voltage (volts)	Frequency (cps)
1.70	100
1.90	200
2.25	400
3.30	800
6.20	1600
10.0	2000

Converts Sine Waves to Sawtooth or Square Waves

THE NEED FOR THIS DESIGN arose when a square wave or sawtooth wave was required for test purposes, and it was discovered that generators giving these waveforms were very scarce and in great demand. However, sine wave audio oscillators were literally "a dime



Converter changes 50-17000 cps sine waves to sawtooth or square waves.

a dozen." The problem was to make a "little black box" using no power, only the signal itself, and come out with square or sawtooth waves. The gadget shown in this article does just that. A number are now in use.

The sawtooth wave is obtained from the sine wave by the linear charging of the capacitors. This action continues into the reverse cycle until the initiating voltage is equal to the capacitor charge voltage. At this point the output drops to zero and then repeats the cycle. The peak to peak voltage of the sawtooth is equal to the peak to peak voltage of the sine wave. The variable resistance R_1, shapes the linearity of the sawtooth upslope.

CR_3 CR_4 = Zen Diodes, IRC #69-1505 (8.0v—.1v)
SW-1 = SPDT Slide Switch
SW-2, SW-3 = DPDT Slide Switch
R_1 = Centralab—Type B-88 (5 meg. —C_2 Taper)
R_2 = 270 K —5 per cent, ½ w resistor
R_3 = 15 K —5 per cent, 2w resistor
Frequency Range
SW-3
Pos. 1— 50 to 2000 cps.
Pos. 2—1800 to 17.000 cps.

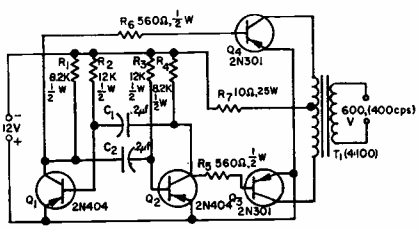
High Power, Variable Frequency Inverter

POWER OUTPUTS up to 100 watts at frequencies ranging from ¼ cps to 1 mc can be obtained with the circuit shown. The circuit is composed of two basic transistor circuits—an astable multivibrator and an inverter. The multivibrator sets the output frequency with its time constants R_2C_1 and R_3C_2, which can be made variable. If the two time constants are made equal, symmetrical output waves will be obtained.

The period of the output wave can be determined from:

$$f_o = \frac{R_3C_2 + R_2C_1}{2R_2R_3C_1C_2}$$

The complementary outputs of the multivibrator are connected to the bases of the inverter transistors. The output wave shape, determined mainly by the transformer reactances, can be made to closely approximate a sine wave.



Multivibrator sets frequency for high-power inverter.

The values shown result in a 600-v, 125-ma ac, 400-cps output. The device will operate equally well from rectified ac as from a battery. The circuit has found a use in powering electro-luminescent panels and may also be used as a frequency source to produce a high-frequency wave at a higher power level than is normally available from standard oscillators.

DC-DC Converter Diode-Starting Network

SOLID-STATE dc-dc converters that must deliver 300 to 500 W of output power at currents of 5 to 20 A have difficulty starting under full-load conditions due to insufficient feedback voltage. This difficulty increases as the ambient temperature is reduced and transistor power is decreased. Several methods of starting heavy-current dc-dc converters are available: starting resistors, extra power-transformer windings, feedback resistors for forward bias current to the power-transistor bases, extra transistors in the base circuit for increased current gain, and many more, all of which add to circuit complexity and decrease over-all converter efficiency.

In the application that led to the design described here, maximum circuit reliability was the governing factor. All the above starting methods were ruled out because of complexity and questionable reliability.

This circuit uses a diode-starting network that electrically accomplishes the equivalent of the simplest starting technique: switching the load out for starting. It operates as if a manually operated switch were placed in series with the power transformer primary to temporary disconnect the load when turning the power on. After the converter has started, the load can be applied without affecting the converter operation.

A pair of silicon power diodes connected in parallel (back-to-back) is used in series with the primary of the power transformer to perform the switching function (Fig. 1). This connection allows each diode to operate on one half of the ac cycle. The threshold voltage at the knee of the forward-current vs forward-voltage curve, as shown in Fig. 2, occurs for germanium and silicon at about 0.3 and 0.6 V, respectively, and is the minimum required voltage to cause conduction or turn-on.

This small difference of 0.3 V permits the germanium power transistors to begin oscillation while the silicon power diodes are nonconducting. Therefore, the converter is started while the load is effectively out of the circuit. Under this condition, oscillations start and gradually build up until the diode threshold voltage is exceeded. At this time, the power-transformer primary is switched in as the diodes begin to conduct.

Environmental tests were performed on a 400-Hz, 400-W, 15-A bridge-type power converter that was fully loaded. Without the diode network, the converter operated from 60° to 120°F. With the diode network, this converter started consistently from −20° to 120°F. Note that the circuit also dissipates a relatively small amount of power under normal operating conditions.

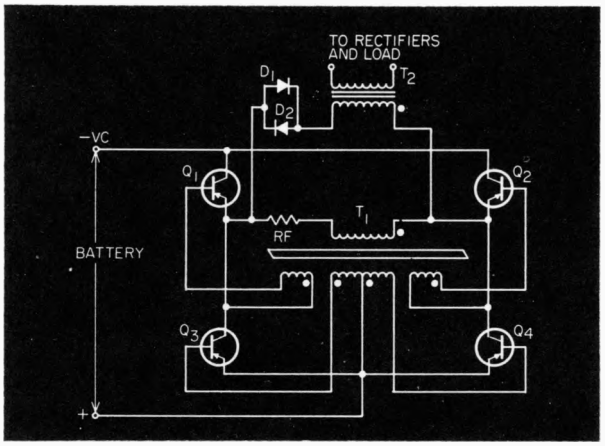


Fig. 1. Wide-temperature range starting network.

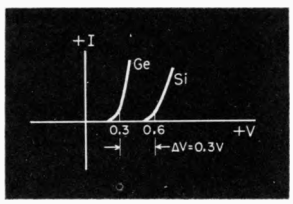


Fig. 2. Threshold voltages for germanium and silicon diodes.

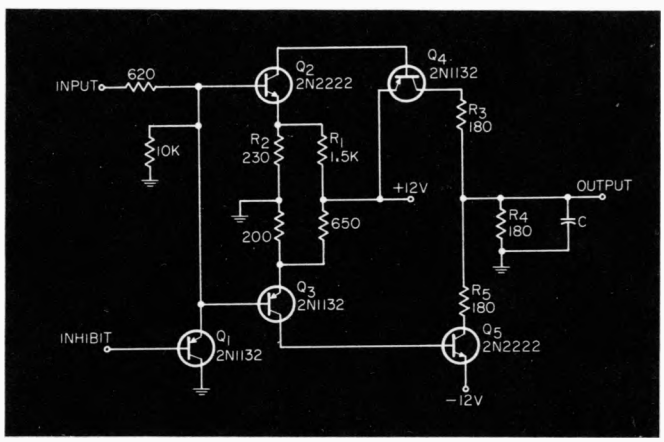
Unbalanced to Balanced Lever-Shifter

THIS LEVEL-SHIFTING circuit converts unbalanced (0 to +4 V) pulses to balanced (−6 to +6 V) pulses. In the "high" state, a 0.12 mA, 3.5 V (minimum) source at the input is needed to insure a +6 V output. In the "low" state, a 1 mA, 0.6 V (maximum) sink at the input gives a −6 V output. With the component values shown, the output impedance of the circuit is 90 ohms.

If the "inhibit" terminal is grounded, the output is held at −6 V regardless of the input voltage. In the original application for this circuit, fast rise time pulses were converted to slow rise time pulses, for transmission over long lines. Capacitor C was adjusted to give the required pulse shape.

Assuming the circuit is not inhibited, a "high" input will turn on Q_2 and hold Q_3 off. R_1 and R_2 control the current through Q_2. This current holds Q_4 in saturation and the +12 V supply appears across R_3 and R_4. Because Q_3 is not conducting, Q_5 is held off.

A "low" input gives the opposite effect; Q_2 and Q_4 are turned off, while Q_3 and Q_5 are turned on. Thus −12 V appears across R_5 and R_4.



Positive pulses at input give ±6 V balanced pulses at output. If inhibit terminal is grounded, output is held at −6 V.

The values of R_3, R_4 and R_5 may of course be changed to give different output voltages and impedances.

Linear period-to-voltage converter with low ripple

In applications where instantaneous voltages proportional to a signal frequency must be derived at rates comparable to the signal frequency, conventional averaging techniques usually prove inadequate. The circuit shown in Fig. 1 can give accurate and linear period-to-voltage conversion under such conditions.

The circuit consists of a monostable multivibrator (Q_1 and Q_2), a linear ramp generator (Q_3 and Q_5) and a sample-and-hold circuit (Q_4 and A_1). The sample/hold circuit at the output allows accurate tracking of rapid changes in period, because each step is independent of its predecessor.

The voltage across C_5 must be sampled before the capacitor is discharged; therefore a delay must be included in the circuit. In the circuit of Fig. 1, the monostable multivibrator (Q_1 and Q_2) provides the necessary delay. This one-shot activates the sample/hold circuit when it is triggered by an incoming pulse. When the one-shot recycles it discharges C_5.

An input pulse causes the collector of Q_2 to go positive, thus turning on Q_4 and allowing C_5 to charge C_6. Note that the capacitance of C_6 is small compared to C_5. Thus the loading of C_6 on C_5 is not a serious problem. This loading affects circuit performance only when the input period slews rapidly; and the effect can be corrected with a unity-gain buffer.

When the multivibrator recycles, Q_4 is turned off and C_6 remains charged to a voltage proportional to the period of the input signal. Amplifier A_1 acts as a buffer and, because A_1 has unity gain, the voltage on capacitor C_6 appears at the output.

Also, when the multivibrator recycles, a positive-going pulse is produced at the base of Q_5. This transistor then discharges C_5. The capacitor then starts to recharge until another input pulse is received and the cycle begins again.

Figure 2 shows typical waveforms at various points in the circuit, illustrating the sequence of events. In the graph of Fig. 3, output voltage is plotted against input period. The scales are logarithmic and a range of two decades is shown. Note that the response is essentially linear and that the slope is unity.

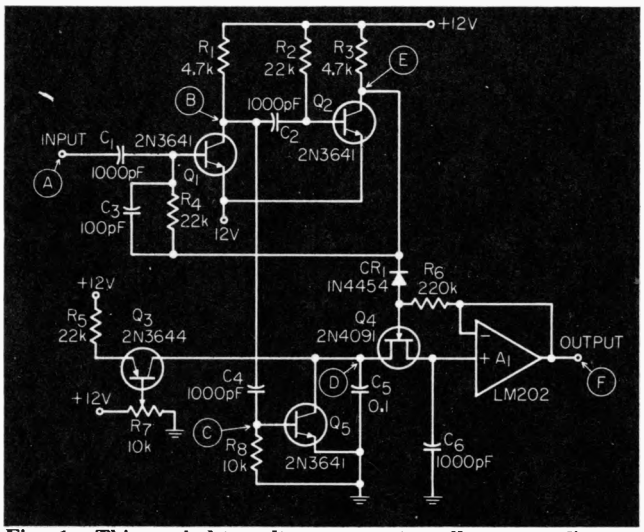


Fig. 1. This period-to-voltage converter allows sampling at rates approaching the input frequency, but without introducing excessive ripple.

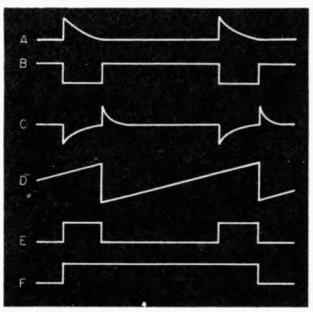


Fig. 2. Timing diagram for the circuit of Fig. 1.

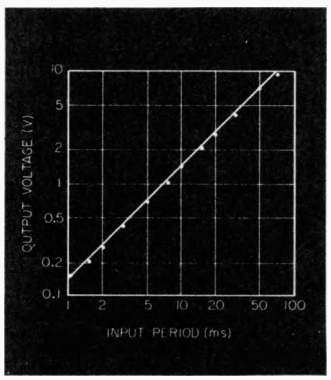


Fig. 3. Measured response shows that output voltage is directly proportional to input period over a range of two decades. The line has a slope of one.

Starting network for transistor inverters

Now that plastic-encapsulated silicon controlled rectifiers and unijunction transistors are widely available at relatively low cost, these devices can be used in many circuits for which they were formerly too expensive. One example is in the starting circuit for a transistorized power inverter.

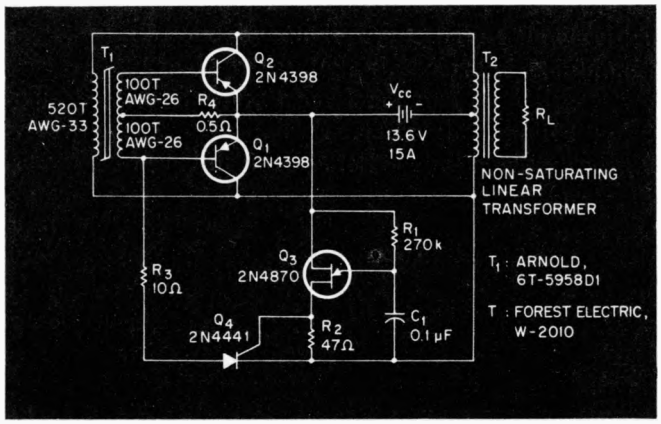
The SCR and UJT circuit described here has the advantage that it consumes negligible power after the inverter has started. Thus the starting circuit doesn't detract from the operating efficiency of the inverter.

Though the schematic shows a common-emitter voltage feedback inverter using pnp transistors. the basic starting circuit can be easily adapted for use with other inverter circuits. Components R_1, C_1, Q_3, R_2, Q_4 and R_3 constitute the starting circuit.

The UJT is connected as a relaxation oscillator. Components R_1 and C_1 form the time-constant for this oscillator, and this time-constant should be long compared with the inverter's oscillation period at maximum supply voltage. Resistor R_g shunts the output from base-1 of the UJT, to prevent overdriving the gate of the SCR.

Resistor R_s limits the drive to Q_1. This resistor should be small enough to supply sufficient base current to fully saturate Q_1 during starting; but it should be large enough to avoid exceeding Q_1's surge rating. The required value can be calculated from the following equation:

$$R_s = \frac{V_{cc} - V_f}{I_c/\beta_f} = \frac{\beta_f (V_{cc} - V_f)}{I_c} \quad (1)$$



The starting circuit (Q_3 and Q_4) for this 400-hertz inverter draws negligible quiescent current — thus it doesn't detract from the inverter's efficiency.

where,
β_f is the forced gain of the inverter transistors under starting conditions,
V_{cc} is power-supply voltage,
I_c is collector current of the transistors under starting conditions,
V_f is forward voltage drop of the SCR while conducting.

The value of R_1 should be less than 1 megohm. With the values shown, time-constant R_1C_1 is 3.75 × 10^{-3} seconds. This assumes that Q_3 has an intrinsic standoff ratio of 0.6 or greater. The R_1C_1 time-constant should be greater than 2.5 milliseconds.

The starting circuit works as follows: Initially, V_{cc} is turned on and capacitor C_1 charges toward the supply voltage through resistor R_1. At this time, the anode of Q_4 is at the positive supply voltage, and the SCR's cathode is connected through the output winding to the negative side of the supply. When the ratio V_{c1}/V_{cc} exceeds the intrinsic standoff ratio of Q_3, the UJT fires and discharges C_1 into the gate of the SCR. Base-drive current for output-transistor Q_1 then flows via R_3 and Q_4, until Q_1 turns on.

Regenerative voltage feedback in the inverter circuit then fully saturates Q_1, and its base becomes negative with respect to its collector. This reverse-biases the SCR, causing it to commutate off. At this point the inverter is free-running.

The starting circuit stays turned off while the inverter is operating normally. Because the time-constant R_1C_1 is relatively long compared with the inverter's half-period of oscillation, the UJT cannot fire the SCR again — not even during the period when Q_2 is conducting and, thus, placing approximately half the supply voltage across the starting circuit.

With the component values shown, the inverter circuit operates at 400 hertz, with an output power of 200 watts at 115 volts. The starting network gives reliable starting over the temperature range −40 to +100 degrees C.

New line-operated inverter offers fast switching and high efficiency

WITH THE AVAILABILITY of improved power transistors (for example, the Fairchild 2N-5264) that can switch inductive loads at high currents and voltages, engineers can now design efficient high-frequency inverters that don't need saturable reactors. The low weight and easy filterability of high-frequency inverters make them a logical replacement for bulky 60-Hz power transformers in power supplies.

For line inverters, the output transistors should have low saturation voltages and fast switching times to allow high efficiency at high frequencies. Gain is relatively unimportant except that, of course, high-gain output transitors can operate with simpler drive circuits, and with less power loss. If the transistors can dissipate inductive energy, at voltages near breakdown, then the circuitry can be further simplified because voltage clamping isn't necessary.

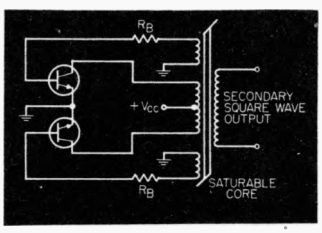


Fig. 1. The simple Jensen inverter has the disadvantage that it uses a saturable core. The core limits the switching speed, so the circuit is inefficient at high frequencies.

The 2N5264, used in the circuit of Fig. 2, has a voltage rating of 180 volts and a current rating of 10 amps. Rise and fall times are typically 250 ns at 7 amps, and typical collector saturation voltage is 0.25 volts at 5 amps.

Before discussing the improved inverter circuit, let's look first at some of the disadvantages of the simple Jensen push-pull inverter shown in Fig. 1. The circuit uses a saturable-core transformer in a grounded-emitter push-pull arrangement. When the core saturates, the drive to one transistor falls off and the device is turned off. This reverses the transformer voltages, turning on the other transistor.

In a later modification to the Jensen circuit, there is a saturable reactor in the base-drive circuit only. Both circuits have the disadvantage that their upper working frequency is limited by the speed at which the core can saturate. Core-dominated switching times cause losses in the transformer and in the output transistors. Hence efficiency of these circuits is poor, especially at high frequencies.

A more sophisticated class of inverter circuit uses a buffered oscillator to drive the output devices. This arrangement has the advantage that drive current and output frequency are independent of loading. Thus operation is stable over a wide range of load conditions. The output devices can be driven directly, or via transformers, or via capacitors.

The circuit of Fig. 2, the IC gates are cross-coupled to form a 20-kHz free-running multivibrator. After two stages of amplification, the output from the multivibrator drives the output transistors. Capacitive coupling eliminates a base transformer. This arrangement is more efficient than direct drive, because low collector voltage can be used for the driver stages.

The output transistors are connected to voltage-sharing capacitors that are connected in series across the rectified line voltage. With this type of circuit the breakdown voltages of the transistors can be half that usually needed for an inverter circuit. Because operating frequency is fixed, simple RC networks across the transformer primaries provide effective clamping with a wide range of loads.

The low-level drive circuitry receives its operating voltage from an eight-turn secondary winding on the output transformer. This type of low-level drive configuration needs a starting circuit. The 2N5264

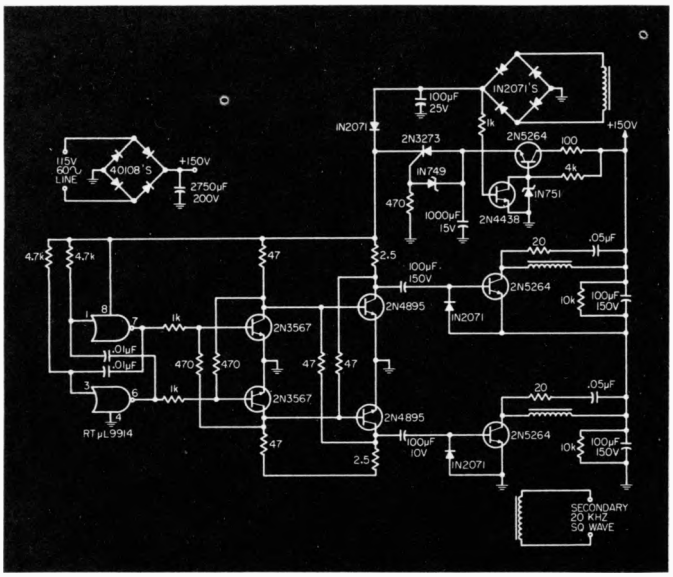


Fig. 2. This improved iuverter circuit has au efficieucy of about 90 perceut at output frequeucies of 20 KHz or higher. Also, the circuit has good voltage regulatiou aud the frequeucy doesu't chauge with load curreut.

pass element and a 2N3273 SCR ensure full-power starting. If there is an overload of sufficient magnitude to cause a drop in secondary voltage, then drive may be temporarily interrupted until the starting circuit can supply a fresh starting pulse. Thus the arrangement provides temporary short-circuit protection.

Output depends, of course, on the transformer ratio. The output stage give 20-kHz square-wave of 148-volts peak across each primary winding. Maximum collector current is 7 amps. Thus the inverter can provide up to 1 kW of output, with power-to-weight ratio of greater than 100 W per pound. Full-load efficiency is at least 90 percent. The total change in collector voltage is only 8 volts for a load change from no-load to full-load.

The cost of this type of inverter is obviously much higher than for a simple line transformer. But the relatively low cost of semiconductors makes the circuit quite competitive with many saturable-reactor designs. Also, for many applications, the advantages of low weight and good regulation will out-weigh any possible cost disadvantage.

Simple circuit converts pulse duty cycle into analog

THIS SIMPLE digital-analog converter uses only four semiconductor devices — three single transistors and a dual transistor. It gives linear conversion from pulse width to output voltage, for duty cycles ranging from 5 to 95 percent. With suitable component values, the circuit can be used with input repetition frequencies from 1 kHz to 1 MHz.

In the circuit of Fig. 1, a linear ramp voltage is generated at point *B*. Amplitude of the ramp depends on input pulse width at point *A*. Peak voltage of the ramp then determines the dc output level at point *C*.

Transistor Q_1 provides a constant-current source that charges capacitor C_2, thus generating a linear ramp at point *B*. Input transistor Q_3 discharges C_2 at the end of each input pulse. Thus pulse width determines ramp duration and, hence, amplitude.

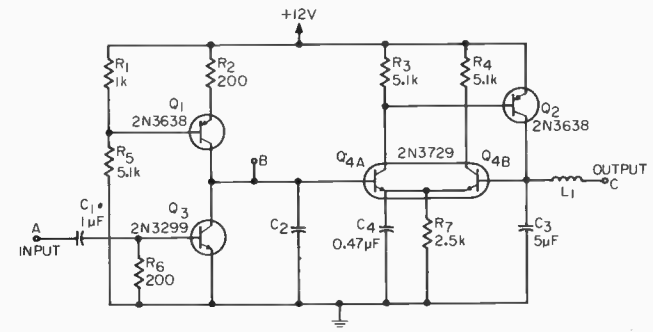


Fig. 1. In this simple D/A converter, Q1 generates a ramp voltage across C_2. Duration and height of the ramp are controlled by the input signal which turns on Q_3 to discharge the capacitor.

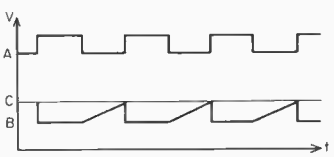


Fig. 2. Typical waveforms show how the output voltage at point C is determined by the peak voltage of the ramp at point B.

The ramp voltage is applied to one input of the differential-amplifier stage, Q_{4A} and Q_{4B}. The other input of the differential amplifier sees the inverted output from amplifier Q_2. A large output capacitor C_3, holds the voltage almost constant at the base of Q_{4B}. Feedback through the differential amplifier tends to maintain the output voltage across C_3. As C_3 starts to discharge through the load, a positive voltage is applied to the base of Q_2 thus maintaining the voltage across the capacitor.

An rf choke, L_1, filters spikes from the output voltage. A prototype version of this circuit has been built with output ripple of 0.4 mV. To obtain low ripple, care must be taken to minimize lead length and decouple supply lines.

Operating frequency is determined by C_2 and R_1. The upper limit of repetition rate is about 1 MHz. The lower limit is determined by the physical size of C_2. Good linearity has been achieved at frequencies as low as 1 kHz, using a suitably large value for C_2.

One disadvantage of the circuit is its relatively poor response time with negative-going signals. This is because the load provides the only discharge path for C_3. For fast response to negative signals, additional circuitry would be required to provide rapid discharge.

Passive Dc Converter for Geiger Counter

HERE'S A simple and safe way to generate high-voltage dc from low-voltage batteries. In the Geiger - counter circuit shown in Fig. 1, ten capacitors are charged in parallel to about 27 V. They are then switched in series, together with the batteries, to give the 300 Vdc required for the Geiger tube.

Though this is an old idea, it has previously been impractical for miniature circuits because of the complicated wiring and switching needed. But a printed-circuit switch as shown in Figs. 2 and 3, needs only two external connections. These connections are for the input and output voltages. All other wiring is contained on the PC board.

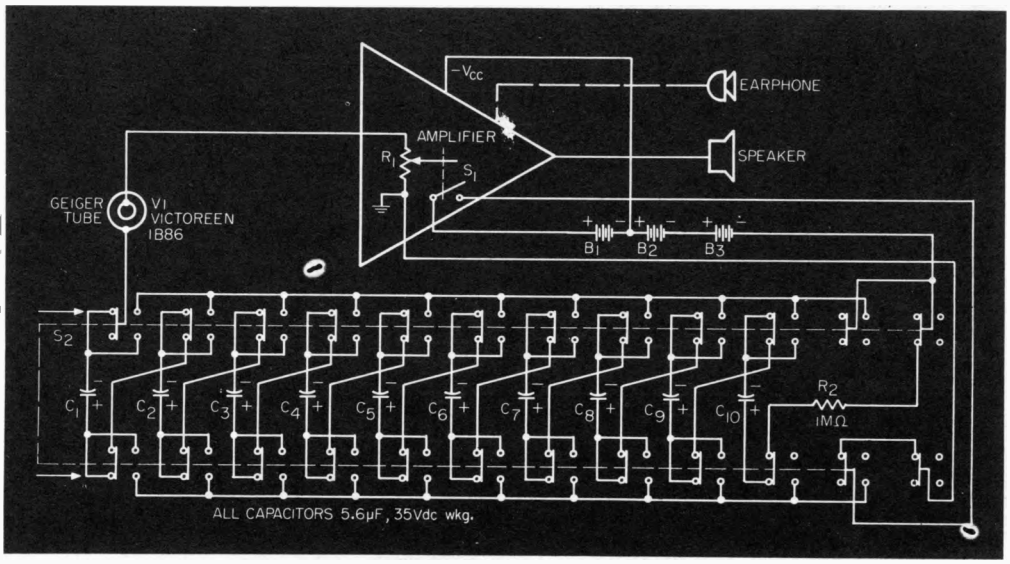


Fig. 1. The switched capacitors in this Geiger-counter circuit provide the high voltage for the Geiger tube.

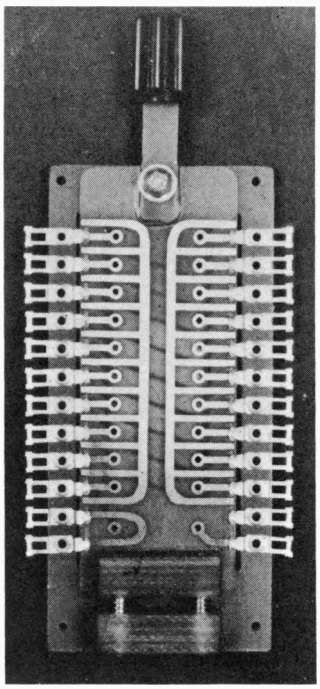


Fig. 2. Front of printed-circuit switch.

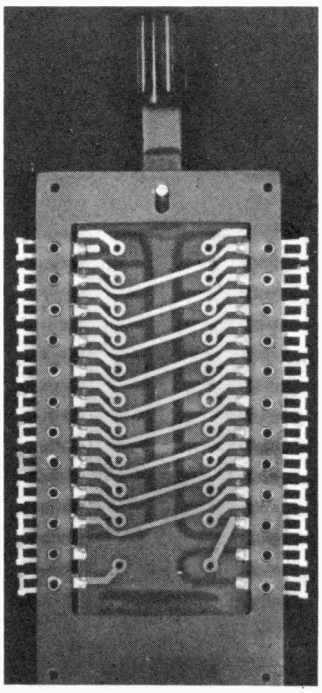


Fig. 3. Rear of printed-circuit switch.

The ten capacitors are mounted on the front of the switch, shown in Fig. 2, in the first ten horizontal positions counting from the top. The eleventh position contains R_2. To understand the switching remember that, except for the input and output voltages, all connections are made by the switch contacts from one edge of the PC board to the other.

The switch has two positions and is spring loaded. In Fig. 1 switch S_2 is shown in the normal operating position. Depressing S_2 with S_1 closed, removes the amplifier from the circuit and places all capacitors in parallel across the three 9-V batteries which are in series. This charges the capacitors.

When S_2 is released, it returns to the normal position shown in the diagram. This connects the amplifier to B_1 and also connects in series the capacitors, R_2 and the batteries. Thus the Geiger tube receives normal operating voltage. Resistor R_2 provides quenching.

The amplifier can be any suitable audio amplifier. The original version of this circuit used the audio portion of a low-cost transistor radio. Components R_1 and S_1 are the ganged volume control and on-off switch of the amplifier.

Current drawn by the Geiger tube is negligible and the operating time, after charging the capacitors, is limited only by leakage. With the components shown in Fig. 1, the counter runs for over 30 minutes on a single charge.

Signal-powered sine-to- square wave converter

FIGURE 1 illustrates a sine-to-square-wave converter that is designed to plug into a 600-Ω audio oscillator. As it is signal powered, no external power source is required.

The 600-Ω oscillator output Fig. 2a, is peak rectified in both directions by D_1 and D_2 in order to derive positive and negative supply voltages. Q_1 and D_4 form a differential amplifier referenced to ground that symmetrically clips the sine wave as illustrated in Fig. 2b. R_1 is used to limit saturation and D_3 balances the input loading.

The output of Q_1 is level shifted by C_4 and D_5 and applied to another stage of clipping. C_5 and C_6 are speed-up capacitors.

As illustrated in Fig. 2c the

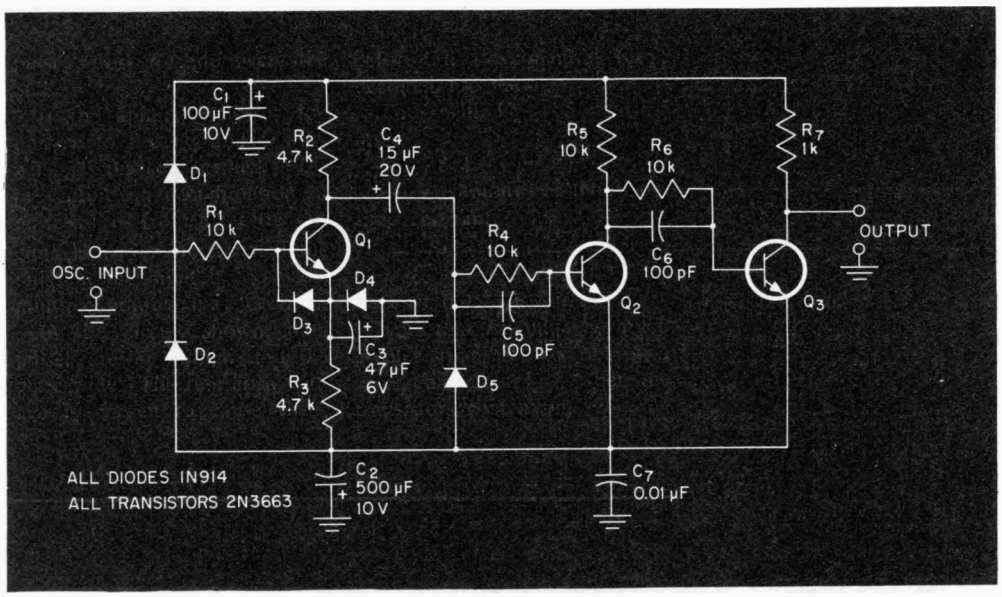


Fig. 1. Signal powered sine-to-square-wave converter schematic.

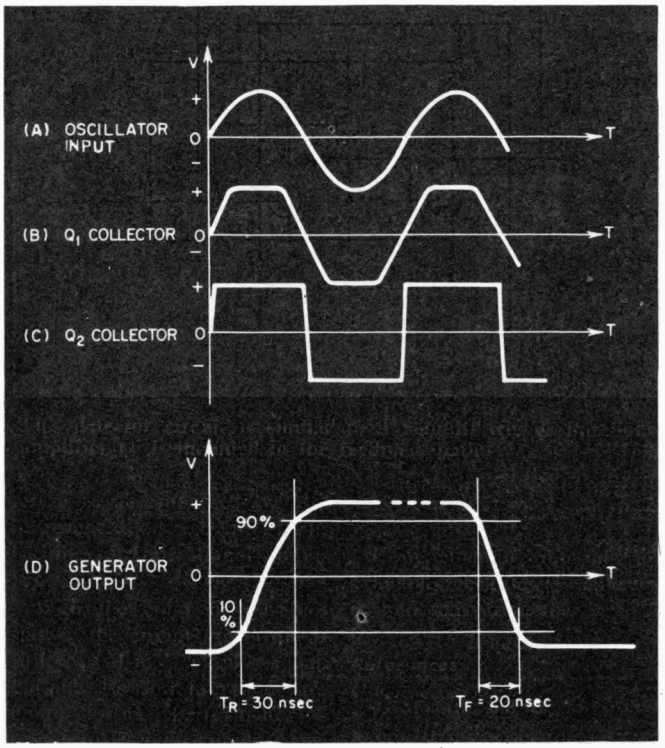


Fig. 2 Typical waveforms at various points in circuit shown in Fig. 1.

signal at this point has sufficiently small rise time so that the rise time of the output stage, Q_3, is only limited by its device characteristics. The output waveform is illustrated in Fig. 2d and is essentially independent of frequency.

This circuit is capable of providing an ac square-wave output from 5 Hz to 600 kHz. The input level adjusts the ouput for 2 to 16 V pk-pk with ±1% symmetry. The output waveform has a 20-ns rise time and a 30-ns fall time. ■

Differential to absolute value converter

A CIRCUIT FOR converting a differential-analog voltage to a single-ended absolute value voltage is shown in the figure. The circuit maintains a high input impedance in order not to load the differential input. A typical use of this circuit is in comparing a differential level to a threshold level with a high measure of common-mode rejection.

The converter operates in the emitter-follower mode with one pair of transistor emitters developing the differential-input voltage between them. For example with the input polarity shown, the emitter of Q_{1A} assumes a voltage according to the equation:

$$V_e\,(Q_{1A}) = V_b\,(Q_{1A}) + V_{be}\,(Q_{1A})$$

The emitter of Q_{1B} assumes the value:

$$V_e\,(Q_{1B}) = V_b\,(Q_{1B}) + V_{be}\,(Q_{1B})$$

The voltage difference between the emitters of Q_1 is:

$$V_e(Q_{1A}) - V_e(Q_{1B}) = V_b(Q_{1A}) + V_{be}(Q_{1A}) - V_b(Q_{1B}) + V_{be}(Q_{1B})$$

But since the 2N2803 is a matched-dual transistor

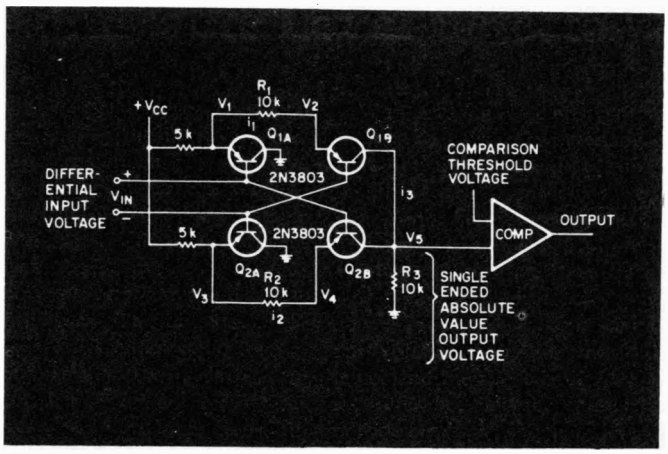
$$V_{be}(Q_{1A}) = V_{be}(Q_{1B})$$

Therefore $V_e(Q_{1A}) - V_e(Q_{1B}) = V_b(Q_{1A}) - V_b(Q_{1B})$. But

$V_b(Q_{1A})$ — $V_b(Q_{1B})$ is the differential input voltage. This voltage appears across R_1 which sets i_1.

Since the minimum hfe of the 2N3803 is 300, the emitter current in Q_{1B} essentially matches the collector current. Therefore $i_1 = i_3$. By making R_3 equal to R_1, the voltage at the single-ended output is then equal to the differential input.

Q_{2B} emitter does not contribute any current since it is in the cutoff state due to its base being at a higher potential than the emitter of Q_{2A}. When the input polarity is reversed, Q_{2A} and Q_{2B} conduct and Q_{1B} is cutoff. It is apparent that the output voltage is also positive in this case. ■

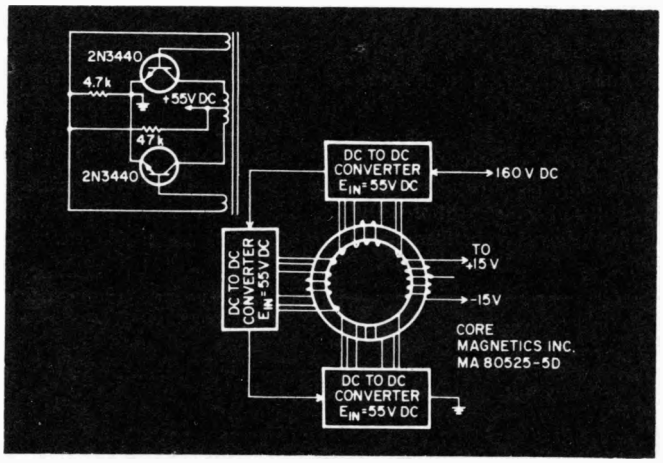


Two dual transistors are used to form a differential to absolute-value converter. The example shown compares a differential level to a threshold level.

High voltage dc-to-dc converter

THIS CIRCUIT CONVERTS a rectified line voltage (about 160 Vdc) to ±15 Vdc. A conventional converter uses transistors with collector ratings of 400 V but this converter by a clever design technique, uses 135-V transistors.

A cascade of three dc-to-dc-converters is constructed on a single tape-wound core. There are three input windings connected in series and one output winding. Since all input windings are on the same core and are magnetically coupled, all three converters share the input voltage equally. The single output winding eliminates load hogging. This unit delivered +15 V at 50 mA and −15 V at 50 mA. Package size is 2.5 in.³ including line rectifiers. ■



A novel cascade scheme eliminates high-voltage transistors in this dc-to-dc converter.

Section 14
POWER SUPPLY CIRCUITS

Full-Wave Control with One Trigger and One Control Rectifier

ONLY one control rectifier and one single-ended trigger, as shown in Fig. 1, are necessary to obtain continuously variable ac or dc full-wave output. Conventional circuitry requires more than one control rectifier and usually double-ended triggers.

The circuit offers increased reliability, simplicity and reduces substantially the components cost.

The voltage of the supply will be determined only by choice of components. Any voltage within the standard service power voltages may be designed into the circuit. In the trigger portion only R_1 will have to be changed with change of input voltage. In the scr circuit, the semiconductors $CR_{2A\text{-}D}$ and the control rectifier scr will be picked out with the proper rating. Size and weight will not be affected. Thus a unit handling 2 kw will be capable of handling 4 kw with components rated for twice the voltage and twice the input voltage without much change of size and weight.

The semiconductor bridge consists of four rectifiers $CR_{2\text{-}AD}$ and one scr. Two rectifiers would be sufficient if a center tap transformer were used. However the weight and size will increase appreciably making center tap in most cases undesirable.

The scr is biased forward every half cycle of supply frequency due to the configuration of the bridge. Load current has always to pass through the scr, and, thus, the amount of load current will depend on the firing angle of the scr, which is in turn dependent on the firing of the unijunction transistor Q_1. Following the instantaneous polarities of the input, when terminal 1 is positive the path for current flow is through CR2A, the scr, and CR2D, to the load. When terminal 2 is positive, the path for current flow is through the load, CR2C, the scr, and CR2B to terminal 1, and load will be furnished controlled current at every half cycle.

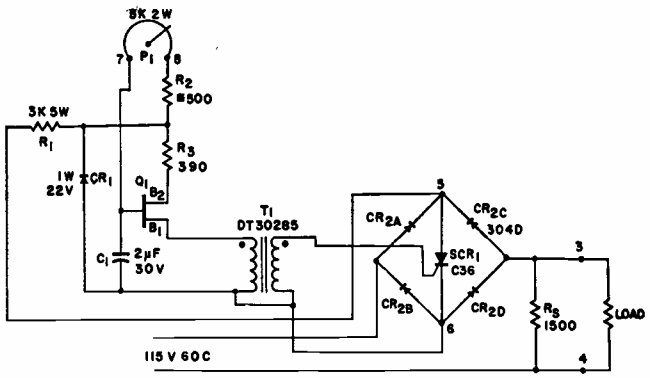


FIG. 1—Full-wave output is provided with one unijunction trigger and one controlled rectifier.

The input to the trigger is connected across points 5 and 6. Point 5 is always positive with respect to point 6 and thus the supply between 5 and 6 is a suitable source of energy for the trigger. No separate rectifier bridge is needed. Resistor R_1 acts as a limiting resistor for the zener diode CR_1 and the trigger circuitry. Zener diode CR_1 acts as a clipper to truncate the input wave and limit it to the proper level. Capacitor C_1 and resistor string P_1 and R_2 make up the RC network which determines at which instant in the cycle unijunction transistor Q_1 will fire.

Transistor Q_1 fires into T_1, which transmits the pulse to the gate of the scr. A pulse will be generated every half cycle at an instant dependent on the setting of P_1. The latter may be remotely connected with light hook up wire or it may be driven by a miniature servo motor or replaced by a tube, tran-

sistor or other means of control when automatic or closed loop operation is desired. It may be eliminated by shorting terminals 7 and 8 and a transistor connected across C_1 for purposes of automatic operation.

The trigger is always synchronized with the power bridge because both obtain power from the same source.

Resistor R_8 provides the ability of the controller to work into highly ac inductive and ac motor loads. It dissipates not more than 3% of the load volt ampere.

Tests were conducted and the unit was used to adjust the speed and drive a single-phase ac induction motor, driving a centrifugal pump and fan, to adjust the speed and drive a uiversal motor of the type used in machine tools, and to adjust the light output of an incandescent high power bulb.

A control of this type, for 2-kw output, will weigh not more than 4 pounds.

Regulated Low Voltage Power Supply

ABILITY to produce positive and negative potentials with an impressive overall regulation derived from one the use of low cost diodes is the feature of the circuit shown in Fig. 1.

It was designed to supply well regulated low dual voltage potentials to transistorized time-controlled circuits. These transistor time-controlled circuits in turn would be used in test equipment that is concerned with the repair of Bell System 28 type (Automatic Sending and Receiving) data processing equipment.

Present commercially manufactured circuits do not provide a low dual voltage with accurate regulation for voltage input variation.

This simple single-phase regulated power supply requires the minimum diodes for rectification and regulation as well as electrolytic capacitors. Since the rectifier in this circuit conducts only when the upper ac input terminal is positive the first filter capacitor C_3 is charged only once during each cycle of the supply voltage, likewise for filter capacitor C_5 charging with regard to the negative portion of the cycle. The ripple frequency therefore is equal to the supply voltage frequency. When rectifier diode D_1 is conducting during the half cycle the upper ac terminal is positive, filter capacitor C_3 will become charged instantaneously to the peak of the ac input voltage (less the conducting voltage drop through the diode) and maintain the dc voltage during the negative cycle.

The function of R_1 (Fig. 1) is to minimize the large surge currents prevalent in half-wave circuits. Current flowing through R_1 causes a voltage drop which is greatest when the surge current reaches its peak and assumes a steady value when, after the first few cycles, the capacitor becomes fully charged. Resistor R_1 also acts as a fuse in the circuit and protects relatively expensive components in the event of a short circuit across the load.

The functions of diode D_2, resistor and capacitors C_4 and C_6 in the negative section of the rectifier are the same as those of the positive section.

Voltage regulation is provided by diodes (zener) D_5 and D_6. These diodes are connected across the power supplies load. This combination is fed from the unregulated supply voltage, V_1, through series chopping resistor, R_3 and R_4. The flat voltage characteristic of the diode holds the load voltage essentially constant on the load current and/or supply voltage changes. A change in load current results in a corresponding change in diode current. Therefore, the voltage drop across resistors R_3 and R_4 remains unchanged with variations in load current. A change in input voltage, V_1 produces a corresponding change in diode current which causes the change in voltage drop across resistor R_3 and R_4 necessary to cancel the change in input voltage, thus holding the load voltage constant.

Input voltage range is from 80 to 120 ac. Output of ± 22 volts can be increased or decreased with

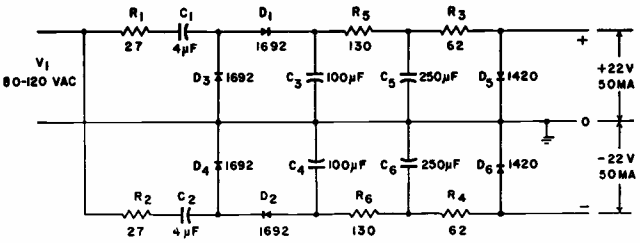


FIG. 1—Regulated low-voltage power supply.

selection of zener diodes per required voltage. Regulation is ± 5 per cent.

Max current range is 100 ma, and can be increased with selection of high current capacity diodes. Diodes D_1, D_2, D_3 and D_4 are General Electric 1692. Diodes D_5 and D_6 are Western Electric type 1420.

Zener Diode Bias Clamp

PROVIDING a stable bias voltage for electronic circuit without complex regulated power supplies has long presented a problem to the design engineer.

The problems involved with bias systems employing the raised common return for the unit power supply are numerous. In particular in those circuits where the bias is used to cut-off control tubes in vacuum tube relay devices, the overall sensitivity of the system is impaired by the bias voltage sliding up as the tube begins to conduct. To overcome this

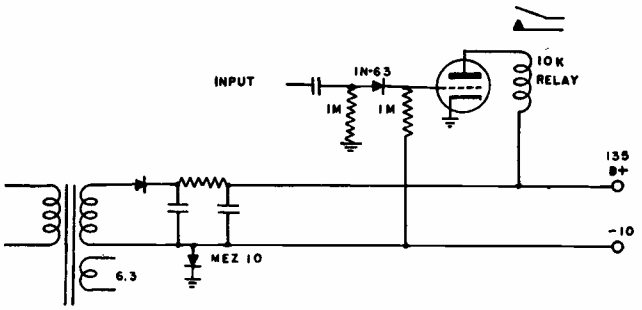


FIG. 1—Zener diode provides ground return for bios supply.

effect, an International Rectifier MEZ-10 zener diode was used as a ground return for the power transformer as shown in Fig. 1.

An additional bonus was derived from the fact that with no filter devices the negative voltage generated exhibited very low ripple and was clean enough to be used as the power source for a two-stage transistor pre-amp.

This system is suggested as an ideal source of both bias and transistor power in hybrid circuitry of this type.

Reference Voltage Polarity Reversing Circuits

IT MAY BE desired to obtain a reference voltage similar to one already existing in a circuit but of opposite polarity, or to obtain voltages of both polarities from a single zener diode. The circuits shown offer several ways of accomplishing this, if an ac supply larger than the reference voltage is available. In each case an ac voltage is developed with a peak to peak amplitude determined by the reference voltage and is then rectified with the desired polarity.

The circuit of Fig. 1 supplies a reference voltage of reverse polarity from an existing voltage E. During the ac input positive half cycle, C_1 is charged up to voltage E, since the drop across D_2 is cancelled by the drop across D_3. On the negative half

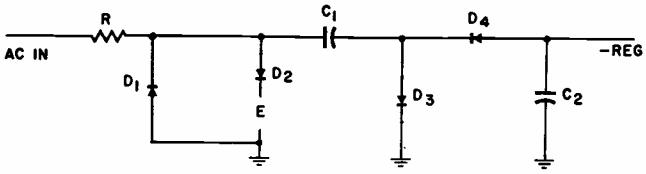


FIG. 1—Voltoge of E is reversed in polority.

cycle, this voltage appears at the output, with the voltage drops across D_1 and D_4 cancelling. Filter capacitor C_2 must be large enough to hold the output relatively constant during the input positive half cycle.

The second and third circuits show two ways of obtaining voltages of both polarities from a single

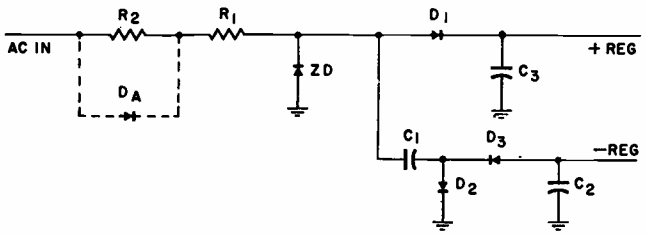


FIG. 2—Zener diode reploces two diodes of Fig. 1.

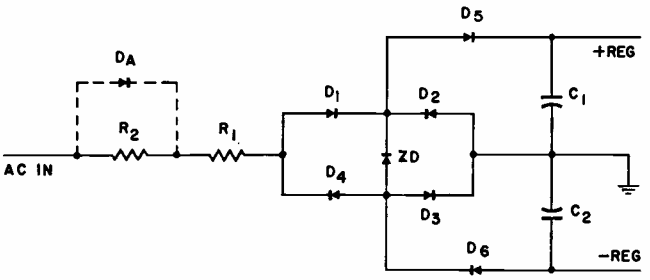


FIG 3—Addition of diode D_A permits adjustment of current.

zener diode. In Fig. 2, the zener diode performs the same function as D_1, D_2 and E of Fig. 1, and the negative output is achieved in the same manner as in that circuit. A positive output voltage is readily obtained by rectifying and filtering the square wave across the zener diode with D_1 and C_3.

A diode bridge is used in the circuit of Fig. 3. During the positive half cycle of the input, current flows through D_1, the zener diode, and D_3. Output capacitor C_1 is charged up to the zener diode voltage, since the drop across D_3 and D_5 cancels. On the negative half cycle, D_4, the zener diode, and D_2 conduct, with negative output across C_4. If needed, diode D_A shown connected with dashed lines in the ac input in Fig. 2 and 3 and its shunt resistor R_2, allow current adjustment for differing positive and negative output currents. The diode polarity is chosen to by-pass the extra resistor R_2 during the half cycle supplying the greater current. All capacitors shown should be large enough so that only a negligible amount of ac appears across them.

High-Efficiency Power Supply Regulation

A POWER SUPPLY capable of regulating the dc output voltage with changes in load and/or input voltage is required for many applications. Most methods of achieving regulation require that the regulating device (transistor, vacuum tube, etc.) absorb the difference in power between extremes in load and/or line excursion. The efficiency of this type of regulator is poor, often as low as 20 to 30 percent.

Figure 1 is a schematic of a regulated power supply where the efficiency is in the order of 80

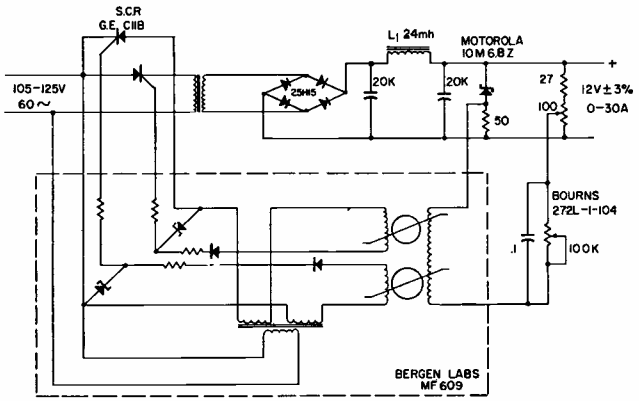


FIG. 1—High-efficiency power supply for low-voltage applications.

per cent. By controlling the firing angle of a pair of silicon controlled rectifiers connected in the primary circuit of the transformer, the voltage delivered to the transformer may be controlled. The high efficiencies achieved are due to the fact that the rectifiers function as near-perfect switches, dissipating little power. The dc output voltage of the supply is referenced against a zener diode voltage and the resultant error signal E_r appears across the control windings of a full-wave magnetic amplifier. The magnetic amplifier provides the necessary gain and gate voltages for controlling the rectifiers. The loop has thus been closed between output and input of the power supply. An increase in the dc output results in a retarded firing angle which brings the output voltage back down. A drop in the dc voltage results in the firing angle being advanced, thus raising the output to its previous level.

Figure 2 illustrates the ability of this arrangement to adapt to almost any output voltage as

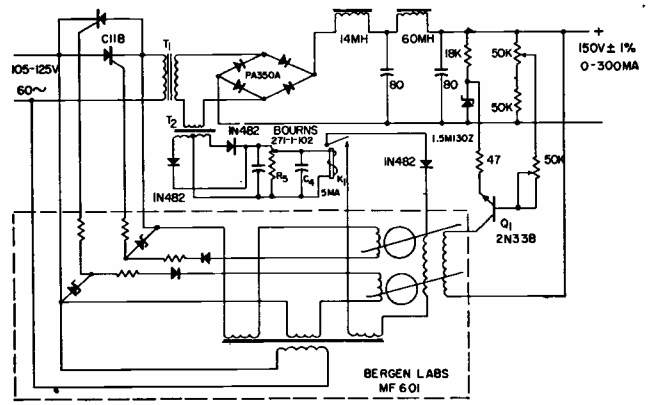


FIG. 2—High-efficiency circuit for 150-volt output and one per cent regulation.

required. A higher order of regulation has been achieved in this circuit by providing additional gain through the use of transistor Q_1.

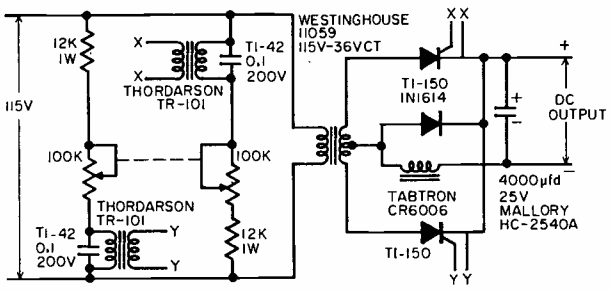
Overload and short circuit protection are accomplished through the use of a relay circuit operated from current transformer T_2. Trimpot R_5 is adjusted so that relay K_1 closes at the desired overload current, causing large reset voltage to be applied to the magnetic amplifier.

Gate voltage to the silicon controlled rectifiers is removed when the magnetic amplifier is fully reset, thus the primary voltage to the power supply is interrupted. Capacitor C_4 determines the rate at which relay K_1 is recycled and hence the quiescent output current during overload conditions. Upon subsequent removal of the short or overload, the output voltage will automatically return to its normal setting. Because of the high efficiency possible with this type of supply, operation at elevated temperatures becomes practical.

Variable High Current Remote Power Supply

WHEN SILICON controlled rectifiers are used as the rectifying elements in power supplies, the output dc voltage can be varied without changing the ac input voltage. The conduction time of the *scr*'s during each half cycle determines the average power that is delivered to the load. The conduction time is controlled with a pulse gating circuit synchronized with the line, and phase variable. The complete circuit is shown.

The filter choke is connected between the center tap of the transformer and ground. This allows the cathodes and gates of the *scr*'s to remain at the output dc voltage at all times and makes *scr* firing easier and more reliable. The choke serves to limit *scr* surge currents and filters the output voltage. A filter capacitor is also



Power supply uses an scr thus enabling the output dc voltage to be varied without changing the input ac voltage.

used for additional smoothing. The rectifier, connected between the center tap of the transformer, and the output, allows the choke to transfer its stored energy to the load when the *scr*'s are not conducting. The transfer of stored energy is in effect a current transformation; it increases the output current capability of the power supply above the current ratings of the power transformer and the *scr*'s.

The two *scr*'s receive gate signals after their respective anodes have gone positive. Once turned on, the *scr*'s conduct the remainder of the half cycle and are

turned off when the line voltage reverses itself. If the *scr's* are fired earlier in the cycle, the output dc voltage will increase as a result of longer conduction time.

Scr's receive their gating pulses from a pulse generator synchronized with the line and phase variable. The pulse generator consists of an *RC* charging network and a breakdown diode. The 0.1μfd capacitor charges at a rate determined by the series *RC* circuit. Once the capacitor has reached the firing potential of the TI-42 breakdown diode, it fires and dumps the stored energy of the capacitor through the primary of the Thordarson RT-101 pulse transformer. This action generates a current pulse which is transformer coupled to the gate of the *scr*. The diodes connected across the 0.1μfd capacitors prevent them from charging in the negative direction, and insures that positive charging will start at the beginning of each positive half cycle, thus preventing erratic firing. Decreasing the resistance in the variable resistor will decrease the charging time of the 0.1μfd capacitor and cause the breakdown diode to fire earlier in the cycle. An increase of resistance will cause a corresponding delay.

A separate pulse generating circuit is provided for each *scr*. The variable resistors of each are ganged together to give simultaneous control. In order to utilize the fast rising wave front of the current pulse, the pulse generating elements should be located near the scr's. The variable resistors need only carry 60 cps ac and may be located a great distance from the power supply. It, therefore, lends itself to easy remote control.

The power output of this type power supply is limited only by the voltage and current ratings of power transformer, choke, *scr's* and rectifier. The components shown in the circuit provide a maximum output of 20 v and 60 a.

Automatic Chassis Ground Circuit

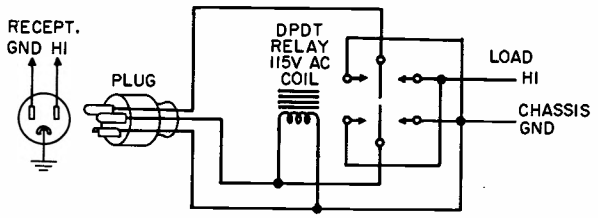
LINE-OPERATED, transformer-less equipment is often used with the chassis connected to one side of the line. If, in such a case, the chassis happens to be plugged into the power hi side, it is connected at line potential with respect to ground. This is a dangerous situation and often leads to electrocution of people operating a home TV set under such conditions.

Various tricks have been devised to minimize this possibility. For instance, polarized receptacles and relays have been designed to shut the circuit off if the plug is incorrectly inserted.

The device described here uses the Underwriters Laboratories plug with ground lug and establishes a true ground which automatically reverses polarity if the chassis is at line potential. If such a receptable is not available, the wire marked with an asterisk may be separately grounded to a water pipe, for example, to achieve the same result.

The only equipment required is a DPDT relay, break-before-make type, with contact capacity sufficient to operate the load. If the plug is inserted with the white blade side at ground, no potential is applied to the relay coil and power goes to the load as shown. If, however, the side marked white is at line potential with respect to ground, the relay operates reversing the polarity of the power before transmitting it to the load, thus properly polarizing the output power.

If, for some reason, both lines are at high potential with respect to ground, a loud relay chatter will be heard and the operator may wish to resort to an isolation transformer.



Automatic chassis grounding polarity selector. Wire marked with asterisk may be grounded to water pipe if plug and receptacle lack ground lug.

VHF Balanced Parametric Doubler

THE REQUIREMENT for a moderate power solid-state source near the upper limit of vhf may be met by using active circuits to about 125 mc, followed by a low-loss passive multiplier. The circuit in Fig. 1 is a balanced configuration with several advantages: 1) It can handle twice as much power as a single-ended circuit using the same varactor diode. 2) The diodes are less expensive than comparable high-power units. 3) The drive current at $I_1 \sin \omega_0 t$ is cancelled in the output arm of the balanced bridge, thus simplifying the filter requirements. 4) Greater than 20 db of ω_0 rejection is easily realized over the single-ended scheme when the bridge is balanced.

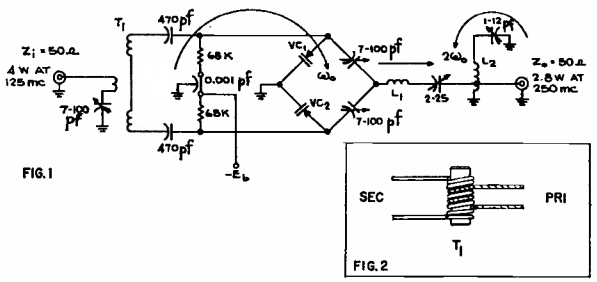


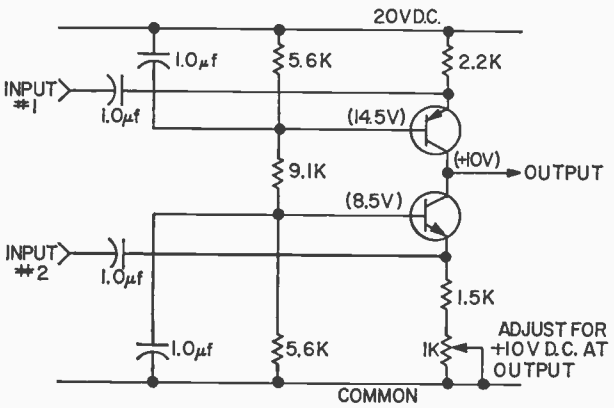
Fig. 1. Balanced parametric doubler for vhf operation. The two varactors are PSI type PC-116. The primary winding of T_1 has two turns of #18 enameled wire, centered and bifilar to the secondary which uses six turns of the same wire on a 1/4 in. diam. core. (See Fig. 2.) L_1 has three turns of #16 enameled wire, spaced one wire diameter apart, on a 1/4 in. core. L_2 is the same as L_1 except for a double tap one turn from the cold end. Capacitors should have mica, glass, or air dielectric.

The bridge trimmers alleviate the necessity of matching diode pairs. At 25 C up to 4 watts at 125 mc may

be applied if the diode cathodes are thermally secured to a heat sink. An efficiency of 70 percent is achieved and the spurious content is about 40 db below $2\omega_0$ with the filtering shown. Separate bias resistors allow the diodes independently to forward conduct a few degrees each cycle. A self-bias voltage of about −30 vdc is common. A fixed $-E_b$ of about 1/2 that voltage is applied, since a zero $-E_b$ "cold start" would present a load that would be over an octave off resonance, a severe chore for the driver stage.

The filter inductors are 1/4 in. I.D. air core and spacing is one wire diameter. T_1 is tight wound on a 1/4 in. nylon rod having the primary bifilar and in the center of the secondary for greatest mutual coupling as shown in Fig. 2. Physical symmetry is important for electrical balance. The series input network, and the bridge trimmers are first adjusted for minimum vswr between the driver and the doubler input. The filters at $2\omega_0$ are next tuned for maximum output at 250 mc, and the bridge finally touched up to minimize ω_0 in the output. Bias adjustments should be varied with input power and varactors to yield maximum efficiency. The output transducer taps may also be adjusted to match the diode bridge to the load.

collector circuit, one can obtain extremely high voltage gain. This is because the constant-current source simulates a very high load resistance though it permits the amplifier to operate at a reasonably high current level.



High-gain, single-transistor amplifier uses constant-current source in collector circuit.

400-Volt SCR Constant-Current Source

AN SCR WILL FUNCTION as a linear amplifier if it is biased with the polarities shown in Fig. 1. High breakdown voltage, linear gain characteristics, and low cost combined with a TO-5 package make the SCR ideal for high-voltage applications. Present small-signal silicon transistors are seldom able to approach the 400-volt capabilities of the 2N1599 SCR.

The anode is biased as a pnp transistor while the gate is biased as an npn device. The disadvantage of low current gain is easily overcome by using a high-gain driver, making possible full utilization of the high-voltage capabilities.

A 400-volt constant current source was designed making use of the high-voltage and linear characteristics of a 2N1599 SCR. Figure 2 shows the schematic of a 1-ma constant current source with a compliance of from 10 v to 400 v. The differential amplifier (Q_1, Q_2) com-

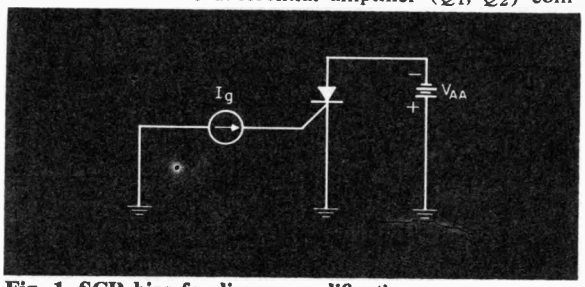


Fig. 1. SCR bias for linear amplification.

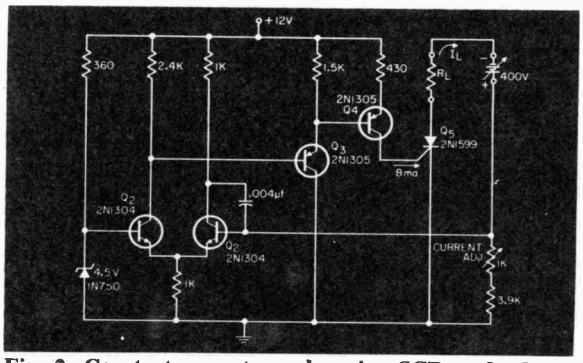


Fig. 2. Constant-current supply using SCR as load-control.

pares the sampled output current with the voltage across a reference zener diode. The output signal from the differential amplifier is fed to a current amplifier (Q_3, Q_4) that controls the gate current (and thus the load current) in the SCR (Q_5).

Regulation, at $I_L = 1$ ma, is typically 0.25 percent with a variation in voltage from 10 v to 400 v. The output current can be adjusted approximately ±10 percent. ◆◆

Low-Loss Biasing Circuit

THE INHERENTLY LOW base-to-emitter drop in germanium power transistors, coupled with the high leakage current, often makes it necessary to reverse-bias the base by returning it to a more positive source than the emitter to obtain stable operation at elevated temperatures. In applications where the emitter is connected to the most positive source, the reverse base biasing often is accomplished with a silicon rectifier in the emitter circuit. A typical example for this is the chopper-stabilized power supply in Fig. 1.

However, in applications where power consumption is critical, the emitter-rectifier type biasing decreases efficiency since the entire load current must flow through the rectifier. Reverse biasing can be better done by winding a small secondary on the filter choke, rectifying it and floating it on top of the dc input as shown in Fig. 2.

This method improves efficiency by eliminating the load current from the biasing circuit while providing sufficient leakage current to insure stable operation to temperatures as high as 80°C. The actual turns ratio and capacitor size are not critical, since R may be selected to provide proper biasing. For the circuit shown, a bias voltage of 6 volts was chosen with $C = 0.56$ μf and $R = 510$ ohms. Measurements show that, with 18-w output and 22-v input, the emitter-rectifier biasing gives

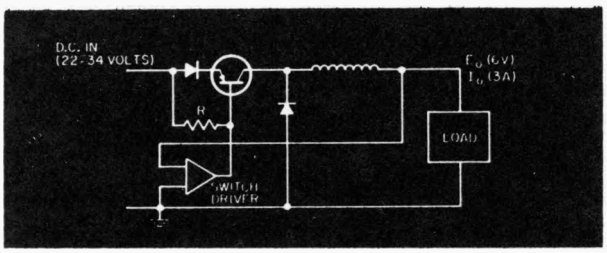


Fig. 1. Emitter-rectifier biasing.

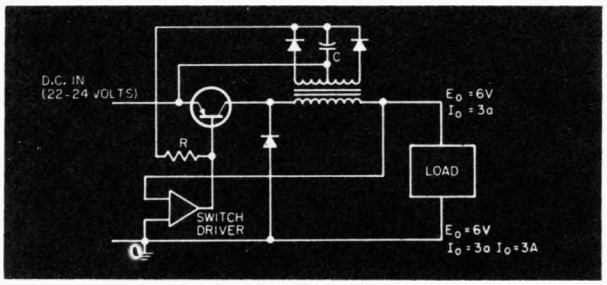


Fig. 2. Low-loss biasing.

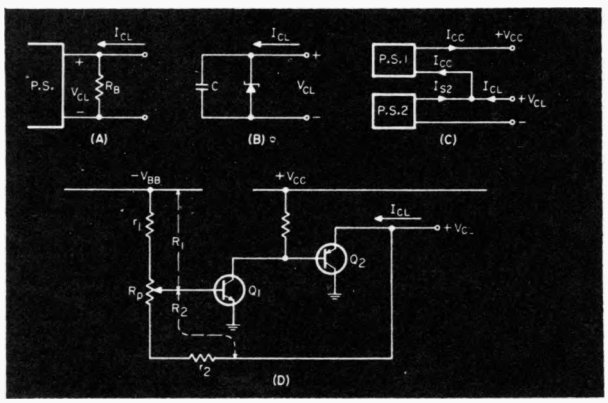
an efficiency of 77.9 percent while the low-loss circuit's efficiency is 83.3 percent.

Constant-Voltage Current Sink

WHENEVER CLAMPED LOGIC CIRCUITS are used, the need arises for a power supply with "negative" output current, or, in other words, a constant-voltage sink. Many methods are commonly used to get that current sink, namely:

■ The use of a bleed resistor R_B (Fig. 1a) calculated to take, at V_{CL}, the maximum clamp current plus the holding current of the power supply. When the clamp current goes to a minimum the power supply must provide $I_{CLmax} - I_{CLmin} + I_{hold}$. The disadvantages here are: the high power dissipated in R_B and the need of a separate power supply for the clamp. The regulation is as good as that of the power supply.

■ The clamp supply is replaced by a zener diode (Fig. 1b) that will develop V_{CL} when I_{CL} flows through it. Capacitor C helps to filter the transients that might appear. The disadvantage is that the regulation is poor. The impedance is that of the zener.



Constant-voltage current sinks: bleed resistor, 1a; zener diode, 1b; two supplies, 1c; and recommended dc-amplifier, emitter-follower circuit, 1d.

■ Two power supplies are connected in series (Fig. 1c). PS_2 provides for V_{CL}, and $PS_1 + PS_2$ give V_{CC}. $I_{R2} = I_{CC} - I_{CL}$. The main disadvantage is the need for two power supplies, one of them (PS_1) being floating.

The new method proposed here (Fig. 1d) consists of a dc amplifier driving an emitter-follower power transistor of the proper polarity (pnp for positive clamping voltage). The input of the dc amplifier is the comparison between the clamping voltage being controlled and a regulated voltage of opposite polarity (the base-bias voltage of the system would do). With some simplifications, the output impedance Z_6 is

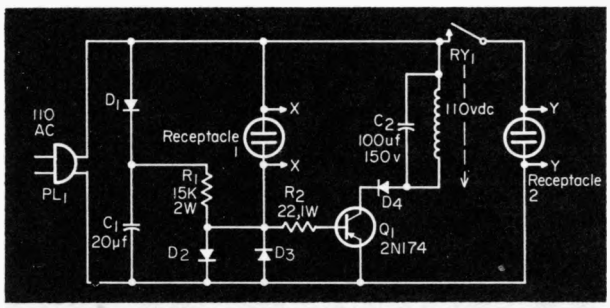
$$Z_0 = \frac{h_{ie}}{\beta_1 \beta_2} \frac{R_1}{R_1 + R_2}$$

where the parameters apply, of course, to the operating point, determined by R_3 (h_{ie} is the most nonlinear in this case).

AC Power Interlock

IF YOU START YOUR DAY turning on a lot of lab equipment, or if you would like to control many ac powered units from a central point, this circuit will make things easy.

Any unit plugged in receptacle 1, drawing anywhere from 5 w to the amount allowed by the D_2 — D_3 rating, will produce a 60 cps square wave at the base of Q_1 when the unit is turned on. Q_1 and D_4 will energize RY_1 on the negative cycles of the ac line, and C_2 will hold RY_1 in on positive cycles. Closure of RY_1 applies power to receptacle 2. Thus, the power switches of units in receptacle 1 control the power to units in receptacle 2 with no re-wiring. D_1, C_1 and R_1 produce positive bias across D_2, which holds Q_1 off when units in receptacle 1 are all off. The x-x and y-y points indicate additional receptacles, if needed.



AC power interlock.

In the circuit shown, the diodes have the following ratings:

$$D_1, D_4 : 0.5 \text{ amp}, 200 \text{ v}$$

$$D_2, D_3 : I = \frac{P_{max} \text{ (Recep 1)}}{130}, 50 \text{ v}$$

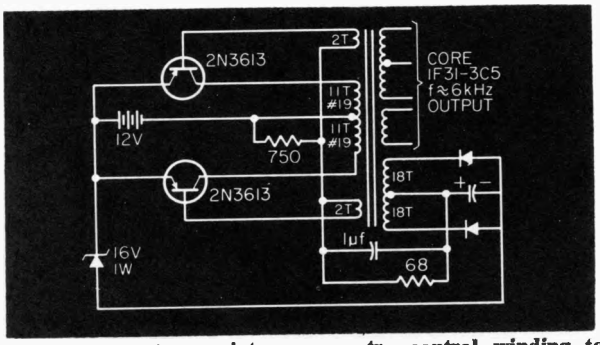
Combined Battery Converter-Regulator Power Source

IN BATTERY-POWERED INSTRUMENTS, regulators frequently are needed to allow for a wide range of battery voltages while converters are also needed to permit isolation of the equipment from the supply, and to provide the required operating voltages. This circuit combines both functions in

one stage, saving space and components. In the circuit shown, excess power is dissipated in two transistors instead of one series transistor, and operation at lower input voltages is possible due to the reduced voltage drop of only one transistor, V_{sat}.

The converter transformer is conventional except for the addition of the control winding. The dc voltage from this winding is compared with a reference voltage from a zener and the difference used to bias the converter transistors.

One such arrangement tolerated an input voltage of 11.5



Battery converter-regulator uses extra control winding to bias converter transistors.

to 19 V and gave an output of 15.5 to 16.5 V at an efficiency of 73 percent at the low input voltage.

Better regulation can be obtained by increasing the voltage of control winding and that of reference diode.

Backward-Diode Power-Supply Reference Elements

IN MANY APPLICATIONS a power supply is required which operates from a single unregulated supply of 6 v or less. Temperature-compensated zener diodes cannot be used as voltage reference elements since they are not available with

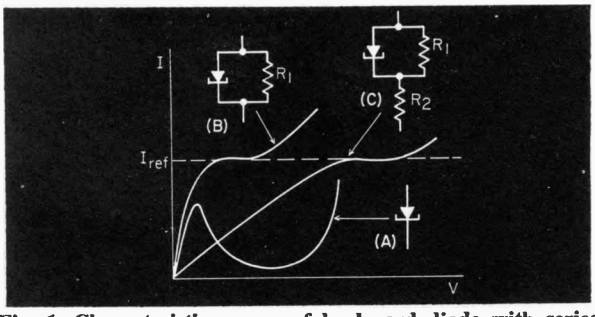


Fig. 1. Characteristic curves of backward diode with series and parallel resistors.

voltages below 6 v. Forward-biased diodes (e.g. stabistors) can be used for reference at low voltages, but their temperature coefficient (about —0.3%/°C) is too large for many applications. A combination backward-diode, resistor network can, however, be an efficient solution to the problem.

The V-I characteristic of a typical backward diode is shown in Fig. 1a. If a resistor, R_1, of the proper value is paralleled with the backward diode, the combination will approximate a constant-current characteristic over a range of about 100 mv (Fig. 1b). If another resistor, R_2, is connected in series, the voltage at which the constant-current region occurs can be increased (Fig. 1c).

A simple series-regulated power supply using the backward diode-resistance network as a reference is shown in Fig. 2. Transistor Q_1 serves as the series regulator and Q_2 serves as the error voltage amplifier in a manner similar to conventional supplies. Series resistor R_2 is selected so that the voltage at which the constant-current region occurs corresponds to the base-emitter voltage, V_{BE}, required by Q_2 at its nominal operating point. Resistor R_3 determines the output voltage according to the equation:

$$V_{out} = V_{BE} + I_{ref}\, R_3$$

Hence V_{out} can be adjusted to any desired value between V_{BE} and a value slightly below the minimum V_{in} simply by selecting the proper value of R_3.

Since the backward-diode, series-resistor network presents a very large impedance at the base of Q_2, any out-

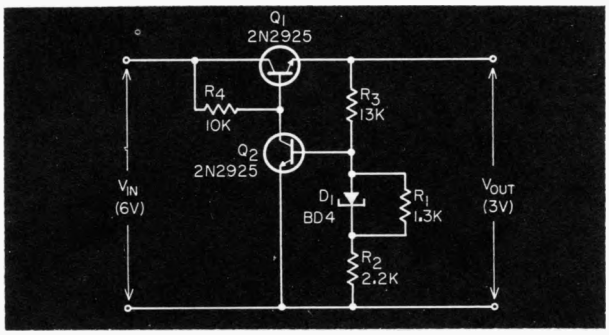


Fig. 2. Series regulated power supply with backward-diode reference.

put voltage changes are transmitted to Q_2's base without attenuation, as in a conventional supply where a voltage divider is used between the output and base of Q_2. This gives higher loop gain with a consequent improvement in voltage regulation, output impedance, and power efficiency. The use of a current reference rather than a voltage reference also results in improved flexibility since a wide range of current reference values is available.

The operating temperature range of the circuit is restricted since the base-emitter voltage of Q_2 must stay within the constant-current range for the regulation to be effective. The operating temperature range could be increased by using a resistor with a negative temperature coefficient for R_2. This would permit the voltage at which the constant current characteristic occurred to track the base-emitter voltage of Q_2.

In an actual power supply, as shown in Fig. 2, a germanium backward diode having a peak-point current of 100 μa was used in parallel with a resistor of 1.3 K. This combination exhibited a constant-current characteristic of 180 μa over a voltage range of 100 mv to 180 mv. Test results on the supply are shown below compared with a two-transistor supply using three series-connected silicon diodes as a reference.

	Tunnel Diode Reference	Silicon Diode Reference
Input Voltage	6 v ±10%	6 v ±10%
Output Voltage	3 v	3 v
Input Regulation ($\Delta V_{in}/\Delta_{out}$)	100:1	60:1
Output Impedance	0.4 ohm	20 ohms
Temperature Coefficient	0.04%/°C	—0.33%/°C

Second Breakdown Gives Fast Pulses

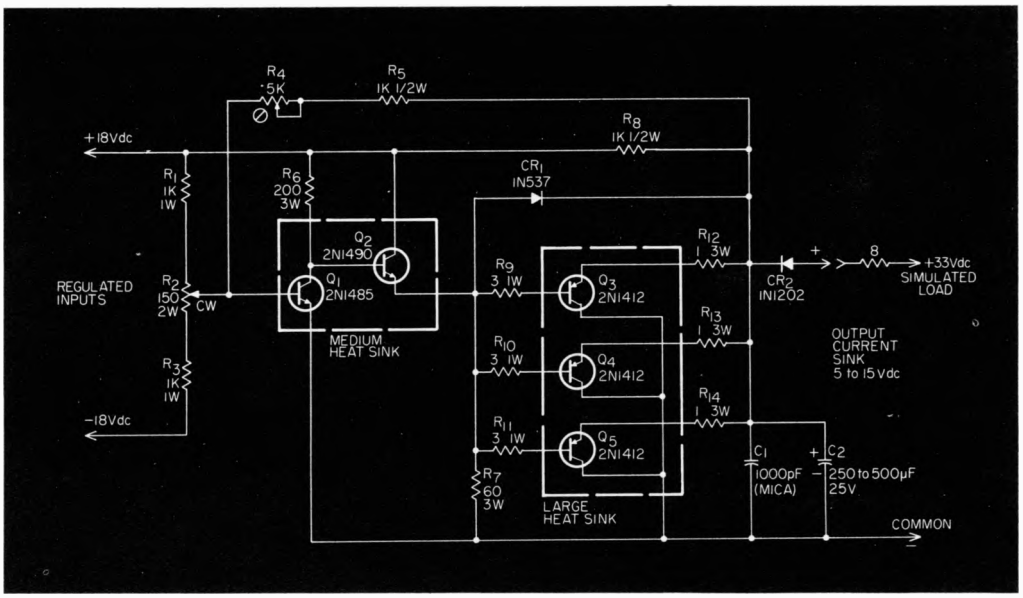
WHENEVER clamped logic circuits are used, the need arises for a power supply with "negative" output current, or, in other words, a constant-voltage sink. This is because, when several logic circuits are clamped simultaneously, the load actually becomes a generator.

The circuit shown here, gives any constant voltage from 5-15 Vdc and will sink up to 3 A of reverse current. The configuration is similar to a conventional shunt-regulated power supply except for the reversed load. Regulation is better than 2% for all voltages.

In the diagram, the sink is connected to +33 V via 8-ohms resistance. This simulates the maximum load condition. Diode CR_2 prevents current from being supplied in the event of an external short. It also prevents damage due to accidental reversal of the external connections.

The shunt-regulator transistors Q_3, Q_4 and Q_5, are derated to prevent loss of gain at high current levels. They are mounted on a common heat sink to distribute the temperature rise. Resistors R_9 thru R_{14} equalize the collector currents. Capacitors C_1 and C_2 prevent fast current changes from affecting the clamp voltage.

Resistor R_7 limits the drive current to the shunt transistors. Because Q_2 bypasses this drive current, the shunt transistors turn on when Q_2 is cut off. At this time the clamp voltage is low and the clamp current is high. As Q_2 is turned on, base drive to the shunt transistors decreases, thus increasing the clamp voltage and decreasing the clamp current.



Current sink absorbs 3-A reverse current. Clamping voltage is adjustable over the range 5-15 V.

Resistor R_6 supplies drive current to Q_2. Transistor Q_1 controls this drive current. Thus when Q_1 is off (R_2 wiper at bottom), Q_2 is fully on. As the arm of R_2 moves toward the positive line, Q_1 starts to turn on and Q_2 starts to turn off.

Resistor R_5 keeps the shunt-regulator transistors alive in the absence of load current. Diode CR_1 turns on the transistors if a short occurs across C_2.

Feedback from the load to the reference amplifier is via resistors R_3 and R_5. Feedback control R_4, is preset during alignment to give 16-V output with the load disconnected. This adjustment is made with R_2 in the extreme clockwise position.

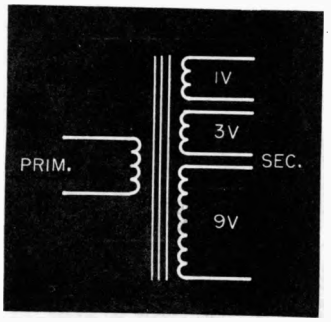
Universal Transformers

HERE IS A NOVEL way to obtain a wide variety of output voltages from a single transformer, using a minimum number of windings. The trick is to use a number of secondary windings giving output voltages in ratios of powers of three. Every voltage step from zero to the sum of the secondary voltages can then be obtained by switching the winding connections. The voltage increments will be determined by the smallest winding voltage.

The example shown in the figure has three secondaries of 1 V, 3 V, and 9 V. In this case, the smallest voltage obtainable is 1 V and the largest is 13 V. But it is also possible to obtain all the intermediate voltages in steps of 1 V. For example: 2 V is obtained by connecting the 3-V winding and the 1-V winding in series opposition; 3 V is obtained by using the 3-V winding alone; 4 V is obtained by connecting

OUTPUT VOLTS	1-VOLT WINDING	3-VOLT WINDING	9-VOLT WINDING
1	+	0	0
2	−	+	0
3	0	+	0
4	+	+	0
5	−	−	+
6	0	−	+
7	+	−	+
8	−	0	+
9	0	0	+
10	+	0	+
11	−	+	+
12	0	+	+
13	+	+	+

Connections for Transformer with Three Secondaries.



Windings required for transformer giving 1 to 13 V in 1 V steps.

the 3-V winding and the 1-V winding in series aiding; etc.

The table shows the possible connections for the transformer described in the example. "+" denotes a winding in phase with the required output, "—" denotes a winding in antiphase with the output, and "0" denotes a winding not used. Note that redundant windings, denoted by "0" in the table, are simultaneously available for driving a separate load if required.

There is a considerable difference in regulation for different output voltages. Winding impedances are always additive, regardless of phase. Thus a 13-V and a 5-V connection will both give the same secondary impedance, as both connections use all three windings. Note however that the percentage regulation will be different due to the different total voltages.

The technique described can be extended to any number of windings. Thus adding a fourth winding with a voltage of 3^3 or 27 V will give all voltages up to 40 V in steps of 1 V. The relationship is given by the equation

$$S = \sum_{x=0}^{(n-1)} 3^x$$

where S—number of steps, and n—number of secondary windings.

Precision full-wave rectifier uses only one op amp

OPERATIONAL AMPLIFIERS are now widely used in precision linear rectifiers to overcome the limitations of simple diode rectifiers. But, for a full-wave rectifier, most conventional circuits need at least two op amps. The circuit shown in Fig. 1 provides full-wave rectification with only one IC op amp, which is used simultaneously in two modes — as a linear amplifier and as a switch driver. Another feature of the circuit is that it uses only two precision resistors instead of the six normally required.[1]

The circuit operates as follows: Because $R_1 = R_2$, the voltage at point B is always equal in magnitude but 180 degrees out of phase with e_{in}, the input voltage. When e_{in} is positive, transistor switch Q_1 is closed and Q_2 is open. Under these conditions e_{in} is coupled directly to the output. When e_{in} is negative, switch Q_1 is open and Q_2 is closed, coupling the voltage at point B to the output. Since this voltage is an inverted version of the negative input, the output is again positive and full-wave rectification has been achieved.

To see the functions of the individual components, let's look at the circuit operation in more detail: Consider the case when e_{in} is positive. The current into R_1 will all flow into R_2, assuming an ideal op amp. Since $R_1 = R_2$, the voltage at point B will be $-e_{in}$, and the voltage V_A at point A will be $-(e_{in} + V_{CR3} + V_{CR4})$, where V_{CR3} and V_{CR4} are the voltage drops across zener diodes CR_3 and CR_4. Because one diode is biased in the reverse or zener direction and the other is biased in the forward direction, the potential at point A, using 1N4734 diodes (with a nominal 5.6-volt zener voltage), is:

$$V_A = -(e_{in} + 6.1)$$
$$= -(e_{in} + 0.5 + 5.6) \quad (1)$$

Though e_{in} may be very small, it is sufficient to turn off transistor Q_2 via forward-biased diode CR_2, leaving a high-impedance path between point B and the output.

Transistor Q_1 is connected to point A through CR_1, but no voltage is transferred to the gate of Q_1 since CR_1 is biased off. The gate and source of Q_1 are therefore at the same potential. This is the condition for minimum source-to-drain channel resistance in a FET. The input voltage e_{in} is therefore coupled directly to the output.

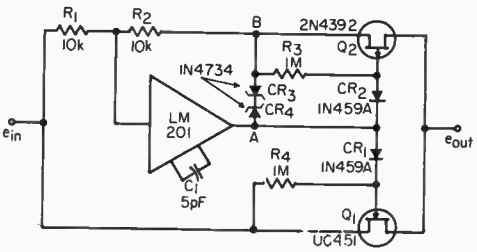


Fig. 1. Unusual linear full-wave rectifier uses fewer expensive components than other circuits having equal performance.

When e_{in} is negative, similar conditions apply, but with opposite polarities so that Q_1 is off and Q_2 is on.

So, the voltage at point B is always linearly related to that at the input. Also, a nonlinear switching voltage, having the desired polarity at the correct time, is available at point A.

The diodes merely switch noncritical voltages; the only requirement is that the zener voltage must exceed the pinch-off voltage of the FET. The FET switches, in the signal paths, act as low value pure resistances, with no offsets.

The circuit gives excellent results up to a few kilohertz. Fig. 2 shows a typical error plot. For higher frequency operation, the FETs could be replaced with MOSFETs to take advantage of their superior high-speed switching characteristics. Also, the LM201 could be replaced by a higher bandwidth op amp.

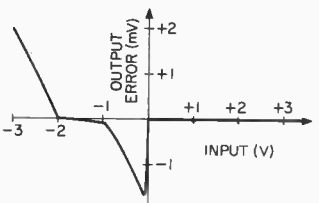


Fig. 2. Maximum error over a ±3 V input range is less than ±2 mV (±0.066% of full scale).

Reference

1. "Full Wave Rectifier," *Handbook of Operational Amplifier Applications*, Burr-Brown Research Corp., p. 73.

Section 15
DETECTION & SENSING CIRCUITS

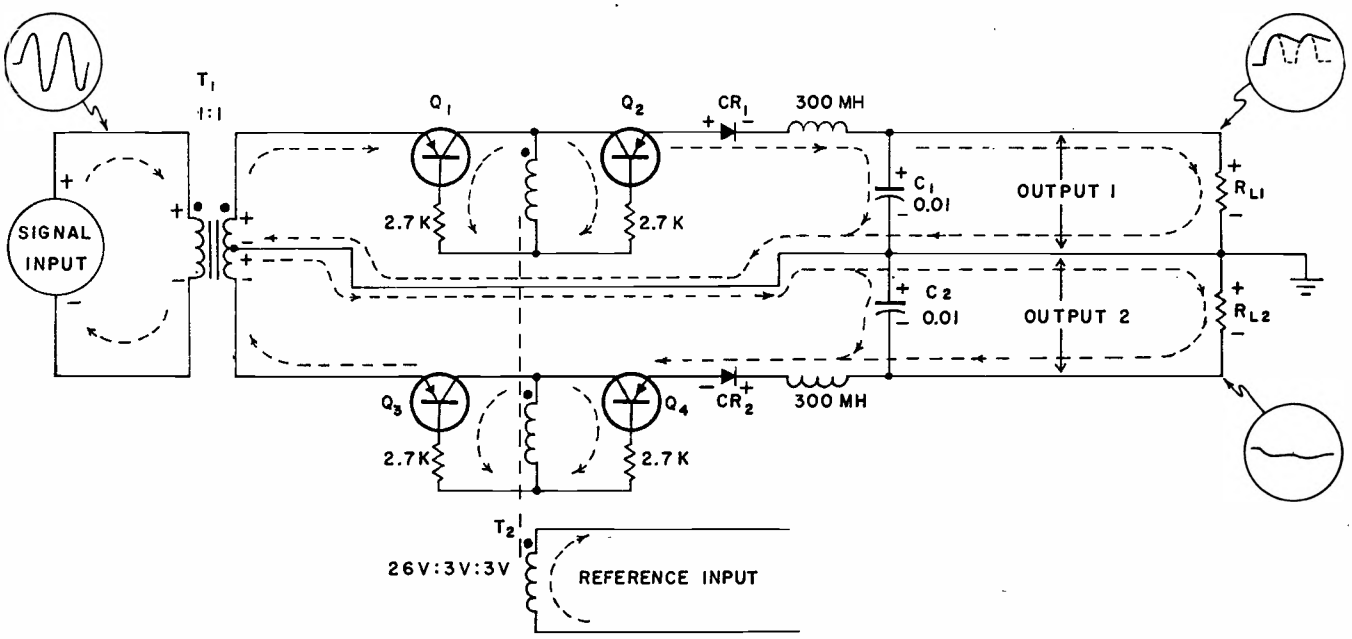
In-Phase, Out-Of-Phase Sensor

HERE is a circuit that I wish I could have developed many years ago. This in-phase, out-of-phase sensor is extremely useful. One application is the determination of the phase of an output signal that has gone through several transformers. Many transformers do not have phase markings and one can not be sure whether the output signal, using these transformers, is in phase or 180 degrees out of phase. This phase sensor will determine phase relationships of this nature.

The circuit operation is as follows. Transistors Q_1,Q_2,Q_3 and Q_4 are connected to the secondaries of reference transformer T_2 so that, during one half cycle of the reference signal, they are all biased to pass current and during the remaining half cycle of the reference signal they are all biased to cut off. Notice the dots on the primary and the secondaries of transformer T_2.

Assume that, during the half cycle of the reference signal when the transistors are biased to pass current, an in-phase input signal is polarized to cause conventional current flow in the primary of transformer T_1 as shown in the diagram. If, then, the phase relationship of transformer T_1 is arranged as indicated by the dots in the diagram, conventional current flow in the remainder of the circuit will be as indicated by the dotted lines.

Notice that diode CR_1 is forward biased, while diode CR_2 is reverse biased. This is the key to the



The phase sensor circuit employs Motorola 2N651A transistors. All diodes are IN645A.

circuit operation. Since diode CR_1 is forward biased, the half-wave rectified signal that passes through transistors Q_1 and Q_2 is filtered and mostly dropped across the load RL_1.

On the other hand, since diode CR_2 is reverse biased, the half-wave rectified signal that passes through transistors Q_3 and Q_4 is dropped mostly across diode CR_2 before it is filtered. The slight amount that remains is barely detectable across the load RL_2.

In the circuit that was constructed in the lab, the loads were 1000-ohm resistors and the input and reference signals were 20-volt peak to peak sine wave signals at a frequency of 6.4 kilocycles. The output signal developed across the in phase load, RL_1, was 4.4 volts peak. The output signal developed across the out of phase load, RL_2, was barely detectable.

When the input signal is 180 degrees out of phase with the reference signal, the larger half-wave rectified filtered signal will be developed across the out of phase load RL_2.

High-Speed Threshold Device

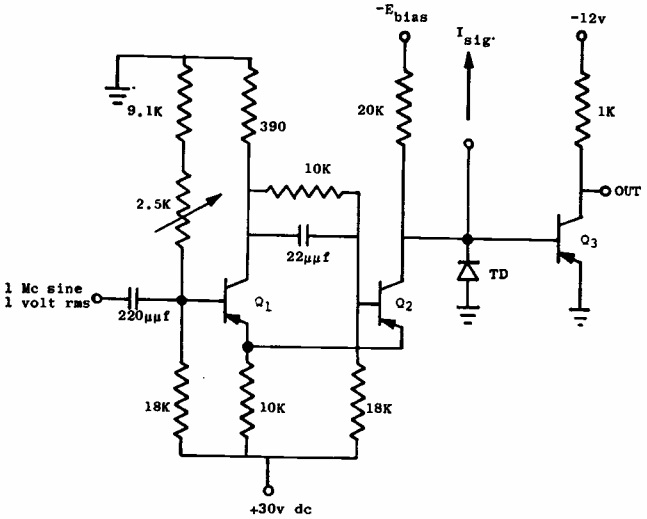


FIG. 1—The three transistors are type 2N384 and tunnel diode TD is a 1N2939 (1-ma peak).

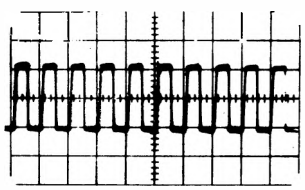


FIG. 2—Output when input is always above the threshold. The horizontal scale is 1 μsec/div.

A TUNNEL DIODE, biased in its switching mode, is being used as a current threshold device. It is fast (0.02 μsec rise time) and puts out a constant amplitude pulse when the threshold value is exceeded. The signal current is analog video information and is sampled every microsecond. If the signal is above the threshold when it is sampled, a 0.5-μsec pulse is generated.

In Fig. 1, transistors Q_1 and Q_2 are used in a circuit that has characteristics of both a current mode logic switch and of a Schmitt trigger circuit. If the 390-ohm resistor in the collector circuit of Q_1 were shorted out, the base of Q_2 would be at fixed potential and a 1-volt rms sine waveform at the base of Q_1 would cause the 2-ma emitter current to be switched back and forth into the two collector circuits. With the resistor in the circuit, the potential at the base of Q_2 varies with the collector current of Q_1 in a manner to speed the switching action.

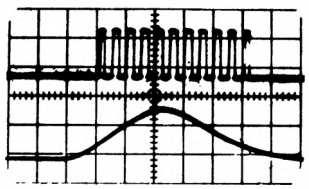


FIG. 3—Output (at top) for the input shown at bottom Scale is 2 μsec/div.

The circuit is now in the configuration of a Schmitt trigger in which saturation is prevented by using the small collector resistor. Thus, drift transistors may be used and biased properly to achieve high-speed operation.

When the emitter current is switched into the collector circuit of Q_2, a small positive voltage appears at the negative terminal of the diode (holding Q_3 off) and current flows into that terminal. When the emitter current is switched back to the other transistor a current flows out of the negative terminal of the diode whose magnitude is

$$E_{bias}/20K + I_{in}$$

If this current exceeds 1 ma, the tunnel diode switches to its high-voltage state and turns transistor Q_3 on. If the current is less than 1 ma the tunnel diode stays in its low-voltage state and holds Q_3 off. The potentiometer is used to set the discrimination level of the Schmitt trigger and hence the fraction of the 1 μsec period in which the tunnel diode is reset.

Figure 2 shows the output that results when no signal current is present and the bias current is greater than the threshold current of the tunnel diode. If the bias current were less than the threshold current, there would be no pulse output.

The upper waveform in Fig. 3 is the output that results from an input shown in the lower portion of the figure. The bias current is set so that the circuit triggers at some fraction of the signal current maximum amplitude. A reliable threshold is obtained because the value of the peak current of the tunnel diode is considerably more stable than most semiconductor parameters.

The threshold may be varied electrically by controlling E_{bias}, possibly with some feedback function.

Large Slope Frequency Discriminator for Low Frequencies

ABILITY of a frequency discriminator to perform in a satisfactory manner can be thought of as a function of the overall Q of the circuit. For high Q's the discrimination would also be of a high degree. One of the problems in low-frequency discrimination is obtaining a Q high enough to yield the desired response characteristic, such as that shown in Fig. 1. The circuit used to obtain this response is shown in Fig. 2.

This problem is approached here from the standpoint of utilizing high Q coils and capacitors in conjunction with amplifiers for the purpose of gaining the benefit of the gain-bandwith product. The idea in many cases is to obtain a large dc output for a small shift away from the center frequency of the discriminator. The intuitive conclusion is to obtain as much attenuation rate as is required from each amplifier to produce the degree of discrimination desired. (Individual slopes contribute in direction proportional to the final output slope). This effect can be readily achieved by the use of high Q amplifiers. A brief explanation of the operation of the circuit is as follows: consider a frequency below that of f_c entering the discriminator; the amplifier tuned to a frequency f_1 below f_c will exhibit an output much greater than the output of the amplifier tuned to some frequency f_2 above f_c; hence, the outputs of the reversed diodes will differ by an

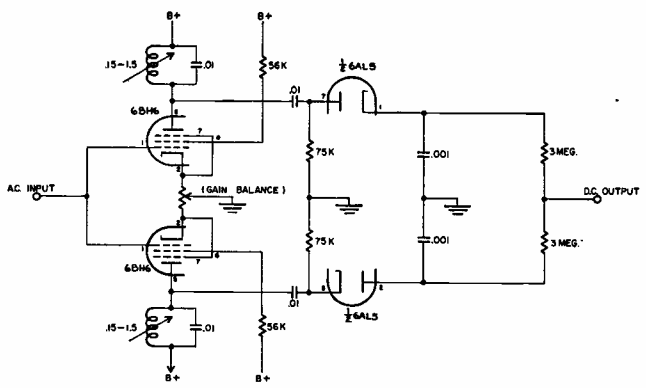


FIG. 2—Circuit of low frequency discriminator.

amount equally as great. These voltages are smoothed and added resistively thereby producing a dc output that is directly proportional to the difference in the input frequency and f_c. The maximum slope that has been obtained to date is 0.15 volt per cycle at 1.5 kc. This is by no means an upper limit. Such a limit would exist only in the ability of the designer to obtain higher Q's by means of higher μ tubes and proper design of the amplifiers with higher Q coils and capacitors; it might be added

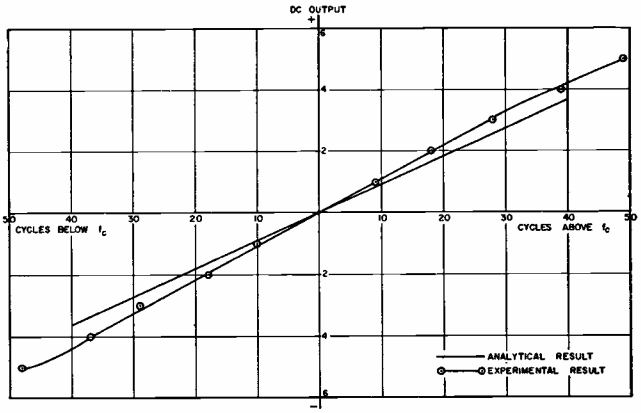


FIG. 1—Discriminator response characteristic.

that the separation of f_1 and f_2 is limited by the individual Q's.

The detailed mathematical treatment of this circuit would be of considerable interest but for practical applications all that is needed is a knowledge of the band of frequencies of interest, the desired output slope and a design equation.

The method of deriving a useful design equation was to approximate the response curves of the amplifiers by two isosceles triangles. The region of interest lies between f_1 and f_2 so that we have the simplest of problems with which to work—two straight lines. The resulting equation is

$$e_o = KK' e_{\Delta f} 2 (f - f_c) \text{ where } f_c = \frac{f_1 + f_2}{2}$$

where

K = attenuation rate of amplifier (assuming $K_1 = K_2$ for both)

K' = loss factor encountered from the amplifier's ac output to the dc output

If the loss through the diode is about ½ and the loss due to resistive addition is 1/3, then $K' = 1/6$, which was the case here.

The slope of the discriminator curve varies in

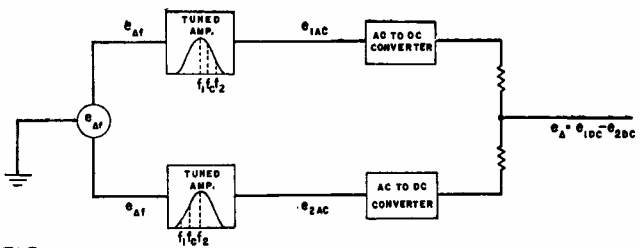


FIG. 3—Analysis of discriminator circuit.

direct proportion to the level of the input voltage, $e_{\Delta f}$. This could prove to be detrimental in some cases but at the same time this fact may be put to use for the purpose of increasing the slope without having to make any actual circuit changes.

The following is a simple treatment of the circuit response. The design equations are provided.

Consider the generalized diagram of discrim-

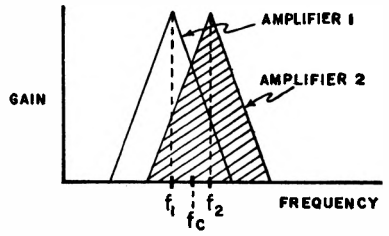


FIG. 4 — Approximation of response curves.

inator given in Fig. 3. Assuming equal gains and attenuation rates in the interval $f_1 \leqslant f_c \leqslant f_2$, a close approximation to the response curves, as shown in Fig. 4, can be obtained.

If only the area under the two response curves bounded by f_1 and f_2 is considered the following treatment may be applied with the introduction of little error:

x_4, y_4 $\quad x_2, y_2$ $\quad\quad$ $\dfrac{y_{(1)}-y_1}{x_{(1)}-x_1}=\dfrac{y_2-y_1}{x_2-x_1}$

x_1, y_1 $\quad x_3, y_3$ $\quad\quad$ $\dfrac{y_{(2)}-y_3}{x_{(2)}-x_3}=\dfrac{y_4-y_3}{x_4-x_3}$

$$y_{(1)}=\frac{y_2-y_1}{x_2-x_1}(x_{(1)}-x_1)+y_1 \qquad y_{(2)}=\frac{y_4-y_3}{x_4-x_3}(x_{(2)}-x_3)+y_3$$

Substituting the following

$$y_{(1)}=G_1 \quad y_{(2)}=G_2; \qquad G_{max}=y_4=y_2; \qquad G_{min}=y_1=y_3$$

$$f_1=x_1=x_4 \quad f_2=x_3=x_2 \quad x_{(1)}=f=x_{(2)}$$

$$G_1=\frac{G_{max}-G_{min}}{f_2-f_1}(f-f_1)+G_{min}$$

$$G_2=\frac{G_{max}-G_{min}}{f_1-f_2}(f-f_2)+G_{min}$$

Subtracting

$$G_1-G_2=\frac{G_{max}-G_{min}}{f_2-f_1}(f-f_1)-(f_2-f)$$

$$=K \qquad 2f-(f_1+f_2)$$

$$G_1=\frac{e_1}{e_{\Delta f}} \qquad G_2=\frac{e_2}{e_{\Delta f}} \qquad G_1-G_2=\frac{e_1-e_2}{e_{\Delta f}}$$

which yields

$$e_o = KK' e_{\Delta f} 2(f-f_c)$$

Photo Diode Pickoff Gives Accurate Angular Reference

THE MEASUREMENT of servo system lag often delineates a requirement for an accurate angular reference. The system described has an accuracy of 0.17 degree in either cw or ccw rotation.

A slot (0.005 x 0.1875 in.) is milled near the periphery of a 5½ in. diameter disc. A synchro control transmitter B_1 and the disc are rotated by motor B_2. The disc (Fig. 1) rotates between the photo diode CR_1 and the light source DS_1 while the light beam is restricted by a shield in which is milled a 0.005 x 0.1875 in. slot.

The photo diode senses the change in light and produces a positive pulse (Fig. 2). This pulse is then fed to an emitter follower Q_1 which transfers the pulse to the Schmitt Trigger circuit Q_2 and Q_3. By adjusting the threshold control R, the trip point of the Schmitt Trigger may be set near the peak of the input pulse and the optical response error becomes insignificant (less than 0.02%).

Accuracy is primarily dependent upon the rotational radius of the slot in the disc and the backlash of the gears. A 2-½ in. rotation slot radius has a circumference of 15.7 in. Thus, the combination of a 0.005 in. light beam and the 0.005 in. slot in the disc represents a maximum response error of 0.115 degrees. Using Precision 1 gears and maintaining a 0.001 in. center distance difference between mountings, the backlash is held at 0.17 degrees or less. Therefore, the maximum total error is the backlash, 0.17 degrees, plus 0.115/2 degrees, (maximum optical response error) either direction of rotation, or 0.222 degrees.

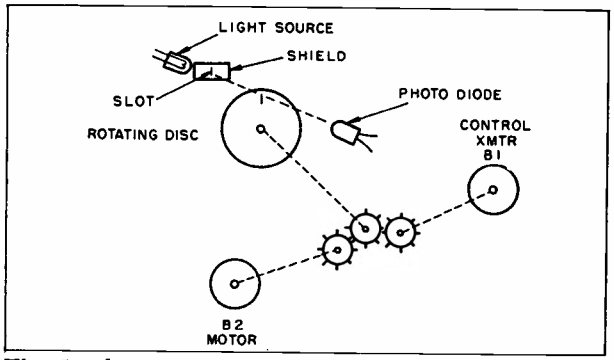


Fig. 1—Photo-Diode Pickoff.

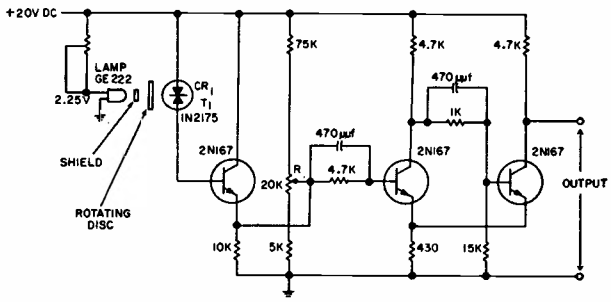


Fig. 2—Circuit Incorporating Photo-Diode Pickoff

Video Switch for Radar

THE OVERALL function of a video switch is to either pass or blank out video signals going to a ppi visual display.

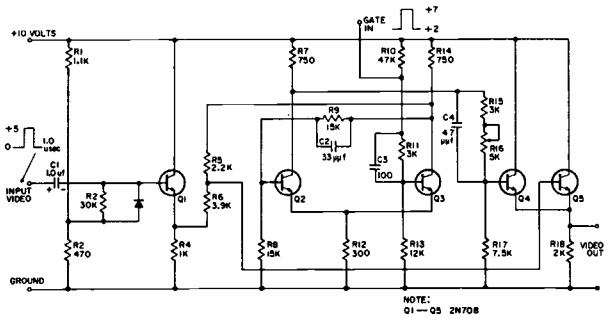
After the video pulses have gone through examinations in other system equipment, a blanking gate input pulse is applied to the switch if the video fails to identify itself as the signal from the associated radar set. If the blanking gate is present, no video output appears on the visual display. The switch is transient free, hence, no false video indications appear on the display.

Resistors R_1 and R_2 form a voltage divider, which

sets the operating point for Q_1. The video pulse is coupled to an adder circuit formed by R_5 and R_6 through emitter follower Q_1. When the video output pulse of the adder circuit is applied to the base of Q_5 with no input gate applied to Q_2 and Q_3 the video output is coupled through emitter follower Q_5 and R_{18} to the video output terminals.

With no gate input to the junction of R_{10} and R_{11}, Q_3 remains in a nonconducting state, while Q_2 conducts. The voltage divider formed by R_{15}, R_{16} and R_{17} is such that the voltage at the junction of R_{16} and R_{17} keeps Q_4 in a nonconducting state. The collector of Q_3 is at approximately 10 v, thereby maintaining the dc level of the output of the adder high enough to keep Q_5 in a conducting state. The video output is developed across emitter resistor R_{18}.

A positive gate input pulse rising from approximately 2 to 7 v at the junction of R_{10} and R_{11} will change the operating states of Q_3 and Q_2 and, by the same



Video switch passes or blanks out video signals going to a ppi visual display.

voltage divider technique, keep Q_5 in a nonconducting state for the duration of the gate input. Under these conditions no video output pulse will exist.

The input video pulse used was 5 v in amplitude, and the attenuation ratio between input and the video output is 2:1.

Sampling Circuit

THE SAMPLING CIRCUIT shown in Fig. 1 and in block diagram form in Fig. 2 was designed to pick out desired periodic information and to eliminate noise and other unwanted voltages which appeared.

By combining two cathode coupled monostable multivibrators which generate pulses whose widths are approximately equal to RC (R_1C_1 in the first monostable multivibrator and R_2C_2 in the second monostable multivibrator) and which are also linear functions of the dc bias voltage at the grids of the normally cut off tubes (tube V_1 of the first monostable multivibrator and V_3 of the second monostable multivibrator), a very versatile circuit can be designed simply by picking $T = RC$ approximately equal to the width of desired pulse and then adjusting their size using potentiometers P_1 and P_2 to fit each particular case. In this way, the control

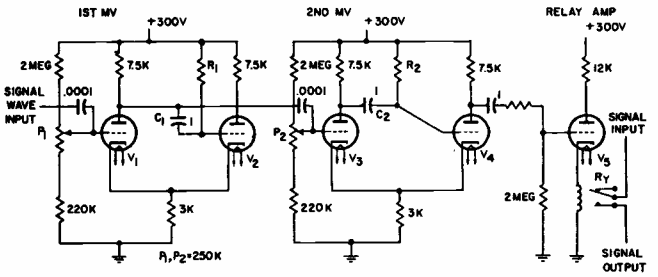


FIG. 1—Sampling circuit using two cathode-coupled multivibrators.

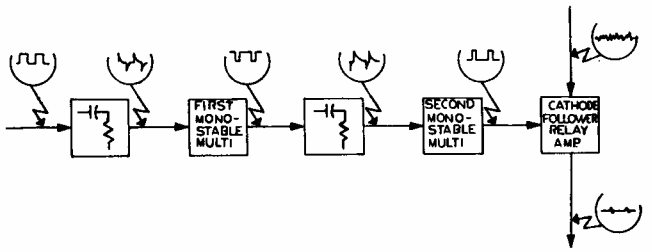


FIG. 2—Block diagram of sampling circuit.

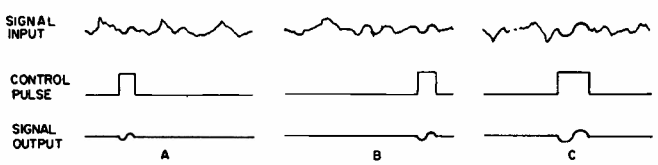


FIG. 3—A narrow-width signal appearing at the beginning of the cycle is shown at (A). A medium-width signal appearing near the end of the cycle is shown at (B) and a very wide signal appearing near center of the cycle is shown at (C).

pulse at the output of tube V_4 can be made any desired width and placed at any point within the cycle. (Fig. 3.)

With this circuit and a dual trace scope, it is a simple matter to position the control pulse so that only the information of interest is allowed to pass through the sampling circuit.

In Fig. 3, one application is shown where this circuit was used to pick out a sine shaped curve which appeared periodically at random positions amid various other voltages which completely obscured it.

The circuit shown in Fig. 1 was used with pulses whose frequencies were low enough so that it was possible to use a relay. At higher frequencies, a diode gate was used.

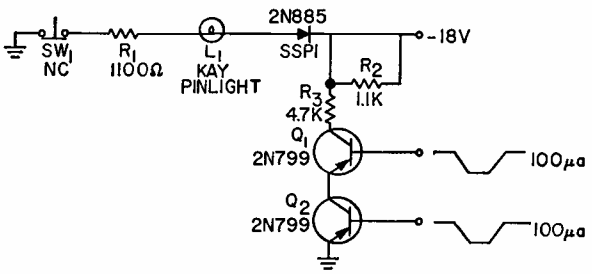
Pulse Coincidence Detector

THIS CIRCUIT will show coincidence of any two pulses that are 100 microamperes in amplitude and that coincide for at least 1 microsecond.

Coincident pulses applied to Q_1 and Q_2 will trigger

the silicon controlled rectifier. Its anode current gives a visual indication of pulse coincidence (turn on L_1). The normally closed switch (SW_1), returns the scr to a non-conducting state and turns the light off.

The circuit shown was used to show the occurence



Pulse coincidence detector.

of coincident outputs from the last stages of two magnetic-core/diode-type counters. Q_1 and Q_2 were driven by windings on the cores of the last stages of the counters.

Pulse Absence Detector

THIS CIRCUIT not only detects the presence or absence of a pulse train, but it is able to indicate whether the level remains positive or negative after cessation of pulsing.

When a pulsed signal which has dc levels of ±3v is received, the signal is rectified by the voltage doubler and filter arrangement consisting of C_1, C_2, Cr_1, and Cr_2. This voltage is more negative than −4.5 v and serves to cut off transistor Q_1. Transistor Q_2 then saturates, with base current being supplied by R_2. On negative half cycles, Q_3 is pulsed with base current through R_3. The pulse of Q_3 collector current is absorbed by Q_2, and the collectors of Q_2 and Q_3 remain at near-ground potential. On positive half cycles, Q_3 is cut off, which tends to cause its collector to go more negative. Under these conditions, the collector and emitter of Q_2 interchange functions, and it becomes an emitter follower. This tends to cause the collector of Q_3 to go positive, which, in turn, causes Q_2 to function in its original manner. The collector of Q_3 is thereby clamped to ground for the duration of the input signal.

If the signal stops (and remains) at its positive (+3v) level, Q_1 saturates with base current through R_1, causing the base of Q_2 to drop toward −4.5 v, cutting off Q_2. The positive level also cuts off Q_3, and the collector of Q_3 becomes negative. Q_4 and Q_6 conduct under these conditions, allowing M, the permanent magnet dc motor, to run.

If the signal stops in its negative state, Q_1 is again turned on, and Q_2 is turned off. Q_3 is turned on, causing the collector voltage of Q_3 to go positive. This allows conduction of Q_5 and Q_7, making the motor run in the opposite direction.

Transistors Q_6 and Q_7 have limit switches LS_1 and LS_2 in their respective base circuits to limit travel when the motor is arranged to drive an actuator over a limited distance.

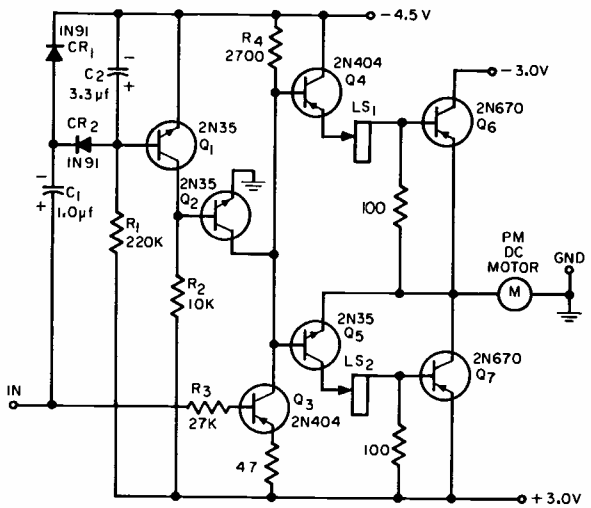


Fig. 1. Pulse absence detector and actuator amplifier.

FM and PDM information can be derived from the signal in other detectors, but this information is not available when the signal stops in one of its dc states.

Pulse and DC Monitor Circuit

DESCRIBED IS A CIRCUIT to perform the three detection-monitoring functions shown in Fig. 1. These functions might arise when it is desired to indicate presence of a continuous train of pulses, absence of one or more pulses in a train, or to monitor a dc voltage.

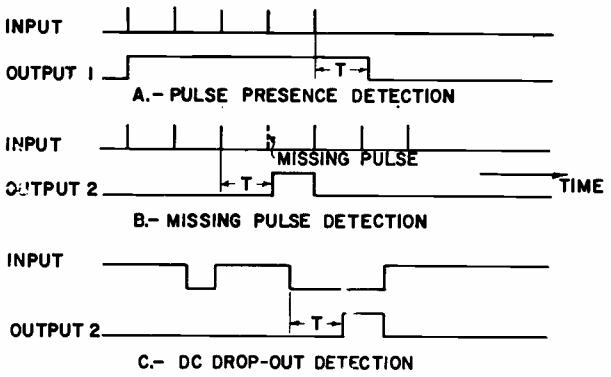


FIG. 1—Functions to be performed.

The circuit to perform these functions is the controlled monostable multivibrator shown in Fig. 2. For every pulse at the input, Q_3 turns on, bringing point (A) to −30 v. This holds Q_1 off, so output *1* is high, and output *2* is low. When the elapsed time since the last pulse arrived exceeds the preset limit T determined by R_1 C_1, C_1 charges through R_1 until (A) is at about +1 v, turning Q_1 on and Q_2 off. Output *1* is now low, and output *2* is high. Thus, functions (a) and (b) of Fig. 1 have been accomplished.

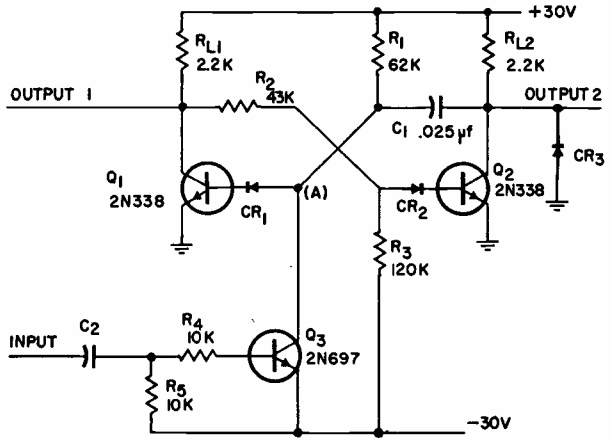


FIG. 3—Circuit that performs functions of FIG. 1.

With dc inputs, C_2 is by-passed. When the input is high, Q_3 is on, Q_1 is off, Q_2 is on, and output 2 is low. If the input drops to a low value for a time greater than the limit T set by R_1 C_1, Q_1 turns on, Q_2 off, and output 2 is high. Thus, function (c) of Fig. 1 is accomplished.

Diode CR_3 permits rapid charging of C_1 when (A) is brought to −30 v. CR_1 and CR_2 prevent the reverse base-emitter voltage of Q_1 and Q_2 from being exceeded.

A working set of component values is included in Fig. 2. The value of T is given approximately by 0.69 R_1 C_1, or 1.07 msec.

Absolute-Value Phase Comparator

A RELIABLE, inexpensive circuit was required that would indicate, with a dc output voltage, the phase relationship of two equal-frequency sine waves, without regard to the polarity of the phase relationship. The dc output voltage was to be maximum when the sine waves were in phase, zero at 180-degree phase difference, and vary linearly with phase for intermediate phase angles.

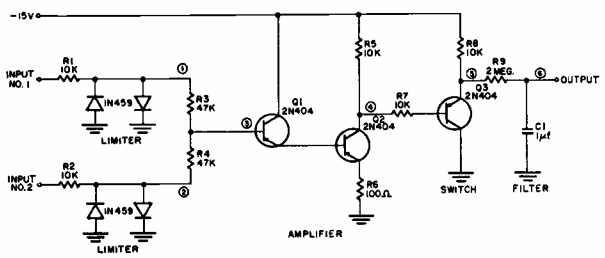


Fig. 1. Phase comparator circuit.

The circuit is shown in Fig. 1. Waveforms at various points are shown in Fig. 2.

Amplitude fluctuations in the input signals are removed by the diode limiters, resulting in equal-amplitude square waves at points 1 and 2. The sum of these waveforms, appearing at point 3, is a series of positive and negative pulses whose width depends on the phase relationship of the square waves. Transistors Q1 and Q2 form an amplifier biased at cutoff. The negative pulses at point 3 drive this amplifier from cut-off to saturation, resulting in positive-going pulses, with a −7.5-volt baseline, at point 4. Q3 is a normally-on switch, grounding point 5. The positive-going pulses at point 4 turn Q3 off. This switches the full power-supply voltage into an output filter composed of R_9 and C_1. The filter will have an output dc voltage proportional to the average voltage at point 5. This, in turn, is equal to the duty cycle of the waveform at point 5, multiplied by the peak amplitude of the pulses at that point. The duty cycle will be one-half if the inputs are in-phase, and zero if they are 180 degrees out of phase. A plot of the measured output voltage versus the input relationship is shown in Fig. 3.

The circuit operates from 20 cps to at least 200 kc, and is insensitive to amplitude fluctuations of the input signals as long as they are above a level of 0.75 volts rms.

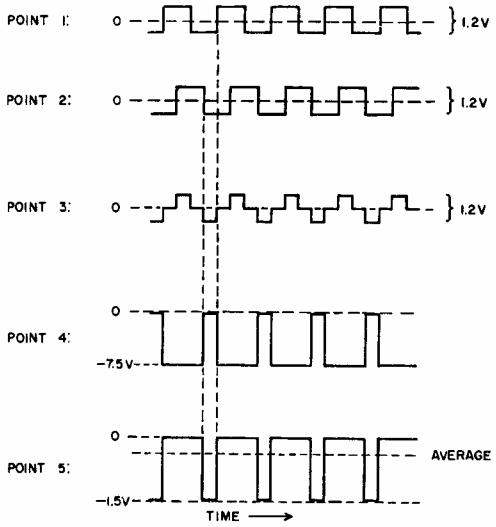


Fig. 2. Waveforms in phase comparator.

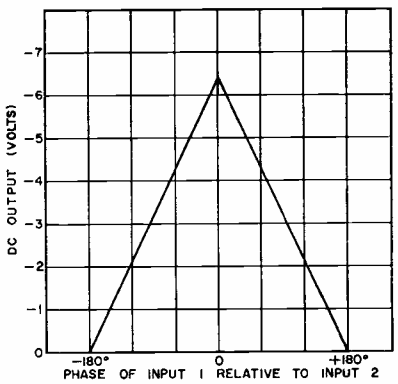


Fig. 3. Output characteristic of phase comparator.

The circuit has a very stable single-ended output. Neither the transistor types nor the component values are critical. No adjustments are required. The circuit is particularly useful if the inputs are corrupted by noise. In this case, the ouput depends only on the phase relationship and the signal-to-noise ratio. It is independent of the absolute levels of signal and noise.

Pulse Detection Circuit

THE CIRCUIT described here provides an output at one voltage level when there are no pulses at the input, and at another level when pulses are present. The presence and absence of pulses is thus converted into bistable or on-off information. This information can be used to operate a relay, light, or initiate action in other circuitry upon arrival or departure of pulses.

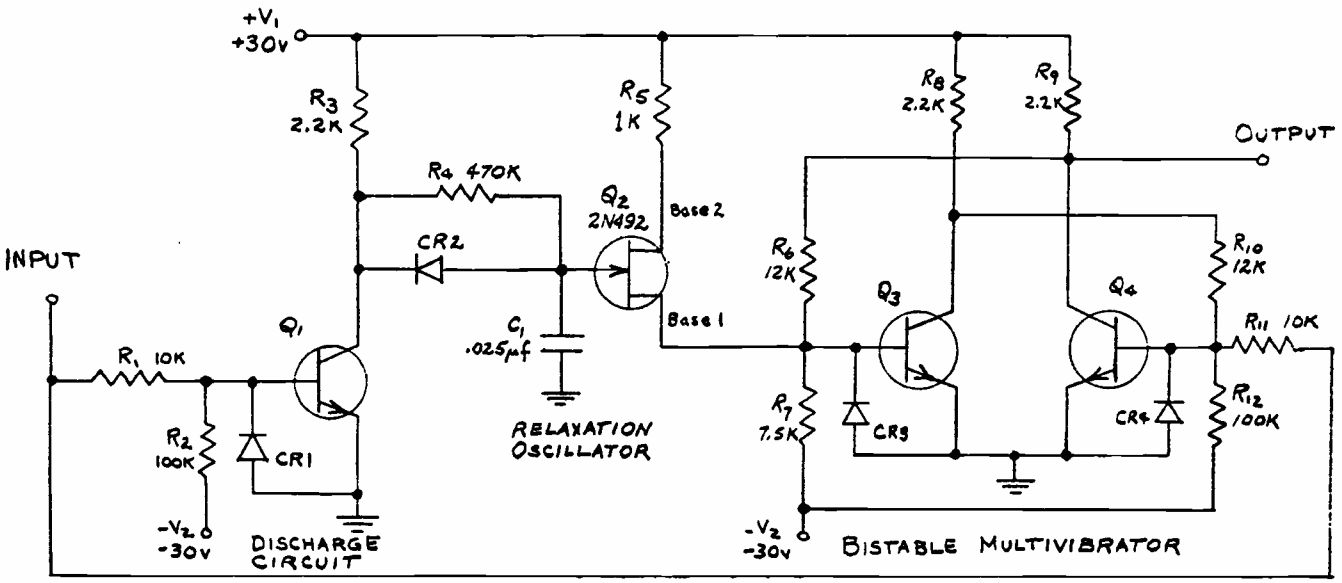
The circuits will work well with narrow pulse inputs and wide pulse separations are readily accommodated. The output will change state when the first pulse arrives, and will go back to its first state as soon as one pulse is missed. This suggests that the circuit could be used as a missing pulse detector. The circuit is also relatively insensitive to pulse amplitudes.

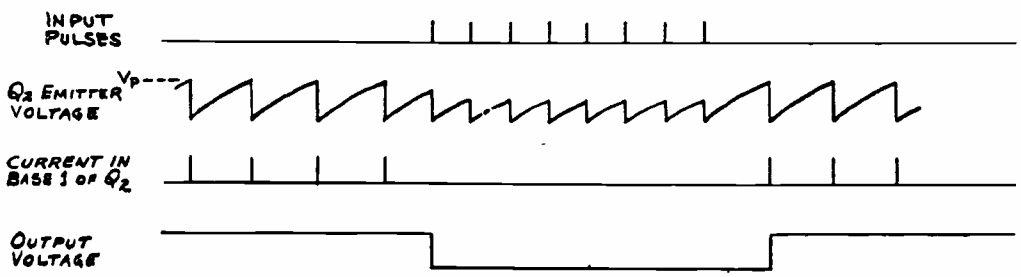
As shown in the circuit diagram, transistors Q_3 and Q_4 are in a bistable multivibrator circuit, Q_2 is a unijunction transistor in a relaxation oscillator circuit. Circuit operation is as follows. With no pulses at the input, Q_1 will be off, allowing capacitor C_1 to charge through R_3 and R_4. When the voltage on C_1 reaches V_P (the peak emitter voltage of Q_2), the emitter-to-base-1 resistance of Q_2 becomes negative, and C_1 rapidly discharges. This causes a large pulse of current to flow in the base-1 lead of Q_2, which turns on Q_3. This, in turn, turns off Q_4. When C_1 is discharged, the characteristic of Q_2 is such that it turns off. This means that C_1 can again charge through R_3 and R_4. If no pulses arrive at the input, C_1 will charge to V_P, and Q_2 will again send a pulse of current to the base of Q_3. However, there will not be a change of the multivibrator state, since Q_3 is already on. Therefore, with no pulses at the input, Q_4 will be off, and the output will be at a high voltage level.

A pulse arriving at the input will turn on Q_4, which forces Q_3 to be off. Transistor Q_1 will also be turned on by the pulse, and C_1 will discharge through CR_2 and Q_1. Later pulses will again turn on Q_1, so that the voltage on C_1 will not reach V_P. Therefore Q_2 will not turn on, which means that Q_3 will remain off and Q_4 will be on. Thus, with pulses present, the output will be at a low voltage level.

If a pulse is now missed, C_1 will charge to V_P, Q_2 will turn on, and the output will return to its high voltage level.

Current in base 1 of Q_2 when it is "off" must be taken into account when setting up the bias for Q_3. The value of this current can be found from the static interbase characteristic of the unijunction transistor, and will be about 3 ma for the 2N492. The following condition must be satisfied: $3K \leqslant R_3 + R_4 \leqslant 500K$.[1] These limits insure that the





Pulse detection uses unijunction transistor as relaxation oscillator.

emitter load line for Q_2 will intersect the emitter characteristic in the negative resistance region. If the input pulses are narrow, C_1 should be small and Q_1 should be a high-speed transistor with low saturation resistance, in order that the narrow pulses can discharge C_1. At the same time, the time constant $(R_3 + R_4)\ C_1$ must be large enough so that the voltage on C_1 does not reach V_P between pulses, Diodes CR_1, CR_3 and CR_4 keep the reverse base-emitter voltage rating of Q_1, Q_3 and Q_4 from being exceed. CR_2 permits rapid discharge of C_1.

Speed-up capacitors across R_1, R_6, R_{10} and R_{11} may be used if required.

A set of component values that were used to detect pulses with a period of 5000 μsec is shown in the figure. Shown also are the waveforms at several points in the circuit.

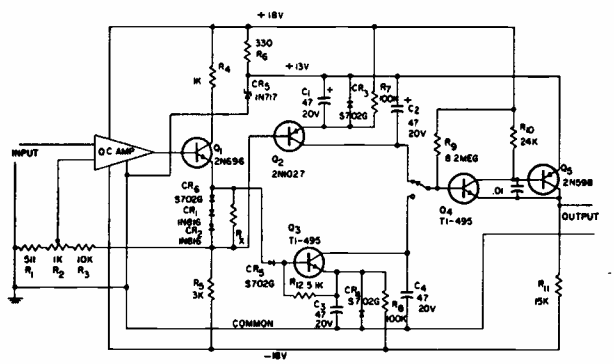
Peak Follower

THE PEAK FOLLOWER to be described accepts an ac input with a dc component and it provides two outputs proportional to the positive and negative peak amplitudes of the ac component. It features extremely long time constants while maintaining fast response to both increasing and decreasing peak amplitudes. Although the circuit shown accepts only signals which are positive with respect to the zero axis, it can be simply modified for positive and negative inputs, with or without a dc component.

The circuit provides very small droop between cycles (except for a small reset pulse at the beginning of each cycle). Its fast response enables it to follow cycle by cycle variations. When the input is removed, the output will fall to zero after a few cycles. Good linearity is obtained from low inputs to full scale.

The peak following action is obtained by Q_2, Q_3, which has Q_1 as an output stage and the feedback network R_1, R_2 and R_3 to stabilize and adjust the gain. The amplifier has a zero adjustment incorporated.

The peak following action is obtained by Q_2, Q_3, and associated components. The pnp transistor Q_2 follows the negative peaks while the npn Q_3 follows the positive peaks. The operation of both is similar so only the Q_2 stage will be described.



Peak follower circuit provides positive and negative peaks of a composite input.

When a signal is applied to the base of Q_2 in the negative direction, both the base to emitter and base to collector junctions conduct and charge capacitors C_1 and C_2 until the negative peak is reached. As the peak is passed both the junctions become reversed biased and, as the transistor is a low leakage type, the capacitors are left to their own devices

The following then takes place:

Capacitor C_1 starts to discharge through R_7. Capacitor C_2 holds its charge as it looks into the high input impedance of the feedback pair Q_4 and Q_5 which also provides useful output current. As the next negative peak is approached, C_1 has discharged a certain amount through R_7 so that the base to emitter junction of Q_2 becomes forward biased before the peak is reached and Q_2 now operates as a normal transistor discharging C_2 into C_1 very rapidly until the voltages are equal and the transistor saturates. Now both C_1 and C_2 charge up to the new peak value and the whole cycle repeats itself.

It can be seen that peaks can be followed cycle by cycle provided that the next peak exceeds the voltage to which C_1 has discharged. If the next peak does not exceed this voltage, then C_1 continues to discharge until the voltage across it is less than the peak signal amplitude. The feedback pair Q_4 and Q_5 provides a high input impedance and good linearity. The output voltage differs from the voltage at C_2 and C_4 only by the base emitter voltage drop of Q_4. As Q_5 supplies the output current while Q_4 only supplies the base current to Q_5 the change in V_{oe} of Q_4 from zero to full scale is only small and linearity is maintained.

Resistor R_9 supplies the quiescent base current to Q_4. CR_1 and CR_2 provide an approximately equal and opposite voltage drop to the sum of the base to collector drops of Q_2 and Q_3 which would otherwise introduce an offset between the positive and negative peak readings. CR_3 and CR_4 stop C_1 and C_3 from becoming reverse biased. SW_1 connects either peak follower to the output stage and R_x provides a small adjustment to the voltage across CR_1 and CR_2.

Transient Spike Pulse Detector

THE PROBLEM: How to determine the occurence of a single spike pulse? The spike will have a maximum amplitude of about 50 volts, 2 ma, and a duration of 1 msec.

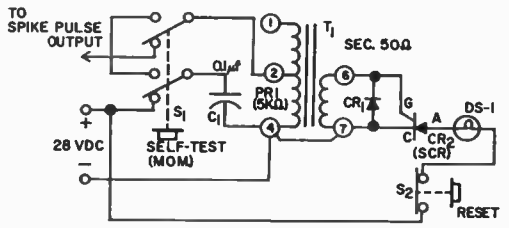
The solution: The circuit shown, which has its own "self-test" feature.

S1 = Push button switch, momentary, dpdt. ("self-test").

S2 = Push button switch, momentary, normally

DS1 = 28-volt lamp.

T1 = Triad JO-23 or any audio transformer with a turns ratio (stepdown) of 10:1. (With an equivalent transformer, if SCR does not fire



Transient spike pulse detector circuit.

closed. ("reset").

$C1$ = 0.1 μf capacitor, 200 v.

$CR1$ = Any standard diode, i.e., 1N270.

$CR2$ = Silicon Controlled Rectifier, i.e., GE #C10.

reverse the secondary loads.)

The spike pulse is stepped down through the transformer to 5 volts at 20 ma, which is sufficient to fire the SCR, causing the lamp to light and stay lit. When the reset button is pressed, the SCR anode circuit is temporarily opened, the SCR cuts off and the lamp goes out. The circuit is then ready for another spike.

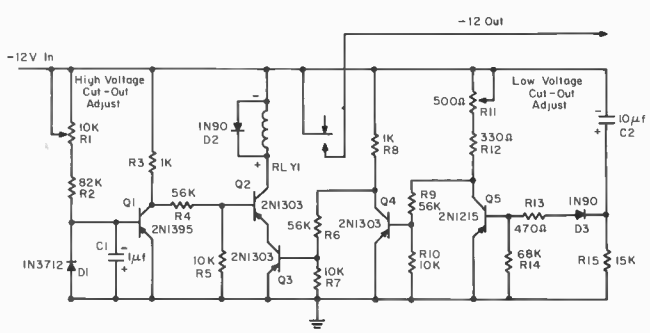
In the self-test mode, $C1$ is kept charged up by the 28-volt line. Prior to the application of the spike voltage, the "self-test" push button is pressed. $C1$ will discharge through the transformer primary causing the lamp to light. This shows that the circuit is operating and will be receptive to a spike pulse after it is reset.

Hi-Lo Voltage Cut-Off Circuit

THIS CIRCUIT senses the excursion of a dc voltage out of a preset range. The upper voltage and lower voltage cut-off limits can be independently set with two potentiometers (R_1 and R_{11}).

The high-voltage sensing element is a tunnel diode D_1. The current through the diode depends on the series resistance R_1 and the voltage to be sensed. As the voltage increases, the current through D_1 increases until it reaches over the point where the tunnel diode switches to its high-voltage state (about 1 ma). This causes Q_1 to saturate, Q_2 then cuts off and the relay RLY_1 de-energizes.

As a low-voltage sensing element, an RCA thyristor Q_5 is used. When the voltage to be sensed is applied, the negative transient formed by R_{15}, C_2, and D_3 causes the thyristor to saturate. As the voltage decreases, the current through the thyristor (adjusted by R_{11}) decreases until the point is reached where the thyristor



High-low voltage cutoff circuit. Tunnel diode D_1 senses high voltage and thyristor Q_5 senses low voltage.

cuts off. This signal is amplified and inverted by Q_4, which in turn cuts off Q_3 which, as above, causes the relay to de-energize.

This circuit does not reset simply by having the voltage return to the preset range. After the voltage has been cut off, it is necessary to re-establish the proper voltage and then interrupt it to reset the cut-off circuit. This allows the on-off switch to function as a reset switch. Thus, no additional pushbutton is needed to reset the circuit.

Missing-Pulse Detector for Narrow Pulses

THE MISSING-PULSE DETECTOR shown in Fig. 1 senses the presence of very narrow pulses of low duty cycle, and lights a lamp if the pulses are absent. A continuous pulse waveform, as shown in Fig. 2a, is applied at the input. Transistors Q_1 and Q_2 form a pulse stretcher whose period is between 30 and 40 msec. The pulse stretcher is necessary because the trigger pulses, only 4 μsec wide, have a period of 50 msec. The pulse stretcher is triggered each time a pulse is received at the input.

The Q_2 collector waveform consists of positive pulses,

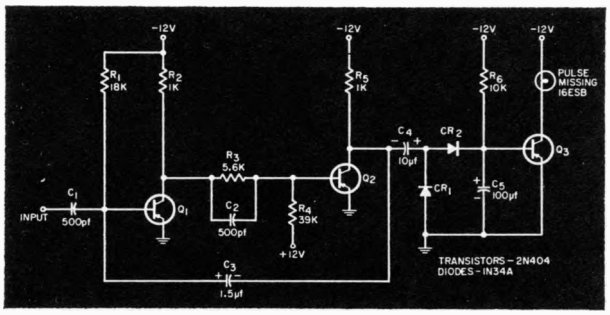


Fig. 1. Missing-pulse detector responds to narrow pulses.

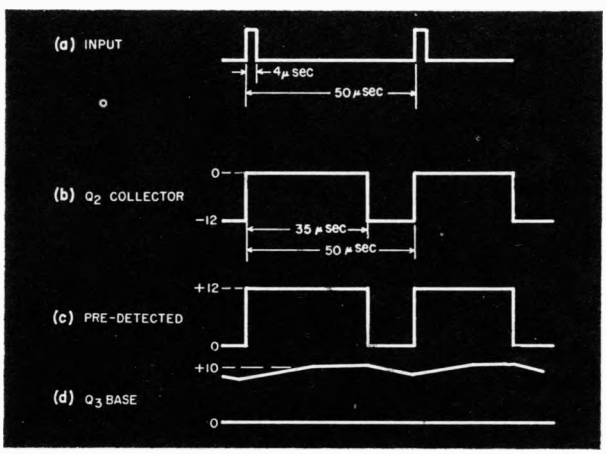


Fig. 2. Waveforms at various points of missing-pulse detector.

rising from —12 v to ground, as shown in Fig. 2b. Diode CR_1 and capacitor C_1 form a dc restorer or negative clamp, clamping the negative portion of the waveform to ground (Fig. 2c).

The positive pulses are peak-detected by CR_2 and C_5, biasing transistor Q_3 off. Thus, as shown in Fig. 2d, the net detected voltage at the Q_3 base is positive, and essentially constant.

In the absence of input pulses, transistor Q_3 will lose its bias and be turned on by the current through R_6, lighting the PULSE MISSING lamp. This circuit is truly fail-safe, for the failure of any component in the circuit will cause the lamp to light. ◆◆

Square-Wave Symmetry Detector

THIS CIRCUIT produces a zero-volt output when a perfectly symmetrical square wave is applied to its input, and positive or negative output voltages for an unsymmetrical wave input, depending on the type of wave.

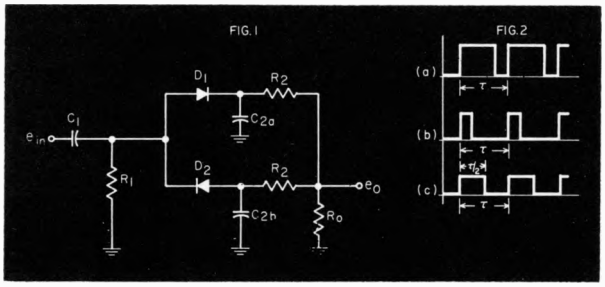


Fig. 1. Square-wave symmetry detector.
Fig. 2. Typical rectangular waveforms.

When wave *a* in Fig. 2 enters the circuit in Fig. 1, a negative output voltage is produced. When wave *b* enters the circuit, a positive dc voltage is produced at the output

The signal's dc component is first removed with the R_1C_1 combination. With wave *a* the negative peak will be larger than the positive peak when the dc component is removed. In wave *b*, the positive peak will be larger than the negative peak after removing the dc component. In wave *c* the positive and negative peaks will be of equal magnitude after the dc component is removed.

Capacitor C_{2a} charges to the positive peaks, while C_{2b} charges to the negative peaks. These two dc voltages are then summed through resistors R_2, and the result applied across the output resistor. One application for this circuit might be as a symmetry detector at the output of a Schmitt trigger which is driven by a sine wave. ◆◆

Current Amplitude Detector

PULSED DRIVE CURRENTS into a memory array often must be monitored as part of a self-detection or self-correcting system, indicating when a current goes out of tolerance. A current detection circuit that senses excess current is shown in Fig. 1.

The current that is monitored is coupled into the circuit through transformer T_1. Diode D_1 clips the reverse voltage

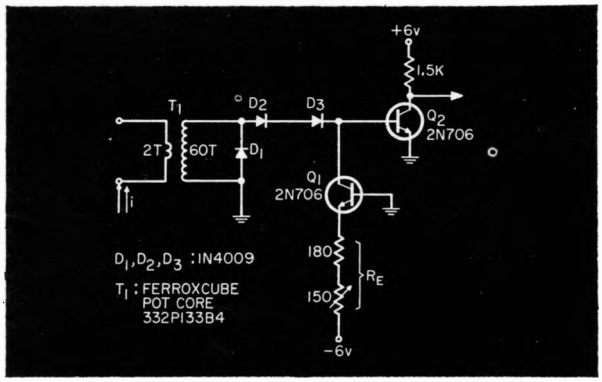


Fig. 1. Current amplitude detection circuit.

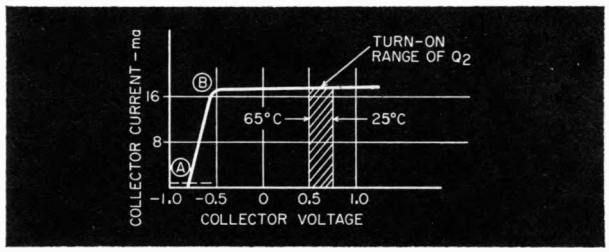


Fig. 2. Operating points for quiescent and alarm conditions.

spike that is developed across the secondary of T_1 when the current pulse terminates. Current is always flowing in quiescent periods between pulses, Q_1 is in deep saturation, its emitter and base current being approximately equal. Collector current is very small, in the microampere range. The collector voltage is equal to the voltage drop across diodes D_2 and D_3. Figure 2 shows the operating points on the V_c-I_c characteristic curve. Quiescent condition is at point *A* on the curve.

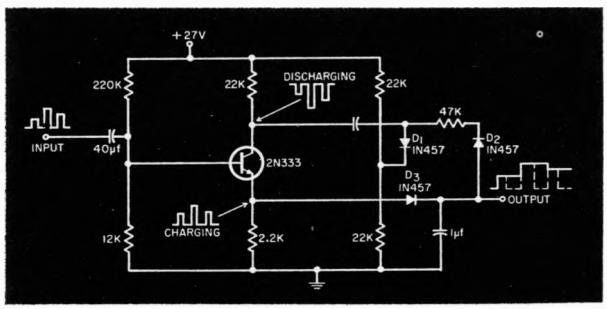
When a current pulse is applied to the primary of T_1, current starts to rise in the secondary circuit. The collector of Q_1 initially absorbs this current. As this current continues to increase, the operating point moves up from point *A* on the bulk resistance slope until the transformer's secondary current approaches the value of Q_1's emitter current at point *B* on the characteristic curve. At this point, Q_1 starts to come out of saturation and its collector voltage rises. When this voltage reaches the turn-on voltage for Q_2 at point *C*, a signal pulse appears at the collector of Q_2.

The circuit shown in Fig. 1 is capable of detecting a current pulse over a 1.2-amp current level within ± 10 ma. When tested at a temperature variation of 25° to 65°C, the detection level increased by 20 ma. This circuit can also be used at other current levels by proper adjustment of R_E, which varies the current clamping level. ◆◆

Boxcar Envelope Detector

ENVELOPE DETECTION with the conventional rectifier circuit produces negative-peak clipping or diagonal distortion on rapidly downward changing envelopes due to the action of the PRF bypass capacitor. More faithful recovery of the modulation envelope can be achieved with "boxcar" generation, as is done in radar systems, which approximates the envelope in level steps between successive peaks in the wavetrain.

The wavetrain whose envelope is to be recovered must



Boxcar envelope detector.

be of one polarity, as from a diode detector. The pulses are applied to a single-stage amplifier having a dual-polarity output, the inverted polarity output being made much the larger.

The amplifier non-inverted output charges the storage capacitor through the series diode; the negative output (whose wave base line is clamped to a positive level higher than that to which the capacitor will ever be charged)

simultaneously tends to discharge the capacitor through a diode and resistor. The voltage level to which the capacitor is charged is thus "corrected," upward or downward, at the time of each input pulse.

The charge-circuit short-circuit current must be substantially greater than the discharging-circuit short circuit current. For a wavetrain with peaks of decreasing amplitude, the discharging circuit gain must be sufficient to afford a discharging voltage at least large enough to decrease the capacitor voltage to that of the charging voltage.

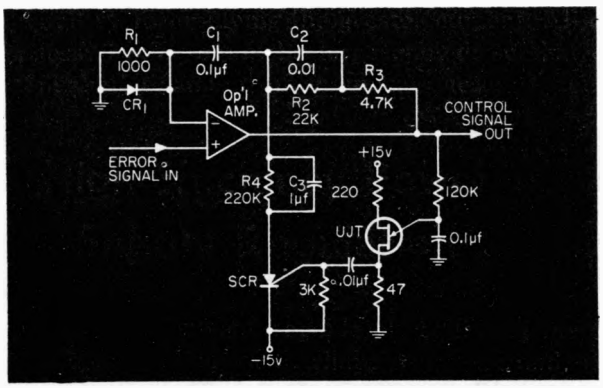
The various R-C time constants in the circuit shown would be rather large for any applications; the application in which it was used was envelope recovery of a 5-pps wavetrain. Smaller time constants would, of course, be more appropriate for a wavetrain of shorter period.

Automatic Search and Control Circuit for Servo Loop

THIS CIRCUIT is applicable to servo control systems where automatic acquisition with a linear search is desired. Applications include afc and phase-lock controls where the wide bandwidths of current solid-state operational amplifiers can be exploited. This basic circuit has been used in a phase-locked microwave system with a bandwidth of 300 kc.

An active integrator is used in a dual role as a linear search generator as well as an integrator in the control system.

In the circuit, the bias applied to the negative summing point of the operational amplifier is set so that in the absence of an error signal input, the integrator output builds up towards positive saturation. V_f, the unijunction firing potential, is set just below the operational amplifier saturation. When the UJT fires, it triggers the SCR, which in turn discharges the integrating condenser C_1. Control-loop acquisition occurs when the error voltage bucks out the bias on the summing point. If acquisition does not occur during one search sweep, the discharge circuit resets the integrator and another sweep is initiated.



Servo automatic search and control circuit.

The values of R_1, R_2, R_3 and C_2 determine the characteristics of the control system and must be chosen accordingly. CR_1 is necessary to permit a low impedance discharge path for C_1.

Since the summing point is a virtual ground, it does not affect normal operation. The sweep rate is a function of R_1, C_1 and the bias into the negative summing point. This bias is set such that the voltage drop across R_1 is about equal to 20 percent of the maximum discriminator output. C_3 should be at least ten times larger than C_1 to insure adequate charge transfer. R_4 must be large to prevent the operational amplifier from supplying SCR hold-in current.

An important feature of this circuit is the positive reset action of the UJT-SCR circuit. Lock-up due to power supply transients, etc., is prevented. The UJT circuit will continue to trigger the SCR as long as the operational amplifier output is above the preset UJT firing potential (V_f). The UJT oscillator should have a time constant sufficient to permit C_3 to discharge appreciably through R_4.

PRF Discriminator

THIS CIRCUIT needs a pulse-train burst of only 2 successive pulses to determine its PRF above or below a given limit, and two such circuits and a NAND gate can indicate the presence of a given PRF within 0.1 percent or 1 kHz ±1 Hz.

The input pulses are first given standard width and amplitude by a one-shot monostable circuit. Then they are applied to isolation diode CR_1. Through CR_1 the pulses charge capacitor C_1, which discharges through resistors R_1 and R_2. The time constant is such that the voltage on C_1 either will or will not reach ground before the next pulse arrives, depending on the PRF rate (see Fig. 2).

The charge on C_1 will charge C_2 through R_3. If the voltage on C_1 goes below ground (Fig. 2a) transistor Q_1 will conduct and bias Q_2 into conduction. Q_2 will quickly discharge capacitor C_2. However, if the next pulse arrives soon enough (Fig. 2b), Q_1 and Q_2 will stay non-conducting, and the second pulse will deliver its charge to C_2, adding to the previous charge. A level detector at the output will now signal the presence of the higher PRF.

The sensitivity of the discriminator depends on the fall-time of the pulse on C_2, which is about 1 μsec. For a PRF of 1 kHz there is about 1 msec between pulses, and a difference in period of only 1 μsec will determine whether the charge on C_2 will build up or not. Hence the 0.1-percent accuracy.

Two such circuits with time constants different by 2

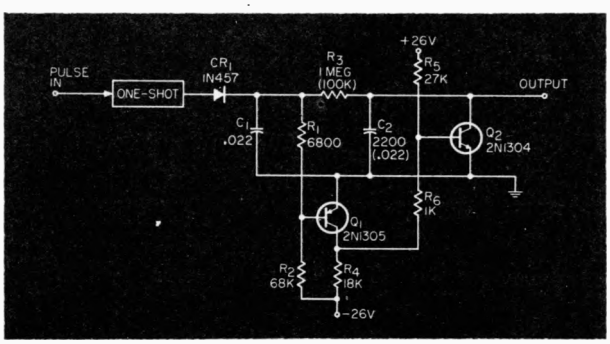


Fig. 1. PRF discriminator.

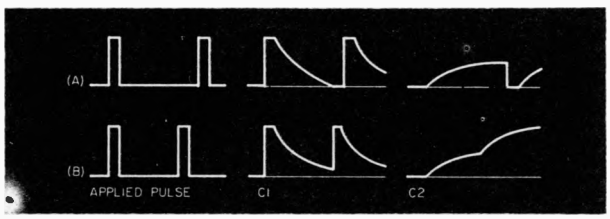


Fig. 2. Capacitor charging waveforms.

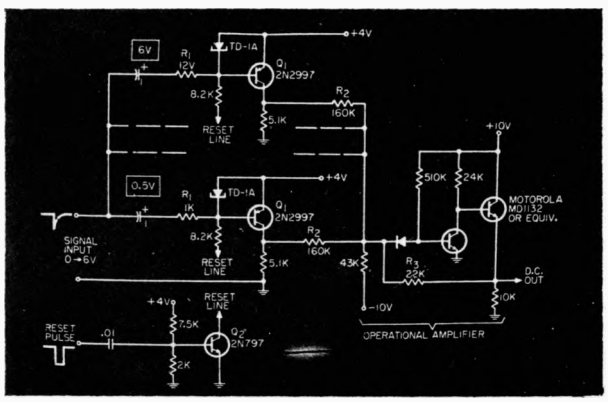
μsec will or will not generate an output level change signal. If for a particular PRF the circuit with the lower time constant generates a signal and the other does not, a NAND circuit will indicate the presence of a pulse train with a period within 1 μsec of the desired PRF. (For continuous pulse trains R_3 should be as large as possible so that built-up charge on C_2 will not affect the circuit time constant.)

Tunnel-Diode Pulse-Height Discriminator

IF A TUNNEL DIODE is biased with a current greater than I_p and loaded with a resistance large enough to yield two stable points of operation, the diode will "latch" in its high-voltage state when pulsed with a current that exceeds I_p. The current can be controlled by series input resistor R_1 and a predetermined range of pulse heights can be detected. When the bias current is interrupted, the tunnel diode returns to its low-voltage state and is ready to be triggered again. A reset pulse width greater than 1 μsec to Q_2 provides this operation.

With several tunnel diodes, each set to detect a given pulse height, transistor Q_1 delivers a fixed current to the operational amplifier when the tunnel diode is triggered. As the input pulse height increases, more and more of the tunnel diodes are triggered and the input current to the operational amplifier increases linearly. The output voltage steps of the amplifier are controlled by the ratio of R_2 to R_3.

This circuit was used to analyze 30-nsec pulses varying in height from 0 to 6.0 v peak and over a temperature range of −20° to +60°C. The trigger points varied no more than ±2 percent of the selected point and the operational amplifier output changed by only ±50 mv using standard 5-percent resistors. In the schematic shown, ten stages were connected in parallel and 0.5 v steps were used for a 0-to-5 v output range.

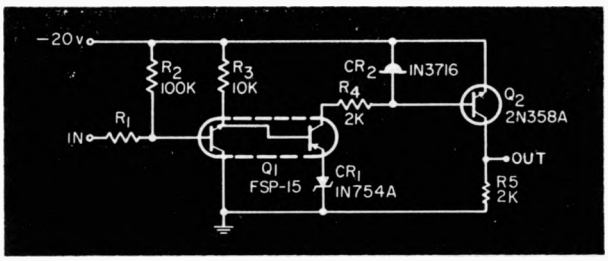


Tunnel-diode pulse-height discriminator.

Accurate DC-Level Detector

THE CIRCUIT shown in Fig. 1 fills a need for an accurate dc level detector with extremely small hysteresis. Input can be either a varying dc voltage or, as in the original application, a variable resistance such as a thermistor.

The dual complementary transistor Q_1 is a high-stability dc amplifier with nearly zero offset voltage. Zener diode CR_1 provides a threshold level which is reflected back to the input base. As the input voltage is increased, no current will flow in the pnp transistor until the threshold voltage of CR_1 is reached, at which point current increases very rapidly. As the current reaches the peak-point current of the tunnel diode CR_2, the diode switches to its high voltage state, turning on Q_2. The tunnel diode-transistor combination provides discrete switching action.



DC level detector with small hysteresis.

The input level at which switching occurs is dependent primarily on the zener voltage, but lower levels can be switched by varying R_1. Hysteresis is controlled by the knee of the zener diode characteristic. Using a sharp-breaking diode, a hysteresis of less than 10 mv has been achieved.

Phase-Locked Frequency Discriminator

THIS CIRCUIT may be used to phase lock a low frequency oscillator to some desired frequency. It employs a flip-flop, a filter, and a dc level shift to provide the required center frequency voltage control to the oscillator.

In the circuit, a trigger generated from the master frequency enters at B, while a trigger from the phase locked frequency enters at A. Operation depends on the fact that when the frequency at A is higher than the frequency at B, the average Q_2 collector voltage is positive, while for B frequency higher than A frequency, the average Q_2 collector voltage is negative. In either case, an error-voltage sensing circuit corrects the frequency at A, thus tending to maintain Q_2 collector at 0 V average.

In operation, the trigger at B causes Q_2 collector to become negative. A trigger at A causes Q_2 collector to become positive. Thus, if more B triggers are received than A triggers, (B frequency greater than A frequency) Q_2 collector will be negative more often than it is positive, as shown in Fig. 2a.

The pulse signal appearing at the Q_2 collector is filtered by a resistor in series with a large capacitor, and the resulting dc is applied to Q_3 base. Q_3 acts as a dc shift and

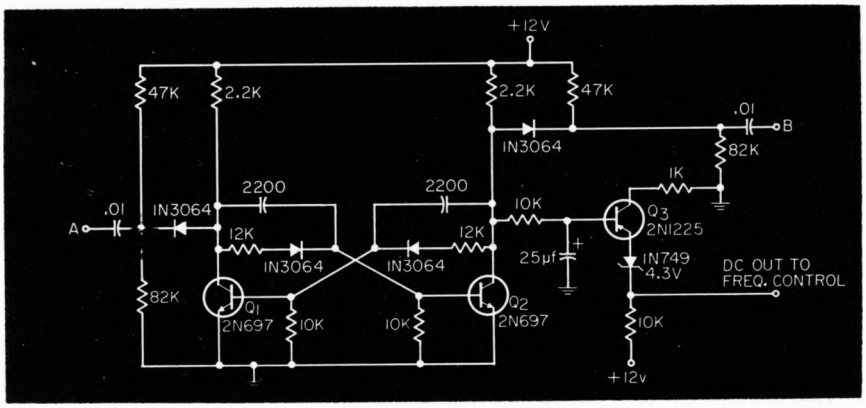


Fig. 1. Frequency detector phase-locks signals at A and B.

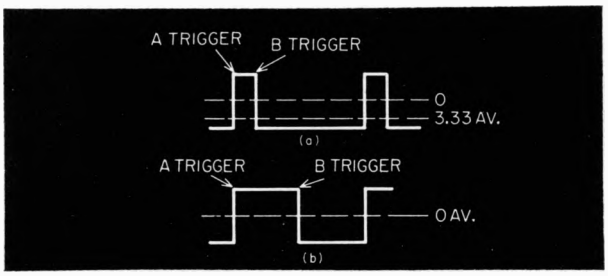


Fig. 2. Waveforms at Q_2 collector for: B frequency greater than A (Fig. 2a) and equal, phase-locked frequencies (Fig. 2b).

emitter follower. The error voltage at Q_3 output is used to correct the oscillator frequency. When correction is complete, Q_2 collector voltage appears as in Fig. 2b, and both frequency and phase lock are achieved.

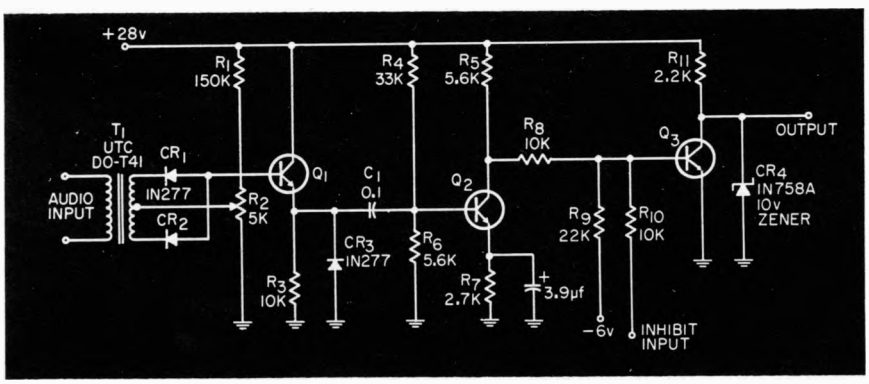
The oscillator used in conjunction with this circuit may be a voltage-tuned multivibrator or a unijunction sawtooth generator. As shown, the circuit was used to sync a unijunction sawtooth generator to operate at 10X the frequency at *B*. *B* frequency had a center value of 16 Hz and varied about this value by ±25 percent. A 1/10 counter followed the unijunction and its output was used to generate the trigger input to *A*.

Sine-Wave Zero Crossing-Detector

THE ZERO-CROSSINGS detector with adjustable output interval furnishes a 10-v pulse that coincides with the zero-crossings of a sine-wave input at frequencies throughout most of the audio range. Transformer T_1 and matched diodes CR_1 and CR_2 form a full-wave rectifier with an average value equal to the voltage selected by adjusting R_2. Q_1 is an emitter follower that has its output referenced to ground by CR_3, clipping the portion of the signal that tends to go below ground. The small positive pulse remaining is ac coupled into amplifier Q_2 which, because of its high gain, is easily driven into saturation. The output of Q_2 is fed into Q_3, which operates as a NOR circuit.

A + 10 v level applied to the second input of the NOR will inhibit its operation, while a ground potential there will allow positive pulses to appear at the output.

The portion of a cycle about the zero-crossing during which a positive pulse is available at the output can be adjusted by varying R_2. By shifting the average value of the rectified sine wave upward, a larger portion of it is amplified and a subsequent earlier rise and later fall of the output pulse takes place.



Zero-crossing detector with adjustable output interval.

Product Detector Uses FET Tetrode

THE CHARACTERISTICS of the dual-gate FET makes it ideal for use in a solid-state version of the common pentagrid product-detector circuit. Since each gate has independent control of the drain current, the beat frequency oscillator voltage can be injected into one gate and the signal into the other. As in the pentagrid circuit, the output current is then the product of the two voltages.

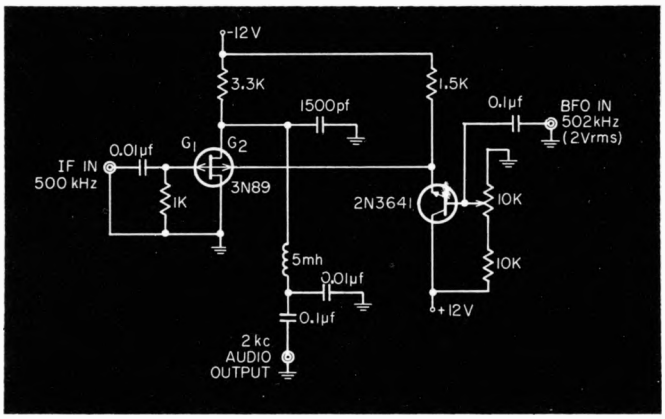


Fig. 1. Pentagrid-type operation of dual gate FET makes it suitable for product-detector circuit.

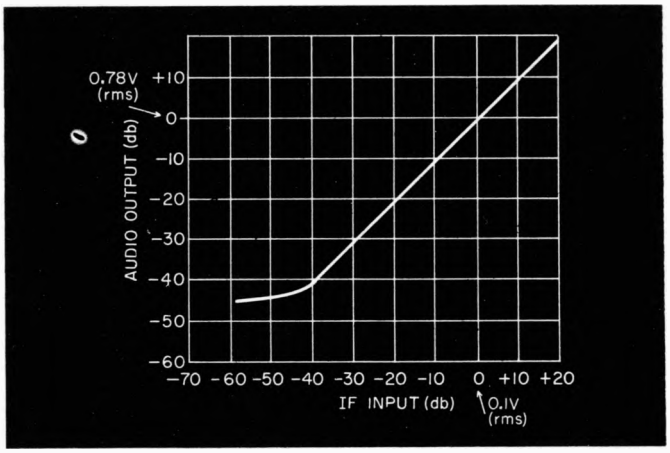


Fig. 2. Output of product detector is linear over a wide dynamic range.

In the circuit of Fig. 1, an emitter-follower is used to isolate the BFO, and provide the proper bias to G_2.

The dynamic range of the detector, shown in Fig. 2, is greater than that found in most typical tube-type product-detectors used in modern single-sideband receivers.

Pulse-Train Detector and Counter

THE CIRCUIT shown in Fig. 1 detects the envelope of bursts of high-frequency pulses or, with a small modification, will give an output after a specified number of pulses have appeared at the input. A built-in threshold excludes noise and pulses of low amplitude.

This circuit can be used over a range of input frequencies from 1 kHz to 1 MHz with suitable component values. With the values shown, the upper limit on the input prf is 1 kHz. The input can of course be R-C coupled if desired.

Transistor Q_1 amplifies the signal from a magnetic pick-up. This stage has built-in noise threshold provided by the clamp diode D_1. The collector of Q_1 goes below +5 V only after the input exceeds V_t (in this case 50 mV), enabling the current source Q_2 to charge the capacitor C. The discharge time constant of C is much larger than the input repetition rate, so V_c changes from −5 V to +2 V, thus turning on Q_3. With the given values, the circuit will operate for duty cycles greater than 0.2%. Turn-on delay for a 10% duty-cycle pulse train is given approximately by

$$T_d = nT = 0.06/(10{,}000\ w/T - 17) \simeq 0.06 \text{ msec}$$

where T_d is the turn-on delay, n the number of high frequency pulses, T the pulse-train period, and w the pulse width.

With a minor modification, the circuit can be used as a pulse counter. If the cathode of diode D_1 is returned to point "A" instead of +5 V supply as shown, the circuit "locks up" after a specified number of pulses have arrived. Capacitor C must be given time to discharge, or must be discharged manually, before the input is reapplied.

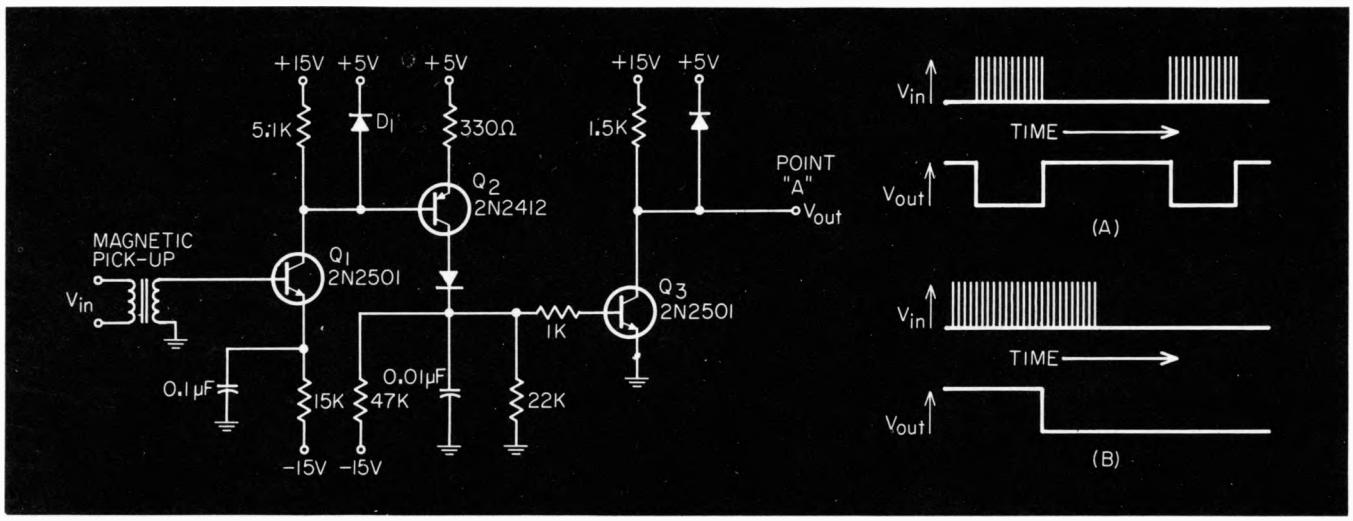


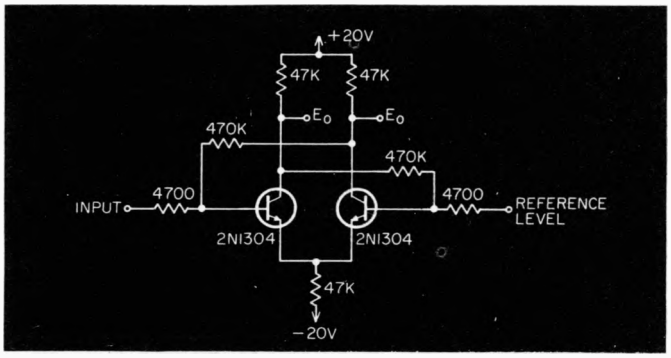
Fig. 1. Basic circuit is a pulse-train detector. If D_1 is returned to point "A", circuit will give an outpnt after counting specified number of pulses.

Fig. 2. Input and output waveforms for detector (2) and counter (B).

Adjustable Level-Detector

THIS CIRCUIT is a differential amplifier with positive feedback, which can be used as a level detector. Like a conventional flip-flop it has two stable states and will switch states when the dc input level goes above or below a preset-reference level. The output can be taken from either collector depending on the polarity required. An advantage of this circuit is its inherent dc-stability due to the balanced configuration.

With component values shown, the circuit will change state for an input-voltage differential of 100 mV with respect to the reference. The hysteresis depends on the amount of positive feedback. The reference level may be above or below ground. Output voltage swing at the collector and the range over which the reference may be changed, are determined by the values of the collector and emitter resistors.

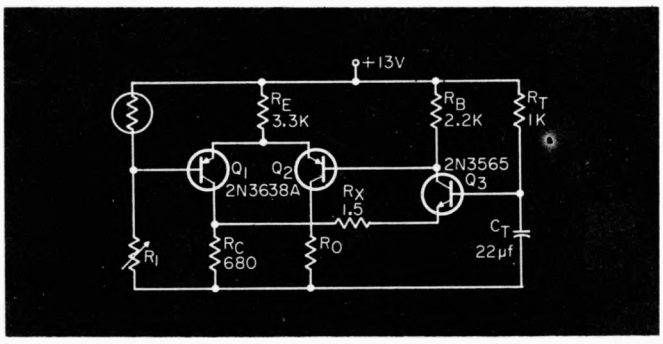


Stable state of this circuit changes when input level crosses the reference level. Output is taken from either collector.

Time-Delayed Schmitt Sensor

THE SCHMITT TRIGGER CIRCUIT is widely used for industrial control sensing because the differential can be designed to be any suitable amount. However, industrial sensing circuits also often require a delay in the sensor control at start-up, until such time as the system and process are in normal operating mode.

In the example shown here, a photocell sensor command is nullified until certain fluid lines have been filled, to prevent the sensor's construing lack of fluid to be a lack of concentration.



Time-delayed Schmitt trigger with photocell as sensor.

The circuit shows a way of incorporating time delay in the Schmitt circuit itself through the use of another transistor as a switch, one that closes the bias circuit of the Schmitt. The delay is obtained with an *RC* network in the base of this transistor, which is designed so that the saturation current of the transistor is equal to the required bias current of the Schmitt. The output transistor is thus held inactive for the time required to charge the timing capacitor to approximately design voltage for its base.

The circuit uses economy-line transistors in a Schmitt configuration giving 0.3-V differential. With a photocell sensor, the value of R_1 will depend on the signal level when at the level for control. This sensor is connected as shown, or is interchanged with R_1 depending on the polarity of control required from the output.

For a 22-μf tantalum as C_T, the time delay is about 15 sec. The value of R_T must be small enough to allow a saturation current equal to the required bias current for the Schmitt. If less delay is wanted, then R_T should be made smaller, but for more delay the capacitor should be increased, not R_T.

The time-delay scheme can be incorporated in any existent Schmitt circuit. However, the saturation current of Q_3 must equal the existent bias current of the Schmitt, and R_X should be reduced according to what the saturation voltage drop actually is. The maximum R_T is set by the saturation current required, and so is proportional to the current gain of Q_3.

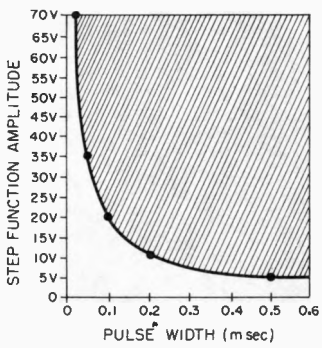
Noise-Rejecting SCR Trigger Circuit

IT IS OFTEN difficult to obtain reliable SCR triggering when inductive switching transients are present. The circuit described here, however, can discriminate between data pulses and random transients.

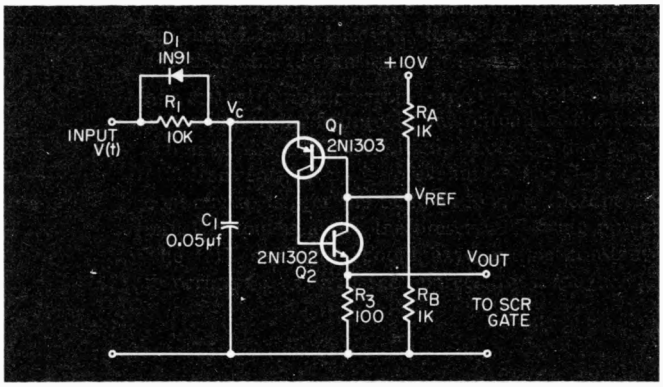
An integrator is combined with a voltage comparator to detect the difference in voltage-time areas in the two types of pulses (random transients have a smaller $V \times t$ area than data pulses, which have a fixed $V \times t$ area).

An approximate integration of the input pulses is performed by C_1R_1. The complementary pair Q_1, Q_2 functions as a voltage comparator, delivering an output whenever V_c *is* greater than V_{ref}.

Without an input, the voltage of C_1 will be zero, and thus Q_1 *and* Q_2 will be cut off. When an input $V(t)$ is applied, the emitter voltage of Q_2 (V_c) will rise. If the (voltage) × (time) area is sufficiently high, Q_1 *and* Q_2 will turn on when V_c is slightly greater than V_{ref}. Since both Q_1 *and* Q_2 are saturated and R_B is shunted by R_3, C_1 will discharge rapidly, producing a 10-μsec



Locus of possible firing points



Data-pulse discriminating trigger circuit.

pulse across R_3 and firing the SCR.

If the applied pulse is too narrow to fire Q_1 and Q_2, C_1 will discharge through D_1, preventing an accumulation of noise pulses from firing the circuit. However, note that if the pulse at the input is too wide, multiple outputs may occur.

In the circuit shown, data pulses are 8 V high and 0.5 msec wide. The reference voltage is chosen to cause firing before the exponential slope becomes too flat.

Thus, with $V_c = 5$ V at 0.5 msec,

$5 = 8(1 - e^{T/\tau})$

Or τ should be about one time constant.

$\tau = RC = T = 0.5 \times 10^{-3}$ sec

$C = 0.05\ \mu F$

Note that R_B must be much greater than R_3 to obtain a large change in V_{ref} when the transistors switch on.

Buffered Detector

MANY DESIGNERS have suggested modifications to the popular Schmitt trigger, but so far no one has significantly reduced the interdependence of the circuit components.

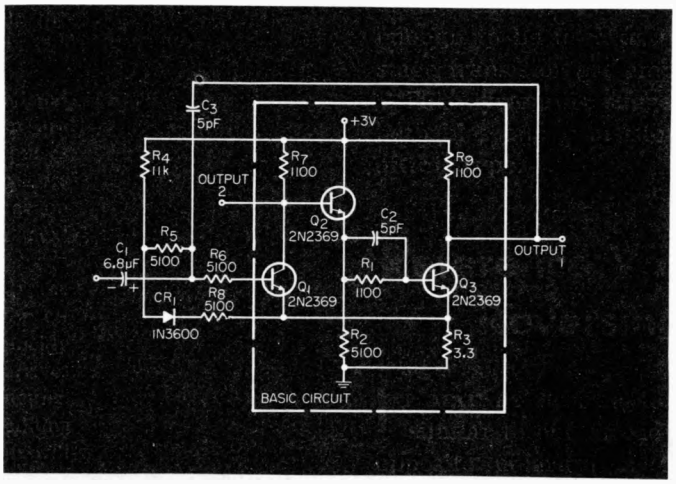
The modified circuit[1] shown here, preserves the emitter coupling of the basic Schmitt, but replaces the divider of that circuit with a buffer network. This simplifies the design of the circuit, by removing the loading effect of Q_3 at the collector of Q_1. The full voltage swing at Q_1 collector is applied to the base of Q_3 via R_1.

When the input is above the threshold level, cutoff of Q_3 is defined by the difference between the collector-emitter saturation voltage of Q_1, and the base-emitter saturation voltage of Q_2. This difference is about 200 mV for most silicon transistors. Thus hysteresis remains low for a wide range of reference voltages.

Resistor R_1 is made large enough to saturate Q_3 when the input is below threshold. Resistor R_2 keeps Q_2 in the active region, preventing this transistor from introducing propagation delay. The value of R_3 is calculated to establish the reference voltage and guarantee regeneration.

Good results are obtained with resistance values in the range 2 to 10 ohms. Therefore a zener diode, with dynamic impedance in this range, can be substituted for R_3 to establish various threshold levels. Diode CR_1 compensates for the effects of temperature on the V_{BE} of Q_3.

The reader is cautioned against attempting to minimize hysteresis, by using tricks such as adding a separate resistor between Q_1 or Q_3 emitter and R_3.[2] As with the Schmitt circuit, total elimination of hysteresis is accompanied by loss of regeneration and the circuit becomes an operational amplifier.



This detector circuit is similar to a Schmitt trigger but buffer amplifier Q_2 is included in the feedback path.

With the component values shown, the circuit fires with as little as 1-mV pk-pk signal. Output rise and fall times are about 40 ns. Performance is satisfactory with supply voltages ranging from 3 V to 28 V.

Complementary outputs are available because Q_1 collector is buffered from the base of Q_3.

References

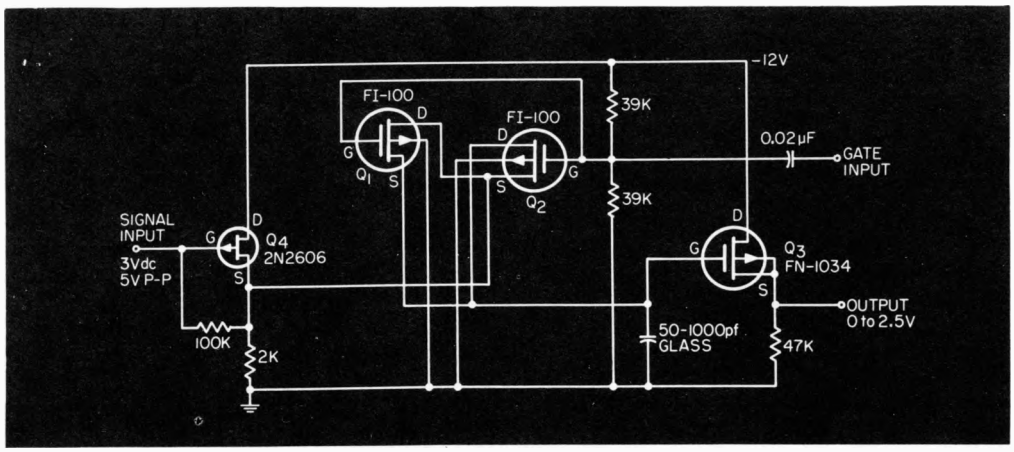
1. Patent pending.
2. J. Millman and H. Taub, *Pulse and Digital Circuits*, McGraw-Hill Book Co., 1956, pp 171-2.

Boxcar Circuit Uses FETs

USE OF FETs simplifies the design of sample-and-hold circuits. The circuit shown here samples either dc or ac signals. Storage quality is excellent due to the high input impedance of Q_3. The circuit works at high sampling rates, needs no temperature stabilization and handles large input amplitudes. Switching transients at the input are suppressed by at least 30 dB.

Transistors Q_1 and Q_2 are cross-coupled from drain to source in a series-switch configuration. The analog input is connected to one drain-source pair and the storage capacitor is connected to the other pair. This circuit conducts in both directions. Thus the switch transfers either increasing or decreasing input signals to the storage capacitor during conduction.

A switching pulse, −12 V in amplitude and 0.5 to 20



Sample-and-hold circuit with FETs gives improved performance.

μsec in duration, controls the FET gates. The series resistance of the switch circuit changes from approximately 250 meg to 100 ohms during switching.

Source-follower Q_3 acts as a buffer between the output and the glass storage capacitor. This combination gives negligible leakage of the stored signal.

With the component values shown, repetition rate is from 200 to 250 kHz. The circuit will store sample voltages having a width of only 0.5 μsec.

Threshold Detector Uses IC

HERE IS A SIMPLE latch circuit which provides a low-cost replacement for conventional threshold circuits in digital systems. The only component used is a dual-gate logic element, connected to give positive feedback.

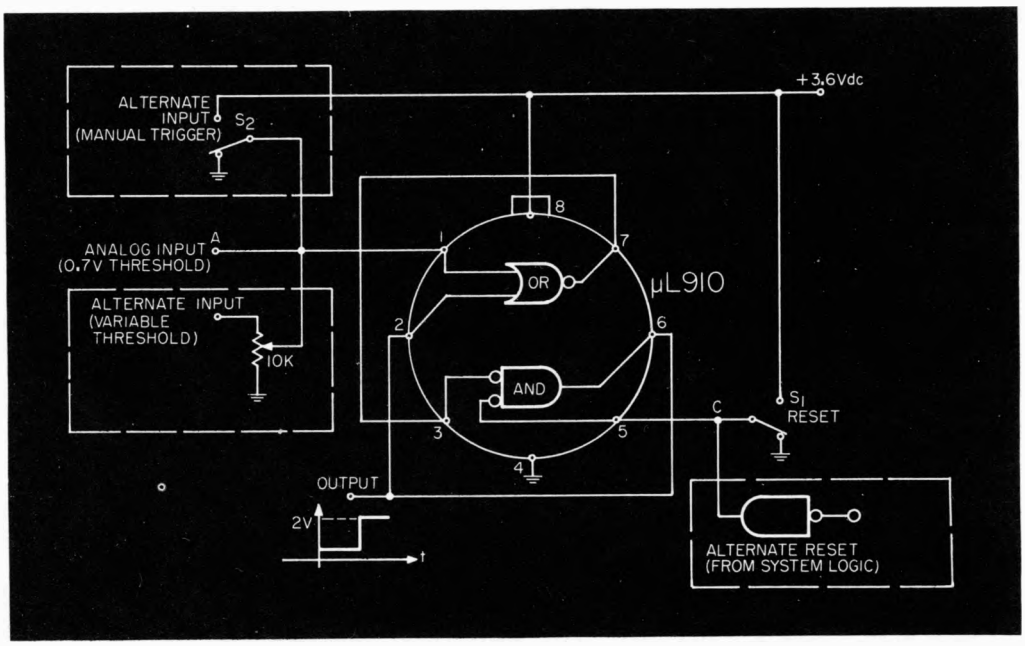
An analog input signal triggers the circuit at a predetermined threshold level, to give a change in dc output level. Because of the feedback configuration, the output has a fast rise time. Output levels are inherently compatible with microcircuit logic.

Depending on the application, the basic circuit can be used in many different ways. If you need a variable threshold, connect the input, *A*, to the wiper of a potentiometer as shown in the figure.

The circuit also eliminates the effects of switch bounce. Instead of using the analog input, connect the switch, S_2, to the input as shown. This gives a manual input for digital systems.

A false (high) level at point *C* resets the latch. A suitable pulse is generated manually by switch S_1, or automatically by the system logic.

The temperature coefficient is the same as for a silicon transistor (approximately 2.2 mV/°C). This technique has been used with conventional DCTL as well as the RTL shown.



This versatile latch circuit has many threshold-sensing applications. Alternative connections are shown inside the dashed boxes.

Sample-and-hold circuit is fast yet accurate

VARIOUS DESIGNERS have recently described simple circuits to sample and hold the peak values of pulse signals. Some of these circuits emphasize accuracy but give limited response speed.

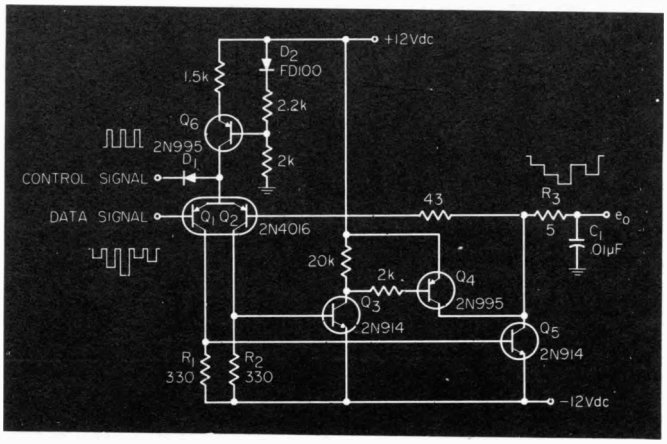
The circuit shown here is relatively simple and is accurate even for submicrosecond sampling periods. The output responds to a step input level in 300 ns with 0.1-percent accuracy. Input-to-output offset is low (typically 1 or 2 mV) because of the characteristics of the matched pair of PNP transistors (Q_1, Q_2).

A logic input, applied to the cathode of D_1, controls the state of the circuit. When the control signal is high, D_1 is back-biased. Transistor Q_3 then supplies current to the

emitters of Q_1 and Q_2, thus enabling the input matched pair. If, during this time, the data signal at Q_1 base is at lower voltage than the output signal, then Q_1 conducts more heavily than Q_2. This increases the current through R_1 and decreases the current through R_2. So Q_3 turns on while Q_2, and therefore Q_4, turns off.

Conversely, if the input data signal is at a higher voltage than the output, transistors Q_3 and Q_4 conduct while Q_5 is disabled. Thus, in the presence of sampling pulses, capacitor C_1 is either charged or discharged with fairly large currents until the output-voltage feedback to Q_2 base equals the input voltage at Q_1 base. Resistor R_5 prevents overdrive and insures monotonic changes in output voltage. The low value chosen for this resistor speeds circuit operation.

A low control-logic level, at D_1 cathode, diverts current from the Q_6 collector through D_1. Simultaneously, transistors Q_1 and Q_2 are turned off. Under this condition, transistors Q_4 and Q_5 are also turned off, thus preventing discharge of C_1 during the "hold" period. In this state the circuit maintains the last value of the input signal that occurred during the previous sampling period.



Fast and accurate sample-hold circuit. Matched transistors (Q_1, Q_2) give low offset between the sampled input and held output.

An improved FET Sample-and-hold circuit

ONE SOURCE OF ERROR, in FET sample-and-hold circuits, can be minimized by adding a few extra components. Other errors can be reduced by careful selection of a suitable op amp and low-leakage FETs.

The conventional FET circuit, shown in Fig. 1, has one serious disadvantage. If the sampled waveform is changing, at the instant of a "hold" command, the capacitor voltage V_c will be diminished by the voltage drop caused by current, i_c, flowing through the finite "on" resistance of the FET. In many applications this loss is significant.

The improved circuit of Fig. 2 largely overcomes the problem. During the "sample" interval, both FETs are on and the bipolar transistor is cut off. During the "hold" interval, the situation is reversed. Because the FETs are inside the loop of a high-gain amplifier, their "on" resistance (as seen by the capacitor) is reduced by the open-loop gain. Thus, charging speed is essentially limited only by the output-current capability of the voltage follower. The resistance seen by the capacitor is given by the following equation:

$$Z_{out} \simeq \frac{R_o + R_{on}}{1 + A} \quad (1)$$

Where R_o = output impedance of amplifier, and R_{on} = "on" resistance of the FET.

When the FETs are off, the capacitor is almost perfectly isolated. During this interval Q_1 saturates, thus holding the amplifier loop closed and preventing it from going into saturation.

Diode D_1 serves to limit the base-emitter voltage of Q_1 to approximately 0.6 V. Thus it protects the transistor from possible damage during the "sample" interval when Q_1 is cut off.

Diode D_2 prevents gate current from flowing in Q_2 and Q_3 during the "sample" interval when the FETs are on. Without the diode, gate current would cause errors in the capacitor voltage.

Resistor R_1 discharges the FET interelectrode capacitances so that the FETs can turn on

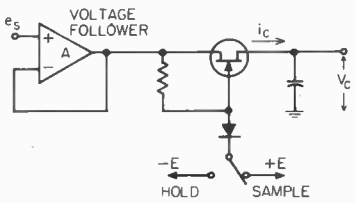


Fig. 1. Conventional FET sample-and-hold circuit has errors caused by drop across the FET during the sample period.

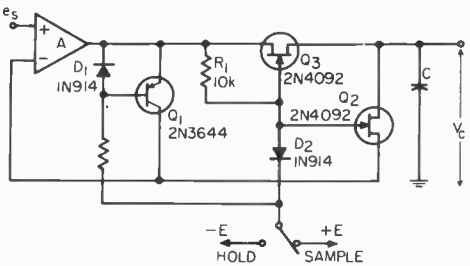


Fig. 2. Modified circuit overcomes the problem of FET "on" resistance, by placing FETs inside feedback loop. Capacitor then sees a much lower source resistance.

after D_2 has been cut off.

Though the modification described here reduces errors caused by FET "on" resistance, other sources of error still remain. The circuit has been tested using a μA709C IC op amp, but, because of its poor transient response, this amplifier is not the best choice for sample-and-hold circuits. However, satisfactory performance can be achieved when tracking at rates well below the limited slew rate of the amplifier.

The following factors all cause errors and should be considered in the design of accurate sample-and-holds.

- Finite amplifier open-loop gain causes finite input and output impedance and less than unity gain for the closed loop.
- Amplifier offset-voltage temperature drift is indistinguishable from desired input signals.
- Finite amplifier slew rate limits the rate of input-voltage change that can be tracked.
- FET drain-source leakage allows partial discharge of the stored capacitor voltage.

Remember, also, that another amplifier is usually required to buffer the output from the capacitor. (This amplifier is not shown in Figure 2). The input impedance and bias current of the second amplifier will provide additional unwanted discharge paths for the stored voltage.

Thermistor circuit senses air temperature and velocity

A THERMISTOR CIRCUIT can be used, not only to sense temperature changes, but also to sense changes in air velocity. Thermistor temperature depends on ambient temperature and also on heating caused by electrical power dissipated within the thermistor. Temperature rise from the latter source is governed by air flow past the thermistor.

The type of circuit described is useful for power-supply protection. Normally, forced-air-cooled supplies are protected by a pressure-actuated switch in the air duct and by temperature sensing devices at critical points in the circuit. But satisfactory protection can be achieved by a single solid-state circuit — thus eliminating electro-mechanical components which may be unreliable.

With careful design of the circuit, and of the thermistor enclosure, this approach can be used to sense any desired linear range of air velocity and temperature. A typical performance curve is shown in Fig. 1, where two set points of air velocity and temperature (v_1, T_{AF1}) and (v_0, T_{AF0}) are chosen as firing points for a control circuit. For best linearity, the thermal resistance of the thermistor should vary linearly with air velocity in the given enclosure.

Figure 2 shows the basic sensing circuit. In general, a resistance element R_2 is placed in series with a thermistor and a constant-voltage source V_T. We sense the voltage V_2 across resistor R_2. The thermistor produces the firing voltage V_{2F} when its resistance reaches some value R_F corresponding to a thermistor temperature of T_F.

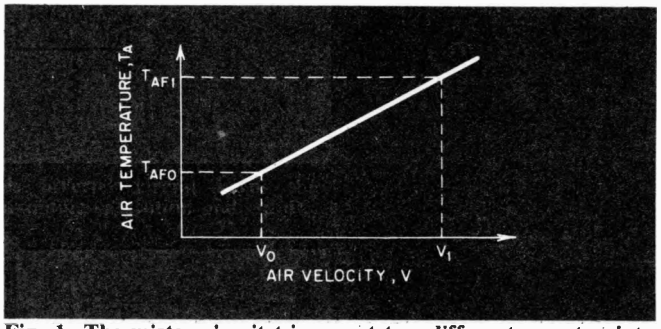


Fig. 1. Thermistor circuit triggers at two different preset points. With zero air velocity it fires at T_{AF0} and with normal air velocity it fires at a higher temperature T_{AF1}.

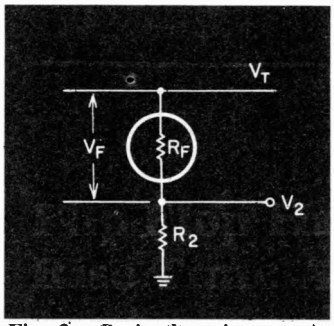


Fig. 2. Basic thermistor sensing circuit. Output V_2 can be used to trigger a breakdown diode, or R_2 can be replaced by a relay.

In a practical circuit, element R_2 may be a relay which fires at a constant current I_F, or it may be a resistor across a semiconductor device whose input current is much less than I_F. Of course, the thermistor's voltage, current or resistance can be considered constant depending upon whether $R_2 \gg R_F$, $R_2 \approx R_F$, or $R_2 \ll R_F$, respectively.

Referring again to Fig. 1, the difference in temperature between the two set points depends on the difference in thermal resistance ($\theta_0 - \theta_1$) of the thermistor at the two different air velocities. The change of temperature also depends on the constant electrical dissipation W_F in the thermistor.

Then,

$$T_F - T_{AF1} = \theta_1 W_F \quad (1)$$

$$T_F - T_{AF0} = \theta_0 W_F \quad (2)$$

Therefore,

$$T_{AF1} - T_{AF0} = (\theta_0 - \theta_1) W_F \quad (3)$$

From the equations, we can see that to achieve maximum sensitivity to change in air velocity, with any given enclosure, we should make W_F as high as possible. We can decrease the lower operating temperature T_{AF0} by insulating the enclosure on the outside (while allowing forced air inside to cool the thermistor). To decrease the higher temperature T_{AF1}, we can impede the flow of forced air

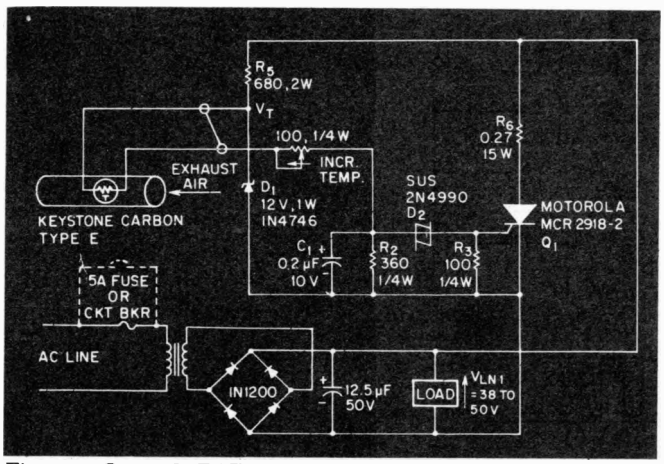


Fig. 3. One of EAI's power supplies uses a temperature-velocity circuit for protection. The SCR fires, blowing the fuse, if ambient temperature becomes excessive or if the forced-air supply fails.

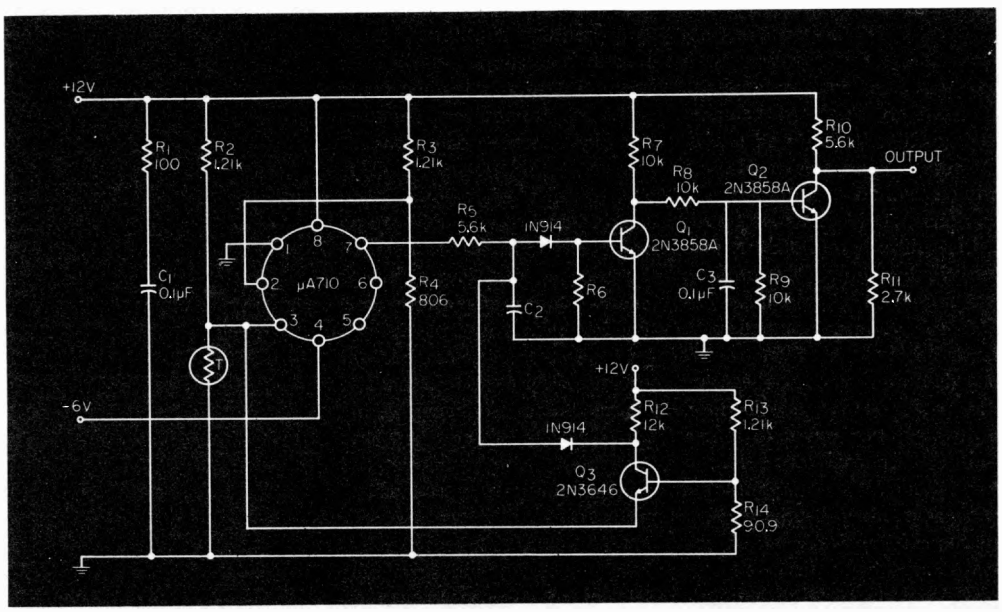
(while keeping the still-air insulation unchanged).

Figure 3 shows how this type of temperature-velocity sensor is used to protect an EAI power supply. The circuit interrupts the ac line if the fan fails, if the air flow is obstructed, or if the incoming temperature is higher than 50 degrees C at full load.

Because, in this supply, the transformer connections are adjustable for 115 or 230 volts, it was found convenient to operate the sensor circuit on an unregulated output V_{LN1} whose voltage is always somewhere in the range 38 to 50 volts dc. When the sensor fires, the breakdown diode conducts and triggers the SCR. The resulting overload then blows the fuse in the ac line circuit.

The sensor monitors exhaust air, and it triggers the SCR when the thermistor temperature at rated velocity v_1 is above $T_{AF1} = 65°C$, or when its temperature at zero velocity v is around $T_{AF0} = 30°C$.

Fail-safe temperature sensor



Temperature-sensing circuit gives an output pulse if the thermistor is shorted or open circuited.

MANY INDUSTRIAL control systems require a temperature-sensing circuit that must be fail safe. The circuit must not only give an output pulse when the temperature reaches a predetermined critical value, but must also give an output pulse if the sensor element opens or shorts. This output pulse then shuts down the system.

The circuit shown here, meets all the above specifications. It was designed for use with a PTC thermistor having a resistance of 30 Ω from 32°F to 160°F and 800 Ω at the critical temperature of 200°F. At 200°F the circuit gives a negative output pulse. The circuit distinguishes between a shorted thermistor and a normal one with 30- Ω resistance.

A wide range of different operating temperatures can be obtained by choosing a suitable temperature sensor and selecting the appropriate values for R_2, R_3 and R_4.

The μA710C IC operates as a differential comparator. When the thermistor resistance increases to a value such that the voltage across it is greater than the voltage across R_4, the IC produces a pulse at pin 7. Transistors Q_1 and Q_2 condition this pulse, to give an output with correct amplitude, impedance and phase. Components R_5 and C_2, filter out spurious pulses triggered by input noise.

Normally, transistor Q_3 is biased off. This stage initiates an output pulse if the thermistor is either open circuited or shorted.

If the thermistor opens, the emitter-base reverse-breakdown voltage of Q_3 is exceeded. The transistor then clamps pin 3 of the IC to around 7.5 V. This protects the IC from damage and also generates a pulse at the output.

If the thermistor resistance is less than 30 Ω, the base-emitter junction of Q_3 is forward biased and the transistor conducts. This turns off Q_1, causing a pulse at the output.

With the components specified, the circuit has an operating-point stability of ±0.5°F for ambient temperatures in the range 0-60°C. This is achieved by using 1% resistors for R_2, R_3 and R_4. These resistors should have a temperature coefficient better than ±50 ppm/°C.

Resistors R_{13} and R_{14} should also be low-tempco types to minimize temperature drift of the base voltage of Q_3. This ensures that the fail-safe circuit works reliably with the specified thermistor variation of 30 Ω. Component values are selected as follows:

Resistor R_4 is dictated by the resistance curve of the thermistor. Resistor R_3 should be as low as possible to minimize variations of IC leakage current with temperature. But the minimum value of R_3 is determined by the maximum-allowable input voltage for the IC. Of course, R_2 must be equal to R_3. The values for the voltage divider R_{13}, R_{14}, are selected to ensure that Q_3 turns on when the thermistor resistance is less than 30 Ω.

Pulse-width discriminator

THE CIRCUIT described here provides an output pulse whenever the input pulse width is either less than a minimum value, or greater than a maximum value. The circuit will also function as a pulse-width error detector by providing error pulses of width equal to the amount that the input pulse width deviates from the allowable limits.

In the block diagram of Fig. 1, a pulse width T is applied to point A. The leading edge of the pulse is delayed by a delay gate (½ SG83) to avoid racing problems with the leading edge of the pulse generated by the Maximum-Pulse-Width One-Shot. This non-critical delay is usually 10 or 20% of the nominal input pulse width. The triggering pulse which drives the two one-shots is derived from the leading edge of the input pulse. The left half of Fig. 2 shows the maximum-pulse-width waveforms. Note that a pulse will appear at point F if T is greater than T_{max}, the maximum allowable pulse width. The width of this pulse at point F will equal $T - T_{max}$.

The minimum-pulse-width waveforms are shown at the right in Fig. 2. The second delay gate (½ SG83) is used to avoid leading-edge racing problems at points D and E. Note that if T is less than T_{min}, the minimum allowable pulse width, then a pulse will appear at point G. The width of this pulse will equal $T_{min} - T$.

The last NOR-gate provides a general indication any time the input pulse width is outside the test window.

An example of a circuit developed for measuring 2-ms pulse widths within a test window of ±10% is illustrated in Fig. 3. The maximum allowable pulse width is calibrated simply by applying 2.2-ms pulses at point A using a precision pulse generator and trimming R_2 to adjust the Maximum-Pulse-Width One-Shot until a pulse just appears at point H. The minimum allowable pulse width is similarly calibrated by applying 1.8-ms pulses at point A and trimming R_6 to adjust the Minimum-Pulse-Width One-Shot until a pulse appears at point H. ■

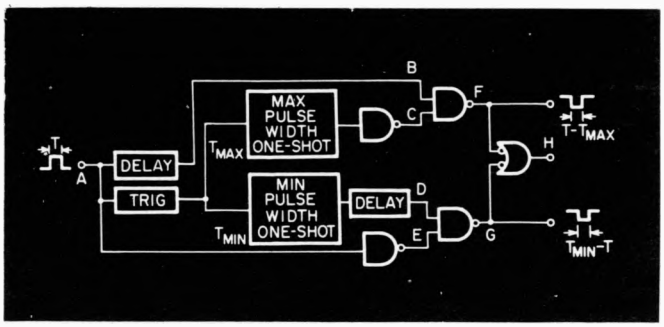


Fig. 1. Pulse-width discriminator in block-diagram form.

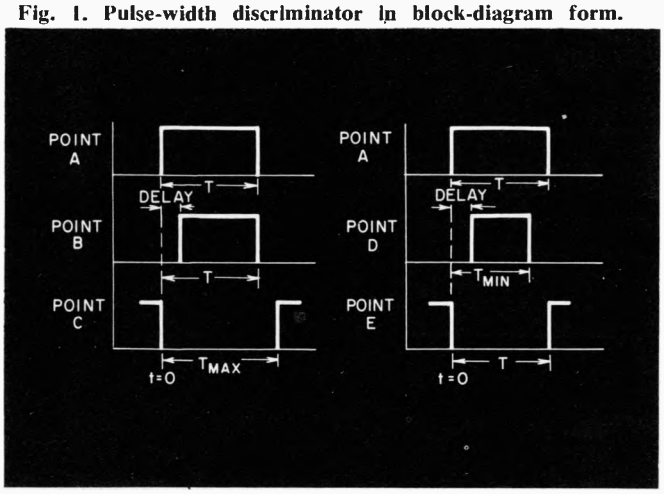


Fig. 2 Waveforms for maximum (left) and minimum (right) pulse widths.

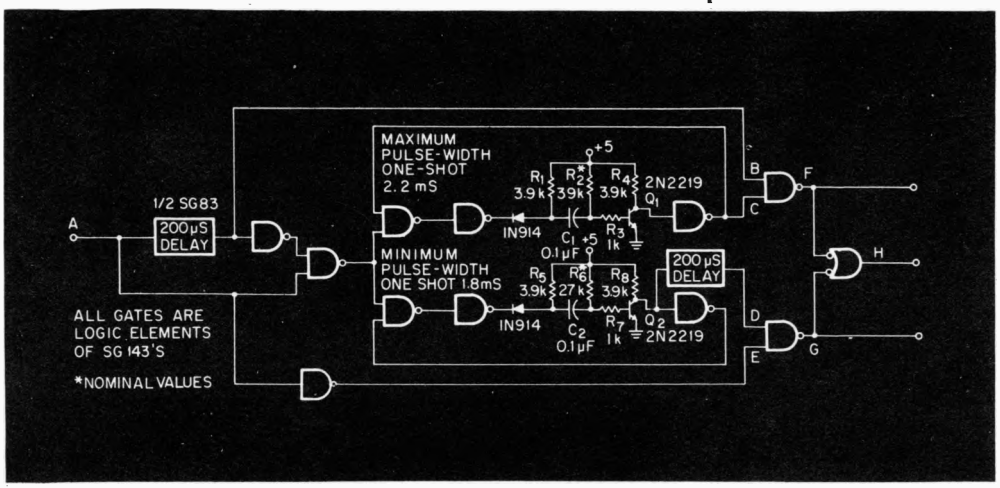
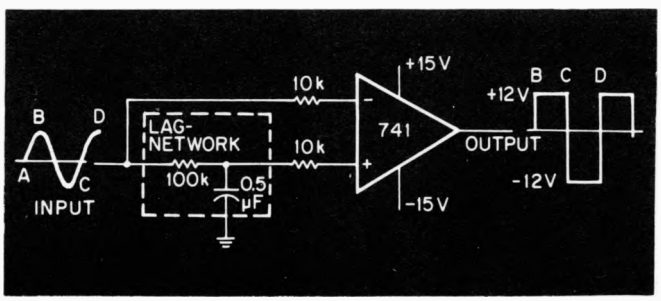


Fig. 3. Circuit for measuring 2-ms pulses with a ±10% window.

Change-of-slope detector

AN OPERATIONAL amplifier with a lag network can be used to detect a change in slope of most periodic waveforms. Any dc component present will not affect the operation of the Detector, providing the dc level remains within the voltage limits of the op amp. A distorted signal can be detected provided that the irregularities in the distorted signal do not reverse slope at too high an amplitude. If this does occur, then additional filtering in the input line is required to make use of the fundamental frequency of the signal.



High and low output levels indicate changes in slope of an input signal, regardless of input level over a wide range.

During the time interval between B and C, the voltage at the non-inverting input will be slightly higher than that at the inverting input because of the phase lag of the signal to the non-inverting input. Therefore, the output of the op amp will be driven into positive saturation, approximately +12 Vdc.

When the slope of the signal changes to the time interval between C and D, the voltage at the non-inverting input will become slightly lower than that at the inverting input. The output will then be driven into negative saturation, or approximately −12 V.

The output signal now indicates the change in slope in a form useful to drive a FET or MOS switch or it can be converted to a 5-volt signal.

The lag network has a time constant of 50 ms and is useful over a frequency range of 0.1 to 10 Hz with approximately a ten percent time shift in the output signal. For any one frequency, the lag network can be tuned to the exact time of occurrence of the change in slope. For lower frequencies the time constant must be increased and for higher frequencies the time constant must be reduced. ■

Peak detector for very narrow pulses

THE CIRCUIT HERE will deliver a dc voltage that's proportional to the peak amplitude of very narrow pulses with duration down to about 10 nanoseconds.

The amplitude of a negative-going input pulse is compared to an arbitrary reference voltage applied to the inverting input of a differential-input gate, the MC 1035. If the pulse amplitude is more negative than the reference, a positive-going pulse appears at the inverting output.

This positive pulse is applied through an MC 1023 line driver to the reset input of the MC 1027, a J-K flip-flop wired as an astable multi whose output width is determined by the value of C_1R_1. The values shown in Fig. 1 give a width of about 500 ns.

This relatively long pulse is amplified, level translated and inverted by Q_1, whose output turns on Q_2, whose collector current charges C_2.

The collector voltage of Q_2 will have a negative value that does not exceed V_{EE}. It should remain essentially constant when there is no input pulse. Therefore, R_2C_2 should be greater than the period of the input pulse. The voltage across C_2 is isolated from the output-current amplifier by a JFET used as a source follower.

The output, a negative voltage proportional to the voltage across C_2, is fed back to the inverting input of the first gate to become the arbitrary reference. This output rises with each input pulse until equilibrium is reached when C_2 stops charging.

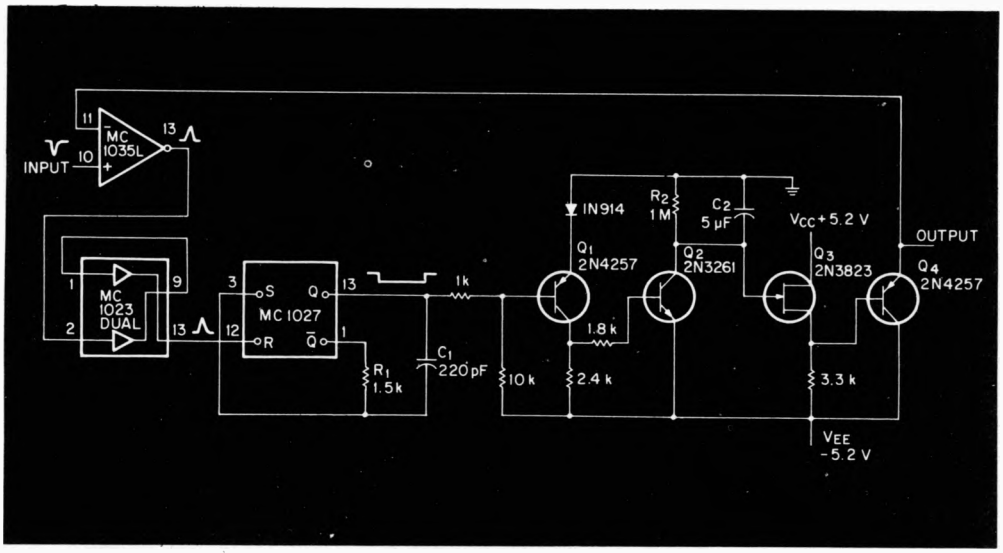


Fig. 1. This circuit responds to the peak amplitude of narrow pulses and is insensitive to their widths.

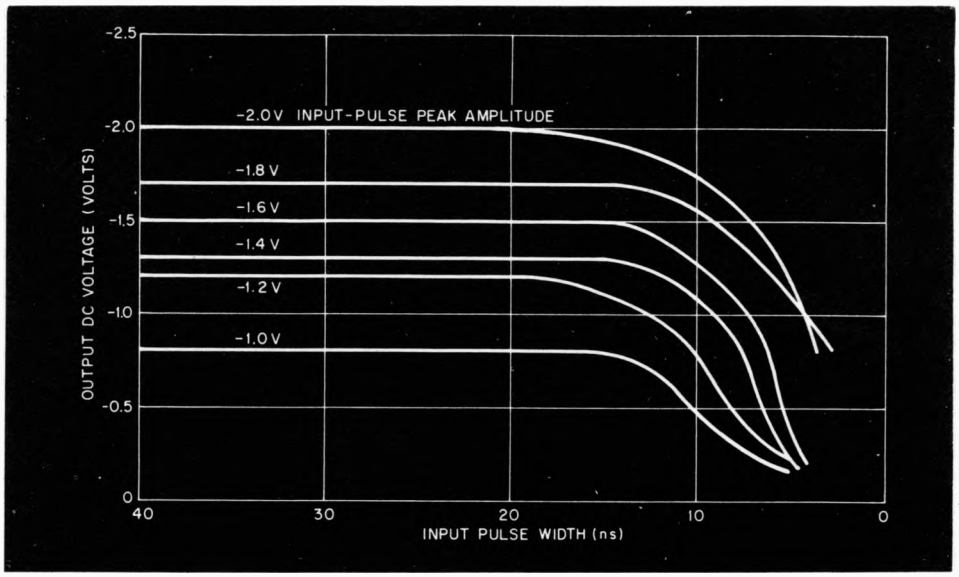


Fig. 2. When an input pulse lasts longer than about 10 ns, the output dc is proportional only to pulse-peak amplitude.

As shown in Fig. 2, the output amplitude is a function of input peak only, not input width. The lowest input-pulse amplitude determines the shortest usable pulse. The work done was performed with a pulse rep rate of 6.25 kHz.

A regulated ±5.2-V power supply is used. The negative supply must be able to deliver up to 100 mA, while the positive supply must deliver up to 10 mA.

The ICs used in the circuit are part of Motorola's MECL II family. The 1035 and 1027 have maximum prop delays of 8 ns while the fastest member of the family, the 1023, has a maximum prop delay of 3.5 ns. ■

Tunnel diode minimum pulse-width detector

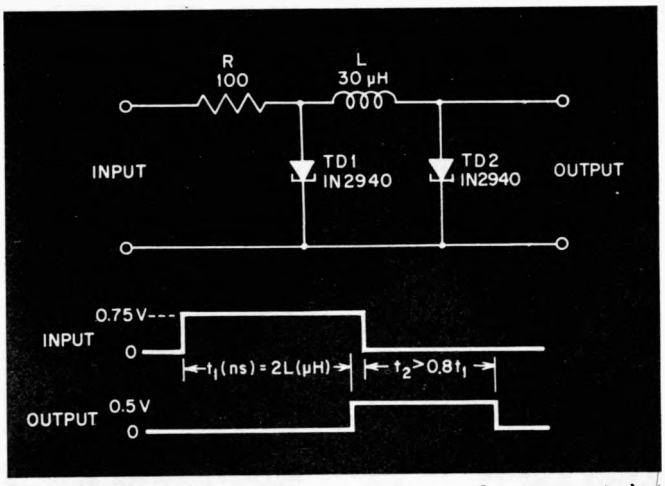
MINIMUM PULSE-WIDTH detectors have often been designed around IC monostables, UJT oscillators and discrete monostables. The circuit illustrated uses tunnel diodes for this purpose and has the advantage of being extremely simple, pulse-powered, predictable and fast.

Referring to the schematic, the input pulse current thru R will switch the tunnel diode (TD_1) to a high voltage state. In this state TD_1, becomes a a relatively constant charging voltage source for the inductor. The constant voltage across the inductor (TD_2) in its low voltage state) causes an inductor current that increases linearly with time. If the input pulse is shorter than the selected minimum width, the inductor current will not reach the level necessary to switch TD_2. If the pulse is longer than the selected minimum width, the inductor current will increase and switch TD_2 to the high voltage state. At the termination of the pulse, TD_1 will return to its low voltage state but TD_2 will remain in the high voltage state until the inductor current decays below the TD_2 valley current. The tunnel diode switching characteristic provides precise resolution (estimated at one nanosecond) while the charged inductor forces a minimum output pulse width. The circuit will not generate a partial output for a borderline pulse width.

The input pulse amplitude must provide a current through R greater than the sum of the valley and peak currents of the tunnel diodes. The minimum pulse width is a linear function of the inductance and is approximately the product of the inductance and TD_2 peak current divided by TD_1 peak voltage. For the circuit shown, this reduces to

$$t \approx 2L \text{ or } 60 \text{ ns.}$$

where t is in nanoseconds and L is in microhenries. ■

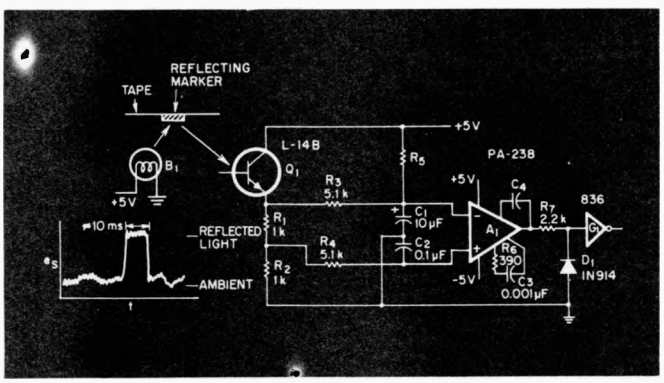


This pulse-width detector uses a minimum of components but operates at high speed.

Optical tape-marker detector

DETECTING beginning and end markers on digital magnetic recording tape is often difficult because of varying ambient light conditions and blank tape reflections. Manually adjusting the sensitivity of the light detector is not a practical solution. This self-compensating sensor does the job automatically by comparing short-term light variations (the signal pulse) against long-term variations (ambient light) in order to detect the presence of the desired signal.

In the diagram B_1 is a light source which illuminates the moving tape. Q_1 is a phototransistor which detects the light reflected from the tape marker. R_3C_1 is a low-pass filter having a time constant of about 5 times the expected incoming pulse width (10 ms). The filter stores the long-term light level without reacting to the short signal pulse. R_4C_2 is a low-pass filter with 1/20 the time constant of the incoming pulse width. This filter reduces spurious noise without deteriorating the incoming pulse. R_5 provides a slight positive bias to hold the output of A_1 in negative saturation. R_7 and D_1 provide a level conversion for DTL-gate G_1. ■



A phototransistor, op amp and DTL gate are used to construct an optical end-of-tape sensor.

High-speed synchronous detector

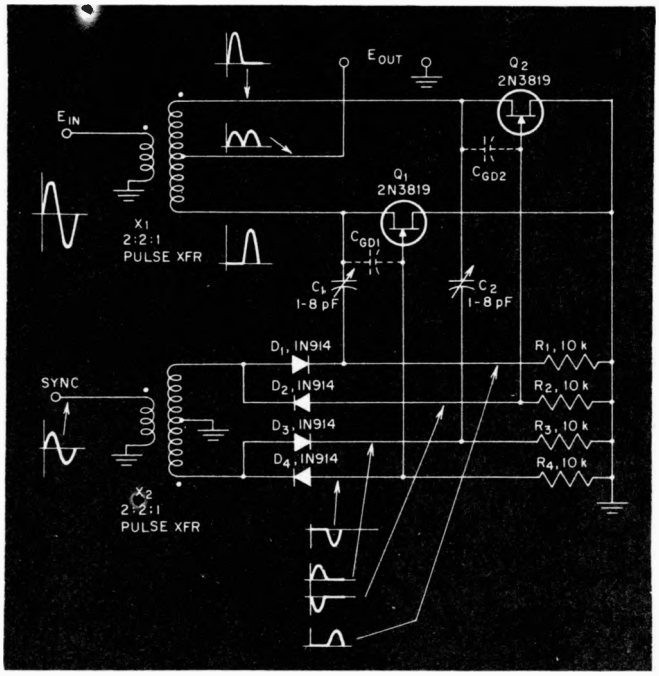
FET OR BIPOLAR-TRANSISTOR choppers cause problems in most synchronous detectors because of gate-to-drain or base-to-collector capacitance. In the FET chopper, for example, the capacitance allows the gate-drive sync signal to enter the drain circuit. This is particularly troublesome at high frequencies and low-input-voltage levels.

A simple solution lies in producing a signal of opposite polarity to the sync signal and feeding it to the drain (in the FET case) through a capacitance that's exactly equal to the gate-to-drain capacitance. This cancels sync feedthrough from gate to drain.

In the circuit shown, the signals at the D_1R_1 and D_2R_2 junctions are equal in magnitude to and 180° out of phase with the sync signals at the gates of Q_1 and Q_2 respectively. If C_1 is made exactly equal to the gate-to-drain capacitance of Q_1, the signals passing

through C_1 and C_{GD1} will cancel and eliminate feedthrough. A similar situation holds for Q_2.

These adjustments are best made by adjusting C_1 and C_2 for zero output with the sync signal present and the input voltage absent. The circuit shown has a dynamic range of 80 dB at 100 kHz. ■



Capacitive feedback of gate signals eliminates forward sync-signal feedthrough, boosting synchronous-detector frequency capability.

Section 16
DISPLAY & READOUT CIRCUITS

Photo Reader for Perforated Tape

THE HEART of this photo reader is the photo sensitive diode *CR*1. This makes use of the fact that the back resistance of a diode changes with light intensity. In this circuit a standard silicon junction diode 1N676 was used. It was necessary to remove the paint covering the glass case to allow the light to reach the junction. Commercially available photo diodes would have been used, but none were on hand at the time. The circuit was developed for reading perforated tape. A photo memory circuit was used to drive loads in order to keep the signal applied to the load until it is required to erase the memory.

When the photo diode is dark, the back resistance is greater than 10 megohms, and therefore, has little effect on the biasing of transistor Q_1. In the dark condition, the sensitivity potentiometer R_1 is adjusted to give a positive bias such that Q_1 is conducting to a point where the collector voltage is approximately —10 volts with respect to ground. The Shockley diode CR_2 is in the nonconducting condition and is therefore high resistant. The —10 volts on the collector of Q_1 passes through R_4 and sees the high resistance of CR_2 and the high back resistance of CR_3. Diode CR_2 requires approximately 40 volts drop across its terminals to cause it to conduct. In the dark condition, there are —10 volts on the cathode and +28 volts on the anode. A potential drop of 38 volts across CR_2 is not enough to cause it to breakdown.

When light is applied to CR_1, its back resistance drops from greater than 10 megohms to approximately 200K ohms. With the total resistance in the base circuit less than 200 K, transistor Q_1 will conduct more and its collector voltage will drop to less than —12 volts. Thus the voltage on the cathode of CR_2 will drop below —12 volts and cause it to break down since the drop across it exceeds 40 volts. When CR_2 breaks down, the current path will be from the +28 vdc supply through the load, CR_2, CR_3, Q_2, and on to ground return. Diode CR_2 will remain in the conducting condition and thus act as a memory as long as the current does not drop below the required holding current (5 to 10 ma on the 4D40 diode used).

Transistor Q_2 is biased on from the +28 vdc supply through R_5. It will stop conducting when ground is applied to its base and therefore acts as a memory erase. Diode CR_2 will go back to the high resistance condition and no current will be supplied to the load. The purpose of R_4 is to apply enough resistance such that less than minimum holding current (5ma) required to keep CR_2 broken down would be allowed to flow through R_4 and Q_1 when Q_2 breaks the current path.

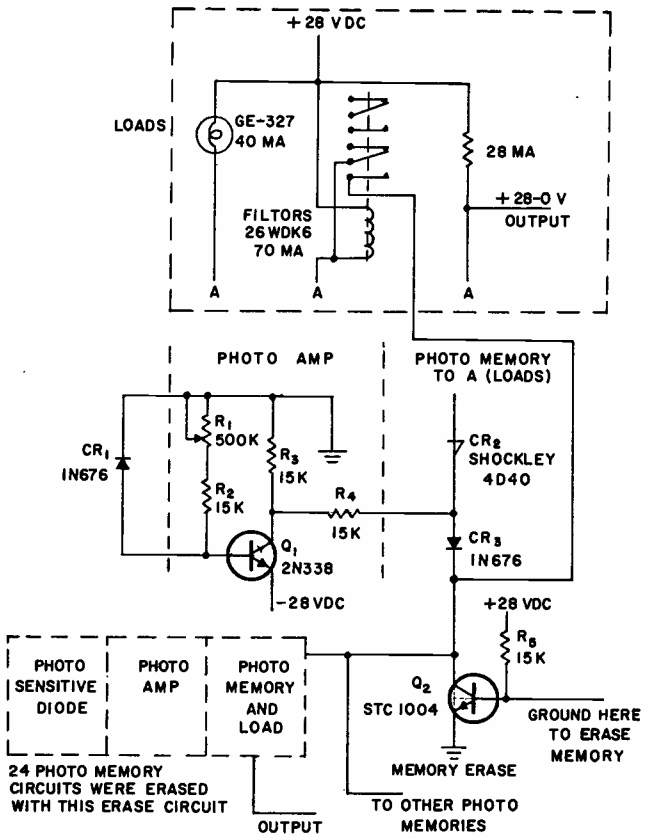
The requirements on Q_2 are that it be low resistance (approximately 1 ohm saturation resistance for STC 1004) such that the activation of a photo memory circuit will not activate or deactivate other photo memory circuits using the same memory erase circuit. As many as twenty-four photo memory circuits were erased with the memory erase circuit with good results.

The three loads shown were used depending on the application required. Using the lamp as a load could have application in verifying punch tape. The relay load could be used to control a circuit where it is necessary to handle large currents. The relay used draws more current than CR_2 is capable of handling for continuous operation, therefore, once CR_2 allows enough current to pass to activate the relay, one set of relay contacts is used to keep the relay latched.

The resistive load is applicable where it is desired

to drive logic circuits with a "1" or "0" using 0 to 28 vdc, respectively.

Various junction and point contact diodes of the glass case type are painted black, and it was required to remove the paint to get light to the junction. All of the diodes tested showed extremely noticeable changes in the back resistance with light



Diode CR_1 is a conventional silicon type with paint removed to allow light to reach junction.

intensity. For more sensitivity, a lens was used to focus the light in the junction area. There are commercially available photodiodes, such as TI 1N2175, with small focusing lens built in.

Inversion Technique for Incandescent Lamp Readouts

IN SWITCHING circuits, incandescent lamps are frequently used for indication of the various circuit outputs. When only a single-pole single-throw switching output is available (e.g. an spst switch, a single relay contact, an scr, or a transistor), a problem arises if a lamp output is required with the switch open or if two lamp outputs are required (one lamp lights for the switch open and one lamp lights for the switch closed). The usual approach to the problem is to add an inverting element such as a transistor switch or a relay.

A solution to this problem, which has proved superior to other possible solutions in several applications, is shown in Fig. 1. The circuit uses an scr, but other switching devices can be used in a similar manner. In this circuit, all lamps are the same type. With the scr off, the two upper lamps in parallel supply current to the lower lamp. Since the resistance of a lamp is much higher when operated at rated current and voltage than it is at lower current or voltage, the resistances of the two upper lamps, L_1 and L_2, will be much less than the resistance of the lower lamp, L_3, and, consequently, a large fraction of the supply voltage will appear across L_3 causing it to light. When the scr is on, the major part of the supply voltage will appear across L_1 and L_2 and consequently they will light. If indication with L_3 only is desired, the two upper lamps, L_1 and L_2, can be shielded.

This circuit was tested with type 39 lamps rated at 6.3 v and 0.36 a. With the scr off, the voltage across L_1 and L_2 was 0.8 v with 6.3 v across L_3. There was no visible light output from L_1 and L_2 under this condition. With the scr on, there were about 6.3 v across L_1 and L_2, and there was no visible output from L_3. The chart shows the advantages of this method compared with the resistor in series with the lamp from the standpoint of power efficiency.

Circuit	Power Dissipation SCR off	SCR On
Circuit of Fig. 1	2.5 w	5.1 w
Circuit with Series Resistor	4.5 w	8.5 w

Considering the lower power required, together with the more effective dispersion of heat by a lamp, the superiority of the circuit of Fig. 1 is evident.

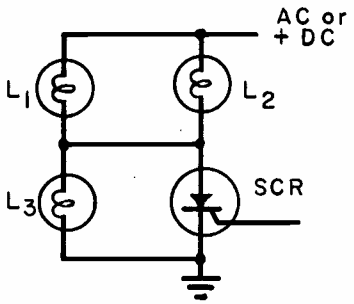


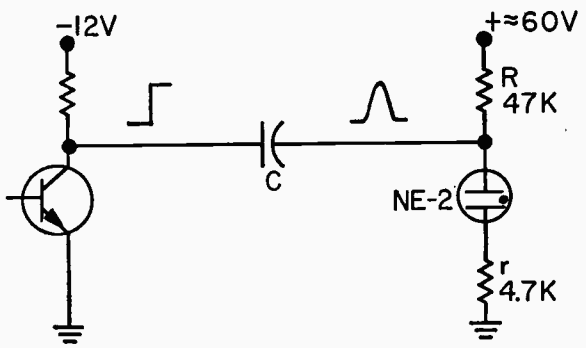
Fig. 1. Basic inversion circuit for incandescent lamp readout.

An alternate approach to this problem would be to use a single lamp in place of L_1 and L_2 in Fig. 1. This lamp, if it is twice the current rating and the same voltage rating as L_3, should produce equivalent results.

Low-Voltage Transistors Drive Neon Readout

THIS SIMPLE, neon-readout system does not require high-voltage transistors. In fact, it can be driven directly from register flip flops. It requires small currents for the neon and it needs very few components.

In operation, the neon's supply voltage is adjusted to lie between the striking and extinguishing potential of the neon. When one transistor of the flip flop turns on, we can assume that a positive-going pulse must be directed by the neon tube's turning on. As shown in the figure, capacitor *C* couples the pulse to the tube in such a way that the sum of the pulse height and the supply voltage is sufficient to fire the neon. Consequently, a pulse height of only 6 to 12 v is necessary to drive the neon.



Small voltage changes are adequate to drive this neon readout.

As the flip flop turns off, a negative pulse reduces the tube voltage below the extinguishing point and turns it off. (It should be noted that, unless the flip flop has made at least one transition, this readout, being ac coupled, will not necessarily indicate the correct state. But this is generally no problem.)

Multitrace Display Device

To permit the measurement of certain pulse parameters between fixed voltage levels in the presence of oscilloscope gain instability, shifting baseline levels, and random line voltage fluctuations, the circuit of Fig. 1 may be used. The circuit allows simultaneous presentation of the pulse under consideration, and of the limit voltage levels, without requiring frequent laborious checking and calibration of the display instrument.

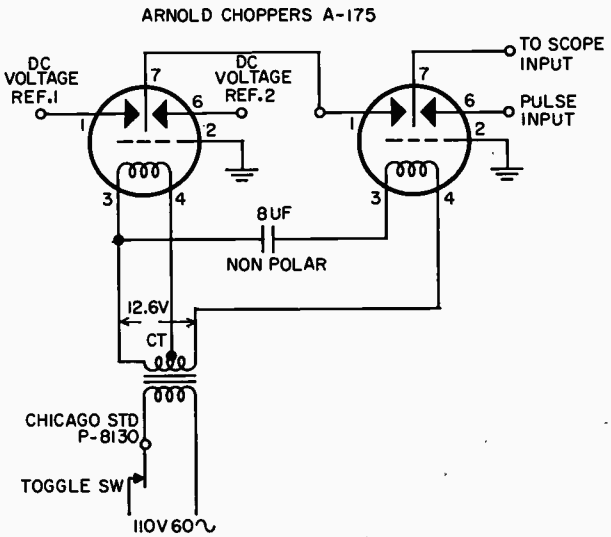


Fig. 1—Multitrace display.

Two A-175 60 cycle, 6.3 v choppers operated approximately 45 degrees out of phase are employed. The first chopper switches alternately between the two set voltage levels; the output of this chopper is then combined, through the second chopper, with the pulse signal. Ideally, the two choppers should operate precisely 90 degrees apart to ensure equal brightness of all the elements of the composite display. The simple phase shifting circuit used here provides approximately 45 degrees phase difference, but the resultant intensity variation is not objectionable.

A requirement for the proper operation of this device is that a pulse repetition rate or an oscilloscope sweep speed be high enough to prevent the appearance of the 60 cycle switching pattern.

Transistor Matrix for BCD-to-Decimal Indicator

Incandescent-lamp decimal indicators that operate from a binary-coded-decimal (BCD) source require some means of BCD-to-decimal conversion. This is usually done with a diode decoder matrix and with transistor drivers for the lamps. For 8-4-2-1 weighted code, a minimum of 30 diodes and 10 transistors would be required with this technique. An alternative circuit that uses only one diode and 18 transistors is shown in Fig. 2. This circuit is similar to the relay switching tree shown in Fig. 1.

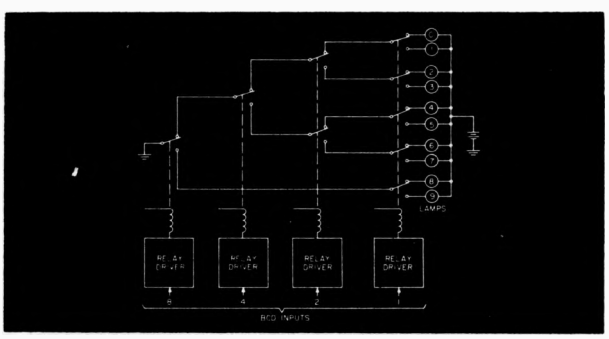


Fig. 1. Relay BCD-to-decimal converter.

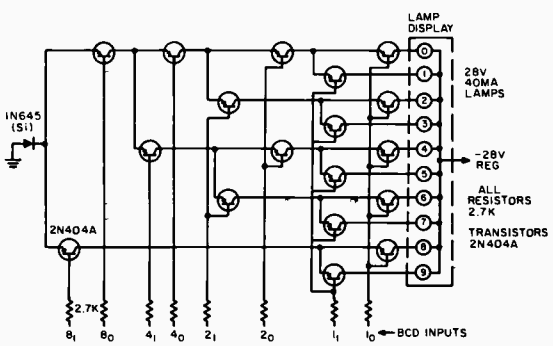


Fig. 2. Transistor BCD-to-decimal converter.

The 1N645 silicon diode provides a common bias for the transistor tree. A given transistor tends to be turned on when a logic *1* (—6 v) is supplied to its base input circuit from the BCD source, which is assumed to be a counter or shift-register stage. A logic *0* is represented by approximately ground potential (saturated collector-

to-emitter drop), and holds a given transistor off.

The use of a common base resistor for each BCD input provides economy in the number of components, but is a disadvantage at higher temperatures since it must handle the combined I_{co} of the bases. Separate base resistors would have to be used for reliable operation at temperatures above 40°C.

For any possible decimal combination for the 8-4-2-1 weighted BCD input, only one closed gate path is possible through the transistors from ground to the correct light. Approximately 2 ma of current drain is required from each logic *1* input (it should be noted that base current is drawn only by those transistors forming the closed gate path).

Inputs from both collectors of each stage must be utilized. If the stage of weight four is in a "set" (logic *1*) condition, for example, then the 4_1 input would be −6 v, while the 4_0 input would be at ground potential.

Lamps rated at 28 v, 40 ma were used in a projection-type decimal indicator. The lamp supply voltage may be slightly higher than 28 v to compensate for the small voltage drop across the combined biasing diode and transistors, which amounts to less than 1 v.

Multi-Aperture Solar Cell Amplifier

THIS CIRCUIT is presently being used as a source of strobe pulses in a high speed commercial card reader. The input is connected to a long solar cell which is masked by an aperture plate having equally spaced windows to allow light to shine on the cell at the required strobe times. With a long, 10-aperture cell and one circuit, this scheme will generate 10 strobe pulses. Eight circuits and eight solar cells are required to generate the 80 strobe pulses needed when reading a conventional punched card.

A common-base input circuit is used so that the solar cell operates in its linear region. The base of Q_1 is biased at $-V_f$ of D_1 so that the emitter of Q_1 is essentially at 0 V, thereby minimizing cell leakage current. The maximum input current which the circuit can accept is determined by

$$I_{L\,MAX} + NI_A + \frac{V}{R_1} \leq \frac{V}{R_3} + I_{B2}$$

where $I_{L\,MAX}$ equals the cell leakage current, N equals the number of apertures uncovered and I_A equals the cell current generated each time an aperture is uncovered.

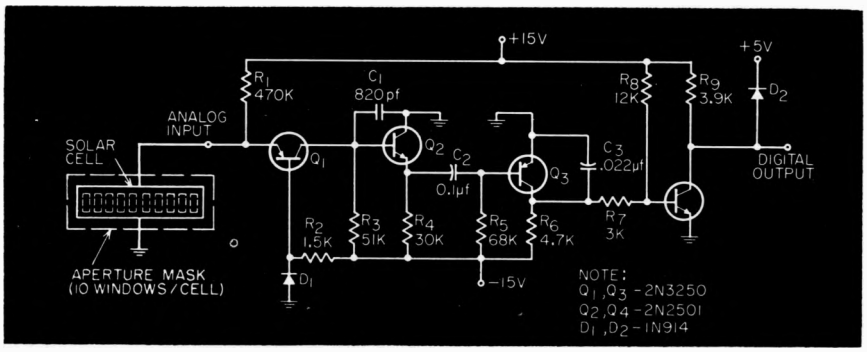


Fig. 1. Solar-cell amplifier for reading punched cards.

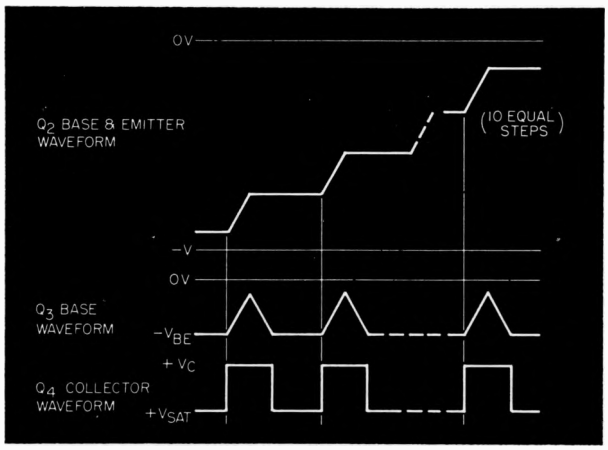


Fig. 2. Waveforms at critical points in the circuit.

Figure 2 shows waveforms at various points of the circuit. The waveform of the signal at the base of Q_3 consists of a series of voltage steps, where the changing portion is a linear voltage which changes by $I_A R_3$ in the time required to uncover an aperture. The flat part of the waveform between steps represents the time that it takes the card to travel between apertures.

In the remainder of the circuit, Q_3 is an emitter follower which has a high input impedance and is capable of driving the R_5C_2 differentiator. Q_4 is an inverter which amplifies the differentiated analog signal and drives the digital pulse shaping output stage, Q_5.

The purpose of C_1 and C_2 is to limit the frequency response of the amplifier so that noise, ever present in most electro-mechanical systems, will not generate digital output strobe pulses.

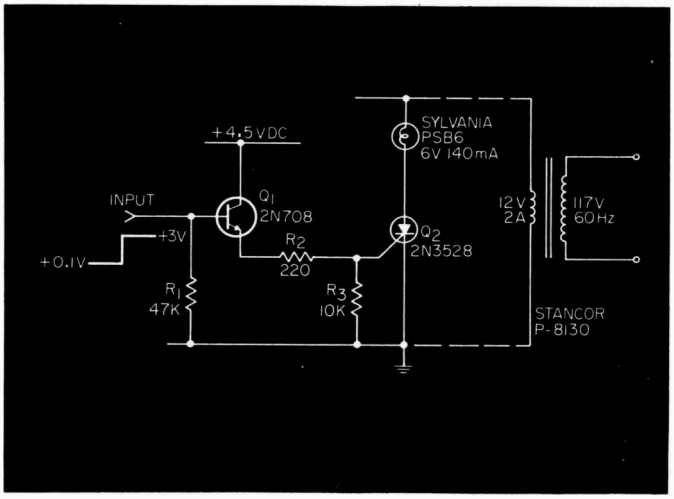
Readout Circuit for Digital ICs

USING SCR circuits, as shown here, you can indicate the state of binary circuits without using bulky power supplies. One 60-Hz transformer will supply many lamp-driver circuits. The circuit is controlled by standard logic levels.

A high input of 3 V (logical 1) supplies sufficient power to the gate of Q_2 through R_2 to cause the SCR to conduct on each positive cycle of the 60-Hz anode voltage. The lamp stays lit with half-wave rectified power as long as the input is at the high level.

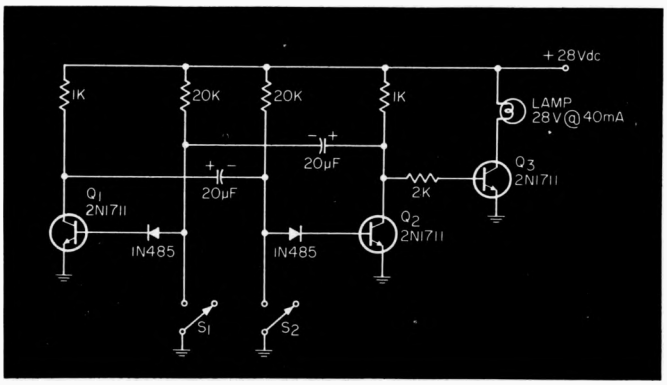
A low input of 0.1 V (logical 0) will not trigger the SCR and the lamp will not light. Current-amplifier Q_1 provides gate current to the SCR while drawing only about 0.2 mA at the input.

Because of its low input-current requirement, this circuit is an excellent readout for integrated circuits. No additional supply voltages are required. With the transformer specified here, as many as 14 stages can be driven simultaneously, with little reduction in lamp intensity.



Simple and efficient readout circuit is compatible with digital ICs. For clarity, only one stage is shown.

Three-State Indicator



With both switches open, this indicator circuit is a free-running multivibrator.

SOMETIMES it's desirable to indicate more than two circuit conditions using a conventional lamp. This indicator circuit gives three modes; on, off and blinking.

If switches S_1 and S_2 are both open, transistors Q_1 and Q_2 form part of an astable multivibrator. With the component values shown, the lamp blinks once every second.

If S_1 is open and S_2 is closed, Q_2 turns off allowing Q_3 to conduct. Thus the lamp stays on.

With S_1 closed and S_2 open, Q_2 conducts cutting off Q_3. Thus the lamp is extinguished.

The switches can be replaced by transistors or relays, depending on the application.

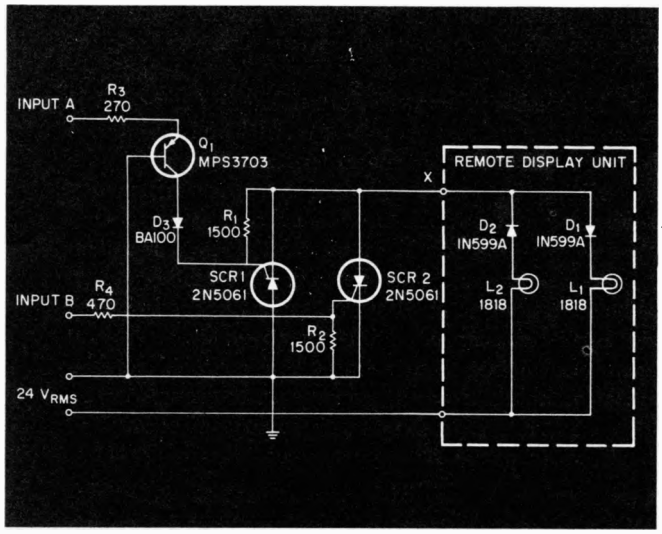
Lamp driver minimizes lines to remote display unit

WHEN IT IS necessary to locate multiple lamp displays at some distance from their drivers, this circuit can minimize the number lines to the remote lamp displays. For n display circuits, n/2 + 1 lines are required, that is one line for each two circuits, plus one common line.

The inputs are compatible with Motorola MRTL logic, and draw one loading unit current from their source. The SCRs and transistor are low-cost plastic devices. Using the Astrodyne #TR-118 spring cooler, each SCR will drive up to five #1818 lamps.

Current for L_1 is supplied by the 24-Vac source through SCR_1 and D_1. Half wave rectified power is supplied to the lamp. Current for L_2 from the 24-Vac source is supplied through SCR_2 and D_2. Therefore, at point X, positive half-cycles turn L_1 on, negative half-cycles turn L_2 on, and ac will operate both.

When input B is more positive than 0.8 V and the SCR_1



Low-cost plastic semiconductors are used in circuit that minimizes the number of drive lines required for remote lamp display.

anode is positive, it fires. R_3 limits the gate sensitivity to the minimum MRTL "on" voltage. Gate current for SCR_1 is supplied via D_3 and Q_1. When the SCR_1 cathode is negative, and the gate more positive than the cathode, it will fire. If Q_1 is on when the SCR_1 cathode and gate are negative, gate current will be supplied through D_3. Q_1 is biased on when input A is more positive than 0.8 V. Q_1 is a grounded-base level shifter. D_3 protects the gate of SCR_1 from large reverse voltages when the cathode goes positive.

Despite the fact that only half-cycles from a 24 Vrms source are supplied to the lamps, a 24 V lamp is used. When 14.4 lamps (#1813) were tried, life was unacceptably short due to excessive filament heating on the half-wave peaks, even though the average power supplied was the same as for 12 Vrms full wave. The 24-V lamps provide adequate brilliance for a translucent readout display and long life is assured. ■

Electronic dipstick

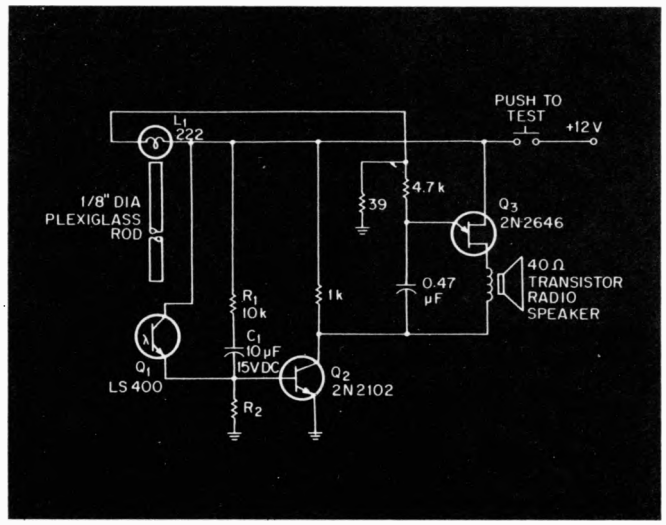
THIS CIRCUIT CHECKS crankcase oil level from the driver's seat. A plexiglass rod is attached to the dipstick and used to conduct light from lamp L_1 to the crankcase. This light is sensed by phototransistor Q_1 which is mounted at the "add oil" mark of the dipstick, about 1/2 in. below the bottom of the rod.

Depressing the test switch charges C_1 and saturates Q_2 for a short time. This activates the unijunction oscillator circuit of Q_3 and a short audio tone is heard. This verifies that the circuitry is functioning properly and that lamp L_1 is not burned out.

If the oil is low, light from the plexiglass rod is sufficiently attenuated so that the phototransistor's resistance will be high. After C_1 charges, Q_2 will turn off.

When oil is low, sufficient light reaches Q_1 to lower its resistance enough to keep Q_2 saturated after C_1 charges. In this case, a continuous tone will be heard as long as the switch is depressed.

The value of R_2 should be determined experimentally. A nominal value is 5kΩ. The plexiglass rod should be polished on the end near Q_1 for greatest light transmission and should be wrapped in foil for minimum light attenuation. The other end should be in contact with the lens of the lamp. Secure the phototransistor and the rod to the dipstick with RTV potting compound or high temperature shrinkable tubing. The sides of the dipstick may have to be filed to allow the assembly to fit in the dipstick hole. ■



Electronic dipstick uses phototransistor and plexiglass rod as sensors. A continuous tone signals a low oil level.

Section 17
GATING & LOGIC CIRCUITS

Gating With Varicaps

A 100-db "on-off" ratio of a 5.5-mc signal can be obtained using a small amplitude positive pulse gate with the circuit of Fig. 1. This ratio is accomplished by using two dual triodes with four tuned circuits with a varicap in each.

Figure 2 shows the gated 5.5-mc with the gate pulse superimposed. The time scale for both signals is 5 μsec/cm. The 5.5-mc is shown 0.1 v/cm and the gate pulse 1.0 v/cm.

The stages are initially tuned for a signal frequency of 5.5-mc. When a gating signal is applied at J_4, the parallel tuned circuit in each stage is shifted to series resonance since the gating voltage changes the bias on the varicaps and hence the capacitances C_3, C_9, C_{14}, and C_{19}.

The unique idea here is the performance of a gating function by detuning parallel resonant stages by switching to series resonant stages for the "on" and "off" conditions respectively. The gating signal for the "off" condition can be a relatively small amplitude (4 v) signal whose width can be anywhere from 20 μsec to dc. A negative pulse could be used by reversing polarity of the varicaps.

The gate input circuit must protect against the 5.5-mc feedback. For proper decoupling the capacitors in the pi network must be large. Good rise

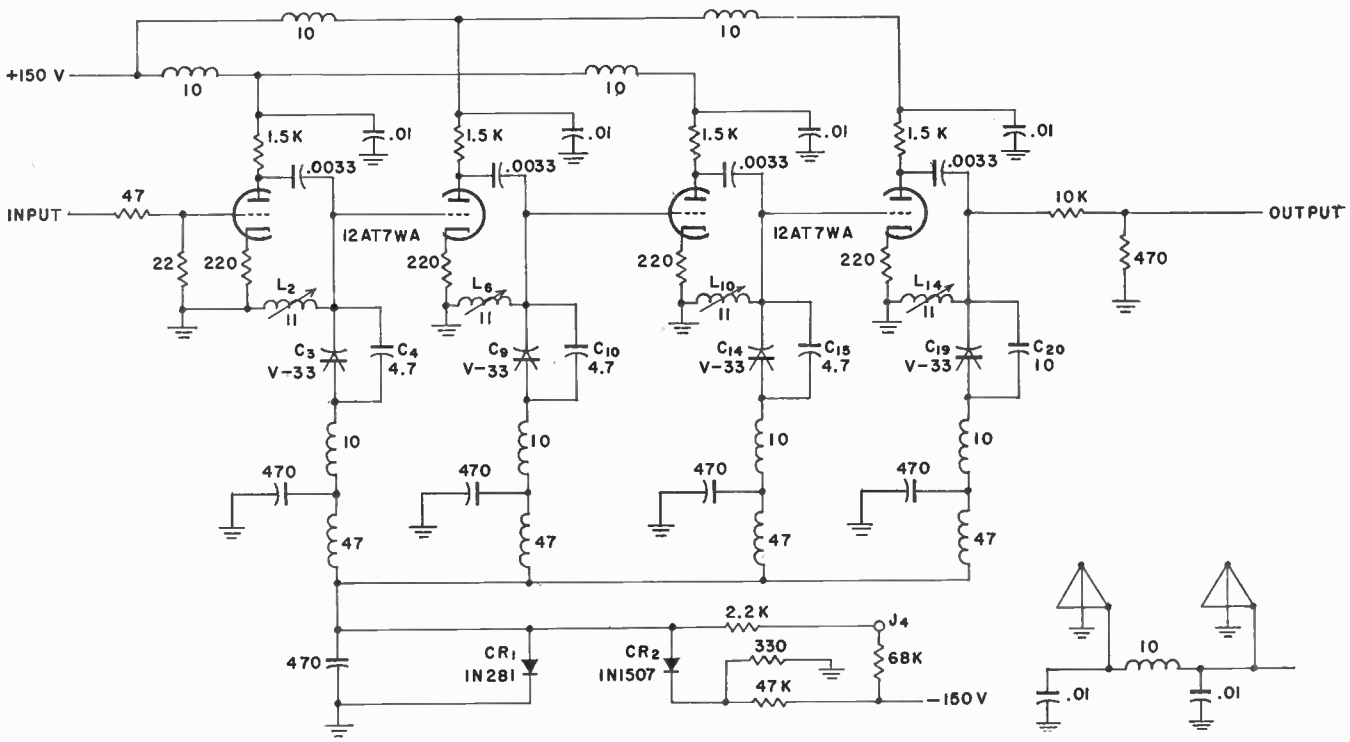


FIG. 1—Tuned circuits are shifted from parallel to series resonance by gating signal.

time and delay time of the gate pulse requires that these same capacitors be small and one capacitor is common to the four pi networks. CR_2, an International Rectifier zener diode, is used to protect the varicaps against a high bias condition and also to reduce the effects of voltage variations of the gate source during the "on" condition. The amplitude of the gating pulse must be greater than the zener voltage of CR_2. If a large gate pulse is available, CR_2 may be chosen with a higher zener voltage and the bias conditions made to agree. The zener voltage must not exceed 25 v. A 1N281 diode is used to speed up the gating action and to clean up the gated 5.5-mc signal output.

With a 500-kc bandwidth and a 5.5-mc signal the capacitance required for resonance (for L_2, L_6, L_{10}, L_{14} at 11 μh) would be 75 μμf. Assuming that the capacitance of the varicaps will be changed 50 per cent by varying the bias voltage across them, the new capacitance would be 37.5 μμf.

The new tuned frequency would then be 2.48 mc and for one tuned stage attenuation to 5.5 mc would be about 25 db.

The total amount of attenuation obtained (> 100 db) was accomplished by using four stages and by creating the series resonance during the

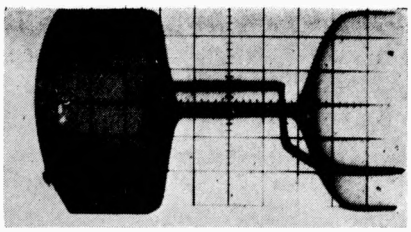


FIG. 2—Gated 5.5-mc signal with gate pulse.

off time. This series resonance condition gives the effect of infinite capacitance or a great degree of detuning of the tuned circuit.

Capacitors C_4, C_{10}, C_{15}, and C_{20} were shunted across the varicaps to eliminate the rectifying action of the semiconductor.

Over 100-db attenuation during the "off" time was achieved using only two low current tube types.

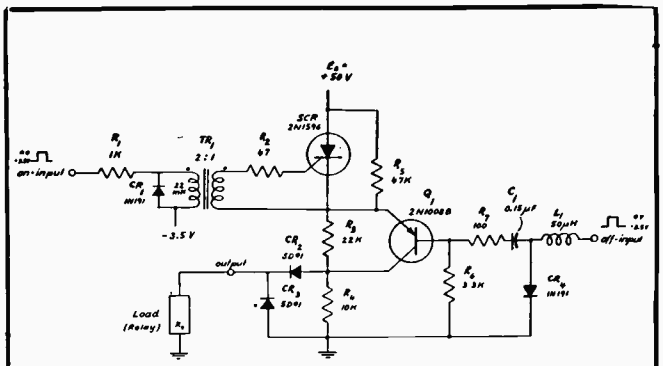
The temperature effects should be less than other standard circuits since fewer tubes are used and the varicaps, as used here, are very stable and non-aging. Thus greater reliability is achieved.

A small gate signal (approximately 4 volts) is sufficient to operate the circuit. With a slight modification an opposite polarity gate could be used instead of the positive gate used here.

There are no balance problems, no pedestals are created by the gate on the signal, and no loss of gain is incurred.

Power Control by Digital Pulses

A CIRCUIT was designed to control input and output units (card reader and card punch) of a



Logic levels of zero and —3.5 volts control 50-volt relay with this circuit.

data processing system. A 50-volt relay (internally connected to ground) of this unit was to be operated by logic levels of —3.5 volts and 0 volt.

Specifications called for no modification of the card machine used. The circuit shown in the diagram also had to be impervious to noise and voltage fluctuations within limitations.

The control of the load by pulses and the signal conversion to a different operating level make this solid state switch unique: In standby, Q_1 is on and draws approximately 1 ma (assuming $R_L << R_5$) shunting R_3 and staying at a slightly positive voltage level. A pulse arriving at the on-input will produce a positive spike at the gate of the silicon controlled rectifier whereby R_2 is limiting the gate current.

The scr will go into conduction and will remain in this state. The output now will rise to a voltage somewhat less than E_B, while the full load current flows through the scr and the saturated transistor Q_1. R_6 will provide sufficient base current to hold Q_1 on.

The leading edge of a pulse appearing at the turn-off input will produce a positive trigger at the base of Q_1, thus turning Q_1 off for a duration of 40 μsec at a specified load current of 250 ma. Since Q_1 turns off, the load current is forced to flow through R_3 and will, therefore, be reduced to less than 2.5 ma. Since the holding current of the scr is 25 ma, it will go out of conduction. The output voltage will drop immediately to almost ground level. Q_1 will turn back on and will establish the standby state of the circuit again.

CR_4 clamps the off-input to ground to protect the driver from positive voltages. R_7 damps peak voltages at C_1, occurring when scr turns on and thereby back biasing the emitter-base junction of Q_1 for a short instant of time. Observe low ac impedance path through scr, Q_1, R_7, C_1, and CR_4. CR_2, L_1 and TR_1 reduce noise and transients from the load (probable source) to the logic circuits.

Turn-on time of this switch is around 3 μsec, turn-off plus recovery time amounts to 2 μsec (at $I_L = 250$ ma)

Exclusive OR Uses One Transistor

WHEN the need for comparing two logic levels exists in a digital system, the "exclusive or" function in generally adopted. The circuits shown have the advantage over other types of circuits in that relatively few components are needed to perform this type of logic. These particular circuits are intended to be used with a 0 volt (ground) and —6 volt logic system. Most other logic levels can be readily adapted with only minor component value changes.

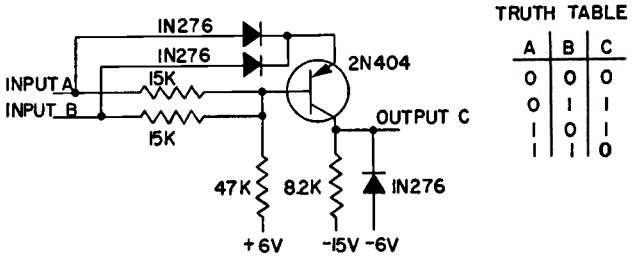
A pnp transistor is used in the basic circuit, Fig. 1, which produces logic "1" whenever the two inputs disagree. When one input is at logic "1" while the other is at logic "0", the logic "1" level is applied through the two diode gate to the emitter. The two diodes act as a conventional "or" gate with the transistor and its collector supply voltage.

With a logic "1" level at the emitter and a logic "0" level at one of the two base inputs, the transistor will conduct and produce the logic "1" output level. If both inputs are at the same logic levels, the transistor will not conduct since the emitter-base junction is reversed biased. The output at this time will be the clamp voltage which is logic "0".

When an npn transistor is used and the two diodes are reversed, as shown in Fig. 2, the circuit produces the complemented output logic. In this circuit the two diodes act as a conventional "and" gate with the transistor and its collector supply. Note the different supply voltages required for the npn transistor.

A variation of the basic circuit is shown in Fig. 3. When used as an Exclusive Or indicator, the neon lamp will glow whenever input *A* and input *B* are in agreement. This action takes place since at this time the transistor which shunts the NE-2 neon lamp is nonconducting, representing a very high impedance. When the two input logic levels are at opposite states, the transistor conducts, extinguishing the neon lamp due to the drop in the lamp's applied voltage.

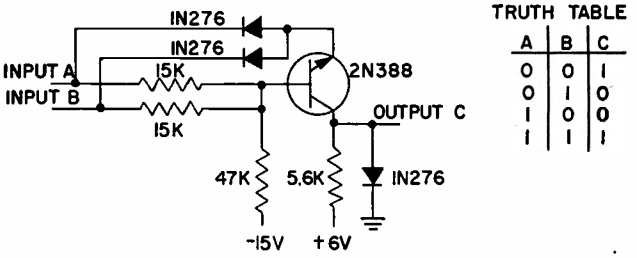
If it is desired to have the indicator follow only one control level, the other input can be placed at a fixed voltage. If the fixed voltage is made logic "0", then the lamp will turn off whenever the control input is at logic "1". Similarly, if the fixed voltage is logic "1" the lamp will turn off whenever the control is at logic "0".



TRUTH TABLE

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

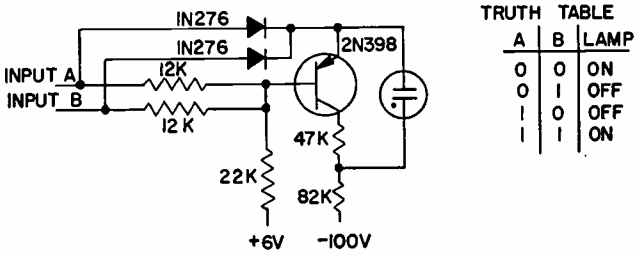
FIG. 1—Transistor conducts when inputs are different levels.



TRUTH TABLE

A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

FIG. 2—Logic circuit for use with an npn transistor.



TRUTH TABLE

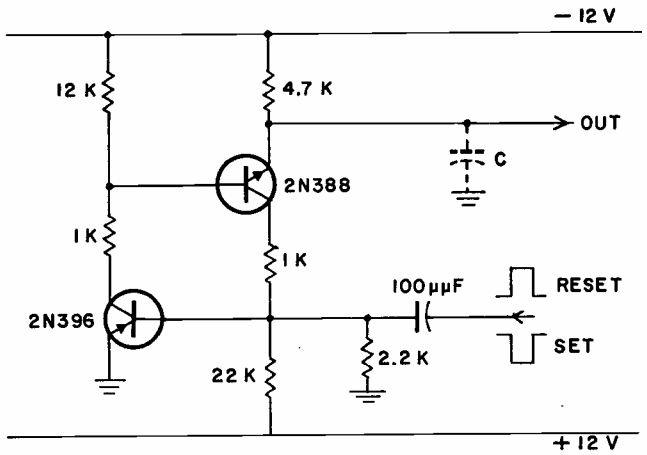
A	B	LAMP
0	0	ON
0	1	OFF
1	0	OFF
1	1	ON

FIG. 3—Neon lamp glows when inputs are at same level. In all three circuits, logic 1 = 0 volts (ground) and logic 0 = —6 volts.

Non-Stalling Flip-Flop for Capacitive Load

WHEN DESIGNING digital systems, the necessity of transferring data into a storage which has a heavy capacitive load, such as long lead wires, is frequently encountered. This capacitive load can slow the response time of the storage to the point where data transfer is unreliable. Buffer amplifiers are an inefficient, and not always effective, approach to the solution of this problem.

The circuit shown has the useful characteristic that the triggering between stable states is not de-



Capacitive load in emitter circuit increases gain.

graded by any amount of capacitive load on the output. Even though the load may be so heavy that milliseconds are required for the output to change state, the stage will trigger reliably in a fraction of a microsecond. In fact, the capacitive load actually assists the flip-flop in triggering. This characteristic is obtained by using a complementary configuration and placing the load in the emitter circuit of one transistor. In this configuration, any capacitive load decreases the emitter degeneration and increases the stage gain available for switching.

The circuit shown has a response time of about 0.3 microsecond. The circuit values are typical and may be altered depending on the application.

Binary Flip-Flop Turns On

THE CIRCUIT of Fig. 1 shows a binary operated flip-flop in which triggering is accomplished by turning the transistors on. Most similar circuits turn the transistors off.

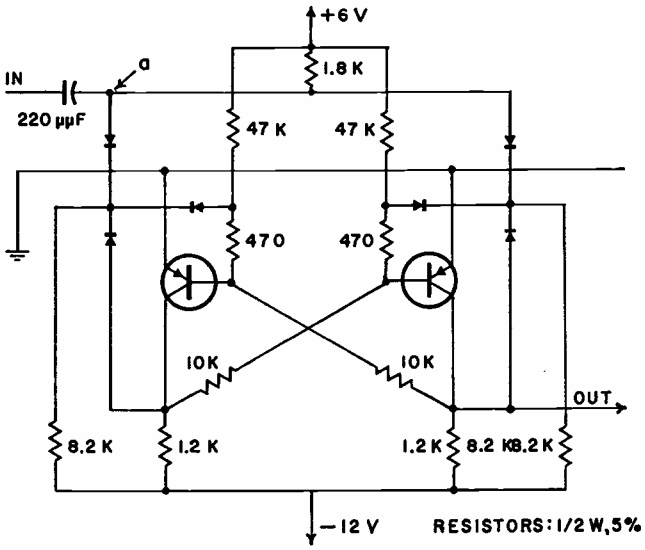


FIG. 1—Trigger turns transistors on in this binary flip-flop.

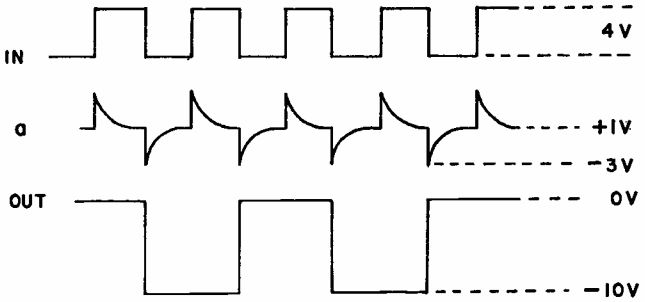


FIG. 2—Waveform at various points in circuit of Fig. 1.

Trigger current is designed into the circuit. The trigger impulse only has to lower point *a* below ground for a small period. (0.05 to 0.3 microsecond depending on transistors). Triggering operation and steering is very efficient, because the "off" transistor turns on.

Virtually any diode and transistor can be used. Speed capability is very high. (10 mc with high-speed transistors).

Output fall time does not have typical slow long fall time.

Phase Locked, Gated Oscillator With Amplitude Regulation

CIRCUITS presented in available literature for gated oscillators work well as long as the duration of the gated sine wave, or tone burst, is short. For longer gate times, say 10 msec. or more, the envelopes tend to expand or decay, conditions which are further aggravated by temperature change. A single zener diode, connected as shown in Fig. 1, provides a means of regulating the feedback to prevent this action. Even though only a

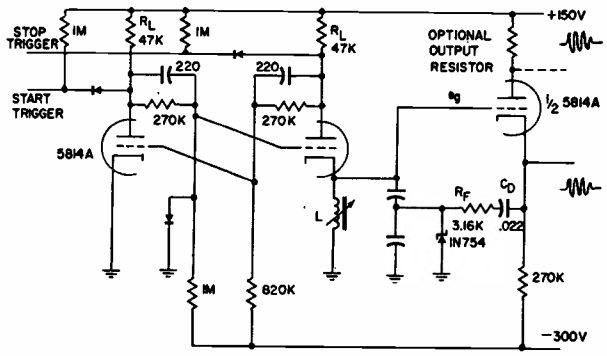


FIG. 1—Amplitude-regulated gated oscillator.

single zener is used, rather than two used back-to-back, the sine wave output is symmetrically regulated, and tone bursts of any length may be obtained. The feedback resistance (R_f) will permit clipping if resistance is too low, and decay if too large. If the blocking capacitor (C_b) is too small, it too will cause envelope decay, but there is no upper limit to this value.

The zener rating can be from 3 to 10 v for the circuit values shown, and the peak-to-peak output voltage will be about twice that. The output will begin at average, and the first half cycle will be negative. If the opposite polarity is desired, a small resistor (35 K or less, depending on the amplitude required) may be placed in the plate circuit as shown. Reversing the zener connections will still produce regulation, but not until after the first half cycle.

The diode placed on the gate grid stops the tone burst sharply at the end of the gate. The gate load resistors, R_L, should be selected to obtain a gate cathode current $i_k = e_g/2\,r_L$ in order to obtain immediate, full amplitude oscillations. e_g is the peak amplitude at the oscillator grid, and depends on the circuit parameters. It was 10 v for the circuit shown.

The oscillator inductor (L) used was a U.T.C. series HVC, which has a temperature coefficient that approximately compensates characteristic F

mica capacitors. The resulting oscillator is relatively insensitive to voltage variations as well as temperature change, both in amplitude and frequency.

XY Code Converter

THE CODE converter illustrated in Fig. 1 was developed as part of a data-selection system now in use with analog computers. General operation is as follows: Normally, all tens and units low-power input transistors are cut off; during selection, one tens transistor and one units transistor are saturated and this energizes the relay having that particular decimal designation.

The actual circuit design proceeded along the following lines: Since the input transistor could only draw 6 ma to ground, while the relays required 90 ma to −12 v, amplification would be required along each relay drive line. This suggested that for each relay, a power transistor be supplied which could be either saturated or cut-off, depending on whether or not

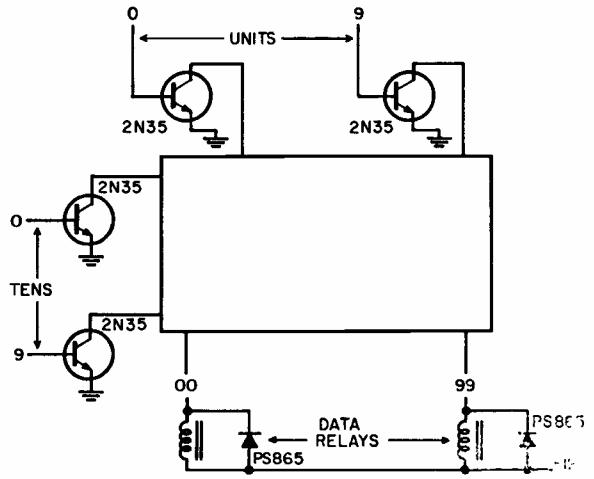


Fig. 1. Basic form of XY code converter.

that relay was to be energized.

Since each relay required its own transistor and since a transistor, to be saturated, required an "and" relationship between emitter and base, it was decided to use this "and" requirement as the code-converting mechanism.

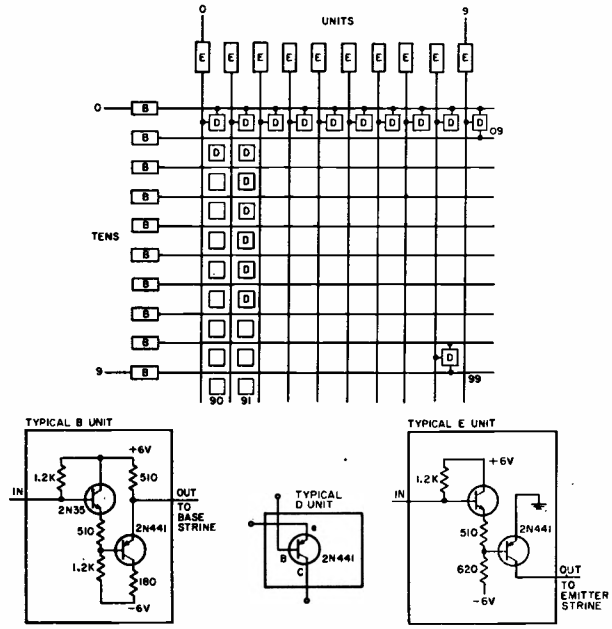


Fig. 2. Matrix form of XY code converter.

By tying the emitters of all transistor drivers having a common units designation together, and the bases of all with a common tens designation together, the code conversion was accomplished in simple *XY* matrix form.

One problem remained, the different drive requirements of a string of emitters as opposed to a string of bases. To drive an emitter string, it was necessary to clamp the emitters to ground via a saturated power transistor whenever its units designation signal was present. To drive the base string, it was merely necessary to lower the base voltage far enough below ground to saturate the conducting matrix transistor.

The final code converter circuit is shown in Fig. 2, where *D* designates relay drivers, *E*, emitter string drivers, and *B*, base string drivers.

Anti-Coincidence Detector

A CIRCUIT, DESIGNED out of necessity, which gives an indication when two input pulses are not coincident is presented here. The logic performed by such a circuit is shown in Fig. 1. For this purpose solid state circuit powered by a 25 v source was developed.

The block diagram of the anti-coincidence detector is shown in Fig. 2. When either pulse is received the respective input silicon controlled rectifier is turned on. This action applies the supply voltage to the bridge rectifier and, thereby, to the cathode of SCR_3. A short time later, a positive voltage is applied by the delay circuit to the gate of SCR_3 turning on both the gate and lamp.

Coincidence of pulse "A" and "B" turns on both input *SCR*'s, thus applying the supply voltage again to the SCR_3. However, since both SCR_1 and SCR_2 are on, the bridge rectifier inhibits the positive voltage which is applied to the gate of SCR_3 only when one input pulse is received. For this input condition the indicator lamp remains off.

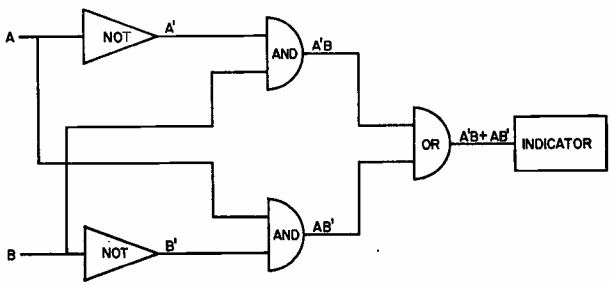


Fig. 1—Logic Performed.

The complete anti-coincidence detector is shown in Fig. 3. Here, a unique utilization of the bridge rectifier enables it to perform a relatively complex operation. Input pulses are fed into the circuit through pulse transformers, T_1 and T_2. The occurrence of pulse "A" turns on SCR_1 which applies −25 v to R_1, and to the cathode of SCR_3 through D_1. Current also starts flowing through C_1, R_3, D_4, and R_4. The time constant determined by R_3C_1 and R_4C_1 causes a delay in the

voltage across the gate of SCR_3. The lamp will be turned on by SCR_3 if pulse "B" does not occur within the delay.

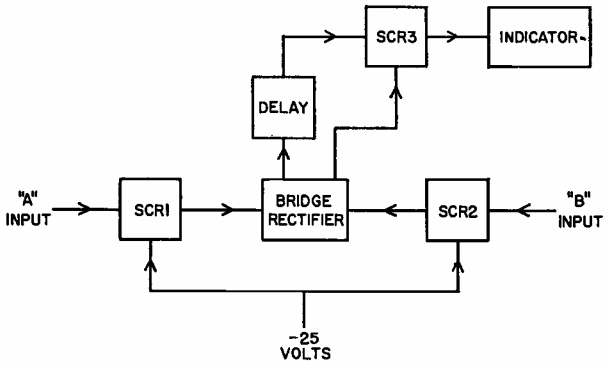


Fig. 2—Block Diagram.

If pulse "B" occurs within the delay, the SCR_2 is turned on thus applying —25 v to the junction of D_3, D_4, and R_4. A balanced condition now exists and current ceases to flow through the arms of the bridge. The voltage across the gate of SCR_3 no longer increases and C_1 is discharged through R_2. As a result, the lamp is not turned on.

Action similar to that just described takes place if pulse "B" occurs first and pulse "A" does or does not occur within the delay.

The delay circuit feeding the gate of SCR_3 is used to select the degree of anti-coincidence which the circuit will detect. The limit on the smallest degree of anti-coincidence which the circuit can detect (C_1 removed) is determined by the turn-on time of *SCR*'s and is about 0.3 usec for the type 2N1595 rectifier. The upper limit on the length of delay is set by the value of C_1. With a value of several hundred microfarads for C_1, the delay is several tenths of a second. The circuit is reset after each input condition by interrupting the —25 v supply.

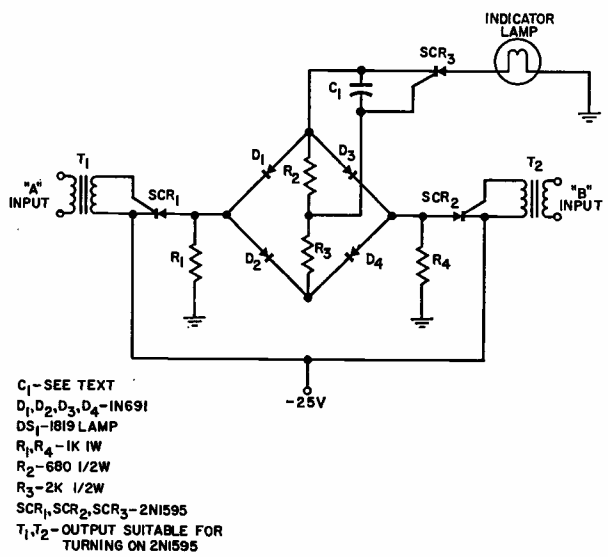


Fig. 3—Anti-Coincidence Detector.

Positive Transmission Gate

DESCRIPTIONS AND CIRCUITS of digital gates can be found readily in present literature on computers. If, however, information on the transmission gate (*i.e.*, digitally controlled analog switch) is desired, only a general description without a circuit is available. The attached circuit was designed when a transmission gate was needed. Some of the advantages are:

- ► There is a minimum of components;
- ► All components are inexpensive and readily available;
- ► Only two, easily obtained, voltages are required.

Advantages which are not obvious include:

- ► The output signal never passes through an active device and hence is not attenuated, distorted, or delayed;
- ► An ac signal with zero average value can be passed;
- ► There is almost negligible attenuation in the switch.

The circuit is merely a shunt switch. When the digital control voltage is 0 v, the transistor is biased in the cutoff region and the signal passes unattenuated. When the digital control voltage is —6 v, the transistor is biased into saturation. The collector potential rises to very near ground, and the signal is shunted through the transistor to ground potential.

The switch has a useable frequency range of 8 to 650 Kc.

The midband region is from 100 to 100 Kc. At Midband, the ratio of on voltage to off voltage is 4.2 v pp to 10 mv pp, or 420:1 which is an isolation of 54.5 db.

All of the above values were otained by using an 18 K simulated load.

The following is a partial list of suggested improvements:

- ► The isolation could be improved by a transistor with a lower $V_{ce\ (SAT)}$;

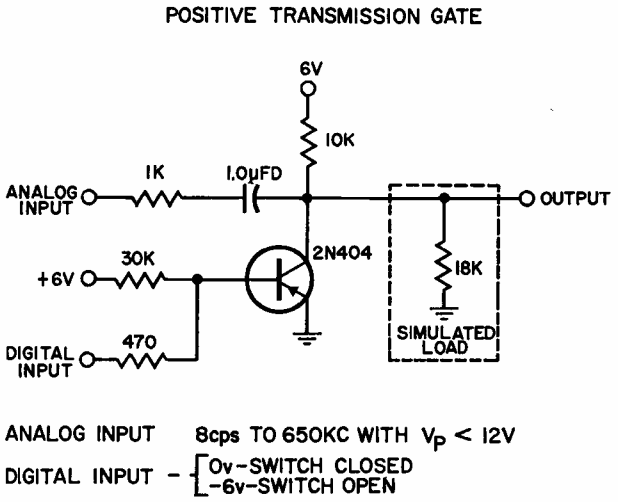


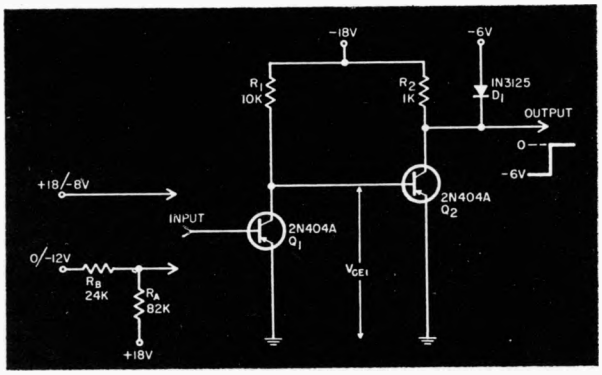
Fig. 1—Positive transmission gate.

- ► The frequency response can be improved by a transistor with lower shunt capacitance to ground;
- ► Higher signal voltages can be used if a higher V_{bb} is chosen;
- ► Almost any logic level can be used for control by changing the 30 K and 470 ohms bias resistors.

Logic-Level Converter

WHEN CONNECTING digital test equipment to data-recording equipment it often is necessary to convert to different logic levels. The circuit shown will convert from +18/—8 v logic levels (which are used, for example, in the Hewlett-Packard 5245L Frequency Counter) to the commonly used 0/—6 v logic levels of a data-logging system.

Logic *1* from the counter causes Q_1 to be turned off, thus causing Q_2 to conduct. With a —8 v input signal, Q_1 will turn on and cause V_{CE} to approach —50 mv, which in turn will cause Q_2 to turn off. Base current to transistor Q_1 is limited by an internal 100-K resistor in the counter output circuitry. Diode D_1 clamps the output voltage excursion at —6 v. With the circuit values shown, the output current capability is 12 ma in the output *O* state. Reliable operation can be expected over a temperature range of 0 to 55°C.



Logical-level couverter with two input circuits for common commercial equipment.

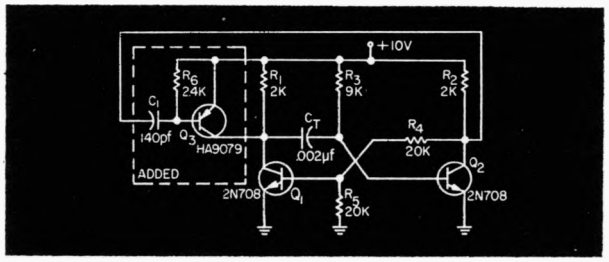
With R_B connected in series with the input transistor base and reverse-bias resistor R_A, the same base circuit can be used to connect 0/—12 v levels (Non-Linear Systems' digital equipment) to an external data-logging system. ◆◆

Added Transistor Reduces One-Shot Recovery Time

THE REPETITION RATE of a transistor one-shot is limited by its recovery time, which is almost entirely determined by the charging of the timing capacitor. In a conventional one-shot the capacitor is charged through R_1 and discharged through R_3 (see figure). The relative magnitudes of these two resistors therefore limit the duty cycle and consequently the repetition rate for a given pulse width. The addition of a transistor, resistor, and capacitor, as shown in the figure, reduces the timing capacitor's charging time to a very small fraction of the one-shot pulse width.

During the output pulse, Q_3 is held off by R_6 and the circuit behaves like a conventional one-shot. When the pulse ends, Q_2 turns on and C_1 transmits a negative impulse to the base of Q_3. Q_3 saturates, providing a low impedance charging path for C_T. C_1 is chosen large enough to keep Q_3 saturated until C_T is fully charged. Then Q_3 cuts off, leaving the circuit ready for the next pulse.

Using the values shown in the figure, the circuit provides 10-μsec pulses with a recovery time of 0.25 μsec. This corresponds to a repetition rate of almost 10^5 pps and a duty cycle of 97.5 percent. ◆◆



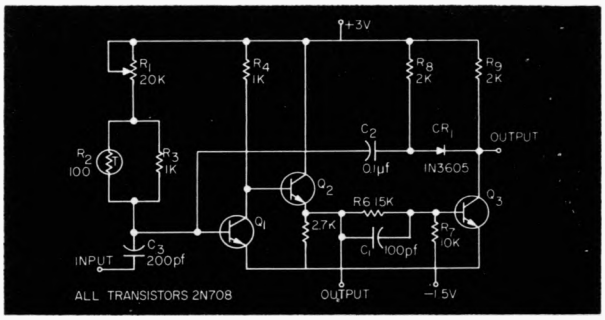
Transistor Q_3 reduces timing capacitor's charging time, increasing the duty cycle.

Temperature-Compensated One-Shot

A NEGATIVE-TEMPERATURE coefficient thermistor is used to keep the pulse width of a multivibrator constant to within 0.6 percent over a temperature range of 25° C. The basic period of the circuit shown is 357 μsec. The period increases to 359 μsec at the temperature extremes.

The thermistor is placed in the pulse-width determining network as shown. The proper compensating network is best found experimentally. The circuit is placed in an oven and a resistance decade box is used for the R_2-R_3 combination. The proper resistance at each temperature is determined and the compensating network then designed to match this temperature characteristic. In the circuit shown, the thermistor has too large a variation over the temperature range, so a fixed resistor R_3 is placed in parallel to obtain the best curve fit. The thermistor used in this example had a resistance of 100 ohms at 25°C.

The potentiometer can be used for small adjustments in pulse width, while the capacitors can be changed for large



Temperature-compensated one-shot.

pulse-width variations.

Diode CR_1 and two collector load resistors R_8 and R_9 decrease the turn-off time of Q_3 at the end of the pulse by

decoupling the collector from the pulse-width determining network. The 3-v power supply is used for very low power consumption and to make the circuit compatible with integrated circuits elsewhere in the system. Power supply fluctuations greater than ±5 percent can be tolerated. ◆ ◆

Analog-Voltage Selection Switch

CONVENTIONAL DIODE logic gates also can be used to switch analog voltages. To choose one analog signal out of several such inputs, a negative control voltage is applied to the proper gate and positive, inhibiting voltages

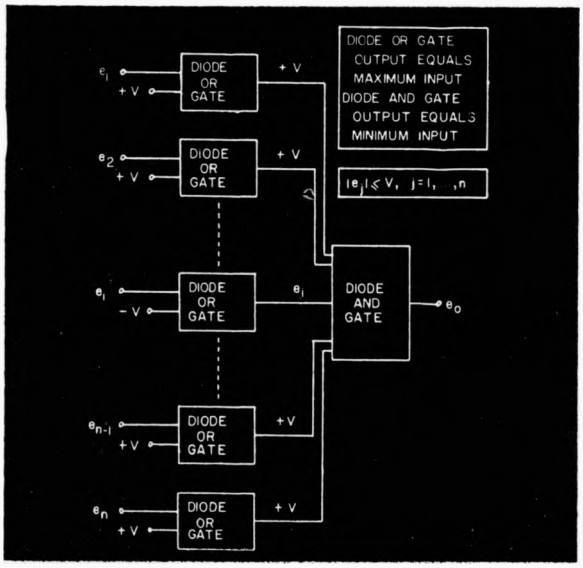


Fig. 1. Analog selection switch. The only gate that switches is the one with -V applied.

are applied to the gates for the undesired analog voltages. In Fig. 1, e_o will equal e_i if $-V$ is applied to the ith gate and if $e_i < V$ (V positive).

A typical 2-input switch is shown in Fig. 2. If r_f and r_b are the diode's forward and backward bias resistances, and if $r_f << R << r_b$ then the level shift through the switch will nominally be, for zero source resistances, $(r_f^2/2R^2)E + (r_f/R)e$ where e is the voltage across the diode just as it becomes forward-biased.

If the source resistances are not zero (but still much less than R), then the legs of the AND gate should be augmented with series resistors, each equal to the resistance of the source whose signal passes through that leg. The level shift will be as before, but with the value of r_f increased by an amount equal to the source resistance.

The crosstalk from the switching signal inputs yields a level shift which will nominally be $(r_f/r_b)V$, a level considerably smaller than the level shift from biasing. The crosstalk from the "off" input signal will be that signal attenuated by approximately $(2r_b^2/r_f^2)$.

The gain of the switch for the "on" input signal will be less than unity by about $(2r_f/R)$. The gain will be down 3 db at a frequency of about $(1/5\pi r_f c)$, where c is the backward bias capacitance of the diodes. In practice this 3-db cut-off frequency is not realizable because of non-zero source resistances and capacitive loading of the switch output by the following stage. At this frequency the "off" input signal will be attenuated by better than 20 db up to a frequency of approximately $(1/8\pi r_f c)$.

If the switching signal is a square wave, so as to provide alternate sampling of the two input signals, then the crosstalk from the switching signal inputs will be a signal 20 db down from the square-wave amplitude for a square-wave period greater than $(80\pi r_f c)$.

The inset in Fig. 2 shows typical parameter values for

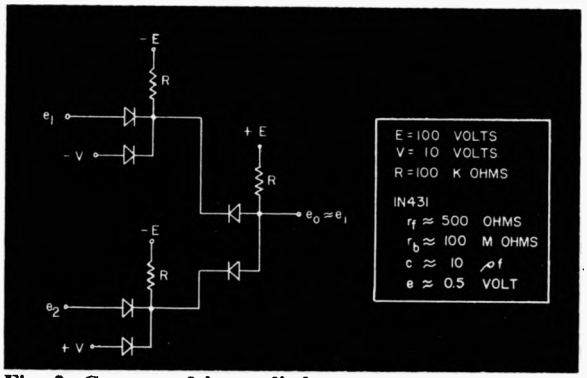


Fig. 2. Common 2-input diode gate.

the circuit as it was built in the laboratory.

Note that the same switching property can be obtained with the diode OR and AND gates interchanged and with polarity reversal of V. ◆ ◆

High Duty-Cycle One-Shot

THE MAXIMUM duty-cycle at which a one-shot may be operated is limited by the recovery time (the time to recharge the timing capacitor). This recovery time is a particular obstacle when the timing capacitor is made large for pulse widths on the order of one second.

Approaches to this problem have produced various methods for reducing the recovery time, but none for eliminating it. The approach described here eliminates the problem and enables the individual designer to use existing digital logic modules. Thus, the reliability of the system incorporating the high duty-cycle one-shot will not suffer from the use of non-standard circuits or components.

The technique, Fig. 1, is to alternately trigger two identical one-shots. To do this, the trigger pulse is alternately steered from the first one-shot to the second by a toggle-connected flip-flop and a pair of pulse steering gates. The flip-flop changes state at the completion of the output pulse, thus delaying the next pulse to be formed only by the transition time of the flip-flop. This means that the trigger pulses may be as close as $T+S$, where T is the output pulse width and S is the flip-flop transition time.

The circuit shown in Fig. 2 is the way the author implemented the logic diagram of Fig. 1. The circuit produces 700 msec pulses and is triggered every 705 msec, a ratio difficult, if not impossible, to attain using the conventional one-shot. A 6 v positive transition with a 1 μsec rise time will trigger the circuit.

This technique was carried one step further as shown in the alternate diagram in Fig. 1. By triggering the toggle flip-flop from a shorter delay one-shot, the output pulses can be made to overlap if the interval between trigger pulses is shorter than the pulse width.

This circuit has variations which are valuable in pulse rate measurements. For example, it can be used to give an output transition when there is a missing pulse; or, it can indicate when a pulse frequency has exceeded or diminished from a preset value.

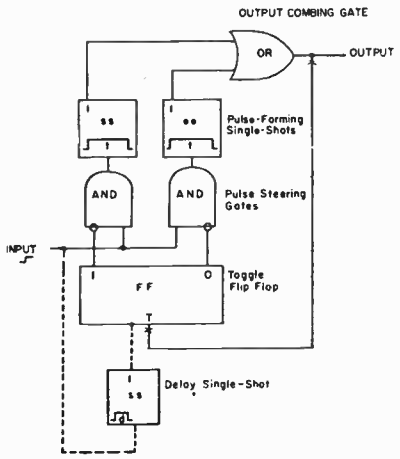


Fig. 1. Logic diagram. With circuit modified as shown dotted, and by breaking connections at x-x, output pulse overlap is obtained.

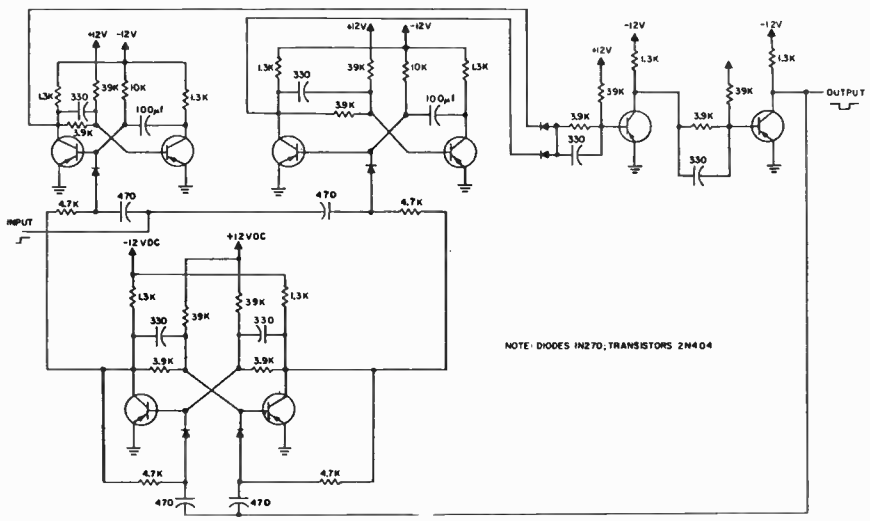


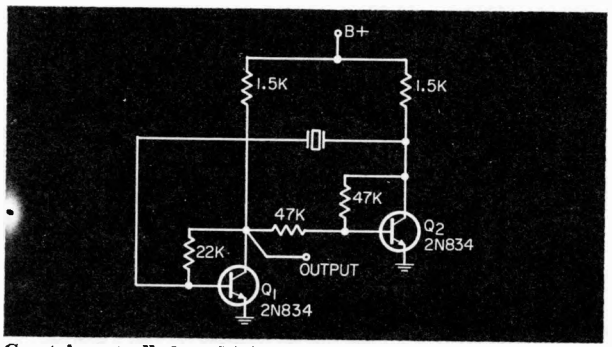
Fig. 2. High duty cycle 700 msec one-shot.

Crystal Controlled Multivibrator

THIS OSCILLATOR is useful as a system clock. It combines simplicity with crystal stability and uses no inductors or capacitors. The circuit can be built up from logic NOR gates with the only frequency controlling element the crystal itself.

Each transistor operates as a feedback amplifier. The Q_2 stage has unity gain. The gain of Q_1 is a function of the resonant impedance of the crystal. But since most crystals have a resonant impedance less than the 22-K feedback resistance, the gain of the Q_1 stage is considerably greater than unity.

The output at the collector of Q_1 is a rounded square wave with a peak-to-peak voltage dependent on the $B+$. The circuit oscillates at 1 mc from 2 v to 30 v. A wide range of frequencies from 3 kc to 10 mc can be accommodated without changing any elements in the circuit because of the sole use of resistance for both biasing and loop gain.



Crystal-controlled multivibrator.

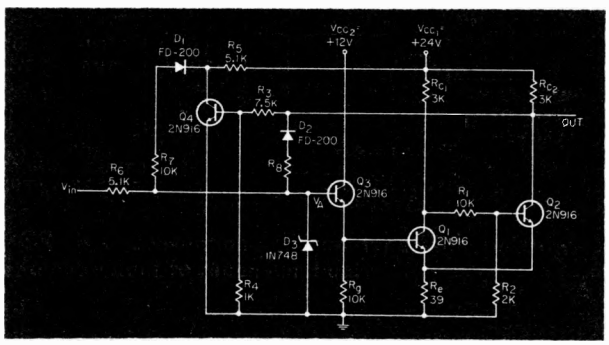


Fig 1. Variable-hysteresis Schmitt trigger.

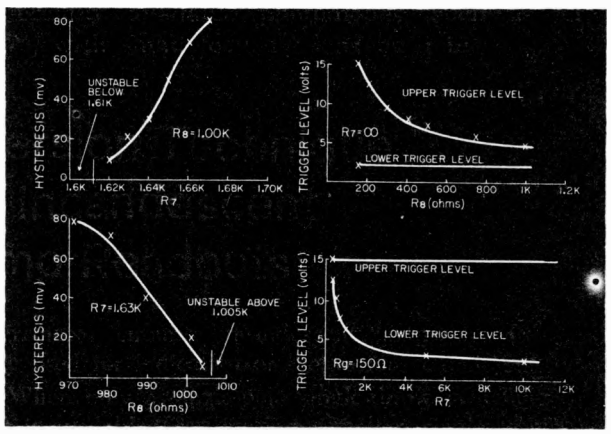


Fig. 2. Trigger-level and hysteresis variations.

The circuit operates over a temperature range of 0° to 60°C with less than 0.05 percent drift. The output can be loaded with a 15-K resistance without seriously affecting the waveshape or frequency.

Variable-Hysteresis Schmitt Trigger

THERE ARE MANY CASES where the hysteresis offered by a Schmitt trigger could be useful if its range could be widened without destroying circuit operation (output pulse amplitudes, etc.). The circuit presented here is quite simple and straightforward and can be easily designed to fit individual needs.

Transistors Q_1 and Q_2 are in a typical Schmitt configuration. Q_3 acts as a buffer so as not to load the driving circuitry.

In the normal state, Q_1 off and Q_2 on (saturated for this analysis), the voltage V_A is approximately

$$V_A = \frac{R_8 V_{in}}{R_6 + R_8} \qquad (1)$$

This assumes that there is no loading on R_8 by zener D_3 or Q_3, and that Q_2 is at ground potential. R_7 is not in the circuit since Q_4 is off, thus back-biasing D_1 and removing R_7 from the circuit.

When V_A nears the inherent upper trigger level (UT) of the circuit, X, Q_1 starts conducting until Q_2 turns off, which in turn turns Q_4 on. Now D_2 is back-biased, thus removing R_8 from the circuit. D_1 becomes forward biased, thus putting R_7 in operation. Now

$$V_A = \frac{V_{in} R_7}{R_6 + R_7} \qquad (2)$$

Thus the Lower Trigger point (LT) can be controlled by R_7. The zener diode is used to limit the maximum voltage across R_6 and to prevent Q_1 from becoming forward-biased.

At first glance it appears that Q_1 could be used in place of Q_4 (since their states are essentially the same). The problem is that Q_1 is a linear amplifier for a short period before Q_2 switches, also it is hard to get V_A close to ground potential.

The inherent UT for the Schmitt, including Q_3, is X and the LT, Y. From the Eqs. 1 and 2:

Upper Trigger

$$V_{in} \simeq \frac{X (R_6 + R_8)}{R_8} \qquad (3)$$

Lower Trigger

$$V_{in} \simeq \frac{Y (R_6 + R_7)}{R_7} \qquad (4)$$

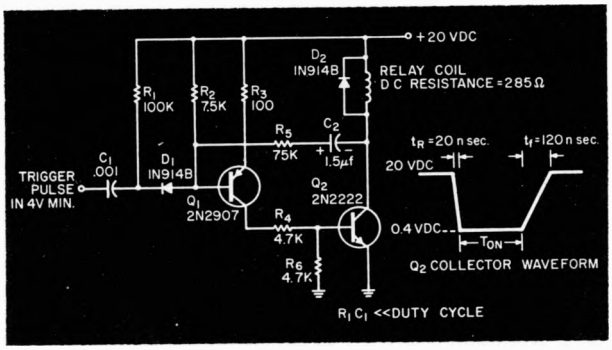
The Hysteresis (H) is

$$\frac{X (R_6 + R_8)}{R_8} - \frac{Y (R_6 + R_7)}{R_7} = H$$

Fig. 2 shows the effects of R_7 and R_8 on the upper and lower trigger levels and the zero-hysteresis as a function of small changes in R_7 and R_8.

Power One-Shot

THIS COMPLEMENTARY symmetry one-shot is one solution to the problem of how to supply 1.4 w for 0.1 sec to a relay coil on a very low duty cycle basis, without giving away any power in standby.



Power one-shot.

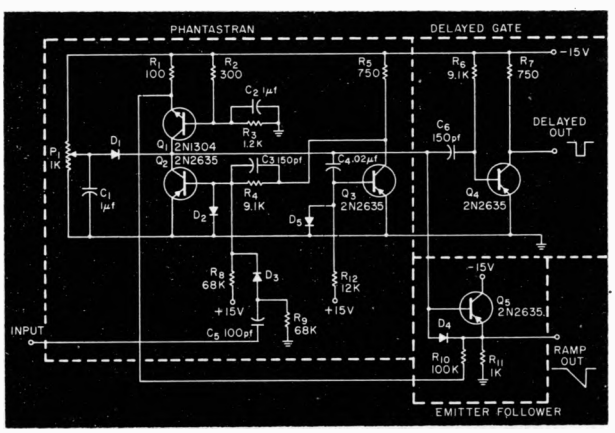
One particular application required a contact closure for 0.1 sec to discharge a 1000-pf capacitor that was charged previously to 10 kv. Two reed switches in series, mounted in a common coil, provided the contact closure but the coil required 20 v at 70 ma to operate.

The complementary symmetry one-shot is triggered on once every 8 sec for 0.1 sec. Prior to an input trigger pulse, Q_1 and Q_2 are in the off state. The input pulse is first differentiated by C_1 and R_1, and diode D_1 passes the negative-going portion, causing base current, causing the collector of Q_2 to fall. C_2 couples the 20 vdc swing to the base of Q_1, regeneratively turning both junctions on hard. C_2 then begins to charge through the base emitter junction of Q_1 in series with R_5. As the base of Q_1 approaches 17 v, Q_1 turns off, turning off Q_2, causing Q_2's collector to rise. This positive 20-v swing is coupled through C_2 to the base of Q_1, regeneratively turning both junctions off.

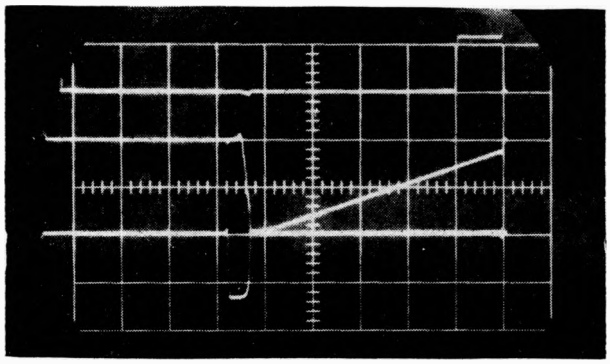
The device on-time is essentially determined by the charging time of C_2 through R_5, but h_{fe} of both junctions enters into the picture, causing T_{on} to be temperature sensitive. A ±20 percent drift from −40°C to +85°C is evident. Temperature compensation might be possible, but often is not required.

Phantastran Delayed Gate

THE ADDITION OF FOUR PARTS to a Phantastran (a solid-state Phantastron) produces a circuit that generates a gate at the end of a sweep which can be used as a delayed signal. The Phantastran itself is made up of Q_1, Q_2, and Q_3. Q_3 is a combination emitter follower and ramp linearizer. The four parts which make up the delayed gate generator are C_6, R_6, R_7, and Q_4.



Phantastran delayed gate.



Phantastran waveshapes. Time is read from right to left. Upper trace: input (10 v/cm); center trace: ramp (5 v/cm); lower trace: gate (10 v/cm).

Q_2 and Q_4 are normally on. Q_3 is off. C_4 has been discharged by the saturated impedance of Q_2 and D_5. A positive trigger through C_5 turns off Q_2. Constant current source Q_1 turns on Q_3 and charges C_4 linearly to a maximum of 13 v. As soon as C_4 charges to the point where D_1 conducts, the constant current generated by Q_1 is diverted through D_1. Q_3 turns off, and Q_2 turns on. C_4 rapidly discharges to ground. This positive step is transmitted through C_6, which turns off Q_4. After a period equal to $0.7 \times R_6C_6$, Q_4 turns on again.

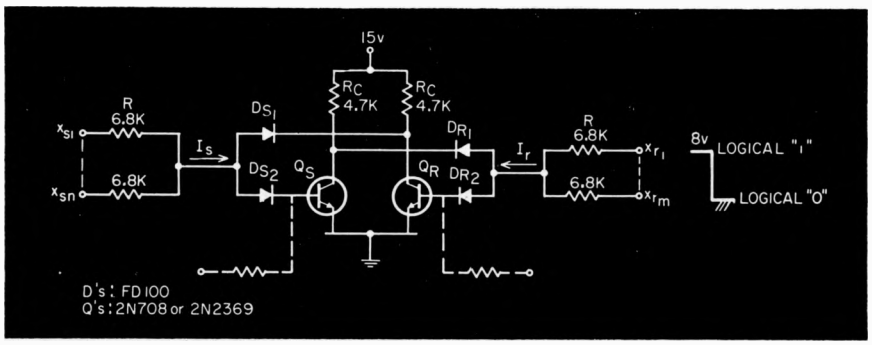
The width of the delayed gate is a function of the maximum amplitude of the sweep, whose slope was designed to be approximately 1 v/μsec in the circuit. The maximum width of the gate is 1 μsec. Potentiometer P_1 sets the maximum amplitude of the sweep. The sweep is linearized by feeding back a signal through the output of an emitter follower back to the current source, Q_1.

Flip Flop Operated by Input Signal NOR

THE USUAL FLIP FLOP, with resistive inputs (RS type), is set (reset) when one of the input signals on the SET (RESET) side goes to its high level. The modified flip flop described here is set (reset) when all the input signals $x_{S1}, \ldots x_{Sn}$ ($x_{R1}, \ldots x_{Rm}$) are low. From a logical standpoint, it is set (reset) by the NOR-function of its input signals instead of the OR function. To implement the same function with the usual flip flop, two extra transistors would be required.

When Q_s is on, the current I_s flows through D_{s2} into the base of Q_s, while I_r flows through D_{R1} into the collector of the same transistor. To drive Q_s OFF, i.e to change the state of the flip flop, the current I_s must be at least temporarily zero. The same considerations apply to the other side of the flip flop since the circuit is symmetrical.

We can add the usual SET or RESET inputs (dotted in figure) by coupling the signals to the base through resistors.



Modified flip flop is set or reset when all input signals are low.

Sample-Hold Circuit

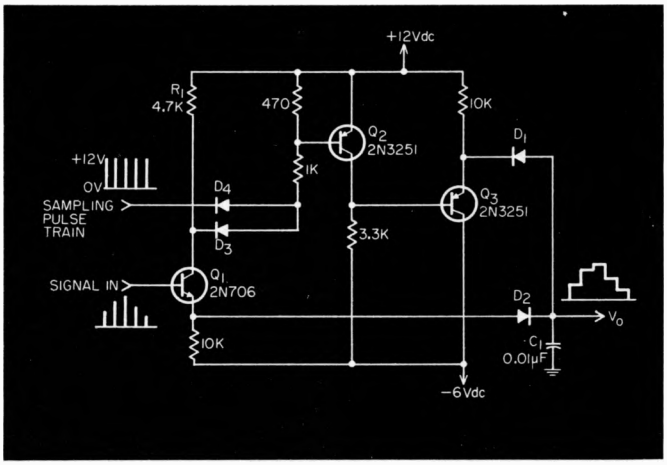
MOST SAMPLE-and-hold circuits are quite complex. Some simpler ones have been published in the last year. However, in these circuits because charge and discharge of the hold capacitor can occur simultaneously, a resistor is placed in one of these paths to limit the current. The resistor drastically limits the speed with which the output responds to new input levels. For short sampling periods, in the order of 1 μsec, the slow speed precludes the use of these circuits.

The circuit shown here does not have this limitation. Charge and discharge do not occur simultaneously, and no current limiting resistor is needed. There are two inputs (see figure); the signal whose amplitude is being sampled, and a positive sampling-pulse train. Between pulses the sampling train is at ground potential, holding Q_s in saturation. Its

collector voltage approaches +12 V, cutting off Q_3, whose emitter is then at +12 V. This reverse-biases low-leakage diode D_1, preventing any discharge of C_1 between pulses. At this time, Q_1 is also turned off, since there is no positive signal. Its emitter is at −6 V, reverse-biasing low leakage diode D_2. This prevents charging of the hold capacitor between pulses.

During sampling periods, if the new signal pulse is more positive than the previous one, C_1 is charged rapidly to the new level through emitter follower Q_1 and diode D_2. The collector voltage of Q_1 drops below +12 V because of the charging current. This drop, applied through diode D_3, drives Q_2 into saturation. As before, Q_2 in saturation cuts off Q_3, and back-biases D_1 so that discharge cannot occur during the charging period.

If the new signal pulse is less than the previous one, Q_1 remains cut off. Also Q_2 remains cut off, and emitter follower Q_3 conducts heavily, providing a low - impedance discharge path for C_1 through D_2. This discharge continues until C_1 has discharged to the amplitude of the new pulse, less the diode drops in Q_1 and D_2. At this time Q_1 turns on, stopping the discharge.



Sample-and-hold circuit in which a new signal level is sensed only when a sampling pulse arrives at the other input.

Flip-Flop Has Improved Rise Time And Stability

THE BASIC FLIP-FLOP of Fig. 1, has an inherently slow rise time due to the charging of C_2 through R_2. This is particularly true if the flip-flop is to have a relatively long period and yet draw little power. This requires large values for C_1 and C_2. A second drawback is the dependence of the half-period on the value of $E_{0\ max}$, which in turn depends on the load. If the load is variable or unknown, stability is lost.

By the addition of a few, inexpensive components, (Fig. 2), the performance can be greatly improved. Output V_2 has a very fast rise time, since it is isolated from the RC time constant by D_1. The fall time of V_2 is slow until D_1 becomes forward biased, at which time the regenerative switching action takes place. (The larger the value of R_7, the faster will be the initial rate of fall; otherwise the value of R_7 is not critical.) The zener diode is chosen such that $E_{o\ max}$ is less than $V_{1\ max}$ so that the switching of E_0 occurs only along the fast slopes of V_2. Using a C of 22 μf and a frequency of less than 15 cps, rise and fall times on the order of tenths of microseconds are easily obtained. Since the timing components of the flip-flop are well isolated from the output, the frequency will remain constant for any load.

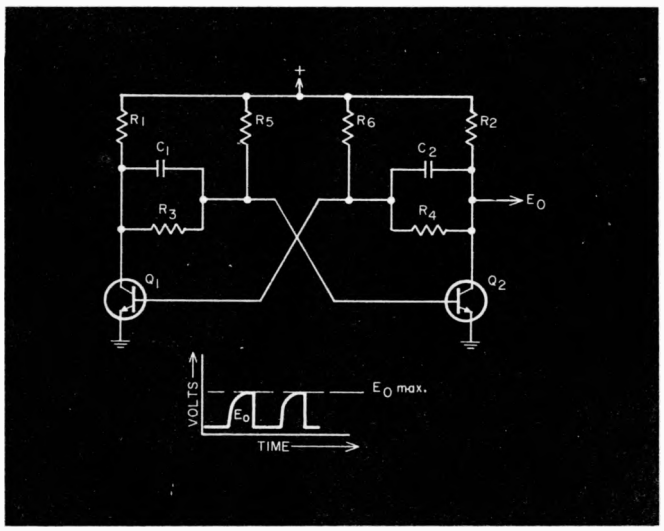


Fig. 1. Basic flip flop rise time is limited by time constants of R_2 C_2.

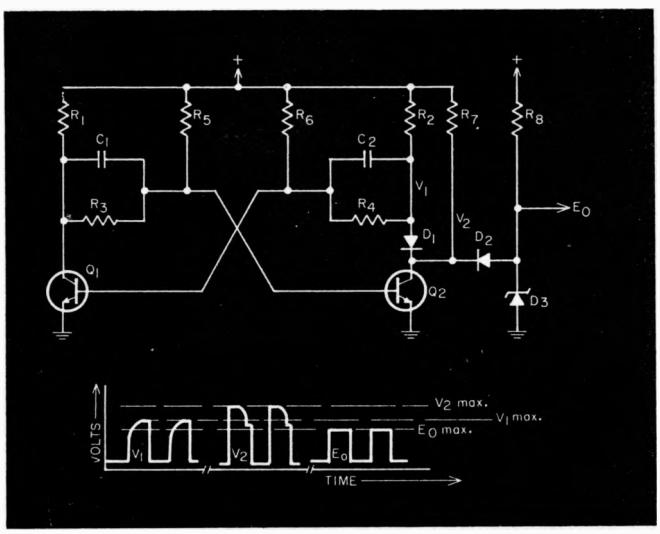


Fig. 2. Modified output circuit isolates output pulse from RC time constant.

Emitter-Coupled Astable with Saturated Output

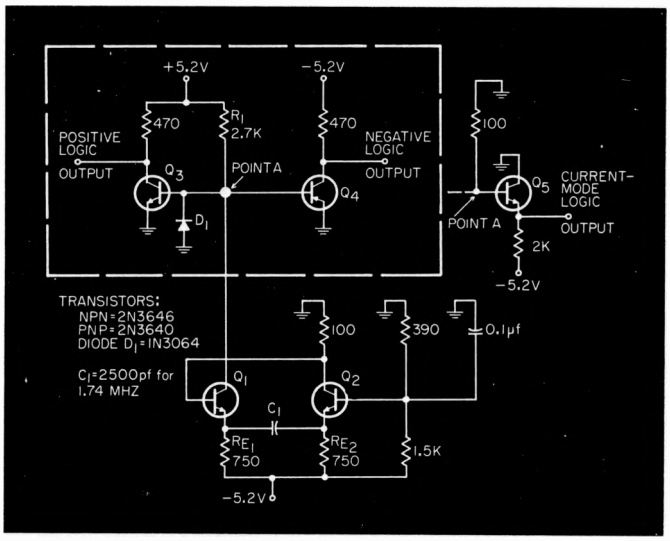
BECAUSE OF ITS OUTPUT CHARACTERISTICS, the emitter-coupled astable is not easily applied as a drive for logic circuitry that requires a low impedance-to-ground output (TTL for example). The modified version of the circuit shown here, however, accomplishes this. It also provides the advantages of being self-starting, has no recovery-time phenomena, and provides the good frequency stability found in emitter-coupled oscillators. In addition, high-speed saturated positive and/or negative polarity outputs or a current-mode logic output can be obtained.

Q_1 and Q_2 operate as an emitter-coupled oscillator. When Q_1 turns off, diode D_1 is reversed-biased and Q_3 is saturated. When Q_1 turns on, the base current of Q_3 is switched into the collector of Q_1. Diode D_1 clamps the collector of Q_1 to about -0.7 V so that Q_1 is not heavily saturated.

Diode D_1 may be removed and a pnp transistor Q_4 added as indicated to obtain either positive or negative or both polarity outputs. The base-emitter diode Q_4 now performs the function of diode D_1.

All circuitry in the dashed box may be replaced by Q_5 and its associated circuitry. The output at Q_5 swings from -0.75 to -1.55 V which is compatible with the present-day integrated-circuit current-mode logic.

Operating frequency may be varied from 50 Hz to 8.5 MHz by varying C_1. Symmetry may be adjusted by varying the ratio of R_{E1} and R_{E2}. Rise and fall times are 10 and 12 nsec respectively and vary little with operating frequency.



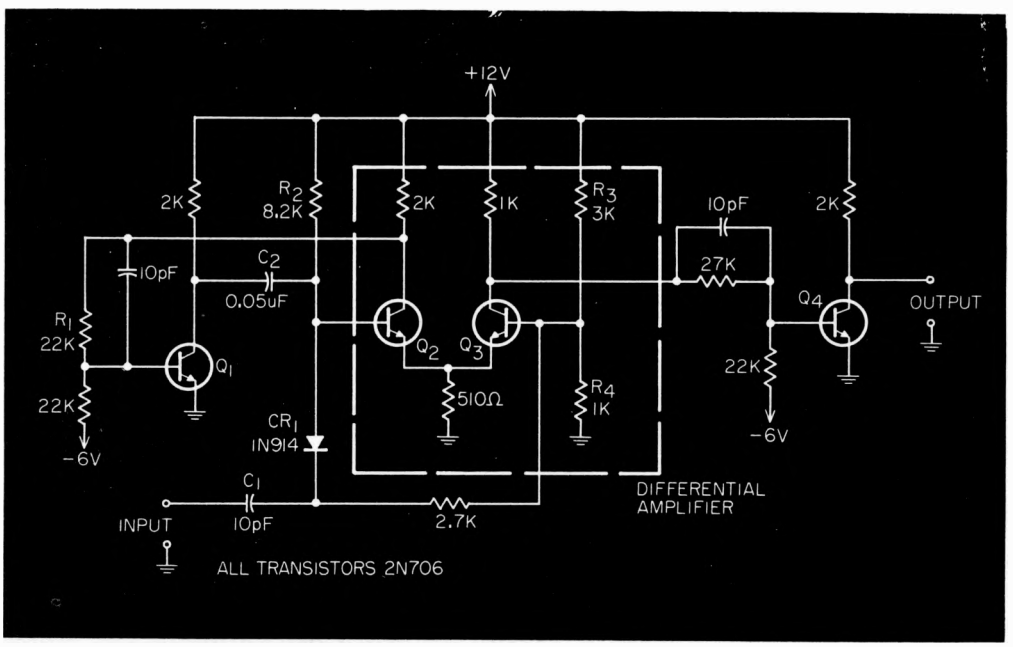
Emitter coupled astable; the circuitry in the dashed box may be replaced by Q_5 as shown.

One-Shot Has Improved Temperature Stability

IN TRANSISTOR one-shots using low-leakage silicon devices, one of the primary causes of variations in output pulse width is the temperature dependent base-emitter voltage of the normally-on transistor. By using a differential amplifier (Q_2 and Q_3) as shown, the turn-on voltage of Q_2 is controlled and hence the output pulse width is stabilized.

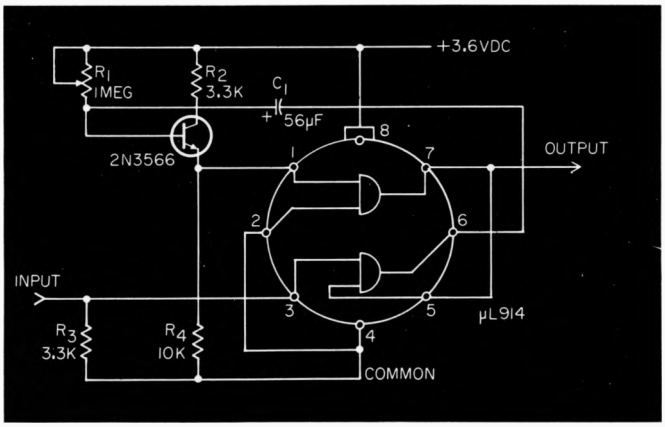
When a negative pulse is applied to the input, Q_2 is turned off and Q_1 is turned on. Also, Q_3 turns on causing the output of Q_4 to be turned off. The time Q_2 remains off is determined by C_2, R_2 and the turn-on point of Q_2. This turn-on point is established by R_3 and R_4 and is about 3 V for the values shown. Since the V_{BE} drops of Q_2 and Q_3 track with temperature, the voltage at the base of Q_2 is only a function of R_3 and R_4.

With the values shown, the pulse width is approximately 300 μsec, with rise and fall times of 50 and 100 nsec.



One-shot circuit has differential amplifier which improves temperature stability.

Long-Duration One-Shot Uses Integrated Circuit



IC/Transistor circuit gives long time-constant without using large capacitors.

ADDING A TRANSISTOR is a solution to the problem of designing a long-duration one-shot multivibrator with integrated circuits. The low impedances of ICs usually dictate the use of large and expensive capacitors to obtain long time-constants. The circuit shown, here, however, uses a small tantalum capacitor and a commercial-grade transistor. For this circuit the total component cost is less than $3.50 in small quantities.

With the component values shown, the circuit provides pulses of up to 75-sec duration, and will operate with supply voltages as low as 2.6 Vdc. Input and output levels are compatible with standard micrologic.

The time constant is determined by R_1 and C_1. Resistor R_2 should be low enough to avoid current-starving the IC. For the μL 914 dual-gate circuit, resistor values in the range 1 k to 10 K are acceptable. R_4 provides a return path for reverse leakage current in the IC. This resistor can be bypassed with a suitable capacitor if necessary, to prevent false triggering due to ripple on the B+ line. A series resistor may be added in the feedback path between pins 5 and 7. The value of this resistor will depend on the output loading.

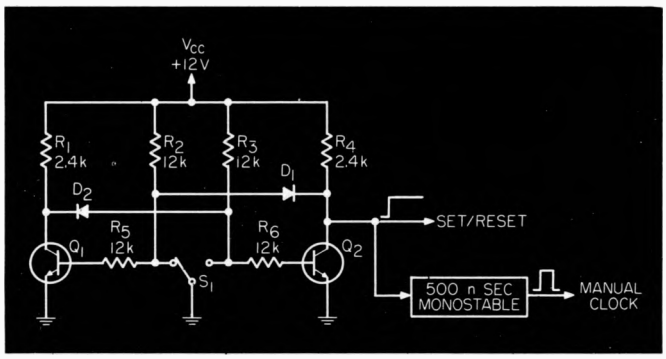
Low-cost manual pulser

THIS SIMPLE low-cost circuit provides manually-initiated set/reset voltages and clock pulses. It is useful for testing many types of digital circuits such as flip-flops, counters and adders. The circuit eliminates the effects of switch bounce that could cause false triggering of circuits under test. Total cost (excluding the optional monostable) can be less than $3.00.

The basic circuit gives complementary set/reset voltages at the collectors of Q_1 and Q_2. If a monostable circuit is connected to one of the collectors as shown, the complete circuit also provides manual clock pulses. The monostable is triggered by changes of state of the collector voltage. In the circuit shown, the monostable gives a single positive-going pulse each time the Q_2 collector voltage changes from "low" to "high."

The circuit works as follows: With the switch in the position shown, Q_1 base is clamped to ground. So Q_1 is cut off. Base current from the V_{cc} line flows through R_3 to turn on Q_2. The collector of Q_2 then approaches ground potential thus latching off Q_1.

When the switch is moved to the other position, Q_2 turns off and Q_1 turns on. With 2N706 transistors, total latching time is less than 200 ns. This is much shorter than the duration of contact bounce for a typical toggle switch. Spurious input pulses, caused by contact bounce after initial switch closure, have no further effect on the circuit. This is because all input pulses are of the same polarity (positive-going for the circuit shown).



Manual no-bounce pulse generator for testing digital circuits.

Another possible circuit modification is to use a momentary pushbutton switch, instead of the toggle switch shown. Then the circuit generates a short pulse each time the switch is pushed. Rise time of Q_1 determines rise time of the collector voltage and hence the delay of the output pulse from the monostable. If the delay is excessive, a faster transistor such as 2N709 can be substituted for the 2N706.

High-Speed Pulse Transmission Gate

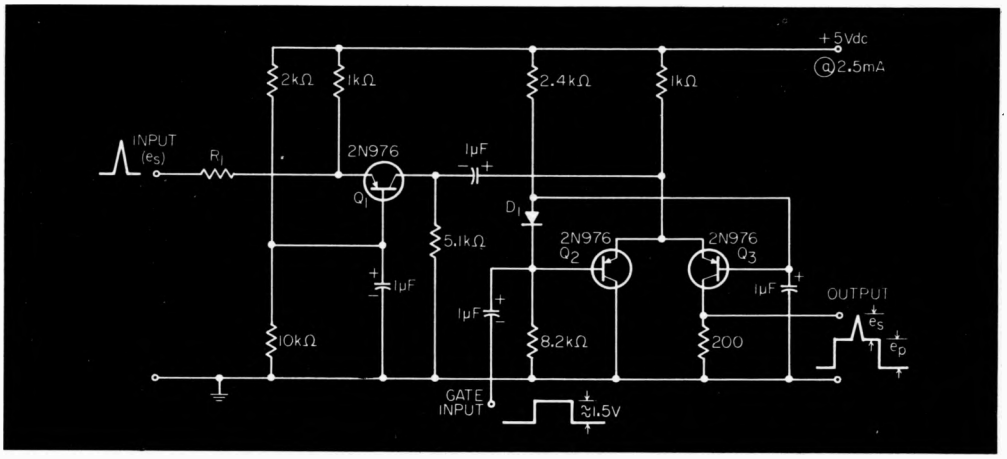
IT'S DIFFICULT to design a transmission gate to give good rejection of fast pulses in the "off" state. Stray capacitances integrate the pulse in the "on" state and bypass the gate element in the "off" state.

The circuit shown uses current switching. This overcomes the above problems because the low impedance levels minimize the effects of stray capacitance.

Transistors Q_2 and Q_3 form the gate element, and Q_1 is the input amplifier. In the absence of a gate pulse, Q_2 is biased into conduction. Incoming signals are thus shorted to ground. The signal voltage at the emitters is less than 0.5 Vpk for signal currents up to 100 mA. Any increase in signal level merely turns Q_2 on harder. Transistor Q_3 is back-biased by about 0.75 V. Thus it isolates signal current from the output. Capaci-

tance of the reverse-biased junction of this transistor is around 1 or 2pf, so negligible signal appears at the output collector.

When a positive gate signal appears at Q_1 base, it cuts off this transistor and switches the bias current into Q_3. Thus, the gate circuit transmits the signal pulse to the output. The bias current causes a pedestal voltage e_p beneath the output pulse. The amplitude of this pedestal can be controlled by varying the emitter resistor of Q_1, Q_2. In practice, however, the pedestal current cannot be reduced below about 0.5 mA, since further reduction will affect r_e and hence the linearity of small-signal transmission. The source for the gate should be a high impedance (>5 kΩ) otherwise bias current will be switched back into the source instead of thru Q_2.



This transmission gate for fast pulses operates in a current-switching mode. The pedestal e_p on the output pulse is caused by bias current in Q_3.

Amplifier Q_1 gives suitable isolation between the input source and the gate circuit. The output impedance of Q_1 is primarily determined by its load resistor. This resistor can be high because the signal voltage at this point is small.

Diode D_1 ensures that Q_3 is completely turned off. It can be any fast silicon diode. Resistor R_1 determines the input signal current when the circuit is driven from a low-impedance source.

The circuit was originally designed for use with a photomultiplier tube. The gate rejection is as high as 100:1 for 1.5-ns pulses. With this input, the output rise time is 3.5 ns. Of course the circuit should be wired with all signal leads as short as possible.

TTL/DTL interface to FET analog switch

IT'S USUALLY difficult to control different types of analog-switch FETs, with their differing cutoff voltages and input levels (up to ±10V), from the 0 and +5-V logic levels of DTL and TTL circuitry. The circuits shown here make it easy and economical to switch different MOS and junction FETs from DTL, TTL or RTL logic.

We can see the problems if we look at either circuit shown here and consider an n-channel JFET like the 2N5459/MPF-105, whose maximum gate-source cutoff is −8 Vdc. This dictates a $-V$ supply of $-V_{in}$ -8 $-|V_{satQ2}|-|V_{D3}|$. The positive supply must be high enough (about $+V_{in}$) to back bias D_3 ($V_{gs}=0$) at the maximum positive peak of the input waveform.

We see that the required magnitudes of ±V can vary widely. So we need a constant-current base drive to insure full saturation or cutoff of Q_2, regardless of the value of $-V$, since Q_1's V_{cb} variations must not alter the value of I_c that drives Q_2 via the voltage developed across R_2.

In the circuits, Q_1 is a grounded-base level shifter that converts the "1" level emitter drive to a constant-current drive for the base of Q_2, independent of $-V$, which must equal or be less than V_{off} of the FET (assuming an enhancement-mode device). Q_2 is a simple inverter with positive and negative supplies of sufficient amplitude to control the gating FET.

The drive to Q_1 can take either of two forms. For current-sinking logic (Fig. 1), a dual-diode gate and a resistor to +5 V are used. A+5-V "1" level back biasis D_1 which turns on Q_1 through R_1 — D_2. A "0" level at D_1 deprives Q_1 of emitter current which, in turn, gates the FET on.

For current-sourcing logic (Fig. 2), a 2.4-kΩ resistor from a 3.6-V "1" level turns Q_2 on, gating the FET off. This circuit can be built for about 60 cents at single-piece pricing.

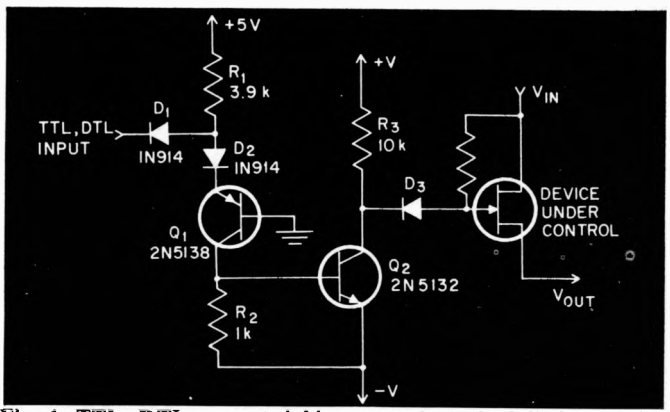


Fig. 1. TTL, DTL current-sinking control. A dual-diode gate is used at the input.

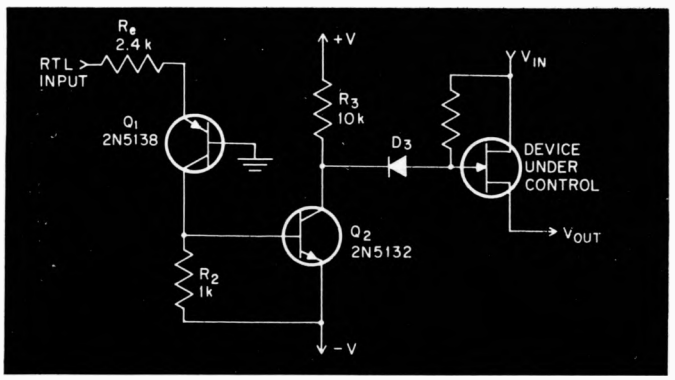


Fig. 2. RTL current-sourcing control uses a simple 2.4-kΩ resistor at the input.

IC NOR gate detects zero-axis crossing

THIS SIMPLE CIRCUIT gives an output pulse when an ac input waveform crosses the zero-voltage axis. The circuit uses just a single IC, a center-tapped transformer and two biasing potentiometers.

In the original application, the circuit was used to gate pulses and thus eliminate spurious transients that could occur during periods of zero pulse amplitude. Other possible applications include phase-control circuits, counting circuits, rectangular pulse shapers and some types of A/D converters.

As shown in Fig. 1, the input signal is transformer-coupled to the IC. The transformer serves two purposes: It steps down the input voltage, if necessary, to avoid exceeding the rating of the IC (±4 V for the μL914). Also, it provides signals of equal amplitude and opposite phase, at the two inputs of the NOR gate.

The two potentiometers provide a forward bias of about +0.8 V to the inputs of the gate. This bias offsets the zero logic level needed for the IC. (Measured value for the μL914 is 0.815 V at 25°C.) Initially, the bias pots are set to give 0.8 V and they are later readjusted for optimum circuit performance.

Since the NOR gate gives a logic-1 output only when the two inputs are simultaneously at logic-0, the complete circuit gives an output only when the input wave is at 0, 180 or 360 degrees. Typical waveforms are shown in Fig. 2.

Figure 2D shows the output waveform before final adjustment of the potentiometers. The pots can be readjusted to give a very sharp spike, as shown in Fig. 2E. After suitable bias adjustment, it's possible to obtain a spike narrow enough to define the zero-crossing point within ±2% of the wave period.

Of course, for noncritical applications, the pots can be replaced by fixed resistors. It should be remembered, though, that the trigger level of the IC is temperature sensitive, so the circuit won't hold its accuracy over a wide temperature range.

With the component values shown in Fig. 1, the circuit has a frequency response of 200 Hz to 10 kHz. Typical input voltage is 1 Vrms, though the basic circuit can be used with higher or lower voltages with a suitable transformer. Output amplitude is 1.2 V pk.

By readjusting the bias voltage below 0.8 Vdc, the circuit can be used to produce rectangular pulses (see Fig. 2D). The width of the pulse depends on the bias setting.

Frequency response of the circuit has been experimentally extended to 200 kHz using a different input transformer.

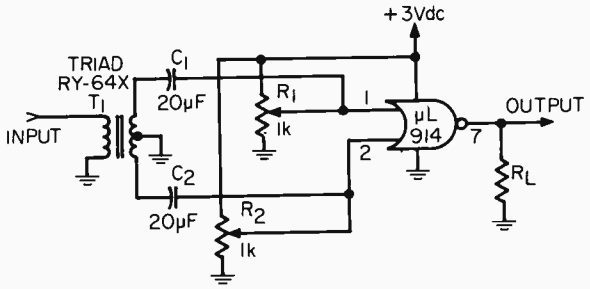


Fig. 1. Simple circuit gives a short-duration output pulse whenever the ac input waveform crosses the zero-voltage axis.

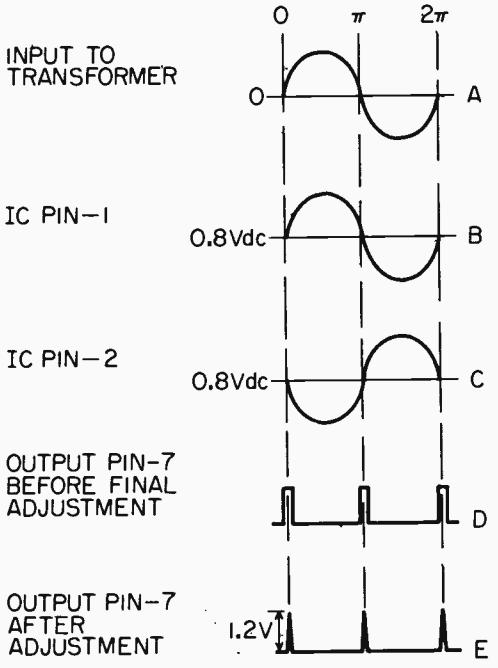


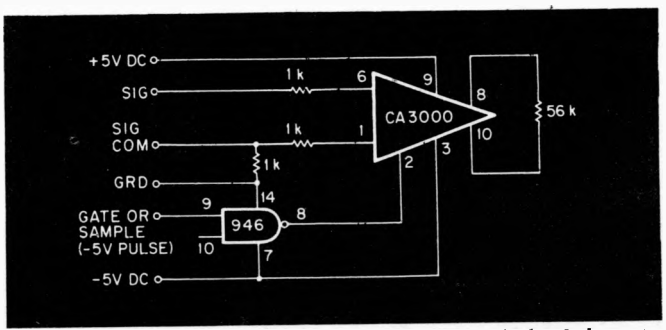
Fig 2. Timing diagram shows how the output pulse coincides with the zero-axis crossing. Width of the output pulse depends on the initial bias voltage.

IC functions as sampling amplifier or tone-burst gate

A LOW COST IC amplifier can be gated by applying digital pulses to its AGC line. Depending on the relative frequencies of the signal and the gate pulses, the circuit can be used either as a sampling amplifier or as a tone-burst gate. Only one IC gate and a few resistors are needed in addition to the basic IC amplifier.

With the components specified in the schematic, the circuit can provide up to 500,000 samples of the input signal per second. The minimum width for the sample pulse is 0.8 μs. If the load is reduced from 56 kΩ to 10 kΩ, then the minimum usable sampling-pulse width increases to 2 μs.

A type CA3001 amplifier (70-Ω output impedance)



Depending on the signal frequency and on the width of the gate pulse, this simple circuit is either a sampling amplifier or a tone-burst gate.

could probably be used instead of the indicated CA3000 (7-kΩ output impedance) to provide improved load driving capability. In the original application, however, the CA3000 was chosen because it has a larger AGC range (90-dB typical, compared with 60-dB for the CA3001).

The possible sampling frequency of 500,000 per second allows the circuit to be used for sampling signal frequencies up to 250 kHz. Alternatively, the width of the gating pulse can be increased so that it is wide compared with the period of the signal frequency. The output will then consist of a tone burst with duration equal to the length of the gate pulse.

The IC amplifier gives an output of +5 Vdc when full AGC is applied. In the amplifying mode, dc output doesn't exceed +4 V with a signal level of 2 V pk-pk. Thus the outputs of several amplifiers can be combined, using diodes biased to clip signals at a level of 4.3 V. This type of circuit would lend itself to multiplexers or tone-burst sequencers.

Fast logic circuits with high noise-immunity

THE LOGIC ELEMENTS described here all use diode feedback to prevent the transistors from reaching cutoff or saturation. Because the transistors are operated in the active region, switching is very fast. In effect the circuits are amplifiers having much less than unity gain for inputs above and below a narrow threshold region. Thus they tolerate input noise almost equal to the required input signal, with little or no change in output.

Figure 1 shows a basic inverter circuit. The inverter stage Q_2 is buffered by an emitter follower Q_1. Diode feedback from Q_2 collector to Q_1 base keeps Q_2 in the active portion of its load line, appreciably reducing the saturation and cutoff delays, t_s and t_d.

For the specified transistors, Motorola gives the following switching-time figures:

$t_s = 110$ ns
$t_d = 20$ ns
$t_r = 17$ ns
$t_f = 50$ ns

Using diode feedback, however, saturation and cutoff delays are reduced to around 2 to 3 ns. These residual delays seem to be related to diode switching time rather than to the transistor characteristics. The inverter switching times, t_r and t_f, are both much less than 4 ns, though it is difficult to measure these parameters accurately. Measurements were made on a Tektronix Type 585 oscilloscope with a Type 82 plug-in. The rise time of this combination is listed as 4.3 ns in the ×10 mode. Displayed rise time of the circuit was approximately 4.5 ns.

Propagation delay for each logic circuit is approximately 4.5 ns. This was measured by connecting three of the circuits in a ring-oscillator configuration. Oscillation frequency was 37 MHz. Propagation delay was calculated from the measured frequency using the following equation:

$$t_{pd} = \frac{1}{6f_0} \qquad (1)$$

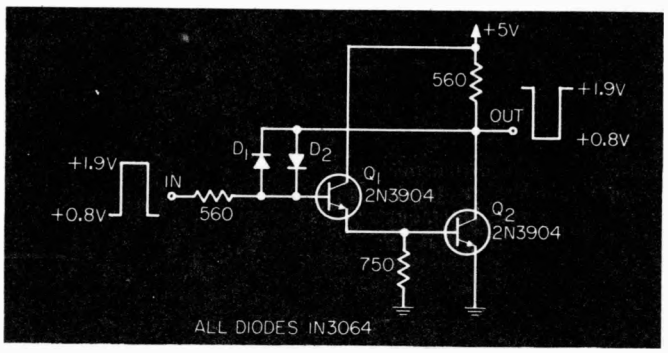


Fig. 1. Diode feedback in this inverter circuit keeps the transistors in the active region (avoiding saturation and cutoff).

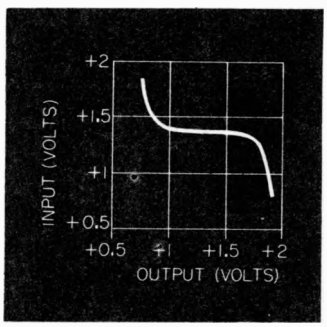


Fig. 2. Input-output transfer characteristic for the circuit of Fig. 1.

The circuit of Fig. 1 works as follows. Because transistors Q_1 and Q_2 have base-emitter voltages $V_{be(on)}$ of 0.7 V each, and the diodes have a forward drop of 0.6 V, Q_1 and Q_2 will conduct when an input voltage of +1.9 V is applied. And, as the collector of Q_2 drops to +0.8 V, D_1 will conduct. This reduces the base drive to Q_1 and Q_2 and prevents further voltage drop at the collector. The base-collector junction of Q_2 then has a reverse bias of 0.1 V.

When the input drops to +0.8 V, Q_1 begins to drop out of conduction. Then, as the collector of Q_2 rises to +1.9 V, D_2 conducts, thus restoring sufficient base drive to Q_1 and Q_2 to prevent further cutoff.

Since the output voltage-swing centers about +1.4 V, noise immunity at the input to an identical stage will be approximately half of the 1.2-V output swing, as shown in the transfer characteristic of Fig 2. Noise immunity can be further improved by adding extra diodes, D_3, D_4 and D_5, as shown in Fig. 3. In this circuit, the output voltages are +0.8 V (input +3.2 V) and +3.2 V (input +0.8 V) with a noise immunity of about 1 V.

Fig. 4 shows how extra diodes can be added at the input of a basic inverter circuit to form an AND-gate. Fig. 5 shows the resulting transfer characteristic. Many other gate configurations are possible.

With these circuits, base-emitter and base-collector capacitances have very little effect on switching speed. This is because of the emitter-follower connection of Q_1 and the minimal voltage change oc-

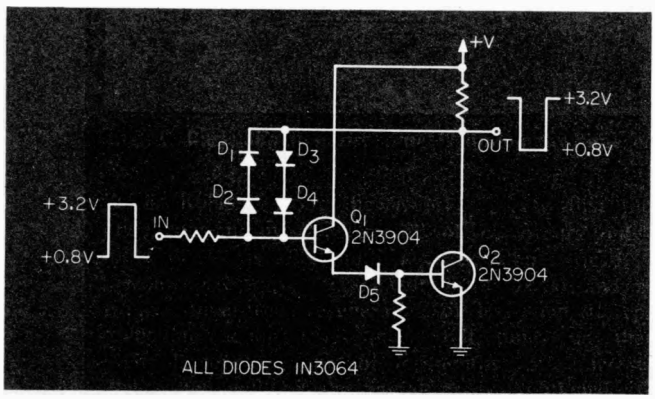


Fig. 3. With extra diodes, as shown here, the noise immunity is improved.

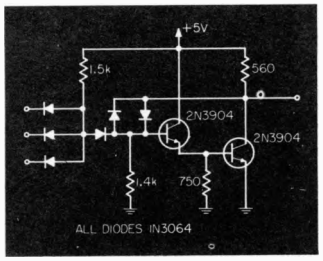


Fig. 4. Diodes can also be added at the input to convert the basic inverter into an AND-gate.

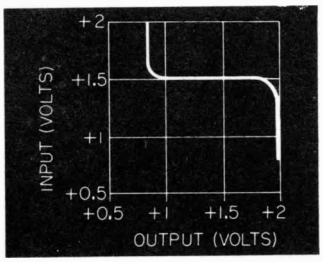


Fig. 5. Input-output transfer characteristic for the circuit of Fig. 4.

curring at Q_1 base. Capacitance of the feedback diodes does introduce Miller effect, though. So, to insure maximum speed of operation, the diodes should be bast-switching, low-capacitance types.

Yet another advantage of these logic circuits is that the transistors needn't be optimized for $V_{ce\ sat}$. High-frequency-amplifier transistors can be used with their typically low output and feedback capacitances.

Split serial adder is fast yet simple

NOW THAT IC manufacturers are offering dual digital circuits in single packages, it is possible to build a split serial adder which uses the same number of IC packages as a conventional circuit, yet which offers twice the speed.

Before looking at an improved circuit, let's look first at the conventional serial adder shown in block-diagram form in Fig. 1. This circuit needs two shift registers of length N (where N is the length of the input words). These registers temporarily store and shift the two binary words that are to be added. Serial outputs of the two registers are added, and the sum is fed back to the serial input of one of the registers. At the end of the add cycle, the register having the serial feedback holds the sum $A+B$.

A carry-store flip-flop stores the CARRY OUT of the preceding sum $Ai + Bi$. The output of this flip-flop provides the CARRY IN to form the next sum $Ai+1 + Bi+1$. Also needed for a conventional serial adder are a bit counter (to determine when N bits have been added) and miscellaneous gating (to gate the adder clock).

Additional time for the circuit of Fig. 1 is NTc, where Tc is the clock period.

A split adder, however, allows us to achieve an add time of only $(N/2)\ Tc$, without using any extra IC packages. Fig. 2 shows a practical circuit for an 8-bit adder. In this circuit we split the input words into two portions, with one portion containing the odd bits and with the other containing even bits. The sums of the odd bits and even bits are formed separately but simultaneously. The CARRY OUT of the odd sum is used directly as the CARRY IN for the even sum. The CARRY OUT of the even sum is stored in a flip-flop whose output provides the CARRY IN for the odd sum. A bit counter divides by $N/2$ to determine when the last bits have been added.

Suggested IC type numbers are indicated in Fig. 2. Though four registers are needed (as compared with two for the conventional circuit), each register has a length of only $N/2$. Circuit operation can be easily understood if one compares the timing diagram of Fig. 3 with the schematic.

If we wish to add words having odd bit lengths, then we must modify the timing circuit. The odd bit registers will be one bit longer than the even registers. So the bit counter must be modified to count to $(N/2) + 1$ instead of to

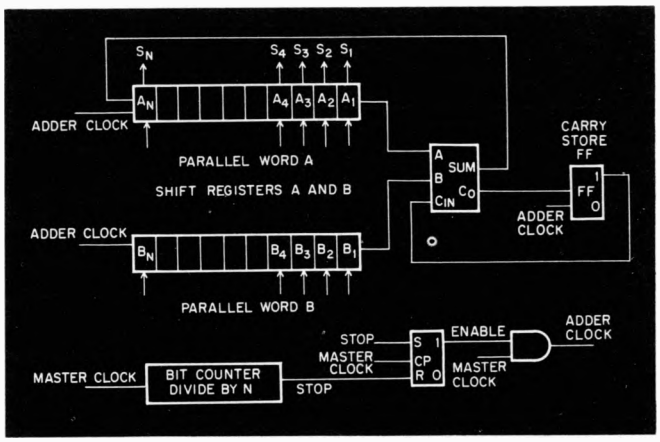


Fig. 1. Block diagram of a conventional serial adder.

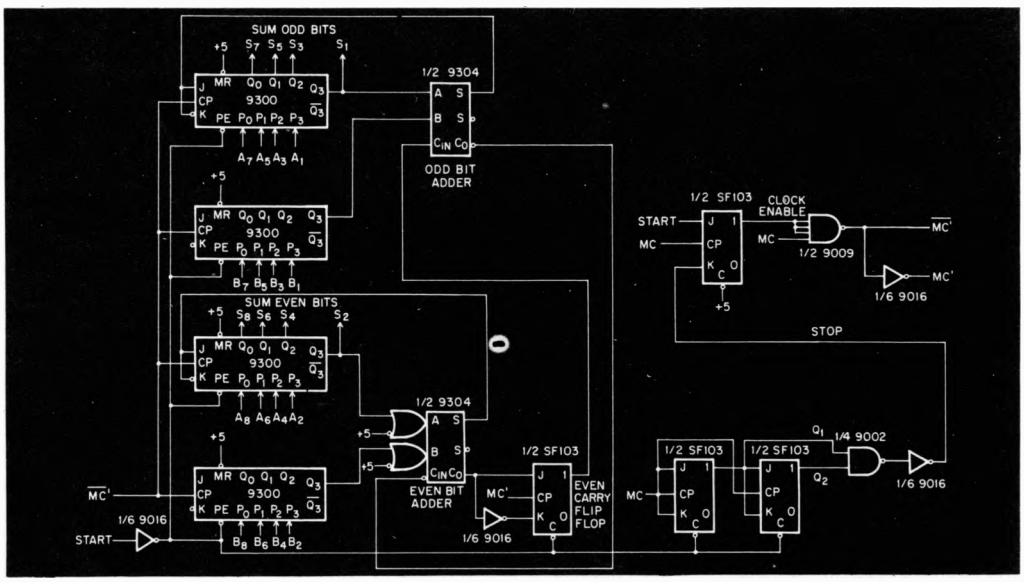


Fig. 2. Practical circuit for an 8-bit split serial adder.

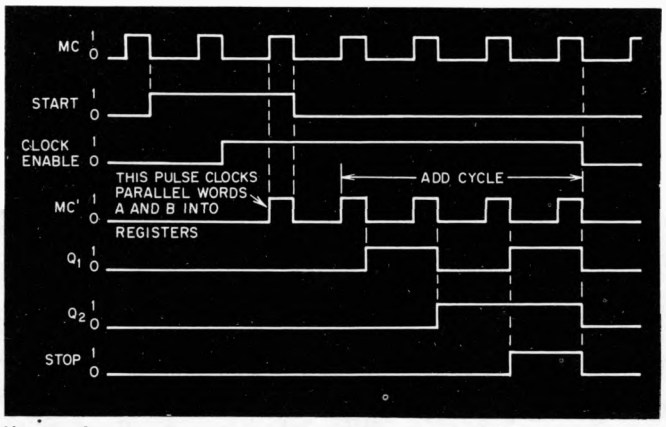


Fig. 3. Timing diagram for the 8-bit split adder.

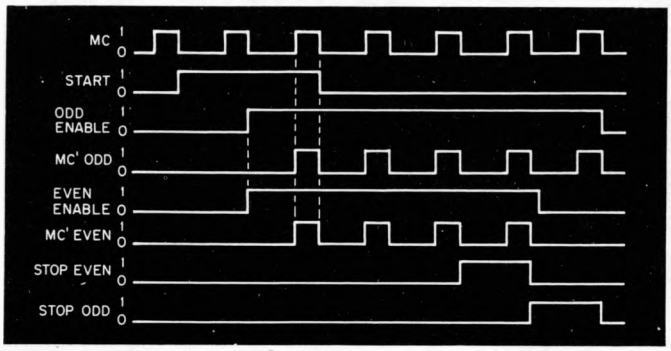


Fig. 5. Timing diagram for the 7-bit split adder.

$N/2$. Gating must be provided to disable the even-register clock after state $N/2$, while the odd-register clock must be disabled after state $N/2 + 1$. Fig. 4 shows the modified timing circuit for a 7-bit adder, and Fig. 5 is a timing diagram for the modified circuit.

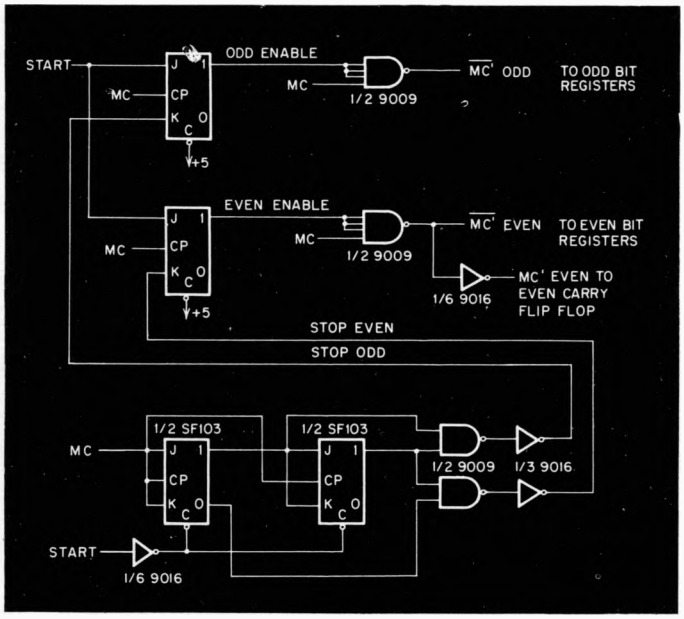


Fig. 4. Modified timing circuit for a 7-bit split adder.

A broadband low-noise gate using hot-carrier diodes

THIS WIDEBAND gate circuit combines the advantages of Schottky-barrier diodes and FETs, to overcome many of the disadvantages of other gate circuits. Signals are switched by a fast-response hot-carrier-diode bridge which is turned on and off by a low R_{ds} FET. Two solar cells, illuminated by a pair of lamps, supply 1.6 volts of isolated power for bridge turn-on.

Resistors R_1 through R_6 bias the bridge so that it is normally non-conducting. When a positive clamp pulse occurs, the FET applies a reverse bias voltage to the bridge which then starts to conduct between the input and output corners. Turn-on time is about 10 ns. Removal of the clamp pulse causes turn-off within 100 ns.

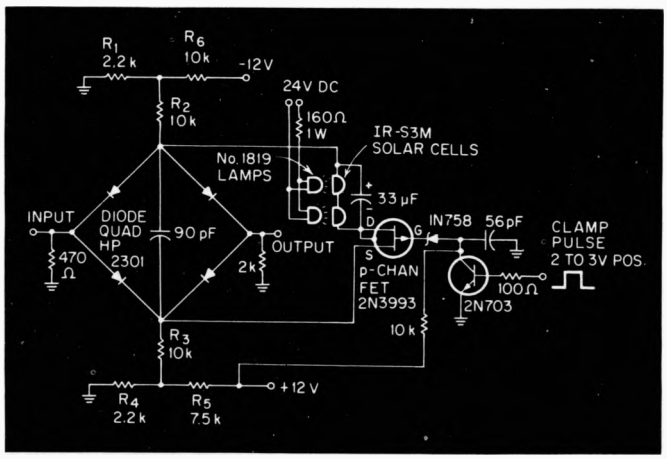
The diode bridge will accept signal voltages up to 4-volts pk-pk. On-off ratios of 60 dB are possible at frequencies up to 20 MHz. Response is down 5 dB at 40 MHz.

Note that in this circuit the corners of the diode bridge are switched simultaneously by a low-impedance source. This minimizes the transients appearing at the output.

The switching technique contrasts with that used in other gate circuits with diode-quad bridges. In most other circuits, the bridge is turned on by two pulses which are applied in anti-phase to opposite corners of the bridge. The 180-degree phase shift is usually derived either from an inverter followed by an amplifier, or from a center-tapped transformer. In either case it is difficult to achieve accurately the required phase shift. Even a small error in the phase of the switching signals will cause unwanted transients at the bridge output.

With ac coupling of the clamp pulses, such as with a transformer, there is the added disadvantage that the bridge cannot be gated on for long time periods. With the circuit described here, however, the gating period can be any required value from a few nanoseconds to several hours.

In this circuit, bridge bias voltages are relatively non-critical. Variable resistor R_6 allows adjustment for exact zero offset. The lamps are operated at reduced voltage, for long life. When operated at 20 volts, the specified lamps have a life of over 10,000 hours. Small reflectors can be placed behind each lamp to increase the efficiency of the lamp/solar-cell combination.



In this unusual gate circuit, a Schottky-diode bridge is switched by a FET. Two illuminated solar-cells provide a floating low-impedance bias source.

Fast binary-to-BCD

THE CIRCUIT in Fig. 1 converts binary numbers to BCD without additional control circuitry. The conversion time is determined only by the propagation time through gates. While the number of individual gates is large, the conversion time is much faster than that available with the common serial methods.

The basis for this circuit is a BCD adder, Fig. 2, which adds two BCD numbers (each with a value between 0 and 9) to give the sum (in BCD) and a carry output if the sum is 10 or greater.

One can usually convert the binary contents of a scaler or the binary value of toggle switches to BCD by adding the decimal weights of each lit binary lamp or of each set switch. A binary sequence such as 100011101 is converted to decimal as the sum of 128 + 16 + 8 + 4 + 1. This approach can be used with the adder in Fig. 2.

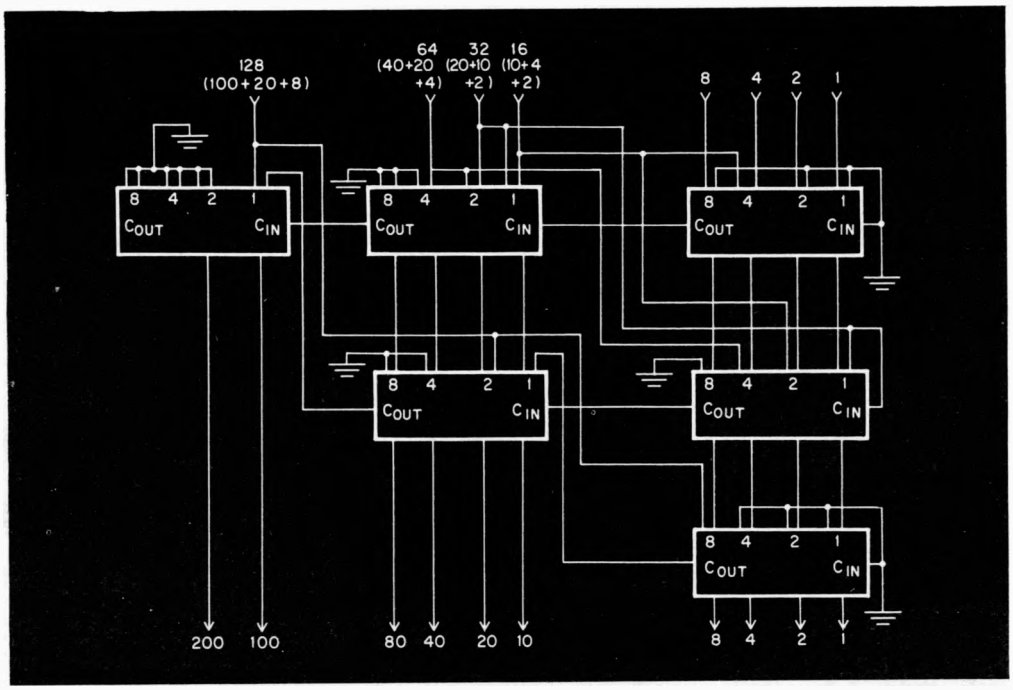


Fig. 1. This circuit converts binary numbers to BCD numbers without additional circuitry.

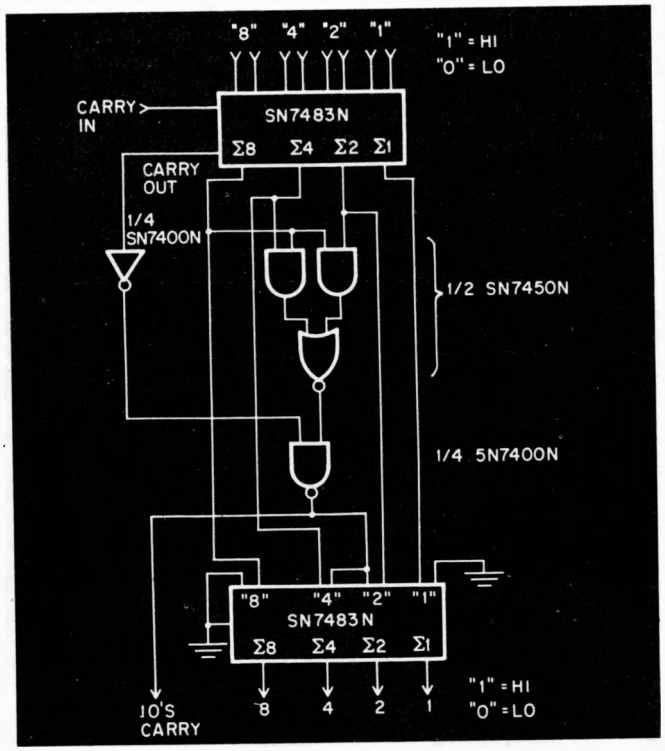


Fig. 2. This BCD adder will add two BCD numbers to give the sum in BCD and a carry output if the sum is greater than 9.

The binary values are broken down to their decimal components and added as shown in Fig. 1 where an 8-bit converter has been implemented. Not all inputs to each decimal adder can be used since this would have a possible sum of 31 (15 + 15 + carry) while a decimal adder, by definition, can only sum 9 + 9 + a carry input.

In some applications, an additional adder can be eliminated by presenting a decimal number to the adder as two addends. This has been done to the middle adder in the units column. In this instance, a "2" is presented to the adder as a "1" and also as an input carry (= "1"). This is not necessary in this case because this "2" could have been applied to the unused "2" input on the last adder in the units column where the largest number presented to this adder is "9" (from the adder above it) plus an "8."

It takes about 300 ns for an 8-bit adder to change from "199" to "200" by the application of a pulse to the carry input of the top adder in the units column. A 27-bit converter using this method requires about 1.8 μs. However, these may not be worst-case times.

A 12-bit converter uses 13 adders and in one implementation, a 27-bit converter required 23 boards. Others may discover a more direct method of determining the interconnections for minimum board count.

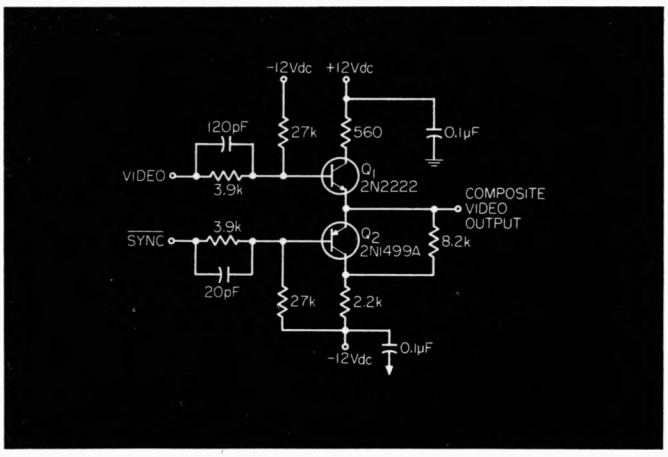
Reference

TI Network News #127, Texas Instruments, May 15, 1967.

Inexpensive video distribution amplifier converts logic signals for TV displays

THIS CIRCUIT provides a simple and inexpensive method of converting logic signals to EIA standard for video in computer-generated digital television displays. The circuit accepts video and inverted sync signals from the display computer (logic "1" = 5 volts, logic "0" = 0 volts) and generates +1 volt for video, −0.1 volt for blanking, and 0.4 volt for sync. The amplifier is designed to work with a 75-Ω load (EIA standard load) and is capable of driving several monitors using the "loop through" technique (i.e., connecting several monitors in parallel with a 75-Ω termination attached at the last monitor to terminate the cable). The frequency response is flat within 1 dB from dc to 20 MHz

The circuit consists of three resistors connected in series to form a voltage divider between the plus and minus supplies. The transistors are used as switches to select the proper combinations of resistors to give the desired output voltage. Five-percent resistors can be used throughout the circuit, but since the load is part of the voltage divider network, care must be taken to insure that it also is held at 75 Ω within 5 percent.



Low-cost video amplifier is compatible with IC logic and EIA standard displays. Frequency response is flat within 1 dB over 20-MHz bandwidth.

The transistors specified are intended as examples of types that can be used. The 2N2222 can be replaced by a less expensive switching type, such as the 2N914, as long as the beta is approximately 50 or greater at the video frequency used. Transistor Q_2 switches only at the sync frequency and therefore can be almost any low-frequency type.

The 120 pF speed-up capacitor is adjusted to give a slight overshoot with 10-MHz video. This was found to be helpful when using inexpensive monitors with low-bandwidth video circuits. Other values can be substituted depending on the application.

The input impedance of the circuit is 50 kΩ for the video input and 10 kΩ for the inverted sync input. This allows operation with most integrated-circuit logic modules without the use of separate drivers. Input terminations can be added as desired.

Simple circuit for division by 8, 9, 10

GATELESS CIRCUITS for division by 9 or 10 require at least four flip-flops. By adding only four gates (a single quad NAND) we can divide by 8, 9 or 10. The 8-9-10 divider in Fig. 1 uses J-K connected Fairchild 9040 flip-flops and a 9046 quad NAND.

The divisor is selected by the logic levels on control lines A and B as follows:

Control Line A	Control Line B	Divide By
0	0	8
0	1	9
1	0	10

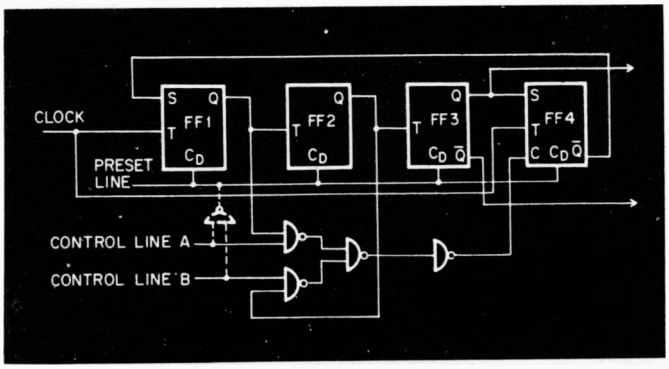


Fig. 1. Circuit for divide-by-8 or -10 and for unambiguous divide-by-9 if the dashed-line gate is added.

Clock Pulse	FF1	FF2	FF3	FF4	Divide By
0	0	0	0	0	
1	1	0	0	0	
2	0	1	0	0	
3	1	1	0	0	
4	0	0	1	0	
5	1	0	1	1	
6	0	1	1	0	
7	1	1	1	1	
8	0	0	0	0	8
8	0	0	0	1	
9	0	0	0	0	9
6	0	1	1	1	
7	0	1	1	0	
8	1	1	1	1	
9	0	0	0	1	
10	0	0	0	0	10

Fig. 2. Truth table for the Q outputs. The flip-flop states for clock pulses 0 to 5 do not depend on the division (determined by the levels on the control lines).

But the 11 combination on the control lines causes the circuit to lock up (at 0111) unless the NAND, shown in dashed lines in Fig. 1, is used for reset.

To begin, the flip-flops must be preset so that $Q_1Q_2Q_3Q_4$ are at 0000. Presetting is accomplished by pulsing the preset line once with logic 0 or by having logic 1 on each control line.

Presetting is not essential when the circuit is to divide by only 8 or 10. But without preset, for certain starting combinations (like 1010, 0101 or 0111 at $Q_1Q_2Q_3Q_4$), when the circuit must divide by 9 it may lock up.

The maximum allowable clock frequency depends on the propagation delay of the flip-flops. The maximum carry time of the circuit is thrice the prop delay of one flip-flop, assuming equal delay for each flip-flop, so the clock pulses must be spaced at greater intervals than the carry time.

The output is taken from Q or $\bar{Q}$ of FF3. The truth table in Fig. 2 shows that the output mark-space ratio is 1:1 for division by 8 or 10, and 4:5 for division by 9.

Three-state logic circuit

THE SIMPLE and reliable logic circuit shown in Fig. 1 can generate one "off" state and two discrete "on" states. A suitable decoding circuit is shown in Fig. 2. The complete circuit, including both the counter and decoder, uses just one Motorola MC790P dual J-K flip-flop and one quadruple dual-input gate type MC-724P.

Circuit operation relies on an important property of MC-790P J-K flip-flops. They will toggle on a negative transition at the trigger input when both steering inputs are low; yet they will maintain their states when both steering inputs are high.

The table in Fig. 1 shows the various output states for successive input pulses. At time t_n, the steering inputs of flip-flop "b" are tied to A and are low. B is high at t_n, forcing a low output from the RTL gate "c". Thus the steering inputs of flip-flop "a" are low.

The first trigger pulse applied to both flip-flops changes their states (t_{n+1}). Note that the output of gate "c" still remains low, allowing flip-flop "a" to toggle on the next trigger pulse. But the high level of A inhibits the flip-flop "b" from changing state. The second trigger pulse therefore generates the states shown in the table under t_{n+2}.

At time t_{n+2}, outputs A and B are both low. These logic levels generate a high at the output of gate "c", thus inhibiting flip-flop "a". The steering gates of flip-flop "b" are both low and the next trigger pulse toggles only flip-flop "b", restoring both flip-flops to their respective states exhibited at t_n.

When power is initially applied to the circuit, one may encounter an illegal state with A high and B low. However the first trigger pulse will restore the condition indicated under. t_n.

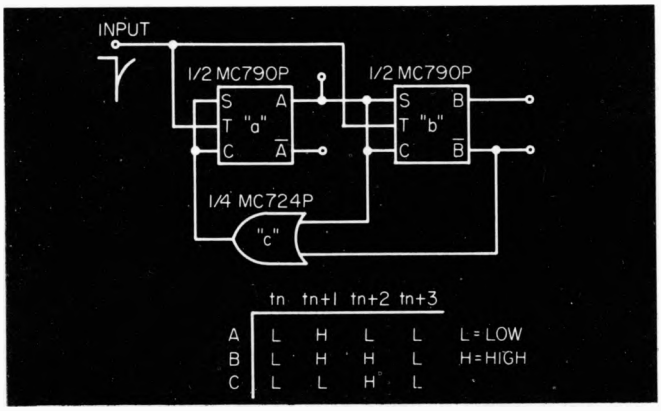


Fig. 1. This simple counter has three discrete stable states. Output states for successive input pulses are shown in the table.

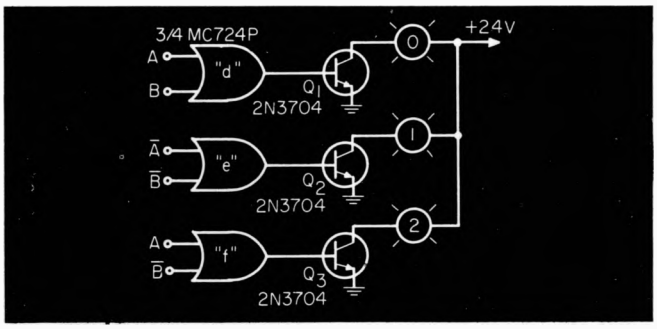


Fig. 2. A decoder circuit can use the remaining three gates of a quadruple dual-input IC. With the transistors shown here, the circuit will drive loads of up to 250 mA.

The remaining three gates of the MC724P can be connected as shown in Fig. 2. Each gate will drive a buffer transistor. With 2N3704 transistors, connected as shown, the circuit will drive loads of up to 250 mA. The loads can be relays, lamps or other suitable devices, depending on the application.

The circuit was originally developed for use in a dual-slope integrating DVM. The first logic state was used to charge the integrating capacitor and the second and third states were used for the discharge cycle. A ripple-type counter had been considered for this application but the circuit described here was found to be preferable. With a conventional ripple-type counter, an extra count was generated intermittently because of delays caused by rippling through the counter and by the reset time of a one-shot circuit.

The decoding circuit of Fig. 2 was developed for an application that required a three-position scanner. The scanner was driven from RTL logic at a rate of three steps per second. The load for the decoder consisted of two mercury-wetted relays and an indicator lamp.

Universal digital interface

THERE ARE MANY different forms of digital logic. For example, logic *"1"* can be represented by zero voltage or by

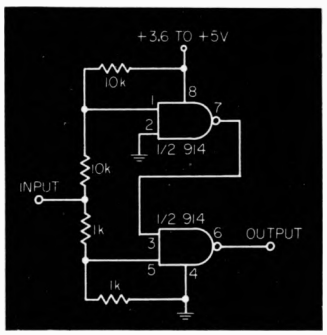


Fig. 1. Universal interface circuit gives +3 volts output with zero input and zero output with positive or negative non-zero inputs.

some positive or negative voltage level, with logic *"0"* being represented by the complementary state. The diversity of logic levels causes compatibility problems in the design of peripheral equipment for digital systems. Ideally, one piece of equipment should be capable of interfacing with any digital system.

The circuit shown in Fig. 1 will interface with many different types of logic, both positive and negative. The only

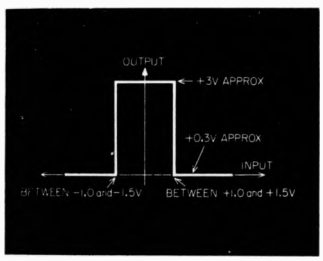


Fig. 2. Input-output transfer characteristics show that positive output occurs only with near-zero inputs.

limitation is that one of the two logic states must be zero volts. Total parts cost is around one dollar. Of course, for complete equipment compatibility, code converters may be required in addition to the logic-level converter described here.

Basically the circuit is a digital inverter. It works as follows:

When the input is negative, pin 1 of the upper gate is biased negative and hence the upper gate has a logic *"1"* output. Pin 5 of the lower gate is also negative, but the logic *"1"* at pin 3 causes the lower gate output to be at logic *"0."*

When the input is positive, at some voltage above +1.5 volts, pin 1 of the upper gate is positive and hence the output from the upper gate is logic *"0."* Pin 5 of the lower gate is positive and this generates a logic *"0"* output.

When the input is zero, pin 1 of the upper gate is biased positive by the resistive divider, thus causing a logic *"0"* at its output. The lower gate has both of its inputs at *"0,"* causing logic *"1"* at its ouput.

Thus the complete circuit generates a logic *"1"* output which is approximately +3 volts for zero input. For a non-zero input, the output is logic *"0."*

Figure 2 shows the input-output transfer characteristics. If the circuit is regarded as an inverter, then its interpretation of different input levels can be summarized as follows:

Logic *"1"* $\geq$ |1.5| volts

Logic *"0"* $\leq$ |1.0| volts

The inverted output is compatible with RTL and DTL logic. For non-inversion, an inverting buffer such as the 900 can be placed in series with the output (pin 6 of the 914). Of course, other types of inverting gates are equally suitable.

Fast BCD-to-binary converter

Both binary and binary-coded decimal number forms occur in digital systems. Because decimal coding is simpler and more familiar, BCD is widely used for manual input devices like thumbwheel switches. But most logical and arithmetic operations are performed in binary code. Therefore, a method of BCD-to-binary conversion is often needed with computer input devices.

Various methods of conversion have previously been described. These basically fall into three categories: direct-conversion logic matrix, simultaneous BCD-and-binary counters and BCD division using shift registers and additional control logic. The first method suffers from the requirement for ex-

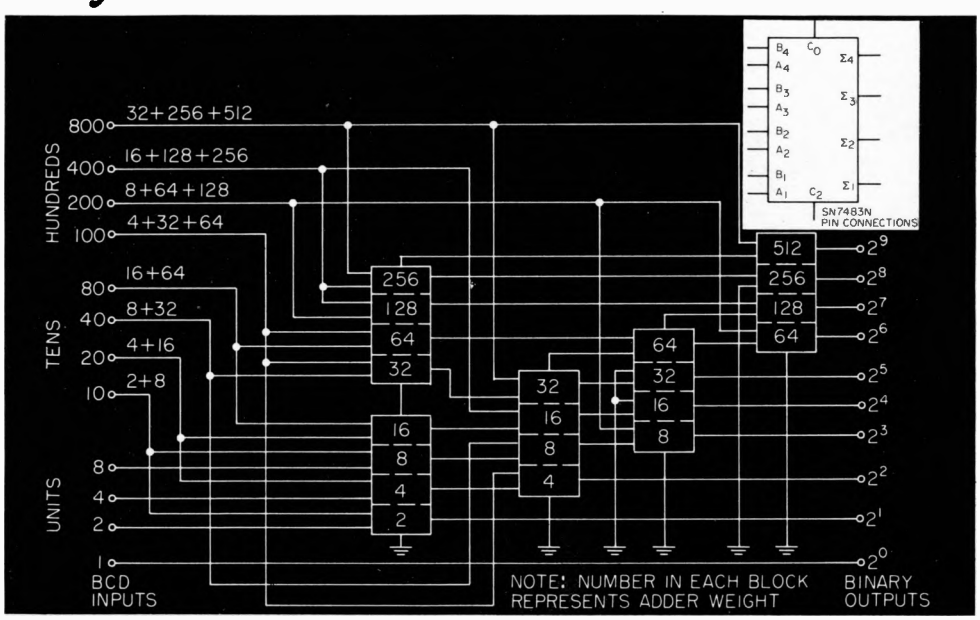


Fig. 1. Simple BCD-to-binary converter uses IC quadruple binary adders to sum the binary equivalents of the parallel BCD inputs.

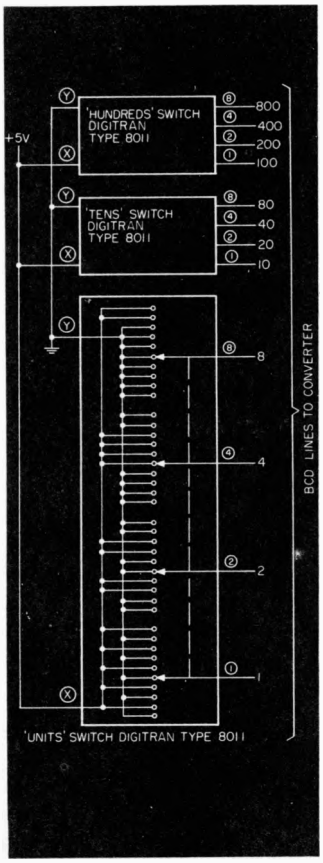


Fig. 2. Typical manual-input circuit using thumbwheel switches.

tensive hardware, the second from a relative lack of speed. The third method requires only one clock pulse per bit; but it also needs a moderate amount of hardware.

The method described here combines the advantage of high conversion speed, minimum hardware, and no requirement for additional control logic. As shown in Fig. 1, the method simply consists of representing each input line of the BCD coded number by its equivalent sum of binary numbers, and adding together these numbers in quadruple binary adders, like Texas Instruments' SN7483N. For example, the input line with weight 200 is equivalent to (8 + 64 + 128); so it is applied as an input to binary adders with weights of 8, 64, and 128.

As illustrated, conversion of a three-digit decimal number to its equivalent 10-bit binary representation requires only five ICs. Conversion speed is limited only by the propagation time of the adders. With the specified ICs it is approximately 250 nanoseconds.

The technique can be extended to numbers with more BCD digits, and can also be used for code weights other than 8421. For example, a four-digit to 14-bit conversion can be done with eleven ICs.

Of course, interface between the manual input device and the converter circuit depends on the application. Fig. 2 shows one suitable arrangement, using thumbwheel switches.

Section 18
RELAY & SWITCHING CIRCUITS

Precision-Timed Short-Interval Relay Switch

THERE EXISTS need in ordnance testing to apply specific potentials to pairs of terminals for precise time intervals, also to pass a definite quantity of electrical energy through a conducting path for a short but definite time. In other fields, it is necessary to pass a known current across the contact junction of two metals for a minute but accurate instant. In electrical therapy, need exists for applying a fixed potential for an accurately known but short increment of time to a patient's body. These applications generally require the closure of a metallic switching element during the required interval of voltage or current application.

The relay switch to be described was devised to meet the requirements outlined. It is relatively low in cost, trouble free, and has excellent accuracy. The basic circuit can be used to either open or close an electric circuit for any reasonably short metered instant.

Figure 1 outlines the arrangement of components. RL_1, RL_2 and RL_3 are contacts operated by relay RL. *Capacitors* C_1 and C_2 are paper types.

The *cycle time* of the relay is defined as the interval during which RL contacts are first opposite to the shown positions until RL contacts are again as shown. Arc *extinction voltage* is that voltage across C_2 which is present near the start of cycle time at the instant contact arc on RL_1 is extinguished.

Switch 1 transfers a definite quantity of electrical charge to coil of relay RL. Contacts RL_1, RL_2 and RL_3 operate with closing of the relay. At that instant the polarity across RL is reversed, due to the collapsing magnetic field; and the potentials across RL and C_1 add in series to drive current across the opening RL_1 contacts.

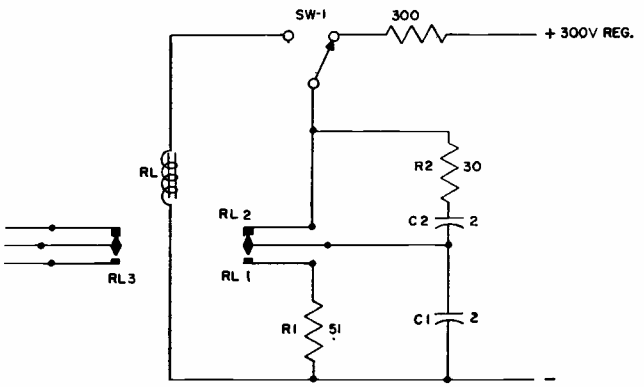
If C_2 were shorted out, then RL would remain operated for a relatively long interval, or until the electrical energy stored in RL and C_1 was insufficient to maintain the required magnetic flux.

With the circuit shown, however, RL_2 in opening unshorts capacitor C_2. At that instant the charging current I into C_2 is large. It should be carefully noted that the potential appearing across C_2 is opposed to, or bucking the combined voltage of RL and C_1.

The combined voltage across RL and C_1 is decreasing while the bucking voltage across C_2 is increasing. The situation will exist until the difference of the opposed potentials is too small to maintain the arc across the opening RL_1 contacts. At the time of arc extinction, the collapse of the flux field in the RL magnetic circuit is necessarily essentially complete.

If we consider Q to be the quantity of electricity stored in C_2 at arc extenction, we may write: $Q = It$ where I is the average current flowing into C_2, during its charging time t, prior to arc extinction. But the quantity stored in C_2 is given by $Q = CE$. We may then write $It = CE$, and by inspection it can be seen that the smaller the value of C_2, the higher E will become in time t. The E limit is set by arc extinction which terminates the charging of C_2. Additionally, it can be shown that the smaller the value of C_2, the shorter the time t required to build arc extinction voltage across C_2.

For good repeatability of cycle time, the original charge in C_1 should be appreciable. The faster the operate time becomes, the greater the velocity with which the armature of R_1 will strike its pole piece If C_2 has been chosen small enough, the rebound velocity of the armature at the time contacts RL_1, RL_2 and RL_3 again operate will be nearly as great



Accurate cycle time of 12 msec is provided by values shown for the short-interval relay switch.

as the velocity with which the armature struck the pole piece in closing. By these means, a relatively slow relay may be made to exhibit a very short cycle time characterized by high repeatability.

Slugged relays are not suitable for this circuit, and no spark suppression circuits should be used across the coil of *RL*. Arc erosion of RL_1 contacts is negligible, since the circuit action is such as to cause contact arc life time to closely approach zero as a limit.

Contacts RL_1 must discharge the residual energy in C_1 through R_1 during the cycle time. Resistor R_1 is, therefore, a vital part of this circuit. Certainly the value of R_1 must be so chosen that 5 × time constant is equal to, or less than the cycle time. It is very desirable to choose R_1 as low as possible consistent with contact current rating, so as to assure timing accuracy. Contact RL_2 is protected by resistor R_2. The discharge time required for C_2 is also important, and must be kept to a minimum. It is suggested that the discharge time for C_2 be as short as possible consistent with contact current rating capabilities.

Values for C_2 may be determined by experiment. A decade box may be employed in a jury rigged circuit to select C_2 size for a specific cycle time. Proper selection of component values and voltage will result in an extremely accurate short interval cycle time. The switched circuit is handled by contacts RL_3.

Using a Potter-Brumfield MH-5576 65 volt relay with C_1 of 2μf, C_2 of 2μf, and a start potential of 300 volts, a cycle time of 12 milliseconds plus or minus 1 per cent was obtained. The circuit is being used in test instrumentation on a contract with Diamond Ordnance Fuse Laboratories.

SCR Switch Eliminates Amplifier for Photoelectric Readers

SIMPLIFIED CIRCUITRY, reduction of components, and increased available output power (more than 20 watts) are a few of the advantages of using a silicon-controlled switch instead of a multi-stage amplifier for photoelectric readers. Storage capability is also an asset of the controlled switch. Its thyratron-like characteristics maintain an output after the photoelectric stimulus subsides, until cut-off by control circuitry. The controlled switch, like the amplifier, isolates the stimulus from the operational circuitry.

The circuit to the right of the broken line in Fig. 1 is the storage amplifier, consisting of a silicon-controlled switch and associated circuitry. A storage

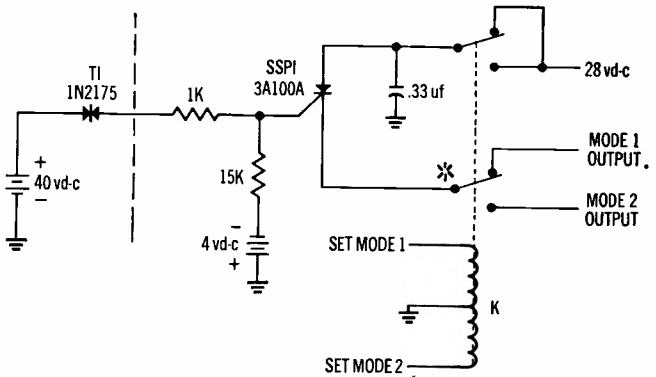


FIG. 1—Complete circuit of silicon controlled switch for photoelectric reader.

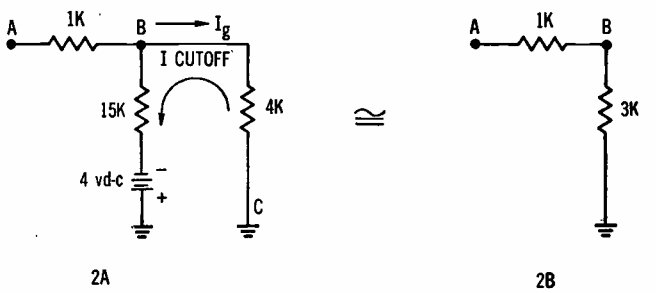


FIG. 2—Equivalent circuit of amplifier before firing.

amplifier is required for each photoelectric stimulus or bit. The bit is represented by the 40-v supply and the 1N2175, photo-duo-diode.

The circuit is for a two-mode operation, which doubles the switching capability of the reader. When using the two-mode operation, all the relays to be energized by the first mode must be the latching type, similar to relay *K* of Fig. 1. The relays energized by the second mode may be the conventional single-coil type. Latching relays are not required in the single-mode operation.

The asterisk pole of relay *K* in Fig. 1 is to remind the reader that a similar pole is required for each bit in the two-mode operation. The anode supply requires only one pole and capacitor, regardless of the number of control switches used. The pole removes the anode supply for approximately 3 μsec, the travel time of the relay wiper, when switching from one mode to another. This action, with the assistance of the —4v dc negative bias, cuts off the controlled switch. The function of the capacitor is to prevent the controlled switch from being re-

fired by the application of a step anode supply voltage.

The circuit of Fig. 2 is equivalent to that of the amplifier prior to being fired. The maximum gate voltage at point B required to fire the controlled switch is 0.8v dc, with a maximum gate current I_g of 0.2 ma. I_{cutoff} may be calculated to be

$$I_{cutoff} = \frac{4}{19{,}000} \cong 0.2 \text{ ma} \qquad (1)$$

since point A can be considered to be open circuited because the impedance of the 1N2175 approaches 100 megohms in the dark state. E_A required to obtain an I_g of 0.2 ma is

$$\frac{E_A}{4{,}000} \times \frac{15}{19} = 0.4 \text{ ma} = I_{BG} \qquad (2)$$

where $I_{BG} = I_g - I_{cutoff} = 0.2 - (0.2) = 0.4$ ma (3)

$$E_A = 4 \times 10^{-4} \times 4 \times 10^3 \times \frac{19}{15} = 2.02\text{v dc} \quad (4)$$

$$I_{AB} = \frac{2.02}{4{,}000} = 0.505 \text{ ma} \qquad (5)$$

Therefore, the maximum gate power required to fire the controlled switch is

$$E_A \times I_{AB} = 2.02 \times 0.505 \times 10^{-3} = 1.02 \text{ mw.} \quad (6)$$

The 1N2175, a photo-duo-diode, output gates the controlled switch. This output varies depending upon the load and the illumination intensity striking its focal lens. With an illumination intensity of 800 foot-candles, and loaded as shown in Fig. 1, the average output is 35 mw. Comparison of this output with that of Eq. 6 indicates the capability of the 1N2175 to cause the controlled switch to fire.

Step Switch Pulser

A CIRCUIT TO ADVANCE automatically a step switch at a relatively constant predetermined rate is given here. This circuit lends itself to automatic test equipment featuring go-no-go evaluations. The output wave form is referenced to the common and normally-open contacts of the output lines.

R_1C_1 form a conventional charging circuit. The voltage to which capacitor C_1 charges is equal to

$$\frac{e_{in}\,(R_3 + \beta R_5 R_4)}{R_1 + R_3 + \beta R_5 + R_4} + e_{CR1}.$$

Resistor R_s, provides the discharge path of capacitor C_1 which controls the output pulse width t_p. Resistor R_5, provides the path for the pulse off time. Resistor R_4 and diode CR_1 furnish a negative bias which prevents false relay actuation at high temperatures.

A 20 vdc voltage applied to R_1 causes C_1 to charge. The relay energizes when the voltage at the junction of R_1, C_1, R_2, and R_3 is of sufficient magnitude to produce ample relay current. This time period is denoted as t_o as indicated on the waveform diagram. The off time t_o is controlled by resistor R_5. The range of R_5 adjustment is t_o and lies between 20 msec to 7 sec.

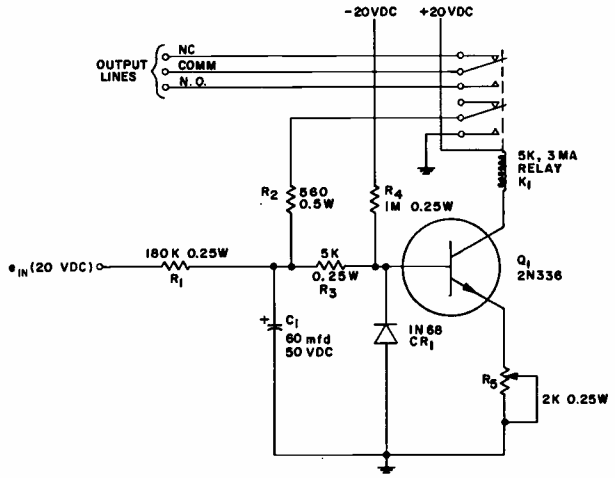


Fig. 1. Circuit for step switch pulsing.

When the relay is energized, C_1 discharges through resistor R_2. The relay remains energized until the voltage across C_1 stops supplying the required driving current to maintain relay current. This actuation period is indicated on the waveform schematic at t_p. For the circuit shown t_p is a fixed time at 80 msec. In most instances a pulse width of 10 to 20 msec is required for

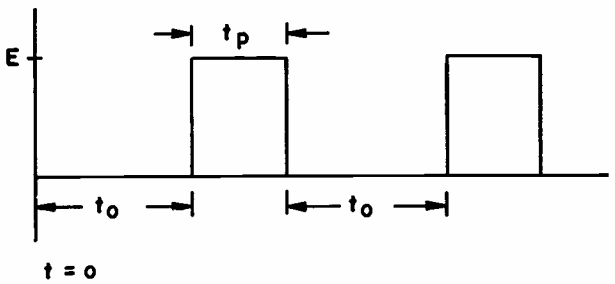


Fig. 2. Output waveshape shows on and off times.

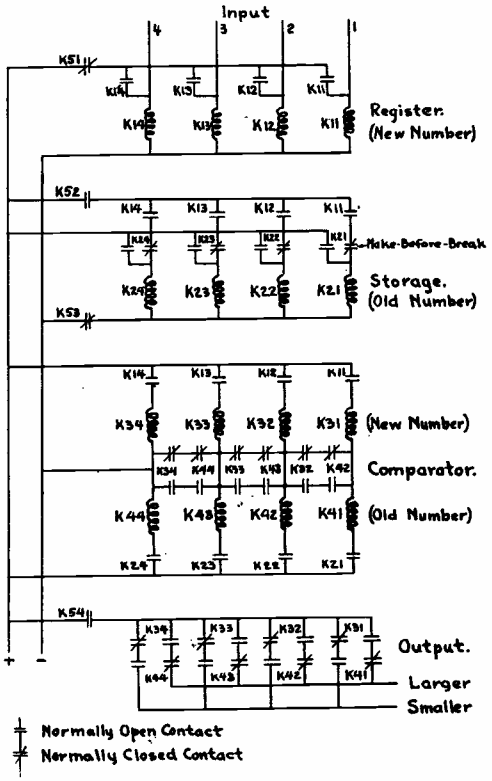
positive operation of a step switch. Therefore, 80 msec is a good and reasonable time for reliable operation.

The circuit was operated at an ambient temperature of −40 to 55C with an overall repeatability of 10 per cent of initial conditions. The power requirements are 20 vdc at 4 ma maximum, and −20 vdc at 1 ma maximum. Both supplies should be regulated to at least 1 per cent.

Relay Circuit Compares Successive Binary Numbers

THIS CIRCUIT was designed for use in a punched-tape controlled positioning machine to determine work-table drive direction. The circuit determines which of two successive binary numbers is the larger and then sets up either of two control conditions.

The comparison is based on the fact that as two binary numbers are compared bit by bit from left to right, the number that is larger will be the first to have a 1 unbalanced by a 1 in the same channel of the other number. As an example, compare the binary



Corresponding bits of the two binary numbers are compared in the relay circuit. The larger number is the one with the highest order 1 that is not matched by the other number.

numbers 5 and 6. They would appear like this:

$$0101 = 5$$
$$0110 = 6$$

Channels 4 and 3 are balanced, but in channel 2 the lower number has a 1 that is not balanced by a 1 in the upper number. Thus the lower number must be the larger.

A relay circuit that compares 4-bit numbers is shown. The Comparator section is connected to make the comparison progress from left to right. Two zeros or two ones in the same channel cause the two relays in that channel to be both unenergized or both energized. In either case the common return circuit is closed for the next lower-order channel.

The double relay closures continue toward the right until an unbalanced channel is found, at which point only one of the two relays in that channel is energized and the return circuit is held open, stopping the comparison. The unbalanced energized relay determines which output line will be energized. If it is the "New Number" relay the "Larger" output is closed. If it is the "Old Number" relay the "Smaller" output is closed.

Let us assume that the last number read into the Register was a 6 and that the comparison and control functions have been completed. The 6 is now held in Old Number Storage with relays *K*22 and *K*23 locked up. *K*43 is held energized by *K*23. All other relays are unenergized.

If the next number of the series is a 5, it will cause register relays *K*11 and *K*13 to pick up and lock. *K*13 causes operation of *K*33 which balances channel 3, since *K*43 is already energized, and the return circuit is thus closed to channel 2. The contacts of *K*22 are still closed so *K*42 immediately picks up. However, since *K*12 is not energized *K*32 does not pick up. Thus an unbalance exists with the Old Number relay energized and the return circuit open to channel 1, stopping the comparison.

With the output contacts of *K*42 transferred, the circuit to the "Smaller" output is closed. This is correct because the 5 in the Register is smaller than the 6 in Storage. *K*54 is now pulsed to energize the output function. Immediately thereafter *K*53 is pulsed to clear the Storage section, *K*52 is pulsed to transfer the 5 from Register to Storage and *K*51 is pulsed to clear the Register. This sequence leaves *K*21, *K*23, and *K*43 energized and the circuit is ready to receive the next number and compare it with the one in Storage.

This circuit has been in successful operation comparing six-digit binary numbers in a production machine for more than a year.

Frequency Selective Transistor Switch

THIS CIRCUIT provides a means by which a transistor may be switched from a cutoff condition to a saturated condition by means of narrow preselected band of frequencies. Essentially this is a frequency selective transistor switch.

The circuit consists of a resonant circuit, as shown in Fig. 1, tuned to a predetermined frequency by means of capacitor, *C*, in parallel with inductance *L*. The inductance consists of two inductors in series, L_1 and L_2, and they are not necessarily mutually coupled. The ratio of L_1 to L_2 is about 5.

A detector circuit consisting of a 1N1561 germanium diode, D_1, and a parallel resistor-capacitor combination, R_L and C_L, is connected across the smaller of the tuned circuit inductors, L_2. A dc voltage is developed across the R_L-C_L combination, the magnitude of which is proportional to the input frequency.

The voltage output as a function of frequency is shown in Fig. 2. The voltage output of the detector circuit is fed into a voltage sensitive transistor circuit.

The voltage sensitive transistor switch consists of

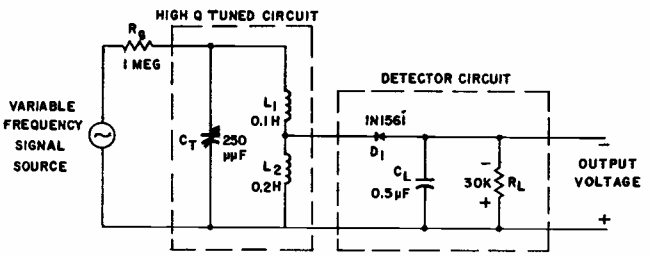


FIG. 1—Resonant circuit and detector for feeding to transistor.

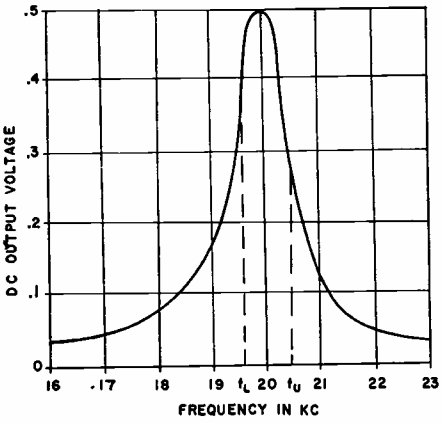


FIG. 2—Output voltage of detector versus frequency.

a common-emitter amplifier circuit held in the cutoff condition by means of a forward-biased diode, D_2, in the emitter circuit, as shown in Fig. 3. This circuit is fed by a regenerative type switching circuit the output of which is always at one of two dc levels, depending on the condition of the input.

When the input signal moves above the predetermined value, the output of the regenerative circuit will switch from one voltage extreme to the other providing enough drive to switch the output transistor from the cutoff to the saturated condition.

Previously it has been difficult to obtain a voltage sensitive transistor switch that would move from the cutoff condition to the saturated condition, or vice-versa, without moving slowly or hesitating in the high power dissipation or linear region, thereby burning out the transistor. This circuit is designed to overcome this and switch rapidly from one condition to the other upon receipt of the proper low level dc signal.

When $E_{IN} = 0$, Q_1 is not conducting and V_{C1} is determined by the voltage divider ratio formed by R_{L1}, R_L and R_2 and V_{CC}. V_{B2} is at some negative potential determined by the same divider network. Transistor Q_2 is turned on. Assuming R_{L1} and R_1 cause Q_2 to saturate, the load current will be determined primarily by R_{L2} and V_{CC}, since $R_E << R_{L2}$. This will cause V_{C2} to be at some small negative potential, say V_{C2L}. V_E is then determined by the maximum collector current of Q_2 and R_E. $V_{Emax} = I_{C2max} R_E$.

If E_{IN} now decreases slightly below the value of V_{Emax}, V_{BE} becomes negative and Q_1 begins to conduct, this causes V_{B2} to become more positive tending to turn Q_2 off. This, in turn, causes I_{C2} to decrease, causing V_E to become more positive which turns Q_1 on still further. The regeneration in the circuit causes this to occur very rapidly with the result that V_{C2} decreases rapidly to a higher negative value, say V_{C2H}. Now, consider the effects of V_{C2L} and V_{C2H} on the common emitter output circuit.

To prevent V_{C2L} from turning on Q_3, a diode is placed in the emitter circuit of Q_3 and biased in the forward direction with a current determined by R_D and V_{CC}. The diode voltage drop V_D, is of such a polarity as to keep Q_3 turned off. Transistor Q_3 will be turned off as long as the following condition is met.

$$\frac{R_4}{R_3+R_4} V_{C2} < V_D$$

This condition is easily met when $V_{C2} = V_{C2L}$.

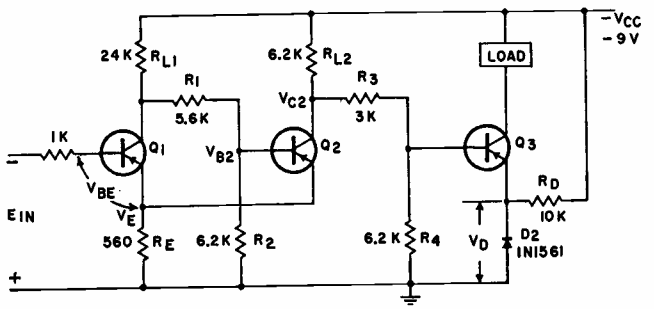


FIG. 3—Basic circuit of transistor switch.

However, the circuit is designed such that when $V_{C2} = V_{C2H}$

$$\frac{R_4}{R_3+R_4} V_{C2H} \gg V_D$$

Q_3 is driven instantly into saturation from the cutoff condition. This completes the operation of the circuit as far as turning on Q_3.

When Q_1 is conducting the voltage, V_E assumes some negative potential less than V_{Emax}, say V_{Emin}. When E_{IN} decreases below the value V_{Emin}, Q_1 turns off and because of the circuit regeneration the circuit returns to the initial condition when $E_{IN} = 0$. This returns Q_3 to the cutoff condition.

When the signal frequency moves above the lower frequency cutoff point, f_L, the output voltage increases in the negative direction causing the voltage sensitive circuit to turn on the transistor switch with a regenerative-type action. As the frequency is increased above the resonant frequency to the upper cutoff frequency point, f_U, the output voltage drops below the value necessary to keep the transistor switch turned on and the transistor switch then turns off with a regenerative-type action.

This circuit is designed to switch rapidly from one condition to the other upon receipt of a signal of frequency within the narrow predetermined range without hesitating in the high power dissipation region of the transistor.

The complete circuit gave excellent performance; turning on and off within 0.5 kc as the frequency was gradually increased through the resonant frequency of 20 kc.

Solid State Latching Relay

USE OF a new type of magnetic firing circuit for silicon controlled rectifiers permits the construction of simple, compact ac solid-state relays of both the latching and non-latching type. The re-

lay is activated by a dc or ac control current in a single electrically isolated control winding and switches load power up to 1.7 kilowatts.

The basic magnetic firing circuit which is used is shown in Fig. 1. Transformer T_1 is made with a small core of square loop material such as Orthonol. If the core of T_1 is unsaturated, winding 1-2 will present a high impedance and the current through R_1 and D_1 will charge C_1 during the initial part of the positive half cycle. Transformer T_1 will saturate after a few degrees of the positive half cycle and permit a rapid discharge of C_1 into the gate of SCR_1 thus causing SCR_1 to fire. If, however, the core of T_1 is initially saturated at the beginning of the positive half cycle, winding 1-2 will present a low impedance thus diverting the current from C_1 and preventing C_1 from being charged. Resistor R_2 is chosen to have a sufficiently low value so that the voltage produced by the current through R_1 will not exceed the minimum gate firing voltage.

Owing to the presence of the diode D_1 the current through winding 1-2 of T_1 will be unidirectional, thus causing the core of T_1 to be normally in the saturated state. Consequently the scr will not be fired, and the circuit will function as a normally open half-wave relay.

A positive signal on the control winding 3-4 of T_1 will cause the core to be reset during the negative half cycle of the ac line so that the scr will be fired on the following positive half cycle.

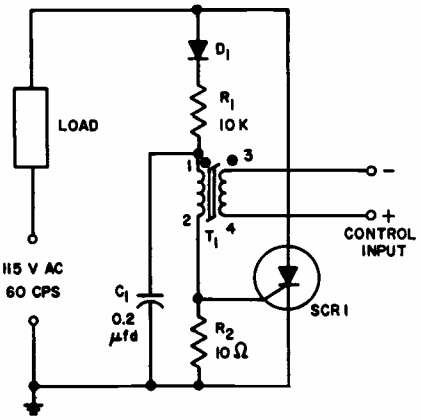
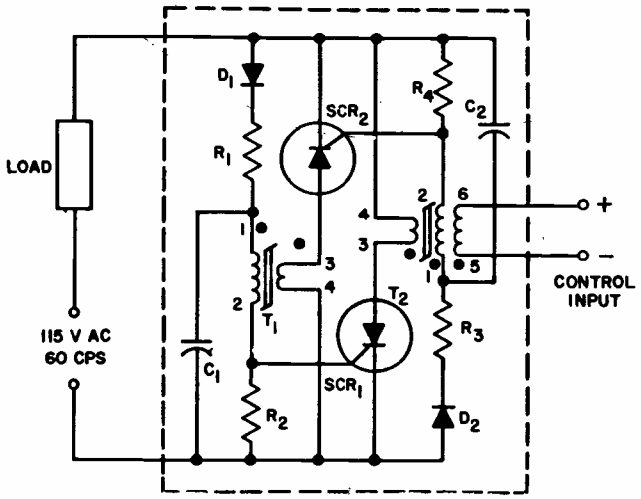


FIG. 1 — Basic magnetic firing circuit.

This firing circuit is unique in that the saturable core is not required to sustain the gate voltage for a full half cycle as is the case in conventional magnetic firing circuits. Consequently the magnetic core can be much smaller and less expensive than those which would ordinarily be required.

Two of the simple half-wave circuits of Fig. 1 can be combined to give a full-wave ac latching relay as shown in Fig. 2. Here the reset signal for the core of T_1 is obtained from a five turn winding in the anode circuit of SCR_2 and the reset signal for the core of T_2 is obtained from an identical winding in the anode circuit of SCR_1. If neither scr is conducting there will be no reset signal furnished to either core and the scr's will remain in the nonconducting state. If the core of T_2 is reset by a momentary positive signal at the control input,



R_1, R_3 10 K, 1 W,
R_2, R_4, 10 ohms ½ W,
C_1, C_2, 0.25 μf,
SCR_1, SCR_2 C10H or C35H
D_1, D_2 1N1695

T_1, T_2 Magnetics Inc. Orthonol #50007-1A
1-2 200 turns #28 AWG
3-4 5 turns #14 AWG
5-6 100 turns #28 AWG

FIG. 2—Solid state ac latching relay.

SCR_2 will fire and its anode current will reset the core of T_1 which in turn will cause SCR_1 to fire. This action will continue with the result that both scr's will remain in the conducting state even after the control signal is removed. To turn off the circuit a negative voltage at the control input will saturate the core of T_2 and thus prevent SCR_2 from firing. The circuit has memory in that when the line voltage is reapplied after an interruption the circuit will remain in the same state (either conducting or nonconducting) as before the interruption occurred.

The circuit of Fig. 2 requires the load current to be above a minimum value (about one ampere for the circuit shown) for conduction to be maintained. Operation at lower values of load current can be obtained by increasing the number of turns on windings 3-4 of T_1 and T_2. In some cases it may be desirable to add a simple series RC line filter across the relay to prevent false triggering due to line transients.

Magnetic Latching Relay Flip-Flop

THERE IS a wide variety of flip-flop circuits available to circuit designers. The flip-flop described here uses a magnetic latching relay as the memory element and has several advantages over the standard relay flip-flop. These advantages include simplicity, reliability and ruggedness suitable for missile application.

The unit has an isolated output through single pole, double throw, relay contacts capable of handling 2 amps, 30v dc or 1 amp, 115v ac. No standby

power is required to maintain state of flip-flop. Up to 100 transfers per second are possible and the unit has a wide signal tolerance of 20 to 30 volts.

The magnetic latching relay flip-flop circuit as shown in Figure 1, uses a Potter & Brumfield, 24V magnetic latching relay and two tantalum capacitors, C_1 polarized, C_2 nonpolarized.

The operation of flip-flop proceeds as follows. A signal of 20 to 30 volts is applied to the input of the device through C_1. This signal may be a pulse of 5 msec or longer. At the instant the voltage appears, current flows into both coils through C_1 and C_2 resulting in a exponential increase in current and then a decay as shown in Fig. 2, (initial phase).

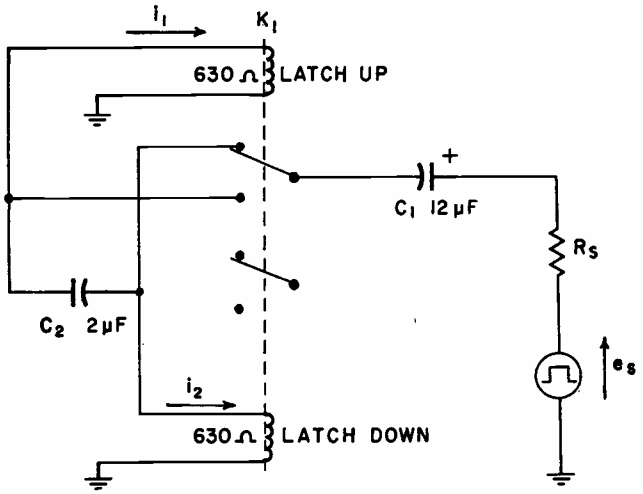


FIG. 1—Magnetic latching relay flip-flop.

After a short time the current in the latch-down coil (i_2) overpowers the effect in the latch-up coil (i_1) and the relay starts to transfer.

At the instant the relay arm leaves contact 1, (transition phase) current stored in the relay coils will discharge through each other by way of C_2. Since the current in the latch-down coil is the larger of the two it will continue to flow in the forward direction while causing the current in the latch-up coil to reverse. The particular relay specified for this application is polarized so that the reverse current in the latch-up coil will also assist in latching the relay down.

When the relay transfers (final phase) current will continue to flow into both coils until C_1 charges. However, C_2 acquired a charge during the initial phase which is opposite to the current flow into the latch-down coil. Therefore, by virtue of C_2 discharging into the latch-down coil, its current will be effectively larger than that in the latch-up coil. This effect is shown in Fig. 2.

It is evident from the circuit diagram that no holding power is required. Another feature of the magnetic latching relay flip-flop is that each phase of the relay operation (initial, transition and final) aids in the relay transfer. Also, a removal of the signal voltage after 5msec will assist in maintaining the transfer. Since C_1 has acquired a significant

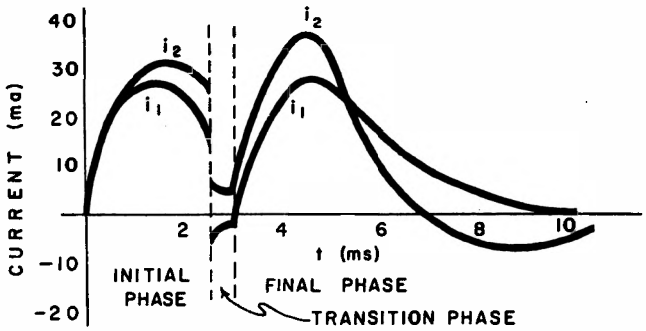


FIG. 2—Current in latching relay coils with 30v input.

charge within 5 msec, it will discharge through the relay in the reverse direction through the signal source impedance thereby aiding the transfer.

The latch-up position and the latch-down position are symmetrical. Therefore, another incoming pulse will transfer the relay to the latch-up position in the same manner as described for the latch-down operation. The tolerance allowable for C_1 and C_2 are ±20 per cent. However, with a tighter control on signal voltage the tolerances can be widened considerably. The components used in Fig. 1 resulted in the following characteristics:

Signal Voltage	*Max Source Current*	*Transfer Time*
20V	40 ma (2.5 msec)	5 msec
30V	60 ma (4.2 msec)	3 msec

Because of its advantages, this flip-flop has found application in satellite vehicles for logic switching of power circuits.

Simple Servo Follow-up System

A NUMBER of positions or channels required in a servo follow-up system can in many cases be broken down in combinations of two components, ($y = x\,z$). The combination of two components which, when added together, yields the smallest sum ($x + z$), forms the basis for a follow-up system with fewer interconnected leads, less volume and inexpensive components.

In Fig. 1 is shown a common zero seeking follow-up system. The physical size of the switch wafers in this system is a function of the number of positions required. The number of interconnecting leads between the remote position or channel selector switch S_1 and the follow-up mechanism equals the number of positions or channels plus 1.

The contact on S_2, (Fig. 1), which represents the position selected with Switch S_1, lines up with an opening on the contact ring when the follow-up procedure has been accomplished. By increasing the number of openings X on the contact ring, the original number of positions can be increased in direct ratio with x. (X = 2 in Fig. 2)

The additional openings on the contact ring have

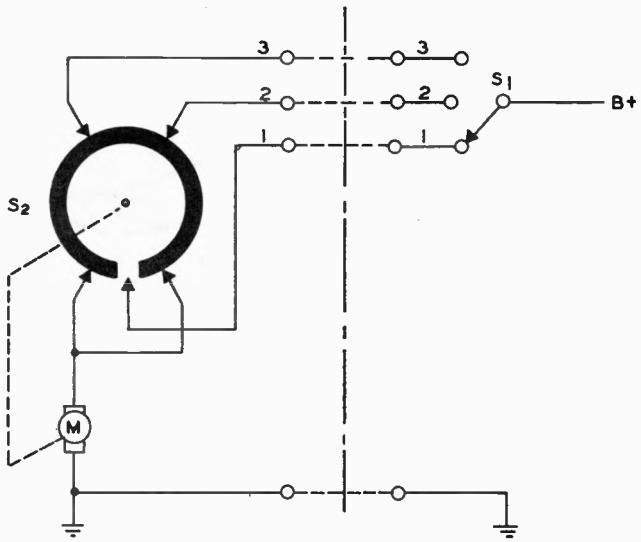


FIG. 1—Zero-seeking follow-up system.

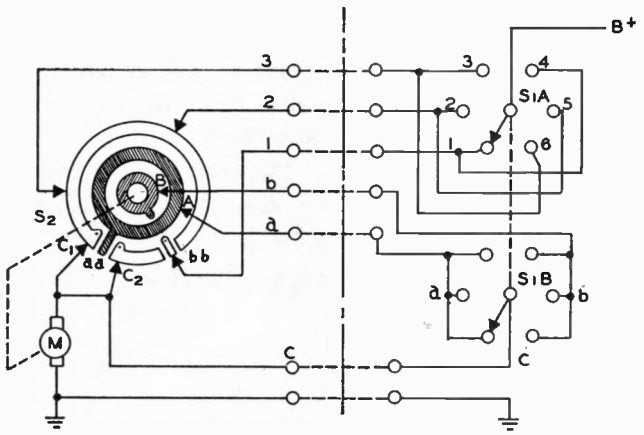


FIG. 2—Contact ring assembly.

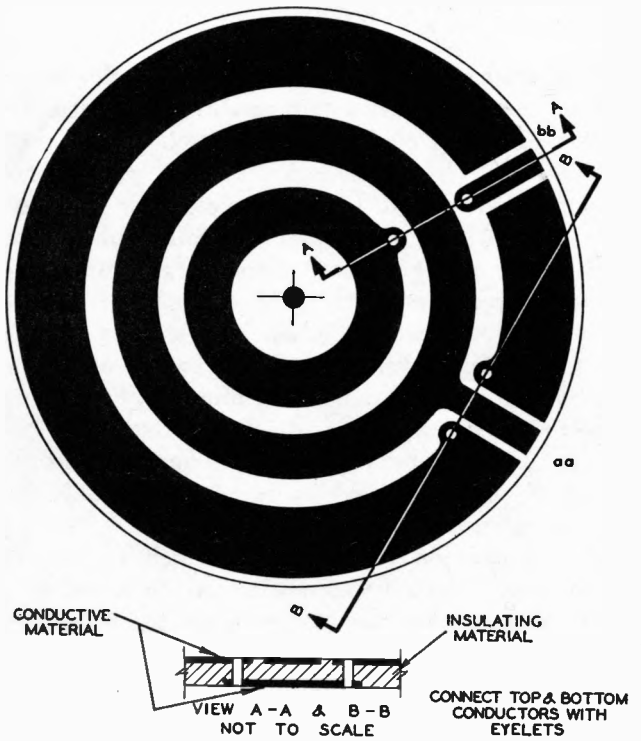


FIG. 3—Top and bottom conductors are connected with eyelets.

been achieved with the aid of a switch as shown in Fig. 3. The outer ring is called the contact ring, the inner rings are called the auxiliary rings. The auxiliary rings make it possible to connect either segment *aa* or *bb*, (See Fig. 3), with the outer ring by means of sliding contacts (A, B, C_1 and C_2) and remote Switch S_{1B}. (See Fig. 2).

By connecting contact *a* with remote switch S_{1B} (Fig. 2), segment *aa* on S_2 is made an integral part of the contact ring of S_2 and *bb* represents the opening. The supply voltage B+ is connected to the wiper arm of remote switch S_{1A} which can select one of Y positions. If switch S_{1A} selects a position which does not face discontinuity on the contact ring, in other words, does not fall on *bb*, current will flow through the contact ring and into the dc motor to ground. The motor is energized and turns switch S_2 until the current through the motor is interrupted because of discontinuity on the contact ring. The contact facing, segment *bb*, correlates the position selected with remote switch S_1.

By connecting contact *b* with remote switch S_{1B} (Fig. 2), segment *bb* is made an integral part of the contact ring of S_2 and *aa* represents the opening. In this case the contact facing segment *aa* correlates the position selected with remote switch S_1.

One advantage of the system is reduction in physical size of the follow-up wafer switch, which can be a printed circuit switch. There is less contact wear on wafers because of decreased number of contacts. A 42-position system with one opening in the contact ring requires 43 contacts, with two openings 25 contacts are required, and with three openings only 19 contacts are necessary.

Integrated Pulses Control DC Output

THE AMPLIFIER shown in Fig. 1 integrates the input pulses, and gives a 28-volt dc output when a specified number of pulses are applied to the

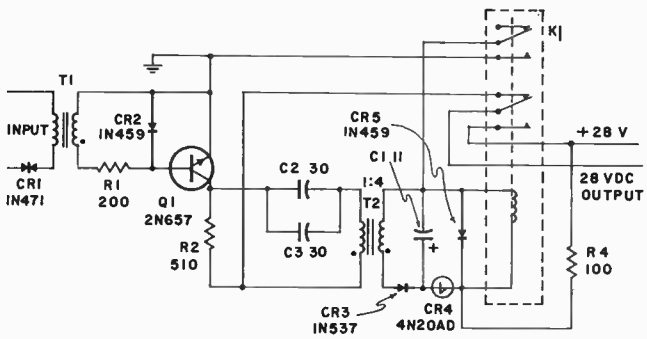


FIG. 1—Circuit of integrating amplifier.

input. Since the 28-volt output is through relay

contacts, relatively high current is available for control purposes.

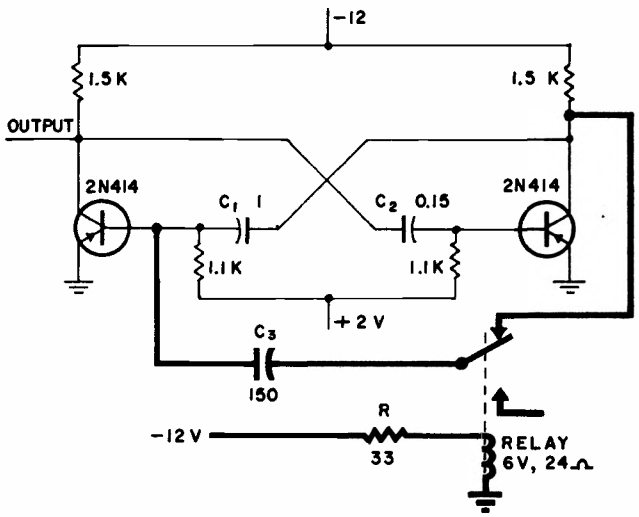
The input signal source is isolated from the amplifier by transformer T_1. Rectifier CR_1 is a double anode Zener diode whose Zener level is below the input signal level, but the Zener level is high enough to prevent inadvertent noise from being amplified by transistor Q_1 and actuating the relay.

Transistor Q_1 is a common emitter amplifier that is coupled to transformer T_2 by capacitors C_2 and C_3. The transformer is a four to one step-up type; its output is rectified by CR_3 and stored by C_1. When the voltage on C_1 reaches the breakover point of the Shockley diode CR_4, C_1 discharges through CR_4 and actuates relay K_1. The relay is latched in the activated position by R_4.

The circuit has a fail-safe feature that is mandatory in some military applications. A failure of any one of the electronic components, excluding the relay contacts, will not cause a premature output signal.

Starter Circuit for Flip-Flop

A FREE-RUNNING flip-flop circuit had several desired features. It uses —12-volt and +2-volt supplies. It has an output impedance of less than 1800 ohms and a period of one millisecond. The



Starter circuit for stalled free-running flip-flop.

circuit is quite stable in operation and we like its characteristics once it is in oscillation. However, the circuit will not commence oscillation of its own accord.

Although many methods might be used to start the multivibrator operation, the novel approach shown in heavy lines was selected. A relay, resistor, and capacitor have been added.

With the power off, 150-μf capacitor is shunting capacitor C_1. The relay will energize at about 9 volts so that C_3 is out of the circuit before normal operation is reached. More significantly, C_3 is in the circuit for the time period during which the power supply increases from zero to 9 volts. This allows C_3 to start the multivibrator operation and then drop out of the picture, much the same as the starter on an automobile functions.

High-Impedance Diode Chopper System

A PROBLEM frequently encountered in semiconductor circuitry is that of chopping a dc signal at a high impedance level. Probably the best known of the conventional methods is the Ring Bridge Modulator[1], using a set of four matched diodes, but although the sensitivity may be of the order of 1 millivolt, the impedance level is seldom above 10,000 ohms, which is too low for many applications.

A 5-megohm impedance level was obtained by the circuit of Fig. 1. It was devised as a method for determing when the voltage across an integrating capacitor reached a predetermined level. The heart of the system is the use of a short sampling pulse and the two diodes D_1 and D_2 to produce a signal whose peak amplitude is equal to the required voltage.

Experiment showed that it was not sufficient (in this case) to ignore the fact that the sampling pulse tended to charge capacitor C_1, and a dc supply was added to neutralize the effect. For design purposes it is convenient to look at an equivalent circuit during the sampling pulse, with R_3 disconnected. In Fig. 2, the pulse height has been transformed to the open-circuit voltage which would appear across R_2 in the absence of any capacitor-charging current and the impedance of the charging resistance R_1 has been transformed into the equivalent resistance of R_1 and R_2 in parallel[2]. (R_1 includes the output impedance of the multivibrator, R_2 includes the ac input resistance of the amplifier and C_2 is ignored in this operation).

The duty cycle of the sampling pulse is t/T (waveform, Fig. 1), typically 0.001. The charging resistor for the neutralizing circuit must therefore be T/t times the value of the equivalent charging resistor of the sampling network, and of course the polarity of the two voltages V_1 and V_2 must be opposite.

Approximate design formulas are given in Fig. 1. If there is a charging resistor or some external circuitry which amounts to a resistance R_4 across the input (in parallel with C_1) then the values of R_3 and V_2 are changed slightly, as below. For improved accuracy, R_3 should also be taken into account as a leakage across the capacitor during the sampling

pulse, and the design formulas can be written more accurately as

$$R_3 = [T - t/t]/[1/R_1 + 1/R_{in} + 1/R_{2A} - t/(T-t)R_4]$$

$$V_2 = -V_1[1 + R_3/R_4]/[1 + R_1(1/R_{in} + 1/R_{2A} + 1/R_3 + 1/R_4)]$$

where R_{in} is the ac input resistance of the amplifier and R_{2A} is the value of resistor wired into the R_2 position in Fig. 1.

The dc impedance of the measuring circuit is

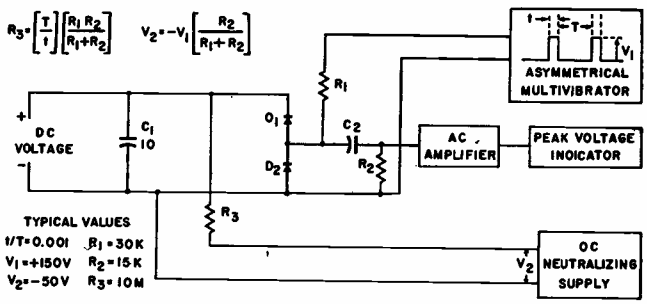


FIG. 1—A dc impedance level of 5 megohms is achieved with values shown. Design formulas shown for R_3 and V_2 can be improved upon, for greater accuracy.

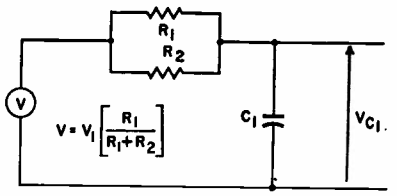


FIG. 2—Equivalent circuit during the sampling pulse.

approximately one half of R_3, or more accurately the parallel combination of R_3, R_4, and the transformed impedance of the sampling pulse. Since R_3 may be 10 meghoms or more, a dc impedance level of 5 megohms is quite easily obtained.

The diodes used for D_1 and D_2 were type 1N300 (Raytheon), with leakage current quoted as 0.001 μa. Minor "tweaking" adjustments were made to the calculated values by setting a charge on C_1 by a battery, and adjusting R_3 and V_2 so that the voltage remained at this level for a minute or so after the battery was removed. The circuit was developed for an integrator [3], but not used in the final design.

Variable-Speed Stepping Switch Control

THE CIRCUIT shown in Fig. 1 was developed to provide a variable speed stepping switch function. Requirements dictated a stepping speed of from 1 to 3 steps per second, and that the switch be able to be stopped at any position, as governed by a selector switch.

Prior approaches using a transistor multivibrator driving a relay to control the stepper switch required 15 parts. The present circuit uses only 7 components, thereby reducing wiring time and space and increasing reliability.

Holding S_1 closed, momentarily, allows C_1 to charge through R_1 and R_2 until sufficient gate voltage is present to turn on the controlled rectifier, energizing the stepper switch coil. The interrupter springs transfer at this time, to discharge C_1 through R_3 and open the anode circuit to allow the controlled rectifier to reset. The coil is thus de-energized, the stepper contacts advance one position, and the interrupter springs return to their original position. Now the OFF NORMAL contacts close and

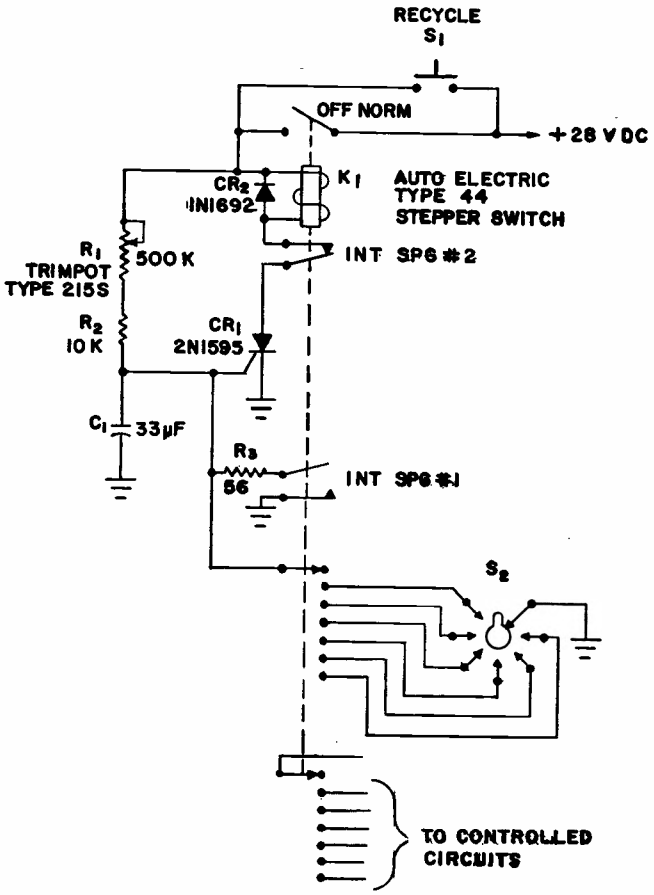


FIG. 1—Stepping switch control requires only seven components.

they remain closed until the stepper arrives back at its home position. The circuit continues stepping with the speed being governed by the setting of R_1, until the home position is reached.

The stepper may be stopped at any position by the action of S_2, which grounds the gate of the controlled rectifier and prevents any buildup of voltage on C_1. CR_2 reduces the inductive spike generated by the stepper switch coil.

All parts are operated within their ratings and no heat sink is required for the controlled rectifier, due to its low duty cycle, hence packaging problems are minimized without sacrificing reliability.

Solid State Variable Time Delay Relay

GROUND support equipment and other missile applications often need a reliable time delay relay capable of handling several watts of power. The circuit described here is a reliable solid state unit which has good repeatability.

The input circuit is designed to accept full-wave rectified dc, such as the output of a magnetic amplifier, or a continuous dc signal. The amplitude need only be large enough to turn Q_1 on (approximately 10 to 100 v dc). With Q_1 conducting the collector of Q_2 goes to + 15 v, the zener voltage of the SV815. This allows C_1 to charge up through R_1 from the + 15 v regulated source. Capacitor C_1 charges up to the peak point voltage of the unijunction transistor, Q_3 and discharges through emitter to B_1 junction and R_9. The rise in voltage at R_9 turns Q_4 on through the coupling capacitor C_3. Transistor Q_5 is turned on through the Schmitt trigger (C_5, R_{16}), and is held on by the positive feedback through R_{17} from collector of Q_5 to base of Q_4. This feedback current is sufficient to hold Q_4 and Q_5 on for output currents in excess of one ampere.

Upon removal of the input signal, Q_1 no longer conducts and Q_2 is turned on by current flow through R_5 and zener diode CR_2. Capacitor C_4 discharges through Q_2, R_8, R_{13} and CR_4 turning Q_4 off. When the input signal is first removed B_2 of Q_3 is lowered to approximately the same potential as B_1. Since the peak point voltage (V_p) of Q_3 is proportional to B_2 voltage, C_1 will discharge through the emitter to B_1 junction. This prepares the R_1, C_1, Q_3 timing circuit for the next input signal.

Due to the method of discharging of C_1 and regulation of base two voltage of Q_3 good repeatability of time delay can be achieved over a wide temperature and supply voltage range without the use of contacts.

The three transistors Q_1, Q_2 and Q_4 used were chosen on the basis of availability and use of a 2N358A or similar high gain, high current switching transistor will improve the reliability. The 2N242 was chosen as the output transistor because it requires very little positive voltage on the base, with respect to the emitter, to turn it off at high temperature. The CR_5 forward voltage drop and R_{11} furnish the necessary bias voltage for cut off.

By changing C_1 to 0.047 μf and removing C_2 from the circuit a lower range of time delays may be utilized, (approximately 100 μsec to 200 msec). The range of time delays for the circuit shown is approximately 100 msec to 16 minutes.

R_1	1K - 10 MEG	C_1 - High Range	100 μf
R_2, R_7 & R_{13}	10K	Low Range	0.047μf
R_3 & R_4	27K	C_2, C_4, C_5	0.1 μf
R_5	2.7K	C_3	0.001 μf
R_6, R_{12}	470	C_6	60 μf
R_8	47	CR_1, CR_4	IN645
R_9, R_{11} & R_{15}	100	CR_2	SV812
R_{10}	56	CR_3	SV815
R_{14}	120K	CR_5	6F20
R_{16}	270	Q_1, Q_2 & Q_4	GT229
R_{17}	5K	Q_3	2N489
R_{18}	1K	Q_5	2N242

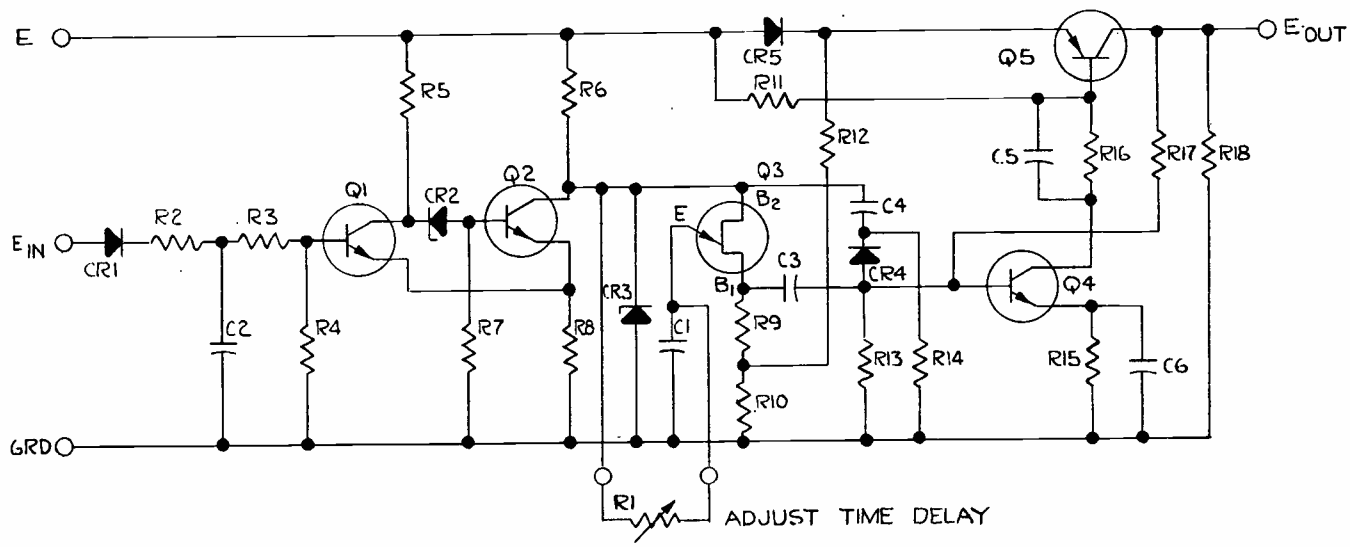


FIG. 1—Circuit of solid state variable time delay relay.

Relay Control Circuit

NEED often arises for a simple relay control amplifier which is stable over the temperature range of —55 to 85C. The usual approach is to design a high-gain transistor amplifier and incorporate plenty of feedback for stability.

An approach found very rewarding is the use of a reset type magnetic amplifier together with a silicon transistor. Figure 1 is a schematic of a temperature controller using this approach. Resistor R_1 is the temperature sensitive element comprising one leg of a balanced bridge, when its resistance changes from nominal a dc voltage appears across points A and B, this is the signal input to transistor Q_1. A change in collector current as a function of input signal alters the reset current through the control winding of the magnetic amplifier T_1. The gate winding of T_1 behaves as a variable impedance between the supply voltage and the load, relay K_1.

Variable resistor R_4 sets the control current to just trip the relay when the voltage between A and B equal zero volts (as determined by the setting of bridge resistance R_3). Resistance R_5 is wound from positive temperature co-efficient wire (Balco) and provides compensation over the temperature range of —55 to +85C. Transformer T_2 provides

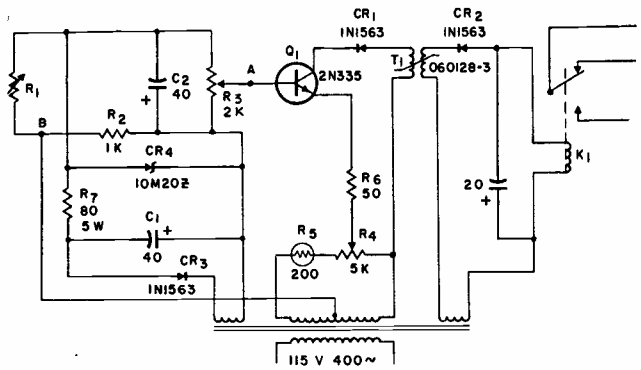


FIG. 1—Relay control amplifier is stable over range from —55 to 85C.

the necessary voltages for operation of the amplifier. This circuit configuration may be used for either ac or dc signal inputs.

Germanium transistors may be utilized by reversing the polarity on diodes CR_1 and CR_2; however changes in I_{co} with temperature represent changes in reset current and it becomes very difficult to compensate over the required range.

The unit shown maintained a temperature setting to 1 degree F over the prescribed ambient range and with line voltage changes of ±10 per cent.

Phototransistor Operated Relay

MANY USES of photocell instrumentation call for a compact unit that can be bolted or clamped in position and be able to operate switching directly from its own relay. It must be compact, self-contained without the use of external amplifiers, and sensitive yet rugged.

Such a circuit is shown in Fig. 1. It uses a silicon controlled rectifier and a phototransistor. Light normally falling on the phototransistor, Q, maintains it conducting so that the gate of the SCR remains at ground potential. When the light beam is broken, the phototransistor is cut off, passing a positive step to the SCR, which fires and operates the relay.

Practically any relay can be used, since the SCR can handle up to 1 ampere, and its fired resistance and volt drop are very low. The circuit is reset by pushbutton or microswitch as shown, or by interrupting the supply to the unit. Capacitor C prevents operation due to spurious noise or light vibration. Diode D and capacitor C prevent re-firing of the SCR due to back-emf coupled to the gate from the relay when resetting.

All the parts, excluding the light source and supply voltage, can be arranged on the relay with hardly any increase in space over the relay itself and, more important, with no extra wiring to the assembly other than is normally required for the relay only. The assembly can then be fixed anywhere by the normal relay mounting screws. Sensi-

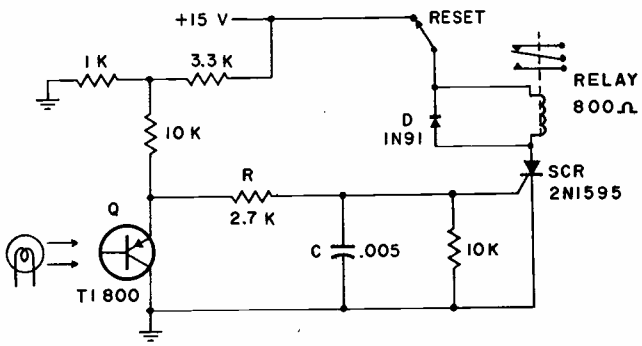


FIG. 1—Phototransistor controls silicon controlled rectifier operated relay.

tivity can be adjusted by varying the value of resistance R.

An interesting adjunct to this circuit is that if a relay can be chosen which has an operating current below that of the holding current of the SCR, no resetting is required although, of course, the light pulse must be long enough to operate the relay. For the normal latching use, however, rise times down to 1 microsecond or less will operate the relay.

Thyratron Actuated Relay Multivibrator

THE CIRCUIT was devised for use as a control element whose on and off times could be conveniently and independently varied over a wide range (from approximately 50 milliseconds to upwards of 5 minutes).

The neon bulbs coupling the timing section to the flip-flop section serve to isolate the charging capacitor from any possible shunting effects thus eliminating the timing error in conventional circuits caused by grid current.

Circuit action is as follows; Assume that when the circuit is first turned on neon #2 conducts. This locks out neon #1 with the result that the thyratron grid is effectively at ground potential. Thus, the thyratron will conduct and energize the relay. The relay contacts keep C_1 discharged and allow C_2 to charge up to the point where neon #4 conducts discharging C_2 through R_2 until neon #4 extinguishes. The extra potential across R_2 caused by this discharge extinguishes neon #2. This allows neon #1 to conduct, locking out #2. A negative potential is thereby applied to the thyratron grid which stops it conducting thus causing the relay to

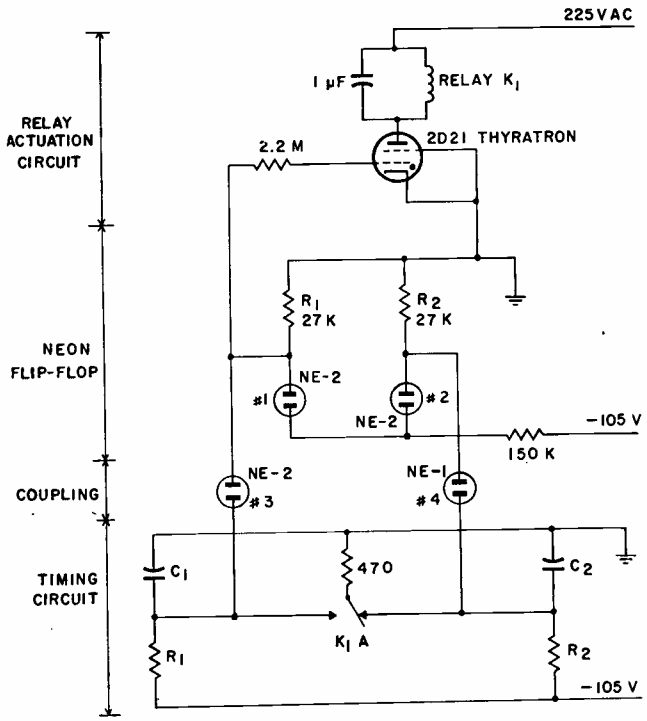


FIG. 1—Thyratron multivibrator off time is controlled by R_1C_1 and on time is controlled by C_2R_2. Values of R_1 and R_2 should be 1 megohm or greater.

fall out. The relay contacts keep C_2 discharged and allows C_1 to charge up to the point where neon #3 conducts discharging C_1 through R_1 until neon #3 extinguishes. The extra potential across R_1 caused by this discharge extinguishes neon #1. Neon #2 will now conduct recommencing the cycle.

Voltage Controlled High Voltage Switch

A VACUUM TUBE with low plate resistance makes a useful switch to control the charging of a line or capacitor used in pulse generation. By turning off the tube at the proper time destruction of a thyratron switch and load can be prevented without sacrificing the pulse rate. To operate the vacuum tube, however, a large d-c voltage swing must be applied to the grid. This can be obtained from the starved operation of another thyratron.

In Fig. 1, capacitor C_1 is to be charged to some value up to 400 volts and subsequently discharged by a gas tube, represented by S_1, into the load R_5. Tube V_2 acts as a cathode follower and charges the capacitor through its plate resistance as long as V_1 does not conduct. When the time arrives for operation of S_1, V_2 is turned off by turning on V_1 for whatever period of time is required for S_1 to operate and recover. Simultaneous conduction of S_1 and V_1 is possible where the discharge time of C_1 exceeds the ionization time of V_1 (the order of a microsecond).

The plate load of V_1, consisting primarily of R_2, will not pass sufficient current to keep V_1 ionized under the conditions imposed in Fig. 1. Therefore its plate swing can be controlled by creating a plasma at the first grid and assisting conduction to the plate. About 0.7 ma at the grid is sufficient to establish the plasma. This current is obtained through R_1 from the input signal.

The negative transition at the plate of V_1 is very fast. (R_3, located close to the plate, limits the peak current produced by stray capacitance.) The positive transition, however, is much slower since stray

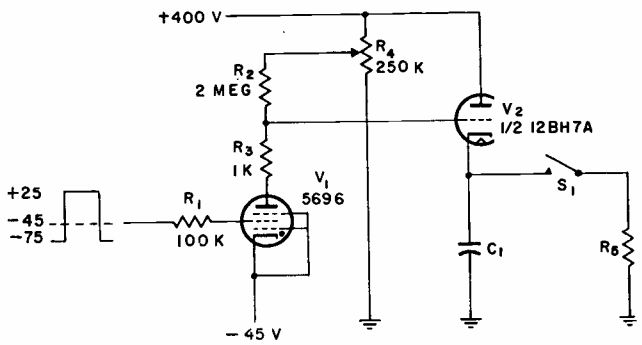


FIG. 1—Circuit of voltage controlled high voltage switch.

capacitance must recharge through R_2. This is not a disadvantage at a 2 kc rate, however, where the circuit has been used. During the time V_1 is conducting, the grid of V_2 is held at about —37 v, which prevents V_2 from conducting regardless of the potential on C_1. R_4 provides a convenient means of varying the charge on C_1.

Separate filament transformers must be provided

for the two tubes with center taps returned to the respective cathodes.

Solid-State DPDT Relay

EIGHT DIODES and four transistors can be connected to act as a double-pole double-throw relay. By continuing the basic pattern, this scheme can render a multi-pole multi-throw relay of any magnitude within the capability of the drive circuit for "coil" terminals X and $\overline{X}$.

The $A + B$ output is clamped to A OR B as a function of $\overline{X}$ and X respectively. The $C + D$ output is clamped to C OR D as a function of $\overline{X}$ and X respectively.

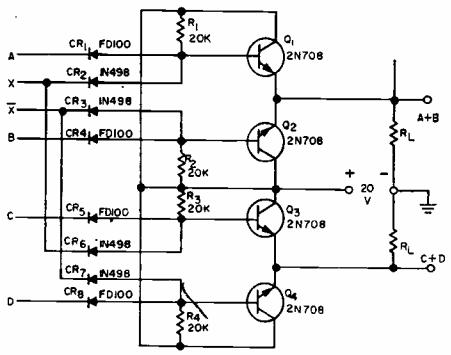
Any output A, B, C, or D will equal, almost exactly, its corresponding input. For example, assume $X = +20$ v; therefore $\overline{X} \cong 0$ v. Then the bases of $Q2$ and $Q4$ will be clamped to 0 v + 0.2 v which is not enough to turn on $Q2$ or $Q4$, since both are silicon junctions. The bases of $Q1$ and $Q3$ would be pulled to +20 v through R_1 and R_3 but are clamped to A and C respectively. Since the emitters will follow the base, −0.7 v, and the base is clamped to A or C, +0.7 v ($CR1$ and $CR5$), the emitters of $Q1$ and $Q2$ will be held = A while $Q3$ and $Q4$ emitters are held = C.

When $\overline{X} = 20$ v and $X \cong 0$ v, the same condition will prevail for $Q2$ and $Q4$ and now Q_1 and $Q3$ will be shut off.

For zero offset, $CR1$, $CR4$, $CR5$ and $CR8$ must be silicon as must $Q1$, $Q2$, $Q3$, and $Q4$. To assure that the off transistors are off, $CR2$, $CR3$, $CR6$, $CR7$ must be germanium. The maximum voltage that can be switched is limited by V_{ebo}. In the case of the 2N708, it is five volts. Output impedance is R_1/β_1 or R_2/β_2 for $A + B$ and R_3/β_3 or R_4/β_4. In the case shown, $R_1 = R_2 = R_3 = R_4 = 20$ K while typical β for the 2N708 is 40, leaving Z_o approximately 500 ohms. Signals in A, B, C or D must be capable of driving 20 K, as must the gates, X, $\overline{X}$ be capable of currents greater than or equal to 1 ma.

The high state of X and $\overline{X}$ must be greater than the largest signal to be switched while the low level must be less than 0.7 v minus 0.2 v or less than 0.5 v.

The 0.7 v being the turn on for the silicon transistors and the 0.2 v being the increase in base clamping voltage across $CR2$, $CR3$, $CR6$ or $CR7$, the germanium clamping diodes. This circuit operates independent of temperature from −20°C to +65°C and E_{in}, (A, B, C or D) from 0.1 v to 4.5 v.



Solid-state dpdt relay.

Relay Lock-Release Circuit

THE CIRCUIT of Fig. 1 was devised for use where a number of relays are wired into a register controlled by pushbuttons.

The circuit action is such that only one relay can be locked in and holding at any time. When a relay is selected by its corresponding pushbutton, any relay previously locked in will be released. Even if several buttons are depressed and released simultaneously only one relay will remain locked in.

Referring to the diagram, the diodes shown typically by A enable the lower set of form C contacts (double throw) to be used in the unenergized position as part of the "one and one only" (i.e., a ground at point X when only one relay is energized)

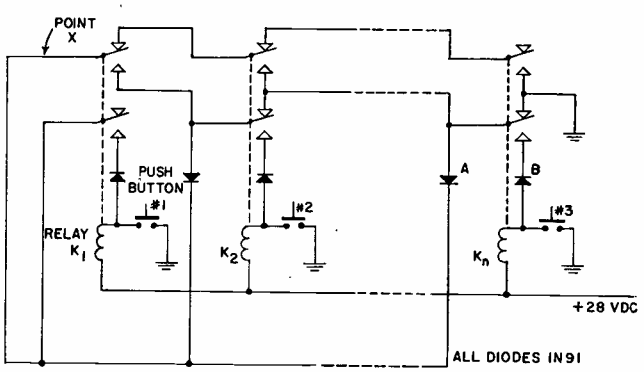


FIG. 1—Diodes permit clearing other relays when one pushbutton is pressed.

and in the energized position as the locking contact for the relay. The diodes shown typically by B prevent the ground supplied by a pushbutton from feeding into the locking circuits.

The circuit was developed for applications where only two sets of form C contacts are available. If a third set is available it can be used for a separate locking circuit thereby eliminating the need for the A diodes (actual contacts required where nonstandard configurations are available are 1A1B1C).

Relay or Switch Driven Pulse Generator

THE FOLLOWING CIRCUIT was designed to generate a voltage step function resulting from the transfer of a switch or relay contact. The width of the pulse is determined by the transfer time of the contacts and is usually two to four milliseconds. The amplitude of the pulse for this circuit is from a —3.5 volt level to +1 volt for repetition rates up to about 10 cps. Due to capacitance filtering, the signal

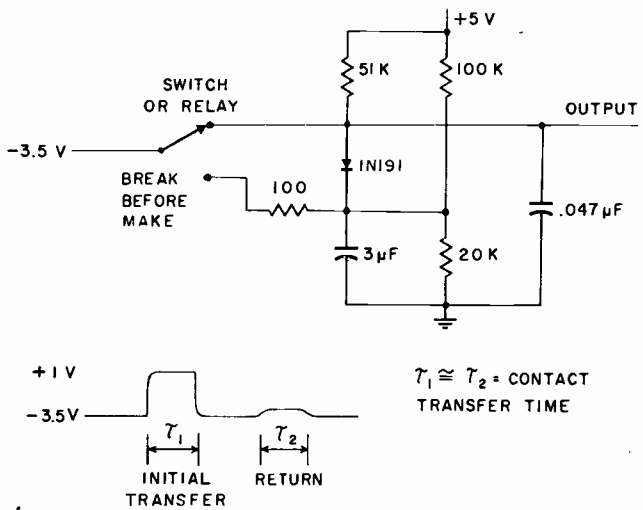


FIG. 1—Pulse generator is driven by switch transient.

is virtually free of contact bounce.

The diode and the 3 μf capacitor are used to clamp the initial pulse from —3.5 volts to +1.0 volt maximum. On the return swing of the contact the capacitor is charged to —3.5 volts and holds the output pulse to about a half volt pulse that gets up to about —3.0 volts. The 0.047 μf capacitor is used to reduce the effects of contact bounce.

Output impedance is determined by forward characteristics of the diode and 100-ohm resistor.

AC Operation of a DC Relay

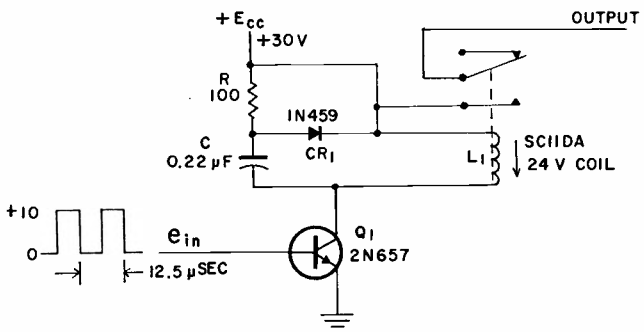
A DC RELAY can be controlled by an ac input signal in a manner such that the relay is energized when the input signal is present and is de-energized when the input is removed. The circuit is shown in the diagram.

The coil of the dc relay L_1 is energized by transistor Q_1, which is used as a common-emitter class-C amplifier to obtain maximum power gain; hence, the input must have sufficient swing to saturate Q_1 as well as cut it off. If the input does not have sufficient swing, it must be amplified. During the "on" portion of the input cycle, current flows through the relay coil, and C is charged through R. During the "off" portion of the input cycle, C maintains the current flow through the coil by discharging through the diode.

Capacitor C performs two functions. It maintains the current through the relay and by so doing, eliminates the inductive kick. The value of C is primarily a function of input frequency and coil resistance, and the discharge time constant is:

$$\tau_d = R_{coil} C$$

τ_d must be large with respect to the input period



Basic relay drive configuration.

$(10 \times T_{in})$. The value of C can then be calculated, because R_{coil} and T_{in} are known.

The value of R, the resistor charging C, is made as small as possible without exceeding the power ratings of the transistor. This value should not be lower than 100 ohms when used with a 2N657 transistor. A low impedance source ($R_g < 2K$) is used to drive the 2N657 transistor.

Stepping Switch Synchronizer

SEVERE noise generated on a segment of a stepper switch, caused by the wiping arm, makes it exceedingly difficult to utilize such a signal to trigger high-speed circuits which may be feeding information to the stepper for distribution. The circuit shown provides a satisfactory remedy for this problem.

A spare bank of the stepper is used. Alternate segments are tied together. Each set of segments is connected to one side of a set-reset flip-flop. The flip-flop senses the very first time the wiper makes contact with a segment, and thereafter is immune to all noise on that segment.

The flip-flop reverses state when the wiper arrives at the next segment. Therefore, a flip-flop transition occurs each time the wiper arrives at a new segment.

The two outputs of the flip-flop are differentiated and added, such that a pulse appears at the output point for each step of the switch.

Obviously, a non-bridging bank of the stepper must be used.

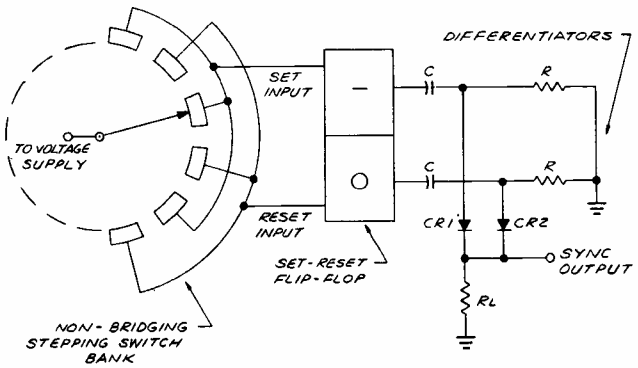
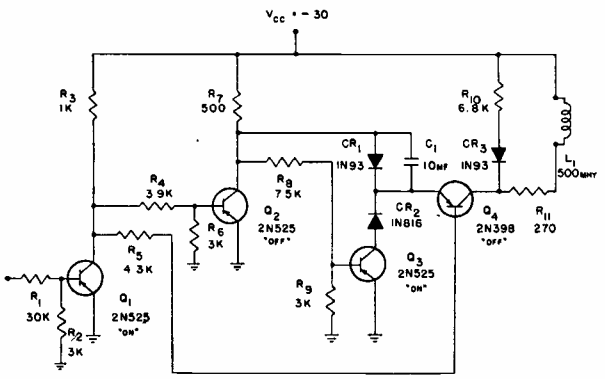


FIG. 1—Synchronizer eliminates noise problems in high-speed switching.

Low Voltage, Fast Current Rise Inductive Load Driver

THIS CIRCUIT may be used to advantage when switching an inductive load requiring faster current rise and fall than could be obtained with low voltage using more conventional circuitry, a problem in transistorized equipments with their inherently low supply voltages.

The problem solved by the circuit shown was obtaining a current waveform with improved rise and fall through a relatively large inductive load from equipment whose collector supply voltage was −30 volts. This was accomplished by charging a capacitor to the supply voltage potential during the interval when no current was supplied to the load, and then placing the charged capacitor in series aiding with the supply voltage when the load was switched on. At the current rise transition this doubled the applied voltage, and for a quarter cycle the circuit exhibited an oscillatory response, at which time the current was stabilized at its steady state value. This approach improved the current rise time over that of the simple transient case with an L/R time constant.



Voltage doubling technique provides fast current rise to drive inductive load.

The circuit as shown is for the condition when no current flows in the inductive load L_1. Since Q_2 is cut-off and Q_3 is in saturation, C_1 is charged to V_{CC} through R_7. When Q_1 is switched to the off condition, Q_2 is turned on, Q_3 is now off, and Q_4 is on. This action connects the voltage on C_1 in series aiding with the supply voltage, V_{CC}, through Q_2, Q_4, and R_{11}, thus at the transition placing $2V_{CC}$ across the inductive load.

Since CR_1 is reverse biased by the capacitor voltage, momentarily the circuit is a series RLC network which produces a damped sine wave current response. The current rises to a peak value at the quarter cycle point at which time C_1 has discharged and diode CR_1 is forward biased. CR_1 now conducts the load current until such time as the circuit is switched to the no current condition, the steady state current being limited by R_{11} in series with the resistance of the inductor. R_{10} and CR_3 are used to reduce the fall time of the load current without a high transient voltage appearing at the collector of Q_4.

The circuit has the reliability feature that should capacitor C_1 open, the circuit will continue to function with a current rise time that would normally be obtained in a conventional RL circuit using the available supply voltage. The same would also be true should either or both CR_1 and C_1 fail as a short circuit. The current fall time would of course remain unchanged.

When driving a solenoid whose inductance was 500 mhy, without the corrective network in the circuit the measured current rise time for a 60-ma load using a 30-volt supply was 9 msec. With the circuit as shown the current rise time was reduced to 1.6 msec, an improvement of 5.6 times. The current fall time was 400 μsec.

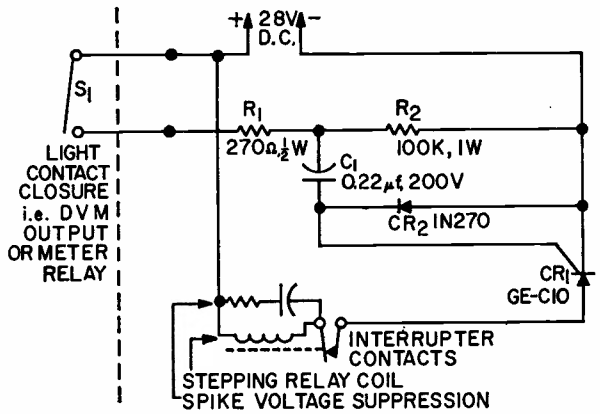
The concept is not restricted to the range of values shown, but may be applied to numerous problems involving switching inductive loads requiring better current transient response than could be obtained conventionally using available supply voltages.

One-Step Function on Switch Closure

THIS CIRCUIT was designed to cause a stepping relay to step once on closure of digital-voltmeter contact. The stepping relay is the type that steps when the coil current (over 1 amp) is removed. Such contacts pass very little current; they remain closed till the input voltage is changed.

In operation, the scr does not conduct when S_1 is open. When S_1 closes, capacitor C_1 charges and causes the scr gate to go sufficiently positive to fire the scr. It conducts and actuates the stepping relay which is then open-circuited by its own interrupter contacts.

The scr will not fire again till S_1 has opened and closed again. When S_1 opens, C_1, discharges through



Circuit converts a switch closure to a one-shot step for a stepping relay.

CR_2 and R_2. CR_2 clamps the negative voltage at the gate of the scr during discharge.

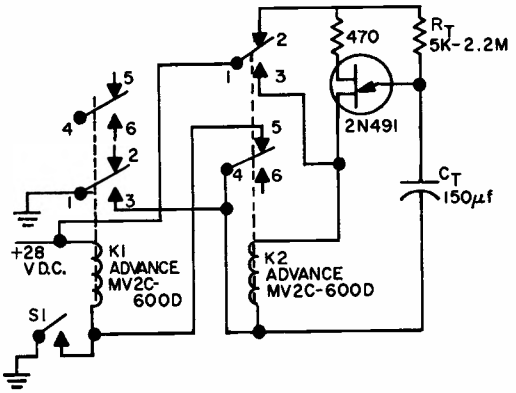
UJT-Relay Circuit Gives Delayed Release

THIS CIRCUIT was developed to give an output for a fixed time interval of up to five minutes after receiving an instantaneous input. An additional requirement was to provide instant reset with a full repeat of the fixed time interval if the circuit was retriggered immediately after a cycle ended. No damage was to be caused if the input trigger was applied continuously.

Operation of the circuit is initiated by closing S1 momentarily and then releasing it. Trigger duration needs to be only long enough to pull in K1 (approximately 7 msec).

A ground is applied to the unijunction transistor timing circuit through contacts 1 and 3 of K1. K1 is held in after the trigger is past by a ground through K2 contacts 4 and 5. The timing circuit receives positive voltage through contacts 1 and 2 of K2. During a time determined by R_TC_T, C_T charges to the peak-point voltage of the unijunction causing emitter current to flow and pull in K2. With sufficient emitter current to pull in K2 the emitter-to-base 1 resistance of the unijunction will be quite low and discharge C_T sufficiently to give a full delay on the next cycle. K2 has its own holding contacts to maintain it closed long enough for K1 to drop out.

When K2 pulls in, contacts 4 and 5 break the self holding circuit for K1, allowing it to drop out. When K1 drops out, K1 contacts 1 and 3 break the ground to K2 and the circuit returns to its original state. The timing circuit is de-energized when K2 pulls in so that no recharge of the timing capacitor can take place until another trigger arrives. If S1 is held closed, K1 is held in permanently as will be K2 after the delay time; thus, an extended time period is available if desired. The delayed release output is a ground at K1 contact 3 and separate contacts 4, 5, and 6 of K1. K2 contacts close momentarily for each timed cycle and can be used for counting elapsed cycles.



The time interval is determined by the R_T-C_T charging circuit, which fires the unijunction transistor.

By adjusting R_T only, time periods of less than one second to over 5 minutes can be obtained with the nominal 150 μf capacitor. Due to the inherent characteristics of the unijunction, timed periods are quite stable with variations in both supply voltage and temperature.

The energizing device (S1) used in the author's application is a frequency sensitive device. Several of the circuits are used with various tone frequencies to give timed remote operation of test equipment.

Transistor Driven AC Relay

THIS DESIGN drives a 12 v ac relay with transistors which were triggered by a low dc current pair of switch contacts. The relay characteristics had a pull in voltage = 9.8 V_{rms}; dc resistance = 8.0 ohms; and a current at pull in voltage = 1.2 amps. A circuit which accomplishes this function with two pnp germanium transistors, 1 npn germanium bilateral transistor, and two diodes is shown in Fig. 1.

When the switch is closed and point A is positive with respect to point B, Q_1 conducts and drives the base of Q_2. In this case the top emitter of Q_1 acts as a collector of this npn transistor. Base current for Q_2 flows through the 75 ohm transistor, Q_1, the other 75 ohm resistor, and the 30 ohm resistor to the other side of the ac line. Relay current flows through Q_1, the relay coil, and the lower diode. When the polarity reverses, Q_1 supplies base current for Q_3 and the lower emitter of Q_1 now acts as an npn collector. Relay current then flows through Q_3, the relay coil, and the upper diode. The switch driving the base of Q_1 can be any mechanical or electrical switch as long as its drop is not a significant portion of the supply voltage. It should, however, be on or off.

The circuit of Fig. 1 can be used to drive any ac relay rated in voltage up to the breakdown of the transistors. Ordinarily the breakdown on the bilateral transistor will be the limiting voltage. For higher voltages, the circuit of Fig. 2 can be applied. This circuit requires an addtional transistor but will work as well

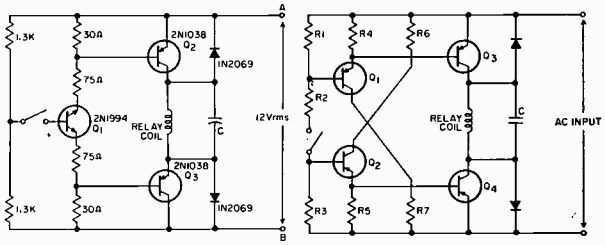


Fig. 1. Circuit drives a 12v ac relay. (left)
Fig. 2. Circuit drives any voltage ac relay. (right)

as the bilateral circuit of Fig. 1. If extra gain is not needed, Q_1, Q_2, R_4, R_5, R_6 and R_7 can be eliminated and the points connecting to bases of Q_1 and Q_2 can go directly to the bases of Q_3 and Q_4 respectively.

In Fig. 2, $R_1 = R_3$, $R_4 = R_5$, $R_6 = R_7$. Resistors R_4 and R_5 are used primarily for stability for Q_3 and Q_4. Resistors R_1 and R_3 are used for the same purpose for Q_1 and Q_2, but in addition, base current for these transistors also flows through R_1 and R_3.

$$\text{Therefore, } R_1 + R_2 = \frac{\text{applied volts (rms)}}{I_{C1}}(h_{fe})$$

$$\text{where } h_{fe} = \text{dc current gain, and } I_{C1} = I_{B3} = \frac{I \text{ (relay)}}{h_{fe3}}$$

When the collector current of Q_1 and Q_2 is known, the size of their collector resistances, R_6 and R_7 can be calculated. In both circuits the value of C should be selected for the particular relay to produce good switching of the transistor and reduce unnecessary dissipation. Also note that one transistor is saturated when the switch is closed and the other has a forward biased diode across it. This provides inherently good protection for the transistors when the relay is energized; only when turned off do the transistors see one-half of the peak sine wave voltage.

Simple, Drift-Free

Voltage Comparator

THIS CIRCUIT indicates whether an input voltage V_1 is positive or negative with respect to a reference voltage V_2. Both voltages vary independently over a wide range (50-150 volts) and then stop for comparison. When the comparison is made, the two voltages might be a hundred volts or only a few millivolts apart. Since, in the intended application, the circuit must perform for many months without adjustment, difference amplifiers must be ruled out because of drift problems in extreme temperatures.

The final circuit (Fig. 1) uses only two relays, three resistors, and a capacitor. K_1 is a fast-make, fast-release mercury-contact type. K_2 is a fast-make, slow-release mercury-contact type. R_1 and R_2 are chosen to make the source impedances of V_1 and V_2 appear equal at the comparator input and to prevent the two sources from being excessively loaded by the comparator.

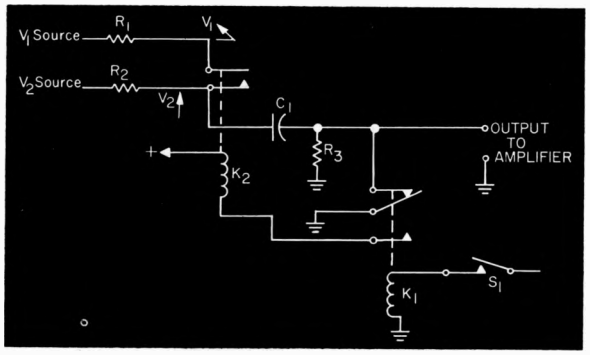


Fig. 1. Voltage comparator circuit.

The output is normally grounded through the contacts of K_1 to prevent the appearance of variations in V_2 at the output. When S_1 is closed, K_1 operates, ungrounding the output (time t_0) (Fig. 2), and energizing K_2 (t_1). The contacts of K_2 connect V_1 to V_2, which produces a positive step at the input to C_1. If V_1 is negative with respect to V_2, a negative step is produced at the input to C_1. The amplitude of the step is $V_1 - V_2/2$. The step is differentiated, producing an output pulse whose polarity is the same as that of V_1 with respect to V_2. This pulse is then easily amplified, and its amplitude may be used to determine the actual difference between V_1 and V_2, although that was not needed in the present application.

The only requirement on the differentiating circuit is that it be fully discharged (t_2) before K_1 releases (t_3) or else a spurious step will be produced at the output

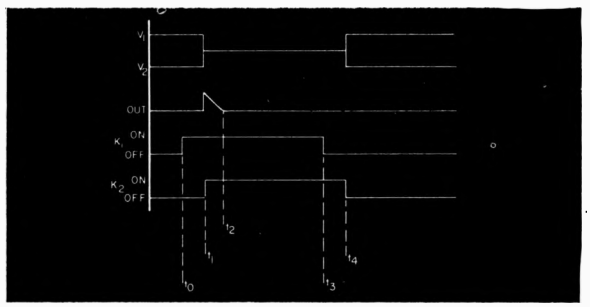


Fig. 2. Timing diagram.

when the output is grounded. When K_1 releases (t_3), the output is grounded before slow-release K_2 can let go (t_4). Therefore, only one pulse appears at the output. This pulse has the fast rise-time needed to trigger following circuits.

High-Power

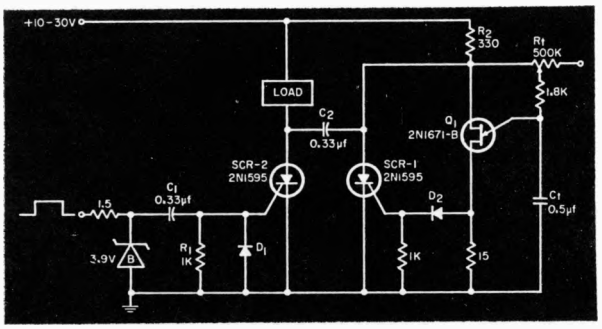
One-Shot Multi

THIS CIRCUIT, operating from an input of a random amplitude (10-28 v) square wave with 1 to 6.5 sec random duration, switches a 20-watt load for an adjustable period

of 5 to 200 msec.

When the supply voltage is applied to the circuit shown, SCR_1 will be turned on by an output pulse from Q_1 after a preset time, determined by R_tC_t. The voltage across Q_1 and its associated timing circuit (R_tC_t) will drop to 0.75v, which is the "on" voltage until an input pulse is applied.

A pulse applied to the input will be amplitude-limited by the zener diode and differentiated by C_1R_1 and will turn on SCR_2. This turns off SCR_1 by the action of the commutating capacitor C_2. When SCR_1 has been turned off, C_t will begin to charge through R_t until the peak-point emitter voltage of Q_1 is reached, at which time an



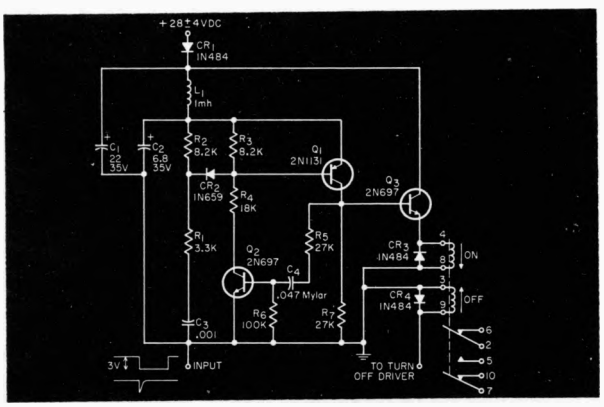
High-power ac static switch.

output pulse from Q_1 will turn on SCR_1. SCR_2 will then be turned off by the action of the commutating capacitor and power will be removed from the load.

The circuit may easily be adapted for transient detection, pulse-width adjustment and time delays by modifying R_tC_t and the input circuitry.

Latching-Relay Driver Requires No Standby Power

A LATCHING RELAY, by itself, consumes no standby power—so, ideally, neither should its control circuitry. Figure 1 illustrates a 24-volt latching-relay driver circuit that requires no standby power. When triggered by a negative-going change (or pulse) of 3 volts or greater, the circuit will provide a 5-msec driving voltage to the latching-relay coil.



Latching-relay driver requires no standby power.

The circuit can easily be modified to trigger from positive-going sources and to operate with 12- or 6-volt latching relays. The time constant of the circuit can be increased by increasing C_4 and R_5, but most latching relays will operate reliably on as little as a 3 msec duration driving voltage.

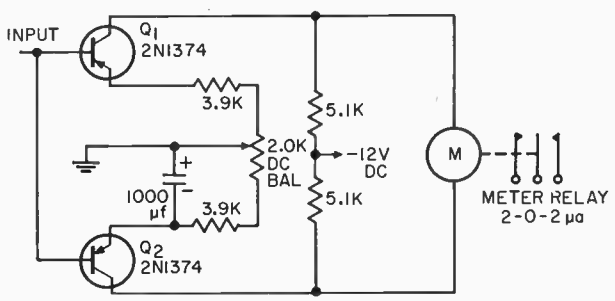
Clamping diodes CR_3 and CR_4 are essential to prevent back emf's in the energized relay coil from false-triggering the off circuit. CR_1 and C_1 are not essential if the supply voltage is not subjected to large current surges but with C_1 and CR_1 in the circuit, the supply voltage may even drop to zero during the driving cycle of one driver without interfering with its duty cycle or false triggering the off circuit.

Rate Circuit

THIS CIRCUIT was developed to satisfy a need for a sensitive and stable dc amplifier which would operate a relay only on fairly rapid changes in input voltage, yet be immune to drift.

The emitter of Q_1 follows a change in input voltage (negative-going or positive-going), while the emitter of Q_2 remains at the voltage across the 1000 µf capacitor. A state of unbalance results during the time required for the capacitor to charge or discharge to the new voltage level, causing the meter relay to operate. The circuit returns to a balanced state as the capacitor charge stabilizes, de-energizing the meter relay. The charge on the capacitor varies along with a slowly changing base voltage, such as that produced by drift in circuit values, with no unbalance sufficient to operate the relay. This rate of change, required to operate the relay, is inversely proportional to capacitor size.

In the original application, stable and reliable operation was obtained with base voltage ranging from −.5 to −3.0 v. Since an ac signal may be considered as a rapidly changing dc signal, it also operates the relay, thus producing a relay operation for a very small ac input.



Rate circuit triggers relay on rapid input voltage changes.

Fast-Rise Current Switch

THIS CIRCUIT demonstrates the use of the law of conservation of electrokinetic momentum (i.e., constant flux linkages) in driving highly inductive loads which require fast-

rise currents. Using this principle, the current is not limited to the slow L/R risetime constant. Instead, the current will rise as fast as it can be switched into the load.

The law of conservation of electrokinetic momentum states that the product $(L \cdot i)$ of an electromagnetic system cannot change except as the system is operated on by an external voltage; in which case the change of $(L \cdot i)$ is equal to the product $(v \cdot t)$ of time and voltage.

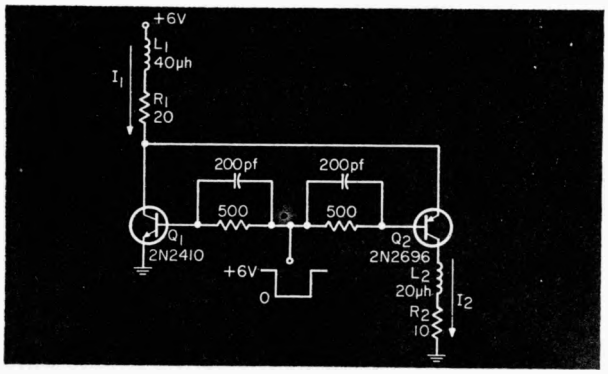


Fig. 1. Fast-rise current switching circuit.

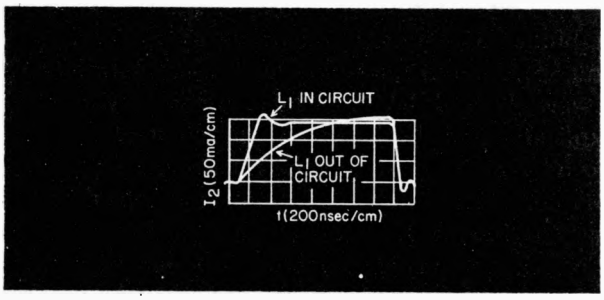


Fig. 2. Load current traces.

The law and its refinement are reduced to practice in the circuit of Fig. 1.

The circuit is in its stand-by condition with Q_1 on and Q_2 off. The standby current I_1 is flowing through L_1, R_1 and Q_1. When a negative input pulse is applied at t_0, Q_1 turns off, and Q_2 turns on. A current i_2 now flows through L_1, R_1, Q_2, L_2 and R_2. At this time $(t > t_0)$, the equation for $i_2(t)$ is:

$$i_2(t) = \frac{V}{R_T}\left[1 - e^{-\frac{R_T}{L_T}t}\right] + \frac{L_1}{L_T} I_1 e^{-\frac{R_T}{L_T}t}$$

where $R_T = R_1 + R_2$

$L_T = L_1 + L_2$

It can be seen that at t_0+, the current (i_2) immediately jumps to:

$$I_2(t_0+) = \left(\frac{L_1}{L_1 + L_2}\right) I_1$$

where I_1 = steady state standby current $= +V/R_1$.

Three conditions are available at t_0+:

(a) $I_{2_{0+}} > I_{2_\infty}$,

where I_{2_∞} is the steady state value of i_2 as t approaches infinity

$$I_2 = V/R_1 tR_2$$

(b) $I_{2_{0+}} > I_{2_\infty}$

(c) $I_{2_{0+}} = I_{2_\infty}$

Condition (c) is the refinement of the law. If this condition is fulfilled, the load current (i_2) will rise as fast as the transistors can switch, and it immediately assumes its steady state value without any L/R transient. This condition can be fulfilled if:

$$L_1 = L_2 (R_1/R_2)$$

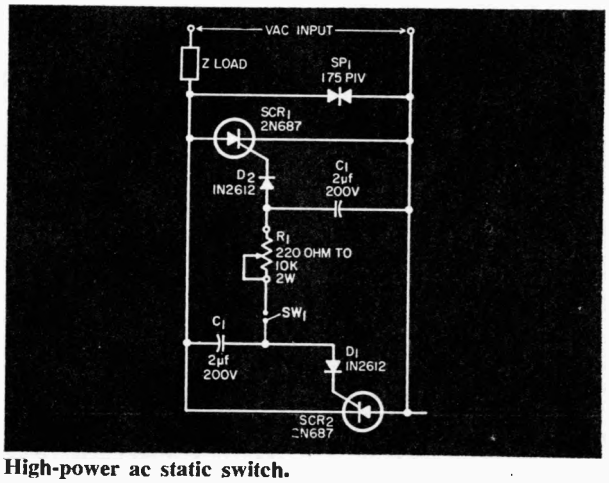
This analysis neglects the voltage drops across the "on" transistor. The only limitation to the circuit is the high voltage which appears across Q_1 when Q_1 goes off. This is a function of the switching time of the transistors. In order to protect Q_1, it must be turned "off" so that the maximum collector voltage of Q_1 is not exceeded. Therefore,

$$L_2 di_2/dt < V_{CBX_{Q1}}$$

Figure 2 shows oscilloscope traces of the actual load currents in the circuit. When L_1 is out of the circuit, the time constant $= L_2/R_1 + R_2$, and risetime $= 840$ nsec. With L_1 in the circuit, the law of constant flux linkages now applies; current risetime improves remarkably (time constant is effectively 0; rise time $= 100$ nsec).

This circuit is applicable as a current driver for digital computer memory arrays, or it may be used for driving relay coils for faster operation.

High Power AC Static Switch



High-power ac static switch.

MECHANICAL SWITCH or relay contacts, which might be burned when switching power to an inductive load, are used in this circuit to control an SCR static switch. The contacts, SW_1, might also be remotely controlled. The output power can be varied with the R_1C_1 time constant, controlling the SCR firing angle.

Diodes D_1 and D_2 provide reverse-bias protection for the SCR gate, while SP_1 provides limiting effects to transient voltages of either polarity. The break-over voltage of SP_1 is chosen as about 30-percent less than the SCR maximum.

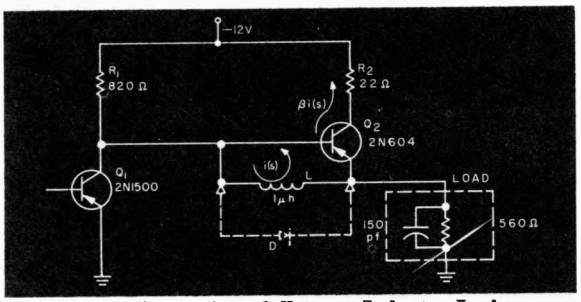
The circuit has been used to switch the primary of a high wattage and inductance transformer operating a 4200 vac secondary.

Forced-Switching Emitter Follower

IF AN EMITTER FOLLOWER is bypassed with an inductor, switching time can be decreased as the load current in-

creases. When Q_1 is turned off, a sudden change if steady-stage current induces a voltage $v(s)$ across L, and the load current removed through R_2 is approximately $\beta v(s)/Ls = \beta i(s)$. Thus the transient drive of the emitter follower increases corresponding to the steady-state load current. This is a desirable characteristic for switching circuit design.

With a 1-μh inductor, the circuit had a fall time of 38 nsec. Without the inductor, the fall time was 70 nsec.



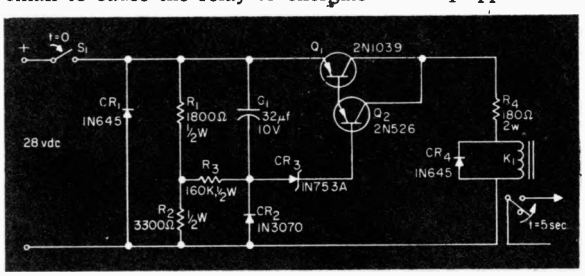
Forced-switching emitter follower. Indnctor L_1 increases the drive for the emitter follower.

Diode D improves rise time without affecting the fall time.

Fast Recycling Time-Delay Relay

THE RATE at which this circuit can be recycled exceeds the recycle rating of most time delay relays. The circuit uses a conventional 28-volt relay to give a 5 sec, ± 1 sec, delay with a recycle time of 200 msec.

The timing circuit basically consists of R_3 and C_1. A considerable reduction in size is gained by reducing the maximum working voltage across C_1 to only 10 volts with voltage divider R_1 and R_2. Transistor Q_1 operates as a switch controlling the current through relay K_1. Q_2 controls Q_1 by amplifying the current through zener diode CR_3, which in turn is determined by the voltage across capacitor C_1. The current through CR_3 is too small to cause the relay to energize until C_1 approaches



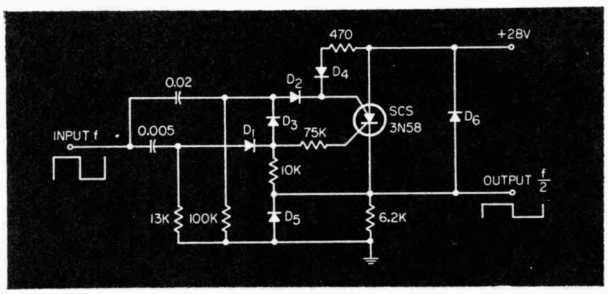
Fast recycling time-delay relay. Time constant R_3C_1 determines timing.

the zener voltage. When S_1 is released, C_1 discharges rapidly through diode CR_2, to make ready for the next cycle. Diodes CR_1 and CR_4 are surge suppressors. Resistor R_4 is selected to limit the relay current to the proper value.

Single-SCS Flip-Flop

THIS CIRCUIT uses only one silicon controlled switch, a 3N58, to perform a flip-flop function over a wide temperature range.

In the circuit, differentiated positive pulses are applied to the cathode gate and anode gate alternately to turn the SCS on and off. When the SCS is off, the steering diode D_3 and rectifying diode D_2 are reverse-biased so that the pulse is applied only to the cathode gate to turn the SCS on. When the SCS is turned on, D_1 is reverse-biased while the reverse bias on D_2 is removed by D_3 and therefore the pulse is applied to anode gate to turn the SCS off.



Single-SCS flip-flop.

The diode D_4 is inserted so that the 470-ohm resistor does not load the positive pulse applied to the anode gate. The diode D_6 is placed so that the turn-off pulse will not appear at output. Diode D_5 prevents the differentiated negative pulse from appearing through D_3 at the output while the SCS is off.

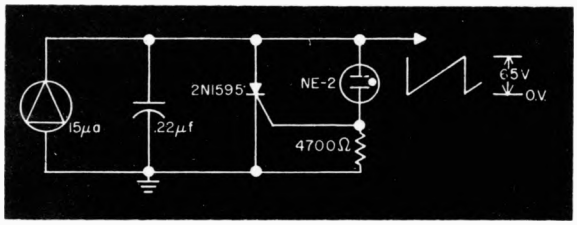
If the anode gate and cathode gate are brought out separately, the circuit can be used as set-reset flip-flop with appropriate signal.

The circuit operates satisfactorily over the temperature range of $-55°C$ to $+100°C$.

High-Current Switch Has High ON/OFF Z Ratio

IN A CERTAIN APPLICATION, a threshold device was required to discharge a capacitor which was being charged from a constant-current source. Since the charging current was about 10-15 μa, the discharging device was required to have an extremely high impedance until breakdown, after which it discharged the capacitor down to a fraction of a volt.

A standard resistively biased SCR could not be used because the bias resistors would bleed off the small charging current and the capacitor would never become charged. A zener or avalanche diode might have been used to hold off and then fire the SCR, but the charging circuit still would be required to supply an appreciable triggering current to the SCR gate.



Neon lamp provides high resistance in off state, fast switching to low-resistance state, and offers low cost.

The substitution of a neon bulb (NE-2) for a zener diode gives several advantages. The voltage step of approximately 10 volts when the NE-2 breaks down will give a good pulse of current into the SCR to ensure its rapid firing. The impedance of the NE-2 before firing approaches 100 meghoms, and certainly not least in attractiveness is the almost 100-to-1 price advantage of the NE-2 over a silicon zener diode.

Normal and Calibrate Mode Switching Circuit

IN A DEVICE having separate "normal" and "calibrate" modes of operation, it is often necessary to initiate an electrical change when transferring to the "calibrate" mode and to assure that several calibration sub-modes are utilized in sequence, and that they are all employed and then rechecked before the device is returned to the "normal" state. The circuit shown accomplishes these functions.

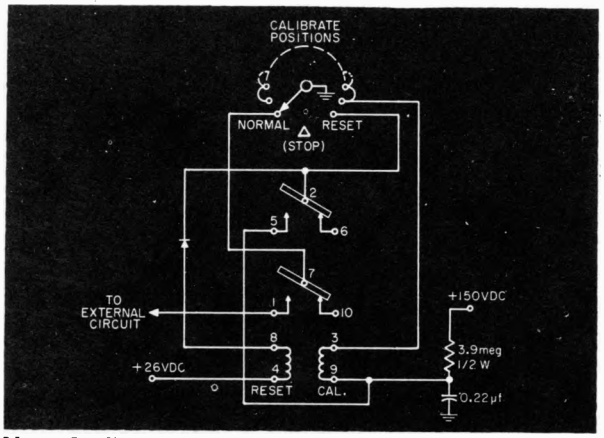
The relay is a magnetically latching bistable type. The switch is a section of the Normal-Calibrate rotary switch, having several calibrate sub-modes and a "reset" mode.

With the switch in "normal" and the relay in the "reset" mode, a ground is connected via the switch rotor and relay contacts 1 and 7 to the external circuit. Upon switching to the first "calibrate" mode, ground is removed from the external circuit and applied through the strapped calibrate mode switch positions to terminal 3 of the "calibrate" relay coil. Current from the previously charged capacitor operates the relay to the calibrate position. Continued application of the ground to relay terminal 3 prevents recharging of the capacitor.

After turning the switch through all "calibrate" positions, advancing it to "reset" applies a ground through the diode to relay coil terminal 8, causing the relay to transfer to the "reset" position. As soon as transfer is made, contacts 2 and 5 re-apply the ground to the "hot" side of the capacitor, preventing its potential from rising, and as the switch is turned back through the calibrate modes, near-zero potential is maintained across the capacitor by the low resistance shunting of the relay's calibrate coil.

Upon operation of the relay to the reset position, connection is again made from the switch's "normal" position via contacts 1 and 7 to the external circuit. Thus when the switch is returned to its "normal" position, the ground is re-applied.

Note that only when the switch is fully advanced to the reset position can the ground to the external circuit be re-applied. Also, the switch must be rotated back through all the calibrate positions to "normal" before the normal mode is reestablished. As soon as the switch reaches "normal," the impulse capacitor is recharged from the +150-v supply. The charging resistor is made large so that recharging during the switch transfers is not enough to operate the relay.



Normal-calibrate mode switching circuit.

Simplified 120 VAC Latching Circuit

WITH ITS SPECIAL trigger and conduction characteristics, the bidirectional controlled rectifier (G.E. Triac) allows simplified static switching of ac power circuits, thereby replacing more complicated circuit arrays of SCRs or power transistors. Figure 1 illustrates how a single BCR, combined with only two other components, a resistor and a capacitor, provides latching action for full wave a-c power at commercial line voltages.

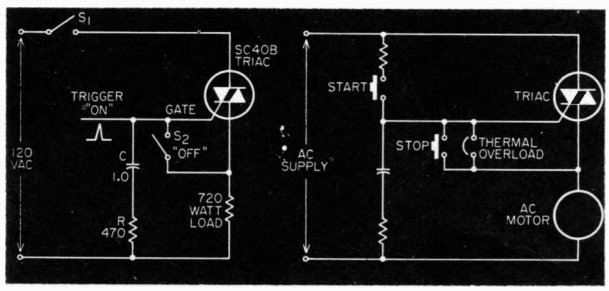


Fig. 1 Fig. 2

Fig. 1. AC latching switch.
Fig. 2. AC motor starter.

In its non-triggered mode, the BCR blocks the application of line voltage to the load. When triggered on by a pulse at its gate, the BCR switches into conduction, applying line voltage to the load. Since the gate is essentially at the same potential as anode 1 of the BCR, capacitor *C* charges to the load voltage through *R*. When the line voltage reverses at the end of a half cycle, capacitor *C* discharges through the BCR gate and the load, thereby triggering the BCR for the next half cycle.

Because of the BCR's bilateral trigger characteristics, this action continues on succeeding half cycles, providing latching action without any further external gate signals. The BCR can be turned off by momentarily shunting the discharge current of *C* around the gate through the reset "OFF" contact or by momentarily opening the main power line.

Figure 2 illustrates how the basic circuit can be adapted to simulate the action of an ac motor magnetic starter. Momentary closing of the "START" button latches the BCR on and starts the motor. The motor is shut down by loss of line voltage, momentary actuation of the "STOP" button, or closing of the thermal overload contact.

Versatile Tunnel-Diode Discriminator

THERE ARE TWO characteristics of a tunnel diode which limit its operation: as a germanium device, it can directly switch only a germanium transistor; and, because it is inherently a latching device, its use is limited to a one-shot operation where the diode is biased to its peak current. A low-level signal then trips it into a high-voltage state and a decaying current due to an inductor in series with the diode resets it to its low-voltage state. To solve the first difficulty, the diode should be connected to a dc amplifier; the second is ideally solved by operating the dynamic load line as in Fig. 2.

In the circuit of Fig. 1, TD_1 is biased close to its peak current, A in Fig. 2. Q_1 is biased by CR_1 so that its collector is at 4.7 V. This is because the voltage gain of Q_1 is 10 and the tunnel diode is in its low-voltage state. The voltage at the emitter of Q_2, 4 V, back-biases CR_2. The load line of the tunnel diode is then set by P_1, AB in Fig. 2.

As soon as the input voltage causes the current through R_3 to exceed the diode peak current, the diode switches to its high-voltage state, 0.5 V. Q_1 amplifies this change by a factor of 10. The emitter of Q_2 drops to 0.7 V. CR_2 becomes forward-biased and now P_2 absorbs current from P_1, causing the load line to shift to AC in Fig. 2. The input current now has only to drop to I_v to revert the diode to its original state. Rise and fall times are about 10 nsec.

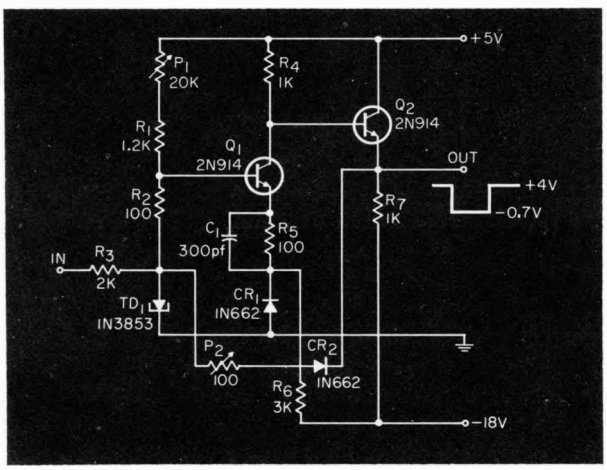


Fig. 1. Tunnel-diode discriminator using dc amplifier.

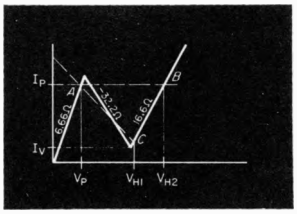


Fig. 2. Tunnel-diode characteristic with operating load lines.

Audio On-Off, Phase-Reversing Switch

THE CIRCUIT SHOWN ENCLOSED in dotted lines in Fig. 1 electronically switches an audio signal on and off. In addition, with the potentiometer connected at the output as shown, a reversible phase signal can be obtained.

Transformer T_1 is a miniature audio isolation transformer that has its secondary referenced to ground through the transistors, the impedance of one side being established through Q_1 and the impedance of the other through Q_2. If the flip-flop A output is at 10 V and the A output is at ground, Q_1 will be forward-biased and will conduct, establishing a low impedance to ground. At the same time, Q_2 will be reverse-biased and the other side of the transformer will see essentially an open circuit to ground. Opposite impedance conditions exist for the opposite state of the flip-flop.

By taking the output from point B or C to ground, the audio on-off function is achieved as the flip-flop changes state. A signal is on at B and off at C for one condition of the flip-flop, and on at C and off at B for the other state.

The potentiometer connected from B to C in Fig. 1 produces a signal from the wiper to ground that reverses its phase each time the flip-flop changes state. The relative amplitudes of the two phases depend on the setting of the pot, and a 10-K pot will drive a 10-K load with no detectable phase error for any setting of the wiper.

If two of the electronic switches are connected to a flip-

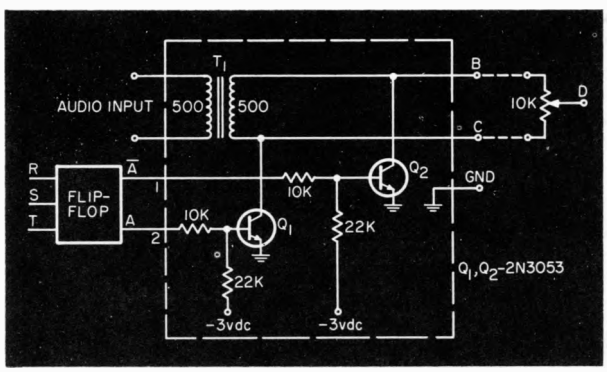


Fig. 1. Electronic audio switch.

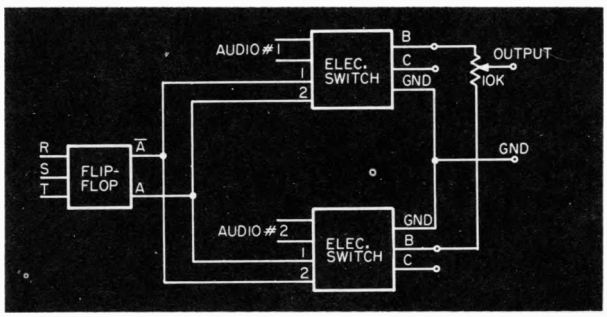


Fig. 2. Two-channel audio switch.

flop as shown in Fig. 2 and each is excited by a different audio signal, then a pot connected across two B or two C outputs as shown will provide a signal from the wiper to

ground that alternates from one audio signal to the other as the flip-flop changes state. Here the pot setting determines the relative amplitudes of the two signals. If the audio inputs are pure sinusoids, the arrangement is a convenient generator of audio FSK signals. If the audio signals are voice channels, the circuit functions as an efficient electronic intercom switch.

Minimizing Inductive Kick and Fall Time

A CIRCUIT USING a zener diode can very effectively be used to reduce the kickback voltage of an inductive load and simultaneously minimize the time to reach a low level of current.

Considering a relay where drop-out time depends upon quickly reaching a low level of current, the circuit arrangement for fastest current fall is as shown in Fig. 1a. However, this arrangement does not provide any voltage protection for the transistor from the inductive kick when the transistor is shut off. The usual method of providing voltage protection is shown in Fig. 1b. The undesirable feature of this circuit is the increased time for the current to decay. In a relay this means increased drop-out time. Also, it involves a trial and error procedure to establish the value of R_s.

The circuit using a zener diode and conventional diode as shown in Fig. 2 provides the fast current fall of Fig. 1a while controlling the kickback voltage as in Fig. 1b. The ordinary diode prevents the inductive load from being shorted in the "ON" state. The kickback voltage in Fig. 2 cannot exceed the zener breakdown voltage. The response for the current i from time $t = 0$ (transistor shut-off) to $t = T$ is shown in Fig. 2 and represented by

$$i = \left(\frac{E}{R} + \frac{V_z}{R}\right) e^{-\frac{R}{L}t} - \frac{V_z}{R}$$

Setting this current equal to zero and solving for time T:

$$T = \frac{L}{R} \ln\left(1 + \frac{E}{V_z}\right)$$

To minimize T, E should approach zero or V_z should approach infinity. In practice E is usually fixed and V_z cannot exceed the breakdown voltage of the transistor.

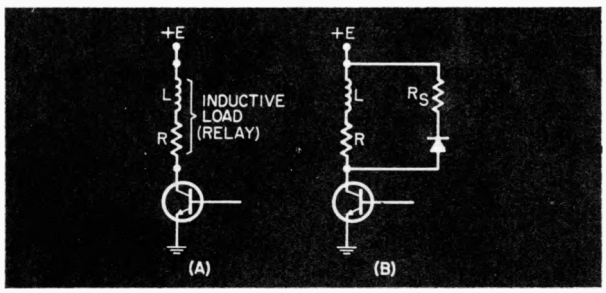


Fig. 1. Inductive load switching circuit (1a) and kickback protection circuit (1b).

The circuit in Fig 2 was tried with several relays and other electromagnetic devices while using a Continental CD3168 51-v zener and a GI 1N3938 diode. In all cases the time for drop-out was not more than 10 percent greater than the time taken for the circuit in Fig. 1a. In Fig. 1a a switch was used in place of the transistor because of the high kickback voltages. The resistance R_s in the circuit of Fig. 1b was adjusted so the kickback voltage was just less than 51 v. At this value of resistance the drop-out time increased from 250 percent to 700 percent. The equation for T also can be used for measuring inductance by measuring the value of T on a current trace.

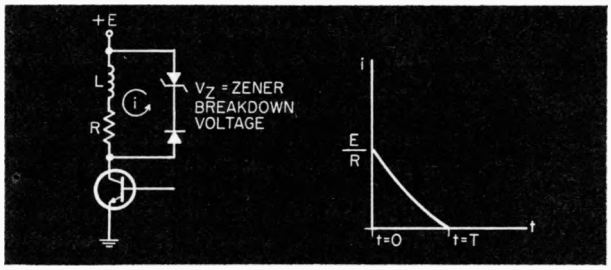


Fig. 2. Voltage protection with diode and zeuer with current decay curve.

DC to DC One-Shot Starting Circuit

IN THIS CIRCUIT, components R_1, C_1, D_1, R_2 and Q_1 function as a one-shot turn-on circuit connected to a typical Royer circuit. Turn-on is independent of the rate of application of the supply voltage, V_s.

At time t_o, D_1 is cut off, and Q_1 supplies turn on current to the base of Q_2. This current is limited by R_1. Note that excessive starting current will inhibit oscillations since it divides between the transistor base and the feedback winding, and as such, represents bucking amp-turns.

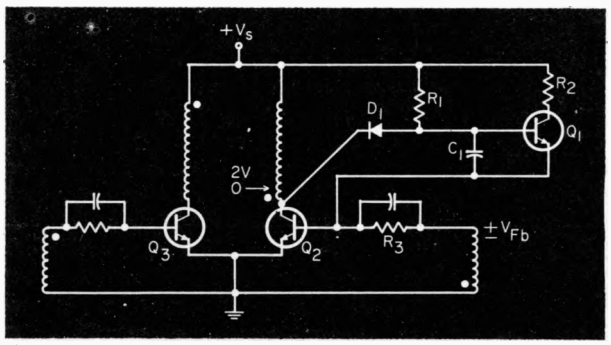


Fig. 1. DC to dc one-shot starting circuit.

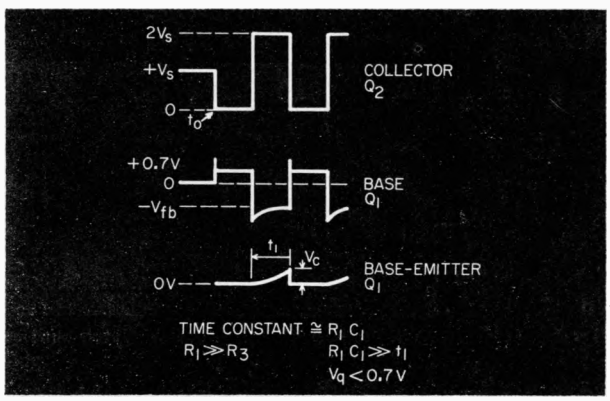


Fig. 2. Waveforms.

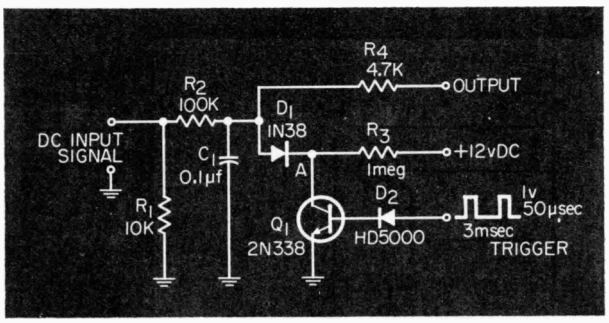
When Q_2 turns on, D_1 clamps the base of Q_1 to 0.8 v. while the base of Q_2 clamps the emitter of Q_1 to 0.7 v. Thus Q_1 is cut off. During the alternate half cycle, C_1 charges toward $+V_s$ via R_1. If the C_1 R_1 time constant is

long compared with a half-cycle, C_1 cannot charge to +0.7 v and Q_1 does not conduct. The function of C_1 is to force the base of Q_1 to follow the emitter of Q_1, which goes to $-V_{bb}$ during the alternate half cycle. (See Fig. 2.) This same scheme is applicable to initializing digital circuits where the frequency of operation is high compared with R_1 C_1.

Integrator Clearing Circuit

THIS SIMPLE CIRCUIT meets the requirement of "clearing" the integrator (R_2, C_1) in approximately 50 μsec while providing isolation between the integrator and the switching network.

During the presence of the trigger pulses, Q_1 is turned on, placing point A at ground. The energy stored in C_1 is then shunted to ground through D_1. Capacitor C_1 discharges to a minimum of approximately 0.3 v, the contact potential of diode D_1 (germanium). Between trigger pulses, diode D_1 isolates the supply voltage from the integrator capacitor.

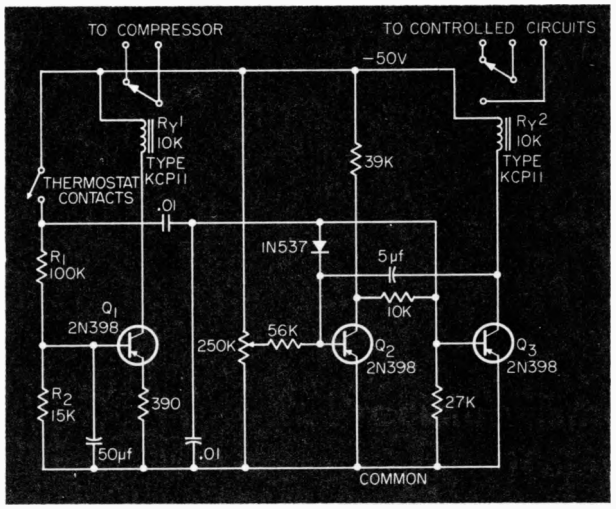


Clearing circuit for R_2-C_1 integrator network.

Diode D_2 is a steering diode. The output is connected to a differential amplifier for voltage level detection.

Motor Transient Anticipator

THIS CIRCUIT is used to turn off a battery of sensitive counters for a preset interval during the switching period of a nearby air conditioner, so as to avoid extraneous counts from the compressor and control switching transients.



Motor transient anticipator.

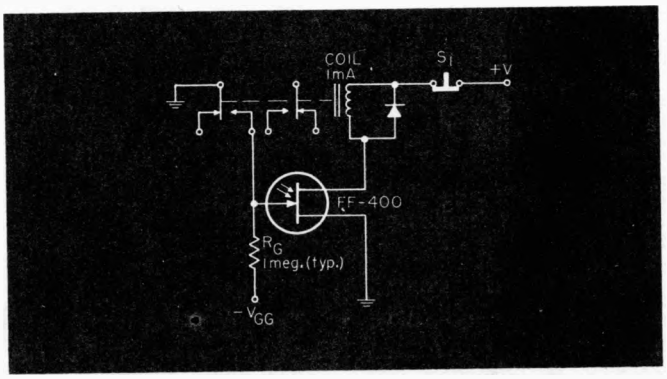
Transistor Q_1 delays the air conditioner thermostat ON signal by its input time constant, after which it pulls in RY_1, turning on the compressor. The thermostat signal also triggers univibrator Q_2Q_3 which rapidly energizes RY_2, thus disabling all critical counters via control relays. The univibrator time constant is chosen about twice the length of Q_1 delay, typically 2 sec. During this period all air conditioner switching transients occur, after which Q_3 returns to cut-off, dropping out RY_2 and re-energizing the protected counters.

The same sequence occurs for the air conditioner turn-off cycle with the exception that the turn-off delay is made approximately equal to the turn-on delay by discharge resistor R_2.

Light-Activated Latching Relay

THE PHOTO SENSITIVE FET, like other junction field-effect transistors, is a normally "on" device. In the relay configuration shown, the device is biased off by $-V_{GG}$ via R_g. When light is applied, gate current flows, causing a positive voltage across R_g in opposition to that of $-V_{GG}$, placing the device in an "on" condition. This energizes the relay, closing the contacts at the gate.

With the closing of the gate contacts, a zero-bias condition is maintained and the relay becomes latched. The circuit will remain in this condition until $B+$ is interrupted by S_1. The circuit sensitivity is proportional to the value of R_g, and by adjusting its value, a sensitivity range as high as 10^6:1 can be realized. This configuration can be used in light activated alarms such as smoke detectors, tape recorders for end of tape sensing, and other similar applications.



Photosensitive FET gives light-activated latching relay.

Low-Cost Bistable Relay Circuits

BISTABLE CIRCUITS using ordinary relays are cheap, and are quite adequate for many low-speed applications in binary registers etc. They may also be used as a substitute for latching relays. Here are two circuits, using capacitor transfer (Fig. 1) and relay transfer (Fig. 2).

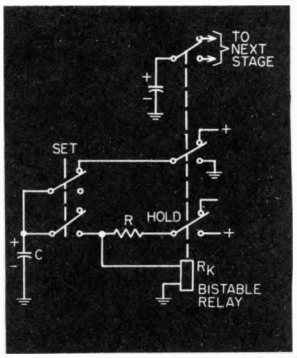


Fig. 1. Bistable relay circuit with capacitor transfer. When used for binary register applications, the "set" contacts shown are part of the bistable relay for the preceeding stage.

In the circuit shown in Fig. 1, capacitor C is initially charged to the supply voltage. When the "set" contacts are activated, capacitor C will discharge through relay coil R_k and the relay will be energized if the time constant R_kC is large. Before the capacitor is completely discharged, the "hold" contact will close and the relay will continue to be energized by the current flowing through resistor R. The "set" contacts may now be deactivated, whereupon the capacitor will discharge rapidly through the grounded relay contact. When the "set" contacts are again activated, the capacitor will provide an effective short across the relay coil, and the relay will be deenergized. After the "set" contacts are returned to the deactivated position, the capacitor will be recharged to the supply voltage and the circuit is ready to repeat the cycle.

The circuit of Fig. 2 is similar to that of Fig. 1 with the exception that the capacitor has been replaced by a relay to perform the transfer-storage function. This transfer relay is initially energized through the "set" contacts and the contacts of the bistable relay, making the supply voltage available to energize the bistable relay when the "set" contacts are activated. After activation, the current through the coil of the transfer relay is maintained through a limiting resistor and through the transfer relay contacts. Upon deactivation of the "set" contacts, the coil of the transfer relay will be shorted to ground through the contacts of the bistable relay, thus deenergizing the transfer relay. The transfer relay contacts will now be grounded and the coil of the bistable relay will thus be deenergized when the "set" contacts are again activated. When the "set" contacts are deactivated, the transfer relay is energized and the circuit is ready to repeat the cycle.

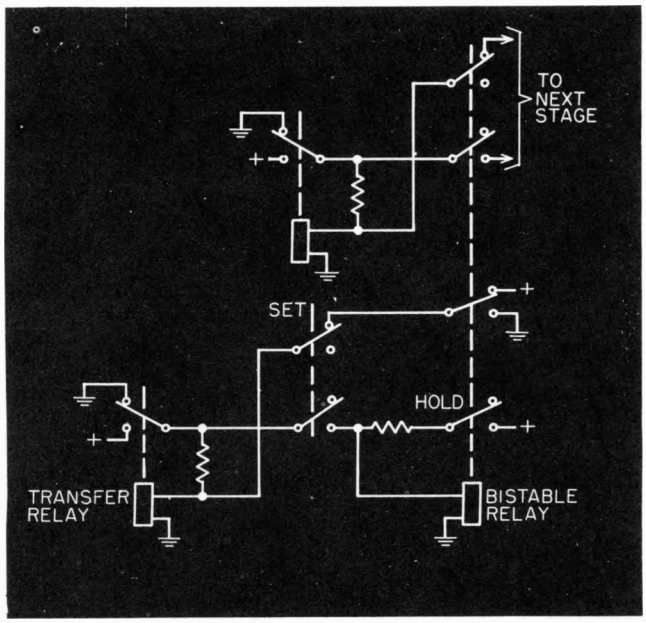
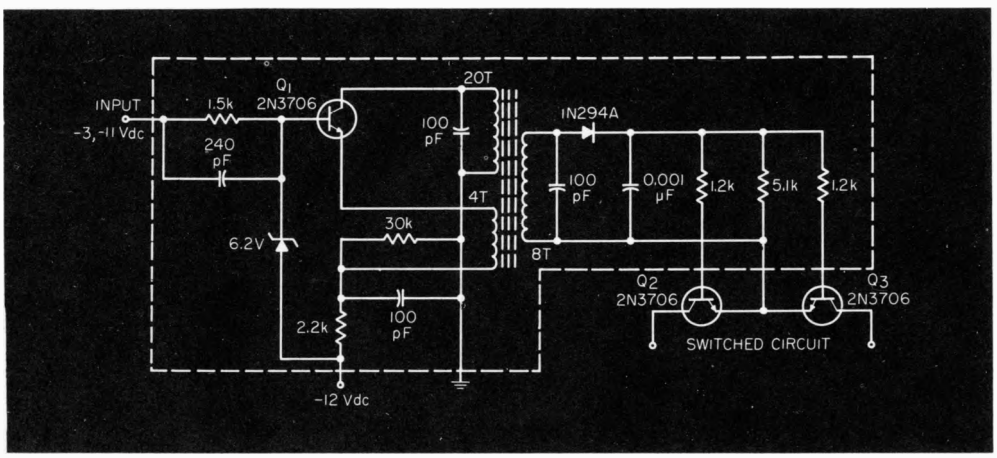


Fig. 2. Circuit similar to that shown in Fig. 1 except that a second relay is used instead of the capacitor for transfer storage.

Solid-State Relay

THIS CHOPPER-DRIVER circuit switches at rates from dc to 10 kHz. Its switched output is completely isolated from the input control signal. The circuit has many of the qualities of a conventional relay, but is much more reliable because it is totally solid state.

The left-hand part of the circuit shown, is a common-base oscillator. Frequency of oscillation is about 10 MHz. Input logic signals bias the base of Q_1, turning the oscillator on and off. Output from the oscillator is transformer coupled, to provide dc isola-



Solid-state switch driver replaces conventional relays.

tion. After rectification and filtering, the oscillator output controls the bipolar switch Q_2, Q_3. The transistor switch shown has an "on" resistance of about 20 ohms, plus a few millivolts offset. "Off" leakage current is less than 1 μA.

The transformer is wound on an Arnold A4-134P toroidal core. Number of turns for each winding is shown in the schematic.

Input logic levels are −3 and −11 V, which are standard for the EECO T-series and similar logic modules.

The basic driver circuit can control other circuits instead of the simple bipolar switch shown here. For example, it can drive a dual-emitter chopper such as the 3N74.

Also a dc load can be controlled via a Darlington-connected switch. For an ac load, the rectified output from the driver can control an SCR circuit[1], which in turn will control the load.

In all the above applications, the basic driver circuit remains the same. Thus it can be encapsulated to form a versatile module. Only the switching transistors are left outside the module (shown dotted) as these may need to be changed for different applications, or replaced if they get damaged by overload.

Reference

1. "150-W Voltage Controller," *SCR Manual, 2nd Edition*, General Electric Co., 1961, p. 116.

Added transistors reduce capacitor size for relay pull-in delay

Pull-in time of relays can easily be slowed, merely by shunting the relay coil with a capacitor. But, for long time delays and with low-resistance coils, several thousand microfarads of capacitance may be needed. However, by adding a simple transistor amplifier, much smaller capacitors can be used to achieve the same time delay.

Figure 1 shows the basic circuit. When switch S_1 is closed, the charging current of C_1 biases Q_1 into saturation. The transistor then shunts the relay coil, preventing pull-in, and the supply voltage appears across R_1. During the charge period, resistor R_3 protects the transistor's base-emitter junction from excessive current. Similarly, series resistor R_1 protects the emitter-collector junction.

The relay can not pull in until Q_1 ceases to shunt the coil. This occurs when the voltage across C_1 approaches the supply voltage, thus removing the forward bias from the transistor.

To reset the relay, we reopen the switch. Diode D_1 protects the transistor from inductive kickback from the relay coil when the current is interrupted.

But the simple circuit of Fig. 1 has a disadvantage. When S_1 is opened, the capacitor charge bleeds off slowly through resistors R_1, R_2 and R_3, and through the relay coil. Thus the circuit has a slow reset time.

To speed reset time, we can use a spare set of relay contacts to rapidly discharge the capacitor through a resistor as shown in Fig. 2. If resistor R_4 is around 100 ohms, reset will be almost instantaneous.

Fig. 2 shows, also, how we can obtain additional gain by connecting two transistors in the Darlington configuration. In a practical 28-volt circuit, the Darlington connection allows a one-second delay for each microfarad of capacitance. Without the transistor amplifier, one would need approximately 5000 microfarads to achieve a one-second delay.

Also in Fig. 2, we see how a bridge rectifier can be added ahead of the time-delay circuit for operation directly from an ac power line.

In general, high-resistance— or high sensitivity — relays are preferable in time-delay circuits because they need smaller capacitors for a given time delay.

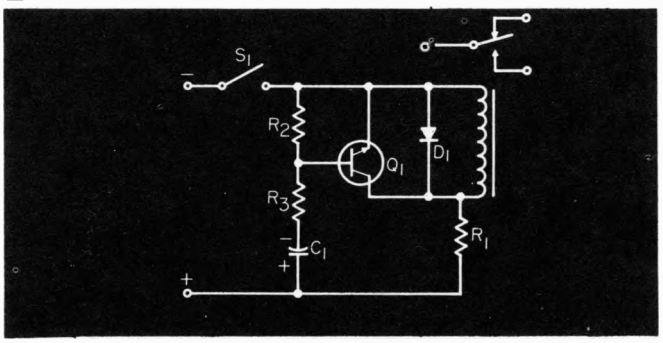


Fig. 1. In this simple time-delay circuit, transistor Q_1 reduces the size of capacitor C_1 needed for a given time delay. But this circuit has slow reset because C_1 must discharge through the resistors and the relay coil.

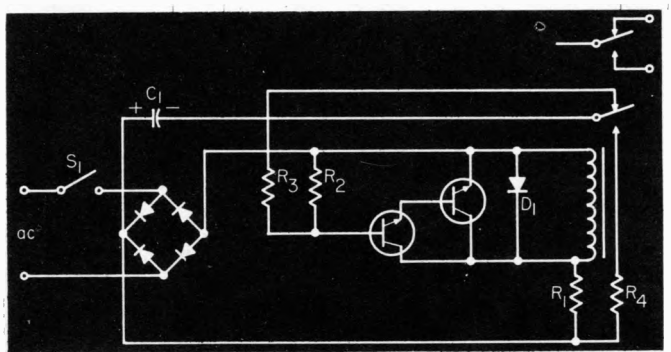


Fig. 2. In an improved circuit, C_1 is rapidly discharged through R_4. Darlington connection gives increased gain and further reduces the size of C_1. A bridge rectifier allows ac operation.

Improved tunnel-diode threshold circuit has adjustable hysteresis

IT'S WELL KNOWN that a tunnel diode TD_1 can be connected between the base and emitter of a transistor Q_1 to form a simple and stable threshold circuit, as shown in Fig. 1. A major disadvantage of this simple circuit is the large hysteresis of the switching characteristic, shown in Fig. 2.

Figure 2 shows that the tunnel diode switches to its high-voltage state when input current i_1 is greater than the diode's peak current I_p. But the diode doesn't switch back to the low-voltage state until i_1 is less than the sum of the diode's valley current I_v and the transistor's base current I_b.

Figure 3 shows an improved circuit in which the hysteresis can be varied over a wide range from positive values to zero. The circuit can also be adjusted to give negative hysteresis though, of course, this is an unstable state.

When the diode TD_1 is in the low-voltage state, Q_1 is nonconducting and bias current i_2 flows through resistors R_L, R_4 and R_3 into the diode. This continues until the input current i_1 reaches the value I_p-i_2. The diode then switches to the high-voltage state and Q_1 saturates. The saturation voltage of Q_1 is only a few hundred millivolts, therefore no bias current i_2 can flow into the diode. Before TD_1 can switch back to the low-voltage state, i_1 must be less than $I_v + I_b$.

If we increase i_2, by adjusting R_4, we can reduce the value of i_1 required for the diode to switch to its high-voltage state. The value of i_1 for back-switching remains unchanged. So we can reduce the hysteresis of the circuit. This is shown dotted in Fig. 2.

The current values for the three possible hysteresis modes are given by the following expressions:

For positive hysteresis,

$$i_2 < I_p - I_v - I_b \quad (1)$$

For zero hysteresis,

$$i_2 = I_p - I_v - I_b \quad (2)$$

For negative hysteresis,

$$I_p - I_v - I_b < i_2 < I_p \quad (3)$$

If the circuit has negative hysteresis, it will oscillate when the input current i_1 is greater than $I_p - I_2$ but less than I_b. The period of oscillation is determined by the switching time constants of Q_1 and by external capacitance C_1 (see Fig. 3).

For normal operation with positive hysteresis, temperature stability of the lower threshold is determined by currents I_v and I_b. Tempco can be greatly improved by first choosing a tunnel diode having a high I_p/I_v ratio and then adding a parallel resistor R_2. The value of R_2 should be selected so that the resulting I_p/I_v ratio is only 3/5, for R_2 and TD_1 together. This technique reduces the temperature coefficient more than four times without appreciably reducing the switching speed of Q_1. Complete compensation can be achieved by using a negative tempco resistor in place of R_2.

The semiconductors used in the original version of the Fig. 3 circuit were of European origin. The tunnel diode was a GaAs type with an I_p of 10 mA (similar to RCA 40060). Q_1 was a high-speed switching transistor type BSY62 (similar to 2N706A).

The circuit was developed for interfacing within a digital computer. Output levels are compatible with TTL or DTL ICs.

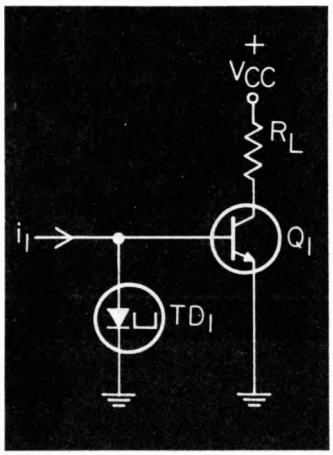


Fig. 1. Widely-used tunnel-diode threshold circuit has the disadvantage of high hysteresis.

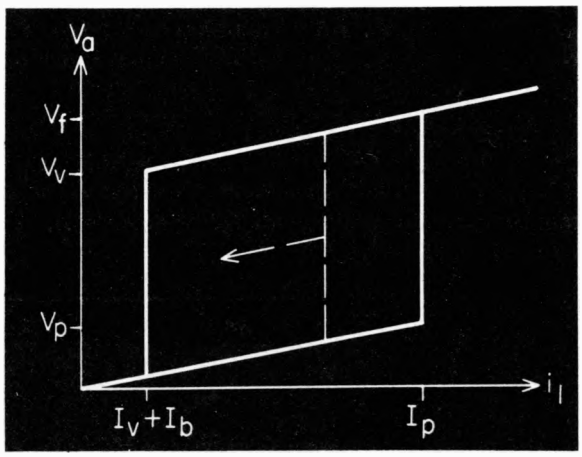


Fig. 2. Hysteresis loop of tunnel-diode threshold circuit. Dotted line shows how hysteresis can be reduced by lowering the value of i needed for switching to the high-voltage stage.

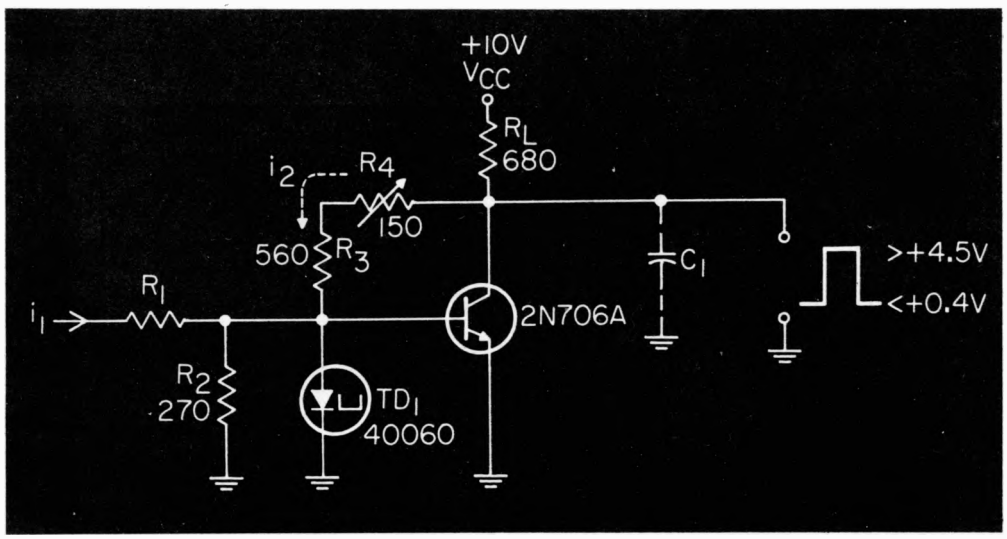


Fig. 3. Improved threshold circuit with adjustable hysteresis. The magnitude of current i_2 determines whether the circuit hysteresis is positive, zero or negative.

An improved rotary-switch interlocking circuit

SOME SORT of interlock circuit is often needed for use with rotary switches. For example, if a switch selects voltage inputs to a multi-range measuring instrument, it would be desirable to prevent switch rotation until the measuring instrument has been set to the correct range — otherwise the instrument could be damaged by excessive voltage.

There are various ways of interlocking switches, but many of them have serious disadvantages. For example, one widely-used method is to interlock a relay-coil voltage through its own contacts, and through the switch as shown in Fig. 1. When S_1 is depressed, K_1 is energized, allowing the interlocked signals to pass through the remaining contacts. When S_1 is rotated K_1 de-energizes momentarily, thus interrupting the interlocked function until K_1 is again energized.

But this method can be unreliable because of relay switching time. Most relays take about 10 ms to de-energize (and longer if arc suppressing components such as diode CR_1 are used), and the travel time of most rotary switches ranges from 1 to 15 ms.

Another possible interlock method is to use a special mechanically interlocked rotary switch. The problem with these switches is they're often expensive and clumsy to use.

Fig. 2 shows an improved interlock technique that could overcome the disadvantages cited above. The circuit uses a silicon controlled switch (SCS) Q_1. When S_2 is depressed, voltage divider R_1 and R_2 supplies 1.2 Vdc to turn on Q_1. This provides a ground return for K_1, energizing it and thus allowing signal current to flow through the relay contacts to the monitoring instrument.

When the switch is rotated to another position, point 2

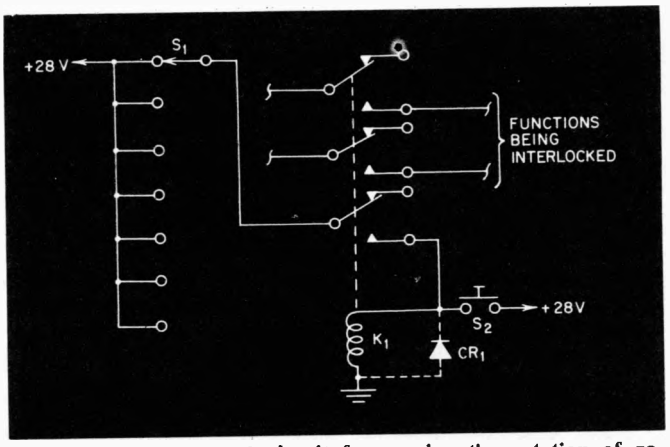


Fig. 1. Commonly-used circuit for sensing the rotation of rotary switch.

provide balanced drive voltages, $\pm V_2 = \pm(V_Z + V_D)$, to the integrator. The resulting sawtooth waveform is symmetrical with a peak amplitude of

$$V_1 = \frac{R_3}{R_4}(V_Z + V_D)$$

The duration of the rise of the sawtooth is

$$\tau_1 = 2\frac{R_3}{R_4}(R_1 + R_2)\,C_1$$

and the fall time is

$$\tau_2 = 2\frac{R_3}{R_4}(R_2 + (R_2 + R_{DS})\,C_1$$

Rise and fall time of the output waveform can be made variable by replacing the appropriate resistors with potentiometers. The waveform parameters are:

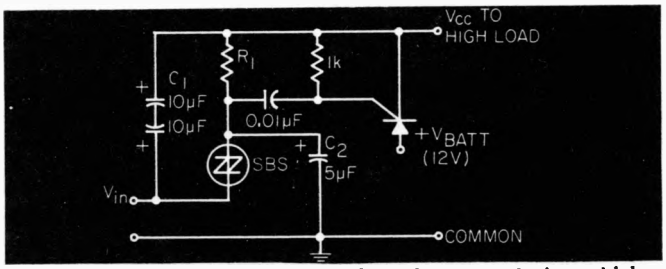
$\tau_1 = 13.2$ seconds
$\tau_2 = 1.2$ seconds
$V_1 = V_2 = 7$ volts

The circuit, with the values shown, is used to sweep a voltage controlled oscillator in a phase-locked loop as part of an automatic acquisition system.

Remote-controlled solid-state switch

Some logic systems require remote circuits which can turn on heavy loads, yet which can be battery powered with low current drain. The duty cycle of such a system may be as low as 1 percent. With most conventional switching circuits, low stand-by current drain usually implies high impedances and slow rise and fall times. If a detector is capacitively coupled directly to an SCR, the detector impedances must be made low enough to couple a pulse of sufficient energy to turn on the SCR. This, necessarily, increases the quiescent current drain.

The circuit shown, however, uses a silicon bilateral switch (SBS) which provides a high input impedance. Thus the switch can easily be driven from a simple detector circuit —for example, a Schmitt trigger. Yet turn-on and turn-off are completely reliable.



Simple switching circuit uses a bilateral trigger device which provides a high input impedance and draws negligible standby current.

The circuit works as follows: In the "off" condition, the high side of the load is at ground potential and C_1 is charged to the lower Schmitt potential, V_{in} (*lower*). When V_{in} rises above the SBS trigger voltage, the output pulse across R_1 couples a turn-on signal to the power controlling SCR. The SCR then back-biases the SBS, returning it to a non-conducting state.

To turn off the circuit, we rely on capacitor C_2 remaining charged at battery voltage. Capacitor C_1 charges to (V_{batt} $-V_{in}$). When V_{in} falls to a voltage that exceeds the SBS firing voltage, in the reverse direction, C_2 is effectively placed in series with C_1 and both capacitors dump their charges into the load. This reduces the SCR anode current to zero, turning it off.

Note that in this circuit the switching voltage of the SBS must be greater than V_{in} (*lower*) but less than the difference between V_{batt} and V_{in} (*lower*).

Bilateral-trigger devices are available from several manufacturers, in a wide range of trigger voltages. Also available are unilateral triggers. These, when connected in a parallel-opposing configuration, act much like the bilateral devices.

General Electric has a bilateral device, D13E, which is available with a trigger range of 6 - 10 volts. Motorola's MPT 28 and MPT 32 range from 24 to 32 and from 28 to 36 volts respectively. These companies also have unilateral devices with ratings up to 50 volts. A smaller firm, Energy Conversion Devices, has delivered units which trigger in the range of 5 to 7 volts. But these are more expensive.

Resistor R_1 must be large enough to couple a substantial pulse to the gate of the SCR, but small enough to allow a quick discharge of C_1 and C_2

for turn-off. A suitable compromise would be around 1 kilohm, in most applications.

Because, in this application, the SBS is primarily a pulse-producing device, one should take care not to exceed the rated product of peak current and pulse duration. At low frequencies, the impedance of the device is less than 5 ohms and it is capable of peak currents of 1 to 2 amps. These ratings allow the switching of fairly large SCRs.

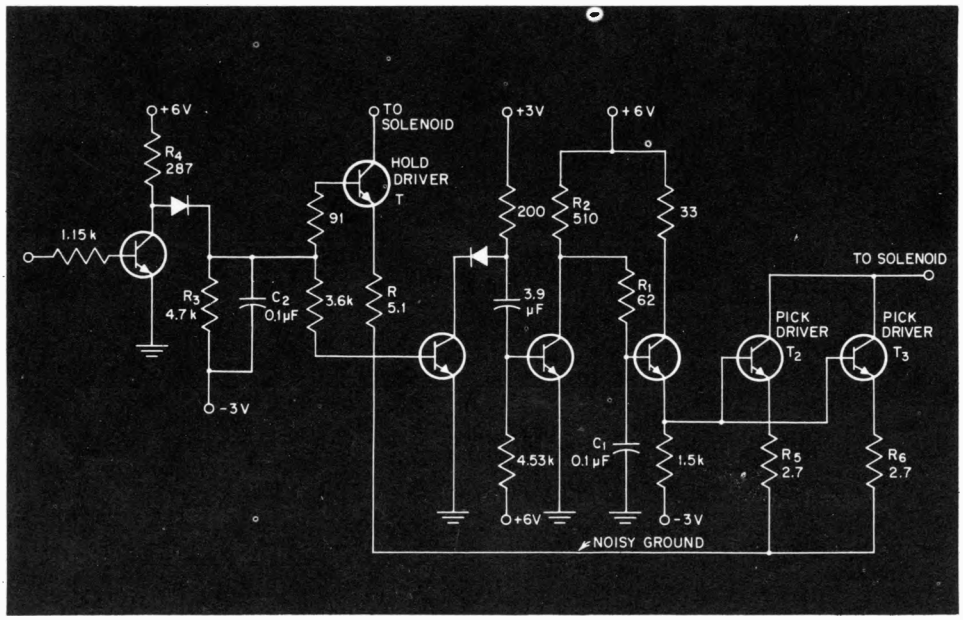
Maximum load currents, therefore, are primarily determined by the current handling capabilities of the SCR. Of course, the SCR should have sufficient gate sensitivity for turn-on by the SBS. Minimum load currents must be at least as large as the SCR holding current. In determining the maximum current for the SCR, one should take into account turn-on time, especially with reactive loads. Capacitor C_1 helps to ensure that short-duration line transients don't prematurely trigger the unit.

Normally the switching circuit will be driven by some sort of detector circuit. This can be any circuit which provides a charging voltage level that exceeds the SBS trigger level. The detector's output impedance must be able to supply the SBS trigger current; usually around 100 microamps.

Thus, $Z_o < \frac{V_{cc}}{I\ (BR)}$

Leakage currents of SBS devices are usually in the range of 50 to 500 nanoamps. ■

Slowed solenoid driver circuit eliminates noise spikes



To eliminate transient noise problems, networks R_1, R_2, C_1, R_5, R_6, and R_3, R_4, C_2, R_7 control the switching speed of high-current drivers T_1, T_2 and T_3.

DRIVER TRANSISTORS can switch large currents so rapidly that they can cause severe noise transients. The solenoid-driver circuit shown here has controlled rise and fall times to minimize noise problems and eliminate system disturbances.

The principle employed is to slow down the transistors so that noise spikes introduced by fast switching are reduced to an acceptable level. The "pick" and "hold" driver transistors are made into amplifiers during their turn-on and turn-off transitions by the addition of small-valued resistors in their emitters (R_5, R_6, R_7). The rise and fall times of the inputs to these driver transistors are slow and controlled by RC networks R_1, R_2, C_1 and R_3, R_4, C_2.

Receiving a slow input transition and amplifying it at its output, each driver transistor turns on and off gradually. The turn-on and turn-off times are relatively independent of the type of transistor.

This circuit produces turn-on times of 20 μs for the "pick" and "hold" drivers and turn-off transition times of 40 μs. The transition times can be adjusted by changing R_1, R_2, C_1 and/or R_3, R_4, C_2. The "hold" driver conducts 250 mA. The "pick" driver conducts 1 A. ■

Simple zero-crossing solid-state switch

MINIMUM RFI is generated when ac power is switched on and off to a load at the zero-voltage crossover point. This switching can be accomplished by a simple circuit consisting of four diodes, an SCR, a transistor and three resistors connected as shown in Fig. 1A.

The positive output of the bridge (Fig. 1B) drives Q_1 on during each half cycle of the supply voltage except when the voltage is at or near zero. The SCR can be triggered on only when Q_1 is off. Closing of switch S_1 provides continuous voltage to the collector of Q_1 but a trigger pulse to the SCR gate is provided only at the zero-crossing point as shown in Fig. 1C. When switch S_1 is open, the SCR will commutate off at the zero-voltage point. The values of resistance for R_1 and R_2 are selected to provide the required pulse width for the SCR being used. ■

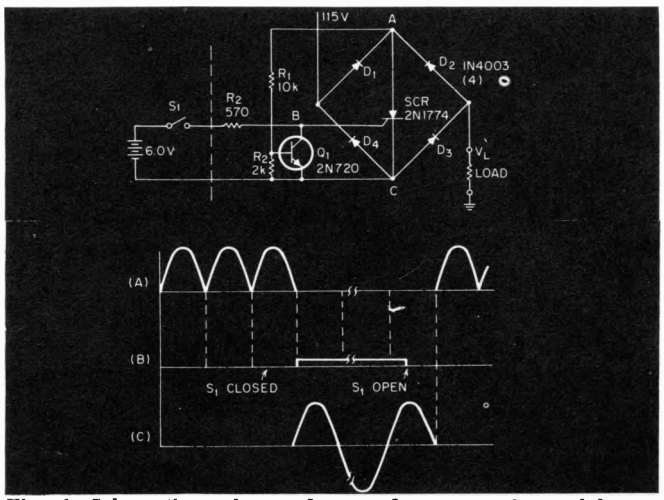


Fig. 1. Schematic and waveforms of zero-crossing solid-state switch.

Section 19
MISCELLANEOUS CIRCUITS

Impedance Matcher for Magnetic Amplifiers

It is sometimes necessary to drive a magnetic amplifier control winding from a relatively high impedance source, where much more voltage is available than the required IR drop of the control winding, such as the output of another magnetic amplifier, and RC time delay circuit or certain transducers. If power loss can be tolerated, a series resistor can be used, giving the advantage of faster response. However, if maximum power gain is required, or if the control winding is to be driven from a low power source, and speed of response is not too critical, the impedance matching device shown may be useful.

The input dc is given a low ac source impedance by bypass capacitor C_1. It is chopped by a diode bridge modulator driven from the main ac supply into the primary of T_1, which is tuned for maximum impedance. The chopper could also be a transistor or other suitable switching device. A full-wave synchronous demodulator is shown, which is suitable for demodulating voltages of less than 1 volt, p-p. Demodulation could also be accomplished by a diode bridge or transistor. Equal capacitors C_3 and C_4 provide a path for the ac demodulator drive current, for which they should be a low impedance, keeping it out of the following magnetic amplifier. In many cases a center-tapped control winding on the following amplifier could be used instead.

With the type of input chopper shown, driving voltage must be at least twice the maximum signal input voltage, to allow the voltage across the primary of T_1 to reverse when the chopper becomes an open circuit. If square-wave chopper drive is used,

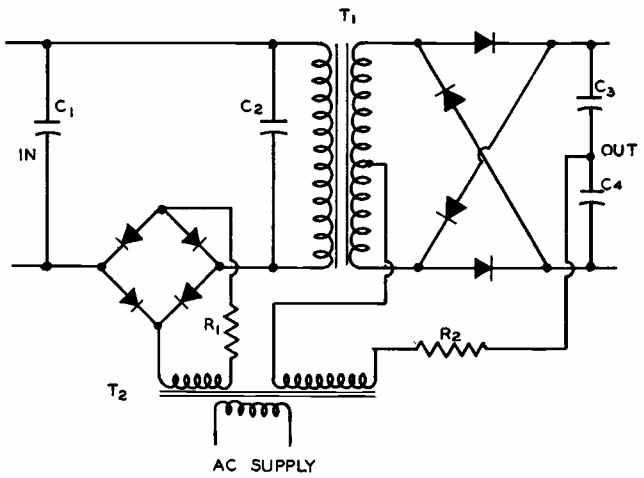


FIG 1—Impedance-matching circuit uses diode chopper and synchronous demodulator.

bypassing R_1 with a suitable capacitor will halve voltage requirements. The driving voltage for the full-wave demodulator shown need be only about one volt, or enough to overcome the diode drop. The size of R_1 and R_2 is determined by providing a diode current greater than the largest signal current. In some cases where signal current is very small, a diode drive current much larger than that of the signal must be used to make the diode impedance low enough. This is easily determined experimentally by decreasing the drive resistor until no further increase in output signal is obtained.

The device as shown provides a fully isolated input and output due to separate drive of the chopper and demodulator provided by T_2. It could be simplified somewhat where these are not needed. Also, if signals of several volts are being handled simpler modulators or choppers could be used.

If the signal source is a low-impedance device compared to readily available control windings, the device could be reversed to step up the impedance,

both power gain and speed of response. Finally, it may find use as a dc impedance matching device in applications unrelated to magnetic amplifiers.

Point-Contact Transistor Multiplier

A POINT-CONTACT transistor and a minimum of additional circuitry can be used to solve the equation $xy = z$. The multiplication is implemented by making the variable x proportional to the emitter current of the transistor and the variable y proportional to the collector current. In this equation z is proportional to collector voltage V_c.

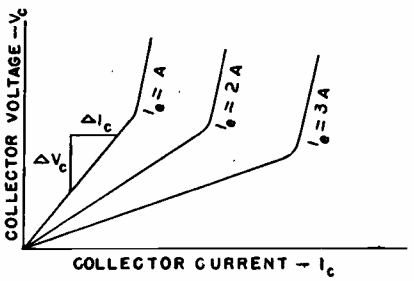


FIG. 1—Collector resistance change for various values of emitter current.

Resistance of the collector-base diode in a point-contact transistor is a linear function of emitter current-collector voltage characteristic curves of a wide range. This fact is illustrated in collector-current-collector-voltage characteristic curves of Fig. 1. The slope of the lines between the origin and the knee of the curves are determined by emitter current and are independent of collector current.

The collector current I_c flowing through the collector-base resistance R_c creates a collector-to-base voltage drop V_c, or simply,

$$I_c \times R_c = V_c$$

This equation is analogus to the opening equation. I_c must be made proportional to the y variable and R_c which is proportional to emitter current is in turn made proportional to the variable x. The xy product or z is then proportional to collector voltage, V_c.

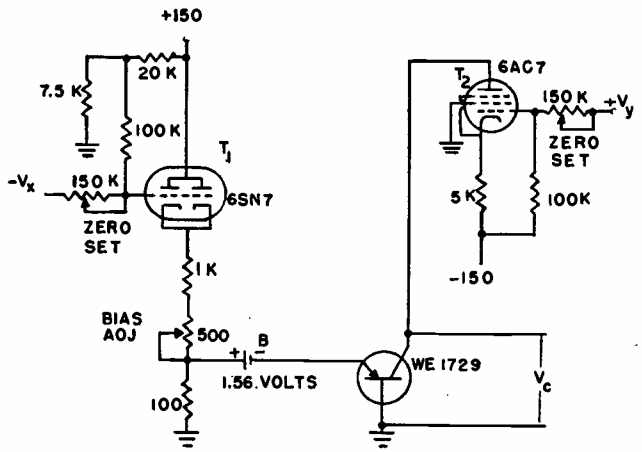


FIG. 2—Multiplier schematic diagram.

The circuit which is used to accomplish the multiplication is shown in Fig. 2. Emitter current and hence the collector resistance R_c is controlled by a voltage V_x fed to the grid of T_1. Collector current I_c is supplied from the constant current generator T_2. A pentode is used as the constant current generator so that I_c is independent of collector resistance, R_c.

Proper bias is established in the emitter circuit by controlling the cathode current of T_1 by means of R_1. R_2 is chosen as 100 ohms to maintain sufficient gain between the x-input voltage and the emitter input current. Since this creates too much positive bias on the emitter, a battery B_1 is used to reduce the bias to the proper level.

Frequency response of the multiplier is very good. Since multiplication is a function of the intrinsic properties of the point-contact transistor, frequency response is only limited by f_{co} characteristics of the transistor and by wiring and tube interelectrode capacities. The point-contact transistor found best suited for the unique application of multiplication is the WE 1729.

Accuracy of multiplication was determined experimentally as being five per cent of full scale output. This accuracy was maintained for variations in V_y from 0 to 25 volts and variations in V_x from —2 to —15 volts. Maximum output is —10 volts.

Eliminating Peak Clipping from Diode A-M Detectors

ADDITION of one 10-cent resistor improves diode a m detectors. Proper application of this resistor will eliminate peak clipping effects allowing the detector to accept 100-percent modulation.

Figure 1a shows a rather poorly designed a-m detector in which $R_1 = R_2$. The rectified carrier, $E_{carrier}$, produces 10 volts dc across R_1 and C_2. At modulation frequencies, where C_2 is a good coupling capacitor, this detector will start clipping at about 50 percent downward modulation as shown in Fig. 1c.

This coupling can be understood if conditions are observed at the time of removal of the rf carrier. Capacitor C_2 will divide the 10-volt charge between R_1 and R_2 with 5 volts appearing on each resistor, since the resistors are equal. This 5 volts is reverse bias for the diode. The diode will not conduct until the instantaneous value of rf on its cathode is more negative than 5 volts.

According to Terman, the maximum downward modulation that this detector will accept without peak clipping is $R_1/(R_1 + R_2) \times 100$ percent or $Z_L/R_L \times 100$ percent, where R_L is the dc resistance and Z_L is the mid-frequency impedance presented to the diode at points X, X' in Fig. 1a.

The detector of Fig. 1a can be made to accept 100 percent modulation without peak clipping by the addition of a constant current to the detector load which exceds the maximum current expected from C_1 during downward modulation and is in opposition to the current from C_2. This constant current will maintain the diode in conduction at 100 percent modulation following the downward mod-

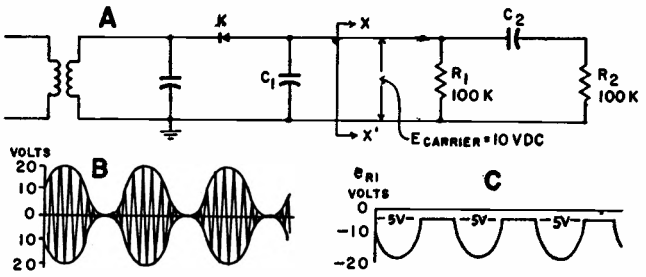


FIG. 1—Diode a-m detector and inherent clipping effect.

ulation of the rf envelope to zero.

The constant current added to the detector does not reduce the demodulated audio level. It causes only a slight shift of the rectified dc level employed for avc. In fact, avc shift due to modulation is greatly reduced when peak clipping is eliminated.

The constant current can be supplied from the plate supply by connecting a high resistance, R_3, as shown in Fig. 2a. To accept 100 percent modulation without peak clipping:

$$R_3 \geqq \frac{E_{bb}\, Z_L}{E_{carrier}\left(1-\frac{Z_L}{R_L}\right)}$$

A further simplification can be had by removing R_1 and adding R_4 as shown in Fig. 2b. To accept 100-percent modulation without peak clipping $R_4 \geqq (E_{bb}\, Z_L)/E_{\text{carrier}}$.

The modification is rewarding, from the lowliest ac/dc set to the most sophisticated navigation re-

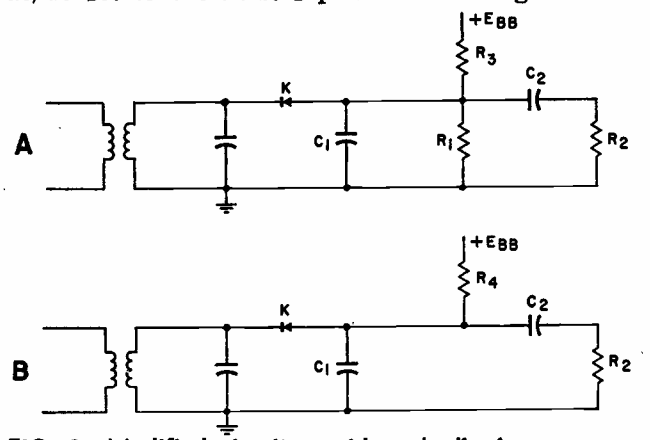


FIG. 2—Modified circuits avoid peak clipping.

ceiver. Normally the more complex the load, the worse the peak clipping. Just add one resistor if the load includes squelch, audio as well as rf avc, and more than one audio output.

A word of caution, this modification will not cure a diagonal clipping problem. It will improve it to a degree related to circuit parameters.

Relay-Operated Energy Restoring Mechanism

THE CIRCUIT to be described is concerned with restoring energy losses in oscillating electromechanical instruments.

Since operation is essentially due to photoelectric actuation of relays in proper combination, the apparatus is free from springs, escapements and other mechanical means of restoring energy losses.

Pendulums are subject to damping due to air friction and other losses. The circuit disclosed here serves the purpose of bringing a pendulum back to the same release point. This provides an dentical

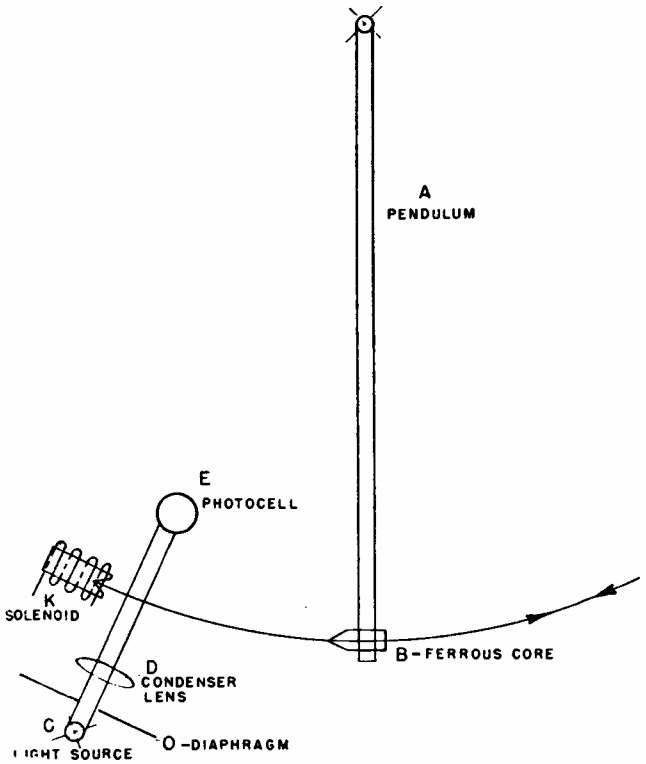


FIG. 1—Basic energy restoring mechanism.

potential energy input at its start.

In Fig. 1 the pendulum A has an adjustable, pointed ferrous shoe at its end B. When moving it intercepts a beam of light near its return point.

This latter originates in the illuminating source C which produces a pencil of light. It is limited by the iris O, is collimated through the condenser lens D and falls on the photocell E. Upon illumination of said photocell E, a flow of electric current takes place which operates a sensitive relay.

As shown in Fig 2, a Weston contact galvanometer relay F closes a circuit consisting of photocell G, the resistance of which is lowered upon illumination, and the battery H.

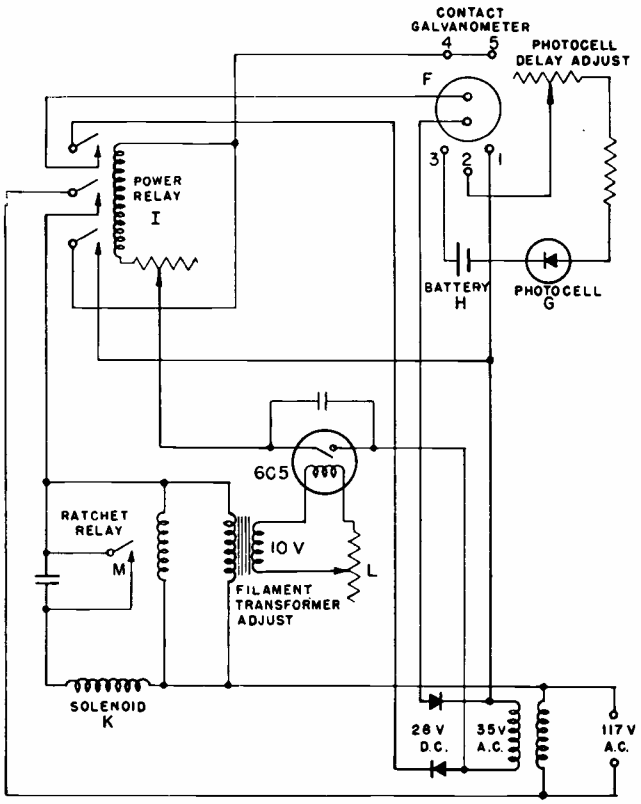


FIG. 2—Solenoid drive circuit for pendulum.

Upon deflection of the galvanometer relay *F*, the power relay *I* is actuated. Relay *I* energizes the solenoid *K*. The length of time during which current remains flowing through the solenoid *K* is controlled by a time delay such as an Amperite 6C5, the actuation of which is adjusted by an adjustable rheostat *L* operating its heater coil. A ratchet relay *M* is inserted in the circuit and mounted in such a manner that only every other pulse produces actuation of the solenoid *K*.

Therefore, when the pendulum's ferrous shoe *B* moves backwards upon release from the solenoid *K* and thus intercepts the beam of light the second time, the core is not pulled back into the solenoid *K* but continues on its path.

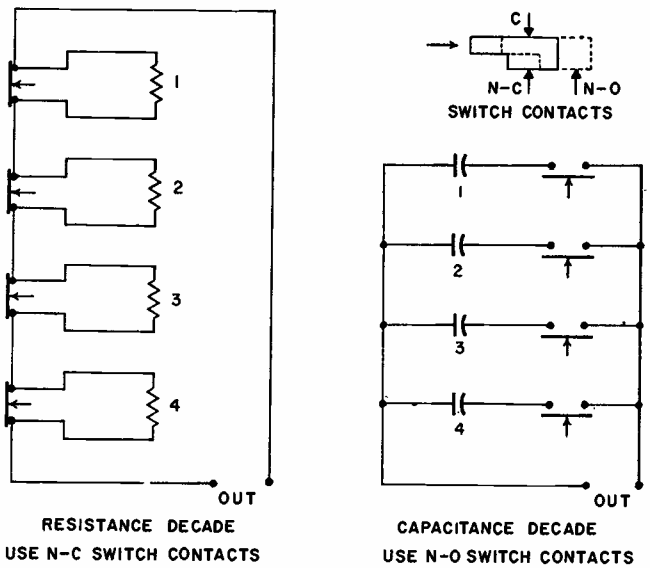
Restoring circuits of this type for pendulums and similar bodies make possible the design of timing circuits and other devices of extreme precision. In addition, by using non-rigid pendulums, such as strips of elastic materials, bending wires and the like, accurate studies of elasticity, recovery characteristics and certain rheological phenomena in said materials can be made.

This pendulum can also be made to swing in viscous fluids, air, rare gases and the like and the precise timing of its motion as well as the recording of its decay curve, permit investigations of the behavior of the medium in which the pendulum swings.

Pushbutton Decade Box

FOUR pushbuttons and four resistors allow selection of ten values from a decade box. The assembly consists of four latching push buttons, each one being a spdt switch, with a fifth button being used to release any of the four latched buttons. The normally closed contacts are used along with the common contacts of each switch.

Each resistor is shorted out until a button is pushed. Pushing the one button puts one unit in the circuit, pushing the two button puts the two unit



Switch connections for two types of decade boxes.

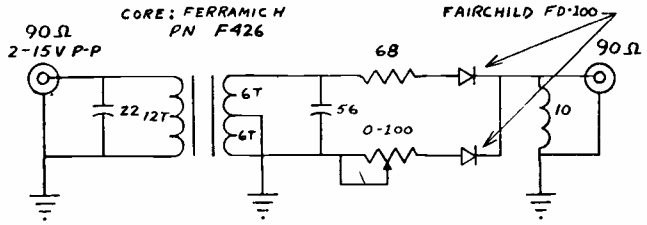
in the circuit, likewise the three and four buttons. To get six units, buttons two and four are pushed. To get seven units, buttons three and four are pushed. To get eight units, buttons, one, three and four are pushed. To get nine units, buttons two, three, and four are pushed. To get ten units simply push all buttons and all the resistors add together. Binding posts are mounted on the other end. This allows connecting the boxes end to end which will put the resistors in series, and allows adding together any number of decade boxes.

The capacitor decade circuit uses the normally NO contact and the common contact of the switch. Without any button depressed, there is no capacitance in the circuit. By pushing button one, a capacitor is put into the circuit. Pushing the remaining buttons connects additional capacitors.

The buttons are numbered one through four and the fifth button is labeled "Release". The multiplier factor will indicate the actual value that each box will supply.

Passive Frequency Doubler

THE CIRCUIT shown was used to double the frequency range of a Tektronix type 190 sine wave generator, although it may be used with other generators that have a maximum output frequency



Circuit for doubling frequency from 25 to 50 mc.

of 50 mc or less.

The transformer is double-tuned and the circuit operates with greatest efficiency for input frequencies between 25 and 50 mc, producing output frequencies from 50 mc to 100 mc. For this range of frequencies, the attenuation will be less than 12 db, and the rectifying action of the diodes will be smoothed out sufficiently so that distortion will be negligible for most applications.

The 0-100 ohm potentiometer is used to compensate for any diode mismatch, and the 10 μh choke prevents any dc level buildup at the output. The entire circuit can be packed in a small shielded box with BNC connectors for the input and output, and may conveniently be inserted in series with 90-ohm coaxial line when needed.

Phase Shift Network with Third Harmonic Suppression

A SIMPLE, active network is described here which gives an accurate 90 deg phase shift at the carrier frequency. Moreover, it provides third harmonic rejection in excess of 20 db with ±2 per cent inductors, and ±5 per cent capacitors.

The complete network uses only one transistor (or vacuum tube). Some of the advantages of this circuit, by comparison with the double lag, or double lag-lead networks and their associated amplifiers include fewer components, greater gain,

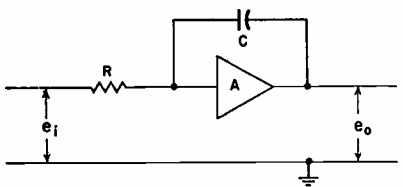


FIG. 1—Basic feedback circuit.

greater third harmonic rejection, precise 90 deg phase shift always maintained, and reduction of space and cost.

The circuit of Fig. 1, where A is negative and large, has a transfer function:

$$\frac{e_o}{e_i} = \frac{1}{j\omega CR} = \frac{1}{\omega CR} \angle -90°$$

The magnitude of the gain is unity when:

$$\omega = \frac{1}{RC}, \quad \frac{e_o}{e_i} = 1 \angle -90°$$

The phase angle of the output voltage is always 90 deg, lagging the input voltage. For a good 90 deg phase-shift network, the amplifier gain should be 20 db, or greater.

To eliminate 1,200 cps components, the circuit can be modified by addition of a series inductance in the feedback loop.

If this LC combination is made series resonant at 1200 cps, the output voltage will tend to zero at this frequency, giving 3rd harmonic suppression.

Below 1,200 cps the impedance of the LC network is capacitive, while above 1200 cps it is inductive. Thus, there is still an equivalent capacitance at 400 cps, and the 90° phase shift is obtained.

Above 1200 cps, the output voltage will rise with frequency, and all harmonics above the third will be amplified. To avoid this, a second capacitor is placed across the inductor resulting in a "Foster type" network shown in Fig. 2.

Having set the first zero to occur at 1200 cps, the second pole can be placed anywhere above 1200 cps. If this pole is set to occur below 1600 cps, the fourth, and all higher harmonics can be attenuated.

There is one more parameter to choose, the value

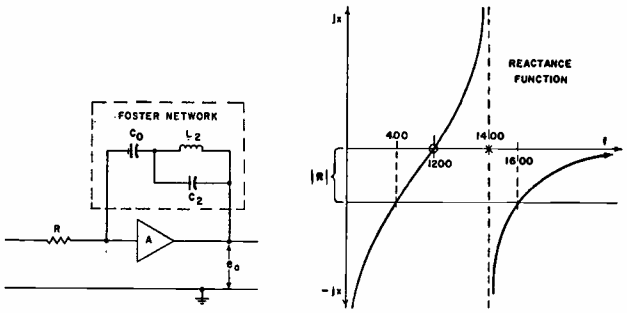


FIG. 2—Foster type feedback network.

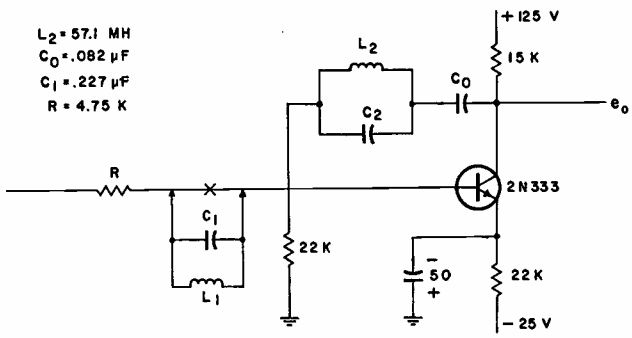


FIG 3—Modified circuit has antiresonant circuit C_1, L_1

of the reactance at any frequency. It is convenient to choose the capacitive reactance at 400 cps to be equal to R, thus getting unity gain.

Since variation in frequency is usually between 360 and 420 cps, the frequency limits for the zero and pole locations must be selected judiciously.

The zero can be made to occur at 1200 cps. The variation in reactance between 1140 and 1260 cps is small, (Fig. 4) and hence a large attenuation is

maintained.

The pole should not occur above about 1400 cps. With these pole and zero locations all the harmonics will be attenuated.

The values of C_o, C_2 and L_2 are as follows: $C_o = 385.13/R$ μf, $C_2 = 1066.54/R$ μf and $L_2 = (12.12)R$ μh.

The circuit is resonant at 1200 cps and antiresonant at 1400 cps.

The circuit in Fig. 2 can be modified as shown in Fig. 3 by the addition of an antiresonant circuit. Its pole can be chosen to occur at any frequency. For example, it can occur at 1200 cps to give more

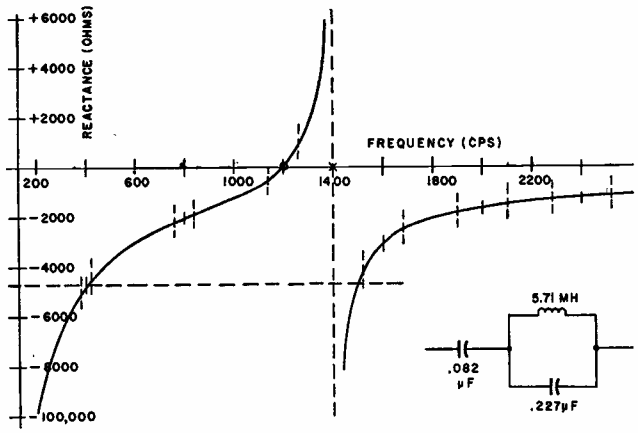


FIG. 4—Network reactance plotted against frequency.

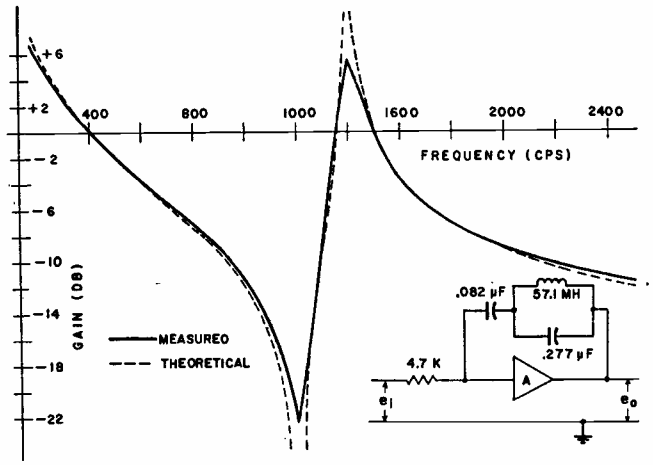


FIG. 5—Theoretical and actual circuit gain.

third harmonic rejection, or it can occur at 1400 cps to eliminate possible amplification of frequencies in the range between 1300 to 1500 cps.

At 400 cps the magnitude of the reactance is made small, so that the phase angle of the impedance formed by R and the reactance of the L_1C_1 combination is small. Otherwise, the phase shift will not be exactly 90 deg.

A single stage transistor amplifier provides adequate gain. Open loop gain varies between 34 db (50 times), using a 2N332 with a beta of 9, to 43.5 db (150 times), using a 2N338 with a beta of 90. A 2N333 is used as a compromise.

The stabilization factor, S, is less than two for this circuit. If only a single supply voltage is available, a voltage divider can be used at the base, returning the emitter resistor to ground. Feedback from the collector should not be used, as it will decrease the open loop gain of the circuit, and the Q of the network.

It should be noted that the output impedance is very low. Since the overall gain at 400 cps is unity, and the open loop gain is fifty or greater, the output impedance is reduced by a factor of 50 or more. Thus, at 400 cps the output impedance is of the order of 300 ohms or less.

The output impedance rises when the network is antiresonant. This is advantageous since frequencies in the 1300 to 1500 cps range will be attenuated by the voltage divider action between the output impedance, and the input impedance of the next stage.

Fig. 5 shows the theoretical amplitude vs. frequency response of the circuit, as well as the actual response.

It is of interest to note that the circuit does not necessarily have to operate with unity gain at 400 cps. If a high beta transistor is used to obtain a large open loop gain, the circuit can provide up to 20 db of voltage gain. The input impedance can be reduced, or the network impedance can be increased as required.

Emitter Follower Transmission Matching

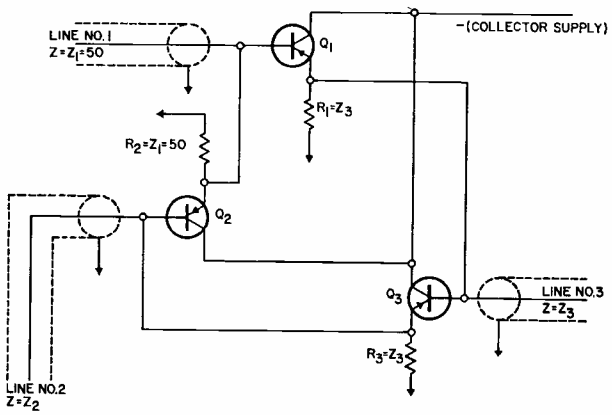
THIS CIRCUIT HAS several desirable features when used as a matching network for transmission lines carrying information in digital form. It is often necessary to connect lines at a junction in such a way that each line is capable of communication with every other line. It may also be desired to mix signal inputs at some distances from their sources to perform an OR operation. Either or both of the above functions can be easily accomplished by the circuit shown.

The basic problem encountered in trying not to impair the signal quality is that the circuitry terminates every line in its characteristic impedance, and has sufficient power gain to drive the input impedance of the remaining lines which appear in shunt.

A circuit which eliminates both of these problems and supplies proper matching of three mutually connected transmission lines without serious amplitude attenuation is shown. The operation of the circuit is as follows: Assume a signal, for example a step function of amplitude −5v, appears on line 1. The base of transistor Q_1 and the emitter transistor of Q_2 are then −5v. The emitter of Q_1 and the base of Q_3 are raised to $-5 + V_{be1} = -4.7$v for germanium. Since the base transistor of Q_3 is connected directly to line 3 the output amplitude of line 3 is −4.7v. The signal impressed across line 2 is that at the emitter of Q_3 which is equal to $-5 + V_{be1} + V_{be3} = -5 + 2V_{be} = -4.4$v. The extension to more imputs is iterative, the maximum num-

ber N, being given by:

$$N = \frac{\text{Input Volt Amp} - \text{Rep. Amp}}{V_{be}}$$



Three transmission lines are matched using emitter follower circuits.

The terminating impedance of line 1 is the emitter resistor of Q_2 in parallel with the input impedance of Q_1. Since the transistors are all operating as emitter followers their input impedances are high ($\beta_x R_e$) and can be neglected when considered in parallel with R_e (the emitter resistors). Thus, each line can be properly terminated by choosing the emitter resistors of the adjacent transistor equal the corresponding line impedance i.e., $R_1 = Z_3$, $R_3 = Z_2$, $R_2 = Z_1$.

Since a signal on any input line produces outputs on all others, the lines are effectively ORed together. Isolation diodes can be inserted at the terminal ends of the lines to prevent received signals from being loaded by driving circuitry if operation in this mode is desired.

The novelty of the circuitry lies in its extreme simplicity. A large number of lines can be mutually connected and properly terminated with a total part count of one transistor and one resistor per line.

Averaging Circuit Has Equal Charge and Discharge Time Constants

IT IS OFTEN REQUIRED to obtain a voltage which is proportional to the mean value of a fluctuating signal averaged over some finite period. If, as is often the case, the *absolute value* of the input signal is to be averaged, either half or full-wave rectification is necessary since positive and negative excursions would otherwise tend to cancel [Ed. note: This is only true when the input signal is symmetrical about the zero axis]. A common application for such signal processing is in an AGC system where an amplitude-modulated sinusoidal carrier is rectified and averaged for use in circuits which vary gain to maintain a fixed average signal level.

A simple circuit which will perform the desired operation is shown in Fig. 1(a). The signal, E_s, from a source having internal impedance R_s, is clipped and averaged by the passive integrator composed of R_1 and C. During a positive input excursion, the capacitor charges through CR_1 with a time constant $T_c = (R_s R_2/[R_s + R_2] + R_1)C$. When E_s goes negative, the diode stops conducting and C discharges with a time constant $T_d = (R_1 + R_2)C$. With $T_c < T_d$ charge is built up, and the output is made unduly sensitive to large signal peaks. The desired condition of equal charge and discharge time constants occurs when $R_2 << R_1$. If, as is often the case, it is unfeasible and/or uneconomical to make R_s small, considerable signal will be lost due to loading. The alternate circuit of Fig. 1(b) exhibits similar time constant inequity.

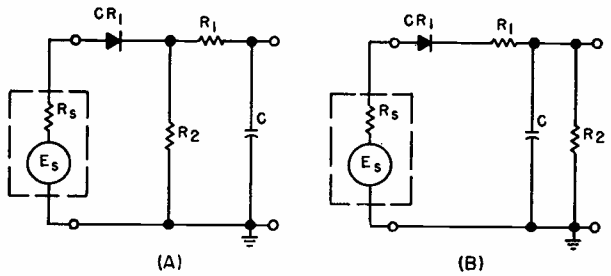


Fig. 1—AGC System

A circuit which provides equal time constants and minimal loading is shown in Fig. 2(a). When E_s is positive, both CR_1 and CR_2 conduct. A drop across R_1 is established which forces E_b to be less than E_a, thus cutting off CR_3 and effectively isolating the capacitor from R_2. The charge time constant is therefore $T_c = (R_s + R_1)C$. If E_s drops to the point where $E_a < E_b$, both CR_1 and CR_2 stop conducting and R_2 is connected across the output through CR_3 which now conducts to provide a discharge time constant, $T_d = R_2C$. The only restrictions on this circuit are that $R_s << R_2$ and E_s be large enough to drive the appropriate diodes out of the high resistance portion of their forward characteristic. If $R_1 = R_2$, the circuit to the right of the generator terminals, neglecting its rectify-

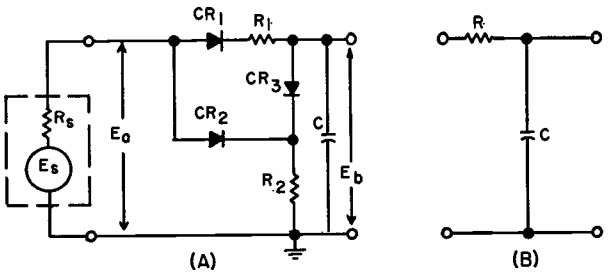


Fig. 2—Circuit with Equal Time Constants

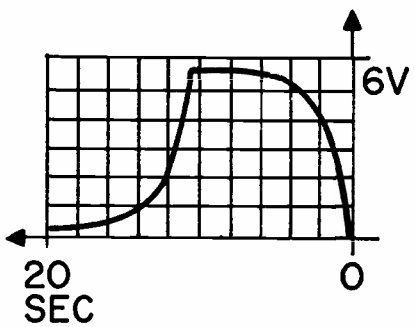


Fig. 3—Output voltage vs Time

ing properties, behaves as the simple *RC* integrator shown in Fig. 2b.

Fig. 3 shows the response when E_s is a 1kc, 14 v rms signal turned on at t=0 and off at t≅11 seconds. The circuit constants are $R_1 = R_2 = 22K$ and C = 60μf.

Combination DC Amplifier, Pulse Operated Relay and Pulse Stretcher

THE TRANSISTOR AMPLIFIER shown in Fig 1 is surprisingly adaptable to a variety of applications. It can be used as a dc amplifier having a current gain of 1000, as an on-off relay or clutch control amplifier, or can be turned on by a 1 μsec. 0.3 ma pulse for either self latching (thryatron like) switching or to produce pulse outputs of predetermined length.

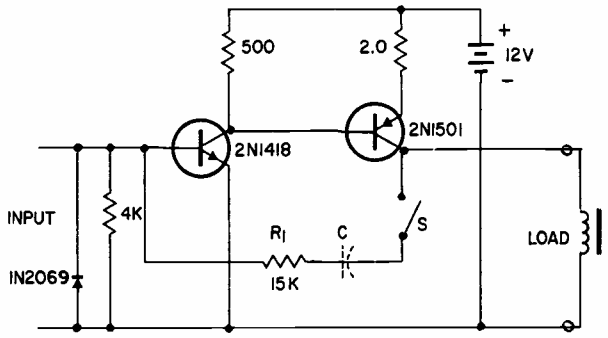


FIG. 1—Universal dc amplifier, pulsed relay, pulse stretcher schematic.

The output can supply 10 v to loads requiring up to 0.5 a. With no signal input the current in the load is only 1 ma. Full output is delivered with 0.3 ma input to the amplifier so that the current gain is nearly 2000 times and the power gain is about 40 db.

The circuit uses a 2N1418 silicon transistor direct coupled to a germanium 2N1501 power transistor. The silicon transistor is used so that the residual load current is less than 10 ma up to 55 C. As an amplifier switch S is left open.

Latching operation is obtained by closing switch S, whereupon the output is triggered by an 0.5 ma 1 μsec. pulse. A pulse output can be secured for each pulse in by connecting a capacitor in series with R_1. The duration of the output pulse is approximately the time constant of R_1 and the associated capacitor, C.

This circuit has proved to be a very useful laboratory tool and a versatile building block in circuit design.

Linear Limiter

A SIMPLE means for reducing impulsive type noise in communications receivers is to use shunt back-to-back diodes as shown in Fig. 1. The standoff voltage of the diodes (1 vpp Si, 0.3 vpp Ge) determines the clipping level. Since the clipping level is fixed, the amount of clipping, relative to the desired signal, is a function of the signal input level. This may be undesirable if the input signal varies. At low signal levels impulsive noise below the gating level is present in the output. At high signal levels (i.e., above gate threshold) the desired signal, as well as the impulsive noise, will be hard clipped. To alleviate this problem the circuit shown in Fig. 2 was designed.

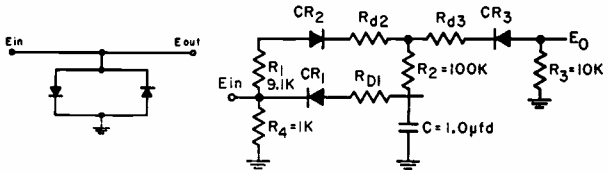


Fig. 1. Common limiter using back-to-back diodes.

Fig. 2. Linear limiter alleviates clipping of the desired signal and impulsive noise.

The input signal is rectified by CR1. The resultant negative voltage is then applied to the cathodes of gating diodes CR2 and CR3. This negative voltage varies with signal input level and supplies variable forward bias to the diodes. The forward bias controls the diodes gate threshold level. As the signal input level varies the gate threshold follows accordingly. Thus the clipping level is now a constant, independent of signal input amplitude. A change in signal amplitude is followed by a corresponding change in gate threshold.

The circuit attack time is R_{D1} C, where R_{D1} (dynamic Diode resistance of CR1), varies as a function of signal input voltage. The attack time should be adjusted such that the rectifier cannot follow the impulsive noise spikes. R_4 is a low impedance shunt and can be left out if the circuit is driven from a direct coupled voltage source.

The currents in CR3 and CR2 should be made equal. This ensures symmetrical clipping on both positive and negative half cycles of the input. (i.e., $R_3 = R_1 + R_4$). To prevent attenuation of the signal entering CR3, R_2 should be $>>R_1$, The circuit decay time is;

$$T_D = \frac{[R_2 + R_{D3} + R_3]\ \ [R_{D2} + R_1 + R_4]\ [C]}{[R_{D2} + R_1 + R_4] + [R_2 + R_{D3} + R_3]}$$

If we assume that the receiver front-end noise is sufficient to provide diode conduction, then

$$(R_{D2} + R_1 + R_4) \,||\, (R_{D3} + R_3) \ll R_2$$

and the circuit decay time reduces to approximately,

$$T_D = R_2\ C$$

Note that the circuit overall decay time would be extremely long if the diodes were not conducting, since the capacitor would have to discharge through the diodes back impedance. The desired amount of limiting is acquired by adjusting R_2 (i.e., controlling the currents in CR2 and CR1).

This circuit can be incorporated within the *age* loop of a receiver, since its output is a linear function of its input. Since this circuit has a built in delay, *agc* time constants are altered accordingly. The circuit as shown in Fig. 2 will limit the input signal −18 ± 2 db from threshold independent of input variations. The circuit was used at 35 Kc but could conceivably be

used at higher frequencies consistent with other design considerations.

Hybrid Balanced Modulator for 100 Kc

THE BALANCED MODULATOR shown in Fig. 1 is essentially a balanced bridge with the carrier injected by Q_1. Balance is maintained by the bias adjustment on V_1 and the balance control. The output is taken across the secondary of the transformer. Modulation is accomplished by unbalancing the bridge in accord with the low frequency input signal. A phase inverter, Q_2, is required so that both V_1 and V_2 will unbalance the bridge in the same direction. The initial balance is the limiting factor in this design since it determines the amount of carrier suppression which can be obtained.

The 6CW4 Nuvistor by RCA was used in the circuit rather than a miniature dual triode because of its exceptional uniformity and ruggedness. It is possible to maintain a carrier null in excess of 60 db below full signal output.

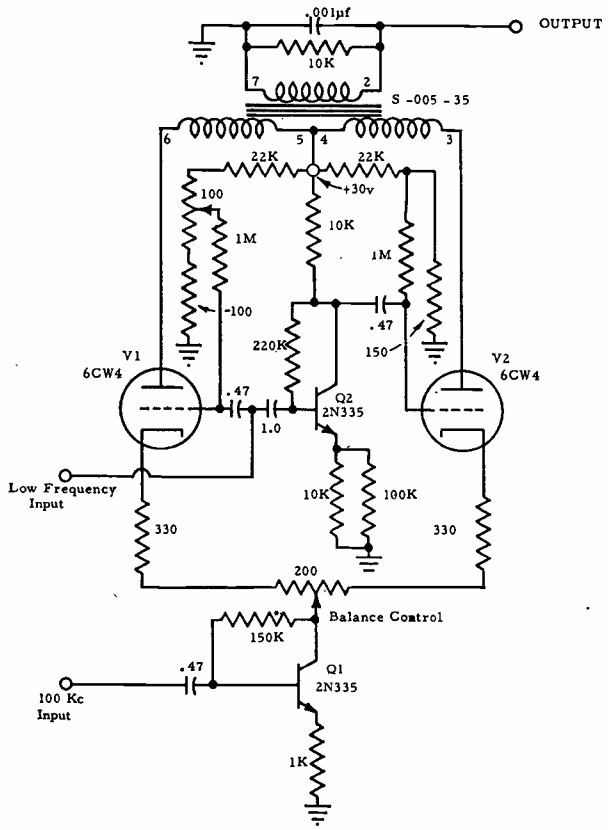


Fig. 1. Hybrid Balanced Modulator for 100 Kc.

DC Input Trigger Circuit

THIS CIRCUIT operates without regard to an input pulse shape (rise time). The input is dc coupled instead of having the usual differentiation circuit. Because of this dc coupling, the circuit can be triggered by sine waves *or* pulses.

Normally Q_1 and Q_2 are conducting with Q_3 cut off. As the input signal goes negative, Q_1 starts to decrease conduction and regeneration occurs. **Output must be taken from Q_3 as shown.**

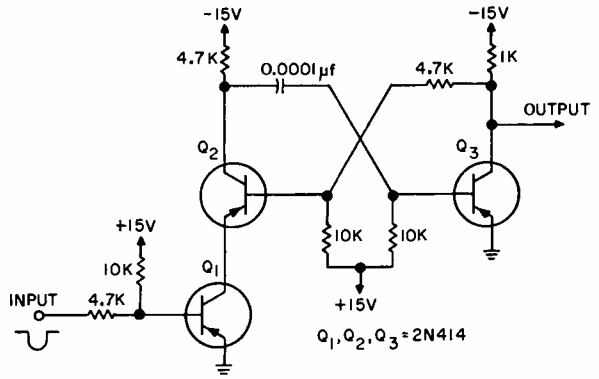


Fig. 1—Circuit for triggering from any-shaped input signal.

Dynamic Range Compressor

THE CIRCUIT of Fig. 1 is a transistorized version of the vacuum tube drawdown limiter or compressor amplifier. It limits the dynamic range of any negative input signal without a threshold or saturation level. The output is approximately proportional to the cube root of the input signal; thus, giving effective dynamic range compression.

The cubic function is generated by a silicon carbide varistor whose output voltage is expressed as $E = KI^{1/3}$. This varistor is the collector load of a transistor amplifier stage that drives the varistor with essentially constant current proportional to the input signal. The varistor voltage in turn, with a large series resistance, appears as a constant current source to the second transistor used as an isolation amplifier. Isolation is required to insure very light loading of the varistor output, for any significant loading would linearize the output.

The circuit as designed is good over the audio range, and is capable of operation in the megacycle region, if used with suitable high frequency transistors and a series inductance to the varistor. Maximum input signal is 200 mv which provides around 3 v of output. Thus the gain at maximum permissible compression is approximately 15. The transfer characteristics E_{out}/E_{in}

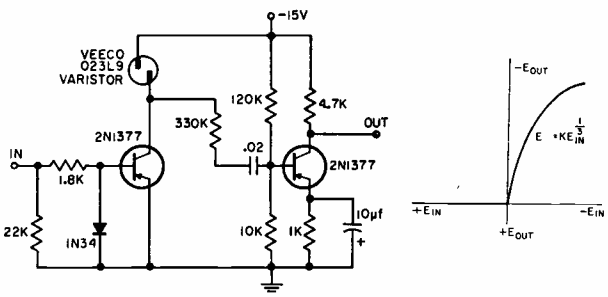


Fig. 1. Dynamic range compressor limits on any negatime imput signal without a saturation level. (left)
Fig. 2. The transfer characteristics E_{out}/E_{in} illustrate cube root proportionality. (right)

are shown in Fig. 2. All positive signals are rejected; those of considerable magnitude are clipped by the base diode to a safe value. All negative signals are amplified in proportion to the cube root of their absolute magnitude. A second limiting action occurs with collector bottoming of the first stage, but this is beyond the intended range of input variation. Input via a voltage divider provides a "drain" path should capacitive input coupling be employed.

Plate-Cathode Follower Wien-Bridge Oscillator

A PLATE-CATHODE follower has low output impedance, good gain stability, wideband response, and low distortion. These characteristics make it useful as a bridge driver for a Wien-bridge oscillator.

The basic arrangement of this oscillator is shown in Fig. 1(A). The frequency determining network, shown in the dotted line, is driven by a pair of plate-cathode followers. If a gain of 2 is given in the second plate-cathode follower, and $C_1 = C_2 = C$, $R_1 = R_2 = R$, the over-all gain of the multiple feedback loop amplifier can be calculated from the flow diagram as shown in Fig. 1(B).

$$G = \frac{\frac{2A}{1 - A\beta_1}}{1 - \frac{2A\beta_2}{1 - A\beta_1}} \qquad (1)$$

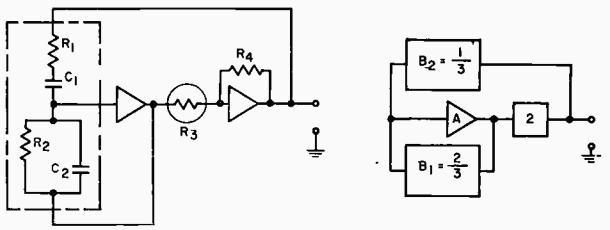


Fig. 1. (A) Basic oscillator arrangement; (B) flow diagram of oscillator in (A).

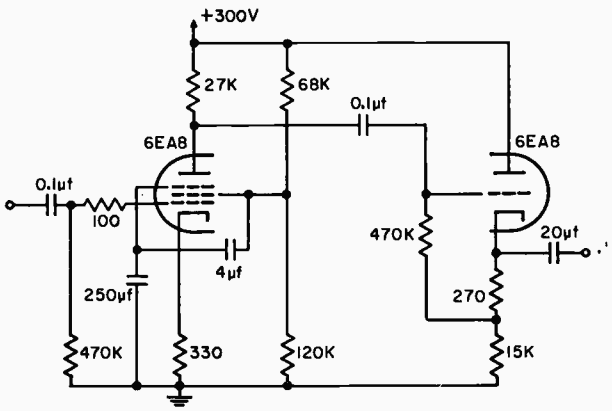


Fig. 2. One of the two identical plate-cathode followers used to drive the Wien-Bridge.

where $\beta_1 = \frac{2}{3}$, and $\beta_2 = \frac{1}{3}$ with no phase shift at frequency $\omega = 1/RC$.

If $A\beta_1 >> 1$, Eq. (1) becomes

$$G = \frac{3}{1 - 3 \times \frac{1}{3}} = \frac{3}{0} \qquad (2)$$

From Eq. (2), the gain is infinite; the amplifier becomes an oscillator at a frequency given by $f = 1/2\pi RC$.

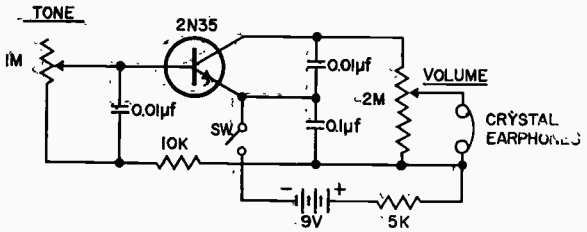
A simple, easy-to-build, and low cost plate-cathode follower, having a relatively large forward loop gain, is shown in Fig. 2.

The chief advantages of this oscillator are that the amplitude and frequency stabilities are insensitive to power-supply variations, and tube aging and replacement.

A Chatter Jammer Circuit

SOONER OR LATER, an engineer learns to live with the sounds of machinery and typewriters in the shop and in the office, but trying to concentrate on a problem while others are conducting a conversation nearby, creates an almost impossible situation. There is a solution.

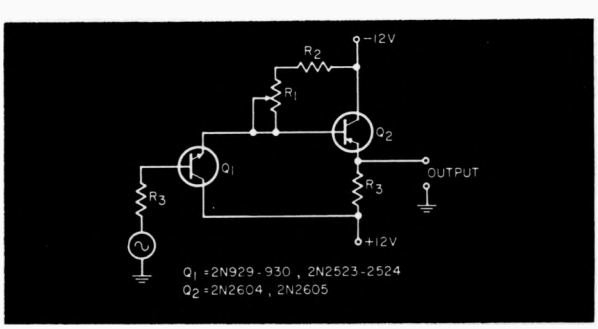
A transistorized audio oscillator, connected to a pair of crystal earplugs, helps you to concentrate. Simply adjust the oscillator to deliver a tone pleasing to your ear and set the gain or output control to a level that drowns out the ambient noises.



Chatter jammer circuit.

Complementary Emitter Follower Offers High Isolation

THE APPEARANCE of very high gain complementary planar transistors now makes possible a dc-to-several-mc emitter follower with no offset voltage, good accuracy, and exceptional isolation. The close tracking of V_{be} with temperature and the low leakage current provide excellent temperature stability.



High-isolation complementary emitter follower.

In the figure, if R_3 is 10 K and R_1 about 1 meg, then the dc input impedance is (for $\beta_1 = 100$, $\beta_2 = 200$) about 66 meg. As long as the output voltage is not limited by the current available (through R_3) the output impedance is $Z_o = R_s \beta_1\beta_2$. For example, if $R_s = 50$ meg, then $Z_o = 2$ K. If much lower output impedances are needed, R_3 can be made 1 K and R_1 about 100 K. With Z_{in} about 6.6 meg, the output impedance, until limiting, will still be $R_s/\beta_1\beta_2$. However, more current is available to drive the load, and the values of β_1 and β_2 are higher.

Laboratory measurements for accuracy and stability are:

input, 0-10 volts; accuracy, 1%

$R_s = 2.5$ K $\quad \Delta T = 60°C \quad \Delta V_o = 0$ v

$R_s = 100$ K $\quad \Delta T = 60°C \quad \Delta V_o = 10$ mv.

The npn is used as the input stage since the leakage current is an order of magnitude lower than the pnp. The change in leakage current through R_s produces most of the error in output voltage due to changes in temperature. ◆◆

FM Limiter

THE LIMITER circuit described has markedly improved noise (a.m.) rejection over conventional limiters used in fm broadcast receivers. Conventional limiters require careful compromises in the grid circuit time constants and resonant circuits. The impulse noise rejection, except in extravagant designs with four i.f. stages and three limiters, is less than perfect and very sensitive to mistuning of the discriminator and i.f. transformers. Many otherwise satisfactory receivers evidence this by the putt-putt of auto ignition, even when tuned to stations of sufficient signal strength to saturate the limiters.

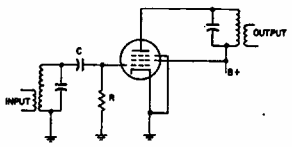


FIG. 1 —Conventional limiter.

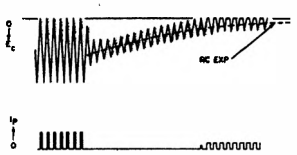


FIG. 2 — Conventional limiter E_c, I_p relationship demonstrates degradation of limiting action caused by grid circuit time constant.

The conventional type of limiter is shown in Fig. 1, and Fig. 2 is a simplified explanation of its behavior under a sudden decrease in carrier voltage. Note that there is a complete drop-out of plate current for a period determined by the grid circuit time constant *RC*, that the fundamental component of the plate current has probably decreased in amplitude, and that the effective damping on the grid tank circuit has undoubtedly changed. The net effect more nearly resembles that of an agc circuit with its unavoidable recovery time than that of a dynamic, or instantaneous limiter. A good procedure for optimizing this circuit is given in the *Radiotron Designer's Handbook*, but what is obviously needed is a different circuit.

The improved limiter circuit, Fig. 3, does not remove all of the difficulties, but represents a significant improvement at little added cost. The pentode is a conventional short time-constant first limiter. The second limiter operates in the same fashion as the familiar vtvm circuit, that is by cutting off one triode or the other. Since limiting is not dependent on grid current and there is no coupling capacitor, recovery from rapid changes in carrier level or noise spikes is virtually instantaneous. The 20 μh coil resonates the interstage capacity at 10.7 mc and the 12 K resistor provides damping as well as a dc return for the right-hand grid.

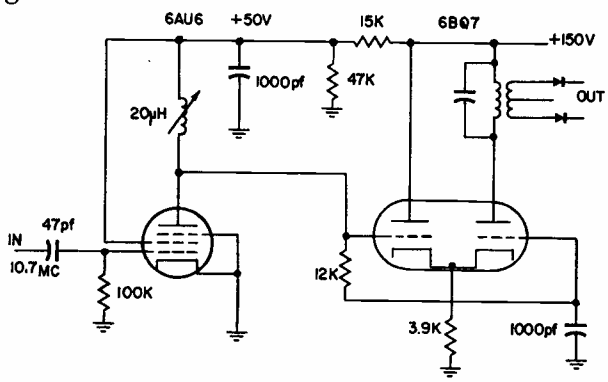


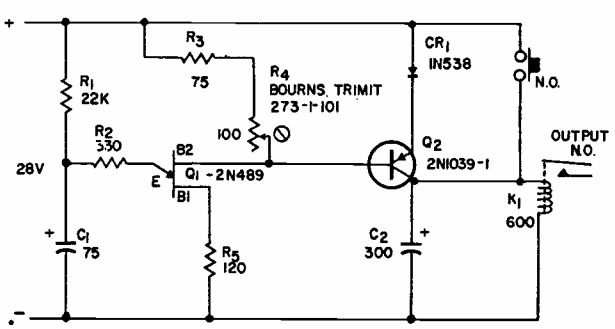
FIG. 3—Improved limiter.

An a.m. rejection test disclosed results startling to those familiar with fm broadcast receivers. A 10 mv signal modulated 40% at 400 cps applied to the input produced no measurable 400 cps output from the detector. The author's customary i.f. alignment technique, using an a.m. signal with the discriminator slightly mistuned, failed completely because of the sharp threshold and near complete removal of a.m.

Low Frequency Switching Circuit

THIS PRACTICAL design was conceived to test the regulation of manufactured power supplies with factory checkout equipment. It is now used in several equipments for various purposes.

The original requirement was to supply dc power to the input of a power supply under test which



Change of dc input to power supply is accomplished by this low-frequency switching circuit. Adjust R_4 for best symmetrical waveform at relay contacts (time on-time off).

would abruptly change in amplitude level (square wave) approximately 10 volts (adjustable) periodically at a rate of 0.5 to 1 cycle per second.

The dc input to the power supply under test is connected in series with the relay contacts (output terminals) with a rheostat connected across the relay contacts. When the relay contacts close, the rheostat is shorted out, which increases the voltage and then the relay contacts open and drop the voltage.

The circuit shown consists of a relaxation oscillator using a unijunction transistor driving a pnp power transistor which actuates a power relay.

The timing circuit R_1 and C_1 periodically fires the unijunction transistor Q_1 which causes Q_2 to conduct and charge C_2 and actuate the 600-ohm relay. The relay coil requires about 12 volts to pull in but will release at about 6 volts. As the actuating voltage is almost a spike, the capacitor tends to keep the relay holding for a longer period which equalizes the on-off time. Q_2 is at cut off at off time. CR_1 minimizes I_{CBO} which could cause thermal runaway at a higher temperature. CR_1 should be mounted on a heat sink. The push-button switch allows the relay to be actuated and held for external circuit adjustments.

Simple Wailing Siren Circuit

MOST SCHEMES for transistorized sirens employ three subcircuits: a voltage-controlled oscillator, a low-frequency oscillator for modulation, and a power amplifier to drive the loudspeaker. The circuit may be simplified, however, by allowing the controlled oscillator to double as the power amplifier, thereby saving the cost of the amplifier components.

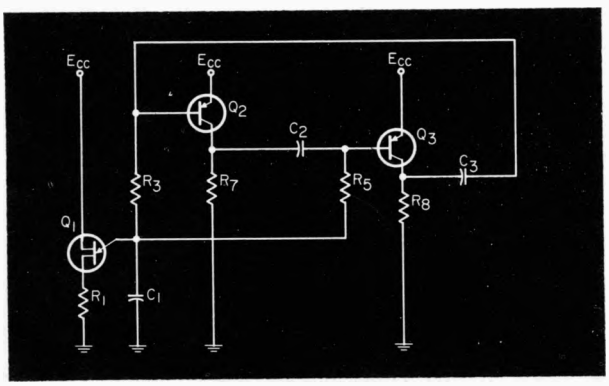


Fig. 1. Basic astable multivibrator circuit.

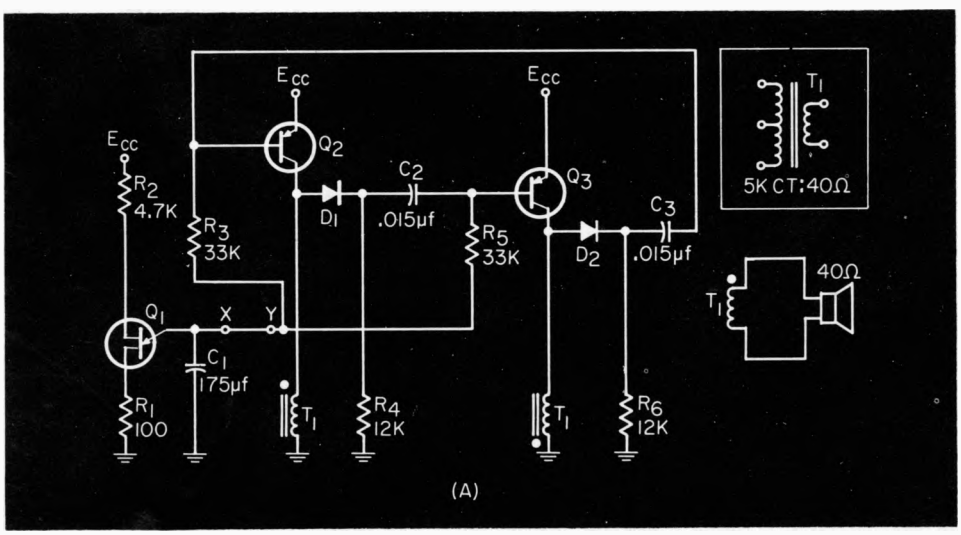
The basic circuit is an astable multivibrator (Fig. 1). The frequency of the oscillator is varied by controlling the voltage to which the timing capacitors discharge during the timing rundown. The base-drive resistors (R_3, R_5) charge the capacitor C_1 and thus vary the control voltage exponentially. C_1 is discharged periodically by the unijunction Q_1, which resets the oscillator to the beginning of its frequency sweep.

The only precaution to be observed in this design is that the base-drive resistors must be small enough to saturate the transistors when the control voltage is at its maximum value (ηE_{cc}), and that they are not so small that they supply a current to the emitter of Q_1 greater than valley current.

To use the oscillator as the power driver, the collector load resistors are replaced by a center-tapped driver transformer (Fig. 2). The additional resistors R_4 and R_6 and the diodes D_1 and D_2 are used to decouple the undriven side of the transformer from the timing capacitors during the capacitor recovery. Note that the transformer is being driven push-pull by the alternately saturated transistors.

The circuit as shown in Fig. 2 can be mounted in a minibox. With the circuit values shown, the circuit draws 10 mA from a 9-V battery. The base-2 resistor R_2 is incorporated in the circuit to decrease the peak power surges during the unijunction firing time; this greatly increases battery life.

The addition of a single transistor or Darlington equivalent Q_4, as shown in Fig. 2b, allows the power capabilities to be increased by approximately the beta of Q_4.



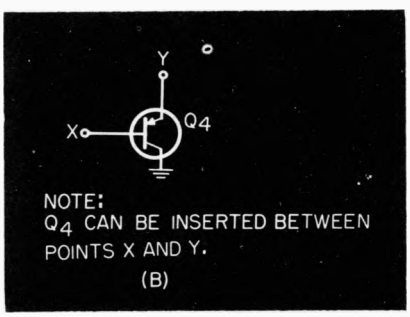


Fig. 2. Oscillator doubles as power driver with extra driver transformer. Power capabilities can be increased by adding transistor as shown in 2b.

Modified Emitter Follower Has No Offset

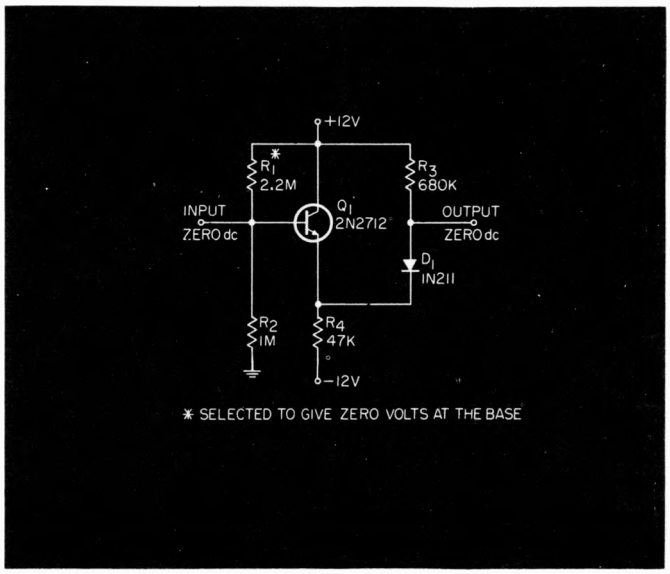
FOR MOST emitter-follower applications, such as impedance matching of ac signals, dc offset is unimportant, so the conventional circuit is adequate. The simple modification shown here gives a more versatile emitter follower, suitable for dc as well as ac applications. This modification eliminates the inherent difference between output and input dc levels caused by V_{BE} of the transistor. A further advantage of the modified circuit is that it's less sensitive to temperature variations.

Diode D_1 is selected to match the V_{BE} of the transistor. Thus a silicon diode is used with a silicon transistor, and germanium with germanium. In order to achieve a high input impedance and to correct for errors due to base current and leakage current, the base of the transistor is biased by a resistive divider. (For low input impedances, a simple resistor to ground may be adequate.) The ratio of the divider network is adjusted to give zero volts at the base.

Making the value of R_3 equal to the parallel combination of R_1 and R_2, i.e.

$$R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

minimizes drift due to variations in power-supply voltage.



Modified emitter follower has equal dc levels at input and output. Offset due to V_{BE} is eliminated by diode D_1.

Radiation Meter Uses MOS FET

THIS CIRCUIT uses a MOS FET to replace the electrometer tube normally used in radiation-survey meters. The MOS device achieves the minimum input-impedance of 10^{13} ohms needed in this application.

The all solid-state circuit has several advantages compared with the tube approach. There is no warm-up time, weight and cost are reduced, and battery life is extended.

In the circuit shown here, radiation strikes the ion chamber, forming ions. Current flows in R_1, and the voltage across this resistor drives the gate voltage of Q_1 less negative. This reduces the drain voltage and causes a change in collector voltage of junction transistor Q_2.

As the collectors of the differential - amplifier transistors Q_2 and Q_3 are initially at the same voltage, the difference in collector voltages is proportional to the rate of incident radiation striking the ion chamber.

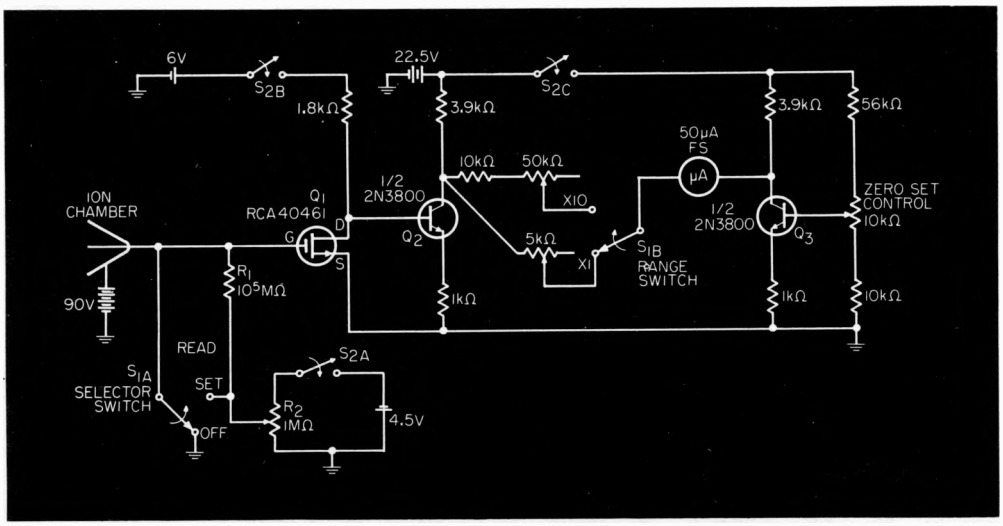
The selector switch has three positions: "off," "zero set," and "read." Initially this switch is in the "off" position, the gate of the MOS transistor is grounded and all batteries are disconnected. Note that though S_1 and S_2 have been shown as separate switches for clarity, in practice they can be ganged in one assembly.

When S_1 is switched to the "zero set" position, this removes the gate ground, shorts R_1 and switches the batteries into the circuit. Also the meter is switched to the "×10" scale. The "zero set" position allows the instrument to be zeroed in an external radiation field.

When S_1 is switched to the "read" position, this removes the short across R_1 and leaves the ammeter on the "×10" scale. (If the switches are ganged, a second "read" position is provided for "×1.")

The preset potentiometer R_2 serves two purposes. First, it adjusts the gate bias to give maximum range of linearity on the transfer characteristic of Q_1. Secondly, it adjusts the gate bias for any gross variations in transistor parameters.

With the component values shown and the ion chamber used, the two full-scale ranges were 500 milliroentgens/hr (×10) and 50 mR/hr (×1).



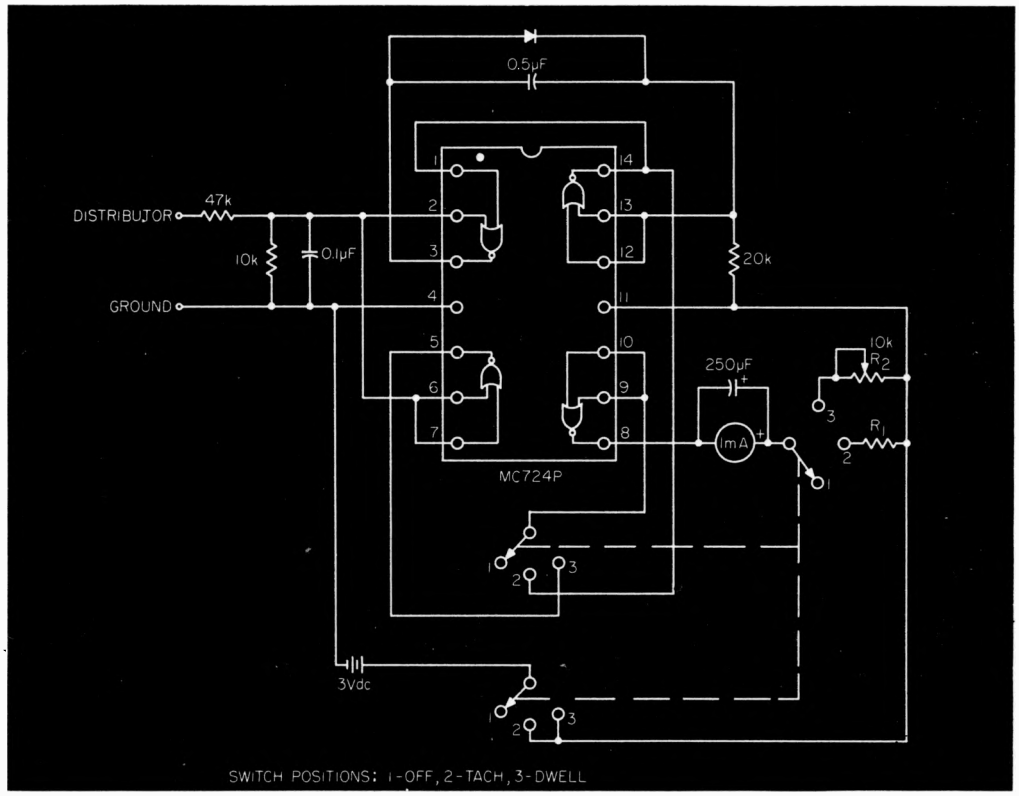
Solid-state radiation-survey meter uses MOS FET to give high input impedance.

Combined Tachometer and Dwell Meter

USING ONLY ONE IC, plus a 1-mA meter and a few discrete components, you can build a compact portable instrument that measures both engine speed and distributor dwell angle of automobiles.

In the circuit shown, the top two gates of the IC are connected as a one-shot trigger circuit. The 20-kΩ resistor and the 0.5 μF capacitor are the timing elements. The output of the one-shot (pins 1 and 14) goes to position 2 of the selector switch. This position is used for tachometer measurements. With the switch in this position the one-shot output connects to pins 9 and 10 of the IC. This IC gate functions as an amplifier and its output (pin 8) goes to the meter. The large capacitor across the meter, integrates the pulses to give a steady reading. Because the pulses are of fixed amplitude and duration determined by the characteristics of the IC one-shot, the meter reading is proportional to pulse frequency and therefore engine speed. For dwell-angle measurements, the remaining gate of the IC is used as an inverter. With the switch in position 3, the inverter output (pin 5) connects to the output gate (pins 9 and 10) to give a second inversion. The output pulses (pin 8) are then integrated, as before, to give a steady meter reading.

Note that the one-shot is not used for dwell-angle measurements. Therefore, though the pulse amplitude is fixed by the characteristics of the IC gate, the pulse duration varies with the dwell angle of the distributor cam. The meter actually reads the ratio of the time the points are closed, compared to the time they are open. The full scale reading of the meter represents the angular distance between lobes on the distributor cam shaft. This angle is 45° for an eight-cylinder engine, 60° for a six, and 90° for a four. So the meter can be calibrated in degrees of dwell, for any type of engine.



Simple meter circuit measures both engine speed and distributor dwell angle of automobiles.

Resistors R_1 and R_2 determine the full scale indication of the meter. To calibrate the dwell scale, set the selector to position 3 and adjust R_2 for a full-scale meter indication with the input leads shorted.

To adjust the tach calibration select a suitable value for R_1, to give full-scale indication with the selector switch in position 2 and with an input pulse-repetition frequency of 66.67 Hz. This frequency corresponds to speed of 1000 rpm for an eight-cylinder engine. For other engines, the oscillator frequency can be determined from: $F=$

$$\frac{(\text{RPM} \times (\text{No. of cylinders})}{120}$$

hertz.

For other full-scale calibrations or for different engine types, the 20-kΩ timing resistor must be changed together with R_1.

SCRs simplify monostable coil-driver

THE HIGH-PEAK currents needed to drive most print-hammer solenoids and punch-actuator coils can be delivered by the circuit shown in Fig. 1. Provided the external load and the energy-storage capacitor C_1 together constitute an "underdamped" tuned circuit, the capacitor delivers constant-energy pulses to the load.

Basically, the complete circuit is an SCR delay flop (monostable multivibrator). This SCR circuit offers the following advantages versus transistor circuits:

- The inherently high gain of SCRs (> 5000) eliminates the extra transistor stages that would be needed to drive an actuator coil from a logic-level pulse. So the SCR circuit is simpler, cheaper and more reliable.
- The voltage and current levels (170 V at 5 A), needed to drive the actuator coil, would be difficult to achieve with transistors except at prohibitively high cost.
- The inherent "automatic reset" feature of the delay-flop circuit eliminates the need for additional circuitry to generate a "reset" pulse.

Compared with a conventional "ring-off" circuit using a single SCR, the dual-SCR circuit can give much higher repetition rates (>100 pulses/second). For example, with the single SCR circuit and with the values shown for coil

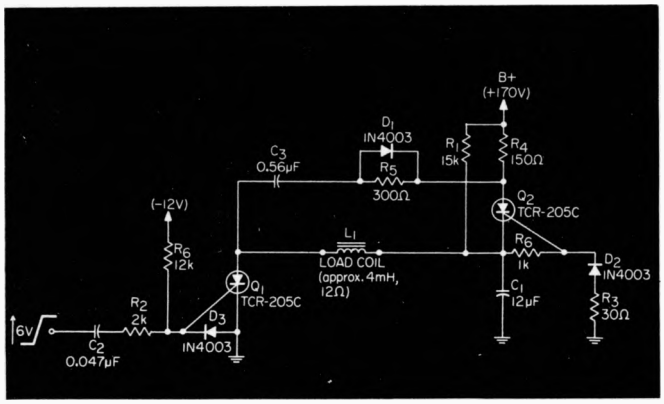


Fig. 1. Dual SCR delay flop drives print-hammer and punch actuator coils. This circuit is faster than a single SCR "ring-off" circuit and much cheaper than transistor circuits.

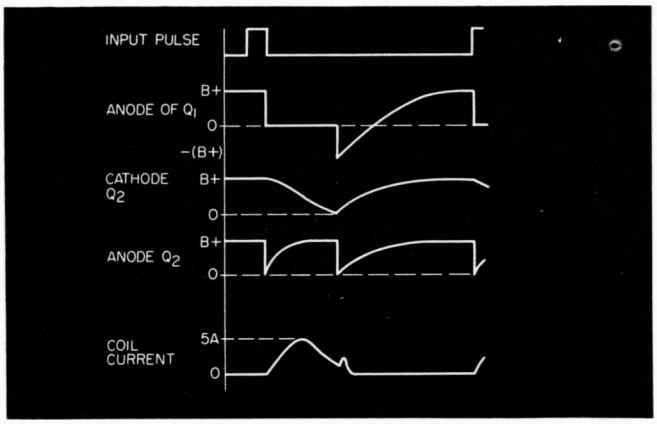


Fig. 2. Typical waveforms for the delay-flop circuit of Fig. 1.

inductance and resistance, the minimum impedance that could be placed between the power supply and storage capacitor would be 4 kΩ. This impedance would limit the repetition rate to a maximum of 4 pulses/second.

The dual-SCR delay flop of Fig. 1 works as follows. When power is initially applied, the energy-storage capacitor C_1 charges to $B+$ through resistor R_1. Application of a positive-going trigger pulse turns on Q_1. This causes C_1 to discharge through the actuator coil, thus energizing the coil. Due to the Q of the load circuit (L_1, C_1) the voltage at the cathode of Q_2 "rings" in a negative-going direction. This causes gate current to be supplied to Q_2 through R_3, thus turning on Q_2. As Q_2 turns on it commutates a negative pulse to Q_1 anode, thus turning off Q_1. Energy-storage capacitor C_1 now starts to charge toward $B+$ with a time constant determined by the values of R_4 and C_1.

When the capacitor has charged to the full B+ voltage, Q_2 may or may not turn off, depending on the value of its hold current and the leakage through C_1. But. when another input pulse occurs. Q_1 will turn on as before and will commutate a negative pulse to the anode of Q_2, turning it off. When Q_2 is turned off, the load circuit is isolated from the $B+$ by the resistance R_1.

Resistor R_2 limits the instantaneous current flowing into the gate of Q_2. Resistor R_5 may not be required in all applications. Its function is to overdamp the tank circuit (C_1, L_1), thus preventing Q_2 from ringing itself off. Diode D_1 shunts the effect of R_5 during Q_1 turnoff. D_2 prevents cathode-to-gate breakdown when the cathode of Q_2 is at $B+$.

The values used for $B+$ and C_1 depend on the application. As previously described, the capacitance of the energy-storage capacitor is determined by the inductance and Q of the print-hammer coil. The $B+$ voltage is then chosen to supply the correct amount of energy ($\frac{1}{2}\ CV^2$) *to* L_1, for proper operation of the print hammer.

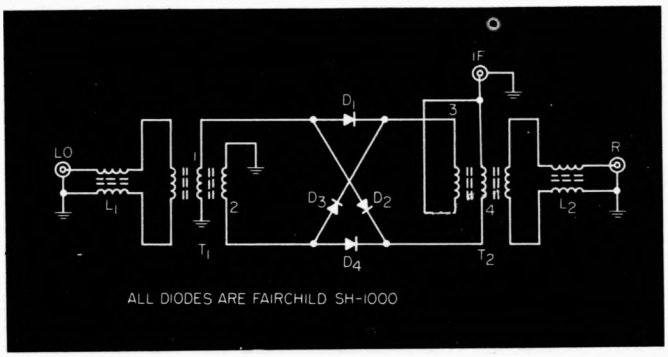
Double-Balanced Diode Mixer

THIS DIODE mixer gives fine performance in the frequency range 2 MHz to 500 MHz, with low conversion loss over the entire bandwidth. Ferrite-bead transformers in the two input ports, ensure good mixer balance at the operating frequencies.

The circuit works as follows: Voltages appearing at points 1 and 2 of transformer T_1, cause diode pairs D_1D_2 or D_3D_4 to conduct, depending on signal polarity. Alternate conduction of these diode pairs causes the ends (3 and 4) of T_2 to switch to ground potential at a rate equal to the frequency at the *LO* port. Output voltage at the *IF* port is determined by the instantaneous voltage appearing across T_2 secondary (3 to 4). I-f output also depends on which end of the secondary is at ground potential at a given instant. Thus the output frequencies appearing at the *IF* port are the frequencies applied to the *R* and *LO* ports, plus their sum and difference.

The mixer should be constructed, using good rf layout techniques. Excessive lead length, from transformers to diodes and input connectors, will increase conversion loss by as much as 3 dB at 500 MHz. All ground return leads should be short.

Transformers T_1 and T_2 are identical, except that the center top of T_2 secondary is connected to the *IF* port, instead of to ground as for T_1. The transformers are wound on a common ferrite bead using 50—Ω bifilar wire, with a third wire twisted around the bifilar pair. This third wire is two to three times longer than the bifilar winding. Thus the three wires form a trifilar winding. The two ends of the long wire are brought together and wound on a separate ferrite bead to form coils L_1 and L_2. These inductors keep the ends of T_1 and T_2 balanced with respect to ground, thus improving mixer



Double-balanced mixer uses hot-carrier diodes. Inductors L_1 and L_2 balance the transformers primaries with respect to ground.

balance. The coils have two turns each and the transformers both have four turns. All windings are 36-AWG wire.

The best way to align the circuit is to adjust the positions of the secondary windings of T_1 and T_2 while measuring conversion loss. In this way you can find the condition of maximum coupling between primary and secondary. The mixer derives its operating power from the local oscillator, so the LO power must be around 3-5 mW for best performance. This level can be optimized during alignment to give the best compromise between conversion loss and noise figure.

Typical performance figures for an experimental mixer using this circuit, are as follows:

- Frequency Range: 2 MHz to 500 MHz (R and LO), and dc to 500 MHz (i-f).
- Conversion Loss: –7 dB to 500 MHz (i-f = 100 MHz).
- Mixer Balance: —35 dB to 500 MHz (LO power at R) and —30 dB to 500 MHz (LO power at i-f).
- Single-Side-Band Noise Figure: 8 dB to 500 MHz.

All measurements made with 10-dB 50—Ω pad on each port.

Improved absolute-value circuit

OTHER CIRCUIT designers have described[1, 2, 3] simple circuits whose output is equal to the absolute value of the input voltage. But all these circuits have the disadvantage that they need several pairs of resistors that are matched to close tolerances. Fortunately, it is possible to design improved absolute-value circuits that achieve high accuracy, yet which need only a single pair of matched resistors.

Let's look first at the conventional circuit shown in Fig. 1. Both operational amplifiers function as inverters. With a negative input voltage, the right-hand amplifier multiplies e by -1, while the left-hand amplifier contributes nothing to the output. With a positive input voltage, both amplifiers invert the signal and the output is $2e_x - e_x = e_x$. The output is therefore positive for either positive or negative input signals — thus realizing the required absolute value $|e_x|$. For proper circuit operation, the following must be true:

$$R_4/R_3 = 1.000$$
$$R_1/R_0 = 1.000$$
$$R_2/R_0 = 0.500$$

The accuracy of these ratios determines the accuracy of the absolute value $|e_x|$. But, for a precision circuit, it is difficult and expensive to match resistors to the required close tolerances.

Figure 2 shows an improved circuit which requires only one pair of matched resistors (R_1 and R_2). With positive input signals, the output of A_1 attempts to go negative while the output of A_2 goes positive. Diode D_2 is therefore back-biased. Diode D_1 prevents A_1 from saturating in the negative direction; thus it speeds circuit operation when the polarity of the input signal changes.

With negative input signals, the output of A_2 attempts to go negative while the output of A_1 goes positive. Diode D_4 therefore becomes back-biased. Diode D_3 serves the same purpose for negative inputs as D_1 serves for positive inputs. Though type 1N914 diodes are indicated in the schematic, any general-purpose silicon type is suitable.

Note that, in the improved circuit, A_1 acts as an inverter while A_2 is a voltage follower. This contrasts with the conventional circuit in which both amplifiers are inverters.

The circuit of Fig. 2 has been tested using 709-style op amps. With these amplifiers compensated so that their upper 3-dB frequency is 10 kilohertz, the absolute-value circuit works well with input frequencies up to 1 kilohertz. This bandwidth was adequate for the original application (an A/D converter system).

Bandwidth of the amplifiers should be several times greater than the highest sinusoidal frequency of interest — this is necessary because high-frequency components generated within the absolute-value circuit must be accommodated to preserve the circuit's accuracy. Ideally, the bandwidth of the op amps should be at least ten times greater than the bandwidth of the input signal.

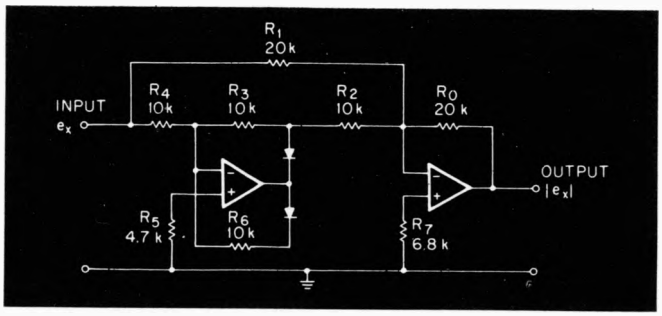


Fig. 1. This widely used absolute-value circuit has the disadvantage that many of the resistors must be accurately matched.

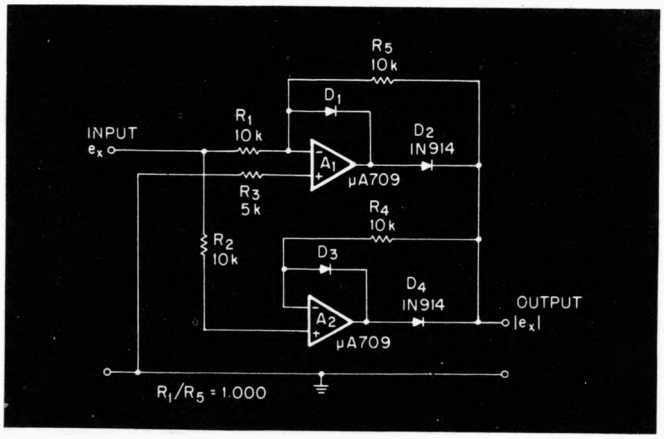


Fig. 2. In this improved circuit only one pair of resistors (R_1 and R_5) is critical.

May have typo error: References to R1, R8 and Rs probably should be R1 and R5 (as Fig 2)

References

1. "Handbook of Operational Amplifier Applications," *Burr-Brown Research Corp*, 1963, p.73.
2. J. N. Giles, "Linear Integrated Circuits Applications Handbook," *Fairchild Semiconductor*, 1967, p.150.
3. "Applications Manual for Operational Amplifiers," *Philbrick/Nexus Research*, 2nd edition 1966, p.59.

Phase indicator for ac tachometer

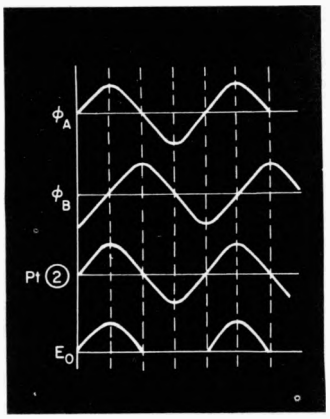


Fig. 1. Phase relationships of tacho output signals and corresponding outputs from the circuit of Fig. 2.

THE OUTPUT of an ac tachometer is a two-phase voltage with either a 90-degree lead or a 90-degree lag between phases as shown in Fig 1. Phase relationship of the output signals depends on rotation direction of the tacho. The circuit shown in Fig. 2 detects signal phase and can therefore indicate the direction of rotation.

The circuit works as follows: Capacitor C_1 together with input impedance Z_{in} shifts phase ϕ_B by 90 degrees. Transistor Q_1 amplifies the ac signal so that voltages at points 1 and 2 are approximately equal. The quiescent voltage for point 2 is set at zero. This results in points 1 and 2 having voltages that are either in phase or 180 degrees out of phase, depending on the tachometer's direction of rotation.

Point 3 always assumes the lowest possible potential so that when 1 and 2 are 180 degrees out of phase and 1 is positive, point 3 will follow point 2 for a half cycle, and follow point 1 for the remaining half cycle. Because the output of D_1 is negative, diode D_2 does not conduct and there is no output.

When the tacho rotation is such that points 1 and 2 are in phase, D_1 will conduct and point 3 will follow point 2 for the entire cycle. So the unfiltered output voltage from D_2 consists of half-wave rectified ac.

Thus the circuit can be used with a peak detector and suitable threshold circuit to provide a pair of discrete logic levels that indicate rotation direction of the tachometer. ■

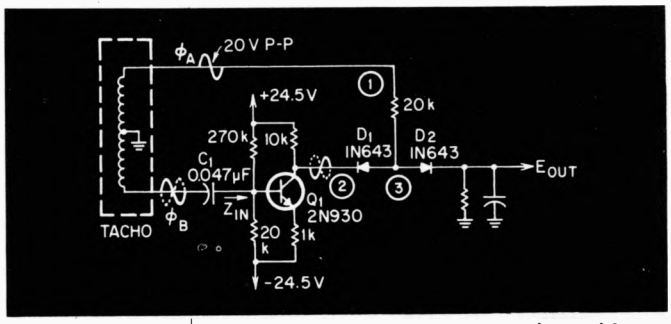


Fig. 2. Simple circuit to detect direction of rotation with ac tacho.

Linear modulator has excellent temperature stability

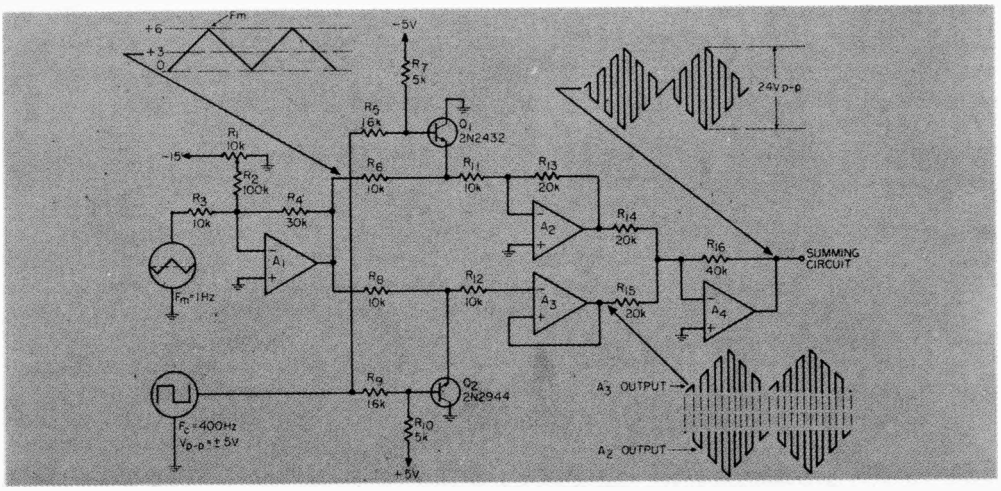
THIS CIRCUIT provides a precise degree of linear amplitude modulation. With the specified transistors, and with low tempco resistors, modulation errors due to temperature variation can be neglected.

In the schematic, components have been chosen for audio-frequency operation. Carrier frequency f_c is 400 Hz and modulation frequency f_m is 1 Hz. However, the same basic circuit can be used for frequencies from zero up to several megahertz. Note that there are no capacitors. Bandwidth is determined primarily by the characteristics of the ICs. Use of closed-loop op amps and chopper transistors gives stable gain, unaffected by temperature.

The modulation signal, at the output of op amp A_1, rides on a positive dc potential as shown in the schematic. Potentiometer R_1 adjusts the dc level. At A_1 output, the signal never goes below ground potential except when over modulation occurs. Chopper transistors Q_1 and Q_2 alternately sample A_1's output waveform at the carrier-frequency rate f_c.

Op amp A_2 inverts the incoming signal, and A_3 provides a noninverted signal. The output signals of both amplifiers are summed at one input terminal of A_4. When A_2 conducts, A_3 is off, and vice versa. Thus the modulated-carrier wave at the output of A_4 is a series of alternating positive and negative pulses, with amplitude determined by the modulating signal. Full 100-percent modulation occurs when the peak of the modulating wave is equal to the dc quiescent level at the output of A_1.

Any temperature drift is likely to be caused by the resistors rather than by the op amps and transistors. Op-amp gains are stabilized by feedback, and V_{sat} for the switching transistors changes less than 0.2 μV/°C. So, low-tempco resistors should be used for optimum temperature performance.



Circuit provides accurate amplitude modulation that isn't temperature dependent. Pot R_1 adjusts quiescent level of the modulating signal.

Pulse-height modulator multiplies voltage by frequency

See added appendix for better image

WITH A FEW extra components, a single op-amp one-shot multivibrator can be used as a pulse-height modulator. The modulator is useful as an analog multiplier in process-control circuits. If we trigger the one-shot with a continuous train of input pulses, and if we simultaneously control the output-pulse height with a dc input voltage, then the mean voltage of the output pulses will be proportional to the product of input frequency and dc control voltage.

In Fig. 1, we can see more clearly how the proportionality occurs. The input pulse train, with repetition frequency f and period T, triggers the one-shot to give output pulses that have the same period T. Pulse height is exactly equal to the control voltage V_c. Because V_m is the mean output voltage,

$$V_c T_1 = T V_m \qquad (1)$$

(Where T_1 is the output pulse width).

But $T = 1/f$, therefore,

$$V_m = T_1 V_c f \qquad (2)$$

Also, in a well-designed one-shot, we can ensure that T_1 is determined solely by the RC time constant and is unaffected by variations in input amplitude or frequency. Then,

$$V_m = kV_c f \qquad (3)$$

Figure 2 shows a practical schematic for a complete pulse-height modulator. The circuit handles input frequencies from 1 Hz to 1 kHz, and control voltages from 0.1 to 15 V. Multiplication accuracy is around 0.1% (referred to maximum input frequency and control voltage).

The circuit works as follows: The leading edge of a positive-going input pulse triggers the one-shot into its astable state. Point A is driven to a more-positive potential than point B. So the output voltage of A_1 drops to its extreme negative value, thus turning off Q_1. With Q_1 cut off, the voltage at point M approaches V_c, giving a voltage $V_c/2$ at point A. The voltage at point B then starts to change exponentially at a rate determined by time-constant R_3C_1. As soon as the voltages at A and B are again equal, the circuit switches back to its stable state.

Note that the time taken for point B to change to the level of point A doesn't depend on V_c. This is because elements R_1, R_2, R_3 and C_1 constitute a bridge network, the balance conditions of which are independent of V_c. Time-constant R_3C_1 alone determines the recovery time of the one-shot. For this circuit T_1 is 0.4 ms.

Capacitor C_1 discharges through the parallel combination of D_1 and R_3, and through Q_1. In practice, the accuracy of the one-shot's recovery time depends partly on the minimum voltage to which C_1 can be discharged. So, Q_1 must have a low saturation voltage V_{CE}. Magnitude of V_{CE} directly influences the multiplier accuracy, as shown in the following equation:

$$V_m = T_1 V_c f + V_{CE} \qquad (4)$$

The European transistor, specified for Q_1, can be replaced by any suitable switching type with low V_{CE}. As shown in Eq 4, V_{CE} determines the minimum practical value for the control voltage V_c.

Obviously, for best performance, the source impedance for V_c should be low. Also, to obtain a smoothed mean-output voltage, a low-pass filter will be needed at the output of the multiplier. This is not shown in the schematic.

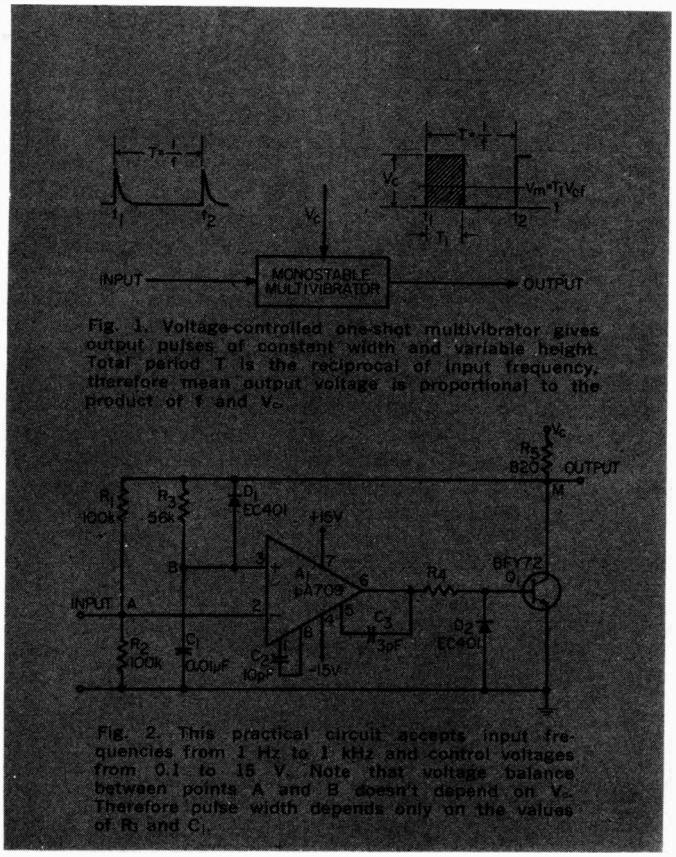


Fig. 1. Voltage-controlled one-shot multivibrator gives output pulses of constant width and variable height. Total period T is the reciprocal of input frequency, therefore mean output voltage is proportional to the product of f and V_c.

Fig. 2. This practical circuit accepts input frequencies from 1 Hz to 1 kHz and control voltages from 0.1 to 15 V. Note that voltage balance between points A and B doesn't depend on V_c. Therefore pulse width depends only on the values of R_3 and C_1.

Delayed-action data receiver

THIS CIRCUIT gives an adjustable delay of the leading edge of an input pulse. Thus it can inhibit digital signals to eliminate unwanted noise such as line reflections and switch bounce.

The specific application for the circuit shown in Fig. 1 is to receive the control line ("Carrier Detect") from a Dataphone per EIA Std. RS-232B. Entry of information, from control line to system, can be delayed by up to 9 milliseconds. This is sufficient delay to avoid the noise (caused by line reflections) which normally appears for the first 3 to 4 milliseconds after the Dataphone's "Carrier-Detect" line comes on.

Of course, the basic circuit can be used in many other applications where signal delay is required. The first stage merely provides a suitable interface for a Dataphone. So, for other applications, Q_1, R_1, R_2 and CR_1 can usually be omitted.

The following circuit description assumes use with a Dataphone — though readers should easily be able to see what modifications will be needed for operation from other signal sources.

Let's assume that, initially, the input to Q_1 is low. The output from inverter Z_1 will also be low, thus clamping the emitter of unijunction transistor Q_2 to near-zero volts ($V_{fd(CR2)} + V_{CE\,SAT(Z1)}$). This prevents C_1 from accumulating a significant charge. Note that the output of Z_1 is also connected to the "Clear" input of edge-triggered flip-flop Z_2. The low "Clear" input holds the Q side of Z_2 in the low state.

When the "Carrier-Detect" line (from the Dataphone) is activated, the input to Q_1 bounces between low and high for 3 or 4 milliseconds, as also does inverter output Z_1. However, because of the random cycling, C_1 never

manages to charge to the necessary UJT firing level (V_p) nor does the cycling affect the "Clear" input of Z_2. When the input ringing finally dampens out, the input remains at a high state. This removes the clamp from C_1, thus allowing a charge current through R_4 and R_5.

When Q_2 finally fires, C_1 discharges through R_7 and develops a positive-going transition at the clock input of Z_2. Amplitude of this transition is approximately (0.4) E_s. The Q output of Z_2 is triggered to the high state.

When the "Carrier-Detect" input returns to the low state, Z_1 output again goes low, thus clearing Z_2 output to the low state and removing any excess charge on C_1.

Figure 2 shows typical input and output waveforms for the circuit. Note that a pulse generator was used for this test, so the input waveform is clean, whereas in practice it would be noisy. Because of the unijunction characteristics, data rates for this circuit should be held to frequencies below 500 kHz.

Delay time is determined by the RC time constant. C (R_1 + R_2), and by the intrinsic firing level V_p for Q_2.

$$V_p = \eta E_s + V_{D(Q2)} \quad (1)$$

where,

η is the intrinsic level of Q_2, V_D is the emitter-base-1 drop of Q_2,

and,

$$V_c = E_s + V_{D(CR2)}\left(1 - e^{\frac{-t}{RC}}\right) \quad (2)$$

If we assume that $V_{D(Q2)} = V_{D(CR2)}$, then, substituting and transposing, the diode drops and E_s cancel, leaving,

$$\frac{t}{RC} = \log_e \eta - 1 \quad (3)$$

(Note that E_s is eliminated from the expression, indicating that delay time is not sensitive to power-supply variations.)

With the component values shown in Fig. 1, the circuit gives a guaranteed minimum delay of 5 milliseconds and a maximum delay of 9 milliseconds for all production spreads of component tolerance. If required, delays of several seconds could easily be achieved by selecting suitable values for R_5 and C_1.

Resistor R_6 helps maintain a low TC for Q_2 (typically 0.01%/°C); while R_8 provides pull-up for the "D" and "Preset" inputs of Z_2, thus reducing the possibility of false triggering.

The circuit described has several advantages compared with circuits using ICs throughout. Its major advantages are low cost, noise immunity, power-supply rejection and long-delay capability. Cost should not exceed $5 in small quantities. Long accurate delays are possible without the need for large capacitors.

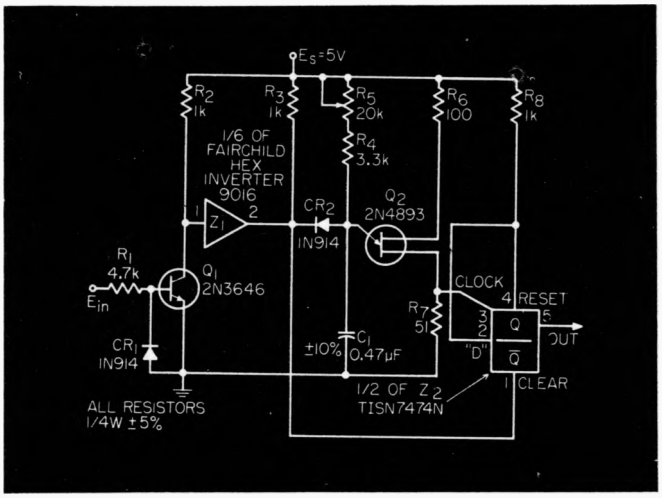


Fig. 1. Delayed-action data receiver inhibits noise in logic systems. Input stage Q_1 is designed to interface with a Dataphone.

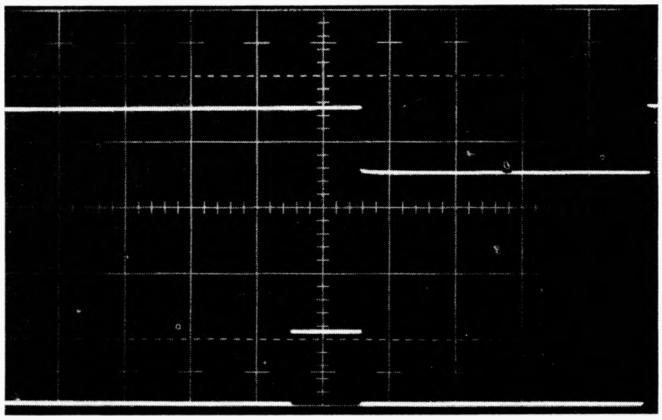


Fig. 2. Inpnt (top) and output (bottom) waveforms for data receiver. Vertical scale is 5 volts/division and horizontal scale is 2 milliseconds/division.

FETs program op-amp gain

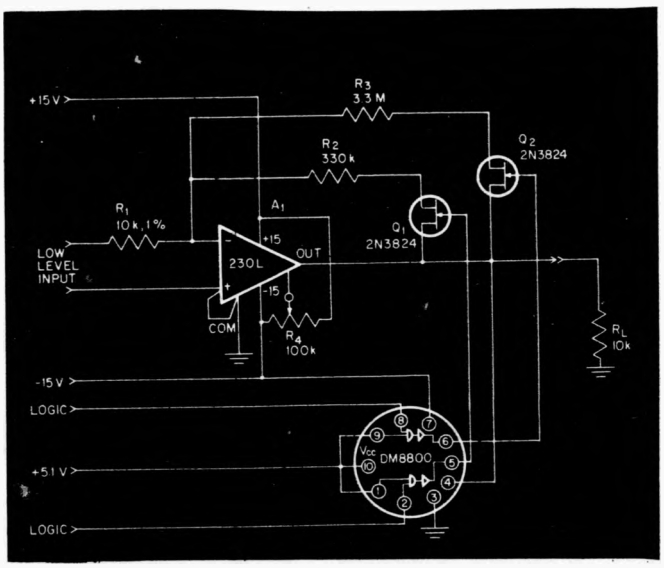
TTL or DTL logic levels can be used to program gains for the amplifier A_1 in the figure over a range of 1 to more than 1200. With the values shown, the amplifier has programmable gains of 33 and 330.

The amplifier is the chopper-stabilized Analog Devices 230L op amp, but any amplifier with low noise, low tempco and dc-millivolt analog interfacing can be used. Gain of the amplifier depends on the feedback resistor (R_2 or R_3) selected by an n-channel junction FET (Q_1 or Q_2).

The FETs used are TI 2N3824s. They have low on resistance ($< 250\ \Omega$) and low I_d (off) (< 0.1 nA with $V_{gs} = -5$ V and $V_{ds} =$ +15 V at 25°C). Off resistances exceed several megohms.

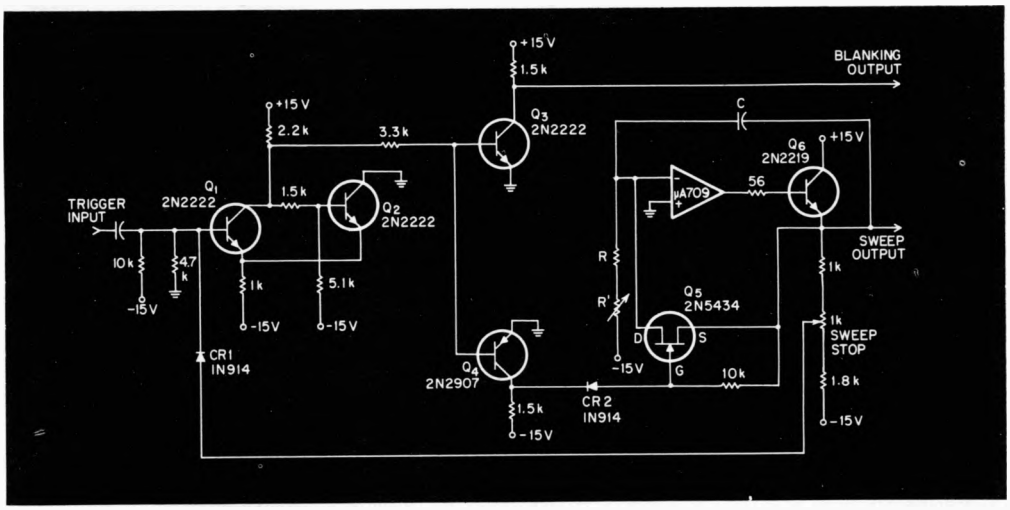
The FETs are controlled by a dual-voltage translator, the National Semiconductor DM-8800. One end of an internal 16-kΩ resistor (pin *4*), is connected to the amplifier's output. The gate of each FET is connected to a different output of the DM8800.

A logic low ($\leq$ 0.8 V) into pin 2 of the DM8800 places output pin *5* at the same potential as the 230L output, which turns on Q_1. A logic high ($\geq$ 2V, $\leq$ 5 V) into pin *8* places the gate of Q_2 at −14 V, which turns it off. Amplifier gain is equal to the ratio of feedback resistance (R_2 or R_3) to input resistance (R_1).



A dual-voltage translator, controlled by DTL or TTL levels, controls the FETs which select the feedback resistance that determines the gain of the op amp. Applied to pin 8 or 2 of the translator, logic low turns on and logic high inhibits a FET.

Triggered sweep features low dc offset



Triggered sweep circuit provides blanking as well as sweep output.

THIS TRIGGERED sweep combines the features available in the μA709 with those of a low-saturation-resistance FET to provide a 10-V linear sweep with very low dc offset.

In the circuit shown, Q_1 and Q_2 form a Schmitt-trigger input circuit. Transistors Q_3 and Q_4 provide the unblanking output and unclamp the FET Q_5 to initiate the sweep. Q_3 and Q_4 are complementary to provide protection for the base-emitter junctions. Transistor Q_6 allows the circuit to drive a low-impedance or capacitive load with little effect on the sweep timing.

Diode CR_2 and the 10-kΩ resistor from source to gate effectively isolate the FET from its driving circuit, thus providing the low dc offset voltage.

Sweep speed is determined by the $C(R + R')$ value. The value of $R + R'$ should be high with respect to the on resistance of the FET since small values of resistance produce a proportionally greater dc offset.

This circuit has been tried for sweep speeds from 1 Hz to 100 kHz. Dc offset voltages of 1 to 5 mV were obtained for these sweep speeds. Higher sweep speeds are limited by the slew rate of the μA709. The slow speeds are limited by the input resistance.

The dc coupling used throughout provides a circuit for use with hybrid microcircuit techniques.

Pulse generator-to-CCSL interface

A SIMPLE CIRCUIT matches the negative output of a pulse generator to the positive-input requirement of an IC in the compatible current-sinking-logic family. It maintains a constant current of at least −1.6 mA for the "O" input to the CCSL and its offers wide latitude in choice of component values.

In the basic circuit of Fig. 1, the base of npn transistor Q_1 is grounded through R and the collector (pin A) is connected (at pin 1) to the CCSL component through a constant-current regulator diode. The generator delivers an output that varies between ground ("O" state) and an adjustable negative voltage ("1" state).

Ideally, the generator output and the required CCSL input are as shown in Fig. 2. To see the various voltage-current relationships, one can apply a negative-going voltage ramp in place of the generator output. In place of the CCSL component, one can use a milliammeter to +5 V (typical for CCSL) as shown in Fig. 1 if A is connected to 2.

When the ramp starts at ground, Q_1 is biased off and no current flows through D_1. As the ramp voltage increases and reaches about −0.7 V, the diode and transistor begin to conduct. Initially the diode has a low resistance so the current through it is governed by the transistor. When the regulating-current level of the diode is reached, the diode resistance rises rapidly, keeping diode current fairly constant. As the ramp continues to rise, the transistor saturates. Fig. 3 shows the voltage-current relationships of this test circuit.

It's convenient to use 1 kΩ for R so the base current in milliamperes will have the same numerical value as V_s in volts. But this can lead to heating because, though the collector current saturates at 2 mA, the base current continues to rise as the ramp voltage increases. If we reduce the base current in the test circuit by using 10 kΩ for R, we modify the collector current as shown by the dashed line in Fig. 3.

Better yet, we can limit the base current to a maximum of 0.2 mA by using a regulator diode (pin B to pin 5) in place of the base resistor in Fig. 1.

The maximum voltage we apply to this circuit depends on the diode used for D_1. The V-I relationship for the 1N5305 is shown in Fig. 4. Constant-current operation occurs at the plateau between 3 V and the peak operating voltage which, in this series, is 100 V. The lower limit of the plateau depends on the diode, being lower for lower-current diodes. Above POV, the current increases sharply. Since the voltage across D_1 is always larger than that across D_2, the voltage applied to the

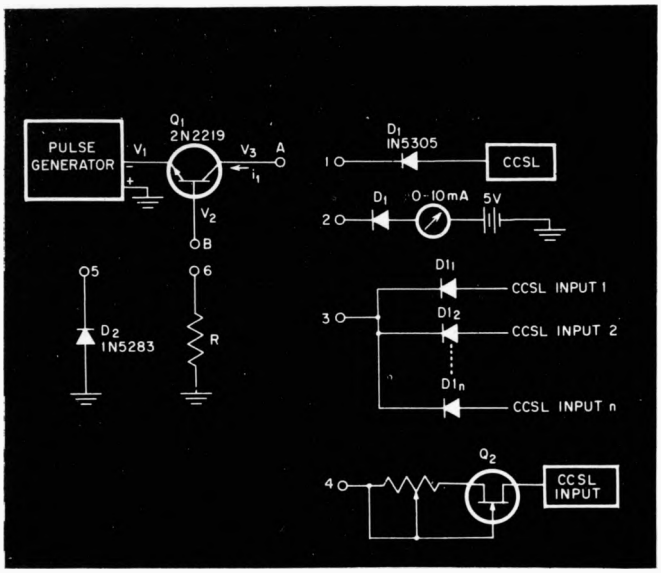


Fig. 1. Basic circuit for interconnecting a negative-going pulse generator to CCSL ICs. Many variations provide flexibility.

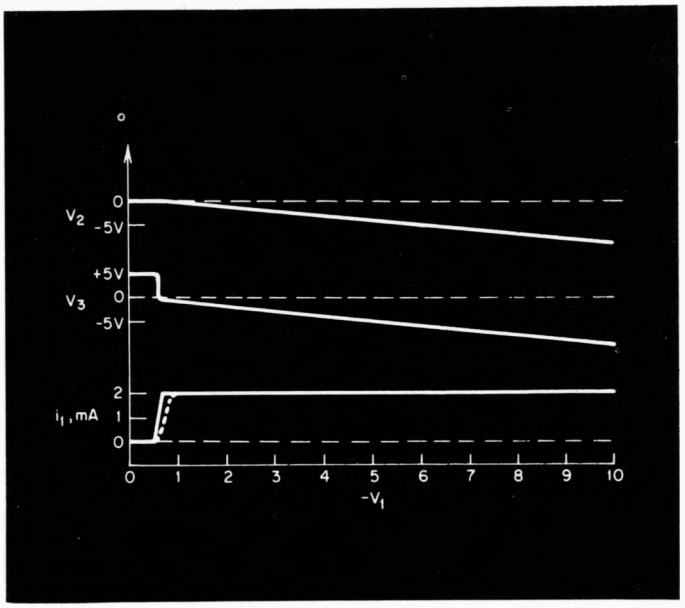


Fig. 3. Voltage-current relationships for a test circuit in which a negative-going ramp replaces the pulse generator and a meter and power supply replace the IC.

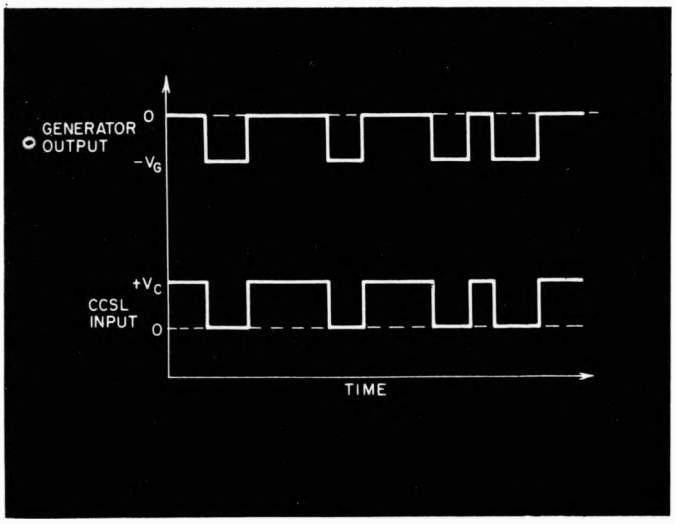


Fig. 2. The generator output must be shifted above the zero axis to provide a suitable CCSL input.

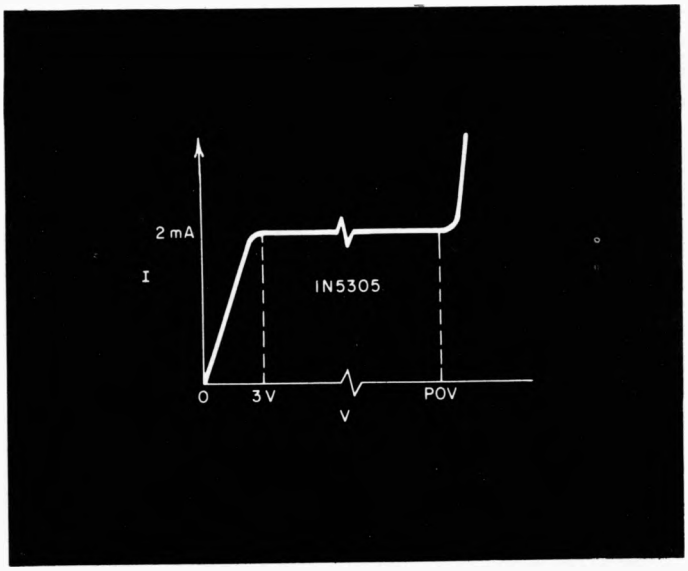


Fig. 4. V-I relationship for the 1N5305. The diode must never be operated beyond its peak operating voltage.

circuit must not produce a drop across D_1 greater than POV.

The 1N5303 regulates at 1.6 mA, which is the current required for a single CCSL input. Additional inputs must be connected (as in Fig. 1 with pin *A* to pin *3*) by using a separate diode for each input. Since all input current must pass through the pulse generator, the generator must be able to sink at least the combined currents.

If it's desirable to set the constant current at different levels, instead of using one regulator diode for each input we can use a potentiometer and FET (pin *A* to pin *4* in Fig. 1) to provide a constant current that's variable. ■

Fixed bias extends zener range

ADDING A SINGLE constant-current diode to a conventional zener regulator allows the zener to serve as a reference over a very wide range of input voltage. The constant-current diode fixes the zener's bias current, eliminating the usual problem that stems from the fact that the zener's bias current is a function of input voltage.

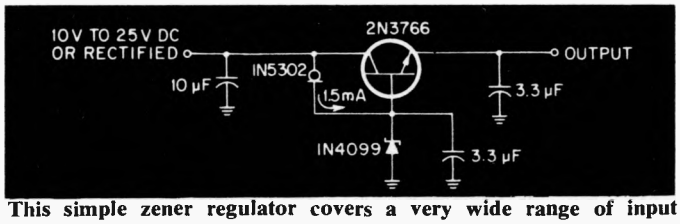
If a series-pass transistor is used with the zener circuit, the regulator becomes an unsophisticated dc supply for inputs of varying dc or rectified ac with large ripple.

In the circuit shown, a 1N-5302 constant-current diode provides the small bias necessary to sustain V_Z. Other diodes are available for constant currents in the 4- or 5-mA range. With a power transistor, these allow the design of hefty supplies for dc into the ampere range without a Darlington arrangement. They offer great ripple reduction.

For a particular supply, one selects the zener according to V_{OUT} and the no-load dissipation. The constant-current diode must supply

$$I = I_{out} + \frac{I_{zener\ bias}}{\beta}$$

while the transistor is chosen for the required dissipation and high beta. The constant-current diodes require about a 3-V drop to stabilize. This fixes $V_{in\ min}$ to $V_Z + 3$, which is the only real restraint on the circuit. ■



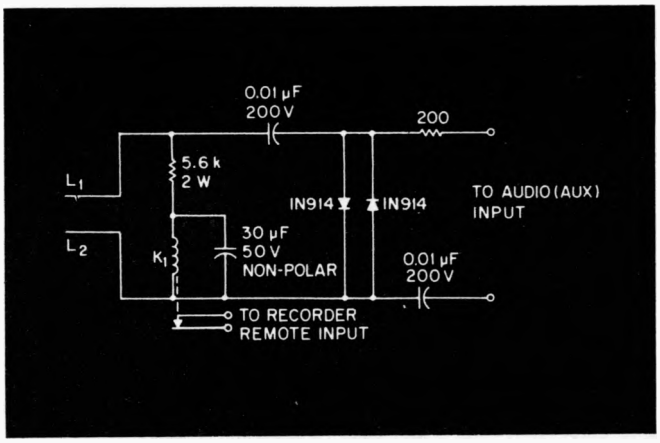
This simple zener regulator covers a very wide range of input voltages — even with large ripple content. It delivers at least 40 mA at a nominal 6 V.

Automatic telephone recorder

THIS SIMPLE CIRCUIT automatically turns on a tape recorder when a telephone receiver is lifted. Normally, there's 48 Vdc across L_1-L_2, the input wires to the telephone. That's enough to energize relay K_1, whose contacts (which go to the tape recorder's remote-switch input) are held open.

The dc resistance of K_1's coil plus the series resistor should be high enough to avoid producing an "off-hook" indication, which requires less than 2 kΩ. The ringing voltage, 90 V 20 Hz, doesn't get to the recorder's audio input because of the 1N914 diode pair, and it doesn't affect the relay coil because of the 30-μF capacitor.

When the receiver is lifted, the phone's varistor produces about 6 Vdc across L_1-L_2. That's low enough to allow K_1 to drop out; it's contacts close and start the recorder. The audio voltage across L_1-L_2 is low enough so the diode pair doesn't introduce distortion. ■



The circuit starts a tape recorder when a telephone receiver is lifted to make a call or receive one. The relay is a Sigma 65F1A —24 Vdc or equivalent.

Constant-amplitude phase shifter

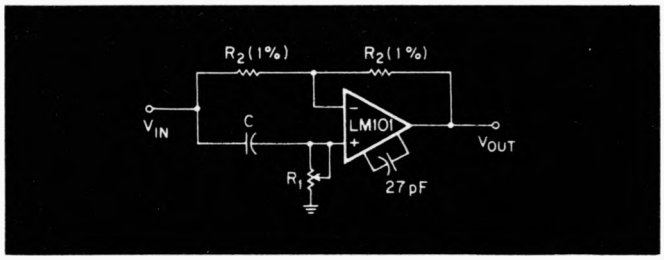
THE CIRCUIT SHOWN produces an output voltage equal in magnitude to the input voltage but shifted in phase. Voltage gain is:

$$G = \frac{j\omega CR_1 - 1}{j\omega CR_1 + 1}$$

where $|G| = 1$ *and phase — lead angle* $\phi = 2\ tan^{-1}\ (1/\omega CR_1)$

As ωCR_1 is varied (by changing R_1) from zero to much greater than unity, the phase shift varies from 180° lead to 90° lead (at $\omega CR_1 = 1$). As ωCR_1 becomes large, phase shift approaches 0°. Interchanging C and R_1 converts phase angle to lag rather than lead.

This circuit was used to vary phase shift of a 2.5-Vrms, 5-kHz sine wave from 180° to 30° lead. The component values are: R_2 equal to 10 k, R_1 is a 20-k pot and C is a 6800-pF capacitor. With a 600-ohm source generator, amplitude variation was less than 100 mV. ■



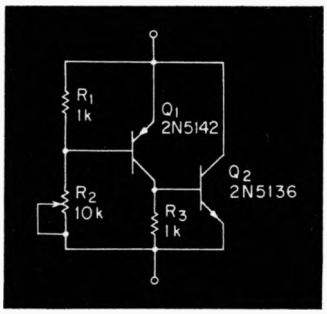
This IC-phase shifter produces 0 to 180° with a constant-amplitude output.

Adjustable, low-impedance zener

THE CIRCUIT in Fig. 1 performs the functions of a zener diode and is adjustable so that the voltage across its terminals is defined by

$$E_z = \frac{0.5\ R_1 + 0.5\ R_2}{R_1}$$

The circuit operates at any voltage above approximately 0.8 V and it has a zener impedance of 3 Ω max below E_z = 5 V. It's particularly useful in the 1- to 3-V region where normal zeners are not generally available and have considerably higher impedances.



This circuit is particularly useful in the 1- to 3-V range, where conventional zeners have much higher impedance.

The operating point is established by the voltage divider R_2/R_1, such that when the base-to-emitter voltage of Q_1 is greater than approximately 0.5 V, it causes Q_1 to pour current into R_3. When the voltage across R_3 becomes greater than approximately 0.5 V, Q_2 turns on quickly.

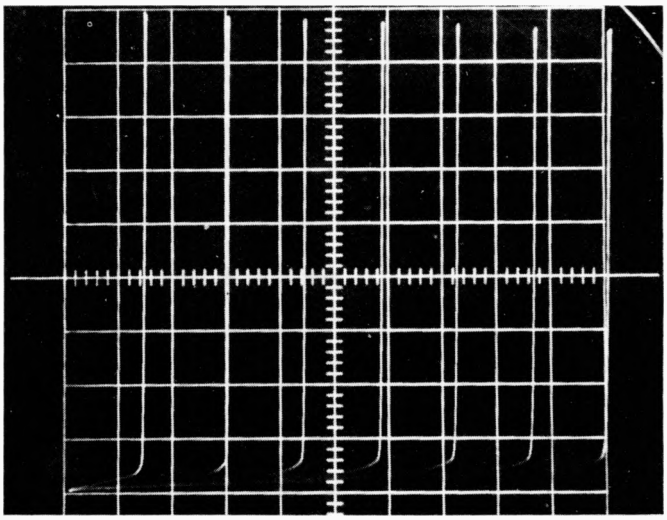


Fig. 2. Zener curves for various settings of R_2 from 0 to 10 kΩ. Vertical scale is 2 mA/div, horizontal is 0.5 V/div.

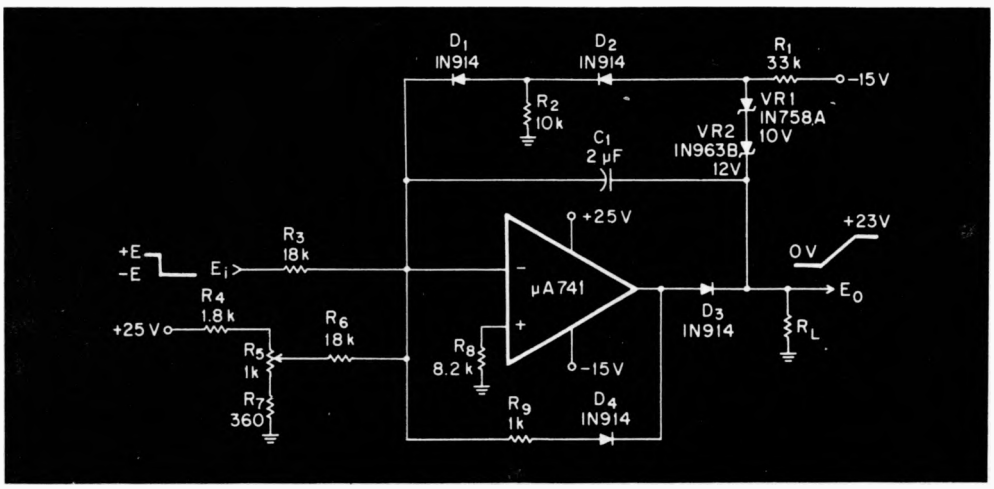
The high voltage gain of Q_1 and the low drive impedance provided by R_3 make the zener knee sharp, as in Fig. 2. ■

Fast-recovery integrator with adjustable threshold

BY PREVENTING the op amp from saturating we can make the recovery time of this integrator approximately equal to the amplifier's slew rate. Diodes D_1 and D_2 are normally biased off until the output voltage E_o exceeds the zener voltage of regulators VR_1 and VR_2.

Further increase of the output voltage forward biases D_1 and D_2. The output is then clamped to the sum of the zener and diode voltages, which is below the amplifier's saturation level.

Resistor R_2 bypasses the diode leakage current to the summing junction when D_2 is reverse biased. The adjustable threshold voltage and the input signal are summed at the inverting input.

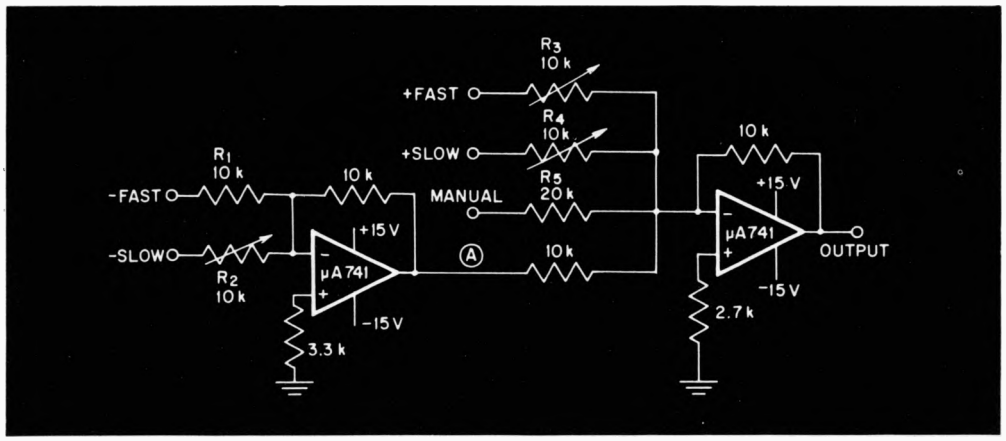


Two diodes and two zeners clamp this integrator's output to below the op amp's saturation voltage, making for fast recovery. All resistors are 5%, 1/4-W carbon comps.

Diode D_3 rectifies and D_4 decouples the amplifier output to provide a circuit output that is always positive. Resistor R_9 provides gain compensation to prevent amplifier oscillation. The polarity of E_o may be made negative by reversing all diodes, the reference input and the zener supply.

With the component values shown and using +25-V and −15-V supplies, the integration time constant (C_1R_3) is 35.6 ms and the output is clamped at +23 V. The output linearity is ±1% and the threshold range of this circuit is −3 to −10 V. ■

Bipolar analog/digital interface for servos



This circuit interfaces between digital or bipolar analog signals and a bi-directional servo.

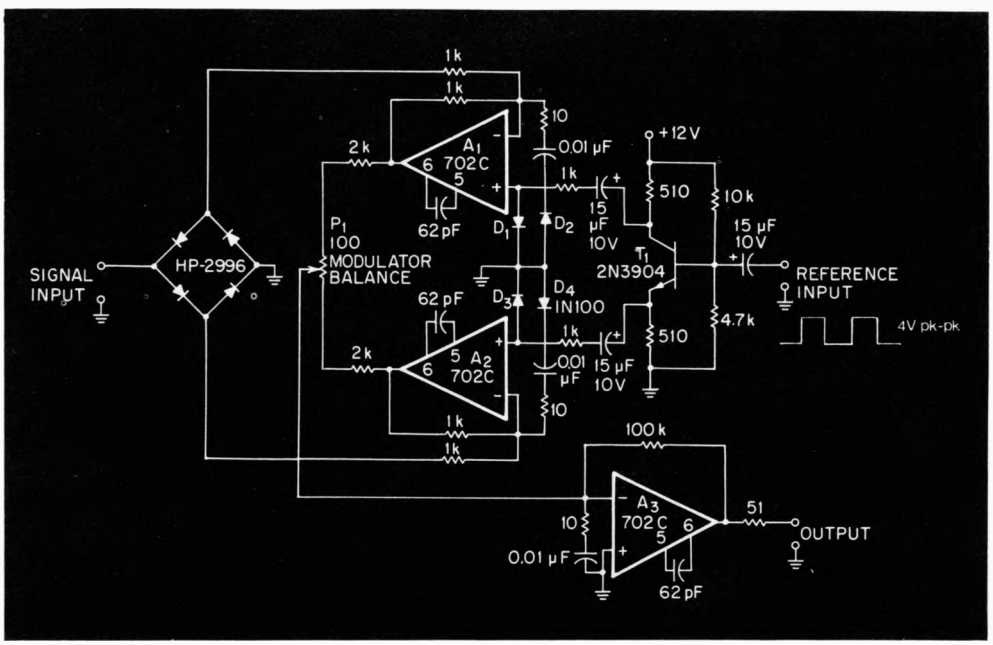
VELOCITY SERVOS often require a positive input voltage for drive in one direction and a negative input for motion in the opposite direction. When a system must provide bidirectional motion for both analog and digital inputs, some sort of interface must be provided.

The configuration in the figure accepts both bipolar manual input (from a speed control, for example) and input logic levels (+ for forward, — for reverse) from digital circuits to provide a bipolar output compatible with the servo input. Resistors R_1 to R_4 provide means for independently adjusting the gain of each channel.

The circuit accepts signals for fast or slow motion in either direction. The "Manual" input can be continuously variable from −15 V to +15 V. The other four inputs take 5-V logic.

At point A, the voltage will be zero when the "—Slow" or "—Fast" input is at 0 V. The voltage at A will be +2 V or +8 V, respectively, for "—Slow" or "—Fast" inputs of +5 V (adjustable to suit the motor being driven). The output can vary between −10 V and +10 V. ■

Transformerless ring modulator



IC op amps obviate transformers and extend the frequency range of this ring modulator.

A RING modulator is very useful for phase detection and modulation, but it requires transformers to operate the diode ring. This severely limits its use at low frequencies and requires a transformer change whenever the operating frequency is changed more than two decades from the transformer's design center.

A satisfactory alternative to transformer operation is provided by inexpensive monolithic operational amplifiers. The circuit shown is usable at frequencies from 10 Hz to 1 MHz with no component changes. Amplifiers A_1 and A_2 gate the hot-carrier diodes and condition the signal.

Gating is done with the signal applied to the positive inputs of two amplifiers. This signal is a 0.6 V pk-pk square wave which also appears at the negative input of each amplifier and hence, across the diode ring through a 1-kΩ resistor. Since the positive inputs are operated from both outputs of the transistor inverter T_1, the drives are out of phase with each other and cause a ±0.6-V signal to be applied across the diode ring at alternate half cycles. This level signal is adequate to switch the diodes.

The incoming signal is passed into each amplifier with a gain of one during one half of the reference cycle and disconnected during the second half. The output of both amplifiers is summed into a third amplifier A_3. The output of A_3 is ground during one half of the reference cycle and equal to twice the input signal during the second half. Potentiometer P_1 adjusts the output of A_3 for best ac zero with no signal input. ■

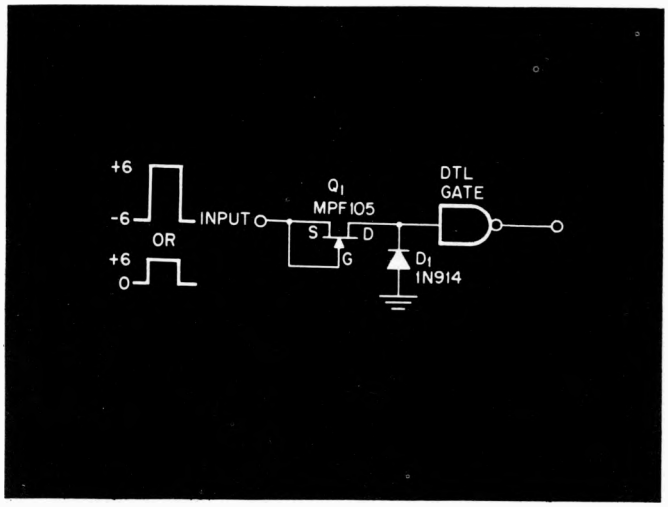
Simple EIA phone level DTL interface

A FIELD-EFFECT transistor, connected as a constant-current diode, allows portable equipment to interface with standard DTL and with EIA telephone-company level shifts from −6 to +6 V.

The input signal goes to a DTL circuit through the FET which clamps the input to ground through diode D_1 in the circuit shown. The FET used has a typical drain current of 9 mA with gate connected to source, thus protecting the driving circuit from current overload in the negative direction.

When standard DTL levels are used with a false level on the interface input, the gate voltage (with one sample lot of FETs) ranges from 0.3 to 0.47 V. If the equipment must work in a high-noise environment, it may be necessary to select FETs to insure optimum performance.

Tests run on the circuit with and without the interface show no change in rise time, fall time or propagation delay. ■



Diode-connected FET interfaces DTL and EIA telephone levels.

Simple gyrator for L from C

THE ADVENT OF low-cost IC amplifiers has made it practical to use the gyrator circuit to provide inductive effects without the usual limitations of coils. The gyrator is a circuit whose input impedance is proportional to the reciprocal of its load impedance. So the input to a gyrator loaded with a capacitor looks like an inductor with higher Q than available in the usual commercial inductor.

Figure 1 shows a simple gyrator with a capacitive load. The gyrator (in dashed lines) includes two amplifiers with gain A, one inverting and one noninverting. Each amplifier has a Z_1, Z_2 and R_L representing, respectively, its input impedance, output impedance and load resistance.

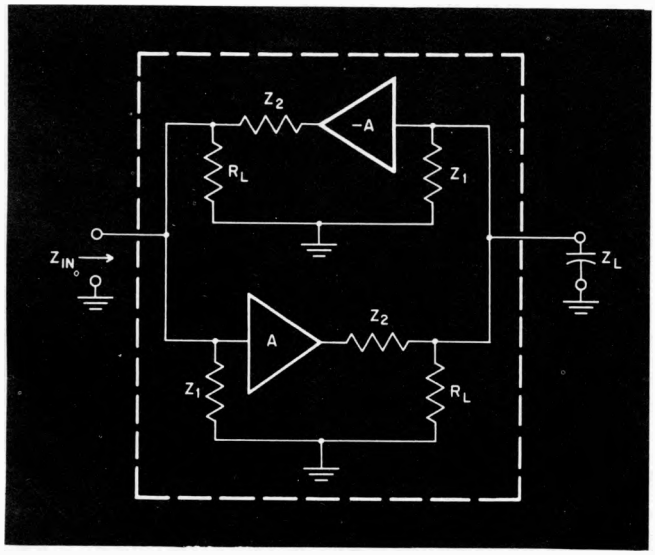


Fig. 1. This is a generalized gyrator circuit with a capacitive load.

The input impedance of a gyrator loaded with capacitor C is

$$Z_{in} = \frac{P(P^2+G^2+\omega^2C^2)+j\omega G^2C}{(P^2+G^2)^2+P^2\omega^2C^2}$$

where $$P = \frac{1}{R_L}+\frac{1}{Z_1}+\frac{1}{Z_2}$$

and $G = A/Z_2$.

The Q of the loaded circuit is

$$Q = \frac{\omega G^2C}{P(P^2+G^2+\omega^2C^2)}$$

which has an approximate maximum of G/2P at an angular frequency

$$\omega = \sqrt{\frac{P^2+G^2}{C^2}}.$$

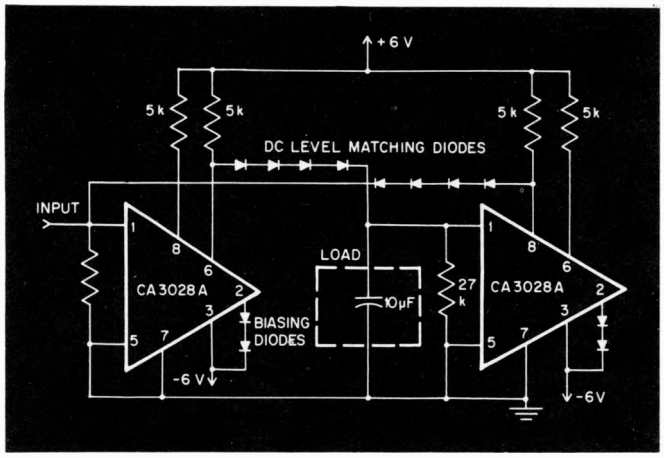


Fig. 2. This specific gyrator, with a 10-μF load, effectively forms a 12-μH inductor.

Figure 2 shows two RCA CA3028A ICs in a gyrator loaded with a 10-μF capacitor. In this circuit, the amplifiers had $A = 1000$, $Z_1 = 2$ kΩ, $Z_2 = 12$ kΩ and $R_L = 5$ kΩ.

These values give an effective 12-μH inductor which is quite constant over a range from 10 Hz to almost 1 MHz. The Q varies from 1 at 10 Hz to a maximum of 500 at 10 kHz. ■

An error-stabilized analog divider

FIGURE 1 illustrates a circuit for analog division. In this method an analog multiplier is placed in the feedback loop of an operational amplifier. However, this method is limited by the drift of the multiplier. Fig. 2 shows a circuit for cancelling error due to multiplier drift.

In the new circuit, the multiplier output (XY/10) is sampled at $t = 0$. This signal is inverted and fed into the op-amp's summing point, effectively cancelling the error at $t = 0$. Fig. 2 illustrates this method for a wide-band error-stabilized analog divider.

The system generates a waveform of the form $e = Z/kt$ where Z varies 40:1 and K is variable from 1.7 V/μs to 0.2 V/μs. System waveshapes are illustrated in Fig. 3 for a prf of 15 kHz. The multiplier selected, a Hybrid System 105, has an inverted output which is used to simplify the error-cancellation circuit. In order to maintain loop stability at the high speed desired, the op-amp unity-gain frequency must be equal to or less than the 3-dB frequency of the multiplier. A limiter loop was also included to prevent overdrive of the op amp and multiplier. ■

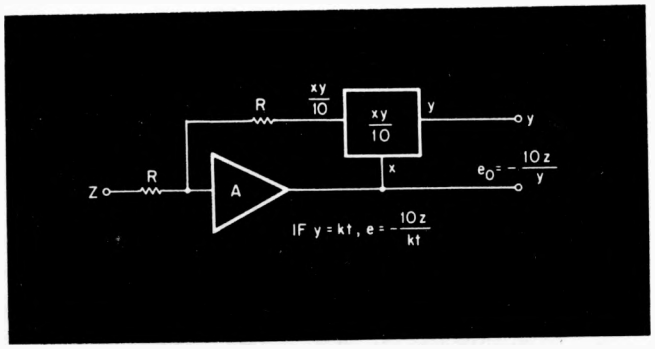


Fig. 1. This is the usual method of analog division.

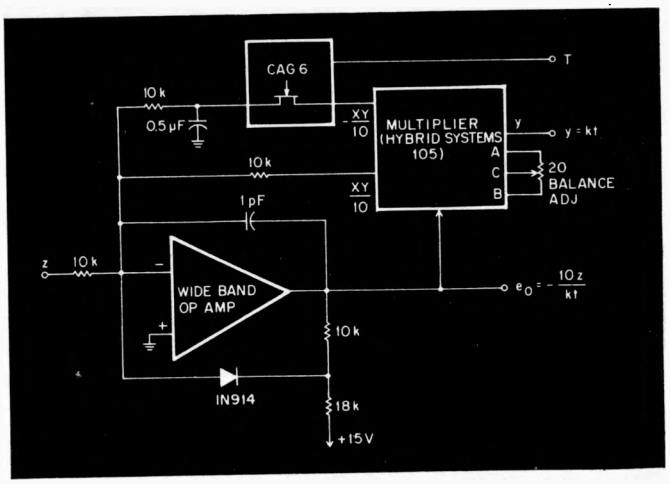


Fig. 2. This circuit shows a method of eliminating multiplier drift.

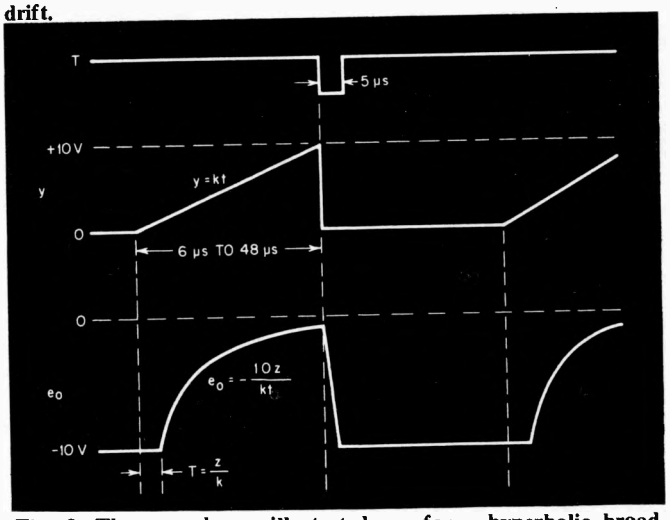
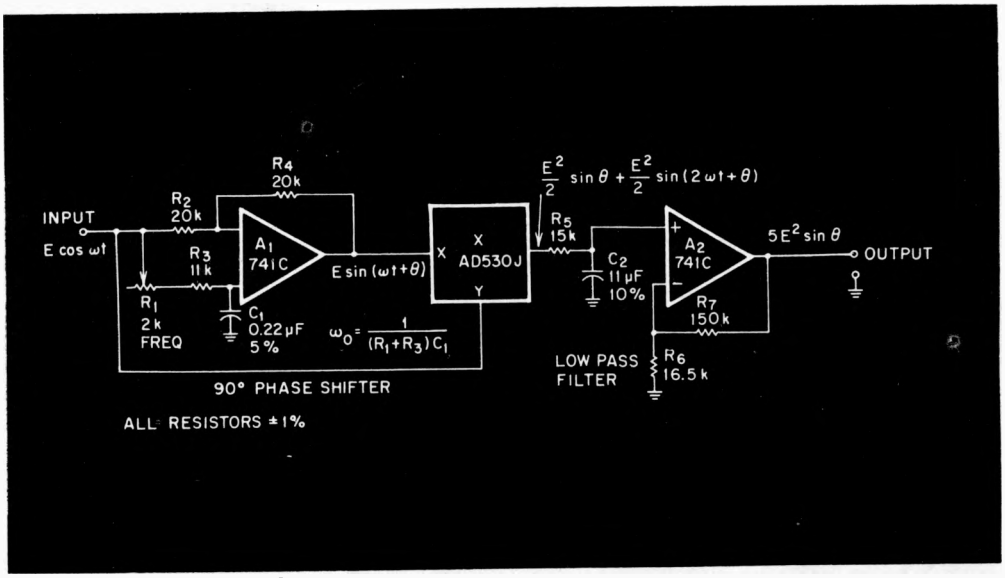


Fig. 3. The waveshapes illustrated are for a hyperbolic broadband generator.

60-Hz frequency discriminator

THIS CIRCUIT delivers a dc output voltage proportional to the frequency deviation of the input voltage from a nominal center frequency. With the values shown, the center frequency is 60 Hz. This circuit is useful for frequency measurement or motor speed control. In addition, the phase shifter and multiplier portion of the circuit can be used for second harmonic generation without producing a dc output.

An input signal is fed directly to the Y input of the multiplier and also through a 90°-phase shifter A_1 to the X input of the multiplier. The output of the multiplier is the second harmonic of the input and a dc component. This signal is filtered and amplified by buffer A_2, A_2's dc gain is 10. Output voltage is proportional to frequency deviation from the frequency at which A_1 has 90°-phase shift. At 7 Vrms input, the dc output is 500 mV per percent of center frequency change. R_1 is adjusted for 0 Vdc at the center frequency. ■



Two IC op-amps and a multiplier form a frequency discriminator circuit.

Steering diodes insure SCR commutation

THE SCR flip-flop of Fig. 1 has a basic problem. Trigger pulses for turn on and turn off must be spaced so that there is adequate time for the commutation capacitor to charge sufficiently to insure proper commutation. Often unwanted or transient conditions cause trigger pulses to appear in rapid succession. This can result in both SCR's turning on (lock-up).

Addition of steering diodes provides automatic rejection of premature triggers, insures commutation when triggered by properly spaced pulses and prevents lock-up. Figure 2 shows the modified switch. Diodes D_1 and D_2 are returned to reference voltages. These are chosen by the minimum requirements for commutation of each SCR. A single reference can be used if maximum speed is not critical. $Ref._1$ determines minimum commutation voltage available for turning off SCR_2, while $Ref._2$ determines the minimum commutation voltage available for SCR_1. Steering and timing are done by biasing D_1 and D_2 off until the anode voltage of SCR_1 and SCR_2 respectively, have risen high enough to forward bias the steering diodes. Trigger pulses will then be rejected until adequate energy is stored in commutation capacitor C. C_1 and C_2 prevent power transients from triggering the SCRs.

This circuit does exhibit start-up problems since the gates are tied to +V. This problem is alleviated by providing a turn-on switch to provide power to one load resistor-SCR combination as well as the reference supplies. After charging transients subside, power can be applied to the other load-SCR combination without latch-up. ■

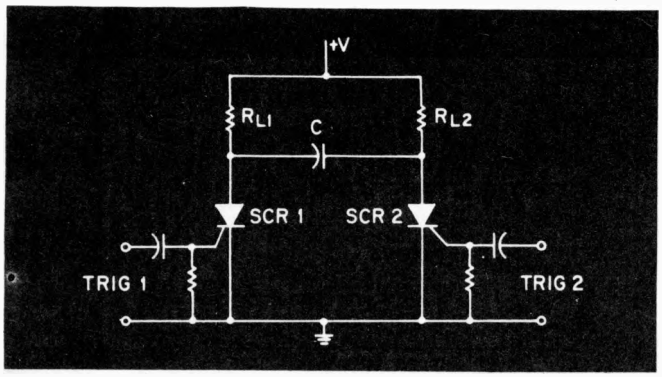


Fig. 1. A conventional SCR flip-flop which has latch-up problems.

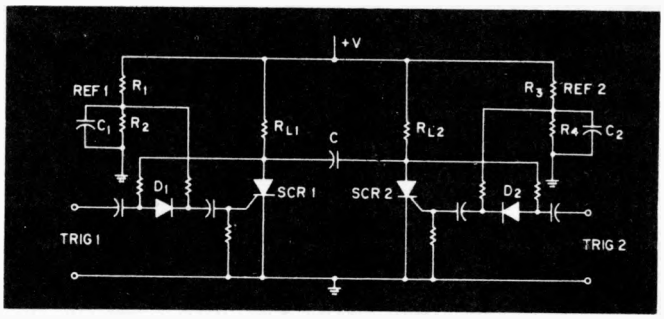


Fig. 2. An improved dc static switch with steering diodes eliminates the latch-up problem.

The ideal voltage follower

WITH A COUPLE of minor changes, a simple voltage follower circuit can be made to have unity gain, zero bias current and infinite input impedance. In the basic circuit of Fig. 1 (without the dashed components) when the input voltage rises, the current in Q_1 increases and the current in Q_2 falls a like amount, since the current source Q_3 insures a constant total current thru the pair. The falling current in Q_2 causes the collector voltage of Q_2 to rise which in turn causes the emitter voltages of Q_3 and Q_4 to rise, thus following the input voltage. Since the currents in Q_1 and Q_2 change, their base-emitter voltages change also and the circuit has less than unity gain as a consequence.

The unmodified circuit has a input impedance of about 33 megohms and requires a bias current of about 0.7 microamps. The addition of R_6 (dashed), which is half the value of R_2, causes the current from the current source to change twice as much as the current in R_2 (or Q_2). Thus the current in Q_1 is made to change just as much as the current in Q_2 and in the same direction!

This results in exactly unity gain; but also in a negative impedance (−33 megohms). The addition of R_7 (dashed) from the input to V_{cc}, supplies most of the bias current and cancels the negative input impedance. If R_7 were connected to a +21 V supply, the bias current would be completely supplied. The temperature sensitivity of the transistor betas causes a departure from the ideal, limiting the benefits of the latter properties to narrow temperature range applications. The effects of temperature and supply voltage on offset voltage can be seen in Fig. 2. The measured gain is 0.9997 V/V with an error of ±0.1% over a ±1.5 V swing. ■

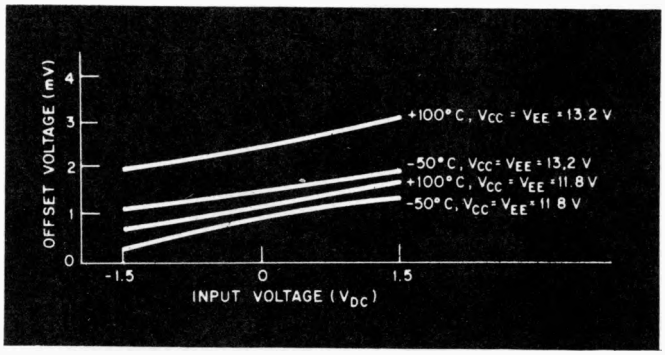


Fig. 2. Offset voltage versus input voltage as a function of supply voltage and temperature.

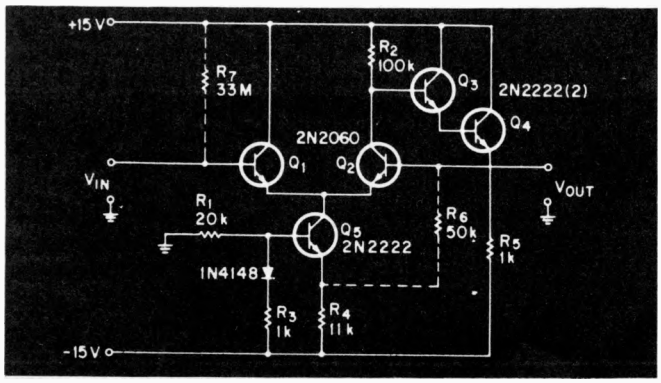


Fig. 1. R_1 and R_6 give the basic follower circuit unity gain, infinite input Z and/or zero input current. Actual gain is 0.9997 V/V.

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