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Contents

Introduction

The ideal logic family should dissipate no power, have zero propagation delay, controlled rise and fall times, and have noise immunity equal to 50 percent of the logic swing. The properties of CMOS (Complementary MOS) begin to approach these ideal characteristics.

First, CMOS dissipates low power. Typically, the static power dissipation is 10 nW per gate, which is due to the flow of leakage currents. The active power depends on power supply voltage, frequency, output load and input rise time, but typically, gate dissipation at 1MHz with a 50-pF load is less than 10 mW.

Second, the propagation delays through CMOS are short, though not quite zero. Depending on power supply voltage, the delay through a typical gate is on the order of 25 to 50 ns.

Third, rise and fall times are controlled, tending to be ramps rather than step functions. Typically, rise and fall times tend to be 20 percent to 40 percent longer than the propagation delays.

Last, but not least, is the noise immunity. This approaches 50 percent, being typically 45 percent of the full logic swing.

On a component basis, CMOS is still more expensive than TTL. However, system level cost may be lower. The power supplies in a CMOS system will be less expensive since they can be made smaller and with less regulation. Because of lower currents, the power supply distribution system can be simpler and, therefore, cheaper. Fans and other cooling equipment are not needed because of the lower dissipation. Longer rise and fall times make the transmission of digital signals simpler. This, in turn, makes transmission

techniques less expensive. Finally, there is no technical reason why CMOS prices cannot approach present day TTL prices as sales volume and manufacturing experience increase. So an engineer about to start a new design should compare the system level cost of using CMOS or some other logic family. He may find that even at today's prices, CMOS is the most economical choice.

The 74C line consists of CMOS parts which are pin and functional equivalents of many of the most popular parts in the 7400 TTL series. This line is typically 50 percent faster than the 4000A series and sinks 50 percent more current. For ease of design, it is specified at TTL levels as well as CMOS levels, and there are two temperature ranges available: 54C, −55°C to +125°C or 74C, −40°C to +85°C.

TTL FAMILY

TTL devices differ widely in function, complexity and performance, but their electrical input and output characteristics are very similar and are defined and tested to guarantee compatibility. The oldest TTL product category is the gold-doped double-diffused type, which is made up of the 7400 devices. The 74H family is a high performance version of the 74 series which uses the gold doped structure, but has higher power and faster speeds. The 74S products are fabricated with a nonsaturating Schottky clamped transistor technique. The 74S TTL products are very high performance, high-power devices. The newest and most popular TTL category is the 74LS low-power schottky family. These products feature the performance of the 74 family at about one-quarter the power.

Absolute Maximum Ratings

The absolute maximum ratings constitute limiting values above which serviceability of the device may be impaired. Provisions should be made in system design and testing to limit voltages and currents as shown in the table.

Operating Temperature and Voltage Ranges

The nominal supply voltage (Vcc) for all TTL circuits is +5.0 volts. Commercial grade (7400) parts are guaranteed to perform with a ±5 percent supply tolerance (±250 mV) over an ambient temperature range of 0°C to 70°C. The Military grade (5400) parts are guaranteed to perform with a ±10 percent supply tolerance (±500 mV) over an ambient temperature range of −55°C to +125°C.

Input Loading and Output Drive Characteristics

The logic levels of all the TTL products are fully compatible with each other. However, the input loading and output drive characteristics of each of these families is different and must be taken into consideration when mixing the TTL families in a system.

Mixing TTL Families

Most TTL families are intended for use together, but this cannot be done indiscriminately. Each family of TTL devices has unique input and output characteristics optimized to get the desired speed or power features. Fast devices like 74S and 74H are designed with relatively low input and output impedances. The speed of these devices is determined primarily by fast rise and fall times internally, as well as at the input and output nodes. These fast transitions cause noise of various types in the system. Power and ground line noise is generated by the large currents needed to charge and discharge the circuit and load capacitances during the switching transitions. Signal line noise is generated by the fast output transitions and the relatively low output impedances, which tend to increase reflections.

The noise generated by these 74S and 74H can only be tolerated in systems designed with very short signal leads, elaborate ground planes, and good, well decoupled power distribution networks. Mixing the slower TTL families like 74 and 74LS with the higher speed families is also possible but must be done with caution. The slower speed families are more susceptible to induced noise than the higher speed families due to their higher input and output impedances. The low power Schottky 74LS family is especially sensitive to induced noise and must be isolated as much as possible from the 74S or 74H devices. Separate or isolated power and ground systems are recommended, and the LS input signal lines should not run adjacent to lines driven by 74S or 74H devices.

Mixing 74 and 74LS is less restrictive, and the overall system design need not be so elaborate. Standard two-sided PC boards can be used with good decoupled power and ground grid systems. The signal transitions are slower and therefore generate less noise. However, good high-speed design techniques are still required, especially when working with counters, registers, or other devices with memory.

Clayton L. Hallmark

Section One

CMOS

Included in this chapter are the 4000 and 74C series of complementary MOS, or CMOS, digital ICs. Throughout, you'll find logic diagrams, which are block diagrams using logic symbols, power dissipation information and truth tables. Also, data for quiescent current, TTL-driving capability loads and supply voltage range are given.

CMOS Chip Listing

4000-Series CMOS

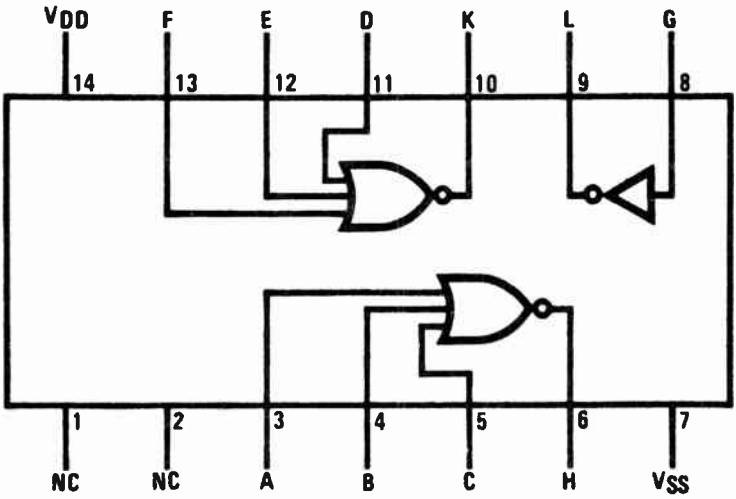
74C00-Series CMOS

80C00-Series CMOS

4000 DUAL 3-INPUT NOR GATE PLUS INVERTER

The 4000 is a monolithic complementary MOS (CMOS) dual 3-input NOR gate plus an inverter. N-channel and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Supply Voltage Range	**3V to 15V**
Power	**10nW typ.**
Noise Immunity	**0.45 V_{DD} typ.**

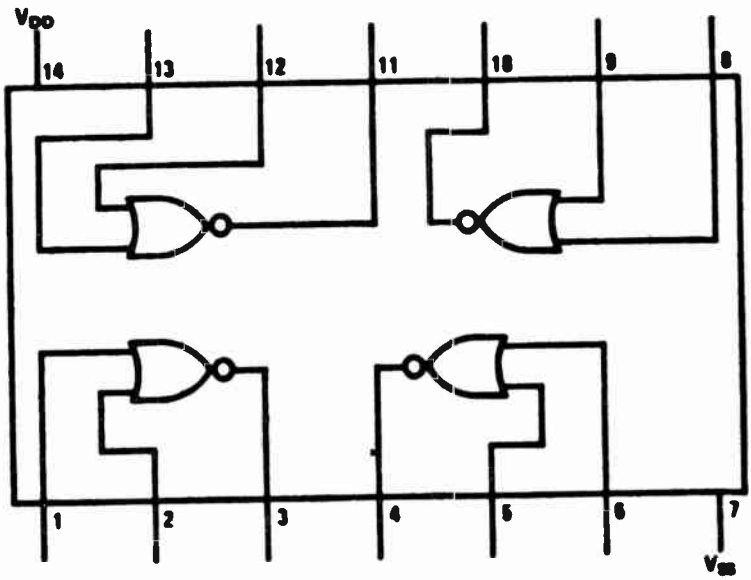


4000

4001 QUADRUPLE 2-INPUT NOR GATE

The 4001 is a monolithic complementary MOS (CMOS) quadruple 2-input NOR gate integrated circuit. N-channel and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Supply Voltage Range	**3V to 15V**
Power	**10 nW (typ.)**
Noise Immunity	**0.45 V_{DD} (typ.)**

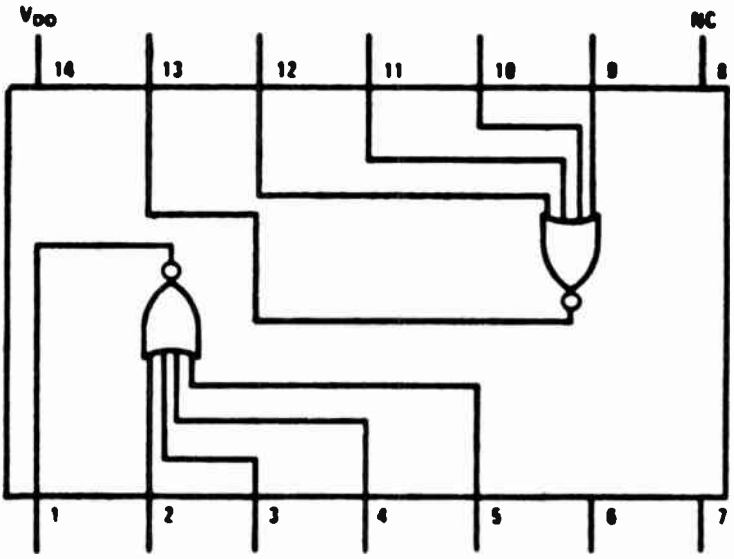


4001

4002 DUAL 4-INPUT NOR GATE

The 4002 NOR gate is a monolithic complementary MOS (CMOS) integrated circuit. The N-channel and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Supply Voltage Range	**3V to 15V**
Power	**10 nW (typical)**
Noise Immunity	**0.45 V_{DD} (typical)**

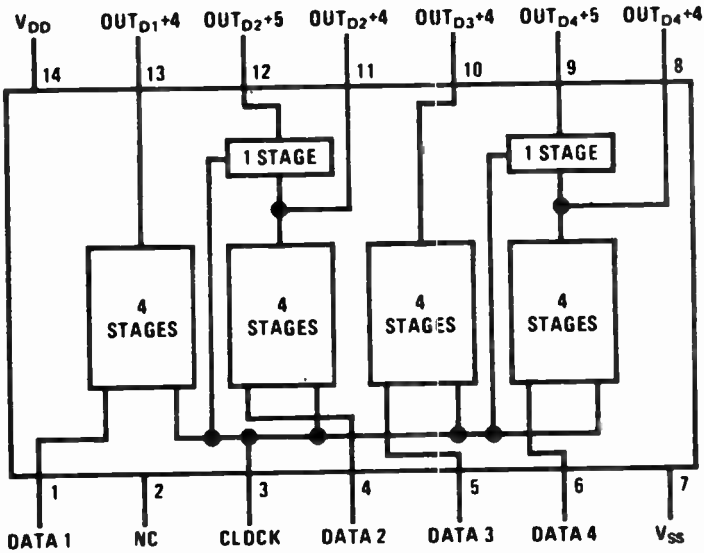


4002

4006 18-STAGE STATIC SHIFT REGISTER

The 4006 18-stage static shift register is comprised of four separate shift register sections, two sections of four stages and two sections of five stages. Each section has an independent data input. Outputs are available at the fourth stage and the fifth stage of each section. A common clock signal is used for all stages. Data is shifted to the next stage on the negative-going transition of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8 and 9 stages or single register sections of 10, 12, 13, 14, 16, 17 and 18 stages can be implemented using one package.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
Clock Input Capacitance	**6 pF typ.**
Speed of Operation	**10 MHz typ. with V_{DD} = 10V**



D	CL$^{\Delta}$	D+1
0	⌐¬	0
1	⌐¬	1
X	⌐¬	NC

4006
Truth Table

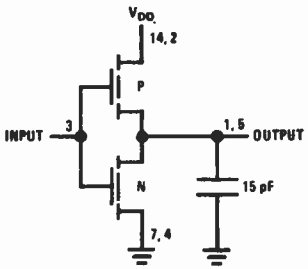
4006
X = Don't care
Δ = Level change
NC = No change

4007 DUAL COMPLEMENTARY PAIR PLUS INVERTER

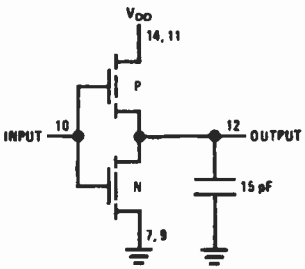
The 4007 consists of three complementary pairs of N-channel and P-channel enhancement mode MOS transistors suitable for series/shunt applications. All inputs are protected from static discharge by diode clamps to V_{DD} and Vss.

For proper operation, the voltages at all pins must be constrained to be between Vss -0.3V and V_{DD} $+0.3$V at all times.

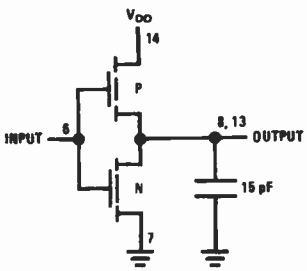
Supply Voltage Range **3V to 15V**
Noise Immunity **0.45 V_{CC} typ.**



4007



4007

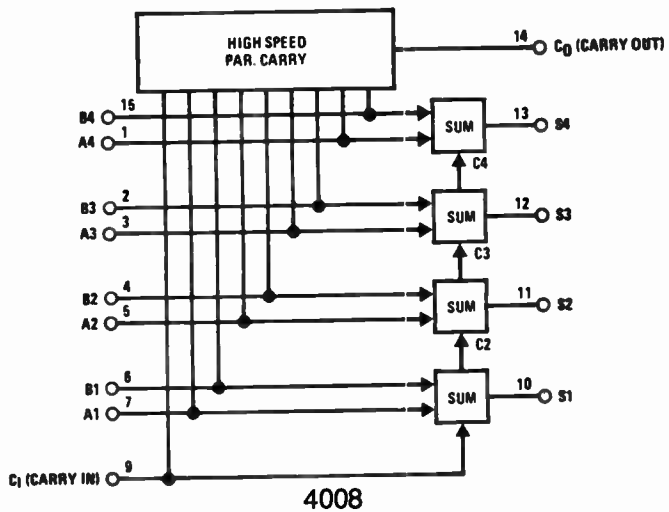


4007

4008 4-BIT FULL ADDER

The 4008 consists of four full-adder stages with fast look ahead carry provision from stage to stage. Circuitry is included to provide a fast parallel carry out bit to permit high-speed operation in arithmetic sections using several 4008Bs. 4008B inputs include the four sets of bits to be added, A1 to A4 and B1 to B4, in addition to the carry in bit from a previous section. 4008B outputs include the four sum bits, S1 and S4, in addition to the high-speed parallel carry out which may be utilized at a succeeding CD4008B section. All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and GND.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**
Quiescent Current	**15V**
Maximum Input Leakage	**1μA at 15V**



4008

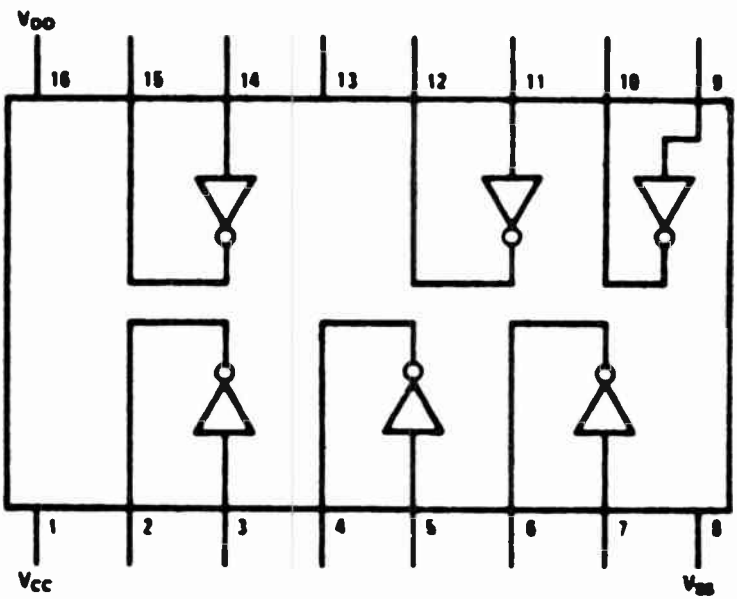
A_i	B_i	C_i	CO	SUM
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

Truth Table
4008

4009 HEX BUFFER (INVERTING)

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits. The N-channel and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge. These gates may be used as hex buffers, CMOS to DTL or TTL interface, or as CMOS current drivers. Conversion ranges are from 3 to 15 volts providing $V_{CC} \leq V_{DD}$.

Supply Voltage Range	**3V to 15V**
Power	**100 nW (typical)**
Noise Immunity	**0.45 V_{DD} (typical)**
Current Sinking Capability	**8 mA (min) at V_O = 0.5V and V_{DD} = 10V**

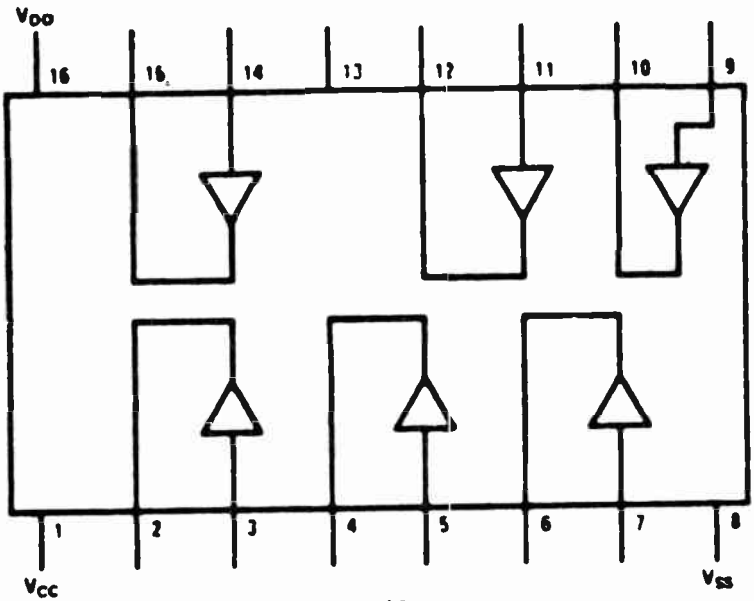


4009

4010 HEX BUFFER (NONINVERTING)

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits. The N-channel and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge. These gates may be used as hex buffers, CMOS to DTL or TTL interface, or as CMOS current drivers. Conversion ranges are from 3 to 15 volts providing $V_{CC} \leq V_{DD}$.

Supply Voltage Range	**3V to 15V**
Power	**10 nW (typical)**
Noise Immunity	**0.45V_{DD} (typical)**
Current Sinking Capability	**8 mA (min) at V_O = 0.5V and V_{DD} = 10V**

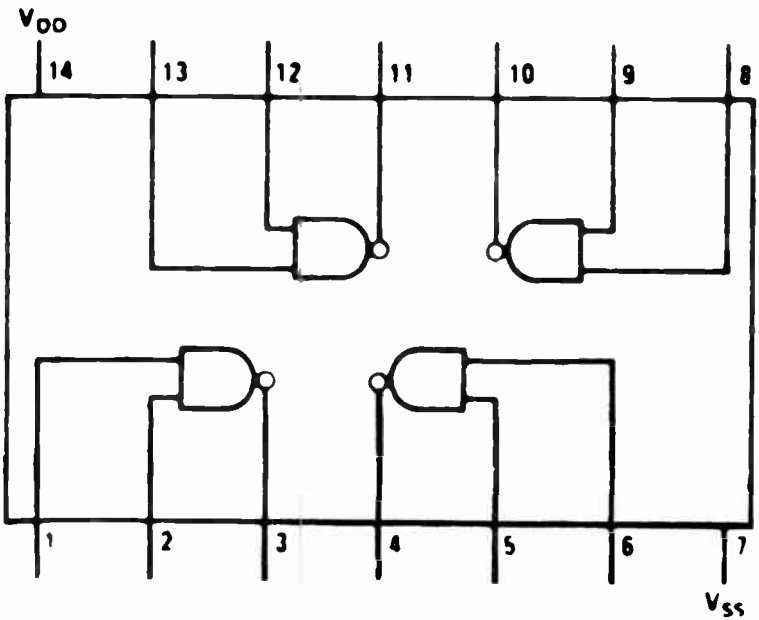


4010

4011 QUAD 2-INPUT NAND GATE

These NAND gates are monolithic complementary MOS (CMOS) integrated circuits. The N-channel and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Supply Voltage Range	**3V to 15V**
Power	**10 nW(typical)**
Noise Immunity	**0.45 V_{DD}(typical)**

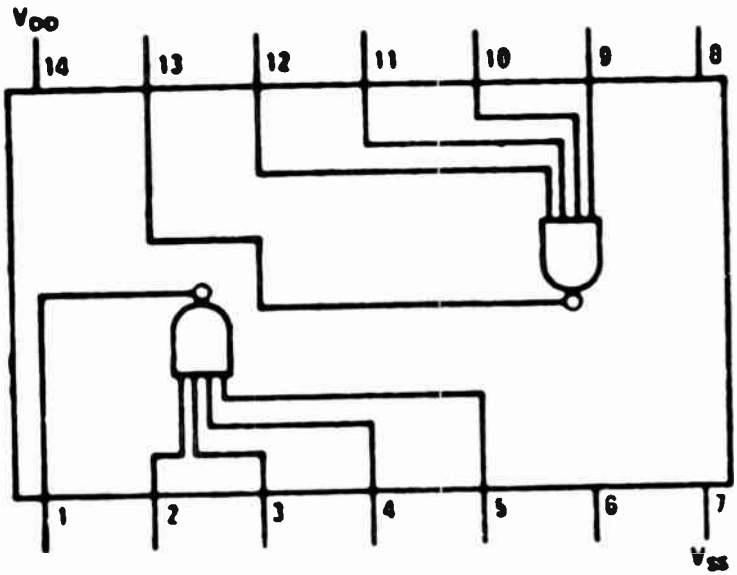


4011

4012 DUAL 4-INPUT NAND GATE

These NAND gates are monolithic complementary MOS (CMOS) integrated circuits. The N-channel and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Supply Voltage Range	**3V to 15V**
Power	**10 nW (typical)**
Noise Immunity	**0.45 V_{DD} (typical)**

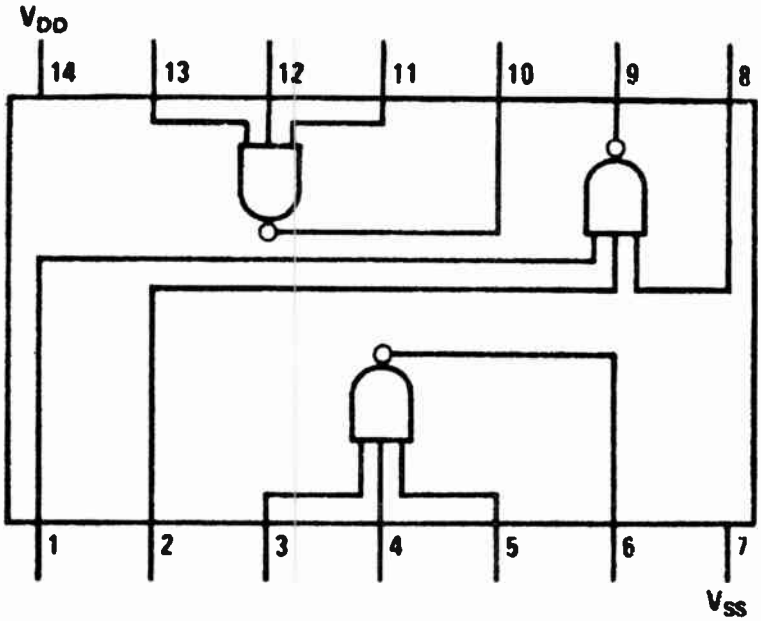


4012

4023 TRIPLE 3-INPUT NAND GATE

These NAND gates are monolithic complementary MOS (CMOS) integrated circuits. The N-channel and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Supply Voltage Range	**3V to 15V**
Power	**10 nW (typical)**
Noise Immunity	**0.45 V_{DD} (typical)**

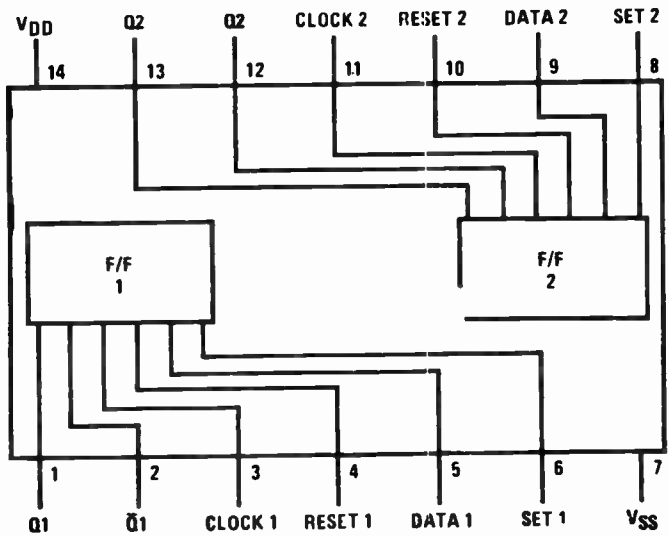


4023

4013 BM DUAL D FLIP-FLOP

The 4013 dual D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N-channel and P-channel enhancement transistors. Each flip-flop has independent data, set, reset and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

Supply Voltage Range — **3V to 15V**
Noise Immunity — **0.45 V_{DD} typ.**
TTL Compatibility — **Fanout of 2 driving 74L or 1 driving 74LS**



4013

CL↑	D	R	S	Q	$\overline{Q}$
⌐‾	0	0	0	0	1
⌐‾	1	0	0	1	0
‾⌐	x	0	0	Q	$\overline{Q}$
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	1	1

Truth Table
4013

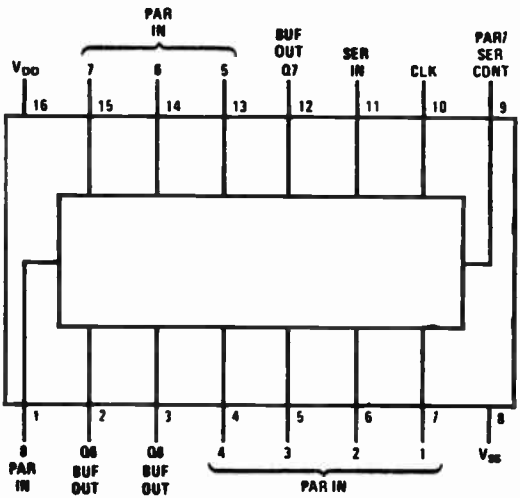
No change
↑ = Level change
x = Don't care case

4014 8-STAGE STATIC SHIFT REGISTER

The 4014 is an 8-stage parallel input/serial output shift register. A parallel/serial control input enables individual jam inputs to each of 8 stages. Q outputs are available from the sixth, seventh and eighth stages.

When the parallel/serial control input is in the logical 0 state, data is serially shifted into the register synchronously with the positive transition of the clock. When the parallel/serial control input is in the logical 1 state, data is jammed into each stage of the register synchronously with the positive transition of the clock.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 Vcc to typ.**
Speed of Operation	**5 MHz typ.**



4014

CL*	SERIAL INPUT	PARALLEL/ SERIAL CONTROL	PI 1	PI n	Q1 (INTERNAL)	Q_n	
⌐	X	1	0	0	0	0	
⌐	X	1	1	0	1	0	
⌐	X	1	0	1	0	1	
⌐	X	1	1	1	1	1	
⌐	0	0	X	X	0	Q_{n-1}	
⌐	1	0	X	X	1	Q_{n-1}	
⌐	X	X	X	X	Q1	Q_n	NO CHANGE

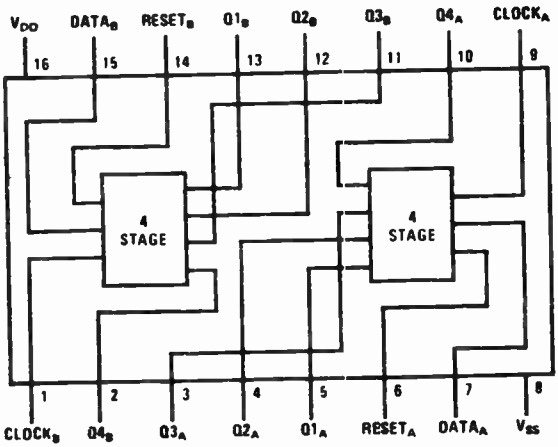
Truth Table
4014

*LEVEL CHANGE X DON'T CARE CASE

4015 DUAL 4-BIT STATIC REGISTER

The 4015 consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent clock and reset inputs, as well as a single serial data input. Q outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the data input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to eight stages using one 4015 package, or to more than eight stages using additional 4015 is possible. All inputs are protected from static discharge by diode clamps to V_{DD} and Vss.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{CC} typ.**
Speed of Operation	**9 MHz (typ.) clock rate at V_{DD} – Vss = 10V**



4015

CL*	D	R	Q1	Q_n	
⌐	0	0	0	Q_{n+1}	
⌐	1	0	1	Q_{n+1}	
⌐	X	0	Q1	Q_n	(No change)
X	X	1	0	0	

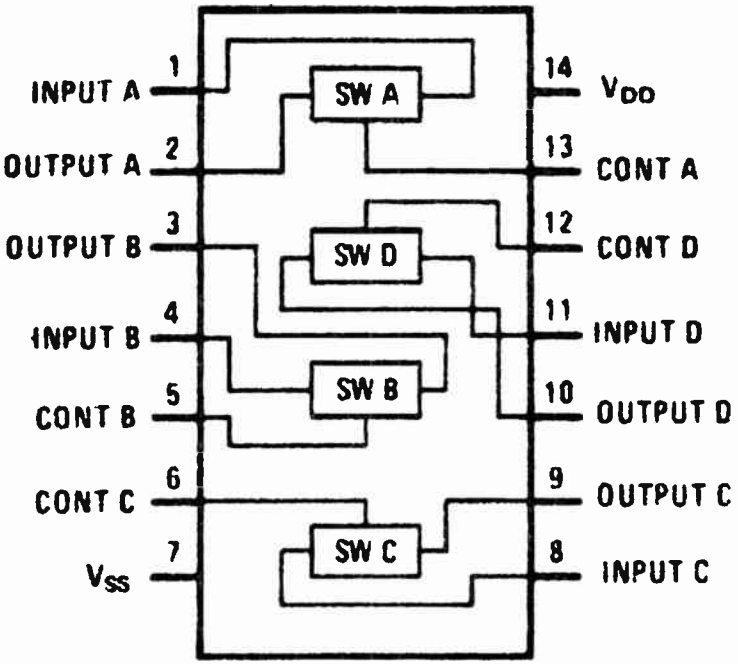
Truth Table
4015

* Level change.
X Don't care case.

4016 QUAD BILATERAL SWITCH

The 4016 is a quad bilateral switch that utilizes P-channel and N-channel complementary MOS (CMOS) circuits to provide an extremely high off resistance and low on resistance switch. The switch will pass signals in either direction and is extremely useful in digital switching.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{CC} typ.**
Digital and Analog Levels	**$\pm$ 7.5 V_{peak}**
On Resistance	**300Ω typ.**
	$V_{DD} - V_{DD} = 15V$
Switch Characteristics	**$\Delta R_{ON} = 40\Omega$ typ.**
On/Off Output	**65 dB typ.**
Voltage Ratio	**@ $f_{is} = 10$ kHz $R_L = 10k$**
Linearity	**.5% distortion typ.**
	@ $f_{is} = 1$ kHz
Leakage	**$V_{is} = 5\ V_{p-p}$**
	$V_{DD} - V_{SS} = 10V$
	$R_L = 10$ kΩ



4016

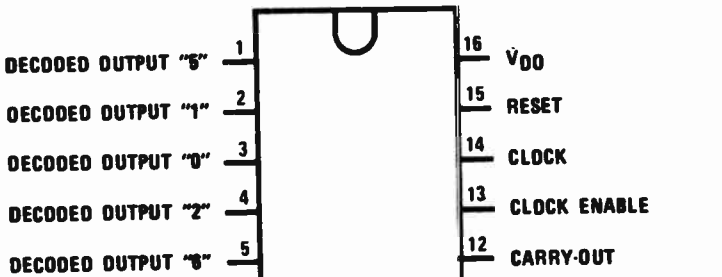
4017 DECADE COUNTER/DIVIDER WITH 10 DECODED OUTPUTS

The 4017 is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry-out bit. The 4022 is a 4-stage divide-by-8 Johnson counter with eight decoded outputs and a carry-out bit.

These counters are cleared to their zero count by a logical 1 on their reset line. These counters are advanced on the positive edge of the clock signal when the clock enable signal is in the logical 0 state.

The configuration of the 4017 and 4022 permits medium-speed operation and assures a hazard free counting sequence. The 10/8 decoded outputs are normally in the logical 0 state and go to the logical 1 state only at their respective time slot. Each decoded output remains high for one full clock cycle. The carry out signal completes a full cycle for every 10/8 clock input cycles and is used as a ripple carry signal to any succeeding stages.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**
Speed of Operation	**5.0 MHz typ. with 10V V_{DD}**
Power	**10μ W typ.**



4017

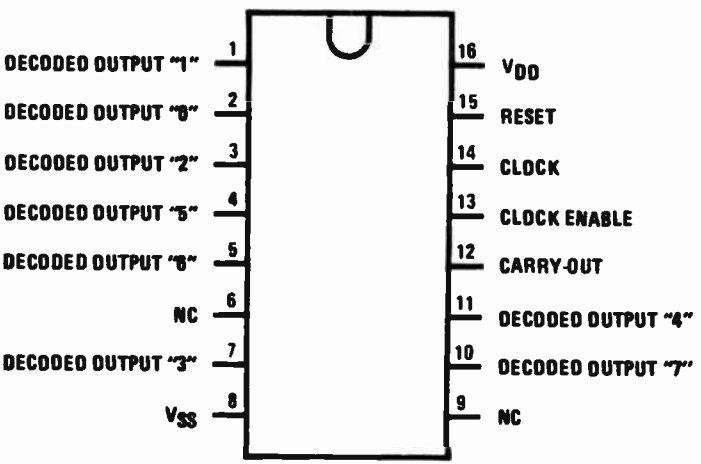
4022 DIVIDE-BY-8 COUNTER/DIVIDER WITH 8 DECODED OUTPUTS

The 4017 is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry-out bit. The 4022 is a 4-stage divide-by-8 Johnson counter with eight decoded outputs and a carry-out bit.

These counters are cleared to their zero count by a logical 1 on their reset line. These counters are advanced on the positive edge of the clock signal when the clock enable signal is in the logical 0 state.

The configuration of the 4017 and 4022 permits medium-speed operation and assures a hazard free counting sequence. The 10/8 decoded outputs are normally in the logical 0 state and go to the logical 1 state only at their respective time slot. Each decoded output remains high for one full clock cycle. The carry out signal completes a full cycle for every 10/8 clock input cycles and is used as a ripple carry signal to any succeeding stages.

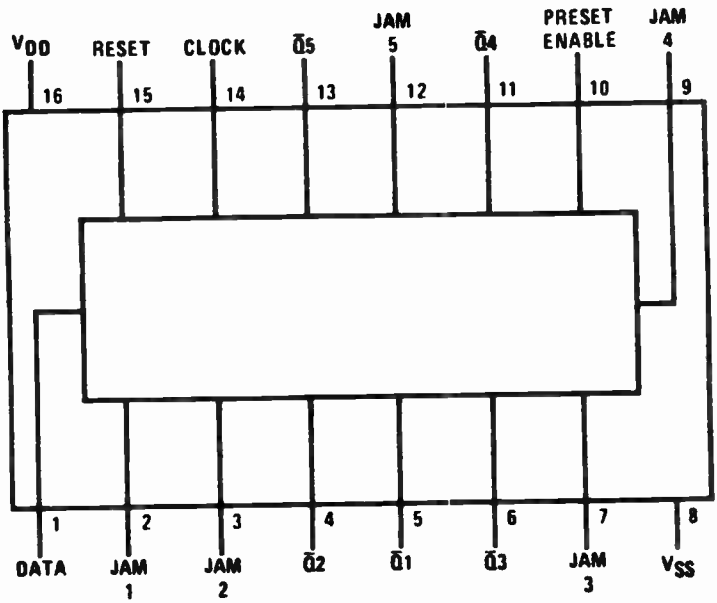
Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**
Speed of Operation	**5.0 MHz typ. with 10V V_{DD}**
Power	**10μ W typ.**



4018 PRESETTABLE DIVIDE-BY-N COUNTER

The 4018B consists of five Johnson counter stages. A buffered $\overline{Q}$ output from each stage, clock, reset, data, preset enable and five individual jam inputs are provided. The counter is advanced one count at the positive clock signal transition. A high reset signal clears the counters to an all zero condition. A high preset enable signal allows information on the jam inputs to preset the counter. Antilock gating is provided to assure the proper counting sequence.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**

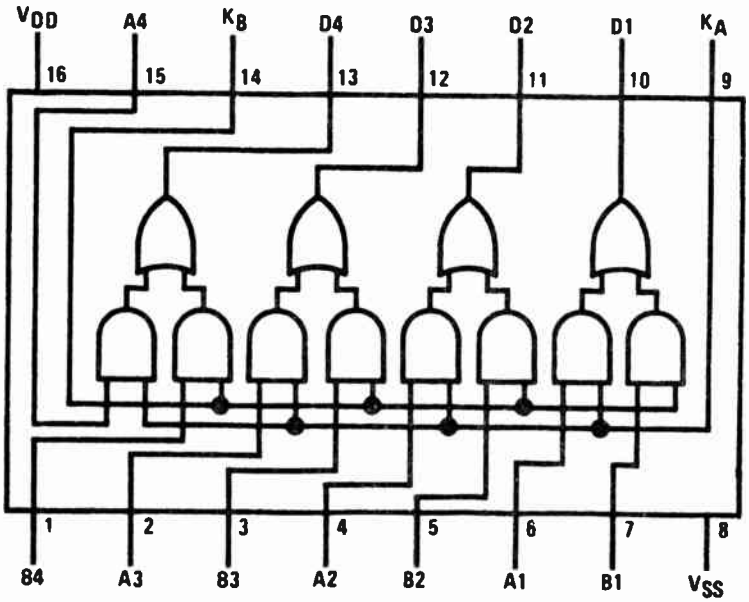


4018

4019 QUAD AND-OR SELECT GATE

The 4019 is a complementary MOS quad AND-OR select gate. Low power and high noise margin over a wide voltage range is possible through implementation of N-channel and P-channel enhancement mode transistors. These complementary MOS (CMOS) transistors provide the building blocks for the 4 AND-OR select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_A and K_B. All inputs are protected against static discharge damage.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Driving 74L or 1 driving 74LS**

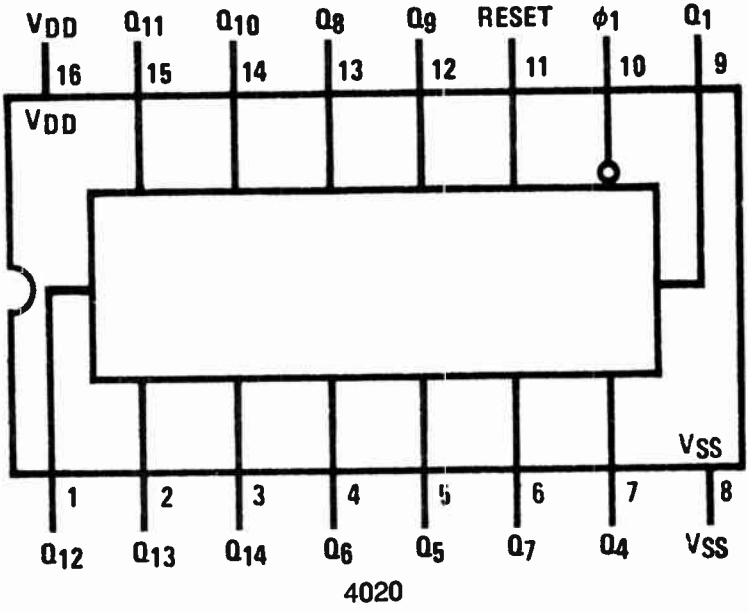


4019

4020 14-STAGE RIPPLE CARRY BINARY COUNTERS

The 4020 and 4060 are 14-stage ripple carry binary counters, and the 4040BM/4040BC is a 12-stage ripple carry binary counter. The counters are advanced one count on the negative transition of each clock pulse. The counters are reset to the zero state by a logical 1 at the reset input independent of clock.

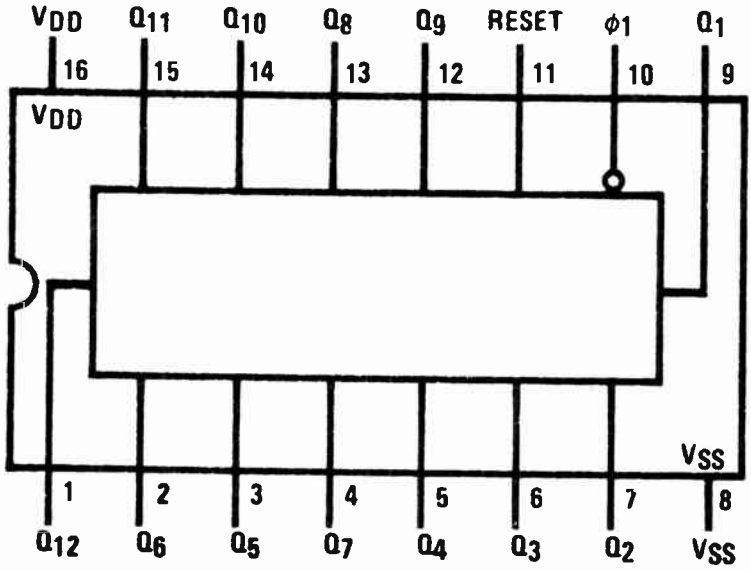
Supply Voltage Range	**1V to 15V**
Noise Immunity	**0.45V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**
Speed of Operation	**8MHz typ. at V_{DD} = 10V**



4040 14-STAGE RIPPLE CARRY BINARY COUNTERS

The 4020 and 4060 are 14-stage ripple carry binary counters, and the 4040BM/4040BC is a 12-stage ripple carry binary counter. The counters are advanced one count on the negative transition of each clock pulse. The counters are reset to the zero state by a logical 1 at the reset input independent of clock.

Supply Voltage Range	**1V to 15V**
Noise Immunity	**0.45V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**
Speed of Operation	**8MHz typ. at V_{DD} = 10V**

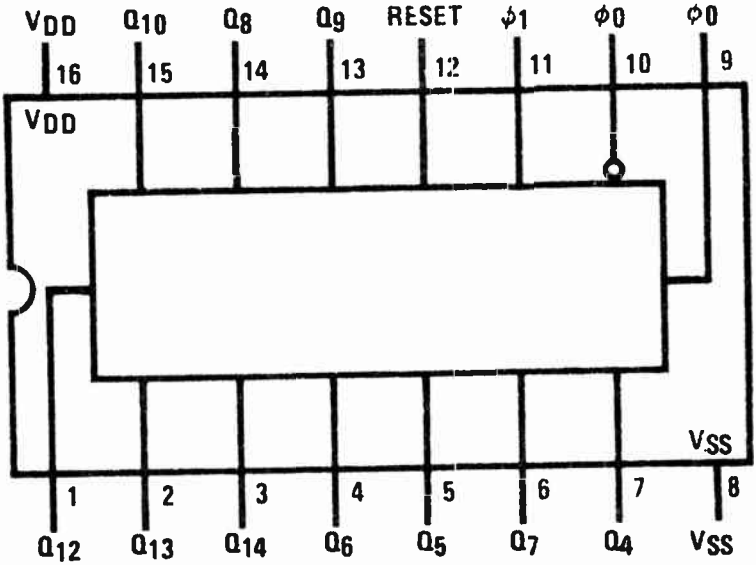


4040

4060 12-STAGE RIPPLE CARRY BINARY COUNTERS

The 4020 and 4060 are 14-stage ripple carry binary counters, and the 4040BM/4040BC is a 12-stage ripple carry binary counter. The counters are advanced one count on the negative transition of each clock pulse. The counters are reset to the zero state by a logical 1 at the reset input independent of clock.

Supply Voltage Range	**1V to 15V**
Noise Immunity	**0.45V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**
Speed of Operation	**8MHz typ. at V_{DD} = 10V**



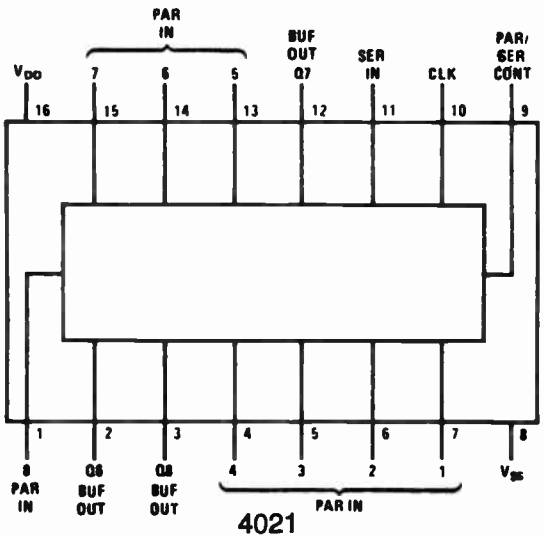
4060

4021 8-STAGE STATIC SHIFT REGISTER

The 4021 is an 8-stage parallel input/serial output shift register. A parallel/serial control input enables individual jam inputs to each of 8 stages. Q outputs are available from the sixth, seventh and eighth stages.

When the parallel/serial control input is in the logical 0 state, data is serially shifted into the register synchronously with the positive transition of the clock. When the parallel/serial control is in the logical 1 state, data is jammed into each stage of the register asynchronously with the clock.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{CC} typ.**
Speed of Operation	**5 MHz typ.**



CL*	SERIAL INPUT	PARALLEL/ SERIAL CONTROL	PI 1	PI n	Q1 (INTERNAL)	Q_n	
X	X	1	0	0	0	0	
X	X	1	0	1	0	1	
X	X	1	1	0	1	0	
X	X	1	1	1	1	1	
⌐	0	0	X	X	0	Q_{n-1}	
⌐	1	0	X	X	1	Q_{n-1}	
⌐	X	0	X	X	Q1	Q_n	NO CHANGE

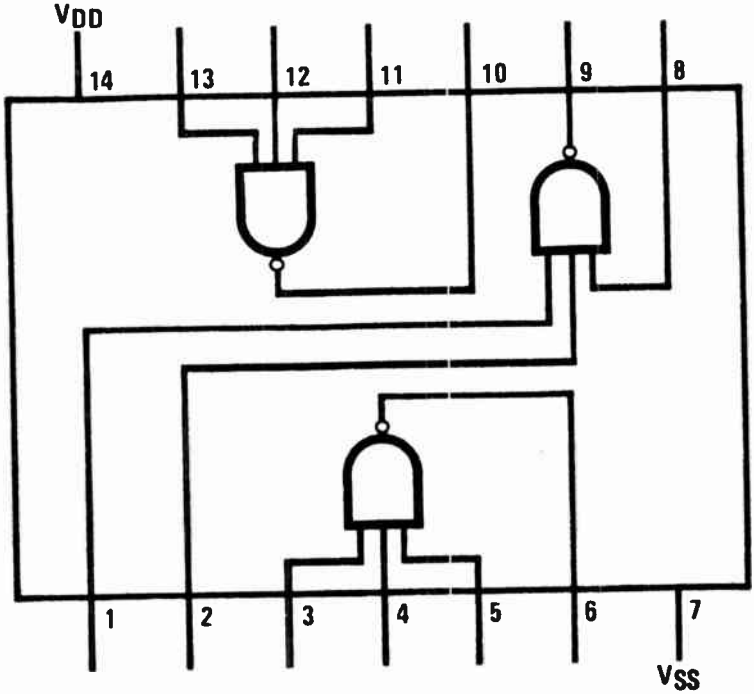
* ⌐ LEVEL CHANGE X DON'T CARE CASE

Truth Table 4021

4023 TRIPLE 3-INPUT NAND GATE

These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs that improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and Vss.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**
Maximum Input Leakage	**1 μA at 15V**

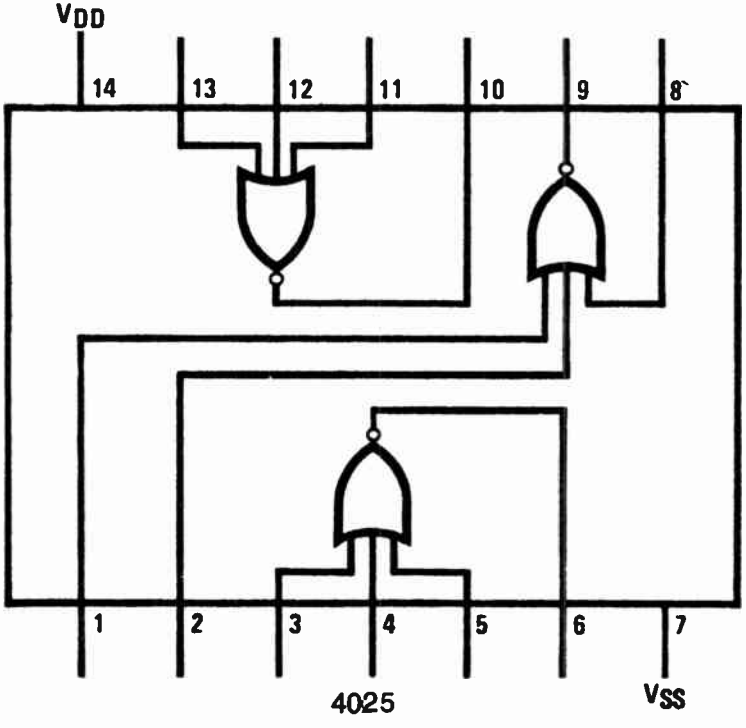


4023

4025 TRIPLE 3-INPUT NOR GATE

These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs that improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and Vss.

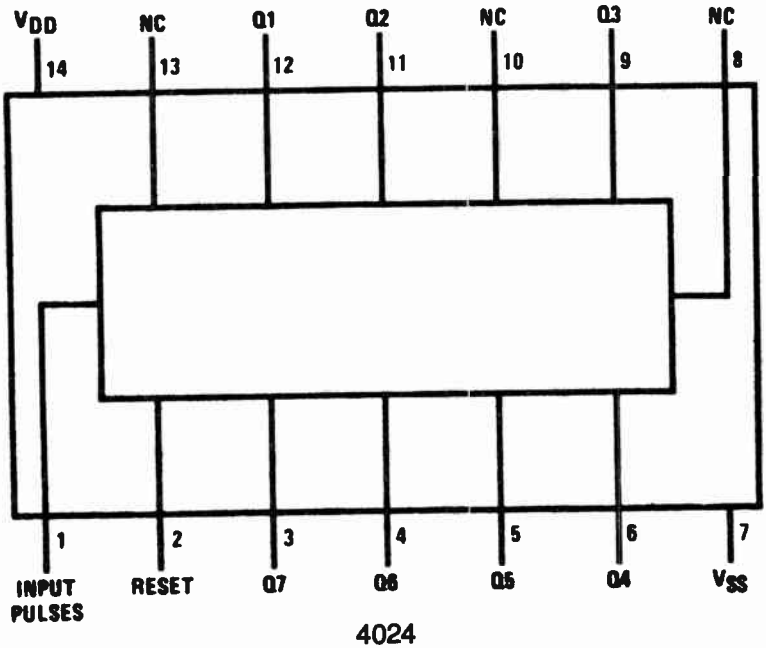
Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**
Maximum Input Leakage	**1 μA at 15V**



4024 7-STAGE RIPPLE-CARRY BINARY COUNTER

The 4024 is a 7-stage ripple-carry binary counter. Buffered outputs are externally available from stages 1 through 7. The counter is reset to its logical 0 state by a logical 1 on the reset input. The counter is advanced one count on the negative transition of each clock pulse.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**
Speed	**12 MHz (typ.) input pulse rate $V_{DD} - V_{SS} = 10V$**

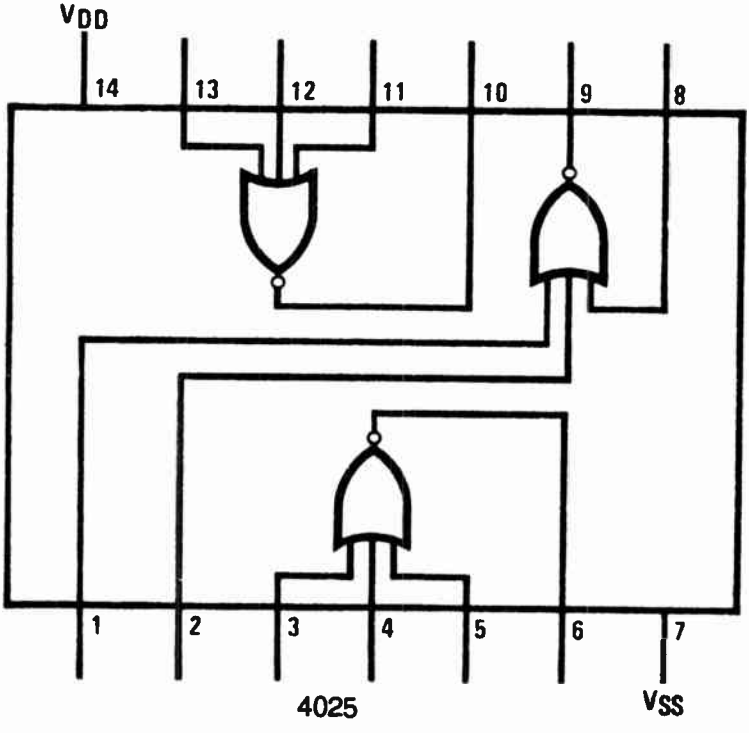


4024

4025 TRIPLE 3-INPUT NOR GATE

These NOR gates are monolithic complementary MOS (CMOS) integrated circuits. The N-channel and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Supply Voltage Range	**3V to 15V**
Power	**10 nW (typ.)**
Noise Immunity	**0.45 V_{DD} (typ.)**
Speed of Operation	**25 ns (typ.) at C_L = 15 pF**



Truth Table

$^{\bullet}t_{n-1}$ INPUTS						$^{\blacklozenge}t_n$ OUTPUTS		
CL▲	J	K	S	R	Q	Q	$\overline{Q}$	
⎍	1	X	0	0	0	1	0	
⎍	X	Q	0	0	1	1	0	
⎍	0	X	0	0	0	0	1	
⎍	X	1	0	0	1	0	1	
⎎	X	X	0	0	X			(No change)
X	X	X	1	0	X	1	0	
X	X	X	0	1	X	0	1	
X	X	X	1	1	X	1	1	

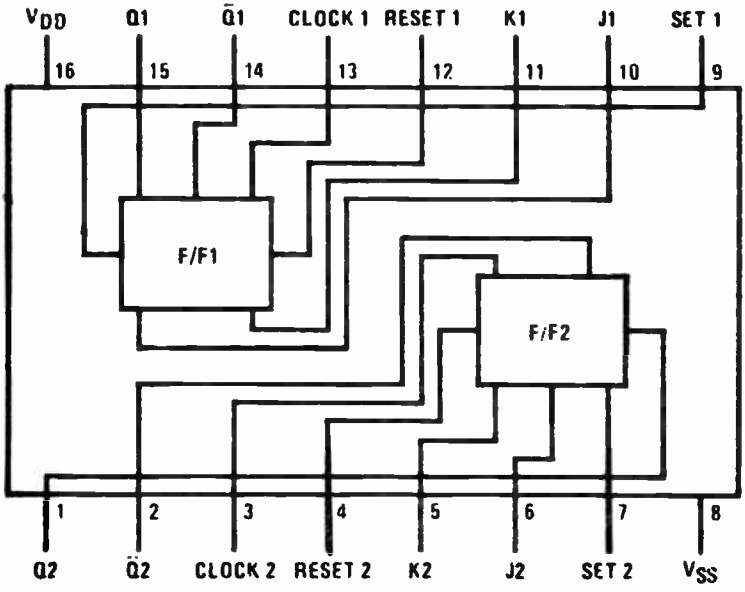
4027

1 = High Level
0 = Low Level
▲ = Level Change
X = Don't Care
● = t_{n-1} refers to the time interval prior to the positive clock pulse transition
◆ = t_n refers to the time intervals after the positive clock pulse transition

4027 DUAL JK MASTER/SLAVE FLIP-FLOP

These dual JK flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. Each flip-flop has independent J, K, set, reset and clock inputs and buffered Q and $\overline{Q}$ outputs. These flip-flops are edge-sensitive to the clock input and change state on the positive-going transition of the clock pulses. Set or reset is independent of the clock and is accomplished by a high level on the respective input. All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and Vss.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**
Power	**50 nW typ.**
Speed of Operation	**12 MHz typ. with 10V supply**

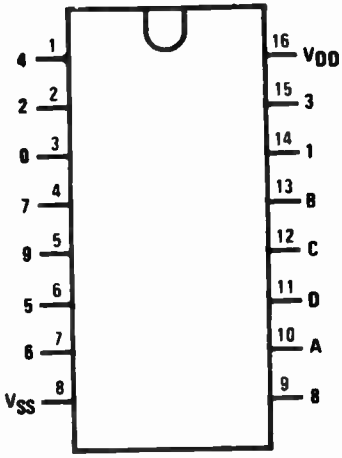


4027

4028 BCD-TO-DECIMAL DECODER

The 4028 is a BCD-to-decimal or binary-to-octal decoder consisting of four inputs, decoding logic gates and 10 output buffers. A BCD code applied to the four inputs, A, B, C and D, results in a high level at the selected one-of-10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A, B and C is decoded in octal at outputs 0-7. A high-level signal at the D input inhibits octal decoding and causes outputs 0-7 to go low. All inputs are protected against static discharge damage by diode clamps to V_{DD} and V_{SS}.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**
Power	



4028

Truth Table 4028

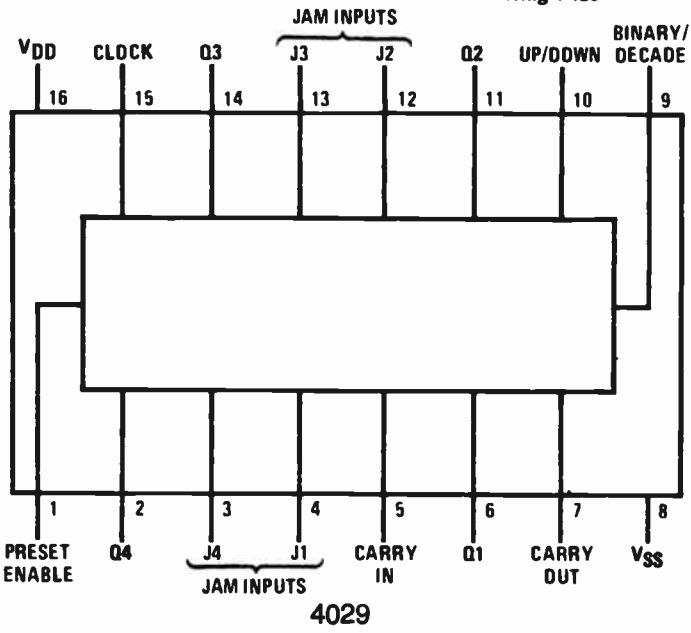
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1

4029 PRESETTABLE BINARY/DECADE UP/DOWN COUNTER

The 4029 is a presettable up/down counter that counts in either binary or decade mode depending on the voltage level applied at binary/decade input. When binary/decade is at logical 1, the counter counts in binary; otherwise, it counts in decade. Similarly, the counter counts up when the up/down input is at logical 1 and vice versa.

A logical 1 preset enable signal allows information at the jam inputs to preset the counter to any state asynchronously with the clock. The counter is advanced one count at the positive-going edge of the clock if the carry in and preset enable inputs are at logical 0. Advancement is inhibited when either or both of these two inputs is at logical 1. The carry out signal is normally at the logical 1 state and goes to the logical 0 state when the counter reaches its maximum count in the up mode or the minimum count in the down mode, provided the carry input is at logical 0 state. All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**

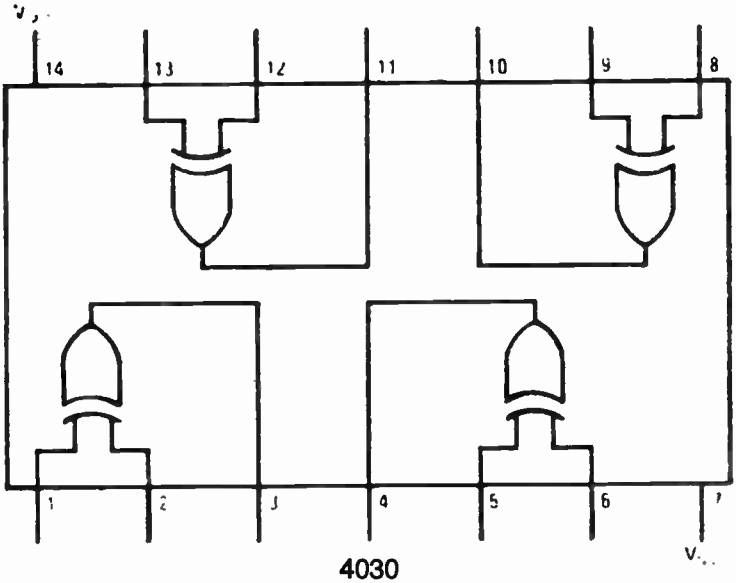


4029

4030 QUAD EXCLUSIVE-OR GATE

These Exclusive-OR gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to V_{DD} and Vss.

Supply Voltage Range	**3V to 15V**
Power	**100 nW (typ.)**
Speed of Operation	**40 ns (typ.)**
Noise Immunity	**0.45 V_{CC} (typ.)**



4030

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Truth Table 4030
Where: "1" = High Level
"0" = Low Level

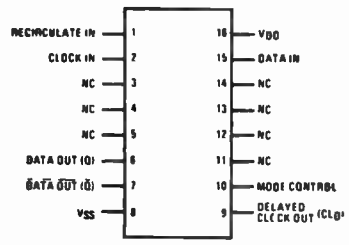
4031 64-STAGE STATIC SHIFT REGISTER

The 4031 is an integrated, complementary MOS (CMOS), 64-stage, fully static shift register. Two data inputs, data in and recirculate in, and a mode control input are provided. Data at the data input (when mode control is LOW) or data at the recirculate input (when mode control is HIGH), which meets the setup and hold time requirements, are entered into the first stage of the register and are shifted one stage at each positive transition of the clock.

Data output is available in both true and complement forms from the 64th stage. Both the data out (Q) and data out ($\overline{Q}$) outputs are fully buffered.

The clock input of the 4031BM/4031BC is fully buffered and presents only a standard input load capacitance. However, a delayed clock output (CL_D) allows reduced clock drive fanout and transition time requirements when cascading packages.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**
Range Of Operation	**DC to 8 MHz (typical @ V_{DD} = 10V)**
Clock Input	**5pF (typ.) Input Capacitance**
High Current Sinking Capability, Q Output	**1.6mA @ V_{DD} = 5V and 25 ° C**



4031

MODE CONTROL (data selection)

MODE CONTROL	DATA IN	RECIRCULATE IN	DATA INTO FIRST STAGE
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

EACH STAGE

O_n	CL	O_n
0	⌐	0
1	⌐	1
X	¬	NC

X = irrelevant
NC = no change
⌐ = Low to High level transition
¬ = High to Low level transition

Truth Tables 4031

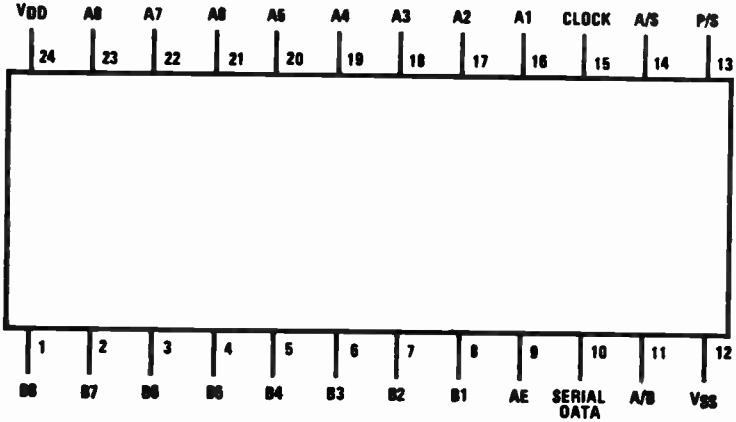
4034 8-STAGE 3-STATE BIDIRECTIONAL PARALLEL/SERIAL INPUT/OUTPUT BUS REGISTER

The 4034 is an 8-bit CMOS static shift register with two parallel bidirectional data ports (A and B) which, when combined with serial shifting operations, can be used to bidirectionally transfer parallel data between two buses, convert serial data to parallel form and direct them to either of two buses, store (recirculate) parallel data, or accept parallel data from either of two buses and convert them to serial form. These operations are controlled by five control inputs:

- A enable (AE)—A data port is enabled only when AE is at logical 1. This allows the use of a common bus for multiple packages.
- A-bus-to-B-bus/B-bus-to-A-bus (A/B)—This input controls the direction of data flow. When at logical 1, data flows from port A to B (A is input and B is output). When at logical 0, the data flow direction is reversed.
- Asynchronous/synchronous (A/S)—When A/S is at logical 0, data transfer occurs at positive transition of the clock. When A/S is at logical 1, data transfer is independent of the clock for parallel operation. In the serial mode, A/S input is internally disabled such that the operation is always synchronous. Asynchronous serial operation is not possible.
- Parallel/serial (P/S)—A logical 1 P/S input allows data transfer into the registers via A or B port (synchronous if A/S = logical 0 and asynchronous if A/S = logical 1). A logical 0 P/S allows serial data to transfer into the register synchronously with the positive transistion of the clock, independent of the A/S input.
- Clock—Single phase, enabled only in synchronous mode. Either P/S = logical 1 and A/S = logical 0 or P/S = logical 0.

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave. All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Supply Voltage Range	**3V to 18V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**



4034

4035 4-BIT PARALLEL-IN/PARALLEL-OUT SHIFT REGISTER

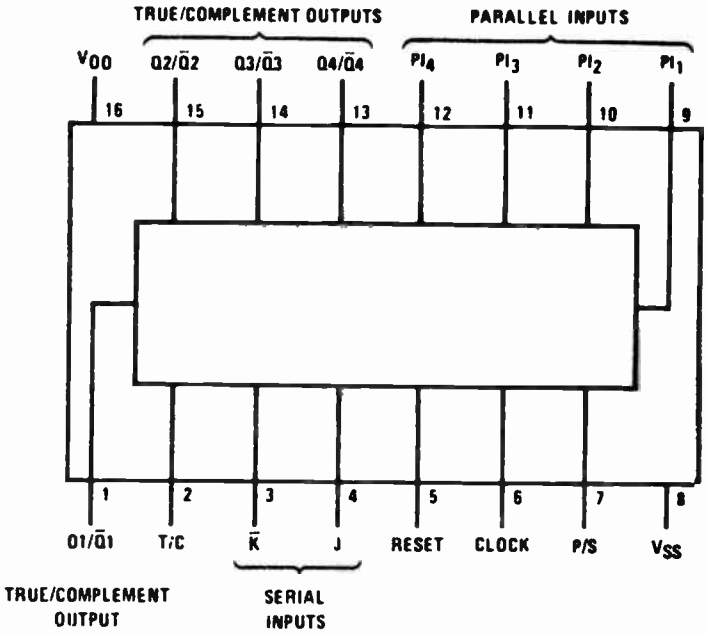
The 4035 4-bit parallel-in/parallel-out shift register is a monolithic complementary MOS (CMOS) integrated circuit constructed with P-channel and N-channel enhancement mode transistors. This shift register is a 4-stage clocked serial register that has provisions for synchronous parallel inputs to each stage and serial inputs to the first stage via $J\overline{K}$ logic. Register stages 2, 3 and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (parallel/serial control LOW).

Parallel entry via the D line of each register stage is permitted only when the parallel/serial control is HIGH. In the parallel or serial mode, information is transferred on positive clock transistions.

When the true/complement control is HIGH, the true contents of the register are available at the output terminals. When the true/complement control is LOW, the outputs are the complements of the data in the register. The true/complement control functions asynchronously with respect to the clock signal.

$J\overline{K}$ input logic is provided on the first stage serial input to minimize logic requirements, particularly in counting and sequence-generation applications. With $J\overline{K}$ inputs connected together, the first stage becomes a D flip-flop. An asynchronous common reset is also provided.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Famout of 2 driving 74L or 1 driving 74LS**
Power Dissipation	**5μ W typ. (ceramic)**
Speed	**To 5 MHz**



4035

Truth Table

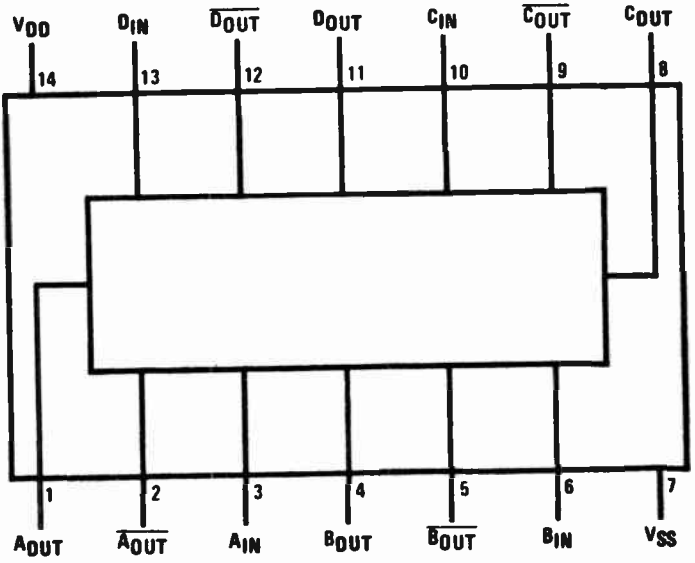
C_L	$t_n - 1$ (INPUTS)				t_n (OUTPUTS)
	J	$\overline{K}$	R	$Q_n - 1$	Q_n
⎍	0	X	0	0	0
⎍	1	X	0	0	1
⎍	X	0	0	1	0
⎍	1	0	0	Q_{n-1}	$\overline{Q_{n-1}}$ TOGGLE MODE
⎍	X	1	0	1	1
⎎	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

4035

4041 QUAD TRUE/COMPLEMENT BUFFER

The 4041 is a quad true/complement buffer consisting of N-channel and P-channel enhancement mode transistors that have low-channel resistance and high current (sourcing and sinking) capability. The 4041 is intended for use as a buffer, line driver, or CMOS-to-TTL driver. All inputs are protected from static discharge by diode clamps to V_{DD} and Vss.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**40% V_{DD} typ.**
True Output:	
High Current Source and Sink Capability	**8 mA (typ.) @ V_O = 9.5V, V_{DD} = 10V** **3.2 mA (typ.) @ V_O = 0.4V, V_{DD} = 5V (two TTL loads)**
Complement Output:	**Medium current source and sink capability** **3.6 mA (typ.) @ V_O = 9.5V, V_{DD} = 10V** **1.6 mA (typ.) @ V_O = 0.4V, V_{DD} = 5V**

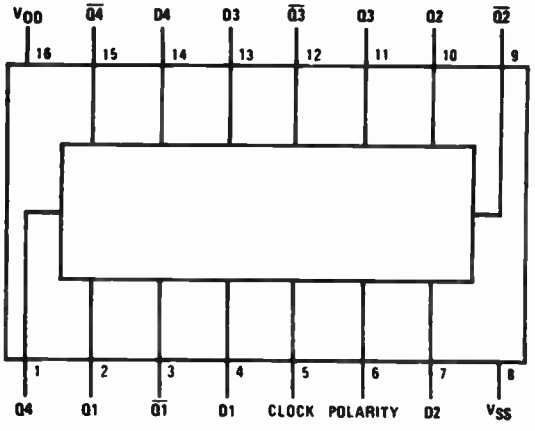


4041

4042 QUAD CLOCKED D LATCH

The 4042 quad clocked D latch is a monolithic complementary MOS (CMOS) integrated circuit constructed with P-channel and N-channel enhancement mode transistors. The outputs Q and $\overline{Q}$ either latch or follow the data input depending on the clock level which is programmed by the polarity input. For polarity equal to 0, the information present at the data input is transferred to Q and $\overline{Q}$ during 0 clock level. For polarity equal to 1, the transfer occurs during the 1 clock level. When a clock transition occurs (positive for polarity equal to 0 and negative for polarity equal to 1), the information present at the input during the clock transition is retained at the outputs until an opposite clock transition occurs.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**



4042

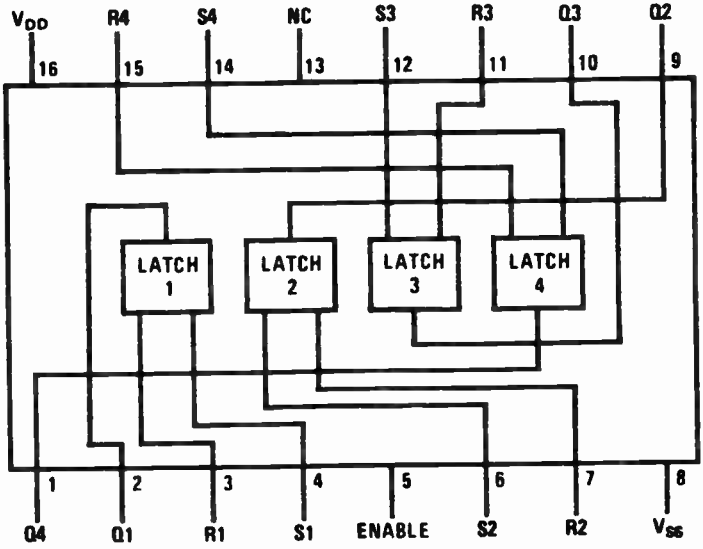
CLOCK	POLARITY	Q
0	0	D
⌜	0	Latch
1	1	D
⌞	1	Latch

Truth Table
4042

4043 QUAD 3-STATE NOR R/S LATCHES

The 4043 is a quad cross-coupled 3-state CMOS NOR latch, and CD4044 is a quad cross-coupled 3-state CMOS NAND latch. Each latch has a separate Q output and individual set and reset inputs. It has a common 3-state enable input for all four latches. A logic 1 on the enable input connects the latch states to the Q outputs. A logic 0 on the enable input disconnects the latch states from the Q outputs resulting in an open circuit condition on the Q outputs. The 3-state feature allows common bussing of the outputs.

Supply Voltage Range	**3V to 15V**
Power	**100 nW typ.**
Noise Immunity	**0.45 V_{DD} typ.**



4043

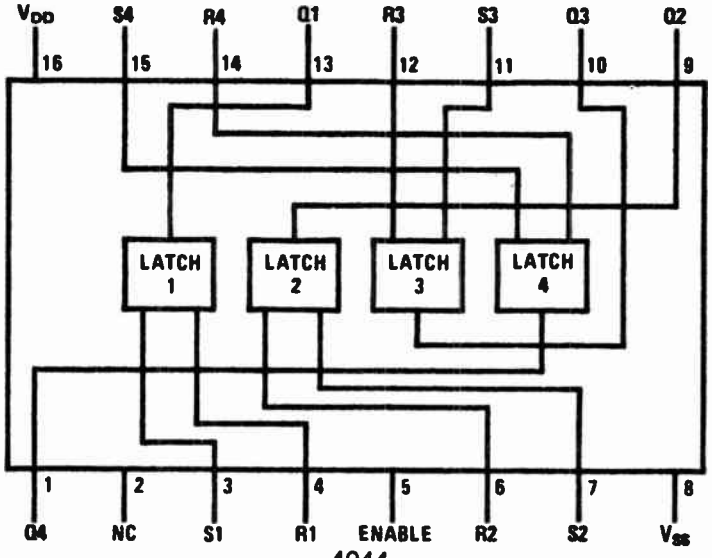
S	R	E	Q
X	X	0	OC
0	0	1	NC
1	0	1	1
0	1	1	0
1	1	1	Δ

Truth Table
4043

4044 QUAD 3-STATE NAND R/S LATCHES

The 4043 is a quad cross-coupled 3-state CMOS NOR latch, and CD4044 is a quad cross-coupled 3-state CMOS NAND latch. Each latch has a separate Q output and individual set and reset inputs. It has a common 3-state enable input for all four latches. A logic 1 on the enable input connects the latch states to the Q outputs. A logic 0 on the enable input disconnects the latch states from the Q outputs resulting in an open circuit condition on the Q outputs. The 3-state feature allows common bussing of the outputs.

Supply Voltage Range	**3V to 15V**
Power	**100 nW typ.**
Noise Immunity	**0.45 V_{DD} typ.**



4044

S	R	E	Q
X	X	0	OC
1	1	1	NC
0	1	1	1
1	0	1	0
0	0	1	ΔΔ

Truth Table 4044

OC – TRI-STATE
NC – No change
X – Don't care
Δ – Dominated by S=1 input
ΔΔ – Dominated by R=0 input

4046 MICROPOWER PHASE-LOCKED LOOP

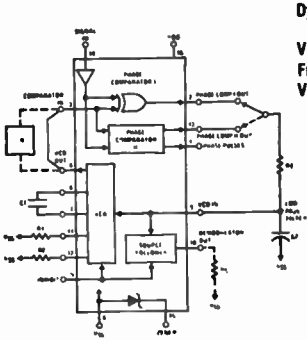
The 4046 micropower phase-locked loop (PLL) consists of a low-power, linear, voltage-controlled oscillator (VCO), a source follower, a zener diode and two phase comparators. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

Phase comparator 1, an exclusive OR gate, provides a digital error signal (phase comparator 1 out) and maintains 90-degree shifts at the VCO center frequency. Between signal input and comparator input (both at 50-percent duty cycle), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator 11 is an edge-controlled digital memory network. It provides a digital error signal (phase comparator 11 out) and lock-in signal (phase pulses) to indicate a locked condition and maintains a 0-degree phase shift between signal input and comparator input. The linear voltage-controlled oscillator (VCO) produces an output signal (VCO out) whose frequency is determined by the voltage at the VCO_{IN} input and the capacitor and resistors connected to pin $C1_A$, $C1_B$, R1 and R2.

The source follower output of the VCO_{IN} (demodulator out) is used with an external register of 10KΩ or more. The inhibit input, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode is provided for power-supply regulation, if necessary.

Supply Voltage Range	**3V to 18V**
Dynamic Power Consumption	**70μ W (typ.) at f_o = 10 kHz, V_{DD} = 5V**
VCO Frequency	**1.3 MHz (typ.) at V_{DD} = 10V**
Frequency Drift	**0.06%/°C at V_{DD} = 10V**
VCO Linearity	**1% (typ.)**



4046

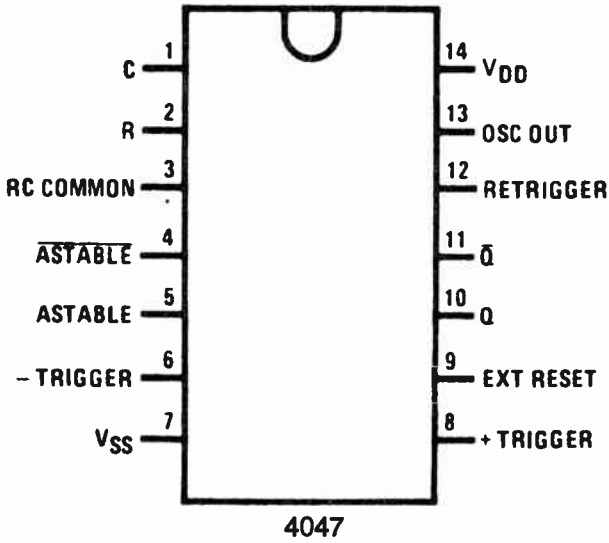
4047 LOW-POWER MONOSTABLE/ASTABLE MULTIVIBRATOR

The 4047 is capable of operating in either the monostable or astable mode. It requires an external capacitor between pins 1 and 3 and an external resistor between pins 2 and 3 to determine the output pulse width in the monostable mode, and the output frequency in the astable mode.

Astable operation is enabled by a high level on the astable input or low level on the $\overline{\text{astable}}$ input. The output frequency (at 50-percent duty cycle) at Q and $\overline{Q}$ outputs is determined by the timing components. A frequency twice that of Q is available at the oscillator output. A 50-percent duty cycle is not guaranteed.

Monostable operation is obtained when the device is triggered by low-to-high transition at + trigger input or high-to-low transition at – trigger input. The device can be retriggered by applying a simultaneous low-to-high transition to both the + trigger and retrigger inputs. A high level on reset input resets the outputs Q to low and $\overline{Q}$ to high.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or driving 74LS**

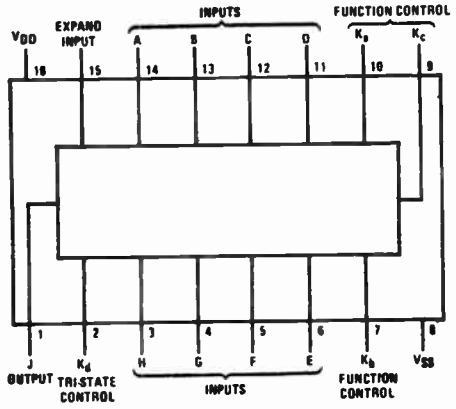


4047

4048 3-STATE EXPANDABLE 8-FUNCTION 8-INPUT GATE

The 4048 is a programmable 8-input gate. Three binary control lines, K_a, K_b and K_c, determine the eight different logic functions of the gate. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR and AND/NOR. A fourth input, K_d, is a 3-state control. When K_d is high, the output is enabled; when K_d is low, the output is a high impedance. This feature enables the user to connect the device to a common bus line. The expand input permits the user to increase the number of gate inputs. For example, two 8-input 4048's can be cascaded into a 16-input multifunction gate. When the expand input is not used, it should be connected to Vss. All inputs are buffered and protected against electrostatic effects.

Supply Voltage Range — **3V to 15V**
Noise Immunity — **0.45 V_{DD} typ.**
TTL Compatibility — **Drives 1 standard TTL load at V_{CC} = 5V, over full temperature range.**



4048

OUTPUT FUNCTION	BOOLEAN EXPRESSION	CONTROL INPUTS K_a	K_b	K_c	K_d	UNUSED INPUTS
NOR	$J = \overline{A+B+C+D+E+F+G+H}$	0	0	0	1	V_{SS}
OR	$J = A+B+C+D+E+F+G+H$	0	0	1	1	V_{SS}
OR/AND	$J = (A+B+C+D)\cdot(E+F+G+H)$	0	1	0	1	V_{SS}
OR/NAND	$J = \overline{(A+B+C+D)\cdot(E+F+G+H)}$	0	1	1	1	V_{SS}
AND	$J = A\cdot B\cdot C\cdot D\cdot E\cdot F\cdot G\cdot H$	1	0	0	1	V_{DD}
NAND	$J = \overline{A\cdot B\cdot C\cdot D\cdot E\cdot F\cdot G\cdot H}$	1	0	1	1	V_{DD}
AND/NOR	$J = \overline{(A+B+C+D)+(E+F+G+H)}$	1	1	0	1	V_{DD}
AND/OR	$J = (A+B+C+D)+(E+F+G+H)$	1	1	1	1	V_{DD}
Hi-Z		X	X	X	0	X

Positive logic: 0 = low level, 1 = high level, X = irrelevant, EXPAND input tied to V_{SS}.

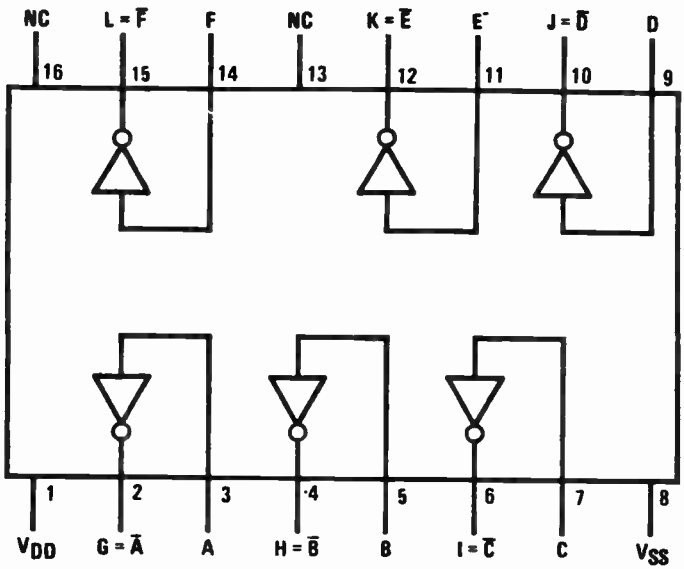
Truth Table 4048

4049 HEX INVERTING BUFFER

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. These devices feature logic-level conversion using only one supply voltage (V_{DD}). The input-signal high level (V_{IH}) can exceed the V_{DD} supply voltage when these devices are used for logic level conversions. These devices are intended for use as hex buffers, CMOS to DTL/TTL converters, or as CMOS current drivers. At V_{DD} = 5V, they can drive directly two DTL/TTL loads over the full operating temperature range.

Supply Voltage Range
TTL Compatability

3V to 15V
Direct drive to 2 TTL loads at 5V over full temperature range.

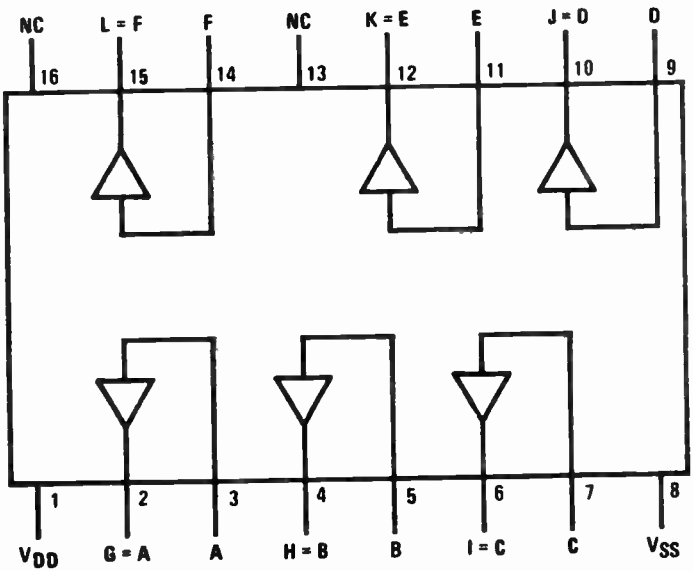


4049

4050 HEX NONINVERTING BUFFER

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. These devices feature logic-level conversion using only one supply voltage (V_{DD}). The input-signal high level (V_{IH}) can exceed the V_{DD} supply voltage when these devices are used for logic level conversions. These devices are intended for use as hex buffers, CMOS to DTL/TTL converters, or as CMOS current drivers. At V_{DD} = 5V, they can drive directly two DTL/TTL loads over the full operating temperature range.

Supply Voltage Range	**3V to 15V**
TTL Compatability	**Direct drive to 2 TTL loads at 5V over full temperature range.**



4050

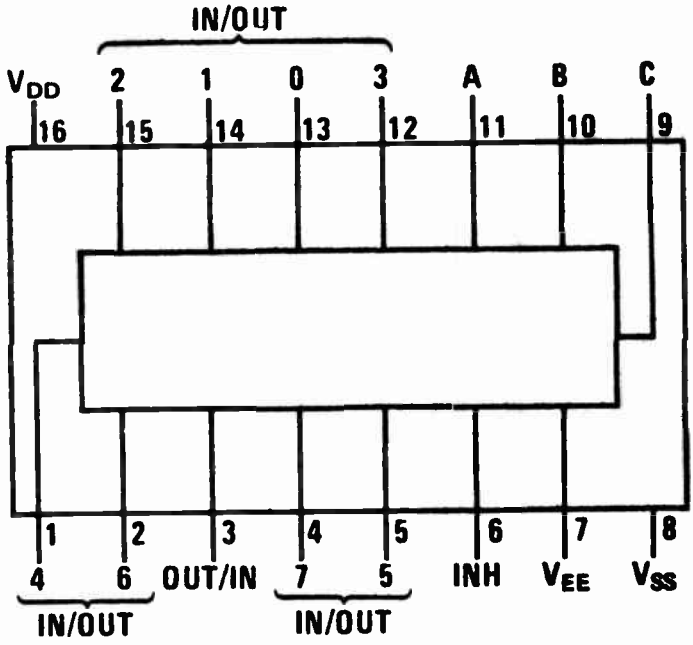
4051 SINGLE 8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

These analog multiplexers/demultiplexers are digitally controlled analog switches having low on impedance and very low off leakage currents. Control of analog signals up to 15 V_{p-p} can be achieved by digital signal amplitudes of 3V to 15V. For example, if $V_{DD} = 5V$, $V_{SS} = 0V$ and $V_{EE} = -5V$, analog signals from $-5V$ to $+5V$ can be controlled by digital inputs of 0V-5V. The multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD} - V_{SS}$ and $V_{DD} - V_{EE}$ supply voltage ranges, independent of the logic state of the control signals. When a logical 1 is present at the inhibit input terminal, all channels are off.

- 4051 is a single 8-channel multiplexer having three binary control inputs, A, B and C, and an inhibit input. The three binary signals select one of eight channels to be turned on and connect the input to the output.
- 4052 is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select one of four pairs of channels to be turned on, and connect the differential analog inputs to the differential outputs.
- 4053 is a triple 2-channel multiplexer having three separate digital control inputs, A, B and C, and an inhibit input. Each control input selects one of a pair of channels that are connected in a single-pole double-throw configuration.

Range of digital and analog signal levels: Digital 3V to 15V, analog to 15Vp-p.
On resistance: 80Ω (typ.) over entire 15Vpp signal-input range for $V_{DD}-V_{EE}$= 15V.
Off resistance: Channel leakage of ±10pA (typ.) at $V_{DD} - V_{EE}$ = 10V.
Logic level conversion for digital addressing signals of 3V to 15V($V_{DD}-V_{SS}$ = 3V to 15V) to switch analog signals to 15Vp-p ($V_{DD} - V_{EE}$ = 15V).
Logic level conversion for digital addressing signals of 3 — 15V($V_{DD}-V_{SS}$= 3V to 15V) to switch analog signals to 15V_{p-p}($V_{DD}-V_{EE}$= 15V).
Matched switch characteristics: ΔR_{ON} = 5Ω (Typ.) for $V_{DD} - V_{EE}$ = 15V.
Quiescent power dissipation under all digital control input and supply conditions: 1 μW (typ.) at $V_{DD}-V_{SS}$= $V_{DD}-V_{EE}$= 10V.
Binary address decoding on chip.

CD4051BM/CD4051BC



4051

INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	CD4051B	CD4052B	CD4053B
0	0	0	0	0	0X, 0Y	cx, bx, ax
0	0	0	1	1	1X, 1Y	cx, bx, ay
0	0	1	0	2	2X, 2Y	cx, by, ax
0	0	1	1	3	3X, 3Y	cx, by, ay
0	1	0	0	4		cy, bx, ax
0	1	0	1	5		cy, bx, ay
0	1	1	0	6		cy, by, ax
0	1	1	1	7		cy, by, ay
1	*	*	*	NONE	NONE	NONE

*Don't Care Condition

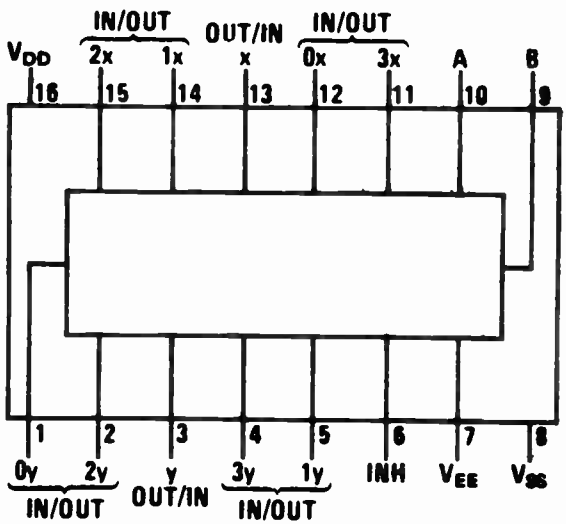
Truth Table 4051,4052, 4053

4052 DUAL 4-CHANNEL MULTIPLEXER/DEMULITPLEXER

These analog multiplexers/demultiplexers are digitally controlled analog switches having low on impedance and very low off leakage currents. Control of analog signals up to 15 V_{p-p} can be achieved by digital signal amplitudes of 3V to 15V. For example, if $V_{DD} = 5V$, $V_{SS} = 0V$ and $V_{EE} = -5V$, analog signals from $-5V$ to $+5V$ can be controlled by digital inputs of 0V-5V. The multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD} - V_{SS}$ and $V_{DD} - V_{EE}$ supply voltage ranges, independent of the logic state of the control signals. When a logical 1 is present at the inhibit input terminal, all channels are off.

- 4052 is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select one of four pairs of channels to be turned on, and connect the differential analog inputs to the differential outputs.
- 4053 is a triple 2-channel multiplexer having three separate digital control inputs, A, B and C, and an inhibit input. Each control input selects one of a pair of channels that are connected in a single-pole double-throw configuration.

CD4052BM/CD4052BC



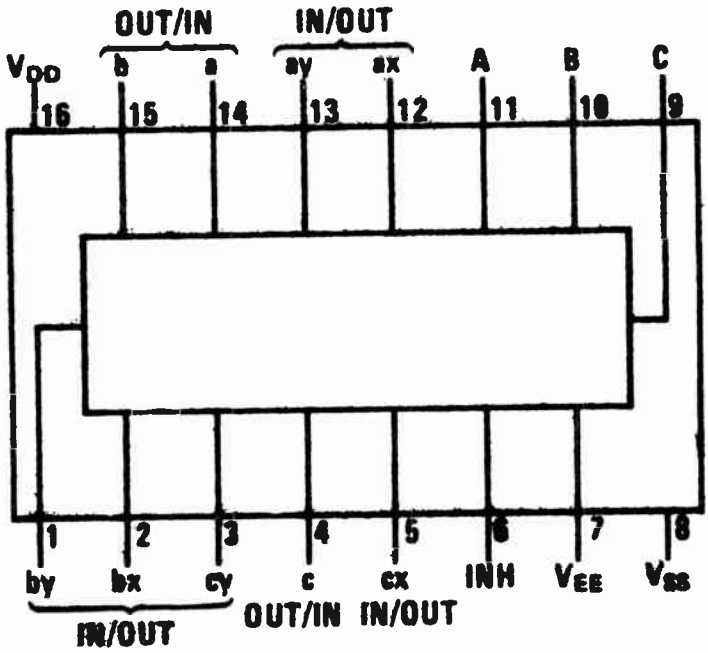
4052

4053 TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

These analog multiplexers/demultiplexers are digitally controlled analog switches having low on impedance and very low off leakage currents. Control of analog signals up to 15 $V_{p\text{-}p}$ can be achieved by digital signal amplitudes of 3V to 15V. For example, if $V_{DD} = 5V$, $V_{SS} = 0V$ and $V_{EE} = -5V$, analog signals from $-5V$ to $+5V$ can be controlled by digital inputs of 0V-5V. The multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD} - V_{SS}$ and $V_{DD} - V_{EE}$ supply voltage ranges, independent of the logic state of the control signals. When a logical 1 is present at the inhibit input terminal, all channels are off.

- 4053 is a triple 2-channel multiplexer having three separate digital control inputs, A, B and C, and an inhibit input. Each control input selects one of a pair of channels that are connected in a single-pole double-throw configuration.

CD4053BM/CD4053BC

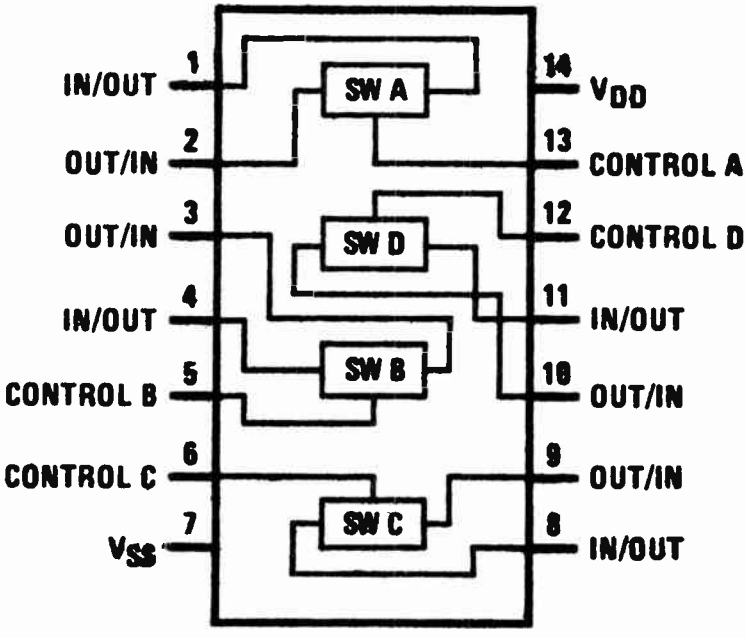


4053

4066 QUAD BILATERAL SWITCH

The 4066 is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with 4016 but has a much lower on resistance, and on resistance is relatively constant over the input-signal range.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
Range of Digital and Analog Switching	**±7.5 V_{PEAK}**
On Resistance for 15V Operation	**80Ωtyp.**
Matched on Resistance Over 15V Signal Input	**Δ RON = 5Ω typ.**
On/off Output Voltage Ratio	**65 dB typ.**
Linearity	**0.4% distortion typ.**
"OFF" Switch Leakage	**0.1 nA typ.**
Control Input Impedance	**10^{12} Ωtyp.**
Crosstalk Between Switches	**-50 dB typ. @fis = 0.9 MHz, RL = 1 KΩ**
Frequency Response, Switch "ON"	**40 MHz typ.**



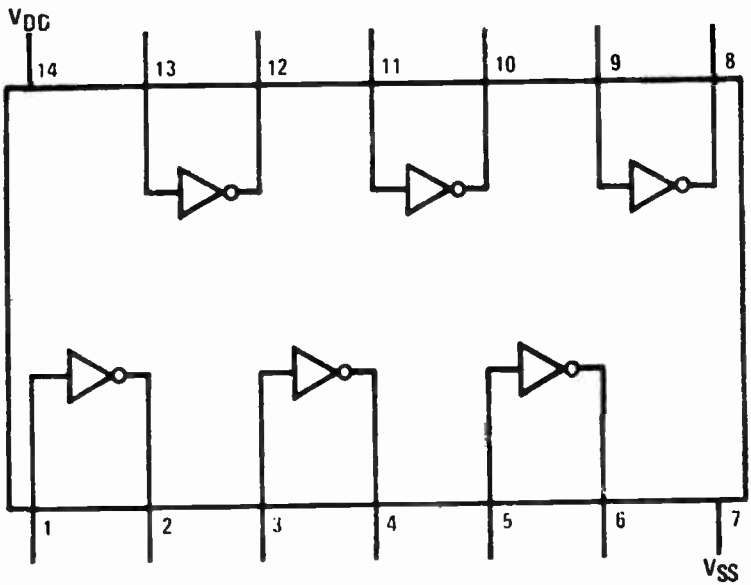
4066

4069 INVERTER CIRCUIT

The 4069 consists of six inverter circuits and is manufactured using complementary MOS (CMOS) to achieve wide power-supply operating range, low power consumption, high noise immunity and symmetric-controlled rise and fall times.

This device is intended for all general purpose inverter applications where the special characteristics of the 74C901, 74C903, 74C907 and 4049 hex inverter/buffers are not required. In those applications requiring larger noise immunity, the 74C14 or 74C914 hex Schmitt trigger is suggested. All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and Vss.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**

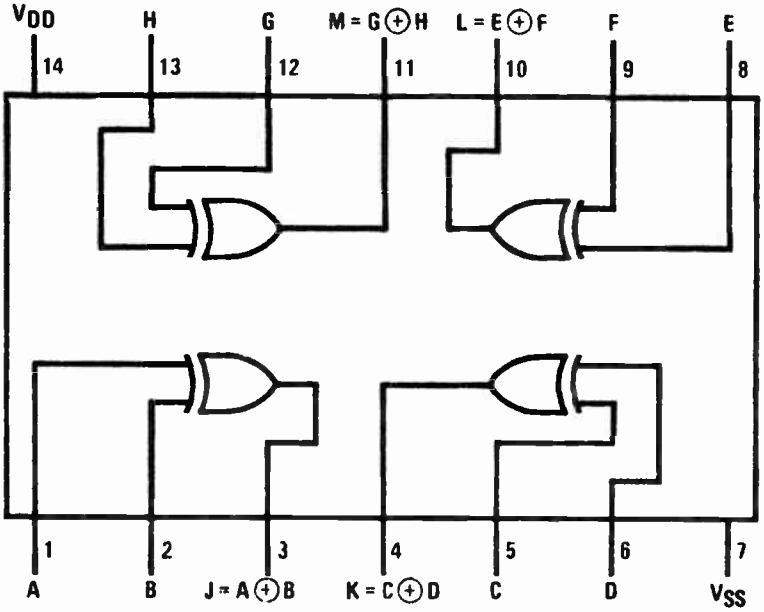


4069

4070 QUAD 2-INPUT EXCLUSIVE-OR GATE

Employing complementary MOS (CMOS) transistors to achieve wide power-supply operating range, low power consumption and high noise margin, this gate provides basic functions used in the implementation of digital integrated circuit systems. The N-channel and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No DC power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Supply Voltage Range — **3V to 15V**
Noise Immunity — **0.45 V_{DD} typ.**
TTL Compatibility — **Fanout of 2 driving 74L or 1 driving 74LS**



4070

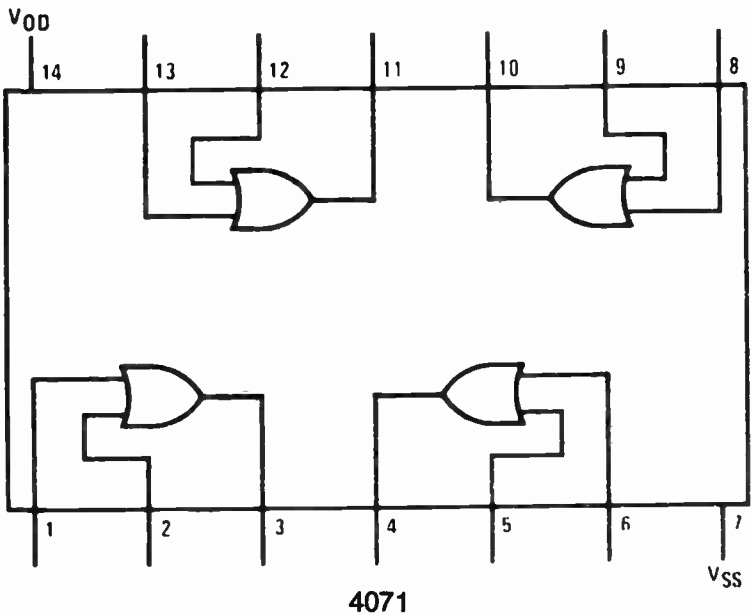
INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Truth Table
4070

4071 QUAD 2-INPUT OR BUFFERED B SERIES GATE

These quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs that improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and Vss.

TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**
Parametric Ratings	**5V—10V—15V**
Maximum Input Leakage	**1 μA at 15V**

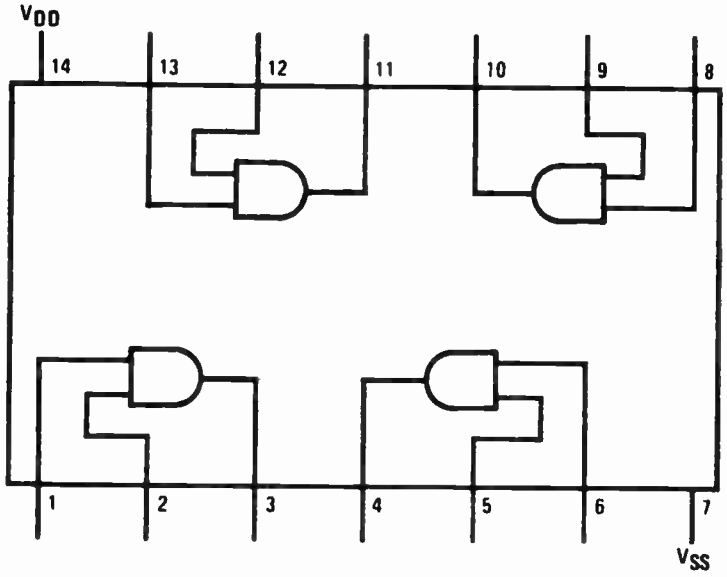


4071

4081 QUAD 2-INPUT AND BUFFERED B SERIES GATE

These quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs that improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**
Parametric Ratings	**5V—10V—15V**
Maximum Input Leakage	**1 μA at 15V**

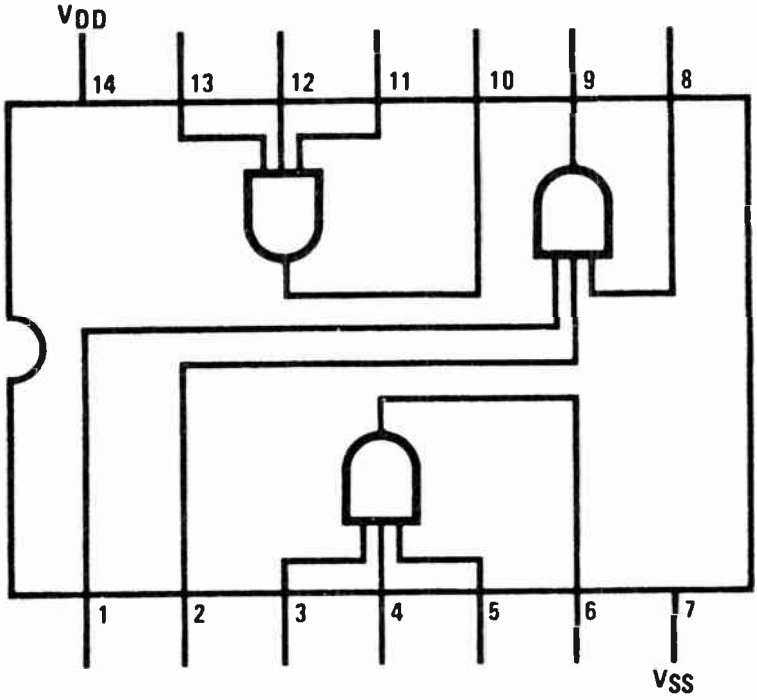


4081

4073 DOUBLE BUFFERED TRIPLE 3-INPUT NAND GATE

These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs that improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to VDD and Vss.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 VDD typ.**
TTL Compatibility	**2 driving 74L or 1 driving 74LS**

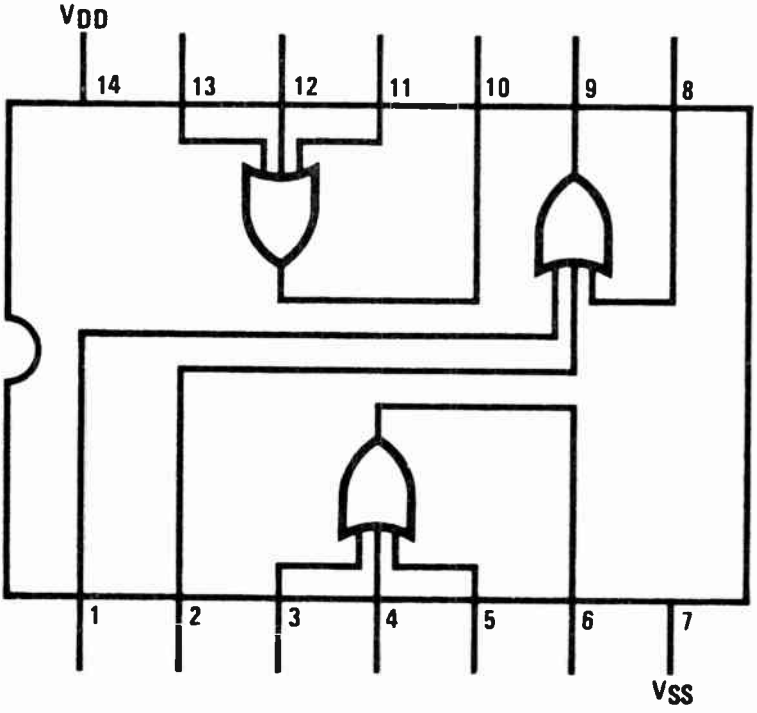


4073

4075 DOUBLE BUFFERED TRIPLE 3-INPUT NOR GATE

These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs that improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and Vss.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**2 driving 74L or 1 driving 74LS**



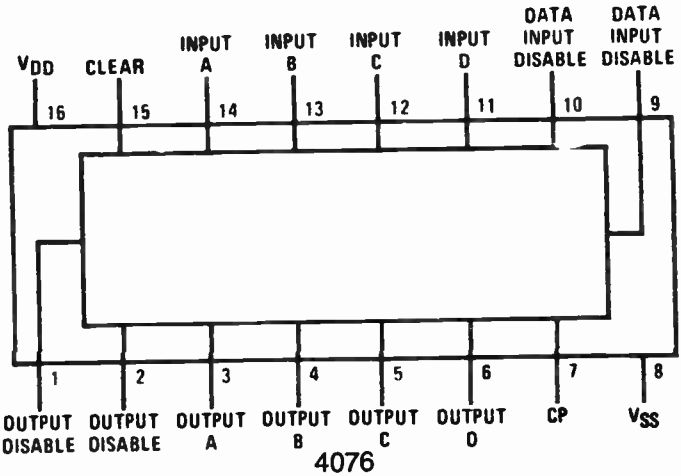
4075

4076 3-STATE QUAD D FLIP-FLOP

The 4076 3-state quad D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N-channel and P-channel enhancement transistors. The four D type flip-flops operate synchronously from a common clock. The 3-state output allows the device to be used in bus organized systems. The outputs are placed in the 3-state mode when either of the two output disable pins are in the logic 1 level. The input disables allow the flip-flops to remain in their present states without disrupting the clock. If either of the two input disables is taken to a logic 1 level, the Q outputs are fed back to the inputs and in this manner the flip-flops do not change state.

Clearing is enabled by taking the clear input to a logic 1 level. Clocking occurs on the positive-going transition. All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Supply Voltage Range — **3V to 15V**
Noise Immunity — **0.45 V_{DD} typ.**
TTL Compatibility — **Fanout of 2 driving 74L or 1 driving 74LS**



4076

t_n		t_{n+1}
DATA INPUT DISABLE	DATA INPUT	OUTPUT
Logic "1" on One or Both Inputs	X	Q_n
Logic "0" on Both Inputs	1	1
Logic "0" on Both Inputs	0	0

Truth Table
4076

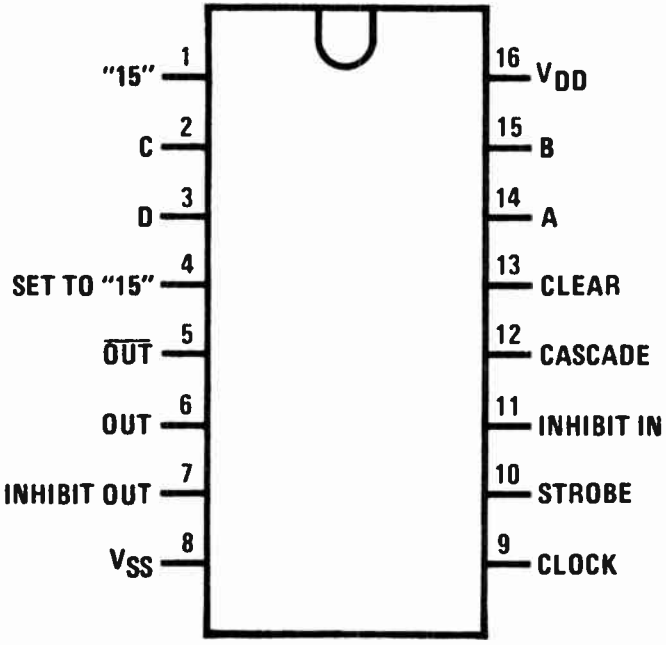
4089 BINARY RATE MULTIPLIER

The 4089 is a 4-bit binary rate multiplier that provides an output pulse rate which is the input clock pulse rate multiplied by 1/16 times the binary input number. For example, if 5 is the binary input number, there will be 5 output pulses for every 16 clock pulses.

The 4527 is a 4-bit BCD rate multiplier that provides an output pulse rate which is the input clock pulse rate multiplied by 1/10 times the BCD input number. For example, if 5 is the BCD input number, there will be 5 output pulses for every 10 clock pulses.

These devices may be used to perform arithmetic operations. These operations include multiplication and division, A/D and D/A conversion and frequency division.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**



4089

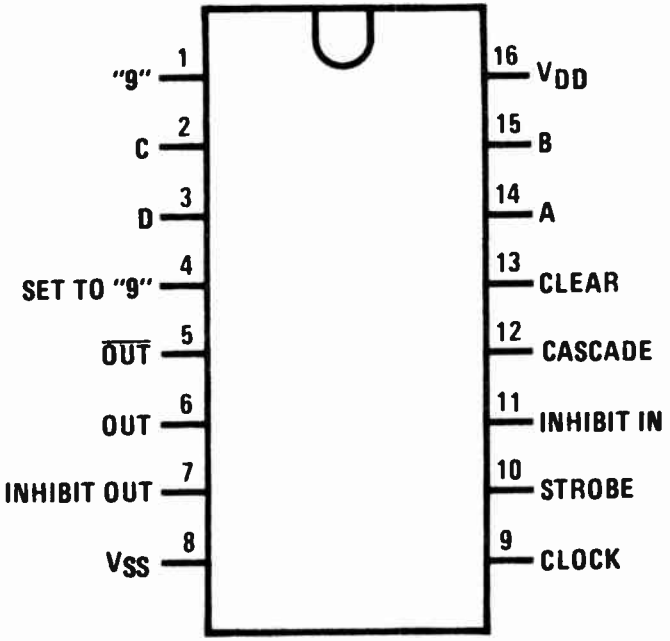
4527 BCD RATE MULTIPLIER

The 4089 is a 4-bit binary rate multiplier that provides an output pulse rate which is the input clock pulse rate multiplied by 1/16 times the binary input number. For example, if 5 is the binary input number, there will be 5 output pulses for every 16 clock pulses.

The 4527 is a 4-bit BCD rate multiplier that provides an output pulse rate which is the input clock pulse rate multiplied by 1/10 times the BCD input number. For example, if 5 is the BCD input number, there will be 5 output pulses for every 10 clock pulses.

These devices may be used to perform arithmetic operations. These operations include multiplication and division, A/D and D/A conversion and frequency division.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**

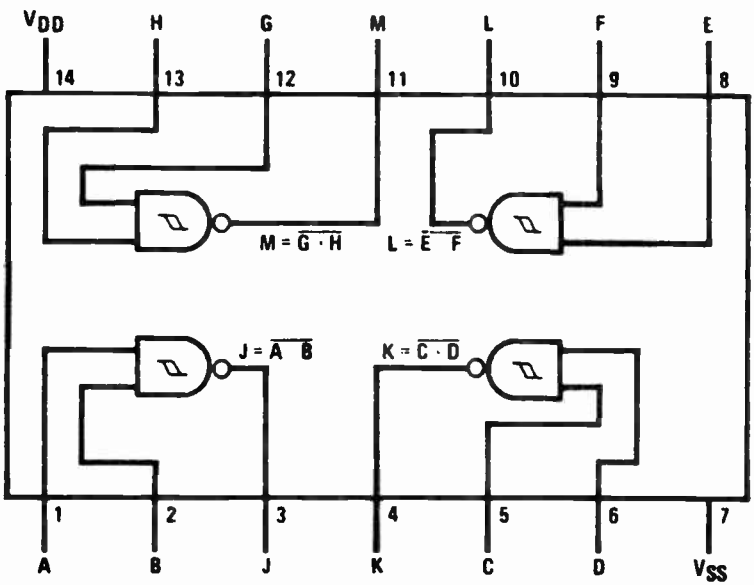


4527

4093 QUAD 2-INPUT NAND SCHMITT TRIGGER

The 4093 consists of four Schmitt trigger circuits. Each circuit functions as a 2-input NAND gate with Schmitt trigger action on both inputs. The gate switches at different points for positive-going and negative-going signals. The difference between the positive (V_{T+}) and the negative voltage (V_{T-}) is defined as hysteresis voltage (V_H). All outputs have equal source and sink currents and conform to standard B-series output drive.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**Greater than 50%**
Hysteresis Voltage (any input)	**T_A = 25° C**
Typical	**V_{DD} = 5V V_H = 1.5V**
	V_{DD} = 10V V_H= 2.2V
	V_{DD} = 15V V_H = 2.7V
Guaranteed	**V_H = 0.1 V_{DD}**

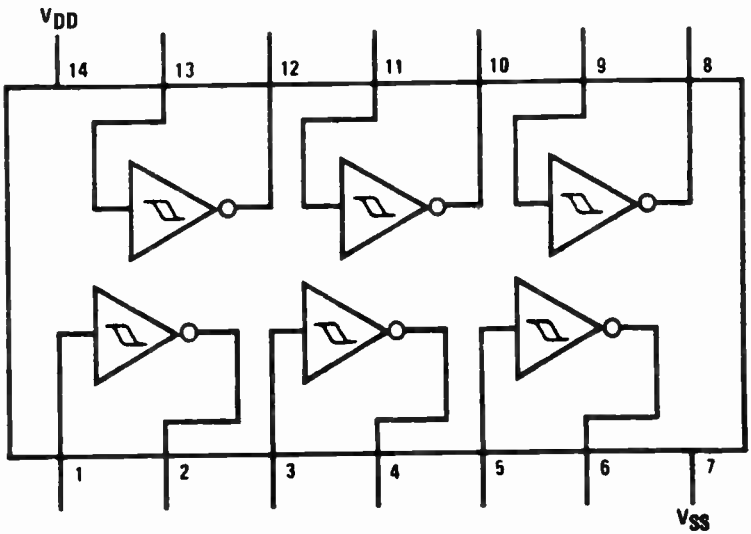


4093

40106 HEX SCHMITT TRIGGER

The 40106 hex Schmitt trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N-channel and P-channel enhancement transistors. The positive-going and negative-going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (Typ. 0.0005V/°C at V_{DD} = 10V). All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.7 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74 L or 1 driving 74LS**
Hysteresis	**0.4 V_{DD} typ. 0.2 V_{DD} guaranteed**



40106

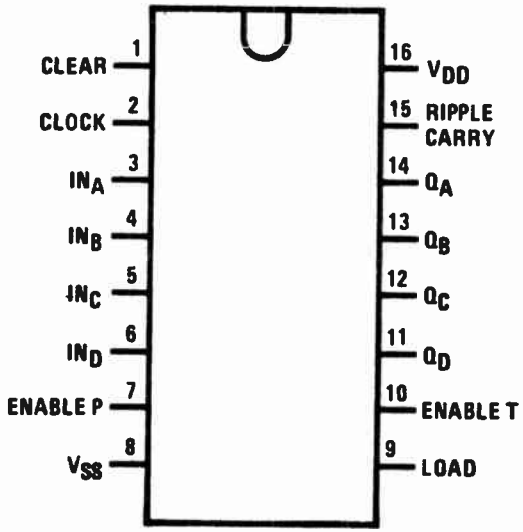
40160 DECADE COUNTER WITH ASYNCHRONOUS CLEAR

These synchronous presettable up counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. They feature an internal carry look ahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the 40162 and 40163 is synchronous, and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the 40160 and 40161 is asynchronous, and a low level at the clear input sets all four outputs low, regardless of the state of the clock.

Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**



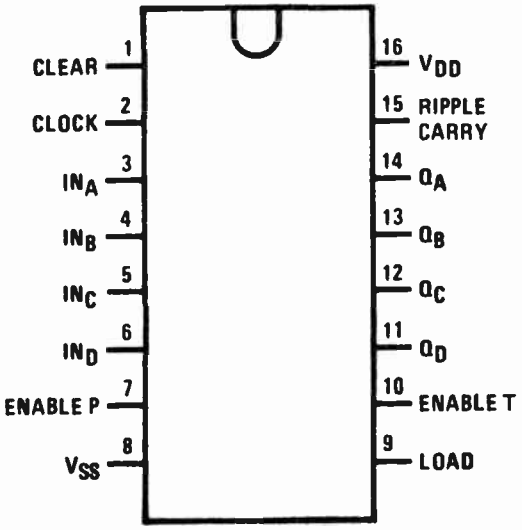
40161 BINARY COUNTER WITH ASYNCHRONOUS CLEAR

These synchronous presettable up counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. They feature an internal carry look ahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the 40162 and 40163 is synchronous, and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the 40160 and 40161 is asynchronous, and a low level at the clear input sets all four outputs low, regardless of the state of the clock.

Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**



40161

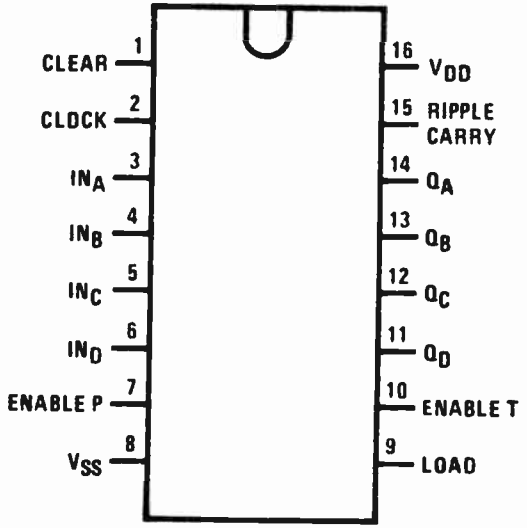
40162 DECADE COUNTER WITH SYNCHRONOUS CLEAR

These synchronous presettable up counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. They feature an internal carry look ahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the 40162 and 40163 is synchronous, and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the 40160 and 40161 is asynchronous, and a low level at the clear input sets all four outputs low, regardless of the state of the clock.

Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**



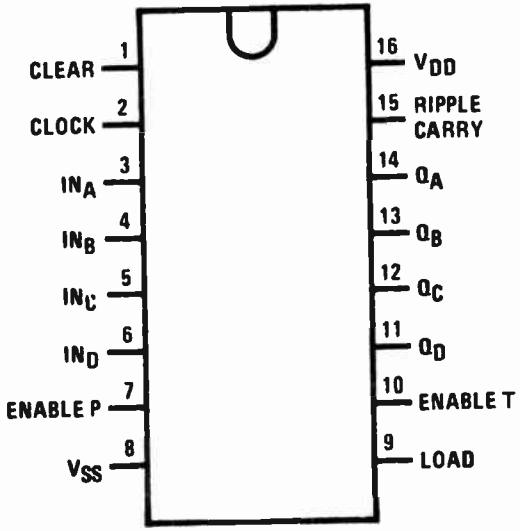
40163 BINARY COUNTER WITH SYNCHRONOUS CLEAR

These synchronous presettable up counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. They feature an internal carry look ahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the 40162 and 40163 is synchronous, and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the 40160 and 40161 is asynchronous, and a low level at the clear input sets all four outputs low, regardless of the state of the clock.

Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**



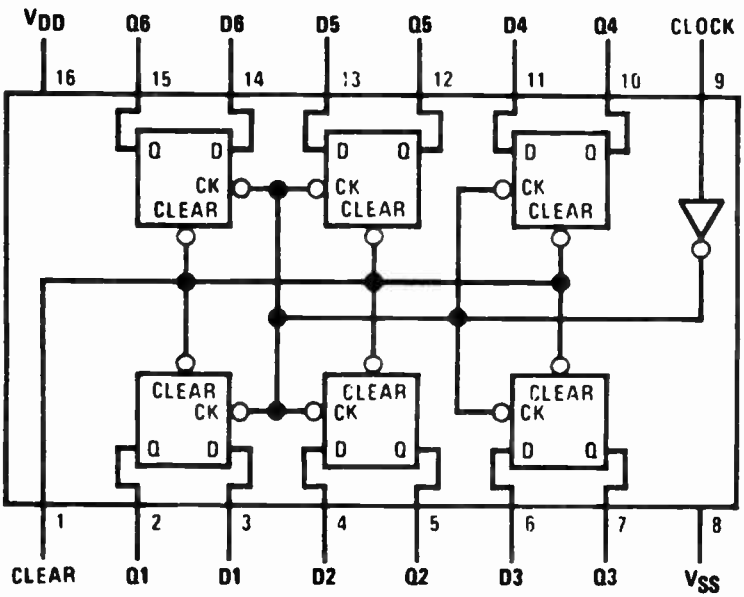
40163

40174 HEX D FLIP-FLOP

The 40174 consists of six positive-edge triggered D-type flip-flops; the true outputs from each flip-flop are externally available. The 40175 consists of four positive-edge triggered D-type flip-flops. Both the true and complement outputs from each flip-flop are externally available.

All flip-flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. The clearing operation, enabled by a negative pulse at clear input, clears all Q outputs to logical 0 and $\overline{Q}$'s (40175 only) to logical 1. All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS}.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**



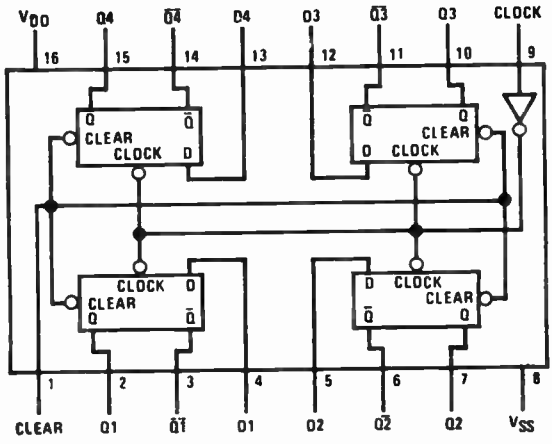
40174

40175 QUAD D FLIP-FLOP

The 40174 consists of six positive-edge triggered D-type flip-flops; the true outputs from each flip-flop are externally available. The 40175 consists of four positive-edge triggered D-type flip-flops. Both the true and complement outputs from each flip-flop are externally available.

All flip-flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. The clearing operation, enabled by a negative pulse at clear input, clears all Q outputs to logical 0 and Q's (40175 only) to logical 1. All inputs are protected from static discharge by diode clamps to V_{DD} and Vss.

Supply Voltage Range — **3V to 15V**
Noise Immunity — **0.45 V_{DD} typ.**
TTL Compatibility — **Fanout of 2 driving 74L or 1 driving 74LS**



40175

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	Q̄•
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	H	X	NC	NC
H	L	X	NC	NC

Truth Table
40174, 40175

H = High level
L = Low level
X = Irrelevant
↑ = Transition from low to high level
NC = No change
• = Q̄ for CD40175B only

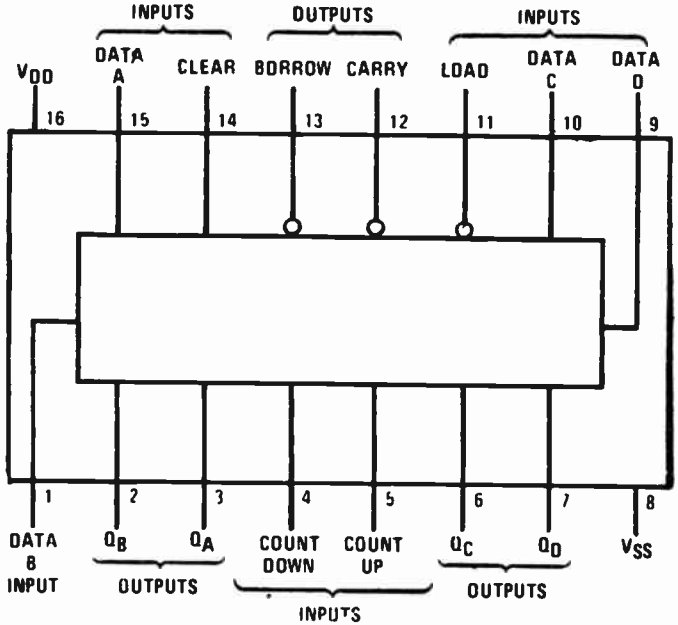
40192 SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTER

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The 40192BM and 40192BC are BCD counters. The 40193BM and 40193BC are binary counters.

Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive-going transition of this clock.

These counters feature preset inputs that are enabled when load is a logical 0 and a clear, which forces all outputs to 0 when it is at logical 1. The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry. All inputs are protected against damage due to static discharge by clamps to V_{DD} and V_{SS}.

Supply Voltage Range — **3V to 15V**
Noise Immunity — **0.45 V_{DD} typ.**
TTL Compatibility — **Fanout of 2 driving 74L or 1 driving 74LS**



40192

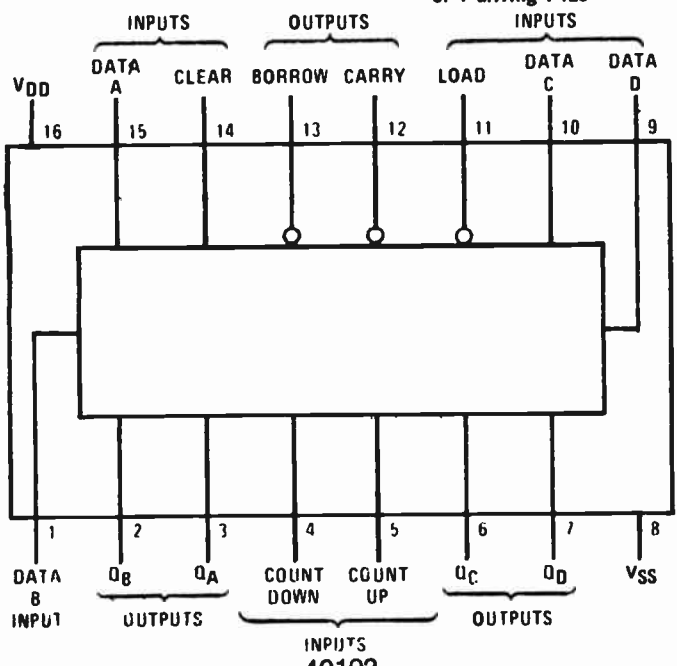
40193 SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTER

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The 40192BM and 40192BC are BCD counters. The 40193BM and 40193BC are binary counters.

Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive-going transition of this clock.

These counters feature preset inputs that are enabled when load is a logical 0 and a clear, which forces all outputs to 0 when it is at logical 1. The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry. All inputs are protected against damage due to static discharge by clamps to V_{DD} and Vss.

Supply Voltage Range — **3V to 15V**
Noise Immunity — **0.45 V_{DD} typ.**
TTL Compatibility — **Fanout of 2 driving 74L or 1 driving 74LS**



40193

4510 BCD UP/DOWN COUNTER

The 4510 and 4516 are monolithic CMOS up/down counters which count in BCD and binary, respectively. The counters count up when the up/down input is at logical 1 and count down when the up/down input is at logical 0. A logical 1 preset enable signal allows information at the parallel inputs to preset the counters to any state asynchronously with the clock. The counters are advanced one count at the positive-going edge of the clock if the carry in, preset enable and reset inputs are at logical 0. Advancement is inhibited when any of these three inputs are at logical 1. The carry out signal is normally at logical 1 state and goes to logical 0 when the counter reaches its maximum count in the up mode or its minimum count in the down mode, provided the carry input is at logical 0 state. The counters are cleared asynchronously by applying a logical 1 voltage level at the reset input. All inputs are protected against static discharge by diode clamps to both V_{DD} and Vss.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**
Quiescent Power Dissipation	**0.25 uW/package typ.@ Vcc = 5V**

Truth Table 4510

CLOCK	RESET	PRESET ENABLE	CARRY IN	UP/DOWN	OUTPUT FUNCTION
X	1	X	X	X	Reset to zero
X	0	1	X	X	Set to P1, P2, P3, P4
⎍	0	0	0	1	Count up
⎍	0	0	0	0	Count down
⎎	0	0	X	X	No change
X	0	0	1	X	No change

⎍ = positive transition

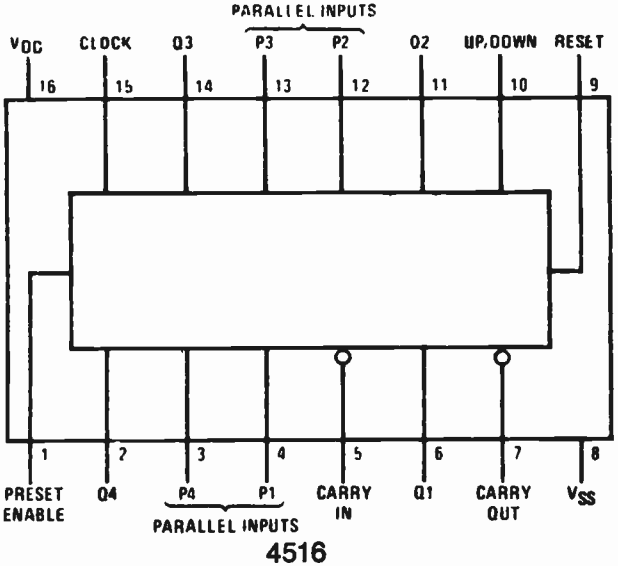
⎎ = negative transition

X = don't care

4516 BINARY UP/DOWN COUNTER

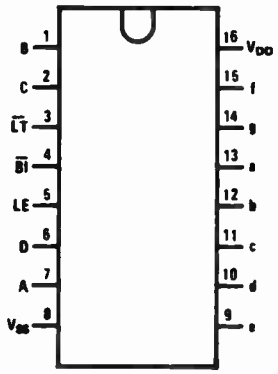
The 4510 and 4516 are monolithic CMOS up/down counters which count in BCD and binary, respectively. The counters count up when the up/down input is at logical 1 and count down when the up/down input is at logical 0. A logical 1 preset enable signal allows information at the parallel inputs to preset the counters to any state asynchronously with the clock. The counters are advanced one count at the positive-going edge of the clock if the carry in, preset enable and reset inputs are at logical 0. Advancement is inhibited when any of these three inputs are at logical 1. The carry out signal is normally at logical 1 state and goes to logical 0 when the counter reaches its maximum count in the up mode or its minimum count in the down mode, provided the carry input is at logical 0 state. The counters are cleared asynchronously by applying a logical 1 voltage level at the reset input. All inputs are protected against static discharge by diode clamps to both V_{DD} and Vss.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**
Quiescent Power Dissipation	**0.25 uW/package typ.@ Vcc = 5V**



4516

The 4511 BCD-to-7 segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with 7-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts, either directly or indirectly. Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver and various clock, watch and timer uses.



4511

4511

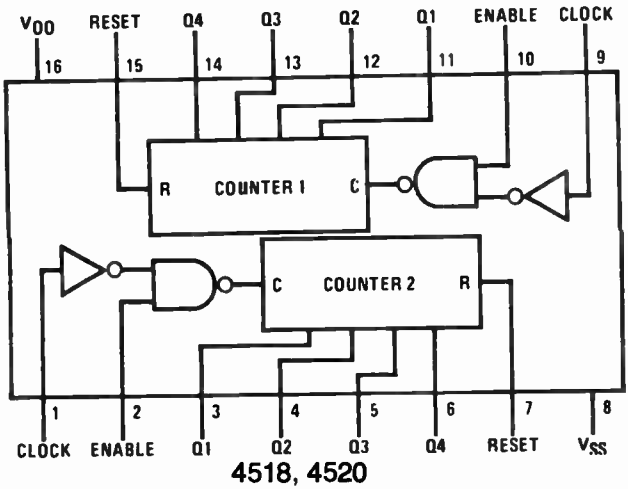
Truth Table 4511

INPUTS							OUTPUTS						
LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	
0	1	1	1	0	1	1	0	0	0	0	0	0	0	
0	1	1	1	1	0	0	0	0	0	0	0	0	0	
0	1	1	1	1	0	1	0	0	0	0	0	0	0	
0	1	1	1	1	1	0	0	0	0	0	0	0	0	
0	1	1	1	1	1	1	0	0	0	0	0	0	0	
1	1	1	X	X	X	X	*	*	*	*	*	*	*	

X = Don't care
*Depends upon the BCD code applied during the 0 to 1 transition of LE

The 4518 dual BCD counter and the 4520 dual binary counter are implemented with complementary MOS (CMOS) circuits constructed with N-channel and P-channel enhancement mode transistors. Each counter consists of two identical, independent, synchronous, 4-stage counters. The counter stages are toggle flip-flops that increment on either the positive-edge of clock or negative-edge of enable, simplifying cascading of multiple stages. Each counter can be asynchronously cleared by a high level on the reset line. All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

Supply Voltage Range — **3V to 15V**
Noise Immunity — **0.45 V_{DD} typ.**
TTL Compatibility — **Fanout of 2 driving 74L or 1 driving 74LS**
Counting rate (typ.) at V_{DD} = 10V — **6 MHz**



4518, 4520

CLOCK	ENABLE	RESET	ACTION
↓	1	0	Increment counter
0	↓	0	Increment counter
↑	X	0	No change
X	↑	0	No change
↓	0	0	No change
1	↑	0	No change
X	X	1	Q1 thru Q4 = 0

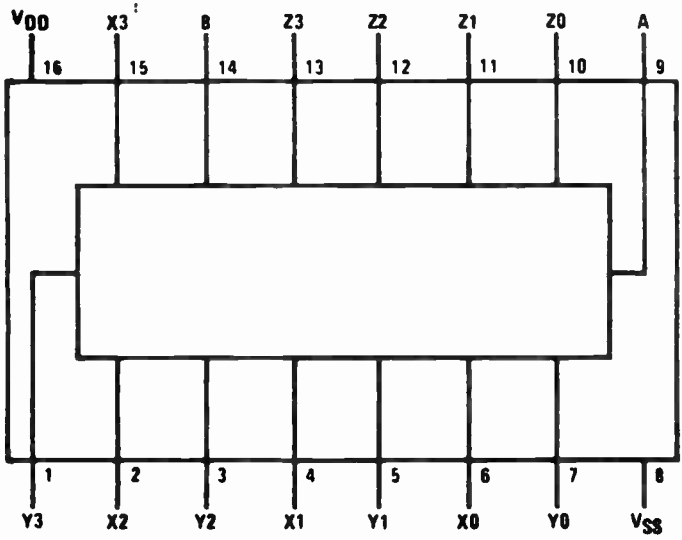
Truth Table
4518, 4520

X = Don't Care

4519 4-BIT AND/OR SELECTOR

The 4519 is a monolithic complementary MOS (CMOS) integrated circuit constructed with N-channel and P-channel enhancement mode transistors. Depending on the condition of the control inputs, this part provides three functions in one package: a 4-bit AND/OR selector, a quad 2-channel data selector, or a quad Exclusive-NOR gate. The device outputs have equal source and sink current capabilities and conform to the standard B series output drive and supply voltage ratings.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{DD} typ.**
TTL Compatibility	**Fanout of 2 driving 74L or 1 driving 74LS**



4519

CONTROL INPUTS		OUTPUT
A	B	Z_n
0	0	0
0	1	Y_n
1	0	X_n
1	1	$X_n \odot Y_n$

Truth Table
4519

Note: $X_n \odot Y_n = \overline{X_n \oplus Y_n} = X_n Y_n + \overline{X}_n \overline{Y}_n$

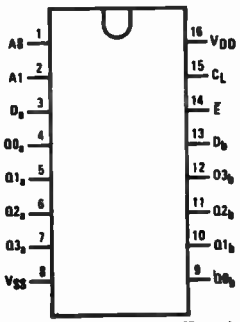
4723 DUAL 4-BIT ADDRESSABLE LATCH

The 4723 is a dual 4-bit addressable latch with common control inputs, including two address inputs (A0 and A1), an active low enable input ($\overline{E}$) and an active high clear input (CL). Each latch has a data input (D) and four outputs (Q0-Q3). The 4724 and 4099 are 8-bit addressable latches with three address inputs (A0-A2), an active low enable input ($\overline{E}$), active high clear input (CL), a data input (D) and eight outputs (Q0-Q7).

Data is entered into a particular bit in the latch when that bit is addressed by the address inputs and the enable ($\overline{E}$) is low. Data entry is inhibited when enable ($\overline{E}$) is high.

When clear (CL) and enable ($\overline{E}$) are high, all outputs are low. When clear (CL) is high, enable ($\overline{E}$) is low, the channel demultiplexing occurs. The bit that is addressed has an active output which follows the data input while all unaddressed bits are held low. When operating in the addressable latch mode ($\overline{E}$ = CL = LOW), changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E}$ = HIGH, CL = LOW).

Supply Voltage Range — **3V to 15V**
Noise Immunity — **0.45 V_{DD} typ.**
TTL Compatibility — **Fanout of 2 driving 74L or 1 driving 74LS**



4723

Truth Table 4723, 4724, 4099

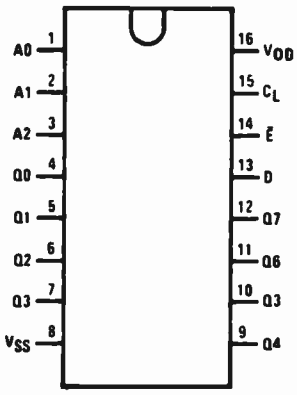
MODE SELECTION				
$\overline{E}$	CL	ADDRESSED LATCH	UNADDRESSED LATCH	MODE
L	L	Follows Data	Holds Previous Data	Addressable Latch
H	L	Holds Previous Data	Holds Previous Data	Memory
L	H	Follows Data	Reset to "0"	Demultiplexer
H	H	Reset to "0"	Reset to "0"	Clear

The 4723 is a dual 4-bit addressable latch with common control inputs, including two address inputs (A0 and A1), an active low enable input ($\overline{E}$) and an active high clear input (CL). Each latch has a data input (D) and four outputs (Q0-Q3). The 4724 and 4099 are 8-bit addressable latches with three address inputs (A0-A2), an active low enable input ($\overline{E}$), active high clear input (CL), a data input (D) and eight outputs (Q0-Q7).

Data is entered into a particular bit in the latch when that bit is addressed by the address inputs and the enable ($\overline{E}$) is low. Data entry is inhibited when enable ($\overline{E}$) is high.

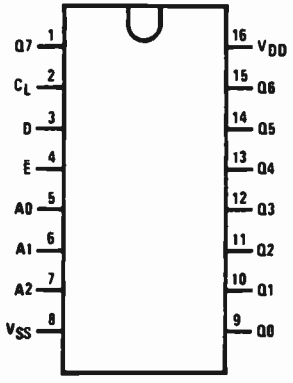
When clear (CL) and enable ($\overline{E}$) are high, all outputs are low. When clear (CL) is high, enable ($\overline{E}$) is low, the channel demultiplexing occurs. The bit that is addressed has an active output which follows the data input while all unaddressed bits are held low. When operating in the addressable latch mode ($\overline{E}$ = CL = LOW), changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E}$ = HIGH, CL = LOW).

Supply Voltage Range
Noise Immunity
TTL Compatibility



4724

3V to 15V
0.45 VDD typ.
Fanout of 2 driving 74L
or 1 driving 74LS



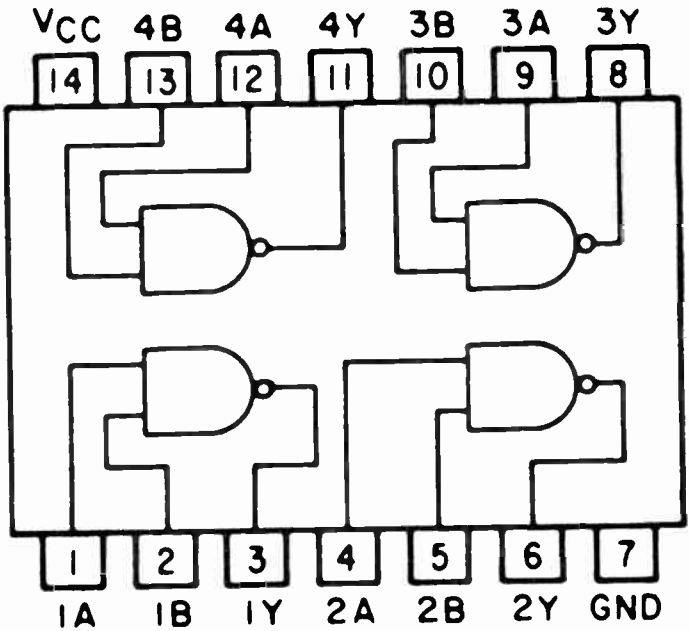
4099

74C00 QUAD 2-INPUT NAND GATE

These logic gates employ complementary MOS (CMOS) to achieve wide power-supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this, the 74C logic family is close to ideal for use in digital systems. Function and pinout compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

All inputs are protected from damage due to static discharge by diode clamps to Vcc and GND. See 7400, 7402, 7404, 7410 and 7420 data for more information on logic and pinouts.

Supply Voltage Range	**3.0V to 15V**
Guaranteed Noise Margin	**1.0V**
Noise Immunity	**0.45 V_{CC} typ.**
Power Consumption	**10 nW/package typ.**
TTL Compatibility	**Fanout of 2 driving 74L**



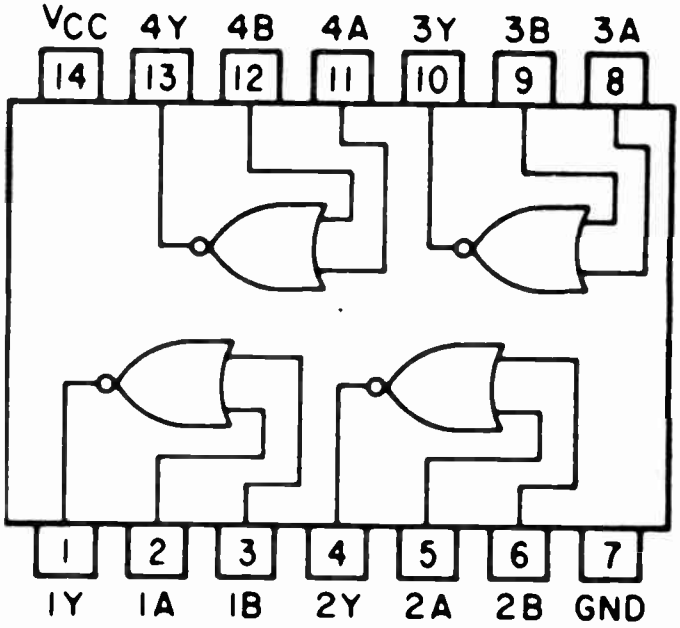
74C00

74C02 QUAD 2-INPUT NOR GATE

These logic gates employ complementary MOS (CMOS) to achieve wide power-supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this, the 74C logic family is close to ideal for use in digital systems. Function and pinout compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

All inputs are protected from damage due to static discharge by diode clamps to Vcc and GND. See 7400, 7402, 7404, 7410 and 7420 data for more information on logic and pinouts.

Supply Voltage Range	**3.0V to 15V**
Guaranteed Noise Margin	**1.0V**
Noise Immunity	**0.45 V_{CC} typ.**
Power Consumption	**10 nW/package typ.**
TTL Compatibility	**Fanout of 2 driving 74L**



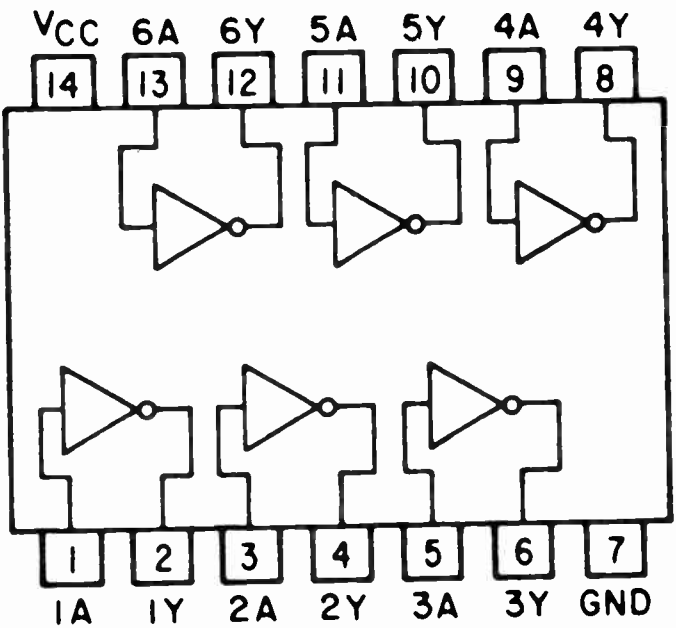
74C02

74C04 HEX INVERTER

These logic gates employ complementary MOS (CMOS) to achieve wide power-supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this, the 74C logic family is close to ideal for use in digital systems. Function and pinout compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

All inputs are protected from damage due to static discharge by diode clamps to Vcc and GND. See 7400, 7402, 7404, 7410 and 7420 data for more information on logic and pinouts.

Supply Voltage Range	**3.0V to 15V**
Guaranteed Noise Margin	**1.0V**
Noise Immunity	**0.45 Vcc typ.**
Power Consumption	**10 nW/package typ.**
TTL Compatibility	**Fanout of 2 driving 74L**



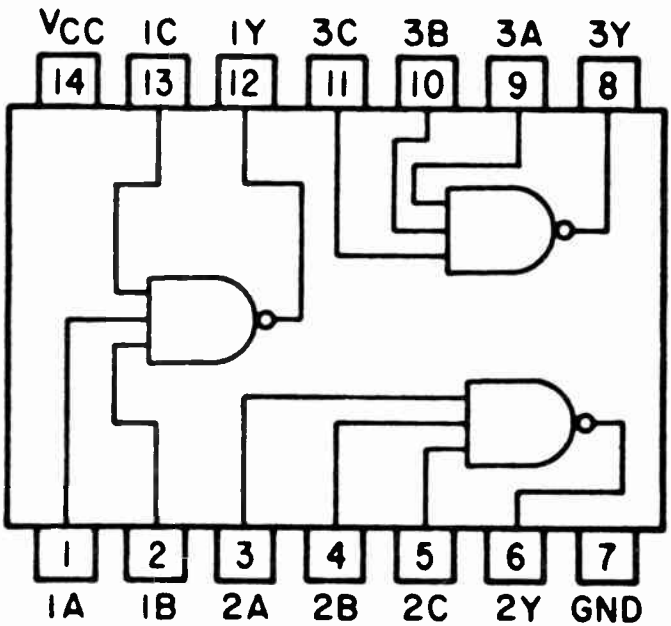
74C04

74C10 TRIPLE 3-INPUT NAND GATE

These logic gates employ complementary MOS (CMOS) to achieve wide power-supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this, the 74C logic family is close to ideal for use in digital systems. Function and pinout compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

All inputs are protected from damage due to static discharge by diode clamps to Vcc and GND. See 7400, 7402, 7404, 7410 and 7420 data for more information on logic and pinouts.

Supply Voltage Range	**3.0V to 15V**
Guaranteed Noise Margin	**1.0V**
Noise Immunity	**0.45 V_{CC} typ.**
Power Consumption	**10 nW/package typ.**
TTL Compatibility	**Fanout of 2 driving 74L**



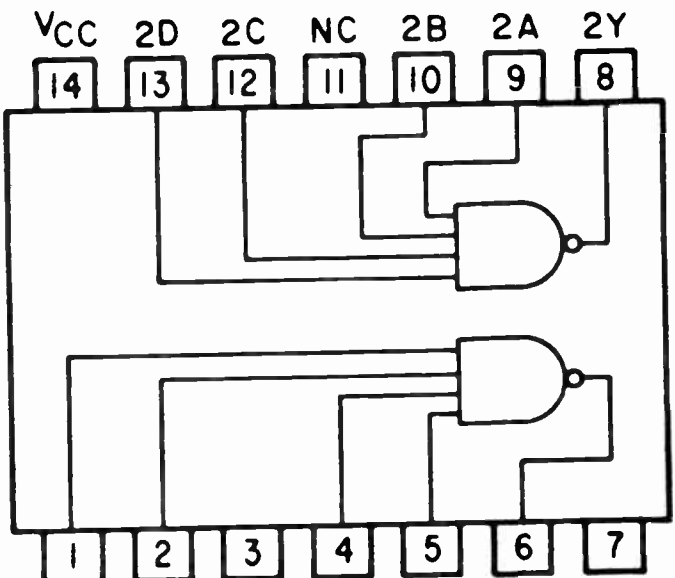
74C10

74C20 DUAL 4-INPUT NAND GATE

These logic gates employ complementary MOS (CMOS) to achieve wide power-supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this, the 74C logic family is close to ideal for use in digital systems. Function and pinout compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

All inputs are protected from damage due to static discharge by diode clamps to Vcc and GND. See 7400, 7402, 7404, 7410 and 7420 data for more information on logic and pinouts.

Supply Voltage Range	**3.0V to 15V**
Guaranteed Noise Margin	**1.0V**
Noise Immunity	**0.45 Vcc typ.**
Power Consumption	**10 nW/package typ.**
TTL Compatibility	**Fanout of 2 driving 74L**

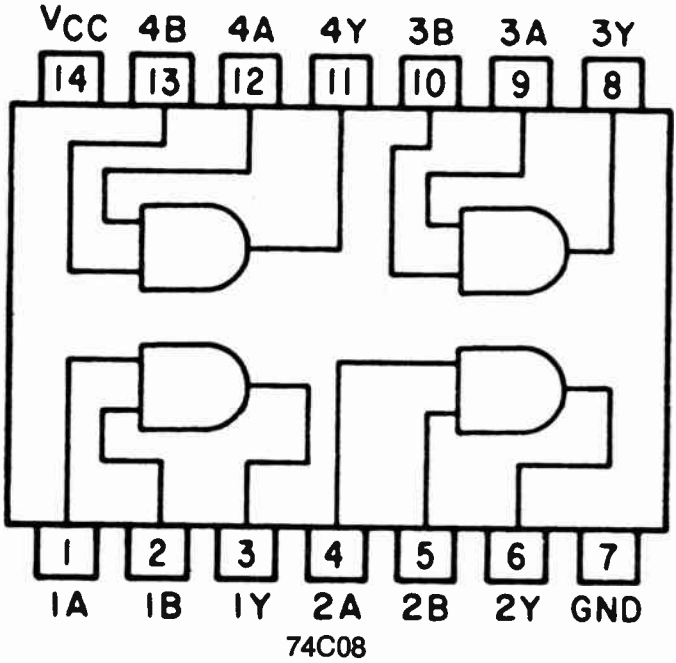


74C20

74C08 QUAD 2-INPUT AND GATE

Employing complementary MOS (CMOS) transistors to achieve wide power-supply operating range, low power consumption and high noise margin, these gates provide basic functions used in the implementation of digital integrated circuit systems. The N-channel and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No DC power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to Vcc and GND. See 7408 and 7486 data for more information on logic and pinouts.

Supply Voltage Range	**3.0V to 15V**
Guaranteed Noise Margin	**1.0V**
Noise Immunity	**0.45 V_{CC} typ.**
TTL Compatibility	**Fanout of 2 driving 74L**
Power Consumption	**10 nW/package typ.**

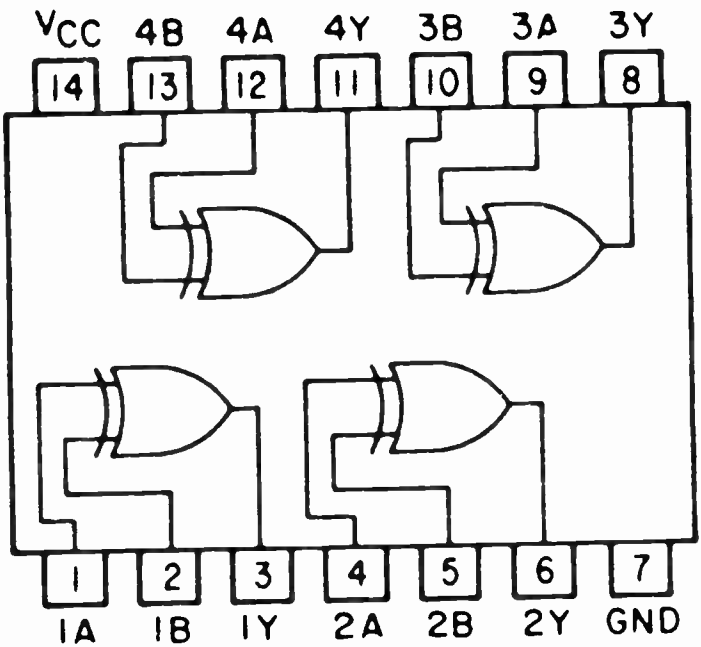


74C08

74C86 QUAD 2-INPUT EXCLUSIVE-OR GATE

Employing complementary MOS (CMOS) transistors to achieve wide power-supply operating range, low power consumption and high noise margin, these gates provide basic functions used in the implementation of digital integrated circuit systems. The N-channel and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No DC power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to Vcc and GND. See 7408 and 7486 data for more information on logic and pinouts.

Supply Voltage Range	**3.0V to 15V**
Guaranteed Noise Margin	**1.0V**
Noise Immunity	**0.45 Vcc typ.**
TTL Compatibility	**Fanout of 2 driving 74L**
Power Consumption	**10 nW/package typ.**



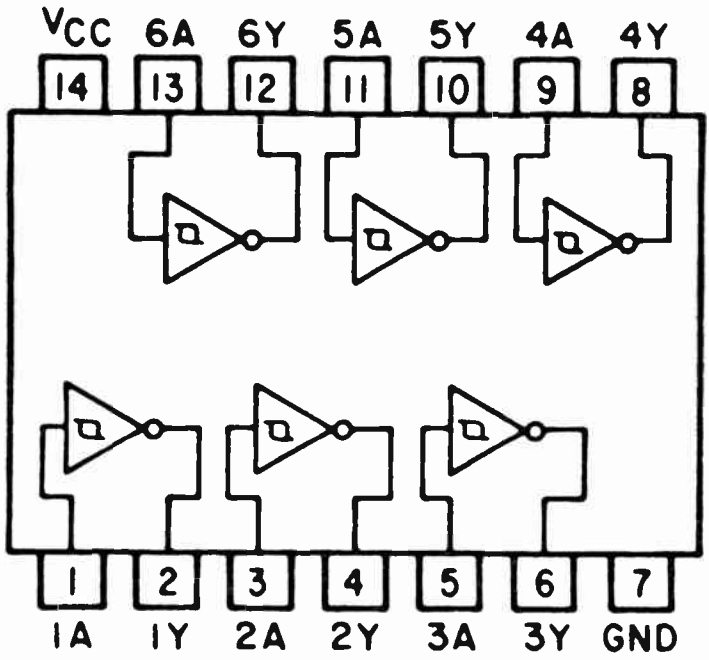
74C86

74C14 HEX SCHMITT TRIGGER

The MM74C14 hex Schmitt trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N-channel and P-channel enhancement transistors. The positive-going and negative-going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ 0.0005V per C at $V_{cc} = 10V$), and hysteresis, $V_{T+} - V_{T-} \geq 0.2\ V_{cc}$ is guaranteed.

All inputs are protected from damage due to static discharge by diode clamps to Vcc and GND. See 7414 data for more information on logic and pinouts.

Supply Voltage Range	**3.0V to 15V**
Noise Immunity	**0.70 V_{cc} typ.**
TTL Compatibility	**Fanout of 2 driving 74L**
Hysteresis	**0.4 V_{cc} typ.** **0.2 V_{cc} guaranteed**



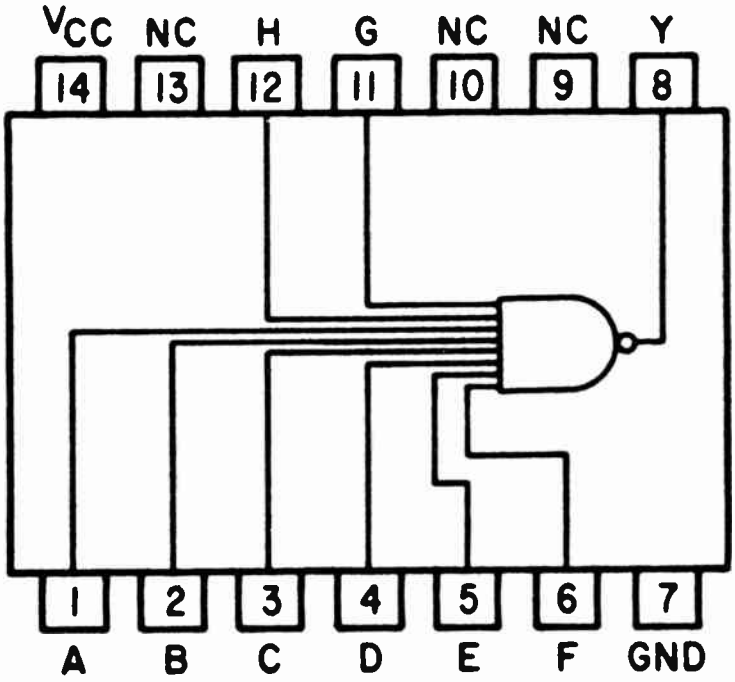
74C14

74C30 8-INPUT NAND GATE

The logic gate employs complementary MOS (CMOS) to achieve wide power-supply operating range, low power consumption and high noise immunity. Function and pinout compatibility with series 54/74 devices minimizes design time for those designers familiar with the standard 54/74 logic family.

All inputs are protected from damage to static discharge by diode clamps to Vcc and GND. See 7430 data for more information on logic and pinouts.

Supply Voltage Range	**3.0V to 15V**
Guaranteed Noise Margin	**1.0V**
Noise Immunity	**0.45 V_{CC} typ.**
TTL Compatibility	**Fanout of 2 driving 74L**

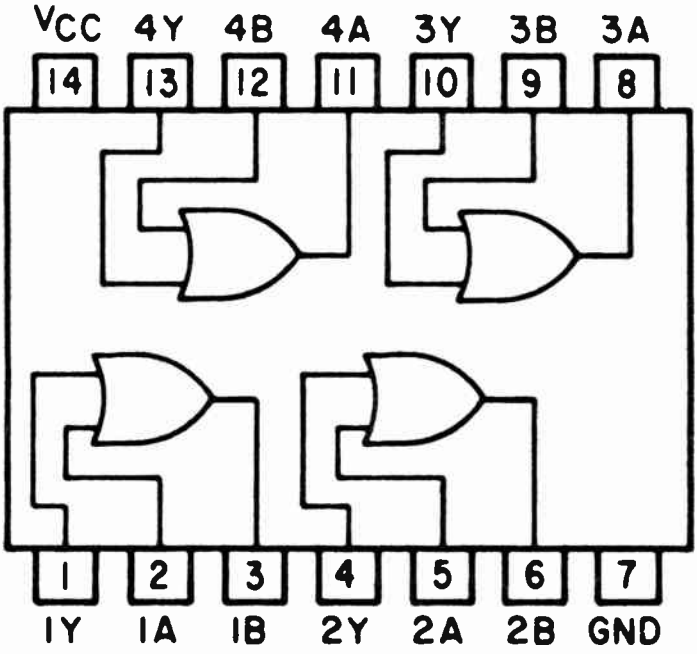


74C30

74C32 QUAD 2-INPUT OR GATE

Employing complementary MOS (CMOS) transistors to achieve low power and high noise margin, these gates provide the basic functions used in the implementation of digital integrated circuit systems. The N-channel and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge damage.

Supply Voltage Range	**3.0V to 15V**
Noise Margin	**1.0V**
Noise Immunity	**0.45 V_{CC} typ.**
TTL Compatibility	**Fanout of 2 driving 74L**

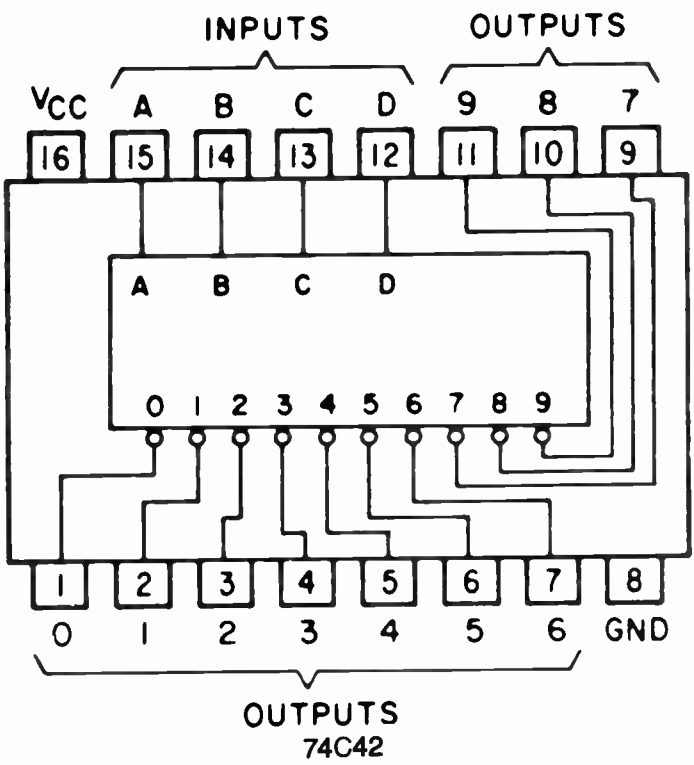


74C32

74C42 BCD-TO-DECIMAL DECODER

The MM74C42 one-of-10 decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N-channel and P-channel enhancement transistors. This decoder produces a logical 0 at the output corresponding to a 4-bit binary input from zero to nine, and a logical 1 at the other outputs. For binary inputs from 10 to 15, all outputs are logical 1. See 7442 data for more information on logic and pinouts.

Supply Voltage Range	**3V to 15V**
Fanout	**Drive 2 LPTTL loads**
Noise Immunity	**0.45 V_{CC} (typ.)**
Power	**50 nW (typ.)**
Speed of Operation	**10 MHz (typ.) with 10V Vcc**

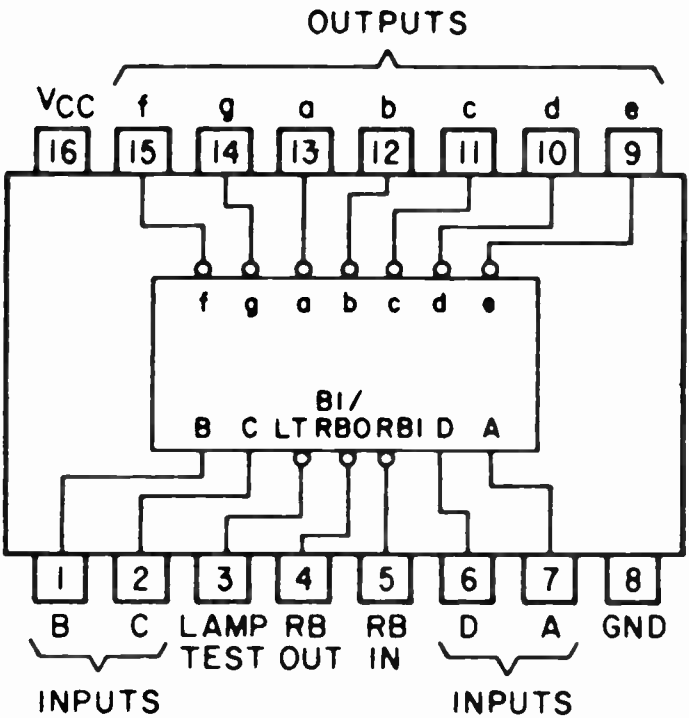


74C42

74C48 BCD-TO-7-SEGMENT DECODER

The MM74C48 BCD-to-7-segment decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N-channel and P-channel enhancement transistors. Seven NAND gates and one driver are connected in pairs to make binary-coded decimal (BCD) data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide test-blanking input/ripple-blanking output, and ripple-blanking inputs. See 7448 data for more information on logic and pinouts.

Supply Voltage Range	**3.0V to 15V**
Guaranteed Noise Margin	**1.0V**
Noise Immunity	**0.45 V_{CC} typ.**
TTL Compatibility	**Fanout of 2 driving 74L**

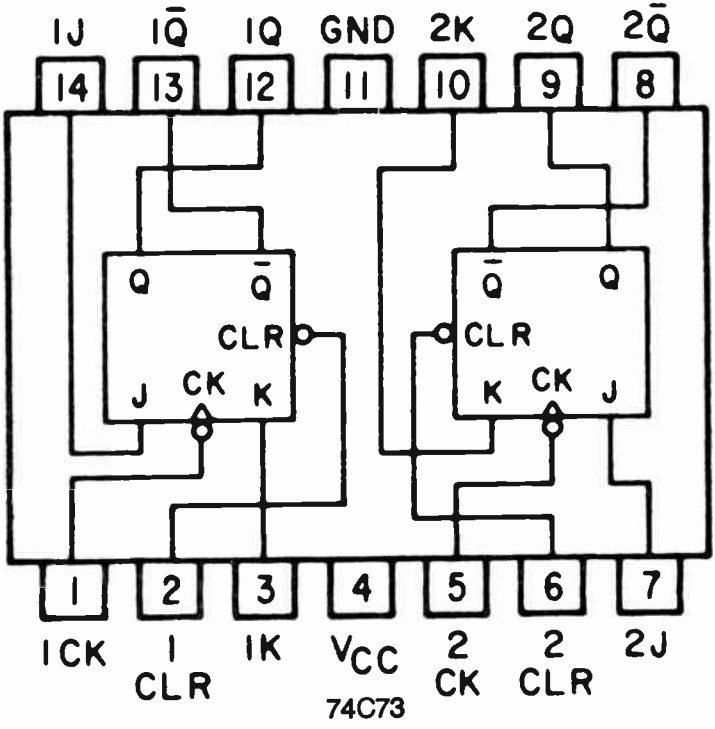


74C48

74C73 DUAL J-K FLIP-FLOPS WITH CLEAR

These dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement transistors. Each flip-flop has independent J, K, clock and clear inputs and Q and $\overline{Q}$ outputs. The MM54C76/MM74C76 flip-flops also include preset inputs and are supplied in 16-pin packages. These flip-flops are edge-sensitive to the clock input and change state on the negative-going transition of the clock pulses. Clear or preset is independent of the clock and is accomplished by a low level on the respective input. See 7473, 7476 and 74107 data for logic information and pinouts.

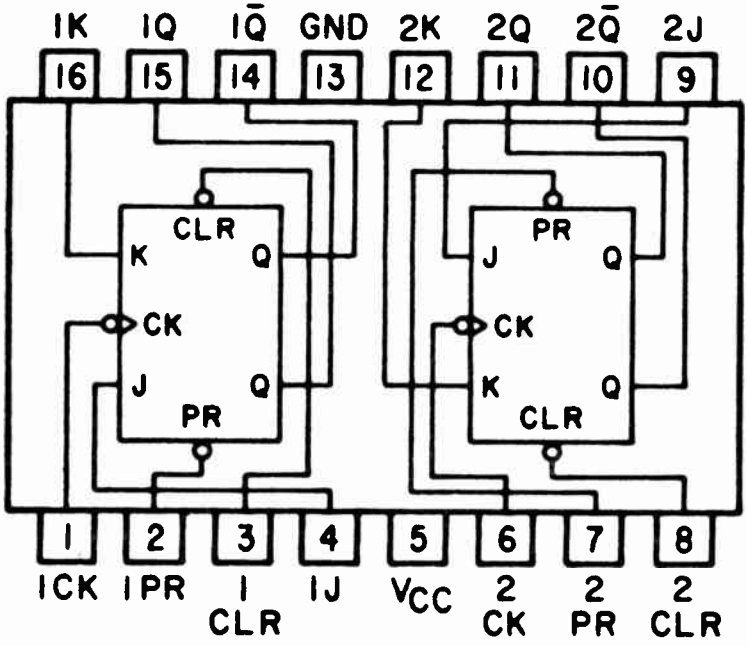
Supply Voltage Range	**3V to 15V**
Fanout	**Drive 2 LPTTL loads**
Noise Immunity	**0.45 V_{CC} (typ.)**
Power	**50 nW (typ.)**
Speed of Operation	**10 MHz (typ.) with 10V Supply**



74C76 DUAL J-K FLIP-FLOPS WITH CLEAR AND PRESET

These dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement transistors. Each flip-flop has independent J, K, clock and clear inputs and Q and $\overline{Q}$ outputs. The MM54C76/MM74C76 flip-flops also include preset inputs and are supplied in 16-pin packages. These flip-flops are edge-sensitive to the clock input and change state on the negative-going transition of the clock pulses. Clear or preset is independent of the clock and is accomplished by a low level on the respective input. See 7473, 7476 and 74107 data for logic information and pinouts.

Supply Voltage Range	**3V to 15V**
Fanout	**Drive 2 LPTTL loads**
Noise Immunity	**0.45 V_{CC} (typ.)**
Power	**50 nW (typ.)**
Speed of Operation	**10 MHz (typ.) with 10V Supply**

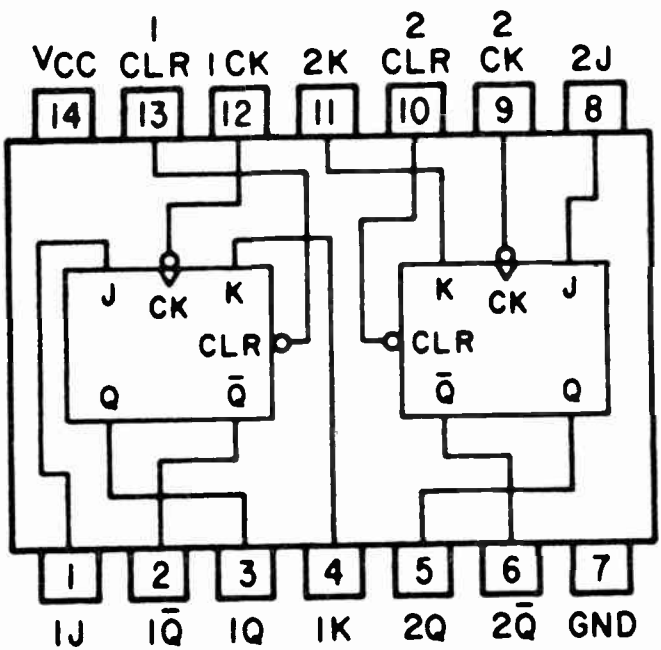


74C76

74C107 DUAL J-K FLIP-FLOPS WITH CLEAR

These dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement transistors. Each flip-flop has independent J, K, clock and clear inputs and Q and $\overline{Q}$ outputs. The MM54C76/MM74C76 flip-flops also include preset inputs and are supplied in 16-pin packages. These flip-flops are edge-sensitive to the clock input and change state on the negative-going transition of the clock pulses. Clear or preset is independent of the clock and is accomplished by a low level on the respective input. See 7473, 7476 and 74107 data for logic information and pinouts.

Supply Voltage Range	**3V to 15V**
Fanout	**Drive 2 LPTTL loads**
Noise Immunity	**0.45 V_{CC} (typ.)**
Power	**50 nW (typ.)**
Speed of Operation	**10 MHz (typ.) with 10V Supply**

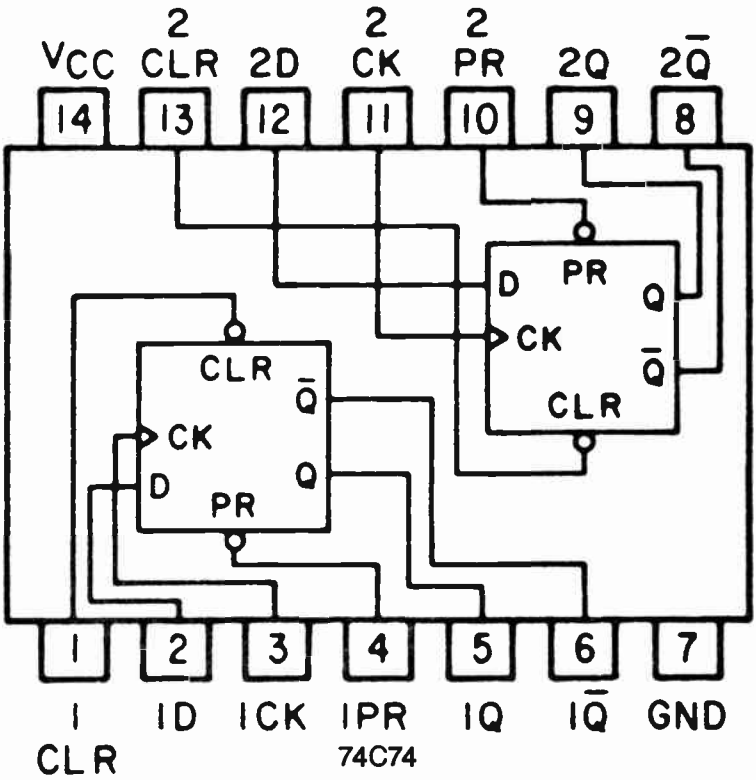


74C107

74C74 DUAL D FLIP-FLOP

The MM74C74 dual D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N - and P-channel enhancement transistors. Each flip flop has independent data, preset, clear and clock inputs and Q and Q outputs. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset or clear is independent of the clock and accomplished by a low level at the preset or clear input. See 7474 data for more logic information and pinouts.

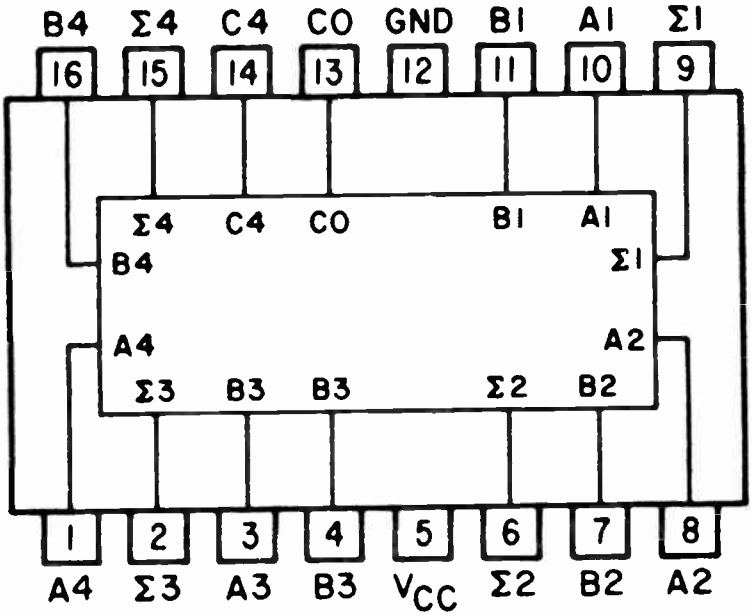
Supply Voltage Range	**3V to 15V**
Fanout	**Drive 2# LPTTL loads**
Noise Immunity	**0.45 V_{CC} (typ.)**
Power	**50 nW (typ.)**
Speed of Operation	**10 MHz (typ.) with 10V supply**



74C83 4-BIT BINARY FULL ADDER

The MM74C83 4-bit binary full adder performs the addition of two 4-bit binary numbers. A carry input (Co) is included. The sum (Σ) outputs are provided for each bit, and the resultant carry (C_4) is obtained from the fourth bit. Because the carry-ripple-time is the limiting delay in the addition of a long word length, carry look ahead circuitry has been included in the design to minimize this delay. Also, the logic levels of the input and output, including the carry, are in their true form. Thus the end-around carry is accomplished without the need for level inversion.

Supply Voltage Range	**3V to 15V**
Guaranteed Noise Margin	**1V**
Noise Immunity	**0.45 V_{CC} typ.**
TTL Compatibility	**Fanout of 2 driving 74L**
Carry Ripple (Co to C_4)	**50 ns typ. @ V_{CC} = 10V and C_L = 50 pF**
Summing	**125 ns typ. @ V_{CC} = 10V and C_L = 50 pF**

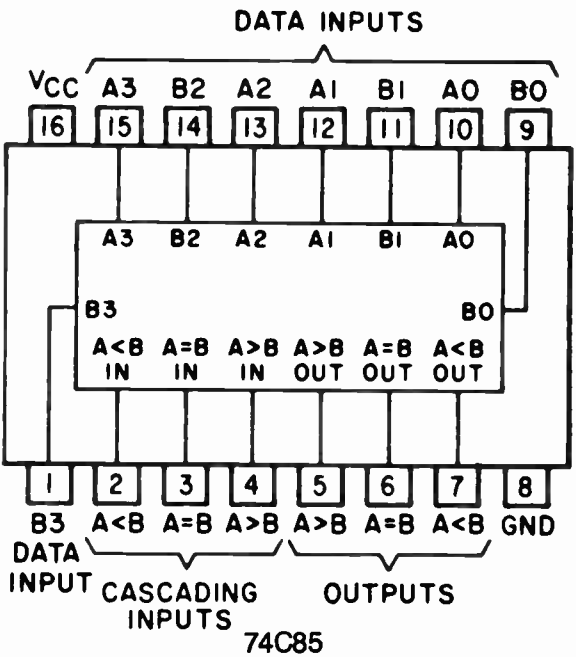


74C83

74C85 4-BIT MAGNITUDE COMPARATOR

The MM74C85 is a 4-bit magnitude comparator which will perform comparison of straight binary or BCD codes. The circuit consists of eight comparing inputs (A0, A1, A2, A3, B0, B1, B2 and B3), three cascading inputs (A>B, A<B and A=B), and three outputs (A>B, A<B and A=B). This device compares two 4-bit words (A and B) and determines whether they are greater than, less than, or equal to each other by a high level on the appropriate output. For words greater than four bits, units can be cascaded by connecting the outputs (A>B, A<B, and A=B) of the least significant stage to the cascade inputs (A>B, A<B and A=B) of the next significant stage. In addition, the least significant stage must have a high-level voltage ($V_{in(1)}$) applied to the A=B input and low-level voltages ($V_{in(0)}$) applied to A>B and A<B inputs.

Supply Voltage Range	**3.0V to 15V**
Guaranteed Noise margin	**1.0V**
Noise Immunity	**0.45 V_{CC} typ.**
TTL Compatibility	**Fanout of 2 driving 74L**



74C89 64-BIT 3-STATE RANDOM ACCESS READ/WRITE MEMORY

The MM74C89 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a write enable line and a memory enable line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register latches the address information on the positive to negative transition of the memory enable input. The four TRI-STATE® data output lines working in conjunction with the memory enable input provides for easy memory expansion.

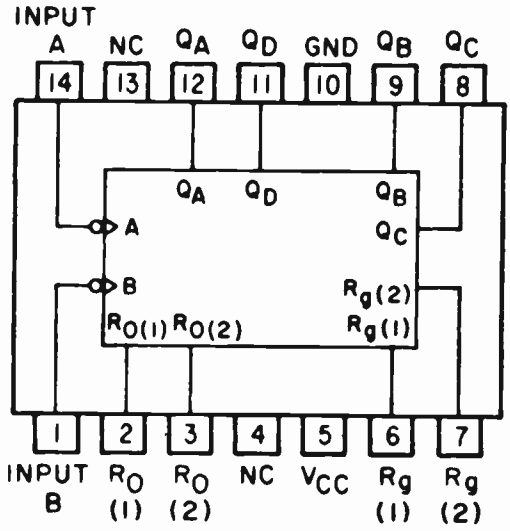
- **Address Operation:** Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable). Note that the timing is different than the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.
- **Write Operation:** Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.
- **Read Operation:** The complement of the information that was written into the memory is nondestructively read out at the four outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high. When the device is writing or disabled, the output assumes a TRI-STATE® (high Z) condition. See 7489 for more logic information and pinout.

Supply Voltage Range	**3.0V to 15V**
Guaranteed Noise Margin	**1.0V**
Noise Immunity	**0.45 V_{CC} typ.**
TTL Compatibility	**Fanout of 2 driving 74L**
Power Consumption	**100 nW/package typ. @ V_{CC} = 5V**
Access Time	**130 ns typ. at V_{CC} = 10V**

74C90 4-BIT DECADE COUNTER

The MM74C90 decade counter and the MM74C93 binary counter are complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. The 4-bit decade counter can be reset to zero or preset to nine by applying appropriate logic level on the R_{01}, R_{02}, R_{91} and R_{92} inputs. Also, a separate flip-flop on the A-bit enables the user to operate it as a divide-by-two, -five or -10 frequency counter. The 4-bit binary counter can be reset to zero by applying high logic level on inputs R_{01} and R_{02}. Also, a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, -8 or -16 divider. Counting occurs on the negative-going edge of the input pulse. See 7490 and 7493 data for more information on logic and pinouts. All inputs are protected against static discharge damage.

Supply Voltage Range	**3V to 15V**
Guaranteed Noise Margin	**1V**
Noise Immunity	**0.45 V_{CC} (typ.)**
Low Power TTL Compatibility	**Fanout of 2 driving 74L**

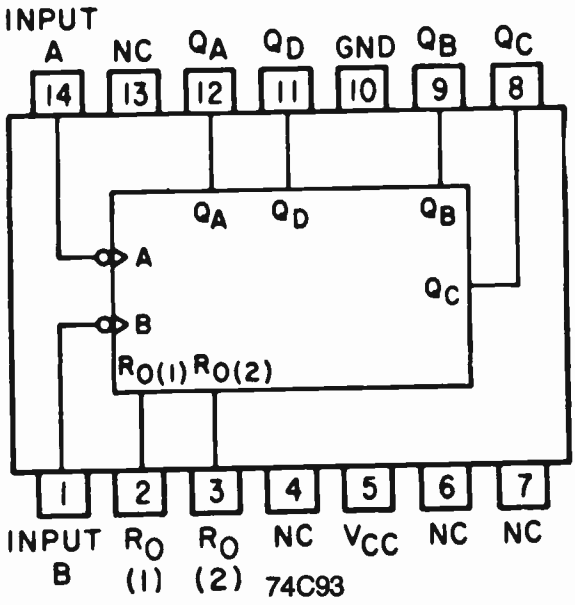


74C90

74C93 4-BIT BINARY COUNTER

The MM74C90 decade counter and the MM74C93 binary counter are complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. The 4-bit decade counter can be reset to zero or preset to nine by applying appropriate logic level on the R_{01}, R_{02}, R_{91} and R_{92} inputs. Also, a separate flip-flop on the A-bit enables the user to operate it as a divide-by-two, -five or -10 frequency counter. The 4-bit binary counter can be reset to zero by applying high logic level on inputs R_{01} and R_{02}. Also, a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, -8 or -16 divider. Counting occurs on the negative-going edge of the input pulse. See 7490 and 7493 data for more information on logic and pinouts. All inputs are protected against static discharge damage.

Supply Voltage Range	**3V to 15V**
Guaranteed Noise Margin	**1V**
Noise Immunity	**0.45 V_{CC} (typ.)**
Low Power TTL Compatibility	**Fanout of 2 driving 74L**

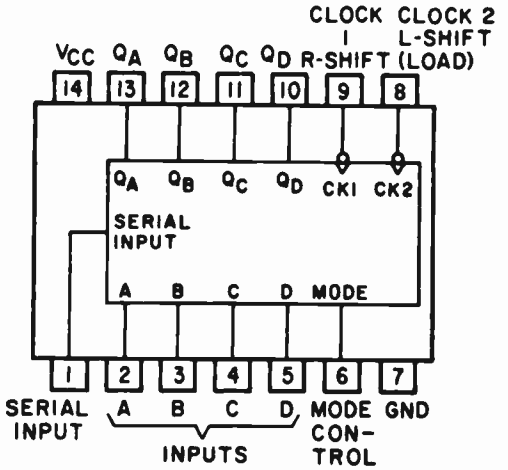


74C95 4-BIT RIGHT-SHIFT/LEFT-SHIFT REGISTER

This 4-bit shift register is a monolithic complementary MOS (CMOS) integrated circuit composed of four D flip-flops. This register will perform right shift or left shift operations dependent upon the logical input level to the mode control. A number of these registers can be connected in series to form an N-bit right shift or left shift register.

When a logical 0 level is applied to the mode control input, the output of each flip flop is coupled to the D input of the succeeding flip-flop. Right shift operation is performed by clocking at the clock 1 input, and serial data entered at the serial input, clock 2 and parallel inputs A through D are inhibited. With a logical 1 level applied to the mode control, outputs to succeeding stages are decoupled and parallel loading is possible. Or with external interconnection, shift left operation can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop, and serial data are entered at input D. See 7495 data for more information on logic and pinout.

Speed of Operation	**10 MHz typ. V_{CC} = 10V, C_L = 50 pF**
Noise Immunity	**0.45 V_{CC} typ.**
Power	**100 nW typ.**
TTL Compatibility	**Drive 2 LTTL loads**
Supply Voltage Range	**3V to 15V**



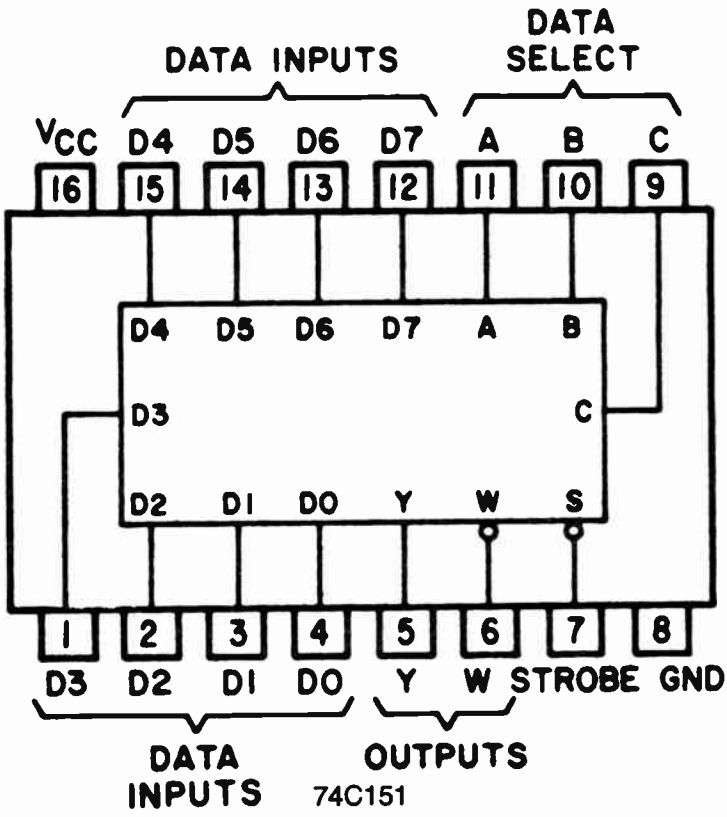
74C95

74C151 8-CHANNEL DIGITAL MULTIPLEXER

The MM74C151 multiplexer is a monolithic complementary MOS (CMOS) integrated circuit constructed with N-channel and P-channel enhancement transistors. This data selector/multiplexer contains on-chip binary decoding. Two outputs provide true (output Y) and complement (output W) data. A logical 1 on the strobe input forces W to a logical 1 and Y to a logical 0.

All inputs are protected against electrostatic effects. See 74151 data for more information on logic and pinout.

Supply Voltage Range	**3V to 15V**
TTL Compatibility	**Drive 2 LPTTL loads**
Noise Immunity	**0.45 V_{CC} typ.**
Power	**50 nW typ.**

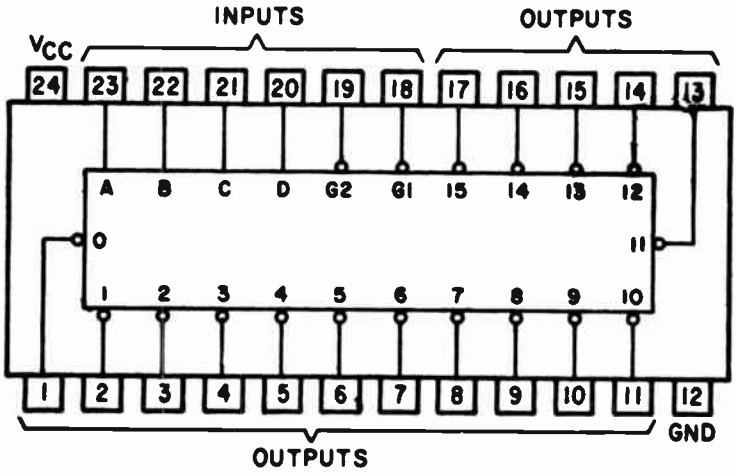


74C154 4-LINE TO 16-LINE DECODER/DEMULTIPLEXER

The MM74C154 one-of-16 decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N-channel and P-channel enhancement transistors. The device is provided with two strobe inputs, both of which must be in the logical 0 state for normal operation. If either strobe input is in the logical 1 state, all 16 outputs will go to the logical 1 state.

To use the product as a demultiplexer, one of the strobe inputs serves as a data input terminal, while the other strobe input must be maintained in the logical 0 state. The information will then be transmitted to the selected output as determined by the four-line input address. See 74154 data for more information on logic and pinout.

Supply Voltage Range	**3V to 15V**
TTL Compatibility	**Drive 2 LPTTL loads**
Noise Margin	**1V guaranteed**
Noise Immunity	**0.45 V_{CC} typ.**

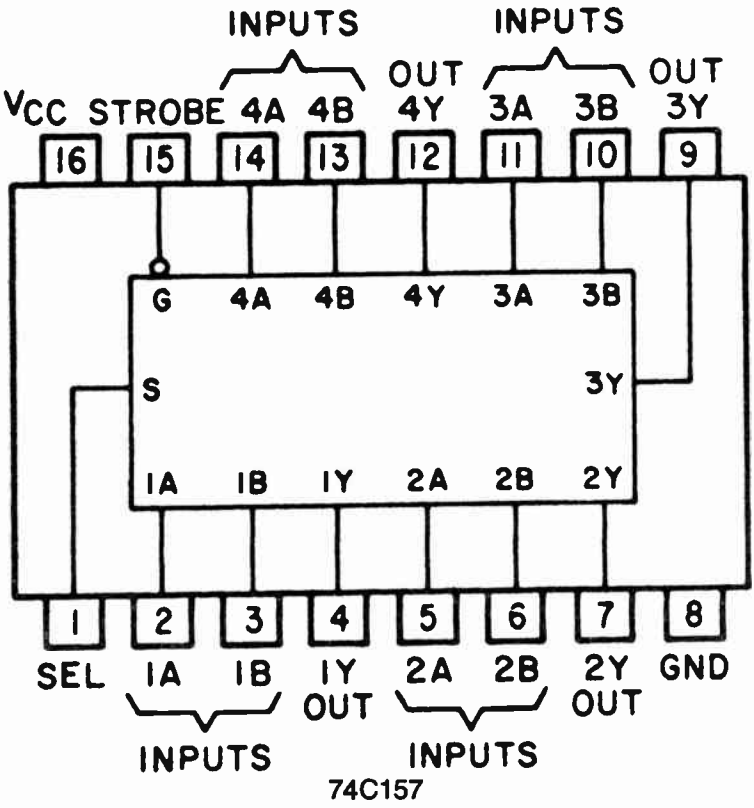


74C154

74C157 QUAD 2-INPUT MULTIPLEXERS

These multiplexers are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement transistors. They consist of four 2-input multiplexers with a common select and enable inputs. When the enable input is at logical 0 the four outputs assume the values as selected from the inputs. When the enable input is at logical 1, the outputs assume logical 0. Select decoding is done internally, resulting in a single select input only. See 74157 data for more information on logic and pinout.

Supply Voltage Range	**3V to 15V**
Noise Immunity	**0.45 V_{CC} typ.**
Power	**50 nW (typ.)**
TTL Compatibility	**Drive 2 LPTTL loads**



74C157

74C160 DECADE COUNTER

These synchronous presettable-up counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. They feature an internal carry look-ahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the C162 and C163 is synchronous, and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the C160 and C161 is asynchronous, and a low level at the clear input sets all four outputs low, regardless of the state of the clock.

Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low. See 74160, 74161, 74162 and 74163 for more logic information and pinout.

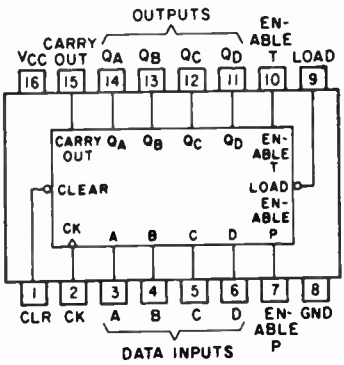
Noise Margin	**1V guaranteed**
Noise Immunity	**0.45 V_{CC} typ.**
TTL Compatibility	**Drives 2 LPTTL loads**
Supply Voltage Range	**3V to 15V**

These synchronous presettable-up counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. They feature an internal carry look-ahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the C162 and C163 is synchronous, and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the C160 and C161 is asynchronous, and a low level at the clear input sets all four outputs low, regardless of the state of the clock.

Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low. See 74160, 74161, 74162 and 74163 for more logic information and pinout.

Noise Margin	**1V guaranteed**
Noise Immunity	**0.45 V_{CC} typ.**
TTL Compatibility	**Drives 2 LPTTL loads**
Supply Voltage Range	**3V to 15V**



74C161

74C162 DECADE COUNTER

These synchronous presettable-up counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. They feature an internal carry look-ahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the C162 and C163 is synchronous, and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the C160 and C161 is asynchronous, and a low level at the clear input sets all four outputs low, regardless of the state of the clock.

Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low. See 74160, 74161, 74162 and 74163 for more logic information and pinout.

Noise Margin	**1V guaranteed**
Noise Immunity	**0.45 V_{CC} typ.**
TTL Compatibility	**Drives 2 LPTTL loads**
Supply Voltage Range	**3V to 15V**

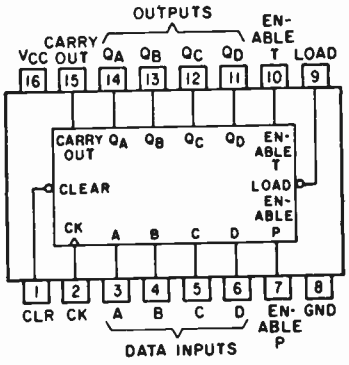
74C163 BINARY COUNTER

These synchronous presettable-up counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. They feature an internal carry look-ahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the C162 and C163 is synchronous, and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the C160 and C161 is asynchronous, and a low level at the clear input sets all four outputs low, regardless of the state of the clock.

Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low. See 74160, 74161, 74162 and 74163 for more logic information and pinout.

Noise Margin	**1V guaranteed**
Noise Immunity	**0.45 V_{CC} typ.**
TTL Compatibility	**Drives 2 LPTTL loads**
Supply Voltage Range	**3V to 15V**



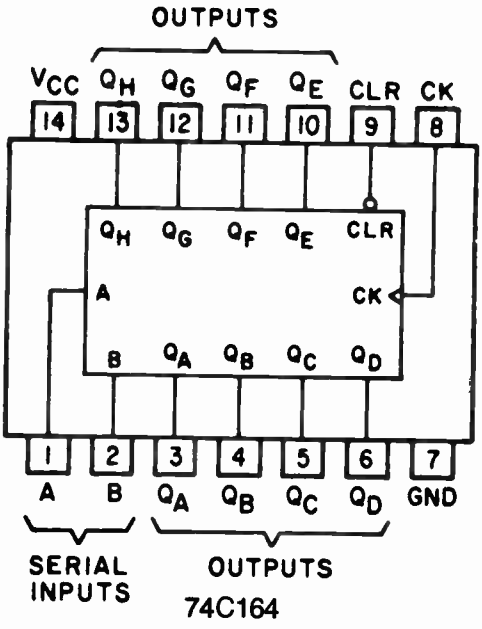
74C163

74C164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

The MM74C164 shift registers is a monolithic complementary MOS (CMOS) integrated circuit constructed with N-channel and P-channel enhancement transistors. These 8-bit shift registers have gated serial inputs and clear. Each register bit is a D-type master-slave flip-flop. A high-level input enables the other input which will then determine the state of the flip flop.

Data is serially shifted in and out of the 8-bit register during the positive-going transition of clock pulse. Clear is independent of the clock and accomplished by a low level at the clear input. All inputs are protected against electrostatic effects. See 74164 data for more information on logic and pinout.

Voltage Range	**3V to 15V**
TTL Compatibility	**Drive 2 LPTTL loads**
Noise Immunity	**0.45 V_{CC} typ.**
Power	**50 nW typ.**
Speed of Operation	**8.0 MHz typ. with 10V supply**

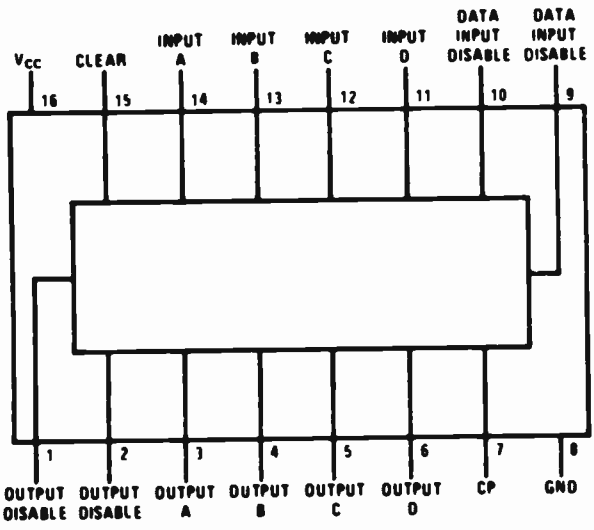


74C173 TRI-STATE® QUAD D FLIP-FLOP

The MM74C173 TRI-STATE® Quad D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N-channel and P-channel enhancement transistors. The four D-type flip-flops operate synchronously from a common clock. The TRI-STATE® output allows the device to be used in bus organized systems. The outputs are placed in the TRI-STATE® mode when either of the two output disable pins are in the logic 1 level. The input disable allows the flip-flop to remain in their present states without disrupting the clock. If either of the two input disables are taken to a logic 1 level, the Q outputs are fed back to the inputs. In this manner, the flip-flops do not change state.

Clearing is enabled by taking the input to a logic 1 level. Clocking occurs on the positive-going transition. See 74173 data for more information on logic and pinout.

Supply Voltage Range	**3V to 15V**
TTL Compatibility	**Drive 2 LPTTL loads**
Noise Immunity	**0.45 V_{CC} typ.**
Power	
Speed of Operation	



TOP VIEW

74C173

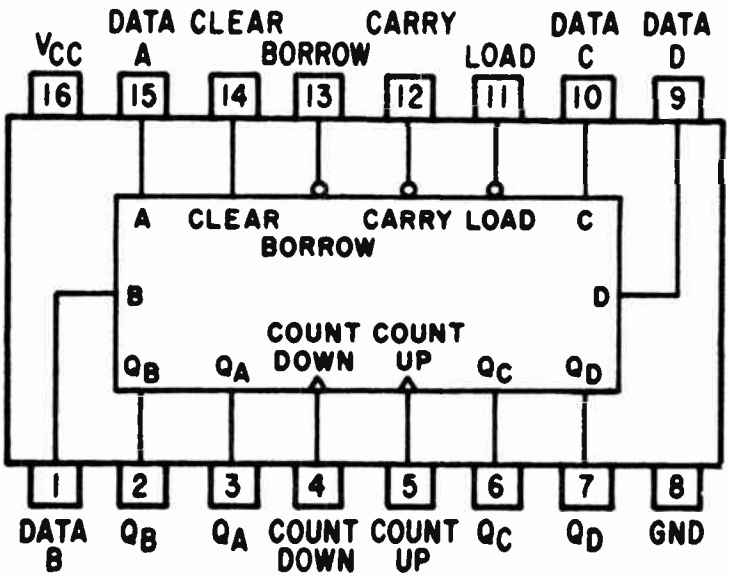
74C192 SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTER

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The MM74C192 is a BCD counter. The MM74C193 is a binary counter.

Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive-going transition of this clock.

These counters feature preset inputs that are set when load is a logical 0 and a clear which forces all outputs to 0 when it is at logical 1. The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry. See 74192 and 74193 data for logic information and pinout.

Noise Margin	**1V guaranteed**
TTL Compatibility	**Drive 2 LPTTL loads**
Supply Range	**3V to 15V**
Noise Immunity	**0.45 V_{CC} typ.**



INPUTS: 1, 4, 5, 9, 10, 11, 14, 15
OUTPUTS: 2, 3, 6, 7, 12, 13

74C192

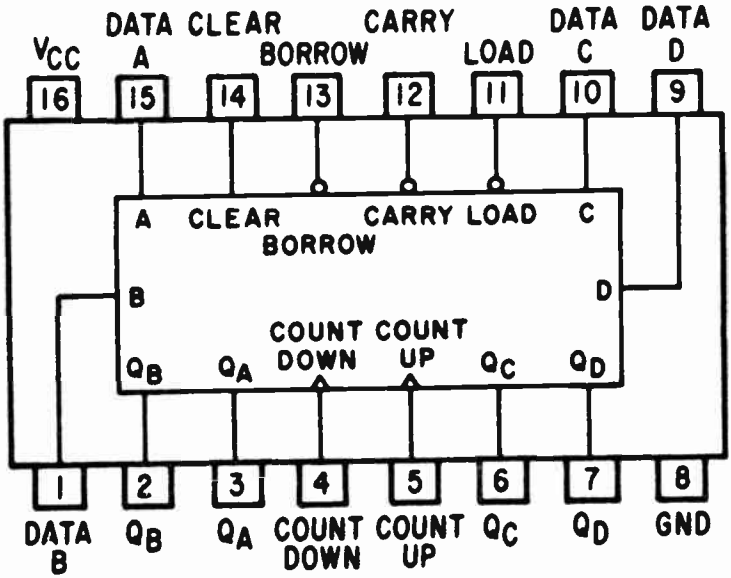
74C193 SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTER

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The MM74C192 is a BCD counter. The MM74C193 is a binary counter.

Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive-going transition of this clock.

These counters feature preset inputs that are set when load is a logical 0 and a clear which forces all outputs to 0 when it is at logical 1. The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry. See 74192 and 74193 data for logic information and pinout.

Noise Margin	1V guaranteed
TTL Compatibility	Drive 2 LPTTL loads
Supply Range	3V to 15V
Noise Immunity	0.45 V_{CC} typ.



INPUTS: 1, 4, 5, 9, 10, 11, 14, 15
OUTPUTS: 2, 3, 6, 7, 12, 13

74C193

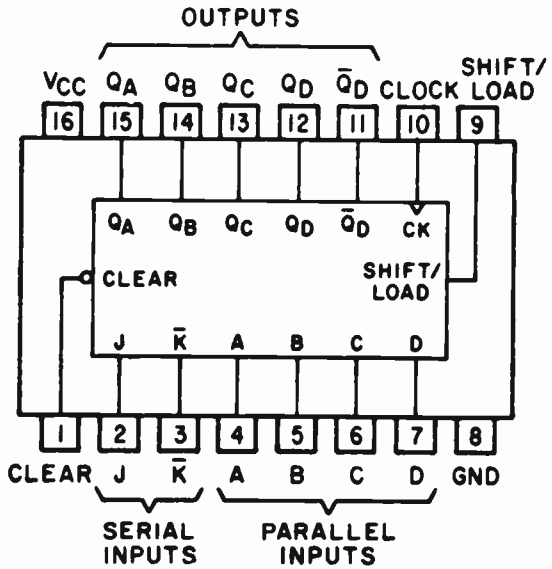
74C195 4-BIT REGISTERS

The MM74C195 CMOS 4-bit register features parallel inputs, parallel outputs, J-K serial inputs, shift/load control input and a direct overriding clear. Two modes of operation are possible: parallel load and shift in direction Q_A towards Q_D.

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited.

Serial shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs allow the first stage to perform as a J-$\overline{K}$, D or T-type flip-flop as shown in the truth table. See 74195 data for logic information and pinout.

Speed of Operation	**8.5 MHz (typ.) with 10V supply and 50 pF load**
Noise Immunity	**0.45 V_{CC} (typ.)**
Power	**100 nW (typ.)**
TTL Compatible	**Drive 2 LPTTL loads**

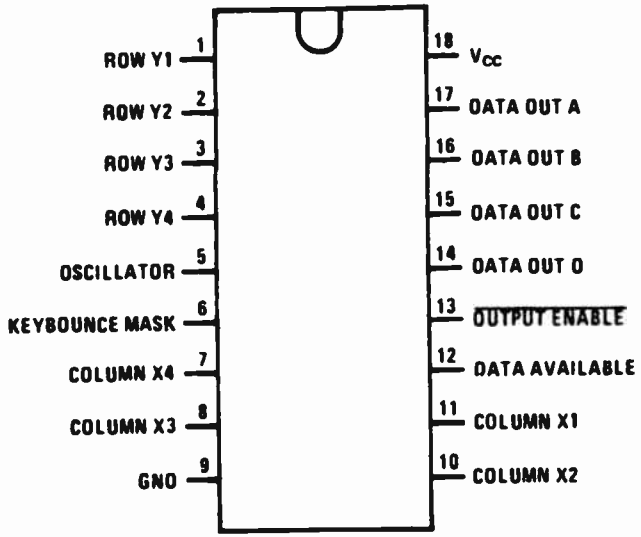


74C195

74C922 16-KEY ENCODER

These CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pullup devices that permit switches with up to 50 kΩ of resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A data available output goes to a high level when a valid keyboard entry has been made. The data available output returns to a low level when the entered key is released, even if another key is depressed. The data available will return high to indicate acceptance of the new key after a normal debounce period; this two-key roll over is provided between any two switches.

An internal register remembers the last key pressed even after the key is released. The TRI-STATE® outputs provide for easy expansion and bus operation and are LPTTL compatible.

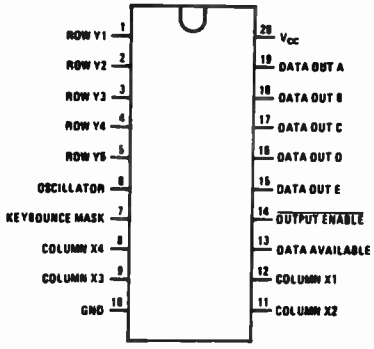


74C922

74C923 20-KEY ENCODER

These CMOS key encloders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pullup devices that permit switches with up to 50 kΩ of resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A data available output goes to a high level when a valid keyboard entry has been made. The data available output returns to a low level when the entered key is released, even if another key is depressed. The data available will return high to indicate acceptance of the new key after a normal debounce period; this two-key roll over is provided between any two switches.

An internal register remembers the last key pressed even after the key is released. The TRI-STATE® outputs provide for easy expansion and bus operation and are LPTTL compatible.



74C923

Truth Table

SWITCH POSITION	0 Y1,X1	1 Y1,X2	2 Y1,X3	3 Y1,X4	4 Y2,X1	5 Y2,X2	6 Y2,X3	7 Y2,X4	8 Y3,X1	9 Y3,X2	10 Y3,X3	11 Y3,X4	12 Y4,X1	13 Y4,X2	14 Y4,X3	15 Y4,X4	16 Y5*,X1	17 Y5*,X2	18 Y5*,X3	19 Y5*,X4
DATA A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
DATA B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
DATA C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
CODE D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
CODE E*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

*Omit for MM54C922/MM74C922

74C927, 74C928 4-DIGIT COUNTERS WITH MULTIPLEXED 7-SEGMENT OUTPUT DRIVERS

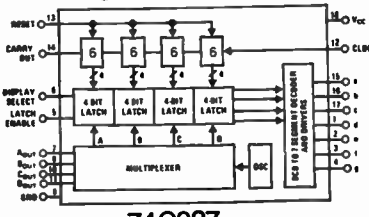
These CMOS counters consist of a 4-digit counter, an internal output latch, NPN output sourcing drivers for a 7-segment display, and an internal multiplexing circuitry with four multiplexing outputs. The multiplexing circuit has its own free-running oscillator, and requires no external clock. The counters advance on the negative edge of the clock. A high signal on the reset input will reset the counter to zero, and reset the carry out low. A low signal on the latch enable input will latch the number in the counters into the internal output latches. A high signal on the display select input will select the number in the counter to be displayed; a low level signal on the display select will select the number in the output latch to be displayed.

The MM74C925 is a 4-decade counter and has latch enable, clock and reset inputs. The MM74C926 is like the MM74C925, except that it has a display select and a carry out used for cascading counters. The carry out signal goes high at 6000 and goes back low at 0000.

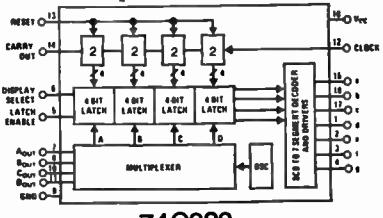
The MM74C927 is like the MM74C926, except the second most significant digit divides by 6 rather than 10. Thus, if the clock input frequency is 10 Hz, the display would read tenths of seconds and minutes (i.e., 9:59.9).

The MM74C928 is like the MM74C926, except the most significant digit divides by 2 rather than 10 and the carry out is an overflow indicator which is high at 2000 and goes back low only when the counter is reset. Thus, this is a 3½-digit counter.

Supply Voltage Range	**3V to 6V**
Guaranteed Noise Margin	**1V**
Noise Immunity	**0.45 Vcc typ.**
Segment Sourcing Current	**40 mA @ Vcc – 1.6V, Vcc = 5V**



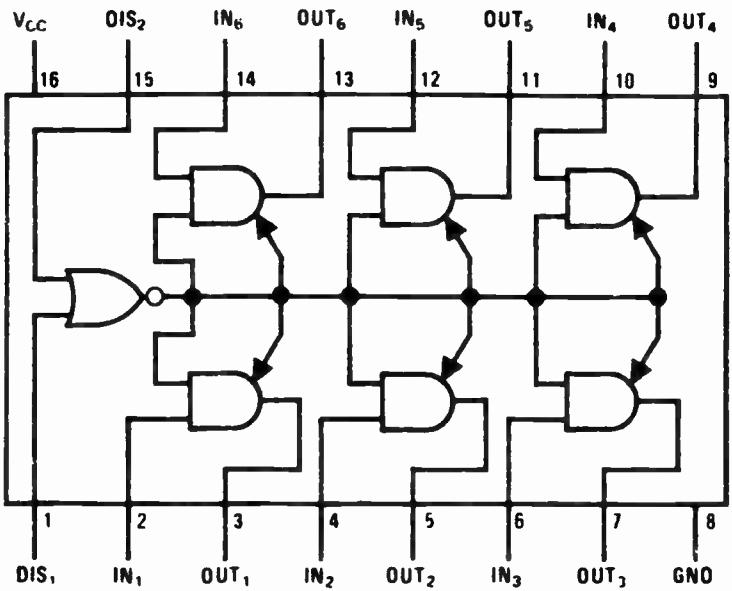
74C927



74C928

These gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. The MM80C95 and the MM80C97 convert CMOS or TTL outputs to TRI-STATE® outputs with no logic inversion. The MM80C96 and MM80C98 provide the logical opposite of the input signal. The MM80C95 and MM80C96 have common TRI-STATE ® controls for all six devices. The MM80C97 and MM80C98 have two TRI-STATE® controls: one for two devices and one for the other four devices. Inputs are protected from damage due to static discharge by diode clamps to Vcc and GND.

Supply Voltage Range	**3.0V to 15V**
Guaranteed Noise Margin	**1.0V**
Noise Immunity	**0.45 V_{CC} (typ.)**
TTL Compatibility	**Drive 1 TTL load**



80C95

These gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N-channel and P-channel enhancement mode transistors. The MM80C95 and the MM80C97 convert CMOS or TTL outputs to TRI-STATE® outputs with no logic inversion. The MM80C96 and MM80C98 provide the logical opposite of the input signal. The MM80C95 and MM80C96 have common TRI-STATE ® controls for all six devices. The MM80C97 and MM80C98 have two TRI-STATE® controls: one for two devices and one for the other four devices. Inputs are protected from damage due to static discharge by diode clamps to Vcc and GND.

Supply Voltage Range	**3.0V to 15V**
Guaranteed Noise Margin	**1.0V**
Noise Immunity	**0.45 Vcc (typ.)**
TTL Compatibility	**Drive 1 TTL load**

Section Two

Exotic CMOS

Certain exotic ICs of the CMOS family are quite popular today in both industry and hobby. A handful are covered here, with information normally supplied with any CMOS devices.

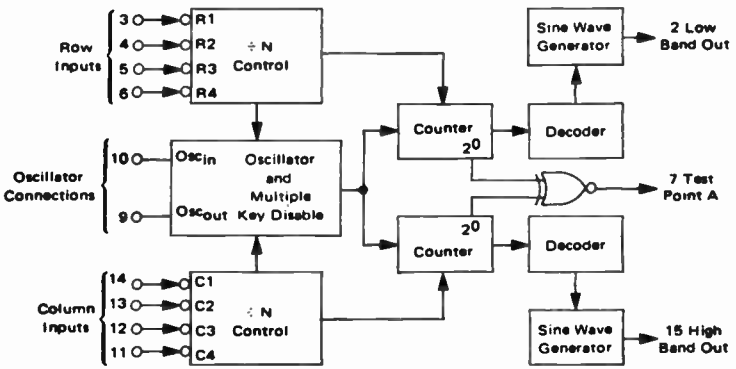
Exotic CMOS Chip Listing

14000-Series Exotic CMOS

14410 TONE ENCODER

The 14410 two-of-eight tone encoder is constructed with complementary MOS (CMOS) enhancement mode devices. It is designed to accept digital inputs in a two-of-eight code format and to digitally synthesize the high-band and low-band sine waves specified by telephone tone dialing systems. The inputs are normally originated from a 4 by 4 matrix keypad, which generates four row and four column input signals in a two-of-eight code format (1 row and 1 column are simultaneously connected to Vss). The master clocking for the 14410 is achieved from a crystal-controlled oscillator which is included on the chip. Internal clocks, which operate the logic, are enabled only by one or more row and column signals being activated simultaneously. The two sine wave outputs have NPN bipolar structures on the same substrate which allows for low output impedance and large source currents. Applications of this device include telephone tone dialing, radio and mobile telephones, process control, point-of-sale terminals and credit card verification terminals.

Noise Immunity	**= 45% of V_{DD} Typical**
Supply Voltage Range	**= 4.4 V_{DC} to 6.0 V_{dc}**
Frequency Accuracy	**± 0.2%**



14410

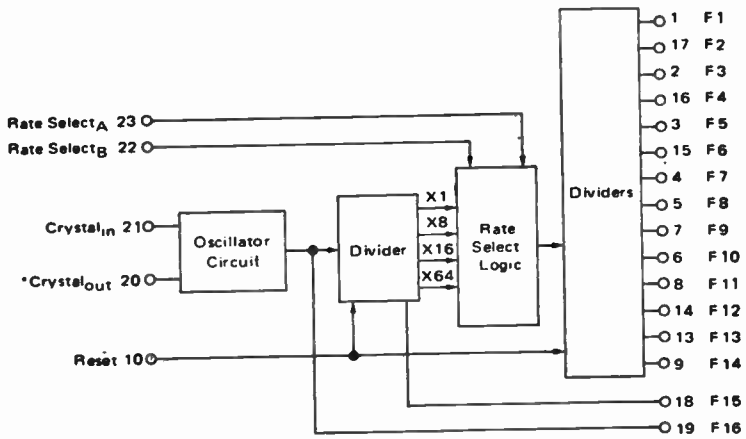
14411 BIT RATE GENERATOR

The 14411 bit rate generator is constructed with complementary MOS (CMOS) enhancement mode devices. It utilizes a frequency divider network to provide a wide range of output frequencies.

A crystal-controlled oscillator is the clock source for the network. A two-bit address is provided to select one of four multiple output clock rates.

Applications include a selectable frequency source for equipment in the data communications market, such as Teletypes, printers, CRT terminals and microprocessor systems. It features:

- Single 5.0 V_{DC} (±5%) power supply
- Internal oscillator crystal-controlled for stability (1.8432 MHz)
- Sixteen different output clock rates
- 50 percent output duty cycle
- Programmable time bases for one of four multiple output rates
- Buffered outputs compatible with low-power TTL
- Noise immunity = 45% of V_{DD} typical
- Diode protection on all inputs



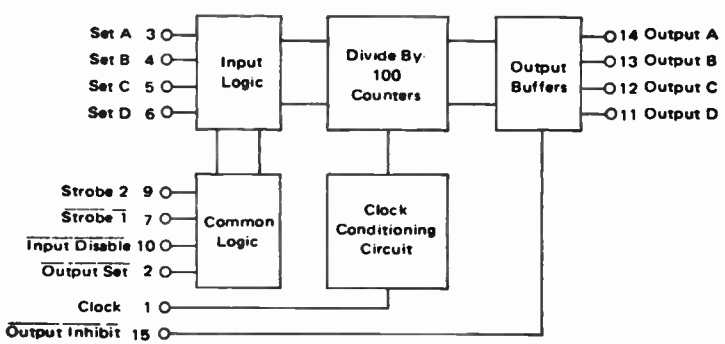
14411

14415 TIMER/DRIVER

The 14415 quad timer/driver is constructed with complementary MOS (CMOS) enhancement mode devices. The output pulse width of each digital timer is a function of the input clock frequency. Once the proper input sequence is detected, the output buffer is set (turned on), and after 100 clock pulses are counted, the output buffer is reset (turned off).

The 14415 was designed specifically for application in high-speed line printers to provide the critical timing of the hammer drivers, but may be used in many applications requiring precision pulse widths. It features:

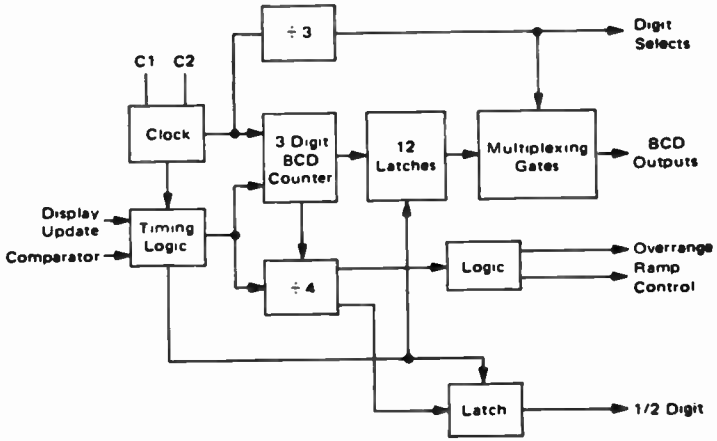
- Four precision digital time delays
- Schmitt trigger clock conditioning
- NPN bipolar output drivers
- Timing disable capability using inhibit output
- Positive or negative edge strobing on the inputs
- Synchronous polynomical counters used for delay counting
- Power-supply operating range
  = 3.0 VDC to 18 VDC (14415EFL)
  = 3.0 VDC to 16 VDC (14415FL/FP)
  = 3.0 VDC to 6.0 VDC (14415EVL/VL/VP)



14415

The 14435 A/D logic is designed specifically for use in a dual-slope integration A/D converter system. The device consists of 3½ digits of BCD counters, 13 memory latches and output multiplexing circuitry. An internal clock oscillator is provided to generate system timing and to set the output multiplexing rate. A single capacitor is required to set the oscillator frequency. It features:

- On-chip clock to control digit select, multiplexing and BCD counters simultaneously
- Multiplexed BCD output
- Built-in 100-count delay for accurate system conversion of low-level inputs
- System overrange output
- Supply Voltage Range
  = 3.0 VDC to 18 VDC (14435EFL)
  = 3.0 VDC to 16 VDC (14435FL/FP)
  = 3.0 VDC to 6.0 VDC (14435EVL/VL/VP)

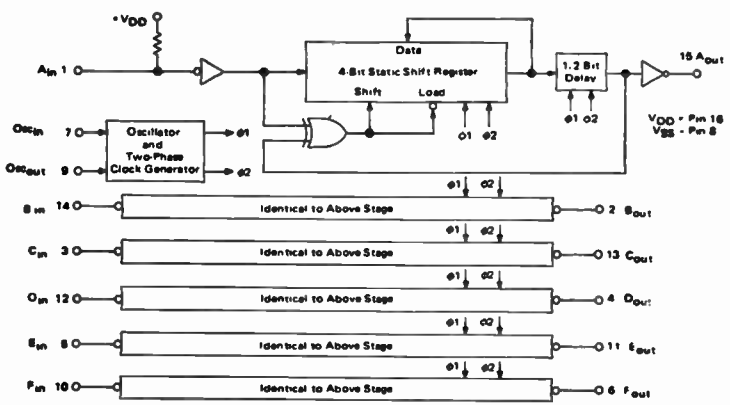


14435

The 14490 is constructed with complementary MOS (CMOS) enhancement mode devices, and is used for the elimination of extraneous level changes that result when interfacing with mechanical contacts. The digital contact bounce eliminator circuit takes an input signal from a bouncing contact and generates a clean digital signal four clock periods after the input has stabilized. The bounce eliminator circuit will remove bounce on both the make and the break of a contact closure.

The clock for operation of the 14490 is derived from an internal R-C oscillator which requires only an external capacitor to adjust for the desired operating frequency (bounce delay). The clock may also be driven from an external clock source or the oscillator of another 14490. It features:

- Noise Immunity = 45% of V_{DD} Typical
- Supply Voltage Range
  = 3.0 V_{DC} to 18 V_{DC} (14490EFL)
  = 3.0 V_{DC} to 16 V_{DC} (14490FL/FP)
  = 3.0 V_{DC} to 6.0 V_{DC} (14490EVL/VL/VP)



14490

Section Three

Linears

For linear ICs, pinouts, a schematic or block diagram, a description, list of features, particular specifications and absolute maximum ratings are included. Frequency response and phase compensation methods accompany various circuits that can be built using these common linear, or analog, integrated circuits.

To aid you in learning about the various ICs, a mini-glossary precedes our description of the most popular linear ICs. Note that term definitions are given for three types of devices: operational amplifiers, voltage comparators and voltage regulators.

Linears Chip Listing

CA3000-Series Linears

LM000-Series Linears

input bias current: The average of the two input currents.

input offset current: The absolute value of the difference between the two input currents for which the output will be driven higher than or lower than specified voltages.

input offset voltage: The absolute value of the voltage between the input terminals required to make the output voltage greater than or less than specified voltages.

input voltage range: The range of voltage on the input terminals (common-mode) over which the offset specifications apply.

logic threshold voltage: The voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

negative output level: The negative DC output voltage with the comparator saturated by a differential input equal to or greater than a specified voltage.

output leakage current: The current into the output terminal with the output voltage within a given range and the input drive equal to or greater than a given value.

output resistance: The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

output sink current: The maximum negative current that can be delivered by the comparator.

positive output level: The high output voltage level with a given load and the input drive equal to or greater than a specified value.

power consumption: The power required to operate the comparator with no output load. The power will vary with signal level, but is specified as a maximum for the entire range of input signal conditions.

response time: The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

saturation voltage: The low-output voltage level with the input drive equal to or greater than a specified value.

strobe current: The current out of the strobe terminal when it is at the zero logic level.

strobed output level: The DC output voltage, independent of input conditions, with the voltage on the strobe terminal equal to or less than the specified low state.

strobe ON voltage: The maximum voltage on either strobe terminal required to force the output to the specified high state independent of the input voltage.

strobe OFF voltage: The minimum voltage on the strobe terminal that will guarantee that it does not interfere with the operation of the comparator.

strobe release time: The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from zero to the one logic level.

supply current: The current required from the positive or negative supply to operate the comparator with no output load. The power will vary with input voltage, but is specified as a maximum for the entire range of input voltage conditions.

voltage gain: The ratio of the change in output voltage to the change in voltage between the input terminals producing it.

VOLTAGE COMPARATOR

bandwidth: That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

common-mode rejection ratio: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

harmonic distortion: The percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental. % harmonic distortion =

$$\frac{(V2^2 + V3^2 + V4^2 + \ldots)^{1/2}\ (100\%)}{V1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, . . . are the rms amplitudes of the individual harmonics.

input bias current: The average of the two input currents.

input common-mode voltage range: The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

input impedance: The ratio of input voltage to input current under the stated conditions for source resistance (Rs) and load resistance (R_L).

input offset current: The difference in the currents into the two input terminals when the output is at zero.

input offset voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

input voltage range: The range of voltages on the input terminals for which the amplifier operates within specifications.

large-signal voltage gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

output impedance: The ratio of output voltage to output current under the stated conditions for source resistance (Rs) and load resistance (R_L).

output resistance: The small signal resistance seen at the output with the output voltage near zero.

output voltage swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

offset voltage temperature drift: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

power supply rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

setting time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

slew rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

supply current: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

transient response: The closed-loop step-function response of the amplifier under small-signal conditions.

unity-gain bandwidth: The frequency range from DC to the frequency where the amplifier open loop gain rolls off to one.

voltage gain: The ratio of output voltage to input voltage under the stated conditions for source resistance (Rs) and load resistance (R_L).

VOLTAGE REGULATORS

current-limit sense voltage: The voltage across the current limit terminals required to cause the regulator to current-limit with a short circuited output. This voltage is used to determine the value of the external current-limit resistor when external booster transistors are used.

dropout voltage: The input-output voltage differential at which the circuit ceases to regulate against further reductions in input voltage.

feedback sense voltage: The voltage, referred to ground, on the feedback terminal of the regulator while it is operating in regulation.

input voltage range: The range of DC input voltages over which the regulator will operate within specifications.

line regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

load regulation: The change in output voltage for a change in load current at constant chip temperature.

long-term stability: Output voltage stability under accelerated life-test conditions at 125°C with maximum rated voltages and power dissipation for 1000 hours.

maximum power dissipation: The maximum total device dissipation for which the regulator will operate within specifications.

output-input voltage differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate within specifications.

output noise voltage: The RMS AC voltage at the output with constant load and no input ripple, measured over a specified frequency range.

output voltage range: The range of regulated output voltages over which the specifications apply.

output voltage scale factor: The output voltage obtained for a unit value of resistance between the adjustment terminal and ground.

quiescent current: That part of input current to the regulator that is not delivered to the load.

ripple rejection: The line regulation for AC input input signals at or above a given frequency with a specified value of bypass capacitor on the reference bypass terminal.

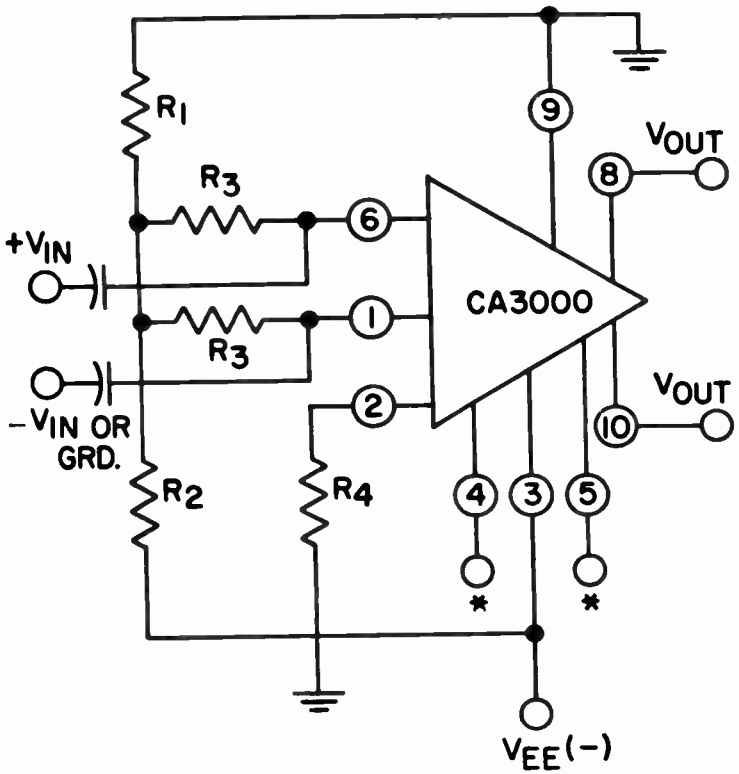
standby current drain: That part of the operating current of the regulator which does not contribute to the load current.

temperature stability: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

CA3000—DC AMPLIFIER

The CA3000 is a general-purpose amplifier used in Schmitt trigger, RC-coupled feedback amplifier, mixer, comparator, crystal oscillator, sense amplifier, and modulator applications. It comes in a 10-lead TO-5 package.

Max. Positive DC Supply Voltage	+ 10V
Max. Negative DC Supply Voltage	− 10V
Max. Input Signal Voltage:	
Single-ended	± 2V
Common mode	± 2V
Max. Total Device Dissipation	300mW
Typ. Input Offset Voltage	1.4mV
Typ. Input-Offset Current	1.2μA
Typ. Input Bias Current	23μA

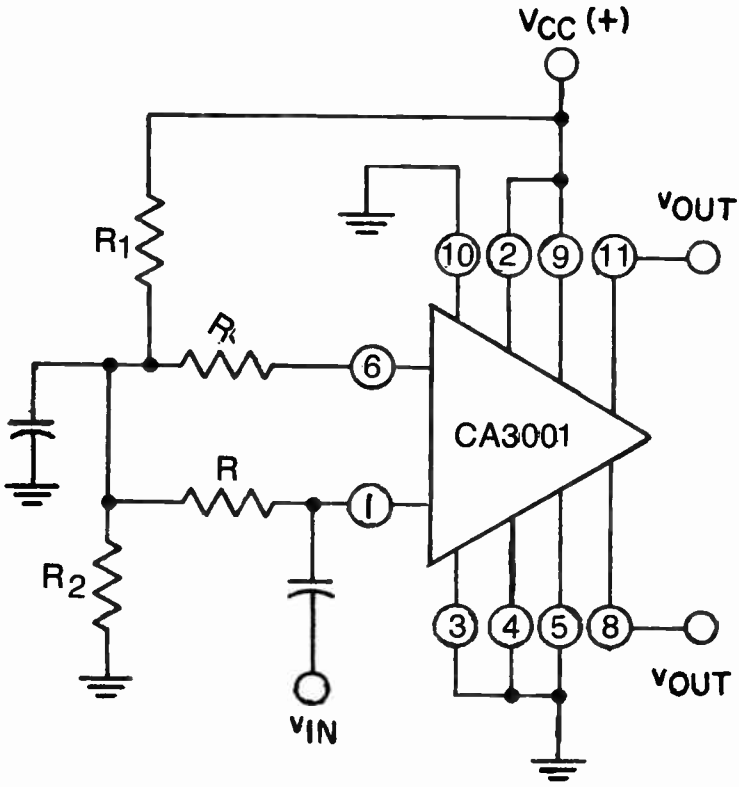


CA3000

CA3001—VIDEO AND WIDE-BAND AMPLIFIER

The CA3001 is a general-purpose amplifier used in DC, i-f, and video amplifier, Schmitt trigger, mixer and modulator applications. It comes in a 12-lead TO-5 package.

Max. Positive DC Supply Voltage	**+ 10V**
Max. Negative DC Supply Voltage	**− 10V**
Max. Input Signal Voltage	
Single-ended	**± 2.5V**
Common-mode	**± 2.5V**
Max. Total Device Dissipation	**300mW**
Typ. Input Offset Voltage	**1.5mV**
Typ. Input Offset Current	**3.4μA**
Typ. Input Bias Current	**10μA**
Typ. Output Offset Voltage	**52mV**

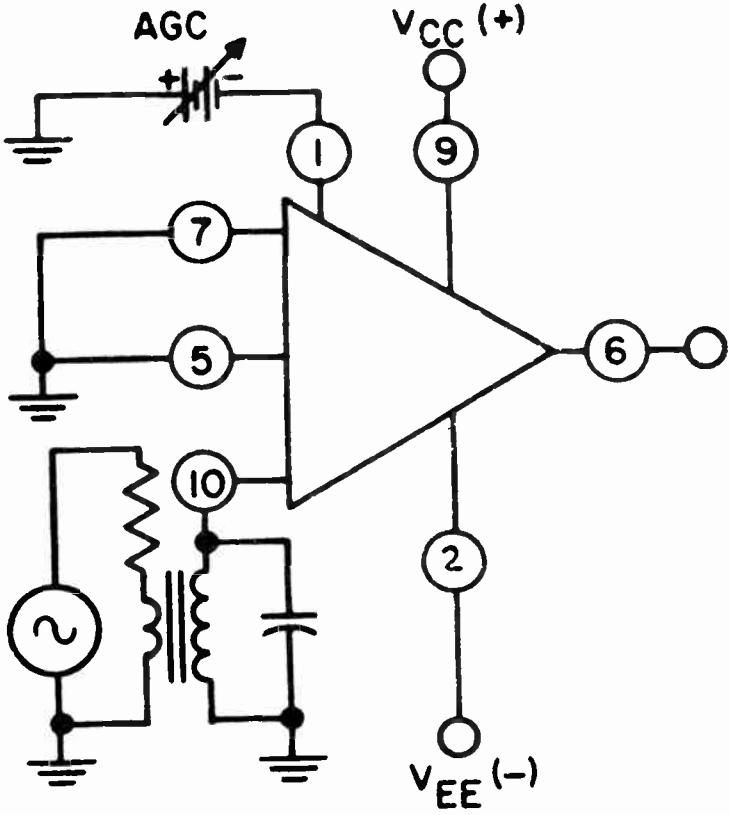


CA3001

CA3002—I-F AMPLIFIER

The CA3002 is a general-purpose amplifier used in video amplifier, product and AM detector applications. It comes in a 10-lead TO-5 package.

Max. Positive DC Supply Voltage	**+ 10V**
Max. Negative DC Supply Voltage	**− 10V**
Max. Input Signal Voltage (single-ended)	**± 3.5V**
Max. Total Device Dissipation	**300mW**
Typ. Input Unbalance Voltage	**2.2mV**
Typ. Input Unbalance Current	**2.2μA**
Typ. Input Bias Current	**20μA**

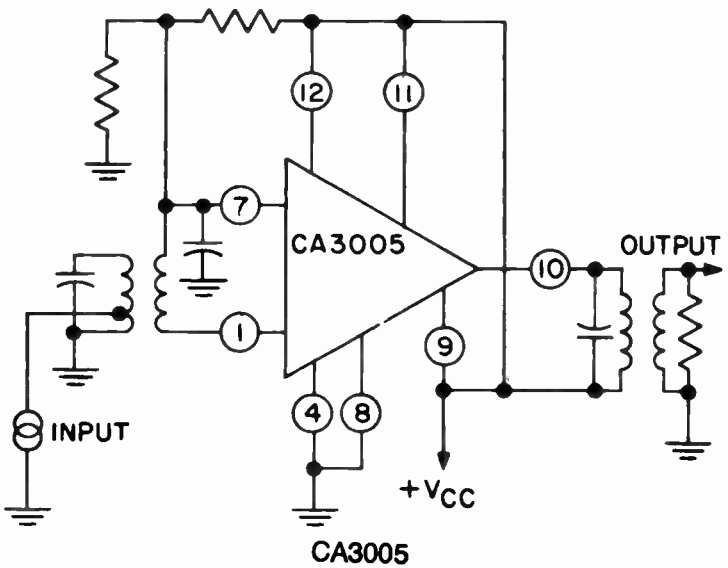


CA3002

CA3005—RF AMPLIFIER

The CA3005 is a general-purpose amplifier used in push-pull input and output, wide-band and narrow-band amplifier, agc, detector, mixer, limiter, modulator and cascode amplifier applications. It comes in a 12-lead TO-5 package.

Max. Positive DC Supply Voltage	**V_{CC} + 12V**
Max. Negative DC Supply Voltage	**V_{EE} – 12V**
Max. Input Signal Voltage:	
Single-ended	**± 3.5V**
Common mode	**+ 3.5 to – 2.5V**
Max. Total Device Dissipation	**300mW**
Typ. Input Offset Voltage	**2.6mV**
Typ. Input Offset Current	**1.4μA**
Typ. Input Bias Current	**19μA**
Typ. Power Gain (f= 100 MHz):	
Cascode Circuit	**20dB**
Differential Amplifier Circuit	**16dB**
Noise Figure (f = 100 MHz):	
Cascode Circuit	**27.80dB**
Differential Amplifier Circuit	**7.8dB**
Common-Mode Rejection Ratio (f=1 kHz)	**101dB**
Useful Frequency Range	**DC to 120 MHz**



CA3005

CA3007—AF AMPLIFIER

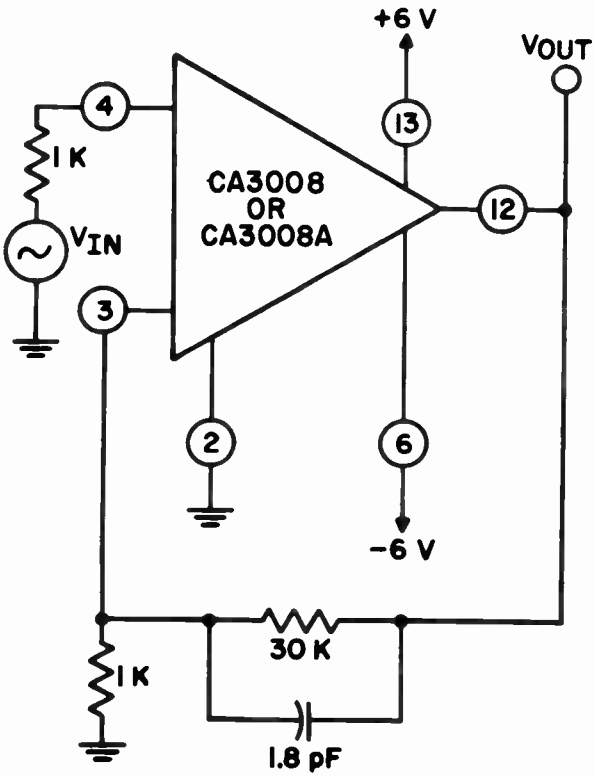
The CA3007 is a special-purpose audio amplifier used in audio driver applications, sound systems and communications equipment. It comes in a 12-lead TO-5 package.

Max. Positive DC Supply Voltage	**+ 10V**
Max. Negative DC Supply Voltage	**− 10V**
Max. Input Signal Voltage:	
Single-ended	**± 2.5V**
Common mode	**± 2.5V**
Max. Total Device Dissipation	**300mW**
Typ. Input Unbalance Voltage	**0.57mV**
Typ. Input Unbalance Current	**0.57μA**
Typ. Input Bias Current	**11μA**

CA3008—OPERATIONAL AMPLIFIER

The CA3008 is a general-purpose amplifier used in narrow-band and band-pass amplifier, feedback amplifier, DC and video amplifier, multivibrator, oscillator, comparator and servo driver applications. It comes in a 14-lead ceramic-and-metal flat package.

Max. Positive DC Supply Voltage	**+10V**
Max. Negative DC Supply Voltage	**−10V**
Max. Input Signal Voltage (single-ended)	**+, −4V**
Max. Total Device Dissipation	**300mW**
Typ. Input Offset Voltage	**1.08mV**
Typ. Input Offset Current	**0.54μA**
Typ. Input Bias Current	**5.3μA**

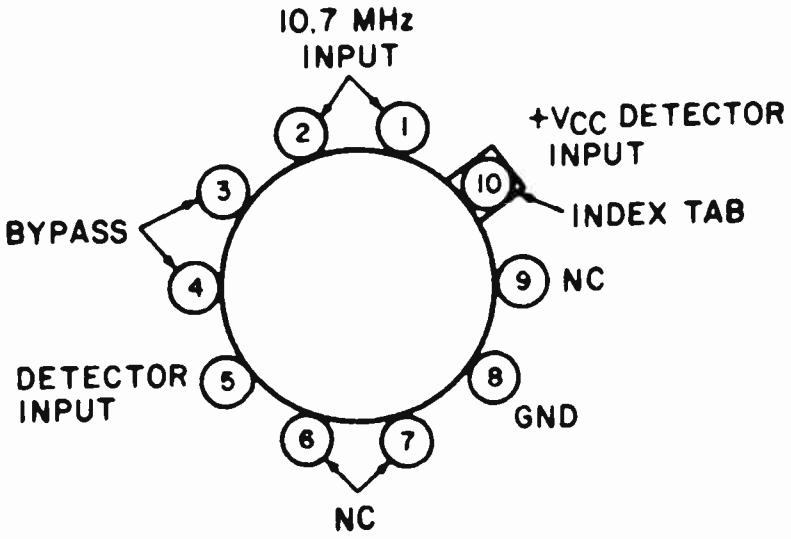


CA3008

CA3011—FM I-F AMPLIFIER

The CA3011 is a special-purpose amplifier used in i-f amplifiers for FM broadcast and TV sound applications. It comes in a 10-lead TO-5 package.

Max. Positive DC Supply Voltage	+ 10V
Max. Recommended Minimum DC Supply Voltage (VCC)	5.5V
Max. Input Signal Voltage (single-ended)	± 3V
Max. Total Device Dissipation	300mW
Typ. Device Dissipation	120mW
Typ. Voltage Gain:	
f= 1 MHz	70dB
f= 4.5MHz	67dB
f= 10.7 MHz	61dB
Typ. Noise Figure (f= 4.5 MHz)	8.7dB
Typ. Useful Frequency Range	100 kHz to > 20 MHz

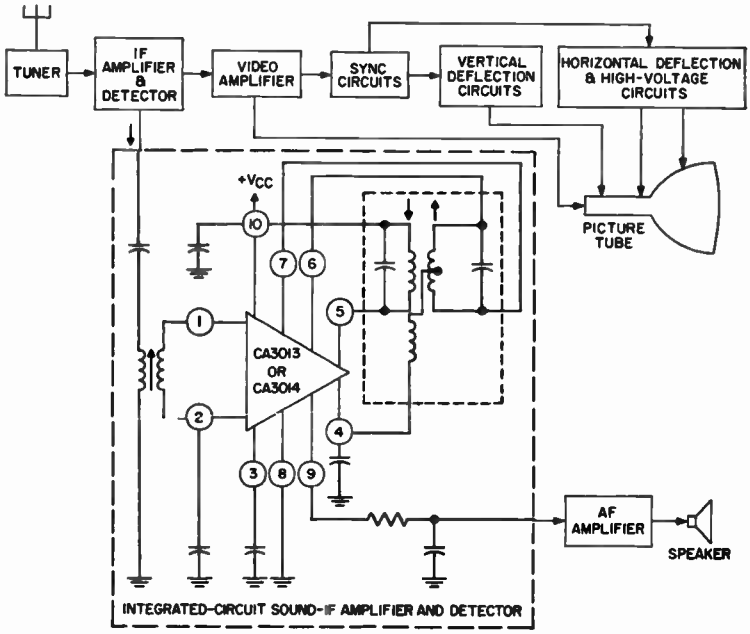


CA3011

CA3013—FM I-F AMPLIFIER/DISCRIMINATOR/AF AMPLIFIER

The CA3013 is a special-purpose amplifier used in IF amplifier, AM and noise limiter, FM detector and AF preamplifier applications. It comes in a 10-lead TO-5 package.

Max. Positive DC Supply Voltage	**+ 10V**
Max. Recommended Minimum DC Supply Voltage (Vcc)	**5.5V**
Max. Input Signal Voltage (Between terminals 1 and 2)	**± 3V**
Max. Total Device Dissipation	**300mW**
Typ. Device Dissipation	**120mW**
Typ. Voltage Gain:	
f= 1MHz	**70dB**
f = 4.5 MHz	**67dB**
f= 10.7 MHz	**60dB**
Typ. Noise Figure (f= 4.5 MHz)	**8.7dB**
Typ. Useful Frequency Range	**100 kHz to > 20 MHz**

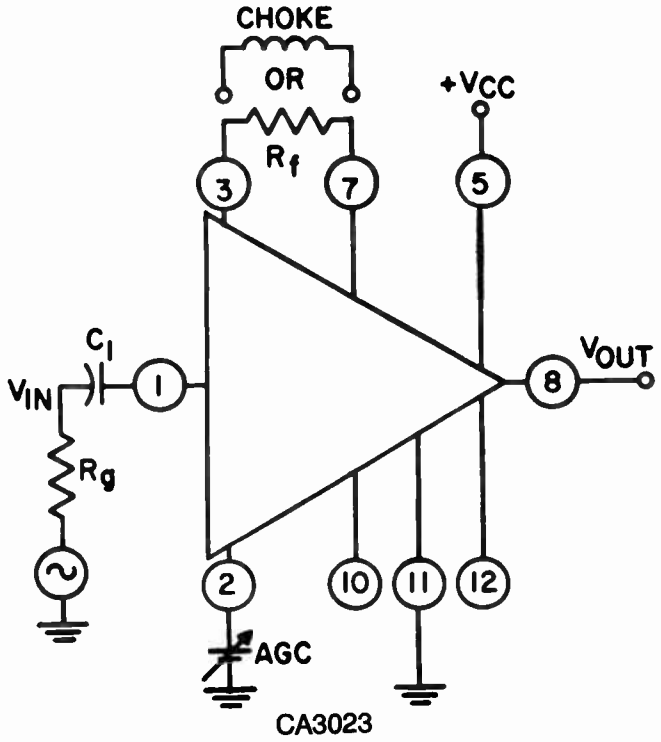


CA3013

CA3023—VIDEO AND WIDE-BAND AMPLIFIER

The CA3023 is a general-purpose amplifier used in gain-controlled linear amplifier, AM/FM i-f amplifier, video amplifier and limiter applications. It comes in a 12-lead TO-5 package.

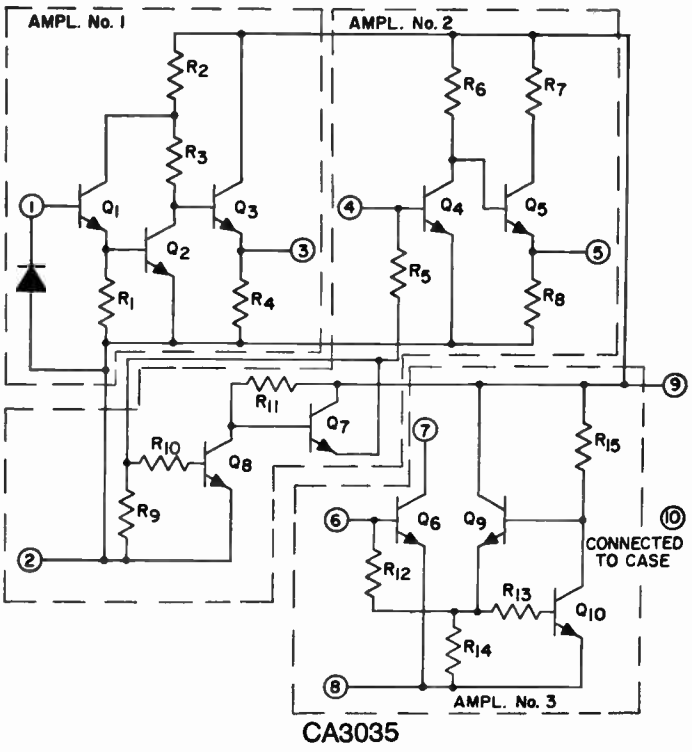
Typ. Device Dissipation	35mW
Typ. Quiescent Output Voltage	1.3V
Typ. AGC Source Current (V_{agc} = 6V)	0.8mA
Typ. Voltage Gain (f = 5 MHz)	53dB
– 3dB Bandwidth	16MHz
Typ. Input Resistance (f = 10 MHz)	300Ω
Typ. Input Capacitance (f= 10 MHz)	13pF
Typ. Output Resistance (f = 10 MHz)	100Ω
Typ. Noise Figure (f= 1 MHz)	6.5dB
Typ. AGC Range (f= 10 MHz)	33dB
Typ. Useful Frequency Range	DC to 40MHz
Typ. Maximum Output Voltage (f= 10 MHz)	0.5Vrms



CA3035—ULTRA-HIGH-GAIN WIDE-BAND AMPLIFIER ARRAY

The CA3035 is a general-purpose amplifier with three individual amplifiers used in remote control amplifier applications, such as TV receivers. It comes in a 10-lead TO-5 package.

Max. Input Signal Voltage (single-ended)	**1Vp-p**
Max. Supply Voltage	**15V**
Max. Total Device Dissipation	**300mW**
Typ. Quiescent Operating Voltage	**2V**
Typ. Quiescent Operating Voltage	**1.9V**
Typ. Quiescent Operating Voltage	**4.9V**
Typ. Total Current Drain (R_{L3} = 5kΩ)	**5mA**
Typ. Voltage Gain (f = 40 kHz):	
Amplifier 1, 2, 3	**44dB**
Cascade	**132dB**
Typ. Noise Figure (Amplifier 1)	**6dB**
Typ. Sensitivity	**100μV**

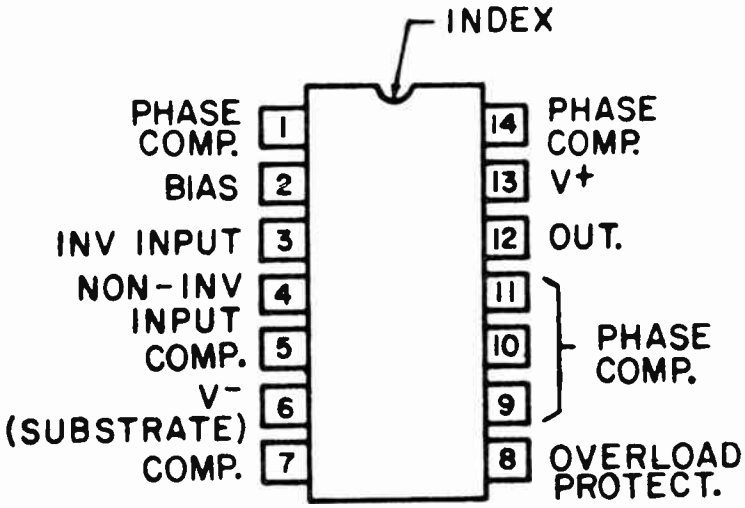


CA3035

CA3037A—OPERATIONAL AMPLIFIER

The CA3037A is a general-purpose amplifier used in narrow-band and band-pass amplifier, feedback amplifier, DC and video amplifier, multivibrator, oscillator, comparator and servo driver applications. It comes in a 14-lead TO-116 dual-in-line ceramic package.

Typ. Input Offset Voltage	**0.9mV**
Typ. Input Offset Current	**0.3μA**
Typ. Input Bias Current	**2.5μA**
Typ. Input Impedance	**20KΩ**
Typ. Output Impedance	**160Ω**
Typ. Noise Figure	**8.3dB**



CA3037A

LM117/LM217/LM317 3-TERMINAL ADJUSTABLE REGULATOR

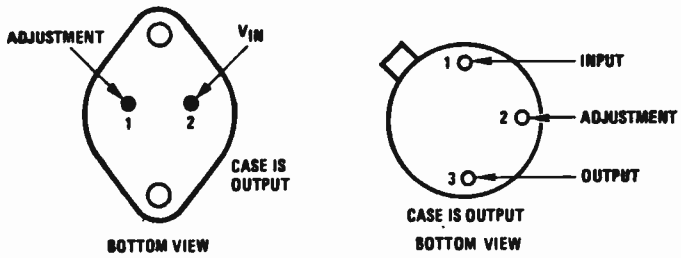
The LM117/LM217/LM317 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5A over a 1.2 V to 37V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM117 is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM117 series offers full overload protection available only in ICs. Included on the chip are current-limit, thermal-overload protection and safe-area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected. Features include:

- Adjustable output down to 1.2V
- Guaranteed 1.5A output current
- Line regulation typically 0.01 percent/V
- Load regulation typically 0.1 percent
- Current limit constant with temperature
- 100 percent electrical burn-in
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection

Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios that are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM117 is useful in a wide variety of other applications. Because the regulator is floating and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as

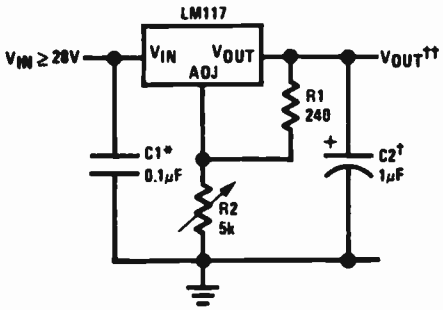


LM117

long as the maximum input to output differential is not exceeded.

Also, the LM117 makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground, which programs the output to 1.2V where most loads draw little current.

1.2V–25V Adjustable Regulator



†Optional—improves transient response

*Needed if device is far from filter capacitors

$$\dagger\dagger V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right)$$

LM117

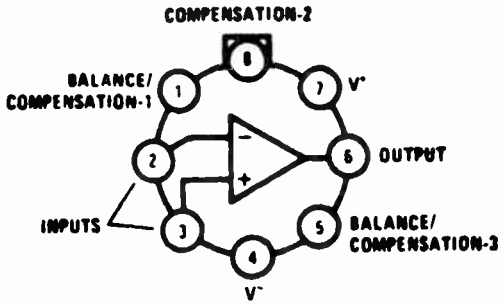
LM118/LM218/LM318 OPERATIONAL AMPLIFIER

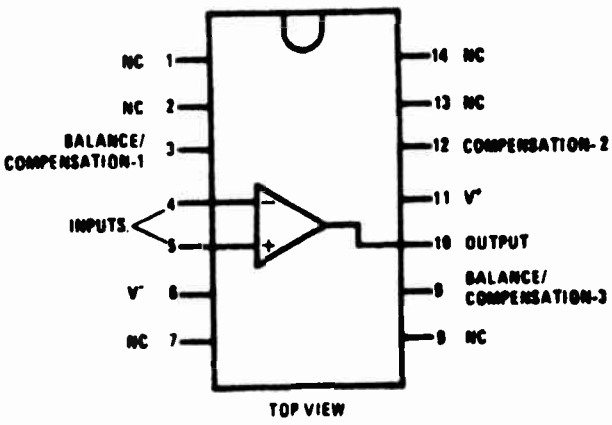
The LM118 series are precision high-speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor of 10 increase in speed over general-purpose devices, without sacrificing DC performance. They feature:

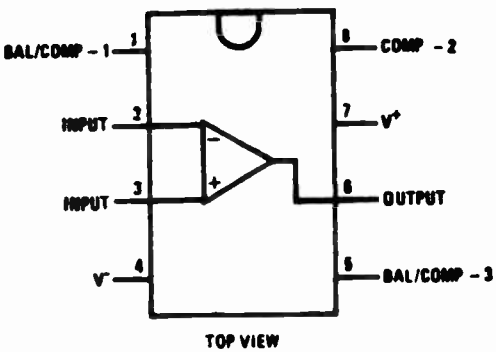
- 15-MHz small signal bandwidth
- Guaranteed 50V/μs slew rate
- Maximum bias current of 250 nA
- Operates from supplies of $\pm$5V to $\pm$20V
- Internal frequency compensation
- Input and output overload protected
- Pin compatible with general-purpose operational amps

The LM118 series has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications feedforward compensation will boost the slew rate to over 150V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1 percent setting time to under 1 μs.

The high speed and fast setting time of these op amps make them useful in A-D converters, oscillators, active filters, sample and hold circuits, or general-purpose amplifiers. These devices are easy to apply and offer better AC performance than industry standards such as the LM709. The LM218 is identical to the LM118, except that the LM218 has its performance specified over a -25°C to +85°C temperature range. The LM318 is specified from 0°C to +70°C.


COMPENSATION-2
BALANCE/
COMPENSATION-1
V+
OUTPUT
INPUTS
BALANCE/
COMPENSATION-3
V-
TOP VIEW


NC 1
NC 2
BALANCE/
COMPENSATION-1 3
INPUTS 4
5
V- 6
NC 7
14 NC
13 NC
12 COMPENSATION-2
11 V+
10 OUTPUT
9 BALANCE/
COMPENSATION-3
8 NC
TOP VIEW


BAL/COMP - 1 1
INPUT 2
INPUT 3
V- 4
8 COMP - 2
7 V+
6 OUTPUT
5 BAL/COMP - 3
TOP VIEW

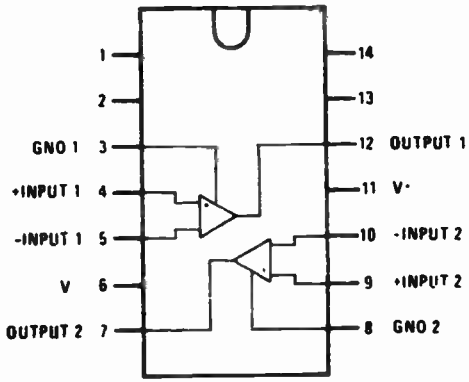
LM118

LM119/LM219/LM319 HIGH-SPEED DUAL COMPARATOR

The LM119 series are precision high-speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the LM710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25 mA. Outstanding features include:

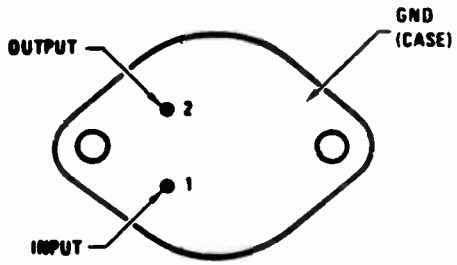
- Two independent comparators
- Operates from a single 5V supply
- Typically 80 ns response time at ±15V
- Minimum fan-out of 2 each side
- Maximum input current of 1 μA over temperature
- Inputs and outputs can be isolated from system ground
- High common mode slew rate

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the LM711. The LM119 is specified from −55°C to +125°C, the LM219 is specified from −25°C to +85°C, and the LM319 is specified from 0°C to +70°C.



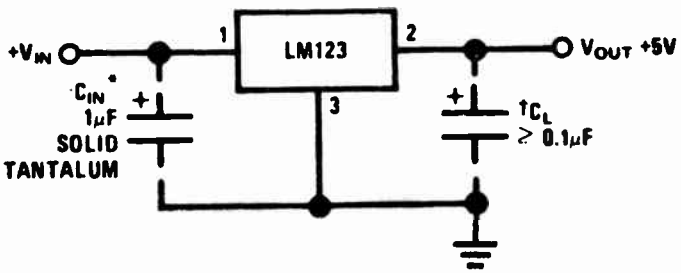
TOP VIEW

LM119



BOTTOM VIEW

Basic 3 Amp Regulator



*Required if LM123 is more than 4" from filter capacitor.

†Regulator is stable with no load capacitor into resistive loads.

LM119

LM120/LM220/LM320 3-TERMINAL NEGATIVE REGULATOR

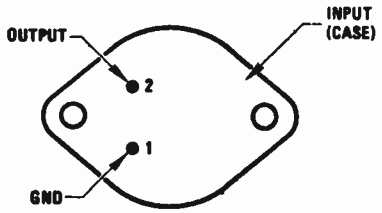
The LM120 series are 3-terminal negative regulators with a fixed output voltage of — 5V, — 5.2V, — 6V, — 8V, — 9V, — 12V, — 15V, — 18V, and — 24V and up to 1.5A load current capability (LM320-5, LM320-5.2, LM320-6, etc.).

These devices need only one external component: a compensation capacitor at the output, making them easy to apply. Worst case guarantees on output voltage deviation due to any combination of line, load or temperature variation assure satisfactory system operation.

Exceptional effort has been made to make the LM120 series immune to overload conditions. The regulators have current limiting which is independent of temperature, combined with thermal-overload protection. Internal current limiting protects against momentary faults while thermal shutdown prevents junction temperatures from exceeding safe limits during prolonged overloads.

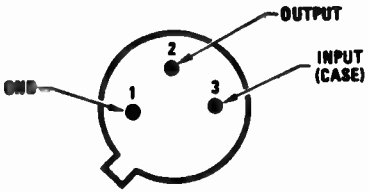
Although primarily intended for fixed output voltage applications, the LM120 series may be programmed for higher output voltages with a simple resistive divider. The low quiescent drain current of the devices allows this technique to be used with good regulation. They feature:

- Preset output voltage error less than ±3 percent
- Preset current limit
- Internal thermal shutdown
- Operates with input-output voltage differential down to 1V
- Excellent ripple rejection
- Low temperature drift
- Easily adjustable to higher output voltage



BOTTOM VIEW

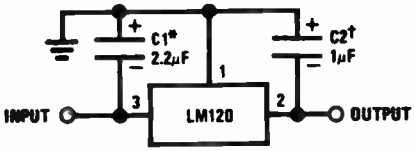
LM120



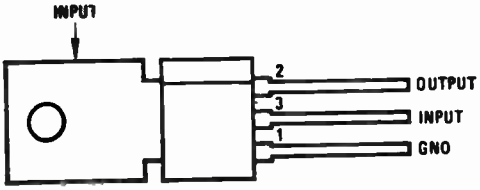
BOTTOM VIEW

LM120

Fixed Regulator

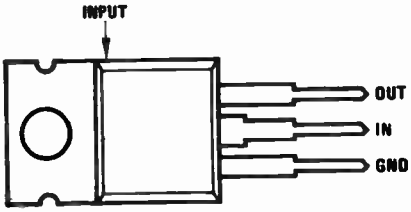


LM120



FRONT VIEW

LM320



TOP VIEW

LM320

The LM122 series are precision timers that offer great versatility with high accuracy. They operate with unregulated supplies from 4.5V to 40V while maintaining constant timing periods from microseconds to hours. Internal logic and regulator circuits complement the basic timing function enabling the LM122 series to operate in many different applications with a minimum of external components.

The output of the timer is a floating transistor with built in current limiting. It can drive either ground referred or supply referred loads up to 40V and 50 mA. The floating nature of this output makes it ideal for interfacing, lamp or relay driving, and signal conditioning where an open collector or emitter is required. A logic reverse circuit can be programmed by the user to make the output transistor either on or off during the timing period.

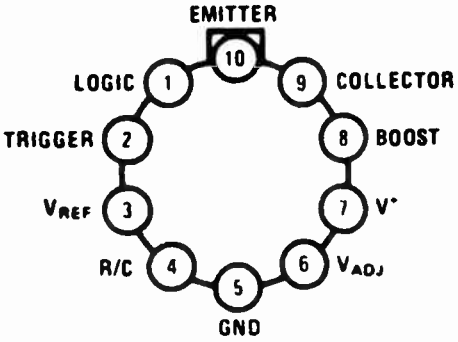
The trigger input to the LM122 series has a threshold of 1.6V independent of supply voltage, but it is fully protected against inputs as high as ±40V, even when using a 5V supply. The circuitry reacts only to the rising edge of the trigger signal, and is immune to any trigger voltage during the timing periods.

An internal 3.15V regulator is included in the timer to reject supply voltage changes and to provide the user with a convenient reference for applications other than a basic timer. External loads up to 5 mA can be driven by the regulator. An internal 2V divider between the reference and ground sets the timing period to 1 RC. The timing period can be voltage controlled by driving this divider with an external source through the V_{ADJ} pin. Timing ratios of 50:1 can be easily achieved.

The comparator used in the LM122 utilizes high-gain PNP input transistors to achieve 300-pA typical input bias current over a common mode range of 0V to 3V. A boost terminal allows the user to increase comparator operating current for timing periods less than 1 ms. This lets the timer operate over a 3μs to multihour timing range with excellent repeatability.

The LM2905/LM3905 are identical to the LM122 series except that the boost and V_{REF} pin options are not available, limiting minimum timing period to 1 ms.

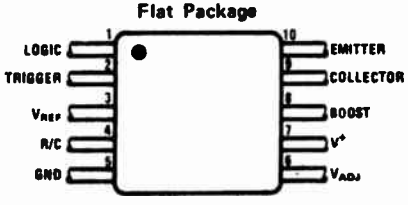
Metal Can Package



TOP VIEW

LM122

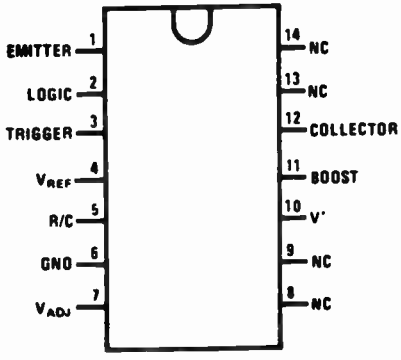
Flat Package



TOP VIEW

LM122F

Dual-In-Line Package



TOP VIEW

LM322N

LM2905/LM3905 PRECISION TIMER

The LM122 series are precision timers that offer great versatility with high accuracy. They operate with unregulated supplies from 4.5V to 40V while maintaining constant timing periods from microseconds to hours. Internal logic and regulator circuits complement the basic timing function enabling the LM122 series to operate in many different applications with a minimum of external components.

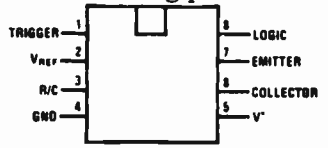
The output of the timer is a floating transistor with built in current limiting. It can drive either ground referred or supply referred loads up to 40V and 50 mA. The floating nature of this output makes it ideal for interfacing, lamp or relay driving, and signal conditioning where an open collector or emitter is required. A logic reverse circuit can be programmed by the user to make the output transistor either on or off during the timing period.

The trigger input to the LM122 series has a threshold of 1.6V independent of supply voltage, but it is fully protected against inputs as high as ±40V, even when using a 5V supply. The circuitry reacts only to the rising edge of the trigger signal, and is immune to any trigger voltage during the timing periods.

An internal 3.15V regulator is included in the timer to reject supply voltage changes and to provide the user with a convenient reference for applications other than a basic timer. External loads up to 5 mA can be driven by the regulator. An internal 2V divider between the reference and ground sets the timing period to 1 RC. The timing period can be voltage controlled by driving this divider with an external source through the V_{ADJ} pin. Timing ratios of 50:1 can be easily achieved.

The comparator used in the LM122 utilizes high-gain PNP input transistors to achieve 300-pA typical input bias current over a common mode range of 0V to 3V. A boost terminal allows the user to increase comparator operating current for timing periods less than 1 ms. This lets the timer operate over a 3μs to multihour timing range with excellent repeatability.

The LM2905/LM3905 are identical to the LM122 series except that the boost and V_{REF} pin options are not available, limiting minimum timing period to 1 ms.



TOP VIEW

LM2905N

LM123/LM223/LM323 3-AMP, 5-VOLT POSITIVE REGULATOR

The LM123 is a 3-terminal positive regulator with a preset 5V output and a load driving capability of 3 amps. New circuit design and processing techniques are used to provide the high output current without sacrificing the regulation characteristics of lower current devices.

The 3A regulator is virtually blowout proof. Current limiting, power limiting, and thermal shutdown provide the same high level of reliability obtained with these techniques in the LM109 1-amp regulator.

No external components are required for operation of the LM123. If the device is more than 4 inches from the filter capacitor, however, a 1μF solid tantalum capacitor should be used on the input. A 0.1μF or larger capacitor may be used on the output to reduce load transient spikes created by fast switching digital logic, or to swamp out stray load capacitance.

An overall worst case specification for the combined effects of input voltage, load currents, ambient temperature and power dissipation ensure that the LM123 will perform satisfactorily as a system element. Features are:

- 3A output current
- Internal current and thermal limiting
- 0.01Ω typical output impedance
- 7.5V minimum input voltage
- 30W power dissipation

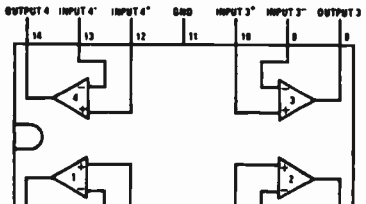
LM124/LM224/LM324, LM124A/LM224A/LM324A, LM2902 LOW-POWER QUAD OPERATIONAL AMPLIFIERS

The LM124 series consists of four independent, high-gain, internally frequency-compensated operational amplifiers that were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

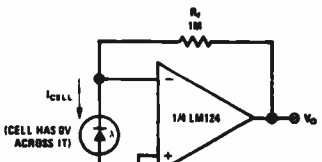
Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5V$_{DC}$ power supply voltage that is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V$_{DC}$ power supplies.

In the linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature compensated. The input bias current is also temperature compensated.

DC Voltage Gain	**100dB**
Bandwidth (Unity Gain)	**1MHz**
Power Supply Range:	
Single Supply	**3V$_{DC}$ to 30V$_{DC}$**
or Dual Supplies	**± 1.5 V$_{DC}$ to ± 15V$_{DC}$**
Supply Current Drain	**800 μA—Essentially independent of supply voltage (1 mW/op amp at + 5V$_{DC}$)**
Input Biasing Current	**45 nA$_{DC}$**
Input Offset Voltage	**2 mV$_{DC}$**
Offset Current	**5 nA$_{DC}$**
Output Voltage Swing	**0V$_{DC}$ to V^+ —1.5 V$_{DC}$**



LM124



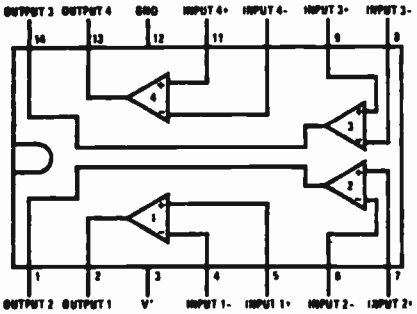
LM124

LM139/LM239/LM339, LM 139A/LM239A/LM339A, LM2901, LM3302 LOW-POWER LOW-OFFSET VOLTAGE QUAD COMPARATORS

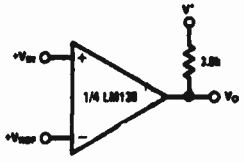
The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV maximum for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators; simple analog to digital converters; pulse, square wave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic, where the low power drain of the LM339 is a distinct advantage over standard comparators.

Supply Voltage Range:	
LM139 series	**2VDC to 36 VDC or**
LM139A series, LM2901	**± 1VDC to ± 18VDC**
LM3302	**2VDC to 28VDC or± 1VDC to ± 14VDC**
Supply Current Drain	**(0.8 mA)**
Input Biasing Current	**25 nA**
Input Offset Current	**± 5 nA**
Offset Voltage	**± 3 mV**
Output Saturation Voltage	**250 mV at 4 mA**



LM139

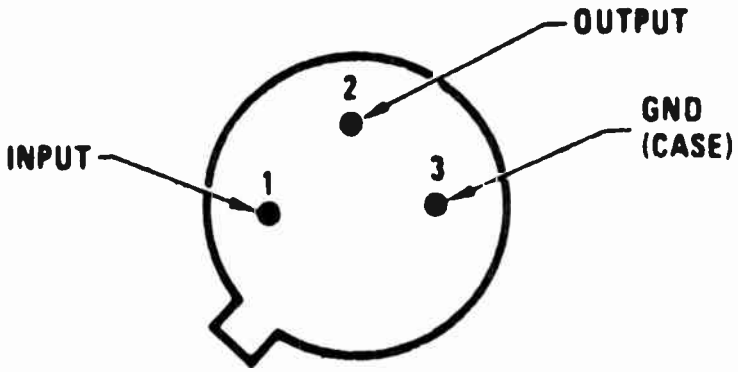


Basic Comparator

LM139

LM140L SERIES 3-TERMINAL POSITIVE REGULATOR

The LM140L series of 3-terminal positive regulators is available with several fixed output voltages, making them useful in a wide range of applications. The LM140LA is an improved version of the LM78LXX series with a tighter output voltage tolerance (specified over the full military temperature range), higher ripple rejection, better regulation and lower quiescent current. The LM140LA regulators have ±2 percent V_{OUT} specification, 0.04 percent/V line regulation, and 0.01 percent/mA load regulation. When used as a zener diode/resistor combination replacement, the LM140LA usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single-point regulation. The voltages available allow the LM140LA to be used in logic systems, instrumentation, stereo and other solid state electronic equipment. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

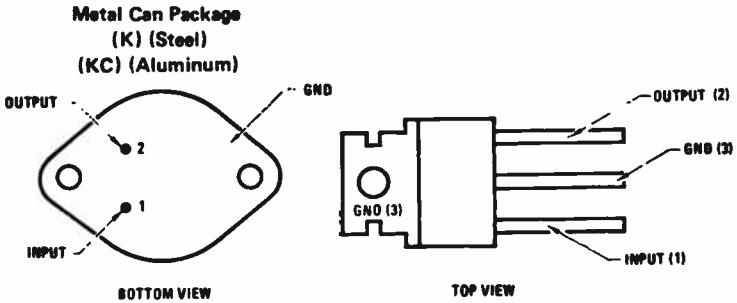


BOTTOM VIEW

LM140

The LM140LA/LM240LA/LM340LA are available in the low profile metal three-lead TO-39 (H) and the LM240LA/LM340LA are also available in the plastic TO-92 (Z). With adequate heat sinking, the regulator can deliver 100 mA output current. Current limiting is included to limit the peak output current to a safe value. Safe-area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided the thermal shutdown circuit takes over, preventing the IC from overheating. Features include:

- Line regulation of 0.04 percent/V
- Load regulation of 0.01 percent/mA
- Output voltage tolerances of ±2 percent at 25°C and ±4 percent over the temperature range
- Output current of 200 mA
- Internal thermal-overload protection
- Output transistor safe area protection
- Internal short-circuit current limit



LM340

LM170/LM270/LM370 AGC/SQUELCH AMPLIFIER

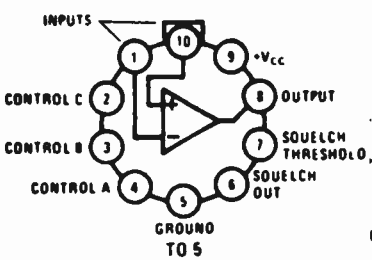
The LM170 is a direct coupled monolithic amplifier whose voltage gain is controlled by an external DC voltage. The device features:

- Large gain control range
- Self-contained agc/squelch system, with fast-attack, slow-release.
- Low distortion
- Minimum DC output shift as gain is varied
- Differential inputs, with large common-mode input range
- Outputs of several amplifiers may be directly summed in multichannel systems.
- Dissipates only 18 mW from +4.5V supply, usable with supply up to +24V.
- Sensitive squelch threshold set by single external resistor.

In addition to communication system squelch and agc applications, the LM170 is useful as constant-amplitude audio oscillator, linear low-frequency modulator, single sideband automatic load control and as a variable DC gain element in analog computation.

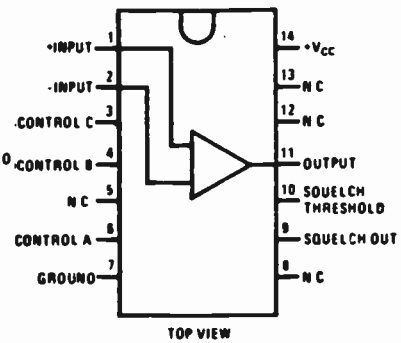
The LM170 is specified for operation over the −55°C to +125°C military temperature range. The LM270 is specified for operation over the −25°C to +75°C temperature range. The LM370 is specified for operation over the 0°C to +70°C temperature range.

Metal Can Package



LM170H

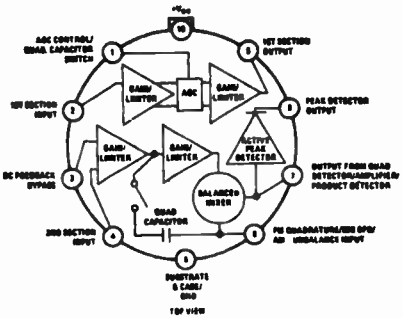
Dual-In-Line Package



LM370N

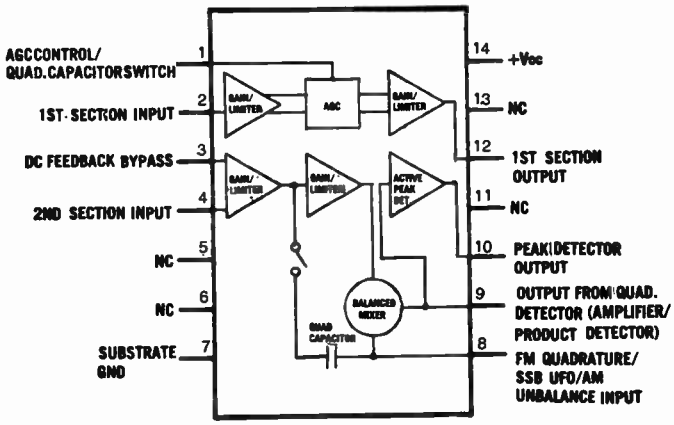
The LM273/LM373 and LM274/LM374 are broad-band communications subsystems, capable of performing the diverse functions required in AM, FM or single sideband receivers and transmitters. In addition, the LM274/LM374 may operate as a high gain automatic gain controlled video amplifier. Band-pass shaping may be performed by a single external filter, connected between amplifier sections, at frequencies from audio up to 30 MHz. The first section of the LM273/LM373 is optimized to drive low impedance loads, such as mechanical or ceramic filters. The LM274/LM374 has a high output impedance, ideal for high-Z crystal, LC or ceramic filters.

Metal Can Package



LM273H

Dual-In-Line Package



LM373N

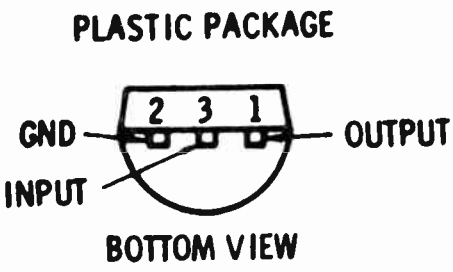
The LM273 and LM274 are specified for operation over the −25°C to +100°C military temperature range. The LM373 and LM374 are specified for operation over the 0°C to +70°C temperature range. Features include:

- AM Operation
  - —High gain; typical sensitivity of 10μV at 455 kHz
  - —Wide bandwidth; 30 MHz capability
  - —Self-contained detector and agc system
  - —Wide agc range; greater than 60 dB for a 10-dB output change at 27 MHz
- FM Operation
  - —Three emitter coupled limiting stages and simple quadrature detector
  - —Detection of ±5 kHz deviation FM at either 455 kHz or 10.7 MHz
  - —Two separated amplifier blocks, allowing filtering in two or more blocks
  - —No DC paths require through external filters or through quadrature network
- SSB operation
  - —Double balanced product detector
  - —Self-contained audio peak agc system
  - —Easy external tailoring of agc characteristic for desired agc figure of merit
- Video amplifier operation
  - —Internal video peak detector for video agc
  - —High-level and low-level video outputs
  - —Gated video agc capability

LM320L SERIES 3-TERMINAL NEGATIVE REGULATOR

The LM320L-XX series of 3-terminal negative voltage regulators features several selected fixed output voltages from —5V to —24V with load current capabilities to 100 mA. Internal protective circuitry includes safe operating area for the output transistor, short circuit current limit, and thermal shutdown. Features include:

- Preset output voltage error less that ±5 percent over temperature
- 100 mA output current capability
- Internal thermal overload protection
- Input-output voltage differential down to 2V
- Internal current limit
- Maximum load regulation -- 0.15 percent/mA
- Maximum line regulation —0.1 percent/V
- Output transistor safe area protection



LM320L

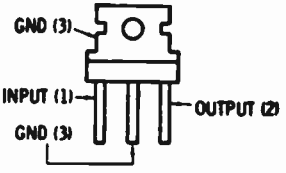
LM340 SERIES VOLTAGE REGULATOR

The LM340-XX series of 3-terminal regulators is available with several fixed output voltages, making them useful in a wide range of applications. One of these is local on-card regulation, eliminating the distribution problems associated with single-point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, stereo and other solid state electronic equipment. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

The LM340-XX series is available in two power packages. Both the plastic TO-220 and metal TO-3 packages allow these regulators to deliver over 1.5A if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe-area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over, preventing the IC from overheating.

Considerable effort was expended to make the LM340-XX series of regulators easy to use, and to minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply. Features include:

- Output current in excess of 1.5A
- Internal thermal-overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit

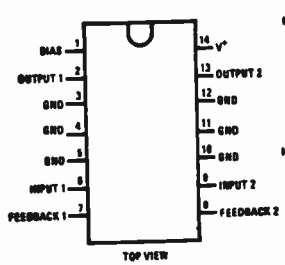


PLASTIC PACKAGE
FRONT VIEW
LM340

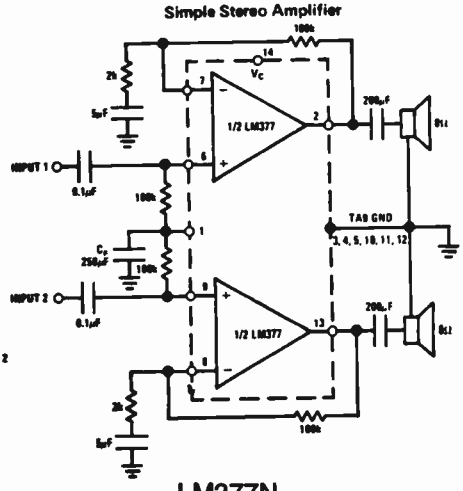
LM377 DUAL 2-WATT AUDIO AMPLIFIER

The LM377 is a monolithic dual power amplifier which offers high quality performance for stereo phonographs, tape players, recorders AM-FM stereo receivers, etc. The LM377 will deliver 2W per channel into 8Ω or 16Ω loads. The amplifier is designed to operate with a minimum of external components and contains an internal bias regulator to bias each amplifier. Device overload protection consists of both internal current limit and thermal shutdown. Features include:

- Avo typical 90 dB
- 2W per channel
- 70-dB ripple rejection
- 75-dB channel separation
- Internal stabilization
- Self-centered biasing
- 3 megohm input impedance
- 10V to 26V operation
- Internal current limiting
- Internal thermal protection



LM377N



LM377N

LM380 AUDIO POWER AMPLIFIER

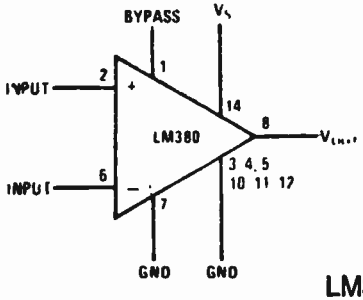
The LM380 is a power audio amplifier for consumer application. In order to hold system cost to a minimum, gain is internally fixed at 34 dB. A unique input stage allows inputs to be ground referenced. The output is automatically self-entering to one-half of the supply voltage.

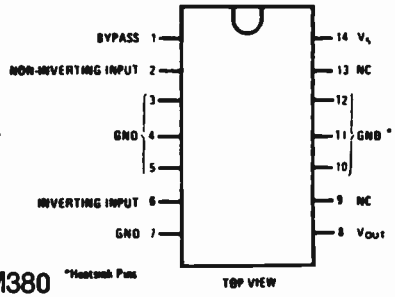
The output is short-circuit proof with internal thermal limiting. The package outline is standard dual-in-line. A copper lead frame is used with the center three pins on either side, comprising a heat sink. This makes the device easy to use in standard p-c layout.

Uses include simple phonograph amplifiers, intercoms, line drivers, teaching machine outputs, alarms, ultrasonic drivers, TV sound systems, AM-FM radio, small servo drivers, power converters, etc.

A selected part for more power on higher supply voltages is available as the LM384. Features include:

- Wide supply voltage range
- Low quiescent power drain
- Voltage gain fixed at 50
- High peak current capability
- Input referenced to GND
- High input impedance
- Low distortion
- Quiescent output voltage is at one-half of the supply voltage
- Standard dual-in-line package





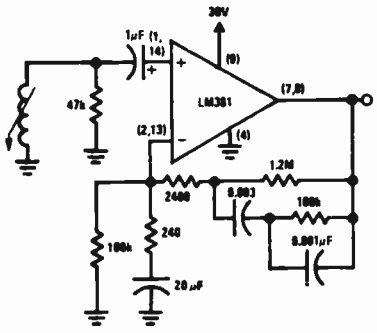
LM380

LM381/LM381A LOW NOISE DUAL PREAMPLIFIER

The LM381/LM381A is a dual preamplifier for the application of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 120-dB supply rejection and 60-dB channel separation. Other outstanding features include high gain (112 dB), large output voltage swing (Vcc – 2V) p-p, and wide power bandwidth (75 kHz, 20Vp–p). The LM381/LM381A operates from a single supply across the wide range of 9V to 40V.

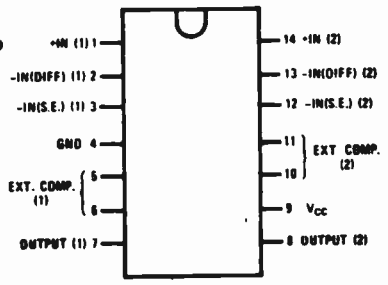
Either differential input or single-ended input configurations may be selected. The amplifier is internally compensated with the provision for additional external compensation for narrow band applications. Features include:

- Low noise—0.5μV total input noise
- High gain—112-dB open loop
- Single supply operation
- Wide supply range—9V to 40V
- Power supply rejection—120 dB
- Large output voltage swing (Vcc to 2V) p-p
- Wide bandwidth—15 MHz unity gain
- Power bandwidth—75 kHz, 20 Vp-p
- Internally compensated
- Short-circuit protected



Typical Magnetic Phono Preamp.

Dual-In-Line Package



TOP VIEW

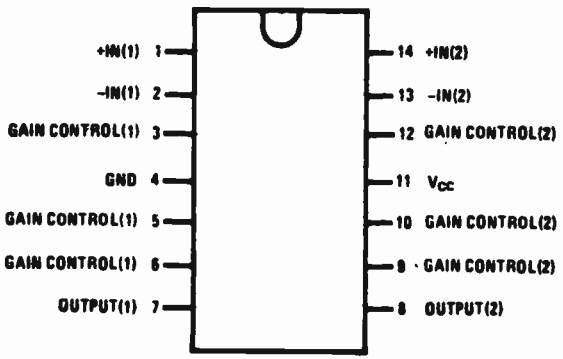
LM381

LM382 LOW NOISE DUAL PREAMPLIFIER

The LM382 is a dual preamplifier for the amplication of low-level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulators, providing 120-dB supply rejection and 60-dB channel separation. Other outstanding features include high gain (100 dB), and wide power bandwidth (75 kHz, 20 Vp-p). The LM382 operates from a single supply across the wide range of 9V to 40V.

A resistor matrix is provided on the chip to allow the user to select a variety of closed loop gain options and frequency response characteristics such as flat-band, NAB or RIAA equalization. The circuit is supplied in the 14-lead dual-in-line package. Features include:

- Low noise—0.8-μV total equivalent input noise
- High gain—100-dB open loop
- Single supply operation
- Wide supply range—9V to 40V
- Power supply rejection—120 dB
- Large output voltage swing
- Wide bandwidth—15 MHz unity gain
- Power bandwidth—75 kHz, 20 Vp-p
- Internally compensated
- Short circuit protected



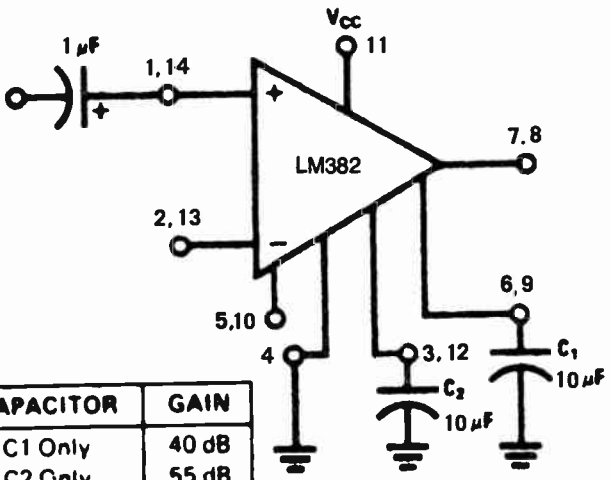
LM382N

LM703L LOW POWER DRAIN RF/I-F AMPLIFIER

The LM703L is a monolithic rf IF amplifier, having an efficient DC biasing system, reducing demands upon power-supply and decoupling elements. Its low internal feedback guarantees a high-stability limited gain.

Applications include limiting and nonlimiting amplifiers, mixers and rf oscillators. The LM703L is specifically characterized for operation in consumer applications such as TV sound i-f, FM-i-f limiter amplifier and chroma reference oscillator for color TV.

Power Consumption	**96 mW (max.)**
Forward Transadmittance	**33 mmhos**
Input Conductance	**0.35 mmhos**
Output Conductance	**0.03 mmhos**
Peak-to-Peak Output Current	**5.0 mA**



CAPACITOR	GAIN
C1 Only	40 dB
C2 Only	55 dB
C1 & C2	80 dB

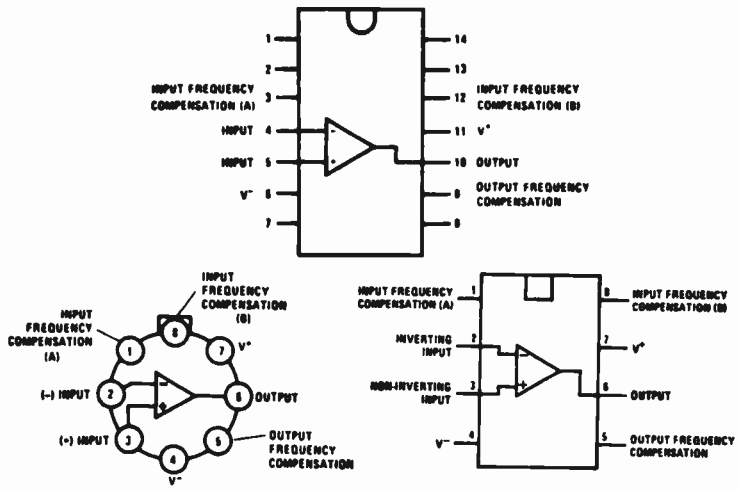
Flat Response—Fixed Gain Configuration
LM703L

The LM709 series is a monolithic operational amplifier intended for general-purpose applications. Operation is completely specified over the range of voltages commonly used for these devices. The design, in addition to providing high gain, minimizes both offset voltage and bias currents. Further, the class B output stage gives a large output capability with minimum power drain.

External components are used to frequency compensate the amplifier. Although the unity-gain compensation network specified will make the amplifier unconditionally stable in all feedback configurations, compensation can be tailored to optimize high-frequency performance for any gain setting.

The fact that the amplifier is built on a single silicon chip provides low offset and temperature drift at minimum cost. It also ensures negligible drift due to temperature gradients in the vicinity of the amplifier.

The LM709C is the industrial version of the LM709;. It is identical to the LM709/LM709A except that it is specified for operation from 0°C to +70°C.



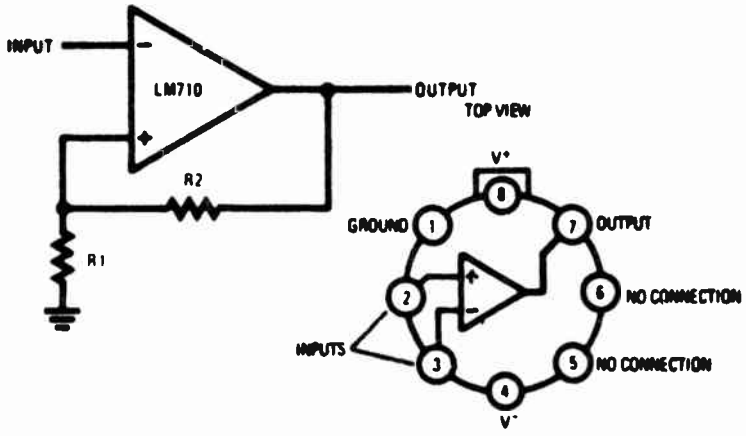
LM709

LM710/LM710C VOLTAGE COMPARATOR

The LM710 series are high-speed voltage comparators intended for use as an accurate, low-level digital level sensors or as replacements for operational amplifiers in comparator applications where speed is of prime importance. The circuit has a differential input and a single-ended output, with saturated output levels compatible with practically all types of integrated logic.

The device is built on a single silicon chip which ensures low offset and thermal drift. The use of a minimum number of stages along with minority-carrier lifetime control (gold doping) makes the circuit much faster than operational amplifiers in saturating comparator applications. In fact, the low stray and wiring capacitances that can be realized with monolithic construction make the device difficult to duplicate with discrete components operating at equivalent power levels.

The LM710 series are useful as pulse height discriminators, voltage comparators in high-speed A-D converters or go-no go detectors in automatic test equipment. They also have applications in digital systems as an adjustable-threshold line receiver or an interface between logic types. In addition, the low cost means it can replace relatively simple discrete component circuitry.



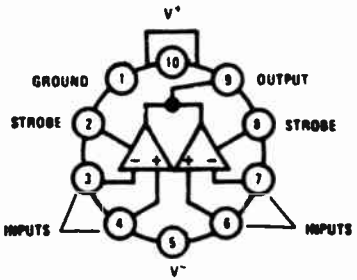
LM710

Note: Pin 4 connected to case.

The LM711 series contains two voltage comparators with separate differential inputs, a common output and provision for strobing each side independently. Similar to the LM710, the device features low offset and thermal drift, a large input voltage range, low power consumption, fast recovery from large overloads and compatibility with most integrated logic circuits.

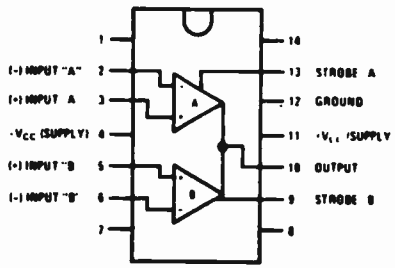
With the addition of an external resistor network, the LM711 series can be used as a sense amplifier for core memories. The input thresholding, combined with the high gain of the comparator, eliminates many of the inaccuracies encountered with conventional sense amplifier designs. Further, it has the speed and accuracy needed for reliably detecting the outputs of cores as small as 20 mils.

The LM711 series are also useful in other applications where a dual comparator with OR'ed outputs is required, such as a double-ended limit detector. By using common circuitry for both halves, the device can provide high speed with lower power dissipation than two single comparators. The LM711C is the commercial/industrial version of the LM711, with operation specified over a 0°C to +70°C temperature range.



Note: Pin 5 connected to case.

LM711H



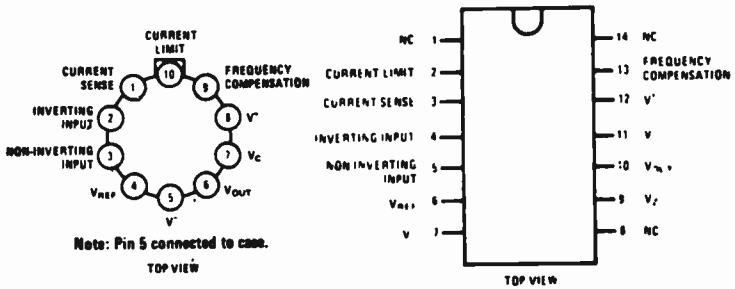
LM711CN

LM723/LM723C VOLTAGE REGULATOR

The LM723/LM723C is a voltage regulator designed primarily for series regulator applications. By itself, it will supply output currents up to 150 mA, but external transistors can be added to provide any desired load current. The circuit features extremely low standby current drain, and provision is made for either linear or foldback current limiting. Important characteristics are:

- 150 mA output current without external pass transistor
- Output currents in excess of 10A possible by adding external transistors
- Input voltage 40V max
- Output voltage adjustable from 2V to 37V
- Can be used as either a linear or a switching regulator

The LM723/LM723C is also useful in a wide range of other applications such as a shunt regulator, a current regulator or a temperature controller.



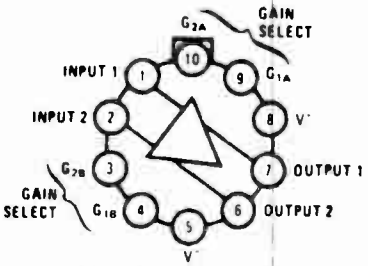
LM723

LM733/LM733C DIFFERENTIAL VIDEO AMPLIFIER

The LM733/LM733C is a 2-stage, differential input, differential output, wide-band video amplifier. The use of internal series-shunt feedback gives wide bandwidth with low phase distortion and high gain stability. Emitter-follower outputs provide a high current drive, low-impedance capability. Its 120-MHz bandwidth and selectable gains of 10, 100 and 400, without need for frequency compensation, make it a very useful circuit for memory element drivers, pulse amplifiers and wide-band linear gain stages.

The LM733 is specified for operation over the −55°C to +125°C military temperature range. The LM733C is specified for operation over the 0°C to +70°C temperature range. Features include:

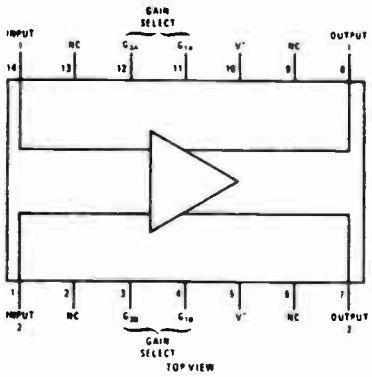
- 120-MHz bandwidth
- 250K input resistance
- Selectable gains of 10, 100, 400
- No frequency compensation
- High common mode rejection ratio at high frequencies.



Note: Pin 5 connected to case.

TOP VIEW

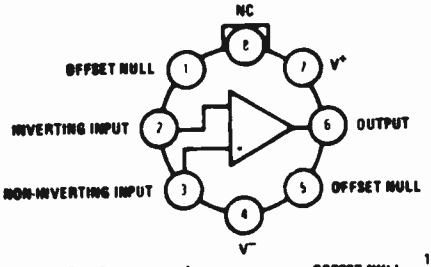
LM733H



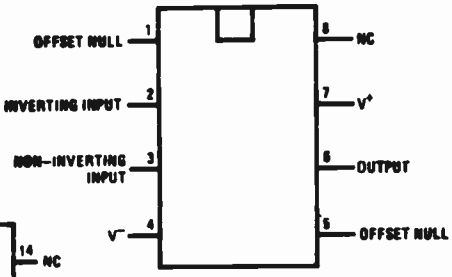
LM733D

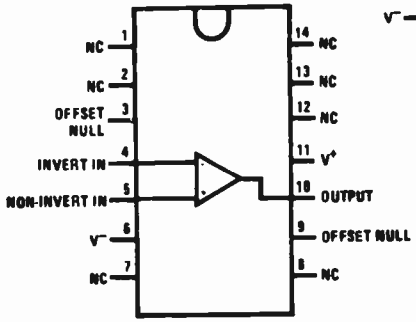
The LM741 series are general-purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features that make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations. The LM741C/LM741E are identical to the LM741/LM741A except that the LM741C/LM741E have their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.



Note: Pin 4 connected to case.



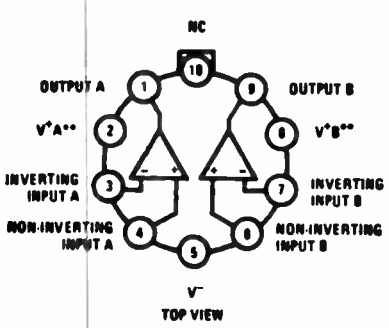


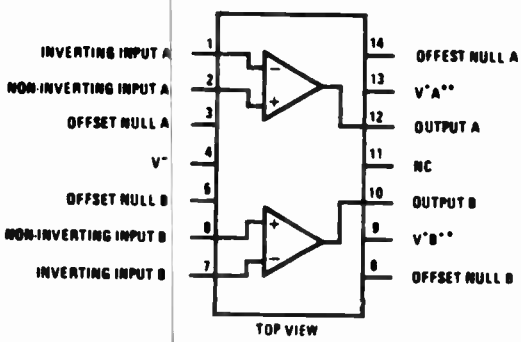
LM741

The LM747 series are general-purpose dual operational amplifiers. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent. Features include:

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low power consumption
- No latch-up
- Balanced offset null

The LM747C/LM747E is identical to the LM747/LM747A except that the LM747C/LM747E has its specifications guaranteed over the temperature range from 0°C to +70°C instead of −55°C to +125°C.





LM747

LM748/LM748C OPERATIONAL AMPLIFIER

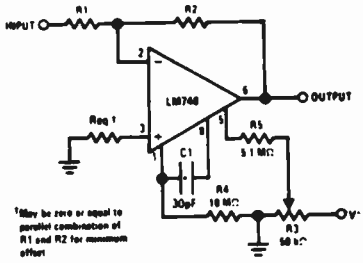
The LM748/LM748C is a general-purpose operational amplifier built on a single silicon chip. The resulting close match and tight thermal coupling gives low offsets and temperature drift as well as fast recovery from thermal transients. In addition, the device features:

- Frequency compensation with a single 30 pF capacitor
- Operation from ± 5V to ± 20V
- Low current drain—1.8 mA at ±20V
- Continuous short-circuit protection
- Operation as a comparator with differential inputs as high as ±30V
- No latch-up when common mode range is exceeded.
- Same pin configuration as the LM101.

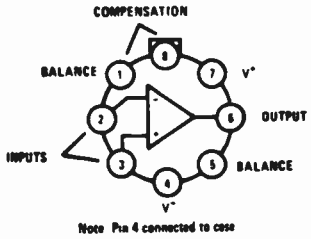
The unity-gain compensation specified makes the circuit stable for all feedback configurations, even with capacitive loads. However, it is possible to optimize compensation for best high-frequency performance at any gain. As a comparator, the output can be clamped at any desired level to make it compatible with logic circuits.

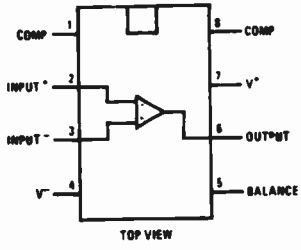
The LM748 is specified for operation over the −55°C to ±125°C military temperature range. The LM748C is specified for operation over the 0°C to +70°C temperature range.

Inverting Amplifier with Balancing Circuit



† May be zero or equal to parallel combination of R1 and R2 for minimum offset



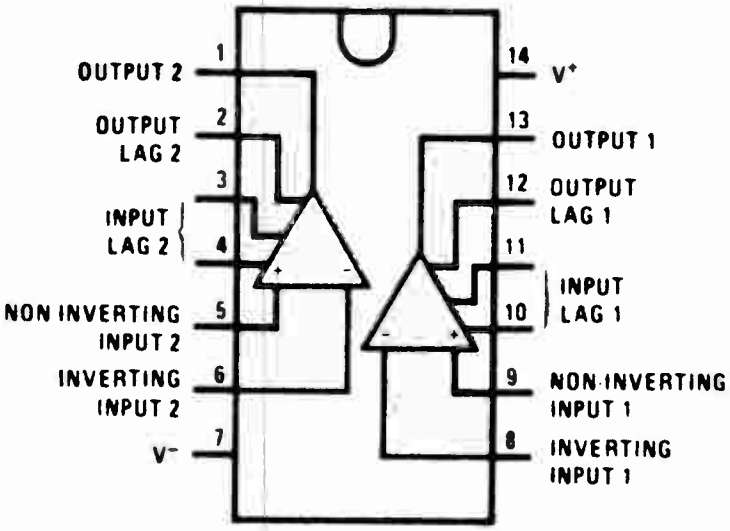


LM748

LM1303 STEREO PREAMPLIFIER

The LM1303 consists of two identical operational amplifiers constructed on a single silicon chip. Intended for amplification of low-level stereo signals, the LM1303 features low input noise voltage, high open-loop voltage gain, large output voltage swing and short-circuit protection.

Output Voltage Swing	4.0V rms min.
Open-Loop Voltage Gain	6,000 min.
Channel Separation	60 dB min. at 10 kHz



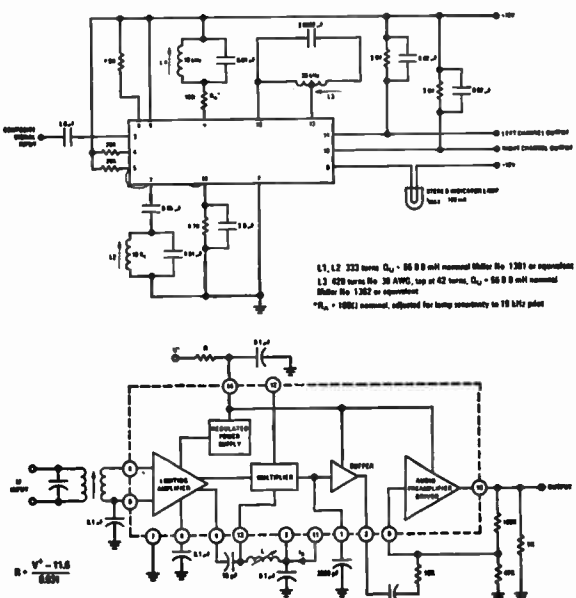
TOP VIEW

LM1303N

LM1304, LM1305, LM1307, LM1307E
FM MULTIPLEX STEREO DEMODULATOR

The LM1304, LM1305, LM1307 and LM1307E are designed to derive the left and right channel audio information from the detected composite stereo signal. The LM1304 eliminates the need for an external stereo-channel separation control. The LM1305 is similar to the LM1304 but permits the use of an external stereo channel separation control for maximum separation. The LM1307 is also similar to the LM1304 but does not have the audio mute control, or the stereo/mono switch. The LM1307E is similar to the LM1307 but has the option of emitter-follower output drivers for buffers or high-current applications. Features include:

- Operation over a wide power-supply range
- Built-in stereo-indicator lamp driver—100 mA typical
- Automatic switching between stereo and monaural
- Audio mute control

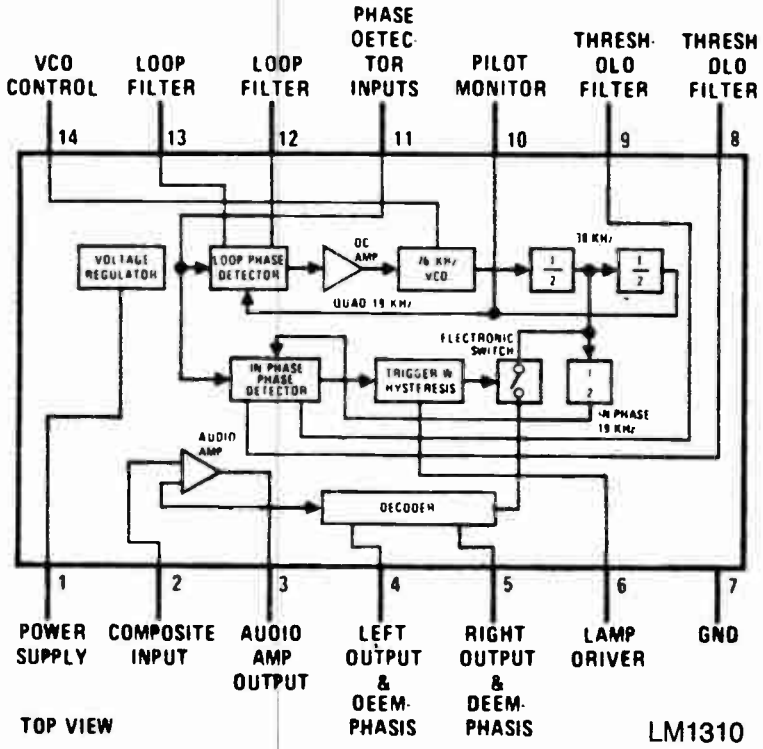


LM1304

LM1310 PHASE-LOCKED LOOP FM STEREO DEMODULATOR

The LM1310 is an integrated FM stereo demodulator using phase-locked loop techniques to regenerate the 38-kHz subcarrier. A second version also available is the LM1800 (see separate data sheet) which adds superb power-supply rejection and buffered (emitter-follower) outputs to the basic phase-locked decoder circuit. The features available in these integrated circuits make possible a system delivering high fidelity sound within the cost restraints of inexpensive stereo receivers. Features include:

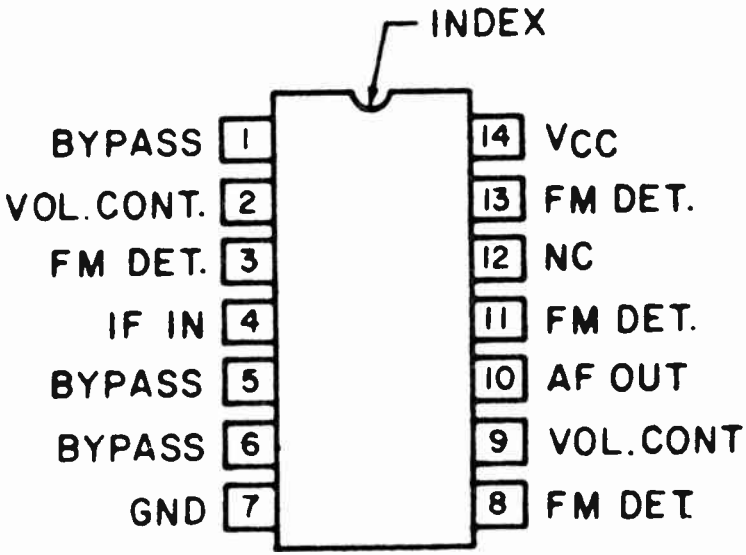
- Automatic stereo/monaural switching
- No coils, all tuning performed with single potentiometer
- Wide supply operating voltage range
- Excellent channel separation



LM1351 FM DETECTOR, LIMITER AND AUDIO AMPLIFIER

The LM1351 is a monolithic integrated circuit FM detector, limiter and audio amplifier that requires a minimum of external components for operation. It includes three stages of i-f limiting and a balanced product detector. The audio amplifier is capable of driving a single external transistor class A audio output stage. Features include:

- Direct replacement for MC1351
- Simple detector alignment—one coil or ceramic filter.
- Sensitivity—3-dB limiting voltage at 80 μV typ.
- Low harmonic distortion
- High i-f voltage gain
- High audio preamplifier open loop gain

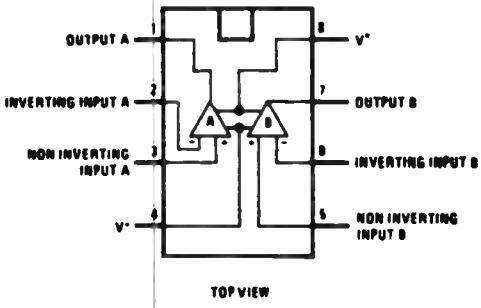


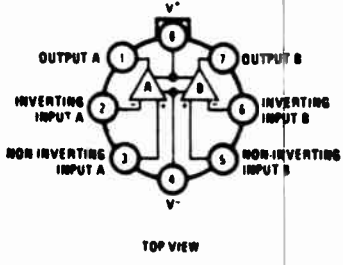
LM1351

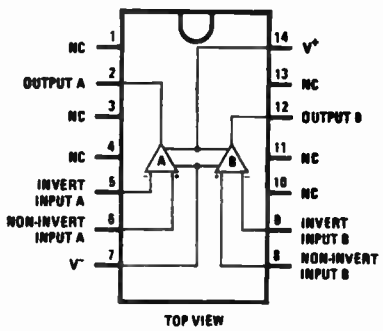
The LM1558 and LM1458 are general-purpose dual operational amplifiers. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent. Features include:

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low-power consumption
- 8-lead TO-5 and 8-lead mini-DIP
- No latch-up when input common mode range is exceeded

The LM1458 is identical to the LM1558 except that the LM1458 has its specifications guaranteed over the temperature range from 0°C to 70°C instead of the −55°C to +125°C range of the LM1588.







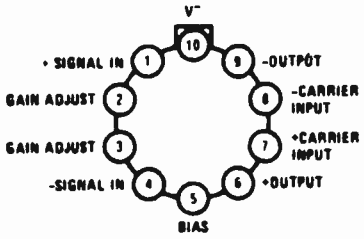
LM1558

The LM1596/LM1496 are double balanced modulator-demodulators that produce an output voltage proportional to the product of an input (signal)voltage and a switching (carrier) signal. Typical applications include suppressed carrier modulation, amplitude modulation, synchronous detection, FM or PM detection and broadband frequency doubling and chopping.

The LM1596 is specified for operation over the −55°C to +125°C military temperature range. The LM1496 is specified for operation over the 0°C to +70°C temperature range. Features include:

- Excellent carrier suppression
  - 65 dB typical at 9.5 MHz
  - 50 dB typical at 10 MHz
- Adjustable gain and signal handling
- Fully balanced inputs and outputs
- Low offset and drift
- Wide frequency response up to 100 MHz

Metal Can Package

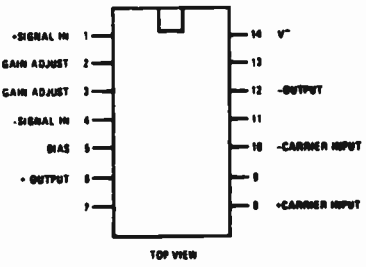


TOP VIEW

Note: Pin 10 is connected electrically to the case through the device substrate.

LM1496H

Dual-In-Line Package



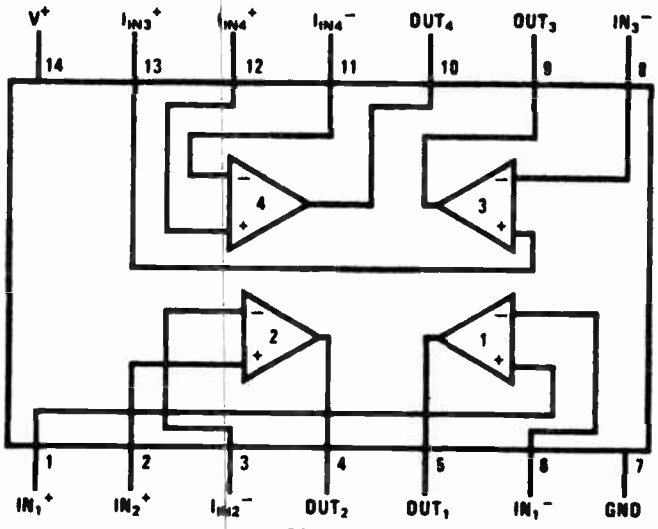
TOP VIEW

LM1496J

LM1900/LM2900/LM3900, LM3301, LM3401 QUAD AMPLIFIER

The LM1900 series consists of four independent, dual input, internally compensated amplifiers that were designed specifically to operate off of a single power supply voltage and to provide a large output voltage swing. These amplifiers make use of a current mirror to achieve the noninverting input function. They are used as AC amplifiers; RC active filters; low-frequency triangle, square and pulse wave generation circuits; tachometers and low-speed, high-voltage digital logic gates. Features include:

- Wide single supply voltage range or dual supplies
  4 V_{DC} to 36 V_{DC}
  ± 2 V_{DC} to ± 18 V_{DC}
- Supply current drain independent of supply voltage
- Low input biasing current 30 nA
- High open-loop gain 70 dB
- Wide bandwidth 2.5 MHz (unity gain)
- Large output voltage swing $(V^+ - 1)$ Vp-p
- Internally frequency compensated for unity gain
- Output short-circuit protection



TOP VIEW

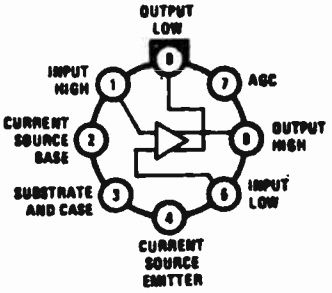
LM1900

LM3028A/LM3028B, LM3053 DIFFERENTIAL RF/I-F AMPLIFIER

The LM3028A/LM3028B and LM3053 is a monolithic rf/i-f amplifier intended for emitter-coupled (differential) or cascade amplifier operation from DC to 120 MHz in industrial and communications equipment. The LM3028A/LM3028B and LM3053 are plug-in replacements for the CA3028A/CA3028B and CA3053 respectively. The LM3028B is similar to the LM3028A but has premium performance with tighter limits in offset voltage and current, bias current and voltage gain. The LM3053 is similar to the LM3028A/LM3028B but is recommended for i-f amplifier operation with less critical DC parameters. Features include:

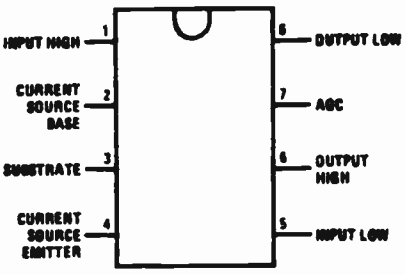
- Controlled for input offset voltage, input offset current and input bias current
- Balanced differential amplifier configuration with controlled-current source to provide unexcelled versatility
- Single-ended and dual-ended operation
- Operation from DC to 120 MHz
- Balanced agc capability
- Wide operating-current range

Metal Can Package



LM3028BH

Dual-In-Line Package

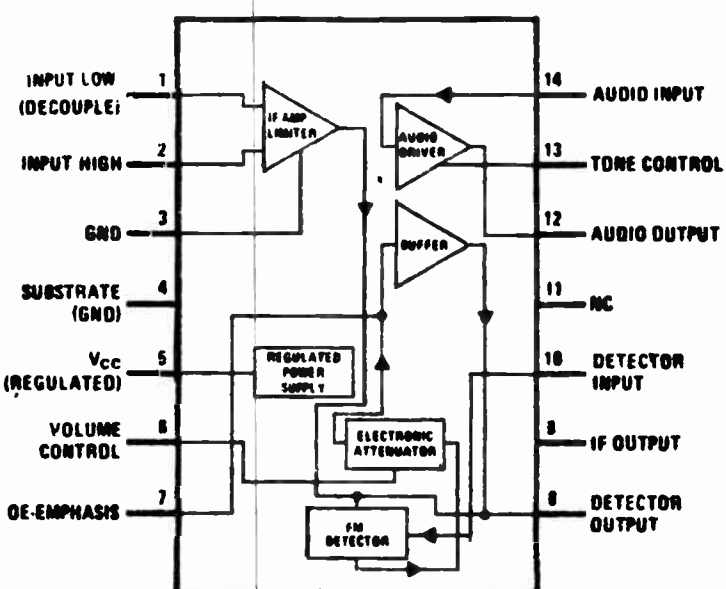


LM3053N

LM3065 TELEVISION SOUND SYSTEM

The LM3065 is a monolithic integrated circuit television sound system that requires a minimum of external components for operation. It includes three stages of i-f limiting, an FM detector, an electronic attenuator or volume control, an audio amplifier-driver, and a temperature-stable regulated power supply. Volume control is accomplished by varying bias levels of the electronic attenuator with a potentiometer between pin 6 and GND. Because no audio signal is present in this control, hum and noise pickup are easily filtered. Unshielded wire may be used for the volume control.

Volume Reduction Range	**> 60 dB**
Sensitivity	**3dB Limiting Voltage −200μV Typ.**
Audio Drive Capability	**6 mA p-p**
Undistorted Audio Output Voltage	**7v p-p**
AM Rejection	**50 dB typ. @4.5 MHz**



TOP VIEW

LM3065N

Section Four

TTL

In this chapter on the transistor-transistor logic, or TTL, family, you'll find the same type of information as we included in Chapter 1 on CMOS chips. In addition, we occasionally give the maximum clock frequency for flip-flops, counters and registers when it is appropriate.

TTL Chip Listing

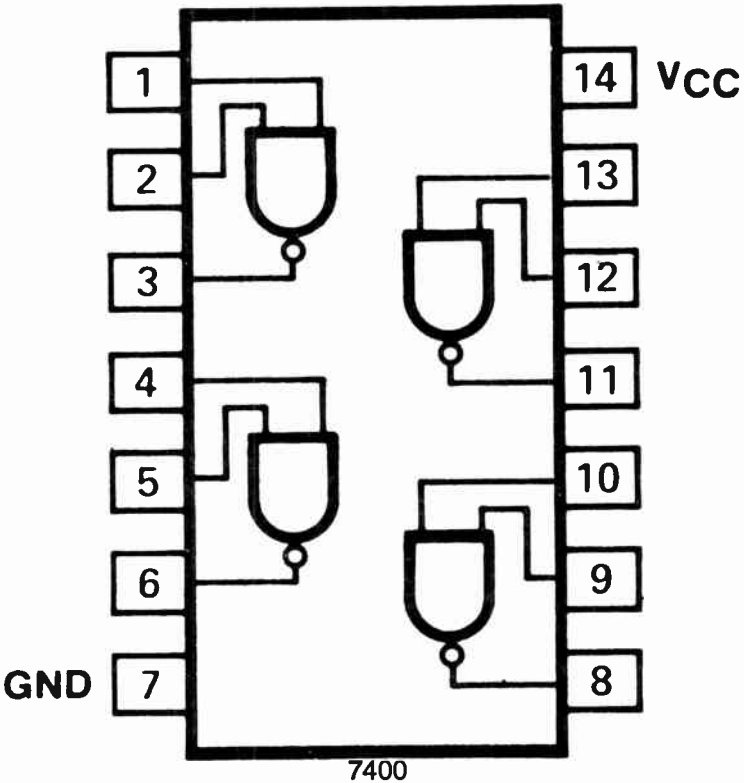
7400-Series TTL

7400 QUAD 2-INPUT NAND GATE

This device consists of four 2-input NAND gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable flip-flop circuits.

The NAND gate is a variation of the conventional AND gate, delivering an inverted (false) output when all inputs are true. The term "NAND" is a contraction of "NOT AND." Note that the output is true when either or both of the inputs are false. Essentially, a NAND gate is the result of using an active inverting element in the gate circuitry. As with a conventional AND gate, the NAND gate may have any number of inputs.

	74S	74H	74LS	74	74L
Typ. Delay Time (nS)	3	6	9.5	10	33
Typ. Power Per Gate (mW)	19	22	2	10	1



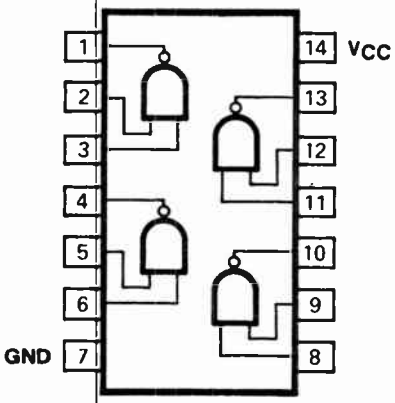
7401 QUAD 2-INPUT NAND GATE

This device consists of four 2-input NAND gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable flip-flop circuits.

The NAND gate is a variation of the conventional AND gate, delivering an inverted (false) output when all inputs are true. The term "NAND" is a contraction of "NOT AND." Note that the output is true when either or both of the inputs are false. Essentially, a NAND gate is the result of using an active inverting element in the gate circuitry. As with a conventional AND gate, the NAND gate may have any number of inputs.

Standard TTL gate outputs should not be tied together unless their logic levels will always be the same. Open-collector outputs, however, may be connected to other open-collector outputs to form additional logic. When outputs are thus tied together (OR-wired), a pullup resistor must be added between the common outputs and the positive supply. This is typically a 2.2K resistor. Open-collector outputs have a high output impedance in the HIGH state. Furthermore, they are slow acting, especially with capacitive loading.

	74H	74LS	74	74L
Typ. Delay Time (nS)	8	16	22	41
Typ. Power Per Gate (nW)	22	2	10	1

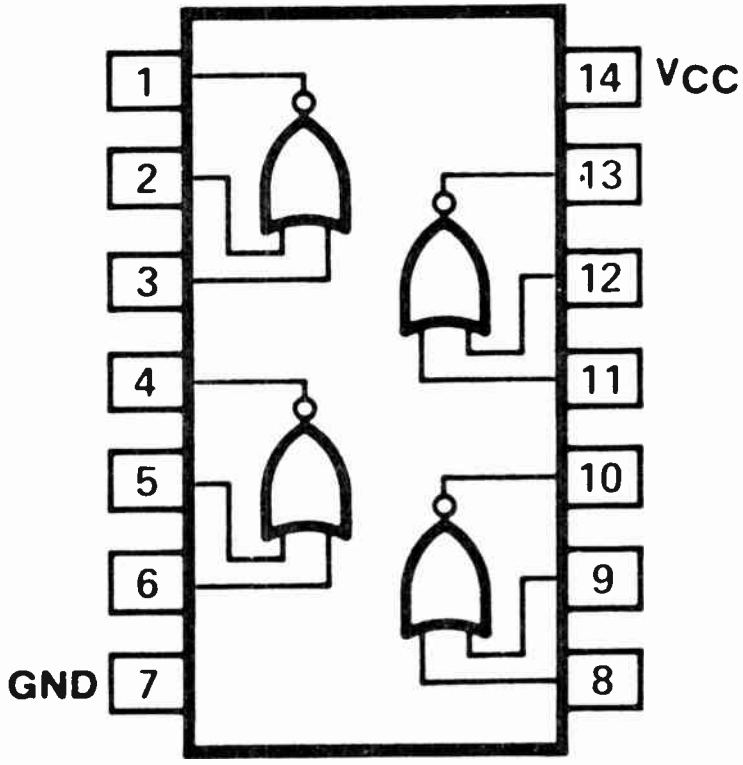


7401

7402 QUAD 2-INPUT NOR GATE

Standard TTL gate outputs should not be tied together unless their logic levels will always be the same. Open-collector outputs, however, may be connected to other open-collector outputs to form additional logic. When outputs are thus tied together (OR-wired), a pullup resistor must be added between the common outputs and the positive supply. This is typically a 2.2K resistor. Open-collector outputs have a high output impedance in the HIGH state. Furthermore, they are slow acting, especially with capacitive loading.

	74S	74LS	74	74L
Typ. Delay Time (nS)	3.5	10	10	33
Typ. Power Per Gate (mW)	29	2.75	14	1.5

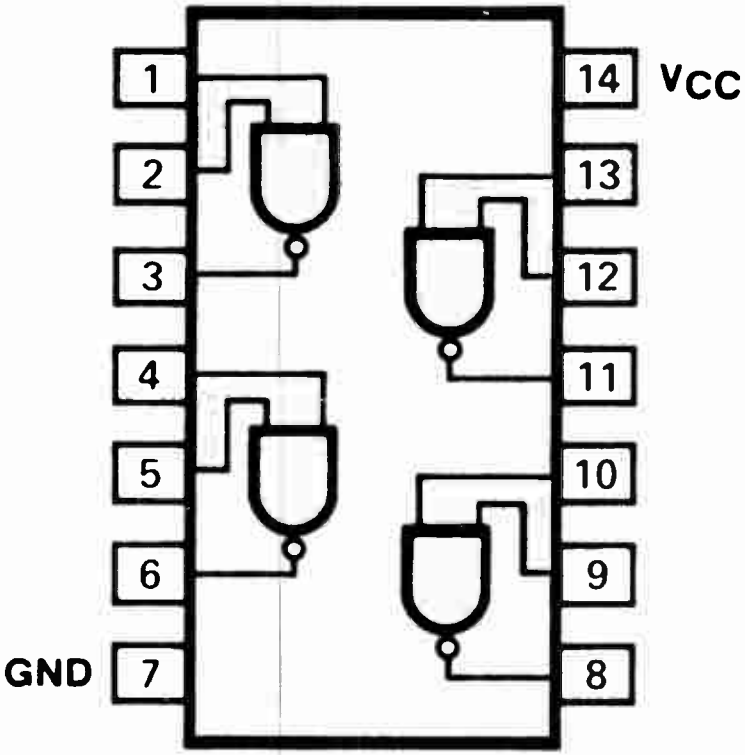


7402

7403 QUAD 2-INPUT NAND GATE (O.C.)

The NAND gate is a variation of the conventional AND gate, delivering an inverted (false) output when all inputs are true. The term "NAND" is a contraction of "NOT AND." Note that the output is true when either or both of the inputs are false. Essentially, a NAND gate is the result of using an active inverting element in the gate circuitry. As with a conventional AND gate, the NAND gate may have any number of inputs.

	74S	74LS	74	74L
Typ. Delay Time (nS)	5	16	22	41
Typ. Power Per Gate (mW)	17.2	2	10	1

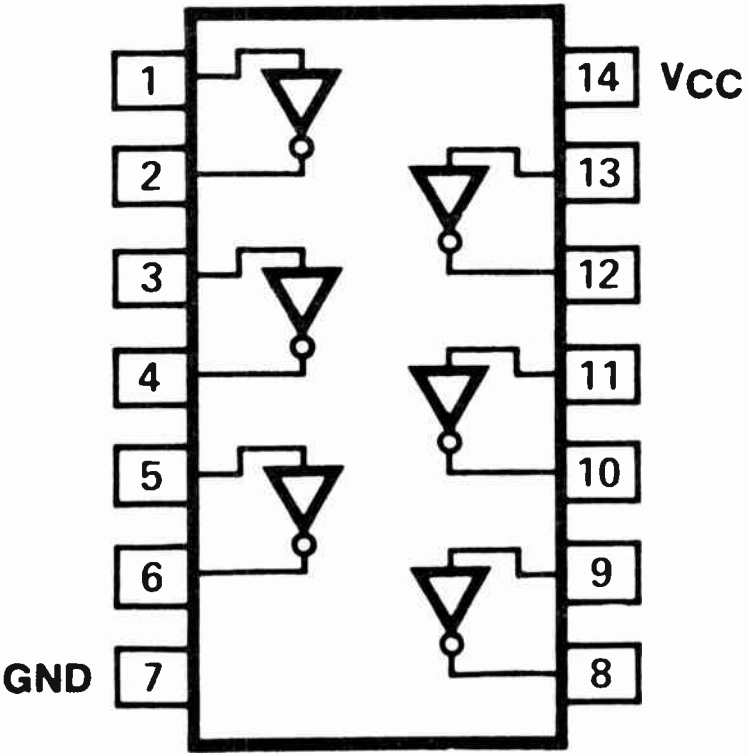


7403

7404 HEX INVERTER

As logic elements are combined in series to perform logic functions, voltage levels tend to degrade. Thus, amplifiers are sometimes needed to restore voltages or currents to proper levels. Assuming no inversion is encountered, a true input will produce a true output, and a false input will produce a false output. When inversion occurs, an inversion is placed at the output, and the symbol is usually termed an inverter.

	74S	74H	74LS	74	74L
Typ. Delay Time (nS)	3	6	9.5	10	33
Typ. Power Per Gate (mW)	19	22	2	10	1

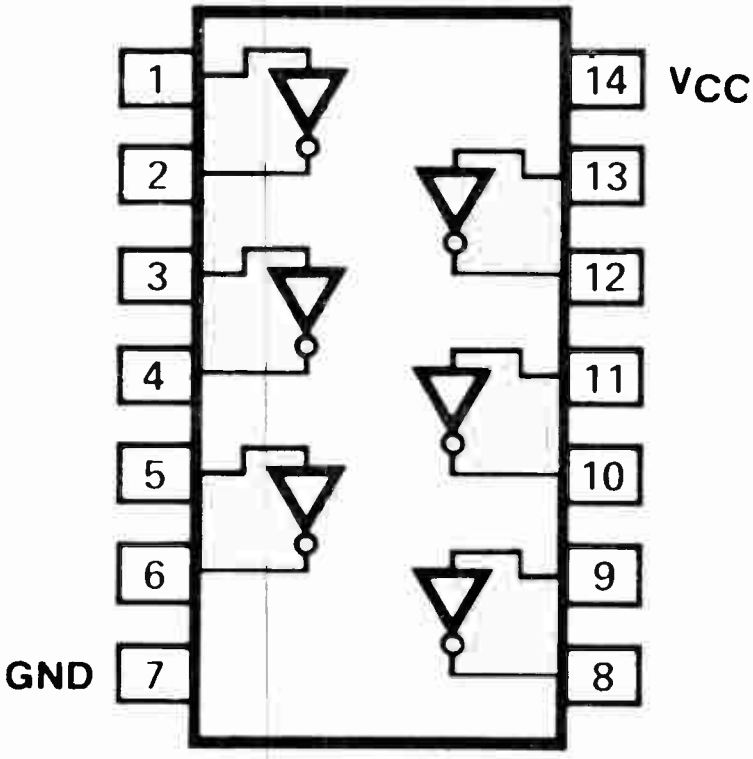


7404

7405 HEX INVERTER (O.C.)

As logic elements are combined in series to perform logic functions, voltage levels tend to degrade. Thus, amplifiers are sometimes needed to restore voltages or currents to proper levels. Assuming no inversion is encountered, a true input will produce a true output, and a false input will produce a false output. When inversion occurs, an inversion is placed at the output, and the symbol is usually termed an inverter.

	74S	74H	74LS	74
Typ. Delay Time (nS)	5	8	16	22
Typ. Power Per Gate (mW)	17.5	22	2	10

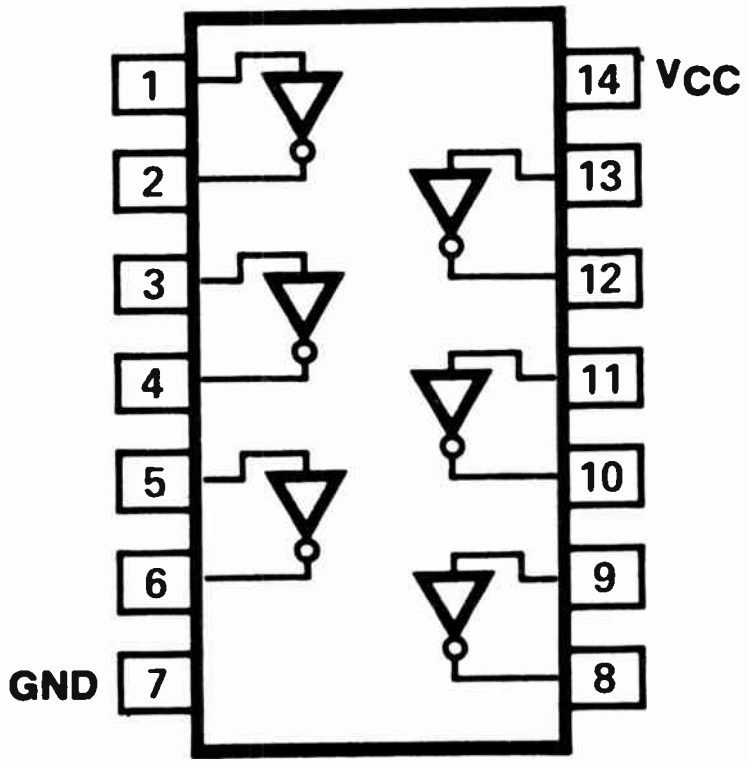


7405

7406 HEX INVERTER BUFFER/DRIVER (O.C.)

As logic elements are combined in series to perform logic functions, voltage levels tend to degrade. Thus, amplifiers are sometimes needed to restore voltages or currents to proper levels. Assuming no inversion is encountered, a true input will produce a true output, and a false input will produce a false output. When inversion occurs, an inversion is placed at the output, and the symbol is usually termed an inverter.

	74
High-Level Output Voltage (V)	30
Low-Level Output Current (mA)	40
Typ. Oelay Time (nS)	12.5
Typ. Power Per Gate (mW)	26

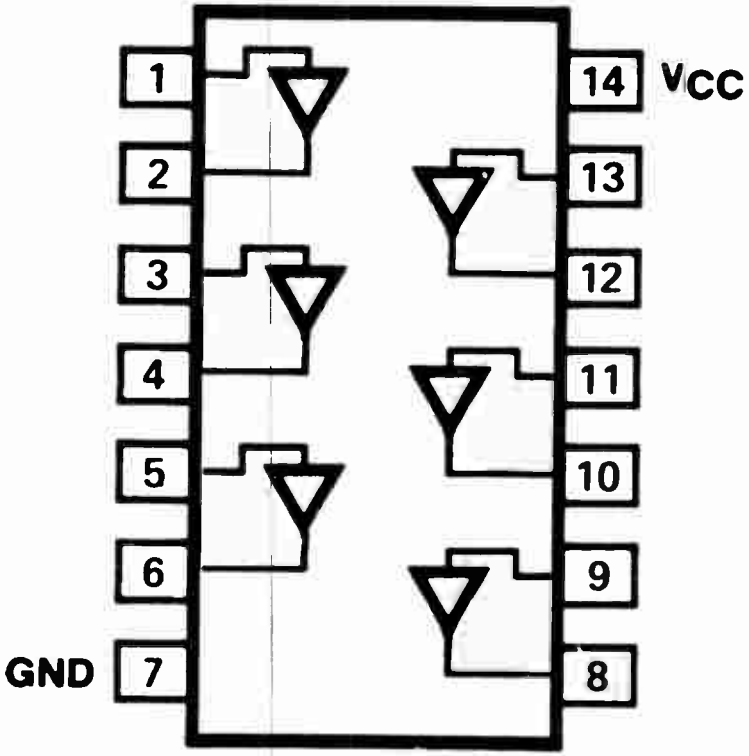


7406

7407 HEX BUFFER/DRIVER (O.C.)

As logic elements are combined in series to perform logic functions, voltage levels tend to degrade. Thus, amplifiers are sometimes needed to restore voltages or currents to proper levels. Assuming no inversion is encountered, a true input will produce a true output, and a false input will produce a false output. When inversion occurs, an inversion is placed at the output, and the symbol is usually termed an inverter.

	74
High-Level Output Voltage (V)	30
Low-Level Output Current	40
Typ. Delay Time (ns)	13
Typ. Power Per Gate (mW)	21

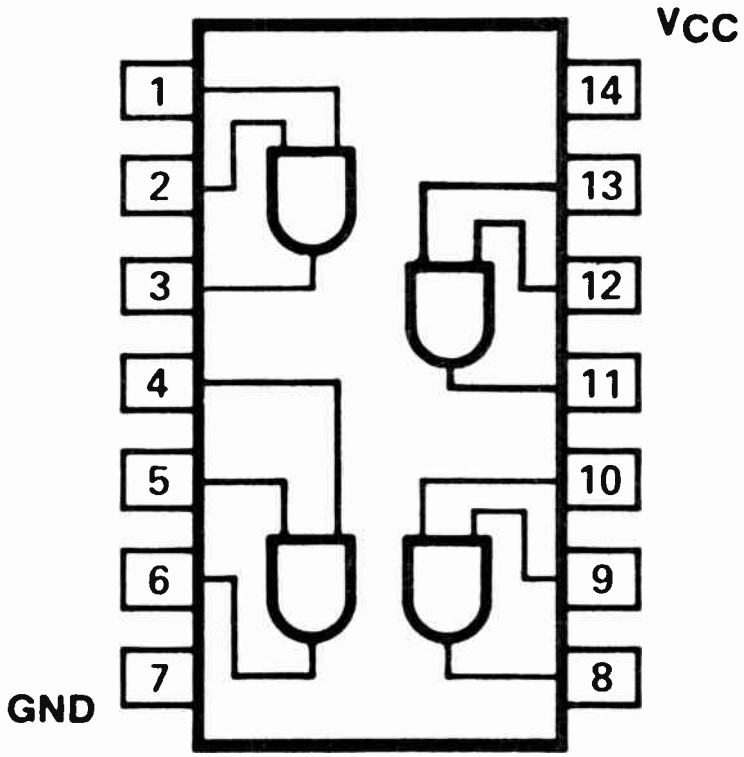


7407

7408 QUAD 2-INPUT AND GATE

The symbol for the AND gate is shown below. By definition, for output C to be true, inputs A and B must be true; hence, the term AND gate.

	74LS	74
Typ. Delay Time (ns)	12	15
Typ. Power Per Gate (mW)	4.25	19

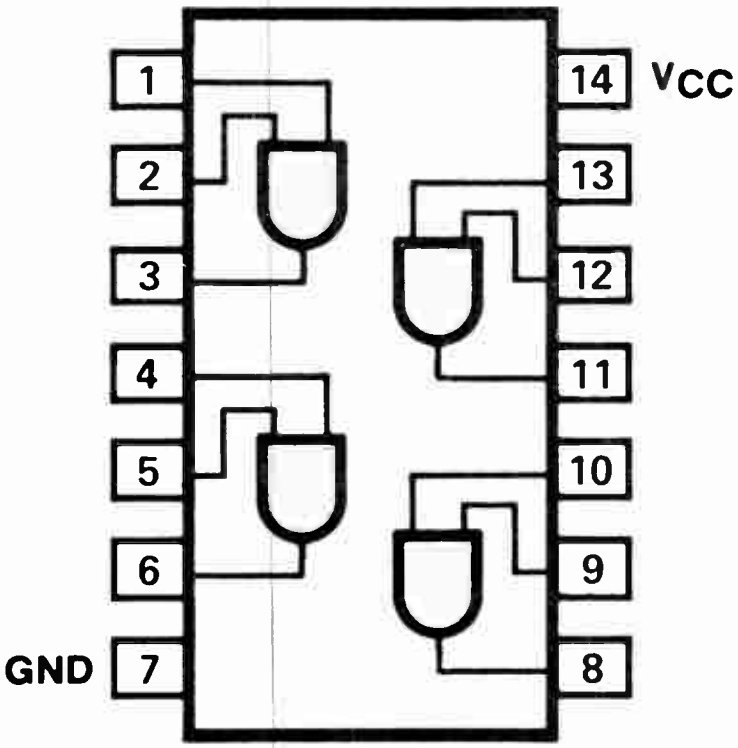


7408

7409 QUAD 2-INPUT AND GATE (O.C.)

The symbol for the AND gate is shown below. By definition, for output C to be true, inputs A and B must be true; hence, the term AND gate.

	74	74LS
Typ. Delay Time (ns)	18.5	20
Typ. Power Per Gate (mW)	19.4	4.25

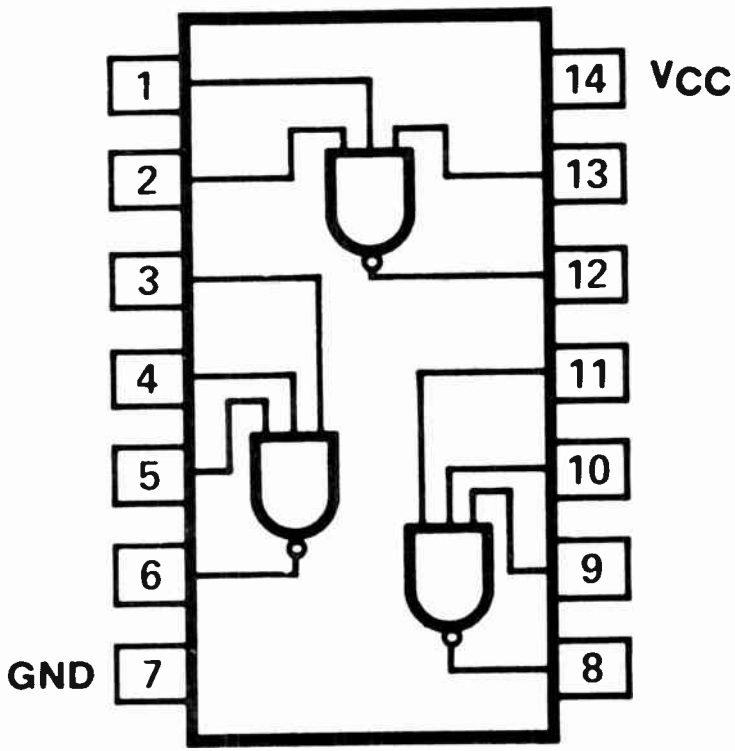


7409

7410 TRIPLE 3-INPUT NAND GATE

The NAND gate is a variation of the conventional AND gate, delivering an inverted (false) output when all inputs are true. The term NAND is a contraction of NOT AND. Note that the output is true when either or both of the inputs are false. Essentially, a NAND gate is the result of using an active inverting element in the gate circuitry. As with a conventional AND gate, the NAND gate may have any number of inputs.

	74S	74H	74LS	74	74L
Typ. Delay Time (ns)	3	6	9.5	10	33
Typ. Power Per Gate (mW)	19	22	2	10	1

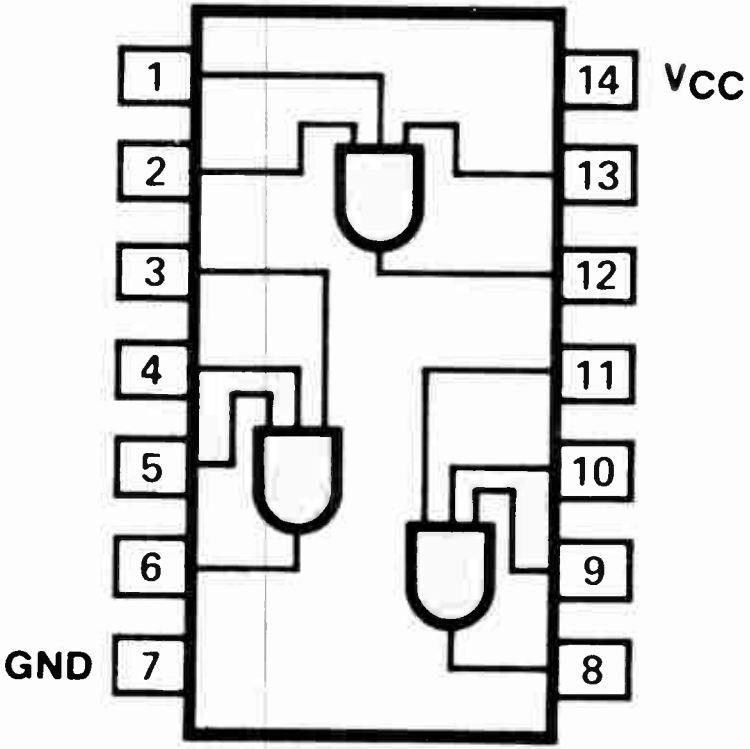


7410

7411 TRIPLE 3-INPUT AND GATE

The symbol for the AND gate is shown here. By definition, for output C to be true, inputs A and B must be true; hence the term AND gate.

	74S	74H	74LS
Typ. Delay Time (ns)	4.75	8.2	12
Typ. Power Per Gate (mW)	31	40	4.25

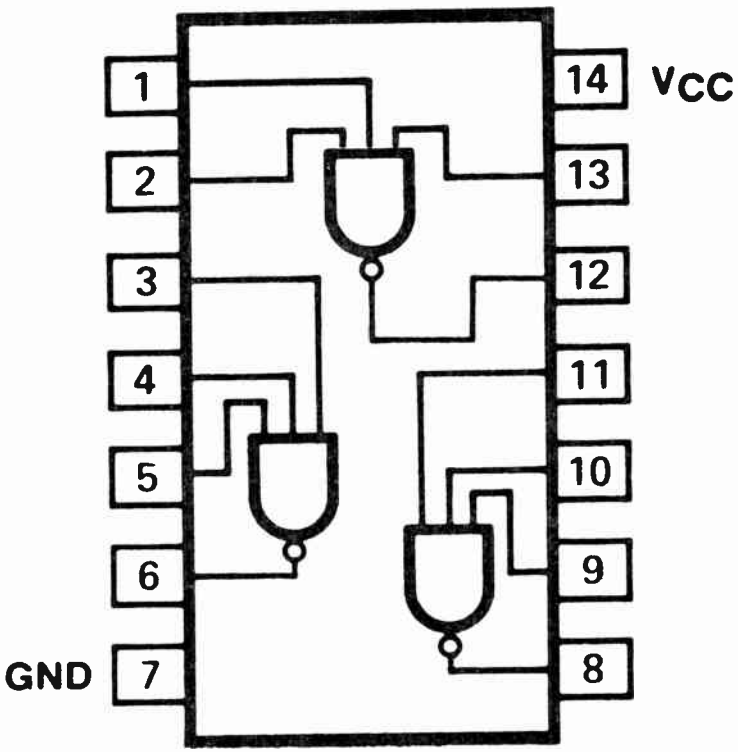


7411

7412 TRIPLE 3-INPUT NAND GATE (O.C.)

The NAND gate is a variation of the conventional AND Gate, delivering an inverted (false) output when all inputs are true. The term NAND is a contraction of NOT AND. Note that the output is true when either or both of the inputs are false. Essentially, a NAND gate is the result of using an active inverting element in the gate circuitry. As with a conventional AND gate, the NAND gate may have any number of inputs.

	74LS
Typ. Delay Time (ns)	16
Typ. Power Per Gate (mW)	2



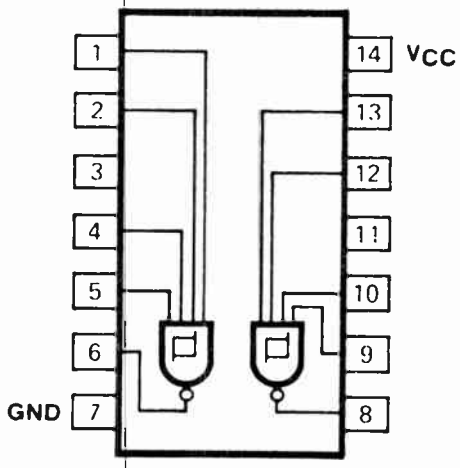
7412

7413 DUAL 4-INPUT NAND SCHMITT TRIGGER

The "13" contains two 4-input NAND gates that accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

Each circuit contains a 4-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger used positive feedback to effectively speed-up slow input transistions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800 mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than $V_{T+\,(max)}$, the gate will respond in the transitions of the other input as shown in Figure A.

	74	74LS
Typ. Hysteresis (V)	0.8	0.8
Typ. Delay Time (ns)	16.5	16.5

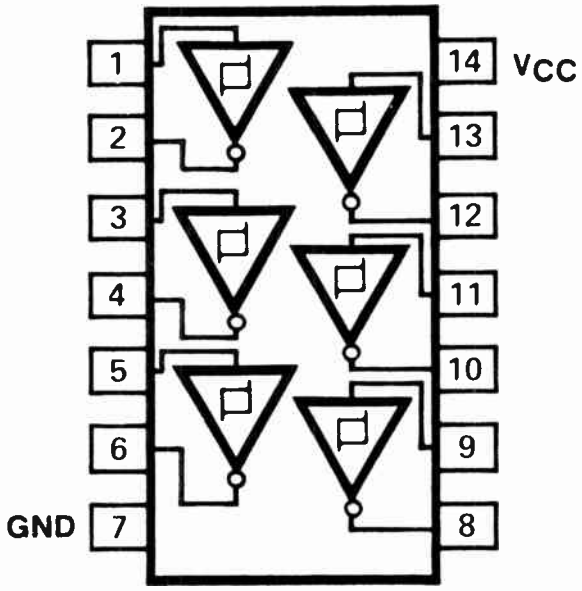


7413

The "14" contains six logic inverters that accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin that conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed up slow input transition, and provide different input threshold voltages for positive-going and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

	74	74LS
Typ. Hysteresis (V)	0.8	0.8
Typ. Delay Time (ns)	15	15

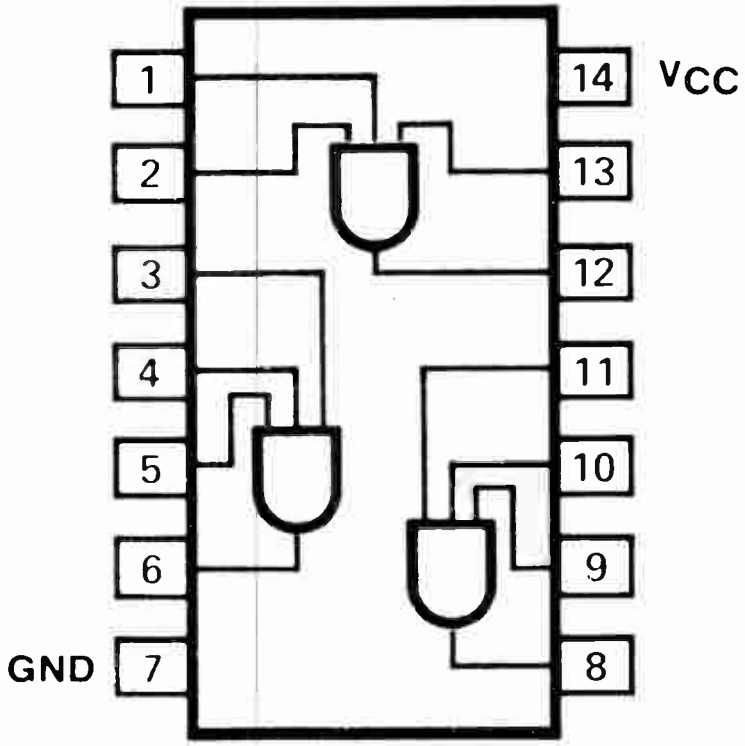


7414

7415 TRIPLE 3-INPUT AND GATE (O.C.)

The symbol for the AND gate is shown here. By definition, for output C to be true, inputs A and B must be true; hence, the term AND gate.

	74S	74LS
Typ. Delay Time (ns)	6	20
Typ. Power Per Gate (mW)	28	4.25

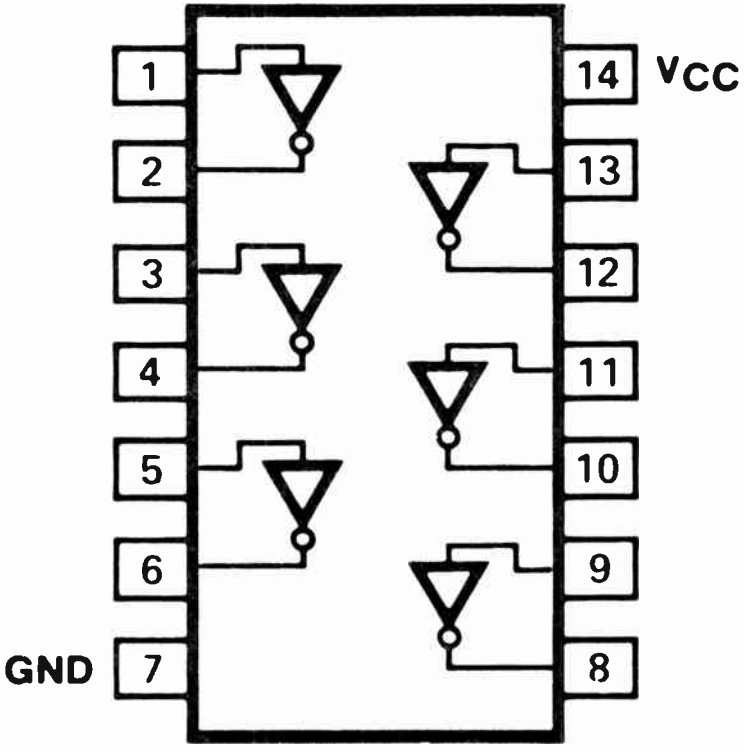


7415

7416 HEX INVERTER BUFFER/DRIVER (O.C.)

As logic elements are combined in series to perform logic functions, voltage levels tend to degrade. Thus, amplifiers are sometimes needed to restore voltages or currents to proper levels. Assuming no inversion is encountered, a true input will produce a true output, and a false input will produce a false output. When inversion occurs, an inversion is placed at the output, and the symbol is usually termed an inverter.

	74
High-Level Output Voltage (V)	15
Low-Level Output Current (mA)	40
Typ. Delay Time (ns)	12.5
Typ. Power Per Gate (mW)	26

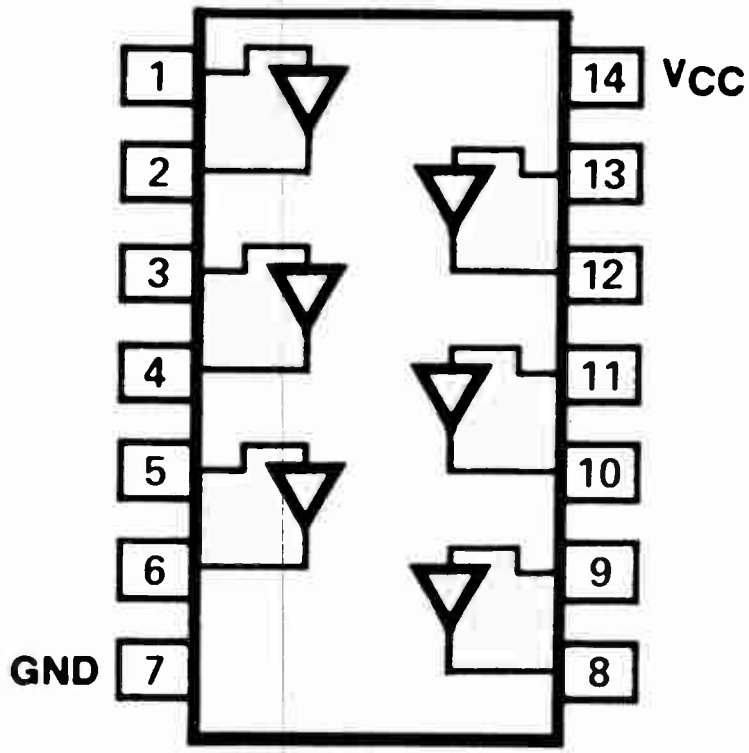


7416

7417 HEX BUFFER DRIVER (O.C.)

As logic elements are combined in series to perform logic functions, voltage levels tend to degrade. Thus, amplifiers are sometimes needed to restore voltages or currents to proper levels. Assuming no inversion is encountered, a true input will produce a true output, and a false input will produce a false output. When inversion occurs, an inversion is placed at the output, and the symbol is usually termed an inverter.

	74
High-Level Output Voltage (V)	15
Low-Level Output Current (mS)	40
Typ. Delay Time (ns)	13
Typ. Power Per Gate (mW)	21

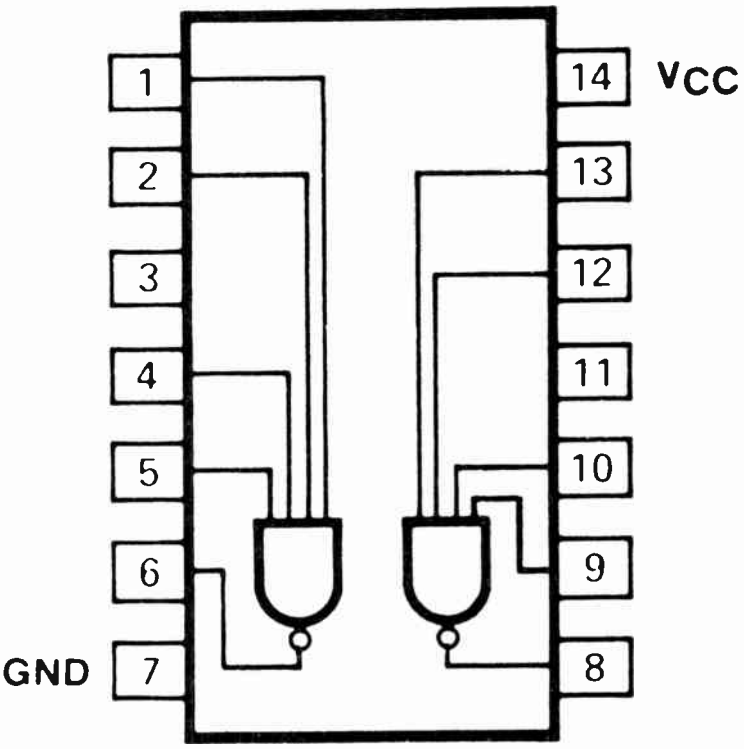


7417

7420 DUAL 4-INPUT NAND GATE

The NAND gate is a variation of the conventional AND gate, delivering an inverted (false) output when all inputs are true. The term AND is a contraction of NOT AND. Note that the output is true when either or both of the inputs are false. Essentially, a NAND gate is the result of using an active inverting element in the gate circuitry. As with a conventional AND gate, the NAND gate may have any number of inputs.

	74S	74H	74LS	74
Typ. Delay Time (ns)	3	6	9.5	10
Typ. Power Per Gate (mW)	19	22	2	10

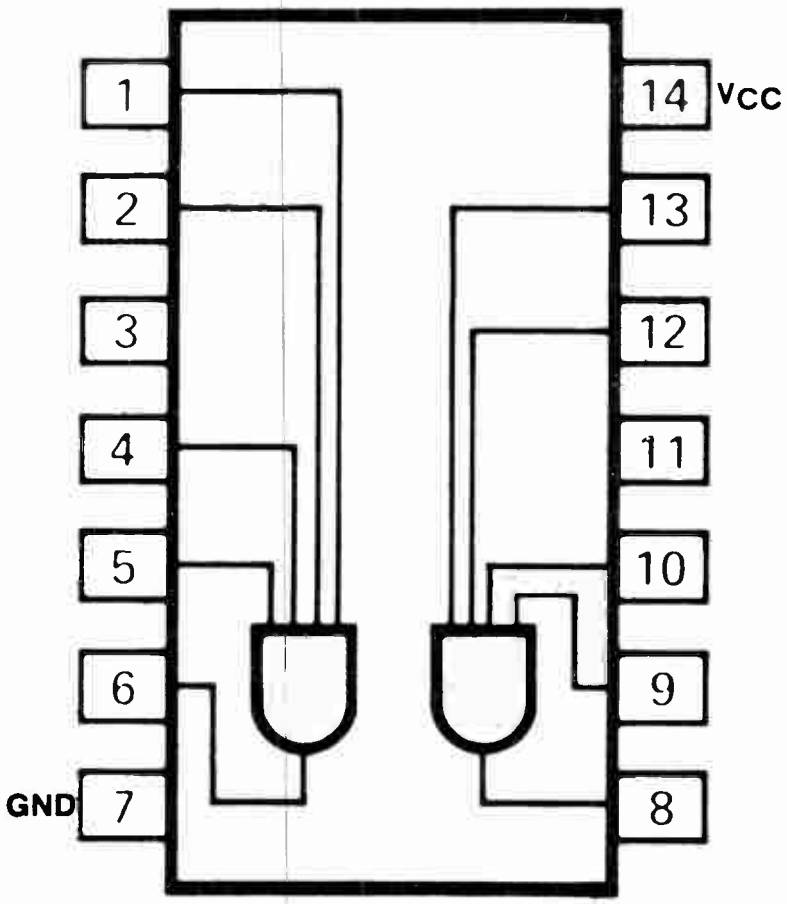


7420

7421 DUAL 4-INPUT AND GATE

The symbol for the AND gate is shown below. By definition, for output C to be true, inputs A and B must be true; hence, the term AND gate.

	74H	74LS
Typ. Delay Time (ns)	8.2	12
Typ. Power Per Gate (mW)	40	4.25

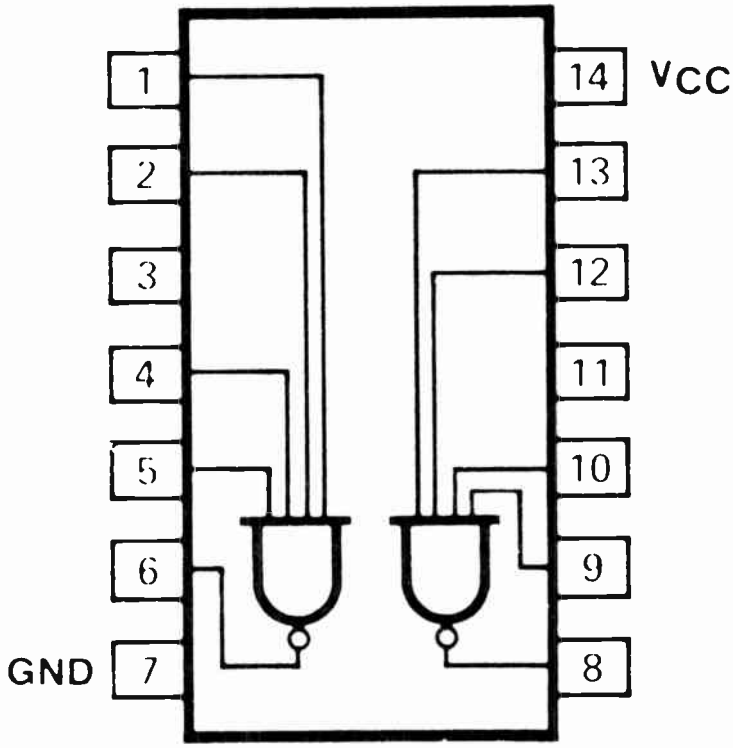


7421

7422 DUAL 4-INPUT NAND GATE (O.C.)

The NAND gate is a variation of the conventional AND gate, delivering an inverted (false) output when all inputs are true. The term AND is a contraction of NOT AND. Note that the output is true when either or both of the inputs are false. Essentially, a NAND gate is the result of using an active inverting element in the gate circuitry. As with a conventional AND gate, the NAND gate may have any number of inputs.

	74S	74H	74LS
Typ. Delay Time (ns)	5	8	16
Typ. Power Per Gate (mW)	17.5	22	2

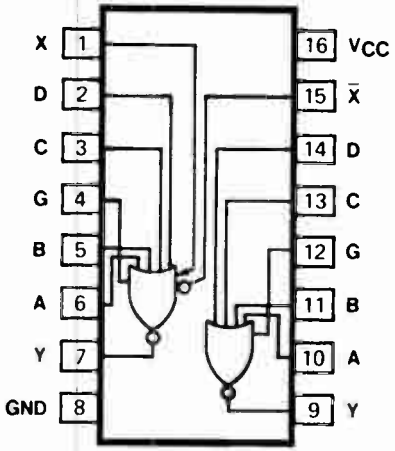


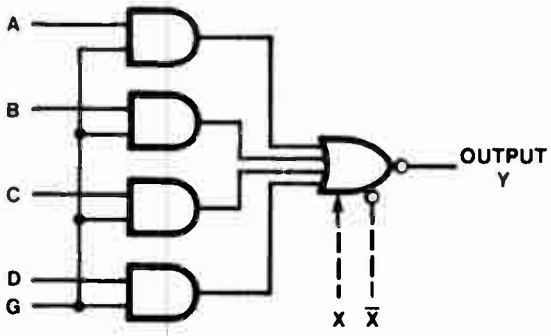
7422

7423 EXPANDABLE DUAL 4-INPUT NOR GATE WITH STROBE

Similar to the NAND gate, the NOR gate is a variation of the conventional OR gate, delivering an inverted (false) output when any or all of its inputs are true. The term NOR is a contraction of NOT OR. Note that the output is true when all inputs are false. Like the NAND gate, the NOR gate uses an active inverting element in the gate circuitry. The NOR gate also may have any number of inputs.

	74
Typ. Delay Time (ns)	10.5
Typ. Power Per Gate (mW)	23



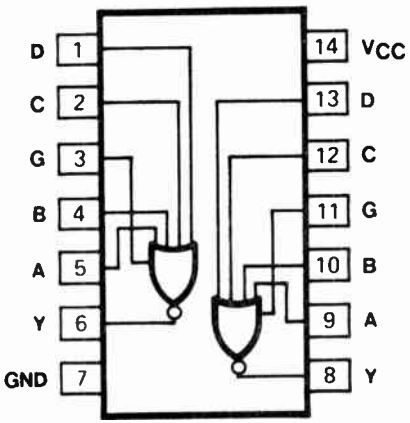


7423

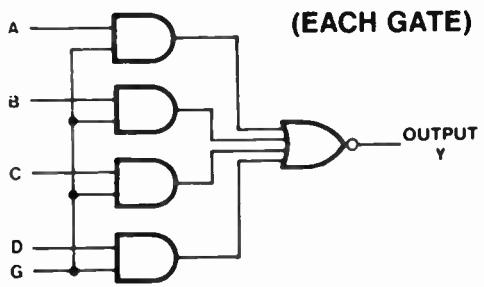
7425 DUAL 4-INPUT NOR WITH STROBE

Similar to the NAND gate, the NOR gate is a variation of the conventional OR gate, delivering an inverted (false) output when any or all of its inputs are true. The term NOR is a contraction of NOT OR. Note that the output is true when all inputs are false. Like the NAND gate, the NOR gate used an active inverting element in the gate circuitry. The NOR gate also may have any number of inputs.

	74
Typ. Delay Time (ns)	10.5
Typ. Power Per Gate (nW)	23



7425

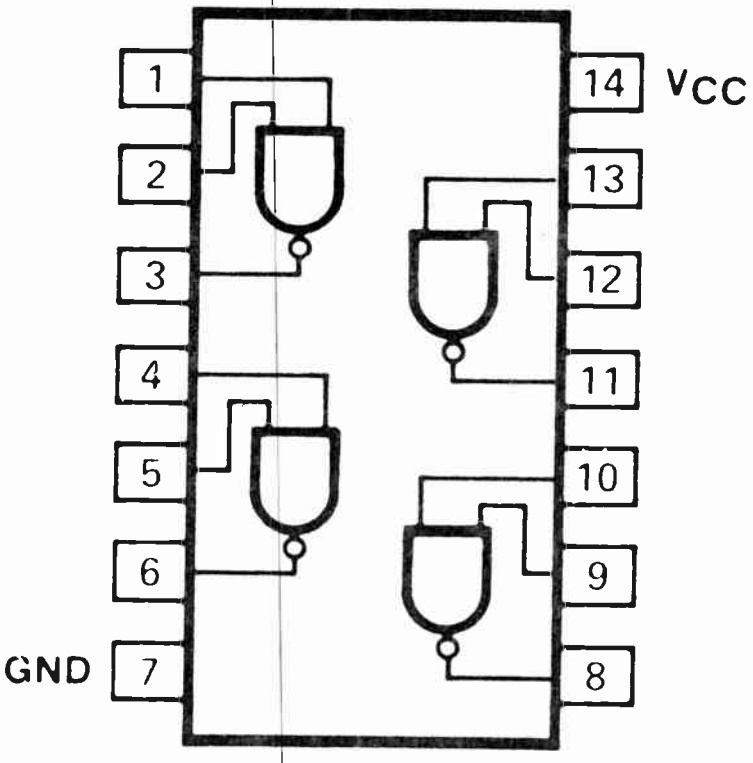


7425

7426 QUAD 2-INPUT NAND GATE (O.C.)

The NAND gate is a variation of the conventional AND gate, delivering an inverted (false) output when all inputs are true. The term AND is a contraction of NOT AND. Note that the output is true when either or both of the inputs are false. Essentially, a NAND gate is the result of using an active inverting element in the gate circuitry. As with a conventional AND gate, the NAND gate may have any number of inputs.

	74	74LS
High-Level Output Voltage (V)	15	15
Low-Level Output Current (mA)	16	8
Typ. Delay Time (ns)	13.5	16
Typ. Power Per Gate (mW)	10	2

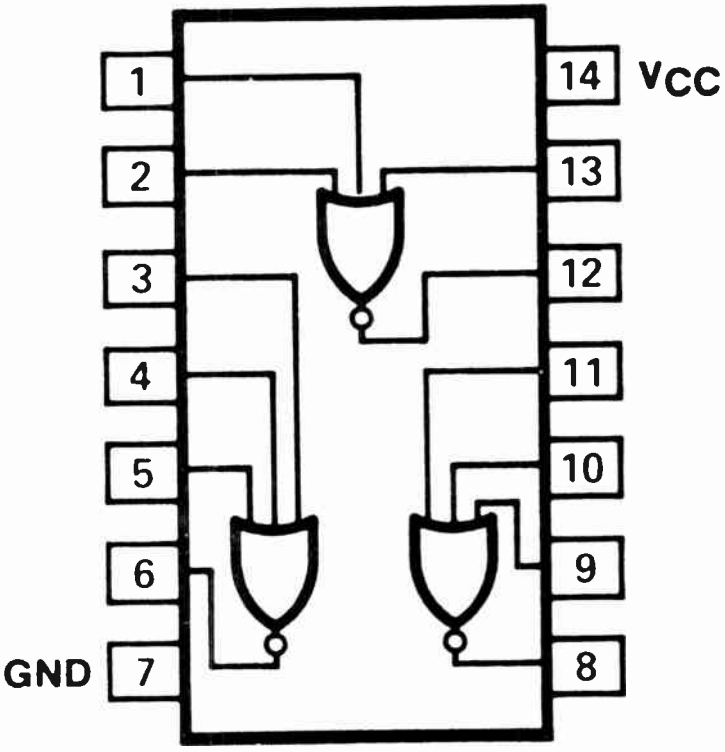


7426

7427 TRIPLE 3-INPUT NOR GATE

Similar to the NAND gate, the NOR gate is a variation of the conventional OR gate, delivering an inverted (false) output when any or all of its inputs are true. The term NOR is a contraction of NOT OR. Note that the output is true when all inputs are false. Like the NAND gate, the NOR gate used an active inverting element in the gate circuitry. The NOR gate also may have any number of inputs.

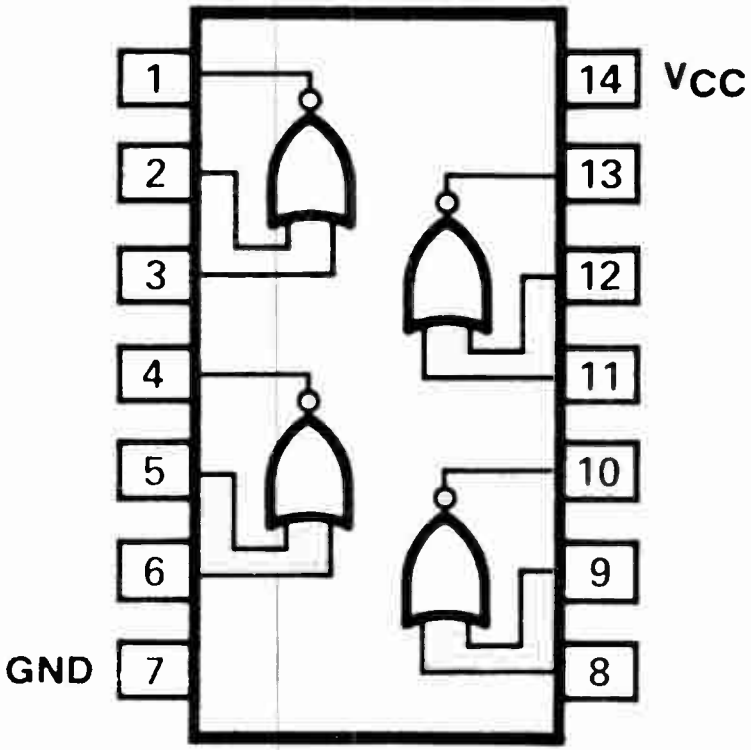
	74	74LS
Typ. Delay Time (ns)	8.5	10
Typ. Power Per Gate (mW)	22	4.5



7427

7428 QUAD 2-INPUT NOR BUFFER

Similar to the NAND Gate, the NOR gate is a variation of the conventional OR gate, delivering an inverted (false) output when any or all of its inputs are true. The term NOR is a contraction of NOT OR. Note that the output is true when all inputs are false. Like the NAND gate, the NOR gate used an active inverting element in the gate circuitry. The NOR gate also may have any number of inputs.

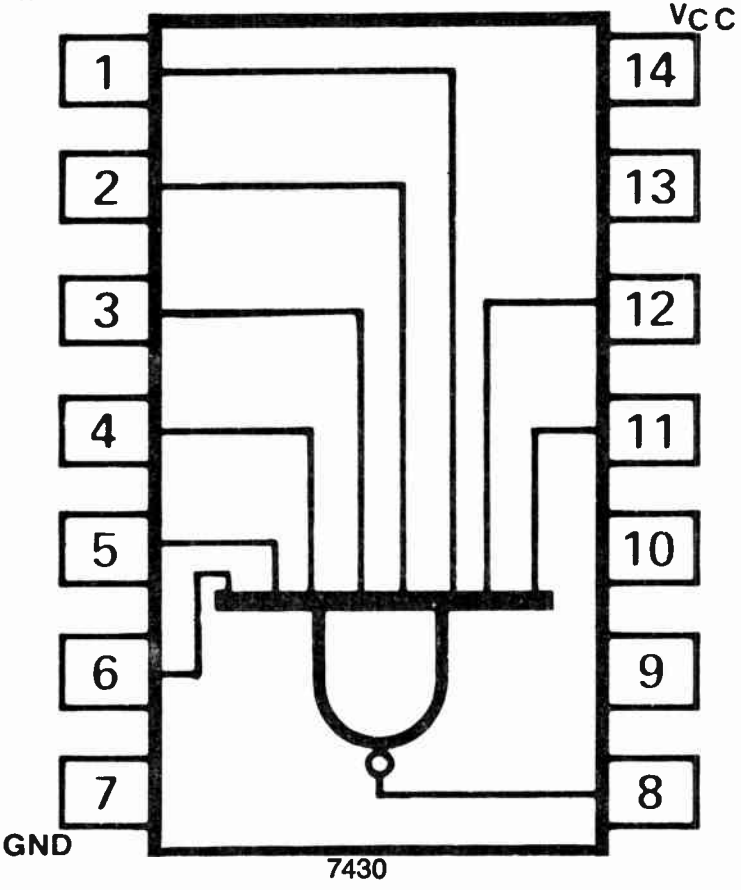


7428

7430 8-INPUT NAND GATE

The NAND gate is a variation of the conventional AND gate, delivering an inverted (false) output when all inputs are true. The term AND is a contraction of NOT AND. Note that the output is true when either or both of the inputs are false. Essentially, a NAND gate is the result of using an active inverting element in the gate circuitry. As with a conventional AND gate, the NAND gate may have any number of inputs.

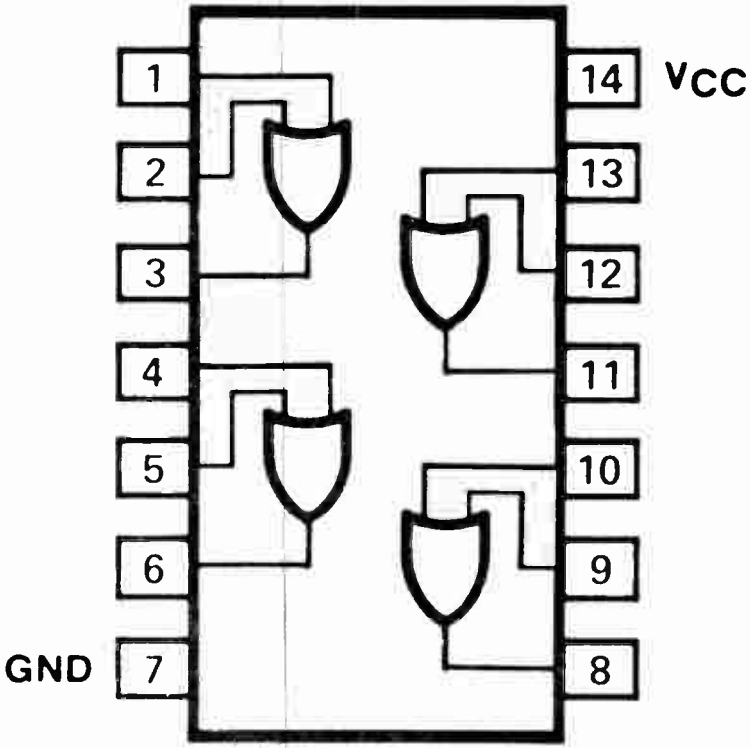
	74S	74H	74	74LS	74L
Typ. Delay Time (ns)	3	6	10	17	33
Typ. Power Per Gate (mW)	19	22	10	2.4	1



7432 QUAD 2-INPUT OR GATE

Note the symbol for the OR gate. By definition, for C to be true, either input A or input B must be true; hence, the name OR gate.

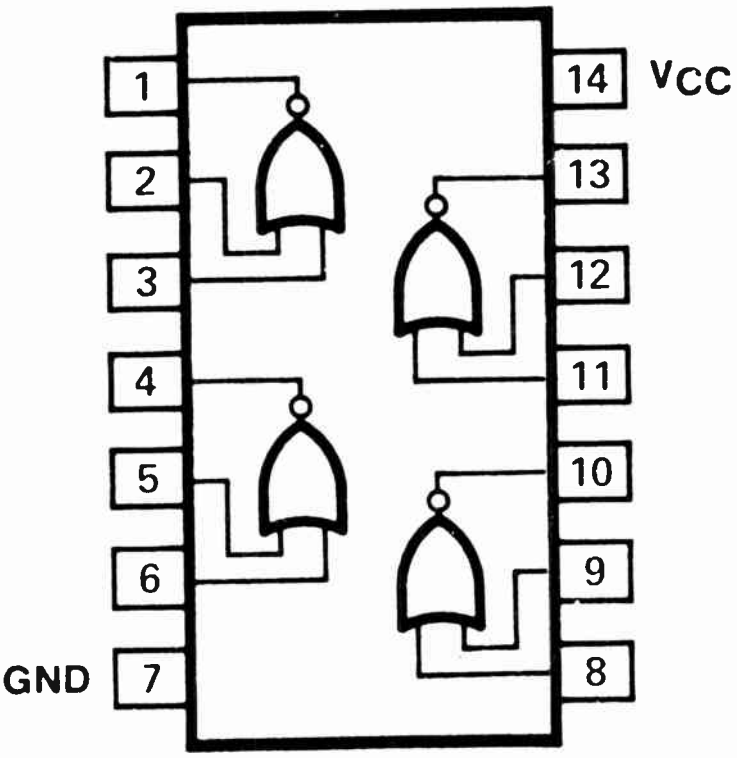
	74
Typ. Delay Time (ns)	12
Typ. Power Per Gate (mW)	24



7432

7433 QUAD 2-INPUT NOR BUFFER

Similar to the NAND gate, the NOR gate is a variation of the conventional OR gate, delivering an inverted (false) output when any or all of its inputs are true. The term NOR is a contraction of NOT OR. Note that the output is true when all inputs are false. Like the NAND gate, the NOR gate uses an active inverting element in the gate circuitry. The NOR gate also may have any number of inputs.

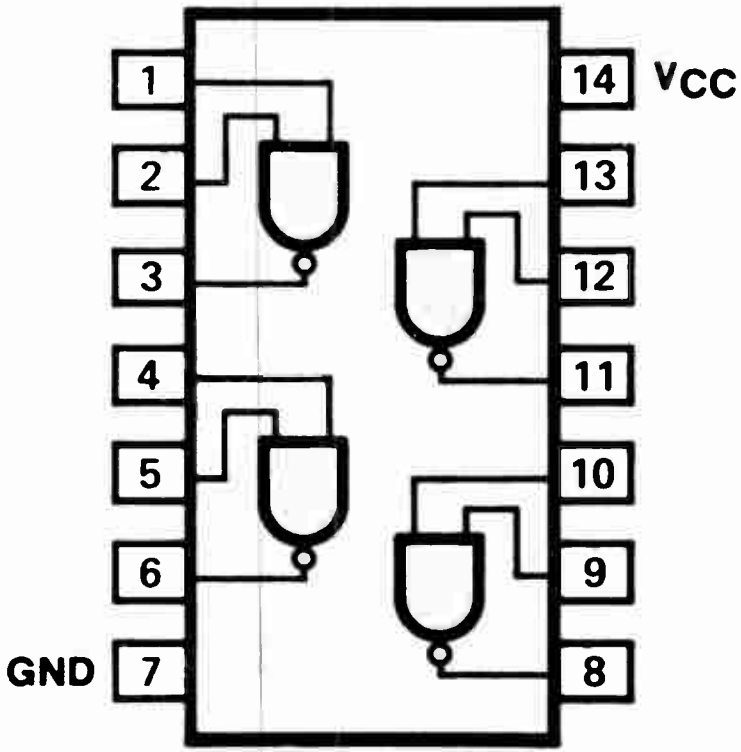


7433

7437 QUAD 2-INPUT NAND BUFFER

The NAND gate is a variation of the conventional AND gate, delivering an inverted (false) output when all inputs are true. The term AND is a contraction of NOT AND. Note that the output is true when either or both of the inputs are false. Essentially, a NAND gate is the result of using an active inverting element in the gate circuitry. As with a conventional AND gate, the NAND gate may have any number of inputs.

	74
Low-Level Output Current (mA)	48
High-Level Output Current (mA)	−1.2
Typ. Delay Time (ns)	10.5
Typ. Power Per Gate (mW)	27

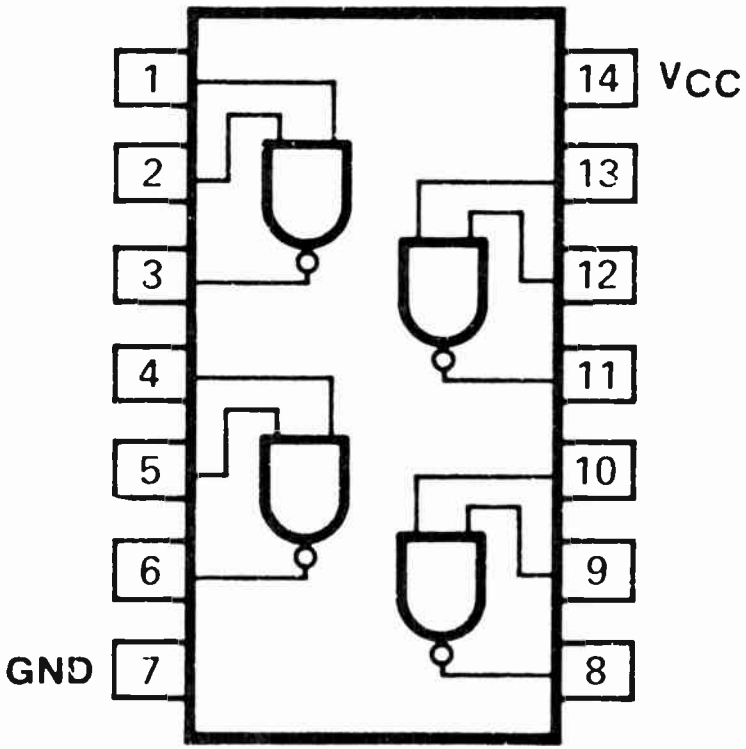


7437

7438 QUAD 2-INPUT NAND BUFFER (O.C.)

The NAND gate is a variation of the conventional AND gate, delivering an inverted (false) output when all inputs are true. The term AND is a contraction of NOT AND. Note that the output is true when either or both of the inputs are false. Essentially, a NAND gate is the result of using an active inverting element in the gate circuitry. As with a conventional AND gate, the NAND gate may have any number of inputs.

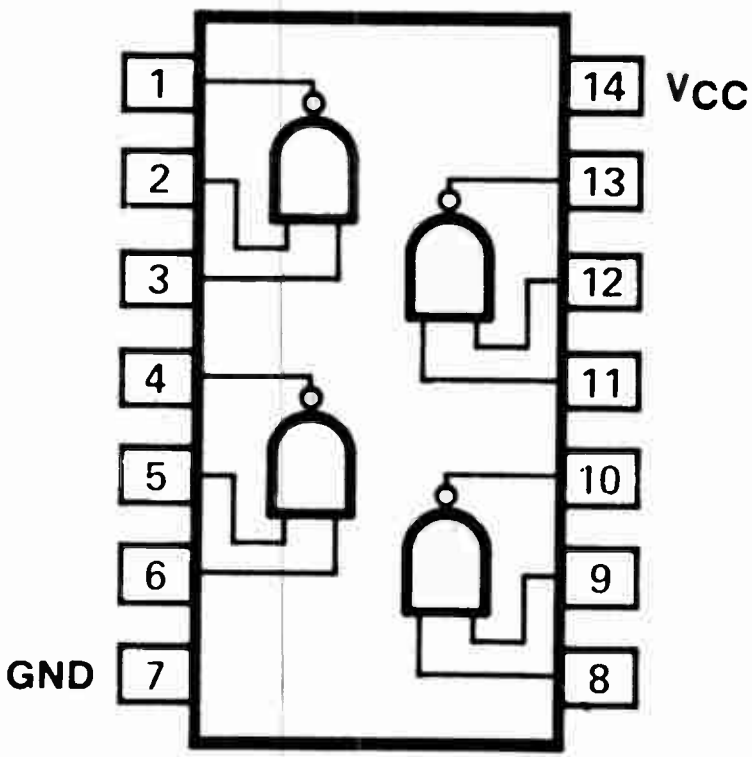
	74	74LS
High-Level Output Voltage (V)	5.5	5.5
Low-Level Output Current (mA)	48	24
Typ. Oelay Time (ns)	12.5	19
Typ. Power Per Gate (mW)	24.4	4.3



7438

7439 QUAD 2-INPUT NAND BUFFER (O.C.)

The NAND gate is a variation of the conventional AND gate, delivering an inverted (false) output when all inputs are true. The term AND is a contraction of NOT AND. Note that the output is true when either or both of the inputs are false. Essentially, a NAND gate is the result of using an active inverting element in the gate circuitry. As with a conventional AND gate, the NAND gate may have any number of inputs.

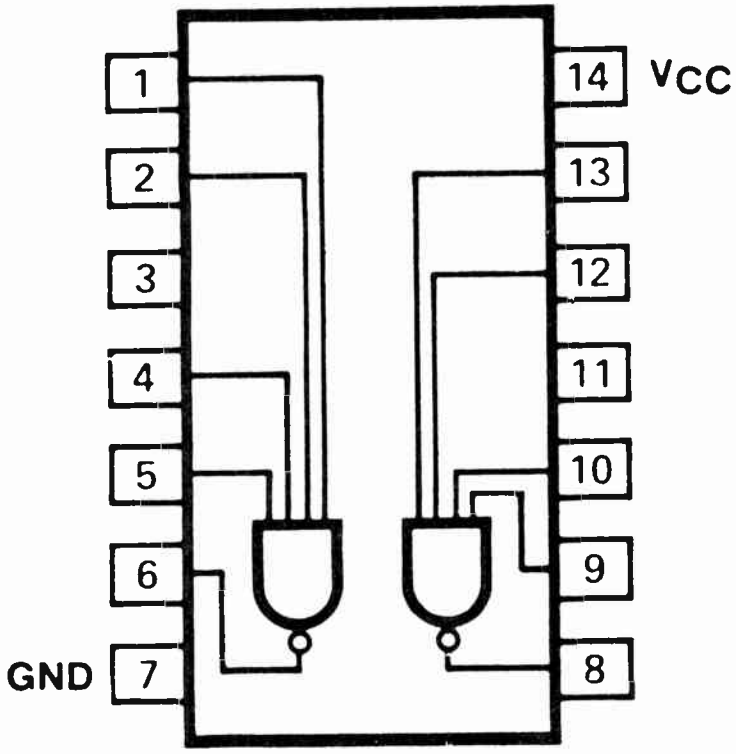


7439

7440 DUAL 4-INPUT NAND BUFFER

The NAND gate is a variation of the conventional AND gate, delivering an inverted (false) output when all inputs are true. The term AND is a contraction of NOT AND. Note that the output is true when either or both of the inputs are false. Essentially, a NAND gate is the result of using an active inverting element in the gate circuitry. As with a conventional AND gate, the NAND gate may have any number of inputs.

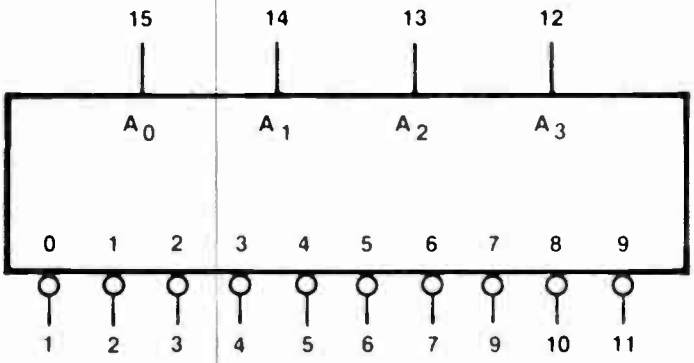
	74S	74H	74	74LS
Low-Level Output Current (mA)	60	60	48	24
High-Level Output Current (mA)	−3	−1.5	−1.2	−1.2
Typ. Delay Time (ns)	4	7.5	10.5	12
Typ. Power Per Gate (mW)	44	44	26	4.3



7440

The "42" decoder accepts four active HIGH BCD inputs and provides 10 mutually exclusive active LOW outputs, as shown by logic symbol. The active LOW outputs facilitate addressing other MSI units with active LOW input enables.

The logic design of the "42" ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs. The most significant input, A_3, produces a useful inhibit function when the "42" is used as a one-or-eight decoder. The A_3 input can also by used as the data input in an 8-output demultiplexer application.



Vcc = Pin 16
GND = Pin 8

7442

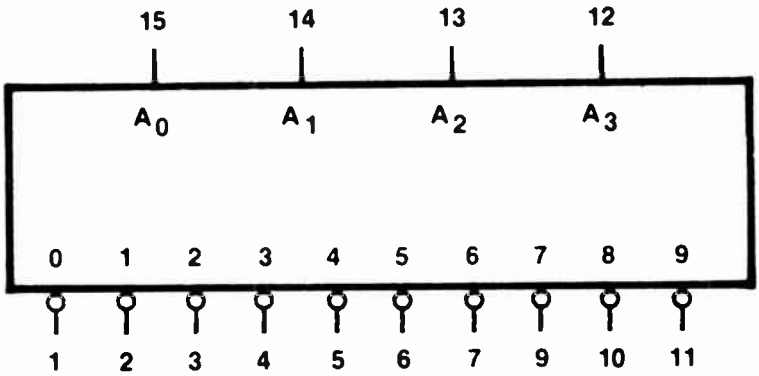
Truth Table

A_3	A_2	A_1	A_0	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

7442

7443 EXCESS-3-TO-DECIMAL DECODER

The "43" is an excess-3-to 1-of-10 decoder that accepts excess-3 coded inputs (binary range 3 through 12) and generates 10 mutually-exclusive active LOW outputs. The excess-3 code is used in decimal arithmetic because of its self-complementing feature (the bit-wise complement of a number is also the complement of the nine) which simplifies subtraction.



V_{CC} = Pin 16
GND = Pin 8

7443

Truth Table

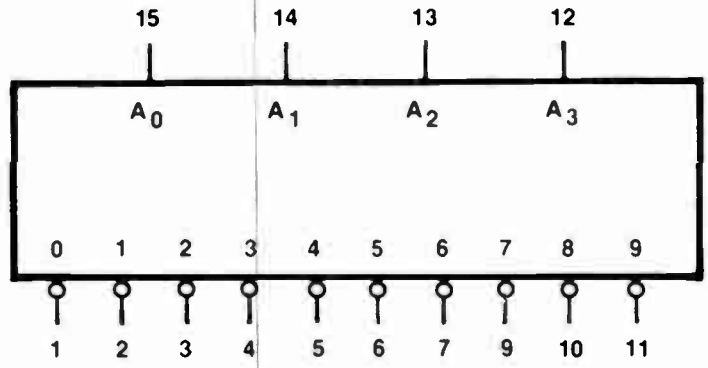
INPUTS				OUTPUTS									
A_3	A_2	A_1	A_0	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	H	H	L	H	H	H	H	H	H	H	H	H
L	H	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	H	H	H	L	H	H	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H	H	H
L	H	H	H	H	H	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	H	H	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	H	L	H	H
H	L	H	H	H	H	H	H	H	H	H	H	L	H
H	H	L	L	H	H	H	H	H	H	H	H	H	L
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage level

7443

7444 EXCESS-3-GRAY-TO-DECIMAL DECODER

The "44" is an excess-3-Gray code to 1-or-10 decoder that accepts excess-3 gray-coded inputs and generates 10 mutually exclusive active LOW outputs. The excess-3 gray code is used in decimal position encoders, because it retains the characteristics of a gray code (only one bit changes between adjacent states) even on the change between nine and zero.



V_{CC} = Pin 16
GND = Pin 8

7444

Truth Table

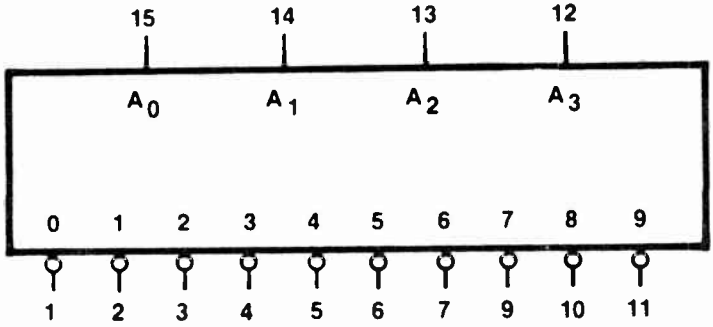
INPUTS				OUTPUTS									
A_3	A_2	A_1	A_0	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	H	L	L	H	H	H	H	H	H	H	H	H
L	H	H	L	H	L	H	H	H	H	H	H	H	H
L	H	H	H	H	H	L	H	H	H	H	H	H	H
L	H	L	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
H	H	L	L	H	H	H	H	H	L	H	H	H	H
H	H	L	H	H	H	H	H	H	H	L	H	H	H
H	H	H	H	H	H	H	H	H	H	H	L	H	H
H	H	H	L	H	H	H	H	H	H	H	H	L	H
H	L	H	L	H	H	H	H	H	H	H	H	H	L
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	L	H	H	H	H	H	H	H	H	H	H	H
H	L	L	L	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage level

7444

The "45" decoder accepts BCD on the A_0 to A_3 address lines and generates 10 mutually exclusive active LOW outputs. When an input code greater than nine is applied, all outputs are off. This device can therefore be used as a 1-of-8 decoder with A_3 used as an active LOW enable.

The "45" can sink 20 mA while maintaining the standardized guaranteed output LOW voltage (V_{OL}) of 0.4V, but it can sink up to 80 mA with a guaranteed V_{OL} of less than 0.9V. The "45" features an output breakdown voltage of 30V and is ideally suited as a lamp and solenoid driver.



V_{CC} = Pin 16
GND = Pin 8

7445

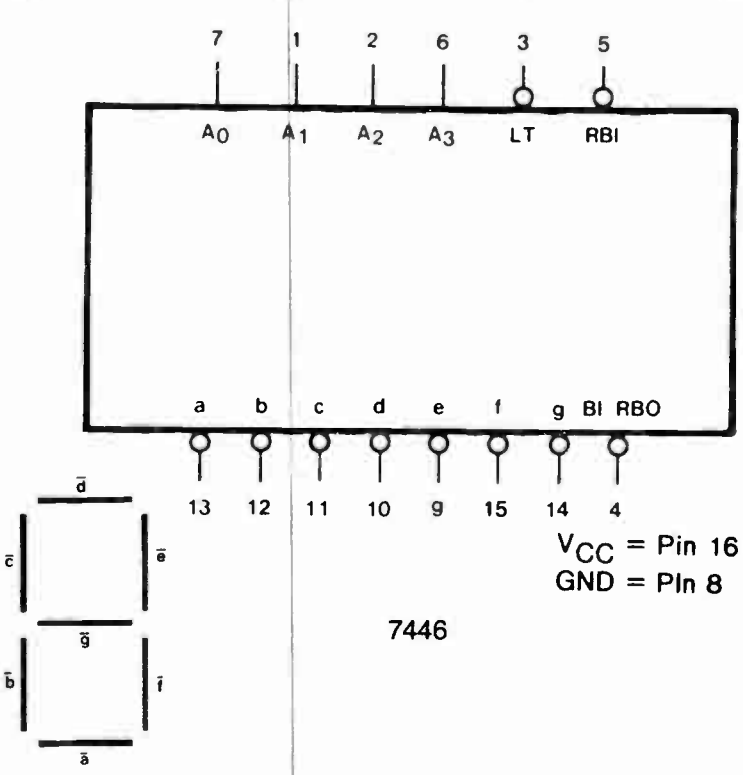
Truth Table

A_3	A_2	A_1	A_0	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

7445

The "46A" and "47A" 7-segment decoders accept a 4-bit BCD code input and produce the appropriate outputs for selection of segments in a 7-segment matrix display used for representing the decimal numbers 0-9. The 7 outputs ($\overline{a}$, $\overline{b}$, $\overline{c}$, $\overline{d}$, $\overline{e}$, $\overline{f}$, $\overline{g}$) of the decoder select the corresponding segments in the matrix shown in Figure A.

The "46A" and "47A" have provisions for automatic blanking of the leading and/or trailing edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an 8-digit mixed integer fraction decimal representation, using the automatic blanking capability, 0070.0500 would be displayed as 70.05. Leading edge zero suppression is obtained by connecting the ripple blanking output ($\overline{BI}/\overline{RBO}$) of a decoder to the



ripple blanking input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded, and because suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeroes.

The decoder has an active LOW input lamp test which overrides all other input combinations and enables a check to be made on possible display malfunctions. The $\overline{BI}/\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross-coupled pair of open collector gates.

DECIMAL OR FUNCTION	INPUTS							OUTPUTS						
	$\overline{LT}$	$\overline{RBI}$	A_3	A_2	A_1	A_0	$\overline{BI}/\overline{RBO}$(b)	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H
$\overline{BI}$(b)	X	X	X	X	X	X	L	H	H	H	H	H	H	H
$\overline{RBI}$(b)	H	L	L	L	L	L	L	H	H	H	H	H	H	H
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

The "48" 7-segment decoder accepts a 4-bit BCD code input and produces the appropriate outputs for selection of segments in a 7-segment matrix display used for representing the decimal numbers 0-9. The seven outputs (a,b,c,d,e,f,g) of the decoder select the corresponding segments in the matrix shown in Figure A.

The decoder has active HIGH outputs so a buffer transistor may be used directly to provide the high currents required for multiplexed LED displays. If additional base drive current is required external resistors may be added from the supply voltage to the 7-segment outputs of the decoders. The value of this resistor is constrained by the 6.4-mA current sinking capability of the output transistors of the circuit.

The "48" has provision for automatic blanking of the leading and/or trailing edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an eight-digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading edge zero suppression is obtained by connecting the ripple blanking output ($\overline{BI}/\overline{RBO}$) of a decoder to the ripple blanking input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded, and because suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeroes.

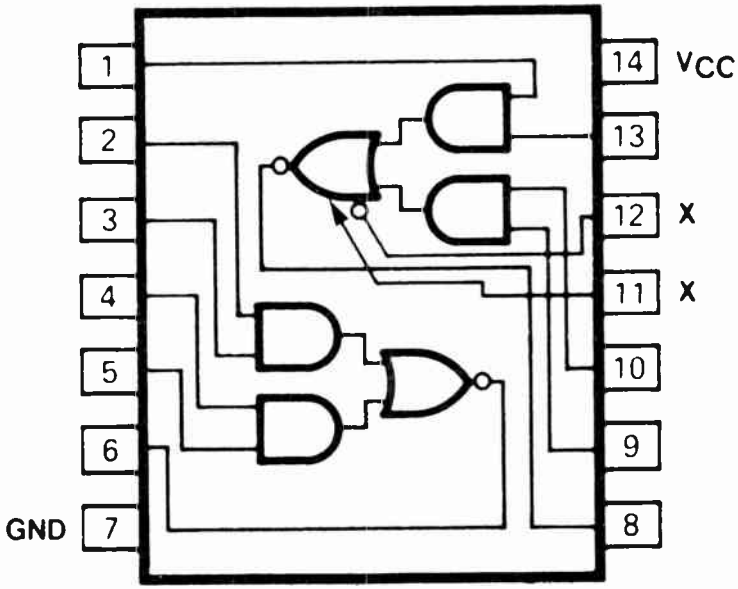
The decoder has an active LOW input lamp test which overrides all other input combinations and enables a check to be made on possible display malfunctions. The $\overline{BI}/\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross-coupled pair of open collector gates.

The symbol for the AND gate is shown here. By definition, for output C to be true, inputs A and B must by true; hence, the term AND gate.

Note symbol for the OR gate. By definition,for C to be true either input A or input B must be true, hence the name OR gate.

As logic elements are combined in series to perform logic functions, voltage levels tend to degrade. Thus, amplifiers are sometimes needed to restore voltages or currents to proper levels. Assuming no inversion is encountered, a true input will produce a true output, and a false input will produce a false output. When inversion occurs, an inversion circle is placed at the output, and the symbol is usually termed an inverter.

	74H	74
Typ. Delay Time (ns)	6.5	10.5
Typ. Power Gate (mW)	29	14



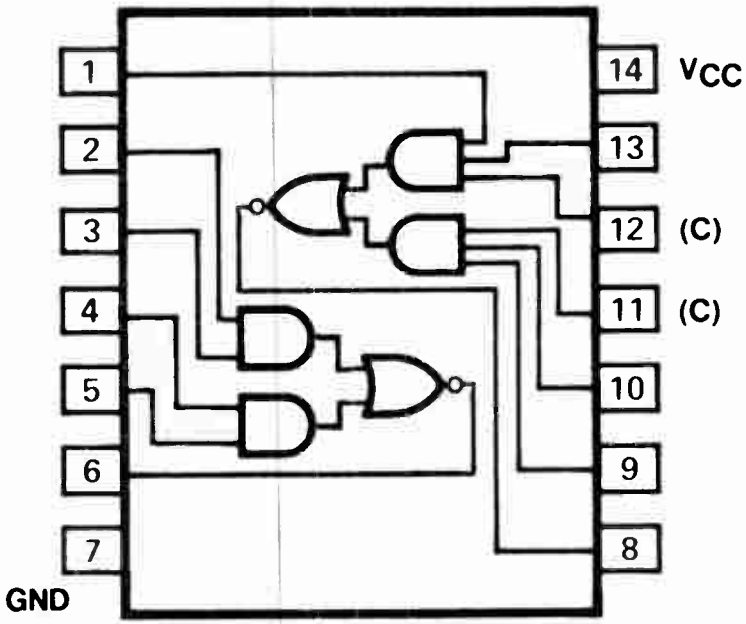
7450

The symbol for the AND gate is shown here. By definition, for output C to be true, inputs A and B must by true; hence, the term AND gate.

Note symbol for the OR gate. By definition,for C to be true either input A or input B must be true, hence the name OR gate.

As logic elements are combined in series to perform logic functions, voltage levels tend to degrade. Thus, amplifiers are sometimes needed to restore voltages or currents to proper levels. Assuming no inversion is encountered, a true input will produce a true output, and a false input will produce a false output. When inversion occurs, an inversion circle is placed at the output, and the symbol is usually termed an inverter.

	74S	74H	74	74LS	74L
Typ. Delay Time (ns)	3.5	6.5	10.5	12.5	43
Typ. Power Per Gate (mW)	28	29	14	2.75	1.5



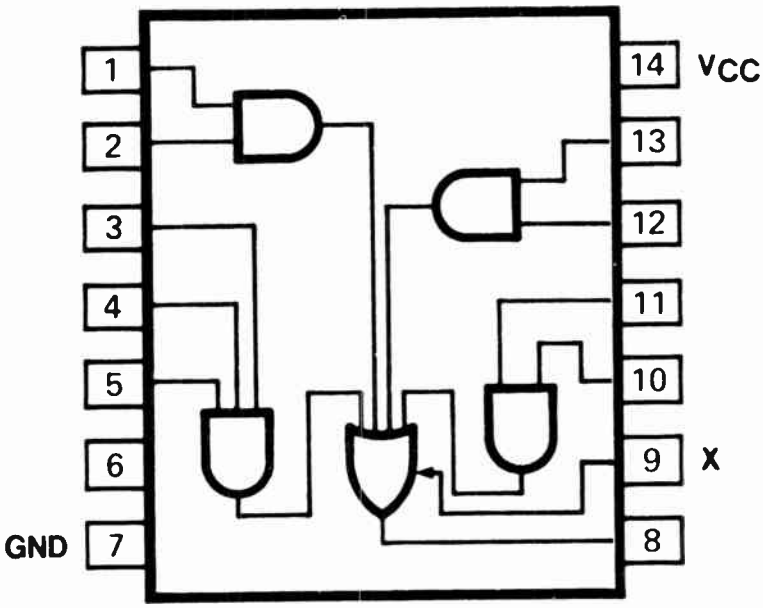
7451

7452 EXPANDABLE 2-2-2-3 AND-OR GATE

The symbol for the AND gate is shown below. By definition, for output C to be true, inputs A and B must be true; hence, the term AND gate.

Note the symbol for the OR gate. By definition, for C to be true, either input A or input B must be true; hence, the name OR gate.

	74H
Typ. Delay Time (ns)	9.9
Typ. Power Per Gate (mW)	88



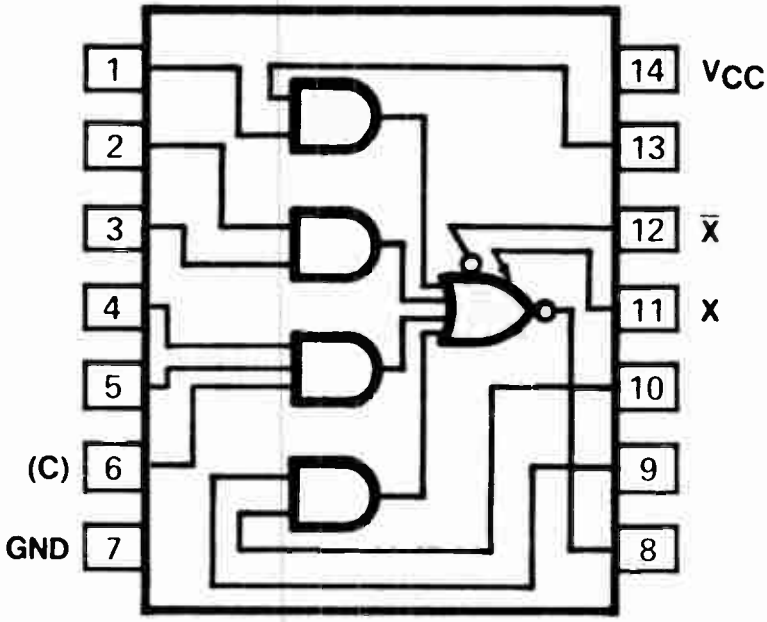
7452

The symbol for the AND gate is shown here. By definition, for output C to be true, inputs A and B must by true; hence, the term AND gate.

Note symbol for the OR gate. By definition,for C to be true either input A or input B must be true, hence the name OR gate.

As logic elements are combined in series to perform logic functions, voltage levels tend to degrade. Thus, amplifiers are sometimes needed to restore voltages or currents to proper levels. Assuming no inversion is encountered, a true input will produce a true output, and a false input will produce a false output. When inversion occurs, an inversion circle is placed at the output, and the symbol is usually termed an inverter.

	74H	74
Typ. Delay Time (ns)	6.6	10.5
Typ. Power Per Gate (mW)	41	23

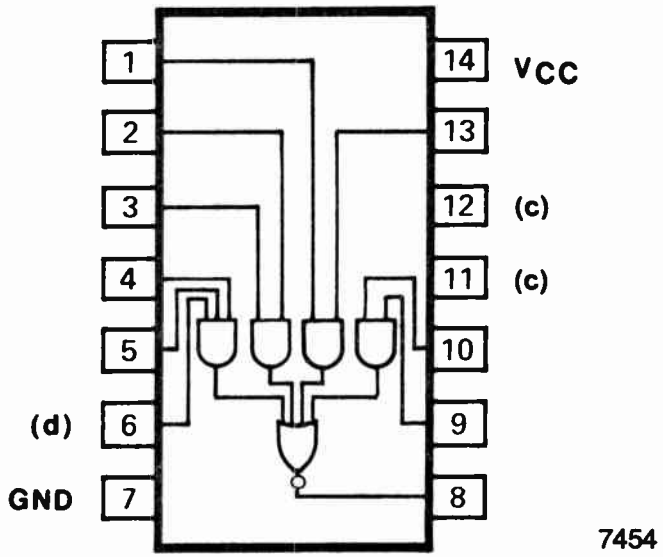


7453

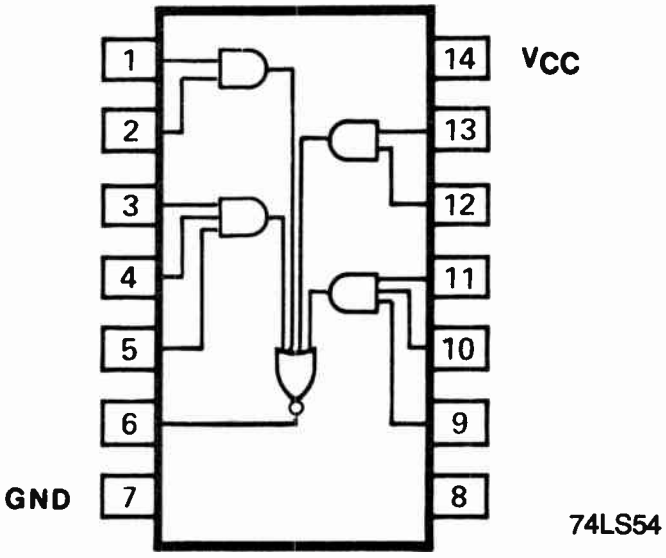
7454 4-WIDE 2 & 3-INPUT AND-OR-INVERT GATE

Refer to the description of the 7450.

	74H	74	74LS	74L
Typ. Delay Time (ns)	6.5	10.5	12.5	43
Typ. Power Per Gate (mW)	41	23	4.5	1.5



7454



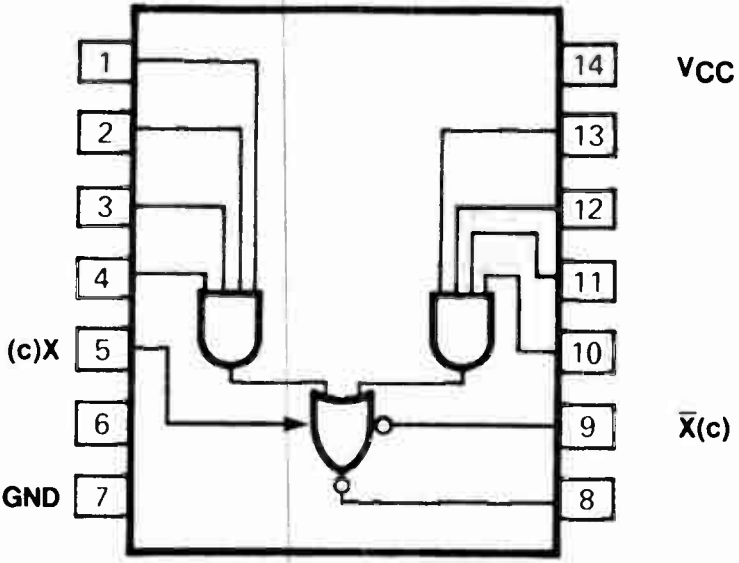
74LS54

The symbol for the AND gate is shown here. By definition, for output C to be true, inputs A and B must by true; hence, the term AND gate.

Note symbol for the OR gate. By definition,for C to be true either input A or input B must be true, hence the name OR gate.

As logic elements are combined in series to perform logic functions, voltage levels tend to degrade. Thus, amplifiers are sometimes needed to restore voltages or currents to proper levels. Assuming no inversion is encountered, a true input will produce a true output, and a false input will produce a false output. When inversion occurs, an inversion circle is placed at the output, and the symbol is usually termed an inverter.

Typ. Delay Time (ns)	**74H**	**74LS (Not Expandable)**
	6.8	12.5
Typ. Power Per Gate (mW)	30	2.75

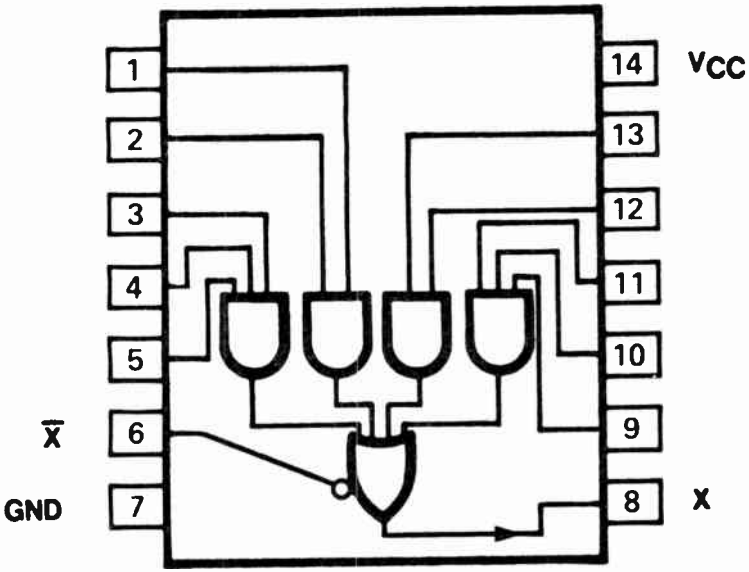


7455

The symbol for the AND gate is shown here. By definition, for output C to be true, inputs A and B must be true; hence, the term AND gate.

Note the symbol for the OR gate. By definition, for C to be true, either input A or input B must be true; hence, the name OR gate.

Type.	Power Per Gate	74H 25



7462

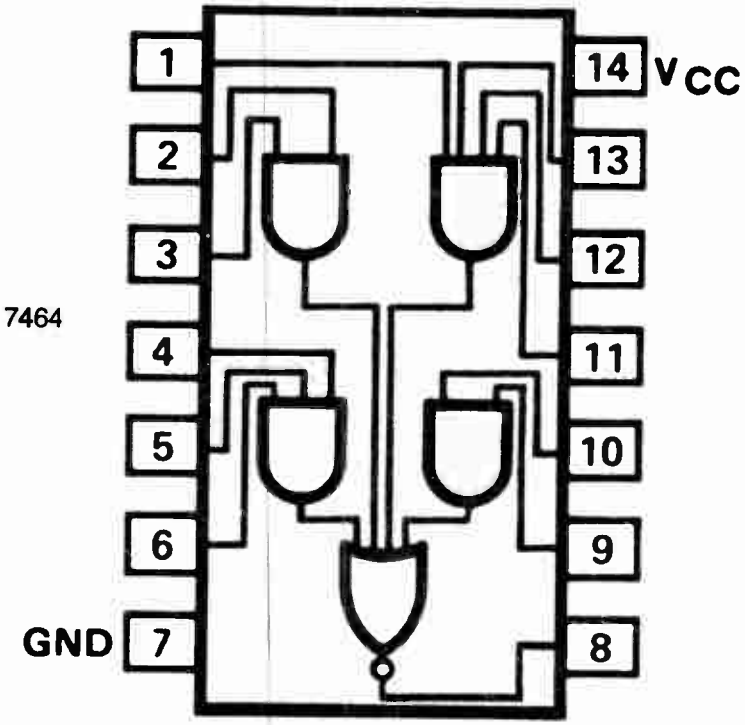
7464 4-2-3-2-INPUT AND-OR-INVERT GATE

The symbol for the AND gate is shown here. By definition, for output C to be true, inputs A and B must by true; hence, the term AND gate.

Note symbol for the OR gate. By definition,for C to be true either input A or input B must be true, hence the name OR gate.

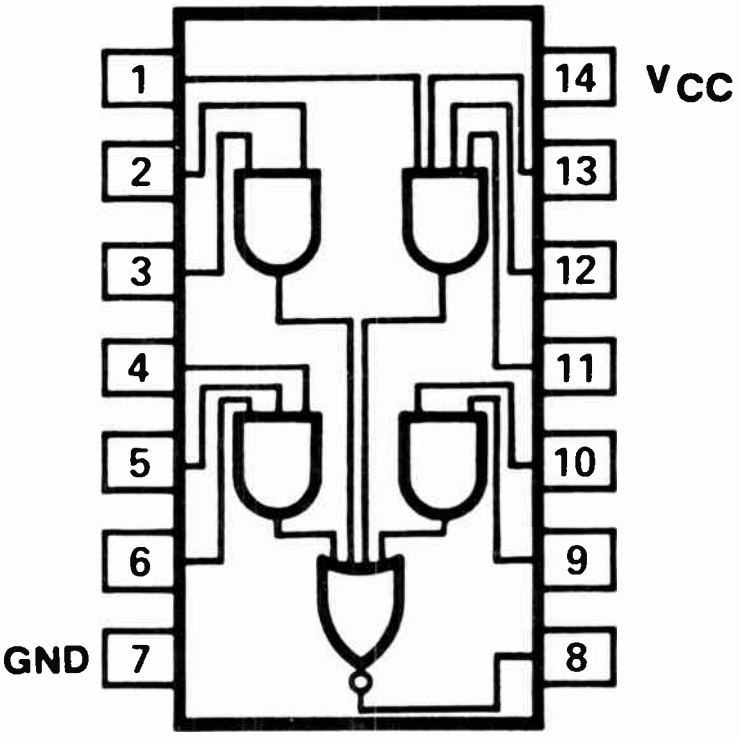
As logic elements are combined in series to perform logic functions, voltage levels tend to degrade. Thus, amplifiers are sometimes needed to restore voltages or currents to proper levels. Assuming no inversion is encountered, a true input will produce a true output, and a false input will produce a false output. When inversion occurs, an inversion circle is placed at the output, and the symbol is usually termed an inverter.

	74S	74H	74	74LS	74L
Typ. Delay Time (ns)	3.5	6.6	10.5	12.5	43
Typ. Power Per Gate (mW)	29	41	23	4.5	1.5



7465 4-2-3-2 INPUT AND-OR INVERT GATE (O.C.)

	74S
Typ. Delay Tiem (ns)	5.5
Typ. Power Per Gate (mW)	36



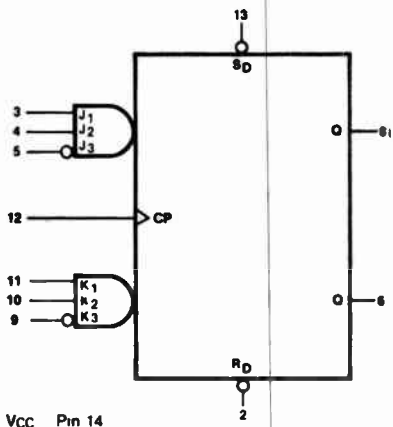
7465

7470 EDGE-TRIGGERED FLIP-FLOP

The 54/7470 is a positive edge-triggered J-K flip-flop featuring direct set and reset inputs and complementary outputs Q and $\overline{Q}$. Information is transferred to the outputs on the LOW-to-HIGH transition of the clock pulse. Multiple J and K inputs are provided to minimize gate requirements in state decoding applications.

The set ($\overline{S}_D$) and reset (R_D) are asynchronous active LOW inputs. When the clock is LOW, they override the data inputs forcing the outputs to their steady state level as shown in the truth table.

	74S
Typ. Max. Clock Frequency (MHz)	**35**
Typ. Power Per Flip-Flop (mW)	**65**



V_{CC} Pin 14
GND Pin 7

Pin numbers are for pin configuration "A

7470

Truth Table

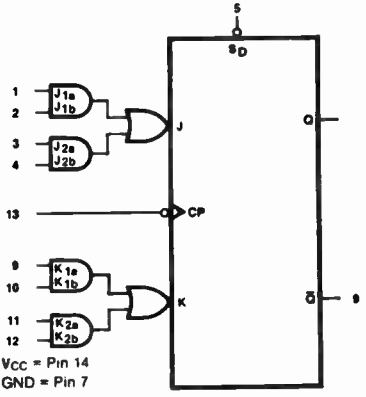
OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	J	K	Q	$\overline{Q}$
Asynchronous Set	L	H	L	X	X	H	L
Asynchronous Reset (Clear)	H	L	L	X	X	L	H
Undetermined [c]	L	L	X	X	X	L	L
Toggle	H	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	$\overline{q}$

J $J = J_2 \cdot \overline{J_3}$
K $K = K_2 \cdot \overline{K_3}$
H HIGH voltage level steady state
L LOW voltage level steady state
h HIGH voltage level one setup time prior to the LOW-to-HIGH Clock transition
l LOW voltage level one setup time prior to the LOW-to-HIGH Clock transition
X Don't care
q Lower case letters indicate the state of the referenced output prior to the LOW to HIGH Clock transition

The "71" is a positive pulse-triggered master slave flip-flop with AND-OR gated JK inputs and direct set ($\overline{S}_D$) input. JK information is loaded into the master while the clock is HIGH and transferred to the slave on the HIGH-to-LOW clock transition. The J and K inputs should be stable while the clock is HIGH for conventional operation. J or K input transitions for HIGH-to-LOW should be avoided while the clock is HIGH because of the feature of this flip-flop to catch ones.

The Set ($\overline{S}_D$) is an asynchronous active LOW input. When LOW, the $\overline{S}_D$ overrides the clock and the data inputs, forcing the Q output HIGH and the $\overline{Q}$ output LOW.

	74H	74L
Typ. Max. Clock Frequency (MHz)	30	6
A Typ. Power Per Flip-Flop (mW)	80	3.8
Setup Time (ns)	0	0
Held Time (ns)	0	0



Pin numbers are for pin configuration "A"

7471

Truth Table

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	X	X	X	H	L
Toggle	H	⎍	h	h	$\overline{q}$	q
Load "1" (Set)	H	⎍	h	l	H	L
Hold "no change"	H	⎍	l	l	q	$\overline{q}$

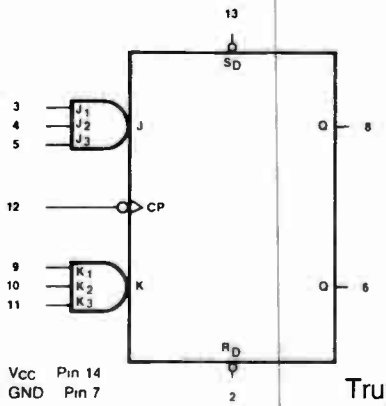
H = HIGH voltage level steady state
L = LOW voltage level steady state
h = HIGH voltage level prior to LOW-to-HIGH Clock transition [1]
l = LOW voltage level prior to LOW-to-HIGH Clock transition [1]
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the HIGH to LOW Clock transition
⎍ = Positive Clock pulse

7472 PULSE TRIGGERED FLIP-FLOP

The "72" is a positive pulse-triggered master slave flip-flop with gated JK inputs and direct set and reset inputs. JK information is loaded into the master while the clock is HIGH and transferred to the slave on the HIGH-to-LOW clock transition. The J and K inputs should be stable while the clock is HIGH for conventional operation. J or K input transitions from HIGH-to-LOW should be avoided while the clock is HIGH because of the feature of this flip-flop to catch ones.

The set ($\overline{S}_D$) and reset ($\overline{R}_D$) are asynchronous active LOW inputs. When LOW, they override the clock and data inputs, forcing the outputs to their steady state level, as shown in the truth table.

	74H	74	74L
Typ. Max. Clock Frequency (MHz)	30	20	6
Typ. Power Per Flip-Flop (mW)	80	50	3.8
Setup Time (ns)	0	0	0
Hold Time (ns)	0	0	0



7472

Truth Table

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (Note c)	L	L	X	X	X	H	H
Toggle	H	H	⎍	h	h	$\bar{q}$	q
Load "0" (Reset)	H	H	⎍	l	h	L	H
Load "1" (Set)	H	H	⎍	h	l	H	L
Hold "no change"	H	H	⎍	l	l	q	$\bar{q}$

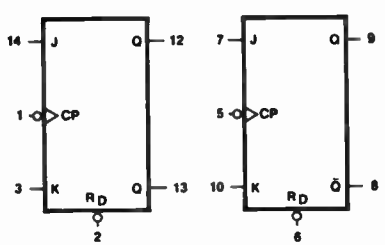
H HIGH voltage level steady state
L LOW voltage level steady state
h HIGH voltage level prior to LOW to HIGH Clock transition
l LOW voltage level prior to LOW to HIGH Clock transition
X Don't care
q Lower case letters indicate the state of the reference output prior to HIGH to LOW Clock transition
⎍ Positive Clock pulse

7473 DUAL JK FLIP-FLOP

The "73" is a dual flip-flop with individual JK, clock and direct reset inputs. The 7473 and 74H73 are positive pulse-triggered flip-flops. JK information is loaded into the master while the clock is high and transferred to the slave on the HIGH-to-LOW clock transition. For these devices, the J and K inputs should be stable while the clock is HIGH for conventional operation. The 74LS73 is a negative edge-triggered flip-flop. The J and K inputs must be stable one setup time prior to the HIGH-to-LOW Clock transition for predictable operation.

The Reset ($\overline{R}_D$) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the Q output LOW and the $\overline{Q}$ output high.

	74H	74	74L	74LS
Typ. Max. Clock Frequency (MHz)	**30**	**20**	**6**	**45**
Typ. Power Per Flip-Flop (mW)	**80**	**50**	**3.8**	**10**
Setup Time (ns)	**0**	**0**	**0**	**20**
Hold Time (ns)	**0**	**0**	**0**	**0**



7473

Vcc = Pin 4
GND = Pin 11

Truth Table

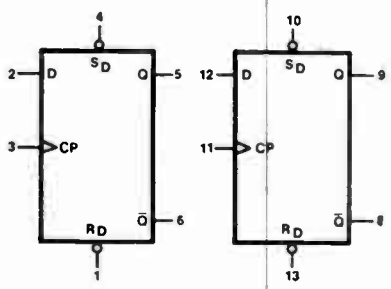
OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{R}_D$	$\overline{CP}$ (d)	J	K	Q	$\overline{Q}$
Asynchronous Reset (Clear)	L	X	X	X	L	H
Toggle	H	⎍	h	h	$\overline{q}$	q
Load "0" (Reset)	H	⎍	l	h	L	H
Load "1" (Set)	H	⎍	h	l	H	L
Hold "no change"	H	⎍	l	l	q	$\overline{q}$

H = HIGH voltage level steady state
L = LOW voltage level steady state
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition [c]
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition [c]
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the HIGH to LOW Clock transition
⎍ = Positive Clock pulse

7474 DUAL D-TYPE FLIP-FLOP

The "74" is a dual positive edge-triggered D-type flip-flop featuring individual data, clock, set and reset inputs and complementary Q and $\overline{Q}$ outputs. Set ($\overline{S}_D$) and reset ($\overline{R}_D$) are asynchronous active LOW inputs and operate independently of the clock input. Information on the data (D) input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one setup time prior to the LOW-to-HIGH clock transition for predictable operation. Although the clock input is level sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock to output delay time for reliable operation.

	74S	74H	74LS	74	74L
Typ. Max. Clock Frequency (MHz)	110	43	33	25	6
Typ. Power Per Flip-Flop (mW)	75	75	10	43	4
Setup Time (ns)	3	15	25	20	50
Hold Time (ns)	2	5	5	5	15



7474

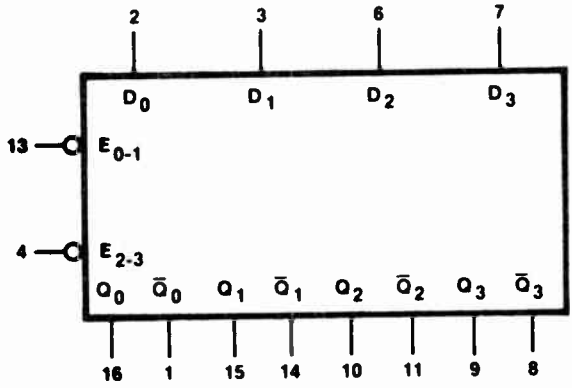
Truth Table

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	L	H
Undetermined (c)	L	L	X	X	H	H
Load "1" (Set)	H	H	↑	h	H	L
Load "0" (Reset)	H	H	↑	l	L	H

H = HIGH voltage level steady state
h = HIGH voltage level one setup time prior to the LOW to HIGH clock transition
L = LOW voltage level steady state
l = LOW voltage level one setup time prior to the LOW to HIGH clock transition
X = Don't care

7475 DUAL 2-BIT TRANSPARENT LATCH

The "75" has two independent 2-bit transparent latches. Each 2-bit latch is controlled by an active HIGH enable input (E). When E is HIGH, the data enters the latch and appears at the Q output. The Q outputs follow the data inputs as long as E is HIGH. The data (on the D) input one setup time before the HIGH-to-LOW transition of the enable will be stored in the latch. The latched outputs remain stable as long as the enable is LOW.



V_{CC} = Pin 5
GND = Pin 12

7475

MODE SELECT FUNCTION TABLE

OPERATING MODE	INPUTS		OUTPUTS	
	E	D	Q	$\bar{Q}$
Data Enabled	H	L	L	H
	H	H	H	L
Data Latched	L	X	q	$\bar{q}$

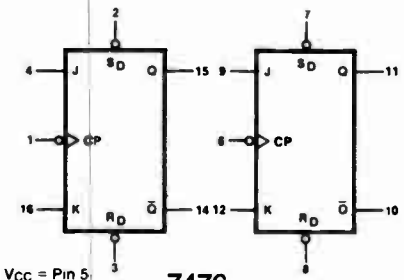
H = HIGH voltage level
L = LOW voltage level
X = Don't care
q = Lower case letters indicate the state of referenced output one setup time prior to the HIGH-to-LOW Enable transition.

7476 DUAL JK FLIP-FLOP

The "76" is a dual JK flip-flop with individual J, K, clock, set and reset inputs. The 7476 and 74H76 are positive pulse-triggered flip-flops. JK information is loaded into the master while the clock is HIGH and transferred to the slave on the HIGH-to-LOW clock transition. The J and K inputs must be stable while the clock is HIGH for conventional operation.

The 74LS76 is a negative edge-triggered flip-flop. The J and K inputs must be stable only one setup time prior to the HIGH-to-LOW clock transition. The set ($\overline{S}_D$) and reset ($\overline{R}_D$) are asynchronous active LOW inputs. When LOW, they override the clock and data inputs forcing the outputs to the steady state levels as shown in the truth table.

	74H	74	74LS
Typ. Max. Clock Frequency (MHz)	30	20	45
Typ. Power Per Flip-Flop (mW)	80	50	10
Setup Time (ns)	0	0	20
Hold Time (ns)	0	0	0



Truth Table

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$ (d)	J	K	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (c)	L	L	X	X	X	H	H
Toggle	H	H	⎍	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	⎍	l	h	L	H
Load "1" (Set)	H	H	⎍	h	l	H	L
Hold "no change"	H	H	⎍	l	l	q	$\overline{q}$

H = HIGH voltage level steady state
L = LOW voltage level steady state
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition (d)
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition (d)
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the HIGH to LOW Clock transition
⎍ = Positive Clock pulse

The "77" has two independent 2-bit transparent latches. Each 2-bit latch is controlled by an active HIGH enable input (E). When E is HIGH, the data enters the latch and appears at the Q output. The Q outputs follow the data inputs as long as E is HIGH. The data (on the D) input one setup time before the HIGH-to-LOW transition of the enable will be stored in the latch. The latched outputs remain stable as long as the enable is LOW.

MODE SELECT FUNCTION TABLE

OPERATING MODE	INPUTS		OUTPUTS
	E	D	Q
Data Enabled	H H	L H	L H
Data Latched	L	X	q

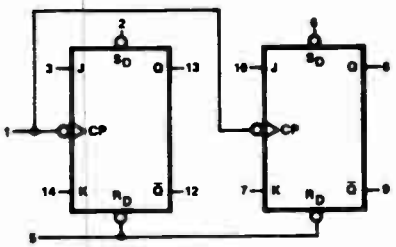
H = HIGH voltage level
L = LOW voltage level
X = Don't care
q = Lower case letters indicate the state of referenced output one setup time prior to the HIGH-to-LOW Enable transition.

7477

7478 DUAL JK EDGE-TRIGGERED FLIP-FLOP

The "78" is a dual JK negative edge-triggered flip-flop featuring individual J, K, set, common clock and common reset inputs. The set ($\overline{S}_D$) and reset ($\overline{R}_D$) inputs, when LOW, set or reset the outputs as shown in the truth table, regardless of the levels at the other inputs. A HIGH level on the clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is HIGH and the flip-flop will perform according to the truth table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

	74H	74L	74LS
Typ. Max. Clock Frequency (MHz)	30	6	45
Typ. Power Per Flip-Flop (mW)	80	3.8	10
Setup Time (ns)	0	0	20
Hold Time (ns)	0	0	0



V_{CC} = Pin 4
GND = Pin 11

7478

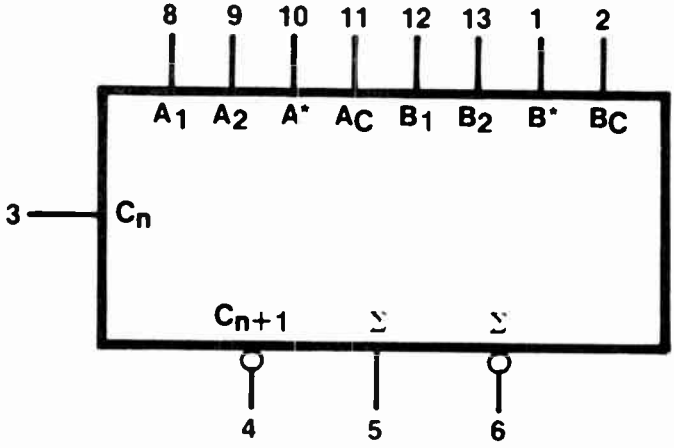
Truth Table

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined [c]	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level steady state
h = HIGH voltage level one setup time prior to the HIGH to LOW Clock transition
L = LOW voltage level steady state
l = LOW voltage level one setup time prior to the HIGH to LOW Clock transition
q = Lower case letters indicate the state of the referenced output prior to the HIGH to LOW Clock transition
X = Don't care

7480 GATED FULL ADDER

The "80" is a single-bit, high-speed, binary full adder with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output. It is designed for medium and high speed, multiple-bit, parallel-add/serial-carry applications. The circuit utilizes DTL for the gated inputs and high-speed, high fanout TTL for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive *lookahead* and carry-cascading circuits.



V_{CC} = Pin 14
GND = Pin 7

7480

Truth Table

INPUTS			OUTPUTS		
C_n	B	A	$\overline{C_{n+1}}$	Σ	Σ
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	L	L
H	L	L	H	H	H
H	L	H	L	L	L
H	H	L	L	H	L
H	H	H	L	L	H

H = HIGH voltage level
L = LOW voltage level

NOTES

b. $A = \overline{A_1 + A_2}$; $B = \overline{B_1 + B_2}$ where $A^* = \overline{A_1 + A_2 + A_C}$; $B^* = \overline{B_1 + B_2}$

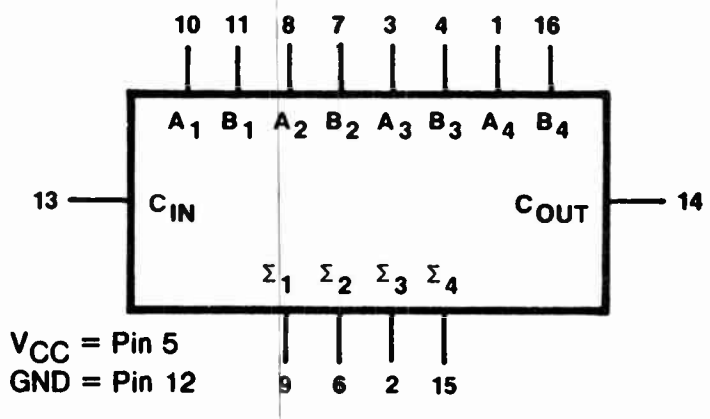
c. When A* or B* are used as inputs, A_1 and A_2 or B_1 and B_2 respectively must be connected to GND

d. When A_1 and A_2 or B_1 and B_2 are used as inputs, A* or B* respectively must be open or used to perform Dot-OR logic

The "83" is a high speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bin binary words ($A_1 - A_4$, $B_1 - B_4$) and a Carry input (C_{IN}). The sum of the two 4-bit words is combined with the carry input and presented at the four Sum outputs ($\sum 1 - \sum 4$) and the carry output (C_{OUT}). It operates with either HIGH or LOW operands (positive or negative logic).

Because of the symmetry of the binary add function the "83" can be used with either all active HIGH operands (positive logic) or with all active LOW operands (negative logic). With active HIGH inputs, C_{IN} cannot be left open; instead, it must be held LOW when no carry in is intended. Interchanging the inputs of equal weight does not affect the operation, so C_{IN}, A_1 and B_1 can arbitrarily be assigned to pins 10, 11, 13, etc.

	74LS	74
Typ. Carry Time (ns)	10	10
Typ. Add Time (ns)	15	16
Typ. Power Per Bit (mW)	24	76



PINS	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

(10+9=19)
(carry+5+6=12)

7485 4-BIT MAGNITUDE COMPARATOR

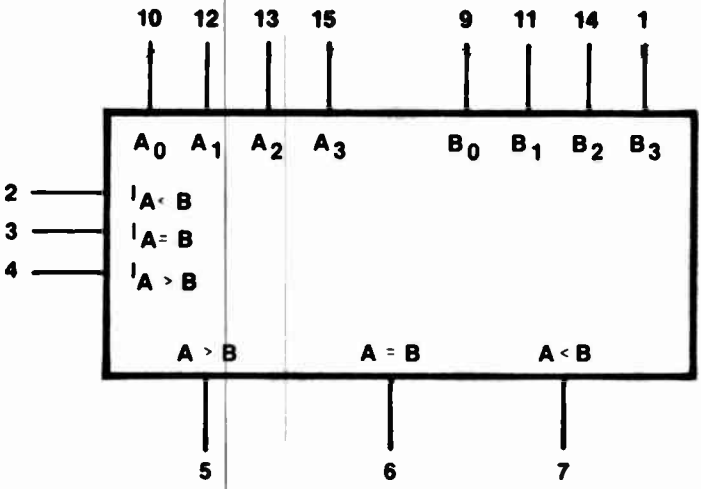
The "85" is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted ($A_0 \rightarrow A_3$) and ($B_0 \rightarrow B_3$), where A_3 and B_3 are the most significant bits.

The operation of the "85" is described in the truth table showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table, the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme.

The expansion inputs $1_{A>B}$, $1_{A=B}$ and $1_{A<B}$ are the least significant bit positions. When used for series expansion, the $A > B$, $A = B$ and $A < B$ outputs of the least significant word are connected to the corresponding $1_{A>B}$, $1_{A=B}$ and $1_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15 ns is added with each additional stage. For proper operation, the expansion inputs of the least significant word should be tied as follows: $1_{A>B}$ = HIGH, $1_{A=B}$ = LOW and $1_{A<B}$ = HIGH.

The parallel expansion scheme shown in Figure A demonstrates the most efficient general use of these comparators. In the parallel expansion scheme, the expansion inputs can be used as a fifth input bit position except on the least significant device which must be connected as in the serial scheme. The expansion inputs are used by labeling $1_{A>B}$ as an A input, $1_{A<B}$ as a B input and setting $1_{A=B}$ LOW. The "85" can be used as a 5-bit comparator only when the outputs are used to drive the (A_0–A_3) and (B_0–B_3) inputs of another "85" device. The parallel technique can be expanded to any number of bits as shown in the table.

	74	74L
Typ. Compare Time (ns)	21	70
Typ. Total Power (mW)	275	20



V_{CC} = Pin 16
GND = Pin 8

7485

Truth Table

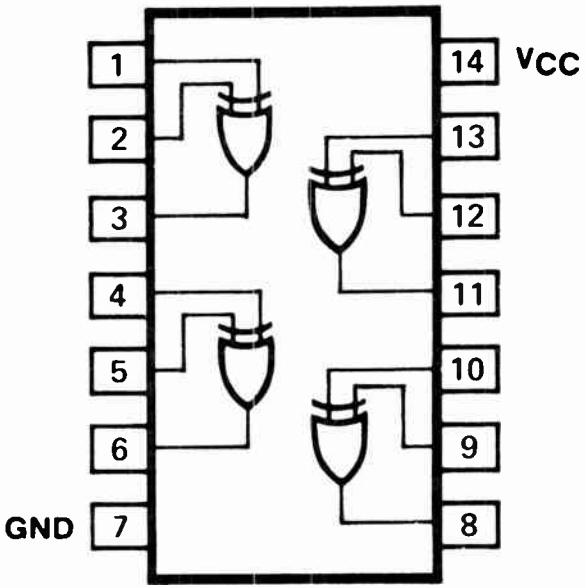
COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A>B	A<B	A=B
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

H = HIGH voltage level X = Don't care
L = LOW voltage level

7485

7486 QUAD 2-INPUT EXCLUSIVE-OR GATE

	74S	74LS	74	74L
Typ. Delay Time (ns)	7	10	14	29
Typ. Total Power (mW)	250	30	150	15



7486

Truth Table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

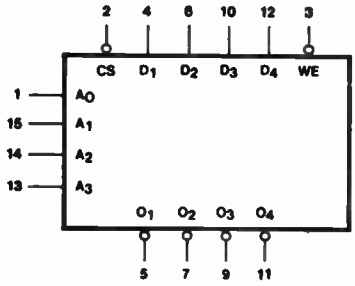
L = LOW voltage level
H = HIGH voltage level

7486

The "89" is a high-speed array of 64 memory cells organized as 16 words of four bits each. A one-of-16 address decoder selects a single word which is specified by the four address inputs ($A_0 - A_3$). A READ operation is initiated after the address lines are stable when the write enable ($\overline{WE}$) input is HIGH and the chip select-memory enable ($\overline{CS}$) input is LOW. Data is read at the outputs inverted from the data that were written into the memory.

A WRITE operation requires that the $\overline{WE}$ and $\overline{CS}$ inputs be LOW. The address inputs must be stable during the WRITE mode for predictable operation. When the write mode is selected the outputs are the complement of the data inputs. The selected memory cells are transparent to changes in the data during the WRITE mode. Therefore, data must be stable one setup time before the LOW-to-HIGH transition of $\overline{CE}$ or $\overline{WE}$.

	74
Read Time (ns)	33
Write Time (ns)	48
Current Per Package (mA)	75



V_{CC} = Pin 16
GND = Pin 8

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{CS}$	$\overline{WE}$	D_n	$\overline{O}_n$
Write	L L	L L	L H	H L
Read	L	H	X	$\overline{Data}$
Inhibit Writing	H H	L L	L H	H L
Store-Diaable Outputs	H	H	X	H

7489

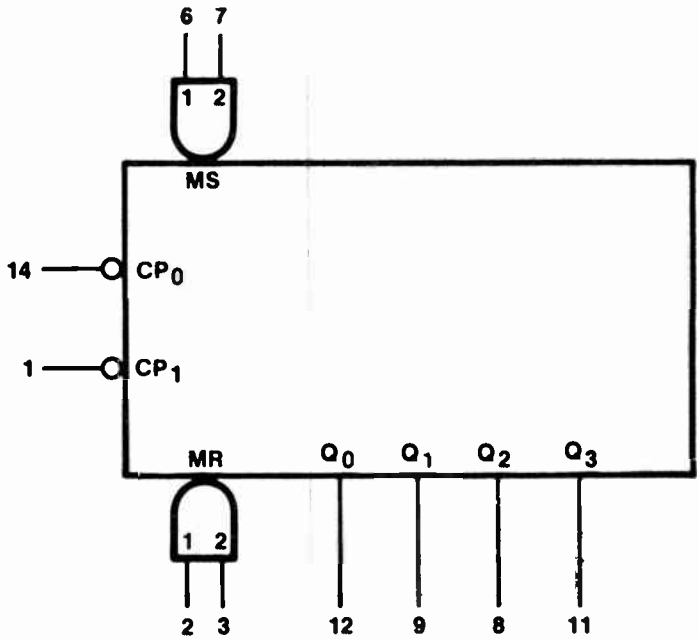
7490 DECADE COUNTER

The "90" is a 4-bit ripple type decade counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therfore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output is designed and specified to drive the rate fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous master reset ($MR_1 \cdot MR_2$) is provided which overrides both clock and resets (clears) all the flip-flops. Also provided is a gated AND asynchronous master set ($MS_1 \cdot MS_2$) which overrides the clocks and the MR inputs, setting the outputs to nine (HLLH).

Because the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a BCD (8421) counter, the $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count, producing a BCD count sequence. In a symmetrical BIquinary divide-by-10 counter, the Q_3 output must be connected externally to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input, and a divide-by-10 square wave is obtained at output Q_0. To operate as a divide-by-two and a divide-by-five counter, no external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain divide-by-five operation at the Q_3 output.

	74LS	74	74L
Count Frequency (MHz)	32	32	6
Parallel Load	set to 9	set to 9	set to 9
Clear	High	High	High
Typ. Total Power (mW)	40	160	20



Vcc = Pin 5
GND = Pin 10

Truth Table

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 connected to input $\overline{CP}_1$

Truth Table

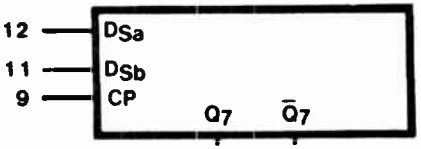
RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

H = HIGH voltage level
L = LOW voltage level
X = Don't care

7490

The "91" is an 8-bit serial-in-serial-out shift register. The serial data are entered through a 2-input AND gate (D_{sa} and D_{sb}). HIGH data are entered when both D_{sa} and D_{sb} are HIGH. LOW data are entered when either serial data input is LOW. The data inputs are edge-triggered and must be stable just one setup time prior to the LOW-to-HIGH transition of the clock input (CP) for predictable operation. The data is shifted one bit to the right ($Q_0 \rightarrow Q_2 \rightarrow Q_7$) synchronous with each LOW-to-HIGH clock transition. The "91" has no reset capacity, so initialization requires the shifting in of at least eight bits of known data. Once the register is fully loaded, the Q output follows the serial inputs delayed by eight clock pulses. The complement ($\overline{Q}$) output from the last stage is also available for simpler decoding applications.

	74	74L
Shift Frequency (MHz)	10	4
Serial Data Input	Gated D	Gated D
Asynchronous Clear	None	None
Shift-Right Mode	Yes	Yes
Shift-Left Mode	No	No
Load Mode	No	No
Hold Mode	No	No
Tup. Total Power (mW)	175	17.5



V_{CC} = Pin 5
GND = Pin 10
Pin numbers for DIP package

Truth Table

OPERATING MODE	INPUTS			First Stage		OUTPUTS	
	CP	D_{Sa}	D_{Sb}	Q_0	$\overline{Q}_0$	Q_7	$\overline{Q}_7$
Shift, reset first stage	↑	l	X	L	H	q_6	$\overline{q}_6$
	↑	X	l	L	H	q_6	$\overline{q}_6$
Shift, set first stage	↑	h	h	H	L	q_6	$\overline{q}_6$

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
q_n = Lower case letters indicate the state of the referenced register output one setup time prior to the LOW-to-HIGH clock transition
X = Don't care
↑ = LOW-to-HIGH clock transition

7492 DIVIDE-BY-TWELVE COUNTER

The "92" is a 4-bit ripple type divide-by-12 Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-six section. Each section has a separate clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output is designed and specified to drive the rated fanout plus the $\overline{CP}_1$ input of the device. A gated AND asynchronous master reset ($MR_1 \cdot MR_2$) is provided which overrides both clocks and resets (clears) all the flip-flops.

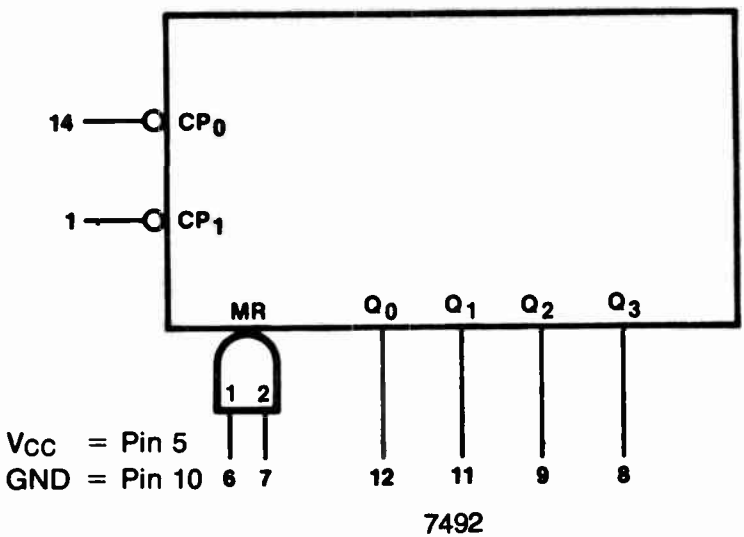
Because the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a modulo-12, divide-by-12 counter, the $\overline{CP}_1$ input must be externally connected to Q_0 output. The $\overline{CP}_0$ input receives the incoming count, and Q_3 produces a symmetrical divide-by-12 square wave output. In a divide-by-six counter, no external connections are required. The first flip-flop is used as a binary element for the divide-by-two function. The $\overline{CP}_1$ input is used to obtain divide-by-three operation at the Q_1 and Q_2 outputs and divide-by-six operation at the Q_3 output.

	74LS	74
Count Frequency (MHz)	32	32
Parallel Lead	None	None
Clear	High	High
Typ. Total Power (mW)	39	160

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH voltage level
L = LOW voltage level
X = Don't care



7492

Truth Table

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

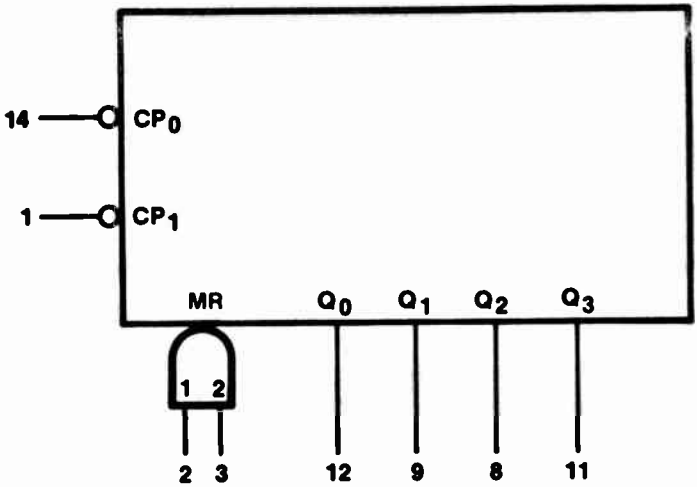
NOTE: Output Q_0 connected to Input $\overline{CP_1}$.

7493 4-BIT BINARY RIPPLE COUNTER

The "93" is a 4-bit ripple type binary counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output is designed and specified to drive the rated fanout plus the $\overline{CP}_1$ input of the device. A gated AND asynchronous master reset ($MR_1 \cdot MR_2$) is provided which overrides both clocks and resets (clears) all the flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a 4-bit ripple counter, the output Q_0 must be connected externally to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8 and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs, as shown in the truth table. As a 3-bit ripple counter, the input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_1, Q_2 and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

	74LS	74	74L
Count Frequency (MHz)	32	32	6
Parrallel Load	None	None	None
Clear	High	High	High
Typ. Total Power (mW)	39	160	20



Vcc = Pin 5
GND = Pin 11

7493

MODE SELECTION

7493

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH voltage level
L = LOW voltage level
X = Don't care

Truth Table

7493

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

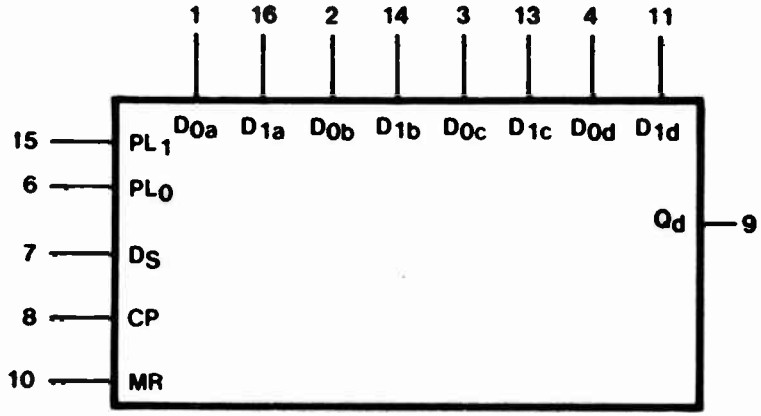
NOTE: Output Q_0 connected to input $\overline{CP}_1$.

7494 4-BIT SHIFT REGISTER

The "94" is a 4-bit shift register with serial and parallel (ones transfer) data entry. To facilitate parallel ones transfer from two sources, two Parallel Load inputs (PL_0 and PL_1) with associated parallel data inputs ($D_{0a} - D_{0d}$ and $D_{1a} - D_{1d}$) are provided. To accommodate these extra inputs only the output of the last stage is available. The asynchronous master reset (MR) is active HIGH. When MR is HIGH, it overrides the clock and clears the register, forcing Q_d LOW.

Four flip-flops are connected so that shifting is synchronous; they change state when the clock goes from LOW-to-HIGH. Data is accepted at the serial D_s input prior to this clock transition. The two parallel load inputs and parallel data inputs allow an asynchronous ones transfer from two sources. The flip-flops can be set independently to the HIGH state when the appropriate parallel input is activated. Parallel inputs D_{0a} through D_{0d} are activated during the time the PL_0 is HIGH and Parallel inputs D_{1a} through D_{1d} are activated when PL_1 is HIGH. If both sets of inputs are activated, a HIGH on either input will set the flip-flops to a HIGH. The register should not be clocked while the parallel data inputs are activated. The Parallel Load and parallel data inputs will override the MR if both are activated simultaneously. However, for predictable operation, both signals should not be deactivated simultaneously.

	74
Max. Supply Current (mA)	58
Max. Clock Frequency (MHz)	10



V_{CC} = Pin 5
GND = Pin 12

7494

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS			
	PL_0	PL_1	D_{0n}	D_{1n}	MR	CP	D_S	Q_a	Q_b	Q_c	Q_d
Parallel Load	H	L	L	X	X	X	X	Q_a	Q_b	Q_c	Q_d
	H	L	H	X	X	X	X	H	H	H	H
	L	H	X	L	X	X	X	Q_a	Q_b	Q_c	Q_d
	L	H	X	H	X	X	X	H	H	H	H
Reset (clear)	L	L	X	X	H	X	X	L	L	L	L
Shift right	L	L	X	X	L	↑	l	L	q_a	q_b	q_c
	L	L	X	X	L	↑	h	H	q_a	q_b	q_c

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
q_n = Lowar case letters indicate the state of the referenced output one setup time prior to the LOW-to-HIGH clock transition
x = Don't care
↑ = LOW-to-HIGH clock transition

7494

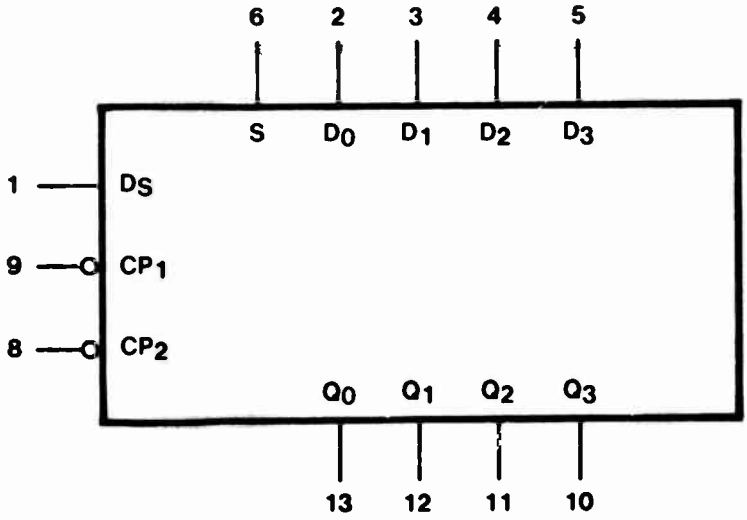
7495 4-BIT SHIFT REGISTER

The "95" is a 4-bit Shift Register with serial and parallel synchronous operation modes. It has a serial data (D_S) and four parallel data ($D_0 - D_3$) inputs and four parallel outputs ($Q_0 - Q_3$). The serial or parallel mode of operation is controlled by a mode select input (S) and two clock inputs ($\overline{CP}_1$ and $\overline{CP}_2$). The serial (shift right) or parallel data transfers occur synchronously with the HIGH-to-LOW transition of the selected clock input.

When the mode select input (S) is HIGH, $\overline{CP}_2$ is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}_2$ loads parallel data from the $D_0 - D_3$ inputs into the register. When S is LOW, $\overline{CP}_1$ is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}_1$ shifts the data from serial input D_S to Q_0 and transfers the data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3, respectively (shift right). Shift left is accomplished by externally connecting Q_3 to D_2, Q_2 to D_1, Q_1 to D_0 and operating the "95" in the parallel mode (S=HIGH).

In normal operations the mode select (S) should change states only when both clock inputs are LOW. However, changing S from HIGH-to-LOW while $\overline{CP}_2$ is LOW, or changing S from LOW-to-HIGH while $\overline{CP}_1$ is LOW will not cause any changes on the register outputs.

	74	74LS	74L
Shift Frequency (MHz)	25	25	6
Serial Data Input	D	D	D
Asynchronous Clear	None	None	None
Shift-Right Mode	Yes	Yes	Yes
Shift-Left Mode	No	No	No
Lead Mode	Yes	Yes	Yes
Hold Mode	No	No	No
Typ. Total Power (mW)	195	65	24



V_{CC} = Pin 14
GND = Pin 7

7495

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	S	$\overline{CP}_1$	$\overline{CP}_2$	D_S	D_n	Q_0	Q_1	Q_2	Q_3
Parellel Load	H	X	↓	X	l	L	L	L	L
	H	X	↓	X	h	H	H	H	H
Shift right	L	↓	X	l	X	L	q_0	q_1	q_2
	L	↓	X	h	X	H	q_0	q_1	q_2
Mode change	↑	L	X	X	X	no change			
	↑	H	X	X	X	undetermined			
	↓	X	L	X	X	no change			
	↓	X	H	X	X	undetermined			

H = HIGH voltage level steady state
L = LOW voltage level steady state
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition
l = LOW voltage level one setup tie prior to the HIGH-to-LOW Clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition
↓ = HIGH-to-LOW transition of Clock or mode Select
↑ = LOW-to-HIGH transition of mode Select.

7495

7496 5-BIT SHIFT REGISTER

The "96" is a 5-bit shift register with both serial and parallel (ones transfer) data entry. Because the "96" has the output of each stage available as well as a D-type serial input and ones transfer inputs on each stage, it can be used in 5-bit serial-to-parallel, serial-to-serial and some parallel-to-serial data operations.

The "96" is five master/slave flip-flops connected to perform right shift. The flip-flops change state on the LOW-to-HIGH transition of the clock. The serial data (D_S) input is edge-triggered and must be stable only one setup time before the LOW-to-HIGH clock transition.

Each flip-flop has asynchronous set inputs allowing them to be independently set HIGH. The set inputs are controlled by a common active HIGH parallel load (PL) input. The PL input is not buffered, and care must be taken not to overload the driving element. When the PL is HIGH, a HIGH on the parallel data ($D_0 - D_4$) inputs will set the associated flip-flops HIGH. A LOW on the $D_0 - D_4$ inputs will cause no change in the appropriate flip-flops.

The asynchronous active LOW master reset ($\overline{MR}$) is buffered. When LOW, the $\overline{MR}$ overrides the clock and clears the register if the PL is not active. The parallel load inputs override the $\overline{MR}$ forcing the flip-flops HIGH if both are activated simultaneously. However, for predictable operation, both signals should not be deactivated simultaneously.

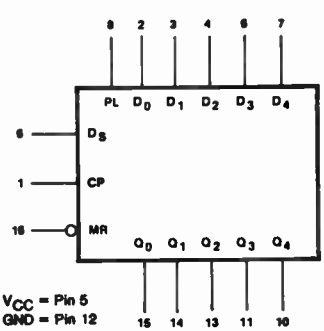
	74LS	74
Shift Frequency (MHz)	10	10
Serial Data Input	D	D
Asynchronous Clear	Low	Low
Shift-Right Mode	Yes	Yes
Shift-Left Mode	No	No
Lead Mode	Yes	Yes
Hold Mode	No	NoTyp.
Total Power (mW)	60	240

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS				
	PL	D_n	MR	CP	D_S	Q_0	Q_1	Q_2	Q_3	Q_4
Parallel Load	H	L	X	X	X	Q_0	Q_1	Q_2	Q_3	Q_4
	H	H	X	X	X	H	H	H	H	H
Reset (clear)	L	X	L	X	X	L	L	L	L	L
Shift right	L	X	H	↑	l	L	q_0	q_1	q_2	q_3
	L	X	H	↑	h	H	q_0	q_1	q_2	q_3

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW to HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW to HIGH clock transition
q_n = Lower case letters indicate the state of the referenced output one setup time prior to the LOW to HIGH clock transition
X = Don't care
↑ = LOW to HIGH clock transition

7496

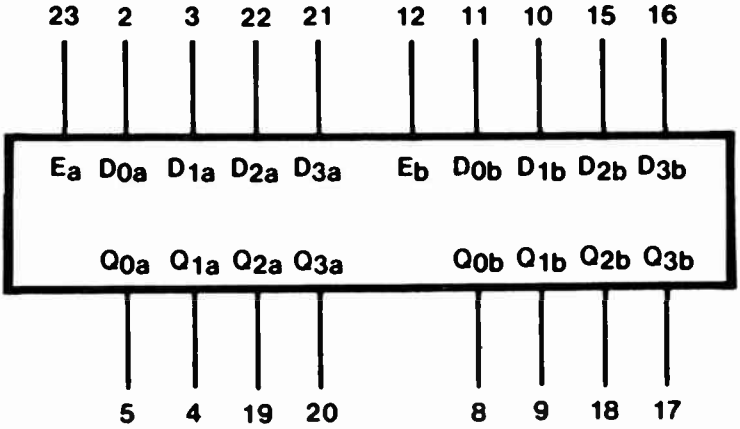


7496

74100 DUAL 4-BIT TRANSPARENT LATCH

The "100" has two independent 4-bit transparent latches. Each 4-bit latch is controlled by an active HIGH Enable input (E). When E is HIGH, the data enters the latch and appears at the output. The outputs follow the data inputs as long as E is HIGH. The data (on the D) input one setup time before the HIGH-to-LOW transition of the enable will be stored in the latch. The latched outputs remain stable as long as the enable is LOW.

	74
Max. Supply Current (mA)	106
Max. Propagation Delay (ns)	30



V_{CC} = Pin 24
GND = Pin 7

74100

MODE SELECT-FUNCTION TABLE

OPERATING MODE	INPUTS		OUTPUTS
	E	D_n	Q_n
Data Enabled	H H	L H	L H
Data Latched	L	X	q

74100

H = HIGH voltage level
L = LOW voltage level
X = Don't care
q = Lower case letters indicate the state of referenced output one setup time prior to the HIGH-to-LOW Enable transition.

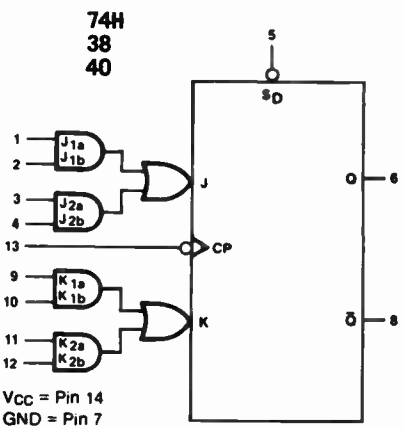
74101 JK EDGE-TRIGGERED FLIP-FLOP

The "101" is a JK negative edge-triggered flip-flop featuring AND-OR gated JK inputs and a direct set input. The Set ($\overline{S}_d$) is an asynchronous active LOW input. When LOW, the $\overline{S}_d$ overrides the clock and data inputs and sets the Q output HIGH and the $\overline{Q}$ output LOW.

A HIGH level on the clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may change while the $\overline{CP}$ is HIGH, and the flip-flop will perform according to the truth table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

	74H
Max. Supply Current (mA)	38
Max. Clock Frequency (MHz)	40

74101



V_{CC} = Pin 14
GND = Pin 7

Pin numbers for pin configuration "A"

MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	X	X	X	H	L
Toggle	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	↓	l	h	L	H
Load "1" (Set)	H	↓	h	l	H	L
Hold "no change"	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.
J = $(J_{1a} \cdot J_{1b}) + (J_{2a} \cdot J_{2b})$
K = $(K_{1a} \cdot K_{1b}) + (K_{2a} \cdot K_{2b})$

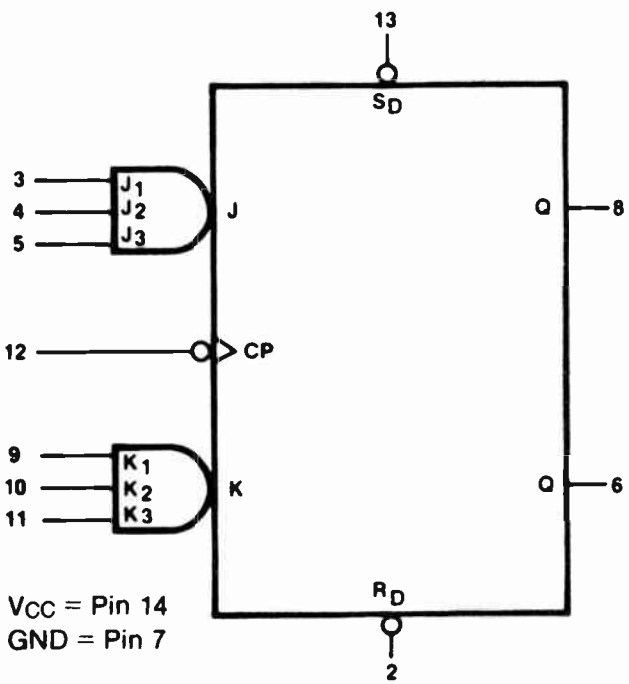
74101

74102 JK EDGE-TRIGGERED FLIP-FLOP

The "102" is a JK negative edge-triggered flip-flop with gated JK inputs and direct set and reset inputs. The set ($\overline{S}_D$) and reset ($\overline{R}_D$) are asynchronous active LOW inputs. When LOW, they override the clock and data inputs, forcing the outputs to their steady state level as shown in the truth table.

A HIGH level on the clock ($\overline{CP}$) input enables the J and K inputs, and data will be accepted. The logic levels at the J and K inputs may change while the $\overline{CP}$ is HIGH, and the flip-flop will perform according to the truth table as long as minimum setup and hold times are observed. Output stage changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

	74H
Max. Supply Current (mA)	38
Max. Clock Frequency (MHz)	40



Pin numbers for pin configuration "A."

74102

MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (c)	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.
J = $J_1 \bullet J_2 \bullet J_3$
K = $K_1 \bullet K_2 \bullet K_3$

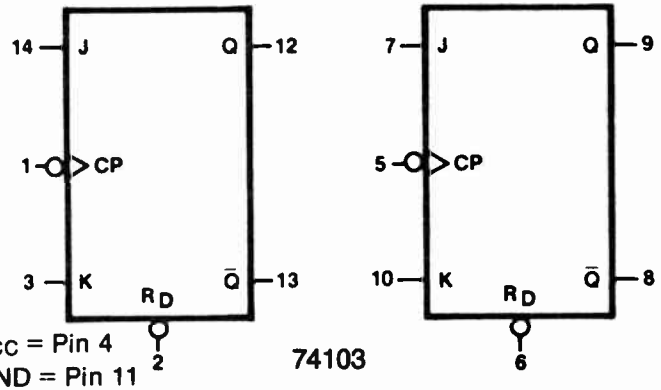
74102

74103 DUAL JK EDGE-TRIGGERED FLIP-FLOP

The "103" is a dual JK negative edge-triggered flip-flop with separate clock and direct reset inputs. The reset ($\overline{R}_D$) is an asynchronous active LOW input. When LOW, the $\overline{R}_D$ overrides the clock and data inputs, and resets (clears) the flip-flop.

A HIGH level on the clock ($\overline{CP}$) input enables the J and K inputs, and data will be accepted. The logic levels at the J and K inputs may change while the $\overline{CP}$ is HIGH, and the flip-flop will perform according to the truth table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

	74H
Typ. Max. Clock Frequency (MHz)	50
Typ. Power Per Flip-Flop (mW)	100
Setup Time (ns)	13
Hold Time (ns)	0



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Reset (Clear)	L	X	X	X	L	H
Toggle	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	↓	l	h	L	H
Load "1" (Set)	H	↓	h	l	H	L
Hold "no change"	H	↓	l	l	q	$\overline{q}$

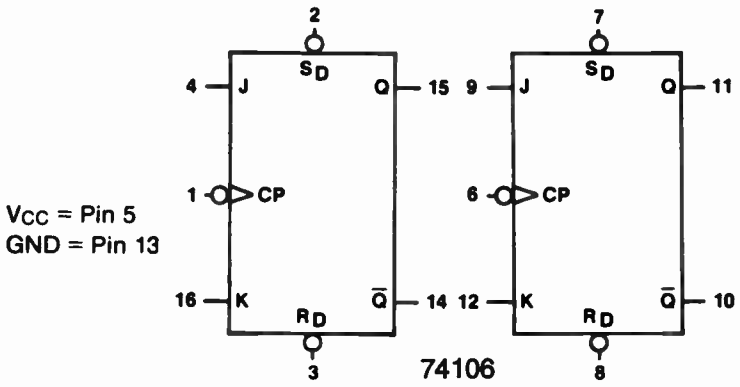
74103

H = HIGH voltage level steady state.
L = LOW voltage level steady state
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.

The "106" is a dual JK negative edge-triggered flip-flop with individual JK, clock, direct set and direct reset inputs. The set ($\overline{S}_D$) and reset ($\overline{R}_D$) are asynchronous active LOW inputs. When LOW, they override the clock and data inputs, forcing the outputs to their steady state level as shown in the truth table.

A HIGH level on the clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may change while the $\overline{CP}$ is HIGH, and the flip-flop will perform according to the truth table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

	74H
Typ. Max. Clock Frequency (MHz)	50
Typ. Power Per Flip-Flop (mW)	100
Setup Time (ns)	13
Hold Time (ns)	0



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined [c]	L	L	X	X	X	H	H
Toggle	H	H	↓	h	l	$\bar{q}$	q
Load "0" (Reset)	H	H	↓	l	l	L	H
Load "1" (Set)	H	H	↓	h	h	H	L
Hold "no change"	H	H	↓	l	h	q	$\bar{q}$

74106

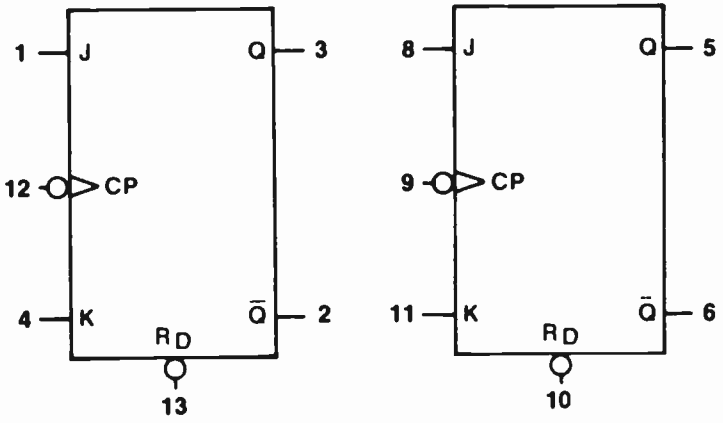
H HIGH voltage level steady state
L LOW voltage level steady state
h HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition
l LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition
X Don't care
q Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition

74107 DUAL JK FLIP-FLOP

The "107" is a dual flip-flop with individual JK, clock and direct reset inputs. The 74107 is a positive pulse triggered flip-flop. JK information is loaded into the master while the clock is HIGH and transferred to the slave on the HIGH-to-LOW clock transition. For these devices, the J and K inputs should be stable while the clock is HIGH for conventional operation.

The 74LS107 is a negative edge triggered flip-flop. The J and K inputs must be stable one setup time prior to the HIGH-to-LOW clock transition for predictable operation. The reset ($\overline{R}_D$) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the Q output LOW and the $\overline{Q}$ output HIGH.

	74LS
Typ. Max. Clock Frequency (MHz)	45
Typ. Power Per Flip-Flop (mW)	10
Setup Time (ns)	20
Hold Time (ns)	0



V_{CC} = Pin 14
GND = Pin 7

47107

MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{R}_D$	$\overline{CP}$(d)	J	K	Q	$\overline{Q}$
Asynchronous Reset (Clear)	L	X	X	X	L	H
Toggle	H	⎍	h	h	$\overline{q}$	q
Load "0" (Reset)	H	⎍	l	h	L	H
Load "1" (Set)	H	⎍	h	l	H	L
Hold "no change"	H	⎍	l	l	q	$\overline{q}$

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition(c).
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition (c).

X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to HIGH-to-LOW Clock transition.
⎍ = Positive clock pulse.

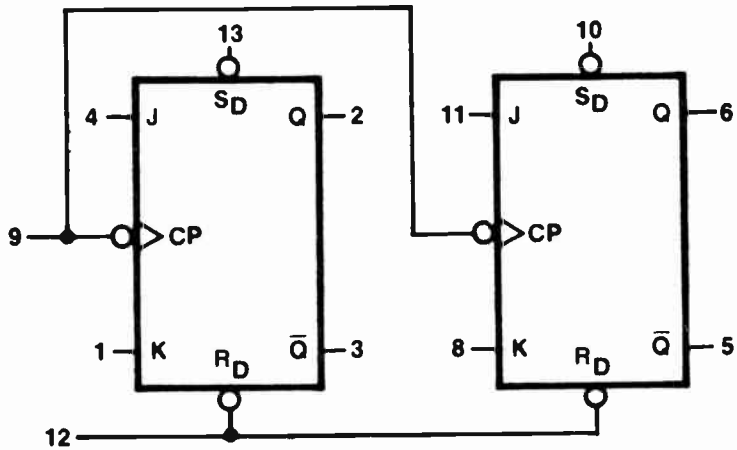
74107

74108 DUAL JK EDGE-TRIGGERED FLIP-FLOP

The "108" is a dual JK negative edge-triggered flip-flop with individual JK and direct set inputs, and common clock and reset inputs. The set ($\overline{S}_D$) and reset ($\overline{R}_D$) are asynchronous active LOW inputs. When LOW, they override the clock and data inputs, forcing the outputs to their steady state level as shown in the truth table.

A HIGH level on the clock ($\overline{CP}$) input enables the J and K inputs, and data will be accepted. The logic levels at the J and K inputs may change while the $\overline{CP}$ is HIGH, and the flip-flop will perform according to the truth table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

	74H
Typ. Max. Clock Frequency (MHz)	50
Typ. Power Per Flip-Flop (mW)	100
Setup Time (ns)	13
Hold Time (ns)	0



74108

V_{CC} = Pin 14
GND = Pin 7

MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined [c]	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.

74108

74109 DUAL $J\overline{K}$ POSITIVE EDGE-TRIGGERED FLIP-FLOP

The "109" is a dual positive edge-triggered $J\overline{K}$-type flip-flop that features individual J, K, clock, set and reset inputs and also complementary Q and $\overline{Q}$ outputs. Set ($\overline{S}_D$) and reset ($\overline{R}_D$) are asynchronous active LOW inputs and operate independently of the clock input.

The J and $\overline{K}$ are edge-triggered inputs that control the state changes of the flip-flops as described in the mode select truth table. The J and $\overline{K}$ inputs must be stable just one setup time prior to the LOW-to-HIGH transition of the clock for predictable operation. The $J\overline{K}$ design allows operation as a D flip-flop by tying the J and $\overline{K}$ inputs together.

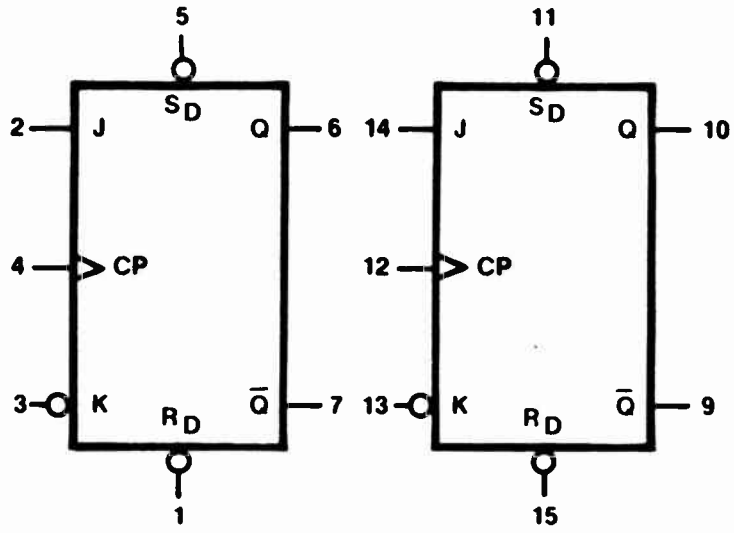
Although the clock input is level-sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock to output delay time for reliable operation.

	74LS	74
Typ. Max. Clock Frequency (MHz)	33	33
Typ. Power Per Flip-Flop (mW)	10	45
Setup Time (ns)	20	10
Hold Time (ns)	5	6

MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (c)	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	$\overline{q}$	q
Load "0" (Reset)	H	H	↑	l	h	L	H
Load "1" (Set)	H	H	↑	h	l	H	L
Hold "no change"	H	H	↑	l	h	q	$\overline{q}$

H = HIGH voltage level steady state
L = LOW voltage level steady state
h = HIGH voltage level one setup time prior to the LOW-to-HIGH Clock transition
l = LOW voltage level one setup time prior to the LOW-to-HIGH Clock transition
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH Clock transition
↑ = LOW-to-HIGH Clock transition



V_{CC} = Pin 16
GND = Pin 8

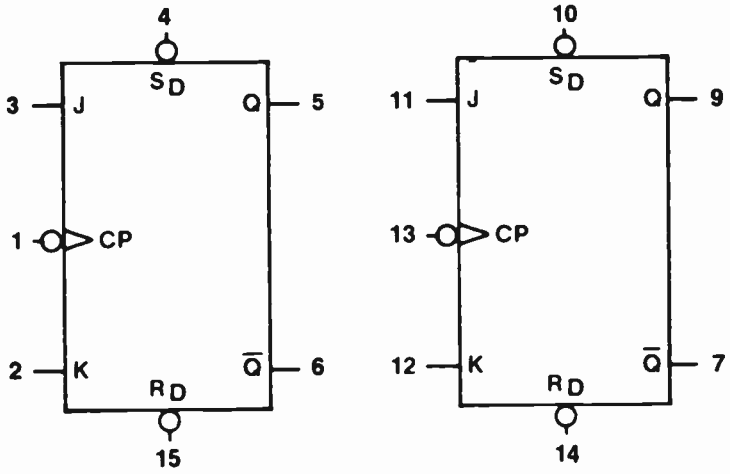
74109

74112 DUAL JK EDGE-TRIGGERED FLIP-FLOP

The "112" is a dual JK negative edge-triggered flip-flop featuring individual J, K, clock, set and reset inputs. The set ($\overline{S_D}$) and reset ($\overline{R_D}$) inputs, when LOW, set or reset the outputs as shown in the truth table, regardless of the levels at the other inputs.

A HIGH level on the clock ($\overline{CP}$) input enables the J and K inputs, and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is HIGH and the flip-flop will perform according to the truth table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

	74S	74LS
Typ. Max. Clock Frequency (MHz)	125	45
Typ. Power Per Flip-Flop (mW)	75	10
Setup Time (ns)	6	20
Hold Time (ns)	0	0



V_{CC} = Pin 16
GND = Pin 8

74112

MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined [c]	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
q = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW Clock transition.
X = Don't care.

74112

74113 DUAL JK EDGE-TRIGGERED FLIP-FLOP

The "113" is a dual JK negative edge-triggered flip-flop featuring individual J, K, set and clock inputs. The asynchronous set ($\overline{S_D}$) input, when LOW, forces the outputs to the steady state levels as shown in the truth table, regardless of the levels at the other inputs.

A HIGH level on the clock ($\overline{CP}$) input enables the J and K inputs, and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is HIGH and the flip-flop will perform according to the truth table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

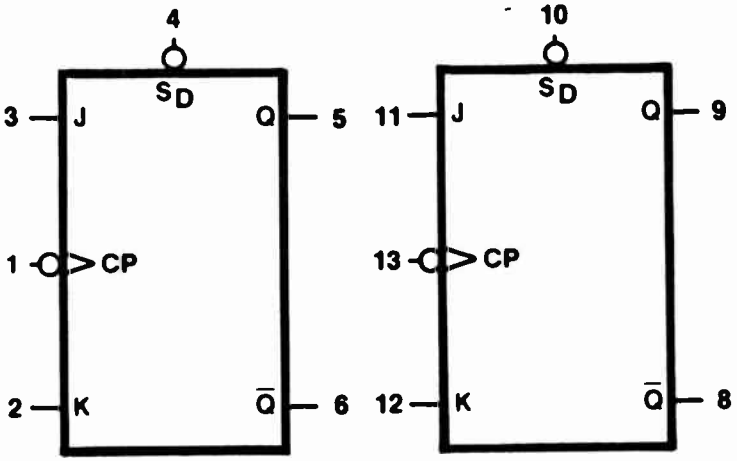
	74S	74LS
Typ. Max. Clock Frequency (MHz)	125	45
Typ. Power Per Flip-Flop (mW)	75	10
Setup Time (ns)	6	20
Hold Time (ns)	0	0

MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	X	X	X	H	L
Toggle	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	↓	l	h	L	H
Load "1" (Set)	H	↓	h	l	H	L
Hold "no change"	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
q = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW Clock transition.
X = Don't care.

74113



V_{CC} = Pin 14
GND = Pin 7

74113

74114 DUAL JK EDGE-TRIGGERED FLIP-FLOP

The "114" is a dual JK negative edge-triggered flip-flop featuring individual J, K and set inputs and common clock and reset inputs. The set ($\overline{S}_D$) and reset ($\overline{R}_D$) inputs, when LOW, set or reset the outputs, as shown in the truth table, regardless of the levels at the other inputs.

A HIGH level on the clock ($\overline{CP}$) input enables the J and K inputs, and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is HIGH, and the flip-flop will perform according to the truth table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

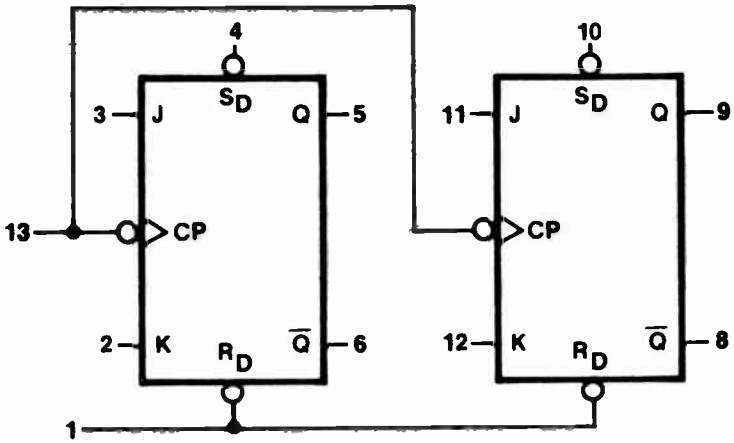
	74S	74LS
Typ. Max. Clock Frequency (MHz)	125	45
Typ. Power Per Flip-Flop (mW)	75	10
Setup Time (ns)	6	20
Hold Time (ns)	0	0

MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (c)	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
q = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW Clock transition.
X = Don't care.

74114



Vcc = Pin 14
GND = Pin 7

74114

The "116" has two independent 4-bit transparent latches. Each 4-bit latch is controlled by a 2-input active LOW Enable gate ($\overline{E_0}$ and $\overline{E_1}$). When both $\overline{E_0}$ and $\overline{E_1}$ are LOW, the data enters the latch and appears at the output. The outputs follow the data inputs as long as $\overline{E_0}$ and $\overline{E_1}$ are LOW. The data on the D inputs one setup time before the LOW-to-HIGH transition of $\overline{E_0}$ or $\overline{E_1}$ will be stored in the latch. The latched outputs remain stable as long as either $\overline{E_0}$ or $\overline{E_1}$ is HIGH.

Each 4-bit latch has an active LOW asynchronous Master Reset ($\overline{MR}$) input. When LOW, the $\overline{MR}$ input overrides the data and enable inputs and sets the four latch outputs LOW.

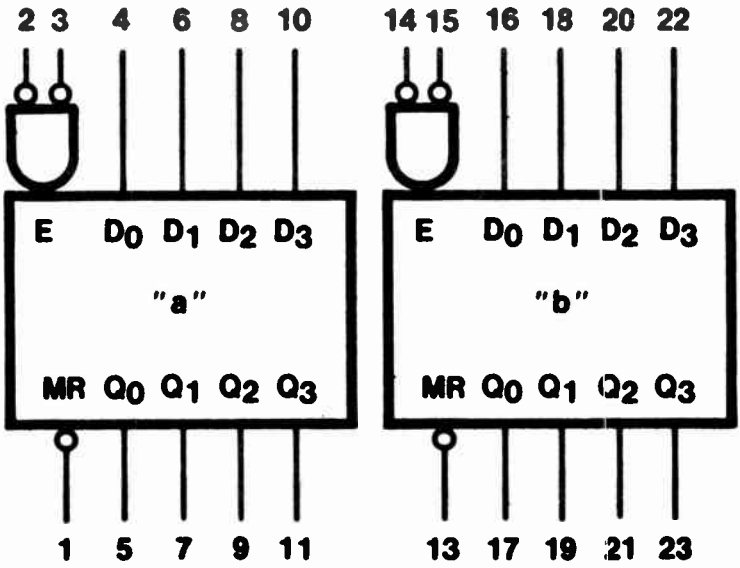
	74
Max. Supply Current (mA)	100
Delay Time, Data to Output (ns)	18

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS
	$\overline{MR}$	$\overline{E}_0$	$\overline{E}_1$	D_n	Q_n
Reset (clear)	L	X	X	X	L
Enable latch	H H	L L	L L	L H	L H
Latch data	H H	↑ L	L ↑	l h	L H

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH Enable transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH Enable transition
X = Don't care
↑ = LOW-to-HIGH Enable transition

74116



V_{CC} = Pin 24
GND = Pin 12

74116

74121 MONOSTABLE MULTIVIBRATOR

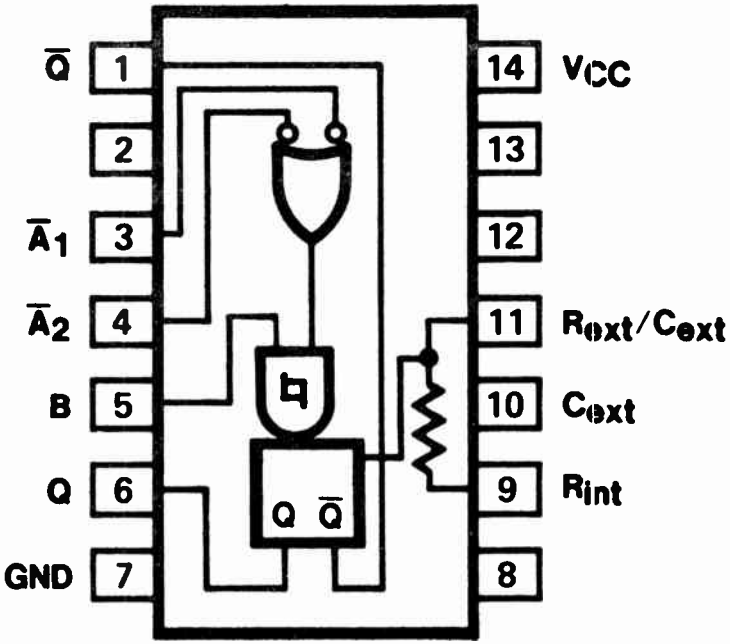
These multivibrators feature dual active LOW-going edge inputs and a single active HIGH-going edge input which can be used as an active HIGH enable input. Complementary output pulses are provided.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{cc} noise of typically 1.5 volts is also provided by internal latching circuitry. Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 20 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R_{int} connected to V_{cc}, C_{ext} and R_{ext}/C_{ext} open), an output pulse of typically 30 or 35 nanoseconds is achieved that may be used as a DC-triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{cc} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{cc} ranges for more than six decades of timing capacitance (10pF to 10μF) and more than one decade of timing resistance (2kΩ to 40kΩ). In circuits where pulse cutoff is not critical, timing capacitance of up to 1000μF and timing resistance of as low as 1.4kΩ may be used.

	74
Positive Inputs	1
Negative Inputs	2
Output Pulse Range (ns to s)	40ns-28s
Typ. Total Power (mW)	90



74121

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{A}_1$	$\overline{A}_2$	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎍
↓	H	H	⎍	⎍
↓	↓	H	⎍	⎍
L	X	↑	⎍	⎍
X	L	↑	⎍	⎍

74121

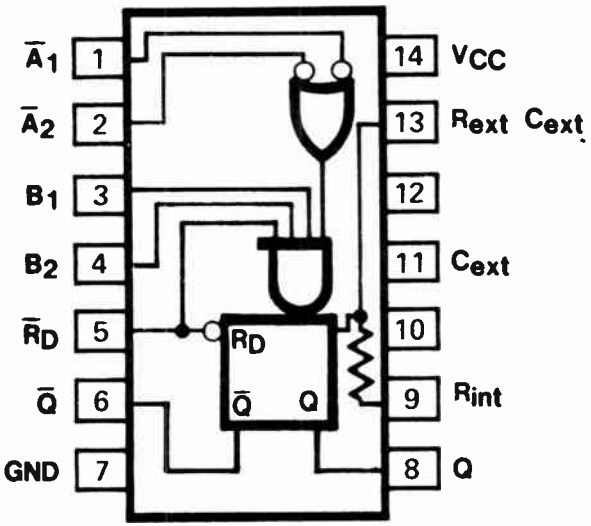
H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition

74122 RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

The "122" is a retriggerable monostable multivibrator featuring output pulse width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values. The "122" has an internal timing resistor that allows the circuit to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated active LOW-going edge inputs ($\overline{A}_1$, $\overline{A}_2$) or the active HIGH-going edge inputs (B_1 B_2), or be reduced by use of the overriding active LOW reset.

To use the internal timing resistor of the "122," connect R_{int} to V_{cc}. For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{cc} with R_{int} left open. To obtain variable pulse widths, connect an external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{cc}.

	74LS
Positive Inputs	2
Negative Inputs	2
Direct Clear	Yes
Output Pulse Range (ns)	45ns-00 (inf.)
Typ. Total Power (mW)	30



74122

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{R}_D$	$\overline{A}_1$	$\overline{A}_2$	B_1	B_2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

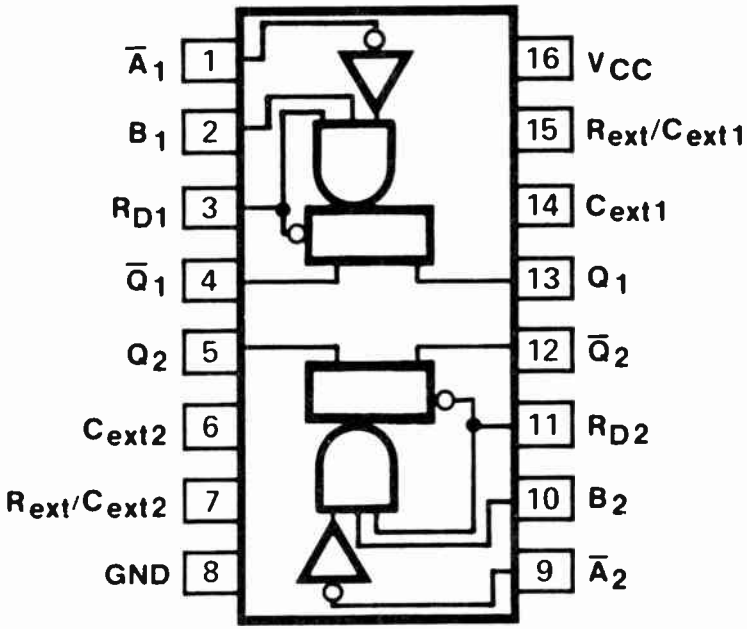
H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH input transition
↓ = HIGH-to-LOW input transition
⎍ = Active HIGH pulse
⎎ = Active LOW pulse

74122

74123 DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

This retriggerable monostable multivibrator features DC triggering from gated active LOW inputs ($\overline{A}$) and active HIGH inputs (B) and also provide overriding direct reset inputs. Complementary outputs are provided. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding reset capability permits any output pulse to be terminated at a predetermined time that is independent of the timing components R and C.

	74	74L	74LS
Positive Inputs	1	1	1
Negative Inputs	1	1	1
Direct Clear	Yes	Yes	Yes
Output Pulse Range (ns)	45ns-00 (inf.)	90ns-00 (inf.)	45ns)00 (inf.)
Typ. Total Power (mW)	230	25	60



74123

FUNCTION TABLE

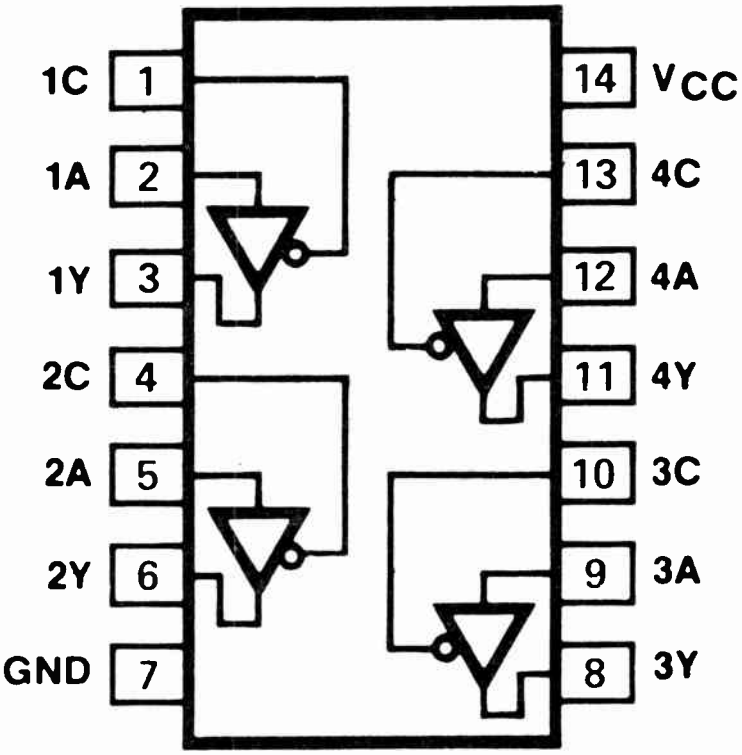
INPUTS			OUTPUTS	
$\overline{R}_D$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition

74123

74125 QUAD 3-STATE BUFFER

	74
Typ. Delay Time (ns)	10
Typ. Power Per Gate (mW)	40



74125

Truth Table

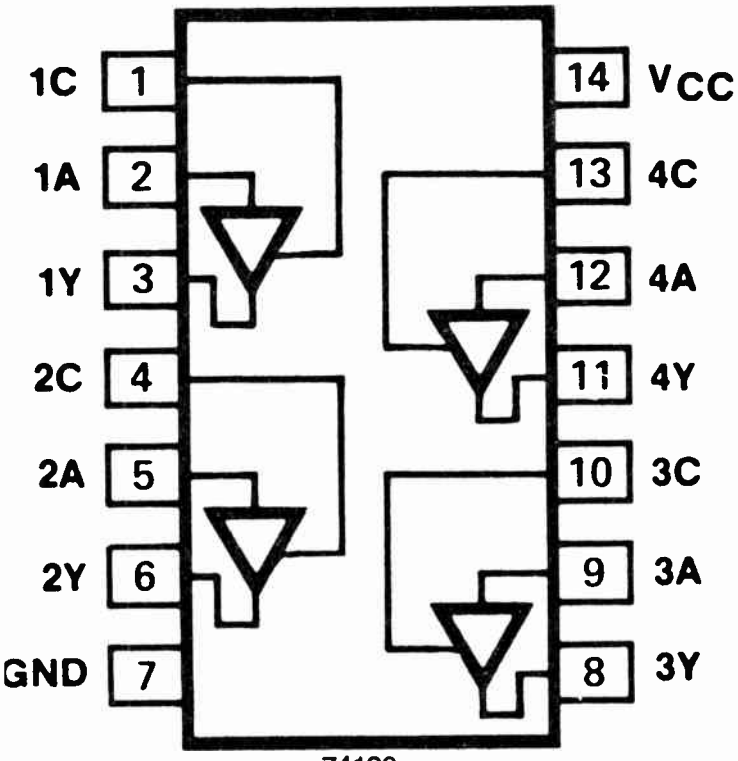
INPUTS		OUTPUT
C	A	Y
L	L	L
L	H	H
H	X	(Z)

L = LOW voltage level
H = HIGH voltage level
X = Don't care
(Z) = High impedance (off)

74125

74126 QUAD 3-STATE BUFFER

	74
Typ. Delay Time (ns)	10
Typ. Power Per Gate (mW)	45



74126

Truth Table

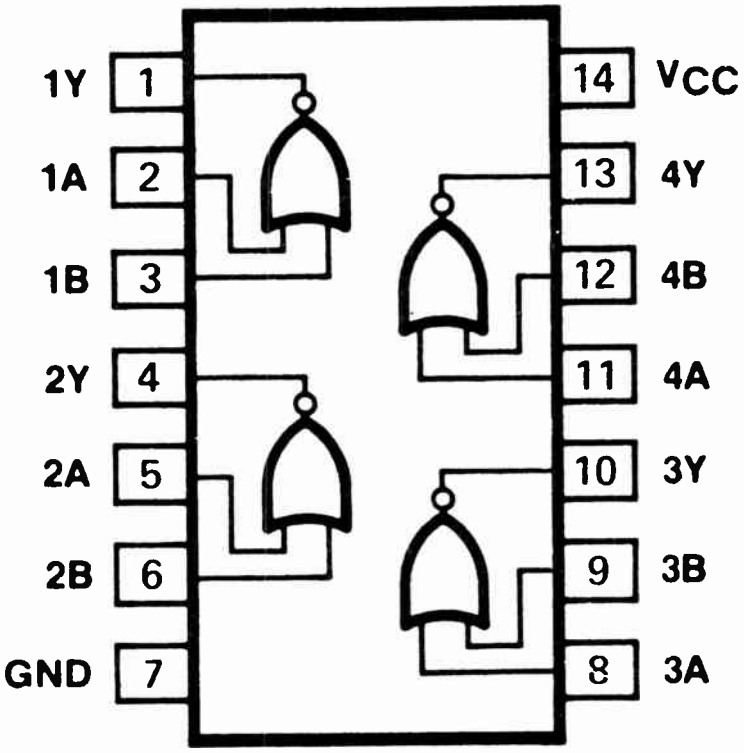
INPUTS		OUTPUT
C	A	Y
H	L	L
H	H	H
L	X	(Z)

L = LOW voltage level
H = HIGH voltage level
X = Don't care
(Z) = High impedance (off)

74126

74128 QUAD 2-INPUT NOR BUFFER

	74
Max. Supply Current (mA)	57
Typ. Max. Propagation Delay (ns)	15



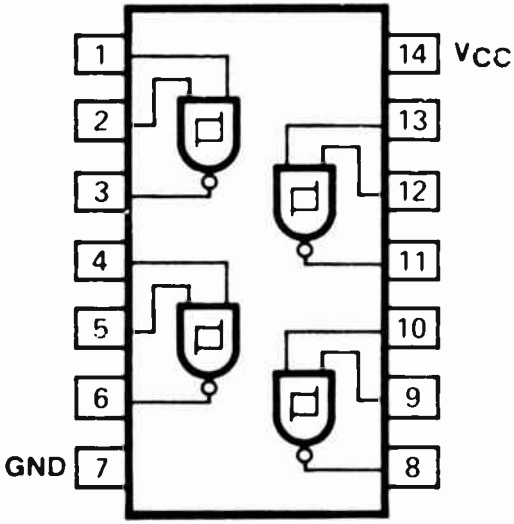
74128

74132 QUAD 2-INPUT NAND SCHMITT TRIGGER

The "132" contains four 2-input NAND gates that accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speedup slow input transition and provide different input threshold voltages for positive-going and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800 mW) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as one input remains at a more positive voltage than V_T + (Max), the gate will respond to the transitions of the other input as shown in the figure.

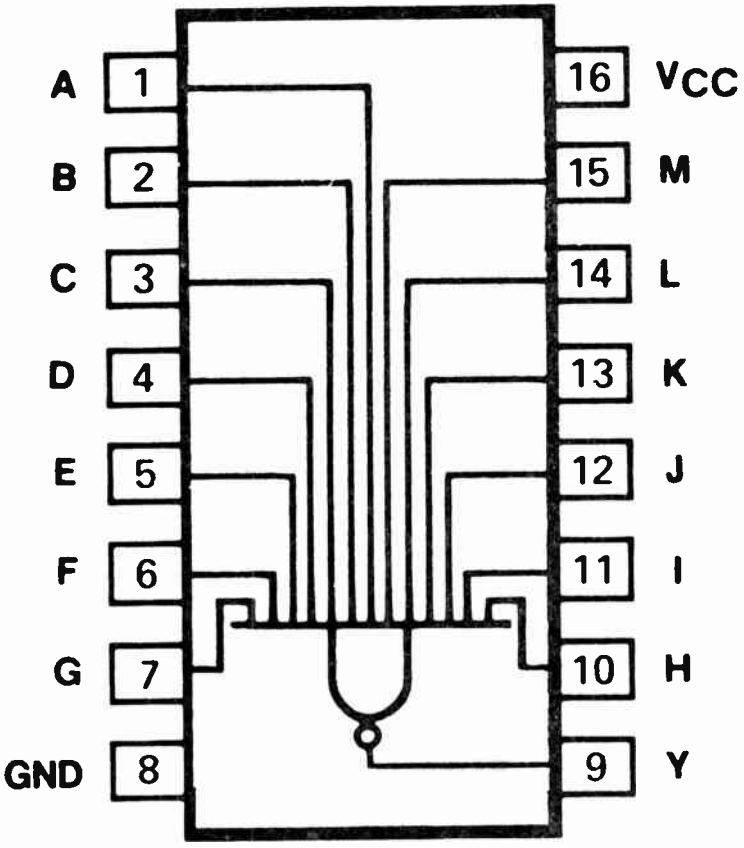
	74	74LS
Typ. Hysteresis (V)	0.8	0.8
Typ. Delay Time (ns)	15	15



74132

74133 13-INPUT NAND GATE

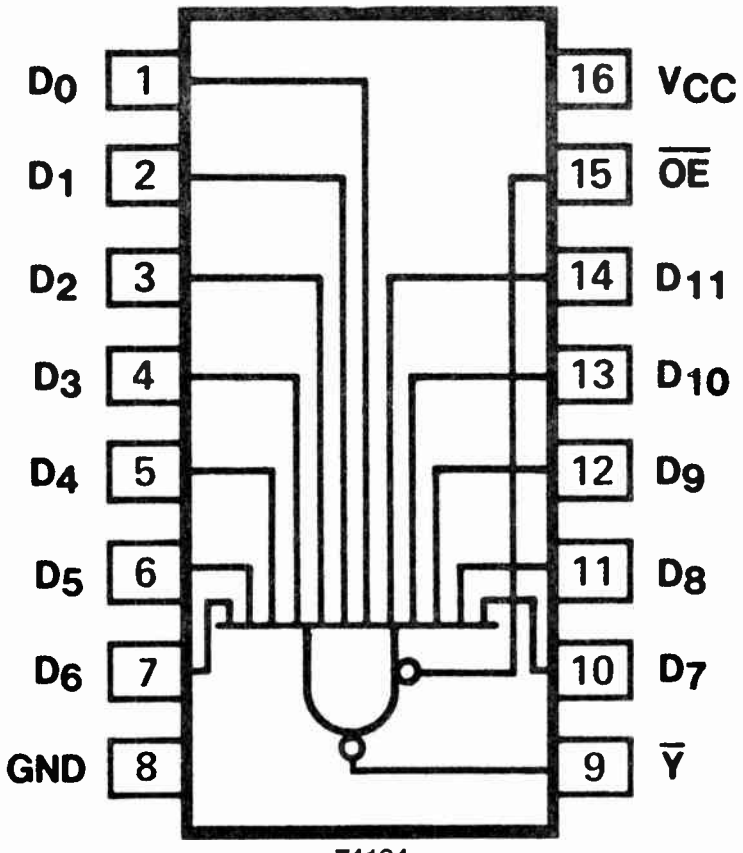
	74S
Typ. Delay Time (ns)	3
Typ. Power Per Gate (mW)	19



74133

74134 12-INPUT NAND GATE (3-STATE)

	74S
Typ. Delay Time (ns)	4.5
Typ. Power Per Gate (mW)	45



74134

Truth Table

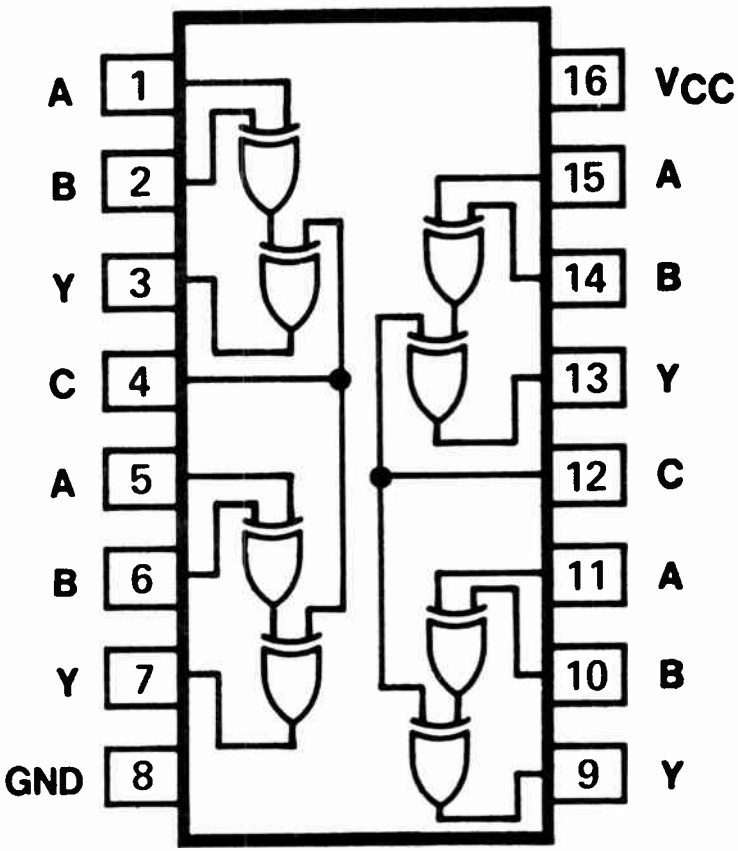
INPUTS		OUTPUT
D_0 - - - - D_{11}	$\overline{OE}$	$\overline{Y}$
H - - - - - H	L	L
one input = L	L	H
X - - - - - X	H	(Z)

74134

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

74135 QUAD EXCLUSIVE OR/NOR GATE

	74S
Max. Supply Current (mA)	99
Typ. Propagation Delay (ns)	12



74135

Truth Table

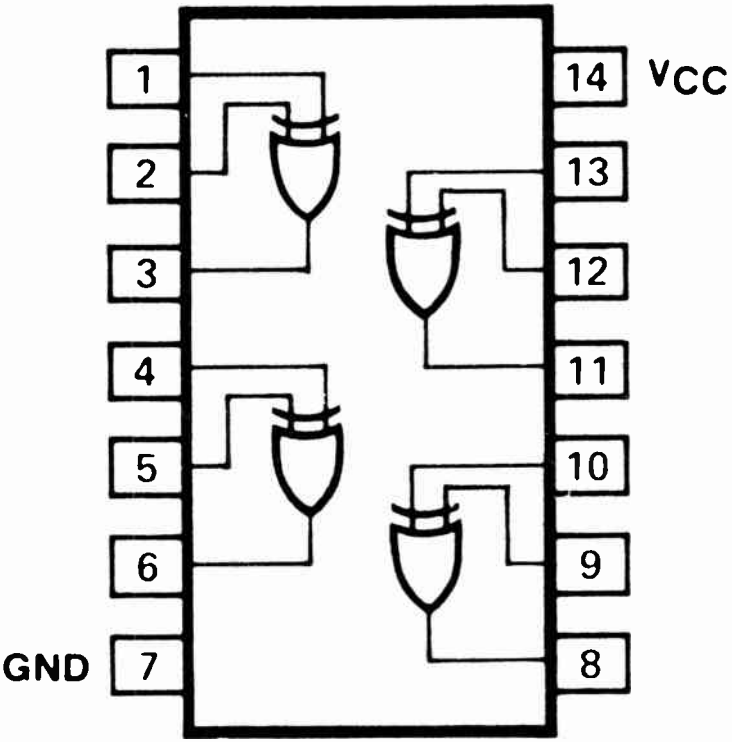
INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

74135

H = HIGH voltage level
L = LOW voltage level

74136 QUAD 2-INPUT EXCLUSIVE-OR GATE (O.C.)

	74LS
Max. Supply Current (mA)	10
Max. Propagation Delay (ns)	30



74136

Truth Table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

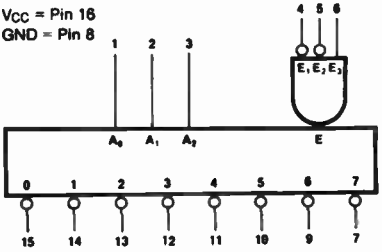
74136

L = LOW voltage level
H = HIGH voltage level

The "138" decoder accepts three binary weighted inputs (A_0, A_1, and A_2) and when enabled, provides eight mutually exclusive active LOW outputs ($\overline{0}$, $\overline{7}$). The device features three enable inputs: two active LOW ($\overline{E_1}$, $\overline{E_2}$) and one active HIGH (E_3). Every output will be HIGH unless $\overline{E_1}$ and $\overline{E_2}$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four "138's" and one inverter.

The device can be used as an eight-output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active HIGH or active LOW state.

	74S	74LS
Type of Output	**Totem Pole**	**Totem Pole**
Typ. Select Time (ns)	**8**	**22**
Typ. Enable Time (ns)	**7**	**21**
Typ. Total Power (mW)	**225**	**31**



74138

Truth Table

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

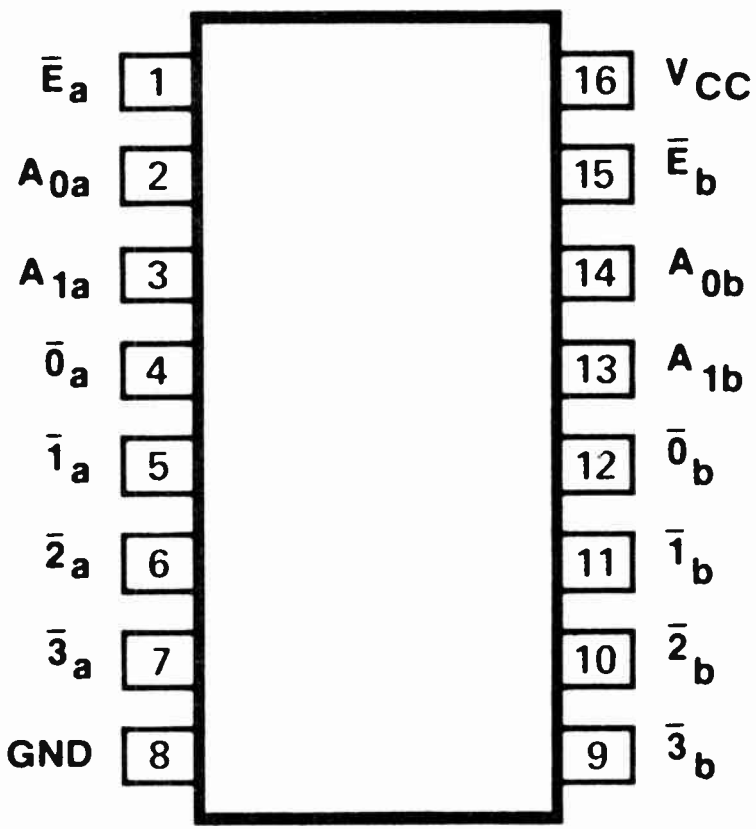
NOTES
H = HIGH voltage level
L = LOW voltage level
X = Don't care

74138

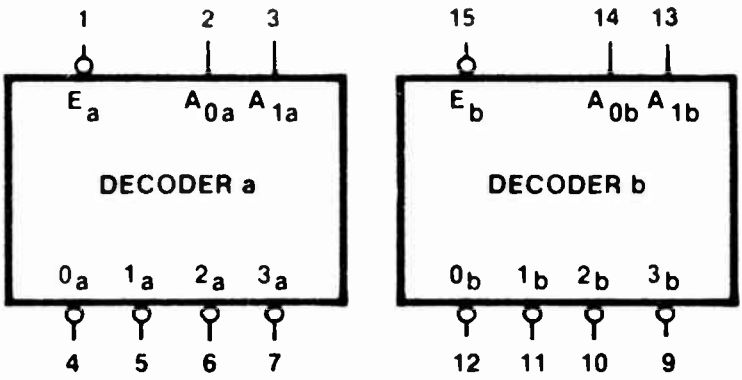
74139 DUAL 1-of-4 DECODER/DEMULTIPLEXER

The "139" is a high-speed dual 1-of-4 decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (A_0 and A_1) and providing four mutually exclusive active LOW outputs ($\overline{0}$ – $\overline{3}$). Each decoder has an active LOW enable. ($\overline{E}$). When $\overline{E}$ is HIGH, every output is forced HIGH. The enable can be used as the data input for a 1-of-4 demultiplexer application

	74S	74LS
Type of Output	Totem Pole	Totem Pole
Typ. Select Time (ns)	7.5	22
Typ. Enable Time (ns)	6	19
Typ. Total Power (mW)	300	34



74139



V_{CC} = Pin 16
GND = Pin 8

74139

Truth Table

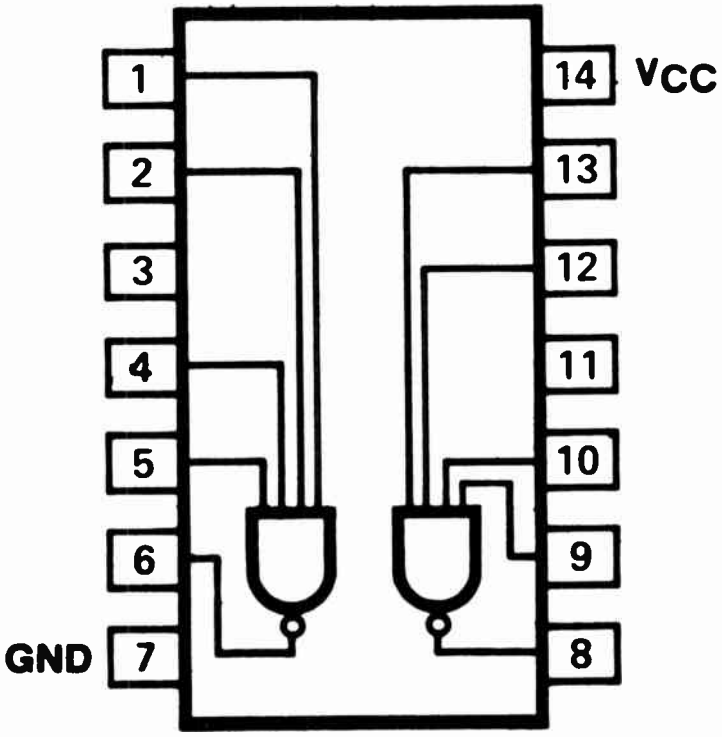
INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level

74139

74140 DUAL 4-INPUT NAND 50-OHM LINE DRIVER

	74S
Low-Level Output Current (mA)	60
High-Level Output Current (mA)	−40
Typ. Delay Time (ns)	4
Typ. Power Per Gate (mW)	44

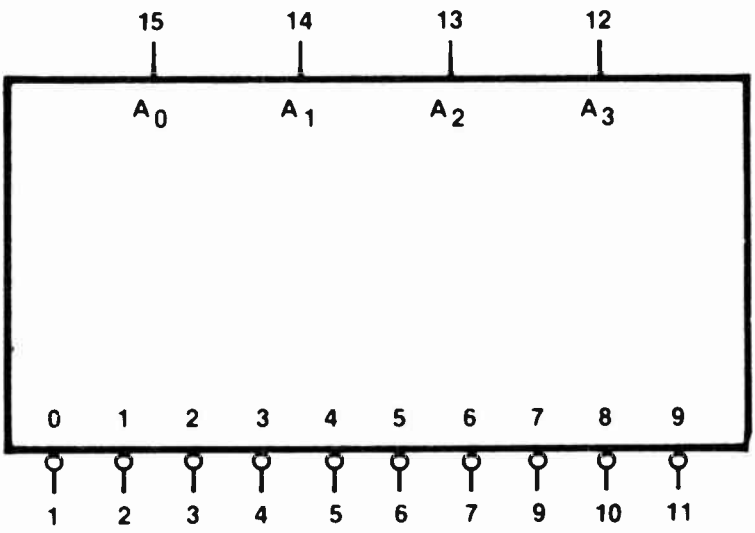


74140

74145 BCD-TO-DECIMAL DECODER/DRIVER (O.C.)

The "145" is a 1-of-10 decoder with open collector outputs. This decoder accepts BCD inputs on the A_0 to A_3 address lines and generates 10 mutually exclusive active LOW outputs. When an input code greater than 9 is applied, all outputs are HIGH. This device can therefore be used as a 1-of-8 decoder with A_3 used as an active LOW enable. The "145" features an output breakdown voltage of 15V. This device is ideal as a lamp or solenoid driver.

	74
Output Sink Current (mA)	80
Off-State Output Voltage (V)	15
Typ. Total Power (mW)	215
Blanking	Invalid Codes



V_{CC} = Pin 16
GND = Pin 8

74145

Truth Table

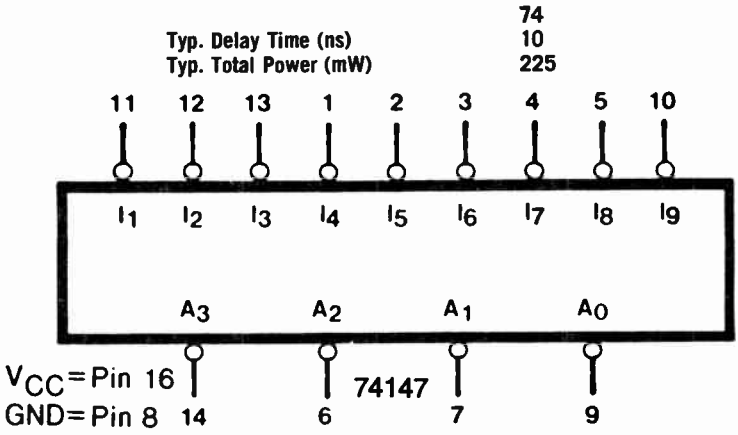
A_3	A_2	A_1	A_0	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage levels
L = LOW voltage levels

74145

The "147" 9-input priority encoder accepts data from nine active LOW inputs ($\overline{I_1}$-$\overline{I_9}$) and provides a binary representation on the four active LOW outputs (A_0-A_3). A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line $\overline{I_9}$ having the highest priority.

The device provides the 10-line-to-4-line priority encoding function by use of the implied decimal zero. The zero is encoded when all nine data inputs are HIGH, forcing all four outputs HIGH.



Truth Table

INPUTS									OUTPUTS			
$\overline{I_1}$	$\overline{I_2}$	$\overline{I_3}$	$\overline{I_4}$	$\overline{I_5}$	$\overline{I_6}$	$\overline{I_7}$	$\overline{I_8}$	$\overline{I_9}$	$\overline{A_3}$	$\overline{A_2}$	$\overline{A_1}$	$\overline{A_0}$
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

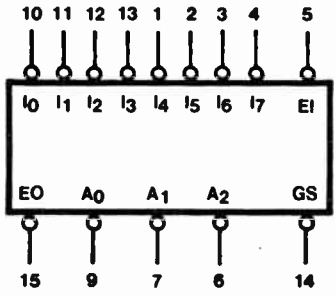
74148 8-INPUT PRIORITY ENCODER

The "148" 8-input priority encoder accepts data from eight active LOW inputs and provides a binary representation on the three active LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line $\overline{I_7}$ having the highest priority. A HIGH on the input enable ($\overline{EI}$) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs.

A group signal output ($\overline{GS}$) and an enable output ($\overline{EO}$) are provided with the three data outputs. The $\overline{GS}$ is active level LOW when any input is LOW. This indicates when any input is active. The $\overline{EO}$ is active level LOW when all inputs are HIGH. Using the output enable along with the input enable allows priority coding of N input signals. Both $\overline{EO}$ and $\overline{GS}$ are active HIGH when the input enable is HIGH.

	74
Typ. Delay Time (ns)	12
Typ. Total Power (mW)	130

V_{CC} = Pin 16
GND = Pin 8



74148

Truth Table

INPUTS									OUTPUTS				
$\overline{EI}$	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{GS}$	A_0	A_1	A_2	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

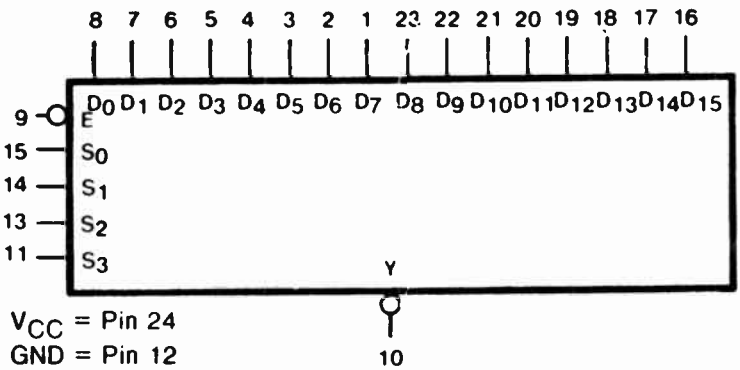
H = HIGH voltage level
L = LOW voltage level
X = Don't care

74148

74150 16-INPUT MULTIPLEXER

The "150" is a logical implementation of a single pole, 16-position switch with the switch position controlled by the state of four select inputs: S_0, S_1, S_2 and S_3. The multiplexer output ($\overline{Y}$) inverts the selected data. The enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, the $\overline{Y}$ output is HIGH, regardless of all other inputs. In one package, the "150" provides the ability to select from 16 sources of data or control information.

	74
Type of Output	**Standard**
Typ. Delay, Data to Inverting Output (ns)	**Standard**
Typ. Delay Time, From Enable (ns)	**18**
Typ. Total Power (mW)	**200**



74150

Truth Table

INPUTS																					OUTPUT
S_3	S_2	S_1	S_0	E	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	Y
X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	H	L	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	H	L	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	L	L	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	L	L	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	H	L	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	H	L	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	L	L	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	H
L	H	L	L	L	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	H	L	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	H
L	H	L	H	L	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	L
L	H	H	L	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	H
L	H	H	L	L	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	L
L	H	H	H	L	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
L	H	H	H	L	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	L
H	L	L	L	L	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	H
H	L	L	L	L	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	L
H	L	L	H	L	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	H
H	L	L	H	L	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	L
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	H
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	L
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	H
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	L
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	H
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	L
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	H
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	L
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	H
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	L
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	H
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

74150

74151 8-INPUT MULTIPLEXER

The "151" is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three select inputs: S_0, S_1 and S_2. True (Y) and complement ($\overline{Y}$) outputs are both provided. The enable input ($\overline{E}$) is active LOW when E is HIGH and the Y output is LOW, regardless of all other inputs.

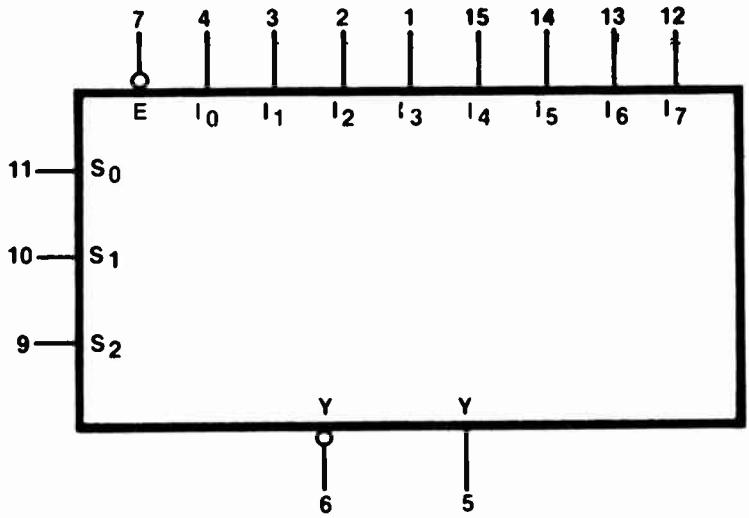
In one package, the "151" provides the ability to select from eight sources of data or control information. The device can provide any logic function of four variables and its negation with correct manipulation.

Type of Output	74S Standard	74 Standard	74LS Standard
Typ. Delay, Data to Inverting Output (ns)	4.5	8	11
Typ. Delay, Data to Noninverting Output (ns)	8	16	18
Typ. Delay Time, From Enable (ns)	9	22	27
Typ. Total Power (mW)	225	145	30

Truth Table

INPUTS												OUTPUTS	
$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage level
L = LOW Voltage level
X = Don't care

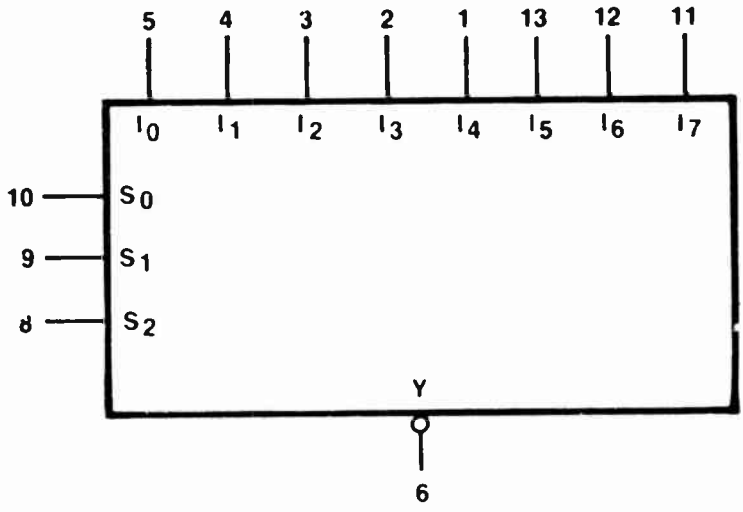


V_{CC} = Pin 16
GND = Pin 8

74151

The "152" is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three select inputs: S_0, S_1 and S_2. The "152" provides in one package the ability to select from eight sources of data or control information.

	74
Max. Supply Current (mA)	43
Max. Delay, Data to Inverting Output (ns)	17



V_{CC} = Pin 14
GND = Pin 7

74152

Truth Table

S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$
L	L	L	L	X	X	X	X	X	X	X	H
L	L	L	H	X	X	X	X	X	X	X	L
L	L	H	X	L	X	X	X	X	X	X	H
L	L	H	X	H	X	X	X	X	X	X	L
L	H	L	X	X	L	X	X	X	X	X	H
L	H	L	X	X	H	X	X	X	X	X	L
L	H	H	X	X	X	L	X	X	X	X	H
L	H	H	X	X	X	H	X	X	X	X	L
H	L	L	X	X	X	X	L	X	X	X	H
H	L	L	X	X	X	X	H	X	X	X	L
H	L	H	X	X	X	X	X	L	X	X	H
H	L	H	X	X	X	X	X	H	X	X	L
H	H	L	X	X	X	X	X	X	L	X	H
H	H	L	X	X	X	X	X	X	H	X	L
H	H	H	X	X	X	X	X	X	X	L	H
H	H	H	X	X	X	X	X	X	X	H	L

74152

H HIGH voltage level
L LOW voltage level
X Don't care

74153 DUAL 4-LINE TO 1-LINE MULTIPLEXER

The "153" is a dual 4-input multiplexer that can select two bits of data from up to four sources under control of the common select inputs (S_0 and S_1). The two 4-input multiplexer circuits have individual active LOW enables ($\overline{E}_a$, $\overline{E}_b$) that can be used to strobe the outputs independently. Outputs (Y_a and Y_b) are forced LOW when the corresponding enables (E_a and E_b) are HIGH.

The device is the logical implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The "153" can be used to move data to a common output bus from a group of registers. The state of the select inputs would determine the particular register from which the data came. An alternative application is as a function generator. The device can generate two functions of three variables. This is useful for implementing highly irregular random logic.

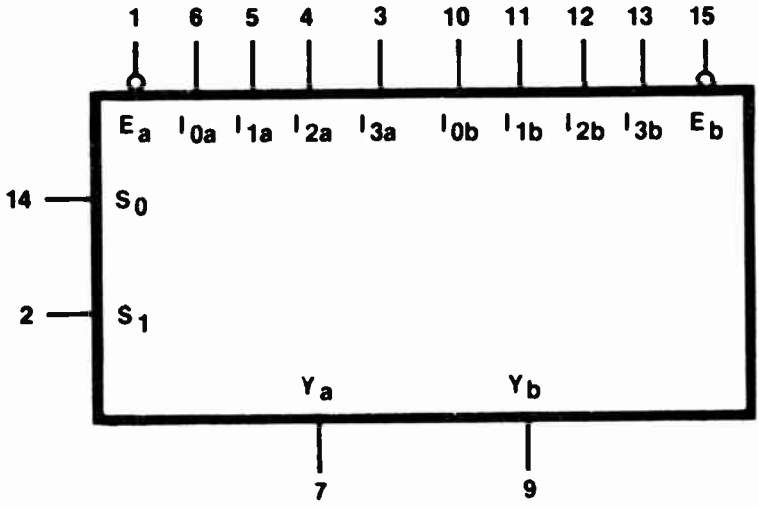
	74S	74	74LS
Type of Output	**Standard**	**Standard**	**Standard**
Typ. Delay, Data to Noninverting Output (ns)	**6**	**14**	**14**
Typ. Delay Time, From Enable (ns)	**9.5**	**17**	**17**
Typ. Total Power (mW)	**225**	**180**	**31**

Truth Table

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Y
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

74153



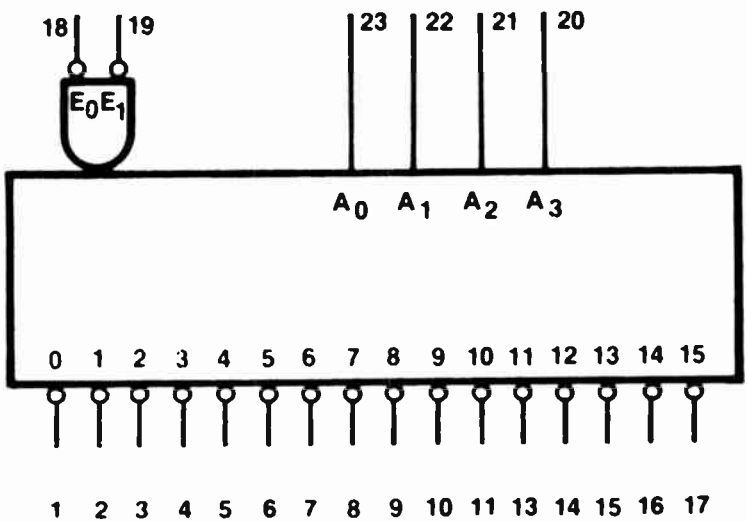
V_{CC} = Pin 16
GND = Pin 8

74153

The "154" accepts four active HIGH binary address inputs and provides 16 mutually exclusive active LOW outputs. The 2-input enable gate can be used to strobe the decoder to eliminate the normal decoding glitches on the outputs, or it can be used for expansion of the decoder. The enable gate has two ANDed inputs which must be LOW to enable the outputs.

The "154" can be used as a 1-of-16 demultiplexer by using one of the enable inputs as the multiplexed data input. When the other enable is LOW, the addressed output will follow the state of the applied data.

Type of Output	74 Totem Pole	74LS Totem Pole	74L Totem Pole
Typ. Select Time (ns)	19.5	23	55
Typ. Enable Time (ns)	17.5	19	45
Typ. Total Power (mW)	170	45	24



V_{CC} = Pin 24
GND = Pin 12

74154

Truth Table

INPUTS						OUTPUTS														
$\overline{E}_0$	$\overline{E}_1$	A_3	A_2	A_1	A_0	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$	$\overline{10}$	$\overline{11}$	$\overline{12}$	$\overline{13}$	$\overline{14}$	$\overline{15}$
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

74154

H = HIGH voltage level
L = LOW voltage level
X = Don't care

The "155" is a dual of 1-of-4 decoder/demultiplexer with common address inputs and separate gated enable inputs. Each decoder section, when enabled, will accept the binary weighted address input (A_0 and A_1) and provide four mutually exclusive active LOW outputs (0-3). When the enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Both decoder sections have a 2-input enable gate. For decoder a, the enable gate requires one active HIGH input and one active LOW input ($E_a \cdot \overline{E}_a$). Decoder a can accept either true or complemented data in demultiplexing applications, by using the $\overline{E}_a$ or E_a inputs respectively. The decoder b enable gate requires two active LOW inputs ($E_b \cdot \overline{E}_b$). The device can be used as a 1-or-8 decoder/demultiplexer by tying E_a or $\overline{E}_b$ and relabeling the common connection address as A_2, forming the common enable by connecting the remaining $\overline{E}_b$ and $\overline{E}_a$.

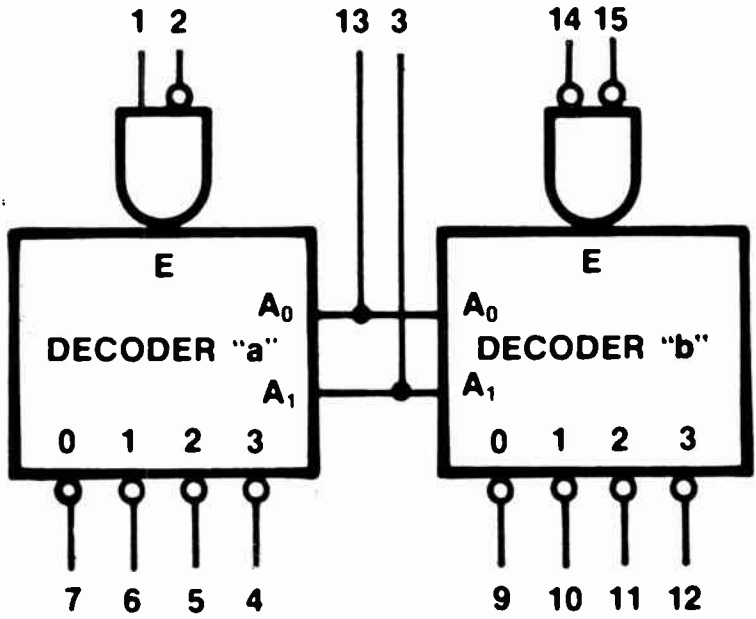
	74LS	74
Type of Output	**Totem Pole**	**Totem Pole**
Typ. Select Time (ns)	**18**	**21**
Typ. Enable Time (ns)	**15**	**16**
Typ. Total Power (mW)	**30**	**250**

Truth Table

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	E_b	$\overline{E}_b$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care.

74155



V_{CC} = Pin 16
GND = Pin 8

74155

74156 DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER (O.C.)

The "156" is a dual 1-of-4 decoder/demultiplexer with, common address inputs and gated enable inputs. Each decoder section, when enabled, will accept the binary weighted address inputs (A_0 and A_1) and provide four mutually exclusive active LOW outputs ($\overline{0}$-$\overline{3}$). When the enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Both decoder sections have a 2-input enable gate. For decoder a, the enable gate requires one active HIGH input and one active LOW input ($E_a \cdot \overline{E}_a$). Decoder a can accept either true or complemented data in demultiplexing applications by using the $\overline{E}_a$ or E_a inputs, respectively. The decoder b enable gate requires two active LOW inputs ($\overline{E}_b \cdot \overline{E}_b$). The device can be used as a 1-or-8 decoder/demultiplexer by tying E_a to $\overline{E}_b$ and relabeling the common connection address as A_2, forming the common enable by connecting the remaining $\overline{E}_b$ and $\overline{E}_a$.

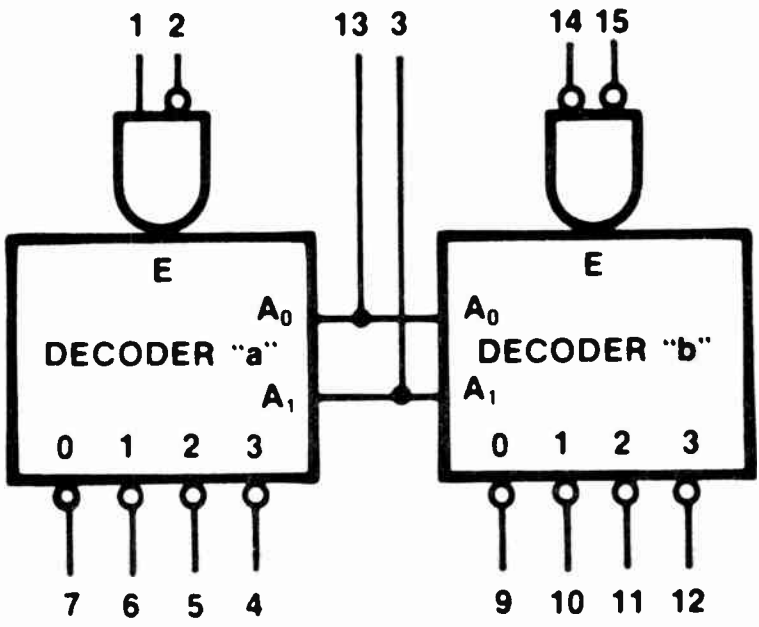
The "156" can be used to generate all four minterms of two variables. The four minterms are useful to replace multiple gate functions in some applications.

	74	74LS
Typ of Output	**Open Collector**	**Open Collector**
Typ. Select Time (ns)	**23**	**33**
Typ. Enable Time (ns)	**18**	**26**
Typ. Total Power (mW)	**250**	**31**

Truth Table

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{E}_b$	$\overline{E}_b$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care.



V_{CC} = Pin 16
GND = Pin 8

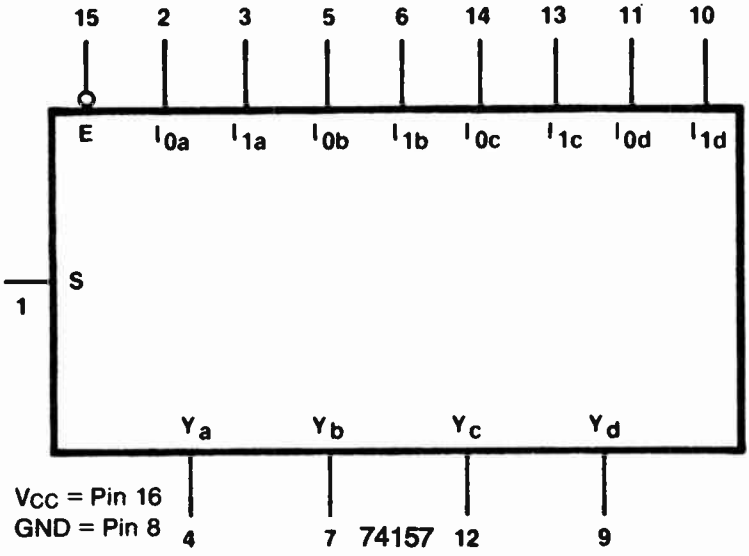
74156

74157 QUAD 2-INPUT DATA SELECTOR/MULTIPLEXER (NON-INVERTED)

The "157" is a quad 2-input multiplexer that selects four bits of data from two sources under the control of a common select input (S). The enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Y) are forced LOW, regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the "157". The state of the select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common. The device is the logic implementation of a four-pole, two-position switch where the position of the switch is determined by the logic levels supplied to the select input.

Type of Output	74S Standard	74LS Standard	74 Standard	74L Standard
Type Delay, Data to Noninverting Output (ns)	5	9	9	40
Typ. Delay, from Enable (ns)	8	14	4	60
Typ. Total Power (mW)	250	49	150	15



Truth Table

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\bar{E}$	S	I_0	I_1	Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

74157

The "158" is a quad 2-input multiplexer that selects four bits of data from two sources under the control of a common select input (S), presenting the data in inverted form at the four outputs ($\overline{Y}$). The enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs ($\overline{Y}$) are forced HIGH, regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the 74158. The state of the select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing gating functions by generating any four functions of two variables with one variable common. The device is the logic implementation of a four-pole, two-position switch where the position of the switch is determined by the logic levels supplied to the select input.

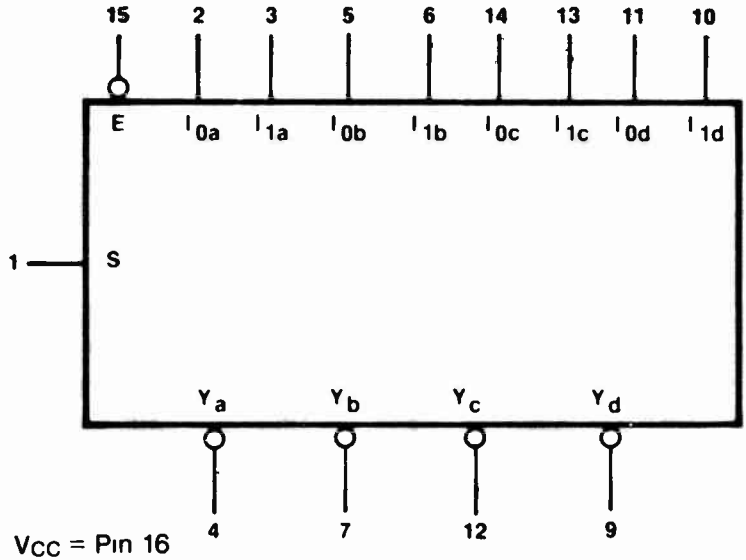
	74S	74LS
Type of Output	**Standard**	**Standard**
Typ. Delay, Data to Inverting Output (ns)	4	7
Typ. Delay, From Enable (ns)	7	12
Typ. Total Power (mW)	195	24

Truth Table

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{E}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H HIGH voltage level
L LOW voltage level
X Don't care

74158



V_{CC} = Pin 16
GND = Pin 8

74158

The "159" decoder accepts four active HIGH binary address inputs and provides 16 mutually exclusive active LOW outputs. The 2-input enable gate can be used to strobe the decoder to eliminate the normal decoding glitches on the outputs, or it can be used for expansion of the decoder. The enable gate has two ANDed inputs which must be LOW to enable the outputs.

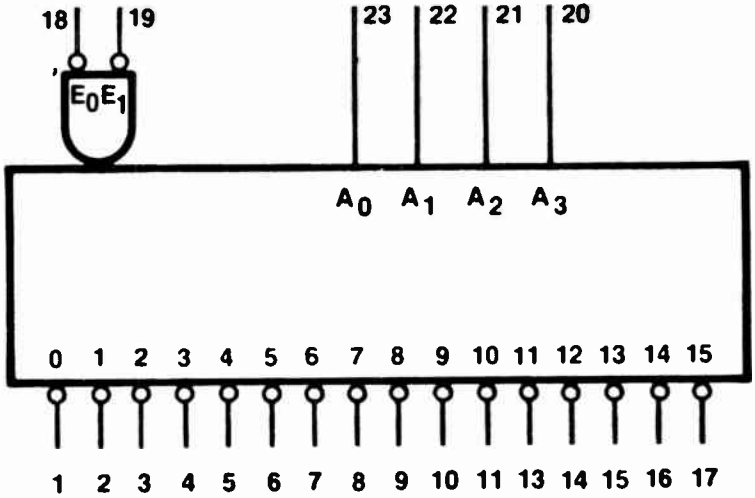
The 74159 can be used as a 1-of-16 demultiplexer by using one of the enable inputs as the multiplexed data input. When the other enable is LOW, the addressed output will follow the state of the applied data. The open collector outputs can be wired together to provide a means of generating any combination of the 16 minterms of four variables applied to the $A_0 \cdot A_3$ inputs.

	74
Max. Supply Current (mA)	**56**
Max. Delay, Address to Output (ns)	**36**

Truth Table

INPUTS						OUTPUTS													
$\bar{E}_0$	$\bar{E}_1$	A_3	A_2	A_1	A_0	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	$\bar{4}$	$\bar{5}$	$\bar{6}$	$\bar{7}$	$\bar{8}$	$\bar{9}$	$\bar{10}$	$\bar{11}$	$\bar{12}$	$\bar{13}$	$\bar{14}$	$\bar{15}$
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care



V_{CC} = Pin 24
GND = Pin 12

74159

74160 DEC DECADE COUNTER

The "160" is a high-speed BCD decade counter. The counters are positive edge-triggered, synchronously presettable and are easily cascaded to n-bit synchronous applications without additional gating. A terminal count output is provided which detects a count of HLLH. The master reset asynchronously clears all flip-flops.

The "160" is a synchronous presettable BCD decade counter featuring an internal carr lookahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting that which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the positive-going edge of the clock. The clock input on the LS 160 features about 400 mV of hysteresis to reduce false triggering caused by noise on the clock line or by slowly rising clock edges.

The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock, and takes place regardless of the levels of the count enable inputs. A LOW level on the parallel enable ($\overline{PE}$) input disables the counter and causes the data at the D_n inputs to be loaded into the counter on the next LOW-to-HIGH transition of the clock. The reset (clear) function for the "160" is asynchronous. A LOW level on the master reset ($\overline{MR}$) input sets all four of the flip-flop outputs LOW, regardless of the levels of the CP, $\overline{PE}$, CET and CEP inputs.

The carry lookahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count enable inputs (CET•CEP) and a terminal count (TC) output. Both count enable inputs must be HIGH to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a HIGH output pulse with a

duration approximately equal to the HIGH level portion of the Q_0 output. This HIGH level TC pulse is used to enable successive cascaded stages. The fast synchronous multi-stage counting connections are shown here.

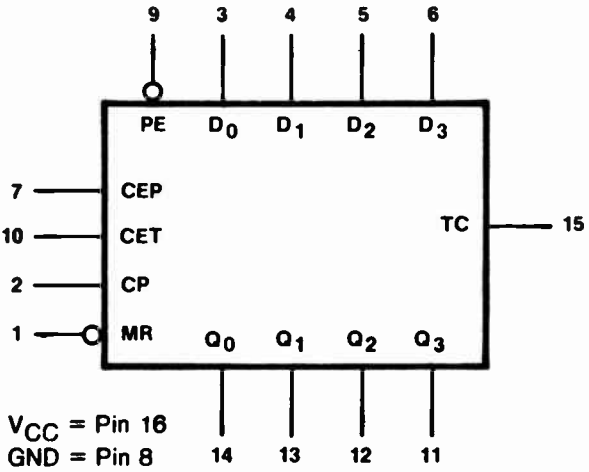
All changes of the Q outputs (except due to the asynchronous master reset) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the clock input (CP). As long as the setup time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs. However, for conventional operation of the 74160 the following transitions should be avoided:

- HIGH-to-LOW transition on the CEP or CET input if the clock is LOW.
- LOW-to-HIGH transition on the parallel enable input when the CP is LOW, if the count enables are HIGH at or before the transition.

For some applications, the designer may want to change those inputs while the clock is LOW. In this case, the 74160 will behave in a predictable manner. For example, if $\overline{PE}$ goes HIGH while the clock is LOW, and Count Enable is not active during the remaining clock LOW period (i.e. CEP or CET are LOW), the subsequent LOW-to-HIGH clock transition will change Q_0-Q_3 to the D_0-D_3 data that existed at the setup time before the rising edge of $\overline{PE}$. If $\overline{PE}$ goes HIGH while the clock is LOW, and count enable is active (CEP and CET are HIGH) during some portion of the remaining clock LOW period, the 74160 will perform a mixture of counting and loading. On the LOW-to-HIGH clock transition, outputs Q_0-Q_3 will change as the count sequence or the loading requires. Only the outputs that would not change in the count sequence and that are also reloaded with their present value stay constant.

If count enable is active (i.e., CEP and CET are HIGH) during some portion of the clock LOW period, and $\overline{PE}$ is HIGH (inactive) during the entire clock LOW period, the subsequent LOW-to-HIGH clock transition will change Q_0-Q_3 to the next count value.

	74LS	74
Count Frequency (MHz)	25	25
Parallel Load	Synchronous	Synchronous
Clear	Asynchronous-Low	Asynchronous-Low
Typ. Total Power (mW)	93	305



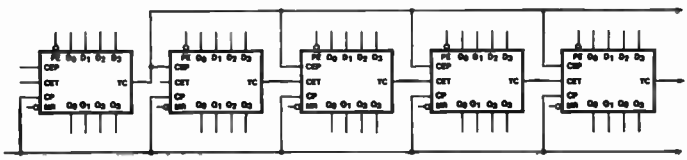
MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(b)
Count	H	↑	h	h	h(d)	X	count	(b)
Hold (do nothing)	H	X	l(c)	X	h(d)	X	q_n	(b)
	H	X	X	l(c)	h(d)	X	q_n	L

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition

NOTES
(b) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HLLH for "160").
(c) The HIGH-to-LOW transition of CEP or CET on the 54/74160 should only occur while CP is HIGH for conventional operation
(d) The LOW-to-HIGH transition of $\overline{PE}$ on the 54/74160 should only occur while CP is HIGH for conventional operation.

SYNCHRONOUS MULTISTAGE COUNTING SCHEME



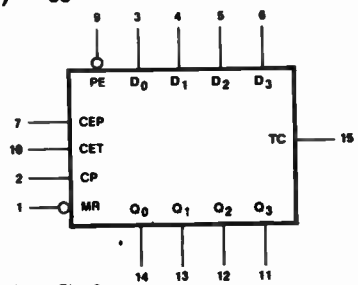
74160

74161 4-BIT BINARY COUNTER

The "161" is a high-speed 4-bit binary counter. The counters are positive edge-triggered, synchronously presettable and are easily cascaded to n-bit synchronous applications without additional gating. A terminal count output is provided which detects a count of HHHH. The master reset asynchronously clears all flip-flops.

Refer to 74160 for a further explanation of binary counters

	74LS	74
Count Frequecy (MHz)	25	25
Parallel Load	Synchronous	Synchronous
Clear	Asynchronous-Low	Asynchronous-Low
Typ. Total Power (mW)	93	305



74161

V_{CC} = Pin 16
GND = Pin 8

MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(b)
Count	H	↑	h	h	h(d)	X	count	(b)
Hold (do nothing)	H	X	l(c)	X	h(d)	X	q_n	(b)
	H	X	X	l(c)	h(d)	X	q_n	L

H = HIGH voltage level steady state.
L = LOW voltage level steady state
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

NOTES
(b) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HHHH for "161").
(c) The HIGH-to-LOW transition of CEP or CET on the 54 74161 should only occur while CP is HIGH for conventional operation.
(d) The LOW-to-HIGH transition of $\overline{PE}$ on the 54 74161 should only occur while CP is HIGH for conventional operation.

74161

74162 BCD DECADE COUNTER

The "162" is a high-speed BCD decade counter. The counters are positive edge-triggered, synchronously presettable and are easily cascaded to n-bit synchronous applications without additional gating. A terminal count output is provided that detects a count of HLLH. The synchronous reset is edge-triggered. It overrides all control inputs, but is active only during the rising clock edge.

Refer to 74160 for a further explanation of binary counters.

	74LS	74
Count Frequency (MHz)	25	25
Parallel Load	Synchronous	Synchronous
Clear	Synchronous-Low	Synchronous-Low
Typ. Total Power (mW)	93	305

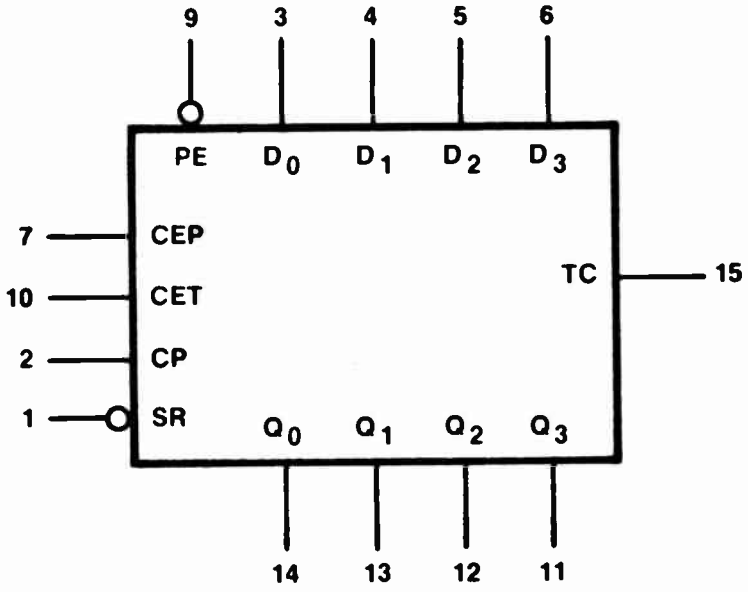
MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (Clear)	l	↑	X	X	X	X	L	L
Parallel Load	h(d)	↑	X	X	l	l	L	L
	h(d)	↑	X	X	l	h	H	(b)
Count	h(d)	↑	h	h	h(d)	X	count	(b)
Hold (do nothing)	h(d)	X	l(c)	X	h(d)	X	q_n	(b)
	h(d)	X	X	l(c)	h(d)	X	q_n	L

H = HIGH voltage level steady state
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

NOTES
(b) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HLLH for "162").
(c) The HIGH-to-LOW transition of CEP or CET on the 54/74162 should only occur while CP is HIGH for conventional operation.
(d) The LOW-to-HIGH transition of $\overline{PE}$ or $\overline{SR}$ on the 54/74162 should only occur while CP is HIGH for conventional operation.

74162



V_{CC} = Pin 16
GND = Pin 8

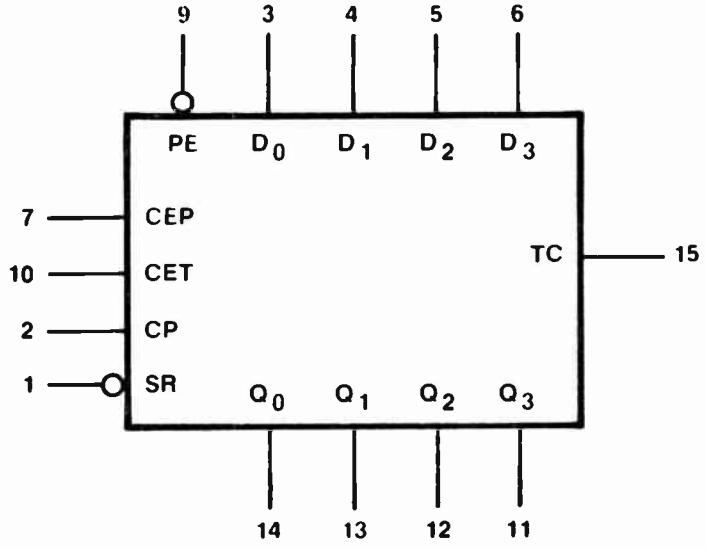
74162

74163 4-BIT BINARY COUNTER

The "163" is a high-speed 4-bit binary counter. The counters are positive edge-triggered, synchronously presettable and are easily cascaded to n-bit synchronous applications without additional gating. A terminal count output is provided which detects a count of HHHH. The synchronous reset is edge-triggered. It overrides all other control inputs, but is active only during the rising clock edge.

Refer to 74160 for a further explanation of binary counters.

	74LS	74
Count Frequency (MHz)	25	25
Parallel Load	Synchronous	Synchronous
Clear	Synchronous-Low	Synchronous-Low
Typ. Total Power (mW)	93	305



V_{CC} = Pin 16
GND = Pin 8

74163

MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (Clear)	l	↑	X	X	X	X	L	L
Parallel Load	h(d)	↑	X	X	l	l	L	L
	h(d)	↑	X	X	l	h	H	(b)
Count	h(d)	↑	h	h	h(d)	X	count	(b)
Hold (do nothing)	h(d)	X	l(c)	X	h(d)	X	q_n	(b)
	h(d)	X	X	l(c)	h(d)	X	q_n	L

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

NOTES

(b) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HHHH for "163").

(c) The HIGH-to-LOW transition of CEP or CET on the 54/74163 should only occur while CP is HIGH for conventional operation

(d) The LOW to HIGH transition of $\overline{PE}$ or $\overline{SR}$ on the 54 74163 should only occur while CP is HIGH for conventional operation

74163

74164 8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER

The "164" is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data are entered serially through one of two inputs (D_{sa} or D_{sb}). Either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shift one place to the right on each LOW-to-HIGH transition of the clock (CP) input, and enter into Q_0 the logical AND of the two data inputs ($D_{sa} \cdot D_{sb}$) that existed one setup time before the rising clock edge. A LOW level on the master reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

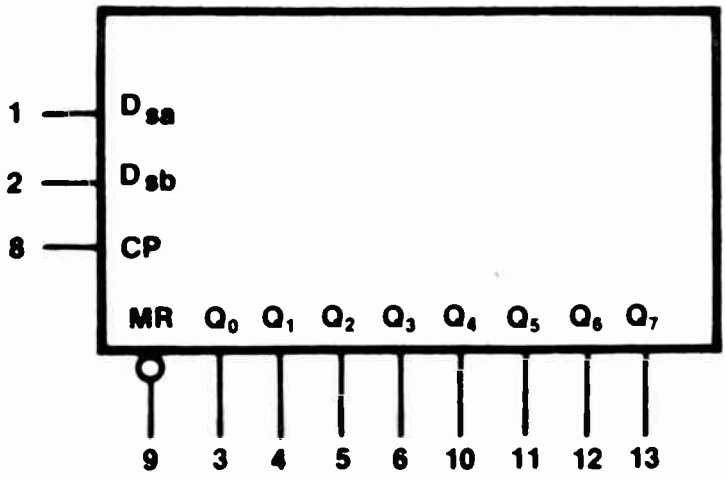
	74LS	74	74L
Shift Frequency (MHz)	25	25	6
Serial Data Input	Gated D	GatedD	Gated D
Asynchronous Clear	Low	Low	Low
Shift-Right Mode	Yes	Yes	Yes
Shift-Left Mode	No	No	No
Load	No	No	No
Hold	No	No	No
Typ. Total Power (mW)	80	175	30

Truth Table

OPERATING MODE	INPUTS				OUTPUTS		
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	Q_1 -	Q_7
Reset (Clear)	L	X	X	X	L	L -	L
Shift	H	↑	l	l	L	q_0 -	q_6
	H	↑	l	h	L	q_0 -	q_6
	H	↑	h	l	L	q_0 -	q_6
	H	↑	h	h	H	q_0 -	q_6

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
q = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
x = Don't care.
↑ LOW-to-HIGH clock transition

74164



V_{CC} = Pin 14
GND = Pin 7

74164

74165 8-BIT SERIAL/PARALLEL-IN, SERIAL-OUT SHIFT REGISTER

The "165" is an 8-bit parallel load or serial-in shift register with complementary serial outputs (Q_7 and $\overline{Q}_7$) available from the last stage. When the parallel load ($\overline{PL}$) input is LOW, parallel data from the D_0-D_7 inputs are loaded into the register asynchronously. When the $\overline{PL}$ input is HIGH, data enter the register serially at the Ds input and shift one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. This feature allows parallel to serial converter expansion by tying the Q_7 output to the Ds input of the succeeding stage.

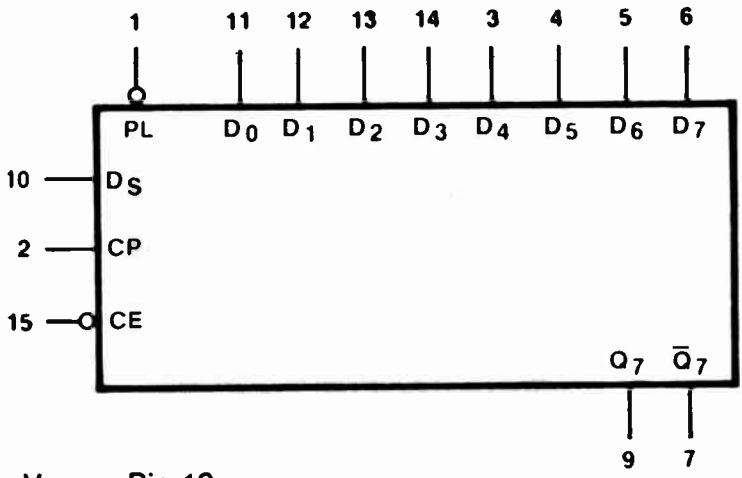
The clock input is a gated OR structure that allows one input to be used as an active LOW clock enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of the $\overline{CE}$ input should only take place while the CP is HIGH for predictable operation. Also, the CP and $\overline{CE}$ inputs should be LOW before the LOW-to-HIGH transition of $\overline{PL}$ to prevent shifting the data when $\overline{PL}$ is released.

	74
Shift Frequency (MHz)	**25**
Serial Data Input	**D**
Asynchronous Clear	**None**
Shift-Right Mode	**Yes**
Shift Left Mode	**No**
Load	**Yes**
Hold	**Yes**
Typ. Total Power (mW)	**200**

MODE SELECT - FUNCTION TABLE

OPERATING MODES	INPUTS					Q_n REGISTER		OUTPUTS	
	$\overline{PL}$	$\overline{CE}$	CP	D_S	D_0 - D_7	Q_0	Q_1 - Q_6	Q_7	$\overline{Q}_7$
Parallel Load	L	X	X	X	L	L	L - L	L	H
	L	X	X	X	H	H	H - H	H	L
Serial Shift	H	L	↑	l	X	L	q_0 - q_5	q_6	$\overline{q}_6$
	H	L	↑	h	X	H	q_0 - q_5	q_6	$\overline{q}_6$
Hold "Do Nothing"	H	H	X	X	X	q_0	q_1 - q_6	q_7	$\overline{q}_7$

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
q_n = Lower case letters indicate the state of the referenced output one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.



V_{CC} = Pin 16
GND = Pin 8

74165

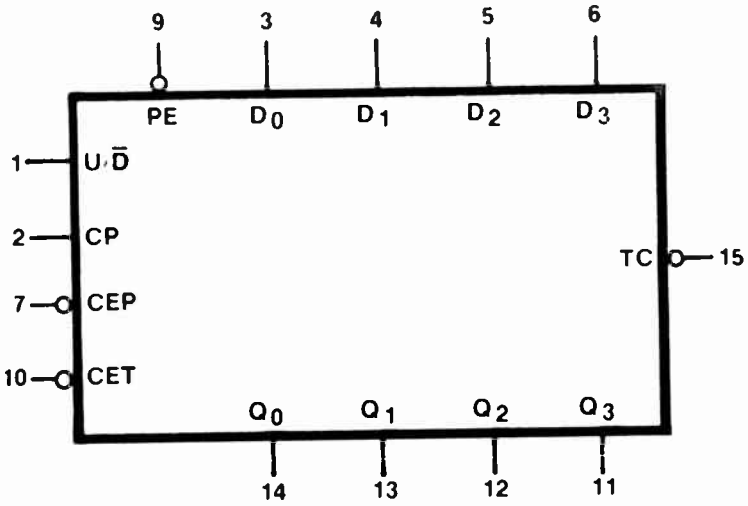
74166 8-BIT SERIAL/PARALLEL-IN, SERIAL-OUT SHIFT REGISTER

The "166" is an 8-bit shift register that has fully synchronous serial or parallel data entry selected by an active LOW parallel enable ($\overline{PE}$) input. When the $\overline{PE}$ is LOW one setup time before the LOW-to-HIGH clock transition, parallel data are entered into the register. When $\overline{PE}$ is HIGH, data are entered into internal bit position Q_0 from serial data input (D_S), and the remaining bits are shifted one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$) with each positive-going clock transition. For expansion of the register in parallel to serial converters, the Q_7 output is connected to the Ds input of the succeeding stage.

The clock input is a gated OR structure that allows one input to be used as an active LOW clock enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The Low-to HIGH transition of $\overline{CE}$ input should only take place while the CP is HIGH for predictable operation.

A LOW on the master reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

	74
Shift Frequency (MHz)	**20**
Serial Data Input	**D**
Asynchronous Clear	**Low**
Shift-Right Mode	**Yes**
Shift-Left Mode	**No**
Load	**Yes**
Hold	**Yes**
Typ. Total Power (mW)	**360**



V_{CC} = Pin 16
GND = Pin 8

74166

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$
Parallel Load	↑ ↑	X X	X X	X X	l l	l h	L H	(b) (b)
Count Up	↑	h	l	l	h	X	Count Up	(b)
Count Down	↑	l	l	l	h	X	Count Down	(b)
Hold (do nothing)	↑ ↑	X X	h X	X h	h h	X X	q_n q_n	(b) H

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

NOTE

b. The $\overline{TC}$ is LOW when $\overline{CET}$ is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLH), and Terminal Count Down is (LLLL).

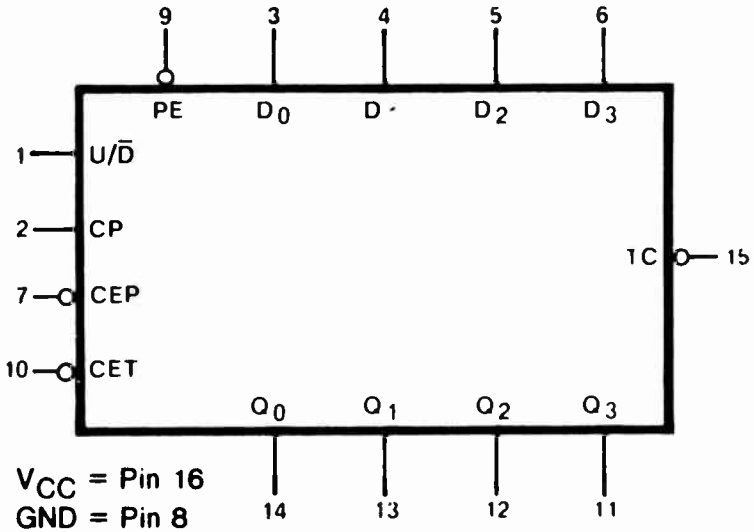
74168 4-BIT UP/DOWN SYNCHRONOUS COUNTER

The "168" is a synchronous presettable BCD decade up/down counter featuring an internal carry lookahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the flip-flops on the LOW-to-HIGH transition of the clock.

The counter is fully programmable; that is, the outputs may be present to either level. Presetting is synchronous with the clock and takes place regardless of the levels of the count-enable inputs. A LOW level on the parallel enable ($\overline{PE}$) input disables the counter and causes the data at the D_n inputs to be loaded into the counter on the next LOW-to-HIGH transition of the clock. The direction of counting is controlled by the up/down ($U/\overline{D}$) input; a HIGH will cause the count to increase, and a LOW will cause the count to decrease.

The carry lookahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs ($\overline{CET}$•$\overline{CEP}$) and a terminal count ($\overline{TC}$) output. Both count-enable inputs must be LOW to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output, thus enabled, will produce a LOW output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This LOW level $\overline{TC}$ pulse is used to enable successive cascaded stages. The fast synchronous multistage counting connections are shown here.

	74LS
Count Frequency (MHz)	**25**
Parallel Load	**Synchronous**
Clear	**None**
Typ. Total Power (mW)	**100**



74168

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$
Parallel Load	↑	X	X	X	l	l	L	(b)
	↑	X	X	X	l	h	H	(b)
Count Up	↑	h	l	l	h	X	Count Up	(b)
Count Down	↑	l	l	l	h	X	Count Down	(b)
Hold (do nothing)	↑	X	h	X	h	X	q_n	(b)
	↑	X	X	h	h	X	q_n	H

H = HIGH voltage level steady state.
L = LOW voltage level steady state
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

NOTE

b. The $\overline{TC}$ is LOW when $\overline{CET}$ is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLH), and Terminal Count Down is (LLLL)

74168

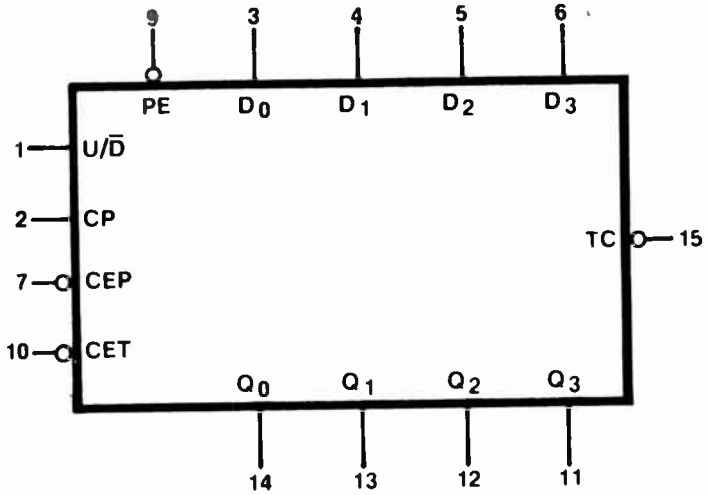
74169 4-BIT UP/DOWN SYNCHRONOUS COUNTER

The "169" is a synchronous presettable modulo 16 binary up/down counter featuring an internal carry lookahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change conincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the flip-flops on the LOW-to-HIGH transition of the clock.

The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock and takes place regardless of the levels of the count enable inputs. A LOW level on the parallel enable ($\overline{PE}$) input disables the counter and causes the data at the D_n inputs to be loaded into the counter on the next LOW-to-HIGH transition of the clock. The direction of counting is controlled by the up/down ($U/\overline{D}$) input. A HIGH will cause the count to increase, and a LOW will cause the count to decrease.

The carry lookahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs ($\overline{CEP}$•$\overline{CEP}$) and a terminal count ($\overline{TC}$) output. Both count-enable inputs must be LOW to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output, thus enabled, will produce a LOW output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This LOW level $\overline{TC}$ pulse is used to enable successive cascaded stages. See 74168 for the fast synchronous multistage counting connections.

	74LS
Count Frequency (MHz)	**25**
Parallel Load	**Synchronous**
Clear	**None**
Typ. Total Power (mW)	**100**



V_{CC} = Pin 16
GND = Pin 8

74169

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$
Parallel Load	↑ ↑	X X	X X	X X	l l	l h	L H	(b) (b)
Count Up	↑	h	l	l	h	X	Count Up	(b)
Count Down	↑	l	l	l	h	X	Count Down	(b)
Hold (do nothing)	↑ ↑	X X	h X	X h	h h	X X	q_n q_n	(b) H

H = HIGH voltage level steady state
L = LOW voltage level steady state
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition

↑ = LOW-to-HIGH clock transition

NOTE

b. The $\overline{TC}$ is LOW when $\overline{CET}$ is LOW and the counter is at Terminal Count. Terminal Count up is (HHHH) and Terminal Count Down is (LLLL).

74169

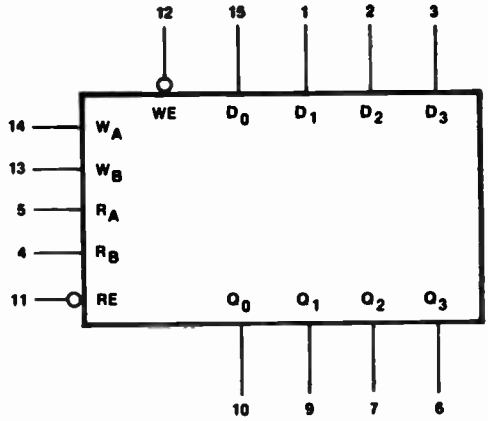
74170 4 × 4 REGISTER FILE (O.C.)

The "170" is a 16-bit register file organized as 4 words of 4 bits each. This permits simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four data inputs. The write address inputs (W_A and W_B) determine the location of the stored word. When the write enable ($\overline{WE}$) input is LOW, data are entered into the addressed location. The addressed location remains transparent to the data while the $\overline{WE}$ is LOW. Data supplied at the inputs will be read out in true (non inverting) form. Data and write address inputs are inhibited when $\overline{WE}$ is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual read address inputs (R_A and R_B). The addressed word appears at the four outputs when the read enable ($\overline{RE}$) is LOW. Data outputs are inhibited and remain HIGH when the read enable input is HIGH. This permits simultaneous reading and writing, eliminates recovery times and is limited in speed only by the read time and the write time.

Up to 256 devices can be stacked to increase the word size to 1024 locations by tying the open collector outputs together. Parallel expansion to generate n-bit words is accomplished by driving the enable and address inputs of each device in parallel.

	74LS	74
Typ. Address Time (ns)	27	30
Typ. Read Enable Time (ns)	15	15
Data Input Rate (MHz)	20	20
Typ. Total Power (mW)	125	635



V_{CC} = Pin 16
GND = Pin 8

74170

WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES(b)
	WE	D_n	
Write Data	L	L	L
	L	H	H
Data Latched	H	X	no change

NOTE

b. The Write Address (W_A & W_B) to the "internal latches" must be stable while $\overline{WE}$ is LOW for conventional operation.

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUTS
	$\overline{RE}$	INTERNAL LATCHES(c)	Q_n
Read	L	L	L
	L	H	H
Disabled	H	X	H

NOTE

c. The Read Address (R_A & R_B) changes to select the "internal latches" are not constrained by $\overline{WE}$ or $\overline{RE}$ operation.

H = HIGH voltage level
L = LOW voltage level
X = Don't care

74170

The "172" is a high performance 16-bit multiport register file with three-state outputs organized as eight words of two bits each. Multiple address decoding circuitry is used so that the read and write operation can be performed independently on up to 3-word locations. Data can be written into 2-word locations through input port A or input port C while data is simultaneously read from both output port B and output port C.

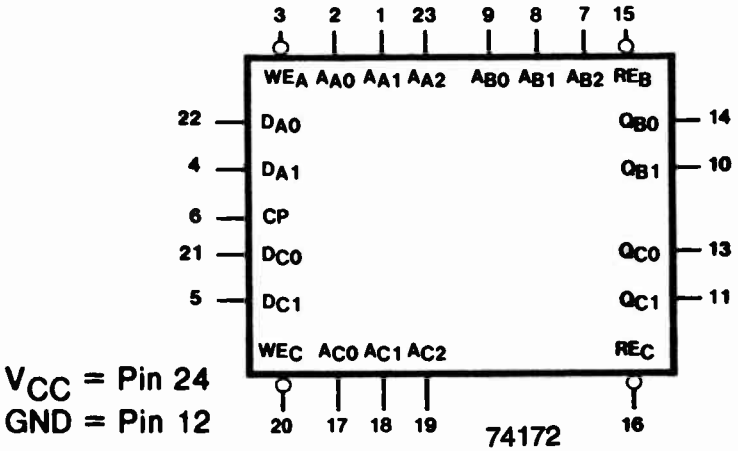
Port A is an input port that can be used to write two bits of data (D_{A0} and D_{A1}) into one of eight register locations selected by the address inputs (A_{A0}, A_{A1} and A_{A2}). When the write enable ($\overline{WE}_A$) input is LOW one setup time prior to the LOW-to-HIGH transition of the Clock (CP) input, the data is written into the selected location.

Port B is an output port that can be used to read two bits of data from one of eight register locations selected by the address inputs (A_{B0}, A_{B1} and A_{B2}). When the read enable ($\overline{RE}_B$) is LOW, the selected 2-bit word appears on outputs Q_{B0} and Q_{B1}. When $\overline{RE}_B$ is HIGH. the Q_{B0} and Q_{B1} outputs are in the high-impedance off state. The read operation is independent of the clock.

Port C is a read/write port that has separate data input and data output sections, but common address inputs (A_{C0}, A_{C1} and A_{C2}). Data can be simultaneously written into and read from the same register location. Port C can be used to write data into one location while port A is writing into a different location but data cannot be written reliably into the same location simultaneously. If both ports A and C are enabled for writing into the same location during the same clock cycle, the LOW data will predominate if there is a conflict.

The register operation is essentially a master-slave flip-flop. Each master acts as a transparent D latch when selected by the A or C address and the clock and applicable write enable are LOW. The data in the master is transferred to the slave (or output section) following the LOW-to-HIGH transi-

tion of the clock (CP). The address inputs must be stable while the clock and write enable inputs are LOW to ensure retention of data previously written into the other locations. Any number of masters can be altered while the clock and write enable are LOW, but the new data will not be loaded into the slaves or be available at the outputs until the clock goes HIGH.



WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS			ADDRESSED REGISTER
	CP	$\overline{WE}$	D_n	
Write Data[b]	↑	l	l	L
	↑	l	h	H
Hold[c]	↓	h	X	no change

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUTS
	$\overline{RE}$	ADDRESSED REGISTER	Q_n
Read	L	L	L
	L	H	H
Disabled	H	X	(Z)

H = HIGH voltage level steady state
h = HIGH voltage level one setup time prior to the LOW-to-HIGH or HIGH-to-LOW clock transition.
L = LOW voltage level steady state
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
(Z) = High impedance "off" state
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

NOTE

b. The Write Address (A_A & A_C) to the "internal register" must be stable while $\overline{WE}$ and CP are LOW for conventional operation.

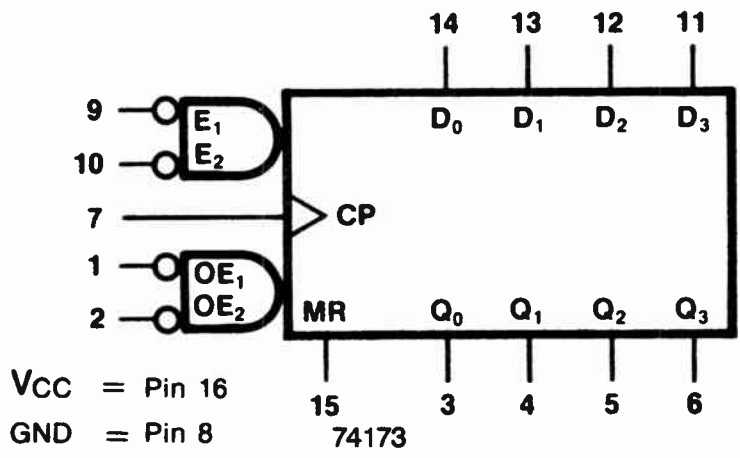
c. The Write Enable must be HIGH before the HIGH-to-LOW Clock transition to ensure that the data in the register is not changed.

74173 QUAD D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

The "173" is a 4-bit parallel load register with clock enable control, 3-state buffered outputs and master reset. When the two clock enable ($\overline{E}_1$ and $\overline{E}_2$) inputs are LOW, data on the D inputs are loaded into the register synchronously with the LOW-to-HIGH clock (CP) transition. When one or both $\overline{E}$ inputs are HIGH one setup time before the LOW-to-HIGH clock transition, the register will retain the previous data. The data inputs and clock enable inputs are fully edge-triggered and must be stable only one setup time before the LOW-to-HIGH clock transition. The master reset (MR) is an active HIGH asynchronous input. When the MR is HIGH, all four flip-flops are reset (cleared) independently of any other input condition.

The 3-state output buffers are controlled by a 2-input NOR gate. When both output enable ($\overline{OE}_1$ and $\overline{OE}_2$) inputs are LOW, the data in the register is presented at the Q outputs. When one or both $\overline{OE}$ inputs is HIGH, the outputs are forced to a high-impedance off state. The 3-state output buffers are completely independent of the register operation. The OE transitions do no affect the clock and reset operations.

	74
Frequency (MHz)	25
Asynchronous Clear	High
Typ. Total Power (mW)	250



VCC = Pin 16
GND = Pin 8

MODE SELECT—FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS
	MR	CP	$\overline{E}_1$	$\overline{E}_2$	D_n	Q_n (Register)
Reset (clear)	H	X	X	X	X	L
Parallel Load	L	↑	l	l	l	L
	L	↑	l	l	h	H
Hold (No change)	L	X	h	X	X	q_n
	L	X	X	h	X	q_n

3-STATE BUFFER OPERATING MODES	INPUTS			OUTPUTS
	Q_n (Register)	$\overline{OE}_1$	$\overline{OE}_2$	Q_0, Q_1, Q_2, Q_3
Read	L	L	L	L
	H	L	L	H
Disabled	X	H	X	(Z)
	X	X	H	(Z)

NOTES

H HIGH voltage level
h HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L LOW voltage level
l LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
q_n Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition
X Don't care
(Z) High impedance "off" state
↑ LOW-to-HIGH transition

74173

74174 HEX D FLIP-FLOP

The "174" has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously. The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding Q output of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

	74S	74LS	74
Frequency (MHz)	75	30	25
Asynchronous Clear	Low	Low	Low
Typ. Total Power (mW)	450	80	225

MODE SELECT-FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = HIGH voltage level steady state

h = HIGH voltage level one setup time prior to the LOW to HIGH clock transition

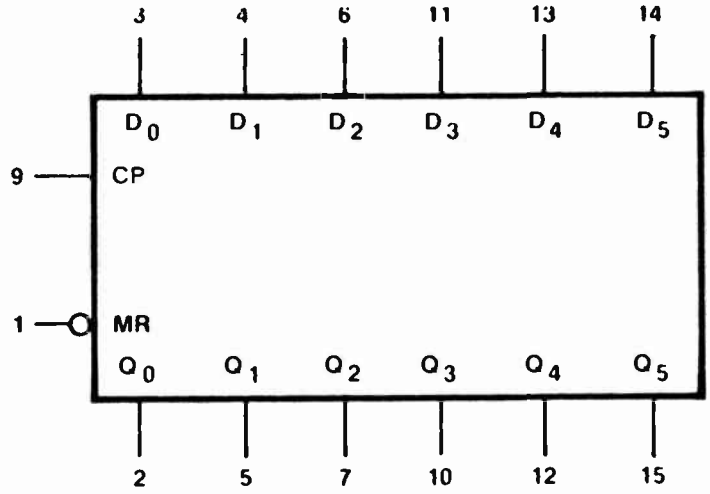
L = LOW voltage level steady state

l = LOW voltage level one setup time prior to the LOW to HIGH clock transition

X = Don't care

↑ = LOW-to-HIGH clock transition

74174



V_{CC} = Pin 16
GND = PIN 8

74174

74175 QUAD D FLIP-FLOP

The "175" is a quad edge-triggered D-type flip-flop with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding Q output of the flip-flop.

All Q outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where both true and complement outputs are required, and the clock and master reset are common to all storage elements.

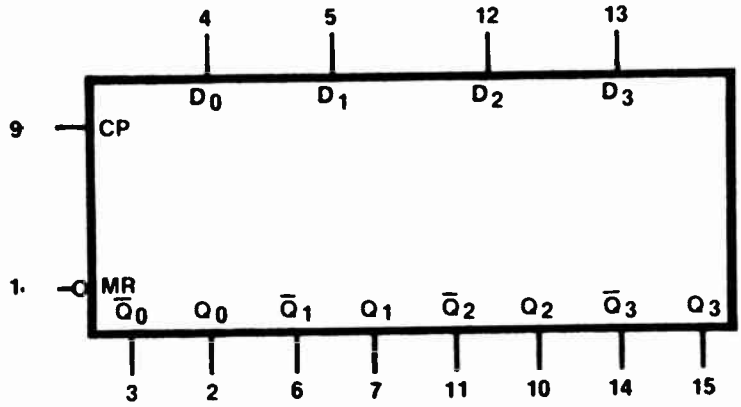
	74S	74LS	74
Frequency (MHz)	75	30	25
Asynchronous Clear	Low	Low	Low
Typ. Total Power (mW)	300	55	150

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
Reset (clear)	L	X	X	L	H
Load "1"	H	↑	h	H	L
Load "0"	H	↑	l	L	H

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

74175



V_{CC} = Pin 16
GND = Pin 8

74175

74180 9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

The "180" is a 9-bit parity generator or checker commonly used to detect errors in high-speed data transmission or data retrieval systems. Both even and odd parity enable inputs and parity outputs are available for generating or checking parity on 9-bits.

True active HIGH or true active LOW parity can be generated at both the even and odd outputs. True active HIGH parity is established with even parity enable input (P_E) set HIGH and the odd parity enable input (P_O) set LOW. True active LOW parity is established when P_E is LOW and P_O is HIGH. When both enable inputs are at the same logic level, both outputs will be forced to the opposite logic level.

Parity checking of a 9-bit word (8-bit plus parity) is possible by using the two enable inputs plus an inverter as the ninth data input. To check for true active HIGH parity, the ninth data input is tied to the P_O input and an inverter is connected between the P_O and P_E inputs. To check for true active LOW parity, the ninth data input is tied to the P_E input and an inverter is connected between the P_E and P_O inputs.

Expansion to larger word sizes is accomplished by serially cascading the "180" in 8-bit increments. The even and odd parity outputs of the first stage are connected to the corresponding P_E and P_O inputs, respectively, of the succeeding stage.

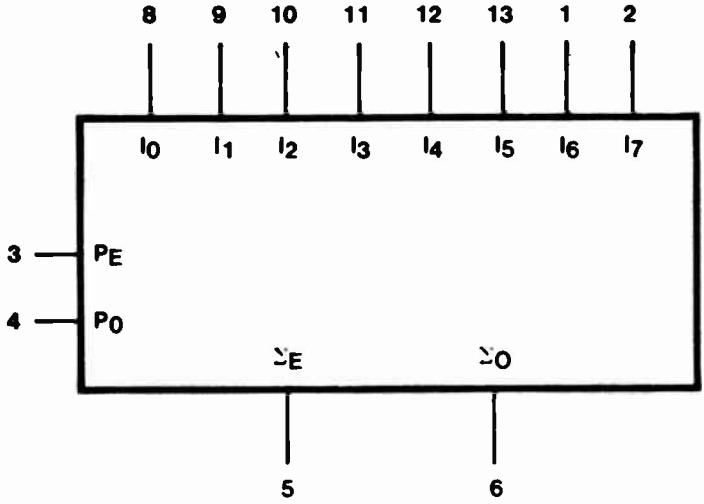
	74
Typ. Delay Time (ns)	35
Typ. Total Power (mW)	170

Truth Table

INPUTS			OUTPUTS	
Number of HIGH Data Inputs (I_0-I_7)	P_E	P_O	Σ_E	Σ_O
Even	H	L	H	L
Odd	H	L	L	H
Even	L	H	L	H
Odd	L	H	H	L
X	H	H	L	L
X	L	L	H	H

74180

H = HIGH voltage level
L = LOW voltage level
X = Don't care



V_{CC} = 14
GND = Pin 7

74180

The "181" is a 4-bit high-speed parallel arithmetic logic unit (ALU). Controlled by the four function select inputs ($S_0 \ldots S_3$) and the mode control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The function table shown here lists these operations.

When the mode control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the mode control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry look ahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry look ahead between packages using the signals $\overline{P}$ (carry propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the carry output (C_{n+4}) signal to the carry input (C_n) of the next unit. For high-speed operation, the device is used in conjunction with the "182" carry look ahead circuit. One carry look ahead package is required for each group of four "181" devices. Carry look ahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

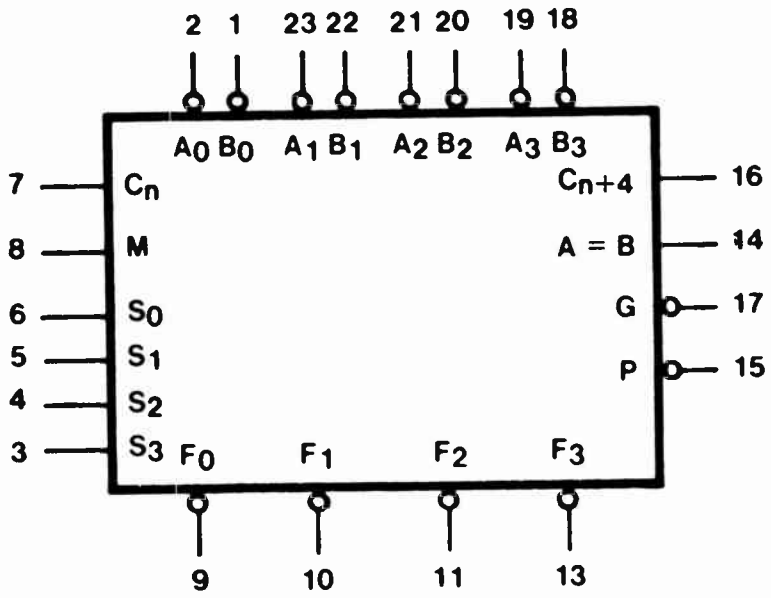
The A=B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A=B output is open collector and can be wired-AND with other A=B outputs to give a comparison for more than four bits. The A=B signal can also be used with the C_{n+4} signal to indicate A>B and A<B.

The function table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because sub-

traction is actually performed by complementary addition (1s complement), a carry out means borrow; thus, a carry is generated when there is no underflow and no carry is generated when there is there is underflow.

This device can be used with either active LOW inputs producting active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case, the table lists the operations that are performed to the operands labeled inside the logic symbol.

	74
Typ. Carry Time (ns)	12.5
Typ. Add Time (ns)	24
Typ. Total Power (mW)	455



V_{CC} = Pin 24
GND = Pin 12

74181

MODE SELECT—FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE HIGH INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A
L	L	L	H	$\overline{A + B}$	A + B
L	L	H	L	$\overline{A}B$	A + $\overline{B}$
L	L	H	H	Logical 0	minus 1
L	H	L	L	$\overline{AB}$	A plus A$\overline{B}$
L	H	L	H	$\overline{B}$	(A + B) plus A$\overline{B}$
L	H	H	L	$A \oplus B$	A minus B minus 1
L	H	H	H	A$\overline{B}$	AB minus 1
H	L	L	L	$\overline{A} + B$	A plus AB
H	L	L	H	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	(A + $\overline{B}$) plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	Logical 1	A plus A*
H	H	L	H	A + $\overline{B}$	(A + B) plus A
H	H	H	L	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A minus 1

74181

*Each bit is shifted to the next more significant position

**Arithmetic operations expressed in 2s complement notation

L = LOW voltage level

H = HIGH voltage level

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS	
				LOGIC	ARITHMETIC**
S_3	S_2	S_1	S_0	(M = H)	(M = L) (C_n = L)
L	L	L	L	$\overline{A}$	A minus 1
L	L	L	H	$\overline{AB}$	AB minus 1
L	L	H	L	$\overline{A} + B$	$A\overline{B}$ minus 1
L	L	H	H	Logical 1	minus 1
L	H	L	L	$\overline{A + B}$	A plus $(A + \overline{B})$
L	H	L	H	$\overline{B}$	AB plus $(A + \overline{B})$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1
L	H	H	H	$A + \overline{B}$	$A + \overline{B}$
H	L	L	L	$\overline{A}B$	A plus (A + B)
H	L	L	H	$A \oplus B$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)
H	L	H	H	A + B	A + B
H	H	L	L	Logical 0	A plus A*
H	H	L	H	$A\overline{B}$	AB plus A
H	H	H	L	AB	$A\overline{B}$ plus A
H	H	H	H	A	A

74181

*Each bit is shifted to the next more significant position

**Arithmetic operations expressed in 2s complement notation

L = LOW voltage level

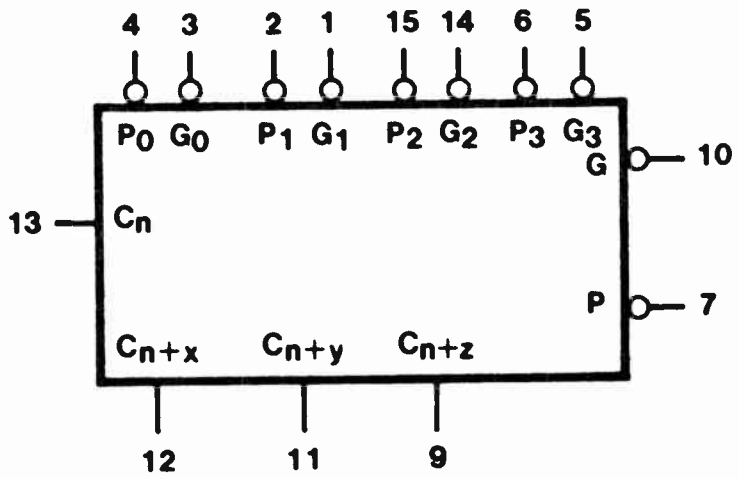
H = HIGH voltage level

74182 LOOK AHEAD CARRY GENERATOR

The "182" carry look ahead generator accepts up to four pairs of active LOW carry propogate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$ and $\overline{P}_3$) and carry generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$ and $\overline{G}_3$) signals and an active HIGH carry input (C_n) and provides anticipated active HIGH carries (C_{n+x} $C_n + y$ C_{n+z}) across four groups of binary adders. The "182" also has active LOW carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs that may be used for further levels of look ahead.

Also, the"182" can also be used with binary ALUs in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry look ahead generator are identical in both cases.

	74S	74
Typ. Carry Time (ns)	7	13
Typ. Total Power (mW)	260	180



V_{CC} = Pin 16
GND = Pin 8

74182

Truth Table

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	H	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

74182

The "189" is a high-speed array of 64 memory cells organized as 16 words of four bits each. A 1-of-16 address decoder selects a single word that is specified by the four address inputs (A_0–A_3). A READ operation is initiated after the address lines are stable when the write enable ($\overline{WE}$) input is HIGH and the chip select-memory enable ($\overline{CS}$) input is LOW. Data is read at the outputs inverted from the data that were written into the memory.

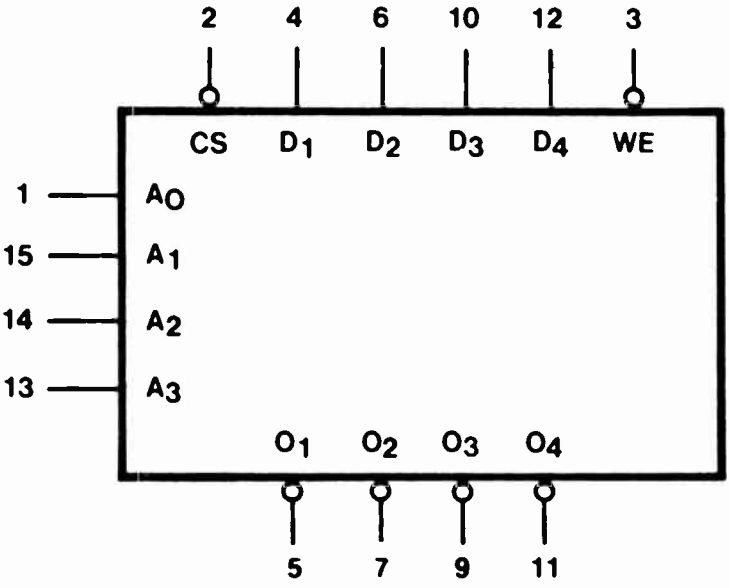
A WRITE operation requires that the $\overline{WE}$ and $\overline{CS}$ inputs be LOW. The address inputs must be stable during the WRITE mode for predictable operation. When the write mode is selected the outputs are in the high-impedance off state, the selected memory cells are transparent to changes in the data during the WRITE mode. Therefore, data must be stable one setup time before the LOW-to- HIGH transition of $\overline{CE}$ or $\overline{WE}$.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{CS}$	$\overline{WE}$	D_n	$\overline{O}_n$
Write - Disable Outputs	L	L	L	(Z)
	L	L	H	(Z)
Read	L	H	X	$\overline{Data}$
Store - Disable Outputs	H	X	X	(Z)

74189

H = HIGH voltage level
L = LOW voltage level
X = Don't care
$\overline{Data}$ = Read complement of data from addressed word location
(Z) = High impedance "off" state



74189

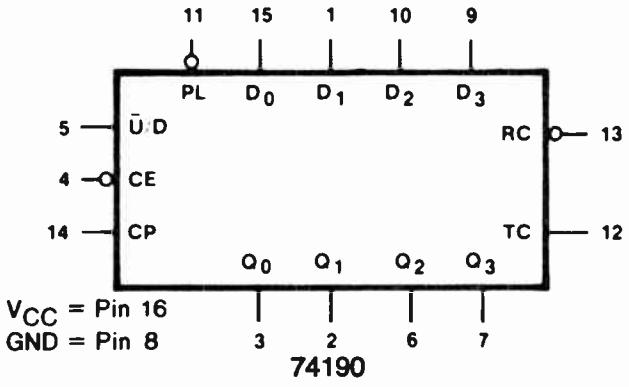
74190 PRESETTABLE BCD/DECADE UP/DOWN COUNTER

The "190" is an asynchronously presettable up/down BCD decade counter. It contains four master-slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous countup and countdown operations.

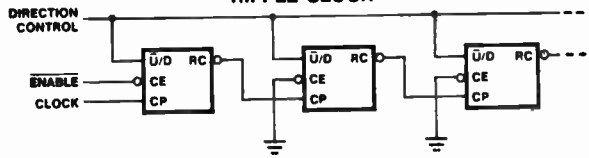
Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel data inputs ($D_0 - D_3$) is loaded into the counter and appears on the outputs when the parallel load ($\overline{PL}$) input is LOW. As indicated in the mode select table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the count enable ($\overline{CE}$) input. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The up/down ($\overline{U}/D$) input signal determines the direction of counting as indicated in the mode select table. The $\overline{CE}$ input may go LOW when the clock is in either state; however, the LOW-to-HIGH $\overline{CE}$ transition must occur only while the clock is HIGH. Also, the $\overline{U}/D$ input should be changed only when either $\overline{CE}$ or CP is HIGH.

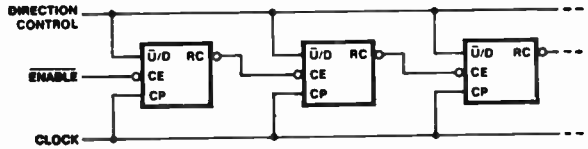
	74LS	74
Count Frequency (MHz)	20	20
Parallel Load	Asynchronous	Asynchronous
Clear	None	None
Typ. Total Power (mW)	100	325



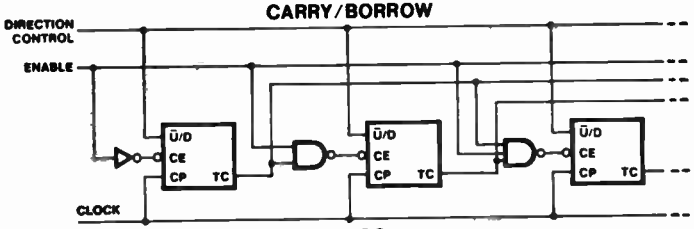
N-STAGE COUNTER USING RIPPLE CLOCK **Figure A**



SYNCHRONOUS N-STAGE COUNTER USING RIPPLE CARRY/BORROW **Figure B**



SYNCHRONOUS N-STAGE COUNTER WITH PARALLEL GATED CARRY/BORROW **Figure C**



74190

MODE SELECT-FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	Ū/D	$\overline{CE}$	CP	D_n	Q_n
Parallel load	L L	X X	X X	X X	L H	L H
Count up	H	L	⌊	⌈	X	count up
Count down	H	H	⌊	⌈	X	count down
Hold "do nothing"	H	X	H	X	X	no change

TC AND $\overline{RC}$ TRUTH TABLE

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
Ū/D	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	X	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⌐⌊	H	X	X	H	H	⌐⌊
L	X	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⌐⌊	L	L	L	L	H	⌐⌊

74190

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
⌊ = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
⌈ = LOW-to-HIGH clock transition.
⌐⌊ = LOW pulse.

74191 PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

The "191" is an asynchronously presettable up/down 4-bit binary counter. It contains four master-slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous countup and countdown operation.

Asynchronous parallel load capability permits the counter to be preset to any desired number, information present on the parallel data inputs ($D_0 - D_3$) is loaded into the counter and appears on the outputs when the parallel load ($\overline{PL}$) input is LOW. As indicated in the mode select table, this operation overrides the counting function.

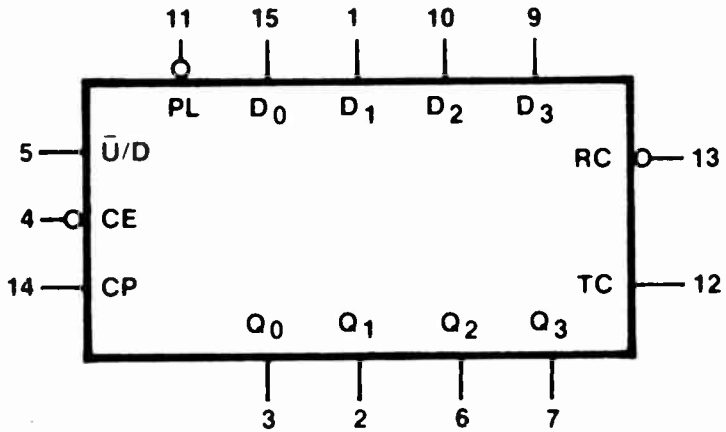
Counting is inhibited by a HIGH level on the count enable ($\overline{CE}$) input. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The up/down ($\overline{U}/D$) input signal determines the direction of counting as indicated in the mode select table. The $\overline{CE}$ input may go LOW when the clock is in either state; however, the LOW-to-HIGH $\overline{CE}$ transition must occur only while the clock is HIGH. Also, the $\overline{u}$/d input should be changed only when either $\overline{CE}$ or CP is HIGH.

	74LS	74
Count Frequency (MHz)	20	20
Parallel Load	Asynchronous	Asynchrnous
Clear	None	None
Typ. Total Power (mW)	90	325

MODE SELECT-FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U}/D$	$\overline{CE}$	CP	D_n	Q_n
Parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
Count up	H	L	l	↑	X	count up
Count down	H	H	l	↑	X	count down
Hold "do nothing"	H	X	H	X	X	no change

74191



74191

V_{CC} = Pin 16
GND = Pin 8

TC AND $\overline{RC}$ TRUTH TABLE

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
Ū/D	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	X	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊓	H	H	H	H	H	⊓
L	X	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓	L	L	L	L	H	⊓

74191

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't care.
↑ = LOW-to-HIGH clock transition
⊓ = LOW pulse.

The "192" is an asynchronously presettable up/down (reversible) internal gating and steering logic to provide asynchronous master reset (clear), parallel load and synchronous countup and countdown operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on the clock inputs cause the Q outputs to change state synchronously. A LOW-to-HIGH transition on the countdown clock pulse (CP_D) input will decrease the count by one, while a similar transition on the countup clock pulse (CP_U) input will advance the count by one. One clock should be held HIGH while counting with the other, because the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The terminal countup ($\overline{TC}_U$) and terminal countdown ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state of 9, the next HIGH-to-LOW transition of CP_U will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, duplicating the countup clock, although delayed by two gate delays. Likewise, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The $\overline{TC}$ outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, because they duplicate the clock waveforms. Multistage counters will not be fully synchronous, because there is a two-gate delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs ($D_0 - D_3$) is loaded into the counter and appears on the outputs, regardless of the conditions of the clock inputs when the parallel load ($\overline{PL}$) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates,

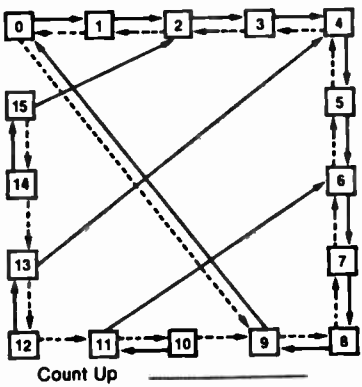
override both clock inputs and set all Q outputs LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

	74LS	74	74L
Count Frequency (MHz)	25	20	6
Parallel Load	Asynchronous	Asynchronous	Asynchronous
Clear	Asynchronous-High	Asynchronous-High	Asynchronous-High
Typ. Total Power (mW)	85	325	40

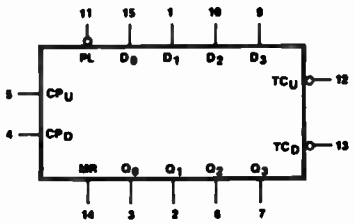
LOGIC EQUATIONS FOR TERMINAL COUNT

$$\overline{TC}_U = Q_0 \cdot Q_3 \cdot \overline{CP}_U$$

$$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$$



74192



74192

V_{CC} = Pin 16
GND = Pin 8

MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS								OUTPUTS					
	MR	PL	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	X	X	H	$Q_n = D_n$				L	H
	L	L	H	X	H	X	X	H	$Q_n = D_n$				H	H
Count up	L	H	↑	H	X	X	X	X	Count up				H[b]	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	H[c]

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition

NOTES:
b. $\overline{TC}_U$ = CP_U at terminal count up (HLLH)
c. $\overline{TC}_D$ = CP_D at terminal count down (LLLL)

74192

74193 PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

The "193" is an asynchronously presettable, up/down (reversible) 4-bit binary counter. It contains four master-slave flip-flops with internal gating and steering logic to provide asynchronous master reset (clear) and parallel load, and synchronous countup and countdown operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on the clock inputs causes the Q outputs to change state synchronously. A LOW-to-HIGH transition on the countdown clock pulse (CP_D) input will decrease the count by one, while a similar transition on the count up clock pulse (CP_U) input will advance the count by one. One clock should be held HIGH while counting with the other, because the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The terminal countup (TC_U) and terminal countdown (TC_D) outputs are normally HIGH. When the circuit has reached the maximum count state of 15, the next HIGH-to-LOW transition of CP_U will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, duplicating the countup clock, although delayed by two gate delays. Likewise, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The $\overline{TC}$ outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, because they duplicate the clock waveforms. Multistage counters will not be fully synchronous for there is a two-gate delay time difference added for each stage that is added.

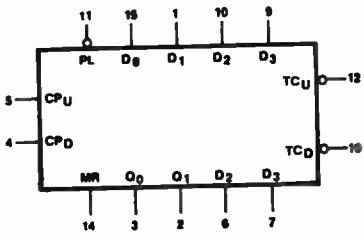
The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D_0 – D_3) is loaded into the counter and appears on the outputs, regardless of the conditions of the clock inputs when the parallel load ($\overline{PL}$) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all Q outputs LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

	74LS	74	74L
Count Frequency (MHz)	25	20	6
Parallel Load	Asynchronous	Asynchronous	Asynchronous
Clear	Asynchronous-High	Asynchronous-High	Asynchrnous-High
Typ. Total Power (mW)	85	325	40

LOGIC EQUATIONS FOR TERMINAL COUNT

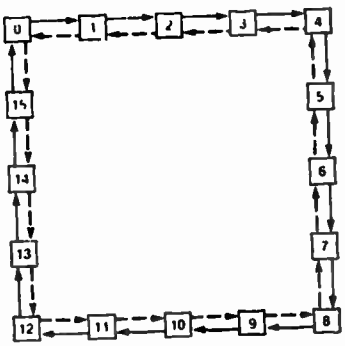
$$\overline{TC}_U = Q_0\ Q_1\ Q_2\ Q_3\ \overline{CP_U}$$

$$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1\ \overline{Q}_2\ \overline{Q}_3 \cdot \overline{CP_D}$$



V_{CC} = Pin 16
GND = Pin 8

74193



Count Up ——————
Count Down – – – – –

74193

MODE SELECT-FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS		
	MR	$\overline{PL}$	CP_U	CP_D	D_0,D_1,D_2,D_3	Q_0,Q_1,Q_2,Q_3	$\overline{TC}_U$	$\overline{TC}_D$
Reset (clear)	H	X	X	L	X X X X	L L L L	H	L
	H	X	X	H	X X X X	L L L L	H	H
Parallel load	L	L	X	L	L L L L	L L L L	H	L
	L	L	X	H	L L L L	L L L L	H	H
	L	L	L	X	H H H H	H H H H	L	H
	L	L	H	X	H H H H	H H H H	H	H
Count up	L	H	↑	H	X X X X	Count up	H[b]	H
Count down	L	H	H	↑	X X X X	Count down	H	H[c]

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition

NOTES
b. $\overline{TC}_U$ = CP_U at terminal count up (HHHH)
c. $\overline{TC}_D$ = CP_D at terminal count down (LLLL)

74193

74194 4-BIT DIRECTIONAL UNIVERSAL SHIFT REGISTER

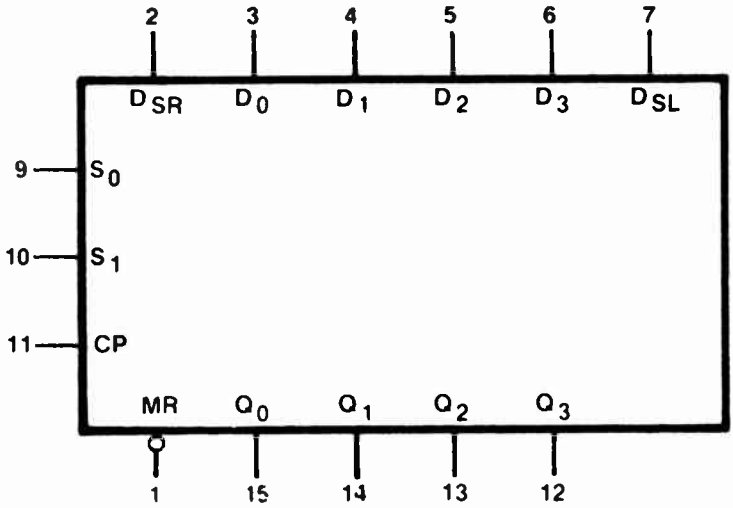
The functional characteristics of the "194" 4-bit bidirectional shift register are indicated in the logic diagram and truth table. The register is full synchronous, with all operations taking place in less than 20 nanoseconds (typical) for the 74 and 74LS, and 12ns (typical) for 74S, making the device especially useful for implementing very high-speed CPUs, or for memory buffer registers.

The "194" design has special logic features that increase the application range. The synchronous operation of the device is determined by two mode select inputs, S_0 and S_1. As shown in the mode select table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.) or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.) or parallel data can be entered, loading all four bits of the register simultaneously. When both S_0 and S_1 are LOW, existing data is retained in a hold (do nothing) mode. The interfering with parallel load operation.

Mode select and data inputs on the 74S194 and 74LS194A are edge-triggered, responding only to the LOW-to-HIGH transition of the clock (CP). Therefore, the only timing restriction is that the mode control and selected data inputs must be stable one setup time prior to the positive transiton of the clock pulse. The mode select inputs of the 74194 are gated with the clock and should be changed from HIGH-to-LOW only while the clock input is HIGH.

The four parallel data inputs ($D_0 - D_3$) are D-type inputs. Data appearing on $D_0 - D_3$ inputs when S_0 and S_1 are HIGH are transferred to the $Q_0 - Q_3$ outputs respectively, following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous master reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs LOW.

	74S	74LS	74
Shift Frequency (MHz)	70	25	25
Serial Data Input	D	D	D
Asynchronous Clear	Low	Low	Low
Shift-Right Mode	Yes	Yes	Yes
Shift-Left Mode	Yes	Yes	Yes
Load	Yes	Yes	Yes
Hold	Yes	Yes	Yes
Typ. Total Power (mW)	450	75	195



V_{CC} = Pin 16
GND = Pin 8

74194

MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS			
	CP	MR	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l(b)	l(b)	X	X	X	q_0	q_1	q_2	q_3
Shift Left	↑	H	h	l(b)	X	l	X	q_1	q_2	q_3	L
	↑	H	h	l(b)	X	h	X	q_1	q_2	q_3	H
Shift Right	↑	H	l(b)	h	l	X	X	L	q_0	q_1	q_2
	↑	H	l(b)	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	↑	H	h	h	X	X	d_n	d_0	d_1	d_2	d_3

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
d_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care
↑ = LOW-to-HIGH clock transition

NOTES
b. The HIGH-to-LOW transition of the S_0 and S_1 inputs on the 54/74194 should only take place while CP is HIGH for conventional operation.

74194

74195 4-BIT PARALLEL ACCESS SHIFT REGISTER

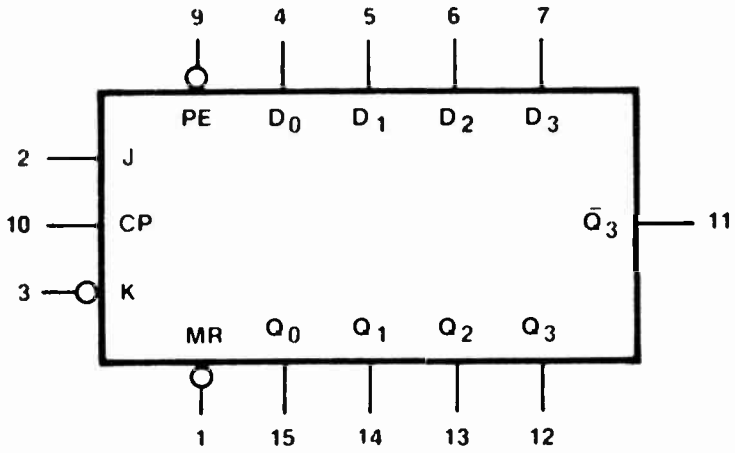
The functional characteristics of the "195" 4-bit parallel-access shift register are indicated in the logic diagram and function table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The "195" operates on two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are both controlled by the state of the parallel enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is HIGH, and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW-to-HIGH clock transition. The J and $\overline{K}$ inputs provide the flexibility of the JK-type input for special applications and, by tying the two pins together, the simple D-type input for general applications. The device appears as four common clocked D flip-flops when the $\overline{PE}$ input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs ($D_0 - D_3$) is transferred to the respective $Q_0 - Q_3$ outputs. Shift left operation ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the D_{n-1} inputs and holding the $\overline{PE}$ input LOW.

All parallel and serial data transfers are synchronous, occuring after each LOW-to-HIGH clock transition. The "195" utilizes edge-triggering; therefore, there is no restriction on the activity of the J, $\overline{K}$, D_n and $\overline{PE}$ inputs for logic operation, other than the setup and release time requirements.

A LOW on the asynchronous master reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition. The $\overline{MR}$ on the 54/74195 is gated with the clock. Therefore, the LOW-to-HIGH $\overline{MR}$ transition should only occur while the clock is LOW to avoid false clocking of the 74195.

	74S	74	74LS
Shift Frequency (MHz)	70	30	30
Serial Data Input	J-$\overline{K}$	J-$\overline{K}$	J-$\overline{K}$
Asynchronous Clear	Low	Low	Low
	74S	**74**	**74LS**
Shift-Right Mode	Yes	Yes	Yes
Shift-Left	No	No	No
Load	Yes	Yes	Yes
Hold	No	No	No
Typ. Total Power (mW)	375	195	70



V_{CC} – Pin 16
GND = Pin 8

74195

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS				
	$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	↑	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset First Stage	H	↑	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle First Stage	H	↑	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain First Stage	H	↑	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel Load	H	↑	l	X	X	d_n	d_0	d_1	d_2	d_3	$\overline{d}_3$

H = HIGH Voltage Level.
L = LOW Voltage Level.
X = Don't care.
l = LOW Voltage level one setup time prior to the LOW-to-HIGH clock transition.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
d_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

74195

74196 PRESETTABLE DECADE RIPPLE COUNTER

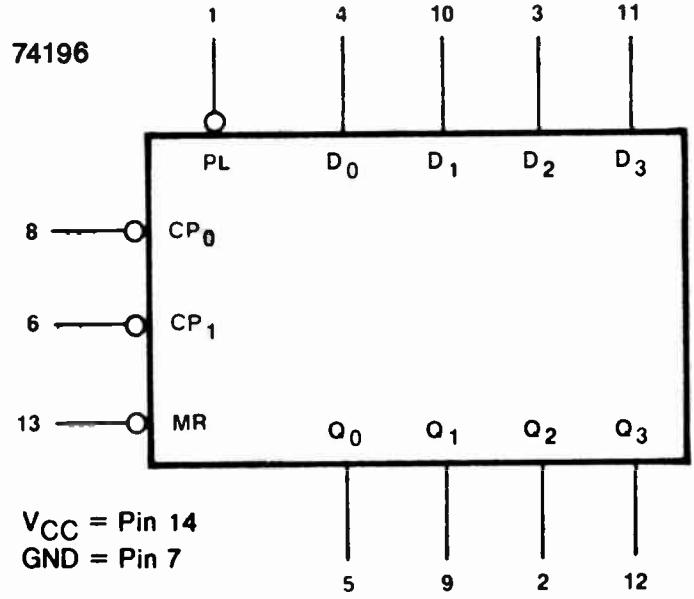
The "196" is an asynchronously presettable decade ripple counter that is partitioned into divide-by-two and divide-by-five sections with each section having a separate clock input. State changes are initiated in the counting modes by the HIGH-to-LOW transition of the clock inputs; however, state changes of the Q outputs do no occur simultaneously because of the internal ripple delays. Designers should keep in mind when using external logic to decode the Q outputs that the unequal delays can lead to spikes, and thus a decoded signal should not be used as a strobe or clock.

The Q_0 flip-flop is triggered by the $\overline{CP_0}$ input, while the $\overline{CP_1}$ input triggers the divide-by-five section. The Q_0 output is designed and specified to drive the rated fanout plus the $\overline{CP_1}$ input.

As indicated in the count sequence tables, the "196" can be connected to operate in two different count sequences. The circuit counts in the BCD (8,4,2,1) sequence with the input connected to $\overline{CP_0}$ and with Q_0 driving $\overline{CP_1}$. Q_0 becomes the low-frequency output and has a 50-percent duty cycle waveform with the input connected to $\overline{CP_1}$ and Q_3 driving $\overline{CP_0}$. The maximum counting rate is reduced in the biquinary configuration because of the interstage gating delay within the divide-by-five section.

The device has an asynchronous active LOW master reset input ($\overline{MR}$) which overrides all other inputs and forces all outputs LOW. The counter is also asynchronously presettable. A LOW on the parallel load input ($\overline{PL}$) overrrides the clock inputs and loads the data from parallel data ($D_0 - D_3$) inputs into the flip-flops. The counter acts as a transparent latch while the $\overline{PL}$ is LOW, and any change in the D_n inputs will be reflected in the outputs.

	74	74LS
Count Frequency (MHz)	50	30
Parallel Load	Yes	Yes
Clear	Low	Low
Typ. Total Power (mW)	240	60



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS
	$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	D_n	Q_n
Reset (Clear)	L	X	X	X	L
Parallel Load	H H	L L	X X	L H	L H
Count	H	H	↓	X	count

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↓ = HIGH-to-LOW Clock Transition

COUNT SEQUENCES

BCD DECADE (b)					BI-QUINARY (c)				
COUNT	Q_3	Q_2	Q_1	Q_0	COUNT	Q_0	Q_3	Q_2	Q_1
0	L	L	L	L	0	L	L	L	L
1	L	L	L	H	1	L	L	L	H
2	L	L	H	L	2	L	L	H	L
3	L	L	H	H	3	L	L	H	H
4	L	H	L	L	4	L	H	L	L
5	L	H	L	H	5	H	L	L	L
6	L	H	H	L	6	H	L	L	H
7	L	H	H	H	7	H	L	H	L
8	H	L	L	L	8	H	L	H	H
9	H	L	L	H	9	H	H	L	L

NOTES
b. Input applied to CP_0; Q_0 connected to CP_1.
c. Input applied to CP_1; Q_3 connected to CP_0.

74197 PRESETTABLE 4-BIT BINARY RIPPLE COUNTER

The "197" is an asynchronously presettable binary ripple counter that is partitioned into divide-by-two and divide-by-eight sections, with each section having a separate clock input. State changes are initiated in the counting modes by the HIGH-to-LOW transition of the clock inputs; however, stage changes of the Q outputs do not occur simultaneously because of the internal ripple delays. Designers should keep in mind when using external logic to decode the Q outputs that the unequal delays can lead to decoding spikes, and thus a decoded signal should not be used as a strobe or clock. The Q_0 output is designed and specified to drive the rated fanout plus the CP_1 input.

The device has an asynchronous active LOW master reset input ($\overline{MR}$) that overrides all other inputs and forces all outputs LOW. The counter is also asynchronously presettable. A LOW on the parallel load input ($\overline{PL}$) overrides the clock inputs and loads the data from parallel data ($D_0 - D_3$) inputs into the flip-flops. The counter acts as a transparent latch while the $\overline{PL}$ is LOW, and any change in the D_n inputs will be reflected in the outputs.

	74	74LS
Count Frequency (MHz)	50	30
Parallel Load	Yes	Yes
Clear	Low	Low
Typ. Total Power (mW)	240	60

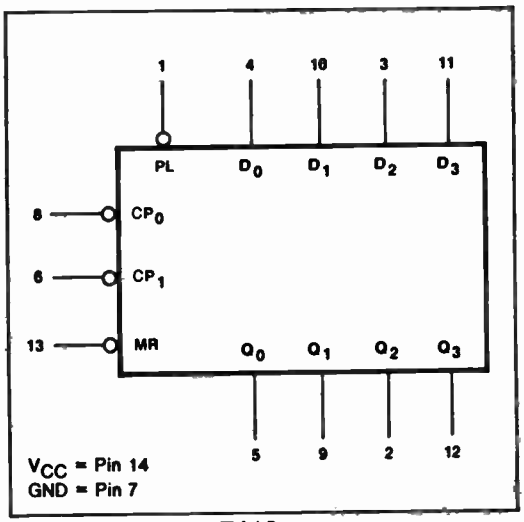
MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS
	$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	D_n	Q_n
Reset (Clear)	L	X	X	X	L
Parallel Load	H	L	X	L	L
	H	L	X	H	H
Count	H	H	↓	X	count

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↓ = HIGH-to-LOW Clock Transition

74197

LOGIC SYMBOL



74197

COUNT SEQUENCE

COUNT	4-BIT BINARY(b)			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

74197

NOTE

b. Q_0 connected to $\overline{CP}_1$; input applied to $\overline{CP}_0$

74198 8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

The functional characteristics of the "198" 9-bit bidirectional shift register are indicated in the logic diagram and truth table. The register is fully synchronous with all operations taking place in less than 20 nanoseconds (typical) making the device especially useful for implementing very high-speed CPUs, or for memory buffer registers.

The "198" design has special logic features that increase the application range. The synchronous operation of the device is determined by two mode select inputs. S_0 and S_1. As shown in the mode select table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.) or right to left (shift left, $Q_7 \rightarrow Q_6$, etc.) or parallel data can be entered, loading all eight bits of the register siumltaneously. When both S_0 and S_1 are LOW, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type serial data inputs (D_{SR} and D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

The mode select inputs of the 74198 are gated with the clock and should be changed from HIGH-to-LOW only while the clock input is HIGH for predictable operation. The eight parallel data inputs ($D_0 - D_7$) are D-type inputs. Data appearing on $D_0 - D_7$ inputs when S_0 and S_1 are HIGH are transferred to the $Q_0 - Q_7$ outputs, respectively, following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous master reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs LOW.

	74
Shift Frequency (MHz)	**25**
Serial Data Input	**D**
Asynchronous Clear	**Low**
Shift-Right Mode	**Yes**
Shift-Left Mode	**Yes**
Load	**Yes**
Hold	**Yes**
Typ. Total Power (mW)	**360**

MODE SELECT—FUNCTION TABLE

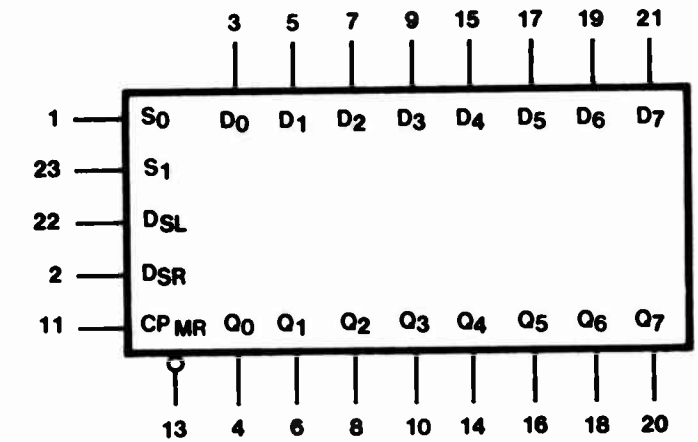
OPERATING MODE	INPUTS							OUTPUTS			
	CP	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	$Q_1 \ldots Q_6$	Q_7
Reset (clear)	X	L	X	X	X	X	X	L	L ... L	L
Hold (do nothing)	↑	H	l(b)	l(b)	X	X	X	q_0	$q_1 \ldots q_6$	q_7
Shift Left	↑ ↑	H H	h h	l(b) l(b)	X X	l h	X X	q_1 q_1	$q_2 \ldots q_7$ $q_2 \ldots q_7$	L H
Shift Right	↑ ↑	H H	l(b) l(b)	h h	l h	X X	X X	L H	$q_0 \ldots q_5$ $q_0 \ldots q_5$	q_6 q_6
Parallel Load	↑	H	h	h	h	X	d_n	d_0	$d_1 \ldots d_6$	d_7

74198

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
d_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition
X = Don't care
↑ = LOW-to-HIGH clock transition

NOTE

b The HIGH-to-LOW transition of the S_0 and S_1 inputs on the 54/74198 should only take place while CP is HIGH for conventional operation.



V_{CC} = Pin 24
GND = Pin 12

74198

74199 8-BIT PARALLEL ACCESS SHIFT REGISTER

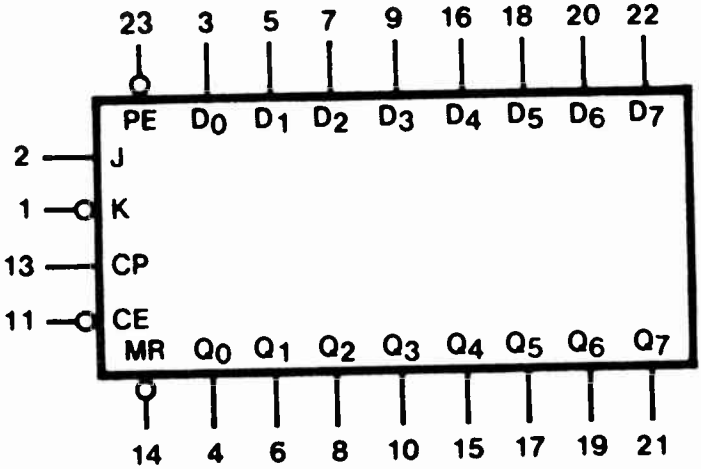
The functional characteristics of the "199" 8-bit parallel-access shift register are indicated in the logic diagram and function table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The "199" operates in two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the parallel enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and K inputs when the $\overline{PE}$ input is HIGH, and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$, following each LOW-to-HIGH clock transition. The J and K inputs provide the flexibility of the JK-type input for special applications and, by tying the two pins together, the simple D-type input for general applications. The device appears as eight common clocked D flip-flops when the $\overline{PE}$ input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs (D_0—D_7)is transferred to the respective (Q_0—Q_7)outputs.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. The 74199 utilizes edge-triggering; therefore, there is no restriction on the activity of the J, $\overline{K}$, D_n and $\overline{PE}$ inputs for logic operation, other than the setup and release time requirements.

The clock input is a gated OR structure which allows one input to be used as an active LOW clock enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of $\overline{CE}$ input should only take place while the CP is HIGH for conventional operation. A LOW on the master reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

	74
Shift Frequency (MHz)	**25**
Serial Data Input	**J-$\overline{K}$**
Asynchronous Clear	**Low**
Shift-Right Mode	**Yes**
Shift-Left Mode	**No**
Load	**Yes**
Hold	**Yes**
Typ. Total Power (mW)	**360**



V_{CC} = Pin 24
GND = Pin 12

74199

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS							OUTPUTS			
	$\overline{MR}$	CP	$\overline{CE}$	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	$Q_1 \ldots Q_6$		Q_7
Reset (clear)	L	X	X	X	X	X	X	L	L . . . L		L
Shift, Set First Stage	H	↑	l	h	h	h	X	H	$q_0 \ldots q_5$		q_6
Shift, Reset First Stage	H	↑	l	h	l	l	X	L	$q_0 \ldots q_5$		q_6
Shift, Toggle First Stage	H	↑	l	h	h	l	X	$\overline{q}_0$	$q_0 \ldots q_5$		q_6
Shift, Retain First Stage	H	↑	l	h	l	h	X	q_0	$q_0 \ldots q_5$		q_6
Parallel Load	H	↑	l	l	X	X	d_n	d_0	$d_1 \ldots d_6$		d_7
Hold (do nothing)	H	↑	h[b]	X	X	X	X	q_0	$q_1 \ldots q_6$		q_7

H = HIGH voltage level steady state
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level steady state
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't Care
d_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition
↑ = LOW-to-HIGH clock transition

NOTE
b The LOW-to-HIGH transition of $\overline{CE}$ should only occur while CP is HIGH for conventional operation

74199

74221 DUAL MONOSTABLE MULTIVIBRATOR

The "221" is a dual monostable multivibrator with performance characteristics virtually identical to those of the "121." Each multivibrator features an active LOW-going edge input ($\overline{A}$) and an active HIGH-going edge input ($\overline{B}$), either of which can be used as an enable input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt trigger input circuitry (TTL hysteresis) for the B input allows jitter free triggering from inputs with transition rates as low as 1 volt per second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to V_{cc} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the $\overline{A}$ and B inputs and are a function of the timing components. The output pulses can be terminated by the overriding active LOW Reset ($\overline{R_D}$. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35 nanoseconds to the maximums shown here by choosing appropriate timing components. With R_{ext}=2k and C_{ext}=0, an output pulse of typically 30 nanoseconds is achieved which may be used as a DC-triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

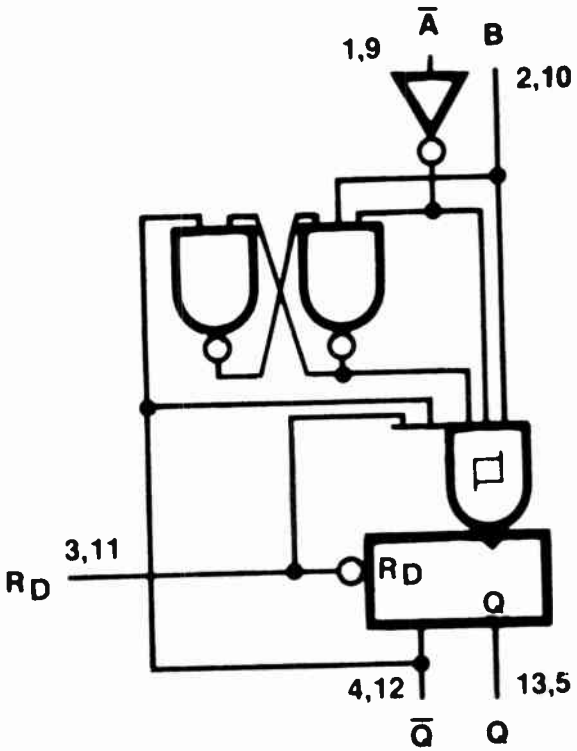
Pulse width stability is achieved through internal compensation and is virtually independent of V_{cc} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter free operation is maintained over the full temperature and V_{cc} ranges for more than six decades of timing capacitance (10pF to 10μF) and more than one decade of timing resistance (2K to 40K for the 74221 and 2K to 100K for the 74LS221). Throughout these ranges, pulse width is defined by the following relationship:

$$t_w \text{ (out)} = C_{ext}\ R_{ext}\ In2$$
$$t_w \text{ (out)} = 0.7 C_{ext}\ R_{ext}$$

In circuits where pulse cutoff is not critical, timing capacitance of up to 1000μF and timing resistance of as low as 1.4K may be used. Pin assignments for these devices are identical to those of the "123" so that the "221" can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext}.

	74LS
Positive Inputs	1
Negative Inputs	1
Output Pulse Range (ns to s)	20ns – 70s
Typ. Total Power (mW)	23



V_{CC} = Pin 16
GND = Pin 8

C_{ext} = Pins 14,6
C_{ext}/R_{ext} = Pins 15,7

74221

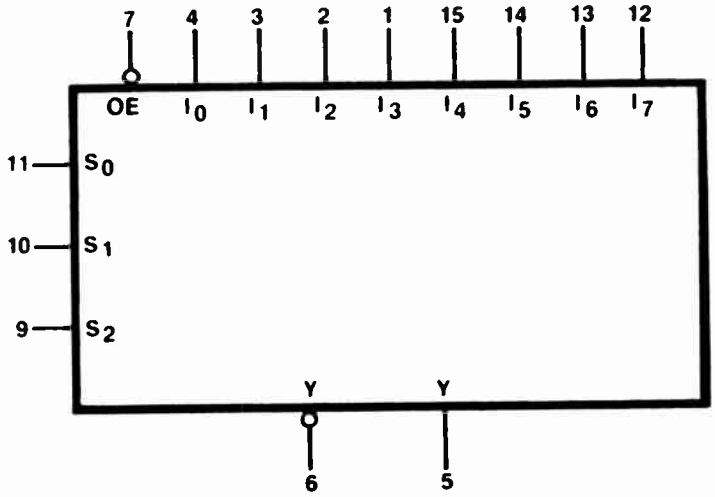
74251 8-INPUT MULTIPLEXER (3-STATE)

The "251" is a logical implementation of a single-pole, 8-position switch with the state of the three select inputs (S_0, S_1 and S_2) controlling the switch position. Assertion (Y) and negation ($\overline{Y}$) outputs are both provided. The output enable input ($\overline{OE}$) is active LOW. The logic function provided at the output, when activated is:

$$Y = \overline{OE}\,(I_0 \cdot \overline{S_0} \cdot \overline{S_2} + I_1 \cdot S_0 \cdot S_1 \cdot \overline{S_2} + I_2 \cdot \overline{S_0} \cdot S_1 \cdot \overline{S_2} + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S_2} + I_4 \cdot \overline{S_0} \cdot \overline{S_1} \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S_1} \cdot S_2 + I_6 \cdot \overline{S_0} \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

Both outputs are in the high-impedance (high-Z) state when the output enable is HIGH, allowing multiplexer expansion by tying the outputs of up to 128 devices together. All but one device must be in the high-impedance state to avoid high currents that would exceed the maximum ratings when the outputs of the 3-state devices are tied together. Design of the output enable signals must ensure there is no overlap in the active LOW portion of the enable voltages.

	74S	74	74LS
Type of Output	**3-State**	**3-State**	**3-State**
Typ. Delay, Data to Inverting Output (ns)	**4.5**	**11**	**17**
Typ. Delay, Data to Noninverting Output (ns)	**8**	**18**	**21**
Typ. Delay, From Enable (ns)	**14**	**17**	**21**
Typ. Total Power (mW)	**275**	**155**	**35**



V_{CC} = Pin 16
GND = Pin 8

74251

Truth Table

INPUTS												OUTPUTS	
$\overline{OE}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance (off)

74251

74253 DUAL 4-INPUT MULTIPLEXER (3-STATE)

The "253" has two identical 4-input multiplexers with 3-state outputs which select two bits from four sources selected by common select inputs (S_0 S_1). When the individual output enable ($\overline{E}_{0a}$, $\overline{E}_{0b}$) inputs of the 4-input multiplexers are HIGH, the outputs are forced to a high-impedance (high $-Z$) state.

The "253" is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two select inputs. Logic equations for the outputs are:

$$Y_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S_1} \cdot \overline{S_0} + I_{1a} \cdot \overline{S_1} \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S_0} + I_{3a} \cdot S_1 \cdot S_0)$$

$$Y_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S_1} \cdot \overline{S_0} + I_{1b} \cdot \overline{S_1} \cdot S_0 + I_{2b} \cdot S_1 \cdot S_0 + I_{3b} \cdot S_1 \cdot S_0)$$

All but one device must be in the high-impedance state to avoid high currents exceeding the maximum ratings, if the outputs of 3-state devices are tied together. Design of the output enable signals must ensure that there is no overlap.

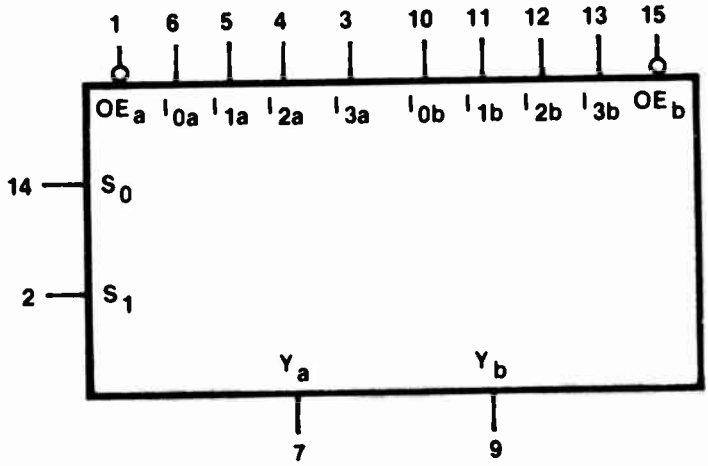
	74LS
Type of Output	**3-State**
Typ. Delay, Data to Noninverting Output (ns)	**12**
Typ. Delay, From Enable (ns)	**16**
Typ. Total Power (mW)	**35**

Truth Table

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Y
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = Don't Care
(Z) = High impedance (off) state

74253



V_{CC} = Pin 16
GND = Pin 8

74253

74256 DUAL 4-BIT ADDRESSABLE LATCH

The "256' dual addressable latch has four distinct modes of operation and are selectable by controlling the clear and enable inputs. In the addressable latch mode, data at the data (D) inputs are written into the addressed latches. The addressed latches will follow the data input will all unaddressed latches remaining in their previous states.

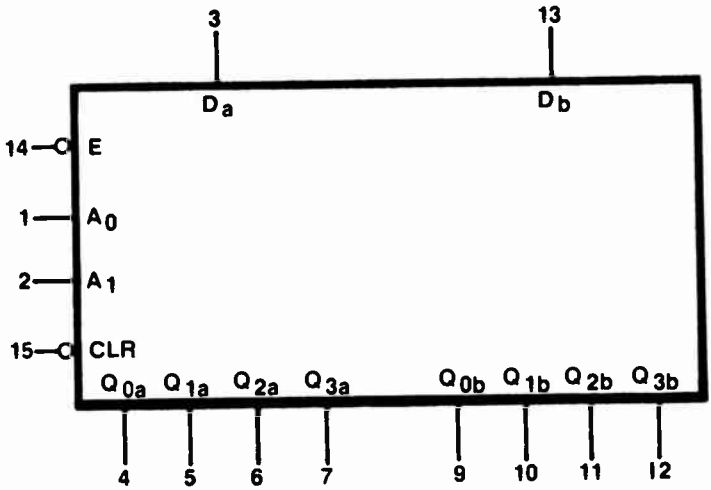
In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches enable should be held HIGH (inactive) while the address lines are changing. In the dual of 1-of-4 decoding or demultiplexing mode ($\overline{CLR} = \overline{E} =$ LOW), addressed outputs will follow the level of the D inputs will all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the address and data inputs.

MODE SELECT – FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	$\overline{CLR}$	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3
Clear	L	H	X	X	X	L	L	L	L
Demultiplex (active HIGH decoder when D=H)	L	L	d	L	L	Q=d	L	L	L
	L	L	d	H	L	L	Q=d	L	L
	L	L	d	L	H	L	L	Q=d	L
	L	L	d	H	H	L	L	L	Q=d
Store (do nothing)	H	H	X	X	X	q_0	q_1	q_2	q_3
Addressable latch	H	L	d	L	L	Q=d	q_1	q_2	q_3
	H	L	d	H	L	q_0	Q=d	q_2	q_3
	H	L	d	L	H	q_0	q_1	Q=d	q_3
	H	L	d	H	H	q_0	q_1	q_2	Q=d

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
X = Don't care.
d = HIGH or LOW data one setup time prior to LOW-to-HIGH Enable transition.
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

74256



V_{CC} = Pin 16
GND = Pin 8

74256

74257 QUAD 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER (3-STATE)

The "257" has four identical 2-input Multiplexers with 3-state outputs that select four bits of data from two sources under control of a common data select input (S). The I_0 inputs are selected when the select input is LOW, and the I_1 inputs are selected when the select input is HIGH. Data appears at the outputs in true (non-inverted) form from the selected inputs.

The "257" is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. Outputs are forced to a high-impedance off state when the output enable input ($\overline{OE}$) is HIGH. All but one device must be in the high-impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

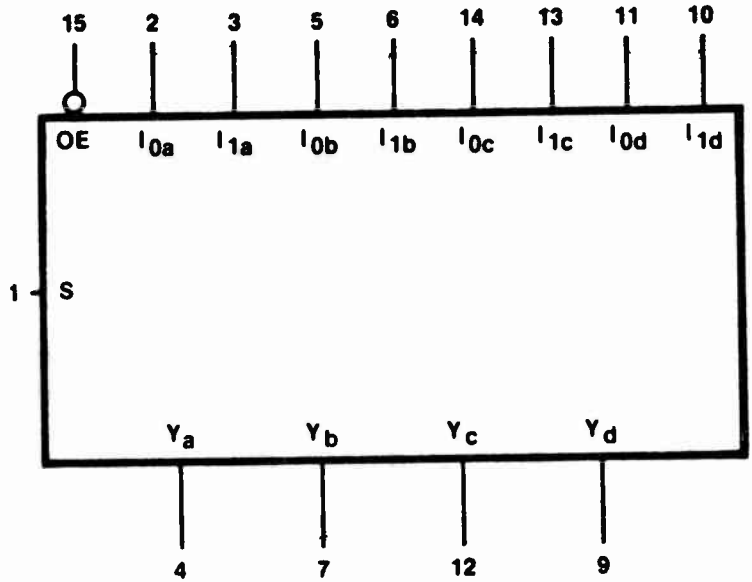
	74S	74LS
Type of Output	**3-State**	**3-State**
Typ. Delay, Data to Inverting Output (ns)	-	-
Typ. Delay, Data to Nonverting Output (ns)	5	12
Typ. Delay, From Enable (ns)	14	20
Typ. Total Power (mW)	320	50

Truth Table

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{OE}$	S	I_0	I_1	Y
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance (off) state

74257



V_{CC} = Pin 16
GND = Pin 8

74257

74258 QUAD 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER (3-STATE)

The "258" has four identical 2-input multiplexers with 3-state outputs that select four bits of data from two sources under control of a common data select input (S). The I_0 inputs are selected when the select input is LOW, and the I_1 inputs are selected when the select input is HIGH. Data appear at the outputs in inverted (complementary) form.

The "258" is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the select input. Outputs are forced to a high-impedance off state when the output enable input ($\overline{OE}$) is HIGH. All but one device must be in the high-impedance state to avoid currents exceeding the maximum ratings if outputs of the 3-state devices are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

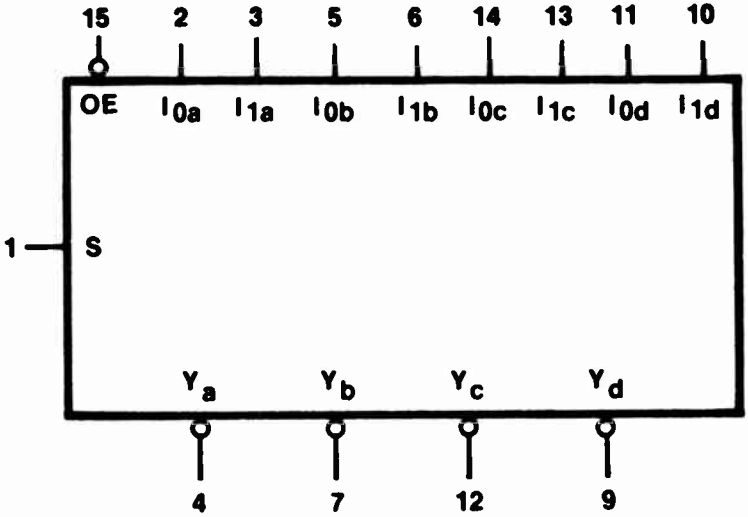
Type of Output	74S	74LS
Typ. Delay, Data to Inverting Output (ns)	3-State 4	3-State 12
Typ. Delay, Data to Noninverting Output (ns)	-	-
Typ. Delay, From Enable (ns)	4	20
Typ. Total Power (mW)	280	35

Truth Table

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	(Z)
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance (off) state

74258



V_{CC} = Pin 16
GND = Pin 8

74258

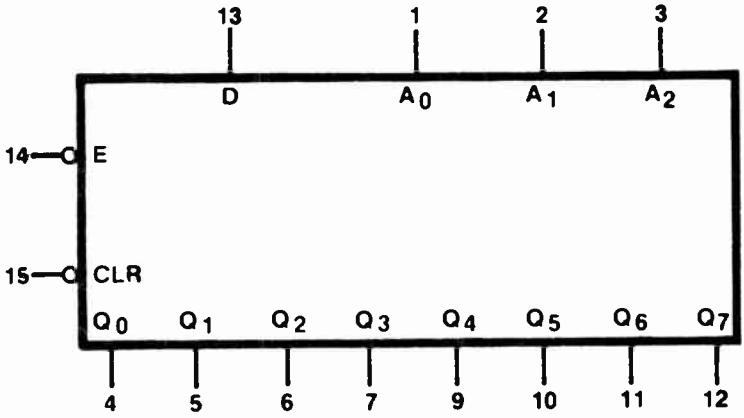
The "259" addressable latch has four distinct modes of operation and are selectable by controlling the clear and enable inputs. In the addressable latch mode, data at the data (D) inputs are written into the addressed latches. The addressed latches will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the one-of-eight decoding or demultiplexing mode, ($\overline{CLR} = \overline{E}$ = LOW) addressed outputs will follow the level of the D inputs with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the address and data inputs.

MODE SELECT—FUNCTION TABLE

OPERATING	INPUTS						OUTPUTS							
MODE	$\overline{CLR}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
Clear	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (active HIGH decoder when D=H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d
Store (do nothing)	H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7
Addressable latch	H	L	d	L	L	L	Q=d	q_1	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	L	L	q_0	Q=d	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	L	H	L	q_0	q_1	Q=d	q_3	q_4	q_5	q_6	q_7
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q=d

H = HIGH voltage level steady state
L = LOW voltage level steady state
X = Don't care
d = HIGH or LOW data one setup time prior to LOW-to-HIGH Enable transition
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

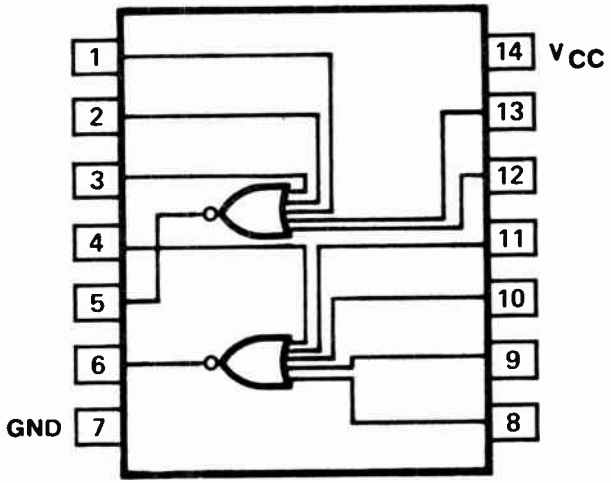
74259



V_{CC} = Pin 16
GND = Pin 8

74259

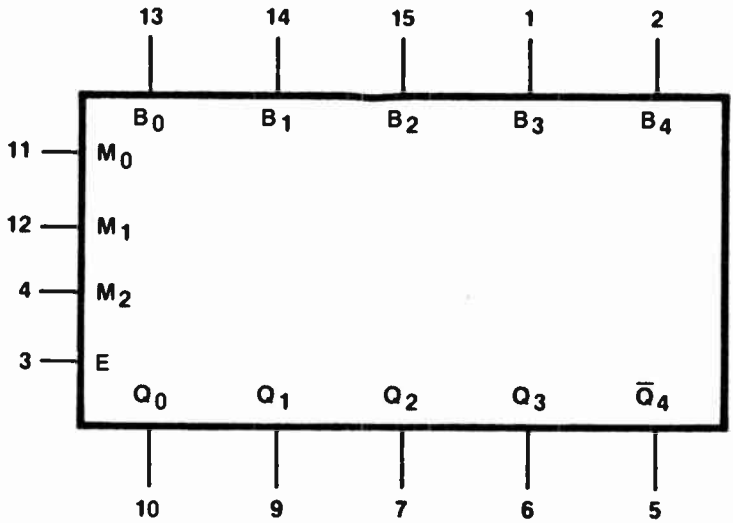
74260 DUAL 5-INPUT POSITIVE NOR GATE



74260

The M inputs are for the multiplier bits, and the B inputs are for the multiplicand. The Q outputs represent the partial product as a recoded base 4 number. This recoding effectively reduces the Wallace-Tree (summing) hardware requirements by a factor of two.

The outputs represent partial products in ones-complement notation generated as a result of multiplication. A simple rounding scheme using two additional gates is needed for each partial product to generate twos complement. The leading (most significant) bit of the product is inverted for ease in extending the sign to left justify the partial product bits.



V_{CC} = Pin 16
GND = Pin 8

74261

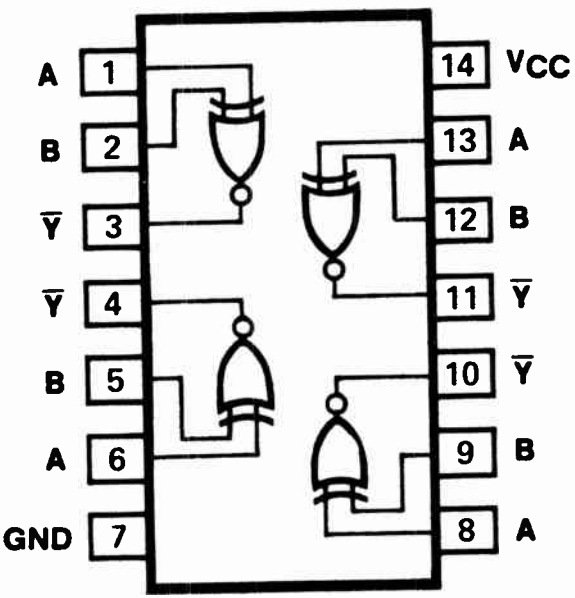
FUNCTION TABLE

INPUTS				OUTPUTS				
E	M_2	M_1	M_0	$\overline{Q}_4$	Q_3	Q_2	Q_1	Q_0
L	X	X	X	$\overline{q}_4$	q_3	q_2	q_1	q_0
H	L	L	L	H	L	L	L	L
H	L	L	H	$\overline{B}_4$	B_4	B_3	B_2	B_1
H	L	H	L	$\overline{B}_4$	B_4	B_3	B_2	B_1
H	L	H	H	$\overline{B}_4$	B_3	B_2	B_1	B_0
H	H	L	L	B_4	$\overline{B}_3$	$\overline{B}_2$	$\overline{B}_1$	$\overline{B}_0$
H	H	L	H	B_4	$\overline{B}_4$	$\overline{B}_3$	$\overline{B}_2$	$\overline{B}_1$
H	H	H	L	B_4	$\overline{B}_4$	$\overline{B}_3$	$\overline{B}_2$	$\overline{B}_1$
H	H	H	H	H	L	L	L	L

H = HIGH voltage level
L = LOW voltage level
q = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW Enable transition.
B_n = The logic level on the referenced multiplicand input.

74261

74266 QUAD 2-INPUT EXCLUSIVE-NOR GATE WITH OPEN-COLLECTOR OUTPUTS



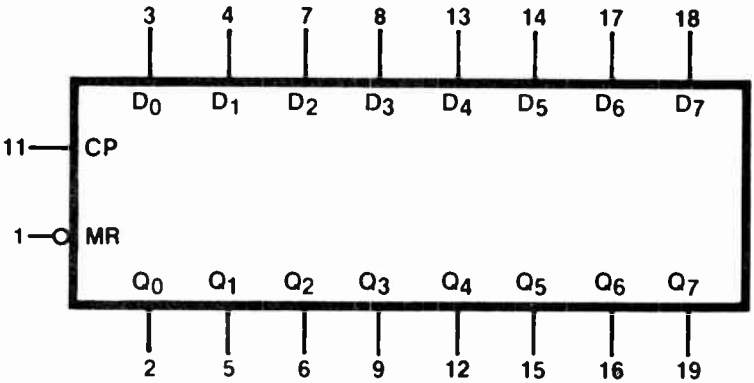
74266

74273 OCTAL D FLIP-FLOP

The "273" has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop Q output.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.



V_{CC} = Pin 20
GND = Pin 10

74273

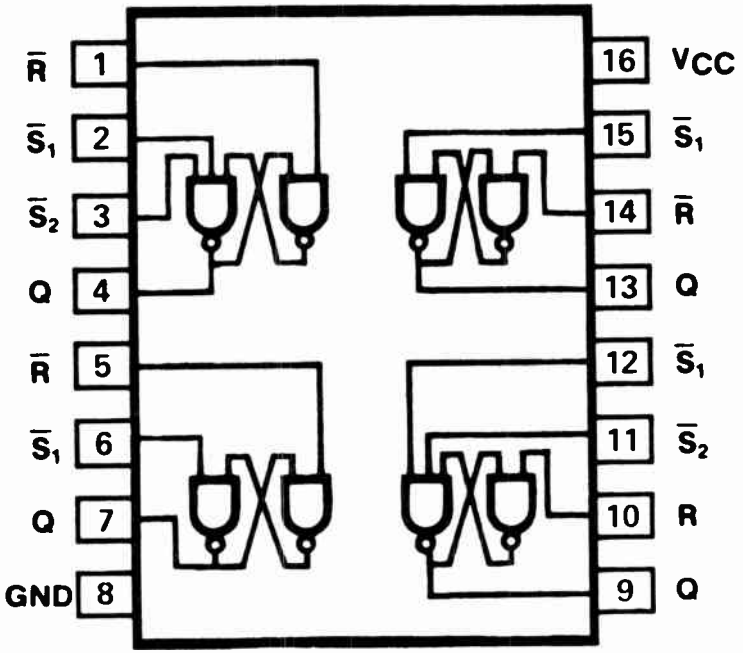
MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

74273

74279 A QUAD $\overline{S}$-$\overline{R}$ LATCH



74279

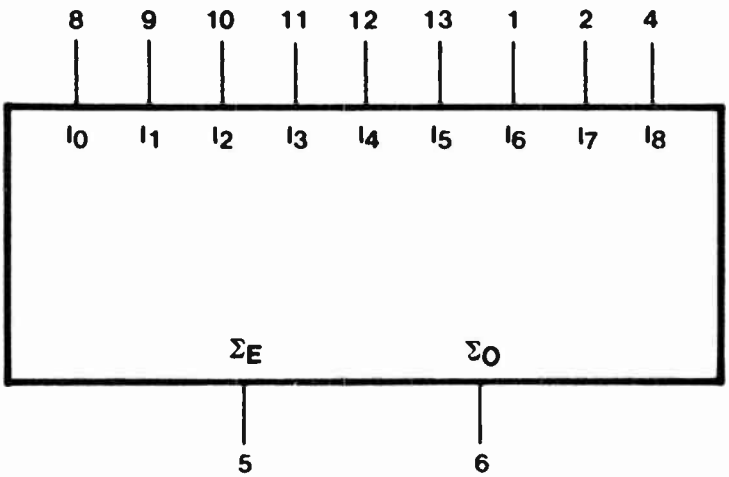
74280 9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

The "280" is a 9-bit parity generator or checker commonly used to detect errors in high-speed data transmission or data retrieval systems. Both even and odd parity outputs are available for generating or checking even or odd parity on up to nine bits.

The Even parity output (Σ E) is HIGH when an even number of data inputs (I_0-I_8) is HIGH. The odd parity output (Σ_O) is HIGH when an odd number of data inputs is HIGH.

Expansion to larger word sizes is accomplished by tying the Even outputs (Σ E) of up to nine parallel devices to the data inputs of the final stage.

	74S
Typ. Delay Time (ns)	13
Typ. Total Power (mW)	335



V_{CC} = Pin 14
GND = Pin 7

74280

Truth Table

INPUTS	OUTPUTS	
Number of HIGH data inputs (I_0-I_8)	Σ_E	Σ_O
Even	H	L
Odd	L	H

74280

74283 4-BIT FULL ADDER WITH FAST CARRY

The "283" adds two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the sum outputs (Σ_1-Σ_4 and the outgoing carry (C_{out}) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT},$$

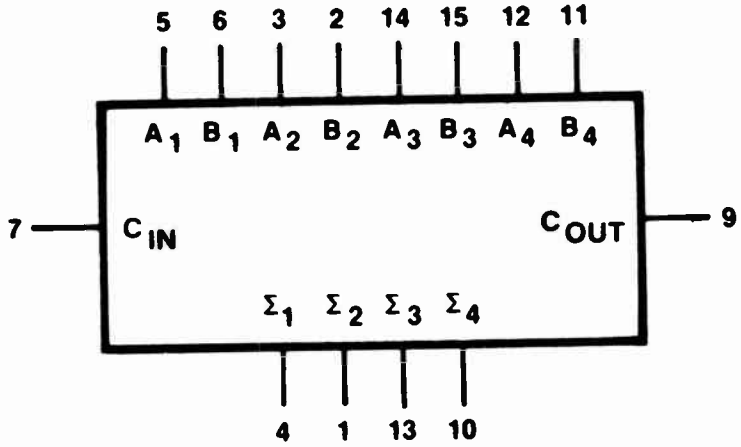
Where (+) = plus.

Due in the symmetry of the binary add function, the "283" can be used with either all active HIGH operands (positive logic) or with all active LOW operands (negative logic). With active HIGH inputs, C_{IN} cannot be left open; it must be held LOW when no carry in is intended. Interchanging inputs of equal weight does not affect the operation; thus, C_{IN}, A_1 and B_1 can arbitrarily be assigned to pins 5, 6, 7, etc.

	74LS
Typ. Carry Time (ns)	10
Typ. Add Time (ns)	15
Typ. Power Per Bit (mW)	24

PINS	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

74283

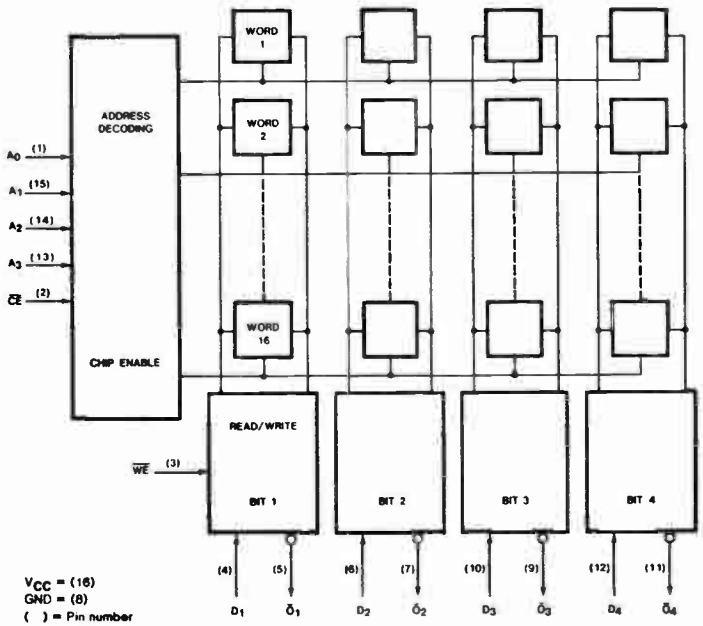


V_{CC} = Pin 16
GND = Pin 8

74283

The "289" is a high-speed array of 64 memory cells organized as 16 words of four bits each. A one-of-sixteen address decoder selects a single word which is specified by the four address inputs (A_0-A_3). A READ operation is initiated after the address lines are stable when the write enable ($\overline{WE}$) input is HIGH and the chip select-memory enable ($\overline{CS}$) input is LOW. Data is read at the outputs inverted from the data, which was written into the memory.

A WRITE operation requires that the $\overline{WE}$ and $\overline{CS}$ inputs be LOW. The address inputs must be stable during the WRITE mode for predictable operation. When the write mode is selected, the outputs are HIGH. The selected memory cells are transparent to changes in the data during the WRITE mode; therefore, data must be stable one setup time before the LOW-to-HIGH transition of $\overline{CE}$ or $\overline{WE}$.



74289

MODE SELECT – FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{CS}$	$\overline{WE}$	D_n	$\overline{O}_n$
Write—Disable Outputs	L L	L L	L H	H H
Read	L	H	X	$\overline{Data}$
Store-Disable Outputs	H	X	X	H

H = HIGH voltage level

L = LOW voltage level

X = Don't care

$\overline{Data}$ = Read complement of data from addressed word location

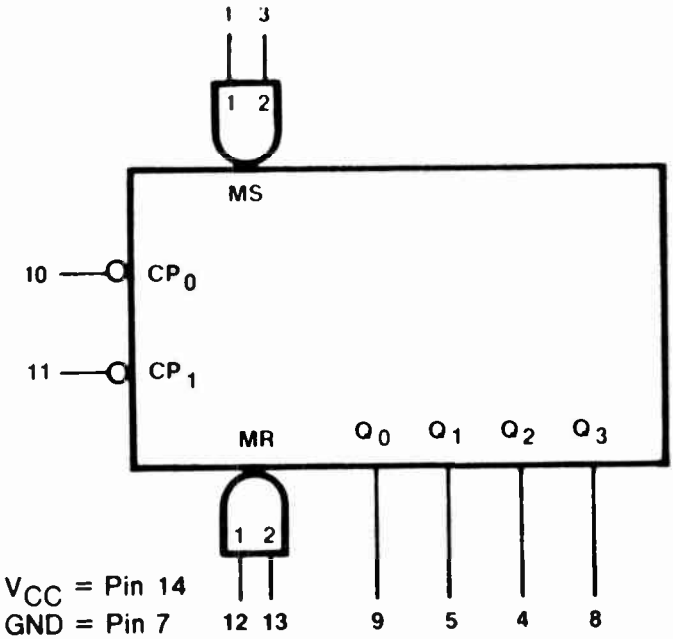
74289

74290 DECADE COUNTER

The "290" is a 4-bit ripple type decade counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output is designed and specified to drive the rate fanout plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous master reset ($MR_1 \cdot MR_2$) is provided, which overrides both clocks and resets (clears) all the flip-flops. Also provided is a gated AND asynchronous master set ($MS_1 \cdot MS_2$), which overrides the clocks and the MR inputs, setting the outputs to nine (HLLH).

Because the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a BCD (8421) counter, the $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count, producing a BCD count sequence. In a symmetrical biquinary divide-by-10 counter, the Q_3 output must be connected externally to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input, and a divide-by-10 square wave is obtained at output Q_0. To operate as a divide-by-two and a divide-by-five counter, no external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain divide-by-five operation at the Q_3 output.



BCD COUNT SEQUENCE—TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE Output Q_0 connected to input $\overline{CP}_1$

MODE SELECTION—TRUTH TABLE

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

H HIGH voltage level
L LOW voltage level
X Don't care

74290

74293 4-BIT BINARY RIPPLE COUNTER

The "293" is a 4-bit ripple type binary counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output is designed and specified to drive the rated fanout plus the $\overline{CP}_1$ input of the device. A gate AND asynchronous master reset ($MR_1 \cdot MR_2$) is provided, which overrides both clocks and resets (clears) all the flip-flops.

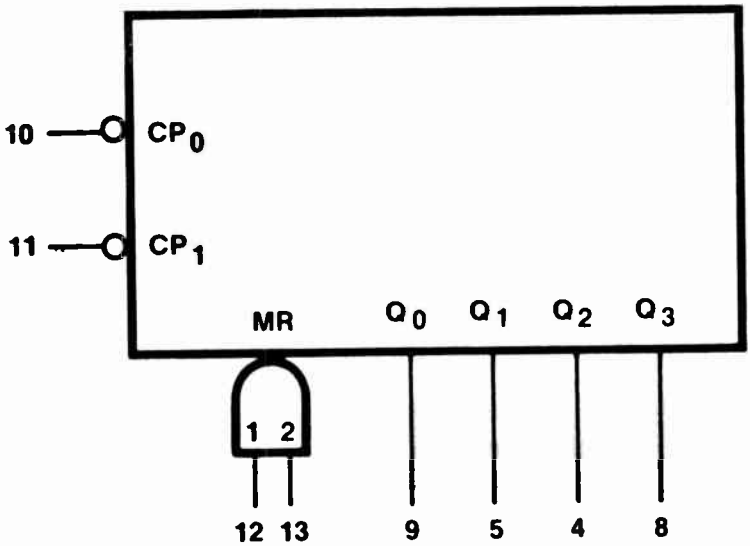
Because the output form the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a 4-bit ripple counter, the output Q_0 must be connected externally to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8 and 16 are performed at the Q_0, Q_1, Q_2 and Q_3 outputs, as shown in the truth table. As a 3-bit ripple counter, the input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_1, Q_2 and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH voltage level
L = LOW voltage level
X = Don't care

74293



V_{CC} = Pin 14
GND = Pin 7

74293

Truth Table

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

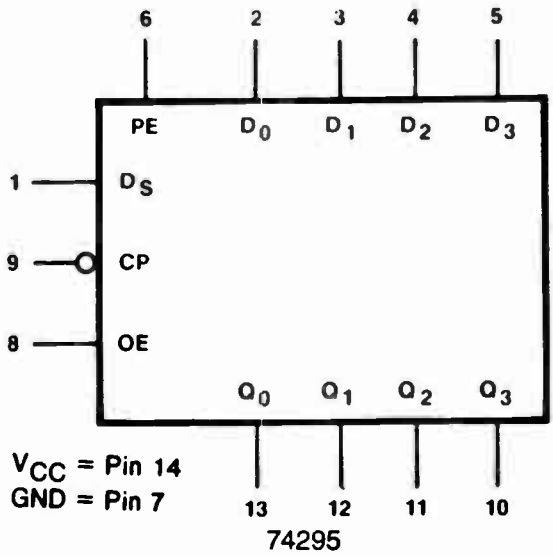
NOTE: Output Q_0 connected to Input $\overline{CP}_1$.

74293

74295 4-BIT SHIFT REGISTER WITH 3-STATE OUTPUTS

The "295" is a 4-bit shift register with serial and parallel synchronous operating modes and four 3-state buffer outputs. The shifting and loading operations are controlled by the state of the parallel enable (PE) input. When PE is HIGH, data is loaded from the parallel data inputs (D_0-D_3) into the register synchronous with the HIGH-to-LOW transition of the clock input ($\overline{CP}$). When PE is LOW, the data at the serial data input (D_S) is loaded into the Q_0 flip-flop, and data in the register are shifted on bit to the right in the direction ($Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$) synchronous with the negative transition of the clock. The PE and data inputs are fully edge-triggered and must be stable only one setup time prior to the HIGH-to-LOW transition of the clock.

The 3-state output buffers are designed to drive heavily loaded 3-state buses or large capacitive loads. The active HIGH output enable (OE) controls all four 3-state buffers independent of the register operation. When OE is HIGH, data in the register appear at the outputs. When OE is LOW, the outputs are in the high-impedance off state, which means they will neither drive not load the bus.



MODE SELECT—FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS				REGISTER OUTPUTS			
	$\overline{CP}$	PE	D_S	D_n	Q_0	Q_1	Q_2	Q_3
Parallel Load	↓	l	l	X	L	q_0	q_1	q_2
	↓	l	h	X	H	q_0	q_1	q_2
Shift right	↓	h	X	l	L	L	L	L
	↓	h	X	h	H	H	H	H

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS
	OE	Q_n (Register)	Q_0, Q_1, Q_2, Q_3
Read	H	L	L
	H	H	H
Disabled	L	X	(Z)

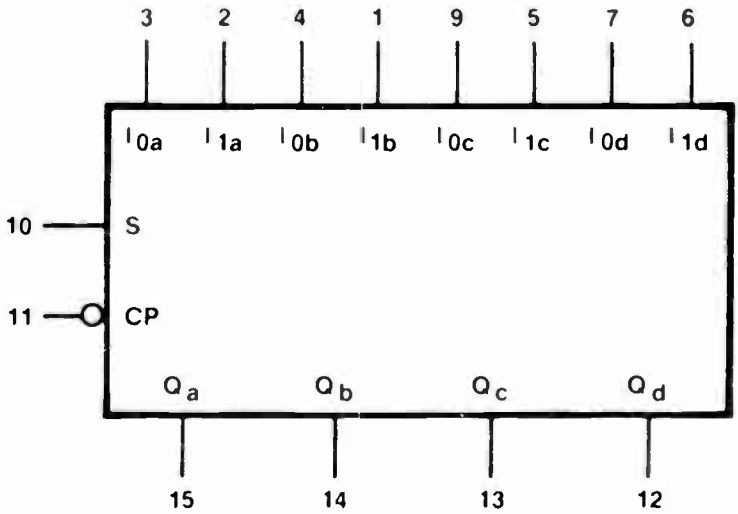
H = HIGH voltage level
h = HIGH voltage level one setup time prior to the HIGH-to-LOW clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW clock transition
q_n = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW clock transition
X = Don't care
(Z) = High impedance "off" state
↓ = HIGH-to-LOW clock transition

74295

74298 QUAD 2-PORT REGISTER

This device is a high-speed quad 2-port register. It selects four bits of data from two sources (ports) under the control of a common select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the clock input ($\overline{CP}$). The 4-bit output register is fully edge-triggered. The data inputs (I_0 and I_1) and select input (S) must be stable only one setup time prior to the HIGH-to-LOW transition of the clock for predictable operation.

	74LS
Frequency (MHz)	25
Delay time, To Noninverting Output (ns)	20
Asynchronous Clear	None
Typ. Total Power (mW)	65



V_{CC} = Pin 16
GND = Pin 8

74298

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS
	$\overline{CP}$	S	I_0	I_1	Q_n
Load Source "0"	↓	l	l	X	L
	↓	l	h	X	H
Load Source "1"	↓	h	X	l	L
	↓	h	X	h	H

H = HIGH voltage level

h = HIGH voltage level one setup time prior to the HIGH-to-LOW clock transition

L = LOW voltage level

l = LOW voltage level one setup time prior to the HIGH-to-LOW clock transition

X = Don't care

↓ = HIGH-to-LOW clock transition

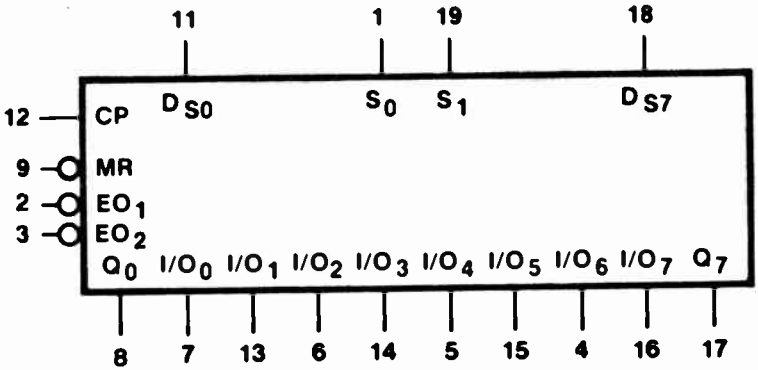
74298

74299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTER

The "229" is an 8-bit general purpose shift-storage register useful in a wide variety of shifting and 3-state bus interface applications. The register has four synchronous operating modes controlled by the two select inputs as shown in the mode select function table. The mode select (S_0 and S_1) inputs, the serial data (D_{S0} and D_{S7}) inputs and the parallel data I/O_0–I/O_7 inputs are edge-triggered, responding only to the LOW-to-HIGH transition of the clock ($\overline{CP}$) input. Therefore, the only timing restriction is that the S_0, S_1 and selected data inputs must be stable one setup time prior to the positive transition of the clock pulse. The master reset ($\overline{MR}$) is an asynchronous active LOW input. When LOW, the $\overline{MR}$ overrides the clock and all other inputs and clears the register.

Serial mode expansion of the register is accomplished by tying the Q_0 serial output to the D_{S7} input of the preceding register, and tying the Q_7 serial output to the D_{S0} input of the following register. Recirculating the (n × 8) bit words is accomplished by tying the Q_7 output of the last stage to the D_{S0} input of the first stage.

The 3-state bidirectional input output port has three modes of operation. When the two output enable ($\overline{OE}_1$ and $\overline{OE}_2$) inputs are LOW, and one or both of the select inputs are LOW, data in the register are presented at the eight outputs. When both select inputs are HIGH, the 3-state outputs are forced to the high-impedance off state and the register is prepared to load data from the 3-state bus coincident with the next LOW-to-HIGH clock transition. In this parallel load mode, the select inputs disable the outputs even if $\overline{OE}_1$ and $\overline{OE}_2$ are both LOW. A HIGH level on one of the output enable inputs will force the outputs to the high-impedance off state. When disabled, the 3-state I/O ports present one unit load to the bus, because an input is tied to the I/O node. The enabled 3-state output is designed to drive heavy capacitive loads or heavily loaded 3-state buses.



V_{CC} = Pin 20
GND = Pin 10

74299

MODE SELECT—FUNCTION TABLES

REGISTER OPERATING MODES	INPUTS							REGISTER OUTPUTS
	$\overline{MR}$	CP	S_0	S_1	D_{S0}	D_{S7}	I/O_n	Q_0 Q_1 - - - Q_6 Q_7
Reset (clear)	L	X	X	X	X	X	X	L L - - - L L
Shift right	H	↑	h	l	l	X	X	L q_0 - - - q_5 q_6
	H	↑	h	l	h	X	X	H q_0 - - - q_5 Q_6
Shift left	H	↑	l	h	X	l	X	q_1 q_2 - - - q_7 L
	H	↑	l	h	X	h	X	q_1 q_2 - - - q_7 H
Hold (do nothing)	H	↑	l	l	X	X	X	q_0 q_1 - - - q_6 q_7
Parallel load	H	↑	h	h	X	X	l	L L - - - L L
	H	↑	h	h	X	X	h	H H - - - H H

3-STATE I/O PORT OPERATING MODE	INPUTS					INPUTS/OUTPUTS
	$\overline{OE}_1$	$\overline{OE}_2$	S_0	S_1	Q_n (Register)	I/O_0 - - - - I/O_7
Read register	L	L	L	X	L	L
	L	L	L	X	H	H
	L	L	X	L	L	L
	L	L	X	L	H	H
Load register	X	X	H	H	$Q_n = I/O_n$	I/O_n = inputs
Disable I/O	H	X	X	X	X	(Z)
	X	H	X	X	X	(Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
q_n = Lower case letters indicate the state of the referenced output one setup prior to the LOW-to-HIGH clock transition
X = Don't care
(Z) = High impedance "off" state
↑ = LOW-to-HIGH clock transition

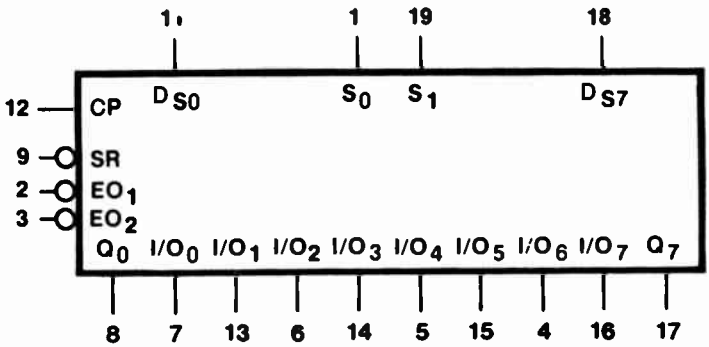
74299

74323 8-BIT UINVERSAL SHIFT/STORAGE REGISTER

The "323" is an 8-bit general purpose shift-storage register useful in a wide variety of shifting and 3-state bus interface applications. The register has five synchronous operating modes controlled by the two select inputs and the synchronous reset as shown in the mode select function table. The mode select (S_0 and S_1) inputs, the synchronous reset ($\overline{SR}$) input, the serial data (D_{S0} and D_{S7}) inputs and the parallel data I/O_0 -- I/O_1 inputs are edge-triggered, responding only to the LOW-to-HIGH transition of the clock (CP) input. Therefore, the only timing restriction is that the $\overline{SR}$, S_0, S_1 and selected data inputs must be stable one setup time prior to the positive transition of the clock pulse. The $\overline{SR}$ input overrides the select and data inputs when LOW and clears the register coincident with the next positive clock transition.

Serial mode expansion of the register is accomplished by tying the Q_0 serial output to the D_{S7} input of the preceding register, and tying the Q_7 serial output to the D_{S0} input of the following register. Recirculating the ($n \times 8$) bit words is accomplished by tying the Q_7 output of the last stage too the D_{S0} input of the first stage.

The 3-state bidirectional Input/Output port has three modes of operation. When the two output enable ($\overline{OE_1}$ and $\overline{OE_2}$) inputs are LOW, and one or both of the selected inputs are LOW, the data in the register is presented at the eight outputs. When both select inputs are HIGH, the 3-state outputs are forced to the high-impedance off state, and the register is prepared to load data from the 3-state bus coincident with the next LOW-to-HIGH clock transition. In this parallel load mode, the select inputs disable the outputs even if $\overline{OE_1}$ and $\overline{OE_2}$ are both LOW. A HIGH level on one of the output enable inputs will force the outputs to the high-impedance of state. When disabled, the 3-state I/O ports present one unit load to the bus, because an input is tied to the I/O mode. The enabled 3-state output is designed to drive heavy capacitive loads or heavily loaded 3-state buses.



V_{CC} = Pin 20
GND = Pin 10

74323

MODE SELECT—FUNCTION TABLES

REGISTER OPERATING MODES	INPUTS							REGISTER OUTPUTS
	$\overline{SR}$	CP	S_0	S_1	D_{S0}	D_{S7}	I/O_n	Q_0 Q_1 - - - Q_6 Q_7
Reset (clear)	l	↑	X	X	X	X	X	L L - - - L L
Shift right	h	↑	h	l	l	X	X	L q_0 - - - q_5 q_6
	h	↑	h	l	h	X	X	H q_0 - - - q_5 Q_6
Shift left	h	↑	l	h	X	l	X	q_1 q_2 - - - q_7 L
	h	↑	l	h	X	h	X	q_1 q_2 - - - q_7 H
Hold (do nothing)	h	↑	l	↑	X	X	X	q_0 q_1 - - - q_6 q_7
Parallel load	h	↑	h	h	X	X	l	L L - - - L L
	h	↑	h	h	X	X	h	H H - - - H H

3-STATE I/O PORT OPERATING MODE	INPUTS					INPUTS/OUTPUTS
	$\overline{OE}_1$	$\overline{OE}_2$	S_0	S_1	Q_n (REGISTER)	I/O_0 - - - - I/O_7
Read register	L	L	L	X	L	L
	L	L	L	X	H	H
	L	L	X	L	L	L
	L	L	X	L	H	H
Load register	X	X	H	H	$Q_n = I/O_n$	I/O_n = inputs
Disable I/O	H	X	X	X	X	(Z)
	X	H	X	X	X	(Z)

74323

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
q_n = Lower case letters indicate the state of the referenced output one setup prior to the LOW-to-HIGH clock transition.
X = Don't care.
(Z) = High impedance "off" state.
↑ = LOW-to-HIGH clock transition.

74323

74350 4-BIT SHIFTER WITH 3-STATE OUTPUTS

The "350" is a combination logic circuit that shifts a 4-bit word from one to three places. No clocking is required as with shift registers.

The "350" can be used to shift any number of bits any number of places up or down by suitable interconnection. Shifting can be:

- Logical with logic zeros filled in at either end of the shifting field.
- Arithmetic where the sign bit is extended during a shift down.
- End around where the data word forms a continuous loop.

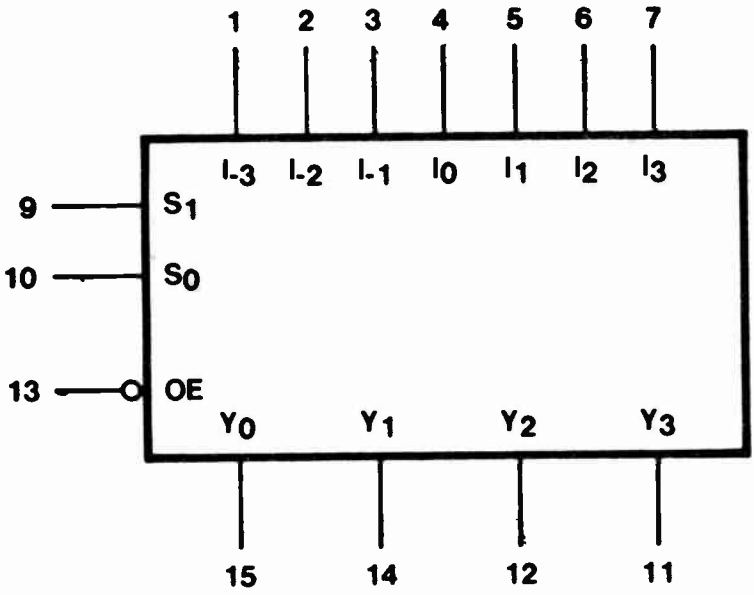
The 3-state outputs are useful for bus interface applications or expansion to a large number of shift positions in end-around shifting. The active LOW output enable ($\overline{OE}$) input controls the state of the outputs. The outputs are in the high-impedance off state when $\overline{OE}$ is HIGH, and they are active when $\overline{OE}$ is LOW.

Truth Table

$\overline{OE}$	S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D_3	D_2	D_1	D_0	X	X	X	D_3	D_2	D_1	D_0
L	L	H	X	D_2	D_1	D_0	D_{-1}	X	X	D_2	D_1	D_0	D_{-1}
L	H	L	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_1	D_0	D_{-1}	D_{-2}
L	H	H	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_0	D_{-1}	D_{-2}	D_{-3}

H = HIGH voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance (off) state
D_n = HIGH or LOW state of the referenced I_n input

74350



74350

V_{CC} = Pin 16
GND = Pin 8

74363 OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS

The "363" is octal transparent latch coupled to eight 3-state output buffers. The two sections of the device are controlled independently by latch enable (E) and output enable ($\overline{OE}$) control gates.

Data on the D inputs are transferred to the latch outputs when the latch enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400 mV of hysteresis built in to help minimize problems that signal and ground noise can cause in the latching operation.

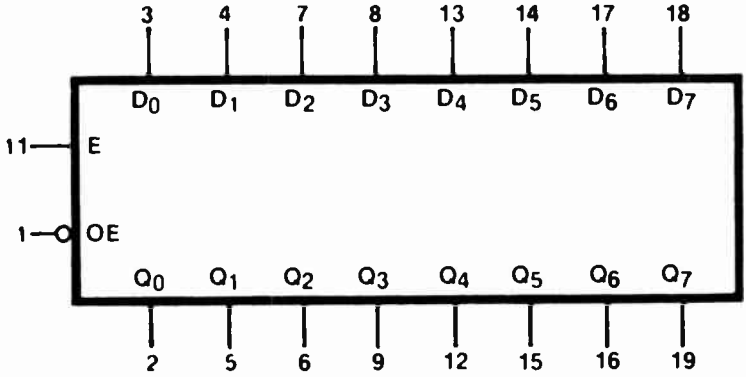
The 3-state output buffers are designed to drive heavily loaded 3-state buses, M05 memories, or MOS microprocessors. The output HIGH level differs from the normal 3-state buffer by driving the output about 1V closer to V_{cc}, or to over 3.5V at minimum V_{cc}. This feature makes these devices ideal for driving MOS memories or microprocessors with thresholds of 2.4V to 3.5V.

The active LOW output enable ($\overline{OE}$) controls all eight 3-state buffers independent of the latch operation. When $\overline{OE}$ is LOW, latched or transparent data appear at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance off state, which means they will neither drive nor load the bus.

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		$Q_0 - Q_7$
Enable & read register	L L	H H	L H	L H	L H
Latch & read register	L L	L L	l h	L H	L H
Latch register & disable outputs	H H	L L	l h	L H	(Z) (Z)

H = HIGH voltage level
h = HIGH voltage one setup time prior to the HIGH-to-LOW enable transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW enable transition
(Z) = High impedance "off" state



V_{CC} = Pin 20
GND = Pin 10

74363

74364 OCTAL D FLIP-FLOP WITH 3-STATE OUTPUTS

The "364" is an 8-bit edge-triggered register coupled to eight 3-state output buffers. The two sections of the device are controlled independently by the clock (CP) and output enable ($\overline{OE}$) control gates.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding Q output of the flip-flop. The clock buffer has about 400 mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

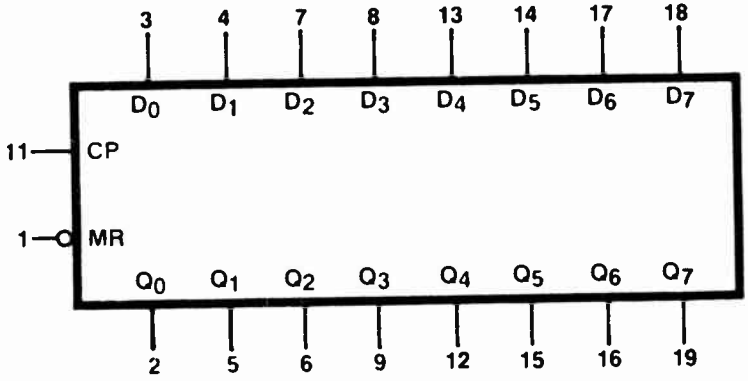
The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The output HIGH level differs from the normal 3-state buffer by driving the output about 1V closer to V_{CC}, or to over 3.5V at minimum V_{CC}. This feature makes these devices ideal for driving MOS memories or microprocessors with thresholds of 2.4V to 3.5V. The active LOW output enable ($\overline{OE}$) controls all eight 3-state buffers independent of the register operation When $\overline{OE}$ is LOW, data in the register appear at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance off state, which means they will neither drive nor load the bus.

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0-Q_7
Load & read register	L	↑	l	L	L
	L	↑	h	H	H
Load register & disable outputs	H	↑	l	L	(Z)
	H	↑	h	H	(Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
(Z) = High impedance "off" state
↑ = LOW-to-HIGH clock transition

74364

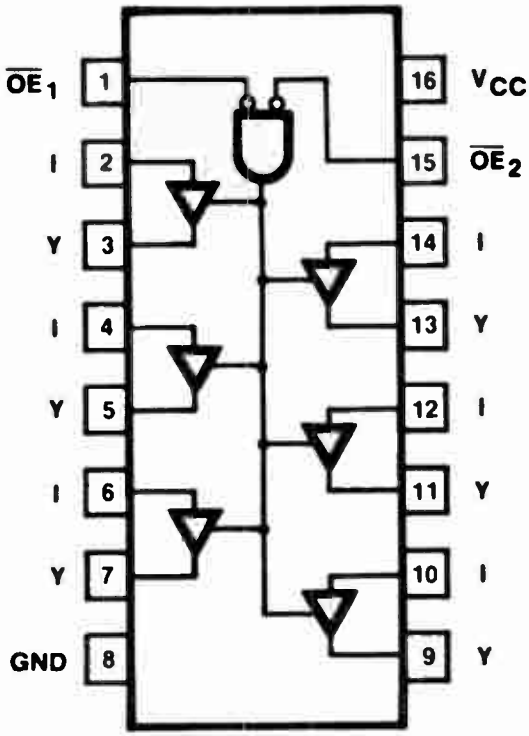


V_{CC} = Pin 20
GND = Pin 10

74364

74365 HEX BUFFER/DRIVER (3-STATE)

	74
Typ. Delay Time (ns)	12
Typ. Power Per Gate (mW)	54



74365

Truth Table

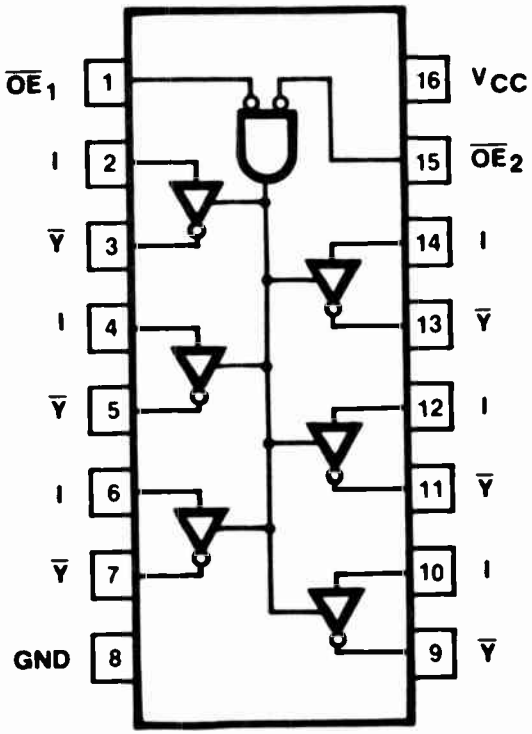
INPUTS			OUTPUTS
$\overline{OE}_1$	$\overline{OE}_2$	I	Y
L	L	L	L
L	L	H	H
X	H	X	(Z)
H	X	X	(Z)

74365

L = LOW voltage level.
H = HIGH voltage level.
X = Don't care.
(Z) = High impedance (off) state.

74366 HEX INVERTER BUFFER (3-STATE)

	74
Typ. Delay Time (ns)	11
Typ. Power Per Gate (mW)	49



74366

Truth Table

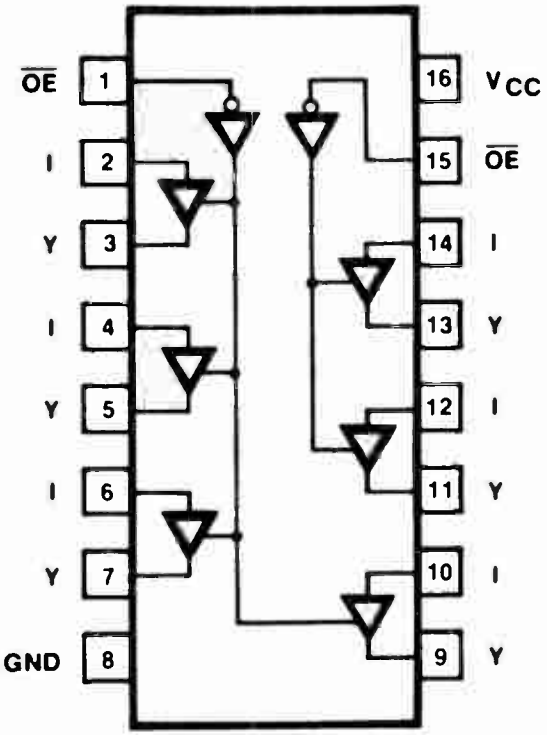
INPUTS			OUTPUTS
$\overline{OE}_1$	$\overline{OE}_2$	I	$\overline{Y}$
L	L	L	H
L	L	H	L
X	H	X	(Z)
H	X	X	(Z)

74366

L = LOW voltage level.
H = HIGH voltage level.
X = Don't care.
(Z) = High impedance (off) state.

74367 HEX BUFFER/DRIVER (3-STATE)

	74
Typ. Delay Time (ns)	12
Typ. Power Per Gate (mW)	54



74367

Truth Table

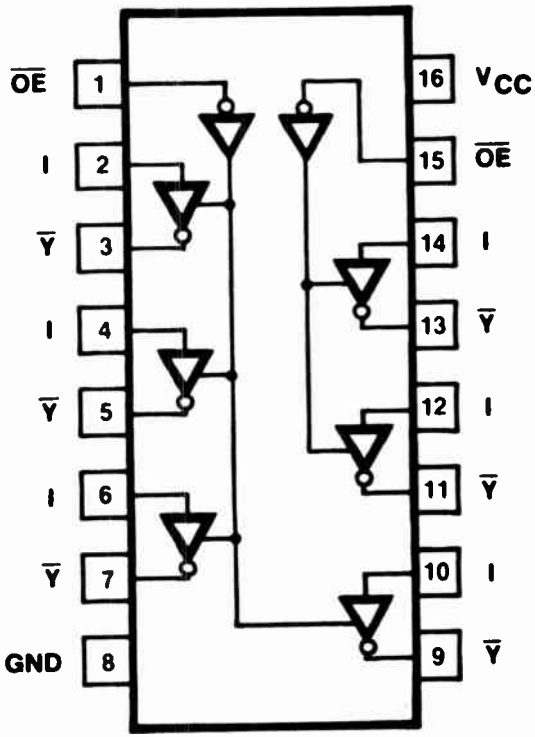
INPUTS		OUTPUTS
$\overline{OE}$	I	Y
L	L	L
L	H	H
H	X	(Z)

74367

L = LOW voltage level
H = HIGH voltage level
X = Don't care
(Z) High impedance (off) state

74368 HEX INVERTER BUFFER (3-STATE)

	74
Typ. Delay Time (ns)	11
Typ. Power Per Gate (mW)	49



74368

Truth Table

INPUTS		OUTPUTS
$\overline{OE}$	I	$\overline{Y}$
L	L	H
L	H	L
H	X	(Z)

74368

L LOW voltage level.
H HIGH voltage level.
X Don't care.
(Z) High impedance (off) state.

74373 OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS

The "373" is octal transparent latch coupled to eight 3-state output buffers. The two sections of the device are controlled independently by latch enable (E) and output enable ($\overline{OE}$) control gates.

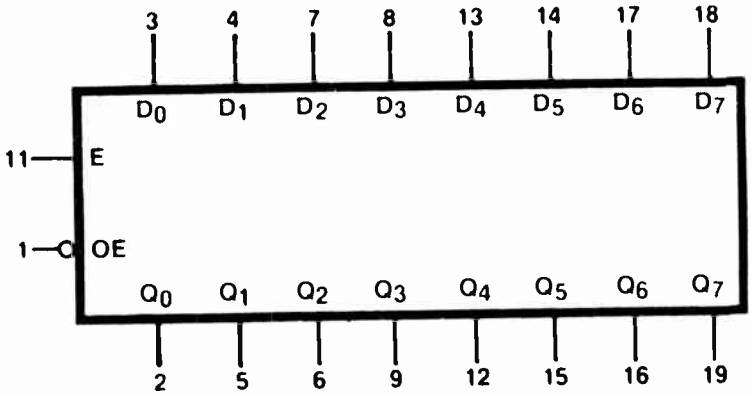
Data on the D inputs are transferred to the latch outputs when the latch enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400 mV of hysteresis built in to help minimize problems that signal and ground noise can cause in the latching operation.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The active LOW output enable ($\overline{OE}$) controls all eight 3-state buffers independent of the latch operation. When $\overline{OE}$ is LOW, latched or transparent data appear at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance off state, which means they will neither drive nor load the bus.

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS				OUTPUTS
	$\overline{OE}$	E	D_n	INTERNAL REGISTER	Q_0-Q_7
Enable & read register	L L	H H	L H	L H	L H
Latch & read register	L L	L L	l h	L H	L H
Latch register & disable outputs	H H	L L	l h	L H	(Z) (Z)

H = HIGH voltage level
h = HIGH voltage one setup time prior to the HIGH-to-LOW enable transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW enable transition
(Z) = High impedance "off" state



V_{CC} = Pin 20
GND = Pin 10

74373

74374 OCTAL D FLIP-FLOP WITH 3-STATE OUTPUTS

The "374" is an 8-bit edge-triggered register coupled to eight 3-state output buffers. The two sections of the device are controlled independently by the clock (CP) and output enable ($\overline{OE}$) control gates.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding Q output of the flip-flop. The clock buffer has about 400 mV of hysteresis built in to help minimize problems that signal and ground noise can cause in the clocking operation.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The active LOW output enable ($\overline{OE}$) controls all eight 3-state buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance off state, which means they will neither drive nor load the bus.

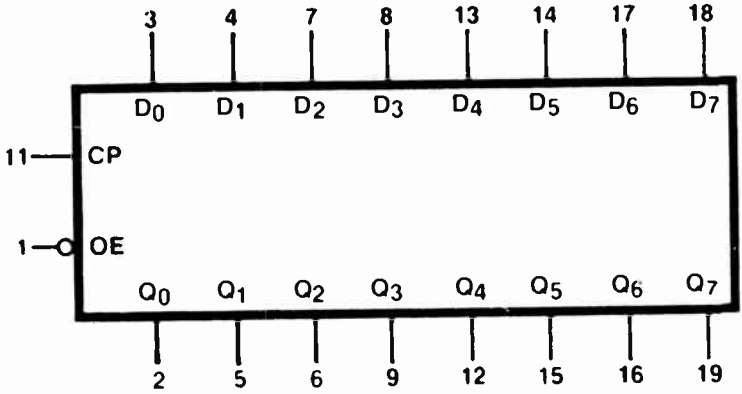
MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0-Q_7
Load & read register	L	↑	l	L	L
	L	↑	h	H	H
Load register & disable outputs	H	↑	l	L	(Z)
	H	↑	h	H	(Z)

74374

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

74374

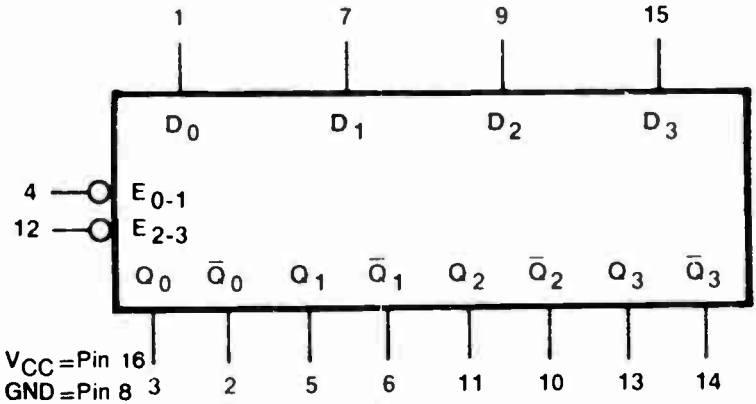


V_{CC} = Pin 20
GND = Pin 10

74374

74375 DUAL 2-BIT TRANSPARENT LATCH

The "275" has two independent 2-bit transparent latches. Each 2-bit latch is controlled by an active HIGH enable input (E). When E is HIGH, data enter the latch and appear at the Q output. The Q outputs follow the data inputs as long as E is HIGH. Data on the D inputs one setup time before the HIGH-to-LOW transition of the enable will be stored in the latch. The latched outputs remain stable as long as the enable is LOW.



74375

MODE SELECT– FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	E	D	Q	Q̄
Data Enabled	H H	L H	L H	H L
Data Latched	L	X	q	q̄

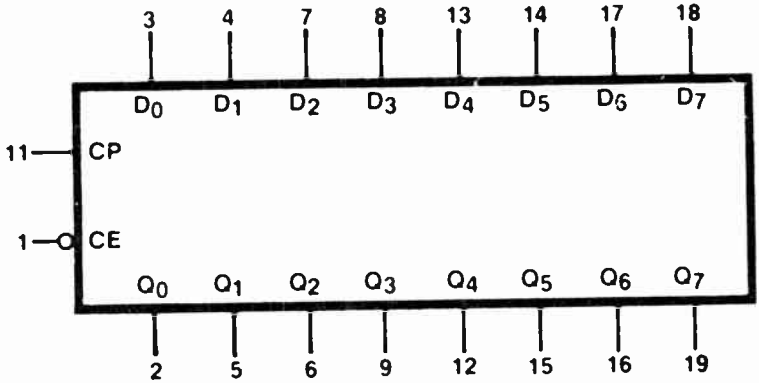
74375

H = HIGH voltage level
L = LOW voltage level
X = Don't care
q = Lower case letters indicate the state of referenced output one setup time prior to the HIGH-to-LOW Enable transition.

74377 OCTAL D FLIP-FLOP WITH CLOCK ENABLE

The "377" has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) input loads all flip-flops simultaneously when the clock enable ($\overline{CE}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding Q output of the flip-flop. The $\overline{CE}$ input is also edge-triggered, and must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.



V_{CC} = Pin 20
GND = Pin 10

74377

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{CE}$	D_n	Q_n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑	h	X	no change
	X	H	X	no change

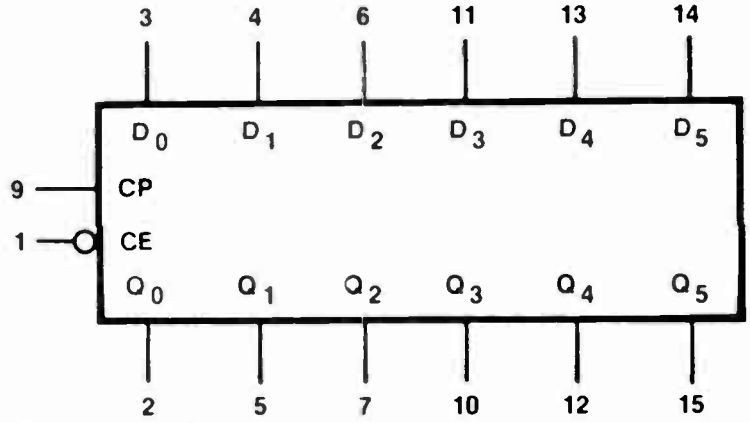
H = HIGH voltage level steady state
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

74377

74378 HEX D FLIP-FLOP WITH CLOCK ENABLE

The "378" has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) input loads all flip-flops simultaneously when the clock enable ($\overline{CE}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding Q output of the flip-flop. The $\overline{CE}$ input is also edge-triggered, and must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.



V_{CC} = Pin 16
GND = Pin 8

74378

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{CE}$	D_n	Q_n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑	h	X	no change
	X	H	X	no change

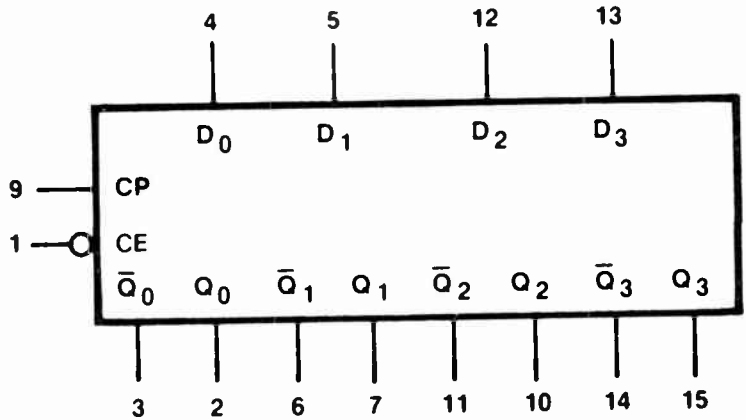
H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

74378

74379 QUAD D FLIP-FLOP WITH CLOCK ENABLE

The "379" is a quad edge-triggered D-type flip-flop with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered clock (CP) input loads all flip-flops simultaneously when the clock enable ($\overline{CE}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding Q output of the flip-flop. The $\overline{CE}$ input is also edge-triggered and must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.



V_{CC} = Pin 16
GND = Pin 8

74379

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	CP	$\overline{CE}$	D_n	Q_n	$\overline{Q}_n$
Load "1"	↑	l	h	H	L
Load "0"	↑	l	l	L	H
Hold (do nothing)	↑	h	X	no change	
	X	H	X	no change	

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

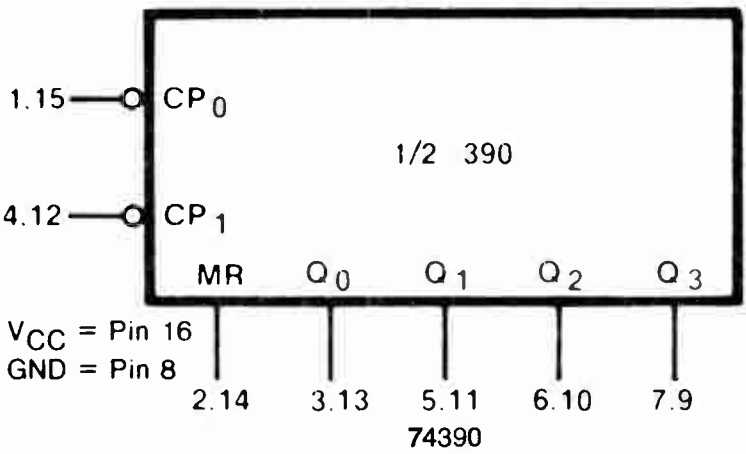
74379

74390 DUAL DECADE RIPPLE COUNTER

The "390" is dual 4-bit decade ripple counter that is divided into four separately clocked sections. The counter has two divide-by-two sections an two divide-by-five sections. The sections are normally used in a BCD decade or a biquinary configuration, because they share a common master reset input. If the two master resets can be used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clocks of each section allow ripple counter or frequency division applications of divide by two, four, five, 10, 20, 25, 50, or 100.

Each section is triggered by the HIGH-to-LOW transition of the clock ($\overline{CP}$) inputs. For BCD decade operation, the Q_0 output is connected to the $\overline{CP}1$ input of the divide-by-five section. For biquinary decade operation (50 percent duty cycle output), the Q_3 output is connected to the $\overline{CP}_0$ input, and Q_0 becomes the decade output.

The master resets (MR_a and MR_b) are active HIGH asynchronous inputs to each decade counter. These inputs operate on the portion of the counter identified by the a and b suffixes in the pin configuration. A HIGH level on the MR input overrides the clocks and sets the four outputs LOW.



BCD COUNT SEQUENCE

For 1/2 the "390"

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE

Output Q_0 is connected to input $\overline{CP}_1$ with counter input on $\overline{CP}_0$.

74390

BI-QUINARY COUNT SEQUENCE

For 1/2 the "390"

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	L	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

NOTE

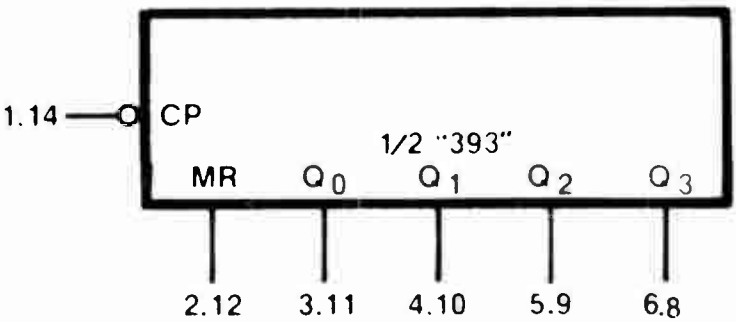
Output Q_3 is connected to input $\overline{CP}_0$ with counter input on $\overline{CP}_1$.

74390

74393 DUAL 4-BIT BINARY RIPPLE COUNTER

The "393" is a dual 4-bit binary ripple counter with separate clock and master reset inputs to each counter. The operation of each half of the "393" is the same as the "93" except no external clock connections are required. The counters are triggered by a HIGH-to-LOW transition of the clock ($\overline{CP}_a$ and $\overline{CP}_b$) inputs. The counter outputs are internally connected to provide clock inputs to succeeding stages. The outputs are designed to drive the internal flip-flops plus the rated fanout of the device. The outputs of the ripple counter do not change synchronously and should not be used for high-speed address decoding.

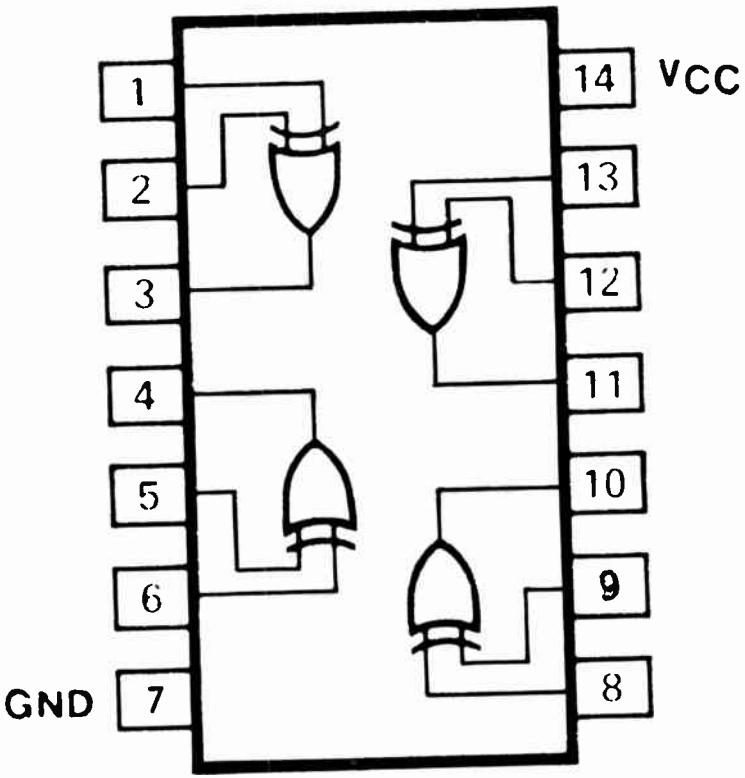
The master resets (MR_a and MR_b) are active HIGH asynchronous inputs to each 4-bit counter identified by the a and b suffixes in the pin configuration. A HIGH level on the MR input overrides the clock and sets the outputs LOW.



74393

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

COUNT SEQUENCE FOR 1 2 THE "393" 74393



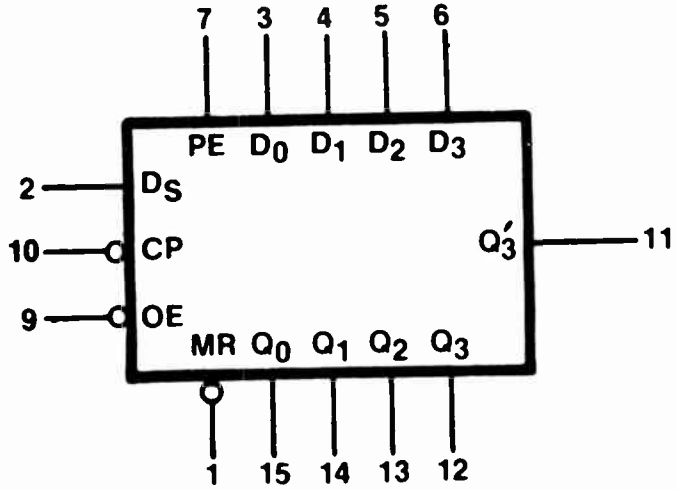
74393

74395 4-BIT CASCADABLE SHIFT REGISTER WITH 3-STATE OUTPUTS

The "395" is a 4-bit shift register with serial and parallel synchronous operating modes and four 3-state buffer outputs. The shifting and loading operations are controlled by the state of the parallel enable (PE) input. When PE is HIGH, data are loaded from the parallel data inputs (D_0-D_3) into the register synchronous with the HIGH-to-LOW transition of the clock input ($\overline{CP}$). When PE is LOW, data at the serial data input (D_S) are loaded into the Q_0 flip-flop, and data in the register are shifted one bit to the right in the direction ($Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$) synchronous with the negative clock transition. The PE and data inputs are fully edge-triggered and must be stable only one setup prior to the HIGH-to-LOW transition of the clock. The master reset ($\overline{MR}$) is an asynchronous active LOW input. When LOW, the $\overline{MR}$ overrides the clock and all other inputs and clears the register.

The 3-state output buffers are designed to drive heavily loaded 3-state buses or large capacitive loads. The active LOW output enable ($\overline{OE}$) controls all four 3-state buffers independent of the register operation. Data in the register appear at the outputs when $\overline{OE}$ is LOW. The outputs are in the high-impedance off state, which means they will neither drive nor load the bus when $\overline{OE}$ is HIGH. The output from the last stage is brought out separately. This output (Q_3') is tied to the serial data input (D_S) of the next register for serial expansion applications. The Q_3' output is not affected by the 3-state buffer operation.

	74LS
Shift Frequency (MHz)	25
Serial Data Input	D
Asynchronous Clear	Low
Shift-Right Mode	Yes
Shift-Left Mode	No
Load Mode	Yes
Hold Mode	No
Typ. Total Power (mW)	75



V_{CC} = Pin 16
GND = Pin 8

74395

MODE SELECT—FUNCTION TABLE

REGISTER OPERATING MODE	INPUTS					OUTPUTS			
	$\overline{MR}$	$\overline{CP}$	PE	D_S	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	L	X	X	X	X	L	L	L	L
Shift right	H H	↓ ↓	l l	l h	X X	L H	q_0 q_0	q_1 q_1	q_2 q_2
Parallel load	H H	↓ ↓	h h	X X	l h	L H	L H	L H	L H

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS	
	$\overline{OE}$	Q_n (register)	Q_0,Q_1,Q_2,Q_3	Q'_3
Read	L L	L H	L H	L H
Disable buffers	H H	L H	(Z) (Z)	L H

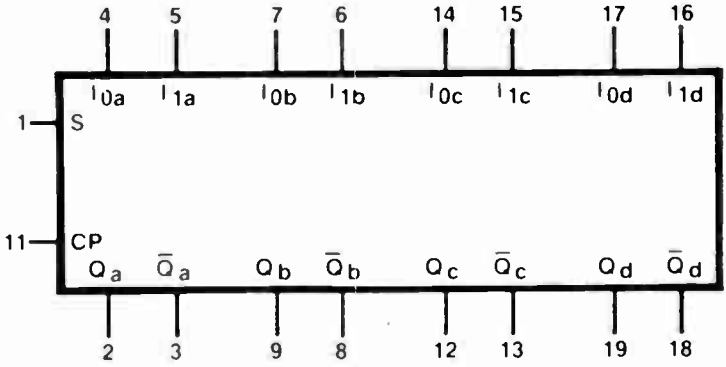
H = HIGH voltage level
h = HIGH voltage level one setup time prior to the HIGH-to-LOW clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW clock transition
q_n = Lower letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW clock transition
X = Don't care
(Z) = High impedance "off" state
↓ = HIGH-to-LOW transition

74395

74398 QUAD 2-PORT REGISTER

The "398" is a high-speed quad 2-port register. It selects four bits of data from two sources (ports) under the control of a common select input (S). The selected data is loaded into four edge-triggered flip-flops synchronous with the LOW-to-HIGH transition of the common buffered clock input (CP). The four flip-flops are combined to form a synchronous 4-bit register with both true and complement outputs available.

The operation of the device is fully synchronous. The data inputs (I_0 and I_1) and the select input (S) must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.



V_{CC} = Pin 20
GND = Pin 10

74398

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	CP	S	I_0	I_1	Q_n	$\bar{Q}_n$
Load Source "0"	↑	l	l	X	L	H
	↑	l	h	X	H	L
Load Source "1"	↑	h	X	l	L	H
	↑	h	X	h	H	L

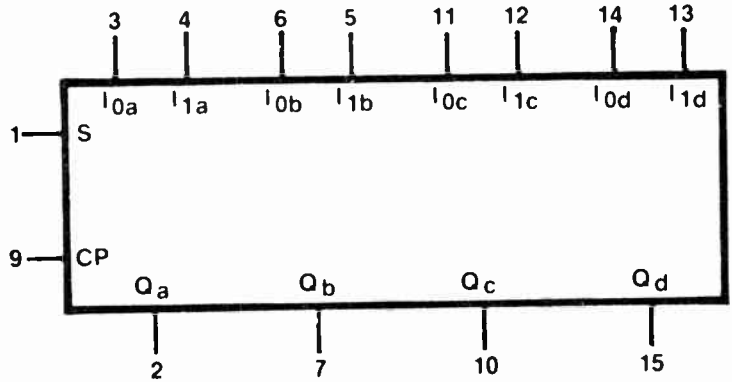
H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't care
↑ = LOW-to-HIGH clock transition

74398

74399 QUAD 2-PORT REGISTER

The "399" is a high-speed quad 2-port register. It selects four bits of data from two sources (ports) under the control of a common select input (S). The selected data is loaded into 4-bit output register synchronous with the LOW-to-HIGH transition of the clock input (CP).

The operation of the device is fully synchronous. The data inputs (I_0 and I_1) and the select input (S) must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.



V_{CC} = Pin 16
GND = Pin 8

74399

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS
	CP	S	I_0	I_1	Q_n
Load Source "0"	↑	l	l	X	L
	↑	l	h	X	H
Load Source "1"	↑	h	X	l	L
	↑	h	X	h	H

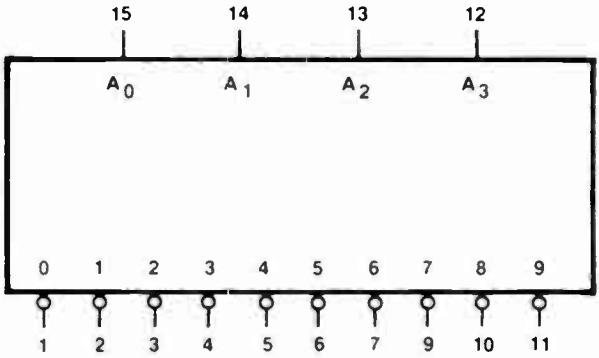
H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't care
↑ = LOW-to-HIGH clock transition

74399

74445 BCD-TO-DECIMAL DECODER/DRIVER (O.C.)

The "445" is a 1-of-10 decoder with open collector outputs. This decoder accepts BCD inputs on the A_0 to A_3 address lines and generates 10 mutually exclusive active LOW outputs. When an input code greater than 9 is applied, all outputs are HIGH. This device can therefore be used as a one-of-eight decoder with A_3 used as an active LOW enable.

The "445" features an output breakdown voltage of 7V. This device is ideal as a lamp or solenoid driver.



V_{CC} = Pin 16
GND = Pin 8

74445

Truth Table

A_3	A_2	A_1	A_0	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage levels
L = LOW voltage levels

74445

74490 DUAL BCD DECADE RIPPLE COUNTER

The "490" is a dual BCD decade ripple counter with separate clock, master set and master reset inputs to each counter. The operation of each half of the "490" is the same as the "90" used in the BCD decade mode.

The counters are triggered by the HIGH-to-LOW transition of the clock ($\overline{CP}$) inputs. No external connections are required to get the full BCD (8421) decade counting scheme from the counters. The counter outputs are internally connected as clock or decoded inputs to succeeding stages. The outputs are designed to drive the internal gates plus the rated fanout of the device. Because this is a ripple-type counter, the outputs do not change synchronously and should not be used for high-speed address decoding.

The master set (MS) and master reset (MR) are asynchronous active HIGH inputs. The HIGH MR input overrides the clock and clears the associated 4 bits of the counter. The HIGH MS input overrides the clock and MR inputs and sets the associated 4 bits to 9 (HLLH).

MODE SELECTION—
FOR 1/2 THE "490"

RESET/SET INPUTS		OUTPUTS			
MR	MS	Q_0	Q_1	Q_2	Q_3
H	X	L	L	L	L
X	H	H	L	L	H
L	L	Count			

H = HIGH voltage level
L = LOW voltage level
X = Don't care

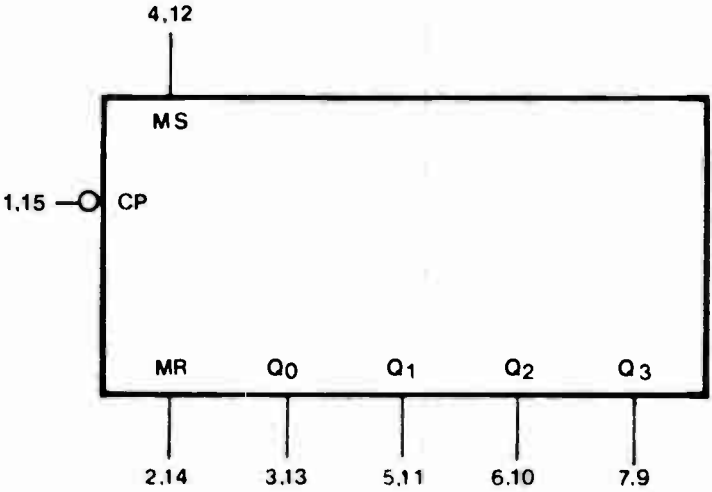
74490

BCD COUNT SEQUENCE—
FOR 1/2 THE "490"

	OUTPUT			
COUNT	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE
Output Q_0 connected to input $\overline{CP}_1$

74490



V_{CC} = Pin 16
GND = Pin 8

74490

74568 BCD DECADE UP/DOWN SYNCHRONOUS COUNTER (3-STATE)

The "568" is a synchronous presettable BCD decade up/down counter featuring an internal carry look ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the flip-flops on the LOW-to-HIGH transition of the clock.

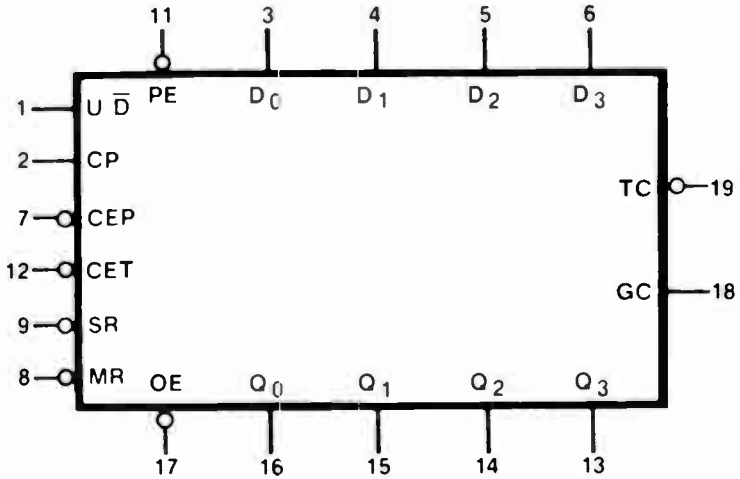
The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock and takes place regardless of the levels of the count-enable inputs. A LOW level on the parallel enable ($\overline{PE}$) inputs disables the counter and causes the data at the D_n inputs to be loaded into the counter on the next LOW-to-HIGH transition of the clock. The synchronous reset ($\overline{SR}$), when LOW one setup time before the LOW-to-HIGH transition of the clock, overrides the $\overline{CEP}$, $\overline{CET}$ and $\overline{PE}$ inputs, and causes the flip-flops to go LOW coincident with the positive clock transition. The master reset ($\overline{MR}$) is an asynchronous overriding clear function which forces all stages to a LOW state while the $\overline{MR}$ input is LOW without regard to the clock.

The carry look ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs ($\overline{CET} \cdot \overline{CEP}$) and a terminal count ($\overline{TC}$) output. Both count-enable inputs must be LOW to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output, thus enabled, will produce a LOW output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This LOW level $\overline{TC}$ pulse is used to enable successive cascaded stages. See the "168" data for the fast synchronous multistage counting connections.

The gated clock output (GC) is a terminal count output that provides a HIGH-LOW-HIGH pulse for a duration equal to the LOW time of the clock pulse when $\overline{TC}$ is LOW. The GC output can be used as a clock input for the next stage in a simple ripple expansion scheme.

The direction of counting is controlled by the up/down (U/$\overline{D}$) input; a HIGH will cause the count to increase, and a LOW will cause the count to decrease.

The active LOW output enable ($\overline{OE}$) input controls the 3-state buffer outputs independent of the counter operation. When $\overline{OE}$ is LOW, the count appears at the buffer outputs. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance off state, which means they will neither drive nor load the bus.



V_{CC} = Pin 20
GND = Pin 10

74568

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS
	$\overline{OE}$	Q_n - Counter	Q_0,Q_1,Q_2,Q_3
Read counter	L L	L H	L H
Disable outputs	H H	L H	(Z) (Z)

74568

MODE SELECT—FUNCTION TABLE

COUNTER OPERATING MODES	INPUTS								COUNTER STATES			
	$\overline{MR}$	CP	$\overline{SR}$	U/$\overline{D}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	D_n	Q_0	Q_1	Q_2	Q_3
Asynchronous Reset	L	X	X	X	X	X	X	X	L	L	L	L
Synchronous Reset	H	↑	l	X	X	L	L	X	L	L	L	L
Parallel load	H H	↑ ↑	h h	X X	l l	X X	X X	l h	L H	L H	L H	L H
Count up	H	↑	h	h	h	l	l	X	count up			
Count down	H	↑	h	l	h	l	l	X	count down			
Hold (do nothing)	H H	↑ ↑	h h	X X	h h	h X	X h	X X	no change no change			

TERMINAL COUNT TRUTH TABLE

INPUTS				COUNTER STATES				OUTPUTS	
CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	Q_0	Q_1	Q_2	Q_3	$\overline{TC}$	GC
H	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L
X	L	H	L	L	L	L	L	L	H
X	L	X	H	L	L	L	L	H	H
H	H	L	L	H	X	X	H	L	H
L	H	L	L	H	X	X	H	L	L
X	H	H	L	H	X	X	H	L	H
X	H	X	H	H	X	X	H	H	H

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW to HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW to-HIGH clock transition
X = Don't care
(Z) = High impedance "off" state
↑ = LOW-to-HIGH clock transition

74568

74569 4-BIT BINARY UP/DOWN SYNCHRONOUS COUNTER (3-STATE)

The "569" is a synchronous presettable modulo 16 binary up/down counter featuring an internal carry look ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the flip-flops on the LOW-to-HIGH transition of the clock.

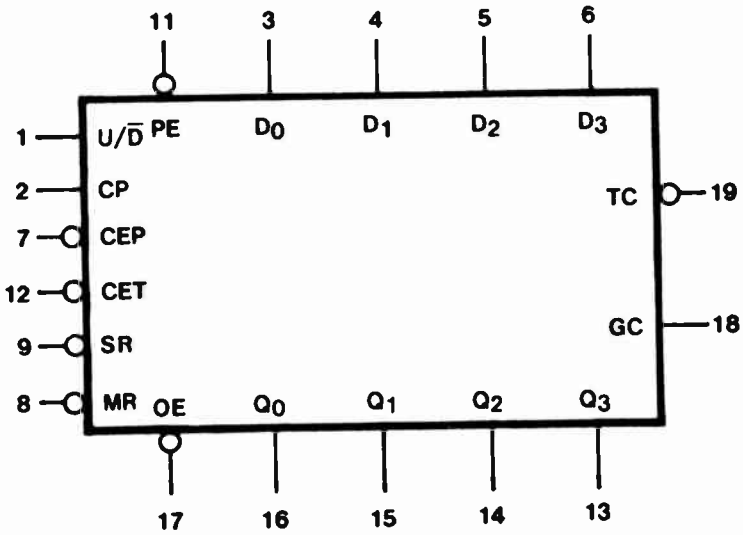
The counter is fully programmable; that is , the outputs may be preset to either level. Presetting is synchronous with the clock and takes place regardless of the levels of the count enable inputs. A LOW level on the parallel enable ($\overline{PE}$) input disables the counter and causes the data at the D_n inputs to be loaded into the counter on the next LOW-to-HIGH transition of the clock. The synchronous reset ($\overline{SR}$), when LOW one setup time before the LOW-to-HIGH transition of the clock, overrides the $\overline{CEP}$, $\overline{CET}$ and $\overline{PE}$ inputs, and cause the flip-flops to go LOW coincident with the positive clock transition. The master rest ($\overline{MR}$) is an asynchronous overriding clear function, which forces all stages to a LOW state while the $\overline{MR}$ input is LOW without regard to the clock.

The carry look ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count enable inputs ($\overline{CET} \cdot \overline{CEP}$) and a terminal count ($\overline{TC}$) output. Both count-enable inputs must be LOW to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ outputs. The $\overline{TC}$ output, thus enabled, will produce a LOW output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This LOW level $\overline{TC}$ pulse is used to enable successive cascaded stages. See the 74169 data for the fast synchronous multistage counting connections.

The gates clock output (GC) is a terminal count output that provides a HIGH-LOW-HIGH pulse for a duration equal

to the LOW time of the clock pulse when $\overline{TC}$ is LOW. The GC output can be used as a clock input for the next stage in a simple ripple expansion scheme. The direction of counting is controlled by the up/down (U/$\overline{D}$) input; a HIGH will cause the count to increase, and a LOW will cause the count to decrease.

The active LOW output enable ($\overline{OE}$) input controls the 3-state buffer outputs independent of the counter operation. When $\overline{OE}$ is LOW, the count appears at the buffer outputs. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance off state, which means they will neither drive nor load the bus.



V_{CC} = Pin 20
GND = Pin 10

74569

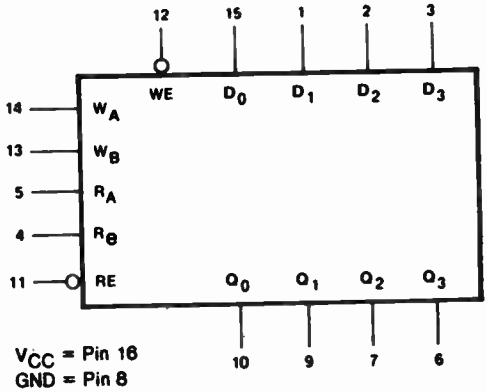
74670 4×4 REGISTER FILE (3-STATE)

The "670" is a 16-bit 3-state register file organized as 4 words of 4 bits each. Separate read and write address and enable inputs are available permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four data inputs. The Write Address inputs (W_a and W_b) determine the location of the stored word. When the write enable ($\overline{WE}$) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the $\overline{WE}$ is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-state outputs. Data and write address inputs are inihibited when $\overline{WE}$ is HIGH.

Direct acquistion of data stored in any of the four registers is made possible by individual read address inputs (R_a and R_b). The addressed word appears at the four outputs when the read enable ($\overline{RE}$) is LOW. Data outputs are in the high-impedance off state when the read enable input is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-state outputs together. Because the limiting factor for expansion is the output HIGH current, further stacking is possible by tying pullup resistors to the outputs to increase the I_{OH} current available. Design of the read enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the enable and address inputs of each device in parallel.

	74LS
Typ. Address Time (ns)	24
Typ Read Enable Time (ns)	19
Data Input Rate (MHz)	20
Typ. Total Power (mW)	135



74670

WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES(b)
	$\overline{WE}$	D_n	
Write Data	L	L	L
	L	H	H
Data Latched	H	X	no change

NOTE

b The Write Address (W_A & W_B) to the "internal latches" must be stable while $\overline{WE}$ is LOW for conventional operation

74670

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUTS
	$\overline{RE}$	INTERNAL LATCHES(c)	Q_n
Read	L	L	L
	L	H	H
Disabled	H	X	(Z)

NOTE

c. The Read Address (R_A & R_B) changes to select the "internal latches" are not constrained by $\overline{WE}$ or $\overline{RE}$ operation.

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance "off" state

74670

Symbols and Definitions

DC VOLTAGES

All voltages are referenced to ground. Negative voltage limits are specified as absolute values (i.e., 10V is greater than -1.0V).

V_{CC} Supply voltage: The range of power supply voltage over which the device is guaranteed to operate within the specified limits.

V_{CD} (Max) Input clamp diode voltage: The most negative voltage at an input when the specified current is forced out of that input terminal. This parameter guaranteed the integrity of the input diode intended to clamp negative ringing at the input terminal.

V_{IH} Input HIGH voltage: The range of input voltages recognized by the device as a logic HIGH.

V_{IH} (Min) Minimum Input HIGH voltage: This value is the guaranteed input HIGH threshold for the device. The minimum allowed input HIGH in a logic system.

V_{IL} Input LOW voltage: The range of input voltages recognized by the device as a logic LOW.

V_{IL} (Max) Maximum input LOW voltage: This value is the guaranteed input LOW threshold for the device. The maximum allowed input LOW in a logic system.

V_M Measurement voltage: The reference voltage level on ac waveforms for determining ac performance. Usually specified as 1.5V for most TTL families, but 1.3V for the low-power Schottky 74LS family.

V_{OH} (Min) Output HIGH voltage: The minimum guaranteed HIGH voltage at an output terminal for the specified output current I_{OH} and at the minimum Vcc value.

V_{OL} (Max) Output LOW voltage: The minimum guaranteed LOW voltage at an output terminal sinking the specified load current I_{OL}.

V_{T+} Positive-going threshold voltage: The input voltage of a variable threshold device which causes operation according to specification as the input transition rises from below V_{T-}(Min).

V_{T-} Negative-going threshold voltage: The input voltage of a variable threshold device which causes operation according to specification as the input transition falls from above V_{T+}(Max).

DC CURRENTS

Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

Icc Supply current: The current flowing into the Vcc supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst case operation unless specified.

I_I Input leakage current: The current flowing into an input when the maximum allowed voltage is applied to the input. This parameter guaranteed the minimum breakdown voltage for the input.

I_{IH} Input HIGH current: The current flowing into an input when a specified HIGH level voltage is applied to that input.

I_{IL} Input LOW current: The current flowing out of an input when a specified LOW level voltage is applied to that input.

I_{OH} Output HIGH current: The leakage current flowing into a turned off open collector output with a specified HIGH

output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the HIGH state.

I_{OL} Output LOW current: The current flowing into an output which is in the LOW state.

I_{OS} Output short-circuit current: The current flowing out of an output which is in the HIGH state when that output is short circuit to ground.

I_{OZH} Output off current HIGH: The current flowing into a disabled 3-state output with a specified HIGH output voltage applied.

I_{OZL} Output off current LOW: The current flowing out of a disabled 3-state output with a specified LOW output voltage applied.

AC SWITCHING PARAMETERS AND DEFINITIONS

f_{MAX} The maximum clock frequency: The maximum input frequency at a clock input for predictable performance. Above this frequency the device may cease to function.

t_{PLH} Propagation delay time: The time between the specified reference points on the input and output waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} Propagation delay time: The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level.

t_{PHZ} Output disable time from HIGH level of a 3-state output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the HIGH level to a high impedance off state.

t_{PLZ} Output disable time from LOW level of a 3-state output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the LOW level to a high impedance off state.

t_{PZH} Output enable time to a HIGH level of a 3-state output: The delay time between the specified reference points on

the input and output voltage waveforms with the 3-state output changing from a high impedance off state to the HIGH level.

t_{PZL} Output enable time to a LOW level of a 3-state output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high impedance off state to the LOW level.

t_h Hold time: The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s Setup time: The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_w Pulse width: The time between the specified reference points on the leading and trailing edges of a pulse.

t_{rec} Recovery time: The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.