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# abc's of FET's

by Rufus P. Turner

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# Preface

Although the field-effect transistor (FET), as its name clearly indicates, is a member of the fast-growing family of transistors, it is so distinctive in a number of ways that it deserves to be considered a special semiconductor device. Indeed, because of its uniqueness, the FET is regarded by some technologists as a "transistorlike" device, rather than as a transistor *per se*.

The electrical characteristics of the FET suit it to many applications formerly pre-empted by the vacuum tube, sometimes even to the partial exclusion of the conventional (bipolar) transistor. The FET brings to such applications tubelike operation plus the well-known advantages of the bipolar transistor: small size, mechanical ruggedness, cool operation, high efficiency, and modest operating-power requirements.

In this book, I have tried to describe the FET in simple language. The presentation is offered to technicians and others who want to know how FET's work and how to use them.

RUFUS P. TURNER

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## CHAPTER 4

CHAPTER 1

# Basic Theory of the FET

The *field-effect transistor* (abbreviated FET) is a special semiconductor device. Although it is similar to the regular transistor (technically known as the *bipolar* transistor), it differs from the latter in several respects. The most important of these is the high input impedance of the FET, compared with the relatively low input impedance of the bipolar transistor. This means that the input signal for a FET can be a voltage at practically zero power level, whereas the input signal of a bipolar transistor must be a current at a significant, though low, power level.

Because the FET employs an input-signal voltage electrostatically to control an output-signal current, its operation strongly resembles that of the vacuum tube. The FET shares with the vacuum tube the properties of transconductance and good input/output isolation, in addition to high power gain and voltage-dependent operation. At the same time, because the FET is an active semiconductor device, it also resembles the bipolar transistor. The FET shares with the bipolar transistor the properties of low power-supply requirements, efficient dc power conversion, the control of

current carriers in a solid material, small size, light weight, mechanical ruggedness, cool operation, and freedom from microphonics. In several respects, the FET is better than either the tube or the bipolar transistor.

This chapter describes the FET and explains its operation. The discussion is presented in simple language with a minimum of mathematics, and presupposes that the reader already knows how a conventional bipolar transistor works.

## *1.1 FET TYPES*

The conventional transistor is called *bipolar* because it employs two types of current carrier (both electrons and holes in a single transistor) in its operation. The field-effect transistor is called *unipolar* because it employs only one type of carrier (either electrons *or* holes, depending on whether the FET is made from N-type or P-type semiconductor material).

The field-effect transistor has three principal electrodes: *source, drain,* and *gate.* These correspond to the emitter, collector, and base, respectively, of the bipolar transistor, and to the cathode, plate, and grid, respectively, of the vacuum tube. In practical terms, one may think of the drain and the source as the anode and the cathode of the device, and of the gate as the control element. Some FET's are *single gate;* others are *dual gate.* Fig. 1-1 shows a simple black-box representation of a single-gate FET, illustrating the relationship of electrode terminals. A FET is termed *symmetrical* when the source and drain terminals may be interchanged without affecting its operation. It is termed *asymmetrical* when the designated source and drain terminals cannot be interchanged without impairing the performance of the device. Most FET's presently manufactured fall into this second class.

Field-effect transistors are classified as *junction FET's* (JFET's) and *metal-oxide semiconductor FET's* (MOSFET's). The MOSFET is known also as an *insulated-gate FET* (IGFET) for reasons that will be explained later. Junction FET's may be further classified according to whether the largest portion is made from N-type or P-

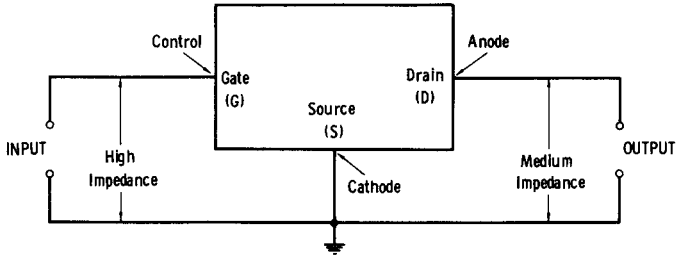



**Fig. 1-1. Black-box representation of a single-gate FET.**

type semiconductor material (N-channel JFET's and P-channel JFET's, respectively). MOSFET's are classified according to their intended mode of operation (*depletion* mode, *enhancement* mode, or *depletion/enhancement* mode, explained later in Section 1.4) and further classified as N-channel or P-channel depending on the type of material used for the drain and source. The entire family of field-effect transistors thus may be classified, at this writing, according to the following outline:

I. JUNCTION FET (JFET)
   A. N-channel JFET (N-type semiconductor)
   B. P-channel JFET (P-type semiconductor)
II. METAL-OXIDE SEMICONDUCTOR FET (MOSFET or IGFET)
   A. N-channel MOSFET
      1. Depletion Mode
      2. Depletion/Enhancement Mode
      3. Enhancement Mode
   B. P-channel MOSFET
      1. Depletion Mode
      2. Depletion/Enhancement Mode
      3. Enhancement Mode

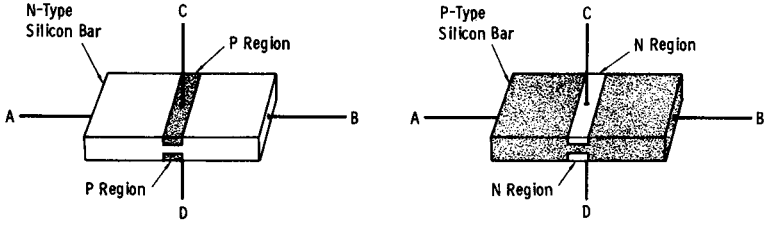
Additionally, JFET's and MOSFET's may be classified as *single gate* or *dual gate*. Most types are the former.

## *1.2 JFET: STRUCTURE AND OPERATION*

Fig. 1-2 shows the basic structure of the junction field-effect transistor (JFET). An N-channel JFET is shown in

Fig. 1-2A, and a P-channel JFET is shown in Fig. 1-2B. Some manufactured FET's look quite different from these simple illustrations, but the latter show the basic geometry well enough for purposes of explanation.

The JFET consists essentially of a small, thin bar of silicon (occasionally germanium) to each end of which an ohmic (nonrectifying) connection (A, B) is made. This silicon bar may be N type (as in Fig. 1-2A) or P type (as in Fig. 1-2B). On each opposite face of the bar, a controlled amount of doping material is diffused in to create two, parallel facing strips of the opposite kind of silicon. Thus, two P-type strips are created in the N-type bar (Fig. 1-2A) where each forms a P-N junction, and two N-type strips

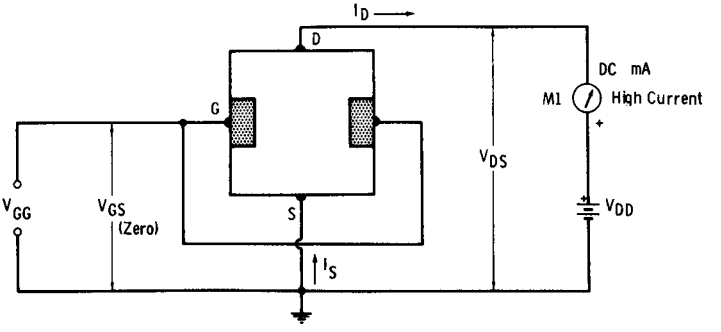



(*A*) *N-channel JFET.* (*B*) *P-channel JFET.*

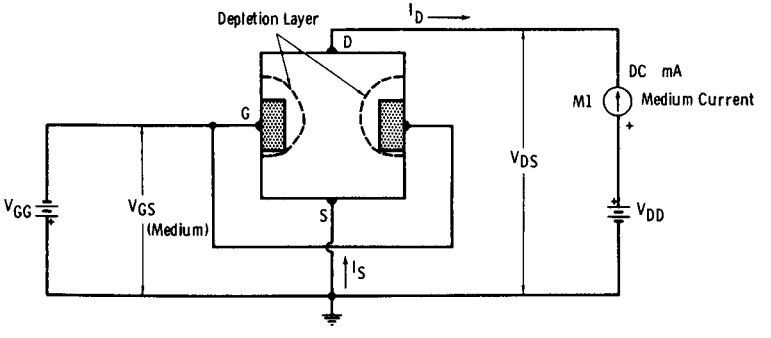
**Fig. 1-2. Basic structure of the junction field-effect transistor (JFET).**

are created in the P-type bar (Fig. 1-2B) where each forms an N-P junction. In a similar fashion, two dots or two squares might be used instead of two strips, provided they are parallel. A connection (C, D) is made to each of the strips, and the basic FET is complete. One of the end-of-bar terminals (A or B) will be the *source* electrode, and the other will be the *drain* electrode. If the FET is symmetrical, either A or B may be the source. The two strip junctions constitute the *gate* electrode, and are usually tied together internally and connected to a single terminal.

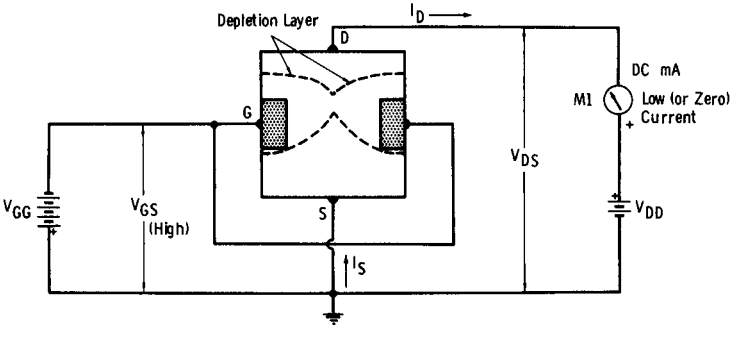
Fig. 1-3 illustrates JFET operation. In each of the three examples here, an N-channel JFET is shown, and the source electrode is the common (grounded) terminal. The gate-to-source circuit is the input, and the drain-to-source circuit is the output. One dc voltage ($V_{DS}$ from the supply $V_{DD}$) biases the drain/source (output) half, and another dc volt-




*(A) Zero gate voltage.*




*(B) Medium gate voltage.*




*(C) High gate voltage.*

**Fig. 1-3. JFET operation.**

age ($V_{GS}$ from the supply $V_{GG}$) biases the gate/source (input) half. In each of the three examples, voltage $V_{DS}$ has the same value.

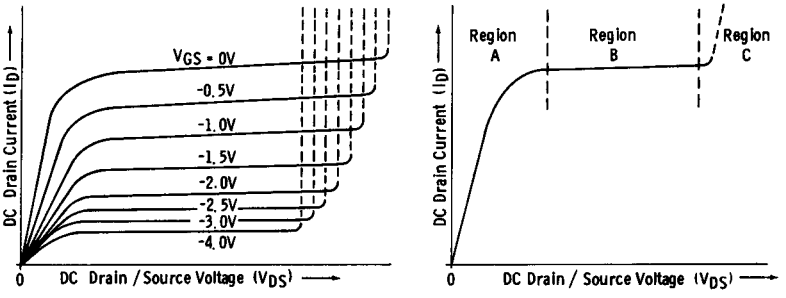
In Fig. 1-3A, $V_{GS}$ is zero, and the drain current ($I_D$) (S to D in the silicon bar) is relatively high. This current path inside the bar is termed the *channel.* The drain current in this instance is proportional to the resistance of the channel.

When a moderate voltage, $V_{GS}$, is applied between the gate and source such that the gate junction is reverse biased, as in Fig. 1-3B, a depletion layer is set up in the normal manner for P-N junctions, around each junction. (A depletion layer is a region that is almost completely free of current carriers; therefore, it acts like a dielectric.) The depletion layers penetrate into the bar, toward each other, and thus reduce the width of the channel. Because fewer current carriers can pass through, $I_D$ is reduced in value, being proportional to gate voltage $V_{GS}$. Since the gate junction is reverse biased, there is virtually no gate current; therefore, the gate/source (input) resistance is very high (resistances of 1000 megohms are found in JFET's).

When a high reverse voltage ($V_{GS}$) is applied between gate and source, as in Fig. 1-3C, the depletion layers penetrate deeper into the bar, further narrowing the channel width and reducing drain current $I_D$ to a value still lower than that in Fig. 1-3B. When $V_{GS}$ is sufficiently high, the depletion layers practically touch each other, blocking the channel and reducing $I_D$ to almost zero. This cutoff point is similar to plate-current cutoff, which occurs in a tube when the negative grid voltage reaches a critical high value.

It is in this way that the JFET uses an input voltage to control an output current. The control mechanism in this operation is the voltage-dependent widening of the depletion layers; and, since the layer is largely the effect of an electrostatic field at the gate junction, the name *field-effect transistor* applies perfectly. The family of transfer curves in Fig. 1-4A illustrates JFET operation. From these plots, and the single curve shown in Fig. 1-4B, note that for a given value of $V_{GS}$, the drain current increases very rapidly at first as $V_{DS}$ is slowly increased from zero, then reaches a knee and levels off. The corresponding rapid-rise region A

from zero to the knee is termed the *ohmic* region, and $I_D$ in this region is proportional principally to $V_{DS}$ and the channel resistance. The flattened region B is termed the *saturation* or *pinchoff* region, and $I_D$ in this region is limited principally by the channel width resulting from the widening of the depletion layers. In region C, which is indicated by the steep, dotted rise of the curve, $I_D$ increases catastrophically as $V_{DS}$ is increased only a small amount above a critical high value that depends on the model of FET. This latter region is termed the *avalanche* or *breakdown* region, and is




(*A*) *Family.* (*B*) *Individual.*

**Fig. 1-4. Typical JFET performance.**

recognized as similar to the same type of sudden current rise that typifies the performance of zener diodes and avalanche diodes. Unless $I_D$ is limited (as by means of a suitable external series resistor), operation in region C may result in burnout of the FET. Region A is sometimes called the *triode* region because the shape of the curve in this region resembles the response of a triode tube. Similarly, region B is sometimes called the *pentode* region because the shape of the curve in this region resembles that of a pentode tube. The arrangements in Fig. 1-3, by means of which the performance data shown in Fig. 1-4 could be obtained, correspond to the common-emitter bipolar-transistor circuit and to the common-cathode vacuum-tube circuit.

In the operation illustrated by Figs. 1-3 and 1-4, the gate bias voltage is either zero or negative. It is apparent, however, from the curves in Fig. 1-4A that if the gate/source voltage, $V_{GS}$, is made positive, the $I_D$ values will be higher

than those shown in the curves. But if this is done, the gate junction will no longer be reverse biased and, like any other forward-biased junction, it will draw significant current from the $V_{GG}$ supply. The gate-junction resistance accordingly will be lowered, and the high-input-impedance feature of the FET will be lost.

Fig. 1-3 and the accompanying explanation concern the operation of N-channel JFET's. A P-channel JFET (Fig. 1-2B) operates in a similar manner. But if a P-channel JFET is used, the polarity of each of the bias supplies ($V_{DD}$ and $V_{GG}$) and that of the milliammeter (M1 in Fig. 1-3) must be reversed; i.e., the drain must be biased negative and the gate must be biased positive. Note, however, that the positive gate of the P-channel JFET represents reverse bias, which, in turn, means high gate resistance.

Since the $V_{GS}$ bias polarity shown in Fig. 1-3 is correct for high gate resistance, gate current ($I_G$) is virtually zero. This means that the source current ($I_S$), corresponding to the cathode current of a tube or the emitter current of a common-emitter-connected bipolar transistor, is in this instance the drain current, $I_D$. If the gate were forward-biased, as explained two paragraphs ago, then $I_G$ would become a significant part of $I_S$.


*(A) Single gate.* *(B) Dual gate.*

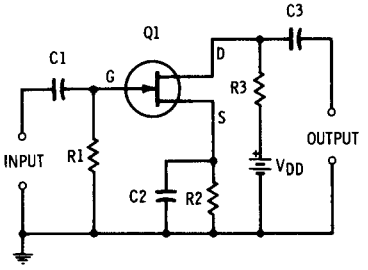
**Fig. 1-5. Circuit symbols for the JFET.**

It is interesting to note that in the JFET, current carriers ($I_D$) flow through a single polarity of semiconductor material; they do not flow across junctions as they do in the bipolar transistor. One of the resulting advantages is the absence of the noise components caused by junction currents.

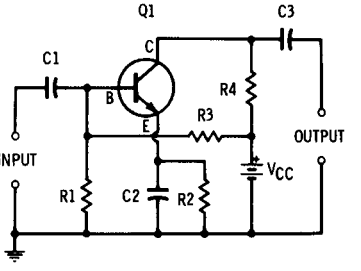
Fig. 1-5 shows circuit symbols for the junction field-effect transistor. Note that the arrowheads of the gate electrodes point toward the channel in N-channel types and away from the channel in P-channel types.

## *1.3 JFET/BIPOLAR/TUBE-CIRCUIT COMPARISON*

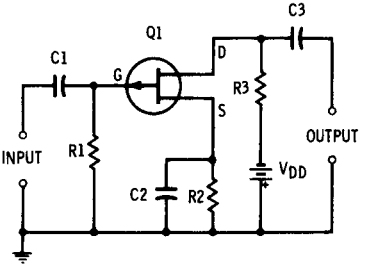
In circuits for performing approximately the same functions, there are many similarities between typical JFET, bipolar transistor, and tube configurations. Figs. 1-6 and 1-7 show, for example, comparisons of "common-cathode" and "cathode-follower" type amplifiers, respectively. In each



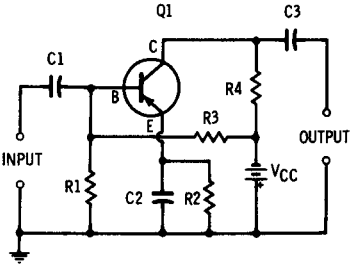

*(A) Common-source N-channel JFET.*



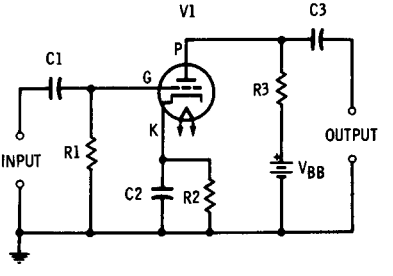

*(B) Common-emitter npn.*




*(C) Common-source P-channel JFET.*




*(D) Common-emitter pnp.*

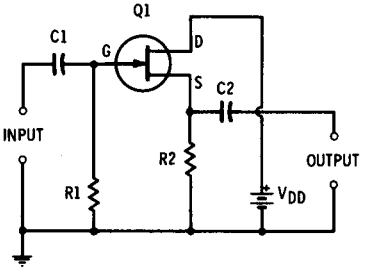



*(E) Common-cathode tube.*

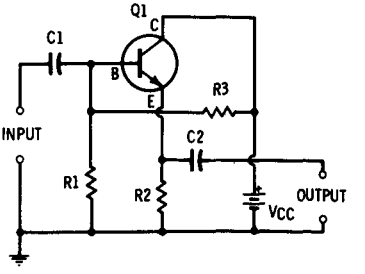
**Fig. 1-6. Comparison: "common-cathode" circuits.**

instance, (A) is the N-channel JFET version, (B) the npn bipolar version, (C) the P-channel JFET version, (D) the pnp bipolar version, and (E) the tube version of the circuit.

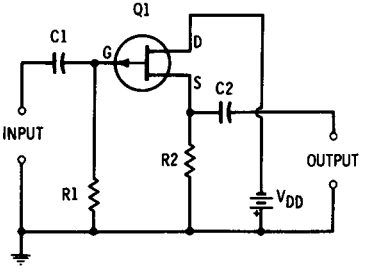
In each application, the control-electrode dc bias is developed as a voltage drop resulting from the flow of output-electrode current carriers through a resistor (R2) connected between the common electrode and ground. This is drain



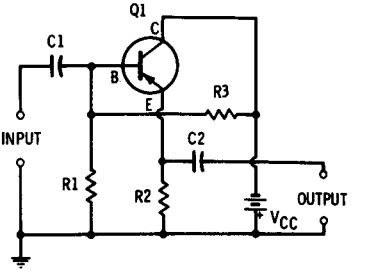

*(A) N-channel JFET source follower.*



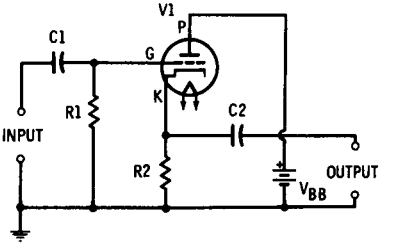

*(B) Npn emitter follower.*




*(C) P-channel JFET source follower.*




*(D) Pnp emitter follower.*




*(E) Tube cathode follower.*

**Fig. 1-7. Comparison: "cathode-follower" circuits.**

current in the JFET's, collector current plus base current (therefore emitter current) in the bipolar transistors, and plate current in the tube. In the bipolar circuits (Figs. 1-6B and D, and Figs. 1-7B and D), additional stabilizing bias is developed by the voltage-divider network R1-R3.

Since bipolar transistors are current-operated devices and the base-bias resistor (R1) is low, their input impedance is low. The JFET and tube, however, are voltage-operated devices that have extremely high input resistance. The grid resistor or gate resistor (R1) therefore largely determines the input impedance of the circuit and may be several megohms, as desired. Because the JFET and tube are high-input-impedance devices, capacitors C1, C2, and C3 in Fig. 1-6A, C, and E, and capacitors C1 and C2 in Fig. 1-7A, C, and E may be low-capacitance units (0.1 $\mu$F, typical), whereas the same capacitors in the equivalent bipolar circuits (Fig. 1-6B and D and Fig. 1-7B and D) must be high-capacitance units (1.0 $\mu$F electrolytic, typical).

Another configuration (not shown in Figs. 1-6 and 1-7) that is sometimes employed is the common-gate FET. This arrangement is analogous to the grounded-grid tube amplifier or the common-base bipolar-transistor amplifier.

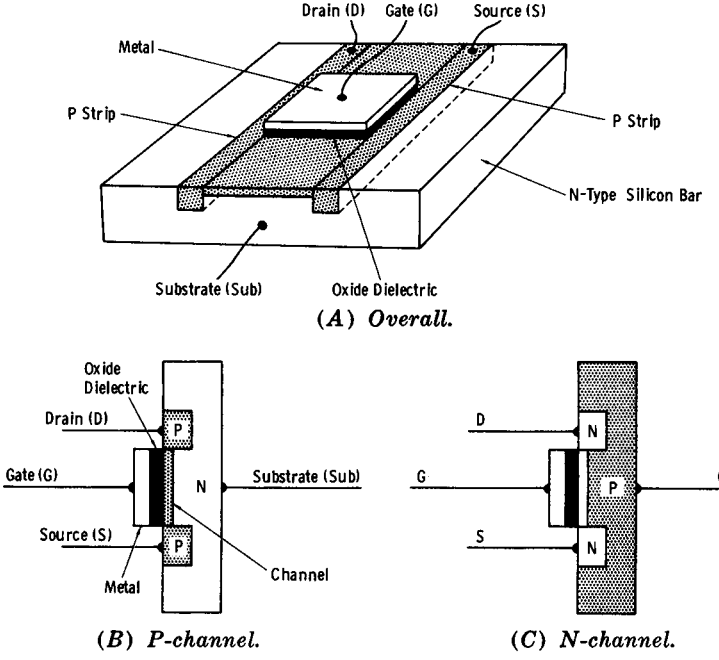
## *1.4 MOSFET: STRUCTURE AND OPERATION*

A particular feature of the metal-oxide semiconductor field-effect transistor (MOSFET) is its extremely high input impedance, which is higher than that of either the JFET or the vacuum tube. The reason for this elevated resistance (impedance) will be clear from the following. Two distinct types of MOSFET's exist: *depletion* and *enhancement*. They differ in both structure and operation, so they will be discussed separately.

### *Depletion Type*

Fig. 1-8A shows the basic structure of the depletion-type MOSFET. As was true in the preceding explanation of the JFET, some manufactured MOSFET's look quite different from this simple illustration, but the latter shows the basic geometry of the unit well enough for purposes of explana-

tion. However, the reader is cautioned that these drawings are not to scale; it is impracticable to show the widths and thicknesses of the MOSFET elements in anywhere near the true relationship they have to each other. Thus, although the text calls certain layers thin, those layers must be shown thick in the drawing in order for the reader to see them.




*(A) Overall.*

*(B) P-channel.* *(C) N-channel.*

**Fig. 1-8. Basic structure of the depletion-type MOSFET.**

Unlike the JFET, the MOSFET does not use a reverse-biased P-N junction as a gate. Instead, it uses a thin metal plate, which is insulated from the rest of the structure by an extremely thin dielectric layer. Both the metal plate and the dielectric layer are deposited films. When a voltage is applied to this metallic gate, the resulting electrostatic field penetrates into the semiconductor material of the MOSFET, and is the mechanism whereby the gate voltage may be used to control the current in the semiconductor.

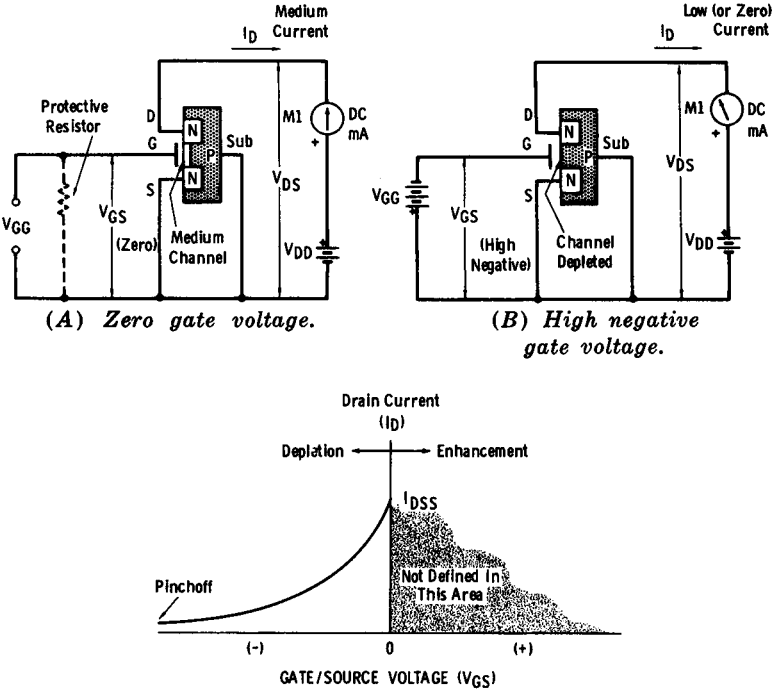
In Fig. 1-8A, the MOSFET has been made from a bar or plate of N-type silicon. This bar forms a base for the other

parts of the device, and is termed the *substrate* (sometimes called the *bulk, base,* or *body*). Two P-type strips (P, P) are diffused a short distance apart into the substrate, and thus form two P-N junctions. One of these junctions acts as the source; the other acts as the drain. A P-type channel is diffused into the substrate between the two P strips. On the surface of the substrate, over the channel, a thin film of silicon-dioxide dielectric is grown. A thin film of metal is then deposited on top of the dielectric film. The metal-film plate is the gate electrode, and is insulated from the substrate by the dielectric film. It is this characteristic arrangement of metal, oxide, and semiconductor that is signified by the name MOSFET. And it is from the fact that the metallic gate is insulated from the rest of the device that this type of transistor is also known as an insulated-gate field-effect transistor (IGFET). While the MOSFET illustrated by Fig. 1-8A is built on an N-type substrate, the opposite type of structure is also possible; that is, two N regions may be diffused into a P-type substrate. The deposition of the metal and oxide films of the gate is the same as before.

A tiny capacitor is formed by the gate. The metal film is one plate of this capacitor, the facing substrate area is the other plate, and the oxide film is the dielectric. The capacitance is small, usually on the order of 1 to 10 picofarads. The dielectric film may be only a few microns thick; as a result, it can be punctured easily (and the MOSFET can be irreparably damaged) by static electric charges that the equivalent capacitor can pick up. For protection of the unit, the manufacturer supplies a MOSFET with its leads short-circuited. The protective shorting device must not be removed until all circuit connections are completed and the MOSFET has been installed. Some MOSFET's have a built-in protective zener diode between gate and source, in order to free the user from these precautions in handling.

Figs. 1-8B and 1-8C show cross sections of the MOSFET. Fig. 1-8B features N-type substrate, and Fig. 1-8C features P-type substrate. In each unit, current carriers will flow from the source, through the channel to the drain. The path between the two P regions in Fig. 1-8B, or between the two N regions in Fig. 1-8C, is the channel, and it is the current

in this channel that is controlled by the electrostatic field from the insulated gate electrode. Leads are connected to the junctions (for source and drain), to the metal film (for gate), and to the substrate, as shown. In some MOSFET's, the substrate is tied to the source internally.




(*A*) *Zero gate voltage.*

(*B*) *High negative gate voltage.*

(*C*) *Response curve.*

**Fig. 1-9. Depletion-type MOSFET.**

It can be seen from Fig. 1-9 that the depletion-type MOSFET may be connected for test and measurement in the same manner as the JFET. That is, the source is the cathode and is the common (or grounded) electrode, the drain is the anode, and the gate is the control electrode. In both of the examples, the drain supply voltage ($V_{DD}$) has the same value and polarity. Operation of the MOSFET may be explained in the following manner: (1) When the gate/source voltage ($V_{GS}$) is zero (Fig. 1-9A), there is a moderate amount of drain current $I_D$, and this is determined

chiefly by the channel resistance and voltage $V_{DS}$. This action corresponds to the point where the response curve crosses the vertical axis in Fig. 1-9C. (2) When the gate voltage is negative (Fig. 1-9B), the drain current is lower than when $V_{GS} = 0$. The reason for this action is the narrowing of the channel due to the negative field from the gate electrode [the negative charge reduces (depletes) the number of charge carriers in the channel between the drain and source in proportion to $V_{GS}$]. This performance corresponds to the curve in Fig. 1-9C. If the negative $V_{GS}$ is made high enough, $I_D$ will be completely cut off (this corresponds to the pinchoff point in Fig. 1-9C). (3) When the gate voltage is positive, the drain current is not defined for depletion-type transistors.

While Fig. 1-9 depicts the operation of an N-channel MOSFET, the same principles apply to the P-channel type, provided the polarities of $V_{GG}$ and $V_{DD}$ and of meter M1 are reversed in each example, and provided the P and N labels are interchanged in the MOSFET symbol.

### *Enhancement Type*

Fig. 1-10A shows the basic structure of the enhancement-type MOSFET. Some manufactured units look quite different from this simple illustration, but the latter shows the basic geometry of the unit well enough for purposes of explanation. However, the reader is cautioned that these drawings are not to scale; it is impractical to show the widths and thicknesses of the MOSFET elements in anywhere near the true relationship they have to each other. Thus, although the text calls certain layers thin, those layers must be shown thick in the drawing in order for the reader to see them.

The enhancement-type MOSFET, like the depletion type, uses a thin metal plate which is insulated from the rest of the structure by an extremely thin dielectric layer. Both the metal plate and the dielectric layer are deposited films. When a voltage is applied to this metallic gate, the resulting electrostatic field penetrates into the semiconductor material of the MOSFET, and is the mechanism whereby the gate voltage may be used to control the current in the semiconductor.

In Fig. 1-10A, the MOSFET has been made from a bar or plate of N-type silicon. This bar, called the substrate, forms a base for the other parts of the device. The P-type strips (P,P) are diffused a short distance apart into the substrate. One of these acts as the source; the other acts as the drain.

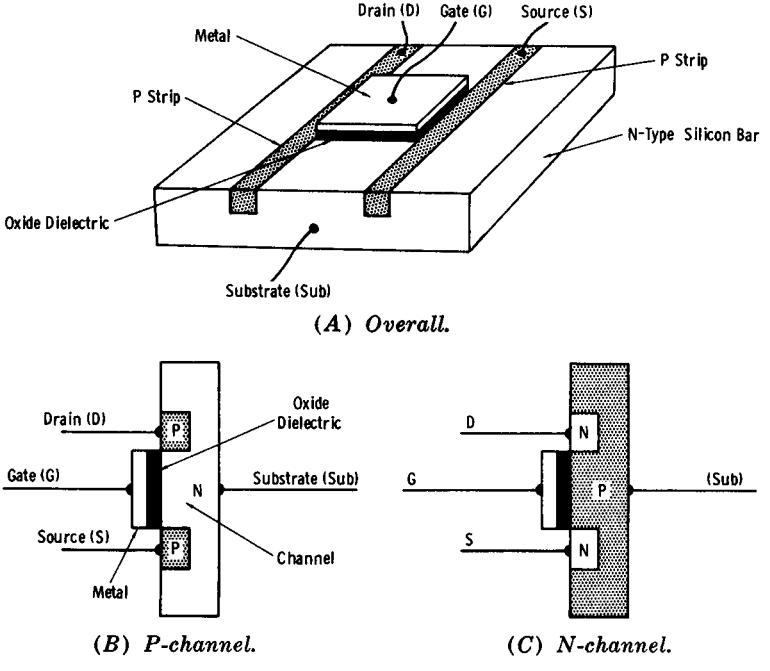


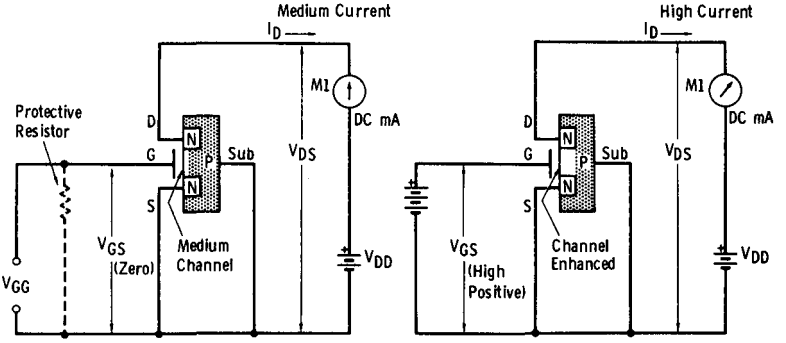

**Fig. 1-10. Basic structure of the enhancement-type MOSFET.**

No channel is diffused into the substrate; this is the distinguishing feature of its construction. While the MOSFET illustrated by Fig. 1-10A is built on an N-type substrate, the opposite type of structure is also possible; that is, two N regions may be diffused into a P-type substrate. The deposition of the metal and oxide films of the gate is the same as before.

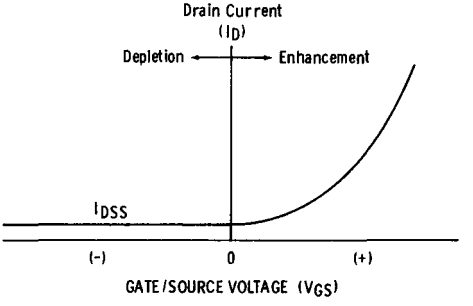
Figs. 1-10B and 1-10C show cross sections of the MOSFET. Fig. 1-10B features an N-type substrate, and Fig. 1-10C features a P-type substrate. In each of these units, current carriers can only flow from the source, through the substrate, to the drain. A portion of the substrate between

the two P regions in Fig. 1-10B or between the two N regions in Fig. 1-10C acts as the channel, and it is the current in this channel that is controlled by the electrostatic field from the insulated gate electrode. Leads are connected to the junctions (for source and drain), to the metal film (for gate), and to the substrate, as shown. In some MOSFET's, the substrate is tied to the source internally.

It can be seen from Fig. 1-11 that the enhancement-type MOSFET may be connected for test and measurement in the same manner as the JFET and the depletion-type MOSFET. That is, the source is the cathode and is the common (or grounded) electrode, the drain is the anode, and the gate is the control electrode. In both of the examples, the drain supply voltage ($V_{DD}$) has the same value and polarity. However, the polarity of the gate-bias voltage




*(A) Zero gate voltage.* *(B) High positive gate voltage.*




*(C) Response curve.*

**Fig. 1-11. Enhancement-type MOSFET.**

($V_{GS}$) is reversed. Operation of the MOSFET may be explained in the following manner: (1) When the gate/source voltage ($V_{GS}$) is zero (Fig. 1-11A), there is only leakage current between the drain and the source. This action corresponds to the point where the response curve crosses the vertical axis in Fig. 1-11C. (2) When the gate voltage is positive (Fig. 1-11B), the drain current is higher than when $V_{GS} = 0$. The reason for this action is the enhancement of the channel due to the positive field from the gate electrode (the positive charge produces an N region in the channel between the N drain and N gate, thus providing an N-N-N conduction path). This performance corresponds to the response curve in Fig. 1-9C. Positive-bias operation is obtained without degrading the high input impedance of the MOSFET. Since the gate electrode is insulated from the substrate by as much as 1 billion megohms, there is no appreciable gate current. This is a definite advantage over both the tube and the bipolar transistor, since the tube will draw grid current, and the corresponding npn bipolar transistor will draw base current when the grid of the tube or base of the transistor is biased positive. The MOSFET has another advantage over the JFET, because driving the junction-type gate of the latter positive in the N-channel JFET, or negative in the P-channel JFET, produces forward current. A MOSFET designed for enhancement-mode operation presents a special case—its channel has extremely high resistance, and therefore is virtually nonexistent until a certain value of positive gate bias is applied. The channel resistance then becomes lower, allowing the conduction of drain current. As the positive gate-bias voltage is increased further, the channel becomes proportionately more conductive (i.e., *enhanced*).

### *Depletion/Enhancement Type*

From the foregoing explanation, one sees two types of construction and operation: (1) a negative-bias type operating in the *depletion* mode, and (2) a positive-bias type operating in the *enhancement* mode. There is a third type operating between these. The *depletion/enhancement* type is so called because when the gate bias is zero, an ac input

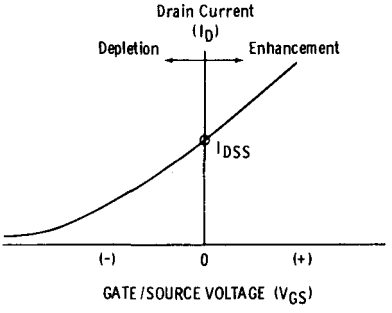


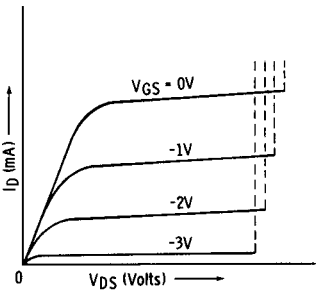

**Fig. 1-12. Depletion/enhancement MOSFET response curves.**

signal will drive the gate alternately negative (into the depletion region of the response curve) and positive (into the enhancement region of the response curve). See Fig. 1-12. By comparison, JFET operation is ordinarily in the depletion mode only, since operation in the enhancement mode will seriously lower JFET input impedance. Some MOSFET's are designed and manufactured expressly for the depletion mode, some for the enhancement mode, and some for the depletion/enhancement mode.

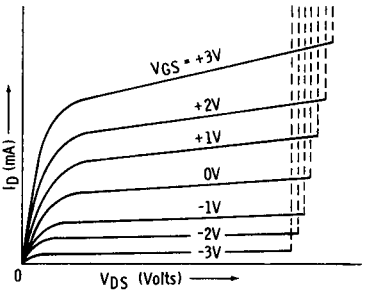
### *Transfer Curves*

The transfer curves in Fig. 1-13 depict the performance of MOSFET's. Note that the slope of the saturation (pinch-off) region of the depletion-mode curves (Fig. 1-13A) is almost horizontal, like those of the JFET (Fig. 1-4), which also is a depletion-mode device. The slope of the same region of the depletion/enhancement-mode curves (Fig. 1-13B) varies from almost horizontal at the maximum negative value of $V_{GS}$ to steep at the maximum positive value of $V_{GS}$. The slope of the same region of the enhancement-mode curves (Fig. 1-13C) varies from almost horizontal at the lowest positive value of $V_{GS}$ to quite steep at the highest positive value of $V_{GS}$. The depletion-mode curves resemble comparable pentode-tube curves, whereas the enhancement-mode curves resemble comparable bipolar-transistor curves.

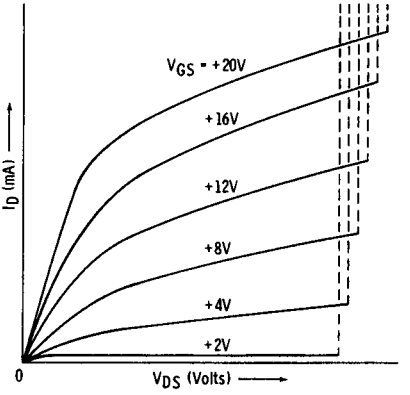
Fig. 1-14 shows circuit symbols for the metal-oxide semiconductor field-effect transistors (MOSFET's). Note that in Fig. 1-14, drawings (c) and (d), the substrate is connected internally to the source. In all other instances, an external connection to the substrate is provided.




*(A) Depletion mode.*

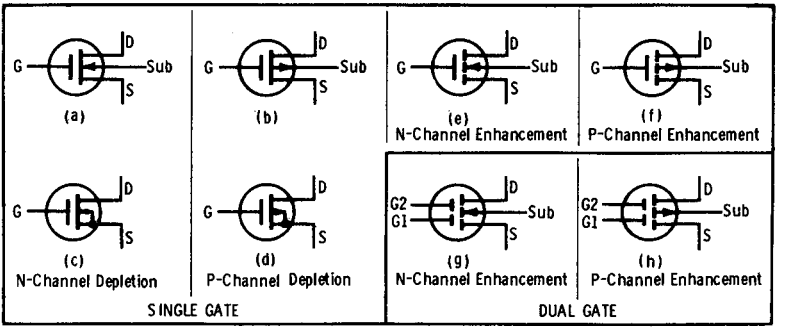



*(B) Depletion/enhancement mode.*




*(C) Enhancement mode.*

**Fig. 1-13. Typical MOSFET performance curves.**

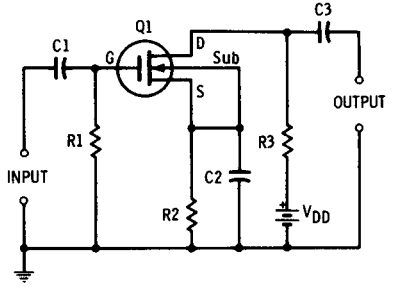



*(A) Single gate.* *(B) Dual gate.*

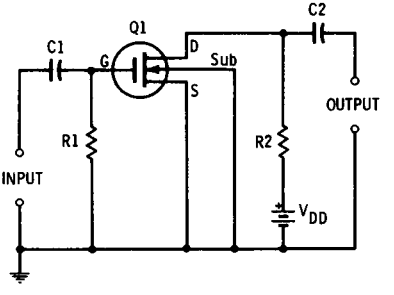
**Fig. 1-14. Circuit symbols for the MOSFET.**

## *1.5 MOSFET IN TYPICAL CIRCUITS*

Fig. 1-15 shows three versions of the common-source MOSFET amplifier circuit, which is comparable to the common-cathode tube, common-emitter bipolar transistor, and common-source FET circuits (see Fig. 1-6 for comparison). In Fig. 1-15A, automatic negative dc gate-bias voltage




*(A) Negative gate bias (depletion mode).*




*(B) Zero gate bias (depletion/enhancement mode).*

*(C) Positive gate bias (enhancement mode).*

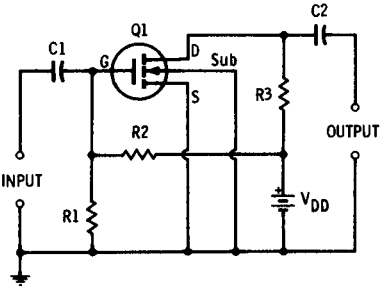



**Fig. 1-15. MOSFET common-source circuits.**

is obtained from the voltage drop across R2 produced by the source current. The MOSFET here consequently operates at negative $V_{GS}$; i.e., in the depletion mode. In Fig. 1-15B, the source is grounded directly and the dc gate-bias voltage is zero. The input ac signal therefore can swing the gate positive on one half-cycle and negative on the other; the MOSFET here accordingly operates in the depletion/enhancement mode. In Fig. 1-15C, positive dc gate-bias volt-

age is obtained from the drain power supply ($V_{DD}$) through the R1-R2 voltage divider. The MOSFET here accordingly operates in the enhancement mode. Each MOSFET is constructed to operate in one of these three modes. The reader who is familiar with tube and transistor circuits will recognize that there are other ways of obtaining negative and positive gate-bias voltage. For example, a fixed gate-voltage source ($V_{GG}$) might be used. The circuits shown in Figs. 1-15A, B, and C, however, offer single-battery simplicity.

Fig. 1-16 shows a simple source-follower circuit, which is comparable to the cathode-follower tube, emitter-follower bipolar transistor, and source-follower JFET circuits (see Fig. 1-7 for comparison).

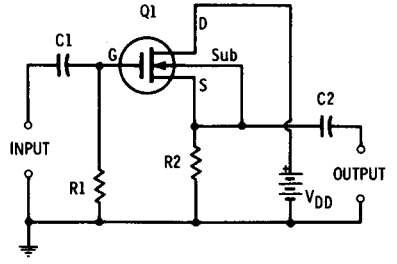



**Fig. 1-16. MOSFET source-follower circuit.**

Another configuration (not shown in Figs. 1-15 and 1-16) that may be used is the common-gate MOSFET. This arrangement is analogous to the grounded-grid tube amplifier and the common-base bipolar transistor amplifier.

In all of the circuits in Figs. 1-15 and 1-16, N-channel MOSFET's are shown. P-channel units may also be employed, provided the battery ($V_{DD}$) is reversed in each instance. It should also be clear how other single-gate MOSFET's from the group shown in Fig. 1-14 might be employed in these circuits.

The MOSFET in all of its applications exhibits the special feature of extremely high input impedance, and this property reduces practically to zero any loading that the MOSFET imposes upon a driving source. In the circuits in Figs. 1-15 and 1-16, therefore, the input impedance is determined principally by the resistance of gate resistor R1, which may be several megohms, as required.

## *1.6 FET RATINGS*

Obviously, a large number of electrical characteristics may be used to specify a FET and describe its operation, since different models (like different tubes and bipolar transistors) often have unique properties. It is impracticable and far from mandatory in this introductory treatment to list all of these here. The list that follows is thought to explain the core of ratings applying to most FET's.

Because the FET, like the tube, is basically an electrostatic-control device, it makes possible the use of a small input voltage to control a large output current (hence, amplification). From this, it follows that the most important FET characteristic perhaps is *transconductance,* as transconductance expresses the extent to which this control is achieved. Transconductance ($g_{fs}$) is equal to the change in drain current ($dI_D$) divided by the change in gate voltage ($dV_G$) and the formula is often written as follows:

$$g_{fs} = 1000\,(dI_D/dV_G)$$

where,

$g_{fs}$ is the transconductance in micromhos,
$I_D$ is the drain current in dc mA,
$V_G$ is the gate/source voltage in dc volts.

These and other characteristics follow. All of these figures depend on the FET make and model.

***Common-Source Forward Transconductance*** **($g_{fs}$)**

The ratio of $dI_D$ to $dV_{GS}$. Similar to tube transconductance ($G_m$). Given for a specified $V_{DS}$, $V_{GS}$, and f = 1 kHz. Range: 35 to 50,000 $\mu$mho.

***Common-Source Output Conductance, Input Shorted*** **($g_{oss}$)**

Reciprocal of drain/source output resistance. Given for specified $V_{DS}$, $V_{GS}$, and f = 1 kHz. Range: 1 to 600 $\mu$mho.

***Common-Source Input Capacitance, Output Shorted*** **($C_{iss}$)**

Capacitance between gate and source. Given for specified $V_{DS}$, $V_{GS}$, and f = 1 kHz. Range: 2 to 65 pF.

### *Common-Source Reverse Transfer Capacitance* ($C_{rss}$)

Given for specified $V_{DS}$, $V_{GS}$, and f = 1 kHz. Range: 0.02 to 6 pF.

### *Drain Current at Zero Gate Voltage* ($I_{DSS}$)

The current in the drain/source circuit (i.e., through the channel) when $V_{GS} = 0$. Given for specified $V_{DS}$. Ranges: 0.1 to 10 mA at $V_{DS} = 5$ V, 5 to 25 mA at $V_{DS} = 8$ V, 0.03 to 6.0 mA at $V_{DS} = 10$ V, 0.2 to 20 mA at $V_{DS} = 15$ V, 0.4 to 7.5 mA at $V_{DS} = 20$ V, 80 to 250 mA at $V_{DS} = 35$ V.

### *Drain Cutoff Current* ($I_D$ OFF)

Leakage current through the channel when $V_{GS}$ has been adjusted for cutoff of output. Given for specified $V_{DS}$ and $V_{GS}$. Range (for $V_{DS} = 15$ V) : 0.05 nA at $V_{GS} = 5$ V, to 0.07 nA at $V_{GS} = 10$ V.

### *Gate/Drain Voltage* ($V_{GD}$)

Also called drain/gate voltage. The maximum voltage that may appear between the gate and drain electrodes. Range: 20 to 50 V at 25°C.

### *Gate Reverse Current* ($I_{GSS}$)

Also called gate leakage current. The reverse current in the gate/source circuit. Given for $V_{DS} = 0$ and a specified value of $V_{GS}$. Range: 2 nA at $V_{GS} = 15$ V, 10 pA to 0.5 nA at $V_{GS} = 20$ V, 0.1 to 30 nA at $V_{GS} = 30$ V.

### *Gate/Source Breakdown Voltage* ($BV_{GSS}$)

The voltage at which the gate junction of a JFET will enter avalanche. Given for $I_G = 1$ $\mu$A and $V_{DS} = 0$. Range: 20 to 50 V at 25°C.

### *Gate/Source Pinchoff Voltage* ($V_P$)

The gate-to-source voltage at which the field just closes the conduction channel. Given for $I_D = 1$ nA, 10 nA, or 1$\mu$A, and for a specified value of $V_{DS}$ (e.g., 5 to 15 V). Range: 0.6 to 50 V.

*Gate/Source Voltage* ($V_{GS}$)

Also called source/gate voltage. The maximum voltage that may appear between the gate and source electrodes. Range: 20 V to 50 V at 25°C.

*Noise Figure* (NF)

Internal noise generated by the FET. Given for $V_{GS} = 0$, and at a specified $V_{DS}$ (e.g., 15 V) and frequency (e.g., 1 kHz, 200-Hz bandwidth). Range: 0.5 to 3 dB for JFET's. Somewhat higher in MOSFET's.

*Total Device Dissipation* (P)

Maximum power that can be safely dissipated by the FET structure. Range: 200 mW to 0.8 W in free air at 25°C.

*Common-Source Parallel Input Resistance* ($r_{GS}$)

The resistance between the gate and source electrodes. Given for a specified value of drain/source voltage and drain current (e.g., $V_{DS} = 10$ V, $I_D = 0.15$ mA). Typical values: $10^9$ ohms for JFET's, $10^{15}$ ohms for MOSFET's.

## *1.7 FET PACKAGING AND APPLICATION*

Like bipolar transistors, FET's are commercially available in a variety of packages ranging from plastic encapsulation to small metal cans. Various basing schemes are employed, so the manufacturer's literature must be consulted for identification of terminals. In some models, one of the electrodes (usually the gate) is tied internally to the metal can, and these FET's must be installed with care to prevent shorts, grounds, or stray pickup. In some models, a separate pigtail is tied to the can.

The family of field-effect devices has now grown to impressive size. Depending on the FET model, field-effect circuits can be employed at frequencies from dc to several hundred megahertz (the Type 40673 MOSFET, for example, is rated to 400 MHz). This wide operating range allows the FET to be used in all types of communications, instrumentation, and control equipment. The designer selects a

FET to suit his purpose much as he would choose a tube or bipolar transistor. Matched pairs of FET's are available for balanced circuit operation, and matched N-channel and P-channel units are available for complementary symmetry operation.

At this writing, the FET is essentially a small-signal device; its power output is limited to the milliwatt region. However, integrated circuits are appearing in which FET's are used in the input circuit to provide high input impedance, and the power output of some of these integrated circuits can be expected to be usefully higher than that of a FET alone.

CHAPTER 2

# Getting Acquainted With the FET

One way to get acquainted with the field-effect transistor is to experiment with it on a breadboard. In this way, using a minimum of parts and the few common test instruments found on any electronic hobbyist's equipment shelf, the experimenter can observe firsthand how the FET works. He can also check performance against the FET manufacturer's data.

This chapter describes, step-by-step, a number of simple tests for the breadboard checking of FET's. The procedures apply in general to any field-effect transistor, provided care is taken to hold voltages, currents, resistor values, and instrument ranges within the limits dictated by a particular type. Where a particular type FET is shown, it is the type that was used in the author's test setup, and the accompanying test data is given for that individual transistor. However, other comparable types will operate in the circuit and will yield similar data.

Before the reader who has had no experience with FET's undertakes any of the tests, we recommend a careful study

of Section 2.1. This will reduce the chance of damaging the FET's or obtaining misleading data.

## *2.1 HINTS AND PRECAUTIONS*

All of the correct procedures for handling bipolar transistors, with which we assume the reader is already familiar, are also valid for the FET. Nevertheless, some of these are repeated below or paraded in new dress simply because they need re-emphasis here. Certain precautions, however, apply especially to the FET; the MOSFET in particular requires special handling. The reader should study all of the hints and precautions listed below, since the FET is more easily damaged than is the bipolar transistor, and is more susceptible to improper operation.

### *DC Supplies*

All dc supplies must be clean; i.e., their output must contain the minimum of ripple or noise. Ripple voltage and noise voltage can cause all sorts of mischief in test circuits. The ripple or noise component of a dc voltage used to bias a FET gate, for example, looks like an ac input signal (which, indeed, it is) and gets amplified unintentionally to reappear as a much bigger signal in the FET output. New batteries make the best dc supplies for experimental testing. But many transistor experimenters will want to use ac-operated supplies that they already own. This is permissible if the ripple or noise voltage is accounted for in the interpretation of test results, or if extra filters are used with the supply.

### *Electrode Voltages and Currents*

Hold all electrode dc voltages and currents within manufacturers' ratings. That is, do not exceed the maximum specified dc or peak-to-peak values for drain/source voltage, gate/source voltage, gate/substrate voltage, drain/gate voltage, drain/substrate voltage, and drain current.

It is always good practice to have voltages smoothly adjustable so that they can be set to the exact desired value. This calls for continuously variable supplies. When bat-

teries are used, a simple potentiometer (the wirewound volume-control type is permissible) may be connected across the battery to provide an adjustable voltage as shown in the "bias-box" unit in Fig. 2-1. A limiting resistor (R1) is connected in series with the battery (B1) and potentiometer (R2) to hold the output voltage to a safe maximum. (For example, if B1 = 22.5 V and the output voltage to be applied to a specific FET must never exceed 12 V, the ratio of R1 to R2 must be chosen such that the maximum output of the potentiometer is 12 volts.) For a given maximum

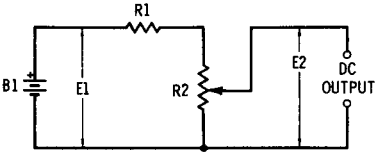



**Fig. 2-1. "Bias-box" type dc supply.**

potentiometer resistance (R2), required maximum output voltage (E2), and available battery voltage (E1), the required value of the limiting resistor (R1) may be calculated:

$$R1 = [(E1/E2) - 1]R2 \qquad (2\text{-}1)$$

Thus, if a 10,000-ohm potentiometer and 22.5-V battery are available, and a maximum safe output voltage of 12 V is required, $R1 = [(22.5/12) - 1]10{,}000 = (1.875 - 1)10{,}000 = (0.875)10{,}000 = 8750$ ohms. If a fixed resistor having the exact calculated value of R1 is not available, a rheostat can be used in its place. The rheostat can be preset to the required resistance with the aid of an ohmmeter or output voltmeter.

In the schematics in this chapter, variable batteries are shown for simplicity, but the dc bias voltages may be supplied, as explained earlier, either by ac-operated supplies or by bias-box supplies.

### *AC Signal Voltages*

Ac signal voltages should be kept as low as practicable. The lowest value that will afford a reliable test should always be used. A good rule of thumb is to restrict the peak value of the signal voltage to $\frac{1}{10}$ or less of the dc bias voltage at

the FET electrode to which the signal is applied. In any event, respect the maximum values specified by the FET manufacturer. When a FET is operated close to the nonlinear portion of its response curve, the signal voltage often must be reduced even lower than the $\frac{1}{10}$ figure would require, to prevent driving into the distortion region.

For the simple tests described in this chapter, ac signal voltages may be supplied by oscillators or signal generators. Service-type instruments will be entirely adequate. For high-precision measurements, laboratory-type instruments are required. An audio test oscillator should have low harmonic distortion, but this is no problem, since even service-type instruments in this category show well under 1 percent total distortion.

### *Current and Voltage Meters*

The milliampere and microampere ranges of a service-type multimeter are satisfactory for dc current measurements. Only in the measurement of drain cutoff current (see Section 2.4) is an extremely sensitive meter, a *picoammeter,* required. But because such tiny currents do not even deflect the lowest-range service-type microammeter, most practical experimenters will safely call these currents zero. Some vacuum-tube voltmeters and equivalent transistorized voltmeters with current ranges are not recommended here because their insertion resistance is too high. The insertion resistance should be as low as possible, in order to create the least upset of a circuit into which the meter is connected. Whereas the insertion resistance of a nonelectronic multimeter, such as the Simpson Model 260, on its milliampere ranges may be on the order of 25 ohms, that of a VTVM adapted for current may be 1000 ohms or higher.

The sensitivity of the ac voltage ranges of most nonelectronic multimeters runs around 1000 to 5000 ohms per volt, and this is too low in some instances to prevent overloading of high-impedance circuits. Also, the frequency response of such ac meters sometimes falls off rapidly within and beyond the top of the audio spectrum. For low-level ac signal-voltage measurements, therefore, an ac vacuum-tube voltmeter/millivoltmeter is recommended. (Many techni-

cians own such a meter, since it has long been available in kit form.) This type of voltmeter usually has a constant input resistance of 10 megohms on all ranges. The ac ranges of a regular VTVM or transistorized voltmeter may be used if full-scale deflections lower than 1.5 volts are of no interest. However, the user should be aware that the input resistance of such instruments is lower on the ac ranges than the traditional 11 megohms of the dc ranges. Some oscilloscopes are sensitive enough for ac millivolt measurements, but some of these instruments have an input resistance of only 1 megohm.

### *Oscilloscope*

An oscilloscope is invaluable for showing waveform simultaneously with amplitude of a signal. Thus, signal voltages (and currents) may be measured, distortion estimated, noise level observed, and signal clipping noted. However, as in the case of the regular VTVM on its ac ranges, the input impedance of a service-type oscilloscope is sometimes low enough that its loading effect must be considered.

### *Special Instrumentation*

The sophisticated experimenter who wishes to look critically into FET performance may require other instruments not shown in the simple test procedures in this chapter. Such instruments include a harmonic distortion meter, intermodulation meter, capacitance meter, temperature-test system, noise meter, frequency meter, and phase meter.

### *General Handling and Testing of FET's*

While transistors, like other solid-state components, are relatively rugged mechanically and electrically, they can be damaged through mishandling and careless test procedures. The following is a list of some do's and don't's in this regard.

(1) Avoid needlessly dropping a FET or otherwise subjecting it to severe mechanical shock.
(2) Do not operate a FET near hot components. If a test requires operating the FET at high tempera-

ture, derate according to the manufacturer's instructions.

(3) Avoid exceeding maximum current and voltage levels even temporarily.

(4) Follow standard transistor procedure when installing a FET. Use a socket or good clip leads. If you solder the FET into a circuit, grip each lead as you solder it, with long-nose pliers, and continue to hold the lead until the soldered joint and lead have completely cooled.

(5) Install the FET last in the circuit. Complete all other wiring beforehand. A safe sequence is to complete the circuit wiring; check the wiring; attach the dc supplies, signal source, and output device, but with all dc and signal voltages switched off; carefully install the FET; switch-on the dc supplies; and switch-on the signal source. When disassembling a test setup, the following procedure is safe: Switch-off the signal voltages; switch-off the dc voltages; disconnect the signal source; disconnect the dc supplies; and remove the FET.

(6) A MOSFET requires special handling. Do not remove its protective short-circuiting device until all the MOSFET leads have been connected. If you solder the MOSFET into the circuit, observe the precautions given in (4) and (5); and, in addition, ground your soldering iron to a good earth connection, such as a cold water pipe. It is a good idea also to ground yourself. Even when grounded, a soldering *gun* is tricky to use since it may induce a voltage kick in the MOSFET; it is better to use a pencil-type soldering iron.

(7) Never allow the gate of a MOSFET to float. It can easily pick up a static charge that will puncture its dielectric film and permanently damage the MOSFET. Connect a resistor between gate and ground (even as much as several megohms, if necessary, to simulate an open circuit).

(8) All FET's, unlike bipolar transistors, have a high input impedance, and this makes them susceptible

(as vacuum tubes are) to stray pickup. This means that you must keep any possible signal-emitting component away from the FET. You must also keep your body away from an operating FET—FET's are quite sensitive to body capacitance. To prevent body capacitance disturbances when making voltage measurements, use a shielded probe, and even then keep your fingers well back of the probe tip. Keep all FET-circuit input-signal leads as short as practicable.

(9) When a MOSFET has an external substrate terminal, connect this terminal to the source terminal, unless otherwise instructed.

(10) Remember that the electrical characteristics of FET's spread over a significant range (note that the manufacturer's data sheet gives minimum, maximum, and typical values), and this variation can cause test results to differ from those given by an author or designer. If you desire to mass produce a circuit, or to offer it for duplication, use typical FET characteristics in your design, and even then make your guarantees well inside the performance limits you observe in your tests of the circuit.

(11) Observe the correct polarity of each electrode voltage.

## *2.2 CHECKING DRAIN CHARACTERISTIC*

The test setup shown in Fig. 2-2 permits the experimenter to observe how dc drain current ($I_D$) varies with dc drain/source voltage ($V_{DS}$) for various values of gate/source dc voltage ($V_{GS}$). The procedure is to hold $V_{GS}$ at a constant value while $V_{DS}$ is varied over an appreciable range, and to note corresponding values of $I_D$.

A dc VTVM or transistorized voltmeter (M1) is used to measure both $V_{GS}$ and $V_{DS}$, and must have an internal polarity shifting switch; otherwise, its input leads must be interchanged when moving from the negative gate to positive drain, and vice versa. A single-pole double-throw

changeover switch (S1) allows this meter to read gate/source voltage in position A and drain/source voltage in position B. The dc milliammeter (M2) must read accurately the range of $I_D$ values to be expected from the FET manu-

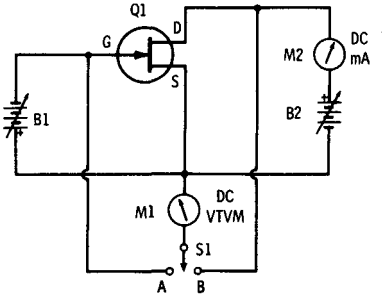



**Fig. 2-2. General-purpose test setup.**

facturer's data; usually, 0-10 and 0-20 mA ranges will suffice. Similarly, the output of the variable dc supplies (B1 and B2) must cover the range of $V_{GS}$ and $V_{DS}$ values, respectively, indicated by the FET manufacturer's data.

(1) Set polarity of meter M1 to negative.
(2) Throw switch S1 to A.
(3) Set B1 to desired gate/source voltage, starting at zero. The value is indicated by M1.
(4) Throw S1 to B.
(5) Set polarity of meter M1 to positive.
(6) Set B2 to zero, indicated by M1. Record.
(7) Read corresponding drain current, indicated by M2.
(8) Set B2 to next higher drain/source voltage. Record.
(9) Read corresponding drain current. Record.
(10) Similarly, increase drain/source voltage in small steps, noting drain current at each step. The results when plotted give a single curve similar to Fig. 1-4B, Chapter 1. This curve corresponds to zero gate/source voltage.
(11) After a complete set of measurements has been made (Steps 1 to 10), change the gate/source voltage to the first desired negative value and repeat the whole series of steps, to obtain a second $V_{DS}/I_D$

curve. Then, set the gate/source voltage to a second, higher negative value and repeat the steps. Repeat this procedure at a full set of gate/source voltage values. The final result will be a family of curves similar to Fig. 1-4A, Chapter 1. If operation at positive gate/source voltage also is to be observed, reverse B1 and repeat the measurements of $I_D$ vs $V_{DS}$.

The test circuit and dc polarities in Fig. 2-2 are given for an N-channel JFET. For a P-channel JFET, reverse B1, B2, M1, and M2. If a MOSFET is under test, the polarities shown here are correct for an N-channel MOSFET in the depletion mode, and the corresponding curves are shown in Fig. 1-13A. For a P-channel MOSFET in the depletion mode, reverse the polarity of B1, B2, M1, and M2. For a MOSFET in the enhancement mode, the gate/source voltage must be positive for N-channel and negative for P-channel units, and the corresponding curves are shown in Fig. 1-13C. For a MOSFET in the depletion/enhancement mode, the gate/source voltage must include both positive and negative values, and the corresponding curves are shown in Fig. 1-13B.

## *2.3 CHECKING GATE/SOURCE PINCHOFF VOLTAGE*

Use the same test setup shown in Fig. 2-2, except substitute a low-range dc microammeter (one capable of reading 1 $\mu$A) for milliammeter M2. This test shows the gate/source voltage value required to cut off the drain current. Actually, the drain current is never completely cut off, but reaches an extremely low value. A value (such as 1 $\mu$A) is specified by the FET manufacturer, together with the test value of drain/source voltage (e.g., 10 V).

(1) With meter M1, set B1 to zero and B2 to 10 V (or to any other value of drain/source voltage specified by the FET manufacturer).
(2) Set S1 to A.

(3) Increase voltage of B1, noting that drain current, indicated by meter M2, decreases. Stop when M2 reads 1 $\mu$A.
(4) At this point, read the corresponding gate/source voltage from meter M1. This is the desired gate/source pinchoff voltage.

The test circuit and dc polarities in Fig. 2-2 are given for an N-channel JFET. For a P-channel JFET, reverse B1, B2, M1, and M2. If a depletion-type or depletion/enhancement-type MOSFET is under test, the polarities shown here are correct for an N-channel MOSFET; for a P-channel MOSFET, reverse the polarity of B1, B2, M1, and M2. For enhancement-type MOSFET's, the polarity of B1 will need to be reversed.

## *2.4 CHECKING DRAIN CUTOFF CURRENT*

The characteristic checked here is the extremely low value of drain current at a specified value of drain/source voltage when the gate/source voltage has been set at a relatively high value. It can be measured only with a very sensitive current instrument (substituted for milliammeter M2 in Fig. 2-2), since it is usually in picoamperes (pA). The test conditions are specified by the FET manufacturer (e.g., $V_{DS} = 5$ V, $V_{GS} = 10$ V).

Use the test setup shown in Fig. 2-2, except replace milliammeter M2 with a dc picoammeter.

(1) With meter M1, set B2 (i.e., $V_{DS}$) to 5 V and B1 (i.e., $V_{GS}$) to 10 V (or to any other value of drain/source voltage and gate/source voltage specified by the FET manufacturer).
(2) Read corresponding drain cutoff current from meter M2.

The test circuit and dc polarities in Fig. 2-2 are correct for N-channel JFET's and MOSFET's. For P-channel JFET's and MOSFET's, reverse B1, B2, M1, and M2. If an enhancement-type MOSFET is under test, reverse the polarity of B1.

## 2.5 *CHECKING DRAIN CURRENT AT ZERO GATE VOLTAGE*

The drain current of interest here is that static value present when the drain/source voltage is a value (such as 10 V) specified by the FET manufacturer, and the gate/source voltage is zero.

Fig. 2-3 shows the test setup. In this arrangement, resistor R1 (1 megohm or higher) prevents the gate from floating. This resistor may be omitted in some JFET tests, but it is mandatory, to prevent damage, in MOSFET tests.

(1) Set B1 for 10 V (or to any other value of drain/source voltage specified by the FET manufacturer), as indicated by meter M1.
(2) Read the corresponding drain current from meter M2.

The test circuit and dc polarities in Fig. 2-3 are correct for N-channel JFET's and MOSFET's. For P-channel JFET's and MOSFET's, reverse B1, M1, and M2.

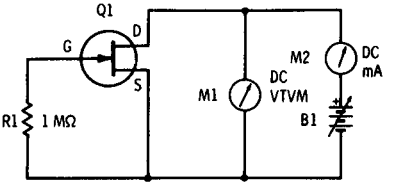



**Fig. 2-3. Setup for checking drain current.**

## 2.6 *CHECKING TRANSCONDUCTANCE*

Unless the experimenter has access to a dynamometer-type ac milliammeter, transformer-coupled ac milliammeter, or transconductance meter (all of which are expensive and uncommon even in some engineering laboratories), he will be unable to measure FET transconductance under ac conditions. A reasonably adequate experimental test may be made, however, with a dc circuit in which the gate/source voltage is varied in two small steps about a mean value, to simulate the peak states of an ac test signal. The corresponding drain-current shift is noted, and from the voltage and current

Fig. 2-4. While the dynamic test is preferable for demonstrating the control properties of the FET, the simpler test is useful in emergencies and requires a minimum of equipment. In this test, the FET gate/source voltage initially is zero. It is then shifted by a known amount (say, 1.5 V). The corresponding drain-current change is noted, and the transconductance is calculated from the voltage and current increments.

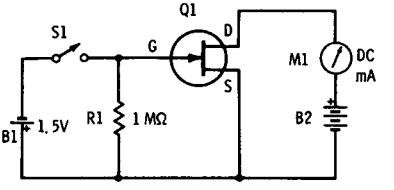



**Fig. 2-4. Setup for static test of transconductance.**

The voltage of battery B2 may be any value that will operate the FET within the saturation region of its drain voltage/drain current curve, usually between 6 and 10 volts. Dc milliammeter M1 should have a 0-10 or 0-20 mA range. The voltage of battery B1 must be known with reasonable accuracy.

(1) Record the voltage of battery B1 as V.
(2) With switch S1 (which may be a single-pole single-throw normally open pushbutton) open, note the reading of meter M1. Record as $I_1$.
(3) Close switch S1, noting that the drain current, indicated by M1, decreases. Record this new reading as $I_2$.
(4) Calculate the transconductance:

$$g_{fs} = 1000\ (I_1 - I_2)/V \qquad (2\text{-}3)$$

where,
$g_{fs}$ is in $\mu$mho,
$I_1$ and $I_2$ are in mA,
V is in volts.

If B1 = 1.5 V, this simplifies to:

$$g_{fs} = 1000\ (I_1 - I_2)/1.5 \qquad (2\text{-}4)$$

which further simplifies to:

$$g_{fs} = 667\ (I_1 - I_2) \qquad (2\text{-}5)$$

The arrangement in Fig. 2-4 shows an N-channel JFET; however, the battery and meter polarities are correct also for an N-channel depletion- or depletion/enhancement-type MOSFET. For a P-channel JFET or a P-channel depletion-type MOSFET, reverse B1, B2, and M1.

## 2.8 *CHECKING VOLTAGE GAIN*

The performance of the FET in a simple amplifier circuit will interest the newcomer to FET circuits. Fig. 2-5 shows a single-stage, common-source audio amplifier with audio

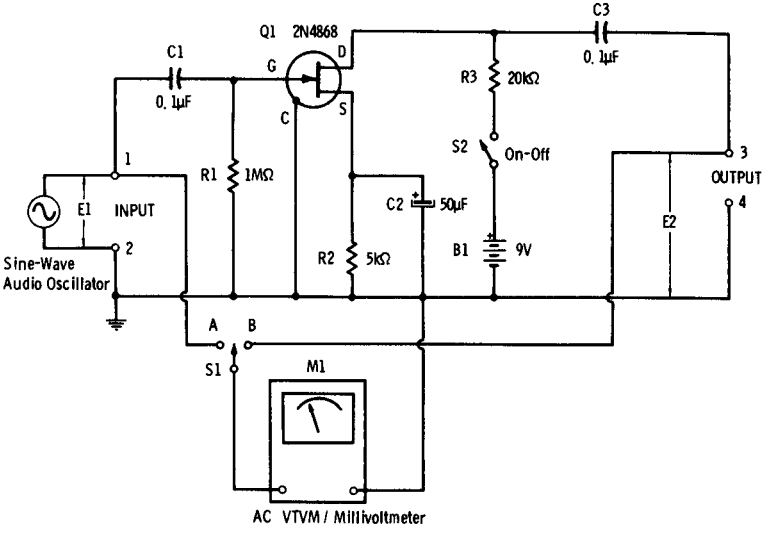



**Fig. 2-5. Setup for checking voltage gain.**

oscillator and ac vacuum-tube voltmeter/millivoltmeter connected for gain measurements. The 2N4868 JFET shown here is metal encased, and a separate terminal (C) is provided for grounding the case.

(1) Open switch S2.
(2) Throw switch S1 to position A.
(3) Set output control in oscillator to zero.
(4) Set oscillator frequency to 1000 Hz.

(5) Set M1 to its 100-mV range.
(6) Close switch S2.
(7) Slowly increase oscillator output until M1 reads 20 mV. Record this value as $E_1$.
(8) Switch M1 to its 1-V range.
(9) Throw switch S1 to position B.
(10) Observe new reading of M1. Record this value as $E_2$.
(11) Calculate the open-circuit voltage gain:

$$A = E_2/E_1 \qquad (2\text{-}6)$$

where,

$E_1$ and $E_2$ are both in V or mV.

The 2N4868 in this experimental setup drew a drain current of 0.3 mA and provided a voltage gain of 20 at 1000 Hz. However, individual FET's of the same type may show more or less gain, depending on their position in the manufacturer's tolerance spread. The input-signal amplitude ($E_1$) could be increased to 50 mV rms, to give a corresponding output-signal amplitude ($E_2$) of 1 V rms before peak clipping of the output signal was observed with an oscilloscope connected to output terminals 3 and 4.

The experimenter should vary R2 and R3, noting the corresponding voltage gain and also the maximum input-signal voltage that may be applied before output-peak clipping.

A similar circuit may be set up for checking other types of FET's. Battery polarity is correct in Fig. 2-5 for the N-channel JFET shown, and also for N-channel depletion-type MOSFET's. For P-channel JFET's and depletion-type MOSFET's, reverse battery B1. For FET's other than the 2N4868, resistances R2 and R3 must be calculated or worked out by cut-and-try methods. The gate of the enhancement-type MOSFET cannot be biased by the source resistor (R2) method at all, but must receive positive bias from a voltage divider (see Fig. 1-15C, Chapter 1). A zero-bias (depletion/enhancement-type) MOSFET would have its source grounded (see Fig. 1-15B, Chapter 1), and the ac input signal would drive the gate alternately positive and negative.

## 2.9 *ADDITIONAL TESTS OF THE AMPLIFIER*

If the reader desires, and has the necessary test gear, he can check the simple amplifier (Fig. 2-5) in the conventional manner for frequency response, harmonic distortion, output impedance, phase shift, and noise level.

## 2.10 *CHECKING OSCILLATOR ACTION*

The readiness of the FET to oscillate may be checked with any simple oscillator circuit. Fig. 2-6 shows an untuned crystal oscillator (FET version of the Pierce circuit) that can be used for this purpose. Any quartz crystal (XTAL in Fig. 2-6) will do; remember, however, that a harmonic-type crystal oscillates in this circuit at its *fundamental* frequency, not at the labeled frequency, which is a harmonic. The 2N3823 FET shown here is a metal-encased unit, and has a separate terminal (C) for grounding the case. In the author's test setup, drain current was 1.8 mA for a B1 voltage of 6 V.

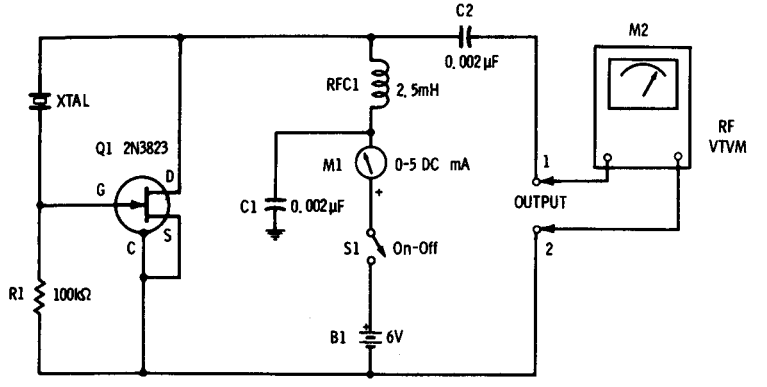



**Fig. 2-6. Setup for checking oscillator action.**

1. Set up circuit, as shown in Fig. 2-6.
2. Connect rf voltmeter (vacuum-tube or equivalent transistorized version) to output terminals 1 and 2.
3. Close switch S1, noting deflection of dc milliammeter M1 and rf voltmeter M2. The author's circuit delivered

rf output of 5 V peak to the voltmeter, with a 7000-kHz crystal.

4. The output signal may be transmitted to a receiver or rf frequency meter for monitoring or frequency checking, by means of an antenna connected to output terminal 1. This antenna can consist of 1 or 2 feet of stiff wire or rod vertically mounted, or a few feet of insulated, flexible wire strung either horizontally or vertically. Keep all antennas as short as possible, however, since the oscillator makes a fair transmitter capable of radio interference.

## *2.11 FET CONDITION CHECKING*

When a user wants to find by a single test whether a FET is good or bad, he may check transconductance. And when time is important, he may prefer the simple test given in Section 2.7 to the more time-consuming one in Section 2.6, especially if he has a number of FET's to check. But there are also specific test instruments for the purpose, and the service technician certainly will own one of them. These include transistor testers and combined tube/transistor testers.

Not all transistor testers, and tube testers that also test transistors, are satisfactory for testing FET's. Some of these carry the caution "not for FET's or MOSFET's." A few modern transistor testers and combined tube/transistor testers will test FET's in and out of circuit. Most of these latter instruments give a dynamic test of transconductance, employing an internally generated ac signal (e.g., 5 kHz). At this writing, at least one service-type tester is designed for FET's only, and affords both in-circuit and out-of-circuit tests for all types, including dual-gate MOSFET's.

One way of getting acquainted with FET's is to observe the transconductance of several types, using a transistor tester. In this way, the newcomer may note the basic amplifying ability of the FET and contrast it to the transconductance of tubes and the beta of bipolar transistors. Only one simple, relatively inexpensive instrument is required.

CHAPTER 3

# Elementary FET-Circuit Design Considerations

When the bipolar transistor first appeared, it caused circuit designers almost endless frustration. These specialists, long accustomed to the vacuum tube, found the low input impedance and the current dependence of the transistor uncongenial factors. Some of the new problems confronting them included stepdown coupling transformers that wasted some of the voltage gain of a preceding stage while affording a power gain, the need for additional stages in an RC-coupled amplifier for a given overall voltage gain, and somewhat inferior input/output isolation. Special components, such as af and i-f transformers, size-compatible with the transistor, eventually became available and put an end to the improvising that had become a necessary part of transistor experimenting. Even then, however, the transistor had to be constantly thought of in terms of current amplification and power gain.

Undoubtedly, had the field-effect transistor come first, the changeover from tubes would have been less painful.

In the years since the birth of the bipolar transistor, however, an entire generation of new engineers has come of age, and many of them have had most of their experience with transistors, not tubes. It seems pointless, therefore, to say to them that the FET will once again allow them to think very much along tube lines when they design circuits. Instead, it seems sufficient to present basic FET design data here, making comparisons with comparable tube and bipolar-transistor circuits where appropriate.

This chapter offers some elementary design and application data selected to acquaint the newcomer further with the FET. Illustrative examples, showing each step in calculation, are offered for the benefit of the student. For simplicity, an N-channel JFET is shown in the schematics (the $V_{DD}$ polarity is also correct for a P-channel depletion-type MOSFET). However, this JFET may be replaced in the circuits with a P-channel JFET if the polarity of $V_{DD}$ is reversed. In all equations, current is given in amperes, voltage in volts, resistance in ohms, and transconductance in mhos (multiply by $10^{-6}$ the $g_{fs}$ value given in micromhos in the FET manufacturer's data sheet).

## *3.1 DC BIAS AND CIRCUIT RESISTORS*

Like its tube and bipolar counterparts, a FET is operated at a selected point on its response curve, determined by dc bias levels. Fig. 3-1A shows a common-source circuit with the currents, voltages, and resistors involved (since gate/source current is virtually zero, for practical purposes, it is ignored in the equations, so source current $I_S$ becomes identical with drain current $I_D$). Fig. 3-1B shows a similar source-follower circuit.

### *Common-Source Circuit*

Suppose that it has been determined from the FET curves that Class-A amplifier performance requires FET Q1 (Fig. 3-1A) to be operated at $V_{DS} = 8$ V, $I_D = 0.5$ mA, and $V_{GS} = -2$ V. Suppose further that the available battery voltage $V_{DD} = 22.5$ V. The value of source resistor $R_S$ required for $V_{GS} = -2$ is:

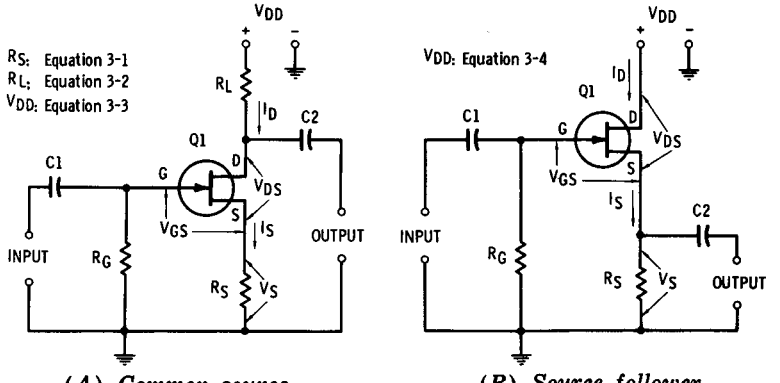
$$R_S = V_{GS}/I_D \qquad (3\text{-}1)$$
$$= 2/0.0005 = 4\ \text{k}\Omega$$

The value of the drain resistor $R_L$ is:

$$R_L = \frac{V_{DD} - (V_{DS} + I_D R_S)}{I_D} \qquad (3\text{-}2)$$
$$R_L = \frac{22.5 - [8 + 0.0005(4000)]}{0.0005}$$
$$= \frac{22.5 - (8 + 2)}{0.0005}$$
$$= 12.5/0.0005 = 25\ \text{k}\Omega$$

Another aspect of the problem of biases and resistors concerns an assigned value of $R_L$. For example, an $R_L$ value of 62 kΩ is specified, since it is twice 31 kΩ, the input resistance of a succeeding stage in a particular amplifier circuit. For the same FET given in the preceding example, $V_{DD}$ must be determined ($R_S$ will be the same 4 kΩ, since the required $V_{GS}$ still is −2 V, and drain current $I_D$ still is 0.5 mA):

$$V_{DD} = V_{DS} + (I_D R_S) + (I_D R_L) \qquad (3\text{-}3)$$
$$= V_{DS} + [I_D(R_S + R_L)]$$
$$= 8 + 0.0005(4000 + 62{,}000)$$
$$= 8 + 0.0005(66{,}000)$$
$$= 8 + 33 = 41\ \text{V}$$




*(A) Common source.* *(B) Source follower.*

**Fig. 3-1. Dc voltages.**

### *Source-Follower Circuit*

The bias situation is somewhat different in the source-follower circuit (Fig. 3-1B), since this circuit has no drain resistor. Source resistor $R_S$ serves as the output resistor, as well as the source of automatic gate bias.

As in the common-source circuit, it is desirable here to operate the FET at a point that will assure Class-A performance. Usually, since $R_S$ will be chosen beforehand for a desired output impedance, the supply voltage must be determined for the specified value of drain current.

*Example:* Suppose $R_S$ is chosen as 1000Ω, and the FET must operate at $V_{DS} = 12$ V, $I_D = 1$ mA, and $V_{GS} = -1$ V. If Equation (3-1) is rewritten $V_{GS} = I_D R_S$, then the gate-bias voltage here is $V_{GS} = 0.001(1000) = 1$ V, which was required. The required supply voltage is calculated:

$$\begin{aligned} V_{DD} &= V_{DS} + I_D R_S \\ &= 12 + [0.001(1000)] \\ &= 12 + 1 = 13 \text{ V} \end{aligned} \tag{3-4}$$

Source resistor $R_S$ has the dual function of supplying automatic gate bias to the FET and establishing the output impedance of the circuit at the same time. But it sometimes fails to perform *both* functions satisfactorily. For example, suppose that Class-A performance demands that the FET be operated at $V_{DS} = 12$ V, $I_D = 1$ mA, and $V_{GS} = -1$ V, and that $R_S$ must be 500 ohms. Equation (3-1) rewritten shows now that $V_{GS} = 0.001(500) = 0.5$ V (only one-half of the required gate voltage). The additional 0.5 V would have to be provided by a supply connected between the bottom of resistor $R_G$ and ground if, as assumed, neither $R_S$ nor $I_D$ may be changed. Conversely, if the voltage drop $I_D R_S$ exceeds the required gate-bias value, the bottom of resistor $R_G$ must be connected to a point along $R_S$ that will provide the correct voltage division.

### *Gate Resistor*

In all of the examples, the gate resistor ($R_G$) may be chosen arbitrarily. As in a tube circuit, but not a bipolar

transistor circuit, this resistance may be high (too high a value will make the circuit oversensitive to noise and stray signals) ; a common value is 1 to 20 megohms.

## 3.2 *COMMON-SOURCE AMPLIFIER (BYPASSED* $R_S$)

Fig. 3-2 shows the circuit of a single-stage, common-source, small-signal amplifier. Here, as in the common-cathode tube circuit, the source resistor ($R_S$) is bypassed (by C2). Thus, the circuit, lacking degeneration, is capable of its highest amplification under a given set of operating conditions.

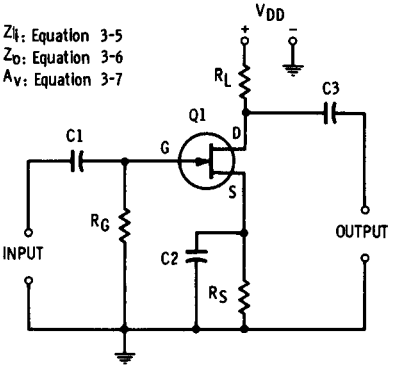



**Fig. 3-2. Common-source amplifier (bypassed $R_S$).**

### *Input Impedance*

In this circuit, the input impedance is determined by gate resistor $R_G$:

$$Z_i = R_G \qquad (3\text{-}5)$$

This convenient attribute places the input impedance of the circuit completely in the hands of the designer. In most practical instances, the gate/source resistance of the FET is enormous in comparison with any values of $R_G$ commonly chosen.

### *Output Impedance*

The output impedance is equal to the value of load resistor $R_L$. Sometimes, this resistance may be chosen arbi-

trarily; often, however, it will be better determined by means of Equation (3-2). In any event,

$$Z_o = R_L \tag{3-6}$$

### *Voltage Gain*

The open-circuit voltage amplification of the circuit may be calculated:

$$A_v = g_{fs}R_L \tag{3-7}$$

*Example:* A Type 2N3631 MOSFET with typical transconductance of 2000 $\mu$mho is operated with a drain resistor ($R_L$) of 10,000 $\Omega$. The expected voltage gain $A_v = 0.002(10{,}000) = 20$.

## *3.3 COMMON-SOURCE AMPLIFIER (UNBYPASSED $R_S$)*

If bypass capacitor C2 is omitted in Fig. 3-2, the unbypassed source resistor ($R_S$) will give rise to current degeneration, which serves to reduce distortion and to linearize response. But its action also reduces the voltage gain.

### *Input Impedance*

Here, as in the original circuit with the bypassed source resistor, the input impedance is determined by gate resistor $R_G$:

$$Z_i = R_G \tag{3-8}$$

Resistance $R_G$ is held to 1 to 20 megohms in most practical circuits, to minimize noise and stray signal pickup.

### *Output Impedance*

The output impedance, as in the preceding example, is equal to the load resistor value. Sometimes, this resistance may be chosen arbitrarily; often, however, it will be determined by means of Equation (3-2). In any event,

$$Z_o = R_L \tag{3-9}$$

### *Voltage Gain*

The open-circuit voltage amplification of the circuit may be calculated:

$$A_v = \frac{g_{fs}R_L}{1 + g_{fs}R_S} \tag{3-10}$$

*Example:* A Type 2N2608 JFET (typical transconductance = 1600 $\mu$mho) is operated with $R_L = 20$ k$\Omega$ and $R_S = 1.6$ k$\Omega$. The voltage gain is:

$$\begin{aligned} A_v &= \frac{0.0016(20{,}000)}{1 + [0.0016(1600)]} \\ &= \frac{32}{1 + 2.56} \\ &= 32/3.56 = 8.98 \end{aligned}$$

Note that if the source resistor is bypassed, and the amplification accordingly is calculated by means of Equation (3-7), $A_v = 32$, or 3.56 times the unbypassed value.

## *3.4 SOURCE FOLLOWER*

Fig. 3-3 shows the circuit of a source follower. Like the tube-type cathode follower and bipolar-transistor-type emitter follower, this circuit has many applications as a high-impedance to low-impedance converter with power gain.

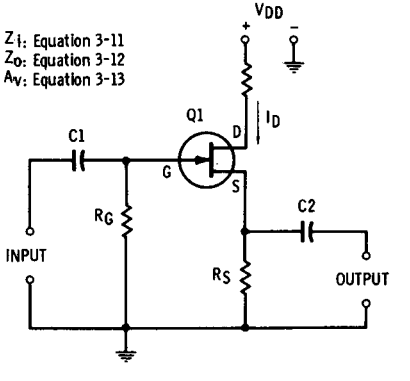



**Fig. 3-3. Source follower.**

### *Input Impedance*

In this circuit, the input impedance is determined by gate resistor $R_G$:

$$Z_i = R_G \tag{3-11}$$

Resistance $R_G$ is held to 1 to 20 megohms in most practical circuits, to minimize noise and stray signal pickup.

### *Output Impedance*

The output impedance may be calculated:

$$Z_o = \frac{R_S}{1 + g_{fs}R_S} \tag{3-12}$$

*Example:* When a Type 2N2609 JFET (transconductance = 3600 $\mu$mho, typical) is operated in the circuit in such a way that $V_{DS} = 15$ V, $I_{DS} = 1$ mA, and $V_{GS} = 0.5$ V, $R_S$ must be 500 Ω. The output impedance is:

$$\begin{aligned} Z_o &= \frac{500}{1 + 0.0036(500)} \\ &= \frac{500}{1 + 1.8} \\ &= 500/2.8 = 178.6\ \Omega \end{aligned}$$

### *Voltage Gain*

The open-circuit voltage amplification of the circuit may be calculated:

$$A_v = \frac{g_{fs}R_S}{1 + g_{fs}R_S} \tag{3-13}$$

*Example:* Use the instance of the 2N2609 JFET source follower cited in the preceding calculation of output impedance. The voltage amplification is:

$$\begin{aligned} A_v &= \frac{0.0036(500)}{1 + [0.0036(500)]} \\ &= \frac{1.8}{1 + 1.8} \\ &= \frac{1.8}{2.8} = 0.643 \end{aligned}$$

As with the cathode follower and emitter follower, the voltage "gain" of the source follower is less than 1.

## *3.5 BOOTSTRAP CIRCUIT*

Fig. 3-4 shows the circuit of a specialized source follower that is useful for increasing the typical input impedance of a JFET beyond the $10^9$-ohms maximum mentioned in Chapter 1. It takes its name from the fact that such a circuit seems to lift the input impedance by its own bootstraps.

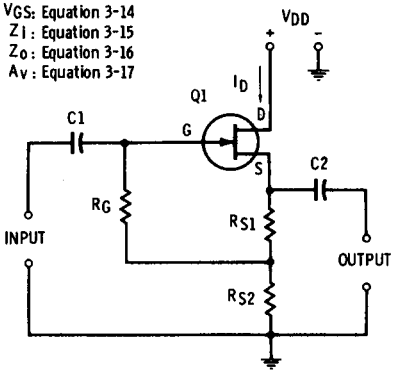



**Fig. 3-4. Bootstrap circuit.**

In this arrangement, the source resistor consists of two series-connected elements ($R_{S1}$ and $R_{S2}$), and the gate resistor ($R_G$) is returned to their junction. The $V_{GS}$ bias voltage required for correct operating point of the FET is the voltage drop developed across $R_{S1}$ by drain current $I_D$:

$$V_{GS} = I_D R_{S1} \qquad (3\text{-}14)$$

*Example:* Suppose a 2N2609 JFET (transconductance = 3600 $\mu$mho, typical) is to be operated at $V_{DS} = 15$ V, $I_{DS} = 1$ mA, and $V_{GS} = 0.5$ V. Rewrite Equation (3-14), $R_{S1} = V_{GS}/I_D = 0.5/0.001 = 500\ \Omega$. This will be the required value for the top member of the source-resistor combination.

The lower half ($R_{S2}$) of the combination must be chosen as high as the supply voltage ($V_{DD}$) will permit, in order to keep the voltage gain as high as possible. If the $R_{S2}$ value is selected as 10 k$\Omega$, the total source resistance ($R_{S1} + R_{S2}$) is

10,500 Ω, and this necessitates a drain supply ($V_{DD}$) of 10.5 V.

### *Input Impedance*

The approximate input impedance of the bootstrap circuit may be calculated:

$$Z_i = \frac{R_G(R_{S1} + R_{S2})}{R_{S1}} \tag{3-15}$$

*Example:* Assume that the gate resistor ($R_G$ in Fig. 3-4) is 1 megohm. Then $Z_i$ equals:

$$Z_i = \frac{10^6(500 + 10{,}000)}{500}$$
$$= \frac{10^6(10{,}500)}{500}$$
$$= \frac{1.05(10^8)}{5} = 21\ M\Omega$$

### *Output Impedance*

The output impedance may be calculated:

$$Z_o = \frac{R_{S1} + R_{S2}}{1 + g_{fs}\ (R_{S1} + R_{S2})} \tag{3-16}$$

*Example:* For the same JFET and the values given in the preceding discussion,

$$Z_o = \frac{500 + 10{,}000}{1 + 0.0036\ (500 + 10{,}000)}$$
$$= \frac{10{,}500}{1 + 0.0036(10{,}500)}$$
$$= \frac{10{,}500}{1 + 37.8}$$
$$= \frac{10{,}500}{38.8} = 270.6\ \Omega$$

### *Voltage Gain*

For the same JFET and the values given previously, the open-circuit voltage amplification may be calculated:

$$A_v = \frac{g_{fs}\ (R_{S1} + R_{S2})}{1 + g_{fs}\ (R_{S1} + R_{S2})} \qquad (3\text{-}17)$$

$$= \frac{0.0036\,(500 + 10{,}000)}{1 + 0.0036\,(500 + 10{,}000)}$$

$$= \frac{0.0036\ \ (10{,}500)}{1 + 0.0036\,(10{,}500)}$$

$$= \frac{37.8}{1 + 37.8} = \frac{37.8}{38.8} = 0.974$$

### *3.6 FET/BIPOLAR CASCADE*

In some impedance-transforming amplifiers, a FET is direct-coupled to a bipolar transistor. This arrangement (see Fig. 3-5) gives the circuit the high input impedance of the FET, and somewhat higher gain and lower output impedance than are afforded by a conventional source follower.

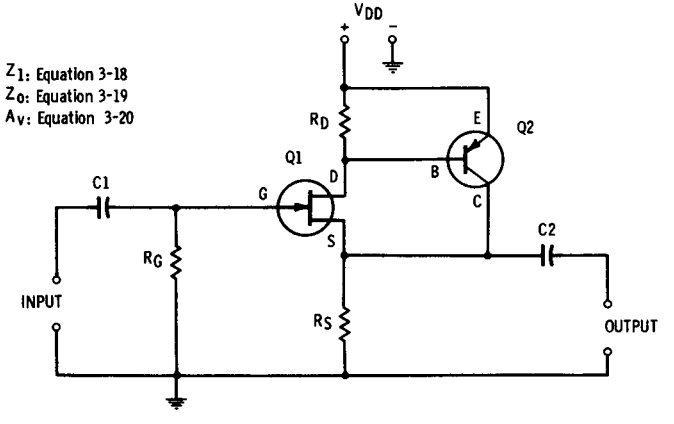



**Fig. 3-5. FET/bipolar cascade.**

For a practical example of this application, let the FET (Q1) be a Type 2N2608 JFET (transconductance = 1600 $\mu$mho, typical) and the bipolar transistor (Q2) be a 2N525 pnp unit ($h_{fe} = 30$, $h_{ie} = 1400\ \Omega$). For the resistors, $R_G = 5$ M$\Omega$, $R_D = 20$ k$\Omega$, and $R_S = 1.6$ k$\Omega$. These values will be used in the illustrative examples that follow.

### *Input Impedance*

The input impedance is equal to the resistance of the gate resistor:

$$Z_i = R_G \tag{3-18}$$

### *Output Impedance*

The output impedance may be calculated:

$$Z_o = \frac{R_S}{1 + g_{fs}R_S} \tag{3-19}$$

*Example:* For the semiconductors and the values given above:

$$\begin{aligned} Z_o &= \frac{1600}{1 + 0.0016(1600)} \\ &= \frac{1600}{1 + 2.56} \\ &= \frac{1600}{3.56} = 449.4\ \Omega \end{aligned}$$

### *Voltage Gain*

The open-circuit voltage amplification may be calculated:

$$A_v = \frac{g_{fs}\, R_S\left[h_{fe}\left(\frac{R_D}{R_D + h_{ie}}\right)\right]}{1 + g_{fs}\, R_S\left[h_{fe}\left(\frac{R_D}{R_D + h_{ie}}\right)\right]} \tag{3-20}$$

*Example:* Use the semiconductors and the circuit values given in the preceding discussion:

$$A_v = \frac{0.0016(1600)\left[30\left(\frac{20{,}000}{20{,}000 + 1400}\right)\right]}{1 + 0.0016(1600)\left[30\left(\frac{20{,}000}{20{,}000 + 1400}\right)\right]}$$

$$= \frac{2.56\left[30\left(\frac{20{,}000}{21{,}400}\right)\right]}{1 + 2.56\left[30\left(\frac{20{,}000}{21{,}400}\right)\right]}$$

$$= \frac{2.56[30(0.935)]}{1 + [2.56(30)0.935]}$$

$$= \frac{71.81}{72.81} = 0.986$$

Note that for this circuit, the voltage gain is close to unity (being only 1.4 percent lower), whereas $A_v$ for the straight source follower (Section 3.4) was 0.643, and $A_v$ for the bootstrap circuit (Section 3.5) was 0.974.

## *3.7 FET CAPACITANCE*

The capacitances of a field-effect transistor are usually so low that they often may be neglected in many circuit calculations. MOSFET input capacitance is very low. In certain instances, however, such as operation at vhf and uhf frequencies, FET capacitances must be considered, since they then become significant components of device impedances.

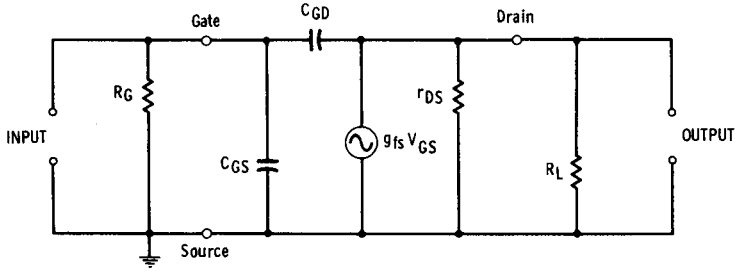



**Fig. 3-6. Equivalent circuit of common-source amplifier.**

In Fig. 3-6, the equivalent circuit of the common-source amplifier, the positions of the FET input capacitance (internal gate/source capacitance $C_{GS}$) and feedback capacitance (internal gate/drain capacitance $C_{GD}$) are shown. In this circuit, $R_G$ represents the external gate resistor, $R_L$ is the external drain (load) resistor, $r_{DS}$ is the internal drain/source resistance of the FET ($r_{DS} = V_{DS}/I_D$), and the equivalent internal generator is represented by its effect $g_{fs}V_{GS}$. Feedback capacitance $C_{GD}$ is equivalent to the grid/plate capacitance of the vacuum tube, and like the latter must be neutralized in some FET amplifiers. In metal-cased FET's,

additional capacitances are present between gate and case, drain and case, and source and case [sometimes, one electrode (e.g., the gate) is internally connected to the case, and the corresponding capacitance between that electrode and case is eliminated].

Because the FET is a relatively high-gain triode with internal feedback capacitance ($C_{GD}$), it is subject to the Miller effect, which acts to multiply the input capacitance ($C_{GS}$). The Miller effect accordingly must be taken into account in all applications (e.g., tuned amplifiers) and in all precise calculations of input impedance (or admittance) or amplifier phase shift.

CHAPTER 4

# Typical Applications

This chapter displays a number of typical applications of the FET in all types of circuits. These examples show the wide range of the uses of the device, but by no means exhaust the possibilities. While the circuits given here are primarily for illustration, the experimenter will be able to set up a selected one for operation with his own FET by means of design and performance equations given in Chapter 3 and the additional data given here. The confirmed experimenter will undoubtedly prefer the breadboard approach for determining optimum operating values for circuit components.

For a collection of practical, predesigned circuits, see the author's book *FET Circuits,* published by Howard W. Sams & Co., Inc.

## *4.1 BASIC AF AMPLIFIERS*

Fig. 4-1 shows basic single-stage FET audio-frequency amplifiers in various combinations of RC and transformer coupling. Figs. 4-1A to D show common-source circuits;

Figs. 4-1E to H show source-follower circuits. An N-channel JFET is shown in each circuit, but another type of FET may be used, provided the polarity of $V_{DD}$ is reversed where required. For working out the dc bias values for the circuits, see Equations (3-1) to (3-4), in Chapter 3. The single-stage circuits may be cascaded in any combination to secure a desired overall amplification.

Fig. 4-1A shows a common-source amplifier with RC input and RC output. This is perhaps the most common arrangement in audio-frequency systems, since it is both simple and compact, and is often the least susceptible to interference. Equations (3-5) to (3-7), in Chapter 3, depict design and performance of this circuit. If bypass capacitor C2 is omitted, the voltage gain will decrease, but fidelity will be improved as a result of negative feedback developed across resistor $R_S$ [see Equations (3-8) to (3-10), in Chapter 3].

Because of the high input impedance of this circuit, such stages are easily cascaded, with no signal-voltage loss be-

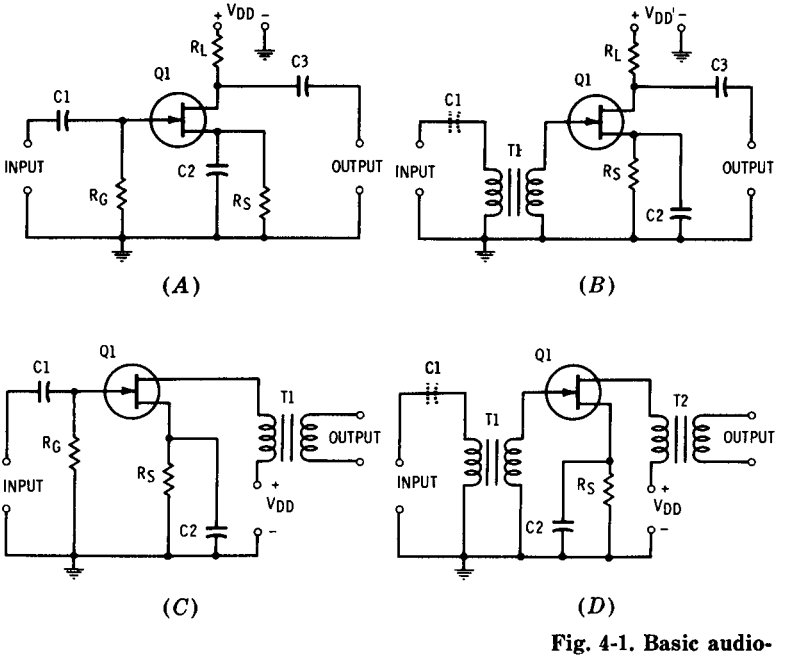
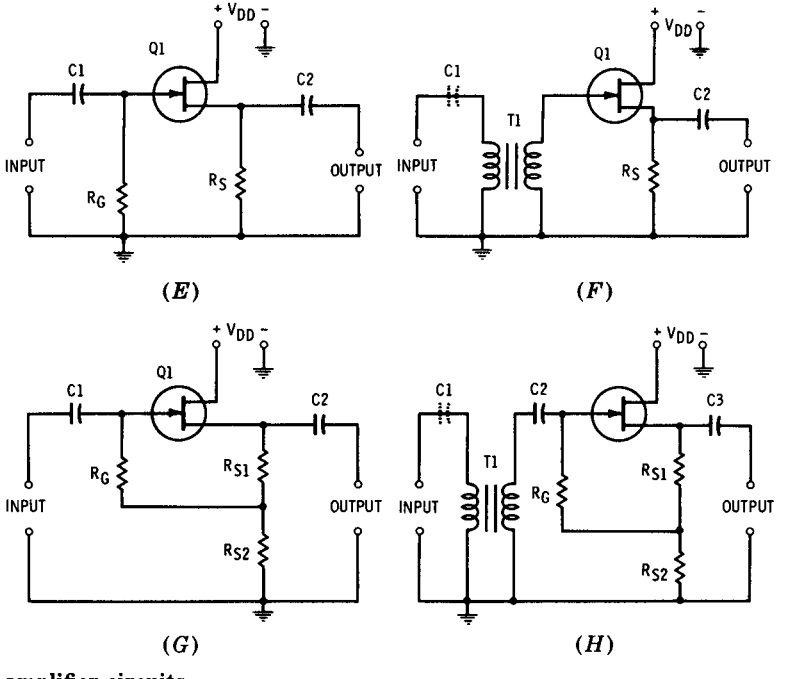



**Fig. 4-1. Basic audio-**

tween stages. Correctly, each succeeding stage should be gate-biased higher than the preceding one, to accommodate the higher signal-voltage level that it receives; this is standard multistage amplifier design. But, for simplicity, identical stages often are cascaded, and the input-signal voltage to the entire system is reduced.

Fig. 4-1B shows an amplifier with transformer input (T1) and RC output. This arrangement enables a certain amount of voltage step-up to be obtained through the transformer, rather than with an additional amplifier stage. The high input impedance of the FET imposes virtually no load on the transformer. When the transformer primary winding must be protected from a dc component in the input signal, blocking capacitor (C1) may be inserted.

Fig. 4-1C shows RC input and transformer output. This arrangement allows either a signal-voltage step-up or step-down, as required, to be obtained at the output of the amplifier. When this type of stage is followed by an RC-input




**amplifier circuits.**

stage, such as in Fig. 4-1A, T1 becomes an interstage coupling transformer—and the second stage, because of its high input impedance, imposes virtually no load on the transformer.

In Fig. 4-1D, both input and output are transformer coupled (T1, T2). Any required combination of signal-voltage step-up or step-down may be obtained by proper selection of transformer turns ratio. If the T1 primary winding must be protected from a dc component in the input signal, a blocking capacitor (C1) may be inserted.

Fig. 4-1E shows a conventional source follower with RC input and RC output. Equations (3-11) to (3-13), in Chapter 3, depict design and performance of this circuit. This arrangement is often used to provide high input impedance for a lower-impedance device. Thus, a source follower may be followed in cascade by a common-emitter bipolar-transistor RC-coupled stage. In this way, the high input impedance of the FET and the high-voltage amplification of the bipolar transistor are available, and the bipolar circuit thus becomes compatible with such high-impedance devices as the crystal microphone, piezoelectric transducer, etc.

Fig. 4-1F shows a source follower with transformer input (T1). Here also, Equations (3-11) to (3-13), in Chapter 3, depict design and performance. The input transformer allows any desired step-up or step-down of input-signal voltage. The high input impedance of the FET reduces virtually to zero any loading of the transformer. If the primary winding of T1 must be protected from a dc component in the input-signal voltage, a blocking capacitor (C1) may be inserted.

Fig. 4-1G shows a conventional bootstrap circuit. This arrangement is convenient when a source follower is needed with input impedance higher than that ordinarily obtained with a JFET, and low input capacitance. Equations (3-14) to (3-16), in Chapter 3, depict design and performance. This circuit, with its added advantages, is usable for the same functions as those afforded by the conventional source follower (Figs. 4-1E and F).

Fig. 41H shows a bootstrap circuit with transformer input (T1). Here, as in Fig. 4-1G, Equations (3-14) to (3-16),

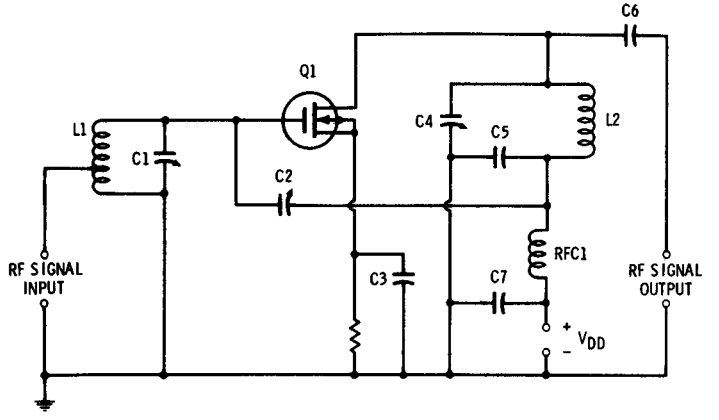
in Chapter 3, depict design and performance. Blocking capacitor C2 is necessary to prevent the secondary winding of T1 from short-circuiting the $R_G$-$R_{S1}$-$R_{S2}$ bias network. If the primary winding of T1 must be protected from a dc component in the input-signal voltage, another blocking capacitor (C1) may be inserted as shown by the dotted symbol. As in the other circuits with transformer input, T1 allows any desired step-up or step-down of signal voltage simply by appropriate selection of its turns ratio.

## *4.2 BASIC RF AND I-F AMPLIFIERS*

Fig. 4-2 shows basic single-stage FET radio-frequency and intermediate-frequency amplifiers. MOSFET's are shown in two of these circuits (Figs. 4-2A and 4-2D), and JFET's are shown in the other two (Figs. 4-2B and 4-2C). However, any desired type of FET may be used in any of these circuits, provided the $V_{DD}$ polarity and the circuit constants—particularly the drain resistor and $V_{DD}$ magnitude—are correctly chosen for that type (see Chapter 3). For Class-A operation, the bias levels for a given FET will be the same as for the basic af amplifiers described in Section 4.1. When, instead, high harmonic content is desired (as when the amplifier is used as a frequency doubler, tripler, or quadrupler), the biases and rf input-signal voltage are adjusted for operation near the ohmic ("triode") region of the FET characteristic. Source bypass capacitors (C3 in Fig. 4-2A, C2 in 4-2B, and C2 in 4-2D) and drain-supply bypass capacitors (C7 in Fig. 4-2A, C3 in 4-2B, C3 in 4-2C, and C3 in 4-2D) must be chosen for lowest practical reactance at the signal frequency.

Fig. 4-1A shows a conventional tuned-input/tuned-output rf amplifier. This is a well-known circuit in tube and transistor practice (receivers, transmitters, and instruments), and may be used at any frequency at which FET Q1 is capable of operating, including intermediate and audio frequencies. The input tank (L1-C1) and output tank (L2-C4) both are tuned to the desired signal frequency. Since this condition encourages oscillation, a neutralizing capacitor (C2) has been provided (sometimes, it is desirable

to supply the dc drain voltage at a tap on inductor L2 and to connect C2 to the bottom of that inductor). The input signal is presented to the input tank through a suitable impedance-matching tap on inductor L1; however, this signal may also be inductively coupled into L1 by means of a suitable coupling coil, or capacitively coupled into L1 through a capacitor connected to the top of L1. Similarly, capacitive output coupling is provided by capacitor C6; this results in high output impedance. Output coupling may also be obtained through a low-impedance tap on inductor L2 or

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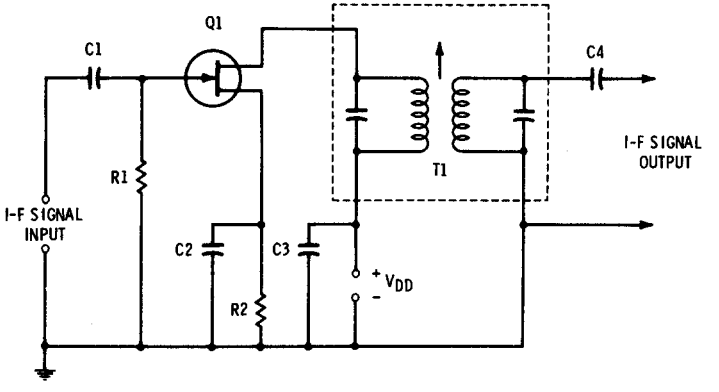
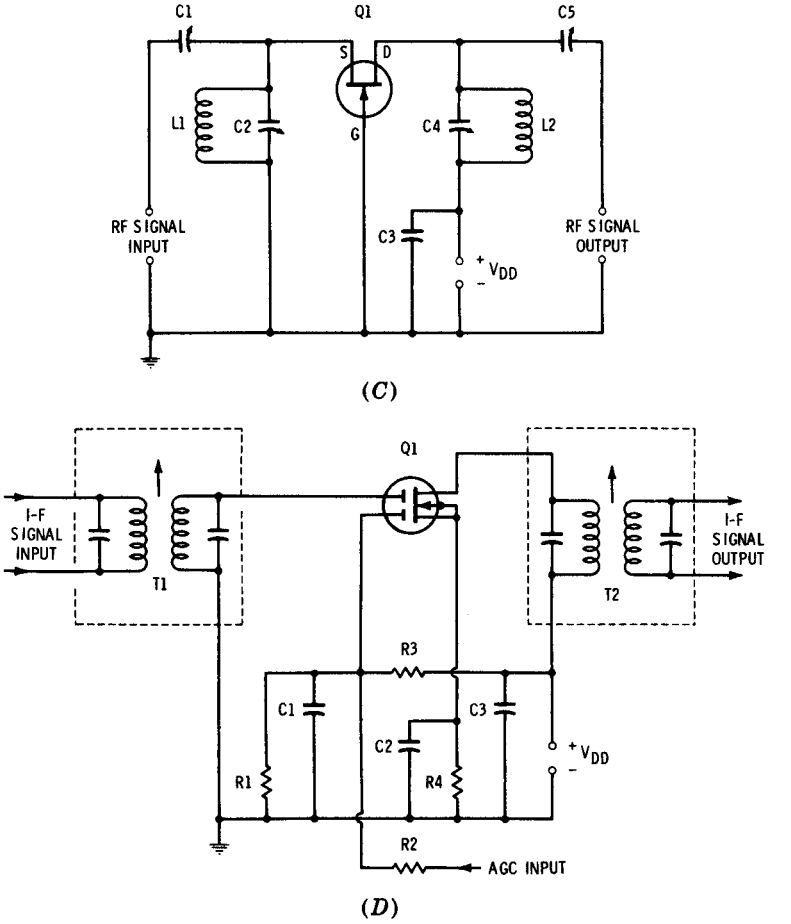



(*B*)

**Fig. 4-2. Basic rf and**

through a suitable output-coupling coil. In receiver service, C1 and C4 are ganged.

Fig. 4-2B shows an i-f amplifier with untuned input and tuned output (i-f transformer T1). An advantage of this arrangement is that, lacking a resonant input circuit, the amplifier is not so likely to oscillate as is its double-tuned counterpart. The input circuit is high impedance; therefore, this amplifier may readily be connected to a signal source, such as a receiver front end, without introducing signal loss. When an input i-f transformer is used (as in Fig. 4-2D),




**i-f amplifier circuits.**

the circuit may or may not tend to oscillate, depending on stage gain and the drain/gate capacitance of the FET. If it does oscillate, however, the circuit may easily be neutralized (see Fig. 4-2A).

Fig. 4-2C shows a common-gate rf amplifier. This arrangement is comparable to the grounded-grid vacuum-tube amplifier and common-base bipolar-transistor amplifier. Particular advantages of the common-gate circuit are its ability to operate without neutralization up to ultrahigh frequencies, and the presence in its output of both the input rf driving power and the Q1 rf output power. This circuit is particularly useful in FET transmitter circuits; e.g., the Type 2N3823 JFET, which gives a power gain of 10 dB at 200 MHz in this circuit, with a dc power input of 0.3 W, and the Type U222 JFET, which is capable of 0.8 W dc power input.

Fig. 4-2D shows a dual-gate MOSFET i-f amplifier circuit with provision for automatic gain control. This circuit has been used, as shown, without neutralization; however, it may easily be neutralized (see C2 in Fig. 4-2A) should it oscillate as a result of input/output tuning (i-f transformers T1 and T2). The agc level is set by a positive voltage developed at one gate of the MOSFET by the dc drain-supply voltage divider, R1-R3. A reverse agc bias is also applied to the same gate through isolating resistor R2.

## *4.3 BASIC OSCILLATORS*

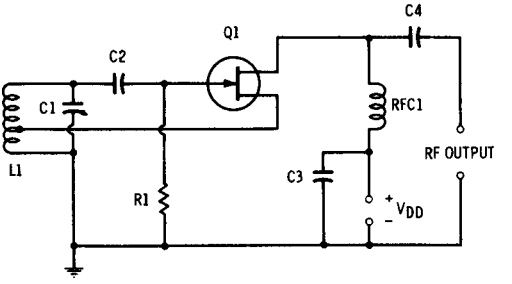
Fig. 4-3 shows basic single-stage FET rf and af oscillators. Although JFET's are shown, FET's of other types also may be used, provided the $V_{DD}$ polarity and circuit constants—particularly the source resistor and $V_{DD}$ magnitude —are correctly chosen for that type (see Chapter 3). For sine-wave output, Class-A bias levels must be used, and will be the same as for the basic af amplifiers described in Section 4.1. When, instead, high harmonic output is desired (as when the rf oscillators are used as frequency standards or as drivers for doubler, tripler, or quadrupler stages), the dc gate voltage may be adjusted to a point that will ensure signal-voltage overdriving of the gate. In all of the circuits,

source bypass capacitors (C1 in 4-3C, C1 in 4-3D, C3 in 4-3E, and C4 in 4-3F) and drain-supply bypass capacitors (C3 in Fig. 4-3A, C1 in 4-3B, C2 in 4-3C, C2 in 4-3D, C1 in 4-3E, and C6 in 4-3F) must be chosen for the lowest practical reactance at the signal frequency.

Fig. 4-3A shows a Hartley-type rf oscillator. In this well-known circuit, tapped inductor L1 serves as an autotransformer in which output-signal current in the lower section of the winding induces a gate/source feedback voltage across the upper section. (The frequency of oscillation (f) equals $1/6.28\sqrt{L1C1}$, where f is in hertz, L1 is in henrys and C1 is in farads.) For sine-wave output, the tap must be placed at ⅓ to ½ the distance from the grounded end of L1, the exact point affording the best compromise between signal-output voltage and sinusoidal waveform. The capacitance output coupling (through C4) shown here provides high output impedance, and may be used only with light loading, and even then only when the load will not detune or stop the oscillator. Inductive output coupling (low or high impedance, as desired) may be obtained by means of a suitable output coil coupled to the lower end of L1.

Fig. 4-3B shows a Colpitts-type rf oscillator. This circuit is distinguished by the split-capacitor (C4-C5) tuning, and is often used in instruments such as dip oscillators. A particular advantage of the Colpitts circuit is its allowance of an untapped inductor. In this circuit, dc gate-bias voltage is developed by the rectified gate/source current through resistor R1. With some FET's, especially MOSFET's, this method may not work, and a source resistor/capacitor combination (such as C1 and R2 in Fig. 4-3C) must be inserted between source and ground to obtain the required bias. The capacitance output coupling (through C6) shown here provides high output impedance, and may be used only with light loading, and even then only when the load will not detune or stop the oscillator. Inductive output coupling (low or high impedance, as desired) may be obtained by means of a suitable coil coupled to the center of L1.

Fig. 4-3C shows a conventional, tuned-drain crystal rf oscillator. This circuit is comparable to the tuned-plate vacuum-tube or tuned-collector bipolar-transistor crystal

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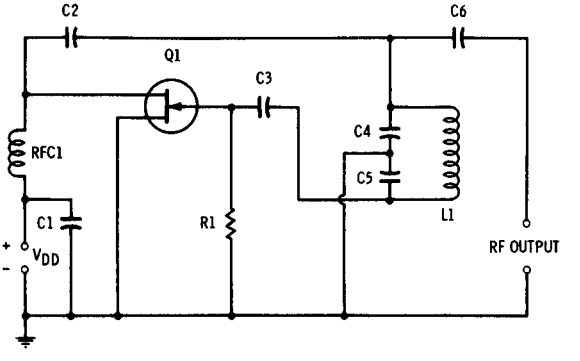


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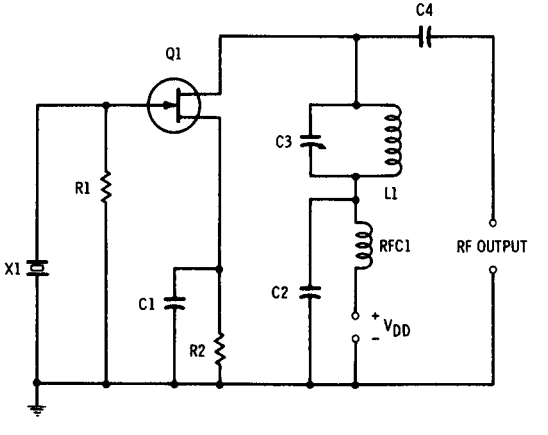


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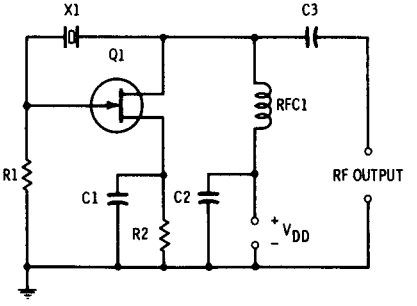
**Fig. 4-3. Basic**

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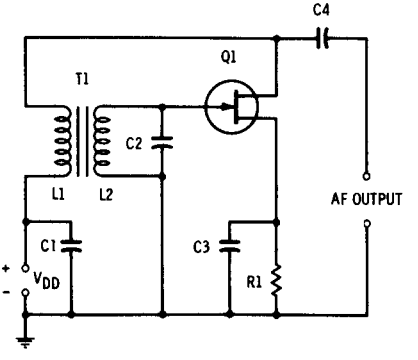


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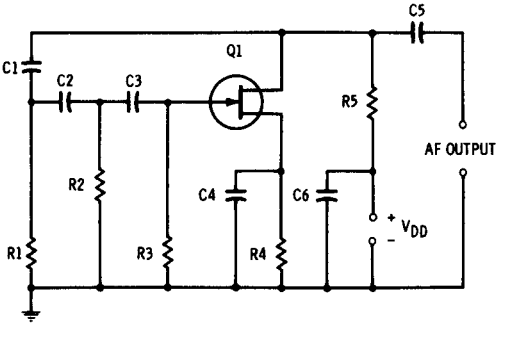


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**oscillator circuits.**

oscillator. For oscillation, the output tank (L1-C3) simply is tuned to the crystal frequency. The capacitive output coupling (through C4) shown here provides high output impedance, and is satisfactory only for light loading, and even then only when the load will not detune or stop the oscillator. Inductive output coupling (low or high impedance, as desired) may be obtained by means of a suitable output coil coupled to the lower end of L1.

Fig. 4-3D shows a conventional Pierce crystal oscillator. This circuit requires no tuning: simply plug in the crystal (X1), and obtain rf output. However, it oscillates at the fundamental frequency of a harmonic-type crystal, not at the labeled (harmonic) frequency. The Pierce circuit makes a very simple frequency spotter if its gate bias is adjusted for a rich harmonic rf output. In this way, a 100-kHz crystal will furnish check points every 100 kHz apart, far into the radio spectrum (see also Fig. 2-6, in Chapter 2). The capacitive output coupling (through C3) shown here provides high output impedance, and is satisfactory only for light loading, and even then only when the load will not detune or stop the oscillator. Lower-impedance output, when required, may be obtained by capacitance coupling the rf output from the top of resistor R2 after omitting bypass capacitor C1. With some FET's, however, omission of the bypass capacitor will reduce the gain of the circuit to such an extent that oscillation will cease (see Section 3.3, in Chapter 3).

Fig. 4-3E shows a transformer-feedback af oscillator. In this circuit, signal voltage is fed from the output (drain) section back to the input (gate) section by transformer T1, which is poled correctly for regeneration. Here, the secondary winding (L2) of the transformer is tuned by capacitor C2 ($f = 1/6.28\sqrt{L2C2}$, where f is in hertz, L2 is in henrys, and C2 is in farads). But either winding may be tuned if it has sufficient inductance. The turns ratio of the transformer must be such that the FET gate is not overdriven by the fed-back signal. This, together with Class-A dc gate bias, is essential for sine-wave output. The capacitive output coupling (through C4) shown here provides high output impedance, and is satisfactory only for light load-

ing, and even then only when the load will not detune or stop the oscillator.

Inductive coupling (low or high impedance, as desired) may be obtained by means of a third (output) winding on transformer T1. Lower-impedance output may be obtained by capacitance coupling the af output from the top of resistor R1 after omitting bypass capacitor C3. With some FET's, however, omission of the bypass capacitor reduces the gain so greatly through degeneration that oscillation ceases (see Section 3.3, in Chapter 3). For output isolation, this oscillator may be followed by a source-follower stage (Figs. 4-1E and G).

Fig. 4-3F shows a phase-shift-type af oscillator. In this circuit, tuning is entirely by means of resistances and capacitances. This circuit also gives excellent sine-wave output. The RC network (C1, C2, C3, R1, R2, R3) controls both oscillation and frequency. Each leg of the network (R1-C1, R2-C2, and R3-C3) introduces 60° phase shift (180° total for the entire network). Since the network is connected from the output (drain) to the input (gate) portion of the circuit, it transmits signal feedback voltage in the correct phase for oscillation (when C1 = C2 = C3, and R1 = R2 = R3, the signal frequency f = 91,900/R1-C1 approximately, where f is in hertz, R1 is in ohms, and C1 is in $\mu$F). Since the three-leg network has a natural attenuation, a high-amplitude signal voltage is required at the drain of Q1; otherwise, the voltage fed back to the gate will be too weak to initiate and maintain oscillation. This calls for a FET with high transconductance. The capacitive output coupling (through C5) shown here provides high output impedance, and is satisfactory only for light loading, and even then only when the load will not detune or stop the oscillator. Lower-impedance output may be obtained by capacitance coupling the af voltage from the top of resistor R4 after omitting bypass capacitor C4. With some FET's, however, omission of the bypass capacitor reduces gain so greatly through degeneration that oscillation ceases (see Section 3.3, in Chapter 3). For output isolation, this oscillator may be followed with a source-follower output stage (see Figs. 4-1E and G).

## *4.4 COMBINATION OSCILLATORS*

The rf oscillator circuits shown in Figs. 4-3A and B may be used also at audio frequencies by suitably selecting the inductance and capacitance values in the tuned circuits. In most cases, this will consist of substituting an iron-core inductor for the air-core L1, and raising the capacitance of C1 in Fig. 4-3A and of C4 and C5 in Fig. 4-3B. Often, L1 will be one winding of a transformer; the other winding serves as an output-coupling coil. (Sometimes in the Colpitts circuit, Fig. 4-3B, L1 is replaced with magnetic headphones that serve as the frequency-determining inductor, as well as the reproducer.) It is not unusual for simple oscillators of this kind to serve for both af and rf use. A set of plug-in tuning units' (inductors or inductor/capacitor combinations) is usually supplied to provide the various frequencies.

The observations made earlier (Section 4.3) concerning capacitive output coupling and its limitations apply as well to the rf oscillators converted for af operation.

## *4.5 MIXER/CONVERTER*

Mixers, or converters, are common and useful in the front ends of superheterodyne receivers and heterodyne-type rf test instruments. Fig. 4-4 shows one simple type of FET

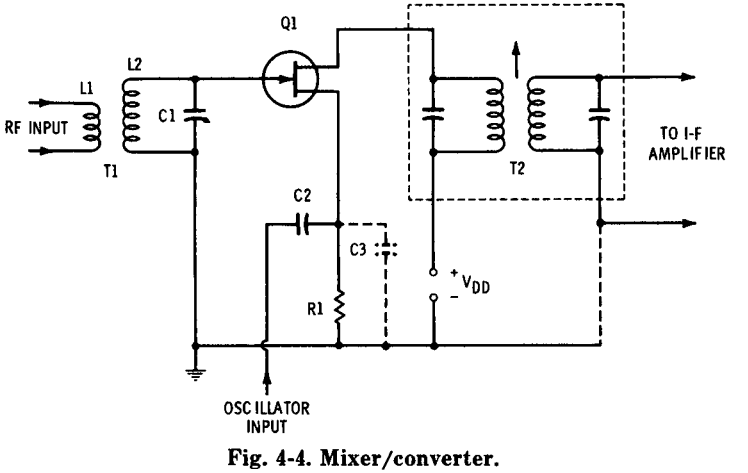


**Fig. 4-4. Mixer/converter.**

mixer/converter. This is basically an amplifier circuit in which the rf input is injected at the gate of the FET (through rf transformer T1), the local oscillator signal is injected (through capacitor C2) across the usually unbypassed source resistor (R1), and the i-f signal is coupled out of the drain circuit through the i-f transformer (T2). The field-effect transistor is especially effective as an rf mixer, since in this function its cross modulation (minimized by its square-law transfer characteristic) and noise figure are superior to those of either the vacuum tube or the bipolar transistor.

## *4.6 AF AMPLIFIER WITH AGC*

Fig. 4-5 shows the circuit of a simple audio-frequency voltage amplifier incorporating automatic gain control. This is a conventional RC-coupled arrangement to which has been added the signal rectifier circuit D1-R5-R8. The low-voltage dc gate control feature of the FET suits it very well to agc amplifier operation.

Operation of the circuit is straightforward: The output signal appearing across resistor R8 is rectified by diode D1. The resulting direct current is transmitted by filter resistor R5 to the gate of the input FET (Q1) through gate resistor

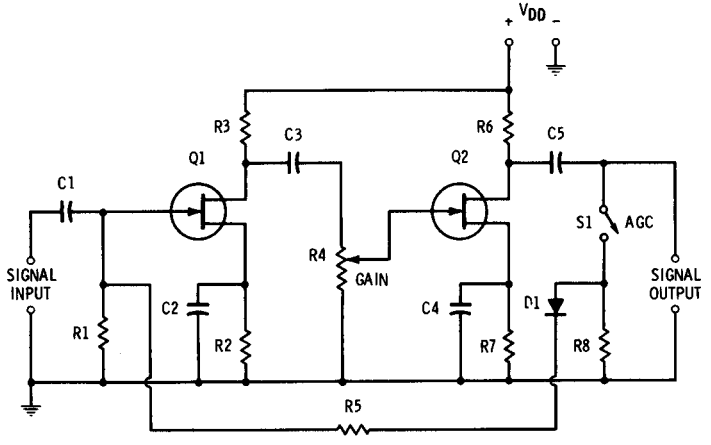


**Fig. 4-5. Audio amplifier with agc.**

R1 to ground. The corresponding voltage drop across R1 is in the correct polarity to reduce the gain of Q1 if diode D1 is correctly poled. With the JFET shown here, the normal gate bias is negative, so the agc voltage must be positive. When R5 is properly proportioned with respect to R1, the dc agc voltage developed at the gate by diode D1 will set the optimum level for the control action. As the input-signal voltage increases, so does the output-signal voltage across R8. The dc output of D1 increases proportionately and decreases the gain of Q1 (and accordingly that of the entire amplifier), thus reducing the output-signal voltage. It is in this way that the gain is automatically controlled.

Diode D1 should be a silicon unit, since the very high front-to-back resistance ratio of the silicon diode permits high resistances for R5 and R8. This means that R8 will not adversely load the amplifier and also that good voltage-divider performance may be obtained with the normally high gate resistor, R1.

## *4.7 CHOPPER*

Numerous circuits have been designed for solid-state dc-to-ac choppers. Fig. 4-6 shows an asymmetrical circuit that uses a FET to exploit the simplicity of a single-transistor circuit.

A square-wave switching signal, supplied by generator G1 through coupling transformer T1, alternately switches the FET (Q1) on and off. This switching signal is applied between gate and source. When Q1 is ON, the dc input-signal current is conducted through Q1 and output resistor R1.

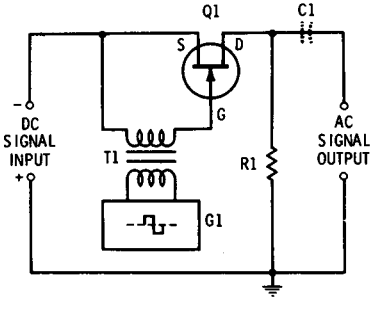


**Fig. 4-6. Chopper.**

The voltage drop developed across R1 constitutes the output signal. When Q1 is OFF, the path through the FET is effectively open. Ideally, no voltage appears across R1. In effect, then, the FET acts as a fast-working electronic switch that alternately connects and disconnects R1 and the DC SIGNAL INPUT terminals.

The output-signal voltage is proportional to the dc input-signal voltage, and has the frequency of the switching voltage. Common practice is to amplify the chopper-circuit output with an ac amplifier, and then to rectify the output of the latter back to dc, securing in this way the desired dc voltage amplification without the instability so often encountered with a dc amplifier. Capacitor C1 is inserted when the chopper must be blocked from the external device.

Unbalanced circuits of this kind using bipolar transistors have often been undesirable because of their significant offset voltage (output voltage present during the OFF interval). The FET, owing to its very high resistance, permits very little leak-through, and this results in offset levels of only a few microvolts.

## *4.8 ELECTRONIC DC VOLTMETERS*

The vacuum-tube voltmeter was never seriously challenged by any bipolar-transistorized version of itself. The reason for the poor competitive position of the transistorized instrument was the low input resistance of the bipolar, which usually restricted the sensitivity to 100,000 ohms per volt, with a different input resistance on each range. Nevertheless, many such transistorized voltmeters have been used because they offered economical, portable battery operation for the first time, and also because the input resistance is comparable to that of a vacuum-tube voltmeter on the 100-V range.

Now the FET permits transistorization of the voltmeter, with all of the advantages of the VTVM (constant input resistance—e.g., 11 megohms—on all ranges, linear dc response, and low drift) plus independence from the power line, and low battery drain. Figs. 4-7 and 4-8 show FET electronic dc voltmeter circuits. The exact correspondence with equivalent VTVM circuits is easily seen.

A single-FET (unbalanced) circuit is shown in Fig. 4-7. Like its tube counterpart, this circuit needs to be reset to zero oftener than the conventional balanced circuit does. However, its zero drift is slight and very slow, and the circuit response is linear. The simplicity of this circuit is noteworthy.

The total resistance of the input-signal voltage divider (R1 to R4) commonly is 10 megohms. An additional 1-megohm isolating resistor in the dc probe brings the input resistance of the instrument up to 11 megohms on all ranges. However, this resistance may be increased, if desired, especially if a MOSFET is employed (100 megohms input is not unusual). While 1-, 10-, 100-, and 1000-V ranges are shown here, intermediate ranges also are often provided: e.g., 0.3, 3, 30, 300, and 3000 V. Resistor R5 introduces no voltage drop, but with capacitor C1 forms a simple input filter for removing stray ac signals that may be picked up by the input circuit of the instrument.

Potentiometer R8 is the conventional zero-set control, and rheostat R6 is the calibration control that allows meter M1 to be set initially to full scale with a standard dc input voltage, such as 1 V. The zero-set operation consists of balancing the drain-circuit bridge whose four arms are R7, the internal drain/source resistance ($r_D$) of the FET, and the two halves of R8.

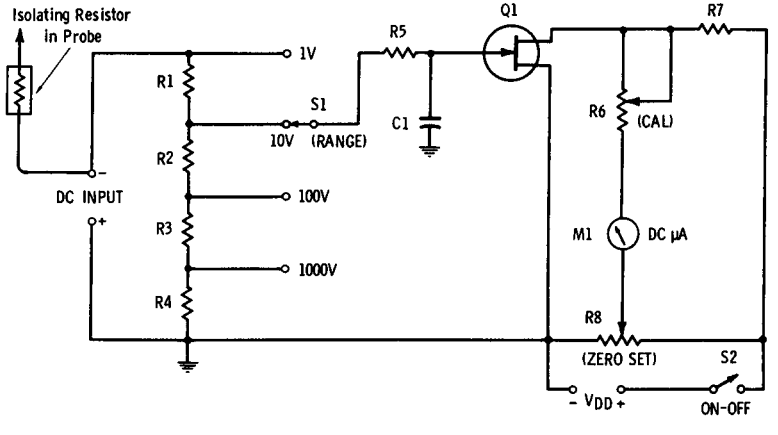


**Fig. 4-7. Electronic dc voltmeter (single-ended).**

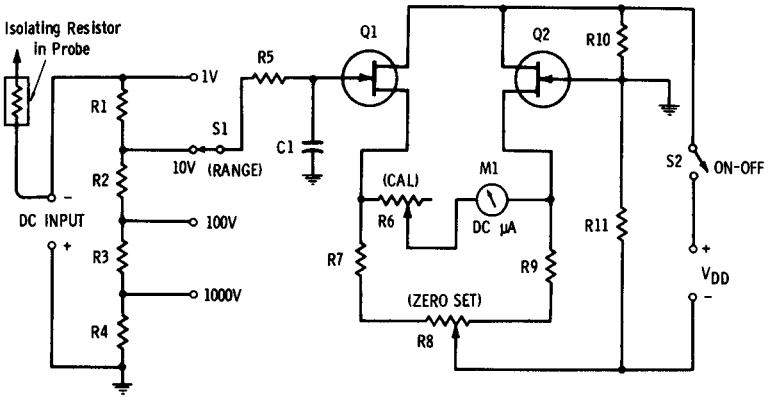


**Fig. 4-8. Electronic dc voltmeter (balanced).**

An input shunt-diode probe will adapt the instrument to ac voltage measurement, but a special calibration of meter M1 then will be needed, owing to the nonlinearity of the diode at low voltages.

Fig. 4-8 shows a two-FET (balanced) circuit. Like its tube counterpart, this circuit has almost no zero drift; and once potentiometer R8 is set to zero microammeter M1, it seldom needs resetting. Also, the circuit is remarkably free from the effects of varying FET parameters.

As in the equivalent tube circuit, the total resistance of the input-voltage divider (R1 to R4) commonly is 10 megohms, and an additional 1-megohm isolating resistor in the dc probe brings the input resistance of the instrument up to 11 megohms on all ranges. However, this resistance may be increased, if desired, especially if a MOSFET is employed (100 megohms input is not unusual). While 1-, 10-, 100-, and 1000-V ranges are shown here, intermediate ranges also are often provided: e.g., 0.3, 3, 30, 300, and 3000 V. Resistor R5 introduces no voltage drop, but with capacitor C1 forms a simple filter for removing any stray ac signals that may be picked up by the input circuit of the instrument.

Potentiometer R8 is the conventional zero-set control, and rheostat R6 is the calibration control that allows meter M1 to be set initially to full scale with a standard input voltage, such as 1 V. The zero-set operation consists of balancing the drain-circuit bridge whose four arms are more complicated

than those in the one-FET circuit (Fig. 4-7). Fig. 4-9 shows the equivalent bridge of the two-FET circuit. Here, $r_{D1}$ and $r_{D2}$ are the internal drain/source resistances of FET's Q1 and Q2, respectively. The four arms of the bridge are: Arm $1 = r_{D1}$, Arm $2 = R7 + R_x$, Arm $3 = r_{D2}$, Arm $4 = R9 + R_y$.

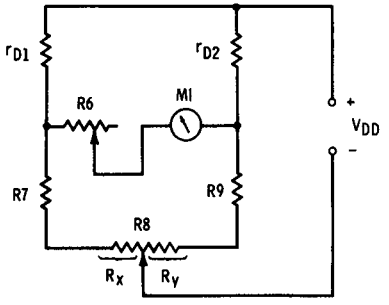


**Fig. 4-9. Equivalent zero-set bridge.**

An input shunt-diode probe will adapt the instrument to ac voltage measurement, but a special calibration of meter M1 will be needed, because of the nonlinearity of the diode at low voltages.

## *4.9 ELECTRONIC AF VOLTMETER*

A standard design for an electronic voltmeter for measuring af volts and millivolts (down to 1 mV full scale) consists of a high-gain af amplifier followed by a rectifier-type dc meter. There are many vacuum-tube voltmeters of this type. Fig. 4-10 shows a FET version of this useful instrument.

The FET af amplifier provides the necessary voltage stepup from low input-signal voltages. The amplifier output-signal voltage is transmitted to the rectifier-type meter circuit (D1-D2-R5-M1) through blocking capacitor C2. The amplifier gain must be high enough to raise the lowest desired input-signal voltage to the level required to deflect M1 to full scale (2.5 V rms deflects a 0-100 dc microammeter to full scale when D1 and D2 are 1N34A germanium diodes, C2 = 0.02 $\mu$F, C3 = 1 $\mu$F, and R5 = 0). In the meter circuit, rheostat R5 is the calibration control that permits M1 to be

set to full scale with a standard af input voltage (at the AF INPUT terminals), e.g., 1 V.

The total resistance of the input-signal voltage divider (R1 to R4) commonly is 10 megohms, although in some commercial instruments it is as low as 1 megohm. However, this resistance may be increased, if desired, especially if a MOSFET is in the first stage of the amplifier. The range taps are unlabeled in Fig. 4-10, but common input-signal voltages for full-scale deflection are 1, 3, 10, 30, 100, and 300 mV; and 1, 3, 10, 30, 100, and 300 V. Blocking capacitor C1 protects the instrument from any dc component in the input signal.

For wide frequency response (most vacuum-tube voltmeters of this type operate up to 1 MHz), the amplifier must be properly compensated. The method, employing compensating inductors and selected drain and source resistor values, is essentially the same as that used in the design of tube-type video amplifiers.

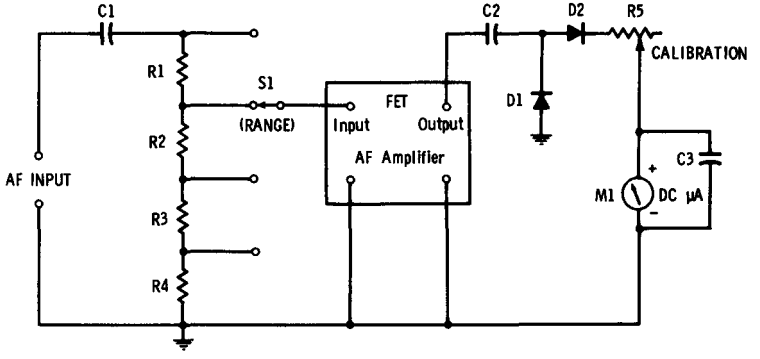


**Fig. 4-10. Electronic audio-frequency voltmeter.**

## *4.10 INTERVAL TIMER*

The use of a field-effect transistor in a simple RC-type electronic timer is completely successful, since the FET gate, like the vacuum-tube grid, does not load the timing capacitor. Fig. 4-11 shows a timer circuit of this kind. In this arrangement, the time interval during which the relay (RY) remains closed is determined by capacitance C1 and re-

sistance R1 ($t = 10^{-6}$ RC, where t is in seconds, R is in ohms, and C is in microfarads). Since R1 is a rheostat, this resistance may be calibrated and subsequently set to any desired time value within the R1-C1 range. Switch S1 (usually a pushbutton) is a single-pole double-throw unit normally closed in position B. When S1 momentarily is thrown to position A, capacitor C1 charges almost instantaneously from battery B1. When S1 is allowed to return to position B, the capacitor discharges through resistance R1 in RC seconds. The voltage of battery B1 must not exceed the gate/source bias voltage developed by drain current in source resistor R2.

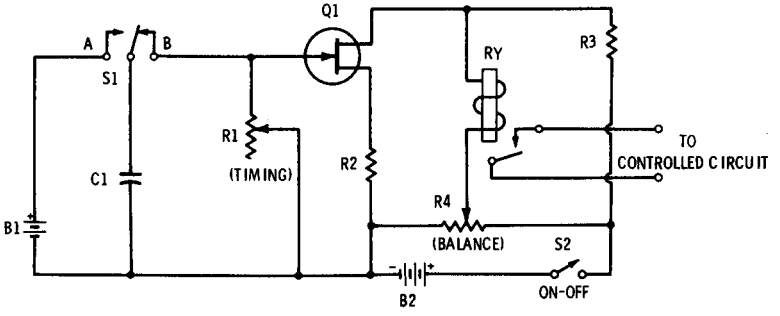


**Fig. 4-11. Interval timer.**

Relay RY is a sensitive dc unit (usually 1-mA pickup) that is connected in a bridge circuit in the FET output so that the steady drain current may be balanced out of its coil. The four arms of the bridge consist of $r_D$ (the internal drain/source resistance of FET Q1), resistor R3, and the two halves of balancing potentiometer R4. When S2 first is closed, if R4 is not accidentally in balance, the FET drain current will pick up the relay. The adjustment of R4 then balances the bridge and reduces the relay-coil current to zero; the relay accordingly drops out (just as adjusting the zero-set potentiometer in an electronic voltmeter circuit zeroes the meter). The timer then is ready to operate.

The operation consists of closing S1 momentarily to position A and then releasing it to return to position B. This causes C1 to charge from battery B1 and then to apply a positive voltage to the gate of Q1. This reduces the negative

bias already present at the gate, and increases the drain current. The bridge accordingly unbalances, and the relay is picked up. Meanwhile, capacitor C1 discharges slowly through R1, and when it has discharged sufficiently, the original negative gate-voltage value will be re-established; the drain current will decrease and the relay will drop out.

## *4.11 FLIP-FLOP*

There are many circuits for solid-state flip-flops; some of them are highly sophisticated. Fig. 4-12 shows the basic circuit, here employing a pair of JFET's (Q1 and Q2).

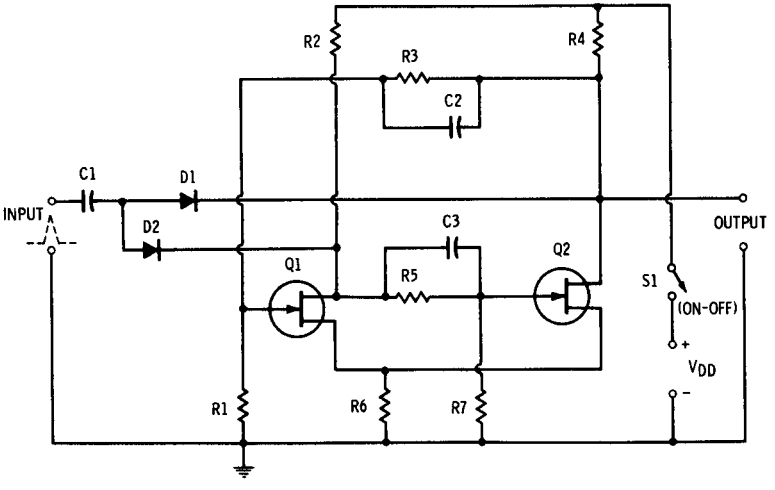


**Fig. 4-12. Flip-flop.**

The bistable mode of operation of this flip-flop is identical with that of the equivalent tube circuit: The FET's are either conducting or nonconducting; when Q1 is ON, for example, Q2 is OFF. The "ON" FET automatically switches the other FET "OFF," and vice versa. Whichever FET is ON will remain ON until it is switched off by means of an actuating signal, or until the $V_{DD}$ dc supply is shut down; likewise, whichever FET is OFF will remain OFF until it is switched on by an actuating signal, or until the $V_{DD}$ dc

supply is shut down. This switching back and forth between the two FET's is accomplished by means of a sharp positive pulse injected at the INPUT terminals. The output of the flip-flop is connected to the drain of Q2; but this FET is ON only half of the time, which means that the number of output pulses in a given interval of time is one-half the number of input pulses. The flip-flop therefore is a scale-of-2 frequency divider.

The operation of the circuit shown in Fig. 4-12 starts when the on-off switch, S1, is first closed. Drain current then exists in both FET's, but a transient pulse, caused by the switch closure or by random noise, drives the gate of one FET, momentarily causing the drain current of that FET to exceed the drain current of the other one. If, for illustration, the affected FET is Q1, the increased drain current raises the voltage drop across resistor R2, thereby lowering the drain voltage of Q1. This fall in voltage is transmitted through the voltage divider R5-R7 to the gate of Q2, and lowers the Q2 drain current, increasing the Q2 drain voltage. This higher drain voltage is transmitted back to the gate of Q1 through voltage divider R3-R1, and raises the Q1 drain current still further. This sequence of actions becomes cumulative in effect, until Q1 is fully conducting (drain current maximum) and Q2 cut off (drain current zero or a very low minimum). This then is one of the two stable states of the circuit: Q1 ON, Q2 OFF.

When a pulse is applied to the INPUT terminals so as to make the top terminal positive, diodes D1 and D2 transmit this pulse simultaneously to both drains. The pulse acts to increase drain current momentarily, but the drain current of Q1 is already maximum (saturated), so the pulse has no effect on this FET. Since Q2 is cut off, the pulse momentarily increases its drain current, increasing the voltage drop across R4 and lowering the Q2 drain voltage. This decrease in voltage is transmitted, through voltage divider R3-R1, to the gate of Q1, and this results in a lowering of the Q1 drain current. The action now proceeds rapidly in this new direction until finally Q1 is cut off and Q2 is fully conducting. This then is the second of the two stable states of the circuit: Q1 OFF, Q2 ON.

The next input pulse switches Q1 ON again, and switches Q2 OFF. Thus, one output pulse (Q2 ON) is delivered for every second input pulse. The alternate switching action is rapid.

While FET's of any type are usable in flip-flops, special switching FET's give highest-speed operation (the switching time of Type 2N4351, for example, is 270 ns).

## *4.12 CAPACITANCE RELAY*

Its very low gate/source capacitance fits the MOSFET very well for use in the oscillator section of a capacitance relay. This type of relay is well known as a proximity device, because of its industrial, domestic, and entertainment applications.

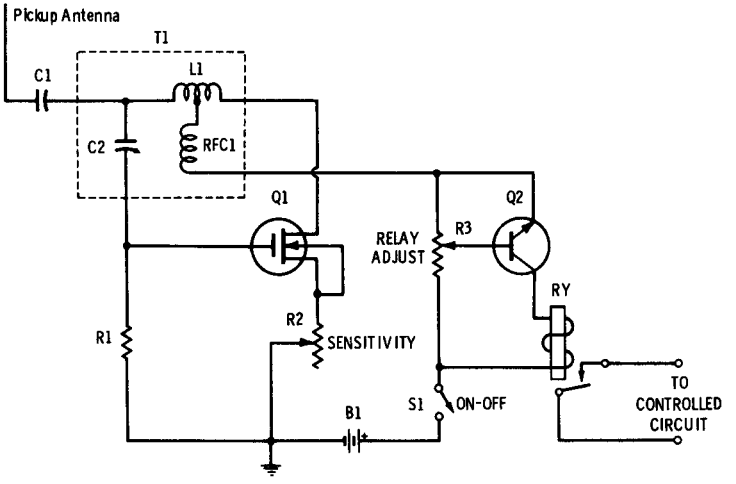


**Fig. 4-13. Capacitance relay.**

Fig. 4-13 shows a conventional circuit in which the usual vacuum-tube oscillator has been replaced with a MOSFET (Q1), and the usual gas-type relay tube has been replaced with an npn bipolar transistor (Q2). Assembly T1 is a commercial capacitance-relay "coil," which contains the tapped oscillator inductor L1, trimmer capacitor C2, and rf choke RFC1. The source resistor (R2) is a wirewound rheostat

for controlling oscillator sensitivity, and the drain resistor (R3) is a wirewound potentiometer for adjusting the pickup point of the relay. The relay itself (RY) is a single-pole single-throw, normally open, sensitive dc type (usually 1 or 2 mA).

When on-off switch S1 is closed, the Q1 circuit usually will oscillate if no conductive objects are near the pickup antenna and if rheostat R2 is set near the center of its resistance range. Also, relay RY will probably close, and R3 must be set to the point at which the relay just drops out. If the operator's hand then is held close to the antenna, his body capacitance will throw the circuit out of oscillation, the Q1 drain current will rise, and the voltage drop across R3 will increase. The base of Q2 will receive an increased dc voltage, and the relay will close. When the hand is withdrawn, the circuit resumes oscillation and the relay again drops out.

By adjustment of the sensitivity control rheostat (R2) and the oscillator trimmer capacitor (C2), the circuit may be made more or less sensitive, as desired, for operation by objects at some desired distance from the antenna.

Since transistors like Q1 are low-powered devices, a capacitance relay incorporating them is less apt to create radio interference than is one using tubes operated, as they are, at 100 V or higher.

# Index

N



O



P



R



S

values, the forward transconductance ($g_{fs}$) is calculated. The test setup shown in Fig. 2-2 is used.

(1) With meter M1, set B1 and B2 so that the operating point of the FET is in the center of the flat portion (saturation region) of the response curve. The curves plotted in Section 2-2 may be used to locate this point.
(2) With S1 thrown to position A, record the corresponding gate/source voltage as $V_1$ and the corresponding drain current (from meter M2) as $I_1$. From here on in the test, the voltage of B1 will be varied, but that of B2 will be held constant.
(3) Leave switch S1 in position A.
(4) Increase B1 for a voltage 0.5 V higher than $V_1$. Record as $V_2$. (Note that the drain current decreases.)
(5) Read the new current value from M2. Record as $I_2$.
(6) Decrease B1 for a voltage 0.5 V lower than $V_1$. Record as $V_3$. (Note that the drain current increases.)
(7) Read the new current value from M2. Record as $I_3$.
(8) Calculate the transconductance:

$$g_{fs} = 1000\,(I_3 - I_2)\,/\,(V_2 - V_3) \qquad (2\text{-}2)$$

where,
$g_{fs}$ is in $\mu$mho,
$I_2$ and $I_3$ are in mA,
$V_2$ and $V_3$ are in volts.

The battery and meter polarities shown in Fig. 2-2 are correct for an N-channel JFET and a depletion-type MOSFET. For a P-channel JFET or MOSFET, reverse B1, B2, M1, and M2. For a zero-biased MOSFET (depletion/enhancement mode), $V_1$ will be zero, $V_2 = +0.5$ V, and $V_3 = -0.5$ V.

## *2.7 STATIC TEST OF TRANSCONDUCTANCE*

The procedure outlined in the preceding section is a simulated dynamic test that approximates the ac measurement of transconductance. A simpler static test setup is shown in