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Boston, Massachusetts

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TABLE OF CONTENTS

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Papers in order of presentation
at RF Technology Expo 86

TABLE OF CONTENTS

PRACTICAL WIDEBAND RF POWER TRANSFORMERS, COMBINERS, AND SPLITTERS

by

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INTRODUCTION

This paper will deal with the practical aspects of designing and building wideband RF power transformers, combiners (or hybrids), and splitters. Emphasis will be on topology. A consistent approach to represent these transformers pictorially and schematically with equivalent circuits showing source and load connections will be developed to help provide an intuitive understanding of the devices. Laboratory test data comparing various designs and topologies is included.

Modern solid state HF power amplifiers are required to operate over increasingly wider bandwidths and at higher power levels for applications in communications as well as electronic countermeasures. Wideband RF power transformers are required for coupling into and out of the solid state devices. The conventional or so-called "wire-wound" transformer and two topologies of the transmission line transformer (conventional and equal delay) are presented.

A wideband RF power combiner (or hybrid) is required to achieve output levels above the capabilities of a single solid state amplifier stage. The RF outputs of two or more identical amplifier modules can be combined to reach these higher powers. Design examples of in-phase, 180-degree, and quadrature combiners are detailed. Two basic topologies for in-phase and 180-degree combiners are presented.

A wideband RF power splitter (or divider) is simply a combiner or hybrid used in reverse. The splitter topology is the same as a combiner, however splitters are usually operated at lower power levels. The discussion centers around combiners but is equally applicable to power splitter applications.

TRANSFORMERS

The bandwidth of rf transformers does not refer to the usual -3 dB points since in power applications this represents an unacceptable loss. Typical HF amplifier designs require operation from 2 to 30 MHz and sometimes lower to 1.6 MHz. The transformer losses must be as low as possible over this operational bandwidth. Transformer losses translate to heat that must be removed as well as extra power that must be supplied by the transistors (at the collector/drain efficiency) and ultimately by the power supply (at its conversion efficiency). A few tenths of a dB of unnecessary loss in output

transformers or combiners can mean significant increases in primary power consumption.

New RF power FET devices have operational bandwidths of 1 to 175 MHz making possible extended range amplifiers covering HF and the lower VHF frequencies. Transformer designs covering over six octaves of bandwidth are required.

A wideband RF power transformer performs one or more of any combination of three basic functions:

(a) Impedance transformation

(b) Balanced to unbalanced transformation

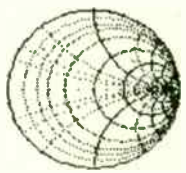
(c) Phase inversion

Transformation of a secondary load to a desired load impedance at the primary of the transformer is the most common function. RF transformers are often referred to by their impedance transformation ratio rather than primary to secondary turns ratio. The former is simply the turns ratio squared. In this application, we are most often interested in manipulating impedances rather than voltages or currents with the transformers. Balanced-to-unbalanced transformers, commonly termed "Baluns" are extremely useful in wideband amplifier designs. A single-ended load can be driven by a push-pull (balanced) source or vice-versa by using a balun transformer. A wideband transformer can also perform a phase reversal from primary to secondary by proper winding connections.

Transformer connections between a source and a load may be either balanced or unbalanced. Additionally, the balanced source or load may be either entirely floating or with center grounded such as two single ended sources phased 180-degrees apart or a load resistor with grounded center tap. The distinction between "balanced, floating" and "balanced, center grounded" may seem unimportant for wideband transformer design, but it is not. A proposed balun transformer equivalent circuit with source and load connected should be drawn showing the magnetization current path.

Figure 1 (a) is an example of a simple 1:1 balun with a floating balanced load. The magnetization current, i_m, flows through the load resistor as shown. Figure 1 (b) illustrates what happens to the magnetization current path if the balanced load is changed to a balanced, center tap grounded load. The magnetization current flows through only one winding and only one-half of the load resistance. This causes undesirable phase and amplitude imbalance in the balun restricting the bandwidth. The balance can be restored by using a third or tertiary winding, as shown in figure 1 (c), to shunt the magnetization current around the load. This illustrates the necessity of considering the type of source and load connections when selecting wideband transformer topologies.

RF TECHNOLOGY EXPO 86
INTERACTIVE COMPUTER AIDED GRAPHICS APPLIED TO RF CIRCUIT DESIGN



ALAN VICTOR

Introduction

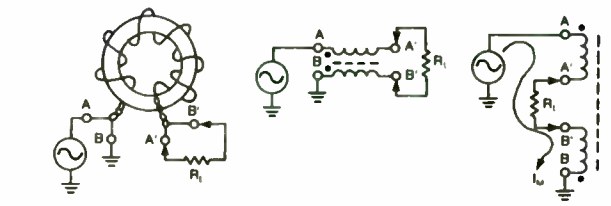
This paper presents several programs which utilize the interactive graphics capability of a desk top computer to aid the RF circuit design engineer. High frequency amplifier design of class A power amplifiers, low noise design and stability analysis are discussed. Computer aided graphics is demonstrated which assist the designer in the appropiate tradeoffs. An interactive routine which handles the communications receiver cascade of noise and distortion is presented along with a "what-if-scenario" applied to a typical receiver system. Finally, a program which computerizes the Smith Chart and provides aid in broadband impedance matching is demonstrated.

The routines were developed on the Hewlett-Packard series 200 personal computer which features an excellent graphics oriented BASIC language and the capability of interactive control of program variables while the program is operating. These features are not necessarily limited to the series 200 computers of HP. In fact many of todays personal computers have excellent high resolution graphics and various forms of interactive control (i.e. light pens, paddles, joystick control and live keyboard). The routines to be discussed will concentrate on the following specific areas:

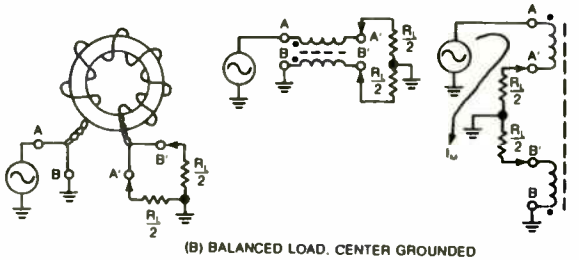
1. Class A power amplifier design
2. Small signal amplifier stability
3. Noise figure/ gain/ and VSWR optimization of amplifiers
4. Smith Chart and interactive graphics aid in broadband matching
5. Noise figure/ gain/ distortion of linear cascaded networks. Interaction aids in the optimization of a given cascade.

Class A Power Amplifier Design

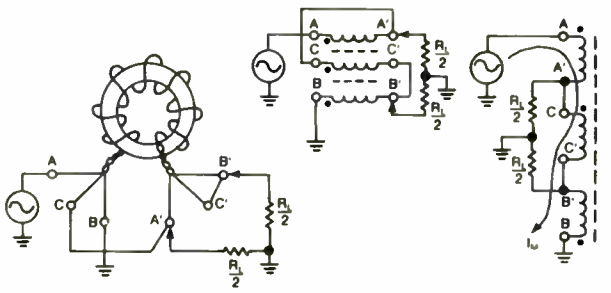
Numerous occasions arise for the need of a small signal linear power amplifier. Normally the design criteria if the device is unconditionally stable is to provide for simultaneous conjugate match at the input and output. If low noise performance is desired than the designer seeks to find the optimum source reflection coefficient and then conjugate match the output and maximize the amplifier transducer gain. At the same time the designer strives to minimize the input VSWR [1]. We will discuss these criteria in more detail; but for now the main interest is to provide maximum output power to the load while operating the device Class A. A good design approach to this problem was presented by Richter and



(A) BALANCED LOAD, FLOATING



(B) BALANCED LOAD, CENTER GROUNDED



(C) BALANCED LOAD, CENTER GROUNDED WITH TERTIARY WINDING (C-C')

FIGURE 1. 1:1 TRANSMISSION LINE BALUN TRANSFORMERS

The nine possible transformer connections are given below:

SOURCE	LOAD
Unbalanced	Unbalanced
Unbalanced	Balanced, floating
Unbalanced	Balanced, center grounded
Balanced, floating	Unbalanced
Balanced, floating	Balanced, floating
Balanced, floating	Balanced, center grounded
Balanced, center grounded	Unbalanced
Balanced, center grounded	Balanced, floating
Balanced, center grounded	Balanced, center grounded

Wideband RF transformers and combiners typically use a magnetic core. The magnetic cores used in wideband RF transformers are available in a wide variety of shapes and sizes. Balun core, toroidal, sleeves, tubes, beads, and cup cores are the common names for the various shapes. The earliest material used was powdered iron followed by modern ferrites. Ferrite is composed of iron oxide in combination with various proportions of oxides of manganese, magnesiun, nickel, and zinc. In general the ferrites composed of iron, nickel, and zinc are applicable for the HF/VHF frequencies. Various mixes of ferrites are available. A high permeability and moderately low loss material is used for HF/VHF power transformers. Operational flux densities must be kept well within the linear portion of the B-H curve of the material. The area inside the

and again by D. Rosemarin and M. Chorev [2], [3]. Their technique is based on choosing the optimum load conductance for a device operating class A at a given collector voltage and collector current. If the device is not to limit on voltage swing or peak output current then the optimum load conductance is given by

$$Glopt = Icq(ma.)/Vcc(volts).$$

If the load conductance is less than the Glopt then the maximum class A output power is given by

$$Pl(mw) = (Vcc^2/2)\ Gl \quad \text{(current limited)}$$

and if the load conductance is greater then Gopt then

$$Pl(mw) = (Icc^2/2\ Gl) \quad \text{(voltage limited)}.$$

Power loci are plotted graphically on the Smith chart as constant conductance contours. The center center and radius as measured from the center of the unit circle chart are given by

$$r = Gln/(1+Gln) \quad \text{and} \quad \rho = 1/(1+Gln)$$

where Gln is the normalized load conductance. At the voltage and current specified the device S-parameters are measured. Given the S-parameters, constant output gain contours are calculated and also plotted on the Smith Chart as circular loci [1]. With the plot of power gain circles and power output circles displayed together it is now possible to visually see the trade-off between maximizing the power output and power gain. It is not uncommon to lose several dB of power output by simultaneously conjugate matching the device. Instead, maximizing the power output may only result in a few tenths of a dB loss in power gain. In [2] the authors show that the location of the optimum output load reflection coefficient is a susceptance contour on the unit circle Smith chart. This contour is the locus of tangency of optimum power output and all the respective gain contours and is shown in Figure (1).

With all this information shown graphically it is now possible to tune the load reflection coefficient and observe the tradeoff in power output, power gain, and potential input and output VSWR. This is achieved in the computer program by allowing the forced load reflection coefficient (* L) to be "tuned" interactively and observing

the location of the required source reflection coefficient conjugate matched input (* S). At the same time the actual load reflection coefficient (* L) for conjugate matched input is displayed thus allowing the designer to minimize the output VSWR. Figures (2) and (3) demonstrate that if the device were conjugate matched the output power would be reduced by 4.8 db from the maximum. On the other hand maximizing the power output only reduces the power gain by 1.1 db, clearly a good tradeoff!

Small Signal Amplifier Stability

The load and source reflection coefficient must be carefully chosen if the device is conditionally stable. Inspection of the Linvill stability factor C, [4] or the Rollet stability factor K, [5] aid in determining the probability of oscillation. Both the Linvill and Rollet stability factors are obtained from the measured Y parameters or S parameters respectfully. In addition to checking the value of C which must be less then 1 to ensure stability, the values of y11 and y22 must both be positive and real for all possible values of real source and load combinations. Using S parameters and the K factor a similiar set of criteria exist. Many individuals look at the K factor alone and this is a necessary condition for stability but not sufficent [6]. The interactive graphics of the next routine demonstrate this vividly and Figures (4) through (6) show the results. In summary a good criterion for unconditional stability is given in [1,6] and repeated here for reference.

1. $K>1$ and $|\Delta| < 1$ where $|\Delta| = |s11 \cdot s22 - s12 \cdot s21|$ or
2. $K>1$ and $B1 = 1 + |s11|^2 - |s22|^2 - |\Delta|^2 > 0$

The computer aided design routines presented here illustrate the stable regions of the Smith chart by circular regions. Depending on the location of these regions the inside of the circular regions may or may not provide a stable load or source reflection coefficient. Consider the previous figures (4,5,6). Interactive control of the load reflection coefficient (* L) allows you to position the load on either a constant VSWR circle or on a constant gain circle. As long as the forced load reflection coefficient remains inside the output stable region circle the source reflection coefficient (* S) and the actual load reflection coefficient (* L) remain positive and real. As the forced load reflection coefficient approaches the edge of the output stable region the source reflection coefficient approaches the edge of the unit circle

B-H curve represents the relative loss, therefore the narrow curves are preferred for low loss designs. Detailed information is available from the various ferrite manufacturers.

Core losses and winding dielectric losses heat the core. The core temperature must be held well below the Curie temperature of the ferrite, otherwise the magnetic properties of the ferrite will be permanently altered. Operation near the Curie temperature is not recommended as some materials can go into thermal runaway. The high temperature increases the core loss which in turn further increases the core temperature until the core is ruined.

CONVENTIONAL OR "WIRE-WOUND TRANSFORMERS"

The conventional broadband RF transformer is characterized by a power transfer from the primary to secondary windings via magnetic coupling through the ferrite core. The transmission line transformer, by contrast, is characterized by the use of a transmission line of characteristic impedance, Z_o, and a ferrite core. The core suppresses common mode or non-transmission line currents which would otherwise flow due to the transmission line interconnections. A core wound with wire may or may not be a conventional transformer, depending upon how the source and load are connected. Figure 2 illustrates this distinction.

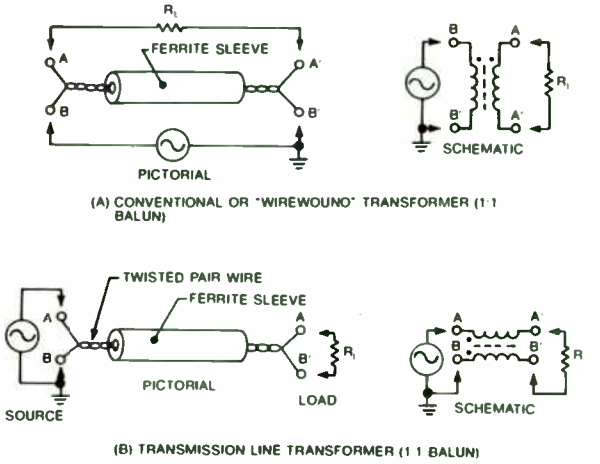


FIGURE 2 COMPARISON OF CONVENTIONAL AND TRANSMISSION LINE TRANSFORMERS

In general, the conventional transformer is inferior to the transmission line transformer for the combination of high power capability, low loss, and wide bandwidth. The conventional transformer can be constructed for a wider range of impedance transformation ratios than the transmission line type. Some ratios will have wider bandwidths than others due to the number of turns to achieve the desired turns ratio. There are no fractional turns. If the wire or line passes through the core, it is one turn.

Smith chart. A movement of the load reflection around the outside of the stable circle will force the source reflection coefficient to trace out the complete outside edge of the Smith chart. Further movement of the load reflection coefficient outside of the stable region will force the source reflection coefficient to move outside the Smith Chart (Γ>1 implies negative real resistive component) and could produce amplifier instability. If the combination of forced load reflection coefficient and actual load reflection coefficient is still net positive and real then no oscillation will be present. On the other hand if this is not the case then both the input and output ports of the device are negative real and oscillation will occur. The interactive graphic nature of the program allows assessment of the amplifier stability as the load (or the source) reflection coefficient is varied.

Low Noise Amplifier Design

Device noise figure is a function of the source reflection coefficient. Minimization of noise figure and maximizing the amplifier gain is the desired design goal. Adler [7] defines a noise measure and Fukui [8] applies this concept or technique to aid in optimizing a low noise amplifier design. Interactive graphics provides another method for observing the tradeoffs involved. A plot of amplifier constant gain contours along with noise contours allows a visual tradeoff to be made [9].

Normally the approach taken is to seek the source reflection coefficient which minimizes the noise figure while maximizing the transistor transducer power gain. This results in minimizing the noise measure of the device. Unfortunately if the source reflection coefficient for minimum noise figure differs from the actual device input impedance then the input VSWR could suffer. One approach to this problem is to apply feedback around the device in an attempt to force the maximum device gain to coincide with the minimum noise figure point [10,11]. Another approach is to adjust the load reflection coefficent interactively and observe the source reflection coefficient movement. What we seek is a forced load reflection coefficient value which yields the maximum available gain and at the same time causes the source reflection coefficient to minimize the device noise figure. At the same time the actual load reflection coefficient should idealy be close to the forced load reflection coefficient in order to minimize the output VSWR. This approach has the benefit of minimizing the input VSWR and therefore preventing input mismatch loss from further

Interactive Computer Aided Graphics Applied to RF Circuit Design
RF Technology Expo 86

degerading the system noise figure. Figures (7) and (8) illustrates thr results for one device.

Computerizing the Smith Chart

The Smith chart is an indespensible graphical tool which solves a number of RF design related problems. The interactive graphics of a personal computer further enhances this tool and provides for additional insight into your design problem. A major application is in impedance matching, narrow band as well as broadband. A number of articles have addressed this application including computer oriented routines [12,13]. The routine demonstrated here provides the solution to the ladder matching network by solving the transmission matrix or chain matrix of each element in the ladder. The chain matrix of any of 12 different element types are included as subroutines. Both parallel and series forms of R,L,C, transmission lines,tuned circuits and ideal transformers are included. The benefits of interactive tuning are quite evident in this application, which allows the designer to literally tweak element values in the matching network with the Smith chart as the graphic backround. Thus the designer can optimize VSWR and bandwidth. In addition the tune feature allows a feeling for element sensitivity as well as which components would lend themselves to optimization in matching say a broadband amplifier. As an example in applying this routine we demonstrate the impedance matching technique presented by Thomas [14,15] in his text. Figure (9) illustrates the Smith chart divided into 4 high Q regions. Depending on the region we wish to match to the center of the chart an appropriate network topology is selected. Figure (10) shows the tuning procedure as each element is "tweaked" and the final VSWR is reduced from 30:1 to less than 3:1.

The sensitivity of maintaining a low VSWR in a broadband match can also be investigated through interactive graphing and the Smith chart. The methodology for synthesizing in closed form optimum broadband matching networks is discussed in Chen's text and in Apel's work [16,17]. Figure (11) shows the results of applying [17] to the match of a GaAs FET and then varying one of the elements in the ladder match. The extent to which this element is changed before a VSWR of 2:1 or greater is exceeded becomes quickly apparent.

Figure 3 is a conventional transformer that finds wide usage at low impedances (3 to 20 ohms). The core is commonly referred to as a balun core, yet the transformer may or may not be connected to perform as a balun. Metal sleeves of copper or brass are inserted into the core and connected together at one end to form a primary winding. Connections to the circuit are made at each of the two sleeves at the opposite end. Two pieces of copper clad G-10 circuit board work nicely at each end. The secondary winding is constructed by winding the required turns of insulated wire through the primary tubes.

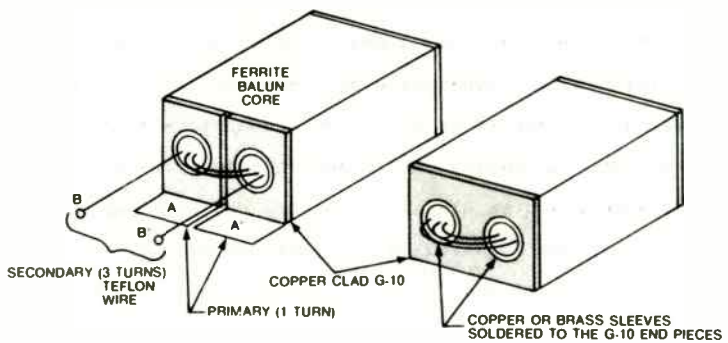


FIGURE 3. EXAMPLE OF A 1:9 IMPEDANCE RATIO CONVENTIONAL TRANSFORMER

One of the factors limiting the high frequency response of the transformer is leakage inductance. Leakage inductance is due to any flux lines that do not link the primary and the secondary. To minimize the leakage inductance, the primary copper tubes should fit quite close in the core holes. They should not be so tight that thermal expansion will cause the core to break. The lead inductances of the primary and secondary windings from the point they exit the core to the circuit connection will also limit performance at the high frequency end, especially on low impedance applications. Shunt capacitance on either the primary or secondary or both will compensate the leakage reactance and extend the useful high frequency limit.

TRANSMISSION LINE TRANSFORMERS

The simplest transmission line transformer is a quarter-wavelength line whose characteristic impedance, Z_C, is chosen to give the correct impedance transformation. This relationship is illustrated in figure 4. Note that this transformer is a narrowband device valid only at frequencies for which the line is odd multiples of a quarter wavelength. The transformation ratio is given by the square of the ratio of the line impedance to the load connected to the line.

Noise Figure, Gain, and Distortion of Linear Cascaded Networks

Communication systems require the proper distribution of gain, noise, and linearity in order to provide the maximum dynamic range. This requires a proper tradeoff in each stage for noise figure, gain, and maximum signal handling ability before distortion sets in. One method for the characterization of a communucations receiver distortion is to use the intercept method [18]. This figure of merit coupled with a stage-by-stage description of noise figure, gain, and selectivity provides a complete description of the receiver performance [19,20]. A graphic presentation of each stage contribution to the total noise figure or distortion aids the designer in seeing which stage in the cascade is the most offensive. Then interactive tuning of each stage gain, noise figure or third order input intercept allows optimization as well as a sensitivity analysis of the receiving system dynamic range. Figure (12) shows a 9 stage cascade including RF amplifier, mixers and crystal filters. Figure (13) is a plot of the individual stage noise figure contribution and Figure (14) is a plot of intermodulation distortion contributions. At a glance the designer can see which stages are causing the distortion level to fall below a specified goal. By adjusting or tuning each stage an optimum gain, noise figure distribution will result. Any increase in gain, for example stage 3, results in improved sensitivity but at the expense of degraded third order distortion due to larger input signal levels present at the earlier stages. A decrease in front-end gain in stage 3 lowers the third order distortion, but degrades the system noise figure and sensitivity. Thus, a lower system dynamic range occurs.

Conclusions

The RF design engineer will benefit from the use of todays personal computers, especially those which provide real-time interactive graphic solutions. This allows the engineer to seek the desired response and investigate the "what-if-secenario". By providing this sort of "tune" function the designer can not only optimize for a given network response but also gain a feeling for the sensitivity of his design.

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RF Technology Expo 86

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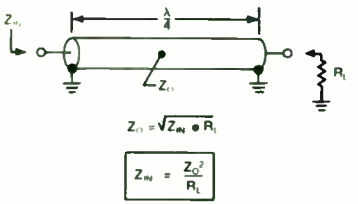

FIGURE 4 SIMPLE QUARTER WAVE TRANSMISSION LINE TRANSFORMER

If a ferrite sleeve is added to the transmission line (see figure 5), common mode currents (currents flowing in both transmission line conductors in phase and in the same direction) are suppressed and the load may be balanced and floating above ground. The line can now be any length with characteristic impedance equal to the balanced load impedance. The result is a 1:1 balun. Low frequency operation is limited by the amount of impedance offered to common mode currents. A good rule-of-thumb requires the impedance presented to common mode currents be not less than five times the load impedance. The line length limits the high frequency response of transmission line transformers.

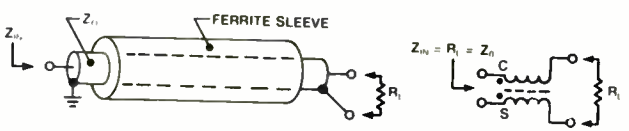

FIGURE 5 1:1 TRANSMISSION LINE BALUN

If the ferrite loaded length of transmission line in figure 5 is folded back so that the two ends may be interconnected, a 1:4 impedance transformer is formed. A load resistance, R_L, connected as shown in figure 6 is reflected to the input of the transformer as $R_L/4$. The line Z_O should be equal to the geometric mean of R_L and Z_{in} for maximum bandwidth. The line length must be as short as possible for extended high frequency operation. The practical high frequency limit for this type of transformer is reached when the line length approaches 1/8 wavelength and appreciable phase error difference occurs at the interconnection of the lines.

A 1:4 transmission line balun transformer may be constructed as shown in figure 7. Two cores are required and may be either balun cores (as shown) or toroids or sleeve cores. The transmission line Z_O should be the geometric mean of the input and load impedances. This transformer may also be used for balanced-to-balanced source and load connections. Transmission line baluns for 1:9 and 1:16 impedance ratios are constructed similarly as shown in figures 8 and 9. The limitation of squared integer transformation ratios is the biggest disadvantage of this type of transmission line transformer. The availability of coaxial cable in a variety of impedances is another limitation. 50 and 75-ohm cables are by far the most common but impedances of 25, 35, 60, 95, and 125-ohms are available.

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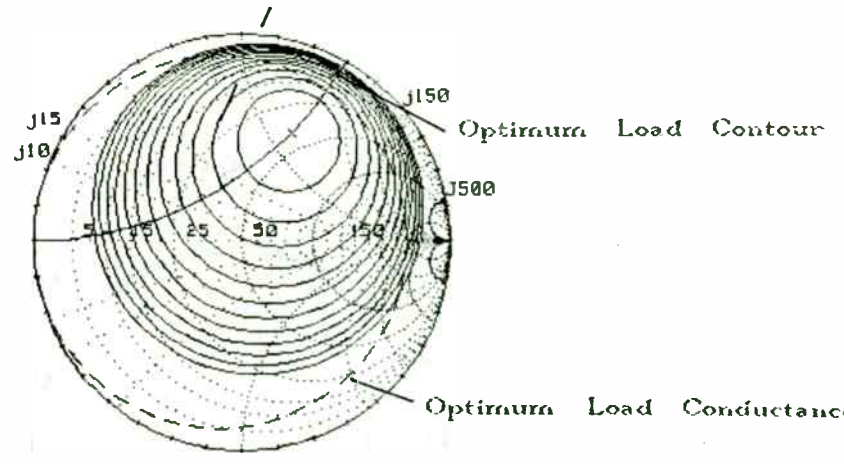
FIG 1 Power Gain Contours



S-Parameter, Class -A- Power Amplifier Design
Version 1.0
4/29/85

Input Scattering parameter data
S11= .5464 (-81
S12= .0708 (33
S21= 2.8183 (119
S22= .4651 (-48

Stability factor= 1.42875416389
Maximum stable gain= 12.1092721374 dB
Load Reflection Coefficent= .585784779614 (65.1388734015
Source Reflection Coefficent= .648125859217 (92.5465324989

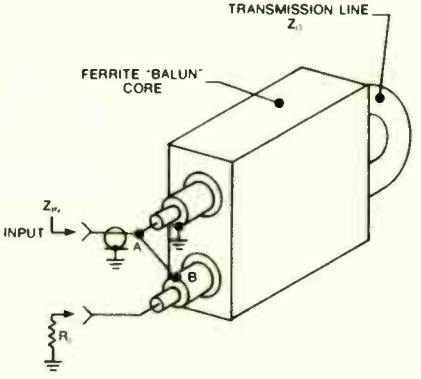
Constant Output Transducer Gain Circles

1.11	.47	.965 (60.17	.783 (102.3	6.35	-5.76
2.21	.94	.932 (60.23	.766 (101.6	8.69	-3.42
3.32	1.41	.9 (60.33	.75 (100.9	9.85	-2.26
4.43	1.88	.869 (60.48	.736 (100.1	10.6	-1.56
5.53	2.35	.839 (60.66	.723 (99.39	11	-1.09
4.61	2.82	.81 (60.89	.712 (98.65	11.3	-.77
3.95	3.29	.782 (61.17	.702 (97.92	11.6	-.54
3.46	3.76	.755 (61.48	.693 (97.2	11.7	-.372
3.07	4.23	.729 (61.84	.684 (96.5	11.9	-.249
2.77	4.7	.703 (62.25	.677 (95.82	11.9	-.159
2.52	5.17	.679 (62.7	.67 (95.15	12	-.0954
2.31	5.64	.656 (63.19	.664 (94.51	12.1	-.0512
2.13	6.11	.633 (63.74	.659 (93.88	12.1	-.0226

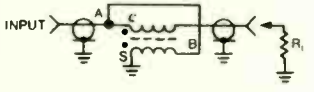
Output Gain Circles relative (to S21^2) 9 dB

Gi(dB)	Center Location	Radius	Operating Power Gain (dB)					
3.11	.586 (65.1	9.29E-9	12.1	1.98	6.58	.611 (64.34	.654 (93.27	12.1	-.00638
2.61	.534 (65.1	.246	11.6	1.84	7.05	.59 (64.99	.649 (92.68	12.1	-.000203
2.11	.486 (65.1	.348	11.1	1.73	7.52	.57 (65.68	.645 (92.11	12.1	-.00222
1.61	.442 (65.1	.426	10.6	1.63	7.99	.551 (66.44	.641 (91.56	12.1	-.011
1.11	.401 (65.1	.491	10.1	1.54	8.46	.532 (67.25	.638 (91.02	12.1	-.0253
.61	.363 (65.1	.547	9.61	1.46	8.93	.514 (68.11	.635 (90.51	12.1	-.0443
.11	.328 (65.1	.596	9.11	1.38	9.4	.497 (69.03	.632 (90.01	12	-.0672
-.39	.296 (65.1	.639	8.61	1.32	9.87	.48 (70.02	.629 (89.53	12	-.0933
-.89	.267 (65.1	.677	8.11	1.26	10.3	.464 (71.06	.627 (89.07	12	-.122
-1.39	.241 (65.1	.711	7.61	1.2	10.8	.449 (72.17	.624 (88.62	12	-.155
-1.89	.217 (65.1	.742	7.11	1.15	11.3	.435 (73.34	.622 (88.19	11.9	-.187
-2.39	.195 (65.1	.769	6.61	1.11	11.8	.421 (74.58	.621 (87.78	11.9	-.221
-2.89	.175 (65.1	.793	6.11						

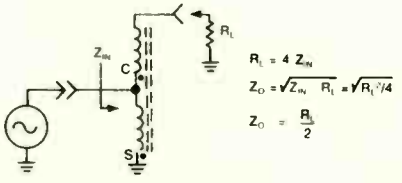
POUT mW.	GL moho	GLopt	GSopt	Power Gain dB	Delta dB Max
1.11	.47	.965 (60.17	.783 (102.3	6.35	-5.76



(A) PICTORIAL VIEW

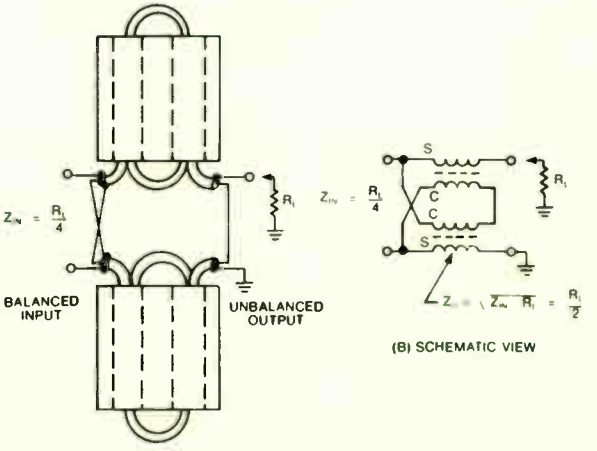


(B) SCHEMATIC



(C) EQUIVALENT CIRCUIT

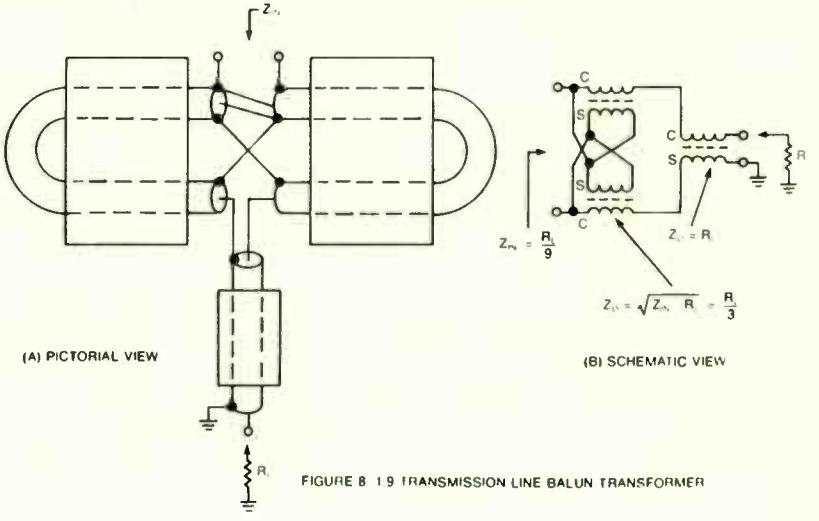
FIGURE 6. TRANSMISSION LINE TRANSFORMER; 4:1 UNBALANCED-TO-UNBALANCED



(A) PICTORIAL VIEW

(B) SCHEMATIC VIEW

FIGURE 7. 1:4 TRANSMISSION LINE BALUN TRANFORMER



(A) PICTORIAL VIEW

(B) SCHEMATIC VIEW

FIGURE 8. 1:9 TRANSMISSION LINE BALUN TRANSFORMER

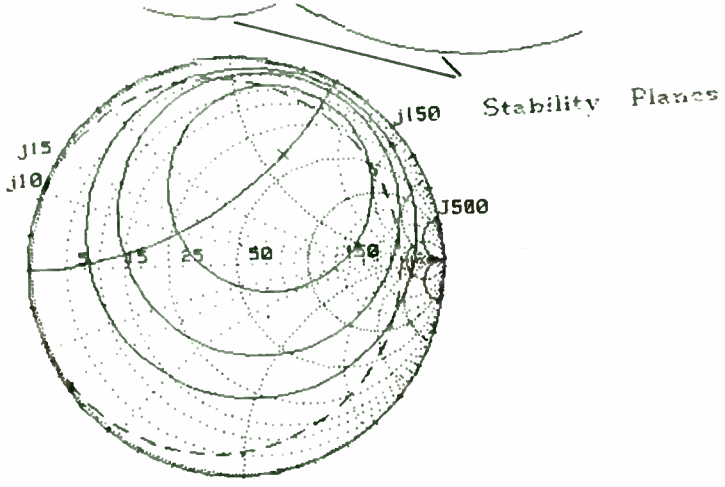


FIG2

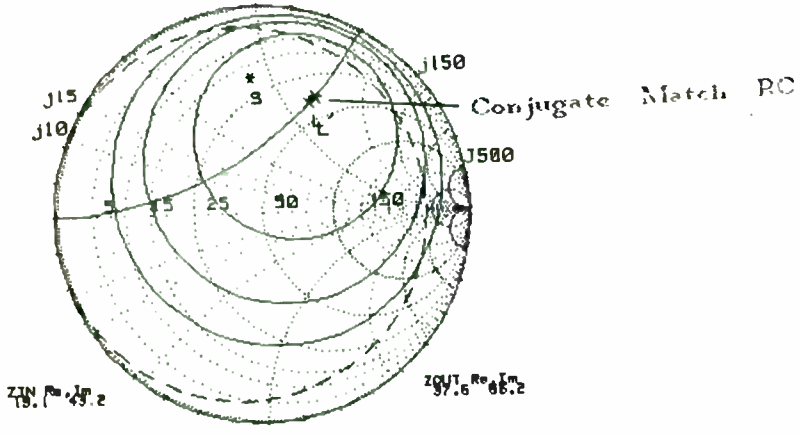


FIG 3

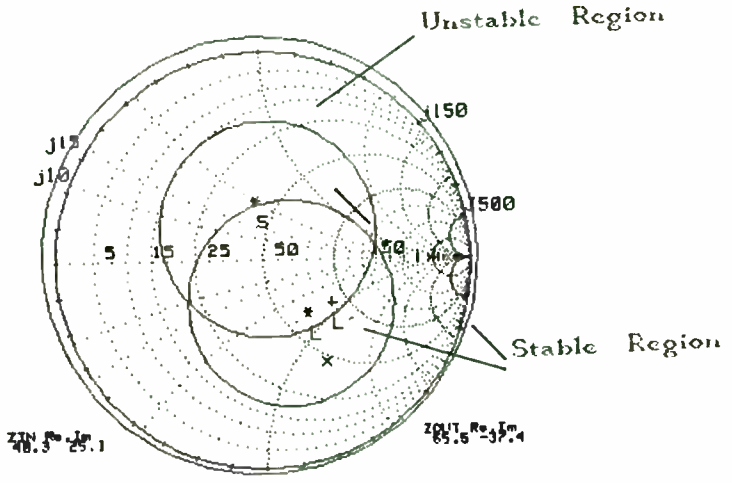


FIG 4

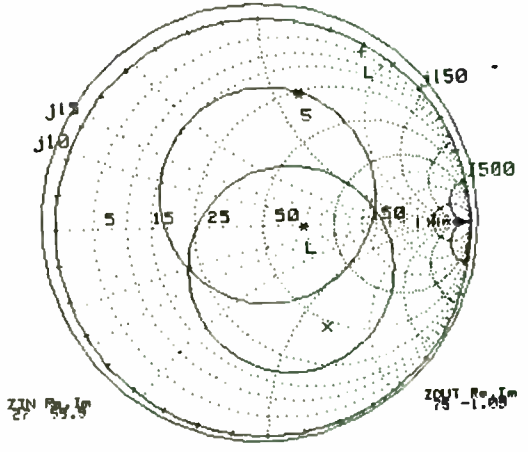
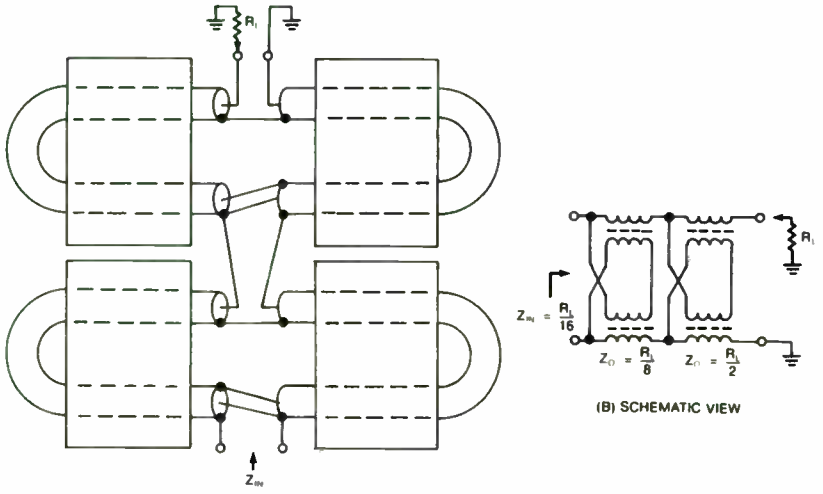


FIG 5



(A) PICTORIAL VIEW

(B) SCHEMATIC VIEW

FIGURE 9. 1:16 TRANSMISSION LINE BALUN TRANSFORMER

Several techniques to achieve nonstandard impedance lines include simply parallel connecting two or more lines. For example, two parallel 50-ohm lines provide an effective 25-ohm line. The parallel lines do not have to be the same impedance either. Bifilar or twisted enameled wire can easily be constructed for odd characteristic impedances also. The impedance depends upon the wire diameter, insulation dielectric, spacing, and number of twists per unit length. Multiples of even numbers of wire may be twisted together and then parallel connected to achieve low characteristic impedances. The characteristic impedance of experimentally constructed bifilar or twisted pair transmission lines may be determined by measuring the reactance of an open circuit, 1/8-wavelength, sample. The magnitude of the reactance is equal to the line impedance at the frequency for which the line is 45-degrees in electrical length. Remember to account for the velocity of propagation when determining the frequency of 1/8 wavelength.

Micro-strip transmission lines on printed circuit boards is another technique for achieving virtually any desired line impedance. Mechanical problems with the strip lines in ferrite cores may be more difficult but interconnections with the amplifier circuit may be improved.

The bandwidth degradation experienced by not using the correct value of line impedance may be acceptable in some applications. Figure 10 is a comparison of two identical 1:4 balun transformers; one wound with the proper 25-ohm line, the other wound with 50-ohm line. The measurement was made by connecting two identical transformers back-to-back to provide matched 50-ohm impedance ports to interface with the network analyzer. The indicated loss of one transformer is half of the measured value. This technique is valuable for evaluating various transformer designs and initially chooseing values of compensation capacitors for leakage reactance.

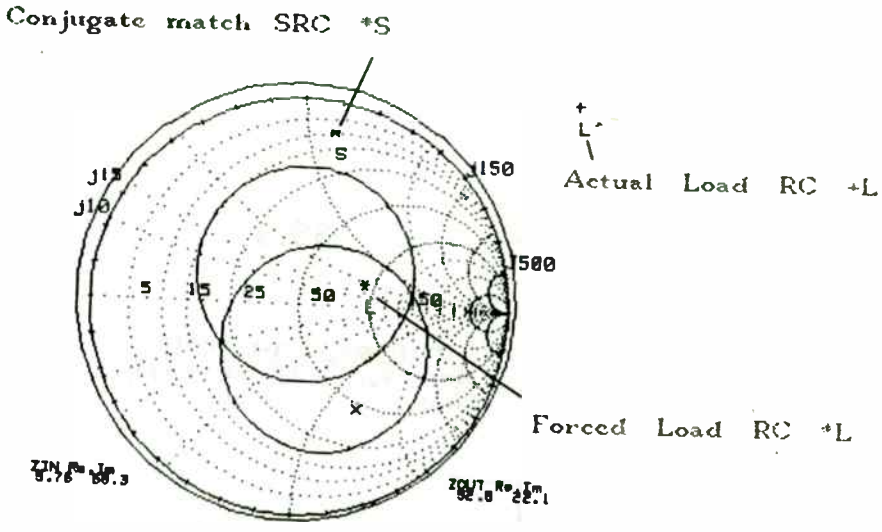


FIG 6

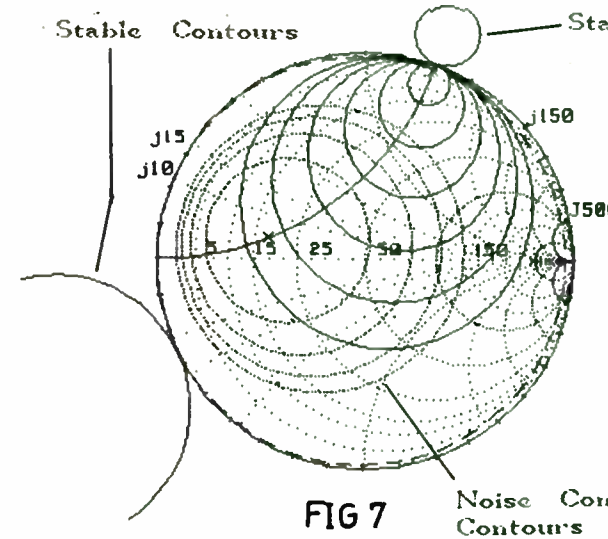


FIG 7 Noise Contours overlay power Contours

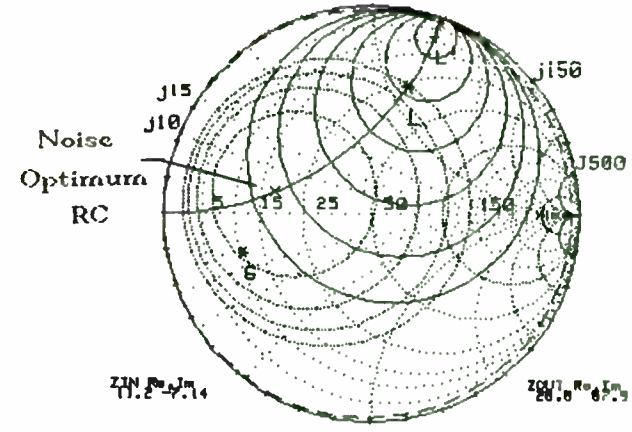


FIG 8 Constant Noise Contours

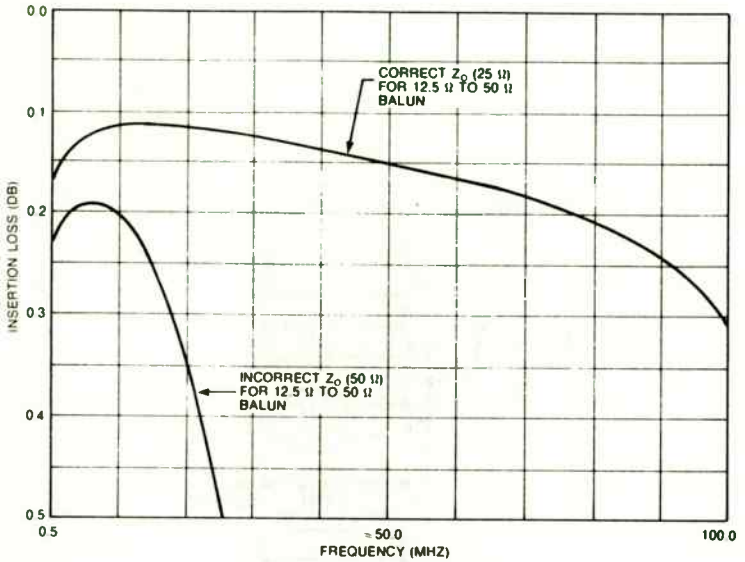


FIGURE 10. COMPARISON OF EFFECT OF Z_O ON 1:4 BALUN TRANSFORMER

As pointed out earlier, the 1:4 transmission line transformers' high frequency response is limited when appreciable phase error is introduced at the interconnection point a-b shown in figure 11. If the connection a-b were made with a transmission line of equal impedance and length as the ferrite loaded line, the phase difference between input and output is eliminated. The transformer topology remains the same, except the a-b connection has the same phase delay as the main transformer line. For this reason this subclass of transmission line transformers are called "Equal Delay Transmission Line Transformers". The transformer input and output connections can be physically separated which is advantageous in some applications.

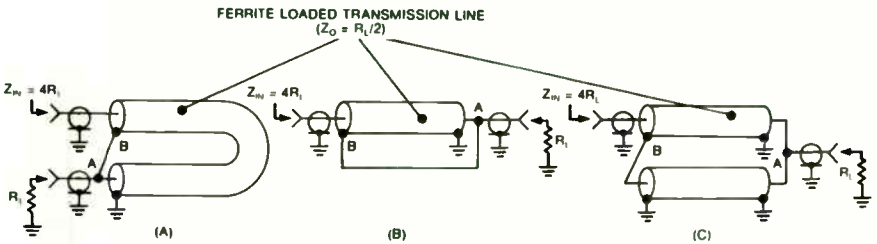
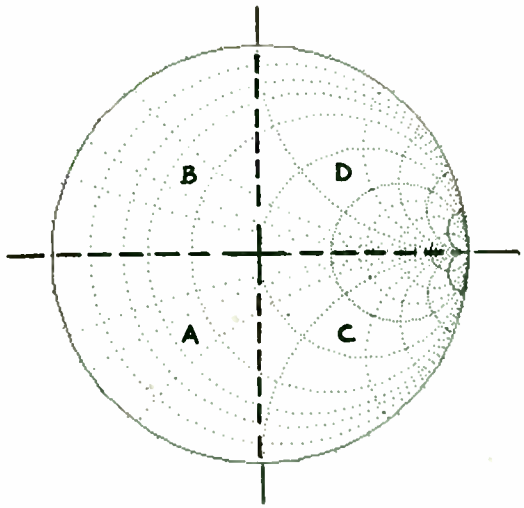
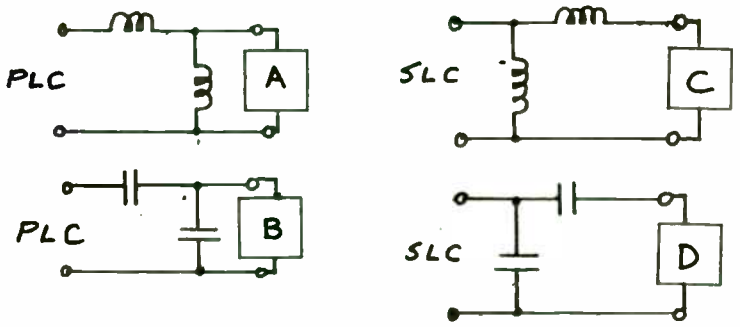


FIGURE 11. DERIVATION OF THE EQUAL DELAY TRANSFORMER

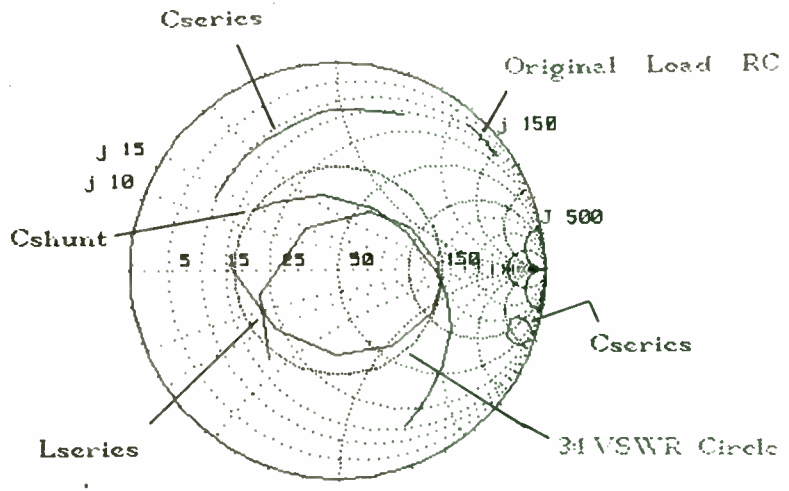
Figure 12 (a) is the usual pictorial and schematic representation of a 1:4 equal delay transformer. If a third line is stacked on the 1:4 design, a 1:9 impedance transformer results. In like manner, four lines produce a 1:16 transformer and so on. Figure 12 (b) and (c) illustrates these ratios. For comparison, if one unit of ferrite is required on the 1:4 transformer for a given bandwidth, then two units will be required for the third line on the 1:9 transformer. In like manner, the fourth line requires three units of ferrite for the same bandwidth. Notice that these designs are all unbalanced-to-unbalanced transformers. Suppose we add ferrite to the bottom line on the 1:4 transformer. Now we can lift the grounds on the parallel connected end (still keeping the shields





Four Element Matching Networks for Maximum Bandwidth Potential

FIG9



Frequency (Mhz)	Reflection Coefficent	Load VSWR	R1	I1
50	.5392 (-129.1	3.34	17.99	-21.23
51	.3994 (-163.6	2.33	21.82	-5.848
52	.2557 (126.5	1.687	34.11	15
53	.3199 (60.67	1.941	56.89	35.35
54	.4079 (30.8	2.378	89.5	44.85
55	.4815 (3.099	2.857	142.1	9.633
56	.498 (-9.617	2.984	141.3	-31.27
57	.4922 (-24.69	2.938	108.9	-59.1
58	.4429 (-54.83	2.59	58.6	-52.79
59	.4047 (-91.3	2.359	35.37	-34.22
60	.4133 (-137.5	2.409	23.29	-15.68
61	.5117 (178.6	3.096	16.15	.5387

Impedance Matching Network Starting From the Lead End:

Component Description	Component Value
CAPACITOR_SERIES	32 pF.
CAPACITOR_SHUNT	68 pF.
CAPACITOR_SERIES	11 pF.
INDUCTOR_SERIES	810 nH.

FIG 10

connected) and connect a balanced, floating load between the center conductors and the shields to form a 1:4 balun. The stray capacitance to ground can be balanced better by interconnecting the center conductor of one coax to the shield of the other coax. The result is the balun transformer described earlier in figure 7.

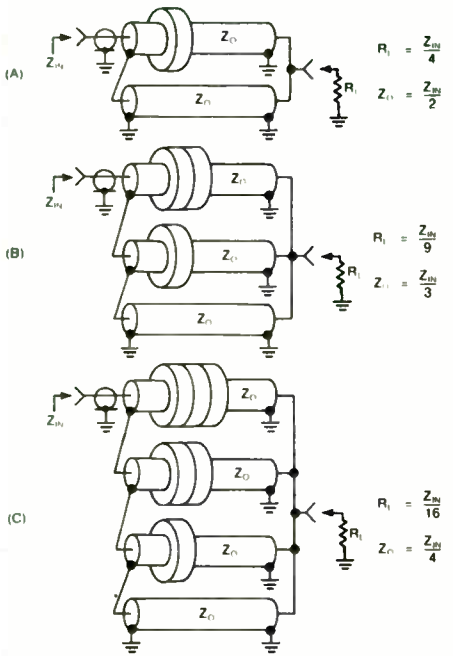


FIGURE 12 EQUAL DELAY TRANSFORMER CONFIGURATIONS

How much improvement in bandwidth does the equal delay transformer give compared to the conventional transmission line transformer? Figure 13 is a plot of insertion loss versus frequency for the two types constructed on identical cores. Again, the test consisted of measuring two identical transformers connected back-to-back, so the actual loss for one transformer is one-half the measured value.

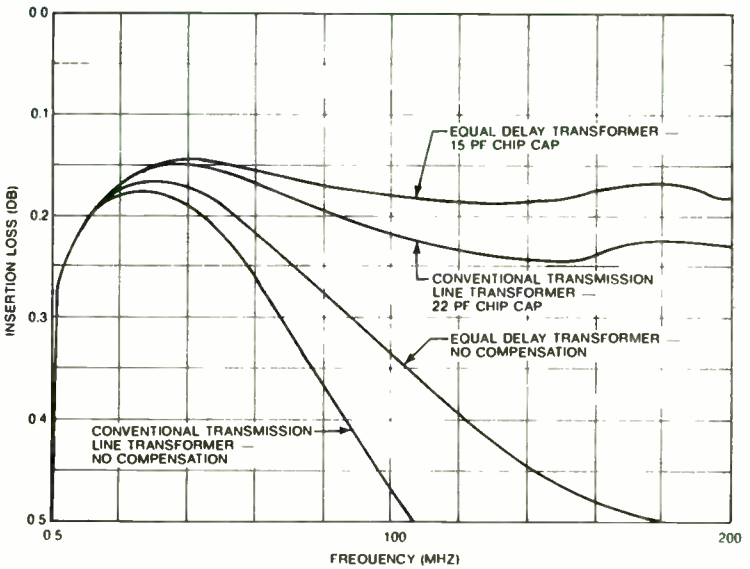
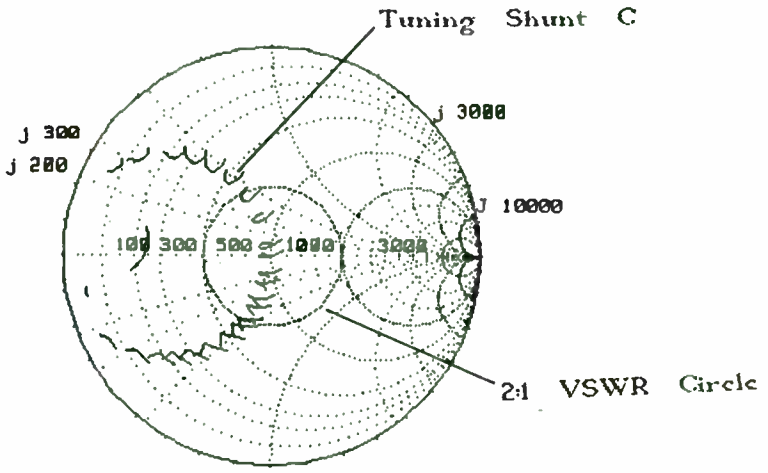


FIGURE 13 BANDWIDTH COMPARISONS OF CONVENTIONAL AND EQUAL DELAY 1:4 TRANSMISSION LINE TRANSFORMERS



Frequency (Mhz)	Reflection Coefficent	Load VSWR	R1	I1
400	.1169 (-69.22	1.265	1060	-234.9
410	.1234 (-80.95	1.282	974.3	-244.2
420	.1326 (-102.7	1.306	913.1	-240.6
430	.1402 (-111.9	1.326	872	-231.5
440	.1447 (-117.7	1.338	847.4	-221.7
450	.1457 (-120.8	1.341	836.3	-214
460	.1442 (-121.3	1.337	836.5	-210.7
470	.1417 (-119.1	1.33	846.2	-213.8
480	.1405 (-114.3	1.327	863.3	-225.4
490	.1434 (-107.3	1.335	885.6	-247.6
500	.1535 (-99.29	1.363	909.9	-282.3

Impedance Matching Network Starting From the Load End:

Component Description	Component Value
CAPACITOR_SERIES	3.668 pF.
INDUCTOR_SHUNT	43.513 nH.
INDUCTOR_SERIES	139.933 nH.
CAPACITOR_SHUNT	.663 pF.

FIG11

++++++++++++++++++++ RECEIVER ++++++++++++++++++++++++++
++++++++++++++++++++ DATA REVIEW ++++++++++++++++++++++++
++

STAGE	NOISE FIGURE Db	GAIN Db	INPUT INTERCEPT(3)Dbm
1	18	100	0
2	1.5	12	10
3	4	-4	27
4	1.2	12	35
5	3	-3	100
6	8	-8	32
7	2.9	-2.9	100
8	1.9	11	35
9	1	-1	100

Rise Sensitivity is 10 Db
Receiver Noise Bandwidth is 2.4 Khz
Temperature is 298 Kelvin

30 MHZ HF COMMUNICATIONS RECEIVER

++++++++++++++++++++ RECEIVER ++++++++++++++++++++++++++
+++++++++++++++ PERFORMANCE WITH PRESENT ++++++++++++++++
++++++++++++++++++++ DESIGN DATA ++++++++++++++++++++++++

STAGE	NOISE FIGURE Db	SENS Dbm	uV	IIP(3) Dbm	IMR Dbm
2	7.268	-123.2	.1539	-12.03	74.11
3	11.27	-119.2	.2439	26.99	97.46
4	3.222	-127.3	.09658	14.94	94.83
5	6.222	-124.3	.1364	17.94	94.83
6	14.22	-116.3	.3427	24.98	94.19
7	17.12	-113.4	.4785	27.88	94.19
8	7.454	-123.1	.1572	16.81	93.27
9	8.454	-122.1	.1764	17.81	93.27

SYSTEM 3rd ORDER IMR IS= 93.27 Db
SYSTEM HALF I.F. REJECTION= 0 Db
SYSTEM SENSITIVITY= .1764 uV

++
+++++++++++++++++ RECEIVER LINE-UP ++++++++++++++++++++++
++

STAGE	DESCRIPTION
1	Receiver Back End
2	IF preamp U 310
3	4 pole crystal filter
4	Mixer post-preamp
5	3 db pad
6	Passive mixer diode ring
7	3 db pad
8	RF preamplifier
9	T/R switch losses and low pass filter loss

FIG 12

COMBINERS AND SPLITTERS

When required output power levels exceed the capabilities of a single power amplifier stage, two or more stages or modules are combined to produce the required output. The combiner is closely related to wideband transformers in design and techniques. A power splitter is simply a lower powered version of the combiner used in reverse. The splitter divides the drive signal into multiple equal amplitude outputs to be applied to the amplifier inputs. The power combiner then recombines the amplified outputs into a single signal. Since the splitter is the same as a combiner, the following discussion will mention only combiners.

A wideband power combiner must perform the following basic functions:

a. Provide low insertion loss over the required bandwidth.

b. Provide isolation (minimum coupling) between the input ports.

c. Provide a low VSWR load at the input ports over the required bandwidth.

The operating bandwidth of combiners must be as wide or wider than the amplifiers to not restrict the overall bandwidth of the transmitter. Transmission line techniques are used for lowest loss and widest bandwidth. The primary function of the combiner is to maintain port-to-port isolation. By isolating the output of one amplifier from the others, multiple failures as a result of a single amplifier failure are avoided. For example, in a two-input-port combiner, if one amplifier is disabled the output power drops by 6 dB. The output drops 3 dB due to lack of power from the disabled module and an additional 3 dB is due to the power from the remaining module dividing equally between the bridging resistor and the output load.

The bridging resistor must dissipate -6 dB of the maximum combiner output power. The bridging resistor value is prescribed by the type and configuration of the combiner as detailed later. Some topologies require either single-ended or balanced, floating bridging resistors. Sometimes the bridging resistor is referred to as the "dump" load or "dump" port since power due to phase or amplitude imbalance is dumped to this load.

The bridging resistor dissipates power due to any slight differences in either the phase or amplitude of the input signals. This relationship is given in figure 14.

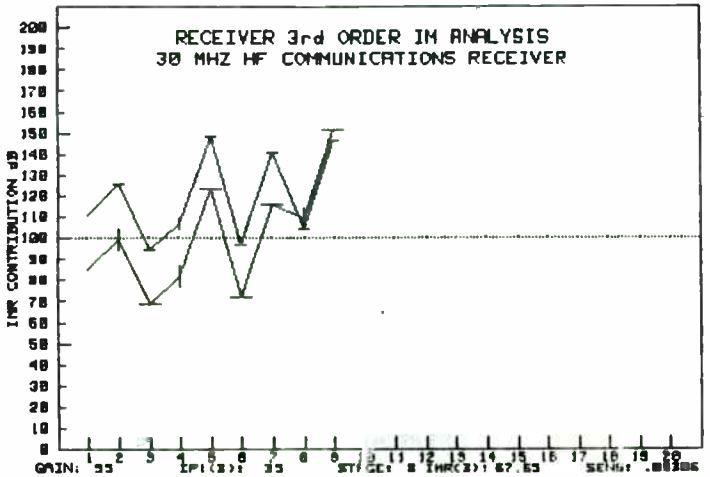
There are three basic types of combiners:

a. In-phase combiner or hybrid (two or more input ports)

b. 180-degree combiner or hybrid (two input ports)

c. 90-degree combiner or quadrature hybrid (two input ports)

FIG 13



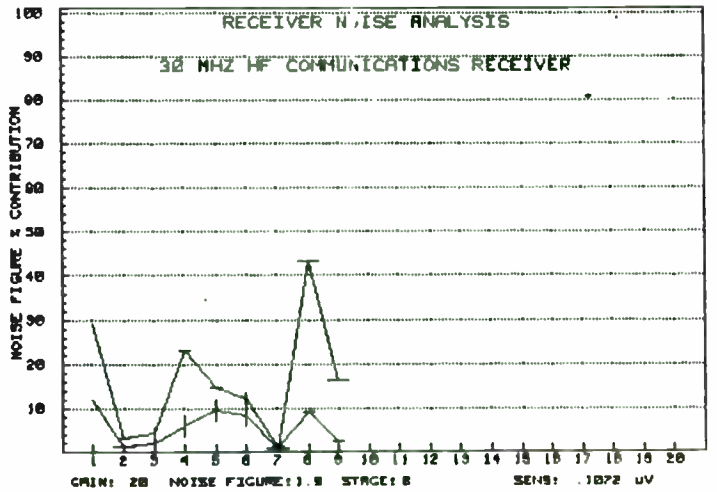
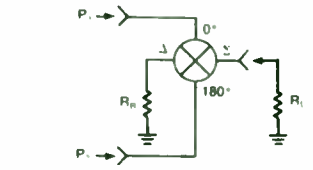


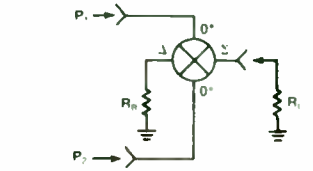
FIG 14



$P_{\Delta} = \frac{P_1 + P_2}{2} - \sqrt{P_1 P_2}\cos\phi$, WHERE ϕ IS DIFFERENCE IN PHASE BETWEEN INPUT PORT SIGNALS

$P_{\Sigma R} = P_1 + P_2 - P_{R_L}$

(A) 180-DEGREE HYBRID COMBINER



$P_{R_L} = \frac{P_1 + P_2}{2} + \sqrt{P_1 P_2}\cos\phi$, WHERE ϕ IS DIFFERENCE IN PHASE BETWEEN INPUT PORT SIGNALS

$P_{\Sigma R} = P_1 + P_2 - P_{R_L}$

(B) IN-PHASE HYBRID COMBINER

FIGURE 14 HYBRID COMBINER POWR RELATIONSHIPS

If more than two signals are combined in-phase, the term "combiner" is used since the term "hybrid" refers to a device with two input ports. The topologies of each of the three basic configurations will be examined.

The following definitions apply:

R_L= output load resistance

R_B= bridging resistor

Z_O= transmission line characteristic impedance

Z_{in}= input impedance (with output port terminated)

S = shield connection of coaxial cable

C = center connection of coaxial cable

IN-PHASE COMBINERS

In-phase combiners operate with two or more inputs of equal phase and amplitude to combine into a single output. There are two basic topologies for in-phase combiners, examples of which are shown in Figures 15 and 16. The differences are in the number and configurations of the ferrite cores and the value of the bridging resistor. The type-I configuration has a single balun core or toroidal core and a bridging resistor equal to four times the output load. The type-II combiner has two separate cores; either sleeves or toroidal. The bridging resistor is equal to the load resistance. Consideration of physical layout, practical transmission line impedances (Z_O), and bridging resistance (R_B) will determine the best type of combiner for a particular design.

A comparison of input impedance and port-to-port isolation between typical type-I and type-II combiners yields interesting results as shown in Figure 17. Both combiners were constructed with a single turn of 50-ohm coax in the cores. Core material was Stackpole 7D for both types. The test data indicates superior port-to-port isolation with a type-II combiner while the type-I combiner exhibited lower input VSWR.

NEW HYBRID POWER AMPLIFIER MODULES SPEED RF SYSTEMS DESIGN

by

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ABSTRACT

For many years low to medium wideband RF amplifiers have been produced in TO-8, TO-12, or TO-39 packages and have become popular with users because of the wide bandwidths, flat gains, small sizes and unconditional stability they offer.

This paper will present the philosophy and design concepts offered in a new hybrid RF power module product line.

INTRODUCTION

For all the convenience and versatility TO style amplifier modules offer the user they still possess two main shortcomings:

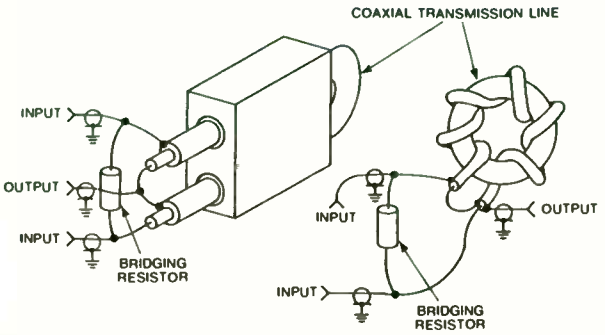
1. RF power output is limited to about a half watt due to the relatively poor thermal conductivity of the Kovar header, and
2. Mounting of a TO style module to a printed circuit board requires physical clearance both above and beneath the board, thereby limiting the component packing density which one can achieve.

To address these two drawbacks Microwave Modules and Devices has developed a new family of Class A RF power amplifier modules, designated the HPM Series, which cover the frequency range of 5 MHz to 2 GHz and which can offer power outputs in the tens of watts. (Figure 1) They are designed in a "Drop-In" flange configuration which is ideal for efficient heat transfer and ease of circuit layout.

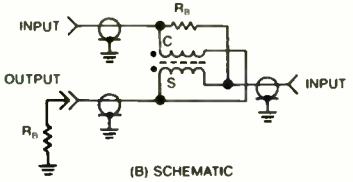
THERMAL CONSIDERATIONS

The RF output power of an amplifier packaged in the standard TO-8 header is limited primarily by the high RF transistor junction temperature due to the thermal conduction characteristics of the header. TO style amplifier modules are most commonly constructed of a ceramic substrate, either alumina (Al_2O_3) or beryllium oxide (BeO), attached to a Kovar header using gold-germanium solder. Kovar, an alloy of nickel, iron, and colbalt, is designed to match the thermal expansion characteristics of the ceramic substrate, thus preventing substrate cracking during temperature changes. While Kovar is an excellent mechanical match for ceramic substrates, it is an extremely poor thermal conductor (Table I). Beryllium oxide, on the other hand, is an excellent thermal conductor, having a thermal conductivity five to six times that of alumina. BeO substrates are typically used in medium power hybrid amplifiers to reduce the device junction temperature as much as possible. Its disadvantages, however, include a high cost when compared to alumina and a high toxicity hazard in a powdered or dust state.

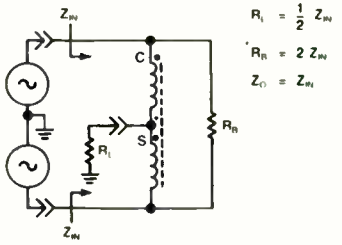
A third substrate material, aluminum nitride (AlN), is just now beginning to become available. Aluminum nitride offers a thermal



(A) PICTORIAL VIEW; BALUN CORE & TOROIDAL CORE

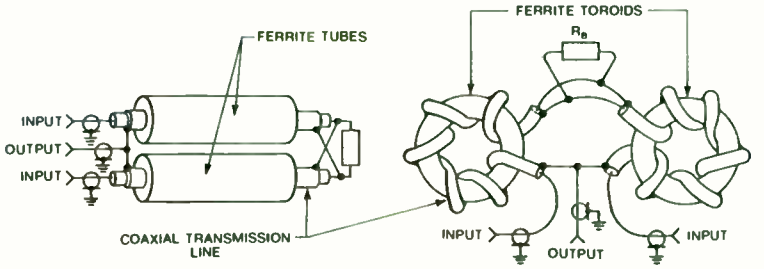


(B) SCHEMATIC

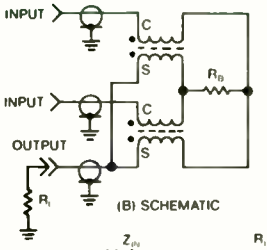


(C) EQUIVALENT CIRCUIT

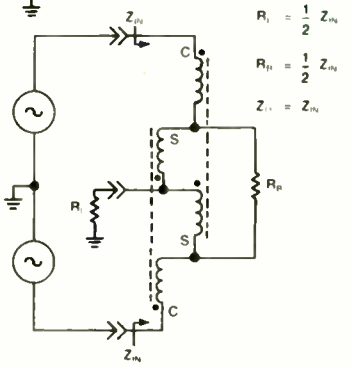
FIGURE 15 TYPE I IN-PHASE TWO PORT COMBINER



(A) PICTORIAL VIEW TUBULAR & TOROIDAL CORES



(B) SCHEMATIC



(C) EQUIVALENT CIRCUIT

FIGURE 16 TYPE II IN-PHASE TWO-PART COMBINER

conductivity near that of BeO without the toxicity problem of BeO. Its present cost, unfortunately, is not less than that of BeO, but, with improved production processes and economies of scale, the cost should come down.

To analyze the temperature problems inherent in packaging a one watt and higher RF amplifier into a TO-8 header the junction to mounting surface temperature rise can be computed for the three situations shown in Figure 2.

Figure 2a and 2b illustrates the cases of a 5 mil thick silicon bipolar transistor die eutectically attached to a 25 mil thick alumina (Figure 2a) or BeO (Figure 2b) substrate which is then soldered to a 50 mil thick Kovar header.

Figure 2c shows the cross section configuration used in the HPM Series product line. For comparison purposes, a 5 mil thick silicon bipolar die is again shown attached, in this case, to a 25 mil thick BeO substrate. The BeO substrate is gold-germanium soldered to a 1/8" thick flange of Elkonite® 10W3 material. Elkonite® 10W3 is a copper/tungsten powdered metal metallurgy material that is designed to match the thermal expansion characteristics of BeO while providing a high thermal conductivity (Table I). Figure 3 shows a photograph of the HPM package. The thin film metallized BeO substrate is mounted inside the alumina "window-frame" by using gold-germanium solder and all circuit components are attached to the BeO substrate by using gold-tin solder. Interconnections are by 1 mil diameter gold bond wire.

Elkonite is a registered trademark of CMW, Inc.

Before calculating the temperature rise in all three cases, a number of assumptions will be made.

1. A semi-infinite lateral extent of the layers.
2. A 45° heat spreading angle.
3. A square heat source configuration.

With these assumptions made, the equation for the thermal resistance of a particular layer can be given as

$$R_{th} = \frac{T}{KW(W + 2T)} \quad (1)$$

Where:

T = material thickness

K = thermal conductivity

W = side dimension of the heat source

The silicon layer heat source dimension is chosen to be 6 mils square, which reflects the approximate active area of a 1 watt Class A RF transistor die.

Using the 45° heat spreading assumption, the heat source side dimension, W, is increased by twice the thickness of the material of the preceding layer. Therefore using Equation (1) the thermal resistances of the various materials can be calculated. The results are as follows:

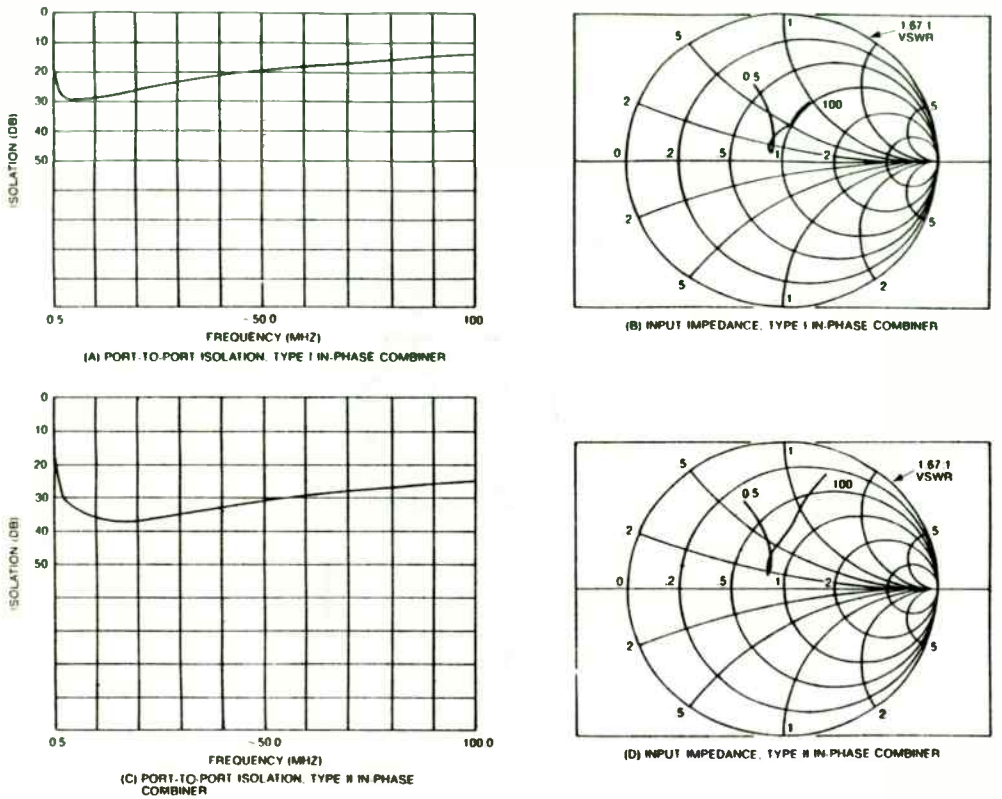
R_{th} (Silicon) = 18.6°C/W

$R_{th}(Al_2O_3)$ = 29.6°C/W

R_{th}(BeO) = 4.6°C/W

R_{th}(Kovar) = 10.9°C/W

R_{th}(Elkonite®) = 1.5°C/W



(A) PORT-TO-PORT ISOLATION, TYPE I IN-PHASE COMBINER

(B) INPUT IMPEDANCE, TYPE I IN-PHASE COMBINER

(C) PORT-TO-PORT ISOLATION, TYPE II IN-PHASE COMBINER

(D) INPUT IMPEDANCE, TYPE II IN-PHASE COMBINER

FIGURE 17 COMPARISON OF TYPE I AND TYPE II IN-PHASE COMBINERS

The combiner output load impedance is usually transformed to another desired value such as 50 or 75 ohms. This is readily accomplished by one of the wideband transformers described earlier. Usually the output impedance transformer is physically integrated into the combiner assembly. The interconnection between combiner and transformer can be made using micro-strip line techniques if it is not a standard coax impedance.

Theoretically any number of inputs may be combined with an in-phase combiner, but a practical limit is reached when the output impedance becomes too low to allow efficient wideband transformation back to the desired load impedance. An example of a type-II four port in-phase combiner is given in figure 18.

Four-port combiners may also be implemented by cascading two port combiners. This technique is illustrated in figure 19 for both types of two port combiners.

In-phase combiners all use a floating bridging resistor. This may be difficult to implement, especially in combiners handling high power. A wideband balun transformer allows using a single-ended or unbalanced load. The balun could also transform the balanced impedance to 50 or 75 ohms. Standard coaxial dummy loads, connected to the combiner with coax cable, may then be used as bridging resistors.

Therefore, for the three cases, summing the thermal resistances:

R_{th} (TO-8, Al_2O_3) = 59.1°C/W

R_{th} (TO-8, BeO) = 34.1°C/W

R_{th} (HPM) = 24.7°C/W

We shall further assume that for 1 watt of Class A RF power, 4 watts total dissipation (25% efficiency) will be expended by the RF transistor. Therefore, the temperature rise of the transistor junctions for the three cases are as follows:

ΔT (TO-8, Al_2O_3) = 236.4°C

ΔT (TO-8, BeO) = 136.4°C

ΔT (HPM) = 98.8°C

With a mounting surface temperature of +50°C the junction temperature can then be computed to be:

T_j (TO-8, Al_2O_3) = 286.4°C

T_j (TO-8, BeO) = 186.4°C

T_j (HPM) = 148.8°C

The impact upon reliability of these three temperatures can be understood by using a graph of median time to failure (MTTF) versus junction temperature, the so-called "Arrhenius" relationship. Major device failure mechanisms have been shown to vary exponentially with temperature according to the equation

$$MTTF = C \exp(\phi/KT)$$

where

C = a constant

ϕ = activation energy

K = Boltzman's constant

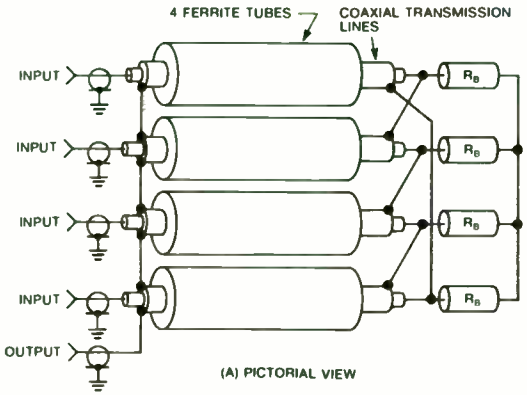
T = temperature (°K)

Typical RF transistors under consideration use a gold metal system and have activation energies between 0.6 and 0.7 eV. If we plot the Arrhenius curve using a gold system activation energy (Figure 4), we observe that for a 20°C rise in junction temperature the device MTTF is reduced by approximately one half.

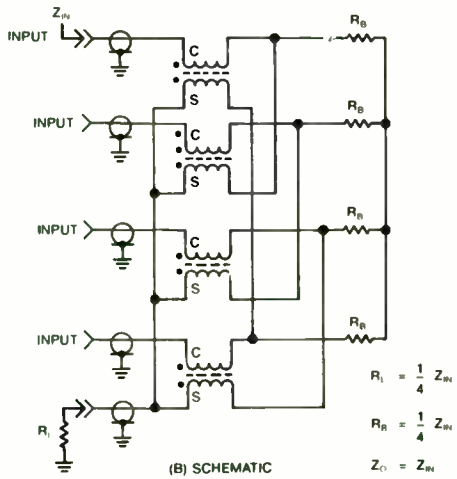
The projected MTTF of the silicon bipolar transistor used in the HPM package is found to be approximately four times greater than when mounted in a TO-8 header on a BeO substrate and one hundred times greater than when mounted in a TO-8 header on an alumina substrate. Because we have assumed that the packages are mounted to an infinite heat sink with no thermal resistance, the junction temperature of the TO-8 devices will actually be higher than those calculated. This is due to the thermally non-ideal mounting requirements inherent in TO devices.

MECHANICAL CONSIDERATIONS

TO style modules must be mounted from the back side of the microstrip PC board such that the package is in intimate contact with the ground plane. Failure to provide a positive contact between the microstrip ground plane and the package can result in gain resonances, VSWR degradation and unwanted oscillations, especially in high gain (~40dB) cascades.

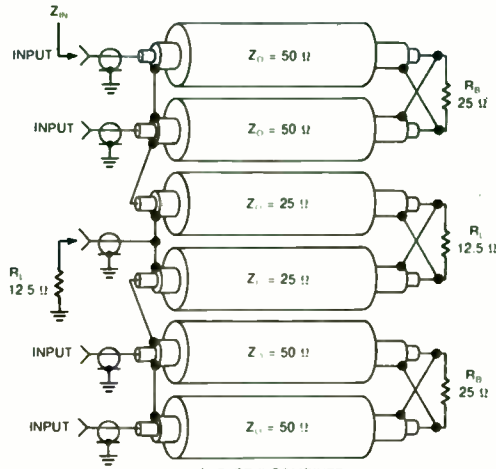


(A) PICTORIAL VIEW

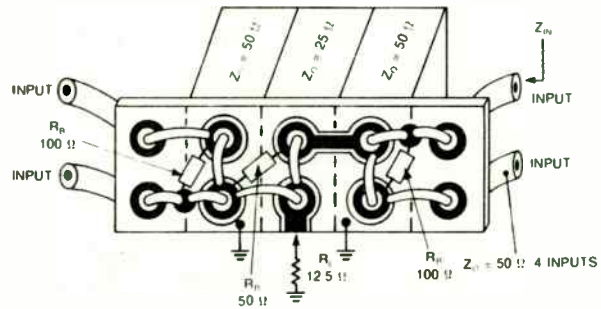


(B) SCHEMATIC

FIGURE 18 TYPE II FOUR PORT IN-PHASE COMBINER



(A) TYPE II COMBINER



(B) TYPE I COMBINER

FIGURE 19 FOUR PORT COMBINERS IMPLEMENTED WITH TWO PORT IN-PHASE HYBRIDS

Because of this requirement, clearance in the housing to which the PC board is mounted must be available both above and below the board. In high package density systems, this volume may not be available without causing the overall subsystem or system package to be larger than desired. In addition, rework and replacement is more difficult with modules mounted on the underside of PC boards. To address these drawbacks some manufacturers have developed surface mount type packages for amplifiers. However, at the present time, their use appears limited to amplifiers whose output power is less than 100 mW.

HPM AMPLIFIERS

The Microwave Modules and Devices HPM series provides an alternative to discrete device amplifiers for those users who enjoy the ease of design and use that existing TO style or surface mount amplifiers offer, but who require higher output power or lower distortion. The HPM product line is an attempt to solve the thermal and mechanical limitations inherent in the TO-8 style packages and is designed as a "Drop-In" component, not unlike existing flange mounted RF power transistors, which is ideal for efficient heat transfer. The "Drop-In" configuration also simplifies the circuit board and housing design.

The HPM product line presently consists of several models (Figure 5) which cover the frequency range of 5 MHz to 2 GHz with models under development that will offer power outputs in the tens of watts.

The HPM package is epoxy sealed and leak tested to ensure high reliability. For military applications requiring conformance to MIL-STD-883 a totally hermetic version is being developed. Figure 6 shows a photograph of a prototype hermetic package. This package is designed to be welded closed by using either laser or seam sealing techniques and will provide a leak rate better than 1×10^{-7} atm-cc/sec.

To illustrate the similarity in concept and integration with existing small signal cascadable amplifiers, Figure 7 shows a connectorized housing designed to accommodate up to 3 TO-8 modules driving an HPM module.

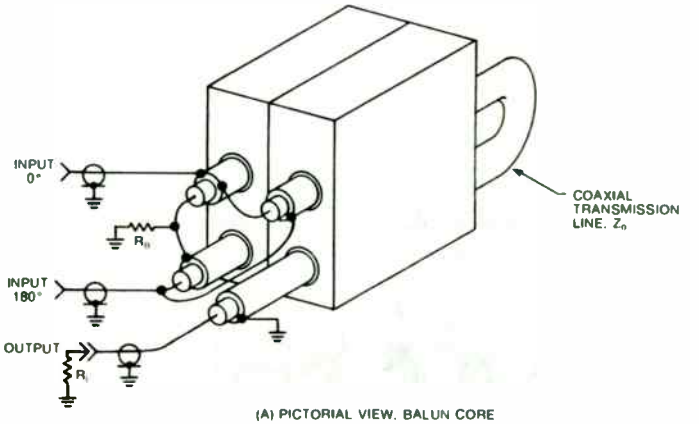
REFERENCES

1. "Handbook of Electronic Packaging" McGraw-Hill, 1969.
2. "Engineering Materials Handbook" Montell, First Edition, 1958.
3. "Handbook for Applied Engineering Science" Chemical Rubber Company, Second Edition, 1973.

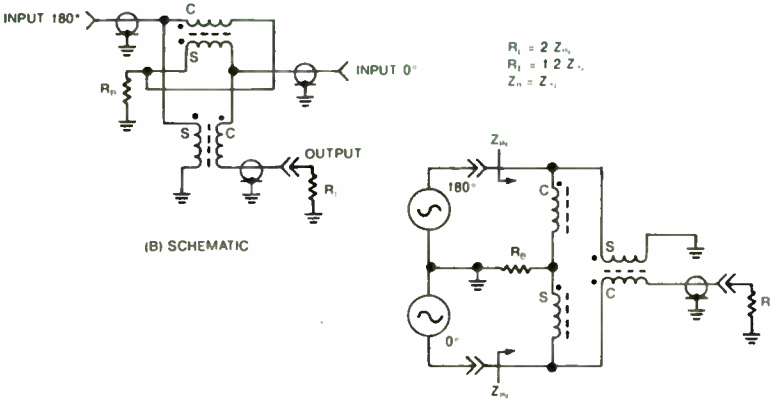
180-DEGREE HYBRIDS

If the roles of the bridging resistor and the load are interchanged, the result is a 180-degree hybrid combiner. The two input signals must be 180-degrees out of phase and of equal amplitude. The output is balanced to ground unless the usual balun is used. Examples of type-I and type-II 180-degree hybrid combiners with output baluns are shown in figures 20 and 21.

Many unique combiner designs are possible by using various combinations of basic combiner types and balun transformers. The combiner described in figures 22 (pictorial) and 23 (schematic) is an example of a four-port combiner using two each type-I in-phase combiners (cores A and F) and two each, parallel connected type-II 180-degree hybrid combiners (cores D and C) and a 4:1 balun transformer (cores B and E) to couple the combined output to a 50-ohm load. Connecting two 180-degree hybrids in parallel avoids using 25-ohm coax cable and provides the extra core material to handle the higher rf power.



(A) PICTORIAL VIEW. BALUN CORE



(B) SCHEMATIC

(C) EQUIVALENT CIRCUIT

FIGURE 20 TYPE I 180-DEGREE HYBRID COMBINER

TABLE 1

Thermal Conductivity and Thermal Expansion of Various Materials

MATERIAL	THERMAL CONDUCTIVITY Watt/°C-in	THERMAL EXPANSION in/in x 10^{-7}/°C
99.6% Al_2O_3	0.80	65
99.5% BeO	5.1	90
Gold	7.5	142
Aluminum	6.4	236
Silver	10.6	197
Kovar (Fe, Ni, Co)	0.42	60
Silicon (@ +95°C)	2.8	35
Molybdenum	4.0	53
Elkonite® 10W3(Cu,W)	6.8	95
Copper	9.5	167
Tungsten	4.2	44

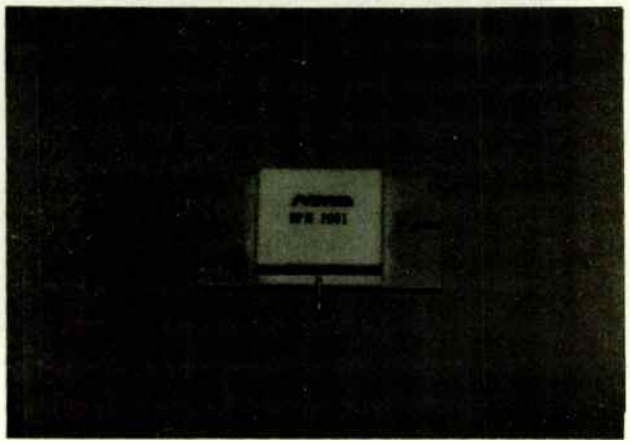
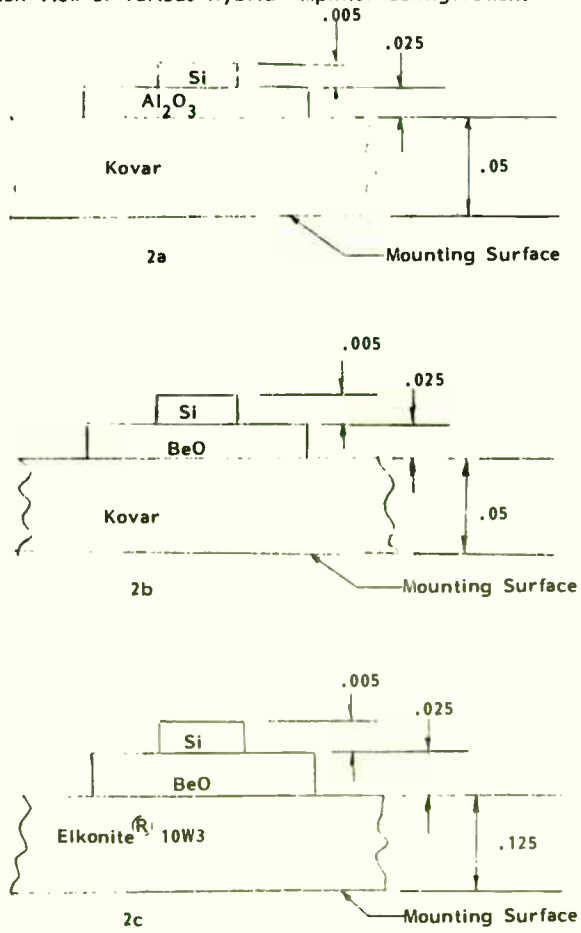


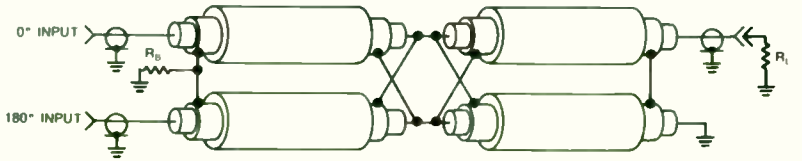
FIGURE 1

HPM Series Package

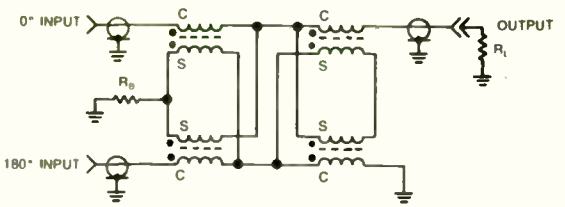
FIGURE 2

Cross Section View of Various Hybrid Amplifier Configurations

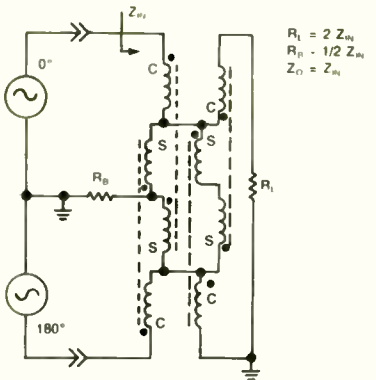




(A) PICTORIAL VIEW, TUBULAR CORES



(B) SCHEMATIC



(C) EQUIVALENT CIRCUIT

FIGURE 21. TYPE II 180-DEGREE HYBRID COMBINER

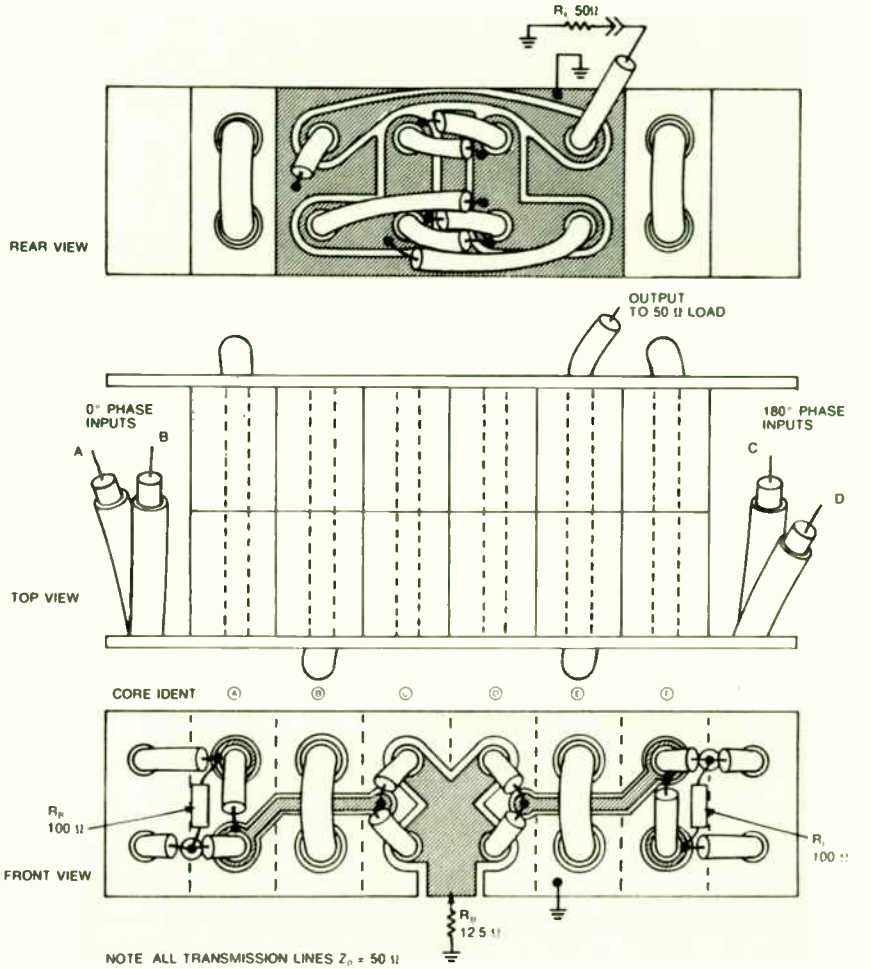


FIGURE 22. FOUR PORT, TWO STAGE COMBINER USING TYPE I AND II HYBRIDS. PICTORIAL

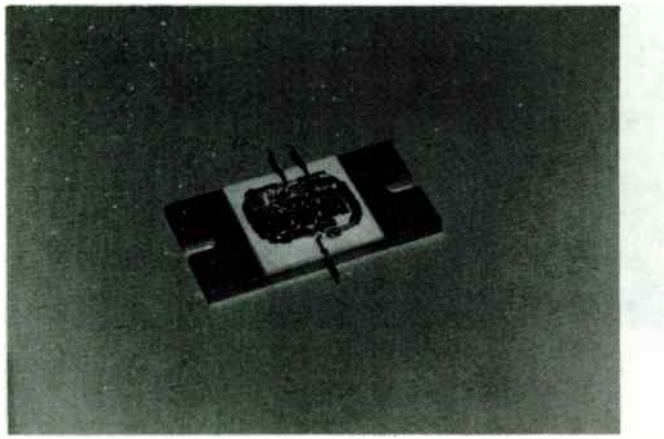


FIGURE 3

Inside View of HPM Series Amplifier

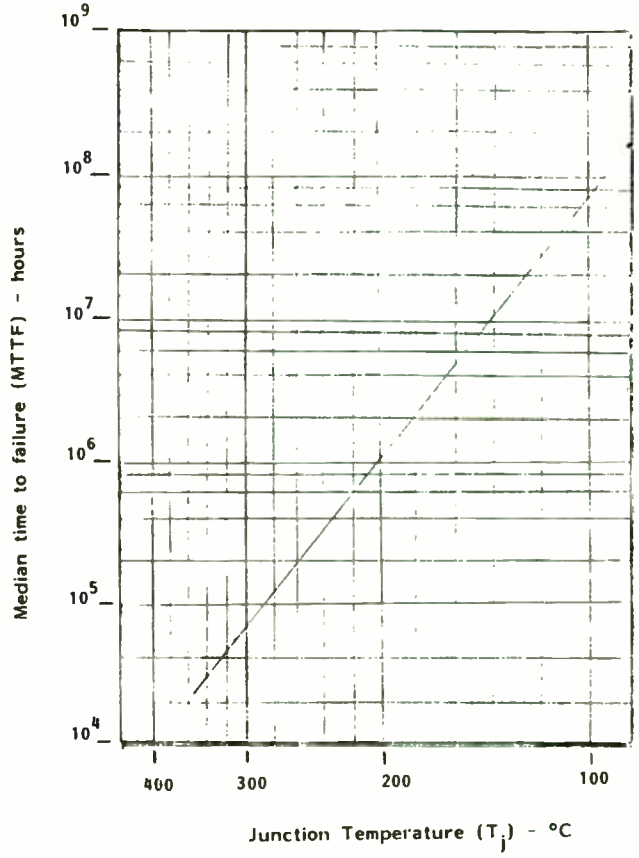


FIGURE 4

MTTF Versus Junction Temperature

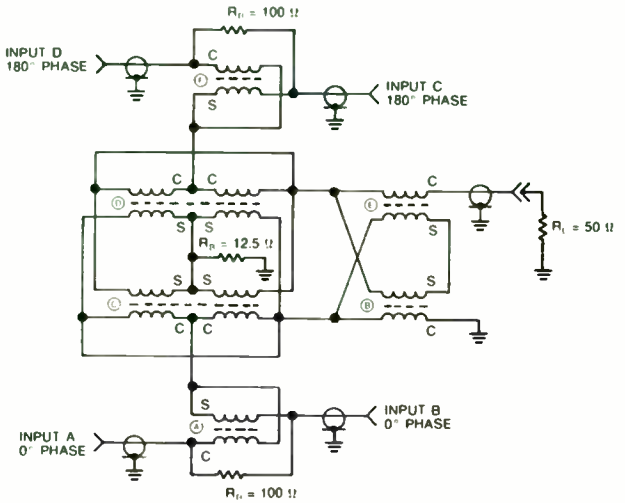


FIGURE 23 FOUR PORT, TWO STAGE COMBINER USING TYPE I & II HYBRIDS; SCHEMATIC

QUADRATURE HYBRIDS

The quadrature hybrid has two input ports, each of equal amplitude but one is 90-degrees out of phase relative to the other. Four-phase combining of four amplifier modules is feasible using two quadrature hybrids and a 180-degree combiner.

The quadrature hybrid is constructed by using "all-pass" networks and a wideband hybrid as shown in the block diagram of figure 24. Two all-pass networks are required; one for 0-degree (reference) phase shift and the other for 90-degree phase shift relative to the reference output. The absolute phase shift across an all-pass network changes with frequency, however, the two networks are designed to maintain a constant 90-degree phase difference between their outputs as the input frequency to both networks is varied.

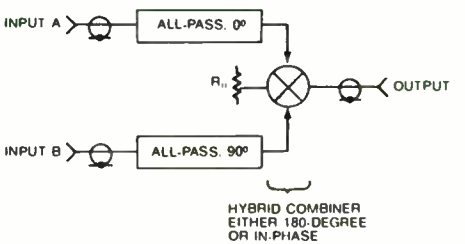


FIGURE 24 BLOCK DIAGRAM OF A QUADRATURE COMBINER

The all-pass networks may either be balanced or unbalanced circuits. Typical circuit topologies for both are shown in figure 25. Note that the mutual coupling in the unbalanced network must be negative and of a prescribed value.

FIGURE 5

Typical Performance Characteristics of HPM Product Line

MODEL	FREQUENCY RANGE	GAIN	POWER OUTPUT @ 1dB GAIN COMPRESSION	DC POWER
HPM 501	5-500	10 dB	1.5 Watts	+24V @ .6A
HPM 505	10-500	8 dB	6 Watts	+24V @ 1.2A
HPM 1002	20-1000	9 dB	3 Watts	+24V @ .8A
HPM 2000	50-2000	1[illegible] dB	.25 Watts	+15 @ .3A
HPM 2001	50-2000	10 dB	1.5 Watts	+15 @ .75A

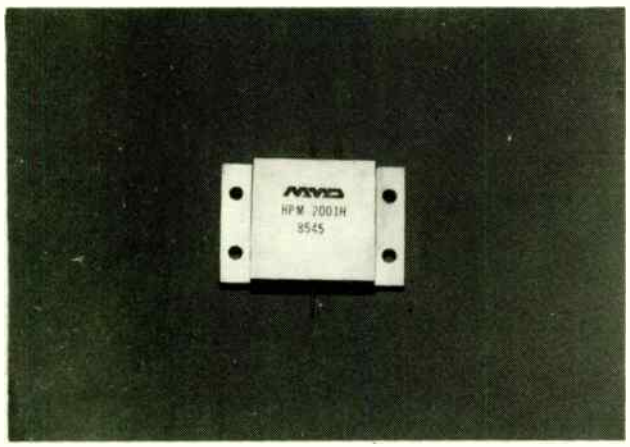


FIGURE 6

Prototype Hermetic HPM Package

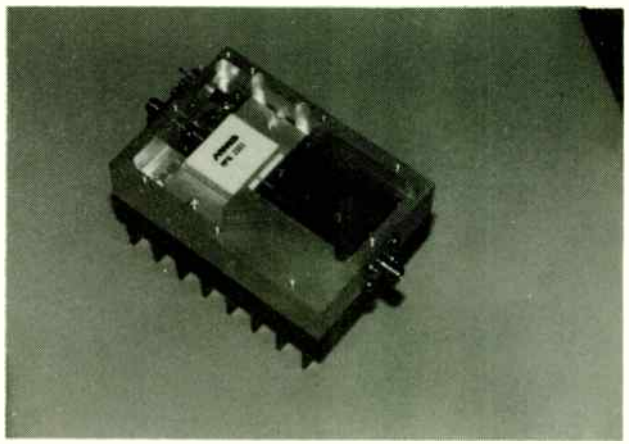


FIGURE 7

Connectorized HPM Enclosure with Capability for 3 TO-8 Style Amplifiers

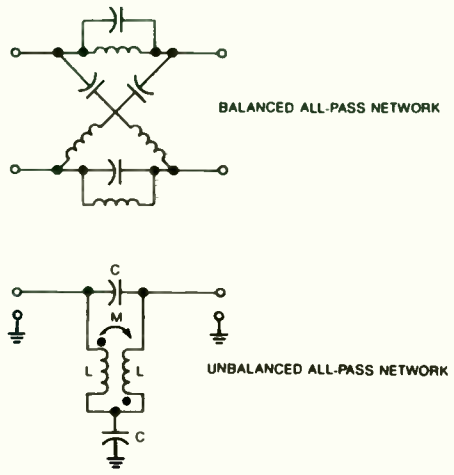


FIGURE 25. TYPICAL ALLPASS NETWORK TOPOLOGIES

Both circuits exhibit difficulties in practical implementation. The balanced lattice network may require long leadlengths and possibly a balun transformer for interface to an unbalanced hybrid. It requires more components than an equivalent unbalanced network and the component values must be closely matched to achieve low VSWR across the design bandwidth.

Implementation of an unbalanced all pass network allows shorter lead lengths and eliminates the balun transformer. It requires fewer components than an equivalent balanced all pass network. No closely matched component values are required, however, an exact amount of mutual coupling is required between two inductors.

The quadrature hybrid offers three advantages over the in-phase and 180-degree hybrids when used as an output combiner in solid state wideband power amplifiers. The third harmonic and certain other odd order harmonics cancel in the output port and add in the bridging resistor. The all pass phase shift networks and the basic combiner specifications must hold up to the frequency of the highest harmonic of concern to achieve this in practice. For example, the all-pass networks must provide the 90-degree phase difference up to at least 90 MHz in order to cancel the third harmonic of a 30 MHz fundamental signal in the hybrid's output.

RF power flowing into the output port of a quadrature hybrid will split, go through the all pass networks, partially reflect at the signal source impedance, go back through the all pass networks, and cancel in the output port and add across the bridging resistor. This is happens whether the power flowing into the output port is the result of a mismatched load or coupling from an adjacent transmitting antenna. The result is the combined power amplifier output behaves as though it has a matched source impedance. The situation of reverse power flow from adjacent transmitter coupling is especially important since the two signals cross modulate each other in the active devices. The

intermodulation products caused would be radiated along with the desired signal. The quadrature hybrid will cancel some of these "backdoor" IMD products in it's output port by terminating the energy in the bridging resistor.

Two wideband linear power amplifiers, combined with a quadrature hybrid, will exhibit nearly constant gain under varying load impedances (varying VSWR). The ratio of input power into the quadrature hybrid splitter to the forward power out of the quadrature hybrid combiner will be nearly constant in contrast to the same situation using in-phase or 180-degree hybrids.

Techniques for wideband RF power transformers, combiners, and splitters have been presented with emphasis on topology. Various types of transformers and combiners were examined and classified. Examples of each were presented in pictorial form, schematic, and equivalent circuit in an effort to bridge the gap from theory to working hardware. A rich variety of combinations of the basic transformers and combiners are possible though not covered here. It is hoped that a more complete understanding of the basic types presented here will enable the reader to produce more sophisticated designs.

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DESIGN CONSIDERATIONS FOR A 1 KW L-BAND RADAR MODULE

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INTRODUCTION

Completely solid-state transmitters for very high power radar systems, such as the SPS-40, PAVE PAWS, or TPS 59 have clearly demonstrated several advantages over tube equipment:

- Overall reliability is greatly improved.
- System down time is decreased.
- Individual modular amplifiers can be replaced while the radar continues to operate.
- Very wide operational bandwidths are easy to achieve.
- Modular solid-state transmitters are ideally suited for phased array systems.

Even though the first solid-state radar systems were significant steps forward in the state-of-the-art, many areas can still be improved further. Microwave Modules & Devices (MMD) has found that an integrated technology approach to the modular amplifier design offers significant performance improvements. MMD's integrated approach includes optimization of the design of the transistor die, device packaging, and special matching components targeted for the specific amplifier program. Areas where performance improvements can be the most dramatic using this integrated approach are:

- Higher power output per module.
- Reduced module cost and improved manufacturability.
- Amplifier efficiency
- Module reliability.
- Ease of combining large numbers of amplifier modules.
- Thermal management.
- Significant increases in power output per cubic inch of module volume.
- Amplifier bandwidth.
- Harmonic reduction.

This paper will address some of these important performance areas as they apply to the design of the new MMD AC-1214-1000P L-Band radar modular building block. Performance improvements push the state-of-the-art forward and make solid construction of multi-kilowatt transmitters more practical than ever. A summary of the performance of the MMD AC-1214-1000P is shown in Table 1.

AMPLIFIER ARCHITECTURE

The 1 KW amplifier architecture (Fig. 1) is a modular structure with commonality that centers around a well designed 350

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watt, building block, sub-module. A basic driver module delivers power to a single sub-module which then drives an array of four sub-modules via a 4-way divider. The sub-modules are then combined through a 4-way combiner and that output is put through an isolator for VSWR protection of the amplifier.

SUB-MODULE

The sub-module uses two separate transistors that are thermally independent. These two transistors are interconnected in a parallel configuration. Figure 2 illustrates the structure of the MMD sub-module. This block is optimized for use as a wideband power amplifier with 50 ohm interface impedance levels. As a result the sub-module becomes an easy to use building block throughout the amplifier. Some of the features of the MMD sub-module are listed in Table 2 and a performance summary is shown in Table 3. To realize a high performance, RF power module (see Fig. 3) that is reliable and reproducible, the design should start at the chip level and build from there. The design of the electrical and mechanical interfaces of the chip with the rest of the module are crucial to the final electrical performance and the long term reliability of the module. Starting a state-of-the-art module design using off-the-shelf RF power transistors often limits both performance and reliability. Following initial electrical ship interfaces, the wideband impedance matching circuitry must be configured.

PERFORMANCE OF MMD'S AC-1214-1000P

1 KILOWATT L-BAND MODULE

POWER OUTPUT:	1000 WATTS MIN.
FREQUENCY RANGE:	1.2 TO 1.4 GHZ
POWER INPUT:	1 WATT
EFFICIENCY:	20% MIN
PULSE WIDTH:	10 USEC
DUTY CYCLE:	5%
OPERATING VOLTAGE:	45 VOLTS
RISE TIME:	200 USEC MAX.
FALLTIME:	200 NSEC MAX.
DROOP:	.5DB MAX

Table 1.

FEATURES OF MMD

SUB MODULE

- 2.0:i VSWR IN AND OUT
- SMALL SIZE
- EASY TO MANUFACTURE
- CONSISTENT ELECTRICAL PERFORMANCE
- WIDE BANDWIDTH AT HIGH POWER

Table 2.

PERFORMANCE OF MMD 350 WATT
SUB-MODULE

POWER OUTPUT:	350 WATTS MIN.
FRQUENCY RANGE:	1.20 TO 1.40 GHZ
GAIN:	7 DB MIN
EFFICIENCY:	40%
PULSE WIDTH:	10 J SEC
DUTY CYCLE:	5%
OPERATING VOLTAGE:	45 VOLTS
RISE TIME:	75 NANOSECONDS (SEE FIG 11)
FALL TIME:	40 NANOSECONDS (SEE FIGURE 11)
PULSE DROOP:	0.2 DB

Table 3.

Two approaches to the sub-module electrical design were considered; the first, was a push-pull configuration, and the second, a parrallel configuration. The push-pull design has the advantage of reduced even harmonics and higher input and output impedances at the device level, but the disadvantage of increased size and complexity. The parallel transistor design has the disadvantage of higher even harmonics and lower input and output impedances at the transistor, but parallel transistor configuration has advantages of smaller size and reduced complexity. Since two of the prime considerations were small physical size and large production quantities, the parallel transistor configuration was chosen for the sub-module design. Even harmonics can be dealt with without much difficulty because of the 15% bandwidth. The microstrip circuit design used for matching the devices is a simple low pass ladder-type network which is straight forward to design and construct. Since the input and output (load conjugate) impedances of the device are quite similar (and both are inductive), the matching circuit is basically the same for both input and output.

First, a simple ladder network is designed to match the impedance of one device referenced to ground (load). Figure 4 illustrates a simple "pi" type match from the device impedance to 15 ohms. Next, the two single ended matches are parallel to give 7.5 ohm impedance. The 7.5 impedance is then transformed to 50 ohms with a 20 ohm transmission line of the appropriate length as

RF AND MICROWAVE TRANSISTOR BIAS CONSIDERATIONS

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INTRODUCTION

The purpose of this paper is to present an overview of the advantages and disadvantages of some common bias circuits. Resistive, diode, and active bias circuits will be examined and compared as to how well they stabilize the transistor bias point against DC parameter changes caused by temperature and device-to-device variations.

BIAS POINT STABILITY

Before examining the bias circuits, let's look at some of the reasons for being concerned about bias stability. Figure 1a shows a transistor biased for Class A operation which is not stabilized against DC parameter changes. Increasing temperature shifts the bias point further to saturation (Figure 1b), while decreasing temperature shifts the bias point closer to cutoff (Figure 1c). Temperature extremes caused the transistor's DC parameters to change which resulted in the shift of the bias point. In the above example the shift in the bias point was large enough to cause unwanted distortion in the output signal. Figure 2a and 2b show that both gain and noise figure of a bipolar transistor are also a function of the collector current.

Bias point shifts caused by temperature are not concern. The DC parameters also change due to device- variations . The DC current gain of microwave bipolar tr can vary over a range of 5:1 and still be wit manufacturer's electrical specification at 25 degrees means that a shift in the bias point can be c temperature and device-to-device variations. Obviously circuit that can minimize these bias point shifts is d The first step in understanding how to stabilize the bi is to identify the DC parameters which affect the bias most and how these parameters respond to temperature var

TEMPERATURE SENSITIVE DC PARAMETERS

The principal dependent variable in DC stability an the collector current (I_C)[1,2]. The following DC par which are shown in the equivalent circuit of Figure temperature sensitive and directly influence the current.

Base to Emitter Voltage (V_{BE}):

V_{BE} is internal to the transistor and has a temperature coefficient of 2 mV/degree C. Figure 4 s temperature characteristic of this parameter.

Reverse Collector Current (I_{CBO}):

I_{CBO} is the current flowing through the reversed bi

shown in Figure 5. Care must be taken with the DC feed design for the best rise time performance, particularly on the input (emitter) side. The feeds should be connected to the lowest possible RF impedance point and have only enough inductance to avoid circuit detuning. As can be seen in Figure 5, the DC feed on both the input and output circuits are connected where the transistor matching networks are paralleled. This is the lowest impedance point where a single inductor can be used. As a result the inductance used to connect into these feed points can be kept to a minimum, thus minimizing the rise time (the rise time of the intrinsic transistors is less than 10 nanoseconds).

The mechanical chip interface is a primary reliability consideration. A major design goal of the modules is to minimize the thermal resistance between the chip and the baseplate. The lower the thermal resistance, the cooler the chip operates and therefore the greater the reliability. The sub-module configuration uses two active areas that are physically separate to better distribute the heat, resulting in lower active area temperaures and improved reliability.

When attempting to design a basic system building block, the ideal is to make all RF connections at the 50 ohm impedance level which is compatible with the system Zo.

By using the sub-module as a building block, the appropriate configuration of blocks can be arranged to construct the 1 KW amplifier as shown in Fig. 1.

TRANSISTOR DIE SELECTION

The heart of any solid-state amplifier design is the semiconductor die and much attention must be paid to this area.

Four basic types of power semiconductor die are available for use at this frequency:

- GaAs MESFET
- Silicon vertical MOSFET
- Silicon Junction FET or SIT
- Silicon Bipolar

GaAs MESFETs are horizontal structures with all three terminals (gate, source, and drain) on the top surface. This creates a major problem with large high power devices for both surface interconnect metallization complexity and device wire bonding. Also GaAs material has a high thermal resistance compared to silicon as well as numerous crystal defect problems that result in very low yields for large area, high power devices.

The silicon vertical MOSFET device is very promising for lower frequencies, but higher device capacitances (compared to silicon bipolar) create significant stability, output matching

junction of the collector to base. Classically, this leakage current is expected to double for every 10 degrees C temperature rise in a silicon semiconductor junction. The leakage current for silicon is so low that under most conditions this parameter can be negected.

DC Current Gain (h_{FE}):

The h_{FE} of a transistor is defined as the ratio of the collector current to the base current. This parameter typically increases linearly with temperature at the rate of 0.5 % /degree C.

STABILITY FACTORS

Before we proceed to examine the bias circuits, it is useful to introduce the concept of stability factors. The stabiliy factors are defined as the ratio of the incremental change of I_C vs the incremental change of each of the three components I_{CBO}, V_{BE}', and h_{FE}. The stability factor equations are given below.

I_{CBO} STABILITY FACTOR

$$S_{ICBO} = \frac{\partial I_C}{\partial I_{CBO}} \Big|_{h_{FE}, V_{BE}' = \text{constant}}$$

V_{BE}' STABILITY FACTOR

$$S_{VBE}' = \frac{\partial I_C}{\partial V_{BE}'} \Big|_{h_{FE}, I_{CBO} = \text{constant}}$$

h_{FE} STABILITY FACTOR

$$S_{hFE} = \frac{\partial I_C}{\partial h_{FE}} \Big|_{I_{CBO}, V_{BE}' = \text{constant}}$$

The total change in collector current can be expressec of each incremental change caused by I_{CBO}, V_{BE}', and h

$$\Delta I_C = S_{ICBO} \Delta I_{CBO} + S_{VBE} \Delta V_{BE} + S_{hFE} \Delta h_{FE}$$

Unfortunately, the stability equations can be complicated even for a simple bias circuit such as th in Figure 5. The equation of Figure 5 can be easily di computer, but it doesn't help the designer gain any i selecting component values or in making circuit c Fortunately, the following approximations can help s stability equations:

* Neglect I_{CBO} when using silicon transistors. As stated, the leakage current for silicon is typic that neglecting I_{CBO} will have negligible effe accuracy of the stability equations.

* Drop the hie term, which is the hybrid-pi inpu for common emitter configuration. The extern resistance is usually much greater than hie, and the hie term will not upset the accuracy of the

* Assume that $h_{FE} >> 1$ then $(h_{FE} + 1)$ simplifie

The stability factor S_{hFE} can be expressed as a percent in I_C vs a percentage change in h_{FE} [3]. The new vi defined as I_{hFE}. The same procedure is used to define

and/power transfer problems at L-Band. Several lower capacitance MOSFET designs have been announced but none has yet to be proven repeatable, manufacturable and reliable. Junction FETs (or SITs) presently available are not useful for 500 MHz because gain and efficiency are too low and the output capacitance is too high. Some new design concepts show promise, particularly for higher voltage operation but production quantity devices are not available.

This then leaves the silicon bipolar device, which in fact, proves to be an excellent solution. Recent processing technology improvements combined with new die geometries have resulted in large signal ft's of over 5 GHz from high power L-band devices.

Two basic types of silicon bipolar die configuration are available for pulse operation at L-Band. Die A (Fig. 6A) has two large base areas perpendicular to the input/output die bonding.

The common lead is bonded down the centerline of this die. The input bonding is staggered from front to back, alternating between the common lead bonds. Die B has many smaller base areas (Fig. 6B) which are arranged parallel to the input/output bonding. Both input and common lead bonds are arranged in an alternating pattern down the center line of the die.

Also to be chosen was the device terminal to be used as ground (common base vs common emitter). For both die types, common base is preferred due to higher gain and better thermal sharing over the device surface during pulse operation at these frequencies.

Advantages of die A are:

- More base area (and therefore emitter perimeter for power capability) per mil of die length.
- Better output capacitance/power ratio (0.4 pF/watt VS 0.5 pF/watt for die B)
- Fewer bond wires.

Disadvantages of die A are:

- Unsymmetrical input (emitter) bonding and wide (7 mil) base cells restrict upper frequency response.
- Limited pulse width/duty factor capability (100 use 5% maximum)

Advantages of die B are:

- Narrow die and numerous base bond wires give very low common lead inducture for improved ruggedness, stability, input/output isolation, efficiency, and upper capability.
- Spread base cell design allows operation from short pulse to CW due to better thermal balance.

$$K_{hFE} = \frac{\Delta I_C / I_C}{\Delta h_{FE} / h_{FE}} = \frac{S_{hFE}}{I_B}$$

$$K_{VBE'} = \frac{\Delta I_C / I_C}{\Delta V_{BE'} / V_{BE'}} = \frac{V_{BE'}}{I_C} S_{VBE'}$$

The stability equations for the previous example (Figure 5) now simplify to the following:

$$K_{hFE} = \frac{1}{\left(1 + \frac{hFE\ RC}{R_B} \right)}$$

$$K_{VBE} = \frac{1}{\left(1 - \frac{VCC}{V_{BE'}} \right)}$$

The simplified stability factors are easier to handle and it is now apparent that increasing the R_C / R_B ratio will decrease K_{hFE} and improve collector current stability against h_{FE} changes. We now have the tools to examine the bias circuits.

RESISTIVE BIAS CIRCUITS

* Fixed Bias

The fixed bias circuit shown in Figure 6, is the simplest and one of the worst methods of biasing a transistor because it has a very high sensitivity to h_{FE} variations. Notice that K_{hFE} is unity, which means that a 20 % change in h_{FE} will result in a 20 % change in collector current. Since h_{FE} can vary by as much as 5:1 from device to device, the transistor could be at cutoff with one device and at saturation with another. The base current, which is fixed by the voltage difference between the supply voltage and $V_{BE'}$, is the cause of the poor bias stability. If the base current were made to decrease with increasing increase with decreasing h_{FE} the bias stability would greatly, which exactly describes the operation of circuit.

* Voltage Feedback Bias

The voltage feedback bias circuit shown in improves bias stability by allowing the base current to to changes in the collector current. If the collector increases, the voltage drop across R_C increases which r a lower collector to emitter voltage (V_{CE}). Since current is set by the resistor R_B and the voltage diffe V_{CE} and $V_{BE'}$, a lower V_{CE} decreases the base curre stabilizes I_C to a current closer to the quiescent bia The circuit will handle a decrease in I_C in a similar m

A circuit designed with I_C = 10 ma, V_{CE}= 10 V, V_C h_{FE}= 50 results in K_{hFE}= 0.826. This means that the current will change by 82.6 % of the change in h_{FE} as co the 100 % change that would be expected from the fi circuit. This is approximately a 17 % improvement over bias circuit for this set of conditions. The K_{hFE} factor shows that increasing the R_C / R_B ratio decre sensitivity of I_C to h_{FE} changes. A small value of R_B the h_{FE} stability, but it isn't alway easy to get a smal of R_B. A smaller effective value of R_B is possible u

Disadvantages of die B are primarily related to a slightly more complex structure to manufacture and assemble.

TRANSISTOR PACKAGING AND INTERNAL MATCHING

Three types of device internal matching were considered: 1) single ended, using a double input and a paralls output resonance matching (Fig. 7); 2) single ended, single input match (Fig. 4); and 3) the split push-pull using a single input match (Fig. 8). The high impedances of the more complex single ended device at least equalled using the four times impedance increase of the single input matched device when split and used push-pull. The disadvantages of the output matched construction must also be considered.

- The series resonance of L1 and C1 (Fig. 7), typically just below the low end of the band (about 1.1 GHz) causes serious oscillation problems when fast rise/fall times are employed. This usually shows up as a "noisy" spurious signal at 1.1 GHz only 20-30 dB down or as a distortion "glitch" on the detected pulse turn-off slope.

  The parallel tank circuit of the output match causes major output signal phase shifts when the device output capacitances change. This "phase modulator" effect can cause phase noise and power combining problems. The output capacitance is, unfortunately, a function of many things including voltage, power level, temperature, and die manufacturing variations.

- Failure of the DC blocking capacitor (C1) has historically been a reliability problem with this type of output matching structure.

Of the three internal matching techniques considered for the transistors, the single ended input matched device was chosen because it was the least complex, both internal to the transistor package and to external circuitry. It would also yield the smallest module size. The single input match chosen will sacrafice some bandwidth and an increase in even harmonics. Typical performance of a single transistor is shown in Table 4.

The die of each transistor is packaged in the BeO ceramic cavity shown in Fig. 9. Note the very wide input/output leads for low inductance of those interfaces. This allows low "Q" device impedances for good broadband performance when shunt tuned and operated into the matching networks. The leads are "captive sealed" between the device lid and the single layer ceramic ring for improved lead strength. Co-fired multi-level ceramic ring packages with exposed, non-captive leads were avoided due to high lead inductance and numerous lead failure problems. 40 mil thick

emitter resistor feedback circuit.

* Voltage Feedback and Constant Base Current Source

The circuit of Figure 8 can be considered to have a constant base current source, formed by the resistor network of R_B, R_{B1} and R_{B2}. The collector current can be made relatively stable if I_{BB} is chosen to be much greater than the transistor base current I_B. A good choice, somewhat arbitrary , is to pick $I_{BB} = 5I_B$ to $10I_B$. A value greater than $10I_B$ gives little improvement in stability.

* Emitter Resistor Feedback

The bias circuit of Figure 9 is one of the best methods of biasing a transistor. The circuit operates in the following manner. When the collector current and therefore the emitter current increases, the voltage drop across R_E increases. The polarity of this voltage opposes the forward bias voltage between base-to-emitter. The reduced V_{BE} decreases I_B and therefore I_C, which stabilizes the collector current closer to its initial value. The stability factor(K_{hFE}) for this circuit is 0.169 when calculated using the design values previously given for the voltage feedback circuit, and $I_{BB} = 5I_B$. A $K_{hFE} = 0.169$ represents a considerable improvement in stability over the previous circuits.

The V_{BE} stability factor for this circuit is:

$$S_{VBE} = \frac{-1}{R_E} \quad (\text{assuming } R_E >> \frac{R_B}{h_{FE}})$$

This equation implies that, the larger the R_E, the stability against V_{BE} variations. There is a limit R_E can be, since the voltage drop across R_E excessive. The next circuit examined (diode compensation) presents a method of stabilizing ac temperature variations without resorting to large R_E v

The emitter resistor feedback circuit does requi RF considerations which are covered in detail late paper.

* Diode Temperature Compensation

The emitter-base voltage has a negative dependence of about 2 mv/ degree C, which can be comp introducing diodes into the voltage divider network a Figure 10[4,5].

The calculated stability factor for this circuit 1/ $5.65R_E$, which is a 5.65 times improvement over t feedback circuit of Figure 9. The above calculation wa the design values from the voltage feedback example, compensation was done with a single diode that had a t characteristic identical to the transistor emitter-base

* Zener Diode Bias

The Zener diode shown in Figure 11 determines the

BeO ceramic is used for the package substrate for improved thermal resistance.

Frequency - 1.2 to 1.4 GHz
Pout - 200 Watt
Gain - 7.0
Efficiency - 45%

TYPICAL TRANSISTOR DATA

Table 4

THERMAL CONSIDERATIONS

Many variables effect the junction temperature of the devices used in the amplifier, including:

- amplifier efficiency and output power
- pulse width/duty factor
- die thermal response time
- die thermal balance ("hot spots")
- overall module baseplate temperature
- die to baseplate thermal resistance

A good indication of the presence of hot spots (and therefore high junction temperature) is the power droop over the length of each output pulse. A droop of 0.2 dB for 30 degrees C baseplate temperature will degrade to 0.5 at elevated temperature. A droop of 0.5 dB at 30 degrees C will degrade to more than 1.0 at elevated temperatures. Droop of over 1 dB is usually an indication of excessive junction temperature. The ultimate thermal test of any amplifier is a scan of all amplifier die with an infared microscope under actual operating conditions. Typical requirements might ba a maximum junction temperature of 140 degrees C with a baseplate temperature of 85 degrees C. Thermal scans for pulse widths less than 5 usec are difficult due to risetime limitations of infared sensors, but are essential for verifying reliable amplifier design and construction.

DIVIDER/COMBINERS CONSIDERATIONS

To achieve the required 1 KW output power, four of the sub-modules must be combined, therefore a divider and combiner must be designed. Two basic types of combining schemes were considered; 1) the Wilkinson combiner and; 2) 90 degree 3 dB hybrid.

Advantages of a Wilkinson divider/combiner

- Excellent amplitude balance.
- Excellent phase balance
- Easy to manufacture basic circuit
- Low insertion loss
- Good port to port isolation

to base voltage V_{CB} of the transistor. The collector to emitter voltage V_{CE} is fixed by the sum of V_{BE} and the Zener diode voltage (V_Z). The current through R_C divides between the transistor and D_1. Temporarily ignoring the current through R_B, the only current flowing through D_1 is the base current of the transistor. Most of the current flows through the collector as I_C. If the h_{FE} is low, the current through D_1 will increase accordingly. However, if h_{FE} is high, the current through D_1 is low and the regulation as a Zener is poor. Therefore, R_B is added to the bias circuit to ensure that enough current flows through the Zener for good voltage regulation[6].

This circuit is more stable than the voltage feedback circuit, but the Zener diode is noisy and may require a large value bypass capacitor to prevent the Zener's noise from modulating the amplified RF signal.

* Active Bias Circuit

An active bias circuit is shown in Figure 12, which uses a PNP transistor (Q_2) to help stabilize the bias point of the RF transistor (Q_1). The transistor Q_2 acts as a DC feedback circuit that senses the collector current of Q_1 and adjusts Q_1's base current to hold the collector current I_{C1} constant. The circuit operates in the following manner. If I_{C1} increases, the voltage drop across R_C increases and opposes the forward bias of the PNP transistor which decreases I_{E2}. The decrease in I_{E2} causes I_{C2} and I_{B1} to decrease. The lower base current into Q_1 dec which opposes the original increase in the collector cu

The collector current equation for the RF tran shown in Figure 12. Notice that if $(1+ h_{FE1}) R_C$ h_{FE2}), then the collector current is essentially inde the DC current gains of either of the transistors detailed analysis of this circuit is available literature[7].

The active bias circuit has the best stability of circuits examined, but does require the most parts. transistor does form a feedback circuit, which must he RF bypassed to prevent bias oscillations.

EMITTER RESISTOR BYPASS

The emitter resistor improves bias stability throug of negative feedback which is desirable at DC, but no frequencies. The RF gain will be reduced if the resist RF bypassed. Bypassing the emitter resistor does req special precautions to prevent possible oscillations.

First, the emitter bypass capacitor must be large provide an effective RF ground at both the design frequ lower frequencies. The Smith Chart of Figure 13 shows t on the transistor S-parameters when the bypass capacitor too small. Changes in the transistor s S_{11} and S_{22} parame

Disadvantages:

- No VSWR isolation at the divider.
- No reduction in back IMDs at combiner.
- Difficult to reduce or eliminate the effects of the capacitanc of isolation resistor.
- Small size can be difficult to achieve and still handle high power.

Advantages of 90 degree 3 dB hybrid:

- VSWR isolation at divider.
- Reduction in back IMDs at combiner.
- Improvement in harmonics.
- 50 ohm terminations are required therefore, capacitance of termination is less of a problem.
- with proper design small size can be achieved.
- Low insertion loss.
- Good port to port isolation.

Disadvantage:

- Amplitude imbalance.

There are several 90 degree 3 dB Hybrid configurations (branch line, backward wave, rat-race, wireline, etc.), but because physical size is of paramount importance the Sage tightly coupled wireline coupler was chosen. Fig. 10 shows the typical insertion loss of a wireline coupler and how the amplitude balance is typically less than 0.2 dB over the frequency band of 1.2 to 1.4 GHz. Fig. 11 is a plot of insertion loss versus frequency of a 4-way divider/combiner the amplitude balance between any of the four ports is less than 0.6 dB peak-to-peak. The physical size is 1.0"W x 4.00"L x .30H for the 4-way combiner including two of the three isolation termination (the output isolation termination is mounted to the bottom of the amplifier housing for better heatsinking).

A combiner and divider were coupled back to back and insertion loss measured and the data is shown in Fig. 12. which shows the insertion loss to be less than .8 dB for a divider and combiner connected back to back.

LOW LEVEL DRIVER MODULE

The block diagram for the driver is shown in Fig. 13. There are three stages that make up the driver plus two attenuators. The 2.0 dB attenuator at the input of the driver is for reducing the drive to the first stage for overdrive protectionand input VSWR improvement. The second stage provides the power to drive the third stage to approximately 100 watts. The 2.0 dB attenuator at the output of the third stage provides VSWR isolation between the output of the driver module and the input of the 350 watt sub-module driver stage. The performance of the drive stage is shown in Table 5:

shown on the Smith Chart as S_{11}/ and S_{22}/. A good RF bypass capacitor should cause little or no effect on the S-parameters . Both S_{11} and S_{22} at 4 GHz remains unchanged after the emitter resistor and 100 pF capacitor are added, but move off the Smith Chart as the frequency decreases. Reflection coefficients greater than 1 indicate conditional stability and are likely to oscillate. A value of 1000 pF would be a much better bypass capacitor value.

The second precaution is to minimize the inductance added in the emitter caused by the resistor and capacitor parasitics. The Smith Chart of Figure 14 shows the effect of emitter inductance on the transistor's S-parameters. Inductance in the emitter can potentially cause conditional stability. In this case, a rather large value of 5 nHy was selected to illustrate the effect. At a frequency of 4 GHz S_{22}/ has moved off the Smith Chart which indicates that the circuit is conditionally stable.

An effective RF bypass of the emitter resistor is a relatively straightforward procedure as long as the above precautions are taken.

SUMMARY

This paper has shown that bias stability is more a function of the bias circuit design than of the transistor's characteristics. The RF and bias circuits should be designed with equal consideration, since the RF performance of an amplifier was shown to be dependent on the bias stability.

REFERENCES

1. Philip Cutler," Electronic Circuit Analysis ". Vol. 2, McGraw-Hill 1967. Chapters 4-11, pp. 220-228.

2. Hewlett-Packard Application Note 944-1, "Microwave Transistor Bias Considerations"

3. Albert Malvino, "Transistor Circuit Approximations", McGraw Hill Book Company, 1968, pp. 202-234.

4. G.J Ritchie, "Transistor Circuit Techniques , Discrete and Integrated ", Van Nostrand Reinhold, 1983, pp. 82-84.

5. D. Schilling, C. Belove, " Electronic Circuits: Discrete and Integrated ", 2 nd Edition pp. 190-192.

6. J.H. Reisert,Jr.," Ultra Low-Noise UHF Preamplifier". Ham Radio Magazine, pp. 8-19, March 1975.

7. Ralph Carson, " High Frequency Amplifiers ", Wiley. 1982, 2nd Edition, pp. 145-187.

Freq.	1.2 to 1.4 GHz
Pout	70 watts min.
Pin	1.0 watts
Vc	45 volts
Ic	9.0 amps (PK) max

INPUT RETURN LOSS -13dB max

TYPICAL PERFORMANCE DATA

LOW LEVEL DRIVER

TABLE 5

1.0KW AMPLIFIER PERFORMANCE

Table 6 is the tabulation of the performance of the 1 kW amplifier module for 1.0 watts input drive. It can be seen that the amplifier module meets or exceeds the design goal set down in Table 1.

CONCLUSION

Multikilowatt all solid state amplifiers are seeing increased popularity. With the availability of modular building blocks such as the 350 watt sub-module, these high power amplifiers are both practical and easy to assemble. The sub-module building block using an integrated design from the silicon out to the 50 ohm terminal can be totally optimized for specific program requirements. The module described above was targeted for narrow pulse width, (10 usec) low duty cycle (5%) application. The same design approach and integrated technology can be applied to long pulse, high duty cycle applications as well. The practical realization of both parallel combining of transistors and 90 degree combining within the amplifier truly provides a wideband, reproduceable 50 ohm block that can be used to build multikilowatt systems.

Freq. GHz	Pout W	Pin W	RL dB	Ic Amps (Avg)	Pulse Droop dB
1.2	1148	1.0	-20	4.4	0
1.3	1445	1.0	-12	5.2	-.3
1.4	1175	1.0	-16	4.2	0

Vc = 45 Volts

Duty Cycle = 4%

Pulse Width 7 use

TYPICAL PERFORMANCE DATA

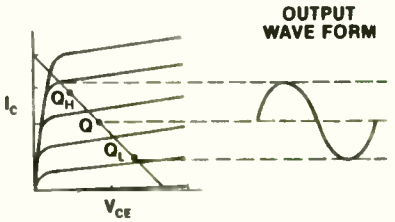
1KW L-BAND POWER AMP.

Table 6

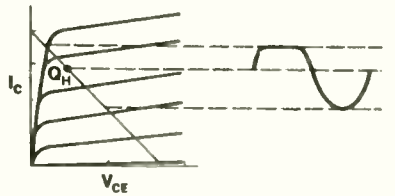
FIGURE 1

EFFECT OF TEMPERATURE ON THE BIAS POINT

A. BIAS POINT: AT 25°C



B. BIAS POINT SHIFT DUE TO INCREASING TEMPERATURE, AND DISTORTION IN OUTPUT WAVE FORM



C. BIAS POINT SHIFT DUE TO DECREASING TEMPERATURE, AND DISTORTION IN OUTPUT WAVE FORM

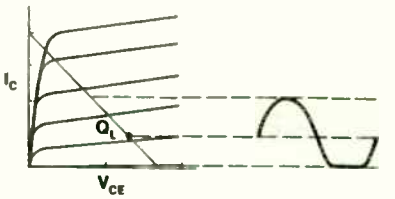
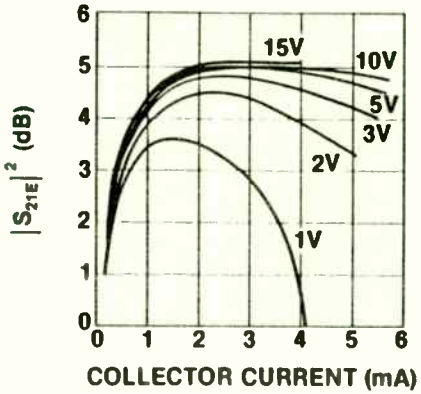


FIGURE 2

A. RF GAIN ($|S_{21}|^2$) VS. BIAS POINT



B. NOISE FIGURE VS. BIAS POINT

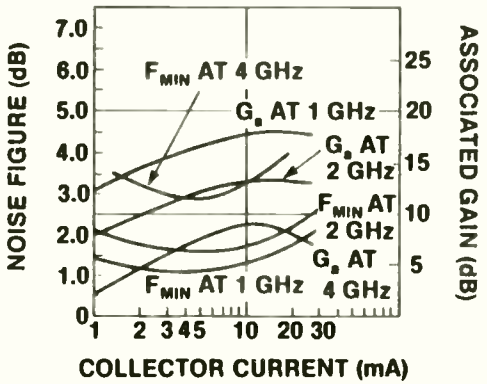


FIGURE 3

PARAMETERS THAT DOMINATE CHANGES IN I_C AND V_{CE} WHEN TEMPERATURE VARIES:

- $V_{BE'}$ (BASE TO EMITTER VOLTAGE)
- I_{CBO} (REVERSE COLLECTOR CURRENT)
- h_{FE} (DC CURRENT GAIN)

DC TRANSISTOR MODEL

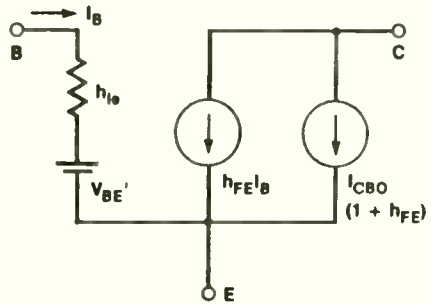
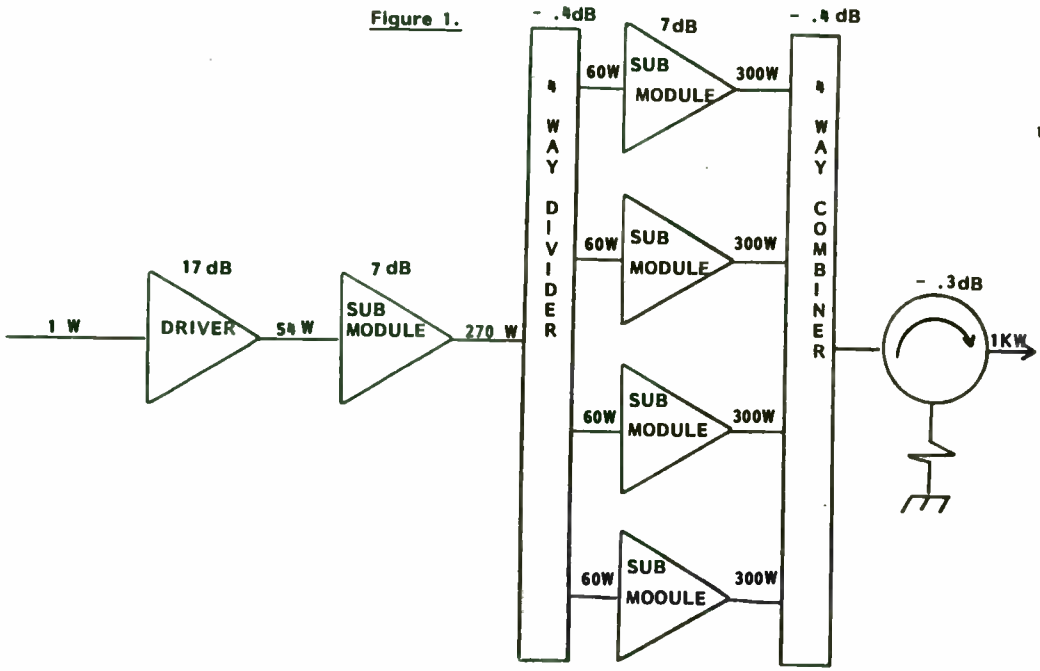
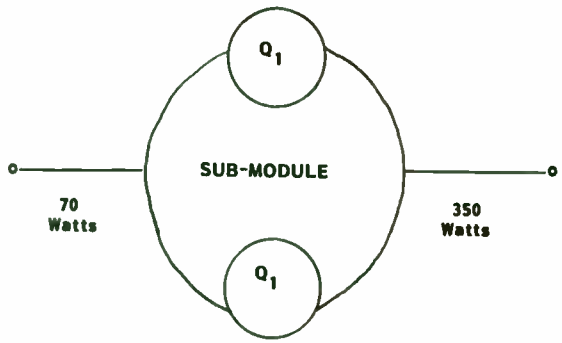


Figure 1.





MMD 1.2 to 1.4 GHZ, 350 WATT, SUB-MODULE

Figure 2

GAIN VS FREQUENCY

AND

EFFICIENCY VS FREQUENCY

OF

MMD 350 WATT

SUB-MODULE

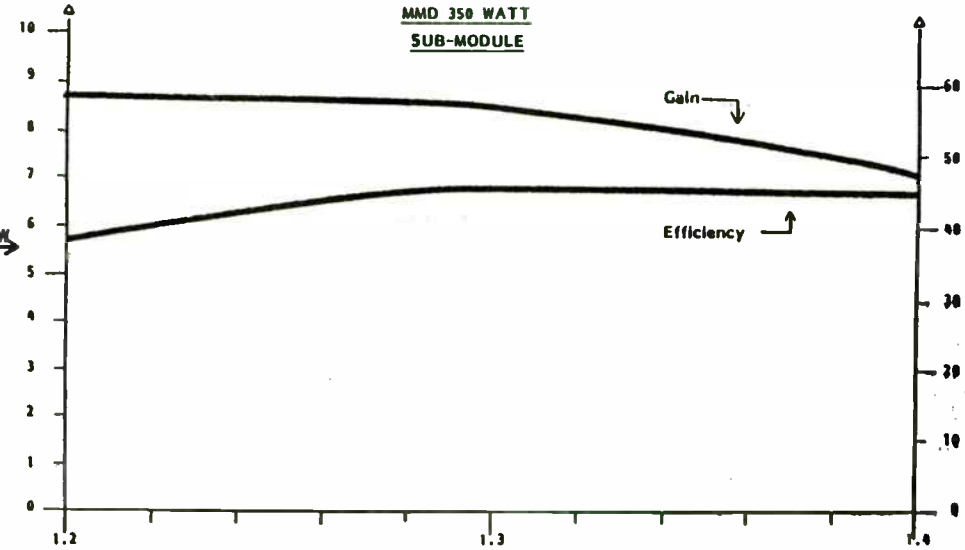


Figure 3

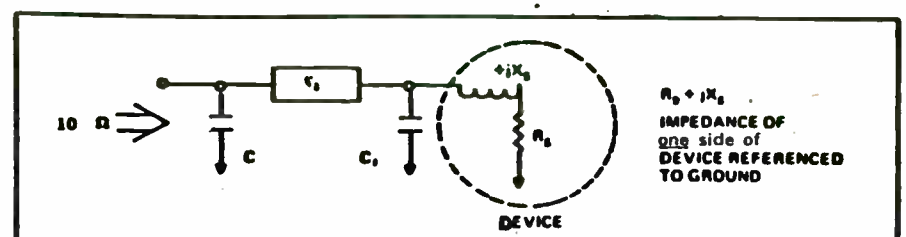


Fig. 4 Single ended input design model.

FIGURE 4

COLLECTOR CURRENT VS. V'_{BE} AND TEMPERATURE

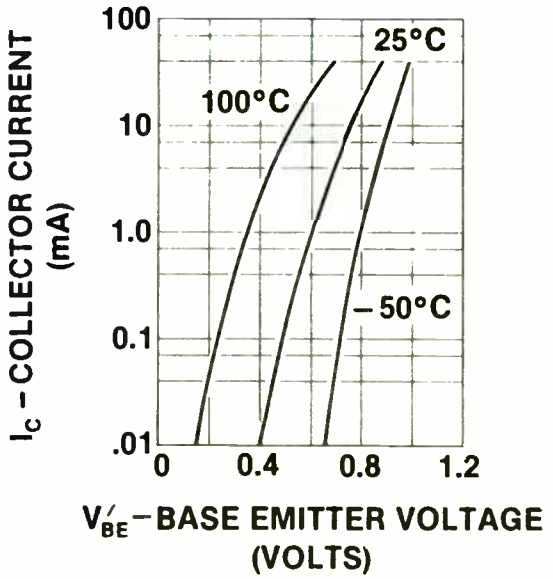
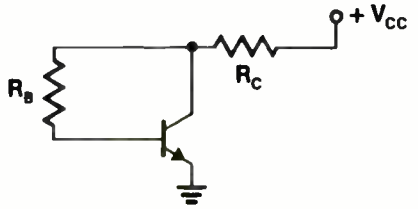


FIGURE 5

EVEN FOR SIMPLE BIAS CIRCUITS THE EQUATIONS BECOME COMPLICATED



$$\bullet\ Sh_{FE} = \frac{h_{FE}R_C + R_B + h_{IE} + R_C)\,(V_{CC} - V'_{BE} + KI_{CBO})}{(h_{FE}\,R_C + R_B + h_{IE} + R_C)^2}$$

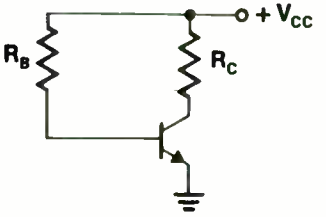
$$- R_C \left[\frac{(h_{FE}\,(V_{CC} - V'_{BE} + KI_{CBO}) + KI_{CBO})}{(h_{FE}R_C + R_B + h_{IE} + R_C)^2} \right]$$

Where: $K = h_{IE} + R_B + R_C$

- GOT ALL THAT?

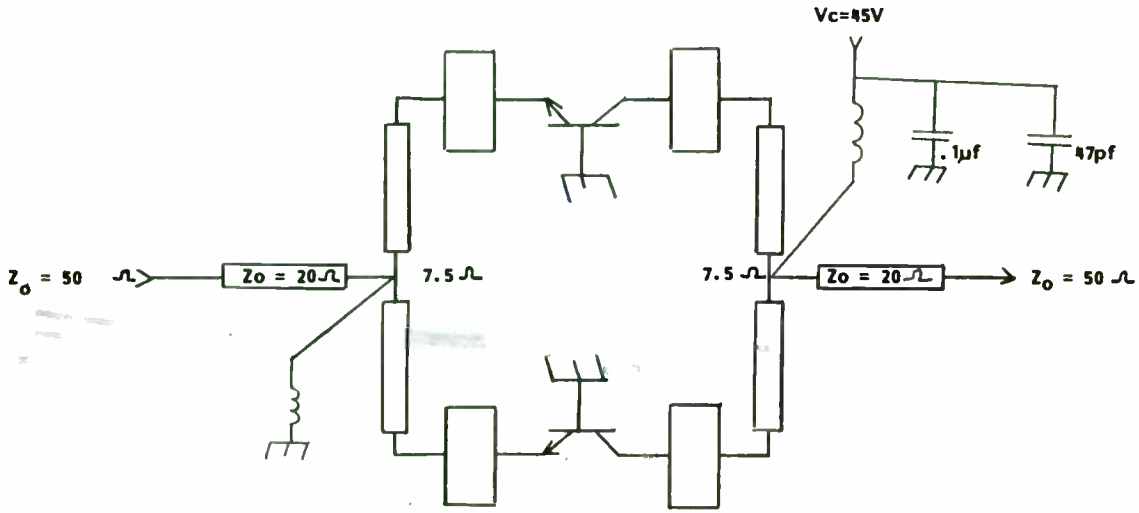
FIGURE 6

FIXED BIAS



- $I_C = \dfrac{h_{FE}\,(V_{CC} - V'_{BE})}{R_B}$
- $Kh_{FE} = 1$
- $KV'_{BE} = \dfrac{1}{(1 - \dfrac{V_{CC}}{V'_{BE}})}$

ADVANTAGE: FEW COMPONENTS,
DISADVANTAGE: INFERIOR TEMPERATURE STABILITY, LARGE I_C VARIATIONS



MMD 1.2 to 1.4 GHz 350 watt. SUB-MODULE

Figure 5

L-BAND DIE CONFIGURATIONS

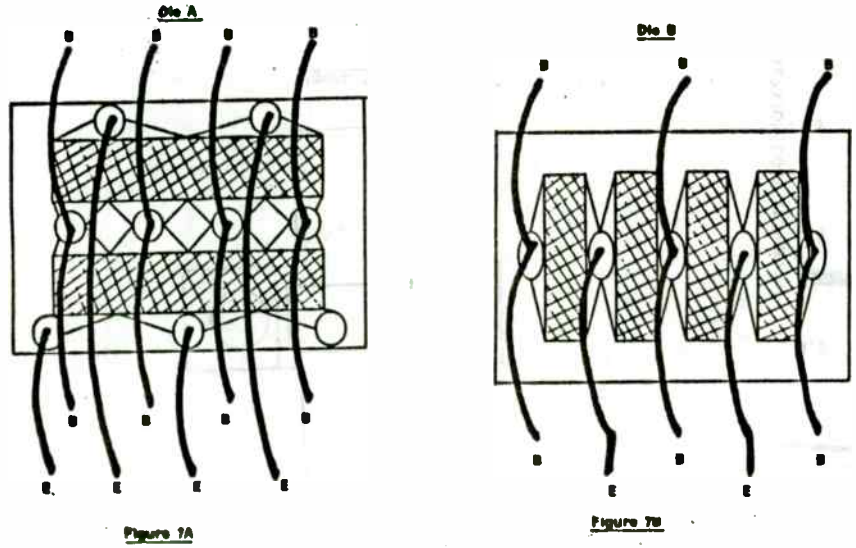


Figure 7A

Figure 7B

Figure 6

SINGLE ENDED DEVICE MATCHING

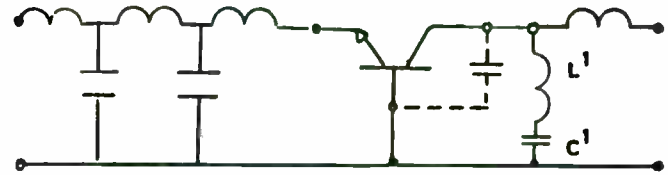


Figure 7.

SPLIT PUSH-PULL DEVICE MATCHING

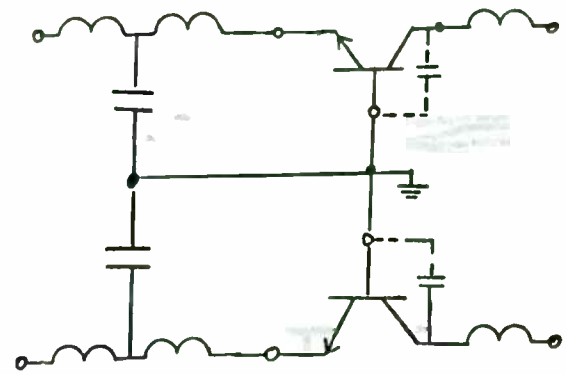
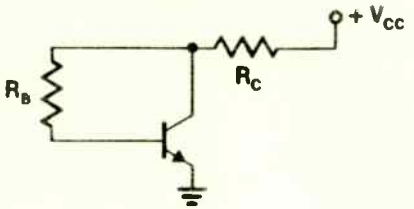


Figure 8

FIGURE 7

VOLTAGE FEEDBACK BIAS



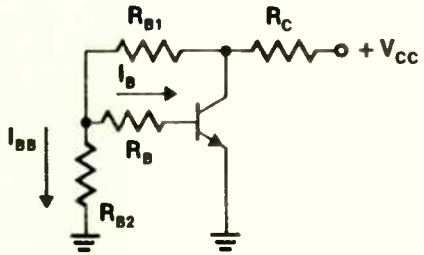
- $I_C = \dfrac{h_{FE}(V_{CC} - V_{BE})}{R_B + h_{FE}R_C}$
- $Kh_{FE} = \dfrac{1}{\left(1 + \dfrac{h_{FE}R_C}{R_B}\right)}$
- $KV_{BE} = \dfrac{1}{\left(1 - \dfrac{V_{CC}}{V_{BE}}\right)}$

ADVANTAGE: SAME AS FIXED BIAS, PLUS BETTER TEMPERATURE STABILITY

DISADVANTAGE: A HIGH R_C/R_B RATIO IMPROVES Kh_{FE}, BUT LOW VALUES OF R_B ARE DIFFICULT TO ACHIEVE

FIGURE 8

VOLTAGE FEEDBACK AND CONSTANT BASE CURRENT SOURCE



- $I_C = h_{FE}\left[\dfrac{-V'_{BE}A - R_{B2}V_{CC}}{R_BA + R_{B2}(h_{FE}R_C + R_C + R_{B1})}\right]$
- $KV_{BE} = \dfrac{1}{\left(1 - \dfrac{V_{BB}}{V'_{BE}}\right)}$

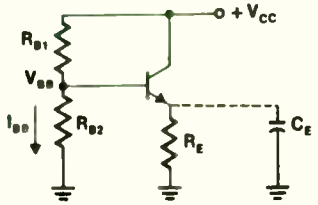
Where: $A = R_{B1} + R_{B2} + R_C$

ADVANTAGE: SAME AS VOLTAGE FEEDBACK PLUS CAN BE MADE h_{FE} INSENSITIVE BY SELECTING $I_{BB} \gg I_B$

DISADVANTAGE: MORE PARTS

FIGURE 9

EMITTER RESISTOR FEEDBACK



- $I_C = \dfrac{(V_{BB} - V'_{BE})h_{FE}}{h_{FE}R_E + R_B}$
- $Kh_{FE} = \dfrac{1}{\left[1 + \dfrac{h_{FE}R_E}{R_B}\right]}$
- $KV'_{BE} = \dfrac{1}{\left[1 - \dfrac{V_{BB}}{V'_{BE}}\right]}$, $SV'_{BE} = \dfrac{-1}{R_E}$

Where: $R_B = R_{B1} \parallel R_{B2}$

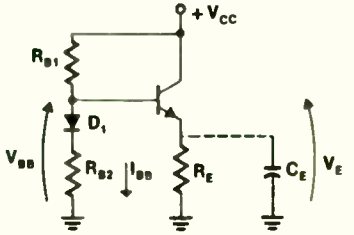
$V_{BB} = \left[\dfrac{R_{B2}}{R_{B1} + R_{B2}}\right] V_{CC}$

ADVANTAGE: VERY STABLE WHEN $h_{FE}R_E \gg R_B$, FEW PARTS

DISADVANTAGE: ADDED INDUCTANCE CAUSED BY R_E AND C_E

FIGURE 10

DIODE TEMPERATURE COMPENSATION



- $SV_{BE} = \dfrac{-1}{R_E\left(1 + \dfrac{R_{B1}}{R_{B2}}\right)}$
- $V_E = V_{BB} - V_{BE}$

$$= \frac{R_{B2}}{R_{B1} + R_{B2}} V_{CC} + \left[\frac{R_{B1}}{R_{B1} + R_{B2}} V_D - V_{BE}\right]$$

- FOR TEMPERATURE INDEPENDANCE OF I_C VS V_{BE} THEN:

$$\left[\frac{R_{B1}}{R_{B1} + R_{B2}} V_D - V_{BE}\right] = 0$$

THEN:

$$V_E = \frac{R_{B2}}{R_{B1} + R_{B2}} V_{CC}$$

ADVANTAGE: STABILIZES I_C AGAINST V_{BE} CHANGES

DISADVANTAGE: EMITTER NOT GROUNDED, REQUIRES MORE PARTS

THE PACKAGE

USED FOR THE PUSH-PULL PAIR

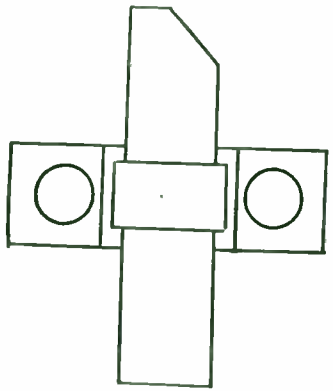


Figure 9

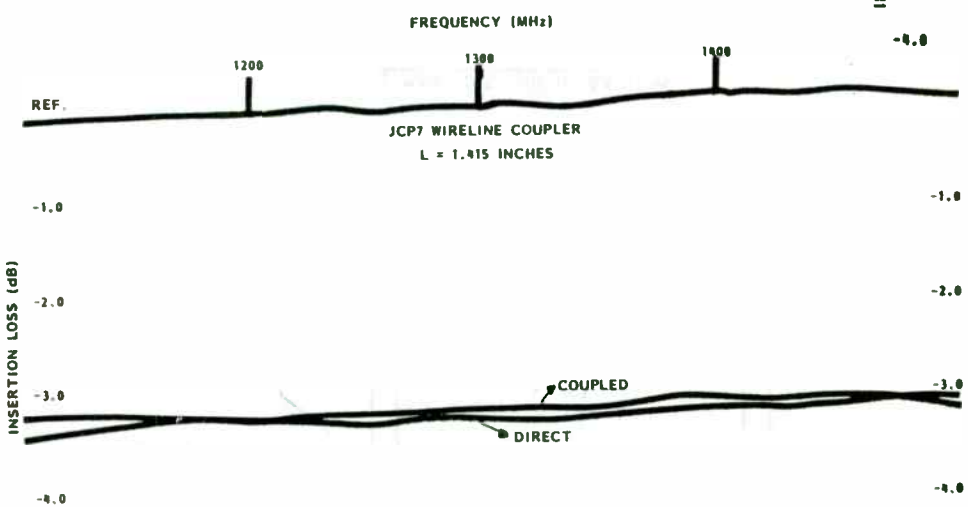
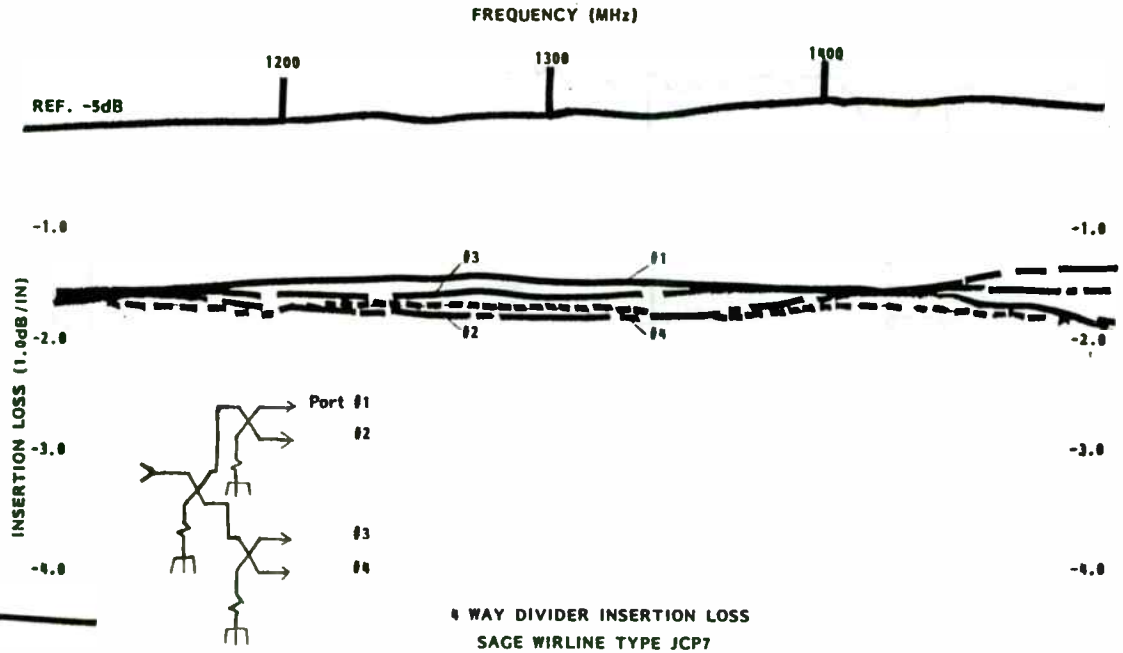


FIGURE 10

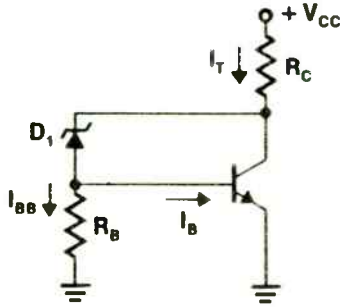


4 WAY DIVIDER INSERTION LOSS
SAGE WIRLINE TYPE JCP7
LENGTH = 1.450 INCHES

FIGURE 11

FIGURE 11

ZENER DIODE BIAS

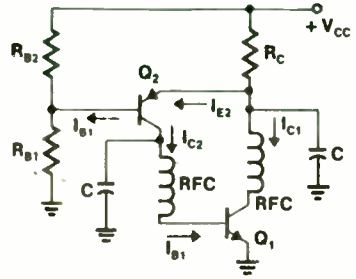


- $V_Z = V_{CE} - V'_{BE}$
- $R_C = \dfrac{V_{CC} - V_{CE}}{I_T}$
- $R_B = \dfrac{V'_{BE}}{I_{BB}}$

ADVANTAGE: EMITTER GROUNDED MORE STABLE THAN WITH A RESISTOR IN PLACE OF THE ZENER
DISADVANTAGE: NOISY

FIGURE 12

ACTIVE BIAS CIRCUIT



- $I_{C1} = \dfrac{h_{FE1}\left[\dfrac{R_{B2}}{R_{B1}+R_{B2}} V_{CC} - V'_{BE2}\right]}{(1+h_{FE1})R_C + R_B/(1+h_{FE2})}$

WHERE: $R_B = R_{B1} \| R_{B2}$

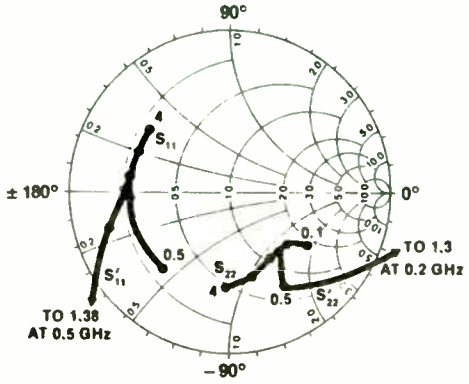
- If $(1+h_{FE1})R_C > \dfrac{R_B}{(1+h_{FE2})}$ THEN

- $I_{C1} \approx \dfrac{h_{FE1}}{(1+h_{FE1})}\left[\dfrac{\dfrac{R_{B2}}{R_{B1}+R_{B2}} V_{CC} - V'_{BE2}}{R_C}\right]$

ADVANTAGE: EMITTER GROUNDED, VERY STABLE, LOW POWER CONSUMPTION
DISADVANTAGE: USES THE GREATEST NUMBER OF PARTS, LOW FREQUENCY OSCILLATIONS POSSIBLE

FIGURE 13

EFFECT OF POOR EMITTER RESISTOR BYPASS



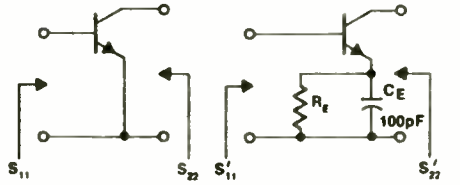
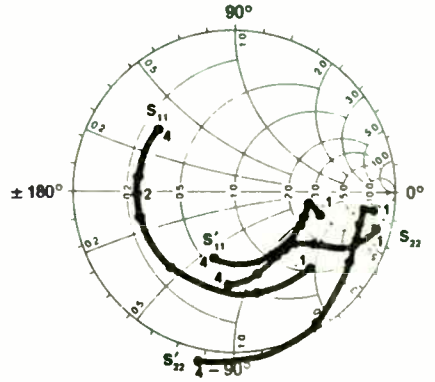
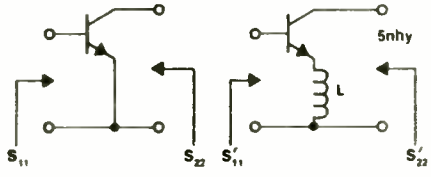


FIGURE 14

EFFECT OF EMITTER INDUCTANCE





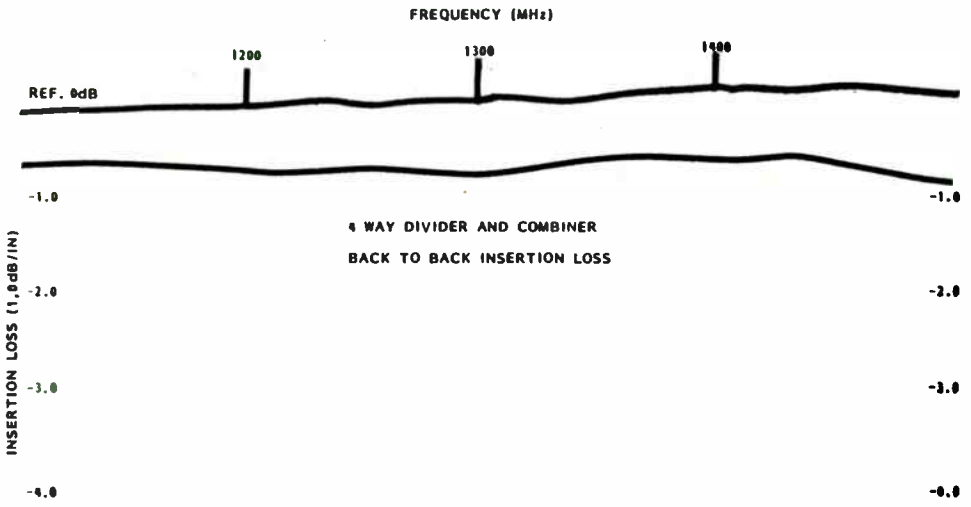
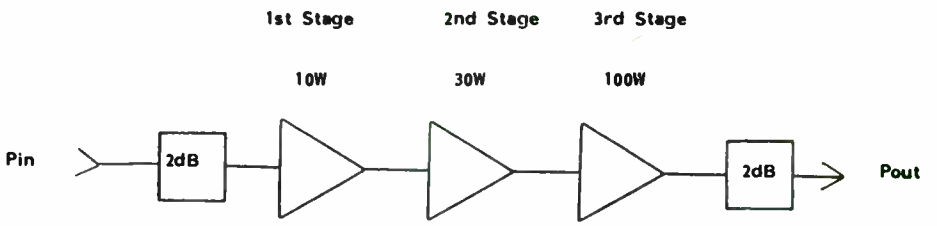


FIGURE 12



BLOCK DIAGRAM LOW LEVEL DRIVER

Figure 13

"THE POOR MAN'S ENGINEERING WORK STATION"
or
"CHEAP CAD"

Richard B. Kolbly, PE

RF TECHNOLOGY EXPO 86

January 30 - February 1, 1986
Anaheim, California

THE POOR MAN'S ENGINEERING WORK STATION

by
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INTRODUCTION

The current literature is full of discussion of the new "Engineering Work Station" or facilities for Computer-Aided Design (CAD). The working RF design engineer reads of these devices with great anticipation, but soon realizes that these are beyond the normal means of a limited personal or engineering budget. Terms like "silicon compiler" and "gate array design" and "standard cells" are resplendent in the literature. Most working engineers probably will not design integrated circuits or semicustom integrated circuits. The purpose of this paper is to show that the working-level RF design engineer, on a limited budget, can provide an effective facility to simplify his engineering duties.

As a practical matter, few companies are going to allocate tens of thousands of dollars to individual engineers unless an immediate increase in productivity can be shown. It has been my experience that if a computer is not immediately available it loses a great deal of its functionality. If we have to sign up or go across the hall (or across the plant!) to use a computer, we are likely not to bother, and either rely on our experience or just "SWAG" it. Since most companies are unwilling or unable to supply a personal computer to each working engineer who desires one, it is up to each of us to provide our own computational resources, just as we did with slide rules and calculators. This paper will show how to use the "low end" home and personal

computers to accomplish most of the computational tasks that are required. By using our experience and intelligence in an interactive manner, we can reduce significantly our design "work load" and produce better products in less time.

SOME DEFINITIONS:

Engineering workstation: A collection of equipment that allows the engineer to design and test circuits. For the purpose of this paper, the engineering workstation is a computer-equipped location where a design engineer will spend a significant portion of his work day.

Personal computer: A computer that is immediately available to an individual, of fairly low cost and relatively low processing power. This paper shall be limited to those computers that fall within the normal range of discretionary income for individuals, in general less that two thousand dollars.

Working engineer: The engineer whose primary task is to produce designs. This is the individual who does not have significant personnel or programmatic management duties.

HARDWARE:

For purposes of comparision, lets see what hardware might be availble to accomplish our needs. Just as most of us have some form of personal transportation, we shall have to have some sort of personal "computing engine".

Similar to the small motorcycles, there are the "home computers", such as the Commodore 64's and the Atari 800XL. With a little judicious shopping, these can be found for less that a hundred dollars. Although these are definitely in the class of "motorcycle" computers, they still have 64 kilobytes of memo and a built-in BASIC interpter. A low-cost computer is ve capable of doing sophisticated engineering analysis - includi using the Method of Moments to calculate wire antenna inp impedance [1]. All of the examples in this paper can be modifi to operate on these little "home computers", such as the Ata with a minimum of effort.

A more typical "personal engineering computer" (PEC) cou be desicribed as having 64K or more of memory, dual disk driv and operating under either the 8-bit CP/M operating system or t 16-bit MS-DOS operating system. A computer such as this wi represent an investment of something between $600 and $20 dollars, depending on how hard one is willing to shop. C course, it is possible to spend more, but the purpose of thi paper is to show how computers that can be purchased by a individual engineer or a tight departmental budget can d significant work.

SYSTEM SOFTWARE:

To operate any computer, you will need a certain amount o programs, or software. We have already mentioned the operatin system, in most cases either CP/M or MS-DOS (or one of thei close relatives). Between these two operating systems most o the personal computers are covered. This operating syste software is generally provided with the computer, and is used t provide basic file handling and program loading.

In addition to the operating system or file handler, yo need some sort of 'translator'. Although for many years FORTRA was widely used, it is not as readily available for persona

THE BASICS OF R. F. POWER AMPLIFIER DESIGN

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What I hope to do in this paper is to provide a basic idea of why RF power amplifier schematics look the way they do. The examplea used are solid atate 2 meter communications amplifiera. A frequency high enough to illustrate some points and low enough to use discrete components. We won't cover transmisaion lines, cavities, etc..

With low priced personal computers and low cost design software, you have to be foolish not to be using a computer for your design work. However, I will intentionally ignore computer design programs. Design programs present an interesting paradox. If you are familiar with designing amplifiers, they allow great insight into an optimum design as they allow you to run through and compare many designs quickly. On the other hand, if you are not familiar with the design process, they can mask what is going on. I am assuming you wouldn't be listening to a basic presentation, such aa thia, if you were already familiar with the design process and, hence, am ignoring computers.

We will not discuss "S" parameters, or the other tools for gain and stability calculations. Some people say such parameters are not useful for power amplifiers. I feel they are quite useful, but will not go into them in this paper. They are beyond the scope of this basic discussion and the subject is treated extensively in the literature [1,2,3,4,5] on small signal amplifiers. The techniques are the same for power amplifiers.

And, wonder of wonders, I won't even mention the Smith chart (Although I think I just did).

To begin, what is an amplifier? For our purposes, an amplifier is an assembly of components using input RF power to convert a source of DC power into output RF power of greater magnitude than the input RF power. This is not a definitive definition, so don't worry about the nuances of the wording.

The important parts of a basic amplifier are shown in Figure 1. Let's take a few examples of typical amplifiers and build some schematics. We will start with a 146 MHz amplifier which we want to deliver 50 Watts into a 50 Ohm load, work off a 13.0 Volt supply, and use an FET as a grounded source amplifier.

First, lets consider the output network.

Using the basic $E = \sqrt{PR}$ (and incidentally, we are not going to use formulas that are much more complex than this), we find that to deliver 50 Watts to 50 Ohms, we must supply 50 Volts rms. Obviously, in order to get 50 volts rms from the 13.0 volt supply, the output network must act as a step-up voltage transformer. To state it a bit differently, the output network must transform the 50 Ohm load so that the transistor sees a lower impedance.

If we asaume the matching network includes tuned circuits of reasonable Q, the waveform of Figure 2 is is the maximum that we will see at the output (drain) of the FET. The output will swing from the supply voltage toward zero down to some minimum voltage limited by the transistor and will swing above the supply voltage approximately the same amount. If, for the sake of this example, we assume that E_{sat} is 3 Volts, we have a maximum voltage of 10 Volts peak (13 V. - 3 V.), or about 7 Volts rms. $E_{rms}=E_{peak}/\sqrt{2}$. To get our 50

computers as BASIC. In most cases, programs written in FORTRAN can be translated to BASIC with a minimum of effort. The only snag in this process (well-known to RF designers) is the lack of COMPLEX data types in BASIC. If BASIC had complex data types, it would be a much more useful language for us. Usually BASIC has been provided with your computer - it might be called MBASIC, GWBASIC, BASICA, APPLESOFT BASIC, etc. but they all tend to be variations of Microsoft's MBASIC V5.2 which has become a de facto standard for small computer BASIC interpeters. By staying with the Microsoft BASIC and its variants, we are assured of:

1 - Ease of program modification and debugging.

2 - A high degree of portability between machines.

3 - A common data file structure that many programs can use.

So far we have discussed the "system software" that comes with each computer. We still cannot do any useful design work until we have applications software - those programs that actually calculate and display the information we use. Where are these programs coming from? As all of you are undoubtedly aware, RF design programs are not as popular as word processors. Yet there are many sources of low cost or free software that are directly applicable or easily modified to our needs.

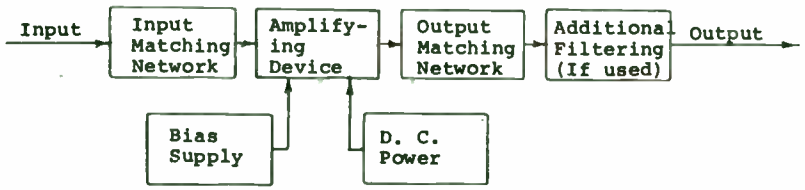
Low- or no-cost software is available from a variety of sources. Most of the programs I use regularly in my duties as a practicing RF engineer have been published in technical magazines. RF Design Magazine is one of the better sources of programs. Other good sources include EDN, Ham Radio, Microwave Journal, etc. The bibliography has several references. The important thing to remember is (to quote Tom Lehr) - "let nothing escape your eyes..." Read or scan as many of the publications as possible and start a clipping file.

Another good source of programs is in manufacturer's application notes. These notes are generally tailored to a specific machine, but I have found them to be easily adopted to other computers. As an example, the now obsolete Hewlett-Packard 9100-series of desktop calculators had excellent discussions of programs that could be used for filter design, transmission line calculations, etc and were easily adapted to BASIC. These programs (and calculators!) often turn up at flea markets, swap meets and house organ classified advertising.

The US Government and universities have a number of catalogs available that describe programs that have been written and are available for a small fee or free. CAED, an excellent microstrip design package (written in FORTRAN) is availble from the US Government [2]. Again, most of these programs are tailored to a specific machine or application, but many of them have wide application. A classic example is the circuit analysis program, SPICE, written and distributed by the University of California [3]. It take a little snooping to find these sources, but other engineers and libraries can be a big help.

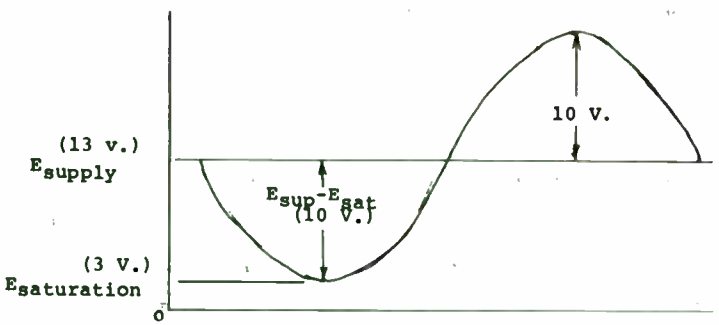
A few companies provide low-cost (defined as under $100) software for engineers. Others, with their full-page advertisements, make us envious, but in general, they tend to be out of range to our budgets. All of us would like to have a program like SPICE2 running on our computers, but cannot justify

Figure 1



BASIC R. F. POWER AMPLIFIER

Figure 2



DRAIN WAVEFORM - MAXIMUM OUTPUT

Watts, the transistor must see an impedance of:

$$R_L = \frac{E_{rms}^2}{P} = \frac{(E_{peak}/\sqrt{2})^2}{P} = \frac{E_{peak}^2}{2P} = \frac{(E_{SUPPLY}-E_{sat})^2}{2P} = \frac{(13-3)^2}{2 \cdot 50} = 1\,\Omega \qquad 1)$$

Thus, the output matching network must transform the 50 Ohms load down to present 1 Ohm to the transistor. If this were an audio amplifier, the output matching network might be a 1 Ohm to 50 Ohm transformer. Because we are designing an amplifier for communications purposes, we will want to add some filtering to the network and we can use narrow band networks.

Note that, other than to consider a saturation voltage, we haven't paid any attention to the transistor. We haven't worried whether it was bi-polar, an FET, or made out of "molded muckite". We have simply said that to get 50 Watts from a 10 Volt peak sine wave we have to present it with a load of 1 Ohm.

Also note that we haven't tried to "match" its output impedance. Again, we simply determined that with a 13 Volt supply, and a device with a saturation voltage of 3 Volts, the transistor must "see" 1 Ohm to deliver 50 Watts.

There is a common misconception that power amplifiers are designed to "match" the output impedance of the transistor; or to us sophisticated RF types, you need a network that presents a "complex conjucate match".

This is not true, and is not true in most power work. If you want to build a toaster, you select the resistance of the heating element to draw the desired power at the voltage available. You do not select a resistance to "match" the source impedance of the power company generators. You would sure brown your toast in a hurry if you did.

Of course, we are not really ignoring the transistor. We are assuming that the device chosen is satisfactory for the supply voltage, has sufficient gain

the cost of many hundreds or thousands of dollars. A more acceptable substitute are "canned" programs such as ACNAP and DCNAP [4,5] from BV Engineering. These companies provide programs at reasonable cost for our requirements. One company, DYNACOMP [6], provides programs in BASIC source form, so they can be modified for a specific application.

The microcomputer publishing industry has been publishing hundreds of books on using your personal computer for everything from cat breeding to sports handicapping. There are several volumes available of programs for engineering computing, but in general, I have found these not to be of much use. A few exceptions are worth noting. F.R. Ruckdeschel's BASIC Scientific Subroutines (Volumes I & II) [7] should be in every engineer's library. These books are a collection of well-documented programs for many of the mathematical operations that are required for serious engineering work. These programs and subroutines are presented with unique line numbers so they can be used directly - a helpful feature. These subroutines can be purchased already on disk at a nominal cost [8]. Another very useful publication is Antenna Design using Personal Computers by David S. Pozar [9]. This little xpublication is a collection of programs for path analysis, transmission line and antenna design, with a good explanation of the theory involved and a comparison of results with calculated values. Also, these programs are availble on disk [10]. A last example of an excellent publication for the engineer engaged in computer-aided design is Circuit Design using Personal Computers by T. R. Cuthbert [11]. This volume has numerous programs for design (as opposed to analysis) for the small computer, and includes an excellent discussion of optimization, which is often neglected in CAD articles and publications.

A final source of suitable applications software for our "poor man's work station" is ourselves. Although it takes a bit of effort, writing a program to solve a particular design problem can be a fun. Possibly a fellow engineer has a similar requirement to yours and already has a suitable program or one that can be modified. An example of "home brew" engineering programs are included in Appendix A of this paper. Both were written by members of the San Bernardino Microwave Society to solve a specific application, and have been widely distributed and modified by others. Most engineers that write these programs are happy to share them, so always ask, and always give credit where credit is due. In general, these are not the slick finished products that would be available from publishers, but are useful.

PRACTICAL CONSIDERATIONS:

Now that we have discussed the sources of programs that are availbe to the RF design engineer, let's discuss some of the problems we can encounter.

First of all, just because all BASIC programs are similar, they are not identical! In general, when getting a program from another machine, it is necessary to make some minor conversions. Such things as file opening and closing, data formats, and minor syntax variations can drive you up the wall. Multiple statement delimiters, "extra" functions, etc., all have to be resolved and

for the application at the operating frequency, can deliver the required current, has sufficient dissipation capabilities and other parameters to assure adequate operating life, etc. In fact, long before you start with the specifics of a particular design, the chances are that you have spent many hours with data sheets deciding which devices are suitable for the application.

Also, the transistor input and output usually appears reactive and our networks will have to account for these reactances.

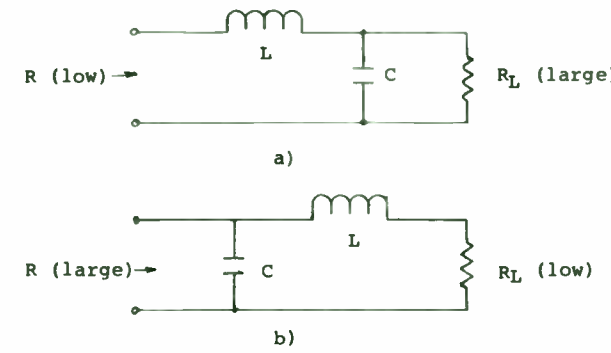
Back to the output network. There are many networks that will transform 50 Ohms to 1 Ohm, and the literature abounds with analyses [6,7,8,9,10,11,12,13,14] of them. For this example I will use a pair of basic "L" networks.

The "L' network (Figure 3a or 3b for the low-pass version and Figure 4a or 4b for the high pass), is a basic building block used in many situations. Although well covered in the literature, we will quickly derive the applicable formulas. I would like to take the time because it is such a basic building block. We will be using the circuit of Figure 3a as our example.

We picked a low pass version because in a well designed amplifier the only spurious signals created by the amplifier are harmonics. Why not use the matching network to help in their removal? If we are using the network to match unequal impedances (R_s not equal to R_p) the response of the network is peaked and a perfect match only occurs at the peak of the response. If the Q is low enough, the bandwidth can be reasonably large.

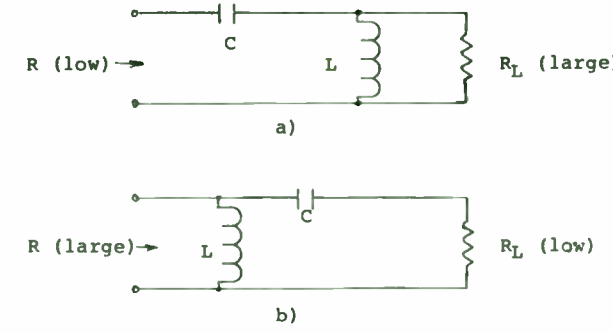
For zero insertion loss, the loaded Q of the series arm must equal the loaded Q of the shunt arm at the peak frequency.

Figure 3



BASIC "L" NETWORK - LOW-PASS CONFIGURATION

Figure 4



BASIC "L" NETWORK - HIGH-PASS CONFIGURATION

corrected. If you are getting a disk-based program from a different (foreign) machine, try to get the program in ASCII format. As a practical matter, I save all of my programs in ASCII instead of the more compact binary format, just to simplify the conversion between different machines. A side benefit of this method of storage allows you to edit and print the source listings with an editor or word processor.

If you are writing programs, try to include provision for storing and loading infomation from disk - this will save you the trouble of typing a circuit over and over. A little effort at this stage can make a program much more professional and easier to use. Data files can be designed that can be used by many programs. I use the format of printing to file the independent variable, followed by dependent variables, e.g. frequency, real part of impedance, imaginary part of impedance in actual values, such as Hz, ohms, etc. Try to avoid the use of specific multipliers, such as GHz; it is then difficult to use your program in a wide variety of situations. Make an effort to maintain consistency whenever possible. When dealing with arrays of data, such as network analysis programs, data files should have a header that specifies the dimensions of the array. It is very easy to forget these parameters when you are working with many different projects.

SOME EXAMPLES

Network Analysis: One of the recurring tasks for the RF design engineer is predicting the performance of a circuit and modifying it until it meets requirements. The normal process is to rely on our experience, etc. to get an initial design, breadboard, measure performance, and "tweak and trim" until the desired performance is achieved. Computer aided design is a much more difficult task than computer-aided analysis. In design, we input the desired performance and the output is a circuit. In analysis, the circuit is input and the output is performance. Most small computer programs use an input circuit and calculate performance. Computer -aided design programs are available [12] but I have found that convergence on an acceptable design by interaction is a faster and more comfortable approach.

As an example, the process for design and evaluation of a simple diplexer will be demonstrated. This diplexer is to split the FM broadcast band (88-108 MHz) and the 2-meter amateur radio band (144-148 MHz) from a common source. Since this is intended for very low-cost applications (mobile reception) we decide to use a simple set of Butterworth filter circuits (Figure 1). After coming up with this "quick and dirty" circuit, we load NET85.ASC (Appendix B) and analyze the circuit over the bands of interest. The results of this anaylsis are shown in Figure 2. Inspection of this data indicates that fabrication could be simplified by using standard circuit elements shown in Figure 3. Continuing to work with NET85, we add these changes and obtain the performance shown in Figure 4. Since our only intent is to build one of these for the car belonging to the president's son, we conclude this is an adequate design.

The NET85 program is derived from a program that was originally described in EDN magazine[13]. It was written in a BASIC-like language and has been translated to GWBASIC (Appendix

The design of a matching network lies in our ability to represent a series combination of components as an equivalent parallel combination, and vice versa (Fig. 5). At the conversion frequency, and it is valid at only one frequency, the series and parallel equivalents will have the same impedance. For Qs greater than one, the series equivalent resistance will always be smaller than the parallel equivalent resistance.

There are many ways to derive the proper values, but we will rely on the fact that the Qs must be equal. First, some familiar formulas.

For parallel components, $Q = \frac{R_p}{X_p}$ 2)

For series components, $Q = \frac{X_s}{R}$ 3)

The standard series to parallel transformation formulas, based on Q, are:

$$X_p = \left(1 + \frac{1}{Q^2}\right) X_s \quad 4)$$

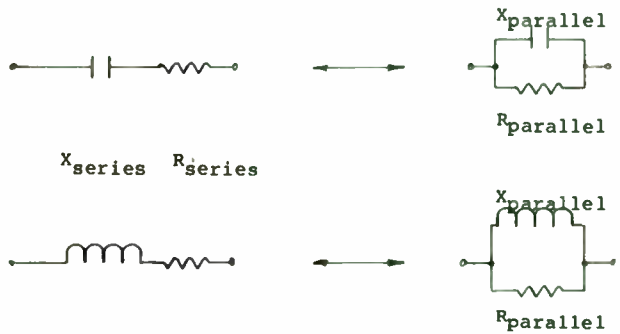
$$R_p = (1 + Q^2) R_s \quad 5)$$

Note that the Q used here is not the total Q of the network but rather the Q of just the two components being considered. In the case of an L network, with the Q of the series arm the same as the Q of the parallel arm, the network Q is 1/2 the Q of each arm, when matched at each end.

In our particular case we have the situation of Figure 6a. We are trying to make a 50 Ohm load appear to be 1 Ohm.

Place a capacitor across the load as in 6b. At any single frequency we can

Figure 5



SERIES / PARALLEL TRANSFORMS

B). The program has been extensively modified to allow for creation and saving of the program data. Examples of input and output data files are also shown in Appendix B. The files are then plotted on a low-cost commercial plotting package [14].

EXAMPLE II: MICROWAVE ANTENNA DESIGN

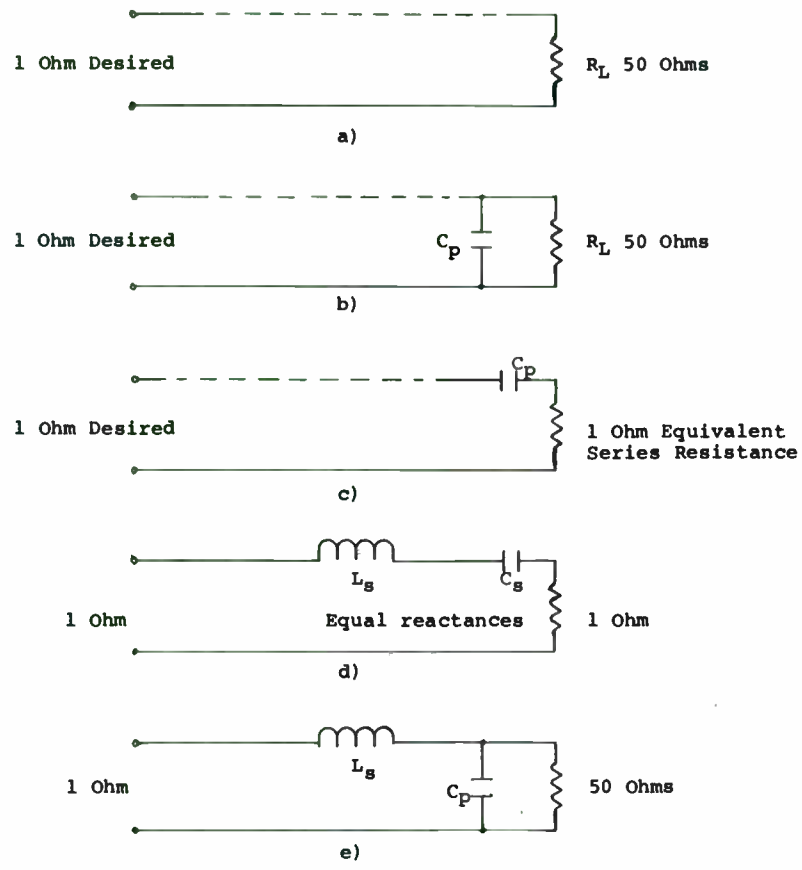
One of the more tedious tasks facing engineers is the occasional design of an antenna. As RF engineers we are often called to come up with at least a rough design for an antenna (How big a dish do we need to receive OSCAR VII?). Appendix B2 has a straight-forward program to design a suitable Cassegrain or prime-focus reflector antenna. Once a suitable design is reached, other BASIC language programs can be used for more detailed analysis [9]. The results can then be presented by using one of many available graphing or plotting programs [14]. When using these relatively simple programs it is important to remember that most of them are based on geometric optic considerations, so do not compensate for edge effects, etc., and will likely provide incorrect answers for small antennas. In general, the higher the antenna gain, the easier it is to predict its performance. There are some programs available [9] that go beyond geometric considerations, but large physical optics or method of moment solutions tend to be beyond personal computers. However, it may be possible to reduce a fairly complex program program to parts that will run on a personal computer. The computation-intensive parts, such as the solution of the complex matricies, could be allowed to run overnight. Most of these programs are availble in FORTRAN [15] and could be loaded and compiled on a MS-DOS based PC, as there are FORTRAN compilers available that can deal with COMPLEX data types. It is possible to translate these programs to BASIC, but it is left as an excercise to the reader to accomplish this.

OTHER APPLICATIONS:

The duties of the RF designer generally include a large portion of 'administrative' duties. These include reports, memoranda, statements of work, project tracking, procurement documents, etc. Most of us find these tasks at best a burden and at worst an imposition. Until management sees fit to provide us with adequate administrative and paraprofessional support, these tasks will remain with us. Our "poor man's engineering work station' can be pressed into service to support these functions. By including some form of text editor or word processing software, reports and memos can be generated quickly and in a more readable form. By relieving the work of preparing documents, I have found that using a small desktop computer increases my engineering productivity significantly. In addition, most engineers would rather design than perform administrative tasks, so the editing function alone makes a personal desktop computer worthwhile.

Procurement actions, schedules, parts and wire lists, etc. can be efficiently maintained using one of the many microcomputer data base managers. As an example, I used a data base on an old microcomputer to maintain a wire list for a large transmitter. By simply inquiring the disk, I could get a list of all the locations a particular signal could be found or all signals on a

Figure 6



DERIVATION OF BASIC "L" NETWORK

replace the combination of parallel capacitor and load with a series equivalent. If the right value of parallel capacitor was used, the equivalent series resistor can be made to be 1 Ohm. (Figure 6c)

If we now place an inductor in series, which has the same reactance magnitude as the computed series capacitor, the reactances will cancel and the impedance looking into the network will be our desired 1 Ohm. (Figure 6d)

Transforming the output section back to a parallel circuit, we have the finished network of Figure 6e. Now lets put some numbers on things. Rearranging series to parallel transformation formula 5), above, and solving for Q, we have.

$$Q = \sqrt{\frac{R_p}{R_s} - 1} \qquad 6)$$

In our case, $$Q = \sqrt{\frac{50}{1} - 1} = 7 \qquad 7)$$

From 2) the reactance of the parallel capacitor is,

$$X_p = \frac{R_p}{Q} = \frac{50}{7} = -j\,7.14\,\Omega \qquad 8)$$

And, from 3), the reactance of the series inductor is,

$$X_s = R_s \cdot Q = 1 \cdot 7 = j\,7\,\Omega \qquad 9)$$

Note that the reactance of the series inductor is not the same as that of the parallel capacitor; although in high Q cases it is often considered so for convenience.

particular connector or terminal block.

These applications are well known, and it is not my intention to go into great detail, but sometimes we overlook the 'support functions' that take up so much time. If we can develop more time for design work, it enables us to be more effective as engineers.

CONCLUSIONS:

This paper has presented one engineer's view of the use of obsolescent technology to make his job easier and more productive. As the cost of computing power continues to decline, we will have the power of supermini computers available to us. In the meantime, the latest technology may not be available. I have tried to show with a few examples how we can use existing low-end hardware combined with relatively simple software to greatly speed up our efforts as design engineers. The key is the immediate availability of a computer. It is better to have an old, slow machine immediately availble to us for a quick evaluation, than a large mainframe that we have to schedule well in advance. The programs and examples I have presented are not necessarily the most efficient or accurate. They are programs that I have used and refined over the years to accomplish specific tasks. There are many things that can be done by the user to make these programs more efficent or easier to use. As an example, an option could easily by added to allow input to NET85.ASC as reactance values, rather than component values. This change would be very helpful, but I never "got around tuit". The bibliography lists several sources of software, but I make no claims for its accuracy or completeness.

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[1] Antenna Design using Personal Computers by David S. Pozar, Ph.D. Artech House, Inc. 888 Washington Street Dedham, Massachusetts 02026

[2] Design of Microstrip Components by Computer, by Terry S. Cisco NASA CR-1982 1972.

[3] SPICE2G.6 College of Engineering, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley 94720

[4] BV Engineering 2200 Business Way, Suite 207 Riverside, CA
[5] 92501 (714) 781-0252

[6] DYNACOMP, Inc. 6 Rippingale Road Pittsford, NY 14534 (716) 586-7579

[7] BASIC SCIENTIFIC SUBROUTINES by F.R. Ruckdeschel McGraw Hill Publications Co. 1981 (Volumes 1 & 2)

[8] DYNACOMP, op. cit.

[9] Pozar, David S. op. cit.

[10] Artech House, Inc. Publication B84139A.

[11] Circuit Design Using Personal Computers by Thomas R. Cuthbert, Jr. John Wiley & Sons, 1983

[12] Cuthbert, op. cit.

[13] EDN Magazine February 14, 1981 pp 126-133

[14] PCPLOT2, published by BV Engineering, op. cit.

[15] A User's Manual for Electromagnetic Surface Patch (ESP) Code: Version II - Polygonal Plates and Wires by E.H. Newman and P. Alexandropolos The Ohio State University Electroscience Laboratory, Department of Electrical Engineering Columbus, Ohio 43212 September 1983.

The Q of the network is 1/2 the Q of either branch, or,

$$Q_{total} = Q_s/2 = Q_p/2 = 7/2 = 3.5$$

Lets calculate the component values at our selected operating frequency of 146 MHz.

$$C = \frac{1}{\omega X_C} = \frac{1}{2\pi f X_C} = \frac{1}{2\pi \cdot 146 \cdot 10^6 \cdot 7.14} = 153 pF \qquad 10)$$

$$L = \frac{X_L}{\omega} = \frac{X_L}{2\pi f} = \frac{7}{2 \cdot \pi \cdot 146 \cdot 10^6} = 7.6\ nH \qquad 11)$$

Note that the Q was determined only by the impedance ratio and the values were determined by Q, impedances and frequency. This is one disadvantage of the simple L network; we can't choose Q. Two elements simply do not give us enough degrees of freedom. By making our network a three element network, such as the T and π we can, with some limitations, design for a specific Q.

Four element networks give us one more degree of freedom and are often used for broadband matching. One version of a four element network is two cascaded L sections; transforming the load to some intermediate value with one section and matching the intermediate value to the final impedance with the second. Each section has a smaller step up and will operate at lower Q. Maximum bandwidth is achieved if the Q of each is the same. This occurs when:

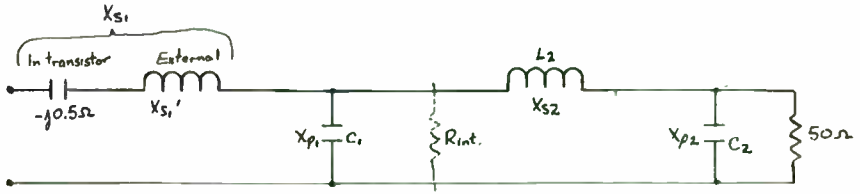
$$R_{intermediate} = \sqrt{R_{Smaller} \times R_{larger}} \qquad 12)$$

The process can be continued with three, four, or more, sections; although little is generally gained with more than three.

Lets recalculate our output network as a two section L network. For convenience, I have summarized the calculations in Figure 7. I have added a

Figure 7

$$R_L = \frac{(V_{DS} - V_{SAT})^2}{2 P_{out}} = \frac{(13-3)^2}{2 \cdot 50} = 1\Omega \quad \text{for } P_{out} = 50W.$$



For maximum bandwidth $R = \sqrt{R_s R_L} = \sqrt{1 \cdot 50} \approx 7.07\Omega$

$$Q = Q_1 = Q_2 = \sqrt{\frac{R_{int}}{R_m} - 1} = \sqrt{\frac{7.07}{1} - 1} = 2.46$$

$X_{S1} = Q \cdot R_s = 2.46 \cdot 1 = 2.46\Omega$ $X_{S1}' = 2.46 + 0.5 = 2.96\Omega$	$L_1 = \frac{X_{S1}'}{\omega} = \frac{2.96}{2\cdot\pi\cdot 146\cdot 10^6} = 3.2nH$
$X_{P1} = \frac{R_{int}}{Q} = 2.86\Omega$	$C_1 = \frac{1}{\omega X_{P1}} = 381pF$
$X_{S2} = Q R_{int.} = 17.4\Omega$	$L_2 = \frac{X_{S2}}{\omega} = 18.9nH$
$X_{P2} = \frac{50}{Q} = 20.3\Omega$	$C_2 = \frac{1}{\omega X_{P2}} = 53.6pF$

146 MHz OUTPUT MATCHING NETWORK USING TWIN "L" NETWORKS

APPENDIX A

USER-WRITTEN BASIC DESIGN PROGRAMS

A.1 DISH.ASC This program was written by Chuck Swedblom of the San Bernardino Microwave Society for design and analysis of Cassegrain-reflector antennas. It is based on ray-trace optics.

```
10 '
20 ' PARABOLIC ANTENNA DESIGN PROGRAM
30 '
40 ' Written by C. Swedblom, WA6EXV January 13, 1981 (not Friday)
50 '
60 ' Revised: March 26, 1981
70 '
80 'Modified for Microsoft Basic by R. Kolbly, K6HIJ April 3, 1981
90 '  (Friday after a Society Meeting!)
100 '
110 CLS$=CHR$(27)+"E"
120 PI=3.1415928#
130 DIM X(100)
140  M$="###.##"
150  D$="###"
160 PRINT CLS$
170 PRINT "Select area of interest"
180 PRINT
190 PRINT "     1.  Calculate f/D and Gain of a Parabolic Dish."
200 PRINT "     2.  Design Sub Reflector for Cassegrain feed."
210 PRINT "     3.  Return to Basic"
220 INPUT "Your Choice";ME
230 IF ME < 1 THEN 260
240 IF ME > 3 THEN 260
250 ON ME GOTO 290,700,1390
260 PRINT CLS$
270 PRINT "Values between 1 and 3 only!"
280 GOTO 170
290 ' Calculate f/D
300 '
310 PRINT CLS$
320 INPUT "Diameter of the Dish in Inches";DIA
330 PRINT
340 INPUT "Depth of Dish, same units as Diameter";CR
350 PRINT
360 INPUT "Frequency of Interest, in MHz";MHZ
370 PRINT
380 INPUT "Efficency of the Dish in %";EFF
390  FDR=DIA/(16*CR)
400  LAMDA=30000/(2.54*MHZ)
410  GAIN=(PI*DIA/LAMDA)^2*EFF/100
420  GAIN=10/LOG(10)*LOG(GAIN)
430 '
440 ' Print Results
450 '
460 'INPUT "Port #",N (For output of Chuck's Basic)
470 PRINT CLS$
480 PRINT "             PARABOLIC DISH f/D and GAIN"
490 PRINT "             --------------------------"
500 PRINT:PRINT
510 PRINT "Diameter of the Parabolic Dish.....";
520 PRINT USING M$;DIA;:PRINT " In."
530 PRINT
540 PRINT "The f/D Ratio of the Parabolic Dish...";
550 PRINT USING M$;FDR
560 PRINT
570 PRINT "The Gain of the Parabolic Dish.....";
580 PRINT USING M$;GAIN;:PRINT " dB at ";MHZ;" MHz"
590 PRINT "    with an Efficiency of ...........";
600 PRINT USING D$;EFF;:PRINT " %"
610 '
620 ' Calculate Distance to the focal point
630 '
640  FR=FDR*DIA
650 PRINT
660 PRINT "The distance to the focal point is....";
670 PRINT USING M$;FR;:PRINT " Inches"
680 PRINT:PRINT:PRINT:PRINT:PRINT
690 END
700 '
710 ' Calculate the size and location of a Sub Reflector for a
720 ' Cassegrain fed Parabolic Dish.
730 '
740 PRINT CLS$
750 INPUT "f/D of the Real Dish in Inches";FDR
760 PRINT
770 INPUT "f/D of the Virtual Dish";FDV
780 PRINT
790 INPUT "Diameter of the Real Dish in Inches";DIA
800 PRINT
810 INPUT "Ratio of Sub Ref Dia. to Diameter, not over .3";FSR
820 PRINT
830  FR=FDR*DIA
840  FV=FDV*DIA
850  CR=DIA^2/(16*FR)
860  CV=DIA^2/(16*FV)
870  DSR=DIA*FSR
880  M=DSR*(FR-CR)/DIA
890  L=DSR*(FV-CV)/DIA
900  A=(L+M)/2*(FV-FR)/(FV+FR)
910  E=(L+M)/(2*A)
920  THETA=2*ATN((DIA/2)/(FV-CV))
930  BLOCK=DIA*DIA-DSR*DSR
940  GAINSR=10/LOG(10)*LOG(BLOCK)
950  GAINRE=10/LOG(10)*LOG(DIA*DIA)
960  BLK=GAINRE-GAINSR
970  THETA=THETA*180/PI
980 'output the Data
```

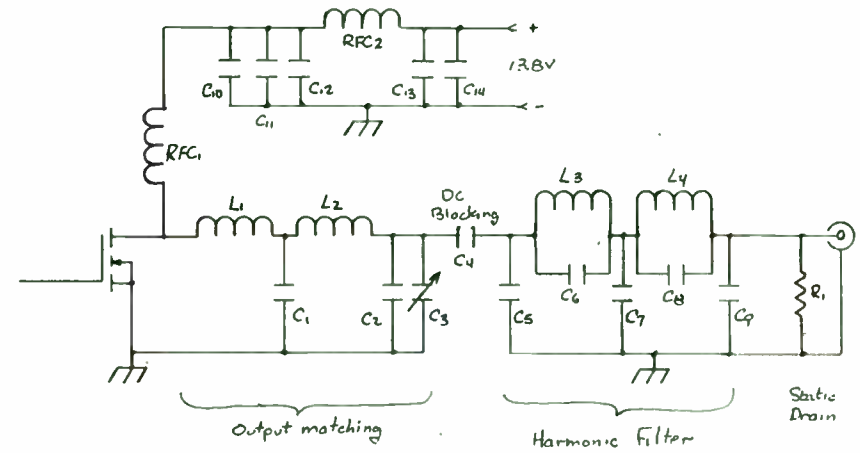
wrinkle and picked an F1260 MOSFET as our device. The data sheet indicates a series equivalent output reactance of -j.5 Ohms at 146 MHz. I absorbed this .5 Ohms by making the first inductor .5 Ohms larger. We could also have handled the reactance by resonating it with a shunt inductor (somewhat inconvenient for DC). At this power level and frequency bi-polar transistor outputs generally look inductive and a shunt C is common.

Figure 8 is a partial schematic showing what the output part of the amplifier we have been discussing might look like.

We are discussing power amplifiers and it might be useful to stop and discuss just what is different when compared to small signal amplifiers. The dividing line between small signal and power amplifiers is a fuzzy one. For example, I used to be very involved with wide dynamic range receiver front ends and when forced to use an RF amplifier might have designed it for over 10 Watts output; yet I considered it a small signal amplifier. On the other hand, I will consider a two Watt intermediate stage in a transmitter chain a power amplifier.

Rather than get bogged down with defining a dividing line, let us say our 50 Watt amplifier is a power amplifier and compare it with small signal amplifiers in the milliwatt range. One apparent difference is the impedance levels brought about by the power level and what this does to the components. For example the input inductor of our example calculates to be 3.2 nH. This is a pretty small inductance and represents a fraction of an inch of PC board trace. When dealing with values this small, simple questions like; where does the transistor tab stop and the inductor begin, become difficult to answer and

Figure 8



SCHEMATIC OF OUTPUT SECTION

```
990 '
1000 '
1010 PRINT CLS$
1020 PRINT  "                PARABOLIC DISH/SUB-REFLECTOR"
1030 PRINT  "                ----------------------------"
1040 PRINT:PRINT
1050 PRINT "Diameter of Dish.............................";
1060 PRINT USING M$;DIA;:PRINT "In."
1070 PRINT "f/D of Real Dish.............................";
1080 PRINT USING M$;FDR
1090 PRINT "f/D of Virtual Dish..........................";
1100 PRINT USING M$;FDV
1110 PRINT "Focal Point of Real Dish.....................";
1120 PRINT USING M$;FR;:PRINT " In."
1130 PRINT "Focal Point of Virtual Dish..................";
1140 PRINT USING M$;FV;:PRINT " In."
1150 PRINT "Diameter of Sub-Reflector....................";
1160 PRINT USING M$;DSR;:PRINT " In."
1170 PRINT "Location of Sub-Reflector....................";
1180 PRINT USING M$;FR-M;:PRINT " Inches from Org."
1190 PRINT "Location of Feed Horn........................";
1200 PRINT USING M$;(FR-M)-L;:PRINT " Inches from Org."
1210 PRINT "Feed Beam Width..............................";
1220 PRINT USING M$;THETA;:PRINT " Deg."
1230 PRINT "Reduction in Gain due to Sub-Reflector.......";
1240 PRINT USING M$;BLK;:PRINT " dB."
1250 PRINT:PRINT:PRINT
1260 '
1270 ' Print X-Y Coordinates of Hyperbolidal Sub-Reflector
1280 '
1290 INPUT "Enter increment for Sub Ref. X-Y Cordinates";INC
1300 PRINT TAB(5);"X-Y Co-ord. for Hyperbolidal Sub-Ref."
1310 PRINT
1320 PRINT TAB(10);"Y-Co-ord.";TAB(28);"X-Co-ord."
1330 PRINT
1340 FOR Y=0 TO DSR/2 STEP INC
1350 X(Y)=SQR(A*A+(Y*Y)/(E*E-1))
1360 Z=X(Y)-X(0)
1370 PRINT TAB(10);:PRINT USING M$;Y;:PRINT TAB(28);
1380 PRINT USING M$;Z
1390 NEXT Y
1400 END
```

A.2 STRIPLIN.ASC This program is for design of microstrip lines

and has been continously refined. Again, it is user-written.

```
10 REM THIS PROGRAM CALCULATES THE WIDTH OF A MICROSTRIP LINE
20 REM FOR A GIVEN IMPEDANCE OF WILL CALCULATE THE IMPEDANCE
30 REM OF A MICROSTRIP LINE OF A GIVEN WIDTH
40 REM
50 REM WRITTEN BY C. SWEDBLOM, WA6EXV 12 JUNE 1979
60 REM MODIFIED BY DICK KOLBLY, K6HIJ 16 SEPT 1979
70 REM DIELECTRIC CONSTANTS ADDED K6HIJ 10 MARCH 1981
80 REM   W=WIDTH OF MICROSTRIP LINE
90 REM   H=THICKNESS OF SUBSTRATE MATERIAL
100 REM   T=THICKNESS OF MICROSTRIP LINE
110 REM  F=FREQUENCY
120 REM  E=DIELECTRIC CONSTANT OF SUBSTRATE MATER
130 REM  E1=DIELECTRIC CONSTANT AT DC
140 REM  E2=DIELECTRIC CONSTANT AT F0
150 REM  Z=CHARACTERISTIC IMPEDANCE OF MICROSTRIP
160 REM  Z1=CHARACTERISTIC IMPEDANCE AT DC
170 REM  Z2=DESIRED IMPEDANCE
180 REM  L=WAVELENGTH
190 REM  D1=IMPEDANCE ERROR FACTOR
200 REM
210 D1=.0001
220 P1=3.141592654
230 PRINT "1 OZ Cu=.0013 in, 2 Oz Cu=.0027"
240 PRINT "(1) AIR             (e=1.00)"
250 PRINT "(2) G10 FIBERGLASS (e=4.80)"
260 PRINT "(3) TEFLON/GLASS    (e=2.55)"
270 PRINT "(4) REXOLITE        (e=2.54)"
280 PRINT "(5) TEFLON          (e=2.10)"
290 PRINT "(6) FORMICA XX      (e=4.04)"
295 PRINT "(7) DUROID          (e=2.23)"
300 INPUT "(8) OTHER";K:IF K=0 OR K=8 THEN 310 ELS
310 INPUT"TYPE OF MATERIAL AND ER";A$,E
320 IF K=1 THEN A$="AIR":E=1!
330 IF K=2 THEN A$="G10":E=4.8
340 IF K=3 THEN A$="TEFLON/FIBERGLASS":E=2.55
350 IF K=3 THEN A$="REXOLITE":E=2.54
360 IF K=5 THEN A$="TEFLON":E=2.1
370 IF K=6 THEN A$="FORMICA XX":E=4.04
375 IF K=7 THEN A$="DUROID":E=2.23
380 IF K<0 OR K>8 THEN 300
390 INPUT"FREQUENCY (GHZ)";F
400 INPUT"SUBSTRATE THICKNESS";H
410 INPUT "LINE THICKNESS";T
420 PRINT "DO YOU WANT"
430 PRINT
440 PRINT"1.  MICROSTRIP WIDTH"
450 PRINT"2.  IMPEDANCE OF MICROSTRIP LINE?"
460 PRINT
470 INPUT X
480 IF X=2 THEN 680
490 INPUT "DESIRED IMPEDANCE=";Z2
500 W=1
510 GOSUB 740
520 GOSUB 820
530 PRINT Z
540 R=Z/Z2
550 IF ABS((1-R)/(1+R))<=D1 THEN 620
560 REM CALCULATE NEW WIDTH
570 W=W*R*R
580 GOTO 510
590 REM
600 REM ADJUST WIDTH FOR THICKNESS OF LINE
```

cause a little more cut-and-try than we would like. Some people feel that a certain amount of "witchcraft" is involved in the design.

If a fraction of an inch of PC trace is a desired inductor in our circuit, how about the lengths needed just to connect the components together and which don't appear on the schematic?

Amplifier schematics liberally throw ground symbols around, implying that when we see the symbol we can assume there is no voltage at the point. Ha! Our fraction of an inch 3.2 nH represents almost 3 Ohms at 146 MHz. The transistor is delivering power into a 1 Ohm network. It doesn't take much ground length to be a goodly percentage of 1 Ohm. Very careful layout is required and even then the network is going to look different than calculated.

Capacitors act like values different than marked, due to lead inductance. When dealing with the high value capacitors dictated by the impedance levels involved in power amplifiers, leadless constructions like chip capacitors and metal cased micas are what you use. Even so, inductance is a consideration. A Motorola publication[15] estimates the metal cased mica capacitors used in VHF power amps, in the values they were discussing, have 1 to 2 nH in parasitic inductance and gives a formula for calculating an equivalent capacitor which will function as the desired value. The amplifier the author was designing required an 880 pF capacitor and the formula indicated that a 420 pF should be used, because of the effect of parasitic inductance. Hardly a small change!

Another significant design difference between small signal and power amplifiers is in the selection of Q. In small signal amplifiers, it is not uncommon to lower the Q of the output tuned circuits simply by paralleling them with resistors. The power lost by this procedure is generally not a consideration and the stability gained is a plus. This is generally not the procedure used in power amplifiers. If you want a specific Q, you design the network so that the desired Q is obtained with the normal loads.

We will cover more differences as we go, but I want to cover one more difference here, and that is the class of amplifier. Small signal amplifiers generally operate class A and occasionally drive into class AB with large signals. Power amplifiers can operate class A, AB, B or C. There is also a group of high efficiency amplifiers, such as classes D, E, F, G, H, and S which we won't even consider here.

Before briefly discussing the classes of amplifier, note that it wasn't necessary to worry about the class when we designed the output network. Whether operating class A, AB, B, or C our device must still see an impedance determined by the available voltage swing and desired power. I have made this point often today and do so because it is one of the most frequently misunderstood areas of power amplifier design. I will now let it rest.

Well, maybe not quite yet; because, I know some of you are going to go home and pull out the ARRL Radio Amateurs Handbook, that wonderful source of misinformation and oversimplification, and when you look in the section on power amplifier design you will find formulas different than we used. For example, their formula for the load resistance of a transistor amplifier ignores saturation resistance. This can lead to a significant error.

Their vacuum tube formula, as if there should be a difference, uses plate voltage, plate current, and a factor K which depends upon the class of

```
610 REM
620 GOSUB 1010
630 W=W-W1
640 GOTO 1090
650 REM
660 REM CALCULATE IMPEDANCE FROM LINE WIDTH
670 REM
680 INPUT"LINE WIDTH =";W
690 GOSUB 1010
700 W=W+W1
710 GOSUB 740
720 GOSUB 820
730 GOTO 1090
740 REM
750 REM SUBROUTINE TO CALCULATE P
760 REM
770 IF W/H<=1 THEN 800
780 P=2*P1/((W/H)+2.42-(.44*H/W)+EXP(8*LOG(1-(H/W))))
790 RETURN
800 P=LOG((8*H/W)+W/(4*H))
810 RETURN
820 REM
830 REM SUBROUTINE TO CALUCLATE E1,E2 AND Z
840 REM
850 E3=((E-1)/2*(1/SQR(1+(10*H/W))-1))
860 E1=E+E3
870 REM
880 REM CALCULATE EFFECTIVE ER
890 REM
900 REM DISPERSION EQUATION FROM GETSINGER
910 REM
920 Z1=60*P/SQR(E1)
930 G=.6+(.009*Z1)
940 D=Z1/(2.54*4*P1*H)
950 E2=E+(E3/(1+G*EXP(2*LOG(F/D))))
960 REM
970 REM CALCULATE IMPEDANCE,Z
980 REM
990 Z=60*P/SQR(E2)
1000 RETURN
1010 REM
1020 REM SUBROUTINE TO CORRECT LINE WIDTH FOR THICKNESS
1030 REM
1040 IF W/H<.15915 THEN 1070
1050 W1=(T/P1)*(1+LOG(2*H/T))
1060 RETURN
1070 W1=(T/P1)*(1+LOG((4*P1*W)/T))
1080 RETURN
1090 REM
1100 REM PRINT OUT RESULTS
1110 REM
1120 L=(11.811/F)/SQR(E2)
1130 REM
1140 REM THESE ARE RESERVED FOR PRINT FORMATS
1150 REM
1160 PRINT:PRINT:PRINT
1170 PRINT"  TYPE OF MATERIAL------------------";A$
1180 PRINT"  DIELECTRIC CONSTANT---------------";E
1190 PRINT"  EFFECTIVE DIELECTRIC CONSTANT-----";E2
1200 PRINT"  OPERATING FREQUENCY---------------";F;" GHZ"
1210 PRINT"  IMPEDANCE OF MICROSTRIP-----------";Z;" OHMS"
1220 PRINT"  WIDTH OF MICROSTRIP---------------";W;" INCHES"
1230 PRINT"  THICKNESS OF SUBSTRATE------------";H;" INCHES"
1240 PRINT"  THICKNESS OF MICROSTRIP LINE------";T;" INCHES"
1250 PRINT"  WAVELENGTH------------------------";L;" INCHES"
1260 PRINT"  QUARTER WAVELENGTH----------------";L/4;" INCHES"
1270 PRINT:PRINT:PRINT
1280 INPUT"ANOTHER RUN";Q$:Q$=LEFT$(Q$,1)
1290 IF Q$="Y" THEN 1300 ELSE END
1300 IF X=1 THEN GOTO 490 ELSE GOTO 680
```

amplifier. The K is, in reality, a factor that ties in efficiency and if you were to play with the formula you could tie it back to our voltage swing power output formula. If you are designing for a particular power output, you don't need to know the efficiency to calculate the load impedance.

Unfortunately, they also get into that garbage about complex conjugate matching of the souce impedance and confuse the issue before trying to straighten it out. Remember our toaster example!

Now, I'll let it rest. Back to class of amplifier. In case some of you have forgotten, we will re-define the classes.

A Class A amplifier is one whos bias and drive are such that current is flowing for the entire 360° of the drive cycle. If you assume a zero source impedance the theoretical maximum efficiency is 50% at maximum output. Values in the 20% to 35% range are more likely. In a truly linear class A amplifier, the power lost in the device is lowest at maximum output. This is the most linear of the classes and also has the highest gain. Due to low efficiency, Class A is generally confined to low power amplifiers.

A class AB amplifier operates at bias and drive levels so the device is conducting for more than 180° but less than 360° of the drive cycle. The tuned circuits fill in the missing parts of the RF cycle (so called flywheel effect) and Class AB RF amplifiers can be used for linear work, such as required by SSB, and for SSB use Class AB amplifiers are the most commonly used. 50% to 60% efficiencies are not uncommon.

I would like to use this class to poke fun at another popular conception and that is you should always operate an amplifier at less than its designed output power for maximum life. There is some validity to this theory. At lower powers some components are stressed less. (I could tell you a story about disintergrating gate bonding wires in poorly designed FET's except we don't have time, and, secondly, I would probably cry a lot.) However, in general, you maximize the life of an amplifier by keeping the transistor temperatures as low as you can.

Falcon Communications makes a Class AB amplifier that delivers 100 Watts when drawing about 12 Amperes from a 13.8 volt supply. 12 Amps at 13.8 Volts is about 166 Watts and if we are getting 100 Watts out, that means we are losing about 66 Watts in the amplifier. Allowing for a few Watts in the DC wiring, the output matching network, and the output filter, we are losing a little over 60 Watts in the two transistors. If we say that 10 of the 12 Watts drive it takes to get 100 Watts out is also dumped in the transistors, we end up with the transistors having to get rid of a little over 70 Watts of heat when the amplifier is driven to full output.

The quiescent current of this amplifier is 6 Amps. Thus, we have 6 x 13.8 or about 83 Watts of heat to get rid of if we have no drive but are keyed up. Almost all of the 83 Watts is dumped in the transistors. Thus, the transistors will run hotter at no output than they do at full output.

The point of the story is to caution you against blanket generalities.

A Class B amplifier is biased so the device is just cut off. Current, thus, flows for 180° of the drive cycle. 65% efficiency can be achieved. It is reasonably linear.

Although the definition of Class B calls for operation just at cut off, in

APPENDIX B

NET85. ASC - A useful network analysis program derived from literature, but extensively modified by users for particular needs, including file storage of circuits and results of analysis.

```
10 ' *** NET*85 ***
20 ' SEE EDN FEB 4, 1981 PP 126-133
30 ' TRANSLATED TO MICROSOFT BASIC BY R.B. KOLBLY
35 ' DISK FILES FOR SAVING AND RESTORING NETWORKS ADDED
36 ' DATA FILE OUTPUT CAPABILITY ADDED
40 ' GOLDEN RULE SYSTEMS - FEBRUARY 22,1985
50 P$=
 "FREQ= ##.####^^^^  AMPL= ##.##^^^^  20LOG= ####.#  PHASE= ####.#"
60 K=INT(FRE(A)/4)-23
70 X=INT((SQR(169+24*K)-26)/12)-1
80 PRINT USING "You have a maximum of ## Nodes Available";X
90 INPUT "Number of Nodes Desired (CR=10)";Y
100 IF X>=10 AND Y=0 THEN X=10:GOTO 140
110 IF X<10 AND Y=0 THEN X=Y:GOTO 140
120 IF Y>X THEN PRINT USING "Maximum of ### nodes!";X:GOTO 90
130 IF Y<X THEN X=Y
140 DIM A(X,X),B(X,X),P(X,X),Q(X,X),R(X,X)
150 DIM S(X,X),I(2*X),FL$(4,2)
160 DIM T(2*X),M(2*X),N(2*X),O(2*X),L(2*X),Z(2*X)
170 PRINT USING "You have selected a maximum of ## nodes";X
180 FOR J=1 TO X
190 FOR I=1 TO X
200 P(I,J)=0
210 Q(I,J)=0
220 R(I,J)=0
230 S(I,J)=0
240 NEXT I
250 NEXT J
260 NODES=X:X=1:T(X)=0
270 N=0
280 PRINT "1   RESISTOR"
290 PRINT "2   CAPACITOR"
300 PRINT "3   INDUCTOR"
310 PRINT "4   TRANSMISSION LINE"
320 PRINT "5   SHORTED STUB"
330 PRINT "6   OPEN STUB"
340 PRINT "7   OPERATIONAL AMPLIFIER"
350 PRINT "8   NPN TRANSISTOR"
360 PRINT "9   FIELD-EFFECT TRANSISTOR"
370 PRINT "10  STOP"
380 PRINT "11  ANALYZE NETWORK"
390 PRINT "12  ENABLE/DISABLE PRINTER"
391 PRINT "13  RESTORE NETWORK FROM DISK"
392 PRINT "14  SAVE NETWORK TO DISK"
393 PRINT "15  GENERATE ASCII NETWORK FILE"
400 PRINT "16  LOAD NETWORK VALUES FROM ASCII FI
410 PRINT
420 R6=0:INPUT "SELECT FROM LIST (<CR> FOR MENU)
430 IF R6=1 THEN PRINT "(1) RESISTOR":GOTO 730
440 IF R6=2 THEN PRINT "(2) CAPACITOR":GOTO 810
450 IF R6=3 THEN PRINT "(3) INDUCTOR":GOTO 770
460 IF R6=4 THEN PRINT "(4) TRANSMISSION LINE":G
470 IF R6=5 THEN PRINT "(5) SHORTED STUB":GOTO 6
480 IF R6=6 THEN PRINT "(6) OPEN STUB":GOTO 710
490 IF R6=7 THEN PRINT "(7) OP AMP":GOTO 990
500 IF R6=8 THEN PRINT "(8) NPN TRANSISTOR":GOTO
510 IF R6=9 THEN PRINT "(9) FET TRANSISTOR":GOTO
520 IF R6=10 THEN PRINT "(10) PROGRAM FINISH":ST
530 IF R6=11 THEN PRINT "(11) ANALYSIS":GOTO 106
540 IF R6=12 THEN INPUT "(12) HARDCOPY OUTPUT (Y/
    :H$=LEFT$(H$,1): GOTO 420
541 IF R6=13 THEN PRINT "(13) RESTORE NETWORK TO
    :GOTO 3000
542 IF R6=14 THEN PRINT "(14) SAVE NETWORK TO DI
543 IF R6=15 THEN PRINT "(15) GENERATE ASCII NET
    :GOTO 5000
544 IF R6=16 THEN PRINT "(16) LOAD NETWORK FROM A
    :GOTO 4000
550 GOTO 280
560 T(X)=1:INPUT "SHIELD IN";M(X):REM *** TRANSMI
570 INPUT "CENTER IN";I(X):INPUT "CENTER OUT";O(X
580 INPUT "SHIELD OUT";N(X):GOTO 610
590 INPUT "NODE A";M(X)
600 INPUT "NODE B";N(X)
610 INPUT "Z0";Z(X)
620 INPUT "QUARTER-WAVE FREQUENCY (HZ)";L(X)
630 IF I(X)>N THEN N=I(X)
640 IF M(X)>N THEN N=M(X)
650 IF N(X)>N THEN N=N(X)
660 IF O(X)>N THEN N=O(X)
670 X=X+1:T(X)=0
680 GOTO 420
690 T(X)=3: REM *** SHORTED STUB ***
700 GOTO 590
710 T(X)=2: REM *** OPEN STUB ***
720 GOTO 590
730 INPUT "NODE A";I:INPUT "NODE B";J:INPUT "RESI
740 V=1/V
750 GOSUB 1430
760 GOTO 420
770 INPUT "NODE A";I:INPUT "NODE B";J:INPUT "INDU
780 V=1/V
790 GOSUB 1360
800 GOTO 420
810 INPUT "NODE A";I:INPUT "NODE B";J
    :INPUT "CAPACITANCE (FARADS)";V
820 GOSUB 1480
830 GOTO 420
840 INPUT "GATE";K:INPUT "SOURCE";J:INPUT "DRAIN";
```

practice any amplifier operating near cut off is considered Class B. For example, a bi-polar transistor power amplifier operating with no bias and low base-to-ground DC resistance is generally considered Class B. This would not be a linear amplifier.

A Class C amplifier is biased beyond cut off. Thus, current flows for less, and generally considerably less, than 180° of the input drive cycle. Class C amplifiers have the highest efficiency, approaching 80%, and the lowest gain of the basic classes. They are very non-linear and used for CW, FM and other services where linearity is not important. They also generate the highest level of harmonics.

When applied to vacuum tubes there are sub classes, such as AB_1 and AB_2. The 1 means you never drive the tube hard enough to draw DC grid current, and the 2 means you do.

Class C vacuum tube amplifiers are almost always driven hard enough to draw grid current but the 2 subscript is seldom used.

For some reason, I hear the 1 and 2 subscripts occasionally applied to solid state amplifiers. They have no meaning. With bi-polar transistors you will have DC base current for all classes. If you draw DC gate current in a MOSFET device you had better get your wallet out because you just destroyed it.

The difference in designing for the different classes is primarily one of using knowledge of the conduction angle to be able to calculate the DC current, efficiency and gain. Time prevents going into the specifics. Once again, the topic is well covered in the literature[16,17].

Next, I would like to briefly cover the input matching network. Here, we are primarily performing an impedance matching function. We are transforming the impedance seen looking into the device to some desired impedance. If we are designing a single stage amplifier, the impedance we desire is generally one of the standard system impedances, such as 50 Ohms, 72 Ohms, 100 Ohms, etc. If we are dealing with a multistage amplifier, the input network of one stage is actually the output network of the preceeding stage. We will limit our discussion to single stage amplifiers, and 50 Ohm systems.

The F1260 MOSFET we have selected for our example amplifier has an input impedance whose real part is about 1 Ohm at the 146 MHz we are using in our example. Thus, the input matching network could be very similar to the output network and we won't go through any calculations.

The schematic of a 50 Watt, 2 Meter amplifier we manufacture is shown in Figure 9. We will use this schematic rather than a hypothetical example to finish our discussion of why the schematics look the way they do.

The input network is a double L, consisting of PC trace and L1 as the inductors and C6, C7 and C9, C10 as the capacitors. C5 is a compensating capacitor added to give a wider range of adjustment. C9 and C10 are metal cased micas for low lead inductance. R5 is just a static drain in this amplifier. In others it could be a swamping resistor. The amplifier has a T/R relay and provision to plug in a receive preamplifier.

Bias is applied to the FET through R3. Because no DC current is involved, R3 is large (10K). Again, if swamping is needed for any reason, R3 could be small. Bias comes from a regulated 8 Volt supply turned on at the same time as

```
    INPUT "GAIN(MHO)";V
850 L=J
860 GOSUB 1530
870 GOTO 420
880 INPUT "BASE";K:INPUT "EMITTER";J:INPUT "COLLECTOR";I:
    INPUT "BETA";R5
890 INPUT "Rbe (OHMS)";V
900 V=1/V
910 L=I
920 I=K
930 GOSUB 1430
940 I=L
950 L=J
960 V=V*R5
970 GOSUB 1530
980 GOTO 420
990 INPUT "+IN";K:INPUT "-IN";L:INPUT "-OUT";I:REM *** OP-AMP ***
1000 INPUT "+OUT";J:INPUT "GAIN(V/V)";R5:
     INPUT "OUTPUT RESISTANCE(OHMS)";V
1010 V=1/V
1020 GOSUB 1430
1030 V=V*R5
1040 GOSUB 1530
1050 GOTO 420
1060 INPUT "INPUT NODE";E:INPUT "OUTPUT NODE";F:N=N-1
1070 INPUT "START,STOP FREQUENCIES (HZ)";G,H
1080 INPUT "# OF DATA POINTS";M
1090 INPUT "FREQUENCY SWEEP-LOG=0(LINEAR=1)";R6
1091 PFG=0:INPUT "Do you want output data files";Q$:Q$=LEFT$(Q$,1)
1092 IF Q$="Y" OR Q$="y" THEN GOSUB 7000
1100 D=(H-G)/(M-1)
1110 R4=EXP(LOG(H/G)/(M-1))
1120 R0=G:R9=0
1130 R9=R9+1
1140 W=2*3.14159*R0
1150 O=E:Z=F
1160 GOSUB 2470
1170 GOSUB 2200
1180 V=R5:U=Z
1190 IF (E+F)/2=INT((E+F)/2) THEN 1210
1200 U=U-180
1210 O=E:Z=E
1220 GOSUB 2200
1230 U=U-Z
1240 IF V=0 THEN R7=-999:GOTO 1270
1250 IF R5=0 THEN R7=9999:GOTO 1270
1260 V=V/R5:R7=8.68589*LOG(V)
1270 IF U>180 THEN U=U-360
1280 IF U<-180 THEN U=U+360
1290 PRINT USING P$;R0,V,R7,U
1300 IF H$="Y" THEN LPRINT USING P$;R0,V,R7,U
1302 IF PFG=0 THEN GOTO 1310
1304 GOSUB 7200
1310 IF R6=0 THEN R0=R0*R4
1320 IF R6<>0 THEN R0=R0+D
1330 IF R9<>M THEN 1130
1340 N=N+1
1350 CLOSE:GOTO 420
1360 R(I,I)=R(I,I)+V:REM INDL
1370 R(J,J)=R(J,J)+V
1380 R(I,J)=R(I,J)-V
1390 R(J,I)=R(J,I)-V
1400 IF I>N THEN N=I
1410 IF J>N THEN N=J
1420 RETURN
1430 P(I,I)=P(I,I)+V:REM RESL
1440 P(J,J)=P(J,J)+V
1450 P(I,J)=P(I,J)-V
1460 P(J,I)=P(J,I)-V
1470 GOTO 1400
1480 Q(I,I)=Q(I,I)+V
1490 Q(J,J)=Q(J,J)+V:REM CAPL
1500 Q(I,J)=Q(I,J)-V
1510 Q(J,I)=Q(J,I)-V
1520 GOTO 1400
1530 P(I,K)=P(I,K)+V:REM TRANS
1540 P(J,L)=P(J,L)+V
1550 P(J,K)=P(J,K)-V
1560 P(I,L)=P(I,L)-V
1570 IF K>N THEN N=K
1580 IF L>K THEN N=L
1590 GOTO 1400
1600 IF N>1 THEN 1630: REM COMP
1610 O=A(1,1):Z=B(1,1)
1620 RETURN
1630 O=1
1640 Z=0
1650 K=1
1660 L=K
1670 S=ABS(A(K,K))+ABS(B(K,K))
1680 I=K-1
1690 I=I+1
1700 T=ABS(A(I,K))+ABS(B(I,K))
1710 IF S>=T THEN 1730
1720 L=I:S=T
1730 IF I<>N THEN 1690
1740 IF L=K THEN 1800
1750 J=0
1760 J=J+1
1770 S=-A(K,J):A(K,J)=A(L,J):A(L,J)=S
1780 A=-B(K,J):B(K,J)=B(L,J):B(L,J)=A
1790 IF J<>N THEN 1760
1800 L=K+1:I=L-1
1810 I=I+1
1820 A=A(K,K)*A(K,K)+B(K,K)*B(K,K)
1830 S=(A(I,K)*A(K,K)+B(I,K)*B(K,K))/A
1840 B(I,K)=(A(K,K)*B(I,K)-A(I,K)*B(K,K))/A
1850 A(I,K)=S
1860 IF I<>N THEN 1810
1870 C=K-1
```

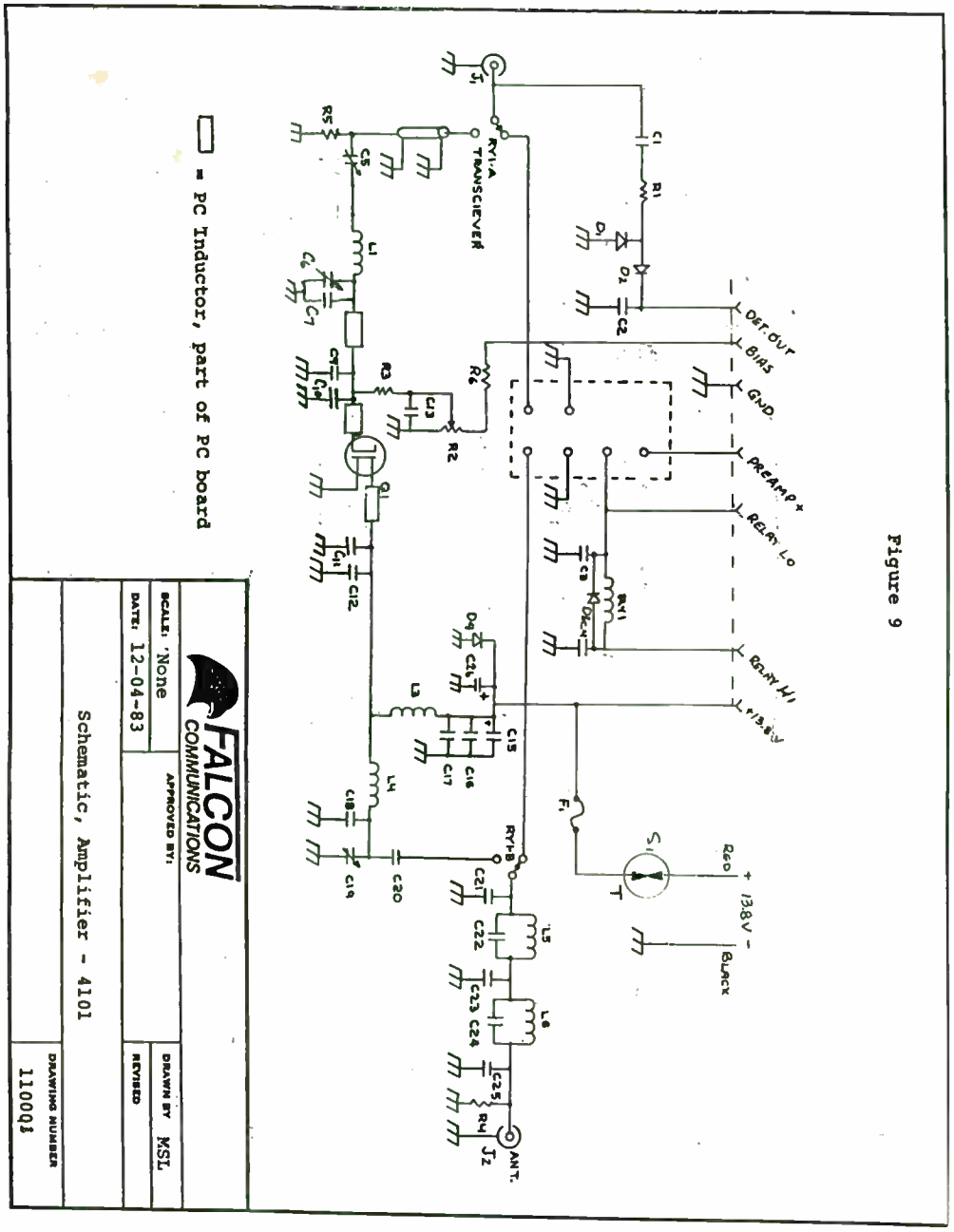


Figure 9

the T/R relay. The output matching network is our familiar double L and I will leave it up to you to find it.

In this amplifier, C20 is simply a d. c. blocking capacitor to keep d. c. out of the antenna. It could easily have been made part of the output matching network.

Following the amplifier is a 2 section "m" derived low pass filter. In this day of modern filter design, using an "m" derived filter may seem a bit archaic. After all the more modern designs do offer sharper roll-offs. Let me defend the choice.

This amplifier is designed as an add-on to a customers transceiver and since we don't know what transceiver might be used we have no way of knowing what frequencies the spurious signals coming out of that transceiver might be located at. Thus, the amplifier designer's task is to design the amplifier for minimum output of any spurious that the amplifier might generate, namely harmonics; with the first, and dominant, one being the second harmonic.

Though the more modern filters can be made to initially roll off steeper, the old "m" derived can put a beautiful notch right where you need it, at 2f. In addition, the efficiency of that notch is less dependendent upon load impedance than the slope of some of the modern filters. The defense rests.

Lets discuss the rest of the components and get on to another example. L3, a choke to feed DC to the transistor, is connected close to Q1 at a low impedance (low voltage) point. L3 is bypassed with four bypass capacitors. Two 470 pF, for high frequency bypassing, a 1 uF, for mid frequency bypassing, and a 1000 uF for low frequency bypassing. The gain of the transistor goes up

```
1880 IF C=0 THEN 1960
1890 J=L-1
1900 J=J+1:I=0
1910 I=I+1
1920 A(K,J)=A(K,J)-A(K,I)*A(I,J)+B(K,I)*B(I,J)
1930 B(K,J)=B(K,J)-B(K,I)*A(I,J)-A(K,I)*B(I,J)
1940 IF C<>I THEN 1910
1950 IF J><N THEN 1900
1960 C=K
1970 K=K+1:I=K-1
1980 I=I+1:J=0
1990 J=J+1
2000 A(I,K)=A(I,K)-A(I,J)*A(J,K)+B(I,J)*B(J,K)
2010 B(I,K)=B(I,K)-B(I,J)*A(J,K)-A(I,J)*B(J,K)
2020 IF J<>C THEN 1990
2030 IF I<>N THEN 1980
2040 IF K<>N THEN 1660
2050 L=1
2060 C=INT(N/2)
2070 IF N=2*C THEN 2100
2080 L=0
2090 O=A(N,N):Z=B(N,N)
2100 I=0
2110 I=I+1
2120 J=N-I+L
2130 S=A(I,I)*A(J,J)-B(I,I)*B(J,J)
2140 A=A(I,I)*B(J,J)+A(J,J)*B(I,I)
2150 T=O*S-Z*A
2160 Z=Z*S+O*A
2170 O=T
2180 IF I<>C THEN 2110
2190 RETURN
2200 R5=N:REM DET
2210 N=N-1
2220 I=0
2230 K=0
2240 K=K+1
2250 IF K<>O THEN 2270
2260 I=1
2270 J=0:L=0
2280 L=L+1
2290 IF L<>Z THEN 2310
2300 J=1
2310 A(K,L)=P(K+I,L+J)
2320 B(K,L)=W*Q(K+I,L+J)-R(K+I,L+J)/W+S(K+I,L+J)
2330 IF L<>N THEN 2280
2340 IF K<>N THEN 2240
2350 GOSUB 1600
2360 N=R5
2370 R5=SQR(O*O+Z*Z)
2380 Y=Z
2390 IF O=0 THEN 2450
2400 Z=180/3.14159*ATN(Z/O)
2410 IF O>0 THEN RETURN
2420 Z=Z+SGN(Y)*180
2430 IF Y=0 THEN Z=180
2440 RETURN
2450 Z=90*SGN(Y)
2460 RETURN
2470 IF T(1)=0 THEN RETURN
2480 X=0
2490 R1=0
2500 R1=R1+1:R2=0
2510 R2=R2+1
2520 S(R1,R2)=0
2530 IF R2<>N+1 THEN 2510
2540 IF R1<>N+1 THEN 2500
2550 X=X+1
2560 IF X>20 THEN RETURN
2570 IF T(X)=0 THEN RETURN
2580 IF T(X)=1 THEN 2640
2590 IF T(X)=2 THEN 2830
2600 R1=-1/(Z(X)*TAN(.25*W/L(X)))
2610 Q=M(X):R=N(X)
2620 GOSUB 2870
2630 GOTO 2550
2640 R1=-1/(Z(X)*TAN(.25*W/L(X)))
2650 Q=M(X):R=I(X)
2660 GOSUB 2870
2670 Q=N(X):R=O(X):GOSUB 2870
2680 R1=1/(Z(X)*SIN(.25*W/L(X)))
2690 P=I(X)
2700 R=N(X)
2710 S(R,P)=S(R,P)-R1
2720 S(P,R)=S(P,R)-R1
2730 R=O(X)
2740 S(R,P)=S(R,P)+R1
2750 S(P,R)=S(P,R)+R1
2760 P=M(X)
2770 S(R,P)=S(R,P)-R1
2780 S(P,R)=S(P,R)-R1
2790 R=N(X)
2800 S(R,P)=S(R,P)+R1
2810 S(P,R)=S(P,R)+R1
2820 GOTO 2550
2830 R2=1/(Z(X)*TAN(.25*W/L(X)))
2840 R3=1/(Z(X)*SIN(.25*W/L(X)))
2850 R1=R3*R3/R2-R2
2860 GOTO 2610
2870 S(Q,Q)=S(Q,Q)+R1
2880 S(R,R)=S(R,R)+R1
2890 S(Q,R)=S(Q,R)-R1
2900 S(R,Q)=S(R,Q)-R1
2910 RETURN
2920 END
3000 INPUT "NAME OF FILE TO LOAD <CR> FOR DIRECTORY";F$:
     ' LOAD FROM FILE
3010 IF LEN(F$)=0 THEN FILES:GOTO 3000
3020 IF F$="B:" THEN FILES "B:*.*":GOTO 3000
3030 IF F$="A:" THEN FILES "A:*.*":GOTO 3000
```

significantly as frequency goes down and proper bypassing is necessary to prevent oscillation.

D4 ia a reverae voltage protection diode which blowa the fuse if the aupply voltage ia connected wrong. A lesa apectacular way to do the job is to connect a diode in aeriea with the aupply line. However, leta look back at our example. We aasumed a 13.0 Volt aupply (13.8 Volts running a little low, less the drop in the #12 wire supply lines, leas the drop across the fuse) less the 3 Volt saturation voltage; gave ua a 10 Volt peak swing. If we add a aeries diode, the 10 Volta goea down another 0.8 Volta or so. This costs power. Hence, the shunt diode.

S1 ia a thermoatat mounted on the heat sink, which shuta the amplifier down if thinga get too hot. C1, R1, D1, D2, and C2 form a detector to sense the presence of input RF and turn the amplifier on. R4 is another atatic drain. The puriata uae a choke here.

There is no temperature compensation in the bias circuit. It is not needed in MOSFET amplifiers of this power level. The amplifier was placed in a temperature chamber and tested over the range of -40 to +60° C. The quiescent current varied only 0.2 Ampa acroas the entire range. Room temperature current was 3 Amps. Current drawn at the 50 Watt point didn't vary aignificantly.

I think we have stared at this 50 Watt amplifier long enough. How about higher power? The power we can design for is, of course, limited by the available devicea. At VHF, using a 13.8 Volt aupply, 60 Watts is about where the induatry is at with MOSFET devices, and 80 Watts with bipolar devices. At higher aupply voltages 150 Watts is obtainable. At low frequencies, Motorola has the grand-daddy of them all. A MOSFET device delivering 600 Watts up to 100 MHz. As frequency goes up, power comes down, with 50 Watts being about the limit at 450 MHz. 120 Watts at 500MHz is available in push-pull packages.

If we want more power we have to use multiple devices connected together. One technique is to use a group of lower power amplifiers and combine their output in combining networks. Combining networks[18,19] are a topic unto themselves and we won't go into them here. Let me simply say that in practice they are more complex than you would be led to believe by the simplified discussion in the texts. We will simply look at devices connected in parallel and push-pull. First parallel.

Lets say we want an amplifier that will deliver 150 Watts at 146 MHz and use a 13.0 Volt aupply. Lets use a pair of bi-polar devices, the MRF247, and assume the saturation voltage is 2 Volts.

Going back to our reliable formula for load impedance we find that the transiators must aee:

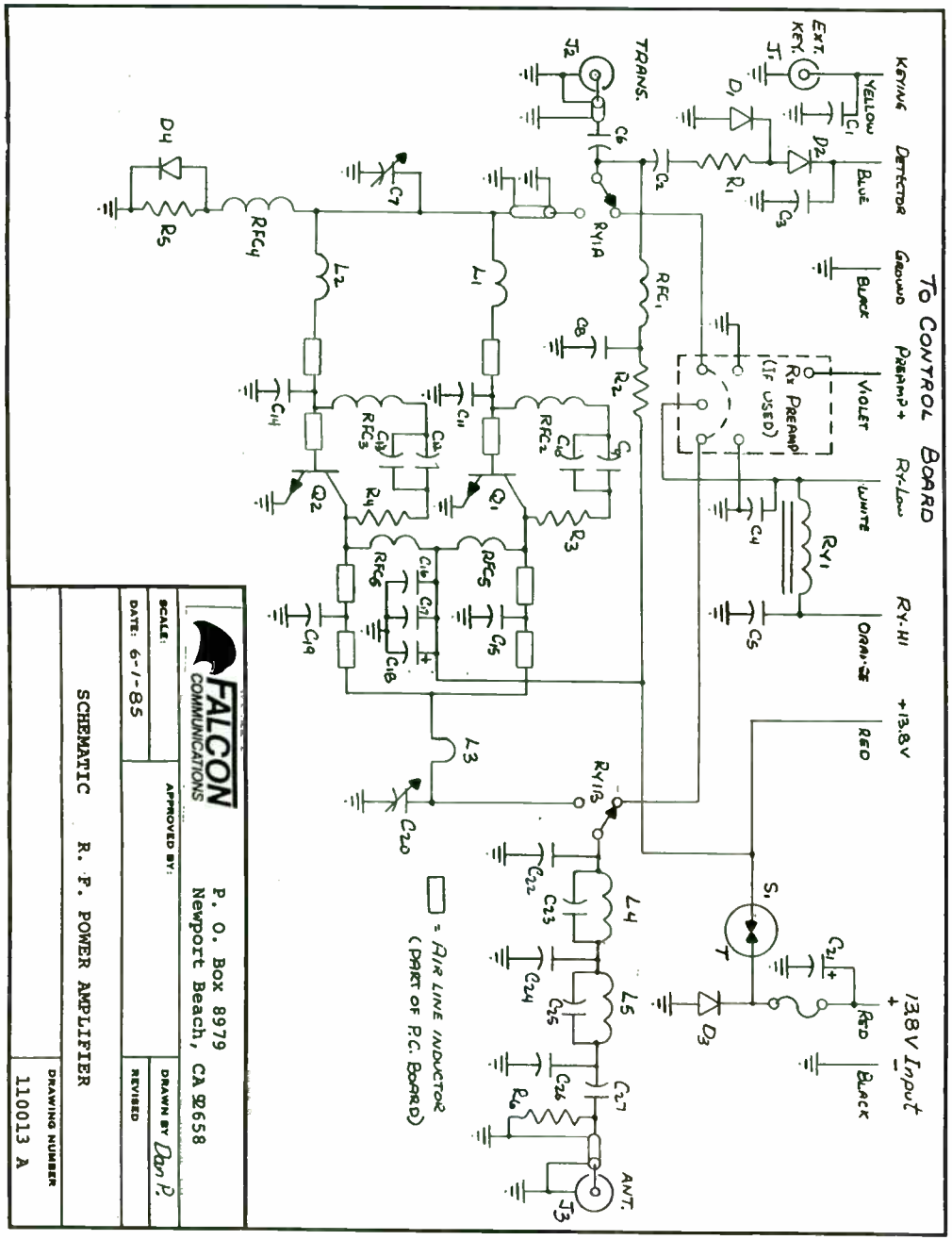
$$R_L = \frac{(E_{supply} - E_{sat})^2}{2P} = \frac{(13-2)^2}{2 \cdot 150} = 0.4\,\Omega \qquad 13)$$

This is a low impedance and trying to get two transiators tied together such that the impedance in the connecting lines is a small fraction of this is almost impossible.

The trick is to tie them together at a higher impedance point and then use matching networks for the individual transistors to get to a lower impedance. This haa a number of advantages, not the least of which ia that it works, and the networks allow some physical separation between the transiators.

Figure 10 is the schematic of a Falcon 150 Watt 2 Meter amplifier using

```
3040 OPEN "I",#1,F$
3050 INPUT #1,X
3060 ERASE A,B,P,Q,R,S,I,T,M,N,O,L,Z
3070 DIM A(X,X),B(X,X),P(X,X),Q(X,X),R(X,X)
3080 DIM S(X,X),I(2*X)
3090 DIM T(2*X),M(2*X),N(2*X),O(2*X),L(2*X),Z(2*X)
3095 INPUT #1,N
3100 FOR J=1 TO X
3110 INPUT #1,I(J),T(J),M(J),N(J),O(J),L(J),Z(J)
3120 FOR K=1 TO X
3130 INPUT #1,A(J,K),B(J,K),P(J,K),Q(J,K),R(J,K),S(J,K)
3140 NEXT K
3150 NEXT J
3160 CLOSE #1
3170 NODES=X:GOTO 420
3500 INPUT "NAME OF FILE TO SAVE <CR> FOR DIRECTORY";F$:
     ' SAVE INTO FILE
3510 IF LEN(F$)=0 THEN FILES:GOTO 3500
3520 IF F$="B:" THEN FILES "B:*.*":GOTO 3500
3530 IF F$="A:" THEN FILES "A:*.*":GOTO 3500
3540 OPEN "O",#1,F$
3550 PRINT #1,NODES,N
3600 FOR J=1 TO NODES
3610 PRINT #1,I(J),T(J),M(J),N(J),O(J),L(J),Z(J)
3620 FOR K=1 TO NODES
3630 PRINT #1,A(J,K),B(J,K),P(J,K),Q(J,K),R(J,K),S(J,K)
3640 NEXT K
3650 NEXT J
3660 CLOSE #1
3670 GOTO 420
4000 INPUT "Name of file to load <cr> for directory";F$
4010 IF LEN(F$)=0 THEN FILES:GOTO 4000
4020 OPEN "I",#1,F$
4030 IF EOF(1) THEN CLOSE:GOTO 420
4035 R6$="":INPUT #1,R6$:R6$=LEFT$(R6$,1)
4040 IF R6$="1" THEN GOTO 4320
4050 IF R6$="2" THEN GOTO 4400
4060 IF R6$="3" THEN GOTO 4360
4070 IF R6$="4" THEN GOTO 4150
4080 IF R6$="5" THEN GOTO 4280
4090 IF R6$="6" THEN GOTO 4300
4100 IF R6$="7" THEN GOTO 4580
4110 IF R6$="8" THEN GOTO 4470
4120 IF R6$="9" THEN GOTO 4430
4130 IF EOF(1) THEN 420
4140 GOTO 4030
4150 T(X)=1:INPUT #1,M$:M(X)=VAL(M$):REM *** TRANSMISSION LINE ***
4160 INPUT #1,I$:I(X)=VAL(I$):INPUT #1,O$:O(X)=VAL(O$)
4170 INPUT #1,N$:N(X)=VAL(N$):GOTO 4200
4180 INPUT #1,M$:M(X)=VAL(M$)
4190 INPUT #1,N$:N(X)=VAL(N$)
4200 INPUT #1,Z$:Z(X)=VAL(Z$)
4210 INPUT #1,L$:L(X)=VAL(L$)
4220 IF I(X)>N THEN N=I(X)
4230 IF M(X)>N THEN N=M(X)
4240 IF N(X)>N THEN N=N(X)
4250 IF O(X)>N THEN N=O(X)
4260 X=X+1:T(X)=0
4270 GOTO 4030
4280 T(X)=3: REM *** SHORTED STUB ***
4290 GOTO 4180
4300 T(X)=2: REM *** OPEN STUB ***
4310 GOTO 4180
4320 INPUT #1,I$:I=VAL(I$):
     INPUT #1,J$:J=VAL(J$):INPUT #1,V$:V=VAL(V$)
4330 V=1/V
4340 GOSUB 1430
4350 GOTO 4030
4360 INPUT #1,I$:I=VAL(I$):
     INPUT #1,J$:J=VAL(J$):INPUT #1,V$:V=VAL(V$)
4370 V=1/V
4380 GOSUB 1360
4390 GOTO 4030
4400 INPUT #1,I$:I=VAL(I$):
     INPUT #1,J$:J=VAL(J$):INPUT #1,V$:V=VAL(V$)
4410 GOSUB 1480
4420 GOTO 4030
4430 INPUT #1,K$:K=VAL(K$):INPUT #1,J$:J=VAL(J$):INPUT #1,I$:
     I=VAL(I$):INPUT #1,V$:V=VAL(V$)
4440 L=J
4450 GOSUB 1530
4460 GOTO 4030
4470 INPUT #1 "BASE";K:INPUT #1,J$:J=VAL(J$):INPUT #1,I$:
     I=VAL(I$):INPUT #1,R$:R5=VAL(R$)
4480 INPUT #1,V$:V=VAL(V$)
4490 V=1/V
4500 L=I
4510 I=K
4520 GOSUB 1430
4530 I=L
4540 L=J
4550 V=V*R5
4560 GOSUB 1530
4570 GOTO 4030
4580 INPUT #1,K$:K=VAL(K$):INPUT #1,L$:L=VAL(L$):
     INPUT #1,I$:I=VAL(I$)
4590 INPUT #1,J$:J=VAL(J$):INPUT #1,R$:R5=VAL(R$):
     INPUT #1,V$:V=VAL(V$)
4600 V=1/V
4610 GOSUB 1430
4620 V=V*R5
4630 GOSUB 1530
4640 GOTO 4030
5000 INPUT "Name of file (<cr> for Directory)";F$
5010 IF LEN(F$)=0 THEN FILES:GOTO 5000
5020 OPEN "O",#1,F$
5200 PRINT "1   RESISTOR"
5210 PRINT "2   CAPACITOR"
5220 PRINT "3   INDUCTOR"
5230 PRINT "4   TRANSMISSION LINE"
```



this technique. You will see many similarities with the previous amplifier: low pass filter in the output, T/R relay, pre-amp provision, etc. The big difference is that there are now two transistors. If you will look at the collector of one of the transistors, you will see we have an L section and part of a second before we parallel with the other transistor. Looking at the input reveals a similar situation. Thats really all there is to it.

Not seen on the schematic is some circuitry internal to the transistor. The input impedance of large bi-polar RF power transistors is very low at these frequencies, so low as to make matching difficult. The manufacturers, thus, very kindly build matching networks into the transistor to raise the input impedance to a workable level. THe MRF247 has a T network consisting of the inductance of the bonding wires and a built-in MOS capacitor in the input of each of the eight cells that make up the device. Even with the internal matching the input impedance is low. The MRF247, in our application, has a series equivalent input impedance of 0.45 +J 0.85 Ohms.

You lose some potential power capability parallelling transistors because there is no guarantee that the two transistors are carrying an equal share of the load and the one carrying the greatest amount becomes the limiting factor. There are a number of things that help. One is to use transistors in matched pairs. Some companies do, some don't. You could also make some of the non common network elements variable. We don't do either on this model; but we do occasionally add a fixed capacitor across one of the transistors when we sense an inbalance in test.

The gain of bi-polar transistors increases much more than MOSFETs as

```
5240 PRINT "5   SHORTED STUB"
5250 PRINT "6   OPEN STUB"
5260 PRINT "7   OPERATIONAL AMPLIFIER"
5270 PRINT "8   NPN TRANSISTOR"
5280 PRINT "9   FIELD-EFFECT TRANSISTOR"
5290 PRINT "10  STOP"
5360 R6=0:INPUT "SELECT FROM LIST";R6:R6$=STR$(R6)
5370 IF R6=1 THEN PRINT "(1) RESISTOR":GOTO 5690
5380 IF R6=2 THEN PRINT "(2) CAPACITOR":GOTO 5770
5390 IF R6=3 THEN PRINT "(3) INDUCTOR":GOTO 5730
5400 IF R6=4 THEN PRINT "(4) TRANSMISSION LINE":GOTO 5520
5410 IF R6=5 THEN PRINT "(5) SHORTED STUB":GOTO 5650
5420 IF R6=6 THEN PRINT "(6) OPEN STUB":GOTO 5670
5430 IF R6=7 THEN PRINT "(7) OP AMP":GOTO 5950
5440 IF R6=8 THEN PRINT "(8) NPN TRANSISTOR":GOTO 5840
5450 IF R6=9 THEN PRINT "(9) FET TRANSISTOR":GOTO 5800
5460 IF R6=10 THEN PRINT "(10) FILE COMPLETED":CLOSE #1:GOTO 420
5510 GOTO 5360
5520 INPUT "SHIELD IN";M$:REM *** TRANSMISSION LINE ***
5530 INPUT "CENTER IN";I$:INPUT "CENTER OUT";O$
5531 PRINT #1,R6$+" * TRANSMISSION LINE"
5532 PRINT #1,M$
5533 PRINT #1,I$
5534 PRINT #1,O$
5540 INPUT "SHIELD OUT";N$:PRINT #1,N$:GOTO 5570
5550 INPUT "NODE A";M$:PRINT #1,M$
5560 INPUT "NODE B";N$:PRINT #1 N$
5570 INPUT "Z0";Z$:PRINT #1,Z$
5580 INPUT "QUARTER-WAVE FREQUENCY (HZ)";L$:PRINT #1,L$
5640 GOTO 5360
5650 REM *** SHORTED STUB ***
5655 PRINT #1,R6$+" * SHORTED STUB"
5660 GOTO 5550
5670 PRINT #1,R6$+" * OPEN STUB":REM *** OPEN STUB ***
5680 GOTO 5550
5690 INPUT "NODE A";I$:INPUT "NODE B";J$:
     INPUT "RESISTANCE (OHMS)";V$
5700 PRINT #1,R6$+" * RESISTOR"
5702 PRINT #1,I$
5704 PRINT #1,J$
5706 PRINT #1,V$
5720 GOTO 5360
5730 INPUT "NODE A";I$:INPUT "NODE B";J$:
     INPUT "INDUCTANCE (H)";V$
5740 PRINT #1,R6$+" * INDUCTOR"
5742 PRINT #1,I$
5744 PRINT #1,J$
5746 PRINT #1,V$
5760 GOTO 5360
5770 INPUT "NODE A";I$:INPUT "NODE B";J$:
     INPUT "CAPACITANCE (FARADS)";V$
5775 PRINT #1,R6$+" * CAPACITOR"
5790 GOTO 5742
5800 INPUT "GATE";K$:INPUT "SOURCE";J$:INPUT "DRAIN";I$:
     INPUT "GAIN(MHO)";V$
5810 PRINT #1,R6$+" * FET"
5812 PRINT #1,K$
5814 PRINT #1,J$
5816 PRINT #1,I$
5818 PRINT #1,V$
5830 GOTO 5360
5840 INPUT "BASE";K$:INPUT "EMITTER";J$:INPUT "COLLECTOR";I$:
     INPUT "BETA";R5$
5850 INPUT "Rbe (OHMS)";V$
5860 PRINT #1,R6$+" * NPN TRANSISTOR"
5861 PRINT #1,K$
5862 PRINT #1,J$
5863 PRINT #1,I$
5864 PRINT #1,R5$
5865 PRINT #1,V$
5940 GOTO 5360
5950 INPUT "+IN";K$:INPUT "-IN";L$:INPUT "-OUT";I$:REM *** OP-AMP ***
5960 INPUT "+OUT";J$:INPUT "GAIN(V/V)";R5$:
     INPUT "OUTPUT RESISTANCE(OHMS)";V$
5970 PRINT #1,R6$+" * OP-AMP"
5972 PRINT #1,K$
5974 PRINT #1,L$
5976 PRINT #1,I$
5978 PRINT #1,J$
5980 PRINT #1,R5$
5990 PRINT #1,V$
6010 GOTO 5360
7000 ' SUBROUTINES FOR FILE HANDLING
7010 FOR J=1 TO 4:READ FL$(J,1):FL$(J,2)="N":NEXT J
7020 FOR J=1 TO 4
7030 IF FL$(J,2)="Y" THEN GOTO 7050
7040 PRINT STR$(J)+"- "+FL$(J,1)
7050 NEXT J
7060 PRINT
7070 INPUT "Choice (enter <cr> or 0 to exit)";C:C=INT(C)
7080 IF FL$(C,2)="Y" THEN PRINT "Already Selected!":GOTO 7070
7090 IF C=0 THEN RESTORE:RETURN
7100 PFG=1:INPUT "Name of Data File (<cr> for Directory)";F$
7110 IF LEN(F$)=0 THEN FILES:GOTO 7100
7120 FL$(C,2)="Y":OPEN "O",C,F$
7130 GOTO 7020
7140 DATA "Amplitude versus Frequency","Phase versus Frequency"
7150 DATA "Amplitude,Phase vs. Frequency","Amplitude vs. Phase"
7160 CLOSE
7200 FOR JJ=1 TO 4
7210 IF FL$(JJ,2)="N" THEN GOTO 7270
7220 ON JJ GOTO 7230,7240,7250,7260
7230 WRITE #1,R0,V:GOTO 7270
7240 WRITE #2,R0,U:GOTO 7270
7250 WRITE #3,R0,V,U:GOTO 7270
7260 WRITE #4,V,U
7270 NEXT JJ
7280 RETURN
```

frequency goes down. This results in a great tendency to oscillate at low frequencies. RFC2, C9, C10, R3 and RFC3, C12, C13, R4 form feedback loops that keep the low frequency gain down. Because we are dealing with bi-polar transistors, which require bias current, our bias supply needs to be low impedance. Also, because of the well known variations of bias requirements with temperature, the bias voltage must vary with temperature.

The bias is the voltage developed across D4, which receives its current through R2, RFC1, RY1a, and RFC4. R5 is a factory adjust to set up the desired quiescent current. If the diode can be considered to be at the same temperature as the transistor this type of bias tracks reasonably well. Some of the tricks used are to use a stud mounted diode mounted on the heat sink, near the transistors, or to mount the diode right on the transistor. We don't do either. The diode is simply a 1N4001 mounted on the PC board.

This simple bias scheme is definitely a compromise. The normal bias stabilization methods used at low power require a DC resistance in either the collector or emitter circuits. Sufficient resistance to effectively stabilize the quiescent would consume a great deal of power and, when we are operating at a low supply voltage, waste enough voltage as to make getting our desired power output difficult. In addition, we don't want to lift the emitter off of ground for RF reasons. Keeping it at an RF ground is difficult enough. They didn't put four emitter tabs on the MRF247 for the fun of it.

There is some help on bias stability built into the transistor. The device is in reality many transistors internally connected in parallel. To prevent current hogging, hot spots and a number of other nasty problems, the manufacturer adds a small resistance in the emitter of each of these many transistors. If you are not familiar with the term, this is known as "emitter ballasting".

There is an additional problem with our simple bias scheme. The input RF is rectified by the transistor base-emitter junction, creating a current opposing the bias current. If the bias source is not stiff enough this can bias you toward Class B, or even C, with the attendant loss of linearity and gain. In the amplifier under review, R2 is 50 Ohms and R5 typically about 2 Ohms and we can still lose about 20% in power gain under some circumstances. It is also important that RFC4 have a low DC resistance.

The final schematic we will take a look at is of a push-pull amplifier. Because we do not make a push-pull amplifier, I have borrowed a schematic from a Motorola Engineering Bulletin[20]. It is shown in Figure 11.

Push-pull at RF is not different in principle from push-pull at audio. You take the input signal and produce two signals 180° out of phase and apply them to two amplifying devices. The two resulting 180° out of phase output signals are combined in a transformer or other device to give the output.

At HF the 180° signals are generally generated and combined with physically identifiable transformers. Years ago, these were generally air cored transformers. Today, toroidal cored transformers are common. For wide bandwidth, the so called transmission line transformer on a toroidal core is common. At VHF and UHF, wound transformers are impractical and baluns made out of lengths of coaxial cable are common. That is what is used in this 420-450 MHz amplifier (T1 and T2). First note that they used matching networks to

APPENDIX B.2 Example of circuit data file for input to the program NET85.ASC. This file can be generated by the program itself or generated or modified by any text editor. The /* */ are delimiters for remarks and are not added by the program. They have been added for explanation of the file structure. Note that the file structure is the same as is input from the keyboard.

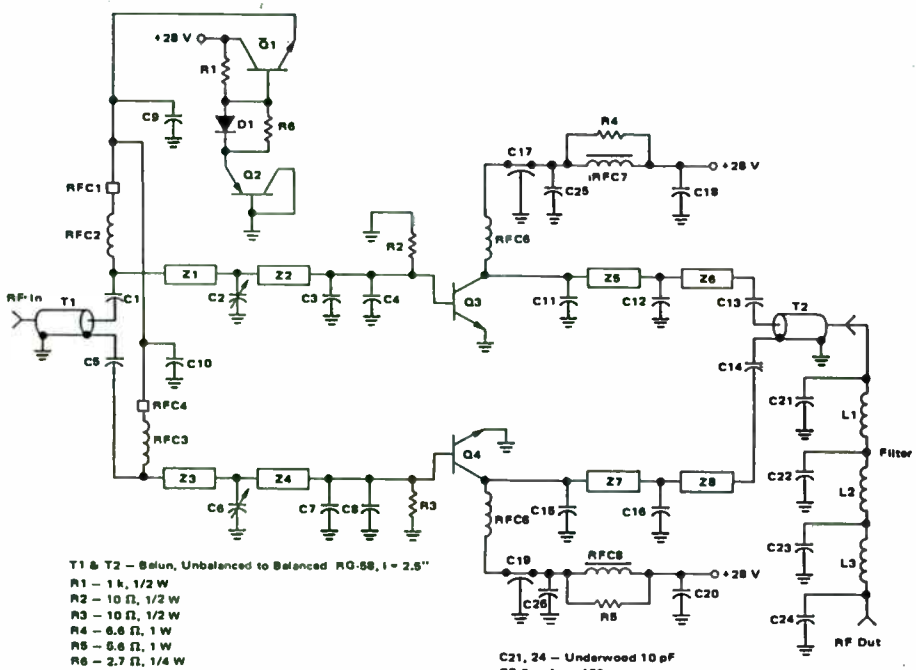
```
 1 * RESISTOR          /* Type of element (1 is a resistor) */
1                      /* Node A  */
2                      /* Node B  */
50
 1 * RESISTOR
4
7
50
 1 * RESISTOR
6
7
50
 2 * CAPACITOR
3
7
58E-12                  /* Value of capacitor in farads (58 pf */
 2 * CAPACITOR
2
5
23E-12
 2 * CAPACITOR
5
6
23E-12
 3 * INDUCTOR
2
3
72E-9                   /* This is a 72 nh inductor */
 3 * INDUCTOR
3
4
72E-9
 3 * INDUCTOR
5
7
28E-9
```

APPENDIX B.3 Sample output file from NET85.ASC. This data can be edited with any text editor, added to a report, or used by a plotting program, such as PCPLOT2 (BV Engineering, Riverside, CA):

(The first number is frequency, the second is amplitude.)

```
8E+07,3.543465E-02
8.269104E+07,3.831959E-02
8.54726E+07,4.173018E-02
8.834772E+07,4.599374E-02
9.131957E+07,.0516254
9.439138E+07,5.938689E-02
9.756651E+07,7.032793E-02
1.008485E+08,8.579546E-02
1.042408E+08,.1073953
1.077473E+08,.1368522
1.113717E+08,.1755944
1.15118E+08,.2237623
1.189903E+08,.2785856
1.229929E+08,.3333452
1.271301E+08,.3794872
1.314065E+08,.4116778
1.358268E+08,.430391
1.403957E+08,.4395925
1.451184E+08,.4434264
1.499998E+08,.4447783
```

Figure 11



T1 & T2 – Balun, Unbalanced to Balanced RG-58, l = 2.5"
R1 – 1 k, 1/2 W
R2 – 10 Ω, 1/2 W
R3 – 10 Ω, 1/2 W
R4 – 6.6 Ω, 1 W
R5 – 5.6 Ω, 1 W
R6 – 2.7 Ω, 1/4 W
Z1 & Z3 – Microstrip – W = 200 mils, l = 1.8"
Z2 & Z4 – Microstrip – W = 200 mils, l = 300 mils
Z5 & Z6 – Microstrip – W = 150 mils, l = 300 mils
Z6 & Z8 – Microstrip – W = 150 mils, l = 1.4"
RFC1, 4 – Ferroxcube Bead 56-590-65-3B
RFC2,3 – 0.15 μH Cambion Molded Coil
RFC5, 6 – 1 Turn #20 Enameled Wire Wound on 6/16" Bolt
RFC7, 8 – VK200 20/4B
C1,3,4,5,7,8,11,15 – Underwood 40 pF
C12,16 – Underwood 25 pF
C13, 14, 22, 23 – Underwood 15 pF
C9,10,18,20 – 1 μF Tantalum

C21, 24 – Underwood 10 pF
C2,6 – Arco 403
C17,19 – Underwood J102, 1000 pF Feed Thru
C25, 26 – 0.1 μF, Erie Red Cap
L1 – 24 nH, #14 Wire, l = 1.2"
L2 – 12 nH, #14 Wire, l = 0.6"
L3 – 24 nH, #14 Wire, l = 1.2"
Board – G10, εR = 5, t = 0.062", l = 8.0", W = 4.0"
Q1 – 2N5192
Q2 – 2N5194
Q3 – MRF309
Q4 – MRF309
D1 – 1N4001

100 WATT 420-450 MHz PUSH-PULL AMPLIFIER

build the impedances up to workable levels before doing any combining. Second, notice the bias circuit (Q1, Q2, D1). This arrangement gives you a stiff source, without as high a DC power loss as was necessary with the simple diode arrangement of the previous schematic.

Some advantages of the push-pull configuration, compared to using two devices in parallel, are:

1) Easier input and output matching due to higher impedance levels.

2) Suppression of even harmonics. This is the classic advantage cited for push-pull stages. However, there are some traps. For example, if in a Class C stage you have capacitive coupling between each device and the output, you may find that the second harmonic is much higher than in the equivalent single ended stage.

3) Collector by-passing is less critical. This is true but don't get carried away.

4) Emitter grounding is less critical. In a push-pull stage it is the emitter-to-emitter path that is more important than the emitter-to-ground path. If you mount the two devices in the same package, where the emitter-to-emitter leads can be real short you can reduce problems considerably. The push-pull package is becoming more common in VHF and UHF devices.

5) The load sharing is better than the equivalent two devices in parallel.

REFERENCES FOLLOW

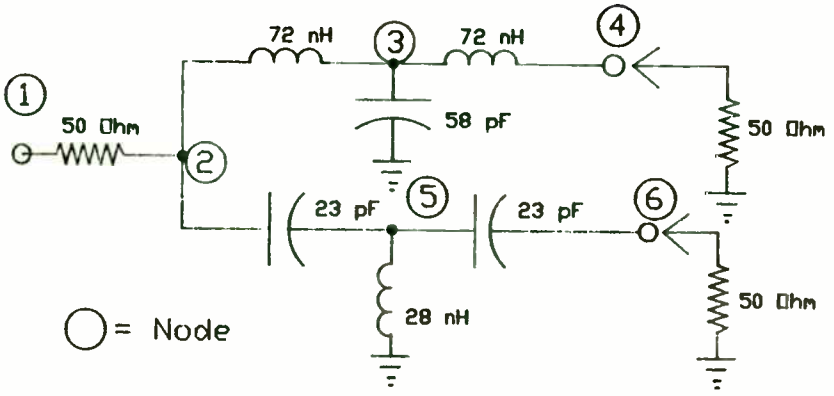


FIGURE 1

Prototype Diplexer Design

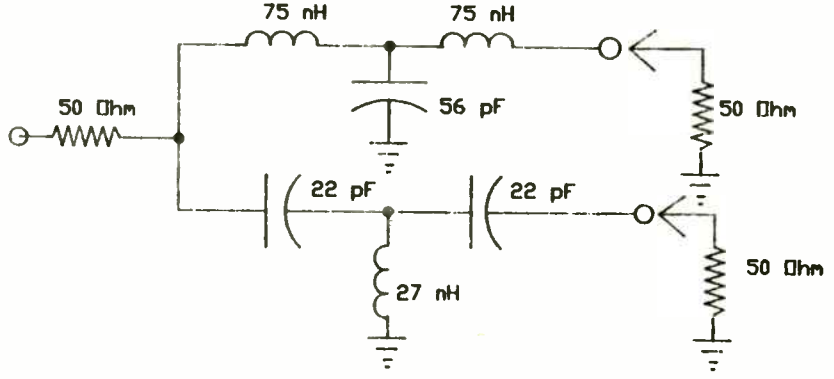


FIGURE 3

Diplexer Design using RETMA Values

LOW-PASS SECTION

FREQ=	8.0000E+07	AMPL=	4.56E-01	20LOG=	-6.8	PHASE=	-105.7
FREQ=	8.5000E+07	AMPL=	4.52E-01	20LOG=	-6.9	PHASE=	-113.1
FREQ=	9.0000E+07	AMPL=	4.49E-01	20LOG=	-7.0	PHASE=	-120.9
FREQ=	9.5000E+07	AMPL=	4.48E-01	20LOG=	-7.0	PHASE=	-129.1
FREQ=	1.0000E+08	AMPL=	4.47E-01	20LOG=	-7.0	PHASE=	-138.1
FREQ=	1.0500E+08	AMPL=	4.46E-01	20LOG=	-7.0	PHASE=	-148.2
FREQ=	1.1000E+08	AMPL=	4.42E-01	20LOG=	-7.1	PHASE=	-160.0
FREQ=	1.1500E+08	AMPL=	4.27E-01	20LOG=	-7.4	PHASE=	-173.6
FREQ=	1.2000E+08	AMPL=	3.94E-01	20LOG=	-8.1	PHASE=	171.2
FREQ=	1.2500E+08	AMPL=	3.40E-01	20LOG=	-9.4	PHASE=	155.7
FREQ=	1.3000E+08	AMPL=	2.75E-01	20LOG=	-11.2	PHASE=	142.0
FREQ=	1.3500E+08	AMPL=	2.13E-01	20LOG=	-13.4	PHASE=	131.6
FREQ=	1.4000E+08	AMPL=	1.62E-01	20LOG=	-15.8	PHASE=	124.7
FREQ=	1.4500E+08	AMPL=	1.25E-01	20LOG=	-18.1	PHASE=	121.1
FREQ=	1.5000E+08	AMPL=	9.77E-02	20LOG=	-20.2	PHASE=	120.1

HIGH-PASS SECTION

FREQ=	8.0000E+07	AMPL=	3.54E-02	20LOG=	-29.0	PHASE=	-136.8
FREQ=	8.5000E+07	AMPL=	4.11E-02	20LOG=	-27.7	PHASE=	-134.5
FREQ=	9.0000E+07	AMPL=	4.89E-02	20LOG=	-26.2	PHASE=	-130.4
FREQ=	9.5000E+07	AMPL=	6.12E-02	20LOG=	-24.3	PHASE=	-125.5
FREQ=	1.0000E+08	AMPL=	8.13E-02	20LOG=	-21.8	PHASE=	-121.8
FREQ=	1.0500E+08	AMPL=	1.13E-01	20LOG=	-18.9	PHASE=	-121.4
FREQ=	1.1000E+08	AMPL=	1.60E-01	20LOG=	-15.9	PHASE=	-125.3
FREQ=	1.1500E+08	AMPL=	2.22E-01	20LOG=	-13.1	PHASE=	-133.9
FREQ=	1.2000E+08	AMPL=	2.93E-01	20LOG=	-10.7	PHASE=	-146.4
FREQ=	1.2500E+08	AMPL=	3.57E-01	20LOG=	-8.9	PHASE=	-161.1
FREQ=	1.3000E+08	AMPL=	4.03E-01	20LOG=	-7.9	PHASE=	-175.9
FREQ=	1.3500E+08	AMPL=	4.28E-01	20LOG=	-7.4	PHASE=	171.0
FREQ=	1.4000E+08	AMPL=	4.39E-01	20LOG=	-7.1	PHASE=	160.1
FREQ=	1.4500E+08	AMPL=	4.43E-01	20LOG=	-7.1	PHASE=	151.0
FREQ=	1.5000E+08	AMPL=	4.45E-01	20LOG=	-7.0	PHASE=	143.4

FIGURE 2 - CALCULATED VALUES OF DIPLEXER

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END

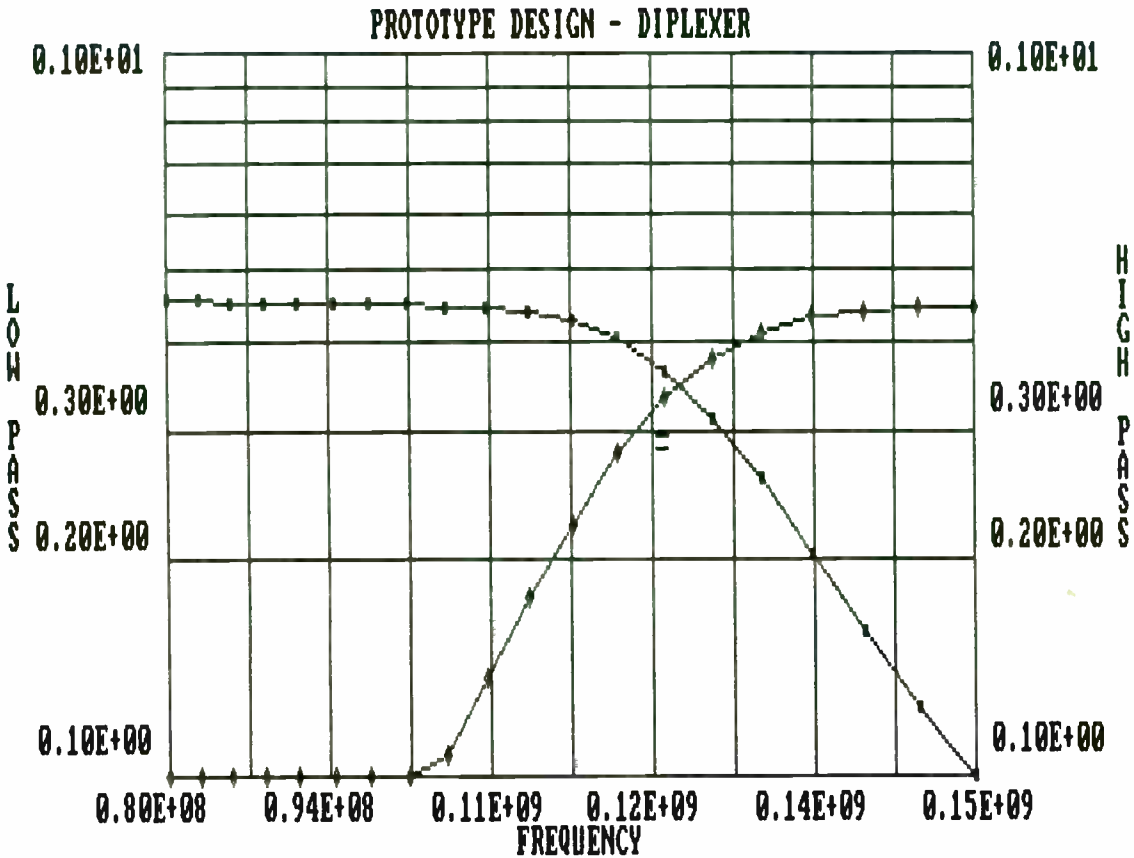

FIGURE 2(6)

LOW-PASS SECTION

FREQ=	8.0000E+07	AMPL=	4.62E-01	20LOG=	-6.7	PHASE=	-105.9
FREQ=	8.5000E+07	AMPL=	4.58E-01	20LOG=	-6.8	PHASE=	-113.4
FREQ=	9.0000E+07	AMPL=	4.55E-01	20LOG=	-6.8	PHASE=	-121.2
FREQ=	9.5000E+07	AMPL=	4.53E-01	20LOG=	-6.9	PHASE=	-129.4
FREQ=	1.0000E+08	AMPL=	4.52E-01	20LOG=	-6.9	PHASE=	-138.3
FREQ=	1.0500E+08	AMPL=	4.50E-01	20LOG=	-6.9	PHASE=	-148.3
FREQ=	1.1000E+08	AMPL=	4.46E-01	20LOG=	-7.0	PHASE=	-159.6
FREQ=	1.1500E+08	AMPL=	4.33E-01	20LOG=	-7.3	PHASE=	-172.6
FREQ=	1.2000E+08	AMPL=	4.06E-01	20LOG=	-7.8	PHASE=	172.8
FREQ=	1.2500E+08	AMPL=	3.59E-01	20LOG=	-8.9	PHASE=	157.5
FREQ=	1.3000E+08	AMPL=	2.99E-01	20LOG=	-10.5	PHASE=	143.2
FREQ=	1.3500E+08	AMPL=	2.36E-01	20LOG=	-12.5	PHASE=	131.3
FREQ=	1.4000E+08	AMPL=	1.82E-01	20LOG=	-14.8	PHASE=	122.6
FREQ=	1.4500E+08	AMPL=	1.40E-01	20LOG=	-17.1	PHASE=	117.0
FREQ=	1.5000E+08	AMPL=	1.08E-01	20LOG=	-19.3	PHASE=	114.2

HIGH-PASS SECTION

FREQ=	8.0000E+07	AMPL=	3.23E-02	20LOG=	-29.8	PHASE=	-134.9
FREQ=	8.5000E+07	AMPL=	3.73E-02	20LOG=	-28.6	PHASE=	-132.7
FREQ=	9.0000E+07	AMPL=	4.40E-02	20LOG=	-27.1	PHASE=	-128.6
FREQ=	9.5000E+07	AMPL=	5.45E-02	20LOG=	-25.3	PHASE=	-123.5
FREQ=	1.0000E+08	AMPL=	7.16E-02	20LOG=	-22.9	PHASE=	-119.3
FREQ=	1.0500E+08	AMPL=	9.88E-02	20LOG=	-20.1	PHASE=	-118.0
FREQ=	1.1000E+08	AMPL=	1.39E-01	20LOG=	-17.1	PHASE=	-120.7
FREQ=	1.1500E+08	AMPL=	1.94E-01	20LOG=	-14.2	PHASE=	-127.9
FREQ=	1.2000E+08	AMPL=	2.59E-01	20LOG=	-11.7	PHASE=	-139.1
FREQ=	1.2500E+08	AMPL=	3.24E-01	20LOG=	-9.8	PHASE=	-152.8
FREQ=	1.3000E+08	AMPL=	3.76E-01	20LOG=	-8.5	PHASE=	-167.3
FREQ=	1.3500E+08	AMPL=	4.09E-01	20LOG=	-7.8	PHASE=	179.2
FREQ=	1.4000E+08	AMPL=	4.27E-01	20LOG=	-7.4	PHASE=	167.6
FREQ=	1.4500E+08	AMPL=	4.36E-01	20LOG=	-7.2	PHASE=	157.8
FREQ=	1.5000E+08	AMPL=	4.40E-01	20LOG=	-7.1	PHASE=	149.6

FIGURE 4 - VALUES ADJUSTED TO NEAREST RETMA VALUES

AN EVOLUTION OF OPTIMIZATION AND SYNTHESIS PROGRAMS FOR PERSONAL COMPUTERS

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AN EVOLUTION OF OPTIMIZATION AND SYNTHESIS PROGRAMS FOR PERSONAL COMPUTERS

by

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ABSTRACT

Two personal-computer programs for RF/microwave applications - CIAO for analysis and optimization, and DESIGN for matching network synthesis - have undergone substantial revision since their introduction over a year ago. CIAO is now a much more powerful program, with the inclusion of rapid sparse-matrix techniques, a choice of three different optimization algorithms, and high resolution graphics output. DESIGN has a greatly improved user interface and, with the inclusion of a fine-tuning option, is now able to consiatently synthesize lumped and distributed matching networks with response errors on the order of a small fraction of a dB. Thia paper discusses the evolution of CIAO and DESIGN to their present states.

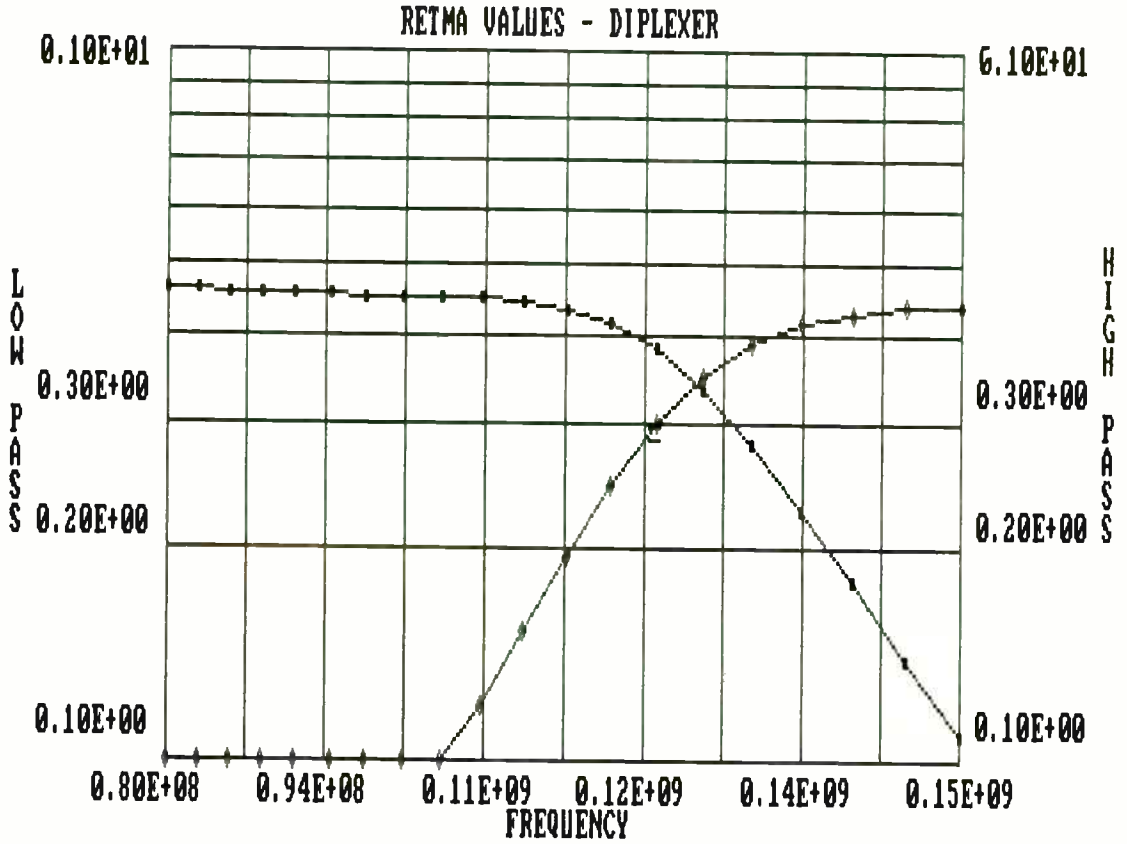

Figure 4(6)

I. INTRODUCTION

CIAO: Circuit Analysis and Optimization on Personal Computers

CIAO, a program for MS-DOS and CP/M personal computers, performs the analysis and optimization of microwave and RF networks in the frequency domain. The initial version of the program was first demonstrated at RF Technology Expo '85 [1]. Since that time, a number of features have been added to the program, significantly improving its capabilities and performance. After a brief review of the original CIAO, we shall present a discussion of the evolution of CIAO to its current state. A circuit optimization example will illustrate the many benefits of CIAO's upgrading.

DESIGN: Automated Matching Network Design on Personal Computers

After the discussion of CIAO, we shall present the newest version of DESIGN, a program for performing the automated synthesis of lumped and distributed matching networks between real sources and complex loads. DESIGN has been improved over its previous release [1] by enhancing the user interface and by adding a fine-tuning option, which enables virtually all matching network designs to meet specifications to within a small fraction of a dB. An example will illustrate the capabilities of the new DESIGN.

II. The Evolution of CIAO

The Capabilities of CIAO: Original Version

CIAO can analyze and optimize circuits comprising the following elements: resistors; capacitors; inductors; (lossy) transmission lines; controlled sources (with delay); one-ports, two-ports and three-ports described by tables of S, Y, or Z parameters; and gyrators. Scattering parameters for the circuit are calculated between either real or complex loads over a frequency band. The magnitude, phase, and/or phase-shape of any number of the S-parameters may be optimized to achieve specified design goals. Generally, for optimization, new sets of element values are found to minimize the error between the calculated and desired S-parameter values.

In the original version of CIAO, the Fletcher-Reeves [2] gradient optimizer was available, highly efficient and accurate adjoint techniques [3] were used to calculate the gradients required by the optimizer, and a "dense" linear equation solver was used in the analysis routines. There was no graphics output. The new CIAO offers a choice of three optimizers, a sparse matrix solver, and simultaneous text and high resolution graphics on a single screen. The benefits of these additions will now be described.

The New CIAO: Three Available Optimizers

CIAO now offers a choice of two gradient algorithms and one random-grid algorithm for circuit optimization. For a given network problem, one method will prove superior to the others; sometimes the best results can be achieved

by applying one algorithm and then switching to another.

The available gradient optimizers are the Fletcher-Reeves (F-R) and Fletcher-Powell (F-P) [4] methods. Both of these use information obtained from the gradient of the error function to search for the minimum. When far from a minimum, F-R and F-P both behave like a steepest-descent method and converge at about the same rate. When close to a minimum, F-P converges faster than F-R because F-P starts acting more like a Newton-Raphson method, which has a quadratic rate of convergence. These properties of the F-R and F-P methods apply exactly only to functions with "locally quadratic" behavior. In practical circuit problems, the error function may or may not have this characteristic. Experience has shown us, however, that F-P is usually superior to F-R, although there are instances where F-R does work better.

CIAO also provides the choice of the Nelder-Mead (N-M) [5] random-grid-search method. In this algorithm, the error function is evaluated several times for a range of element values - i.e. over a "grid" in the vector space of optimizable element values - and from this a "better" set of circuit parameters is deduced. N-M, like most random-grid methods, is generally able to avoid convergence to local minima, although sometimes the number of function evaluations required becomes large. The algorithm is also very effective in those circuit problems where the response is not too sensitive to small changes in the network parameters. Such a situation arises, for example, when optimizing the passband of a lossless, doubly-terminated filter or matching network. This is so because the first-order sensitivity of S21 to the component values of such a network is zero at frequencies corresponding to maximum transfer of power between the source and load [6].

CIAO, with its three optimizers, provides sufficient flexibility to handle the most difficult circuit optimization problems.

The New CIAO: Sparse Matrix Techniques

Both the analysis and optimization performed in CIAO involve repeatedly constructing and solving the linear nodal equations of a circuit to obtain scattering parameters. The conventional means of solving linear equations, such as Gaussian elimination or LU factorization, generally requires a number of mathematical operations proportional to n^3, i.e. the cube of the number of nodes in the circuit. Many of these mathematical operations involve multiplications by zero, because the typical nodal admittance matrix Y is sparse, i.e. contains only a small percentage of nonzero entries. For example, the percentage density of nonzero entries in Y for a ten-node ladder network is 28%, while for a twenty-node ladder the density falls to under 15%. Clearly, if the useless multiplications by zero were eliminated in solving the linear equations, a great increase in processing speed would be realized.

Sparse matrix techniques consist of specialized algorithms for solving linear equations by working only on the nonzero entries of the coefficient matrix. For typical nodal equations, the number of mathematical operations required for solution is linearly proportional to n, the number of nodes. Obviously, an enormous saving in processing time is realized by using sparse

The Schottky Diode Mixer

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INTRODUCTION

A major application of the Schottky diode is the production of the difference frequency when two frequencies are combined or mixed in the diode. This mixing action is the result of the non-linear relationship between current and voltage, usually expressed as

$$I = I_s(e^{\frac{q(V-IR_s)}{nkT}} - 1)$$

The series resistance, R_s, is a parasitic element representing bulk resistance of the semiconductor and contact resistance. It is sometimes confused with dynamic resistance which is the sum of the series resistance and the resistance of the junction where the frequency conversion takes place. The ideality factor, n, is unity for an ideal diode and less than 1.1 for a silicon Schottky diode.

Variations in n are not important for n less than 1.1. The effect of saturation current, Is, is very important when the level of local oscillator power is low. This will be demonstrated by comparing results of mixing with diodes having different values of saturation current. Although temperature, T, is seen in the exponential and is present in a more complicated manner in saturation current, the effect on mixing efficiency is less than 0.5 dB for 100 degrees C change in temperature. Electron charge, q, and Boltzmann constant, k, may be combined in the equation

$$I = I_s(e^{\frac{V-IR}{.026}} - 1) \qquad (1)$$

Conversion Loss

Mixing efficiency is measured by the conversion loss, the ratio of signal input power to intermediate frequency output power. The intermediate frequency is the difference between the signal frequency and the local oscillator frequency. The diode may also generate the sum of these two frequencies. In this case the mixer may be called an upconverter. For a given local oscillator frequency, the difference frequency may be produced by two signal frequencies - one above the l.o. frequency and one below. Of course noise is also contributed at these two frequencies. In some cases, the mixer is designed to respond to both these frequencies. A mixer of this type is called a double sideband mixer. More commonly the mixer is designed to respond to one of these inputs. Since noise comes from both frequencies the double sideband mixer is better - typically 3 dB better.

Noise figure is another measure of mixing efficiency. This is the ratio of signal to noise ratio at the input to signal to noise ratio at the output. Single and double sideband definitions apply to noise figure also. In some applications noise figure and conversion loss are essentially equal. However, noise figure includes diode noise which becomes significant at intermediate frequencies in the audio range (1/f noise). In these applications noise figure may be much larger than conversion loss.

matrix methods in circuit analysis and optimization.

CIAO now employs a sophisticated sparse matrix equation-solving algorithm, and the resulting increase in processing speed has been impressive, as compared to the original CIAO, which used the conventional "dense" solver. For example, with the sparse solver, the analysis and optimization speeds for various ladder networks improved as follows: (1) four-node network - ran 1.04 times faster; (2) ten-node network - ran twice as fast; (3) twenty-one node network - ran ten times faster. Generally, the larger and sparser the network, the greater will be the advantage that sparse matrix techniques realize over dense solvers.

The New CIAO: Graphics Output and Other Enhancements

CIAO's normal screen-output mode now provides simultaneous text and high-resolution graphics output. In CIAO's graphics mode, which is the default option, the upper half of the screen displays the text output. This consists of the program queries directed to the user, and the analysis and optimization results for the circuit. The user may redirect this text output to the printer. The graphics output from CIAO appears in the bottom half of the screen.

The graphics output is generated automatically by CIAO according to certain default options. By including the appropriate command in the data file, the user may override the defaults either to plot the magnitude or phase of any scattering parameter, or to suppress graphics output altogether. When the graphics mode is activated, a plot is generated for the initial analysis of the circuit and for each optimizing iteration after the initial analysis. After three plots are constructed on the coordinate axes, the graph is erased and a new set of axes is constructed, possibly with a different ordinate scale. As the iterations proceed, another three plots are drawn. At this point, the graph is refreshed again. The process repeats until the desired number of iterations is completed. Each plot of a group of three is distinguishable by the intensity of the trace on the screen, and by either dot, cross, or box marks on the plot at the frequency points specified in the data file.

Hardcopy output of the screen's graphics images is possible via the GRAPHICS.COM program, which comes with most MS-DOS 2.x operating systems. Before running CIAO, one need only execute GRAPHICS.COM; then at any time during or after a CIAO execution, Shift-PrtSc will dump the screen image to the printer.

Automatic Updating of Data Files. Whenever an optimization is concluded or interrupted, the user may, in response to screen query, direct CIAO to save to disk a new data file with the current values of the optimizable circuit elements. This feature makes it very easy to start, stop, and resume an optimization of a circuit - even changing the optimization algorithm along the way, if so desired.

Improved Interrupt Handling. CIAO's analysis and optimization maybe interrupted instantly by holding down any key. Execution may be then terminated with a final analysis or continued, as desired.

Another complication of noise figure is the effect of the amplifier following the mixer. Diode manufacturers include the effect of a 1.5 dB noise figure IF amplifier in the mixer noise figure. Mixer manufacturers do not include this amplifier in the mixer noise definition. In this paper diode efficiency will be measured by conversion loss.

Parasitic Losses

The diode equivalent circuit of Figure 1 shows the presence of two elements that degrade performance by preventing the incoming signal from reaching the junction resistance where the mixing takes place. The effect of junction capacitance and series resistance was studied by comparing conversion loss data measured with three diodes covering a wide range of these parameters. The 5082-2800 is a general purpose diode, typically used in switching circuits. The 5082-2817 is a 2 GHz mixer diode. The 5082-2755 is a 10 GHz detector diode. Figure 2 shows the conversion loss measured at 2 GHz for these three diodes.

The 5082-2800 general purpose diode has a conversion loss several dB worse than that of the other diodes. This is expected because this diode has a higher junction capacitance. The behavior of the low capacitance 5082-2755 detector diode is more interesting. At local oscillator power levels below -3 dBm the conversion loss is better than the loss of the 5082-2817 mixer diode, but at higher power levels it is worse.

A good approximation to the effect of junction capacitance and series resistance on conversion loss is:

$$L_1 = 1 + \frac{R_s}{R_j} + \omega^2 C_j^2 R_s R_j \qquad (2)$$

This is the ratio of available power to the power delivered to the junction resistance, R_j, using the diode equivalent circuit of Figure 1. The value of junction capacitance varies with voltage as

$$C_j = \frac{C_o}{\sqrt{1 - \frac{V}{0.6}}} \qquad (3)$$

where 0.6 is a typical value of barrier voltage.

The relative values of conversion loss in Figure 2 may be explained by these equations. Zero bias capacitances for the three diodes were measured to be 0.84 pF, 1.29 pF, and 0.13 pF for the -2817, -2800, and -2755 diodes respectively.

At a local oscillator power level of 1 milliwatt the forward current is about 1 milliampere. Using the corresponding forward voltages, C_j is computed for the three diodes. Assuming a junction resistance of 150 ohms, reasonable values of series resistance may be chosen to make the relative values of L_1 correspond to the relative measured values.

The familiar junction resistance equation $R_j = \frac{26}{I}$ does not apply for I= rectified current. It refers to I= DC bias current. When

III. An Optimization Example for the New CIAO

Presented below are a data file, circuit diagram, and partial program output for an optimization example run using the new CIAO. The data file contains comments which explain the optimization process for the circuit. (Comment lines are denoted by an apostrophe being the first character on the line; blank lines are also allowed. CIAO also permits text comments to be appended to any line.) The circuit is described in a nodal-interconnect format and the optimizable parameters are denoted by an asterisk appended to the element codes.

```
'   CIAO DATA FILE:  OPTIMIZATION OF A FOUR-STAGE GaAs FET AMPLIFIER
'   ---- ---- ----   ------------ -- - ---- ----- ---- --- ---------

'CIAO is used here to optimize a four-stage, 21-node amplifier to
'(1) a prescribed S11 magnitude and phase (for noise figure), (2)
'a flat 30 dB gain for S21, and (3) an S22 magnitude of below
'0.20.  The initial design of the amplifier  displays a
'satisfactory match for S22, a poor match for S11, and a maximum
'gain error for S21 of 4.3 dB.  The optimized design still
'displays a satisfactory match for S22, a greatly improved match
'for S11, and a maximum gain error for S21 of 0.4 dB.

'The optimization was stopped after 4 Nelder-Mead iterations,
'which required a total of 91 function evaluations.  In this
'particular example, neither Fletcher-Powell nor Fletcher-Reeves
'alone is able to achieve results anywhere nearly as good as those
'achieved with Nelder-Mead.

'       TYPE of OPTIMIZATION:  Nelder-Mead
'       RUN-TIME for the INITIAL ANALYSIS:  2.1 sec. per frequency point
'       TOTAL RUN-TIME for ITR. 0 - 4  (91 fn. eval.):  19 min. 11 sec.

'Using the dense solver of the original CIAO, the above run-times
'increase by a factor of TEN.
'- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

ind 1 2 .05e-9
cap 2 3 8.2e-12
   'For trl, ost: Zo, Length (deg.) Freq.
trl_* 3 0 4 0     50  69.48          7.5e9
ost_* 3 0 50 49.72 7.5e9
two 4 0 5 0 table1

cap 5 6 8.2e-12
ind 6 7 .05e-9
trl_* 7 0 8 0 50 75.6 7.5e9
ost_* 8 0 50 43.3 7.5e9
two 8 0 9 0 table2

cap 9 10 8.2e-12
ind 10 11 .05e-9
trl_* 11 0 12 0 50 61.98 7.5e9
two 12 0 13 0 table3

cap 13 14 8.2e-12
ind 14 15 .05e-9
ost_* 15 0 50 59.33 7.5e9
trl_* 15 0 16 0 50 31.43 7.5e9
two 16 0 17 0 table3

cap 17 18 8.2e-12
ind 18 19 .05e-9
trl_* 19 0 20 0 50 48.24 7.65e9
ost_* 20 0 50 50.89 7.65e9
trl_* 20 0 21 0 50 57.24 7.65e9
ost_* 21 0 50 21.31 7.65e9

port1 1 0 50
port2 21 0 50
perform twoport optimization table9
'Optimization goal: match circuit S-Parameters to those of table 9
end

'frequencies              Mag./Phase weights for Sij
7.250e9 7.750e9  0.1e9  \  645.2/.1  0  1/0  10e4/0.,0.2/0
end

table1 sparam (first device)
50  (Reference impedance for S parameters)
.79 -137  .04 33  1.50 59  .75 -74
.79 -139  .04 34  1.48 58  .76 -76
.79 -139  .04 35  1.45 57  .76 -77
.79 -140  .04 36  1.42 57  .77 -78
.79 -141  .03 37  1.39 56  .77 -79
.79 -142  .03 38  1.37 55  .78 -81

table2 sparam (second device)
50
.78 -135  .03 68  1.88 59  .75 -81
.78 -136  .03 70  1.84 58  .76 -82
.78 -137  .03 72  1.80 57  .76 -83
```

rectified current is 1 mA, instantaneous current varies over forward and reverse values. Junction resistance is very large when the current is negative so the average junction resistance is larger than predicted by this equation.

Diode	C (pF)	R (ohms)	L (dB)
2817	1.3	6	1.07
2800	2.2	16	4.68
2755	0.24	50	1.47

At -3 dBm the 2817 and 2755 curves cross, with the 2800 loss 4.5 dB higher. This relative loss can be explained by raising R to 235 ohms and decreasing the capacitance values.

Diode	C (pF)	L (dB)
2817	1.12	1.2
2800	2.1	5.7
2755	0.23	1.2

These values of C_j and R_s were chosen to illustrate the effect on conversion loss. Since saturation currents are different for these diodes and junction resistances may be different, the actual values of C_j and R_s may be somewhat different.

Equation 2 shows the loss behavior with frequency. At low frequencies the loss is independent of frequency and capacitance. Choosing a low value of series resistance provides the best diode. At high frequencies low capacitance becomes more important than low series resistance because capacitance is squared in the equation. Figure 3 shows L_1 vs frequency for the 5082-2835 diode with R_s = 6 ohms and C_j = 1.0 pF and for the HSCH-5310 diode with R_s = 17 ohms and C_j = 0.1 pF. The lower capacitance makes the -5310 the better diode at microwave frequencies while the lower resistance makes the -2835 the better diode at low frequencies.

The Effect of Barrier Voltage

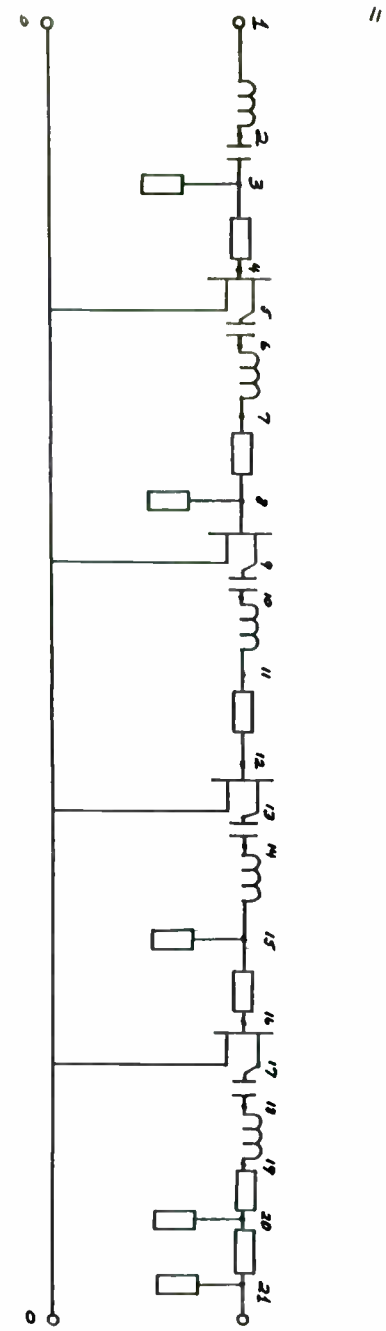
The type of metal deposited on silicon to form a Schottky barrier influences the barrier voltage which is involved in the saturation current determining the forward current. We use the term low barrier for diodes with low values of voltage for a given current (usually 1 mA). We have previously shown the effect of barrier voltage on the variation of junction capacitance with forward voltage.

Figure 4 shows the measurement of conversion loss for three diodes having a range of barrier potential values.

Diodes	Barrier Potential
5082-2817	0.64
5082-2835	0.56
HSCH-3486	0.35

```
.78 -138  .03 74  1.77 57  .77 -85
.79 -139  .03 75  1.74 56  .77 -86
.79 -140  .03 77  1.70 55  .78 -87

table3 sparam  (third and fourth devices)
50
.78 -147  .155 -37.6  1.14 -33.0  .76 -129
.78 -148  .157 -43.8  1.13 -34.9  .76 -130
.78 -149  .158 -49.7  1.11 -36.7  .76 -130
.78 -150  .159 -55.4  1.10 -38.5  .76 -131
.78 -151  .160 -60.9  1.09 -40.2  .76 -132
.78 -152  .160 -66.1  1.07 -41.9  .76 -133

table9 sparam  (optimizing table)
'match s11 for noise figure; s21 for 30dB gain; s22 for min. value
.86 -19  0 0  31.622 0  0 0
.89 -29  0 0  31.622 0  0 0
.90 -39  0 0  31.622 0  0 0
.91 -47  0 0  31.622 0  0 0
.87 -54  0 0  31.622 0  0 0
.86 -62  0 0  31.622 0  0 0
end
'- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

The circuit diagram and (partial) program output are given on the next two pages.



At low LO power levels the lower barrier diodes have better performance, significantly better for the lowest barrier diode, the HSCH-3486. At higher power levels this diode loses its advantage because of higher series resistance. The 5082-2835 has lower capacitance and lower series resistance so its performance is better than the 5082-2817 at all power levels. The maximum rated power level of 150 mW is not high enough to demonstrate the increase in conversion loss seen at high power levels for the other diodes.

Effects of DC Bias and Local Oscillator Power Level

Figure 5 shows the conversion loss of a 5082-2817 mixer diode measured at 2 GHz. The top curve was measured without DC bias. Optimum DC bias was applied at each level for the bottom curve. The curves meet at the optimum local oscillator level where bias does not help. Below this level forward bias is used. Above this level reverse bias is used to reduce the rectified current.

At low levels of LO power, the conversion loss degrades rapidly unless DC bias is used. At -10 dBm the degradation is about 7 dB from the performance at the standard 0 dBm power level. Replacing the lost LO power with DC bias recovers about 6 dB of the degradation.

At high levels of LO power the performance degrades again. This is caused by the rapid increase of junction capacitance. Reverse bias reduces the current and the capacitance, restoring the diode performance.

Effect of Load Resistance

Figure 6 shows the effect of mixer load resistance on conversion loss. At low local oscillator power levels the effect is similar to the barrier effect. More rectified current flows with smaller load resistance so performance is better. At higher power levels the degradation due to higher capacitance appears first with the lower load resistances. As a result the optimum value of load resistance increases with LO power level. At +9 dBm 100 ohms becomes better than 10 ohms. AT +19.5 dBm 400 ohms becomes better than 100 ohms. The load circuit can be designed to provide the optimum resistance as the local oscillator power level changes.

HARMONIC DISTORTION

Sums and differences of multiples of the two mixing frequencies are produced in the mixing diode. These frequencies appear as spurious responses in the output. This effect was studied by setting the signal frequency at 2 GHz and the power at -30 dBm. The local oscillator was then set at various frequencies to produce harmonic mixing with a difference frequency of 30 MHz. Local oscillator power was one milliwatt. Then the local oscillator was set at 2 GHz and the signal frequency varied. The output levels in dB below fundamental mixing are shown in Figure 7. The diode was placed in a 50 ohm untuned coaxial mount.

The output levels of the m1 products, mixing of the signal fundamental with multiples of the local oscillator, are much higher than

CIAO Output for 4-Stage Amplifier Example

CIRCUIT ANALYSIS and OPTIMIZATION PROGRAM

Initial Analysis

Freq.	S11		S12		S21		S22		S21	K
(Hz)	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	dB	Fact
7.250E+009	0.78	-36	-67.8dB	-58.5	51.934	-32.3	0.08	-66	34.3	9.1
7.350E+009	0.76	-45	-68.5dB	-90.5	44.087	-60.7	0.11	-59	32.9	12.6
7.450E+009	0.74	-49	-69.5dB	-116.9	36.102	-83.9	0.10	-66	31.2	18.5
7.550E+009	0.74	-55	-70.3dB	-145.3	30.748	-107.5	0.07	-87	29.8	24.2
7.650E+009	0.73	-57	-73.7dB	-171.5	25.733	-130.1	0.01	-114	28.2	43.6
7.750E+009	0.74	-62	-75.0dB	163.0	20.689	-153.6	0.07	57	26.3	60.1

Iteration number: 0 - using 1 function evaluation(s).
Error function: 147.877

Magnitude errors [11,12,21,22]: 1.20E+001 0.00E+000 1.24E+002 0.00E+000
Phase errors [11,12,21,22]: 1.20E+001 0.00E+000 0.00E+000 0.00E+000

Variable	Value
1	4.97200E+001
2	6.94800E+001
3	7.56000E+001
4	4.33000E+001
5	6.19800E+001
6	5.93300E+001
7	3.14300E+001
8	4.82400E+001
9	5.08900E+001
10	5.72400E+001
11	2.13100E+001

Iteration number: 1 - using 28 function evaluation(s).
Error function: 90.539

Magnitude errors [11,12,21,22]: 1.47E+000 0.00E+000 8.03E+001 5.04E-001
Phase errors [11,12,21,22]: 8.23E+000 0.00E+000 0.00E+000 0.00E+000

Variable	Value
1	4.65707E+001
2	7.47423E+001
3	6.98742E+001
4	4.65794E+001
5	5.96321E+001
6	5.75146E+001
7	3.50699E+001
8	5.09605E+001
9	4.91413E+001
10	6.15752E+001
11	1.96960E+001

CIAO Output (cont'd)

Iteration number: 2 - using 9 function evaluation(s).
Error function: 6.292

Iteration number: 3 - using 51 function evaluation(s).
Error function: 4.938

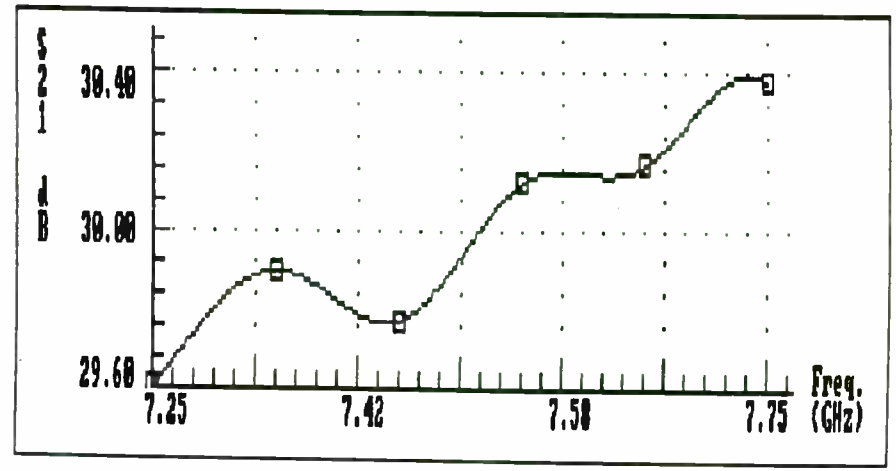
Iteration number: 4 - using 2 function evaluation(s).
Error function: 4.281

Magnitude errors [11,12,21,22]: 5.04E-001 0.00E+000 8.80E-001 0.00E+000
Phase errors [11,12,21,22]: 2.90E+000 0.00E+000 0.00E+000 0.00E+000

Variable	Value
1	4.68837E+001
2	7.71597E+001
3	5.97823E+001
4	4.47366E+001
5	5.52477E+001
6	5.71373E+001
7	3.31566E+001
8	5.31364E+001
9	5.30837E+001
10	5.39265E+001
11	2.40746E+001

Final Analysis

Freq.	S11		S12		S21		S22		S21	K
(Hz)	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	dB	Fact
7.250E+009	0.86	-28	-72.5dB	10.9	30.217	37.1	0.15	156	29.6	17.7
7.350E+009	0.89	-37	-71.5dB	-13.5	31.259	16.3	0.07	95	29.9	12.5
7.450E+009	0.91	-43	-70.8dB	-37.7	30.810	-4.7	0.08	10	29.8	10.0
7.550E+009	0.93	-49	-69.9dB	-63.0	32.078	-25.2	0.13	-33	30.1	6.7
7.650E+009	0.90	-56	-71.8dB	-89.0	32.238	-47.6	0.16	-57	30.2	10.7
7.750E+009	0.92	-62	-70.9dB	-117.9	33.011	-74.5	0.17	-77	30.4	8.0



the in products, mixing of the local oscillator fundamental with multiples of the signal. For example, the 2x1 output is 5 dB below fundamental. Figure 5 shows that this level of fundamental mixing corresponds to a local oscillator level of -8 dBm. The doubling efficiency was about 8 dB. The 1x2 output is 16 dB below fundamental mixing. This corresponds to a signal level of -46 dBm. The doubling efficiency is 16 dB for the lower level signal frequency. Although fundamental mixing in Figure 5 was measured in a tuned system and the data of Figure 7 was measured in an untuned system, this analysis nevertheless gives a comparison of multiplying at the one milliwatt and one microwatt power levels. Mixing of signal multiples above 2 with local oscillator multiples above the fundamental produced outputs below the -100 dBm sensitivity of the receiver.

Harmonic Mixing

While harmonic products are usually considered spurious, in some designs the desired output is the result of harmonic mixing. This is a valuable mixer technique when the frequency is so high that it is difficult to generate the local oscillator power. Hewlett-Packard Application Note 991, "Harmonic Mixing With the HSCH-5500 Series Dual Diode" describes a technique using the 2nd harmonic of the local oscillator with little loss of efficiency compared to fundamental mixing. Mixers using the 6th, 8th, and 10th harmonics are used to extend the range of Hewlett-Packard spectrum analyzers to 60 GHz.

Two Tone Distortion

Harmonic distortion may be suppressed by a band pass filter at the mixer input. When the distortion is caused by

$$m f_{LO} - n f_s = f_{if}$$

the unwanted frequency is

$$f_s = \frac{m}{n} f_{LO} - \frac{f_{if}}{n} \qquad (4)$$

The narrowest filter required corresponds to m = n = 2 with a rejection bandwith equal to the intermediate frequency.

Two tone distortion is the result of two unwanted signals mixing with each other and the local oscillator to produce an intermediate frequency output. The equation is

$$f_{LO} - m f_1 + n f_2 = f_{if} \qquad (5)$$

Third order two tone intermod may correspond to m = 2, n = 1. In this case the correct intermediate frequency is produced when the desired signal f_s equals $2f_1 - f_2$. The unwanted frequencies may be arbitrarily close to the desired frequency so the problem cannot be solved with a filter.

Third order two tone distortion in a 5082-2817 diode was investigated with a local oscillator frequency of 1.94 GHz and input

IV. The Evolution of DESIGN

The Capabilities of DESIGN: Original Version

DESIGN synthesizes lossless lumped and distributed matching networks to provide a specified S21 magnitude response between a real source and a complex load impedance. The method is discussed in [1] and is based on the work of Carlin and Komiak [7]. The most important advantages of DESIGN are: (1) no equivalent circuit models need be constructed for the source and load - only a simple numerical description of the source and load is required as data for the synthesis; (2) the designs are "simpler in structure and superior in frequency response to [classical] equiripple designs" [8]; and (3) no parasitic absorptions or Norton/Kuroda transformations are required in the synthesis.

The original DESIGN was generally able to synthesize networks that were at most a few dB within the S21 requirements across the frequency band. In any event, the response was close enough to specifications to enable a circuit optimizer (such as CIAO) to reduce the error to a small value. The new DESIGN has enhancements which eliminates the need for such optimization after the synthesis.

The New DESIGN

DESIGN now has an internal fine-tuning option, as well as certain algorithmic enhancements, which enable the program, by itself, to design its networks with response errors not exceeding a small fraction of a dB. The fine-tuning option is actually a special purpose optimizer that has been built into the program. The other enhancements mainly involve the proper initial selection of the network topology to guarantee the success of the synthesis for all choices of the source and load. Finally, the user interface has been improved.

The example which follows will illustrate the new DESIGN's ease of use and excellent accuracy in synthesizing matching networks.

V. A Synthesis Example for the New DESIGN

We first summarize below the requirements for the matching network to be designed. This is followed by a statement concerning the options used in the DESIGN program. The user must select an appropriate value for the network degree; DESIGN suggests values for the other options. (Most often the defaults suffice.) Then the results of the synthesis are presented before and after the fine-tuning optimization. Finally, a copy of the actual printout of the program is given, along with a schematic of the networks and a plot of the frequency response.

frequencies of 2 GHz and 1.985 GHz. The intermediate frequency was 2 x 1.985 - 2 - 1.94 = 0.03 GHz. The measure of distortion is the input intercept point, the power level where the line of output vs input power for the desired mixing intersects the extension of the spurious line. This is shown in Figure 8. Since the desired output is linear, the suppression of the spurious output is 2A and input intercept is input power plus half the suppression.

With the help of this relationship the intercept point was measured as a function of local oscillator power level. The results are shown in Figure 9. At higher local oscillator power levels the desired output increases while the spurious output decreases. This raises the suppression and the intercept point. At lower levels both desired output and spurious decrease so the intercept point levels off to a constant value.

Tuning for Better Sensitivity

The ideal mixer should convert all of the signal power to output power at the desired output frequency. However, it is customary to test diodes in a broadband mixer circuit. In this test no attempt is made to recover the power lost in the unwanted output frequencies. Because of these losses and the losses in the diode parasitics, an efficiency of about 35% is usually achieved.

Special circuits have been developed to improve this figure to come closer to the ideal 100% efficiency. The most serious spurious response, called the image response, produces an output at the frequency $2 f_{LO} - f_S$. Image recovery mixers are designed to recover this lost power. Two dB improvement has been reported. By properly terminating harmonics up to the third, conversion loss under 2 dB was obtained with a Hewlett-Packard beam lead diode.

MULTIPLE DIODE MIXERS

Although the intermediate frequency may be produced by mixing in a single diode, very few mixers are made this way. The problems generated by using a single diode include radiation of local oscillator power from the input port, loss of sensitivity by absorption of input power in the local oscillator circuit, loss of input power in the intermediate frequency amplifier, and the generation of spurious output frequencies by harmonic mixing. Some of these problems may be solved by circuit techniques but these circuits often introduce new problems. Most mixers use multiple diode techniques to better solve these problems.

Early mixer designs prevented loss of signal power in the local oscillator circuit by loosely coupling the local oscillator power to the mixer diode. This technique is wasteful of local oscillator power and it sends as much power to the input, possibly an antenna, as it sends to the diode. This local oscillator radiation could be interpreted as a target return when received by a radar. This problem may be alleviated by using

MATCHING NETWORK DESIGN REQUIREMENTS

- Device Considered: Raytheon RLC832 Low Noise GaAs FET - Matching S11 to 50 ohms for maximum unilateral transducer gain
- Source Impedance: 50 ohms
- Number of Frequency Points: 5
- Load Description: Reflection coefficient with 50 ohm reference resistance

Frequency (GHz)	Load (Refl. Coef.) magnitude	phase-deg	Desired S21 Magnitude of Matching Network	
6.0	.78	-89	0.578	(-4.76 dB)
7.0	.75	-103	0.659	(-3.62 dB)
8.0	.73	-117	0.746	(-2.55 dB)
9.0	.70	-131	0.865	(-1.26 dB)
10.0	.67	-144	1.000	(0.00 dB)

OPTIONS SELECTED in DESIGN DATA INPUT

- Desired degree of matching network: ----- 5
- Bandpass or Lowpass matching network structure: ----- L
- Defaults used for all other options.

DESIGN RESULTS: (Preliminary, before fine-tuning)

- Lumped Circuit, S21 matched across frequency band to within 0.40 dB
- Distributed Circuit, S21 matched across band to within 0.48 dB

DESIGN RESULTS: (Final, after fine-tuning)

- Lumped Circuit, S21 matched across frequency band to within 0.06 dB
- Distributed Circuit, S21 matched across band to within 0.07 dB

The next few pages contain a condensed version of DESIGN's printout, the circuit schematics, and a frequency response plot.

DESIGN Output For Matching Network Design Example

```
                MATCHING NETWORK DESIGN PROGRAM

(C) Copyright 1984 Stephen E. Sussman-Fort
All Rights Reserved

Degree of network to be designed:  5
Source resistance (ohms): 5.00E+001

Load Frequencies (Hz)          Magnitude   Angle      Desired |S21| (mag)
 6.000E+009                    7.80E-001   -89.0            0.578
 7.000E+009                    7.50E-001  -103.0            0.659
 8.000E+009                    7.30E-001  -117.0            0.746
 9.000E+009                    7.00E-001  -131.0            0.865
 1.000E+010                    6.70E-001  -144.0            1.000

MATCHING NETWORK DESIGN BEGINS:   The Resistance Excursion Optimization

        ... hold down any key to interrupt optimization ...

Iteration    Function Evaluations    RMS % Error of |S21|**2 Across Passband
   0              1                          62.589
   1              5                          10.263
   2              3                           3.806
Error function has changed by less than 0.50 percent.
Do you wish to continue optimization?  (Y/N): y

Optimization continues ...

   3              2                           3.806
   4              1                           3.604
   5              2                           3.458
   6              2                           3.325
   7              1                           3.176
   8              2                           3.163
Error function has changed by less than 0.35 percent.
Do you wish to continue optimization?  (Y/N): n

RESULTS: MATCHING NETWORK ELEMENT VALUES FROM THE   50 OHM SOURCE
                TO THE COMPLEX-LOAD.

  The Lumped Element Design          The Distributed Element Design

Series Inductor: 2.299E-010 H    TRL: 120.0 ohms,   5.53 deg at 8.000E+009 Hz
Shunt Capacitor: 3.726E-013 F    OST:  25.0 ohms,  25.09 deg at 8.000E+009 Hz
Series Inductor: 8.046E-010 H    TRL: 120.0 ohms,  19.70 deg at 8.000E+009 Hz
Shunt Capacitor: 7.328E-013 F    OST:  25.0 ohms,  42.64 deg at 8.000E+009 Hz
Series Inductor: 5.514E-010 H    TRL: 120.0 ohms,  13.35 deg at 8.000E+009 Hz

   A circuit analysis follows ...

Freq. (Hz)    S21 in dB:  Desired    Lumped Design    Distributed Design
----                      -------    -------------    ------------------
6.000E+009                -4.76        -5.16             -4.94
7.000E+009                -3.62        -3.68             -3.46
8.000E+009                -2.55        -2.26             -2.07
9.000E+009                -1.26        -1.00             -0.86
1.000E+010                 0.00        -0.29             -0.07
```

a directional coupler to send the local oscillator power to the mixer diode. Coupling must be loose so that LO power is still wasted.

A balanced mixer (Figure 10) provides a better solution. The hybrid circuit splits the LO power to the two diodes with little coupling to the antenna. A low pass filter is needed to prevent loss of power to the intermediate frequency amplifier. Additional advantages are reduction of LO noise and harmonic mixing. LO noise is rejected because two signals originating in the same port produce IF outputs that cancel. This is a property of the hybrid circuit. Similarly, even order harmonics of either the LO or the signal produce cancelling outputs.

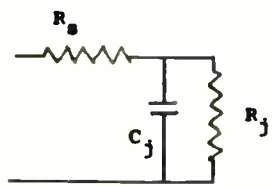
In the double balanced mixer (Figure 11) even order harmonics of both the LO and the signal frequency are rejected. This mixer does not require a low pass filter to isolate the IF circuit. The three ports are isolated from each other by the symmetry of the circuit. These mixers usually cover a broader band than the others. Ratios as high as 1000:1 are available. Microwave equivalents of these mixer circuits are available. Bandwidth ratios as high as 40:1 are available at microwave frequencies.

Intermodulation distortion is reduced when local oscillator power is increased. Several design techniques are used to allow higher drive.

A higher barrier diode may be used to retain linear response at higher drive levels. More than one diode may be used in each arm of the ring in a double balanced mixer. This permits higher drive level without overheating the diodes. Two rings may also be used to increase the local oscillator level. This technique is also used for image tuning described earlier.

Summary:

Schottky diode mixing efficiency is related to both diode parameters and circuit parameters. Diode parameters studied include capacitance, resistance, and barrier voltage. Circuit parameters include DC bias and load resistance. Harmonic response and third order two tone intermodulation were also studied.



EQUIVALENT CIRCUIT
FIGURE 1

Design Output For Matching Network Design Example (cont'd)

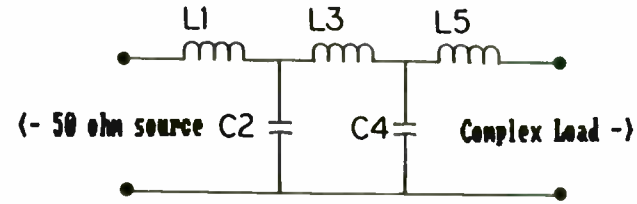
```
Optimize the (L)umped or (D)istributed design or (Q)uit - (L/D/Q): l
Optimization proceeds - hold down any key to stop ...

        Function Evaluation No.:   82

 Maximum Response Error in dB (=  0.06

Design refinement completed - hit (cr) to continue ...
```

```
RESULTS: MATCHING NETWORK ELEMENT VALUES FROM THE   50 OHM SOURCE
                TO THE COMPLEX-LOAD.

  The Lumped Element Design

Series Inductor: 2.129E-010 H       A circuit analysis follows ...
Shunt Capacitor: 3.757E-013 F
Series Inductor: 1.081E-009 H    Freq. (Hz)    S21 in dB:  Desired    Lumped Design
Shunt Capacitor: 7.858E-013 F    ----                      -------    -------------
Series Inductor: 6.554E-010 H    6.000E+009                 -4.76      -4.77
                                 7.000E+009                 -3.62      -3.61
                                 8.000E+009                 -2.55      -2.56
                                 9.000E+009                 -1.26      -1.20
                                 1.000E+010                  0.00      -0.06
```

```
Optimize the (D)istributed design or (Q)uit - (D/Q): d
Optimization proceeds - hold down any key to stop ...

        Function Evaluation No.:   94

 Maximum Response Error in dB (=  0.07

Design refinement completed - hit (cr) to continue ...
```

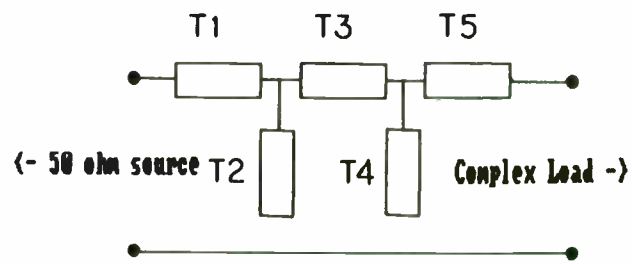
```
RESULTS: MATCHING NETWORK ELEMENT VALUES FROM THE   50 OHM SOURCE
                TO THE COMPLEX-LOAD.

                          The Distributed Element Design

                TRL: 120.0 ohms,   5.22 deg at 8.000E+009 Hz
                OST:  25.0 ohms,  23.76 deg at 8.000E+009 Hz
                TRL: 120.0 ohms,  22.98 deg at 8.000E+009 Hz
                DST:  25.0 ohms,  43.20 deg at 8.000E+009 Hz
                TRL: 120.0 ohms,  13.84 deg at 8.000E+009 Hz

   A circuit analysis follows ...

Freq. (Hz)    S21 in dB:  Desired    Distributed Design
----                      -------    ------------------
6.000E+009                 -4.76      -4.83
7.000E+009                 -3.62      -3.61
8.000E+009                 -2.55      -2.49
9.000E+009                 -1.26      -1.20
1.000E+010                  0.00      -0.07
```

Lumped Matching Network from DESIGN



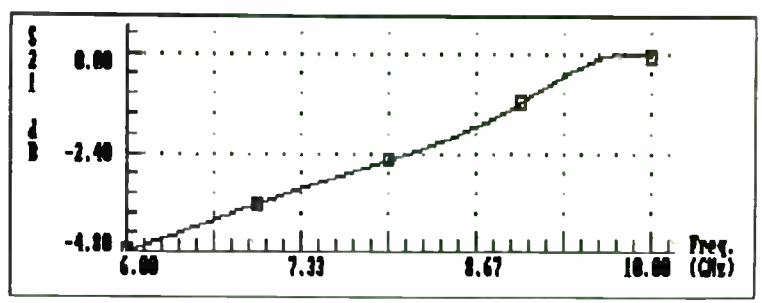
L1: 2.129e-10 H
C2: 3.757e-13 F
L3: 1.081e-09 H
C4: 7.858e-13 F
L5: 6.554e-10 H

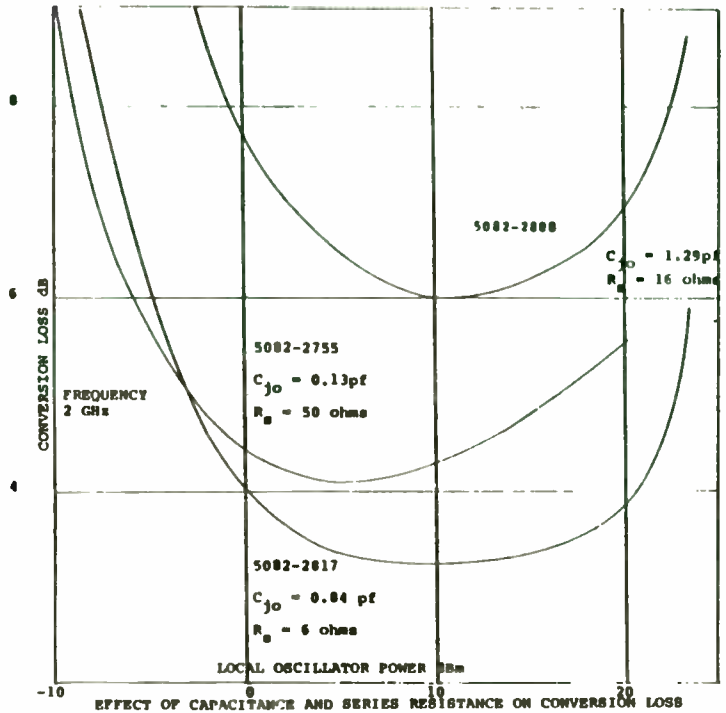
Distributed Matching Network from DESIGN



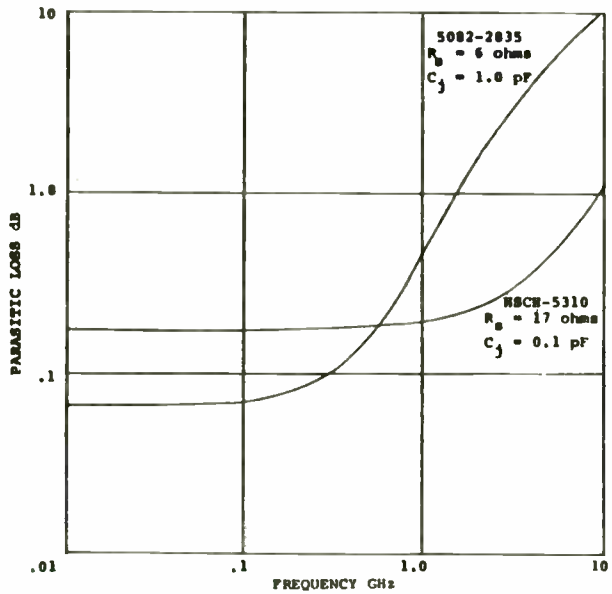
T1: 120 ohms, 5.22 deg @ 8 GHz
T2 25 ohms, 23.76 deg @ 8 GHz
T3: 120 ohms, 22.98 deg @ 8 GHz
T4: 25 ohms, 43.20 deg @ 8 GHz
T5: 120 ohms, 13.84 deg @ 8 GHz

Lumped and Distributed Frequency Response is Coincident with Desired S21 Shape

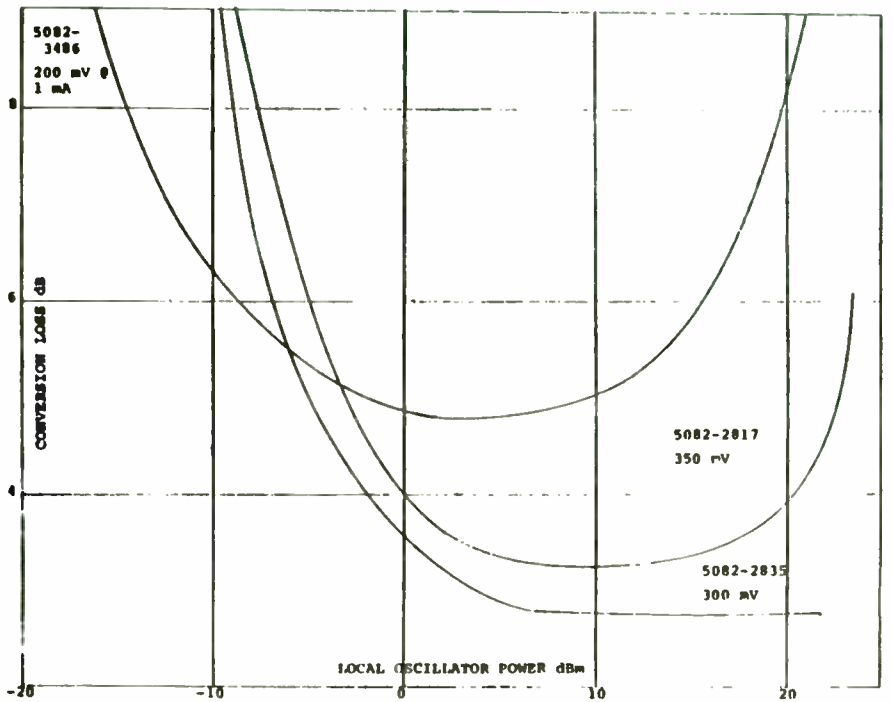




EFFECT OF CAPACITANCE AND SERIES RESISTANCE ON CONVERSION LOSS
FIGURE 2



PARASITIC LOSS
FIGURE 3



EFFECT OF BARRIER
ON CONVERSION LOSS
FIGURE 4

VI. Conclusion

The evolution of two programs for RF and microwave circuit analysis, optimization, and synthesis has been presented. We expect to continue to improve CIAO and DESIGN to include additional features and speed enhancements.

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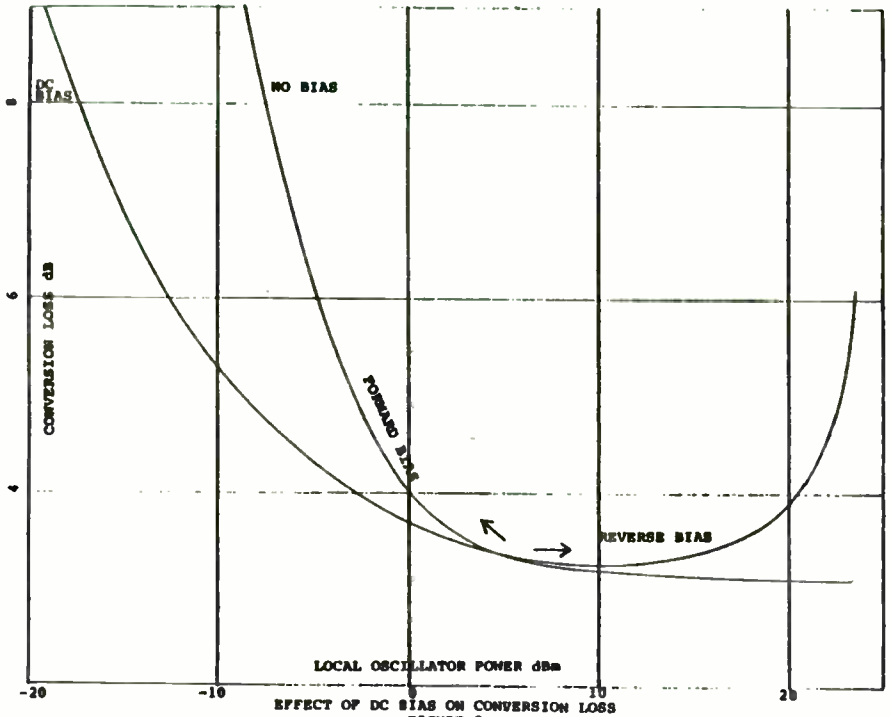
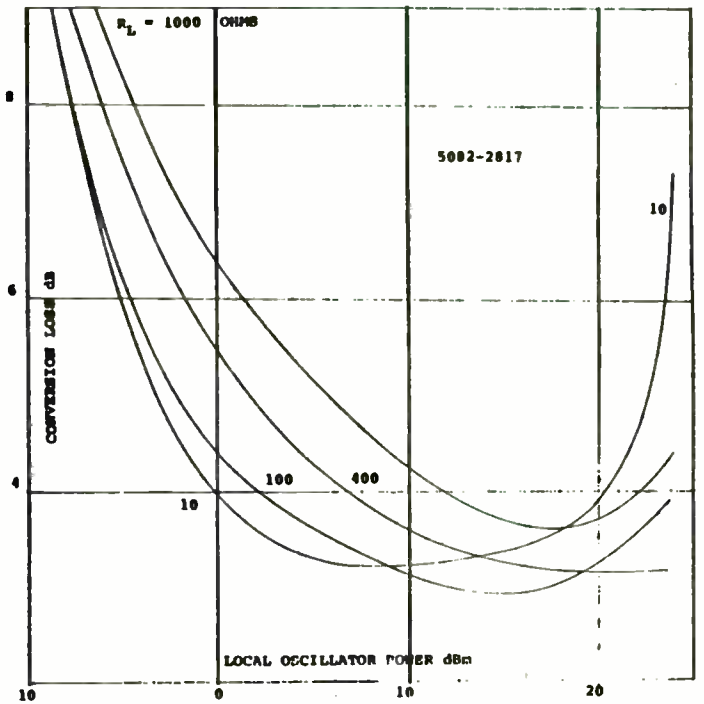


EFFECT OF DC BIAS ON CONVERSION LOSS
FIGURE 5



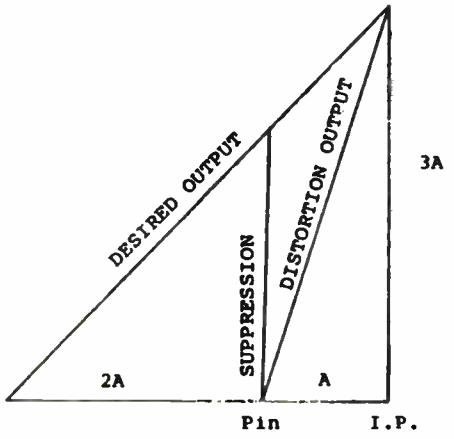
EFFECT OF LOAD RESISTANCE ON CONVERSION LOSS
FIGURE 6

SIGNAL				
4	43	42	X	X
3	21	56	X	X
2	16	45	38	39
1	0	5	13	19
	1	2	3	4

LOCAL OSCILLATOR

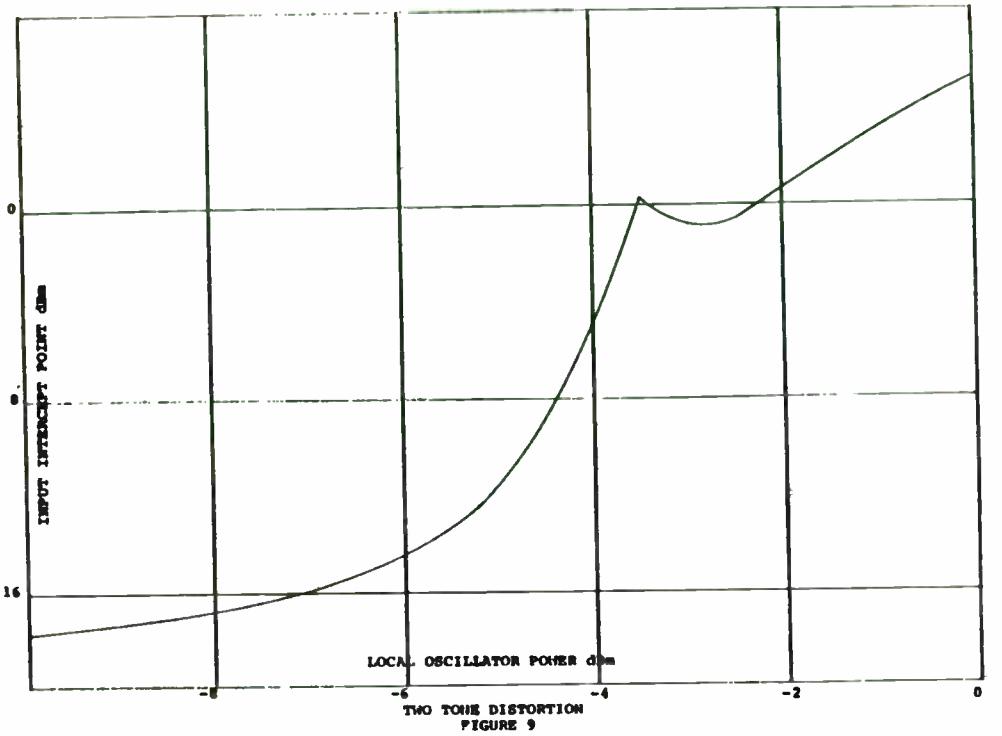
HARMONIC DISTORTION

FIGURE 7



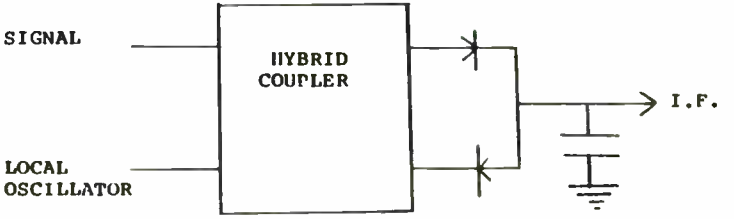
INTERCEPT POINT

FIGURE 8



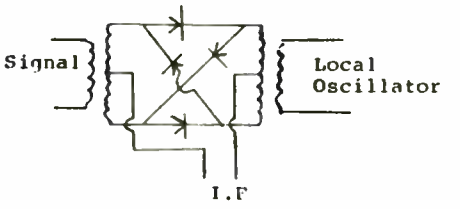
TWO TONE DISTORTION

FIGURE 9



BALANCED MIXER

FIGURE 10



DOUBLE BALANCED MIXER

FIGURE 11

"THE POOR MAN'S ENGINEERING WORK STATION"
or
"CHEAP CAD"

Richard B. Kolbly, PE

RF TECHNOLOGY EXPO 86

January 30 - February 1, 1986
Anaheim, California

THE POOR MAN'S ENGINEERING WORK STATION

by
Richard B. Kolbly
Staff Engineer, Lockheed-California Company
Post Office Box 551
Burbank, California 91520

INTRODUCTION

The current literature is full of discussion of the new "Engineering Work Station" or facilities for Computer-Aided Design (CAD). The working RF design engineer reads of these devices with great anticipation, but soon realizes that these are beyond the normal means of a limited personal or engineering budget. Terms like "silicon compiler" and "gate array design" and "standard cells" are resplendent in the literature. Most working engineers probably will not design integrated circuits or semicustom integrated circuits. The purpose of this paper is to show that the working-level RF design engineer, on a limited budget, can provide an effective facility to simplify his engineering duties.

As a practical matter, few companies are going to allocate tens of thousands of dollars to individual engineers unless an immediate increase in productivity can be shown. It has been my experience that if a computer is not immediately available it loses a great deal of its functionality. If we have to sign up or go across the hall (or across the plant!) to use a computer, we are likely not to bother, and either rely on our experience or just "SWAG" it. Since most companies are unwilling or unable to supply a personal computer to each working engineer who desires one, it is up to each of us to provide our own computational resources, just as we did with slide rules and calculators. This paper will show how to use the "low end" home and personal

The PIN Diode - Uses and Limitations

by
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ABSTRACT

The PIN diode is a useful element in the design of attenuators, switches, and modulators. Under ideal conditions the diode acts as a current controlled resistor. However, there are limitations on performance related to frequency and power.

This paper covers some of the low frequency and high frequency limitations of PIN diode applications and factors determining these limits. Other topics are diode parameters that control resistance and power limitations on attenuator performance.

INTRODUCTION

The PIN diode is a three layer device (figure 1) - an intrinsic high resistance I layer in the center with conducting P and N layers on either side. The conducting layers are formed by adding impurities to produce an excess of positive charges on one side and an excess of negative charges on the other. Diode resistance can be controlled by DC bias voltage. Both positive and negative charges injected into the I layer lower its resistance. Diode resistance is approximately proportional to the inverse of the current.

Ideally PIN diode resistance is controlled by the DC current and independent of the RF power level. However, at high power levels the charge in the I layer may vary at the carrier frequency. In attenuator applications this variation in diode resistance is responsible for distortion. The effect is most severe in absorptive attenuators at low frequencies, with some power also absorbed by diodes in reflective attenuators. Since the amount absorbed depends on the attenuation level, distortion in both types is a function of attenuation.

Most switches are reflective; power is either reflected or passed. Little power is absorbed by the diode so distortion in switches is not a problem. PIN diodes can have a wide range of switching times - from a few nanoseconds to close to a microsecond. The time depends on the combination of forward current for one state and reverse voltage for the other. Switching time is faster in the transition from reverse to forward bias.

Reverse recovery time is related to switching time. Forward current injects charge into the diode, then a reverse pulse removes the charge. Time for recovery to a low value of current is defined as reverse recovery time, and depends on the values of forward current and reverse voltage used in the measurement.

In addition to switches and attenuators, PIN diodes can be used as absorptive modulators. The diode resistance is varied at the modulating

computers to accomplish most of the computational tasks that are required. By using our experience and intelligence in an interactive manner, we can reduce significantly our design "work load" and produce better products in less time.

SOME DEFINITIONS:

Engineering workstation: A collection of equipment that allows the engineer to design and test circuits. For the purpose of this paper, the engineering workstation is a computer-equipped location where a design engineer will spend a significant portion of his work day.

Personal computer: A computer that is immediately available to an individual, of fairly low cost and relatively low processing power. This paper shall be limited to those computers that fall within the normal range of discretionary income for individuals, in general less that two thousand dollars.

Working engineer: The engineer whose primary task is to produce designs. This is the individual who does not have significant personnel or programmatic management duties.

HARDWARE:

For purposes of comparision, lets see what hardware might be availble to accomplish our needs. Just as most of us have some form of personal transportation, we shall have to have some sort of personal "computing engine".

Similar to the small motorcycles, there are the "home computers", such as the Commodore 64's and the Atari 800XL. With a little judicious shopping, these can be found for less that a hundred dollars. Although these are definitely in the class of "motorcycle" computers, they still have 64 kilobytes of memory and a built-in BASIC interpter. A low-cost computer is very capable of doing sophisticated engineering analysis - including using the Method of Moments to calculate wire antenna input impedance [1]. All of the examples in this paper can be modified to operate on these little "home computers", such as the Atari with a minimum of effort.

A more typical "personal engineering computer" (PEC) could be desicribed as having 64K or more of memory, dual disk drives and operating under either the 8-bit CP/M operating system or the 16-bit MS-DOS operating system. A computer such as this will represent an investment of something between $600 and $2000 dollars, depending on how hard one is willing to shop. Of course, it is possible to spend more, but the purpose of this paper is to show how computers that can be purchased by an individual engineer or a tight departmental budget can do significant work.

SYSTEM SOFTWARE:

To operate any computer, you will need a certain amount of programs, or software. We have already mentioned the operating system, in most cases either CP/M or MS-DOS (or one of their close relatives). Between these two operating systems most of the personal computers are covered. This operating system software is generally provided with the computer, and is used to provide basic file handling and program loading.

In addition to the operating system or file handler, you need some sort of 'translator'. Although for many years FORTRAN was widely used, it is not as readily available for personal

frequency while passing a higher carrier frequency. The ability to modulate diode resistance is limited by the diode carrier lifetime, the time required to remove charges from the I layer. For efficient modulation the lifetime must be short compared to the modulation period, while low distortion requires the lifetime to be long compared to the carrier period. When these two frequencies are not far apart it may not be possible to satisfy both conditions, and a compromise value of lifetime is chosen.

Figure 2 shows the frequency limitations for diodes with lifetimes ranging from 10 nanoseconds to 2 microseconds. The fast switching diodes are best with carrier frequencies above a gigahertz and modulation frequencies below 100 kilohertz. The long lifetime diodes are best with carrier frequency above 10 megahertz and modulation frequency below 1 kilohertz. However, these limits are not rigid and diodes are useful beyond these limits.

In addition to the inverse current relation, I layer resistance varies as the square of the I layer thickness and inversely as the lifetime. However, the lifetime is itself a function of I layer thickness so that a longer lifetime diode has more resistance in spite of this inverse relationship. Figure 4 shows that the 5082-3081 diode with 2 microseconds lifetime has 30 times the resistance of the 5082-3043 diode with 15 ns lifetime. Another example of resistance dependence on lifetime is seen in Figure 5. These diodes are in shunt so higher attenuation means lower resistance. The short lifetime 3141 has lower resistance because it has a thinner I layer.

The relation between resistance and current is not valid at high currents. The resistance levels off at a current which depends on the diode construction. This residual series resistance is usually guaranteed to be below a specified maximum.

Attenuator designers often need more information about the resistance current relationship. The specifications for current controlled resistor diodes such as the HPND-4165 shown in Figure 6 include maximum and minimum resistance values at 10 microamperes and at 1 milliampere. In addition, the slope of the curve, the exponent of current, must be matched to 0.04 for all diodes in a batch. Since the slope, x, can vary from 0.83 to 1.00 while satisying the resistance specs, this delta slope spec tightens the matching considerably.

A low frequency limitation of the PIN diode is the dielectric relaxation frequency. When current is removed from the diode most of the charges return to the p and n layers. However, some charges remain in the underpleted portion of the I layer. At low frequencies this undepleted I layer resistance shorts out the I layer capacitance. A capacitance measurement would be high because only a portion of the I layer, the depleted portion, would be measured. Capacitance measurements at low frequencies (1MHz) require the use of reverse bias to drive out the

computers as BASIC. In most cases, programs written in FORTRAN can be translated to BASIC with a minimum of effort. The only snag in this process (well-known to RF designers) is the lack of COMPLEX data types in BASIC. If BASIC had complex data types, it would be a much more useful language for us. Usually BASIC has been provided with your computer - it might be called MBASIC, GWBASIC, BASICA, APPLESOFT BASIC, etc. but they all tend to be variations of Microsoft's MBASIC V5.2 which has become a de facto standard for small computer BASIC interpeters. By staying with the Microsoft BASIC and its variants, we are assured of:

1 - Ease of program modification and debugging.

2 - A high degree of portability between machines.

3 - A common data file structure that many programs can use.

So far we have discussed the "system software" that comes with each computer. We still cannot do any useful design work until we have applications software - those programs that actually calculate and display the information we use. Where are these programs coming from? As all of you are undoubtedly aware, RF design programs are not as popular as word processors. Yet there are many sources of low cost or free software that are directly applicable or easily modified to our needs.

Low- or no-cost software is available from a variety of sources. Most of the programs I use regularly in my duties as a practicing RF engineer have been published in technical magazines. RF Design Magazine is one of the better sources of programs. Other good sources include EDN, Ham Radio, Microwave Journal, etc. The bibliography has several references. The important thing to remember is (to quote Tom Lehr) - "let nothing escape your eyes..." Read or scan as many of the publications as possible and start a clipping file.

Another good source of programs is in manufacturer's application notes. These notes are generally tailored to a specific machine, but I have found them to be easily adopted to other computers. As an example, the now obsolete Hewlett-Packard 9100-series of desktop calculators had excellent discussions of programs that could be used for filter design, transmission line calculations, etc and were easily adapted to BASIC. These programs (and calculators!) often turn up at flea markets, swap meets and house organ classified advertising.

The US Government and universities have a number of catalogs available that describe programs that have been written and are available for a small fee or free. CAED, an excellent microstrip design package (written in FORTRAN) is availble from the US Government [2]. Again, most of these programs are tailored to a specific machine or application, but many of them have wide application. A classic example is the circuit analysis program, SPICE, written and distributed by the University of California [3]. It take a little snooping to find these sources, but other engineers and libraries can be a big help.

A few companies provide low-cost (defined as under $100) software for engineers. Others, with their full-page advertisements, make us envious, but in general, they tend to be out of range to our budgets. All of us would like to have a program like SPICE2 running on our computers, but cannot justify

charges in the undepleted I layer in order to measure the capacitance of the entire I layer. At higher frequencies the reactance of the undepleted I layer is small and the resistance of the undeplete charges is not small enough to cause this capacitance error, so no reverse bias is needed.

The dielectric relaxation frequency is the frequency where the resistance of the undepleted charges equals the reactance of the undepleted I layer. This frequency is about 80 MHz for general purpose diodes, about 16 GHz for the fast switching diodes. When operating below the dielectric relaxation frequency it is necessary to use reverse bias to reach the specified capacitance. Since reverse bias is normally used in switching applications to speed up the switching, the concept is not important for fast switching diodes.

We have seen two possible problems at low frequency. The resistance can vary at the carrier frequency and the capacitance can vary with reverse voltage. There is also a high frequency limitation. At zero bias we expect the diode to approximate an open circuit. This is true at low frequencies when the capacitive reactance is high. At higher frequencies the reactance decreases and the insertion loss of a shunt diode increases, related to the product of frequency and capacitance. Figure 8 shows how insertion loss varies. When this product is 3.2 for example, the loss is 1 dB.

Figure 9 indicates a technique for extending this frequency limitation. The diode capacitance may be included in a low pass filter with the lead inductances on either side of the diode. Package outline 60 and 61 diodes are made this way. The ribbons to the diode chip are properly shaped to provide the needed inductance. When chips are placed in other packages the limitations due to package parasitics appear at frequencies well below what is shown in Figure 8. Before the insertion loss increases because of low diode reactance, the package inductance resonates with the diode capacitance. Figure 11 shows this resonance for a 0.12 pF diode in packages 15 and 31 at 9.2 GHz and 14.5 GHz. Insertion loss due to diode capacitance alone at these frequencies is about 0.1 dB.

Figure 12 shows the problem at forward bias. The package parasitics resonate with each other changing the low resistance Rs to an open circuit. Similar problems limit the performance of series diodes to the VHF region. Figure 13 shows that isolation drops below 20 dB at a few hundred MHz. Chip isolation was calculated with 0.5 nH assumed for the lead inductance. The graph demonstrates that microwave applications for series diodes require the use of beam leads.

Isolation in a shunt switch is limited by the diode series resistance. Using two diodes together cuts the resistance in half and improves isolation 6 dB. Figure 14 shows the results of using two diodes spaced by 90 degrees. The dB isolation more than doubles, and the bandwidth is quite wide, exceeding 50 dB isolation for about a 10:1

the cost of many hundreds or thousands of dollars. A more acceptable substitute are "canned" programs such as ACNAP and DCNAP [4,5] from BV Engineering. These companies provide programs at reasonable cost for our requirements. One company, DYNACOMP [6], provides programs in BASIC source form, so they can be modified for a specific application.

The microcomputer publishing industry has been publishing hundreds of books on using your personal computer for everything from cat breeding to sports handicapping. There are several volumes available of programs for engineering computing, but in general, I have found these not to be of much use. A few exceptions are worth noting. F.R. Ruckdeschel's BASIC Scientific Subroutines (Volumes I & II) [7] should be in every engineer's library. These books are a collection of well-documented programs for many of the mathematical operations that are required for serious engineering work. These programs and subroutines are presented with unique line numbers so they can be used directly - a helpful feature. These subroutines can be purchased already on disk at a nominal cost [8]. Another very useful publication is Antenna Design using Personal Computers by David S. Pozar [9]. This little xpublication is a collection of programs for path analysis, transmission line and antenna design, with a good explanation of the theory involved and a comparison of results with calculated values. Also, these programs are availble on disk [10]. A last example of an excellent publication for the engineer engaged in computer-aided design is Circuit Design using Personal Computers by T. R. Cuthbert [11]. This volume has numerous programs for design (as opposed to analysis) for the small computer, and includes an excellent discussion of optimization, which is often neglected in CAD articles and publications.

A final source of suitable applications software for our "poor man's work station" is ourselves. Although it takes a bit of effort, writing a program to solve a particular design problem can be a fun. Possibly a fellow engineer has a similar requirement to yours and already has a suitable program or one that can be modified. An example of "home brew" engineering programs are included in Appendix A of this paper. Both were written by members of the San Bernardino Microwave Society to solve a specific application, and have been widely distributed and modified by others. Most engineers that write these programs are happy to share them, so always ask, and always give credit where credit is due. In general, these are not the slick finished products that would be available from publishers, but are useful.

PRACTICAL CONSIDERATIONS:

Now that we have discussed the sources of programs that are availbe to the RF design engineer, let's discuss some of the problems we can encounter.

First of all, just because all BASIC programs are similar, they are not identical! In general, when getting a program from another machine, it is necessary to make some minor conversions. Such things as file opening and closing, data formats, and minor syntax variations can drive you up the wall. Multiple statement delimiters, "extra" functions, etc., all have to be resolved and

frequency range. It might be expected that this two-diode switch would double the power handling ability, but there is no improvement. The second diode absorbs very little power and does not contribute to the power specification (Figure 15).

With 1 ohm resistance a shunt diode absorbs less than 10% of the incident power. In this application the incident power can be 10 times the power rating of the diode. In attenuator applications the multiplier is only two, corresponding to 6 dB of attenuation. Figure 16 shows this ratio as a function of attenuation. Switches can handle many times the diode power rating, since the loss switches from low insertion loss to high isolation. However, this assumes that switching time is fast compared to diode thermal time constant.

Both shunt and series diodes attenuate by reflecting most of the incident power. In many applications this reflected power disturbs the operation of another element of the system. Figure 17 shows a number of attenuator designs that maintain a low value of SWR at all attenuation levels. The π and T attenuators are symmetrical with the outer diodes set at the same resistance, but the inner diode set at a different value. Bias circuits may be built with "one knob" tuning providing the proper bias current to all three diodes.(1)

The ideal behavior of attenuation controlled by current, independent of RF power, is not valid at high power levels, due to rectification of the RF signal. Figure 18 shows how low level attenuation is increased at 1.6 watts, with the effect most severe at 3 dB attenuation. Rectification is easier with short lifetime diodes so the 5082-3141 curve is higher. Rectification is also easier at lower frequencies so we would see VHF curves above these. Bias resistance was zero for this data.

Since this increase in attenuation is due to rectified current we expect a reduced effect when bias resistance is increased. This is shown in Figure 19 where the effect is not seen until the power reaches a half watt with bias resistance increased to 100 kilohms. Above that level the opposite effect is seen. Attenuation decreases at higher power indicating an increase of diode resistance. This increase of resistance is the result of diode heating. In this example rectified current is small so the diode heating effect is dominant.

(1) Hewlett-Packard Application Note 936, High Performance PIN Attenuator For Low Cost AGC Application.

corrected. If you are getting a disk-based program from a different (foreign) machine, try to get the program in ASCII format. As a practical matter, I save all of my programs in ASCII instead of the more compact binary format, just to simplify the conversion between different machines. A side benefit of this method of storage allows you to edit and print the source listings with an editor or word processor.

If you are writing programs, try to include provision for storing and loading infomation from disk - this will save you the trouble of typing a circuit over and over. A little effort at this stage can make a program much more professional and easier to use. Data files can be designed that can be used by many programs. I use the format of printing to file the independent variable, followed by dependent variables, e.g. frequency, real part of impedance, imaginary part of impedance in actual values, such as Hz, ohms, etc. Try to avoid the use of specific multipliers, such as GHz; it is then difficult to use your program in a wide variety of situations. Make an effort to maintain consistency whenever possible. When dealing with arrays of data, such as network analysis programs, data files should have a header that specifies the dimensions of the array. It is very easy to forget these parameters when you are working with many different projects.

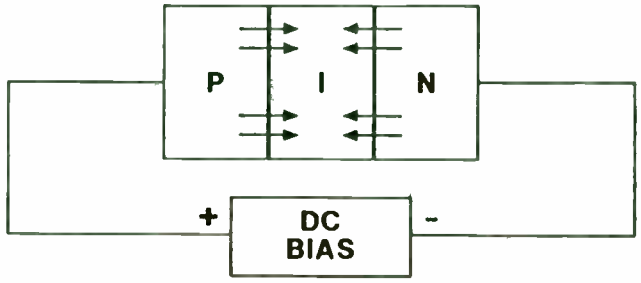
SOME EXAMPLES

Network Analysis: One of the recurring tasks for the RF design engineer is predicting the performance of a circuit and modifying it until it meets requirements. The normal process is to rely on our experience, etc. to get an initial design, breadboard, measure performance, and "tweak and trim" until the desired performance is achieved. Computer aided design is a much more difficult task than computer-aided analysis. In design, we input the desired performance and the output is a circuit. In analysis, the circuit is input and the output is performance. Most small computer programs use an input circuit and calculate performance. Computer -aided design programs are available [12] but I have found that convergence on an acceptable design by interaction is a faster and more comfortable approach.

As an example, the process for design and evaluation of a simple diplexer will be demonstrated. This diplexer is to split the FM broadcast band (88-108 MHz) and the 2-meter amateur radio band (144-148 MHz) from a common source. Since this is intended for very low-cost applications (mobile reception) we decide to use a simple set of Butterworth filter circuits (Figure 1). After coming up with this "quick and dirty" circuit, we load NET85.ASC (Appendix B) and analyze the circuit over the bands of interest. The results of this anaylsis are shown in Figure 2. Inspection of this data indicates that fabrication could be simplified by using standard circuit elements shown in Figure 3. Continuing to work with NET85, we add these changes and obtain the performance shown in Figure 4. Since our only intent is to build one of these for the car belonging to the president's son, we conclude this is an adequate design.

The NET85 program is derived from a program that was originally described in EDN magazine[13]. It was written in a BASIC-like language and has been translated to GWBASIC (Appendix

THE PIN DIODE



Q ∝ DC BIAS CURRENT

G ∝ Q

$$R = \frac{1}{G}$$

FIGURE 1

I LAYER RESISTANCE

$$R \propto \frac{W^2}{I\tau}$$

W IS I LAYER THICKNESS

BUT LIFETIME IS LONG WHEN I LAYER IS THICK

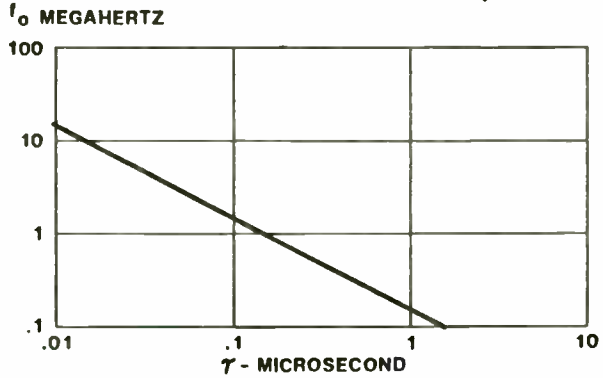
USUALLY W^2 OVERCOMES τ EFFECT

SO FOR SAME CURRENT LONG LIFETIME DIODE HAS HIGHER RESISTANCE THAN SHORT LIFETIME DIODE

FIGURE 3

MODULATOR FREQUENCY LIMITATIONS

FREQUENCY PERFORMANCE LIMITED BY LIFETIME - τ

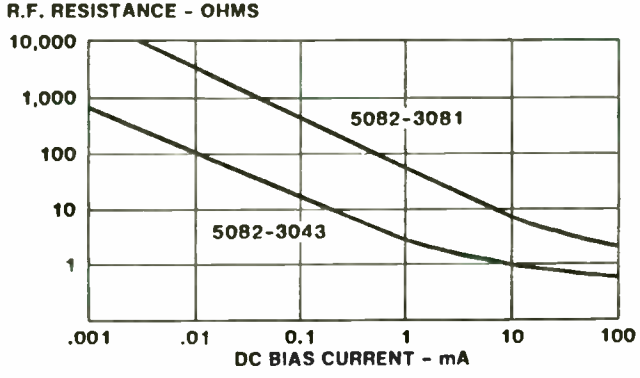


$$f_o = \frac{1}{2\pi\tau}$$

$100\, f_m < f_o < .01 f_c$

FIGURE 2

PIN DIODE RESISTANCE



DIODE 3081 HAS LONG LIFETIME 2μs

DIODE 3043 HAS SHORT LIFETIME 15ns

FIGURE 4

B). The program has been extensively modified to allow for creation and saving of the program data. Examples of input and output data files are also shown in Appendix B. The files are then plotted on a low-cost commercial plotting package [14].

EXAMPLE II: MICROWAVE ANTENNA DESIGN

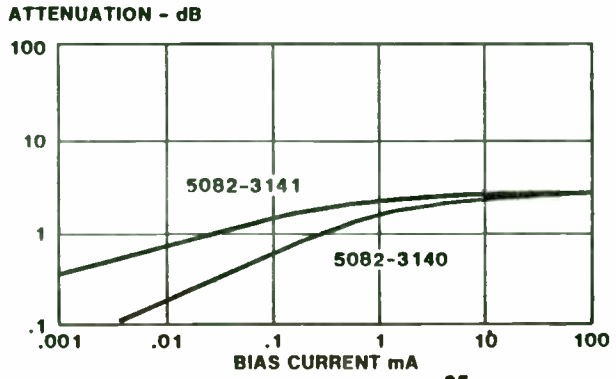
One of the more tedious tasks facing engineers is the occasional design of an antenna. As RF engineers we are often called to come up with at least a rough design for an antenna (How big a dish do we need to receive OSCAR VII?). Appendix B2 has a straight-forward program to design a suitable Cassegrain or prime-focus reflector antenna. Once a suitable design is reached, other BASIC language programs can be used for more detailed analysis [9]. The results can then be presented by using one of many available graphing or plotting programs [14]. When using these relatively simple programs it is important to remember that most of them are based on geometric optic considerations, so do not compensate for edge effects, etc., and will likely provide incorrect answers for small antennas. In general, the higher the antenna gain, the easier it is to predict its performance. There are some programs available [9] that go beyond geometric considerations, but large physical optics or method of moment solutions tend to be beyond personal computers. However, it may be possible to reduce a fairly complex program program to parts that will run on a personal computer. The computation-intensive parts, such as the solution of the complex matricies, could be allowed to run overnight. Most of these programs are availble in FORTRAN [15] and could be loaded and compiled on a MS-DOS based PC, as there are FORTRAN compilers available that can deal with COMPLEX data types. It is possible to translate these programs to BASIC, but it is left as an excercise to the reader to accomplish this.

OTHER APPLICATIONS:

The duties of the RF designer generally include a large portion of 'administrative' duties. These include reports, memoranda, statements of work, project tracking, procurement documents, etc. Most of us find these tasks at best a burden and at worst an imposition. Until management sees fit to provide us with adequate administrative and paraprofessional support, these tasks will remain with us. Our "poor man's engineering work station' can be pressed into service to support these functions. By including some form of text editor or word processing software, reports and memos can be generated quickly and in a more readable form. By relieving the work of preparing documents, I have found that using a small desktop computer increases my engineering productivity significantly. In addition, most engineers would rather design than perform administrative tasks, so the editing function alone makes a personal desktop computer worthwhile.

Procurement actions, schedules, parts and wire lists, etc. can be efficiently maintained using one of the many microcomputer data base managers. As an example, I used a data base on an old microcomputer to maintain a wire list for a large transmitter. By simply inquiring the disk, I could get a list of all the locations a particular signal could be found or all signals on a

MATCHED ATTENUATOR



ATTENUATION = 20 LOG $(1 + \frac{25}{R})$

$R \propto \frac{W^2}{IT}$

FOR SAME CURRENT, HIGHER ATTENUATION FOR THINNER I LAYER NOT FOR LONGER LIFETIME.

FIGURE 5

DIELECTRIC RELAXATION FREQUENCY

AT LOW FREQUENCIES UNDEPLETED I LAYER RESISTANCE SHUNTS CAPACITANCE SO TOTAL CAPACITANCE IS HIGHER

$$R = \frac{1}{2\pi f_{DR} C}$$

FOR EXAMPLE:

$$R = \frac{\rho d}{A} \qquad C = \frac{\varepsilon A}{d}$$

$$f_{DR} = \frac{1}{2\pi\rho\varepsilon}$$

for $\varepsilon = 10^{-12}$

IF $\rho = 2000$, then $f_{DR} = 80$ MHz

or, IF $\rho = 10$ then $f_{DR} = 16$ GHz

FIGURE 7

CURRENT CONTROLLED RESISTORS

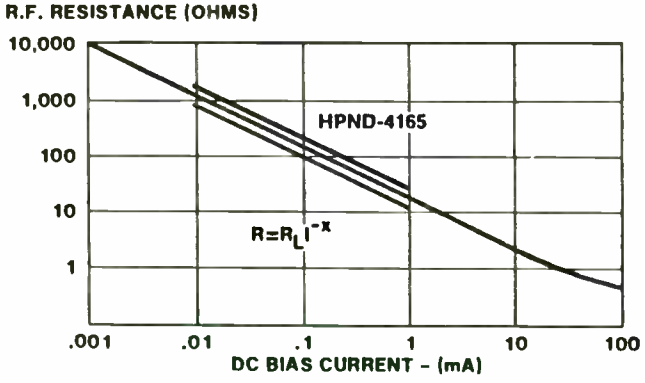
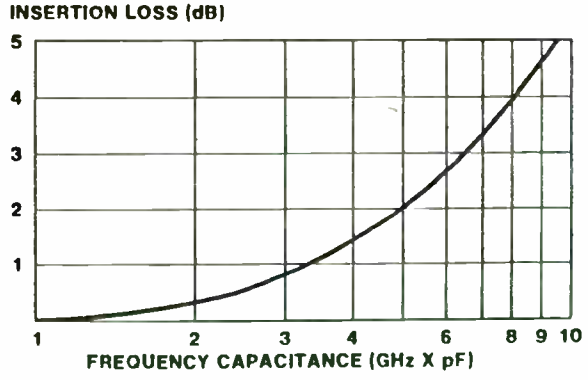


FIGURE 6

SHUNT DIODE INSERTION LOSS

$$10 \text{ LOG } \left[1 + \left(\frac{\pi FC}{20}\right)^2\right]$$



particular connector or terminal block.

These applications are well known, and it is not my intention to go into great detail, but sometimes we overlook the 'support functions' that take up so much time. If we can develop more time for design work, it enables us to be more effective as engineers.

CONCLUSIONS:

This paper has presented one engineer's view of the use of obsolescent technology to make his job easier and more productive. As the cost of computing power continues to decline, we will have the power of supermini computers available to us. In the meantime, the latest technology may not be available. I have tried to show with a few examples how we can use existing low-end hardware combined with relatively simple software to greatly speed up our efforts as design engineers. The key is the immediate availability of a computer. It is better to have an old, slow machine immediately availble to us for a quick evaluation, than a large mainframe that we have to schedule well in advance. The programs and examples I have presented are not necessarily the most efficient or accurate. They are programs that I have used and refined over the years to accomplish specific tasks. There are many things that can be done by the user to make these programs more efficent or easier to use. As an example, an option could easily by added to allow input to NET85.ASC as reactance values, rather than component values. This change would be very helpful, but I never "got around tuit". The bibliography lists several sources of software, but I make no claims for its accuracy or completeness.

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[4] BV Engineering 2200 Business Way, Suite 207 Riverside, CA
[5] 92501 (714) 781-0252

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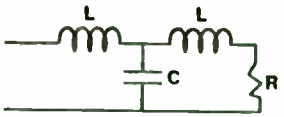
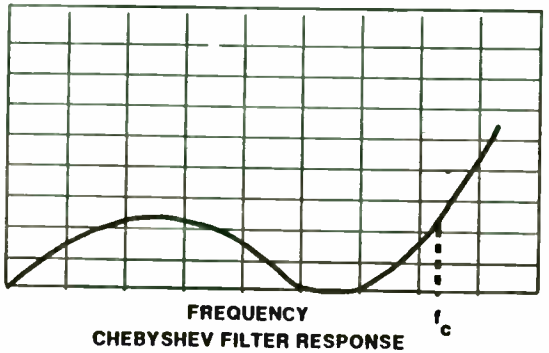
EXTENSION OF HIGH FREQUENCY LIMITATIONS

SOLUTION



LOW PASS FILTER WITH DIODE AS SHUNT CAPACITOR

INSERTION LOSS



CHEBYSHEV FILTER RESPONSE
APPLICATION NOTE 957-2

FIGURE 9

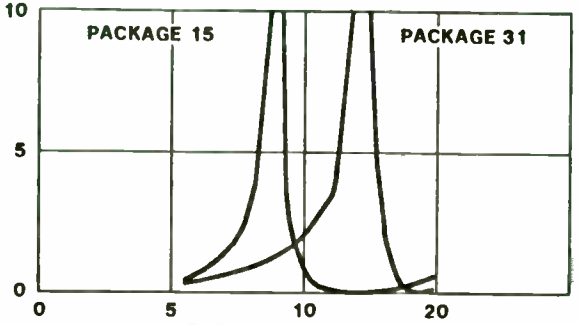
PACKAGE LIMITATIONS

HIGH INSERTION LOSS AT FIRST RESONANCE

$$F_{RES} = \frac{1}{2\pi\sqrt{L_p C_J}}$$

LOW INSERTION LOSS AT SECOND RESONANCE WITH PACKAGE CAPACITANCE

INSERTION LOSS - dB

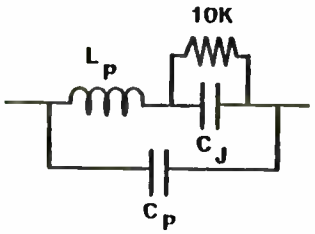


INSERTION LOSS OF PACKAGED SHUNT DIODES
.12 pF JUNCTION CAPACITANCE

FIGURE 11

FIGURE 10

PACKAGE LIMITATIONS



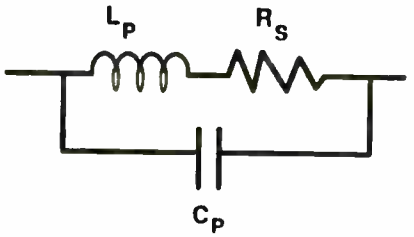
REVERSE OR ZERO BIAS

PKG.	15	31
C_P PF	.13	0.2
L_P nH	2.5	1.0

AT L_P C_J RESONANCE - LOW ISOLATION FOR SERIES DIODE - HIGH INSERTION LOSS FOR SHUNT DIODE; AT SECOND RESONANCE WITH C_P - GOOD PERFORMANCE

FIGURE 12

PACKAGE LIMITATIONS



FORWARD BIAS

AT RESONANCE - HIGH INSERTION LOSS FOR SERIES DIODE - LOW ISOLATION FOR SHUNT DIODE

THIS PROPERTY IS USEFUL IN NARROW BAND WAVEGUIDE SWITCHES

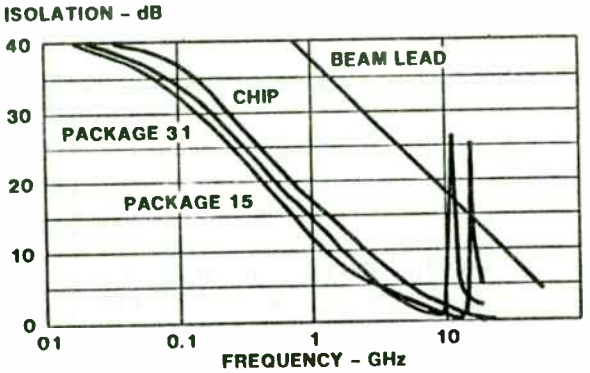
APPENDIX A

USER-WRITTEN BASIC DESIGN PROGRAMS

A.1 DISH.ASC This program was written by Chuck Swedblom of the San Bernardino Microwave Society for design and analysis of Cassegrain-reflector antennas. It is based on ray-trace optics.

```
10 '
20 ' PARABOLIC ANTENNA DESIGN PROGRAM
30 '
40 ' Written by C. Swedblom, WA6EXV January 13, 1981 (not Friday)
50 '
60 ' Revised: March 26, 1981
70 '
80 'Modified for Microsoft Basic by R. Kolbly, K6HIJ April 3, 1981
90 '  (Friday after a Society Meeting!)
100 '
110 CLS$=CHR$(27)+"E"
120 PI=3.1415928#
130 DIM X(100)
140  M$="###.##"
150  D$="###"
160 PRINT CLS$
170 PRINT "Select area of interest"
180 PRINT
190 PRINT "     1.  Calculate f/D and Gain of a Parabolic Dish."
200 PRINT "     2.  Design Sub Reflector for Cassegrain feed."
210 PRINT "     3.  Return to Basic"
220 INPUT "Your Choice";ME
230 IF ME < 1 THEN 260
240 IF ME > 3 THEN 260
250 ON ME GOTO 290,700,1390
260 PRINT CLS$
270 PRINT "Values between 1 and 3 only!"
280 GOTO 170
290 ' Calculate f/D
300 '
310 PRINT CLS$
320 INPUT "Diameter of the Dish in Inches";DIA
330 PRINT
340 INPUT "Depth of Dish, same units as Diameter";CR
350 PRINT
360 INPUT "Frequency of Interest, in MHz";MHZ
370 PRINT
380 INPUT "Efficency of the Dish in %";EFF
390  FDR=DIA/(16*CR)
400  LAMDA=30000/(2.54*MHZ)
410  GAIN=(PI*DIA/LAMDA)^2*EFF/100
420  GAIN=10/LOG(10)*LOG(GAIN)
430 '
440 ' Print Results
450 '
460 'INPUT "Port #",N (For output of Chuck's Basic)
470 PRINT CLS$
480 PRINT "            PARABOLIC DISH f/D and GAIN"
490 PRINT "            ---------------------------"
500 PRINT:PRINT
510 PRINT "Diameter of the Parabolic Dish.....";
520 PRINT USING M$;DIA;:PRINT " In."
530 PRINT
540 PRINT "The f/D Ratio of the Parabolic Dish...";
550 PRINT USING M$;FDR
560 PRINT
570 PRINT "The Gain of the Parabolic Dish.....";
580 PRINT USING M$;GAIN;:PRINT " dB at ";MHZ;" MHz"
590 PRINT "    with an Efficiency of ...........";
600 PRINT USING D$;EFF;:PRINT " %"
610 '
620 ' Calculate Distance to the focal point
630 '
640  FR=FDR*DIA
650 PRINT
660 PRINT "The distance to the focal point is....";
670 PRINT USING M$;FR;:PRINT " Inches"
680 PRINT:PRINT:PRINT:PRINT:PRINT
690 END
700 '
710 ' Calculate the size and location of a Sub Reflector for a
720 ' Cassegrain fed Parabolic Dish.
730 '
740 PRINT CLS$
750 INPUT "f/D of the Real Dish in Inches";FDR
760 PRINT
770 INPUT "f/D of the Virtual Dish";FDV
780 PRINT
790 INPUT "Diameter of the Real Dish in Inches";DIA
800 PRINT
810 INPUT "Ratio of Sub Ref Dia. to Diameter, not over .3";FSR
820 PRINT
830  FR=FDR*DIA
840  FV=FDV*DIA
850  CR=DIA^2/(16*FR)
860  CV=DIA^2/(16*FV)
870  DSR=DIA*FSR
880  M=DSR*(FR-CR)/DIA
890  L=DSR*(FV-CV)/DIA
900  A=(L+M)/2*(FV-FR)/(FV+FR)
910  E=(L+M)/(2*A)
920  THETA=2*ATN((DIA/2)/(FV-CV))
930  BLOCK=DIA*DIA-DSR*DSR
940  GAINSR=10/LOG(10)*LOG(BLOCK)
950  GAINRE=10/LOG(10)*LOG(DIA*DIA)
960  BLK=GAINRE-GAINSR
970  THETA=THETA*180/PI
980 'output the Data
```

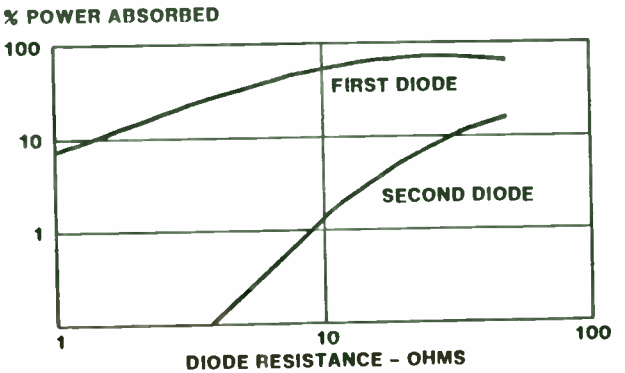
ISOLATION OF SERIES DIODES



0.12 pF JUNCTION CAPACITANCE FOR CHIP AND PACKAGED UNITS
0.02 pF BEAM LEAD DIODE CAPACITANCE
PACKAGE 15 RESONATES FIRST BECAUSE Lp LARGER
PACKAGE 31 WORSE BELOW RESONANCE BECAUSE Cp LARGER

FIGURE 13

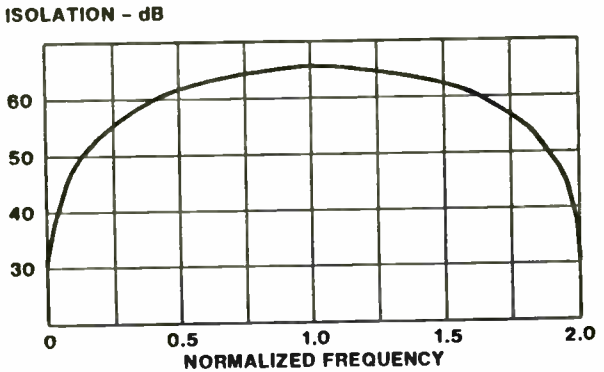
ABSORBED POWER DIVISION IN QUARTER WAVE PAIR



SECOND DIODE DOES NOT IMPROVE ABILITY TO HANDLE HIGH POWER

FIGURE 15

BROAD BAND SWITCH DESIGN



QUARTER WAVE PAIR
ONE OHM DIODES

ISOLATION MORE THAN DOUBLE SINGLE DIODE

FIGURE 14

RATIO OF INCIDENT POWER TO ABSORBED POWER

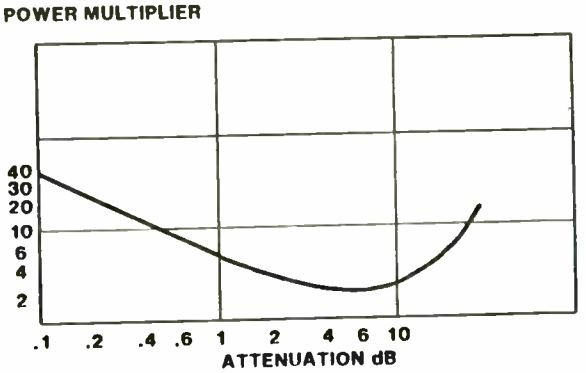


FIGURE 16

```
990 '
1000 '
1010 PRINT CLS$
1020 PRINT  "                PARABOLIC DISH/SUB-REFLECTOR"
1030 PRINT  "                ----------------------------"
1040 PRINT:PRINT
1050 PRINT "Diameter of Dish.............................";
1060 PRINT USING M$;DIA;:PRINT "In."
1070 PRINT "f/D of Real Dish.............................";
1080 PRINT USING M$;FDR
1090 PRINT "f/D of Virtual Dish..........................";
1100 PRINT USING M$;FDV
1110 PRINT "Focal Point of Real Dish.....................";
1120 PRINT USING M$;FR;:PRINT " In."
1130 PRINT "Focal Point of Virtual Dish..................";
1140 PRINT USING M$;FV;:PRINT " In."
1150 PRINT "Diameter of Sub-Reflector....................";
1160 PRINT USING M$;DSR;:PRINT " In."
1170 PRINT "Location of Sub-Reflector....................";
1180 PRINT USING M$;FR-M;:PRINT " Inches from Org."
1190 PRINT "Location of Feed Horn........................";
1200 PRINT USING M$;(FR-M)-L;:PRINT " Inches from Org."
1210 PRINT "Feed Beam Width..............................";
1220 PRINT USING M$;THETA;:PRINT " Deg."
1230 PRINT "Reduction in Gain due to Sub-Reflector.......";
1240 PRINT USING M$;BLK;:PRINT " dB."
1250 PRINT:PRINT:PRINT
1260 '
1270 ' Print X-Y Coordinates of Hyperbolidal Sub-Reflector
1280 '
1290 INPUT "Enter increment for Sub Ref. X-Y Cordinates";INC
1300 PRINT TAB(5);"X-Y Co-ord. for Hyperbolidal Sub-Ref."
1310 PRINT
1320 PRINT TAB(10);"Y-Co-ord.";TAB(28);"X-Co-ord."
1330 PRINT
1340 FOR Y=0 TO DSR/2 STEP INC
1350 X(Y)=SQR(A*A+(Y*Y)/(E*E-1))
1360 Z=X(Y)-X(0)
1370 PRINT TAB(10);:PRINT USING M$;Y;:PRINT TAB(28);
1380 PRINT USING M$;Z
1390 NEXT Y
1400 END
```

A.2 STRIPLIN.ASC This program is for design of microstrip lines

and has been continously refined. Again, it is user-written.

```
10 REM THIS PROGRAM CALCULATES THE WIDTH OF A MICROSTRIP LINE
20 REM FOR A GIVEN IMPEDANCE OF WILL CALCULATE THE IMPEDANCE
30 REM OF A MICROSTRIP LINE OF A GIVEN WIDTH
40 REM
50 REM WRITTEN BY C. SWEDBLOM, WA6EXV 12 JUNE 1979
60 REM MODIFIED BY DICK KOLBLY, K6HIJ 16 SEPT 1979
70 REM DIELECTRIC CONSTANTS ADDED K6HIJ 10 MARCH 1981
80 REM   W=WIDTH OF MICROSTRIP LINE
90 REM   H=THICKNESS OF SUBSTRATE MATERIAL
100 REM   T=THICKNESS OF MICROSTRIP LINE
110 REM  F=FREQUENCY
120 REM  E=DIELECTRIC CONSTANT OF SUBSTRATE MATERIAL
130 REM  E1=DIELECTRIC CONSTANT AT DC
140 REM  E2=DIELECTRIC CONSTANT AT F0
150 REM  Z=CHARACTERISTIC IMPEDANCE OF MICROSTRIP
160 REM  Z1=CHARACTERISTIC IMPEDANCE AT DC
170 REM  Z2=DESIRED IMPEDANCE
180 REM  L=WAVELENGTH
190 REM  D1=IMPEDANCE ERROR FACTOR
200 REM
210 D1=.0001
220 P1=3.14159265#
230 PRINT "1 OZ Cu=.0013 in, 2 Oz Cu=.0027"
240 PRINT "(1) AIR             (e=1.00)"
250 PRINT "(2) G10 FIBERGLASS (e=4.80)"
260 PRINT "(3) TEFLON/GLASS    (e=2.55)"
270 PRINT "(4) REXOLITE        (e=2.54)"
280 PRINT "(5) TEFLON          (e=2.10)"
290 PRINT "(6) FORMICA XX      (e=4.04)"
295 PRINT "(7) DUROID          (e=2.23)"
300 INPUT "(8) OTHER";K:IF K=0 OR K=8 THEN 310 ELSE 320
310 INPUT"TYPE OF MATERIAL AND ER";A$,E
320 IF K=1 THEN A$="AIR":E=1!
330 IF K=2 THEN A$="G10":E=4.8
340 IF K=3 THEN A$="TEFLON/FIBERGLASS":E=2.55
350 IF K=3 THEN A$="REXOLITE":E=2.54
360 IF K=5 THEN A$="TEFLON":E=2.1
370 IF K=6 THEN A$="FORMICA XX":E=4.04
375 IF K=7 THEN A$="DUROID":E=2.23
380 IF K<0 OR K>8 THEN 300
390 INPUT"FREQUENCY (GHZ)";F
400 INPUT"SUBSTRATE THICKNESS";H
410 INPUT "LINE THICKNESS";T
420 PRINT "DO YOU WANT"
430 PRINT
440 PRINT"1.  MICROSTRIP WIDTH"
450 PRINT"2.  IMPEDANCE OF MICROSTRIP LINE?"
460 PRINT
470 INPUT X
480 IF X=2 THEN 680
490 INPUT "DESIRED IMPEDANCE=";Z2
500 W=1
510 GOSUB 740
520 GOSUB 820
530 PRINT Z
540 R=Z/Z2
550 IF ABS((1-R)/(1+R))<=D1 THEN 620
560 REM CALCULATE NEW WIDTH
570 W=W*R*R
580 GOTO 510
590 REM
600 REM ADJUST WIDTH FOR THICKNESS OF LINE
```

ABSORPTIVE ATTENUATORS

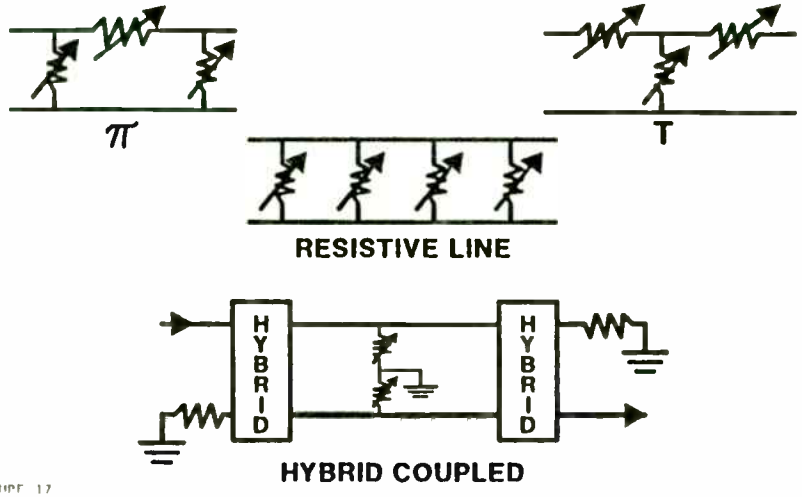
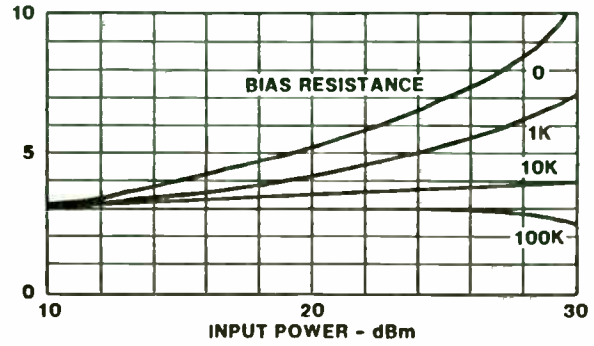


FIGURE 17

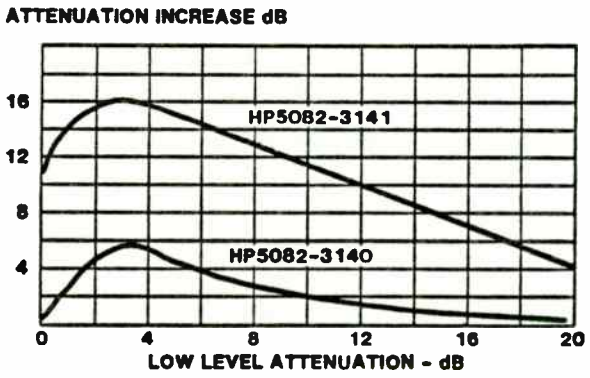
POWER SENSITIVITY IN A 3 dB PIN ATTENUATOR



FREQUENCY 10 GHz
DIODE HP5082-3141
REVERSE EFFECT AT HIGH VALUE OF BIAS RESISTANCE
DUE TO TEMPERATURE EFFECTS.

FIGURE 19

POWER SENSITIVITY AT +32 dBm INPUT



DATA TAKEN AT 2 GHz ZERO OHMS BIAS RESISTANCE
THE INCREASE IS LESS AT HIGHER FREQUENCIES
THE INCREASE IS LESS FOR THE DIODE WITH LONGER LIFETIME (3140)
SEE AN 957-3

FIGURE 18

```
610 REM
620 GOSUB 1010
630 W=W-W1
640 GOTO 1090
650 REM
660 REM CALCULATE IMPEDANCE FROM LINE WIDTH
670 REM
680 INPUT"LINE WIDTH =";W
690 GOSUB 1010
700 W=W+W1
710 GOSUB 740
720 GOSUB 820
730 GOTO 1090
740 REM
750 REM SUBROUTINE TO CALCULATE P
760 REM
770 IF W/H<=1 THEN 800
780 P=2*P1/((W/H)+2.42-(.44*H/W)+EXP(8*LOG(1-(H/W))))
790 RETURN
800 P=LOG((8*H/W)+W/(4*H))
810 RETURN
820 REM
830 REM SUBROUTINE TO CALUCLATE E1,E2 AND Z
840 REM
850 E3=((E-1)/2*(1/SQR(1+(10*H/W))-1))
860 E1=E+E3
870 REM
880 REM CALCULATE EFFECTIVE ER
890 REM
900 REM DISPERSION EQUATION FROM GETSINGER
910 REM
920 Z1=60*P/SQR(E1)
930 G=.6+(.009*Z1)
940 D=Z1/(2.54*4*P1*H)
950 E2=E+(E3/(1+G*EXP(2*LOG(F/D))))
960 REM
970 REM CALCULATE IMPEDANCE,Z
980 REM
990 Z=60*P/SQR(E2)
1000 RETURN
1010 REM
1020 REM SUBROUTINE TO CORRECT LINE WIDTH FOR THICKNESS
1030 REM
1040 IF W/H<.15915 THEN 1070
1050 W1=(T/P1)*(1+LOG(2*H/T))
1060 RETURN
1070 W1=(T/P1)*(1+LOG((4*P1*W)/T))
1080 RETURN
1090 REM
1100 REM PRINT OUT RESULTS
1110 REM
1120 L=(11.811/F)/SQR(E2)
1130 REM
1140 REM THESE ARE RESERVED FOR PRINT FORMATS
1150 REM
1160 PRINT:PRINT:PRINT
1170 PRINT"  TYPE OF MATERIAL-----------------";A$
1180 PRINT"  DIELECTRIC CONSTANT--------------";E
1190 PRINT"  EFFECTIVE DIELECTRIC CONSTANT-----";E2
1200 PRINT"  OPERATING FREQUENCY---------------";F;" GHZ"
1210 PRINT"  IMPEDANCE OF MICROSTRIP-----------";Z;" OHMS"
1220 PRINT"  WIDTH OF MICROSTRIP---------------";W;" INCHES"
1230 PRINT"  THICKNESS OF SUBSTRATE------------";H;" INCHES"
1240 PRINT"  THICKNESS OF MICROSTRIP LINE------";T;" INCHES"
1250 PRINT"  WAVELENGTH-----------------------";L;" INCHES"
1260 PRINT"  QUARTER WAVELENGTH----------------";L/4;" INCHES"
1270 PRINT:PRINT:PRINT
1280 INPUT"ANOTHER RUN";Q$:Q$=LEFT$(Q$,1)
1290 IF Q$="Y" THEN 1300 ELSE END
1300 IF X=1 THEN GOTO 490 ELSE GOTO 680
```

APPENDIX B

NET85. ASC - A useful network analysis program derived from literature, but extensively modified by users for particular needs, including file storage of circuits and results of analysis.

```
10 ' *** NET*85 ***
20 ' SEE EDN FEB 4, 1981 PP 126-133
30 ' TRANSLATED TO MICROSOFT BASIC BY R.B. KOLBLY
35 ' DISK FILES FOR SAVING AND RESTORING NETWORKS ADDED
36 ' DATA FILE OUTPUT CAPABILITY ADDED
40 ' GOLDEN RULE SYSTEMS - FEBRUARY 22,1985
50 P$=
 "FREQ= ##.####^^^^  AMPL= ##.##^^^^  20LOG= ####.#  PHASE= ####.#"
60 K=INT(FRE(A)/4)-23
70 X=INT((SQR(169+24*K)-26)/12)-1
80 PRINT USING "You have a maximum of ## Nodes Available";X
90 INPUT "Number of Nodes Desired (CR=10)";Y
100 IF X>=10 AND Y=0 THEN X=10:GOTO 140
110 IF X<10 AND Y=0 THEN X=Y:GOTO 140
120 IF Y>X THEN PRINT USING "Maximum of ### nodes!";X:GOTO 90
130 IF Y<X THEN X=Y
140 DIM A(X,X),B(X,X),P(X,X),Q(X,X),R(X,X)
150 DIM S(X,X),I(2*X),FL$(4,2)
160 DIM T(2*X),M(2*X),N(2*X),O(2*X),L(2*X),Z(2*X)
170 PRINT USING "You have selected a maximum of ## nodes";X
180 FOR J=1 TO X
190 FOR I=1 TO X
200 P(I,J)=0
210 Q(I,J)=0
220 R(I,J)=0
230 S(I,J)=0
240 NEXT I
250 NEXT J
260 NODES=X:X=1:T(X)=0
270 N=0
280 PRINT "1   RESISTOR"
290 PRINT "2   CAPACITOR"
300 PRINT "3   INDUCTOR"
310 PRINT "4   TRANSMISSION LINE"
320 PRINT "5   SHORTED STUB"
330 PRINT "6   OPEN STUB"
340 PRINT "7   OPERATIONAL AMPLIFIER"
350 PRINT "8   NPN TRANSISTOR"
360 PRINT "9   FIELD-EFFECT TRANSISTOR"
370 PRINT "10  STOP"
380 PRINT "11  ANALYZE NETWORK"
390 PRINT "12  ENABLE/DISABLE PRINTER"
391 PRINT "13  RESTORE NETWORK FROM DISK"
392 PRINT "14  SAVE NETWORK TO DISK"
393 PRINT "15  GENERATE ASCII NETWORK FILE"
400 PRINT "16  LOAD NETWORK VALUES FROM ASCII FILE"
410 PRINT
420 R6=0:INPUT "SELECT FROM LIST (<CR> FOR MENU)";R6
430 IF R6=1 THEN PRINT "(1) RESISTOR":GOTO 730
440 IF R6=2 THEN PRINT "(2) CAPACITOR":GOTO 810
450 IF R6=3 THEN PRINT "(3) INDUCTOR":GOTO 770
460 IF R6=4 THEN PRINT "(4) TRANSMISSION LINE":GOTO 560
470 IF R6=5 THEN PRINT "(5) SHORTED STUB":GOTO 690
480 IF R6=6 THEN PRINT "(6) OPEN STUB":GOTO 710
490 IF R6=7 THEN PRINT "(7) OP AMP":GOTO 990
500 IF R6=8 THEN PRINT "(8) NPN TRANSISTOR":GOTO 880
510 IF R6=9 THEN PRINT "(9) FET TRANSISTOR":GOTO 840
520 IF R6=10 THEN PRINT "(10) PROGRAM FINISH":STOP
530 IF R6=11 THEN PRINT "(11) ANALYSIS":GOTO 1060
540 IF R6=12 THEN INPUT "(12) HARDCOPY OUTPUT (Y/N)";H$
    :H$=LEFT$(H$,1): GOTO 420
541 IF R6=13 THEN PRINT "(13) RESTORE NETWORK TO DISK"
    :GOTO 3000
542 IF R6=14 THEN PRINT "(14) SAVE NETWORK TO DISK":GOTO 3500
543 IF R6=15 THEN PRINT "(15) GENERATE ASCII NETWORK FILE"
    :GOTO 5000
544 IF R6=16 THEN PRINT "(16) LOAD NETWORK FROM ASCII FILE"
    :GOTO 4000
550 GOTO 280
560 T(X)=1:INPUT "SHIELD IN";M(X):REM *** TRANSMISSION LINE ***
570 INPUT "CENTER IN";I(X):INPUT "CENTER OUT";O(X)
580 INPUT "SHIELD OUT";N(X):GOTO 610
590 INPUT "NODE A";M(X)
600 INPUT "NODE B";N(X)
610 INPUT "Z0";Z(X)
620 INPUT "QUARTER-WAVE FREQUENCY (HZ)";L(X)
630 IF I(X)>N THEN N=I(X)
640 IF M(X)>N THEN N=M(X)
650 IF N(X)>N THEN N=N(X)
660 IF O(X)>N THEN N=O(X)
670 X=X+1:T(X)=0
680 GOTO 420
690 T(X)=3: REM *** SHORTED STUB ***
700 GOTO 590
710 T(X)=2: REM *** OPEN STUB ***
720 GOTO 590
730 INPUT "NODE A";I:INPUT "NODE B";J:INPUT "RESISTANCE (OHMS)";V
740 V=1/V
750 GOSUB 1430
760 GOTO 420
770 INPUT "NODE A";I:INPUT "NODE B";J:INPUT "INDUCTANCE (H)";V
780 V=1/V
790 GOSUB 1360
800 GOTO 420
810 INPUT "NODE A";I:INPUT "NODE B";J
    :INPUT "CAPACITANCE (FARADS)";V
820 GOSUB 1480
830 GOTO 420
840 INPUT "GATE";K:INPUT "SOURCE";J:INPUT "DRAIN";I:
```

A COMMUTATION DOUBLE-BALANCED MIXER OF HIGH DYNAMIC RANGE

by

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INTRODUCTION

Dynamic range remains the principle goal of HF mixer design. The intermodulation performance and overload characteristics of a mixer are fundamental qualities used in the evaluation of a good design. Heretofore, most mixers sporting a high dynamic range have been either the passive diode-ring variety, or the active FET mixer.[1][2]

Common to both the diode and FET is their square-law characteristic so important in maintaining low distortion during mixing. However, equally important for high dynamic range is the ability to withstand overload that has been identified as a principle cause of distortion in mixing.[3] Some passive diode-ring mixer designs have resorted to paralleling of diodes to effect greater current handling, yet the penalty for this apparent improvement is the need for a massive increase in local-oscillator power.

This report examines a new FET mixer where commutation achieves high dynamic range without exacting the anticipated penalty of increased local-oscillator drive. Using the Siliconix Si8901, third-order intercept points upwards of +39 dBm (input) have been achieved with only +17 dBm of local-oscillator drive!

CONVERSION EFFICIENCY OF THE COMMUTATION MIXER

Unlike either the conventional diode-ring mixer or the active FET mixer, the commutation mixer relies on the switching action of the quad-FET elements to effect mixing action. Consequently, the commutation mixer is, in effect, no more than a pair of switches reversing the phase of the signal carrier at a rate determined by the local-oscillator frequency. Ideally, we would anticipate little noise contribution and, since the switching mixer, consisting of four "switches," has finite ON resistance, performance is similar to that of a switching attenuator. As a result, the conversion efficiency of the commutation mixer may be expressed as a loss.

This loss results from two related factors. First, is the r_{DS} of the MOSFET relative to the signal and IF impedances; second -- a more common and expected factor -- is the loss attributed to signal conversion to undesired frequencies. There are, however, ways to reduce the effects of undesired frequency generation by the use of filters.

The effect of r_{DS} of the MOSFETs may be determined from the analysis of the equivalent circuit shown in Figure 1, assuming that our local oscillator waveform is an idealized square-wave. It is not, but if we assume that it is, our analysis is greatly simplified; and for a commutation mixer, a high local-oscillator voltage begins to approach the ideal waveform of a square-wave.

Figure 1, showing switches rather than MOSFETs, also identifies the ON state resistance, r_{DS}, as well as the OFF-state resistance, r_{OFF}. The latter can be disregarded in this analysis as it is generally extremely high. On the other hand, the ON-state resistance, r_{DS}, together with the source and

```
    INPUT "GAIN(MHO)";V
850 L=J
860 GOSUB 1530
870 GOTO 420
880 INPUT "BASE";K:INPUT "EMITTER";J:INPUT "COLLECTOR";I:
    INPUT "BETA";R5
890 INPUT "Rbe (OHMS)";V
900 V=1/V
910 L=I
920 I=K
930 GOSUB 1430
940 I=L
950 L=J
960 V=V*R5
970 GOSUB 1530
980 GOTO 420
990 INPUT "+IN";K:INPUT "-IN";L:INPUT "-OUT";I:REM *** OP-AMP ***
1000 INPUT "+OUT";J:INPUT "GAIN(V/V)";R5:
     INPUT "OUTPUT RESISTANCE(OHMS)";V
1010 V=1/V
1020 GOSUB 1430
1030 V=V*R5
1040 GOSUB 1530
1050 GOTO 420
1060 INPUT "INPUT NODE";E:INPUT "OUTPUT NODE";F:N=N-1
1070 INPUT "START,STOP FREQUENCIES (HZ)";G,H
1080 INPUT "# OF DATA POINTS";M
1090 INPUT "FREQUENCY SWEEP-LOG=0(LINEAR=1)";R6
1091 PFG=0:INPUT "Do you want output data files";Q$:Q$=LEFT$(Q$,1)
1092 IF Q$="Y" OR Q$="y" THEN GOSUB 7000
1100 D=(H-G)/(M-1)
1110 R4=EXP(LOG(H/G)/(M-1))
1120 R0=G:R9=0
1130 R9=R9+1
1140 W=2*3.14159*R0
1150 O=E:Z=F
1160 GOSUB 2470
1170 GOSUB 2200
1180 V=R5:U=Z
1190 IF (E+F)/2=INT((E+F)/2) THEN 1210
1200 U=U-180
1210 O=E:Z=E
1220 GOSUB 2200
1230 U=U-Z
1240 IF V=0 THEN R7=-999:GOTO 1270
1250 IF R5=0 THEN R7=9999:GOTO 1270
1260 V=V/R5:R7=8.68589*LOG(V)
1270 IF U>180 THEN U=U-360
1280 IF U<-180 THEN U=U+360
1290 PRINT USING P$;R0,V,R7,U
1300 IF H$="Y" THEN LPRINT USING P$;R0,V,R7,U
1302 IF PFG=0 THEN GOTO 1310
1304 GOSUB 7200
1310 IF R6=0 THEN R0=R0*R4
1320 IF R6<>0 THEN R0=R0+D
1330 IF R9<>M THEN 1130
1340 N=N+1
1350 CLOSE:GOTO 420
1360 R(I,I)=R(I,I)+V:REM INDL
1370 R(J,J)=R(J,J)+V
1380 R(I,J)=R(I,J)-V
1390 R(J,I)=R(J,I)-V
1400 IF I>N THEN N=I
1410 IF J>N THEN N=J
1420 RETURN
1430 P(I,I)=P(I,I)+V:REM RESL
1440 P(J,J)=P(J,J)+V
1450 P(I,J)=P(I,J)-V
1460 P(J,I)=P(J,I)-V
1470 GOTO 1400
1480 Q(I,I)=Q(I,I)+V
1490 Q(J,J)=Q(J,J)+V:REM CAPL
1500 Q(I,J)=Q(I,J)-V
1510 Q(J,I)=Q(J,I)-V
1520 GOTO 1400
1530 P(I,K)=P(I,K)+V:REM TRANS
1540 P(J,L)=P(J,L)+V
1550 P(J,K)=P(J,K)-V
1560 P(I,L)=P(I,L)-V
1570 IF K>N THEN N=K
1580 IF L>K THEN N=L
1590 GOTO 1400
1600 IF N>1 THEN 1630: REM COMP
1610 O=A(1,1):Z=B(1,1)
1620 RETURN
1630 O=1
1640 Z=0
1650 K=1
1660 L=K
1670 S=ABS(A(K,K))+ABS(B(K,K))
1680 I=K-1
1690 I=I+1
1700 T=ABS(A(I,K))+ABS(B(I,K))
1710 IF S>=T THEN 1730
1720 L=I:S=T
1730 IF I<>N THEN 1690
1740 IF L=K THEN 1800
1750 J=0
1760 J=J+1
1770 S=-A(K,J):A(K,J)=A(L,J):A(L,J)=S
1780 A=-B(K,J):B(K,J)=B(L,J):B(L,J)=A
1790 IF J<>N THEN 1760
1800 L=K+1:I=L-1
1810 I=I+1
1820 A=A(K,K)*A(K,K)+B(K,K)*B(K,K)
1830 S=(A(I,K)*A(K,K)+B(I,K)*B(K,K))/A
1840 B(I,K)=(A(K,K)*B(I,K)-A(I,K)*B(K,K))/A
1850 A(I,K)=S
1860 IF I<>N THEN 1810
1870 C=K-1
```

load impedances (viz., signal and intermediate-frequency impedances) directly affects the conversion efficiency.

If we assume that our local-oscillator excitation is an idealized square-wave, the switching action may be represented by the Fourier series as,

$$s(x) = \frac{1}{2} + \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{\sin(2n-1)\,\omega t}{(2n-1)} \qquad \text{Eq. (1)}$$

The switching function, $\varepsilon(t)$, shown in the derivative equivalent circuit of Figure 2, is derived from the magnitude of this Fourier series expansion as a power function by squaring the first term, viz., $(\frac{2}{\pi})^2$.

The available power that can be delivered from a generator of RMS open-circuit terminal voltage, V_{in}, and internal resistance, R_g, is,

$$P_{av} = \frac{V_{in}^2}{4R_g} \qquad \text{Eq. (2)}$$

or, in terms shown in Figure 3,

$$P_{av} = \frac{V_{in}^2}{\pi^2 R_g} \qquad \text{Eq. (3)}$$

The output power, deliverable to the intermediate-frequency port, is,

$$P_{out} = \frac{V_o^2}{R_L} \qquad \text{Eq. (4)}$$

To arrive at V_o, we first need to obtain the loop current, i_L, which from Figure 3, offers,

$$i_L = \frac{V_{in}}{\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}} \qquad \text{Eq. (5)}$$

then,

$$V_o = \frac{V_{in} R_L}{\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}} \qquad \text{Eq. (6)}$$

Combining Eqs. (4) and (6),

$$P_{out} = \frac{V_{in}^2 R_L}{\left[\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}\right]^2} \qquad \text{Eq. (7)}$$

Conversion efficiency -- in the case for the commutation mixer, a loss -- may be calculated from the ratio of P_{av} and P_{out},

$$L_c = 10 \log \frac{P_{av}}{P_{out}} \quad dB \qquad \text{Eq. (8)}$$

Substituting Eq. (3) for P_{av}, and Eq. (7) for P_{out}, we obtain,

$$L_c = 10 \log \frac{\left[\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}\right]^2}{\pi^2 R_L R_g} \quad dB \qquad \text{Eq. (9)}$$

The conversion loss represented by Eq. (9) is for a broadband double-balanced mixer with all ports matched to the characteristic line impedances. The ideal commutation mixer operating with resistive source and load impedances will result in having the image and all harmonic frequencies dissipated. For this case, the optimum conversion loss reduces to,

$$L_c = 10 \log \frac{4}{\pi^2} \quad dB \qquad \text{Eq. (10)}$$

or -3.92 dB.

However, a truly optimum mixer also demands that the MOSFETs exhibit an ON-state of zero Ohms, and, of course, an ideal square-wave excitation. Neither is possible in a practical sense.

Equation 9 can be examined for various values of source and load impedances as well as r_{DS} by graphical representation, as shown in Figure 4, re-

```
1880 IF C=0 THEN 1960
1890 J=L-1
1900 J=J+1:I=0
1910 I=I+1
1920 A(K,J)=A(K,J)-A(K,I)*A(I,J)+B(K,I)*B(I,J)
1930 B(K,J)=B(K,J)-B(K,I)*A(I,J)-A(K,I)*B(I,J)
1940 IF C<>I THEN 1910
1950 IF J><N THEN 1900
1960 C=K
1970 K=K+1:I=K-1
1980 I=I+1:J=0
1990 J=J+1
2000 A(I,K)=A(I,K)-A(I,J)*A(J,K)+B(I,J)*B(J,K)
2010 B(I,K)=B(I,K)-B(I,J)*A(J,K)-A(I,J)*B(J,K)
2020 IF J<>C THEN 1990
2030 IF I<>N THEN 1980
2040 IF K<>N THEN 1660
2050 L=1
2060 C=INT(N/2)
2070 IF N=2*C THEN 2100
2080 L=0
2090 O=A(N,N):Z=B(N,N)
2100 I=0
2110 I=I+1
2120 J=N-I+L
2130 S=A(I,I)*A(J,J)-B(I,I)*B(J,J)
2140 A=A(I,I)*B(J,J)+A(J,J)*B(I,I)
2150 T=O*S-Z*A
2160 Z=Z*S+O*A
2170 O=T
2180 IF I<>C THEN 2110
2190 RETURN
2200 R5=N:REM DET
2210 N=N-1
2220 I=0
2230 K=0
2240 K=K+1
2250 IF K<>O THEN 2270
2260 I=1
2270 J=0:L=0
2280 L=L+1
2290 IF L<>Z THEN 2310
2300 J=1
2310 A(K,L)=P(K+I,L+J)
2320 B(K,L)=W*Q(K+I,L+J)-R(K+I,L+J)/W+S(K+I,L+J)
2330 IF L<>N THEN 2280
2340 IF K<>N THEN 2240
2350 GOSUB 1600
2360 N=R5
2370 R5=SQR(O*O+Z*Z)
2380 Y=Z
2390 IF O=0 THEN 2450
2400 Z=180/3.14159*ATN(Z/O)
2410 IF O>0 THEN RETURN
2420 Z=Z+SGN(Y)*180
2430 IF Y=0 THEN Z=180
2440 RETURN
2450 Z=90*SGN(Y)
2460 RETURN
2470 IF T(1)=0 THEN RETURN
2480 X=0
2490 R1=0
2500 R1=R1+1:R2=0
2510 R2=R2+1
2520 S(R1,R2)=0
2530 IF R2<>N+1 THEN 2510
2540 IF R1<>N+1 THEN 2500
2550 X=X+1
2560 IF X>20 THEN RETURN
2570 IF T(X)=0 THEN RETURN
2580 IF T(X)=1 THEN 2640
2590 IF T(X)=2 THEN 2830
2600 R1=-1/(Z(X)*TAN(.25*W/L(X)))
2610 Q=M(X):R=N(X)
2620 GOSUB 2870
2630 GOTO 2550
2640 R1=-1/(Z(X)*TAN(.25*W/L(X)))
2650 Q=M(X):R=I(X)
2660 GOSUB 2870
2670 Q=N(X):R=O(X):GOSUB 2870
2680 R1=1/(Z(X)*SIN(.25*W/L(X)))
2690 P=I(X)
2700 R=N(X)
2710 S(R,P)=S(R,P)-R1
2720 S(P,R)=S(P,R)-R1
2730 R=O(X)
2740 S(R,P)=S(R,P)+R1
2750 S(P,R)=S(P,R)+R1
2760 P=M(X)
2770 S(R,P)=S(R,P)-R1
2780 S(P,R)=S(P,R)-R1
2790 R=N(X)
2800 S(R,P)=S(R,P)+R1
2810 S(P,R)=S(P,R)+R1
2820 GOTO 2550
2830 R2=1/(Z(X)*TAN(.25*W/L(X)))
2840 R3=1/(Z(X)*SIN(.25*W/L(X)))
2850 R1=R3*R3/R2-R2
2860 GOTO 2610
2870 S(Q,Q)=S(Q,Q)+R1
2880 S(R,R)=S(R,R)+R1
2890 S(Q,R)=S(Q,R)-R1
2900 S(R,Q)=S(R,Q)-R1
2910 RETURN
2920 END
3000 INPUT "NAME OF FILE TO LOAD <CR> FOR DIRECTORY";F$:
     ' LOAD FROM FILE
3010 IF LEN(F$)=0 THEN FILES:GOTO 3000
3020 IF F$="B:" THEN FILES "B:*.*":GOTO 3000
3030 IF F$="A:" THEN FILES "A:*.*":GOTO 3000
```

membering that a nominal 3.92 dB must be added to the values obtained from the graph.

To illustrate how seriously the ON-state of the MOSFETs affects performance, we need only to consider the Si8901 with a nominal r_{DS} (at V_{GS}=15V) of 23 ohms. With a 1:1 signal transformer (50 to 25-0-25Ω), Rg/r_{DS} = 1.1. Allowing a 4:1 IF output impedance to a 50 ohm preamplifier, the ratio R_L/r_{DS} approximates 4. From Figure 4 we read a conversion loss, L_c, of approximately 3.7 dB, to which we add 3.92 dB for a total loss of 7.62 dB. Additionally, we must also include the losses incurred by both the signal and IF transformers. The results compare favorably with measured data.

A careful study of Figure 4 reveals what appears as an anomalous characteristic. If we were to raise R_g/r_{DS} from 1.1 to 4.3 (by replacing the 1:1 transformer with a 1:4 to effect a signal-source impedance of 100-0-100Ω), we would see a dramatic improvement in conversion efficiency! The anomaly is that this suggests that a mismatched signal-input port improves performance.

Caruthers [4] first suggested that reactively terminating all harmonic and parasitic frequencies would reduce the conversion loss of a ring demodulator to zero. This, of course, would also require that the active mixing elements (MOSFETs in this case) have zero r_{DS}, in keeping with the data of Figure 4.

A double-balanced mixer is a 4-port, consisting of a signal, image, IF and local-oscillator port. Of these, the most difficult to terminate is the image-frequency port simply because, in theory it exists as a separate port, but in practice it shares the signal port. Any reactive termination would, therefore, be narrow-band irrespective of its proximity to the active mixing elements.

The performance of an image-termination filter offering a true reactance to the image frequency (100% reflective) may be deduced to a reasonable degree from Figure 4, if we first presume that the conversion loss between signal and IF compares with that between signal and image. The relationship is displayed in Figure 5 where we see the expected variation in amplitude proportional to conversion efficiency (inversely proportional to conversion loss).

Image-frequency filtering affects more than conversion efficiency. As the phase of the detuned-short position of the image-frequency filter is varied we are able to witness a cyclical variation in the intermodulation distortion as has been confirmed by measurement, shown in Figure 6. By comparing Figure 5 with Figure 6, we see that any improvement in conversion loss appears to offer a corresponding degradation in the intermodulation distortion.

INTERMODULATION DISTORTION

Unbalanced, single-balanced and double-balanced mixers are distinguished by their ability to selectively reject spurious frequency components, as defined in table I. The double-balanced mixer, by virtue of its symmetry, suppresses twice the number of spurious frequencies as does the single-balanced mixer.

In the ideal mixer, the input signal is translated to an intermediate-

```
3040 OPEN "I",#1,F$
3050 INPUT #1,X
3060 ERASE A,B,P,Q,R,S,I,T,M,N,O,L,Z
3070 DIM A(X,X),B(X,X),P(X,X),Q(X,X),R(X,X)
3080 DIM S(X,X),I(2*X)
3090 DIM T(2*X),M(2*X),N(2*X),O(2*X),L(2*X),Z(2*X)
3095 INPUT #1,N
3100 FOR J=1 TO X
3110 INPUT #1,I(J),T(J),M(J),N(J),O(J),L(J),Z(J)
3120 FOR K=1 TO X
3130 INPUT #1,A(J,K),B(J,K),P(J,K),Q(J,K),R(J,K),S(J,K)
3140 NEXT K
3150 NEXT J
3160 CLOSE #1
3170 NODES=X:GOTO 420
3500 INPUT "NAME OF FILE TO SAVE <CR> FOR DIRECTORY";F$:
     ' SAVE INTO FILE
3510 IF LEN(F$)=0 THEN FILES:GOTO 3500
3520 IF F$="B:" THEN FILES "B:*.*":GOTO 3500
3530 IF F$="A:" THEN FILES "A:*.*":GOTO 3500
3540 OPEN "O",#1,F$
3550 PRINT #1,NODES,N
3600 FOR J=1 TO NODES
3610 PRINT #1,I(J),T(J),M(J),N(J),O(J),L(J),Z(J)
3620 FOR K=1 TO NODES
3630 PRINT #1,A(J,K),B(J,K),P(J,K),Q(J,K),R(J,K),S(J,K)
3640 NEXT K
3650 NEXT J
3660 CLOSE #1
3670 GOTO 420
4000 INPUT "Name of file to load <cr> for directory";F$
4010 IF LEN(F$)=0 THEN FILES:GOTO 4000
4020 OPEN "I",#1,F$
4030 IF EOF(1) THEN CLOSE:GOTO 420
4035 R6$="":INPUT #1,R6$:R6$=LEFT$(R6$,1)
4040 IF R6$="1" THEN GOTO 4320
4050 IF R6$="2" THEN GOTO 4400
4060 IF R6$="3" THEN GOTO 4360
4070 IF R6$="4" THEN GOTO 4150
4080 IF R6$="5" THEN GOTO 4280
4090 IF R6$="6" THEN GOTO 4300
4100 IF R6$="7" THEN GOTO 4580
4110 IF R6$="8" THEN GOTO 4470
4120 IF R6$="9" THEN GOTO 4430
4130 IF EOF(1) THEN 420
4140 GOTO 4030
4150 T(X)=1:INPUT #1,M$:M(X)=VAL(M$):REM *** TRANSMISSION LINE ***
4160 INPUT #1,I$:I(X)=VAL(I$):INPUT #1,O$:O(X)=VAL(O$)
4170 INPUT #1,N$:N(X)=VAL(N$):GOTO 4200
4180 INPUT #1,M$:M(X)=VAL(M$)
4190 INPUT #1,N$:N(X)=VAL(N$)
4200 INPUT #1,Z$:Z(X)=VAL(Z$)
4210 INPUT #1,L$:L(X)=VAL(L$)
4220 IF I(X)>N THEN N=I(X)
4230 IF M(X)>N THEN N=M(X)
4240 IF N(X)>N THEN N=N(X)
4250 IF O(X)>N THEN N=O(X)
4260 X=X+1:T(X)=0
4270 GOTO 4030
4280 T(X)=3: REM *** SHORTED STUB ***
4290 GOTO 4180
4300 T(X)=2: REM *** OPEN STUB ***
4310 GOTO 4180
4320 INPUT #1,I$:I=VAL(I$):
     INPUT #1,J$:J=VAL(J$):INPUT #1,V$:V=VAL(V$)
4330 V=1/V
4340 GOSUB 1430
4350 GOTO 4030
4360 INPUT #1,I$:I=VAL(I$):
     INPUT #1,J$:J=VAL(J$):INPUT #1,V$:V=VAL(V$)
4370 V=1/V
4380 GOSUB 1360
4390 GOTO 4030
4400 INPUT #1,I$:I=VAL(I$):
     INPUT #1,J$:J=VAL(J$):INPUT #1,V$:V=VAL(V$)
4410 GOSUB 1480
4420 GOTO 4030
4430 INPUT #1,K$:K=VAL(K$):INPUT #1,J$:J=VAL(J$):INPUT #1,I$:
     I=VAL(I$):INPUT #1,V$:V=VAL(V$)
4440 L=J
4450 GOSUB 1530
4460 GOTO 4030
4470 INPUT #1 "BASE";K:INPUT #1,J$:J=VAL(J$):INPUT #1,I$:
     I=VAL(I$):INPUT #1,R$:R5=VAL(R$)
4480 INPUT #1,V$:V=VAL(V$)
4490 V=1/V
4500 L=I
4510 I=K
4520 GOSUB 1430
4530 I=L
4540 L=J
4550 V=V*R5
4560 GOSUB 1530
4570 GOTO 4030
4580 INPUT #1,K$:K=VAL(K$):INPUT #1,L$:L=VAL(L$):
     INPUT #1,I$:I=VAL(I$)
4590 INPUT #1,J$:J=VAL(J$):INPUT #1,R$:R5=VAL(R$):
     INPUT #1,V$:V=VAL(V$)
4600 V=1/V
4610 GOSUB 1430
4620 V=V*R5
4630 GOSUB 1530
4640 GOTO 4030
5000 INPUT "Name of file (<cr> for Directory)";F$
5010 IF LEN(F$)=0 THEN FILES:GOTO 5000
5020 OPEN "O",#1,F$
5200 PRINT "1   RESISTOR"
5210 PRINT "2   CAPACITOR"
5220 PRINT "3   INDUCTOR"
5230 PRINT "4   TRANSMISSION LINE"
```

frequency without distortion, viz., without imparing any of the contained information. Regrettably, the ideal mixer does not occur in practice. Because of certain nonlinearities within the switching elements as well as imperfect switching resulting in phase modulation, distortion results.

Identifying Intermodulation Distortion Products

The most damaging intermodulation distortion products (IMD) in receiver design are generally those attributed to odd-order, and, in particular, to those identified as the third-order IMD.

Any nonlinear device may be represented as a power series,

$$i_d = g_m e_g + \frac{1}{2!}\frac{\delta g_m}{\delta V_G} e_g^2 + \frac{1}{3!}\frac{\delta^2 g_m}{\delta V_G^2} e_g^3 + \ldots \frac{1}{n!}\frac{\delta^{n-1} g_m}{\delta V_G^{n-1}} e_g^n \qquad \text{Eq. (11)}$$

which can be further broken into

TERM	OUTPUT	TRANSFER CHARACTERISTIC
$g_m e_g$	F1, F2	Linear
$\frac{1}{2!}\frac{\delta g_m}{\delta V_G} e_g^2$	2F1, 2F2 F1 ± F2	[Second-order Square-Law]
$\frac{1}{3!}\frac{\delta^2 g_m}{\delta^2 V_G} e_g^3$	3F1, 3F2 2F1 ± F2 2F2 ± F1	Third-Order

The second term is the desired intermediate-frequency we seek, all other higher-orders are undesirable, but, unfortunately, present to a varyign degree as illustrated in Figure 7.

There are both fixed-level IMD products and level-dependent IMD products.[5] The former are produced by the interaction between a fixed-level signal, such as the local oscillator and the variable-amplitude signal. The resulting frequencies may be identified,

$$n\delta_1 \pm \delta_2 \qquad \text{Eq. (12)}$$

where, n is an integer greater than 1.

Level-dependent IMD products result from the interaction of the harmonics of the local oscillator and those of the signal. The resulting frequencies may be identified,

$$n\delta_1 \pm m\delta_2 \qquad \text{Eq. (13)}$$

where, m and n are integers greater than 1.

For a mixer to generate IMD products at the intermediate frequency we must account for at least a two-step process. First, the generation of the harmonics of the signal and local oscillator; and, second, the mixing or conversion of these frequencies to the intermediate frequency. Consequently, the mixer may be modelled as a series connection of two nonlinear impedances, the first to generate the harmonic products, the second to mix or convert to the intermediate frequency. Although many harmonically-related products are possible, we will focus principally on odd-order IMD products.

If we allow two interfering signals, f_1 and f_2, to impinge upon the first nonlinear element of our mixer model, the result will be $2f_1 - f_2$ and $2f_2 - f_1$. These are identified as third-order intermodulation products (IMD_3). Other products are also generated taking the form $3f_1 - 2f_2$ and $3f_2 - 2f_1$, called fifth-order IMD products (IMD_5). Unlike the even-order products, odd order products lie close to the fundamental signals and, as a consequence, are

```
5240 PRINT "5   SHORTED STUB"
5250 PRINT "6   OPEN STUB"
5260 PRINT "7   OPERATIONAL AMPLIFIER"
5270 PRINT "8   NPN TRANSISTOR"
5280 PRINT "9   FIELD-EFFECT TRANSISTOR"
5290 PRINT "10  STOP"
5360 R6=0:INPUT "SELECT FROM LIST";R6:R6$=STR$(R6)
5370 IF R6=1 THEN PRINT "(1) RESISTOR":GOTO 5690
5380 IF R6=2 THEN PRINT "(2) CAPACITOR":GOTO 5770
5390 IF R6=3 THEN PRINT "(3) INDUCTOR":GOTO 5730
5400 IF R6=4 THEN PRINT "(4) TRANSMISSION LINE":GOTO 5520
5410 IF R6=5 THEN PRINT "(5) SHORTED STUB":GOTO 5650
5420 IF R6=6 THEN PRINT "(6) OPEN STUB":GOTO 5670
5430 IF R6=7 THEN PRINT "(7) OP AMP":GOTO 5950
5440 IF R6=8 THEN PRINT "(8) NPN TRANSISTOR":GOTO 5840
5450 IF R6=9 THEN PRINT "(9) FET TRANSISTOR":GOTO 5800
5460 IF R6=10 THEN PRINT "(10) FILE COMPLETED":CLOSE #1:GOTO 420
5510 GOTO 5360
5520 INPUT "SHIELD IN";M$:REM *** TRANSMISSION LINE ***
5530 INPUT "CENTER IN";I$:INPUT "CENTER OUT";O$
5531 PRINT #1,R6$+" * TRANSMISSION LINE"
5532 PRINT #1,M$
5533 PRINT #1,I$
5534 PRINT #1,O$
5540 INPUT "SHIELD OUT";N$:PRINT #1,N$:GOTO 5570
5550 INPUT "NODE A";M$:PRINT #1,M$
5560 INPUT "NODE B";N$:PRINT #1 N$
5570 INPUT "Z0";Z$:PRINT #1,Z$
5580 INPUT "QUARTER-WAVE FREQUENCY (HZ)";L$:PRINT #1,L$
5640 GOTO 5360
5650 REM *** SHORTED STUB ***
5655 PRINT #1,R6$+" * SHORTED STUB"
5660 GOTO 5550
5670 PRINT #1,R6$+" * OPEN STUB":REM *** OPEN STUB ***
5680 GOTO 5550
5690 INPUT "NODE A";I$:INPUT "NODE B";J$:
     INPUT "RESISTANCE (OHMS)";V$
5700 PRINT #1,R6$+" * RESISTOR"
5702 PRINT #1,I$
5704 PRINT #1,J$
5706 PRINT #1,V$
5720 GOTO 5360
5730 INPUT "NODE A";I$:INPUT "NODE B";J$:
     INPUT "INDUCTANCE (H)";V$
5740 PRINT #1,R6$+" * INDUCTOR"
5742 PRINT #1,I$
5744 PRINT #1,J$
5746 PRINT #1,V$
5760 GOTO 5360
5770 INPUT "NODE A";I$:INPUT "NODE B";J$:
     INPUT "CAPACITANCE (FARADS)";V$
5775 PRINT #1,R6$+" * CAPACITOR"
5790 GOTO 5742
5800 INPUT "GATE";K$:INPUT "SOURCE";J$:INPUT "DRAIN";I$:
     INPUT "GAIN(MHO)";V$
5810 PRINT #1,R6$+" * FET"
5812 PRINT #1,K$
5814 PRINT #1,J$
5816 PRINT #1,I$
5818 PRINT #1,V$
5830 GOTO 5360
5840 INPUT "BASE";K$:INPUT "EMITTER";J$:INPUT "COLLECTOR";I$:
     INPUT "BETA";R5$
5850 INPUT "Rbe (OHMS)";V$
5860 PRINT #1,R6$+" * NPN TRANSISTOR"
5861 PRINT #1,K$
5862 PRINT #1,J$
5863 PRINT #1,I$
5864 PRINT #1,R5$
5865 PRINT #1,V$
5940 GOTO 5360
5950 INPUT "+IN";K$:INPUT "-IN";L$:INPUT "-OUT";I$:REM *** OP-AMP ***
5960 INPUT "+OUT";J$:INPUT "GAIN(V/V)";R5$:
     INPUT "OUTPUT RESISTANCE(OHMS)";V$
5970 PRINT #1,R6$+" * OP-AMP"
5972 PRINT #1,K$
5974 PRINT #1,L$
5976 PRINT #1,I$
5978 PRINT #1,J$
5980 PRINT #1,R5$
5990 PRINT #1,V$
6010 GOTO 5360
7000 ' SUBROUTINES FOR FILE HANDLING
7010 FOR J=1 TO 4:READ FL$(J,1):FL$(J,2)="N":NEXT J
7020 FOR J=1 TO 4
7030 IF FL$(J,2)="Y" THEN GOTO 7050
7040 PRINT STR$(J)+"- "+FL$(J,1)
7050 NEXT J
7060 PRINT
7070 INPUT "Choice (enter <cr> or 0 to exit)";C:C=INT(C)
7080 IF FL$(C,2)="Y" THEN PRINT "Already Selected!":GOTO 7070
7090 IF C=0 THEN RESTORE:RETURN
7100 PFG=1:INPUT "Name of Data File (<cr> for Directory)";F$
7110 IF LEN(F$)=0 THEN FILES:GOTO 7100
7120 FL$(C,2)="Y":OPEN "O",C,F$
7130 GOTO 7020
7140 DATA "Amplitude versus Frequency","Phase versus Frequency"
7150 DATA "Amplitude,Phase vs. Frequency","Amplitude vs. Phase"
7160 CLOSE
7200 FOR JJ=1 TO 4
7210 IF FL$(JJ,2)="N" THEN GOTO 7270
7220 ON JJ GOTO 7230,7240,7250,7260
7230 WRITE #1,R0,V:GOTO 7270
7240 WRITE #2,R0,U:GOTO 7270
7250 WRITE #3,R0,V,U:GOTO 7270
7260 WRITE #4,V,U
7270 NEXT JJ
7280 RETURN
```

most susceptible of falling within the passband of the intermediate frequency and thus degrading the performance of the mixer.

A qualitative definition of linearity based upon intermodulation distortion performance is called the Intercept Point. By recognizing that,

the fundamental output (IF) response is directly proportional to the signal input level;

the second-order output response is proportional to the square of the signal input level; and,

the third-order output response is proportional to the cube of the signal input level,

then convergence occurs. The point of convergence is termed the Intercept Point. The higher the value of this intercept point, the better the dynamic range.

Intermodulation Distortion in the Commutation Mixer

Although the double-balanced mixer outperforms the single-balanced mixer as we saw in Table I, a more serious source of intermodulation products result when the local-oscillator excitation departs from the idealized square-wave.[6][7] This phenomenon is easily recognized by a careful examination of Figure 8, where a sinusoidal local-oscillator voltage reacts not only upon a varying transfer characteristic but also on a varying nonlinear, voltage-dependent capacitance (not shown in Figure 8). Although the effects of this sinusoidal transition are not easily derived, Ward [8] and Rafuse [9] have concluded that lowering R_g will provide improved intermodulation performance! This conflicts with low conversion loss, as we saw in Figure 4.[10]

Further examination of Figure 8 reveals that the sinusoidal local-oscillator excitation results in phase modulation. That is, as the sinusoidal wave goes through a complete cycle, the resulting gate voltage, acting upon the MOSFET's transfer characteristic, produces a resulting nonlinear waveform. Since all FETs have some offset -- a JFET has a cut-off voltage; a MOSFET has threshold voltage -- it is important, for symmetry as well as for balance, to offer some DC offset voltage to the gates. Optimum IMD performance demands that the switches operate in a 50% duty cycle; that is, the switches must be fully ON and fully OFF for equal time. Without some form of offset bias this would be extremely difficult unless we were to implement an idealized square-wave drive.

Walker [11] has derived an expression showing the predicted improvement in the relative level of two-tone third-order intermodulation products (IMD_3) as a function of the rise and fall times of the local-oscillator waveforms.

$$20 \log \left[\frac{\left[t_r \, \omega_{LO} \, \frac{V_\Delta}{V_c} \right]^2}{8} \right] \; dB \qquad \text{Eq. (14)}$$

where, V_c is the peak-to-peak local-oscillator voltage,

V_Δ is the peak signal voltage,

t_r is the rise and fall time of V_c,

ω_{LO} is the local-oscillator frequency.

Equation 14 offers us several interesting aspects on performance. Since any reduction in the magnitude of V_s improves the IMD, we again discover that lowering R_g (which, in turn, decreases the magnitude of V_s) appears to bene-

APPENDIX B.2 Example of circuit data file for input to the program NET85.ASC. This file can be generated by the program itself or generated or modified by any text editor. The /* */ are delimiters for remarks and are not added by the program. They have been added for explanation of the file structure. Note that the file structure is the same as is input from the keyboard.

```
 1 * RESISTOR          /* Type of element (1 is a resistor) */
1                      /* Node A  */
2                      /* Node B  */
50
 1 * RESISTOR
4
7
50
 1 * RESISTOR
6
7
50
 2 * CAPACITOR
3
7
58E-12                  /* Value of capacitor in farads (58 pf */
 2 * CAPACITOR
2
5
23E-12
 2 * CAPACITOR
5
6
23E-12
 3 * INDUCTOR
2
3
72E-9                   /* This is a 72 nh inductor */
 3 * INDUCTOR
3
4
72E-9
 3 * INDUCTOR
5
7
28E-9
```

APPENDIX B.3 Sample output file from NET85.ASC. This data can be edited with any text editor, added to a report, or used by a plotting program, such as PCPLOT2 (BV Engineering, Riverside, CA):

(The first number is frequency, the second is amplitude.)

```
8E+07,3.543465E-02
8.269104E+07,3.831959E-02
8.54726E+07,4.173018E-02
8.834772E+07,4.599374E-02
9.131957E+07,.0516254
9.439138E+07,5.938689E-02
9.756651E+07,7.032793E-02
1.008485E+08,8.579546E-02
1.042408E+08,.1073953
1.077473E+08,.1368522
1.113717E+08,.1755944
1.15118E+08,.2237623
1.189903E+08,.2785856
1.229929E+08,.3333452
1.271301E+08,.3794872
1.314065E+08,.4116778
1.358268E+08,.430391
1.403957E+08,.4395925
1.451184E+08,.4434264
1.499998E+08,.4447783
```

fit performance. Second, the higher the local-oscillator voltage the better the IMD performance. Third, if we can provide the idealized square-wave drive we achieve infinite improvement in IMD performance!

An additional fault of sinusoidal local-oscillator excitation results whenever the wave approaches the zero-crossing at half-period intervals. As the voltage decays we find that any signal votlage may overload the MOSFETs causing intermodulation and crossmodulation distortion.[12] This can be easily visualized from Figure 9 where we see the classic i-ℓ characteristics of the MOSFET at varying gate voltages. Only at substantial gate voltage do we witness reasonable linearity, and consequently, good dynamic range.

DYNAMIC RANGE OF THE COMMUTATION MIXER

As the two-tone Intercept Point increases in magnitude, we generally conclude a like improvement in dynamic range results. Yet, as we have concluded from earlier study, the intermodulation products appear to be a function of both the generator or source impedance as well as the ratio R_g/r_{DS} and R_L/r_{DS} (see Figure 4).

In any receiver performance can be quantified by the term Dynamic range. Dynamic range can be extended by improving the sensitivity to low-level signals and by increasing the power-handling ability without being overcome by interfering intermodulation products or the effects caused from desensitization.

There are rules to follow if we are to improve the low-level signal sensitivity. Ideally we would like a mixer to be transparent, acting only to manipulate the incoming signals for easy processing by subsequent equipment. The perfect mixer would have no conversion loss and a zero noise figure. However, in the preceeding analysis we discovered that optimum intermodulation performance occurred when the signal-input port is mismatched to the quad MOSFETs (Figure 4). It now becomes clear that a performance trade-off appears necessary. Either we seek low conversion loss and with it a lower noise figure, or we aim for the highest two-tone intercept point. Fortunately, as we seek the latter, our dynamic range will actually improve since a mismatched signal port has less effect upon the signal-to-noise performance of the mixer than does a matched signal port have upon the intermodulation distortion.

Convention has identified minimum sensitivity to be the weakest signal which will produce an output signal 10 dB over that of the noise in a prescribed bandwidth (usually 1 kHz), or

$$Sens. = 20\ Log\ \frac{V_S + V_N}{V_N} + 10\ dB \qquad \text{Eq. (15)}$$

Desensitation occurs whenever a nearby unwanted signal causes the compression of the desired signal. The effect appears as an increase in the mixer's conversion loss.

THE Si8901 AS A COMMUTATION MIXER

Because of package and parasitic constraints, the Si8901 appears best suited for performance in the HF to low VHF region. A surface-mounted version may extend performance to higher frequencies.

In our review of intermodulation distortion we recognized that to achieve

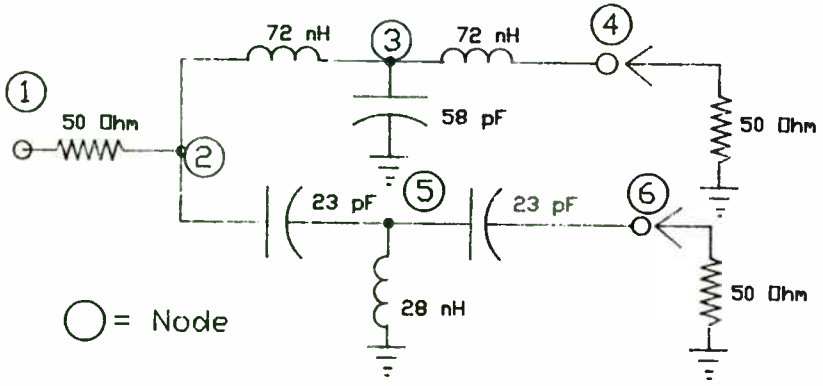

FIGURE 1

Prototype Diplexer Design

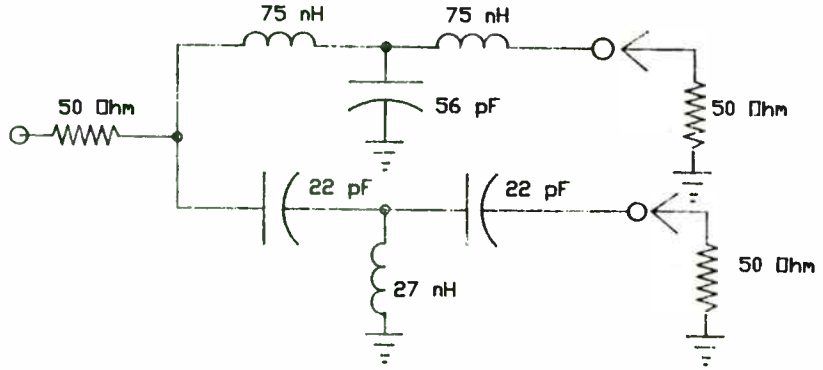

FIGURE 3

Diplexer Design using RETMA Values

LOW-PASS SECTION

FREQ=	8.0000E+07	AMPL=	4.56E-01	20LOG=	-6.8	PHASE=	-105.7
FREQ=	8.5000E+07	AMPL=	4.52E-01	20LOG=	-6.9	PHASE=	-113.1
FREQ=	9.0000E+07	AMPL=	4.49E-01	20LOG=	-7.0	PHASE=	-120.9
FREQ=	9.5000E+07	AMPL=	4.48E-01	20LOG=	-7.0	PHASE=	-129.1
FREQ=	1.0000E+08	AMPL=	4.47E-01	20LOG=	-7.0	PHASE=	-138.1
FREQ=	1.0500E+08	AMPL=	4.46E-01	20LOG=	-7.0	PHASE=	-148.2
FREQ=	1.1000E+08	AMPL=	4.42E-01	20LOG=	-7.1	PHASE=	-160.0
FREQ=	1.1500E+08	AMPL=	4.27E-01	20LOG=	-7.4	PHASE=	-173.6
FREQ=	1.2000E+08	AMPL=	3.94E-01	20LOG=	-8.1	PHASE=	171.2
FREQ=	1.2500E+08	AMPL=	3.40E-01	20LOG=	-9.4	PHASE=	155.7
FREQ=	1.3000E+08	AMPL=	2.75E-01	20LOG=	-11.2	PHASE=	142.0
FREQ=	1.3500E+08	AMPL=	2.13E-01	20LOG=	-13.4	PHASE=	131.6
FREQ=	1.4000E+08	AMPL=	1.62E-01	20LOG=	-15.8	PHASE=	124.7
FREQ=	1.4500E+08	AMPL=	1.25E-01	20LOG=	-18.1	PHASE=	121.1
FREQ=	1.5000E+08	AMPL=	9.77E-02	20LOG=	-20.2	PHASE=	120.1

HIGH-PASS SECTION

FREQ=	8.0000E+07	AMPL=	3.54E-02	20LOG=	-29.0	PHASE=	-136.8
FREQ=	8.5000E+07	AMPL=	4.11E-02	20LOG=	-27.7	PHASE=	-134.5
FREQ=	9.0000E+07	AMPL=	4.89E-02	20LOG=	-26.2	PHASE=	-130.4
FREQ=	9.5000E+07	AMPL=	6.12E-02	20LOG=	-24.3	PHASE=	-125.5
FREQ=	1.0000E+08	AMPL=	8.13E-02	20LOG=	-21.8	PHASE=	-121.8
FREQ=	1.0500E+08	AMPL=	1.13E-01	20LOG=	-18.9	PHASE=	-121.4
FREQ=	1.1000E+08	AMPL=	1.60E-01	20LOG=	-15.9	PHASE=	-125.3
FREQ=	1.1500E+08	AMPL=	2.22E-01	20LOG=	-13.1	PHASE=	-133.9
FREQ=	1.2000E+08	AMPL=	2.93E-01	20LOG=	-10.7	PHASE=	-146.4
FREQ=	1.2500E+08	AMPL=	3.57E-01	20LOG=	-8.9	PHASE=	-161.1
FREQ=	1.3000E+08	AMPL=	4.03E-01	20LOG=	-7.9	PHASE=	-175.9
FREQ=	1.3500E+08	AMPL=	4.28E-01	20LOG=	-7.4	PHASE=	171.0
FREQ=	1.4000E+08	AMPL=	4.39E-01	20LOG=	-7.1	PHASE=	160.1
FREQ=	1.4500E+08	AMPL=	4.43E-01	20LOG=	-7.1	PHASE=	151.0
FREQ=	1.5000E+08	AMPL=	4.45E-01	20LOG=	-7.0	PHASE=	143.4

FIGURE 2 - CALCULATED VALUES OF DIPLEXER

a high intercept point the local-oscillator drive must

approach the ideal square-wave;

ensure a 50% duty cycle; and,

offer sufficient amplitude to ensure a full ON and OFF switching condition, as well as to offer reduced r_{DS} when ON.

Furthermore, to maintain superior overall performance -- in conversion loss, dynamic range (noise figure) and intercept point -- some form of image frequency termination would be highly desirable even though, understandably, the mixer's bandwidth would be restricted. Consequently, the principal effort in the design of a high dynamic range commutation mixer is two-fold. First, and most crucial, is to achieve a gating or control voltage sufficient to ensure a positive and hard turn-ON as well as a complete turn-OFF of the mixing elements (MOSFETs). Second, and of lesser importance, is to properly terminate the parasitic and harmonic frequencies developed by the mixer.

Establishing the Gating Voltage

Local-oscillator injection to the conventional diode-ring, FET, or MOSFET double-balanced mixer is by the use of the broadband, transmission-line, transformer, [13] as shown in Figure 10. For the diode-ring mixer where switching is a function of loop current, or for active FET mixers that operate on the principle of transconductance and thus need little gate voltage, [14] the broadband transformer is adequate. If this approach is used for the commutation mixer, we would need extraordinarily high local-oscillator drive to ensure positive turn-ON. Rafuse [15] and Ward [16] used a minimum of 2 W to ensure mixing action; Lewis and Palmer [17] achieved high dynamic range using 5 Watts! The MOSFETs used in these early designs were p-channel, enhancement (2N4268) with moderately high threshold (6 V max.) and high input capacitance (6 pF max.). All of these early MOSFET double-balanced mixers relied on the conventional 50 to 100-0-100Ω transformer for local-oscillator injection to the gates.

A major goal is the conservation of power. This goal cannot be achieved using the conventional design. Simply increasing the turns ratio of the coupling transformer is thwarted by the reactive load presented by the gates.

The obvious solution is to use a resonant gate drive. The voltage appearing across the resonant tank -- and thus on the gates -- may be easily calculated,

$$V = (P \cdot Q \cdot X) \qquad \text{Eq. (16)}$$

P is the power delivered to the resonant tank circuit;

Q is the loaded Q of the tank circuit; and,

X is the reactance of the gate capacity.

Since the gate capacitance of the MOSFET is voltage dependent, the reactance of the gate becomes dependent upon the impressed excitation voltage. To allow this would severely degrade the IMD performance of the mixer. However, we can minimize the change in gate capacitance and remove its detrimental influence using a combination of substrate and gate bias, as shown in Figure 11. Not only does this show itself beneficial in this regard, but, as we saw in Figure 8, a gate bias is necessary to ensure the required 50% duty cycle. Furthermore, a negative substrate voltage ensures that each MOSFET on the monolithic substrate is electrically isolated and that each source-/drain-to-body

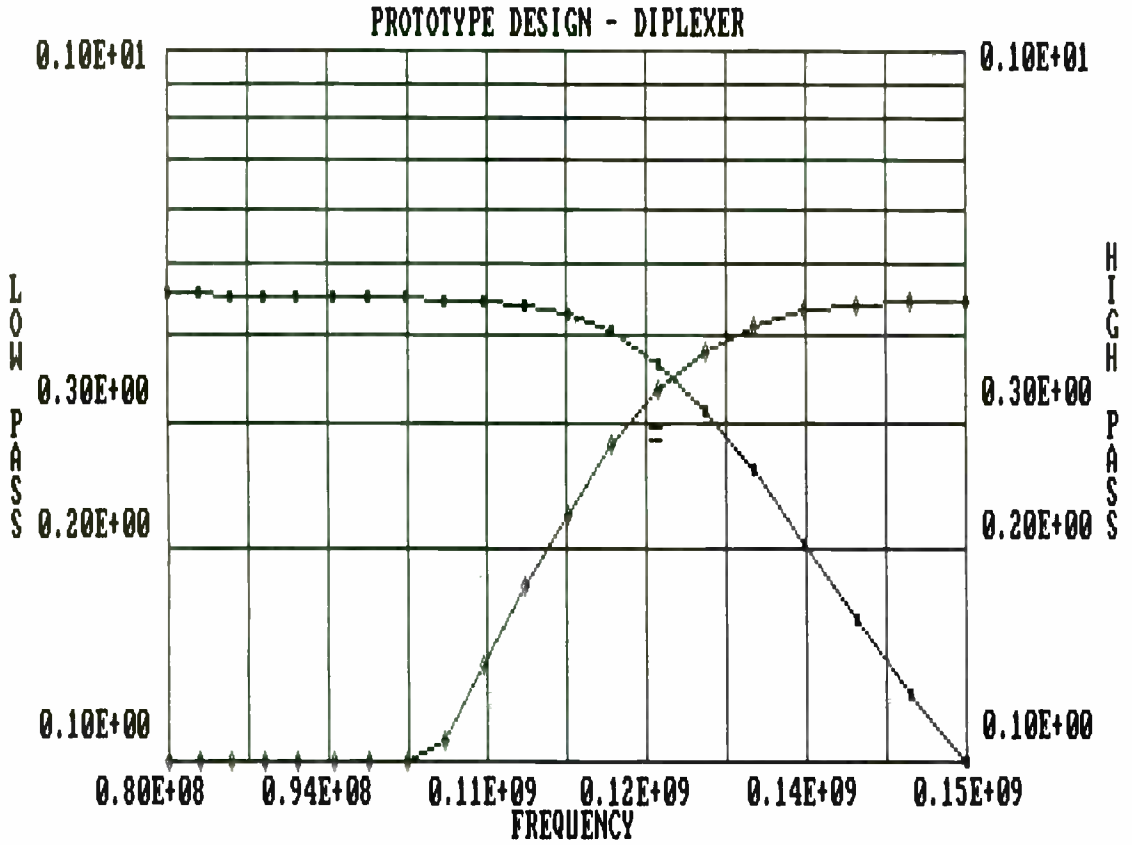

Figure 2(6)

LOW-PASS SECTION

FREQ=	8.0000E+07	AMPL=	4.62E-01	20LOG=	-6.7	PHASE=	-105.9
FREQ=	8.5000E+07	AMPL=	4.58E-01	20LOG=	-6.8	PHASE=	-113.4
FREQ=	9.0000E+07	AMPL=	4.55E-01	20LOG=	-6.8	PHASE=	-121.2
FREQ=	9.5000E+07	AMPL=	4.53E-01	20LOG=	-6.9	PHASE=	-129.4
FREQ=	1.0000E+08	AMPL=	4.52E-01	20LOG=	-6.9	PHASE=	-138.3
FREQ=	1.0500E+08	AMPL=	4.50E-01	20LOG=	-6.9	PHASE=	-148.3
FREQ=	1.1000E+08	AMPL=	4.46E-01	20LOG=	-7.0	PHASE=	-159.6
FREQ=	1.1500E+08	AMPL=	4.33E-01	20LOG=	-7.3	PHASE=	-172.6
FREQ=	1.2000E+08	AMPL=	4.06E-01	20LOG=	-7.8	PHASE=	172.8
FREQ=	1.2500E+08	AMPL=	3.59E-01	20LOG=	-8.9	PHASE=	157.5
FREQ=	1.3000E+08	AMPL=	2.99E-01	20LOG=	-10.5	PHASE=	143.2
FREQ=	1.3500E+08	AMPL=	2.36E-01	20LOG=	-12.5	PHASE=	131.3
FREQ=	1.4000E+08	AMPL=	1.82E-01	20LOG=	-14.8	PHASE=	122.6
FREQ=	1.4500E+08	AMPL=	1.40E-01	20LOG=	-17.1	PHASE=	117.0
FREQ=	1.5000E+08	AMPL=	1.08E-01	20LOG=	-19.3	PHASE=	114.2

HIGH-PASS SECTION

FREQ=	8.0000E+07	AMPL=	3.23E-02	20LOG=	-29.8	PHASE=	-134.9
FREQ=	8.5000E+07	AMPL=	3.73E-02	20LOG=	-28.6	PHASE=	-132.7
FREQ=	9.0000E+07	AMPL=	4.40E-02	20LOG=	-27.1	PHASE=	-128.6
FREQ=	9.5000E+07	AMPL=	5.45E-02	20LOG=	-25.3	PHASE=	-123.5
FREQ=	1.0000E+08	AMPL=	7.16E-02	20LOG=	-22.9	PHASE=	-119.3
FREQ=	1.0500E+08	AMPL=	9.88E-02	20LOG=	-20.1	PHASE=	-118.0
FREQ=	1.1000E+08	AMPL=	1.39E-01	20LOG=	-17.1	PHASE=	-120.7
FREQ=	1.1500E+08	AMPL=	1.94E-01	20LOG=	-14.2	PHASE=	-127.9
FREQ=	1.2000E+08	AMPL=	2.59E-01	20LOG=	-11.7	PHASE=	-139.1
FREQ=	1.2500E+08	AMPL=	3.24E-01	20LOG=	-9.8	PHASE=	-152.8
FREQ=	1.3000E+08	AMPL=	3.76E-01	20LOG=	-8.5	PHASE=	-167.3
FREQ=	1.3500E+08	AMPL=	4.09E-01	20LOG=	-7.8	PHASE=	179.2
FREQ=	1.4000E+08	AMPL=	4.27E-01	20LOG=	-7.4	PHASE=	167.6
FREQ=	1.4500E+08	AMPL=	4.36E-01	20LOG=	-7.2	PHASE=	157.8
FREQ=	1.5000E+08	AMPL=	4.40E-01	20LOG=	-7.1	PHASE=	149.6

FIGURE 4 - VALUES ADJUSTED TO NEAREST RETMA VALUES

diode is sufficiently reverse biased to prevent half-wave conduction.

Implementing the resonant gate drive may take any of several forms. The resonant tank circuit may be merged with the oscillator, or it can be a varactor tuned Class B stage, [18] or, as in the present design, an independent resonant tank, shown in Figure 12.

To ensure symmetrical gate voltage in 180° anti-phase, if the local oscillator drive is asymmetrical, viz., fed by unbalanced coax, an unbalanced-to-balanced balun must be used (T1 in Figure 12), otherwise capacitive unbalance results with an attendant loss in mixer performance.

Table II offers an interesting comparison between a resonant-gate drive with a loaded tank Q of 14 and a conventional gate drive using a 50 to 100-Ω-100Ω transformer. The importance of a high tank Q is graphically portrayed in Figure 13. The full impact of a high gate voltage swing can be appreciated by using Equation 14. Here, as V_c (gate voltage) increases the intermodulation performance (IMD) also improves as we might intuitively expect. Calculated and measured results are shown in Figure 14 and demonstrate reasonable agreement. The difference may reflect problems encountered in measuring V_c as any probe will inadvertently load, or detune, the resonant tank even with the special care that was taken to compensate.

If we have the option to choose "high side" or "low side" injection -- viz., having the local-oscillator frequency above (high) or below (low) the signal frequency -- a closer inspection of Equation 14 should convince us to choose low-side injection.

Terminating Unwanted Frequencies

If our mixer is to be operated over a restricted frequency range where the local oscilator and signal frequencies can be manipulated, image-frequency filtering may be possible. Image-frequency filtering does affect performance. For high-side local-oscillator injection an elliptical-function low-pass filter, or for low-side injection a high-pass filter might offer worthwhile improvement. In either case, the filter offers a short-circuit reactance to the image frequency forcing the image to return once again for demodulation. The results of using a low-pass filter with the commutation mixer are known from our earlier examination of Figures 5 and 6.

The resonant-gate drive consisting of a high-Q tank offers adequate bypassing of the intermediate frequency and image frequency.

If the IF is narrow band, filtering may be possible by simply using a resonant LC network across the primary of the transformer. [19]

Design Techniques in Building the Commutation Mixer

The mixer was fabricated on a high-quality double-copper clad board (PCB) shown in Figure 15. An improvised socket held the S1890l. The signal and IF ports used Mini-Circuits, Inc., plastic T-case PF transformers. For the IF, the Mini-Circuits T4-1 (1:4); for the signal, the Mini-Circuits T1-1T (1:1) or T4-1 was used. The resonant tank was wound on a ¼-inch ceramic form with no slug. The unbalanced-to-balanced resonant tank drive used a T4-1. The schematic diagram, Figure 16, is for a commutation mixer with high-side injection, operating with an IF of 60 MHz.

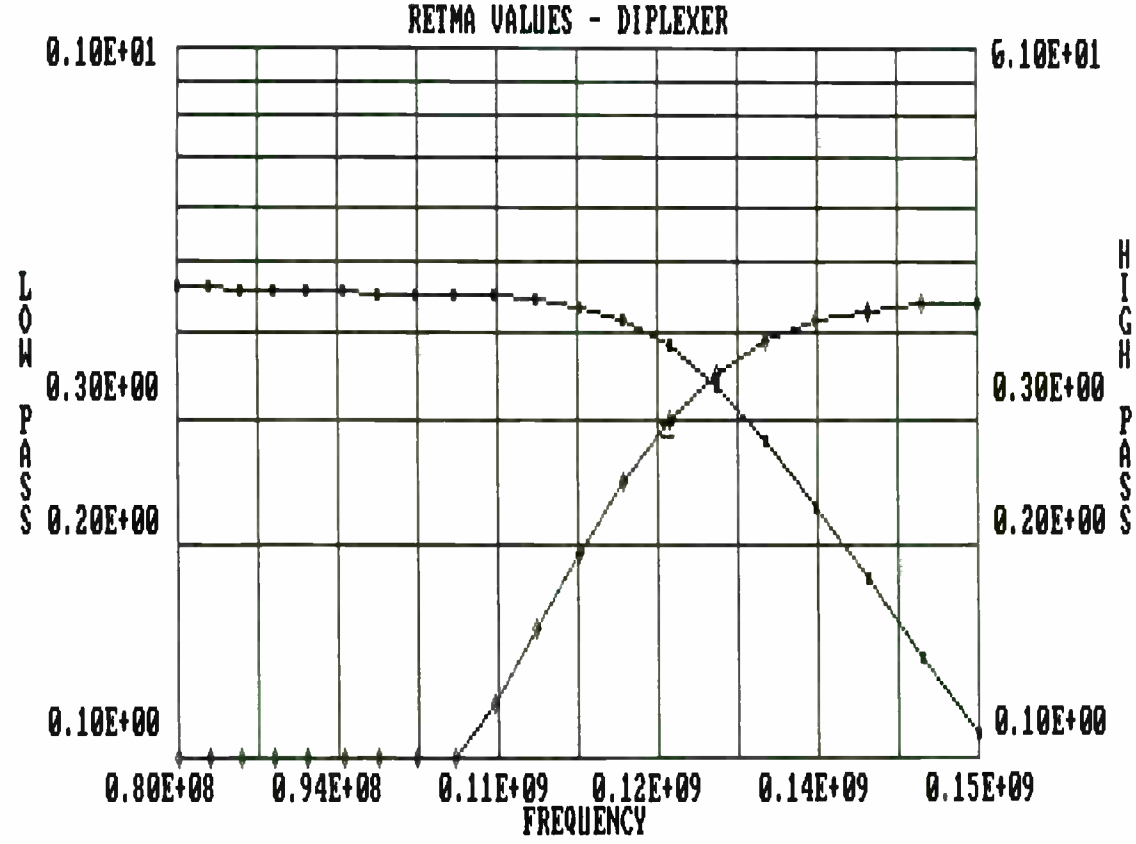

Figure 4(6)

The principle effort involved the design of the resonant-gate drive. This necessitated an accurate knowledge of the gate's total capacitive loading effect. To accomplish this a precision fixed capacitor (5 pF) was substituted for the Si8901 and at resonance it was a simple task to calculate the inductance of the resonant tank. Substituting the Si8901 made it again a simple task to determine the capacitive effect of the Si8901. Once known, a high-Q resonant tank can be quickly designed and implemented. To ensure good interport isolation, symmetry is important, so care is necessary in assembly to maintain mechanical symmetry, especially with the primary winding.

Performance of the Si8901 Commutation Mixer

The primary goal in developing a commutation double-balanced mixer is to achieve a high dynamic range. If this task can be accomplished with an attendant savings in power consumption, then the resulting mixer design should find wide application in HF receiver design.

The following tests were performed.

Conversion efficiency (loss)
Two-tone, 3rd-order Intercept Point
Compression level
Desensitization level
Noise Figure

Conversion loss and Intercept Point are directly dependent upon the magnitude of the local-oscillator power. The mixer's performance is offered in Figure 17, where the input intercept is plotted with conversion loss.

Both the compression and desensitization levels may appear to contradict reason. Heretofore, conventional diode-ring demodulators exhibiting compression and desensitization levels an order of magnitude below the local-oscillator power level. However, with a commutation MOSFET mixer, switching is not accomplished by the injection of loop current but by the application of gate voltage. At a local-oscillator power level of +17 dBm (50 mW), the 2 dB compression level and desensitization level was +30 dBm! The single-sideband HF noise figure of 7.95 dB was measured also at a local-oscillator power level of +17 dBm.

CONCLUSIONS

Achieving a high gate voltage to effect high-level switching by means of a resonant tank is not a handicap. Although one might at first label the mixer as narrow-band, in truth the mixer is wideband. For the majority of applications, the intermediate frequency is fixed, that is, narrow band. Consequently, to receive a wide spectrum of signal frequencies the local oscillator is tuned across a similar band. In modern technology this tuning can be accomplished by numerous methods. Likewise the resonant tank may take several forms. It can be part of the oscillator, or, as in Ref. (18), it can be a varactor-tuned driver electroncially tracking the local oscillator.

If the local-oscillator drive was processed to offer a more rectangular waveform, approaching the idealized square-wave, we might then anticipate even greater dynamic range as predicted by Equation 14.

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Single-Balanced	Double-Balanced
f_s	
$3f_s$	
$5f_s$	
f1 ± f2	f1 ± f2
f1 ± 3f2	f1 ± 3f2
f1 ± 5f2	f1 ± 5f2
2f1 ± f2	
2f1 ± 3f2	
3f1 ± f2	3f1 ± f2
3f1 ± 3f2	3f1 ± 3f2
4f1 ± f2	
5f1 ± f2	5f1 ± f2

A Comparison of Modulation Products in Single and Double Balanced Mixers to the 6th Order

TABLE I

SAW ACCELEROMETERS: INTEGRATION OF THICK AND THIN FILM TECHNOLOGIES

by
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INTRODUCTION

Surface Acoustic Wave (SAW) devices are now being used in many sensor applications[1-3] because of their inherent advantages (Figure 1). The ability to integrate the SAW delay lines with hybrid microelectronics to make compact, reliable units (Figure 2) and the requirement to obtain RF outputs directly proportional to the measurand (i.e., acceleration, pressure, vapor, etc.) have allowed this relatively new family of sensors to compete with other established sensor technologies such as capacitance and strain gauge type.

This paper describes how both thick and thin film processing technologies were combined to form a successful prototype SAW accelerometer intended for missile applications sensing ±50 Gs.

BASIC DESIGN AND OPERATION

The discussion on the basic design and operation of this accelerometer centers on its key sensing element, the SAW delay line. Since cost and size were not a major emphasis in this developmental program, a custom machined, two-tier, connectorized package (Figure 3) was designed to support and protect the SAW line and house the hybridized electronics.

Mechanical Design

Initially, two standard SAW materials were investigated; Y-Z lithium niobate and ST-X quartz. These materials were chosen for the following reasons:

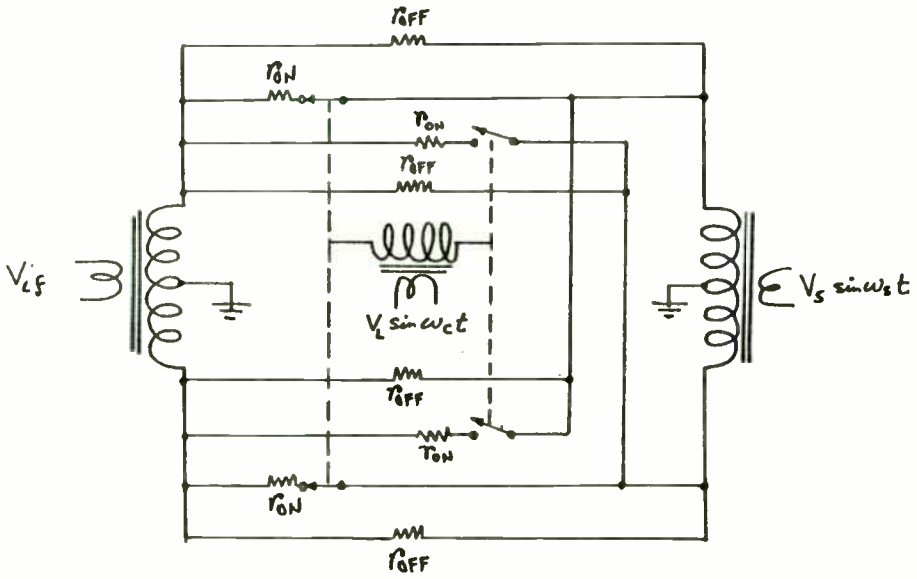
1. Historically they have been the most popular substrates used for SAW devices. $LiNbO_3$ is used for its high piezoelectric coupling and SiO_2 is used for its thermal stability.
2. Material constants for these particular crystalline cuts are well known, thus allowing the SAW velocity change due to strain to be predicted.
3. These materials have better mechanical properties than other candidate materials, leading to better production yields and a more rugged accelerometer.

The mechanical configurations investigated were those which were readily derivable from these standard SAW materials and those providing maximum strain at the surface of the SAW substrate. Mechanical analysis of several configurations was performed and resulted in how the SAW substrate velocity changed as a function of applied stress, mechanical dimensions, material constants, etc. This analysis concluded that the cantilever beam approach required the least force to achieve a given strain and hence SAW velocity change (Figure 4). The force ($F_\perp$) applied to the cantilever beam is provided primarily by the acceleration field acting upon a seismic mass attached to the beam's end. In this cantilever beam configuration the mechanical calculations for strain and the material constants demonstrated that ST-X quartz has nearly twice the sensitivity of lithium niobate, thus making quartz the material selected

Power in (mW)	NR Gate Voltage (V)	Res Gate Voltage (V)
10	0.20	5.4
20	0.29	7.7
30	0.33	9.4
60	0.44	13.3

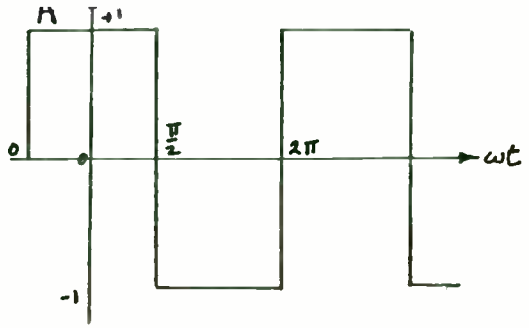
Comparison of a-c gate voltage versus local-oscillator drive between a non-resonant (NR) and resonant (Res) tank with a loaded Q of 14 (Freq. 150 Mhz)

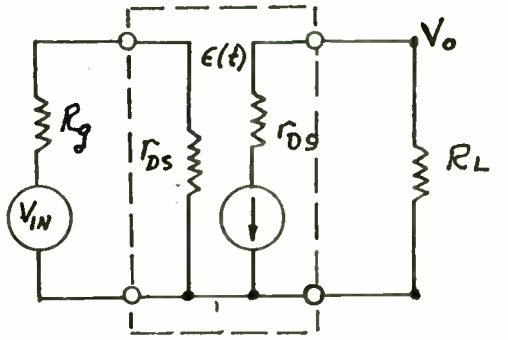
TABLE II



EQUIVALENT CIRCUIT OF COMMUTATION MIXER

FIGURE 1

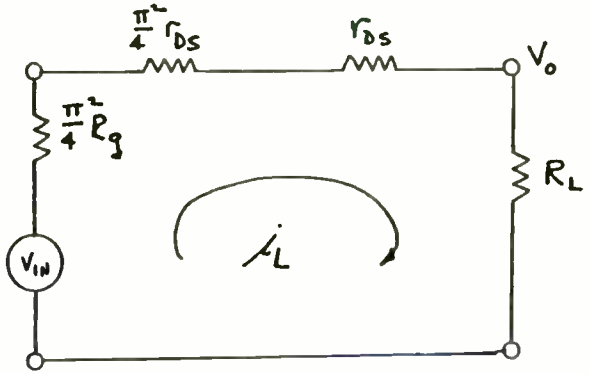




$$\epsilon(t) = \frac{4}{\pi^2}$$

DERIVATIVE EQUIVALENT CIRCUIT

FIGURE 2



THE POWER-LOOP CIRCUIT WITH ALL ELEMENTS EQUIVALENT, BASED ON THE TRANSFER FUNCTION, $\epsilon(t) = 4/\pi^2$

FIGURE 3

for the SAW accelerometer prototypes.

Electrical Design

The basic design used for the SAW accelerometer prototypes consisted of a single SAW oscillator (fo = 314 MHz) driving twin cantilevered SAW delay lines. One delay line is used as a reference and the other is stressed or "deformed" under acceleration by the seismic mass. The intent of this twin delay line configuration is to minimize any temperature effects between the two lines. The two outputs are fed to a phase detector to compare the relative phase shift due to a velocity change in the stressed substrate. The phase detector output is then amplified and used to produce both DC analog and RF outputs proportional to the applied acceleration force.

BASIC FABRICATION AND ASSEMBLY

The electronics circuitry for the accelerometer was fabricated as a thick film hybrid circuit on a 1" x 0.8"x .025" alumina substrate. The main electronics board contained a SAW oscillator, power divider, phase detector, amplifier section, and V-to-F circuit (Figure 5). The two delay lines and their tuning elements were mounted on a separate base plate and attached to the bottom of the package by screws (Figure 6).

PRELIMINARY TUNING

Prior to package assembly it was necessary to functionally adjust the reference SAW delay line to 90 degrees phase difference in relation to the deformable SAW delay line. This insured maximum sensitivity of the phase detector to any stress in the deformable cantilever. The package and baseplate fixtures were connected such that the outputs of the power divider were injected into both cantilevered SAW lines. The outputs of both the reference and deformable SAW lines were then fed back into the phase detector on the main electronics board. The DC amplifier output was then monitored and the reference cantilever was adjusted by means of locking screws on the seismic mass. When maximum amplifier output was obtained the reference cantilever screws were locked in place.

With the reference SAW line now held stationary, the deformable SAW line was manually deflected and the amplifier output checked. The result was approximately a one volt shift at full scale deflection.

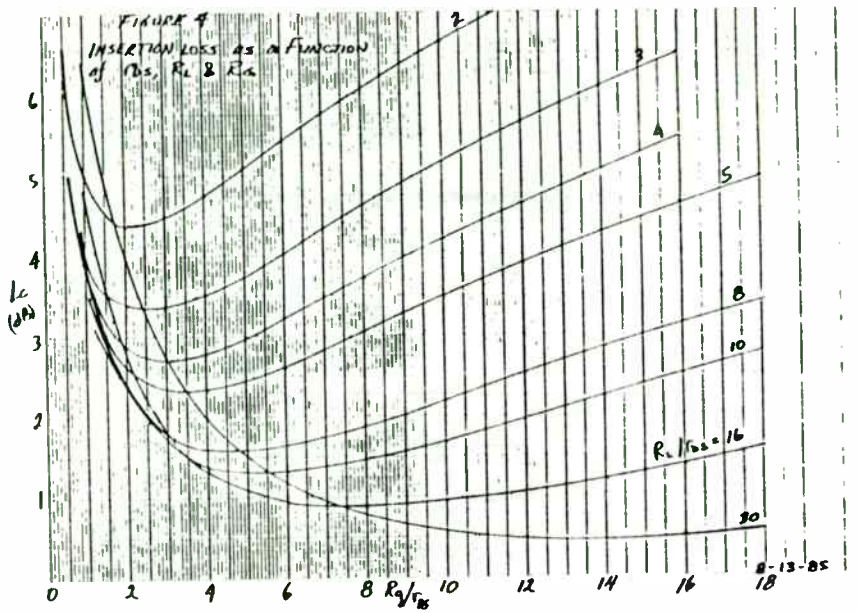
The R-C circuitry on the V-to-F section was now adjusted to give a stationary output difference frequency of 550 KHz ± 25 KHz. This was necessary due to the fact that, because of individual SAW characteristics, component tolerances, etc., the stationary amplifier output varied.

TESTING RESULTS

Four prototype devices were built and tested for the following parameters:

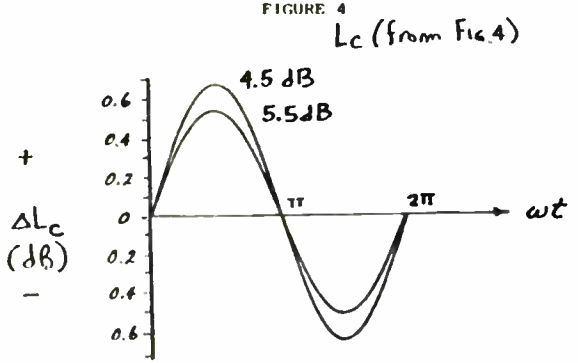
1. Linearity
2. Sensitivity
3. Hysteresis
4. Effects of temperature
5. Transverse Sensitivity

The basic procedure for testing the SAW accelerometers was to mount them onto a centrifuge and calculate the acceleration by converting RPM into Gs. The acceleration was incremented in steps of 5 Gs and the DC output voltage monitored and recorded for each acceleration point.



INSERTION LOSS AS A FUNCTION OF r_{DS}, R_L, & R_G

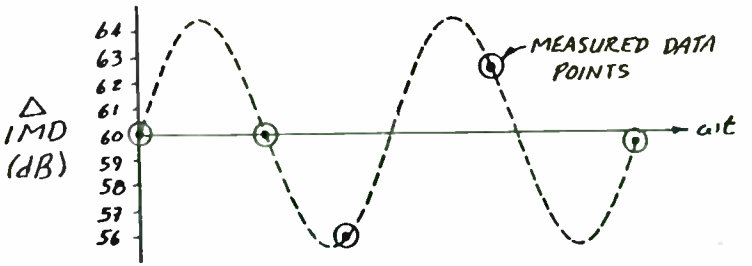
FIGURE 4



EFFECT OF IMAGE TERMINATION ON

CONVERSION LOSS

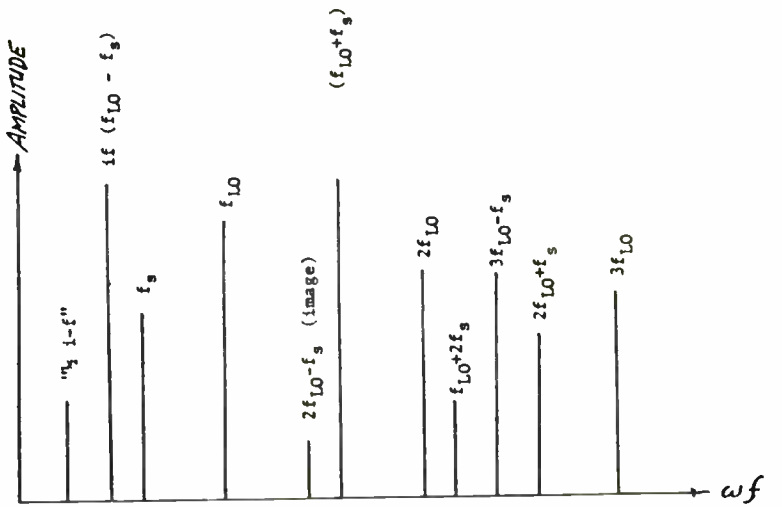
FIGURE 5



EFFECT OF IMAGE TERMINATION ON

3rd-ORDER DISTORTION

FIGURE 6



THE HARMONIC & SPURIOUS CONTENT

EXITING THE IF PORT OF THE

COMMUTATION MIXER

FIGURE 7

Linearity and Sensitivity

The SAW accelerometers were tested for the linearity and sensitivity at ambient, hot, and cold temperatures. The results of the ambient temperature runs on two units can be seen in Graph #1 entitled "SAW-DC Voltage vs. Acceleration". From this graph it can be seen that the two units displayed a very linear relationship between acceleration and output voltage. The sensitivities of both units differed from around the zero acceleration point to the acceleration extremes. See Table below.

Acceleration	SAW 2	SAW 3
50 Gs	2.6mV/G	5.2mV/G
0 Gs	6.6mV/G	7.8mV/G
-50 Gs	7.8mV/G	9.5mV/G

It must be noted that the cantilevered structures were designed to maximize +G deflection and limit -G travel to save package space.

Hysteresis

The hysteresis of the SAW accelerometer was found by measuring the DC output voltage while incrementing the acceleration from zero to +50 Gs and decrementing back to zero. This procedure was repeated for negative acceleration. A typical SAW hysteresis curve can be seen in Graph #2 "SAW Accelerometer HYSTERESIS". From this graph it can be seen that there is a minimal amount of lag and the accelerometers deviated from their initial measured value by a maximum of 5 mV and 11 mV respectively.

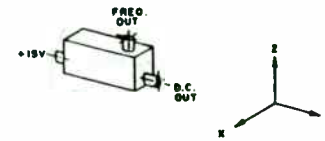
Effects of Temperature

The effects of temperature were measured by cooling or heating the SAW device and then placing the unit inside an insulated box and running the tests. Raising and lowering the temperature generally had the effect of raising and lowering the operating point. Raising and lowering the temperature also effected the sensitivity of the SAW units. Sensitivity increased to -9.46mV/G when cold (-25F) and decreased to -7.0mV/G when hot (150F). Sensitivity at ambient temperature is -7.89mV/G. This phenomenon is probably due more to semiconductor physics than the SAW temperature sensitivity. Saturation current through the phase detector diodes will increase with temperature and thereby reduce phase detection sensitivity. These effects can be compensated for with additional electronics.

NOTE: The operating point of the accelerometer at times shifted around irrespective of operating conditions. This explains why the hot curve is lower than the ambient curve in Graph #3 "SAW Accelerometer Temperature Effects". In general the operating point for this particular unit lowered with use.

Transverse Acceleration

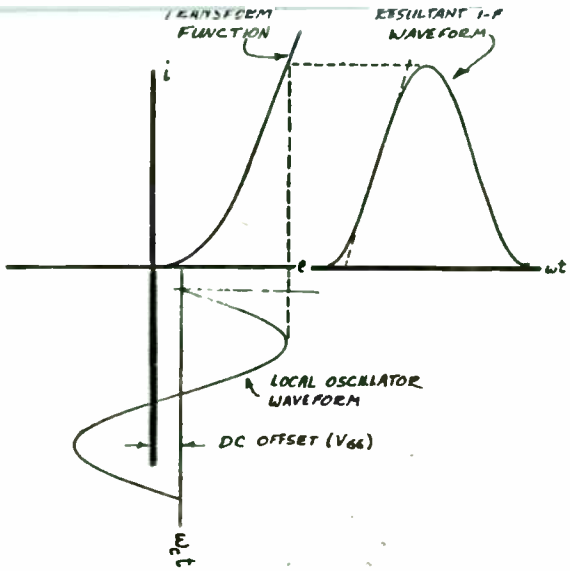
Transverse acceleration is a critical in missile applications because acceleration occurs in more than one axis as the missile maneuvers. However, transverse acceleration was found to have very little if no affect on the DC output voltage. See Table below.



X direction is axis of desired motion

Y direction acceleration has no affect at all

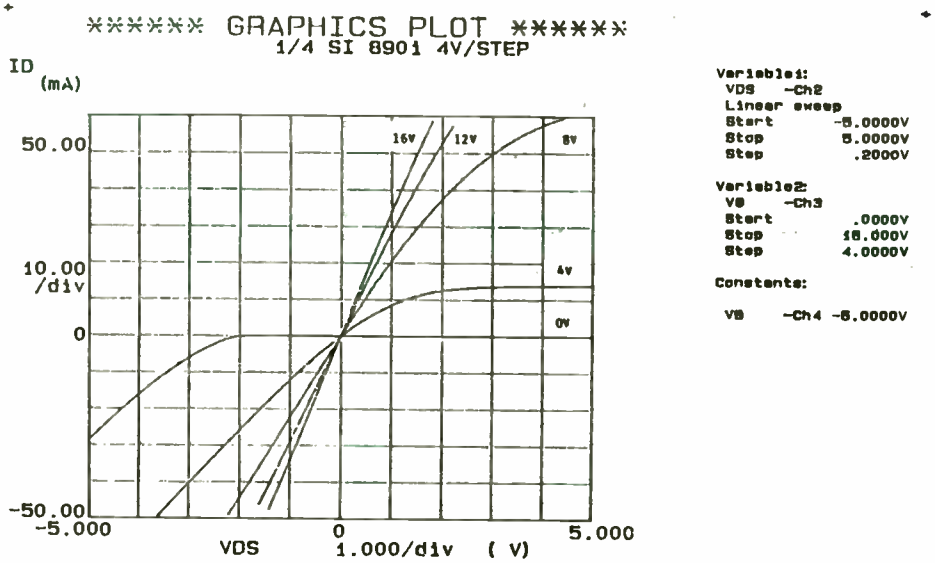
Z direction acceleration has 0.2mV/G sensitivity



EFFECT OF SINUSOIDAL LOCAL OSCILLATOR

WAVEFORM ON IF LINEARITY

FIGURE 8



Variable1:
VDS -Ch2
Linear sweep
Start -5.0000V
Stop 5.0000V
Step .2000V

Variable2:
VB -Ch3
Start .0000V
Stop 16.000V
Step 4.0000V

Constants:

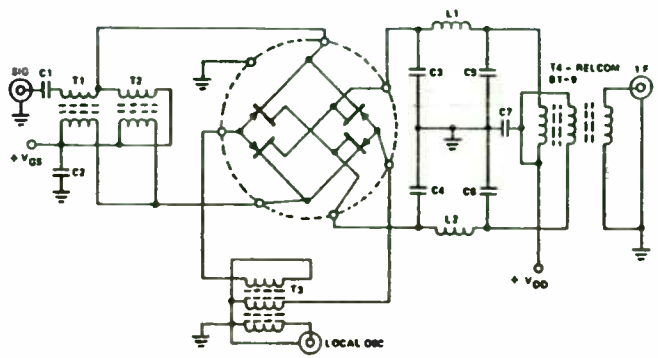
VB -Ch4 -6.0000V

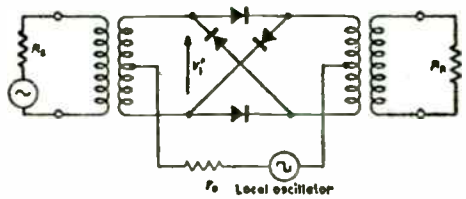
FIRST & THIRD QUADRANT I-E CHARACTERISTICS

SHOWING EFFECTS OF GATE VOLTAGE LEADING TO

LARGE SIGNAL OVERLOAD DISTORTION

FIGURE 9





LOCAL OSCILLATOR DRIVE USING

CONVENTIONAL BROADBAND TRANSFORMERS

FIGURE 10

Summary of Testing Results

The SAW accelerometers exhibited a reasonably linear relationship between output voltage and acceleration. The units did display some offset and sensitivity drift with temperature variations. The offset voltage increased with a temperature increase and sensitivity increased as temperature decreased. Transverse acceleration is not a problem and hysteresis effects also don't appear to be a problem but more testing is needed to confirm this. The most common problem encountered in testing the units was that the offsets were at times unpredictable and often took a long time to stabilize.

In general, the SAW accelerometers worked well for prototypes. There were problems encountered in the testing that pointed to the associated electronics and mechanical mounting. Several improvements to overcome these problems will be addressed in the next phase of development.

CONCLUSION

This development program on SAW accelerometers proved very successful. The acceleration versus output voltage data was linear and reproducible to ±50 Gs. Size and cost reductions are being pursued in a follow-on developmental program which will provide a low profile, surface mountable package.

REFERENCES

[1] "A Surface Acoustic Wave Gas Detector", A. Bryant et.al., 1981 Ultrasonics Symposium Proceedings, pp 171-174.

[2] "Cantilever-Beamed SAW Accelerometers", P. L. Meunier and P. Hartemann, 1982 Ultrasonics Symposium Proceedings, pp 299-302.

[3] "Temperature Sensor Using SAW Delay Line", D. Hauden et.al., 1981 Ultrasonics Symposium Proceedings, pp 148-151.

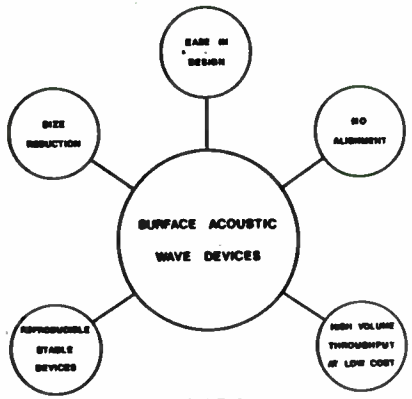


FIGURE 1
Reasons to Use SAW Devices

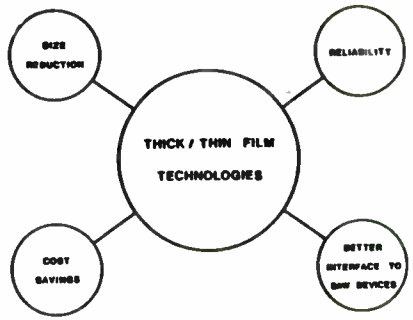
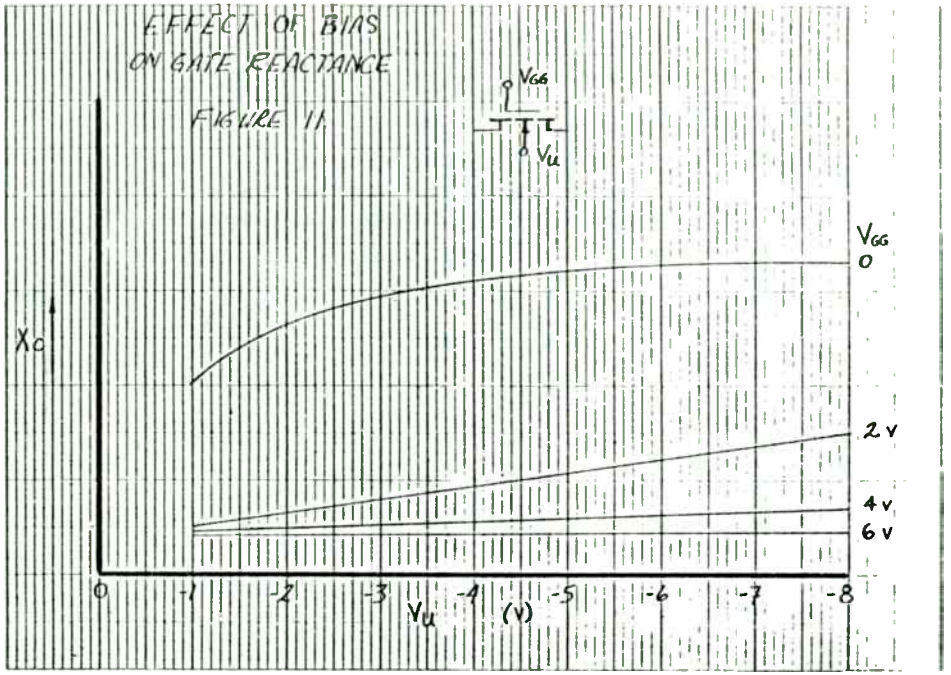
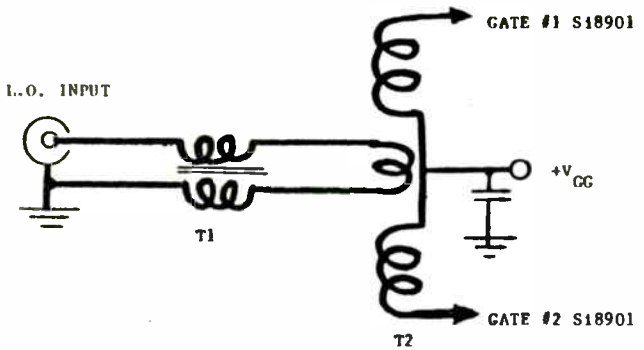


FIGURE 2
Reasons to Use Thick/Thin
Technologies with SAW Devices

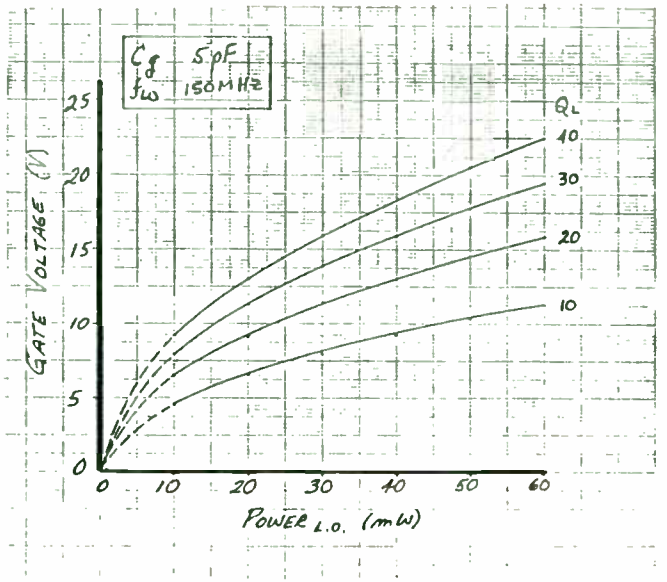


EFFECT OF BIAS AND SUBSTRATE VOLTAGE ON
GATE REACTANCE
FIGURE 11



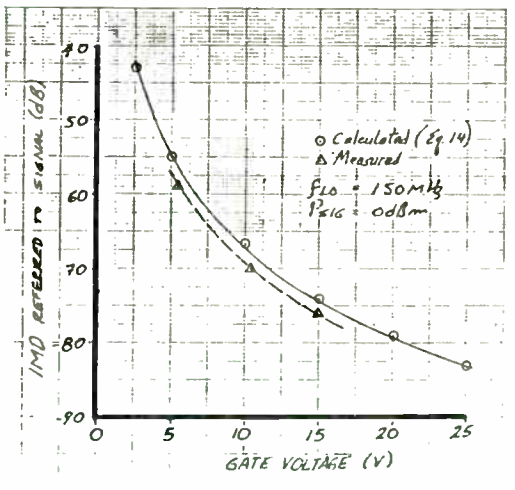
RESONANT-GATE DRIVE TRANSFORMER, T2, IS TUNED
TO RESONATE WITH C_{GG} OF S18901

FIGURE 12



INFLUENCE OF LOADED Q ON GATE
VOLTAGE VERSUS L.O. POWER

FIGURE 13



EFFECTS OF GATE VOLTAGE ON
INTERMODULATION DISTORTION

FIGURE 14

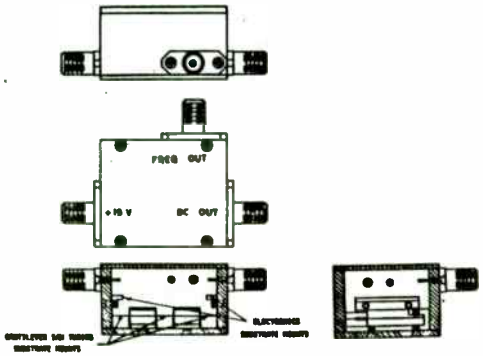


FIGURE 3
SAW Accelerometer
Package Assembly

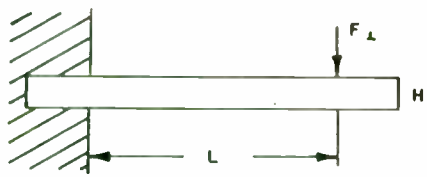


FIGURE 4
Cantilever Beam

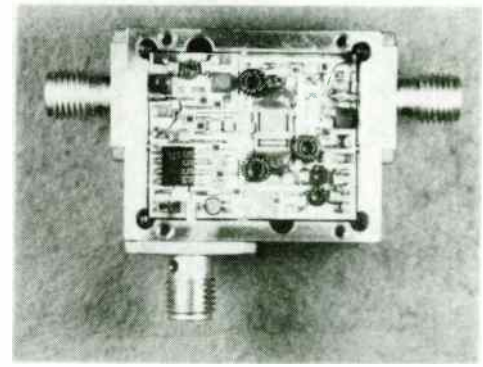


FIGURE 5
Electronics Substrate

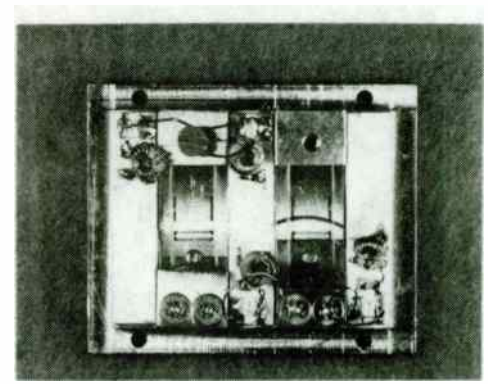
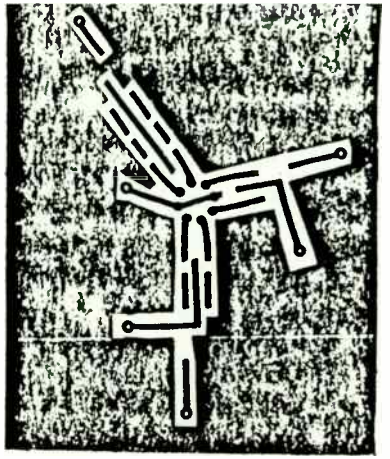


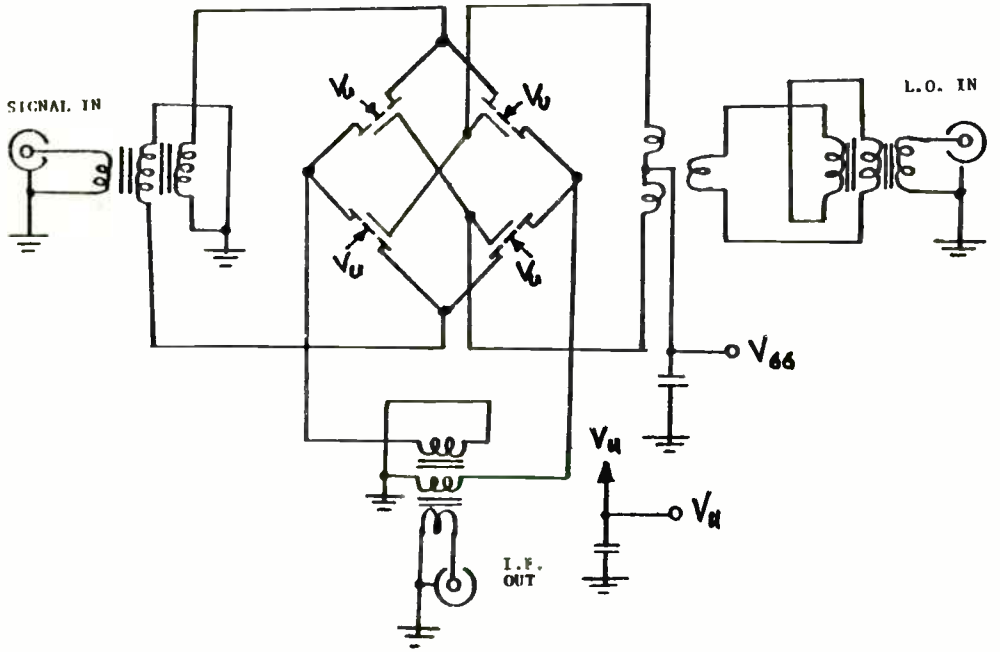
FIGURE 6
Cantilever SAW Substrate
with Tuning Components



MASK LAYOUT -- PRINTED CIRCUIT BOARD

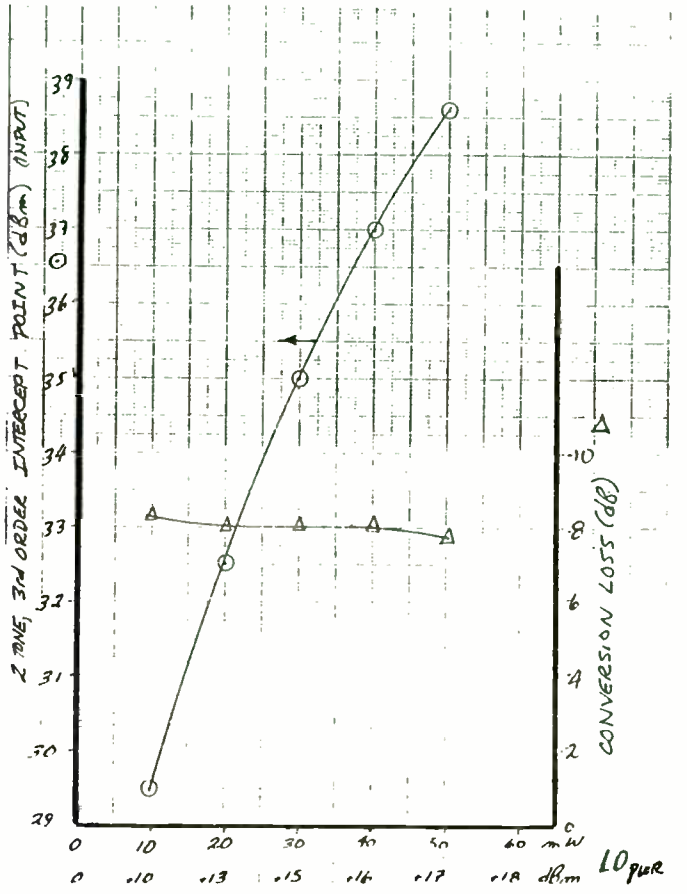
PROTOTYPE BALANCED MIXER

FIGURE 15



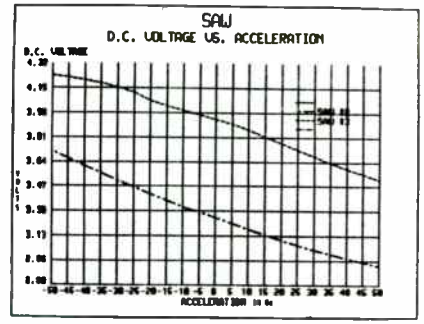
SCHEMATIC - COMMUTATION DOUBLE-BALANCED MIXER

FIGURE 16

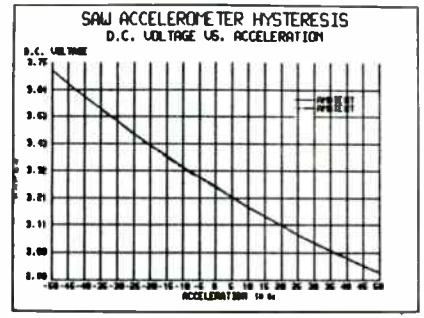


INPUT INTERCEPT POINT & CONVERSION LOSS

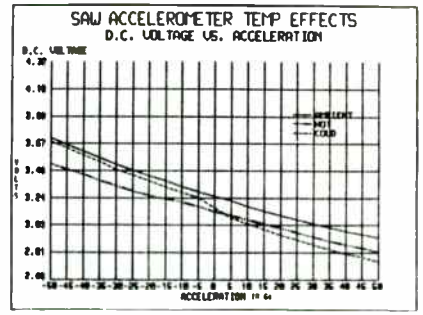
FIGURE 17



GRAPH 1



GRAPH 2



GRAPH 3

IMPROVE SYNTHESIZED TRANSCEIVER PERFORMANCE AND RELIABILITY BY SIMPLE SCREENING OF THE VCO ACTIVE DEVICE

ABSTRACT:

This article describes the effect of 1/f noise from high frequency bipolar junction transistors on the performance of a synthesized transceiver; and it offers an explanation for the origin of the noise together with a simple screening technique to improve the transceiver performance and reliability.

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Introduction:

A basic element of frequency synthesized transceivers is the phase-lock loop circuit in which the output of a voltage-controlled oscillator (VCO) is constantly compared with the frequency of a reference crystal controlled oscillator. Synthesized transceiver performance is mostly based on the choice of design parameters for the phase-lock loop circuit. A compromise in loop bandwidth will optimize the desired switching speed with respect to the specified spurious output levels. The phase noise sources in the phase-lock loop [1, 2] are responsible for the spectral purity of the transceiver. The close-in phase noise will affect the residual FM hum and noise performance as well as the transceiver adjacent channel selectivity specifications.

To achieve good close-in phase noise, it is necessary to maximize the resonator's loaded Q and its available output power while choosing an active device with a low noise figure and a low 1/f noise contribution. This article describes the effect of 1/f noise from high frequency bipolar junction transistors on the performance of a synthesized transceiver; and it offers an explanation for the origin of the noise together with a simple screening technique to improve the transceiver performance and reliability.

Cause and Effect of 1/f Transistor Noise:

The major cause of 1/f noise in bipolar transistors has been traceable to surface properties. Surface contamination or defects can degrade 1/f noise performance and transistor reliability by creating early failures in the field.[3]

The 1/f transistor noise caused a degradation in the VCO phase noise in the synthesized transceiver; distinctly affecting the residual FM hum and noise and the

CHOOSING THE RIGHT CRYSTAL AND OSCILLATOR FOR THE APPLICATION

by

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Some of the considerations which go into a decision on the choice and design of crystals and crystal oscillators are listed below:

1. Fundamental versus overtone mode crystal.
2. Parallel mode versus series mode.
3. VHF crystal versus multiplier chain.
4. Uncompensated versus TCXO or OCXO.
5. Trimable versus no trim adjustment.
6. Solder sealed package versus hybrid.
7. Voltage control required.
8. Stringent short term stability requirements.
9. Tight ageing requirements.
10. Start-up time.
11. Radiation requirements.
12. Shock and vibration rquirements.
13. Low current (battery operated).
14. Low parts count. Gate Oscillator.

In order to organize some of the above considerations, this paper arbitrarily begins with a 20 MHz , fundamental mode crystal in an HC-18 holder, to be used in an oscillator driving a receiver local oscillator chain to 400 MHz.
The characteristics of this crystal and its circuit are described and some of the options and considerations of the list are compared to this 20 MHz example.

FREQUENCY STABILITY

Assume that the oscillator has a temperature stability of $\pm$40 PPM (parts per million) over the temperature range of -40°C to +85°C. To this must be added an ageing factor. One can conservatively assume 2 PPM ageing the 1st year of operation and a life time ageing factor of 4PPM. Using these assumptions, the worst case frequency error will be 40 + 4 or 44 PPM.

In Hertz;

$$20 * 10^{6} * 44 * 10^{-6} = 880 \text{ Hz},$$

and at the end of the x20 multiplier chain

$$20 \times 880 = 17{,}600 \text{ Hz}.$$

This frequency error would be tolerable if this fictitious local oscillator was part of a receiver with a 200 kHz I.F. bandwidth. If, however, the bandwidth were only 2 kHz,a 17600 Hz error in the local oscillator would be excessive. The narrow band assumption will be made in order to see where it leads the

adjacent channel selectivity performance. The 1/f transistor noise was first verified by the -9dB per octave slope of the single-sideband phase noise spectral density, L(fm) plot.[4] The high frequency bipolar transistor noise was then amplified in a low noise amplifier and recorded on a low frequency spectrum analyzer.

The transistors with excessive 1/f noise showed a relatively low DC beta and a large difference in the absolute value of this parameter at different collector currents. Thus, a simple characterization of the DC beta of the VCO active device can improve synthesized transceiver performance and reliability.

Transceiver Performance Background:

The transceiver includes a transmitter and a receiver section coupled to the frequency synthesizer which generates the appropriate injection signals to allow the transmission and reception of the carrier frequency.

The transmitter residual FM hum and noise specification is a measurement of the signal-to-noise quality of the transmitter within a specified bandwidth. Specifically, it denotes the ratio of residual frequency modulation to standard test modulation measured on a test receiver. In a narrowband system the standard test modulation is 60% of the 5 kHz maximum system deviation, and the test receiver bandwidth is in the audio voice pass-band range of 300 to 3000 Hz.

The synthesizer characteristics play a major role in determining the receiver selectivity specification; in particular, the close-in phase noise. Receiver selectivity is a measure of channel protection against undesirable signals close to the receiver carrier frequency. This is typically measured at the adjacent channel frequency, and it serves as a figure of merit for different types of receivers.

The transmitter sideband noise is also directly influenced by the phase noise at the output of the voltage controlled oscillator which serves as the injection frequency for the transmitter section.

Transceiver Degradation Due To 1/f Noise:

The residual FM hum and noise level of the VCO varied in excess of 20 dB from a maximum measurement of -36 dB. (ratio in dB of the test modulated audio to the residual noise audio level). The inconsistent VCO hum and noise levels were traced to the 1/f noise of the active device in the oscillator circuit.

The spectral response of the voltage controlled oscillator was measured using a double balance mixer as a phase detector in a narrow bandwidth loop to maintain phase quadrature with the reference source.[5] This setup was capable of measuring better than -140 dB/Hz from the reference source. A plot of the spectral density response for two different bipolar transistors from the same generic lot measured on the same VCO is shown in Figure 1.

The difference shown in the spectral density plot is due to the higher 1/f transistor noise. The characteristic -9 dB per octave slope is clearly shown on the top trace of the plot, while the spectral density slope for the good device (bottom trace) shows the -6 dB per octave normally associated with the white FM noise.

The adjacent channel receiver selectivity, 25 kHz from the carrier frequency, was also degraded by 5.5 dB for the measurements taken with the samples outlined on Figure 1. After tracing the transceiver degradations to the active device of the oscillator circuit, the high frequency bipolar transistor was fully characterized.

oscillator design. The maximum error must now be restricted to about 200 Hz, or

$$\Delta f, \text{ PPM} = 200/400 = 0.5 \text{ PPM}$$

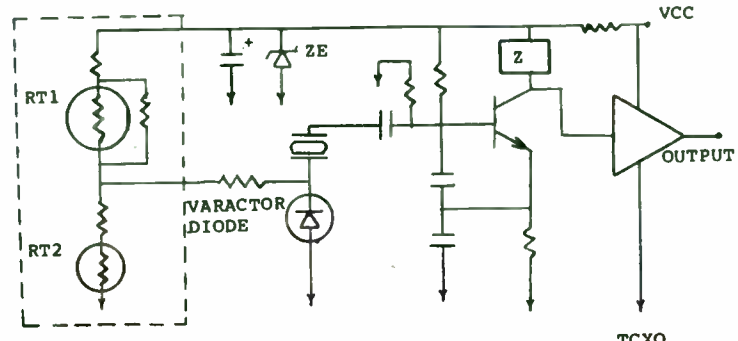
This new requirement forces the design to either a much more stable crystal oscillator, or to a system in which the oscillator is locked to a stable master reference. These two approaches will be considered next.

TCXO's and OCXO's

(Temperature Compensated Crystal Oscillator and Oven Controlled Crystal Oscillators)

Before considering the two options of TCXO and OCXO, the questions of ageing and setability must be addressed. If the receiver must operate without adjustment throughout its life, then ageing will probably determine the quality of crystal oscillator required (and therefore the price, size and D.C. power). If the frequency of the oscillator can be corrected by electrical or mechanical adjustment to remove frequency error due to ageing, the frequency accuracy will be dominated by temperature rather than age. TCXO's and OCXO's will be considered with this assumption.

Briefly, a TCXO corrects the crystal frequency versus temperature characteristic by means of a compensation network which applies a correction voltage to a varicap diode in series with the crystal. An OCXO addresses the problem by controlling the temperature at the crystal with a miniature oven. Simplified schematics of a typical TCXO and OCXO are shown in Figure 1.



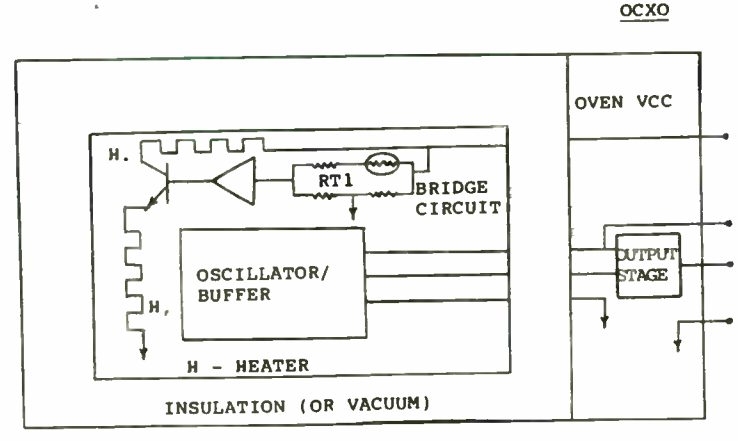


Figure 1, Simplified TCXO and OCXO

Bipolar Transistor Characterization:

The $1/f$ transistor noise was amplified and recorded on a low frequency spectrum analyzer. An audio amplifier was built with the high frequency bipolar transistor to amplify its own internal noise, and its output was passed through two additional stages of low-noise operational amplifiers. An overall gain of 100 dB was obtained from these amplification stages which served to drive the low frequency spectrum analyzer.

The noise spectral density for several transistors is shown in Figure 2. These pictures illustrate the different noise patterns observed.

The VCO residual FM hum and noise was measured for several transistors, then the spectral density was recorded on the low frequency spectrum analyzer, and finally the DC beta at the operating collector current (5mA) was measured for each device. A graph illustrating the correlation among these variables is shown in Figure 3.

The noise voltage at 1 kHz versus beta graph (Figure 3) shows a strong correlation of the high noise bipolar transistors responsible for the poor hum and noise levels to the low DC beta values recorded. In particular, transistor noise levels below $3nV\sqrt{Hz}$ at 1 kHz were found to correspond to VCO hum and noise levels lower than -52 dB.

However, since the residual FM hum and noise is measured in the audio voice pass-band range rather than at a specific frequency, a more accurate means of measurement was developed. This consisted of a noise test system whose output was a DC voltage level resulting from rectifying and integrating the $1/f$ noise in the specified audio bandwidth. A block diagram of the new noise test system is shown in Figure 4.

The amplified transistor noise was band limited from 300 to 3000 Hz with a 750 µsec preemphasis filter, processed through a full wave rectifier and integrated over a seven second period. The result of the integration was a DC voltage level proportional to the $1/f$ transistor noise. Figure 5 shows the relation of the rectified band limited noise voltage to the measured hum and noise levels. This graph also correlates an average DC noise voltage threshold limit of 0.5 Vdc to a VCO hum and noise acceptable level of -51 ± 1 dB.

Furthermore, Figure 6 shows the more accurate relationship of the rectified DC noise voltage to the hum and noise measurement and the oscillator transistor DC beta. This graph shows that the majority of the transistors with DC betas higher than 90 at 5 mA collector currents (VCE = 5V) had good VCO hum and noise performance. Further tests on a larger number of the same generic type transistors have shown a similar correlation (Figure 7).

Moreover, data at different collector currents was also taken, specifically at 5 mA and 10 µA. This data showed that the transistors with high noise levels demonstrated a large difference in these two collector currents. Refer to Figure 8.

Separate batches of transistors from different lots were specifically tested for noise, DC beta and the beta difference at different collector currents. In general, all transistors with betas higher than 90 showed low noise voltage levels and fairly close DC beta readings at the two collector currents mentioned. One batch of the high beta transistors (ßave = 130) showed high average noise voltage levels, but a large difference in DC betas at these two collector currents also was characteristic of this batch of transistors (beta difference was greater than 60).

The new specification of .5 PPM puts the requirement somewhere in the gray area between TCXO's and OCXO's. Low cost, commercial TCXO's typically meet ±1 PPM over 0°C to 50° The example oscillator's specification and temperature range puts the design near the border of the best that can be done with a TCXO, and consequently it would be a costly unit. OCXO's easily provide stabilities of $\pm 1 \times 10^{-8}$ over the required temperature range, and provide ageing rates less than 1×10^{-9} per day.

However, ovenized units are larger, heavier, and consume much more power than non-oven types. Representative specifications are shown in Table 1. Notice that some compromises may have to be made between requirements, performance, and price.

PHASE LOCKED SYSTEM

As an alternative, assume that this system already contains a stable master oscillator at 5 MHz. The basic crystal oscillator can then be locked to this master using a phase locked loop. Figure 2 illustrates the circuitry involved. Notice that a varactor in series with the crystal has been added in order to be able to pull (frequency shift) the frequency to exactly four times the reference 5 MHz.

Some notes concerning phase locking a crystal oscillator are appropriate.

1. The gain constant of a crystal controlled oscillator, KO, in Hertz per volt, is typically three to four orders of magnitude

TABLE 1 -- TYPICAL OCXO AND TCXO

SPECIFICATION	OCXO	TCXO
Frequency	5 or 10 MHz	5 to 50 MHz
Output Level	1 Vrms into 50 ohms	sinewave, TTL, or CMOS
Harmonic Distortion	-40 dBc	-20 dBc
Frequency Adjustment	+2.5 PPM minimum coarse mechanical. ±2x10E-6 fine ±1 PPM voltage control	±2x10E-6 minimum
Input Voltage	+ 12 V.D.C., ±10%	+ 12 V.D.C., ±5%
Frequency Stability vs Input Voltage	±3x10E-9 for ±10%	±2x10E-7 for ±5%
Frequency Stability vs Load	±1x10E-9 for ±10%	±2x10E-7 for ± 2:1 VSWR
Frequency Stability vs Temperature	±5x10E-9 -20°C to +75°C	±5x10E-7 -20°C to +60°C
Warm-Up Time	±1x10E-7 in 15 mins ±1x10E-8 in 20 mins	< 1 second
Aging Rate	1x10E-9/24 hours	1x10E-8/24 hours
Short Term Stability	3x10E-11 r.m.s Tau = 1 sec	1x10E-9 r.m.s Tau = 1 sec
Input Current	340ma. at turn-on 135ma. at 25°C 225ma. at -20°C	15 ma.
Size	2" x 2" x 4"	1" x 2" x 0.5"

1/f Noise Correlation To Surface Effects:

The major cause of 1/f noise in semiconductor devices is traceable to surface properties of the materials. The generation and recombination of carriers in the surface energy states and the density of surface states are important contributing factors. The 1/f noise has decreased with improved surface treatments in manufacturing, but even the interface between the silicon surface and the grown oxide passivation can create 1/f noise sources.[3]

Three distinct sources of low-frequency noise in bipolar junction transistors have been reported in the literature:[6]

1. A 1/f noise source associated with the surface of the emitter-base junction,
2. A 1/f noise source associated with the active base region of the transistor, and
3. Anomolous burst noise associated with the forward-biased emitter-base junction.

The noise spectral density of the transistors shown in Figure 2 correlates to these reported findings.

A good NPN high frequency transistor is designed with a narrow base width to reduce the transit time of the minority carriers, and with small emitter and collector areas to reduce junction capacitance.[7] A common fabrication technique uses interdigitated (emitter-base) geometries to increase the useful emitter edge length while keeping the overall emitter area to a minimum. This technique maximizes the perimeter-to-area ratio so that most of the emitter current will pass through the periphery, avoiding the large series resistance of the extremely thin base region.

Thus, the increased amount of current flow through the surface junction periphery tends to make the high frequency transistor more susceptible to surface defects. In contrast, low frequency (audio) transistors tend to have lower 1/f noise because their emitter geometries are designed to minimize the perimeter-to-area ratio so that more of the emitter current will avoid the periphery.

1/f Noise Correlation to DC Beta:

The basic operation of the NPN bipolar transistor consists of the injection of electrons from the emitter as minority carriers into the base region. Through the diffusion process they are collected at the collector region. The design objective for an efficient transistor is to match the number of electrons arriving at the collector to those being injected by the emitter. However, because of the electron-hole-pair (EHP) recombination at the base through the bulk and the surface, a 100 percent efficiency is never achieved. The holes required for the EHP recombination are supplied by the base current. In addition, the hole current that flows across the base to the emitter junction is also supplied by the base current.

The narrow base region width requirement minimizes the EHP recombination at the bulk, while recombination at the surface is best treated with careful and clean processing steps. Some of the Si-SiO_2 surface charge mechanisms reported are:[8]

1. Space charge within the oxide due to mobile contaminant ions (such as sodium),
2. Energy "traps" due to ionizing irradiation of the silicon sample,
3. Fast surface states which occur because of disruption of the periodicity of the lattice at the surface, and
4. Fixed surface state charge, Qss.

Since the DC beta (base to collector current amplification factor) is the ratio of collector

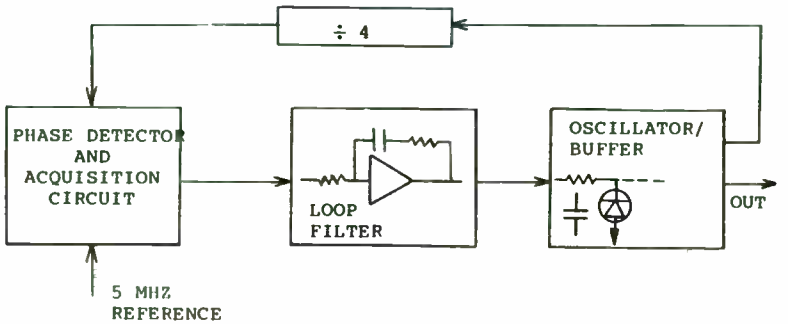


Figure 2, Phase Locking

less than that for a VCO (voltage controlled oscillator). The 20 MHz example would have an average KO of 500 Hz per volt.

2. The loop bandwidth for a phase locked loop using a crystal controlled oscillator is typically 10 to 200 Hz. Very much narrower bandwidths may cause loop phase jitter problems. Wider bandwidths are limited by frequency response roll-off caused by the narrow band nature of the oscillator.

3. The crystal oscillator must be capable of being pulled, or slewed, by an amount equal to its' temperature and ageing frequency error. This assumes that the master oscillator drift is negligible. The TCXO and the phase locked oscillator both require electronic tuning, by means of a varactor diode, or varicap. It is appropriate to discuss varactor tuning in more detail, before discussing overtone crystal oscillators because overtones have very limited "pullability."

VCXO (VOLTAGE CONTROLLED CRYSTAL OSCILLATOR

The equivalent circuit for a crystal is shown in Figure 3.

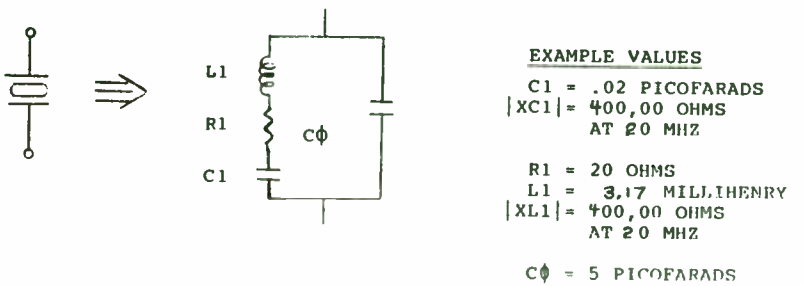


Figure 3, CRYSTAL EQUIVALENT CIRCUIT

L1, C1 and R1 represent the piezoelectric coupled mechanical resonator characteristics. CO is the capacitor formed by the crystal electrodes. Typical values for the 20 MHz crystal are shown. When the crystal is part of a complete circuit,as shown in Figure 4, oscillation occurs at a frequency above F1, where the crystal series arm presents a net inductive reactance, resonant with the capacitors and inductors in the circuit.

current to base current, the EHP recombination mechanism is a major contributor to this amplification factor. Consistently, for a given emitter current, if there is additional recombination due to surface effects, a larger number of electrons will recombine with the holes at the base and surface, decreasing the collector current and dropping the DC beta.

The surface effects and $1/f$ noise on high beta devices tend to be less noticeable because of the larger collector currents, but severe $1/f$ noise in high beta devices could still degrade the transceiver performance. For this reason, the difference in DC betas at separate collector currents became a second screening mechanism. A large beta roll-off at the low collector current of 10 μA, compared to the operating collector current of 5 mA, has been observed on devices with high $1/f$ noise, whereas normal devices have exhibited a minor beta roll-off (a difference of 10-20) due to the smaller number of electrons available for the EHP recombination.

In general, transistors with a high DC beta at low collector currents did not exhibit excessive $1/f$ noise.

Excessive $1/f$ Noise - A Reliability Predictor:

Correlation exists between high values of $1/f$ noise and poor reliability. It has been reported in reference 3 that artificial aging experiments have correlated excessive $1/f$ noise with the probability of early failure. The artificial aging experiments have noted that a large increase in $1/f$ noise occurs just prior to device failure, and units with low initial values of noise have demonstrated a longer life under these artificial conditions.

In a separate noise testing study for reliability screening[9], defective devices from tested samples showed abnormally high noise levels compared to the majority of good samples. The study concluded that defective samples can be identified and rejected using noise testing methodology based on $1/f$ noise.

In addition to the surface effect mechanisms covered, excessive $1/f$ noise may be the result of defective contacts, fractures or irregularities at the emitter-base junction which could also cause an early transistor failure. Early screening of the excessive $1/f$ noise devices will improve the reliability of the circuit and hence the system in which they will operate, in our case, the synthesized transceiver.

Conclusion:

Excessive $1/f$ noise in the active device of the VCO was shown to degrade the performance of the synthesized transceiver. Spectral purity, transmitter residual FM hum and noise, and receiver selectivity were degraded by the transistors with $1/f$ noise problems.

Noise testing on a large sample of high frequency bipolar transistors from different manufacturing lots showed a strong correlation for low noise transistors to high DC beta samples and especially at low collector currents.

Therefore, a simple screening of the VCO active device for high DC beta and a small difference in this parameter at the two specified collector currents could improve the synthesized transceiver performance and reliability.

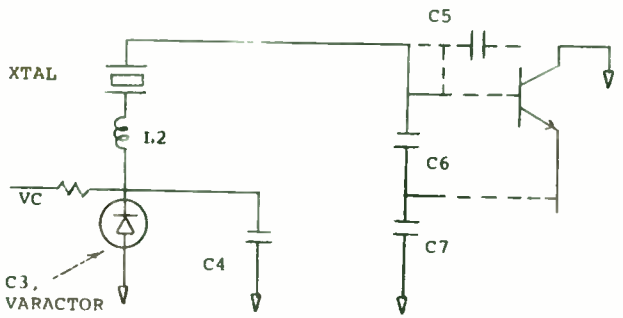


Figure 4, CRYSTAL AND CIRCUIT

The resonant frequency of the complete circuit can be calculated for any particular set of values by writing the appropriate equations for the resonant frequency and solving. This is conveniently done on a computer. Seven cases have been calculated and presented in Table 2 for typical circuit values.

In Table 2 the values of C1, C4, C6/C7, L2 and the varactor parameters (C3) are varied to show the effect on frequency pulling and linearity. A control voltage range of 1 volt to 10 volts is assumed. The frequency data is listed as; (1) PPM away from crystal series arm resonance, (2) the 1 V to 10 V frequency delta, (3) The frequency voltage sensitivity in PPM per volt, at the ends of the range.

In case 1, the difference in sensitivity at 1 V and 10 V is extreme. This results from the varactor capacity-voltage characteristic and from the loss of sensitivitiy as the crystal is pulled further from resonance. Case 2 is like Case 1 except that C1 has been halved. It is seen that the delta F is also reduced by 2, showing the direct dependence of "pullability" on C1. This is discussed in the section on overtone operation. Notice that the difference in 1 V to 10 V sensitivity is not as extreme in case 2 because the crystal is not pulled as far from series resonance. Case 3 shows that C4 reduces pulling and degrades linearity.

In Case 4 the varactor 4 volt value is changed from 30 picofarads to 15 picofarads, resulting in greater pullability and better linearity. Cases 5, 6, and 7 use a hyperabrupt varactor (gamma = .8) instead of the abrupt junction one. This yields improvement in pulling and linearity. Finally, Case 7 shows that the addition of a three microhenry series inductor (L2) further increases pulling. One note of caution. Reducing the varactor capacity results in an increase of the circuit parallel loss. In Case 6, for example, unless the crystal resistance is suitably low, the circuit may stop oscillating at 10 volts.*

* This topic is addressed in the paper "Maximizing Crystal Oscillator Frequency Stability" Session A-2, r.f. expo 86.

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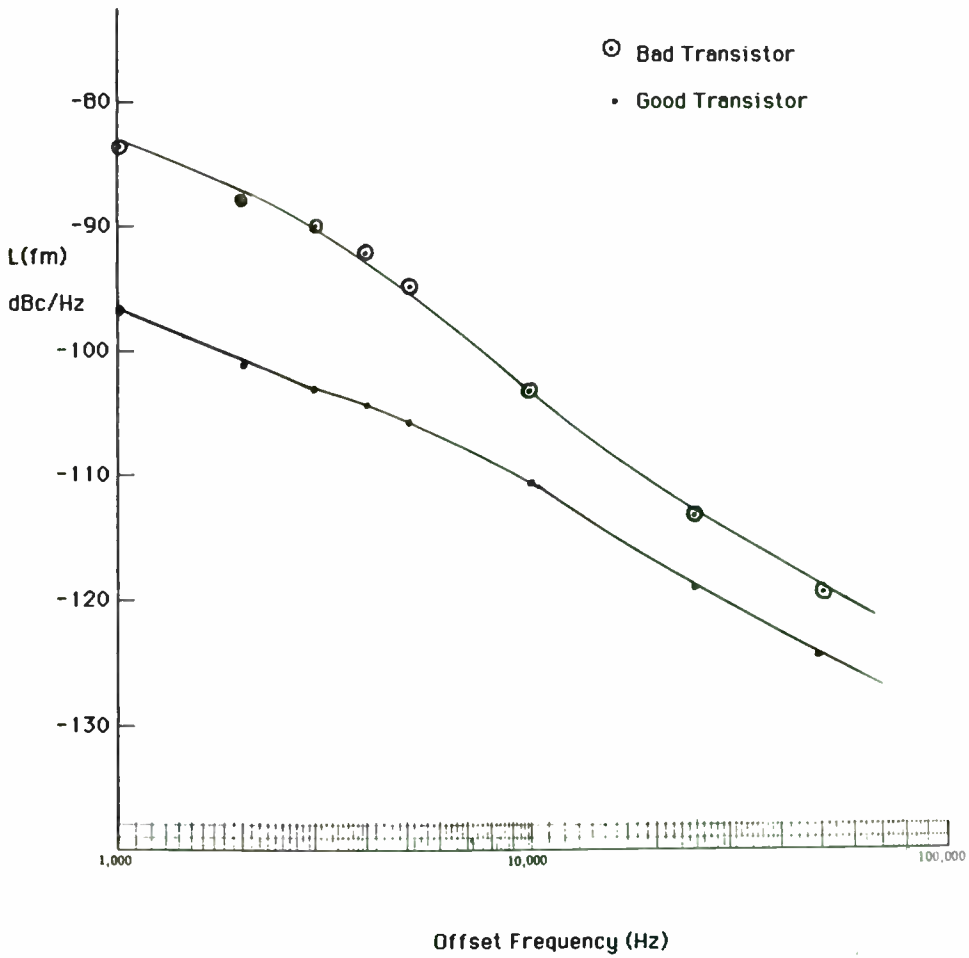
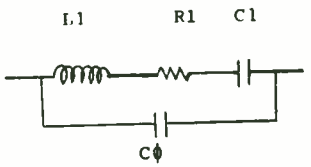
Figure 1 : Single Sideband Phase Noise 1Hz Bandwidth vs. Carrier Frequency Offset



THE OVERTONE CRYSTAL AND OSCILLATOR

It might be asked of the model local oscillator chain, "Why start at 20 MHz?" "Why not use a 5th overtone crystal at 100 MHz, save a lot of multiplication and move the close in spurious out by a factor of 5"?

For the original stability assumption of ± 40 PPM, this might be an attractive choice. With a tight frequency tolerance, it is not, and to see why, the overtone equivalent circuit will be examined. Shown in Figure 5 below is the equivalent circuit of the same 20 MHz crystal, but for the 3rd or 5th overtone mode:



L1 = 3.17 μH; R1 = 10 TO 100 OHMS

C1; 3rd OVERTONE = $\frac{C1,\ FUND.}{9}$ ≈ .0022 PFD.

5th OVERTONE = $\frac{C1,\ FUND.}{25}$ ≈ .0008 PFD.

Figure 5, OVERTONE EQUIVALENT CIRCUIT

It is seen that the inductance remains the same, while C1 is reduced by a factor N^2, where N is the overtone, 3, 5, 7*, 9* etc. Consequently, the "pullability" of an overtone crystal is reduced by approximately the overtone number squared, compared to the fundamental mode. Typical pullability for a 60 MHz 3rd overtone would be on the order of ±30 PPM, and for a 100 MHz 5th overtone, ±10 PPM. Clearly, there is not enough pull range to use these modes in the TCXO or phase locked examples described here.

* Higher than 5th are relatively rare.

SHORT TERM STABILITY

Thus far, those systematic changes in frequency have been discussed which are due to factors such as temperature and time. Oscillator frequency is also perturbed by random, noise-like factors, and these perturbations typically are important for disturbances with time constants from microseconds to seconds. This short term stability is measured in the time domain where some type of frequency counter is the key instrument, and in the frequency domain, where spectral analysis of one form or another is used.

In many of these measurements it is necessary to use two oscillators, either with a small frequency offset, or locked together in a phase locked system. Some typical time domain values are listed in Table 1.

OTHER TOPICS IN CRYSTAL AND OSCILLATOR SELECTION

1. Clock oscillators: Miniature, self contained crystal oscillator and output buffer combinations. These hybrid units are available with output frequencies from sub-Hertz to 150 MHz. Outputs are compatible with standard logic families, TTL, CMOS, ECL. Militarized units are available with stabilities of ±50 PPM

FIGURE 2

Noise spectral density of high frequency transistors

The spectrum analyzer setting

Bandwidth	300 Hz
Vertical Scale	dbv with +10 db offset
Horizontal Scale	1 KHz/Div
Noise Gain	100 db

Each photograph shows two traces; the bottom trace is the reference transistor, while the top trace is the device under test.

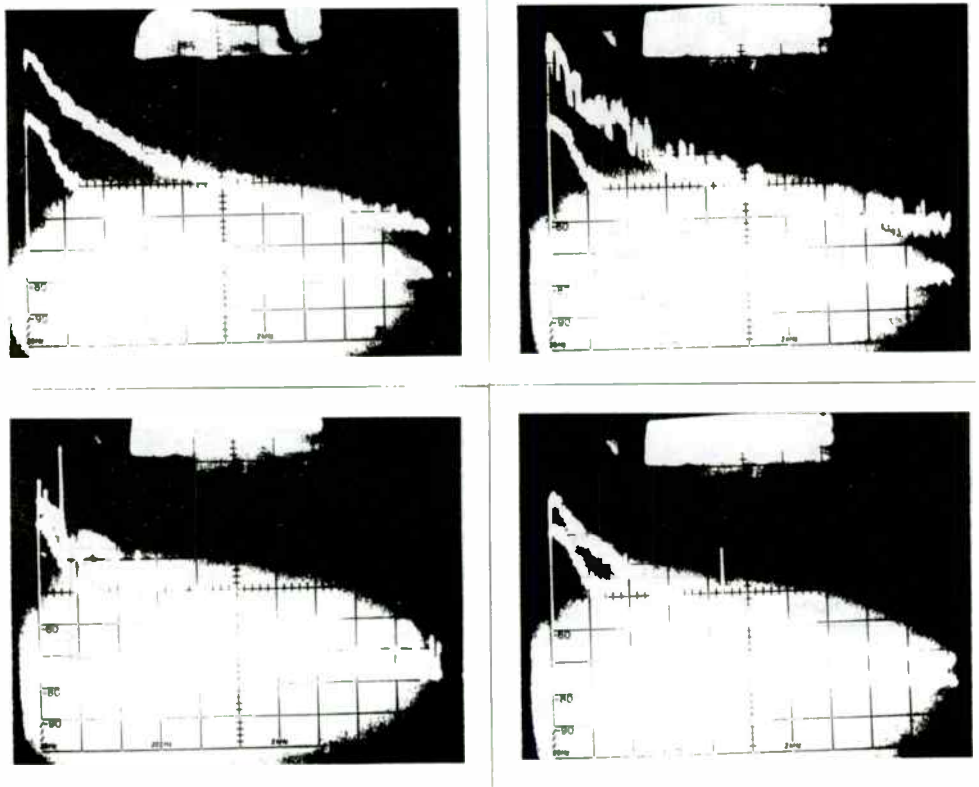
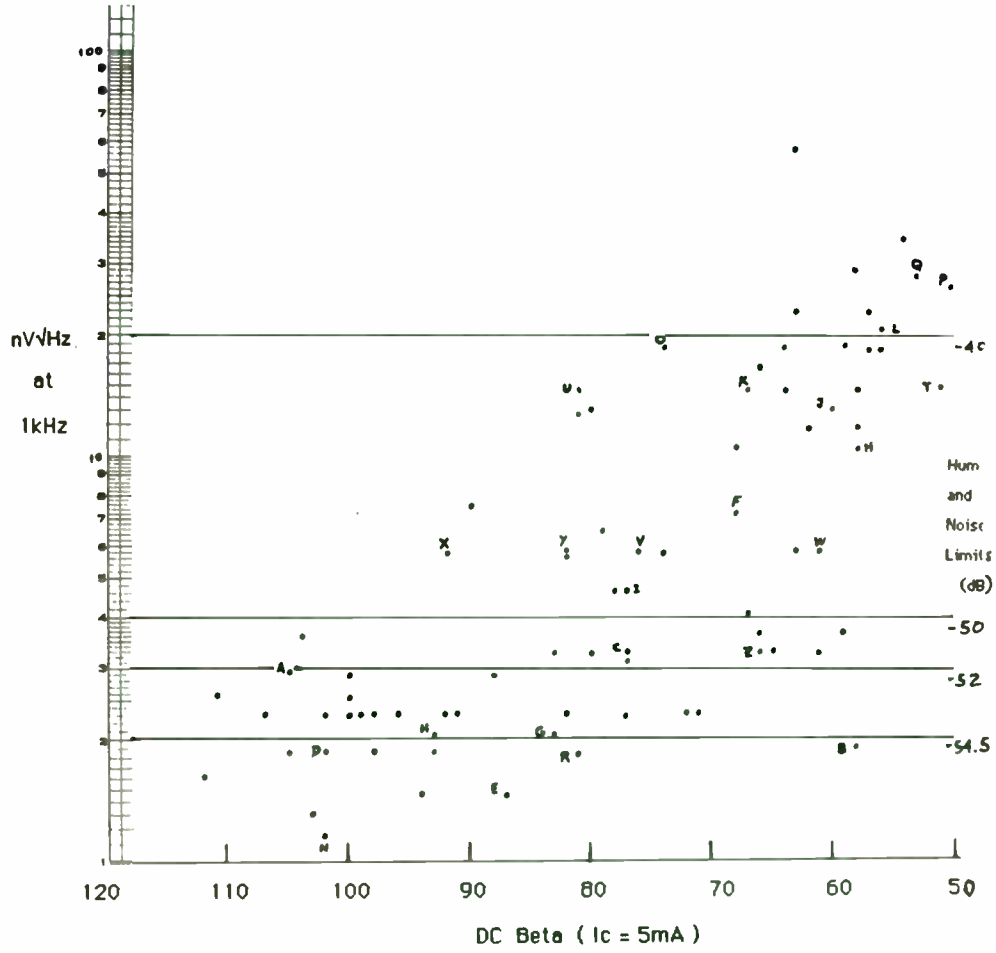


Figure 3 : Noise Voltage at 1kHz vs. DC Beta (Sample Size 83)



over the temperture range -55° C to +125° C.

2. Low power oscillators: Oscillators for battery operated equipment must sometimes operate on less than one milliampere. Using AT cut crystals in the low megahertz range and special circuits this kind of requirement can be met while retaining the advantage of the AT cut crystals. For outputs in the tens of kilohertz, where looser frequency tolerances or narrower temperature ranges obtain, tuning fork crystal oscillators are available with current drains in the tens of microamperes.

3. AGC: Simple AGC control of the oscillator operating point provides many advantages. Low crystal power dissipation, important for good ageing, can be achieved while avoiding circuit start-up problems sometimes associated with very low power operation.

SUMMARY

Choosing a crystal and crystal oscillator circuit requires matching between the requirements of the application and the characteristics of the oscillator. If the oscillator must be pulled more than 10 or 20 PPM, a fundamental crystal in the 10 to 25 MHz range is probably indicated. If the ultimate in temperature stability, ageing and close-in noise is the object, a 3rd or 5th overtone, 5 MHz, ovenized unit is indicated. For small size, low cost, and nominal AT cut stability, a clock oscillator might meet the objectives.

If VHF or UHF outputs are needed a 3rd or 5th overtone crystal oscillator, operating up to 150 MHz might simplify the design.

TABLE 2 - VCXO

	CIRCUIT PARAMETERS C3, VARACTOR								FREQUENCY PULLING DELTA F, PPM				
CASE	C1	CO	4V.C	GAMMA	C4	C5	C6/C7	L2	1V	10V	DELTA	OF/OV (1V)	OF/OV (10V)
1	.02	5	30	.5	0	2	100	0	322	519	197	38	4
2	.01	5	30	.5	0	2	100	0	161	259	98	19	7
3	.02	5	30	.5	20	2	100	0	284	363	79	20	4
4	.02	5	15	.5	0	2	100	0	447	753	306	65	20
5	.02	5	15	.8	0	2	100	0	379	858	479	87	34
6	.02	5	15	.8	0	2	50	0	488	912	424	76	30
7	.02	5	15	.8	0	2	100	3	-5	680	685*	130	45

* Even greater pulling can be accomplished with a more complex circuit.

Figure 4 : Noise Test Fixture Block Diagram

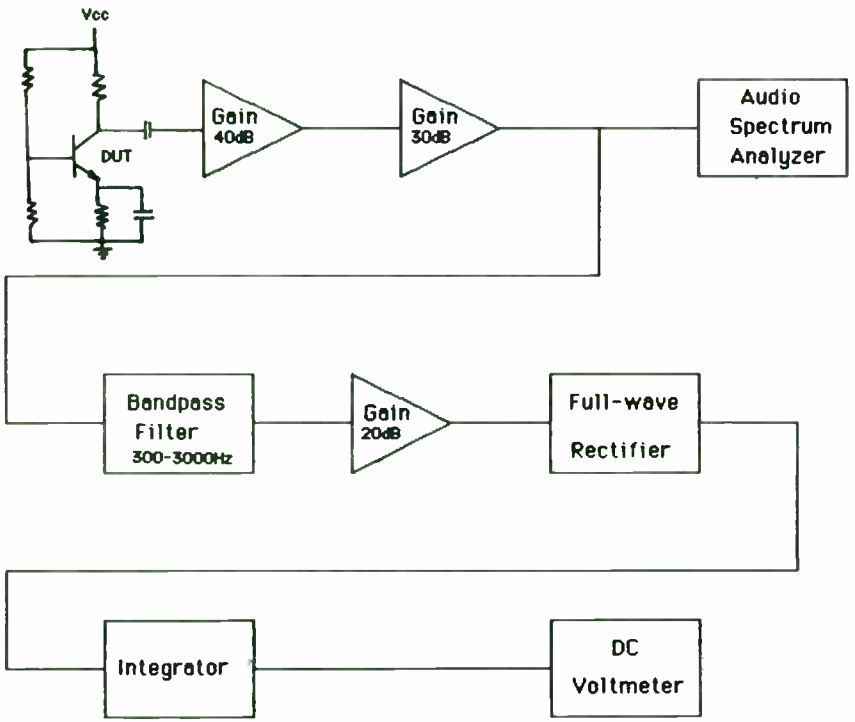


Figure 5 : Rectified DC Voltage vs. Hum and Noise

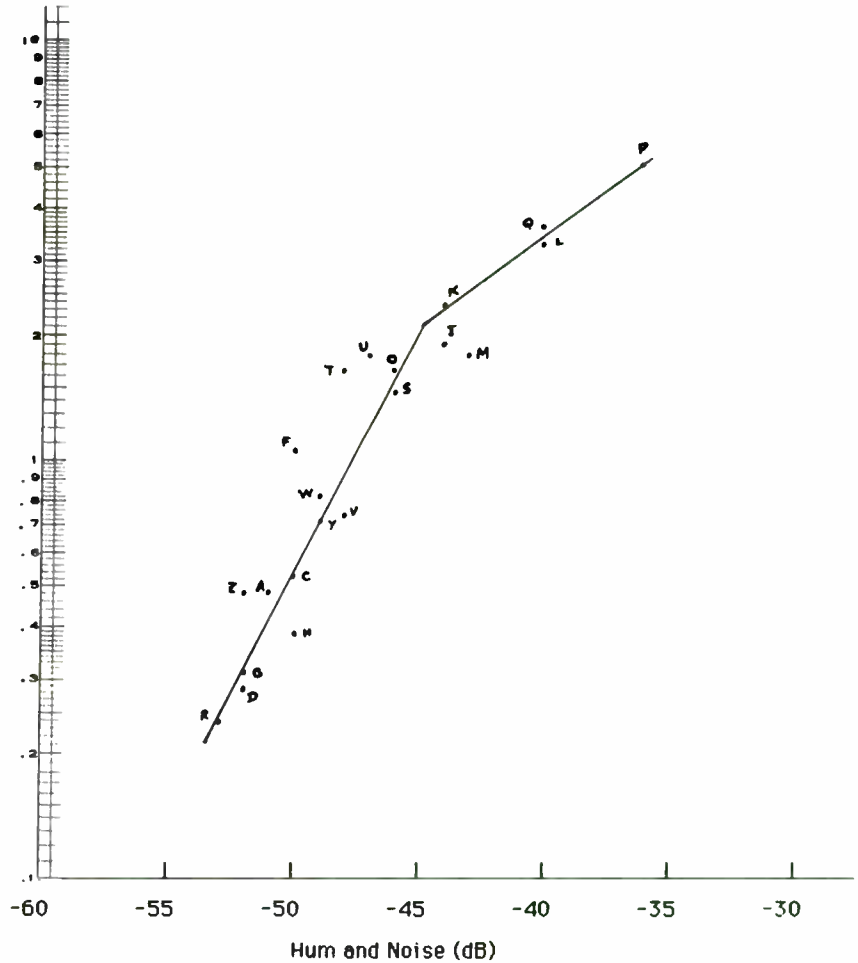


Figure 6 : Rectified DC Voltage vs. DC Beta (Sample Size 45)

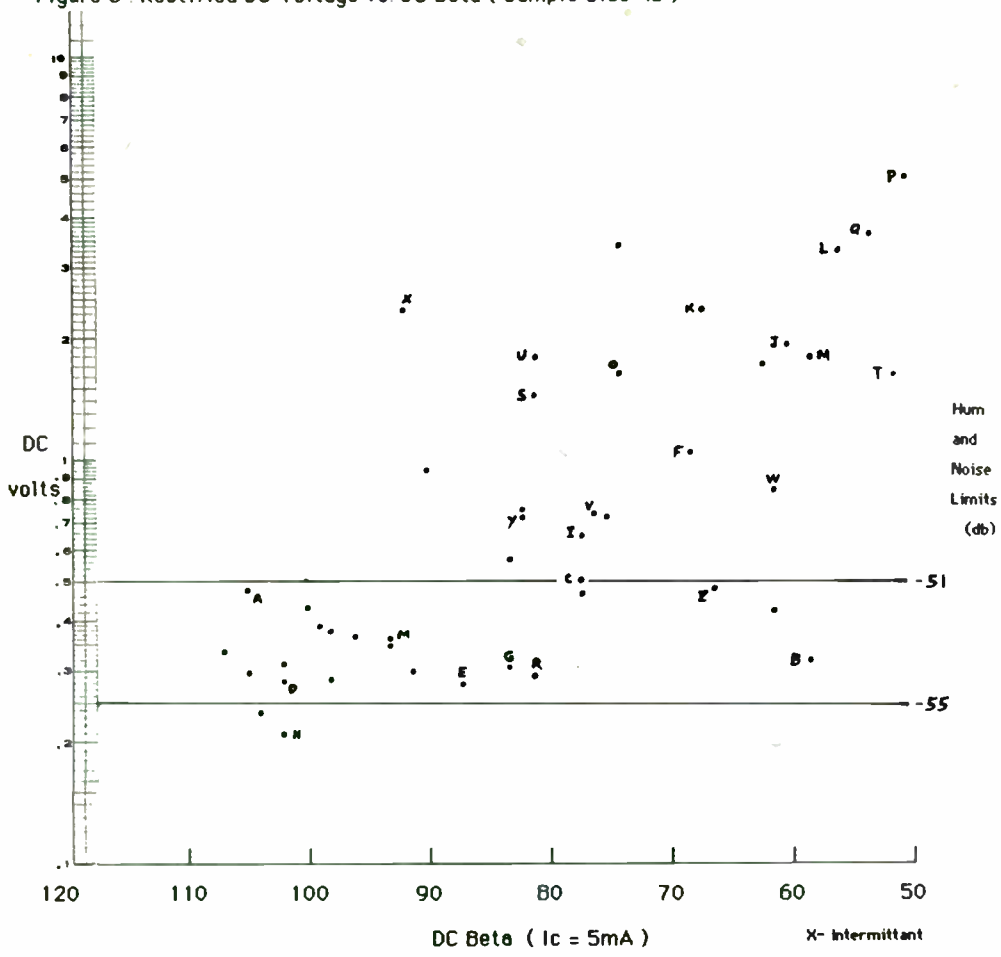
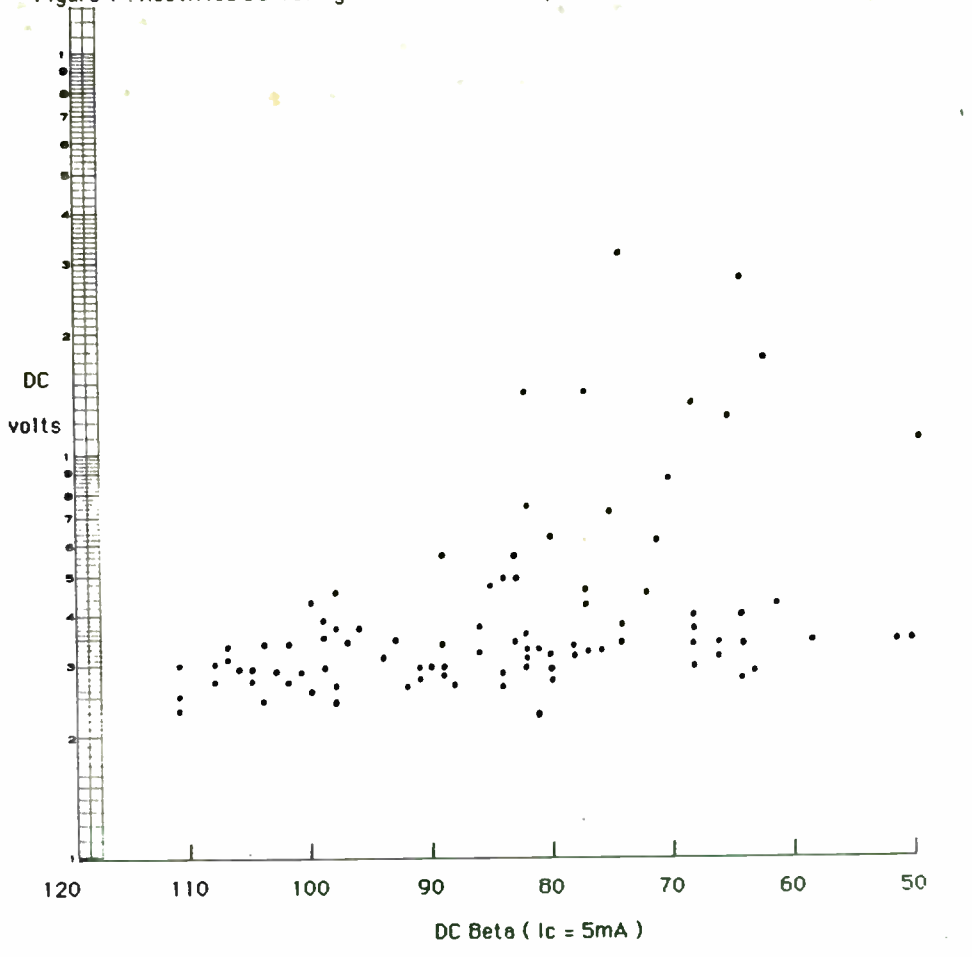


Figure 7 : Rectified DC Voltage vs. DC Beta (Sample Size 106)



MAXIMIZING CRYSTAL OSCILLATOR FREQUENCY STABILITY

by

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INTRODUCTION

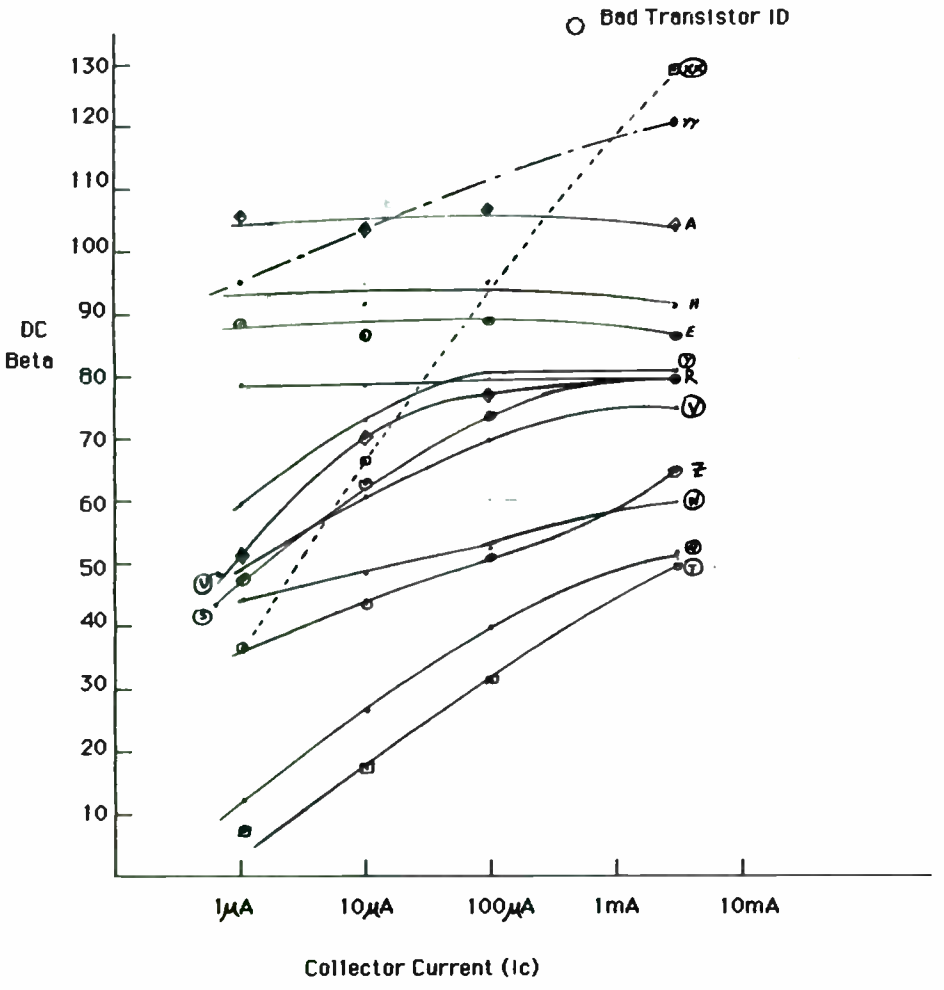
Frequency stability is one of the central topics in the study of crystal oscillators, for the exceptional stability of quartz crystals is their fundamental advantage over other resonators. Both the long term and short term stability of crystal oscillators is important. Long term stability, characterized by terms such as "drift" or "ageing", is the systematic, non-random change in frequency with time, often expressed in terms of frequency change per day or per year. Short term stability is the random, noise-like behavior of the output frequency. In a measurement system based on a frequency counter (time domain), the short term stability is typically measured over gate times from milliseconds to seconds. The same random behavior of the frequency, but measured in a system based on a spectrum analyzer (frequency domain), is often specified in terms of the single-sideband level (relative to the carrier) of the angle modulation noise sidebands, at video frequencies from fractions of a Hertz to tens of Megahertz.

The studies which have been done on this topic fall into two groups: Studies of the crystal by itself, and analysis of crystal oscillator behavior. The former are often concerned with the theory of quartz resonators and with practical considerations concerning surface preparation, electrodes, cleanliness, new designs, etc. The latter include studies and experiments with the various oscillator configurations, such as the Colpitts, Clapp, Pierce, Butler, etc.

In the study of crystal oscillator stability, it is critical to examine the oscillator and circuit together. Particularly when considering short term stability, conclusions based on observations of the crystal alone can lead to erroneous results. In order to examine the crystal-circuit relationship in some detail, this study is confined to one particular oscillator configuration. However, insights obtained from the particular case will allow conclusions which are useful in the general. Exact equations for the crystal are used, and computer numerical methods are used to generate the various reactances and, even more important, the derivatives of these reactances.

For the purpose of analyzing the stabilizing effect of the crystal on the rest of the circuit, assume that the crystal is

Figure 8 : DC Beta vs. Collector Current



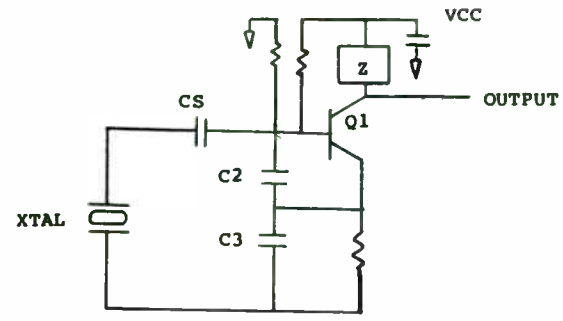
perfectly stable. In fact, certain noisy processes are associated with the crystal itself, and crystal frequency dependance on temperature and time is well known.

THE CIRCUIT

Figure 1a shows the circuit chosen for the analysis of the relationship between crystal , circuit, and frequency stability. The oscillator configuration is the popular Colpitts. Although the Colpitts is a grounded collector type of circuit, a small impedance in the collector provides a convenient signal output point and at frequencies of 10 MHz and lower this impedance has little effect on the oscillator base-emitter circuit.

THE CRYSTAL

Figure 1b shows the equivalent circuit of the frequency control crystal. The series circuit of C1, L1 and R1 represent the electrical equivalent circuit of the piezoelectric coupled mechanical resonance of the crystal. The reactances of C1 and L1 are orders of magnitude larger than that which would be obtained from electrical components, and the ratio of these reactances to R1, the loss term, or Q, is typically 50,000 to 1,000,000; again, three or more orders of magnitude larger than what can be obtained from electrical capacitors and inductors. C0 represents the parallel plate capacitor formed by the crystal electrodes. Typical values for a 10 MHz fundamental crystal are noted in the figure.

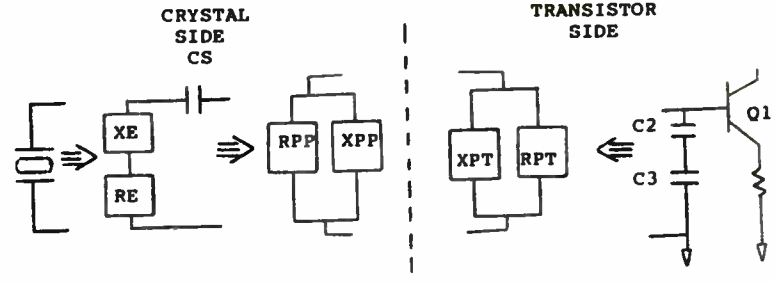


1.a.

1.b.

EXAMPLE

$F1 = \frac{1}{2\pi\sqrt{L1C1}} = 10$ MHZ
C1= .02 PICOFARADS
L1= 12.665 MILLIHENRY
R1= 20 OHMS
c0= 3.8 PICOFARADS



FOR STABLE OSCILLATION: XPP = -XPT; RPP = -RPT

1.c.

Figure 1a, b, c The Circuit

A CAD DESIGN PROGRAM FOR ANALYSIS OF ELECTRO-THERMAL COUPLING IN HIGH POWER RF BIPOLAR TRANSISTORS

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ABSTRACT

A sophisticated thermal analysis program for CAD and CAE in the field of high frequency bipolar power transistors is presented. It is shown to agree with the experimental observations of phenomena associated with RF transistor operation, namely, electro-thermal interactions. Temperature, and current density distributions are analyzed and presented as a function of power density, RF and DC operation, total emitter ballasting, contour emitter ballasting, ambient temperature, and cell splitting. A figure of merit to describe current uniformity across the active area is introduced. The method of solution and modeling of transistor electro-thermal coupling is discussed.

INTRODUCTION

The push in solid state amplifier design has constantly been toward both higher frequency and power requirements. This only emphasizes the need for quantitative understanding of the coupling between the two major physical phenomena present in transistor operation, namely, electrical and thermal behavior. Both are intimately related to device performance that is crucial to the amplifier designer. These are reliability and efficiency issues, which although they appear to be at opposite ends of the performance spectrum at first thought, are indeed very much tied together.

Efficiency ultimately can always be related to current uniformity over the transistor cell. This itself is tied to both the temperature distribution over the cell and the vertical structure of the transistor, such as collector thickness, collector resistivity, base profile, etc. Horizontal factors such as finger spacing, cell spacing, and resistor ballasting also play a major role. Reliability is usually thought of in terms of maximum junction temperature because of its direct impact on mean time to failure. Other reliability issues include current distribution (ie. current densities which can not be verified directly experimentally), and catastrophic failure due to thermal runaway usually due to misuse of the device.

Other researchers have solved the temperature distribution problem for uniform and even arbitrary power distribution for idealized transistor-like structures. These solutions include both analytical and numerical models. The result generally is the temperature distribution for the entire device. These works are adequate in those regimes when the temperature and current distributions are not extreme, ie., when the temperature and current distributions are independent of each other. It is common knowledge that

THEORY OF OSCILLATION

The crystal, capacitors CS, C2, and C3, plus the transistor reactances form a parallel resonant network at frequency F. The transistor provides gain, enough to offset the losses in the resonant circuit. It is useful for the present analysis to divide the circuit into the two parts shown in Figure 1c. The crystal, plus capacitor CS can be analyzed as a net inductive reactance XPP and parallel resistance, RPP. The transistor and C2 plus C3 are analyzed as a single parallel capacitive reactance and a parallel negative resistance, resulting from transistor gain. The circuit oscillates at a frequency where the positive (inductive) reactance of the crystal "side" equals the negative (capacitive) transistor "side". At turn-on, the negative resistance RPT developed by the transistor (connected to the complete tuned circuit) is of a lower value than the positive loss factor RPP. The net resistance is therefore negative, and oscillation begins. The amplitude of the oscillation builds to the point where some amplitude dependant gain factor, such as transistor saturation, lowers the gain and raises the effective negative resistance to exactly equal RPP, the condition necessary for steady state oscillation.

This establishes the conditions for the analysis. The following sections show that over the very narrow frequency range of inductive reactance of the crystal, the capacitive reactance of XPT is essentially constant and therefore oscillation occurs at the "intersection" of the value of XPT and the rapidly changing XPP. The stability of oscillation depends on this relationship.

THE REACTANCE CURVE

Figure 2 shows graphically * the steep rise of the parallel reactance and resistance curves due to the crystal, plotted as a function of frequency. As mentioned above, over the narrow frequency range depicted (.2%), the capacitive reactance of XPT is essentially constant. Therefore, the capacitance associated with the XPT value can be assigned to the right hand vertical scale. If, for example, we choose C2=C3=40 pF, then CT=20 pF, and the frequency of oscillation will be at point B.

The pertinent question is where we would choose to operate for best stability, but two forbidden regions must be discussed first. Practical circuit considertions including parasitic reactances and active device capacitances limit the maximum reactance of operation. In Figure 3, the boundary above which it is impractical to operate is arbitrarilly chosen as 8,000 ohms, or 2 pF.

The exact values are unimportant because this is not the region of optimum stability. The other boundary, which is important, is determined by RPP, the equivalent parallel resistance.

* Equations in Appendix

current injection for the transistor as a whole is very much dependent on temperature, but this dependence is much more pronounced for the transistor locally. High current injection aggravates high temperatures, which in turn promote even higher current injection, which results in even higher temperatures. This process, known as current localization, can easily lead to thermal runaway. The normal RF transistor in fact operates under these aggravated conditions of high current densities and high temperatures, and the results of the works mentioned above cannot be used.

In this paper we report the simultaneous solution of this coupled problem (when it exists, ie., no thermal runaway). Our own work resulted in a digital computer program TEMP3D that is easy to use, requiring a minimum of inputs, and is built around an extremely robust algorithm.

MODEL DESCRIPTION

Because the thermal time constants involved are long compared to the exciting frequencies (in the RF range) we concern ourselves with the steady state case. TEMP3D solves for the surface temperature distribution in the active regions of the RF transistor. These regions may consist of a single cell or a multi-celled array. Each cell is composed of an array of emitter fingers. TEMP3D also provides the current distribution over these fingers. The results, both current and temperature, can either be tabulated or plotted.

Thermal Model - 3 Dimensional Heat Transfer Problem

The algorithm for the calculation of the temperature distribution is based on an analytical solution of the three dimensional problem for surface temperatures.

$$\nabla^2 T(x,y,z) = 0 \qquad (1)$$

The solution for the temperature at the surface T(x,y,0) takes on the following form:

$$T(x,y,0) = \int \phi(x,y;x',y') P(x',y') dx'dy' \qquad (2)$$

where $\phi(x,y,x',y')$ is the Green's function for (1). The analytical solution is derived with the assumption that the heat distribution P(x,y) developed at the surface is known. The temperature at the bottom of the chip is held constant and uniform. The chip is homogenous and uniform. The dependence of the thermal conductivity K of silicon is described by the expression

$$K = Ao * T \hat{} B \qquad [Watts/cm/K] \qquad (3)$$

where Ao, B are constants that depend on the bulk resistivity of the silicon substrate and T is the temperature in Kelvin.

Electrical Model - Transistor Action

The electrical behavior of the device is treated by breaking up each emitter finger in all cells into a number of identical transistors whose electrical parameters are derived from an appropriately scaled version of the entire device. These individual nodal transistors are coupled by means of base and emitter resistors to

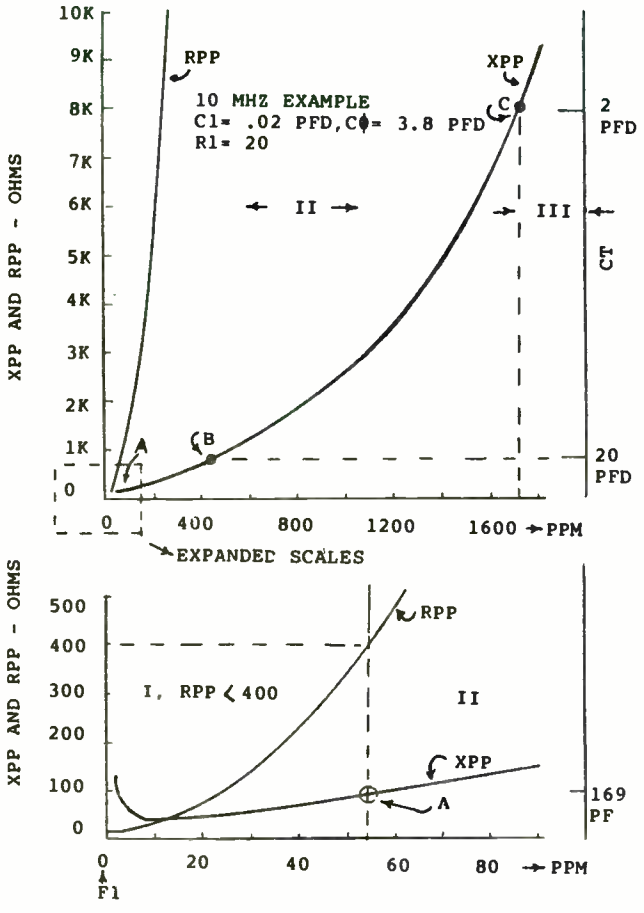

Figure 2, XPP, RPP

As discussed above (Theory of Oscillation), negative resistance is the model chosen to represent the gain relation between the transistor and the circuit. This resistance depends on the transistor characteristics and the values and ratio of C2 and C3. At present, it is important only to note that a minimum value of RPT (maximum gain), exists for any circuit value choice. Clearly, the circuit will not oscillate if RPP on the crystal side is less than RPT generated on the transistor side, so a boundary exists.

In the example, 400 ohms has been chosen as the boundary*, so the circuit must operate somewhere between point A and point C. Where shall the greatest stability be obtained? If the crystal side only is considered, one might be tempted to choose point C, since the derivative of XPP with respect to frequency is highest at this point. To resolve the question, one must examine the transistor side in greater detail and determine the form of the unstable reactance.

THE TRANSISTOR SIDE

Recall from Figure 1 that the transistor side is defined as containing the capacitors C2 and C3 and the transistor itself. The admittance of this side will have real and imaginary parts as shown in that figure. The real part will be a negative

* Since RPT depends on C2, C3 and C2/C3, the boundary between I and II is actually a curved line.

make a single emitter finger (Figure 1). Furthermore, these emitter fingers are coupled to one another via emitter ballasting resistors which may or may not be equal. The constraints for the electrical problem are that the total collector current and collector voltage are given, and the base-emitter voltage is the same for all finger transistors. The model for the nodal transistors is derived from a modified Gummel-Poon model which includes high current beta rolloff. The current injection of each elementary transistor is effected by the local temperature at that node. The current distribution calculation reflects either a DC or Class A RF solution, or high frequency Class C operation where the low frequency beta is scaled with the ft of the device.

Electro-Thermal Coupling

The solution to the total problem requires the simultaneous solution to both the thermal and electrical problems as described above so that each problem is consistent with the conditions imposed on it by the other. Namely, the electrical solution is to be consistent with the temperature distribution as dictated by the thermal problem. Similarly, the thermal solution is to be consistent with the power (current) distribution as calculated by the electrical problem.

The solution to the total problem being nonlinear in nature requires some kind of iterative scheme. The electrical problem being intrinsicly nonlinear (I ~ exp(V/Vt)) is also solved by iteration. Only the thermal problem including the nonlinearity of the thermal conductivities is put into such a form that the solution is given by exact techniques, or rather an analytic form.

The algorithm for the solution of the total problem can be seen readily in Figure 2. First, a uniform current distribution is assumed, and the corresponding temperature distribution is calculated. This thermal distribution provides the assignment of operating temperatures to the individual nodal transistors. For this thermal profile, the common emitter-base voltage for all fingers is the only parameter which uniquely defines the current at each nodal transistor. The appropriate value for this emitter-base voltage satisfies the condition that the total collector current is conserved.

Normally, the resulting nodal currents will not be consistent with the power distribution previously used to calculate temperatures. If this were the case, this would mean a self-consistent solution pair for both temperature and current has been obtained. However, a new temperature distribution needs to be calculated based on the latest solution to the electrical problem. From this resulting temperature distribution a new set of nodal currents can be calculated. This process is repeated until self consistency is reached.

The determination of the emitter-base voltage, however, is not so straight-forward. It is complicated by the fact that the nodal transistors are not coupled directly to one another. This is true only

conductance of value 1/RPT and the imaginary a positive susceptance B=1/XCT parallel (the defining equations are shown in the Appendix.)

It is beyond the scope of this paper to quantitatively model and analyze the various long and short term instabilities on this side of the circuit. Rather, some systematic and random processess will be postulated, and the form of the circuit reactance instabilities will be shown. Armed with these models we can join the left and right sides of the circuit to describe the parameter that determines frequency stability.

CASE 1

The first model assumes that C parallel has a tolerance on its average value which varies this value with time, temperature, or other systematic function. In this case

$$C = CT * (1 + e) \qquad (1.6.1)$$

Where e represents the delta change from nominal (temperature, tolerance, etc.). The incremental reactance change, DX, due to e is then:

$$DX = 1/(2\pi FCT) - 1/(2\pi FCT(1+e)) \qquad (1.6.2)$$

$$DX = (1-(1-e))/(2\pi FCT) \qquad (1.6.3)$$

$$DX = e/(2\pi FCT) = XT * e \qquad (1.6.4)$$

CASE 2

Assume that the parallel capacitor CT has a fixed, stable part in parallel with a small variable capacitor CV which represents all of the instability or noisy portion of the circuit.

$$DX = XT - XT^* XCV/(XT+XCV) \qquad (1.6.5)$$

$$DX = (XT)^2/(XT+XCV) \qquad (1.6.6)$$

For XCV >> XN:

$$DX = (XT^2/XCV) = (XT)^2 *(2\pi F)CV \qquad (1.6.7)$$

CASE 3

Assume that the current generator gm * Ib has a quadrature noise component $\overline{in} \angle 90^\circ$

The noise current into the base is derived in appendix B as:

$$\overline{iin} = \overline{in}/(1+X2/X3+gm*X2) \qquad (1.6.8)$$

Assuming gm * X2 >> (1 + X2/X3):

$$\text{then } |\overline{iin}| = \overline{in}/(gm * X2) \qquad (1.6.9)$$

The "noisy reactance", XN, which would cause this current to flow is:

$$XN = gm * X2 * es / \overline{in} \qquad (1.6.10)$$

Where es is the oscillator voltage at the base. Then

$$DX = XT - XT*XN / (XT+XN) \qquad (1.6.11)$$

$$= (XT)^2 / (XT+XN) \qquad (1.6.12)$$

for XN >> XT

$$DX = (XT)^2 * \overline{in} / (es * gm * X2) \qquad (1.6.13)$$

for X2 = K * XT (1.6.14)

(1.6.13)

$$DX = XT * \overline{in} / (K * es * gm) \qquad (1.6.15)$$

on a finger level. The nodal transistors that belong to one finger are decoupled from the next by means of the external emitter finger ballasting resistors. In practice, this means that the same problem exists on the finger level that exists for the total device. Each emitter finger has its own unique potential that satifies conservation of current in that finger.

The iterative procedure described above results in the electrical and thermal solution for the DC case. This solution can also be used for Class A RF applications where the RF power is small compared to the DC power dissipation. This analysis is also applicable to Class C operation by modifying the injection efficiency of the transistor. In this case the transistor current gain should be scaled down and determined by ft and the operating frequency:

$$beta = beta0 / sqrt(1 + (beta0 * f / ft)^2) \quad (4)$$

where beta0 is the DC current gain, f the frequency of operation, and ft is the current gain bandwidth product.

Computational Considerations

Like any other numerical solution that approximates a continuum by discretization, the accuracy improves with the number of nodes. In the same manner, this increases the time required for calculation. Specific to our problem, the time necessary for the calculation of temperature increases with the square of the number of points. For the electrical problem which involves three nested loops (node current, finger current, and emitter-base voltage), the computational effort also increases rapidly with the number of nodes. By taking advantage of symmetry which most real devices employ the computational time required was observed to be reduced by a factor of 10.

Additional reduction in the cost of computation was achieved by the use of look up tables for eliminating redundant calculations. Special efforts were made in accelerating the convergence of the algorithm by using improved prediction methods.

The time required for a typical example (1 cell, 550 nodes, well ballasted, moderate power dissipation ~ 11 kW/cm2) was about 300 CPU seconds on a PRIME 750.

User Inputs/Parameters

The inputs for program use can be broken up into two categories: those that describe horizontal configuration, those that describe the device's vertical parameters, and those that describe operating and boundary conditions.

The horizontal parameters that determine device performance include:

- chip dimensions
- chip thickness

Summarizing the three cases :

(1) $DX = (XT) * e$ (1.6.16)

(2) $DX = (XT)^2 * (2\pi F) * CV$ (1.6.17)

(3) $DX = (XT) * \overline{in} / es * gm * K$ (1.6.18)

Now we turn back to the complete circuit to find the form of delta frequency, DF.

DELTA FREQUENCY

The reactance curve of Eq. A6 plotted in figure 2 has a slope of DX/DF ohms per PPM. If one assumes an "operating" point of XT, then the frequency instability at that point will be:

$DF = [1/DX/DF] * DX$ (1.7.1)

Going back to the three cases developed in section 1.6, and substituting XPP=XPT=XT (condition of resonance),

$DF = [1/((DX/DF) * (1/XPP))] * e$ (1.7.2)

$DF = [1/((DX/DF) * (1/(XPP)^2))] * (2\pi F) * CV$ (1.7.3)

$DF = [1/((DX/DF) * (1/XPP))] * \overline{in}/(gm*es*K)$ (1.7.4)

These are the functions which yield the value of DF, the frequency instability of the total circuit, for the three cases of the preceding section. The quantities to the right of the brackets are constants determined by the degree of instability on the transistor side. The two functions in the brackets (one and three are the same) are determined by the crystal, the capacitor CS, and the value of the XT, the parallel reactance. In order to minimize delta frequency, we wish to maximize the inverse of these, which are,

I $(DX/DF)*1/XPP$ (1.7.5)

II $(DX/DF)*1/(XPP)^2$ (1.7.6)

These functions will be called the fractional reactance slope, Type I and Type II, to emphasize the fact tht it is the fractional slope which determines stability, not the absolute slope. In Figure 3, the fractional reactance slope functions and the reactance slopes have been plotted for a number of example cases, including the 10 MHz crystal of Figure 2, 5 MHz third overtone, and a 60 MHz third overtone. The functions are maximum at the lower boundary. The intuitively attractive steep slope at point "C" in Figure 2 is now shown to be deceptive because of the role of fractional slope in stability.

The effect of R1 and Q now becomes clear. The fractional reactance slope depends on XC1 of the crystal, so for all other factors equal, one always wants to maximize that. But best stability is found at the lowest reactance, and that occurs at a value determined by RPP which depends on R1, the crystal series

- cell configuration - to itself and to chip

- emitter configuration in the cell

- emitter ballasting distribution (Re)

  uniform or arbitrary on a finger basis

Vertical parameters which characterize a particular transistor process include

- epi thickness and resistivity

- Gummel-Poon parameters

- parasitic emitter resistance

- two dimensional injection effects
  extrinsic base resistance - rb'
  knee current

- ft

Finally, transistor operating conditions are input. These include:

- bottom chip temperature

- total collector current

- collector voltage

- operating frequency

RESULTS

Benchmark Problem

For purposes of illustration a model to be used as a benchmark will now be considered. It represents a typical RF transistor with ft on the order of 5 GHz and saturated output capability of 1 W at 1 GHz. This structure as seen in figure 3 consists of 50 emitter fingers, 2 microns wide, spaced 4 microns apart. Each emitter finger has its own ballast resistor of 80 ohms, which makes for 1.6 ohms for the whole device. The total base area is 17 by 1.2 mils. Chip size is 25 by 18 mils, and 4.5 mils thick.

The benchmark operating conditions for purposes of comparison, are Ic = 100mA, Vce = 15 V, and Tmin = 60C. The typical printed output for the solution of this problem under these conditions can be seen in figure 4.

This data is organized into three parts. The first of these is a short summary that reports the minimum and maximum temperatures and nodal currents and the asscociated fingers. This is done for each cell in the structure. It should be noted that all currents unless noted are normalized to the current that would exist if the current were uniformly distributed across the device. Also seen is the heading "X AREA USED" which is a figure of merit that describes uniformity in current distribution across the cell.

The next section describes the temperature and current profiles along the fingers (y axis microns) that were selected

Several things have happened. At XPP equal 94 ohms, point C, RPP now equals 277 ohms, so this point violates the lower boundry of 400 ohms. Adjusting XCT to 112 ohms (changing CT), point D, gives RPP equal 402 ohms. DX/DF is now 2.14 so the fractional reactance slope (I) is 1.91E-2. The stability has been improved by about 14 percent for type I instabilities,compared to point A. But the type II fractional reactance slope is decreased by about 5 percent. So the answer for this particular example depends on the exact nature of the circuit instabilities. Note that this example assumes a perfect capacitor for CS. If CS were a varactor diode it is apparent that as the value decreases it is possible to move to a point where RPP is too low for oscillation. In VCXO designs then, the margin for oscillation should be adjusted at minimum capacity.

CONCLUSION

For several models of transistor and circuit instabilities it is seen that frequency stability is maximized when the fractional reactance slopes, Type I and Type II, are maximum. For a number of crystal examples these functions are maximum at the lowest parallel reactance. The minimum reactance point depends on the value of RPT, the parallel negative resistance. The effect of a capacitor in series with the crystal on stability depends on the exact nature of the circuit instabilities.

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6. Parzen, B., "Design of Crystal and Other Harmonic Oscillators," New York: John Wiley & Sons, 1983

in the previous part for extrema in temperature and current.

The last part of the printout is a detailed summary on a finger by finger basis for each cell. Included are the temperatures and currents at both ends and center of each finger. Also included is the total finger current normalized and in mA as well as the ballast resistance associated with that finger.

As can be seen for this benchmark case the maximum temperature and current occur in the same finger, number 26. This maximum junction temperature of 114 C occurs in the same finger where the current is 13.5% greater than nominal. The minimum current and temperature occur at the corner of the cell in finger number 1. The temperature here is 87 C and the current is only 81% of nominal. As seen in the summary for all fingers, the variation in finger currents is only 10.7% while the variation in nodal current over the whole device is 28.5%. This uniformity in finger current is due to strong emitter ballasting, while there is no mechanism to force uniform current distribution along the finger.

The same data is effectively presented graphically in figures 5 and 6. Temperature and nodal current are plotted as a function of finger positioned for cross-sections along the center of the cell and cell edge. It is evident that even for these benign operating conditions there is a noticeable variation in temperature and current from center to edge.

Figures 7 and 8 present similar data for temperature and current, except that the independent variable is position along the finger. Chosen for illustration are the hottest and coolest fingers at the center and end of the cell respectively.

In figure 9 total finger current in mA is plotted as a function of finger position. The sum of these finger currents must add up to the required 100 mA.

Data can also be presented in a quasi three dimensional format as seen in figure 10. The output from TEMP3D is compatible with two dimensional thermal analysis programs using finite element techniques that were also generated by the authors. Shown in figure 10 is temperature over the active region. The projection of the contour over the bottom plane gives the position and shape of the cell. The "x" and "y" dimensions are in mils. Isothermal representation of this same data is seen in figure 11. The difference between isotherms corresponds to 2 C.

Influence of Operating Point

It is well known that the high-current, low-voltage operating regime represents a less stressful condition than low-current, high-voltage operation for constant power. The low-current, high-voltage condition yields higher junction temperatures and greater nonuniformity in current distribution. This increase in stress results from ineffectual emitter ballasting

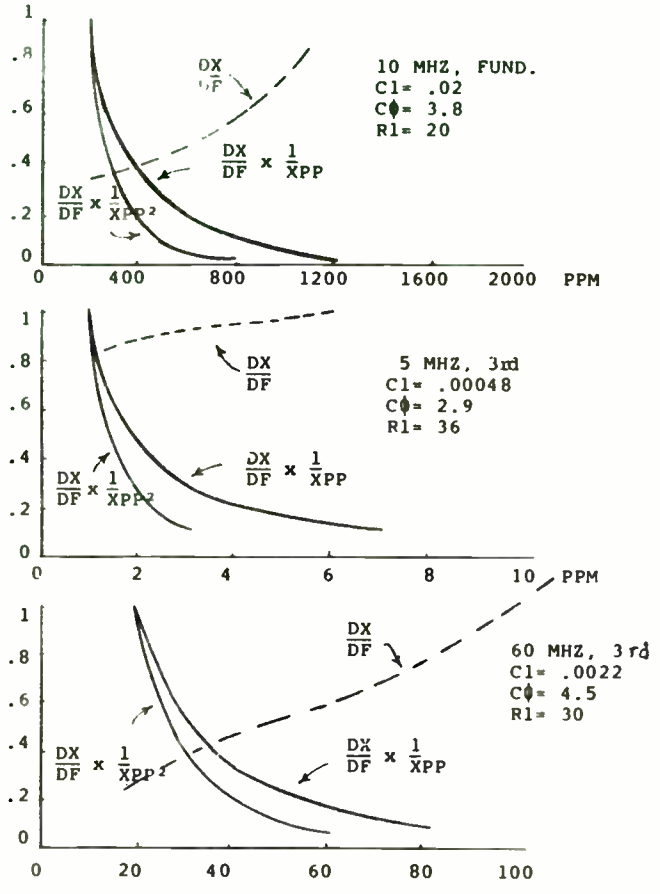


Figure 3, Relative Slopes

resistance. The crystal resistance determines stability indirectly by restricting the "operating" point of the circuit.

SERIES CAPACITANCE

Can one improve frequency stability by putting a capacitor in series with the crystal? The intuitive answer to this recurring question goes as follows (refer to Figure 2). The slope, DX/DF, increases with frequency but the fractional reactance slope decreases with frequency. At points A and B then,

Table 1.8.1

	PPM	RPP	XPP	DX/DF	TYPE I DX/(DF*XPP)	TYPE II DX/(DF*XPP^2)
A	55	402	94	1.58	1.68E-2	1.79E-4
B	440	25K	841	2.29	2.7E-3	3.2E-6

so better stability is obtained at A. If one adds a capacitor of reactance -747 ohms in series with the crystal, the entire curve is shifted in the negative direction. Is not now the reactance at F = 440 PPM equal to 841 minus 747 or 94? And since the curve is simply shifted, have we not now the DX/DF of point B but at the reactance of point A? Table 1.8.2 shows the results of adding a 21.3 pFd capacitor.

TABLE 1.8.2

	PPM	RPP	XPP	DX/DF	TYPE I DX/(DF*XPP)	TYPE II DX/(DF*XPP)
C	436	277	94	2.04	2.17E-2	2.31E-4
D	444.4	402	112	2.14	1.91E-2	1.71E-4

at low currents. Another reason for this behavior is due to the degradation of beta with high current which makes base resistance ballasting significant. This is borne out by reference to Figure 12. For all data points, the total DC dissipation was held to 1.5 W; the current was changed from 35 to 300 mA. Not only is a reduction in the maximum junction temperature observed, but the effective area used increases from 60 to 99% with increasing current. This effect is even more dramatic as the total dissipation increases.

Ambient Conditions

The role of the nonlinearities associated with the thermal conductivity of silicon and current transport can be seen in Figure 13. In this case we have plotted the maximum junction temperature versus the bottom temperature of the chip. If the thermal conductivity of silicon had no dependence on temperature there still should not be a one for one increase in junction temperature as denoted by the line "linear model". This is because current injection itself depends strongly (expotentiallly) on temperature.

Emitter Ballasting (Re)

The dilemma in the use of emitter ballasting is that even though it provides for a more rugged device, it acts as a parasitic element electrically, which reduces transistor efficiency and gain. The RF transistor designer would like to minimize these undesirable effects and still guarantee reliable operation. Figure 14 presents the dependence of maximum junction temperature and "% Area Used", ie. current nonuniformity, on total emitter resistance. This is done for the benchmark model with identical ballasting resistors. It is seen that no significant change in transistor behavior occurs until Re drops below .4 ohms. After the total emitter resistance drops below the dynamic resistance of the emitter-base junction Vt/Ic ~ .33 ohms at 110 C the maximum junction temperature begins to rise quickly, and current becomes localized to the hot spot of the device. If ballasting were much further reduced, the benchmark model would experience thermal runaway even for these moderate operating conditions. This is evident from the fact, that for Re = .1 ohms the maximum junction temperature jumps to 136 C and the "% Area Used" drops to 48%. Figures 15 and 16 present the temperature and nodal current distributions for the case Re = .1 ohms. The localization of current and temperature in the center of the cell is readily observed.

Figure 17 shows the normalized finger currents as a function of finger position with Re as a parameter. It can be seen that with the decrease in emitter ballasting the current tends to crowd in the center of the cell. As seen previously in Figure 14 one can observe the striking jump in current localization in going from .2 to .1 ohms.

APPENDIX A, EQUATIONS

CRYSTAL

$$X1 = XL1 + XC1 \quad ; \quad F1 = 1/2\pi\sqrt{(L1 + C1)^{.5}} \qquad (A1)$$

$$= j2\pi F / ((2\pi F1)^2 * C1) - j/(2\pi F * C1) \qquad (A2)$$

$$XO = -j / 2\pi F * CO \qquad (A3)$$

CRYSTAL SERIES EQUIVALENT

$$XE = XO*((R1^2 + X1*(XO + X1))/(R1^2 + (XO + X1)^2) \qquad (A4)$$

$$RE = R1/((R1/XO)^2 + ((XO + X1)/XO)^2) \qquad (A5)$$

PARALLEL: XPP and RPP from RE and XE + XCS

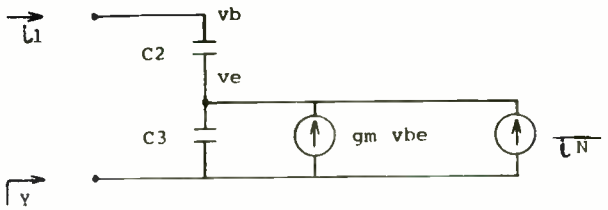
$$XPP = (RE^2 + (XE + XCS)^2)/(XE + XCS) \qquad (A6)$$

$$RPP = (RE^2 + (XE + XCS)^2)/RE \qquad (A7)$$

DERIVATIVES: COMPUTER CALCULATED INCREMENT

$$\Delta XPP = XPP @ F - XPP @ (F\text{-freq. increment}) \qquad (A8)$$

APPENDIX B, TRANSISTOR MODEL



$$i1 = vb*1/(1 + x2/x3 + gm*x2) + \overline{in}/(1 + x2/x3 + gm*x3) \qquad (B1)$$

$$Y = i1/vb = 1/RPT + 1/XCT \qquad (B2)$$

$$RPT = gm*x2*x3 + (x2 + x3)^2/gm*x2*x3 \qquad (B3)$$

$$XCT = ((x2 + x3)^2) - (gm*x2*x3)^2))/(x2 + x3) \qquad (B4)$$

$$\dot{XCT} = x2 + x3 \qquad (B5)$$

$$\overline{in} = \overline{in}/(1 + x2/x3 + gm*x2) \qquad (B6)$$

$$\dot{\overline{in}} = \dot{\overline{in}}/gm*x2 \qquad (B7)$$

$$\dot{XN} = \dot{es}/in - \dot{in}\,es/in^2 = gm*x2*es \qquad (B8)$$

Contoured Ballasting

In view of the fact that it is desirable to ballast at lower levels from an circuit point of view, TEMP30 gives the RF transistor designer the tool to change ballasting contours and obtain quantitative information on the effects of contouring on current and temperature distribution. As an example, the benchmark model for Re = .2 ohms was selected. The emitter finger ballast resistors were chosen as seen in Figure 18. The emitter resistors were varied linearly in value from 6 to 10 ohms for fingers 1 to 10 respectively. Fingers 11 to 25 were assigned resistor values that also varied linearly from 10 to 14 ohms respectively. The resistors belonging to positions 26 through 50 are symmetric about the center of the cell. The total emitter resistance for this contcured case was held to .2 ohms. This level is also shown for the uniform case where all 50 resistors have the value of 10 ohms.

The effect of this contour ballasting is presented in Figure 19. The results for the uniform case yeilded a maximum junction temperature of 123 C and "X Area Used" of 70%. By going to this contoured scheme the junction temperature was reduced to 114 C. This is the same result as calculated for the 1.6 uniformly ballasted case. More significant, however, is the fact that the figure of merit for current uniformity increased to 85%.

This could still further be improved upon by refining the contour of the ballast resistors. The example shown represent a simple guess on our part based on the results from the uniform case.

RF Behavior

It is also well known that the level for adequately ballasting RF transistors for Class C operation is much lower than for Class A. This is reflected in the fact that thermal resistance as measured under self-bias in Class C is lower than under pure DC conditions. What is inferred, is that the power distribution under strictly RF conditions is more uniform than in Class A. We attribute this improvement in uniformity to degradation of gain with frequency. This degradation of gain is not only due to beta rolloff with frquency but is also a strong function of collector current amplitude. As the current amplitude increases, base widening effects become more pronounced. This phenomenon sharply limits the ability of the RF current to localize. The DC component of this current, which is responsible for heating, follows the RF current distribution and tends to be more uniform in comparison to DC operation with the same power dissipation. Figure 20 illustrates how this phenomenon is handled in TEMP3D. Both curves correspond to the benchmark model with uniform emitter ballasting of .2 ohms. The difference between 1 GHz and DC operation is dramatic in

temperature (114 C vs 134 C), area used (99% vs 70%), as well as the finger current distribution as shown in Figure 20.

Multi-Cell Structures

The ability of TEMP3D to handle multi-celled structures is shown in Figure 21. A new transistor configuration based on the benchmark model was investigated. This new device is a four cell array having the same number of emitters and base area as the benchmark model. The spacing between cells was 2 mils in both directions. In all other respects the conditions and model parameters of these two devices were the same. As seen from the short summaries, the improvement in "% Area Used" (97% vs 90%) and maximum junction temperature (96 C vs 114 C) is significant. An interesting observation is that the fingers where maximum temperature and current occur is shifted from the center of each cell. This means that there still is thermal coupling between cells.

Device Miniaturization

The reasons for shrinking geometries of RF transistors are directly related to improving frequency performance. The reduction of cell area results in smaller collector-base capacitance. Tighter emitter structures lead to improved injection performance and reduction of the extrinsic base resistance. All these directly impact the maximum frequency of operation. The limitations here are related to two parameters primarily, chip thickness and power density.

Figure 22 illustrates the effects of scaling down the benchmark model: all horizontal dimensions were scaled down by a factor of two. In the new device all 50 emitters are 1 micron wide, the length of the cell is reduced to 8.5 mils, and the cell width is retained to be 1.2 mils. The results of the computer calculation are presented in Figure 22. Both maximum temperature and the "% Area Used" dramatically change for the worse. The "% Area Used" goes from 89% to 64%, while the peak junction temperature jumps to 166 C versus 114 C.

Correlation with Experimental Results

The quantitative reliability of TEMP3D was verified using liquid crystal techniques. Liquid crystals were used because of their excellent spatial resolution (~ 2 micron). For the structures measured agreement with measured data was excellent (within 5 C).

CONCLUSIONS

A sophisticated thermal analysis program for CAD and CAE in the field of high frequency bipolar power transistors was developed. It has been shown to agree with the qualitative phenomenon associated with RF transistor operation, namely, electro-thermal interactions. Temperature, and current density distribution were analyzed and presented as a function of power density.

HARMONIC FILTERING AT UHF AND MICROWAVE FREQUENCIES

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The need for good filtering at a reasonable cost, size and performance is important to the designer of communications systems and/or equipment. For instance, harmonic suppression in oscillators have traditionally utilized low or band pass filter circuits to reduce distortion. These types of filters usually have well defined "skirt(s)" and high out-of-band rejection that require coupled, multi-element, high Q resonators.

At UHF and microwave frequencies, distributed elements (transmission lines of prescribed impedance) are employed to achieve an acceptable design due to their higher Q and predictability at microwave frequencies compared with standard lumped elements. However, distributed element filters also have problems. Tuning ("tweaking") multi-distributed elements in production is tedious and odd frequency reentrant modes are omnipresent. Tuning is a problem in that the lengths of the distributed elements must be altered (shortened/lengthened) in the alignment of the filter. This is not easy since the multi-resonant elements interact. The reentrant issue is one that is difficult to deal with in design and generally requires a compromise in performance to minimize its effect. By concentrating on the harmonic frequencies and the reentrant nature of distributed elements, a designer can turn a problem into a simple solution.

Before actually designing any filter using transmission lines, it is important to understand transmission line resonant circuits and their reentrant behavior. The general expression for the impedance down a dissipationless transmission line is:

$$Zin = Zo*((Zl+jZo*\tan(B*l))/(Zo+jZl*\tan(B*l))) \qquad \text{(Eq.1)}$$

where: Zo = characteristic impedance of the transmission line

B = 2*Pi/L

L = the frequency wavelength in the transmission line.

l = the length of the transmission line between Zin & Zl.

Zl = the load impedance on the end of the line.

To form a simple minimum loss resonant circuit, Zl can be a short-circuit (Zl=0) or Zl can be an open-circuit (Zl=00). In reality, at microwave frequencies even a good short-circuit is slightly inductive (due to its finite length) and an open-circuit is slightly capacitive (due to end fringing capacitance). Both these parasitic effects require the transmission line to be

RF and DC operation, total emitter ballasting, contour emitter ballasting, ambient temperature, and cell splitting. A figure of merit to describe current uniformity across the active area was introduced. The method of solution and modeling of transistor electro-thermal coupling was discussed. The program is easy to use, converges rapidly, and presents data in a concise and convenient format.

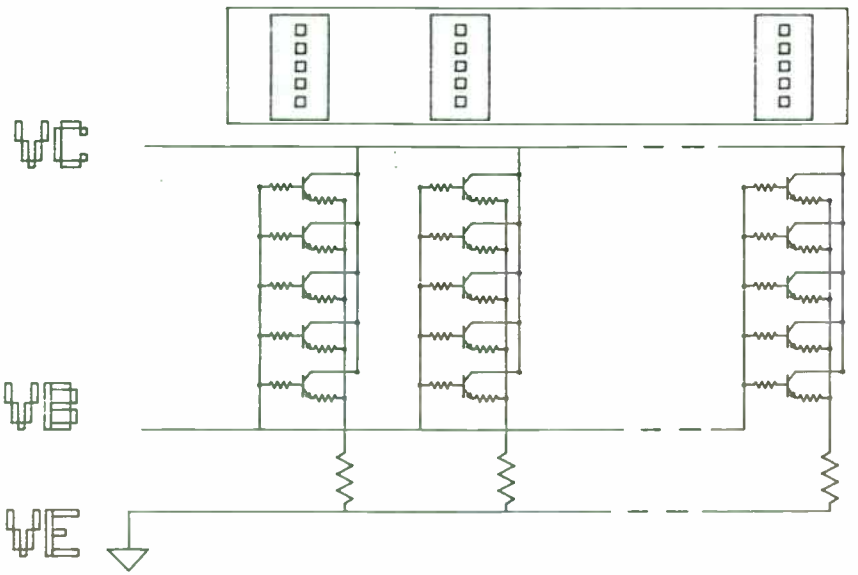


Figure 1. Electrical Schematic of Transistor (Electrical) Model

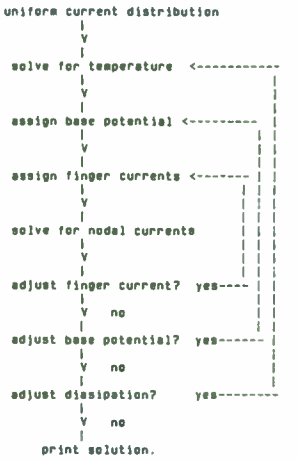


Figure 2. Schematic Representation of Algorithm for the entire solution, both current and temperature.

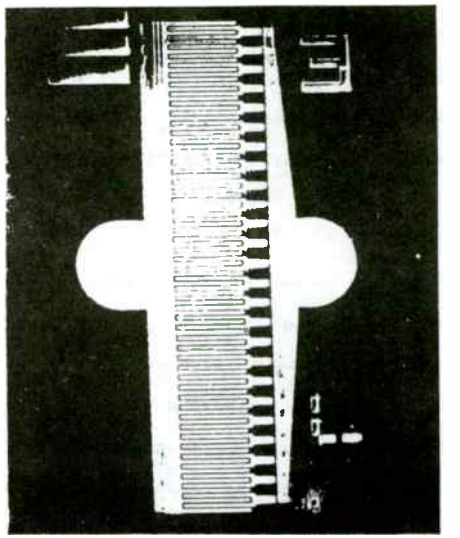


Figure 3. Electromicrograph of typical RF power bipolar transistor - base area 17 x 2.5 mils sq.

slightly longer to achieve a desired Zin that would normally be predicted by Eq.1.

If Zl=0 (short-circuit load) is substituted into Eq.1 then:

$$Zin = Zsc = jZo*Tan(2*Pi*l/L) \qquad (Eq.2)$$

From the transcendental nature of Eq.2, it is apparent that the impedance of a shorted transmission line has more than one unique length; (l) for a given wavelength, (L) at which it will be series resonant at Zsc = 0, and parallel resonant at Zsc = 00. Therefore, from Eq.2 the following information can be derived:

Zsc = 0 when l = 0, L/2, L, (3/2)*L, 2*L, ...

Zsc = 00 when l = L/4, (3/4)*L, (5/4)*L, (7/4)*L, ...

If Zl = 0 (open-circuit load) and is substituted into a rearranged form of Eq.1 then:

$$Zin = Zoc = -jZo*Cot(2*Pi*l/L) \qquad (Eq.3)$$

Eq.3 is also transcendental, and it is apparent that the impedance of an open transmission line has more than one unique length (l) for a given wavelength (L) at which it will be parallel resonant at Zoc = 00 and series resonant at Zoc = 0. From Eq.3 the following information can be derived:

Zoc = 00 when l = 0, L/2, L, (3/2)*L, 2*L, ...

Zoc = 0 when l = L/4, (3/4)*L, (5/4)*L, (7/4)*L, ...

From inspection of the derived length (l) data for Zsc and Zoc, it can be concluded that the shortest or fundamental line for a distributed resonant circuit is one-quarter wavelength (L/4). This excludes l=0 because it is outside the boundary conditions for a finite resonant element.

Thus far the discussion of distributed resonant circuits has been confined to a fixed wavelength (L) or frequency with a variable line length (l). This constraint has allowed the concept of the fundamental one-quarter wavelength to be established as a basic resonant building block for a filter. From a practical stand point (l) is fixed and by definition (L) is variable across the frequency spectrum. The relationship between wavelength (L) and frequency (F) is:

```
CELL NO.          MAXIMUM                          MINIMUM                    % AREA
          TEMP   FO  CURRENT  FO   TEMP   FO  CURRENT  FO                    USED

  1  :  1    114.  20   1.135  20     87.   1   0.011   1  80.515

CELL NO.   FINGER NO.    Y        TEMP   CURRENT
  1   :    1     20
                        2.718     102.   0.840
                        5.487     107    0.950
                        8.256     110.   1.033
                       11.026     112.   1.088
                       13.800     114.   1.124
                       16.571     114.   1.135
                       19.342     114.   1.124
                       22.113     112.   1.088
                       24.884     110.   1.033
                       27.655     107    0.950
                       30.425     102.   0.840

CELL NO.   FINGER NO.    Y        TEMP   CURRENT
  1   :    1     1
                        2.718      87.   0.011
                        5.487      86.   0.080
                        8.256      82    0.824
                       11.026      83.   0.853
                       13.800      84    0.870
                       16.571      84.   0.870
                       19.342      84    0.870
                       22.113      83    0.853
                       24.884      82    0.824
                       27.655      80    0.800
                       30.425      87.   0.011

FO          TEMPERATURE                    CURRENT          FCUR      Ic (mA)    Re (ohms)
  1      87.    84.    87.   0.011   0.870   0.011   0.014   1.0870    80.0
  2      91.    88.    91.   0.011   1.015   0.011   0.041   1.0810    80.0
  3      93.   102.    93.   0.010   1.041   0.010   0.050   1.0150    80.0
  4      94.   105.    94.   0.021   1.050   0.021   0.070   1.0401    80.0
  5      88.   108.    88.   0.025   1.070   0.025   0.070   1.0505    80.0
  6      87.   107.    87.   0.020   1.080   0.020   0.007   1.0730    80.0
  7      88.   108.    88.   0.032   1.087   0.032   0.002   1.0847    80.0
  8      88    108.    88.   0.035   1.083   0.035   0.007   1.0844    80.0
  9      88    110.    88    0.037   1.088   0.037   1.001   2.0025    80.0
 10     100    111.   100.   0.030   1.103   0.030   1.005   2.0082    80.0
 11     100    111.   100.   0.041   1.100   0.041   1.007   2.0150    80.0
 12     100.   112.   100.   0.042   1.108   0.042   1.010   2.0180    80.0
 13     101    112    101    0.043   1.112   0.043   1.012   2.0240    80.0
 14     101    112.   101.   0.045   1.114   0.045   1.014   2.0275    80.0
 15     101.   112.   101.   0.045   1.110   0.045   1.015   2.0300    80.0
 16     101    113.   101.   0.046   1.110   0.046   1.017   2.0331    80.0
 17     101    113.   101.   0.047   1.118   0.047   1.018   2.0353    80.0
 18     102    113.   102.   0.048   1.120   0.048   1.018   2.0372    80.0
 19     102    113.   102.   0.048   1.121   0.048   1.019   2.0387    80.0
 20     102    113    102    0.048   1.122   0.048   1.020   2.0400    80.0
 21     102    113.   102.   0.048   1.122   0.048   1.021   2.0410    80.0
 22     102    113.   102    0.048   1.123   0.048   1.021   2.0418    80.0
 23     102    113.   102.   0.048   1.123   0.048   1.021   2.0424    80.0
 24     102    114.   102.   0.048   1.124   0.048   1.021   2.0428    80.0
 25     102.   114.   102.   0.048   1.124   0.048   1.021   2.0430    80.0
```

Figure 4. Typical TEMP3D output for structure shown above. This benchmark model represents a device with 50 emitters, base area of 17 x 1.2 mils sq., Re = 1.6 ohms, chip thickness of 4.5 mils. Operating conditions are Vce = 15 V, Ic = 100 mA, and Tmin = 60 C.

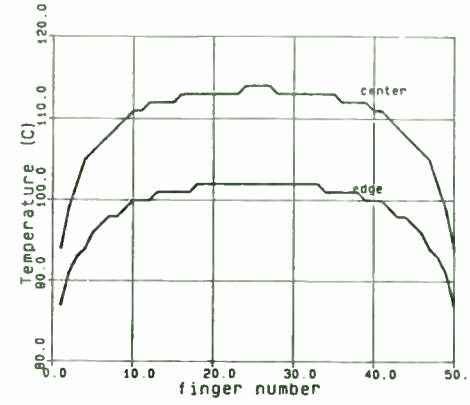


Figure 5.

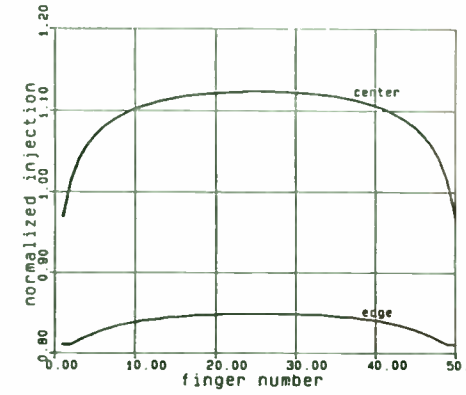


Figure 6.

Temperature and Current distributions along the cell length for the benchmark model under conditions described in Figure 4.

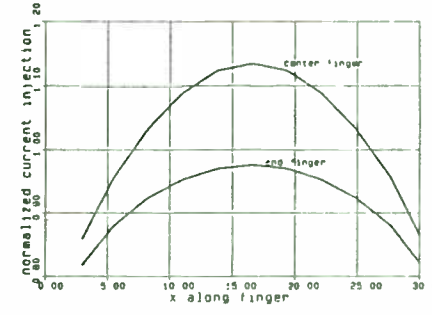


Figure 7.

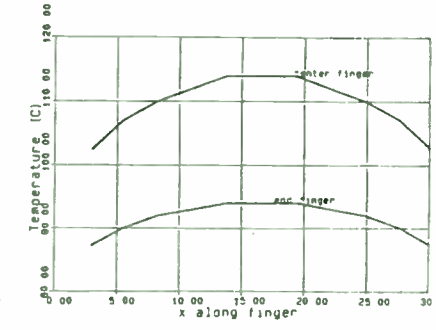


Figure 8.

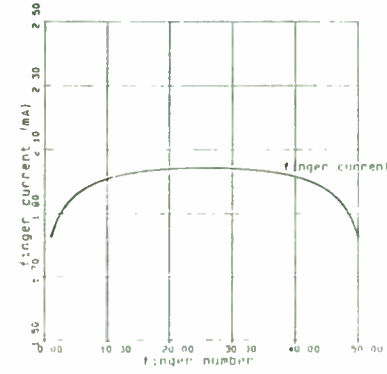


Figure 9.

Figures 7, 8. Temperature and Current distributions along finger length for the benchmark model (Figure 4.)

Figure 9. Finger Current injected at each finger for the benchmark model.

L = Vp/F (Eq.4)

where: Vp = velocity of propagation of the wave within the line.

For purposes of further discussion, the angular expression in Eq.2 and Eq.3 can be rewritten in the following form:

2*Pi*l/L = (Pi/2)*(F/Fo) (Eq.5)

where: l = Lo/4

Lo = Vp/Fo

Fo = fundamental resonant frequency

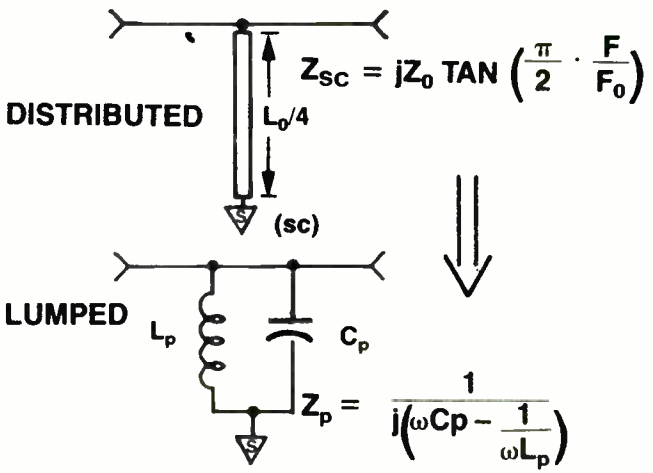


Figure 1.

Figures 1 and 2 show Lo/4 shunt transmission lines with short-circuit and open-circuit loads respectively. Their analogous lumped element equivalent is shown adjacent to them.

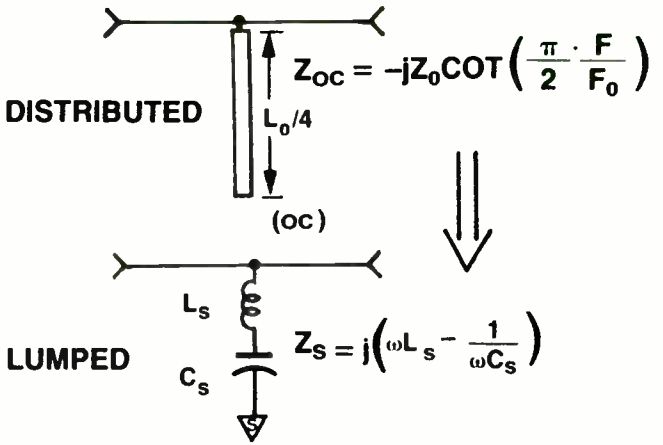


Figure 2.

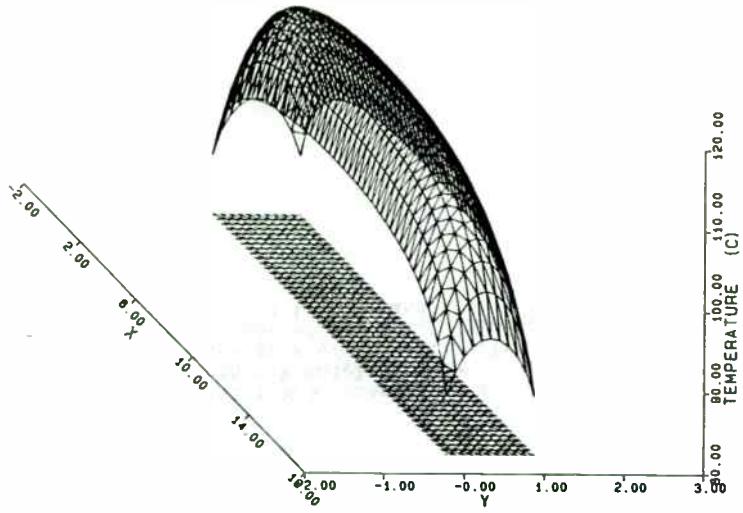


Figure 10. Three Dimensional Representaion of Surface Temperature for the benchmark model (Figure 4.). Tmax = 114 C, Tmin = 87 C.

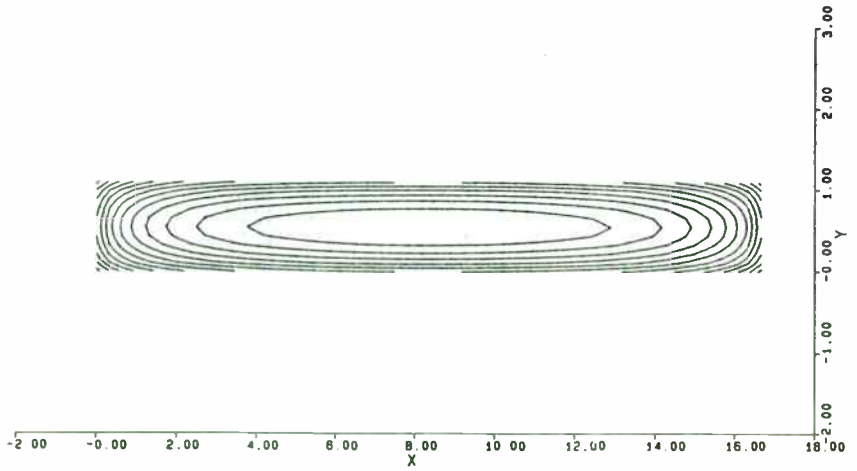


Figure 11. Isothermal Representation of Surface Temperatures shown in Figure 10. Tmax = 114 C, Tmin = 87 C. 2 C/isotherm.

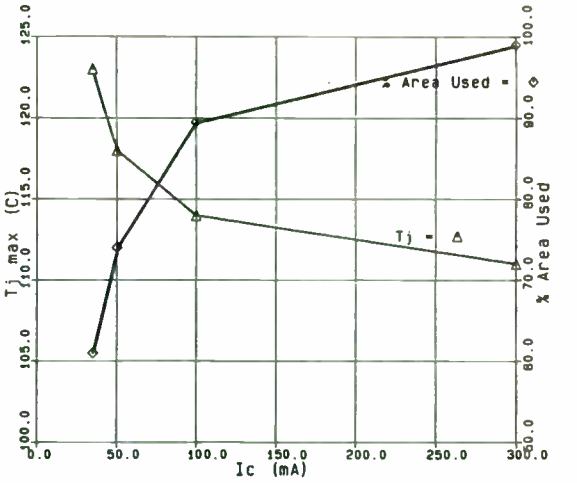


Figure 12. Effects of tradeoff in current vs. voltage for constant power dissipation for the benchmark model (Figure 4.).

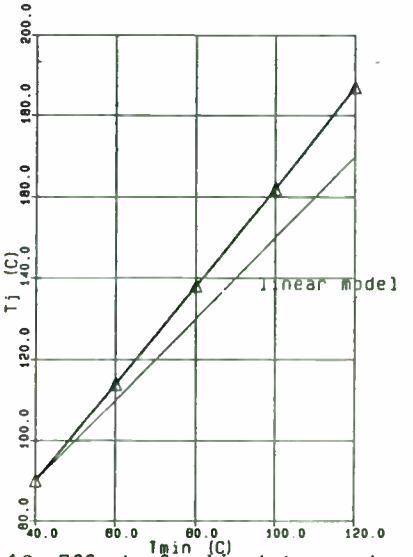


Figure 13. Effect of ambient temperature on maximum junction temperature Tj for the benchmark model (Figure 4.).

The impedances (Zsc and Zoc) of the distributed circuits in Figures 1 and 2 are shown plotted versus freuency in Figures 3 and 4 respectively:

Figure 3.

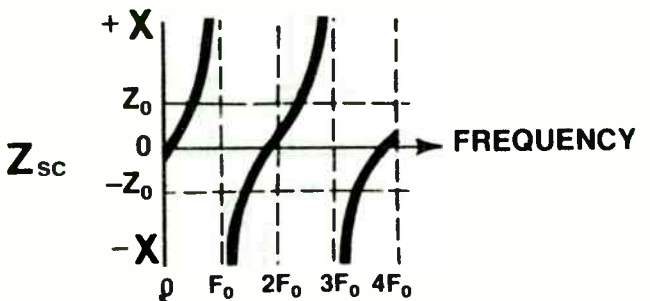


Figure 4.

The multiple parallel and series resonances are unique to distributed elements compared to their lumped element counterparts which have only one resonant frequency.

It should be apparent by now what is meant by the reentrant or periodic nature of distributed resonant elements from Figures 3 and 4 and how they can be used as repetitive band-reject filters to suppress harmonics in an oscillator application. However what might not be obvious is how to achieve parallel resonance at the fundamental oscillator frequency (F1) and series resonance at the even and odd harmonics of that frequency. The distributed circuit shown in Figure 5 is the key structure and the initial step in designing such a filter.

There is a unique characteristic about a shorted quarter-wave resonator. No matter where it is tapped along its length, it will always be parallel resonant.

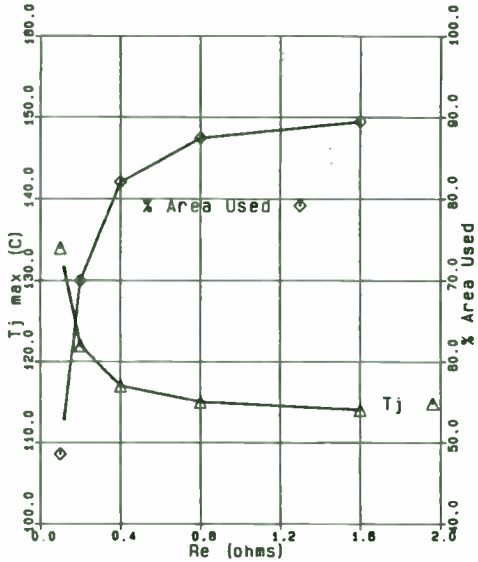


Figure 14. Effect of total Re in the case of uniform ballasting on Tj, maximum junction temperature (see Figure 4. benchmark model).

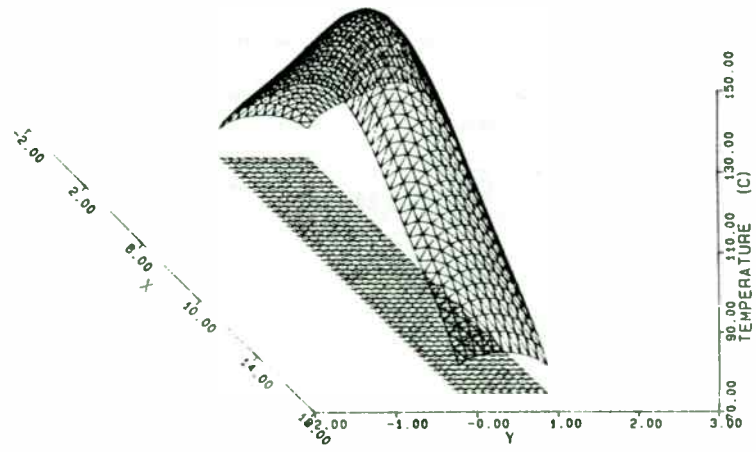


Figure 15.

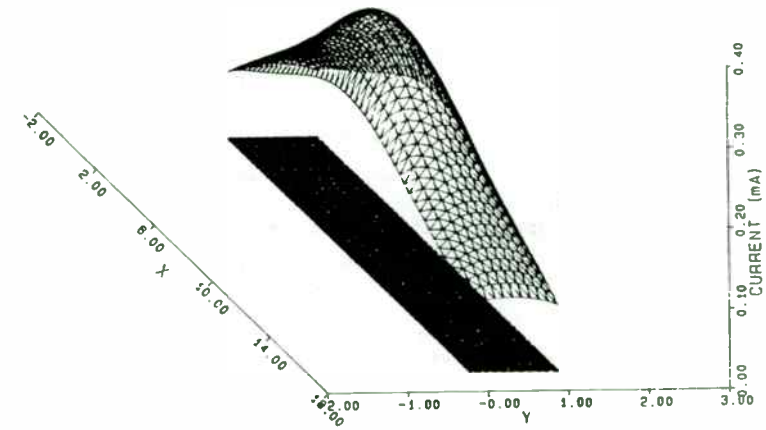


Figure 16.

Temperature and Current Distributions for the benchmark under standard conditions with uniform ballasting and total Re = .1 ohms.

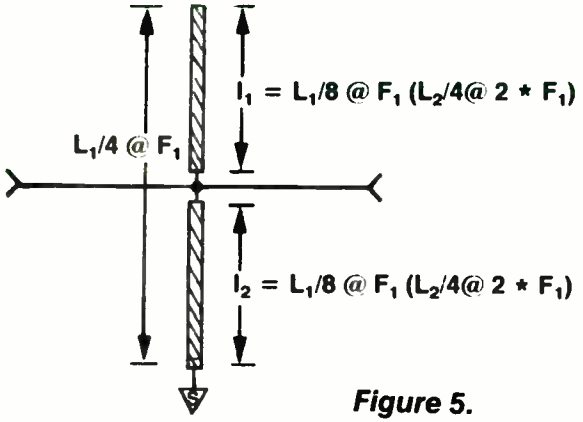


Figure 5.

The reason for this is that shorted transmission lines less than (L/4) (i.e. l2) will always be inductive and open transmission lines less than (L/4) (i.e. l1) will always be capacitive. If (l1 +l2) = (Ll)/4 then the two resultant reactances (or susceptances) will be equal in magnitude and opposite in sign on the imaginary impedance axis. Thus the shunt configured circuit in Figure 5 is parallel resonant at the frequency Fl. This can be readily proved by substituting l = (Ll)/8 and L = Ll into Eq.2 and Eq.3 which yields:

Zsc = jZo and Zoc = -jZo

Since it makes little difference where a shorted quarter-wave transmission line is tapped to achieve a parallel resonance, the next question might be why was the circuit in Figure 5 configured such that l1 = l2 = (Ll)/8? The answer to that is simple. Series resonance (band-reject) will occur: when l1 = L/4 at 2*Fl, (3/4)*L at 6*Fl, (5/4)*L at 8*Fl,..... and when l2 = L/2 at 4*Fl, L at 8*Fl,..... Thus, the circuit in Figure 5 exhibits the composite impedance of that shown in Figures 3 and 4: where Fo = 2*Fl.

The filter structure in Figure 5 is, however, only good for filtering "even" harmonics of the desired or band-pass frequency Fl. All the "odd" harmonics (3*Fl, 5*Fl, 7*Fl....) cannot be suppressed as easily as ALL the "even" harmonics are with a SINGLE tapped (Ll)/4 distributed structure shown in Figure 5. This is due to the fact that Fl is, in a broad sense, an "odd" harmonic (1*F) and conflicts with the requirement that Fl be band-passed while the remaining "odd" harmonics (F3, F5, F7.....) be band-rejected. Thus to achieve this design constraint each "odd" harmonic requires one unique shunt (Ll)/4 distributed structure tapped progressively closer to the open end of the transmission line the higher the "odd" harmonic frequency.

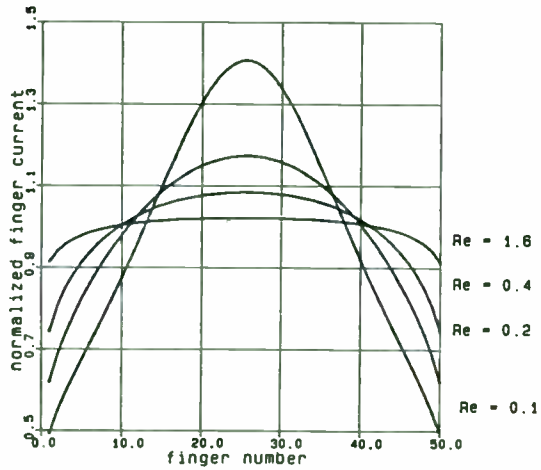


Figure 17. Effect of total Re in the case of uniform ballasting on finger current (ie., current injection along cell length) for the benchmark model.

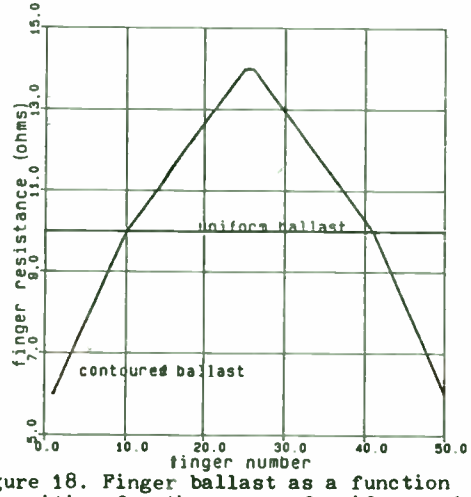


Figure 18. Finger ballast as a function of position for the cases of uniform and contoured ballasting.

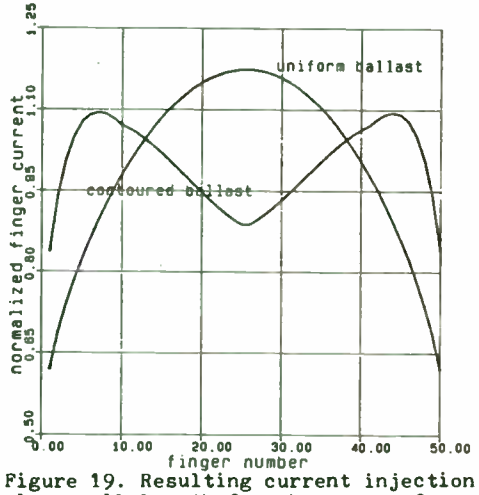


Figure 19. Resulting current injection along cell length for the cases of uniform and contoured ballasting (Figure 18).

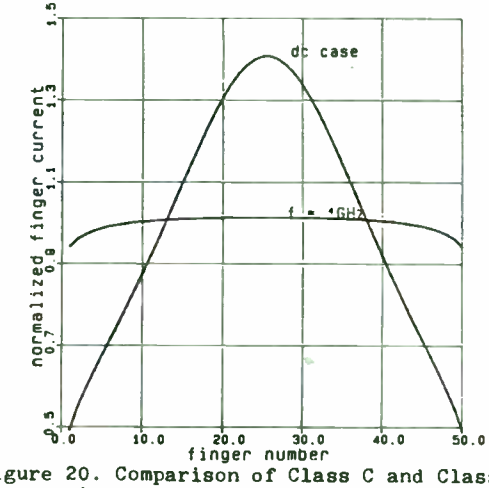
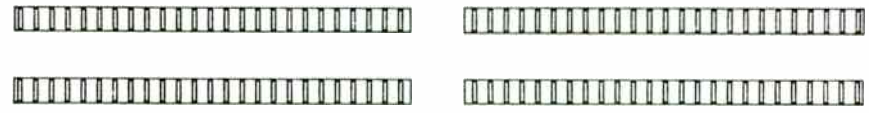


Figure 20. Comparison of Class C and Class A operation for the case Re = 0.1 ohms.

CELL NO.	MAXIMUM				MINIMUM				% AREA
	TEMP	F#	CURRENT	F#	TEMP	F#	CURRENT	F#	USED
1 : 1	98.	15	1.081	15	81.	1	0.878	2	97.220
1 : 2	98.	15	1.081	15	81.	1	0.878	1	97.220
2 : 1	98.	11	1.081	11	81.	25	0.878	25	97.220
2 : 2	98.	11	1.081	11	81.	25	0.878	25	97.220



CELL NO.	MAXIMUM				MINIMUM				% AREA
	TEMP	F#	CURRENT	F#	TEMP	F#	CURRENT	F#	USED
1 : 1	114.	26	1.135	26	87.	50	0.811	50	89.513

Figure 21. Illustration of cell splitting and multi-cell handling by TEMP3D Total base area, and emitter areas are conserved. Cell spacing in top model is 1.0 mils edge to edge.

Figure 6 shows these structures graphically depicted to the 7th harmonic:

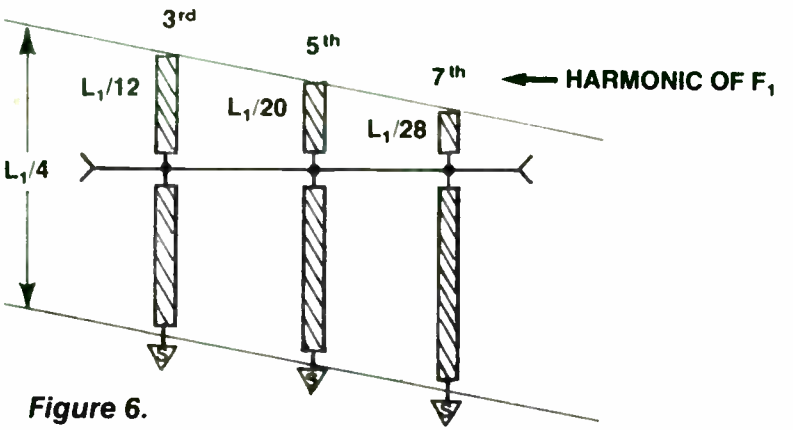


Figure 6.

The length of each of the "open" sections of the distributed structures must be L/4 (series resonance, Zoc = 0) at the desired "odd" harmonic frequencies. This open-stub length (Loc) translates to the fundamental wavelength (L1) using the following equation:

$$Loc = (L1)/(4*N) \qquad \text{(Eq.6)}$$

where: N = the "odd harmonic number (i.e. 3,5,7.....)

Combining the structure in Figure 5 with any or all of the tapped (L1)/4 structures in Figure 6 constitutes a filter that can be tailored to a prescribed harmonic suppression. The author used this technique to reduce the distortion in a 500 MHz SAW resonator oscillator. Only two (L1)/4 structures were required; the "even" one in Figure 5 and the 3rd harmonic "odd" one in Figure 6. A photograph of the transmission characteristics of this filter is shown in Figure 7.

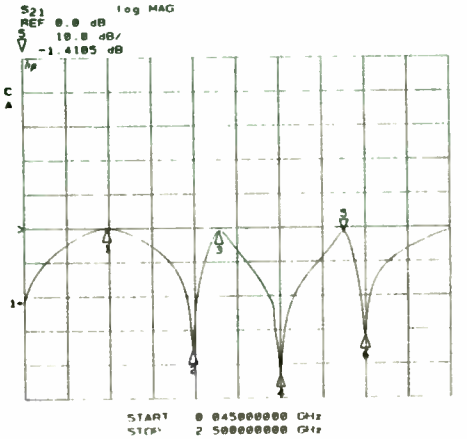


FIGURE 7.

Note the parallel resonance at the 500 MHz fundamental and the series resonance at the 2nd (1000 MHz), 3rd (1500 MHz), and 4th (2000 MHz) harmonics. Figure 8a shows the oscillator without the filter, and Figure 8b shows the oscillator with the filter. Thus, with a few shunt distributed elements, an effective yet

CELL NO.	MAXIMUM				MINIMUM				% AREA
	TEMP	F#	CURRENT	F#	TEMP	F#	CURRENT	F#	USED
1 : 1	166.	28	1.384	28	101.	50	0.865	50	83.758

CELL NO.	FINGER NO.	Y	TEMP	CURRENT
1 : 1	28			
		2.718	132.	0.891
		5.487	143.	0.960
		8.256	152.	1.062
		11.029	159.	1.219
		13.800	164.	1.328
		16.571	166.	1.384
		19.342	164.	1.328
		22.113	159.	1.219
		24.884	152.	1.062
		27.655	143.	0.960
		30.425	132.	0.891

CELL NO.	FINGER NO.	Y	TEMP	CURRENT
1 : 1	50			
		2.718	101.	0.875
		5.487	106.	0.781
		8.256	108.	0.826
		11.029	112.	0.878
		13.800	113.	0.906
		16.571	114.	0.917
		19.342	113.	0.906
		22.113	112.	0.878
		24.884	108.	0.826
		27.655	106.	0.781
		30.425	101.	0.875

CELL NO.	MAXIMUM				MINIMUM				% AREA
	TEMP	F#	CURRENT	F#	TEMP	F#	CURRENT	F#	USED
1 : 1	114.	28	1.135	28	87.	50	0.811	50	89.513

CELL NO.	FINGER NO.	Y	TEMP	CURRENT
1 : 1	28			
		2.718	102.	0.849
		5.487	107.	0.858
		8.256	110.	1.033
		11.029	112.	1.089
		13.800	114.	1.124
		16.571	114.	1.135
		19.342	114.	1.124
		22.113	112.	1.089
		24.884	110.	1.033
		27.655	107.	0.858
		30.425	102.	0.849

CELL NO.	FINGER NO.	Y	TEMP	CURRENT
1 : 1	50			
		2.718	87.	0.811
		5.487	90.	0.880
		8.256	92.	0.924
		11.029	93.	0.953
		13.800	94.	0.970
		16.571	94.	0.978
		19.342	94.	0.970
		22.113	93.	0.953
		24.884	92.	0.924
		27.655	90.	0.880
		30.425	87.	0.811

Figure 22. Illustration of device scaling. All horizontal dimensions of cell on the left have been reduced by a factor of 2. Benchmark model is seen on the right.

simple filter can be designed without complex synthesis and fabricated without tedious "tweaking" in manufacturing.

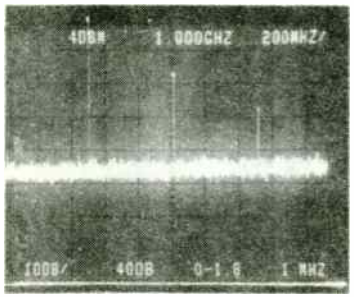


FIGURE 8a

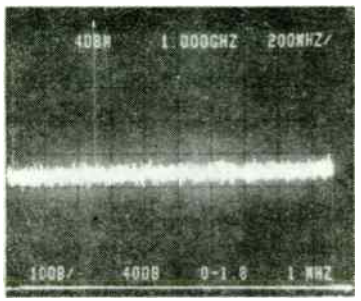


FIGURE 8b

From the filter response shown in Figure 7, it should be apparent that the harmonic attenuation (suppression) is finite (i.e. >30 dB), not infinite as predicted by Eq.2 or 3, where Zin = 0. Equations 2 and 3 are derived from Eq. 1 which assumed no loss (dissipationless line). Distributed quarter-wave (L/4) resonant lines have loss that can be calculated if the equivalent unloaded Q value is known.

The equation for the equivalent (lumped L/C) unloaded Q for an "open" L/4 resonant line can be derived by equating its derivative of impedance (with respect to angular frequency (2*Pi*F)) with the derivative of impedance of a lumped L/C series resonant circuit. The resultant of that mathematical computation divided by Rs (series resistance) yields:

$$Qu = (Pi/4)*(Zo/Rs) \qquad \text{(Eq.7)}$$

Eq.7 can be used to calculate Rs at any harmonic frequency (Fn) if Qu is known at Fn. The harmonic attenuation (An) at any Fn can be predicted by judicious use of the following equation:

$$An = Rs'/(Rs'+(Ro/2)) \qquad \text{(Eq.8)}$$

Where: Rs' = the equivalent series resistance of all the L/4 and multiple L/4 lines with series resistance at Fn.

Ro = Source and load resistance assumed equal (i.e. 50 ohms)

Applying a similar procedure as used to obtain Eq.8 an equation for insertion loss can be created as follows.

The equation for the equivalent (lumped L/C) unloaded Q for a "shorted" L/4 resonant line can be derived by equating its

derivative of susceptance (with respect to angular frequency) with the derivative of susceptance of a lumped L/C parallel resonant circuit. The resultant of that mathematical computation divided by G (parallel conductance) yields:

$$Qu = (Pi/4)*(Rp/Zo) \qquad \text{(Eq.9)}$$

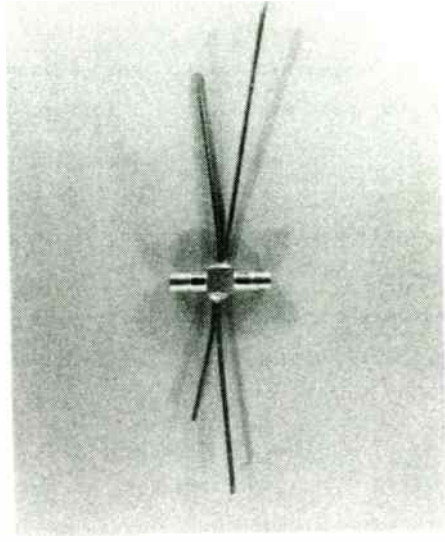
Where: Rp = 1/G = parallel resistance.

Eq.9 can be used to calculate Rp at the fundamental frequency (F1) if Qu is known. The insertion loss (I.L.) can be predicted using the following equation:

$$I.L. = (Rp/m)/((Rp/m) + (Ro/2) \qquad \text{(Eq.10)}$$

Where: m = number of shunt (L1)/4 resonators in the filter. (i.e. m=2 for the filter in Figure 7.)

The filter in Figure 7 was configured with .047 inch diameter semirigid coaxial cable with a dielectric constant Er = 2. Different transmission line media, whether coax, stripline, microstrip, etc. will have different Qu's. By configuring some (Ln)/4 "open" resonant lines in the desired transmission line media and making harmonic attenuation (An) measurements at each harmonic frequency (Fn), the unloaded Q's (Qu) can be calculated using Equations 7 and 8. Rs' reduces to Rs in a single (Ln)/4 resonant line. n = desired harmonic number (i.e. 1,2,3,4....).



Microwave Integrated Receiver for the Morelos Mexican Satellite System

by
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ABSTRACT

This article describes the characteristics and design procedure of a microwave integrated front-end for the Morelos Mexican Satellite System. The receiver works at Ku band and provides a 0.9-1.4 GHz signal to the modem. The main application of this receiver is educational television reception. However, the system can be used for thin route telephone and data transmission applications.

INTRODUCTION

The Morelos Satellite is a hybrid system for both C and Ku Band[1]. It is expected to be fully operational at the beginning of 1986. The satellite system is composed of two satellites, Morelos I located at 113.5°, and Morelos II located at 116.5° West. The two satellites are versions of the HS376, the most purchased commercial communications satellite in the world. Morelos is the first Hughes Aircraft satellite to use a planar array for reception of the four Ku band channels, each one with 108 MHz bandwidth, covering the country with a minimum effective isotropic radiated power (KuEIRP) of 44 dBw. The transmit and receive beams for C band and the transmit beams in Ku band are provided by a 6-foot wide shared aperture grid antenna with two polarization selective surfaces. The front surface detects horizontally polarized signals and the rear detects vertically polarized signals. Two separate microwave feeds are used for both polarizations. The C band structure of the satellite consists of 12 vertically polarized narrowband channels with 36 MHz bandwidth each and six horizontally polarized with 72 MHz bandwidth. The front-end described in this article is designed for the Ku frequency band of the Morelos System. Figures 1 and 2 show the physical structure of Morelos and its EIRP "footprint" respectively.

II. LINK CALCULATIONS

In order to define the technical specs of the Ku band front-end, a computer program that provides the main parameters of the link was developed. This program is particularly adapted to the characteristics of the Morelos Satellite system and gives important information about the receiver's performance under several input conditions. Fig. 3 shows a flow-diagram of the computer program. The output data are given graphically and can be adjusted for different input data according to the designer needs.

HIGH POWER FILTERS

Specsmanship & Design Considerations

By Dick Wainwright, Chief Scientist
Cir-Q-Tel, Inc.

Abstract:

Blivetry*: power; feasibility; Q: selectivity; gradients; hot spots; energy storage; contaminants; ionization; breakdown; peak-average; C.W.; A.M.; % modulation; F.M.; etc.; volt-amps; connectors; size; weight; heat generation, flow & sinking; ionization; impacting; altitude; humidity; salt spray; insulation; shock; vibration; harmonic content; rejection; source & load; EMI; form factor; skin depth-plating; dissipation factor; dielectric strength; topology; susceptibility; losses; volts; amps; volt-amps; Q; MTBF; manufacturers ratings & reality; heat; heat flow; - - all are but a smattering of the flow of words/thoughts that haunt every sensible designer of high power devices. (Notice: certain key words were repeated to emphasize their importance.)

---

*Blivetry: The art of defying the basic laws of physics by forcing two or more objects to fit into the same space - analogous to fitting ten pounds of parts into a one pound container.

Customers, bless them, generally think of filters as bandaids - one often hears the uninformed say, "Anyone can design filters - the textbooks are full of tables of element values". That is true, but volts and amps and concomitant happenings make a difference. "The ratings", not the values, are of fundamental importance in power handling devices, design and application. A little experience usually results in a lot of smoke testing.

An intimate knowledge and an awareness bordering on paranoia, plus considerable experience are fundamental requisites.

The writer has on innumerable occasions lost the "first go-around" on a project bid on the basis of: price, size, weight and exceptions prudently taken, in some instances, because the user did not know or furnish such very important information as:

a. Harmonic content of transmitter power output relative to fundamental power
b. Possible incompatibility of specified connectors with specified power and load conditions
c. The amount of surface area available for heat conduction/radiation and/or availability of cooling air. Assuming that cooling air is available, the rate of air flow, pressure, as well as the temperature of the cooling air, must be known.

Figures 4 and 5 are provided by the program and show the behabior of carrier to noise ratio (C/N) with respect to two basic parameters, the low noise amplifier noise figure F_{LNA} and the low noise amplifier gain G_{LNA} for different antenna gains. Fig. 6 shows the relation between C/N and S/N for a typical TVRO receiver (Microdyne 1100 TVR)[2].

It can be seen from fig.4 that for F_{LNA} = 3 dB, C/N is around 19 dB. According to Fig.6 this value fo C/N would give a S/N of more than 50 dB which would imply a good TV reception; however, if the sensitivity of the system given by Equation 1 is taken into consideration for the case of the Morelos System with a KuEIRP of 44 dB, it is observed that for F_{LNA} = 3 dB there is a minimum acceptable operational margin (OM) of around 3 dB. The operational margin is given by Equation 2 as:

$$s(dBm) = (\text{Noise Floor} = -174\ dBm) + F_{LNA} + 10 \log_{10} BW \qquad 1)$$

$$OM(dBm) = I_{LNA} - S, \qquad 2)$$

where BW is the satellite channel bandwidth, which is 500 MHz for Morelos (11.7 - 12.2 GHz), and I_{LNA} is the signal level at the LNA's input and is given as:

$$I_{LNA}(dBm) = EIRP + \text{Free Space Loss} + G_{ANT}, \qquad 3)$$

where G_{ANT} is the earth station antenna gain.

For F_{LNA} = 3 dBm and BW = 500 MHz, we obtain S = -84.02 dBm and for EIRP = 44 dBW free space loss of -205.18 dB and GANT = 50 dB; I_{LNA} = -81.18 dBm. This will result in an OM according to Equation 2 of around 3 dB.

Taking into account the results of the above described example it can be observed that if a F_{LNA} = 6 dB is chosen OM would be around zero; e.g., the input signal is immersed in noise. This situation is not desirable at all. In order to increase the operational margin OM, I_{LNA} should increase. It can be seen from Eq. 3 that EIRP and G_{ANT} should in turn be increased. However, increasing EIRP is not feasible because it is fixed from the satellite specs, and G_{ANT} is difficult to increase beyond 50 dB, at least for Ku band commercial antennas. The most practical possibility to improve OM is to reduce F_{LNA} to the minimum and try to push G_{ANT} beyond 50 dB with the minimum possible losses in the antenna feed system.

Fig. 5 shows the direct influence of G_{LNA} on the C/N value. Available Ku band commercial antennas with 40-50 dB gain are considered for this figure. It can be observed that for F_{LNA} = 2 dB the LNA's gain could be around 35 dB to obtain adequate values of C/N. This implies that increasing the gain beyond 35 dB at the 11.7-12.2 GHz frequency band

d. Heavy shock and vibration specifications were specified along all three major axes when in fact the application, under power, was indoors and fixed.

e. Specifications indicating unrealistically low values of device VSWR (e.g. 1.1:1) when in fact the filter would in practice be operating continuously into loads of never less than 2:1 and often in excess of 3:1 VSWR. (In some cases an infinite VSWR of any phase) Specified selectivity, i.e., ratio of "f" low-reject/"f" high pass ($f_{p(high)}$ was given as very nearly 1:1; and it is not unusual to find specifications indicating selectivity ratio values of 1.01:1, 1.02:1, etc. When using a number of filters to cover a broad range of frequencies it is usually best to uniformly distribute the power pass band and reject to pass ratios to avoid undue stress on any of the filters: see Example (1).

f. Other mitigating relationships that, taken as whole, result in unrealistic designs.

Taking it from the top, a-f:

a. Harmonic content of transmitter output:

Typical solid state transmitters, of recent vintage, can be expected to yield harmonic power levels of (push-pull final through combiner to 50 ohms unbalanced): Table 1

TABLE 1

Harmonic Order		Level dBc	Harmonic watts/KW (fundamental)
2nd	:	-18	15.8
3rd	:	-12	63.1
4th	:	-21	7.9
5th	:	-18	15.8
6th	:	-22	6.3
7th	:	-21	7.9
8 - 13	:	Avg. -22	37.8) Avg.: 6.3W/harmonic

Total Harmonic Power: 154.6 watts/KW fundamental power

As an aside, note at this juncture that the customer may wish to use a ferrite isolator at the transmitter output to obtain a well-matched transmitter output, but, through oversight, may neglect the fact that most isolators are frequency sensitive, resulting (possibly) in excessive heating by harmonics, resulting in isolator burn-out and/or additional harmonic generation caused by the ferrite being operated near the Curie temperature of the materials, etc.

(b) Connectors power rating insufficient for application. Most connector manufacturers haven't the foggiest idea of how much power/apparent power their connectors will safely handle. Current ratings, not voltage ratings, are generally the problem drivers. Z_o is of little consequence in systems working with very high VSWR values - of course they are directly related.

does not provide any further improvement.

From the link analysis we can define the design requisites of the receiver for Morelos in the Ku band: Maximum $F_{LNA} < 3$ dB; desirable $G_{ANT} \geq 50$ dB and $G_{LNA} \geq 30$ dB.

SYSTEM INTEGRATION

Fig. 7 shows the basic structure of the Ku band receiver for the Morelos Satellite system. We are using an integration approach that combines monolithic microwave integrated circuit (MMIC) subsystems (basically LNA blocks) manufactured by NEC with other hybrid microwave circuits assembled in our laboratory. The technical specs for the LNA-MMIC are[3]: Bandwidth - 11.7-12.2 GHz, F_{LNA} = (MC5806A) - 2.2 dB F_{LNA} (MC5806B) - 3.0 dB G_{LNA} = 17 dB. Considering these specs and the design requisites defined before, it can be seen that if two LNA modules are connected in cascade we will achieve the design objectives: $G_{LNA} \geq 30$ dB and $F_{LNA} \leq 3$ dB. Careful packaging and assembling of the MMIC modules is an important factor to obtain a successful design. Improper assemblies would result in a loss of gain per module of around 2 or 3 dB and instabilities in noise figure.

The picture shown in figure 8 corresponds to the subassembly of the Ku band integrated receiver. Local oscillator, mixer and intermediate frequency amplifier are respectively MC5808, MC5807 and MC5805 NEC hybrid modules. The band pass filter and other interstage modules are designed in our laboratory.

CONCLUSIONS

The Ku band front-end described in this article will be tested directly on the Morelos System when the two satellites are fully operational around the first trimester of 1986. Final testing of the modules will provide information about the conveniences of using MMIC instead of conventional hybrid modules from the economic and efficiency points of view. The program developed for the link analysis of Morelos has been very useful in defining the receiver's specs and it is expected to improve it to cover more subtle aspects of the parameters of the link.

ACKNOWLEDGEMENTS. We thank Ricardo Chavez, Benjamin Ramirez and Isabel Alcaraz for their valuable participation in the final manuscript.

REFERENCES

1) Comparative Analysis of C and Ku Frequencies for the Mexican Satellite Communications Domestic System (In spanish) Hughes Document Ref 43 (82) 001132/F2017, March, 1982, Hughes Aircraft Co.

Given the fact that most filters are "reflective devices" i.e. produce attenuation by reflection of power rather than being absorptive, absorptive filters are generally much more expensive and generally considerably larger than reflective devices. However, in many UHF and above, frequency range applications the use of harmonic absorptive filters may make a lot of sense.

(c) How much surface area should one allow for the cooling of high power filters, and, if cooling air is available, what is its pressure and rate of flow?

First one may make the assumptions:

1. The maximum power vs. connector type is in the order of 2/3 of the cable attached, derated appropriately.
2. Normally a high power filter ("hot" surface temperature) is designed such that the hot surface temperature of the filter does not exceed ambient C° + 50°C with a heat sinking plate average temperature of no more than ambient air C° + 10°C= +95°C max. Cooling air, if available, should not exceed an effective temperature of +80°C; hence, air speed may be an important consideration as the air approaches the filter hot spots.

In many cases substantial size fins may be required but fins are not very effective in cramped air flow spaces - convection air currents must be free to circulate if convection cooling represents a substantial portion of the cooling means, and surrounding heat conducting surfaces may need to have rough surface to "wipe" the heat out of the circulating air.

(d) Heavy shock and vibration specifications along all three major axes, i.e., G forces applied to coaxial filters should be studied carefully and if at all possible, the strong G forces should be confined to the smaller dimensions of the coaxial structure. Minimal forces of no more than 5G, preferably, and no more than 10G max. (11 m/sec. std. shock specifications) on the length should be applied to coaxial high power filters of substantial size, plus consideration as to the adequacy of mounting hardware and supporting structures is essential.

(e) Selectivity, time delay, energy storage & electrical (absorptive) losses/heat generation go hand in hand.

Q: The ratio of:

$$\frac{\text{Energy Stored per Cycle}}{\text{Energy Dissipated per Cycle}}$$ of the applied energy

is a critical consideration in the design of all filters in general, and is of great importance in high power filters. For a given loss, the required ratio of Q unloaded/Q loaded is different for every filter design. It is not uncommon for certain designs to require inductor Q unloaded values in excess of 500-1000 or more and for capacitors 3500-8000 or more to barely eke out a responsive design, where rejection bandwidths to low loss band edge ratios are quite small, say much less than 1.2:1 for 40-60 dB rejection; almost impossible values

2) Microdyne 110 TVR Receiver Data Sheet, Microdyne Corp., Ocala Florida 1983.

3) MMIC data sheet, MC 5806A, MC 5806B, Nippon Electric Corp. 1984.

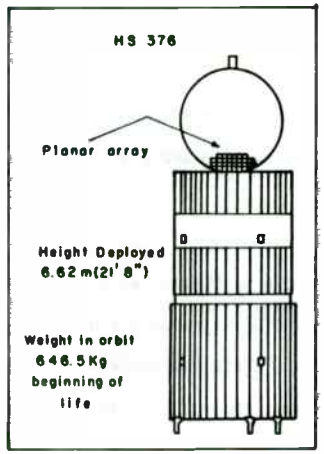

FIG. I) BASIC STRUCTURE OF MORELOS I, II

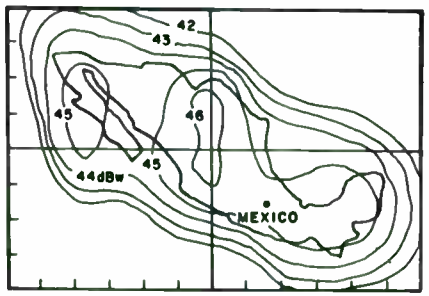

FIG. 2) Ku BAND SATELLITE "FOOT PRINT"

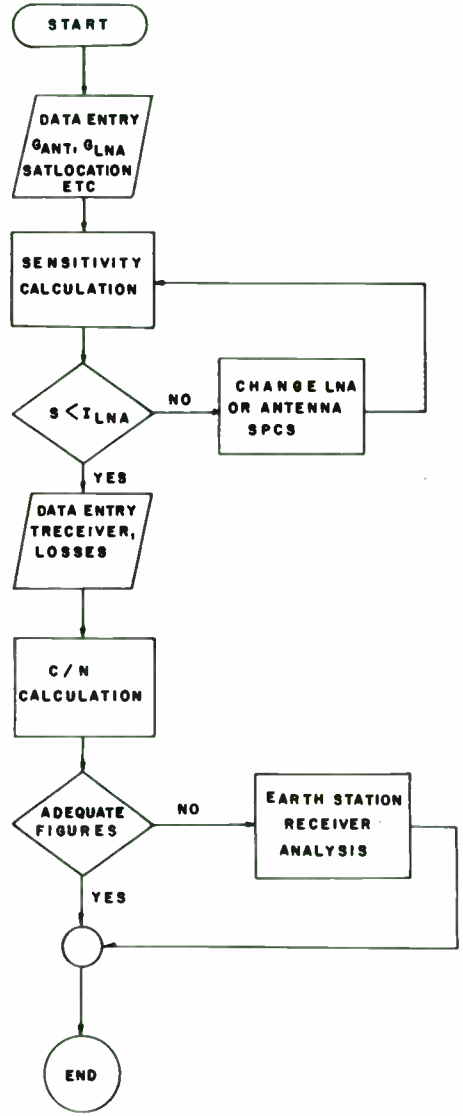

FIG. 3) LINK CALCULATION FLOW CHART FOR MORELOS

of 2000 or more for coil Q and over 10,000-15,000 capacitor Q may be required, but unobtainable because of space, moding and/or frequency limitations.

The Q of coils increases roughly as the square root of frequency, hence generally high frequency filters yield lower losses, given the same selectivity and available space.

For a given loss (see Table 2) the unloaded Q required increases substantially with passband ripple (VSWR), complexity, n and type of filter. (Elliptic, all-pole Chebishev, Butterworth, etc.).

TABLE 2

Selectivity f60dB/f3dB	Nominal VSWR	Filter Design	Representative Qul. for a Given Loss (approx.)	Energy Storage
1.25	1.2	Elliptic (0.01 dB Ripple)	1000	20
1.5	1.35	Chebishev (all-pole) ripple=0.1 dB	650	15
1.7	1.2	Chebishev (all-pole) ripple=0.01 dB	460	12
-	-	Chebishev (all-pole) ripple=0.001 dB	290	-
2.1	1.2	Butterworth	200	10
4.2	-	Bessel		-

Table 2 indicates representative values - not absolutes.

As an example, a 0.01 dB Chebishev (all-pole) filter required approximately $\frac{460}{200}$ -1$\sim$84% more Q than a Butterworth filter for a given loss and the Elliptic filter given has twice the energy storage indicating that voltages and currents are roughly 40% more than in a Butterworth filter.

(f) Other factors of consequence:

(1) Phase linearity vs. f.

(2) Matching of phase: A $\pm$ 5° phase matching specifications may nearly double the price relative to a non-matching phase unit because of the component tolerance problem alignment accuracy and the need to "fix" parts to preclude minute variations in operating environment.

(3) Humidity: High humidity conditions, especially with condensation presents substantial problems.

(4) Altitude: Derating or pressurization with dry nitrogen or sulfur hexafluoride may be forced as a solution. Of course, pressurization eliminates humidity problems.

(5) etc.

The author wishes to thank the following people who were very helpful in the preparation of this paper as well as for the permission of the management of Cir-Q-Tel to publish these data and information:
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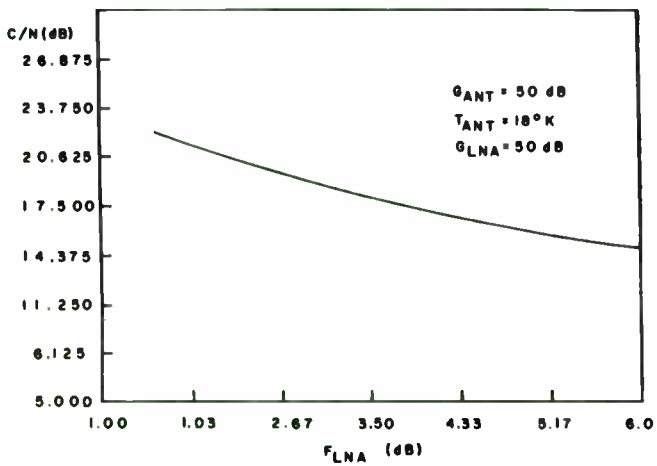


FIG. 4) C/N V.S. F_{LNA} FOR A Ku BAND RECEIVER

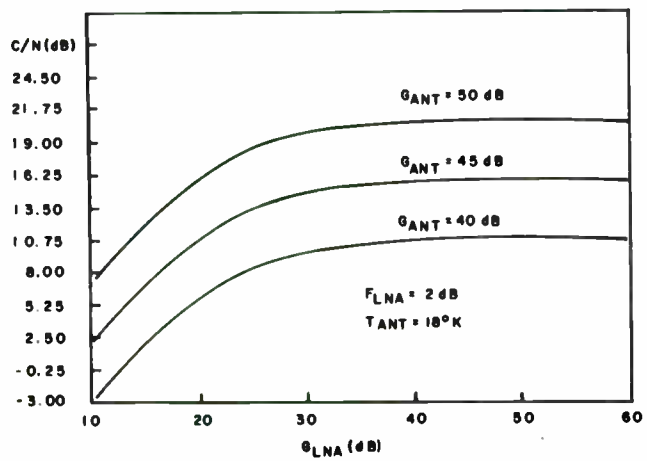


FIG. 5) C/N V.S. G_{LNA} FOR A Ku BAND RECEIVER

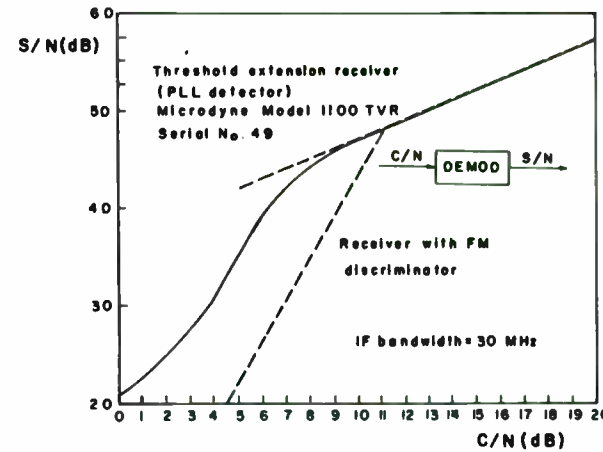


FIG. 6) OUTPUT S/N AS A FUNCTION OF FM DETECTOR INPUT C/N

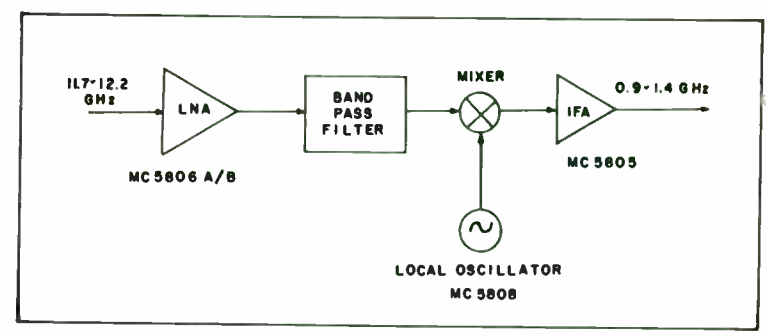


FIG.7) BASIC STRUCTURE OF THE Ku BAND RECEIVER

Addenda to: High Power Filters, Specsmanship
and Design Considerations -
by: R.A. Wainwright

Suppose one wishes to provide filters covering the 100-1000 MHz frequency range that will in turn yield greater than 40 dB attenuation at the second and higher order harmonics; let Nf be the number of contiguous band filters.

First, determine the number of octaves included in this band: 100-1000 MHz (an octave is a 2:1 frequency ratio).

Then:

(1) 100-200 MHz - 1st octave

(2) 200-400 MHz - 2nd octave

(3) 400-800 MHz - 3rd octave

(4) 800-1600 MHz - 4th octave (up to 1000 MHz is all the coverage that is required however,

or

On: octave number is an integer: On 2^{Nf}. If one is to evenly distribute the filters such that: Note all logarithms are to base 10.

[1] $Ki = \frac{fc\ (VSWR)\ high}{f\ operate(VSWR)\ low}$ is about the same for all filters, then given: $KNf = \frac{1000}{100} = 10$

then for each filter Ki

[2] $K(Nf)=10 = Ki^{Nf}_{(1)}$ etc.; Nf=4 (filters minimum)

Then: $\frac{\log 10}{Nf} = \log Ki$

and

Ki=(antilog 10)/4 =1.77827941

(see Fig. E-1)

If 5 filters were to be used, which number will be determined upon evaluation of filters chosen for this task, then, (see Fig. E-2)

if Nf=5

Then

Ki=(antilog 10)/5 =1.584893192

Assuming 4 or 5 filters, then develop Table 1

Table 1

VSWR Passband of Filters 1-4 or 1-5

Ki		1	2	3	4	5
1.78	Nf=4	100-178	178-316	316-562	562-1000	-
1.56	Nf=5	100-158	158-250	250-395	395-628	628-1000

From Fig. E-4 for N(f)=4 or 5 given Ki=1.78 and Ki=1.58 respectively, assuming an elliptic-like response device is compatible with other electrical parameters, ratings, etc.;

Then:

The ratio of the lowest 2nd harmonic frequency (2fL) to highest passband (VSWR) frequency (fcH) for Nf=4 and 5 are

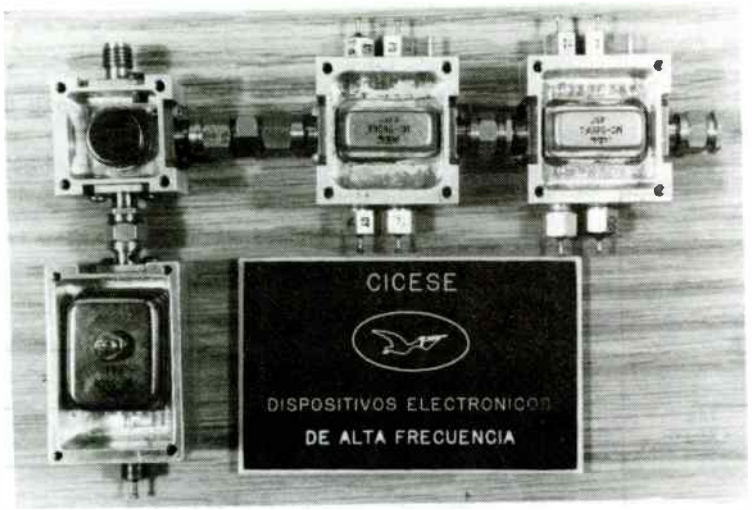


FIG. 8) SINGLE CONVERSION MODULE FOR THE Ku BAND RECEIVER

as given in Table 2

Table 2

	Filter 1 (2fL/fcH)	Filter 2 (2fL/fcH)	Filter 3 (2fL/fcH)	Filter 4 (2fL/fcH)	Filter 5 (2fL/fcH)
Nf=4	200/178= 1.123	1.123	1.123	1.123	1.123
Nf+5	200/158= 1.26	1.26	1.26	1.26	1.26

From Fig. E-2, [(2fL/fcH) -1]=0.123 absissa (frequency scale) and: rejection + return loss= 60 dB ordinate. If return loss is selected as 20 dB VSWR approx. 1.25:1) then 40 dB rejection + 20 dB return loss = 60 dB at 0.123 and 0.26 respectively (absissa value on Fig. E-4).

For Nf=4: at 0.123 (abissa) and 60 dB: rejection + return loss (ordinate) one finds n=11 (elliptic) filter. (see mark "°")

For Nf=5: at 0.26 (absissa) and 60 dB on ordinate. (see mark "x"), n=9 (elliptic) filters, (Fig. E-2).

If on the other hand one wishes to use an all-pole 0.01 dB ripple Chebishev, (of practical construction) ladder network series coil, and shunt capacitors, with no finite frequency traps

Then: for n=19 the ratio: fcH/2fL=1.36 for 40dBc attenuation, (note: Chebishev filters having more than 19 elements, n ≥ 19

are not generally considered practical) it becomes apparent that additional 10-1000 MHz band segmentation may be necessary, (see Fig. E-3 and Table 3.

If: fcH/2fL = 1.36 then solving for Nf (minimum), fL(1)=100 MHz, then 1.36 fcH =2fL =200 MHz

Then fcH(1)=200/1.36=147 MHz

Proof: $1.47^6 = 10 = 10.09029837$

Please be aware that the Tables and graphs given herein Do Not List Theoretical Values.

Figures E-1, E-2 etc. are self explanatory. For all-pole (equi-ripple passband and monotonic reject band) Chebishev filters the reject band attenuation (dB) given by

[Eqn. 5]

$$dB\ @fx = 10 \log\left\{\left[1 + \log^{-1}\frac{\alpha r(dB)}{10}\right]\cosh^2\left[n \cosh^{-1}\left(\frac{fx}{fcH}\right)\right]\right\} fx > fcH$$

where: [fx(dB] is the frequency of x(dB) of rejection α r is the specified pass band ripple (dB)

fcH is the theoretical passband upper end, i.e. equi-ripple band edge. Table 3 gives the (practical) values of the rejection and frequency parameters for 0.01 dB ripple (α r) in the pass band for various practical n odd values. Practical filter intrinsic-matched conditions, VSWR values between 1.25 & 1.4:1 will in general be obtained depending on practical component tolerances. Table 3 lists (practical) ratios of f(xdB)/fcH

HIGH EFFICIENCY POWER AMPLIFICATION WITH OPTIMALLY LOADED HARMONIC WAVESHAPING

by
William McCalpin

High efficiency power amplification is achievable by utilizing harmonic waveshaping techniques to control the collector voltage and current waveforms. By appropriately manipulating these waveforms, the collector-voltage current product is minimized; thus, the power dissipated in the device is reduced. The goal of the waveshaping is to approximate a switching type device which has at least one abrupt step in either voltage or current in order to reduce the time in which both are present. This can be accomplished by pulsing the input to produce a square current waveform and employing the device as a saturated current source with a load network that will create a first approximation of a half-sinusoid voltage.

To elucidate the realization process of the RF amplifier made, five main points are presented: the need for Class F operation, a description of Class F amplification, a Fourier analysis of the waveforms required, the practical realization of the amplifier and the data and analysis from operation and testing.

Power amplification is separated into several modes of operation having various maximum theoretical efficiencies and output powers. In practical terms, operation in all of these classes is in suboptimum conditions due to losses, bandwidth and drive level requirements, and saturation limits of the active device. For our application, an amplifier output level of 50 watts at a single frequency of 425 MHz is used, so it is expected that the practical data should come close to the theoretical limits of the class of operation.

For this particular frequency and output level, Class F was chosen because high efficiency was required and there exists inherent problems with high efficiency operation in other classes at this carrier frequency. Class A linear amplification was avoided because an optimum efficiency of only 50% at maximum power output is possible. This limit exists because the device and the load receive the same amount of power from the supply. The most common form of Class B amplification is a transformer coupled push-pull configuration with a maximum theoretical efficiency of 78.5%. Class C has a maximum efficiency between 85 and 90% depending on the angle of conduction; however, at UHF frequencies it has relatively low efficiency. Class D utilizes the notion of a switch in order to reduce device dissipated power which brings the theoretical efficiency to 100%. However, in order to reasonably simulate the switching action, an active device of 25 to 30 times the fundamental frequency is required. The fundamental frequency of our amplifier was set at 425 MHz which puts the f_T too high for a UHF device to reasonably simulate a switch.

Class F models the device as a saturated current source and utilizes a load network that resonates at harmonic frequencies as well as the fundamental. Class F efficiency is limited in that fully switched waveforms are not possible because the power dissipating in each switching transition cannot be reduced simutaneously. [1] In addition, the waveshaping in Class F requires an

for all-pole Chebishev filters. Where α_r =0.01 dB (passband ripple)

Table 3

Table of Practical Values of f(dB)/fc(high) for x dB Rejection for 0.01 dB ripple, practical, VSWR: 1.25:1 Chebishev all-pole ladder

n	20dB	30dB	40dB	50dB	60dB	70dB	80dB	90dB
7	1.8	2.15	2.75	3.4	4.2	5	-	
9	1.52	1.80	2.15	2.5	3.0	3.5	4.0	
11	1.42	1.73	1.85	2.1	2.42	2.75	3.1	
13	1.32	1.50	1.70	1.90	2.15	2.38	2.65	
15	1.23	1.37	1.55	1.72	1.94	2.15	2.36	2.60
17	1.15	1.28	1.44	1.60	1.77	1.95	2.14	2.30
19	1.12	1.21	1.36	1.52	1.64	1.78	1.90	2.06

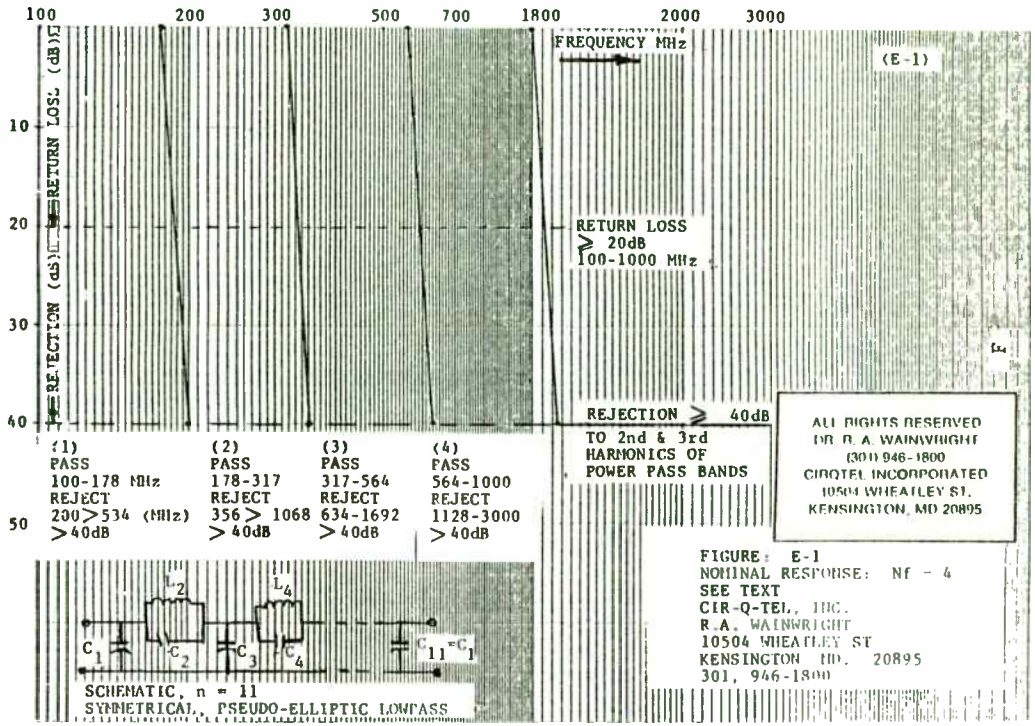
FIG. E-3 might well be a graphical specification for a set of 6 filters spanning the 100-1000 MHz power passband where Ki=1.47 and 40dB is obtained as harmonic rejection. Additional figures show Typical-All-Pole-Lowpass Filters.

Table 4*

Passband VSWR/ripple (dB)

VSWR	2	1.8	1.5	1.4	1.36	1.3	1.24	1.2	1.1	1.05
ripple	0.51	0.37	0.18	0.12	0.10	0.07	0.05	0.035	0.01	0.0026

* Ref: Cir-Q-Tel, Inc. catalog (since 1962) page 35, Table 28



(E)

f_T of only 10 times the fundamental frequency which is more within the limitations of an active UHF device. "Second Harmonic Peaking" is a variation that uses a second harmonic resonator to include the second harmonic component in the collector voltage making a first approximation of a half-sinusoid. The device produces a square collector from a pulsed input. The collector waveforms and a circuit containing the second harmonic resonator are given in Figure 1 below.

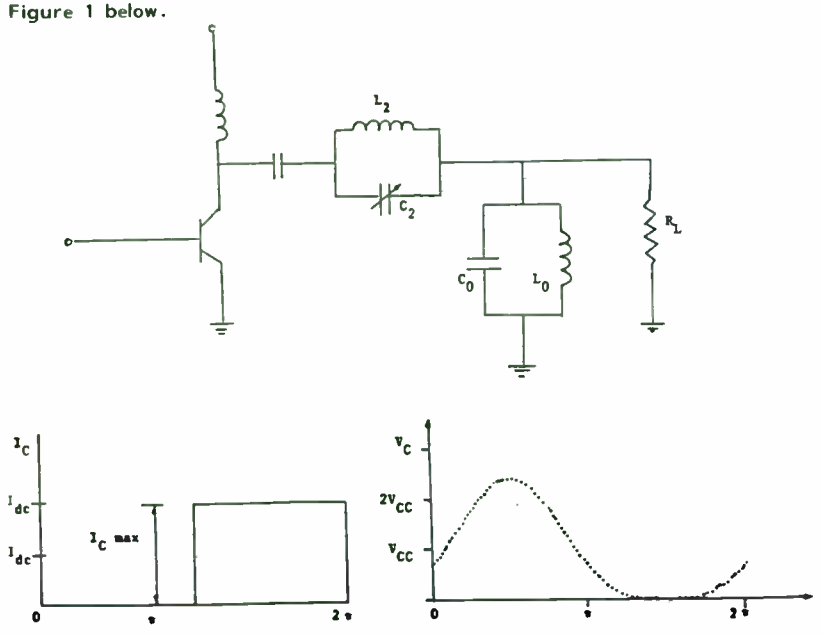


Figure 1

Circuit and waveforms from Fourier Analysis, See Raab, F.H. "Analysis of Second-Harmonic-Peaking Power Amplifier", May 1982, pp 2-3.

The second harmonic resonator in Figure 1 (represented by L_2/C_2) presents a load to the second harmonic which is included in the collector voltage waveform. The fundamental resonator shunted to ground acts as a low-pass filter to the second harmonic removing it from the output, thus the load only dissipates power at the fundamental frequency.

A Fourier analysis of the collector waveforms, given by F.H. Raab[2], clarifies the increase in efficiency due to the harmonic loading. With the second harmonic resonator, the collector voltage waveform is represented by

$$v_C(\theta) = V_{CC} + V_{OM}\sin\theta + V_{2M}\cos 2\theta.$$

Because the second harmonic sine wave is centered in the middle of the voltage waveform it cannot flatten the collector voltage and is therefore not included. Maximum flatness is achieved when the second derivative is zero which implies that the switching transition has become abrupt. The first two derivatives of the collector voltage are given below.

$$\partial v_C(\theta)/\partial\theta = V_{OM}\cos\theta - 2V_{2M}\sin 2\theta$$

$$\partial^2 v_C(\theta)/\partial\theta^2 = -V_{OM}\sin\theta - 4V_{2M}\cos 2\theta$$

By setting the second derivative equal to zero and theta equal to three pi over two it is observed that

$$0 = -(-V_{OM}) - 4V_{2M}(-1)$$

or

$$V_{2M} = -V_{OM}/4.$$

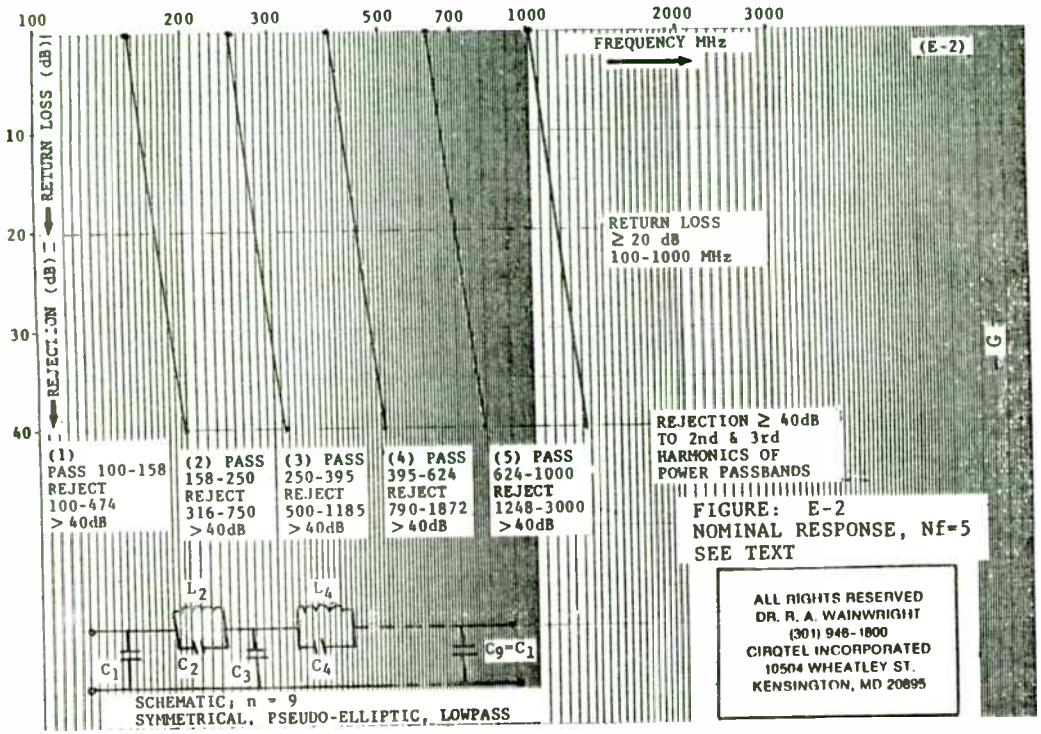


FIGURE: E-2
NOMINAL RESPONSE, Nf=5
SEE TEXT

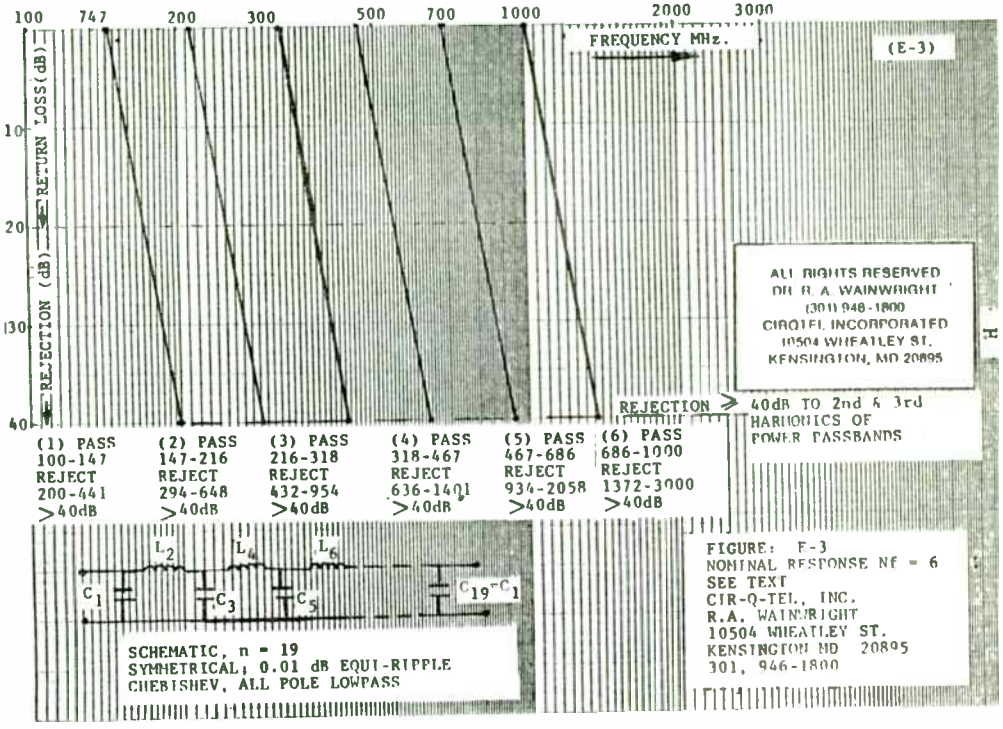


FIGURE: E-3
NOMINAL RESPONSE Nf = 6
SEE TEXT
CIR-Q-TEL, INC.
R.A. WAINWRIGHT
10504 WHEATLEY ST.
KENSINGTON MD 20895
301, 946-1800

If the minimum collector voltage is to be zero, and if V_{2M} is negative one fourth V_{OM} when theta is three pi over two, then

$$0 = V_{C,min} = V_{CC} - V_{OM} - V_{2M}$$

or

$$V_{OM} = (4/3)\, V_{CC},$$

and

$$V_{C,max} = V_{CC} + V_{OM} - V_{2M}$$

or

$$V_{C,max} = (8/3)\, V_{CC}.$$

The power output is therefore

$$P_O = V^2_{OM} / 2R = (8/9)\, V_{CC}^2 / R$$

Since the device produces a square collector current, the values of the DC input current and the peak collector current can be evaluated from the collector voltage.

$$I_{OM} = V_{OM} / R = (4/3)\, V_{CC} / R$$

Because the collector current is a squarewave

$$I_{OM} = (2/PI)\, I_{C,max}$$

or

$$I_{C,max} = (2\ PI / 3)\, V_{CC} / R,$$

and if the DC input is half the maximum collector current, then

$$I_{DC} = (\ PI / 3\ )\, V_{CC} / R.$$

The input power is the product of the supply voltage and current and is therefore

$$P_i = V_{CC} * I_{DC} = (\ PI / 3\ )\, V_{CC}^2 / R.$$

With this information the performance of the power amplifier can now be determined. The collector efficiency of the P.A. is the ratio of the output power to the supply power input or

$$\text{eff.} = P_O / P_i = (\ (8/9)\, V_{CC}^2 / R) / (PI / 3)\, V_{CC}^2 / R$$
$$= (.849) * 100\% = 84.9\%$$

The normalized power output capability is defined as the ratio of the power to the product of the peak collector voltage and the peak collector current or

$$P_{max} = P_O / V_{C,\ max} * I_{C,\ max}$$
$$= (8/9) V_{CC}^2 / R) / (\ (8/9) V_{CC} * (2\ PI / 3)\, V_{CC} / R)$$
$$= (\ 1/2\ PI\ ) = 0.159.$$

For comparison the normalized power output for a Class C amplifier operating at 85% efficiency is calculated to be equal to 0.112. Thus, a high theoretical efficiency and normalized power output is attainable by manipulating the second harmonic component in a Class F amplifier configuration.

A pulse amplifier using the theoretical analysis described above was constructed that operated at 425 MHz with a peak power output of 50 watts. The circuit construction used is given below in Figure 2. The transmission lines shown serve two purposes, one is to match the low output impedance of the

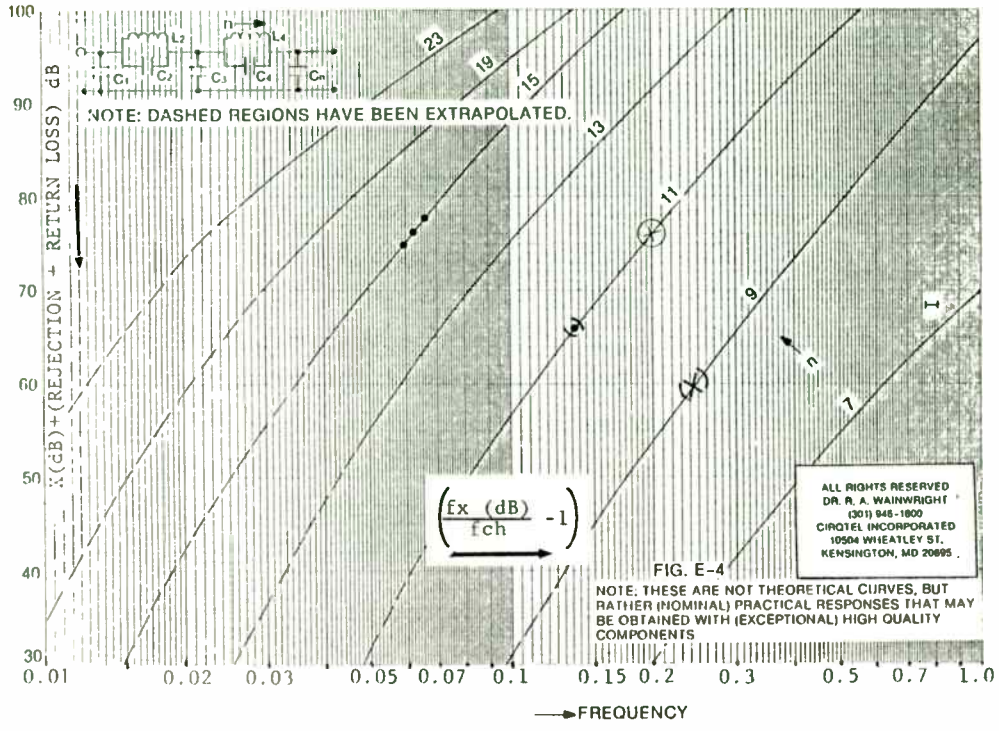
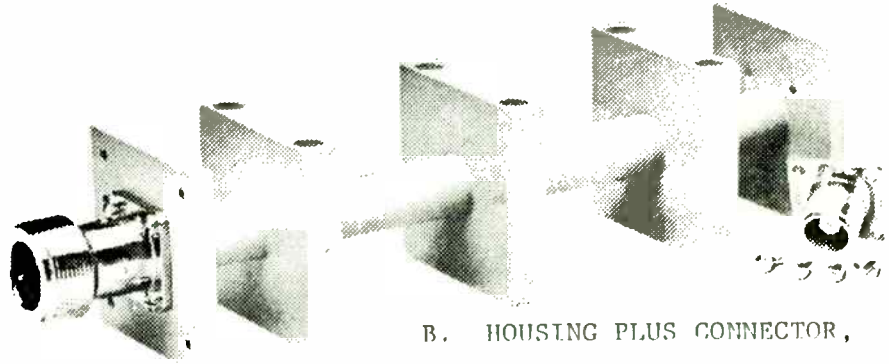


FIG. E-4

NOTE: THESE ARE NOT THEORETICAL CURVES, BUT RATHER (NOMINAL) PRACTICAL RESPONSES THAT MAY BE OBTAINED WITH (EXCEPTIONAL) HIGH QUALITY COMPONENTS

A. FILTER ELEMENT



B. HOUSING PLUS CONNECTOR,

FIG. E-5

LEVY A-Z, n=19 -2KW C.W. 2:1 LOAD-HIGH POWER LOW PASS FILTER; fc = 1.65 GHz

PASSBAND LOSS: 0.1dB TYPICAL

CIRQTEL INCORPORATED

device collector to the standard 50 ohm output, and the other is to present the second harmonic loading required to produce the desired waveforms at the device collector for Class F operation.

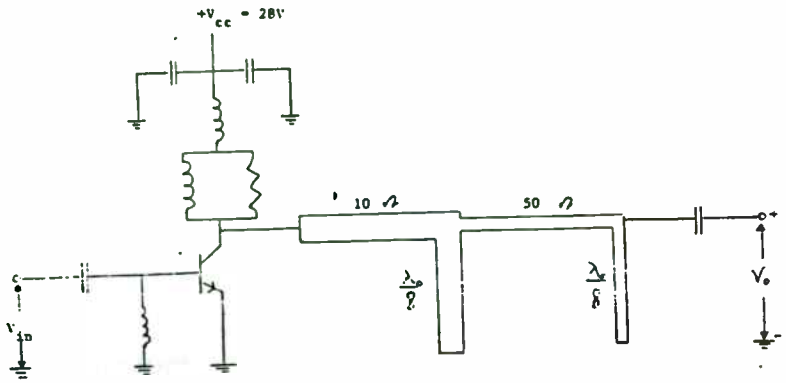


FIGURE 2

The first step in matching the collector impedance of the device used to the circuit output is determinimg the impedance looking back at the device from the transmission lines. A model of the device used in the circuit design is given below.

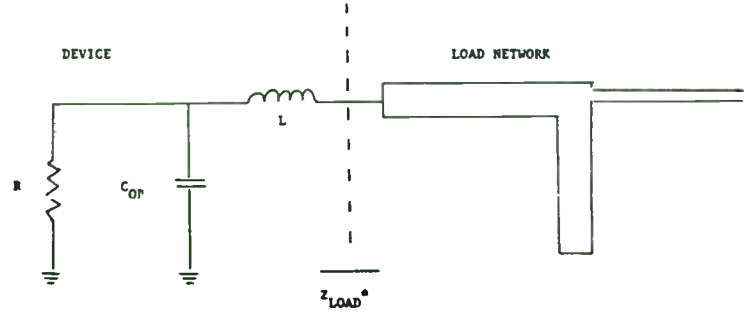


FIGURE 3

Where:

$L = .8$ nH

$C_{OB} = 39$ pF (measured at 1/2 $V_{CC} = 14V$

$R = (V_{CC} - V_{sat})^2 / 2 P_O$, $V_{sat} = 3V$

$= (25)^2 / 2 * 50$ watts $= 6.25$ ohms

$Z_L = 4.45 \angle -.163$

$Z_L = 4.39 - j.721$ at 425 MHz

In order to calculate the circuit elements necessary to match the device collector impedance to 50 ohms and manipulate the second harmonic loading, a computerized circuit optimization program was used. Withe the stubs modeled as shunt capacitors, (at the fundamental frequency) the optimized dimensions for the microstrip lines were calculated. The result values are shown in Figure 4.

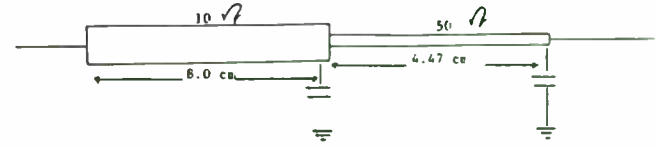


FIGURE 4

The optimized capacitance values were then used in a microstrip stub program which iterates the process of calculating an accurate value of E_{eff} from the dielectric thickness and the E_{rel} of the Teflon fiberglass material. From this, the dimensions of the stubs and the speed of the wave in the line were determined. The two stubs are lambda over eight in length at the fundamental frequency or lambda over four in length at the second harmonic Points A and

B on Figure 5 are open circuited which translate through a lambda over four stub transformation to present a second harmonic short to ground, thus providing the low-pass filter shown in Figure 1. Moving back towards the device collector from the circuit output, the second harmonid shorts at points A' and B' translate through the lambda over four lines to a high impedance which presents a second harmonic load at the collector.

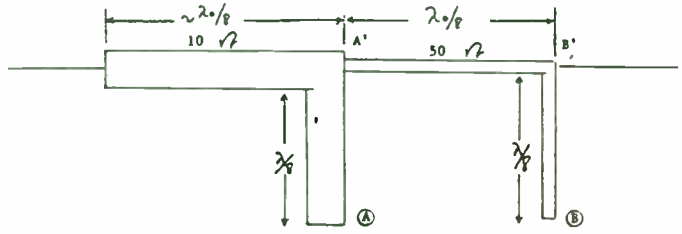


FIGURE 5

The remainder of the circuit elements in Figure 2 are positioned to provide DC supply to the device collector while maintaining stability in the circuit. The series capacitors on the input and output are 510pf chip capacitors for DC blocks. The inductor-resistor branches are ferrite core wire would inductors with a 15 ohm resistor to provide a supply path while presenting an open circuit to the RF power. The left-hand capacitor on the supply branch is a 1500 MF charge storage capacitor to preserve the squareness of the current pulse at the collector by preventing pulse slump and poor rise time. The right-hand capacitor is a .1 MF parallel plate bypass capacitor to bring RF ground to that node to prevent any RF power from entering the power supply or meters.

Along with the circuit in Figure 2, a circuit with exactly lambda over eight transmission lines, and a circuit with the optimized line lengths but using tuning capacitors instead of the stubs were constructed and tested for comparison. The three configurations are shown in Figure 6.

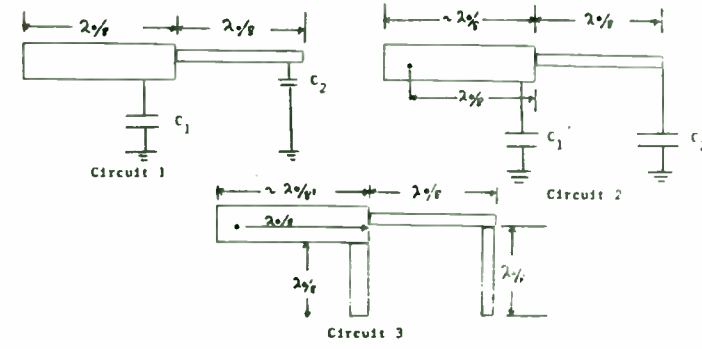


FIGURE 6

The data below shows the device collector efficiency, overall efficiency, and overall gain of the three amplifier configurations, where:

$$\text{Collector efficiency} = P_O \,/\, V_{CC} * I_{D.C.}$$

$$\text{Overall efficiency} = P_O - P_i \,/\, V_{CC} * I_{D.C.}$$

$$\text{Overall gain} = 10 \log_{10} P_O \,/\, P_i$$

High Reliability Electromechanical Switching

by
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Abstract

Recent developments and industry trends in electromechanical switching are presented. Switch life, measured in millions of cycles per switch position, is compared between what is obtainable in the laboratory and what switch manufacturers will guarantee. The maximum frequency of operation, recently extended from 18 to 26.5 Ghz, can be expected to reach 40 Ghz soon, with the connector performance being the critical factor. Switch configurations of the single-pole n-throw and transfer types are standard, and new configurations include the "S-switch" and n-port matrix switches. Drivers are available with TTL and optional BCD decoders built into the switch. Switch design and fabrication techniques are focused on high reliability, including materials and processes for spacecraft and operating vibration levels up to 82 g_{rms}.

Introduction

When the subject of high reliability electromechanical switches comes up, the first question that is usually asked is "why electromechanical switches in the age of solid state?" Comments then follow about the lower reliability of components with moving parts. The purpose of this paper is to present performance characteristics of electromechanical switches currently available that are accurately described by the term "high reliability."

Besides having no moving parts, solid-state switches have the advantages of very fast switching time and small size. The disadvantages of solid state switches generally include higher loss, less isolation, higher SWR, lower power handling, and higher price. Also, solid state switches do not offer many of the options that are available with electromechanical switches.

The type of switches described will be limited to those with coaxial RF connectors only.

Switch Operation

The functional block diagram of an electromechanical switch is shown in Figure 1. The actuator provides the necessary mechanical forces to perform the switching functions, which take place in the RF head. The key parts of the actuator are at least one solenoid (including a coil and plunger), and rockers and springs as required by

Circuit 1: lambda over eight transmission lines with tuning capacitors of

C_1 = 33.4 pF and C_2 = 18.1 pF.

P_{in} = 15 W , P_{out} = 73 W, V_{CC} = 28 V , I_C = 4.3 A

Collector eff. = 60.6%

Overall eff. = 48.2%

Overall gain = 6.9 dB

Circuit 2: optimally matched transmission lines with tuning capacitors of

C_1 = 24.0 pF and C_2 = 8.45 pF.

P_{in} = 8 W, P_{out} = 54 W , V_{CC} = 28 V , I_C = 2.7 A

Collector eff. = 71.4%

Overall eff. = 60.8%

Overall gain = 8.3 dB

Circuits 3: optimally matched transmission lines with lambda over eight stubs.

P_{in} = 7.7 W , P_{out} = 51 W , V_{CC} = 27.9 V , I_C = 2.2 A

Collector eff. = 83.1%

Overall eff. = 70.5%

Overall gain = 8.2 dB

The above data was optimized and measured after careful tuning. The increase in efficiency is believed to be primarily due to an improvement in impedance matching along with a drop in the supply current necessary to maintain the specified output level. As shown in Figure 7 below, the highest efficiency was attained in a tight notch at 425 MHz. This notch is caused by a small dip in the supply current, however, a relatively high level of efficiency was maintained over a 20 MHz bandwidth. Because a trade-off exists between gain and efficiency due to the fact that the collector waveforms can be overdriven to produce sharper edges, the data in Figures 7 and 8 was tuned for optimal efficiency and gain simultaneously to more accurately portray the frequency response shown below[3]

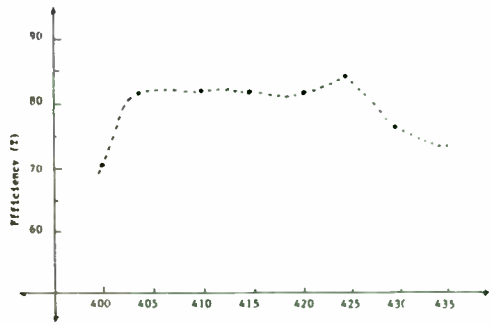

Figure 7

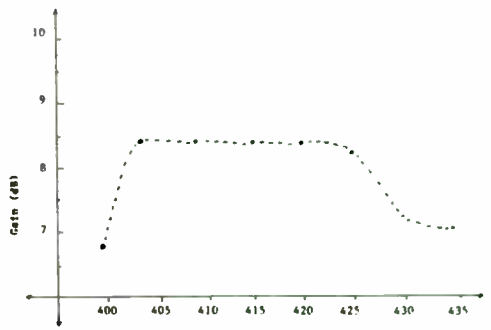

Figure 8

the actuation mode. The RF head includes the RF connectors, center conductor probes, and reeds (contacts).

The driver circuit may be internal or external to the switch, and provides the selected actuation voltages. Optional indicator circuits permit external monitoring of the switch position and operation.

Figures 2 through 4 illustrate the common types of actuation available in an electromechanical switch. In the latching configuration (Figure 2) the switch remains in a position until a new control voltage is applied to another position. In the normally open configuration (Figure 3) no position is connected until power is applied, and the position is disconnected when power is removed. In a failsafe switch (Figure 4) one position will remain connected whenever power is removed.

Design Reliability

The industry standard guaranteed switch life currently being offered by switch manufacturers is one million cycles per position. Much longer life has been obtained in the laboratory, including a Wavecom SP6T switch which performed for more than 27 million cycles per position.

Actuator. The actuator subassembly is the most critical part of the electromechanical switch from a reliability standpoint. Referring to Figure 2, the actuator must provide a vertical force with no horizontal component. Any horizontal force will cause chatter, wear, stress, fatigue, and eventual failure of the switch. A properly designed solenoid has parts which are independent of each other, resulting in a minimum of interference, and is capable of 150 million cycles with no impairment of function.

Reed. The second most important part of the switch is the reed, which provides the electrical contacts. Two processes must be performed correctly on the reeds: heat treating and gold plating. These processes are usually developed and maintained in a proprietary status by each switch manufacturer. In achieving the 27 million cycles per position mentioned above, there was no change in insertion loss.

Temperature. The parts of a switch which are affected the most by temperature extremes are springs and solenoid coils. Standard spring steel will stiffen at -54 deg C and will soften and lose tension at +120 deg C. A special corrosion-free spring material which stiffens at -100 deg C and softens at +370 deg C may be used instead. Coils may be constructed to function from -85 to +190 deg C. Using these techniques, an electromechanical switch will operate from -60 to +135 deg C with no degradation in loss, SWR, or isolation.

Vibration. Wavecom switches in a normally-open multi-position configuration have passed operating tests with up to 82 g_{rms} random vibration.

Spacecraft. The manufacture of high reliability switches for space systems may require more material traceability and process

A spectrum analyzer was used to probe along the series transmission lines to determine the harmonic component at different locations. Figures 9 and 10 show the harmonic response for the optimally matched transmission lines with and without the stubs respectively. (The stubs replaced by tuning capacitors).

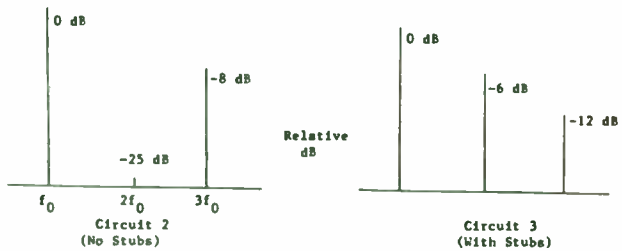

FIGURE 9
Measured at Point C' in Circuits of Figure 6

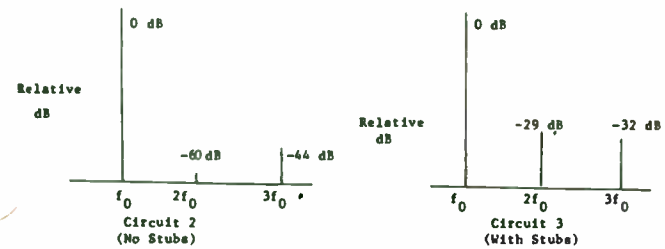

FIGURE 10
Measured at Amplifier Output

As shown in the data above, there is more second harmonic component in the circuit with the stubs acting as a second harmonic load, yet the second harmonic component is removed from both when probed at the output. Since the efficiency increased from Circuit 2 to Circuit 3, it can be concluded that this rise in efficiency is due to the waveshaping caused by the harmonic load. It is also possible that a better impedance match resulted from using the stubs; however, the junctions of the stubs with the lines can only at best be approximated in a practical sense and is therefore difficult to determine for certain.

Thus, it has been demonstrated that high efficiency and power output are available in practical terms at a UHF radio frequency of 425 MHz. At this carrier frequency, a collector efficiency of 83.1% with a gain of 8.3 dB was achieved using the second harmonic waveshaping techniques and impedance matching described above.

Options

Internal terminations. All positions may be independently terminated in 50 ohms, with a 1.5 SWR maximum and 5 watts CW dissipation to 26.5 Ghz, .

Indicators. As a result of recent improvements in indicator circuits, the same lifespan is now possible for indicators as for the RF switch. Typically after a million cycles, the indicator DC resistance is less than 0.5 ohm.

Driver logic. Most switch applications now involve computer control. Electromechanical switches can interface to IEEE 488, HP-IB, BCD/CMOS and TTL logic. In effect, almost any type of electronic interface is possible, either internal or external. The driver circuits can also control other circuits besides the switch.

Configurations. Figures 8-11 show the details of SP2T failsafe and latching switches, and SP6T failsafe and normally open switches. These are representative of conventional configurations. Options in these types of switches include normally open with failsafe to position 1, break before make, and either electronic or mechanical make before break (capable of hot switching).

Figure 12 is a schematic of the common transfer switch, which permits switching between the combinations 1-3, 2-4 and 1-2, 3-4. A more general type is the "S-switch" shown in Figure 13. This adds the combination 1-4, 2-3 to those of the transfer switch.

Another type of configuration is called a matrix switch (not to be confused with a switch matrix), as shown in Figure 14. The center position is a dummy one that has no external connection. By appropriate actuation, any two external ports can be connected to each other through the center, with all other ports open or terminated internally. Variations are possible such as adding reeds between adjacent ports, which allows the simultaneous connection of certain port pairs.

Applications

Because of the increasing reliability and performance of electromechanical switches, they are now being used routinely in high-reliability space, airborne, missile and ground systems. They continue to be widely used in test equipment, instrumention and communication systems.

FOOTNOTES

[1]Frederick H. Raab, Ph.D., "Fundamental Limitations in Class-E and Class-F Power Amplifiers, " Green Mountain Radio Research Co., Copyright 1982.

[2]Complete Fourier Analysis by Frederick H. Raab, Ph. D., "Analysis of Second-Harmonic-Peaking Power Amplifier", Green Mountain Radio Research Co., Copyright, 1982.

[3]David M. Snider, "A Theoretical Analysis and Experimental Confirmation of the Optimally Loaded and Overdriven RF Power Amplifier", IEEE Transactions on Electron Devices, Vol, ED-14, No. 12, December 1967.

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1. J.H. Johnson, High Power Solid State Circuit Design, Unpublished Paper, 1985.

2. H.L. Krauss, C.W. Bostian, and F.H. Raab, Solid State Radio Engineering, New York, John Wiley and Sons, 1980.

3. F.H. Raab, Analysis of Second-Harmonic-Peaking Power Amplifier, Green Mountain Radio Research Co., Copyright, 1982. (RN82-26).

4. F.H. Raab, Fundamental Limitations In Class-E and Class F Power Amplifiers, Green Mountain Radio Research Co., Copyright, 1982 (RN82-18)

5. D.M. Snider, A Theoretical Analysis and Experimental Confirmation of the Optimally Loaded and Overdriven RF Power Amplifier, IEEE Transactions on Electron Devices, Vol, ED-14, No. 12, December 1967.

control than is required for other applications. Depending on system requirements, some materials and parts may be prohibited due to outgassing or radiation sensitivity. Taking these into account, electromechanical switches are well-suited for space applications.

Performance

RF characteristics. Single-pole switches with two through six positions and SMA connectors are capable of the following performance through 26.5 Ghz:

SWR	1.5 maximum
Insertion loss	0.5 db maximum
Isolation	60 db to 18 Ghz
	50 db to 26.5 Ghz

Swept-frequency performance data are shown in Figures 5-7.

Until recently, the industry standard performance was only up to 18 Ghz. This was extended to 26.5 Ghz through careful refinement of the design. The high frequency SWR performance is determined by the electrical characteristics of the connector and the RF cavity (see Figure 8). The SMA connectors used are very rigid and not susceptable to damage from many matings, and they perform better than APC 3.5 mm or K connectors through 26.5 Ghz. Sources of discontinuities which affect the SWR are the transitions from the coax probes to the reed, and the teflon guide pins in the sides of the RF cavity. By experimentally matching out these discontinuities, and by maintaining close mechanical tolerances in fabrication, good SWR performance is possible.

The absolute upper frequency limit is determined by the isolation, which results from the waveguide-below-cutoff characteristic of the RF cavity. As more switch poles and positions are added, the high frequency performance suffers due to the size of the RF cavities. The maximum operating frequency for some representative production switches are

2P2T	24 Ghz
SP8T	19.5 Ghz
SP10T	18 Ghz
SP12T	12 Ghz

Using new designs, switches in the pre-production stage include SP2T, 2P2T, SP4T and SP6T configurations which operate up to 40 Ghz.

Switching. The industry standard switching time has been 20 ms. This has been reduced to less than 7 ms for normally open and 2.5 ms for latching modes. A switching time of less than 1 ms can be expected in the near future.

Power handling. The power handling capability of electromechanical switches is limited usually by that of the RF connector.

MODULATION TECHNIQUES FOR BIOTELEMETRY

by
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Biotelemetry can be defined as a means of wireless transmission of physiological data. Transmission can be via radio, infrared or ultrasound. The frequencies of interest range from DC for temperature telemetry to several thousand Hertz for muscle voltage monitoring.

In aerospace biotelemetry, the telemeter is carried in the aircraft or spacecraft and need not be extremely lightweight. This is not the case, however, when ambulatory people or animals must be monitored. Ambulatory biotelemetry has necessitated the development of a number of interesting battery saving techniques.

Probably the first ambulatory biotelemeter was developed by Norman Holter. It was about the size of a five gallon water can and had to be carried on a pack board. This was followed in 1952 by a compact telemeter using Raytheon subminiature tubes (1).

The advent of the transistor led to renewed interest in ambulatory biotelemetry in the late fifties and early sixties (2-6). These early telemeters usually exployed self excited oscillators operating in the 100 MHz FM broadcast band (Fig 1). This circuit utilized the patient as a transmitting antenna.

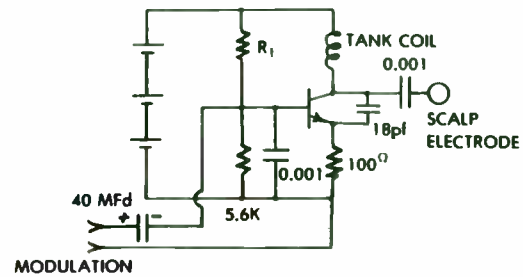

Fig. 1. A 100 MHz self excited oscillator. The transistor is a 2N835. Modulation sensitivity is adjusted by selecting the biasing resistor (R1). The batteries are miniature 1.35 volt mercury cells.

Although transistor manufacturers don't like to mention the fact, the junctions in bipolar transistors are actually voltage controlled tuning diodes. Telemeter designers soon learned to utilize this property as a method of frequency modulation. A base to emitter signal of only about a millivolt was found to produce adequate deviation at 100 MHz. This meant that the amplifier for telemetering a 50 microvolt EEG (brain voltage) signal need have a gain of only 20.

A major problem with these direct FM transmitters was motion artifact due to detuning of the transmitter when the person being telemetered moved his hand near the tank coil. The problem was solved by using an FM-FM system with a frequency modulated audio subcarrier. This technique is still used in most EKG (heart rate) telemeters.

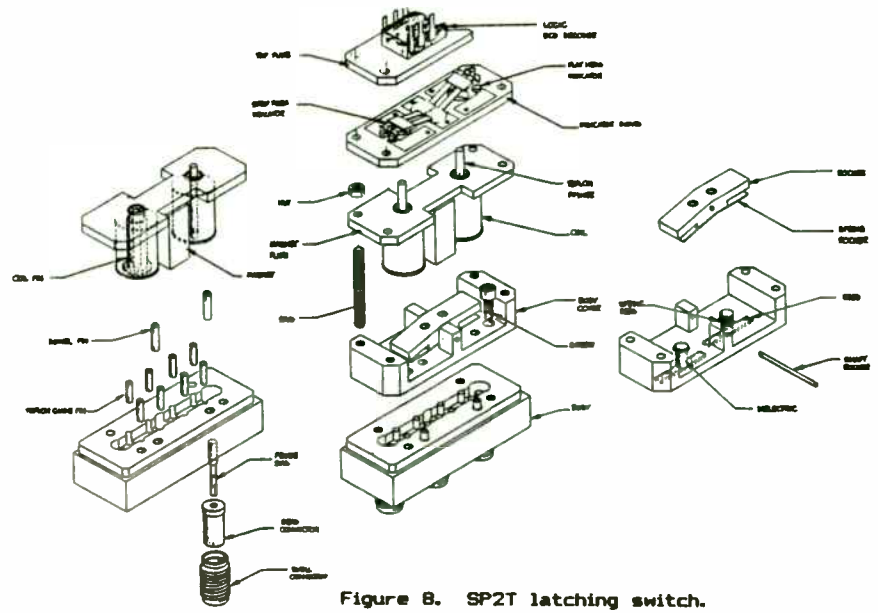

Figure 8. SP2T latching switch.

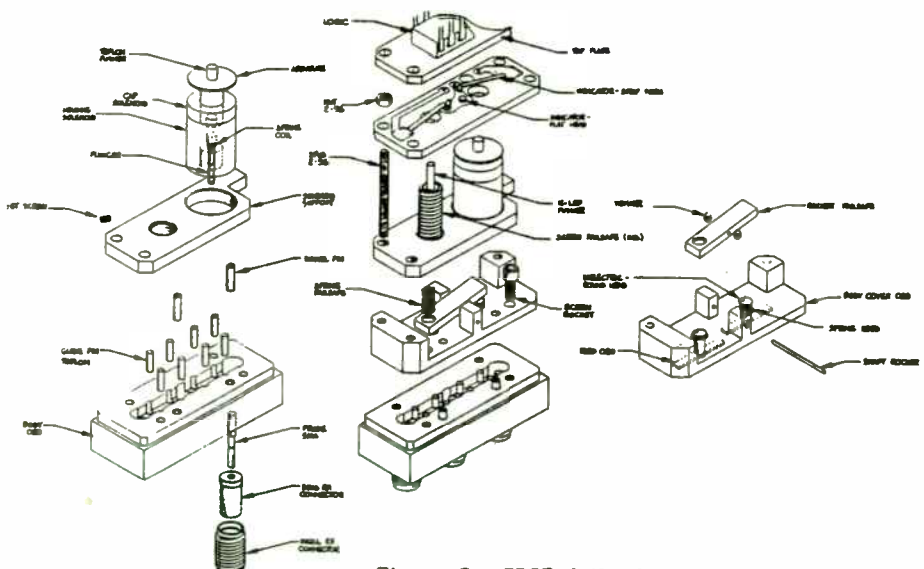

Figure 9. SP2T failsafe switch

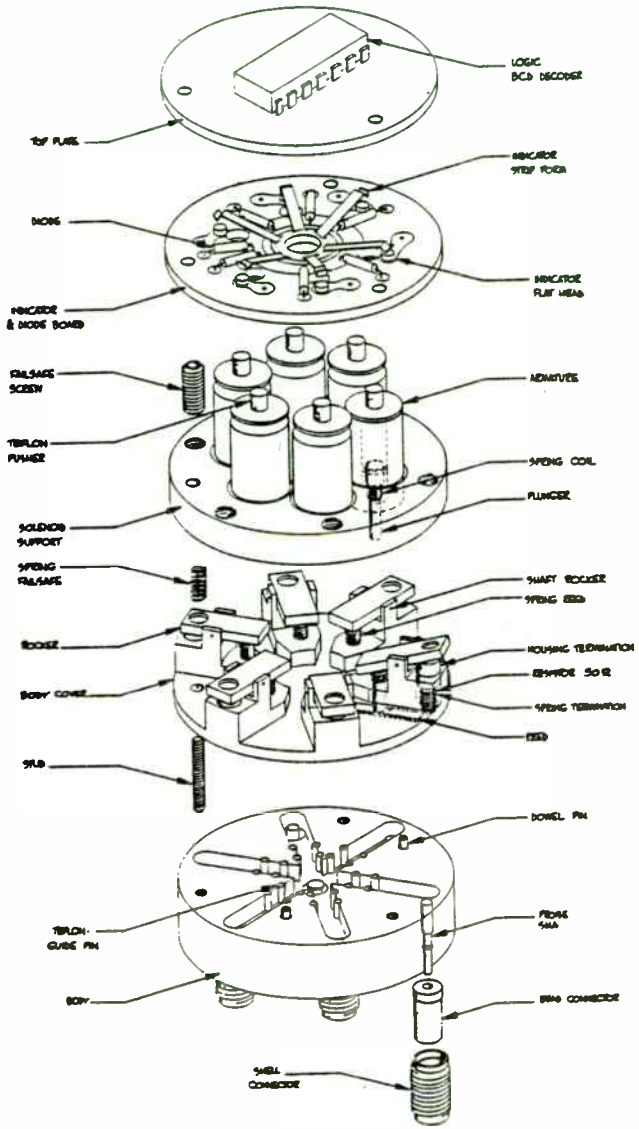

Figure 10. SP6T failsafe switch with terminations.

Hand capacitance detuning is a problem only when low frequency signals such as heart voltage or brain voltages are to be telemetered. In the case of higher frequency signals such as muscle voltage, the movement artifact can be removed by high pass filtering. We have used this technique in a simple multiplex telemeter for muscle voltage and muscle tension (7). Direct FM was used for the muscle voltage and a high frequency subcarrier was used to transmit data from the muscle tension strain gage.

Much of the early interest in biotelemetry was for EEG (brain voltage) studies. A typical application was the location of a seizure focus by implanting multiple electrodes within the patient's brain. A continuous multichannel recording was made day and night until the patient had a seizure. The focus was then located by observing which electrodes detected the strongest signal. The epilepsy could then be treated by destroying a small portion of the brain at the seizure focus. This was usually done by heating the brain with a radio frequency probe. Cases of this type are now usually treated with drugs rather than surgery.

In the beginning, multiple channel recording was done with a separate transmitter for each channel. This was soon found to be impractical. The IRIG format of multiple FM subcarriers was then used to some extent (Fig. 2). However, it had a fairly heavy battery drain because a separate subcarrier oscillator was required for each channel. Continuous operation of the transmitter and all subcarrier oscillators was required.

It soon became evident that the best way to conserve battery power was to pulse the carrier on and off. As early as 1961 Kamp and Storm Van Leeuwen (8) used a combination of pulse width modulation and pulse repetition rate modulation in a two channel system. Although a third channel could have been added

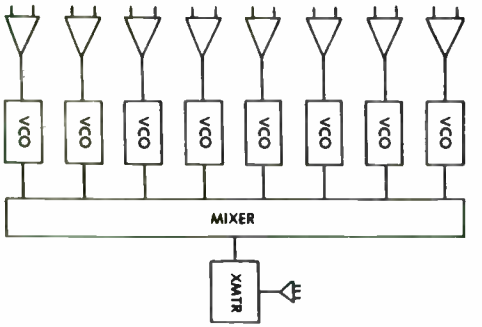

Fig. 2. The IRIG format of multiple subcarriers was used in some early telemeters. Its major disadvantage was excessive battery drain.

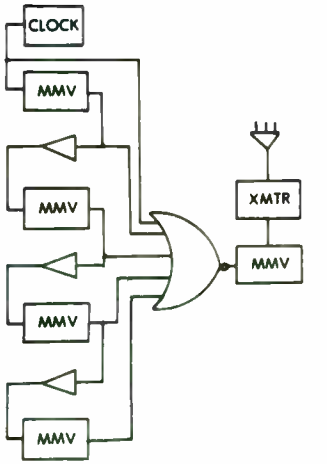

Fig. 3. Pulse position modulation can be generated by a train of pulse width modulated one-shots. This circuit uses SN518B one-shots. They are modulated by SN524A amplifiers.

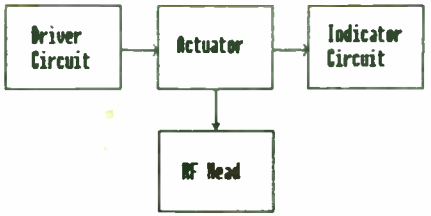

Figure 1. Functional block diagram.

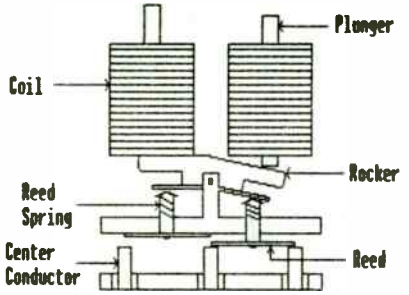

Figure 2. Latching switch.

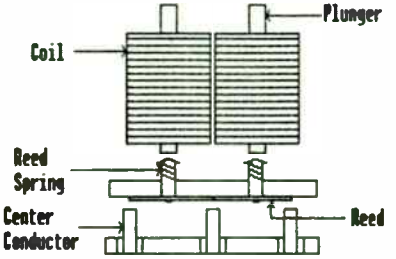

Figure 3. Normally open switch.

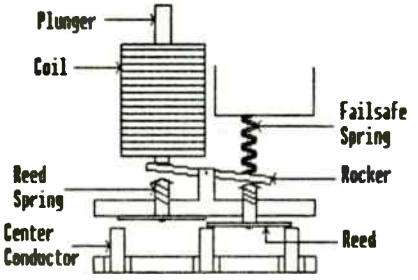

Figure 4. Failsafe switch.

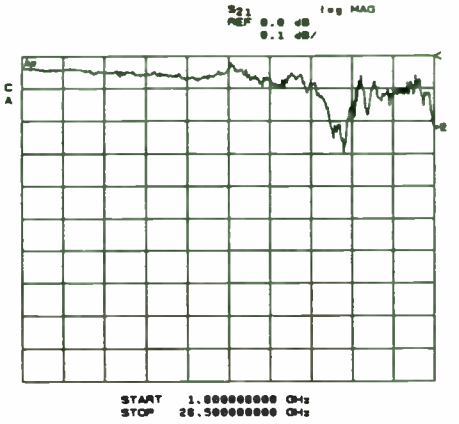

Figure 5. Insertion loss plot.

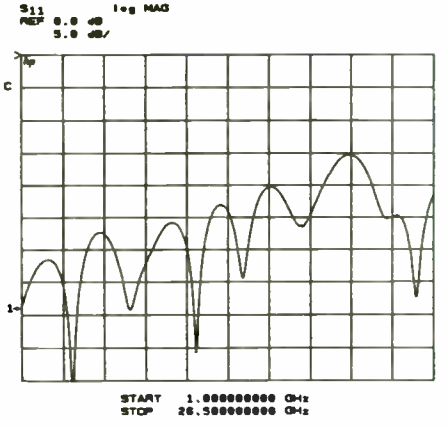

Figure 6. Return loss plot.

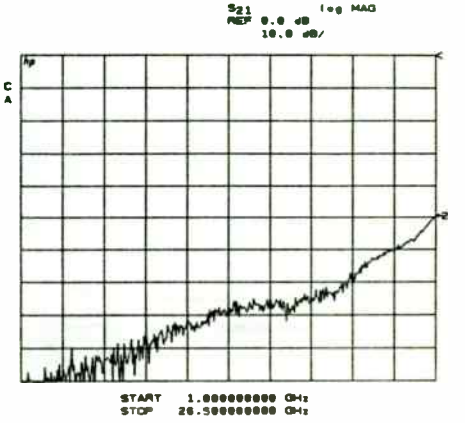

Figure 7. Isolation plot.

by employing pulse amplitude modulation they recognized that this would have been undesirable because of amplitude variations due to signal fading.

A typical hard wired electroencephalograph machine has eight or more channels. Researchers have always wanted to telemeter that number of signals with low battery drain. In order to do this, various pulse coding schemes have been tried. The simplest and most commonly used is pulse position modulation. In this system, the spacing between any adjacent pair of pulses represents the height of an amplitude sample for a particular channel. The data samples for the various channels are transmitted sequentially. At the end of the pulse train there is either a synchronizing pulse or a synchronizing space. A new pulse train representing the next set of amplitude samples is then transmitted.

One of the earliest pulse position modulation telemeters used a chain of pulse width modulated one shots separated by buffers (9) (Fig. 3). The buffers introduced a short delay between adjacent one-shot pulses so that a pulse train was generated when the one-shot outputs were combined in a NOR gate. This pulse train triggered a one microsecond one-shot which in turn keyed the transmitter. Each pulse train was initiated by a clock pulse. There was a synchronizing space at the end of each pulse train.

The received pulses were fed serially into a shift register with parallel outputs for the four data channels. At the start of each received pulse train a reset one-shot was triggered. Its time constant was chosen so that it would time out during the sychronizing space at which time it reset the shift register. Other investigators (10) have used a synchronizing pulse rather than a synchronizing space. This, however, required special circuitry to distinguish between the synchronizing pulse and the data pulses.

We subsequently built a six channel telemeter using the same basic multiplexing one-shot chain (11). This technique worked well but did not make the best use of available battery power.

In order to prolong battery life, we decided to eliminate the one-shots and substitute a ramp generator and a voltage comparator. These circuits were common to all of the nine data channels (12). The data channels were sequentially connected to the comparator by CD4016 CMOS switches (S1-S9) (Fig. 4).

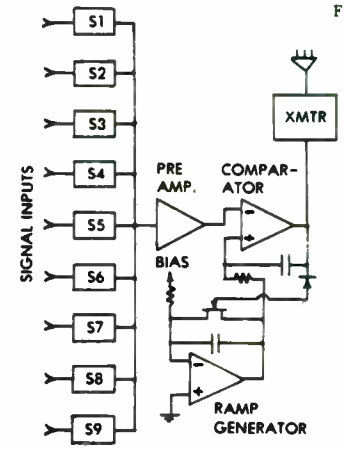

Fig. 4. A simplified block diagram of a nine channel pulse position modulation telemeter. The signal input switches are CD4016's. A MMT3823 J FET is used to dump the capacitor in the ramp generator after each data sample. Pulse spacing is determined by the reference level set on the comparator by the input signal sample.

Actually eighteen switches were used because each input was push

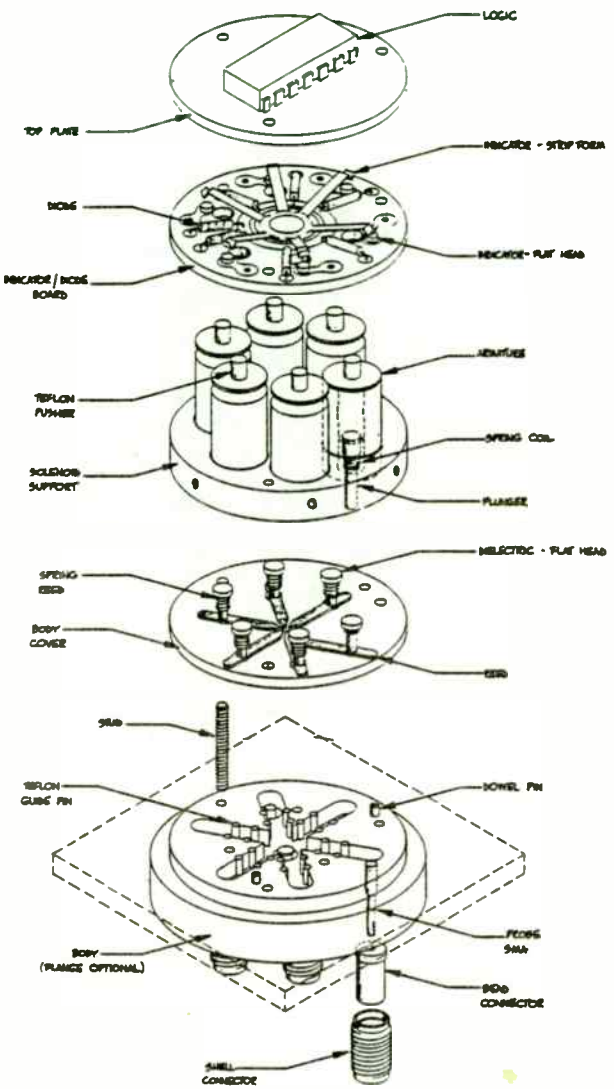

Figure 11. SP6T normally open switch.

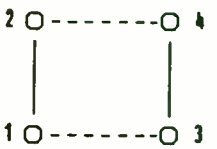

Figure 12. Transfer switch schematic.

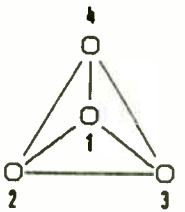

Figure 13. "S-switch" schematic.

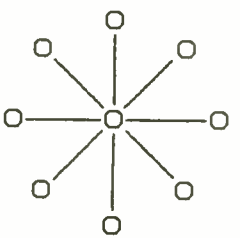

Figure 14. Matrix switch schematic.

pull. Sequencing of the switches was done by a CD4017 shift register. The selected signal channel was amplified by the common pre-amplifier and used to establish a reference level on the voltage comparator. If the signal level was high, the reference level was high and it took the ramp generator longer to run up to this reference level. When the reference level was reached, the comparator dumped the ramp generator integrating capacitor via a J FET. It also pulsed the transmitter on and shifted the shift register to enable the next input channel. After all nine channels had been sampled there was a synchronizing space. A clock then reset the shift register.

This circuit eliminated the need for separate pre-amplifiers and separate pulse width modulators for each channel. The elimination of separate preamplifiers was due to the low noise characteristics of CMOS switches. This property of CMOS is not well known. Let us suppose that we are switching with a single MOS FET other than CMOS. The gate must be pulsed high to close the switch. Since the line we are switching is high impedance (200K ohms) a portion of the control pulse will be coupled via the gate to channel capacitance into the signal line. Now, let us assume that we are using a CMOS switch. This consists of a P channel MOS FET in parallel with an N channel MOS FET. Since these two MOS FETS require opposite polarity control pulses the portions of the control pulses that are capacitively coupled into the signal line effectively cancel. This circuit worked well for recording from depth electrodes implanted within the brain since the brain signal level was a couple of hundred microvolts peak to peak. For scalp electrode recording an individual preamplifier for each channel was required.

The NASA people have built an eight channel 0.1 percent accuracy pulse code modulation telemeter (13). The data signals were first converted into pulse width modulation by a ramp generator. These pulses gated a 10 MHz oscillator. The 10 MHz pulses within these gated pulse trains were counted by a 10 stage counter. Output from the counter went to a parallel in, serial out shift register which in turn keyed the transmitter.

All of the foregoing telemetery systems were for AC signals. Drift is a major problem when DC signals such as temperature are telemetered. Fryer (14) has used a free running multivibrator as a subcarrier oscillator. One of the two time constant determining resistances was the temperature sensing thermistor. The other was a reference resistor which established the zero reference level. The telemetered temperature was proportional to the ratio of these two resistances.

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Microprocessor Control Considerations for Modern RF Signal Generators

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Since the introduction of the microprocessor in the early 70's, there have been many improvements in technology. These improvements have allowed the microprocessor and its associated control elements to be more frequently incorporated into electronic designs. This paper examines some of these improvements and discusses them in the context of a new RF signal generator design.

The most significant improvements affected the microprocessor itself. Improvements in manufacturing lead to more efficient chip layouts and faster speeds which allowed more high-level functions to be included in the basic device. Figure 1 illustrates this by showing the types of functions which are now available in a single package. The resulting reduced chip count allows for a more cost effective design. In addition, the single-chip microprocessor now creates the possibility of including high-level control in the lowest levels of a design. For an RF design which includes a VCO, the high-level functions can include frequency control, linearity correction, leveling, calibration, and dynamic loop compensation. There is a device specifically made for TV tuner control which includes a simple phase detector and frequency prescaler.

Additional ROM/EPROM allows for more code to be written which means more control features. On-board RAM usually satisfies the software engineers programming requirements. In addition, a portion of the RAM can usually be battery backed up so that information such as calibration data can be retained during power-down conditions. The serial port is useful for providing a simple interface to other microprocessors in the design. A programmable timer is important in providing those valuable delays associated with real-world events such as settling times associated with narrow loop bandwidths. In addition to delays, the timer function usually includes an event count feature. This may be useful for control event timing during a digital sweep. The I/O ports provide a simple parallel interface to control elements such as D/A converters, counters, and storage registers. They may also be used to implement a simple serial data-bus.

In more recent devices, EEPROM has been included allowing for non-volatile data storage without the battery mentioned above. There is, however, still a limitation on the number of write cycles for these storage elements. EEPROM should still be used only for storing data which is infrequently modified, e.g. calibration data.

The A/D converter opens a whole range of possibilities such as a comprehensive self-test and diagnostics as well as calibration of detected RF level and modulation circuitry.

CMOS technology appears to be dominating over older technologies such as bipolar (TTL) and NMOS. The small geometries are allowing for faster speeds while retaining the overall low power advantage over the older technologies. In addition, a total CMOS design allows for fully static operation. This means that the timing element or oscillator of a digital element can be stopped

without affecting the state of the digital operation. HCMOS is the nomenclature for high-speed low-power digital devices.

Improvements in microprocessor design are not limited to the hardware. Although the Von Newmann architecture is still retained, instructions have been added to the traditional microprocessor control set.

Software Engineers routinely set and clear flag and status indicators just as Hardware Engineers utilize single bit control mechanisms like those required by analog transmission gates and relay controls. The System or Product Engineer will want to group the non-byte control lines into logically grouped, however, highly mixed byte elements to keep the hardware count low. This means a lot of software activity on a bit basis. Bit orientated instructions which SET, CLEAR and TEST/BRANCH are now available which allow more efficient programming and faster throughput. These instructions were traditionally accomplished by AND'ing and OR'ing a mask byte to the desired control register. The mask byte would affect the desired bits of the control register.

As mentioned previously, HCMOS technology allows for fully static operation. Two instructions (STOP and WAIT) have been added to take advantage of this. WAIT causes the microprocessor to halt operation while the on-board oscillator remains on. STOP halts the microprocessor operation but shuts off the on-board oscillator. The microprocessor returns to full operation through its INTERRUPT facility. The microprocessor resumes operation when a restart or wake-up signal is applied to the interrupt pin of the microprocessor. These instructions provide two important operational advantages: 1) extremely low power consumption and 2) no interference to surrounding circuitry (conducted) or the external (radiated) environment while in the STOP or WAIT modes.

When designing an RF signal generator there are two major control considerations which affect the overall instrument performance. The first is the user interface (front-panel keyboard, display and GPIB) and the second is the overall control mechanism which manipulates the RF section (frequency, level and modulation). Attention to both of these areas is important to good overall user friendliness.

In general, it is considered to be good practice to keep the processing speed of a user orientated device below 100 msec. This will minimize an effect called "rubber-banding". This effect is noticed when the user modifies an instrument setting and does not notice an effect on the instrument operation until after the next setting has been obtained. If a spin knob or cursor keys are used on the front panel, the operator will overshoot the desired setting and will have to go through several iterations of adjustment to get to the desired operating point.

The Wavetek Model 2500 RF Signal Generator utilizes the Motorola MC146805E2 microprocessor and a serial data-bus control structure. The user interface is entirely interrupt driven except for the displays which use dedicated drivers for the custom LCD's.

Either a parallel or serial data-bus structure can be used when designing the control mechanism. Since the data-bus will be the mechanism for controlling both the front-panel operation and the RF sections, special

WIDE-BAND HIGH-DYNAMIC-RANGE FRONT-END CIRCUITRY FOR AM RADIO

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ABSTRACT

This paper presents the bipolar integrated input-amplifier and frequency-conversion circuitry of an AM upconversion front end for car-radio receivers. Thanks to the upconversion concept and the excellent performance of the wide-band high-dynamic range front end, tuned preselection filters can be omitted, thereby eliminating the need for adjustments and reducing production costs considerably. Tuning is easily accomplished by varying only the oscillator frequency.

The dynamic range of the front end exceeds 120 dB. Field strengths up to about 20 and 200 mV/m can be handled without noticeable second- and third-order intermodulation, respectively.

INTRODUCTION

Conventional AM receivers for long-wave and medium-wave reception use intermediate frequencies somewhere between 450 and 490 kHz. Such receivers need a preselection filter to reject the image and other spurious channels. This filter has to be tuned along with the local oscillator. Band switches and several adjustments are required to ensure adequate tracking.

Well-aligned receivers with mechanically tuned variable capacitors or coils can provide excellent performance, but are expensive. The use of varactors for tuning as an alternative offers the possibility of digital synthesizer tuning. However, their nonlinearity reduces the useful dynamic range of the preselection filter. Besides, band switches and adjustments are still needed.

This paper presents the front-end circuitry of an upconversion receiver for car-radio with a block diagram as shown in Figure 1. The complete receiver has been integrated in a conventional bipolar process (f_{Tnpn} = 400 MHz). Channel selectivity has been realized by a low-cost 10.7 MHz quartz filter. The upconversion concept evades the need for tuned preselection. A low-pass filter at the mixer input effectively rejects image and local-oscillator-related spurious responses. However, a proper noise match to the whip antenna has to be realized in a wide-band low-distortion amplifier, since a fixed low-pass filter in front of this amplifier would seriously impair noise performance [1]. The gain of this amplifier has to be kept low because very large input signals have to be handled linearly. As a consequence, the noise and intermodulation performance of the frequency-conversion circuits (mixer and local oscillator) are also very important.

The first section of this paper discusses a capacitive-feedback wide-band input amplifier with an optimally biased bipolar input stage. The dynamic range of this amplifier has been extended by means of an automatic gain switch, which is activated when very large field strengths are present somewhere in the spectrum.

The second section deals with the frequency conversion circuits. A double-balanced switching mixer, a negative-resistance "one-pin" LC oscillator and a buffer stage maximize the dynamic range. In order to accurately fix the oscillator output amplitude even with large parameter variations, while maintaining an acceptable noise performance, a novel type of AGC has been employed.

INPUT AMPLIFIER AND AGC SWITCH

amplifier configuration

The low-frequency equivalent circuit of a car-radio whip antenna, including the cable to the receiver input is shown in Figure 2. The open antenna voltage is given by

$$V_a = h_{eff} E_a,$$

where E_a is the electric field strength and h_{eff} is the effective height. For a whip antenna, h_{eff} equals half its physical length l_a

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consideration was given to the selection to minimize conducted noise to the RF sections, reduce the device count for implementing the data-bus, and maintain good overall throughput to ensure good user response. The serial data-bus easily satisfies the first two design criteria. There is an obvious 8:1 speed disadvantage over a byte orientated parallel data-bus. The real question is "How bad is it?" Measurements made on the Model 2500 show that the entire RF control structure of 112 bits or 14 bytes can be transmitted in less than 10 msec. Figure 2 shows a schematic of the data-bus and Figure 3 shows a flow-chart of the algorithm used to transmit the data.

Within the control circuitry of the RF section the 74HC595 shift register was the primary storage element. These devices were cascaded as necessary to complete the control strings. There are six (6) control strings and a strobe signal. Table I shows the partitioning of the control functions.

TABLE I. CONTROL FUNCTION STRINGS

- VCO Control
- Frequency Divider
- Modulation
- DDS Programming
- Output Level and FM Deviation Correction
- Status Data
- Register Strobe

TABLE II. STATUS INDICATORS

- 400 Hz Square Wave
- Frequency Calibration
- FM Over-Deviation
- Lo-Loop Unlock
- Main-Loop Unlock
- Reverse Power Protection Trip
- Unlevel

Several error conditions can be detected and indicated to the operator on the front-panel. Table II lists these as well as two additional status lines.

The 400 Hz clock line is read during the power-up sequence to determine if the frequency reference is operational. Since the 400 Hz output is the last output in the reference chain, this is just like taking its pulse. An error will also occur if the rear-panel switch is set to EXT REF and the external reference is not connected.

The other status line is used to implement a frequency self-calibration routine for each of the four VCO's. In this routine, each of the oscillators is calibrated and the results stored in the battery backed-up RAM. The entire frequency vs. voltage characteristic is measured for each oscillator. No external equipment is required.

Another contributor to generator performance is computational throughput. Microprocessors are not very good number crunchers. While this may seem contrary to the primary usage of a microprocessor, the existence of the floating-point coprocessor is evidence that the need exists for better arithmetic capability. The computation of a transcendental function should always be avoided. Floating-point multiply and divide routines should be used only when absolutely necessary while the use of add and subtract should be minimized. BCD representations are generally very acceptable even though they are inefficient for RAM storage. Binary representations are native to the microprocessor but are difficult to interpret as the result is usually always binary related and not in nice multiples of 10.

$$h_{eff} = \tfrac{1}{2} l_a .$$

In conventional receivers, the source capacitance $C_a + C_c$ forms an inherent part of the preselection filter. Its reactive part is thus tuned out, thereby significantly simplifying the realization of good noise and intermodulation performance. It can be shown [1] that a filter that covers the whole band to be received and that includes the source impedance would unacceptably degrade noise performance. Therefore a wide-band amplifier has to be used.

A frequency-independent response to the electric field, and consequently to the open antenna voltage, is obtained in a capacitive-feedback amplifier according to Figure 3. The gain of this amplifier is approximately given by

$$\frac{V_o}{V_a} = -\frac{C_a}{C_f} .$$

Note that the cable capacitance ideally does not influence the gain. The impedance level of the low-pass filter behind the preamplifier is chosen as high as 470 Ω to keep the output current low. Insertion loss has been kept small by using an asymmetrical filter terminated in the high input impedance of the voltage-to-current converter of the mixer.

AMPLIFIER IMPLEMENTATION

Figure 4 shows the circuit diagram of the wide-band input amplifier. The signal path is formed by the NPN transistor Q_A, Q_B and Q_C. The noise of the circuit is determined predominantly by the first two stages. Assuming that the bias current of the second stage is much larger than that of the first stage, the spectra of the equivalent input noise sources of the amplifier can be approximated as

$$S(v_n) = 4kT\{r_{bA} + r_{bB} + r_{eA}/2\}, \quad S(i_n) = 2qI_B .$$

Referring to Figure 5, the spectrum of v_{eq} in series with the antenna voltage v_a can be written as

$$S(v_{eq}) = \left\{\frac{(C_a + C_c + C_f)^2}{C_a}\right\} S(v_n) + \frac{1}{\omega^2 C_a^2} S(i_n).$$

The equivalent noise voltage (v_{eq}) in a 2.5 kHz bandwidth and for $r_{bA} + r_{bB} = 100$ Ω is depicted in Figure 6 for various values of the input-stage bias current. A tradeoff is observed between high- and low-frequency noise performance. An acceptable compromise is obtained at a bias current of 50 μA. The equivalent noise voltage than equals 0.8 μV at 1 MHz and 1.5 μV at 150 kHz measured in a 2.5 kHz bandwidth

In order to achieve a high loop gain, the second-stage load is made very high by means of active bootstrapping (Q_1 - Q_4). The loop gain has a dominant pole determined by the impedance level at node B. The impedance is formed by a capacitance with a value of about 10 pF. With a feedback capacitance $C_f = 22$ pF, a gain of about 0.6 and a bandwidth of 60 MHz is obtained. In order to minimize intermodulation due to high-frequency input signals a smaller bandwidth is highly desirable; however, this should not be realized at the expense of a smaller slew rate. The only appropriate technique to reduce the bandwidth without deteriorating, as a result of slew-rate limitations, the intermodulation performance is the use of phantom zeros [2]. A network consisting of two coils and a resistor in series with the amplifier input provides such zeros. It has been designed such that the amplifier noise performance is scarcely degraded and the frequency response is 3 dB down at 7 MHz.

The output stage is biased at a collector current of 6 mA and can deliver a peak-to-peak voltage of 4 V to the low-pass filter. In low-end applications a fixed feedback capacitor of 22 pF can be used. In that case an antenna voltage of about 2 V, corresponding to a field strength of 4 V/m can be handled. The total equivalent noise (including mixer contributions) can then have a value of 1.6 μV (B = 2.5 kHz). The dynamic range exceeds 120 dB. Second- and third-order intermodulation products become noticeable (i.e. are equal to the noise floor) at input-signal levels of 15 and 100 mV, respectively. These measurement results bring the second- and third-order intermodulation-free dynamic range (IMFDR) to 80 and 97 dB, respectively.

A good compromise is to perform any analog scaling required to give a "good" result. For instance the level control DAC is a 10 bit binary device with the LSB scaled for 1 mV RMS of RF output. This gives a 1 mV to 1.024 V control range. Logarithmic or dBm representations are obtained by first converting the dBm value to volts through the use of a precalculated look-up table. The binary result is then applied to the 10 bit DAC.

The frequency control is primarily BCD. This keeps the reference frequency an even value and simplifies the required arithmetic.

An interesting concern is the organization of the data strings. It is recommended that the data flow be from left to right or LSB shifted out first. This means that the most significant byte of a BCD control string will be the last to the transmitted in the serial string. Logical control string organization reduces the amount of manipulations required by the software to format the string before it is transmitted.

One method of improving the user response time would be to run the microprocessor clock at a faster rate. The MC146805E2 runs at a 4 MHz clock rate which results in a 1 MHz cycle time due to internal divide by 4 circuitry. HCMOS devices are running at toggle rates in excess of 30 MHz. Successful experiments were performed at a clock rate of 8 MHz or 2 MHz cycle times, however, the standard device is not guaranteed at those speeds. Faster parts could be selected by the manufacturer. Note that a change in processor speed affects the value of the delays produced by the microprocessor's timer element.

The Model 2500 utilizes a single microprocessor to handle both the front-panel operations as well as the RF control. The previously described clock directed serial data-bus performs the communication to each of the sections. An alternate approach would be to have two microprocessors, one for each of the required control functions. Communications between each microprocessor would take place with either a bi-directional serial or parallel data-bus. The Model 2500 does use an additional microprocessor to implement the standard GPIB communications feature. A parallel 8 bit bidirectional data-bus provides the data exchange mechanism. The handshake mechanism has been simplified for a two microprocessor implementation. However, a multiprocessor parallel data-bus structure has been conceptualized called Quick-bus. It provides a data exchange mechanism for up to 14 microprocessor controlled elements. There are some similarities to the VME bus operation, however the simplification makes a multiprocessor parallel data-bus practical for applications such as an RF signal generator or sweeper. The signaling and arbitration logic is realizable in a simple Programmable Array Logic (PAL) device.

The front-panel was designed for maximum flexibility and smooth operation. Two custom LCD displays with switchable EL back-lighting were used. The modulation and level displays were designed so they are interchangeable. The keyboard matrix is implemented with two MSI devices and can be expanded up to 64 elements. The spin-knob is a conductive plastic incremental encoder which sells in modest quantities for eight dollars. This is in contrast to the optical encoders which sell for 30 to 50 dollars. The keyboard and spin knob are serviced on demand through the interrupt service routine. The interrupt facility provides a minimum response time for the user.

Automatic gain switch

In order to further increase the dynamic range of the input amplifier, the gain is switched automatically to a lower value as soon as a certain input level is exceeded. Figure 7 shows the basic implementation, where the position of the switch has been chosen such that it has no detrimental effect on noise and intermodulation performance. An external JFET is used as a switch. It is driven by a logic signal obtained by appropriate detection and comparison with a reference level of the amplifier output signal. The comparator hysteresis is chosen 3 dB more than the required gain variation so as to obtain a safe margin, where the gain remains low before the switch is deactivated, thereby avoiding bouncing.

In order to detect the signal level sufficiently accurately, a full-wave rectifier is employed. Comparison with the reference level is performed by two cascaded comparators, the first of which has the required hysteresis. The second comparator is added to avoid a possible source of instability in the switch operation. With C_{f1} = 10 pF and C_{f2} = 30 pF, field strengths of 2 V/m and 8 V/m, respectively, can be handled linearly. The noise floor in a 1.5 kHz bandwidth lies at 1 and 2 μV at 1 MHz, respectively. Second- and third-order IMFDR are at 77 and 90 dB when the switch is deactivated and at 86 and 97 dB when it is activated.

MIXER, BUFFER AND LOCAL OSCILLATOR

Since the preamplifier has to handle large signals at a restricted supply voltage (V_{Bmin} = 7.5 V), the gain is limited to a rather low value. The same holds for the conversion gain of the mixer. The large dynamic range desired and the low gain values involved make the noise and distortion originating from the frequency conversion action more important than in conventional receivers. When infinite betas and a zero switching time are assumed, the current transfer i_o/i_{in} of a double-balanced mixer (Figure 8) does not contribute to noise and distortion. In the case of finite betas, the distortion is generated by current-induced beta variations and the noise is determined by the base-current shot noise, exclusively. Finite switching times introduce additional mixer distortion, since the signal current is transferred in a nonlinear way from input to output during the switch transitions. Finite switching times also lead to other noise contributions besides the base-current shot noise.

Without a doubt, the best mixer performance is obtained when it is driven by a high-slope local-oscillator signal. Ideally, the "finite-slope" noise contributed by the conversion process is then completely determined by the local-oscillator noise. In the frequency-conversion circuitry described here, this situation has been accomplished to a reasonable extent. The mixer switching time is less than 5 ns.

In order to obtain adequate noise performance in the local oscillator an LC oscillator is preferred over a relaxation oscillator. Pulling effects are avoided by employing a limiting differential-pair stage that drives the mixer. Though this limiting action may increase the white noise floor of the local-oscillator signal, the carrier-to-noise ratio of the output signal is still sufficiently high so as not to degrade the receiver noise performance significantly.

The amplitude of the oscillator sine-wave should be fixed well enough to guarantee that the differential-pair buffer stage acts as a current switch. Some form of automatic level control in the oscillator is required to make the amplitude virtually independent of impedance variations in the resonance circuit.

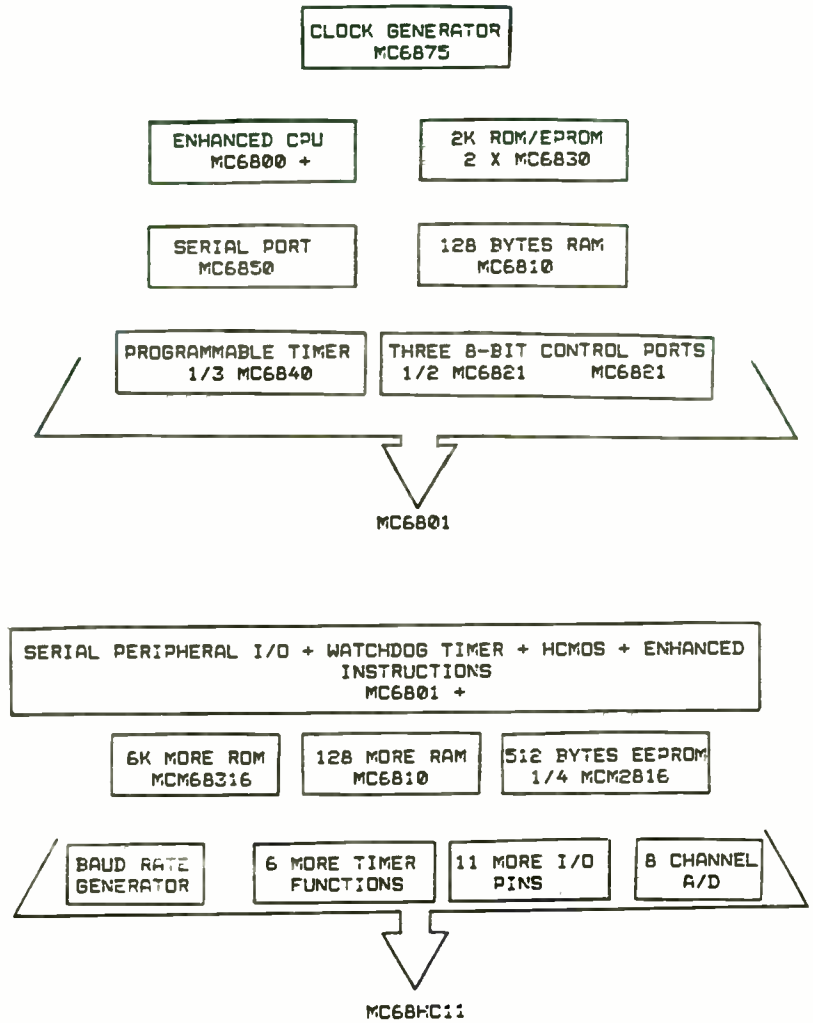
A basic method for the realization of a suitable negative-resistance "one-pin" oscillator is shown in Figure 9. This circuit, however, does not include the proper means for amplitude stabilization. It is useful for appreciating the stabilization technique used in the oscillator to be presented here to distinguish three different modes of operation.

In the first mode, the incremental loop gain $g_m R_p$ is just slightly higher than unity. When the oscillator amplitude in that case is smoothly limited by the third-order nonlinearity of the differential-pair transconductance, the circuit behaves as a Van der Pol oscillator. In this mode of operation, small variations, either in the resonance-circuit impedance or in the bias current,

The Model 2500 has full and state-of-the-art talker and listener implementation for the GPIB interface. The command set is very user friendly. It allows a verbose and essentially self-documenting command format for modern ATE and lab bench test systems. The implementation eliminates the vague and cryptic command sets present in current competitive RF signal generators. The talker function allows the full machine status to be obtained as well as a comprehensive reporting mechanism for functional errors.

The most important consideration in the control of RF designs is good communications between the RF and Software Design Groups. The communications mechanism should be a controlled document which both groups can comprehend. It will start with copies of the RF Designer's engineering notebook and end up being reformatted into a form that the Software Engineer can perform his design. The result should be one that either group can pick up and understand the control mechanism of RF sections.

I would like to acknowledge the efforts and contributions of the entire Model 2500 design team. In particular the RF Design Engineers for their patience with the Software Design efforts, the Software Engineers who worked through some difficult organizational situations, and the Mechanical Design Engineers who were the brunt of all the loose ends.



may easily result in turn-off or in an increase in amplitude and a much stronger limiting action.

In the second mode of operation the stronger limiting action is put to good use, and the differential pair acts as a current switch. As long as the output voltage of the circuit is so small that no saturation occurs, the output amplitude depends linearly on the tail current and on the resistance in the resonance circuit. Though less than in the previous situation, the output amplitude is still rather sensitive to parameter spread, and the appropriate level for the buffer is hard to guarantee.

In the third mode of operation, the tail current and the resistance of the resonance circuit are so large, and the collector-to-base voltage so small that either Q1 or Q2 saturates. During the peaks of the output voltage, the resonance circuit is short-circuited and the noise performance cannot be expected to be much better than in a regenerative oscillator.

The oscillator can be forced to operate either in the first or second mode by using well-known AGC techniques. These techniques, however, require a form of detection together with some low-pass filtering in order to control the magnitude of the tail current. The method presented here is intended to force the oscillator to operate in the second mode by using a novel AGC technique. The operation principle is illustrated in Figure 10. The tail current of the differential pair is modulated with the oscillator signal. In the waveform supplied to the resonance circuit the first-harmonic content is thus reduced, all the more so as the output amplitude increases, as depicted in Figure 11.

The differential pair providing the tail current is biased such that Q4 initially conducts and Q5 does not. After the oscillations are started, the amplitude at the base of Q4 will get a value such that this transistor will be driven out of conduction during the peaks of the oscillator signal. The amplitude will thus be fixed at a value closely corresponding to the DC bias voltage between the bases of the tail-current differential pair.

A complete circuit diagram of the oscillator-buffer combination is shown in Figure 12. The tuning range amply exceeds the required range of 10.85 - 12.32 MHz, so that no adjustments are needed for guaranteed acquisition of the frequency-synthesizer phase-lock loop.

The output sine-wave amplitude is fixed at a value of about 0.5 V, large enough to obtain a proper switching action of the buffer stage. A wide range of tank-circuit impedances can be used. Impedances as low as 1 kΩ still do not stop oscillations. With a resonance circuit with a Q of 50, the carrier-to-noise ratio at 9 kHz from the carrier is about 70 dB in a 5 kHz bandwidth. Since the adjacent-channel rejection in the IF filter is much smaller than 70 dB, the oscillator noise does not impair receiver selectivity.

The signal input of the mixer is driven from a differential-pair voltage-to-current converter using simple emitter degradation. As only low-frequency operation (up to 1600 kHz) is involved, the nonlinearity of this circuit can be solely attributed to the exponential relationship between V_{BE} and I_C. A straightforward calculation of the third-order intermodulation then shows that it hardly contributes to the intermodulation generated in the preamplifier when it is biased at a tail current of 10 mA and with 150 Ω degeneration resistors.

The noise contribution of the mixer as a whole (including the V-I converter) can be largely attributed to the V-I converter. As a consequence of the switching operation, not only is the noise of the input frequency band and the image frequency band converted to the IF frequency, but also the noise in the bands related to the odd oscillator harmonics. The low-pass filter effectively short circuits the equivalent noise current source of the V-I converter at frequencies higher than the cut-off frequency. So, only the base-band contribution is determined by both the equivalent input sources. A calculation of the various contributions leads to an equivalent input spectrum in series with the preamplifier output $S(v_{no}) = 4kT3700$. This source transforms into an equivalent source in series with the antenna voltage:

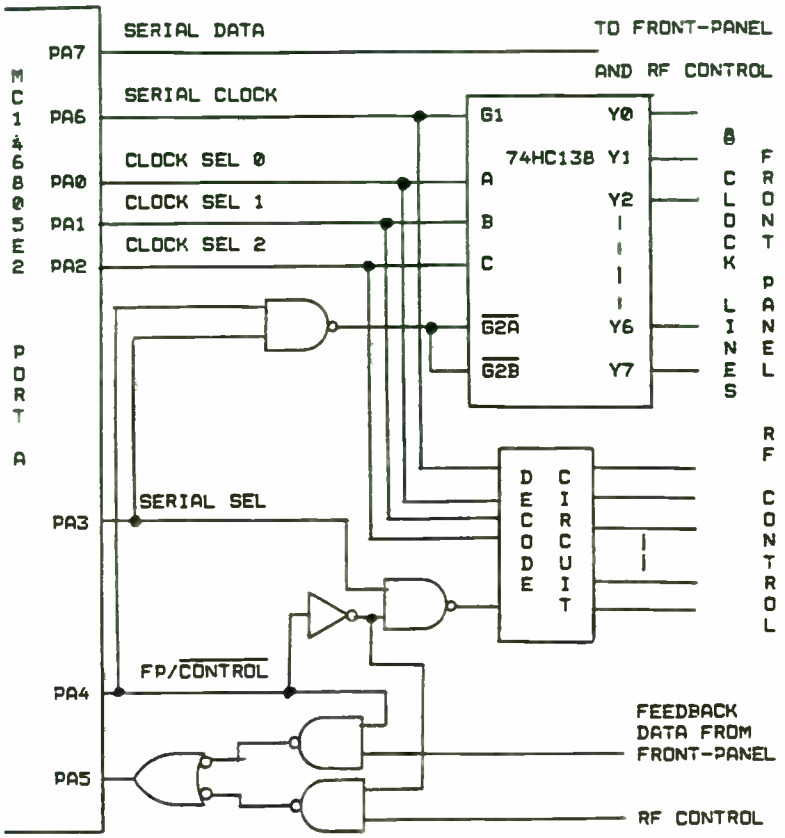


FIGURE 2 : MODEL 2500 SERIAL DATA-BUS STRUCTURE

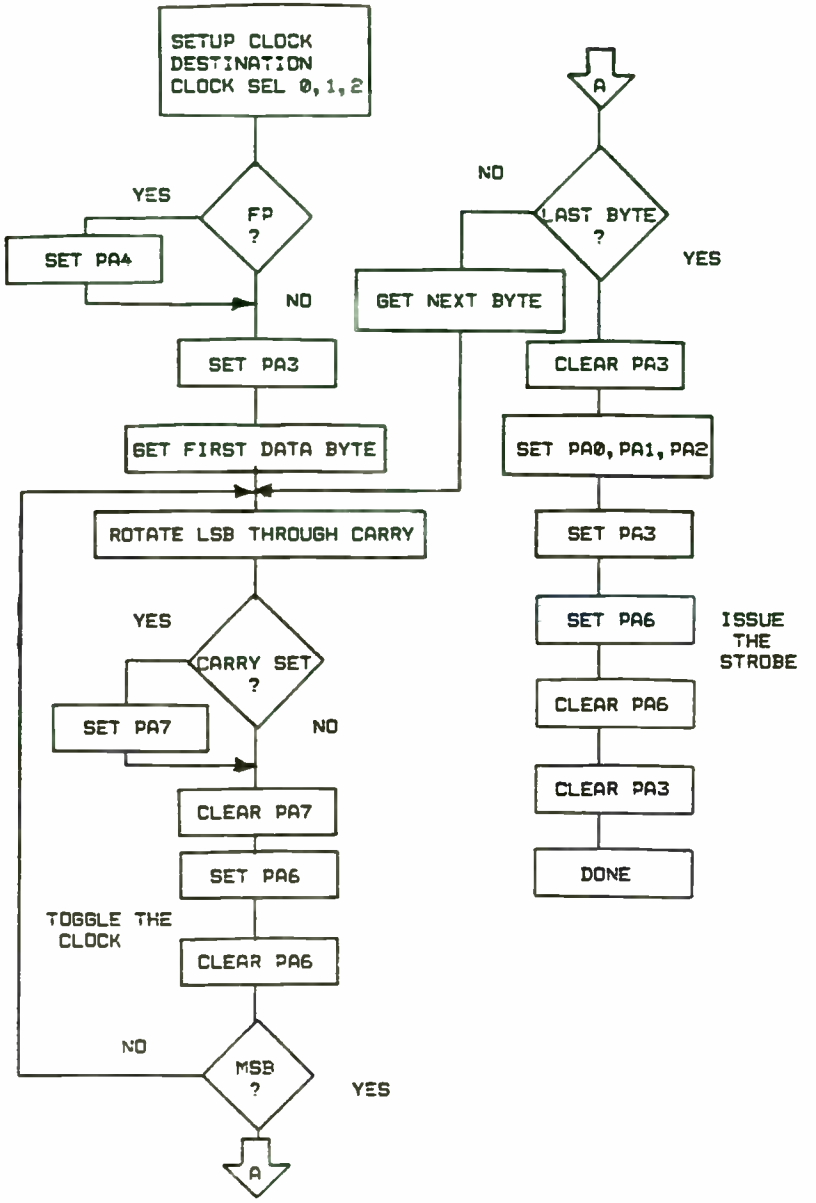


FIGURE 3 : MODEL 2500 SERIAL DATA-BUS CONTROL

$$S(v_{eq},a) = \left(\frac{C_f}{C_a}\right)^2 S(v_{no}).$$

This noise source is significant in the case of low preamplifier gain (activated switch). In the high-gain situation (deactivated switch) the preamplifier noise dominates.

CONCLUSIONS

This paper presented an integrated front end for a long-wave and medium-wave AM car-radio receiver. The circuits are realized in a conventional bipolar process (f_T = 400 MHz). Thanks to the upconversion concept and the high dynamic range of the various circuits, the system needs no adjustments, thereby significantly reducing production costs. The second- and third-order IMFDR amount to 86 and 97 dB, respectively, in high field-strength situations, where an automatic gain switch in the preamplifier is activated. The maximum field strength that can be handled is 8 V/m.

ACKNOWLEDGEMENT

The authors wish to thank the Philips Industry Group Car Radio for its interest and support. The efforts of the IC workshop of the Delft University of Technology are gratefully acknowledged.

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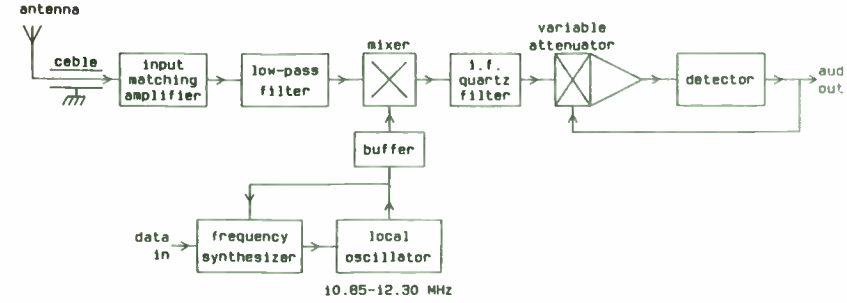

Fig. 1 Block diagram of an upconversion receiver.

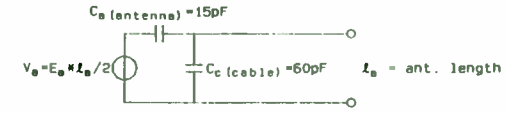

Fig. 2 Circuit representation of whip antenna and cable.

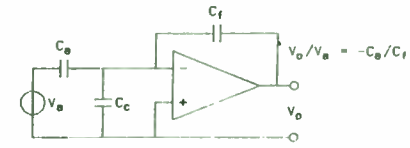

Fig. 3 Input-amplifier configuration with capacitive feedback.

EVERYTHING YOU WANTED TO KNOW ABOUT TUNING DIODES

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INTRODUCTION

Voltage variable capacitors or tuning diodes are best described as diode capacitors employing the junction capacitance of a reverse biased PN junction. There is a wide range of available capacitances and different device types. The capacitance of these devices varies inversely with the applied reverse bias voltage.

Tuning diodes have several advantages over the more common variable capacitor. They are much smaller in size and lend themselves to circuit board mounting. They are available in most of the same capacitance values as air variable capacitors. Tuning diodes offer the designer the unique feature of remote tuning.

SIMPLIFIED THEORY

A tuning diode is a silicon diode with very uniform and stable capacitance versus voltage characteristics when operated in its reverse biased condition. In accordance with semiconductor theory, a depletion region is set up around the PN junction. The depletion layer is devoid of mobile carriers. The width of this depletion region is dependent upon doping parameters and the applied voltage. Figure 1A shows a PN junction with reverse bias applied, while Figure 1B shows the analogy, a parallel plate capacitor. The equation for the capacitance of a parallel plate capacitor given below predicts the capacitance of a tuning diode.

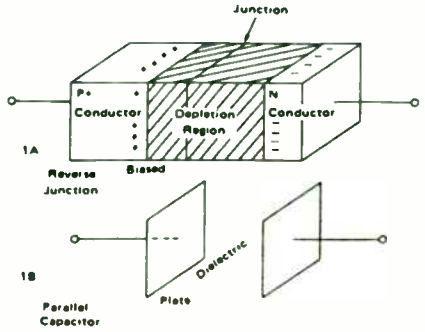

FIGURE 1 - Tuning Diode Capacity Analogy

$$C = \frac{\epsilon A}{d} \qquad (1)$$

where ϵ = dielectric constant of silicon equal to $11.8 \times \epsilon_0$

$\epsilon_0 = 8.85 \times 10^{-12}$ F/m

A = Device cross sectional area

d = Width of the depletion layer.

The depletion layer width d may be determined from semiconductor junction theory.

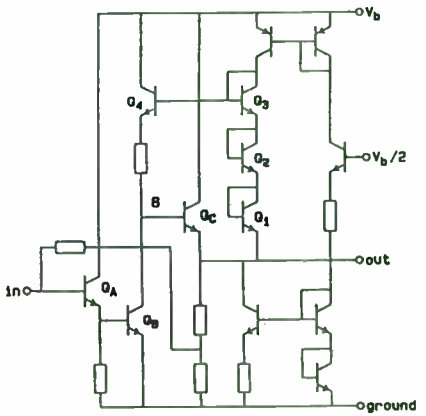

Fig. 4. Complete circuit diagram of the amplifier.

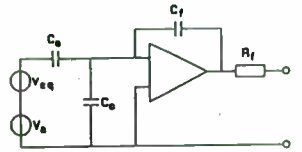

Fig. 5. Equivalent noise voltage in series with the antenna voltage.

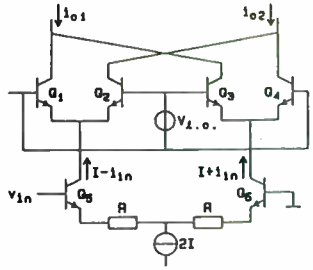

Fig. 8. Double-balanced switching mixer. V_{lo} is the local-oscillator signal.

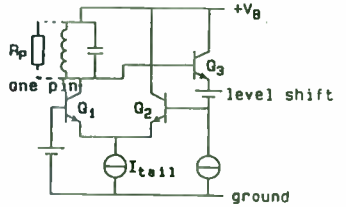

Fig. 9. Basic negative-resistance oscillator.

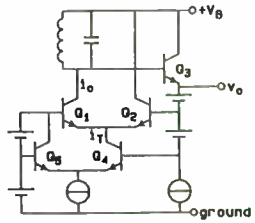

Fig. 10. AGC by tail-current modulation.

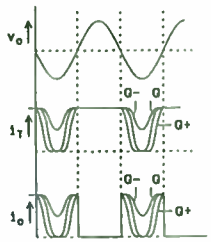

Fig. 11. Waveforms in the circuit of Fig. 10.

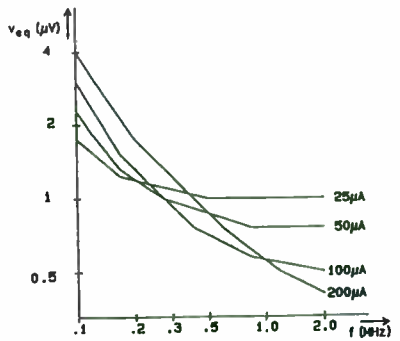

Fig. 6. Equivalent input noise versus frequency with bias current of the first stage as parameter.

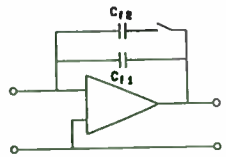

Fig. 7. Gain control by switching the feedback-capacitor values.

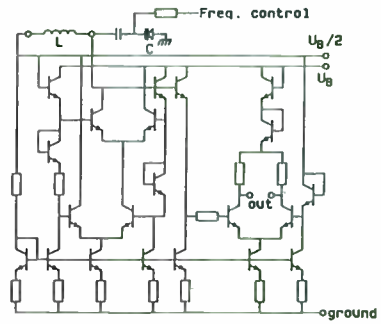

Fig. 12. Complete circuit diagram of oscillator-buffer.

The more accepted method of determining tuning diode capacitance is to use the defining formula for capacitance.

$$C = \frac{dQ}{dV} \qquad (2)$$

The charge, Q per unit area, is defined as:

$$Q = \epsilon E \qquad (3)$$

where E = Electric field

So we have capacitance per unit area:

$$c = \frac{C}{A} = \epsilon \frac{dE}{dV} \qquad (4)$$

Norwood and Shatz use these ideas to develop a general formula:

$$c = \left[\frac{q B \epsilon^{m+1}}{(m+2)(V+o)} \right]^{1/m+2} \qquad (5)$$

m = Impurity exponent

c = Capacitance per unit area

Lumping all the constant terms together, including the area of the diode, into one constant, C_D we arrive at:

$$C_J = \frac{C_D}{(V+\phi)^{\gamma}} \qquad (6)$$

where γ = Capacitance Exponent, a function of impurity exponent

ϕ = The junction contact potential ($\approx$0.7 Volts)

The capacitance constant, C_D, can be shown to be a function of the capacitance at zero voltage and the contact potential. At room temperature we have:

$$C_D = C_o(\phi)^{\gamma} \qquad (7)$$

C_o = Value of capacitance at zero voltage

The simple formula given in Eq. 6, very accurately predicts the voltage-capacitance relationship of tuning diodes. There are many detailed derivations of junction capacitance, so further explanation is not necessary in this paper.

The capacitance of commercial tuning diodes must be modified by the case capacitance.

The equation then becomes:

$$C = C_C + C_J \qquad (8)$$

where

C_C = Case capacitance typically 0.1 to 0.25 pF

C_J = Junction capacitance given by equation 6.

The Schottky Diode Mixer

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INTRODUCTION

A major application of the Schottky diode is the production of the difference frequency when two frequencies are combined or mixed in the diode. This mixing action is the result of the non-linear relationship between current and voltage, usually expressed as

$$I = I_s(e^{\frac{q(V-IR_s)}{nkT}} - 1)$$

The series resistance, R_s, is a parasitic element representing bulk resistance of the semiconductor and contact resistance. It is sometimes confused with dynamic resistance which is the sum of the series resistance and the resistance of the junction where the frequency conversion takes place. The ideality factor, n, is unity for an ideal diode and less than 1.1 for a silicon Schottky diode.

Variations in n are not important for n less than 1.1. The effect of saturation current, Is, is very important when the level of local oscillator power is low. This will be demonstrated by comparing results of mixing with diodes having different values of saturation current. Although temperature, T, is seen in the exponential and is present in a more complicated manner in saturation current, the effect on mixing efficiency is less than 0.5 dB for 100 degrees C change in temperature. Electron charge, q, and Boltzmann constant, k, may be combined in the equation

$$I = I_s(e^{\frac{V-IR_s}{.026}} - 1) \qquad (1)$$

Conversion Loss

Mixing efficiency is measured by the conversion loss, the ratio of signal input power to intermediate frequency output power. The intermediate frequency is the difference between the signal frequency and the local oscillator frequency. The diode may also generate the sum of these two frequencies. In this case the mixer may be called an upconverter. For a given local oscillator frequency, the difference frequency may be produced by two signal frequencies - one above the l.o. frequency and one below. Of course noise is also contributed at these two frequencies. In some cases, the mixer is designed to respond to both these frequencies. A mixer of this type is called a double sideband mixer. More commonly the mixer is designed to respond to one of these inputs. Since noise comes from both frequencies the double sideband mixer is better - typically 3 dB better.

Noise figure is another measure of mixing efficiency. This is the ratio of signal to noise ratio at the input to signal to noise ratio at the output. Single and double sideband definitions apply to noise figure also. In some applications noise figure and conversion loss are essentially equal. However, noise figure includes diode noise which becomes significant at intermediate frequencies in the audio range (1/f noise). In these applications noise figure may be much larger than conversion loss.

TUNING RATIOS/MANUFACTURING PROCESSES

The tuning or capacitance ratio, TR, denotes the ratio of capacitance obtained with two values of applied bias voltage. This ratio is given by the following expression for the tuning diode junction.

$$TR = \frac{C_J(V_2)}{C_J(V_1)} = \left[\frac{V_1+\phi}{V_2+\phi}\right]^{\gamma} \quad (9)$$

where $C_J(V_1)$ = Junction capacitance at V_1

$C_J(V_2)$ = Junction capacitance at V_2

where $V_1 > V_2$

In specifying T/R, some tuning diode data sheets use four volts for V_2. However, in order to achieve larger tuning ratios, the devices may be operated at slightly lower bias levels with some degradation in the Q specified at four volts. (See the discussion of Q versus voltage in the circuit Q section, later in this paper.) Furthermore, care must be taken when operating tuning diodes at these low reverse bias levels to avoid swinging the diode into forward conduction upon application of large ac signals. These large signals may also produce distortion due to capacitance modulation effects.

Since the effects of ϕ and case capacitance, C_C, are usually small, Eq. 9 may be simplified to the following for most design work:

$$TR = \frac{C(V\text{min})}{C(V\text{max})} = \left[\frac{V\text{max}}{V\text{min}}\right]^{\gamma} \quad (10)$$

The frequency ratio is equal to the square root of the tuning ratio. This tunable frequency ratio assumes no stray circuit capacitance.

Another parameter of importance is γ, the capacitance exponent. Physically, γ depends on the doping geometry employed in the diode. Varactor diodes with γ values from 1/3 to 2 can be manufactured by various processing techniques. The types of junctions, their doping profiles, and resulting values of γ are shown in Figure 2. These graphs show the variation of the number of acceptors (N_A) and the number of donors (N_D) with distance from the junction.

Abrupt junctions are the easiest to manufacture. This type of junction gives a γ of approximately 1/2 and a tuning ratio on the order 3 with the spcified voltage range. Therefore the corresponding frequency range which may be tuned is about 1.7 to 1.0. A typical example is the IN5441A:

$C(V_2) = C_{(30\ V)} = 2.34$ pF

$C(V_1) = C_{(4\ V)} = 6.8$ pF

$TR = 2.9$

$\gamma = 0.47$

The subscripts on the capacitance refer to the bias voltage applied.

In many applications such as tuning the television channels or the AM broadcast bands, a wider frequency range is required. In this event, the circuit designer must use a tuning diode with a hyper-abrupt junction. The hyper-abrupt junction TD has a γ of one or two and much larger turnable frequency range than does the abrupt junction TD. Table I shows typical types of tuning diodes available and their unique characteristics. Figure 2 also shows the processing steps necessary to achieve the desired capacitance exponent. To produce an abrupt junction a P+ diffusion forms the anode in an epitaxial layer which is the cathode. To produce a hyper-abrupt junction

Another complication of noise figure is the effect of the amplifier following the mixer. Diode manufacturers include the effect of a 1.5 dB noise figure IF amplifier in the mixer noise figure. Mixer manufacturers do not include this amplifier in the mixer noise definition. In this paper diode efficiency will be measured by conversion loss.

Parasitic Losses

The diode equivalent circuit of Figure 1 shows the presence of two elements that degrade performance by preventing the incoming signal from reaching the junction resistance where the mixing takes place. The effect of junction capacitance and series resistance was studied by comparing conversion loss data measured with three diodes covering a wide range of these parameters. The 5082-2800 is a general purpose diode, typically used in switching circuits. The 5082-2817 is a 2 GHz mixer diode. The 5082-2755 is a 10 GHz detector diode. Figure 2 shows the conversion loss measured at 2 GHz for these three diodes.

The 5082-2800 general purpose diode has a conversion loss several dB worse than that of the other diodes. This is expected because this diode has a higher junction capacitance. The behavior of the low capacitance 5082-2755 detector diode is more interesting. At local oscillator power levels below -3 dBm the conversion loss is better than the loss of the 5082-2817 mixer diode, but at higher power levels it is worse.

A good approximation to the effect of junction capacitance and series resistance on conversion loss is:

$$L_1 = 1 + \frac{R_s}{R_j} + w^2 C_j^2 R_s R_j \qquad (2)$$

This is the ratio of available power to the power delivered to the junction resistance, R_j, using the diode equivalent circuit of Figure 1. The value of junction capacitance varies with voltage as

$$C_j = \frac{C_o}{\sqrt{1 - \frac{V}{0.6}}} \qquad (3)$$

where 0.6 is a typical value of barrier voltage.

The relative values of conversion loss in Figure 2 may be explained by these equations. Zero bias capacitances for the three diodes were measured to be 0.84 pF, 1.29 pF, and 0.13 pF for the -2817, -2800, and -2755 diodes respectively.

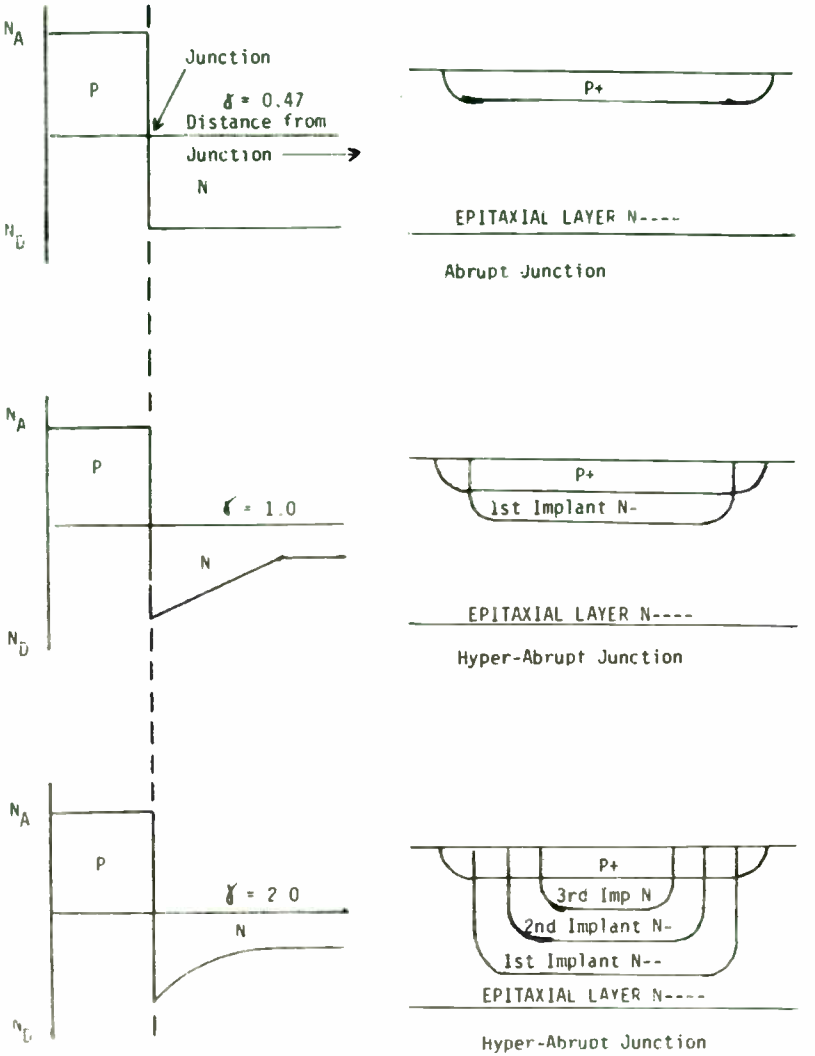
At a local oscillator power level of 1 milliwatt the forward current is about 1 milliampere. Using the corresponding forward voltages, C_j is computed for the three diodes. Assuming a junction resistance of 150 ohms, reasonable values of series resistance may be chosen to make the relative values of L_1 correspond to the relative measured values.

The familiar junction resistance equation $R_j = \frac{26}{I}$ does not apply for I= rectified current. It refers to I= DC bias current. When

Device Series	Capacitances Available	Tuning Radio	Tuning Voltage		Freq. Ratio	Junction Type
1N5139	6.8-47 pF	2.9-3.4	4-60 V	0.47	1.7-1.85	Abrupt
1N5441A	6.8-100 pF	2.9-3.1	2-30 V	0.47	1.7-1.75	Abrupt
MV105G	10 pF	4.5	3-25 V	1.0	2.12	Hyper-Abrupt
MV3102	22 pF	5.0	3-25 V	1.0	2.25	Hyper-Abrupt
MV209	29 pF	5.5	3-25 V	1.0	2.35	Hyper-Abrupt
MV1403	120-250 pF	12	2-10 V	2.0	3.5	Hyper-Abrupt
MVAM108	500 pF	16	1-8 V	2.0	4	Hyper-Abrupt

TABLE 1

with a γ of 1.0 it is necessary to "grade" the epitaxial layer with an ion impant. This produces a tuning diode with a tuning ratio of 4 to 6 when a supply voltage of 25 volts is available. The final challenge to tuning diode designer is to produce a junction with a tuning ratio in excess of 10 with a supply voltage of only 10 volts or less. For this characteristic a hyper-abrupt junction with a γ = 2.0 is required. It is produced by "grading" this epitaxial layer with a triple ion implant. The ability of the manufacturer to place these implants in the epitaxial layer in a repeatable manner as well as the uniformity of the epitaxial layer determines the consistency of the device to device C-V curve



EXAMPLE 2 - Doping Profiles and Manufacturing Processes for Common Types of Tuning Diodes

rectified current is 1 mA, instantaneous current varies over forward and reverse values. Junction resistance is very large when the current is negative so the average junction resistance is larger than predicted by this equation.

Diode	C (pF)	R (ohms)	L (dB)
2817	1.3	6	1.07
2800	2.2	16	4.68
2755	0.24	50	1.47

At -3 dBm the 2817 and 2755 curves cross, with the 2800 loss 4.5 dB higher. This relative loss can be explained by raising R to 235 ohms and decreasing the capacitance values.

Diode	C (pF)	L (dB)
2817	1.12	1.2
2800	2.1	5.7
2755	0.23	1.2

These values of C_j and R_s were chosen to illustrate the effect on conversion loss. Since saturation currents are different for these diodes and junction resistances may be different, the actual values of C_j and R_s may be somewhat different.

Equation 2 shows the loss behavior with frequency. At low frequencies the loss is independent of frequency and capacitance. Choosing a low value of series resistance provides the best diode. At high frequencies low capacitance becomes more important than low series resistance because capacitance is squared in the equation. Figure 3 shows L_1 vs frequency for the 5082-2835 diode with R_s = 6 ohms and C_j = 1.0 pF and for the HSCH-5310 diode with R_a = 17 ohms and C_j = 0.1 pF. The lower capacitance makes the -5310 the better diode at microwave frequencies while the lower resistance makes the -2835 the better diode at low frequencies.

The Effect of Barrier Voltage

The type of metal deposited on silicon to form a Schottky barrier influences the barrier voltage which is involved in the saturation current determining the forward current. We use the term low barrier for diodes with low values of voltage for a given current (usually 1 mA). We have previously shown the effect of barrier voltage on the variation of junction capacitance with forward voltage.

Figure 4 shows the measurement of conversion loss for three diodes having a range of barrier potential values.

Diodes	Barrier Potential
5082-2817	0.64
5082-2835	0.56
HSCH-3486	0.35

CIRCUIT Q

Popular types of mechanical tuning capacitors often have Q's on the order of a thousand or greater. The Q of tuned circuits using these capacitors is generally dependent only on the coil. When using a tuning diode, however, one must be conscious of the tuning diode Q as well. The Q of the tuning diode is not constant being dependent on bias voltage and frequency. The Q of tuning diode capacitors falls off at high frequencies, because of the series bulk resistance of the silicon used in the diode. The Q also falls off at low frequencies because of the back resistance of the reverse-biased diode.

The equivalent circuit of a tuning diode is often described as shown:

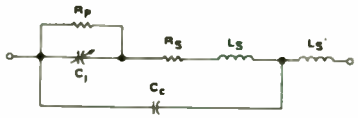


FIGURE 3 - Equivalent Circuit of a Tuning Diode

where

R_P = Parallel resistance or back resistance of the diode

R_S = Bulk resistance of the silicon in the diode

L_S' = External lead inductance

L_S = Internal lead inductance

C_C = Case capacitance

Normally we may neglect the lead inductance and case capacitance. This results in the simplified circuit of Figure 4.

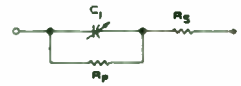


FIGURE 4 - Simplified Equivalent Circuit of A Tuning Diode

The tuning diode Q may be calculated with equation 11.

$$Q = \frac{2\pi f C R_p^2}{R_s + R_p + (2\pi f C)^2 R_s R_p^2} \qquad (11)$$

This rather complicated equation is plotted in Figure 5 for RS = 1.0 ohm,

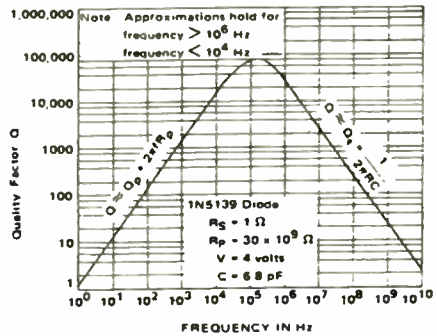


FIGURE 5 - Graph of Q versus Frequency

At low LO power levels the lower barrier diodes have better performance, significantly better for the lowest barrier diode, the HSCH-3486. At higher power levels this diode loses its advantage because of higher series resistance. The 5082-2835 has lower capacitance and lower series resistance so its performance is better than the 5082-2817 at all power levels. The maximum rated power level of 150 mW is not high enough to demonstrate the increase in conversion loss seen at high power levels for the other diodes.

Effects of DC Bias and Local Oscillator Power Level

Figure 5 shows the conversion loss of a 5082-2817 mixer diode measured at 2 GHz. The top curve was measured without DC bias. Optimum DC bias was applied at each level for the bottom curve. The curves meet at the optimum local oscillator level where bias does not help. Below this level forward bias is used. Above this level reverse bias is used to reduce the rectified current.

At low levels of LO power, the conversion loss degrades rapidly unless DC bias is used. At -10 dBm the degradation is about 7 dB from the performance at the standard 0 dBm power level. Replacing the lost LO power with DC bias recovers about 6 dB of the degradation.

At high levels of LO power the performance degrades again. This is caused by the rapid increase of junction capacitance. Reverse bias reduces the current and the capacitance, restoring the diode performance.

Effect of Load Resistance

Figure 6 shows the effect of mixer load resistance on conversion loss. At low local oscillator power levels the effect is similar to the barrier effect. More rectified current flows with smaller load resistance so performance is better. At higher power levels the degradation due to higher capacitance appears first with the lower load resistances. As a result the optimum value of load resistance increases with LO power level. At +9 dBm 100 ohms becomes better than 10 ohms. AT +19.5 dBm 400 ohms becomes better than 100 ohms. The load circuit can be designed to provide the optimum resistance as the local oscillator power level changes.

HARMONIC DISTORTION

Sums and differences of multiples of the two mixing frequencies are produced in the mixing diode. These frequencies appear as spurious responses in the output. This effect was studied by setting the signal frequency at 2 GHz and the power at -30 dBm. The local oscillator was then set at various frequencies to produce harmonic mixing with a difference frequency of 30 MHz. Local oscillator power was one milliwatt. Then the local oscillator was set at 2 GHz and the signal frequency varied. The output levels in dB below fundamental mixing are shown in Figure 7. The diode was placed in a 50 ohm untuned coaxial mount.

The output levels of the m1 products, mixing of the signal fundamental with multiples of the local oscillator, are much higher than

$R_p = 30 \times 10^9$ ohms, at V = 4 volts and C = 6.8 pF, typical for a 1N5139 tuning diode at room temperature.

At frequencies above several MHz, the Q decreases directly with increasing frequency by the simpler formula given below:

$$Q \approx Q_S = \frac{1}{2\pi f C R_s} \quad \text{(High Frequency Q)} \qquad (12)$$

The emphasis today is on decreasing R_s so better high frequency Q can be obtained. At low frequencies Q increases with frequency since only the component resulting from R_p, the back resistance of the diode, is of consequence.

$$Q \approx Q_p = 2\pi f C R_p \quad \text{(Low frequency Q)} \qquad (13)$$

Q is also dependent on voltage and temperature. Higher reverse bias voltage yields a lower value of capacitance, and also since R_s decreases with increasing bias voltage, the Q increases with increasing voltages. Similarly, low reverse bias voltages accompany larger capacitances, and lower Q's. Increasing temperature also lowers the Q of tuning diodes. As the junction temperature increases, the leakage current increases, lowering R_p. There is also a slight decrease in R_s with increasing temperature, but the effects of the decreasing R_p are greater and this causes the Q to decrease. The effects of temperature and voltage on the Q of a 1N5139 at 50 MHz are plotted in Figure 6.

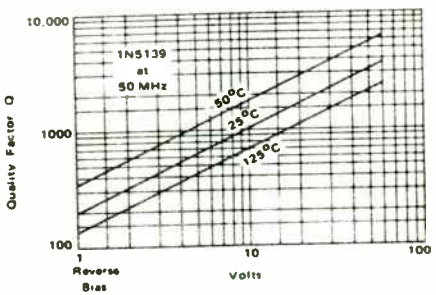
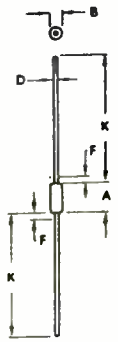


FIGURE 6 - Q versus Reverse Bias and Temperature

PACKAGE CONSIDERATIONS

Tuning diodes are available in a variety of packages. Two common ones are the axial lead DO204AA, previously referred to as the DO7 and the radial lead TO226AC, sometimes called the two lead TO92. The DO204AA is a hermetically sealed glass package wheras the TO226AC is a plastic encapsulated one. Figures 7 and 8 show the form and dimensional analysis of these two packages. The cost of a tuning diode



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.84	7.62	0.230	0.300
B	2.16	2.72	0.085	0.107
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	25.40	38.10	1.000	1.500

FIGURE 7 - DO204AA Dimensional Analysis

the 1n products, mixing of the local oscillator fundamental with multiples of the signal. For example, the 2x1 output is 5 dB below fundamental. Figure 5 shows that this level of fundamental mixing corresponds to a local oscillator level of -8 dBm. The doubling efficiency was about 8 dB. The 1x2 output is 16 dB below fundamental mixing. This corresponds to a signal level of -46 dBm. The doubling efficiency is 16 dB for the lower level signal frequency. Although fundamental mixing in Figure 5 was measured in a tuned system and the data of Figure 7 was measured in an untuned system, this analysis nevertheless gives a comparison of multiplying at the one milliwatt and one microwatt power levels. Mixing of signal multiples above 2 with local oscillator multiples above the fundamental produced outputs below the -100 dBm sensitivity of the receiver.

Harmonic Mixing

While harmonic products are usually considered spurious, in some designs the desired output is the result of harmonic mixing. This is a valuable mixer technique when the frequency is so high that it is difficult to generate the local oscillator power. Hewlett-Packard Application Note 991, "Harmonic Mixing With the HSCH-5500 Series Dual Diode" describes a technique using the 2nd harmonic of the local oscillator with little loss of efficiency compared to fundamental mixing. Mixers using the 6th, 8th, and 10th harmonics are used to extend the range of Hewlett-Packard spectrum analyzers to 60 GHz.

Two Tone Distortion

Harmonic distortion may be suppressed by a band pass filter at the mixer input. When the distortion is caused by

$$m f_{LO} - n f_s = f_{if}$$

the unwanted frequency is

$$f_s = \frac{m}{n} f_{LO} - \frac{f_{if}}{n} \qquad (4)$$

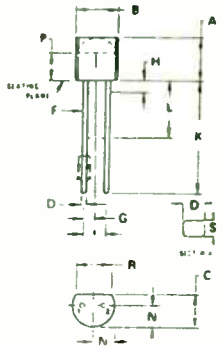
The narrowest filter required corresponds to m = n = 2 with a rejection bandwith equal to the intermediate frequency.

Two tone distortion is the result of two unwanted signals mixing with each other and the local oscillator to produce an intermediate frequency output. The equation is

$$f_{LO} - m f_1 + n f_2 = f_{if} \qquad (5)$$

Third order two tone intermod may correspond to m = 2, n = 1. In this case the correct intermediate frequency is produced when the desired signal f_s equals $2f_1 - f_2$. The unwanted frequencies may be arbitrarily close to the desired frequency so the problem cannot be solved with a filter.

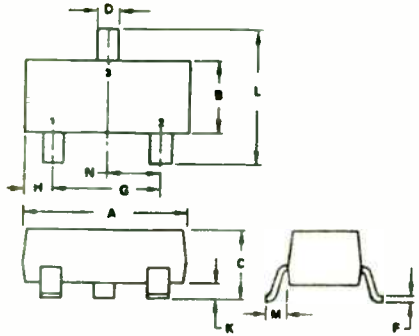
Third order two tone distortion in a 5082-2817 diode was investigated with a local oscillator frequency of 1.94 GHz and input



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	—	1.27	—	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—
S	0.36	0.41	0.014	0.016

FIGURE 8 - TO226AC Dimensional Analysis

package is a function of its piece parts cost and its adaptability toward automation in the assembly process. Because of its relatively expensive piece parts and non-adaptability toward automated assembly the DO204AA is the most expensive tuning diode package, but it does provide a hermetically sealed environment for the tuning diode die. On the other hand, the TO226AC has much less expensive piece parts and is very highly adaptable to automated assembly, but it is not a hermetically sealed package. Tuning diodes are also now available in a surface mount package. This package is available in the TO236AA (standard profile) and TO236AB (low profile) configurations. This package is also commonly known as SOT23. Figure 9 shows the form and dimensional analysis of the package. Due to size constraints about the largest capacitance tuning diode available in the package is 33 pF. This barrier will



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.472	0.0551
C	0.85	1.20	0.033	0.0472
D	0.37	0.50	0.0150	0.020
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.45	0.60	0.0177	0.0236
K	0.10	0.25	0.0040	0.0098
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.0180	0.0236
N	0.89	1.02	0.0350	0.0401

FIGURE 9 TO236AA Dimensional Analysis

surely be broken by the development of larger surface mount packages. At this time the cost of a surface mount package is somewhat higher than that of the two lead TO92, but because the surface mount package is highly adaptable to automated assembly it is expected that as the use of surface mount packages increases this volume will reach the point where the piece parts cost of the package will approach that of the two lead TO92.

MANUFACTURER'S DATA SHEETS

This section will discuss the information available to the designer from typical

frequencies of 2 GHz and 1.985 GHz. The intermediate frequency was 2 x 1.985 - 2 - 1.94 = 0.03 GHz. The measure of distortion is the input intercept point, the power level where the line of output vs input power for the desired mixing intersects the extension of the spurious line. This is shown in Figure 8. Since the desired output is linear, the suppression of the spurious output is 2A and input intercept is input power plus half the suppression.

With the help of this relationship the intercept point was measured as a function of local oscillator power level. The results are shown in Figure 9. At higher local oscillator power levels the desired output increases while the spurious output decreases. This raises the suppression and the intercept point. At lower levels both desired output and spurious decrease so the intercept point levels off to a constant value.

Tuning for Better Sensitivity

The ideal mixer should convert all of the signal power to output power at the desired output frequency. However, it is customary to test diodes in a broadband mixer circuit. In this test no attempt is made to recover the power lost in the unwanted output frequencies. Because of these losses and the losses in the diode parasitics, an efficiency of about 35% is usually achieved.

Special circuits have been developed to improve this figure to come closer to the ideal 100% efficiency. The most serious spurious response, called the image response, produces an output at the frequency $2 f_{LO} - f_S$. Image recovery mixers are designed to recover this lost power. Two dB improvement has been reported. By properly terminating harmonics up to the third, conversion loss under 2 dB was obtained with a Hewlett-Packard beam lead diode.

MULTIPLE DIODE MIXERS

Although the intermediate frequency may be produced by mixing in a single diode, very few mixers are made this way. The problems generated by using a single diode include radiation of local oscillator power from the input port, loss of sensitivity by absorption of input power in the local oscillator circuit, loss of input power in the intermediate frequency amplifier, and the generation of spurious output frequencies by harmonic mixing. Some of these problems may be solved by circuit techniques but these circuits often introduce new problems. Most mixers use multiple diode techniques to better solve these problems.

Early mixer designs prevented loss of signal power in the local oscillator circuit by loosely coupling the local oscillator power to the mixer diode. This technique is wasteful of local oscillator power and it sends as much power to the input, possibly an antenna, as it sends to the diode. This local oscillator radiation could be interpreted as a target return when received by a radar. This problem may be alleviated by using

manufacturer's data sheets. Figure 10 shows the first page of a data sheet for an abrupt junction TD. It normally includes basic type information, maximum ratings and package mechanical information. Figure 11 shows the second page of this data sheet. Information on this page concentrates on electrical characteristics and parameter test methods, as well as including the first graph of a typical characteristic - normalized capacitance versus temperature at various reverse bias voltages. Figure 12 shows the third page of the data sheet. It includes the graphs of most interest to the designer. These include: diode capacitance versus reverse voltages, (C-V curve) figure of merit (Q) versus reverse voltage at a fixed frequency and versus frequency at a fixed voltage, reverse current versus reverse bias voltage for three temperatures and forward voltage versus forward currents. Figure 13 shows the first page of a data sheet for a hyper-aburpt junction tuning diode. It includes primarily the same information as on the first page of the data sheet for the abrupt junction tuning diode. Figure 14 shows the second page of this data sheet. It again includes a table of electrical characteristics, but in this case also shows a C-V curve and a graph of figure of merit (Q) versus voltage at a fixed frequency. A useful comparison is the C-V curve of the abrupt junction diode versus that of the hyper-abrupt junction diode.

1N5441A,B,C thru 1N5456A,B,C

VVC

SILICON EPICAP▲ DIODES

. . . epitaxial passivated abrupt junction tuning diodes designed for electronic tuning, FM, AFC and harmonic-generation applications in AM through UHF ranges, providing solid-state reliability to replace mechanical tuning methods.

- Excellent Q Factor at High Frequencies
- Guaranteed Capacitance Change – 2.0 to 30 V
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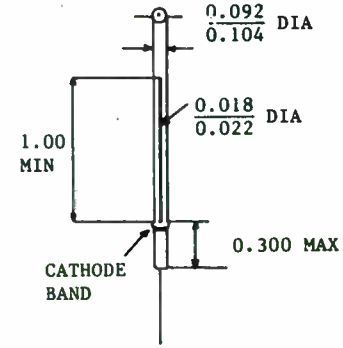
- Capacitance Tolerance – 10%, 5.0%, and 2.0%
- Complete Typical Design Curves

VOLTAGE-VARIABLE CAPACITANCE DIODES

6.8 – 100 pF
30 VOLTS

DS 8526

DO-7 GLASS



CASE 51
DO-7

** MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	30	Volts
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 2.67	mW mW/°C
Operating Junction Temperature Range	T_J	+175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

**Indicates JEDEC Registered Data

FIGURE 10

a directional coupler to send the local oscillator power to the mixer diode. Coupling must be loose so that LO power is still wasted.

A balanced mixer (Figure 10) provides a better solution. The hybrid circuit splits the LO power to the two diodes with little coupling to the antenna. A low pass filter is needed to prevent loss of power to the intermediate frequency amplifier. Additional advantages are reduction of LO noise and harmonic mixing. LO noise is rejected because two signals originating in the same port produce IF outputs that cancel. This is a property of the hybrid circuit. Similarly, even order harmonics of either the LO or the signal produce cancelling outputs.

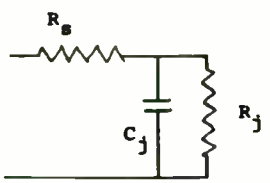
In the double balanced mixer (Figure 11) even order harmonics of both the LO and the signal frequency are rejected. This mixer does not require a low pass filter to isolate the IF circuit. The three ports are isolated from each other by the symmetry of the circuit. These mixers usually cover a broader band than the others. Ratios as high as 1000:1 are available. Microwave equivalents of these mixer circuits are available. Bandwidth ratios as high as 40:1 are available at microwave frequencies.

Intermodulation distortion is reduced when local oscillator power is increased. Several design techniques are used to allow higher drive.

A higher barrier diode may be used to retain linear response at higher drive levels. More than one diode may be used in each arm of the ring in a double balanced mixer. This permits higher drive level without overheating the diodes. Two rings may also be used to increase the local oscillator level. This technique is also used for image tuning described earlier.

Summary:

Schottky diode mixing efficiency is related to both diode parameters and circuit parameters. Diode parameters studied include capacitance, resistance, and barrier voltage. Circuit parameters include DC bias and load resistance. Harmonic response and third order two tone intermodulation were also studied.



EQUIVALENT CIRCUIT
FIGURE 1

**ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic – All Types	Test Conditions	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage	I_R = 10 μAdc	BV_R	30	–		Vdc
Reverse Voltage Leakage Current	V_R = 25 Vdc, T_A = 25°C V_R = 25 Vdc, T_A = 150°C	I_R	–	–	0.02 20	μAdc
Series Inductance	f = 250 MHz, lead length ≈ 1/16"	L_S		4.0	10	nH
Case Capacitance	f = 1.0 MHz, lead length ≈ 1/16"	C_C	0.1	0.17	0.25	pF
Diode Capacitance Temperature Coefficient (Note 6)	V_R = 4.0 Vdc, f = 1.0 MHz	TC_C	–	300	400	ppm/°C

Device	C_T, Diode Capacitance* V_R = 4.0 Vdc, f = 1.0 MHz, pF			TR, Tuning Ratio C_2/C_{30} f = 1.0 MHz		Q, Figure of Merit V_R = 4.0 Vdc f = 50 MHz
	Min (Nom −10%)	Nom	Max (Nom +10%)	Min	Max	Min
1N5441A	6.1	6.8	7.5	2.5	3.1	450
1N5442A	7.4	8.2	9.0	2.5	3.1	450
1N5443A	9.0	10.0	11.0	2.6	3.1	400
1N5444A	10.8	12.0	13.2	2.6	3.1	400
1N5445A	13.5	15.0	16.5	2.6	3.1	400
1N5446A	16.2	18.0	19.8	2.6	3.1	350
1N5447A	18.0	20.0	22.0	2.6	3.1	350
1N5448A	19.8	22.0	24.2	2.6	3.2	350
1N5449A	24.3	27.0	29.7	2.6	3.2	350
1N5450A	29.7	33.0	36.3	2.6	3.2	350
1N5451A	35.1	39.0	42.9	2.6	3.2	300
1N5452A	42.3	47.0	51.7	2.6	3.2	250
1N5453A	50.4	56.0	61.6	2.6	3.3	200
1N5454A	61.2	68.0	74.8	2.7	3.3	175
1N5455A	73.8	82.0	90.2	2.7	3.3	175
1N5456A	90.0	100.0	110.0	2.7	3.3	175

*To order devices with C_T Nom ±5.0%, or ±2.0% add Suffix B or C respectively.

**Indicates JEDEC Registered Data.

PARAMETER TEST METHODS

1. **L_S, Series Inductance**
   L_S is measured on a shorted package at 250 MHz using an impedance bridge (Boonton Radio Model 250A RX Meter or equivalent).

2. **C_C, Case Capacitance**
   C_C is measured on an open package at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

3. **C_T, Diode Capacitance**
   $(C_T = C_C + C_j)$. C_T is measured at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

4. **TR, Tuning Ratio**
   TR is the ratio of C_T measured at 2.0 Vdc divided by C_T measured at 30 Vdc.

5. **Q, Figure of Merit**
   Q is calculated by taking the G and C readings of an admittance bridge at the specified frequency, and substituting in the following equation:

$$Q = \frac{2\pi fC}{G}$$

(Boonton Electronics Model 33AS8 or equivalent).

6. **TC_C, Diode Capacitance Temperature Coefficient**
   TC_C is guaranteed by comparing C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = −65°C with C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = +85°C in the following equation which defines TC_C:

$$TC_C = \frac{|C_T(+85°C) - C_T(-65°C)|}{85 - (-65)} \cdot \frac{10^6}{C_T@25°C}$$

Accuracy limited by C_T measurement to ±0.1 pF.

– NORMALIZED DIODE CAPACITANCE versus JUNCTION TEMPERATURE

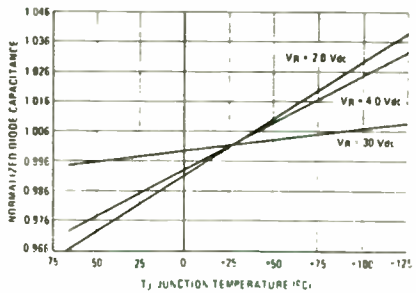
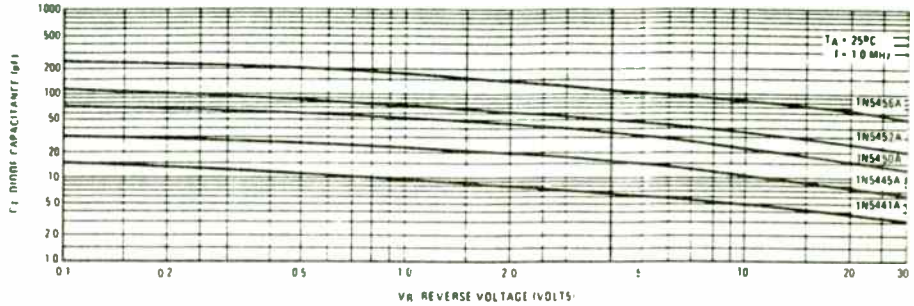


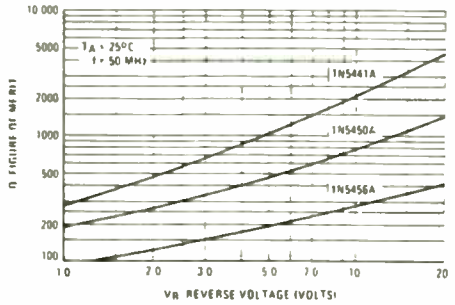
FIGURE 11

TYPICAL DEVICE PERFORMANCE

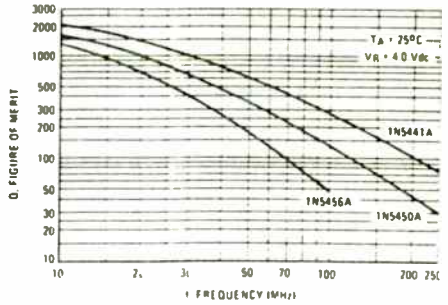
– DIODE CAPACITANCE versus REVERSE VOLTAGE



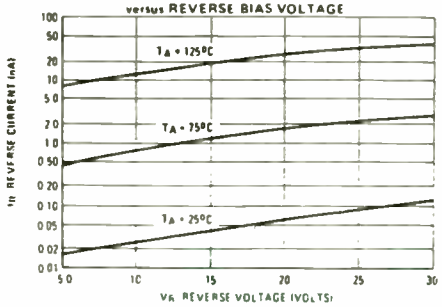
– FIGURE OF MERIT versus REVERSE VOLTAGE



– FIGURE OF MERIT versus FREQUENCY



– REVERSE CURRENT versus REVERSE BIAS VOLTAGE



– FORWARD VOLTAGE versus FORWARD CURRENT

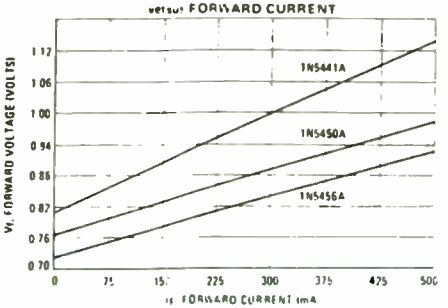
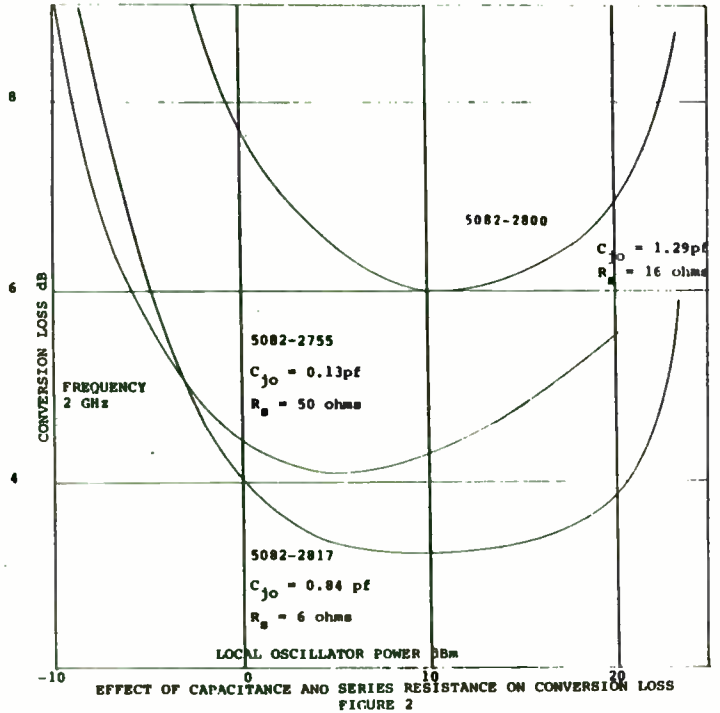
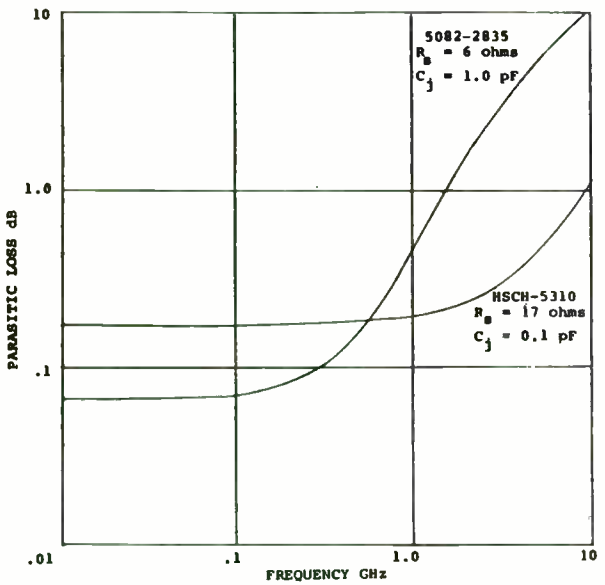


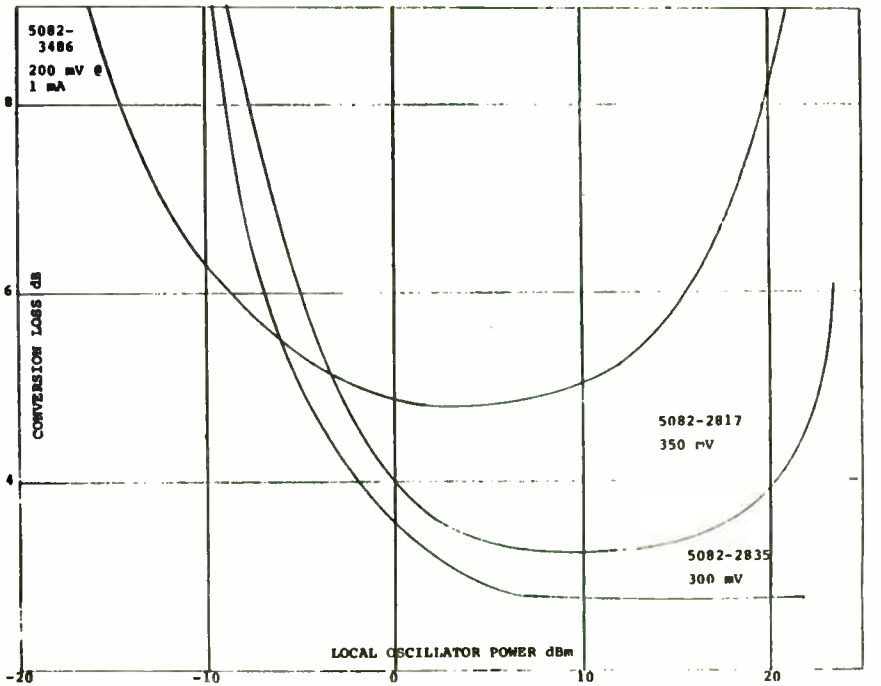
FIGURE 12



EFFECT OF CAPACITANCE AND SERIES RESISTANCE ON CONVERSION LOSS
FIGURE 2



PARASITIC LOSS
FIGURE 3



EFFECT OF BARRIER
ON CONVERSION LOSS
FIGURE 4

MVAM108 MVAM109 MVAM115 MVAM125

VVC

SILICON TUNING DIODE

designed for electronic tuning of AM receivers and high capacitance, high tuning ratio applications

- High Capacitance Ratio — C_R = 15 (Min)
  MVAM 108, 115, 125
- Guaranteed Diode Capacitance — C_t = 440 pF (Min) — 560 pF (Max) @ V_R = 1.0 Vdc, f = 1.0 MHz
  MVAM108, MVAM115, MVAM125
- Guaranteed Figure of Merit — Q = 150 (Min) @ V_R = 1.0 Vdc, f = 1.0 MHz

TUNING DIODES WITH VERY HIGH CAPACITANCE RATIO

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage — MVAM108	V_R	12	Volts
MVAM109		15	
MVAM115		18	
MVAM125		28	
Forward Current	I_F	50	mA
Power Dissipation @ T_A = 25°C	P_D	280	mW
Derate Above 25°C		2.8	mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +125	°C

— TYPICAL AM RADIO APPLICATION

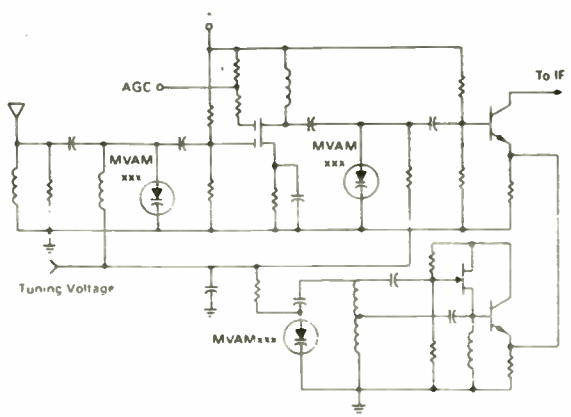
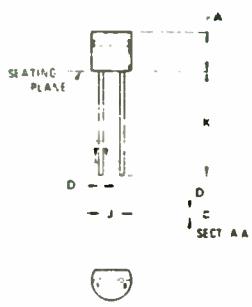


FIGURE 13



STYLE 1
PIN 1 ANODE
2 CATHODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.45	4.70	0.175	0.185
D	0.41	0.48	0.016	0.019
J	2.29	2.79	0.090	0.110
K	12.70	—	0.500	—

CASE 182-03

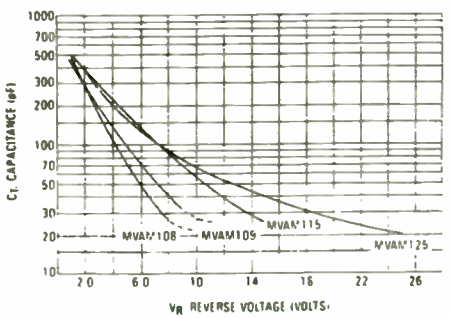
DS8016-E

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, Each Device)

Characteristic — All Types		Symbol	Min	Typ	Max	Unit
Breakdown Voltage (I_R = 10 μAdc)	MVAM108	$V_{(BR)R}$	12	—	—	Vdc
	MVAM109		15	—	—	
	MVAM115		18	—	—	
	MVAM125		28	—	—	
Reverse Current		I_R				nAdc
(V_R = 8.0 V)	MVAM108		—	—	100	
(V_R = 9.0 V)	MVAM109		—	—	100	
(V_R = 15 V)	MVAM115		—	—	100	
(V_R = 25 V)	MVAM125		—	—	100	
Diode Capacitance Temperature Coefficient (1) (V_R = 1.0 Vdc, f = 1.0 MHz, T_A = -40°C to +85°C)		TC_C	—	435	—	ppm/°C
Case Capacitance (f = 1.0 MHz, Lead Length = 1/16")		C_C	—	0.18	—	pF
Diode Capacitance (2) (V_R = 1.0 Vdc, f = 1.0 MHz)	MVAM108, 115, 125	C_t	440	500	560	pF
	MVAM109		400	460	520	
Figure of Merit (f = 1.0 MHz, Lead Length = 1/16")		Q	150	—	—	—
Capacitance Ratio (f = 1.0 MHz)	MVAM108	C_1/C_8	15	—	—	—
	MVAM109	C_1/C_9	12	—	—	
	MVAM115	C_1/C_{15}	15	—	—	
	MVAM125	C_1/C_{25}	15	—	—	

Notes
(1) The effect of increasing temperature 1.0°C at any operating point is equivalent to lowering the effective tuning voltage 1.25 mV. The percent change of capacitance per °C is nearly constant from -40°C to +100°C.
(2) Upon request: diodes are available in matched sets. All diodes in a set can be matched for capacitance to 3 or 2.0 pF (whichever is greater) at all points along the specified tuning range.

— CAPACITANCE versus REVERSE VOLTAGE



— FIGURE OF MERIT

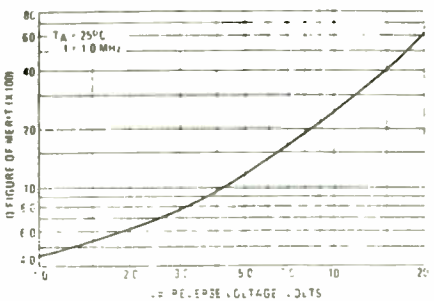
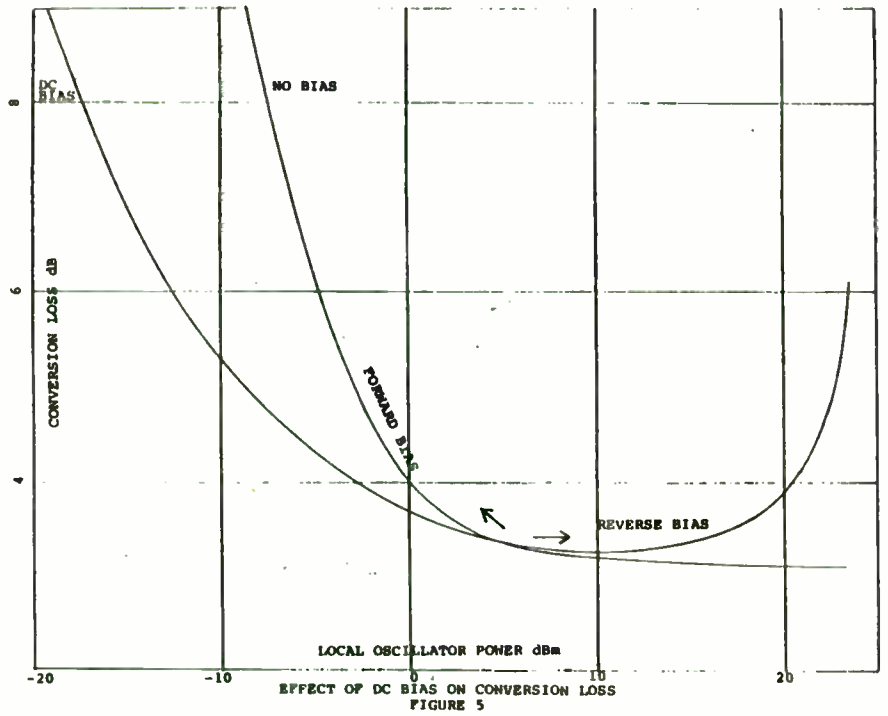
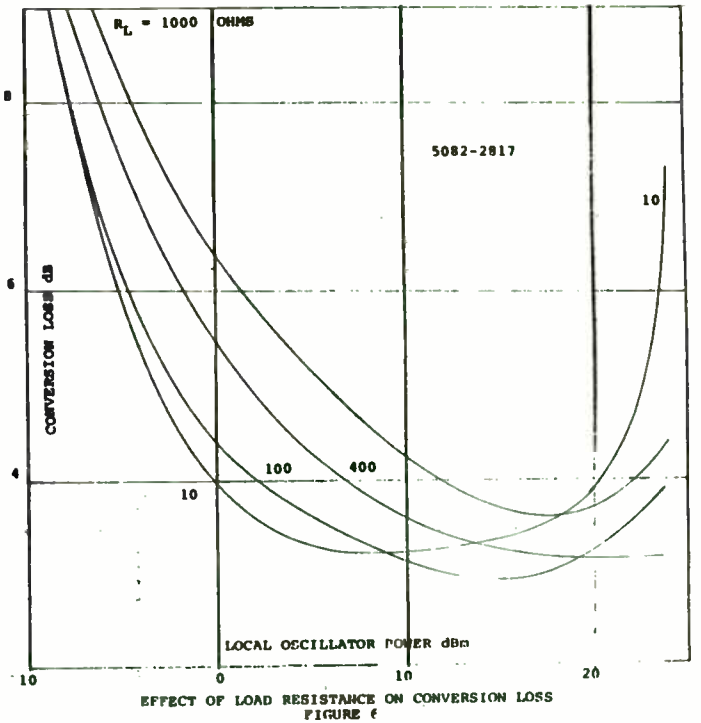


FIGURE 14



EFFECT OF DC BIAS ON CONVERSION LOSS
FIGURE 5



EFFECT OF LOAD RESISTANCE ON CONVERSION LOSS
FIGURE 6

SPECIFYING TUNING DIODES

Three common methods of specifying tuning diodes for a particular design application are as follow:

1. Specify a nominal capacitance ± the maximum allowed variation in percent at the lowest voltage which is to be used and a capacitance ratio minimum (and maximum if necessary) between the lowest voltage and highest voltage to be used in the design. This is the method found on most manufacturers' data sheets.
2. Specify a minimum and maximum capacitance at the lowest and highest voltages to be used in the design.
3. Specify a minimum and maximum capacitance at the lowest, the median, and highest voltages to be used in the design. This method enables the circuit designer to "tie down" the C-V curve of a hyper-abrupt junction tuning diode over a large voltage variation.

SUMMARY

Voltage variable capacitors commonly referred to as tuning diodes are rapidly replacing air capacitors in many applications. These devices offer many advantages over previously available variable capacitors, the major one, of course, is the ability to employ remote tuning which has made possible the electronically tuned radio. The circuit designer must be aware of the tuning range and Q limitations of tuning diodes in order to use these devices effectively. Also to be considered must be the package chosen and the cost thereof. A well constructed manufacturer's data sheet can provide the circuit designer with a wealth of information needed to aid him in his design, but the designer must realize that the manufacturer only specifies a capacitance at one voltage and a capacitance ratio between one pair of voltages. If necessary, the circuit designer must request these specifications for his own particular design voltages.

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2. Chang, Y.F., "Capacitance of p-n Junctions: Space Charge Capacitance." Journal of Applied Physics, 37:6, May 1966, pp. 2337-42.

3. Gimmel, H.K.; and Schauftter, D.L., "Depletion Layer Capacitance of p⁺n Step Junctions." Journal of Applied Physics, 38:5, April, 1967, pp. 2148-53.

4. Gray, P.E.; DeWitt, D.; Boothroyd, A.; Gibbons, J., Physical Electronics and Circuit Models of Transistors. New York, John Wiley & Sons, 1964, pp. 8-54.

5. Warner, R.; Fordemwalt, J., Integrated Circuits, Design Principles and Fabrication, New York, McGraw-Hill, 1965, pp. 31-68.

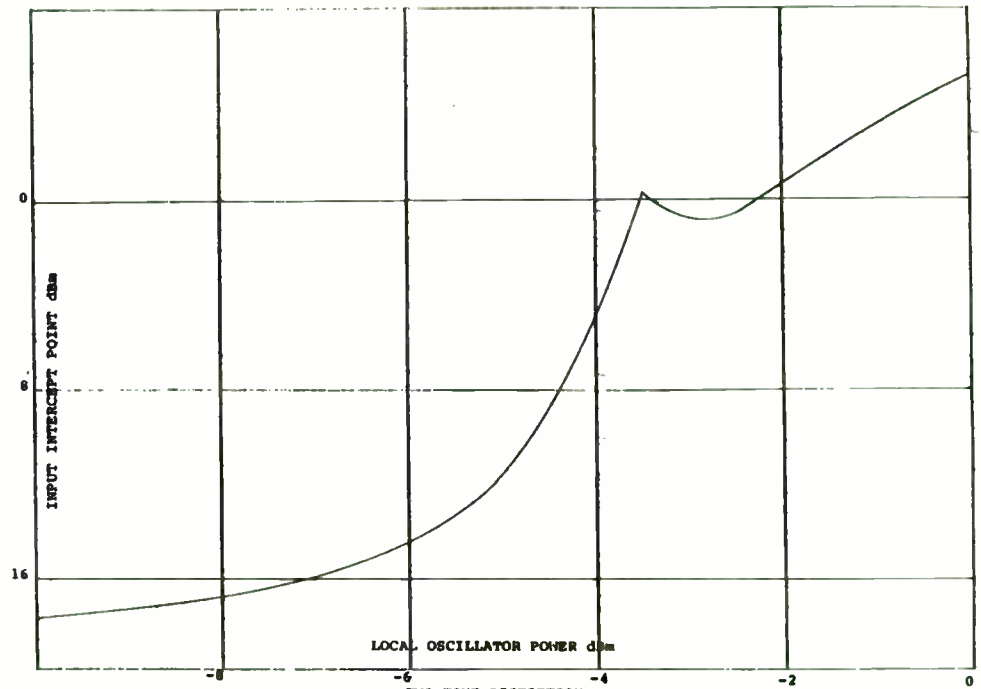
6. Doug Johnson and Roy Hejhall, "Tuning Diode Design Techniques," Motorola Application Note AN-551.

7. George C. Onodera, "Method of Producing an Ion Implanted Tuning Diode," United States Patent #4,106,953, August 15, 1978.

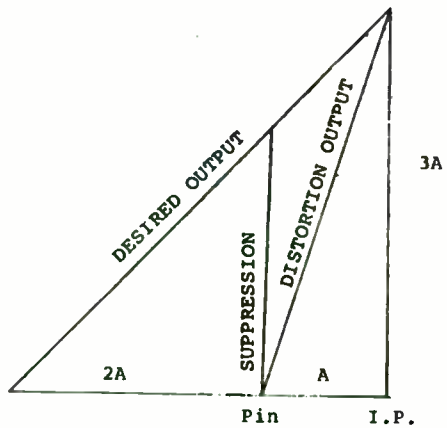
SIGNAL	1	2	3	4
4	43	42	X	X
3	21	56	X	X
2	16	45	38	39
1	0	5	13	19

LOCAL OSCILLATOR

HARMONIC DISTORTION
FIGURE 7

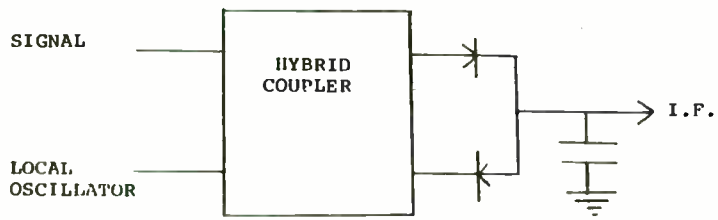


TWO TONE DISTORTION
FIGURE 9



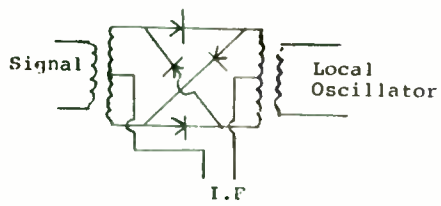
INTERCEPT POINT

FIGURE 8



BALANCED MIXER

FIGURE 10



DOUBLE BALANCED MIXER
FIGURE 11

DESIGN OF COAXIAL HIGH-PASS FILTERS HAVING VARIOUS TRANSFER PROPERTIES

by Dick Wainwright
Chief Scientist, Cir-Q-Tel, Inc.

Abstract: As explained in a companion paper 1/ "Design of Combline and Interdigitated Bandpass Filters" (usually with narrow band wide tuning range) the cost of construction depends heavily on the physical form assumed by the precision ground plane housing and the physical form and fit of the component parts/elements.

Various types of filters of highpass formulation are given. Pseudo-elliptic and all-pole Butterworth, Chebishev and other realizations such as Gaussian, etc. are described. The series capacitive elements may be formed as Teflon-insulated coaxial capacitors, the shunt elements of which may be composed of a simple helix or straight (coaxial) inductor for the all-pole designs or by a series inductor-capacitor combination for the Elliptic or Pseudo-elliptic high pass. n-odd values are in general preferred, which simplifies construction. Other classes of filters: Zobel, Levy A-Z, (Ref.6) Butterworth, Gaussian and Bessel all-pole (n-odd) are of similar consruction; however, the Bessel, various Gaussian realizations, Transitional, and the Inverse Chebishev Elliptic are, in general, unsymmetrical; thus they are somewhat more difficult to build.

Figures 2A and 2B are schematic diagrams highlighting the series 'C' capacitors of the devices described comprising the centrally located coaxial capacitors, the $C_{1+2}\cdots C_{n-2}$. These C_{odd} capacitors may be broken up into an array of two capacitors each in series to provide for the filter-internal 'C' series, the schematics for which are as shown in Figures 2B and 3B. This construction technique provides for accessible attachment of shunt elements 'L' or 'L-C'. Of course, these elements may be stepped as to diameter (see Fig. 4A and B) and plugged into each other, resulting in a lesser number of pieces in the construction, but somewhat more complicated in terms of component tolerance realization and assembly; in which case, the capacitors C_s are not present.

In general, n-odd equally terminated filters ($R_s=R_L=Z_o$ maximum power transfer terminations) have been assumed, i.e., n-odd: 3, 5, 7...n-odd.

The shunt elements connect at convenient accessible locations as shown in the various pictorial cutaway figures: 4, 5 and 6.

1/ "Design of Combline and Interdigitated Bandpass Filters"

MICROWARE

An Interactive Microwave Filter Design Program

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Microware is a microwave filter design program that enables the user to design filters in a logical, step by step manner. A brief outline, including a flow chart will be given followed by three examples.

Three common filter designs are now supported by the program. They are:

1. **Lumped Component Designs.** A majority of filter design in the frequency range below 1 GHz is of the lumped component type. Virtually any type of circuit configuration may be realized. The sub-program "LUMP" designs some of the more basic circuits. The types supported by this program are:

Tank, Mesch, Lowpass/Bandpass, 4 types of elliptical filters. Impedance and Nortons transforms can be applied to the prototype circuit. Filters can be designed by component value allowing "off the shelf" components to make up a large part of the circuit.

2. **Waveguide Filters.** An accurate design sub-program is included. "IPWG" is based on realizing a lumped circuit with waveguide elements. Currently the program only supports TE01 mode designs. With this, inductive coupled elements in the form of an iris or post may be used.

3. **Cavity Filters.** The third sub-program "INTCL" can design interdigital and combline filters. The user has a variety of options as to the size and electrical configuration. Both round rod and rectangular resonator designs are available. The user also has the option of tapped loading, short or open circuit transmission lines to transform in and out of the filter.

- MainMenu -
The Cornerstone of Microware

While there seems to be an abundance of analysis and optimization programs on the market, the first step, Synthesis is often neglected. In addition to this, many segments of our industry require specilized programs that may not be marketable. A few programs that do have synthesis capabilities are:

Compac - Has a built in synthesis package that lets the user design coupled lines, impedance matching transformers and filters. Available separately is a filter design kit, complex matching and PLL design.

These Figures 4, 5 and 6 all include schematic of (actual) the complete high pass filter (type of shunt element(s) optional for Chebishev all-pole or Pseudo-Elliptic high pass filter); note capacitors C_s, 1-3, C_s, 3-5, etc. (See Note, Figure 5.)

Note: In suspended substrate (SSS) or strip/microstrip designs the dual of the networks shown may conveniently be used.

Patent protection has been applied for on these device designs.

The determination of element values follows standard design procedure which is described in the references. See example pages 8, 9 and 10.

REFERENCES FOR FURTHER READING

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Ref. 2: Frederick E. Terman, "Radio Engineers Handbook", McGraw Hill Book Co., Inc., New York. 1943; First Edition

Ref. 3: Anatol Zverev, "Handbook of Filter Synthesis", John Wiley & Sons, New York, Library of Congress Card No. 67-17352

Ref. 4: D.J. McLean, "COCC1 Insertion Loss Design of Electric Filters", Technical Report No. 2, 1956, Stanford Electrical Laboratories, Stanford University. Prepared under ONR Contract No. 225(4), NR 373 360

Ref. 5: L. Young, G.L. Matthaei, E.M.T. Jones, "Microwave Filters, Impedance-Matching Networks and Coupling Structures", McGraw Hill Book Co., Library of Congress Catalog No. 64-7937

Fig. 6: R. Levy, Generalized rational function approximation in finite intervals using Zolatarev functions, IEEE Trans. Microwave Theory Tech Vol. MTT-18, Dec. 1970 pp. 1052-1064

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EESof - Has a series of filter design programs by Wenzel/Erlinger Associates. PLL and complex match synthesis programs are also available.

Filsyn - Has the most comprehensive lumped element designs available. The user has the option of specifying all design parameters, including the location of the poles and zeros.

Other programs with design capabilities are available from DSI Software (microstrip and stripline coupled lines), Etron (various RF design programs) and the E.E Public Domain Library (many design programs in the public domain).

It was found that none of these programs provided all of the capabilities for our day to day needs. With this in mind the concept of an all purpose microwave filter design program was conceived. One of the foremost requirements was to provide an interactive environment so that the designs could be modified via software. This program consists of three different areas:

1. User inputs design criteria.
2. Edit Specs.
3. Electrical design

As the user procedes through the program they are guided with the "Windows" and pull down "Menus" familiar to user of the Macintosh. If, at any time the user exceeds the limits of the program's design capability the user is warned with a prompt. Next the specs that have been entered are presented on the screen. The user has the opportunity to change or delete them at this time. When satisfied the design specifications are written to a file named "INSPECS". At any time during the design procedure this can be recalled and changed. Now the program enters the electrical design stage. The normalized element values are calculated and then impedance and frequency scaled. The program now links with the desired sub-program. The Macintosh provides the most "User-Friendly" environment both for programming and design. While the terms "Windows", "menus" and "event-managers" might not be familiar to many electrical engineers, they are an integral part in the world of computer programming. When this program was first written, Microsoft Basic was one of the few languages available. Since beginning, the availability of C language compilers has provided a more flexible environment. A great part of the math routines have been converted to "C".

While the user proceeds through the program, menus document the

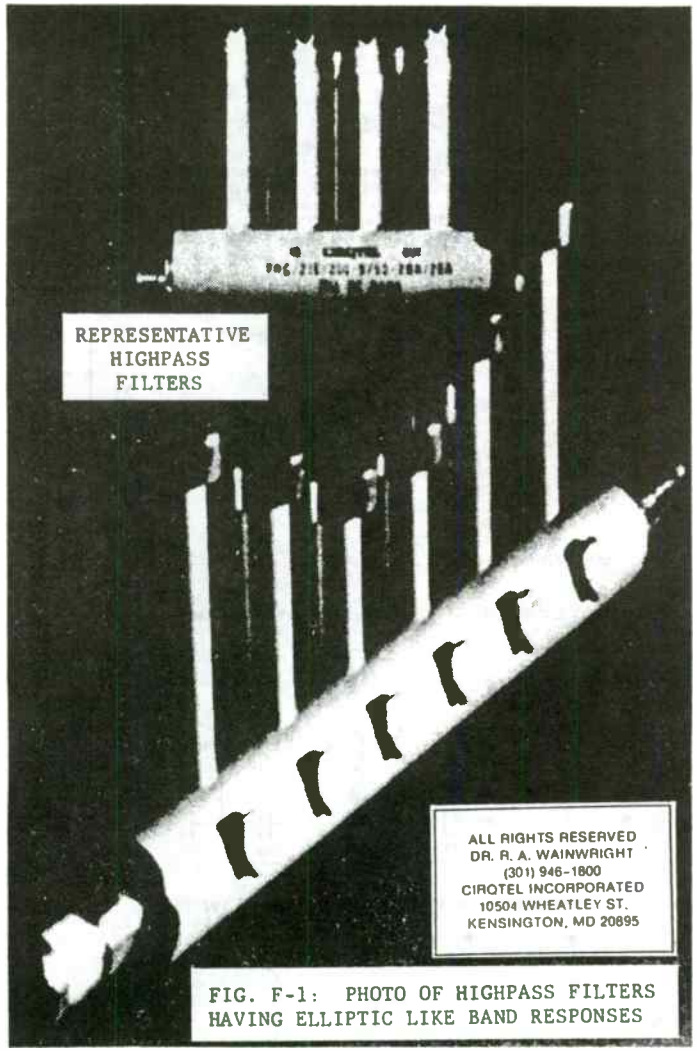


FIG. F-1: PHOTO OF HIGHPASS FILTERS HAVING ELLIPTIC LIKE BAND RESPONSES

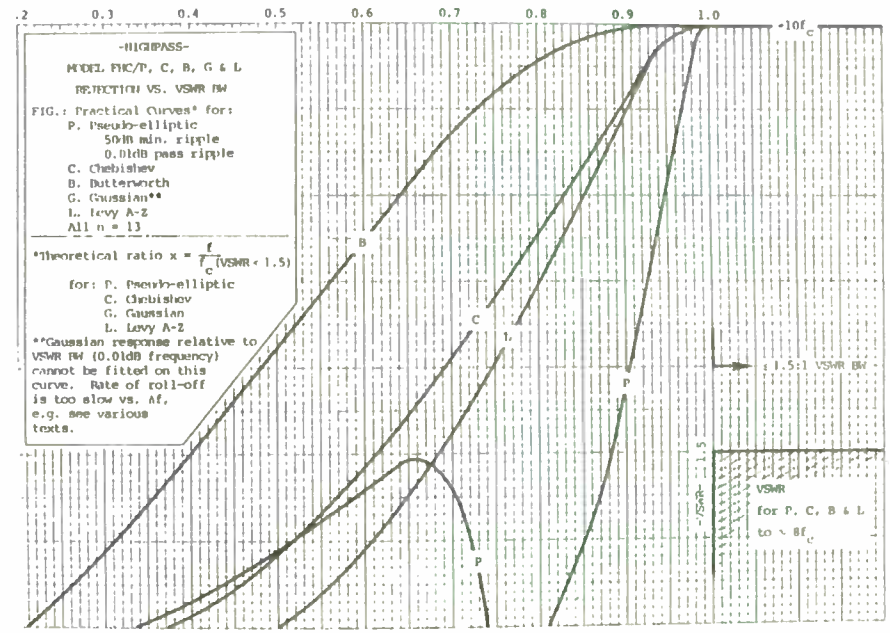


FIG. F-2: PRACTICAL CURVES FOR REPRESENTATIVE HIGHPASS FILTERS

progress and the user can "pull" down a menu at any time and modify that particular specification. Much of the program can be executed with use of the "mouse", a graphic pointing device used in this program.

The Design Examples.

Three design examples will be given, all originating from the same main program. The user is offered a variety of design considerations and the program flows in a logical, straight-forward way. The three design examples given here are actual working designs now in production at Microlab/FXR. The management of Microlab/FXR is to be thanked for providing the design information for publication.

Example 1. Lumped Component Design.

This example is for a "Reflectionless" bandpass filter. Reflectionless in that the unit maintains a good VSWR over a much wider range then the bandpass filter. Required also was a flat group delay over the 3 dB bandwidth of the filter necessitating a Bessel Response. The design specifications are as follows:

Center Frequency: 300 MHz.

Bandwidth (3 dB): F_0 +/- 15 MHz. min. +/-18 MHz. max.

VSWR: ≤1.1:1 at F_0
≤1.3:1 from 250 - 350 MHz.

Group Delay: 20 +/- 2 nS. relative to a thru line
≤1.5 nS over 3 dB bandwidth

Insertion Loss: ≤1.0 dB at F_0

Stopband: ≥20 dB relative from D.C. -250 MHz. and 350 - 1000 MHz.

Figure II shows a functional diagram of the required circuit.

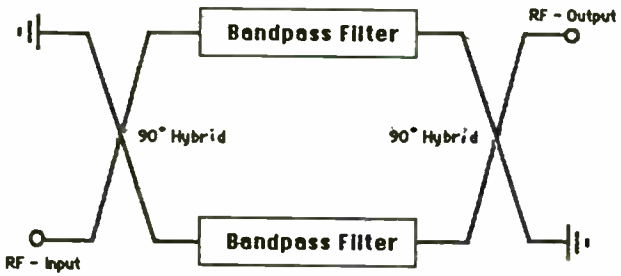


Figure II

To obtain a good VSWR over a bandwidth much wider then the passband of the filter a combination of two 3 dB hybrid couplers are used. The filters are separated by a line length via the coupled line of 90 degrees at center frequency (300 MHz.). When the filters are phase matched over their 3 dB bandwidth, reflection from either filter is absorbed by 50 ohm termination incorporated on either side of the coupler. Thus the input VSWR is determined by the accuracy that the two filters can be phase matched. This

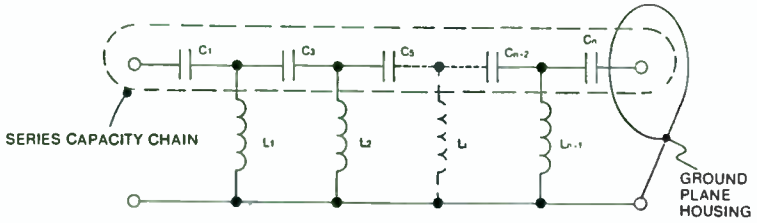


FIG. 2A1 TYPICAL SCHEMATIC, n odd, ALL-POLE HIGH PASS FILTER

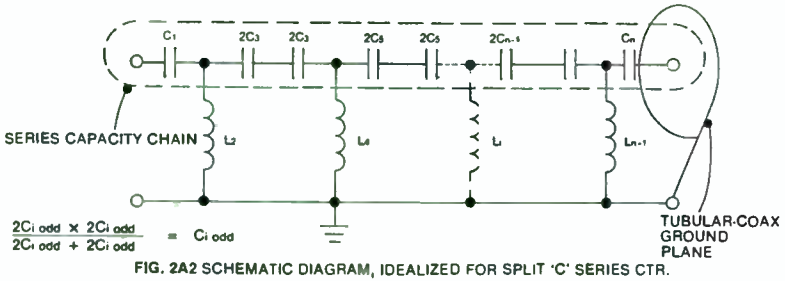


FIG. 2A2 SCHEMATIC DIAGRAM, IDEALIZED FOR SPLIT 'C' SERIES CTR.

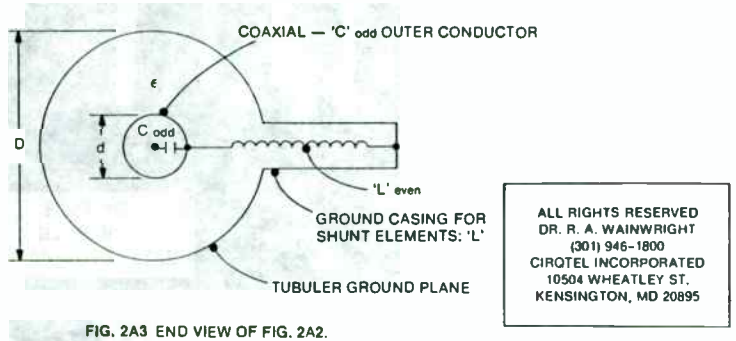


FIG. 2A3 END VIEW OF FIG. 2A2.

NOTE: THE TUBULAR GROUND-PLANE ENCASING THE SERIES CAPACITY CHAIN C_1, C_3, C_5 . . . C odd IDEALLY PROVIDES FOR A $Z_o = R_g = R_L$ CONFIGURATION (CO-AXIAL) TO PROVIDE FOR A WIDE-BAND MATCH TO FREQUENCIES (f > 2 fc to f mode) WELL ABOVE THE CUTOFF FREQUENCY. f mode is that frequency above which a tube of diameter D no longer supports a TEM wave.

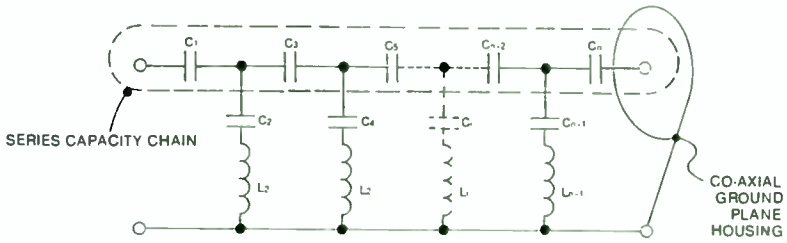


FIG. 2B1 TYPICAL SCHEMATIC, n odd, ELLIPTIC-LIKE LOW PASS FILTER

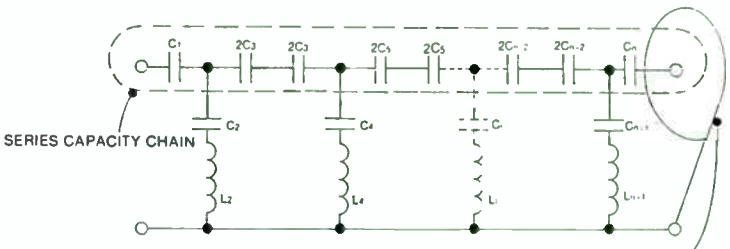


FIG. 2B2 IDEALIZED SCHEMATIC DIAGRAM OF ELLIPTIC-LIKE HIGHPASS FILTER. SHOWING SPLIT CENTRAL 'C' SERIES.

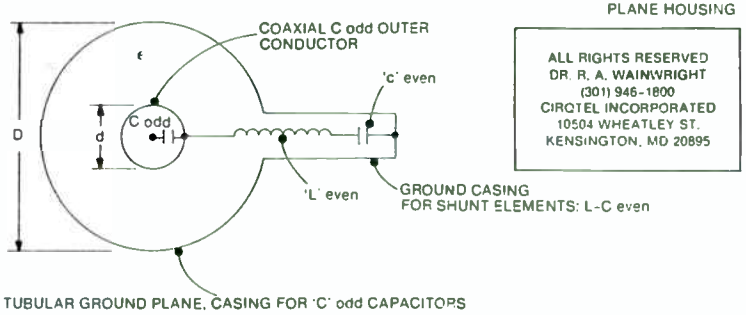


FIG. 2B3: END VIEW OF FIG. 2B2

NOTE: THE TUBULAR GROUND-PLANE ENCASING THE SERIES CAPACITY CHAIN C_1, C_3, C_5 . . . C odd IDEALLY PROVIDES FOR A $Z_o = R_g = R_L$ CONFIGURATION (CO-AXIAL) TO PROVIDE FOR A WIDE-BAND MATCH TO FREQUENCIES (f > 2 fc to f mode) WELL ABOVE THE CUTOFF FREQUENCY. f mode is that frequency above which a tube of diameter D no longer supports a TEM wave

technique is also used to phase match filters when only a scalar network analyzer is available. When first constructed two prototype filters and hybrid couplers were built. Then the filters were aligned and adjusted for best group delay response. With the appropiate connectors the two filters and couplers were put together. At this time it was necessary to match the filters to get the required VSWR response. The combination of VSWR and tight group delay variation requirements made this a difficult and time consuming procedure. An electrical schematic is shown below.

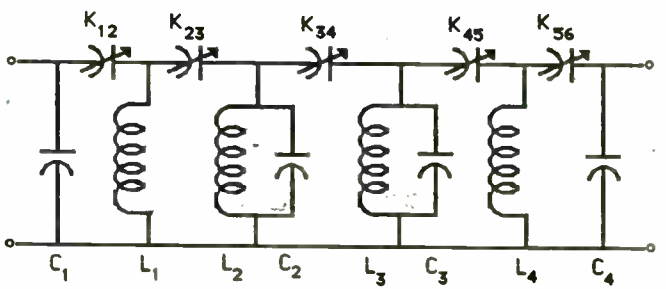


FIGURE III

Design Impedance: 50 Ω Transform to: 1329.91 Ω

Shunt Capacitor C_1= 51.57344 pF.
Series Capacitor C_2= 12.40538 pF.
Shunt Inductor L_1= 2.796390E-02 µH.

Coupling Capacitor K_{12}= .630816 pF.

Inductor L_2= 2.86628 µH. Capacitor C_3= 10 pF.

Coupling Capacitor K_{23}= 1.12957 pF.

Inductor L_3= 2.86628 µH. Capacitor C_4= 10 pF.

Coupling Capacitor K_{34}= 2.58944 pF.

Shunt Inductor L_4= 2.796390E-02 µH.
Series Capacitor C_5= 15.62833 pF.
Shunt Capacitor C_1= 27.76726 pF.

Transform to: 122.12335 Ω to 50 Ω

The responses of a typical production unit are shown in figure V.

Example 2. Interdigital Filter

This example shows the extreme bandwidths that can be achieved by this program. An equi-ripple bandwidth of 66% has been achieved in this design (program maximum is ~70%). In addition to the wide bandwidth, the VSWR and insertion loss specifications add to the difficulty of this requirement. The design specifications are as follows:

Passband Frequency: 8.0 - 16.0 GHz.

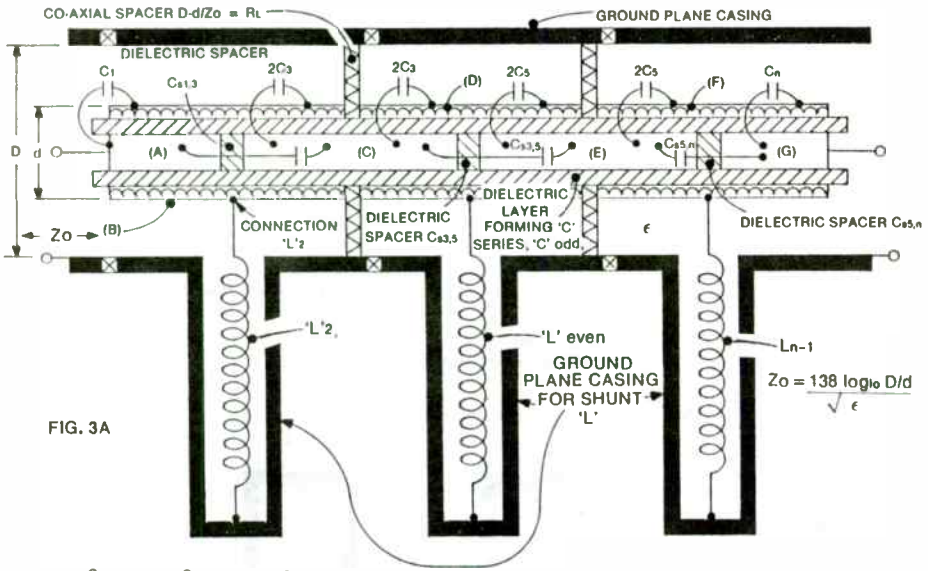


FIG. 3A

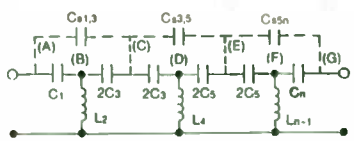
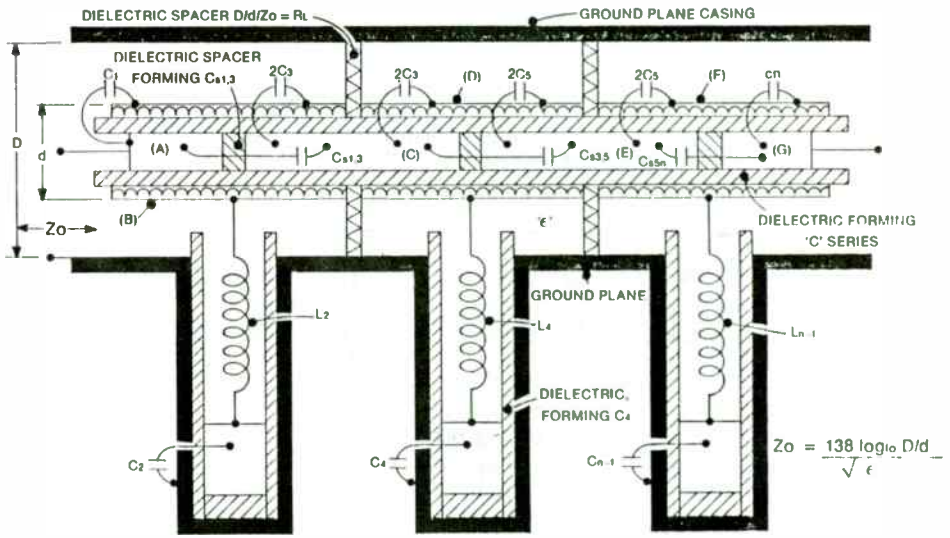


FIG. 3B, n = 7, ALL POLE, COAXIAL HIGH PASS FILTER — ACTUAL SCHEMATIC DIAGRAM.

FIGURE 3 A, B: PICTORIAL CUTAWAY VIEW SHOWING RELATIONSHIP OF ALL PARTS & SCHEMATIC DIAGRAM.

ALL POLE — (CONSTANT 'K' CONFIGURATION) REFERENCE FIGS. 2A2 AND 2A3



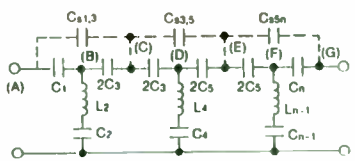


FIG. 4B: 7 POLE, 3 ZERO, COAXIAL HIGHPASS FILTER, SCHEMATIC

FIGURE 4 A, B: PICTORIAL CUTAWAY VIEW SHOWING RELATIONSHIP OF ALL PARTS AND SCHEMATIC DIAGRAM REF FIGS. 2B1 AND 2B2

(PATENT APPLIED FOR)

VSWR: ≤1.5:1 over passband

Insertion Loss: ≤0.6 dB. over passband

Stopband: ≥25 dB @ 6.4 GHz. and 20 GHz.

Power: 100 Watts Avg. 3 KW peak 1% Duty Cycle

This requirement for a wideband interdigital filter approaches the limits of both the electrical and physical designs currently available. The basis for interdigital filter design is widely documented (See Ref. 1-6). This program offers the user the option of designing with rectangular and round rods, rectangular giving the most efficient coupling for a given spacing and the round rod approach being less expensive to manufacture. A schematic is shown below:

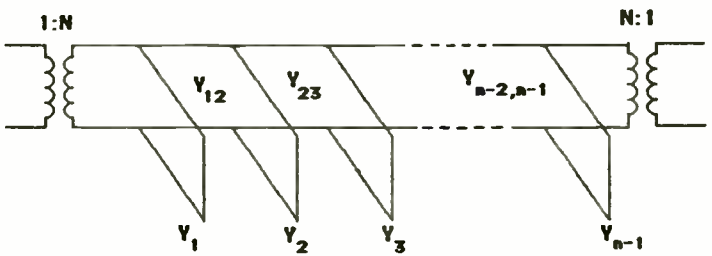


FIGURE IV

The filter was designed following the program prompts (see menus at the end of the article). The wideband design with rectangular bar resonators was used. To make the spacings between the bars practical, a high internal impedance and a large ratio of ground plane spacing to bar thickness was used. The printout containing the mechanical dimensions is shown below.

INTERDIGITAL / COMBLINE DESIGN

Bar Thickness: 0.02 ins. Ground Plane Spacing: 0.300 ins.
Design Impedance: 50 Ω Internal Impedance: 175 Ω
Bar Length(1,N): 0.225 ins. Bar Length (2,N-1): .200 ins.
Cavity Width: 0.2459 Ins.

k	C_k / e	Width (ins.)	$C_{k,k+1}$ / e	Spacing (ins.)
Bar (1)	3.2772	.1398		
Spacing (1,2)			2.0716	.0220
Bar (2)	.8419	.0343		
Spacing (2,3)			1.0040	.0532
Bar (3)	1.4699	.0556		
Spacing (3,4)			.9137	.0605
Bar (4)	1.5228	.0557		
Spacing (4,5)			.8839	.0634
Bar (5)	1.5413	.0557		
Spacing (5,6)			.8735	.0644
Bar (6)	1.5462	.0557		
Spacing (6,7)			.8735	.0644
Bar (7)	1.5413	.0557		
Spacing (7,8)			.8839	.0634
Bar (8)	1.5228	.0557		
Spacing (8,9)			.9137	.0605

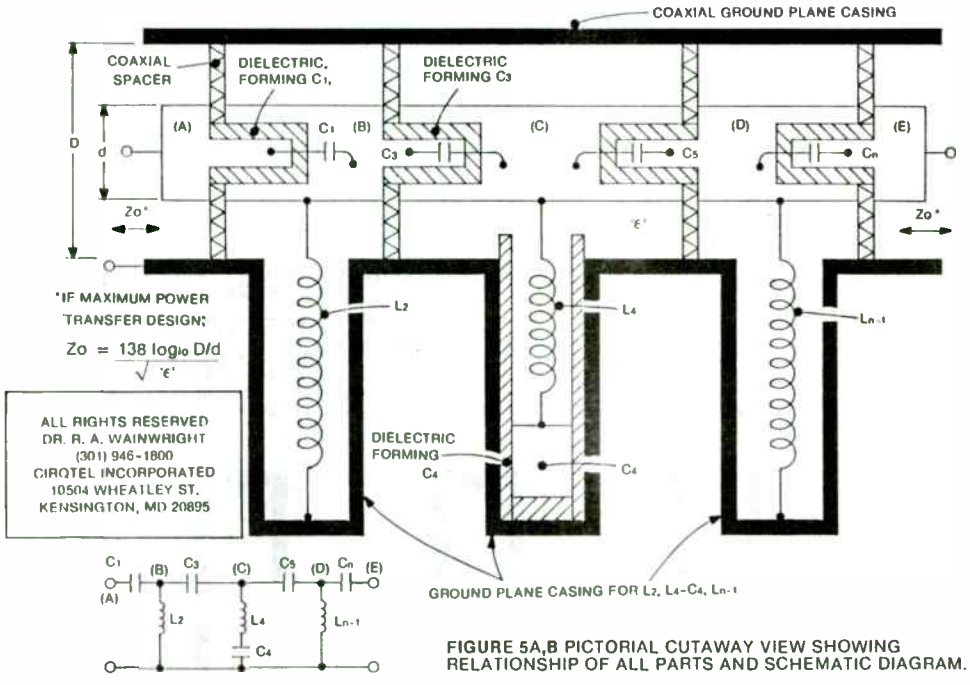


FIG. 5B, n = 7, 7 pole-1 ZERO COAXIAL HIGH PASS FILTER SCHEMATIC

FIGURE 5A,B PICTORIAL CUTAWAY VIEW SHOWING RELATIONSHIP OF ALL PARTS AND SCHEMATIC DIAGRAM.

(PATENT APPLIED FOR)

EXAMPLE:

DESIGN A HIGH PASS FILTER TO THE FOLLOWING SPECIFICATIONS

1. PASSBAND: 0.9 ≥ 4 GHz; LOSS ≤ 0.5 dB
2. Zo = 50 ohms, passband VSWR ≤ 1.5-1
3. REJECT ≤ 500 MHz: ≥ 35 dB
4. CONNECTORS: N(F) IN; N(M) OUT

FROM REFERENCES, ALLOWING DESIGN MARGIN, SET fc AT 800 MHz THEN:

$$\frac{fc}{fr\ (>35dB)} \sim \frac{800}{500} = 1.6, \text{ Indicating } n = 8,$$

USE n = 9 FOR SYMMETRICAL DESIGN (n-odd)

THEN COMPUTE ELEMENTS: (0.01 dB ripple)

C1 = 4.885 pf L2 = 6.97 n H
C3 = 2.205 pf L4 = 5.808 n H
C5 = 2.088 pf

SEE SCHEMATIC BELOW (FIG. E-1)

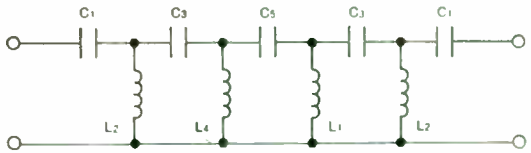
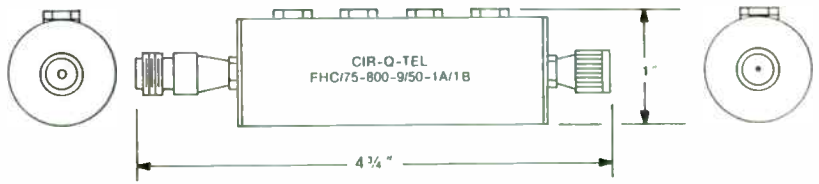


FIG. E-1; SCHEMATIC

RESULTING IN:



WEIGHT: < 5 OZ. FIG. E-2 OUTLINE DRAWING HIGHPASS FILTER

THE RESPONSE CURVES: AMPLITUDE AND RETURN LOSS FROM 10 MHz - 10 GHz IS GIVEN IN FIG. E-2 A AND B
LOSS: < 0.5dB FROM 0.850-4.7 GHz
VSWR: < 1.5:1 FROM 0.810-4.6 GHz
REJECTION: > 35dB at ≤ 535 MHz

Bar (9)	1.4699	.0556		
Spacing (9,10)			1.0040	.0532
Bar (10)	.8419	.0343		
Spacing (10,11)			2.0716	.0220
Bar (11)	3.2772	.1398		

The electrical response for a typical production unit is shown in figure VI

Example 3. Waveguide Filter

This example shows the accuracy which a waveguide filter with difficult stopband requirements can be realized. Adding to the difficulty of this design are the insertion loss and VSWR requirements.

Center Frequency: 15.1 GHz.

Bandwidth: .25 GHz.

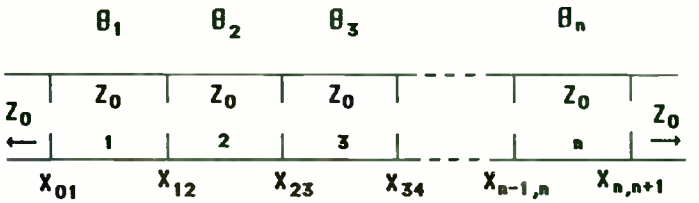
Insertion Loss: ≤0.3 dB over Passband

VSWR: ≤1.3:1 over passband

Stopband: ≥60 dB. @ 14.6 GHz. and 15.7 GHz.

This third requirement is for a low loss waveguide filter uses equations available from ref. 1-3. The user may choose to design with an inductive post or iris. The program includes corrections for the finite thickness of the post or irises. If the calculated reactance causes the thickness of the end posts to be less then 0.050 ins. the program will calculate an offset post.

The electrical circuit is shown below:



The user follows the program prompts and the print out of the mechanical dimensions are as follows.

Inductive Post Wavguide Design

Post Diameters

Post (1)= 0.100 ins.	Offset from C/L= .047
Post (2)=0.16295 ins.	
Post (3)=0.16746 ins.	
Post (4)=0.17001 ins.	
Post (5)=0.17001 ins.	
Post (6)=0.16746 ins.	
Post (7)=0.16295 ins.	
Post (8)=0.100 ins.	Offset from C/L=.047

Post Spacings

Spacing (1,2)= 0.60709 ins.
Spacing (2,3)=0.67603 ins.
Spacing (3,4)=0.68136 ins.
Spacing (4,5)=0.68136 ins.
Spacing (5,6)=0.67603 ins.

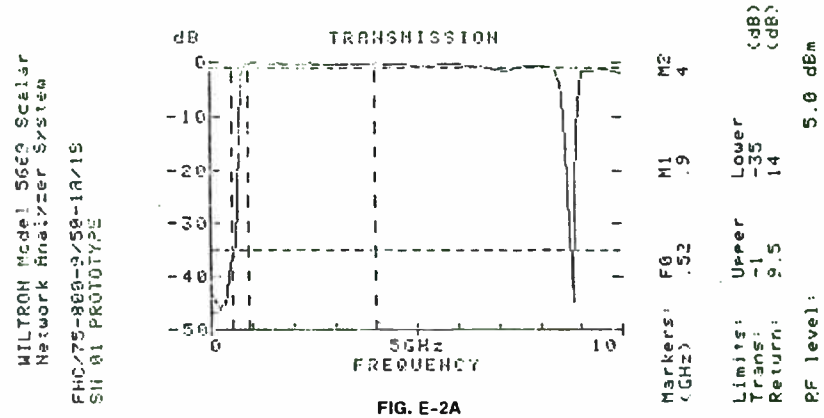
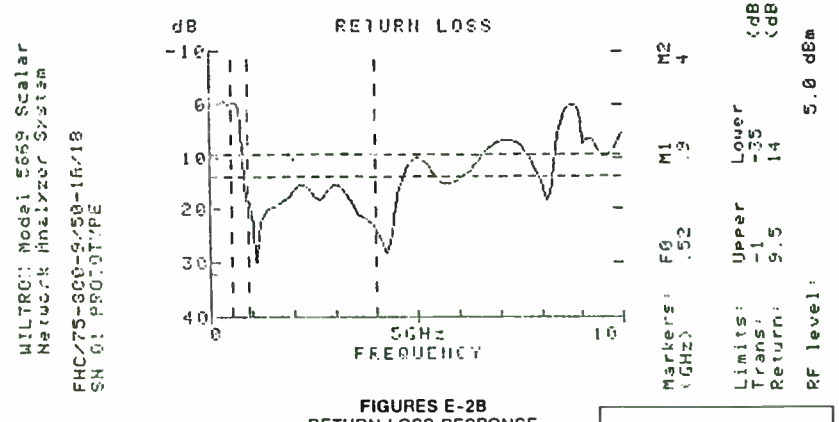


FIG. E-2A
AMPLITUDE RESPONSE OF EXAMPLE DESIGN FIG. E-1 (MEASURED)



FIGURES E-2B
RETURN LOSS RESPONSE (MEASURED)

Spacing (6,7)=0.60709 ins.

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3. A Study of the Phase and Filter Properties of Arrays of Parallel Conductors Between Ground Planes
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2. Reference Data for Radio Engineers
ITT

3. Filtering in the Time and Frequence Domains
Blinchikoff and Zverev
Wiley-InterScience

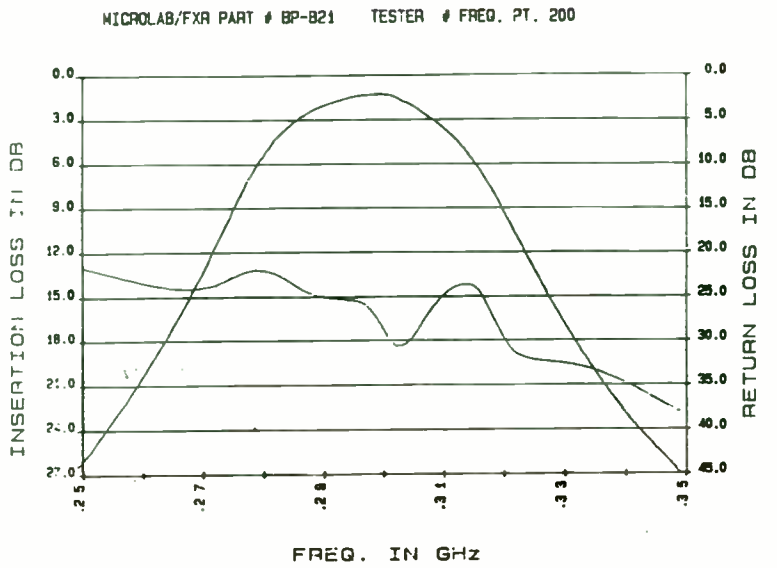


FIGURE V

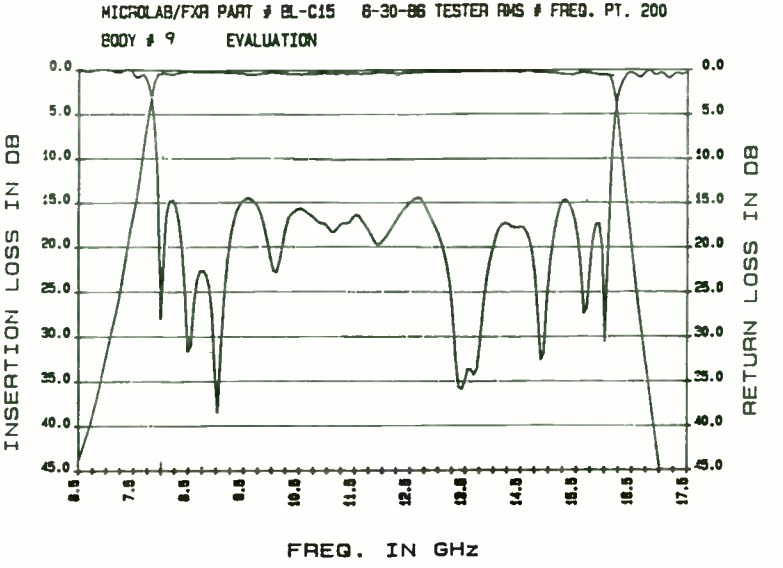
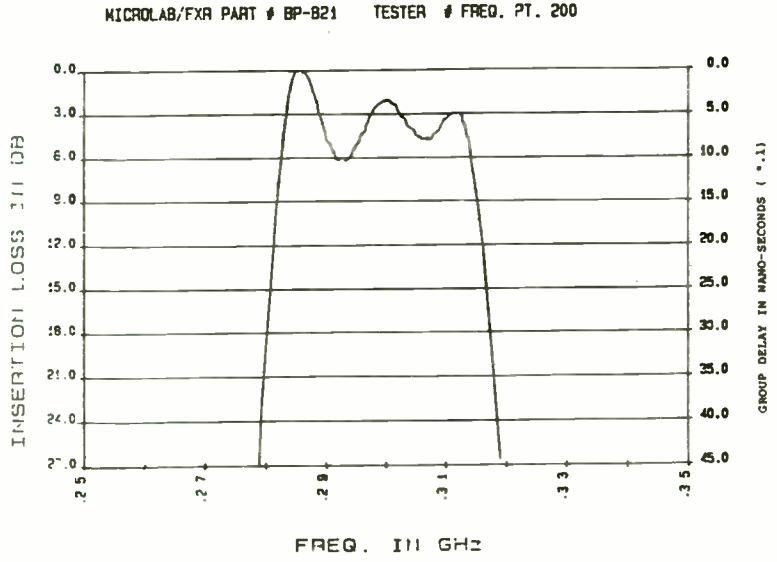
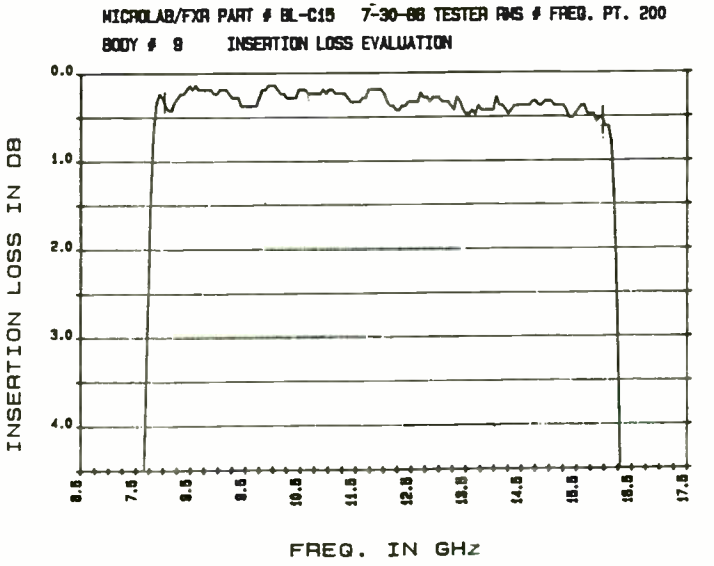


FIGURE VI





HIGH POWER FILTERS

Specsmanship & Design Considerations

By Dick Wainwright, Chief Scientist
Cir-Q-Tel, Inc.

Abstract:

Blivetry*: power; feasibility; Q: selectivity; gradients; hot spots; energy storage; contaminants; ionization; breakdown; peak-average; C.W.; A.M.; % modulation; F.M.; etc.; volt-amps; connectors; size; weight; heat generation, flow & sinking; ionization; impacting; altitude; humidity; salt spray; insulation; shock; vibration; harmonic content; rejection; source & load; EMI; form factor; skin depth-plating; dissipation factor; dielectric strength; topology; susceptibility; losses; volts; amps; volt-amps; Q; MTBF; manufacturers ratings & reality; heat; heat flow; - - all are but a smattering of the flow of words/thoughts that haunt every sensible designer of high power devices. (Notice: certain key words were repeated to emphasize their importance.)

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*Blivetry: The art of defying the basic laws of physics by forcing two or more objects to fit into the same space - analogous to fitting ten pounds of parts into a one pound container.

Customers, bless them, generally think of filters as bandaids - one often hears the uninformed say, "Anyone can design filters - the textbooks are full of tables of element values". That is true, but volts and amps and concomitant happenings make a difference. "The ratings", not the values, are of fundamental importance in power handling devices, design and application. A little experience usually results in a lot of smoke testing.

An intimate knowledge and an awareness bordering on paranoia, plus considerable experience are fundamental requisites.

The writer has on innumerable occasions lost the "first go-around" on a project bid on the basis of: price, size, weight and exceptions prudently taken, in some instances, because the user did not know or furnish such very important information as:

a. Harmonic content of transmitter power output relative to fundamental power
b. Possible incompatibility of specified connectors with specified power and load conditions
c. The amount of surface area available for heat conduction/radiation and/or availability of cooling air. Assuming that cooling air is available, the rate of air flow, pressure, as well as the temperature of the cooling air, must be known.

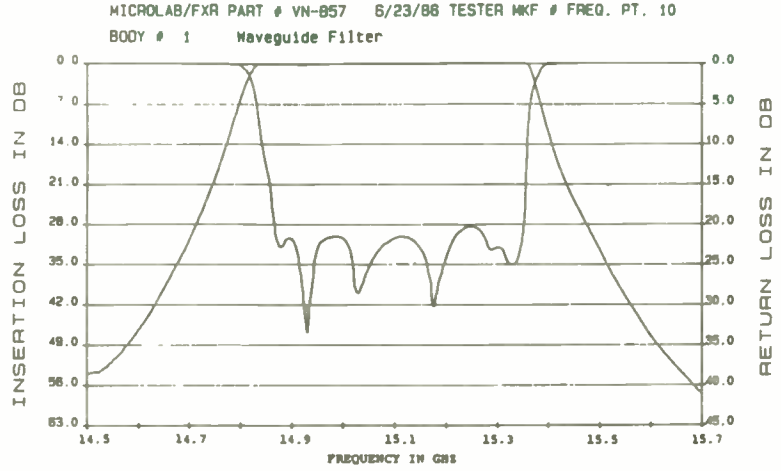

FIGURE VII

d. Heavy shock and vibration specifications were specified along all three major axes when in fact the application, under power, was indoors and fixed.

e. Specifications indicating unrealistically low values of device VSWR (e.g. 1.1:1) when in fact the filter would in practice be operating continuously into loads of never less than 2:1 and often in excess of 3:1 VSWR. (In some cases an infinite VSWR of any phase) Specified selectivity, i.e., ratio of "f" low-reject/"f" high pass ($f_{p(high)}$ was given as very nearly 1:1; and it is not unusual to find specifications indicating selectivity ratio values of 1.01:1, 1.02:1, etc. When using a number of filters to cover a broad range of frequencies it is usually best to uniformly distribute the power pass band and reject to pass ratios to avoid undue stress on any of the filters: see Example (1).

f. Other mitigating relationships that, taken as whole, result in unrealistic designs.

Taking it from the top, a-f:

a. Harmonic content of transmitter output:

Typical solid state transmitters, of recent vintage, can be expected to yield harmonic power levels of (push-pull final through combiner to 50 ohms unbalanced): Table 1

TABLE 1

Harmonic Order		Level dBc	Harmonic watts/KW (fundamental)
2nd	:	-18	15.8
3rd	:	-12	63.1
4th	:	-21	7.9
5th	:	-18	15.8
6th	:	-22	6.3
7th	:	-21	7.9
8 - 13	: Avg.	-22	37.8) Avg.: 6.3W/harmonic

Total Harmonic Power: 154.6 watts/KW fundamental power

As an aside, note at this juncture that the customer may wish to use a ferrite isolator at the transmitter output to obtain a well-matched transmitter output, but, through oversight, may neglect the fact that most isolators are frequency sensitive, resulting (possibly) in excessive heating by harmonics, resulting in isolator burn-out and/or additional harmonic generation caused by the ferrite being operated near the Curie temperature of the materials, etc.

(b) Connectors power rating insufficient for application. Most connector manufacturers haven't the foggiest idea of how much power/apparent power their connectors will safely handle. Current ratings, not voltage ratings, are generally the problem drivers. Z_o is of little consequence in systems working with very high VSWR values - of course they are directly related.

Given the fact that most filters are "reflective devices" i.e. produce attenuation by reflection of power rather than being absorptive, absorptive filters are generally much more expensive and generally considerably larger than reflective devices. However, in many UHF and above, frequency range applications the use of harmonic absorptive filters may make a lot of sense.

(c) How much surface area should one allow for the cooling of high power filters, and, if cooling air is available, what is its pressure and rate of flow?

First one may make the assumptions:

1. The maximum power vs. connector type is in the order of 2/3 of the cable attached, derated appropriately.
2. Normally a high power filter ("hot" surface temperature) is designed such that the hot surface temperature of the filter does not exceed ambient C° + 50°C with a heat sinking plate average temperature of no more than ambient air C° + 10°C= +95°C max. Cooling air, if available, should not exceed an effective temperature of +80°C; hence, air speed may be an important consideration as the air approaches the filter hot spots.

In many cases substantial size fins may be required but fins are not very effective in cramped air flow spaces - convection air currents must be free to circulate if convection cooling represents a substantial portion of the cooling means, and surrounding heat conducting surfaces may need to have rough surface to "wipe" the heat out of the circulating air.

(d) Heavy shock and vibration specifications along all three major axes, i.e., G forces applied to coaxial filters should be studied carefully and if at all possible, the strong G forces should be confined to the smaller dimensions of the coaxial structure. Minimal forces of no more than 5G, preferably, and no more than 10G max. (11 m/sec. std. shock specifications) on the length should be applied to coaxial high power filters of substantial size, plus consideration as to the adequacy of mounting hardware and supporting structures is essential.

(e) Selectivity, time delay, energy storage & electrical (absorptive) losses/heat generation go hand in hand.

Q: The ratio of:

$$\frac{\text{Energy Stored per Cycle}}{\text{Energy Dissipated per Cycle}}$$ of the applied energy

is a critical consideration in the design of all filters in general, and is of great importance in high power filters. For a given loss, the required ratio of Q unloaded/Q loaded is different for every filter design. It is not uncommon for certain designs to require inductor Q unloaded values in excess of 500-1000 or more and for capacitors 3500-8000 or more to barely eke out a responsive design, where rejection bandwidths to low loss band edge ratios are quite small, say much less than 1.2:1 for 40-60 dB rejection; almost impossible values

A Practical Approach to the Design of Voltage Tunable Lowpass and Bandpass Filters

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Introduction

Many filters are used in RF systems. Most are fixed tuned but occasionally a tunable filter is required. A preselector in a receiver is one example. Tunable filters are also useful as tracking filters in frequency synthesizers, as variable IF filters in block conversion receivers and as variable post detection video filters. Tunable filters can be constructed by mechanically ganging tuning components to a common tuning shaft but this approach is bulky, expensive and not very adaptable to microprocessor control. Voltage tuned filters overcome these difficulties and are suitable in many applications. The control voltage can come from a front panel potentiometer, a microprocessor controlled DAC, or from another voltage controlled stage such as a voltage controlled oscillator allowing both stages to track one another.

This paper explores the design of voltage tuned lowpass and constant percentage bandwidth bandpass filters. Many filters are designed quite easily using tables of normalized component values. A lowpass filter design example is presented to emphasize the relationship between filter component values, impedance, and frequency. This relationship implies careful control of filter impedance is essential if the filter is to be tuned. With this understanding the lowpass filter is transformed into a tunable lowpass filter covering one octave with the help of a pair of impedance control networks.

Next this approach is extended to include constant percentage bandwidth bandpass filters. The paper concludes with a discussion of intermodulation performance, practical frequency and tuning range, and circuit modifications to improve realizability. Filters, tunable over at least one octave, from several hundred kilohertz to several hundred megahertz, can be successfully designed using this approach.

Filter Design Review

Textbook filter design usually involves finding the roots of the filter transfer function as the starting point for a classical circuit synthesis approach. While providing insight to the mathematical origins of the filter this approach has little to recommend it for day to day filter design.

It is simple to design most filters from standard tables. These tables consist of component values for filters normalized to one ohm, one radian per second and are available from several references including Williams and Zverev. Select from the table the component values for a prototype lowpass filter with the appropriate number of poles and of the desired filter family (Butterworth, Tschebyshev, Bessel, etc). Final component values are obtained by frequency and impedance scaling of the prototype values. Figure 1 shows a three pole, 20 MHz Butterworth lowpass filter and the prototype from which it was scaled.

A lowpass filter can be transformed into a highpass, bandpass, or bandstop filter and implemented with lumped LC components, or transmission

of 2000 or more for coil Q and over 10,000-15,000 capacitor Q may be required, but unobtainable because of space, moding and/or frequency limitations.

The Q of coils increases roughly as the square root of frequency, hence generally high frequency filters yield lower losses, given the same selectivity and available space.

For a given loss (see Table 2) the unloaded Q required increases substantially with passband ripple (VSWR), complexity, n and type of filter, (Elliptic, all-pole Chebishev, Butterworth, etc.).

TABLE 2

Selectivity f60dB/f3dB	Nominal VSWR	Filter Design	Representative Qul. for a Given Loss (approx.)	Energy Storage
1.25	1.2	Elliptic (0.01 dB Ripple)	1000	20
1.5	1.35	Chebishev (all-pole) ripple=0.1 dB	650	15
1.7	1.2	Chebishev (all-pole) ripple=0.01 dB	460	12
-	-	Chebishev (all-pole) ripple=0.001 dB	290	-
2.1	1.2	Butterworth	200	10
4.2	-	Bessel		-

Table 2 indicates representative values - not absolutes.

As an example, a 0.01 dB Chebishev (all-pole) filter required approximately $\frac{460}{200}$ -1∿84% more Q than a Butterworth filter for a given loss and the Elliptic filter given has twice the energy storage indicating that voltages and currents are roughly 40% more than in a Butterworth filter.

(f) Other factors of consequence:

(1) Phase linearity vs. f.

(2) Matching of phase: A $\pm$ 5° phase matching specifications may nearly double the price relative to a non-matching phase unit because of the component tolerance problem alignment accuracy and the need to "fix" parts to preclude minute variations in operating environment.

(3) Humidity: High humidity conditions, especially with condensation presents substantial problems.

(4) Altitude: Derating or pressurization with dry nitrogen or sulfur hexafluoride may be forced as a solution. Of course, pressurization eliminates humidity problems.

(5) etc.

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lines as required. Other transformations that rearrange component values to improve realization are also possible.

To transform a lowpass filter into a bandpass filter shunt inductors and series capacitors are added to resonate the shunt and series branches at the desired filter center frequency. The new filter retains the bandwidth and impedance of the original lowpass filter. A 60 MHz bandpass filter transformed from a 20 MHz lowpass filter has a passband extending from 50 to 70 MHz. The center frequency can be shifted by changing the values of the shunt inductors and series capacitor without affecting the filter bandwidth or impedance.

Tunable Lowpass Filter Design

This section of the paper develops an approach to the design of tunable lowpass filters which takes advantage of frequency and impedance scaling. The results will be applied later to the design of voltage tuned bandpass filters. Since frequency and impedance scaling go hand in hand to obtain filter component values careful control of filter impedance is necessary if the filter is tuned. What type of impedance control is required and how can it be incorporated into a practical design?

Let's look at a three pole Butterworth lowpass filter, tunable over an octave from 60 to 120 MHz with a 50 ohm input and output impedance. A 60 MHz filter is designed by frequency and impedance scaling of the Butterworth prototype (Figure 2a). The 120 MHz version of this filter is identical in form but has inductors and capacitors one half as large as its 60 MHz counterpart (Figure 2b).

The filter in Figure 2b can be converted into its 100 ohm equivalent (Figure 2a) by doubling the inductor value and halving the size of the capacitors. Notice the inductor in this filter is the same as the inductor in the 60 MHz 50 ohm filter.

A voltage tuned filter could be built if each of the filter components were replaced with its voltage variable equivalent. While voltage variable capacitors are widely available in the form of varactor diodes, voltage variable inductors are a bit of a problem.

Electrically variable inductors, relying upon the saturation of a ferrite core by a DC control current, are available; however, they are expensive, bulky and consume a large amount of control current. An ideal voltage tuned filter would use only varactor diodes as tuning elements.

The total variation required to tune a filter over an octave is four to one, half of the variation coming from the inductors, the other half from the capacitors. Fixing the inductor value and using varactors to tune the filter means the entire four to one tuning variation must come from the varactors. Something has to give, and as implied earlier that something is the filter impedance. Comparing Figures 2a and 2c shows that a fourfold reduction of the filter capacitors doubles both the filter frequency and impedance. Filter impedance variation as the filter is tuned is the price that must be paid for the convenience of fixed inductors.

Impedance variation of this magnitude is not acceptable in most applications. In addition to the obvious VSWR problem, filter bandwidth and insertion loss are adversely affected by input and output mismatch. Perhaps the unwanted impedance variation can be compensated by a tunable matching network that provides a variable impedance match as the filter is tuned. This compensation network should be as simple as possible and should not require variable inductors. In addition, its tuning varacters

Addenda to: High Power Filters, Specsmanship
and Design Considerations -
by: R.A. Wainwright

Suppose one wishes to provide filters covering the 100-1000 MHz frequency range that will in turn yield greater than 40 dB attenuation at the second and higher order harmonics; let Nf be the number of contiguous band filters.

First, determine the number of octaves included in this band: 100-1000 MHz (an octave is a 2:1 frequency ratio).

Then:

(1) 100-200 MHz - 1st octave

(2) 200-400 MHz - 2nd octave

(3) 400-800 MHz - 3rd octave

(4) 800-1600 MHz - 4th octave (up to 1000 MHz is all the coverage that is required however,

or

On: octave number is an integer: On 2^{Nf}. If one is to evenly distribute the filters such that: Note all logarithms are to base 10.

[1] $Ki = \frac{fc\ (VSWR)\ high}{f\ operate(VSWR)\ low}$ is about the same for all filters, then given: $KNf = \frac{1000}{100} = 10$

then for each filter Ki

[2] $K(Nf)=10 = Ki^{Nf}_{(1)}$ etc.; Nf=4 (filters minimum)

(A)

Then: $\frac{\log 10}{Nf} = \log Ki$

and

Ki=(antilog 10)/4 =1.77827941

(see Fig. E-1)

If 5 filters were to be used, which number will be determined upon evaluation of filters chosen for this task, then, (see Fig. E-2)

if Nf=5

Then

Ki=(antilog 10)/5 =1.584893192

Assuming 4 or 5 filters, then develop Table 1

Table 1

VSWR Passband of Filters 1-4 or 1-5

Ki		1	2	3	4	5
1.78	Nf=4	100-178	178-316	316-562	562-1000	-
1.56	Nf=5	100-158	158-250	250-395	395-628	628-1000

From Fig. E-4 for N(f)=4 or 5 given Ki=1.78 and Ki=1.58 respectively, assuming an elliptic-like response device is compatible with other electrical parameters, ratings, etc.; Then:

The ratio of the lowest 2nd harmonic frequency (2fL) to highest passband (VSWR) frequency (fcH) for Nf=4 and 5 are

(B)

should track those of the filter to which it is connected.

An L-Match is a simple two element impedance transformation network used for single frequency resistive impedance matching. Figure 3a shows an L-Match network, transforming 50 ohms to 75 ohms at a frequency of 60 MHz, and the relevant design equations. Can this network provide twice the impedance transformation (50 ohms to 150 ohms) at twice the design frequency without changing the inductor?

Repeating the L-Match design for a frequency of 120 MHz and an impedance transformation of 50 to 150 ohms gives the network shown in Figure 3b. The shunt capacitor is one half of its 60 MHz value and the inductor is unchanged.

By simultaneously tuning the shunt capacitor, the L-Match can properly terminate a 60 to 120 MHz tunable lowpass filter providing the filter is redesigned to present an impedance of 75 ohms at 60 MHz.

The initial impedance step-up required at the minimum filter frequency is a function of the filter tuning range and is found by simultaneous solution of the L-Match design equations to provide the proper impedance transformation at both ends of the filter tuning range. This solution is expressed by the equation listed below where R is the filter tuning ratio, and N is the initial impedance transformation at the low frequency end of the filter tuning range. N is equal to 1.5 for a one octave tunable filter and decreases to 1.25 for a two octave filter.

$$N = \frac{R^2 - 1}{R(R - 1)} \qquad R = \frac{\text{filter upper frequency}}{\text{filter lower frequency}}$$

Octave tuning requires a four to one capacitance ratio in the filter section as opposed to the two to one ratio needed in the matching network. Ideally both ratios should be the same to allow the use of a common tuning varactor.

The matching and filter section varactors can be combined into a single varactor if part of the varactor capacitance variation is absorbed or swamped with a fixed padding capacitor. For an octave tuned filter the padding capacitor makes up one third of the low frequency matching capacity with the other two thirds coming from the varactor.

Combining the matching network shown in Figure 3 with the filter from Figure 2a and 2c gives the tunable filters in Figure 4. The tuning capacitance varies fourfold from 69 pf at 60 MHz to 17.3 pf at 120 MHz. At 60 MHz 16.7 pf of the tuning capacitance tunes the matching network, while the remaining 52 pf is part of the filter network.

Blocking capacitors can be added to isolate the varactor control voltage which is supplied through a decoupling resistor or RF choke. The actual padding capacitor will be smaller than calculated when the stray capacitance at that node is considered.

Tunable Bandpass Filters

A voltage controlled bandpass filter can be designed by lowpass to bandpass transformation of a voltage controlled lowpass prototype. Unfortunately the lowpass to bandpass transformation which works well for wideband (BW > 10%) filters gives unrealizable component values if a narrowband filter design is attempted. Many advantages of a tunable bandpass filter are lost if the filter bandwidth is too large.

An alternative narrowband approach exists which gives more reasonable component values. It relies upon capacitive, inductive, or magnetic, coupling of parallel resonators and is suitable for filter bandwidths of 20

as given in Table 2

Table 2

	Filter 1 (2fL/fcH)	Filter 2 (2fL/fcH)	Filter 3 (2fL/fcH)	Filter 4 (2fL/fcH)	Filter 5 (2fL/fcH)
Nf=4	200/178= 1.123	1.123	1.123	1.123	1.123
Nf+5	200/158= 1.26	1.26	1.26	1.26	1.26

From Fig. E-2, [(2fL/fcH) -1]=0.123 absissa (frequency scale) and: rejection + return loss= 60 dB ordinate. If return loss is selected as 20 dB VSWR approx. 1.25:1) then 40 dB rejection + 20 dB return loss = 60 dB at 0.123 and 0.26 respectively (absissa value on Fig. E-4).

For Nf=4: at 0.123 (abissa) and 60 dB: rejection + return loss (ordinate) one finds n=11 (elliptic) filter. (see mark "∘")

For Nf=5: at 0.26 (absissa) and 60 dB on ordinate. (see mark "x"), n=9 (elliptic) filters, (Fig. E-2).

If on the other hand one wishes to use an all-pole 0.01 dB ripple Chebishev, (of practical construction) ladder network series coil, and shunt capacitors, with no finite frequency traps

Then: for n=19 the ratio: fcH/2fL=1.36 for 40dBc attenuation, (note: Chebishev filters having more than 19 elements, n ≠ 19

are not generally considered practical) it becomes apparent that additional 10-1000 MHz band segmentation may be necessary, (see Fig. E-3 and Table 3.

If: fcH/2fL = 1.36 then solving for Nf (minimum), fL(1)=100 MHz, then 1.36 fcH =2fL =200 MHz

Then fcH(1)=200/1.36=147 MHz

Proof: $1.47^6 = 10 = 10.09029837$

Please be aware that the Tables and graphs given herein Do Not List Theoretical Values.

Figures E-1, E-2 etc. are self explanatory. For all-pole (equi-ripple passband and monotonic reject band) Chebishev filters the reject band attenuation (dB) given by

[Eqn. 5]

$$dB\ @fx = 10 \log\left\{\left[1 + \log^{-1}\frac{\alpha r(dB)}{10}\right]\cosh^2\left[n \cosh^{-1}\left(\frac{fx}{fcH}\right)\right]\right\} fx > fcH$$

where: [fx(dB] is the frequency of x(dB) of rejection α r is the specified pass band ripple (dB)

fcH is the theoretical passband upper end, i.e. equi-ripple band edge. Table 3 gives the (practical) values of the rejection and frequency parameters for 0.01 dB ripple (α r) in the pass band for various practical n odd values. Practical filter intrinsic-matched conditions, VSWR values between 1.25 & 1.4:1 will in general be obtained depending on practical component tolerances. Table 3 lists (practical) ratios of f(xdB/fcH

percent or less. Minimum filter bandwidth is limited primarily by resonato Q and acceptable filter insertion loss. Of the three possible coupling configurations the capacitively coupled version is the most common due to its economy and ease of manufacture.

Several references are available to guide the design of capacitively coupled resonators but one of the most straightforward approaches is given by Williams. Nodal Q's and coupling coefficients for a wide variety of filters including Butterworth, Tschebyshev, and Bessel filters are listed in tabular form. Component values are found by frequency and impedance scaling of these values. The process is best illustrated by an example.

The design starts with the desired filter Q.

$$Q = \frac{fo}{BW}$$

fo = filter center frequency

BW = filter 3dB bandwidth

Nodal inductors and capacitors are found next.

$$L = \frac{Z}{2\pi foQqn} \qquad C = \frac{1}{(2\pi fo)^2 L}$$

Z = filter impedance

qn = nodal Q (from tables)

The coupling capacitor C_{12} is found by

$$C_{12} = \frac{k12\ C}{Q}$$

k_{12} = coupling coefficient (from tables)

The total capacitance at each node must equal the nodal capacitance. In a two pole filter the shunt capacitor equals the nodal capacitance Minus the value of the coupling capacitor. Working through the equations for a two pole Butterworth, 60 MHz filter gives the filter shown in Figure 5a. The filter bandwidth is 20 percent.

From this point the filter can be impedance and frequency scaled without affecting its percentage bandwidth. A fourfold capacitor value reduction will double the filter frequency and impedance just as before (Figure 5b). Combining this filter with the previously designed L-Match network gives a constant percentage bandwidth filter tunable from 60 to 120 MHz. This filter is shown in Figure 5c.

The inductors are rather small but still entirely feasible for small diameter air wound coils. Accurate repeatable coils can be wound using commonly available machine screw threads as winding forms. (For details see the article by Anderson listed at the end of this paper). Alternatively the inductors can be made larger, and the capacitors made smaller, by raising the 50 ohm filter impedance to something higher with a pair of broadband transformers.

Implementation

Substituting varactors for the variable capacitors in Figure 5c produces a voltage tuned filter. In principal only three varactors are required for a two pole bandpass filter; one coupling capacitor and two tuning capacitors. However, the coupling capacitor is much smaller than the tuning capacitors so two different types of varactor diodes must be used. Moreover, the varactor capacitance variation and tuning curves must match exactly. Finding two different varactors each having the correct capacice and identical tuning curves is very difficult.

A more reasonable approach is to choose a varactor for the coupling capacitor and obtain the larger tuning capacitance by placing a number of varactors in parallel. This way precise tracking between the coupling and tuning varactors is insured although the ratio between the tuning and the

for all-pole Chebishev filters. Where $\alpha_{v.r}$=0.01 dB (passband ripple)

Table 3

Table of Practical Values of f(dB)/fc(high) for x dB Rejection for 0.01 dB ripple, practical, VSWR: 1.25:1 Chebishev all-pole ladder

n	20dB	30dB	40dB	50dB	60dB	70dB	80dB	90dB
7	1.8	2.15	2.75	3.4	4.2	5	-	
9	1.52	1.80	2.15	2.5	3.0	3.5	4.0	
11	1.42	1.73	1.85	2.1	2.42	2.75	3.1	
13	1.32	1.50	1.70	1.90	2.15	2.38	2.65	
15	1.23	1.37	1.55	1.72	1.94	2.15	2.36	2.60
17	1.15	1.28	1.44	1.60	1.77	1.95	2.14	2.30
19	1.12	1.21	1.36	1.52	1.64	1.78	1.90	2.06

FIG. E-3 might well be a graphical specification for a set of 6 filters spanning the 100-1000 MHz power passband where Ki=1.47 and 40dB is obtained as harmonic rejection. Additional figures show Typical-All-Pole-Lowpass Filters.

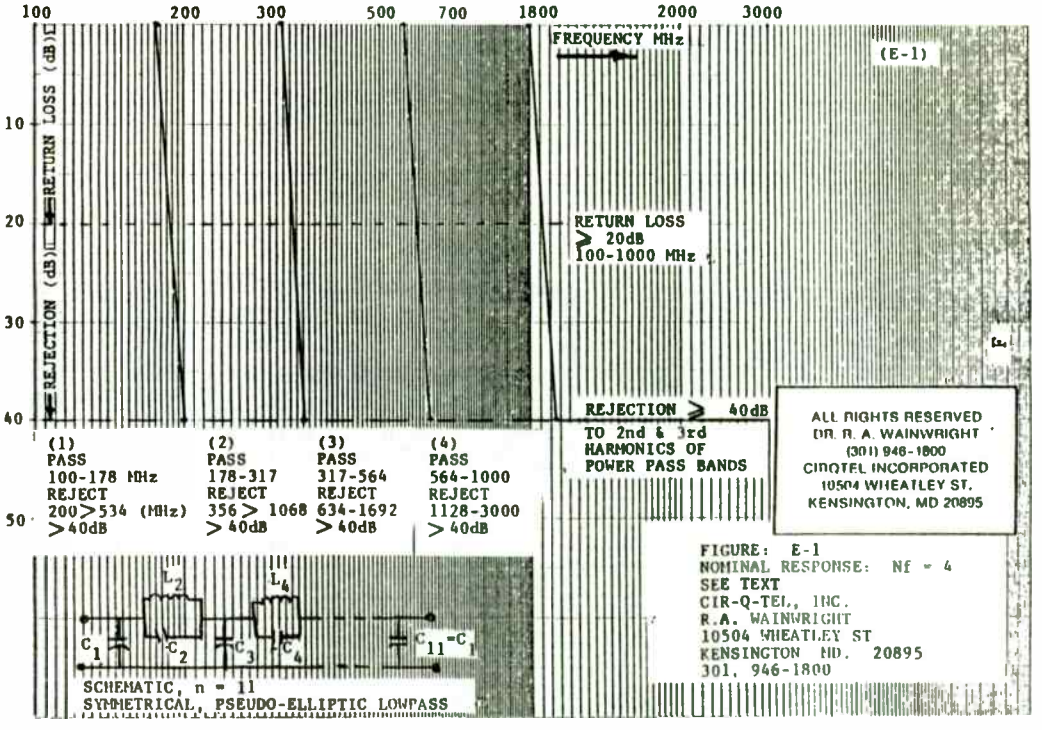
Table 4*

Passband VSWR/ripple (dB)

VSWR	2	1.8	1.5	1.4	1.36	1.3	1.24	1.2	1.1	1.05
ripple	0.51	0.37	0.18	0.12	0.10	0.07	0.05	0.035	0.01	0.0026

* Ref: Cir-Q-Tel, Inc. catalog (since 1962) page 35, Table 28

(E)



coupling capacitors is limited to integer values. Pole to pole and unit to unit tracking is also improved since varactor variations tend to average out across the group.

For the filter in Figure 5c the ratio between the tuning and the coupling capacitance is almost seven to one. Nearly perfect tracking is possible using one varactor for the series coupling capacitor and seven varactors for each shunt capacitor. The BB-109 varactor which has a capacity of 8.8 pf at 15 vdc and 35 pf at 2 vdc is suitable.

The number of varactor diodes required can be reduced by manipulating the filter to reduce the shunt to series impedance ratio. Tapped inductors can be used to increase the size of the coupling capacitor, or decrease the size of the shunt capacitors. The tap can be located anywhere along the coil, however, a centertap providing a four to one impedance transformation is physically convenient. The capacitors scale directly with impedance so a four to one transformation increases (or decreases) the affected capacitors by a factor of four.

The series coupling capacitor can also be increased with a Pi to Tee conversion. First form a Pi network consisting of the series capacitor and a portion of the two adjacent shunt capacitances. Then convert this network into a Tee increasing the value of all three capacitors in the process. Design equations are given in Figure 6. Choosing equal values for C_1, C_2 and C_3 increases all the capacitors by a factor of three.

Intermodulation for Performance

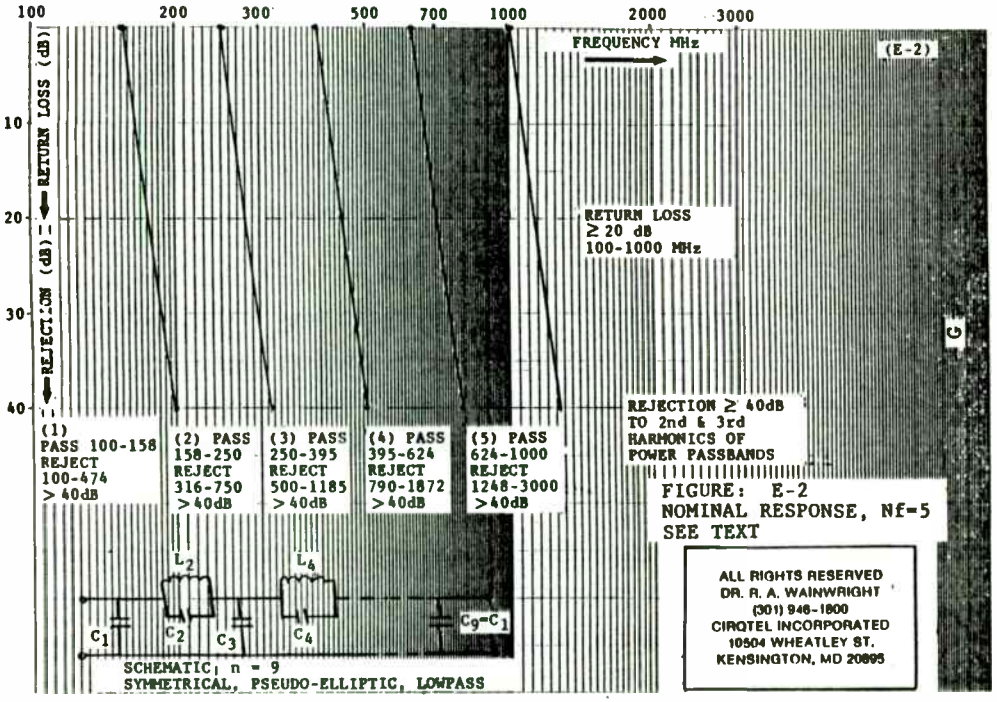
The use of series opposed diodes is often suggested to reduce intermodulation distortion. This configuration makes it impossible for the applied RF to force either diode into conduction. In addition, the RF voltage applied to each diode is cut in half. Large amounts of distortion will be generated if a varactor is driven into conduction but in low power filters the dominant distortion mechanism appears to be RF modulation of the varactor tuning voltage. This effect is most pronounced at low varactor voltages where the slope of the varactor tuning curve is large and the tuning voltage is small.

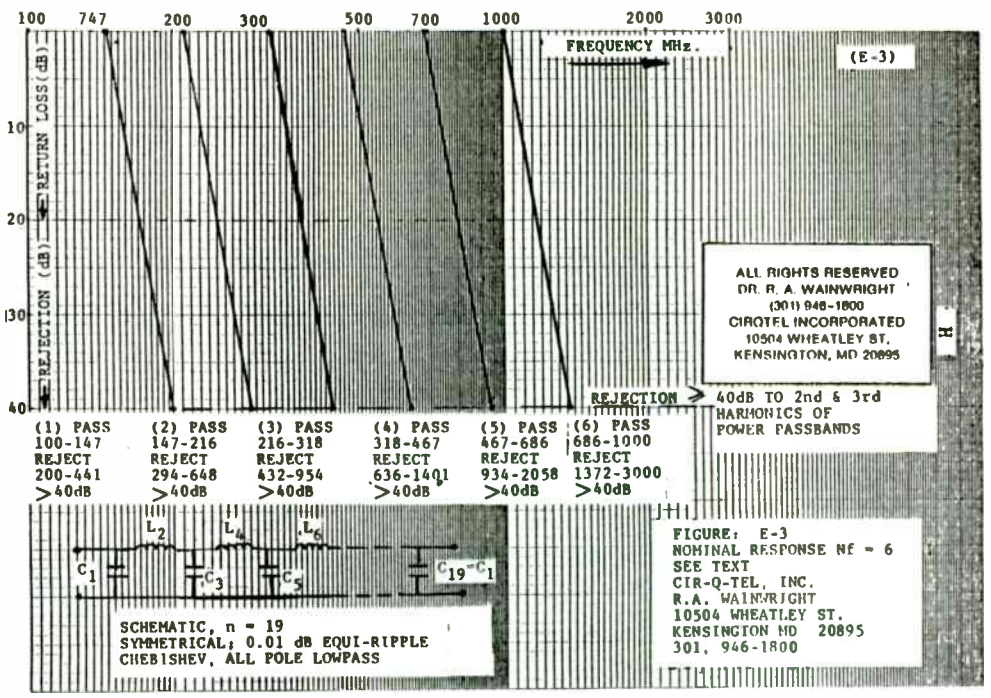
One test with a single pole varactor tuned filter gave an input third order intercept of +10 dBm. Replacing the single varactor diode with a pair of series opposed diodes (total of four varactors) increased the third order intercept by six dB. The tuning voltage was two volts in both cases. Intermodulation distortion decreased rapidly as the tuning voltage was increased. Best intermodulation performance is obtained by keeping the filter impedance as low as possible, avoiding low varactor tuning voltages, and using series opposed diodes.

Tuning Range

Filter tuning range is essentially the square root of the usable varactor capacitance range with octave tuning requiring a four to one capacitance variation. Several factors tend to limit the available tuning range. At the high frequency end stray capacity can significantly limit the maximum filter frequency. At the low frequency end intermodulation performance is degraded and the filter insertion loss may increase.

A simple varactor equivalent circuit consists of a variable capacitor in series with a fixed resistor. When the varactor capacitance is small as it is at higher tuning voltages the resistor makes up a small portion of the overall device impedance and the varactor Q is high. Decreasing the tuning voltage decreases the varactor reactance without greatly affecting the series resistance. The result is decreased varactor Q and increased





filter loss at low tuning voltages. Whether the filter loss actually increases or not depends upon the bandwidth of the filter and the Q of the filter inductors.

Despite these effects octave range filters are easy to build and wide capacitance range varactors such as the Motorola MVAM-125 make filters tunable over at least two octaves possible although perhaps not easy. Needless to say wider tuning ranges require better varactor tracking and greater attention to stray capacitance and inductance.

Frequency Range

Filters below one megahertz are possible although the number of varactors required might be excessive. Increasing the filter impedance helps at the expense of increased inductor size and reduced intermodulation performance.

In the UHF region filters to at least 500 MHz are possible. At these frequencies the filter inductors become very small, the effects of component lead and package parasitics become apparent, and finding suitable varactors is difficult. As before the filter impedance can be increased to reduce the inductor problem but the improvement that can be achieved is limited by the effects of stray capacitance. Careful circuit layout is very important and reducing the tuning range to less than an octave helps.

The maximum practical frequency of these filters is an interesting question. Microstrip and other transmission line techniques come to mind but transmission line inductors have the undesirable property of turning into capacitors if the frequency is doubled. With careful design and construction useful filters with limited tuning ranges might be possible well above one gigahertz.

Summary

The design of voltage tuned lowpass and constant percentage bandwidth filters can be summarized as follows.

- Choose filter type, tuning range, number of poles and impedance.
- Determine initial impedance transformation N needed at the low frequency end of the filter tuning range.
- Design L-Match networks using N obtained above.
- Use tables to design the filter section. Use capacitively coupled resonators to implement narrowband bandpass filters. Filter impedance at the low end of its tuning range is N times 50 ohms in most cases.
- Select fixed padding capacitors to equalize tuning capacity ratios in the matching and filter sections then merge matching and filter varactors. Absorb stray capacitance into the padding capacitor.
- Manipulate filter impedance using tapped inductors or a capacitance Pi to Tee conversion to obtain an integer ratio between shunt and coupling capacitance using a minimum number of varactors.
- Use series opposed varactors and low filter impedances to minimize intermodulation distortion.

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Anderson, Leonard H., "Self-Supporting Coils", Ham Radio Magazine, July 1977.

Williams, Arthur B., Electronic Filter Design Handbook. McGraw-Hill Book Company, New York, 1981.

Zverev, Anatol I., Handbook of Filter Synthesis, John Wiley and Sons, Inc. New York, 1967.

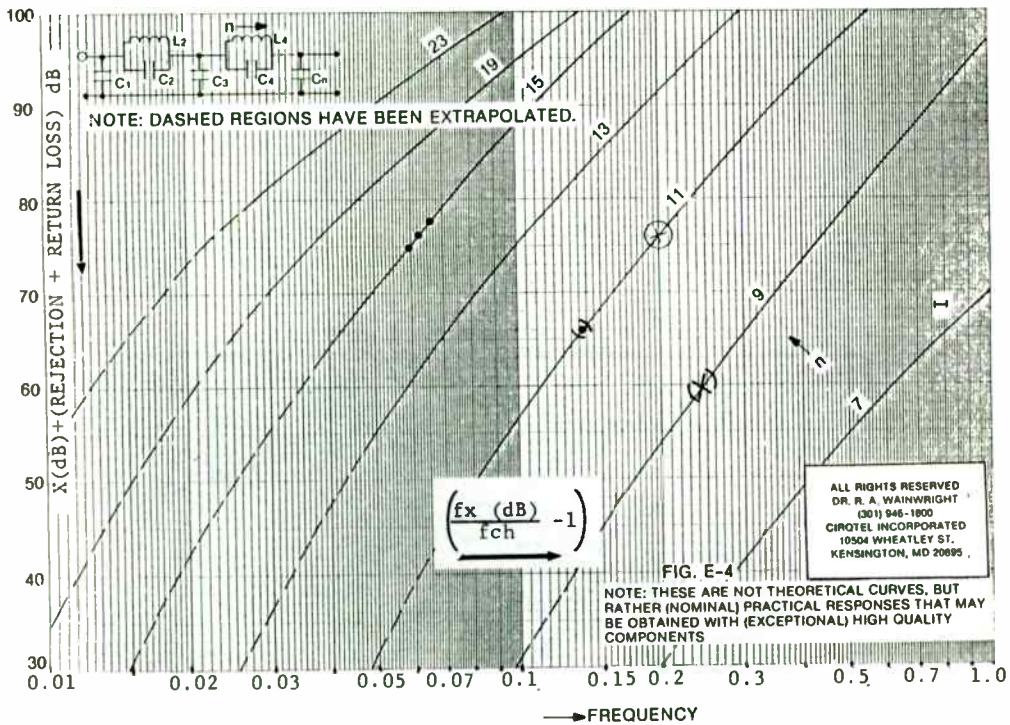
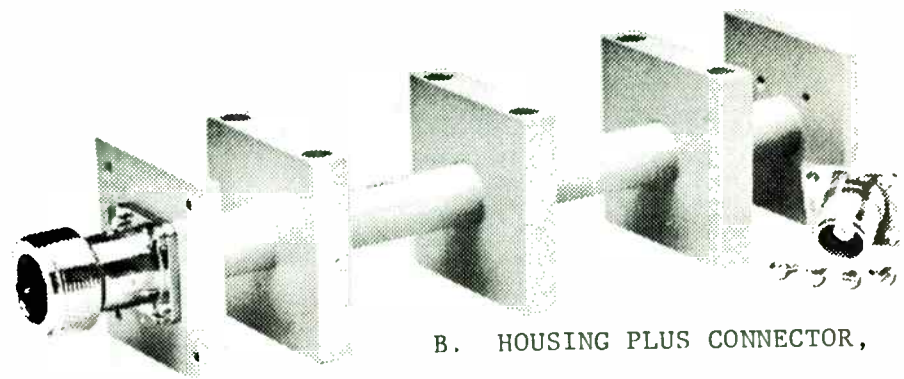


FIG. E-4

NOTE: THESE ARE NOT THEORETICAL CURVES, BUT RATHER (NOMINAL) PRACTICAL RESPONSES THAT MAY BE OBTAINED WITH (EXCEPTIONAL) HIGH QUALITY COMPONENTS

A. FILTER ELEMENT



B. HOUSING PLUS CONNECTOR,

FIG. E-5

LEVY A-Z, n=19 -2KW C.W. 2:1 LOAD-HIGH POWER LOW PASS FILTER; fc = 1.65 GHz

PASSBAND LOSS: 0.1dB TYPICAL

CIRQTEL INCORPORATED

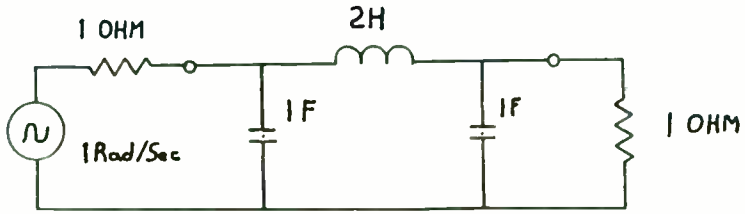
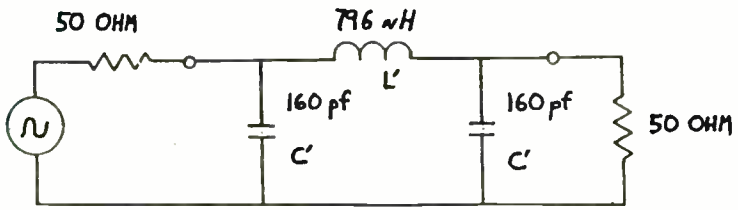
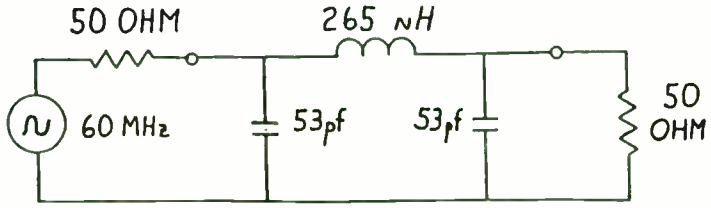


Figure 1a
Butterworth Lowpass Filter Prototype
3 pole, 1ohm, 1 Radian/Second

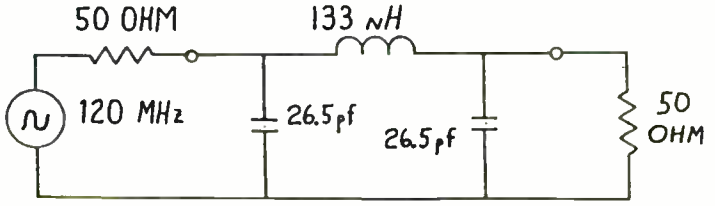


$C' = \frac{C}{2\pi f Z}$ $L' = \frac{L Z}{2\pi f}$ where L and C are prototype values

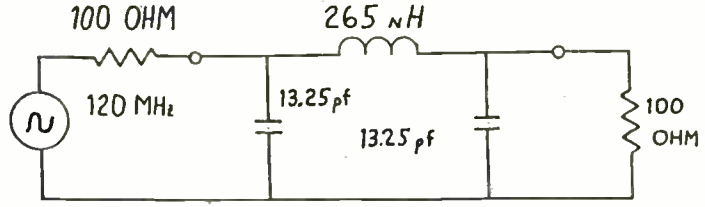
Figure 1b
Butterworth Lowpass Filter
3 pole, 50 ohm, 20 MHz



2a 60 MHz, 50 OHM

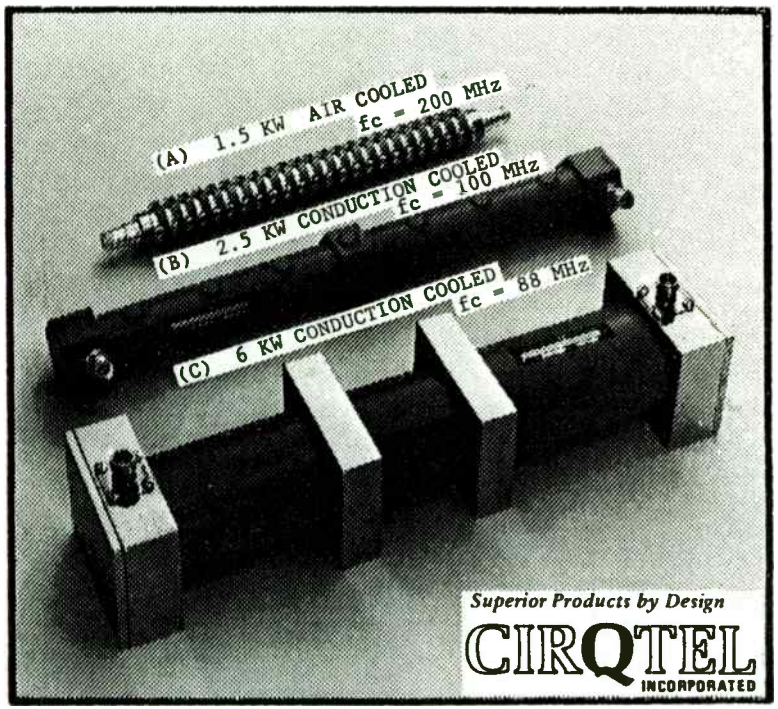


2b 120 MHz, 50 OHM



2c 120 MHz, 100 OHM

Figure 2
3 Pole Butterworth Lowpass Filters



HIGH POWER LOWPASS FILTERS

And now the most versatile of them all...

THE LEVY A-Z
QUASI-LOWPASS FILTER

Power range: 25 x 10^{12} (25 kilowatts to nanowatts); < 1 MHz to 40 GHz.

Similar highpass filters from < 1 MHz - 2 GHz.

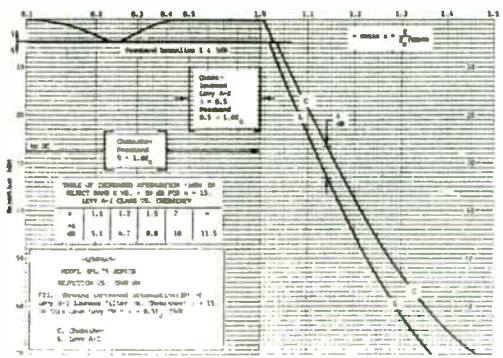
Why the Levy A-Z?

1. Virtually unlimited variation of all poles...Pseudo-Chebishev, sometimes referred to as "ECL", but more appropriately "the Levy A-Z" (designs using Achieser & Bolotarev's arithmetic).
2. Handles much more power (in almost every case) than Chebishev types + sharper response with a lesser number of elements. This means lower loss and higher power in a smaller package (e.g., 0.07dB max. loss over f_c(VSWR) BW in 15-pole, f_c=1650 MHz, 1.5KW filter). (An equivalent Chebishev went up in smoke.)
3. Lowpass filters are seldom required to respond to DC, nor highpass filters to infinity. By trading off unused passband range for selectivity, and a wide range of filter Z_o, we get:
   - added spurious (waveguiding) response-free bandwidth.
   - easily realizable multi-section, passband-limited (as allowed), lowpass or highpass, coaxially configured filters; hence, inherently low-cost filters having time-proven superiority in hostile environments.
   - an internal construction that is far more rigid and reliable than older models of the same externally configured (Chebishev) types and, for that matter, most of the box-like suspended substrate filter configurations.

At Cir-Q-Tel no filter design problem is too great or too small for us to consider. We have more engineers per total employment (25%) than any other significant filter-producing company. Remember, we have over 30 years experience and 10X demonstrated innovative abilities all wrapped up in just one of our world class engineer/scientists.

The coaxial-configured filter has more experience and use application than any other. It works, and works well, so why change to unproven configurations?

Call Dr. Dick Wainwright—his flat passband width at present is 40 GHz!



HIGH POWER LEVY A-Z QUASI-LOWPASS

In our quest for more effective filtering at yet higher power frequency and selectivity with lower loss and VSWR than true Chebishev lowpass filters we designed a full line of quasi-lowpass filters from 1 MHz to 40 GHz, n=7-21, one of which is the HPL/75-1500-19/50-33A/34A.

<0.2dB LOSS

1500W CW in 3:1 VSWR load
<1.25:1 VSWR
850-1400 MHz passband
1.7-3.0 GHz >45-80dB rej
3.3-5.5 GHz >30dB rejection
Type N, SC & LT connectors

Call us for more details about our new quasi-lowpass series and/or for a catalog of our wide range of filters, CIRQULATORS and Isolators.

Superior Products by Design

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INCORPORATED

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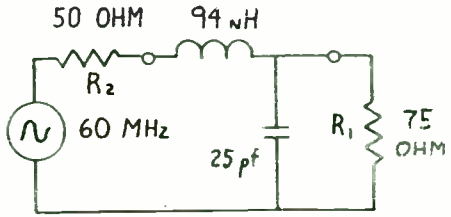
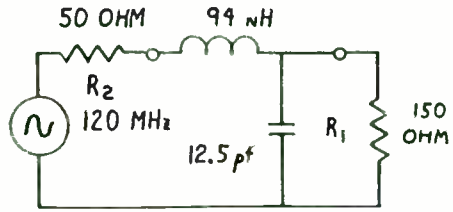
Kensington, Maryland 20895
Telephone (301) 946-5900
TWX 710 828-9521

L



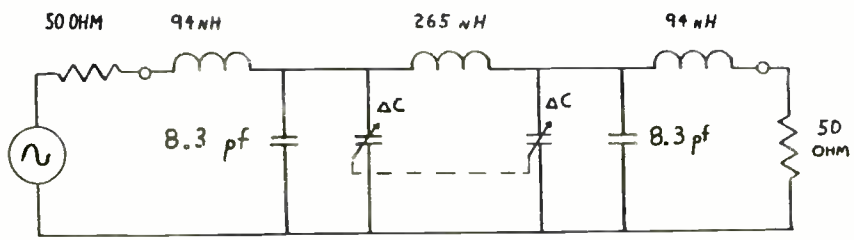
(A)



(B)

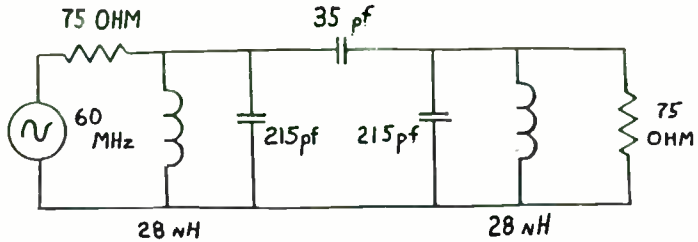
$$X_L = \sqrt{R_1 R_2 - R_2^2} \qquad X_C = \frac{R_1 R_2}{X_L}$$

Figure 3 L-Match Networks

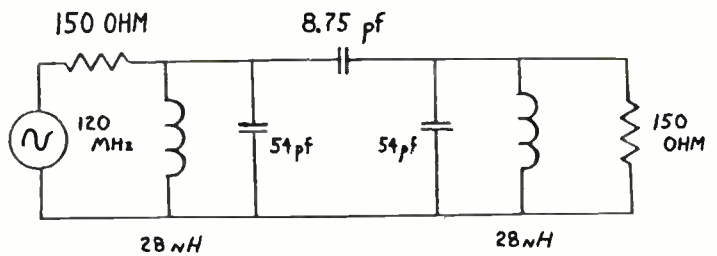


ΔC = 69 pf @ 60 MHz
17.3 pf @ 120 MHz

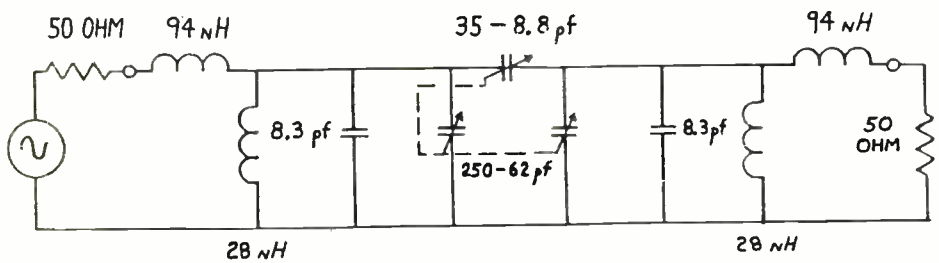
Figure 4 Tunable Lowpass Filter 60 to 120 MHz



(A) 60 MHz, 75 OHM



(B) 120 MHz, 150 OHM



(C) 60–120 MHz, 50 OHM

Figure 5 Bandpass Filters

AN I F LIMITING AMPLIFIER DESIGN ON "K" SOFT BOARD

by

Steve Chambers
Section Head
Discrete and Module Engineering
ACRIAN, INC.

Discriminators have long been used in receiver design for the reception of FM, PM and FSK signals (Frequency Modulation, Pulse Modulation and Frequency Shift Keying). Unfortunately, discriminators are susceptable to instantaneous amplitude pertavation of the modulated carrier. Therefore, because detected noise may be misconstrued as meaningful data, it is necessary to limit the peak amplitude swing to the carrier. For this purpose, Acrian has designed a limiting I F amplifier.

The limiting amplifier design that will be described in this article will limit the peak amplitude swings of the carrier. At the same time, it will establish the receiver's dynamic range, the signal to noise ratio, and other important parameters of the receiver.

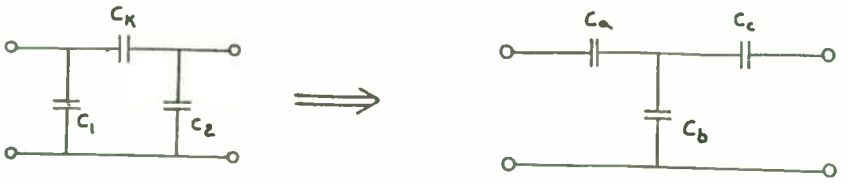
Table I describes the key performance requirements of the limiting amplifier. These key performance requirements are the signal to noise ratio, signal power, noise power, intermodulation distortion, noise pedestal flatness, and frequency range. Note that the signal to noise ratio is -60 dBc with an input of -50 dBm. The signal power output is +10 dBm with a -50 to +10 dBm signal input. The noise power, with a -97 KTN noise power input, must also have a +10dBm output. The intermodulation distortion requirement is -19 dBc. The noise pedestal flatness across the frequency range of 1 GHz + 50 MHz is +5 dB. The noise power requirement of this limiting amplifier design serves to quiet the receiver when no signal is present.

KEY PERFORMANCE REQUIREMENTS

- SNR; -50dBm - INPUT = -60dBc
- SIGNAL POWER, - -50 TO +8dBM INPUT = +10dBm
- NOISE POWER, - -97 KTN NOISE INPUT = +10 dBm
- I M D = -19 dBm
- NOISE PEDESTAL FLATNESS = 5 dB @ 50 MHz
- FREQUENCY = 1000 ± 50 MHz

THE NOISE POWER WAS REQUIRED TO QUIET THE RECEIVER WHEN NO SIGNAL WAS PRESENT.

TABLE I



$$\Sigma C = C_1C_2 + C_2C_3 + C_KC_1$$

$$C_a = \frac{\Sigma C}{C_1} \qquad C_b = \frac{\Sigma C}{C_K} \qquad C_c = \frac{\Sigma C}{C_2}$$

Figure 6 Capacitor PI to TEE Conversion

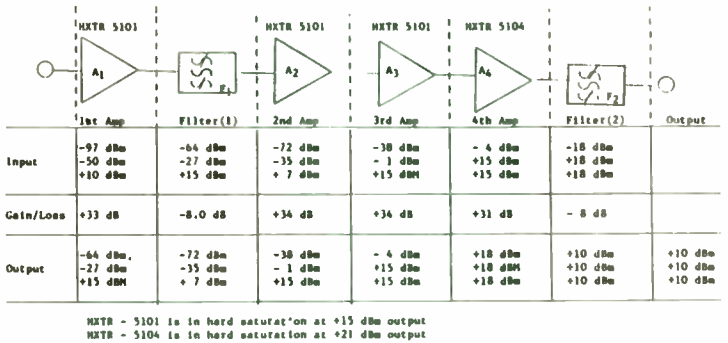
Block Diagram I and Table II shows the allocation of performance by stage. There are four amplifier stages and two filters. The amplifiers each contribute approximately +34 dB gain for a total of 130 dB gain. The gain level of 130 dB is required to amplify the -97 KTN noise energy of the input up to a +10 dBm output. Stage A1 is biased somewhat differently than the other three amplifiers to establish the noise figure of the total amplifier. Filters F1 and F2 both have an insertion loss of -8 dB due to the installation of 3 dB pads at both input and output. Amplifiers A1, A2 and A3 all use HXTR-5101 transistors, while the output amplifier A4 uses HXTR-5104 transistors for a higher saturated output level. Amplifier A1, while establishing the noise figure of the amplifier, also has the widest range of input level (from -97 KTN to a +10 dBm input). Its output saturates at +15 dBm of output power due to the use of the HXTR-5101 transistor.

The block diagram shows that as we get further down the amplification path, each of the amplifier stages is going into hard saturation. This causes a problem in the first layout.

As previously stated, the amplifier A1 establishes the signal to noise ratio (SNR) of the total amplifier. Filter F1 sets the noise bandwidth. Amplifiers A1 thru A4 combine for a total of 130 dBm gain. Filter F2 shapes the signal bandwidth, and Amplifier A4 is in a limiting mode for all input signals.

One of the problems of this design is that all the amplifiers are in hard saturation with the +10 dBm input to the first stage. Amplifier A3 is in a hard saturation at the -51 dBm input level. Ideally, amplifier A4 should be the only amplifier in saturation. This causes several types of problems. When an amplifier stage has an overdriven base emitter junction, the bias becomes negative and the second harmonics increase to a level equal to that of the fundamental signal. This overdriven condition causes this stage to become a good multiplier. It also causes what is known as the McDonald Effect. The McDonald Effect occurs when the emitter-base junction is overdriven by an input signal over an extended period of time. Hot carriers build up in this junction. With hot carriers in the junction, the HFE or Beta of the device goes to 0, limiting the gain of the device.

ALLOCATION OF PERFORMANCE BY STAGE



BLOCK DIAGRAM I

ALLOCATION

- AMPLIFIER A_1 ESTABLISHES THE SNR
- FILTER F_1 SETS THE NOISE BAND WIDTH
- AMPLIFIERS A_1 -A_4 COMBINE FOR 130 DB OF GAIN.
- FILTER F_2 SHAPES THE SIGNAL BAND WIDTH
- AMPLIFIER A_4 IS IN A LIMITING MODE AT ALL INPUT LEVELS.

PROBLEM

- ALL AMPLIFIER IN HARD SATURATION AT THE +10 DBM INPUT
- AMPLIFIER A_3 IS IN HARD SATURATION AT THE -50 DBM INPUT

TABLE II

There are solutions to these design problems. First, it is imperative that we establish a device Beta parameter for the vendor. Second, control of the bias current must be established. Passive limiting must also be added. Figure I shows the current divider ratio of base current to shunt current which is established at a 10:1 ratio. The shunt current is actually 10 times that of the base current. Under these conditions, the effect of the base voltage going negative is eliminated.

Figure II shows the adding of a Schottky barrier diode in a passive limiting application. These diodes clip the input signal, to all stages except for the last output stage, at a .4 Volt peak to peak swing. This can only be done with an FSK, PM or FM type signal and cannot be employed on an AM signal. The overall schematic of amplifiers A1 through A3, shown in Figure II, shows how each of the bases uses a Schottky barrier diode to add the passive limiting. Only one device now remains in an active limiting mode.

In order to design the matching network for amplifier A4, it is necessary to establish some large signal S parameters for the device. Table III shows the published small signal S parameters and the measured large signal S parameters at the appropriate VCE and collector current. In order to establish the optimum S parameters for designing the matching circuitry that works for the output stage, it is necessary to set up a special S parameter measurement test station. This test station employs a signal generator, circulators, an input and reflective power meter, a triple stub tuner, and a special 50 Ohm to 50 Ohm circuit with the transistor soldered in. Another triple stub tuner is used on the output, a spectrum analyzer (HP8410) is needed to check for second harmonic, and an output power meter will be required to obtain optimum output power.

After optimum performance is achieved at each individual frequency, the triple stub tuners are terminated at 50 Ohms and the transistor is removed from the circuit. The network analyzer is used to launch in and measure the output complex conjugate and the input complex conjugate of the device. Figure IV shows such a test setup.

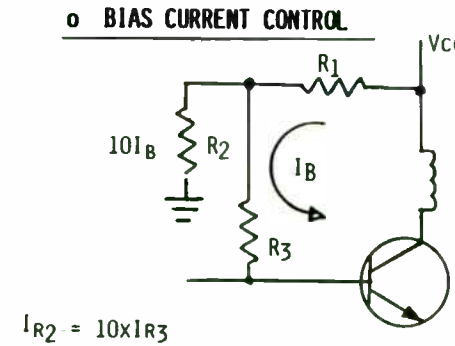


FIGURE I

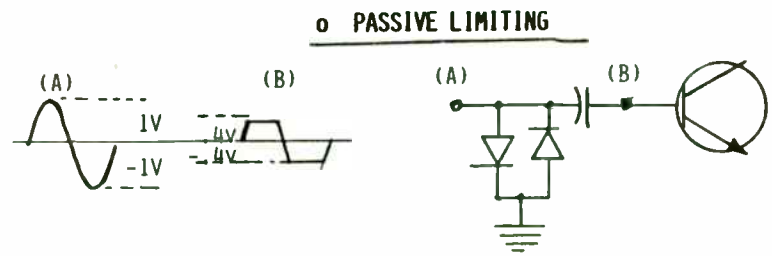


FIGURE II

RF Design Evaluation Made Easier Through Automated Control

by
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P. O. Box 190
Beech Grove, IN 46107

With the advent of work stations for more efficient product development, attention now turns to the task of adequate design and product testing. The manufacturing environment offers an excellent automated testing solution which can readily be applied to the engineering development laboratory. Thia solution is based around the IEEE 488 general purpose interface bus (GPIB). The following discussion will take the reader through an introduction to GPIB, common definitions and specifications, and an outline of criteria for selecting a GPIB instrument. In addition, specific RF design examples will be given to emphasize the enhanced testing capability and efficiency. A series of programs are included in the appendix for reference in setting up similar test and evaluation procedures.

The manufacturing environment has experienced automation for many years. This began with the first assembly lines and continues to be a driving factor for economical production facilities. Industrial societies have learned that automation is an essential requirement for an efficient, as well as high quality operation.

In the past ten years that mind set has found a niche in the development engineering laboratories. We've graduated from mechanical pencils, to hand held calculators, to sophisticated work stations and CAD/CAM development. The impellent for this transition was much the same as for the manufacturing floor. The need was crucial to shorten the development time without risking the quality of the product or incurring undue liabilities by putting a product on the market without adequate testing. In addition, our country is experiencing a shortage of experienced design engineers on top of the rising cost of an engineering education and the rapid rise in starting salaries for new graduates. These factors all call for a new methodology for producing quality products, at a low cost, and even lower development cycle time.

It is easy to see why the application of automated testing has moved into the engineering development laboratory to become a permanent fixture. New design test and characterization can benefit from the same efficiency as manufacturing by utilizing equipment containing automated testing features. Design verification can be made at each level of the product before the finished item is complete, thus saving the need for costly corrections and redesigns. The savings in time and personnel is obvious. Yet, there are other subtle areas where integrated automated testing during product development can have an impact. There is a great potential for a higher quality of work and increased productivity by reducing the tedium and length of tasks; such as harmonic characterization in a particular design. Design documentation becomes easier and an additional confidence in the design is obtained through the ability to repeat the same tests for verification. Essentially, most user error attributed to test methodology can be eliminated.

Current automated design tools for the electronics world are usually inefficient in terms of data bases or are not compatible or applicable.

AMPLIFIERS A_1 - A_3

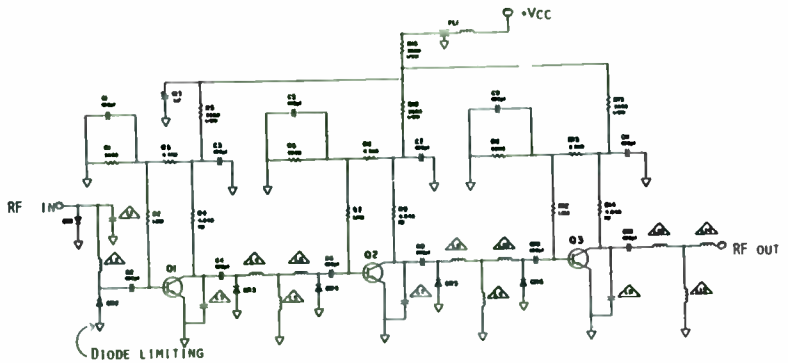


FIGURE III

S-PARAMETER MEASUREMENT

TEST SET-UP

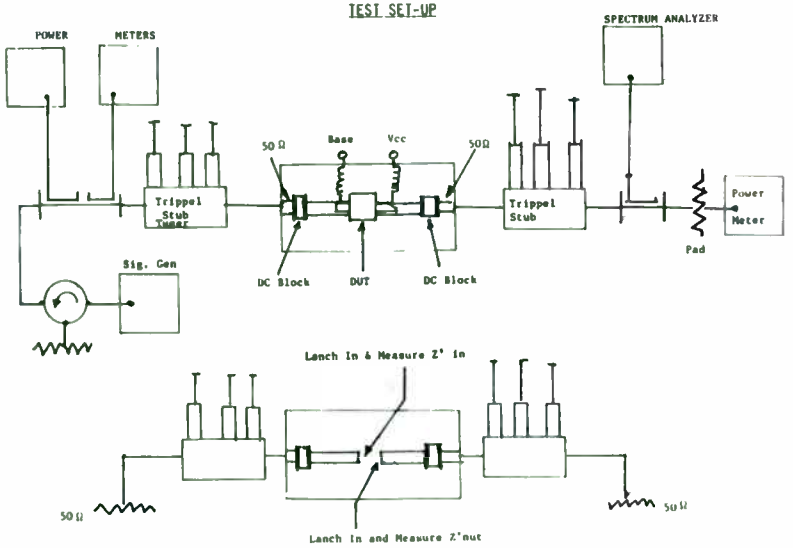


FIGURE IV

Block Diagram II shows the final line up of the devices using the passive diode limiting at each of the stages (except for the last device in A4). As indicated in the block diagram, the output saturated level of all the amplifiers is +9 dBm, well below the hard saturated output level. Only amplifier A4, with its good matching network for large signal parameters, is in saturation. This gives us a flat +10 dBm across the band of interest.

CIRCUIT CARD ASSEMBLY MATERIAL

When it was decided that high "K" Duroid material would be used for the construction of this amplifier, strong concerns were voiced by the production and manufacturing engineers. But there are both pros and cons of using the old standard of Kovar/Ceramic materials. On the positive side, Kovar/Ceramic works and we have procedures that are already in place to manufacture using this material. The thermal expansion of the Alumina/Kovar to the chips mounted on top is approximately the same. It is extremely stable down to -55 C, and we hold etching tolerances to 3 mils + 1mil.

On the negative side, using the Ceramic/COR system, extra drawings are required for the ceramic printed circuit board. Kovar is very heavy and costly to machine and plate. The Kovar carrier must be ultra flat, you must use thin film techniques for etching, and it requires a hot plate. In addition, the alumina substrate requires the use of laser drilling for the printed circuit holes.

While using the Duroid 610.5 material has some manufacturing handicaps (the fabricated boards must be bought outside, new internal manufacturing procedures must be devised, and there is a danger of pad lifting from excessive rework), the advantages are significant. The use of the Duroid material requires no ceramic drawings, Kovar carriers or flatness. The material is flexible and can be batched, stepped and repeated using MC equipment. Most of all, during breadboard testing it has passed temperature cycling on the breadboards from 0 through 85 C with components attached to the boards and using the alumina backing. No dielectric fractures have occured.

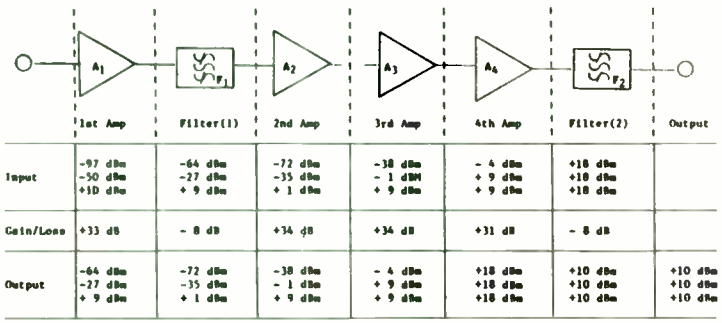
Therefore, the question now becomes "Where are these automated test features available?". The answer is simple, "They are already here - just look for them out in your production facility and bring them into the lab". The General Purpose Interface Bus available on many pieces of test equipment provides the ability for this automated testing. In the engineering lab, it offers one of the best methods for characterizing a new design A GPIB instrument allows the creation of an application specific data base with a minimum amount of pain. Visualize some of the advantages to performing the following characterizations through an automated means: phasa noise, output level accuracy and flatness, frequency settling time and switching speed, spurious and harmonic response. All of these are available now and actual test setups and programs for some of these applications will be given in this discussion.

Let's pause a moment and take a look at GPIB and what it has generically to offer. The GPIB is a communications protocol specified by IEEE 488 "Standard Digital Interface for Programmable Instrumentation". You may have also heard of Hewlett-Packard's version called HPIB. The general purpose interface bus allows the remote transmission of an ASCII data string which simulates the front panel operation of an instrument. Each instrument is assigned an address over the bus and is then polled when activated. This allows for multiple addressing of several identical instruments which are used for the same purpose or provides the means to daisy chain different pieces of test equipment. In comparison, the RS-232 interface requires a specific hardware data port at a host computer or concentrator for each piece of interfacing equipment.

GPIB communication has been available since 1975 and highly accepted and supported since 1978. It provides a digital data exchange at rates of 1M byte per second in a byte aerial, bit parallel format. The IEEE 488 specification provides a means for standardizing the mechanical interface, the electrical interface, and the bus communications protocol that is the signaling of data ready, data accepted, etc. As of this date no standard is provided for the codes and formats which are used to represent the instrument's front panel operation. A subsection of the IEEE P-981 Committee called TAPIS (Transportable Architecture for Programmable Instrument Systems) is trying to standardize on the codes that GPIB instruments understand. A published document on their recommendations will probably not be available for another year as they were scheduled for completion Mid 1986 and have not yet reached that milestone. For now, the format of codes is instrument dependent. In some cases, a specific manufacturer may use the same codes and formats for all of their products. In any event, it is the instrument dependent qualities of GPIB application which make the selection of test equipment critical. This interface is tantamount to the successful transition of the automated test from the manufacturing to the development environment.

Aside from the decision to employ automated testing through GPIB there is a bit of system design which must be completed in order to produce the test setup. The system will require the device under test, the GPIB test equipment, and a system/test controller. The test equipment involved must be capable of either receiving external communication, transmitting information, or both. In GPIB lingo, these qualities are referred to as listen and talk.

DIODE LIMITING PERFORMANCE BY STAGE



	1st Amp	Filter(1)	2nd Amp	3rd Amp	4th Amp	Filter(2)	Output
Input	-97 dBm -50 dBm +10 dBm	-64 dBm -27 dBm + 9 dBm	-72 dBm -35 dBm + 1 dBm	-38 dBm - 1 dBM + 9 dBm	- 4 dBm + 9 dBm + 9 dBm	+18 dBm +18 dBm +18 dBm	
Gain/Loss	+33 dB	- 8 dB	+34 dB	+34 dB	+31 dB	- 8 dB	
Output	-64 dBm -27 dBm + 9 dBm	-72 dBm -35 dBm + 1 dBm	-38 dBm - 1 dBm + 9 dBm	- 4 dBm + 9 dBm + 9 dBm	+18 dBm +18 dBm +18 dBm	+10 dBm +10 dBm +10 dBm	+10 dBm +10 dBm +10 dBm

BLOCK DIAGRAM II

THE ACTIVE LIMITING STAGE

- THE LAST STAGE OF AMP A_4 IS THE TRUE ACTIVE LIMITER.
- MUST USE LARGE SIGNAL "S" PARAMETERS TO DESIGN THE INPUT AND OUTPUT MATCHING NETWORK.
- HP SMALL SIGNAL S-PARAMETERS

  V_{CE} = 18V, I_C = 110MA

S11	S21	S12	S22
.64 ∠179	3.7 ∠ 69	.08 ∠32	.32 ∠ -90

- MEASURED LARGE SIGNAL S-PARAMETERS

  V_{CE} = 10V I_C = 35MA

S11	S21	S12	S22
.70 ∠169	1.5 ∠ 78	.10 ∠ 64	.21 ∠-105

TABLE III

CONCLUSION

When designing an IF limiting amplifier that requires 130 dB gain, passive limiting is critical at each individual stage except for the last output stage. The last stage, which is actually doing the active limiting, must have large signal S parameter data taken in order to establish good input and output matching networks. Passive diode clipping or limiting can only be used with FSK, FM or PM type modulation, and cannot be used for AM. High "K" Duroid material makes an excellent material for this type of circuitry.

A device that listens is capable of receiving data over the common bus when and only when it is addressed. Examples of these devices are programmable signal sources, programmable power supplies, printers, and "dumb" display devices. A device that talks is capable of transmitting data over the common bus under the same addressing conditions. Examples of talkers are frequency counters and tape readers.

Some instruments include labeling on the back of a piece of test equipment that will give the equipment's specific level of GPIB intelligence. Be careful, not all instruments can both talk and listen. The HP 8656 A or B signal generator, for example, is a listen only device. Unfortunately, decoding the GPIB label may be difficult if it is not properly documented or if a copy of IEEE 488 is not readily accessible.

For a quick overview of what to look for, take the example of the Wavetek 2500 signal generator. It has complete source and acceptor capability (SH1, AH1), is a basic talker and listener (T6, L4), has extended modes of talk and listen disabled (TE0, LE0), has complete remote/local (RL1), device clear (DC1), and device trigger (DT1), and service request (SR1) capability. It has the parallel poll (PP0) and controller (C0) options disabled. E2 designates the type of electrical interface as one using tri-state drivers as opposed to open collector (E1) drivers.

In addition to the talk and/or listen capability of the test equipment, the system will require a GPIB controller. The controller will specify the talkers and listeners on the bus and regulate the data flow and access. Most controllers will also provide a means of programming test sequences to further increase throughput. Usually, this programming will be in BASIC or a BASIC related form for universality.

There are several sources of controllers in the current marketplace. The traditional form is an independent, dedicated instrument with keyboard entry and some sort of display feedback. Wavetek, Tektronix, and Hewlett-Packard all make this sort of GPIB controller. With the wide acceptance of IBM PC compatibles there are several companies producing plug-in boards for P.C.s to perform the IEEE 488 interfacing. In many cases, this can also be accomplished through an RS-232 to IEEE 488 converter. National Instruments and IOTech manufacture such equipment which allows the user to tap off of computer resources currently in house.

A good application of the PC type arrangement is a custom integrated workstation consisting of an IBM PC with a GPIB interface card communicating with an HP 8753 Network Analyzer with S parameter test set and the design under test. Using GPIB and Touchtone software the device under test can be fully characterized.

There is little specific advice for selecting a controller. The basic guidelines of cost, ease of use, longevity, and compatibility, as used in any capital expenditure, should be taken under consideration. Efficient usage of equipment provides a strong case for selecting a PC based product for integration as a controller. The drawback to be aware of for this application is the speed of execution. The PC products are notoriously slower than dedicated controllers which can be a distinct hinderance in the ATE environment.

As alluded to briefly before, it is in those areas, unregulated by the IEEE standards, which make the selection of automated test equipment critical. It is the area of codes and formats that exhibits the least amount of standardization. As each piece of test equipment has its own set of codes and formats, the user is essentially learning a new language developed specifically to talk to that equipment. The language should offer a consistent methodology for replicating the front panel operation of the instrument. The codes should be easy to remember through the use of mnemonics with the restrictions of being neither too cryptic nor too verbose. As an illustration, look at the specification of frequency, RF output level, and AM using the HP 8901A modulation analyzer and the Wavetek 2500 signal generator.

HP 8901	Wavetek 2500	Specification
M5	FRQ	frequency
R2	dBm	suffix for RF output level
M1	IAM	AM, the 2500 has internal AM (IAM) and external AM (XAM)

Though both offer a simplified mnemonic for the specified front panel input, there are no memory clues provided in the 8901 code.

More than a simplified code is needed to adequately convey the meaning of the front panel operations across the GPIB bus. The code should provide for a variety of numeric input formats such as engineering suffixes (MHz) and exponents (E6). Flexibility should be allowed in the syntax of the programming e.g. the use of space characters should not be restricted. In selecting a GPIB instrument, remember, the user will have to be learning a new programming language. To reduce the learning curve time, that language should be as close to normal conversant engineering terms as possible.

Some instruments have accomplished the task of providing a user friendly interface with a technique called minimum uniqueness formatting. This means that each command entry (front panel function) can be represented by a minimum number and sequence of alphanumeric inputs. As long as the user includes those minimum characters in the required order, any version of the command can be accepted. The minimum format may be consistent for all entries, such as a three character mnemonic, or it may vary. If the only command available starting with the letter F is frequency, then the minimum representation of a frequency input may be the single initial letter. Using the minimum uniqueness philosophy, F, FRQ, FREQ, FRQCY, FREQUENCY may all be employed to request a frequency command. In addition, an instrument with this type of coding will usually allow any combination of upper or lower case letters.

After formatting the command portion of the GPIB message, there is a requirement for formatting the numeric entry and termination of the message. Fortunately, there is a defacto standard for all of this data entry, pioneered by Tektronix. Tek codes and formats are specified under Tektronix Standard 962-1780-01 and cover the device dependent message coding for all Tektronix GPIB controllable products. As the IEEE standard is not yet available, any instrument advertising that they conform to Tek codes and formats will be the closest to following a standard as there is today.

DESIGN OF COMBLINE and INTERDIGITAL BANDPASS FILTERS

by Dick Wainwright
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Abstract: The economic design of parallel coupled bandpass filters, e.g. interdigitated and combline having rod (finger-like), helical coil and annular ring inductive elements with necessary tuning capacitors C_t, in precision machined rectangular box-like (ground plane) containers can be an expensive proposition, especially given the fact that the average purchase order quantity for such devices is in the order of 10-15 units. Hence, in general, the savings resulting from volume manufacturing processes are not available.

Standardization is in many organizations a sometime thing. The cost of precision machining for small volume orders even with CNC machining substantially drives the cost of manufacturing, the making of cavities-holes, drilling and tapping is expensive in any shop, by almost any means.

The component value(s) realization of various filters having Pseudo(Quasi) 1/ Elliptic, (Inverse Chebishev), all-pole Chebishev, Butterworth, Gaussian, Bessel and other response shapes to satisfy a given set of specifications is not terribly difficult. One can, with a digital computer, design rather complex devices in seconds - the precision machining and assembly processes may take hours. If one must "design in" self equalization 1/ and/or near band edge traps by means of non-adjacent resonator coupling, etc., the machine assembly/adjustment times may expand astronomically and will usually require very astute technicians for their adjustment.

This paper suggests designs* that have been realized in round, hollow, right circular cylindrical ground-plane housings that have been manufactured in substantial quantities, that yield superior time and frequency responses. Cavities-holes are expensive, unless one buys them ready-made, as is the case with the seemingly infinite variety of commercially available tubing: round, rectangular or of almost any shape, size, wall thickness, material, etc. that are easily made by casting, drawing or extruding and perhaps by other means.

The round-tube ground plane housing is easily punched, drilled, tapped, plated, painted, etc., and it provides degrees of freedom for a wide variety of resonator shapes: posts, helically coiled of many shapes, annular ring-like (uniform transmission line, semi-microstrip-line) (Fig.1),

*Patent(s) Applied For

1/ J. D. Rhodes, "Theory of Electrical Filters" Chapter 7, John Wiley & Sons ISBN: 0 471 71806 8

Tektronix presents a great amount of detail on the formatting of a basic message unit. There are several building blocks which are combined as required for each message. The code representing the front panel command key is termed a header. With a header there may be an argument which can be either a numeric entry, such as a frequency setting, or a character entry, such as commanding "RF ON". Each message is completed with a terminator which may be an end of message designator such as carriage return / line feed or it may be a concatenation terminator indicating that there is another message on the same line. The diagram below illustrates a typical message string.

HEADER sp NUMERIC ARGUMENT sp SUFFIX sp TERMINATOR

The spaces in all areas except between the header and first argument are optional. The following examples are actual code input for the Wavetek 2500. They illustrate both the minimum uniqueness format and the methods of building a complete message string.

Frequency 500.00 MHz; LVL 300 mV; RF ON cr lf

IAM 50%; FRQ 123 E6; Level 500 E-9; STR 5 lf eoi

The semicolon is used as a message delimeter and the end of string terminations are actually control characters and are not actually printed.

Aside from the friendliness of the user interface, choosing a GPIB instrument should also include an evaluation of supplementary functions. These are commands which are available to the GPIB user but are not accessible from the front panel of the instrument. One of the biggest advantages is remote error reporting. A GPIB user may be able to receive RF error feedback from the instrument in more detail and in a more obvious manner than the local user. Indications such as FM over deviation, loop unlocked, and carrier unleveled can be communicated across the bus as soon as they occur and in "plain English" terminology. Error reporting may also include syntactical errors as related to the GPIB input e.g. Header Error, and system and communications errors. Additional enhancements such as service requests from the instrument to the bus controller and executing a group of commands simultaneously may also be available.

The concerns outlined above are basically software driven. There are other areas to be aware of when selecting a GPIB instrument which are more hardware related. Two rather simplistic ones involve setting the address of the instrument and the end of string identifiers. If these items are assigned via a hardware switch in the GPIB instrument further investigation as to the location and accessibility of the switch is needed. A software override of the address and termination may also be provided.

Some unobvious pitfalls may be present in the actual digital architecture of the GPIB instrument under consideration. If a single processor is controlling all instrument functions, the speed of execution may be relatively slow. This will effect both the GPIB responsiveness and the RF output. If the instrument uses two separate processors for control, specifically separate processors for the front panel operations and GPIB communications, there is a possibility of master/slave contention. Care should be taken to determine which side has execution priority so that the maximum throughput can be obtained.

In addition, a GPIB processor will need to have its clock running at

which may be simply arrayed in comb-line, interdigital, or, because of the round element mounting (ground) plane one may angularly rotate (Fig. 2D) the elements up to ± 180° (Θ plane) or tilt them (Ψ plane)-(yaw-Z axis) or rotate annular inductors in the ± ϕ plane. One may also simply add fixed or adjustable decoupling elements and/or design for very wide tuning ranges, e.g., narrow band designed for up to 7% dB BW, or more, that may be simply adjusted over 2:1, 3:1, or, 5:1 tuning ranges. Many such devices have been designed and constructed. In the case of helical coils, pitch and winding sense may also be a design variable.

By proper design of coupling structures and general parts layout, one may obtain nearly constant percentage/MHz bandwidth over very wide tuning ranges in the 1 MHz 18 GHz range of frequencies.

The possibilities literally boggle one's imagination!

All devices electronic contain nothing more than: coils (L), capacitors (C), ± resistance (± R) or the equivalents or mixes thereof, and their necessary connections by means of conduction or induction (field coupled), which are necessarily limited to L, C or R or a mix thereof as elements/equivalent elements, in passive circuitry.

Figures 1 and 2 are self-explanatory. Figure 1 shows some of the possible inductive element, physical configurations that may be used in round-tubular ground plane housings. Figure 2 shows some possible array configurations of the inductive elements that may be used in a round-tubular ground planes. Figure 3 gives details on an 8 resonator, interdigitated, annular ring inductive element bandpass filter that tunes the range 300 > 600 MHz, having a nominal 3 dB BW of: 1.3% @ 300 MHz, 2.5% @ 450 MHz and 3.3% @ 600 MHz, roughly linearly increasing % 3 dB BW vs. fo, as was required in the specifications.

Table 1 lists general passband responses for this device. Figure 3C and D are plots of the general passband response. Figure 3D is the plotted response obtained while sweeping the passband and from 125 MHz to 4.9 GHz. Over 80 dB of rejection was obtained for this filter on an HP N.A. 8505 sweeping to 1.3 GHz. However, the plots given were taken on an HP scaler N.A. having a noise floor of roughly -50 dBc. Figs. 3D and 3G are the filter responses with wide band sweep, as indicated. Figs. 3E and 3H are plots of the group delay responses.

TABLE 1

fo MHz	∝ fo dB	3 dB BW	±10° (MHz) LINØ BW	±5° (MHz) LINØ BW	±2.5° (MHz) LINØ BW	1.5:1 (MHz) VSWR BW
300	8.1*	4	4.4	3.5	2.7	2.7
600	5.4*	20	27.2	17.9	11.8	11.8

* All tests were on unplated devices of aluminum construction. Data measured on an HP 8505 vector N.A. for Table 1.

all times in order to detect its address from the bus. This clock will induce noise throughout the instrument. How the manufacturer handles the area of RF immunity to this clock noise is another critical point.

The actual GPIB interface to the BUS can be controlled through a single dedicated chip. This relieves the instrument software from the handshaking tasks. Several devices are currently on the market to handle this communication. Yet, some of those do not conform to the IEEE 488 standard nor can they handle the higher data transmission rates now prevalent in today's technologies. In those cases, data can actually be lost. Another pitfall is the exiatence of ghost interrupts through the BUS communication device. These are timing related problems where the controller is faster than the interfaca device used in the instrument being controlled. The interface device can miss critical communication signals due to its inability to handle the transmission rates.

In summation, there are critical areas to research in choosing a GPIB instrument which involve both software and hardware. The most evident area, though, is that of the user interface. The user is essentially employing three different languages when implementing an automated test setup: the language of the test instrument (individual codes and formats), the language of the controller, and the language of the control program. Choosing a system which will reduce the learning curve in any of these areas will be a great asset.

Now that you have completed a crash course on selecting and setting up a GPIB system, here comes the fun part. What can you actually do with this information?

For the GPIB novice, the appendix includes a walk through program demonstrating talk and listen features. This program is written for the HP 9825 controller and the Wavetek 2500 signal generator. It shows the combination of controller language and instrument specific language which a user would have to implement to achieve GPIB communication.

A typical example of an efficiency improvement through GPIB usage is the characterization of harmonics as related to the carrier in an RF design. This is a task which is exceedingly tedious to do under manual conditions. Typically, a system under test would be connected to a spectrum analyzer. The user would manually change the source frequency and "eye-ball" the occurrence of harmonics and spurs. Of course, it was easier if one knew where to look in frequency range and in level. By automating this sort of test, no previous knowledge of the circuitry is needed. A purely objective search can be made across the frequency band and a recording can be produced showing all power occurrences. The same test could be repeated at several temperature ranges to characterize the loss in the attenuators due to increases in temperature. Spikes or drops could be easily located emphasizing the phase relationships between various oscillators. All of this could be plotted and permanently stored in a period of 15 minutes. Factors such as allowing settling time for the signal generator can be included in the controlling program insuring the most accurate data possible.

The sketch below illustrates the test set up for harmonic characterization of the Fluke 6060A signal generator. Included in the appendix are plots of the results at varying temperatures.

Figure 4 gives general details on a 10 resonator combline tunable bandpass filter tuning from 3>8 GHz (the electrical performance data on the devices shown in Figures 5C through F are incomplete in that the N.A. noise floor is shown at about -60 dBc. This unit should yield an ultimate rejection of well over -100 dBc).

The tunable combline filter shown in Figure 4 has essentially a 2.5%, 3 dB BW over its entire>3:1 tuning range: 3>8 GHz. No noticeable spurious returns (above approximately -60 dBc) are apparent to nearly 13.4 GHz over the entire tuning range.

If one were so inclined, one might say that this device in an evanescent mode device at the lower tuned frequencies where:

$$\frac{F\ (min)\ mode}{Fo\ (min)\ tuned} = \frac{13.4\ GHz}{2.7\ GHz} \sim 5:1$$

and a combline at the upper reaches of its tuning range where: $F\ mode/f_o = \frac{13.4}{8.15} < 2:1$

Remembering, of course, that the response above 13.4 GHz is waveguide moding, and not an element caused spur response.

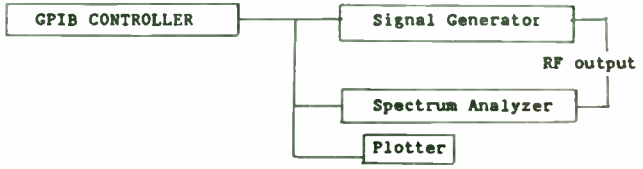
Figure 5 gives the general details on the rotation coupled (WS^2 /Θ,Ψ,ϕ, p,) bandpass filter, in this case a 4 pole, 2 zero tunable device tuned to 92.3 MHz, spacing, sense, and judicious use of partial electric walls and an adjustable coupling capacitor between two of the elements yields exceptional time and frequency domain properties in a relatively small package weighing 4.2 ounces.

Figure 5C: Linear frequency, 2 cycle semi-log plot of: amplitude, return loss and group delay. The group delay is exceptionally flat to the 7 dB, B.W. and then rolls off monotonically, a general characteristic of linear phase filters that also have excellent time domain properties.

The additional data table: (Figure 5C) shows tabulations for the non-linear $\pm$ 1° and $\pm$ 0.5° bandwidths; the interesting features are, however, the exceptionally deep notches: 110-112 dBc, and the pulse response, which was traced from an oscilloscope photograph; the apparent time sidelobe (note: looks more like it may have been caused by a load mismatch since it is devoid of normal zero-axes crossings which are typical of the "ringing effect") is on the order of -33 dBc, which incidentally is the return loss minima value measured at fo. See Return Loss Plot (Figure 5C)

Conclusions: The physical realization of parallel coupled-tubular-like, combline, interdigital filters and the use of angularly variable coupling means Θ, Ψ and ϕ angle rotated elements for controlled coupling/decoupling have been described for a variety of inductive element

The use of this type of program was exceedingly beneficial in determining whether or not the generator met its rated specifications.



Using the same setup, automated testing can be used to determine the frequency switching time of a new design. The following two plots show the responsiveness of the Wavetek 2500 during its initial design stages. The signal generator is rated at a switching speed of 200 ms, +/- 100 Hz of final value in CW and for changes greater than 10 kHz in FM mode, with a typical speed of 100 ms. To prove the initial design, GPIB testing was used to determine, plot, and record the switching speeds across critical bands. This exercise was extremely beneficial in pointing out both the high performance areas, as seen in the switch completed in approximately 50 msec, and the areas which required refinement. Such characterization can assist not only the design groups but can emphasize design superiority in a sales or marketing arena. A picture is worth a thousand words as the saying goes. Those pictures, proving technical superiority, are easily generated using GPIB test procedures in the engineering lab. The program used to generate the switching time evaluation is also included for your reference in the appendix.

The last example to be presented is no more complex in test procedures or setup as the previous illustrations, but does encompass a more critical RF design area, that of phase noise characterization. As the local oscillator phase noise will affect the overall performance of a receiving system, obtaining an accurate analysis of the receiver system is highly critical. In a manual mode, this measurement is time consuming and highly vulnerable to human error. In an H.P. application note (270-2) the recommendation is to use a narrow resolution bandwidth and perform eight sweeps, collecting data by hand at specified offset frequencies. All of these functions can be efficiently programmed and controlled through the use of the GPIB and a programmable spectrum analyzer. Using the programmable features of the analyzer will provide the opportunity to determine the phase noise sideband envelope over a wide frequency range. This is done by selectively avoiding discrete signal points.

The last series of charts in the appendix shows a thorough evaluation and comparison between Fluke, HP, and Marconi signal generators with respect to upper sideband phase noise.

Again, the use of test equipment with GPIB can be seen as a very valuable design development tool. It can be employed both in technical market definition, such as the comparison of competitive equipment, and in design definition and evaluation. GPIB in the engineering lab increases both the credibility of the data and the efficiency in obtaining that data. Certainly, RF design testing can be made easier through automated testing procedures.

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SMM

configurations that are easily incorporated into moderately narrow band tunable bandpass filters. Because tunability was of prime consideration in these designs, wide bandwidth > 5% BW 3dB was not considered. However, much wider bandwidths are practical with many of these structures, depending on (a) type of resonator, and (b) orientation of inductive elements, spacing, θ, Ψ, and ϕ angle relationships, etc.

Coupling or decoupling may be obtained by spacing, rotation or by the use of decoupling iris, or other means, in the form of probes, crossing wires or posts which may in turn be rotated as a design variable: Figures 5.

As an added feature, one may incorporate (a) partial walls (septums) which may be rotated as to position to provide controlled decoupling (partial electric or magnetic walls) or one may use direct or tapped L or C coupling to further enhance the range of possibilities for various response shapes in the frequency and/or time domain.

A generalized design procedure has not been presented here since the arithmetic is rather cumbersome and to some extent proprietary; also, patent protection has been sought on the general design of all of these devices.

(conclusions continued on page 8)

(conclusions continued)

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(3) G. L. Mattaei, L. Young, E. M. T. Jones, "Microwave Filters, Impedance-Matching Networks and Coupling Structures" Chapters 5-8, McGraw Hill Book Co. Copyright 1964, Library of Congress Catalog Card No. 64-7937

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```
0: "LISTEN & TALK ROUTINE on 2500":
1: "t1f0?T#202 204u086":
2: trk 1:lol 8
3: dim M$[2],O$[2],R$[40]
4: "GPIB address":dev "sg",702
5: "Time delay ms":500)w
6: cli 7
7: wait W
8: "Enable SRQ":wrt "sg","ROS ON"
9: wait W
10: gsb "ROS"
11: osb "SELECT"
12:
13: "FRQ":fxd 5
14: ent "Enter FREQUENCY in MHz",F
15: wrt "sg","FRQ "&str(F)&" MHz"
16: wrt 0,"FRQ "&str(F)&" MHz"
17: wrt "sg","FRQ?"
18: gsb "Read"
19: gsb "SELECT"
20:
21: "LVL":fxd 2
22: ent "Enter OUTPUT LEVEL in dBm",L
23: wrt "sg","LVL "&str(L)&" dBm"
24: wrt 0,"LVL "&str(L)&" dBm"
25: wait W
26: wrt "sg","LVL?"
27: wait W
28: gsb "Read"
29: gsb "SELECT"
30:
31: "MOD":fxd 2
32: ent "Enter: IAM, IFM, XAM, or XFM",M$
33: if M$="IAM" or M$="iam" or M$="XAM" or M$="xam":osb "AM"
34: if M$="IFM" or M$="ifm" or M$="XFM" or M$="xfm":osb "FM"
35: osp "SELECT KEY or Press CONTINUE":stp
36: gto "RTE"
37:
38: "AM":fxd 1
39: ent "Enter AMPLITUDE MODULATION in %",M
40: wrt "sg",M$[" "&str(M)&" %"
41: wrt 0,M$[" "&str(M)&" %"
42: wait W
43: if M$="IAM":wrt "sg","IAM?"
44: if M$="XAM":wrt "sg","XAM?"
45: wait W
46: osb "Read"
47: ret
48:
49: "FM":fxd 2
50: ent "Enter FM DEVIATION in kHz",M
51: wrt "sg",M$[" "&str(M)&" kHz"
52: wrt 0,M$[" "&str(M)&" kHz"
53: wrt "sg",M$[2]
54: wait W
55: osb "Read"
56: ret
57:
58: "RTE":
59: ent "Enter 1000 or 400 for MOD RATE",R
60: wrt "sg","RTE "&str(R)
61: wrt 0,"RTE "&str(R)
62: wait W
63: wrt "sg","RTE?"
64: wait W
65: osb "Read"
66: gsb "SELECT"
67:
68: "MOD OFF":
69: wrt "sg","IAM 0%:IFM 0 kHz:XAM 0%:XFM 0kHz"
70: wait W
71: wrt "sg","MOD OFF"
72: wrt 0,"MOD OFF"
73: wait W
74: wrt "sg","MOD?"
75: wait W
76: osb "Read"
77: osb "SELECT"
78:
79: "RF":
80: ent "Enter ""ON"" or ""OFF"" for RF state",O$
81: wrt "sg","RF "&O$
82: wrt 0,"RF "&O$
83: wait W
84: wrt "sg","RF?"
85: wait W
86: gsb "Read"
87: gsb "SELECT"
88:
89: "SET?":
90: wrt "sg","SET?"
91: wait W
92: osb "ROS"
93: for I=1 to 10
94: red "sg",R$
95: wait W
96: dsp R$:wait 1e3
97: next I
98:
99: "ID?":
100: wait W
101: wrt "sg","ID?"
102: wrt 0,"ID?"
103: wait 1e3
104: osb "ROS"
105: for I=1 to 2
106: red "sg",R$
107: wait W
108: dsp R$
109: wait 1e3
110: next I
111:
112: "HELP?":
113: wrt "sg","HELP?"
114: wrt 0,"HELP?"
115: wait 1e3
116: osb "ROS"
117: for I=1 to 3
118: red "sg",R$
119: dsp R$:wait 1e3
120: next I
121:
122: dsp "END of ROUTINE":beep:stp :gto +0
123:
124: "Read":
125: wait W
126: red "sg",R$
127: wait W
128: red "sg",R$
129: dsp "Press CONTINUE for READ string":stp
130: dsp R$:stp
131: ret
132:
133: "SELECT":
134: dsp "SELECT USER KEY or CONTINUE":stp :ret
135:
136: "ROS":
137: ros(7))A:wait W
138: if bit(2,A)=0:gto +2
139: if bit(6,ros(702)):wait W:gto -3
140: ret
141:
142: "KEY LIST":
143: "f0:  FRQ":
144: "f1:  LVL":
145: "f2:  MOD":
146: "f3:  RTE":
147: "f4:  MOD OFF":
148: "f5:  RF":
149: "f6:  SET?":
150: "f7:  ID?":
151: "f8:  HELP?":
*25221
```

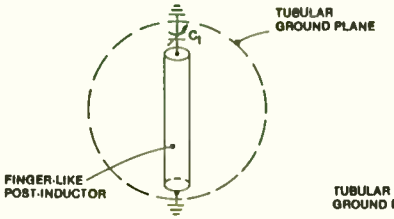


FIG. 1A

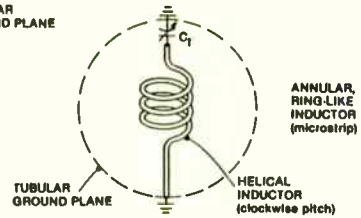


FIG. 1B1

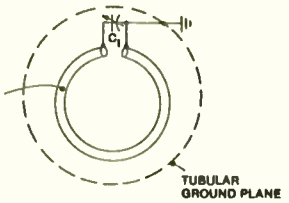


FIG. 1C

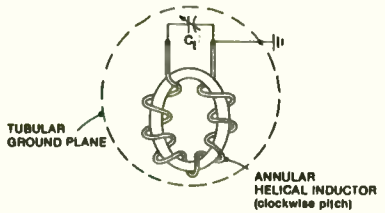


FIG. 1B2

FIG. 1 SOME OF THE POSSIBLE INDUCTIVE ELEMENT PHYSICAL CONFIGURATIONS THAT MAY BE USED IN A ROUND-TUBULAR GROUND PLANE HOUSING.

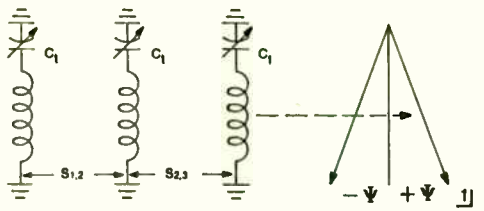


FIG. 2A1: HELICAL COMBLINE
NOTE: Pitch and Sense is also a considered variable as well as Helix Diameter and S: Spacing

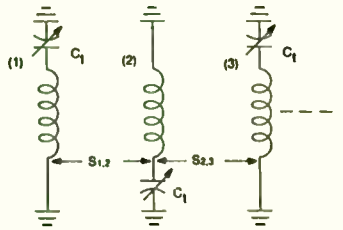


FIG. 2A2: HELICAL, INTERDIGITATED
(See Note: FIG. 2A1)

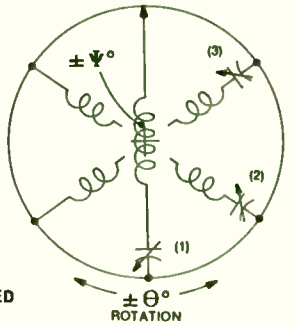
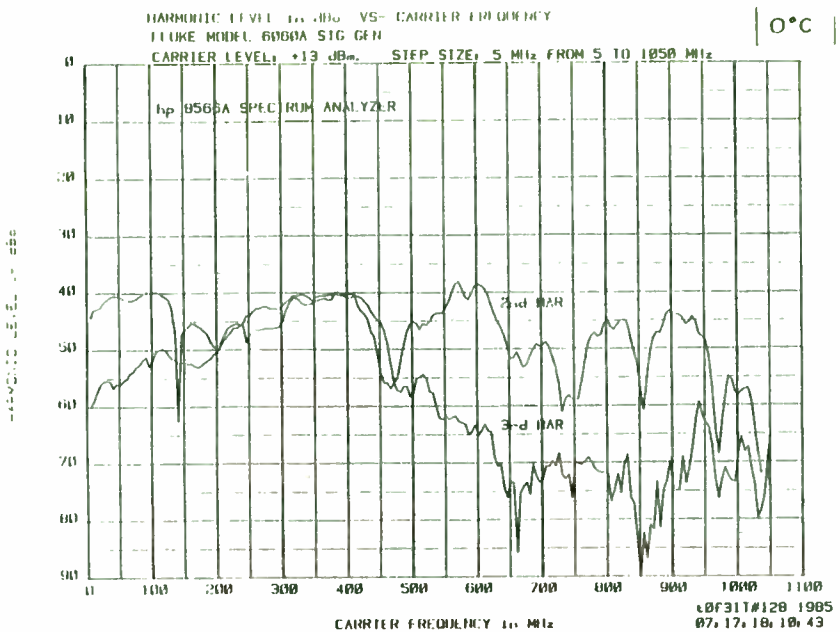
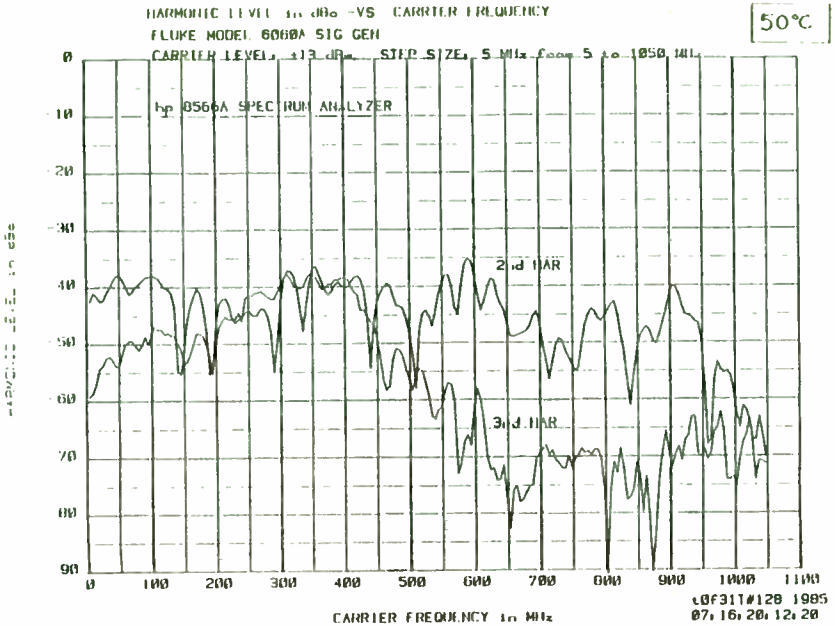
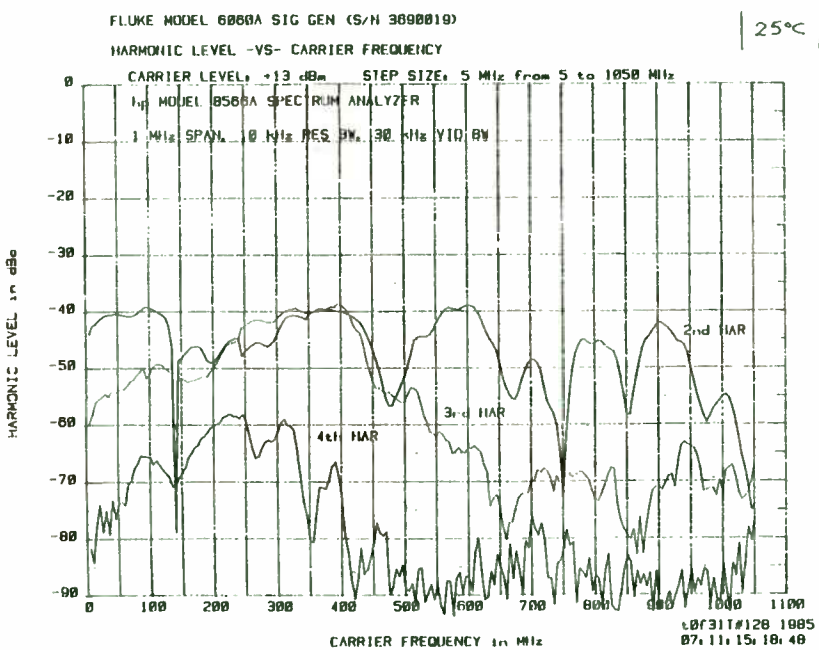


FIG. 2A3
HELICAL, ROTATION COUPLED

SOME POSSIBLE TYPES OF INDUCTIVE ELEMENT ARRAYS THAT MAY BE USED IN A ROUND TUBULAR GROUND PLANE: Θ and Ψ ROTATION FOR FIGS. 2A & 2B AND Θ, Ψ AND ϕ FOR ANNULAR RING, TOROIDAL HELIX RING: REF. 2B2: TO THESE MAY BE ADDED VARIOUS COUPLING STRUCTURES FOR ADDITIVE/SUBTRACTIVE INTERFERENCE 1] Angle Ψ applies to all Figure 2 drawings.







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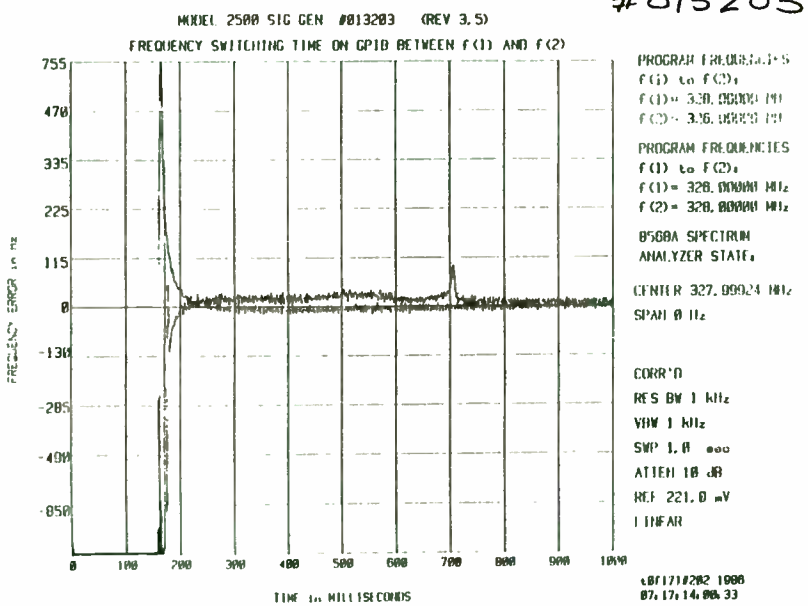

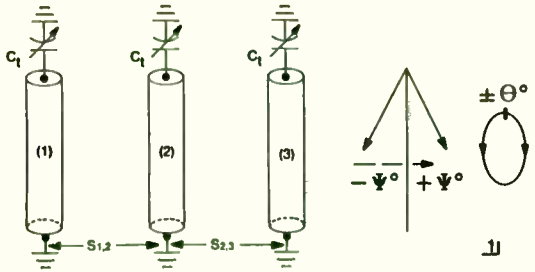

FIG. 2B1: POST/FINGER COMBLINE

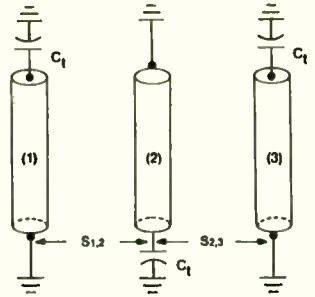

FIG. 2B2: POST/FINGER, INTERDIGITATED

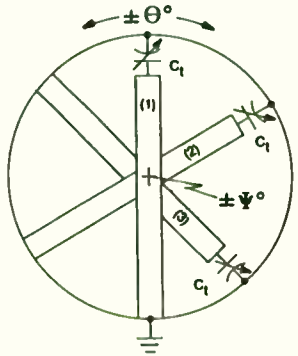

FIG. 2B3: POST-ROTATION COUPLED

SOME POSSIBLE TYPES OF INDUCTIVE ELEMENT ARRAYS THAT MAY BE USED IN A ROUND TUBULAR GROUND PLANE: Θ and Ψ ROTATION FOR FIGS. 2A & 2B AND Θ, Ψ AND ϕ FOR ANNULAR RING, TOROIDAL HELIX RING: REF. 2B2: TO THESE MAY BE ADDED VARIOUS COUPLING STRUCTURES FOR ADDITIVE/SUBTRACTIVE INTERFERENCE 1 Angle Ψ applies to all Figure 2 drawings.

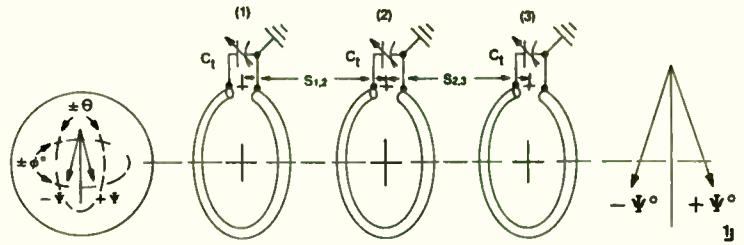

FIG. 2C1: ANNULAR RING, COMBLINE
NOTE: Rings have an added degree of freedom in $\pm\phi°$ rotation angle

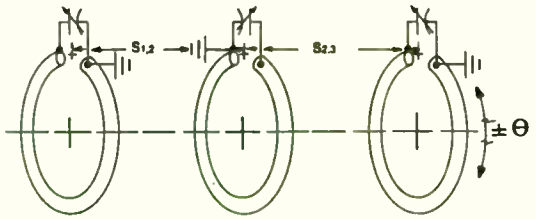

FIG. 2C2: ANNULAR RING - INTERDIGITATED

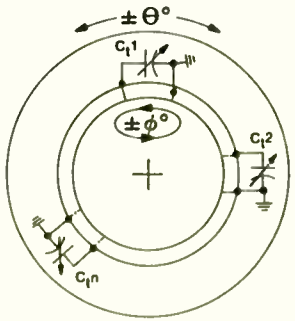

FIG. 2C3: ANNULAR RING, ROTATION COUPLED

NOTE: The Helical Ring Toroidal Inductor Array is left to the imagination of the reader, Ref. FIG. 1B2

SOME POSSIBLE TYPES OF INDUCTIVE ELEMENT ARRAYS THAT MAY BE USED IN A ROUND TUBULAR GROUND PLANE: Θ and Ψ ROTATION FOR FIGS. 2A & 2B AND Θ, Ψ AND ϕ FOR ANNULAR RING, TOROIDAL HELIX RING: REF. 2B2: TO THESE MAY BE ADDED VARIOUS COUPLING STRUCTURES FOR ADDITIVE/SUBTRACTIVE INTERFERENCE 1 Angle Ψ applies to all Figure 2 drawings.

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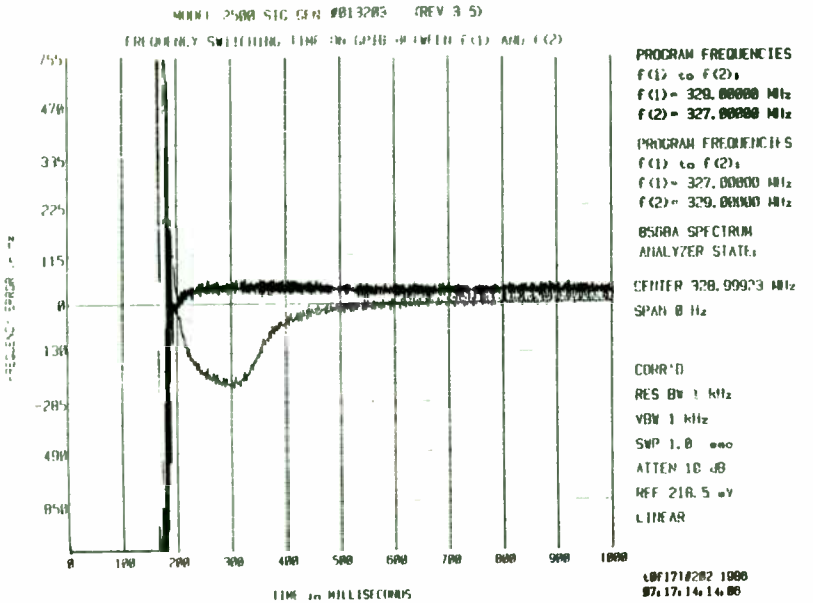
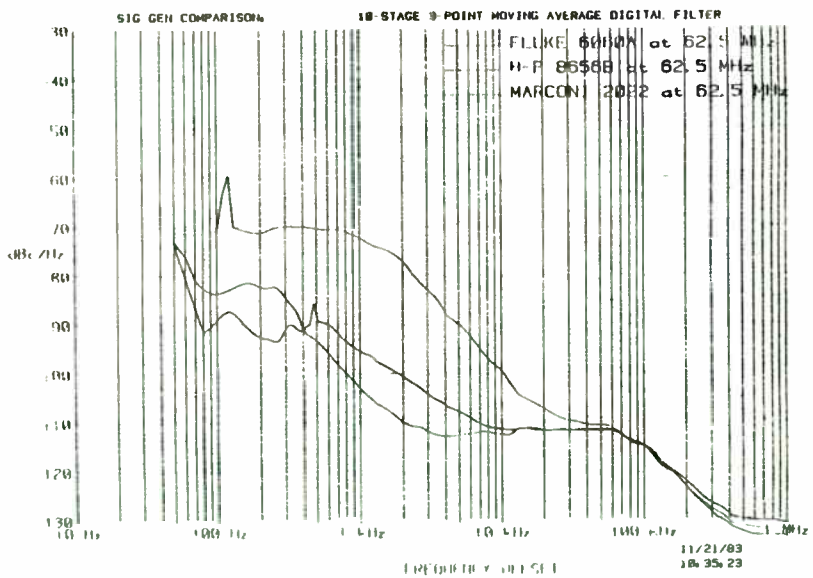
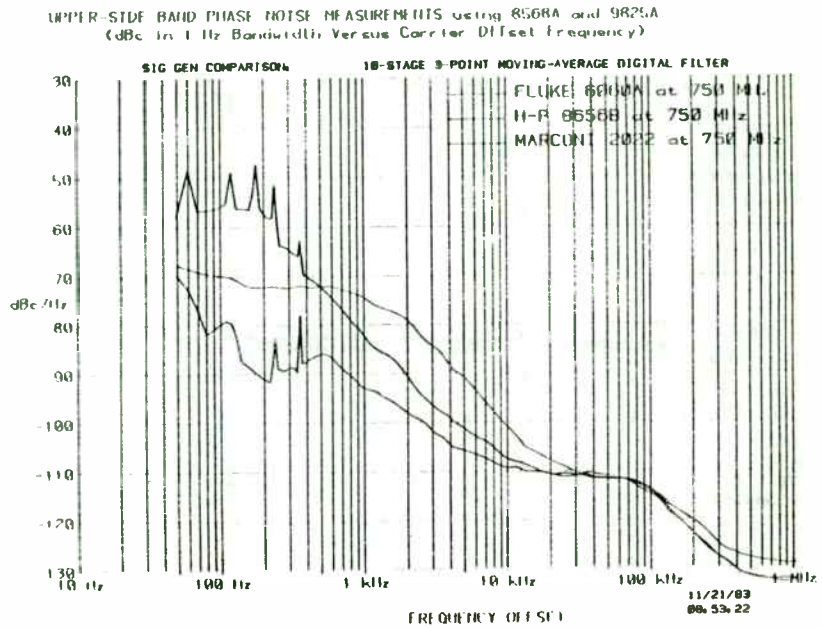






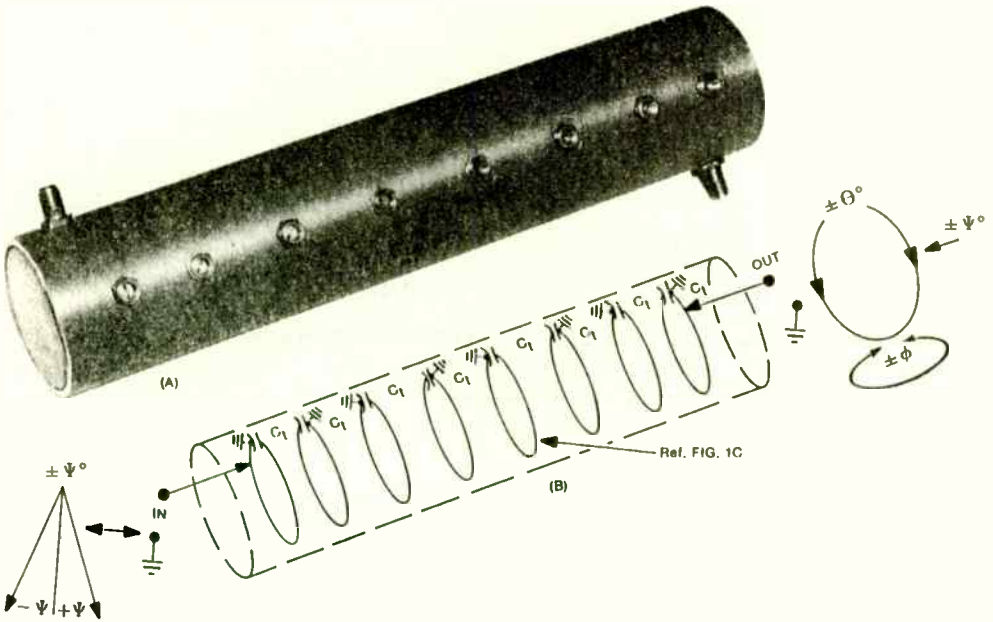
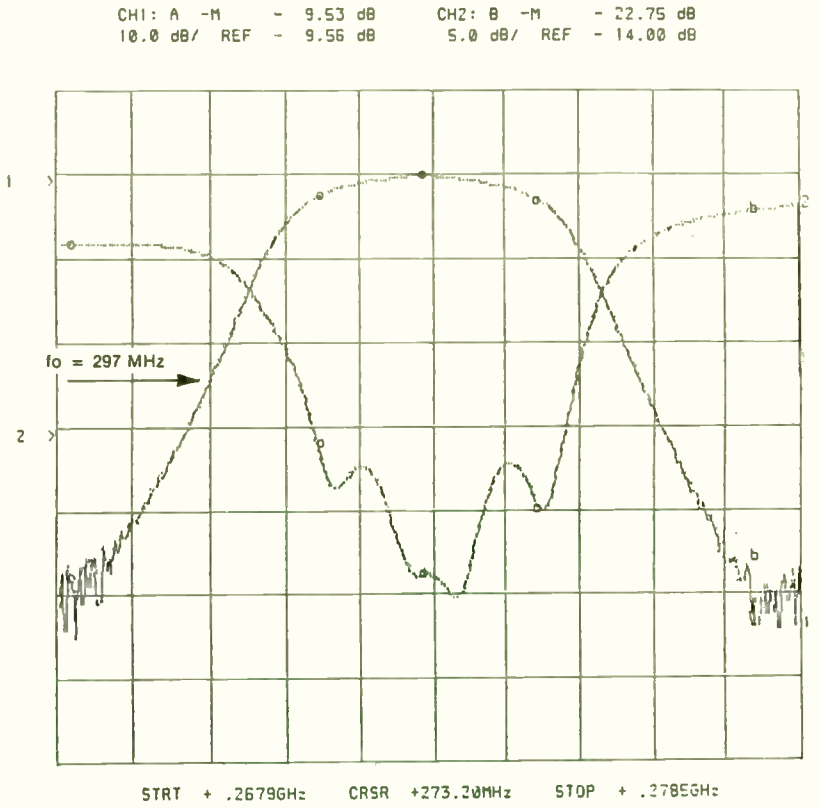


FIG. 3 A: PHOTO; B: SCHEMATIC FOR 8 RESONATOR, INTERDIGITATED ANNULAR RING, TUNABLE BANDPASS FILTER;

RANGE = 300 > 600 MHz.



NARROW SWEEP BAND

FIG. 3C

OOK, FSK, and PSK Data Receivers Using an AM-FM Receiver IC

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HCR Box 110, Pulpit Rock Road
South Woodstock, CT 06267

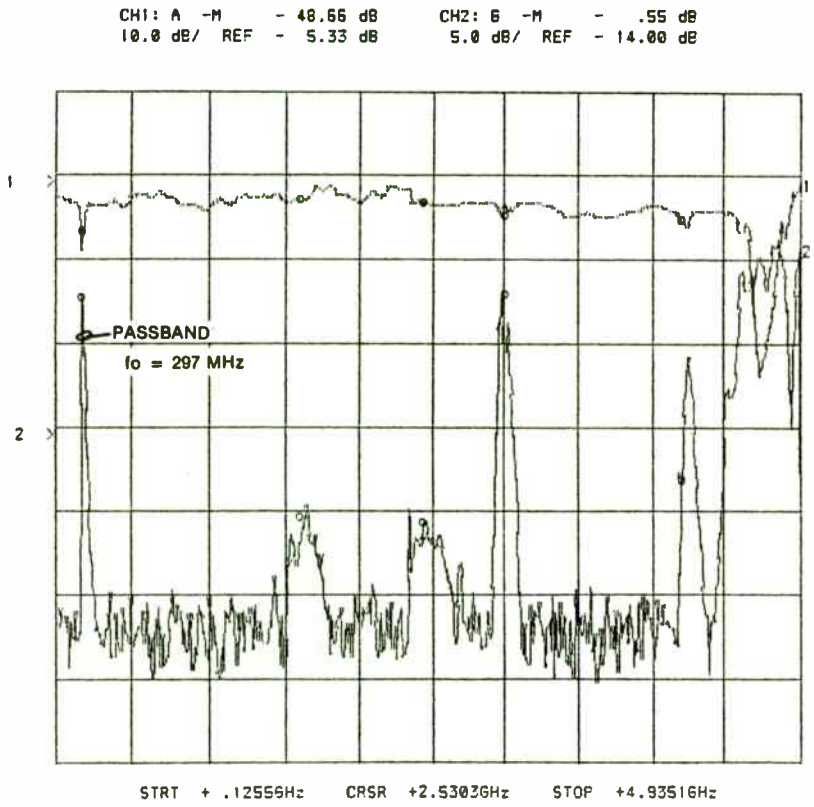
Abstract

The Sprague ULN2241A and ULN3840A ICs are designed to be used in consumer AM-FM radios. They contain all the necessary functions for a complete AM tuner plus the FM IF and detector. With a few simple changes in the recommended circuitry, they can be used in a wide variety of low cost crystal controlled or synthesized OOK (carrier is amplitude modulated or turned on and off by the data), FSK (carrier is shifted in frequency by the data), and PSK (carrier is shifted in phase by the data) data receivers. The range of data rates is almost unlimited because the IF frequency is not limited to 455 kHz and the inclusion of an internal mixer and regulated supply means that in many cases, the complete unit can be built with a few coils and an unregulated supply.

ULN2241A and ULN3840A

Block diagrams of the ULN2241 and ULN3840 are shown in Figures 1 and 2 respectively. The two ICs are essentially identical in performance except that the latter has more features and therefore more pins. The one exception is that the ULN2241 provides an AGC output from pin 10 in the FM mode which goes from 5V to 0 as the input signal increases. The ULN3840, on the other hand has a DC output from pin 15 which increases with the input signal level and goes from 0 to about 4 volts in both the AM and FM modes. Other features unique to the ULN3840 are an AFC output, a mute signal, and a mute input pin.

Typical radio receiver circuits using these two ICs are shown in Figures 3 and 4. Note that the complete AM tuner is contained in the IC and only the tuned circuits need to be added. The AM local oscillator is a negative resistance type and is internally connected to a low-noise balanced mixer. A very important feature of the ICs is that the AM and FM IF amplifier are common and use the same transistors. Each stage of the IF amplifier is down 3 dB at about 30 MHz, and there are four stages. This differs from most combination radio IC's which have different IF sections for AM and FM and the AM section is usually designed not to have much gain above 455 kHz. Since they are common in the ULN2241 and ULN3840, the IF out pin is common for both modes and the detector coils must be connected to feed the FM and AM detectors. In this application, the AM detector coil is a short circuit in the FM mode, and the 22 uH coil feeds the FM quadrature detector coil. Because a quadrature detector is a phase detector with one input connected internally to the IF output and the other connected to the quadrature coil, it can also be used, as we shall see later, as part of a phase



WIDE BAND SWEEP TO 14.9 GHz

FIG. 3D

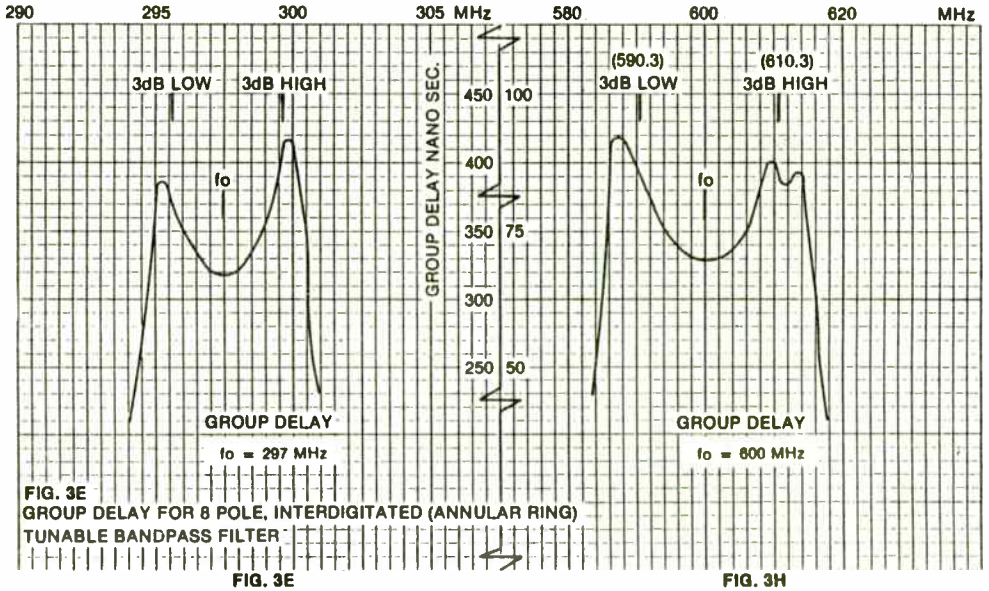


FIG. 3E
GROUP DELAY FOR 8 POLE, INTERDIGITATED (ANNULAR RING)
TUNABLE BANDPASS FILTER

FIG. 3E FIG. 3H

detector in both FSK and PSK demodulation.

The frequency range of operation of the mixer is from audio up to about 100 MHz and although the mixer is designed to work only in the AM mode, it can be turned on in the FM mode by connecting a bias resistor from the reference voltage to the mixer bias pin (12 on the ULN2241 and 15 on the ULN3840). The mixer works quite well at 100 MHz if a buffered signal is fed to the oscillator input port, and it will handle input signals up to about 30 mV without significant crossmodulation, but in the AM mode the internal oscillator gives up at about 30 MHz. A stable internal regulated voltage is available from pin 9 on the 2241 or 13 on the 3840. If this voltage is used for other circuits in the receiver which require a regulated voltage like an oscillator, then the unit can be built to operate from an unregulated supply. (The current drawn from the regulator should not be more than about 2 mA.) The input impedances to the mixer and IF amplifier are quite high at the lower frequencies, and so it is possible to accommodate a wide variety of RF or IF filters.

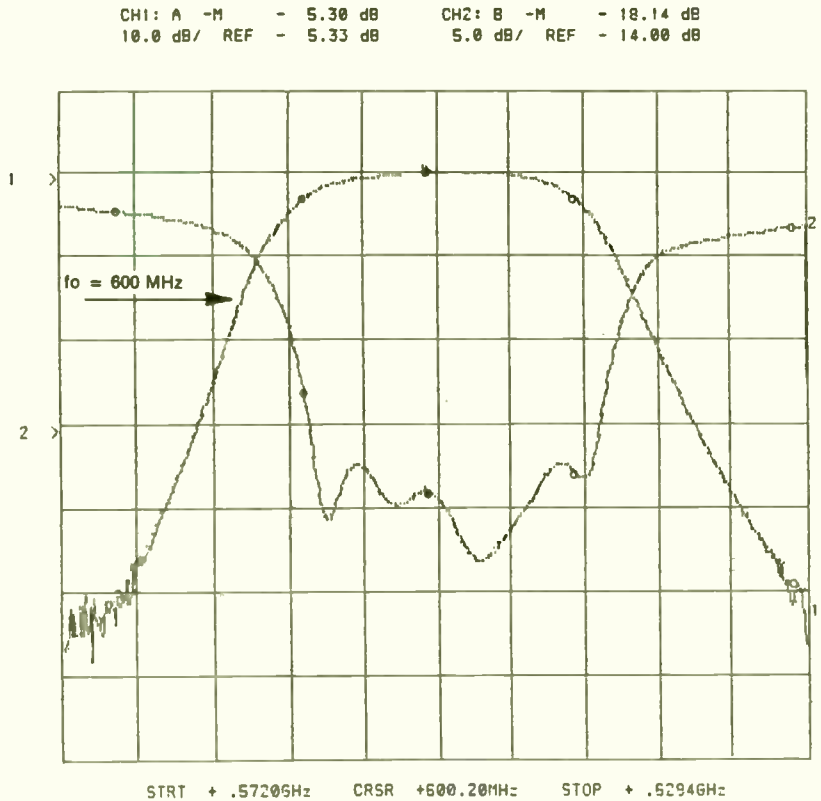
The mute output pin of the ULN3840 can be used to drive the internal mute when in the FM mode so that noise is not present at the output when no carrier is being received. It can also be set up to mute if there is a tuning error and the mute signal could also be fed to the data processing circuits to indicate a loss of carrier or a signal too small for reliable reception.

OOK Data Receivers

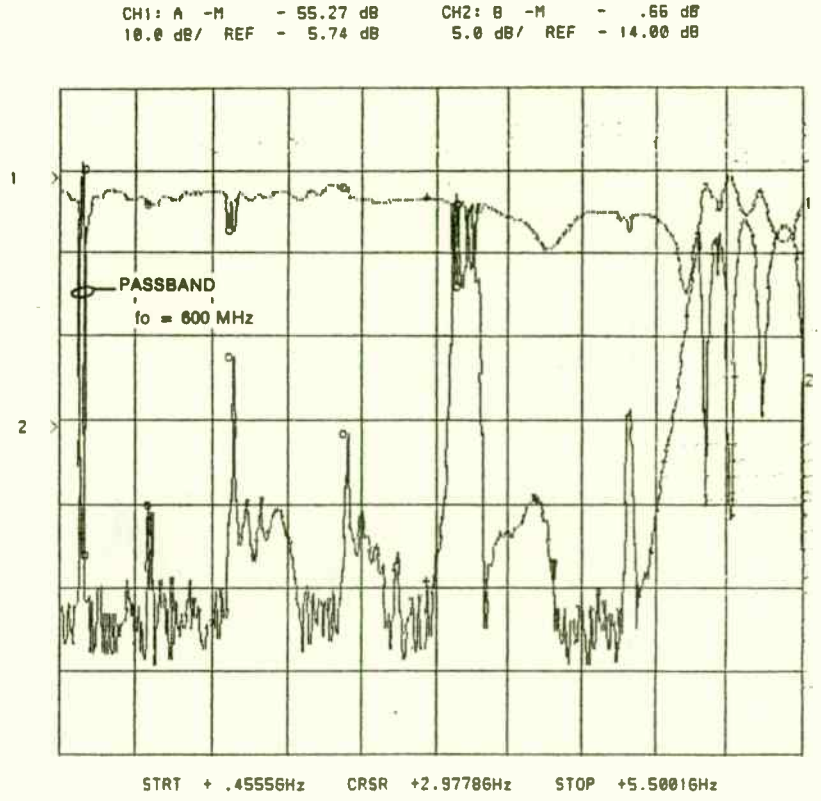
Personally, I do not like the term OOK because the carrier may not be completely off because of leakage. AM seems to be a more appropriate term with the ON/OFF ratio being specified.

AM modulation is not used very often in data transmission, because of claimed susceptibility to errors, but this seems to be grounded in the belief that AM radio has more static than FM. In fact, AM requires a S/N (power ratio) of only about 18.5 dB for a BER of 10E-9 (1). AM is also very easy to generate by simply gating the RF signal on and off, and it occupies much less bandwidth than FSK. A 20 dB S/N is not difficult to guarantee in cable systems and bandwidth might be an important factor in these cases. (2) The only restriction here is that the receiver IC has an internal AGC system, so it is better to operate the system with the carrier normally on and the data signals turning it off. The number of data signals in succession which turn the carrier off must be limited depending on the time constant selected for the AGC or the IC gain will increase until it reaches its maximum gain condition.

Figure 5 shows a 14.5 MHz AM data receiver using a crystal controlled external oscillator. The AM local oscillator coil is replaced by a 100 Ohm resistor to prevent it from oscillating due to the internal negative resistance. The IF



NARROW BAND SWEEP
FIG. 3F



WIDE BAND SWEEP TO 14.9 GHz
FIG. 3G

frequency in this case is 4.5 MHz and was selected as a compromise between image rejection and available coil Q to produce the desired IF selectivity. Note that the internal detector has not been used here. This is because the data rate for this receiver is up to 38 KBPS and the internal detector is designed for audio use. At lower data rates, the internal detector can be connected to an external comparator. Other possibilities might be a diode detector and comparator.

The AGC time constants are set by the capacitors on pins 16 and 12 with the one on pin 16 being the most important. If the carrier is always on and long strings of data are to be sent, the capacitor on pin 16 can be made larger. If fast attack for the AGC is desired, it can be made smaller.

If higher data rates are desired, a wider bandwidth filter can be used. A 10.7 MHz ceramic FM IF filter will allow data rates up to about 140 KBPS. If the data rates are low, a 455 kHz IF can be used but this may require dual conversion to achieve the desired spurious response rejection.

It should be pointed out that the occupied bandwidth of AM data signals is only two times the data rate. The occupied bandwidth of FSK signals is approximately 2(data rate)+ 2(frequency shift) so that this data receivers which can handle 140 KBPS in the AM mode would handle only about 65 KBPS in an FSK mode with a frequency shift of 75 kHz.

FSK Data Receivers

Grounding pin 16 of the ULN2241 or 1 of the ULN3840 puts it into the FM mode. As was mentioned above, the mixer is off in this mode, but as was mentioned earlier, it can be turned on by connecting a resistor from the reference voltage to the mixer bias pin. In the ULN2241, this resistor can instead be connected to the AGC voltage on pin 10 so that the mixer gain is reduced as the signal level increases. Figure 6 shows a 49 MHz FSK receiver using an external crystal oscillator and comparator to produce the output pulses. Unlike in the AM case, there is no limit on how long the data can stay in the 0 or 1 state. This particular data receiver uses a 10.7 MHz FM receiver IF filter and will operate up to about 50 KBPS. Current 10.7 MHz FM receiver IF filters such as the Murata SFE 10.7 ML or Toko CFSD have excellent group delay response and cause very little pulse distortion.

The FM detector is a standard quadrature detector and when it is correctly tuned at the center frequency, the output from pin 5 is the same DC voltage as the reference voltage on pin 9. In the ULN3840, the AFC output pin can also be used if a load resistor is connected from pin 7 to pin 13. The reference voltage can then be used as the other input to the comparator.

An alternative to this arrangement is, of course, the Motorola MC 3356 which has been specifically designed as an FSK data receiver.

FIG. 4A

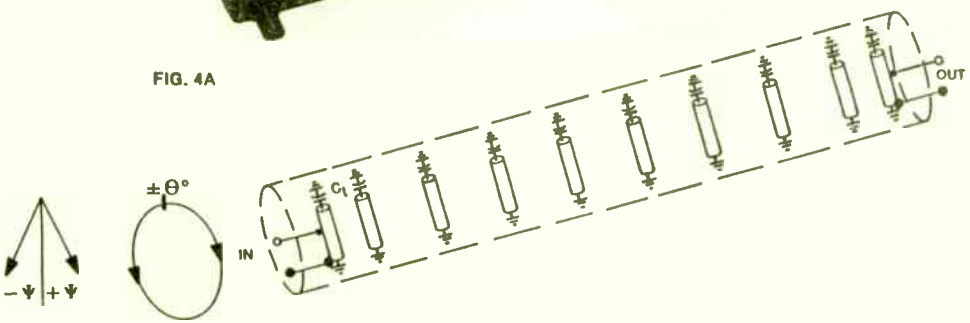
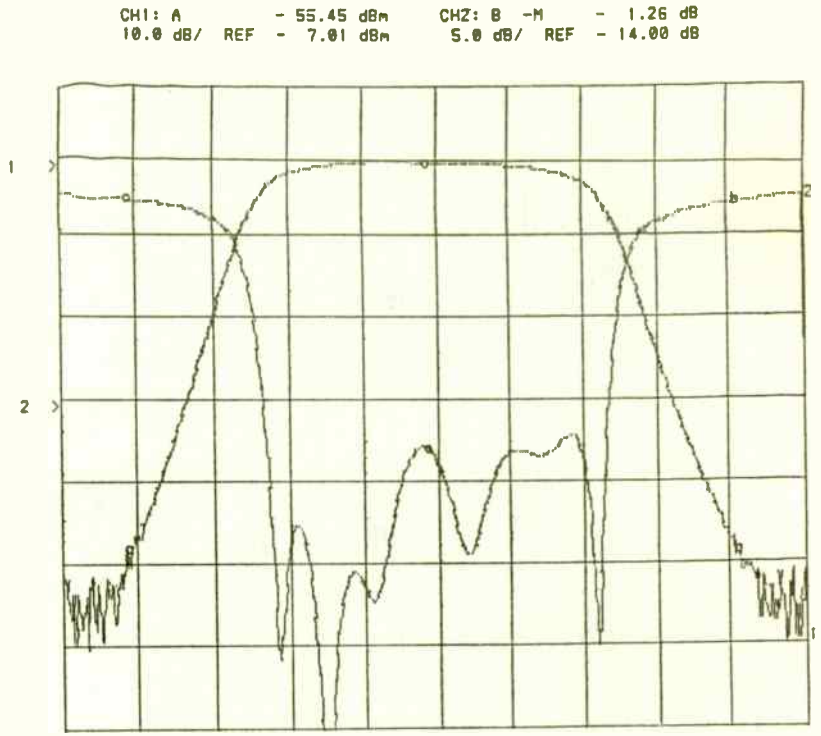


FIG. 4B

FIG. 4: A = PHOTO, B = SCHEMATIC FOR 10 RESONATOR COMBLINE (POST) BANDPASS FILTER RANGE: 3 > 8 GHz. 3dB BW : 2.5%



PASSBAND SWEEP, fo = 2.7 GHz

FIG. 4C

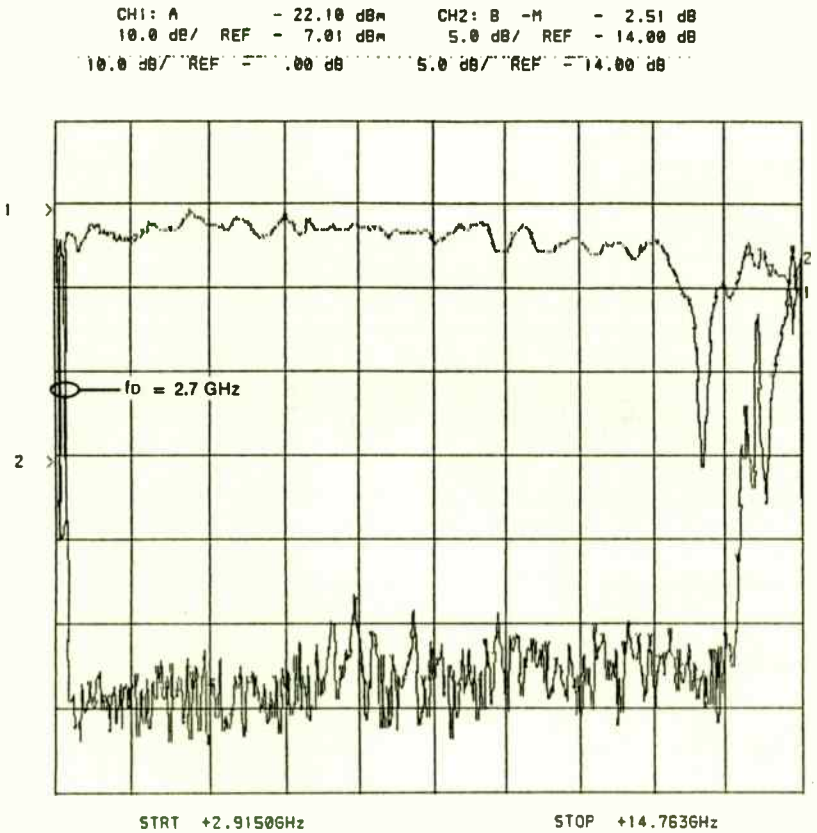
PSK Data Receivers

PSK modulation is capable of low error rates in the presence of noise (1) and occupies a bandwidth only equal to twice the data rate (6), but the circuitry is complex and there are restrictions on the data format because of the phase ambiguity problem. One solution for polled systems was mentioned in another paper (4) and other schemes are presently used for telephone data receivers. (Polled systems are those in which a number of receivers are polled in sequence.) The most common solution for RF data receivers is to use a phase-locked-loop with a very narrow bandwidth for demodulation. In any case, the ULN2241 and ULN3840 have many of the necessary components for constructing the loop (3). Figure 7 shows a PSK demodulator which uses the phase detector in the ULN2241 for the loop and an external MC1496 phase detector to detect the 180 degree phase changes. The VCO locks up at 90 degrees from the signal at the IF output on pin 8 of the ULN2241, and the IF output is shifted 90 degrees by T10 and applied to the MC1496. Thus the ULN2241 contains the Q detector and the MC1496 the I detector. The output of the I detector is fed through a low-pass filter to a comparator to produce the output data.

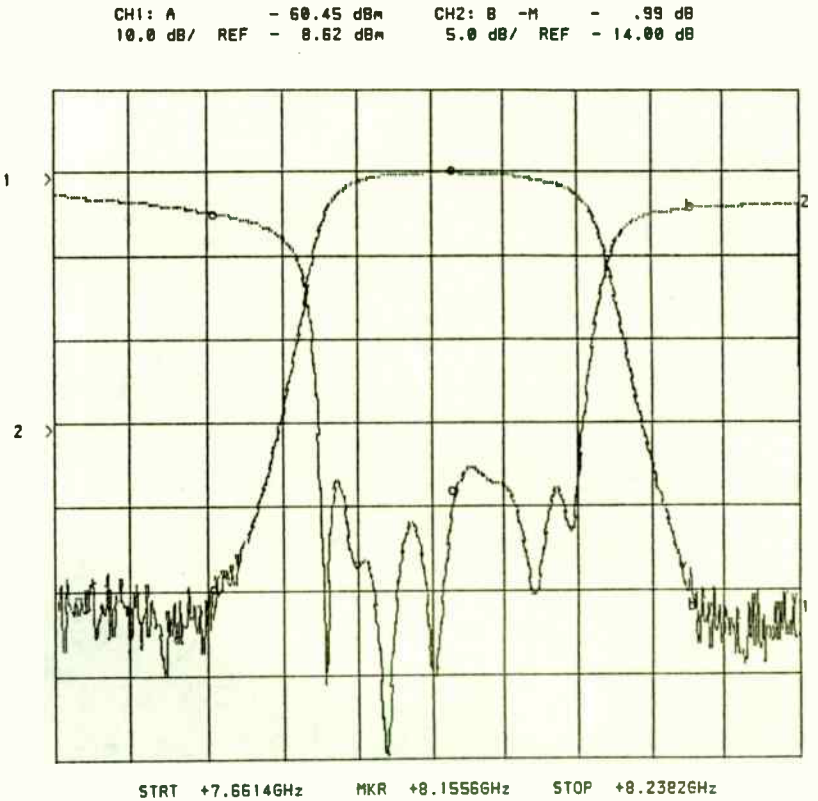
The Q or loop phase detector consists of the quadrature detector components in the IC, and the audio output pin, pin 5, is the phase detector output. The phase detector constant for the ULN2241 and ULN3840 is 3.8 volts/radian. The internal impedance at the audio output pin is about 900 ohms so R1 is added together with R2 and C to form a passive loop filter. If the ULN3840 is used instead, the AFC output could be used, and the load resistor from pin 7 to 13 could be R1 of the loop filter. The AFC output is a current source with a detector constant of about 700 uA/radian. The oscillator constant, Ko, for this circuit is 577e3 radians/sec/volt, so the loop frequency of this design is 1 kHz.(5) This is a relatively narrow band loop, but it still will have a problem with data pulses over about 200 microseconds long;(5) When the carrier changes phase 180 degrees, the loop tries to follow it, and if the carrier stays at 180 degrees long enough , the VCO will lock on to the 180 degree carrier. If the VCO changes only 90 degrees, the role of the two phase detectors is reversed and the data will be lost. Thus, the length of the data pulses must be restricted or some means must be found to accommodate longer ones. A common solution is to build a very narrow-band loop and use a crystal-controlled VCO to keep it very close to the center frequency so that lock-up can be achieved in a reasonable length of time.

Conclusion

It has been shown that low-cost RF data receivers can be built with integrated circuits commonly used for consumer AM/FM radios, and their operating frequencies are not limited to the broadcast frequencies. Almost any range of data rates and type of modulation can be accommodated, and in many



WIDE BAND SWEEP TO 14.9 GHz
FIG. 4D



PASSBAND SWEEP fD = 8.15 GHz
FIG. 4E

cases, very few external components are required. In particular, the Sprague ULN2241A and ULN3840A are exceptionally good for this application because of the wide frequency response of their internal mixer and IF stages and features like AGC drive, signal strength indication and mute input and output.

Figure 1 ULN2241A

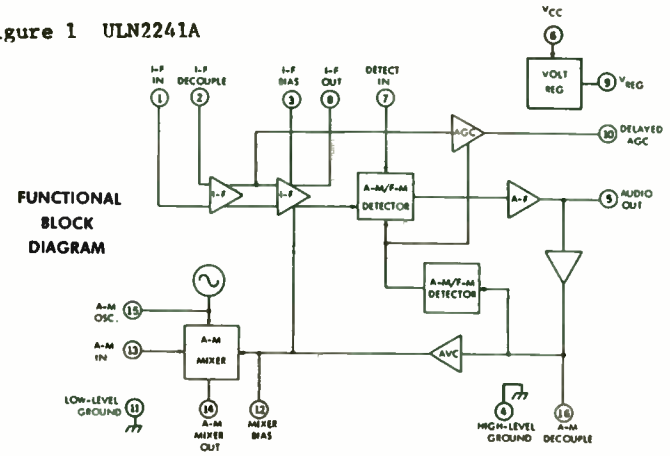
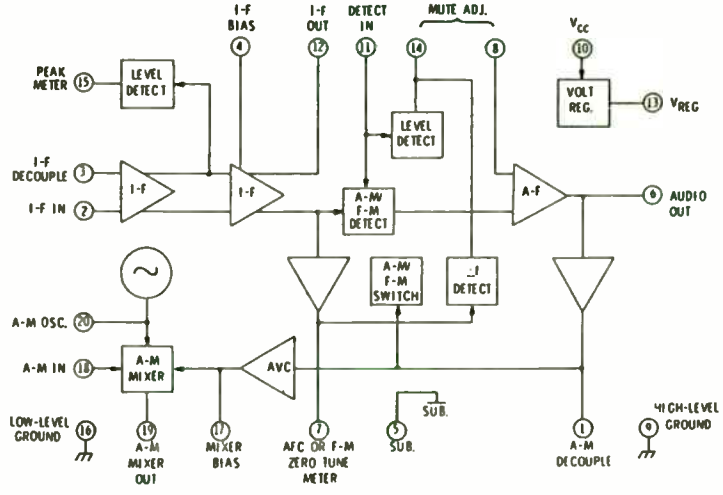


FIGURE 2 ULN-3840A



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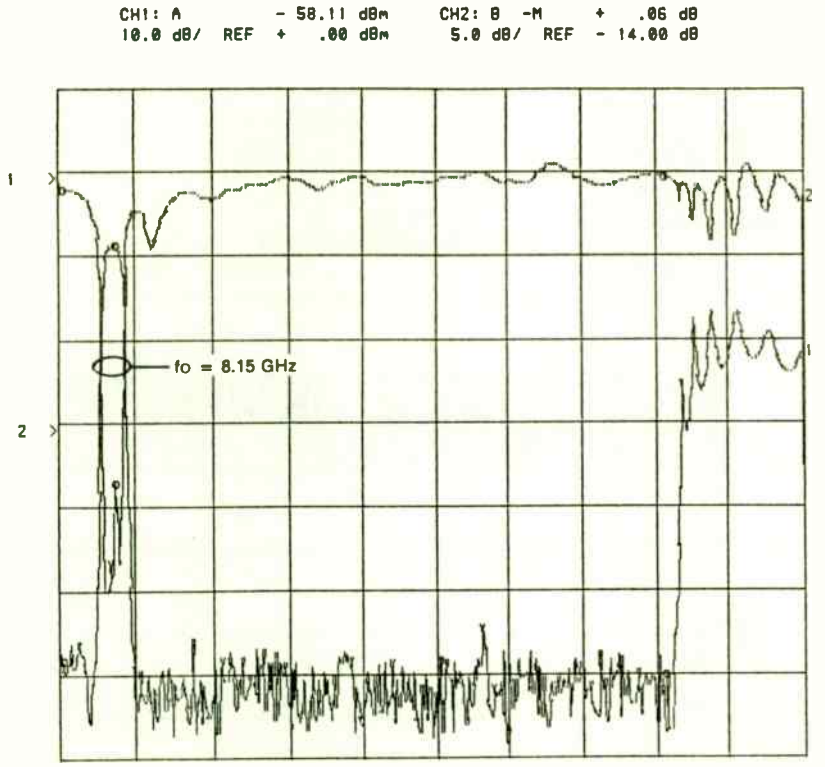
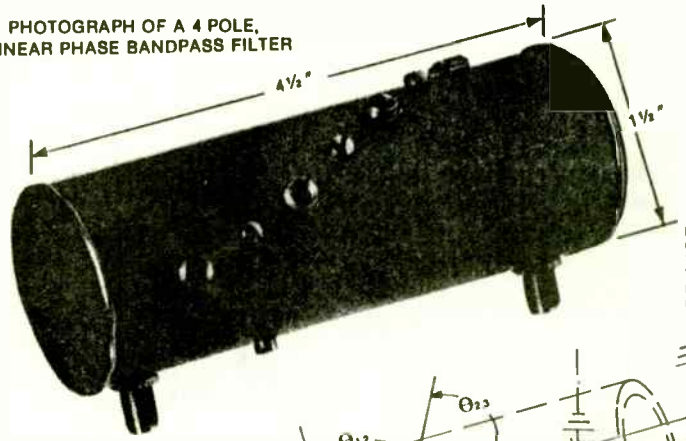
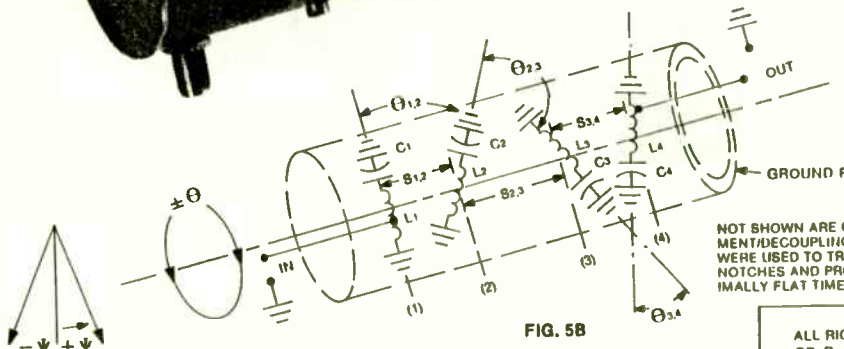


WIDE BAND SWEEP TO 14.9 GHz
FIG. 4F

FIG. 5A = PHOTOGRAPH OF A 4 POLE, 2 ZERO LINEAR PHASE BANDPASS FILTER



K_{123} COMPLEX COUPLING COEFFICIENT FROM RESONATORS (1) TO (2) TO (3) TO (4) MAY BE MODIFIED BY THE MUTUAL COUPLING FROM RESONATOR (1)-(3) AND THE INTRODUCTION OF COUPLING-ENHANCEMENT AND/OR DECOUPLING ELEMENTS-ETC.



NOT SHOWN ARE COUPLING ENHANCEMENT/DECOUPLING ELEMENTS WHICH WERE USED TO TRIM ATTENUATION NOTCHES AND PROVIDE NEARLY MAXIMALLY FLAT TIME DELAY, SEE FIG. 5C.

FIG. 5B

FIG. 5B SCHEMATIC-CONCEPT OF A: (W-S^3 / Θ, Ψ, ϕ, P) TUNABLE BANDPASS FILTER
S = SPACING; Se: WINDING SENSE (HELICAL COILS): $S\mathring{e}$, $S\bar{e}$: (CW, CCW)
$\pm\Theta_{i,i+1}$: ROTATION ANGLE BETWEEN ADJACENT INDUCTORS
$\pm\Psi_{i,i+1}$: YAW ANGLE FROM NORMAL MAJOR z AXIS OF ADJACENT ELEMENTS
$\pm\phi_{i,i+1}$: TWIST ANGLE (ANNULAR INDUCTORS) BETWEEN ADJACENT ELEMENTS
P: PITCH OF WINDINGS

PATENT APPLIED FOR

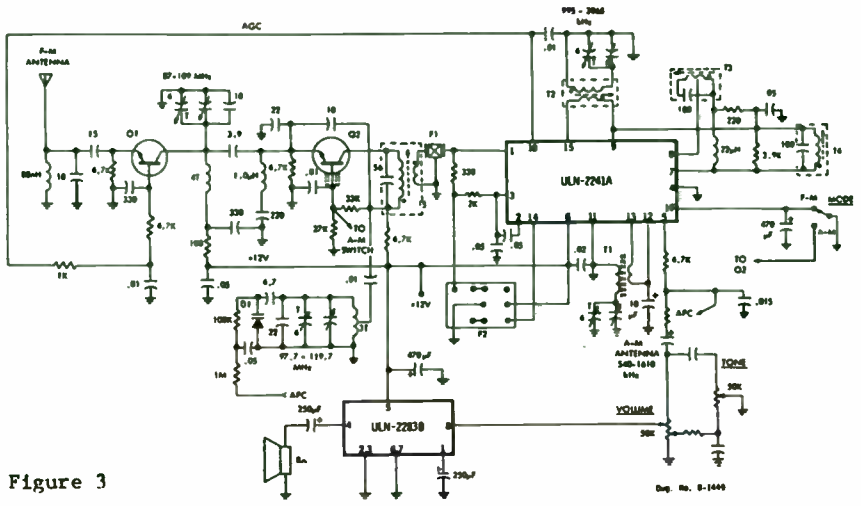


Figure 3

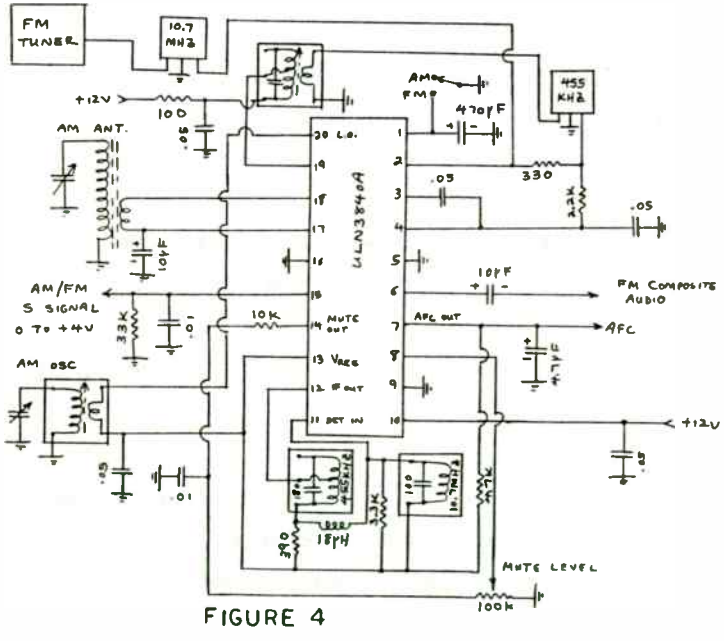
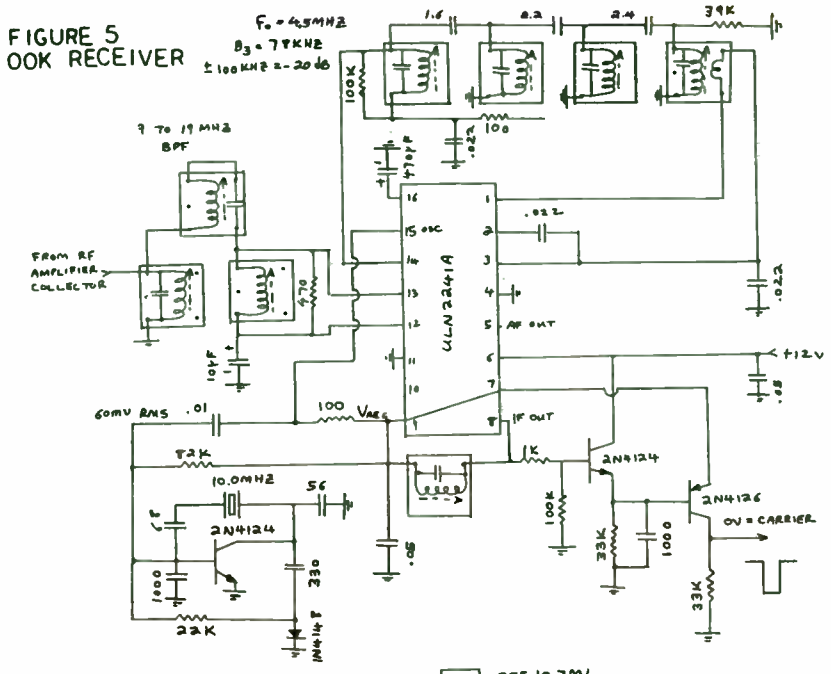


FIGURE 4



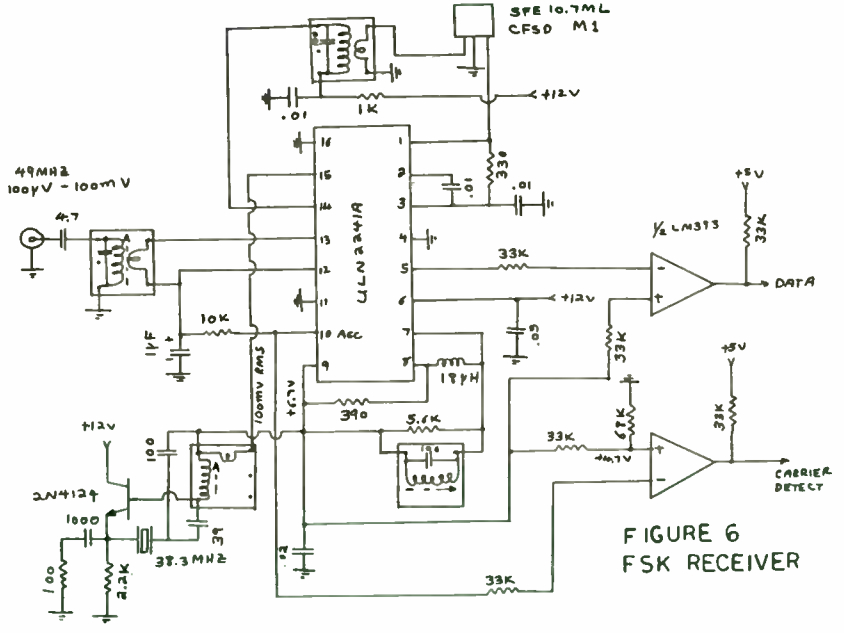
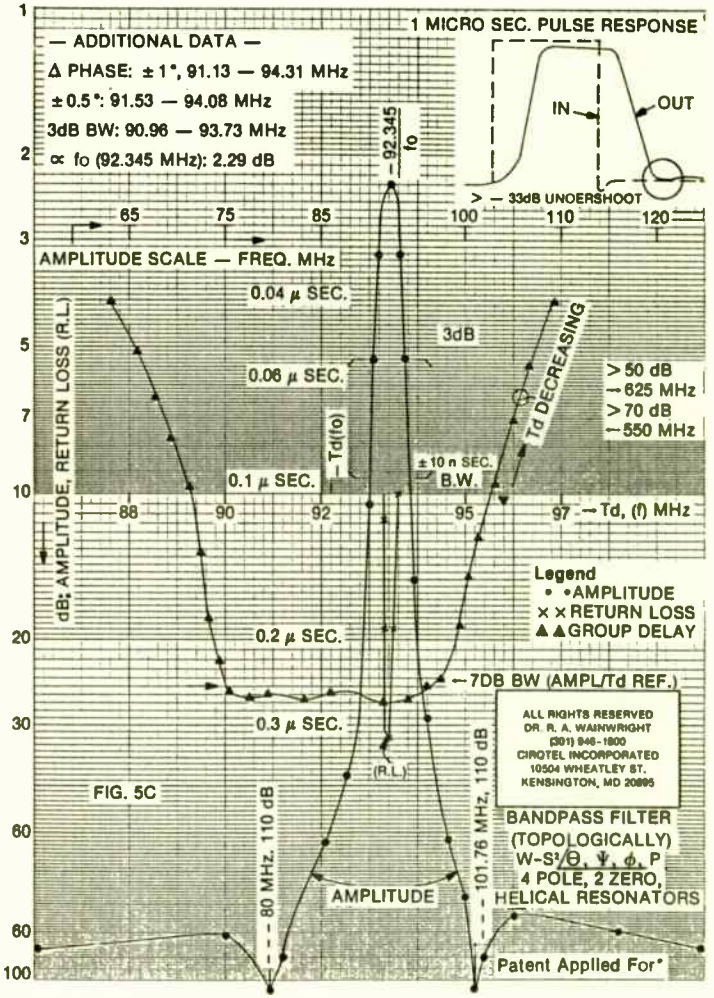


FIGURE 6
FSK RECEIVER



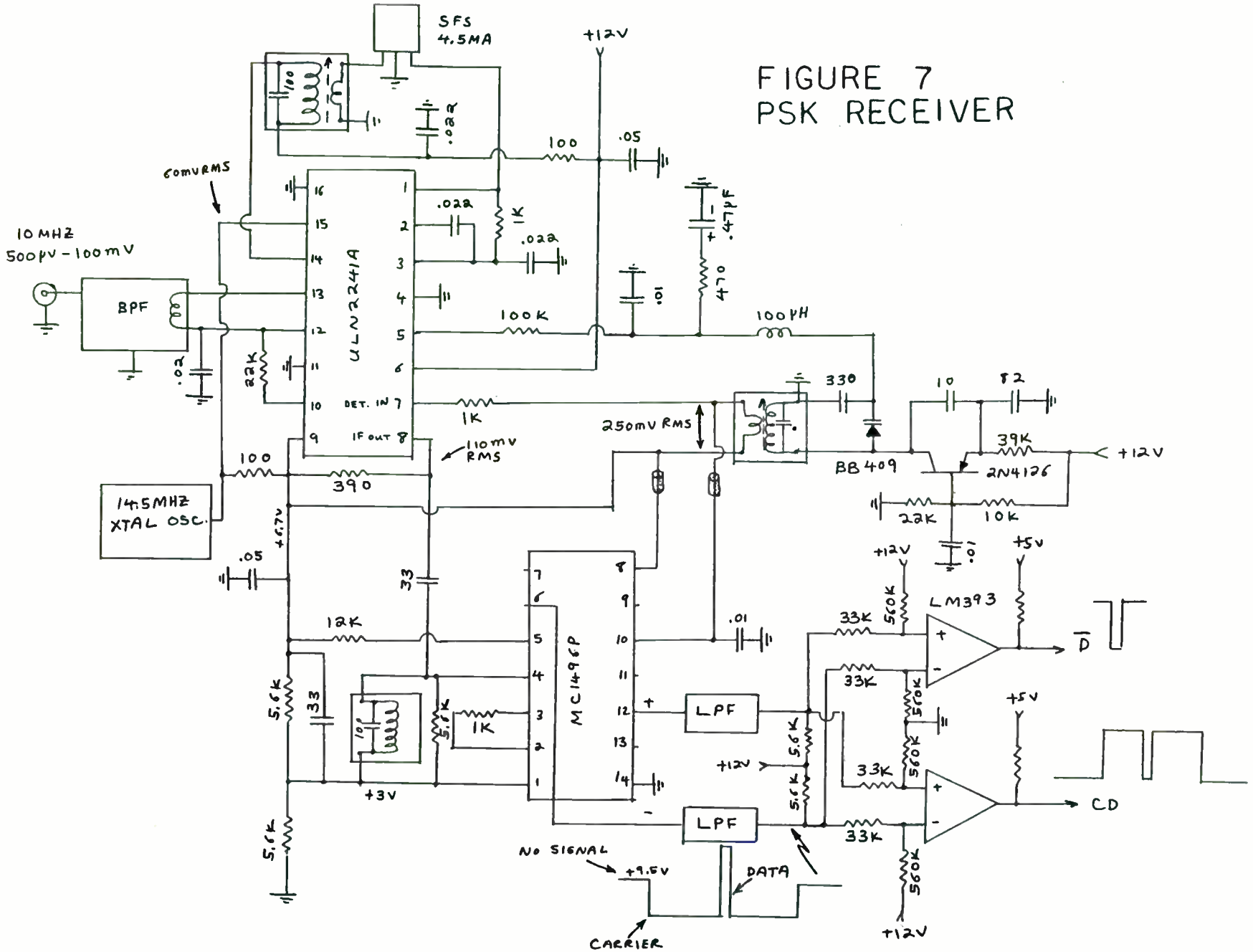


FIGURE 7
PSK RECEIVER

The PIN Diode - Uses and Limitations

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ABSTRACT

The PIN diode is a useful element in the design of attenuators, switches, and modulators. Under ideal conditions the diode acts as a current controlled resistor. However, there are limitations on performance related to frequency and power.

This paper covers some of the low frequency and high frequency limitations of PIN diode applications and factors determining these limits. Other topics are diode parameters that control resistance and power limitations on attenuator performance.

INTRODUCTION

The PIN diode is a three layer device (figure 1) - an intrinsic high resistance I layer in the center with conducting P and N layers on either side. The conducting layers are formed by adding impurities to produce an excess of positive charges on one side and an excess of negative charges on the other. Diode resistance can be controlled by DC bias voltage. Both positive and negative charges injected into the I layer lower its resistance. Diode resistance is approximately proportional to the inverse of the current.

Ideally PIN diode resistance is controlled by the DC current and independent of the RF power level. However, at high power levels the charge in the I layer may vary at the carrier frequency. In attenuator applications this variation in diode resistance is responsible for distortion. The effect is most severe in absorptive attenuators at low frequencies, with some power also absorbed by diodes in reflective attenuators. Since the amount absorbed depends on the attenuation level, distortion in both types is a function of attenuation.

Most switches are reflective; power is either reflected or passed. Little power is absorbed by the diode so distortion in switches is not a problem. PIN diodes can have a wide range of switching times - from a few nanoseconds to close to a microsecond. The time depends on the combination of forward current for one state and reverse voltage for the other. Switching time is faster in the transition from reverse to forward bias.

Reverse recovery time is related to switching time. Forward current injects charge into the diode, then a reverse pulse removes the charge. Time for recovery to a low value of current is defined as reverse recovery time, and depends on the values of forward current and reverse voltage used in the measurement.

In addition to switches and attenuators, PIN diodes can be used as absorptive modulators. The diode resistance is varied at the modulating

A THICK FILM HYBRID TRANSMITTER FOR CELLULAR TELEPHONE

by

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Introduction

Rapidly growing markets of cellular telephones are demanding smaller lighter and cheaper radiotelephones. To fulfill these demands manufacturer have to search new production techniques also for the radio units of the cellular telephones. This paper describes the design and performance of a thick film hybrid transmitter. Thick film technique was selected, because it is cheaper and more suitable for mass-production than thin film technique. The frequency range of the transmitter is from 890 MHz to 915 MHz.

The design of the power amplifier is based on measured S-parameters and large signal impedances of the transistors and equivalent circuits of passive components. The analysis and optimization of the matching circuits was done using computer, because the same work done manually would be an overwhelming task.

Measurement of S-parameters was done using an automatic network analyser. Large signal impedances were measured with conventional pull-load method and equivalent circuits of passive components were measured using HP 4191A impedance analyser and the least squares fitting method.

Properties of class A and B power amplifiers

For power amplifiers , the output current is either in the cutoff region or saturation region during a portion of the input signal cycle. This leads to the classification of power amplifiers into three modes of operation: class A, B and C. When the output current flows during the whole input signal cycle, the amplifier is called class A amplifier. If the output current flows only during the half of the input signal cycle, the mode of operation is B and if the output current flows less than half of the input signal cycle the amplifier is called class C amplifier.

The class of operation of the transistor amplifier has significant effect on available gain and efficiency. Figure 1 shows the variation of efficiency and maximum output power as a function of operation mode and conduction angle.

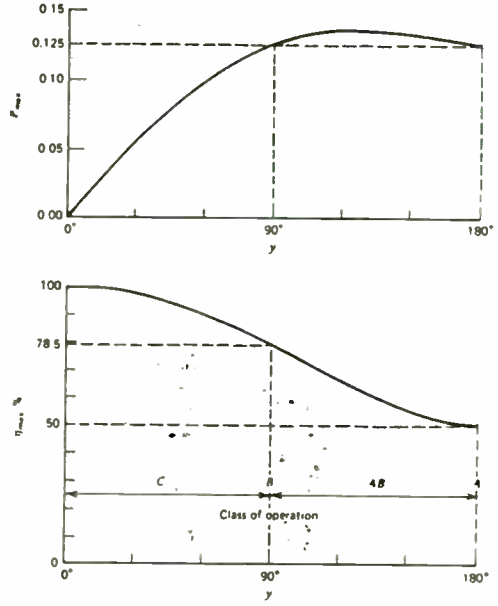


Figure 1. Efficiency and power output of power amplifier /1/.

frequency while passing a higher carrier frequency. The ability to modulate diode resistance is limited by the diode carrier lifetime, the time required to remove charges from the I layer. For efficient modulation the lifetime must be short compared to the modulation period, while low distortion requires the lifetime to be long compared to the carrier period. When these two frequencies are not far apart it may not be possible to satisfy both conditions, and a compromise value of lifetime is chosen.

Figure 2 shows the frequency limitations for diodes with lifetimes ranging from 10 nanoseconds to 2 microseconds. The fast switching diodes are best with carrier frequencies above a gigahertz and modulation frequencies below 100 kilohertz. The long lifetime diodes are best with carrier frequency above 10 megahertz and modulation frequency below 1 kilohertz. However, these limits are not rigid and diodes are useful beyond these limits.

In addition to the inverse current relation, I layer resistance varies as the square of the I layer thickness and inversely as the lifetime. However, the lifetime is itself a function of I layer thickness so that a longer lifetime diode has more resistance in spite of this inverse relationship. Figure 4 shows that the 5082-3081 diode with 2 microseconds lifetime has 30 times the resistance of the 5082-3043 diode with 15 ns lifetime. Another example of resistance dependence on lifetime is seen in Figure 5. These diodes are in shunt so higher attenuation means lower resistance. The short lifetime 3141 has lower resistance because it has a thinner I layer.

The relation between resistance and current is not valid at high currents. The resistance levels off at a current which depends on the diode construction. This residual series resistance is usually guaranteed to be below a specified maximum.

Attenuator designers often need more information about the resistance current relationship. The specifications for current controlled resistor diodes such as the HPND-4165 shown in Figure 6 include maximum and minimum resistance values at 10 microamperes and at 1 milliampere. In addition, the slope of the curve, the exponent of current, must be matched to 0.04 for all diodes in a batch. Since the slope, x, can vary from 0.83 to 1.00 while satisying the resistance specs, this delta slope spec tightens the matching considerably.

A low frequency limitation of the PIN diode is the dielectric relaxation frequency. When current is removed from the diode most of the charges return to the p and n layers. However, some charges remain in the underpleted portion of the I layer. At low frequencies this undepleted I layer resistance shorts out the I layer capacitance. A capacitance measurement would be high because only a portion of the I layer, the depleted portion, would be measured. Capacitance measurements at low frequencies (1MHz) require the use of reverse bias to drive out the

The gain of the transistor decreases if the bias point of the transistor is transfered from class A towards class B, while efficiency increases. Both of these parameters determine also the total efficiency of whole amplifier. The first stage of the power amplifier operates usually in class A, because this class gives the highest gain and power level is relatively low so the efficiency in this case is not of major importance. The last stages operate on high power level and efficiency has to be as high as possible without sacrificing the gain of the transistor. For this reason in the UHF frequency range class B is usually chosen as good compromise between gain and efficiency.

Amplifier design

The target specifications for hybrid amplifier were 23 dB gain with 2 W output power and 12 V supply voltage in 890-915 MHz frequency range. This leads to three amplifier stages when the average gain of each stage is 7-8 dB. The operation classes of the stages were A, B and B for optimum total efficiency.

Class A amplifier can be considered a linear amplifier and the theory of linear two ports can be applied directly to the design of matching circuits of the transistor. The small signal S-parameters are not useful for class B amplifier design , because it operates in nonlinear region. In this case the design of the matching circuits is based on large-signal impedances which can be measured using conventional pull load method.

Manufacturers usually give the typical values of S-parameters for packaged transistors. However, in hybrid circuits transistors are bonded on a substrate in chip form. This structure is different from packaged transistor and S-parameters mentioned in data sheet are not valid anymore.

S-parameters for the first stage transistor were measured using automatic network analyser and three point calibration method, which uses short circuit, 50 ohm load and open circuit as reference impedances. The test jig is shown in figure 2 and reference impedances in figure 3.

Figure 2. S-parameter measurement jig.

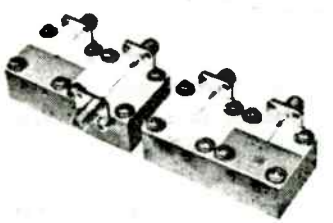


Figure 3. Reference impedances for three point calibration.

charges in the undepleted I layer in order to measure the capacitance of the entire I layer. At higher frequencies the reactance of the undepleted I layer is small and the resistance of the undeplete charges is not small enough to cause this capacitance error, so no reverse bias is needed.

The dielectric relaxation frequency is the frequency where the resistance of the undepleted charges equals the reactance of the undepleted I layer. This frequency is about 80 MHz for general purpose diodes, about 16 GHz for the fast switching diodes. When operating below the dielectric relaxation frequency it is necessary to use reverse bias to reach the specified capacitance. Since reverse bias is normally used in switching applications to speed up the switching, the concept is not important for fast switching diodes.

We have seen two possible problems at low frequency. The resistance can vary at the carrier frequency and the capacitance can vary with reverse voltage. There is also a high frequency limitation. At zero bias we expect the diode to approximate an open circuit. This is true at low frequencies when the capacitive reactance is high. At higher frequencies the reactance decreases and the insertion loss of a shunt diode increases, related to the product of frequency and capacitance. Figure 8 shows how insertion loss varies. When this product is 3.2 for example, the loss is 1 dB.

Figure 9 indicates a technique for extending this frequency limitation. The diode capacitance may be included in a low pass filter with the lead inductances on either side of the diode. Package outline 60 and 61 diodes are made this way. The ribbons to the diode chip are properly shaped to provide the needed inductance. When chips are placed in other packages the limitations due to package parasitics appear at frequencies well below what is shown in Figure 8. Before the insertion loss increases because of low diode reactance, the package inductance resonates with the diode capacitance. Figure 11 shows this resonance for a 0.12 pF diode in packages 15 and 31 at 9.2 GHz and 14.5 GHz. Insertion loss due to diode capacitance alone at these frequencies is about 0.1 dB.

Figure 12 shows the problem at forward bias. The package parasitics resonate with each other changing the low resistance Rs to an open circuit. Similar problems limit the performance of series diodes to the VHF region. Figure 13 shows that isolation drops below 20 dB at a few hundred MHz. Chip isolation was calculated with 0.5 nH assumed for the lead inductance. The graph demonstrates that microwave applications for series diodes require the use of beam leads.

Isolation in a shunt switch is limited by the diode series resistance. Using two diodes together cuts the resistance in half and improves isolation 6 dB. Figure 14 shows the results of using two diodes spaced by 90 degrees. The dB isolation more than doubles, and the bandwidth is quite wide, exceeding 50 dB isolation for about a 10:1

The nonidealities of the network analyser are eliminated by computer, which-calculates the correction factors for measured S-parameters and writes out the corrected values on paper or to mass-storage media like floppy disk. These parameters can be used directly to the design of the matching circuits without any kind of peeling process, because reference planes were selected to be on the connection point of the transistor bonding wires.

As previously mentioned, a power transistor can be described in terms of the large-signal source and load impedances required to produce a given output power and gain. A typical measuring system for large-signal impedances and power measurements is illustrated in figure 4.

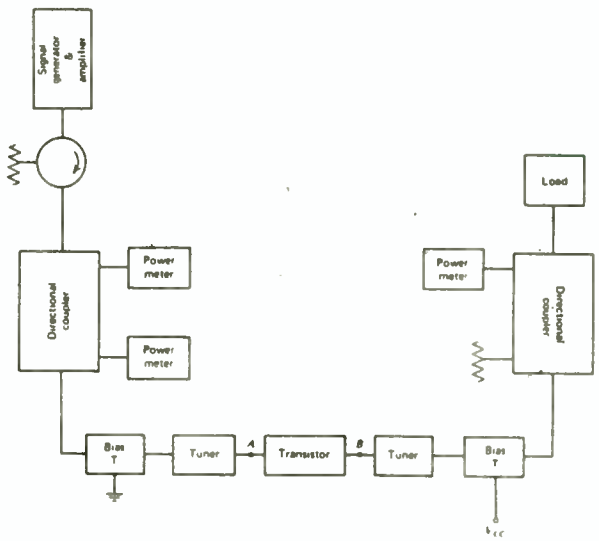


Figure 4. Measuring system for large-signal impedances /3/.

Tuners used in this measurement system were coaxcial stub tuners. The input tuner was adjusted until reflected power was zero and output tuner was adjusted for given output power level. After the transistor was properly tuned for given power level , the transistor was disconnected from the test setup and the impedances at the reference planes A and B looking toward the generator and toward the load were measured with a network analyser. The conjugates of these impedances represent the transistor's large-signal input and output impedances, respectively. These impedances are functions of output power level, frequency and bias conditions. For this reason the transistor has to be measured in those conditions where it is intended to be used.

Matching circuits consist of microstriplines and ceramic chip capacitors. In spite of the small size of the chip capacitor its equivalent circuit contains small series inductor, which means that the capacitance is a function of frequency. For accurate computer analysis the equivalent circuit of the capacitor has to be measured.

The capacitance was measured with HP 4191A impedance analyser as a function of frequency . The equivalent circuit of the capacitor, which consists of inductor and capacitor in series connection, was fitted to the measurement results, using least squares fitting method. The total capacitance can be written in form

$$\frac{1}{C_{tot}} = \frac{1}{C} - \omega^2 L \qquad (1)$$

where C and L are the values of the equivalent circuit.

This equation is of quadratic type and coefficients C and L can be solved using quadratig regression analysis.

frequency range. It might be expected that this two-diode switch would double the power handling ability, but there is no improvement. The second diode absorbs very little power and does not contribute to the power specification (Figure 15).

With 1 ohm resistance a shunt diode absorbs less than 10% of the incident power. In this application the incident power can be 10 times the power rating of the diode. In attenuator applications the multiplier is only two, corresponding to 6 dB of attenuation. Figure 16 shows this ratio as a function of attenuation. Switches can handle many times the diode power rating, since the loss switches from low insertion loss to high isolation. However, this assumes that switching time is fast compared to diode thermal time constant.

Both shunt and series diodes attenuate by reflecting most of the incident power. In many applications this reflected power disturbs the operation of another element of the system. Figure 17 shows a number of attenuator designs that maintain a low value of SWR at all attenuation levels. The π and T attenuators are symmetrical with the outer diodes set at the same resistance, but the inner diode set at a different value. Bias circuits may be built with "one knob" tuning providing the proper bias current to all three diodes.(1)

The ideal behavior of attenuation controlled by current, independent of RF power, is not valid at high power levels, due to rectification of the RF signal. Figure 18 shows how low level attenuation is increased at 1.6 watts, with the effect most severe at 3 dB attenuation. Rectification is easier with short lifetime diodes so the 5082-3141 curve is higher. Rectification is also easier at lower frequencies so we would see VHF curves above these. Bias resistance was zero for this data.

Since this increase in attenuation is due to rectified current we expect a reduced effect when bias resistance is increased. This is shown in Figure 19 where the effect is not seen until the power reaches a half watt with bias resistance increased to 100 kilohms. Above that level the opposite effect is seen. Attenuation decreases at higher power indicating an increase of diode resistance. This increase of resistance is the result of diode heating. In this example rectified current is small so the diode heating effect is dominant.

(1) Hewlett-Packard Application Note 936, High Performance PIN Attenuator For Low Cost AGC Application.

The basic structures of the matching circuits were designed using immittance chart. The starting values were optimized with computer using APLAC program /2/. This program is intended for the linear analysis of the microwave circuits, but also matching circuits for nonlinear transistor stages can be designed when the input and the output ports of the transistors are treated as passive impedances (large-signal impedances). Today there is more powerful programs commercially available than APLAC. Most widely known programs are probably Touchstone and Super-Compact.

Construction

The circuit was printed on 0.635 mm thick alumina substrate using gold and resistor pastes. Metallized holes were made printing gold on both sides of the substrate. Chip transistors were bonded to the substrate with conductive epoxy and gold wires using ultrasonic bonding. After this the substrate was fixed to the heatsink with conductive epoxy and the whole circuit was connected to the test jig. The construction of the transmitter is shown in figure 5 and the test jig is illustrated in figure 6.

Measured performance

The manufactured amplifier was measured in 890 - 915 MHz frequency range with 10 mW input power and 12 V supply voltage. The measured gain of the amplifier is shown in figure 7. The amplifier achieves 22 dB gain and 1.5 W output power.

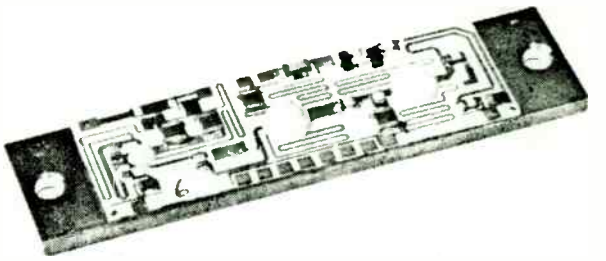


Figure 5. The manufactured hybrid transmitter.

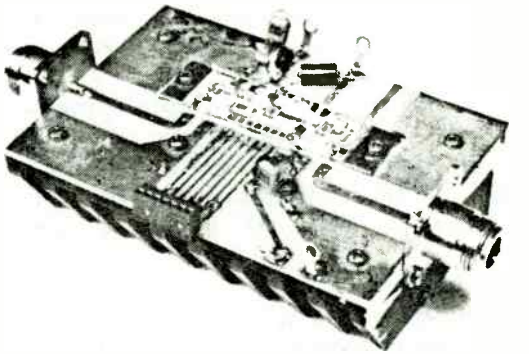
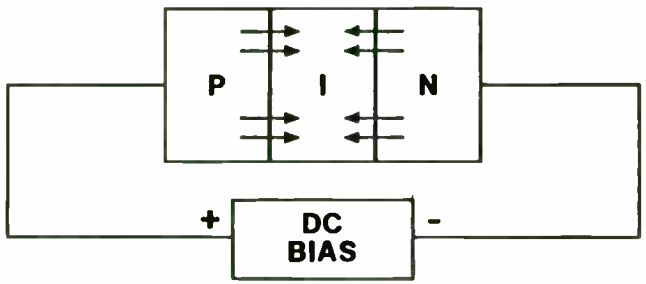


Figure 6. The test jig of the transmitter.

THE PIN DIODE



Q ∝ DC BIAS CURRENT

G ∝ Q

$$R = \frac{1}{G}$$

FIGURE 1

I LAYER RESISTANCE

$$R \propto \frac{W^2}{I\tau}$$

W IS I LAYER THICKNESS

BUT LIFETIME IS LONG WHEN I LAYER IS THICK

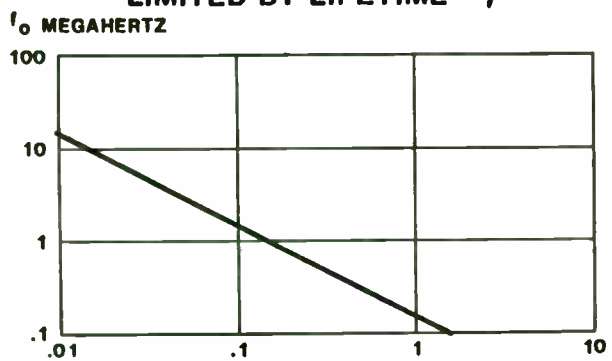
USUALLY W^2 OVERCOMES τ EFFECT

SO FOR SAME CURRENT LONG LIFETIME DIODE HAS HIGHER RESISTANCE THAN SHORT LIFETIME DIODE

FIGURE 3

MODULATOR FREQUENCY LIMITATIONS

FREQUENCY PERFORMANCE LIMITED BY LIFETIME - τ

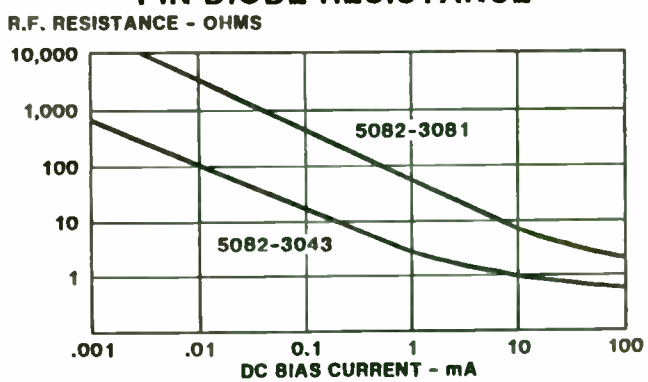


$$f_o = \frac{1}{2\pi\tau}$$

$100\ f_m < f_o < .01 f_c$

FIGURE 2

PIN DIODE RESISTANCE



DIODE 3081 HAS LONG LIFETIME 2μs

DIODE 3043 HAS SHORT LIFETIME 15ns

FIGURE 4

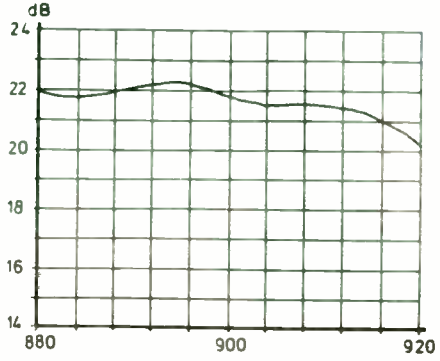


Figure 7. The gain of the amplifier.

Conclusion

The aim of this paper is to investigate possibilities to realize UHF power amplifier with thick film techniques. This technique was verified to achieve acceptable performance in this frequency range if low losses and sharp outlines of the microstrip are not required.

Acknowledgement

The author wishes to express his gratitude to professor Veikko Porra of Helsinki University of Technology. Discussions with professor Porra have been very useful during this work.

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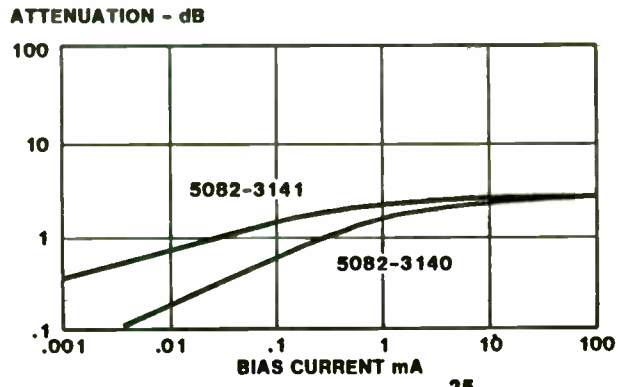
/2/ Valtonen M.:"APLAC - a frequency domain circuit design program for HP 9816 and HP 9836 computers, 11 Jan 1985 revised 5 May 1986, Helsinki University of Technology, Laboratory of circuit theory and basic electronics.

/3/ Ha T.T.:"Solid State Microwave Amplifier Design", New York - Chichester - Brisbane - Toronto, John Wiley and Sons, Inc. 1981,326 pp.

MATCHED ATTENUATOR



$$\text{ATTENUATION} = 20 \log \left(1 + \frac{25}{R}\right)$$

$$R \propto \frac{W^2}{IT}$$

FOR SAME CURRENT, HIGHER ATTENUATION FOR THINNER I LAYER NOT FOR LONGER LIFETIME.

FIGURE 5

CURRENT CONTROLLED RESISTORS

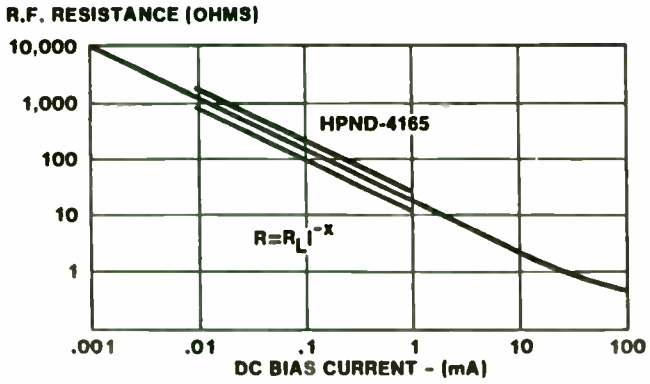


FIGURE 6

DIELECTRIC RELAXATION FREQUENCY

AT LOW FREQUENCIES UNDEPLETED I LAYER RESISTANCE SHUNTS CAPACITANCE SO TOTAL CAPACITANCE IS HIGHER

$$R = \frac{1}{2\pi f_{DR} C}$$

FOR EXAMPLE:

$$R = \frac{\rho d}{A} \qquad C = \frac{\varepsilon A}{d}$$

$$f_{DR} = \frac{1}{2\pi\rho\varepsilon}$$

for $\varepsilon = 10^{-12}$

1F $\rho = 2000$, then $f_{DR} = 80$ MHz

or, 1F $\rho = 10$, then $f_{DR} = 16$ GHz

FIGURE 7

SHUNT DIODE INSERTION LOSS

$$10 \log \left[1 + \left(\frac{\pi FC}{20}\right)^2\right]$$

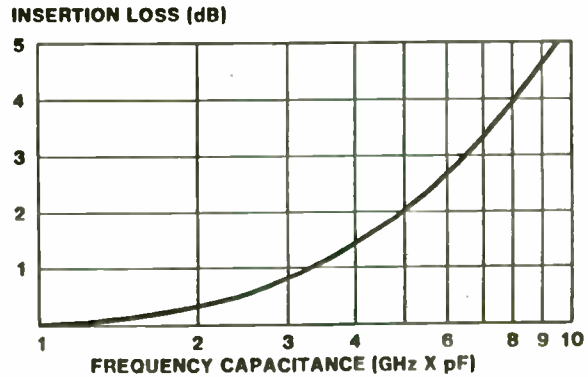
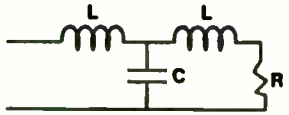


FIGURE 8

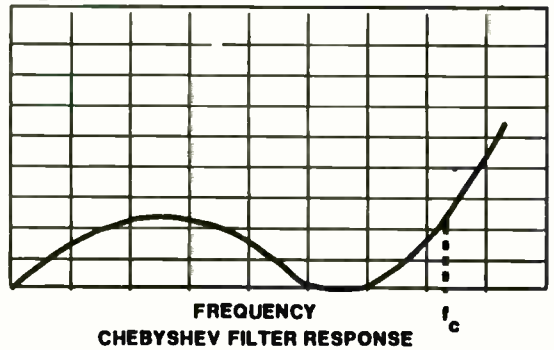
EXTENSION OF HIGH FREQUENCY LIMITATIONS

SOLUTION



LOW PASS FILTER WITH DIODE AS SHUNT CAPACITOR

INSERTION LOSS



CHEBYSHEV FILTER RESPONSE
APPLICATION NOTE 957-2

FIGURE 9

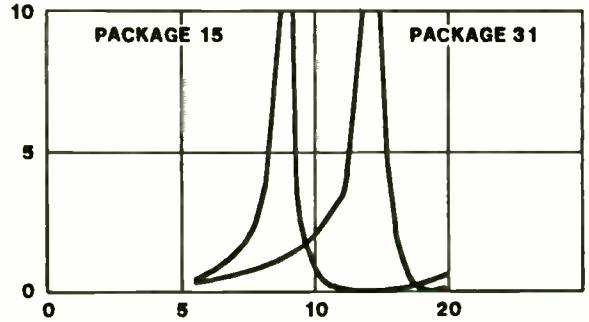
PACKAGE LIMITATIONS

HIGH INSERTION LOSS AT FIRST RESONANCE

$$F_{RES} = \frac{1}{2\pi\sqrt{L_p C_j}}$$

LOW INSERTION LOSS AT SECOND RESONANCE WITH PACKAGE CAPACITANCE

INSERTION LOSS - dB

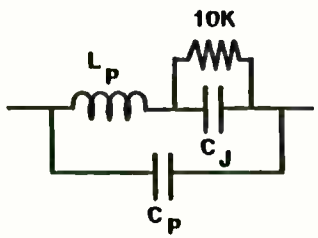


INSERTION LOSS OF PACKAGED SHUNT DIODES
.12 pF JUNCTION CAPACITANCE

FIGURE 11

FIGURE 10

PACKAGE LIMITATIONS



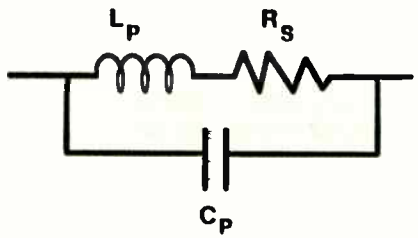
REVERSE OR ZERO BIAS

PKG.	15	31
C_p pF	.13	0.2
L_p nH	2.5	1.0

AT L_p C_J RESONANCE - LOW ISOLATION FOR SERIES DIODE - HIGH INSERTION LOSS FOR SHUNT DIODE;
AT SECOND RESONANCE WITH C_p - GOOD PERFORMANCE

FIGURE 12

PACKAGE LIMITATIONS



FORWARD BIAS

AT RESONANCE - HIGH INSERTION LOSS FOR SERIES DIODE - LOW ISOLATION FOR SHUNT DIODE

THIS PROPERTY IS USEFUL IN NARROW BAND WAVEGUIDE SWITCHES

DESIGN: A Program for the Automated Synthesis of Broadband Matching Networks between Complex Terminations

by

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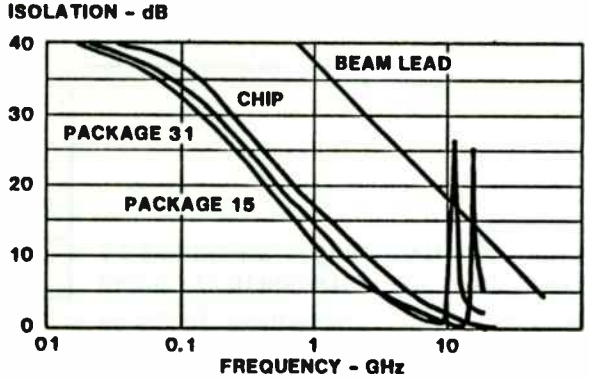
I. ABSTRACT: DESIGN - A Program for the Automated Synthesis of Broadband Matching Networks between Complex Terminations

A computer program has been written that performs the truly automated synthesis of precision, broadband, gain-sloped, lumped-element or distributed-parameter matching networks between complex sources and complex loads. The algorithm is based upon the real-frequency technique, which requires, as essential data, only a table of values for the source and load impedances, along with a set of desired values for the transducer gain function of the equalizer at a number of frequency points.

The program proceeds virtually automatically to the realization of the matching network once the data file has been read and a degree for the equalizer has been selected. This is in contrast to previous efforts, where the user had to provide special initial solutions, particular error-function weights, and other detailed information in order to obtain convergence of the design algorithm.

The capabilities of the algorithm have been verified in many different matching-network design examples. Some of these examples have been taken from the literature, and, in each such case, the program has been able to meet or

ISOLATION OF SERIES DIODES



0.12 pF JUNCTION CAPACITANCE FOR CHIP AND PACKAGED UNITS

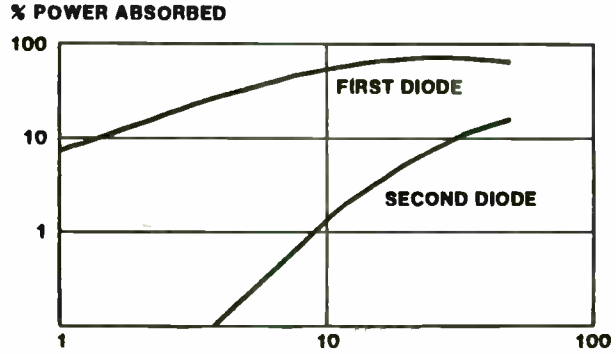
0.02 pF BEAM LEAD DIODE CAPACITANCE

PACKAGE 15 RESONATES FIRST BECAUSE Lp LARGER

PACKAGE 31 WORSE BELOW RESONANCE BECAUSE Cp LARGER

FIGURE 13

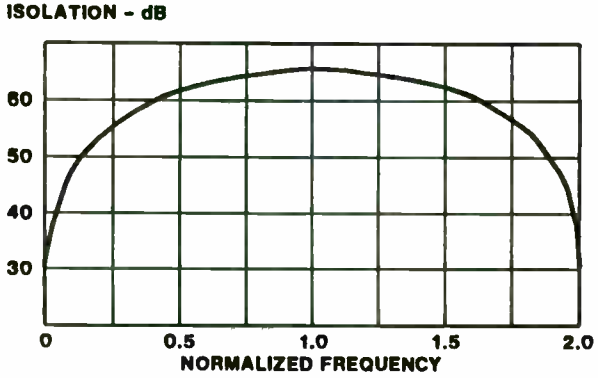
ABSORBED POWER DIVISION IN QUARTER WAVE PAIR



SECOND DIODE DOES NOT IMPROVE ABILITY TO HANDLE HIGH POWER

FIGURE 15

BROAD BAND SWITCH DESIGN



QUARTER WAVE PAIR
ONE OHM DIODES

ISOLATION MORE THAN DOUBLE SINGLE DIODE

FIGURE 14

RATIO OF INCIDENT POWER TO ABSORBED POWER

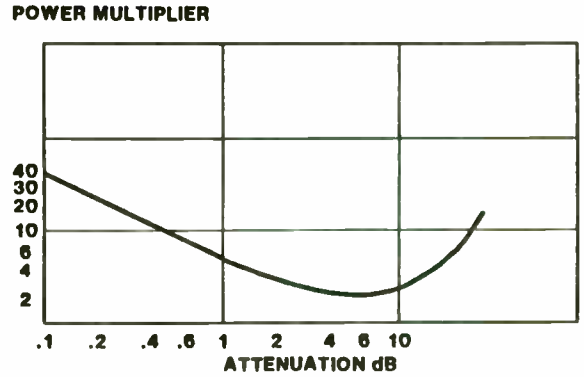


FIGURE 16

exceed the efficiency and performance of the previously published designs.

The program runs on IBM PC/XT/ATs and compatibles as well as on HP-series desktop computers.

II. INTRODUCTION

A. The Methods and Capabilities of DESIGN

DESIGN performs the truly automated synthesis of precision, broadband, gain-sloped, lumped-element or distributed-parameter matching networks - also referred to as equalizers - between complex sources and complex loads.

1. The Advantages of DESIGN's "Real-Frequency" Technique

The essential part of the synthesis method used in DESIGN is based upon the work of Carlin and Komiak [1]. Their method, also known as the real-frequency technique, has been shown to produce matching networks that are "simpler in structure and superior in frequency response to equal-ripple designs" [2] based upon the classical approaches of Fano [3] and Youla [4] as developed by Chen [5] and Mellor [6]. Furthermore, the real-frequency technique requires only a simple numerical description of the source and load as necessary data for the synthesis. The design process can proceed automatically once the source and load has been so described. On the other hand, the classical approaches require, as a preliminary task, the construction of equivalent circuit models for the source and load, and then require substantial designer interaction to perform such tasks as parasitic absorption and impedance scaling via the Norton/Kuroda transformations. To the best of our knowledge, DESIGN is the only commercially available program that employs Carlin and Komiak's superior real-frequency technique for matching network synthesis.

2. DESIGN: What It Does

DESIGN synthesizes lossless matching networks to provide a specified magnitude response (Sm21) across a frequency band between a complex source impedance and a complex load impedance. The program user must first construct a data file containing (1) the source and load data, and (2) the desired values for Sm21 at a number of frequencies points which define the passband. The user interactively inputs the name of the data file and the desired degree of the network once the program starts executing. DESIGN then proceeds with

ABSORPTIVE ATTENUATORS

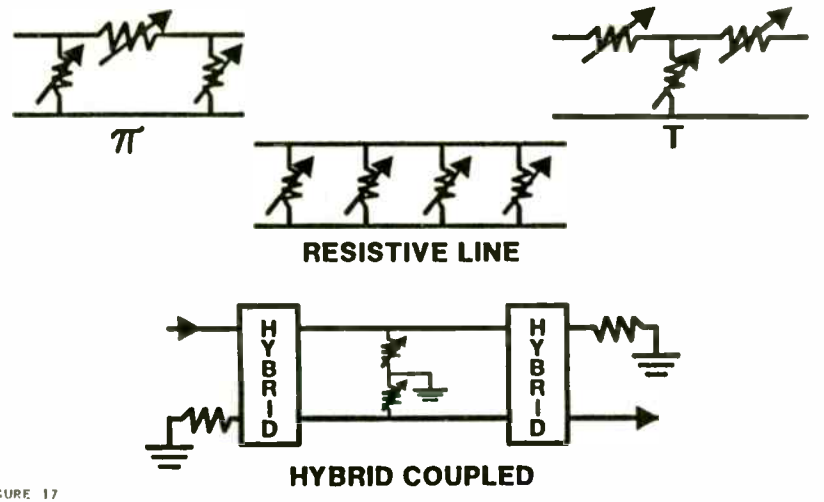
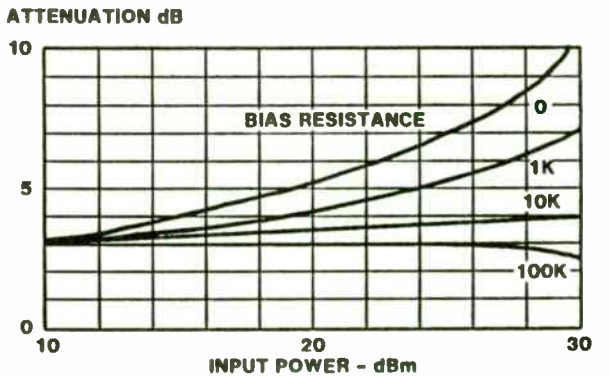


FIGURE 17

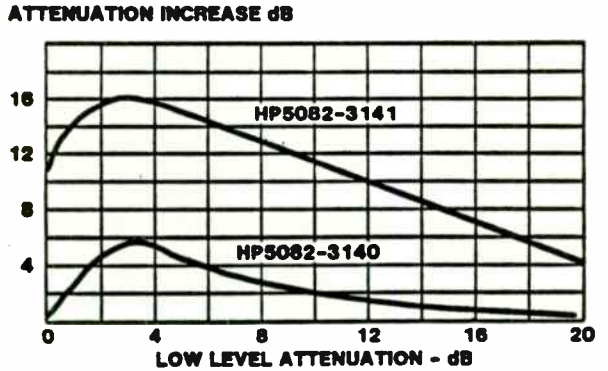
POWER SENSITIVITY IN A 3 dB PIN ATTENUATOR



FREQUENCY 10 GHz
DIODE HP5082-3141
REVERSE EFFECT AT HIGH VALUE OF BIAS RESISTANCE
DUE TO TEMPERATURE EFFECTS.

FIGURE 19

POWER SENSITIVITY AT +32 dBm INPUT



DATA TAKEN AT 2 GHz ZERO OHMS BIAS RESISTANCE
THE INCREASE IS LESS AT HIGHER FREQUENCIES
THE INCREASE IS LESS FOR THE DIODE WITH LONGER LIFETIME (3140)
SEE AN 957-3

FIGURE 18

only a small amount of user interaction after this point, although certain default options may be reset, if desired, during the synthesis process.

The design procedure is based on a lumped, shunt-capacitor, series-inductor, lowpass topology, with an optional shunt-inductor at the load end of the network providing a bandpass response, if so desired. The program indicates which topology is most appropriate for a given set of source and load data, and the program user has the option to follow this suggestion or not. The allowable circuit structures are capable of handling virtually any set of matching network design requirements.

3. DESIGN: Single Matching Problems

The real frequency technique was developed in somewhat different ways for the "single-matching" case, i.e. a real source and a complex load, and for the "double-matching" case, i.e. a source and load which are both complex. The method for single-matching has been described in [7]. Basically, the method involves: (1) constructing a piecewise linear function of frequency, R(f), as an initial approximation to the real-part of the matching network impedance at the output port; (2) optimizing R(f) so that the network, if it could be realized exactly from R(f), would provide the prescribed gain shape across the passband; (3) constructing a rational approximation to R(f); and (4) realizing and optimizing the final circuit. Our enhancements to the original Carlin-Komiak algorithm include the automation of the design process and the optimization of the final circuit.

4. DESIGN: Double Matching Problems

At least two different methods have been developed previously to match complex sources to complex loads [8], [9], [10]. In each case a difficult optimization problem must be solved to yield the final circuit. To obtain convergence, the user must first generate a good initial guess to the solution.

DESIGN's method for solving the double-matching problem is a direct extension of the approach to single-matching. The presence of complex sources and complex loads is accommodated by performing a relatively easy optimization on a preliminary design of the network. This initial design is produced automatically by the program.

The technique begins with the conversion of the double-matching problem to one which initially involves only single-matching. This is done by resonating the source impedance with either a series-inductor or a shunt-capacitor so that the source impedance becomes purely real at one frequency. The synthesis then proceeds on the presumption of a purely real source, constant with frequency across the passband, and the given complex load. Hence this part of the design process is identical to the single-matching case. After this preliminary network is designed, the actual complex source is reintroduced,

and the network is optimized to meet the original design goals. The optimization proceeds quickly and efficiently to a solution since (1) we start from a comparatively good initial guess obtained in our preliminary design; and (2) we use an optimizer specially developed by us to handle this kind of circuit problem.

B. The Efficacy of DESIGN's Single- and Double-Matching Algorithms

DESIGN has been able to duplicate, if not exceed, the quality and efficiency of the networks designed by any of the other single- or double-matching synthesis algorithms. It should also be noted that while DESIGN goes through a sequence of intricate steps to realize the desired matching network, the user need not be familiar with the details of the techniques, because the program proceeds automatically, with very little input from the user. The program does indicate what it is doing at any given moment, and various parts of the program may be interrupted and re-executed, as desired, with different values for the defaults.

III. DESIGN SAMPLE SESSION: DOUBLE-MATCHING

A. The Data File Format for Double-Matching

The rules for constructing the file are as follows.

The first line of the data provides the following information:

1. The nature of the matching problem - C indicates complex-source to complex-load;
2. How the source is described - Z for impedance values, Y for admittance values, or S followed by a corresponding reference resistance for reflection coefficient values;
3. How the load is described - Z for impedance values, Y for admittance values, or S followed by a corresponding reference resistance for reflection coefficient values; and
4. How the desired gain for S21 is specified - A for absolute magnitude, and D for decibels.

Each subsequent line gives, for each frequency,

1. The frequency in Hertz, followed by
2. The values for the source (real and imaginary parts for impedance and admittance, magnitude and phase in degrees for reflection coefficient), followed by

RF AND MICROWAVE TRANSISTOR BIAS CONSIDERATIONS

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Applications Engineer
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INTRODUCTION

The purpose of this paper is to present an overview of the advantages and disadvantages of some common bias circuits. Resistive, diode, and active bias circuits will be examined and compared as to how well they stabilize the transistor bias point against DC parameter changes caused by temperature and device-to-device variations.

BIAS POINT STABILITY

Before examining the bias circuits, let's look at some of the reasons for being concerned about bias stability. Figure 1a shows a transistor biased for Class A operation which is not stabilized against DC parameter changes. Increasing temperature shifts the bias point further to saturation (Figure 1b), while decreasing temperature shifts the bias point closer to cutoff (Figure 1c). Temperature extremes caused the transistor's DC parameters to change which resulted in the shift of the bias point. In the above example the shift in the bias point was large enough to cause unwanted distortion in the output signal. Figure 2a and 2b show that both gain and noise figure of a bipolar transistor are also a function of the collector current.

Bias point shifts caused by temperature are not the only concern. The DC parameters also change due to device-to-device variations . The DC current gain of microwave bipolar transistors can vary over a range of 5:1 and still be within the manufacturer's electrical specification at 25 degrees C. This means that a shift in the bias point can be caused by temperature and device-to-device variations. Obviously , a bias circuit that can minimize these bias point shifts is desirable. The first step in understanding how to stabilize the bias point is to identify the DC parameters which affect the bias point the most and how these parameters respond to temperature variations.

TEMPERATURE SENSITIVE DC PARAMETERS

The principal dependent variable in DC stability analysis is the collector current (I_C)[1,2]. The following DC parameters, which are shown in the equivalent circuit of Figure 3 , are temperature sensitive and directly influence the collector current.

Base to Emitter Voltage (V_{BE}):

V_{BE} is internal to the transistor and has a negative temperature coefficient of 2 mV/degree C. Figure 4 shows the temperature characteristic of this parameter.

Reverse Collector Current (I_{CBO}):

I_{CBO} is the current flowing through the reversed biased PN

3. The values for the load (real and imaginary parts for impedance and admittance, magnitude and phase in degrees for reflection coefficient), followed by

4. The desired value for S21 (absolute magnitude or dB, as noted above).

Any time an alphabetic character is called for in the first line of the data file, any other symbol may be appended to that character to aid, for example, in the readability of the file. All alphabetic data may be entered in either upper or lower case.

Data entry in the file is entirely free-format; blank lines are allowed anywhere; comment lines are denoted by the single apostrophe (') being the first non-blank character on the line. Furthermore, comments may be appended to the end of any data line. DESIGN will inform the user of most data file errors.

B. Matching a Complex Source to a Complex Load - An Example

Consider a typical microwave transistor amplifier, where the topology is a cascade of transistors and matching networks. We shall consider the design of an interstage matching network that (1) couples the output of one Plessey GAT6 GaAs FET to the input of an identical device, and that (2) provides maximum unilateral transducer gain through the cascade of the equalizer and one of the devices. In other words, we seek an equalizer to provide a prescribed transducer gain function when terminated at the source end by the S22 of the GaAs FET and terminated at the load end by the S11 of the device.

1. The Data File

The data file for this problem could be written as follows, according to the rules of the previous section.

```
'The name of this data file on disk is CEXAMPLO.MCH
'S22 as a source, S11 as a load between a pair of GAT6 GaAs FETs
'First line of data could be written simply as:  C  S 50  S 50  D

Complex-source    Sparams-for-source 50    Sparams-for-load 50    dB-S21

 8e9    .735  -42    .775  -107     -2.71
 9e9    .740  -47    .750  -118     -1.84
10e9    .750  -52    .730  -128     -1.16
11e9    .755  -58    .710  -136     -0.515
12e9    .765  -62    .695  -145      0.0
```

The gain slope of the equalizer was chosen to achieve an overall flat gain shape between the matching network and the terminating transistor, and to obtain the maximum available unilateral gain.

2. Performing the Synthesis

junction of the collector to base. Classically, this leakage current is expected to double for every 10 degrees C temperature rise in a silicon semiconductor junction. The leakage current for silicon is so low that under most conditions this parameter can be negected.

DC Current Gain (h_{FE}):

The h_{FE} of a transistor is defined as the ratio of the collector current to the base current. This parameter typically increases linearly with temperature at the rate of 0.5 % /degree C.

STABILITY FACTORS

Before we proceed to examine the bias circuits, it is useful to introduce the concept of stability factors. The stabiliy factors are defined as the ratio of the incremental change of I_C vs the incremental change of each of the three components I_{CBO}, V_{BE}', and h_{FE}. The stability factor equations are given below.

I_{CBO} STABILITY FACTOR

$$S_{ICBO} = \frac{\partial I_C}{\partial I_{CBO}} \Big|_{h_{FE}, V_{BE}' = \text{constant}}$$

V_{BE}' STABILITY FACTOR

$$S_{VBE}' = \frac{\partial I_C}{\partial V_{BE}'} \Big|_{h_{FE}, I_{CBO} = \text{constant}}$$

h_{FE} STABILITY FACTOR

$$S_{hFE} = \frac{\partial I_C}{\partial h_{FE}} \Big|_{I_{CBO}, V_{BE}' = \text{constant}}$$

The total change in collector current can be expressed as the sum of each incremental change caused by I_{CBO}, V_{BE}', and h_{FE}.

$$\Delta I_C = S_{ICBO}\,\Delta I_{CBO} + S_{VBE'}\,\Delta V_{BE'} + S_{hFE}\,\Delta h_{FE}$$

Unfortunately, the stability equations can become very complicated even for a simple bias circuit such as the one shown in Figure 5. The equation of Figure 5 can be easily digested by a computer, but it doesn't help the designer gain any insight into selecting component values or in making circuit comparisons. Fortunately, the following approximations can help simplify the stability equations:

* Neglect I_{CBO} when using silicon transistors. As previouslv stated, the leakage current for silicon is typicallv so low that neglecting I_{CBO} will have negligible effect on the accuracy of the stability equations.

* Drop the hie term, which is the hybrid-pi input impedance for common emitter configuration. The external biasing resistance is usually much greater than hie, and neglecting the hie term will not upset the accuracy of the equations.

* Assume that $h_{FE} >> 1$ then $(h_{FE} + 1)$ simplifies to h_{FE}.

The stability factor S_{hFE} can be expressed as a percentage change in I_C vs a percentage change in h_{FE}[3]. The new variable is defined as F_{hFE}. The same procedure is used to define F_{VBE}

In response to screen queries, we type in the data file name, and then specify a degree of 5 with a lowpass topology. As shown on the next 3 pages, the resistance-excursion optimization proceeds (with all options set to their default values), and we stop it after 12 iterations. DESIGN performs the curve-fitting and final synthesis steps to yield preliminary lumped and distributed circuits, which are seen to furnish a good response at the high end of the band, but whose response degrades at lower frequencies. This is expected as part of our design algorithm. The final optimization is then applied, again in response to screen queries, and the lumped and distributed circuits yield a final response error of 0.46 dB and 0.78 dB, respectively.

IV. CONCLUSION

DESIGN represents what we believe to be the best program available to date for matching network synthesis. The program has been constructed to proceed rapidly and automatically to a circuit realization from a basic set of user-supplied data. The User's Guide for DESIGN, obtainable from us, demonstrates 18 examples of matching network synthesis. In those cases where the examples have been taken from the open literature, the program has been able to meet or exceed the efficiency and performance of the previously published designs.

```
MATCHING NETWORK DESIGN BEGINS:  The Resistance Excursion Optimization

        ... hold down SPACE BAR to interrupt optimization ...

Iteration    Function Evaluations    RMS % Error of |S21|**2 Across Passband
   4                 2                          2.578
   5                 2                          2.445
   6                 2                          2.426
   7                 3                          2.385
   8                 2                          2.238
   9                 2                          2.224
  10                 2                          2.104
  11                 2                          2.028
  12                 2                          1.937
Error function has changed by less than 0.50 percent.
Do you wish to continue optimization?  (Y/N): n

**Convergence Achieved, final summary follows.

  13                2                          1.934

Do you want to RETRY the resistance excursion optimization with different
internal program defaults or do you want to CONTINUE with the design process?

Retry or Continue -- (R/C): c

RESULTS: MATCHING NETWORK ELEMENT VALUES FROM THE COMPLEX SOURCE
                    TO THE COMPLEX-LOAD.

  The Lumped Element Design              The Distributed Element Design

Series Inductor: 1.054E-009 H      TRL: 120.0 ohms,  33.51 deg at 1.000E+010 Hz
Shunt Capacitor: 4.482E-013 F      OST:  25.0 ohms,  35.14 deg at 1.000E+010 Hz
Series Inductor: 3.737E-010 H      TRL: 120.0 ohms,  11.29 deg at 1.000E+010 Hz
Shunt Capacitor: 8.443E-013 F      OST:  25.0 ohms,  32.98 deg at 1.000E+010 Hz
Series Inductor: 4.195E-010 H      TRL: 120.0 ohms,  12.69 deg at 1.000E+010 Hz

Press <cr> to clear the screen and to proceed ...

   A circuit analysis follows ...

Freq. (Hz)     S21 in dB:  Desired    Lumped Design    Distributed Design
----                       -------    -------------    ------------------
8.000E+009                   -2.71        -6.96             -4.75
9.000E+009                   -1.84        -1.93             -0.37
1.000E+010                   -1.16        -0.03             -0.69
1.100E+010                   -0.52        -0.58             -0.69
1.200E+010                    0.00        -0.25             -0.60

Do you want to retry the curve-fitting with new values
for the curve-fit factor or the degree?  (Y/N): n
```

$$K_{hFE} = \frac{\Delta I_C / I_C}{\Delta h_{FE}/h_{FE}} = \frac{S_{hFE}}{I_B}$$

$$K_{VBE'} = \frac{\Delta I_C / I_C}{\Delta V_{BE'} / V_{BE'}} = \frac{V_{BE'}}{I_C} S_{VBE'}$$

The stability equations for the previous example (Figure 5) now simplify to the following:

$$K_{hFE} = \frac{1}{(1 + \frac{hFE\ RC}{R_B})}$$

$$K_{VBE'} = \frac{1}{(1 - \frac{VCC}{V_{BE'}})}$$

The simplified stability factors are easier to handle and it is now apparent that increasing the R_C / R_B ratio will decrease K_{hFE} and improve collector current stability against h_{FE} changes. We now have the tools to examine the bias circuits.

RESISTIVE BIAS CIRCUITS

* Fixed Bias

The fixed bias circuit shown in Figure 6, is the simplest and one of the worst methods of biasing a transistor because it has a very high sensitivity to h_{FE} variations. Notice that K_{hFE} is unity, which means that a 20 % change in h_{FE} will result in a 20 % change in collector current. Since h_{FE} can vary by as much as 5:1 from device to device, the transistor could be at cutoff with one device and at saturation with another. The base current, which is fixed by the voltage difference between the supply voltage and $V_{BE'}$, is the cause of the poor bias stability. If the base current were made to decrease with increasing h_{FE} and increase with decreasing h_{FE} the bias stability would improve greatly, which exactly describes the operation of the next circuit.

* Voltage Feedback Bias

The voltage feedback bias circuit shown in Figure 7 improves bias stability by allowing the base current to respond to changes in the collector current. If the collector current increases, the voltage drop across R_C increases which results in a lower collector to emitter voltage (V_{CE}). Since the base current is set by the resistor R_B and the voltage difference of V_{CE} and $V_{BE'}$, a lower V_{CE} decreases the base current which stabilizes I_C to a current closer to the quiescent bias point. The circuit will handle a decrease in I_C in a similar manner.

A circuit designed with I_C = 10 ma, V_{CE}= 10 V, V_{CC}= 12 V, h_{FE}= 50 results in K_{hFE}= 0.826. This means that the collector current will change by 82.6 % of the change in h_{FE} as compared to the 100 % change that would be expected from the fixed bias circuit. This is approximately a 17 % improvement over the fixed bias circuit for this set of conditions. The K_{hFE} stability factor shows that increasing the R_C / R_B ratio decreases the sensitivity of I_C to h_{FE} changes. A small value of R_B improves the h_{FE} stability, but it isn t alway easy to get a small value of R_B. A smaller effective value of R_B is possible using the

```
       Function Evaluation No.:  188

 Maximum Response Error in dB <=  0.46

Design refinement completed - hit <cr> to continue ...
```

```
RESULTS: MATCHING NETWORK ELEMENT VALUES FROM THE COMPLEX SOURCE
                    TO THE COMPLEX-LOAD.

  The Lumped Element Design

Series Inductor: 1.645E-009 H
Shunt Capacitor: 5.143E-013 F
Series Inductor: 5.426E-010 H
Shunt Capacitor: 8.550E-013 F
Series Inductor: 3.870E-010 H
```

Press <cr> to clear the screen and to proceed ...

NOTE: Maximum response error in Lumped Design is 0.46 dB.

```
   A circuit analysis follows ...

Freq. (Hz)     S21 in dB:  Desired    Lumped Design
----                       -------    -------------
8.000E+009                  -2.71       -2.76
9.000E+009                  -1.84       -1.38
1.000E+010                  -1.16       -1.62
1.100E+010                  -0.52       -0.49
1.200E+010                   0.00       -0.45

Optimize the (D)istributed design or (Q)uit - (D/Q): d
Optimization proceeds - hold down SPACE BAR to stop ...

       Function Evaluation No.:  233

 Maximum Response Error in dB <=  0.78

Design refinement completed - hit <cr> to continue ...
```

```
RESULTS: MATCHING NETWORK ELEMENT VALUES FROM THE COMPLEX SOURCE
                    TO THE COMPLEX-LOAD.

                  The Distributed Element Design

TRL: 120.0 ohms,   47.59 deg at 1.000E+010 Hz
OST:  25.0 ohms,   36.98 deg at 1.000E+010 Hz
TRL: 120.0 ohms,    9.73 deg at 1.000E+010 Hz
OST:  25.0 ohms,   33.11 deg at 1.000E+010 Hz
TRL: 120.0 ohms,   11.70 deg at 1.000E+010 Hz
```

NOTE: Maximum response error in Distributed Design is 0.78 dB.

Press <cr> to clear the screen and to proceed ...

```
   A circuit analysis follows ...

Freq. (Hz)     S21 in dB:  Desired    Distributed Design
----                       -------    ------------------
8.000E+009                  -2.71       -2.74
9.000E+009                  -1.84       -1.06
1.000E+010                  -1.16       -1.88
1.100E+010                  -0.52       -1.24
1.200E+010                   0.00       -0.75

Do you wish to restart the entire design process from the beginning (with
the same load data) or do you wish to quit?

Restart or Quit -- (R/Q): q
```

emitter resistor feedback circuit.

* Voltage Feedback and Constant Base Current Source

The circuit of Figure 8 can be considered to have a constant base current source, formed by the resistor network of R_B, R_{B1} and R_{B2}. The collector current can be made relatively stable if I_{BB} is chosen to be much greater than the transistor base current I_B. A good choice, somewhat arbitrary , is to pick $I_{BB} = 5I_B$ to $10I_B$. A value greater than $10I_B$ gives little improvement in stability.

* Emitter Resistor Feedback

The bias circuit of Figure 9 is one of the best methods of biasing a transistor. The circuit operates in the following manner. When the collector current and therefore the emitter current increases, the voltage drop across R_E increases. The polarity of this voltage opposes the forward bias voltage between base-to-emitter. The reduced V_{BE}, decreases I_B and therefore I_C, which stabilizes the collector current closer to its initial value. The stability factor(K_{hFE}) for this circuit is 0.169 when calculated using the design values previously given for the voltage feedback circuit, and $I_{BB} = 5I_B$. A $K_{hFE} = 0.169$ represents a considerable improvement in stability over the previous circuits.

The V_{BE}, stability factor for this circuit is:

$$S_{VBE'} = \frac{-1}{R_E} \quad \left(\text{assuming } R_E >> \frac{R_B}{h_{FE}} \right)$$

This equation implies that, the larger the R_E, the better the stability against V_{BE}, variations. There is a limit to the size R_E can be, since the voltage drop across R_E will become excessive. The next circuit examined (diode temperature compensation) presents a method of stabilizing against V_{BE}, temperature variations without resorting to large R_E values.

The emitter resistor feedback circuit does require special RF considerations which are covered in detail later in this paper.

* Diode Temperature Compensation

The emitter-base voltage has a negative temperature dependence of about 2 mv/ degree C, which can be compensated by introducing diodes into the voltage divider network as shown in Figure 10[4,5].

The calculated stability factor for this circuit is $S_{VBE'} = 1/ 5.65R_E$, which is a 5.65 times improvement over the emitter feedback circuit of Figure 9. The above calculation was made with the design values from the voltage feedback example, and assumed compensation was done with a single diode that had a temperature characteristic identical to the transistor emitter-base junction.

* Zener Diode Bias

The Zener diode shown in Figure 11 determines the collector

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to base voltage V_{CB} of the transistor. The collector to emitter voltage V_{CE} is fixed by the sum of V_{BE} and the Zener diode voltage (V_Z). The current through R_C divides between the transistor and D_1. Temporarily ignoring the current through R_B, the only current flowing through D_1 is the base current of the transistor. Most of the current flows through the collector as I_C. If the h_{FE} is low, the current through D_1 will increase accordingly. However, if h_{FE} is high, the current through D_1 is low and the regulation as a Zener is poor. Therefore, R_B is added to the bias circuit to ensure that enough current flows through the Zener for good voltage regulation[6].

This circuit is more stable than the voltage feedback circuit, but the Zener diode is noisy and may require a large value bypass capacitor to prevent the Zener's noise from modulating the amplified RF signal.

* Active Bias Circuit

An active bias circuit is shown in Figure 12, which uses a PNP transistor (Q_2) to help stabilize the bias point of the RF transistor (Q_1). The transistor Q_2 acts as a DC feedback circuit that senses the collector current of Q_1 and adjusts Q_1's base current to hold the collector current I_{C1} constant. The circuit operates in the following manner. If I_{C1} increases, the voltage drop across R_C increases and opposes the forward bias of the PNP transistor which decreases I_{E2}. The decrease in I_{E2} causes I_{C2} and I_{B1} to decrease. The lower base current into Q_1 decreases I_{C1} which opposes the original increase in the collector current.

The collector current equation for the RF transistor is shown in Figure 12. Notice that if $(1+h_{FE1})R_C >> R_B/(1+h_{FE2})$, then the collector current is essentially independent of the DC current gains of either of the transistors. A very detailed analysis of this circuit is available in the literature[7].

The active bias circuit has the best stability of all the circuits examined, but does require the most parts. The PNP transistor does form a feedback circuit, which must be carefully RF bypassed to prevent bias oscillations.

EMITTER RESISTOR BYPASS

The emitter resistor improves bias stability through the use of negative feedback which is desirable at DC, but not at RF frequencies. The RF gain will be reduced if the resistor is not RF bypassed. Bypassing the emitter resistor does require two special precautions to prevent possible oscillations.

First, the emitter bypass capacitor must be large enough to provide an effective RF ground at both the design frequency and lower frequencies. The Smith Chart of Figure 13 shows the effect on the transistor S-parameters when the bypass capacitor (C_E) is too small. Changes in the transistor s S_{11} and S_{22} parameters are

DEVELOPING NON-LINEAR OSCILLATOR MODELS USING LINEAR DESIGN TOOLS

Summary

The design of oscillators typically starts from the Class A operating condition and then changes into the large signal range for the semiconductor. The designer has two choices: either to design for highest output power, (highest efficiency) or for lowest noise. Highest output power and lowest noise are not necessarily the same. This paper is a brief summary of requirements towards designing high power low noise oscillators at high frequencies using a dielectric resonator oscillator as an example.

Introduction

A variety of transistor feedback arrangements are possible which lead to building an oscillator. Figure 1 a-c show successful RF topologies. The tuned element is an LC circuit, depending upon the devices, with a grounded emitter, grounded base, or grounded collector circuit is a better choice. The tuned circuit is responsible for determining the resonant frequency and at the same time provides 180^{o} phase shift. The overall performance of the oscillator depends on the Q of the resonator and of the high frequency performance of the semiconductor. By making slight changes in the circuit, a field effect transistor can be used at UHF frequencies and higher, instead of the bipolar transistor. At microwave frequencies, MESFETs are frequently used. In looking at Figure 1-C the capacitor from emitter to ground can be replaced by a series resonant device and therefore obtaining the possibility of using a second tuned circuit. This configuration has been used for designing low phase noise oscillators (1) and if this emitter circuit takes over the burden of the high Q devices, then the other LC circuit is only used as a phase shifter.

In analyzing the semiconductor one obtains the equivalent circuits, Figure 2 and 3, which describe the intrinsic model of the bipolar transistor and the MESFET. For reason of convenience, the model used for the MESFET has has all the elements to describe a HEMPT (high electron mobility transistor). In the past, the dominant nonlinearities have been described in the so-called SPICE model. SPICE is a program that uses non-linear approximation. The computation time is excessive. SPICE programs, including microwave extensions, suffer from the lack of accurate microwave models and do not have any facilities for optimizations. Execution speed of SPICE programs are 1,000 times slower than their linear counterparts. A new method called the Modified Harmonic Balance method has been developed with the key authors being Fred Rosenbaum and Rowan Gilmore (2). This allows the use of SPICE-like models together with linear programs with as little as 1% overhead and taking full advantage of linear optimizers. As a result, transparent linear programs can be designed. This literature (3, 4) provides information on modelling of MESFETs.

Figures 4 and 5 show the large signal equivalent circuits of

shown on the Smith Chart as S_{11}/ and S_{22}/. A good RF bypass capacitor should cause little or no effect on the S-parameters . Both S_{11} and S_{22} at 4 GHz remains unchanged after the emitter resistor and 100 pF capacitor are added, but move off the Smith Chart as the frequency decreases. Reflection coefficients greater than 1 indicate conditional stability and are likely to oscillate. A value of 1000 pF would be a much better bypass capacitor value.

The second precaution is to minimize the inductance added in the emitter caused by the resistor and capacitor parasitics. The Smith Chart of Figure 14 shows the effect of emitter inductance on the transistor's S-parameters. Inductance in the emitter can potentially cause conditional stability. In this case, a rather large value of 5 nHy was selected to illustrate the effect. At a frequency of 4 GHz S_{22}/ has moved off the Smith Chart which indicates that the circuit is conditionally stable.

An effective RF bypass of the emitter resistor is a relatively straightforward procedure as long as the above precautions are taken.

SUMMARY

This paper has shown that bias stability is more a function of the bias circuit design than of the transistor's characteristics. The RF and bias circuits should be designed with equal consideration, since the RF performance of an amplifier was shown to be dependent on the bias stability.

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the bipolar and the MESFET. One of the best papers on bipolar nonlinearities is the book, Modeling the Bipolar Transistor, by Ian Getreu, published by Tektronix, Inc., Beaverton, Oregon, in 1976, Order #062-2841-00.

In order to maintain information on the large signal handling capabilities during Class C operation, a nonlinear analysis like the one leading to the oscillator amplitude stabilization was calculated. This is shown in the Appendix. While the interested reader can follow the Appendix, for those with less patience, we will assume the following simplifications. The emitter diffusion capacitants

$$C_{ed} = K \cdot I_e/V_t$$

with I_e being the diode current, in our case the emitter current and V_t is the temperature voltage or 26 mV. The emitter diffusion resistor rd = Vt/i_d. These two nonlinearities are related to the emitter current. The depletion layer capacitants are proportional to $\frac{1}{\sqrt{V}}$. Any large voltage or current modulates those elements. It can be shown that the depletion layer capacitants follow the equation C = f(V) =

$$\int_{t=o}^{\infty} f(c)dt = 2 \cdot C$$

The transconductance G_m can be expressed as

$$G_m = \sum_{V=1}^{n} g_v =$$

$$= g_o + g_1 + g_2 + + + g_n,$$

whereby the first component g_o is the DC transconductance, g_1 is the transconductance for the basic frequency, and the following are the harmonics.

Translation Into Nonlinearities

Recent publications have mostly dealt with modelling the GAS FET where the translation into large signal parameters is easier based on the fact that the nonlinearities in FETs are somewhat better to describe. Device measurements on the large signal indicate that the most contribution for the nonlinearities are G_m and Rds, while the other capacitors have smaller contributions. For this paper, I will concentrate on bipolar effects.

As a general rule, bipolar transistors have lower phase noise contribution at high frequencies based on the fact that corner frequency, f_c, which describes the flicker noise contribution is low. For small currents and for power transistors, the following table can be assumed for f_c:

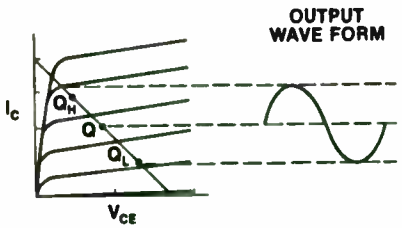
1 mA	= 300 Hz
10 mA	= 1,000 Hz
30 mA	= 10,000 Hz

This noise contribution f_c can be reduced by incorporating a resistor feedback piece in the emitter, but this is done at the expense of efficiency and cut-off frequency following the approximation A = AO/(1 + $R_e \cdot G_m$). At frequencies above several thousand MHz, the gain band width product of the bipolar

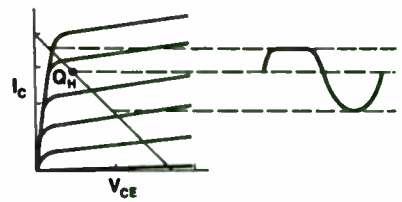
FIGURE 1

EFFECT OF TEMPERATURE ON THE BIAS POINT

A. BIAS POINT: AT 25°C



B. BIAS POINT SHIFT DUE TO INCREASING TEMPERATURE, AND DISTORTION IN OUTPUT WAVE FORM



C. BIAS POINT SHIFT DUE TO DECREASING TEMPERATURE, AND DISTORTION IN OUTPUT WAVE FORM

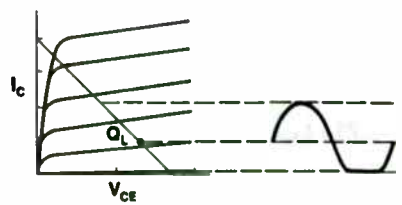
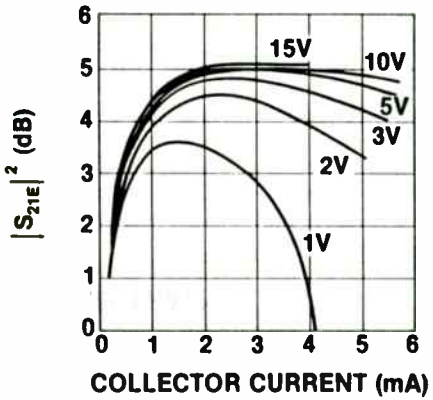


FIGURE 2

A. RF GAIN ($|S_{21}|^2$) VS. BIAS POINT



B. NOISE FIGURE VS. BIAS POINT

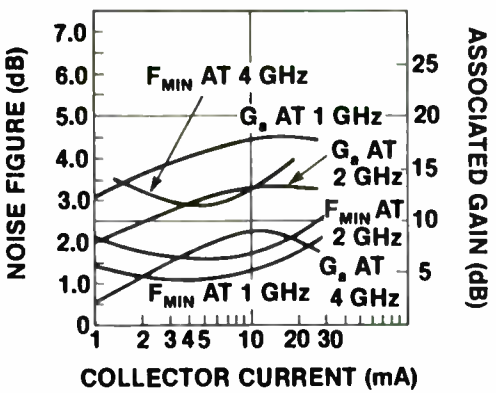
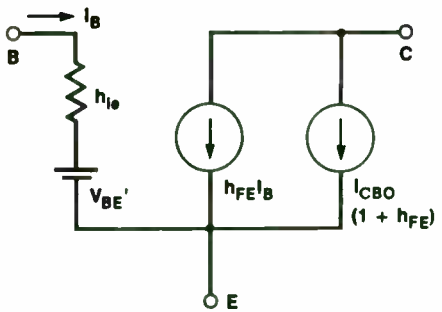


FIGURE 3

PARAMETERS THAT DOMINATE CHANGES IN I_C AND V_{CE} WHEN TEMPERATURE VARIES:

- V_{BE}' (BASE TO EMITTER VOLTAGE)
- I_{CBO} (REVERSE COLLECTOR CURRENT)
- h_{FE} (DC CURRENT GAIN)

DC TRANSISTOR MODEL



transistors is no longer sufficient to maintain oscillation. Therefore, one has to switch over to MESFETs. The N-channel field effect transistors are useful in oscillators from less than a few MHz to approximately 1,000 MHz. Then bipolar microwave transistors should take over, and above 4-6 GHz MESFETs are the choice.

A convenient way of obtaining large signal parameters for the bipolar transistor is to look at the nonlinear model Figure 4 and to computer optimize the equivalent model Figure 2, by adjusting the nonlinearities as previously indicated by approximately doubling the depletion layer capacities and reducing G_m and adjusting R_{de}.

Fourier analysis can show that the transconductance Gm and the input conductance Re(Y11) can be calculated from the following. The emitter resistance R_e, which has been described by

$$R_e = 26mV/I_e,$$

will be rewritten in the form $R_e = \frac{KT}{qI_e}$ whereby R_e is said to be the small signal emitter resistance which increases with signal level, then the ratios

$$\frac{R_e^*}{R_e} = \frac{\left|\frac{Eq}{kT}\right| J_0\left(\frac{Eq}{kT}\right)}{2 J_1\left|\frac{Eq}{kT}\right)} = \frac{V J_0(V)}{2 J_1(V)}; \frac{C_e^*}{C_e} = \frac{g_m^*}{g_m} = \frac{2 \cdot J_1(V)}{V J_0(V)}$$

whereby E is the peak value of the base emitter signal voltage assume to be given by $E \cdot \cos(\omega t)$. These ratios, expressed in $I_0(v)$ and $I_1(v)$, which are hyberbolic Bessel functions of the first kind of order zero and one are shown in the Appendix. It can be further shown mathematically that the transconductance and the input capacitance get reduced in value as a function of the base emitter drive voltage, while the input resistance increases. The final emitter current is also going to change based to a bias shift as a function of the applied signal voltage following the equation

$$V_{BIAS} = \frac{KT}{q} \ln\left[J_0(V)\right]$$

Finally the peak emitter current using the same hyperbolic function can be expressed as

$$i_c \text{ (peak)} = \frac{I_e \text{ (mean) } e^V}{I_0(V)} .$$

Example: Setting the base to emitter drive voltage $\frac{qE}{KT}$ to 2, the value of the transconductance reaches the 3dB point and the input resistance also increases from the relative value 1 to 1.4. This base emitter drive voltage generates an approximate bias shift of $\frac{q\ E}{KT}$ which then results into a ratio of the collector current components relative to twice the mean current of approximately 1.5 for the peak current, .7 for the fundamental frequency component,

FIGURE 4

COLLECTOR CURRENT VS. V'_{BE} AND TEMPERATURE

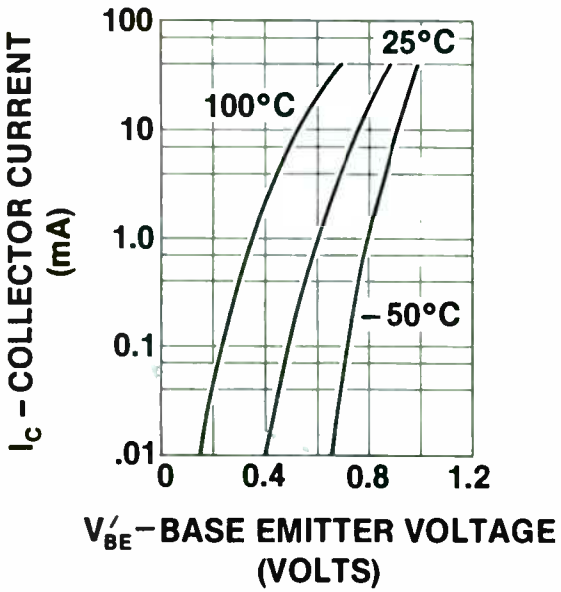
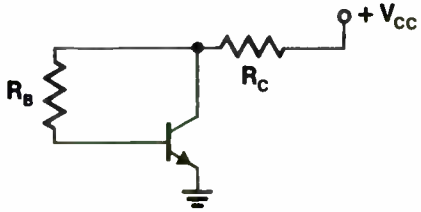


FIGURE 5

EVEN FOR SIMPLE BIAS CIRCUITS THE EQUATIONS BECOME COMPLICATED



- $$Sh_{FE} = \frac{h_{FE}R_C + R_B + h_{IE} + R_C)\,(V_{CC} - V'_{BE} + KI_{CBO})}{(h_{FE}\,R_C + R_B + h_{IE} + R_C)^2}$$

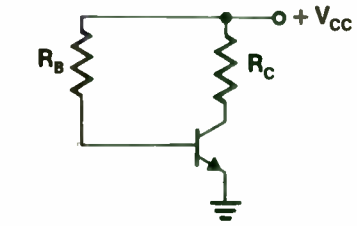
$$- R_C \left[\frac{(h_{FE}\,(V_{CC} - V'_{BE} + KI_{CBO}) + KI_{CBO})}{(h_{FE}R_C + R_B + h_{IE} + R_C)^2} \right]$$

Where: $K = h_{IE} + R_B + R_C$

- GOT ALL THAT?

FIGURE 6

FIXED BIAS



- $$I_C = \frac{h_{FE}\,(V_{CC} - V'_{BE})}{R_B}$$
- $$Kh_{FE} = 1$$
- $$KV'_{BE} = \frac{1}{(1 - \frac{V_{CC}}{V'_{BE}})}$$

ADVANTAGE: FEW COMPONENTS,
DISADVANTAGE: INFERIOR TEMPERATURE STABILITY, LARGE I_C VARIATIONS

.3 for the second harmonic, and less than .1 for the third harmonic.

Our large signal model now can be easily obtained by adjusting the values of the small signal equivalent circuit. As previosuly indicated, the voltage dependent capacitors should be essentially doubled.

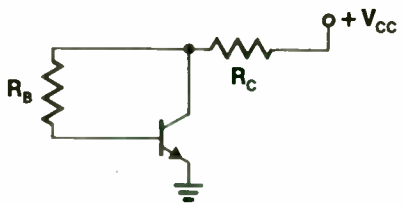
Practical Application

The recent trend to develop oscillators with dielectric stabilizers shall be picked up here and our example shall be developed around it. Figure 6 shows the equivalent circuit of a dielectric resonator oscillator. The entire circuit is described in a circuit file for CADEC 4 using the parallel resonator approach for the dielectric resonator. The LCR values have been determined from th definition of physics. The transmission line terminated with 50 ohms is set at quarter wavelengths for best coupling and the transmission line into the emitter of the transistor is set at approximately quarter wavelengths as the parallel resonant condition of the dielectric resonator transforms into approximately 2 ohm resistive output resistance into the emitter of the transistor. The circuit can therefore be redrawn as shown in Figure 7. To meet the requirements for oscillation the combination of internal and external feedback has to provide the necessary phase shift and this oscillator circuit can be made unstable to meet the approximate criteria by optimizing the inductance betwen base and ground while allowing for the resistive feedback in the emitter at large DC currents. This feedback will reduce the gain band width product of the oscillator. Figure 8 shows the measured resonant character of the dielectric of the DRO of the function using an HP8510 network alanyzer. This permits measurement of the Q of the resonator. Figures 9 and 10 show the close-in purity of the oscillator; and Figure 11 shows the single side band phase noise. I will deal with the noise calculation in a future paper. The maximum output power is achieved by matching the output impedance calculated from P out $=\frac{(.9 \times VCE)^2}{2P \text{ out}}$.

The maximum available output power can be determined from the Fourier coefficient of the fundamental current and the voltage swing across the transistor. The output matching stub guarantees 50 ohms matching. By selecting the feedback properly, superior noise performance can be obtained if matching for best noise figure and best output power is done by adjusting the emitter transmission line lengths slightly offset to the dielectric resonator coupling. CADEC 4 allows one to do such analysis and the details on optimum noise matching will be shown in the following paper. Table 1 shows the circuit listing for the CADEC circuit file. Note the statement NAB, which stands for Noise Analysis Begin; and the #300 refers to the noise temperature of 300° Kelvin. Table 2 shows the listing of the results. Please note that S22 magnitude at 4GHz is approximately 100.

FIGURE 7

VOLTAGE FEEDBACK BIAS



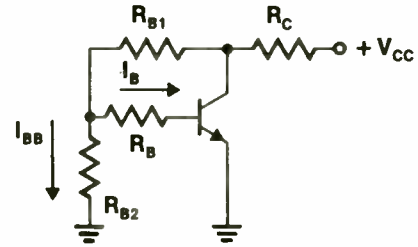
- $I_C = \dfrac{h_{FE}(V_{CC} - V_{BE})}{R_B + h_{FE}R_C}$
- $Kh_{FE} = \dfrac{1}{\left(1 + \dfrac{h_{FE}R_C}{R_B}\right)}$
- $KV_{BE} = \dfrac{1}{\left(1 - \dfrac{V_{CC}}{V_{BE}}\right)}$

ADVANTAGE: SAME AS FIXED BIAS, PLUS BETTER TEMPERATURE STABILITY

DISADVANTAGE: A HIGH R_C/R_B RATIO IMPROVES Kh_{FE}, BUT LOW VALUES OF R_B ARE DIFFICULT TO ACHIEVE

FIGURE 8

VOLTAGE FEEDBACK AND CONSTANT BASE CURRENT SOURCE



- $I_C = h_{FE}\left[\dfrac{-V'_{BE}A - R_{B2}V_{CC}}{R_BA + R_{B2}(h_{FE}R_C + R_C + R_{B1})}\right]$
- $KV_{BE} = \dfrac{1}{\left(1 - \dfrac{V_{BB}}{V'_{BE}}\right)}$

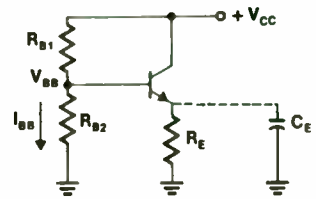
Where: $A = R_{B1} + R_{B2} + R_C$

ADVANTAGE: SAME AS VOLTAGE FEEDBACK PLUS CAN BE MADE h_{FE} INSENSITIVE BY SELECTING $I_{BB} > I_B$

DISADVANTAGE: MORE PARTS

FIGURE 9

EMITTER RESISTOR FEEDBACK



- $I_C = \dfrac{(V_{BB} - V'_{BE})h_{FE}}{h_{FE}R_E + R_B}$
- $Kh_{FE} = \dfrac{1}{\left[1 + \dfrac{h_{FE}R_E}{R_B}\right]}$
- $KV'_{BE} = \dfrac{1}{\left[1 - \dfrac{V_{BB}}{V'_{BE}}\right]}$, $SV'_{BE} = \dfrac{-1}{R_E}$

Where: $R_B = R_{B1} \parallel R_{B2}$

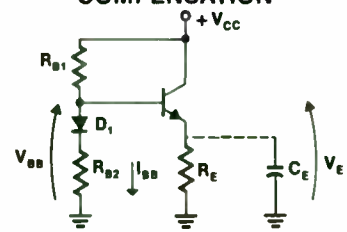
$V_{BB} = \left[\dfrac{R_{B2}}{R_{B1} + R_{B2}}\right] V_{CC}$

ADVANTAGE: VERY STABLE WHEN $h_{FE}R_E \gg R_B$, FEW PARTS

DISADVANTAGE: ADDED INDUCTANCE CAUSED BY R_E AND C_E

FIGURE 10

DIODE TEMPERATURE COMPENSATION



- $SV_{BE} = \dfrac{-1}{R_E\left(1 + \dfrac{R_{B1}}{R_{B2}}\right)}$
- $V_E = V_{BB} - V_{BE}$

$= \dfrac{R_{B2}}{R_{B1} + R_{B2}} V_{CC} + \left[\dfrac{R_{B1}}{R_{B1} + R_{B2}} V_D - V_{BE}\right]$

- FOR TEMPERATURE INDEPENDANCE OF I_C VS V_{BE} THEN:

$$\left[\frac{R_{B1}}{R_{B1} + R_{B2}} V_D - V_{BE}\right] = 0$$

THEN:

$$V_E = \frac{R_{B2}}{R_{B1} + R_{B2}} V_{CC}$$

ADVANTAGE: STABILIZES I_C AGAINST V_{BE} CHANGES

DISADVANTAGE: EMITTER NOT GROUNDED, REQUIRES MORE PARTS

Figure 12 shows a plot of the noise figure and the gain due to the Q multiplier effect, the noise figure gets the unusual curve based on matching for maximum output power rather than best noise figure. Figure 13 shows the noise and gain circles for the circuit configuration chosen.

Conclusion

To predict the output power at microwave frequencies and analyze the phase noise of the oscillator, specifically for MESFETs, more modern techniques like load pulling or Harmonic Balance methods have been developed. It was shown in this paper that by using a somewhat cruder approach for first approximation using bipolar transistors, fairly good understanding of the mechanism is possible. More experimental results and noise theory will be presented in a forthcoming paper.

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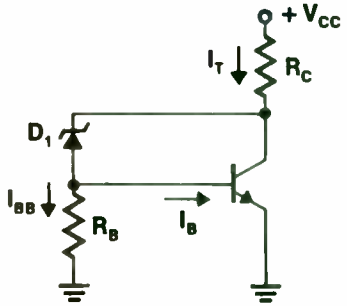
(2) R. Gilmore, "Design of a Novel FET Frequency Doubler Using a Harmonic Balance Algorithm," Schlumberger, Houston, TX, presented June 3, 1986 at 1986 IEEE MTT-S International Microwave Symposium, Baltimore, Maryland, June 2-4, 1986.

(3) Kenneth M. Johnson, "Large Signal GaAs MESFET Oscillator Design," IEEE Transactions on Microwave Theory and Techniques, Vol. MTT 27, No. 3, March 1979.

(4) Hiroyuki Abe, "A GaAs MESFET Oscillator Quasi-Linear Design Method," IEEE Transactions on Microwave Theory and Techniques, Vol MTT-34, No. 1, January 1986.

FIGURE 11

ZENER DIODE BIAS

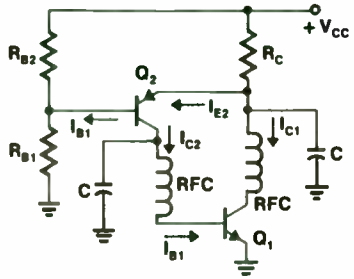


- $V_Z = V_{CE} - V'_{BE}$
- $R_C = \dfrac{V_{CC} - V_{CE}}{I_T}$
- $R_B = \dfrac{V'_{BE}}{I_{BB}}$

ADVANTAGE: EMITTER GROUNDED MORE STABLE THAN WITH A RESISTOR IN PLACE OF THE ZENER
DISADVANTAGE: NOISY

FIGURE 12

ACTIVE BIAS CIRCUIT



- $I_{C1} = \dfrac{h_{FE1}\left[\dfrac{R_{B2}}{R_{B1}+R_{B2}} V_{CC} - V'_{BE2}\right]}{(1+h_{FE1})R_C + R_B/(1+h_{FE2})}$

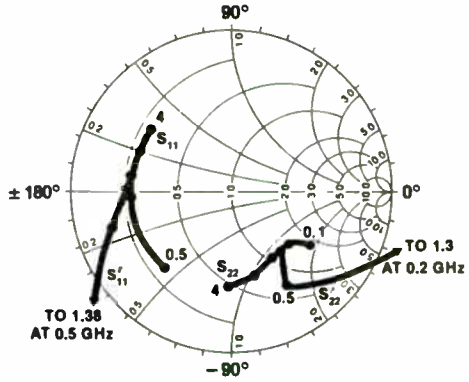
WHERE: $R_B = R_{B1} \| R_{B2}$

- If $(1+h_{FE1})R_C > \dfrac{R_B}{(1+h_{FE2})}$ THEN
- $I_{C1} = \dfrac{h_{FE1}}{(1+h_{FE1})}\left[\dfrac{\dfrac{R_{B2}}{R_{B1}+R_{B2}} V_{CC} - V'_{BE2}}{R_C}\right]$

ADVANTAGE: EMITTER GROUNDED, VERY STABLE, LOW POWER CONSUMPTION
DISADVANTAGE: USES THE GREATEST NUMBER OF PARTS, LOW FREQUENCY OSCILLATIONS POSSIBLE

FIGURE 13

EFFECT OF POOR EMITTER RESISTOR BYPASS



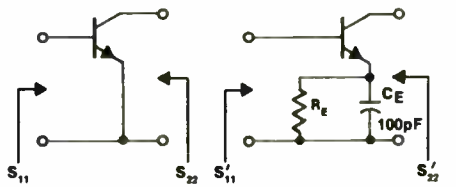
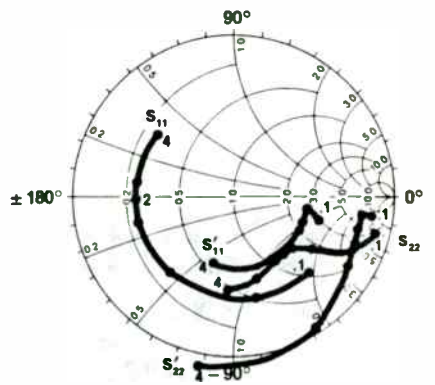
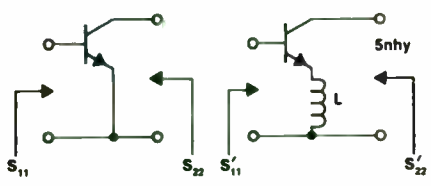


FIGURE 14

EFFECT OF EMITTER INDUCTANCE





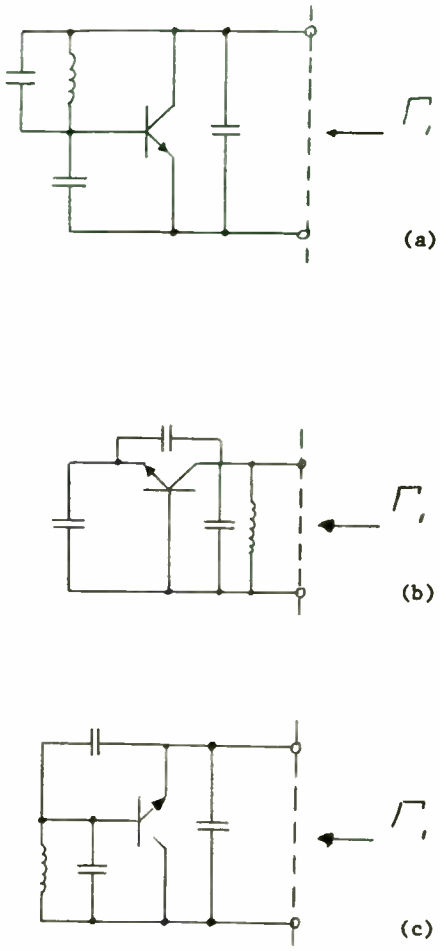


FIGURE 1

A range of possible oscillator circuits.

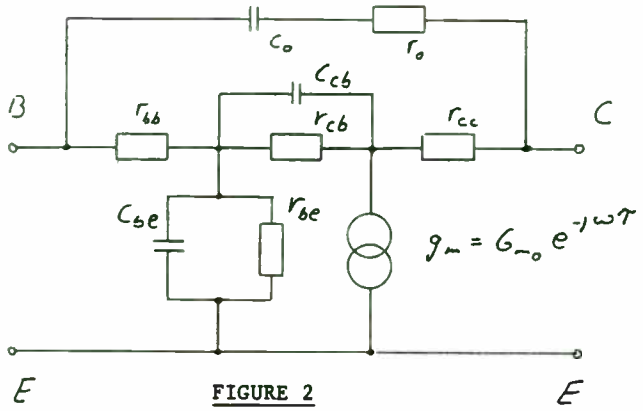


FIGURE 2

Equivalent circuit for a bipolar transistor.

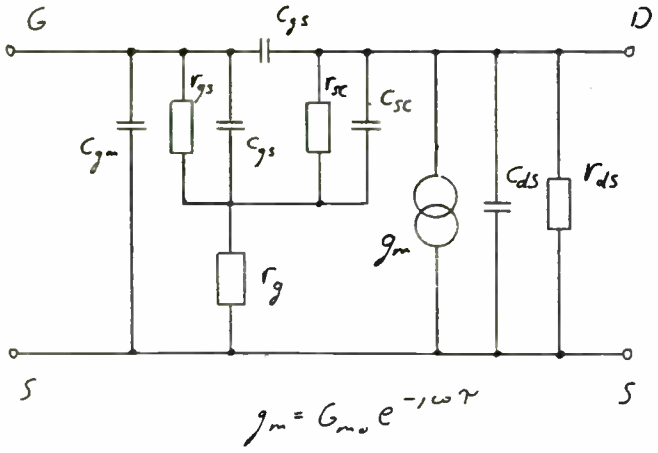


FIGURE 3

Equivalent circuit for a MESFET, including extensions to HEMPT.

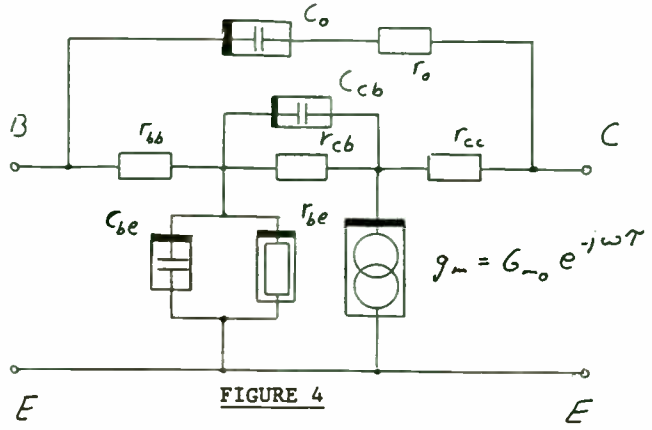


FIGURE 4

Large signal components in the equivalent circuit of a bipolar transistor.

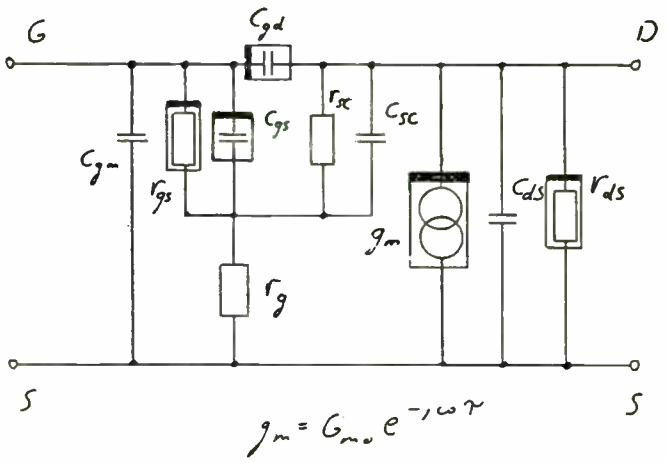


FIGURE 5

Large signal components in a field effect transistor.

PRACTICAL WIDEBAND RF POWER TRANSFORMERS, COMBINERS, AND SPLITTERS

by

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INTRODUCTION

This paper will deal with the practical aspects of designing and building wideband RF power transformers, combiners (or hybrids), and splitters. Emphasis will be on topology. A consistent approach to represent these transformers pictorially and schematically with equivalent circuits showing source and load connections will be developed to help provide an intuitive understanding of the devices. Laboratory test data comparing various designs and topologies is included.

Modern solid state HF power amplifiers are required to operate over increasingly wider bandwidths and at higher power levels for applications in communications as well as electronic countermeasures. Wideband RF power transformers are required for coupling into and out of the solid state devices. The conventional or so-called "wire-wound" transformer and two topologies of the transmission line transformer (conventional and equal delay) are presented.

A wideband RF power combiner (or hybrid) is required to achieve output levels above the capabilities of a single solid state amplifier stage. The RF outputs of two or more identical amplifier modules can be combined to reach these higher powers. Design examples of in-phase, 180-degree, and quadrature combiners are detailed. Two basic topologies for in-phase and 180-degree combiners are presented.

A wideband RF power splitter (or divider) is simply a combiner or hybrid used in reverse. The splitter topology is the same as a combiner, however splitters are usually operated at lower power levels. The discussion centers around combiners but is equally applicable to power splitter applications.

TRANSFORMERS

The bandwidth of rf transformers does not refer to the usual -3 dB points since in power applications this represents an unacceptable loss. Typical HF amplifier designs require operation from 2 to 30 MHz and sometimes lower to 1.6 MHz. The transformer losses must be as low as possible over this operational bandwidth. Transformer losses translate to heat that must be removed as well as extra power that must be supplied by the transistors (at the collector/drain efficiency) and ultimately by the power supply (at its conversion efficiency). A few tenths of a dB of unnecessary loss in output

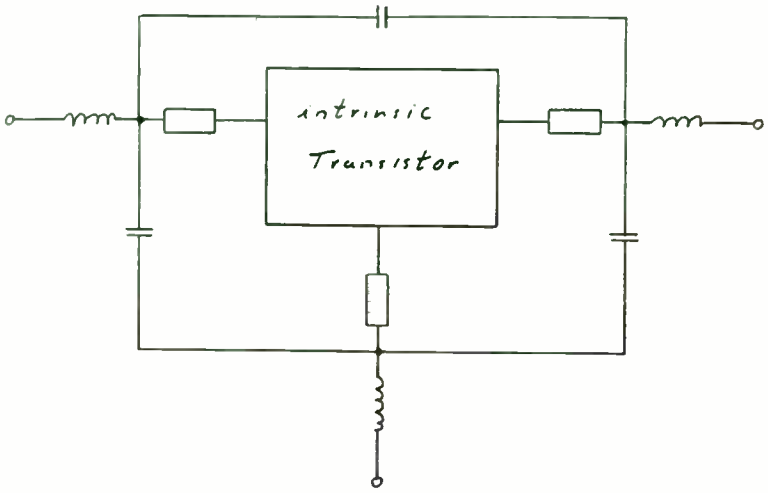


FIGURE 6

Influence of the packaging to the "intrinsic" transistor.

FIGURE 7

Equivalent circuit of oscillator.

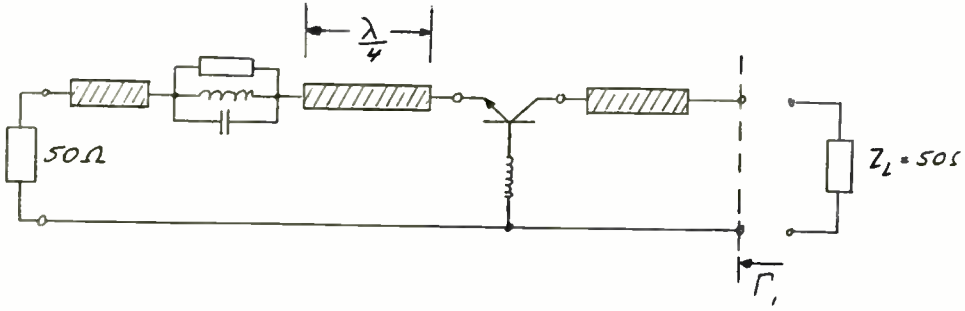


FIGURE 8

Measured response of a dielectric resonator at 4GHz.

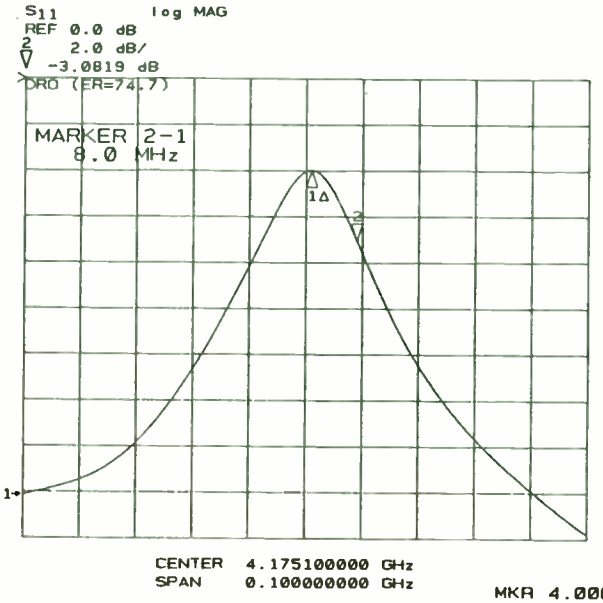
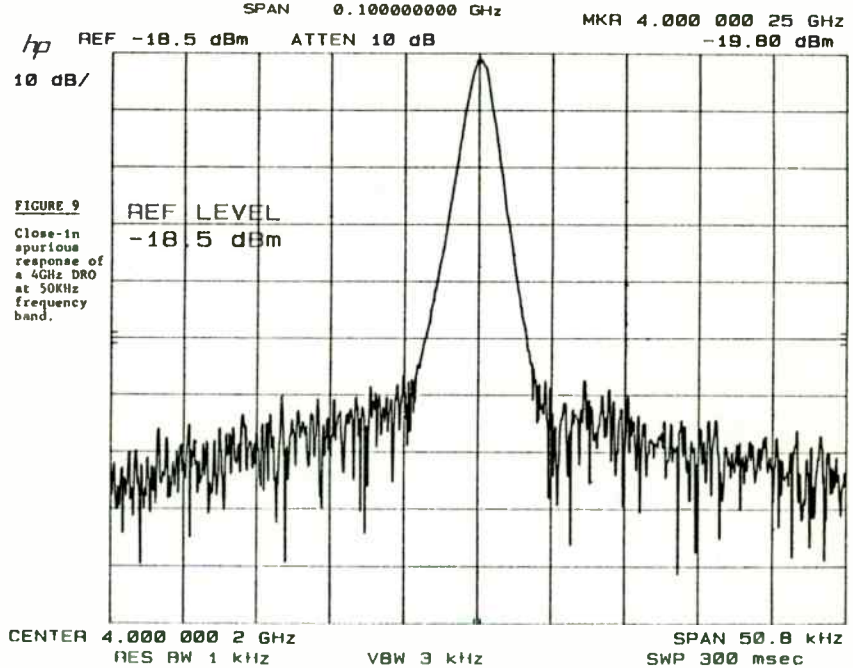


FIGURE 9

Close-in spurious response of a 4GHz DRO at 50KHz frequency band.



transformers or combiners can mean significant increases in primary power consumption.

New RF power FET devices have operational bandwidths of 1 to 175 MHz making possible extended range amplifiers covering HF and the lower VHF frequencies. Transformer designs covering over six octaves of bandwidth are required.

A wideband RF power transformer performs one or more of any combination of three basic functions:

(a) Impedance transformation

(b) Balanced to unbalanced transformation

(c) Phase inversion

Transformation of a secondary load to a desired load impedance at the primary of the transformer is the most common function. RF transformers are often referred to by their impedance transformation ratio rather than primary to secondary turns ratio. The former is simply the turns ratio squared. In this application, we are most often interested in manipulating impedances rather than voltages or currents with the transformers. Balanced-to-unbalanced transformers, commonly termed "Baluns" are extremely useful in wideband amplifier designs. A single-ended load can be driven by a push-pull (balanced) source or vice-versa by using a balun transformer. A wideband transformer can also perform a phase reversal from primary to secondary by proper winding connections.

Transformer connections between a source and a load may be either balanced or unbalanced. Additionally, the balanced source or load may be either entirely floating or with center grounded such as two single ended sources phased 180-degrees apart or a load resistor with grounded center tap. The distinction between "balanced, floating" and "balanced, center grounded" may seem unimportant for wideband transformer design, but it is not. A proposed balun transformer equivalent circuit with source and load connected should be drawn showing the magnetization current path.

Figure 1 (a) is an example of a simple 1:1 balun with a floating balanced load. The magnetization current, i_m, flows through the load resistor as shown. Figure 1 (b) illustrates what happens to the magnetization current path if the balanced load is changed to a balanced, center tap grounded load. The magnetization current flows through only one winding and only one-half of the load resistance. This causes undesirable phase and amplitude imbalance in the balun restricting the bandwidth. The balance can be restored by using a third or tertiary winding, as shown in figure 1 (c), to shunt the magnetization current around the load. This illustrates the necessity of considering the type of source and load connections when selecting wideband transformer topologies.

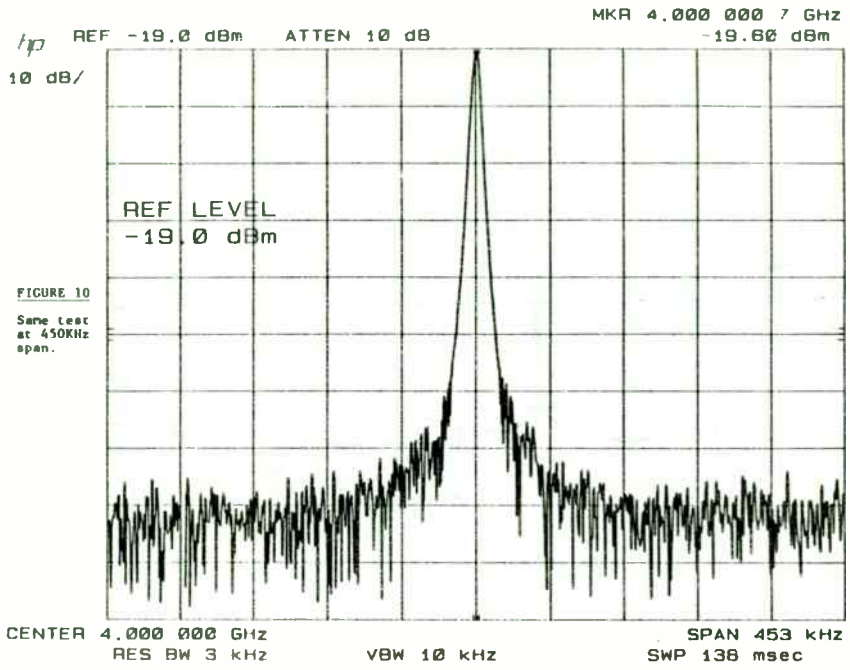


FIGURE 10

Same test at 450KHz span.

FIGURE 11

Single side band phase noise of the oscillator under phase locked condition to improve close-in noise.

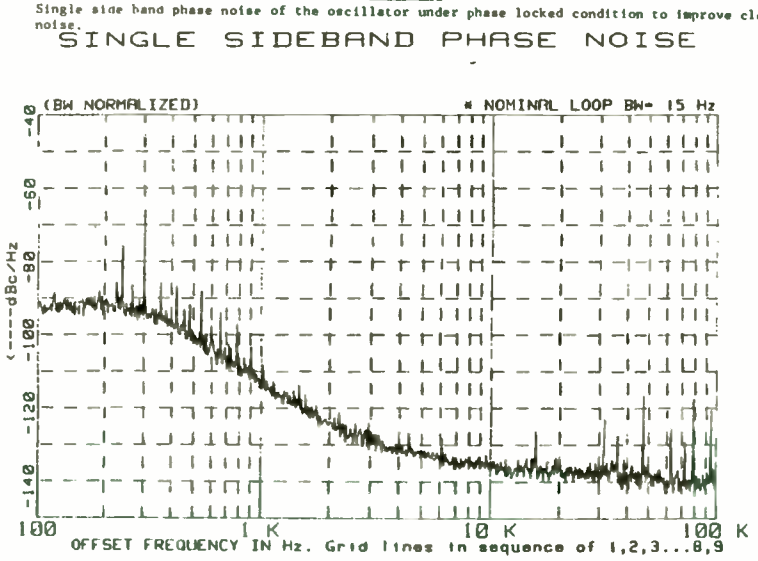


FIGURE 12

Noise and gain as a function of frequency

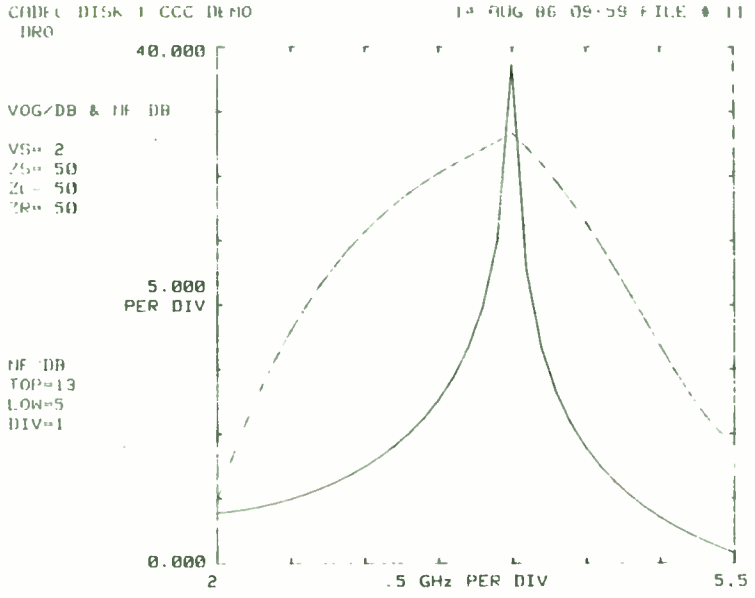
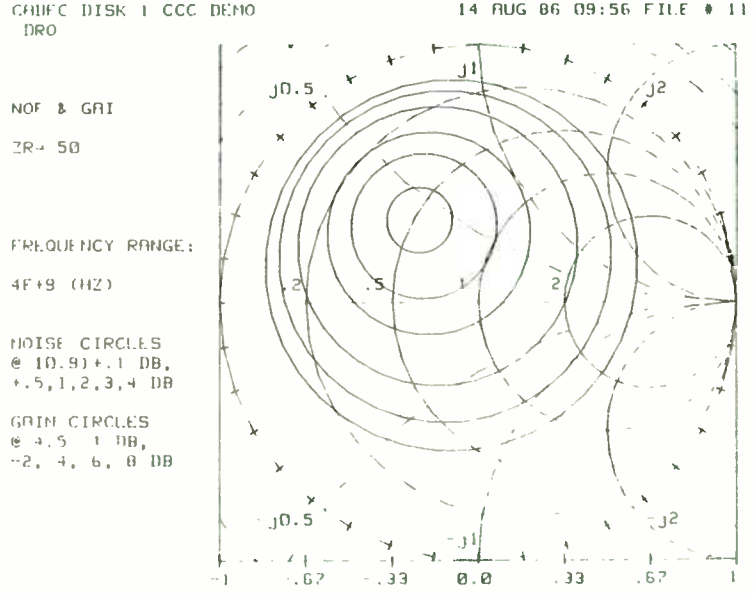
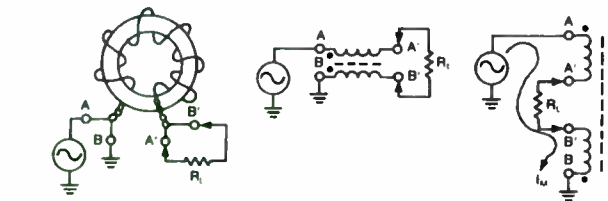


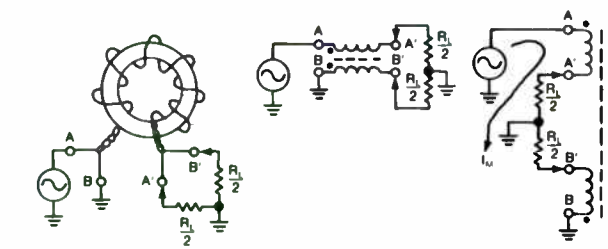
FIGURE 13

Noise and gain circles.

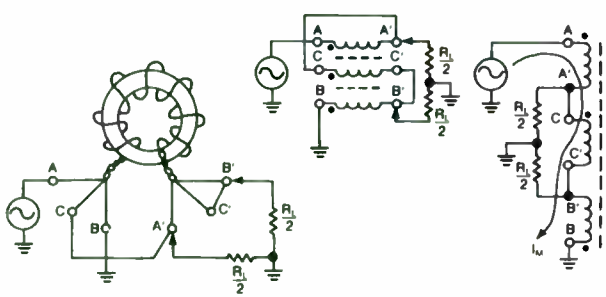




(A) BALANCED LOAD, FLOATING



(B) BALANCED LOAD, CENTER GROUNDED



(C) BALANCED LOAD, CENTER GROUNDED WITH TERTIARY WINDING (C-C')

FIGURE 1 1:1 TRANSMISSION LINE BALUN TRANSFORMERS

The nine possible transformer connections are given below:

SOURCE	LOAD
Unbalanced	Unbalanced
Unbalanced	Balanced, floating
Unbalanced	Balanced, center grounded
Balanced, floating	Unbalanced
Balanced, floating	Balanced, floating
Balanced, floating	Balanced, center grounded
Balanced, center grounded	Unbalanced
Balanced, center grounded	Balanced, floating
Balanced, center grounded	Balanced, center grounded

Wideband RF transformers and combiners typically use a magnetic core. The magnetic cores used in wideband RF transformers are available in a wide variety of shapes and sizes. Balun core, toroidal, sleeves, tubes, beads, and cup cores are the common names for the various shapes. The earliest material used was powdered iron followed by modern ferrites. Ferrite is composed of iron oxide in combination with various proportions of oxides of manganese, magnesiun, nickel, and zinc. In general the ferrites composed of iron, nickel, and zinc are applicable for the HF/VHF frequencies. Various mixes of ferrites are available. A high permeability and moderately low loss material is used for HF/VHF power transformers. Operational flux densities must be kept well within the linear portion of the B-H curve of the material. The area inside the

TABLE 1

```
CADEC DISK # 1 CCC DEMO                13 AUG 86 21:27 FILE # 11
    FRI DRO
  1: SRC           2V  50ohm
  3: TER           50ohm
  4: LFR           2GHz  6GHz  100MHz
    REM  OPT   S22/M =100/1
    REM  SFR          4GHz
  7: NAB           290K
  8: RS            50ohm
    .CON  0  0  1
  9: CAB           .1mm  50ohm
    .CON  1  0  2
 11: LIS           795.774pH  500  4GHz  4GHz
    .CON  2  0  3
 15: CS            19.894pF
    .CON  2  0  3
 16: CAB           17.5mm  50ohm
    .CON  3  0  4
 18: LS            500pH
    .CON  4  0  5
    REM  TRB          20  10GHz  30mA
    OLD R_BIP
    .XIG
    .CON  5  6  7
 19: LS            344.010382111pH(1a/10n)
    .CON  6  0  0
    TWO  1  7
    .OUT VOG/DB   K/M    S22/M   NF/DB
```

TABLE 2

```
Loading OLD R_BIP:,707,0
5GHZ_BIP

CADEC DISK # 1 CCC DEMO                12 AUG 86 21:29 FILE # 11

 DRO
 VG= 2  ZS= 50  ZL= 50  ZR= 50
```

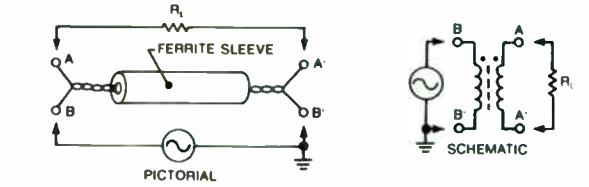
FREQUENCY/HZ	VOG/DB	K/M	S22/M	NF/DB
2.0000E9	3.8834	-1.7910	1.3326	5.9668
2.1000E9	3.9953	-2.0137	1.4080	6.6199
2.2000E9	4.1620	-2.1896	1.4901	7.1993
2.3000E9	4.3795	-2.3280	1.5801	7.7163
2.4000E9	4.6465	-2.4360	1.6795	8.1795
2.5000E9	4.9639	-2.5186	1.7901	8.5957
2.6000E9	5.3342	-2.5792	1.9145	8.9703
2.7000E9	5.7616	-2.6207	2.0557	9.3078
2.8000E9	6.2517	-2.6448	2.2180	9.6119
2.9000E9	6.8123	-2.6530	2.4071	9.8858
3.0000E9	7.4539	-2.6466	2.6310	10.1321
3.1000E9	8.1902	-2.6265	2.9009	10.3536
3.2000E9	9.0404	-2.5935	3.2338	10.5526
3.3000E9	10.0312	-2.5485	3.6561	10.7314
3.4000E9	11.2015	-2.4922	4.2113	10.8926
3.5000E9	12.6114	-2.4253	4.9762	11.0387
3.6000E9	14.3600	-2.3487	6.1014	11.1727
3.7000E9	16.6285	-2.2629	7.9264	11.2980
3.9000E9	19.8063	-2.1689	11.4104	11.4184
3.9000E9	25.0126	-2.0673	20.7047	11.5391
4.0000E9	38.6398	-1.9590	98.8514	11.6661
4.1000E9	22.5771	-1.8358	15.4591	11.4400
4.2000E9	16.6318	-1.6967	7.7296	11.1960
4.3000E9	13.1829	-1.5457	5.1390	10.9048
4.4000E9	10.7703	-1.3860	3.8399	10.5977
4.5000E9	8.9298	-1.2205	3.0571	10.2664
4.6000E9	7.4540	-1.0518	2.5321	9.9131
4.7000E9	6.2318	-.8819749	2.1541	9.5410
4.8000E9	5.1969	-.7129069	1.8660	9.1546
4.9000E9	4.3061	-.5461834	1.6431	8.7557
5.0000E9	3.5298	-.3831572	1.4610	8.3644
5.1000E9	2.8468	-.2249662	1.3101	7.9791
5.2000E9	2.2411	-.0725551	1.1827	7.6172
5.3000E9	1.7006	.0733075	1.0733	7.2949
5.4000E9	1.2156	.2120132	.9782942	7.0313
5.5000E9	.7783439	.3430991	.8949142	6.8471
5.6000E9	.3824293	.4662352	.8211659	6.7629
5.7000E9	.0225103	.5812119	.7555744	6.7975
5.8000E9	-.3059532	.6879287	.6970482	6.9660
5.9000E9	-.6068647	.7863835	.6447851	7.2804
6.0000E9	-.8836193	.8766621	.5982061	7.7519

B-H curve represents the relative loss, therefore the narrow curves are preferred for low loss designs. Detailed information is available from the various ferrite manufacturers.

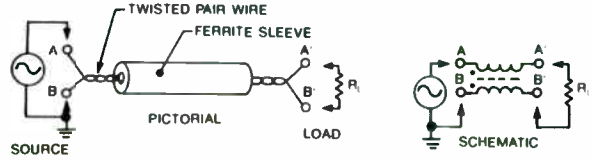
Core losses and winding dielectric losses heat the core. The core temperature must be held well below the Curie temperature of the ferrite, otherwise the magnetic properties of the ferrite will be permanently altered. Operation near the Curie temperature is not recommended as some materials can go into thermal runaway. The high temperature increases the core loss which in turn further increases the core temperature until the core is ruined.

CONVENTIONAL OR "WIRE-WOUND TRANSFORMERS"

The conventional broadband RF transformer is characterized by a power transfer from the primary to secondary windings via magnetic coupling through the ferrite core. The transmission line transformer, by contrast, is characterized by the use of a transmission line of characteristic impedance, Z_O, and a ferrite core. The core suppresses common mode or non-transmission line currents which would otherwise flow due to the transmission line interconnections. A core wound with wire may or may not be a conventional transformer, depending upon how the source and load are connected. Figure 2 illustrates this distinction.



(A) CONVENTIONAL OR "WIREWOUND" TRANSFORMER (1:1 BALUN)



(B) TRANSMISSION LINE TRANSFORMER (1:1 BALUN)

FIGURE 2 COMPARISON OF CONVENTIONAL AND TRANSMISSION LINE TRANSFORMERS

In general, the conventional transformer is inferior to the transmission line transformer for the combination of high power capability, low loss, and wide bandwidth. The conventional transformer can be constructed for a wider range of impedance transformation ratios than the transmission line type. Some ratios will have wider bandwidths than others due to the number of turns to achieve the desired turns ratio. There are no fractional turns. If the wire or line passes through the core, it is one turn.

APPENDIX

We mentioned briefly that the oscillator amplitude stabilizes due to some nonlinear performance of the transistor. There are various mechanisms involved, and depending on the circuit, several of them are simultaneously responsible for the performance of an oscillator. Under most circumstances, the transistor is operated in an area where the dc bias voltages are substantially larger than the ac voltages. Therefore, the theory describing the transistor performance under these conditions is called "small-signal theory". In a transistor oscillator, however, we are dealing with a feedback circuit that applies positive feedback. The energy that is being generated by the initial switch-on of the circuit is being fed back to the input of the circuit, amplified, and returned to the input again until oscillation starts. The oscillation would theoretically increase in value unless some limiting or stabilization occurs. In transistor circuits, we have two basic phenomena responsible for limiting the amplitude of oscillation.

1. Limiting because of gain saturation and reduction of open-loop gain.
2. Automatic bias generated by the rectifying mechanism of either the diode in the bipolar transitor or in the junction field-effect transistor. In MOSFETs an external diode is sometimes used for this biasing.
3. A third one would be external AGC, but it will not be considered here

The oscillators we discuss here are self-limiting oscillators.

The self-limiting process, which by generating a dc offset bias moves the operating point into a region of less gain, is generally noisy. For very low noise oscillators, this operation is not recommended. After dealing with the quarter-wavelength oscillator in the preceding section, we will deal here only with the negative resistance oscillator, in which, through a mechanism, a negative resistance is generated due to feedback and is used to start oscillation with the passive device. Here we look at what is happening inside the transistor that is responsible for amplitude stabilization, and we will thus be in a position to make a prediction regarding the available energy and the harmonic contents.

Figure A-1 shows the quarter-wavelength oscillator redrawn in such a way that the source electrode is now at gorund potential while the gate and drain electrode are electrically hot. The reason for doing this is because we will look at the gate-to-source transfer characteristic and use its nonlinearities as a tool to describe what is happening. The same analysis can be applied to a transistor circuit, provided that the resistors used for dc bias are small enough not to cause any dc offset. The field-effect transistor characteristic follows a square law and, therefore, can be expressed as

$$i_2 = I_{DSS}\left(1 - \frac{V_1}{V_p}\right)^2 \qquad \text{(A-68)}$$

Figure 3 is a conventional transformer that finds wide usage at low impedances (3 to 20 ohms). The core is commonly referred to as a balun core, yet the transformer may or may not be connected to perform as a balun. Metal sleeves of copper or brass are inserted into the core and connected together at one end to form a primary winding. Connections to the circuit are made at each of the two sleeves at the opposite end. Two pieces of copper clad G-10 circuit board work nicely at each end. The secondary winding is constructed by winding the required turns of insulated wire through the primary tubes.

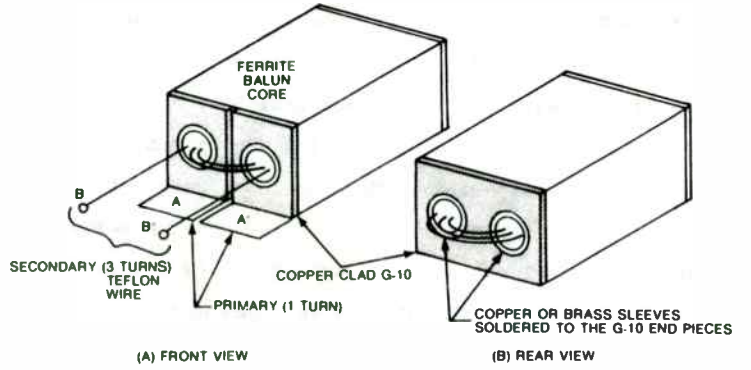


FIGURE 3. EXAMPLE OF A 1:9 IMPEDANCE RATIO CONVENTIONAL TRANSFORMER

One of the factors limiting the high frequency response of the transformer is leakage inductance. Leakage inductance is due to any flux lines that do not link the primary and the secondary. To minimize the leakage inductance, the primary copper tubes should fit quite close in the core holes. They should not be so tight that thermal expansion will cause the core to break. The lead inductances of the primary and secondary windings from the point they exit the core to the circuit connection will also limit performance at the high frequency end, especially on low impedance applications. Shunt capacitance on either the primary or secondary or both will compensate the leakage reactance and extend the useful high frequency limit.

TRANSMISSION LINE TRANSFORMERS

The simplest transmission line transformer is a quarter-wavelength line whose characteristic impedance, Z_o, is chosen to give the correct impedance transformation. This relationship is illustrated in figure 4. Note that this transformer is a narrowband device valid only at frequencies for which the line is odd multiples of a quarter wavelength. The transformation ratio is given by the square of the ratio of the line impedance to the load connected to the line.

For any other device, we have to take the necessary transfer characteristic into consideration, and this could theoretically be done by changing the square law into nth order. The voltage v_1 will be in the form

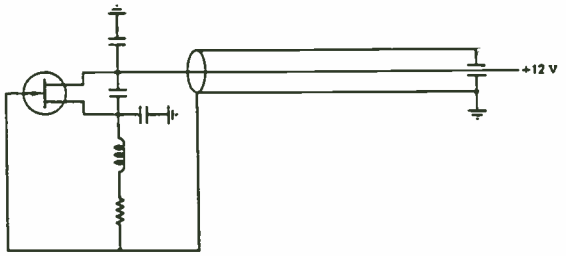


Figure A-1 Quarter-wavelength oscillator with grounded source electrode.

$$v_1 = V_b + V_1 \cos\omega t \tag{A-69}$$

This is the voltage that is being generated due to the selectivity of the tuned circuit at which there is a resonant frequency. Inserting this into the above equation and using

$$V_x = V_p - V_b \tag{A-70}$$

we obtain

$$i_2 = \frac{I_{DSS}}{V^2}\left(V_x^2 - 2V_x V_1 \cos\omega t + V_1^2 \cos^2\omega t\right) \tag{A-71}$$

Once we know the peak value of i_2, we can expland this into a Fourier series. In this case a Fourier series expansion for i_2 has only three terms; that is,

$$i_2(t) = I_o + I_1 \cos\omega t + I_2 \cos 2\omega t \tag{A-72}$$

$$I_o = \frac{I_{DSS}}{V^2} V_x^2 + \frac{V_1^2}{2} \tag{A-73}$$

$$I_1 = -2\frac{I_{DSS}}{V_p^2} V_x V_1 \tag{A-74}$$

$$I_2 = \frac{I_{DSS}}{V^2} \frac{V_1^2}{2} \tag{A-75}$$

Because of the square-law characteristic, I_1 is a linear function of V_1 and we can define a large-signal average transconductance G_m,

$$G_m = \frac{I_1}{V_1} = -2\frac{I_{DSS}}{V_p^2} V_x \tag{A-76}$$

In the case of the square-law characteristic, we find the interesting property that the small-signal transconductance g_m at any particular point is equal to the large-signal average transconductance G_m at the same point. The second harmonic distortion is the output current is given by

$$\frac{I_2}{I_1} = \frac{V_1}{4V_x} = \frac{V_1}{4V_p} \frac{g_{mo}}{g_m} \tag{A-77}$$

The transconductance G_m can be defined in such a way that it indicates the gain for a particular frequency relative to the fundamental, which means that there is a certain G_m for the fundamental frequency and one for the second harmonic, and in the general case, a G_{mn} for the nth-order harmonic. In the more general form, we rewrite our equation

$$i_d = C_n(-V_b + V_1 \cos x)^n \tag{A-78}$$

As this current will exist only during the period from $-\alpha$ to $+\alpha$, the equation

$$-\alpha < x < +\alpha$$

exists only for

$$i_2 = 0$$

$$x = \pm\alpha$$

$$\cos\alpha = \frac{V_b}{V_1}$$

We can rewrite our equation for the drain current or collector current of a transistor:

$$i_d = C_n V_1^n (\cos x - \cos\omega)^n \tag{A-79}$$

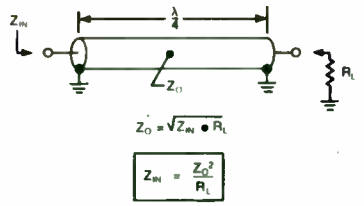


FIGURE 4. SIMPLE QUARTER WAVE TRANSMISSION LINE TRANSFORMER

If a ferrite sleeve is added to the transmission line (see figure 5), common mode currents (currents flowing in both transmission line conductors in phase and in the same direction) are suppressed and the load may be balanced and floating above ground. The line can now be any length with characteristic impedance equal to the balanced load impedance. The result is a 1:1 balun. Low frequency operation is limited by the amount of impedance offered to common mode currents. A good rule-of-thumb requires the impedance presented to common mode currents be not less than five times the load impedance. The line length limits the high frequency response of transmission line transformers.

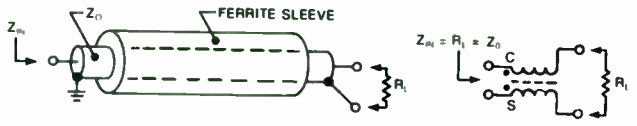


FIGURE 5. 1:1 TRANSMISSION LINE BALUN

If the ferrite loaded length of transmission line in figure 5 is folded back so that the two ends may be interconnected, a 1:4 impedance transformer is formed. A load resistance, R_L, connected as shown in figure 6 is reflected to the input of the transformer as $R_L/4$. The line Z_O should be equal to the geometric mean of R_L and Z_{in} for maximum bandwidth. The line length must be as short as possible for extended high frequency operation. The practical high frequency limit for this type of transformer is reached when the line length approaches 1/8 wavelength and appreciable phase error difference occurs at the interconnection of the lines.

A 1:4 transmission line balun transformer may be constructed as shown in figure 7. Two cores are required and may be either balun cores (as shown) or toroids or sleeve cores. The transmission line Z_O should be the geometric mean of the input and load impedances. This transformer may also be used for balanced-to-balanced source and load connections. Transmission line baluns for 1:9 and 1:16 impedance ratios are constructed similarly as shown in figures 8 and 9. The limitation of squared integer transformation ratios is the biggest disadvantage of this type of transmission line transformer. The availability of coaxial cable in a variety of impedances is another limitation. 50 and 75-ohm cables are by far the most common but impedances of 25, 35, 60, 95, and 125-ohms are available.

The dc value of the current

$$I_d = \frac{1}{\pi}\int_o^{\pi} i_d \, dx \qquad \text{(A-80)}$$

or

$$I_d = \frac{C_n V_1}{\pi}\int_o^{\pi}(\cos x - \cos x)^n \, dx \qquad \text{(A-81)}$$

The amplitude of the fundamental frequency

$$I_1 = \frac{2}{\pi}\int_o^{\pi} i_d \cos x \, dx \qquad \text{(A-82)}$$

or

$$I_1 = \frac{2C_n V_1^n}{\pi}\int_o^{\pi}(\cos x - \cos\alpha)^n \cos x \, dx \qquad \text{(A-83)}$$

For n = 1, the collector current

$$I_d = C_1 V_1 A_1 \qquad \text{(A-84)}$$

and the amplitude of the fundamental frequency

$$I_1 = C_1 V_1 B_1 \qquad \text{(A-85)}$$

For n = 2, the collector current is therefore

$$I_d = C_2 V_1^2 A_2 \qquad \text{(A-86)}$$

and the amplitude of the fundamental frequency

$$I_1 = C_2 V_1^2 B_2 \qquad \text{(A-87)}$$

With the definition of the conduction angle,

$$\alpha = \text{arc}\,\frac{V_b}{V_1} \qquad \text{(A-88)}$$

These values are listed in Table A-3.

TABLE A-3 NORMALIZED FOURIER COEFFICIENTS

$\frac{V_b}{V_1}$	A_1	B_1	$\frac{B_1}{A_1}$	A_2	B_2	$\frac{B_2}{A_2}$
0	0.318	0.500	1.57	0.250	0.425	1.7
0.1	0.269	0.436	1.62	0.191	0.331	1.73
0.2	0.225	0.373	1.66	0.141	0.251	1.78
0.3	0.185	0.312	1.69	0.101	0.181	1.79
0.4	0.144	0.251	1.74	0.0674	0.126	1.87
0.5	0.109	0.195	1.79	0.0422	0.0802	1.90
0.6	0.077	0.141	1.83	0.0244	0.0458	1.95
0.7	0.050	0.093	1.86	0.0118	0.0236	2
0.8	0.027	0.052	1.92	0.0043	0.0082	2
0.9	0.010	0.020	2	0.00074	0.00148	2
1.0	0	0	2	0	0	2

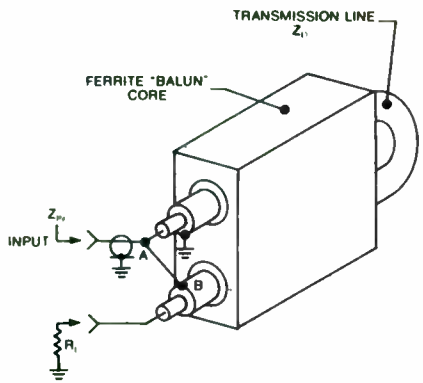
These are the normalized Fourier coefficients as a function of n and the conduction angle. Theoretically, this has to be expanded to the order n of 3 or 4, depending on the particular device, and can be found from tables or by a digital computer.

For simplifications, let us go back to the case of our square-law device, where our transconductance

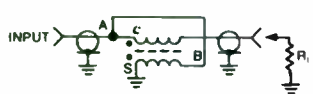
$$G_m = \frac{I_1}{V_1} = -2\frac{I_{DSS}}{V_P^2} V_x \qquad \text{(A-89)}$$

This can be rewritten in the form

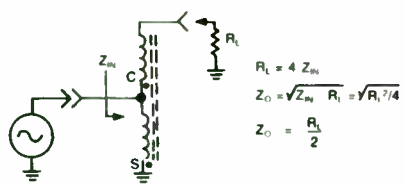
$$G_m = \frac{2I_{DSS}}{V_P^2}\left(V_P - V_b + V_i \cos\omega t\right) \qquad \text{(A-90)}$$



(A) PICTORIAL VIEW

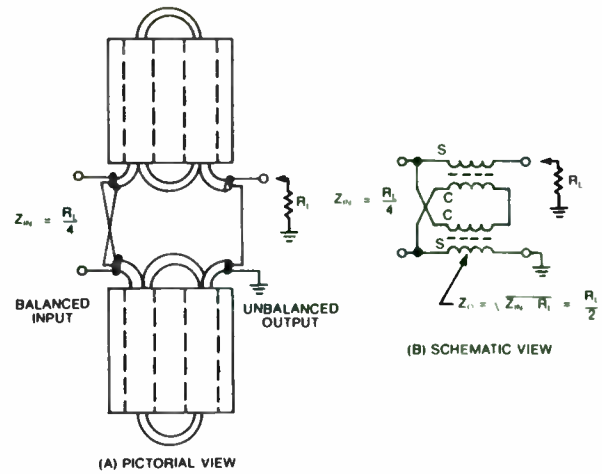


(B) SCHEMATIC



(C) EQUIVALENT CIRCUIT

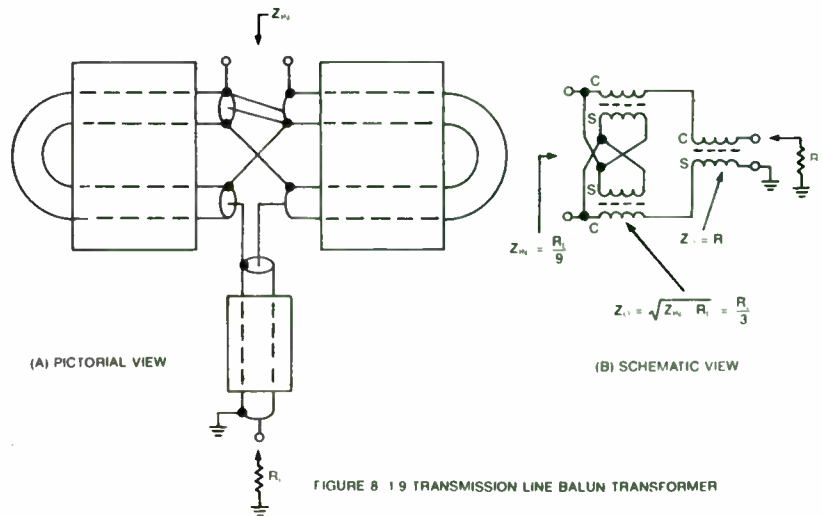
FIGURE 6 TRANSMISSION LINE TRANSFORMER, 4 1 UNBALANCED-TO-UNBALANCED



(A) PICTORIAL VIEW

(B) SCHEMATIC VIEW

FIGURE 7. 1:4 TRANSMISSION LINE BALUN TRANFORMER



(A) PICTORIAL VIEW

(B) SCHEMATIC VIEW

FIGURE 8. 1:9 TRANSMISSION LINE BALUN TRANSFORMER

V_p is the pinch-off voltage of the field-effect transistor, V_b is the bias voltage that is measured between source and ground, and V_1 is the peak value of the voltage of the fundamental frequency. Figure A-2 shows the effect where the sine wave is driving the transfer characteristic, and the resulting output currents are narrow pulses. Based on the duration, the mutual conductance g_m becomes a fraction of the dc transconductance G_m, and therefore the gain is reduced. For small conduction angles $I_n | I_d$, the mutual conductance can take very small values, and therefore the gain gets very small; that is the cause for stabilizing the amplitude in the oscillator. We note that the gain is being reduced as the amplitude causing the small conduction angle is increased.

Fourier analysis indicates that, for a small harmonic distortion, the RF voltage at the source or gate (depending on where it is grounded) has to be less than 80 mV. Now we can design the oscillator performance.

Let us assume that the saturation voltage of the active device is 2 V, battery voltage applied to the transistor is 12 V, and the transistor starts at a dc current of 10 mA with a source resistor of 200Ω. This results in a voltage drop of 1 V at the source and 2 V in the device; therefore, 9 V is available. It can be assumed that the maximum voltage at the drain will be $9 \times \sqrt{2}$. The capacitor voltage divider from drain to voltage now depends on the gain. If we assume an $I_n | I_d$ of 0.15 for about 50° conduction angle, 2α, and the dc conductance of the transistor at

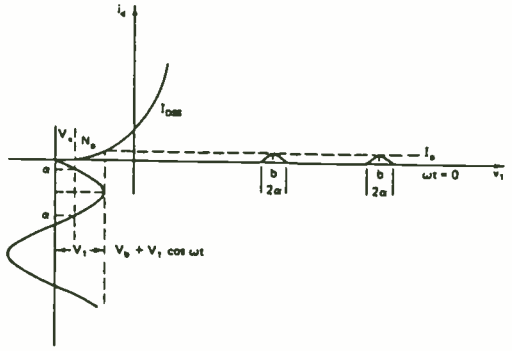


FIGURE A-2 Current tips as a function of narrow conduction angles in a square-wave transfer characteristic.

the starting dc operating point is 20 mA|V, the resulting transconductance is 3 mA|V.

Next we need the output impedance the quarter-wave resonator provides,

$$R_L = Q\frac{1}{\omega C}(250\ \text{MHz})$$

or

$$R_L = 600\frac{1}{2\pi \times 47 \times 10^{-12} \times 250 \times 10^6} = 8127\Omega$$

As we want 9 V rms at the output, we have to use the equation

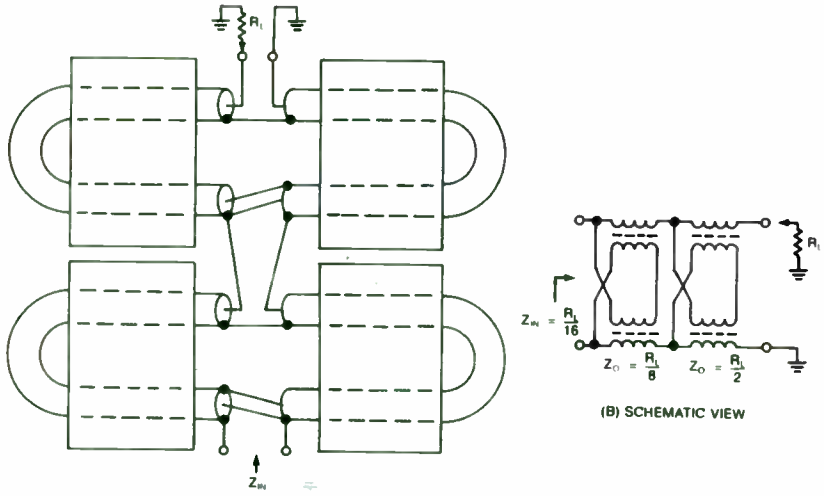
$$\frac{V_{out}}{V_{in}} = A(\text{voltage gain}) = g_m R_L = 3 \times 10^{-3} \times 8.127 \times 10^3$$

$$A = 24.38$$

or

$$V_{in} = \frac{8V}{A} = 328\text{mV}$$

This would mean that the capacitance ratio of the feedback capacitors C_1 and C_2 would be 1:24.38. In practice we will find that this is incorrect, and we need a 1:4 or 1:5 ratio. The reason for this is that the equations we have used so far are not



(A) PICTORIAL VIEW

(B) SCHEMATIC VIEW

FIGURE 9. 1:16 TRANSMISSION LINE BALUN TRANSFORMER

Several techniques to achieve nonstandard impedance lines include simply parallel connecting two or more lines. For example, two parallel 50-ohm lines provide an effective 25-ohm line. The parallel lines do not have to be the same impedance either. Bifilar or twisted enameled wire can easily be constructed for odd characteristic impedances also. The impedance depends upon the wire diameter, insulation dielectric, spacing, and number of twists per unit length. Multiples of even numbers of wire may be twisted together and then parallel connected to achieve low characteristic impedances. The characteristic impedance of experimentally constructed bifilar or twisted pair transmission lines may be determined by measuring the reactance of an open circuit, 1/8-wavelength, sample. The magnitude of the reactance is equal to the line impedance at the frequency for which the line is 45-degrees in electrical length. Remember to account for the velocity of propagation when determining the frequency of 1/8 wavelength.

Micro-strip transmission lines on printed circuit boards is another technique for achieving virtually any desired line impedance. Mechanical problems with the strip lines in ferrite cores may be more difficult but interconnections with the amplifier circuit may be improved.

The bandwidth degradation experienced by not using the correct value of line impedance may be acceptable in some applications. Figure 10 is a comparison of two identical 1:4 balun transformers; one wound with the proper 25-ohm line, the other wound with 50-ohm line. The measurement was made by connecting two identical transformers back-to-back to provide matched 50-ohm impedance ports to interface with the network analyzer. The indicated loss of one transformer is half of the measured value. This technique is valuable for evaluating various transformer designs and initially chooseing values of compensation capacitors for leakage reactance.

accurate enough to represent the acutal dc shifts and harmonic occurrences. As mentioned in Sections 4-1 and A-1-5 a certain amount of experimentation is required to obtain the proper value. To determine the actual ratio, it is recommended that one obtain from the transistor manufacturer the device with the lowest gain and build an oscillator testing it over the necessary temperature range. As the gain of the transistor changes as a funciton of temperature (gain increases as temperature decreases for field-effect transistors and acts in reverse for bipolar transistors), a voltage divider has to be chosen that is, on the one hand, high enough to prevent the device from going into saturation which will cause noise, and on the other hand, small enough to allow oscillation under worst-case conditions. Suitable values were determined for the CP643 transistor and shown in the circuit for the field-effect quarter-wavelength transistor.

--See Chapter A-1-6, "Oscillator Amplitude Stabilization," from Digital PLL Frequence Synthesizers, pp. 400-405. Copyright, Dr. Ulrich L. Rohde.

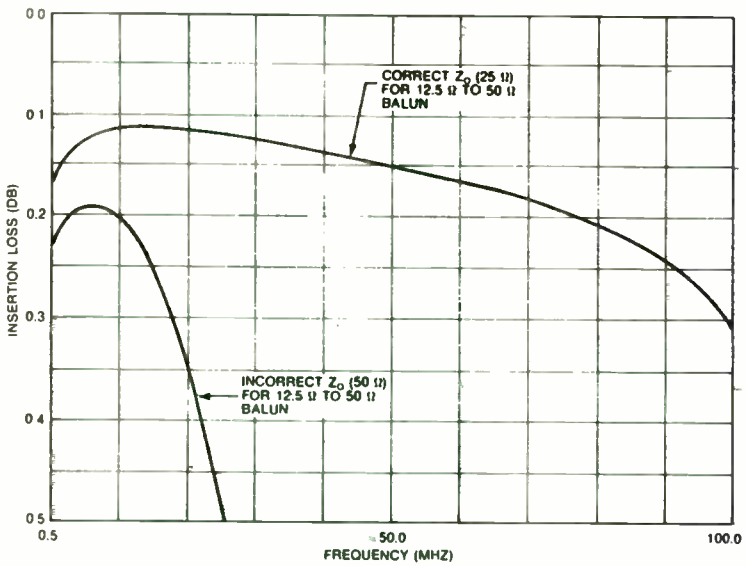


FIGURE 10. COMPARISON OF EFFECT OF Z_O ON 1:4 BALUN TRANSFORMER

As pointed out earlier, the 1:4 transmission line transformers' high frequency response is limited when appreciable phase error is introduced at the interconnection point a-b shown in figure 11. If the connection a-b were made with a transmission line of equal impedance and length as the ferrite loaded line, the phase difference between input and output is eliminated. The transformer topology remains the same, except the a-b connection has the same phase delay as the main transformer line. For this reason this subclass of transmission line transformers are called "Equal Delay Transmission Line Transformers". The transformer input and output connections can be physically separated which is advantageous in some applications.

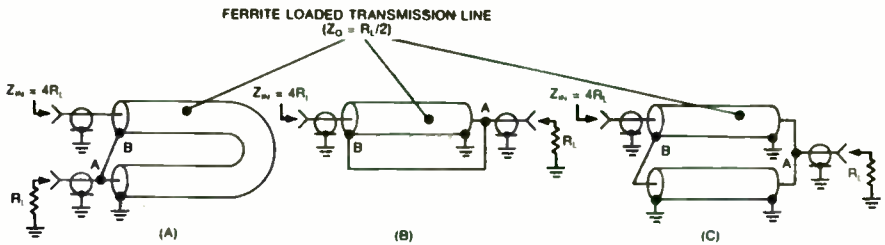


FIGURE 11. DERIVATION OF THE EQUAL DELAY TRANSFORMER

Figure 12 (a) is the usual pictorial and schematic representation of a 1:4 equal delay transformer. If a third line is stacked on the 1:4 design, a 1:9 impedance transformer results. In like manner, four lines produce a 1:16 transformer and so on. Figure 12 (b) and (c) illustrates these ratios. For comparison, if one unit of ferrite is required on the 1:4 transformer for a given bandwidth, then two units will be required for the third line on the 1:9 transformer. In like manner, the fourth line requires three units of ferrite for the same bandwidth. Notice that these designs are all unbalanced-to-unbalanced transformers. Suppose we add ferrite to the bottom line on the 1:4 transformer. Now we can lift the grounds on the parallel connected end (still keeping the shields

Logarithmic Amplifiers

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Radio first started with just a simple detector. Some early users complained that this lacked sensitivity. The next step was to add a linear amplifier. Then the problem was strong signals, which occasionally required an alert hand on the gain control to avoid severely overloading the receiver. The immediate solution was an automatic finger on the gain reduction control, but AGC systems had problems with choices for time constants, occasionally causing inappropriate responses.

With the advent of radar at the start of WW II the job of the IF amplifier became more demanding. The origin of the problem can be seen in the radar range equation below.

$$S = \frac{PG^2\sigma\lambda^2}{(4\pi)^3R^4}$$

S = received power

P = transmitted power

G = antenna gain (ratio, not dB)

σ = target radar cross section (area)

λ = wavelength

R = range

The troublsome term is the $1/R^4$ factor. Since the received signal varies as $1/R^4$, a 2:1 change in range leads to a 12 dB change in signal. A radar with a maximum range of 32 miles will normally be expected to resolve the same target at less than 1 mile. A 32:1 range variation gives a 96 dB signal variation. Linear amplifiers with such dynamic range are not currently practical.

One solution to this problem is a swept gain IF amplifier strip. Predictive information is available on the returning radio echo. The time of arrival is directly proportional to the range. If we make the gain of the amplifier time variant so that the gain is proportional to T^4 (T = time elapsed since the transmission of the outgoing pulse) then the IF strip output amplitude should be constant for a particular target at all ranges.

The swept gain method allows wide dynamic range while maintaining the fine amplitude resolution of a linear amplifier. The problem is that swept gain deals poorly with "surprises". A large target can easily paralyse the amplifier. If the recovery time is 1 us, then any object less than 250 feet behind the large reflector will be hidden. The swept gain IF will also fail to pick up small targets, even when they are close in. Surface skimming anti-ship missles are an example of this class of low radio reflection objects.

Limiting amplifiers, which level the output of the IF to a fixxed amplitude, are useful in radars where frequency or phase information is of interest. Doppler and MTI sytems are examples. A limiting IF requires a separate detector system to retain received signal amplitude information if needed.

connected) and connect a balanced, floating load between the center conductors and the shields to form a 1:4 balun. The stray capacitance to ground can be balanced better by interconnecting the center conductor of one coax to the shield of the other coax. The result is the balun transformer described earlier in figure 7.

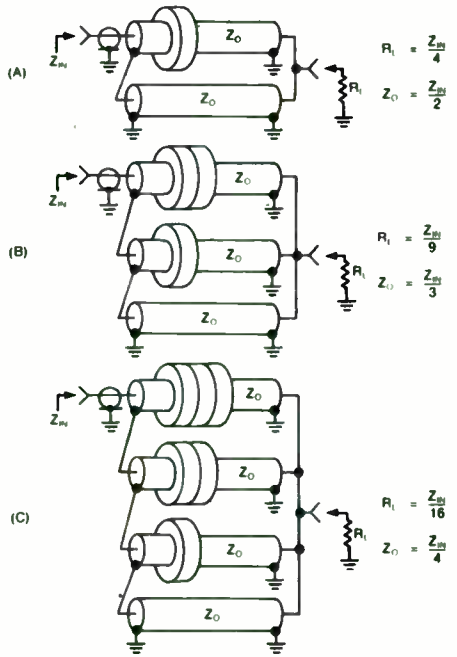


FIGURE 12. EQUAL DELAY TRANSFORMER CONFIGURATIONS

How much improvement in bandwidth does the equal delay transformer give compared to the conventional transmission line transformer? Figure 13 is a plot of insertion loss versus frequency for the two types constructed on identical cores. Again, the test consisted of measuring two identical transformers connected back-to-back, so the actual loss for one transformer is one-half the measured value.

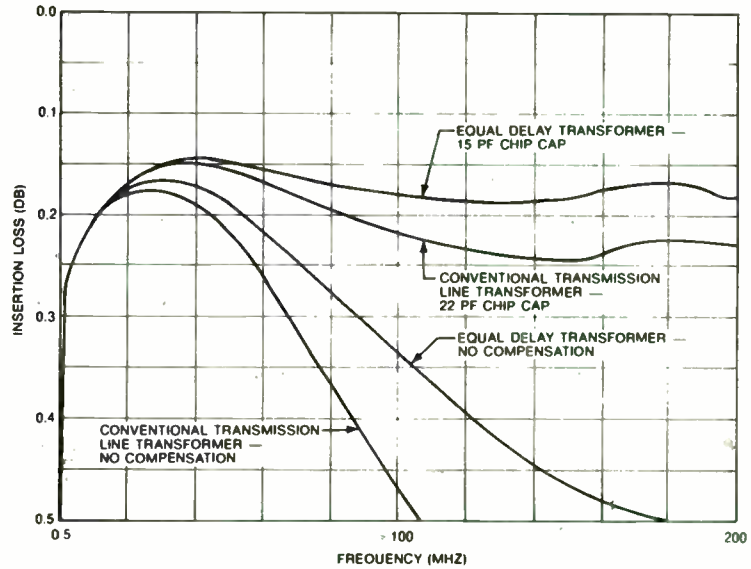


FIGURE 13 BANDWIDTH COMPARISONS OF CONVENTIONAL AND EQUAL DELAY 1:4 TRANSMISSION LINE TRANSFORMERS

In the demanding environments of radar, sonar and ECM rapid pulse repetition and amplitude variation cannot be dealt with by the normal AGC loops used in AM and SSB radio systems, because these depend on the continuous nature of the carrier. New techniques used to avoid interception and jamming involve wider use of the electromagnetic spectrum, frequency agility, and pulse compression or dispersion. Such systems require broadband IF amplification that responds instantaneously.

The common technique to achieve the instantaneous compression of dynamic range is to use a logarithmic amplifier. This gives an output voltage that is proportional to the logarithm of the input. Compare this to the case of linear amplifiers where output voltage is proportional to input voltage and to limiting amplifiers where amplitude information is removed by leveling the output.

The important characteristic of a log amp system is its huge instantaneous dynamic range and resulting fast response time. This has advantages over AGC systems where a fixed time constant is optimised to meet predicted variations in amplitude. Sophisticated AGC variations are bulky and expensive. The typical result is a loss of amplitude information if the time constant is too large.

When is a logarithmic amplifier IF system the best choice? The electronics industry sees requirements for instantaneous amplitude compression of input signals in many specialized receiver systems. In a typical log amplifier strip an input dynamic range of 80 dB can be compressed to about 20 dB by the logging action. The output can then be easily processed by succeeding circuitry.

When is a log amp inappropriate? When input amplitude is an important component of the desired information. In applications like radar signature analysis, terrain mapping radar, and terrain following radar linear amplifiers are often used. Logarithmic amplifiers sacrifice amplitude precision for dynamic range, so a linear amplifier will provide superior resolution in these systems.

TYPES OF LOG RECEIVER SYSTEMS

Receivers that accept pulsed signals, such as those used in radar and ECM, tend to use two techniques to step down the signal to a manageable frequency. The heterodyne mixer is widely used in search radar. The crystal video (or microwave detector) is seen on broadband warning and direction finders. Figure 1 shows schematically the essential output signal differences of the logarithmic signal processing employed with these techniques.

(1) LOG VIDEO SYSTEMS

Log video amplifiers are used in systems requiring simplicity, compactness and low price. These systems lack the sensitivity and dynamic range achieved by successive

COMBINERS AND SPLITTERS

When required output power levels exceed the capabilities of a single power amplifier stage, two or more stages or modules are combined to produce the required output. The combiner is closely related to wideband transformers in design and techniques. A power splitter is simply a lower powered version of the combiner used in reverse. The splitter divides the drive signal into multiple equal amplitude outputs to be applied to the amplifier inputs. The power combiner then recombines the amplified outputs into a single signal. Since the splitter is the same as a combiner, the following discussion will mention only combiners.

A wideband power combiner must perform the following basic functions:

a. Provide low insertion loss over the required bandwidth.

b. Provide isolation (minimum coupling) between the input ports.

c. Provide a low VSWR load at the input ports over the required bandwidth.

The operating bandwidth of combiners must be as wide or wider than the amplifiers to not restrict the overall bandwidth of the transmitter. Transmission line techniques are used for lowest loss and widest bandwidth. The primary function of the combiner is to maintain port-to-port isolation. By isolating the output of one amplifier from the others, multiple failures as a result of a single amplifier failure are avoided. For example, in a two-input-port combiner, if one amplifier is disabled the output power drops by 6 dB. The output drops 3 dB due to lack of power from the disabled module and an additional 3 dB is due to the power from the remaining module dividing equally between the bridging resistor and the output load.

The bridging resistor must dissipate -6 dB of the maximum combiner output power. The bridging resistor value is prescribed by the type and configuration of the combiner as detailed later. Some topologies require either single-ended or balanced, floating bridging resistors. Sometimes the bridging resistor is referred to as the "dump" load or "dump" port since power due to phase or amplitude imbalance is dumped to this load.

The bridging resistor dissipates power due to any slight differences in either the phase or amplitude of the input signals. This relationship is given in figure 14.

There are three basic types of combiners:

a. In-phase combiner or hybrid (two or more input ports)

b. 180-degree combiner or hybrid (two input ports)

c. 90-degree combiner or quadrature hybrid (two input ports)

detection and true log amplifiers. Log video amplifiers perform the logging function directly on the video signal from a microwave detector. It is worth noting that although it is possible to get a log video amplifier system with a dynamic range of 80 dB, the overall system dynamic range is reduced to half by the square law of the detector. Log video sytems are employed in direction finders, alarm systems and other less sensitive measurement equipment.

(2) TRUE LOG SYSTEMS

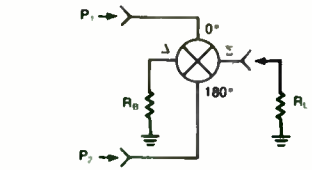
The second system works from a mixer and is for applications where both sensitivity and minimal frequency distortion in the IF are required. True log amplifiers have a undetected, undistorted IF output of amplitude approximating the logarithm of the input amplitude. Stages can be cascaded to give up to 80 dB of dynamic range. A dual-gain technique is used to obtain the log transfer function. Figure 2 shows such a stage, consisting of a limiting amplifier of gain G in parallel with a unity gain amplifier. This is in fact a hybrid between a linear and a limiting amplifier in form as well as function.

The single stage soft limiting dual-gain characteristic is shown in Figure 3. For small input signals the gain is around 10 dB. The gain drops to unity when the input signal reaches the saturation point of the limiting amplifier part of the stage. The delays can be matched in the unity gain and limiting amplifier portions of the stage to minimize frequency distortion and phase error. The theoretical transfer function of a six stage true log system is shown in figure 4, plotted with both axes linear. It is a series of straight lines with breakpoints where each limiting amplifier saturates. The practical characteristic is curved, giving reduced ripple and less log error. Low ripple is dependent on component matching. An eight stage strip with an 80 dB dynamic range is possible.

(3) SUCCESSIVE DETECTION LOG SYSTEMS

Successive Detection is the most commonly used log IF amplification system. To meet the required dynamic range, identical limiting amplifiers with logarithmic detectors are cascaded. The parallel sum of their detected outputs produce a composite logarithmic straight line transfer function.

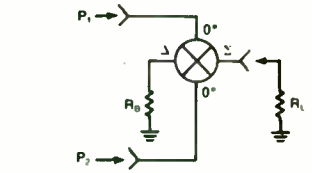
The basic stage in a successive detection strip is shown in Fig. 5. A limiting amplifier of 10 dB gain is followed by a low level detector. The single stage response is shown in Fig. 6. An important feature is that the video and RF outputs limit at a precise input level. A three stage strip built with circuits of this type is shown in Fig. 7. The first stage will give a video output identical to a single device. The second is constant so when a logarithmic scale is used for the RF input the second stage video output will be identical to that of the first stage just displaced to the



$P_{RL} = \frac{P_1 + P_2}{2} - \sqrt{P_1 \cdot P_2} \cos \phi$; WHERE ϕ IS DIFFERENCE IN PHASE BETWEEN INPUT PORT SIGNALS

$P_{RB} = P_1 + P_2 - P_{RL}$

(A) 180-DEGREE HYBRID COMBINER



$P_{RL} = \frac{P_1 + P_2}{2} + \sqrt{P_1 \cdot P_2} \cos \phi$; WHERE ϕ IS DIFFERENCE IN PHASE BETWEEN INPUT PORT SIGNALS

$P_{RB} = P_1 + P_2 - P_{RL}$

(B) IN-PHASE HYBRID COMBINER

FIGURE 14 HYBRID COMBINER POWR RELATIONSHIPS

If more than two signals are combined in-phase, the term "combiner" is used since the term "hybrid" refers to a device with two input ports. The topologies of each of the three basic configurations will be examined.

The following definitions apply:

R_L= output load resistance

R_B= bridging resistor

Z_O= transmission line characteristic impedance

Z_{in}= input impedance (with output port terminated)

S = shield connection of coaxial cable

C = center connection of coaxial cable

IN-PHASE COMBINERS

In-phase combiners operate with two or more inputs of equal phase and amplitude to combine into a single output. There are two basic topologies for in-phase combiners, examples of which are shown in Figures 15 and 16. The differences are in the number and configurations of the ferrite cores and the value of the bridging resistor. The type-I configuration has a single balun core or toroidal core and a bridging resistor equal to four times the output load. The type-II combiner has two separate cores; either sleeves or toroidal. The bridging resistor is equal to the load resistance. Consideration of physical layout, practical transmission line impedances (Z_O), and bridging resistance (R_B) will determine the best type of combiner for a particular design.

A comparison of input impedance and port-to-port isolation between typical type-I and type-II combiners yields interesting results as shown in Figure 17. Both combiners were constructed with a single turn of 50-ohm coax in the cores. Core material was Stackpole 7D for both types. The test data indicates superior port-to-port isolation with a type-II combiner while the type-I combiner exhibited lower input VSWR.

left by the stage gain, as shown in Fig. 8. This shows the individual transfer characteristics of the three cascaded stages separated by the gain of each limiting amplifier. A 10 dB increase in signal will drive number three detector to its maximum output and similar increases will sequentially saturate D2 and then D1.

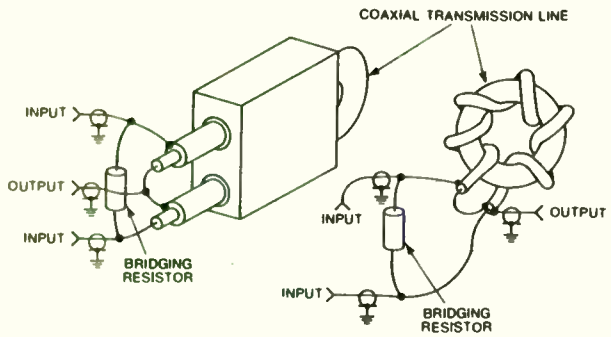
The final step is to sum the video outputs. The schematic and corresponding response are shown in Fig. 9. For each increase in input level corresponding to a single stage gain, a contribution equal to the maximum video output from a single stage is added to the summed video output. To obtain a straight log law, stages must be well matched, particularly the detector characteristic and the flatness of the limiting level.

Successive detection log strips give amplification, great sensitivity (-80 dBm), and large dynamic range. They are widely used in marine radars, I.F.F. systems, primary surveillance radars, missile radars, navigation aids, instrumentation, etc.. Their only disadvantage is that the signal phase and frequency information is degraded.

The dynamic range of a log strip can be extended by increasing the number of stages. The limit is reached when the last stage in the cascade reaches full video output solely on the noise produced by the first stage. The number of stages can be increased if the bandwidth of the strip is reduced. It is common practice to insert a bandpass filter in the centre of the log strip for this purpose. Care must be taken that the filter insertion loss is 0 dB or the log response of strip will have a "kink" in the middle of the response curve. Another technique for increasing the dynamic range is to attenuate the input signal and apply it to another short strip operating in parallel to the main strip. The video output from this "lift" strip is added to that from the main strip. Normally the log response limits when the input signal exceeds that necessary to produce full video output from the first stage. The lift strip is fed with an attenuated signal and will continue to give an output change. The limit to this technique is reached when the input voltage is sufficient to cause damage or overload in the first stage of the main strip.

The Plessey SL2521 is a monolithic IC approach to the successive detection log amplifier. The features that make it unique are an improved bandwidth over previous IC amps, 1.3 GHz, and the ability to simultaneously give both a log linear successive detection video output and a phase linear limited IF output. This previously required two separate IF strips, a successive detection log strip for video information and a limiting strip for phase information. When cascaded into a six stage strip the result is 60 dB dynamic range, 600 MHz video detection bandwidth, and 450 MHz IF bandwidth with low phase error.

The monolythic approach offers advantages over and above its combined excellence in both phase and amplitude accuracy.



(A) PICTORIAL VIEW, BALUN CORE & TOROIDAL CORE

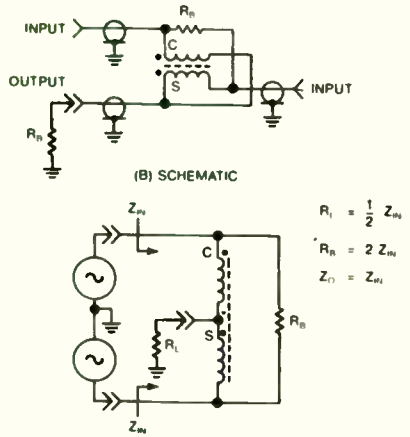
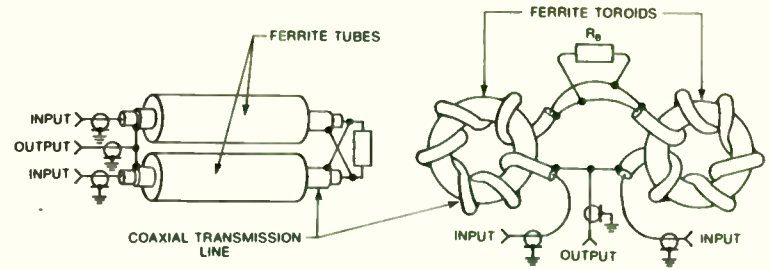


FIGURE 15 TYPE I IN-PHASE TWO PORT COMBINER



(A) PICTORIAL VIEW: TUBULAR & TOROIDAL CORES

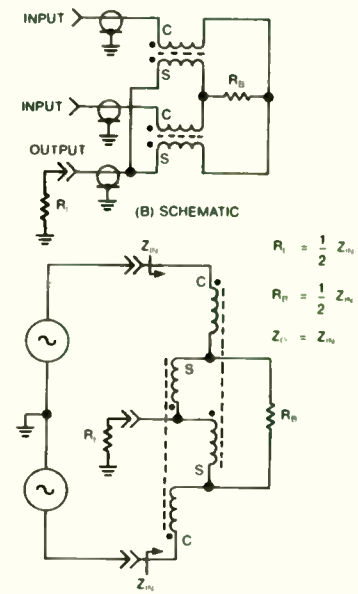


FIGURE 16 TYPE II IN-PHASE TWO-PART COMBINER

Compared to a hybrid device the monolythic system has higher reliability, since there are no bonds or solder joints to fail. The final result is not only more reliable than the labor intensive solution, it is physically smaller and lighter. Last but not least the monolythic solution is cheaper.

Three six stage log amplifiers were constructed and evaluated by the Royal Signals and Radar Establishment in England. The basics of the R.S.R.E. results are summarized in the following five figures.

Fig. 10 shows the detected video response of the strip as the input amplitude is varied from -80 dBM to +10 dBM. Response is shown for four different frequencies. Note that the response is log linear between -55 dBM and -5 dBM at frequencies from 60 to 600 MHz. The detected video level drops as the frequency increases, but the slope of the detected output remains relatively constant.

Fig. 11 is the error of the video response. Fig 10 shows small deviations from a perfect linear response. Fig 11 shows this deviation at two frequencies. Note that this is a very difficult measurement to make, requiring attenuators with an absolute accuracy of .25 dB across a range of 80 dB. Hewlett Packard offers a laboratory service that is capable of providing special attenuators individually calibrated to these tolerances. the calibration is valid only at one frequency, so each frequency measured requires a set of super precision attenuators. The video output thus obtained indicates accuracy of .5 dB max error between -55 dBM and -5 dBM at both frequencies tested.

Fig. 12 graphs the output amplitude of the IF port with varying input levels at three frequencies in the range. One of the virtues of the SL2521 is its ability to provide both accurate video output and a quality limited IF respose. The IF output gives solid limiting from -45 dBM to +5 dBM. Both the limiting level and the limiting knee are essentially constant with changes in frequency.

Fig. 13 illustrates the change in phase with change in input amplitude of one of the strips. One of the most unique properties of the SL2521 is that it gives both a log linear video output and a phase linear IF output. At 70 and 450 MHz the phase delay through the six stage strip changes less than 2 degrees across the full dynamic range. The worst case frequency gives a maximum change of 8 degrees across the amplitude range.

Fig. 14 gives the differential phase tracking error between amplifiers across 70 dB of dynamic range. For many uses the absolute amount of the phase shift through the amplifier and the variation of the phase shift with input amplitude are not important. What is important is that the

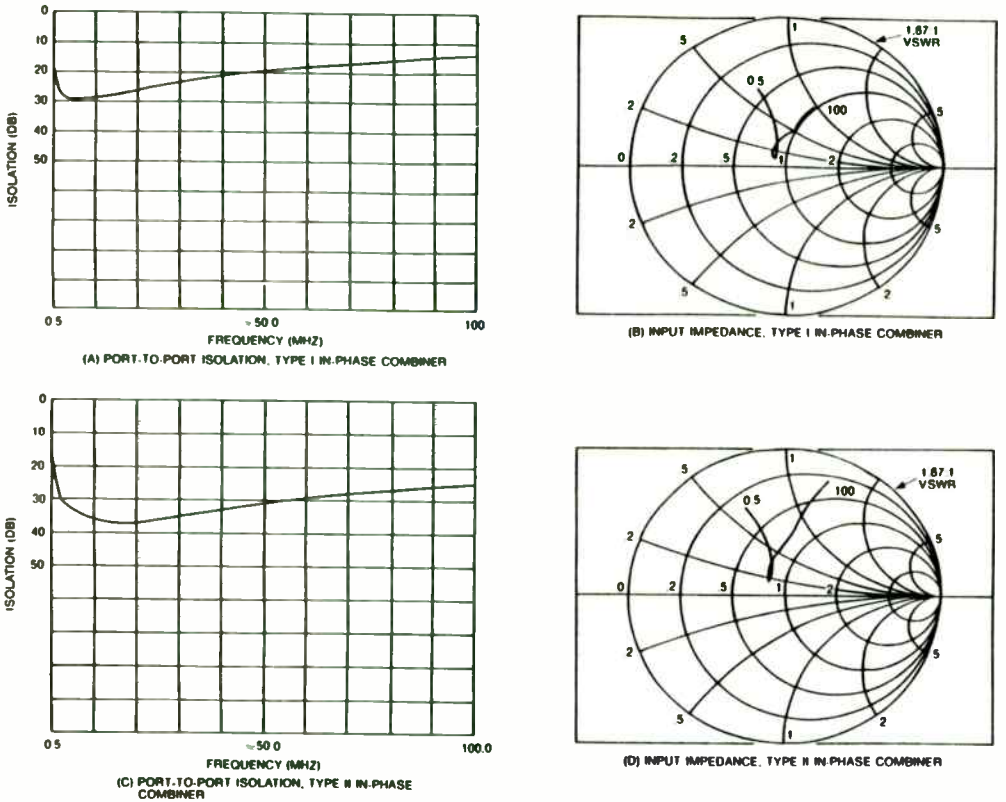


FIGURE 17 COMPARISON OF TYPE I AND TYPE II IN-PHASE COMBINERS

The combiner output load impedance is usually transformed to another desired value such as 50 or 75 ohms. This is readily accomplished by one of the wideband transformers described earlier. Usually the output impedance transformer is physically integrated into the combiner assembly. The interconnection between combiner and transformer can be made using micro-strip line techniques if it is not a standard coax impedance.

Theoretically any number of inputs may be combined with an in-phase combiner, but a practical limit is reached when the output impedance becomes too low to allow efficient wideband transformation back to the desired load impedance. An example of a type-II four port in-phase combiner is given in figure 18.

Four-port combiners may also be implemented by cascading two port combiners. This technique is illustrated in figure 19 for both types of two port combiners.

In-phase combiners all use a floating bridging resistor. This may be difficult to implement, especially in combiners handling high power. A wideband balun transformer allows using a single-ended or unbalanced load. The balun could also transform the balanced impedance to 50 or 75 ohms. Standard coaxial dummy loads, connected to the combiner with coax cable, may then be used as bridging resistors.

difference between two channnels remain constant. Phased array radars are an example of such a system.The differential phase change across the available dynamic range is less than 1 degree at 60 and 120 MHz and less than 2.5 degrees at 450 MHz for the six stage SL2521 log strip..

Special thanks to Peter Chadwick and Doug Kleven for assistance in the preparation of this manuscript.

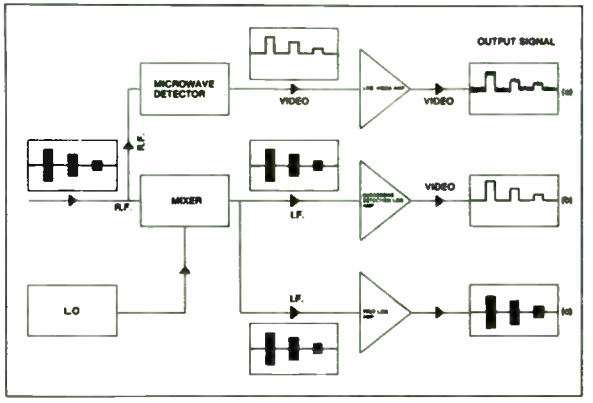


Fig. 1 Block diagram of broadband pulse amplification showing log video, successive detection, and true log techniques.

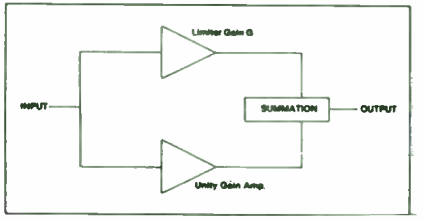


Fig. 2 True log amp block diagram showing limiter and unity gain amps in parallel

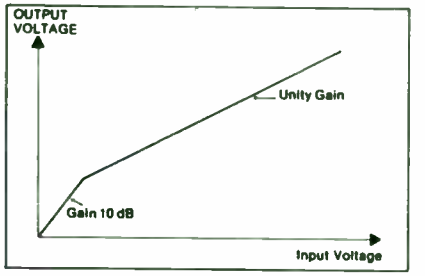


Fig. 3 Transfer function of true log stage showing dual gain characteristic

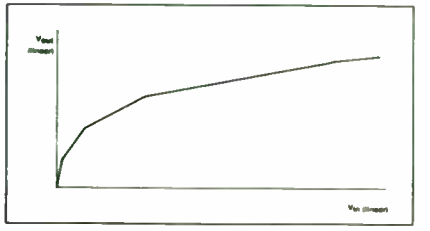


Fig. 4 Transfer function of six stage true log strip showing approximation of logarithmic response

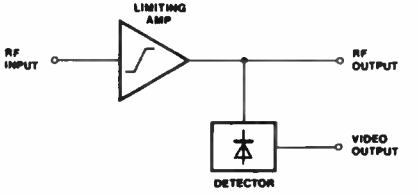


Fig. 5 Basic successive detection stage

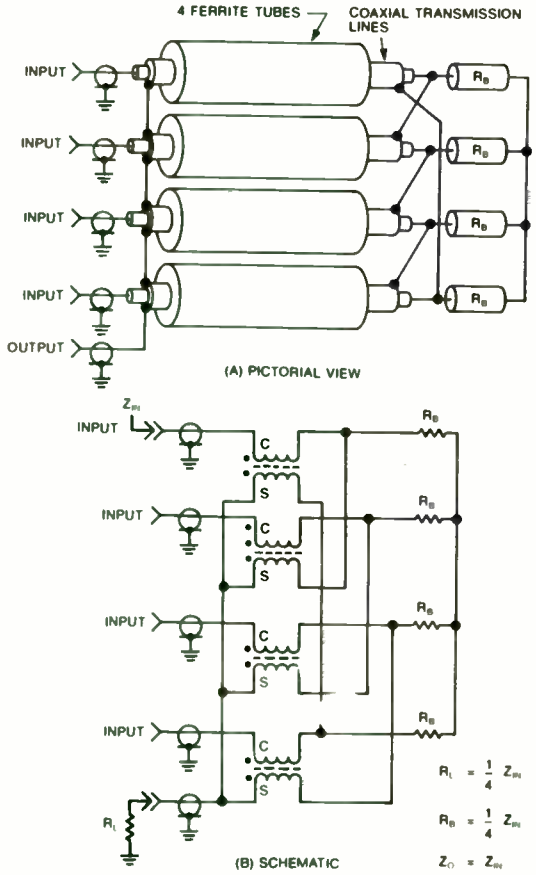


FIGURE 18 TYPE II FOUR PORT IN-PHASE COMBINER

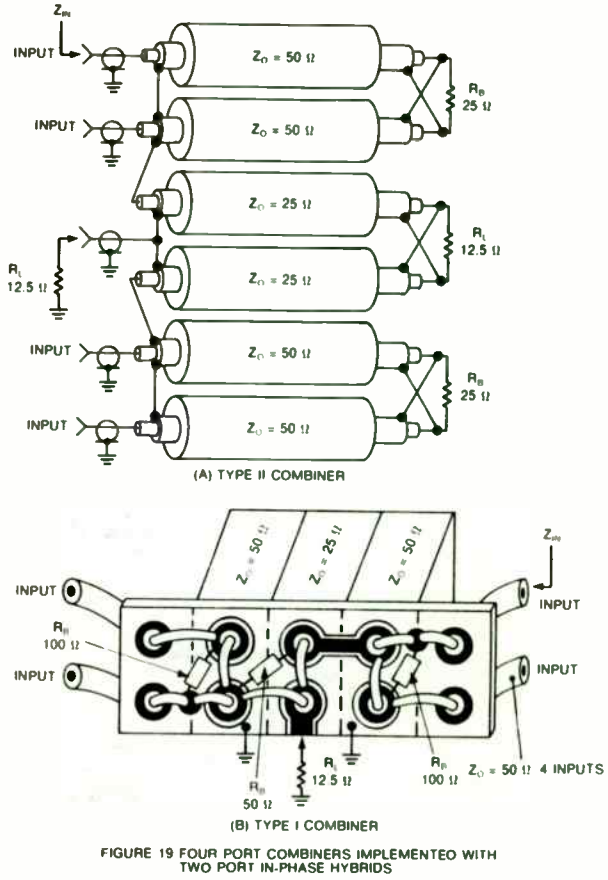


FIGURE 19 FOUR PORT COMBINERS IMPLEMENTED WITH TWO PORT IN-PHASE HYBRIDS

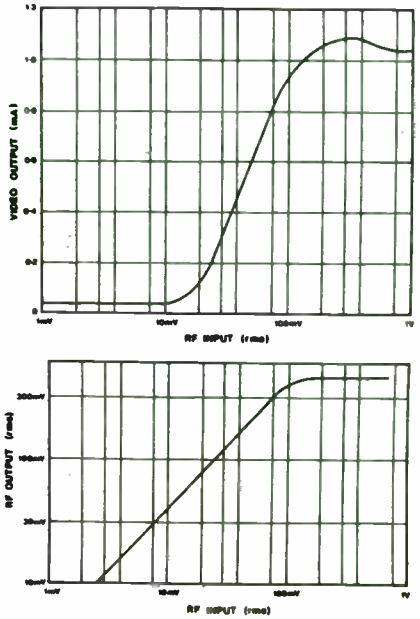


Fig. 6 Successive detection stage transfer function

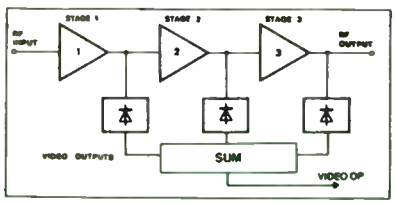


Fig. 7 Three stage log strip

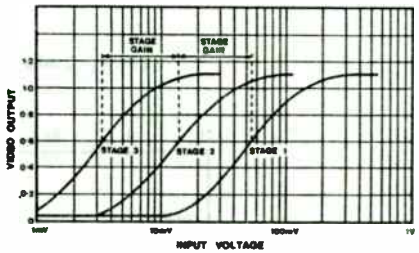


Fig. 8 Video outputs from three stage strip

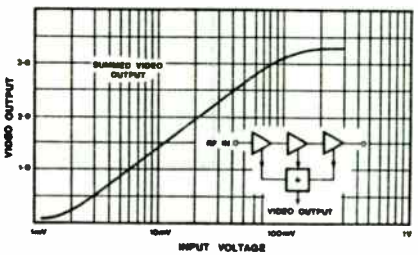


Fig. 9 Summed video output from three stage strip

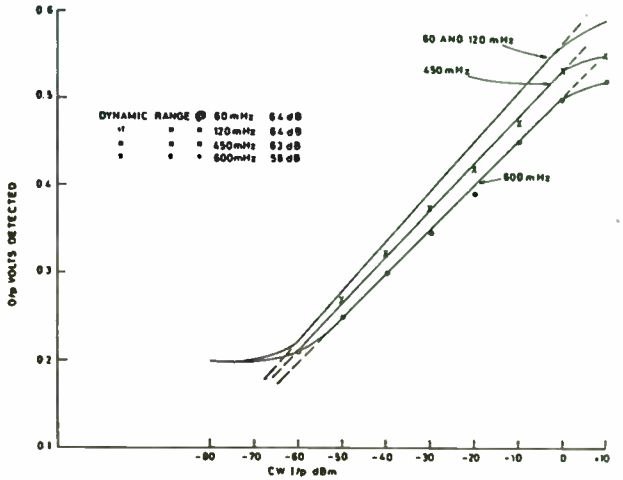


Fig. 10 Video output vs. IF input for six stage SL2521 strip

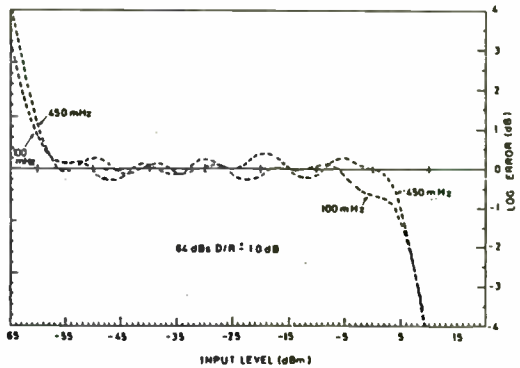
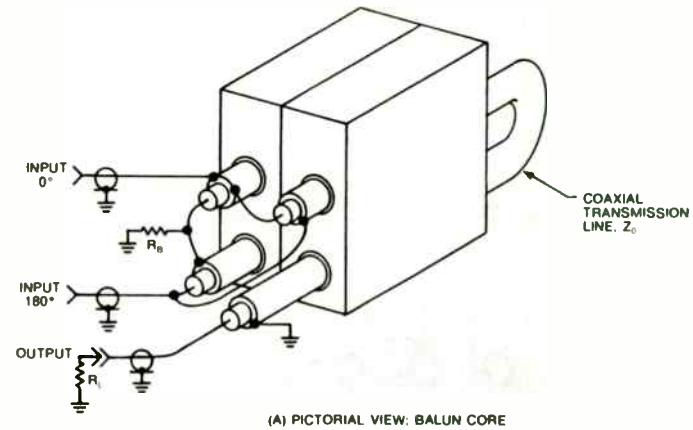


Fig. 11 Log error vs. input level

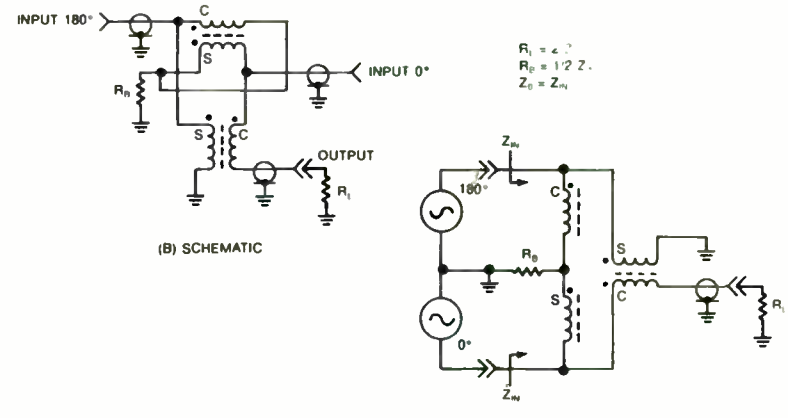
180-DEGREE HYBRIDS

If the roles of the bridging resistor and the load are interchanged, the result is a 180-degree hybrid combiner. The two input signals must be 180-degrees out of phase and of equal amplitude. The output is balanced to ground unless the usual balun is used. Examples of type-I and type-II 180-degree hybrid combiners with output baluns are shown in figures 20 and 21.

Many unique combiner designs are possible by using various combinations of basic combiner types and balun transformers. The combiner described in figures 22 (pictorial) and 23 (schematic) is an example of a four-port combiner using two each type-I in-phase combiners (cores A and F) and two each, parallel connected type-II 180-degree hybrid combiners (cores D and C) and a 4:1 balun transformer (cores B and E) to couple the combined output to a 50-ohm load. Connecting two 180-degree hybrids in parallel avoids using 25-ohm coax cable and provides the extra core material to handle the higher rf power.



(A) PICTORIAL VIEW: BALUN CORE



(B) SCHEMATIC

(C) EQUIVALENT CIRCUIT

FIGURE 20 TYPE I 180-DEGREE HYBRID COMBINER

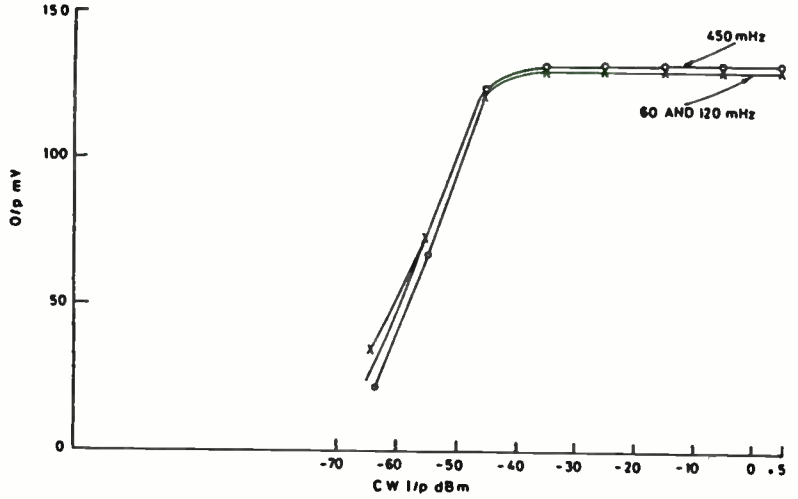


Fig. 12 IF limiting characteristic

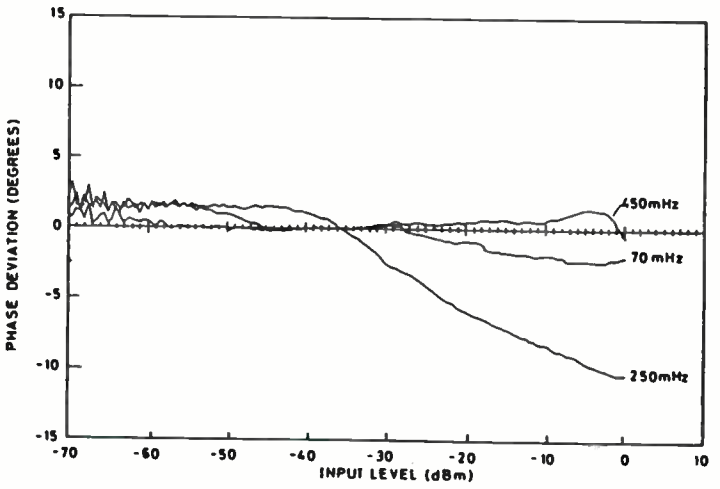


Fig. 13 Phase change vs. input level

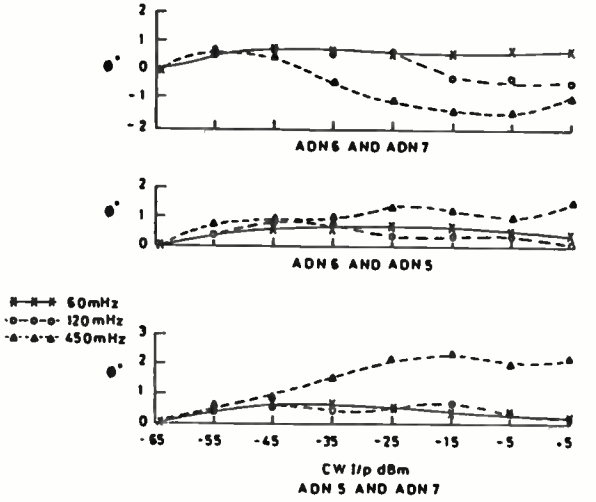
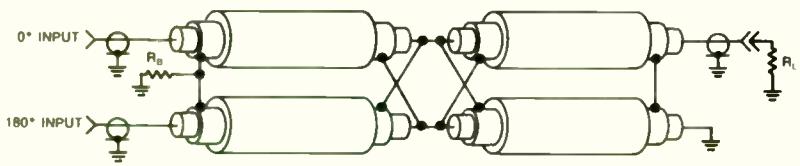
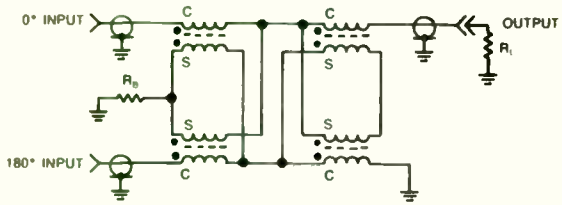


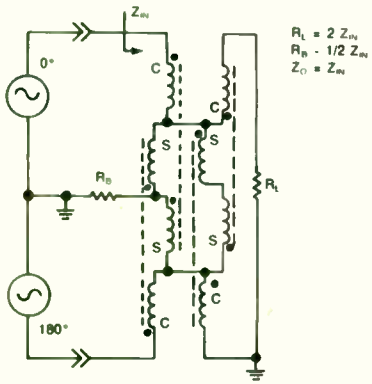
Fig. 14 Phase tracking of amplifier pairs with changing input level



(A) PICTORIAL VIEW, TUBULAR CORES



(B) SCHEMATIC



(C) EQUIVALENT CIRCUIT

FIGURE 21. TYPE II 180-DEGREE HYBRID COMBINER

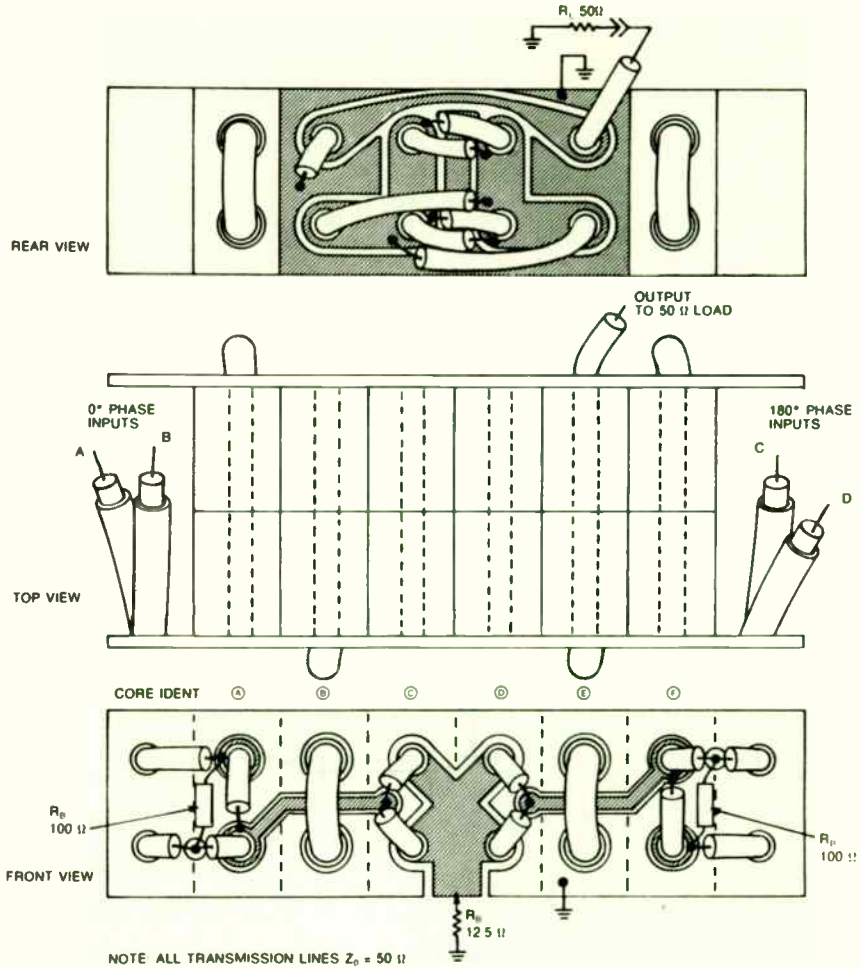


FIGURE 22. FOUR PORT, TWO STAGE COMBINER USING TYPE I AND II HYBRIDS, PICTORIAL

LINEAR FM MODULATOR

by
Jerry Isell
RF Design Engineer
Texas Instruments
P.O. Box 660246 M/S 8276
Dallas, TX 75266

ABSTRACT:

A system has been developed that will generate a linear FM modulated pulse signal. The system uses a 100 MHz clock and a 200 MHz CW input to generate a 20 ns pulse of 200 MHz energy. This pulse is used to excite a surface acoustic wave (SAW) expander. The resulting signal is a continuous linear sweep of frequencies of 75 MHz bandwidth, centered about 200 MHz. The duration of this sweep, or chirp, of frequencies is selected by using different SAW expanders. The chirp is then amplified and gated in time to sharpen the corners of the generated spectrum. The system has been designed, assembled, and successfully tested.

INTRODUCTION

Linear FM is a modulation scheme that is commonly used in radar systems.[1] This modulation consists of a sweep of frequencies, sometimes called a chirp, that occur within a given time period and with a specific repetition rate (Figure 1). This paper discusses a system that has been developed to generate this modulation.

THEORY

A Linear FM waveform may be generated by exciting a dispersive delay line with an impulse function. The dispersive delay line transfer function is flat in amplitude and has linear group delay within its bandwidth (Figure 2). The impulse response of the dispersive delay line is the inverse Fourier transform of its transfer function. This is a signal of time duration t with the instantaneous frequency varying linearly over the bandwidth of the delay line. This waveform is called the expanded pulse (Figure 1).[2]

This transformation may be visualized by thinking of the delay line as a frequency sensitive delay element that passes lower frequencies with the least amount of delay and higher frequencies with the greatest delay (Figure 3). If you simultaneously input all the frequencies within the delay line's bandwidth they come out in progression from low to high resulting in the expanded pulse.

In our case the dispersive delay line is implemented with a Surface Acoustic Wave (SAW) expander. Three different expanders are used to generate different expanded pulse widths. The

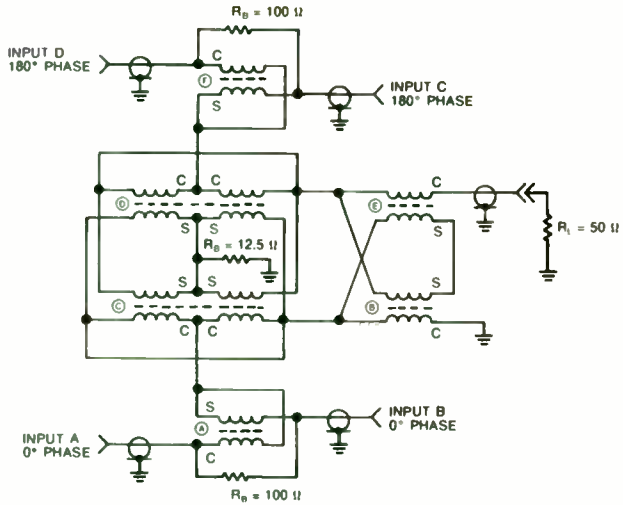


FIGURE 23 FOUR PORT, TWO STAGE COMBINER USING TYPE I & II HYBRIDS; SCHEMATIC

QUADRATURE HYBRIDS

The quadrature hybrid has two input ports, each of equal amplitude but one is 90-degrees out of phase relative to the other. Four-phase combining of four amplifier modules is feasible using two quadrature hybrids and a 180-degree combiner.

The quadrature hybrid is constructed by using "all-pass" networks and a wideband hybrid as shown in the block diagram of figure 24. Two all-pass networks are required; one for 0-degree (reference) phase shift and the other for 90-degree phase shift relative to the reference output. The absolute phase shift across an all-pass network changes with frequency, however, the two networks are designed to maintain a constant 90-degree phase difference between their outputs as the input frequency to both networks is varied.

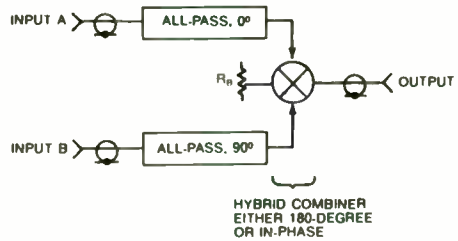


FIGURE 24 BLOCK DIAGRAM OF A QUADRATURE COMBINER

The all-pass networks may either be balanced or unbalanced circuits. Typical circuit topologies for both are shown in figure 25. Note that the mutual coupling in the unbalanced network must be negative and of a prescribed value.

expanders have a transfer function which exhibits linear group delay over a bandwidth of 75 MHz centered at 200 MHz.

To approximate the impulse function the SAW expanders are excited with a 10 ns pulse of 200 MHz. The spectrum of this pulse approximates an impulse function within the 75 MHz bandwidth (Figure 4).

In the SAW expanders the 10 ns input signal is spread over many microseconds resulting in a large loss in amplitude. The loss may be calculated by:

$$(1)\quad \text{Expansion Loss (db)} = 10 \log \frac{\text{Expanded pulse width}}{\text{input pulse width}}$$

This loss is in addition to the CW insertion loss of the device. The expansion and insertion losses for the three SAW expanders are summarized in Table 1.

SAW EXPANDER	INSERTION LOSS	EXPANSION LOSS	TOTAL LOSS
0.64 us	35 db	18.1 db	53.1 db
5.12 us	35 db	27.1 db	62.1 db
20.48 us	42 db	33.1 db	75.1 db

TABLE 1. SAW EXPANDER LOSSES

SYSTEM CONFIGURATION

The linear FM signal is generated by simultaneously inputing a spectrum of frequencies to a SAW expander. Three SAW expanders are used to generate expanded pulse widths of 0.64 us, 5.12 us, and 20.48 us. These pulses are then amplified and gated to eliminate any undesired signals outside the pulse. A CW mode is also available for test purposes.

The modulator consists of four sections; a digital control section, a Pre-SAW module, the SAW expanders, and the Post-SAW module. These sections are configured as shown in Figure 5.

The construction style for the RF sections is microstip PWBs on G10 material. The Pre and Post-SAW sections were mounted in separate aluminum housings to provide shielding and isolation for the circuitry. The digital control section is located on a card cage PWB as part of the parent system. The switches and SAW expanders are connectorized modules and are connected to the other sections with semi-rigid cable and SMA connectors.

DIGITAL CONTROL SECTION

In response to a modulator trigger signal the digital control section generates two signals; a 10 ns ECL pulse which is sent to the Pre-SAW module and a variable width TTL gate which is sent to the Post-SAW module. The width of the TTL gate signal is equal to the output pulse width of the selected SAW expander, within the resolution of its clock (400 ns).

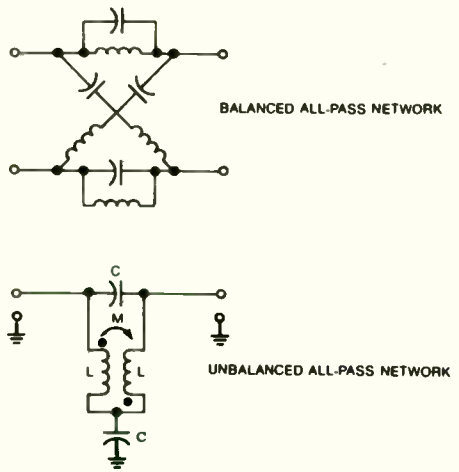


FIGURE 25 TYPICAL ALLPASS NETWORK TOPOLOGIES

Both circuits exhibit difficulties in practical implementation. The balanced lattice network may require long leadlengths and possibly a balun transformer for interface to an unbalanced hybrid. It requires more components than an equivalent unbalanced network and the component values must be closely matched to achieve low VSWR across the design bandwidth.

Implementation of an unbalanced all pass network allows shorter lead lengths and eliminates the balun transformer. It requires fewer components than an equivalent balanced all pass network. No closely matched component values are required, however, an exact amount of mutual coupling is required between two inductors.

The quadrature hybrid offers three advantages over the in-phase and 180-degree hybrids when used as an output combiner in solid state wideband power amplifiers. The third harmonic and certain other odd order harmonics cancel in the output port and add in the bridging resistor. The all pass phase shift networks and the basic combiner specifications must hold up to the frequency of the highest harmonic of concern to achieve this in practice. For example, the all-pass networks must provide the 90-degree phase difference up to at least 90 MHz in order to cancel the third harmonic of a 30 MHz fundamental signal in the hybrid's output.

RF power flowing into the output port of a quadrature hybrid will split, go through the all pass networks, partially reflect at the signal source impedance, go back through the all pass networks, and cancel in the output port and add across the bridging resistor. This is happens whether the power flowing into the output port is the result of a mismatched load or coupling from an adjacent transmitting antenna. The result is the combined power amplifier output behaves as though it has a matched source impedance. The situation of reverse power flow from adjacent transmitter coupling is especially important since the two signals cross modulate each other in the active devices. The

PRE-SAW MODULE

A schematic diagram of the Pre-SAW module is shown in Figure 6. The input signal for the expander is generated by gating a 200 MHz CW signal for 10 ns. This waveform is shown in Figure 4.

The 200 MHz CW input is amplified by A1 to +7 dbm at the input to the mixer, M1. A 10 ns ECL pulse is input from the digital control board to the mixer IF port through A2. The DC offset voltage on the IF port is trimmed by the 500 ohm pot; this increases the LO to RF isolation of the mixer to approximately 60 db at room temperature. The waveforms shown in Figures 4 are present at the RF port of M1. This signal is amplified to +20 dbm before it is output to the SAW expanders. A test input is provided which turns the mixer on at all times to allow a CW output. It is important that all amplifiers which process the pulsed signal be broadband so that a minimum of distortion is generated.

SAW EXPANDER ASSEMBLY

A schematic diagram of the SAW expander assembly is shown in Figure 7. S1 and S2 determine which of the three SAW expanders or a bypass path is selected. The attenuators on the expander outputs are used to adjust the signal level so that it is identical irregardless of which path is selected.

POST-SAW MODULE

A schematic diagram of the Post-SAW module is shown in Figure 8. The Post-SAW module consists of three amplification stages, a gated mixer and a limiter. The signal level at the input to this module is approximately -67 dbm, therefore a large amount of gain is needed to restore it to a useable level; this is accomplished with A1, A2 and A3. The mixer is gated on by a TTL signal coincident with the leading edge of the expanded pulse. This prevents the large gain in front of the mixer from producing unnecessary noise when the pulse is not present; it also sharpens the edges of the expanded pulse. As in the Pre-SAW module DC bias is provided for the mixer to improve its isolation. The gated expanded pulse at the mixer output is limited by about 6 db in L1. This removes any amplitude ripple in the expanded pulse. The output level is 0 dbm.

SUMMARY AND SUGGESTIONS FOR FURTHER WORK

This system has been prototyped and thoroughly tested. All of the design goals were met. The modulator is presently integrated into a prototype radar system.

There are three areas which I feel could be changed to improve the performance.

intermodulation products caused would be radiated along with the desired signal. The quadrature hybrid will cancel some of these "backdoor" IMD products in it's output port by terminating the energy in the bridging resistor.

Two wideband linear power amplifiers, combined with a quadrature hybrid, will exhibit nearly constant gain under varying load impedances (varying VSWR). The ratio of input power into the quadrature hybrid splitter to the forward power out of the quadrature hybrid combiner will be nearly constant in contrast to the same situation using in-phase or 180-degree hybrids.

Techniques for wideband RF power transformers, combiners, and splitters have been presented with emphasis on topology. Various types of transformers and combiners were examined and classified. Examples of each were presented in pictorial form, schematic, and equivalent circuit in an effort to bridge the gap from theory to working hardware. A rich variety of combinations of the basic transformers and combiners are possible though not covered here. It is hoped that a more complete understanding of the basic types presented here will enable the reader to produce more sophisticated designs.

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1. To achieve the maximum signal to noise level at the modulator output it is necessary to drive the SAW expanders with as large a signal as possible. This creates a requirement for a high power switch at the expander inputs. This part can be costly and hard to obtain. A low power switch may be used by assigning a separate power amp to each expander and switching the low power input to the amp as shown in Figure 9.

2. The signal to noise level is degraded on the .64 us and 5.12 us expanders by the attenuators on their outputs. The attenuators are used to provide equal levels at the Post-SAW input. This equalization may also be accomplished by amplifying the output of the 20.48 us and 5.12 us expanders to the level of the .64 us expander before the switch. This is shown in Figure 10.

3. The expanded pulse is gated by a signal that is generated from a 400ns clock. For the .64 us (640ns) expanded pulse this results in a rather coarse gate. Originally a fourth expander with a longer pulse width was used in the system. This required the 400 ns clock to generate a gate signal long enough for it. With the present three expanders a higher frequency clock could be used to generate a gate of finer resolution. This will eliminate some ootential signal processing problems elsewhere in the radar.

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18. Waight, M., "Report on Quadrature Hybrid Investigation - Aug.1985", Unpublished.

Figure I. Linear FM Pulse Modulation

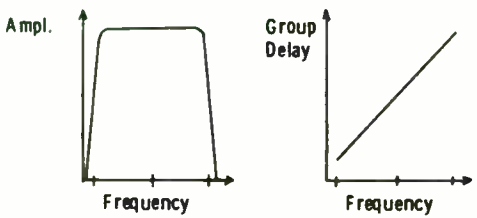

Figure 2. Transfer Function of Dispersive Delay Line

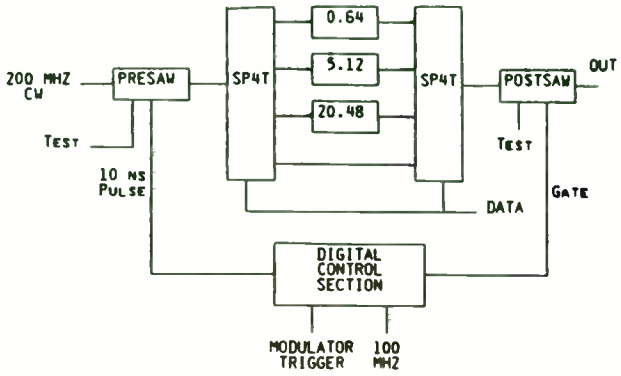

FIGURE 5. SYSTEM CONFIGURATION

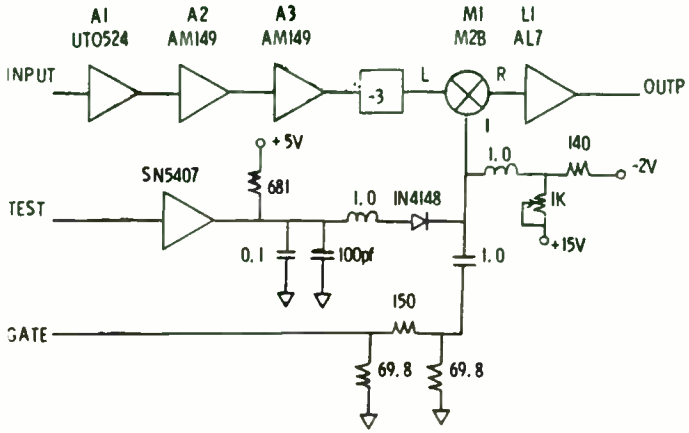

FIGURE 8. Post SAW Module

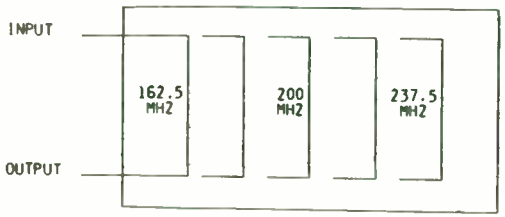

FIGURE 3. DISPERSIVE DELAY LINE

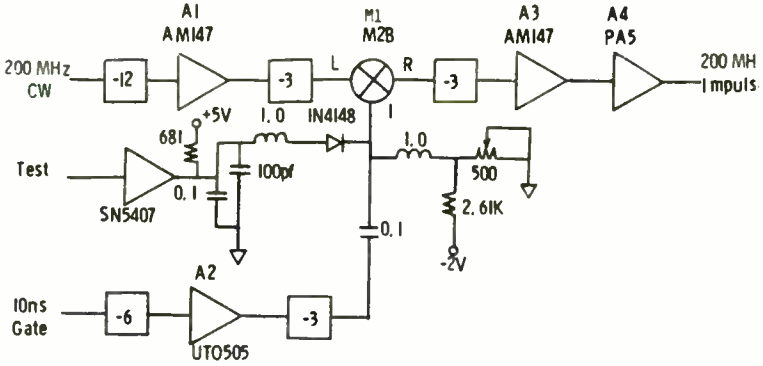

Figure 6. PreSAW Module

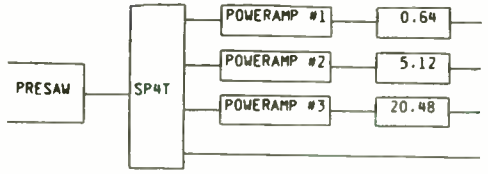

FIGURE 9. LOW POWER SWITCH MODIFICATION

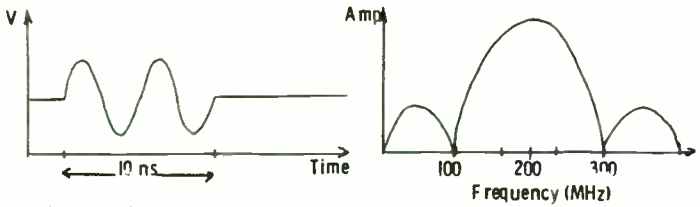

Figure 4. 200 MHz Impulse

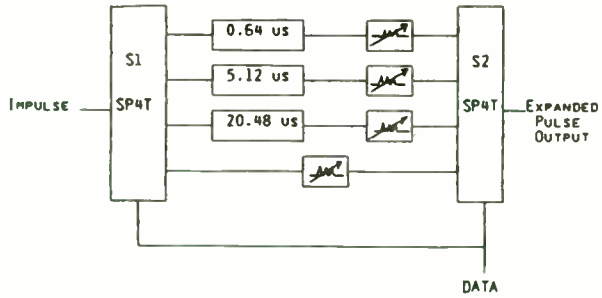

FIGURE 7. SAW EXPANDER ASSEMBLY

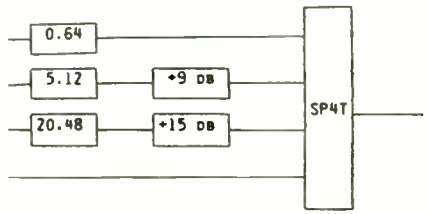

FIGURE 10. SWITCHED OUTPUT AMPS MODIFICATION

HIGH POWER UHF PULSED PUSH-PULL AMPLIFIER DESIGN

Prepared by:

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Applications Engineer

October 1985

RF Push Pull amplifiers can be somewhat of a mystery to those engineers who've never designed one. This application note attempts to unlock some of that mystery by simplifying those nebulous areas that make a push pull amplifier different than a single ended or parallel amplifier. The name push pull in itself implies a different mode of operation than two transistors operating in parallel.

In a standard Class C amplifier, one half of the input sine wave (positive or negative) turns the amplifier on while the other half maintains a reverse bias. If a periodic sine wave symmetrical about a horizontal axis with positive and negative half cycles were being delivered to two Class C common emitter transistors in parallel, the positive half cycle would turn on both of the transistors while the negative half cycle would keep them reverse biased. In push pull operation, the sine wave is shifted 180 degrees for one of the two parallel transistors. The result is such that the positive half cycle is no longer delivered to each transistor simultaneously but instead separately so that when one transistor is on the other is off. This mode of operation has a lot of nice advantages not the least of which are thermal since two transistors in close proximity are not dissipating power at the same moment in time.

Figure 1 shows the current flow through a one to one transformer being delivered to two resistive loads where $Rs = R_1 + R_2$ and $R_1 = R_2$.

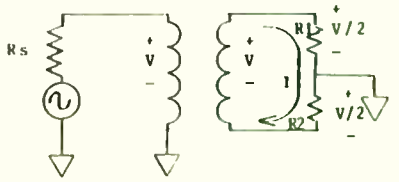

FIGURE 1

EW APPLICATIONS OF HIGH RESOLUTION COMPRESSIVE RECEIVERS

BY

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ABSTRACT

With the crowding of the electromagnetic spectrum and the evolution of spread spectrum and other complex signatures, the ELINT/ESM demands of the 1990's will pose new challenges to EW receiver manufacturers. Resolution down to the hundreds of Hertz and real-time processing will be essential.

This paper will make the system designer aware of a few of these analog technologies for signal processing in radar systems. When low cost, low complexity, and flexibility are key considerations in configuring a system, analog technology should be the system designer's first choice to meet these requirements.

INTRODUCTION: THE EW SCENARIO

Analog compressive (microscan) receivers can be used to provide fast, real-time spectrum analysis of the IF operating band. The range of their performance is characterized in Figure 1. The microscan receiver can provide quick processing times, wide bandwidths or very good resolution depending on the environment and users' needs. Applications can vary from electronic intelligence gathering, radar warning receivers, anti-radiation seekers to moving target indicators (MTI).

The compressive receivers' function is to perform threat analysis on a complex signal environment. This environment is crowded with different modulating techniques, magnitudes of signals and frequencies. The compressive receiver can be configured to gather and translate an unknown, crowded frequency/time spectra, perform a true instantaneous Fourier transform and output valuable information which can be used for threat accuracy measurements.

Threat accuracy can be defined as the probability of intercept (POI) ratio, processing and scan time and system resolution. Each one of these topics will be discussed within the body of the paper.

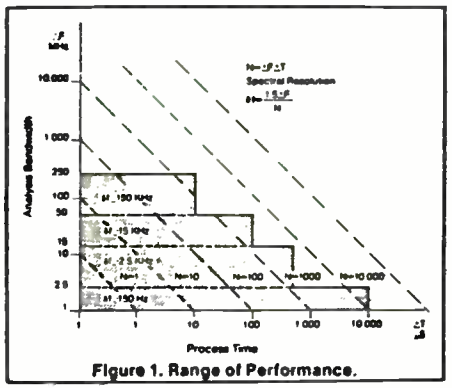

Figure 1. Range of Performance.

Since the primary voltage equals the secondary voltage and primary current equals secondary current, then the voltage drop across the two loads is equal assuming equal resistances. It's easy to see that during the positive half cycle current flows in a clockwise direction and R_1 has a positive voltage drop across it with respect to ground while R_2 has negative drop with respect to ground. If R_1 and R_2 were emitter base junctions, R_1 would be on and R_2 would be off during the positive half cycle. The negative half cycle is just the reverse.

Many times a one to one balun made out of a single piece of fifty ohm coax is used to generate push pull action in an RF amplifier. Figure 2 shows a typical arrangement. The electrical configuration is different than the one to one transformer in Figure 1, but the basic operation is the same.

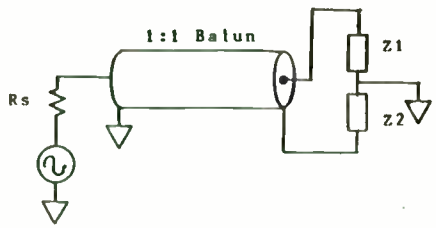

FIGURE 2

The center conductor acts as the primary and the outside shield acts as the secondary. The transformer coupling action between the primary and the secondary is identical to a one to one transformer in that there is an induced EMF in the secondary. The only difference between the coaxial transformer and a conventional transformer is the way the interwinding capacitance is laid out. In conventional transformers, the interwinding capacitance is an unwanted capacitance that limits high frequency performance because it resonates with the leakage inductance to produce a loss peak [1]. In transmission line transformers, the interwinding capacitance is arranged such that it is part of the characteristic impedance of the line. Therefore, if the transmission line transformer is terminated in its Z_0, there will be no resonances that will limit its upper frequency response. This means that the coaxial balun is a transmission line as well as a transformer.

Because the electrical configuration of the coaxial balun is identical to that of a twisted pair, the theoretical explanation of the balun will be carried out using the twisted pair. Figure 3A shows a conventional twisted pair. In order to maintain good transformer action, the primary and secondary must be tightly coupled. This results in interwinding capacitance which can be tolerated because it contributes to the Z_0 of the line. The inductance per unit length, along with the distributed interwinding capacitance, assigns some Z_0 to the transformer. The Z_0 simply becomes part of the matching circuit while the transformer allows for push pull action. If it were possible to achieve good coupling without interwinding capacitance, than push pull action could be achieved without the transmission line. Said another way, it is only necessary to have transformer action for the push pull effect, it is not necessary to have a transmission line.

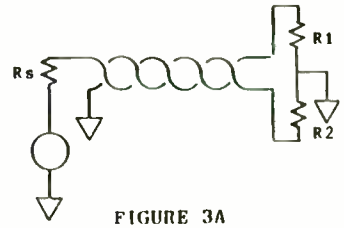

FIGURE 3A

Figure 3B shows the twisted pair in a simpler form so that it can be analyzed. During the positive half cycle, a current I_1 flows into the load R_1 causing an increasing magnetic field ϕ_1 in the direction shown by the right hand rule. The direction of the induced current in the secondary can be found by Lenz's Law: "If the external flux increases, the magnetic field of the induced current will be in the opposite direction" [2]. Therefore, ϕ_2 is responsible for the induced current I_2. The secondary is now a source with its own current and voltage. The voltage of this source is in such a direction as to maintain the direction of current I_2. [3] It's

THEORY OF THE COMPRESSIVE RECEIVER

A compressive receiver can be configured in two basic forms which are illustrated in Figure 2. Each one has its own applications when used within the EW environment.

The C-M-C compressive receiver, Figure 2B, has its own applications within the EW environment, but due to its poorer dynamic range and increased cost over the M-C-M system, it will only be briefly mentioned.

The C-M-C configuration suffers from poorer dynamic range due to its signal-to-noise ratio. Typically the dispersive devices' insertion loss is -30dB to -40dB. Any incoming RF signal must be recovered before convolution occurs, and then be recovered again at the output of the second dispersive device. With the M-C-M configuration this recovery of signal-to-noise is minimized.

In the M-C-M configuration, Figure 2A, the incoming RF signal has only to be recovered after going through one dispersive device and not two. The sweeping local oscillator (SLO) has negligible effect on the incoming signal due to its noise level. The noise level of the SLO is strictly limited to the thermal noise of itself.

The M-C-M compressive receiver will be discussed in depth and specifically mention the multiply long-convolve short M-C-M transform method. Either M-C-M or C-M-C configuration can guarantee 100% probability of intercept when a tandem system is implemented.

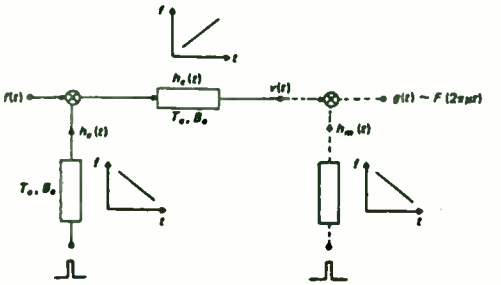

FIGURE 2A: Multiply-Convolve-Multiply Fourier Transform System

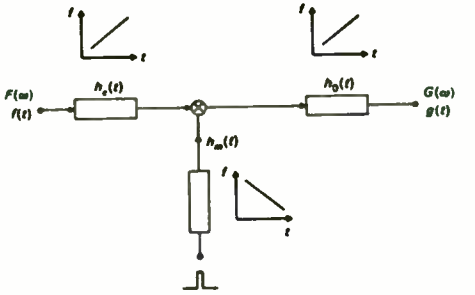

FIGURE 2B: Convolve-Multiply-Convolve Fourier Transform System

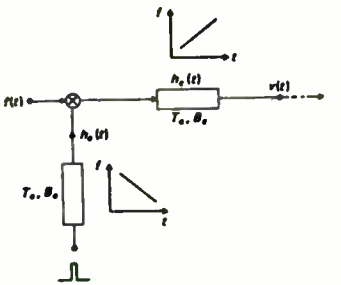

FIGURE 2C: Multiply-Convolve Fourier Transform System

important to mention here that the currents I_1 and I_2 are considered odd modes of currents which are the dominant modes in this type of transformer [4]. Even modes of current are not shown here but would be in the same direction instead of the opposite direction. Even modes of current are caused by flux linkages between the primary and secondary instead of linkages around each.

Summing up the voltages around the loop (Figure 3C) it's easy to see that the transformer primary voltage cancels the transformer secondary voltage so that the source voltage (Vs) is impressed across two equal loads just as originally shown in Figure 1. Since the current through the two loads is the same and the voltage across each is half the source voltage, the impedance of each is one half the source impedance. If a 50 ohm twisted pair (or coaxial line) is used, then each side of the balanced end is 25 ohm's to ground.

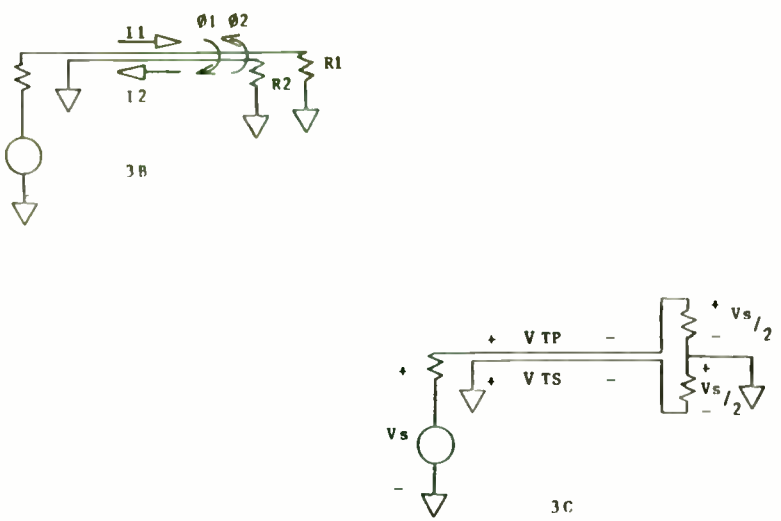

FIGURE 3B, C

DESIGN #1

A one to one coaxial balun will now be used in a push pull design. Inspection of Figure 2 shows that the length of the balun determines how much inductance to ground Z_2 will see. The impedance to ground of the outside shield of a coaxial cable is termed the rejection mode impedance. This is basically the X_L of this shield. If the balun is sufficiently long, this rejection mode impedance will not affect the match at Z_2 significantly. As a rule of thumb, the balun should be made long enough so that the rejection mode impedance is five times that of the Z_0 of the line [5]. If size constraints restrict the balun's length, an alternate solution would be to use the rejection mode impedance as a shunt L to ground at Z_2. This would then require an equivalent inductance to ground at Z_1 to insure that each side of the balun have the same complex impedance. The first design to be demonstrated will use this approach.

The SD1565 was selected for this narrowband 425 MHZ push pull 500 Watt application due to its excellent thermal characteristics under long pulse conditions. This transistor operates at 40 Volts and is capable of 500 Watts at 250 microseconds, ten percent duty cycle, Class C operation.

The input and output impedances from the data sheet are 1.75 + J2.75Ω and 1.8 + J.5Ω respectively. Referring to Drawing #1, which is normalized to 25Ω , the effect of shunt L can be seen. For convenience, the impedance and admittance coordinates have been reproduced on the left side of the chart. The inductive reactance of the outside shield of two inch semi-rigid coax was measured to be +J34.15Ω . Normalized to 25Ω this gives 34 15/25 = 1.366. Starting at the center of the chart at A (25Ω) and moving along the constant resistance circle to B gives a shunt inductive reactance value of 1.36 read at C. A series capacitance of value .48 read at D transforms the impedance to .65 at E. The unnormalized impedance at E is then (.65) 25 Ω = 16.25 Ω and the capacitance value at D is $C = 1/2 * F X_C$ where $C = 1/(2)\ (3.14)\ (425 \times 10^6)\ (.48)\ (25) = 31.2$ PF. This shunt L, series C high pass configuration will be the same for the input and output of the circuit (see Drawing #4) so that the rest of this example will be matched from the impedance of the device out to

If only one system is to be used and a maximum FOI is required, the M-C-M multiply short microscan receiver should be implemented. This configuration is designed with a shorter dead time interval to provide maximum coverage of the analysis bandwidth. This system has an added advantage in that amplitude and phase information is preserved for possible down line signal processing if the user requires. Spectral phase can be preserved allowing inverse transforming back to the original input domain. If spectral phase data is not required by the user, in threat analysis, the user could simply eliminate the final multiply stage which is used to preserve phase data, Figure 2C. Derivation of the above systems' mentioned generated waveforms can be reviewed in Morgan, Surface-Wave Devices for Signal Processing, pp 271-275 [1].

A point that should be mentioned is that the M-C-M multiply long system's Fourier output spectra does not exactly correspond to the input spectra. This is due to an effect known as a "Sliding Fourier Effect" [2] transform.

OPERATION OF THE COMPRESSIVE RECEIVER

Let us assume the scenario in which Figure 3, a functional block diagram of a compressive receiver, detects a variety of threat spectra which must be quickly detected, analyzed, discriminated and acted upon. This threat spectra could be transmitted from a hostile frequency jammer, hopper or ECM communications. These intercepted signals are mixed with the known generated chirp or the sweeping local oscillator.

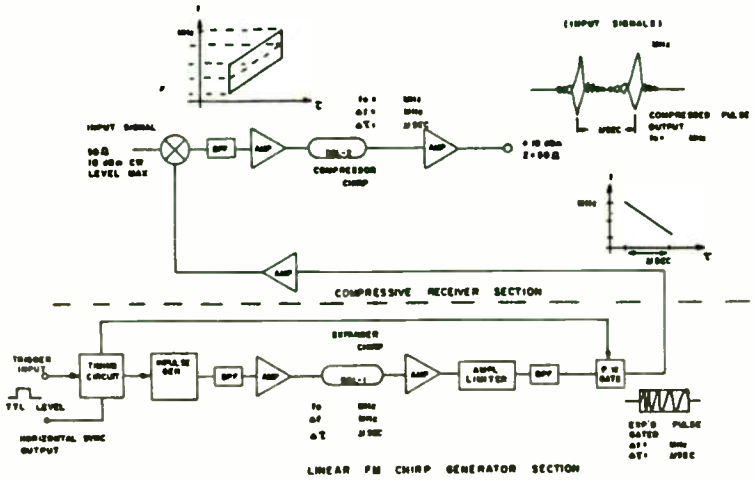

FIGURE 3: Compressive IF Receiver
Functional Block Diagram

This signal is amplified and fed into the compressor of the microscan receiver. The compressor is designed with the required bandwidth, dispersion and opposite sign slope of the SLO and can be weighted. Convolution occurs, and the output is the magnitude of the Fourier transform of the complex input spectra.

The weighting can be a separate "Black Box" within the receiver if the user prefers. Typically a Hamming or Taylor weighting function is used. Weighting is performed within the receiver to reduce time sidelobes at the output. This gives the system the capability to resolve similar frequencies with substantially different power levels and modulating techniques. Weighting of the output pulse does incur some system resolution loss, but the device bandwidth can be increased to compensate for this. A coherent or non-coherent system can be designed if the user requires.

16.25 Ω on input and output.

The output matching is configured using Drawing #2 and starts at 16.25 Ω at A (.65 normalized) and works back towards the generator (the transistor's output impedance). The movement from A to B represents a shunt capacitive reactance of (1.25) 25 Ω = 31.25 Ω at C. This reactance can be realized in a shunt configuration to ground or can be referenced to the opposite side of the balun. Since one side of the balun is always 180 degrees out of phase with respect to the other, the voltage across the balun is always twice the voltage to ground. Therefore, the same transformation can be realized by doubling the capacitive reactance to ground and referencing it to the opposite side of the balun. Instead of 31.25 Ω to ground then this becomes 62.5 Ω across the line. The value of capacitance across the line is given by:

$$(1)\ C = 1/(2 \pi F X_C)\ (2)$$

where X_C is the unnormalized value.
Therefore $C = 1/(2)\ (3.14)\ (425 \times 10^6)\ (31.25)\ (2) = 5.9$ PF

Since the chart is normalized to 25 Ω all transmission line matching sections will be 25 Ω lines for simplicity. The first transmission line matching section transforms from B to E by rotating around the center of the chart along a constant VSWR circle from B toward the generator to the real axis. The length of line is determined by extending a straight line from the chart center through B. The value at D is then .054 wavelengths. One wavelength in free space equals

$$(2)\ \lambda_o = 11808/F\ (MHZ)$$

This becomes 11808/425 = 27.78 inches. The relative velocity of propogation for the substrate is .4729. The guided wavelength in the material is then

$$(3)\ \lambda_o \cdot V_p = \lambda g$$

which gives λ_g = (.4729) 27.78 = 13.137 inches. The length of transmission line in inches is

$$(4)\ \lambda_g \cdot (\text{fractional wavelength}) = \text{physical length (inches)}$$

which gives 13.137 (.054) = .709 inches.

Another shunt capacitance moves from E to F which gives a reactance at G of (.5) 25 Ω = 12.5 Ω and a capacitance value from equation (1) of 15 pf. Another transmission line of length .037 read at H transforms from F to I. This length in inches is computed from (4) which makes it .486 inches. The last shunt capacitance moves from I to J and is computed from (1) to be 48 PF. The final transmission line is a movement from J to N and its length is computed from L minus M or .018 - .0035 = .0145. Then from (4) its length is .190 inches. Point N is the conjugate of the output impedance of the generator. Since the scheme here has been to match from the load towards the generator then it is necessary to match to the generators conjugate and not the output impedance of the generator itself. Point N is read as .072 - J.020, unnormalized is then 1.8 - J.5 Ω which is the conjugate of the output impedance of the transistor at 425 MHZ.

The input network will be configured on Drawing #3. The input impedance of the device is given to be 1.75 + J2.75 Ω and this is normalized at point A. Since this is the load the network configuration will still work towards the generator which is the 25 Ω point at the center of the chart. The first shunt capacitance immediately at the device leads is a movement from A to B and is read at C to be 50 PF from (1). A transmission line matching section from B to D is read at E to be .0535 which is .702 inches (4). The final shunt capacitance from D to F is read at G to be 13.5 PF (1). F is now matched to the center of the chart (25 Ω) by the configuration of Drawing #1.

The completed circuit is shown in Drawing #4. Evaluation of this design showed very good performance at the 500 Watt level; however, a problem of instability was observed during drive up. To explain further, as the input power was varied, it was observed that the part would oscillate but once full power was applied complete stability was achieved. This is attributable to the fact that the part has higher gain at less than full power. Since the device is a common base configuration, at some frequency it has a negative resistance input component. This negative resistance component coupled with the

BUILDING BLOCKS OF THE COMPRESSIVE RECEIVER

Analog pulse compression can be accomplished using specific technologies of Surface Acoustic Wave (SAW) Reflective Array Compressors (RAC) or Impedance Control Devices (IMCON). Each device has its advantages and applications within the receiver.

IMCON TECHNOLOGY

The IMCON, which was developed at Andersen Laboratories, Inc., in 1968, is used as a key signal processing component for commercial, military and aerospace system applications.

The IMCON is based on the concepts of a single grating dispersive device which makes use of Perini's[3] observations that impedance mismatches which occur at joints in waveguides can produce reflections. By controlling the location of these impedance mismatches or surface discontinuities, a grating device could be generated where reflections could be advantageously used.

As illustrated in Figure 4, the IMCON is configured using a rectangular thin steel strip as the media for wave propagation. At one end of this steel strip two piezoelectric horizontal shear mode transducers are edge bonded to the steel. These piezoelectric transducers are cut and lapped along the proper axis to allow for highest coupling of electric energy. The function of the piezoelectric transducers is to convert an electric signal to an acoustic signal and then to retransfer this acoustic energy back to electric energy at the output of the device. A herringbone-like pattern or grating is designed and photolithographically etched on to the steel at a 45 degree angle to the acoustic path from the transducers. The grating pattern is designed so that the acoustic energy at various frequencies reflects at differing distances from the transducers, giving a precisely controlled time delay as a function of frequency to the output.

An acoustic damping material is applied to the edges and one end of the steel strip. This acoustic damping material helps to eliminate any type of time spurious signals which may degrade the performance of the device.

A key advantage of the IMCON over other technologies is the availability to routinely amplitude correct and phase correct for any type of ambiguities which may occur due to manufacturing imperfections.

Depending on a customer's requirements, amplitude and phase errors can be controlled to a tolerance typical of $\pm$0.2dB of amplitude error, and $\pm$ 1^{o} of phase error. Sidelobe structure in the area of -40dB is the norm for IMCON performance and -50dB sidelobes have been demonstrated. Dispersions from 8 μsec to 5.5 μsec can be implemented on one steel strip, and if required the IMCONs can be cascaded together to achieve 10,000 μsec of dispersion in one package.

The IMCON is a linear device whose delay vs. frequency characteristic curve can be defined by Figure 5. The phase response of the IMCON is defined as a quadratic response. It is considered a reciprocal device in that once it is tuned either transducer can be configured as either input or output.

IMCONs can be designed, according to the users needs, as either up-chirp (positive slope devices) or down-chirp (negative slope devices). An up-chirp

fact that the high pass (section from Drawing #1) has a series resonance which will reflect a zero impedance, at some frequency, to the device at the input and output sets the stage for potential instability. The solution for this is to get away from the series resonance by using a low pass configuration.

DESIGN #2

If a one to one balun is made long enough so that the rejection mode impedance does not contribute to the match, it can be characterized quite easily for the intended frequency of use. By connecting the balun as shown in Figure 2 and using good high frequency 25 Ω chip resistors for Z_1 and Z_2, the balun will show a low VSWR (50 Ω unbalanced impedance) for all frequencies where the unbalanced to balance transformation is occurring. At very low frequencies its input will simply be 25 Ω and at high frequencies it will be limited only by leakages [6]. No compensation for the rejection mode impedance is necessary if the balun is long enough. Drawing #7 shows a 5 inch balun suitable for UHF.

With the rejection mode impedance out of the way, the design will be fabricated between the device and 25 Ω . This second design will be broader bandwidth, from 400 to 450 MHZ which will require low Q matching. The Q is calculated from the following:

$$(5)\quad \frac{\sqrt{F1 \cdot F2}}{F2 - F1} = Q$$

For this example $Q = \frac{\sqrt{400 \cdot 450}}{450 - 400} = \frac{424.3}{50} = 8.5$

This is a 3 db Q which means that the half power points will be at the band edges. A more desirable situation would be to have 90% of max power at the band edges which would correspond to a .5 db Q. The conversion factor from a 3 db Q to a .5 db Q is .34 [7]. Therefore, 8.5 (.34) = 2.83. To be conservative, a Q of 2 will be used. A constant Q circle of 2, where Q = X/R, is plotted on Drawing #5.

Without the aid of an optimization program, the approach will be to select the transistors impedance at some frequency to design around. The center frequency is approximately 425 MHZ; however, all transistors exhibit some roll off with frequency so that an impedance point above center frequency will be used. A convenient point will be 435 MHZ. At 435 MHZ the transistors output impedance is 1.8 + J 2 Ω Drawing #5 is normalized to 25 Ω , point A. The first shunt capacitance from A to B is read at C to be 1.4 (25 Ω) = 35 Ω and from equation (1) C = 5.2 PF. From B to D is a length of transmission

device is designed with the low frequency grating lines appearing closest to the transducers and traversing up the media of proportion. As the frequency increases the grating line spacing will physically get closed together through the band of interest. This is opposite for down-chirp devices. The up-chirp IMCON can operate from 4 MHz to 24 MHz with 50% bandwidths. Down-chirp devices do have some bandwidth limitations due to undesired accustic modes[4], but can be implemented as long as the bandwidth is under 10%. IMCONs can be designed depending on a customer's preference as linear FM or non-linear FM. The NLFM IMCON has a slope which will vary across its operating band.

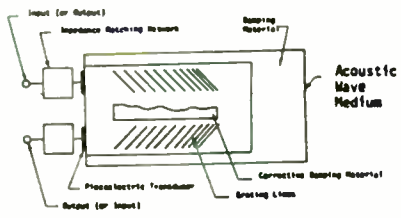

FIGURE 4: SAW RAC/IMCON Structure

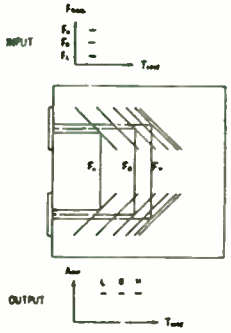

FIGURE 5: SAW RAC/IMCON UP-CHIRP FREQUENCY DISPERSION

SAW RAC TECHNOLOGY

Within the last 10 years the SAW device has become the "most common high throughput analog device for pulse compression techniques"[5]. Center frequencies as high as 1 GHz are being developed and soon will be able to be commercially fabricated. Dispersions of 100 µs, bandwidths of 500 MHz, and sidelobes of -40dB can be realized within the laboratory under tightly controlled manufacturing tolerances. The advantage of the SAW RAC over most other analog devices and the digital counterpart is its size, weight, cost and reliability.

The surface acoustic wave reflective array compressor (SAW RAC) is the SAW technology counterpart to the IMCON. The SAW RAC is conceptually similar in structure to the IMCON in that grating lines are etched into a substrate such as lithium niobate, or other, depending on the user's applicable environment. The SAW RAC offers practical methods of achieving linear and non-linear FM dispersive delay characteristics. Using ion beam etching, grating lines can be etched into a substrate in varying depths to achieve the user's required amplitude/frequency weighting characteristics. Grating lines can be positioned if required to achieve the above mentioned non-linear delay function.

The SAW RAC is most suited for moderate dispersions (<100 µsec), bandwidth capabilities from 20 MHz to 100 MHz and sidelobe performance of -35dB, typical, in the linear FM application.

The SAW RAC operates at center frequencies from 10 MHz to 1000 MHz and can be easily manufactured as up-chirp or down-chirp devices.

SAW RAC AND IMCON USE IN COMPRESSIVE RECEIVERS

The compressive receiver is a fast, active real time Fourier analysis receiver that has applications in ELINT/ESM surveillance. The IMCON or SAW RAC when configured in the compressive receiver will generate the linear sweep of the desired dispersion and analysis bandwidth. The linear sweep can be generated by impulsing the specific dispersive devices as in the case of a coherent system or the user may choose to do their own triggering of the chirp as in the non-coherent system.

line read from E to F as .0975 - .0609 = .0366. At 435 MHZ λ_o = 11808/435 = 27.14 inches and λ_g = (.4729) 27.14 = 12.836. From equation (4) this length of transmission line is .470 inches. The shunt capacitance from D to G is read from C and H as

$$(6)\ \frac{1}{X_1} - \frac{1}{X_2} = \frac{1}{X_C}$$

where X_C is the normalized reactance.

Therefore, $\frac{1}{.5} - \frac{1}{1.4} = \frac{1}{X_C}$ and X_C = .777. Unnormalizing and using equation (1), C = 9.4 PF. From G to J is a transmission line of length determined by I plus K where I = .0535 and K = .003. From equation (4) this length is .725 inches. The value of capacitance from J to M is read at L and N using equation (6) but now X_2 is a negative quantity since it's on the opposite side of the chart.

$$1/.142 - (-1/44) = 1/X_C$$

where X_C = .1415. From equation (1) and unnormalizing, C = 51.6 PF. The length of transmission line form M to P is read at O as .01558. This length is .200 inches. The impedance at P unnormalized is 1.8 - J.2 Ω which is the conjugate of the collector output impedance.

The input circuit is shown on Drawing #6. The input impedance at 435 MHZ is 1.75 + J2.65 Ω and is shown at A. The capacitance from A to B is measured at C plus D and computes to be 52 PF. The transmission line from B to E and measured at F plus G and computes to be .810 inches. The second capacitance from E to H read at I minus J is 8.7 PF. Another transmission line from H to M read at L minus K is .450 inches. Then the last capacitance from M to O measured at N is 4.9 PF which matches to 25 Ω .

The completed circuit is shown in Drawing #7 and provides excellent broadband performance. Typical performance shows in excess of 500 Watts at 400 MHZ through 430 MHZ and 480 Watts at 450 MHZ. The design is very stable with changes in power levels, changes in tuning and changes in collector voltage thus proving that the high pass design was the reason for some previous instability.

Conclusion:

The theory of a one to one balun was described along with two applications. Both applications have definite advantages. In no way does this device note intend to imply that the high pass configuration is inferior. However, the conclusion is drawn that its application is better suited to high power common emitter or lower power common base devices.

It is recommended that all baluns are characterized before being used in a new design. Experience proves that the additional time to characterize baluns is worth avoiding the frustration of not knowing whether an inoperable circuit is due to the balun or matching components.

The output of the dispersive device is a high energy expanded pulse with the designed dispersive content and analysis bandwidth.

PERFORMANCE OF A COMPRESSIVE RECEIVER

Now that the basic building blocks are understood we can begin to define some terminology within the receiver. This terminology will be helpful when the user is ready to draw up a technical specification of a compressive receiver.

SPECTRAL RESOLUTION COMPUTATIONS

Spectral resolution (δf), is defined as the smallest frequency deviation or difference that can be detected and accurately measured. Resolution down to the hundreds of Hertz can be achieved when large time bandwidth products are implemented.

Resolution is defined as: $\delta f = \frac{P_b}{\Delta\tau}$

where δf = System Resolution

$\Delta\tau$ = System Dispersion

P_b = Pulse Broadening Factor as a result of a weighting function being used to suppress temporal sidelobes. For example, when $P_b = 1.0$ this is a typical pulse broadening factor for no weighting; when $P_b = 1.5$ this is a typical pulse broadening factor for a Taylor weighting of 47-50dB.

PROCESSING TIME COMPUTATIONS

Processing time is defined as the amount of time the compressive receiver needs to analyze an incoming frequency spectrum once it has been captured within the analysis band and display the Fourier transform at the output as a function of time.

Processing time is defined as. $P_t = K(\Delta\tau) + t$

where P_t = Signal Processing Time

K = Multiplication factor for the number of cascaded compressive receivers

$\Delta\tau$ = System Dispersion

t = Delay Time attributed to non-dispersive devices, i.e., mixers, bandpass filters, etc.

PULSE WIDTH COMPUTATIONS

Pulse width measurements can be defined as:

$$\text{-4dB pulse width} = \frac{P_b}{\Delta\tau}$$

where P_b = Pulse Broadening Factor as a result of a weighting function being used to suppress temporal sidelobes

Δf = Analysis Bandwidth

NAME	TITLE	DWG. NO.
D'Agostino	1565 Engineering Prototype	1
SMITH CHART FORM 6283PR (2-49)	RAY ELECTRIC COMPANY, PINE BROOK, N.J. ©1949 PRINTED IN U.S.A.	DATE

Supersedes G R Form 5301 7560 N

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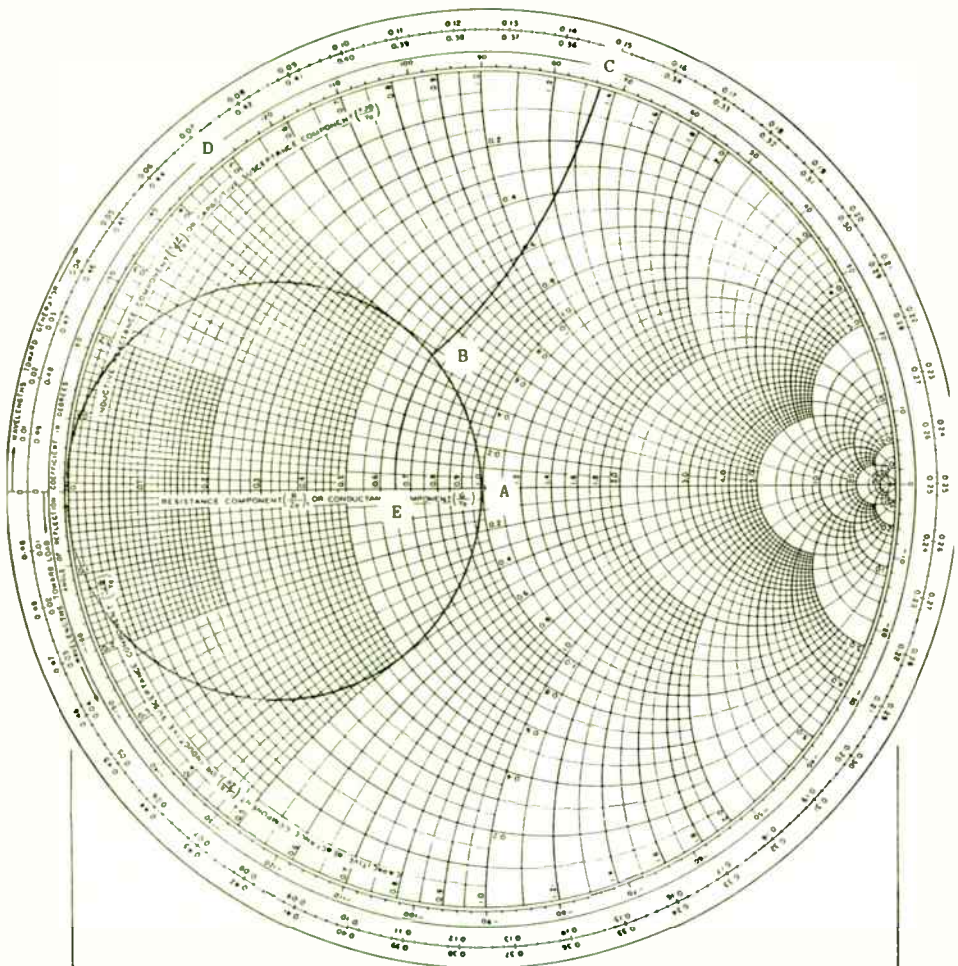

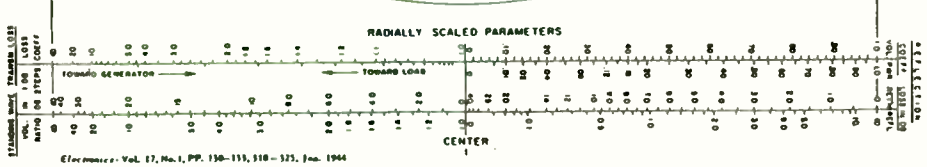

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NAME	TITLE	DWG. NO.
D'Agostino	1565 Engineering Prototype	2
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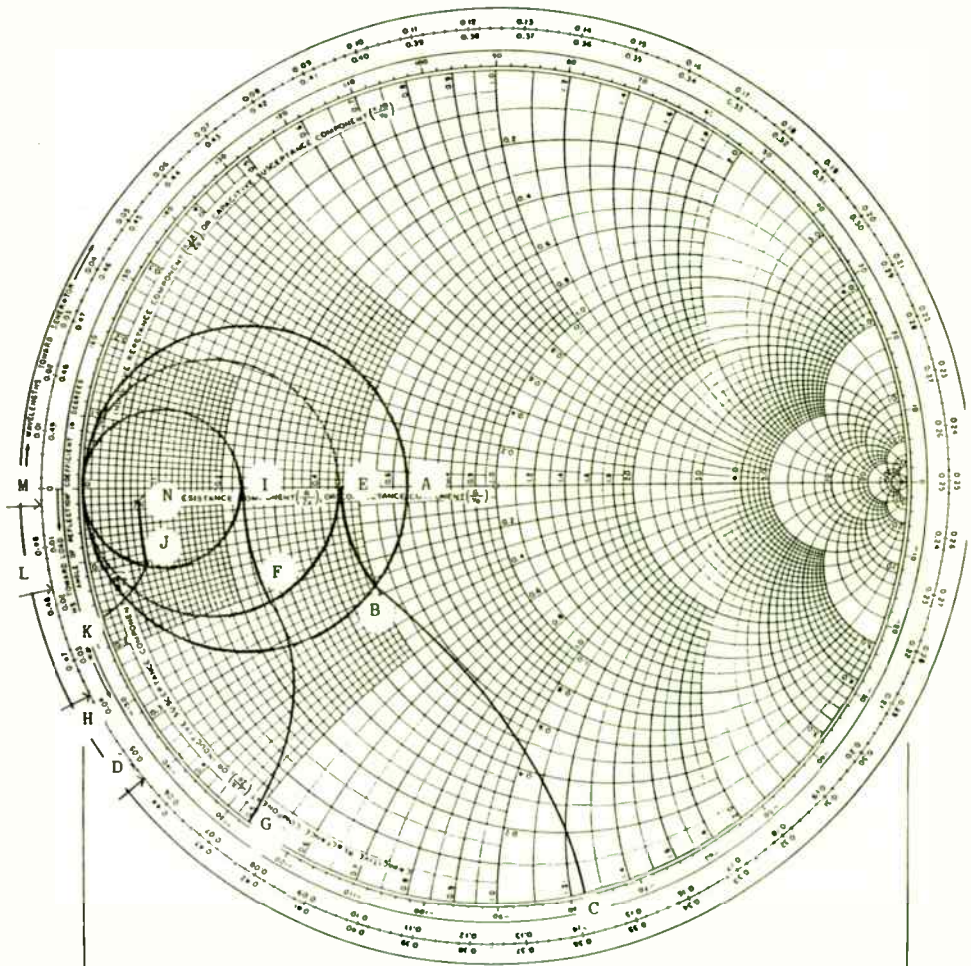
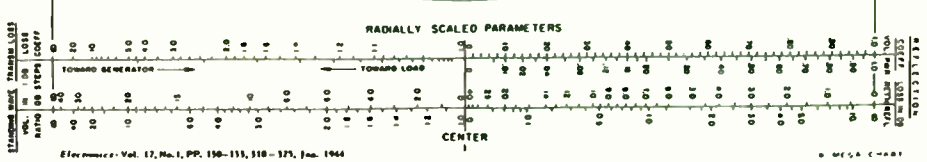




Electronics - Vol. 17, No. 1, PP. 150–153, 310–325, Jan. 1944

POI COMPUTATIONS

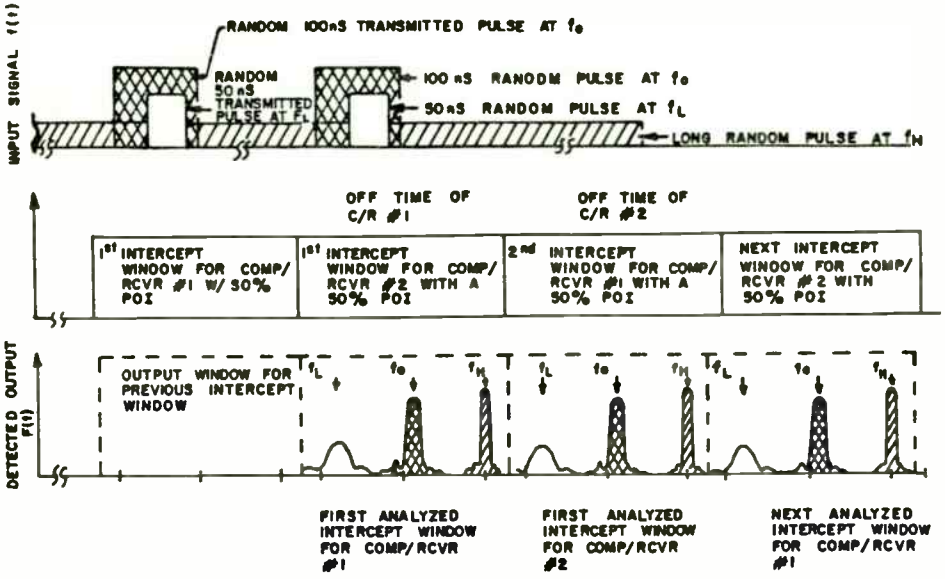
Probability of intercept is defined as the chance that a signal, if present within a given frequency/time spectra, will be detected.

POI for a compressive receiver can be defined as a minimum of 50%. This is characterized by:

$$\frac{\Delta\tau}{\text{Pulse Repetition Time}}$$

where $\Delta\tau$ = system dispersion.

Any signal which is captured within the ramp of the chirp will be displayed as a Fourier transform. If two compressive receivers were to be run so that their "chirps" were to share some overlap time, Figure 6, a 100% POI would be guaranteed!



100% GUARANTEED POI
COMP/RCVR SYSTEM
BLOCK DIAGRAM
FIGURE 6

CONCLUSION

The use of such devices as SAW and IMCON technology give the compressive receiver the flexibility, low cost and low complexity that is required when designing signal processing radar systems. These technologies give a user the necessary requirements of excellent resolution, wide band surveillance and true fast Fourier analysis of all types of incoming signatures which are present within the EW/ECM environment. When the IF spectrum is to be analyzed, IMCON and SAW analog technology should be the system designer's choice.

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5. Brookner. Eli, "Trends in Radar Signal Processing", Microwave Journal, October 1982.

NAME	TITLE	DWG. NO.
D'Agostino	1565 Engineering Prototype	3
SMITH CHART FORM 8283PR (2-48)	RAY ELECTRIC COMPANY, PINE BROOK, N.J. ©1948 PRINTED IN U.S.A.	DATE

Somersedes G R Form 5301 7560 N

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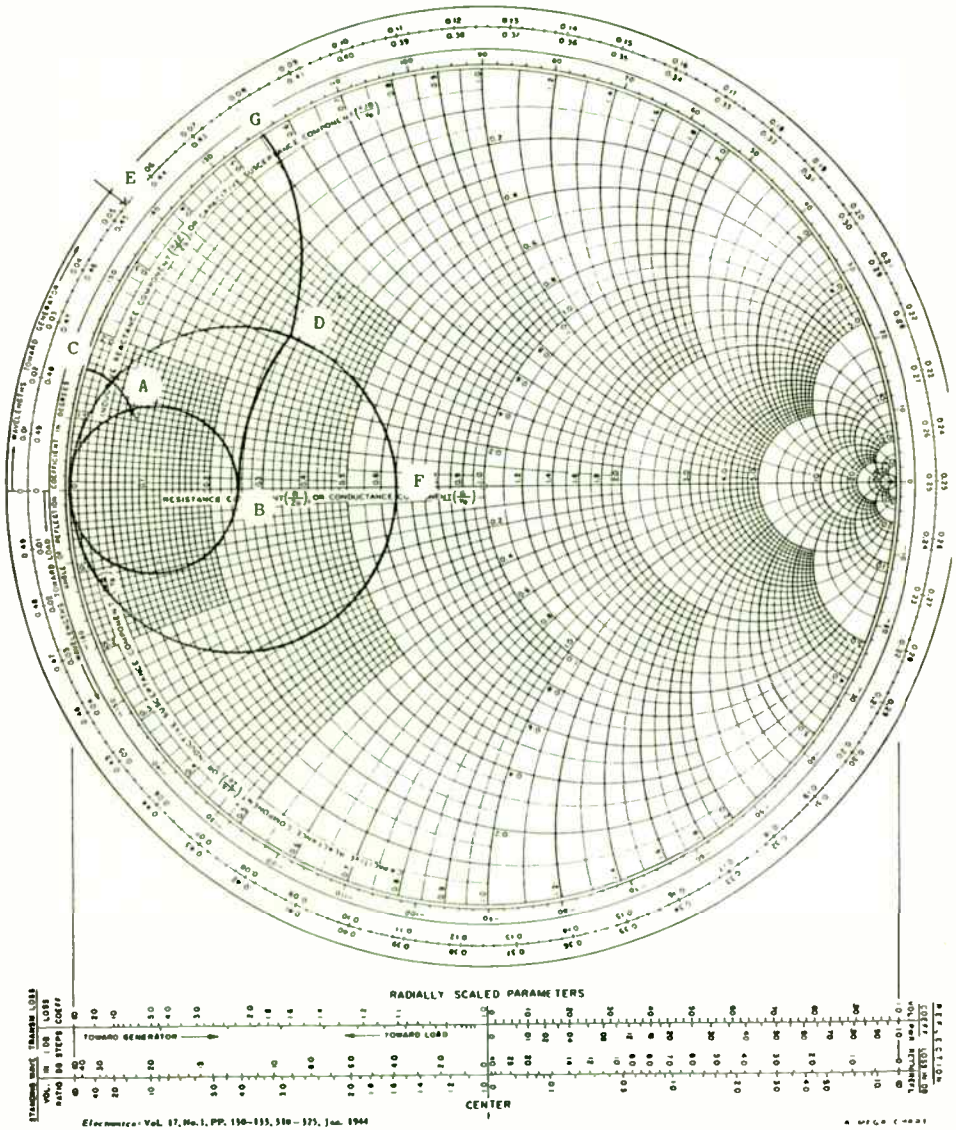


Electronics, Vol. 17, No. 1, PP. 156–155, 310–325, Jan. 1944

Drawing # 4

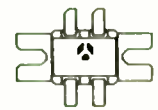
THOMSON-CSF

MONTGOMERYVILLE, PENNSYLVANIA

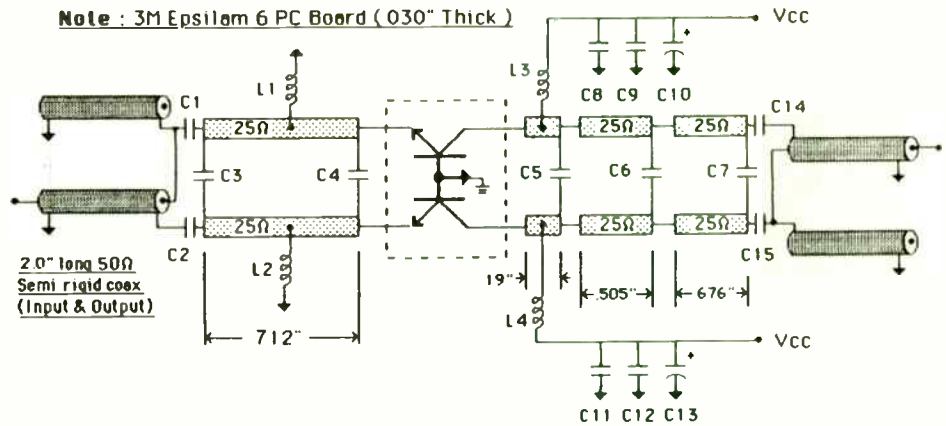
SEMICONDUCTOR DIVISION

SD1565-H0
Circuit Diagram
425 MHz Engineering
Prototype

.400 X .500
4 Lead Flange



Note : 3M Epsilam 6 PC Board (030" Thick)



Component	C1,C2,C14,C15	C3	C4	C5	C6	C7	C8,C11	C9,C12	C10,C13	L1,L2,L3,L4
Value	32	13	50	48	15	5	1	1000	1000	12 5 Turns Number 24 Wire
Units	pF	pF	pF	pF	pF	pF	µF	pF	µF	

Comments: This engineering prototype circuit works well but it is unstable on drive up Once the circuit is into saturation the stability is fine

NAME	TITLE	DWG. NO.
D'Agostino	1565 Broadband Circuit	5
SMITH CHART FORM 828SPR (2-48)	RAY ELECTRIC COMPANY, PINE BROOK, N.J. ©1948 PRINTED IN U.S.A.	DATE

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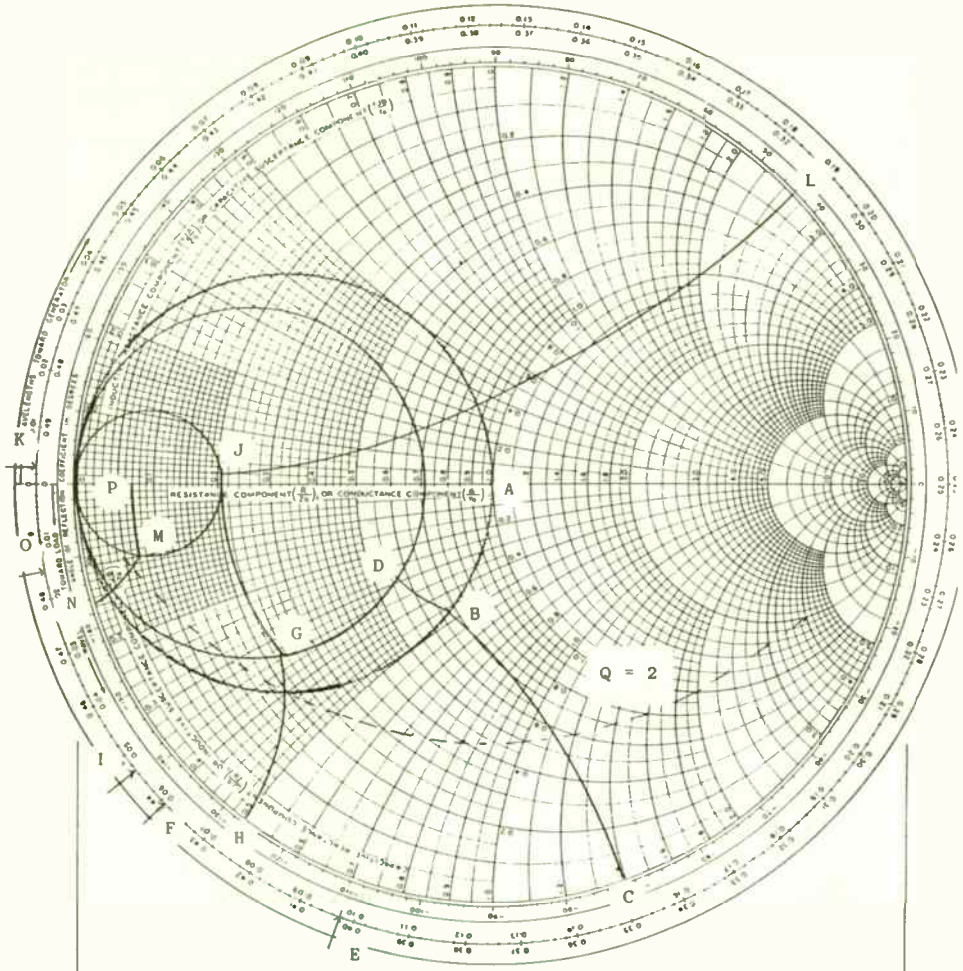
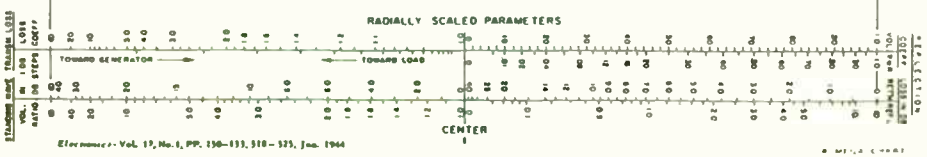


RADIALLY SCALED PARAMETERS



Electronics - Vol. 17, No. 1, PP. 130–133, 310–325, Jan. 1944

NAME	TITLE	DWG. NO.
D'Agostino	1565 Broadband Circuit	6
SMITH CHART FORM 828SPR (2-48)	RAY ELECTRIC COMPANY, PINE BROOK, N.J. ©1948 PRINTED IN U.S.A.	DATE

Somersetes G.R. Form 5301 7560 N

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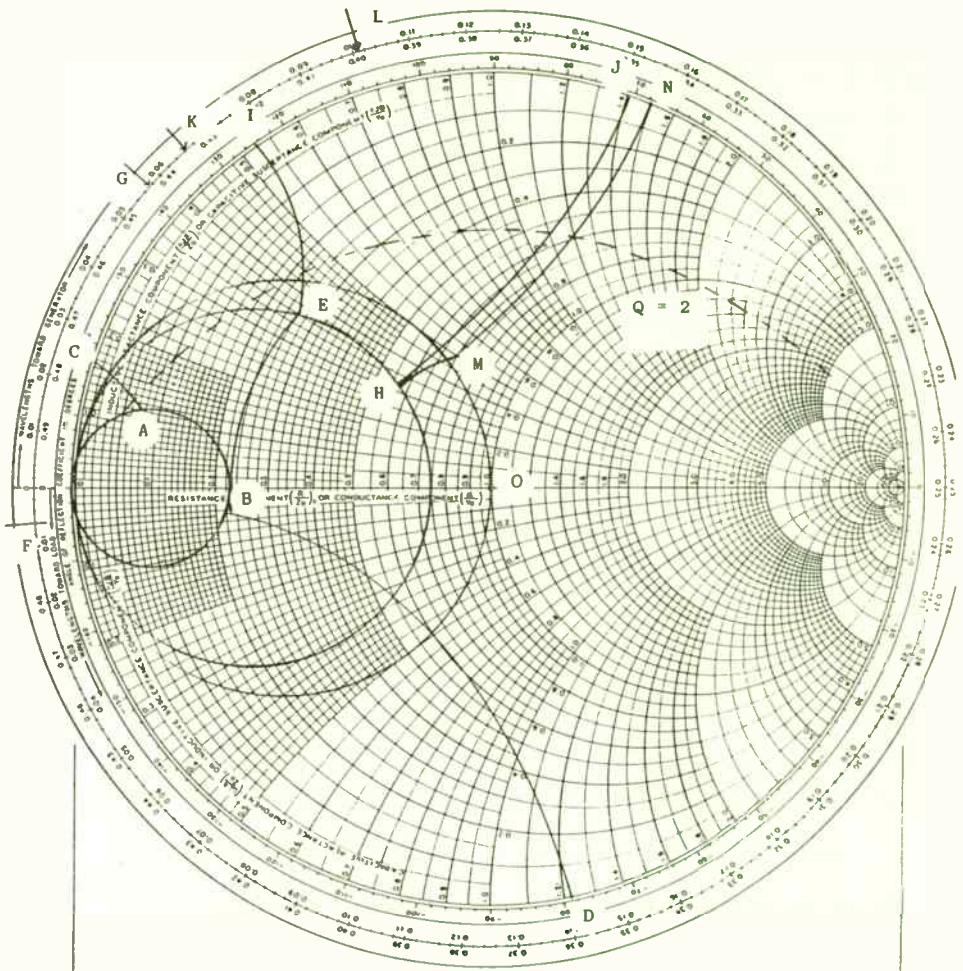

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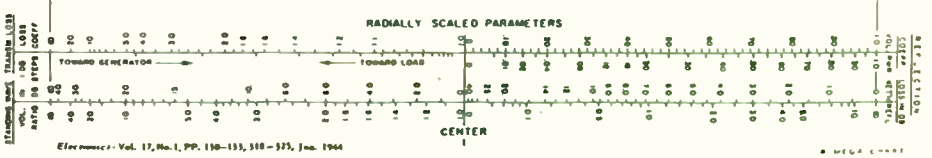


Electronics - Vol. 17, No. 1, PP. 130–133, 310–325, Jan. 1944

DIGITAL - RF INTERFACING

The Story of a Marriage

by

Robert W. Sproul

Vice President, Director of Engineering

Lorch Electronics Corp.

submitted to

RF DESIGN RF EXPO EAST

NOV. 1986

My story begins in a far-off place, many years ago, at the time of the flood. All creatures of the earth boarded the Ark in pairs, two by two. Noah, the engineer in charge of construction, selected at the last moment his final pair, a couple of engineers. One was an RF engineer, the other of the digital persuasion.

Since then, the two disciplines have prospered in their separate ways, managing until recently to avoid much contact with each other. Within the last few years, however, the cultural restraints of the past have been thrust aside, and we are now in an era of fruitful cooperation.

The disciplines of RF and Digital have joined forces. The place where they have met is called the interface. Fraught with problems and tensions of protocol, this boundary is important and deserves our attention .

Three factors make the digital-RF interface increasingly important:

First, the systems of today call for sophisticated, almost symphonic control of a large number of separate elements, be they antennas, phase shifters, attenuators or separate signal paths, etc., etc. The individual contributions of these elements are combined and manipulated by computer programs to create powerful systems.

Second, the necessary digitally controlled components are available today to control the phase, attenuation and routing of RF signals; (RF and IF are considered equals in this discussion).

Third, computer programs and control systems are available to give, receive and digest information to and from RF equipment.

Where is the RF-Digital interface? Precisely where does RF become digital? This is rather like asking where the source of the Nile is. The most obvious case is that of a digitally controlled RF component, in the form of an attenuator, phase shifter, multi-pole electronic switch or switch matrix, to name a few. Inside each such package, the designer has to do what is required so that the unit will perform its function when addressed digitally by the user. The component designer thus provides the first interface, but he does it in private, as it were. As long as he remains consistent with an accepted method of address, he can do what he wants inside his box, and in that sense he has few problems with this first interface, most of which is hidden mercifully from view.

THOMSON-CSF

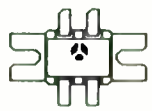
MONTGOMERYVILLE, PENNSYLVANIA

SEMICONDUCTOR DIVISION

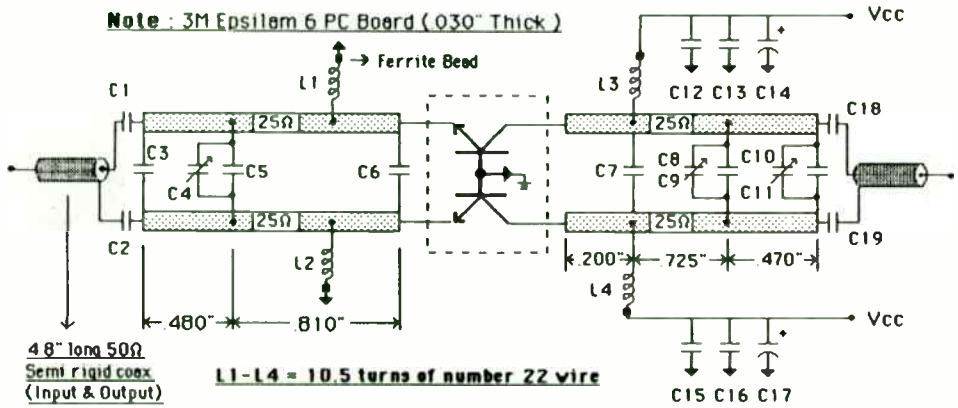
Drawing # 7

SD1565-H0
Circuit Diagram
425 MHz Wide Band

.400 X .500
4 Lead Flange



Note : 3M Epsilam 6 PC Board (.030" Thick)



L1-L4 = 10.5 turns of number 22 wire

Component	C1,C2,C18,C19	C3,C11	C4,C10	C5	C6,C7	C8	C9	C14,C17	C15,C18	C16,C19
Value	470	5	4-40	8	52	8-80	7	.1	1000	1000
Units	pF	pF	pF	pF	pF	pF	pF	µF	pF	µF

Symbols	Values			Units	Test Conditions
	Min.	Typ	Max.		
Po *	500.0	-	-	W	f = 425MHz Vce = 40.0V Pin = 54W
Po *	450.0	480.0	-	W	f = 400 - 450 MHz Vce = 40.0V
Nc	50.0	55.0	-	%	f = 425MHz Vce = 40.0V Po = 500W
VSWR**	-	30:1	-	-	f = 425Mhz Vce = 40.0V Po = 500W

*Pulse Width 250µS, 10% Duty Cycle

**All Phase Angles

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If we assume that our RF designer is producing an RF receiver, then he will soon have the confidence to group various components, each digitally controlled, into a complete, self-contained design. Now he has to face a different, and more scary, interface, because in the outside world strangers will want to talk to his machine, and he will not be able to cover up little idiosyncrasies as he could in the privacy of his own domain.

In that sense the first true interface is the public one, where the digitally controlled component, sealed in its own container and provided with connections and data sheet, meets its alien user. As units became more complex, and as major assemblies are separated physically from each other by greater distances, the interface changes in nature, and requires quite different approaches. Most of these latter interface considerations can be said to be purely digital in nature, and no longer of the RF sort, but in this age of increasing complexity it behoves the RF engineer to become more aware of the overall digital scene, and certainly the digital engineer can learn from the RF engineer, particularly in terms of processing high frequency bit-streams.

One aspect of the interface is that of architecture, the 'big picture', in which the flow of information is studied in terms of systems such as the IEEE-488 bus and its associates, for example the economical and hard-working RS-422C and variants. References thereto are appended to this paper.

The other aspect concerns the nitty-gritty detail of interfacing, at the level where wire meets wire and voltage meets current. This aspect, in the experience of this speaker, is the most problematic, and gives the greatest opportunity for creative chaos. My company supplies digitally controlled components to the industry, and I believe it is appropriate to discuss some of the practical problems that have risen with the interface. Some of them may sound silly and obvious, but all have caused problems at one time or another for those peering across the Digital-RF frontier. The list is unending, but I have selected a few of the more obvious.

Any discussion of interface detail must begin with Transistor-Transistor Logic, or TTL, which has truly become the day-to-day language, the lingua franca, of RF-Digital interfacing. Most RF engineers have heard of TTL, and know that it uses two voltage levels to represent the two states of the binary system; a low voltage of about zero represents a '0', while a high voltage of plus 5 or so represents a '1'. Right?.....WRONG!

The above statement epitomizes the type of misunderstanding that can make life difficult. Figure 1 illustrates my own first attempt, many years ago, to test a TTL device. When switch S was open, voltage Vi applied across the input of the gate was zero. When the switch was closed, Vi became +5V. Should have worked! All digitally literate persons in the audience will smirk at such innocence, but I found later that a lot of people had been down this particular alley, to their later chagrin.

Figure 2 uses a typical TTL interface to demonstrate what was wrong. At the left is a TTL gate output of the open-collector type, which uses R1 to provide the collector of transistor Q1 with positive voltage. Sometimes a transistor is used to perform the function of R1, and the output is referred to quaintly as a 'totem pole'. R1 is also connected to the emitter of gate input transistor Q2.

When the base of Q1 is biased 'on', base and collector currents ib and ic flow, the latter being predominantly from the emitter of Q2, since R1 is of high resistance. Inter-stage voltage Vi changes from +5V to about +0.3V, with the flow of emitter current Ie from Q2 thru Q1 to ground. The effect on Q2 is to lower the collector voltage, cutting off transistor Q3 and changing the state of gate 2. It is interesting to see how TTL evolved as an improved version of the earlier Diode-Transistor-Logic, or DTL. The circular inset of Figure 2 shows how the diodes of DTL became the transistor of TTL. Note that the input voltage Vi indeed changed from +5V to +0.3V, just as the test circuit of Figure 1 was meant to simulate; the difference is that something else happened too. Transistor Q1 of gate 1 acted as a sink, permitting emitter current from input transistor Q2 to flow, thus initiating the state-change process in gate 2. Table 1 summarises the action.

A full discussion of the exact operating criteria for proper TTL operation is beyond the scope of this paper, (the interested are encouraged to read the attached References), but already we can see the important truth that TTL operation is first and foremost concerned with impedance change, in this case from the emitter of Q2 to ground. Anything that causes that impedance, or simply resistance, to change efficiently from a low to a high value will operate the TTL gate properly. A screwdriver held from emitter to ground will do just fine. The +5V level at the input is not essential, but enhances noise immunity in practical systems, by ensuring that transistor Q2 is held 'off' even when noise spikes of a few volts are present.

A 350 Mhz Dual-gate GaAs FET Frequency Multiplier

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Abstract

This paper describes a dual-gate FET frequency multiplier with 13 dB conversion gain for an input frequency of 350 Mhz. The bias on the second gate provides gain control in excess of 40 dB while maintaining better than 20 dB return loss.

I. Introduction

Since its development in 1966 [1], the GaAs MESFET has continually increased in popularity. In its youth, the GaAs MESFET was used almost exclusively in high microwave frequency and low noise applications where low cost silicon transistors were not functional. An increased interest in GaAs technology has produced a variety of GaAs FETs including the dual-gate GaAs FET which was developed in 1971 [2]. The dual-gate FET has been widely used in mixers, variable gain amplifiers, and in modulators [3]-[5]. It has also been reported as a frequency multiplier with 8 dB conversion gain at Ku band [6].

Eventually, fabrication techniques have brought the cost down, and the high volume demand of such industries as mobile cellular radio has in particular brought about the development of a low frequency (less than 1 GHz), low cost dual-gate GaAs FET.

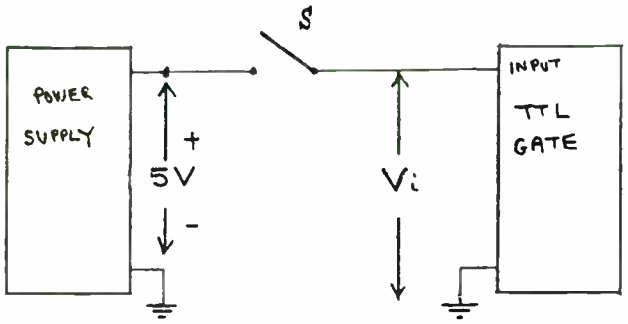
The purpose of this paper is to demonstrate the feasibility of using a low cost dual-gate GaAs FET as a frequency multiplier and to indicate the important parameters in the design of this multiplier. This paper presents the design of a frequency doubler with 10 dBm output power and 13 dB conversion gain for an input frequency of 350Mhz.

II. The Dual-gate FET

The characteristics of the dual-gate FET have been well documented [1]-[6], and will be presented here as a brief summary. The forward transconductance of a dual-gate FET has inherent non-linear characteristics which can be used to generate harmonics of the drive frequency. The addition of a second gate provides a simple means to vary the device gain, with little effect on the characteristics of the first gate. In addition, with proper RF termination of the second gate, the dual-gate FET has higher gain than the single-gate FET of the same width [3].

III. Circuit Description

The dual-gate FET multipier can be used in a variety of applications requiring frequency doubling and gain control. The application discussed here is the replacement of current



S	Vi
OPEN	0
CLOSED	+5

FIG 1
HOW NOT TO CONTROL A TTL GATE

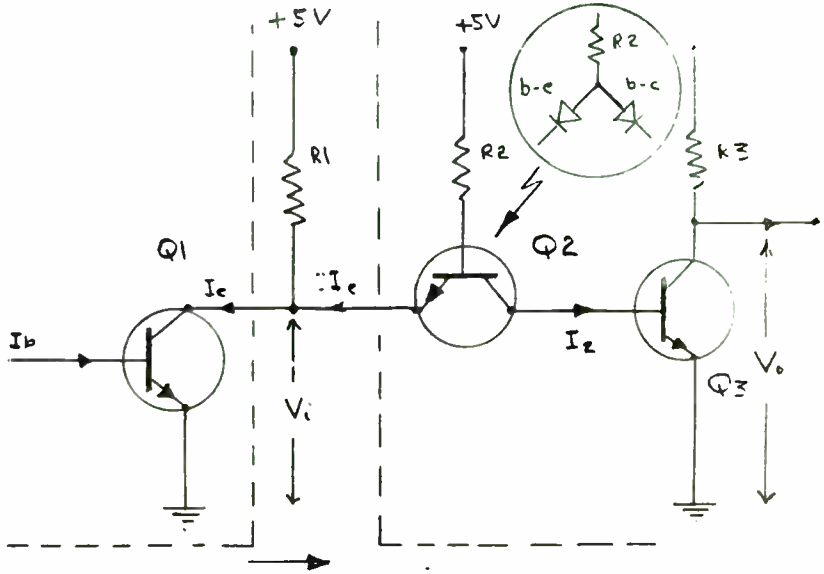


TABLE 1

I_b mA	V_i V	I_e mA	I_2 mA	V_o V
0	4.5	0	2	.3
2	.3	2	0	4.5

FIG 2
BASIC TTL INTERFACE

circuitry which consists of a PIN diode attenuator and a bipolar multiplier. The redesign was motivated by three factors: first, the PIN diode attenuator reqires a fairly large amount of board space; second, the attenuator requires more current than can be provided by a common Op-amp, thus requiring additonal transistors for current supply; finally, the dual-gate FET is much easier to bias since the bias on the PIN diodes must inversely track each other to maintain 50 ohms input and output impedances.

In order to be a functional replacement for the present circuitry, the dual-gate FET doubler is required to deliver an output power ranging from +8 dBm to -7 dBm with an input power to the multipier of -3 dBm at 350 Mhz.

The multiplying device used for this circuit is an MRF967. However, for commercial applications, the MRF966 or NEC's NE41137 could be used. The multiplier is constructed on 30 mil Teflon glass with 50 ohms input and output impedances.

With sufficient RF voltage at the first gate, the FET generates harmonics in the drain current due to its non-linear transfer characteristics. The output circuit filters the desired harmonic while reflecting the unwanted components. It is important that at the fundamental frequency the filter produce a low impedance on the drain rather than a high impedance because, for a given peak drain voltage, any voltage at the fundamental frequency requires a corresponding decrease in the peak voltage of the second harmonic. Also, for power efficiency, it is important that there be a reactive load for the higher order harmonics. A square wave at 2 Fo yields a voltage component at 2 Fo of 1.3 times the voltage of the square wave. This suggests that the drain voltage should include odd harmonics of 2 Fo.

An output filter which is an open circuit above 2 Fo provides a means for the higher harmonic voltages to add to the second harmonic voltage to produce a square wave. In contrast, a filter that becomes short circuited at higher harmonics could also be used to reflect those components, but would reduce the possibility of generating a square wave voltage at the drain. Both types of filters were used, and while the open circuit filter gave better results, it is believed that this is a result of better reflection of the unwanted harmonics rather than improved drain voltage wave form.

Figures 1a and 1b show the drain voltage and output spectrum, respectively, with the short circuit filter, while Figures 1c and 1d show the results with the open circuit filter. The figures show that the wave shape of the drain voltage is not an improved square wave when using the open circuit filter, however, the unwanted harmonics are better suppressed. It is believed that the reason the open circuit did not produce a square wave is that the harmonics were not added in proper phase. In fact, the filter was replaced with two quarter-wave stubs such that the impedance was a short at all odd harmonics of Fo, passed 2 Fo, was a short at even harmonics of 2 Fo and an open at odd

Figure 3 shows a practical TTL test circuit at the right, compared with the original non-working circuit of Figure 1 at the left. The value of the resistor R is arbitrary within limits; 3K ohms is reasonable. When switch S2 is open, the gate input is high impedance and held high to +5V. When S2 is closed, the input voltage is close to zero and a low impedance permits the emitter current of the input gate to flow unimpeded.

The above does not mean that the TTL recommended levels corresponding to '1' and '0' are unimporant; it is just that a gate input will of its own accord assume the appropriate voltages if the proper high or low impedance connections are made to it. You never 'apply' the correct voltages to it. If, for example, the sink path impedance connected to the gate input is too high, then the emitter current to ground will cause too high a voltage drop, and the emitter bias will not permit proper gate operation. In that case the input voltage will exceed the specified maximum.

While these considerations are important when testing a TTL unit, they are equally important in normal circuit design. For example, the output of a TTL gate that will 'feed' the input of another has a finite sink current capability. If more current has to be sunk than can be handled by the gate output, then the emitter voltage of the input gate will become too high and exceed permitted limits.

Figure 4 illustrates this point. Assume that, for some reason, a total of twenty gate inputs are connected in parallel and have to be driven from a TTL source. The emitters of the input transistors, Q1 thru Q20, each carry a normal sink current of about 1.6 mA. (This is standard for TTL, although it is sensible always to check the handbook for the sink requirements of a particular gate). The total sink current is then 32mA.

If the twenty input gates of the figure are hidden, being enclosed within a digital attenuator or like device, then a problem can arise when the user of the device goes to provide a TTL control driver. All he has been told is that the attenuator is TTL compatible, and he may assume that a normal low-current gate will do the job, providing a maximum sink current capability of 16mA. The interface will not work, and a lot of effort may be expended finding out why.

The answer here is to tell the user more detail about the required interface, and this is done by adding the note 'TTL compatible, 20 standard loads'. It will be realized that this is a very unusual case, but it is not at all unusual to have two gates in parallel, and to find that the driver

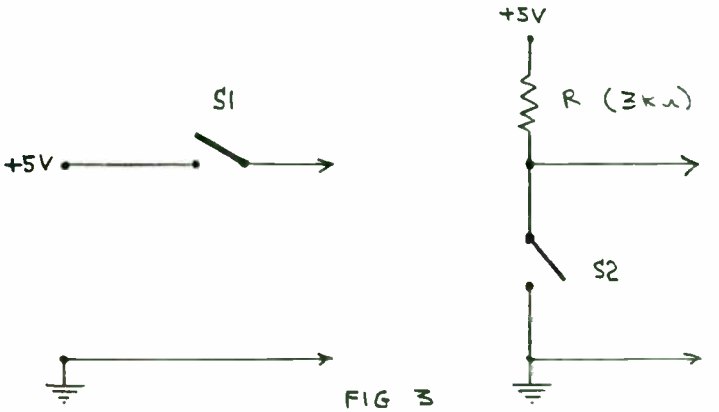


FIG 3

TEST CIRCUITS

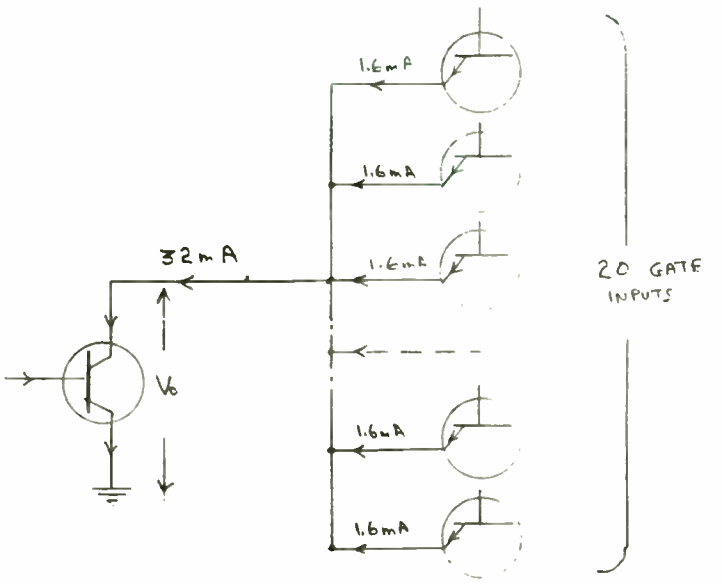
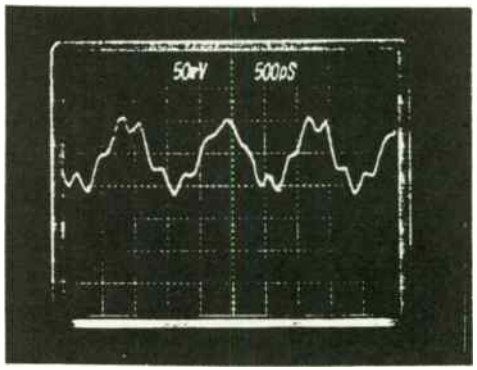
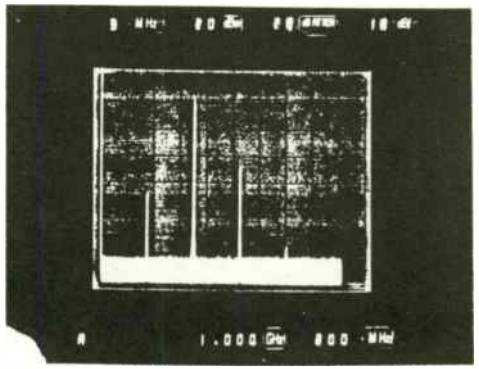


FIG 4

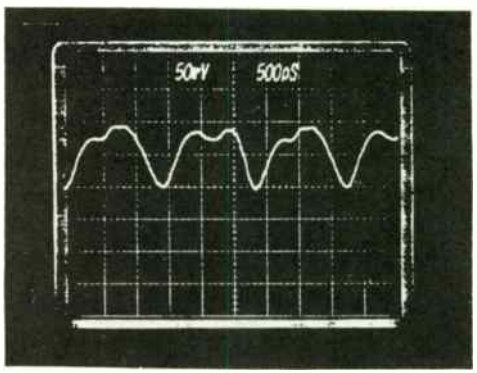
OVERLOAD



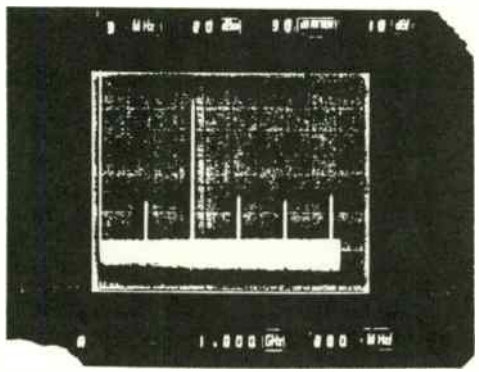
(a)



(b)



(c)



(d)

Figure 1. Drain voltage and output spectrum of multiplier different filter schemes. (a) and (b) correspond to a short circuit filter, (c) and (d) correspind to an open ciruit filter. NOTE: The voltages in (a) and (c) were measured through a resistive divider which corresponds to 5V/div.

harmonics of 2 Fo. This is the condition required for generating a square wave at 2 Fo; however, the odd harmonics of 2 Fo added to the voltage produced by the 2 Fo component in the wrong phase, and instead of a square wave, it produced a triangle wave which degraded performance. This experiment tends to verify the assumption that the improved performance due to an open circuit filter was the result of better filtering.

It has also been demonstrated that a reactive termination at the second gate is very important in maximizing gain [3]. A sliding short was used for RF termination on gate 2 to allow adjustments of the reactance in order to optimize conversion gain.

Finally, a triple stub tuner on the output and a series and shunt variable capacitor on the input were used to match into 50 ohms.

IV. Circuit Optimization

Figure 2 shows the circuit schematic. With Vd set at 5 volts and P_{in} at -3 dBm, Vg1, Vg2, the termination at g2, and the load impedance were simultaneously adjusted to give maximum conversion gain. The first attempt at optimizing the circuit was done by optimizing the gain with respect to one variable, then holding that variable constant, optimizing with respect to another variable, and then the next variable, etc., and continuing again with the first variable until all variables were

gate was feeding other gates in addition to those of the attenuator in question. If told how many standard loads have to be sunk, the user can provide a high-current driver gate or take other precautions.

A further caveat. You may recall my associating the low-voltage state with digital '0', and the high-voltage state with a '1'. Beware! Your digital engineer can get very tricky with things like "negative logic, active low", and you can find , too late and to your expensive embarrassment, that he meant 'TTL 1 = low '. The safest thing for the RF engineer to do is refer to the states as 'TTL High', and 'TTL Low' or even 'TTL Low Voltage', etc. In the case of a digital attenuator, for example, the specification should then read:

'TTL high = 0dB, TTL low = xxdB'

Rather than:

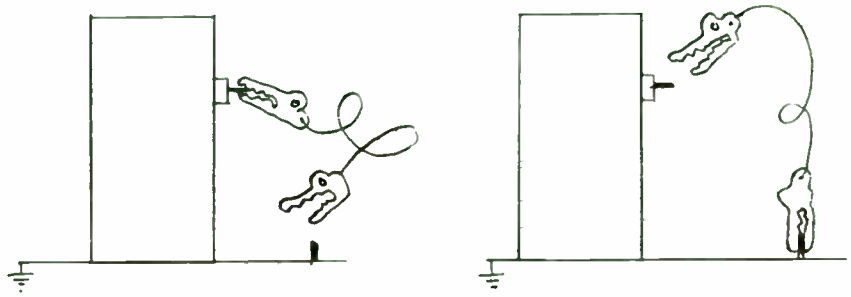
'TTL 1 = 0dB, TTL 0 = xxdB'

Such a message rings loud and clear across the interface. Never proceed with a design until this matter is fully clarified. You may get laughed at for being pedantic, but he who laughs last laughs within budget and delivers on time.

It was pointed out earlier that a TTL device can be tested by making a simple metallic, e.g. screwdriver, connection from TTL input to ground. Figure 5 shows how not to do that, and raises an important point about handling devices safely without impairing reliability.

Whether it is a screwdriver or an alligator clip held in the hand, the wrong method, i.e. touch the input and then ground it, can result in destruction of the unit, because of the static charge that can build up on hands and other things that may touch the input. In the right method, the grounded metal is applied to the input. Small difference, big effect! Such a circumstance may not be likely to arise in a completed design, but many a chip has gone to its reward at Incoming Inspection, at the hands of a dedicated inspector who wanted to make sure the thing was working properly, and who did not have specialized test equipment to test all the different devices that cross his bench.

Fortunately, TTL devices are remarkably rugged and under most circumstances do not require special handling as some CMOS and diode assemblies do, with grounded wrists and conductive floor mats. Simple good manners and common sense will usually suffice.



WRONG FIG 5 RIGHT

GROUNDING

Earlier we encountered Open-Collector and Totem-Pole TTL output circuits, each of which has its place in classical digital practice. One facet of their use can be exploited by the RF engineer. Figure 6 shows the two types side-by-side, with each in the high output state. In the case of the open-collector output, the circuit is defined fully by the values of Vcc and R, both of which can be known with precision; if some analog function is to be operated by the output, it can be properly designed. In the case of the totem-pole circuit, the exact value of the open-circuit voltage is dependent on a number of variables, and cannot be known as precisely. The primary reason for the totem-pole's use is in achieving speed of operation, as the output is driven high.

The one area where the digital engineer can learn from his RF colleague is that of high speed operation. TTL gates are available with operating times in the region of a few nanoseconds. In addition, the gates of TTL include very high gain amplifiers that limit severely to form the square waves we all enjoy; but they are still very high gain devices with enormous bandwidths. In terms of RF amplifiers, we are dealing with units having gains of 40 to 60 dB, and bandwidths of DC to several hundred Megahetrtz. Whereas the RF engineer would shield such boxes and have them on a proper ground plane with short interconnecting leads, the digital world tends still to think in terms of plastic devices mounted on boards having no effective ground plane, and with long, thin wire interconnections. Shame on them! They deserve the oscillations, crosstalk and ringing they get.

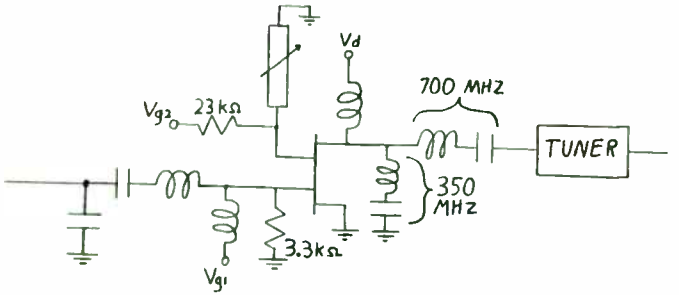


Figure 2. Circuit schematic showing open circuit type output filter.

optimized. It was found that by setting the voltage at g1 and adjusting the other variables a maximum could be reached where changes in Vg1 or any other variable only degraded performance, which indicated that the circuit was optimized. However, by setting Vg1 at a different value and re-optimizing the other variables, a different optimum (sometimes better) was reached. The same phenomenon was observed when holding any other variable constant. Therefore, one could not simply tune each variable one at a time and arrive at the global optimum. It was observed, however, that the optimum position of the sliding short did not change much from one optimum to the next, thus giving a good starting point for that variable. The optimum Vg1 and Vg2 were found by plotting optimum gain against set values of Vg1 and Vg2. This data was found by starting at a fixed Vg1 and Vg2, adjusting

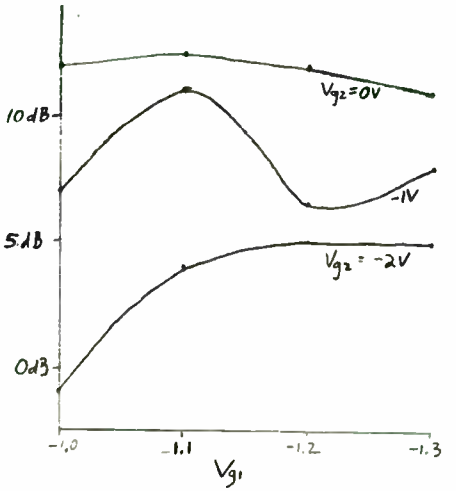


Figure 3. Optimum gain vs. Vg1 with Vg2 as a parameter.

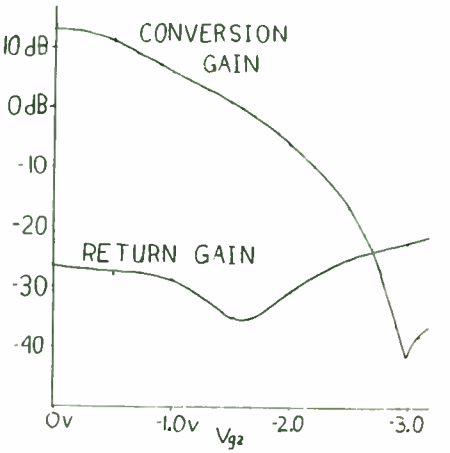


Figure 4. conversion gain and return loss vs. Vg2.

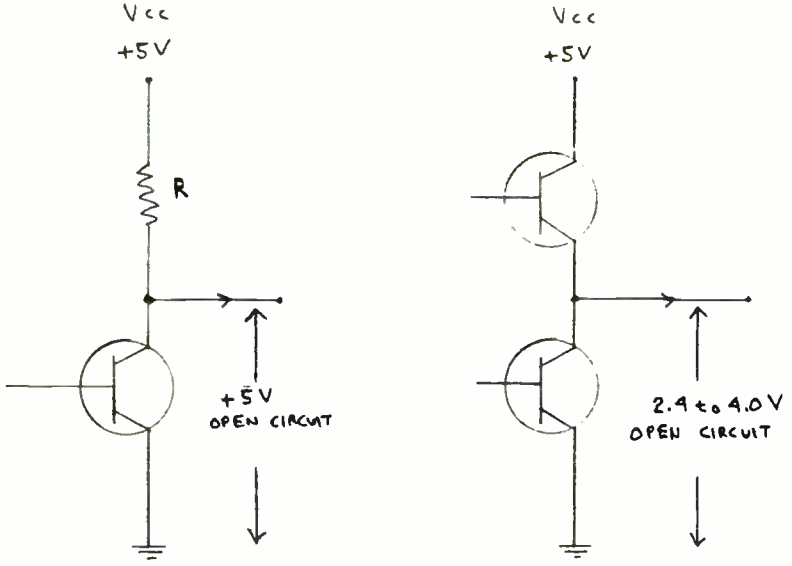
the output impedance to its optimum, and then adjusting the sliding short to its optimum position. The gain was then recorded, Vg2 was incremented, and the circuit was optimized again. After repeating this over the range of Vg2, Vg1 was incremented, Vg2 reset, and the process was repeated. This process gave the plot of optimum gain vs. Vg1 and Vg2 which was used to determine optimum bias conditions.

V. Results

The gain data obtained from optimizing at various bias conditions is shown in Figure 3. The optimum bias was determined

Similarly, when high-speed digital bit streams have to be transported more than an inch or so, there is an ancient body of transmission line theory and practice available to the digital engineer from the earliest days of radio, so that he can improve his systems without reinventing the wheel. Such knowledge deals directly with the problems of delay, circuit ringing, reflections, etc., that plagued the engineers who laid the first trans-Atlantic cable eons ago.

What I have tried to do is highlight some of the problems of the Digital-RF interface in practical terms; there is a long way to go, but it looks as if the artificial interface of mutual ignorance is being broken down, to the benifit of both camps. We now have reached another interface - that between this talk and the next. Thank you for listening.



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from Figure 3 to be -1.1 volts at g1 and 0 volts at g2. The corresponding termination on gate 2 was measured to have a reflection coefficient of 1/36deg. at 700 Mhz.

According to small signal theory, the optimum voltage on g2 should have been +2V [2],[3]. However, very little improvement was achieved here at higher voltages, and in fact, as Vg2 became positive,the circuit stability became very sensitive to changes in the termination at gate 2 and in the output circuitry.

With the variables held constant at the positions of maximum gain, Vg2 was decremented to give conversion gain and return loss as functions of second gate bias voltage. The shunt resistor on gate 1 degraded conversion gain by about 1 dB, but it improved the variation of the input impedance significantly. Figure 4 shows the conversion gain and return gain as functions of Vg2. As indicated in the figure, this circuit gave 12 dB conversion gain with -3 dBm input power, and demonstrated more than 50 dB gain control while maintaining better than 20 dB return loss.

VI. Conclusions

The usefulness of a low frequency GaAs dual-gate FET as a frequency multiplier has been demonstrated. This multiplier slightly exceeded its maximum output requirement of 8 dBm and exceeded its range requirement by almost 40 dB, demonstrating the dual gate FET's unique feature of gain control through the bias of its second gate. Furthermore, with the correct termination on the second gate, the dual-gate FET provides more gain than can be achieved from a single-gate FET of the same size.

Acknowledgements

The author wishes to thank J. P. Young for his participation in technical discussion.

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RF BIPOLAR PARAMETER EXTRACTION FOR MODELING CLASS C AMPLIFIER RESPONSE

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Today's RF circuit designer has many circuit response simulation models at his disposal to speed breadboarding, and to provide some unique analysis capabilities. Some of these models employ rigorous transistor models based to a large extent upon the Integral Charge-Control bipolar transistor model published by H. K. Gummel and H. C. Poon in 1970. [1] The G-P model basically improves upon the dc model of Ebers and Moll [2] in that it incorporates a unified approach to charge storage within the device thus enhancing its ability to predict ac performance.

Our major concern here is with the accuracy of the model parameters, as evidenced by the precision of the circuit simulation. Since parameter extraction from dc and ac measurements involves curve fitting and extrapolation from tangents, one must take care to arrive at solutions that are physically rational as well as satisfying the requirements for a good fit. We begin with those derived from dc measurements of the device.

Parameter Extraction From DC Measurements

The most informative dc measurement to be performed is what is known as the "Gummel Plot" (fig 1.) This is simply a log vs. linear plot of collector and base currents (I_C and I_B) vs. the intrinsic base-emitter forward bias voltage ($V_{B'E'}$) with V_{BC}=0. From this plot one can determine:

the transport saturation current (I_S),

ideal maximum forward beta (B_F),

the foward current emission coefficient (N_F),

the base-emitter forward bias emission coefficient (N_E),

the base-emitter forward bias leakage saturation current (I_{SE} or C_2), the forward knee current (I_{KF}).

Transport Saturation Current (I_S) is obtained by extrapolating the plot of the natural log of collector current to the y axis (V_{BE}=0). The value obtained for I_S is proportional to the area of the emitter base junction, and therefore is device type dependent.

Ideal maximum forward beta (B_F) can be determined from the maximum separation between the two curves (I_C/I_B), and varies substantially from wafer lot to wafer lot. A typical low noise transistor may have B_F from 100 to 200, while a 12.5 volt, class C power transistor will typically have a B_F of 40 to 80.

The forward emission coefficient (N_F) is extracted from the slope of the I_B locus in the mid region of the plot and models the deviation from ideal slope. N_F typically has a value of near unity.

The base-emitter low level forward bias emission coefficient (N_E or n_{EL}) is typically 2 for a shallow junction transistor, and is calculated from the slope of the I_B line near the Y axis.

$$\text{Slope} = q/(NE)KT$$

The base-emitter leakage saturation current (I_{SE} or C_2) models leakage current of the forward biased base-emitter junction. It is obtained from the Y axis intercept of the extrapolated curve for IB.

$$(\text{Y intercept}) = C_2 I_S$$

Forward knee current (I_{KF}) characterizes the onset of high injection effects and is near where the slope of the I_C curve changes to half its original value.

Similarly, a group of parameters is extracted from the Gummel Plot of the reverse transistor (i.e., exchanging collector for emitter) (fig. 2),

yielding:

maximum reverse beta (B_R),

reverse current emission coefficient (N_R),

base-collector leakage emission coefficient (N_C),

base-collector saturation current (I_{SC} or C_4),

and reverse knee current (I_{KR}).

Extracted from DC Beta plots (I_C vs V_{CE} for stepped I_B) are measurements from which the forward Early Voltage (V_{AF}), and collector resistance (R_C) can be extracted.

V_{AF} can be graphically determined (fig. 3) by extending a tangent of the I_C plot to intercept the x axis (a negative number). The foward Early Voltage is an indication of the doping level of the active base in the vicinity of the collector. As the voltage across the collector-base junction is increased, the effective base charge is reduced as the collector depletion area spreads into the base, and so forward beta increases (the Early Effect[3]). For lower frequency devices with deeper bases (f_t < 2 Ghz), V_{AF} is typically over 100 volts, but for very high frequency NPNs, and especially PNPs , the Early Voltage may be considerably less than 50 volts.

R_C can be extracted as $R_{C(sat)}$ and/or $R_{C(active)}$ by calculating the slope of the line tangent to the I_C curve in the saturation region, or through the knees of the active region, respectively (fig. 4).

The reverse Early Voltage (V_{AR}) is similarly extracted from the reverse beta plot (fig. 5). Because the reverse transistor's "collector" is the heavily doped emitter region of the forward transistor, the depletion area spreads more readily into the more lightly doped base, and V_{AR} is normally less than V_{AF}.

Parameter Extraction From Capacitance Vs. Voltage Mesurements

Capacitance parameters are obtained by employing curve fitting techniques, assuming that capacitance vs voltage follows the model:

$$C_j(V) = C_j0 / (1-V/\phi)^m + C_{(para)}$$

$C_{(para)}$, the parasitic capacitance of the package, bond pads, and die metallization must be measured and/or calculated. With the appropriate algorithm, $C_{(para)}$ can also be curve fitted. A reasonable approximation of $C_{(para)}$ would be 50% of specified capacitance at rated voltage for a typical 12 volt UHF transistor, to less than 20% for a 50 volt microwave pulsed power transistor.

Barrier potential ϕ is typically 0.5 to 0.7 volt, and the gradient factor m is expected to be .33 to .50, representing the graded junction and abrupt junction respectively. Specific conditions such as collector grading can lead to effective values of m beyond the normal range. More accurate models are needed.

Simulation programs such as SPICE [8] use ϕ and m only to calculate capacitance vs voltage, so even though the absolute numbers arrived at through curve fitting may not be in agreement with physical data, the circuit simulation results may be. The art is to set limits for parameters derived from device layout and process knowledge, and force the optimization of the curve fit (fig. 6, 7).

Parameter Extraction From AC Measurements

Forward transit time (t_F) is the sum of the emitter to collector time delays for carrier propagation through a transistor, and can be determined from the measurement of hfe over a range of frequencies and collector currents. The common emitter forward current gain is most easily derived for RF and microwave devices by first measuring the scattering parameters on a network analyzer, and then converting to the hybrid parameters. There are now a number of network analyzer systems available offering semi-automatic, and automatic, parameter extraction and calibration. Many systems offer on-line conversion from 's' parameters to other parameters including 'h' parameters. Determination of transit time from hfe then becomes a relatively simple task of plotting the inverse product of the forward current gain (hfe) and radian frequency

AIDING COMPUTER-AIDED DESIGN
Curve Fitting With Any Number of Variables

by Albert Pergande
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Introduction

A large amount of specialized design data is not available in convenient form for use with computer-aided design (CAD) systems. This data may be in tabular form, graphical form, or as a large mathematical system requiring advanced solution techniques. A polynomial or other simple function can often be used to approximate the data over some limited range of independent variables. The resulting approximations are in a convenient form and can be used in existing CAD programs or with custom CAD software.

Multivariate Curve Fitting

If given a set of (n) observed data points (Yi, i = 1 to n) and a set X of the m independent variables that generated them (X_1, X_2, ... X_m), it is convenient to approximate the Ys with some function:

$$Y = F(X_1, X_2, \ldots X_m). \tag{1}$$

The function F must be linear in its coefficients, its form must be:

$$[B_1 \times G_1 (X_1, X_2, \ldots X_m) + B_2 \times G_2 (X_1, X_2, \ldots X_m) + B_k \times G_k (X_1, X_2, \ldots K_m)] \tag{2}$$

Where each function G has no undetermined coefficients.

Equivalently:

$$\frac{dG_j}{dB_j} = 0 \tag{3}$$

and

$$\frac{dF}{dB_j} = Gj \tag{4}$$

for j from 1 to k.

With these restrictions it is possible to find the coefficient set B directly using linear algebra.

Utilizing the least squares method to find the set of B coefficients that form the best fit to the given data set, a function of the form

$$e = \sum_{i=1}^{n} [Y_i - F_i (X_1, X_2, \ldots X_m)] \tag{5}$$

needs to be minimized, where e is the sum of the squares of the errors (SSE).

By setting:

$$\frac{de}{dB_j} = 0 = \sum_{i=1}^{n} (Y_i - \frac{dF_i}{dB_j})^2 \tag{6}$$

a set of k equations in k unknowns is generated, and allows a solution for the elements of B.

Matrix Solution

There is a concise solution to the set of equations generated by Equation (6). The first step is to define the following matrices:

1. X is a matrix of n rows and k columns, where each row consists of the functions G_1, G_2, ... G_k applied to the independent variable set
2. X^t is the transpose of X
3. Y is a column vector of the dependent variables to be approximated
4. B is a column vector of the coefficients B_k that we wish to find
5. e is a column vector of the errors in the approximation at each point.

It can be shown (Reference 1) that to determine B, the matrix equation

$$[X^t X] B = X^t Y \tag{7}$$

must be solved.

frequency intercept is given by [6]:

$$RE(h_{ie})=r_{bcon}+r_{b'}+r_{bb'}+r_{e'}+w_tL_e$$

The effect of the parasitic capacitances, C_{bc} and C_{be}, and the extrinsic collector junction capacitance, C_o, is to reduce the real component of h_{ie} by an amount depending on the magnitude of h_{ie} including this capacitance, and, as h_{in} approaches the real axis, at high frequency the real part of the input impedance can be approximated by [7]:

$$RE(h_{in})=RE(h_{ie})/(1+B^2*RE(h_{ie})^2)$$

where

$$B=2\pi\geq f(C_{bc}+C_{be}+C_o)$$

Accurate determination of Rb by this method depends on a knowledge of the emitter inductance, and the parasitic package and transistor capacitances. For transistors with high ft, small values of base resistance are easily swamped by the dominant emitter inductance term.

Difficulties in measuring the 'h' parameters at high frequencies are best avoided by the more practical method of measuring the 's' parameters. The base resistance is a function of the current, and this dependence is modeled in the circuit simulator by allocating a low and high current value for the base resistance, RB and RBM, and a current at which RB falls half way to the minimum value, IRB. Input impedance circles are required over a range of bias currents to determine these values (Fig. 12).

For class 'B' and 'C' amplifier simulations, RB can be represented by the high current value without much loss of accuracy.

Application of SPICE in Class 'C' Amplifier Design

Parameters determined by the above methods can be used to simulate the operation of class 'C' amplifier circuits and gain an appreciation of the various terminal current and voltage waveforms. SPICE has been used to simulate a rf transistor operating as a class 'C' amplifier at 870MHz with 12.5 Volt collector bias, with the results compared to the performance of an actual circuit.

The 12 cell interdigitated geometry used in this comparison was packaged in a UHF flange package, with double emitter wire bonds to minimize package inductance. The SPICE parameters were extracted on a single cell die to improve accuracy. These parameters were then scaled for the larger die and the package parasitics included. Measurements were made, at an output power of 5 Watts, of the input and output impedances at the fundamental, second and third harmonics. Impedance transforming networks on input and output were modeled to accurately represent the load seen by the transistor (Fig. 13). Since the performance, especially efficiency, is strongly dependent on the collector harmonic loading, operating conditions of the test amplifier were replicated as closely as possible. In a synthesis role the packaged transistor impedances would normally be calculated from the terminal current and voltage waveforms. SPICE was able to predict the gain within 0.5dB and the efficiency within 6% of the performance of the actual circuit.

Collector voltage for the initial 100 nsec after the start of the analysis is shown in fig. 14. Because the operation of the circuit is highly non-linear and certain of the circuit time constants are relatively long, a number of cycles need to be analyzed before the response reaches a quasi-static solution. The collector voltage waveform indicates a damped oscillation exists, eventually decaying after approximately 150 nsec. The oscillation is a resonance of the collector bias choke with the collector capacitance, and illustrates the need for long analysis periods.

Five cycles have been expanded in the subsequent plots to show the collector and base voltage and current waveforms (fig. 15, 16, 17). The collector and base current waveforms are forced to be sinusoidal by the active matching networks. SPICE also provides the facility for determining the circuit performance as a function of frequency, but only for small signal conditions, and therefore is unusable when the device is initially biased off.

Although SPICE does not provide circuit optimization capabilities, when allied with network synthesis and analysis programs (i.e. SUPERCOMPACT [9] or TOUCHSTONE [10]) circuit performace can be evaluated and the design checked to ensure maximum ratings are not exceeded. The effects of changes in the device parameters can also be assessed and the influence of parasitic components can be analyzed. This

There are several ways to solve Equation (7), including methods that do not require forming the matrix inverse of X^tX. [Q-R Decomposition, (Reference 2)]. The general method of solving Equation (7) is to evaluate:

$$B = [X^t X]^{-1} X^t Y \tag{8}$$

Although not as efficient as the Q-R Decomposition, its methodology is somewhat clearer and provides results adequate for the purpose at hand.

Choice of a Basis Function

Virtually any function with the appropriate number of variables is a suitable basis function, as long as it is linear in its coefficients. The following are some examples of linear and nonlinear basis functions:

$$F = Axy^2 + Byz^3 \cos(w) + C\sqrt{X} + De^{(2x+1)} \tag{9}$$

Equation (9) is linear, with coefficients A through D to be determined.

$$F = Ax^By^Cz^D \tag{10}$$

Equation (10) is also linear; however logarithms must be used to transform it to:

$$\log(F) = \log(A) + B\log(x) + C\log(y) + D\log(z). \tag{11}$$

Finally, the equation

$$F = A\cos(Bw + C) \tag{12}$$

is nonlinear in its coefficients, as there is no transform that will separate all unknowns (A,B,C) into linearly independent functions of the variables.

The choice of basis function depends largely on what result is desired. For multivariate problems, a family of polynomials is a good choice because of its simplicity and the ability to add as many variables as needed. Polynomials are also the easiest to implement in CAD programs, and run the fastest. It should be noted that a polynomial in the form

$$(Ax^3 + Bx^2 + Cx + D)(Ey^3 + Fy^2 + Gy + H)(Jz^3 + Kz^2 + Mz + N) \tag{13}$$

must be expanded to:

$$A_1x^3y^3z^3 + A_2x^2y^3z^3 \ldots A_{64} \tag{14}$$

to make the coefficient set linear. Also note that what initially appears to be a system with 12 unknowns actually requires solving for 64 coefficients. Given the 64 coefficients, it may be possible to separate them and solve for the set (A,B, ...N) but this is a difficult task and the coefficients are generally complex.

The degree of the individual polynomials should be chosen with some discretion. As the individual number of terms grow, the number of coefficients to be determined grows alarmingly. A large number of coefficients makes the matrix X^tX large, and many data points are required to prevent it from becoming singular. If the system is not heavily overdetermined (i.e., $n \gg m$) the fit will be "wavey" (Figure 1). In Figure 1, a 1st, 4th and 8th degree polynomial approximate a set of points. As the order of the polynomial increases, the error of the approximation decreases until the SSE is 0. Although this fit is technically correct, as it hits all the points, it clearly fails to provide a good interpolation to the data set.

The last basis set to consider is the function:

$$f = A0 + A1\sin(w) + A2\sin(2w) \ldots + Ap\sin(pw) + B1\cos(w) + B2\cos(2w) \ldots + Bq\cos(qw) \tag{15}$$

where both p and q do not both = 0.

When this series is truncated to some finite number of terms, the result is an approximation to a Fourier transform. The data must be transformed using equation (16) to the interval (-pi,pi) or (0,2pi). While this is not the most efficient method of calculating a Fourier transform, it does allow the freedom to make A, and B polynomial functions. The Fourier transform of some data set may then be calculated as a function of another variable, allowing one to optimize a particular coefficient.

Scaling

As higher degree functions are used to fit a particular data set, the individual terms in the X matrix become larger. When they differ by several orders of magnitude, the potential for numerical error increases, and inversion of X^tX becomes a larger problem. To counter this, all of the dependent and independent variables should be mapped onto the range (-1,1) using a linear transform (Equation (9)). After the regression is performed, the inverse transform can be applied to map the function back to its original range. All terms of X and Y will then lie between $\pm$ 1:

$$V1 = \frac{2}{(Vmax - Vmin)} \times V + \frac{(Vmin + Vmax)}{(Vmin - Vmax)} \tag{16}$$

is demonstrated by the influence on gain and collector efficiency of variation in emitter inductance shown in fig. 18.

Conclusions

While linear models for RF circuit response have been in use for some time, models based upon intrinsic transistor parameters have only recently found utility in predicting RF power amplifier response Extraction of these parameters from I-V, C-V and AC measurements is still, however, something of an art Utilizing these models to characterize the AC response of a class C amplifier gives insight into device design and process optimization, as well as circuit performance considerations.

To demonstrate this approach to computer aided design, a 12.5 Volt, 870 MHz, 5 Watt amplifier has been modeled, and the results discussed, especially model parameter extraction.

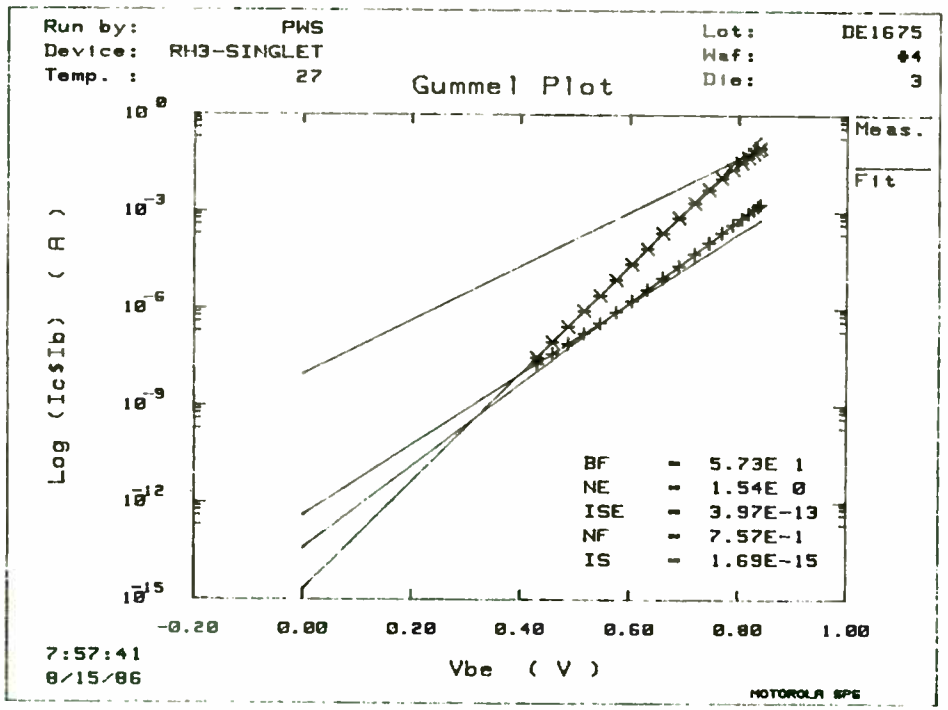

Fig. 1. Gummel Plot

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9. SUPERCOMPACT, a software product of **Compact Software,** Palo Alto, Ca. (703-698-0215)
10. TOUCHSTONE, a software product of **EEsof**, Westlake Village, Ca. (818-991-7530)

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When scaled in this manner, the coefficients of the regression follow a set pattern. That is, the coefficient that makes the smallest contribution to the approximation has the smallest absolute magnitude. If the exact number of basis functions for optimum fit isn't known, one can begin with a large number of them, and repeatedly perform the regression, dropping the least important function until either the accuracy begins to erode or the desired number of functions remains.

Quality of the Fit

After approximating a set of data with some function, a natural question is "How good a fit is it?". In other words, does the derived function accurately model the data, or is a more or less elaborate model needed? A common way to answer this question is to consider the multiple regression coefficient, or R^2. R^2 is defined as:

$$R^2 = \frac{\sum_{i=1}^{n} (\hat{Y}_i - \bar{Y})}{\sum_{i=1}^{n} (Y_i - \bar{Y})} \qquad (17)$$

Where $\bar{Y}$ is the average value of y
$\hat{Y}$ is the predicted value of y
Y is the data set
i is taken over the range 1 to n.

R^2 varies from 0 to 1. A value of 0 indicates that the fitted function approximates the data no better than $\hat{Y} = \bar{Y}$. A value of 1 means that the approximation has matched all the points exactly. This should be viewed with some skepticism, as R^2 can be made to equal exactly 1 by choosing as many coefficients as there are data points. (Again, see Figure 1 and its "wavey" fit.)

Limitations of Curve Fitting

Although curve fitting is a very powerful tool in many branches of science and engineering, its results must be taken with a grain of salt. The resulting equations must be viewed for what they are - an approximation over a limited range to a physical phenomenon. When using fitted curves, one must be careful to limit them to the range of data from which they were derived. They can be used for interpolation, but not for extrapolation. Outside of the intended range, the equations might do anything, and it certainly has no particular relationship to what the modeled system would do. And, if the system is not over determined to a sufficient degree, a "wavey" function may well result. Always plot your results to perform a visual inspection.

Example 1 - Suspended Stripline

A function for a frequency dependent suspended stripline transmission line is generated (Figure 2). The three parameters to be considered are strip width, dielectric constant of the substrate, and operating frequency. We will predict wave impedance (Zo) and effective dielectric constant (keff). The data will be scaled to the interval (-1,1). Variables mapped to this region are primed. Initial values were determined from a standard paper on suspended stripline (Reference 3) using the program SuperCompact. The time needed to calculate the 125 values for the regression took well over an hour on SuperCompact, which was running on the Apollo Domain System. The resulting polynomials run considerably quicker.

The curve is valid over the following range of input parameters with the corresponding transfer functions:

$$Freq' = (0.05714 \times Frequency) - 1 \text{ [GHz, from 0 to 35 GHz]} \qquad (18)$$

$$Width' = (0.04082 \times Strip\ Width) - 1.04082 \text{ [mils, from 1 to 50 mils]} \qquad (19)$$

$$Er' = Er - 3.2 \text{ [unitless from 2.2 to 4.2]} \qquad (20)$$

$$Zo = (Zo' + 1.41473)/0.01686 \text{ [in Ohms]} \qquad (21)$$

$$Keff = \frac{(Keff + 2.87945)}{1.09589} \text{[unitless]} \qquad (22)$$

Additional parameters describing the stripline are:

$\frac{B_1}{h} = 3$, $\frac{B_2}{h} = 3$, $\frac{a}{h} = 10$ and the metal has zero thickness and is a perfect conductor.

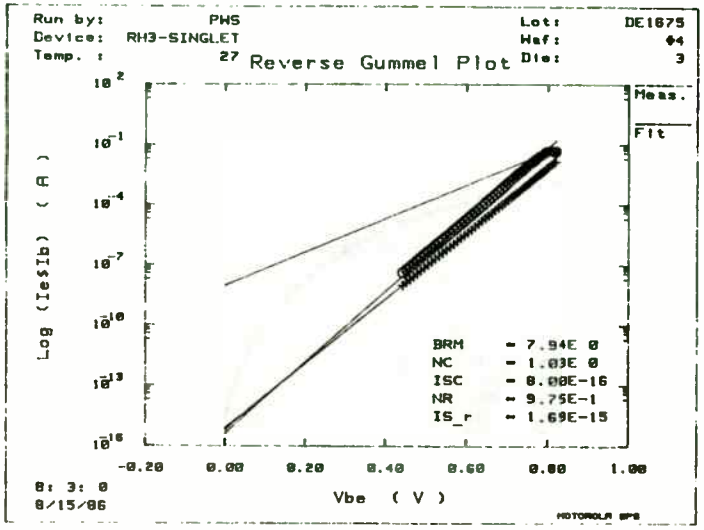

Fig. 2. Reverse Gummel Plot.

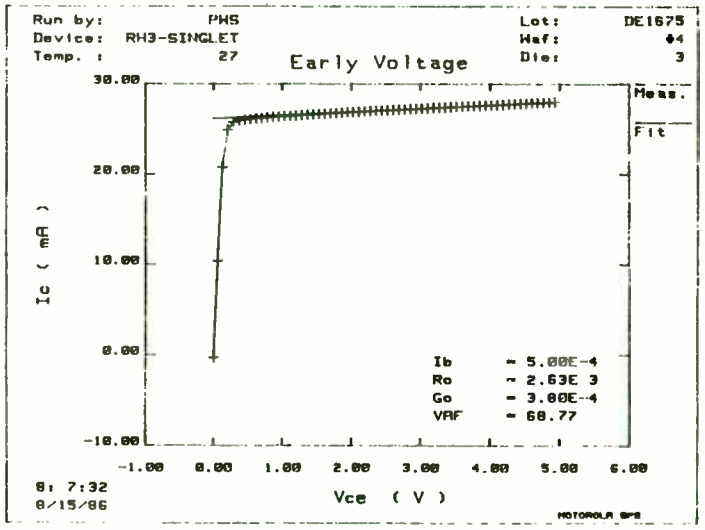

Fig. 3. Forward Early Voltage

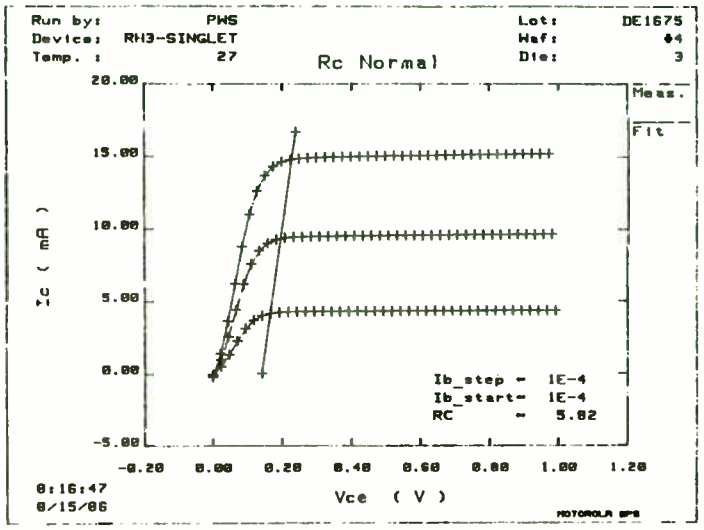

Fig. 4. Collector Resistance (RCactive).

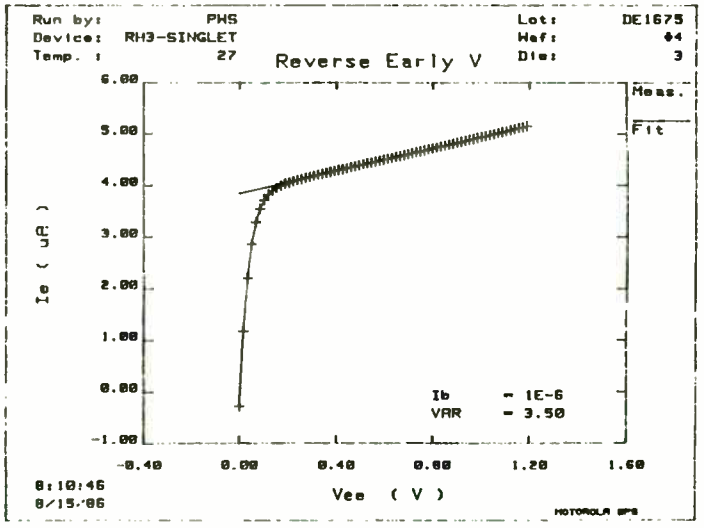

Fig. 5. Reverse Early Voltage.

The resulting functions are good over these ranges to within 2.67% for Zo and 4.5% for Keff.

(23)

$$Zo' = -0.6385352098 - 0.1067620906\ Er' + 3.481023304E\text{-}03\ Freq' + 2.435179168E\text{-}03\ Er' \times Freq' - 0.5161190977\ Width' + 6.722957429E\text{-}02\ Width' \times Er' - 2.867867028E\text{-}04\ Freq' \times Er' \times Width' + 0.5297363704\ Width'^2 - 6.539253142E\text{-}02\ Er' \times Width'^2 - 8.288004956E\text{-}04\ Er' \times Freq' \times Width'^2 - 0.3191094332\ Er' \times Width'^3 + 3.948039494E\text{-}02\ Freq' \times Width'^3$$

(24)

$$Keff' = -0.1607894999 + 0.7549461296\ Er' + 0.0814640615\ Freq' + 0.0572409262\ Er' \times Freq' + 0.2464396608\ Width' + 0.1040612513\ Width' \times Er' + 0.0454664369\ Width' \times Freq' + 0.0421388077\ Width'^2 - 0.1771355508\ Er' \times Width'^3 - 0.0459836924\ Freq' \times Width'^3$$

Waveguide E-Plane Septum Filter

A popular way of building waveguide filters is to place an array of rectangular strips of metal (called septa) in the E-plane of the waveguide. These septa may be etched, allowing easily repeatable filters to be built at a very low cost (Reference 4). To build such a filter, the septum is modeled as a Tee of inductors (Figure 3). The values Xs and Xp are a complex function of the septum, waveguide dimensions, and frequency (Reference 5). Owing to the dispersive nature of waveguide, Xp and Xs can be modeled as physical inductors over only a narrow bandwidth. Plots of Xs and Xp as a function of W with frequency as a parameter are available as small plots in the published literature. Approximate solutions for Xp and Xs as functions of physical dimensions may be had by solving a complex set of equations using the variational method (Reference 5). Since graphical data is available in the region of interest (i.e., WR-28), the simplest way to determine Xs and Xp is to fit a curve to the graphical data and use the resulting equations to design the filter. Initial values for the filter are generated from classical filter design methods (Reference 6).

The first step is to enlarge the graphical data so that values may accurately be read from it. An enlarging photo-copier works well, but it is also possible to use an overhead projector, a microscope with digital positioning, or whatever is most easily accessible. This data is operated on by Equation 8, yielding regression coefficients for the data set, along with the R^2 value and the SSE value. These coefficients are listed in Equations 29 and 30. Over the range 28 to 38 GHz and septum widths form 1 to 200 mil, the error is less than 2.6 and 2.5% for these equations:

$$W' = (0.01111 \times Width) - 1.22222 \quad (25)$$

$$F' = (0.16667 \times Frequency) - 5.33333 \quad (26)$$

$$Xp' = (2.41525 \times Xp) - 1.00977 \quad (27)$$

$$Xs' = (3.41329 \times Xs) - 1.25031 \quad (28)$$

(29)

$$Xp' = -0.7348365815 - 0.4007322178\ W' + 0.2520677187\ W'^2 - 0.2189697101\ W'^3 + 0.1627606451\ W'^4 + 0.2697266795\ F' - 0.2522981693\ F' \times W' + 0.8263478164E\text{-}01\ F' \times W'^2 + 0.7993333394E\text{-}01\ F'^2 - 0.4333514566E\text{-}01\ F'^2 \times W'^2 - 0.8596676895E\text{-}01\ F'^3 \times W'^2 + 0.9651804516E\text{-}01\ F'^3 \times W'^4$$

(30)

$$Xs' = 0.4674951695\ W' - 0.2667132517\ W'^2 + 0.1441766713\ W'^3 + 0.5238057254\ F' + 0.2172888051\ F' \times W' - 0.1135707485\ F' \times W'^2 + 0.5170873288E\text{-}01\ F' \times W'^3 - 0.2741439220E\text{-}01\ F'^2 \times W' + 0.7424136480E\text{-}01\ F'^2 \times W'^2 - .8060922104E\text{-}01\ F'^2 \times W'^4$$

With a simple set of expressions for the reactance values, the filter design procedes along well worn paths (Reference 6). A 1 GHz bandwidth 3 dB ripple Chebychev filter was designed with a 35 GHz center frequency (Figure 4).

Conclusion

A method to fit a set of data to a group of basis functions in any number of variables has been described, along with criteria for judging the quality of the fit and the appropriateness of the basis functions used. Several design examples were used to show the application of curve fitting to typical microwave engineering problems. The limitations of curve fitting were discussed.

I would like to thank Joe Chenkin for the valuable help he has provided, particularly for the design of the filter.

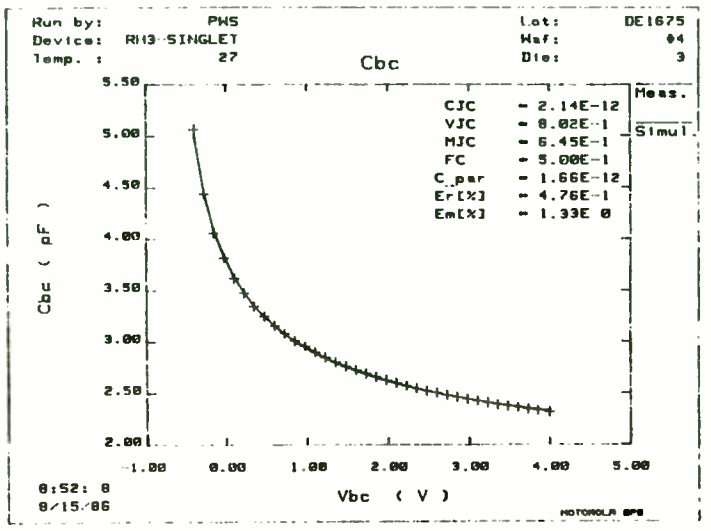

Fig. 6. Collector-Base Junction Capacitance

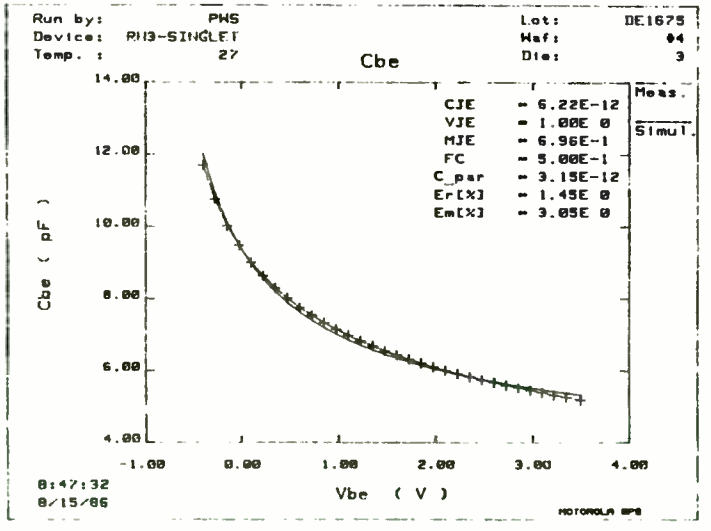

Fig. 7. Emitter-Base Junction Capacitance.

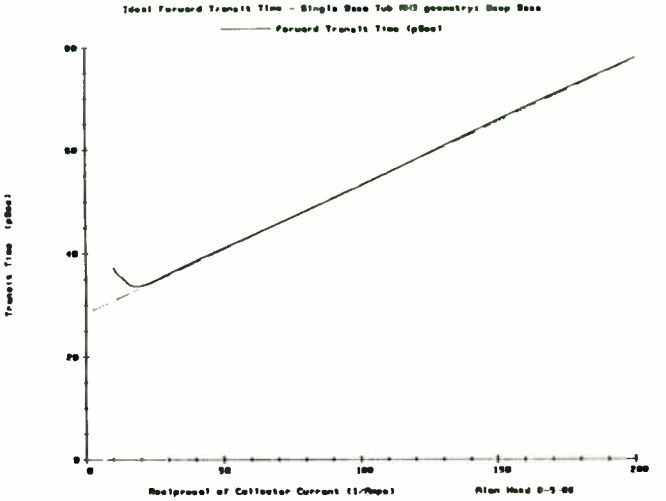

Fig. 8. Forward Transit Time Extraction.

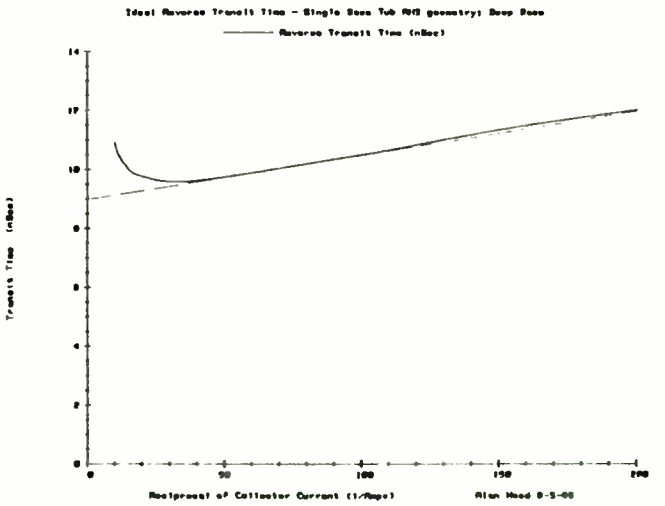

Fig. 9. Reverse Transit Time Extraction.

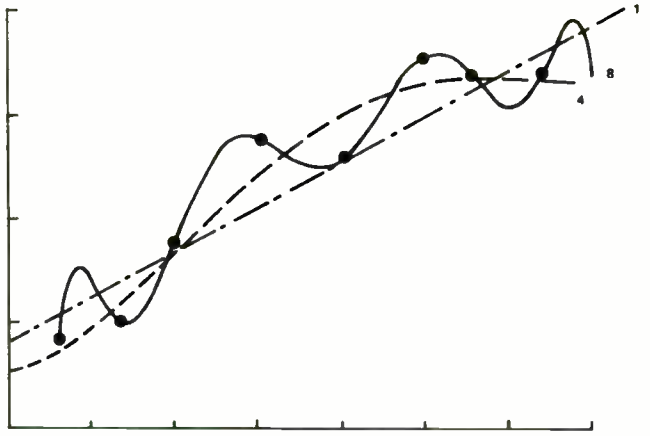

Figure 1. Increasing the degree of approximation improves the accuracy of the fit on a point by point basis, at the expense of a "wavey" fit.

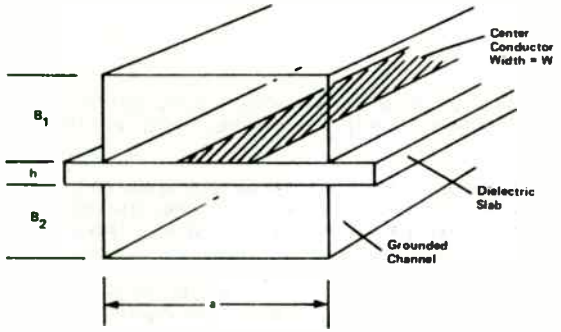

Figure 2. The 3 parameters to be considered in this suspended stripline are strip width, dielectric constant of the substrate and operation frequency.

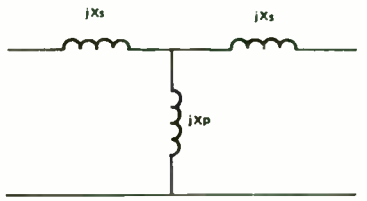

Figure 3. The e-plane waveguide septum filter was built by placing rectangular strips of metal (septa) in the e-plane of the waveguide.

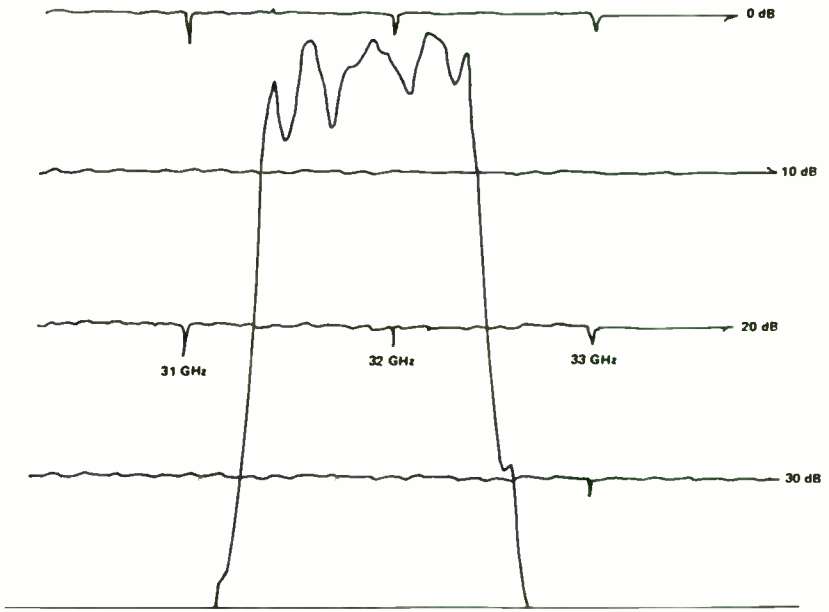

Figure 4. A 1 GHz bandwidth 3 dB ripple Chebychev filter, designed with a 35 GHz center frequency will produce the above response curves.

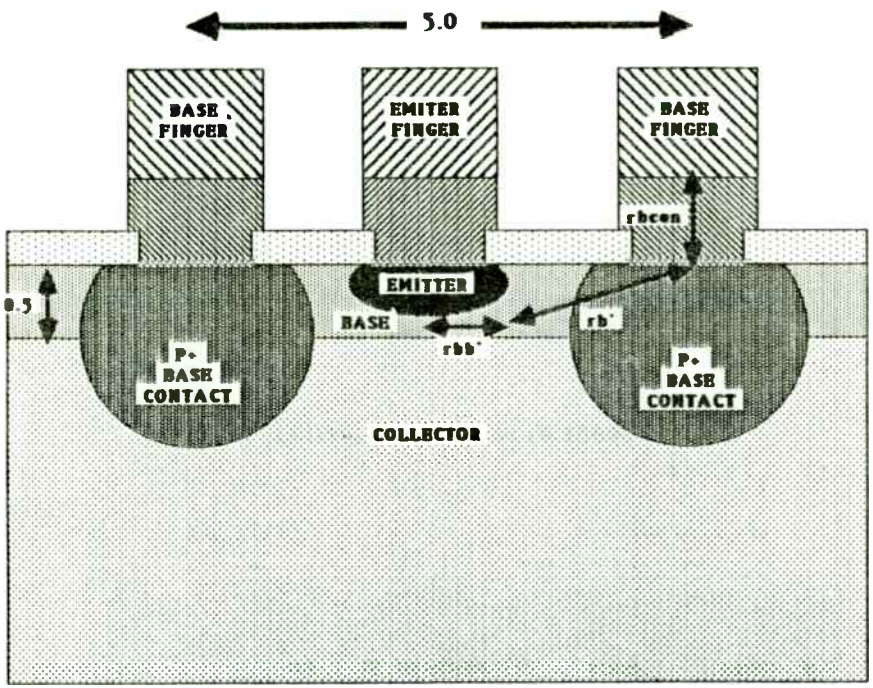

Fig. 10. Note that rbb' is the primary current dependent component of Rb.

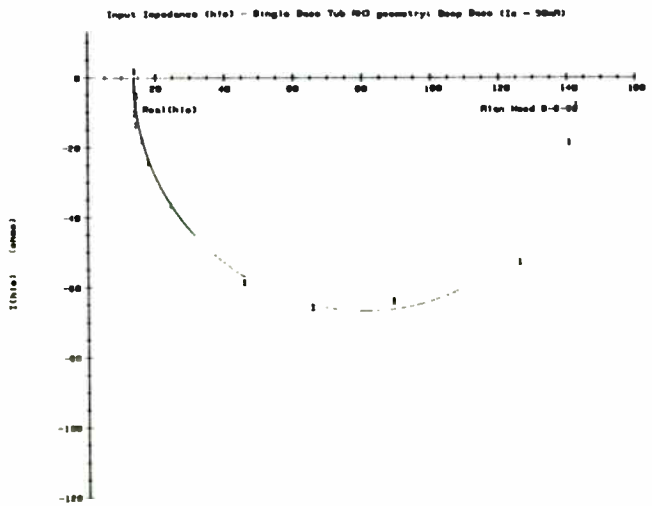

Fig. 11. Base Resistance Extraction From Impedance Circles

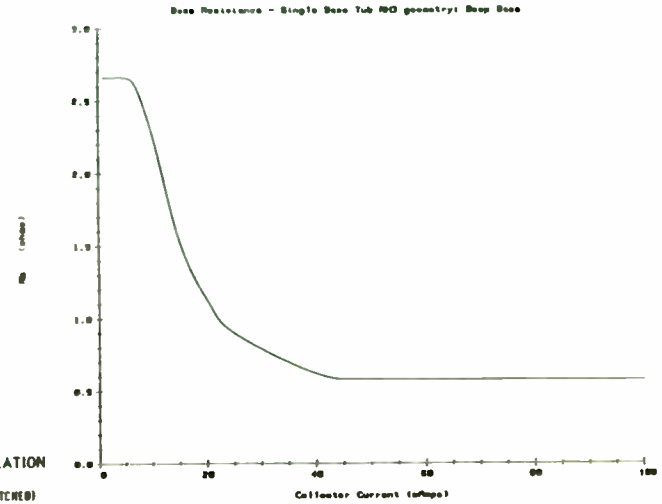

Fig. 12. Plot of Rb vs. Current.

DATA FILE FOR CIRCUIT SIMULATION

```
SIMPLE CLASS 'C' AMPLIFIER (12 CELL AR3 UNMATCHED)
VCC 9 0 12.5
RS 1 2 50
CB1 2 3 1000PF
LBC1 4 0 60NH
CSHUNT1 3 0 0.320PF
CSHUNT2 4 0 56.12PF
LBIN1 3 4 2.41NH
LB  4 55 0.78NH
CEPARS 5 7 17.46PF
VIDM 55 5
LC  10 0 0.50NH
CCPARS 6 7 9.54PF
LE  7 0 0.50NH
VICM 10 6
LCC 8 9 50NH
LSER1 8 10 2.039NH
CCSHUNT 10 15 2.097PF
LCSHUNT 15 0 0.9046NH
LSER2 10 11 2.0592NH
RLOAD 14 0  50
TRL2 11 0 12 0 Z0=10.05 F=870MEG NL=0.0739
CSER1 12 13 43PF
LCSER2 13 14 0.77NH
VIN 1 0 SINE(0 10 870MEG)
Q1 6 5 7 MOD1
.MODEL MOD1 NPN (BF=66.2 VAF=10 IS=0.758E-14 NF=0.929 NR=0.999
+          RB =0.225 IRB =0.056 IRB = 0.1680
+          CJE=56.6PF MJE=0.767 VJE=1.2
+          CJC=13.90PF MJC=0.573 VJC=0.861
+          RE=0.12 RC=0.902 IKF=20  VAR=7.29 IKR=400MA VAR=3.48
+          TF=0.020NS XTF=6  ITF = 3.5A VTF = -24  TR = 9.00NS  ) .
.TRAN 0.05NS 165NS 160NS
.VSTEP IN=00 OUT = 00
.OPTIONS LIMPTS=2500 ITL5=50000
.FOUR 870MEG V(6)
.FOUR 870MEG V(14)
.PLOT TRAN V(2) V(5) V(6) I(VICM) V(14) I(VIDM) I(VCC)
.END
```

Fig. 13. SPICE File

References for Polynomial Fitting Paper

1 Draper and Smith, "Applied Regression Analysis," John Wiley & Sons, New York, 1967, pages 58-59.

2 Dongrarra, Moler, Bunch, and Stewart, "Linpak User's Guide," Chapter 9, Siam, Philadelphia, PA, 1979.

3 Yamashita and Atsuki, "Stripline with Retangular Outer Conductor and Three Dielectric Layers," Institute of Electrical and Electronic Engineers, Volume 18, #5, May 1970, pages 238-244.

4 Yi-Chi Shi, Tatsuo Itoh, and L.Q. Bui," Computer Aided Design of Millimeter Wave E-plane Filters, "Institute of Electrical and Electronic Engineers, Volume 31, #2, February 1983, pages 139-141.

5 Kunisi and Venakada, "The Design of a Bandpass Filter with Inductive Strip - Planar Circuit Mounted in Waveguide," Institute of Electrical and Electronic Engineers, Volume 22, #10, October 1974, pages 869-873.

6 Matthaei, Young, and Jones, "Microwave Filters, Impedance Matching Networks, and Coupling Structures," Aratech House, Dedham, MA, pages 427-440.

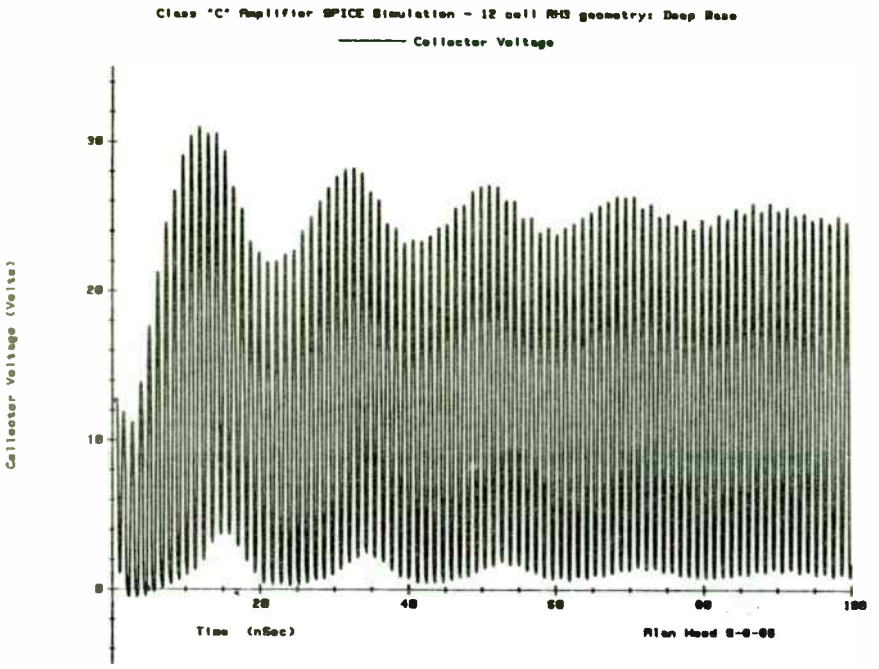

Fig. 14. Collector Waveform To 100ns

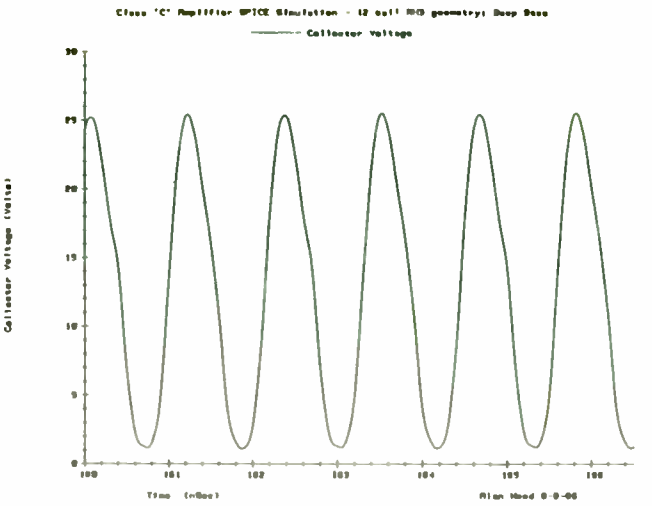

Fig. 15. Collector Waveform 160-166ns

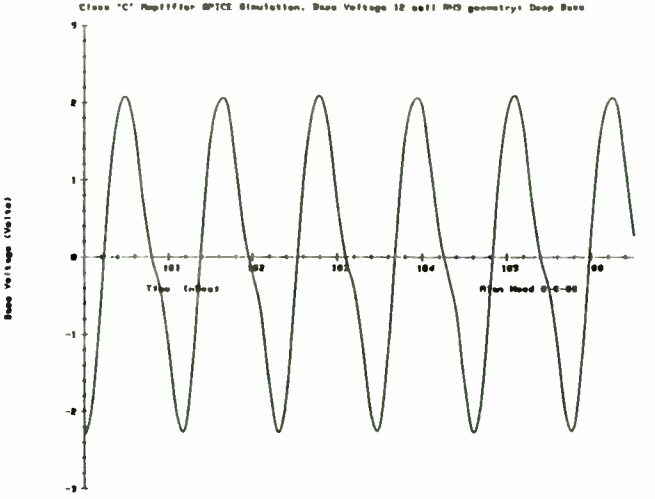

Fig. 16. Base Waveform 160-166ns

OSCILLATOR DESIGN USING THE DEVICE LINE METHOD AND LOAD PULL METHOD

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Hewlett-Packard
San Jose, Ca.

INTRODUCTION

The purpose of this paper is to examine two methods of oscillator design. The general requirements for designing an oscillator using the concept of the negative resistance one port will be covered, along with how the device line and load pull methods are used to determine the load impedance necessary for maximum oscillator output power.

NEGATIVE RESISTANCE ONE PORT

The design examples in this paper use the concept of transforming a three port bipolar transistor into a negative resistance one port. Before proceeding with a design example, the concept of the negative resistance one port needs to be examined. Figure 1 shows a negative resistance one port connected to a load which has both a reactive and resistive component. This network combination will start oscillating if the magnitude of the small signal resistance ($|R_D|$) is greater than the load resistance R_L, and at a frequency where the reactive components X_D and X_L are equal but of opposite sign. The steady state oscillation condition requires that $|R_D| = R_L$, which implies that the S-parameters of the one port decrease with increasing power. Computer programs can be used to design the one port and the output matching circuit required for oscillation, if the large signal impedances of the one port are known. The device line and load pull method provide a means of measuring the large signal impedances of the one port.

DEVICE LINE METHOD

As was pointed out above, one problem when designing an oscillator is not knowing what load impedance should be placed on the one-port to deliver the required output power and frequency. One solution to this problem is to measure the one-port impedance as a function of output power. The impedances can be measured by first designing the one-port not to oscillate when loaded by a 50 ohm generator. A network analyzer is used to measure the impedances as the one-port is driven by increasing input power. Since the one-port is a negative resistance device, the reflected power is greater than the input power. The added power is the reflected power minus the input power and will reach a maximum.

The above procedure has generated the device line for the one-port[1]. All of this may seem very complicated, but is really nothing more than the measurement of large signal S-parameters for an amplifier. In this case the amplifier is a one-port device and the test is limited to the measurement of S_{11}.
The design procedure may be summarized as follows:

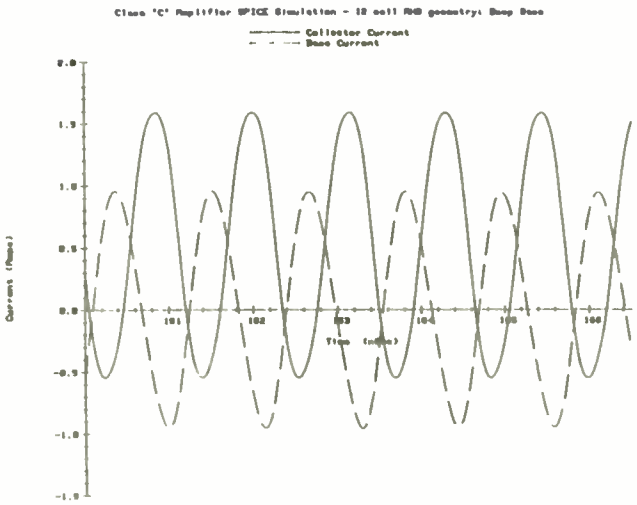

Fig. 17. Collector and Base Waveforms 160-166ns

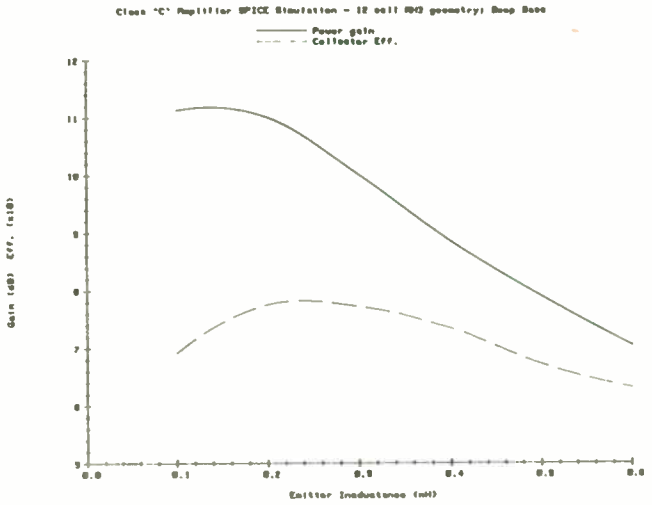

Fig. 18. Amplifier Gain and Efficiency vs. Emitter Inductance

1. Choose a transistor circuit topology that will induce a negative resistance on the terminal used as the output port. This circuit configuration will be determined in part by the transistor package used, and how the device will be biased.

2. Maximize the reflection coefficient of the one port using the transistor's small signal S-parameters. Figure 2 shows that when the one port reflection coefficent is infinity, the one port impedance is equal in magnitude to the load impedance, but with opposite sign.

3. If the circuit of step 2 does not oscillate into 50 ohms, then use the device line method to measure the load impedance for maximum output power.

4. If the circuit of step 2 does oscillate into 50 ohms, then use the load pull method to measure the load impedance for maximum output power[2]. Details of the load pull method will be covered later in this paper.

5. Design an output matching network using the measured load impedance.

6. Build a complete oscillator by combining the circuits of steps 2 and 5.

An example will help clarify the above procedure and how the negative resistance port is designed.

FIRST EXAMPLE

The first example uses an HXTR-4101 common base bipolar transistor. The goal is to design an oscillator at 4.3 GHz that will deliver the maximum output power from the transistor (about + 20 dBm)[3]. The objective is to place the transistor in some type of circuit topology that will produce a negative resistance on its output port. Using the transistor's small signal S-parameters and with the help of a computer analysis program, several different circuit topologies were examined for the ability of inducing a negative resistance. Figure 3 shows the circuit topology finally selected. This circuit must have a large signal negative resistance magnitude less than 50 ohms so it will not oscillate when loaded by the test equipment. Remember that our purpose thus far is to design and build a non-oscillating circuit from which we can measure its negative resistance as a function of output power.

A COMPACT[4] computer program was written to maximize S_{22}' by varying transmission line lengths L_1 and L_2 (Figure 3). The minus sign in line 14 instructs the optimization program to maximize the reflection coefficient. Optimizing the circuit for maximum S_{22}' also sets the negative resistance magnitude to be equal to the load resistance (refer back to Figure 2). It was convenient to design for a negative resistance of 50 ohms. The first line of the COMPACT program specifies the open stub on the emitter with an estimated line length of 2.54 mm (0.100 inch) to be optimized. The shorted stub on the base (Figure 3) is actually composed of two parallel shorted stubs which are specified in

lines three and four. After maximizing for S_{22}', the emitter stub length was increased to 2.96mm (0.117 inch) and the base stubs to 7.86mm (0.310 inch). The circuit was constructed on 0.031 inch thick Duroid™ 5880, and is shown in Figure 4. We will come back to the circuit shortly, but for now continue with another example.

SECOND EXAMPLE

In this second example the objective is to design a medium power (1 watt) oscillator at 2.0 GHz. For this design an HXTR-4103 common collector bipolar transistor will be used[5]. This transistor is housed in a flange mounted package, the HPAC-200GB/GT. Once again a circuit topology is selected (Figure 5) and the circuit element optimized to maximize S_{22}' using the transistor's small signal S-parameters. The impedance of the open transmission line was arbitrarily picked to be 50 ohms and only the length of the transmission line optimized. This circuit was also constructed on 0.031 inch thick Rogers RT/Duroid™ 5880 and is shown in Figure 6.

DEVICE LINE METHOD

The 4.3 GHz circuit using the HXTR-4101 transistor did not oscillate into 50 ohms ; therefore, the device line method was used to measure the load impedance for oscillation. The test set-up is shown in Figure 7. Since the resistance is negative the reflection coefficient exceeds unity and the impedance lies outside the normal Smith Chart. Displaying a reflection coefficient greater than one is possible by interchanging the test and reference ports on the HP 8411A harmonic frequency converter. This inverts the reflection coefficient so that the analyzer shows the circuit impedance with the sign changed. This is exactly the impedance that must be connected to the circuit to complete the oscillator. Figure 8 shows the admittance load line measured for the circuit. The admittance of 0.26 + j0.32 corresponds with the maximum added power of the circuit which is the output power expected when the oscillator is completed.

4.3 GHz OUTPUT MATCHING NETWORK

The output matching network must transform the 50 ohm load to a normalized admittance of 0.26 +j 0.32 at point A (Figure 9). First an open shunt line is added to move the 50 ohm load to point B. A 50 ohm transmission line then rotates the admittance at point B to point A. The final 4.3 GHz oscillator circuit is shown in Figure 10. The measured output power of the oscillator agreed very well with the predicted P_{max} of 19.6 dBm (Figure 11). Figure 12 shows the phase noise for the final oscillator. This completes the design and testing of the 4.3 GHz oscillator. Now we will return to the 2 GHz oscillator.

LOAD PULL METHOD

The 2 GHz circuit using the HXTR-4103, did oscillate into 50 ohms, which prevents the use of the device line method. Re-optimizing the circuit with a load resistance lower than 50 ohms may result in a circuit that will not oscillate, but the

HOW TO SPECIFY PIN DIODE SWITCHES

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I INTRODUCTION

When purchasing PIN diode swithces, it is important that they are completely specified to assure system performance. It is also important that the specification be achievable. This paper is designed to help a systems designer specify realizeable PIN diode switches.

There are six key parameters essential to specify pin diode switches. These are:

1) TYPE i.e., SPST, SPDT, SP3T, DPDT, etc.
2) OPERATING FREQUENCY BAND
3) INSERTION LOSS
4) ISOLATION
5) SWITCHING SPEED
6) POWER HANDLING

There are five secondary parameters that may require specification. These are:

1) LOGIC COMPATIBLE DRIVER TYPE AND SPEED.
2) PHASE TRACKING ARM TO ARM AND/OR UNIT TO UNIT.
3) OFF ARM TERMINATIONS.
4) INTERCEPT POINT OR COMPRESSION POINT
5) VIDEO TRANSIENTS

II SWITCH TYPE

Most PIN diode switches are of the single pole multiple throw type. They range from single throw up through 8-12 throws. The most popular type is the SPST or pulse modulator type. In general the greater the number of throws, the less popular the switch and, hence the less readily available it is. American Microwave has standard switch designs up through 5 throws in the three popular bands of interest HF, UHF/VHF, and Microwave. We also have designs for 8 and 10 throws at HF and Microwave.

The most popular multi-pole switch is the DPDT type, commonly known as the TRANSFER SWITCH. These units are available in UHF/VHF and Microwave bands. High order multi-pole switches are generally referred to as switch matrices, which is a whole subject matter by itself.

III OPERATING FREQUENCY BANDS

American Microwave classifies PIN switches into five operating frequency bands. They are:

a) VIDEO which covers from 10KHZ to 2MHZ, not manufactured at AMC.
b) HF which covers 2MHZ to 32MHZ, AMC series SW-0230 switches.
c) UHF/VHF covering 10MHZ to 2000MHZ, AMC series SW-2000 switches.
d) MICROWAVE covering 10MHZ to 20GHZ and above, AMC series SW-218 switches.
e) Milimeter wave switches, 20GHZ and up.

The above bands have loosely defined boundaries which overlap. They are indicative of the five different technologies available to the switch

decision was made to use the load pull method to measure the load resistance necessary for maximum oscillator output power. Figure 13 shows the test set-up for the load pull measurement system. The output of the oscillator is connected to a sliding tuner and 50 ohm load combination. The output power of the oscillator, and the load impedance presented to the oscillator is measured as the tuner is varied. The spectrum analyzer is used to verify that the output spectrum of the oscillator is a stable single frequency before an impedance measurement is made. Figure 14 shows the optimum load impedance measured for the 2.0 GHz circuit (115 + j 70 ohms). The output network for the 2.0 GHz circuit was then designed.

2.0 GHz OUTPUT MATCHING NETWORK

The load impedance for maximum output power at 2.0 GHz is first normalized to 70 ohms and plotted as an admittance at point A (Figure 15). The output matching network must transform the 50 ohm load to a normalized admittance of .444 - j0.270 at point A. First an open shunt line is added to move the 50 ohm load to point C. A 70 ohm transmission line of 0.201 wavelength then rotates the admittance at point C to point B. The design is completed by adding another open shunt line to move the admittance at point B to point A. The PC board artwork layout forthe final oscillator is shown in Figure 16. The output power of the oscillator is typically + 30 dBm. The phase noise of the oscillator is shown in Figure 17 . This completes the design of the 2.0 GHz oscillator.

SUMMARY

The two examples given in this paper have shown that the device line and load pull methods are useful tools for the designer. The methods help bring a systematic approach to the design of oscillators in an area where empirical methods abound.

REFERENCES

1. Walter Wagner, "Oscillator Design by Device Line Measurement", Microwave Journal February 1979 pp. 43-48.

2. Dennis Poulin, "Load-Pull Measurements Help Meet Your Match", Microwaves November 1980 pp. 61-65.

3. Hewlett-Packard Application Note 975, " A 4.3 GHz Oscillator Using the HXTR-4101 Bipolar Transistor."

4. Compact Software

5. Hewlett-Packard Application Note 994, " A 2 GHz Power Oscillator Using the HXTR-4103 Bipolar Transistor."

manufacturer as well as four distinct applications areas of switch requirements.

There are some special application bands and technologies such as the high speed, low transient IF switching technology which is reflected in the SWB-0070 series of switches in the AMC catalog.

IV THE PIN DIODE

A simplified equivalent circuit of the PIN diode is shown in figure 1. The forward biased diode is a current controlled resistor. The resistance vs current behavior of a typical PIN diode is shown in figure 2. The reversed biased diode is a voltage controlled capacitor. The capacitance vs voltage of a typical PIN diode is shown in figure 3.

V INSERTION LOSS

Simple, most basic switches have the lowest loss for any given operating band. For a given technology or operating band, insertion loss increases with increasing frequency proportional the square root of frequency in a well designed PIN switch. Insertion loss originates in four basic areas.

a) Conductor or transmission line loss within switch itself due to the presence of microstrip, coaxial line or waveguide interconnecting lines.

b) Resistance losses due to finite resistance of series connected components such as PIN diodes and/or finite "Q" capacitors.

c) VSWR losses due to mismatch of components within the switch or at the terminals of the switch. VSWR losses at the terminals of the switch can be tuned out externally to improve losses, those within the switch must be minimized in design. These actually are the cause for ripples in the insertion loss vs frequency characteristic.

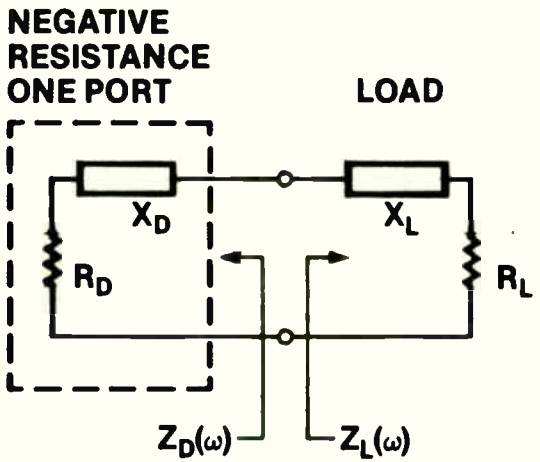
Assuming a switch is well designed, i.e., lowest loss transmission media, lowest resistance diodes and other series components are employed and all internal VSWR's are minimized, the loss of the switch is then dependent on the complexity of the design. In general, multi-throw units are more lossy as the number of throws increases. The addition of off-arm terminations and video filters increases the loss of the switch for a given technology. Also increased on/off isolation will contribute slightly to the loss. The insertion loss is lowest in the least complex switch configurations. For low loss switches, keep the specification simple.

VI ISOLATION

PIN diodes are connected to the transmission line in series or in shunt. Isolation is achieved by reverse biasing series connected diodes or forward biasing shunt connected diodes. The shunt mounted diode provides the most effective means for achieving broadband, relatively frequency independent isolation. It is ideally frequency independent but practically, small parasitic reactances generally affect broadband performance. Isolation is also acheived by reverse biasing series mounted diodes. Isolation for the series mounted diode decreases with increasing frequency.

Series-shunt diode configurations are frequently employed in multithrow broadband switches to achieve relatively high isolation in a simple structure. An example of the performance of a series-shunt connection is shown in figure 4 for the AMC model SW-218-2 switch. Note how the isolation decreases with increasing frequency. Multiple diodes connected in series or in shunt are frequently employed in PIN switches to achieve relatively high isolation over

FIGURE 1



- **START-UP CONDITION**

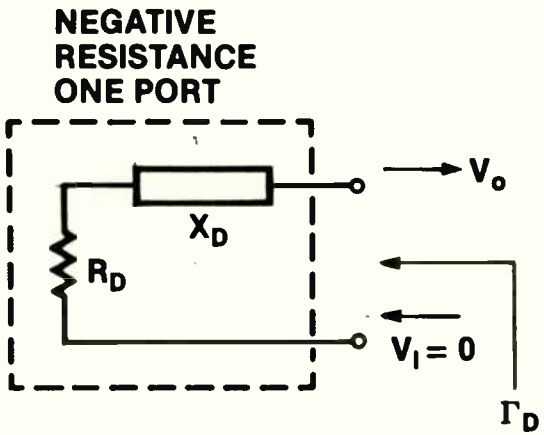
$$|R_D(\omega_o)| > R_L$$

$$\text{AND } -X_D = X_L$$

- **STEADY STATE CONDITION**

$$|R_D(\omega_o)| = R_L$$

FIGURE 2



- $\Gamma_D = \dfrac{V_o}{V_i} = \dfrac{V_o}{o} = \infty$

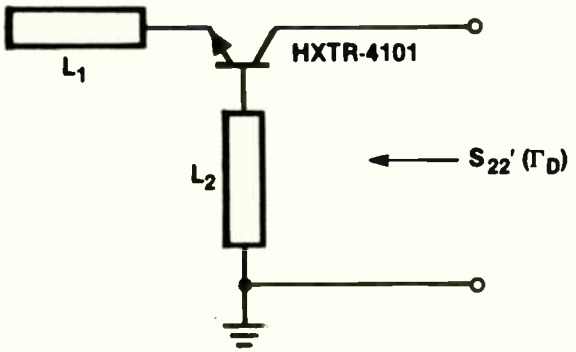
- SINCE $\Gamma_D = \dfrac{Z_L - Z_D}{Z_L + Z_D}$

- THEN $Z_L = -Z_D$

FIGURE 3

EXAMPLE NO. 1

COMMON BASE BIPOLAR



COMPACT PROGRAM TO MAXIMIZE S_{22}'

```
OST   AA   PA   50   -100   1.9   0   0
TWO   BB   B1   50
SST   CC   PA   50   -300   1.9   0   0
CAS   CC   CC
SER   BB   CC
CAS   AA   BB
PRI   AA   OR   50   1E9
END
4300
END
1.02   104   1.88   -142   .142   78   1.14   -109
END
.001
-100   0   0   0
END
Optimization begins with following variables and gradients
        VARIABLES                GRADIENTS
    ( 1):  100.000           ( 1): -28.5006
    ( 2):  300.000           ( 2): -49.3956
ERR. F =        3.501
        __****__
ERR. F =         .666
ERR. F =         .003
    ( 1):  116.557           ( 1): -.130112
    ( 2):  309.643           ( 2): .964984E-01
ERR. F =         .000
        __****__
Function termination with above values  Final analysis
follows
4300.00   ****   131.9   58.18   -49.92   .09
```

a broad band of frequencies. The isolation vs frequency characteristic of a shunt connected array of forward biased diodes is the AMC model SW-2184-1A SPST unit, shown in figure 6 which achieves 85dB isolation over the 2-18GHZ band by judiciously spacing four shunt connected diodes. An example of a switch employing an array of reverse biased series connected diodes is the AMC model SW-2000-1, shown in figure 7, which achieves 70dB minimum isolation over the 10-2000MHZ band. It is interesting to note that the SW-2000-1 unit has more insertion loss at the low end of the band than that of the SW-218-1A unit. This of course is due to the finite resistance of the forward biased series diodes in the SW-2000-1 unit.

For narrowband applications, the possibilities are endless for combining and tuning diodes for excellent tradeoffs between insertion loss and isolation. Many designers have employed series and shunt inductors to resonate the capacitance of reverse biased PIN diodes to achieve excellent isolation-insertion loss performance over limited frequency bands. (see reference 1)

VII SWITCHING SPEED

Switching speed of a PIN diode switch is generally defined as the time for the RF to traverse 10% to 90% levels. Other definitions such as the time from 1dB to 60dB levels are occasionally employed for high isolation requirements. The switching speed is generally controlled by two factors, the time required to remove the stored charge from the diode junction and the theoritical maximum speed at which the charge can be removed from the junction. The time required to remove the stored charge from the junction is limited by the transit time of the PIN diode. The transit time is given by

$$It=W1/Vs$$

where W1= the device I-region thickness (cm)

Vs=maximum saturated velocity= 10exp7 cm/sec

The I-region thickness is related to the breakdown voltage Vb by

$$W1=Vb/20$$

Additionally, the stored charge in the forward biased diode junction is related to the monority carrier lifetime of the junction by

$$Qs=I*T$$

where Qs=stored charge (coulombs)

If=forward current (amperes)

T=minority carrier lifetime (seconds)

As a minimum for operation as a PIN switch the diode lifetime is shown vs the lowest operating frequency in figure 8. Further, the transit time as a function of breakdown voltage is shown in figure 9. (see reference 2) For minority carrier lifetimes shorter than 10ns, state-of-the-art PIN drivers can switch in approximately the transition time of the device. Longer lifetimes require higher currents and larger, slower switching transistors causing switching times to be longer than the transition time.

Low intermodulation and harmonic distortion PIN switches require diodes with longer than minimum minority carrier lifetimes and hence switch more slowly.

High power PIN switches require higher Vb diodes which results in slower transition times and slower switching times.

FIGURE 4

TOPOLOGY OF NON-OSCILLATING CIRCUIT

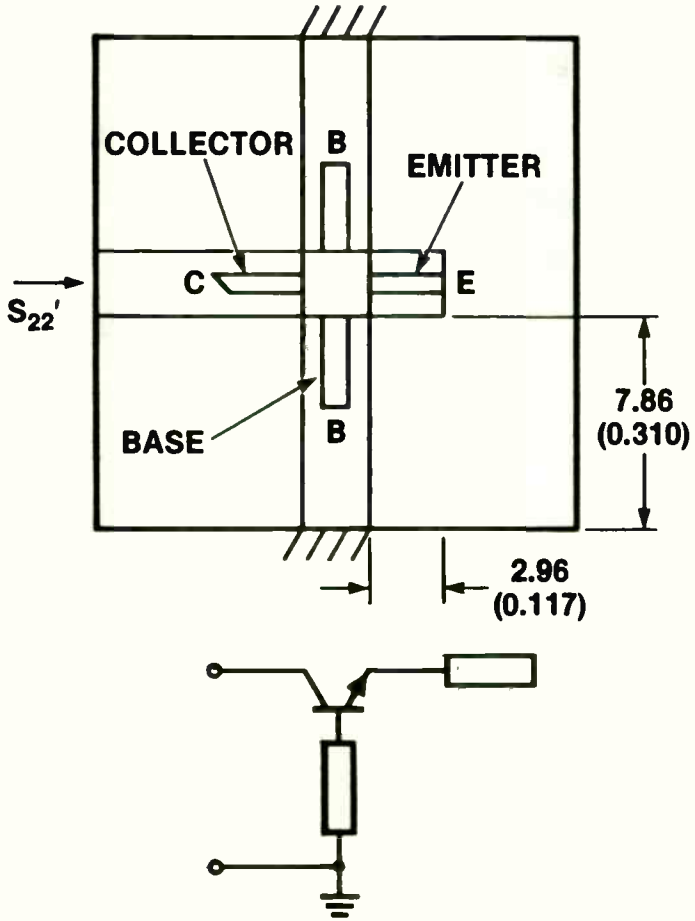
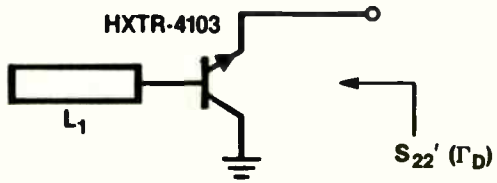


FIGURE 5

EXAMPLE NO. 2

COMMON COLLECTOR BIPOLAR

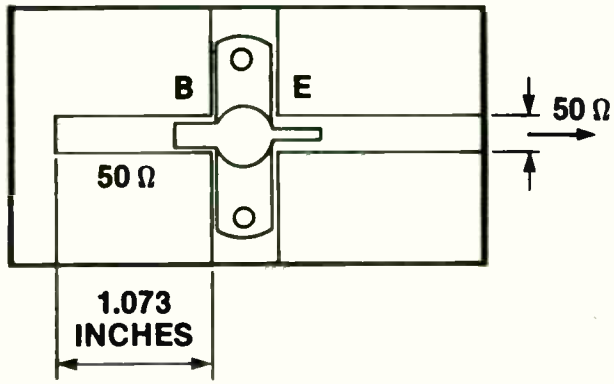


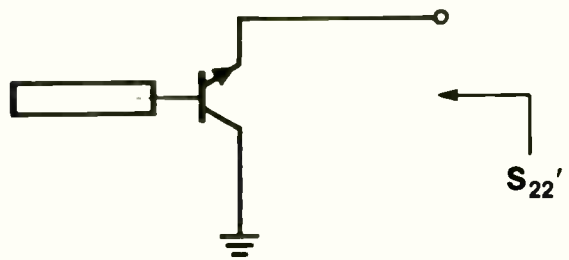
COMPACT PROGRAM TO MAXIMIZE S_{22}'

```
OST AA PA -50(20,100) -1500(10,2500) 1,0
TWO BB SI 50
CAP AA BR
PRI AA OR 50 10000 .0001
END
2000
END
1.014 -144.6 1.324 -104.7 .476 -24.9 .609 95.6
END
 .001
 -100 0 0 0
END

OPTIMIZATION BEGINS WITH FOLLOWING VARIABLES AND GRADIENTS

     VARIABLES                GRADIENTS
  ( 1): 50.0000            ( 1):-4.19617
  ( 2): 1500.00            ( 2):-264.053
 ERR. F.=    35.250
             ****
  ( 1): 50.1295            ( 1):-.312179
  ( 2): 1765.01            ( 1):-1.72275
 ERR. F.=     .044
             ****
  ( 1): 50.1367            ( 1): .246614E-01
  ( 2): 1765.50            ( 2): .421761
 ERR. F.=     .042
             ****
GRADIENT TERMINATION WITH ABOVE VALUES. FINAL ANALYSIS FOLLOWS

 F(MHZ)    RHO(MAG.<ANGLE)          RET L/G (DB)    Z(R+JX)OHM

2000.000    48.106    -166.1          33.64    -48.02    -.48
```

FIGURE 6

TOPOLOGY OF CIRCUIT





VIII POWER HANDLING

The power handling capability of PIN diode switches is controlled by three parameters. First is the upper operating temperature of the device. Second is the breakdown voltage and third the charge storage capability of the device. For silicon PIN diodes, best reliability is achieved by keeping junction operating temperatures below 200 degrees centigrade. Since series mounted diodes are more dissipative and have poorer heat sinking capabilities than shunt mounted configurations switch designers tend to avoid series configurations in high power applications. Since series configurations are essential to wideband multi-throw switches, these units tend to be the lowest power handling configurations. Hence, high power broadband switches are difficult to realize. One usually ends up trading power for bandwidth.

It is necessary that the breakdown voltage be at least twice the peak RF voltage that the diode will see and that the forward charge stored in the junction be greater than the charge moved on one-half cycle of the RF current waveform. The former requirement will assure that the diode not exceed its voltage breakdown and the latter that the forward biased junction will not be depleted in operation. The elements are essential to linear non-destructive operation of the diode under high power operation.

IX LOGIC COMPATIBLE DRIVERS

The three most popular logic families are Transistor-Transistor-Logic (TTL), Emitter Coupled Logic (ECL) and Metla Oxide Semiconductor (MOS/CMOS).

Of the three, TTL logic is by far the most popular. ECL and CMOS are a distant second. Four of the most popular forms of TTL driver circuits are shown in figure 10. We will confine this discussion to TTL compatible drivers. For best performance, switch drivers must be electrically as well as mechanically integrated in the switch unit. It is possible to achieve clean, transient free switching by designing electrically compatible drivers.

"Unit load" drivers are highly desirable because they are compatible with the widest range of TTL product line I.C.'s. A "unit load" is defined as 40 microamperes maximum source current and 1.6 milliamperes maximum sink current. Drivers are available in multiples of "unit load". True TTL compatibility also requires a logic "low" to be 0-.8 volts and a logic "high" to be 2.0-5.0 volts at the input (0.8-2.0 volts is an undefined region).

All TTL compatible drivers have delay. Generally the driver delay is defined as the time from 50% TTL level to where the RF signal changes by 10%. i.e., 0-10% for turn-on or 100-90% for turn-off. It is caused by energy storage in the driver and/or RF circuitry. The delay is a result of the time required to remove the stored energy before the switch state can be changed. The stored energy can be stored charge in the base region of a switching transistor or stored in various capacitors and inductors in the driver circuit or the bias decoupling circuit. Often this delay is different for turn-on and turn-off. This phenomenon can lead to pulse shrinkage or pulse expansion when the PIN switch is operated in a pulse mode. Since driver delay is consistent from unit to unit in a well designed PIN switch, a systems designer can often pre-trigger the switch and essentially "program-out" the driver delay. When it is not possible to anticipate the delay, it is necessary to specify delay equalization. An example of a PIN switch with equalized delay is the AMC model SW-218-1A series pulse modulator with modulation characteristics shown in figure 11. This unit has on/off delay equalization to 5ns, maximum.

FIGURE 7

TEST SET-UP FOR NON-OSCILLATING SYSTEM

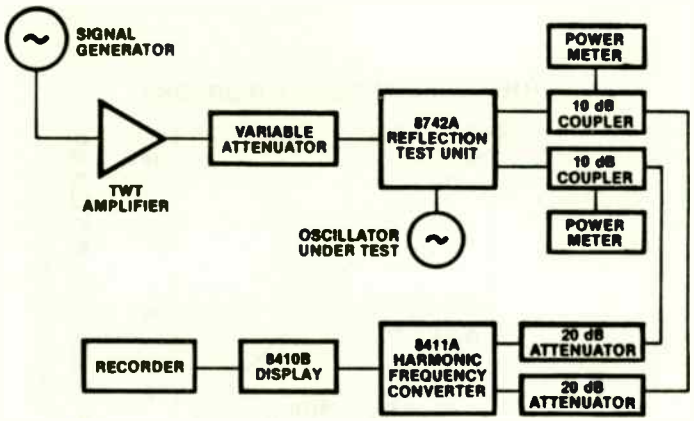


FIGURE 8

ADMITTANCE LOAD LINE

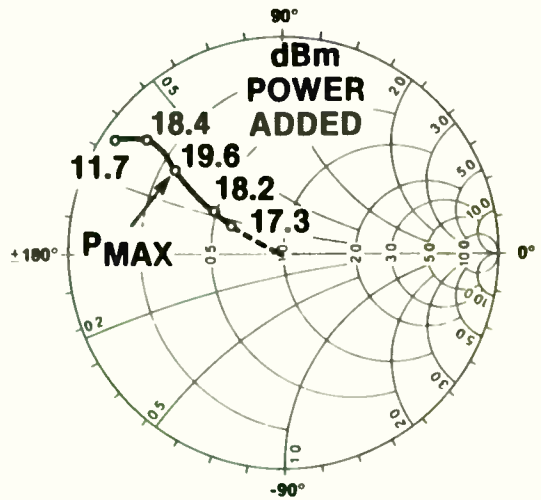


FIGURE 9

OUTPUT NETWORK DESIGN

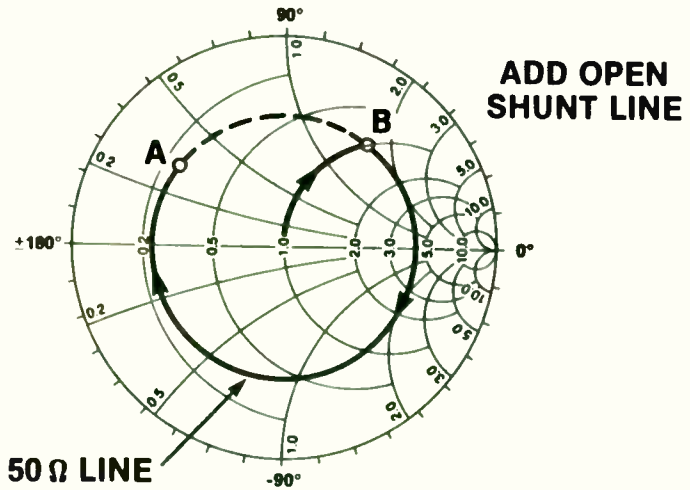
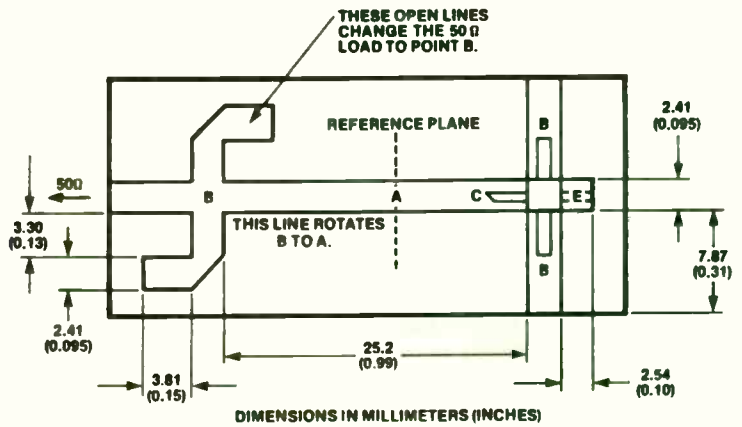


FIGURE 10

4.3 GHz FINAL OSCILLATOR CIRCUIT



Another phenomenon of driver delay is minimum pulse width. Since delay involves charging and discharging of components within the driver circuit, it isnecessary to "charge" or "discharge" the driver before any RF changes in signal level are observed. This results in a minimum pulse width for any switch with integral logic drivers. The minimum pulse width is approximately equal to the delay in the driver.

X PHASE TRACKING

Often systems require switches that are "phase tracked". A phase tracking requirement is best achieved by first equalizing the time delay between arms of a multi-throw switch (if a multi-throw is indicated) and equalizing the time delay from unit to unit within a production run or product line if required.

Since the PIN switch is made up internally of many elements, i.e., diodes, capacitors and chokes with their accompanying mounting parasitic reactances and losses, it is necessary to control the uniformity of parts and assembly techniques to achieve best phase tracking.

For unit-to-unit phase tracking on a lot-to-lot basis, it is necessary to build a phase standard unit that is maintained at the switch vendor's facility which has an impact on the price of the initial lot of switches.

Typical state-of-the-art phase tracking is as follows:

BAND	PHASE TRACKING
HF	1 Degree
UHF/VHF	2 Degrees
MICROWAVE	10 Degrees

XI OFF ARM TERMINATIONS

Often PIN switches are employed to commutate or switch VSWR sensitive components such as antenna elements in an array, oscillators or amplifiers. Normally switches have an infinite VSWR in the OFF position. Figure 12 shows a switch with off arm terminations having an extra switching section that switch the terminal in question into a matched load when that arm is turned off. This in effect controls and stabilizes the VSWR in both the ON and OFF condition of the switch. You must specify off arm terminations when it is necessary to control OFF VSWR.

Be aware that when the specified arm is commutated or switched there is a period of time when the VSWR is unspecified. This is particularly important in high power switches where momentary high reflected power levels can be troublesome.

The addition of off arm terminations adds complexity to the switch which results in additional insertion loss and poorer phase tracking.

XII INTERCEPT POINT OR COMPRESSION POINT

Compression in a PIN switch is a less well defined parameter than in say an amplifier. So we will limit our remarks in this section to intercept point. The concept of intercept point is well documented in the literature and we will not go into it here. Rather we will examine the elements that control intercept point of PIN diode switches and their tradeoff on overall switch performance.

Intermodulation is a result of nonlinear mechanisms within the PIN diode primarily and occasionally caused by other elements such as nonlinear capacitors, resistors and/or ferrite cores in the bias decoupling chokes. We will confine this discussion to the PIN diode only.

FIGURE 11

OSCILLATOR POWER CHARACTERISTIC

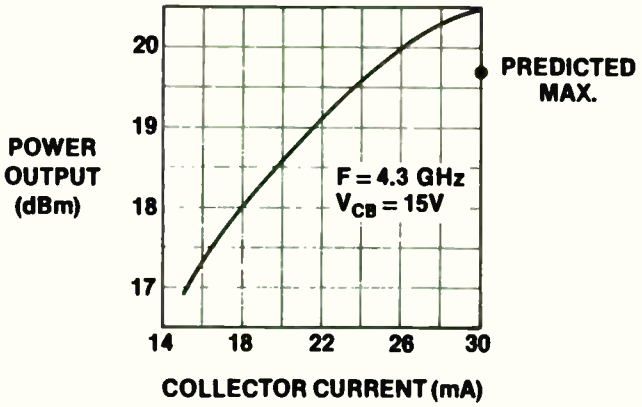


FIGURE 12

PHASE NOISE

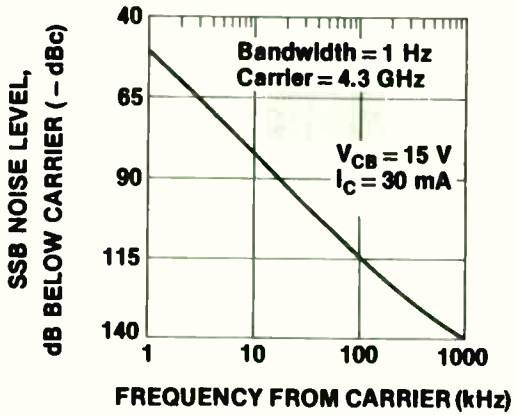


FIGURE 13

LOAD-PULL BASIC MEASUREMENT SYSTEM

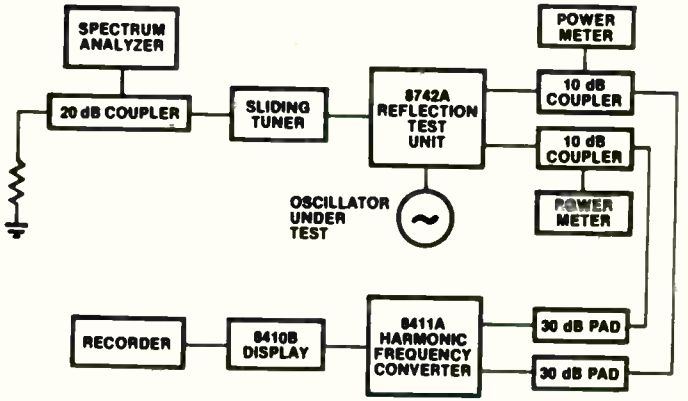
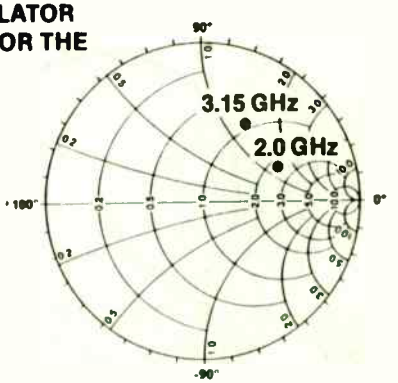


FIGURE 14

LOAD IMPEDANCE FOR MAXIMUM OSCILLATOR OUTPUT POWER FOR THE HXTR-4103



18 V
130 mA

The primary intermod generator in a PIN switch is the forward biased series PIN diode. Intermod is generated in the diode when the stored charge becomes close to being swept out (or depleted) from the I layer region. Hence low intermod switches employ diodes with longer than minimum minority carrier lifetimes and are biased at relatively high forward currents to store a lot of charge in the junction. The degree of linearity is controlled by the percentage of charge depleted from the junction by the RF cycle. Highly linear switches have small percentages of charge depletion.

A secondary intermod generator is the non-linear capacitance vs voltage characteristic of the reversed biased PIN diode. This phenomenon is relatively easily controlled by selecting diodes with flat capacitance vs voltage characteristics and biasing the device into that region of the curve.

XIII VIDEO TRANSIENTS

Refer to figure 13, the equivalent circuit of a typical PIN switch. When the diodes are switched between biasing conditions a change on voltage or current occurs at the bias decoupling element adjacent to the output terminals. This element acts to differentiate the waveform (current for the shunt inductor and voltage for the series capacitor) and cause a pulse, spike or video transient at the output terminal. This transient occurs in all PIN switches but is controllable by various means.

The most effective means of controlling video transients are:

1) Slowing the switching waveform
2) Filtering the video spectrum
3) Balancing or cancelling two equal video transients

The first is very effective when switching speed is not important. Slowing the switching waveform will slow switching speed. The second is effective when the switch operating band is above the frequency band where the video spectrum is concetrated. The addition of high pass filters at the input and output terminals of PIN switches at frequencies above 500MHZ has proven very effective in reducing transients. Typically the highest speed switches (1NS) have at least 90% of the video spectrum below 1GHZ. Filtering has its accompanying side effects. It will often introduce unwanted "ringing" in the switching waveform. Balancing has been employed very effectively as a means of reducing video transients without affecting switching speed or introducing "ringing". Unfortunately present state-of-the-art technology has limited balancing technique to UHF/VHF band. An example of the balancing technique is the AMC SWB-0070 series of IF switches shown in figure 14.

XIV CONCLUSION

Six essential and five supplementary parameters have been presented to aid in the specification of PIN diode switches. Tradeoffs between the various parameters have also been explored. It is hoped that this will help bridge the gap between switch users and switch designers.

A sample specification is presented in figure 15 to serve as a prototype switch specification to aid in bridging the gap.

REFERENCES:

1. R.N. Assaly, "PIN Diode Switches for Space Applications", MTT, 1967
2. M/A COMM PIN Diode Designers' Guide, 1983.

FIGURE 15

OUTPUT NETWORK DESIGN

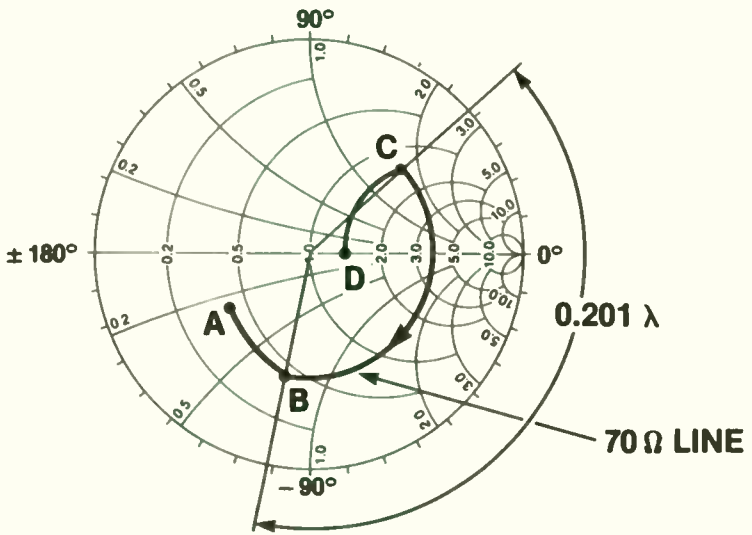


FIGURE 16

FINAL CIRCUIT TOPOLOGY FOR THE 2.0 GHz OSCILLATOR

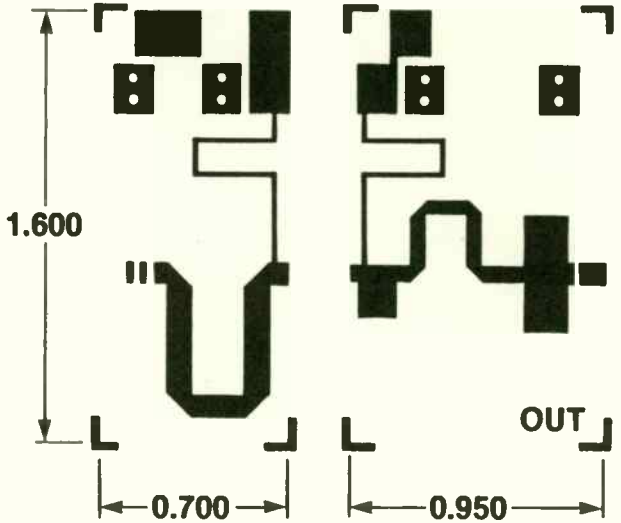
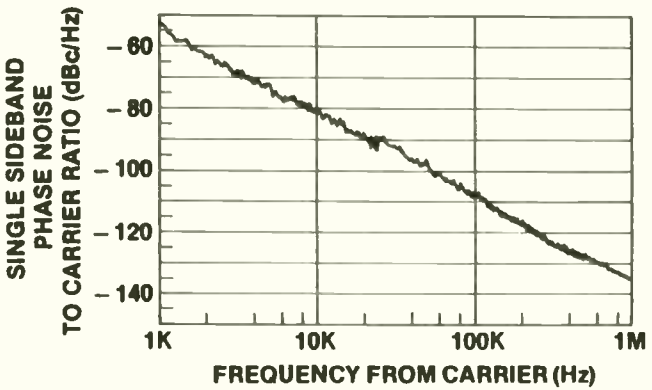


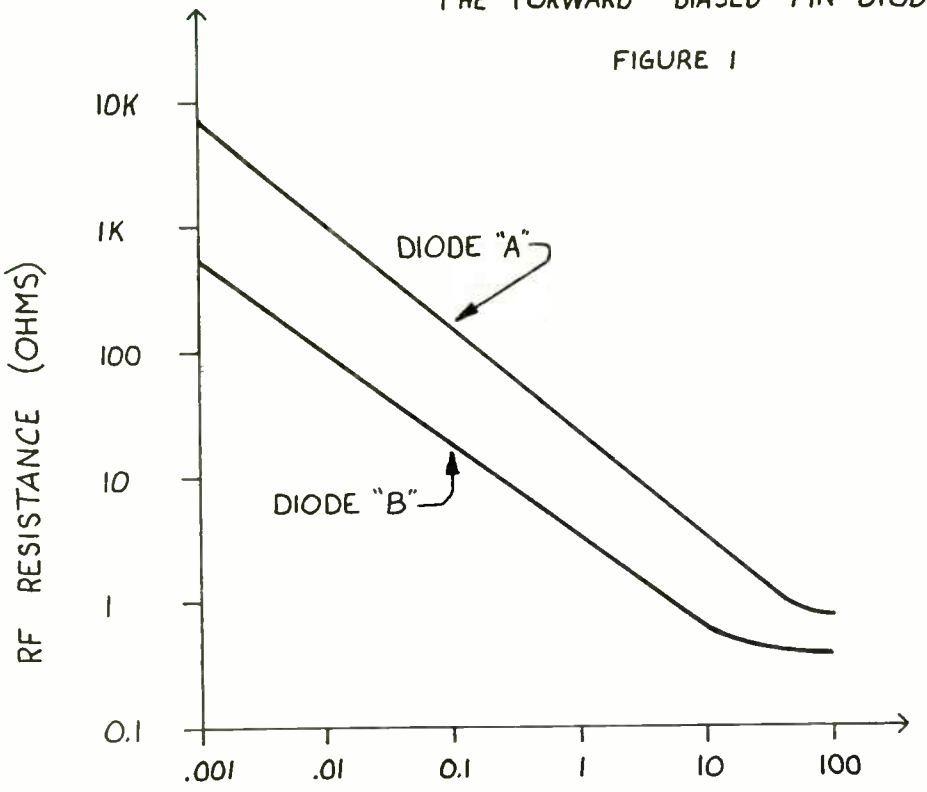
FIGURE 17

PHASE NOISE OF THE LOW Q MICROSTRIP 2.0 GHz OSCILLATOR USING THE HXTR-4103 (P_{osc} = 29.8 dBm)



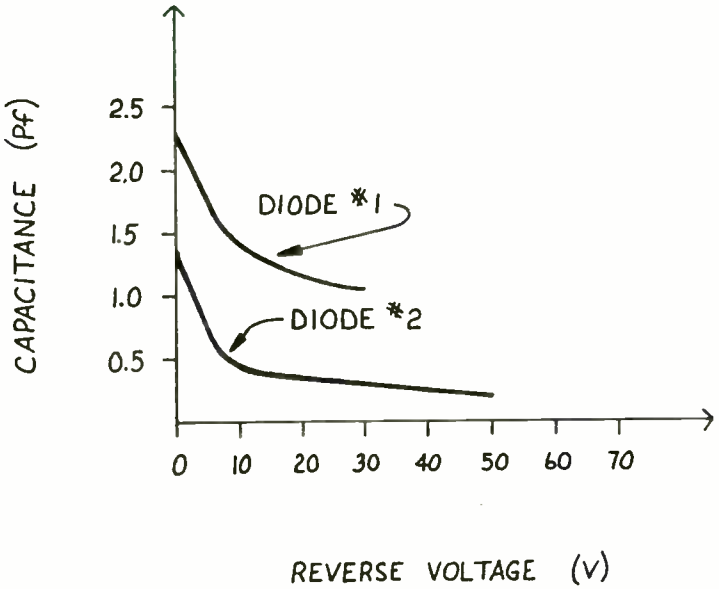
THE FORWARD BIASED PIN DIODE

FIGURE 1



RF RESISTANCE VS. FORWARD BIAS CURRENT

FIGURE 2

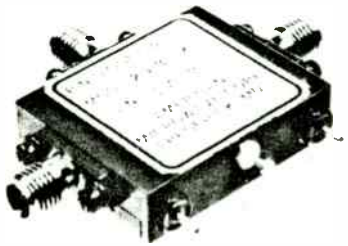


PIN DIODE

CAPACITANCE VS. VOLTAGE

FIGURE 3

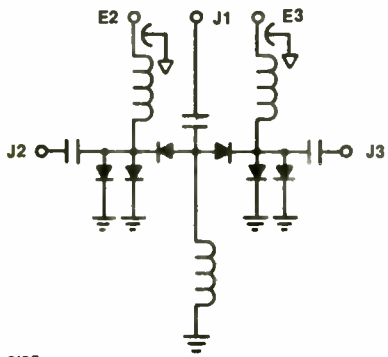
*BROADBAND PIN SWITCH SPDT
SW-218-2
0.3 TO 18 GHz



FEATURES

- 0.3 to 18 GHz Frequency Range
- Low Insertion Loss
- Small Size
- Light Weight
- Rugged Chip and Microstrip Construction

FUNCTIONAL SCHEMATIC



6/85

SPECIFICATIONS

- Frequency Range: 0.3 to 18 GHz
- Insertion Loss: 2.5 dB, Max.
- Isolation: 55 dB, Min.
- VSWR: 2.0 to 1
- Switching Speed: 100 μs typ.
- Bias: Port on: −50ma
  Port off: +30ma
- Power Handling: +20 dBm, CW, Mex.
- Operating Temp.: −85° C to +85° C

DESCRIPTION

The SW-218-2 is a SPDT Pin Switch intended for wide band switching applications in commercial and military environments. It has an instantaneous frequency coverage from 0.3 to 18 GHz and features all solid state chip diode and microstrip construction for rugged, reliable operation.

*Licensed under U.S. Patent No. 3,812,438

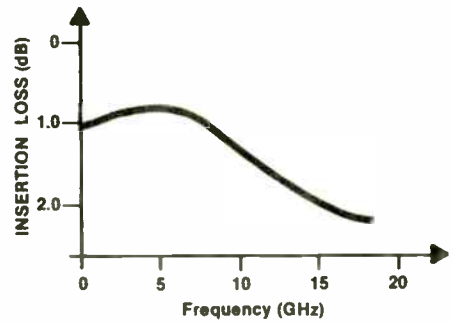
4

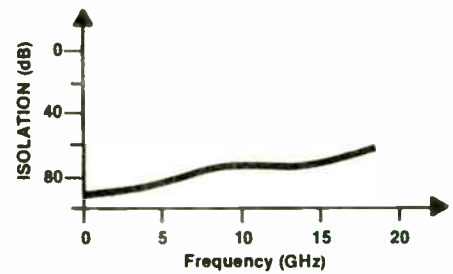
SPECIFICATIONS, Cont'd.

FREQUENCY (GHz)	0.3	0.2	4.0	8.0	12.0	16.0
MAX. INSERTION LOSS (dB)	1.2	1.2	1.1	1.0	1.8	2.5
MIN. ISOLATION (dB)	85	80	75	70	85	55
MAX. VSWR	1.7	1.5	1.5	2.0	2.3	2.3

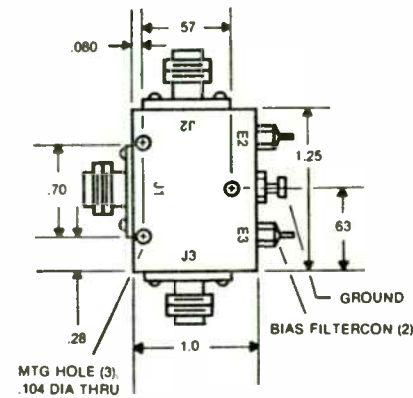
HUMIDITY, SHOCK, ETC. PER MIL-STD 202C
CONNECTORS: 1) RF: SMA FEMALE
2) BIAS: FEED THRU FILTER-SOLDER PIN
3) CONFIGURATION OPTIONS:
001- ONE MALE AND TWO FEMALE SMA CONNECTORS
002- TWO MALE AND ONE FEMALE SMA CONNECTORS
003- THREE MALE CONNECTORS

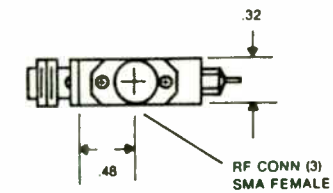
TYPICAL PERFORMANCE





MECHANICAL DATA





SERIES SHUNT CONFIGURATION

FIGURE 4

PACKAGING CONSIDERATIONS FOR RF TRANSISTORS

by

Norman E. Dye

Motorola Semiconductors

INTRODUCTION

Parasitic reactances, material losses and for higher power devices thermal limitations combine to make package selection for RF transistors a technically challenging undertaking. It has been said the best RF package is NO package. And while this is understandable, it is not practical. Thus the trick is to design a package that protects the RF die, heat sinks it and makes connections to the "outside world" with minimal deleterious effects.

This paper will discuss thermal, electrical, mechanical and other considerations in the design of RF packages. Several existing packages will be described in discussing the evolution of RF packages. Finally, new approaches will be proposed to achieve packages with satisfactory characteristics at LOWER COST.

RF TRANSISTOR PACKAGE CHARACTERISTICS

Figure 1 is a summary of the primary characteristics of a package suitable for use with high power at high frequencies. Thermal and electrical requirements predominate; however, many other factors influence what can and can't be done in designing an acceptable RF package. These characteristics will be discussed in the following paragraphs.

THERMAL CONSIDERATIONS

The name of the thermal game with RF devices is to maintain die temperature below a prescribed temperature (150 degC to 200 deg C) during normal operation. For low power devices with the die mounted on the collector portion of the lead frame or on alumina oxide ceramic, this presents little difficulty for dissipations below 1/4 watt. Typical packages are shown in Figure 2. Use of a copper lead frame and modest heat sinking of the collector lead can increase the dissipation limitation to 3/4 watt. A wider, thicker collector lead results in the so-called PowerMacro package (Figure 3) which has a thermal rating of 1.5 watts.

However, where higher power dissipation is required, the RF die must be heat sunk through some medium which offers low thermal resistance while maintaining electrical isolation. The most practical material currently available offering low thermal resistance and simultaneously high electrical resistance is beryllium oxide (BeO). Figure 4 depicts the thermal properties of BeO compared with other materials. Figure 5 shows electrical resistivity of BeO along with several common insulators.

ELECTRICAL CONSIDERATIONS

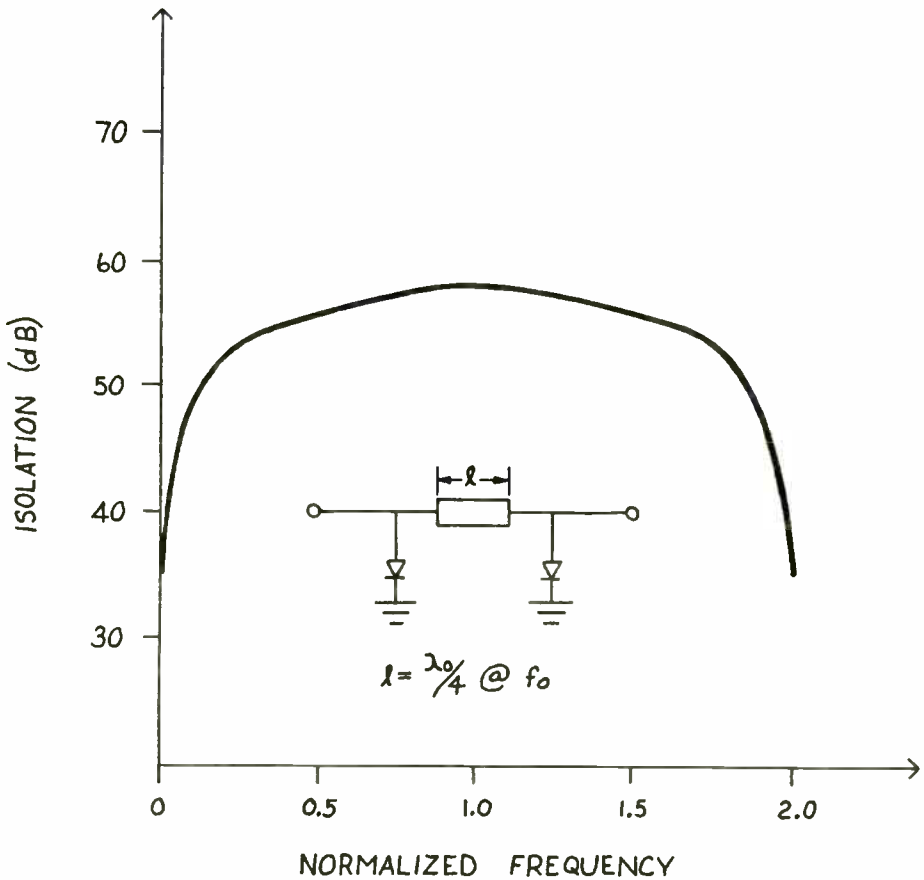
Objectively, one wishes to make contact with the RF die while keeping parasitic capacitance and inductance along with conductivity losses at a minimum. Package design--location of external leads, thickness of BeO, path length from die to external lead connections and choice of plating materials allow the package designer to approach these desired results.

A key objective is to keep lead length from die to the external circuit as short as possible. Also leads (including current paths on the ceramic) must be sufficiently wide to prevent excess resistance or inductance. And most important the plating on both ceramic and leads must be low loss and sufficiently thick in skin depths to minimize series resistance to RF current flow.

OTHER CONSIDERATIONS

Other factors in addition to thermal and electrical must be considered in designing RF transistor packages. Primarily these can be grouped under "Reliability and Cost" although some may fall more conveniently under "Customer Convenience." In the latter category are items such as type of heat sink (stud or flange) and form factor (surface mount, machine insertable, stripline compatible, etc.)

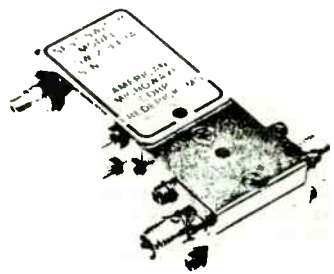
Reliability, here, covers die attach, wire attach, hermeticity and lead solderability. Both die and wire attach are dependent on plating. High power die attach must have void free, low thermal resistance bonds (Silicon-Gold eutectic is the most common) to prevent thermal hot spots and these bonds can be achieved most readily with an adequate amount of smooth, pure gold (Au). Wire bonds are generally reliable whether Au on Au, Au on aluminum (Al), Al on Au or Au on copper (Cu) but if Au plating of the package is involved with Al wire, it is imperative that the plating be free of even the smallest amounts of Thallium (used sometimes in Au plating solutions to improve rate and smoothness of plating).



ISOLATION VS. FREQUENCY, SHUNT ARRAY

FIGURE 5

*SERIES SW-218 WIDEBAND SPST PIN DIODE SWITCHES WITH INTEGRAL DRIVERS



FEATURES

- 0.3 to 18 GHz Frequency Range
- Low Insertion Loss
- Up to 85 dB Isolation
- High Speed - 10 nsec
- Small Size
- Light Weight
- Rugged Chip and Microstrip Construction

DESCRIPTION

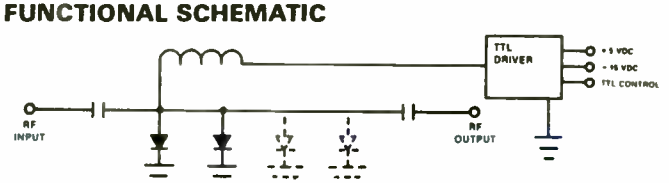
The series SW-218 switches are broadband, high speed, low loss SPST switches with integral drivers. They are powered by +5 and −15 volt supplies and are available powered by ±15 volts. They are available in three models that operate over the entire 0.3 to 18 GHz band. Each features rugged integrated circuit assemblies of chip PIN on a microstrip transmission line and proprietary wideband bias decoupling circuitry.

Switching is accomplished by a TTL compatible driver which is controlled by the user.

SPECIFICATIONS

- Control Impedance - TTL Compatible, One Load. (A Load is 1.6 mA Sink Current and 40 µA Source Current.)
- Control Logic - Logic "0" (−0.3 to +0.7 Volt) for Switch OFF. Logic '1" (+2.5 to +5.0 Volts) for Switch ON.
- Temperature - Operating: −65°C to +85°C Non-operating: −65°C to +125°C
- Humidity, Shock, Etc. - Per MIL-STD 202C

FUNCTIONAL SCHEMATIC



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*Licensed under U.S. Patent No. 3,812,438

6

Hermetic packages, a representative sample of which is shown in Figure 6, have requirements contrary to those of good RF packages. The lead length through the hermetic seal is usually longer and more lossy than the length required for similar non-hermetic packages. Today, hermeticity is seldom warranted for commercial applications. Modern transistors are constructed with silicon nitride (SiN4) die passivation, Au top metal and Au wire which alleviates the need to keep moisture and foreign material from coming in contact with the die and wire bonds. However, if packages are subjected to contaminants such as those found in vapor phase soldering and subsequent flux removal solutions, gross leak hermeticity is important to prevent particles from getting inside the transistor where long term chemical action could result in premature device failure.

Lead solderability is generally thought to create no problems provided leads are covered with not less than 50 micro-inches of Au plating. But even Au can cause difficulties in soldering if sufficient time is used in soldering such that the Au plating is dissolved in the solder solution. Also, both silver (Ag) and Cu tarnish such that these material finishes are rendered useless unless the user is willing to remove the oxides just prior to solder attach (or use the parts with minimal shelf life).

Of the many "other" considerations in designing an RF package, perhaps the most important of all is COST. Metal ceramic packages represent 50% or more of the product cost for most RF transistors. The basic problem, then, is how to devise a package with suitable RF characteristics in which a transistor can be assembled without difficulty, which can be put to use at some time in the future, with high reliability, and yet be relatively low in cost.

What are the cost ingredients of RF packages? One can identify 3 major components as shown in Figure 7. These are materials (such as ceramic disc, metal heat sink and lead frame), brazing operations used to assemble the constituent pieces, and plating. Brazing is probably the least expensive of the three and since it is essential--without creating user problems in heat sinking (no heat sink on package) and/or soldering into a circuit (no leads on package)--it will not be discussed further.

Material costs particularly when using BeO can be a sizeable portion of the total package costs. Reduce the amount of BeO and you can reduce material costs. Finally there are plating costs. Since Au is a normal final plate for an RF package for the obvious reasons of good conductivity, inertness, etc., it became a prime target of cost reduction particularly when Au was selling for $800/oz. 1) Even today at $325/oz. Au adds significantly to RF package costs and efforts continue to eliminate it wherever possible.

EVOLUTION OF BASIC PACKAGE TYPES

The SOE Package

In the early 1960's as transistors began to deliver watts of power at frequencies greater than 50 MHz, a new RF power package evolved suitable for micro-strip circuit applications. It was called Stripline Opposed Emitter (SOE) after its planar lead construction with two opposing leads tied to the common element in grounded emitter amplifiers. A picture of the SOE is shown in Figure 8. The raised bridge - an integral part of the lead frame - permits both short base and emitter wires simultaneously thereby reducing parasitic reactances. Thickness of the BeO (typically 60 mils) resulted in a compromise between thermal resistance (thin BeO desired), electrical resistance (thick BeO desired), and mechanical considerations necessary for heat sink attach without fracture of the ceramic disc (thick BeO desired).

Variations of the basic SOE package have resulted in the dual emitter bond (DEB) package (Figure 9). The addition of a 2nd emitter bridge (flat) on the BeO surface allows parallel emitter wires which lowers emitter inductance leading to increased amplifier gain. By widening the flat emitter stripe, the semiconductor manufacturer can add a MOS capacitor thereby achieving the input matched package (CQ or J0) (Figure 10). Wiring the capacitor between base and emitter raises the input impedance, reduces input losses and reduces input Q. Matching inside the package close to the die is essential for higher power, higher frequency devices in which Zin and/or Zout of the die is less than 0.5 ohms. Without input matching, a device would exhibit excessive circuit losses as well as extremely narrow band characteristics.

The Isolated Collector Package

An attempt to achieve the lowest possible common element inductance resulted in the transistor die being isolated on a collector "island" completely surrounded by the common element metallization (Figure 11). Of course this requires the collector contact to be made via

1)First, Au was removed from the heat sink (flange or stud) where it served no useful purpose other than appearance. Next the Au was reduced in thickness (typically to 50 micro-inches) in all areas of the package except the die bond pad where it is essential to maintain >100 micro-inches of Au to achieve void free Si-Au eutectic bonds.

SPECIFICATIONS, Cont'd.

MODEL NO.	CHARACTERISTICS	FREQUENCY (GHz) 0.3 to 1.0	1.0 to 2.0	2.0 to 4.0	4.0 to 8.0	8.0 to 12.4	12.4 to 18.0	SWITCHING* SPEED ON-to-OFF and OFF-to-ON	POWER HANDLING CAPABILITY AVG (WATTS)	Peak 1 µsec, max. pw (WATTS)	POWER SUPPLY +15 VDC	+5 VDC	−15 VDC
SW-2182-1A	Min Isolation (dB)	30	40	45	45	45	45	10 ns	2	10	55 mA	55 mA	35 mA
	Max Ins Loss (dB)	1.0	1.0	1.0	1.1	1.6	2.0						
	Max VSWR (ON Pos)	1.3	1.3	1.4	1.6	1.9	1.9						
SW-2183-1A	Min Isolation (dB)	40	60	70	70	70	70	10	2	10	65 mA	65 mA	35 mA
	Max Ins Loss (dB)	1.0	1.0	1.1	1.4	1.8	2.3						
	Max VSWR (ON Pos)	1.4	1.4	1.4	1.6	1.9	1.9						
SW-2184-1A	Min Isolation (dB)	45	70	85	85	85	80	10	2	10	75 mA	75 mA	35 mA
	Max Ins Loss (dB)	1.0	1.0	1.2	1.5	2.0	2.5						
	Max VSWR (ON Pos)	1.4	1.4	1.4	1.6	1.9	1.9						

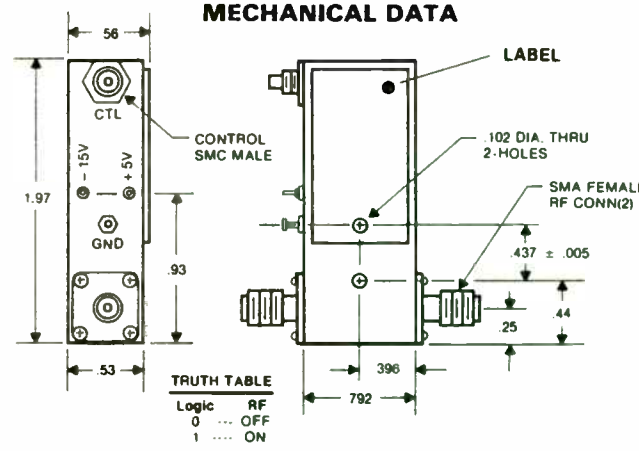
*Switching speeds are 10% to 90% RF and 90% to 10% RF. Standard TTL delay is 20 ns, Max from 50% TTL to 90% RF for turn-off and 50 ns, Max from 50% TTL to 10% RF for turn-on.

FIGURE 6

AVAILABLE OPTIONS

Option No.	Description
001	Two SMA Male RF Connectors
002	One SMA Male and One SMA Female RF Connector
003	Solder Type Control Terminals
004	±15 Volt Power Supply Requirement (+5, −15 Volt is Standard)
005	50 Ohm Control Impedance
006	Cannon Multipin MDM9SSP
007	Inverted Logic
008	Extend Frequency to 100 MHz
009	20 ns, Max Delay
010	100 ns, Max Switching Speed
011	
012	2 ns, Max Switching Speed

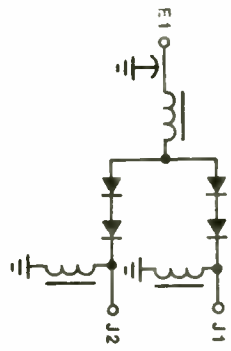
MECHANICAL DATA



FEATURES

- Wide Bandwidth - 10-3000 MHz
- Low Insertion Loss
- Solid State Reliability
- Available up to SP5T
- High Intercept Point
  +80 dBm 2nd Order
  +45 dBm 3rd Order
- TTL Control Available

FUNCTIONAL SCHEMATIC



SPST PIN DIODE SWITCH
MODEL SW-2000-1
10-3000 MHz

SPECIFICATIONS

Frequency Range:	10-3000 MHz
OFF Isolation:	
10-1000 MHz	80 dB, Min
1000-2000 MHz	70 dB, Min
2000-3000 MHz	60 dB, Min
ON Insertion Loss:	
10-500 MHz	1.0 dB, Max
500-1000 MHz	1.5 dB, Max
1000-2000 MHZ	2.5 dB, Max
2000-3000 MHz	3.5 dB, Max
VSWR:	50 Ohms
Harmonic Distortion:	
2nd Harmonic:	−60 dBc @ 0 dBm
Switching Speed:	5 µs, typical
Bias:	
ON Port	100 ma, Max
OFF Port	−25 v, Max
Temperature Range:	−50 to +85 Deg C
RF Connectors:	SMA

wires which can result in increased collector series inductance. Again provisions can be made for use of an input matching capacitor (Figure 12), or both input and output matching capacitors (Figure 13).

Common Emitter TO39 (CE-TO39)

Cost considerations led to the addition of BeO to a conventional TO39 package (see Figure 14) in a successful effort to reduce the cost of 1 to 4 watt driver transistors operating at frequencies through 500 MHz. Tying the emitter leads to the case and isolating electrically the collector results in high performance (>10 dB gain) amplifiers that cost in the vicinity of $1 to $2-- a substantial decrease in price from SOE packaged devices.

Common Emitter TO220 (CE-TO220)

Still the power levels above 4 watts even at frequencies as low as 50-100 MHz required the use of the expensive SOE package. This necessitated the modification of a low cost, higher power package (the TO220) such that satisfactory RF performance could be achieved at least through 175 MHz. Again the key was the use of BeO to isolate the collector and permit low inductance "grounding" of the emitter as shown in Figure 15.

Cost savings are not as substantial as in the case of TO39's. Although the basic TO220 package is lower in cost than a TO39, modifying the TO39 involves a relatively small amount of unpatterned BeO while the TO220 requires larger, patterned BeO and, generally, with "wraparound" metallization. The basic package costs of the CE-TO220 can be approximately half that of an SOE and if these savings can be maintained through subsequent assembly and final test operations (not an easy feat to accomplish), the resulting transistor should have a sell price $1 to $2 less than a comparable SOE packaged part.

Frequency and power limitations do exist in the TO220 package. Basically it is highly undesirable from the standpoint of parasitic lead inductance which results in the package essentially being impractical for use at power levels above 40 watts at 50 MHz, 30 watts at 200 MHz and 10 watts at 500 MHz.

NEW PACKAGE CONCEPTS

Achieving packages that still provide low thermal resistance, low parasitics, ways to heat sink and ways to access the terminals of the transistor all at LOWER COST is still the primary objective of modern day RF packaging efforts. A novel approach at Motorola is to minimize use of Au by using it only on the die bond pad of an essentially standard SOE package (Figure 16). Excellent electrical conductivity is still achieved by the use of a copper clad lead frame with the external leads tin plated after assembly. One major problem with this process is the necessity for package hermeticity during the lead plating operation. Also the design concept leaves the basic SOE package intact - which means the cost of patterned BeO and the cost of brazing remain essentially unchanged.

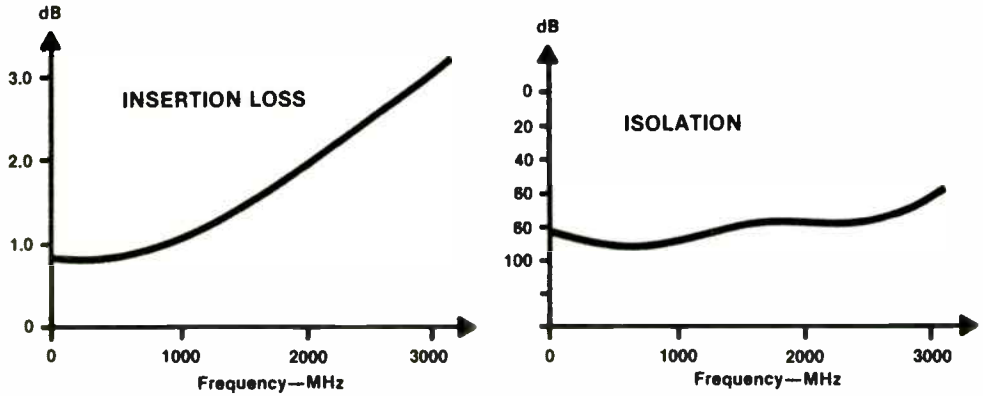
Reducing the BeO is the major thrust of another new RF package concept. Since BeO is only needed under the active transistor die, it can be reduced from a patterned disc or rectangle to a small unpatterned disc or rectangle that is substantially less costly to manufacture. One example of such a package is shown in Figure 17. Here the center disc is BeO while the outer ring is less expensive aluminum oxide (Al_2O_3). The lead frame includes a collector lead that bridges the gap between materials and covers the collector bond pad area. While the amount of BeO is minimized, other costs such as brazing and plating are left unchanged. And the extended collector lead necessitates use of a separate raised bridge (if desired).

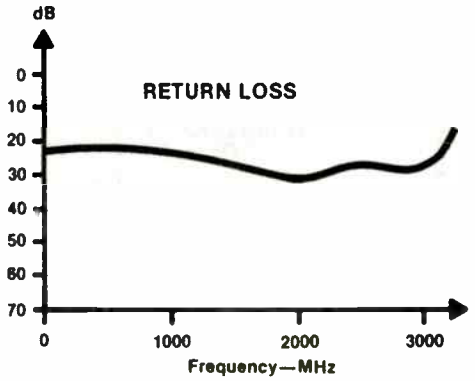
A less expensive concept that utilizes a semiconductor manufacturer's main asset - the ability to process silicon - is shown in Figure 18. Two thick rectangles of intrinsic silicon are placed on either side of a rectangular block of unpatterned BeO. The three metalized but electrically insulating pieces are brazed to a copper flange along with two pieces of lead frame material. It is relatively simple (and inexpensive) to pattern the silicon rectangles to provide shorting bars on the sides adjacent to the BeO. Wiring, then, provides for collector and base contacts and dual emitter bonds.

SUMMARY

Packages suitable for use at RF frequencies must have low parasitics and low loss. For power transistors, the package must also have low thermal resistance from die to case. These requirements historically have resulted in RF power packages being a significant portion of the manufacturing cost of RF power transistors.

TYPICAL PERFORMANCE





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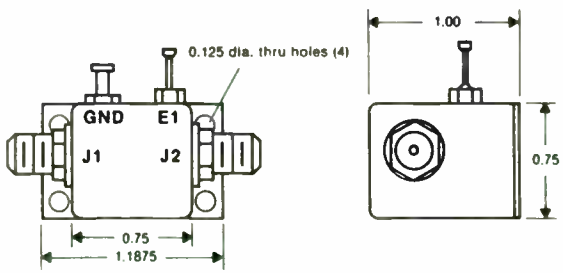
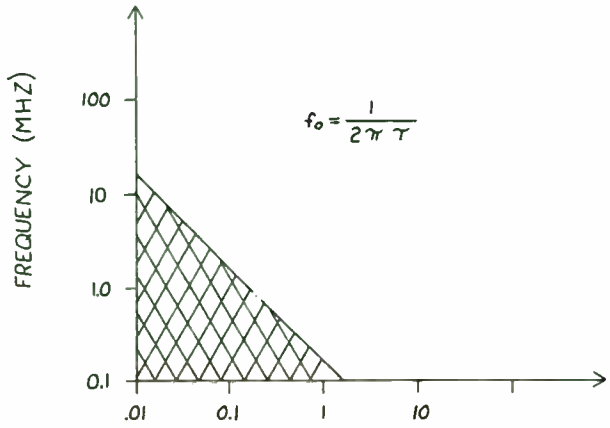
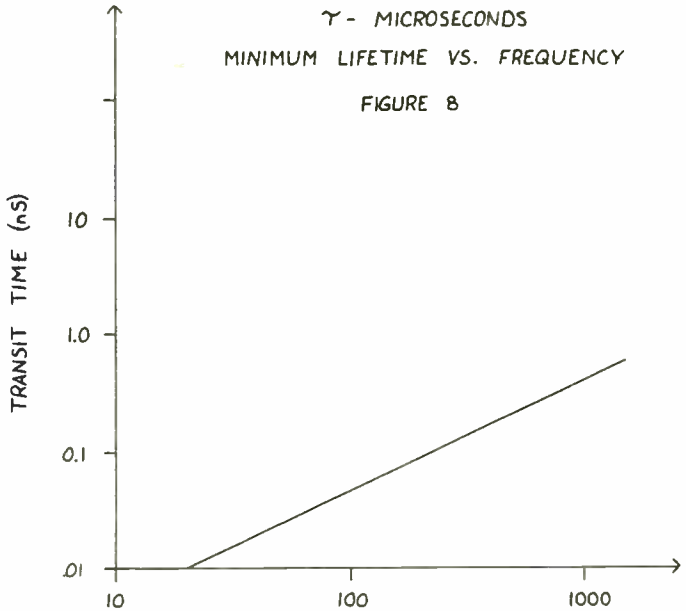


FIGURE 7



MINIMUM LIFETIME VS. FREQUENCY

FIGURE 8



TRANSIT TIME VS. BULK BREAKDOWN VOLTAGE

FIGURE 9

Various packages have been designed (CE-TO39, CE-TO220) in efforts to reduce package costs; however, their limitations with respect to power dissipation and parasitics make them unsuitable except in very restricted applications.

This paper has discussed the considerations necessary in RF package design and the evolution of a variety of packages suitable for use at radio frequencies. Finally, several alternate approaches to devising a LOW COST package suitable for use at both high power and high frequency have been proposed.

FIGURE 1

CHARACTERISTICS OF RF POWER PACKAGES

1. **GOOD THERMAL PROPERTIES**
2. **LOW INTERELECTRODE CAPACITANCE**
3. **LOW PARASITIC INDUCTANCE**
4. **HIGH ELECTRICAL CONDUCTIVITY**
5. **RELIABLE**
6. **LOW COST**
7. **FORM FACTOR SUITABLE FOR CUSTOMER APPLICATION**

K7127

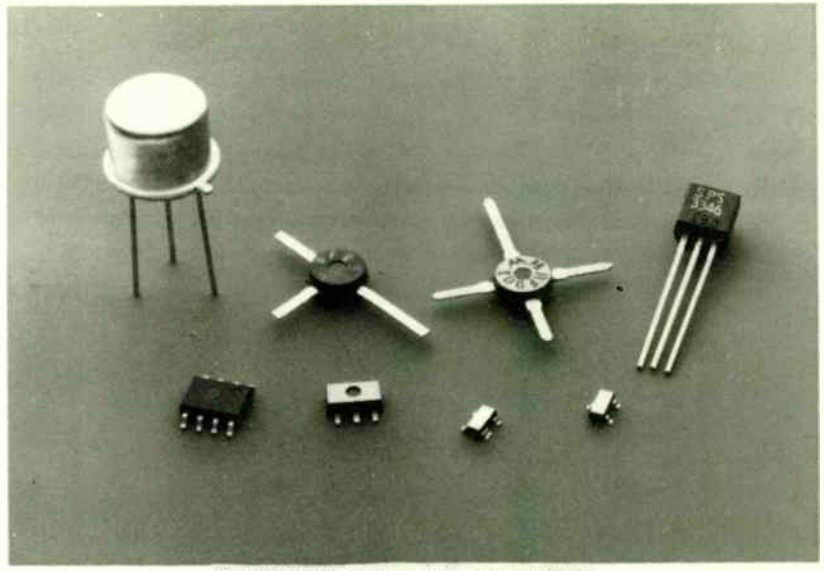


FIGURE 2-LOW POWER PACKAGES FOR RF

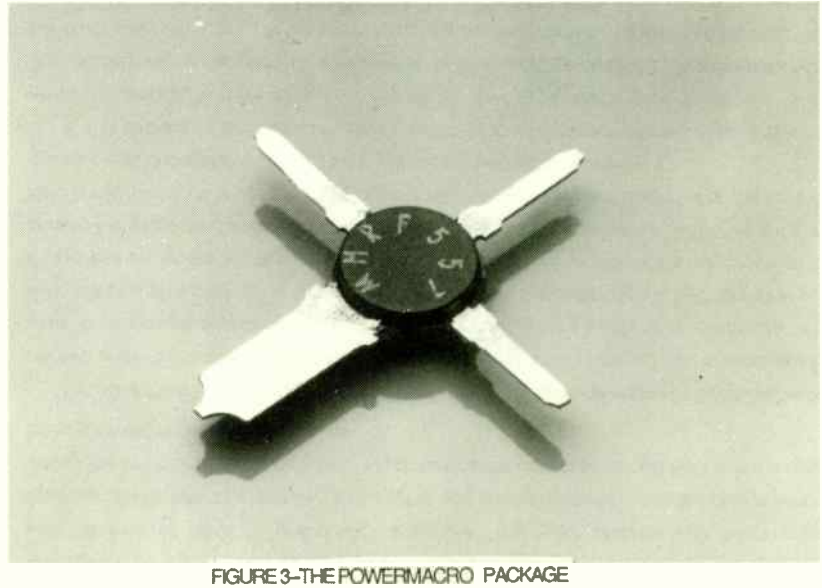
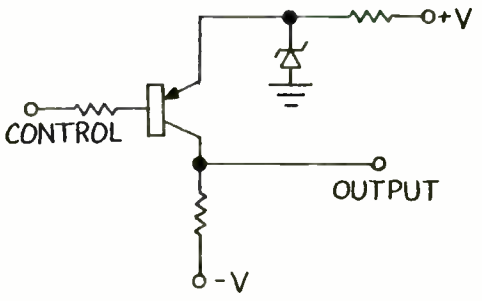
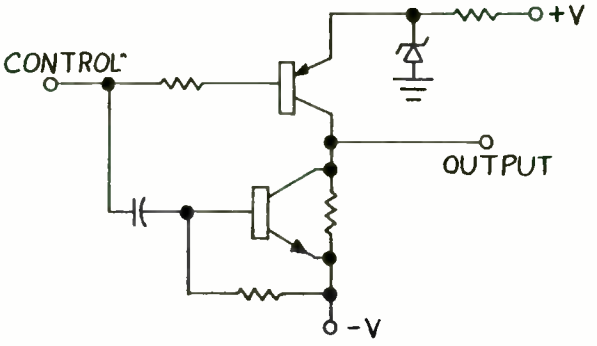


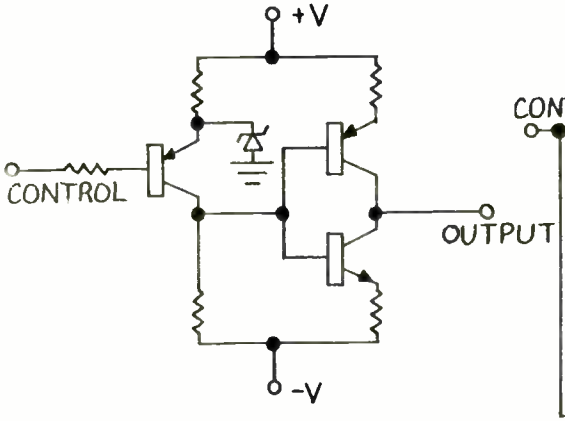
FIGURE 3-THE POWERMACRO PACKAGE



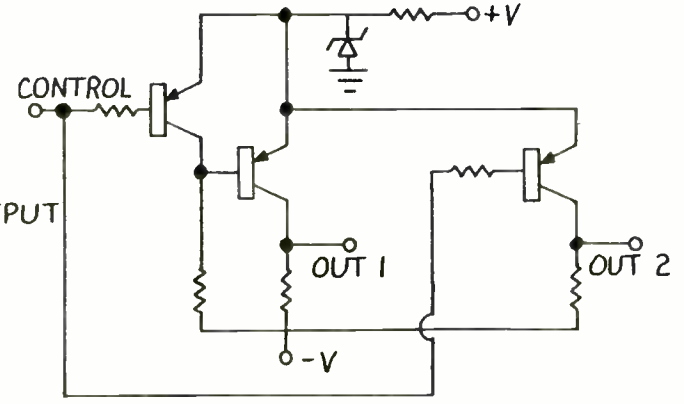
SINGLE TRANSISTOR DRIVER
(a)



SINGLE TRANSISTOR WITH SPIKER
(b)

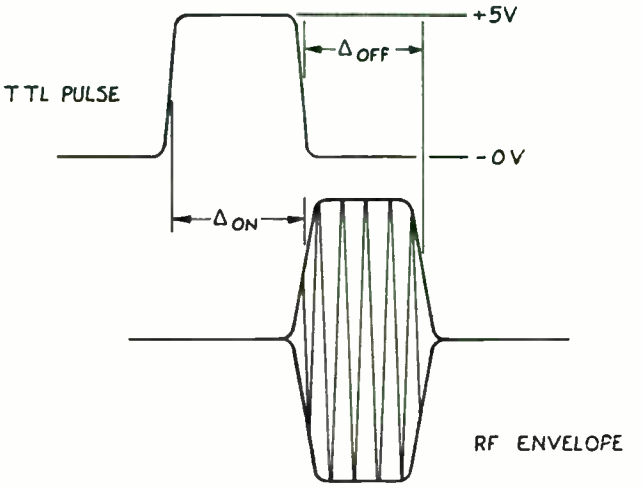


PULL-UP, PULL-DOWN TOTEM POLE
(c)



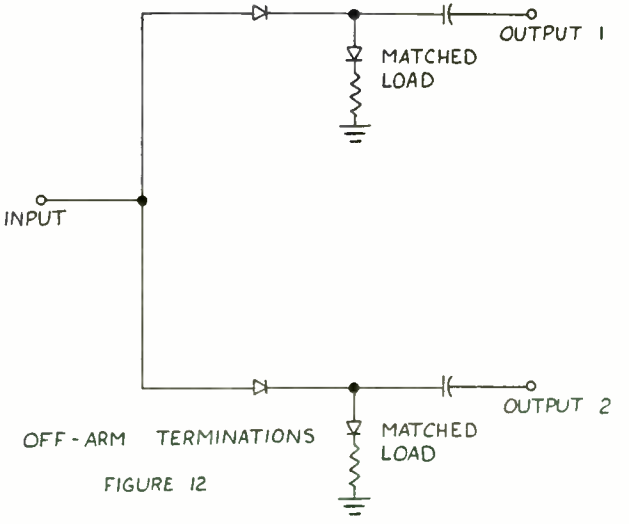
COMMUTATING DRIVER
(d)

TTL DRIVER CIRCUITS
FIGURE 10



DRIVER DELAY EQUALIZED

FIGURE 11



OFF-ARM TERMINATIONS

FIGURE 12

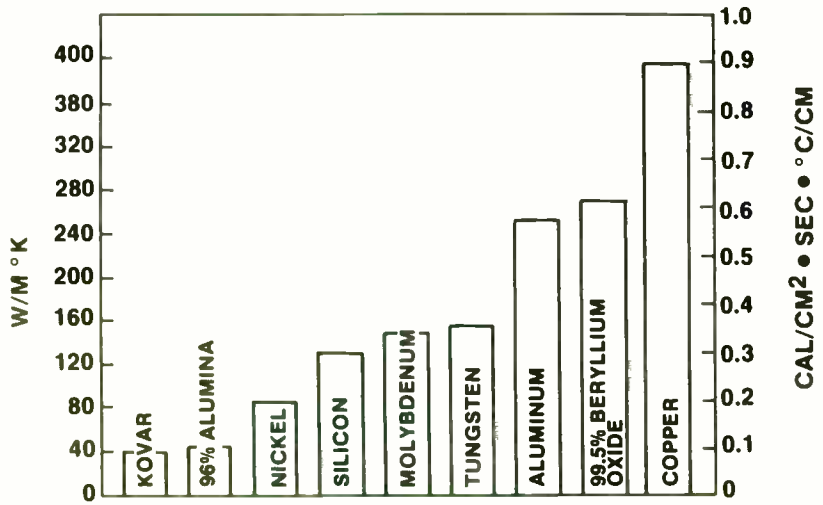


FIGURE 4–THERMAL PROPERTIES OF METALS/CERAMICS

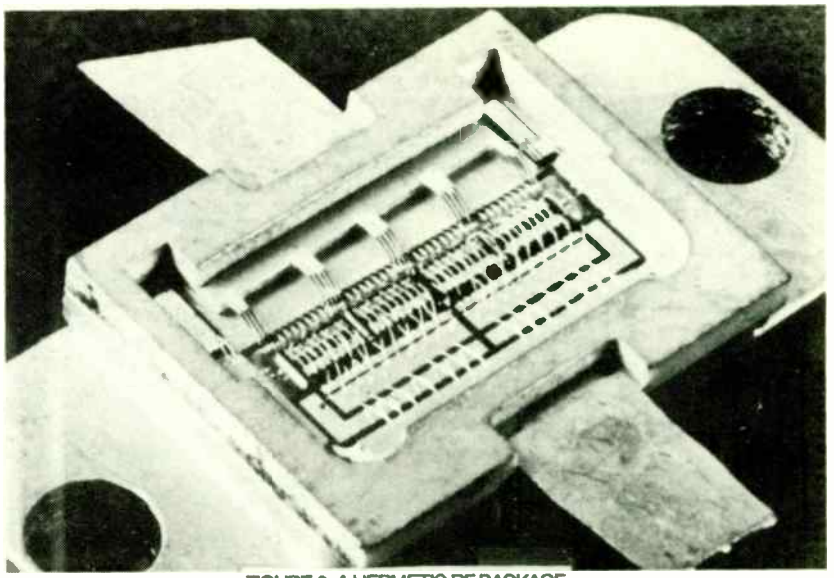


FIGURE 6–A HERMETIC RF PACKAGE

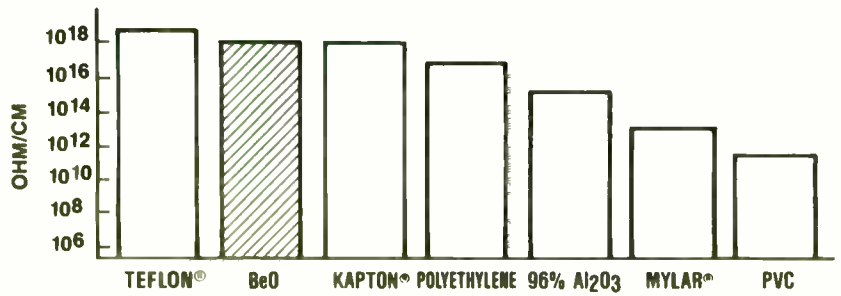


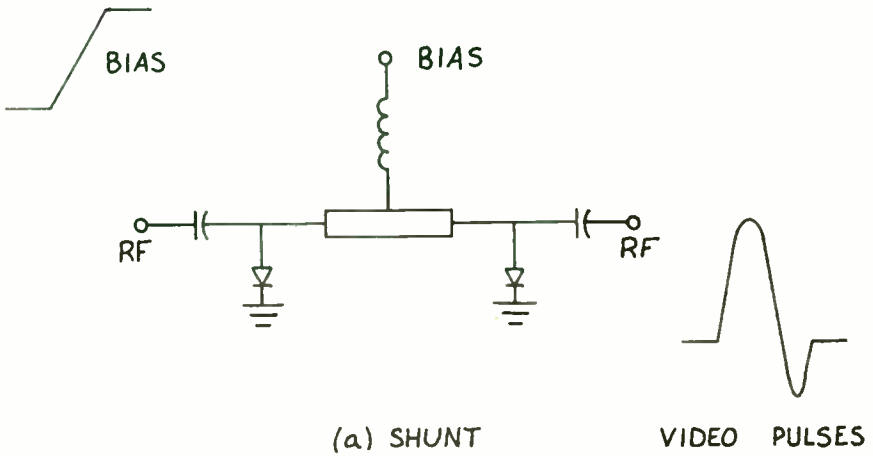
FIGURE 5–ELECTRICAL RESISTIVITY OF TYPICAL INSULATORS K7129A

FIGURE 7

COST INGREDIENTS OF TYPICAL RF POWER PACKAGE.

MATERIAL		$0.40
BeO	$0.08	
METALLIZATION OF BeO	0.10	
FLANGE, Ni PLATED	0.10	
LEAD FRAME, Ni PLATED	0.12	
ASSEMBLY		0.15
FINAL PLATE		0.45
		$1.00

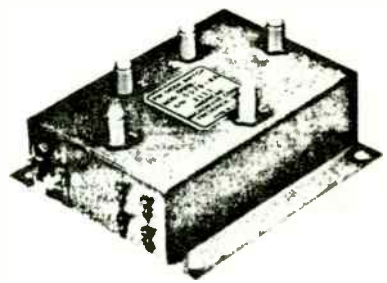
K7125



PIN SWITCH EQUIVALENT CIRCUITS

FIGURE 13

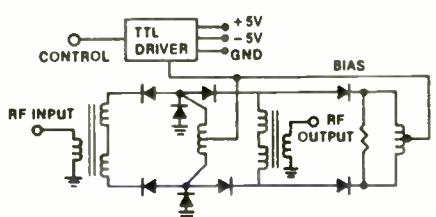
SWB-0070 SERIES
HIGH SPEED I.F. SWITCHES
WITH TTL DRIVERS
50 - 90 MHz



FEATURES

- HIGH SPEED: 10 ns, Max
- LOW TRANSIENT: 50 mv, Max
- Reverse Polarity Protection
- 300% Overload Protection for Up To 2 Minutes
- Rugged Microstrip Construction
- Integrated TTL Drivers
- HIGH ISOLATION: 70 dB, Min
- Off-arm Terminations
- SPST Thru SP8T Configurations

FUNCTIONAL SCHEMATIC (SPST)



SPECIFICATIONS

TYPE	MODEL
SPST	SWB-0070-1A
SP2T	SWB-0070-2A
SP3T	SWB-0070-3A
SP4T	SWB-0070-4A
SP5T	SWB-0070-5A
SP6T	SWB-0070-6A
SP7T	SWB-0070-7A
SP8T	SWB-0070-8A
- Frequency Range: 50-90 MHz
- Insertion Loss: 1.5 dB, Max
- Isolation: 70 dB, Min
  80 dB, Typ
- Switching Speed: TTL Delay: 5 ns, Max
  10%-90% RF: 10 ns, Max
  90%-10% RF: 10 ns, Max
- Video Transients: 50 mv, Max
- Return Loss: Input: – 17 dB, Min
  Output (on): – 17 dB, Min
  Output (off): – 14 dB, Min
- Intermodulation:
  3rd Order: 2 Tones @ +7 dBm,
  – 50 dBc

FIGURE 14

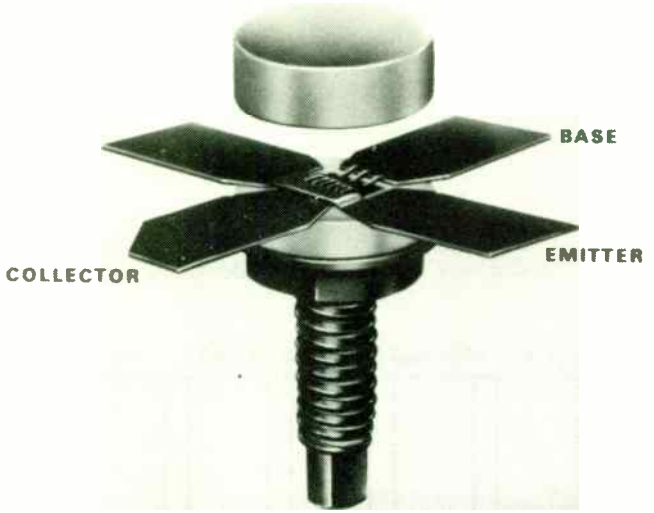


FIGURE 8–THE STRIPLINE OPPOSED EMITTER PACKAGE

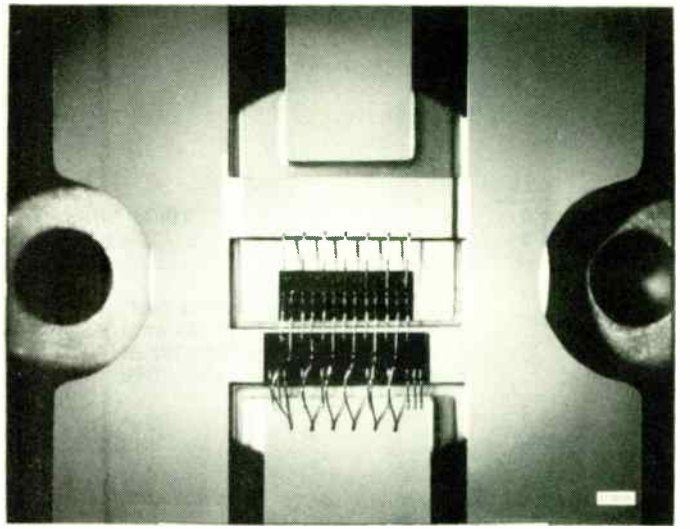


FIGURE 10–THE INPUT MATCHED PACKAGE

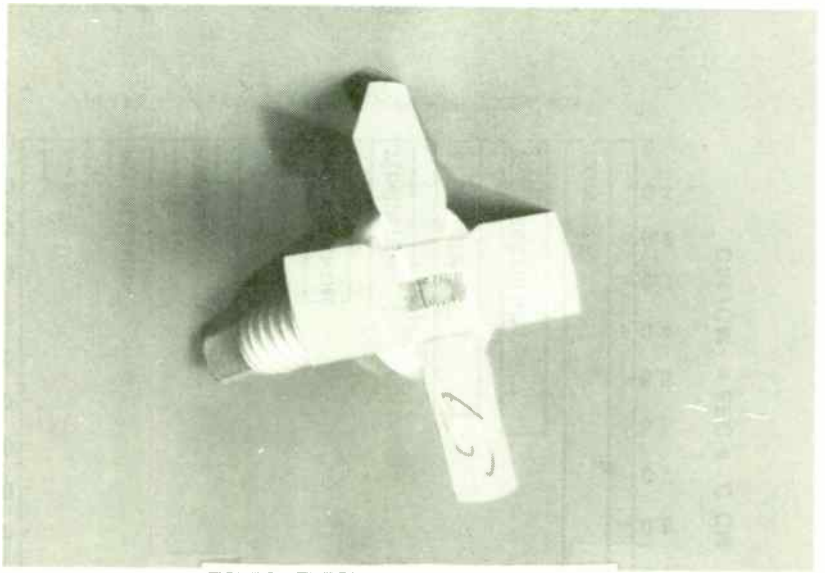


FIGURE 9–THE DUAL EMITTER BOND PACKAGE

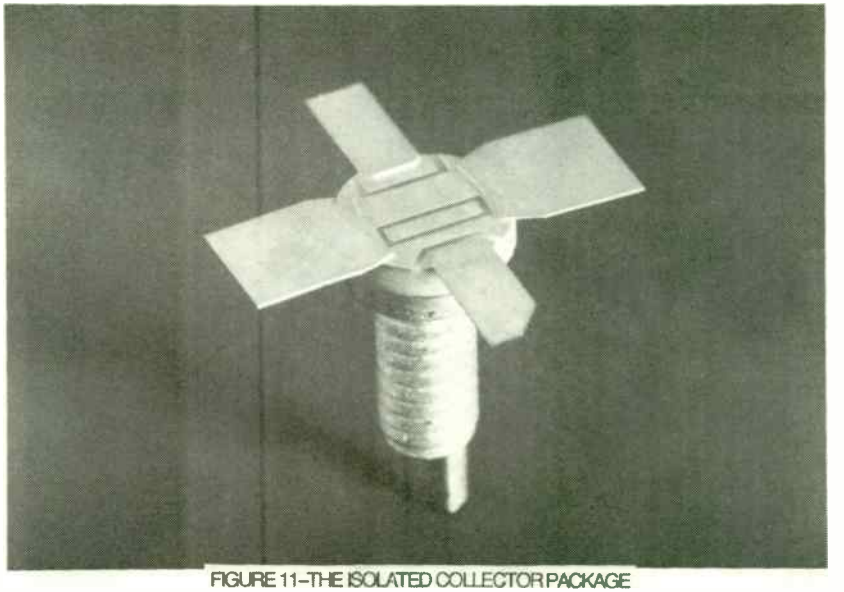
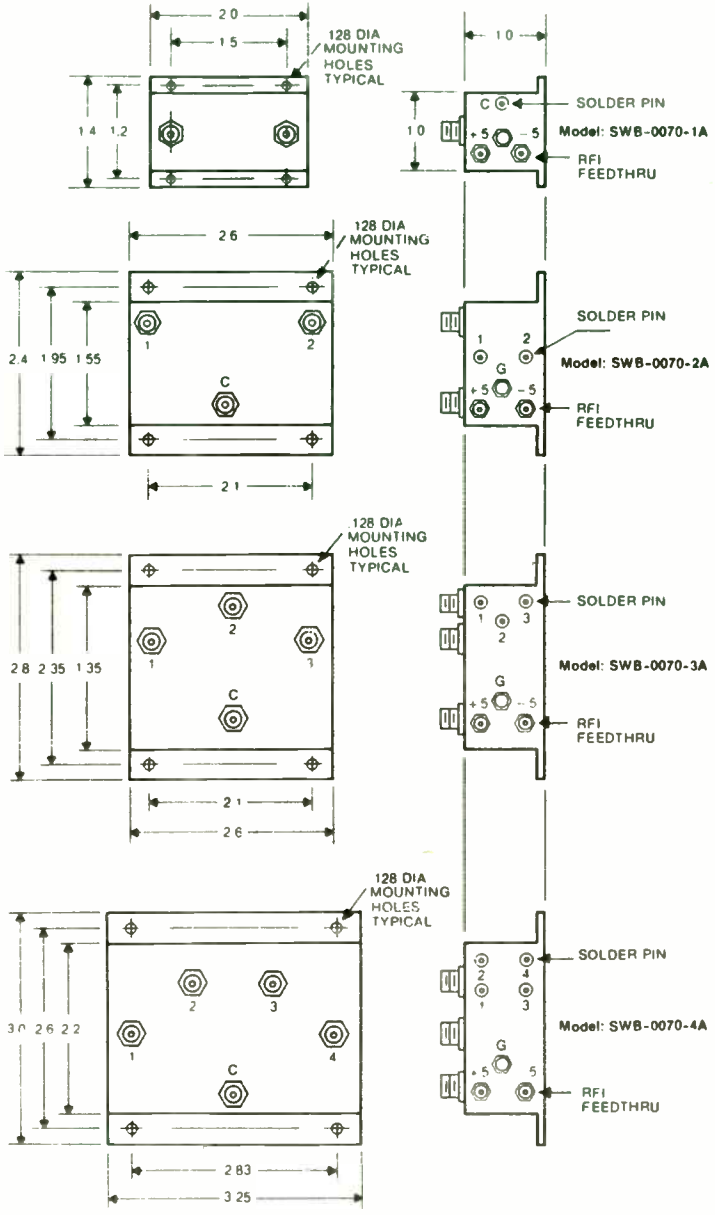


FIGURE 11–THE ISOLATED COLLECTOR PACKAGE

MECHANICAL DATA



14

AMERICAN MICROWAVE CORPORATION

SWITCH SPECIFICATIONS DATA SHEET

CUSTOMER:_____ MODEL:_____ OPT:_____

1.0 CONFIGURATION:

2.0 FREQUENCY BAND (GHZ):

3.0 INSERTION LOSS:

- 3.1) MAXIMUM:
- 3.2) VARIATION:

4.0 ISOLATION:

- 4.1) MINIMUM:
- 4.2) TYPICAL:

5.0 SWITCHING SPEED:

- 5.1) 50% TTL TO 90% RF
- 5.2) 50% TTL TO 10% RF
- 5.3) 10% RF TO 90% RF
- 5.4) 90% RF TO 10% RF

6.0 VSWR:

- 6.1) INPUT
- 6.2) OUTPUT (ON)
- 6.3) OUTPUT (OFF)

7.0 RF POWER:

- 7.1) CW
- 7.2) PEAK POWER
- 7.3) PULSE DUTY RATIO

8.0 CONTROL: NO DRIVER ☐
TTL DRIVER ☐
TTL DECODER ☐

9.0 POWER SUPPLY:

VOLTAGE	CURRENT (mA)
+5	
+15	
-5	
-15	

10.0 CONNECTORS:

- 10.1) RF: SMA N BNC TNC
- 10.2) POWER: MULTI-PIN SOLDER PIN
- 10.3) CONTROL: SOLDER PIN SMC SMA

11.0 INTERCEPT POINT:

- 11.1 3rd ORDER
  _____dBm @ _____dBm input power
- 11.2 2nd ORDER
  _____dBm @ _____dBm input power

12.0 VIDEO TRANSIENTS:

_____MV, MAX

13.0 PHASE TRACKING:

_____DEGREES MAXIMUM DEVIATION

FIGURE 15

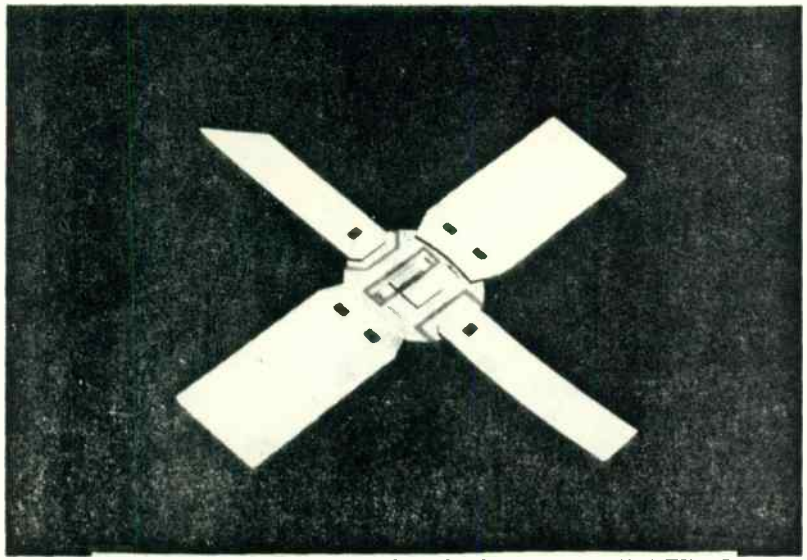


FIGURE 12–AN ISOLATED COLLECTOR PACKAGE WITH INTERNAL MATCHING

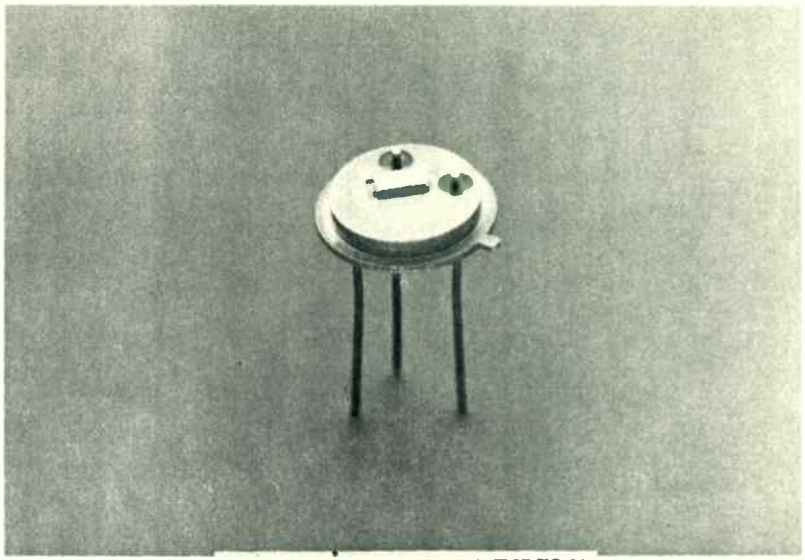


FIGURE 14–THE COMMON EMITTER TO-39

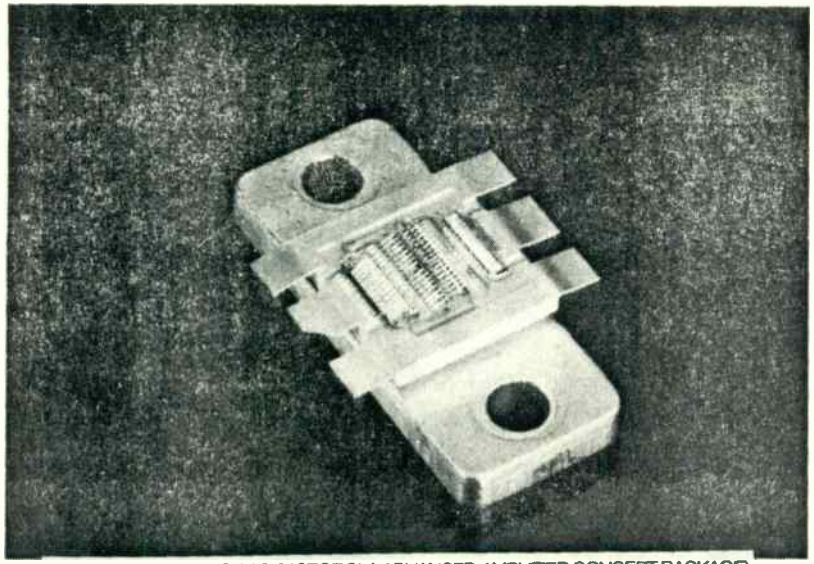


FIGURE 13–THE MAAC PAC (MOTOROLA ADVANCED AMPLIFIER CONCEPT PACKAGE)

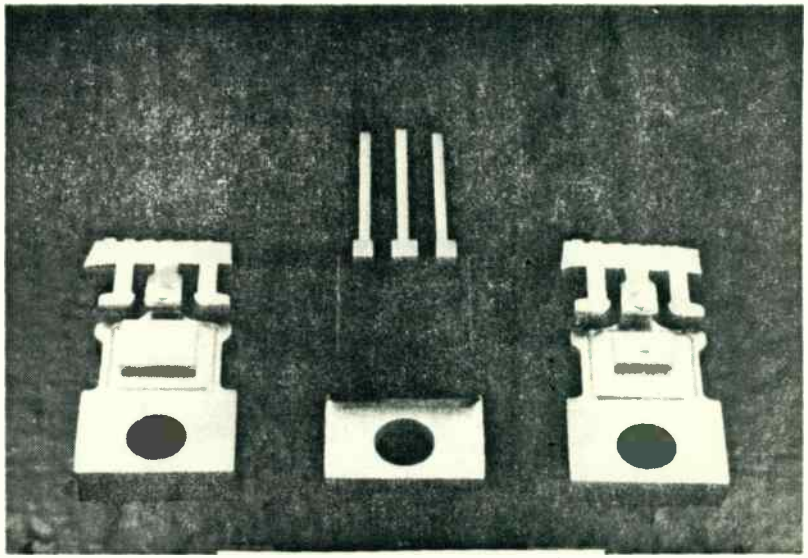


FIGURE 15–THE COMMON EMITTER TO-220

A Low Noise Fiber Optics Receiver/Amplifier in VHF Range

by
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P.O.Box 3409, Sunnyvale, Ca 94088-3409

Despite numerous advantages, the relatively high cost of fiber-optic transmission prevented its wide-spread industrial acceptance. High bandwidth-distance products, a prerequisite for cost-effectiveness, could not be achieved with relatively inexpensive components. The latest technological advances on both transmitter and receiver sides, however, are about to change that.

Transmitter

Starting at the transmitter side (Figure 1), the two major problems of the past were the unavailability of inexpensive, light emitting diode (LED) transmitters, capable of 10-20 MHz modulation rates, and the compounded problem of cost and reliability of laser diodes, required for large channel capacity, single mode, long-distance systems.

In examining the present status of the fiber-optic industry we observe, however, that new generations of LEDs, used in most *short-range*, multimode transmitters, can achieve wide modulation bandwidths, enabling system designers to develop cost-effective systems. For example, commercially available 820-850 nanometer AlGaAs surface emitting devices have significantly decreased in price and can be used up to and beyond 100 MHz (200 MBaud). InGaAsP LEDs can be used in the 1.3μm range. Their highly doped versions can be modulated up to bandwidths of several hundred MHz at the expense of lower output power.

InGaAsP laser diodes can go well beyond 1GHz. Their higher output power and an order of magnitude narrower spectral widths make these devices the ideal choice for *long-range*, very high data rate telecommunication systems.

Receiver

The key to cost effectiveness at the receiver side is the ability to offer monolithic IC building blocks that can match those high transmitter data rates with bandwidth, large dynamic range and low noise. These kinds of IC building blocks weren't readily available in the past. Consequently, system designers had to choose between limiting data rates to below 20 MBaud or using costly hybrid modules.

Signetics' solution to the problem is the introduction of the SE/NE5212 trans-impedance amplifier (TIA).

Although the real meaning is different, "trans-resistance" and "trans-impedance" are used interchangeably in practice. These names designate that these types of amplifers are current-driven at their inputs and generate voltage at their outputs. The transfer function is therefore a ratio of output voltage to input current with dimensions of ohms. Since the input is current driven, the input resistance must be low, which means low input voltage swings, no capacitive charge/discharge currents and wide frequency response with a generous phase margin.

Alternative approaches to the TIA, such as high input impedance FET preamplifiers vith a shunt input resistor, tend to be more bandwidth limited. They exhibit integrating characteristics, and therefore must be

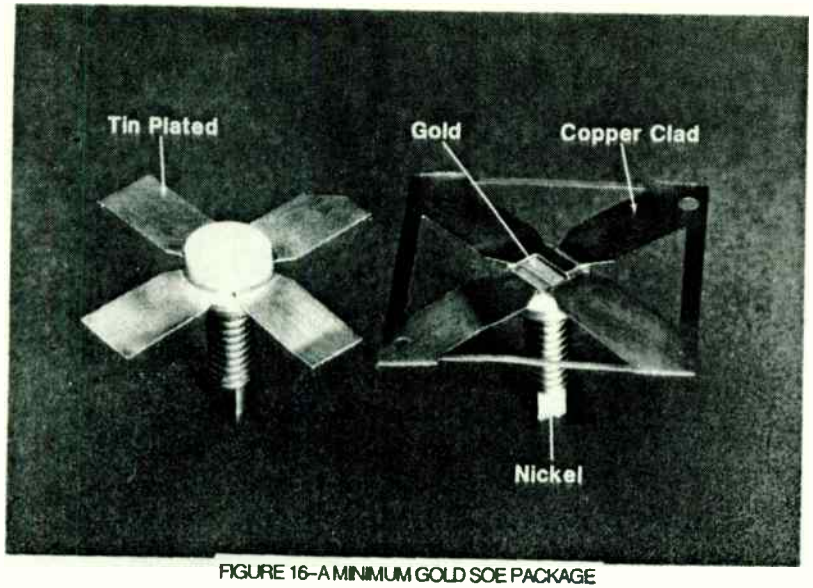

FIGURE 16–A MINIMUM GOLD SOE PACKAGE

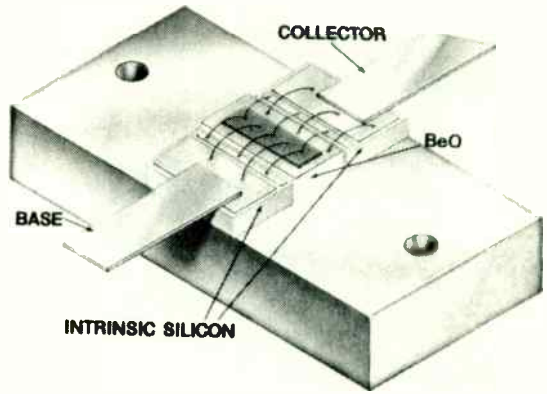

FIGURE 18–A NEW PACKAGE CONCEPT

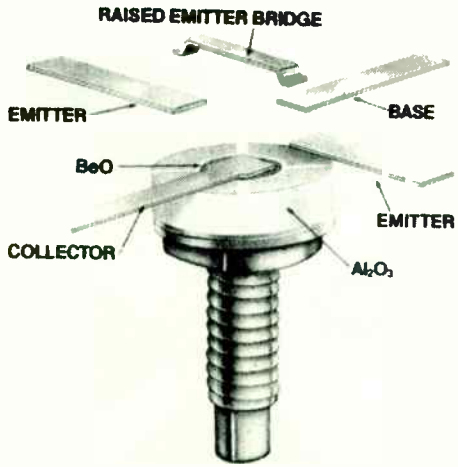

FIGURE 17–A MINIMUM BEO SOE PACKAGE CONCEPT

equalized by a differentiating second stage to achieve broad frequency response. The integrating input stage, however, is prone to overload with signals that have high low-frequency content. If the amplifier overloads for any reason, the integrated waveform cannot be restored by differentiation and dynamic range suffers despite the low noise characteristics.
Since the trans-impedance configuration does not have this problem, its superior dynamic range, inherently large bandwidth and compatibility with low cost IC technologies make it an attractive approach.

The NE5212

The NE5212 TIA is a low noise, wide band integrated circuit with single signal input and differential outputs, ideally suited for fiber optic receivers in addition to many other RF applications.
As shown in Figure 2, a differential output configuration was chosen to achieve good power supply rejection ratio and to provide ease of interface with ECL type post-amplifier circuitry. The input stage (A1) has a low noise shunt-series feedback configuration. The open loop gain of A1 (R_F=infinite) is about 70; therefore, we can assume with good approximation an input stage trans-resistance equal to the value of R_F=7.4 KOhms. Since the second stage differential amplifier (A2) and the output emitter followers (A3 and A4) have a voltage gain of about two, the input to output trans-resistance is twice the value of R_F, about 14.5 KOhms. The single-ended trans-resistance is half of this value.
Returning to the input stage (Figure 3), a simple analysis can be used to determine the performance of the TIA. The input resistance, R_{in}, can be calculated as

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{R_F}{1 + A_{VOL}} = \frac{7400}{1 + 70} = 104 \text{ Ohms}$$

More exact calculations lead to a slightly higher value of 110 Ohms.
The collector-base capacitance ($C_{\mu 1}$=0.12 pF) of Q1 is by far the largest contributor to the input capacitance due to the Miller-effect:

$$C_{in} = C_{\mu 1}(1 + 70) \approx 9 \text{ pF}$$

Thus, while neglecting driving source- and stray capacitances, C_{in} and R_{in} will form the dominant pole of the entire amplifier:

$$f_{-3dB} = \frac{1}{2\pi R_{in} C_{in}} = \frac{1}{2\pi R_F C_{\mu 1}} \qquad f_{-3dB} = \frac{1}{2\pi \, 7.4\times10^{3} \times 0.12\times10^{-12}} = 180 \text{ MHz}$$

Although significantly wider bandwidths could have been achieved by a cascode input stage configuration, the present solution has the advantage of a very uniform, highly de-sensitized frequency response because the Miller-effect dominates over external photodiode and stray capacitances. As an example, a relatively high source-capacitance of 4 pF would decrease the bandwidth by only about 30% . Consequently, the NE5212 will be relatively insensitive to PIN photodiode source capacitance variations. Since the dominant pole of the amplifier is at the input node, PIN diode source capacitance will not degrade phase margin.

Package parasitics

Package parasitics, particularly ground-lead inductances and parasitic

MICROSTRIP MINIATURE TRANSFER SWITCH

by

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ABSTRACT

A microstrip transfer PIN switch has been developed for the 675 MHz digital microwave system of Indian Telephone Industries Limited, Bangalore. It uses lumped elements to provide 90° electrical length between two diodes which is required to increase isolation. An isolation of more than 50 dB is obtained at two isolated ports in the 600 to 750 MHz frequency band with a minimum of 15 dB return loss at all the four ports. The maximum insertion loss obtained in the band is 0.8 dB. The switch is TTL compatible and has replaced the bulky, coaxial switch which used relays.

INTRODUCTION

Transfer switches are required to switch two transmission lines betaween the antenna and load Z_o. The configuration of a transfer switch using PIN diodes is shown in Fig.(1). When the control voltages V_{c1} and V_{c2} are positive and zero respectively, only the diodes D_1 and D_3 conduct and lines (1) and (2) get connected to the antenna and load Z_o respectively. When the control voltages V_{c1} and V_{c2} ae zero and positive respectively, only the diodes D_2 and D_4 conduct and line (1) gets connected to the load Z_o and line (2) gets connected to the antenna. First, a switch was developed with only one diode in each path and then a switch with two diodes in each path separated by an electrical length of 90° made of lumped elements was developed. The development of these switches will be discussed in the following sections.

Microstrip Transfer Switch with One Diode in Each Path:

The configuration of the microstrip transfer switch with one diode in each path is shown in Fig. (2). The switch was developed on 1/32" thick Teflon fiberglass substrate (ϵ_r=2.54) using HP 5082 - 3001 glass package PIN diodes. The high frequency chip capacitors were used for DC blocking. Air-core coil inductors were used for RF to DC isolation. The measured performance of the switch is shown in Fig. (3). The minimum return loss obtained is 22.0 dB. The isolation at port No.3 has decreased from 29.0 dB to 26.5 dB over the 600 to 750 MHz frequency band. The minimum isolation obtained at port No.4 is 34.5 dB. The isolation at port No. 3 is about 6 dB less than that of the isolation at port No.4. This is because the two signals add in phase at port No.3. The maximum insertion loss obtained is 0.5 dB.

Microstrip Transfer Switch with Two Diodes in Each Path:

The isolation is expected to increase when two similar

capacitances, can significantly degrade frequency response. To minimize parasitics, the NE5212 is offered in a 14-pin as well as an 8-pin package. The 14-pin version uses multiple grounds to minimize ground wire-bond inductances and leaves pins adjacent to the input unconnected. This will minimize parasitic capacitance and feedback from the outputs. Since the 8-pin version cannot afford all these techniques, its frequency response is inevitably compromised.

While the surface mount SO-14 version has a typical bandwidth of 150 MHz, the SO-8 version achieves 125 MHz. The difference in bandwidth can be utilized advantageously by choosing the appropriate package type and bandwidth as dictated by a particular system requirement.

Further bandwidth modifications can be achieved by a small capacitance between input and output or input and ground. Since the NE5212 has differential outputs, both peaking and attenuating type frequency response shaping are possible.

Fighting noise

Since most currently installed and planned fiber optic systems use non-coherent transmission and detect incident optical power, receiver noise performance becomes important. The SE/NE5212 goes a long way towards solving this problem. Its input stage configuration achieves a respectably low input referred noise current spectral density of 3 pA/$\sqrt{Hz}$, measured at 10 MHz. This low value is nearly flat over the entire bandwidth. The trans-resistance configuration assures that the external high value bias resistors, often required for photodiode biasing, will not contribute to total system noise. As shown in the following equation [1], the equivalent input RMS noise current is determined by the quiescent operating point of Q_1, the feedback resistor, R_F, and the bandwidth, Δf, however, it is not dependent on the internal Miller-capacitance. The noise current equation is then

$$\overline{i_{eq}^2} = 4kT\frac{\Delta f}{R_F} + 2qI_{BQ1}\Delta f + 2qI_{CQ1}\frac{1}{g_{mQ1}^2}\omega^2(C_s+C_{\pi 1})^2\Delta f + 4kT\, r_{bQ1}\,\omega^2 C_s^2\Delta f$$

Using design values of I_{CQ1}=0.5 mA, R_F=7.4kOhms, β=50 and Δf=100 MHz, the frequency independent term yields 25 nA_{RMS} noise. Design values for the frequency-dependent term are: C_s=1.3 pF, $C_{\pi 1}$=0.7pF and r_{bQ1}=170 Ohms. The measured integrated noise was 33 nA.

Testing the NE5212

Connecting the NE5212 in an actual fiber optic pre-amplifier configuration, dynamic range, transient response, noise and overload recovery tests are easily measured (Figure 4) . In order to replicate actual parasitic capacitances, effects of the photodiode bias network and circuit layout effects, the test circuit should closely resemble the real application conditions. If the intention is to use the device in die form, then the actual hybrid circuit mounting techniques should be used while testing.

In the test circuit shown, an 850 nm modulated laser light source feeds an HP-HFBR2202 PIN photodiode which is mounted in close proximity to the NE5212 input. The R-C filter in series with the photodiode eliminates

diodes separated by a quarterwave transmission line are used in each path instead of one diode. At the frequency at which the electrical length between the diodes is exactly 90^{o}, the isolation will be double that offered by a single diode. The dimensions of the switch become too large if the distributed quarterwave lines are used because the length of a quarter wave line on 1/32" thick Teflon fiberglass (ϵ_r=2.54) is approx. 7.5 cm. The equivalent T- or π - section lumped element networks are very convenient in such applications.

The element values of the T-equivalent lumped circuit calculated using the equations:

$$f_o = \frac{1}{2\pi\sqrt{LC}} \quad , \quad Z_o = \sqrt{\frac{L}{C}}$$

where f_o = 675 MHz, Z_o = 50 Ω

are L = 11.789 nH, C = 4.715 pF

The air-core coil inductors were characterized by making them resonate in series with the chip capacitors. Johanson thin film variable capacitors were used as shunt capacitors. These capacitors were tuned so that a T-equivalent network consisting of L's and C offered a 90^{o} electrical length at 675 MHz. The electrical lengths measured at the band edges (at 600 and 750 MHz) are approximately 77^{o} and 105^{o}. The switch circuit is shown in Fig. (4). A photograph of the unit is shown in Fig.(6).

The measured performance of the switch is shown in Fig.(5). It can be seen that a minimum return loss of 15 dB is obtained over the required frequency band and is maximum ($\simeq$ 32 dB) around 700 MHz. The minimum isolation obtained is 50 dB. The maximum insertion loss is 0.8 dB. Almost similar results were obtained when the ports (2), (3) and (4) were taken as input ports. The increase in the insertion loss from 0.5 dB to 0.8 dB in the frequency band can be attributed to the lead inductances of the diodes. The computed results obtained taking the forward diode resistance as 1 ohm and the reverse junction capacitance as 0.2 pF are as follows: The return loss is more than 17 dB and isolation is more than 50 dB.

The microstrip transfer PIN switch with lumped elements has given good results over a frequency bandwidth of 22% (600 to 750 MHz). The switch being a planar circuit can be easily integrated with other subsystems.

ACKNOWLEDGEMENT

The authors wish to record their thanks to management of M/S Indian Telephone Industries Limited, Bangalore for kind permission to publish this paper.

possible disturbances from the power supply. Both differential outputs are AC coupled through 33 Ohm resistors in order to match to the 50 Ohm test system. In most applications these matching resistors are unnecessary. Performance evaluation in the linear region, including amplitude and phase response and power supply rejection can be accomplished by a network analyzer and S parameter test set (Figure 5). The simple equations given in the figure for the calculation of trans-resistance, R_T , are accurate for $R \gg R_{in}$, where R_{in} is the input resistance of the NE5212.

General purpose RF applications.

Besides the main fiber-optic receiver applications, many other interesting possibilities exist for the the NE5212. Simplicity and ease-of-use are the prevailing characteristics of this device. For instance, amplifiers with 20 dB gain can be built requiring only one external gain setting resistor (Figure 6). The voltage gain of the differential configuration with no load at the outputs can be calculated as follows:

$$v_{out} = i_{in} \times R_T = \frac{v_{in}}{R_s + R + R_{in}} R_T \quad \text{and} \quad A_v = \frac{v_{out}}{v_{in}} = \frac{R_T}{R_s + R + R_{in}}$$

where Rs is the signal-source resistance, R is the external gain setting resistor and R_{in} is the input resistance of the NE5212. Substituting the actual values:

$$A_v = \frac{14000}{R_s + R + 110}$$

where all values are in Ohms. The graph of Figure 6 is an experimental verification of this formula in a single-ended, 50 Ohm system, using the test configuration of Figure 5. Note the 6 dB loss due to the single-ended configuration and another 6dB due to the 50 Ohm load.

As in all other RF applications, attention to power supply bypassing, clean grounds, and minimization of input stray capacitances is required for optimum performance.

Another useful application of the NE212 is as a voltage controlled amplifier, using a DMOS FET device biased into the linear region (Figure 7). An operational amplifier with supply-to-ground output swing and supply-to-ground input common mode range (such as the Signetics NE5230) can provide adequate gate control voltage even with a single 5V power supply. This type of circuit can have 25dB AGC range at 50 MHz and 45dB at 10MHz with less than 1% harmonic content. AGC range is determined by the ON-resistance range of the FET and capacitive drain to source feedthrough. If lowest RF feedthrough were required, the FET should be used in a shunt configuration rather than in a series.

Turning towards an entirely different area of application, where contrary to the NE5212s' capabilities, poor phase margins are mandatory, a simple crystal oscillator with buffered output can be built using a minimum number of external components (Figure 8). The feedback signal is taken from the non-inverting output, while the inverting output provides a low impedance (15 Ohm) output drive. The crystal operates in its series resonance mode. Figure 9 shows a varactor tuned version with a large tuning range. In Figure 10 the circuit has been optimized for stability at the expense of tuning range.

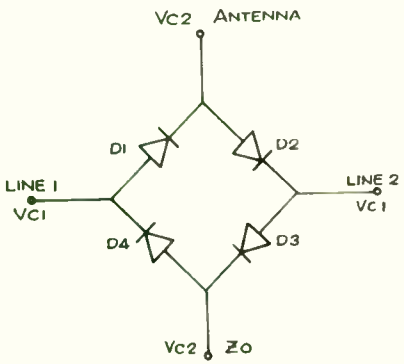


FIG. 1. TRANSFER SWITCH

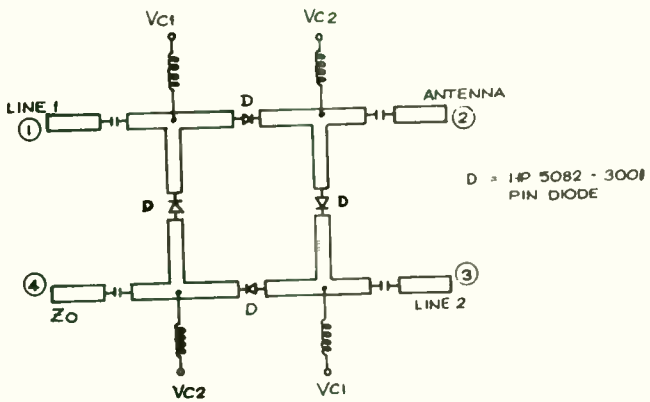
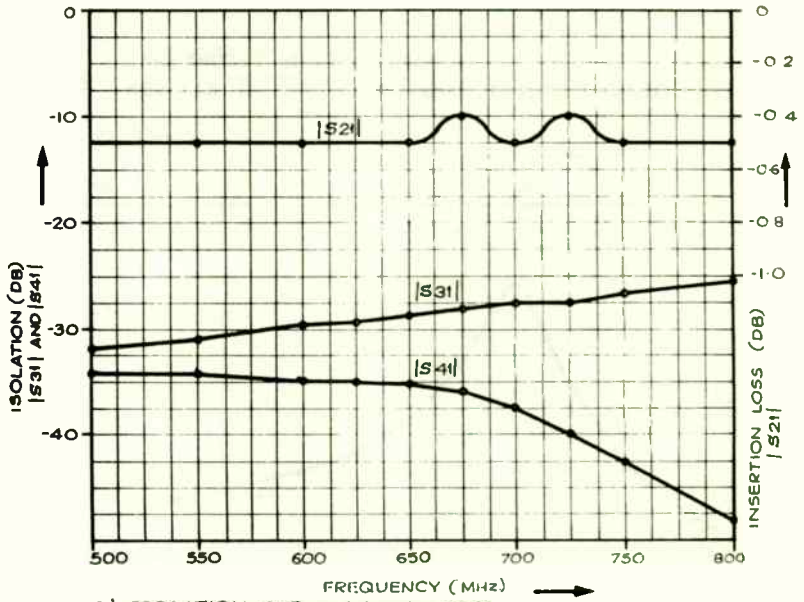
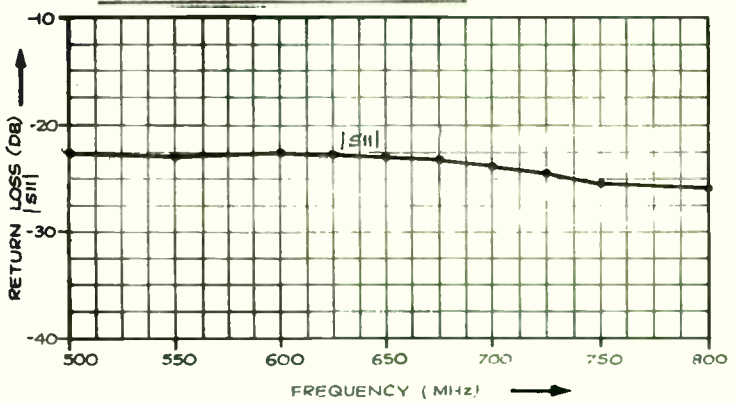


FIG. 2. MICROSTRIP TRANSFER SWITCH WITH ONE DIODE IN EACH PATH



a) ISOLATION AND INSERTION LOSS



b) RETURN LOSS

FIG. 3. RESULTS OF THE MICROSTRIP TRANSFER SWITCH WITH ONE DIODE IN EACH PATH.

In RF amplifier applications it is often desirable to limit the amplifier bandwidth in order to minimize noise and RFI. The 100-150 MHz bandwidth of the NE5212 can be easily modified by connecting a capacitor to the input pin. The device bandwidth then becomes

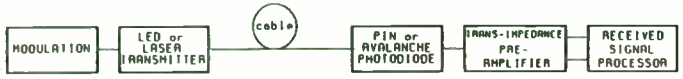
$$f_{-3dB} = \frac{1}{2\pi R_{in} (C_{in}+C_{EXT})}$$

where R_{in} is the input resistance, C_{in} is the input capacitance as specified in the data sheet and C_{EXT} is the external capacitance. For example, a C_{EXT}=33 pF will reduce the amplifier bandwidth to 42 MHz with a single pole roll-off. The transfer curve is shown in Figure 11. Single-ended to differential conversion is another useful application for the device. Impedance matching is easily accomplished by resistors connected in series with the outputs.

The NE5212 was designed using an advanced oxide-isolated bipolar process. This technology advantageously combines the required characteristics of low noise, large bandwidth, and relatively low cost, due to its high density. The under $2.00 quantity-price of the device, coupled with the capability of up to 300 MBaud data rates will lead to further cost-reduction of fiber-optic receivers. Due to its versatility, many non-fiber optic applications are also possible.

Reference:

[1] Robert. G. Meyer, Robert. A. Blauschild: "A Wide-Band Low-Noise Monolithic Transimpedance Amplifier." IEEE Journal of Solid-State Circuits, Vol. SC-21 No 4, pp 530-533, Aug. 1986.



Fiber optic transmission system, using trans-resistance pre-amplifier.

Figure 1

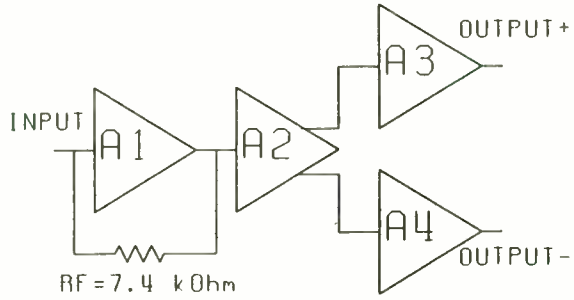
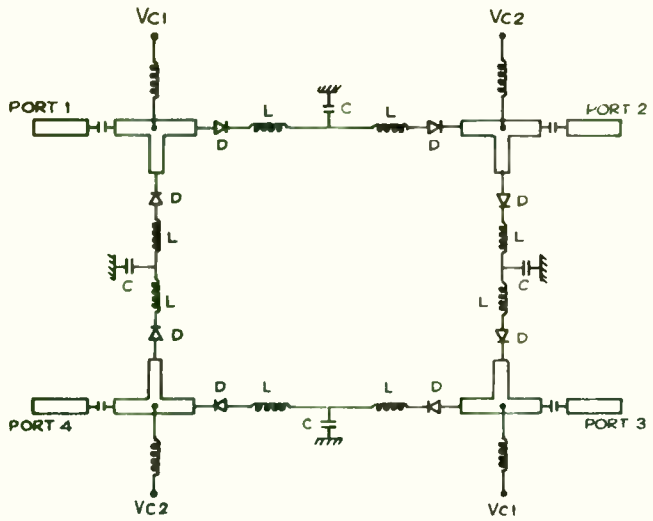


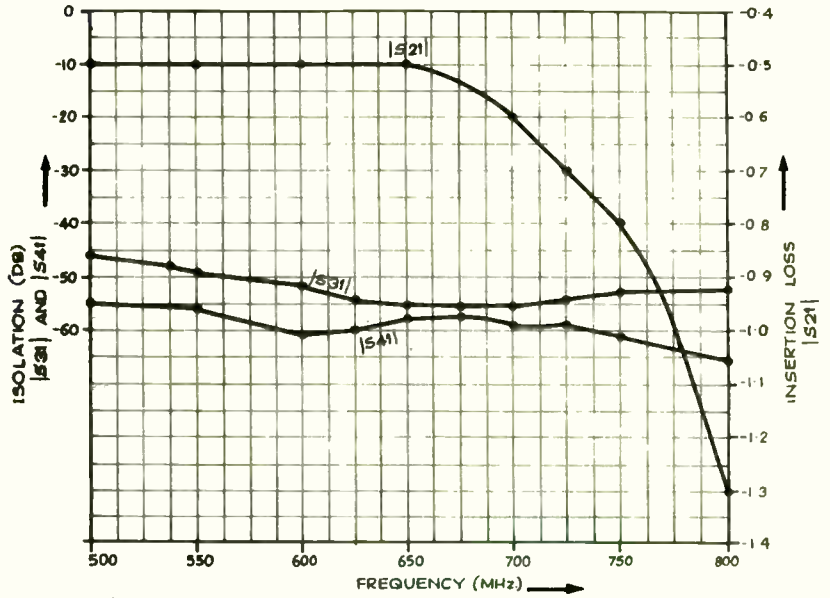
Figure 2.

NE5212 block diagram showing the trans-resistance pre-amplifier with the internal feedback resistor and the buffered differential outputs.



L = 11.79 nH
C = 4.715 PF
D = HP 5082 - 3001
PIN DIODE

FIG. 4. MICROSTRIP TRANSFER SWITCH WITH TWO DIODES IN EACH PATH



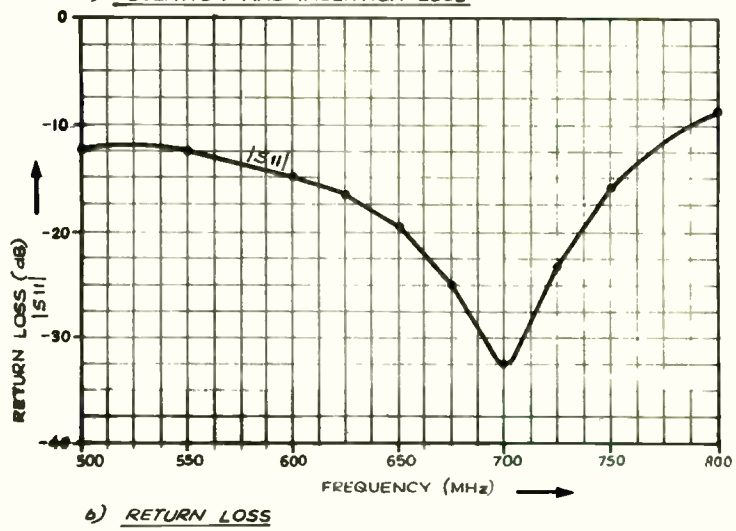
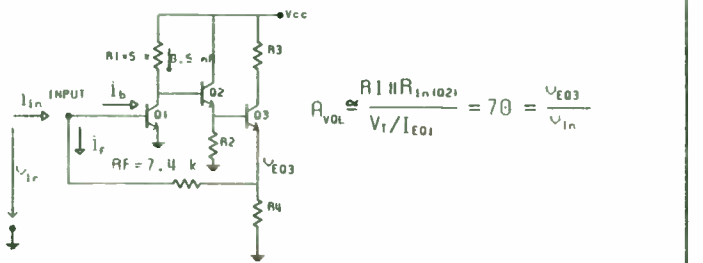
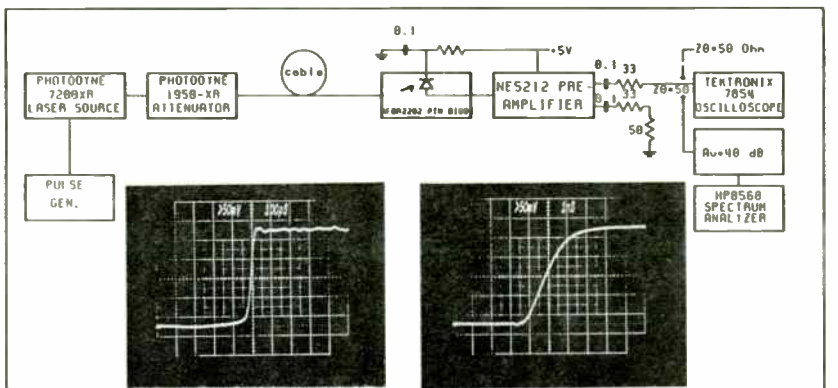


FIG. 5. RESULTS OF THE MICROSTRIP TRANSFER SWITCH WITH TWO DIODES IN EACH PATH.



This simple shunt-series input stage has some hidden features besides its very low noise. Due to the Miller-effect, the collector- base capacitance of Q1, multiplied by a voltage gain of 70, forms the dominant pole with RF, while desensitizing frequency response to source capacitance variations.

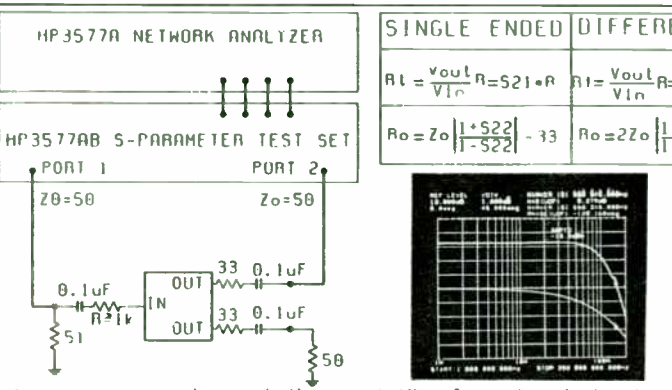
Figure 3.



a. Stimulus b. Response

Figure 4.

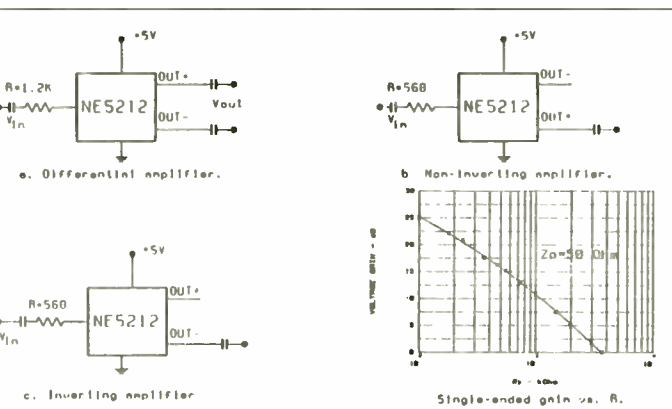
Dynamic range, impulse response and noise test circuit.



SINGLE ENDED	DIFFERENTIAL
$Rt = \frac{Vout}{Vin} R = S21 \cdot R$	$Rt = \frac{Vout}{Vin} R = 2 \cdot S21 \cdot R$
$Ro = Zo \left\lvert \frac{1+S22}{1-S22} \right\rvert - 33$	$Ro = 2Zo \left\lvert \frac{1+S22}{1-S22} \right\rvert - 66$

The frequency response can be conveniently measured with an S-parameter network analyzer. The 1 kOhm input resistor acts as a voltage to current converter and the resistors at the output do the impedence matching. The curves show a smooth, wide band response with ample phase margin. Trans-resistance and output resistance can be calculated from the S-parameters as shown in the table.

Figure 5.



A 150 MHz, 20 dB amplifier requires only one external gain setting resistor. Differential or single ended operation with or without inversion is possible.

Figure 6.

MATHEMATICS OF THE LINVILL STABILITY CRITERIA

by

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For the power transistor, the 'Y' parameters at various frequencies are known. The device input admittance and the output admittance are complex. The transistor may not be stable at some frequencies or loadings. The RF designer is interested in finding circuitry and loading which will produce stability. He looks first at the output. Finding this he then determines the input network. For the mathematics to be used the following circuit model will be used.

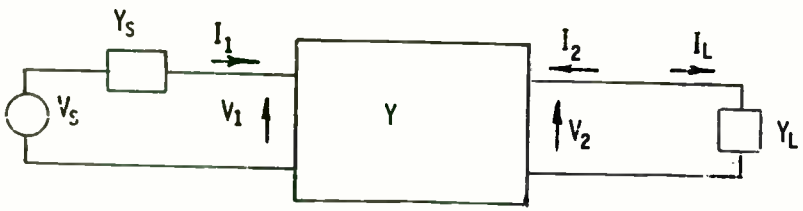


Figure 1, 'Y' Parameter Transistor Circuit

A technique the designer may use to select the the output circuit is the mathematics of Linvill. The output power from the device is described by a parabaloid of revolution. The power input to the device is described by an inclined surface, the input power plane. This inclined plane intersects the parabaloid of revolution. The slope and angles of orientation are dependent upon both device parameters and the output loading.

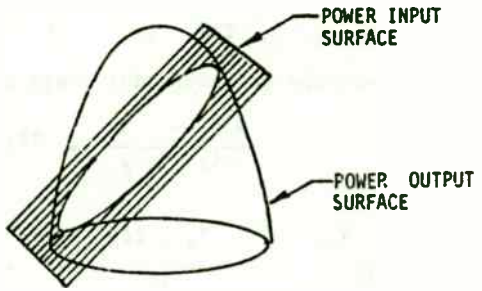
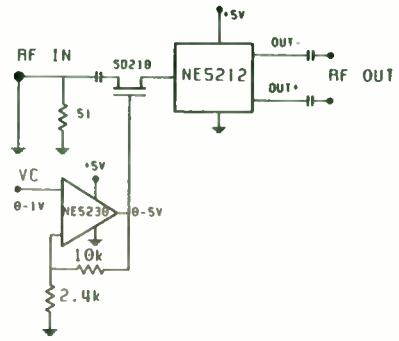


Figure 2, Power Input and Output Surfaces

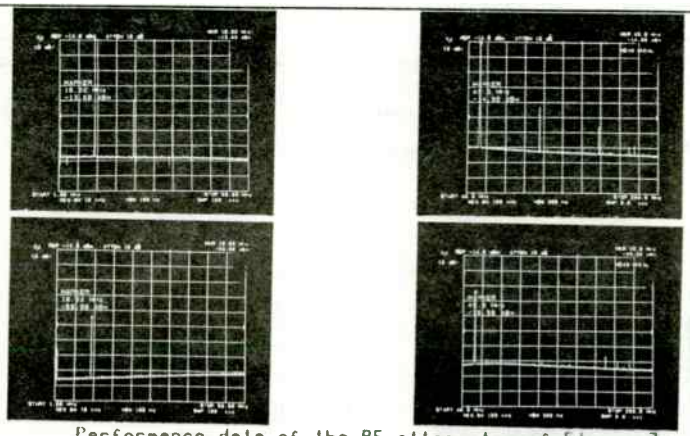
The parabolic power surface of revolution rests on the LM plane. This LM plane is a Smith chart rotated 180 degrees. The axis of the paraboloid of revolution is perpendicular to the LM plane. The intersection of the LM plane and the paraboloid is a circle of unit radius.

The center of the circle is at L=1 and M=0. Recapping, P_o and P_{in} is represented in a three-dimensional coordinate system whose axes are L, M, and P (power). The LM plane represents the zero power output reference.



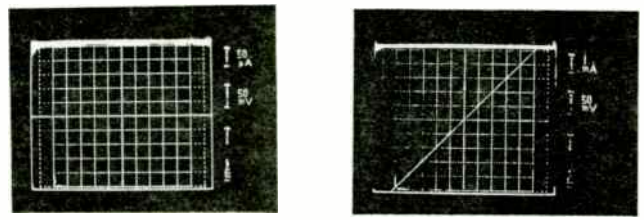
This variable gain RF amplifier has less than 1% distortion, 25 dB range at 50 MHz and 45 dB range at 10 MHz, with a 0-1 V control signal.

Figure 7



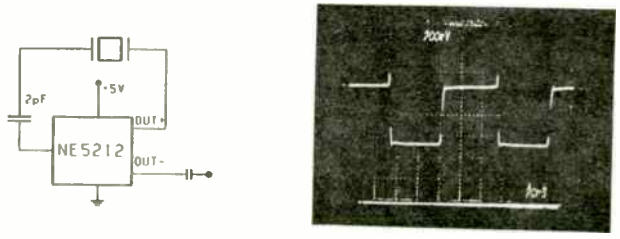
Performance data of the RF attenuator of Figure 7.

Figure 7a



FET resistance in its linear region at Vgs=0V (left) and at Vgs=5V (right).

Figure 7b



This 16 MHz crystal oscillator has minimum component count and operates in the series resonant mode. Output- provides independent 50 Ohm drive capability.

Figure 8

$$P_o = R_e \ (V_2 \ I_L^*)$$

$$P_o = \frac{L \ |Y_{21}|^2}{2 \ R_e \ Y_{22}} - \frac{(L^2 + M^2) \ |Y_{21}|^2}{4 \ R_e \ Y_{22}}$$

From the above equation the power is also zero if L = 2 and M = 0; or if L = 1 and M = 1. And also is if L = 1 and M = 1; and is if L = 1 and M = -1. The result of the intersection of the paraboloid and the LM plane is a circle of unit radius in the LM plane. The center of the circle is at L = 1, M = 0.

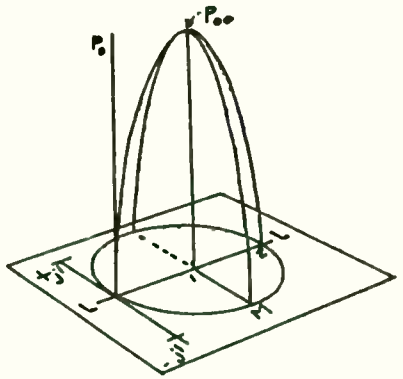


Figure 3, Sketch of Power Output as a Function of L and M.

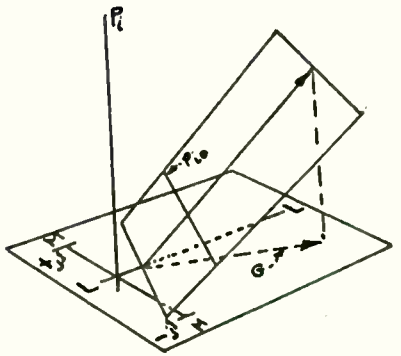


Figure 4, Sketch of Power Input as a Function of L and M.

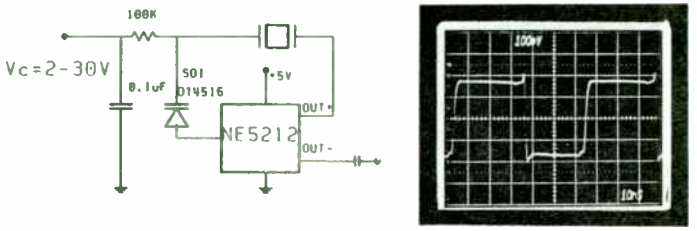
Consider a property of the LM plane following from the fact,

$$V_2 = - \frac{Y_{21}}{Y_{22} + Y_L} = - \frac{Y_{21}}{2R_e \ Y_{22}} (L + jM)$$

and

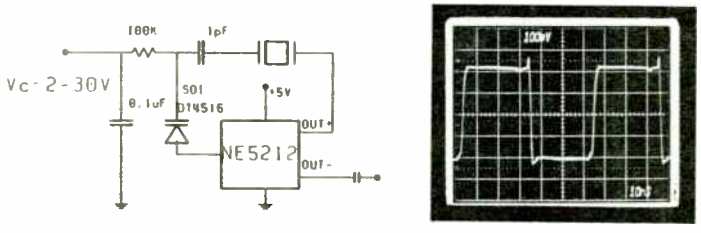
$$Y_L + y_{22} = \frac{2 \ R_e \ Y_{22}}{L + j \ M}$$

Any point in the LM plane represents an admittance whose value is related to $Y_L + y_{22}$. If y_{22} of the active device is known then the load admittance Y_L can be calculated. The expression for $Y_L + y_{22}$ can be rationalized to give real and imaginary parts. Using the Smith chart overlay, it should be remembered that any immittance chosen from it is a sum, L_L and y_{22}. In finding Y_L values, a conversion from the readings taken from the Smith chart must be done.



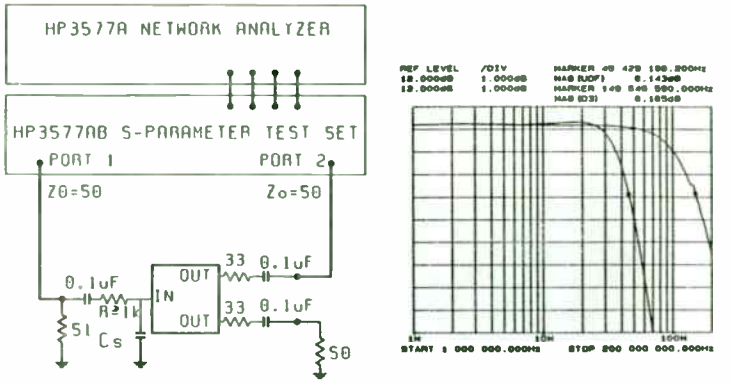
Varactor tuned crystal oscillator with 0.28% tuning range

Figure 9.



Varactor tuned oscillator with 1 ppm/V supply sensitivity.

Figure 10.



Setting bandwidth with shunt input capacitor, Cs.

Figure 11.

CONDUCTANCE READ FROM THE SMITH CHART

$$g_c = \frac{\mathrm{Re}\ (Y_L)}{g_{22}}$$

SUSCEPTANCE READ FROM THE SMITH CHART

$$b_c = \frac{\pm\ \mathrm{Im}\ (Y_L)}{g_{22}}$$

These results will be used later after the Linvill charts are plotted.

The following are equations that will be used to prepare the Linvill chart.

GRADIENT LINE ANGLE, θ

$$\theta = \tan^{-1} \frac{I_m\ (y_{12}\, y_{21})}{-R_e\ (y_{12}\, y_{21})}$$

STABILITY FACTOR, C

(Less than one, unconditionally stable)

$$C = \frac{\left| y_{12}\ \ y_{21} \right|}{2\, g_{11}\, g_{22} - R_e\ (y_{12}\, y_{21})}$$

GAIN AT MAXIMUM POWER OUTPUT, G_{oo}

$$G_{oo} = \frac{C}{2} \left| \frac{y_{21}}{y_{12}} \right| \quad (\text{In dB} = 10 \log G_{oo})$$

MAXIMUM GAIN, G_{MAX}

(Available power gain)

$$G_{MAX} = K_g\, G_{oo}$$

$$K_g = 2 \left[\frac{1 - \sqrt{1 - C^2}}{C^2} \right]$$

GAIN CIRCLE DATA

GAIN RATIO

$$g = \frac{G}{G_{oo}}$$

DISTANCE TO CENTER OF GAIN CIRCLE, FROM LINVILL CHART CENTER, ALONG GRADIENT LINE

$$d = -g\, \frac{C}{2}$$

RADIUS OF GAIN CIRCLE

(Radius of Linvill chart is unity)

$$r = \sqrt{1 - g + \frac{C_g^{\,2}}{2}}$$

A Thermally Tuned VCO

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Electronic tuning of an oscillator is almost universally accomplished with a varactor diode. There are, however, some applications where the use of the varactor poses some problems. One such example is a high power oscillator where the high voltage present in the oscillator tuned circuit causes either conduction of the diodes or diode breakdown. Likewise, a pulsed oscillator using a varactor diode can cause a transient frequency shift at turn-on. A high power or pulsed oscillator frequency can be controlled using heated ceramic capacitors without the problems of a varactor diode.

Figure 1 shows an oscillator using a pair of temperature-compensating ceramic capacitors heated with a resistor for frequency control. Although the example circuit operates at a relatively low power level, the technique can be adapted to oscillators of practically any power level. For the demonstration circuit, two common N750 ceramic disc capacitors were used. The dipped insulation was removed from the capacitors using a file and a ceramic-based resistor was sandwiched between the two capacitors. Thermal heat sink compound was used to insure good thermal contact between the resistor and capacitors. The ceramic resistor was used because of the relatively high power dissipation of this resistor for its small size. A good source of flat ceramic resistors is the DIP or SIP resistance pack where all of the resistors can be placed in parallel.

Figure 2 shows the frequency-voltage and the frequency-time characteristics of the test oscillator. As suspected, the oscillator shows a significant time delay between the applied control voltage and the frequency change. This limits the applications for such an oscillator and precludes any applications requiring rapid frequency correction. An oscillator of this sort would be suited for the control of industrial heating equipment, where frequency control is necessary because of FCC requirements, but tolerances are loose. Another application is for radar transponders where a high power oscillator is pulsed but the frequency control is loose (0.3%).

One of the significant disadvantages of the demonstration thermally-tuned oscillator is the use of a capacitor with a high temperature coefficient. Unless the temperature coefficient exactly compensates for the temperature variation of the oscillator inductor, the oscillator will be unstable with ambient temperature. Of course, the oscillator is to be used in an electronically stabilized system and the temperature instabilities will be corrected. However, the inherent instabilities subtract from the possible tuning range of the system. To achieve nominal operating frequency the capacitor must be adjusted to a temperature equal to or higher than the highest desired ambient temperature. This is not an impossible situlation, as it is often done in crystal ovens and temperature stabilized voltage references.

CALCULATOR PROGRAM, HP 15c Linvill Gradient Line Angle. O and Stability Factor, C

REG	VALUE	TRIAL NUMBERS
1	g_{11}	17.2
2	b_{11}	11.6
3	g_{12}	0
4	b_{12}	-0.64
5	g_{21}	32.2
6	b_{21}	-63.1
7	g_{22}	0.27
8	b_{22}	1.89
9	g_{result}	-40.38
.0	b_{result}	-20.6
.1	$y_{12}y_{21}$	45.338
.2	0	-27.03
.3	C	0.9127

LINE	KEYCODE	KEYS	VALUE
001	42,21,11	f LBL A	
002	45 3	RCL 3	g_{12}
003	45 4	RCL 4	b_{12}
004	42 25	f I	y_{12}
005	45 5	RCL 5	g_{21}
006	45 6	RCL 6	b_{21}
007	42 25	f I	y_{21}
008	20	X	$y_{12}y_{21}$

Gradient Line Angle and Stability Factor Program, continued

LINE	KEYCODE	KEYS	VALUE
009	44 9	STO 9	STORE g_r
010	42 30	f Re≷Im	
011	44 .0	STO .0	STORE b_r
012	42 30	f Re≷Im	
013	43 1	g →P	$\|y_{12}\ y_{21}\|$
014	44 .1	STO .1	
015	43, 5, 8	g CF 8	CLEAR COMPLEX MODE
016	45 .0	RCL .0	Im ($y_{12}\ y_{21}$)
017	45 9	RCL 9	Re ($y_{12}\ y_{21}$)
018	- 16	CHS	-Re ($y_{12}\ y_{21}$)
019	10	÷	Im ($y_{12}\ y_{21}$)/-Re ($y_{12}\ y_{21}$)
020	43 25	g $\tan^{-1}$	$\tan^{-1}$(Re($y_{12}\ y_{21}$)/-Re($y_{12}\ y_{21}$))
021	44 .2	STO .2	ϕ
022	2	2	2
023	45 1	RCL 1	g_{11}
024	20	X	$2g_{11}$
025	45 7	RCL 7	g_{22}
026	20	X	$2g_{11}\ g_{22}$
027	45 9	RCL 9	Re ($y_{12}\ y_{21}$)
028	30	-	$2\ g_{11}\ g_{22}$ - Re ($y_{12}\ y_{21}$)
029	45 .1	RCL .1	$\|y_{12}\ y_{21}\|$
030	34	X≷Y	$2g_{11}\ g_{22}$ - Re ($y_{12}\ y_{21}$)
031	10	÷	$\|y_{12}\ y_{21}\|$/ (2 $g_{11}\ g_{22}$ - Re ($y_{12}y_{21}$))
032	44 .3	STO .3	C
033		g RTN	PROGRAM END

As an example, if the capacitor were operated at a nominal temperature of 85 C for a maximum ambient of 70 C, the maximum temperature variation would be 15 degrees negative and as much positive variation as the components would allow. For maximum frequency variation, the nominal operating temperature of the controlled capacitor would be midway between the maximum temperature that the heated capacitor would allow and the highest ambient temperature expected. The significant disadvantage of this is that there would be a "warm up" period in order to bring the temperature of the heated capacitor to the operating point. In the case of the demonstration oscillator, standard off-the-shelf components were used which were relatively large and had a significant thermal inertia. Small geometry ceramic capacitors with integral heating elements could be fabricated to reduce the thermal inertia and improve the thermal coupling to reduce this problem to an acceptable level.

A solution to the warm-up problem is shown in Figure 3. In this example the oscillator tuned circuit is resonated with two capacitors. The capacitors have identical values and equal but opposite temperature coefficients. Therefore, the combination of the two temperature coefficients would theoretically be equal to zero.

In this example, each capacitor would be individually heated, allowing the oscillator frequency to be increased by heating the negative coefficient capacitor or lowered by heating the positive coefficient capacitor.

Two advantages are available from this arrangement. First, the oscillator will be more ambient-stable as previously explained. Secondly, the tuning range of the oscillator would be twice that obtained with a single capacitor, as each capacitor could be heated from the ambient to the maximum temperature the capacitor would allow. In addition, the capacitors do not need to be preheated to a temperature above the ambient and thus there would be a saving of power. Since one capacitor would provide an upward variation of frequency while the second capacitor would provide a similar downward frequency variation, the total variation is twice what a single capacitor would supply.

From a practical standpoint, positive temperature capacitors are rare. A quick check of major capacitor manufacturer's literature indicated that only P100 temperature coefficient capacitors were available. In addition, there was no standard corresponding negative coefficient, the closest being N080 or N150. A parallel combination of equal P100 and N150, for example, will produce an equivalent temperature coefficient of N50. Since most inductors require a negative temperature coefficient capacitor for temperature stabilization, this was not considered as a significant deterrent.

The significant problem was the fact that the largest positive temperature coefficient of off-the-shelf capacitors was only 100 PPM/C. For many applications, much larger coefficients would be desired. One manufacturer of ceramic capacitors was contacted to determine the range of positive temperature coeffi-

The preceding complex arithmetic program calculates both the stability factor and the gradient line angle by the Linvill technique. The HP 15c has two parallel stacks for number manipulation. The first parallel stack contains the real part of the complex number; the second stack contains the imaginary part of the complex number. Once the complex numbers are loaded into the stack, the complex arithmetic follows as if you were carrying out ordinary arithmetic operations.

Between lines 002 and 007 the parameters for y_{12} and y_{21} are loaded into the stack. The complex product $y_{12}\ y_{21}$ is taken at line 008. The real and imaginary parts of this product are stored in registers 9 and .0 The real and imaginary parts of $y_{12}\ y_{21}$ are recalled, divided, and the gradient line angle, θ calculated. This is at lines 016 through 020. The factors for the calculation of the stability factor, C are recalled and operated on. This is in lines 022 through 031. Finally the result, C is stored in register .3

CALCULATOR PROGRAM FOR THE GAIN AT MAXIMUM POWER OUTPUT, P_{oo}

This program gives G_{oo} in dB. This is the power level of the gain circle that passes through the LM plane at L = 1 and M = 0, (the center of the Smith chart). The values of the transistor 'y' parameters must be in the memory stack; and program 'A' must have been run, so that 'C' is stored in reg .3

Maximum Power Output, P_{oo} program

LINE	KEYCODE	KEYS	VALUE
172	42,21,14	f LBL 0	
173	45 5	RCL 5	g_{21}
174	45 6	RCL 6	b_{21}
175	42 25	I	MOVE TO COMPLEX STACK
176	45 3	RCL 3	g_{12}
177	45 4	RCL 4	b_{12}
178	42 25	I	MOVE TO COMPLEX STACK
179	10	÷	y_{21}/y_{12}
180	43 1	→P	$\lvert y_{21}/y_{12} \rvert$
181	43, 5, 8	CF 8	CLEAR COMPLEX FUNCTION
182	45 .3	RCL .3	C
183	20	X	
184	2	2	
185	10	÷	$\frac{C}{2} \left\lvert \frac{y_{21}}{y_{12}} \right\rvert$
186	43 13	g LOG	
187	1	1	
188	0	0	
189	20	X	
190	43 32	RTN	G_{oo} in dB

cient capacitors available. It was learned that positive temperature coefficient capacitors were available to P600 and higher. These were not generally off-the-shelf capacitors, but are practical capacitors.

One practical application of the thermally-tuned oscillator is to stabilize a power oscillator for use in the ISM (industrial, scientific and medical) band. This frequency band is set aside by the FCC for RF heating, burglar alarms, and motion and position sensing. The nominal frequency of the ISM band is 915 MHz and the tolerance is +/- 13 MHz, which is primarily to accomodate free-running oscillators. The tolerance of +/- 1.4% is achievable with a careful design of a low power oscillator. There are good reasons to include additional frequency stability into the design of an ISM oscillator. Achieving the desired stability would be more difficult for higher power oscillators. In addition it may be desirable to purposely offset the frequency of an ISM oscillator so that more than one system could coexist at a single location. This offsetting would ebb the permissable tolerance and require a more stable oscillator.

Figure 4 shows a block diagram of a stabilized 915 MHz oscillator using an inexpensive color burst crystal and an inexpensive ECL divider. In this example, an old-design phase/frequency detector with separate pump-up and pump-down outputs is used. There are several LSI frequency synthesizer chips available with the separate outputs. To use a conventional single-ended output phase detector, a window comparator would be required to provide the separate up and down control outputs.

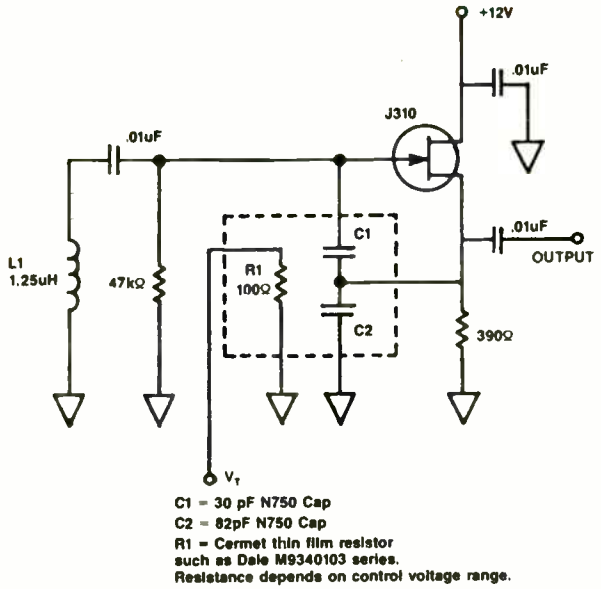
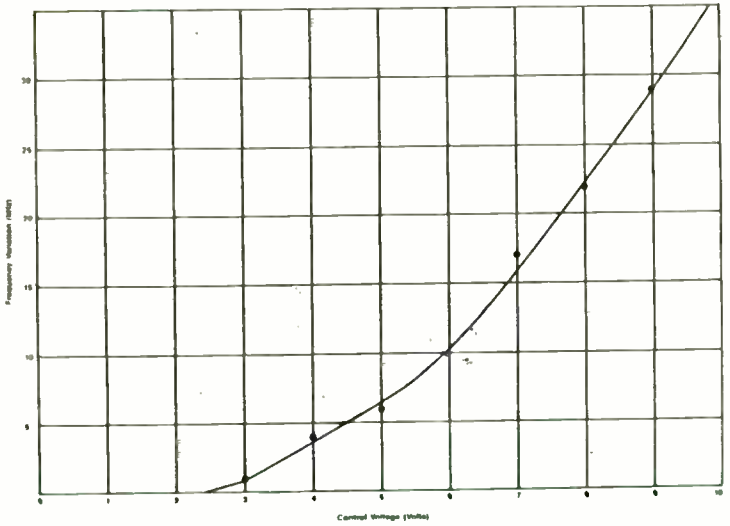


Figure 1. 30 MHz Test oscillator circuit diagram.



TRANSISTOR 'y' PARAMETERS, FOR SAMPLE CALCULATION

y_{11} = 17.2 + j 11.6 m mhos

y_{12} = 0 - j 0.64 m mhos

y_{21} = 32.2 - j 63.1 m mhos

y_{22} = 0.27 + j 1.89 m mhos

GRADIENT LINE ANGLE

θ = -27.03 DEG

GAIN AT MAXIMUM POWER OUTPUT

G_{oo} = 17.03 dB

STABILITY FACTOR

C = 0.9127

MAXIMUM GAIN

G_{MAX} = 19.374 dB

SAMPLE CALCULATION OF MAXIMUM GAIN

$$K_g = 2\left[\frac{1 - \sqrt{1 - C^2}}{C^2}\right]$$

Where C + 0.9127

K_g = 1.41982

$G_{MAX} = K_g G_{oo}$

Where G = 50.5159

G_{MAX} = 1.41982 X 50.5159

G_{MAX} = 71.7234

$G_{MAX_{dB}}$ = 10 LOG 71.7234

$G_{MAX_{dB}}$ = 18.5566 dB

This gain point on the paraboloid of revolution is the point where the input plane, so oriented, just touches the paraboloid.

CALCULATION OF GAIN CIRCLE DATA

GAIN RATIO 'g'	GAIN RATIO IN dB 'g_{dB}'	DISTANCE TO CENTER 'd'	RADIUS OF GAIN CIRCLE 'r'
1.41982	1.522 dB	-0.6479	.00693
1.25893	1.0	-0.574546	.266783
1.0	0	-.456376	.456376
0.707	-1.5	-.322658	.630165

The distance is measured from the point L = 1, M = 0 (The center of the Smith chart). A measurement from this central point to the edge of the chart is 3.57 inches. The above values of distance and radius are in relation to unity. These must be converted by a ratio of one to 3.57 This is so that the distances may be made directly on the Smith chart. Sample calculation,

$$\frac{d_{in}}{3.57} = \frac{-.6479}{1} \quad ; \quad d_{inches} = 2.306 \text{ in}$$

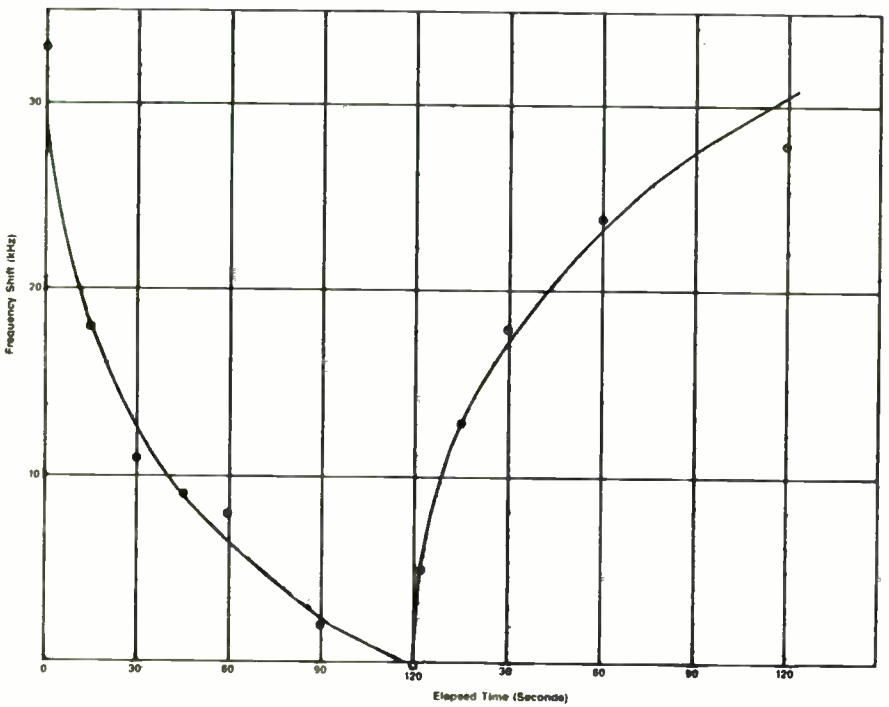


Figure 2(b). Time-Frequency Dependence

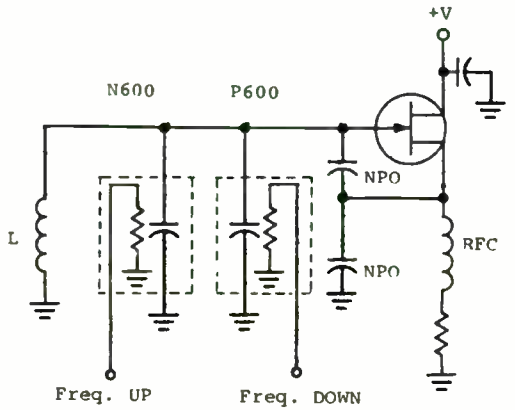


Figure 3. Oscillator configuration with positive and negative temperature coefficient capacitors.

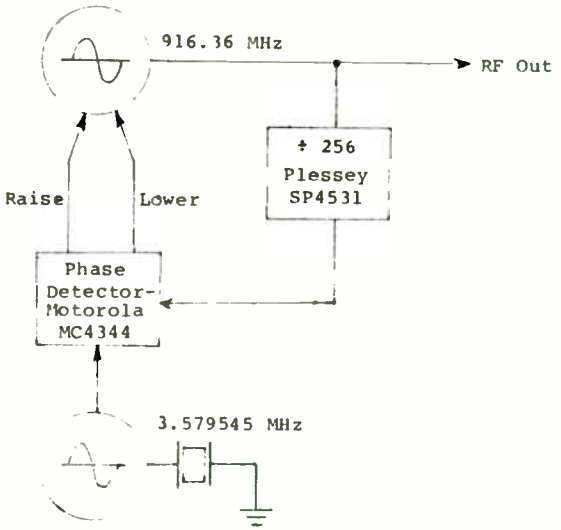


Figure 4. Stabilized oscillator application.

DISTANCES IN INCHES FOR DIRECT TRANSFER TO THE SMITH CHART

GAIN RATIO	GAIN RATIO dB	$G_{oo}+g_{dB}$	DISTANCE TO CENTER OF GAIN CIRCLE IN INCHES	RADIUS OF GAIN CIRCLE IN INCHES
1.41982	1.522	18.55	-2.306 IN	0.02467
1.25893	1.0	18.03	-2.04538	0.949747
1.0	0	17.03	-1.62470	1.62470
0.707	-1.5	15.53	-1.14866	2.24339

Remember, the gradient line angle, -27.03; and using these above values of distance and radius, draw the Linvill chart.

LINVILL CHART

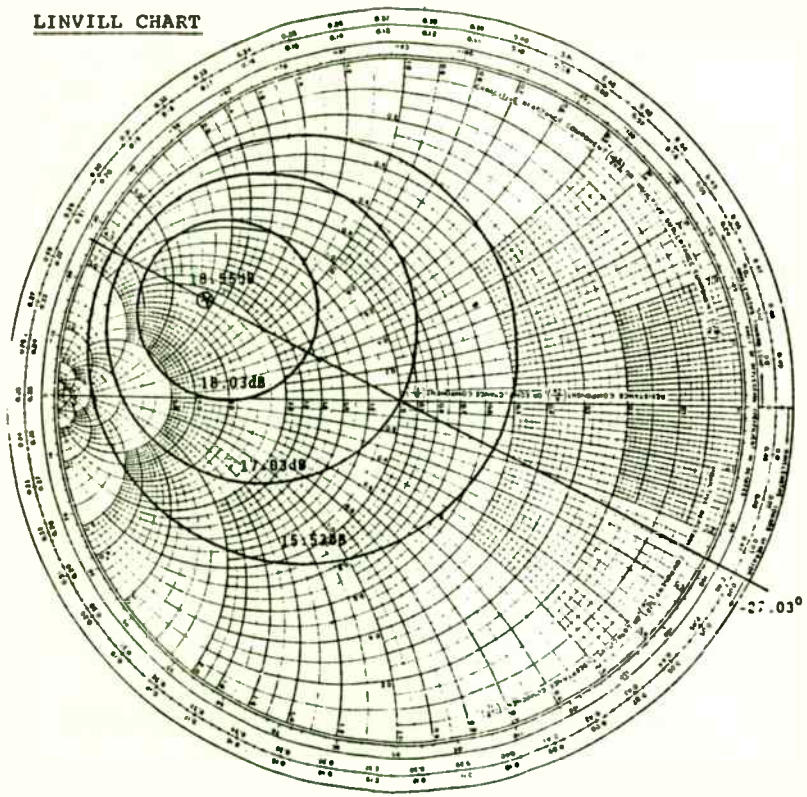


Figure 5, Linvill Chart

The Linvill chart has been drawn from the 'y' parameters. These parameters were selected for the sample calculation. The LM plane of the power output graph has a correspondence to a Smith chart rotated 180 degrees. Points on this chart have a relation to the output load to be selected for the transistor. This output load may be selected from any point in the LM plane. But for this demonstration select a LM point under the maximum gain point. A G_{MAX} of 18.55 dB is read. Reading from the Smith chart, the conductance is 2.2, and the susceptance is -2.2 These are related to the output load and the transistor reactance by the following,

$$G_L = 2.2 \times g_{22} = 2.2\ (0.27\ ) = 0.594 \text{ m mho}$$

$$B_L = -2.2 \times g_{22} - b_{22} = -2.2\ (\ 0.27\ ) - 1.89 = -2.484 \text{ m mho}$$

OUTPUT LOAD FOR G_{MAX}

$$Y_L = G_L + j\,B_L = 0.594 - j\ 2.48 \text{ m mho}$$

Computer-Aided Design of a Bipolar Transistor Amplifier

by

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Introduction

To be competitive in the RF and microwave hardware industry, companies must develop sophisticated components and systems at competitive prices -- with delivery schedules that tax the most experienced engineers. In response to growing market requirements many companies are turning to computer-aided engineering (CAE) and design (CAD) software to reduce design time and manufacturing costs.

Different design techniques and problems must be understood in order to be efficient with computer-aided design. The purpose of this paper is to present many of the necessary design techniques typically used in developing a new component. The design of a medium power bipolar transistor amplifier serves as an example of how to use these new computer-aided tools in designing modern hardware.

Design Outline

The complete procedure used for this example will be as follows:

1) Device Modeling
2) Device Characterization
3) Synthesizing A Matching Network
4) Small Signal Simulation
5) Large Signal Simulation
6) Fine Tuning the Design
7) Generating the Layout
8) Results
9) Conclusions

Device Modeling

The first part of any active design begins with the DC characterization of the active device. For this example the device was a bipolar transistor, MRA0500-19L, manufactured by TRW. This device is a linear power transistor designed for Class "A" medium power linear amplifiers with a useable frequency range from 100 to 500 GHz. The transistor is a multi-cell device with internal matching and produces 19 watts @Vce=19 volts and Ic=3.5 amps when compressed 1 dB. The small signal gain is 8 dB minimum.

In order to predict device performance, a suitable model must be used in conjunction with a nonlinear simulator program (mwSPICE) that can provide power measurement and S-parameters [1]. The Gummel-Poon model [2] for an NPN was used for this example. Initially, the I-V and C-V characteristics [3] were measured to obtain the parameters for the BJT model.

Table I lists the key parameters in evaluating the device. The performance of the mwSPICE circuit file listed in Figure A-1, Appendix A, was used for simulation. The default values of other model parameters (not listed) were used during the analysis. Further details concerning

THE INPUT MATCHING CIRCUIT

Previously defined 'y' parameters, at 200 mHz

y_{11} = 17.2 + j 11.6 m mho

y_{12} = 0 - j 0.64 m mho

y_{21} = 32.2 - j 63.1 m mho

y_{22} = 0.27 + j 1.89 m mho

and Y_L has been selected, 0.594 - j 2.48

Substitute these values into the following equation,

$$y_{in} = y_{11} - \frac{y_{12}\ y_{21}}{y_{22} + Y_L}$$

(On the HP 15c, run GSB 1; Note y_{11} through y_{22} must be entered in registers 1 through 8. Y_L must be in reg .9 & .0)

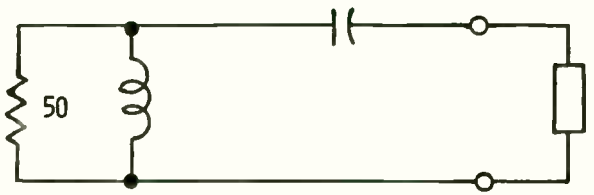

Figure 6, Input Matching Network

A matching circuit is developed by starting with the admittance Y_{in}, and working leftwards to obtain a 50 ohm termination. First the input admittance, 37.97 + j 49.6 m mho is not a normalized admittance. It must be divided through by a reciprocal 50 ohms. This is equivalent to a division by 20×10^{-3}. The normalized value is 1.898 + j 2.482 This normalized admittance can now be placed directly on the Smith chart. The normalized impedance and admittance coordinates Smith chart is best used here. The impedance values are on the orange lines; and the admittance values are on the green lines. Looking through from the green lines to the orange, transforms from admittance to impedance. Move counter-clockwise from -j 0.255, along a constant impedance circle, and arrive at -j 0.395 on the normalized 50 ohm circle. The difference of these two gives the normalized reactance the input impedance must first see. (-j 0.395 - (-j 0.255)) = -j0.14 It is normalized, so it must be multiplied by 50 to obtain the reactance.

$$\begin{array}{r} -j\ 0.14 \\ \times 50 \\ \hline -j\ 7.0 \end{array}$$

$$X_C = -7.0 = \frac{1}{2\pi fC}\ ;\quad C = \frac{1}{7.0\ (\ 2 \times 3.14 \times 200 \times 10^6)}$$

C = 113.68 pF

The impedance of the circuit is at this point parallel to the input impedance. Therefore conversion is now made to admittance, the green lines.

Table I. Key BJT Model Parameters.

Parameter	Description	Value	
IS	Transport Saturation Current	1.5E-3	Amp
BF	Maximum Foward Beta	85	
VAF	Forward Early Voltage	52	Volt
IKF	Beta Knee Current	80	Amp
ISE	Base Emitter Leakage Current	4E-5	Amp
NE	Base Emitter Leakage Coefficient	1.35	
VAR	Reverse Early Voltage	6	Volt
RB	Zero Bias Base Resistance	0.08	Ohms
RE	Emitter Resistance	0.115	Ohms
RC	Collector Resistance	0.35	Ohms
CJE	Base Emitter Capacitance	200p	Farad
VJE	Base Emitter Potential	0.20	Volt
MJE	Base Emitter Coefficient	3.5	
TF	Forward Transit Time	115p	Sec
XTF	TF Bias Coefficient	3.5	
VTF	TF Vbc Coefficient	3.0	Volt
ITF	TF High Current Parameter	4.5	Amp
CJC	Base Collector Capacitance	115p	Farad
VJC	Base Collector Potential	0.22	Volt
MJC	Base Collector Coefficient	0.185	

device model characterization will soon appear in an article in RF Design Magazine. Table II provides a description of key features of the mwSPICE circuit file.

Table II. Circuit File Summary of Figure A-1.

Circuit Data/Block	Content
subcircuit "TRAN"	Describes all of the bond lead inductances and all internal parasitics associated with the packaged device.
subcircuit "NET"	Supplies the biases to "TRAN."
MODEL block	Describes the parameters used in the analysis.
SOURCE block	Provides a quiescent bias point. The AC input is used for the S-parameter measurement.
CONTROL block	Lists the frequencies over which the S-parameters will be measured with the stepped bias condition for I-V generation.
SPICEOUT block	Lists the desired data for output and the name of the S-parameter file where the data will be saved.

Device Characterization

Using the aforementioned circuit file, a simulation of the primary characteristics, I-V and S-parameters, was performed. In addition, to ensure that the mwSPICE model predicted the correct device performance, a comparison was made between the measured and mwSPICE-predicted I-V and S-parameter data over the design band of 170 to 230 MHz.

Figure 1 shows the comparison of the measured and simulated I-V characteristics while Table III provides the S-parameter comparison of the packaged device. As seen in Figure 1 and Table III, the theoretical and measured data agree quite well.

We are at the point, 1 + j 2.05 admittance. Moving along the constant admittance circle to one, takes us in a negative admittance direction. Therefore the value is inductive. This distance is -j 2.05 Multiply by 20×10^{-3} (reciprocal 50 ohms).

$$2.05 \times 20 \times 10^{-3} = 41.0 \times 10^{-3} \text{ mho}$$

Take the reciprocal to get it into a reactance value (reciprocal of mho).

$$X_L = 24.39$$

$$X_L = 2\pi fL$$

$$L = \frac{24.39}{2 \times 3.14 \times 200 \times 10^6}$$

$$L = 0.0194089 \text{ micro henry}$$

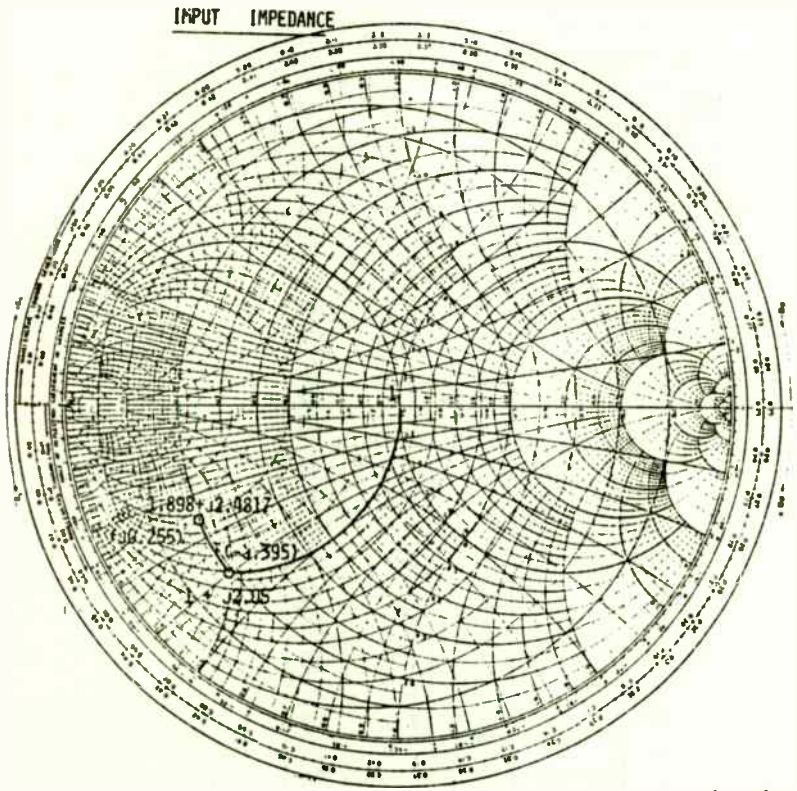

Figure 7, Input Impedances

Admittance, unbracketed

Impedance, bracketed

CALCULATOR PROGRAM FOR INPUT IMPEDANCE

$$Y_{in} = Y_{11} - \frac{Y_{12}\, Y_{21}}{Y_{22} + Y_L}$$

(equation obtained when the 'y' parameter model was first defined.)

To run - GSB 1; (to go to a line GTO CHS 191)

(Note this program will eliminate any previously calculated values of ⊖ and C obtained in program 'A'.)

REG	PARAMETER	
1	Re Y_{11}	17.2
2	Im Y_{11}	11.6
3	Re Y_{12}	0
4	Im Y_{12}	-0.64
5	Re Y_{21}	32.2
6	Im Y_{21}	-63.1
7	Re Y_{22}	0.27
8	Im Y_{22}	1.89
9	Re Y_L	0.594
.0	Im Y_L	-2.48
.1	Re $(Y_{22} + Y_L)$	0.864
.2	Im $(Y_{22} + Y_L)$	-0.590
.3	Re Y_{IN}	37.96
.4	Im Y_{IN}	49.634

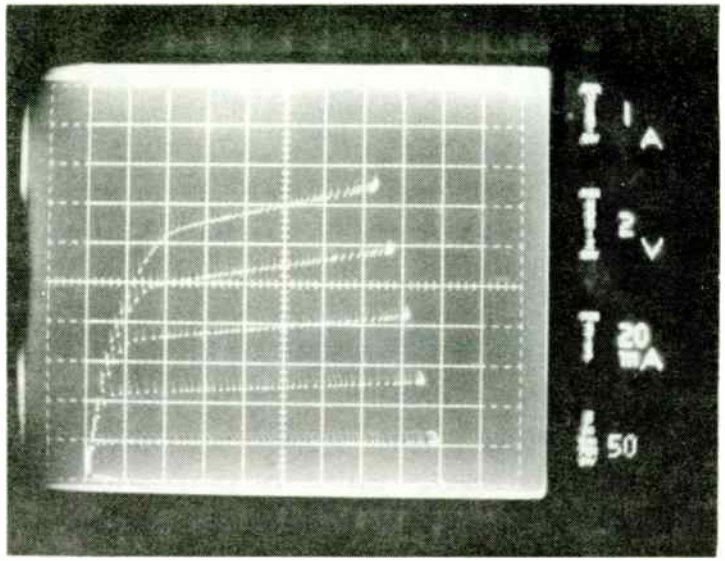

Figure 1(a). Measured I-V curves.

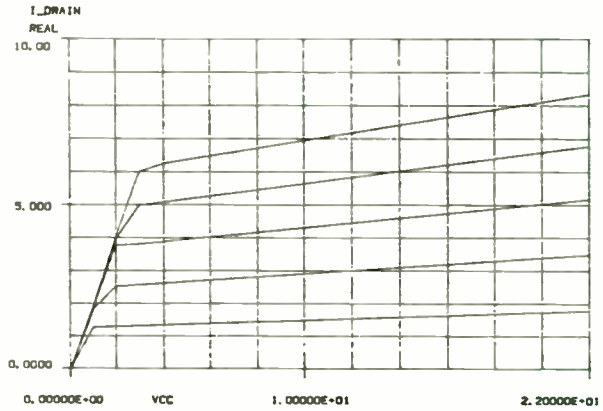

Figure 1(b). mwSPICE-produced I-V curves.

Table III. Comparison of Measured and Theoretical S-Parameters.

Measured S-Parameters

```
! MEASURED BY A NETWORK ANALYZER
! VDS=19V, IDS=3.5A
# GHZ S MA R 50
```

! FREQ	M(S11)	A(S11)	M(S21)	A(S21)	M(S12)	A(S12)	M(S22)	A(S22)
170.000	0.992	175.197	0.699	69.035	0.013	48.455	0.814	174.903
180.000	0.992	174.885	0.676	65.900	0.013	47.980	0.813	175.069
190.000	0.992	174.573	0.653	62.764	0.013	47.504	0.813	175.235
200.000	0.992	174.261	0.630	59.628	0.014	47.028	0.813	175.401
210.000	0.991	173.978	0.614	57.017	0.014	46.477	0.814	175.401
220.000	0.990	173.696	0.598	54.405	0.014	45.925	0.816	175.401
230.000	0.989	173.413	0.583	51.794	0.014	45.374	0.817	175.401

mwSPICE-produced S-Parameters

```
!  GENERATED BY mwSPICE
!  TEMPERATURE =   27.000 DEG C      8/26/86      20:24:8
#  S  GHZ  MA  R   50.0
```

! FREQ	M(S11)	A(S11)	M(S21)	A(S21)	M(S12)	A(S12)	M(S22)	A(S22)
170.000	0.986	175.620	0.700	69.790	9.6E-03	47.600	0.818	176.150
180.000	0.986	175.340	0.675	68.380	0.010	48.300	0.816	175.830
190.000	0.985	175.050	0.653	66.950	0.011	48.850	0.813	175.520
200.000	0.984	174.750	0.635	65.490	0.012	49.260	0.811	175.190
210.000	0.984	174.450	0.620	63.990	0.012	49.540	0.808	174.870
220.000	0.983	174.140	0.608	62.460	0.013	49.690	0.805	174.530
230.000	0.982	173.830	0.598	60.890	0.014	49.710	0.801	174.190

CALCULATOR PROGRAM,

FOR INPUT IMPEDANCE

(Continued)

191	42,21. 1	LBL 1		
192	45 7	RCL 7	g_{22}	0.27
193	45 8	RCL 8	b_{22}	1.89
194	42 25	f I	y_{22}	0.27
195	45 9	RCL 9	G_{Y_L}	0.594
196	45 .0	RCL .0	B_{Y_L}	-2.48
197	42 25	f I	Y_L	0.594
198	40	+	$Y_{22} + Y_L$	0.864
199	44 .1	STO .1	RE $(Y_{22}+Y_L)$	0.864
200	42 30	f RE≷IM		-0.59
201	44 .2	STO .2	IM $(Y_{22}+Y_L)$	-0.59
202	42 30	f RE≷IM	$y_{22} + Y_L$	0.864
203	45 3	RCL 3	g_{12}	0
204	45 4	RCL 4	b_{12}	-0.64
205	42 25	f I	y_{12}	0
206	45 5	RCL 5	g_{21}	32.2
207	45 6	RCL 6	b_{21}	-63.1
208	42 25	I	y_{21}	32.2
209	20	X	$Y_{12}Y_{21}$	-40.38 -j20.608
210	45 .1	RCL .1	RE $(Y_{22}+Y_L)$	0.864
211	45 .2	RCL .2	IM $(Y_{22}+Y_L)$	-0.59
212	42 25	f I	$Y_{22} + Y_L$	0.864
213	10	÷	$y_{12}y_{12}/(y_{22}+Y_L)$	-20.7-j38.0
214	45 1	RCL 1	g_{11}	17.2
215	45 2	RCL 2	b_{11}	11.6
216	42 25	f I	y_{11}	17.2
217	34	X≷Y	$y_{12}y_{21}/(y_{22}+Y_L)$	-20.7-j38.0
218	30	-		37.9+j49.63
219	44 .3	STO .3	Re Y_{in}	37.968
220	42 30	f RE≷IM		49.634
221	44 .4	STO .4	Im Y_{in}	49.6340
222	42 30	f RE≷IM	Y_{in}	37.96+j49.634
223	43 32	RTN		

THE CIRCUIT

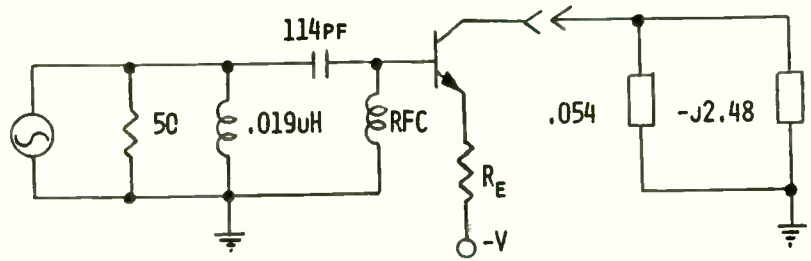

Figure 8, Transistor Matching Circuit

It is assumed that the output circuits can be developed with the normalized impedance and admittance Smith chart. This is the chart used to develop the input circuits.

Synthesizing A Matching Network

With the DC/AC characterization verified, we were then ready to synthesize, in E-Syn [4], an input and output matching network based on the S-parameter file that was generated from the mwSPICE model. For a power design, the output was matched for maximum output power while the input was designed for the best match.

The input matching network utilized Chebyshev bandpass networks. Several circuits were provided during synthesis which satisfied the matching requirements. However, the Figure A-2 circuit was selected because it provided a DC block for the base of the BJT.

The results of a power contour analysis revealed that S22 was the best match for maximum power; this occurred due to internal matching by the manufacturer. For this example, the nominal output impedance of the device was used as the load to be matched in E-Syn. The output circuit was then synthesized using a Chebyshev transformer (Figure A-3) and matched to an output impedance of 5.2 Ohms.

Small Signal Simulation

The two networks synthesized in E-Syn were incorporated into the original circuit file (Figure A-1) to create the Figure A-4 circuit file. Figure A-4 is a Touchstone/mwSPICE circuit file modified to include S-parameters of the device (S2PA) and allow for immediate cross-checking of return loss and gain in both the linear (Touchstone) and nonlinear (mwSPICE) simulators.

The Touchstone simulation of the complete circuit (Figure 2) shows that the amplifier has a maximum input and output return loss of -7.6 dB and the gain varies from 14.5 dB at the low end of the band to 12.8 dB at the high end. A tabular listing of the Figure 2 circuit file, Table IV indicates that the circuit is unconditionally stable for this simulation.

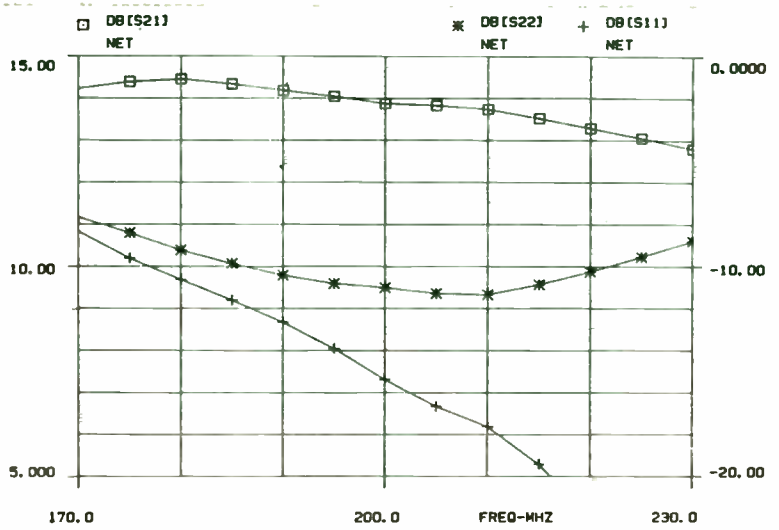

Figure 2. Small signal response in Touchstone.

Table IV. Small Signal Results.

FREQ-MHZ	DB[S21] NET	DB[S11] NET	DB[S22] NET	K NET
170.000	14.224	-8.331	-7.660	1.158
175.000	14 389	-9.598	-8.405	1.158
180.000	14.455	-10.619	-9.227	1.159
185.000	14 337	-11.594	-9.867	1.163
190.000	14 186	-12.648	-10.421	1.168
195.000	14 042	-13 890	-10 816	1.170
200.000	13.871	-15.367	-11 015	1.172
205.000	13.820	-16.647	-11.288	1 182
210.000	13.735	-17.609	-11 348	1.191
215.000	13.517	-19.407	-10.864	1 191
220.000	13.285	-21.900	-10.259	1.191
225 000	13.050	-26.221	-9 548	1.191
230.000	12.801	-37.245	-8.795	1.191

PARAMETER CONVERSION

$$Y_{11} = \frac{(1 + S_{22})\ (1 - S_{11})\ + S_{12}\,S_{21}}{(1 + S_{11})\ (1 + S_{22})\ - S_{12}\,S_{21}}$$

$$Y_{12} = \frac{-2\,S_{12}}{(1 + S_{11})\ (1 + S_{22})\ - S_{12}\,S_{21}}$$

$$Y_{21} = \frac{-2\,S_{21}}{(1 + S_{11})\ (1 + S_{22})\ - S_{12}\,S_{21}}$$

$$Y_{22} = \frac{(1 + S_{11})\ (1 - S_{22})\ + S_{12}\,S_{21}}{(1 + S_{22})\ (1 + S_{11})\ - S_{12}\,S_{21}}$$

With these equations, parameters measured in 's' parameters can be converted to the admittance 'y' parameters.

CALCULATOR PROGRAM, HP15c, PARAMETER CONVERSION 's' TO 'y'

0	S_{11} R	.13548	.2395
1	S_{11} I	-.54337	.9606
2	S_{12} R	.0064279	.001730
3	S_{12} I	.00766043	-.001066
4	S_{21} R	-1.3339	-.06387
5	S_{21} I	3.6648	3.049
6	S_{22} R	.60211	.06957
7	S_{22} I	-.37624	.884
8	DENO R	1.65	$(1+S_{11})(1+S_{22})-S_{12}S_{21}$ (R)
9	DENO. I	-1.3	(I)
.0	$S_{12}S_{21}$ R	-36.648×10^{-3}	
.1	$S_{12}S_{21}$ I	13.339×10^{-3}	

's' TO 'y' CONVERSION, continued

071	42,21,15	LBL E	
072	45 2	RCL 2	
073	45 3	RCL 3	
074	42 25	f I	
075	45 4	RCL 4	
076	45 5	RCL 5	
077	42 25	f I	
078	20	X	
079	44 .0	STO .0	
080	42 30	f Re≷Im	
081	44 .1	STO .1	
082	1	1	
083	45 0	RCL 0	
084	45 1	RCL 1	
085	42 25	f I	
086	40	+	
087	1	1	
088	45 6	RCL 6	
089	45 7	RCL 7	
090	42 25	f I	
091	40	+	
092	20	X	
093	45 .0	RCL .0	
094	45 .1	RCL .1	
095	42 25	f I	
096	30	-	
097	44 8	STO 8	
098	42 30	f Re≷Im	
099	44 9	STO 9	
100	42 30	R f I	
101	1	1	
102	45 6	RCL 6	
103	45 7	RCL 7	
104	42 25	f I	S_{22}
105	40	+	$(1 + S_{22})$
106	1	1	
107	45 0	RCL 0	
108	45 1	RCL 1	
109	42 25	f I	
110	30	-	
111	20	X	
112	45 .0	RCL .0	$S_{12}S_{21}$
113	45 .1	RCL .1	
114	42 25	f I	
115	40	+	
116	45 8	RCL 8	
117	45 9	RCL 9	
118	42 25	f I	
119	10	÷	
120	44 .2	STO .2	
121	42 30	f Re≷Im	
122	44 .3	STO .3	
123	2	2	
124	16	CHS	
125	45 2	RCL 2	

Large Signal Simulation

mwSPICE was then used in conjunction with the circuit file (Figure A-4) to to simulate the large signal performance of the complete circuit. An input power level of 1 watt (+30 dBm) was used during the simulation because the device was designed for a particular application. Figure 3 shows the simulated output power and gain vs. input power.

At the 1-watt drive level, the device response was in the linear region; therefore, both the linear and nonlinear simulators should have yielded the same results. This was verified by comparing the graphs of Figures 2 and 4.

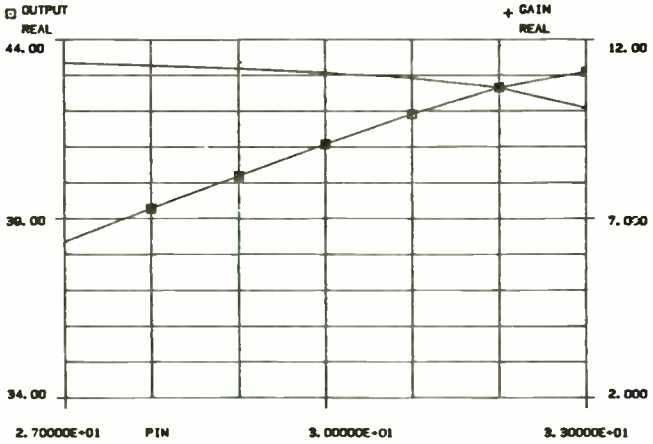

Figure 3. Output power and gain vs. input power response in mwSPICE.

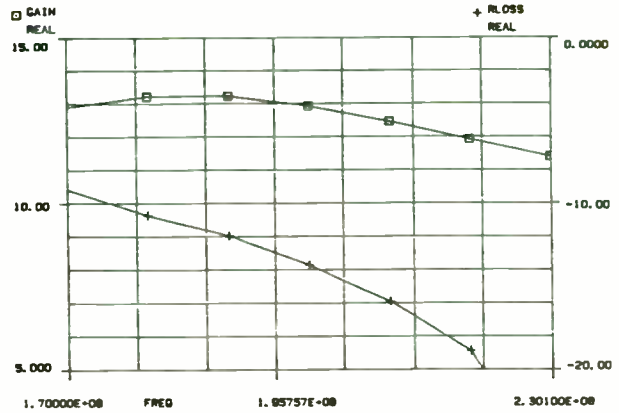

Figure 4. Return loss and gain vs. frequency response in mwSPICE.

The results of the mwSPICE Fourier analysis (Table V) then indicated that the second harmonic had the highest level at -31 dBc.

Table V. mwSPICE-Produced Fourier Analysis of Circuit.

DC COMPONENT = 1.345D+00

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	2.300D+08	1.779D+01	1.000000	-29.160	.000
2	4.600D+08	5.108D-01	.028709	-119.318	-90.158
3	6.900D+08	1.229D-01	.006910	-55.691	-26.531
4	9.200D+08	5.701D-02	.003204	-12.316	16.844
5	1.150D+09	3.966D-02	.002229	1.091	30.251
6	1.380D+09	3.140D-02	.001765	2.539	31.700

's' TO 'y' CONVERSION, continued

126	45 3	RCL 3
127	42 25	f I
128	20	X
129	45 8	RCL 8
130	45 9	RCL 9
131	42 25	I
132	10	÷
133	44 .0	STO .4
134	42 30	R I
135	44 .5	STO .5
136	2	2
137	16	CHS
138	45 4	RCL 4
139	45 5	RCL 5
140	42 25	I
141	20	X
142	45 8	RCL 8
143	45 9	RCL 9
144	42 25	I
145	10	÷
146	44 .6	STO .6
147	42 30	R I
148	44 .7	STO .7
149	1	1
150	45 0	RCL 0
151	45 1	RCL 1

152	42 25	I
153	40	+
154	1	1
155	45	RCL 6
156	45	7
157	42 25	I
158	30	-
159	20	X
160	45 .0	RCL .0
161	45 .1	RCL .1
162	42 25	I
163	40	+
164	45 8	RCL 8
165	45 9	RCL 9
166	42 25	I
167	10	÷
168	44 .8	STO .8
169	42 30	R I
170	44 .9	STO .9
171	43 32	RTN

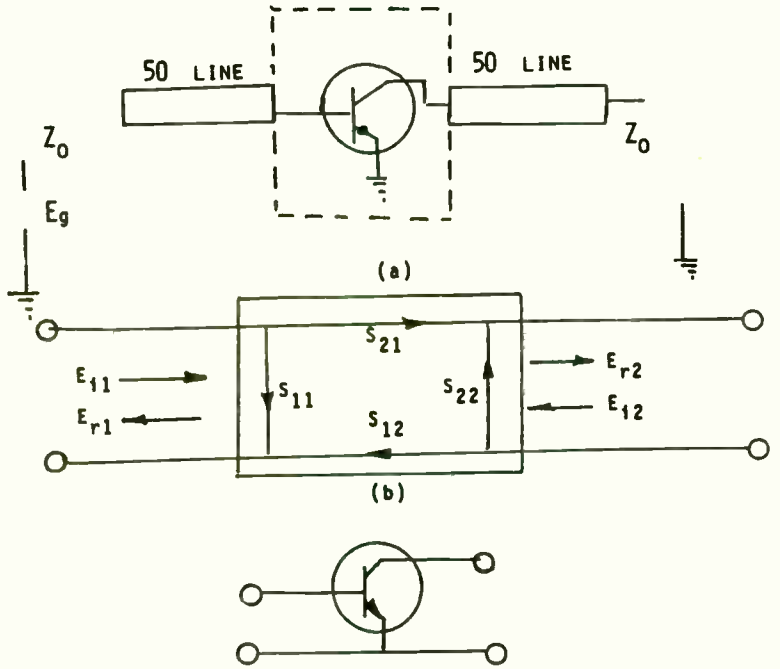

Figure 9, Block Diagram of a Typical 's' Parameter Measurement system

COMMON EMITTER

$s_{11} = s_{ie}$

$s_{21} = s_{fe}$

$s_{22} = s_{oe}$

$s_{12} = s_{re}$

$$s_{11} = \left.\frac{E_{r1}}{E_{i1}}\right|_{E_{i2}=0} \qquad s_{22} = \left.\frac{E_{r2}}{E_{i2}}\right|_{E_{i1}=0}$$

$$s_{21} = \left.\frac{E_{r2}}{E_{i1}}\right|_{E_{i1}=0} \qquad s_{12} = \left.\frac{E_{r1}}{E_{i2}}\right|_{E_{i1}=0}$$

Fine Tuning the Design

Next, the variables were tweeked using the tune mode in Touchstone to achieve a flatter gain response. In addition, parameters to generate the layout were added to the circuit file, which resulted in Figure A-5.

The modified circuit file design was cross-checked in mwSPICE. The results (Tables VI and VII and Figures 5 and 6) demonstrated close agreement between the programs. The mwSPICE gain response was 1 dB less than the Touchstone response due to bias circuitry contained in the SPICEOUT data block which was ignored by Touchstone but had a loading affect on mwSPICE performance.

Table VI. Touchstone Tabular Results of the Final Circuit Design.

FREQ-MHZ	DB[S21] NET	DB[S11] NET	DB[S22] NET	K NET
170.000	11.292	-6.835	-2.235	1.158
180.000	12.001	-12.127	-2.430	1.159
190.000	11.891	-16.194	-3.092	1.168
200.000	11.737	-19.846	-3.737	1.172
210.000	11.846	-21.765	-4.264	1.191
220.000	11.613	-20.603	-4.292	1.191
230.000	11.225	-14.417	-4.110	1.192

Table VII. mwSPICE Tabular Results of the Final Circuit Design.

FREQ MHZ	INPUT POWER (dBm)	OUTPUT POWER (dBm)	GAIN (dB)	RLOSS (dB)
170.00	30.00	40.08	10.089	- 7.60
180.00	30.00	40.88	10.88	-12.80
190.00	30.00	41.16	11.16	-17.51
200.00	30.00	41.08	11.08	-18.13
210.00	30.00	40.79	10 79	-20.27
220.00	30.00	40 41	10.41	-23.56
230.00	30.00	39.98	9.97	-16.48

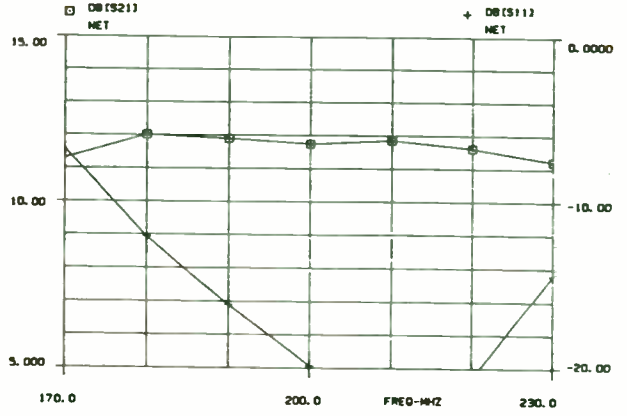

Figure 5. Final circuit file gain response in Touchstone.

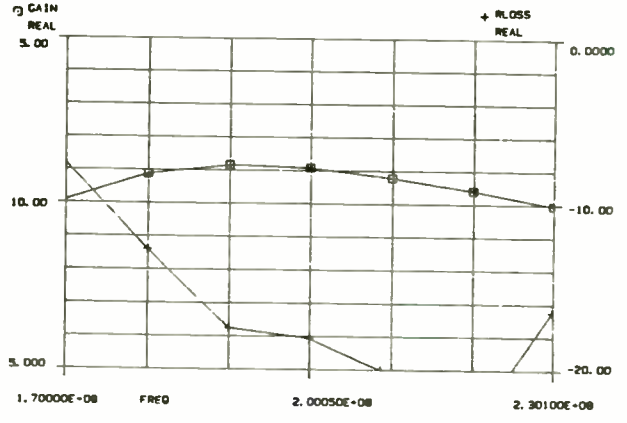

Figure 6. Final circuit file gain response in the mwSPICE.

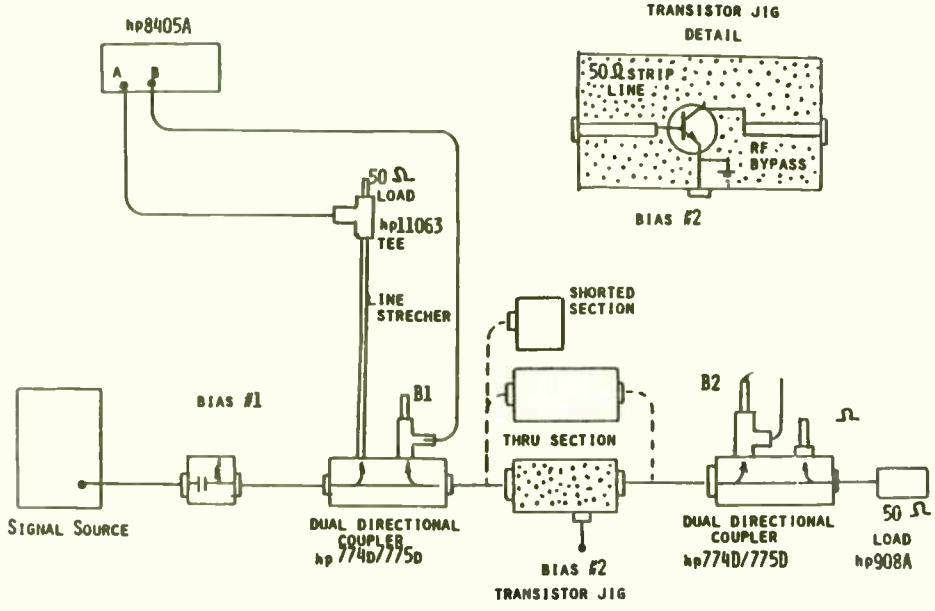

Figure 10, Block Diagram of a Typical 's' Parameter Measurement System

REFERENCES:

1) "The Design of Tetrode Transistor Amplifiers" J. G. Linvill & L. G. Schimpf, Bell System Technical Journal, Vol 35, July 1956, pages 813-840

2) Application Note 77-1, Hewlett Packard, pages 2-4

Generating the Layout

A circuit layout was then generated by the CAD drawing program MiCAD [6] and transformed by the postprocessing program MICmask [7] to drive a laser photoplotter -- thus creating the mask for manufacturing the circuit.

The layout modification does not interfere with the design analysis -- MiCAD only reads the necessary physical description while the simulators Touchstone and mwSPICE only read those portions of the circuit file required for a particular simulation.

To add microstrip lines for all lumped elements, in MiCAD we added PAD1 statements which set up transmission lines, their lengths, and the gap desired between them. The PARA statements simply identify parasitics which are to be ignored by MiCAD in the layout. Allowing a number of layouts and "mapping" of repeat components and parts to different drawings, MiCAD files were set up as follows:

Layer 0: Used the autoprocessed file input from Figure A-5 to create the 1:1 mask drawing file. Text, ground pads, and bias circuitry were added without using the circuit file.

Layer 1: Held the corner markers and alignment markers.

Layer 2: Held the substrate etched drawing with dimensions and Layer 1 markers copied to it

Layer 3: Held the transistor outline which was copied into the necessary locations on Layer 0 as needed.

Layer 4: Provided the assembly drawing.

The completed mask layout is shown in Figure 7 and the associated assembly drawing appears in Figure 8.

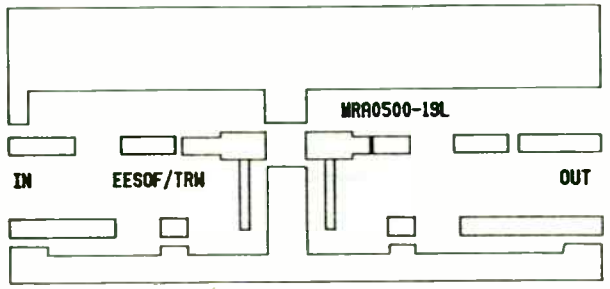

Figure 7. Amplifier mask layout generated by MiCAD.

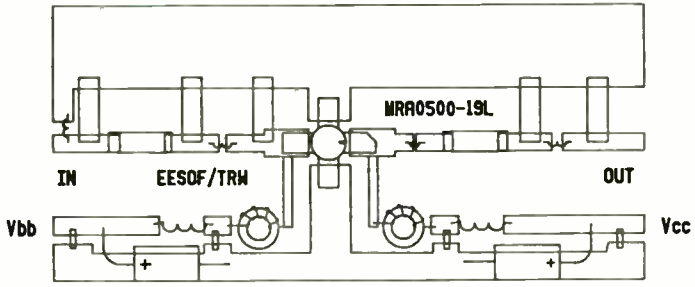

Figure 8. Amplifier assembly drawing generated by MiCAD.

The Results

The final design was then built and tested on a scalar network analyzer. The schematic for the final amplifier design is shown in Figure 9.

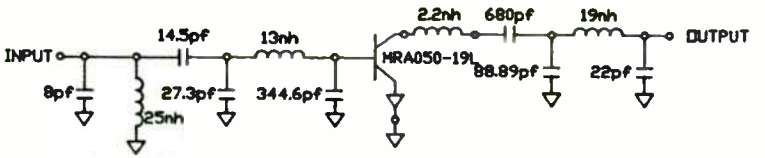

Figure 9. The final bipolar transistor amplifier design.

The measured results (Figure 10) confirm the accuracy of the circuit design illustrated in the mwSPICE response (Figure 11). Although the dip in the return loss for the measured response was at a lower frequency than predicted and the gain was slightly lower than predicted, the nature of both responses was the same.

The device used in the test amplifier was selected from a group of 10 devices used during the device modeling procedure. Since the parameters of the 10 devices were averaged and then used in the circuit file, any single device would not provide a measured response identical to the predicted response. However, if all 10 devices had been rotated in the test amplifier to generate a measured average response, the measured and predicted responses would have been identical.

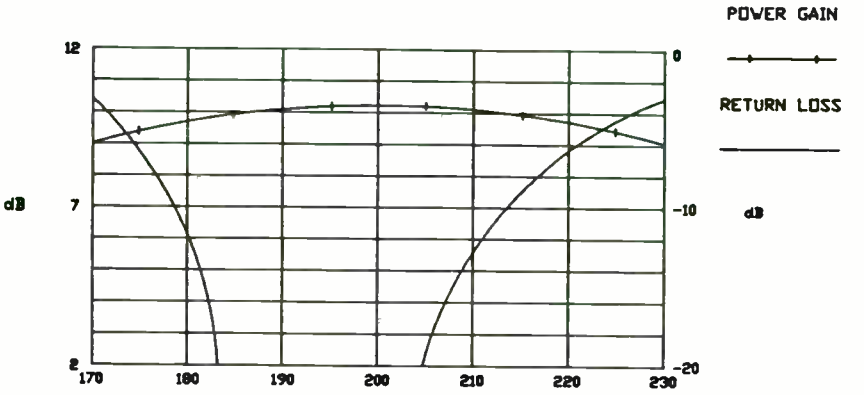

Figure 10. Measured gain response of the actual circuit.

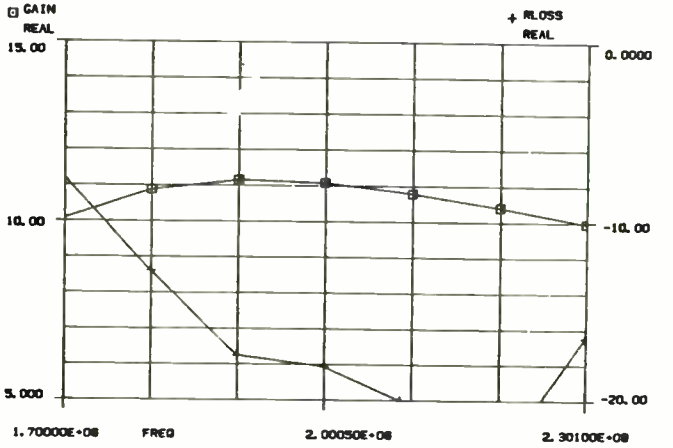

Figure 11. mwSPICE circuit file response.

Basic MODAMP™ MMIC Circuit Techniques

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Introduction and MODAMP™ MMIC Structure

This paper describes Avantek's MSA (Monolithic Silicon Amplifier) series MODAMP™ silicon bipolar Monolithic Microwave Integrated Circuits (MMICs), intended for use as general purpose 50 ohm gain blocks. Their single chip construction minimizes size and parasitics and maximizes uniformity. The wafer fabrication process uses nitride self-alignment for precise registration, ion implantation for precise doping control, and both gold metalization and nitride passivation for high reliability. A variety of geometries allow the designer to select for appropriate gain, power, noise, and frequency chacteristics. Packaging options, ranging from inexpensive plastics to high reliability, hermetically sealed ceramic microstrip.

The internal structure of the MODAMP™ MMIC is a Darlington connected pair of transistors with resistive feedback and a simple resistive biasing scheme. A general schematic is shown in Fig. 1. Since S_{11} and S_{22} are set primarily by resistive divider networks, they remain relatively constant over a wide frequency range. The use of both series feedback (R_E adjusting the emitter voltage of Q2) and shunt feedback (R_F adjusting the base voltage of Q1) helps desensitize the design to variations in active device parameters. A "bleeder" resistor attached to the emitter of Q1 decouples the quiescent bias point of Q1 from the β of Q2 (without this resistor the emitter current of Q1 would necessarily equal the base current of Q2). R_C also serves a feedback function. As the transistors draw more current, the voltage drop across R_C will decrease the collector voltages, tending to shut down the transistors.

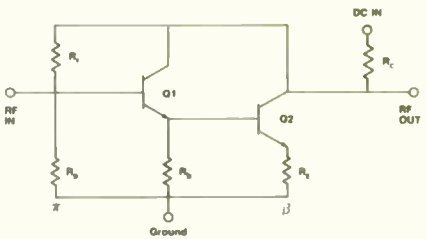


Figure 1. General MODAMP™ schematic.

Since device β (and, therefore, collector current, given a fixed bias) tends to increase with temperature, R_C also serves as a temperature compensating element. Note: On some MODAMP™ MMICs, R_C is an internal element whose value may be a selectable option; on others it must be added as an external component. MODAMP™ MMICs containing internal R_C's have dash suffixes beginning with "1", e.g., MSA-0235-11. Units without an internal collector resistor have dash suffixes beginning with "2" or have no dash suffix.

Since the internal resistive networks prematch both input and output to 50 ohms, MODAMP™ MMICs are particularly easy to design with. To design an amplifier, all that's needed is a 50 ohm microstrip line, blocking capacitors, and some very simple bias circuitry. Nonetheless, because MODAMP™ MMICs are high frequency devices, there are some basic construction rules that should be followed when using them.

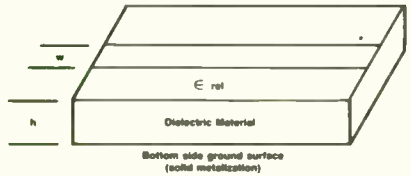


Figure 2. Microstrip structure.

Stripline Structures

Fig. 2 shows a typical microstrip structure. Line impedances are determined by strip width (w), board dielectric material ($\in_r$), and dielectric thickness (h). Since the impedances of the MODAMP™ MMICs are prematched to operate in a 50 ohm system, microstrip lines should be as close to 50 ohms as possible to realize full specified performance. Dimensions of 50 ohm line for some common board materials are shown in Table 1. Operation in systems with characteristic impedances other than 50 ohms is possible with somewhat reduced performance; in particular most MODAMP™ MMICs perform satisfactorily in 75 ohm systems without additional impedance matching.

Board Material Selection

A board material should be selected that is appropriate for the intended frequency of operation. Although G10 (epoxy-glass board) is an acceptable low cost choice for small signal, low frequency applications, inconsistencies in the dielectric (usually glass pockets) can cause problems at frequencies above 500 MHz, or with low impedance power stages built on the same board. PTFE woven-glass has much more consistent dielectric characteristics, and performs well to frequencies in excess of 2 GHz. It is also a fairly rugged material that can tolerate substantial rework, and is not particularly sensitive to heat or humidity.

Duroid is the favored material of many microwave designers because of its high dielectric consistency and low dielectric dissipation. Note that 50 ohm line on .015" RT/duroid-5870 is a particularly good match to the lead width of the 70 mil package, meaning minimal step discontinuity effects with this combination. RT/duroid is a somewhat fragile material—it crushes fairly easily, and glues do not adhere well to its substrate so thin metalization patterns are subject to lifting if abused with repeated rework. Some versions can also be quite hydroscopic, and can show substantial dielectric shifts with variations in humidity. Care should be taken when working with this material.

Table 1. Line widths for 50 ohm line for various board materials.

Board Material	∈	Thickness	w/h for 50Ω	w for 50Ω
RT/Duroid 5870[1]	2.3	.015"	2.90	.044"
PTFE-Woven Glass Fiber (Typ.)	2.55	.010"	2.55	.025"
		.031"	2.55	.079"
		.062"	2.55	.158"
Epoxy-Glass (G10)	4.8	.062"	1.75	.108"
Alumina/E10[2]	10.0	.025"	0.95	.024"
		.050"	0.95	.048"

[1] Trademark of Rogers Corp for its PTFE nonwoven glass PC material (RT is reinforced teflon and PTFE is polytetrafluorethylene)
[2] E-10 and Epsilam-10 are trademarks of 3M for its ceramic filled PTFE substrate

Table 2. Representative board material and thickness for various package options.

Package	04	20	35	70	85
Lead Width	.030"	.030"	.020"	.040"	.020"
Representative Board	G10 (.062")	PTFE (.031")	PTFE (.010")	5870 (.015")	G10 or PTFE (.062") (.010")

Alumina is an excellent high frequency material, but because it is a ceramic, it is expensive to process and requires etchants or a diamond scribe for line rework. It is the material of preference for hybrid circuits. Several manufacturers make soft board materials with dielectrics closely approximating those of alumina. These boards are also good choices for high frequency (>1 GHz) applications.

All boards must be plated on both sides. For soft boards, 1 oz. Cu plating is the most common choice. When etching the circuit pattern, the entire bottom side plating should be left intact to provide the best possible ground plane.

Parasitics

During board layout, care should be taken to minimize all parasitics. Remember that extra lead length equals extra inductance added to the design. This is particularly important if the circuit is to be operated above 1 GHz. Transmission lines should, whenever possible, run flush to the package. For some package options this will require that a hole be made in the circuit board so that the MODAMP™ MMICs' leads are in the same plane as the transmission line. MODAMP™ MMICs should be mounted on the etched side of the board to minimize the inductance of "fed through" connections. Abrupt changes in transmission line width also create parasitic effects, called step discontinuities. Although the complete model for such a discontinuity can become quite complicated, the overall effect of the step from a MODAMP™ MMIC lead to a 50 ohm transmission line is typically .05 to .2 nH of extra series inductance. Tapering the transmission lines from 50 ohms down to the MODAMP™ MMIC lead width helps minimize this effect. Bends in transmission lines also create parasitic effects and should be avoided when possible; when they must be used, the corners should be chamfered to prevent the bends from acting as extra shunt capacitance. For more information on the properties of microstrip structures, see K.C. Gupta, et al, *Microstrip Lines and Slotlines*, Artech House, 1979, Dedham, MA.

To illustrate how important parasitic effects can be, a "careful" design using a MSA-0204 on 1/16" PTFE woven-glass was simulated using a computer program and analyzed from 500 MHz to 3 GHz. Both step discontinuities and parasitic inductances were included in the model. The blocking capacitor was assumed to be a 100 pF, 0.1 inch square ceramic chip with infinate Q and an associated parasitic inductance of .9 nH. The analysis was of the input circuit mismatch only; assuming losses due to output mismatch are of a similar magnitude, the total amplifier loss would be about double that shown. To help distinguish the effects of parasitic mismatch from those due to device impedances, the simulation was also made of both the network with parasitics terminated in a "perfect" (50 + j0 ohm) device and of a MSA-0204 operated in an ideal (parasiticless) system. Table 3 shows the results of the analysis. In this case, amplifier gain loss ranges from negligible (less than .1 dB) at 500 MHz to nearly .4 dB at 3 GHz. Remember that the results shown are for minimal realistic parasitics. If the layout is "sloppy," impedance mismatches in excess of 2:1 and consequent amplifier gain decreases of 1 dB or more can be expected.

Table 3. Parasitic effects on input impedance mismatch of MSA-0204.

Frequency	MSA-0204, No Parasitics		Parasitics Only		MSA-0204 + Parasitics	
MHz	VSWR	Loss, dB	VSWR	Loss, dB	VSWR	Loss, dB
500	1.09:1	0.0	1.01:1	0.0	1.18:1	.03
1000	1.23:1	.04	1.12:1	.01	1.39:1	.11
1500	1.29:1	.07	1.22:1	.04	1 46:1	.15
2000	1.29:1	.07	1.30:1	07	1.45:1	.15
2500	1.26:1	.05	1.38:1	11	1 45:1	.15
3000	1.26:1	.05	1.45:1	.15	1.53:1	.19

Conclusions

The design techniques detailed in this paper are representative of typical CAE/CAD designs for achieving a working model. These techniques are especially important in anticipating circuit sensitivities to manufacturing tolerances. With computer technology rapidly improving engineering efficiency and accuracy, we will soon see computer-aided testing (CAT) available which will enable an engineer to take measured results from automatic network analyzers and *automatically* update the theoretical model.

The successful prediction of the actual performance of this RF amplifier demonstrates the accuracy of CAE/CAD products. The fact that engineers can now evaluate linear and nonlinear characteristics of circuits before they are manufactured dramatically saves both time and money.

APPENDIX A

CAD CIRCUIT FILES

```
! FILE :SP_SPAR
! GENERATE I-V curves and S-PARAMETERS FROM MWSPICE MODEL

DIM
  FREQ MHZ
  CAP  PF
  IND  NH
CKT
  MSUB ER=2.55 H=28.5 T=1.35 RHO=1 RGH=0.02
  MLIN_T1      1   2          W=300 L=500
  IND_LBIN     2   3          L=0.25
  CAP_CMATCH   3   0          C=345
  IND_LB       3   4          L=0.20
  S2PA_Q1      4   5   6      [MODEL=QNPN AREA=1.0]
  IND_LE       6   0          L=0.18
  IND_LC       5   7          L=0.05
  MLIN_T2      7   8          W=300 L=500
     DEF2P     1   8          TRAN
  TRAN_X1      1    2
     DEF2P     1    2         NET
MODEL
  QNPN  NPN     IS =1.5E-3 BF=85    VAF=52 IKF=80
              + ISE=4E-5   NE=1.35  VAR=6
              + RE =0.115  RC=0.35
              + RB=0.08
              + CJE=200pf VJE=0.20 MJE=3.5
              + TF =115PS XTF=3.5  VTF=3.0   ITF=4.5
              + CJC=115Pf VJC=0.22 MJC=0.185
SOURCE
       NET     ICS_IBB   0  1       DC=0.042
       NET     IVS_VCC   2  0       DC=19.0
CONTROL
       NET     DC IVS_VCC 0 22 1.0 ICS_IBB .020 .100 .020
       NET     AC LIN  7 170MEG 230MEG
       NET     OPTIONS ACCT LIST NODE LIMPTS=5e3
SPICEOUT
       NET     DC ALL
       NET     SP TRAN_X1   B:EESOF.S2P 50
```

Figure A-1. I-V and S-parameter circuit file.

Grounding

Perhaps the second most important consideration in PC board layout (after impedance matching) is good RF grounding. Ground planes should be kept as large and as solid as possible. Return paths for high frequency circulating currents must be kept as short as possible, especially at the "emitters" of the MODAMP™ MMICs. If, for example, plated through holes are used as ground returns, they should be placed directly under the ground leads of the MODAMP™ MMIC and be located as near as possible to the body of the package. This is because any additional path length here acts as series inductance, which translates into unwanted emitter resistance at operating frequencies. Gain, power compression, and high frequency rolloff will all be degraded if proper grounding techniques are not used. Fig. 3 shows a variety of ways of providing good return paths between topside ground connections and the bottom ground plane.

RF grounding. The device analyzed is the MSA-0135-21. Gain vs. frequency curves are shown for emitter inductances ranging from 0 to 4 nH.

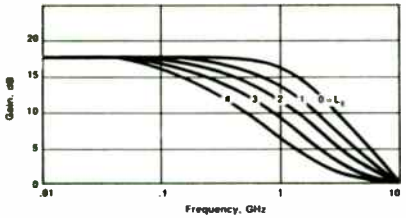
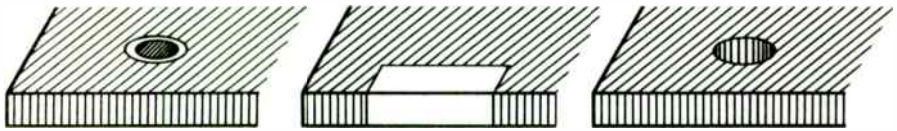


Figure 5. Gain vs. frequency as a function of emitter inductance (L_E) for the MSA-0135-21.



a. Wire "feed through" soldered in place in hole drilled through board

b. "Wrap around" of copper foil (may be used with slit in board)

c. Plated through hole (side walls of hole metalized).

Figure 3. Methods of realizing minimal length return paths to ground.

MODAMP™MMICs incorporating internal "collector" resistors (dash 1 option) help demonstrate how important good grounding is. These units give up one ground lead to allow the designer access to the internal resistor. As a consequence they sacrifice significant high frequency performance. The gain vs. frequency curves of the MSA-0270-12 (single ground lead) and the MSA-0270-22 (dual ground leads) shown in Fig. 4, demonstrate this performance tradeoff. Note the decrease in $f_{1\,dB}$ (the frequency at which the gain is 1 dB lower than the gain at 100 MHz) from around 1.6 GHz to below 1 GHz. Fig. 5 shows a further example of the effects of parasitic emitter inductance resulting from poor

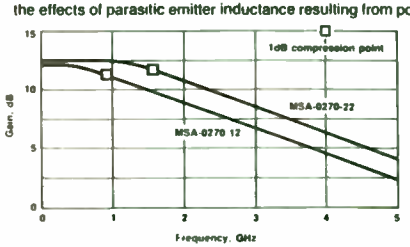


Figure 4. Typical gain vs. frequency for MSA-0270-12 and MSA—0270-22.

DC Blocking Capacitance

DC blocking capacitors must be used in both the RF input and the RF output lines to isolate the resistive bias circuitry of the MODAMP™ MMIC from the source and load resistances. These capacitors will also put limits on the frequency response of the finished amplifier. Low frequency response will be determined by the capacitor's value; it must be high enough to be a reasonable RF "short" at the lowest frequency of operation. High frequency response will be limited to the frequency at which the capacitor's associated parasitic inductance becomes resonant with the blocking capacitor ($1/(2\pi\sqrt{LC})$ Hz, where L = parasitic inductance in Henrys, and C = the capacitor value in Farads). Operation above this frequency often leads to highly unpredictable circuit behavior.

Fig. 6 shows typical effects of blocking capacitors on impedance match as a function of frequency, capacitance, and parasitic inductance. Note that low frequency match is determined by capacitor value, with the parasitic inductance having negligible influence; whereas at higher frequencies, the value of the parasitic inductor dominates the match, with the value of the capacitor becoming unimportant so long as it is large enough to be a low series impedance path. The ratio of capacitive reactance to parasitic resistance is called the Q of the capacitor. Blocking capacitors with high Qs should always be used to minimize insertion losses.

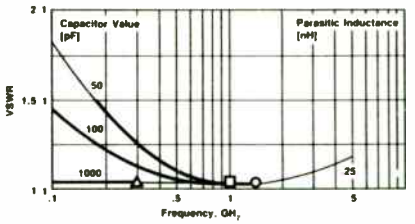


Figure 6a.

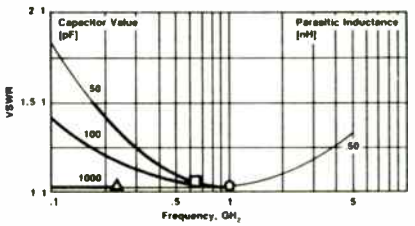


Figure 6b.

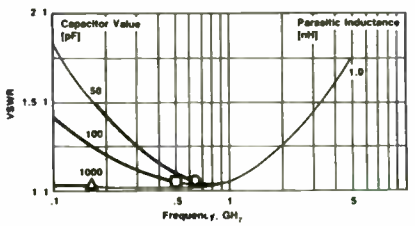


Figure 6c.

□ : resonant frequency, .25 nH parasitic inductance
○ : resonant frequency, 0.5 nH parasitic inductance
△ : resonant frequency, 1.0 nH parasitic inductance

Figure 6. Effects of DC blocking capacitors on VSWR as a function of frequency, capacitance and parasitic inductance.

Biasing

In order to deliver full performance, MODAMP™ MMICs must be biased correctly. The internal resistive networks determine individual transistor operating points; all the user needs to do is present the proper voltage at the DC input terminal. For the purpose of bias stability over temperature, the internal transistors should have their bias supplied through a collector resistor (labeled R_C in Fig. 1). This resistor works in two ways. First, it compensates for increases in device β with temperature by dropping the transistor's collector voltages whenever they try to draw more collector current. Coupled with this effect is the fact that the collector resistor will itself be changing in value over temperature. Resistors with positive temperature coefficients such as the common carbon composite (+.0001% per degree C) do an excellent job of compensating for the temperature drift of the negative coefficient on-chip resistors.

For bias stabilization over a temperature range of −10° to +100°C, a drop of at least 1.5 volts across the collector resistor is necessary. The larger this voltage drop is, the more stable the bias will be. An interesting point is that for a fixed bias (constant quiescent current vs. temperature), the gain of the MODAMP™ MMIC will decrease as temperature increases. A voltage drop of about 2V across the collector resistor allows the bias swing over temperature to compensate for this gain change, yielding best gain flatness over temperature.

Table 4 shows an example of how selection of the bias stabilization resistor influences performance over temperature. These results come from device simulations using PSPICE and correlate well with observed performance of actual amplifiers. Note that with no stabilization resistor the user risks having the MODAMP™ MMIC self destruct at elevated temperatures. In general, bias current will increase as temperature increases (due to increases in device betas with temperature); gain may either increase or decrease depending on how well the bias shift compensates for the decreased gain at a constant bias at higher temperatures.

Table 4. Effects of R_C on performance over temperature.

MSA-0104		Operating Voltage = 5.07 V Nom.		
Voltage Drop, volts	Resistor Value, ohms	Temperature degrees C	Bias Current, mA	Power Gain @ 100 MHz, dB
0	0	−10	9.5	−0.5
		25	18.4	18.8
		100	**	**
1.5	82	−10	14.2	17.0
		25	17.3	18.3
		100	24.1	19.0
2.0	100	−10	16.3	18.5
		25	18.9	18.9
		100	24.6	19.0
7.0	412	−10	16.1	18.3
		25	16.8	18.1
		100	18.3	17.5

** Device destroyed due to excessive current draw

The value of the bias stabilization resistor R_C is given by:

$$R_C = \frac{V_{CC} - V_d}{I_d} \text{ ohms}$$

where V_{CC} = the power supply voltage applied to R_C (in volts)
V_d = the voltage at the DC input terminal of the MMIC (in volts)
I_d = the quiescent bias current drawn by the MMIC (in amps)

The recommended values of I_d and V_d can be found on the individual MODAMP™ MMIC data sheets, both in the *Electrical Specifications* table and above the listing of S-parameters

The dissipation of this resistor is given by:

$$P_{diss} = I_d^2 \times R_C \text{ watts}$$

```
! ------------------------- E-SYN  07/21/86 -------------------------

!                    LUMPED CHEBYSHEV BANDPASS NETWORK
!                   FREQUENCY : 170.0000 to 230.0000 MHz
!    INPUT FILE  : EESOF.S2P
!    OUTPUT TERM : R = 50.00000 Ohms
!                          3 RESONATORS
!    0.010000 dB RIPPLE          0.542478 dB MIL          0.000000 dB SLOPE

! ------------------------------------------------------------------

                          R = 50.00000  Ohms
               PLC     1    0  L = 31.73057  nH  C = 10.57711 pF
               CAP     1    2  C = 15.38323  pF
               CAP     2    0  C = 27.30423  pF
               IND     2    3  L = 15.17621  nH
               CAP     3    0  C = 344.6401  pF
                          S = EESOF.S2P
```

Figure A-2. Synthesized input circuit created in E-Syn.

```
! ------------------------- E-SYN   08/26/86 -------------------------

!                    LUMPED CHEBYSHEV TRANSFORMER NETWORK
!                   FREQUENCY : 170.0000 to 230.0000 MHz
!    INPUT TERM  : R = 5.200000 Ohms
!    OUTPUT TERM : R = 50.00000 Ohms
!                          ORDER = 2
! ------------------------------------------------------------------

                          R = 5.200000  Ohms
               IND     1    2  L = 6.742091  nH
               CAP     2    0  C = 88.88526  pF
               IND     2    3  L = 23.11017  nH
               CAP     3    0  C = 25.93112  pF
                          R = 50.00000  Ohms
```

Figure A-3. Synthesized output circuit created in E-Syn.

```
! FILE:SP_CKT
! COMPLETE MODEL OF DEVICE AND COMPLETE CIRCUIT

DIM
  ! standard units of measure
CKT
  MSUB ER=2.55 H=28.5 T=1.35 RHO=1 RGH=.02
  MLIN_T1      1   2          W=300 L=500
  IND_LBIN     2   3          L=0.25
  CAP_CMATCH   3   0          C=345
  IND_LB       3   4          L=0.20
  S2PA_Q1      4   5   6      [MODEL=QNPN AREA=1.0]
  IND_LE       6   0          L=0.18
  IND_LC       5   7          L=0.05
  MLIN_T2      7   8          W=300 L=500
     DEF2P     1   8          TRAN

  CAP_CM1      1    0         C=10.58
  IND_LM1      1    0         L=31.73
  CAP_CM2      1    2         C=15.38
  CAP_CM3      2    0         C=27.30
  IND_LM2      2    3         L=15.18
  CAP_CM4      3    0         C=344.6
  TRAN_X1      3    4
! S2PA         3    4   0     B:EESOF.S2P
  IND_LM3      4    5         L=6.74
  CAP_CM5      5    6         C=680
  CAP_CM6      6    0         C=88.89
  RES_RM7      6    0         R=1E6
  IND_LM4      6    7         L=23.11
  CAP_CM7      7    0         C=25.93
  RES_RM8      7    0         R=1E6
     DEF2P     1    7         NET

MODEL
  QNPN  NPN     IS =1.5E-3 BF=85    VAF=52 IKF=80
              + ISE=4E-5   NE=1.35  VAR=6
              + RE =0.115  RC=0.35
              + RB =0.08
              + CJE=200pf  VJE=0.2  MJE=3.5
              + TF =115PS  XTF=3.5  VTF=3.0 ITF=4.5
              + CJC=115pf  VJC=0.22 MJC=0.185
```

Figure A-4. E-syn input and output networks combined and modified in Touchstone (page 1 of 2)

The power rating of R_C must exceed P_{diss}; if necessary, resistors with lower power ratings may be paralleled to achieve the necessary dissipation capability. Some MODAMP™ MMICS are available with the collector resistor on the chip. This has obvious size and parts count advantages. The tradeoff is for high frequency performance (see the discussion of grounding above) and bias flexibility (only one supply voltage will be appropriate for a given internal resistor value). Also, the on-chip resistors have negative temperature coefficients, and will not hold the MODAMP™ MMIC's bias as constant over temperature as will an external carbon resistor.

Chokes and Bypass Capacitors

It is recommended that an RF choke (large value inductor) be used in series with the bias stabilization resistor. Although the choke is not generally needed to keep the RF out of the DC (the relatively high impedance of the bias stabilization resistor compared to a 50 ohm load is sufficient for this), it is needed to keep the stabilization resistor from appearing in parallel with the load circuit, and thus degrading the output match. A good rule of thumb is that the impedance of the choke at the lowest frequency of operation (given by $2\pi \cdot F \cdot L$) plus the value of the stabilization resistor should be at least 500 ohms. A 10 μH inductor works well as a choke at frequencies as low as 10 MHz; it can be either a molded inductor (for low cost applications) or a chip inductor (in cases where space is at a premium). At lower frequencies several turns of wire on a high permeability ferrite bead should be used. If the choke is omitted, the designer should expect a gain loss of between 0.5 and 1 dB and a decrease in $P_{1\ dB}$ of as much as 2 dB from the guaranteed performance due to load impedance mismatch.

A large value bypass capacitor (1 μF or so) should be used in conjunction with the choke to present a low impedance path to ground for any signal that does manage to get past the choke. This capacitor should be attached between the supply side of the RF choke and ground.

Typical Circuit Layouts

Fig. 7 shows a typical MODAMP™ MMIC circuit board layout that uses the above construction techniques. The layout is for 1/32" PTFE woven-glass board—a reasonable compromise between cost, durability, and electrical performance. Note that the transmission lines have no bends and are tapered near the package of the MODAMP™ MMIC to minimize step discontinuities. Twelve plated through holes, including two under the emitter leads, provide solid ground planes and minimal emitter parasitics for best high frequency performance. The gaps in the transmission line are appropriate for 50 mil ceramic chip capacitors, which have relatively low associated parasitic inductances—typically about 0.5 nH. The DC pad arrangement requires that a bias stabilization resistor be used, but makes the use of an RF choke optional. If the choke is not used, the stabilization resistor would be connected between the output 50 ohm line and the V_{supply} line, and the bypass capacitor would be attached between the V_{CC} line and ground. Spacing is appropriate for ¼ watt carbon resistors, molded inductors, and 1 μF electrolytic capacitors. The layout has been designed so that the section between the arrows in Fig. 7 can be repeated for multiple cascaded stages. Overall circuit dimensions are 1" × 1.5" for a single stage, with each additional stage adding 1" to the overall length. The size was chosen for convenience of assembly; a more compact layout providing a three stage cascade of MODAMP™ MMICs in the same space and using chip resistors and inductors as shown in Fig. 9. Fig. 8 shows a circuit layout analogous to that in Fig. 7 for a MODAMP™ MMIC with the internal bias stabilization resistor.

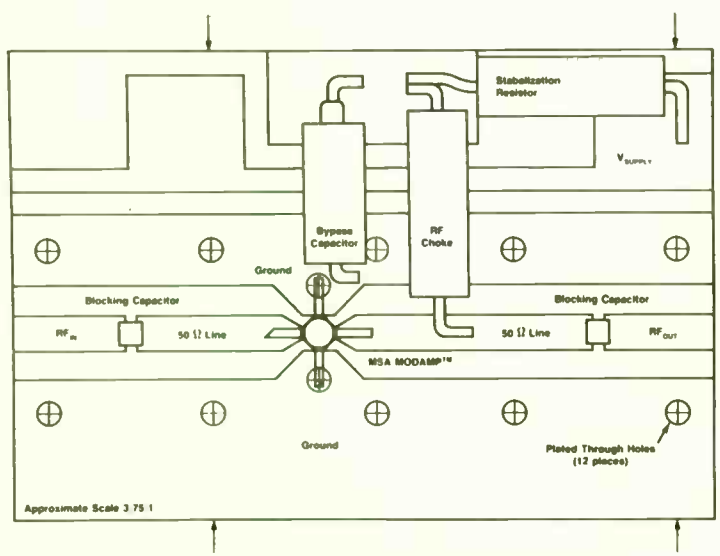


Figure 7. Typical MODAMP™ MMIC circuit (dual ground configuration).

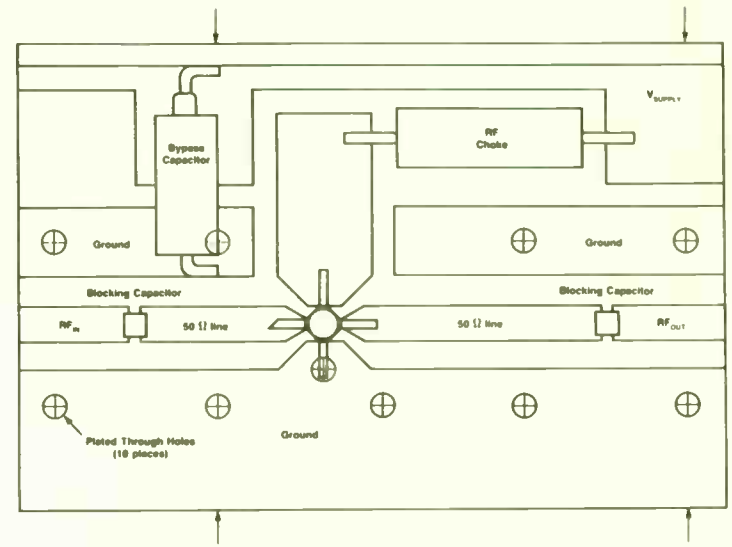


Figure 8. Typical MODAMP™ MMIC circuit (interal R_C configuration).

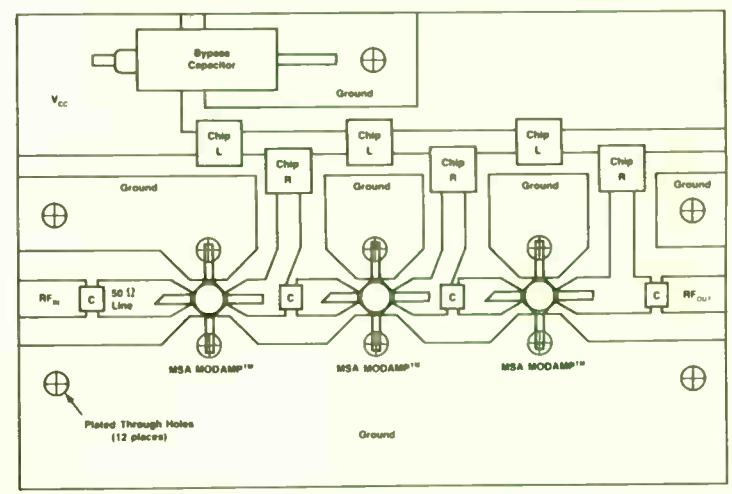


Figure 9. MODAMP™ MMIC circuit layout three stage cascade.

```
SOURCE
       NET     ICS_IBB   0 20       DC=.042
       NET     CAP_CB1  20  0       C=35E6
       NET     CAP_CB2  20  0       C=1E3
       NET     IND_LB1  20 21       L=500
       NET     CAP_CB3  21  0       C=470
       NET     IND_LB2  21  3       L=100

       NET     IVS_VCC  30  0       DC=19.0
       NET     CAP_CC1  30  0       C=35E6
       NET     CAP_CC2  30  0       C=1E3
       NET     IND_LC1  30 31       L=500
       NET     CAP_CC3  31  0       C=470
       NET     IND_LC2  31  4       L=100

       NET     IVS_VIN  40  0   AC=1.0 PWR=(30 30 0 1.7E8 2.3E8 .1e8)
       NET     RES_RIN  40  1       R=50
       NET     RES_ROUT  7  0       R=50
CONTROL
       NET     TRAN 40PS 25NS  0  40PS
       NET     PWR IVS_VIN RES_RIN
       NET     AC LIN 13 170MEG 230MEG
       NET     DC IVS_VCC 0 22 1.0 ICS_IBB .020 .100 .020
!      NET     FOUR 200MEG V(7)
       NET     OPTIONS ACCT LIST NODE LIMPTS=5e3
!      NET     TEMP 27.0
SPICEOUT
       NET     PWR RES_RIN 1 0 RES_ROUT 7 0
       NET     DC ALL
       NET     AC ALL
!      NET     SP TRAN_X1 B:EESOF.S2P 50
OUT
   NET DB[S21] GR1
   NET DB[S11] GR1A
   NET DB[S22] GR1A
   NET K
FREQ
  SWEEP 170 230 5
GRID
  RANGE 170 230 10
  GR1 5 15 1
  GR1A -20 -0
```

Figure A-4. E-Syn input and output networks combined and modified in Touchstone (page 2 of 2)

```
! FILE:SP2_CKT WITH COMPLETE CIRCUIT FILE DESIGN INCLUDING LAYOUT
VAR
  W50=189
DIM
! Standard units of measure
CKT
  MSUB ER=2.55 H=28.5 T=1.35 RHO=1 RGH=.02
! MLIN_T1      1   2          W=300 L=500
! IND_LBIN     2   3          L=0.25
! CAP_CMATCH   3   0          C=345
! IND_LB       3   4          L=0.20
! S2PA_Q1      4   5   6      [MODEL=QNPN AREA=1.0]
! IND_LE       6   0          L=0.18
! IND_LC       5   7          L=0.05
! MLIN_T2      7   8          W=300 L=500
!    DEF2P     1   8          TRAN
  MLIN         10   1         W^W50  L=524
  CAP_CM1      1    0         C=8              para
  IND_LM1      1    0         L=25             para
  CAP_CM2      1    2         C=14.5           PAD1 W^W50 S=200 L=900
  CAP_CM3      2    0         C=27.3           para
  IND_LM2      2    3         L=13             PAD1 W^W50 S=412 L=900
  CAP_CM4      3    0         C=344.6          para
  MLIN_T1      3    30        W=300 L=500
! TRAN_X1      3    4
  S2PA         30   40  0     B:EESOF.S2P      SPAC L=450
  MLIN_T2      40   4         W=300 L=500
  IND_LM3      4    5         L=2.2            PAD1 W^W50 S=200 L=426
  CAP_CM5      5    6         C=680            PAD1 W^W50 S=200 L=900
  CAP_CM6      6    0         C=88.89          para
  RES_RM7      6    0         R=1E6            para
  IND_LM4      6    7         L=19             PAD1 W^W50 S=390 L=900
  CAP_CM7      7    0         C=22             para
  RES_RM8      7    0         R=1E6            para
  MLIN         7    8         W^W50 L=500
     DEF2P     10   8         NET
MODEL
  QNPN  NPN      IS =1.5E-3 BF=85    VAF=52 IKF=80
              +  ISE=4E-5   NE=1.35  VAR=6
              +  RE =0.115  RC=0.35
              +  RB =0.08
              +  CJE=200pf  VJE=0.2  MJE=3.5
              +  TF =115PS  XTF=3.5  VTF=3.0 ITF=4.5
              +  CJC=115pf  VJC=0.22 MJC=0.185
```

Figure A-5. Final circuit file designed for layout generation (page 1 of 2)

```
SOURCE
       NET     ICS_IBB   0 20       DC=.042
       NET     CAP_CB1   20  0      C=35E6
       NET     CAP_CB2   20  0      C=1E3
       NET     IND_LB1   20 21      L=500
       NET     CAP_CB3   21  0      C=470
       NET     IND_LB2   21  3      L=100

       NET     IVS_VCC   30  0      DC=19.0
       NET     CAP_CC1   30  0      C=35E6
       NET     CAP_CC2   30  0      C=1E3
       NET     IND_LC1   30 31      L=500
       NET     CAP_CC3   31  0      C=470
       NET     IND_LC2   31  4      L=100

       NET     IVS_VIN   40  0   AC=1.0 PWR=(30 30 0 1.7E8 2.3E8 .1e8)
       NET     RES_RIN   40  1      R=50
       NET     RES_ROUT   7  0      R=50
CONTROL
        NET     TRAN 40PS 25NS  0  40PS
        NET     PWR IVS_VIN RES_RIN
        NET     AC LIN 13 170MEG 230MEG
!       NET     DC IVS_VCC 0 22 1.0 ICS_IBB .020 .100 .020
!       NET     FOUR 200MEG V(7)
        NET     OPTIONS ACCT LIST NODE LIMPTS=5e3
!       NET     TEMP 27.0
SPICEOUT
        NET     PWR RES_RIN 1 0 RES_ROUT 7 0
!       NET     DC ALL
!       NET     AC ALL
!       NET     SP TRAN_X1 B:EESOF.S2P 50
OUT
   NET DB[S21] GR1
   NET DB[S11] GR1A
   NET DB[S22]
   NET K
FREQ
  SWEEP 170 230 10
GRID
  RANGE 170 230 10
  GR1 5 15 1
  GR1A -20 -0
```

Figure A-5. Final circuit file designed for layout generation (page 2 of 2)

APPENDIX B

BIBLIOGRAPHY

[1] mwSPICE program, EEsof, Inc., Copyright 1985.

[2] H. K. Gummel and H. C. Poon, "An Integral Charge Control Model of Bipolar Transistors," Bell Systems Technical Journal, Vol. 49, pp. 827-852, May 1970.

[3] TECAP, Hewlett Packard, Copyright 1985.

[4] E-Syn program, EEsof, Inc., Copyright 1986.

[5] Touchstone program, EEsof, Inc., Copyright 1984.

[6] MiCAD program, EEsof, Inc., Copyright 1985.

[7] MICmask program, EEsof, Inc., Copyright 1985.

DESIGN OF DIELECTRICALLY STABILIZED OSCILLATORS USING FEEDBACK TECHNIQUES

by

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ABSTRACT

A simple model of a dielectric resonator FET oscillator stabilized with the resonator in the feedback path is presented. Based on this model a high efficiency, high Q DRO was developed in the 7 GHz frequency band. The oscillator has excellent frequency stability and noise performance. A mechanical frequency tunability of ± 50 MHz and power output of +18 dBm was achieved.

INTRODUCTION

Recent advances in the technology of temperature stable dielectric materials like Barium Tetratitanate and Zirconium - Tin Tetratitanate have inspired interest in techniques to dielectrically stabilize fundamental microwave oscillators.

Dielectric resonator oscillators (DROs) are highly compatible with modern microwave integrated circuitry. A sufficiently high output power, high frequency stability, small size and low cost are the features of a DRO. The resonator's high Q contributes to the DRO's excellent FM noise performance.

Oscillators stabilized by a dielectric resonator coupled to the output circuit one-half wave length away from the FET ("passive" injection locking) do not give as high loaded Qs and stability as feedback DROs (series or shunt) exhibit.

The development of fundamental microwave oscillators using a dielectric resonator for shunt feedback has been reported in recent articles. This technique has tended to be empirical in nature, often at the design stage itself. This paper presents a design approach which has been found to be both predictable and sufficiently accurate. Using an approximate feedback model, it was possible to calculate the lengths and impedances of the feedback microstrip elements required to sustain oscillation, with the dielectric resonator completing the feedback loop. DROs for the 7 GHz and 13 GHz frequency bands were developed using this modeling technique. The test results of the 7 GHz DRO only have been included in this paper. The preliminary results obtained for the Ku band have been encouraging.

DESIGN

The basic schematic of an oscillator is shown in Figure 1. The condition for oscillation is given by

$$\Gamma_R S_{11}' = 1 \quad \text{OR} \quad \Gamma_L S_{22}' = 1$$

The two conditions being equivalent [2], we choose

$$|\Gamma_R||S_{11}'|\, e^{j(\theta_R + \theta_{S_{11}'})} = 1$$

The magnitude and phase conditions are given by

$$|\Gamma_R||S_{11}'| = 1 \quad \text{AND} \quad \theta_R + \theta_{S_{11}'} = 0$$

For oscillations to build up it is required that $|\Gamma_R||S_{11}'| > 1$. The microstrip resonator has low losses and hence it is sufficient if S11' can be made greater than unity at the input

LOW-NOISE PREAMPLIFIER DESIGN FOR NMR

by

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1. INTRODUCTION

An important component in any nuclear magnetic resonance (NMR) imaging or spectroscopy system is a low-noise preamplifier. The required minimization of its noise figure can be obtained only by careful design. It must go hand in hand with an optimization of the "noise figure" of the NMR receive coil. The latter requires that the coil quality factor Q is made as high as possible. Other receiver system components such as cables, protection circuits, matching networks, transmit/receive (T/R) switches etc. should not be neglected in a low-noise design. They can easily add many tenths of a dB to the overall receiver noise figure.

2. QUALITATIVE LOW-NOISE DESIGN

The most critical item in a low-noise preamplifier is its input device. Bipolar transistors have the advantage to provide a relatively large bandwidth at higher frequencies (20-200 MHz). They must be selected for a high current gain, a large gain-bandwidth product FT of several Gigahertz and especially a low base-region bulk resistance. The latter can be reduced by paralleling two or more transistors. Due to their high input impedance junction field-effect transistors are suitable for low-noise narrow-band preamplifiers. They should exhibit a high transconductance which increases with the electron mobility in the channel. Since the latter is much higher in gallium-arsenide than in silicon GaAs-MESFET's are also good candidates for low noise NMR preamplifer designs.

As far as circuit design is concerned, the following rule should be obeyed: Eliminate all parasitic series or parallel impedances between base-emitter or gate-source terminals. This implies that, for example, by-passed emitter resistors must not be used and biasing resistors have to be chosen very high compared to the transistor input impedance.

3. QUANTITATIVE DESIGN

The expanded noise equivalent circuit of a preamplifier or its input transistor is shown in Figure 1. Ys=Gs+jBs is the source admittance producing the noise current Is. Y=G+jB is the input admittance of the noise-less (F=1) ideal amplifier of voltage gain A. The amplifier noise is in good first-order approximation represented by the input related equivalent noise voltage and current generators V and I. At higher frequencies they may be partially correlated, an effect which can be represented by the additional current generators (YC)V=(GC+jBC)V where YC is the so-called correlation admittance. Table 1 summarizes the important noise formulas. The noise figure F defined as the ratio of the total amplifier output noise power to the output noise due to the source resistor only is given by Equation 1. F is minimized by chosing an optimum source admittance Ys=Gs+jBs as given by Equation 3. The minimum noise figure obtainable is expressed in Equation 4. The following relationship

of the two port network.

For the NEC GaAs FETs used in the 7 GHz and 13 GHz bands, /S 11/ is between 0.2 to 0.8. Shunt feedback is developed to make /S11'/ > 1 for the condition of oscillation to be met.

The characterization of the feedback network (Figure 2) proceeds as follows. For the chosen electrical length θ1 and impedance Z1, and from the measured S parameters of the device, the Y parameters (say [Y1]) of the combination of the device and output microstrip element are obtained. It is assumed that at resonance, the dielectric resonator is purely resistive (R). For modeling purposes it is also assumed that the dielectric resonator is placed at the end of microstrip element (θ2,Z2), θ2 away from gate of the FET. For the chosen θ2, Z2, and a value of R, the Y parameters (say [Y2]) of the combination of microstrip and dielectric resonator are calculated. Adding [Y1] and [Y2] gives the overall Y parameters of the feedback network with the active device. The new S parameters are derived from this.

The lengths of the microstrip elements θ1 and θ2 are chosen depending upon the mechanical configuration of the active device and the circuit topology. A simple computer program was developed to check oscillation conditions for different values of θ1, θ2, Z1, Z2 and R. The value of R is dependent on the coupling coefficients β1 and β2 between the dielectric resonator and microstrip lines. An optimum coupling is required as weak coupling results in lower output and a tendency to cease oscillations at higher temperatures, while very tight coupling effects the frequency stability. θ1, θ2, Z1 and Z2 are varied to get the condition of /S11'/ >1. A complex conjugate is presented at the gate to determine the frequency. Load matching at the output is optimized for a good RF power.

FABRICATION AND PERFORMANCE

The DRO was fabricated on Teflon (1/32") fibreglass board (Er = 2.54). The biasing arrangement is as shown in Figure 3 with a chip capacitor on the output side for a DC block. The dielectric resonator is magnetically coupled in the TE 018 mode to the gate and drain microstrip lines. The resonator acts as a bandpass filter whose centre frequency can be tuned by varying the gap between the top lid and the dielectric. The exact positioning of the dielectric is critical and a purely empirical approach has been followed to obtain high frequency stability and a sufficiently high power output. The DRO was free from mode jumps and hysteresis. A chip resistor of 50 ohms terminating the gate circuitry was used to eliminate spurious oscillations.

The frequency stability of the DRO was within ±400 kHz over 0°C to 55°C at a centre frequency of 7410 MHz. The frequency drift over temperature can be adjusted by proper choice of the resonator temperature coefficient. A resonator with a positive temperature coefficient of 6 ppm/°C was used in the oscillator. The output power variation remained within ± 0.8 dB over the entire temperature range, as shown in Figure 4. Figure 5 shows the variation of frequency as a function of air gap thickness h.

(Equation 5) shows that the noise figure has a parabolic dependence on the source susceptance Bs. The same is partially true for Gs. It is interesting to note that the formulas for F do not explicitly depend on the input admittance Y. Its effect is contained in the noise generators V and I. In many cases, especially at lower frequencies, the correlation admittance Yc is negliglible. The optimum source conductance Gc(opt) is then given by the simple expression I/V.

4. OPTIMUM SOURCE ADMITTANCE

The analysis suggests a simple algorithm for determining the optimum source admittance Ys(opt) to minimize the noise figure F:

a. Determine the preamplifier input admittance Y=G+jB.
b. Measure the output RMS noise voltage VL(Gs=oo) for a shorted input and VL(Gs=o) for a open-circuited input.
c. Determine from Equation 6 a trial optimum source conductance Gs(opt).
d. Measure the noise figure with this source resistor as a function of parallel source susceptance Bs. The value of Bs which minimizes the noise figure is Bs(opt)=-Bc.
e. Repeat step b with Bs=-Bc and obtain the final value of Gs(opt) which will not be much different from the previously determined one.

It is interesting to note that Bs(opt) is independent of Gs and that in the above procedure it was not necessary to determine the correlation explicitly. Note that if there is no correlation (Yc=0) then the optimum source impedance is real and simply given by Rs=1/Gs=V/I.

In order to minimize the preamplifier and the NMR system noise figure it is now important that the receiver coil input impedance is matched by a transformation network to the optimum source admittance given by Equation 3 or 6 in Table 1. The question may arise: What should the input impedance Y of the preamplifier be? Since the formulas for the noise figure and the optimum source admittance Ys(opt) are independent of Y the answer is: It does nor matter as long as the source , in an NMR system the receiver coil, is matched to Ys(opt). Since the input impedance of NMR head or body receiver coils is dependent on the size of the patient to be imaged one can use a variable matching network in order to minimize the noise figure or one should use a preamplifier with a very low F.

5. MEASUREMENT TECHNIQUES

Since most NMR system operators have liquid nitrogen available in their facilities the so-called two-temperature method of noise figure measurement is very suitable. The preamplifier output noise voltage is measured with the source resistor Rs=1/Gs first at room temperature T1, (V1), and then dipped into liquid nitrogen (T2=77 degree Kelvin, V2). From the curve of Figure 2 (courtesy Dr. Howard Hart, GE-CRD) and the output noise voltage ratio V2/V1 the noise figure F is obtained. The advantage of this method is its low cost and its suitability for noise measurements in a complete NMR system. It also permits an easy determination of F as a function of source resistance without impedance transformation networks. Accurate measurements can be made with the fine HP-8970A noise figure meter (10-1500 MHz), but only in a 50 Ohm system. A comparison between the two methods resulted in good agreement For all NMR low-noise preamplifier measurements one should use only the HP346A and not the 346B noise source.

Excess tuning causes sharp output power variation, a fall in loaded Q and mode separation problems. A tendency to mode jump is seen for very low values of h. Moreover close proximity of the tuning screw over the dielectric degrades temperature stability performance. The mechanical tuning range was limited to ± 50 MHz in keeping with practical considerations.

The use of a quartz spacer is recommended for improving the loaded Q [4]. The diameter to height ratio of the dielectric resonator has to be properly chosen for optimum mode separation or spurious oscillations at other modes are possible for an improper selection of D/H ratio. When the dielectric is coupled between the feedback microstrip lines, oscillation over a range of ± 50 MHz of dielectric resonant frequency is possible depending upon the position of the dielectric from the drain port and also on the tightness of coupling. The frequency of the oscillator is set for a slightly higher value than the resonant frequency of the dielectric. Sweep measurement results conducted for the resonator coupled between parallel microstrip lines gave loaded Q values ranging from 800 to around 1000 depending upon the closeness of the lines with the dielectric. It is imperative that the resonant frequency and Q measurement of the resonator be made using a box with the same mechanical dimensions as that of the oscillator. The same microstrip layout was used for fabricating oscillators with centre frequencies from 7.2 to 7.8 GHz. The thickness of the dielectric and its positioning alone had to be varied to construct the oscillators. Repeatability of the oscillators was excellent and final placing of the dielectric resonator was optimized rapidly.

EFFECT OF BIASING

At lower values of gate voltage the frequency pushing was less. In the configuration used the frequency dependence on gate voltage was considerable. A pushing figure of approximately 1 MHz/Vgs and 300 kHz/Vds was obtained. At higher values of gate voltages, pushing was 3 MHz/Vgs. The pushing figures for a free running oscillator constructed with the same device read 80 MHz/Vgs and 3 MHz/Vds.

The measured FM noise at 10 kHz from carrier was -97 dBc 1 Hz BW (Figure 7). A harmonic rejection of greater than -30 dBc and spurious rejection more than -60 dBc was obtained.

A dielectric resonator feedback GaAs FET oscillator has been developed which exhibits:

(1) A frequency stability of better than ± 2.5 ppm/°C.

(2) Mechanical tunability of ± 50 MHz of centre frequency.

(3) FM noise of better than -97 dBc at 10 kHz from carrier, 1 Hz BW.

(4) A stable power output over 0 to 50°C and over the tuning range.

ACKNOWLEDGMENT

Our thanks are due to A.K. Sekhar and Eswarappa for the many useful discussions we had with them. We also wish to thank K.R. Shantharam, N.K. Ramesh and H.R. Keshavamurthy for the assistance given in fabricating the DRO.

6. RESULTS: NOISE FIGURE MEASUREMENTS

In Figure 3 the measured noise figure is shown as a function of source resistance Rs=1/Gs for a preamplifier of a low-field NMR system (0.12 Tesla, 5.1 MHz). A cascode configuration of 2 junction field-effect transistors (U-310) is used in the input stage. The optimum source resistance is approximately 750 Ohm. Feedback damping has been employed in order to increase the bandwidth of the receiver coil without degrading the noise performance too much. It is interesting to note that Rs(opt) remains the same with and without feedback (RF=00) whereas the input impedance changes drastically from 1700 Ohm, -82 degrees to 250 Ohm, 22 degrees. This preamplifier was connected directly to an NMR receive coil tuned to Zin=750 Ohm. For RF=00 a noise figure of F=0.5 dB and for RF=20 kohm//1pF, F=0.7 dB was obtained. These measurements demonstrate also that the optimum source resistor is for junction field-effect transistors relatively high. Figure 4 shows F at 5.1 MHz as a function of the source admittance phase angle. For Ø=+-45 degree a capacitor or inductor having a reactance of of X=1000 Ohm was connected in parallel to a source conductance of 1mS. The minimum of the noise figure F occurs for Ø=0 indicating that the correlation admittance Yc is zero. This means that the input related noise voltage and current generators V and I in the equivalent circuit of Figure 1 are uncorrelated. The curve demonstrates that even relatively small deviations from the optimum source conductance by a capacitive or inductive component results in a noise figure degradation of several tenths of a dB. One concludes that for noise optimization it is necessary to control especially the phase angle of the source admittance Ys. In practical terms this means that a few undesired picofarads in parallel to a preamplifier input can degrade F. On the other hand Figure 3 demonstrates that deviations from Gs(opt) are not that critical because that curve has a relative broad minimum. Figure 5 shows the circuit diagram of this J-FET preamplifier.

At higher frequencies bipolar transistors can be used, especially if a large bandwidth is desired, for example for a preamplifier covering the imaging and the spectroscopy frequencies. (64, 59, 26, 16 MHz). Their optimum source resistor is much lower (Rs(opt)=40...100 Ohm). Figure 6 shows the frequency response of the noise figure for an amplifier using MA-42197 bipolar devices demonstrating that F-values of less than 1 dB can be achieved over a large frequency range. In Figure 7 the noise figure is plotted as a function of the source resistor and the source susceptance for 64 MHz.

Figure 8 demonstrates an example of a preamplifer for which the correlation admittance Yc is not zero. The minimum noise figure occurs for a source susceptance of Bs=-3mS. (Parallel inductance with a reactance of XL=330 Ohm). By not neglecting the correlation effect expressed by the correlation admittance Yc one obtains in this case a noise figure improvement of about 0.2 dB. This amplifier used a by-passed emitter resistor in the first stage which probably caused the noise correlation.

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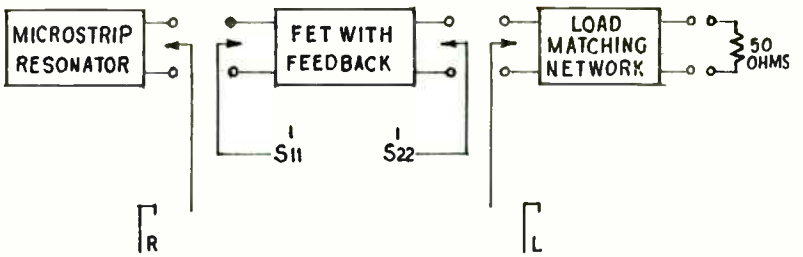

FIG.1 SCHEMATIC OF OSCILLATOR CIRCUIT

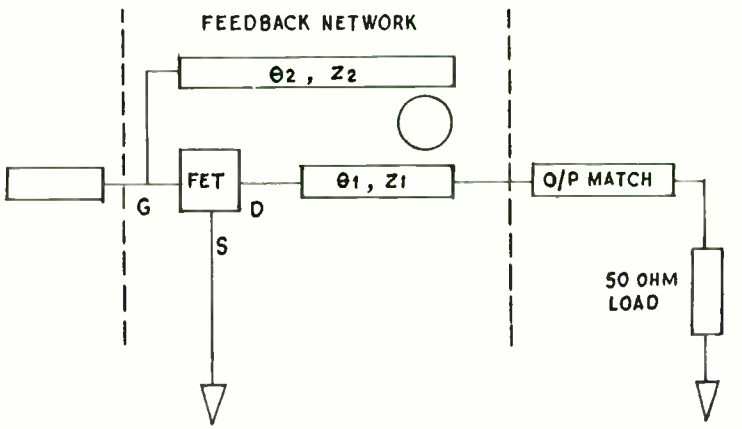

FIG.2 DESIGN MODEL

7. SUMMARY AND CONCLUSION

In order to obtain good NMR image quality low-noise preamplifiers are required. With careful design and by providing the optimum source impedance noise figures of 0.5 dB can be achieved. At higher frequencies the correlation between V and I in the noise equvalent circuit should not be neglected if the noise figure is to be minimized.

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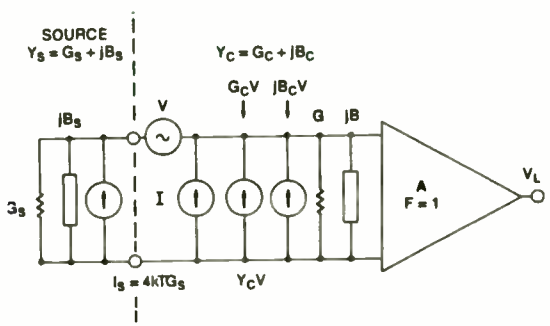
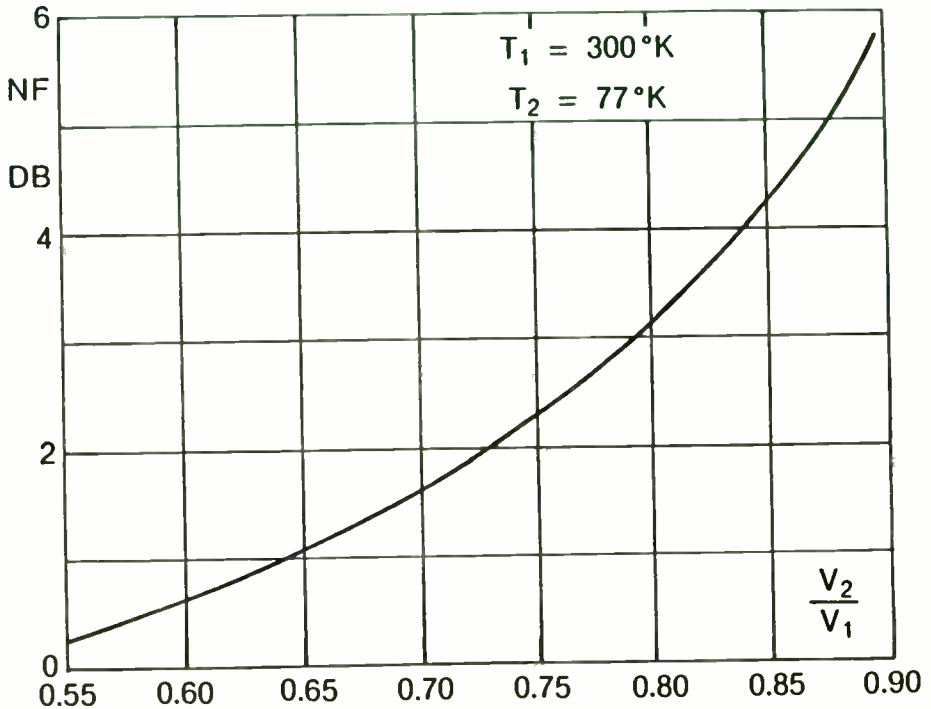


EQUIVALENT AMPLIFIER NOISE CIRCUIT INCLUDING CORRELATION BETWEEN VOLTAGE AND CURRENT NOISE SOURCES

FIGURE 1



LIQUID NITROGEN METHOD: NOISE FIGURE AS A FUNCTION OF THE NOISE VOLTAGE RATIO V_2/V_1.

FIGURE 2

①	$F = 1 + \frac{V^2\lvert Y_S+Y_C\rvert^2 + I^2}{I_S^2}$ = MINIMUM	
②	$\partial F/\partial B_S = 0$	$\partial F/\partial G_S = 0$
③	$B_S(OPT) = -B_C$	$G_S(OPT) = \frac{\sqrt{I^2 + G_C^2V^2}}{V}$
④	$F_{MIN} = 1 + \frac{V^2}{2kT}(G_S(OPT) + G_C)$	
⑤	$F = F_{MIN} + \frac{V^2}{4kTG_S}\left[(G_S(OPT) - G_S)^2 + (B_S(OPT) - B_S)^2\right]$	
⑥	$Y_C = 0$:	$G_S(OPT) = \lvert G + jB\rvert \cdot \frac{V_L(G_S=0)}{V_L(G_S=\infty)}$

TABLE 1: NOISE FORMULAS

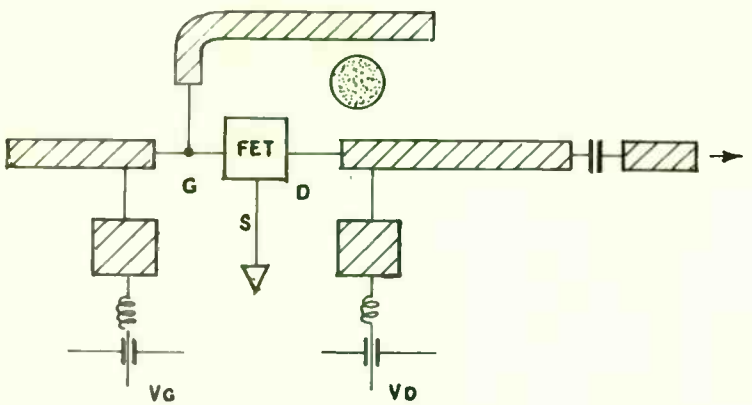


FIG. 3 DRO TOPOLOGY

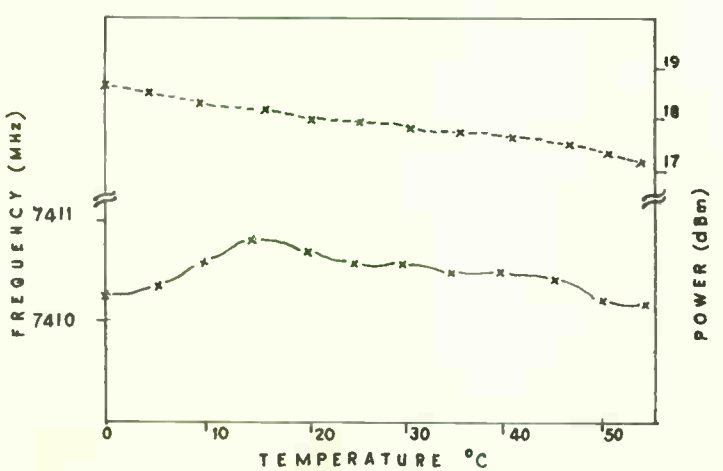


FIG. 4 OSCILLATION FREQUENCY AND POWER OUTPUT OVER 0 TO 50°C

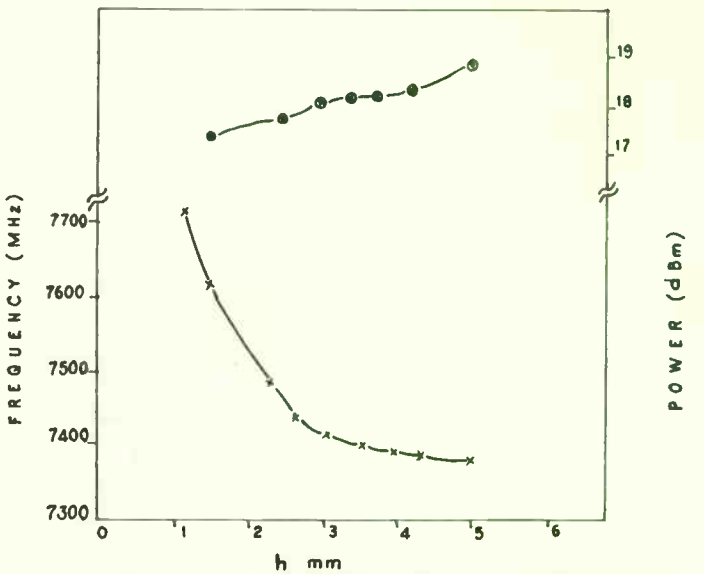


FIG. 5. MECHANICAL TUNING AS A FUNCTION OF AIR GAP THICKNESS (h)

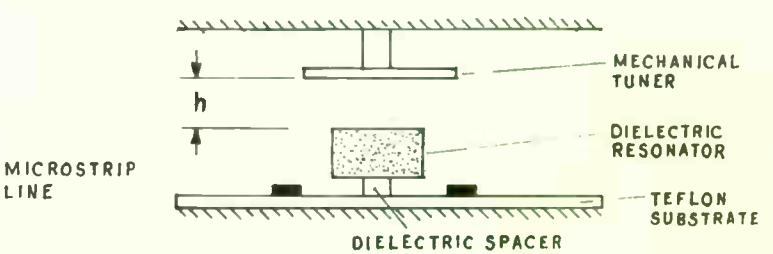
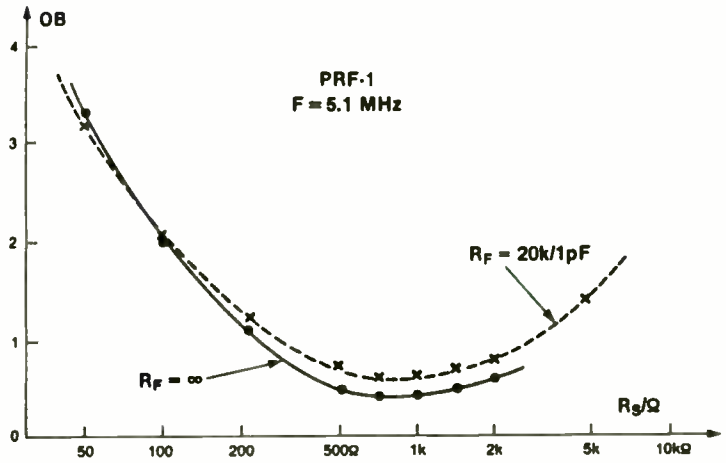
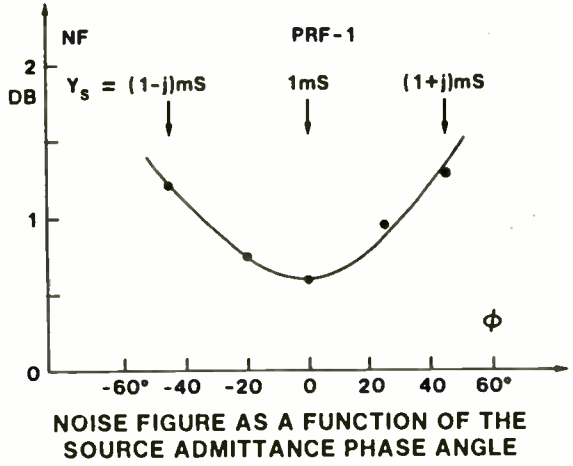


FIG. 6 SIDE VIEW OF DIELECTRIC RESONATOR COUPLED BETWEEN FEEDBACK MICROSTRIP LINES



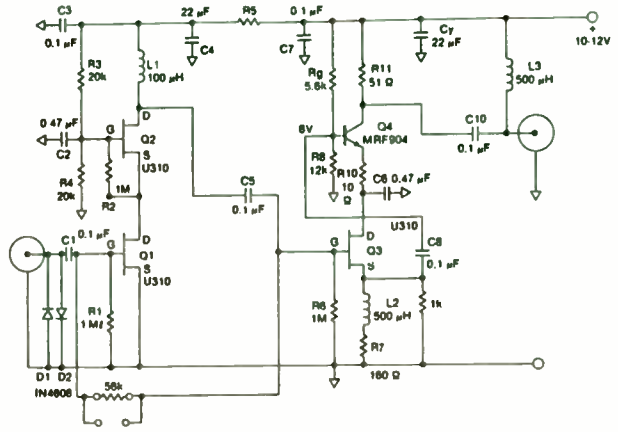
NOISE FIGURE VS SOURCE RESISTOR

FIGURE 3



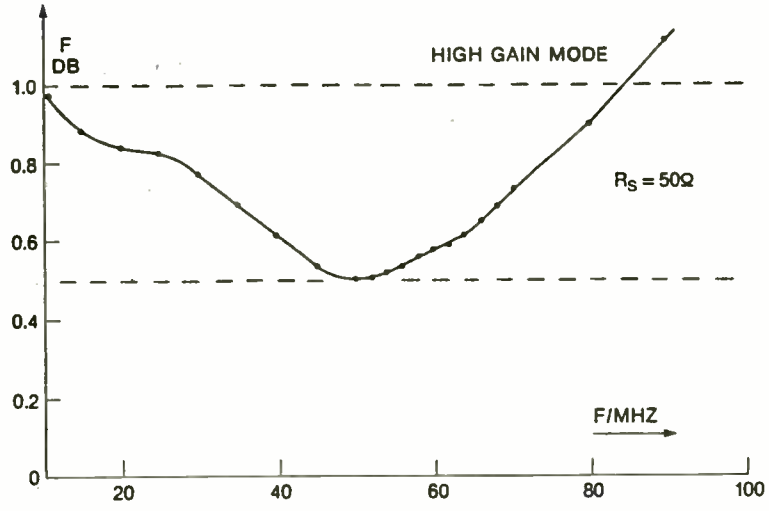
NOISE FIGURE AS A FUNCTION OF THE SOURCE ADMITTANCE PHASE ANGLE

FIGURE 4



LOW-NOISE PREAMPLIFIER
PRF-1

FIGURE 5



LNA-V-1: NOISE FIGURE F VS FREQUENCY

FIGURE 6

DOUBLE SIDEBAND DEMODULATED FM NOISE
PER 3.1 kHz BAND WIDTH
200 kHz rms DEVIATION = 0dB = 1mW

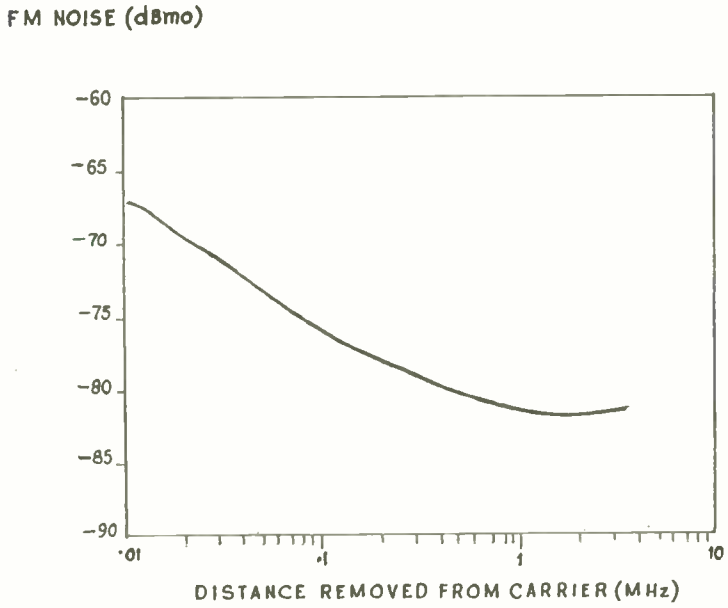
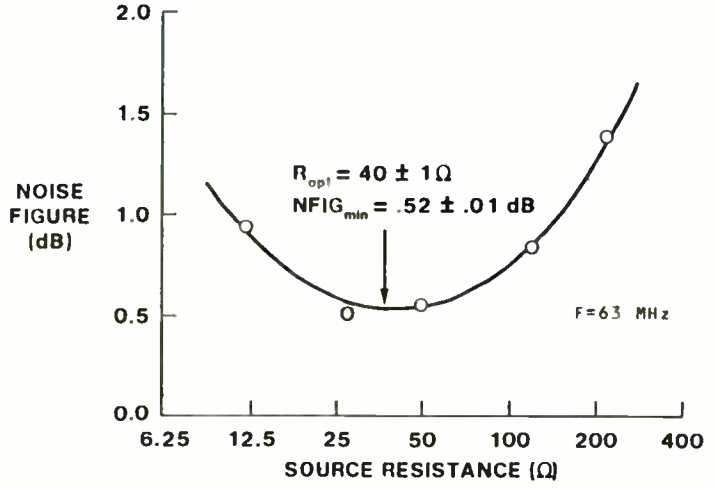
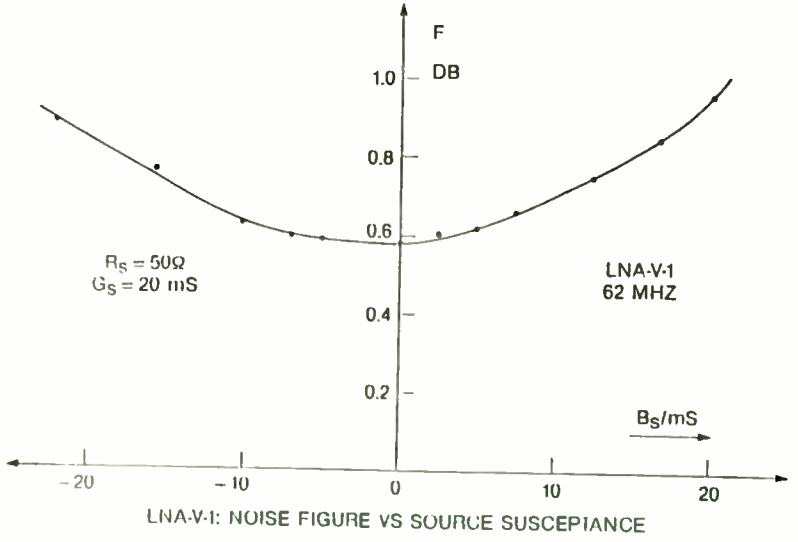


FIG. 7

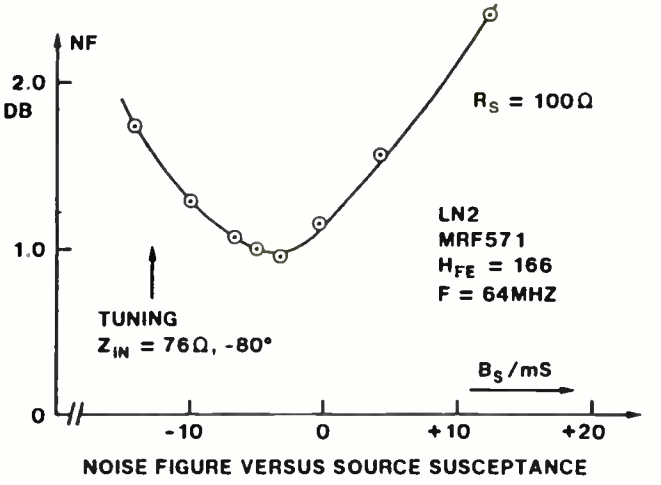
NOISE FIGURE VS. SOURCE RESISTANCE FOR LOW NOISE PREAMPLIFIER





LNA-V-1: NOISE FIGURE VS SOURCE SUSCEPTANCE

FIGURE 7



NOISE FIGURE VERSUS SOURCE SUSCEPTANCE

FIGURE 8

IRON POWDER CORES FOR HIGH Q INDUCTORS

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SUBJECT: A brief overview will be given of the development of carbonyl iron powders. It will be shown how the magnetic properties of a given iron powder will effect inductor performance and, through example, how the physical size of a core along with its winding details interact to effect Q versus frequency characteristics.

INTRODUCTION: A circuit designer is often faced with a need for inductors and transformers. Regardless of whether it is decided to make or buy these components, it is valuable to have a practical understanding of the parameters that affect their performance.

In the last century the use of solid magnetic material for DC electromagnetics and later laminated magnetic materials for low frequency applications led to the need for materials that would operate efficiently at higher and higher frequencies. With the original thick laminations it was discovered that the apparent permeability or inductance decreased as frequency increased and, at the same time, losses became prohibitive. It was found that by using thin sheets of material insulated from one another that better results were obtained. This is primarily due to an effect known as eddy current shielding. As frequency increases the depth of magnetic penetration decreases for any given material. Thus by having thin sheets, effectively, more of the core body is utilized. This progression worked toward thinner laminations and grain oriented alloys to meet the higher frequency needs.

While the thin oriented laminations were useful for broadband audio transformers, they were unable to meet the need for selective circuits where high Q is required. While at low frequency the magnetic field in a coil is in its axial direction, at high frequency, each turn generates its own field concentric with the wire. These fields are coupled with fields from adjacent turns and are coupled to the core through axial fields rather than one central field. This type of field requires cores laminated in all directions in order to minimize losses and thus maintain reliable inductance and Q versus frequency. As a result, powdered iron cores were developed.

There are two basic classes of iron powders available; Hydrogen reduced irons and carbonyl irons. The hydrogen reduced irons have low resistance, and a relatively large particle size. This type of powder produces the highest permeabilities, (approaching 100), has low losses at low frequency, but the losses increase significantly at high frequency, producing very low Q at RF. Cores from this powder are commonly used for differential-mode chokes in line filters and DC output chokes in switching power supplies.

The carbonyl irons, on the other hand, have a particle which is formed by the decompositon of pentacarbonyliron vapor. This produces a spherical particle with an onion skin structure. The laminating affect of the onion skin produces a resistivity of the individual particles which is much higher than that of pure iron. This high resistance in conjunction with the very small particles size (3 to 5 microns) greatly enhances the high frequency performance. The permeability of carbonyl iron powders, and thus their inductance, can be manufactured to a very tight tolerance and they remain extremely stable with frequency, temperature, and applied signal level. All of these are important considerations in high Q selective circuits.

The distributed air-gap characteristic of the carbonyl iron powder produces a core with permeabilities ranging from 4 to 35. This feature in conjunction with the inherent high saturation point of iron makes it very difficult to saturate at high power RF. Normally, high power applications are limited by temperature rise due to core loss.

In the middle 1930's the first ferrites were investigated. The development of these materials produced higher permeabilities than that attainable with iron powder and, at the same time, they had reasonable losses. In many applications the higher permeability of the ferrite materials is a distinct advantage. However, with high frequency and high Q tuned circuits, high permeability is not nearly as important as attainable Q and good stability with varying environmental and electrical conditions.

A Complex Impedance Meter

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Carpinteria, CA 93013-2918

The idea of this instrument was conceived through the better understanding of the Smith chart that I was able to receive in the late '70s. It took a few years, until around 1980, to get around to building one, verifying the concept. I remember that it was an antenna that defied tuning, and a 2-meter version of the instrument was built.

As is apparent in the Smith chart, all mismatches reflect power. At an open end of a transmission line a voltage maximum will occur. This corresponds to a point at the right edge of a Smith chart. At a shorted end there will be a voltage minimum (the left edge), and in the case of a perfect match, there will be equal voltage along the line (chart center). Correspondingly, loads with some imaginary part, inductors and capacitors combined with the load, will move vertically from the center, inductors up and capacitors down. They will not move on a straight line, like their resistive counterparts, but along some resistive circle, and the unity circle if the resistive part is a match. In the vicinity of the center, this vertical movement is approximately a straight line. How do we detect and indicate these deviations, then?

A wise man, Magnus Koch at the Chalmers U. of Technology, Göteborg, Sweden once told me, "If you can measure something with a bridge, do it!" As the years have gone by, I have found them to be words of wisdom, and they certainly apply here. A bridge, how to make a bridge that can detect in what direction something takes off on a Smith chart?

One does not have to! As you go along a transmission line away from, say a shorted end, you start at the leftmost end, and we all know that after $\lambda/8$, looking back, we will see an inductance with $j\omega L = Z_o$. After another $\lambda/8$, making $\lambda/4$ total, it looks like an open circuit, and so on. After one turn around the chart we have traveled $\lambda/2$ along the line. Let us now put four little detector diodes, monitoring the voltage on the line, spaced $\lambda/8$ apart, one in each "compass direction" around the chart. Well, you say, you can not do that! It introduces a mismatch! True, but all four diodes do the same. Since they are mutually cancelling, AT THAT FREQUENCY, plus a little line loss, it does not matter.

Let us excite the line and try various loads at the other end. The last diode is to be positioned where the loads will be applied, or an integer multiple of $\lambda/8$, in which case the indicators will change sign and label.

Referring to the basic schematic, Figure 1, let us look at a short circuit. D4 will obviously get no voltage at all to detect, but D2 will get twice the normal. D3 and D1 will not see any change. Due to the way D2 and D4 are turned, a negative voltage will appear at their summing point. An open circuit will produce the opposite, with a positive voltage from D4 and no voltage from D2. In both cases, D1 and D3 will detect equally strong

Ferrites are typically manufactured to a +/-20% tolerance.

INDUCTANCE: The inductance per turn of a closed magnetic structure, like a toroidal core, is described by:

$$\frac{L}{n^2} = \frac{4\pi u A_e}{l}$$

where: L = inductance in (nH)

u = permeability

A_e = cross-sectional area (cm^2)

l = path length cm

n = number of turns

This illustrates that the inductance per turn of a core is directly related to its permeability and the ratio of its cross-section to its path length. Core manufacturers provide an inductance rating for their cores. There are 3 different descriptions commonly used: nh/t, mh/1000t, and uh/100t. Because the inductance varies, squared with turns, the three compare according to this example:

5nh/t = 50 uh/100 turns = 5mh/1000 turns

These ratings are used to calculate the required turns for a desired inductance as follows:

If Al is in nh/t,

$$\text{required turns} = \left[\frac{\text{desired L (nh)}}{Al}\right]^{\frac{1}{2}}$$

If Al in mh/1000 turns,

$$\text{required turns} = 1000\left[\frac{\text{desired L (mH)}}{Al}\right]^{\frac{1}{2}}$$

If rated in uh/100 turns;

$$\text{required turns} = 100\left[\frac{\text{desired L/uh}}{Al}\right]^{\frac{1}{2}}$$

For example, if 3uh is needed on a core with an inductance index (Al) of 49uh/100 turns then;

$$\text{required turns} = 100\left[\frac{3}{49}\right]^{\frac{1}{2}} = 24.7 \simeq 25 \text{ turns}$$

Q CONSIDERATION: What are some of the considerations for producing high Q inductors? What is Q? In a simplified view $Q = \tan\theta = wL/R$ where θ is the phase angle, wL is the inductive reactance and R is the effective series resistance. In the ideal inductor, the phase angle is 90 degrees and the Q is infinite. Likewise, an inductor with a Q of 1 has a phase angle of 45 degrees and thus its reactive and resistive elements are equal. A Q of 150 has a phase angle of 89.6 degrees.

The factors which make up the effective resistance are quite complex. They involve both the core and winding losses. The core losses vary with material, frequency, flux density, and core size. The winding losses involve wire resistance, turn-to-turn, and turn-to-core capacitive effects which are all frequency and size dependent. There are rigorous analyses of these inter-relationships available, but in general they are far too complex to be of much practical use when it comes to designing a high Q, high frequency inductor. The basic trends of these inter-relationships as they relate to frequency are shown in the following exapmles. The examples will use toroidal or donut-shaped cores, but the principles can be applied to other core shapes.

Optimum Q occurs when the combined core loss equals the total winding loss. It has been shown by Legg that, in general, the maximum attainable Q is directly related to the physical size of a core for any given material. It has also been shown that the frequency at which this maximum attainable Q occurs is, in general, inversely proportional to permeability, core size, and the square root of the core loss.

Figure 1 illustrates this basic relationship. For a given core material (carbonyl E, u = 10, recommended frequency range of .25 to 10 mHz), the physically large cores provide a higher peak Q than the physically small cores and the frequency at which

signals, but of opposite signs, so their sum is zero. In a similar way it works for imaginary deviations from the matched condition. Just imagine the chart rotated 90 degrees!

The beauty of the Smith chart, or at least one of them, is preserved in this apparatus. It is the fact that near perfect loads will be treated especially carefully and accurately. The concept is clearly not limited to 50 ohm lines. One can imagine the use of perhaps a 5 ohm line in a test fixture for measuring transistor input impedances.

A limitation is the bandwidth. I would say that the function is very satisfying within a 10% band centered around the design frequency. That is certainly more than enough for most "band" operations, be it ham radio, cellular mobile, radar, microwave link or CB. An exception from the bandwidth limitation is of course the well-matched load, which will appear as such, no matter what the frequency.

The maximum possible frequency of operation that can be achieved remains to be determined. The diodes have to be operating, of course, and can always be spread by multiples of $\lambda/8$ if physically necessary, but the bandwidth will suffer. Hewlett-Packard has been kind enough to supply me with some zero bias diodes good to 10 GHz, but in spite of a lot of care, they got damaged by static electricity. Using regular "hot carrier" diodes will work to at least 1 GHz, but a signal level of at least -15 dBm is necessary for good signals. A possible method of building the instrument for microwave frequencies is shown in Figure 2.

Practical Aspects

It may be more desirable to have the testplane outside the connector, as opposed to just behind it. This is possible by just adding some line after the last diode. This may actually be the preferred method, since all the diodes then will be mounted in an identical manner on the line, thereby balancing each other better. They will then have to be permutated, changing the order from 1-2-3-4 to 4-1-2-3.

It is also possible to measure remote (100λ) objects. By leaving the end of the line open, one can determine to what extent the chart is rotated, and either change the frequency slightly to get the open located on the right, or add some cable, or just remember the position. The insertion loss of the cable limits the sensitivity, of course, but I have derived useful information about a load with a 20 dB attenuator in line and +10 dBm excitation. This corresponds to a VSWR of 1.02:1 or 40 dB return loss. With the same level of excitation I can detect the difference between a "perfect" load and one of 70 dB reflection. To observe that mismatch on a Smith chart, you would have to use a microscope, since it corresponds to a distance from the center of half the thickness of a human hair.

Displaying the voltages on an X-Y oscilloscope (or a plotter for swept signals) is very convenient. It then becomes apparent that the outline of the displayed field, corresponding to the circular border of the Smith chart, is not really circular, but somewhat diamond shaped. Should this be disturbing, a 6 dB attenuator can be left on the measurement port. It is "transparent"

this peak occurs is indeed inversely proportional to the core size. That is to say, large cores reach their optimum at a lower frequency than the small cores.

Figure 2 illustrates that for the same physical size core, a T50, (which is a 1/2 o.d. toroidal core), that the frequency at which the peak Q occurs increases with decreasing permeability. Eddy current losses also are involved in determining this optimum frequency.

In this comparison, the inductance has been a variable in order to approach an optimized Q at an optimized frequency. Figure 3 shows a series of Q curves for the same size core and material, each with a different single layer winding. These curves show that the frequency at which the Q peaks, decreases as the number of turns, and thus the inductance, increases. It also shows that there is a point at which a peak-peak is obtained.

Another interesting comparison is to set the inductance at a fixed value and see how the core size, core material and required windings interact. Figure 4 shows this comparison. While these are not optimized coils, this example illustrates that even with a fixed inductance, larger cores produce higher Q at a lower frequency than the smaller cores.

Thusfar, the examples given have not considered the winding details, but have looked at the interaction of core size and material as it relates to Q and frequency. In the examples shown, the windings have all been a full single layer. The following examples illustrate the effects of different types of windings and their implications versus frequency.

WINDING CONSIDERATIONS: In arriving at the best winding for a given coil, there are two basic effects, which reduce Q, that need to be considered: resistive and capacitive.

The resistance of copper wire at very low frequency is the same as its DC resistance. The skin depth of an AC current is inversely proportional to the square root of the operating frequency. Thus the AC resistance of a conductor is proportional to $\sqrt{f}$. Because of this, the increased resistance due to skin effect will begin to come into play at higher frequencies for smaller wire and at relatively low frequency for large wire. As an example, #30 wire will begin to see increased resistance as low as 300 KHz and #40 wire is affected around 3 MHz. This resistance is further increased in wound coils due to the proximity effect of adjacent turns.

In order to help the AC resistance of a conductor approach its DC resistance at moderate frequency, Litz wire can be used. Litz wire is formed by a number of strands of small insulated wire connected in parallel at the ends and completely interwoven. The interweaving is essential in order for the various strands to equally share the current. There is a significant difference between true Litz wire and stranded wire.

Practical Litz wire is very effective at frequencies up to 1 MHz. As frequency increases, however, the benefits begin to disappear. At very high frequencies the reduced resistance due to the interwoven stranding is more than off-set by the capacitive build-up between the strands. Since most of the work in RF today is at frequencies above 1 MHz the use of Litz wire has become rather uncommon.

In a winding, the self- capacitance that is built up is a result of the turn- to-turn capacitance of adjacent wires as well as turn-to-core capacitance. The turn-to-turn capacitance is affected by the wire size, the number of turns, and the spacing and positioning of the turns. In general, capacitive affects on Q become increasingly important with frequency squared (f^2). For a toroidal coil, one of the most important factors in controlling capacitive built-up is to limit the winding to a single layer. Figure 5, from Welsby, shows how the self capacitance of a toroidal coil varies with the number of winding layers. It is seen that the addition of even a partial second layer dramatically increases the self-capacitance.

This capacitive effect is evident in figure 6. In this example all the coils are wound with #28 wire and essentially the same number of turns. Curve #1 is a single layer winding and has a peak Q of 244. Curve #2 is the result of adding only 2 turns on a second layer. The resulting Q is 7% lower. Curve #3 is a randomly wound coil and exhibits even lower Q. And the worst of the group is curve #4 which has 60 turns on the first layer and 40 turns on the second layer. In this example the capacitive effects have lowered the Q by over 25%.

Since the objective is to minimize both resistance, which implies larger conductors and thus multi-layers, and at the same time to minimize capacitance, which implies single layers with good spacing, it is valuable to keep in mind that the importance of resistance varies with $\sqrt{f}$ and the importance of capacitance varies with f^2. This indicates that at low frequencies resistance is the dominant factor and that at high frequencies capacitance is the most important factor.

enough to make good measurements through. It also provides the necessary DC return path for the diode currents, that may not be present in the load or source.

The matching impedance of the source is not critical at all. A mismatch there reflects part of the power back to the source, but what travels down the line is what counts.

With zero bias diodes it should be possible to use a regular signal generator for the source, with levels of 1 mV (-47 dBm), and measure receiver inputs without driving them into non-linear regions.

Other Applications

Substituting the "perfect" load with a resonant circuit opens up a few interesting applications. The output from the jX detector becomes very sensitive to changes in frequency, being zero at resonance. This can be used to measure deviation, modulation, PLL step response and maybe even phase noise. The higher the Q of the attached resonant circuit, the more sensitivity. A VCO can be locked to a cavity or a stub, by feeding back the DC signal.

Another application could be a distance meter, connecting both outputs to an UP/DOWN counter, with an antenna for a load. The sine/cosine information in the reflected signal will run the counter up or down, and one count for every half wavelength will be gathered. This may be a good detector for doopler radar burglar alarms, eliminating false alarms from objects that are just swinging back and forth in the wind.

Conclusion

A detector has been described, that in sensitivity far exceeds the common VSWR meter, and furthermore provides information about the complex nature of the load, while still being of the same simplicity as a VSWR meter. The tradeoff is bandwidth. Also, it has other potential uses, as outlined, that a VSWR meter has not.

Acknowledgements

To Magnus Koch, as mentioned above, and to Ingvar Svensson, my teacher at TGG, Göteborg, who had the ability of explaining the Smith chart so vividly that this concept surfaced in one of his more absent-minded students' mind! If all teachers were like him, this world would be a much better place.

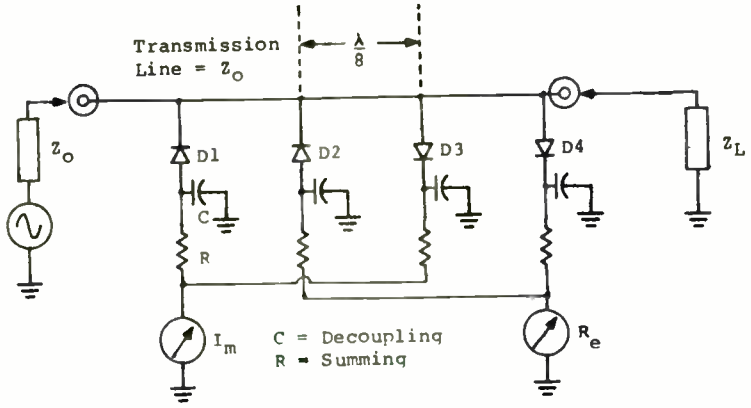
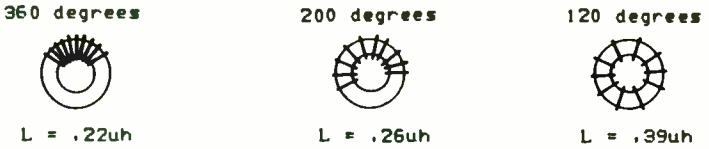


Figure 1(a). Basic Schematic of Impedance Meter.

Aside from the effect that coil capacitance has on Q, it also affects the self resonant frequency and apparent inductance of the coil. The greater the coil capacitance, the lower the self resonant frequency and the higher the apparent inductance.

These coils are also, often times, either dipped in a material to secure turns or are completely encapsulated. The dielectric characteristics of the material coming in contact with the winding can have a profound effect on the coil capacitance and, therefore, the Q, the apparent inductance and the self-resonant frequency. In order to minimize the shift that occors due to encapsulation, a material with a low dielectric constant must be used.

Another characteristic which effects the apparent inductance is leakage inductance. Leakage inductance acts in series with a coils self inductance. This is the result of uncoupled flux and becomes most apparent in high frequency, low inductance coils, particularly when the turns are not evenly distributed around the core. Here is an example using a T50-17 toroid (u = 4) wound with 10 turns, #20 wire:



In instances like this where it is possible to drastically change the positioning of the turns, and the permeability of the core material is low, very large differences are seen. In higher permeability materials this effect is much less. In a number of applications, toroidal coils are tuned by this means.

SUMMARY: Iron powder is a core material well suited for high Q stable inductors to be used in the 100 KHz to 200 MHz frequency range.

The following relationships regarding core material and size have been shown:

1. For a given material, larger cores produce a higher Q at a lower frequency.

2. For a given material and core size, Q peaks at a lower frequency as the turns are increased. There is a frequency and winding where Q is optimized.

3. For a given core size, the optimum value of Q is inversley proportional to the permeability.

It has also been shown that from the winding standpoint, in order to help optimize Q:

1. At low frequency (< 500 KHz) that the resistive losses are dominant and thus the use of Litz wire is advantageous.

2. At frequencies above 1 MHz losses due to capacitive effects begin to dominate and that multilayering is very detrimental to Q. It can generally be stated that a full single layer will provide the best result.

In order to help the design engineer in his efforts to build high Q inductors, Micrometals, Inc. has printed an extensive series of Q vs frequency curves for iron powder cores known as "The Q-Curve Book." In studying this information it can be seen that when high Q is required at a particular frequency and the physical size is limited by packaging requirements that, when possible, it is best to optimize the coil for Q and to adjust the value of the external resonating capacitors rather than to select the desired inductance and then sacrifice Q in order to achieve the inductance.

Another application for which iron powder is receiving increased attention is for use in very high frequency broadband matching applications. The extremely linear frequency response of iron powder even with 35 permeability material makes it useful for transformers above 50 MHz. The primary attraction of iron powder is its repeatability at the extremely high frequencies. Full characterization of these materials for broadband applications up to 1 GHz will be available in the future.

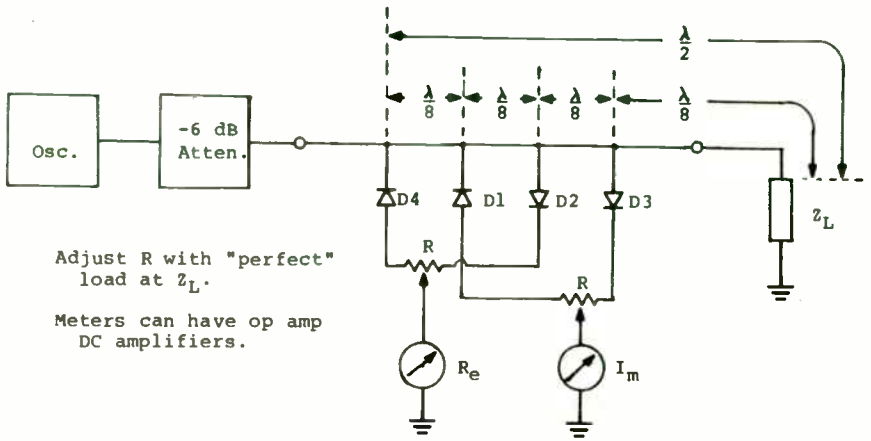


Figure 1(b). Circuit with measurement plane outside 'unknown' connector. Note diode numbering change.

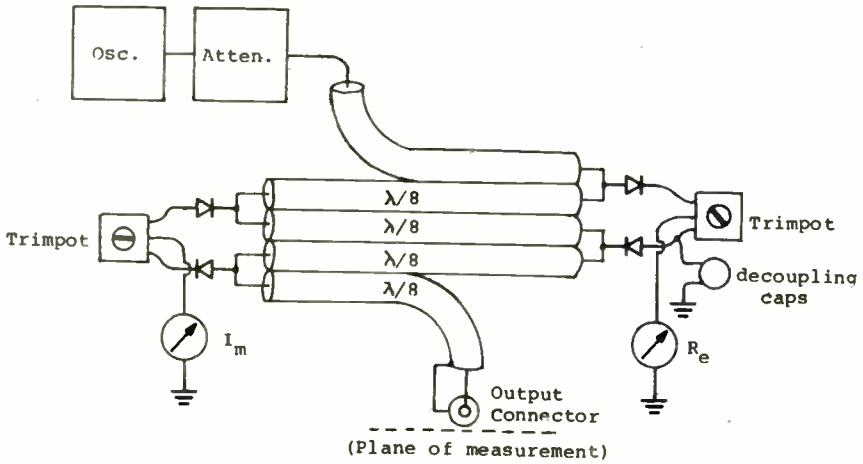


Figure 1(c). Practical construction method.

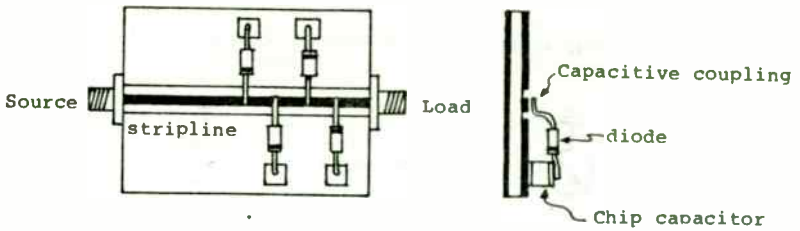


Figure 2. Possible microwave construction method.

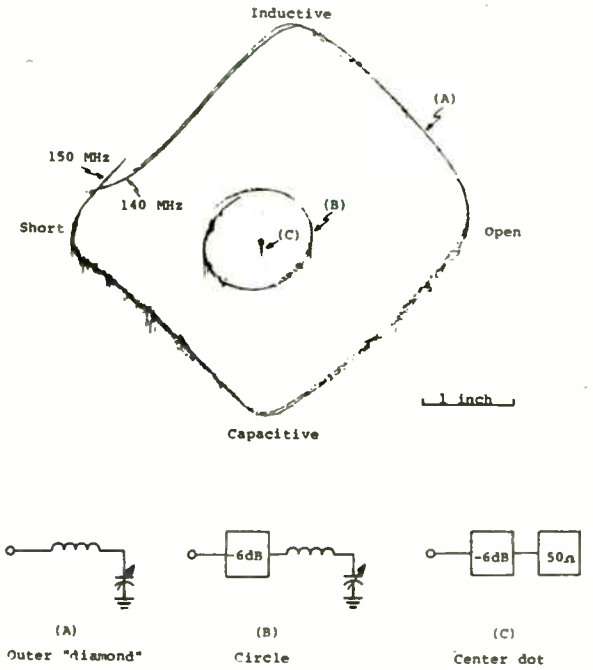
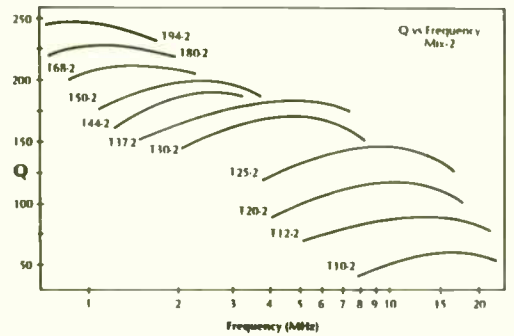


Figure 3. Display of measurements made with Impedance Meter.

Carbonyl E 10 μo

MIX-2

Micrometals Part No.	Turns	Wire	L (uh)
T-94-2	100	#28	84
T-80-2	100	#28	55
T-68-2	100	#30	57
T-50-2	77	#30	29
T-44-2	66	#30	23
T-37-2	53	#30	11.5
T-30-2	47	#32	9.3
T-25-2	30	#30	3.0
T-20-2	30	#33	2.4
T-12-2	25	#36	1.3
T-10-2	25	#40	.9



PART NUMBER

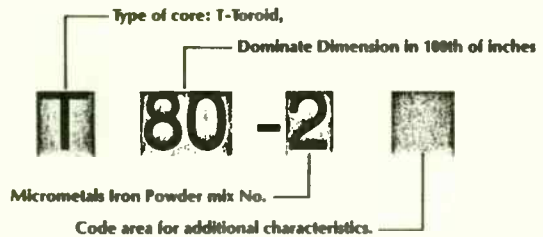
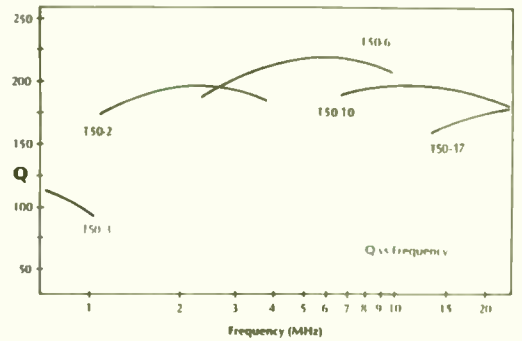


Figure 1



General Magnetic Properties

Mix #	Basic Iron Powder	Material Permeability (μo)	Temperature Stability (+)	Resonant Circuit Frequency Range[1] (MHz)	Color Code
1	Carbonyl C	20	280 ppm/°C	.15-2.0	Blue
2	Carbonyl E	10	95	.25-10.	Red
3	Carbonyl HP	35	370	.02-1.0	Gray
6	Carbonyl SF	8.5	35	2.0-30.	Yellow
7	Carbonyl TH	9.0	30	1.0-20.	White
8	Carbonyl GQ4	35	255	.02-1.0	Orange
10	Carbonyl W	6.0	150	10-100	Black
12	Synthetic Oxide	4.0	170*	20-200	Green/White
15	Carbonyl GS6	25	190	.10-3.0	Red/White
17	Carbonyl	4.0	50	20-200	Blue/Yellow
22	Synthetic Oxide	4.0	410*	20-200	Green/Orange
0	Phenolic	1	0	50-250	Tan

[1]Frequency range indicated is for maximum Q. For wide-band applications where high Q is not required, the useful frequency range will typically extend 10 to 100 times higher.

*Non-linear

Figure 2

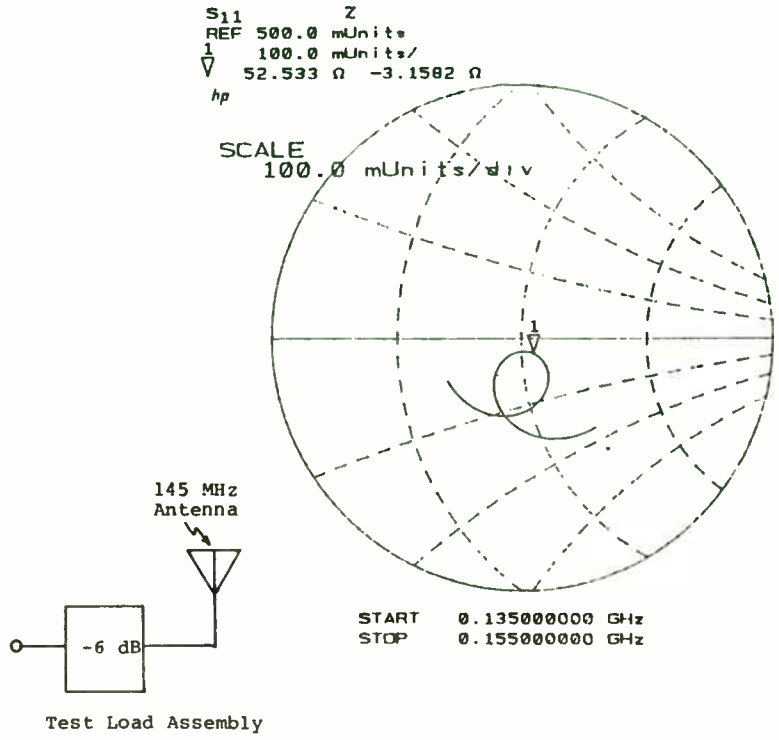


Figure 4. Top plot was made with a Hewlett-Packard 8510 Network Analyzer. The bottom plot is the same load measured with the Impedance Meter. Shapes of the curves are nearly identical, with some differences in rotation of the display and the calibration of the center dot (50 ohm load).

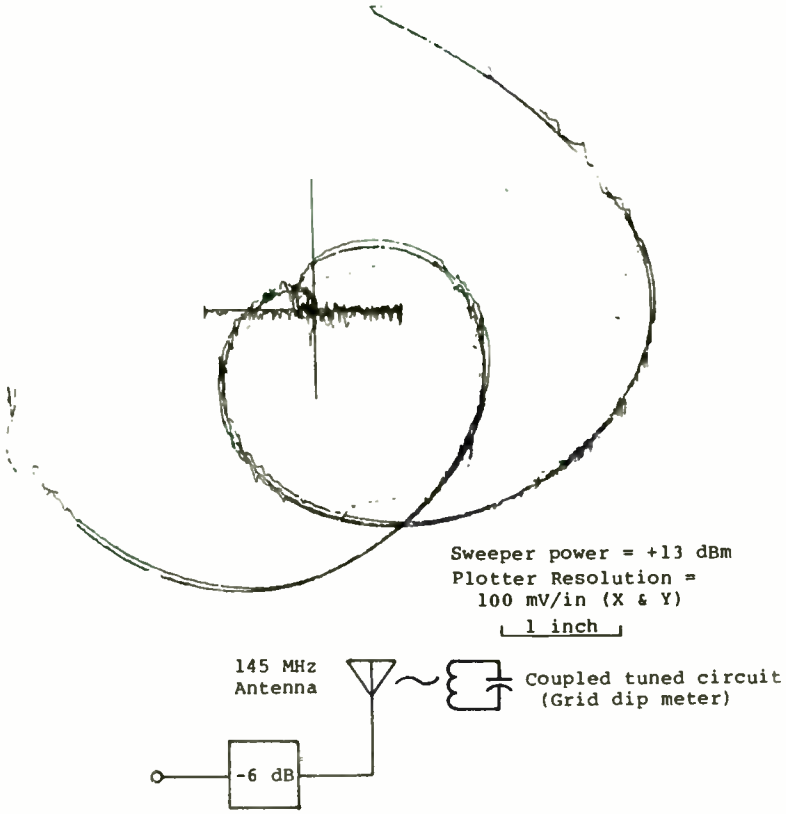


Figure 5. Effects of an additional tuned circuit, coupled to the antenna. As would be predicted, a high-Q response (small loop) occurs at the additional resonant frequency. Light coupling does not greatly disturb the primary antenna response.

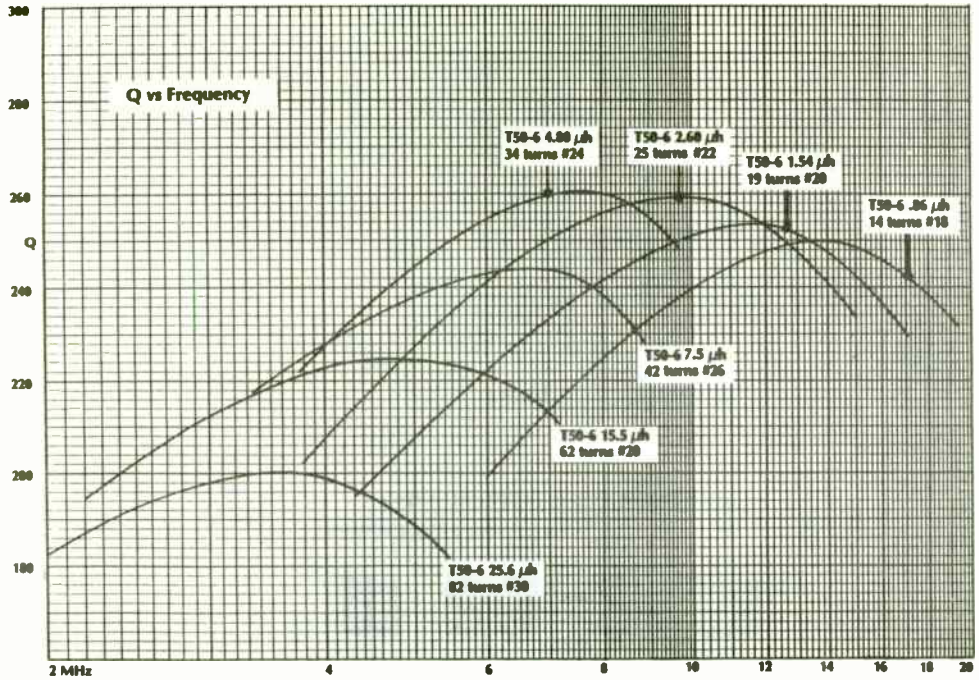


Figure 3

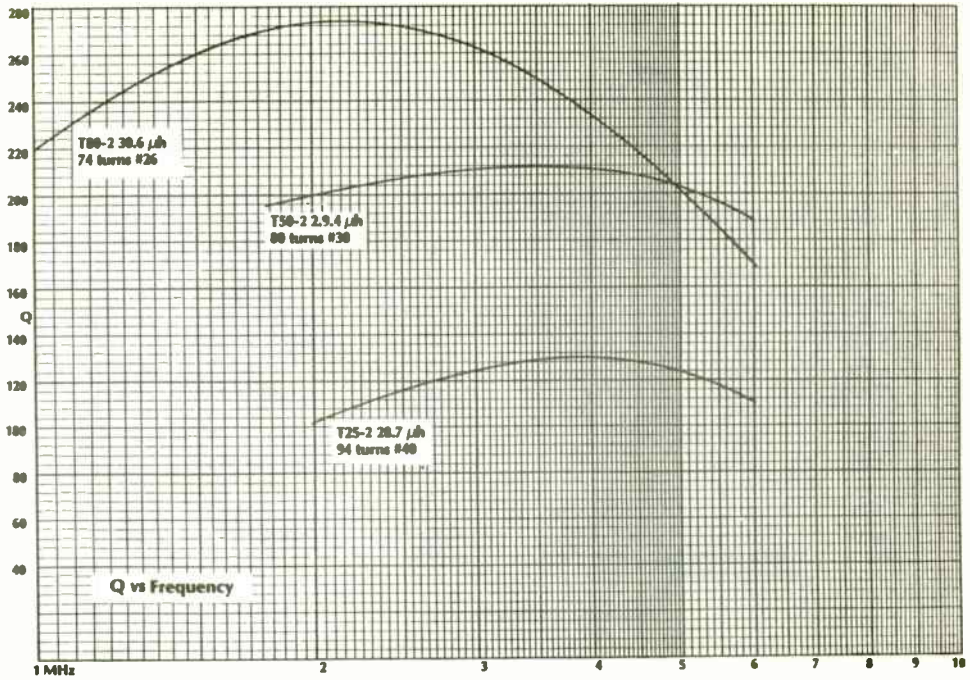
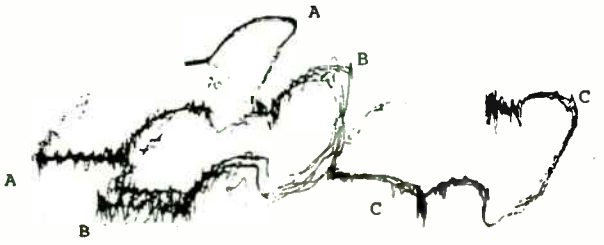
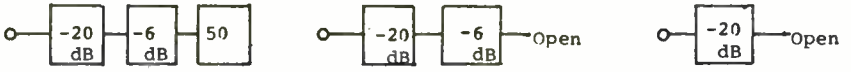


Figure 4



Sweeper power = +13 dBm
Plotter resolution = 5 mV/in
(X & Y)

1 inch



Plot A: "perfect" load. Plot B: 52 dB return loss, (20 + 6) X 2. Plot C: 40 dB return loss.

Figure 6. Sensitivity demonstration - High sensitivity display can discern difference between "perfect", 52 dB return loss and 40 dB return loss loads. Plot A is a magnification of the center dot in Figure 3.

CAPACITANCE OF TOROIDAL WINDINGS AS
A FUNCTION OF THE NUMBER OF LAYERS

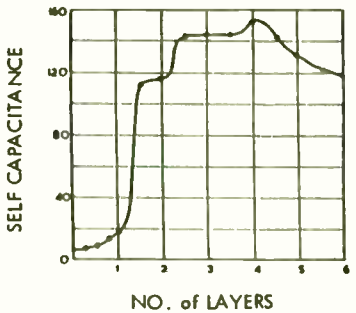


Figure 5

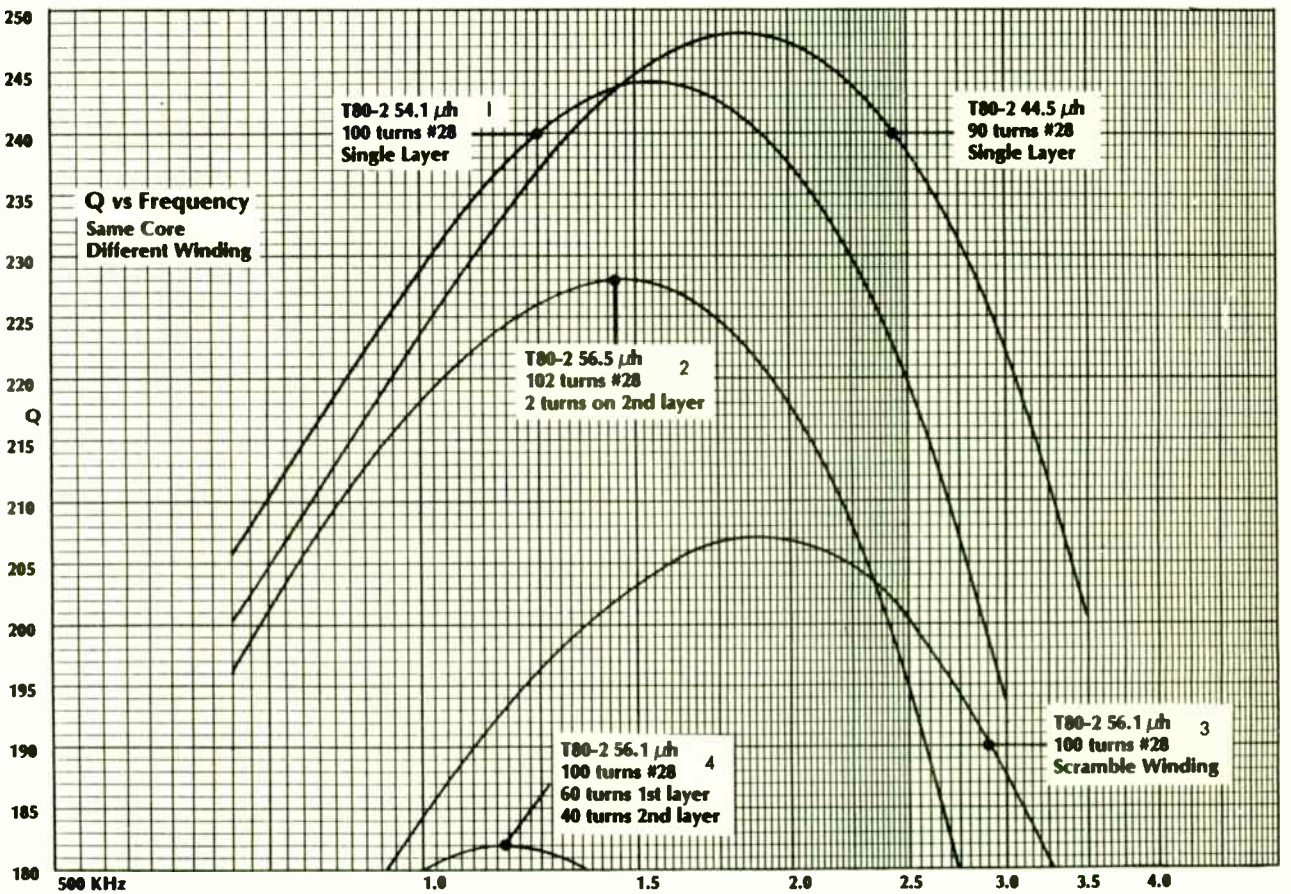


Figure 6

Efficiency of Envelope-Tracking RF Power-Amplifier Systems

by
Frederick H. Raab, Ph.D.
Green Mountain Radio Research Company
50 Vermont Avenue, Fort Ethan Allen
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ABSTRACT

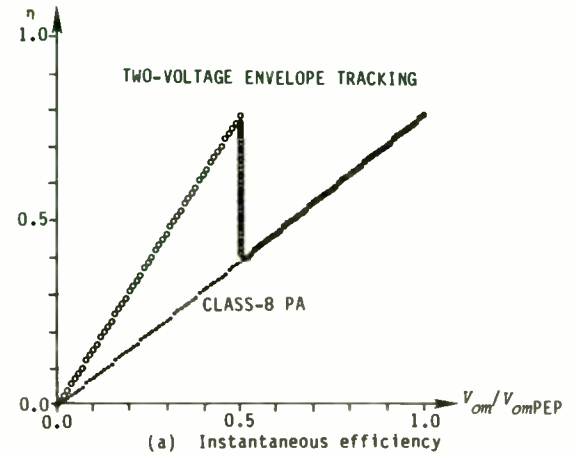
Envelope tracking is a technique for increasing the efficiency of a linear RF power amplifier (PA) by varying its supply voltage to track the envelope of the RF signal. Potential advantages of envelope tracking over other techniques include simple circuitry and usability at any RF frequency, RF bandwidth, and signal bandwidth. Instantaneous power and efficiency characteristics are derived using ideal class-B PAs so that the results can easily be scaled for use with practical PAs. The average efficiencies are then determined as functions of the supply-voltage ratio for a variety of amplitude-modulated signals. The improvement in average efficiency can be quite significant but naturally depends upon the specific type of signal and its peak-to-average ratio. For example, the 28-percent average efficiency of a single-voltage PA with a Rayleigh-envelope signal of 10-dB peak-to-average ratio can be increased to 48 and 57 percent by two- and three-voltage envelope tracking, respectively.

1. INTRODUCTION

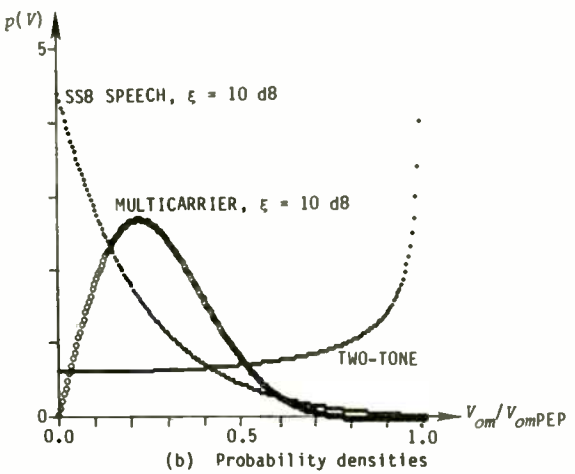
Envelope tracking is a technique for increasing the efficiency of a linear RF power amplifier (PA) by varying its dc supply voltage to track the envelope of the desired output signal. The improvement in efficiency is achieved because the efficiency of almost any PA is proportional (or approximately proportional) to the ratio of its output voltage to its PEP-output voltage. The improvement in efficiency is especially significant when the signal to be amplified has a high peak-to-average ratio, which causes a linear PA to operate in a low-power, low-efficiency region most of the time.

Consider, for example, the curves in Figure 1. The instantaneous efficiency of an ideal class-B PA increases from zero to 78.5 percent as its output increases from zero to peak-envelope power (PEP). The two-tone test signal has a 3-dB peak-to-average ratio and spends most of its time at amplitudes near PEP, hence the ideal class-B PA amplifier has an average efficiency of 61 percent. However, the speech and multicarrier signals more commonly encountered during actual use have larger peak-to-average ratios (e.g., 10 dB), resulting in average efficiencies on the order of 30 percent.

If the PA is operated from half of the full supply voltage, the instantaneous efficiency increases from zero to 78.5 as the RF-output voltage increases from zero to half of the PEP-output voltage, doubling the instantaneous efficiency for low-amplitude signals. For larger instantaneous outputs, the PA must be operated from the full supply voltage, dropping the instantaneous efficiency to that of an ordinary class-B PA. Nonetheless, the average



(a) Instantaneous efficiency



(b) Probability densities

Figure 1. Efficiency and distribution characteristics.

efficiency for signals with a 10-dB peak-to-average ratio is increased from approximately 30 percent to approximately 48 percent.

The block diagram of a two-voltage envelope-tracking system is shown in Figure 2. The envelope of the input signal is detected and compared to a threshold value. When the envelope is larger than the threshold value, V_{DDRF} (the dc supply voltage for the RF PA) is switched to the full dc supply voltage V_{DD}. Otherwise, V_{DDRF} is switched to the lower supply voltage αV_{DD} to reduce power dissipation in the RF PA. The lower supply voltage can be obtained from an efficient switching regulator or from a center connection in a series of batteries.

The concept is readily extended to three or more supply voltages. However, the use of a larger number of supply voltages adds to circuit complexity, thus eliminating one of the advantages of envelope tracking. The supply voltage to the RF driver amplifiers can also be varied to reduce their power consumption. In addition, a switched compensation network can be added to correct for gain and phase changes associated with operation of the PA from different supply voltages.

A number of techniques [1 - 6] are known for implementing high-efficiency RF power amplifiers (e.g., classes D, E, and F) and for combining PAs to increase efficiency (e.g., envelope elimination and restoration, outphasing, and Doherty). Envelope tracking is thus neither the only technique nor necessarily the best technique for improving efficiency. However, it may be the most practical or most effective technique in certain situations, such as when

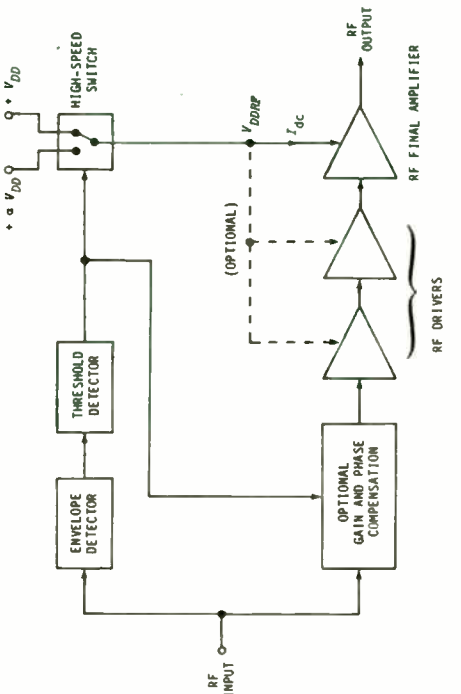


Figure 2. Block diagram of envelope-tracking system.

140 MHz Lumped Element 3dB Hybrid

by

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A 140 MHz, 3 dB hybrid was realized using lumped inductances and capacitances. At microwave frequencies 3 dB hybrids are realized using branched line hybrid couplers. Branched line hybrid consists of series and shunt $\lambda/4$ transmission lines. At 140 MHz the $\lambda/4$ transmission line will be about 53.5 cm long in air, and it would be impractical to fabricate branched line hybrids at these frequencies. The characteristics of transmission lines can be realized using lumped inductances and capacitances. It is thus possible to realize the branched line coupler in its equivalent form.

The commonly used single section branched line hybrid coupler is shown in Fig.1(a). The $\lambda/4$ transmission lines of this hybrid can be realized by the lumped element pi-network shown in Fig.1(b). The inductance L and the capacitance C of this network, in terms of the characteristic impedance Z_o and the centre frequency of operation f_o of the equivalent transmission line, are given by the following equations.

$$\sqrt{L/C} = Z_o \qquad \text{-------- (1)}$$

$$1/\sqrt{LC} = 2\pi f_o \qquad \text{------ (2)}$$

Using these equations the L and C values for the 50 Ω and $50/\sqrt{2}$ Ω charecteristic impedance $\lambda/4$ transmission line were calculated and the lumped element equivalent of the 140 MHz 3 dB two branched line hybrid is shown in Fig.2(a). This can be further simplified to the network in Fig.2(b).

Realization of the lumped element $\lambda/4$ transmission line:

A $\lambda/4$ transmission line was realized using aircore inductors and variable capacitors (Thintrim^R). The aircore inductors were measured by reasonating them with a chip capacitor (at a series resonant frequency of 140 MHz). The series resonant circuit was loosely coupled to input and output microstrip lines with two 6.8 pF series capacitors. Thintrim^R variable capacitors were tuned to the appropriate value by resonating them with the measured aircore inductors in a similar way. To measure the insertion loss and insertion phase response of the lumped element pi-network, two equal length 50 ohms lines were used on the 31 mil thick Teflon fiberglass substrate. One microstrip line was used as the reference line to eliminate the ambiguities due to co-axial to microstrip transitions. Layout for this experiment is shown in Fig.3 (a). The series inductor L (56.84 nH) was connected by cutting the other microstrip line, and the capacitors C (22.736 pF) were grounded by through holes in patches P_1 and P_2. SMA connectors were used for the external

- The operating frequency is too high for implementation of high-efficiency RF PAs,
- The signal bandwidth is so large that class-S envelope modulators are impractical or inefficient,
- The frequency range of operation is larger than that of the transmission-line couplers required by the outphasing and Doherty techniques, or
- Economic or space considerations do not permit implementation of a class-S envelope modulator.

The objective of this paper is to determine the improvement in efficiency that can be achieved by applying two- or three-voltage envelope tracking to a class-B linear RF PA. While the use of multiple supply voltages in audio PAs has been discussed in the literature [7, 8], little consideration has been given to analogous techniques for RF PAs. To obtain generally applicable results, ideal class-B PAs are assumed. Predictions for a practical PA can be obtained by scaling the results presented here by the efficiency of the PA at peak output.

2. INSTANTANEOUS EFFICIENCY

The characteristics of ideal and practical class-B PAs are discussed in [1]. It is useful to recall that the dc input current for an ideal class-B PA is

$$I_{dc} = \frac{2}{\pi} \frac{V_{om}}{R} \quad , \tag{1}$$

where V_{om} is the output envelope voltage (i.e., $V_{om} \sin \omega t$) and R is the load resistance. Note that I_{dc} is *not* dependent upon supply voltage.

A two-voltage envelope tracking system employs supply voltages of V_{DD} and αV_{DD} where $\alpha < 1$. Linear operation of the RF PA requires its supply voltage to be at least as large as the desired output voltage. The threshold comparison (Figure 2) required to vary the V_{DDRF} (as in Figure 3) is described by

$$V_{DDRF} = \begin{cases} \alpha V_{DD}, & 0 < V_{om} < \alpha V_{DD} \\ V_{DD}, & \alpha V_{DD} < V_{om} < V_{DD} \end{cases} \quad , \tag{2}$$

The resultant dc input power is therefore

$$P_i = \begin{cases} \alpha V_{DD} I_{dc}, & 0 < V_{om} < \alpha V_{DD} \\ V_{DD} I_{dc}, & \alpha V_{DD} < V_{om} < V_{DD} \end{cases} \quad , \tag{3}$$

The instantaneous dc-input power curves and the corresponding efficiency curves are shown in Figure 4. Note the abrupt decrease in power consumption and increase in efficiency when the V_{DDRF} is switched from the higher supply voltage to the lower supply voltage.

The three-voltage envelope-tracking concept is analogous to the two-voltage concept but employs supply voltages $\alpha_1 V_{DD}$, $\alpha_2 V_{DD}$, and V_{DD}, where $\alpha_1 < \alpha_2 < 1$. The voltage-switching algorithm is described by

connections to the microstrip lines. HP 8505A network analyzer and 8503A S-parameters sets were used for measurements. Using an in-house circuit analysis package the theoretical response of the pi-network was calculated. The measured and theoretical insertion loss phase response for the lumped element $\lambda/4$ 50Ω transmission line is shown in Fig.4. There was a very close correlation between the measured and theoretical responses.

The realization of the lumped element branched line hybrid:

Since the lumped element pi-network design based on equations (1) and (2) had a satisfactory phase response, the branched line hybrid was realized as per Fig.2(b). The layout of the lumped element hybrid is shown in Fig.3(b). All the inductors and capacitors were tuned to proper values by the procedure outlined earlier. For this coupler the return loss and isolation maxima occured at different frequencies. The measured return loss and isolation characteristics are shown in Fig.5. Using the in-house "SCAT" circuit analysis program the lumped element hybrid circuit was analyzed. From the theoretical analysis it was found that it is possible to obtain the measured response when there is 10% increase in three of the inductor values, 8% decrease in the capacitor values and about 10% decrease in the value or L_1 (Fig.3b). This order of error in the measurement of L's and C's can be due to the following reasons:

1. Inaccuracy of the series resonant frequency measurement on the network analyzer.
2. Tolerance of chip capacitors used for measuring the aircore inductors.
3. The unaccounted loading of the series resonant circuit used for measuring L's and C's.

Based on the theoretical analysis, the 3 dB hybrid was tuned to get the response shown in Fig.6. It can be seen that this hybrid has a minimum return loss of about 14 dB, a minimum isolation of about 15 dB and a maximum coupling imbalance of 0.7 dB over 128 MHz to 144 MHz. Thus the lumped element 140 MHz 3 dB hybrid has a satisfactory performance over about 12% bandwidth. The difference in the theoretical and experimental results (fig.(6)) could be due to the fact that in theoretical modeling the finite Q's of the inductors and capacitors were not included. Though this coupler was realized with microstrip input and output lines and SMA connectors were used for our convenience, it can be realized on a PCB for integration with other circuits. Unline a Ruthroff transformer this coupler is compatible with planar technology and can be easily miniaturized using thick and thin film techniques. For a broader bandwidth, lumped element equivalent circuits for higher order branched line hybrids can be realized.

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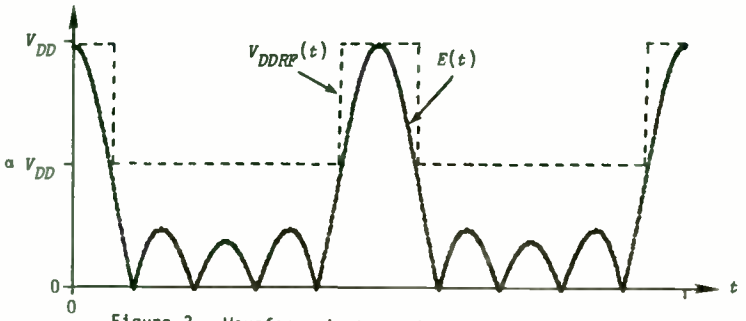


Figure 3. Waveforms in two-voltage envelope-tracking system.

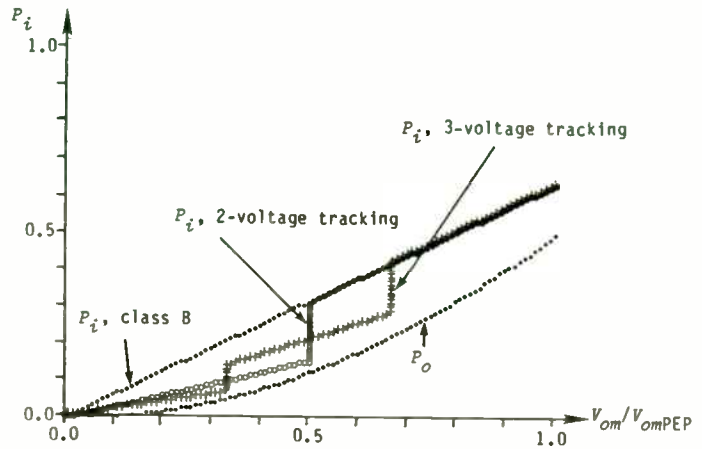
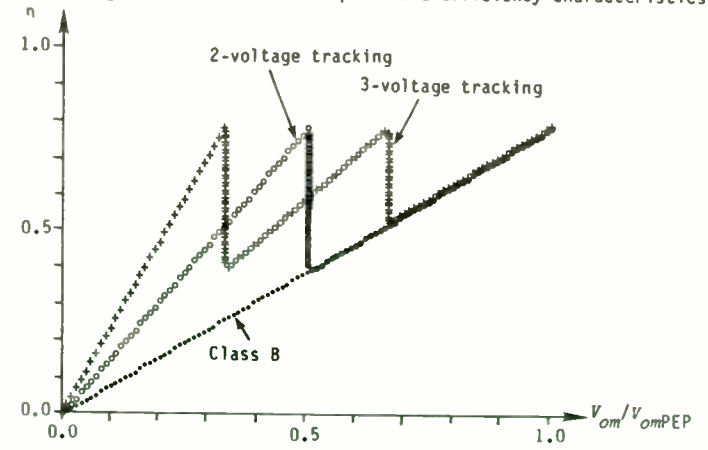


Figure 4. Instantaneous power and efficiency characteristics.



$$V_{DDRF} = \begin{cases} \alpha_1 V_{DD}, & 0 < V_{om} < \alpha_1 V_{DD} \\ \alpha_2 V_{DD}, & \alpha_1 V_{DD} < V_{om} < \alpha_2 V_{DD} \\ V_{DD}, & \alpha_2 V_{DD} < V_{om} < V_{DD} \end{cases} \tag{4}$$

and the corresponding dc input power is

$$P_i = \begin{cases} \alpha_1 V_{DD} I_{dc}, & 0 < V_{om} < \alpha_1 V_{DD} \\ \alpha_2 V_{DD} I_{dc}, & \alpha_1 V_{DD} < V_{om} < \alpha_2 V_{DD} \\ V_{DD} I_{dc}, & \alpha_2 V_{DD} < V_{om} < V_{DD} \end{cases} . \tag{5}$$

The instantaneous power input and efficiency curves are also shown in Figure 4.

3. AVERAGE POWER INPUT AND EFFICIENCY

Average efficiency [1, 9] is defined as the ratio of the average RF-output power to the average dc-input power; i.e.,

$$\eta_{AVG} = P_{oAVG} / P_{iAVG} . \tag{6}$$

The average powers are determined by integrating the instantaneous powers weighted by the envelope probability-density function (p.d.f.) over the range of envelope values:

$$P_{oAVG} = (1/2) \int_0^{V_{omPEP}} V_{om}^2\, p(V_{om})\, dV_{om} \tag{7}$$

and

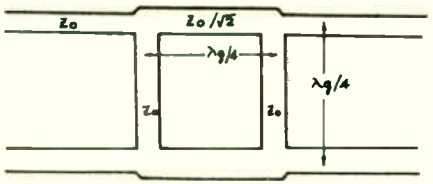


FIG. 1(a). SINGLE SECTION BRANCHED LINE COUPLER

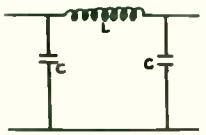


FIG. 1(b) TRANSMISSION LINE EQUIVALENT LUMPED ELEMENT NETWORK.

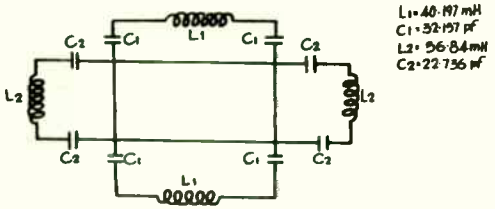


FIG. 2(a) L C ANALOGUE OF A BRANCHED LINE COUPLER

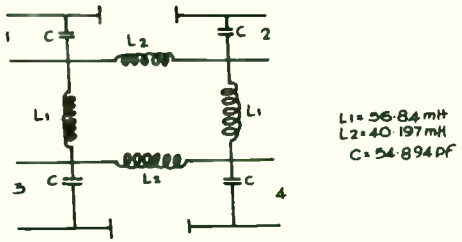


FIG. 2(b). SIMPLIFIED LUMPED ELEMENT BRANCHED LINE HYBRID.

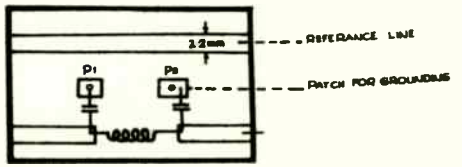


FIG. 3(a) LAYOUT FOR LUMPED ELEMENT λ/4 TRANSMISSION LINE MEASUREMENTS.

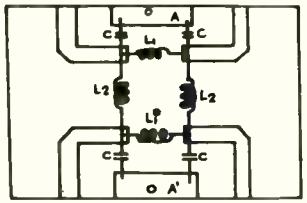


FIG. 3(b) LAYOUT OF THE LUMPED ELEMENT HYBRID.

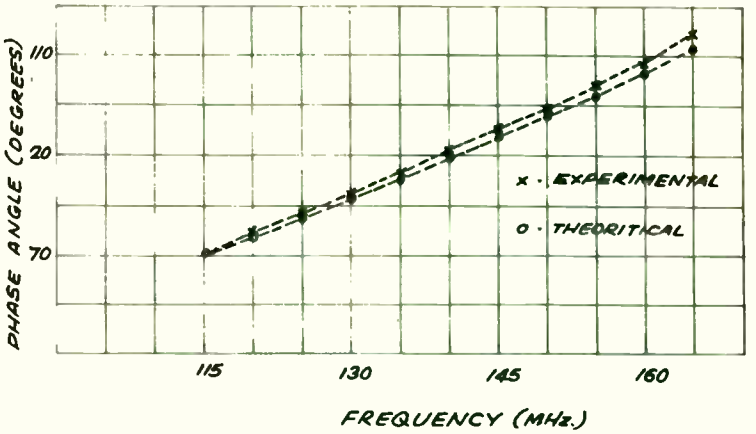


FIG. 4. THEORETICAL & EXPERIMENTAL VALUES OF INSERTION PHASE FOR λ/4 LINE.

$$P_{iAVG} = \int_0^{V_{omPEP}} P_i(V_{om})\, p(V_{om})\, dV_{om} \quad . \tag{8}$$

The peak-to-average ratio is defined by

$$\xi = P_{oPEP} \,/\, P_{oAVG} \quad . \tag{9}$$

A number of useful p.d.f.s are defined in [5] and [9]. For the uniform p.d.f., the dc input power and maximum-efficiency values of α, α_1, and α_2 can be determined analytically. However, for the other p.d.f.s, the evaluation is most readily accomplished numerically.

Selected Signals

Single-sideband suppressed-carrier (SSB/SC) transmitters are commonly tested with a two-tone signal, while full-carrier AM transmitters are commonly tested with a single-tone modulating signal. Some types of amplitude companders are said to produce a nearly uniform amplitude distribution. Quadrature amplitude modulation (QAM) is being used with increasing frequency in data-transmission systems because of its ability to pack a large number of bits into a single data symbol. All of these selected signals have relatively low peak-to-average ratios.

The average efficiency of two-voltage envelope tracking with the four selected signals is shown in Figure 5 as a function of the transition ratio α. The maximum average efficiency attainable with both two- and three-voltage envelope tracking as well as the corresponding average efficiency for a single supply voltage are given in Table 1. For these signals, two-voltage tracking

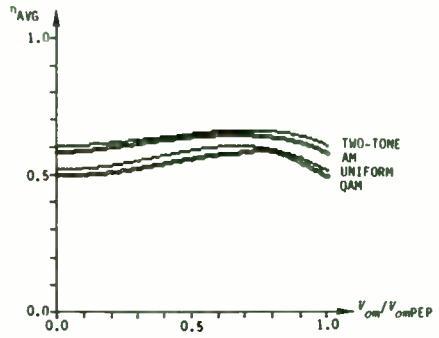


Figure 5. Average efficiency of two-voltage tracking with selected signals.

SIGNAL	ξ, dB	η_{AVG} class-B	Two-Voltage Tracking max η_{AVG}	Two-Voltage Tracking α	Three-Voltage Tracking max η_{AVG}	Three-Voltage Tracking α_1	Three-Voltage Tracking α_2
Two-tone	3.0	0.614	0.673	0.71	0.701	0.56	0.82
AM	4.3	0.587	0.655	0.66	0.687	0.50	0.79
Uniform	4.8	0.524	0.615	0.67	0.658	0.52	0.78
QAM	4.8	0.484	0.605	0.71	0.653	0.57	0.76
Rayleigh	5.0	0.455	0.580	0.63	0.635	0.50	0.73
Rayleigh	6.0	0.425	0.561	0.61	0.621	0.48	0.71
Rayleigh	7.0	0.387	0.540	0.58	0.607	0.45	0.68
Rayleigh	8.0	0.350	0.519	0.55	0.592	0.42	0.65
Rayleigh	9.0	0.314	0.498	0.52	0.578	0.39	0.61
Rayleigh	10.0	0.280	0.479	0.49	0.566	0.36	0.57
Rayleigh	11.0	0.250	0.462	0.45	0.556	0.33	0.53
Rayleigh	12.0	0.223	0.448	0.42	0.547	0.30	0.49
Rayleigh	13.0	0.198	0.435	0.39	0.540	0.28	0.46
Rayleigh	14.0	0.177	0.424	0.36	0.534	0.25	0.42
Rayleigh	15.0	0.158	0.414	0.33	0.529	0.23	0.39
Rayleigh	16.0	0.140	0.405	0.30	0.524	0.20	0.35
Rayleigh	17.0	0.125	0.397	0.28	0.520	0.18	0.32
Rayleigh	18.0	0.112	0.390	0.25	0.516	0.17	0.29
Rayleigh	19.0	0.099	0.383	0.23	0.513	0.15	0.27
Rayleigh	20.0	0.089	0.377	0.21	0.509	0.14	0.24
Laplacian	5.0	0.401	0.537	0.55	0.601	0.40	0.68
Laplacian	6.0	0.386	0.527	0.53	0.594	0.38	0.67
Laplacian	7.0	0.369	0.516	0.52	0.585	0.37	0.65
Laplacian	8.0	0.350	0.504	0.50	0.576	0.36	0.64
Laplacian	9.0	0.330	0.490	0.48	0.566	0.34	0.62
Laplacian	10.0	0.308	0.475	0.47	0.555	0.32	0.60
Laplacian	11.0	0.286	0.459	0.45	0.543	0.31	0.58
Laplacian	12.0	0.263	0.443	0.43	0.531	0.29	0.56
Laplacian	13.0	0.240	0.435	0.41	0.518	0.27	0.53
Laplacian	14.0	0.217	0.408	0.39	0.505	0.25	0.51
Laplacian	15.0	0.195	0.391	0.37	0.492	0.24	0.49
Laplacian	16.0	0.175	0.375	0.35	0.480	0.22	0.46
Laplacian	17.0	0.157	0.359	0.33	0.469	0.20	0.43
Laplacian	18.0	0.140	0.345	0.31	0.459	0.19	0.41
Laplacian	19.0	0.125	0.332	0.29	0.449	0.17	0.38
Laplacian	20.0	0.111	0.320	0.27	0.441	0.14	0.36
Gaussian AM	5.0	0.478	0.594	0.66	0.645	0.54	0.76
Gaussian AM	10.0	0.431	0.585	0.65	0.644	0.54	0.72
Gaussian AM	15.0	0.405	0.610	0.62	0.671	0.53	0.66
Gaussian AM	20.0	0.397	0.653	0.58	0.707	0.52	0.61
Laplacian AM	5.0	0.455	0.595	0.63	0.648	0.54	0.73
Laplacian AM	10.0	0.425	0.598	0.62	0.635	0.54	0.70
Laplacian AM	15.0	0.405	0.590	0.59	0.678	0.53	0.65
Laplacian AM	20.0	0.397	0.570	0.57	0.709	0.52	0.61

Table 1. Maximum average efficiencies and corresponding voltage ratios.

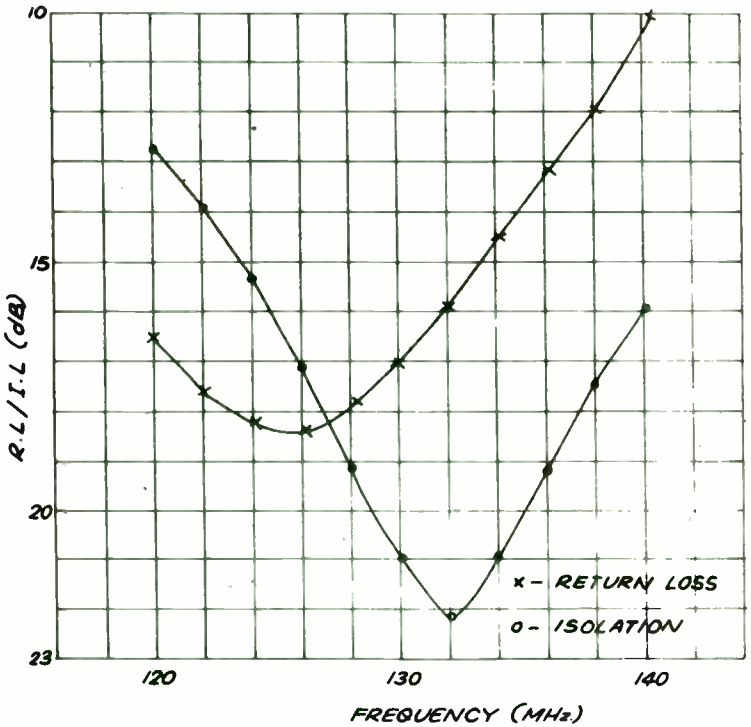


FIG. 5 UNTUNED COUPLER RESPONSE

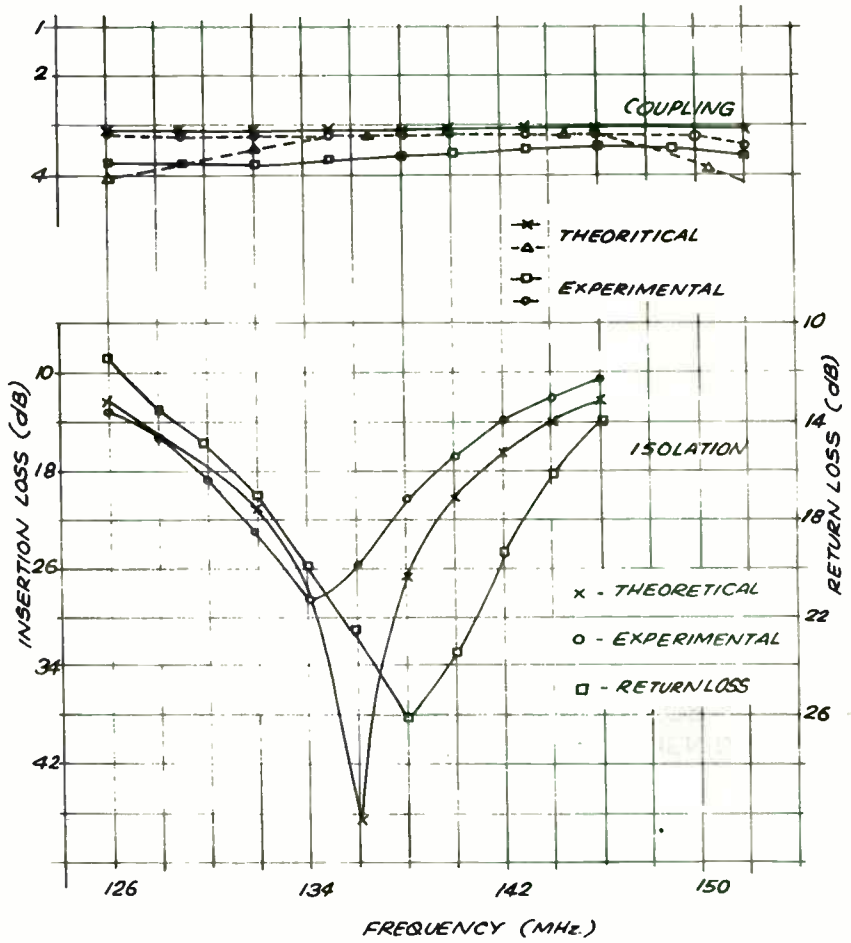


FIG. 6 TUNED HYBRID COUPLER RESPONSE

makes a significant improvement in average efficiency but three-voltage tracking makes only a small additional improvement.

Multicarrier and SSB/SC Voice

The envelope of bandlimited Gaussian noise has a Rayleigh distribution [10]. The envelope of the sum of a large number of independent RF carriers (with either FM or AM) also tends to have a Rayleigh distribution. The average efficiency of two-voltage envelope tracking with Rayleigh-envelope is shown in Figure 6 for peak-to-average ratios of 5, 10, 15, and 20 dB. The maximum average efficiency (obtained with proper choice of α) is shown in Figure 7 for peak-to-average ratios from 5 to 20 dB. Average-efficiency contours for three-voltage envelope tracking with $\xi = 10$ are shown in Figure 8.

For $\xi = 5$ dB, the improvements are similar to those obtained with the four selected signals. However, the improvement in average efficiency becomes much more significant as the peak-to-average ratio increases (Figure 8). For example, at $\xi = 10$ dB, the 28-percent average efficiency of a single-voltage PA is increased to 48 percent by two-voltage envelope tracking and to 57 percent by three-voltage tracking. For $\xi = 20$ dB, the average efficiency is increased from a meager 8.9 percent to 38 and 51 percent by two- and three-voltage envelope tracking, respectively. Note that the effect of the transition voltage increases as the peak-to-average ratio increases.

The envelope of an SSB/SC signal produced by speech has a Laplacian (one-sided exponential) distribution. The average efficiency as a function of transition voltage is shown in Figure 9 for Laplacian-envelope signals with

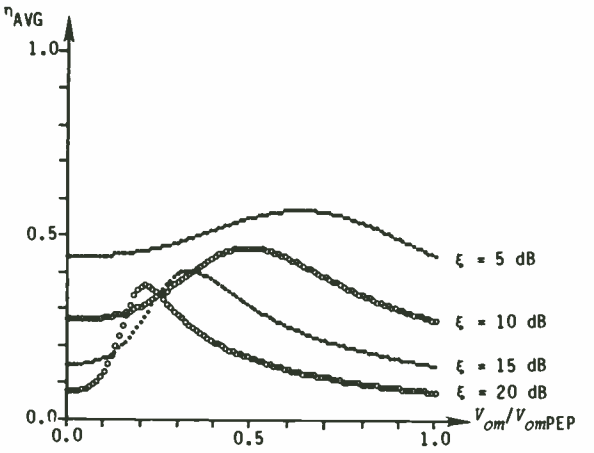


Figure 6. Average efficiency of two-voltage tracking with Rayleigh envelope.

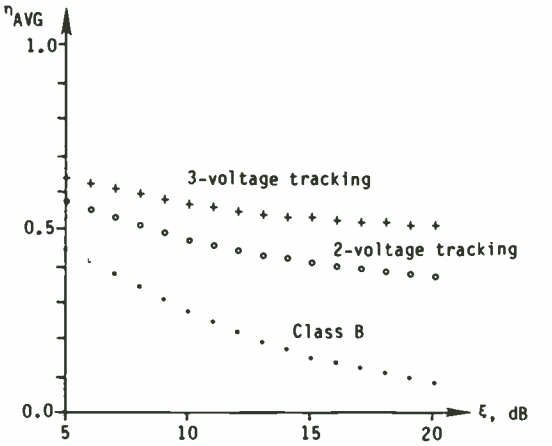


Figure 7. Maximum average efficiency of two-voltage tracking for Rayleigh envelope.

A COMMUTATION DOUBLE-BALANCED MIXER OF HIGH DYNAMIC RANGE

by

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INTRODUCTION

Dynamic range remains t ⁰ principle goal of HF mixer design. The intermodulation performance and overload characteristics of a mixer are fundamental qualities used in the evaluation of a good design. Heretofore, most mixers sporting a high dynamic range have been either the passive diode-ring variety, or the active FET mixer.[1][2]

Common to both the diode and FET is their square-law characteristic so important in maintaining low distortion during mixing. However, equally important for high dynamic range is the ability to withstand overload that has been identified as a principle cause of distortion in mixing. [3] Some passive diode-ring mixer designs have resorted to paralleling of diodes to effect greater current handling, yet the penalty for this apparent improvement is the need for a massive increase in local-oscillator power.

This report examines a new FET mixer where commutation achieves high dynamic range without exacting the anticipated penalty of increased local-oscillator drive. Using the Siliconix Si8901, third-order intercept points upwards of +39 dBm (input) have been achieved with only +17 dBm of local-oscillator drive!

CONVERSION EFFICIENCY OF THE COMMUTATION MIXER

Unlike either the conventional diode-ring mixer or the active FET mixer, the commutation mixer relies on the switching action of the quad-FET elements to effect mixing action. Consequently, the commutation mixer is, in effect, no more than a pair of switches reversing the phase of the signal carrier at a rate determined by the local-oscillator frequency. Ideally, we would anticipate little noise contribution and, since the switching mixer, consisting of four "switches," has finite ON resistance, performance is similar to that of a switching attenuator. As a result, the conversion efficiency of the commutation mixer may be expressed as a loss.

This loss results from two related factors. First, is the r_{DS} of the MOSFET relative to the signal and IF impedances; second -- a more common and expected factor -- is the loss attributed to signal conversion to undesired frequencies. There are, however, ways to reduce the effects of undesired frequency generation by the use of filters.

The effect of r_{DS} of the MOSFETs may be determined from the analysis of the equivalent circuit shown in Figure 1, assuming that our local oscillator waveform is an idealized square-wave. It is not, but if we assume that it is, our analysis is greatly simplified; and for a commutation mixer, a high local-oscillator voltage begins to approach the ideal waveform of a square-wave.

Figure 1, showing switches rather than MOSFETs, also identifies the ON state resistance, r_{DS}, as well as the OFF-state resistance, r_{OFF}. The latter can be disregarded in this analysis as it is generally extremely high. On the other hand, the ON-state resistance, r_{DS}, together with the source and

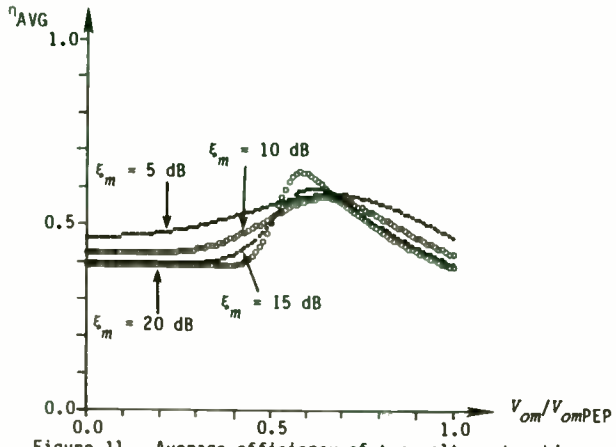

Figure 11. Average efficiency of two-voltage tracking with Laplacian-AM signals.

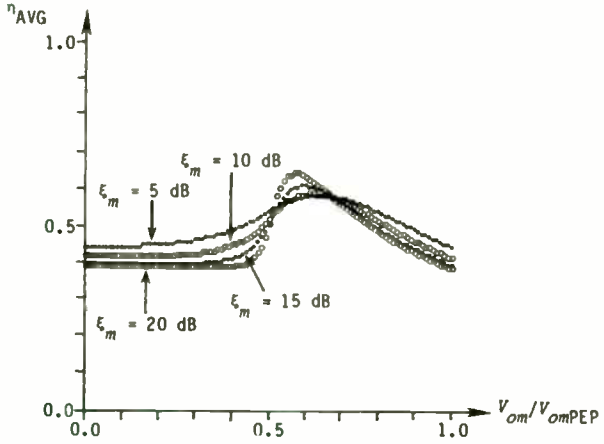

Figure 12. Maximum average efficiencies and corresponding voltage ratios.

added by envelope tracking are:

- PA gain and phase variation with supply voltage and
- Envelope distortion produced by finite switching time.

Gain and Phase Variation

Virtually all solid-state power transistors (whether BJT or FET) contain significant voltage-variable capacitance. In addition, most FETs have inherently nonlinear transfer characteristics. As a result, variation of the supply voltage produces unwanted amplitude and phase modulation of the output signal.

Typical curves of gain and phase variation for a bipolar RF-power transistor [11] suggest maximum deviations of 2 dB and 5°. However, the contours further suggest that simultaneous reductions in supply voltage and drive result in nearly constant gain and phase characteristics.

In general, determination of the carrier-to-intermodulation (C/I) level requires numerical evaluation based upon a particular signal and PA characteristic. However, some idea of the tolerable gain and phase changes can be obtained by considering the spectrum of squarewave modulation.

Squarewave amplitude modulation between two levels that differ by 0.42 dB results in third-order IMD products 30 dB below the carrier. Squarewave phase modulation produces third-order products whose amplitude is $2\Delta\phi/3\pi$ relative to a unity-amplitude carrier. Consequently, a phase jump of 5.7° (0.1 rad) produces a C/I ratio of 30 dB. It therefore appears that phase variations are not likely to be a problem, while gain variations must be compensated if they

load impedances (viz., signal and intermediate-frequency impedances) directly affects the conversion efficiency.

If we assume that our local-oscillator excitation is an idealized square-wave, the switching action may be represented by the Fourier series as,

$$\epsilon(x) = \frac{1}{2} + \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{\sin(2n-1)\,\omega t}{(2n-1)} \qquad \text{Eq. (1)}$$

The switching function, $\epsilon(t)$, shown in the derivative equivalent circuit of Figure 2, is derived from the magnitude of this Fourier series expansion as a power function by squaring the first term, viz., $(\frac{2}{\pi})^2$.

The available power that can be delivered from a generator of RMS open-circuit terminal voltage, V_{in}, and internal resistance, R_g, is,

$$P_{av} = \frac{V_{in}^2}{4R_g} \qquad \text{Eq. (2)}$$

or, in terms shown in Figure 3,

$$P_{av} = \frac{V_{in}^2}{\pi^2 R_g} \qquad \text{Eq. (3)}$$

The output power, deliverable to the intermediate-frequency port, is,

$$P_{out} = \frac{V_o^2}{R_L} \qquad \text{Eq. (4)}$$

To arrive at V_o, we first need to obtain the loop current, i_L, which from Figure 3, offers,

$$i_L = \frac{V_{in}}{\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}} \qquad \text{Eq. (5)}$$

then,

$$V_o = \frac{V_{in} R_L}{\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}} \qquad \text{Eq. (6)}$$

Combining Eqs. (4) and (6),

$$P_{out} = \frac{V_{in}^2 R_L}{[\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}]^2} \qquad \text{Eq. (7)}$$

Conversion efficiency -- in the case for the commutation mixer, a loss -- may be calculated from the ratio of P_{av} and P_{out},

$$L_c = 10 \log \frac{P_{av}}{P_{out}} \quad \text{dB} \qquad \text{Eq. (8)}$$

Substituting Eq. (3) for P_{av}, and Eq. (7) for P_{out}, we obtain,

$$L_c = 10 \log \frac{[\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}]^2}{\pi^2 R_L R_g} \quad \text{dB} \qquad \text{Eq. (9)}$$

The conversion loss represented by Eq. (9) is for a broadband double-balanced mixer with all ports matched to the characteristic line impedances. The ideal commutation mixer operating with resistive source and load impedances will result in having the image and all harmonic frequencies dissipated. For this case, the optimum conversion loss reduces to,

$$L_c = 10 \log \frac{4}{\pi^2} \quad \text{dB} \qquad \text{Eq. (10)}$$

or -3.92 dB.

However, a truly optimum mixer also demands that the MOSFETs exhibit an ON-state of zero Ohms, and, of course, an ideal square-wave excitation. Neither is possible in a practical sense.

Equation 9 can be examined for various values of source and load impedances as well as r_{DS} by graphical representation, as shown in Figure 4, re-

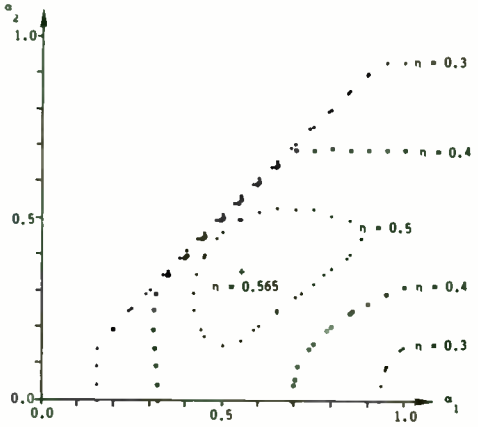

Figure 8. Average-efficiency contours for three-voltage tracking with Rayleigh envelope, ξ = 10 dB.

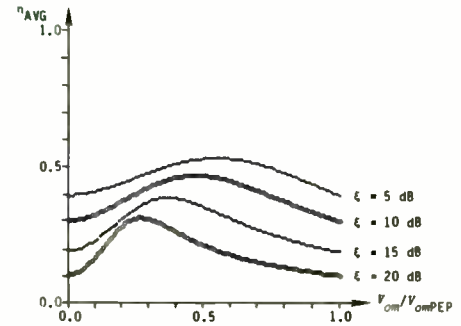

Figure 9. Average efficiency of two-voltage tracking with Laplacian envelope.

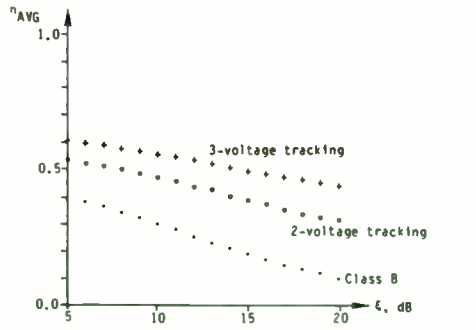

Figure 10. Maximum average efficiency for Laplacian envelope.

peak-to-average ratios of 5, 10, 15, and 20 dB. The maximum attainable average efficiency as a function of peak-to-average ratio is shown in Figure 10 and values of α are given in Table 1.

The average-efficiency characteristics for a Laplacian envelope are similar to those for a Rayleigh envelope. For a typical 10-dB peak-to-average ratio, the 30.8 percent efficiency of class B is increased to 47.5 percent by two-voltage envelope tracking, and to 55.5 percent by three-voltage envelope tracking.

Amplitude Modulation

The modulating signals for full-carrier AM typically have either Gaussian distributions (corresponding to music or the sum of a variety of sounds) or Laplacian distributions (corresponding to speech). The average-efficiency curves for two-voltage envelope tracking with these two signals are shown in Figures 11 and 12 for several modulation peak-to-average ratios.

The maximum average efficiencies and the corresponding transition voltages are given in Table 1. Since the RF peak-to-average ratio for these signals is relatively low, their average-efficiency characteristics are similar to those of the selected signals.

4. PRACTICAL CONSIDERATIONS

Application of envelope tracking requires consideration of intermodulation distortion (IMD) as well as efficiency. The two principal sources of IMD

membering that a nominal 3.92 dB must be added to the values obtained from the graph.

To illustrate how seriously the ON-state of the MOSFETs affects performance, we need only to consider the Si8901 with a nominal r_{DS} (at V_{GS}=15V) of 23 ohms. With a 1:1 signal transformer (50 to 25-0-25Ω), Rg/r_{DS} = 1.1. Allowing a 4:1 IF output impedance to a 50 ohm preamplifier, the ratio R_L/r_{DS} approximates 4. From Figure 4 we read a conversion loss, L_c, of approximately 3.7 dB, to which we add 3.92 dB for a total loss of 7.62 dB. Additionally, we must also include the losses incurred by both the signal and IF transformers. The results compare favorably with measured data.

A careful study of Figure 4 reveals what appears as an anomalous characteristic. If we were to raise R_g/r_{DS} from 1.1 to 4.3 (by replacing the 1:1 transformer with a 1:4 to effect a signal-source impedance of 100-0-100Ω), we would see a dramatic improvement in conversion efficiency! The anomaly is that this suggests that a mismatched signal-input port improves performance.

Caruthers [4] first suggested that reactively terminating all harmonic and parasitic frequencies would reduce the conversion loss of a ring demodulator to zero. This, of course, would also require that the active mixing elements (MOSFETs in this case) have zero r_{DS}, in keeping with the data of Figure 4.

A double-balanced mixer is a 4-port, consisting of a signal, image, IF and local-oscillator port. Of these, the most difficult to terminate is the image-frequency port simply because, in theory it exists as a separate port, but in practice it shares the signal port. Any reactive termination would, therefore, be narrow-band irrespective of its proximity to the active mixing elements.

The performance of an image-termination filter offering a true reactance to the image frequency (100% reflective) may be deduced to a reasonable degree from Figure 4, if we first presume that the conversion loss between signal and IF compares with that between signal and image. The relationship is displayed in Figure 5 where we see the expected variation in amplitude proportional to conversion efficiency (inversely proportional to conversion loss).

Image-frequency filtering affects more than conversion efficiency. As the phase of the detuned-short position of the image-frequency filter is varied we are able to witness a cyclical variation in the intermodulation distortion as has been confirmed by measurement, shown in Figure 6. By comparing Figure 5 with Figure 6, we see that any improvement in conversion loss appears to offer a corresponding degradation in the intermodulation distortion.

INTERMODULATION DISTORTION

Unbalanced, single-balanced and double-balanced mixers are distinguished by their ability to selectively reject spurious frequency components, as defined in table I. The double-balanced mixer, by virtue of its symmetry, suppresses twice the number of spurious frequencies as does the single-balanced mixer.

In the ideal mixer, the input signal is translated to an intermediate-

exceed 0.42 dB.

Switching Time

Delays in switching to the higher supply voltage can distort the envelope, producing IMD. In general, the C/I ratio depends upon both the type of signal and the transition ratio α. However, useful insight is obtained by considering the results of simulations of two-tone signals with $\alpha = 0.5$.

A pure delay in the voltage transition produces a C/I of 30 dB or more when the delay is less than 0.1 s / B(Hz). Similarly, a linear (ramp) transition between voltage levels produces a 30-dB or better C/I ratio provided the total risetime does not exceed 0.6 s / B(Hz). These do not appear to produce unreasonable switching-time requirements for most applications. For example, delays of up to 35 μs or risetimes of up to 200 μs can be tolerated for ordinary SSB voice with bandwidth B = 3 kHz.

5. CONCLUSIONS

Envelope tracking can be implemented by adding relatively simple and inexpensive hardware to an existing RF power amplifier. This paper shows that it can produce significant increases in average efficiency for amplitude-modulated signals with large peak-to-average ratios. The power-supply switching-time requirements are quite reasonable for voice-bandwidth signals. Envelope tracking should therefore be considered when improved efficiency is desired.

6. ACKNOWLEDGEMENTS

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frequency without distortion, viz., without imparing any of the contained information. Regrettably, the ideal mixer does not occur in practice. Because of certain nonlinearities within the switching elements as well as imperfect switching resulting in phase modulation, distortion results.

Identifying Intermodulation Distortion Products

The most damaging intermodulation distortion products (IMD) in receiver design are generally those attributed to odd-order, and, in particular, to those identified as the third-order IMD.

Any nonlinear device may be represented as a power series,

$$i_d = g_m e_g + \frac{1}{2!}\frac{\delta g_m}{\delta V_G} e_g^2 + \frac{1}{3!}\frac{\delta^2 g_m}{\delta V_G^2} e_g^3 + \ldots \frac{1}{n!}\frac{\delta^{n-1} g_m}{\delta V_G^{n-1}} e_g^n \qquad \text{Eq. (11)}$$

which can be further broken into

TERM	OUTPUT	TRANSFER CHARACTERISTIC
$g_m e_g$	F1, F2	Linear
$\frac{1}{2!}\frac{\delta g_m}{\delta V_G} e_g^2$	2F1, 2F2 F1 ± F2	[Second-order Square-Law]
$\frac{1}{3!}\frac{\delta^2 g_m}{\delta^2 V_G} e_g^3$	3F1, 3F2 2F1 ± F2 2F2 ± F1	Third-Order

The second term is the desired intermediate-frequency we seek, all other higher-orders are undesirable, but, unfortunately, present to a varyign degree as illustrated in Figure 7.

There are both fixed-level IMD products and level-dependent IMD products.[5] The former are produced by the interaction between a fixed-level signal, such as the local oscillator and the variable-amplitude signal. The resulting frequencies may be identified,

$$n\omega_1 \pm \omega_2 \qquad \text{Eq. (12)}$$

where, n is an integer greater than 1.

Level-dependent IMD products result from the interaction of the harmonics of the local oscillator and those of the signal. The resulting frequencies may be identified,

$$n\omega_1 \pm m\omega_2 \qquad \text{Eq. (13)}$$

where, m and n are integers greater than 1.

For a mixer to generate IMD products at the intermediate frequency we must account for at least a two-step process. First, the generation of the harmonics of the signal and local oscillator; and, second, the mixing or conversion of these frequencies to the intermediate frequency. Consequently, the mixer may be modelled as a series connection of two nonlinear impedances, the first to generate the harmonic products, the second to mix or convert to the intermediate frequency. Although many harmonically-related products are possible, we will focus principally on odd-order IMD products.

If we allow two interfering signals, f_1 and f_2, to impinge upon the first nonlinear element of our mixer model, the result will be $2f_1 - f_2$ and $2f_2 - f_1$. These are identified as third-order intermodulation products (IMD_3). Other products are also generated taking the form $3f_1 - 2f_2$ and $3f_2 - 2f_1$, called fifth-order IMD products (IMD_5). Unlike the even-order products, odd order products lie close to the fundamental signals and, as a consequence, are

most susceptible of falling within the passband of the intermediate frequency and thus degrading the performance of the mixer.

A qualitative definition of linearity based upon intermodulation distortion performance is called the Intercept Point. By recognizing that,

the fundamental output (IF) response is directly proportional to the signal input level;

the second-order output response is proportional to the square of the signal input level; and,

the third-order output response is proportional to the cube of the signal input level,

then convergence occurs. The point of convergence is termed the Intercept Point. The higher the value of this intercept point, the better the dynamic range.

Intermodulation Distortion in the Commutation Mixer

Although the double-balanced mixer outperforms the single-balanced mixer as we saw in Table I, a more serious source of intermodulation products result when the local-oscillator excitation departs from the idealized square-wave. [6][7] This phenomenon is easily recognized by a careful examination of Figure 8, where a sinusoidal local-oscillator voltage reacts not only upon a varying transfer characteristic but also on a varying nonlinear, voltage-dependent capacitance (not shown in Figure 8). Although the effects of this sinusoidal transition are not easily derived, Ward [8] and Rafuse [9] have concluded that lowering R_g will provide improved intermodulation performance! This conflicts with low conversion loss, as we saw in Figure 4.[10]

Further examination of Figure 8 reveals that the sinusoidal local-oscillator excitation results in phase modulation. That is, as the sinusoidal wave goes through a complete cycle, the resulting gate voltage, acting upon the MOSFET's transfer characteristic, produces a resulting nonlinear waveform. Since all FETs have some offset -- a JFET has a cut-off voltage; a MOSFET has threshold voltage -- it is important, for symmetry as well as for balance, to offer some DC offset voltage to the gates. Optimum IMD performance demands that the switches operate in a 50% duty cycle; that is, the switches must be fully ON and fully OFF for equal time. Without some form of offset bias this would be extremely difficult unless we were to implement an idealized square-wave drive.

Walker [11] has derived an expression showing the predicted improvement in the relative level of two-tone third-order intermodulation products (IMD_3) as a function of the rise and fall times of the local-oscillator waveforms.

$$20 \log \left[\frac{\left[t_r \, \omega_{LO} \, \frac{V_\delta}{V_c} \right]^2}{8} \right] \text{ dB} \qquad \text{Eq. (14)}$$

where, V_c is the peak-to-peak local-oscillator voltage,

V_δ is the peak signal voltage,

t_r is the rise and fall time of V_c,

ω_{LO} is the local-oscillator frequency.

Equation 14 offers us several interesting aspects on performance. Since any reduction in the magnitude of V_s improves the IMD, we again discover that lowering R_g (which, in turn, decreases the magnitude of V_s) appears to bene-

Direct Single Sideband Modulation of Transmitter Output Switcher Stages

Florin G. Tinta

Abstract

A new technique allows to obtain Single Sideband (SSB) Pulse Duration Modulation without using intermediate DSB signals.

The technique employs instantaneous voltage comparison between modulating and carrier waveforms and between their harmonic conjugates. Timing signals are generated at instantaneous value equality. Through a set of logic gates, these timing signals are applied to a system of master flip-flops, driving switching output stages for power RF transmitters.

In the simplest implementation two such master flip-flops drive differentially the halves of a switching bridge generating a three-level output (1,0,-1). All digital FFT based real-time processing can generate output signals free of the third and all even harmonics using high efficiency five-level bridges operated in the top 92% of their nominal power output.

I INTRODUCTION

In general, SSB signals are obtained from Double Sideband Suppressed Carrier (DSB) signals. DBS modulators have always been used as a first explicit processing step of the transmitted signal.

The most conventional method consists in eliminating one of the sidebands of the DSB signal by filtering at low power level.

A second method uses phase shifting and several versions of this phase-shift method exist [1], [2]. The output of two DSB modulators supplied with harmonic conjugate (i.e., 90° phase shifted) modulating and carrier waveforms are combined by linear addition. This cancels one of the sidebands and enhances the other if the modulators and the phase-shifting networks are ideal. It implies perfect balancing of modulator non-linearities and requires practically very delicate control of amplitudes and phases.

A third method [3] for SSB generation has four DSB modulators, low-pass filters and a final adding circuit. Again, perfect balancing is required for mutual cancellation of the unwanted sidebands.

Pulse Duration Modulation (PDM or PWM) can be applied directly for amplitude modulation of RF carriers [4].

The pulse duration is tailored in such a way that there is a linear relation between the magnitude of the modulating signal and the fundamental amplitude of the pulse train. As a result, the pulse duration is related to the

fit performance. Second, the higher the local-oscillator voltage the better the IMD performance. Third, if we can provide the idealized square-wave drive we achieve infinite improvement in IMD performance!

An additional fault of sinusoidal local-oscillator excitation results whenever the wave approaches the zero-crossing at half-period intervals. As the voltage decays we find that any signal votlage may overload the MOSFETs causing intermodulation and crossmodulation distortion.[12] This can be easily visualized from Figure 9 where we see the classic i-e characteristics of the MOSFET at varying gate voltages. Only at substantial gate voltage do we witness reasonable linearity, and consequently, good dynamic range.

DYNAMIC RANGE OF THE COMMUTATION MIXER

As the two-tone Intercept Point increases in magnitude, we generally conclude a like improvement in dynamic range results. Yet, as we have concluded from earlier study, the intermodulation products appear to be a function of both the generator or source impedance as well as the ratio R_g/r_{DS} and R_L/r_{DS} (see Figure 4).

In any receiver performance can be quantified by the term Dynamic range. Dynamic range can be extended by improving the sensitivity to low-level signals and by increasing the power-handling ability without being overcome by interfering intermodulation products or the effects caused from desensitization.

There are rules to follow if we are to improve the low-level signal sensitivity. Ideally we would like a mixer to be transparent, acting only to manipulate the incoming signals for easy processing by subsequent equipment. The perfect mixer would have no conversion loss and a zero noise figure. However, in the preceeding analysis we discovered that optimum intermodulation performance occurred when the signal-input port is mismatched to the quad MOSFETs (Figure 4). It now becomes clear that a performance trade-off appears necessary. Either we seek low conversion loss and with it a lower noise figure, or we aim for the highest two-tone intercept point. Fortunately, as we seek the latter, our dynamic range will actually improve since a mismatched signal port has less effect upon the signal-to-noise performance of the mixer than does a matched signal port have upon the intermodulation distortion.

Convention has identified minimum sensitivity to be the weakest signal which will produce an output signal 10 dB over that of the noise in a prescribed bandwidth (usually 1 kHz), or

$$Sens. = 20\ Log\ \frac{V_S + V_N}{V_N} + 10\ dB \qquad \text{Eq. (15)}$$

Desensitation occurs whenever a nearby unwanted signal causes the compression of the desired signal. The effect appears as an increase in the mixer's conversion loss.

THE Si8901 AS A COMMUTATION MIXER

Because of package and parasitic constraints, the Si8901 appears best suited for performance in the HF to low VHF region. A surface-mounted version may extend performance to higher frequencies.

In our review of intermodulation distortion we recognized that to achieve

magnitude of the modulating signal in a non-linear way. The fundamental amplitude A_1 of a periodic sequence of bipolar pulses of duration t_o, period T_c and unit amplitude is given by:

$$A_1 = 4/\pi \sin(\pi t_o/T_c) \quad (1)$$

This relation leads to modulation techniques based on instantaneous voltage comparison between a sinusoidal carrier and the modulating signal. This will be discussed later in more detail. Full amplitude modulated transmitters using such techniques have been built [5]. Possible extension to the generation of DSB signals has been also indicated [5] and practical circuits presented [6]. Indirect generation of SSB signals by adding phase shifted DSB PDM appears also feasible. Limitations of methods of combining outputs of DSB modulators have been mentioned [5]. Alternative ways of producing SSB PDM signals using Kahn's approach [7] were considered. The method of envelope elimination and restoration has received some refinements by using feedback loops[8]. Nevertheless, this approach has some inherent limitations in the phase tracking circuit (for complex and extended dynamic range modulating signal) and is basically indirect, in the sense that the SSB signals are generated by conventional means at low level. A PDM power amplifier using transistor switching bridges for the envelope restoration allowed to obtain an SSB transmitter with unusually high efficiency [9].

The object of the following paper is the generation of SSB PDM waveforms without the explicit use of DSB signals at a level of efficiency at least comparable with the best AM PDM modulated systems. Digital processing of the transmitted signal makes it possible to generate more efficient waveforms which are reducing loss in harmonic power and filtering circuit difficulties.

II SWITCHING CONCEPTS

a. DSB Pulse Duration Modulator

This is presented mostly for conceptual definitions. Figure 1 shows the block diagram of a Double Sideband Suppressed Carrier Pulse Duration Modulator designed to drive differentially a full switching bridge. Two master flip-flops, F1 and F2 are triggered by two pairs of voltage comparators C1 and C2.

The modulating signal in "normalized" to the carrier amplitude, i.e., its amplitude to smaller and at most equal (for m = 1) with the amplitude of the carrier.

The first comparator pair C1 receive the carrier c(t) and the modulating signal s(t) while for the second comparator pair the sign of one of these voltages is reversed.

At instantaneous voltage equality one can have "positive" or "negative" crossing of the applied waveforms if one connects the relative magnitude of their first time derivatives and it is rather simple to produce separate signals corresponding to these two situations.

In the example selected in Figure 1, one uses distinct comparators. C1+ produces a positive trigger forming pulse when the carrier exceeds the modulating signal immediately after crossing, while C1- produces the positive trigger where the carrier "goes under" the modulating signal.

a high intercept point the local-oscillator drive must

approach the ideal square-wave;

ensure a 50% duty cycle; and,

offer sufficient amplitude to ensure a full ON and OFF switching condition, as well as to offer reduced r_{DS} when ON.

Furthermore, to maintain superior overall performance -- in conversion loss, dynamic range (noise figure) and intercept point -- some form of image frequency termination would be highly desirable even though, understandably, the mixer's bandwidth would be restricted. Consequently, the principal effort in the design of a high dynamic range commutation mixer is two-fold. First, and most crucial, is to achieve a gating or control voltage sufficient to ensure a positive and hard turn-ON as well as a complete turn-OFF of the mixing elements (MOSFETs). Second, and of lesser importance, is to properly terminate the parasitic and harmonic frequencies developed by the mixer.

Establishing the Gating Voltage

Local-oscillator injection to the conventional diode-ring, FET, or MOSFET double-balanced mixer is by the use of the broadband, transmission-line, transformer, [13] as shown in Figure 10. For the diode-ring mixer where switching is a function of loop current, or for active FET mixers that operate on the principle of transconductance and thus need little gate voltage,[14] the broadband transformer is adequate. If this approach is used for the commutation mixer, we would need extraordinarily high local-oscillator drive to ensure positive turn-ON. Rafuse [15] and Ward [16] used a minimum of 2 W to ensure mixing action; Lewis and Palmer [17] achieved high dynamic range using 5 Watts! The MOSFETs used in these early designs were p-channel, enhancement (2N4268) with moderately high threshold (6 V max.) and high input capacitance (6 pF max.). All of these early MOSFET double-balanced mixers relied on the conventional 50 to 100-0-100Ω transformer for local-oscillator injection to the gates.

A major goal is the conservation of power. This goal cannot be achieved using the conventional design. Simply increasing the turns ratio of the coupling transformer is thwarted by the reactive load presented by the gates.

The obvious solution is to use a resonant gate drive. The voltage appearing across the resonant tank -- and thus on the gates -- may be easily calculated,

$$V = (P \cdot Q \cdot X)^{\frac{1}{2}} \qquad \text{Eq. (16)}$$

P is the power delivered to the resonant tank circuit;

Q is the loaded Q of the tank circuit; and,

X is the reactance of the gate capacity.

Since the gate capacitance of the MOSFET is voltage dependent, the reactance of the gate becomes dependent upon the impressed excitation voltage. To allow this would severely degrade the IMD performance of the mixer. However, we can minimize the change in gate capacitance and remove its detrimental influence using a combination of substrate and gate bias, as shown in Figure 11. Not only does this show itself beneficial in this regard, but, as we saw in Figure 8, a gate bias is necessary to ensure the required 50% duty cycle. Furthermore, a negative substrate voltage ensures that each MOSFET on the monolithic substrate is electrically isolated and that each source-/drain-to-body

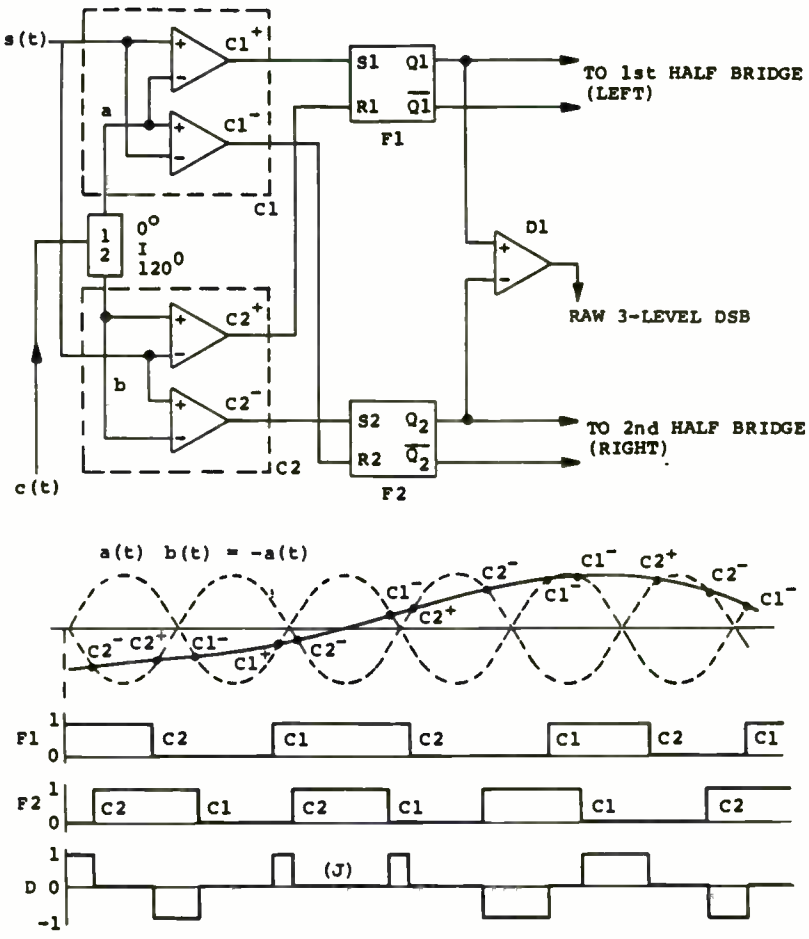

Figure 1. DSB Pulse Duration Modulation

The second comparator pair operates in a similar way. The situation shown in Figure 1 corresponds to a 180° phase shift of the carrier.

F1 is set at positive crossings s(t) by c(t) and reset at positive crossings of s(t) by -c(t).

F2 is set by negative crossings of s(t) by -c(t) and reset at negative crossings of s(t) by c(t).

The outputs of F1 and F2 shown in Figure 1 correspond to a sinusoidal carrier and slow-varying, sign-changing modulating signal. They drive the independently controlled halves of a three-level switching bridge whose basic arrangement is indicated in Figure 2. Biasing, snubbering and circuit details are left aside for clarity.

One can see from that in this arrangement the output signal delivered by the transformer U depends upon the difference of the switching commands given by F1 and F2. For a bipolar (output), PDM requires at least a three-state or three-level (1,0,-1) configuration.

In a three-level bridge, such a differential arrangement has definite advantages in switching conditions for transistors, easing snubbing problems. It is evident that at zero mediated transitions, the U-C circuit will include a pair of conducting transistors (Q1 and Q2, Q3 and Q4).

Of course, an identical three-level waveform can be obtained by using a less sophisticated difference circuit, also represented in Figure 1.

diode is sufficiently reverse biased to prevent half-wave conduction.

Implementing the resonant gate drive may take any of several forms. The resonant tank circuit may be merged with the oscillator, or it can be a varactor tuned Class B stage, [18] or, as in the present design, an independent resonant tank, shown in Figure 12.

To ensure symmetrical gate voltage in 180° anti-phase, if the local oscillator drive is asymmetrical, viz., fed by unbalanced coax, an unbalanced-to-balanced balun must be used (T1 in Figure 12), otherwise capacitive unbalance results with an attendant loss in mixer performance.

Table II offers an interesting comparison between a resonant-gate drive with a loaded tank Q of 14 and a conventional gate drive using a 50 to 100-Ω-100Ω transformer. The importance of a high tank Q is graphically portrayed in Figure 13. The full impact of a high gate voltage swing can be appreciated by using Equation 14. Here, as V_c (gate voltage) increases the intermodulation performance (IMD) also improves as we might intuitively expect. Calculated and measured results are shown in Figure 14 and demonstrate reasonable agreement. The difference may reflect problems encountered in measuring V_c as any probe will inadvertently load, or detune, the resonant tank even with the special care that was taken to compensate.

If we have the option to choose "high side" or "low side" injection -- viz., having the local-oscillator frequency above (high) or below (low) the signal frequency -- a closer inspection of Equation 14 should convince us to choose low-side injection.

Terminating Unwanted Frequencies

If our mixer is to be operated over a restricted frequency range where the local oscilator and signal frequencies can be manipulated, image-frequency filtering may be possible. Image-frequency filtering does affect performance. For high-side local-oscillator injection an elliptical-function low-pass filter, or for low-side injection a high-pass filter might offer worthwhile improvement. In either case, the filter offers a short-circuit reactance to the image frequency forcing the image to return once again for demodulation. The results of using a low-pass filter with the commutation mixer are known from our earlier examination of Figures 5 and 6.

The resonant-gate drive consisting of a high-Q tank offers adequate bypassing of the intermediate frequency and image frequency.

If the IF is narrow band, filtering may be possible by simply using a resonant LC network across the primary of the transformer. [19]

Design Techniques in Building the Commutation Mixer

The mixer was fabricated on a high-quality double-copper clad board (PCB) shown in Figure 15. An improvised socket held the Si8901. The signal and IF ports used Mini-Circuits, Inc., plastic T-case RF transformers. For the IF, the Mini-Circuits T4-1 (1:4); for the signal, the Mini-Circuits T1-1T (1:1) or T4-1 was used. The resonant tank was wound on a ¼-inch ceramic form with no slug. The unbalanced-to-balanced resonant tank drive used a T4-1. The schematic diagram, Figure 16, is for a commutation mixer with high-side injection, operating with an IF of 60 MHz.

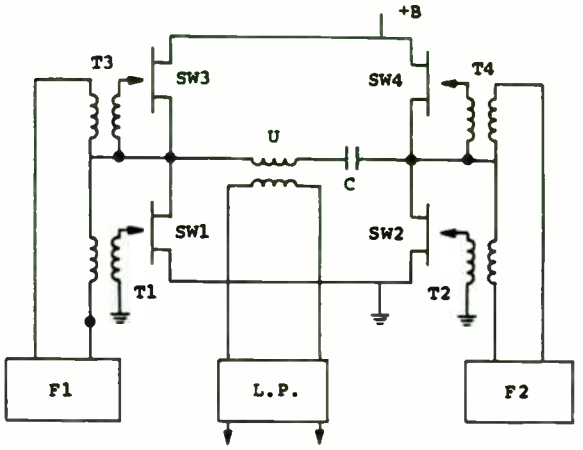

Figure 2. Three Level (Bipolar) PDM Bridge

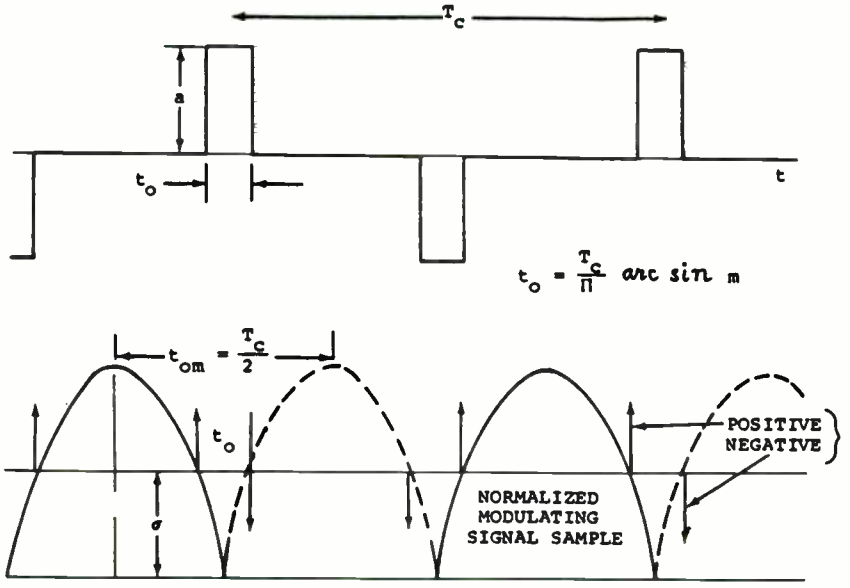

Figure 3. Bipolar Pulse Duration Moduation by a DC Signal

This waveform satisfies condition (1) for a DBS (SC) radio frequency Pulse Duration Modulation. The duration of a pulse defined by the alternating crossing of 180° phase shifted carrier waveforms satisfies the equivalent relation:

$$t_o = T_c/\pi \text{ arc sin } m \qquad (2)$$

Figure 3 illustrates the situation for a constant normalized modulating signal of amplitude m (the modulation index). Polarity reversal of the modulating signal (region j in Figure 1) results in the 180° phase shift characteristic of DSB (SC) modulated signals.

b. Three Level SSB Pulse Duration Modulator

The switching bridge of Figure 2 can be used to generate bipolar SSB PDM signals. A different control of the two driving flip-flops is required.

In Figure 4, F1 and F2 are controlled by a combination of command signals originated in four pairs of comparators and logic gates. An upper side band PDM signal is generated by this arrangement; the lower side band can be alternatively generated by reversing a couple of internal connections. Like in the phase-shifting method [2] [3] harmonic conjugates of at least the modulating signal are generated by 90° (or 45° alternates) phase shifting all pass filters, but the similarity ends at this point. An explicit DSB is nowhere generated in this circuit.

Comparator pairs C3 and C4 are supplied with the modulating and carrier signals, the latter being shifted with 180° in phase (sign reversal) for C4.

The principle effort involved the design of the resonant-gate drive. This necessitated an accurate knowledge of the gate's total capacitive loading effect. To accomplish this a precision fixed capacitor (5 pF) was substituted for the Si8901 and at resonance it was a simple task to calculate the inductance of the resonant tank. Substituting the Si8901 made it again a simple task to determine the capacitive effect of the Si8901. Once known, a high-Q resonant tank can be quickly designed and implemented. To ensure good interport isolation, symmetry is important, so care is necessary in assembly to maintain mechanical symmetry, especially with the primary winding.

Performance of the Si8901 Commutation Mixer

The primary goal in developing a commutation double-balanced mixer is to achieve a high dynamic range. If this task can be accomplished with an attendant savings in power consumption, then the resulting mixer design should find wide application in HF receiver design.

The following tests were performed.

Conversion efficiency (loss)
Two-tone, 3rd-order Intercept Point
Compression level
Desensitization level
Noise Figure

Conversion loss and Intercept Point are directly dependent upon the magnitude of the local-oscillator power. The mixer's performance is offered in Figure 17, where the input intercept is plotted with conversion loss.

Both the compression and desensitization levels may appear to contradict reason. Heretofore, conventional diode-ring demodulators exhibiting compression and desensitization levels an order of magnitude below the local-oscillator power level. However, with a commutation MOSFET mixer, switching is not accomplished by the injection of loop current but by the application of gate voltage. At a local-oscillator power level of +17 dBm (50 mW), the 2 dB compression level and desensitization level was +30 dBm! The single-sideband HF noise figure of 7.95 dB was measured also at a local-oscillator power level of +17 dBm.

CONCLUSIONS

Achieving a high gate voltage to effect high-level switching by means of a resonant tank is not a handicap. Although one might at first label the mixer as narrow-band, in truth the mixer is wideband. For the majority of applications, the intermediate frequency is fixed, that is, narrow band. Consequently, to receive a wide spectrum of signal frequencies the local oscillator is tuned across a similar band. In modern technology this tuning can be accomplished by numerous methods. Likewise the resonant tank may take several forms. It can be part of the oscillator, or, as in Ref. (18), it can be a varactor-tuned driver electroncially tracking the local oscillator.

If the local-oscillator drive was processed to offer a more rectangular waveform, approaching the idealized square-wave, we might then anticipate even greater dynamic range as predicted by Equation 14.

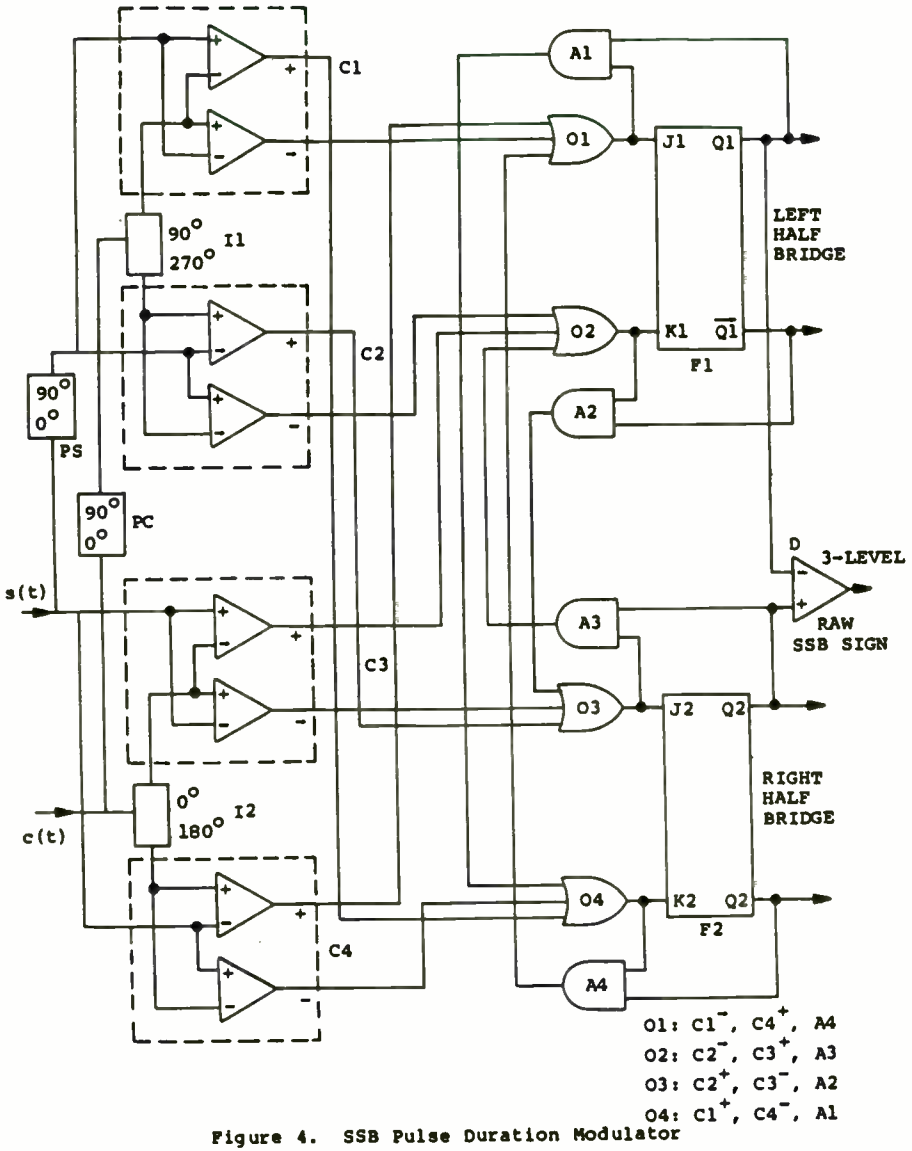

Figure 4. SSB Pulse Duration Modulator

Comparator pairs C1 and C2 are supplied with the harmonic conjugates [1] of the same signals. This implies the use of 90° (or 45° alternates) phase shifting all pass filters for the modulating signal at least. For a sinusoidal carrier a single frequency phase shifter can be employed.

Regular as well as J-K type flip-flops may be used. In Figure 4, clock inputs for J-K flip-flops and some delay circuits have been not represented in order to preserve with more clarity the basic concept. Clock signals can be used for further refinements of this modulation technique.

The outputs of F1 and F2 (which are not DSB PDM signals) are applied differentially to the switching bridge of Figure 2. The bridge produces three level waveforms which in general may contain successive pulses of the same polarity. One can show that for carrier to modulating signal frequency ratios R>3 the maximum number of successive pulsed of same polarity is two. Figure 5 shows the particular case of the upper SSB PDM signal produced for R = 3, at a modulating index m = .65. The sequence is bipolar, with no successive pulses of same polarity.

For m = 1, the SSB pulse duration modulation produced by this technique uses the full half period, i.e., generates a square wave with direct transitions from +1 to -1 and vice versa and gets the maximum power which can be generated by a full switching bridge.

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Single-Balanced	Double-Balanced
f_s	
$3f_s$	
$5f_s$	
f1 ± f2	f1 ± f2
f1 ± 3f2	f1 ± 3f2
f1 ± 5f2	f1 ± 5f2
2f1 ± f2	
2f1 ± 3f2	
3f1 ± f2	3f1 ± f2
3f1 ± 3f2	3f1 ± 3f2
4f1 ± f2	
5f1 ± f2	5f1 ± f2

A Comparison of Modulation Products in Single and Double Balanced Mixers to the 6th Order

TABLE I

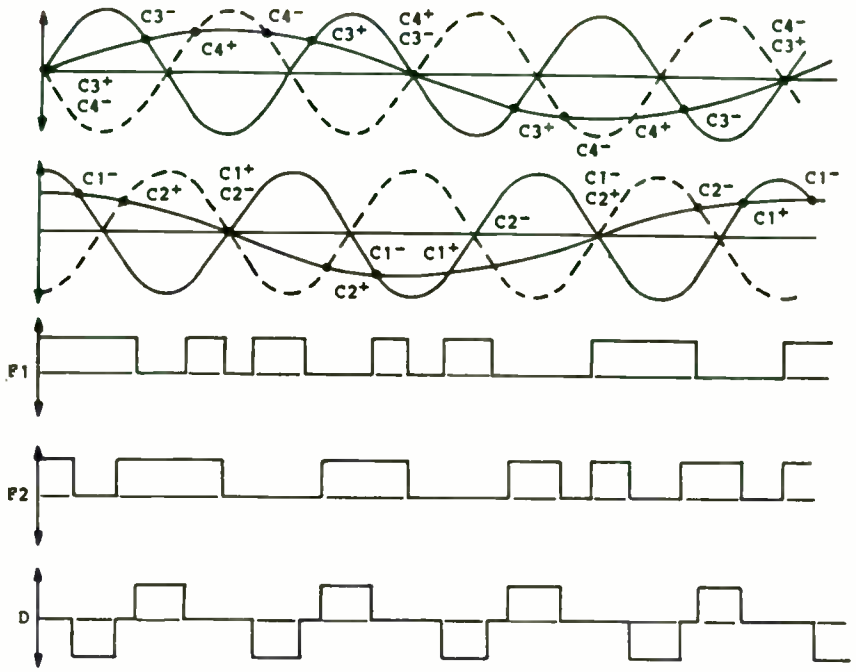


Figure 5. Direct Generation of Constant Amplitude Raw SSB Signal (m = .65, R = 3)

This can be simply demonstrated by considering sinusoidal constituents of the modulating and carrier waveforms. Let us consider the time angle θ_c of the carrier when the instantaneous values of the modulating sinusoid of amplitude m and of a sinusoidal carrier of unit amplitude become equal in absolute value. The time angle for the modulating signal is θ_c/R, where $R = f_c/f_m$. Both angles are measured from a common origin. Flip-flop transitions appear when:

$$\sin \theta_c = \left| m \cdot \sin (\theta_c/R) \right| \qquad (3)$$

The absolute value condition represents the fact that conjugate comparator pairs receive sign changed carrier signals.

Equation (3) is transcendental and can be solved by numerical methods (one of the solutions has been used in Figure 5).

If m = 1, we have $\sin \theta_c = \left| \sin \theta_c/R) \right|$ (4)

and the solutions are given by the following:

$$n \cdot \pi \pm \theta_c = \theta_c/R \qquad (5)$$

The solutions of equation (7) extend to all trigonometric functions and in particular to

$$\cos \theta_c = \left| \cos (\theta_c/R) \right| \qquad (6)$$

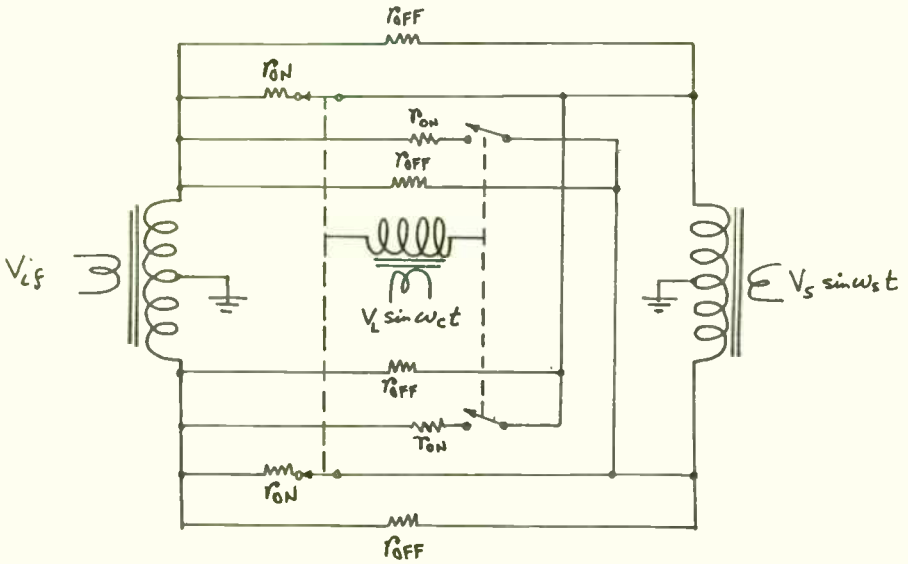
which represents the condition for instantaneous value equality of the harmonic conjugate waveforms.

This means that upward and downward transitions in the paired flip-flop outputs Q1 and $\overline{Q1}$, Q2 and $\overline{Q2}$ (Figure 4) are simultaneous. This implies two level transitions from 1 to -1 and vice versa. The result is a square wave: QED.

Power in (mW)	NR Gate Voltage (V)	Res Gate Voltage (V)
10	0.20	5.4
20	0.29	7.7
30	0.33	9.4
60	0.44	13.3

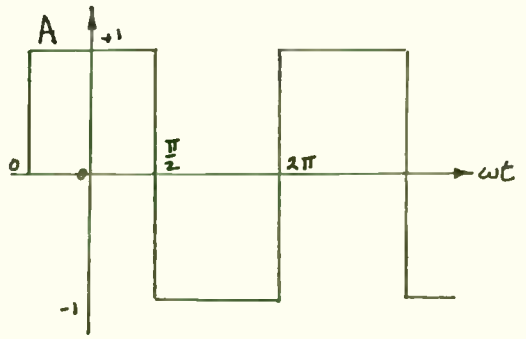
Comparison of a-c gate voltage veraus local-oscillator drive between a non-resonant (NR) and resonant (Res) tank with a loaded Q of 14 (Freq. 150 MHz)

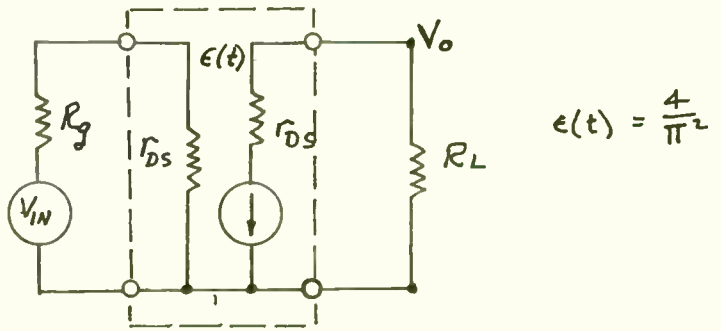
TABLE II



EQUIVALENT CIRCUIT OF COMMUTATION MIXER

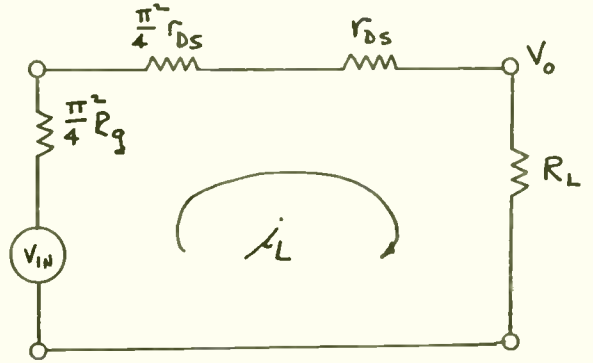
FIGURE 1





DERIVATIVE EQUIVALENT CIRCUIT

FIGURE 2



THE POWER-LOOP CIRCUIT WITH ALL ELEMENTS EQUIVALENT, BASED ON THE TRANSFER FUNCTION, $\epsilon(t) = 4/\pi^2$

FIGURE 3

III DIGITAL GENERATION OF SSB-PDM SIGNALS

A review of digital alternatives of the operations involved in SSB-PDM generation is given below. In addition, the case of five level (2,1,0,-1,2) switching bridges is considered. For multi-level switching bridges which can generate waveforms with reduced harmonic content at high power level, analog approaches, although possible for a certain dynamic range, do not seem practical.

The relative situation of SSB-PDM generation methods is given in Figure 6. For generality indirect methods based on low level analog DSB/SSB signal production followed by envelope AM-PDM restoration are also indicated. Dotted lines show various possible combinations of methods.

a. Harmonic Analysis and Conjugation of Signals

The modulating signal can be sampled and subject to real-time FFT processing for bandwidths covering at least the audio frequency range by using now readily available microprocessors and allied circuits. This may constitute a first step for digitally generating 90° phase shifted response, i.e., the harmonic conjugate of the modulating signal.

For the carrier quadrature signals can be simply generated by divide-by-four flip-flops [10].

Initially, the application of SSB-PDM signal generation was considered for emergency transmissions in the LF

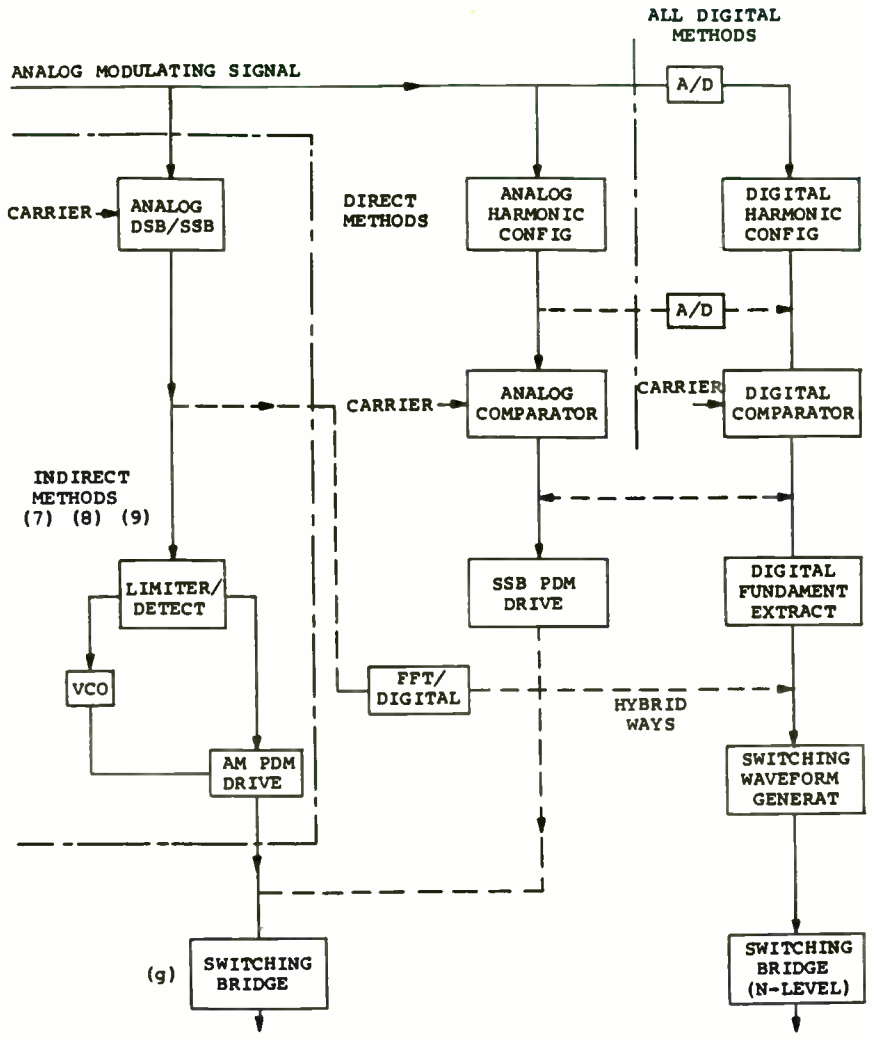
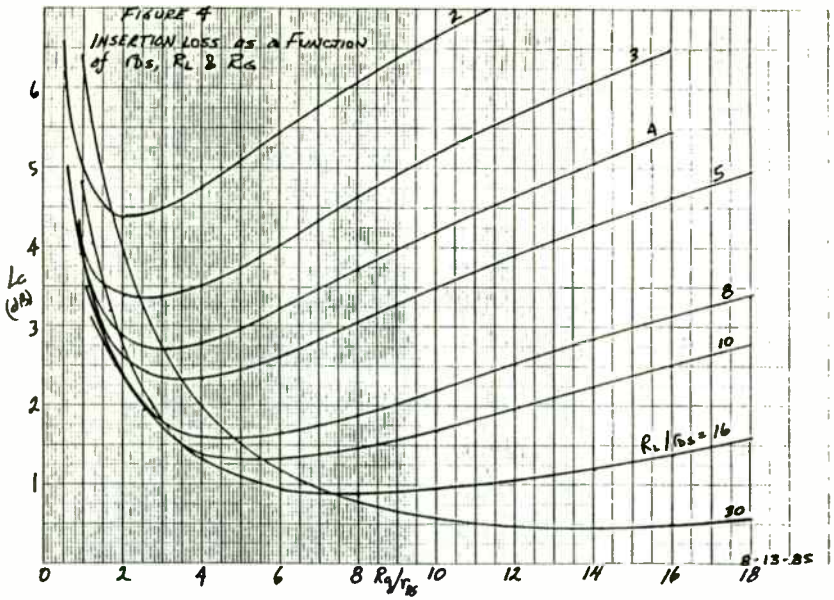
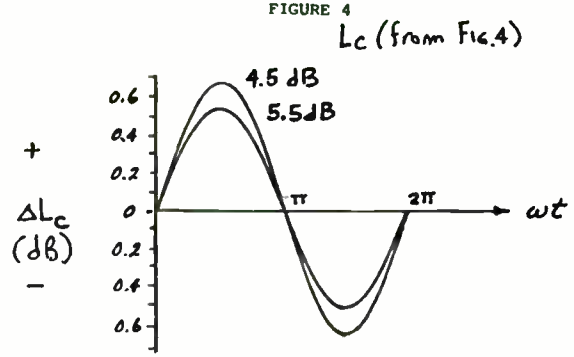


Figure 6. Map of SSB PDM Methods



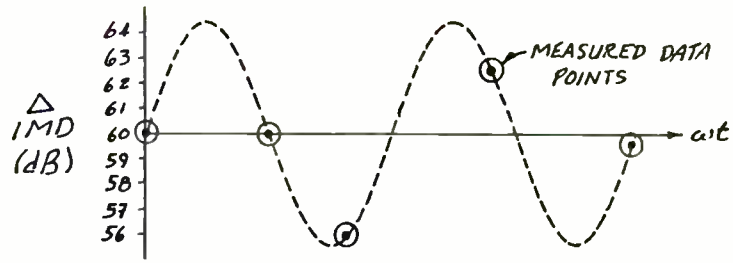
INSERTION LOSS AS A FUNCTION OF r_{DS}, R_L, & R_G

FIGURE 4



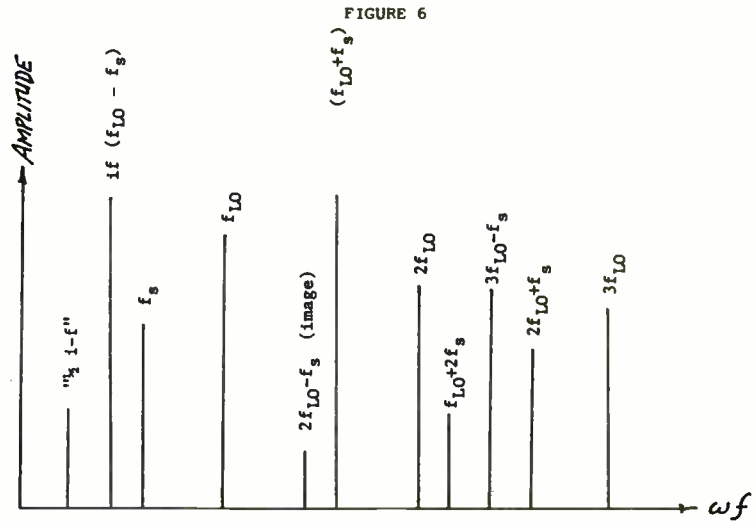
EFFECT OF IMAGE TERMINATION ON
CONVERSION LOSS

FIGURE 5



EFFECT OF IMAGE TERMINATION ON
3rd-ORDER DISTORTION

FIGURE 6



THE HARMONIC & SPURIOUS CONTENT
EXITING THE IF PORT OF THE
COMMUTATION MIXER

FIGURE 7

range, but it appears that with fast processors the scope and the frequency range of such transmissions can be considerably enlarged.

Digital harmonic conjugation of signals will not be discussed further in this paragraph. Analog constant phase delay, all pass filters have been constructed over wide frequency ranges. Our experience showed that they can be very adequate for carriers in the 2 to 32 MHz range (4 octaves) in spread spectrum transmission techniques.

b. Digital Comparison

High resolution video frequency A/D are commercially available. The digitized modulating signal can be compared with the stored or analytically generated carrier waveform, at a normalized scale.

Negative and positive waveform crossing in the sense defined previously can be easily defined and their timing accuracy is determined by the clock rate ratio to the highest frequency involved in the signals.

This operation can be done in parallel (or in a serial way, by successive sampling) for sign changed carrier and for the harmonic conjugated of the modulating signals generated in either analog or digital way.

c. Digital Evaluation of the SSB Fundamental

The fact that the SSB-PDM signal is a succession of pulses of constant amplitude makes the evaluation of the fundamental component by numerical methods straightforward. Because no power generation is considered at this level, it is advantageous to use unipolar (1,0) pulse sequences instead of bipolar (1,0,-1).

Th fundamental can be simply evaluated by the sum of sampled values of a sinusoidal by the gated clock pulses.

The simplicity of operations involved allows their implementation in real time with the help of now commercially available microprocessors, for ranges of modulating and carrier signals covering many telecommunications applications.

Digital evaluation of the fundamental for an analog generated SSB is somewhat more complex, but still it can be performed in real time using FFT algorithms. This is indicated in Figure 6 as a hybrid way which may be considered an extension of the Kahn's method [7].

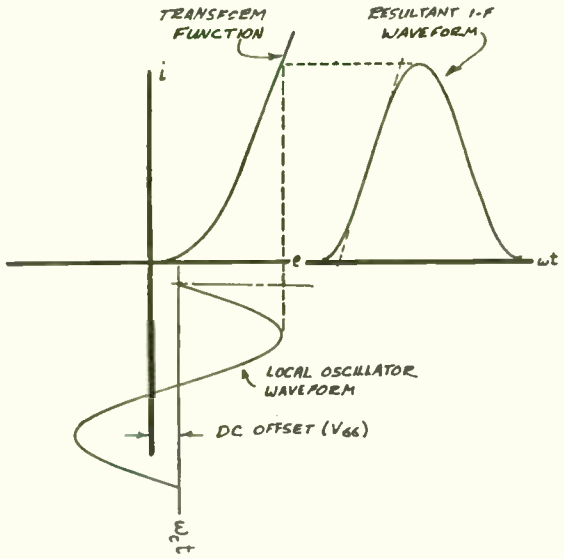
d. Five Level Switching Bridges

Bipolar five level waveforms generation can be generated by a switching bridge of the type represented in Figure 7. The normalized (supply) levels are 2,1,0,-1 and-2. A generic example is given in Figure 8a.

Up to a scale factor of $\pi/4$, the fundamental amplitude is given by:

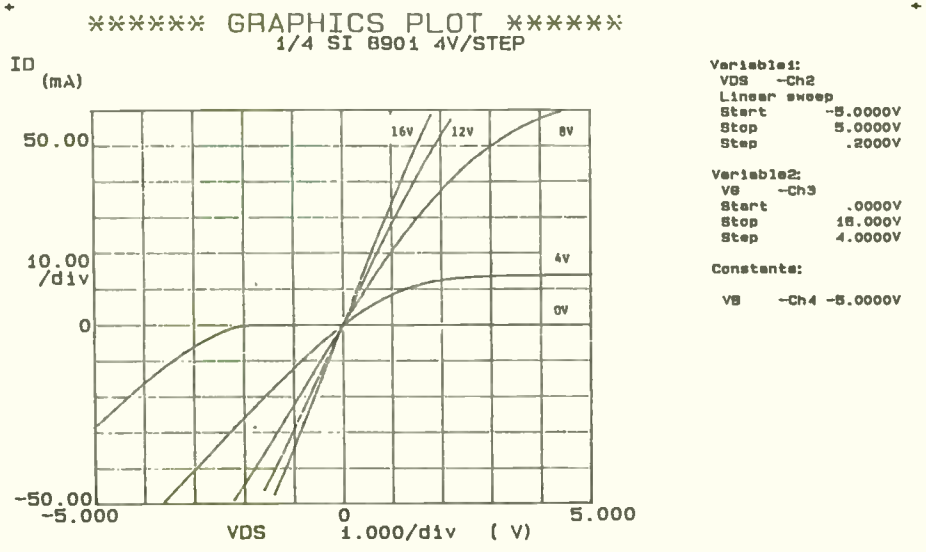
$$A = \int_0^u 2 \cos wdw + \int_u^v \cos wdw = \sin u + \sin v$$

$$A = 2 \sin \frac{u+v}{2} \cos \frac{u-v}{2} \qquad (7)$$



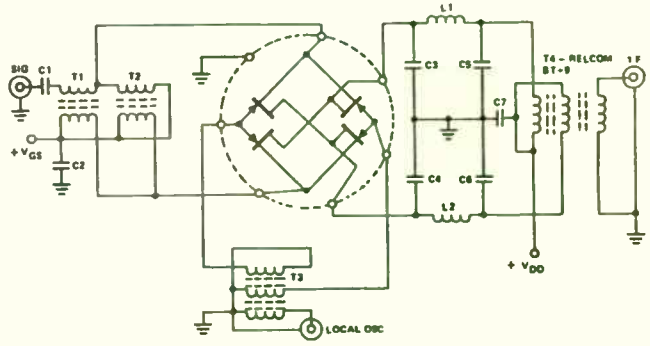
EFFECT OF SINUSOIDAL LOCAL OSCILLATOR WAVEFORM ON IF LINEARITY

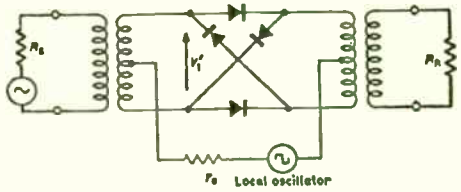
FIGURE 8



FIRST & THIRD QUADRANT I-E CHARACTERISTICS SHOWING EFFECTS OF GATE VOLTAGE LEADING TO LARGE SIGNAL OVERLOAD DISTORTION

FIGURE 9





LOCAL OSCILLATOR DRIVE USING CONVENTIONAL BROADBAND TRANSFORMERS

FIGURE 10

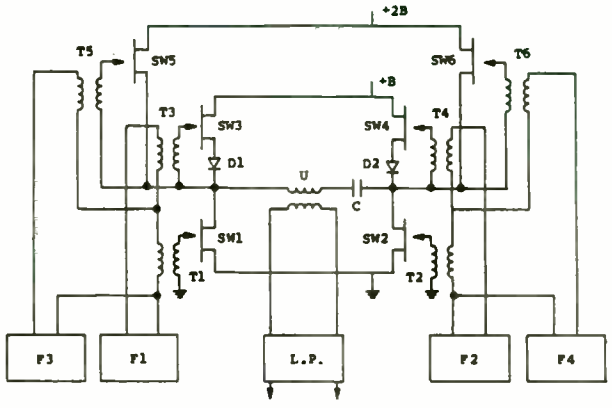


Figure 7. Five Level (Bipolar) Switching Bridge

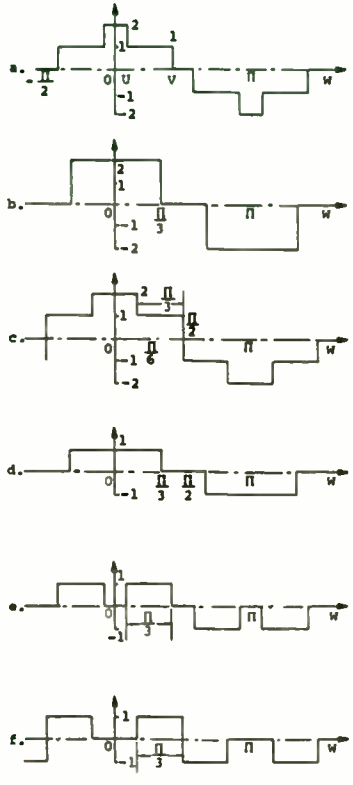


Figure 8. Switching Waveforms Eliminating the 3rd Harmonic in SSB PDM

Natural limitations can be described by:

$$\pi/2 \geq v \geq u \geq o \qquad (8)$$

The symmetry of the waveform eliminates even harmonics.

The third harmonic can be eliminated if:

$$\sin 3u + \sin 3v = o \qquad (9)$$

which, considering (8) leads to the conditions:

$$v - u = \pi/3 \qquad (10)$$

or

$$v + u = 2\pi/3 \qquad (11)$$

The fundamental amplitude of a five level waveform satisfying (10) results from (7).

$$A(\beta) = 2 \sin \frac{u+v}{2} \cdot \frac{\sqrt{3}}{2} = \sqrt{3} \sin(v - \pi/6) \qquad (12)$$

This relation indicates that an analog timing method similar to the one presented in Section II is possible.

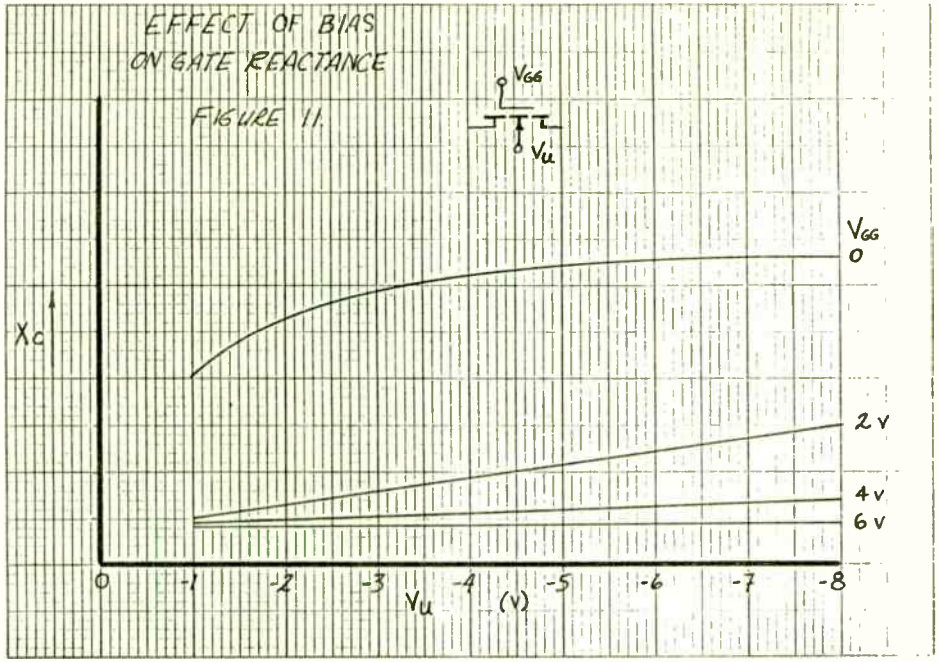
Condition (11) leads to a different relation:

$$A(\beta) = \sqrt{3} \cos(v - \pi/3) \qquad (13)$$

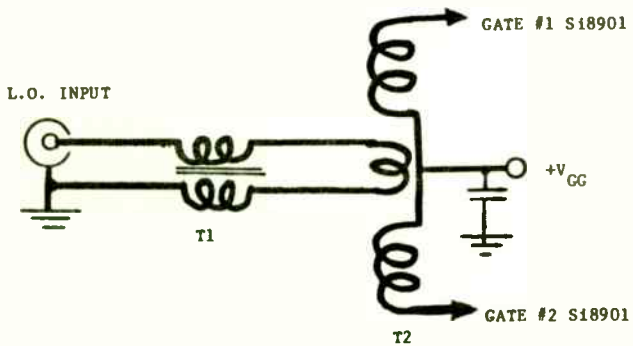
$$A(\beta)M = \sqrt{3} \qquad (13a)$$

The maximum amplitude of the fundamental following relation (13) corresponds to $\sqrt{3}$, for $u = v - 60°$, a three level degnerate waveform shown in Figure 8b.

For decreased fundamental amplitude while satisfying limitation (8) u shall decrease also, while v shall grow. The minimum amplitude obtainable in this way corresponds to 3/2 for $u = 30°$, $v = 90°$. This satisfies in the same time condition (10) and is the maximum which can be obtained according to the relation (12).

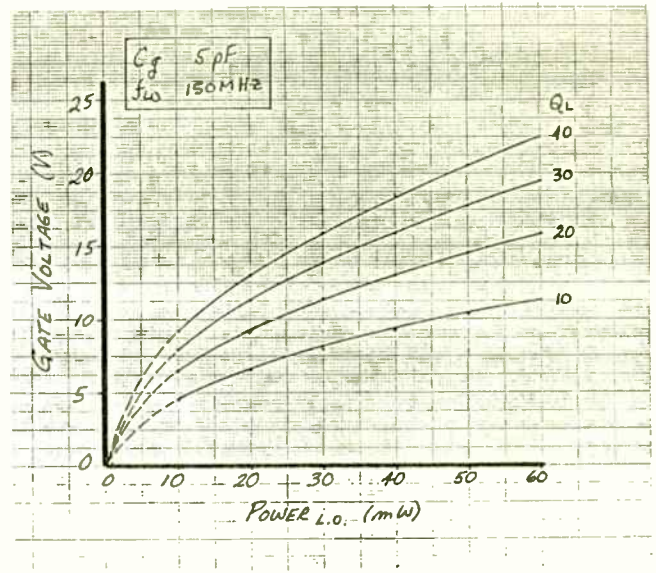


EFFECT OF BIAS AND SUBSTRATE VOLTAGE ON
GATE REACTANCE
FIGURE 11

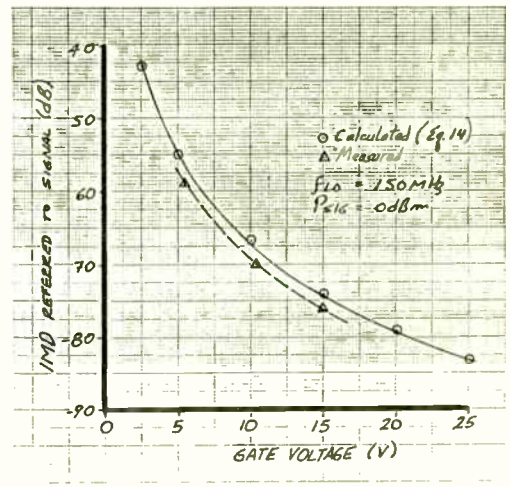


RESONANT-GATE DRIVE TRANSFORMER, T2, IS TUNED
TO RESONATE WITH C_{GG} OF S18901

FIGURE 12



INFLUENCE OF LOADED Q ON GATE
VOLTAGE VERSUS L.O. POWER
FIGURE 13



EFFECTS OF GATE VOLTAGE ON
INTERMODULATION DISTORTION
FIGURE 14

A particular solution of (13), corresponding to u = 42°, v = 78° given A(1) = 1.647 and simultaneously eliminate the third and the fifth harmonic. Such a waveform can be used for high efficiency phase modulated or keyed transmitters. From this level down one has to reduce both u and v under the condition (10) up to u = o, as shown in Figure 8c. In this range one has again elimination of the fifth harmonic for u = 6° and v = 66°.

The amplitude of the fundamental at u = o, v = 60 is half of the value given by (13a).

$$A(1)L = \sqrt{3} \sin \frac{\pi}{6} = \frac{\sqrt{3}}{2} \qquad (14)$$

Below this fundamental level one can generate third harmonic free waveforms by splitting the pulse in the center and moving the two halves toward v = ± π/2 limits. Such a waveform is shown in Figure 8d. One can show that for third harmonic elimination the duration of each resulting pulse should be π/3.

In split pulse mode the amplitude of the fundamental is

$$A(1)S = \sin v - \sin u = 2 \sin \frac{v-u}{2} \cos \frac{v+u}{2} \qquad (15)$$

where u indicates this time the o to 1 transition. For

$$v - u = \pi/3 \text{ and } v = \pi/2$$

one gets the minimum findamental amplitude

$$A(1)m = \cos \pi/3 = 1/2 \qquad (16)$$

Below this level the third harmonic cannot be eliminated, in switching waveforms with only four switching transitions (or maximum two pulses) per half period.

The power range in which the amplitude of the fundamental can be continuously varied and the third harmonic eliminated is given by the ratio:

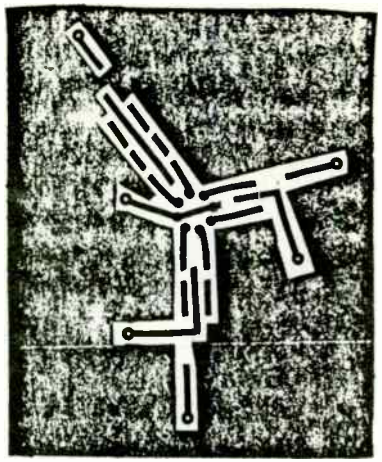
$$P = \frac{A(3)^2}{A(3)m} = 12 \qquad (19)$$

which corresponds to the top 92% of the maximum power output. The complications of adaptive transitions between various modes involved in extending the range have to be traded against high power LC filtering hardware.

IV CONCLUSION

The renewed interest in SSB communications comes at a time when the development of fast switching electronics appears to give the possibility of new approaches in generating and modulating power RF signals. New modulation systems are made possible by circuitry developed for digital techniques. Such applications in the audio domain are now well established.

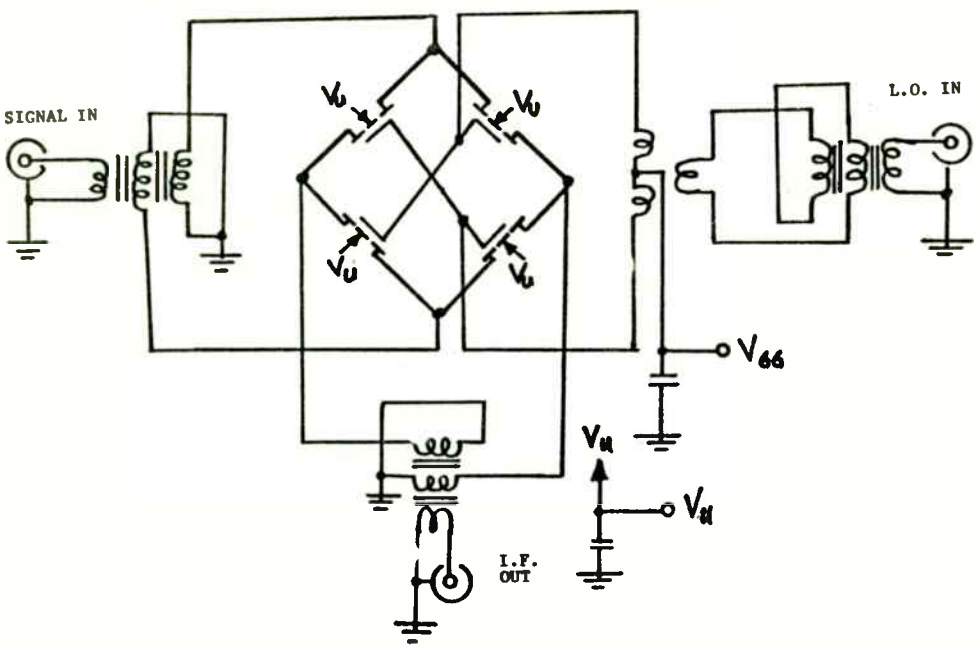
Advances in Fast Digital Signal Processing may result in further reconsideration of traditional modulation methods leading to new levels of quality, efficiency and adaptability. Application Specific Integrated Circuits (ASIC) allowing extremely rapid FFT may contribute to the spread and economic viability of complex modulation techniques in conventional and spread spectrum communications. The present paper gives indirectly some hints on future development possibilities.



MASK LAYOUT -- PRINTED CIRCUIT BOARD

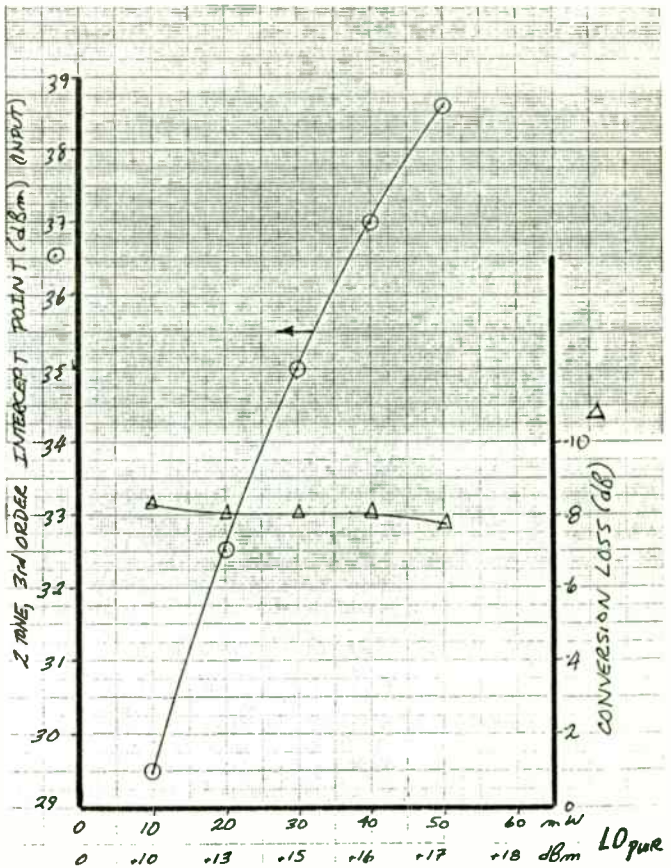
PROTOTYPE BALANCED MIXER

FIGURE 15



SCHEMATIC - COMMUTATION DOUBLE-BALANCED MIXER

FIGURE 16



INPUT INTERCEPT POINT & CONVERSION LOSS

FIGURE 17

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MAXIMIZING CRYSTAL OSCILLATOR FREQUENCY STABILITY

by

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INTRODUCTION

Frequency stability is one of the central topics in the study of crystal oscillators, for the exceptional stability of quartz crystals is their fundamental advantage over other resonators. Both the long term and short term stability of crystal oscillators is important. Long term stability, characterized by terms such as "drift" or "ageing", is the systematic, non-random change in frequency with time, often expressed in terms of frequency change per day or per year. Short term stability is the random, noise-like behavior of the output frequency. In a measurement system based on a frequency counter (time domain), the short term stability is typically measured over gate times from milliseconds to seconds. The same random behavior of the frequency, but measured in a system based on a spectrum analyzer (frequency domain), is often specified in terms of the single-sideband level (relative to the carrier) of the angle modulation noise sidebands, at video frequencies from fractions of a Hertz to tens of Megahertz.

The studies which have been done on this topic fall into two groups: Studies of the crystal by itself, and analysis of crystal oscillator behavior. The former are often concerned with the theory of quartz resonators and with practical considerations concerning surface preparation, electrodes, cleanliness, new designs, etc. The latter include studies and experiments with the various oscillator configurations, such as the Colpitts, Clapp, Pierce, Butler, etc.

In the study of crystal oscillator stability, it is critical to examine the oscillator and circuit together. Particularly when considering short term stability, conclusions based on observations of the crystal alone can lead to erroneous results. In order to examine the crystal-circuit relationship in some detail, this study is confined to one particular oscillator configuration. However, insights obtained from the particular case will allow conclusions which are useful in the general. Exact equations for the crystal are used, and computer numerical methods are used to generate the various reactances and, even more important, the derivatives of these reactances.

For the purpose of analyzing the stabilizing effect of the crystal on the rest of the circuit, assume that the crystal is

Chapter II

PIN Diodes and the Theory of Microwave Operaton

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A. The PIN Diode — An Extension of the PN Junction

1. Structure

The PIN diode should not be thought of as something physically different from the PN junction discussed in Chapter I, but rather different in a sense of degree. In Chapter I we saw that with the abrupt junction the width of the depletion zone is inversely proportional to the resistivity of the P or N region, whichever has the lesser impurity doping concentration. As the width of the depletion zone increases, the capacitance per unit area of the junction decreases. This effect is very beneficial for a diode which is intended for use as a microwave switch because the lower the capacitance the higher the impedance of the diode under reverse bias, and the more effective the device is as an "open circuit."

The limiting case of high resistivity material is undoped (or "intrinsic") *I* silicon. In practice, of course, no silicon material is without some impurities. A practical PIN diode, then, consists of an extremely high resistivity P or N zone between low resistivity (highly doped) P and N zones at its boundaries, as shown in Figure II-1. To distinguish unusually heavily or lightly doped material, special nomenclature has evolved. Heavily doped P and N materials are referred to as P+ and N+, respectively. To identify very lightly doped, high resistivity P and N material, the Greek letters are used; thus high resistivity P material is called *π-type* and high resistivity N material is called *ν-type*. Recognizing that perfectly intrinsic material is not practically obtainable, the I region of a PIN diode can consist of either *ν*- or *π*-type material. The result-

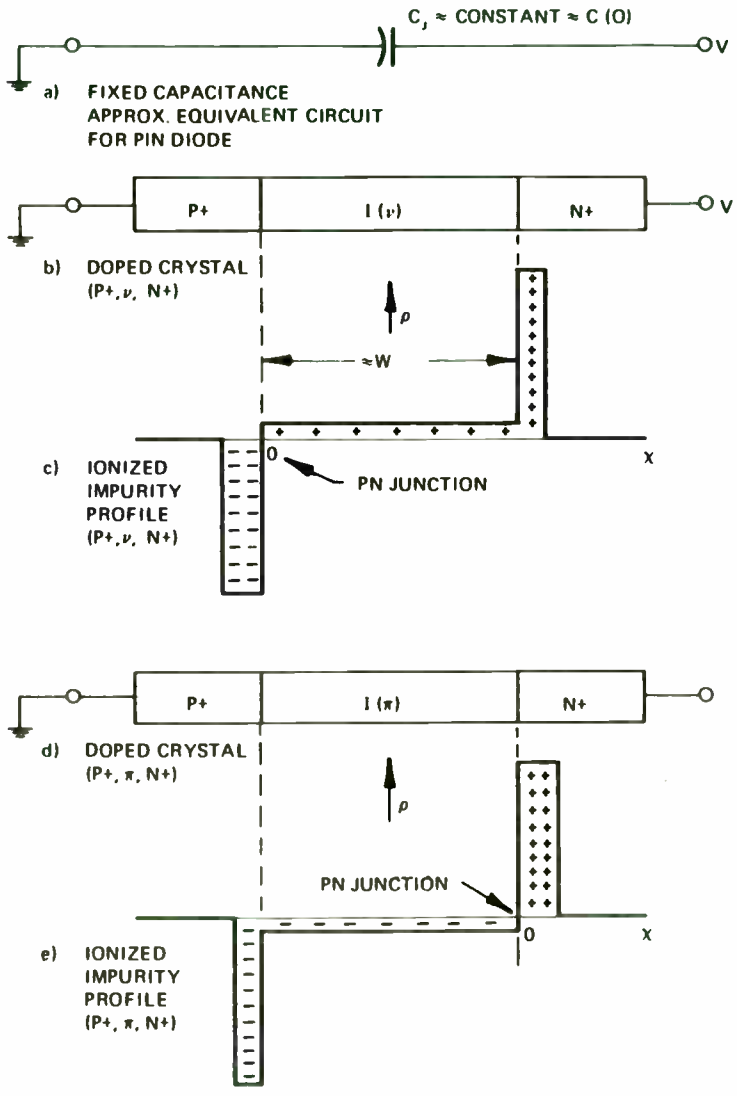


Figure II-1 Profiles for the Two PIN Diode Types

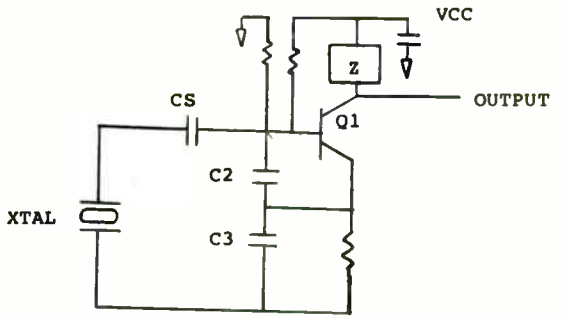
perfectly stable. In fact, certain noisy processes are associated with the crystal itself, and crystal frequency dependence on temperature and time is well known.

THE CIRCUIT

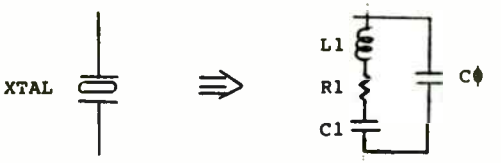
Figure 1a shows the circuit chosen for the analysis of the relationship between crystal , circuit, and frequency stability. The oscillator configuration is the popular Colpitts. Although the Colpitts is a grounded collector type of circuit, a small impedance in the collector provides a convenient signal output point and at frequencies of 10 MHz and lower this impedance has little effect on the oscilletor base-emitter circuit.

THE CRYSTAL

Figure 1b shows the equivalent oirouit of the frequency control crystal. The series circuit of C1, L1 and R1 represent the electrical equivalent circuit of the piezoelectric coupled mechanical resonance of the orystal. The reactances of C1 and L1 are orders of magnitude larger than that which would be obtained from electrical components, and the ratio of these reactances to R1, the loss term, or Q, is typically 50,000 to 1,000,000; again, three or more orders of magnitude larger than what can be obtained from electrical capacitors and inductors. CO represents the parallel plate capacitor formed by the crystal electrodes. Typical values for a 10 MHz fundamental crystal are noted in the figure.



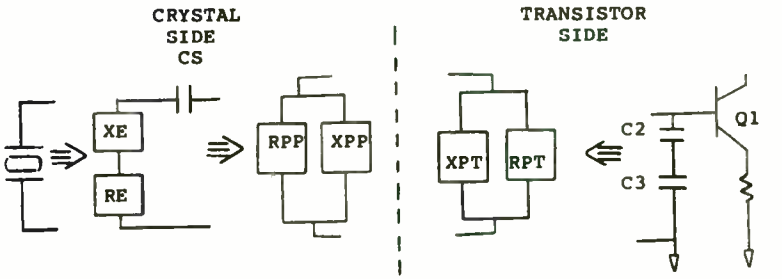
1.a.



1.b.

EXAMPLE

$F1 = \frac{1}{2\pi\sqrt{L1C1}} = 10$ MHZ
C1= .02 PICOFARADS
L1= 12.665 MILLIHENRY
R1= 20 OHMS
C∅= 3.8 PICOFARADS



FOR STABLE OSCILLATION: XPP = -XPT; RPP = -RPT

1.c.

Figure 1a, b, c The Circuit

ing diodes are indistinguishable from a microwave point of view; however, the actual junction forms at opposite ends of the intrinsic zone depending on the choice. This distinction is diagrammed for both cases in Figure II-1.

The first type shown in Figure II-1(b) shows a P+, ν, N+ diode structure. If the I region is of sufficiently high resistivity, what few impurity atoms it has will be ionized and the depletion zone will extend throughout the I region and include a small penetration into both the P and N regions. Because of the heavy doping in the P+ and N+ zones the depletion zone will not extend very far into them, and the depletion zone will be essentially equal to the I layer width, W_I. The alternate diode structure, P+, π, N+ is shown schematically in Figure II-1(d). Here the depletion zone width is likewise approximately equal to the width of the intrinsic layer but the junction is formed at the N+ interface rather than that of P+. Controlling the location of the junction has important consequences from the standpoint of passivating the diode chip, but no impact on performance. Most PIN diodes use ν material for the I region and the junction is formed at the P+ interface.

2. *C(V) Law and Punchthrough Voltage*

In the preceding section it was assumed that the I layer is of such high resistivity that, even with no applied bias, the depletion zone extends across the I layer to the P+ and N+ zones. Under such circumstances C_J is practically independent of applied voltage. At zero voltage the depletion zone has already extended through the I region; as further reverse bias is applied to the diodes, little further widening of the depletion zone proceeds because of very high impurity concentrations and correspondingly large availability of ionizable donors and acceptors in the P+ and N+ regions.

The PIN diode which actually does have so high a resistivity I layer that it is depleted at zero bias is called a *zero punchthrough* diode, because the depletion zone has "punched through" to the high conductivity zones even before bias is applied.

Such a situation, however, represents an idealization. Not all practical diodes are zero punchthrough. A more *general definition of the PIN is a semiconductor diode which consists of two heavily doped P and N regions separated by a substantially higher resistivity P or N region.*

Figure II-2 shows schematically a practical PIN diode with ionized impurity profiles at zero bias and at punchthrough. At zero bias a large portion, but not necessarily all, of the I region impurities have been ionized and the depletion zone, W(0), may be somewhat less than the I layer width, W. As reverse bias voltage is applied to

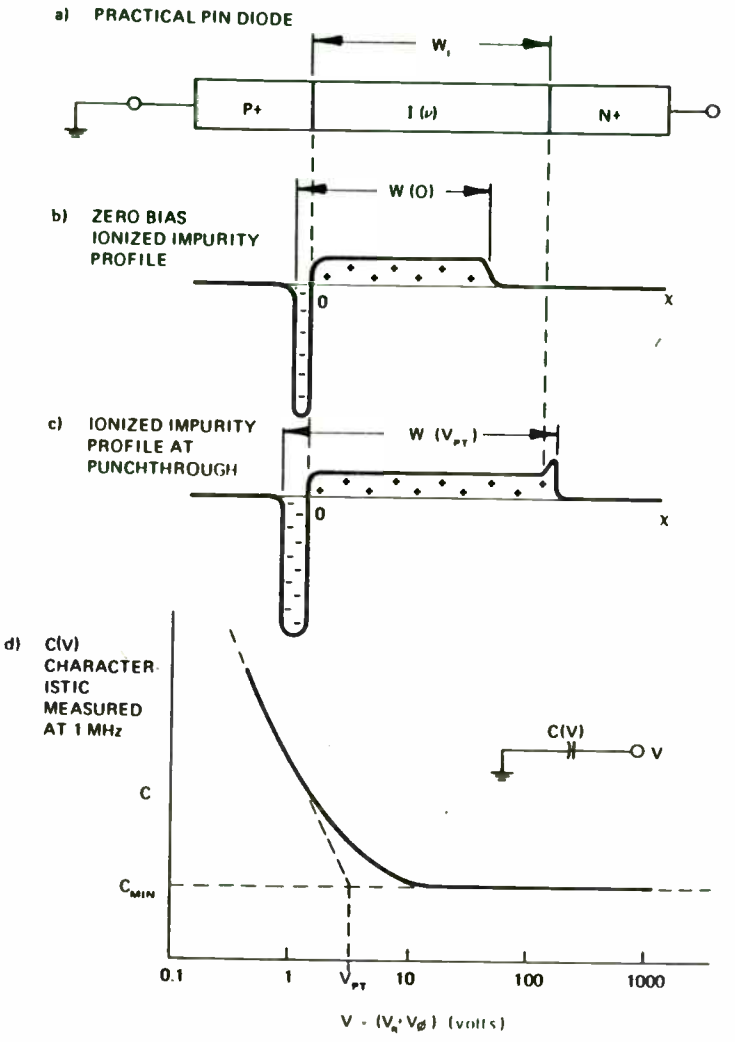


Figure II-2 Practical PIN and Reversed Punchthrough Characteristics

THEORY OF OSCILLATION

The crystal, capacitors C6, C2, and C3, plus the transistor reactances form a parallel resonant network at frequency F. The transistor provides gain, enough to offset the losses in the resonant circuit. It is useful for the present analysis to divide the circuit into the two parts shown in Figure 1c. The crystal, plus capacitor C6 can be analyzed as a net inductive reactance XPP and parallel resistance, RPP. The transistor and C2 plus C3 are analyzed as a single parallel capacitive reactance and a parallel negative resistance, resulting from transistor gain. The circuit oscillates at a frequency where the positive (inductive) reactance of the crystal "side" equals the negative (capacitive) transistor "side". At turn-on, the negative resistance RPT developed by the transistor (connected to the complete tuned circuit) is of a lower value than the positive loss factor RPP. The net resistance is therefore negative, and oscillation begins. The amplitude of the oscillation builds to the point where some amplitude dependent gain factor, such as transistor saturation, lowers the gain and raises the effective negative resistance to exactly equal RPP, the condition necessary for steady state oscillation.

This establishes the conditions for the analysis. The following sections show that over the very narrow frequency range of inductive reactance of the crystal, the capacitive reactance of XPT is essentially constant and therefore oscillation occurs at the "intersection" of the value of XPT and the rapidly changing XPP. The stability of oscillation depends on this relationship.

THE REACTANCE CURVE

Figure 2 shows graphically * the steep rise of the parallel reactance and resistance curves due to the crystal, plotted as a function of frequency. As mentioned above, over the narrow frequency range depicted (.2%), the capacitive reactance of XPT is essentially constant. Therefore, the capacitance associated with the XPT value can be assigned to the right hand vertical scale. If, for example, we choose C2=C3=40 pF, then CT=20 pF, and the frequency of oscillation will be at point B.

The pertinent question is where we would choose to operate for best stability, but two forbidden regions must be discussed first. Practical circuit considertions including parasitic reactances and active device capacitances limit the maximum reactance of operation. In Figure 3, the boundary above which it is impractical to operate is arbitrarilly chosen as 8,000 ohms, or 2 pF.

The exact values are unimportant because this is not the region of optimum stability. The other boundary, which is important, is determined by RPP, the equivalent parallel resistance.

* Equations in Appendix

this diode, depletion layer spreading occurs, and the capacitance, shown in Figure II-2(b), decreases until the depletion layer has spread definitely to the N+ region, as shown in Figure II-2(c). At this voltage the depletion layer width, $W(V_{PT})$, is approximately equal to W_I. Further spreading of the depletion layer into the low resistivity P+ and N+ regions is, for most applications, negligible. The voltage at which the depletion zone just reaches the N+ contact is the punchthrough voltage, V_{PT}.

Because in practice the resistivity levels in the P+, I, and N+ regions do not change abruptly, the resulting capacitance versus voltage characteristics have a *soft knee*. Therefore the punchthrough voltage is not directly measureable with precision. However, the practical diode usually does have two definable slopes in its C(V) characteristic, when plotted using semilog paper as shown in Figure II-2(d). *By convention, the voltage intersection of these two straight line projected slopes is called the punchthrough voltage.*

It is to be emphasized that this C(V) characteristic is what one obtains when the measurements are made at relatively low frequencies, typically 1 MHz. At microwave frequencies, the dielectric susceptibility of silicon is much larger than the conductivity of ν or π material; thus, the capacitance is effectively equal to the minimum capacitance for all values of reverse bias, as is shown in the following discussion of dielectric relaxation.

3. Capacitance Measurements and Dielectric Relaxation

If the capacitance of a PIN diode which does not punch through at zero bias is measured at zero bias, a larger value of capacitance will be measured at a low frequency (such as 1 MHz) than would be measured at microwave frequencies (such as with a slotted line measurement at 1 GHz). The reason is that silicon, in addition to being a variable conductor, also has a high dielectric constant. Therefore, its bulk differential equivalent circuit appears as a parallel combination of conductance and capacitance. The relative current division between these two equivalent circuit parameters varies with the frequency of the applied signal, higher frequency currents being carried mostly by the capacitive path.

To illustrate this point, consider Figure II-3 which shows a PIN diode below punchthrough. The portions of the P+ and the I regions which are depleted represent the depletion zone, or "swept region." The remainder of the I region is "unswept" and can be modelled, as shown in Figure II-3(c), as a parallel resistance-capacitance circuit, represented by the equivalent circuits elements, C_{US} and R_{US}.

The division of current through C_{US} and R_{US} depends upon the ratio of the susceptance of C_{US} to the conductance ($1/R_{US}$). This ratio in turn depends on the dielectric constant of silicon to its bulk resistivity. The frequency at which the current division between these two elements is equal (i.e., when the susceptance is equal to the conductance) is defined as the *dielectric relaxation frequency*, f_R, of the material.

When the operating frequency, f, is equal to or greater than $3\ f_R$, the total capacitance represented by the series combination of C_{SW} and C_{US} is approximately equal to C_J (within 10%), the parallel plate capacitance of the totally depleted I region. This value corresponds to the minimum capacity C_{MIN} measured beyond punchthrough at low frequency.

This point is a major one in the practical characterization of PIN diodes intended for microwave switching applications. It means that practical measurements of the capacitance of a PIN junction can be made at 1 MHz, and the values so attained will represent a good approximation to the actual capacitance applicable at microwave frequencies. This test only requires that sufficient bias voltage is used during the low frequency measurement to insure that the I region is fully depleted. A check to determine whether the I region is in fact fully depleted can be made simply by plotting the C(V) characteristic for a few representative diodes from the production lot to determine at what minimum bias voltage the measured capacitance reaches what is essentially its minimum value.

The remaining required quantity to determine the applicability of the low frequency C_{MIN} as a representation for the microwave capacitance, C_J, is an estimate of the relaxation frequency for the I region of the diodes being measured. High purity silicon material used to make PIN diodes typically has resistivity in the range of 500-10,000 Ω-cm prior to the diffusion and/or epitaxial growth steps used to achieve the low resistivity P+ and N+ regions. However, after the high temperature processing needed to realize these regions, the resistivity of the I region is always less than that of the starting crystal. Typical values for I region resistivity are in the range of 100-1000 Ω-cm. The dielectric relaxation frequency for the unswept portion of the I region can be written in terms of the equivalent circuit parameters, directly from the definition which

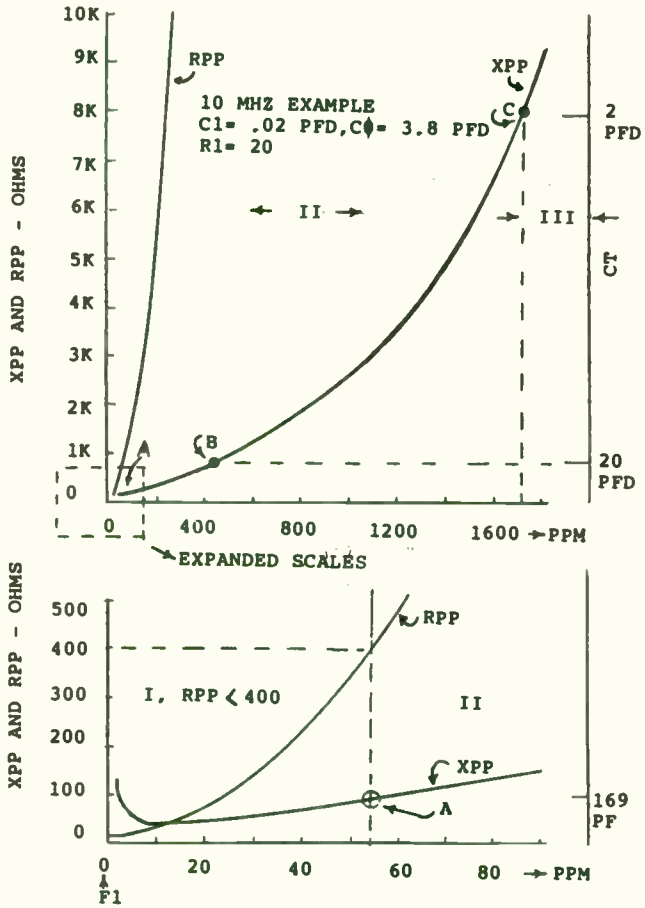


Figure 2, XPP, RPP

As discussed above (Theory of Oscillation), negative resistance is the model chosen to represent the gain relation between the transistor and the circuit. This resistance depends on the transistor characteristics and the values and ratio of C2 and C3. At present, it is important only to note that a minimum value of RPT (maximum gain), exists for any circuit value choice. Clearly, the circuit will not oscillate if RPP on the crystal side is less than RPT generated on the transistor side, so a boundary exists.

In the example, 400 ohms has been chosen as the boundary*, so the circuit must operate somewhere between point A and point C. Where shall the greatest stability be obtained? If the crystal side only is considered, one might be tempted to choose point C, since the derivative of XPP with respect to frequency is highest at this point. To resolve the question, one must examine the transistor side in greater detail and determine the form of the unstable reactance.

THE TRANSISTOR SIDE

Recall from Figure 1 that the transistor side is defined as containing the capacitors C2 and C3 and the transistor itself. The admittance of this side will have real and imaginary parts as shown in that figure. The real part will be a negative

* Since RPT depends on C2, C3 and C2/C3, the boundary between I and II is actually a curved line.

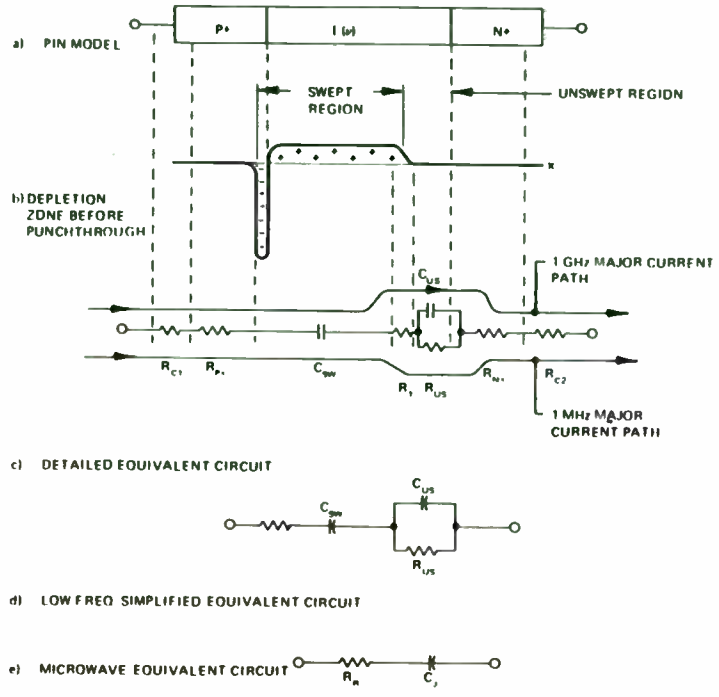


Figure II-3 **Reverse Bias PIN Equivalent Circuit**

requires that the conductance and capacitive susceptance be equal at f_R. The result is

$$f_R = \frac{1}{2\pi R_{US} C_{US}} \qquad \text{(II-1)}$$

In turn, the specific values for R_{US} and C_{US} can be written in terms of the length, L, and the area, A, of this unswept region together with the bulk resistivity, ρ, and the absolute dielectric constant, $\epsilon_0 \epsilon_R$, as follows

$$R_{US} = \frac{\rho L}{A} \qquad \text{(II-2)}$$

$$C_{US} = \frac{\epsilon_0 \epsilon_R A}{L} \qquad \text{(II-3)}$$

Substituting these expressions into Equation (II-1) together with the value $\epsilon_R = 11.8$ for silicon yields Equation (II-4), which gives the dielectric relaxation frequency directly in GHz when the resistivity, ρ, is known.

$$f_R = \frac{1}{2\pi \epsilon_0 \epsilon_R \rho}$$

$$f_R = \frac{153}{\rho(\text{ohm-centimeters})} \quad \text{(gigahertz)} \qquad \text{(II-4)}$$

This expression is shown graphically in Figure II-4.

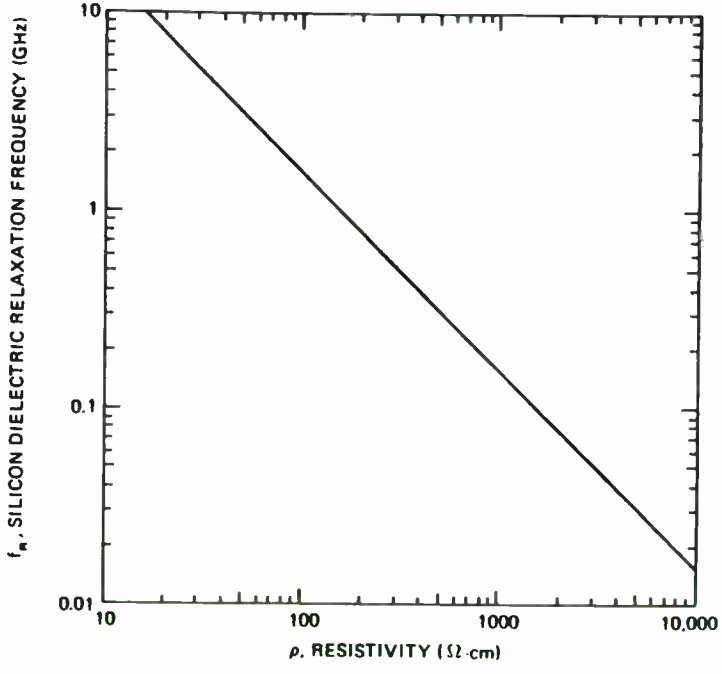


Figure II-4 **Dielectric Relaxation Frequency in Silicon of Various Resistivities**

conductance of value 1/RPT and the imaginary a positive susceptance B=1/XCT parallel (the defining equations are shown in the Appendix.)

It is beyond the scope of this paper to quantitatively model and analyze the various long and short term instabilities on this side of the circuit. Rather, some systematic and random processess will be postulated, and the form of the circuit reactance instabilities will be shown. Armed with these models we can join the left and right sides of the circuit to describe the parameter that determines frequency stability.

CASE I

The first model assumes that C parallel has a tolerance on its average value which varies this value with time, temperature, or other systematic function. In this case

$$C = CT * (1 + e) \quad (1.6.1)$$

Where e represents the delta change from nominal (temperature, tolerance, etc.). The incremental reactance change, DX, due to e is then:

$$DX = 1/(2\pi FCT) - 1/(2\pi FCT(1+e)) \quad (1.6.2)$$

$$DX = (1-(1-e))/(2\pi FCT) \quad (1.6.3)$$

$$DX = e/(2\pi FCT) = XT * e \quad (1.6.4)$$

CASE 2

Assume that the parallel capacitor CT has a fixed, stable part in parallel with a small variable capacitor CV which represents all of the instability or noisy portion of the circuit.

$$DX = XT - XT^* XCV/(XT+XCV) \quad (1.6.5)$$

$$DX = (XT)^2/(XT+XCV) \quad (1.6.6)$$

For XCV >> XN:

$$DX = (XT^2/XCV) = (XT)^2 *(2\pi FCV \quad (1.6.7)$$

CASE 3

Assume that the current generator gm * Ib has a quadrature noise component $\overline{in} \angle 90^\circ$

The noise current into the base is derived in appendix B as:

$$\overline{i1n} = \overline{in}/(1+X2/X3+gm*X2) \quad (1.6.8)$$

Assuming gm * X2 >> (1 + X2/X3):

$$\text{then } |\overline{i1n}| \doteq \overline{in}/(gm * X2) \quad (1.6.9)$$

The "noisy reactance", XN, which would cause this current to flow is:

$$XN = gm * X2 * es / \overline{in} \quad (1.6.10)$$

Where es is the oscillator voltage at the base. Then

$$DX = XT - XT*XN / (XT+XN) \quad (1.6.11)$$

$$= (XT)^2 / (XT+XN) \quad (1.6.12)$$

for XN >> XT

$$DX = (XT)^2 * \overline{in} / (es * gm * X2) \quad (1.6.13)$$

for X2 = K * XT (1.6.14)

(1.6.13)

$$DX = XT * \overline{in} / (K * es * gm) \quad (1.6.15)$$

Strictly speaking, since the final resistivity of the I layer of a practical diode depends upon the actual processing steps used to fabricate the diode, one could not know beforehand what dielectric relaxation frequency would apply for a particular diode unless a method for determining the magnitude of ρ as realized in a final device were available. Usually a PIN diode has an I layer resistivity of at least 100 Ω-cm, which corresponds to f_R = 1.53 GHz. Thus for operating frequencies of 5 GHz or more the simplified equivalent circuit in Figure II-3(e) can nearly always be applied.

An experimental method does exist for the determination of I layer resistivity through the measurement of the punchthrough voltage and knowledge of the I layer width, which usually is known with reasonable accuracy by the diode manufacturer. To make the calculation, Equation I-10 is solved for V_{PT} at which the depletion layer is equal to the I region width, W. Recognizing that for a PIN the impurity concentration of the N+ contact, N_A, is much larger than the impurity concentration in the I region, N_D, the result becomes

$$V_{PT} = \frac{eN_D W^2}{2\epsilon_0 \epsilon_R} \qquad \text{(II-5)}$$

But the resistivity of the I region is related to the donor impurity density according to

$$\rho = \frac{1}{N_D e \mu_N} \qquad \text{(II-6)}$$

where μ_N is the *electron mobility* (i.e., the effective drift velocity of electrons in the I region per unit applied electric field) and e is the charge of a single electron. Substituting this result in Equation (II-5) gives

$$\rho = \frac{W^2}{2V_{PT}\epsilon_0 \epsilon_R \mu_N} \qquad \text{(II-7)}$$

$$\rho = \frac{(2.4 \times 10^8) W^2}{V_{PT}} \text{(ohm-centimeters)}$$

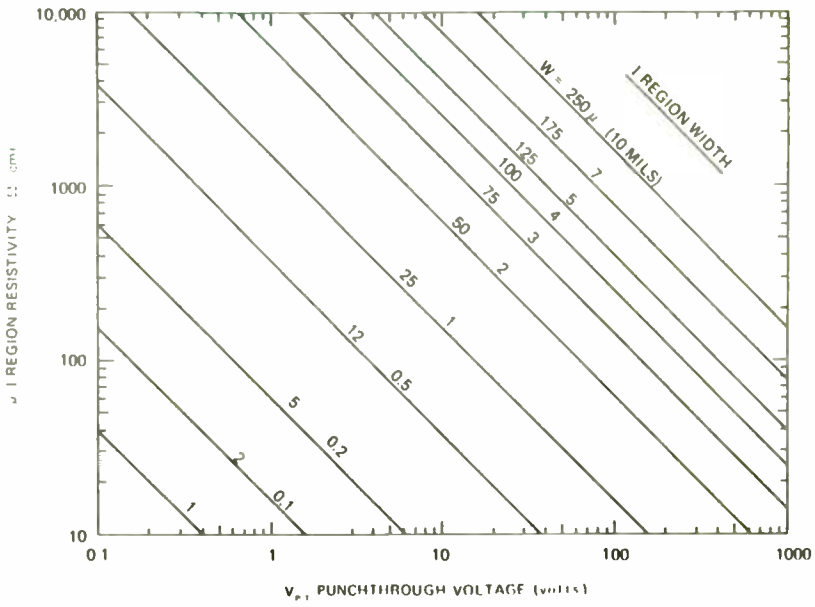


Figure II-5 Punchthrough Voltage vs. I Region Resistivity for Various I Region Widths

where ϵ_R = 11.8 (silicon)

μ_N = 2000 (centimeters²/volt-second)*

W = I region width (centimeters)

V_{PT} = punchthrough voltage (volts)

Thus, for example, if a particular diode having an I region width of 0.0025 cm (1 mil) is found to have a punchthrough voltage of 10 V, the resultant average resistivity is 150 Ω-cm. Equation (II-7) is shown graphically in Figure II-5 for various values of I region width, W.

B. Microwave Equivalent Circuit

1. Charge Control Model

Transit Time Limit of the I-V Law

In Chapter I the I-V characteristic for a PN junction was given (Equation (I-1)). The same characteristic applies for the PIN *at*

*This mobility value is representative for electrons in high resistivity N type silicon, as shown in Figure II-8. Thus, this method of I region width determination is limited by the accuracy with which mobility can be estimated.

Summarizing the three cases :

(1) $DX = (XT) * e$ (1.6.16)

(2) $DX = (XT)^2 * (2\pi F) * CV$ (1.6.17)

(3) $DX = (XT) * \overline{in} / es * gm * K$ (1.6.18)

Now we turn back to the complete circuit to find the form of delta frequency, DF.

DELTA FREQUENCY

The reactance curve of Eq. A6 plotted in figure 2 has a slope of DX/DF ohms per PPM. If one assumes an "operating" point of XT, then the frequency instability at that point will be:

$DF = [1/DX/DF] * DX$ (1.7.1)

Going back to the three cases developed in section 1.6, and substituting XPP=XPT=XT (condition of resonance),

$DF = [1/((DX/DF) * (1/XPP))] * e$ (1.7.2)

$DF = [1/((DX/DF) * (1/(XPP)^2))] * (2\pi F) * CV$ (1.7.3)

$DF = [1/((DX/DF) * (1/XPP))] * \overline{in}/(gm*es*K)$ (1.7.4)

These are the functions which yield the value of DF, the frequency instability of the total circuit, for the three cases of the preceding section. The quantities to the right of the brackets are constants determined by the degree of instability on the transistor side. The two functions in the brackets (one and three are the same) are determined by the crystal, the capacitor CS, and the value of the XT, the parallel reactance. In order to minimize delta frequency, we wish to maximize the inverse of these, which are,

I $(DX/DF)*1/XPP$ (1.7.5)

II $(DX/DF)*1/(XPP)^2$ (1.7.6)

These functions will be called the fractional reactance slope, Type I and Type II, to emphasize the fact tht it is the fractional slope which determines stability, not the absolute slope. In Figure 3, the fractional reactance slope functions and the reactance slopes have been plotted for a number of example cases, including the 10 MHz crystal of Figure 2, 5 MHz third overtone, and a 60 MHz third overtone. The functions are maximum at the lower boundary. The intuitively attractive steep slope at point "C" in Figure 2 is now shown to be deceptive because of the role of fractional slope in stability.

The effect of R1 and Q now becomes clear. The fractional reactance slope depends on XC1 of the crystal, so for all other factors equal, one always wants to maximize that. But best stability is found at the lowest reactance, and that occurs at a value determined by RPP which depends on R1, the crystal series

low frequencies, for which the RF period is long compared with the *transit time* of an electron or hole across the I region.

The discussion to follow using a simple carrier transit time model is only approximate. Real diodes have more complex carrier flow, which is non uniform, subject to applied voltages (i.e., nonlinear), and so forth. The approximation is useful, as it permits estimates of frequency behavior and switching speed. The transition between low and high frequency behavior occurs when this transit time is equal to the RF period. To estimate the transit time, recall that the injection of carriers into the depletion zone occurs under forward bias by diffusion. That is, once forward bias is applied it reduces the magnitude of the built-in junction potential, causing holes to diffuse from the P to the N region and electrons to diffuse in the opposite direction.

The mechanics of this diffusion charge transport are described by *diffusion constants* for holes and electrons, D_P and D_N respectively. Diffusion, being the flow of carriers from a region of high to lower density, is described in terms of a current density proportional to the spatial gradient of charge density according to Equations (II-8) and (II-9).

$$\text{(For holes)} \quad \vec{J}_P = -eD_P(\nabla p) \qquad \text{(II-8)}$$

$$\text{(For electrons)} \quad \vec{J}_N = -eD_N(\nabla n) \qquad \text{(II-9)}$$

where

J = current density

e = unit charge *magnitude* = $(+1.6 \times 10^{-19}$ coulomb$)$

$D_{P,N}$ = diffusion constants for holes and electrons respectively

∇p = spatial gradient of hole density

∇n = spatial gradient of electron density

To illustrate diffusion, let us estimate the approximate *transit time* for holes, the slower moving carrier, across the depletion zone of a PN junction of width W. A one dimensional analysis is used, and Equation (II-8) becomes

$$J_P = -eD_P \frac{dp}{dx} \qquad \text{(II-10)}$$

The minus sign is required (D is defined as a positive constant) since current flow is opposite to the direction of increasing charge density. Figure II-6 shows a simplified model of the PIN and majority carrier profiles. The gradient dp/dx is abrupt at the P/I interface and an exact analysis would require an analytic representation of p(x). However, as an approximation, we use the *average gradient of the hole density across the I region*, or

$$\frac{dp}{dx} \approx \frac{P_P}{W}$$

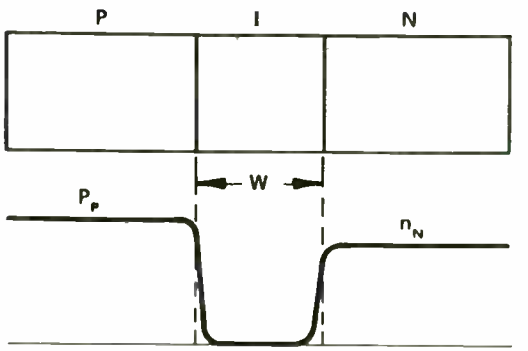


Figure II-6 **Depletion Zone Model Used to Estimate Transit Time Frequency**

Equation (II-10) then becomes

$$J_P = P_P e v_P \approx -eD_P \frac{P_P}{W}$$

where J_P has been written explicitly using carrier velocity, v_P, and the density of carriers participating in the hole current flow. But the hole transit time, T_P equals W/v_P; therefore

$$\text{Transit Time} = T_P \approx \frac{W^2}{D_P} \qquad \text{(II-11)}$$

Several things have happened. At XPP equal 94 ohms, point C, RPP now equals 277 ohms, so this point violates the lower boundry of 400 ohms. Adjusting XCT to 112 ohms (changing CT), point D, gives RPP equal 402 ohms. DX/DF is now 2.14 so the fractional reactance slope (I) is 1.91E-2. The stability has been improved by about 14 percent for type I instabilities,compared to point A. But the type II fractional reactance slope is decreased by about 5 percent. So the answer for this particular example depends on the exact nature of the circuit instabilities. Note that this example assumes a perfect capacitor for CS. If CS were a varactor diode it is apparent that as the value decreases it is possible to move to a point where RPP is too low for oscillation. In VCXO designs then, the margin for oscillation should be adjusted at minimum capacity.

CONCLUSION

For several models of transistor and circuit instabilities it is seen that frequency stability is maximized when the fractional reactance slopes, Type I and Type II, are maximum. For a number of crystal examples these functions are maximum at the lowest parallel reactance. The minimum reactance point depends on the value of RPT, the parallel negative resistance. The effect of a capacitor in series with the crystal on stability depends on the exact nature of the circuit instabilities.

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Accordingly, we can expect that the low frequency I-V characteristic (Equation (I-1)) can no longer be used at frequencies for which the RF period is comparable to T_P. If a transition frequency, f_T, is defined for the PIN diode at which

$$f_T = \frac{1}{T_P}$$

then

$$f_T = \frac{D_P}{W^2}$$

Frequently, the mobility, μ, rather than the diffusion constant, D, is evaluated for semiconductor materials. These two constants are related according to the Einstein relationship

$$D = \mu \frac{kT}{e} \quad \text{(centimeters}^2\text{/second)} \qquad \text{(II-12)}$$

where D = diffusion constant (centimeters^2/second)

μ = mobility (average carrier drift velocity per unit applied electric field)

k = Boltzmann's Constant

T = absolute temperature (Kelvin)

At 300 K (near room temperature) kT/e = .026 V; thus

$$D = .026\,\mu \text{ (at 300 K)} \qquad \text{(II-13)}$$

The hole and electron mobilities vary both with impurity densities (see Figure II-7) and temperature (see Figure II-8). For the present example the hole mobility at 300 K in high resistivity silicon is about 500 cm^2/V-s and therefore

$$f_T = \frac{1300}{w^2} \text{ megahertz} \qquad \text{(II-14)}$$

where w is I region thickness in microns.

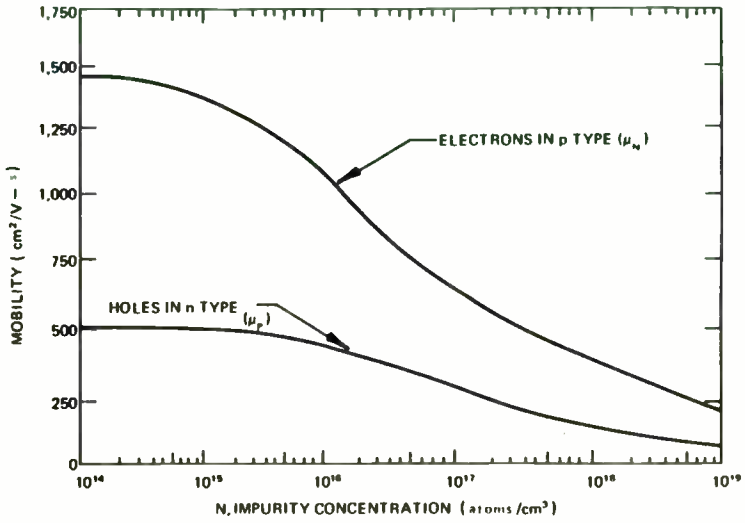


Figure II-7 **Hole and Electron Mobilities (at 300 K in silicon) vs. Impurity Density (After A.B. Phillips [1])**

Thus, even for a very thin base PIN diode having only a 2.5μ (0.1 mil) I region, f_T = 200 MHz. A graph showing how f_T varies with w is shown in Figure II-9. In practice, PIN diodes used for microwave switching have I region widths of 25-250 μm (1-10 mils) *and accordingly the low frequency I-V characteristic given in Equation (I-1) is useless for evaluating microwave resistance.*

I Region Charge and Carrier Lifetime

However, all of the concepts introduced so far to describe low frequency behavior are easily applied to determine the microwave resistance. We shall evaluate I region charge and use it to gauge resistance. From Figure II-9 it is evident that once charge, consisting of holes and electrons, has been injected into the I region under forward bias, *it cannot be removed in the brief duration of a half cycle of RF frequency* if that RF frequency is above a few hundred megahertz, even for the thinnest I region (or base width) diodes.

The *charge control model* for the PIN diode allows RF performance to be related to the net steady state hole and electron

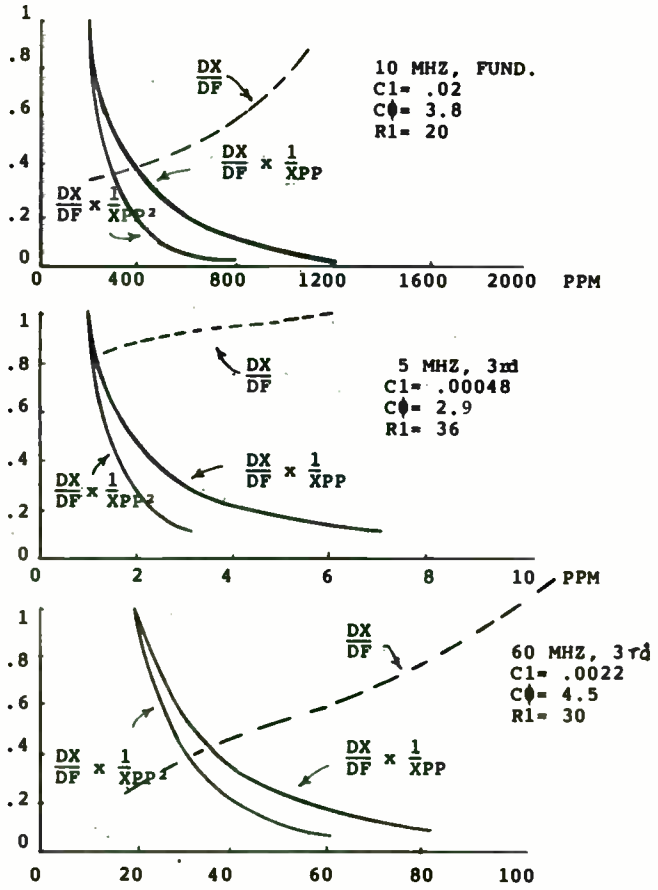


Figure 3, Relative Slopes

resistance. The crystal resistance determines stability indirectly by restricting the "operating" point of the circuit.

SERIES CAPACITANCE

Can one improve frequency stability by putting a capacitor in series with the crystal? The intuitive answer to this recurring question goes as follows (refer to Figure 2). The slope, DX/DF, increases with frequency but the fractional reactance slope decreases with frequency. At points A and B then,

Table 1.8.1

	PPM	RPP	XPP	DX/DF	TYPE I DX/(DF*XPP)	TYPE II DX/(DF*XPP^2)
A	55	4D2	94	1.58	1.68E-2	1.79E-4
B	44D	25K	841	2.29	2.7E-3	3.2E-6

so better stability is obtained at A. If one adds a capacitor of reactance -747 ohms in series with the crystal, the entire curve is shifted in the negative direction. Is not now the reactance at F = 44D PPM equal to 841 minus 747 or 94? And since the curve is simply shifted, have we not now the DX/DF of point B but at the reactance of point A? Table 1.8.2 shows the results of adding a 21.3 pFd capacitor.

TABLE 1.8.2

	PPM	RPP	XPP	DX/DF	TYPE I DX/(DF*XPP)	TYPE II DX/(DF*XPP)
C	436	277	94	2.D4	2.17E-2	2.31E-4
D	444.4	4D2	112	2.14	1.91E-2	1.71E-4

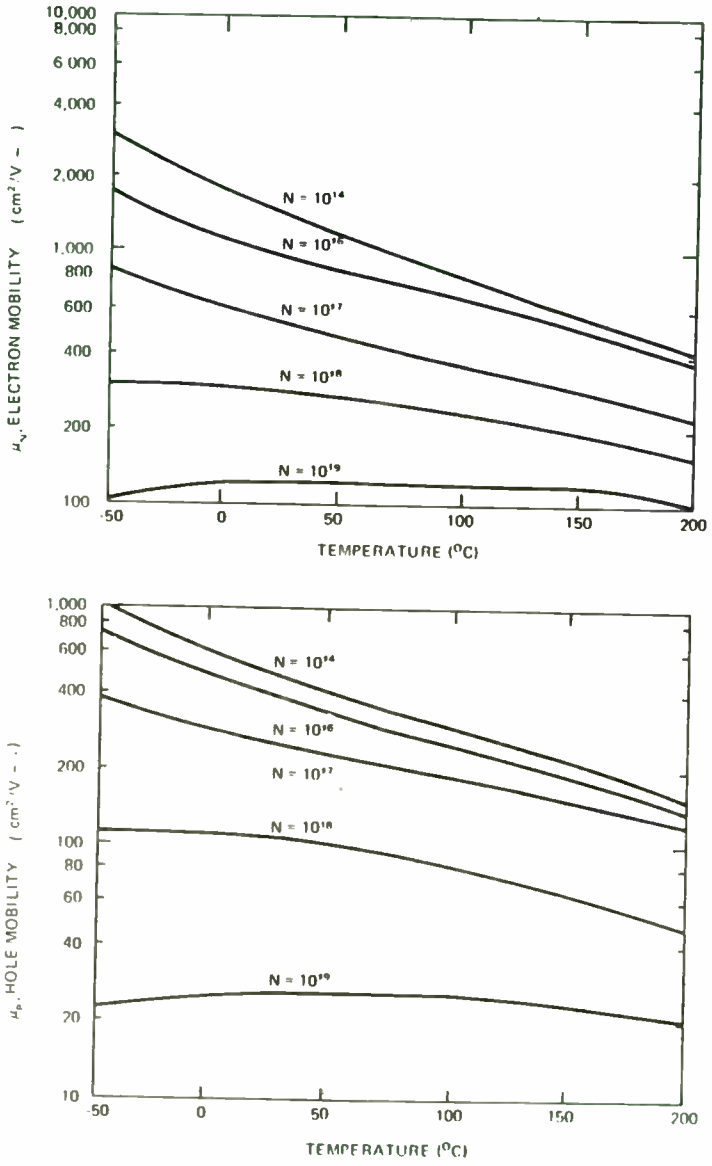


Figure II-8 Hole and Electron Mobilities vs. Temperature for Various Impurity Densities in Section (After A.B. Phillips [1])

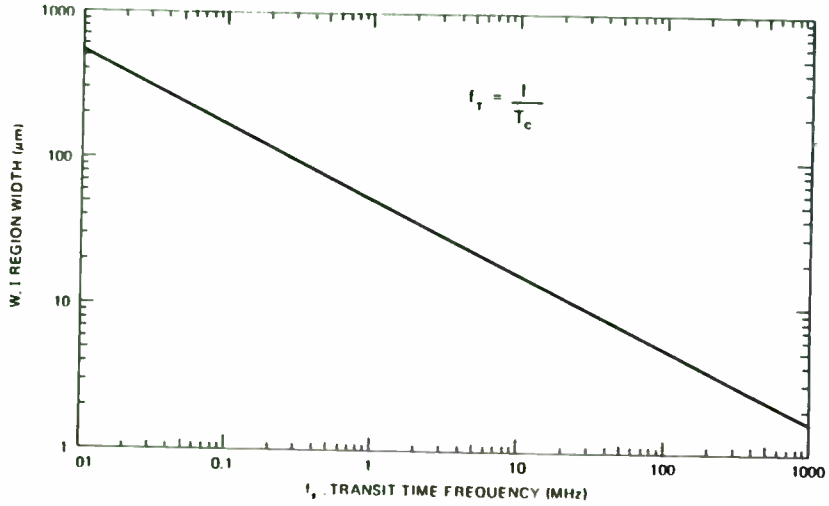


Figure II-9 I Region Width vs. Transit Time Frequency for Silicon PIN Diodes at Room Temperature

charges, Q_P and Q_N respectively, in the I region. These charges are equal to the product of the (low frequency) bias current and the respective average carrier lifetime, thus

$$Q_P = I_0 \cdot \tau_P \qquad \text{(II-15)}$$

$$Q_N = I_0 \cdot \tau_N \qquad \text{(II-16)}$$

That is, after the turn on transient during which the I region charge density is established, the bias current serves as a replenishment source for holes and electrons which have recombined. Referring to Figure II-10, the bias current at the P/I interface consists almost entirely of holes being injected into the I region. At the I/N interface the same bias current consists mainly of electron injection into the I region.

The longer the lifetime, the less bias current required to maintain a given charge density and, accordingly, a given microwave conductivity. Before proceeding further it is important to note that *long lifetime does not necessarily imply slow switching speed.* A properly designed driver can remove I region charge, and thereby reverse bias the diode, in a period shorter than the lifetime. Rather, long lifetime should be considered a measure of the crystalline perfection within the diode.

APPENDIX A, EQUATIONS

CRYSTAL

$$X1 = XL1 + XC1 \quad ; \quad F1 = 1/2\pi\sqrt{(L1 + C1)^{.6}} \tag{A1}$$

$$= j2\pi F / ((2\pi F1)^2 * C1) - j/(2\pi F * C1) \tag{A2}$$

$$XO = -j / 2\pi F * CO \tag{A3}$$

CRYSTAL SERIES EQUIVALENT

$$XE = XO*((R1^2 + X1*(XO + X1))/(R1^2 + (XO + X1)^2) \tag{A4}$$

$$RE = R1/((R1/XO)^2 + ((XO + X1)/XO)^2) \tag{A5}$$

PARALLEL: XPP and RPP from RE and XE + XCS

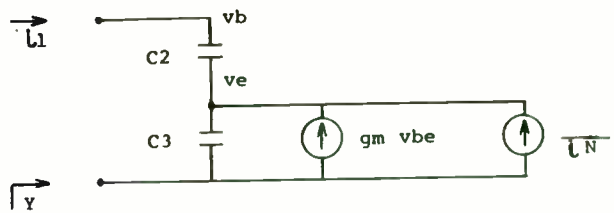
$$XPP = (RE^2 + (XE + XCS)^2)/(XE + XCS) \tag{A6}$$

$$RPP = (RE^2 + (XE + XCS)^2)/RE \tag{A7}$$

DERIVATIVES: COMPUTER CALCULATED INCREMENT

$$DXPP = XPP @ F - XPP @ (F\text{-freq. increment}) \tag{A8}$$

APPENDIX B, TRANSISTOR MODEL



$$i1 = vb*1/(1 + x2/x3 + gm*x2) + \overline{in}/(1 + x2/x3 + gm*x3) \tag{B1}$$

$$Y = i1/vb = 1/RPT + 1/XCT \tag{B2}$$

$$RPT = gm*x2*x3 + (x2 + x3)^2/gm*x2*x3 \tag{B3}$$

$$XCT = ((x2 + x3)^2) - (gm*x2*x3)^2))/(x2 + x3) \tag{B4}$$

$$\dot{XCT} = x2 + x3 \tag{B5}$$

$$\overline{i1n} = \overline{in}/(1 + x2/x3 + gm*x2) \tag{B6}$$

$$\dot{\overline{i1n}} = \dot{\overline{in}}/gm*x2 \tag{B7}$$

$$XN = es/in = gm*x2*es \tag{B8}$$

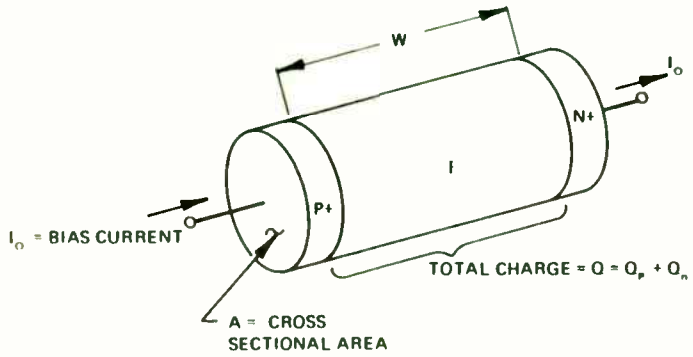


Figure II-10 Cylindrical I Region Model Used to Estimate I Region Resistance of PIN Diode

A pure intrinsic silicon crystal has a calculated carrier lifetime of 3.7 *seconds*. With impurity doping of 10^{15} cm^{-3} this figure drops to 0.11 ms. [1 (p. 80)] In actual diodes the lifetime typically ranges from 0.1 to 10 μs, orders of magnitude less than these theoretically attainable values. To appreciate the reason for this great disparity, it is necessary to review what lifetime represents.

Lifetime is proportional to the *improbability* that an electron and hole will recombine. Imperfections in the regular array of crystal atoms create energy states within the otherwise *disallowed* band gap of silicon. Such intermediate states provide a virtual energy "staircase" by which the recombination proceeds. In a very regular crystalline structure, energy must be given off in the transition of an electron from conduction to valence bands in the form of a 1.1 eV (light emitting) photon; the statistical probability of such an occurrence is low. But with crystalline irregularities, intermediate allowed energy states between these two bands permit a transition in a "staircase" of smaller energy transitions with corresponding low energy phonon (lattice vibrations) emissions, the overall probability of which is higher. Thus lifetime is reduced and recombination is enhanced by the presence of crystalline imperfections and/or impurities.

There are two categories of crystalline irregularities – boundary surfaces and bulk impurities. For a PIN diode the I region boundaries consisting of the highly doped P+ and N+ represent rapid recombination surfaces for carriers which diffuse into them. Likewise the peripheral surface boundary of the I region, although not to the same extent as the P+ and N+ regions, provides greater recombination probability than would be present for carriers were the silicon crystal of infinitely extended dimensions. Furthermore, from a bulk point of view, even the structure of an undoped silicon crystal is never ideal. There are stress lines and faults where the probability of electron-hole recombination increases. A doped crystal is all the more susceptible to such imperfections because of the temperature shocks, imperfect atomic fit of doping atoms within the silicon, and related crystal stress producing factors associated with diode manufacture.

This brief discussion of lifetime and its determining factors is qualitative. Even an approximate theoretical treatment of the effective lifetime for a real diode is impractical, although some bulk quantitive analytical treatments of semiconductor crystal lifetime have been made. [3] For the diode maker and user, resort must be made to experimental means by which *average* carrier lifetime can be measured. The conventional method for measuring PIN diode lifetime, τ, consists of injecting a known amount of charge, Q_0, into the I region and measuring the time, τ_S, required to extract it using a "constant" reverse bias current. [4,5] To appreciate this method, consider the equivalent circuit and charge versus time profiles shown in Figure II-11.

A forward bias current, I_F, is established and permitted to flow for a period long compared to the expected lifetime, thus storing a charge, Q_0 equal to $I_F \cdot \tau$ in the diode under test. The current supplies are chosen so that $R_R \ll R_F$. Thus, when the switch, S, closes, the diode current, I_D, reverses direction and reaches a magnitude, I_R-I_F. The stored charge is removed by this current until it is fully depleted. If the discharge period, τ_S, is short compared to the lifetime ($\tau_S \ll \tau$), then negligible recombination occurs during the turnoff and the total stored charge is recovered. In this case, $Q_0 = I_F \cdot \tau = (I_R - I_F)\tau_S$ and the lifetime is found from

$$\tau \approx \tau_S \left(\frac{I_R}{I_F} - 1\right) \quad \text{where } \tau_S \ll \tau \qquad \text{(II-17)}$$

This same expression gives the approximate switching time, τ_S, of a driver which switches from forward bias, I_F, to reverse bias and has a reverse bias transient current switching capability of $I_R - I_F$

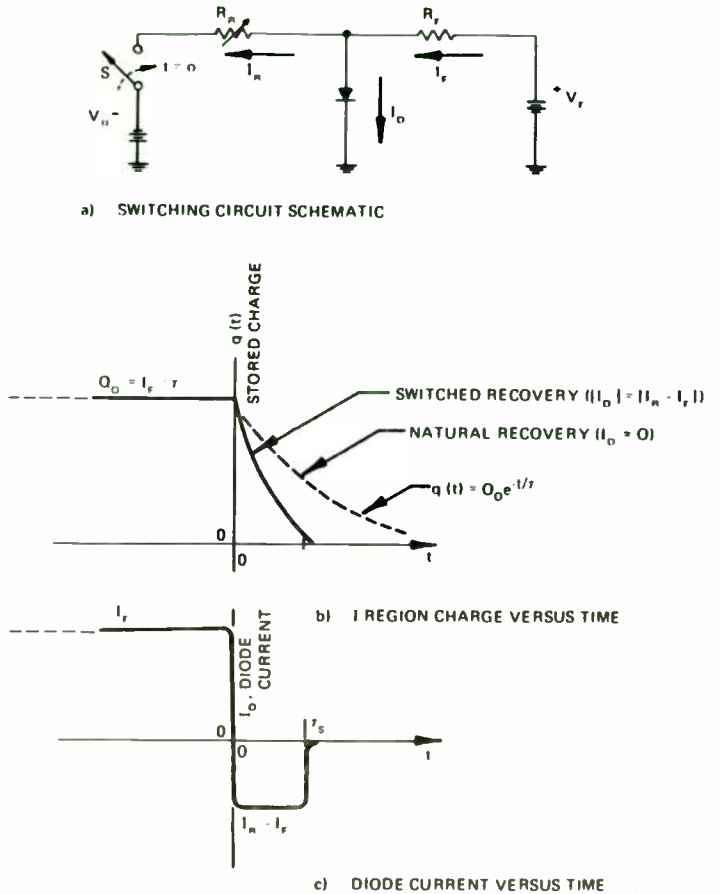


Figure II-11 Lifetime Measuring Method

amperes. Of course, in a practical driver circuit the forward current supply, I_F, would be switched off during reverse bias.

Practically, however, Equation (II-17) is not always directly useable because it may be difficult to switch the diode off in a time short compared with the lifetime. Typical PIN diode lifetimes may range from 0.1-10 μs, requiring extremely fast switches to satisfy the requirements that τ_S be small, say one-tenth, of the expected value of τ. To overcome this problem, a test setup is

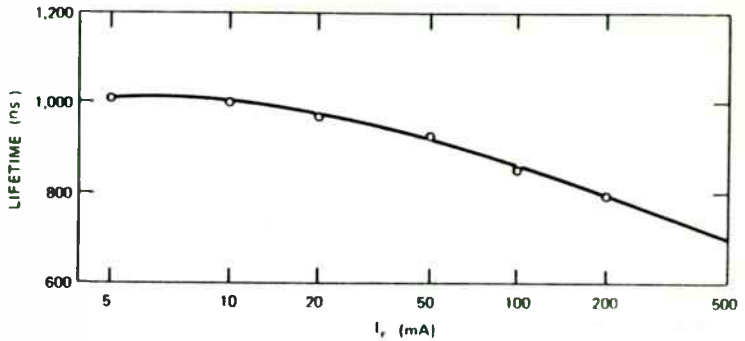


Figure II-12 Typical Variation of PIN Lifetime with Forward Current (After Ciccolella, Johnston, and DeLoach [6 (p. 289)])

made whereby the switching time can be adjusted. In the circuit of Figure II-11, R_R is made variable. The ratio I_R/I_F is adjusted so that $\tau_S = \tau$; the applicable condition is determined by analysis as follows.

If, at t = 0, I_F were turned off, the initial charge, Q_0 would decay at a rate proportional to the product of the instantaneous charge magnitude in the I region and the recombinate rate, $1/\tau$. Actually lifetime is somewhat dependent on the bias current level; a typical variation of PIN lifetime is shown in Figure II-12 [6] for a range of bias currents commonly used. Conventionally this variation of lifetime is ignored, not because it is insignificant, but because its inclusion would not permit the simple analysis which follows. Which is not to say that the analysis isn't useful. Common practice is to apply it, but one should be aware of its limitations.

With the constant lifetime assumption, suppose that the "driver" described in Figure II-11 provides no charge extraction current. Then for $t > 0$, the expression describing the instantaneous rate of charge (dq/dt) of charge in the I region, q, is

$$\frac{dq}{dt} = -\frac{q}{\tau} \quad (t > 0) \tag{II-18}$$

The solution of this differential equation is

DIELECTRIC RESONATOR FILTERS FOR UHF AND MICROWAVE APPLICATIONS

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ABSTRACT

Simplified design methods for dielectric resonator bandpass and bandstop microwave filters are discussed. Two typical cases of dielectric resonator operation in the filter circuit, single- and dual-mode, are considered. Some practical filter realizations suitable for UHF and microwave applications are also described.

1. INTRODUCTION

Considerable advances have been made over the last decade in technology of low-loss and temperature stable ceramic materials suitable in a high-frequency filter applications. Low-loss (or high Q), large dielectric constant, and low frequency-temperature coefficient are the most significant features of temperature compensated ceramic materials that make them very attractive for filter applications at UHF and microwave frequencies [1].

Typically, these filters employ a cylindrical or rectangular shaped dielectric resonator as a basic element in the bandstop, bandpass, and directional filter realizations. A dielectric resonator filter operation is based on a specific mode of dielectric resonator at which the coupling between resonators and distributed transmission medium can be realized and practically controlled in order to obtain the desired filter characteristics. Depending upon applications and frequency range the dielectric resonator filters use a rectangular waveguide, cylindrical waveguide, coaxial line, or microstrip line for transmission medium [2]. Typically, at the UHF frequencies the TEM coaxial transmission lines containing the dielectric ring resonator are most often used for the bandpass filter realizations [3]. At microwave and millimeter wave frequencies the waveguide or microstrip line are mainly used as transmission media since their fundamental propagation modes are compatible with the $TE_{01\delta}$ mode of dielectric resonator [1], [2].

The objective of this paper is to present a brief outline of dielectric resonator filter design methods and to discuss some practical design considerations related to bandpass and bandstop filter realizations.

$$q = Q_0 e^{-t/\tau} \qquad \text{(II-19)}$$

This equation shows the "natural recovery" curve in Figure II-11(b) and demonstrates the definition of lifetime as τ, the time constant of charge decay. In time $t = \tau$, q decays to 1/e or about 40% of its initial value. However, to make a practical measurement it is necessary to have a measurable quantity; this requirement is most easily fulfilled by providing a reverse current during recovery. Since the reverse current also removes charge from the I region, its effect must be included in the charge defining equation. Equation (II-18) then becomes

$$\frac{dq}{dt} = \frac{-q}{\tau} + I_D \qquad \text{(II-20)}$$

This expression is called the *continuity equation* for stored charge; the name underlies the fact that stored charge is neither created nor destroyed instantaneously, but rather has time continuity. This equation is general and applies for charge building with I_D positive, as well as for recovery when the diode bias current direction is reversed and I_D is negative. The solution, which can be verified by substitution into Equation (II-20), is

$$q = Q_0 e^{-t/\tau} + I_D \tau \qquad \text{(II-21)}$$

Imposing the condition that the stored charge be depleted in time $t = \tau$, as shown graphically in Figure II-11(b), and noting that $Q_0 = I_F \tau$ and that $I_D = -(I_R - I_F)$, Equation (II-21) gives

$$\left| \frac{I_R}{I_F} \right| = e^{-1} + 1 \approx 1.4 \qquad \text{(II-22)}$$

as the test condition under which $q = 0$ at $t = \tau_S = \tau$, permitting a convenient direct measurement. In practice, I_R and I_F can be monitored by connecting an oscilloscope across a small resistance in series with the diode under test. Switch S is realized using a pulse generator with repetition rate adjusted to permit the application of forward current, I_F, for a time which is long compared to the lifetime, τ, in order that the steady state charge, Q_0 equal to $I_F \tau$, is established before the recovery process is measured. A practical description of lifetime and switching speed measurements is given by McDade and Schiavone [7].

The Charge Control Model and Microwave Currents

We have just seen that, from transit time considerations, the PIN I region conductivity cannot follow a microwave signal because the diffusion of charge carriers isn't rapid enough to traverse the I region within the half period of an RF cycle. Moreover, from the preceding discussion of carrier lifetime it is clear that once charge is injected into the I region it resides there for 0.1-10 μs — the lower limit of which is even long compared to the 0.005 μs half period of, say, a 1 GHz signal. These two facts taken together indicate that the resistance behavior of the PIN at microwave frequencies can be described in terms of the charge present in the I region, q.

To illustrate this point, consider the diode I-V characteristic with superimposed RF excitations, as shown in Figure II-13. The I-V law shown is typical for a high voltage PIN. Under a forward bias current of 100 mA the I region becomes sufficiently conductive that its microwave impedance drops below 1 ohm of resistance (as we describe in the next section). If a microwave current having, say, 50 A peak amplitude (500 times the bias current) is then passed through the diode, the diode is found to remain in the low impedance condition despite the large "negative-going" half cycle of the RF waveform. The reason for this linear operation even under high RF current magnitudes is clear when the total charge movement produced by the RF signal is considered. Assuming a lifetime of 5 μs, typical of a high voltage PIN, the 100 mA bias results in a stored charge of 0.5 μC. However, during the negative-going portion of a 1 GHz sinusoid, the total charge movement is less than 0.025 μC, not even a tenth of the stored charge. This example epitomizes the charge control viewpoint that *it is the total stored charge produced by a bias which determines I region resistance rather than the instantaneous magnitude of an RF current.*

*Ryder** has likened the bias level on a PIN diode to "large signal" and the RF as the "small ac component," with respect to the amount of charge stored or removed from the I region. From the above example, the value of the charge control viewpoint is evident.

*R. Ryder (Bell Telephone Laboratories; Murray Hill, New Jersey) in a talk given at the NEREM Conference in Boston, circa 1970.

2. PRACTICAL DESIGN OF SINGLE-MODE DIELECTRIC RESONATOR FILTERS

Band-pass and band-stop filter design procedures are based on the low-pass prototype element model and a low-pass to band-pass or band-stop frequency mapping as described in [4]. All subsequent steps of the design procedure are outlined in Figure 1. It can be seen from Figure 1 that both maximally flat (or Butterworth) and equi-ripple (or Tchebyscheff) responses can be obtained following the design procedure outlined. It also follows that for the determination of a filter components, the dielectric resonator parameters required for a given circuit topology, such as the external Q's, Q_{ex}, and coupling coefficient k_i must be determined first. The $Q_{ex's}$ and k's values related to the physical dimensions of the filter can be obtained either analytically or expermintally or by combination of these two techniques.

With the reference to the band-pass filter equivalent circuit shown in Figure 2 the external Q, Q_{ex} and coupling coefficientds K_i's are functionally related to the circuit elements as follows [4]

$$Q_{ex1} = X_1/(K_{01}^2/R_1) = g_0\, g_1\, \omega_1'/W \qquad (1a)$$

$$Q_{ex_n} = X_n/(K_n^2,\ n+1/R_n) = g_n\, g_{n+1}\, \omega_1'/W \qquad (1b)$$

and

$$K_{i,\,i+1} = K_{i,\,i+1}/\sqrt{X_i,\ X_{i+1}} = W/\omega_1'\ \sqrt{g_i\, g_{i+1}} \qquad (2)$$

where $W = (\omega_2 - \omega_1)/\omega_o$ is the fractional bandwidth

ω_o is the center frequency of B-P filter

ω_i is the edge frequency of L-P prototype filter

$g_0, g_1, \ldots g_i, g_{i+1}, \ldots g_n, g_{n+1}$ are the elements of a L-P prototype filter.

It is essential, however, for a proper design to have the $Q_{ex's}$ and k's parameter values expressed in terms of the filter physical structure and dielectric resonator parameters.

In the most common case of the $TE_{01\delta}$ operation mode of cylindrical dielectric resonator being integrated with the waveguide or microstripline, approximate equations for the resonant frequency f_o, and unloaded Q factor, Q_o have been derived and practically verified in various designs [5], [6], [7].

However, there is no approximate expression available for a coupling coefficient, k, nor for resonator-to-resonator, nor transmission line-to-resonator coupling arrangements. Therefore, the best way in practice is to determine k from the external Q factor measurements for a pratical circuit structure, as any attempt to determine the coupling coefficient k value from analysis inevitably leads to rather complex algebra requiring the use of a computer to get the final solution.

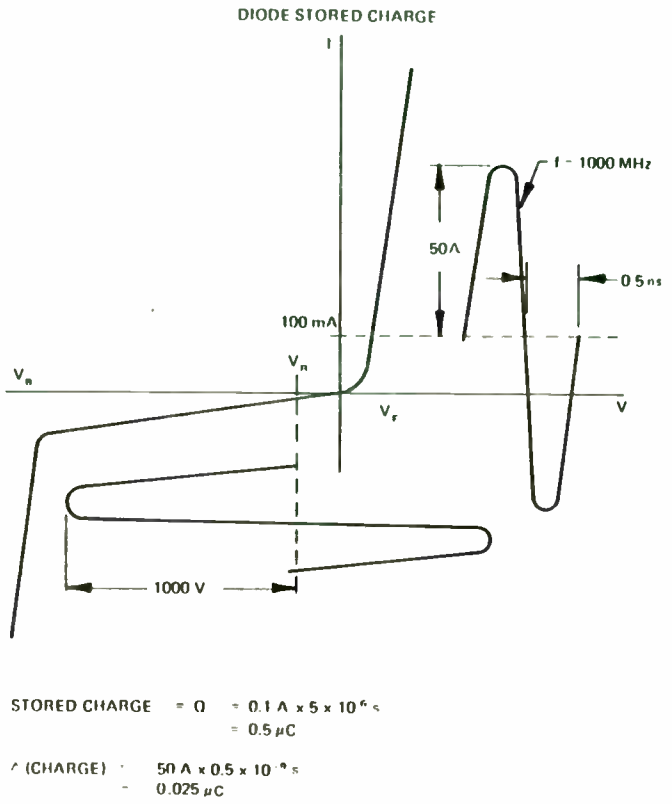

Figure II-13 Example Comparing Charge Stored by Bias to Charge Movement Due to High Level Microwave Signal

Under reverse bias, a relatively small voltage, about -100 V, is sufficient to hold off conduction of the diode under the application of an RF voltage whose peak voltage amplitude is as large as 1,000 V. Again, the brief duration of the half-period of the RF cycle is not sufficient to cause appreciable modulation of the I region of the diode, and the diode appears as a high impedance even with this large voltage magnitude applied.

One might ask why any reverse bias is necessary at all if the diode is nearly non-conducting at zero bias. First, reverse bias fully depletes the I region and its boundaries of charge. Thus, the diode has a higher microwave Q with reverse bias. Second, the role of a reverse bias is to maintain an average field which tends to prevent the accumulation of significant amounts of charge in the I region. The presence of excessive charge in the space, under high RF fields, can produce impact ionization, with a "runaway" current rise and resultant diode destruction. Nevertheless, under large RF excitation, impact ionization effects are often observed, resulting in a *pulse leakage current*, since it occurs only under the combined action of RF and reverse bias excitation. It is necessary that the driver circuit have *sufficiently low impedance* to be capable of providing this pulse leakage current (usually 1-5 mA) in a high power control device without causing an appreciable drop in the bias voltage supplied, if destructive diode conduction in the reverse bias state with high RF applied voltage is to be avoided.

2. Forward Biased I Region Resistance

Having demonstrated the suitability of the charge control approach for determining microwave properties, let us use it to calculate the conductivity and resistance of the I region under forward bias.

Conductivity, σ, is a bulk property equal to the ratio of current density, J, to applied electric field strength, E

$$\sigma = \frac{J}{E} \tag{II-23}$$

But J is the directed average rate of flow of electric charge. In terms of I region holes and electrons

$$\sigma = \frac{J}{E} = e\left(\frac{v_P \cdot p}{E} + \frac{v_N \cdot n}{E}\right) \tag{II-24}$$

Also, by definition, *mobility*, μ, is the average carrier velocity per unit of applied electric field, thus

$$\sigma = e(\mu_P p + \mu_N n) \tag{II-25}$$

If the Q_{ex} is obtained from measurements and the unloaded, Q, Q_o is for example determined analytically, then the coupling factor k can be obtained from

$$k = Q_o/Q_{ex} \qquad (3)$$

Considering a typical filter structure of the form shown in Figure 3 (a) and (b) the unloaded Q factor can be calculated using [5]:

$$Q_o = \frac{\varepsilon_r a + \varepsilon_s b_a d_s + b_a d_a}{\varepsilon_r a \tan\sigma_r + \varepsilon_s b_s d_s \tan\sigma_s + R\lambda_o^2 d_r/2\pi^2} \qquad (4)$$

Where the meaning of constants in (4) can be explained with the reference to Figure 3 as follows:

$$a = t + \sin(\gamma_r t)/\gamma_r$$

$$b_s = [\cos(\gamma_r t/2)/\sinh(\gamma_s S)]^2$$

$$b_a = [\cos(\gamma_r t/2)/\sinh(\gamma_a d)]^2$$

$$d_s = \sinh(2\gamma_s s)/2\gamma_s - S$$

$$d_a = \sinh(2\gamma_a d)/2\gamma_a - d$$

$$d_r = \sqrt{b_s b_a}\left[\frac{\gamma_s \sinh(\gamma_a d)}{\sinh(\gamma_s s)} + \frac{\gamma_a \sinh(\gamma_s s)}{\sinh(\gamma_a d)}\right]$$

where

$$\gamma_r = \left[\left(\frac{\omega_o}{c}\right)^2 \varepsilon_r - \left(\frac{u}{R}\right)^2\right]^{\frac{1}{2}} \qquad (5a)$$

$$\gamma_s = \left[\left(\frac{2.405}{R}\right)^2 - \left(\frac{\omega_o}{c}\right)^2 \varepsilon_s\right]^{\frac{1}{2}} \qquad (5b)$$

$$\gamma_a = \left[\left(\frac{2.405}{R}\right)^2 - \left(\frac{\omega_o}{c}\right)^2 \varepsilon_o\right]^{\frac{1}{2}} \qquad (5c)$$

where the parameter u in (5a) can be approximated as follows:

$$u = 2.32 + \sqrt{0.033\, R^2 \left(\frac{\omega_o}{c}\right)^2 - 0.185} \qquad (6)$$

under the assumption that $\varepsilon_r >> 1$, which holds for most dielectric resonators.

In order to assure that the filter circuit shown in Figure 3 is a bandpass type, which means that the RF power flow through the circuit relies on the presence of the $TE_{01\delta}$ mode of dielectric resonators, the metallic enclosure must act as a waveguide under cut-off conditions at the filter operated frequency. Otherwise, the circuit will operate as the bandstop filter with the signal power absorbtion at the frequency corresponding to the dominant $TE_{01\delta}$ mode (or possibly on some other adjacent hybrid modes).

where

$e = +1.6 \times 10^{-19}$ coulomb = magnitude of electron's charge

$\mu_{P,N}$ = mobility of holes and electrons respectively

p, n = respective injected hole and electron densities in I region

The formula for the resistance of a cylindrical conductor of electrical conductivity, σ, length W along the current path, and cross sectional area Λ is [9]

$$R = \frac{W}{\sigma \Lambda} \tag{II-26}$$

Using the dimensional notation of Figure II-10, the I region resistance is then

$$R_I = \frac{W}{e\Lambda(\mu_P p + \mu_N n)} \tag{II-27}$$

Three main assumptions* have been made in this derivation of R_I:

1) The I region as a whole is electrically neutral.
2) The bias current, I_0, injects holes and electrons which *recombine with each other in the I region;* the limitations of this assumption are discussed later.
3) The carrier lifetime is sufficiently long that both the holes and electrons are uniformly distributed within the I region. Another way of stating this point is that the average hole and electron diffusion lengths, L_P and L_N, are much longer than the I region width, W. This condition is usually valid for well designed PIN diodes and can always be verified by using the relation for diffusion length given below

$$L = \sqrt{D_{\Lambda P}\tau} \tag{II-28}$$

where

$D_{\Lambda P}$ = ambipolar diffusion constant = $2D_P D_N/(D_P + D_N)$

τ = lifetime within the I region

In silicon, $D_{\Lambda P}$ has an effective average value for holes and electrons, the *ambipolar diffusion constant,* of 15.6 cm^2/s [8]. Thus

$$L = 40\sqrt{\tau\ (\text{microseconds})}\ \ (\text{microns})$$
$$L = 1.7\sqrt{\tau\ (\text{microseconds})}\ \ (\text{mils}) \tag{II-29}$$

For example, if the bulk lifetime is 10 μs the diffusion length is about 133 μ (5 mils).*

Under these combined assumptions, it follows that the injected hole and electron densities are equal and uniform

$$p = n \tag{II-30}$$

and, furthermore, since they recombine with one another directly

$$\tau_P = \tau_N \tag{II-31}$$

Then

$$R_I = \frac{W}{2e\ \Lambda\ \mu_{\Lambda P}\ p} \tag{II-32}$$

where $\mu_{\Lambda P} = 2\mu_P\mu_N/(\mu_P + \mu_N)$, 610 $cm^2/V\text{-}s$ in silicon [8], is the *ambipolar mobility*, i.e., the effective average of the hole and electron mobilities. But the injected charge is directly proportional to the bias current.

$$Q_P = epA W = I_0\tau \tag{II-33}$$

Combining the last two equations gives

$$R_I = \frac{W^2}{2\mu_{\Lambda P}\tau I_0} \tag{II-34}$$

This expression is applied frequently. We note from it that R_I is theoretically independent of I region area, being proportional to the square of I region width and varying inversely with mobility, lifetime, and bias current. However, care must be taken in the application of Equation (II-34) to practical situations. In particular, the following generalizations should be qualified:

1) *Holding all process steps the same except for varying A produces a selection of diodes with different capacitances but the same R_I for a given bias current.* This situation is true only if

*Fletcher, Neville H.: "The High Current Limit for Semiconductor Junction Devices," *Proceedings of the IRE, Vol. 45,* pp. 862-872, June 1957.

*For an analysis of the case where this assumption is not made, see Leenov's paper, Reference 8.

In either case the resonant frequency of the circuit including the dielectric resonator operated in the $TE_{01\delta}$ mode may be determined using the transmission line equivalent circuit model introduced in [5] and [6]. For example, the frequency, f_o, of the structure shown in Figure 3(b) basically depends on the dielectric resonator parameters such as D - diameter, L - height, and dielectric permittivity ε_r being also a function of the circuit parameters described by the following two equations:

$$\gamma_r L = \tan^{-1}\left(\frac{\gamma_a}{\gamma_r}\coth(d\gamma_a)\right) + \tan^{-1}\left(\frac{\gamma_s}{\gamma_r}\coth(s\gamma_s)\right) \qquad (7)$$

and

$$\frac{J_1(u)}{u J_o(u)} = -\frac{K_1(W)}{W K_o(W)} \qquad (8)$$

where J_o and J_1 are Bessel functions of the first kind of nth order, while K_n is the modified Hankel function of the nth order. The γ_a, γ_r, and γ_s propagation parameters are defined by (5), with the u given by (6).

The following approximation can be used to simplify Eq. (2) [7]:

$$\frac{J_1(x)}{x J_o(x)} \simeq \frac{0.23}{(x-2.405)^{1.5}} \quad \text{for} \quad 2.405 < x < 3.83$$

$$\therefore \quad \simeq \frac{0.08}{(x-5.52)^{1.3}} \quad \text{for} \quad 5.52 < x < 7.02$$

$$\text{etc} \qquad (9)$$

and

$$\frac{K_1(x)}{x K_o(x)} \simeq \frac{2.06}{x^{1.3}} \qquad (10)$$

with

$$W = \sqrt{\left(\frac{\omega_o}{c}\right)^2 R^2 \varepsilon_r - u^2} \qquad (11)$$

Equations (7) to (11) can be used to determine the f_o value when the circuit's and dielectric resonator's parameters are known, or if the f_o is given to find the dielectric resonator parameters (the height L, for example) incorporated with a given circuit structure. In either case the calculations are carried out using a standard iteration method which leads to solution. Therefore, it is customary to asume an initial value for the dielectric resonator diameter D which would reduce the computation time, for example , an initial value for D can be determined from the following equation:

$$D = 2.405\,\frac{c}{\omega_o}\left[\varepsilon_r^{-\frac{1}{2}} + \varepsilon_s^{-\frac{1}{2}}\right] \qquad (12)$$

The resonant frequencies determined from measurements and the analysis using Eq. (7) - (11) for different values of a distance d are shown in Figure 4. The agreement between the

τ remains constant; but generally, τ decreases with a decrease in A, since I region carriers are then nearer to the periphery where recombination can occur more rapidly.

2) *R_I decreases as $(1/I_0)$.* Again, this statement holds true only so long as τ remains constant. However, as I_0 increases, carrier density increases, and the recombination probability increases, decreasing τ. Furthermore, a saturation is reached when p and n increase sufficiently that substantial injection (holes into the N+ region and electrons into the P+ region) becomes significant, in violation of the second assumption used to derive Equation (II-34). Put simply, if there are high densities of electrons and holes in the I region, their chance for recombining increases, decreasing the average lifetime, τ.

3) *Above the transit time frequency, R_I is essentially independent of frequency.* This stipulation is only approximately true for most microwave PIN applications. Skin effect causes both the contact and I region resistances to increase somewhat with frequency.

Despite these limitations, Equation (II-34) is very useful and is typically invoked to estimate I region resistance at microwave frequencies. For example, consider a PIN with a 100 μ (4 mil) I region and a 5 μs lifetime operated with 100 mA bias current.

Using $\mu \approx 610$ cm^2/V-s

$$R_I = \frac{10^{-4}\ \text{centimeter}^2}{(2)(0.1\ \text{ampere})(5 \times 10^{-6}\ \text{second})(610\ \text{centimeters}^2/\text{volt-second})}$$

$$= 0.16\ \text{ohm} \qquad \text{(II-35)}$$

This result is in reasonable agreement with the measured value of 0.3 Ω for a 1.56 mm (61 mil) diameter*, when one considers that the measured value includes resistive contributions of the ohmic contacts as well as those of the P+ and N+ regions. Furthermore, the lifetime at 100 mA is likely to be less than the 5 μs value which is measured at 10 mA — an additional factor contributory to a higher measured resistance than that calculated.

Using this example let us examine the role of skin effect in the forward biased I region. Using the parameters of the above example and solving Equation (II-26) gives $\sigma = 3\ (\Omega\text{-cm})^{-1}$. The skin depth, δ, in a conductor is given by [9]

$$\delta = \frac{1}{\sqrt{\pi f \mu_0 \sigma}} \qquad \text{(II-36)}$$

where f = operating frequency (hertz)

$\mu_0 = 4\pi \times 10^{-9}$ henry/centimeter = free space permeability

σ = conductivity (ohm-centimeters)$^{-1}$

From Equation (II-36), the skin depth for $\sigma = 3\ (\Omega\text{-cm})^{-1}$ at 1 GHz is 0.09 cm, about equal to the diode radius. This diode example has a junction capacitance of about 2 picofarads and would not usually be used at frequencies much above 1 GHz. At higher frequencies a lower capacitance, and hence reduced diameter, would be employed. Thus, it can be seen I region* skin effect usually has but a moderate effect in PIN control devices in the 0.1 to 10 GHz frequency range.

Before leaving the subject of I region conductivity it is interesting to note what level of carrier density, p, was injected into the I region of this sample diode to produce $R_I = 0.16\ \Omega$. An estimate can be made using Equation (II-32) and $\mu \approx 610$ cm^2/V-s, thus

$$p = \frac{W}{2eA\mu R_I} = 1.7 \times 10^{16}/\text{cubic centimeter} \qquad \text{(II-37)}$$

Since there is an approximately equal electron density, n, in the I region, the total free carrier density required to produce $R_I = 0.16\ \Omega$ is 3.4×10^{16}/cm^3. Recalling that the atom density is about 10^{23}/cm^3, this figure represents *less than one carrier per million atoms.* It is therefore easy to see why the skin depth, so significant with metallic conductors at microwave frequencies, has only a moderate effect even under "high injection" levels in the I region of the PIN diode.

3. R_R and C_J Reverse Biased Circuit Model

Under reverse bias the I region is depleted of carriers and the PIN appears as an essentially constant capacitance to a microwave signal. The presence of dissipative losses can be taken into account by either a series or parallel resistance element in the equivalent circuit. In a well-made PIN, the I region has sufficiently high resistivity that most of the dissipation under low RF power conditions occurs in the ohmic contacts made to the diode and in the resistances of the P+ and N+ regions. Accordingly, a fixed series resistance, R_R, used to represent these losses can be expected to offer an equivalent circuit model which is applicable over a broader

*See data for the MA-47891 PIN diode in Table III-1, pp. 94-95.

*Skin resistance may be more important in the P and N regions and in the leads attached to them because it affects how the currents enter the I region.

results obtained is very good. It can be observed from Figure 4 that the resonant frequency, f_o is sensitive to the change of distance, d, which in practical filter realizations can be used for frequency tuning. The unloaded Q factor, Q_o for the resonator incorporated in the structure shown in Figure 4 was 3000 determined from measurements and 2200 using Eq (4), both at frequency 10GHz.

The band-pass filter for operation at 10 GHz center frequency has been designed using two identical dielectric resonators (with the parameters shown in Figure 4) to obtain maximally flat (Butterworth) transfer characteristic with the 3 dB bandwidth of 50 MHz. The filter was made in the form shown in Figure 3. With the 50 ohm terminations the filter has an external Q factor, $Q_{ex} = 380$.

The low pass filter prototype elements used in computation were: $g_o = g_3 = 1$ and $g_1 = g_2 = \sqrt{2}$, and the coupling coefficient k_{12} between resonators was approximately equal to 3.5×10^{-3}, corresponding to the spacing l between resonators of 4.2 mm. The distance d between the top wall of the resonator metallic enclosure and the upper surface of each resonator has been set at 0.5 mm. A good agreement between the designed and measured characteristics of the filter has been obtained. The filter insertion loss within the pass-band determined experimentally was 1.7 dB at 10 GHz.

An example of another band-pass or band-stop filter realization is shown in Figure 5. This filter realization employes axially coupled cylindrical resonators suspended in the circular waveguide which is furnished with two coaxial couplings. Each resonator has a small centre hole to accommodate the coaxial arrangement of the filter structure. The hole diameter, d_i must be much smaller in comparison with the diameter of dielectric resonator, D to assure almost undisturbed propagation of the $TE_{01\delta}$ mode. It has been found that the presence of a small hole in the centre of dielectric resonator helps to better separate the HE modes from the operational $TE_{01\delta}$ mode [8]. The input/output coaxial coupling probes are usually adjusted experimentally for an optimal coupling condition.

The coupling coefficient, k between resonators may be determined using the following formula, provided that $d_i \ll D$;

$$k = \frac{F}{2\pi d_e^4} \sum_{n \geq 1} \frac{U_{on}^2}{A_n^2} B_n \frac{e^{-\alpha_{on} s}}{\alpha_{on}} \qquad (13)$$

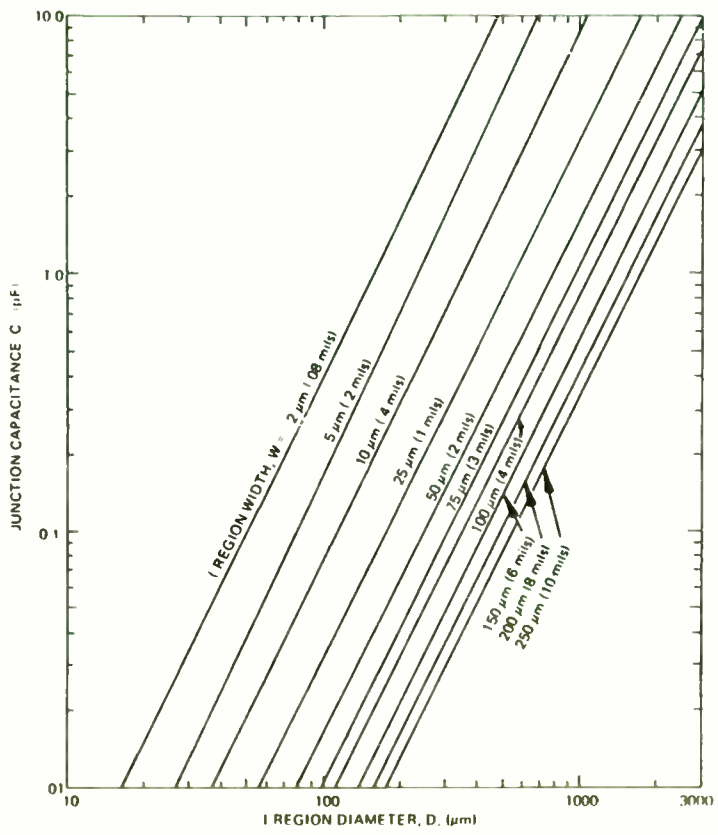

Figure II-14 PIN Diode C_J vs. I Region Diameter and Thickness

bandwidth than a parallel conductance. In any event, due to the ratio of diode capacitive reactance to practical RF circuit impedances, the dissipative losses of the PIN under reverse bias are usually much smaller than those under forward bias; thus, the choice of series or parallel R-C equivalent circuit under reverse bias usually can be made according to whichever offers greater computational convenience.

Because of the high relative dielectric constant for silicon (ϵ_R = 11.8), the fringing capacitance (in air) around the I region is relatively small and the capacitance calculated using the parallel plate capacitance formula given below provides a useful estimate of junction capacitance, C_J. Thus

$$C_J \approx \frac{\epsilon_0 \epsilon_R \pi D^2}{4W} \qquad \text{(II-38)}$$

where $\epsilon_0 = 8.85 \times 10^{-14}$ farad/centimeter = free space permittivity

$\epsilon_R = 11.8$ = relative dielectric constant for silicon

D = junction diameter

W = I region thickness

For many design calculations – estimating thermal capacities, breakdown strength, and RF bandwidth – it is desirable to be able to interrelate the tradeoffs between I region dimensions (W and D) and junction capacitance (C_J). Figure II-14 shows Equation (II-38) graphically for typically available PIN I region widths.

4. Microwave Circuit Measurements and Cutoff Frequency, f_{cs}

Equivalent Circuit Definition and f_{cs}

The microwave equivalent circuit for the unpackaged PIN diode chip to be used in this text is shown in Figure II-15. In most applications the PIN diode is used as a switch; therefore, the less capacitance, the better an "open circuit" it presents with reverse bias. The lower the resistances, R_F and R_R, the smaller the dissipative losses, and, under forward bias, the more the diode resembles a "short circuit." A figure of merit has been defined [10] to relate the PIN's switching effectiveness, termed *switching cutoff frequency*, f_{CS}. The utility of this definition is apparent later in the discussion of performance limitations.

$$f_{CS} = \frac{1}{2\pi C_J \sqrt{R_F R_R}} \qquad \text{(II-39)}$$

The equivalent circuit parameters are as defined in Figure II-15. Because the additional loss at high power is treated here by a separate equivalent circuit element, G_R, the *definition of f_{CS} as used in this text is limited to microwave power levels below the onset of nonlinear dissipation.* The effect of G_R is discussed in the next section.

where

$F = 15.2 \frac{D^4 L}{\lambda_o^2} \varepsilon_r \, (cm)^3$ with the assumption that,

$0.25 < L/D < 0.7$

λ_o is the free space wavelength corresponding to the resonant frequency f_o.

$A_n = 1 - (U_{on} D/2 \, p_{01} d_e)^2$ is the resonator/circuit parameter

U_{on} are the roots of Bessel function: $J_1(u) = 0$, i.e.,

$U_{01} = 3.832$, $U_{02} = 7.016$, etc.

with $n = 1$ for $s > 0.6$

and $n = 2$ for $0.16 < s < 0.6$

$s = 1 + L$ is the center-to-center spacing between resonators.

$P_{01} = 2.405$ is the first root of Bessel function: $J_0(u) = 0$

$\alpha_{on} = \frac{2\pi}{\lambda_{on}} \left[1 - (\lambda_{on}/\lambda)^2\right]^{\frac{1}{2}}$ is the attenuation constant of TE_{on} mode ($\lambda_{01} = 1.64 \, d_e$, $\lambda_{02} = 0.896 \, d_e$, etc)

$B_n = J_o^2 (U_{on} D/2 \, d_e)/J_o^2 (U_{on})$ is the ratio of a squared Bessel functions (zero order).

Equation (13) is typically solved for the s value with the values of coupling coefficients k's constrained by the low-pass filter prototype parameters and the remaining circuit parameters intially pre-determined (including dielectric resonators). The dielectric resonator parameters; D, L, d_i and ε_r, should be computed first based on the resonant frequency, f_o, required for the filter in both band-pass and band-stop designs.

3. PRACTICAL DESIGN OF DUAL MODE DIELECTRIC RESONATOR FILTERS

The dual-mode dielectric resonator BP filter is a fairly new development in the microwave filter technology [9]. It is based on a dual- mode cavity approach which proved to be a very successful for the elliptic-type transfer characteristic realizations. The implementation of dielectric resonators into a classical dual- mode cavity filter leads to its weight and size reduction. A typical section of a dual-mode filter loaded by a cylindrical dielectric resonator is shown in Figure 6. The HE_{11} hybrid mode of dielectric resonator is employed in the filter operation. To design microwave cavity filters with dielectric resonators, determination of two basic factors; the resonant frequency of the cavity and coupling coefficients between

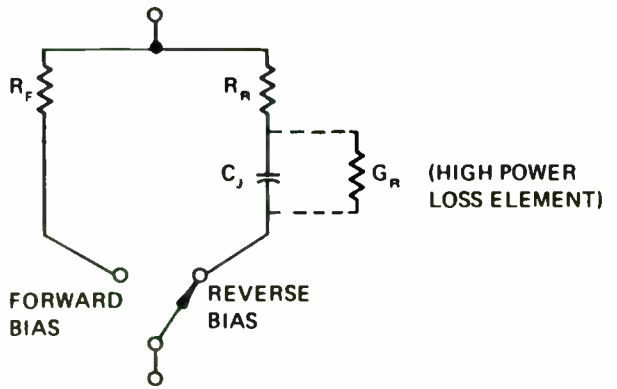

Figure II-15 PIN Diode Chip Equivalent Circuit

In principle, the values for R_F and R_R could be evaluated and f_{CS} could be specified under high power conditions. But it is not usually possible to obtain diodes characterized under high power as this task falls to the circuit designer; for this reason the separation of low and high power characterization is more consistent with actual practice.

Isolation Measurements

It was shown earlier, C_J measurements made at low frequency ($\approx$ 1 MHz) with sufficient reverse bias to deplete the I region provide a useable indication of the microwave capacitive reactance to be expected. However, the *resistances under forward, R_F, and reverse, R_R, bias conditions must always be determined by direct microwave measurements* since they include not only the inherent I region loss effects of the diode but P+ and N+ region as well as contact resistances, none of which is predictable with desirable analytic precision. Since, in most control device circuits, the greater microwave dissipation occurs under forward bias, the determination of R_F usually warrants the greater attention.

Many diode resistance measurement methods have been described. [11, 12] Ultimately the diode loss in the actual circuit of use is what is desired. For determining R_F, in either a test circuit or the actual circuit of use, the terminals where the diode is to be connected are short circuited and the loss of the circuit without diodes (i.e., the *cold circuit loss*) is measured. The additional circuit loss with diodes installed can then be attributed to the diodes themselves and, if the RF currents through the diodes can be estimated, the equivalent circuit parameters can be determined. Of course, by this time the insertion loss of the circuit under test is known and the value of knowledge of the diode equivalent circuit parameters is only of use in future design applications. Nevertheless, such direct evaluation in the circuit of end use is often required especially where diodes are circuit mounted in chip or beam lead configurations, requiring permanent bonding into the circuit to make the adequate ohmic contact necessary for accurate resistance determinations.

The two most common methods used to characterize PIN diodes, outside of the circuit of end use, are the *isolation* and *reflection* (or "slotted line") measurements.

To make an isolation measurement, the diode is used to interrupt a transmission line. When the diode is mounted in shunt with the line (Figure II-16), this method provides a sensitive measurement of the forward resistance, R_F. The isolation produced by a line shunting admittance Y is (the derivation is in Chapter V)

$$\text{Isolation} = \frac{P_A}{P} = \frac{V_A^2/Z_0}{V_L^2/Z_0} = |1 + YZ_0/2|^2 \qquad \text{(II-40)}$$

$$= 1 + GZ_0 + \frac{G^2Z_0^2}{4} + \frac{B^2Z_0^2}{4}$$

where $Y = Z^{-1} = G + jB$

To achieve the maximum test sensitivity, any series inductance introduced when mounting the diode across a transmission line is series resonated by a tunable capacitor. For this reason the measurement is most practical in the 0.5 to 1.0 GHz frequency range. Under these conditions the net series reactance, jX, of the mounted diode is zero and Equation (II-40) reduces to

$$\text{Isolation} = 1 + \frac{Z_0}{R} + \frac{Z_0^2}{4R^2} \qquad \text{(II-41)}$$

individual cavities or input/output coupling ports is necessary. With reference to the cavity shown in Figure 6 the resonant frequency, f_o, can be obtained by solving the following two equations [9].

$$\beta \tan(\beta L/2) \tanh(\gamma_o s) - \gamma_o = 0 \qquad (14)$$

where $S = (T - L)/2$, and

$$\gamma = [(1.841/B)^2 - k_o^2]^{\frac{1}{2}}$$

and

$$\left(\frac{\epsilon_r}{p} A_1 J' + \frac{b_2}{h} J\right)\left(\frac{b_1}{h} J' + \frac{a_2}{h} J\right) - \frac{\beta^2}{k_o^2 R^2} a_1 b_1 J^2 \left(\frac{1}{p^2} + \frac{1}{h^2}\right)^2 = 0 \qquad (15)$$

where $a_1 = K_b I_a - I_b K_a$

$a_2 = K_b' I_a - I_b' K_a'$

$b_1 = K_b' I_a - I_b' K_a$

$b_2 = K_b' I_a - I_b K_a'$

$J = J_1(hR)$

$I_a = I_1(pR)$, $I_b = I_1(pB)$

$K_a = K_1(pR)$, $K_b = K_1(pB)$

where $K_1(x)$ is modified Hankel function

$I_1(x)$ is modified Bessel function

with the primes denoting a differentiation in respect to argument and

$$h = (\epsilon_r k_o^2 - \beta^2)^{\frac{1}{2}}$$

$$p = (\beta^2 - k_o^2)^{\frac{1}{2}}$$

$$\beta = \pi/L$$

$$k_o = \omega\sqrt{\mu_o \epsilon_o} = 2\pi/\lambda_o$$

where λ_o is the free space wavelength corresponding to the resonant frequency f_o.

The coupling coefficient, k, between the cavity sections of the form shown in Figure 6 can be determined from the following equation.

$$k = \frac{\mu_o}{\epsilon_o} M \frac{|H_t|^2}{\int |\bar{E}|^2 dV} = 0.4082 M \frac{(1.841/B)^2 \gamma_o^3}{k_o^2 [\sinh(\gamma T) - \gamma_o T]} \qquad (16)$$

where M is the magnetic polarizability of the coupling aperture.

Equation (16) can serve only as a good estimate of the coupling coefficient value, since in practice some adjustments of the coupling slot length, l, and its width, w, are necessary. A

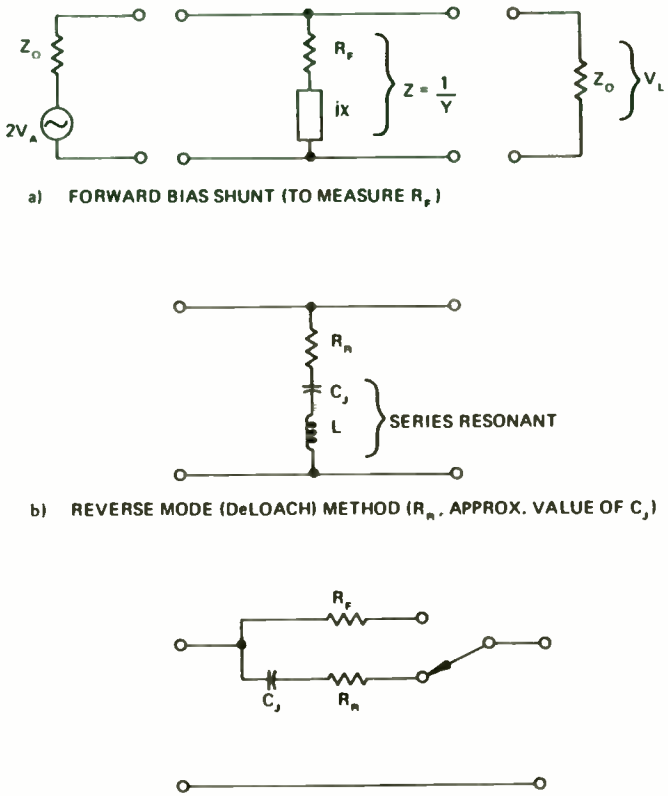

Figure II-16 Equivalent Circuits for Diode Measurements.

Thus, for example, if a series resonated diode having forward resistance of 1 Ω shunts a 50 Ω line, the normalized conductance, GZ_0 equals $Z_0 R_F = 50$. The resulting isolation equals 676, or approximately 28 dB. The resistance limited isolation described by Equation (II-41) is encountered often in both diode measurement and SPST switch design. For convenient reference it is shown graphically in Figure II-17.

There are some fine points to be considered in performing this measurement. First, if the diode is mounted in a package, the

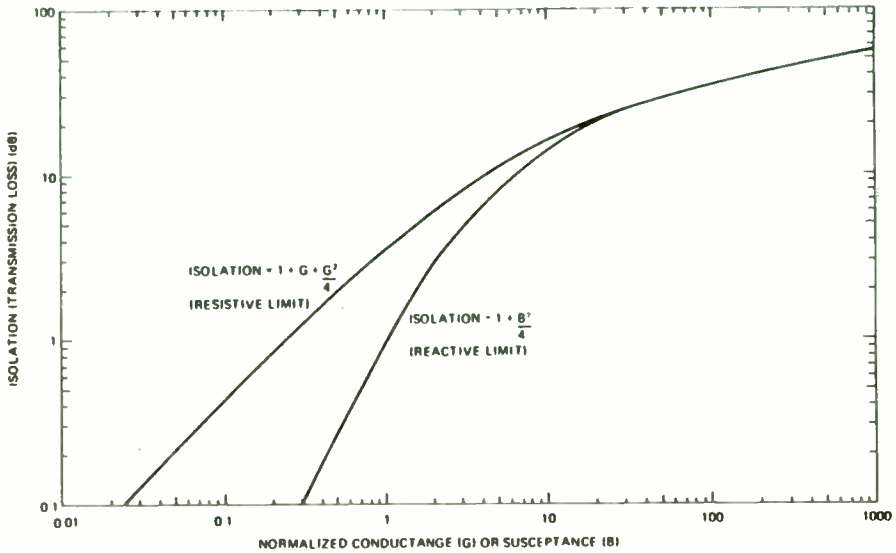

Figure II-17 **Isolation of Line Shunting G or B**

package capacitance transforms the effective resistance of the diode. This effect is usually negligible in the 0.5-1.0 GHz frequency band. Second, the circuitry used must not have significant leakage paths whereby power can reach the load from the generator by alternate paths such as higher order waveguide modes, fringing electric fields and so forth. This condition is readily tested by measuring isolation with the diode replaced by a short circuit of dimensions similar to the diode. Apart from ensuring that the leakage through the device is within acceptable limits, the isolation value so obtained gives an indication of the circuit *contact resistance. It is common practice to subtract contact resistance when quoting diode resistance.*

An interesting variation of the shunt mounted isolation measurement occurs when C_J series resonates with the mounted inductance of the diode (Figure II-16(b)). Then the diode shorts the transmission line under *reverse bias* and the isolation is a measure of R_R. From the isolation bandwidth an estimate of C_J is possible. This technique is usually used in waveguide at high frequencies, 5-15 GHz, to effect resonance with C_J. Switches built this way are often called *reverse mode*; the measurement technique is called the DeLoach method. [11] The reverse mode switching circuit is

fine tuning of the resonant frequency in each filter section shown in Figure 6 can be achieved by using metallic screw-tuners mounted on the cylindrical wall of the filter. A 4-pole, elliptical-type band-pass filter for operation at the center frequency of 4.2 GHz using the filter modules shown in Figure 6 has been recently reported [9]. This filter is currently used for the satellite communication applications.

4. CERAMIC MATERIAL COMPOSITIONS USED FOR DIELECTRIC RESONATORS

The first number in the parentheses corresponds to materials dielectric permittivity and the second one to the temperature coefficient of resonant frequency in ppm/°C.

- $Ba\ (Zn_{1/3}Nb_{2/3})O_3$ } (38, ± 4)
- $Ba\ (Zn_{1/3}Ta_{2/3})O_3$ }
- $Ba\ Ti_4\ O_9$ (38, +10)
- $Ba_2\ Ti_9\ O_{20}$ (40, +2)
- (Zr, Sn) TiO_4 (~35, 20)
- (Ca, Sr)(Ba,Zr)O_3 (~30, 50)

Typical values of Q's for the dielectric resonators using above ceramics are in the range of 5000-10000 at 10 GHz.

5. CONCLUSION

Design aspects of the bandpass and bandstop filters using dielectric resonators for microwave and UHF applications have been discussed. Some practical filter realizations have been presented. Due to their relatively small size and light weight, they are ideally suited for operation in the space technology applications. These filters also offer excellent temperature stability and can be developed at a low cost.

It has been also shown that both types of filters discussed in the paper can be designed using standard filter synthesis method.

6. REFERENCES

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important for duplexer and radar receiver protector designs where isolation in the zero biased diode state is required, as well as in other *fail safe* applications where it is desirable that, should there be a failure of the driver to bias the diode, the high reflection state of the diode switch is obtained.

If the diode is mounted in series with the line (Figure II-16(c)) the high isolation condition gives a measurement of capacitive reactance, X_C, equal to $-(2\pi f C_J)^{-1}$, and hence, C_J. For an impedance $Z = R + jX$ in series with a line of characteristic impedance, $Z_0 = 1/Y_0$, the isolation, by duality, is given by the dual of Equation (II-41)

$$\text{Isolation} = \left|1 + \frac{ZY_0}{2}\right|^2 = 1 + RY_0 + \frac{(RY_0)^2}{4} + \frac{(XY_0)^2}{4} \qquad \text{(II-43)}$$

If $|X_C| > 15\ R_R$, as is almost always the case, the RY_0 terms in Equation (II-43) can be ignored with an error of less than 1%, and the reactance versus isolation can be read directly from the reactance dominated characteristic curve shown in Figure II-17. This method is especially useful for measuring the circuit mounted capacitance of low capacitance devices such as beam lead diodes.

Series mounted diodes require special equivalent circuit treatment. Figure II-18 shows schematically the electric field contours of a capacitor representing a reverse biased diode both within and without a series coaxial line mounting. Measured in free space, all E field lines terminate on the diode terminals directly, and a capacitance, C_0, is measured. When mounted in the coax line, however, some E field lines intercept the outer conductor. The effect is that the effective series capacitance, C, is less than C_0. An additional shunt capacitance, C_2, appears, but in most cases the effect of C_2 on the transmission line is negligble, since it serves to replace the distributed capacitance of the section of center conductor removed to install the diode. However, the fact that the mounted series capacitance, C_1, is less than the capacitance associated with the diode, C_0, means that a higher isolation is obtained in a switching circuit (generally a benefit). Moreover, in a phase shifter circuit a different phase shift than that anticipated will be obtained if this effect is overlooked.

The accuracy of the series measurement can be related to the loss and isolation measurement accuracies. Typically the series isolation

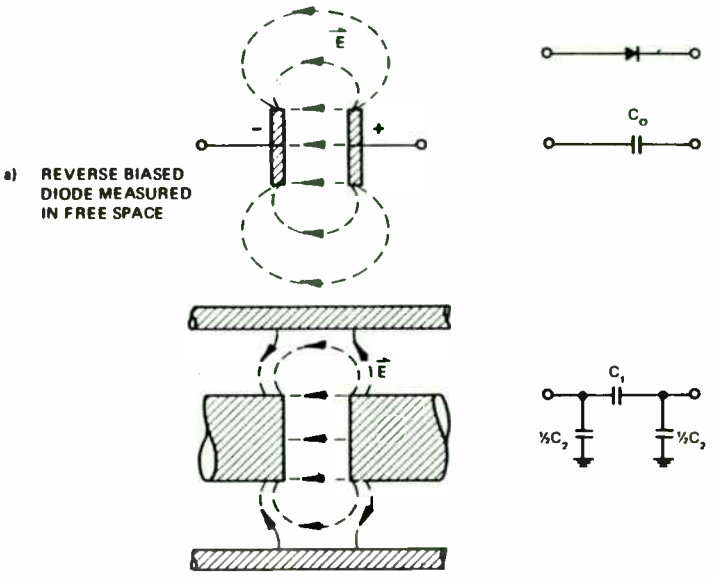

Figure II-18 Change of Effective Series Capacitance with Circuit Mounting

(or loss) measurement can be made to within an accuracy of ±0.1 dB for losses below 3 dB, and ±0.3-0.5 dB for isolation values from 10-40 dB. Thus, R_F can be determined to an accuracy of about ±2%; X_C, to about ±5% of the magnitude of Z_0. For most PIN diodes operated at sufficient forward bias to saturate the I region, $R_F < 1\ \Omega$; this measurement method would require impractically low Z_0 for meaningful measurements. However, for R_F measurements at low bias levels or with beam lead diodes wherein R_F = 2-10 Ω, the measurement is very practical using standard 50 Ω line. For example, a beam lead diode having $R_F = 5\ \Omega$ produces a 10% insertion loss of about 0.5 dB. The same diode, having C_J = 0.03 pF, has a reactance of -j795 Ω at 10 GHz, yielding, in the same test fixture, isolation under reverse bias at 10 GHz of 24 dB.

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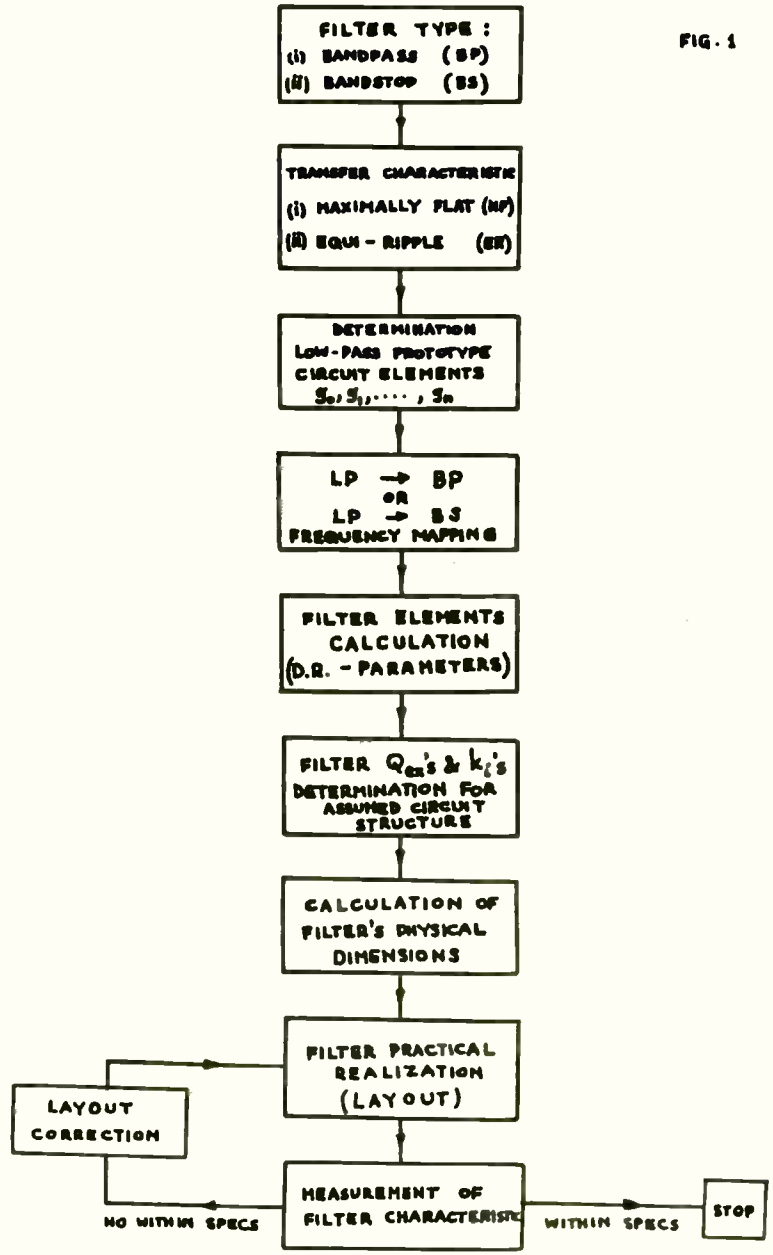

FIG. 1

*Reflection Measurements**

Most of the principles described for isolation measurements are likewise applicable to reflection measurements wherein the diode is used to terminate the line (Figure II-19); the reflection coefficient (Γ equal to $\rho e^{j\phi}$) measurement is used to deduce diode parameters. Other things being equal, the sensitivity of this measurement method is about four times that of the matched load method described previously in the determination of R_F and R_R for a given line impedance and dissipation; therefore, it is used for most standard diode characterizations. Diode reactances under both forward and reverse bias can be determined from the reflection coefficient argument.

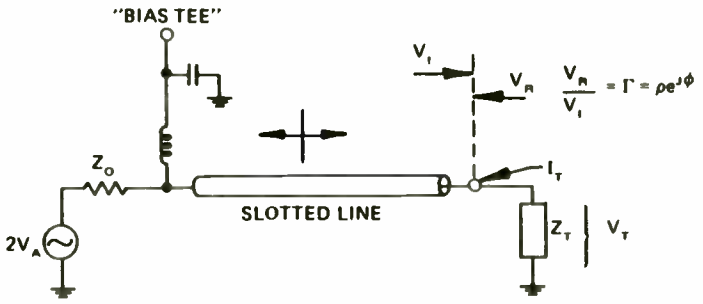

Figure II-19 Reflection Measurement Equivalent Circuit

The added sensitivity arises because, if the magnitude of Γ_L is either high or low compared to Z_0, the current (I_L) or voltage (V_L) at the end of the line is nearly double the value (V_A/Z_0 or V_A, respectively) experienced under matched load ($Z_L = Z_0$) conditions; the relative power absorbed in the diode consequently increases fourfold. For both a load impedance $Z_L = R_L + jX_L$ and a line with Z_0 characteristic impedance, the reflection coefficient at the load position is [13, 14]

$$\Gamma = \rho e^{j\phi} = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{(R_L - Z_0) + jX_L}{(R_L + Z_0) + jX_L} \qquad \text{(II-44(a))}$$

$$\phi = \tan^{-1}\left(\frac{X_L}{R_L - Z_0}\right) - \tan^{-1}\left(\frac{X_L}{R_L + Z_0}\right) \qquad \text{(II-44(b))}$$

*See Appendix J, The Smith Chart, for the development of reflection principles.

$$\rho = \sqrt{\frac{(R_L - Z_0)^2 + X_L^2}{(R_L + Z_0)^2 + X_L^2}} \qquad \text{(II-44(c))}$$

The fractional dissipation in Z_L is

$$\text{Insertion Loss} = 1 - \rho^2 = \frac{4\,R_L Z_0}{(R_L + Z_0)^2 + X_L^2} \qquad \text{(II-45)}$$

Under forward bias, using $Z_0 = 50\ \Omega$, both R_L and X_L are usually much less than Z_0. The fractional power loss is approximately equal to $4R/Z_0$. Under the same approximation, the insertion loss ratio by the series isolation measurement is approximately equal to $1 + R/Z_0$ and the *fractional loss* is approximately R/Z_0, only one fourth that of the reflection measurement. Thus, for example, with $Z_0 = 50\ \Omega$ and $R_F = 1\ \Omega$, the measured loss is about 0.4 dB with the reflection method and 0.1 dB with the isolation method, giving (with ±0.1 dB accuracy) the determination of R_F with ±0.25 Ω and ±1.0 Ω accuracies, respectively. Accordingly, when the diode is mounted in series with the line, the reflection measurement is usually employed for determining R_F.

This method is also used for determining R_R and C_J, but the calculations are less convenient than for R_F because the series reactance, X, cannot be ignored. Furthermore, the impedance transformation effects of a diode package (the package being necessary if the diode is to be conveniently mounted at the end of a slotted line) are not negligible in the reverse biased condition. For routine diode evaluation the reflection coefficient magnitude, ρ, and phase, ϕ, are measured and the exact equations relating diode C_J and R_R are solved using a computer program.* It is common practice to use a coaxial line and obtain a zero impedance reference by short circuiting the line at the leading surface of the diode package (as shown in Figure II-20). Both a phase reference ($\phi = 180°$) and a loss reference ($\rho = 1.0$) are thereby established. The packaged diode impedance, Z_L, is then evaluated by solving Equation (II-46) for Z_L

$$Z_L = R_L + jX_L = Z_0\,\frac{(1+\Gamma)}{(1-\Gamma)} = Z_0\,\frac{(1+\rho e^{j\phi})}{(1-\rho e^{j\phi})} \qquad \text{(II-46)}$$

*Computer programming for circuit evaluation is discussed in Chapter VI.

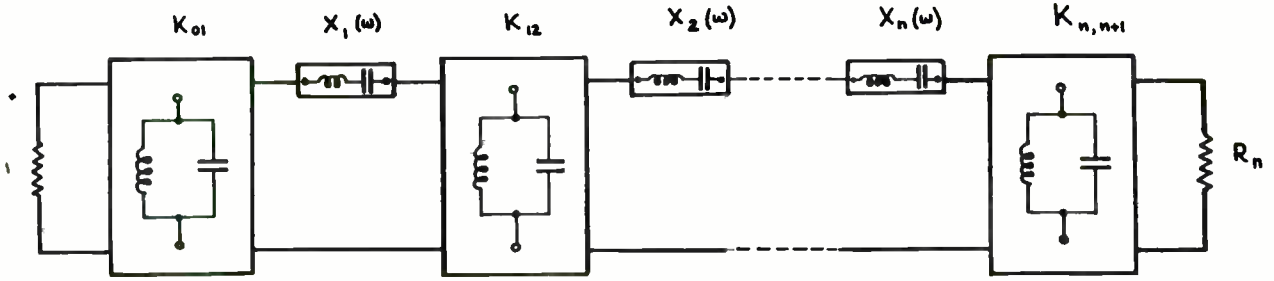

FIG. 2

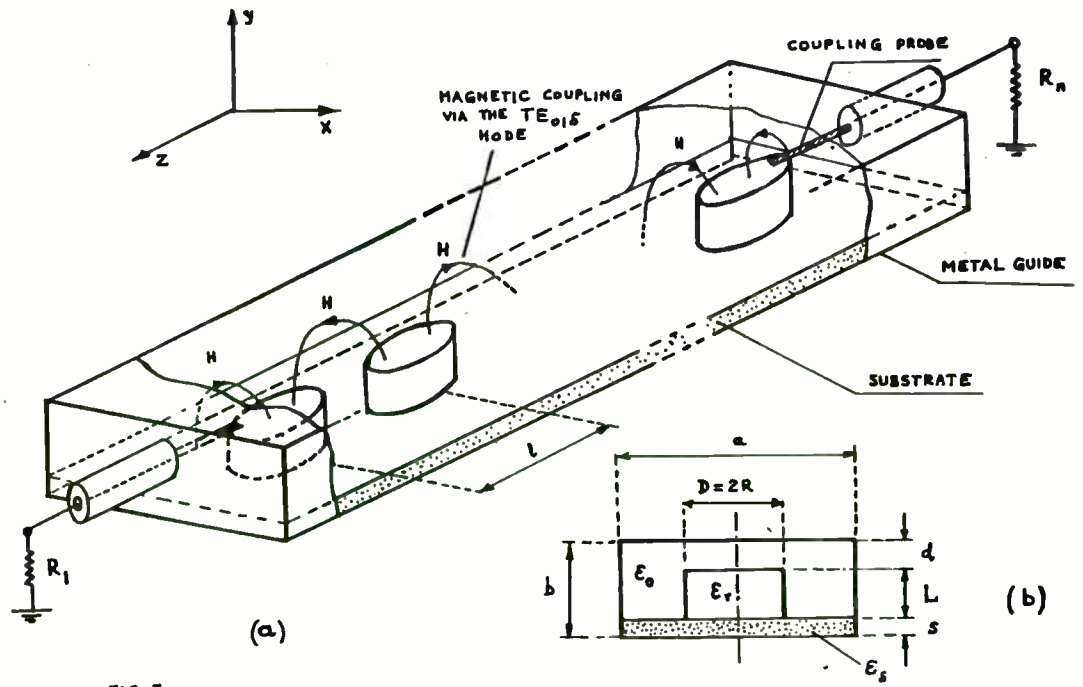

FIG. 3

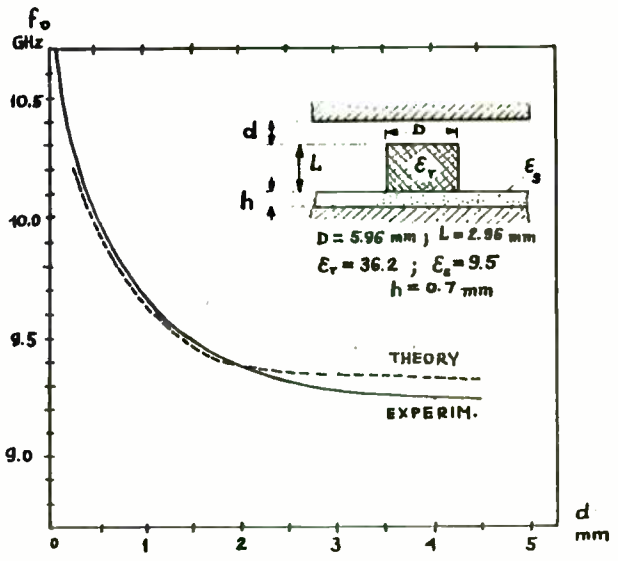

FIG. 4

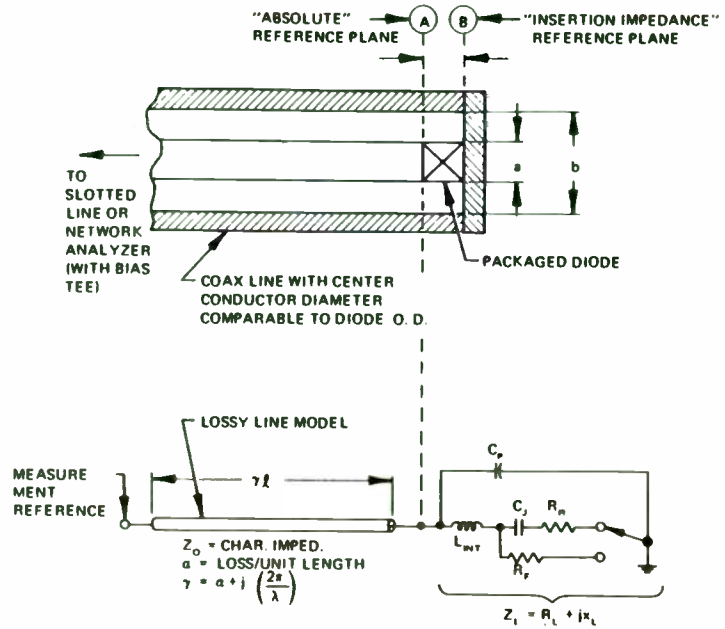

Figure II-20 Schematic and Equivalent Circuit Detail for "Slotted Line" Measurement of Packaged PIN Diode

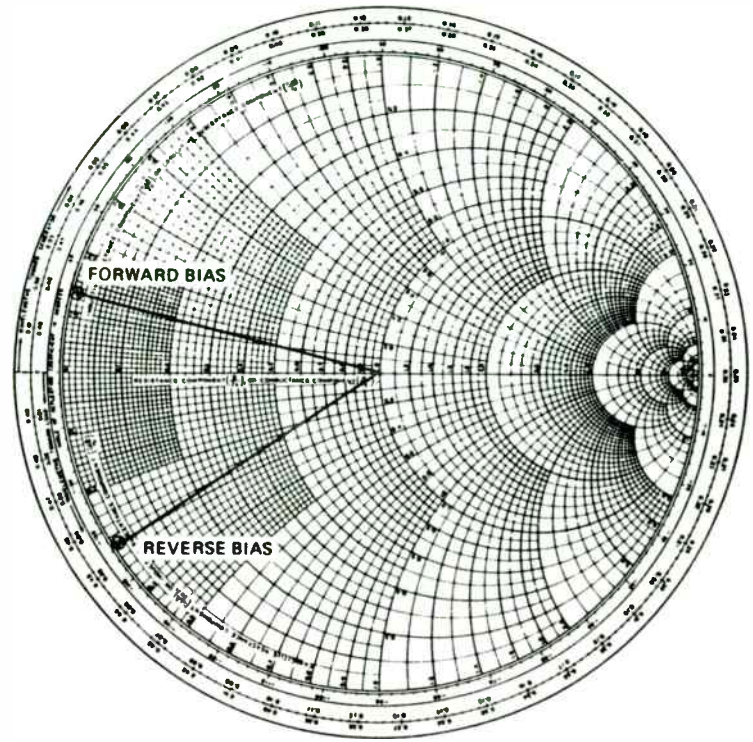

Figure II-21 Reflection Coefficients for Measurement Example

It is illustrative of the measurement method to plot the reflection coefficients obtained under forward and reverse bias on the Smith Chart. For this example, consider a PIN with C_J = 2 pF, $R_R = R_F$ = 0.3 Ω mounted in a package having C_P = 1 pF and L_{INT} = 0.3 nH. At 3 GHz the *chip* impedances are 0.3 Ω and (0.3−j26.5) Ω under forward and reverse bias; they are transformed by the package to (0.37+j6.30) Ω and (0.15−j15) Ω, respectively. When normalized to Z_0 = 50 Ω the corresponding reflection coefficients are (from Equation (II-44)) $\Gamma = 0.986/165.6°$ with forward bias and $\Gamma = 0.976/-145.8°$ with reverse bias. These results are shown graphically in Figure II-21. The proximity of the points to the Smith Chart periphery ($\rho = 1.0$) underscores the need for careful measurements if R_F and R_R are to be evaluated accurately.

While the application of the principles of this method is straightforward, great care must be exercised if results with useful accuracy are to be obtained. Since a single frequency measurement of Γ produces only two bits of data, ρ and ϕ, it is necessary either to have foreknowledge of the values of package *parasitics* (internal inductance, L_{INT}, and package capacitance, C_P) or to perform the reflection measurement at more than one frequency in order to solve for C_P, C_J, R_R, and R_F. In practice the former method is usually followed. C_P is first determined using an empty diode package; this result for C_P is used with an internally shorted package having a wire or strap lead similar to that to be employed with the diodes to be measured. In this respect, the eventual accuracy of evaluation of C_J and R_R is dependent upon the reproducibility of

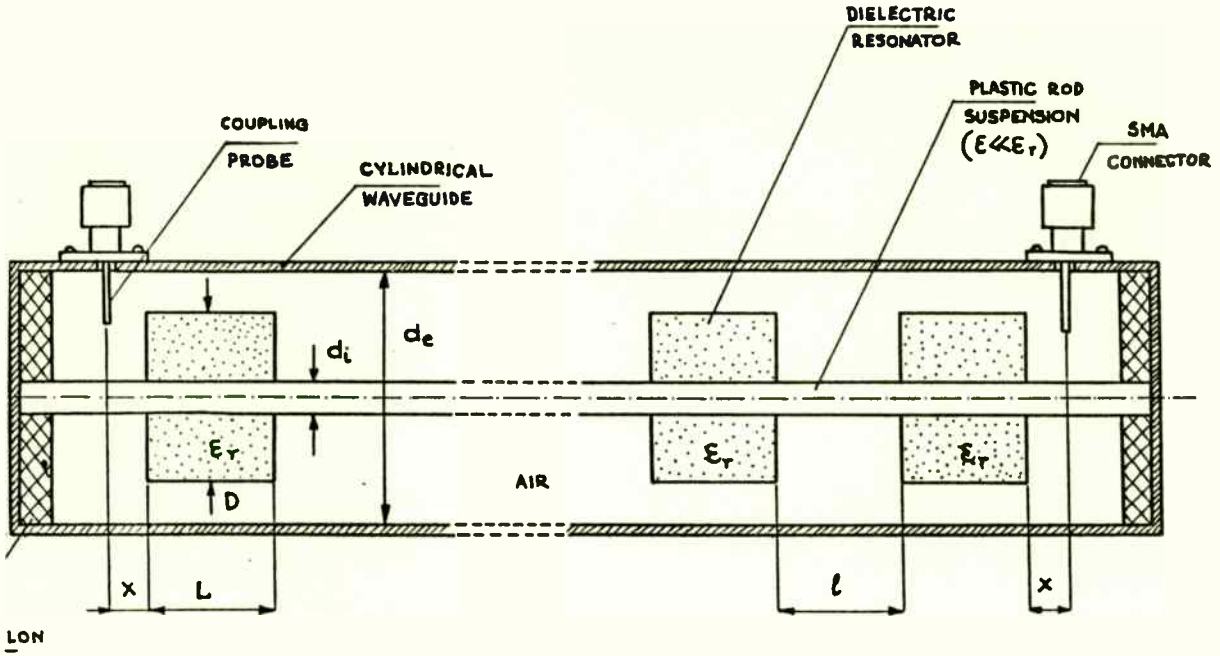

FIG. 5

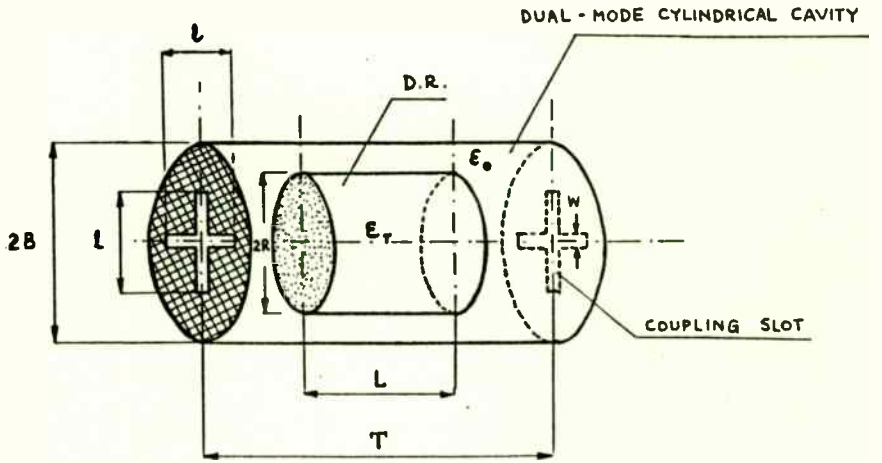

FIG. 6

C_P and L_{INT} and their relative reactances compared to that of C_J. Furthermore, since the point of measurement and diode reference plane are separated by a line with finite loss, the resulting *lossy line transformation* (see Chapter VI, Equation (VI-2)) must be taken into account when R_F and/or R_R are small ($< 2\%$ of Z_0) as is usually the case. This requirement necessitates a computer program to reduce the data if such measurements are to be made routinely.

Diode Inductance Measurements and Definitions

It should be noted that values measured for diode impedances depend to some extent on the test fixture – especially with inductive reactance, which can *only* be specified in terms of a return path. For example, the inductance per unit length of coaxial line having an outer conductor diameter, b, and an inner conductor diameter, a, is [9]

$$L = \frac{\mu_0}{2\pi} \ln \frac{b}{a} \tag{II-47}$$

and the characteristic impedance Z_0 is [9]

$$Z_0 = \frac{1}{2\pi} \sqrt{\frac{\mu_0}{\epsilon_0}} \ln \frac{b}{a} \tag{II-48}$$

For 50 Ω, the ratio b/a equals 2.3 for air dielectric coax. Suppose a packaged diode having 2.5 mm (0.1 in) length and effective diameter, a of 1.25 mm (0.05 in), is first measured under forward bias in a 50 Ω line having b equal to 15 mm (0.6 in); the inductance is 0.62 nH. If, however, the same measurement is performed using a smaller diameter 50 Ω coaxial line in which b equals 7.5 mm (0.3 in), the inductance is 0.45 nH.

Not only the absolute circuit dimensions but also the reference plane definition affects the inductance determination. For example, the above determination of inductance corresponds to reference plane A selection in Figure II-20. If, however, reference plane B were selected – by replacing with an equivalent length of center conductor to obtain a short circuit measurement reference – *insertion impedance* would be obtained. Insertion impedance is Z_L less the Z_S of the short circuit terminated length of the measurement line, ℓ, neglecting line loss

$$Z_S = jZ_0 \tan\left(\frac{2\pi\ell}{\lambda}\right) \tag{II-49}$$

where λ = wavelength at test frequency.

If, as is usually the case, $2\ell < \lambda$, the value of the tangent term can be replaced by its argument (within 3%). Furthermore, Z_S is an inductive reactance ($j2\pi fL_S$); for a coaxial line

$$\begin{aligned} L_S \text{ (nanohenries)} &\approx 0.0033 \cdot \ell \text{ (millimeters)} \cdot Z_0 \text{ (ohms)} \\ &\approx 0.084 \cdot \ell \text{ (inches)} \cdot Z_0 \text{ (ohms)} \end{aligned} \tag{II-50}$$

For the example cited, ℓ = 2.5 mm, L_S = 0.41 nH, and the diode respective *insertion inductance** values determined from measurements in the two line sizes is 0.21 and 0.04 nH respectively.

These examples highlight the importance, especially for inductance measurements of specifying both the measurement fixture and reference plane selection. Similar reasoning indicates that if the actual circuit of use does not duplicate these conditions – and usually it doesn't – calculations of performance sensitive to inductance will be inaccurate unless the new conditions are taken into account.

C. High RF Power Limits

1. Forward Biased Limits

Under forward bias the PIN diode chip usually has an RF resistance of 1 Ω or less. Failure of the diode in this bias state will occur if the dissipative heating (I^2R_F) is sufficient to cause the diode temperature to rise sufficiently to induce metallurgical changes. For silicon and its dopants, this point is not reached until a temperature of about 1000°C. However, the metal contacts at the silicon boundaries introduce failure mechanisms in the vicinity of 300-400°C, at which temperatures common contact metals form eutectic alloys with silicon. For example, the gold-silicon eutectic occurs at 370°C [16]. Repeated or continuous exposure of silicon to the eutectic temperature in the presence of the corresponding metal can produce conducting filaments of metal-silicon alloy, which eventually "grow" across the I region of a PIN diode, short circuiting it. This structural change of the diode crys-

*Also sometimes called *excess inductance*.

tal is the most common diode failure mechanism with heat, even with reverse breakdown induced failures, described subsequently.

Failure of a diode does not occur instantaneously when an over stress is applied unless the resulting temperature greatly exceeds 300°C, as can occur with filamentry heating produced by avalanche breakdown in the reverse bias condition. This situation is also discussed subsequently. Except for the rapid failure induced by avalanche breakdown, thermally produced failures proceed over a time period related to the ratio of the operating temperature, T, to that which causes near instantaneous burnout. Rather extensive experiments carried out on computer diodes have shown that the mean time to failure can be described by the empirical relationship [15] given by Equation (II-51)

$$t_M(T) = \Lambda e^{+Q/kT} \qquad \text{(II-51)}$$

where $t_M(T)$ = the mean time to failure at operating temperature T

Λ = a constant

Q = the "activation energy" constant

k = Boltzmann's Constant

T = the average device temperature in Kelvin (= °C + 273)

This expression is called the Arrhenius Law. It can be applied when the variation of operating life with temperature is determined by *only one* failure mechanism – for example, the formation of a particular alloy of the metallization system with the silicon.

To apply this relationship, the failure temperature, T_F, is first determined for the diode type; it depends on the semiconductor material (usually silicon for a PIN) and the metallization system. Next the device is operated at a lower temperature for a period until 50% of the samples under test fail, establishing a data point along the temperature-time graph. Additional data points at different temperatures are determined to allow for averaging of experimental data. This process, called *step-stress temperature testing*, is time-consuming because data points corresponding to hundreds and thousands of operating hours are required if the failure curve is to be established with sufficient accuracy to permit meaningful extrapolation to long life operation – on the order of years.

Care must be exercised that only the common *thermal* failure mode applies throughout the step stress tests. Careful analysis, usually including sectioning of failed diodes, is required to confirm the failure mode of each diode specimen used to establish the failure curve. The resulting temperature-time data plotted on semi-log paper form a straight line, permitting extrapolation for longer periods. Figure II-22 shows a typical plot for a surface-glass passivated; mesa type, high voltage PIN diode used in a phased array application. Notice that with a 200°C junction temperature (often cited as a safe operating limit for semiconductor devices) the anticipated mean life is 1000 hours (or 0.1 years), while for 140°C the anticipated mean life is extended to 1,000,000 hours (or 114 years). Accordingly the role of operating temperature must be given careful consideration if the estimate of anticipated life is to be meaningful.

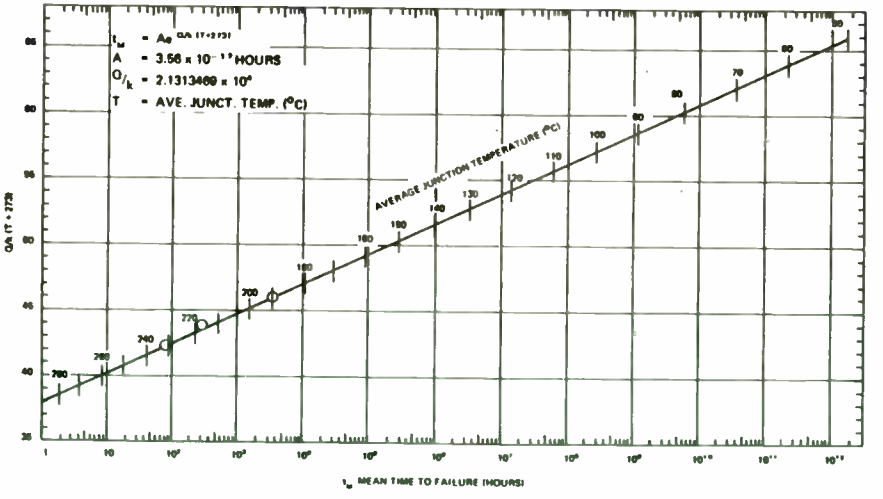

Figure II-22 PIN Life Expectancy vs. Temperature (Courtesy P. Ledger, Microwave Associates, Inc.)

UNDERSTANDING RF TRANSISTOR DATA SHEET PARAMETERS

Norman E. Dye
Motorola Semiconductor Products

INTRODUCTION

Data sheets often are the sole source of information about the capability and characteristics of a product. This is particularly true of RF transistors that are used throughout the world. Thus it is important that the user and the manufacturer of a product speak a common language, i.e., what the semiconductor manufacturer says about a transistor is understood fully by the circuit designer.

This paper reviews RF transistor parameters from maximum ratings to functional characteristics. Comments are made about critical specifications, about how values are determined and what are their significance. A brief description of the procedures used to obtain impedance data and thermal data is set forth. The importance of test circuits is elaborated. Finally, comments are made about possible tradeoffs in device specifications and their importance to the circuit design engineer.

DC SPECIFICATIONS

Basically RF transistors are characterized by two types of parameters: DC and functional. The "DC" specs consist (by definition) of breakdown voltages, leakage currents, hFE (DC beta) and capacitances, while the functional specs cover gain, ruggedness, noise figure, Zin and Zout. Thermal characteristics do not fall cleanly into either category since thermal resistance and power dissipation can be either DC or AC. Thus, we will treat the spec of thermal resistance as a special specification and give it its own heading called "thermal characteristics." Figure 1 is one page of a typical RF power data sheet showing DC and Functional specs.

Breakdown voltages are largely determined by material resistivity and junction depths (Figure 2). Each junction voltage - collector/base and emitter/base - is generally specified at a current level that is well within the safe operating limits of a reverse biased junction. The specifications are conventional and generally standard throughout the semiconductor industry.

Leakage currents (defined as reverse biased junction currents that occur prior to avalanche breakdown) are likely to be more varied in their specification and also more informative. Many transistors do not have leakage currents specified because they can result in excessive (and frequently unnecessary) wafer/die yield losses. Leakage currents arise as a result of material defects, mask imperfections and/or undesired impurities that enter during wafer processing. Some sources of leakage currents are potential reliability problems; most are not. Leakage currents can be material related such as stacking faults and dislocations or they can be "pipes" created by mask defects and/or processing inadequacies. These sources result in leakage currents that are constant with time and if initially acceptable for a particular application will remain so. They do not pose long term reliability problems. On the other hand, leakage currents created by channels induced by mobile ionic contaminants in the oxide (primarily sodium) tend to change with time and can lead to increases in leakage current that render the device useless for a specific application. Distinguishing between sources of leakage current can be difficult which is one reason devices for application in military environments require HTRB (high temperature reverse bias) and burn in testing. However, even for commercial applications where battery drain is critical or where bias considerations dictate limitations, it is essential that a leakage current limit be included in any complete device specification.

DC parameters such as hFE and Cob (output capacitance) need little comment. Typically, for RF devices hFE is relatively unimportant because the functional parameter of gain at the desired frequency of operation is specified. Note, though, that DC beta is related to AC beta (Figure 3). Functional gain will track DC beta particularly at lower RF frequencies. Generally RF device manufacturers do not like to have tight limits placed on hFE. Primarily the reasons that justify this position are:

a) Lack of correlation with RF performance
b) Difficulty in control in wafer processing
c) Other device manufacturing constraints dictated by functional performance specs which preclude specific limits for hFE.

A good rule of thumb for hFE is to set a maximum to minimum ratio of not less than 3 with the minimum hFE value determined by an acceptable margin in functional gain.

Output capacitance is an excellent measure of comparison of device size (base area) provided the majority of output capacitance is created by the base-collector junction and not parasitic capacitance arising from bond pads and other top metal of the die. Remember that junction capacitance will vary with voltage (Figure 4) while parasitic capacitance will not vary. Also, in comparing devices, one should note the voltage at which a given capacitance is specified. No

2. Reverse Biased Limits

The reliability criteria apply for reverse biased operation as just discussed for forward bias. The junction temperature is again the result of ambient and RF heating. Unlike the forward biased condition, however, the fractional RF insertion loss does not remain nearly constant once the applied RF voltage has a magnitude which is comparable to either the reverse bias and/or the diode's reverse breakdown voltage. Under these conditions diode dissipation (is nonlinear and increases more rapidly than RF power, producing at times a runaway insertion loss). The onset of this rapidly increasing insertion loss nonlinearity can be used as a practical measurement that the destructive temperature has been reached in the reverse biased state, since diode failure usually occurs if the incident RF power level is increased much beyond this level. Figure II-23 shows a typical insertion loss versus RF power characteristic obtained with a reverse biased diode phase shifter. The mechanisms of reverse biased diode failure under RF voltage stress are

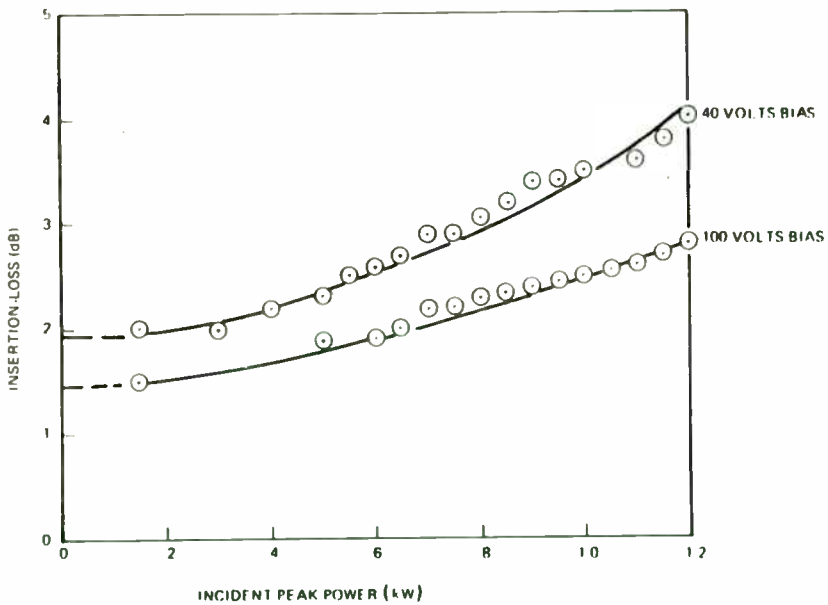

Figure II-23 Insertion Loss vs. Peak Power for a 4 Bit X-Band Phase Shifter Under Reverse Bias in All Bits (Phase Shifter Described in Chapter IX, pp. 470-475)

not sufficiently evaluated for a definitive theory to be developed, largely because of the difficulty of performing such measurements, with enough samples to have adequate statistical data. Qualitively, two conditions in which I region charge is generated occur and which one predominates depends, as described in Figure II-24, upon the relative magnitudes of the peak RF voltage, V_P; the bias voltage, V_{BIAS}; and the diode breakdown voltage, V_{BD}, as described in Figure II-24.

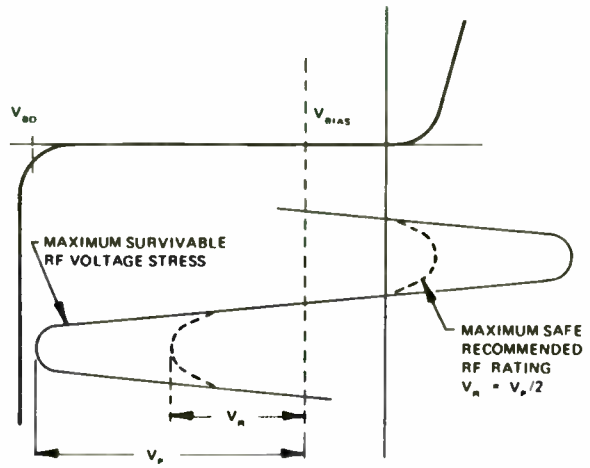

Figure II-24 Operation at High RF Voltage and Reverse Bias

The condition shown in Figure II-24 with voltage, V_P, is representative of typical operation near the failure limit. The RF voltage has a large excursion into the forward direction. Although, as has been shown earlier, the duration of this half cycle is insufficient to result in conduction by the diffusion transit (injection) of P region holes and N region electrons across the I region, *some charge* is introduced into the I region from these boundaries, and not all of it is extracted by the combined action of the reverse bias and

industry standard exists. The preferred voltage at Motorola is the transistor Vcc rating, i.e., 12.5 volts for 12.5 volt transistors and 28 volts for 28 volt transistors, etc.

MAXIMUM RATINGS and THERMAL CHARACTERISTICS

Maximum ratings (shown for a typical RF power transistor in Figure 5) tend to be the most frequently misunderstood group of device specifications. Ratings for maximum junction voltages are straight forward and simply reflect the minimum values set forth in the DC specs for breakdown voltages. If the device in question meets the specified minimum breakdown voltages, then voltages less than the minimum will not cause junctions to reach reverse bias breakdown with the potentially destructive current levels that can result.

A maximum rating for power dissipation (Pd) is closely entwined with thermal resistance (θjc). Actually maximum Pd is in reality a fictitious number - a kind of figure of merit - because it is based on the assumption that case temperature is maintained at 25 degC. However, providing everyone arrives at the value in a similar manner, the rating of maximum Pd is a useful tool with which to compare devices.

The rating begins with a determination of thermal resistance - die to case. Knowing θjc and assuming a maximum die temperature, one can easily determine maximum Pd (based on the previously stated case temperature of 25 degC). Measuring θjc is normally done by monitoring case temperature (Tc) of the device while it operates at or near rated output power (Po) in an RF circuit. The die temperature (Tj) is measured simultaneously using an infra-red microscope (see Figure 6) which has a spot size resolution as small as 1 mil in diameter. Normally several readings are taken over the surface of the die and an average value is used to specify Tj.

It is true that temperatures over a die will vary typically 10-20 degC. A poorly designed die (improper ballasting) could result in hot spot (worst case) temperatures that vary 40-50 degC. Likewise, poor die bonds (see Figure 7) can result in hot spots but these are not normal characteristics of a properly designed and assembled transistor die.

By measuring Tc and Tj along with Po and Pin - both DC and RF - one can calculate θjc from the formula

$$\theta_{jc} = \frac{T_j - T_c}{P_{in} - P_o}$$

Typical values for an RF power transistor might be Tj=130 degC; Tc=50 degC; VCC=12.5 V; Ic=12 A; Pin (RF)=10 W; Po (RF)=80 W. Thus

$$\theta_{jc} = \frac{130 - 50}{10 + (12.5 \times 12) - 80} = \frac{80}{80} = 1\ ^\circ C/W.$$

Several reasons dictate a conservative value be placed on θjc. First, thermal resistance increases with temperature (and we realize Tc=25 degC is NOT realistic). Second, Tj is not a worst case number. And, third, by using a conservative value of θjc, a realistic value is determined for maximum Pd. Generally Motorola's practice is to publish θjc numbers approximately 25% higher than that determined by the measurements described in the preceding paragraphs, or for the case illustrated, a value of θjc=1.25 degC/W.

Now a few words are in order about die temperature. Reliability considerations dictate a safe value for an all Au (gold) system (die top metal and wire) to be 200 degC. (1) Once Tj max is determined along with a value for θjc, maximum Pd is simply

$$P_{D(MAX)} = \frac{T_{J(MAX)} - 25^\circ C}{\theta_{jc}}.$$

Specifying maximum Pd for Tc=25 degC leads to the necessity to derate maximum Pd for any value of Tc above 25 degC. The derating factor is simply the reciprocal of θjc!

Maximum collector current (Ic) is probably the most subjective maximum rating on RF transistor data sheets. It can, and is, determined in a number of ways each leading to different maximum values. Actually three possible current limitations can exist in RF transistors. One is package related; one is wire related; and a third is die related. Most older, lower frequency transistors are wire and/or package limited which is why these parts generally have Ic max determined by the current handling capability of the emitter wires or by dividing maximum Pd by collector voltage (or by BVCEO for added safety). Most higher voltage parts (28V and 50V) tend to be wire limited and when operated at lower voltage can safely handle sizeable amounts of current. Lower voltage parts (7.5V and 12.5V), however, tend to be package limited and should have Ic max determined by power dissipation considerations.

(1)For a more thorough discussion of die temperature, θjc and reliability the reader is referred to "Thermal Rating of RF Power Transistors" by Robert Johnsen, Motorola Appl. Note #790

the negative-going half of the RF cycle before the next forward-going RF voltage excursion. However small the magnitude of the injected charge may be, it can increase multiplicatively with each succeeding RF cycle through *impact ionization*; electron-hole pair production results when mobile carriers accelerated by the high RF field strike silicon atoms in the I region lattice with sufficient energy to promote valence band electrons to the conduction band. This cause of increased insertion loss can be identified experimentally by its bias voltage dependence. Increasing the magnitude of reverse bias voltage sweeps such injected charge out of the I region more effectively and thereby extends to a higher applied RF voltage the onset of rapid insertion loss increase, which precedes what, for present purposes, is called the *injection mode* failure mechanism.

The second mechanism causing nonlinear insertion loss is the *direct impact-ionization mode*, occurring when the combined RF + bias voltage exceeds the diode bulk breakdown, i.e, $V_P + V_{BIAS} > V_{BD}$. In this case no partial injection is needed to initiate impact ionization; the requisite electron-hole pairs are obtained directly by high electric field ionization of I region silicon atoms. One might think this mechanism would be eliminated by reducing the bias voltage, since this action would reduce the combined magnitude ($V_{BIAS} + V_P$); but, in most practical cases, where the bias is 10-20% of V_{BD}, reduction of V_{BIAS} would only precipitate the injection-mode failure. An exception, of course, is when the bias is kept at half the breakdown (i.e., $V_{BIAS} = V_{BD}/2$). Then the RF waveform makes no injecting excursion into the forward direction. But for high power switching applications, a driver circuit to accomplish this end requires prohibitively high voltage transistors (500 V or more); the overall expense of the RF control circuit with driver could be more readily reduced by using a larger number of PIN diodes operated with less RF voltage stress.

Practically, the maximum sustainable RF voltage, V_P must be determined by measurement. Taking high power loss data for the diode – RF frequency, pulse length, and duty cycle of intended use – is the most direct and effective technique. In no case can $V_P + V_{BIAS}$ exceed V_{BD}, where V_{BD} is the bulk breakdown voltage of the diode.* The bias voltage is selected to be as large as is possible in a practical driver circuit (usually 10-20% of the diode's reverse bulk breakdown voltage) and the RF power level (from which the corresponding voltage, V_P, can be calculated) is set at the point at which a statistical sample of diodes have been found to undergo rapid loss increase and/or failure. Failures due to either of the two modes described are usually evidenced by a permanent short formed by a conducting filament across the I region.

Most high power switching applications use the PIN diodes in a transmissive circuit with a matched load. Accordingly, failure or removal of the load, transmission line arcing, or any mechanism which affects the load match can result in a voltage reflection and possible RF voltage enhancement at the diode. Neglecting losses in the switching circuit and diodes, this reflection voltage enhancement can double the stress on the diodes. Such a condition, even if encountered only briefly, usually precipitates diode failure. Therefore it is good practice to rate the diode at a stress level $V_R \leq V_P/2$ (see Figure II-24) in order for the device to be able to survive such a total reflection. Since power is proportional to the square of voltage, *PIN diode devices should be rated at one-fourth or less of the power level at which, with matched load, they would be expected to undergo near instantaneous failure.* Even if provision has been made to minimize the likelihood of a totally reflecting load, consideration should be given to the following factors before opting a power safety factor of less than 4 to 1:

1) Diode failure is not an exactly reproducible event even with PIN's made by the same process within the same lot. A 2 to 1 variation in burnout is typical for a given process. Thus, a production run of diodes may have a considerably lower (or higher) burnout than experienced with a prototype test lot.
2) Most high power tests are conducted at room temperature while practical devices usually must perform at considerably higher temperature, reducing the power safety margin that is inferred from a room temperature test.
3) High power RF testing is often of short duration, an hour or less, due to the generally limited availability of high power testing facilities. However, semiconductor devices are usually expected to have useful lifetimes of years. Derating, according to Figure II-22, is necessary to accomplish long life.
4) PIN devices operated at or below one-fourth of their burnout power are typically found to be able to survive temporary driver failures wherein the high power RF signals are applied with the diodes at zero bias.

*See Chapter III for bulk breakdown voltage evaluation of practical diodes.

Most modern, high frequency transistors are die limited because of high current densities resulting from very small current carrying conductors and these densities can lead to metal migration and premature failure. The determination of Ic max for these types of transistors results from use of Black's equation for metal migration which determines a mean time between failures (MTBF) based on current density, temperature and type of metal. At Motorola, MTBF is generally set at >7 years and maximum die temperature at 200 degC. For plastic packaged transistors, maximum Tj is set at 150 degC. The resulting current density along with a knowledge of the die geometry and top metal thickness allows the determination of Ic max.

It is up to the transistor manufacturer to specify an Ic max based on which of three limitations (die, wire, package) is paramount. Note however the limitation depends to some extent on application. It is recommended that the circuit design engineer consult the semiconductor manufacturer for additional information if Ic max is of any concern in his specific use of the transistor.

Storage temperature is another maximum rating that is frequently not given the attention it deserves. A range of -55 degC to 200 degC has become more or less an industry standard. And for the single metal, hermetic packaged type of device the upper limit of 200 degC creates no reliability problems. However, a lower high temperature limitation exists for plastic encapsulated or epoxy sealed devices. These should not be subjected to temperatures above 150 degC to prevent deterioration of the plastic material.

FUNCTIONAL CHARACTERISTICS

Functional characteristics of an RF transistor are by necessity tied to a specific test circuit (an example is shown in Figure 8). Without specifying a circuit, the functional parameters of gain, reflected power, efficiency - even ruggedness - hold little meaning. Furthermore, most test circuits used by RF transistor manufacturers today (even those used to characterize devices) are designed mechanically to allow for easy insertion and removal of the device under test (D.U.T.). This mechanical restriction sometimes limits achievable device performance which explains why performance by users frequently exceeds that indicated in data sheet curves. On the other hand, a circuit used to characterize a device is usually narrow band and tunable. This results in higher gain than attainable in a broadband circuit. Unless otherwise stated, it can be assumed that characterization data such as Po vs frequency is generated on a point-by-point basis by tuning a narrow band circuit across a band of frequencies and, thus, represents what can be achieved at a specific frequency of interest provided the circuit presents optimum source and load impedances to the D.U.T.

Broadband, fixed tuned test circuits are the most desirable for testing functional performance of an RF transistor. Fixed tuned is particularly important in assuring everyone - the manufacturer and the user - of product consistency, i.e., that devices made tomorrow will be identical to devices made today.

Tunable, narrow band circuits have led to the necessity for device users and device manufacturers to resort to the use of "correlation units" to assure product consistency over a period of time. Fixed tuned circuits minimize (if not eliminate) the requirement for correlation and in so doing tend to compensate for the increased constraints they place on the device manufacturer. On the other hand, manufacturers like tunable test circuits because their use allows adjustments that can compensate for variations in die fabrication and/or device assembly. Unfortunately gain is normally less in a broadband circuit than it is in a narrow band circuit and this fact frequently forces transistor manufacturers to use narrow band circuits to make their product have sufficient attraction when compared with other similar devices made by competition. This is called "specsmanship." A good compromise for the transistor manufacturer is to use narrow band circuits with all tuning adjustments "locked" in place. In comparing functional parameters of two or more devices, then, the data sheet reader should be careful to observe the test circuit in which specific parameter limits are guaranteed.

For RF power transistors, the parameter of ruggedness takes on considerable importance. Ruggedness is the characteristic of a transistor to withstand extreme mismatch conditions in operation (which causes large amounts of output power to be "dumped" back into the transistor) without altering its performance capability or reliability. Many circuit environments particularly portable and mobile radios have limited control over the impedance presented to the power amplifier by an antenna, at least for some duration of time. In portables, the antenna may be placed against a metal surface; in mobiles perhaps the antenna is broken off or inadvertently disconnected from the radio. Today's RF power transistor must be able to survive such load mismatches without any effect on subsequent operation. A truly realistic possibility for mobile radio transistors (although not a normal situation) is the condition whereby an RF power device "sees" a worst case load mismatch (an open circuit, any phase angle) along with maximum Vcc AND greater than normal input drive - all at the same time. Thus the ultimate test for

Generally PIN devices to control pulsed high RF power are limited in the reverse biased state by the maximum safe rated RF voltage stress, V_R, as is seen in the circuit discussions to follow. While a device which fails to meet circuit performance expectations may cause some user disappointment, it has been the author's observation that nothing quite equals the state of dissatisfaction resulting when solid-state control devices fail catastrophically due to overrating. No doubt it is for reasons such as this one that it has been industry practice in large phased array systems to design PIN phase shifters to survive operation into a short circuit load of any phase.

Only by carefully rating these devices can the good reliability which has come to be expected, indeed often assumed without question, of solid-state control be sustained. Accordingly, the designer should adopt as a minimum a policy of both designing diode control devices to sustain operation into a short circuit of any phase and testing throughout production to insure that this level, at least statistically, is maintained for the complete population of devices built.

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ruggedness is to subject a transistor to a test wherein Pin (RF) is increased up to 50% above that value necessary to create rated Po; Vcc is increased about 25% (12.5 V to 16 V for mobile transistors) AND then the load reflection coefficient is set at a magnitude of unity while its phase angle is varied through all possible values from 0 degrees to 360 degrees. Many 12 volt (land mobile) transistors are routinely given this test at Motorola Semiconductors by means of a test station similar to the one shown in Figure 9.

Ruggedness tests come in many forms (or guises). Many older devices (and even some newer ones) simply have NO ruggedness spec. Others are said to be "capable of" withstanding load mismatches. Still others are guaranteed to withstand load mismatches of 2:1 VSWR to ∞:1VSWR at rated output power. A few truly rugged transistors are guaranteed to withstand 30:1 VSWR at all phase angles (for all practical purposes 30:1 VSWR is the same as ∞ :1 VSWR) with both over voltage and over drive. Once again it is up to the user to match his circuit requirements against device specifications.

Then as if the whole subject of ruggedness is not sufficiently confusing, the semiconductor manufacturer slips in the ultimate "muddy the water" condition in stating what constitutes passing the ruggedness test. The words generally say that after the ruggedness test the D.U.T. "shall have no degradation in output power." A better phrase would be "no measurable change in output power." But even this is not the best. Unfortunately the D.U.T. can be "damaged" by the ruggedness test and still have "no degradation in output power." Today's RF power transistors consist of up to 1K or more small transistors connected in parallel. Emitter resistors are placed in series with groups of these transistors in order to better control power sharing throughout the transistor die. It is well known by semiconductor manufacturers that a high percentage of an RF power transistor die (say up to 25-30%) can be destroyed with the transistor still able to deliver rated power at rated gain, at least for some period of time. If a ruggedness test destroys a high percentage of cells in a transistor, then it is likely that a 2nd ruggedness test (by the manufacturer or by the user while in his circuit) would result in additional damage leading to premature device failure.

A more scientific measurement of "passing" or "failing" a ruggedness test is called Δ Vre - the change in emitter resistance before and after the ruggedness test. Vre is determined to a large extent by the net value of emitter resistance in the transistor die. Thus if cells are destroyed, emitter resistance will change with a resultant change in Vre. Changes as small as 1% are readily detectable with 5% or less normally considered an acceptable limit. Today's most sophisticated device specifications for RF power transistors use this criteria to determine "success" or "failure" in ruggedness testing.

Data sheets for low power RF transistors show such special characteristics as noise figure (NF), maximum available gain (GUmax) and scattering (S) parameters. "S" parameters are normally taken with the D.U.T. in a standard commercial fixture using a network analyzer such as the one shown in Figure 10. Typically these are given as functions of frequency and Ic. The measurements are routine and need no further comment.

NF and GNF likewise use commercial equipment such as the Eaton 4012 gain-noise analyzer or the HP8970A Noise Figure Meter. NF of a transistor will vary with input match and as a result is generally measured in a test fixture with input tuning. Usually data is given with a circuit tuned initially for lowest possible NF and then for a standard 50 ohm input. Measuring NF at 50 ohms Zin is more repeatable albeit not normally as low in value. The 50 ohm measurement is preferred for production testing because it requires no tuning and can be done with automated test equipment and for this reason is frequently the value specified on data sheets. Likewise, gain is normally specified for best NF conditions and for 50 ohms Zin.

RF power transistors are typically characterized by impedance parameters rather than small signal "S" parameters. Both Zin and Zout of a device are determined in a similar way, i.e., place the D.U.T. in a circuit and tune both input and output circuit elements to achieve maximum Po at the desired frequency of interest. At maximum output power, D.U.T. impedances will be the conjugate of the input and output network impedances. Thus, terminate the input and output ports of the test circuit, remove the device and measure Z looking from the device, first, toward the input to obtain the conjugate of Zin and, second, toward the output to obtain ZOL which is normally given as the load required to achieve maximum Po.

A network analyzer is used in the actual measurement process to determine the complex reflection coefficient of the circuit using, typically, the edge of the package as a plane of reference. A typical measurement setup is shown in Figure 11. Figure 12 shows the special fixture used to obtain the short circuit reference while Figure 13 illustrates the adapter which allows the circuit impedance to be measured from the edge of the package.

The entire impedance measuring process is somewhat laborious and time consuming since it must be repeated for each frequency of interest. Note that the frequency range permitted for characterization is that over which the circuit will tune. For other frequencies, additional test circuits must be designed and constructed, which explains why it is sometimes difficult to get a

PIN Diodes

Questions

1. What is the punchthrough voltage of a PIN diode having a 50μ (2 mil) I region width and I region resistivity of 300 Ω-cm?
2. What is the dielectric relaxation frequency of the PIN diode in Question 1?
3. What is the transit time of the PIN diode in Question 1?
4. If the PIN diode in Question 1 has an average carrier lifetime of τ = 2 μs, what is the microwave resistance of the I region, R_I, when a forward bias of 50 mA is applied?
5. For the conditions in Question 4 what is the value of R_I 1 μs, 10 μs, and 15 μs following the turn off of the forward bias? Neglect reactive effects and assume a constant lifetime of 2 μs, and that the forward bias had been on long enough to establish a steady state charge in the I region before turnoff.
6. If the diode in Question 5 has contact resistance of 0.2 Ω what isolation does it produce when it shunts a 50 Ω line with negligible inductance (SPST switch) with 50 mA bias? What is the isolation 1 μs, 10 μs, and 15 μs after the bias is turned off?

semiconductor manufacturer to supply impedance data for special conditions of operation such as different frequencies, different power levels or different operating voltages.

TRADEOFFS IN SPECIFICATIONS

Gain and ruggedness are the most obvious device parameters for compromise in RF power specifications. Devices with high gain - at least high with respect to their figure of merit (emitter periphery/base area) - tend to be fragile, i.e., not rugged. By using higher resistivity material, material with a thicker epitaxial layer and/or increased values of emitter resistance, ruggedness can be enhanced at the expense of gain. Likewise to get higher gain, the user may be asked to accept lower collector/base breakdown voltages (BVCBO orBVCES and BVCEO) in order to reduce collector resistivity and thereby increase gain.

Transistors specified for operation at a high frequency can be used at a lower frequency to obtain increased gain but almost always such devices at the lower frequency of operation will be fragile. Again for RF power transistors, the user should be wary of unnecessarily specifying tight limits on hFE particularly when functional gain is a test parameter. Also tight leakage current specifications lead to high costs as a result of yield losses and, except where essential such as low power and power devices with bias, should be candidates as tradeoffs for better prices.

SUMMARY

Understanding data sheet specifications and what they mean can be a major asset to the circuit designer as he goes about selecting and using an RF transistor for his specific application. This paper has emphasized some unique data sheet parameters of RF transistors and has explained what these mean from the semiconductor manufacturer's point-of-view. It is hoped this effort will help the circuit engineer make his selection and use of transistors more efficient and effective.

The RF transistor is an unusually complex semiconductor device and difficult to fully characterize. Not all information about RF transistor characteristics has been explained in this paper. Nor can all be covered in a data sheet. The circuit design engineer should contact the device manufacturer for more detailed information whenever it is appropriate. Most if not all current manufacturers of RF transistors have extensive applications support for the express purpose of assisting the circuit designer whenever and wherever assistance is needed.

FIGURES

1. A PAGE FROM MRF646 DATA SHEET (2ND PAGE)
2. GRAPH OF BV VS DOPING LEVEL AND JUNCTION DEPTH
3. BETA VS FREQUENCY CURVE
4. CAPACITANCE VS REVERSE BIAS VOLTAGE CURVE
5. A PAGE FROM MRF646 DATA SHEET (FRONT PAGE)
6. PHOTO OF INFRA RED MICROSCOPE SETUP
7. X-RAY PHOTO OF DIE BONDED TO BED
8. PHOTO OF RF TEST CIRCUIT (MRF 646)
9. PHOTO OF FINAL TEST STATION
10. PHOTO OF NETWORK ANALYZER
11. PHOTO OF IMPEDANCE MEASUREMENT SETUP
12. PHOTO OF SPECIAL REFERENCE FIXTURE
13. PHOTO OF SPECIAL IMPEDANCE ADAPTER

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	BV_{CEO}	16	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	BV_{CES}	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	BV_{EBO}	4.0	–		Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	–	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	40	70	100	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}		90	125	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 45 W, I_C(Max) = 5.8 Adc, f = 470 MHz)	G_{pe}	4.8	5.4		dB
Input Power (V_{CC} = 12.5 Vdc, P_{out} = 45 W, f = 470 MHz)	P_{in}	–	13	15	Watts
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 45 W, I_C(Max) = 5.8 Adc, f = 470 MHz)	η	55	60		%
Load Mismatch Stress (V_{CC} = 16 Vdc, P_{in} = Note 1, f = 470 MHz, VSWR = 20:1, All Phase Angles)	ψ*	No Degradation in Output Power			
Series Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 45 W, f = 470 MHz)	Z_{in}		1.4 + j4.0		Ohms
Series Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 45 W, f = 470 MHz)	Z_{OL}**		1.2 + j2.8		Ohms

Notes

1. P_{in} = 150% of Drive Requirement for 45 W output @ 12.5 V
2. * ψ = Mismatch stress factor - the electrical criterion established to verify the device resistance to load mismatch failure. The mismatch stress test is accomplished in the standard test fixture (Figure 11) terminated in a 20:1 minimum load mismatch at all phase angles.
3. ** Z_{OL} - Conjugate of the load impedance into which the device output operates at a given output power, η, and frequency.

FIGURE 1–TYPICAL DC AND FUNCTIONAL SPECIFICATIONS

DESIGN CONSIDERATIONS FOR THE DEVELOPMENT OF INTERNALLY MATCHED FETs

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Abstract

This paper describes design considerations for the development of internally matched power GaAs FETs. Both power FET and matching circuit designs are discussed. Examples of single chip and multi-chip designs with power levels of up to 10 Watts in C-band and 2 Watts in Ku-band are presented.

1.0 INTRODUCTION

Over the last few years the challenges offered by high power FET design have been largely overlooked in favor of more glamourous projects on Monolithic Microwave Integrated Circuits (MMICs). Monolithic circuits have received a great deal of research funding and effort, and for some applications, MMICs are clearly the technology of choice, i.e., low cost satellite down converters and low power (.2 Watts) T/R modules for phased array radars; systems where the volume justifies the development costs. However, in many cases where high power is required or the volume required is low, and this is typical of microwave systems, the discrete power FET is the device of choice. For example, high power internally matched FETs are widely used in point to point microwave communications systems where they have replaced TWTAs because of superior reliability. In space, power FETs are currently used for some satellite down link applications and this use will grow as higher power, higher efficiency devices become available.

At MSC, a wide range of devices for these and other applications is under development in the 2-26 GHz range. In this paper, design considerations to optimize output power, efficiency and bandwidth will be discussed and illustrated with examples from current development projects.

2.0 POWER FET DESIGN

To achieve high power capability, a large number of gates must be connected in parallel. This can be accomplished with the simple interdigitated layout of a typical MSC FET shown in Figure 1, with such a layout comes the first problem facing a power FET designer. The FET is a three terminal device, thus any two sets of electrodes can be interconnected directly on the surface of the Gallium Arsenide (in Figure 1, the gate and drain electrode sets are connected) but the third electrode set cannot. It is this fundamental problem that has led to the wide diversity of designs throughout the industry. Some designers have elected to use air bridge or dielectric cross-

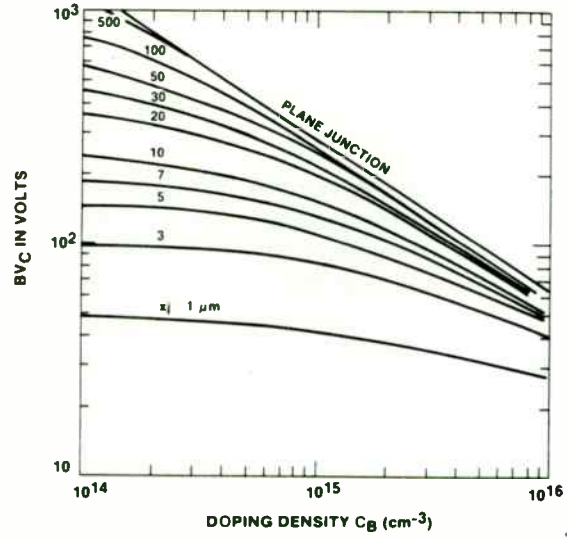


FIGURE 2–THE EFFECT OF CURVATURE AND RESISTIVITY ON BREAKDOWN VOLTAGE

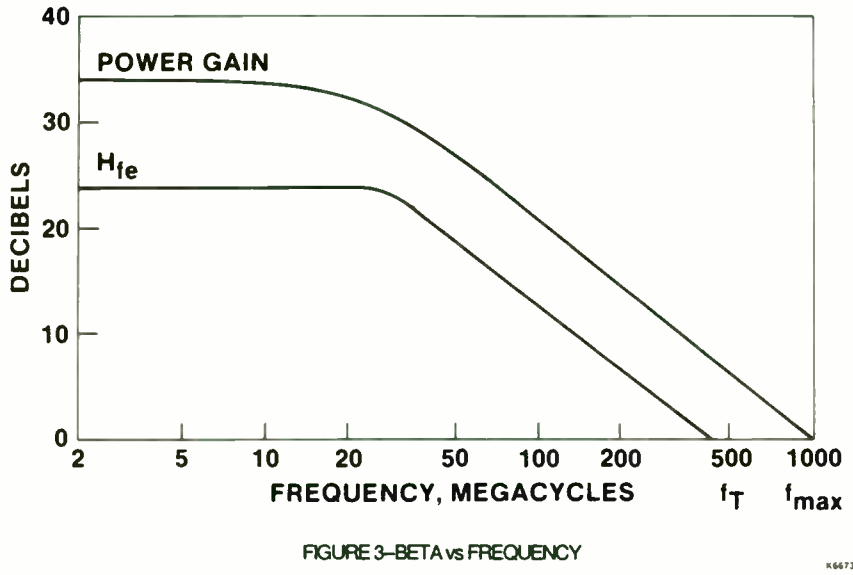


FIGURE 3–BETA vs FREQUENCY

K6673A

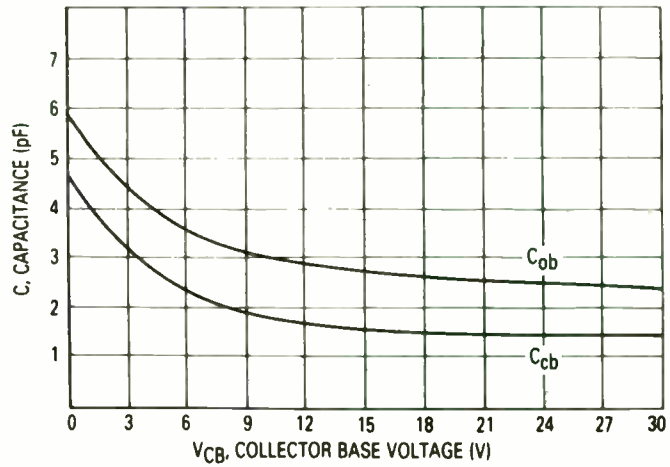
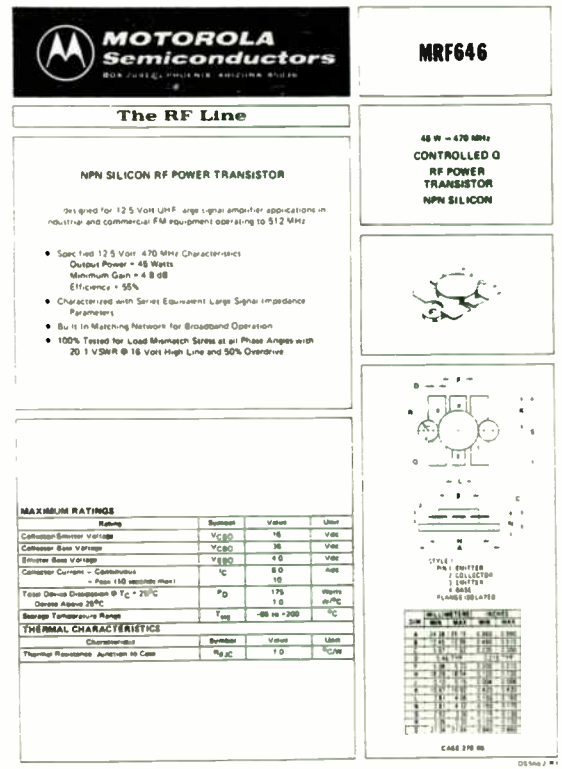


FIGURE 4–JUNCTION CAPACITANCE vs VOLTAGE


MOTOROLA Semiconductors

MRF646

The RF Line

NPN SILICON RF POWER TRANSISTOR

CONTROLLED Q RF POWER TRANSISTOR NPN SILICON

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	8.0	Adc
		10	
Total Device Dissipation @ T_C = 25°C	P_D	175	Watts
Derate Above 25°C		1.0	W/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Junction to Case	θ_{JC}	1.0	°C/W

FIGURE 5–TYPICAL MAXIMUM RATINGS OF AN RF POWER TRANSISTOR

overs to interconnect the third electrode, other have used a flip chip approach as shown in Figure 2, but the technique that is now becoming most widely adopted is the use of via hole connectors as shown in Figure 3.

Via hole technology has two significant advantages. It enables the source electrode to be grounded directly through the chip, thus ensuing a minimum parasitic source inductance and it results in an optimum thermal configuration. To form via holes with high yield, the GaAs wafer must be thinned to approximately 30 microns as shown in Figure 3. This minimizes the heat conduction path through the GaAs to the integral gold plated heat sink.

Having solved the source grounding and thermal design problems, the designer is next faced with choices concerning the number of gates to interconnect the individual width and length of these gates. The gate width and length are selected based on the desired frequency of operation. It is desirable to use the maximum gate width possible at a desired frequency to reduce the number of gates required and thus minimize the overall chip size. Because of losses along the gate which increase with frequency, the gate width is limited to approximately 500 microns at 4 GHz and 100 microns at 20 GHz. Similarly, it is desirable to use the minimum gate length consistent with high yield at a given frequency and in most power FET designs, 1.0 micron is chosen for up to 10 GHz operation and 0.5 micron for above 10 GHz.

The total gate width (number of gates x gate width) is chosen to achieve the desired output power based on 0.4 Watts/mm of gate width. However, as the total gate width is increased, the input and output impedances are reduced and the device becomes progressively more difficult to match. For very high power devices, a compromise between the difficulties of matching a large single chip versus matching and combining several smaller chips have to be investigated. For 10% bandwidth applications, it is feasible to design single chip devices with output powers in the 5 Watt range with total gate widths of up to 14mm, but for broad band applications, such as octave band ECM systems, the largest feasible devices are in the 1 Watt range.

Modern process lines for power FETs are highly automated, especially in the photolithography area where cassette to cassette equipment is used for the application and development of photoresists and for mask alignment. The most critical steps in the fabrication process are concerned with the gate formation. At MSC, two different types of FETs have been developed which differ only in the details of the gate cross section. One type is designed to operate at the conventional drain bias of 8-10 Volts, the other is designed to operate at 16 Volts. High voltage operation has advantages in the areas of improved linearity for communications systems and improved

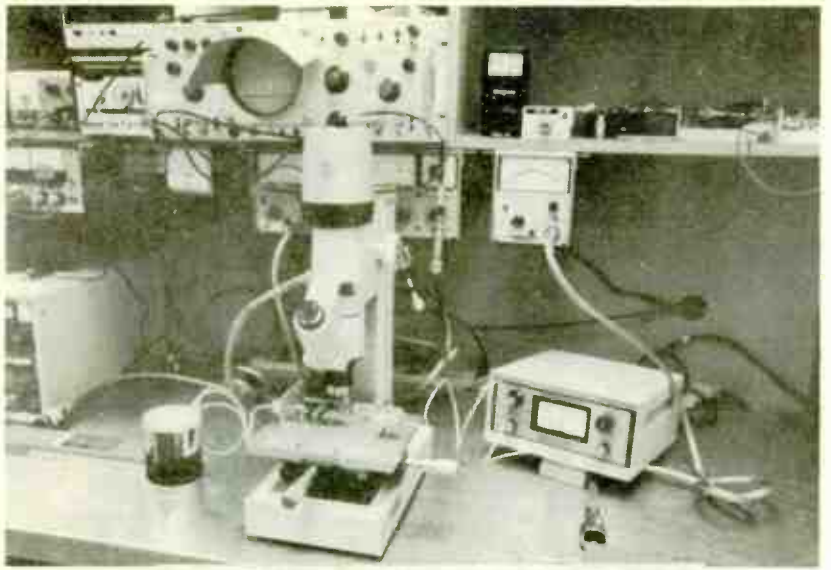


FIGURE 6–EQUIPMENT USED TO MEASURE DIE TEMPERATURE

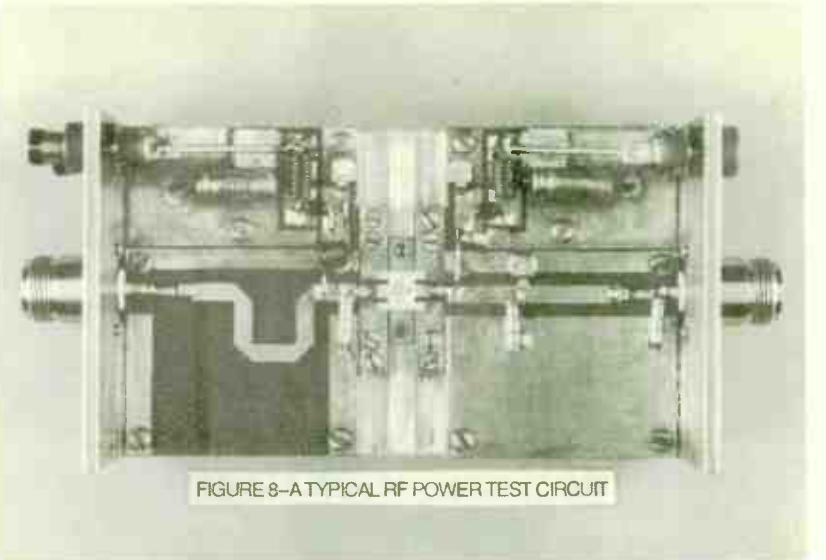


FIGURE 8–A TYPICAL RF POWER TEST CIRCUIT

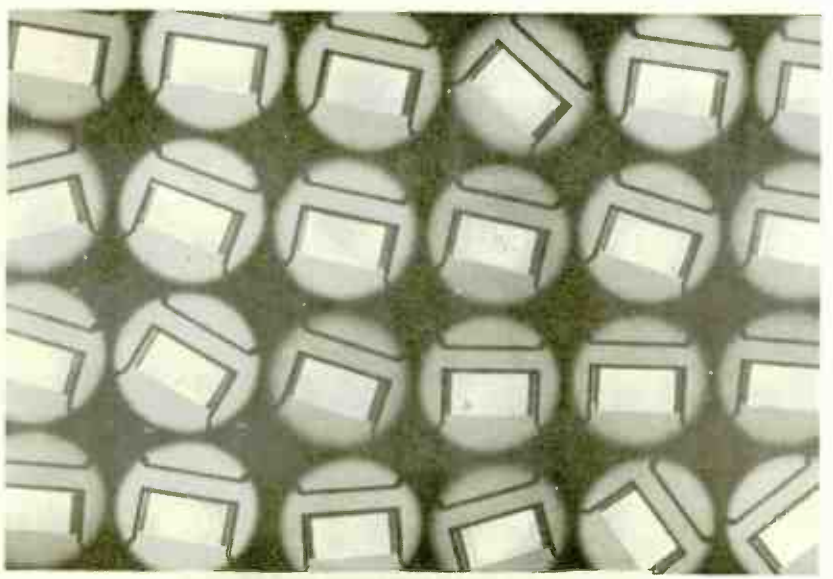


FIGURE 7–AN EXAMPLE OF INCOMPLETE DIE ATTACH

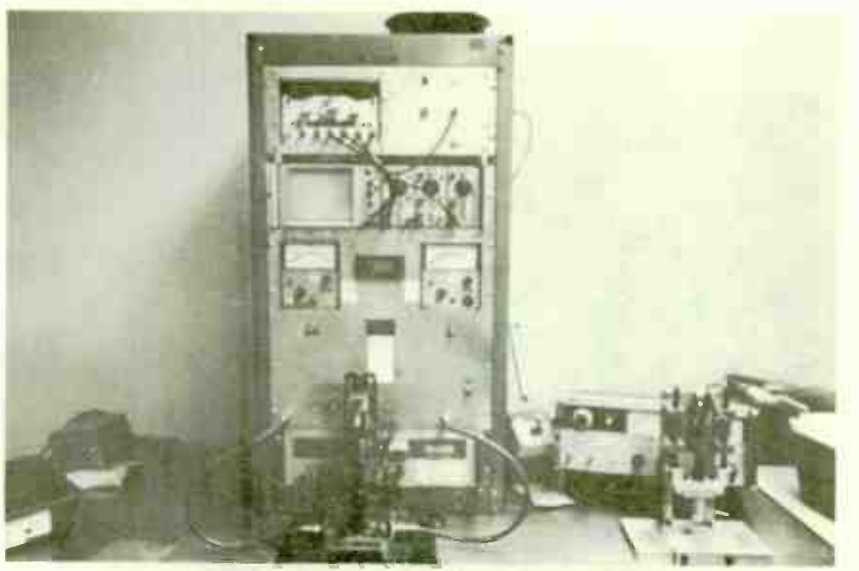


FIGURE 9–A TYPICAL FUNCTIONAL TEST STATION

efficiency in phased array radars. At higher voltage the I^2R losses in the feed to the array are significantly reduced and the conversion losses from the typical 28 Volts of airborne and satellite systems are also reduced. Although processing yields with highly automated lines can be extremely high, especially if the definition of the 1.0 micron or 0.5 micron gate is accomplished with direct write e-beam technology, (at MSC a Philips EBPG 4 system, which alone represents an investment of $2M is used for this function), overall yields are low because power FETs must operate at high current densities and voltages near breakdown where their performance is dominated by the quality of the GaAs materials. At MSC the GaAs layers are grown by vaper-phase-epitaxy and their quality and uniformity are carefully monitored using C-V analysis and DLTS (Deep Level Transient Spectroscopy).

3.0 MATCHING CIRCUIT DESIGN

In this section, designs of matching circuits for internally matched FETs are presented. Matching of the input and output impedances of a power FET to 50 ohms requires accurate small and large signal S-parameters and device modeling. The small signal S-parameters are measured using an HP8510 Network Analyzer. A good de-embedding procedure is required to obtain accurate S-parameters. Through-Short-Delay (TSD) is one such method being used to de-embedd the S-parameter at the chip level.

For design of the output matching circuit, it is important to obtain the large signal S-parameters. An automated load-pull technique is used to obtain the large signal output impedance. This technique uses a computer-controlled mechanical double slug coaxial tuner at the output of the FET to match the output impedance of the FET under large signal conditions. Load-pull contours for output power, gain and efficiency are obtained. The large signal output impedance for optimum output power, gain and efficiency is measured using an HP8510 network analyzer. At MSC an automated load-pull system operating in 2-26 GHz band is currently being used for the development of a range of internally matched power FETs.

Touchstone and Supercompact microwave circuit design CAD programs are used to design the input and output impedance matching circuits for the FET. The choice of circuit approach, and its implementation, must be considered while designing the input and output matching networks since the overall dimensions of the matching circuits are limited by the package dimensions. At C- and X-band a 12.9mm wide package is used while at Ku-band a 9.8mm wide package is used. At 20 GHz a .248" wide open carrier is used since a package for this frequency is not available at the present time.

Figure 4 is a Smith Chart representation of the design methodology for an internally matched FET. A two section low pass

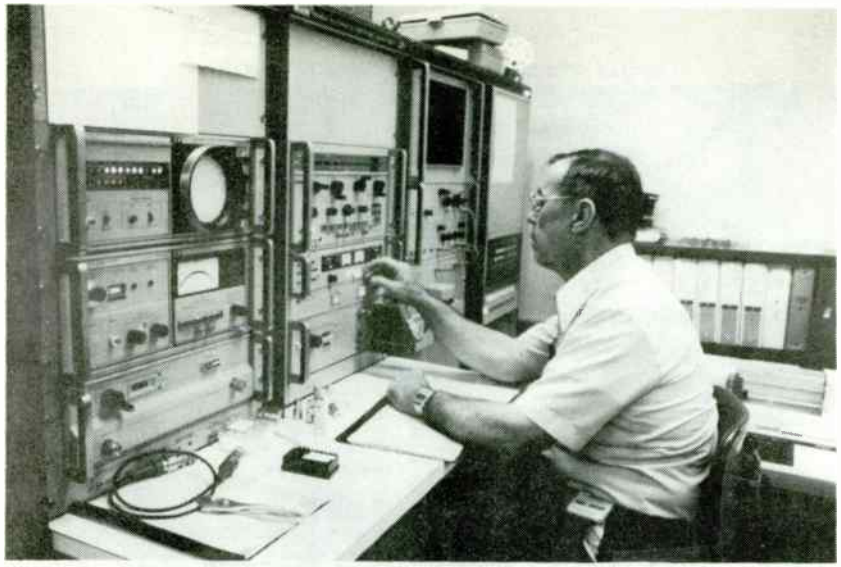


FIGURE 10–THE HP AUTOMATIC NETWORK ANALYZER

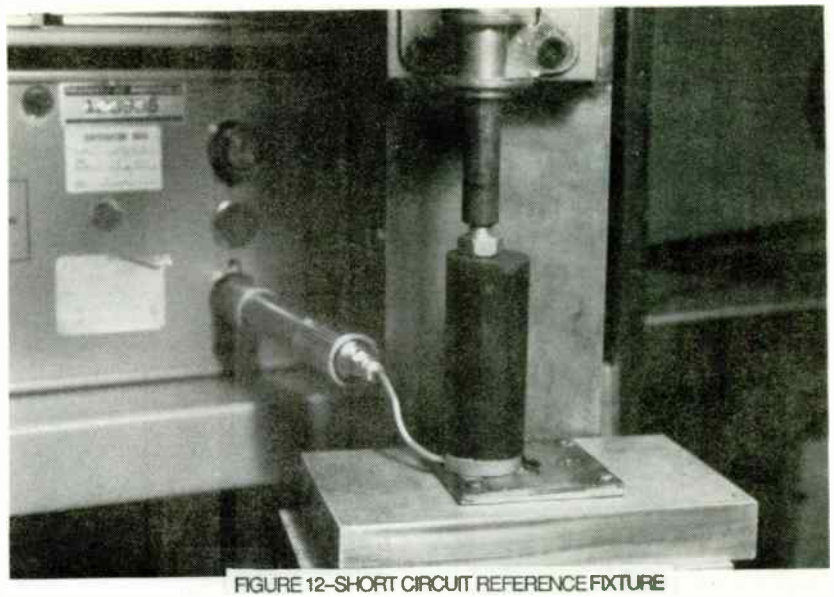


FIGURE 12–SHORT CIRCUIT REFERENCE FIXTURE

FIGURE 11–EQUIPMENT USED TO MEASURE DEVICE IMPEDANCE

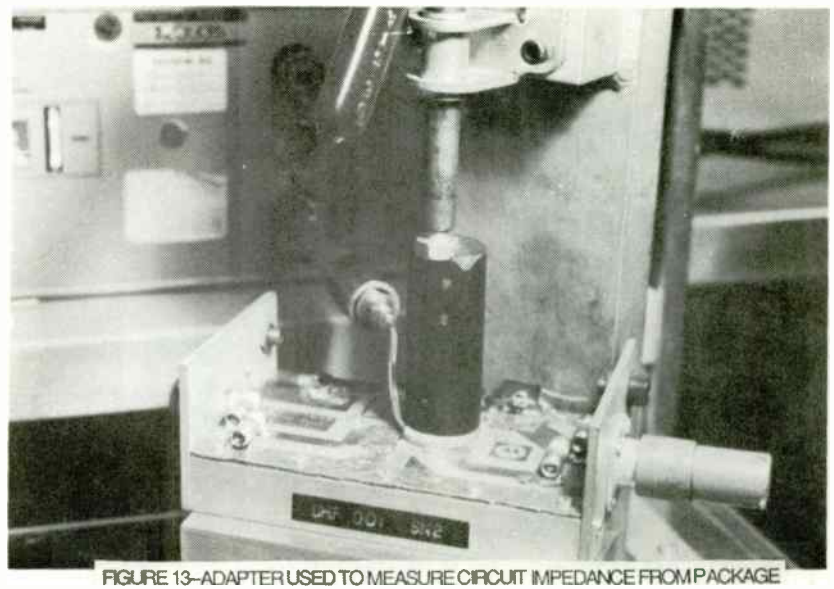


FIGURE 13–ADAPTER USED TO MEASURE CIRCUIT IMPEDANCE FROM PACKAGE

filter is used for matching the input and output impedances. Lumped element matching is used in C-band whereas distributed approach is used in Ku and K-band. A combination of lumped and distributed elements are used at X-band. Since the overall size of the matching circuit has to be small to fit the package, a high dielectric constant substrate, such as barium tetratinate with Er-38 is necessary in C-band, whereas the more conventional Alumina substrate material (Er=9.8) is used in X, Ku and K-bands. The thickness of the substrate is also a factor in determining the overall size of the input and output matching circuits. The width of the distributed microstripline is proportional to the thickness of the substrate. Use of thinner substrate reduces the overall dimension. However, loss in the circuit increases as the width of the line is reduced. Five and ten mil thick alumina substrates are used in Ku and K-band, while 5 mil thick Barium Tetratitanate substrate and 10-15 mil alumina substrates are used in C- and X-bands. The choice of substrate thickness depends on the impedance level of the FET. The input and output impedance of the FET fall with increases in output power. To obtain higher output power, larger gate peripheries and multiple chips are used. Thus, a trade-off is made between the thickness of substrate, the size of the overall matching circuit and the losses in the output matching network.

4.0 EXAMPLES OF INTERNALLY MATCHED GaAs POWER FETs

Several internally matched power FETs have been developed at MSC. 3 Watt and 10 Watt internally matched FETs operating over 3.7-4.2 GHz have been developed. Figures 5 and 6 show the variation of output power and third order intermodulation distortion (IMD_3) products as a function of input power for 3 and 10 Watt internally matched FETs, respectively. The gain and efficiency of the 3 Watt FET are 12dB and 40%. The 10 Watt internally matched FET exhibited 9dB gain and 30% efficiency.

Figure 7 shows the output power and efficiency variation as a function of input power for a high voltage internally matched FET. This FET operates at Vds = 16V and exhibited 14 Watt output power with 7.5dB gain and 29% efficiency at 5.3 GHz.

Table 1 shows the results for output power, gain and efficiency for an internally matched FET operating over 14.5-15.35 GHz band. An output power of 1 Watt with 6-7 dB gain and 20-25% efficiency has been obtained.

A 2 watt output power with 4-5 dB gain and 19% efficiency has been obtained over 17-18 GHz. Results for output power, gain, efficiency and return loss over 17-18 GHz are presented in Table 2.

PIN Diode Attenuators and Vector Modulators at Intermediate Frequencies

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The PIN Diode

A PIN diode differs from an ordinary detector or switching diode in that it has an extra layer of undoped or Intrinsic semiconductor sandwiched between the P and N doped layers normally found. When the device is reverse or zero biased this I layer is devoid of charge carriers and the diode has a very high AC resistance. With forward bias, carriers are injected into the I layer, the diode conducts and the AC resistance drops.

The key difference between the PIN diode and the ordinary PN diode is that the minority carriers in the I layer have a significant lifetime, and when this lifetime exceeds the period of an RF signal the normal rectification effects begin to be suppressed because the charges transferred in an RF cycle are less than the charge stored in the device.

When a PIN diode is used for switching a signal the forward bias current in the "on" state need not be as high as the peak RF current and the reverse voltage in the "off" state need not be as high as the peak RF voltage. This is a distinct advantage over the PN diode with no carrier storage but it is the behaviour of the PIN diode at intermediate bias states that makes it especially useful.

For small signals at RF frequencies the PIN diode appears essentially as a pure resistor. The exact resistance depends on the device construction but it is roughly inversely proportional to the bias current. Typically, a bias range of 1 μA to 10 mA might give RF resistances of 10K to 1 Ohms.

The quality of this resistance, ie., its linearity and lack of distortion products, can be very good indeed if the diode is used under the right conditions [1]. In practical terms this usually means ensuring that the minority carrier lifetime is at least 10 times the signal period and keeping to power levels of less than 0 dBm.

PIN diodes are available from several manufacturers and in a variety of packages, eg. for waveguide or stripline mounting, but for general purposes the most useful is the familiar in-line wire lead glass package. Figure 1 shaows the resistance characteristics of varous Hewlett Packard diodes [2]. Note that the 3080 and 3081 types show less linear control curves. They are, though, particularly useful devices as they have long carrier lifetimes, typically 1.3 μs and 2 μs respectively.

Matched Variable Attenuators

A simple attenuator can be made with a single series or shunt variable impedance element. This, however, is only a matched device at zero attenuation and is not necessarily suitable for the majority of applications. At microwave frequencies it is common to convert unmatched

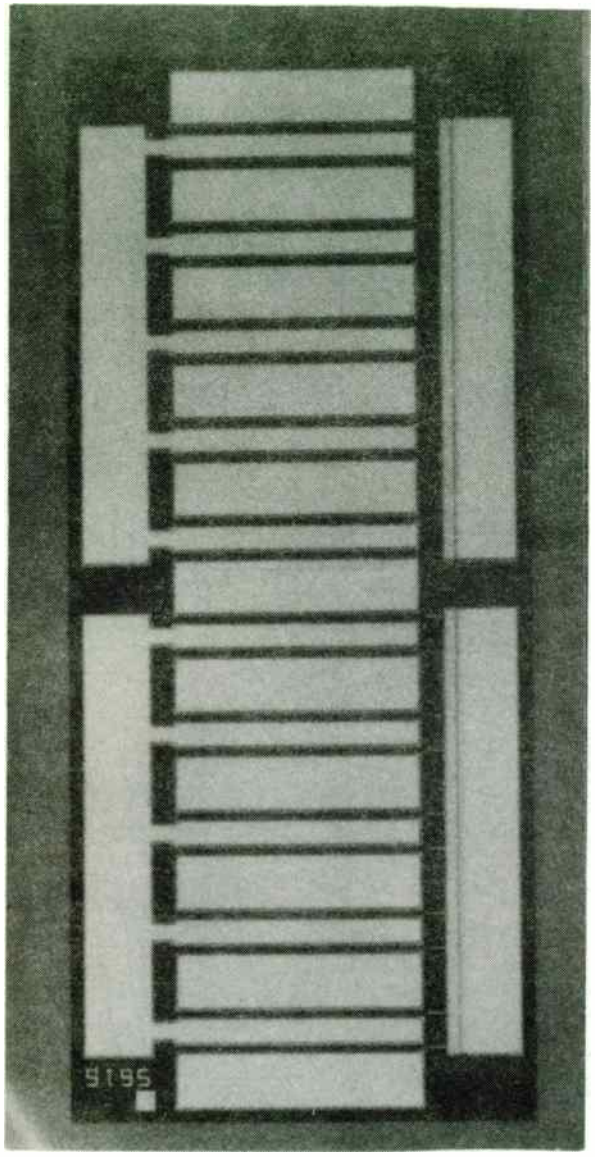
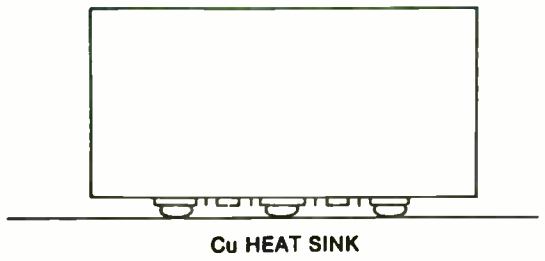


FIG. 1 Photograph of a typical MSC FET



FLIP-CHIP TECHNOLOGY

Fig. 2 Cross-section of a flip-chip FET

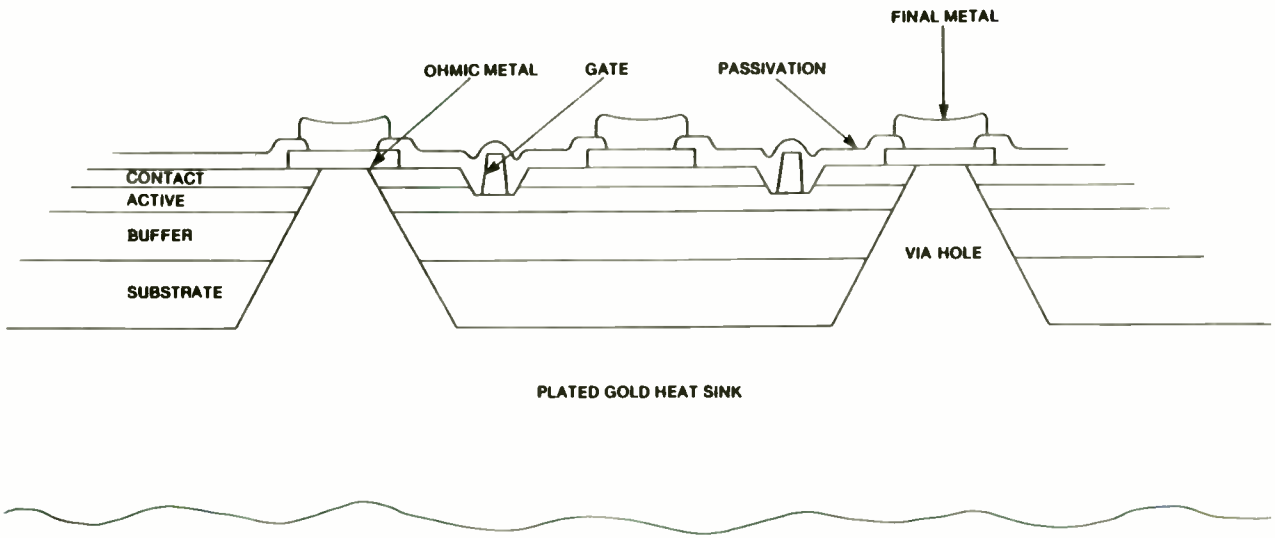


Fig. 3 Cross-section of a via-hole FET

circuits to matched by the use of quadrature hybrid couplers (Figure 2a), which are readily printable in stripline.

At lower frequencies hybrids are costly components and other matching techniques can be used. The bridged-tee, Figure 2b, and the pi, Figure 2c, attenuators are well known circuits capable of giving variable, matched attenuation over a wide bandwidth if the elements are controlled properly. The bridged-tee requires one less active element but the pi configuration is normally preferred for its higher maximum attenuation with typical components.

Practical Pi Attenuator Design

The series and parallel resistances, Rs and Rp, in the pi attenuator must be controlled simultaneously to ensure a good match as the circuit gain, G, is varied. The required resistances are given by

$$Rp = Z\left[\frac{1+G}{1-G}\right] \qquad Rs = \frac{Z}{2}\left[\frac{1}{G} - G\right]$$

and these equations can be used, together with published device data, to calculate the PIN diode bias currents required at various attenuation settings. Because of the nature of the diode characteristics, this procedure is bound to result in control curves that are extremely difficult to realise in practice. It also sheds little light on the performance deterioration to be expected when the curves are not followed exactly.

At this point, many workers might turn to an extensive computer simulation; this author, however, believes that this is a case where better and quicker results can be obtained from a simple set of measurements.

Figure 3 shows the circuit of a PIN diode pi attenuator in which the series and parallel bias currents, Is and Ip, can be varied independently. If this is connected to a network analyser capable of measuring return loss, $|S_{11}|$, and transmission, $|S_{21}|$, curves of constant return loss and attenuation can easily be plotted. A representative set is shown in Figure 4.

For a given specification on return loss, there is a certain operating area into which the pattern of bias currents must be fitted. The easiset control pattern appears as a straight line on the plot; this can be generated from a single supply with one control line as shown in Figure 5a.

In the case illustrated, though, 20 dB return loss has been chosen as the target and inspection shows that, within this restriction, a straight line control locus can only give a limited attenuation range. It is clear, though, that a locus of two straight lines, as drawn, will cover the full range. Two circuits for generating such a locus are given in Figure 5b and 5c. Both give the same pattern of bias currents but the control voltage vs. attenuation responses are different; one is better suited to percentage gain control, the other to dB attenuation systems.

The calculation of component values for these driver circuits is straightforward and will not be detailed here. For the case in question, the attenuator was to be driven from a D to A converter and it was desired to keep the fractional gain change per LSB as constant as possible over the whole attenuation range.

Figure 6 shows the final circuitused; a batch of eight of these were construted for signal levelling purposes in a phased arrary system.

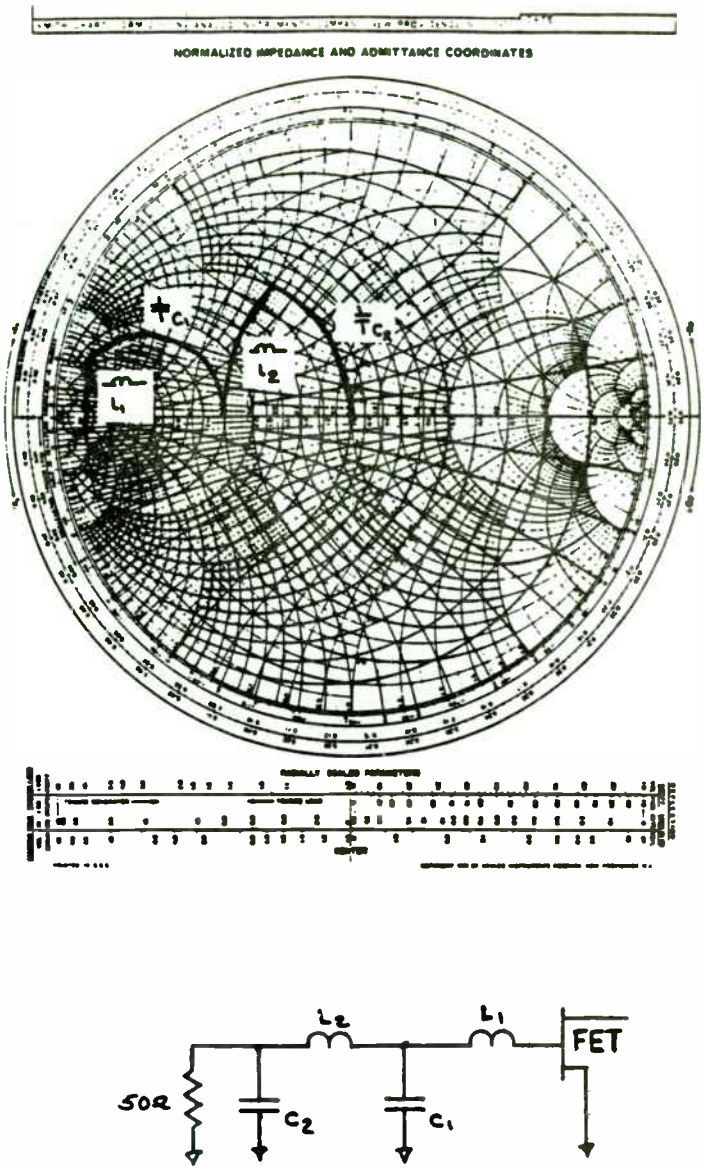


Fig. 4 Smith Chart representation of the design for an internally matched FET

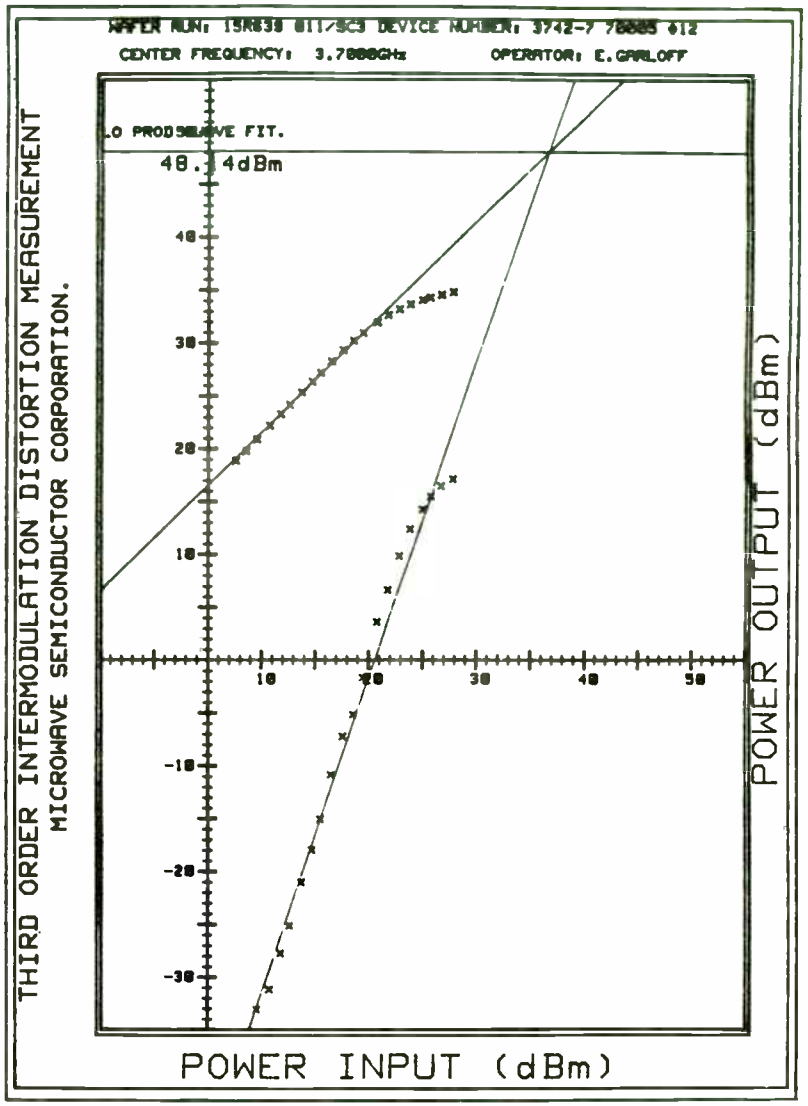


Fig. 5 Variation of output power and third order intermodulation distortion as a function of input power for a 3 Watt internally matched FET at 3.7 GHz

Figure 7 shows typical performance at 70 MHz. The control characteristic is reasonably linear; certainly the slope variations are small enough for 8 bit digital control to give consistently small step sizes of 0.5% or less. In this application the attenuator was to be used in a closed loop operation so absolute linearity or accuracy of the control was not a requirement; if this had not been the case, some further software linearisation could have been applied.

At low attenuations the input match worsens slightly. This is partly due to compromises made in the bias driver design and partly to stray reactances incurred by the layout and the connecting sockets.

The foregoing example shows how a wideband signal attenuator can be made with a minimum of components. Only one control line is needed and the driver circuit to achieve both a good match and reasonably linear control simultaneously is simple in the extreme.

Vector Modulators

In many applications, phase as well as amplitude control of a signal path is required. This might occur, for instance, in certain modulation systems, phased array processing or adaptive cancellation systems.

Standard phase shifter circuits employ switched line lengths, switched loaded lines etc., Figure 8. Variable reactance devices, such as varactors, can also be used but are limited to only small phase shifts. Switched systems can be cascaded to give phase shifters capable of covering the full 360 degrees in given step sizes. A disadvantage is that the phase settings are quantised and fine resolution demands many stages, which increases the insertion loss and potential inaccuracies. It should be noted that these systems are strictly delay inserters rather than pure phase shifters and wideband operation is not generally possible. Nevertheless, the use of cascaded phase shifters in conjunction with an attenuator does give full four quadrant control of the transmission characteristic. The controls are polar, ie., r and θ, or separate gain and phase adjustments.

In many cases it is more appropriate to combine the gain and phase control mechanisms into a single complex attenuator, or vector modulator. The basic scheme is shown in Figure 9. Full control of the transmission vector is possible but the controls in this case are cartesian, ie., x and y, or I and Q. If all four quadrants are to be covered bi-phase attenuators are required; these have a gain range of -1 to 1 rather than just 0 to 1. There is a 3 dB minimum theoretical loss through such a modulator; this, however, occurs only at certain phase settings, at others the minimum loss is 6 dB.

Despite this, the vector modulator is useful when fine or continuous adjustment is needed. It compares favourably with, for instance, a 6 or 8 bit phase shifter that may have up to 1 dB loss per bit.

Simple attenuators can be converted to bi-phase by the addition of a phase inverter, Figure 10a, or by offsetting half the signal, Figure 10b. The latter method offers easier control but has an inherent 6 dB loss; in the first arrangement it may be difficult to achieve zero transmission.

A better circuit is the hybrid coupler attenuator, versions of which appear in Figure 11. The input power is split between the two variable terminating resistances and the reflections from these terminations

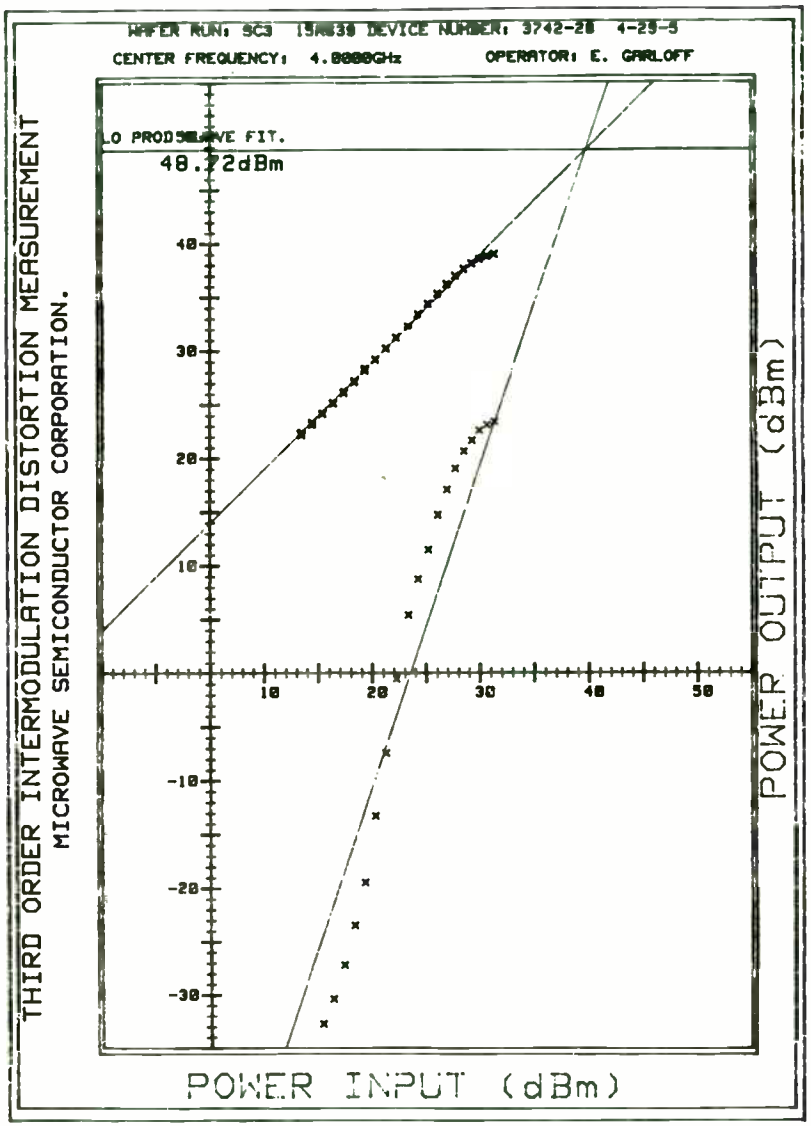


Fig. 6 Variation of output power and third order intermodulation distortion as a function of input power for a 10 W internally matched FET at 4 GHz

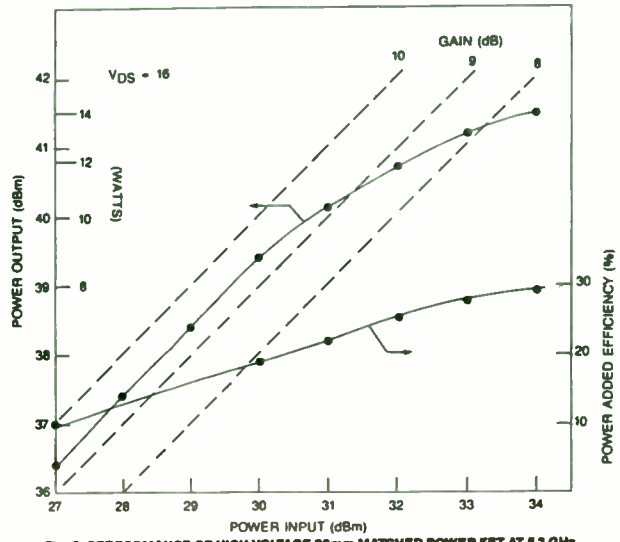


Fig. 7 PERFORMANCE OF HIGH VOLTAGE 28mm MATCHED POWER FET AT 5.3 GHz

TABLE 1. 14.5 - 15.35 GHz 1 WATT INTERNALLY MATCHED FET

Frequency (GHz)	Output Power @ G1dB (dBm)	Gain @ P1dB (dB)	Return Loss (dB)	Efficiency (%)
14.5	31	6	9.8	21
15.0	31.5	7.25	12	25
15.35	31	5.5	6	20

TABLE 2. 17 - 18 GHz 2 WATT INTERNALLY MATCHED FET

Frequency (GHz)	Output Power @ G1dB (dBm)	Gain @ P1dB (dB)	Return Loss (dB)	Efficiency (%)
17.0	33.5	4.7	10.5	19.3
17.5	33.2	4.7	25	18.5
18.0	33.5	4.0	14.6	18.1

cancel at the input port and add at the output. The depth of cancellation, and hence the input match, depends on the quality of the hybrid and how well the resistances track each other. Zero transmission, apart from hybrid leakage, occurs when the resistances are 50 Ohms; above or below this value transmission increases, with a phase reversal between the two regimes.

With PIN diodes as the variable elements the transmission vs. bias current response is parabolic rather than linear. Also, because of circuit imperfections and temperature effects, repeatable fine control around the zero transmission point may prove difficult. This type of attenuator is best suited to closed loop systems or those with regular calibration.

Any of these bi-phase attenuators can be used to make a four quadrant vector modulator but the hybrid attenuator, with single line control and low minimum loss, is probably the best, Figure 12. The bandwidth of such a circuit is determined by the quadrature hybrids used. It is interesting to note that the coupling network arrangement for this is exactly that found in the six-port network that is used for signal comparison and measurement [3]. This type of vector modulator has been used successfully at 750 MHz by the Independent Broadcasting Authority in Britain [4]. A version using a microwave printed stripline network has also been investigated at University College London and shown to give useful results over nearly an octave bandwidth.

A new variation is that shown in Figure 13; this is a method of extending a single bi-phase attenuator to give control of the quadrature transmission as well. No extra quadrature hybrids are required but with phase shifts provided by line lengths the bandwidth is limited. In the circuit shown the biasing arrangement is simplified by allowing the currents to flow to ground through the power dividers. Most bought in components of this type allow this but care must be taken to ensure that the currents do not saturate any ferrite devices inside.

This circuit, the Reflective Delay Line modulator, has been tried at UCL using commercial couplers at 70 MHz. The PIN diodes used were all HP 3080 types but were not specifically matched. Full cartesian control of the transmission vector was demonstrated; there were no missing sectors or regions of the coverage and because leakage in the couplers can be compensated by adjusting one or the other bias control the zero transmission point can always be accessed. The input return loss varied slightly with control settings but was about 20 dB over the whole range.

A further possibility would be to replace the quadrature hybrid with a 180 degree one and a quarter wave line; this would give an extremely economical four quadrant vector modulator.

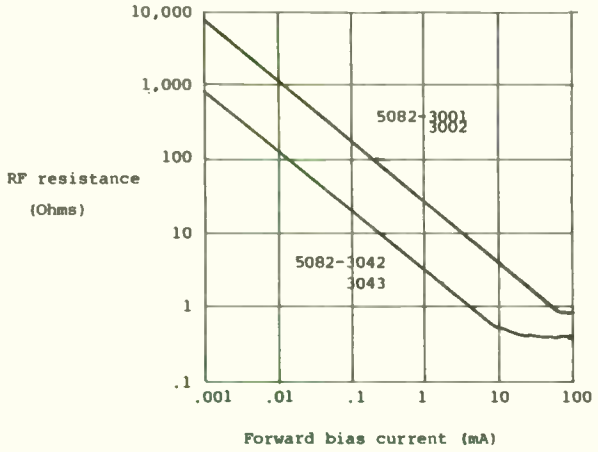
References

[1] "Rectification effects in PIN attenuators", Hewlett Packard Application Note 957-3.

[2] "Diode and Transistor Designer's Catalog", Hewlett Packard Data Book.

[3] A. L. Cullen, "The 6-port and the microprocessor in microwave measurements", Proc. European Microwave Conference 1980, pp74-82.

[4] H. J. O'Neill and B. V. W. Isaacs, "An adaptive cross-polar cancellation system for satellite communications employing dual polarisation frequency re-use", IEE Radio Spectrum Contraverbosity Techniques Conference, 1980, pp 137-141.



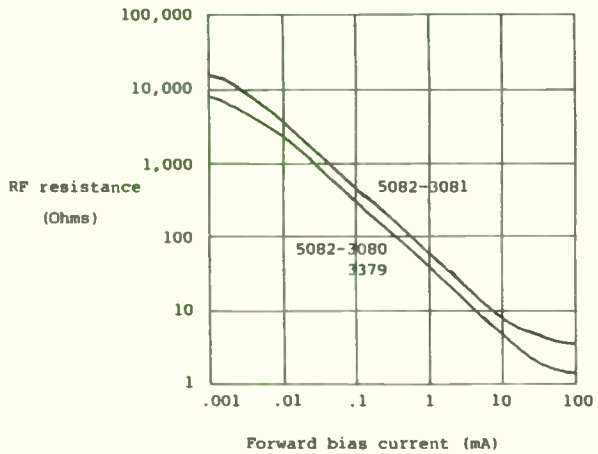


Figure 1: PIN diode RF resistances vs. current [2]

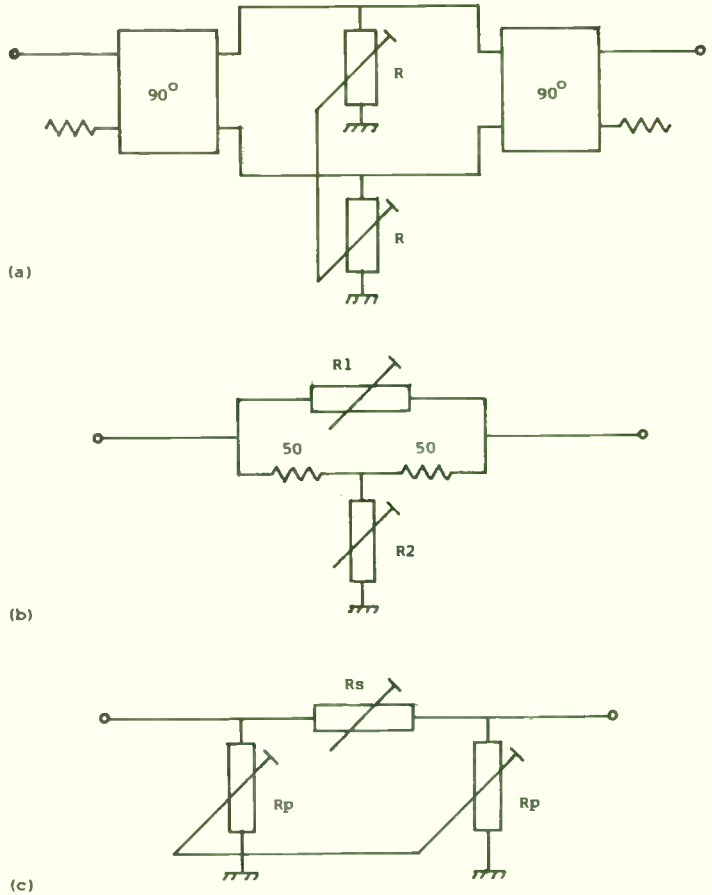


Figure 2: Attenuator configurations

LOW NOISE OSCILLATOR PAPER

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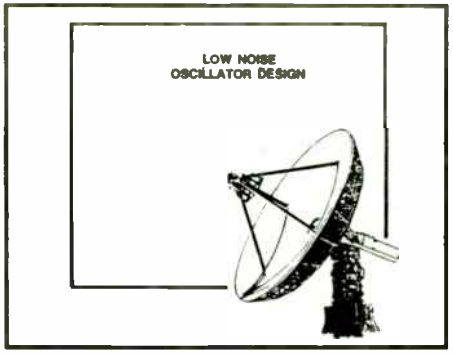


961

LOW NOISE OSCILLATOR DESIGN
- SPECTRAL PURITY
  - A. What is spectral purity in oscillators?
  - B. What determines spectral purity?
- LOW NOISE OSCILLATOR DESIGN
  - A. Establish objectives
  - B. Select a resonator
  - C. Select a circuit topology
  - D. Select an active device
  - E. Select matching network
  - F. Measure
- OSCILLATOR COMPUTER ANALYSIS
  - A. Open loop
  - B. Closed loop
- OTHER NOISE MECHANISMS
  - A. Spurious modes
  - B. Upconverted noise

962

SPECTRAL PURITY DEFINITIONS

$V(t) = \cos w_o t$

$V(w) = \delta(w_o) + \delta(-w_o)$

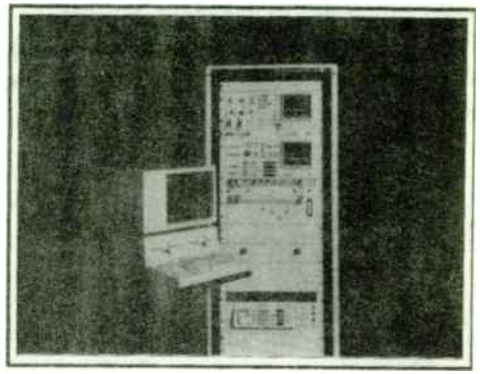
$V(t) = [1+e_n(t)] \cos [w_o t + \phi(t)]$

(AM Noise; PM Noise)

$\mathcal{L}(f_m) = \frac{\text{SSB Noise Power in a 1Hz Bw } f_m \text{ Hz from Carrier}}{\text{Total Signal Power}}$

$\mathcal{L}(f_m) = \frac{S\phi(f_m)}{4}$

964



963

Spectral Purity describes the degree of degradation from a perfect impulse in the frequency domain:

$$V(t) = \cos \omega_0 t$$

$$V(\omega) = \delta(\omega_0) + \delta(-\omega_0)$$

Real signals have some noise associated

$$V(t) = [1 + e_A(t)] \cos [\omega_0 t + \phi(t)]$$

We will focus primarily on phase noise (PM) components. $\mathcal{L}(f_m)$ describes the ratio of SSB power in a 1 Hz B.W. due to phase noise, offset f_m Hz, from the carrier, to the total signal power.

Ref. 2, 14, 15

This is a typical phase noise measurement. This oscillator uses a 832.5 MHz surface acoustic wave resonator as the resonator. How good is this performance? Could it be better? What are the limits to the noise performance of this oscillator? What are the significant contributors to its noise?

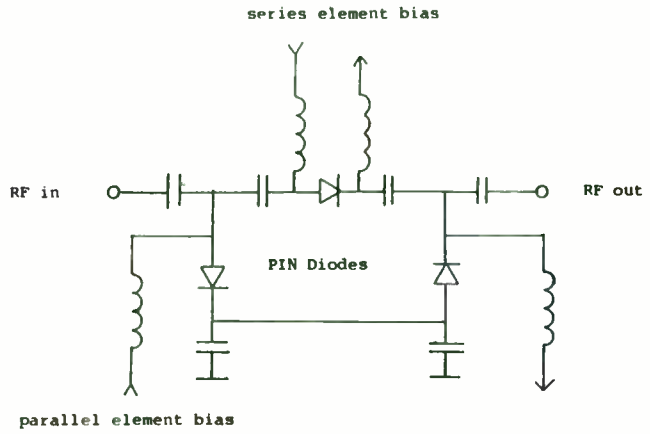


Figure 3: Pi Attenuator test circuit

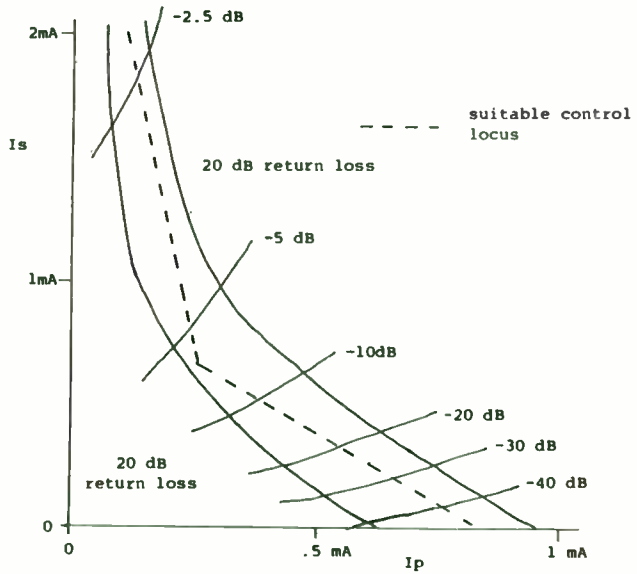


Figure 4: Lines of constant return loss and attenuation

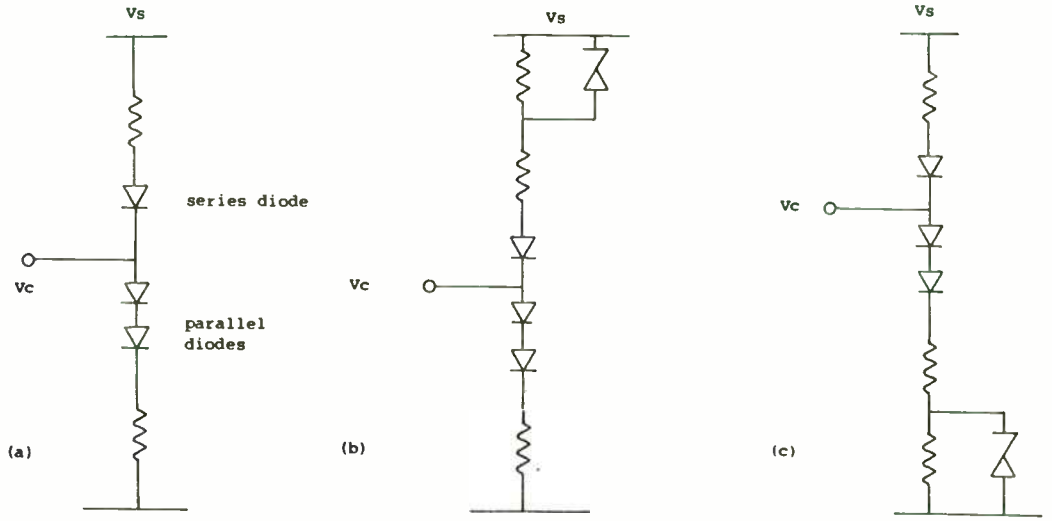
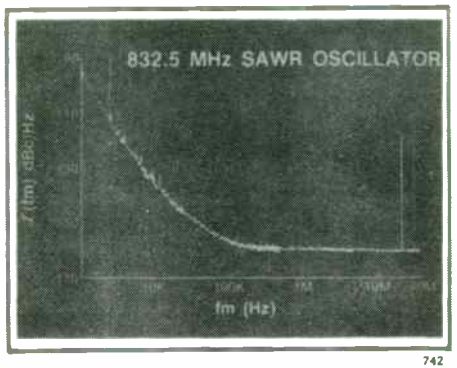


Figure 5: Bias driver circuits



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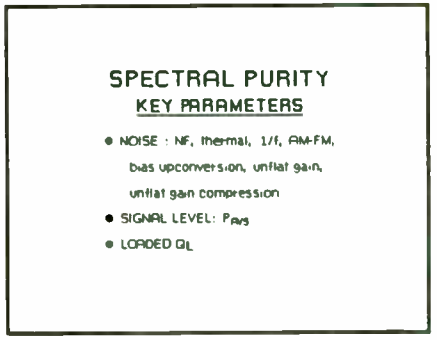
The previous phase noise plot was measured on Hewlett-Packard's 3047 phase noise measurement system. This system has the capability of measuring noise as low as ~−170 dBc. It covers the frequency range 10 MHz to 18 GHz.



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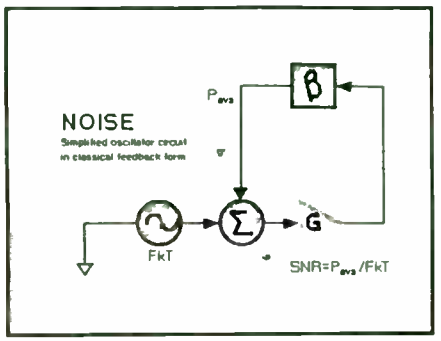
Key parameters that will be important in our discussion of phase noise in oscillators include noise iteself as evidenced by the noise figure of the active devices and circuits used in the oscillator, 1/f noise of active devices and resonators, AM-FM conversion of noise, upconversion of bias noise, and unflat gain.

Signal levels in the circuit are important. Higher signal levels lead to higher signal to noise ratios and thus better phase noise.

We will see that loaded resonator Q will determine phase noise close to the carrier and that increasing loaded Q will improve phase noise close to the carrier.



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We can model an oscillator in the classical feedback form with an amplifier with gain G and feedback β which includes the resonator. For oscillation at $f = f_0$, two conditions must be satisfied:

1. Loop gain is greater than one at f_0.

$$|G\beta| > 1 \text{ at } f = f_0$$

2. Phase shift around the loop = 0

$$\angle G\beta = 0 \text{ at } f = f_0$$

In the interest of preventing spurious oscillations at undesired frequencies, two other conditions should be met:

$$|G\beta| < 1 \text{ at } f \neq f_0$$

and

$$\Gamma_{node} < 1 \text{ for all nodes at } f \neq f_0$$

where Γ is the reflection coefficient looking into any node. (Meeting this condition at the collector and base nodes is usually sufficient.)

Signal to noise ratio at the input to the amplifier is P_{avs}/FkT where P_{avs} is the power available at the input of the amplifier and F is the noise figure of the amplifier.

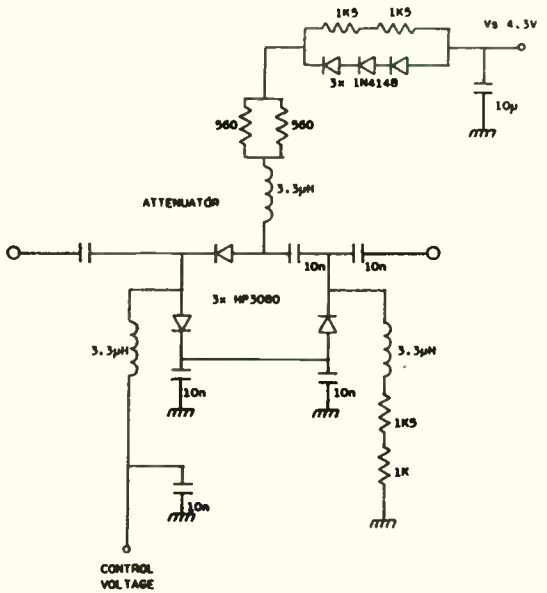


Figure 6: Final pi attenuator circuit

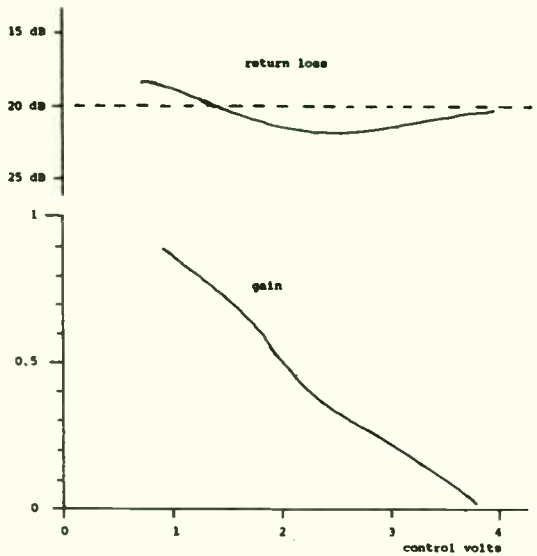


Figure 7: Attenuator performance

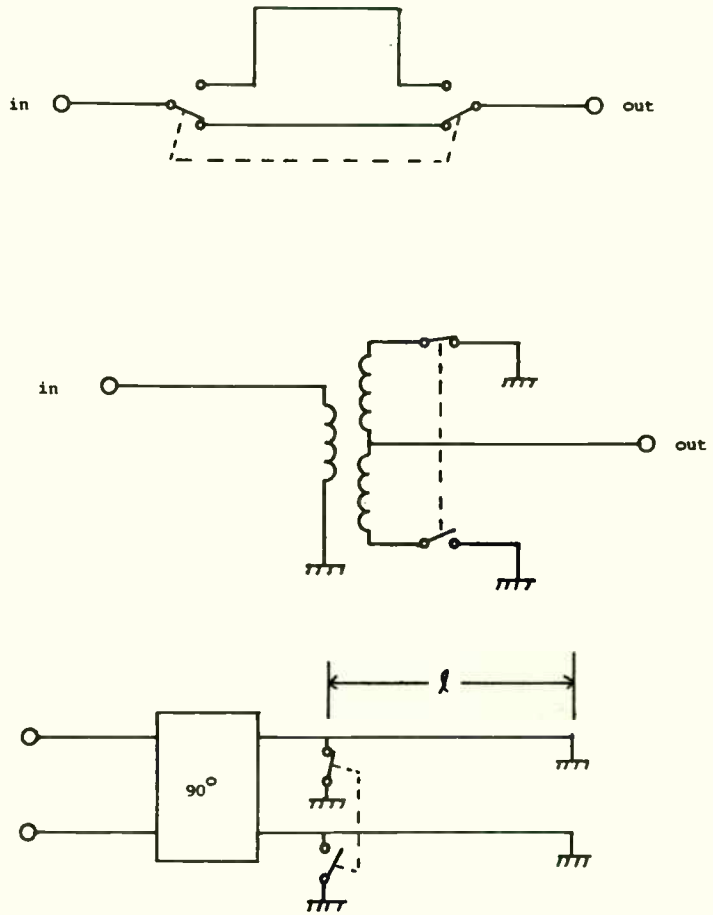
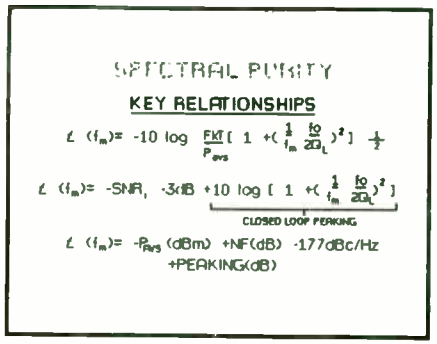


Figure 8: Phase shifter circuits



967

We assume that the signal to noise ratio at the input P_{avs}/FkT causes both amplitude and phase noise in equal amounts. For frequencies far from resonance, f_0, where loop gain $\ll 1$, phase noise relative to the carrier will be

$$f_m = \frac{1}{2}\,\frac{FkT}{P_{avs}}$$

Thus

$$\mathcal{L}(f_m) = -SNR_i - 3\ dB$$

where

$$SNR_i = 10 \log \left(\frac{P_{avs}}{FkT}\right)$$

for $f_m \gg$ loop bandwidth.

Close to the carrier, loop gain peaking will cause amplification of this noise. Let's first understand loaded resonator Q:

$$Q_L = \frac{f_0}{2}\,\frac{\partial \angle(G\beta)}{\partial f}\bigg|_{f=f_0}$$

where

$$\frac{\partial \angle(G\beta)}{\partial f} = \text{loop gain phase slope.}$$

Loaded Q determines the open loop bandwidth of the feedback loop used to represent the oscillator. Inside the bandwidth,

$$\frac{f_0}{2Q_L},$$

when the loop is closed loop peaking increases phase noise. A first order approximation of phase noise is then

$$L(f_m) = \frac{1}{2}\,\frac{FkT}{P_{avs}}\left[1 + \left(\frac{1}{f_m}\,\frac{f_0}{2Q_L}\right)^2\right]$$

where

$L(f_m)$ = the ratio of SSB noise power due to PM in a 1 Hz bandwidth (centered f_m Hz off the carrier) to total signal power;

F = the noise factor of the active device;

k = Boltzmann's constant; = 1.38×10^{-23} W-s

T = Temperature (in °K $\approx$ 300°K)

P_{avs} = the power available from the source, resonator, in watts

f_0 = oscillation or carrier frequency

f_m = offset frequency

or

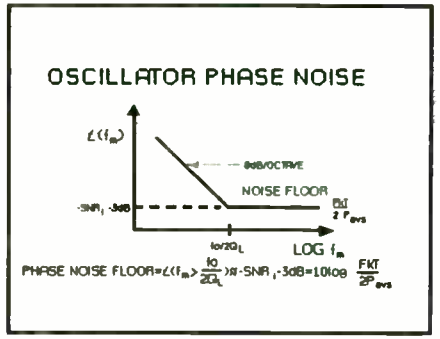
$$\mathcal{L}(f_m) = -10 \log \left[\frac{1}{2}\,\frac{FkT}{P_{avs}}\left[1 + \left(\frac{1}{f_m}\,\frac{f_0}{2Q_L}\right)^2\right]\right]$$

or

$$\mathcal{L}(f_m) = -3\ dB - SNR_i + 10 \log \left[1 + \left(\frac{1}{f_m}\,\frac{f_0}{2Q_L}\right)^2\right]$$

If we express P_{avs} in dBm, and knowing that thermal noise in a 1 Hz bandwidth = −174 dBm, then

$\mathcal{L}(f_m) = -P_{avs}$ (dBm) + NF (dB) − 177 dBc/Hz + peaking term (dB).



968

This slide presents the previous results in graphical form. For large offsets

$$\left(f_m \gg \frac{f_0}{2Q_L}\right),$$

the phase noise floor =

$$\frac{FkT}{2P_{avs}} = -SNR_i - 3\ dB.$$

Inside the offset frequency

$$\frac{f_0}{2Q_L},$$

which is the bandwidth of the open loop circuit of our oscillator model, noise rises 6 dB/octave.

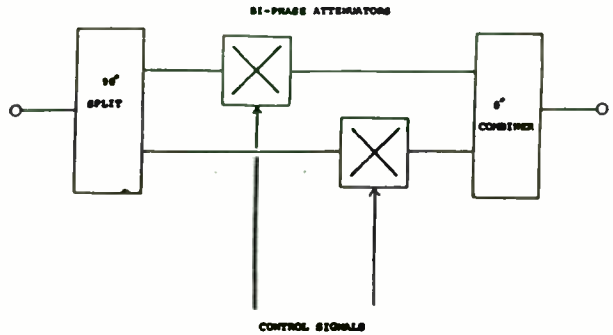


Figure 9: Vector modulator

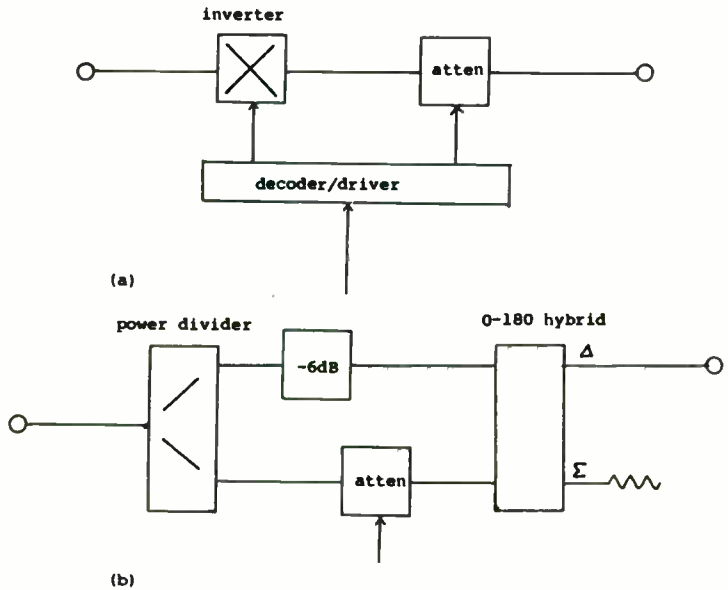


Figure 10: Bi-phase attenuators

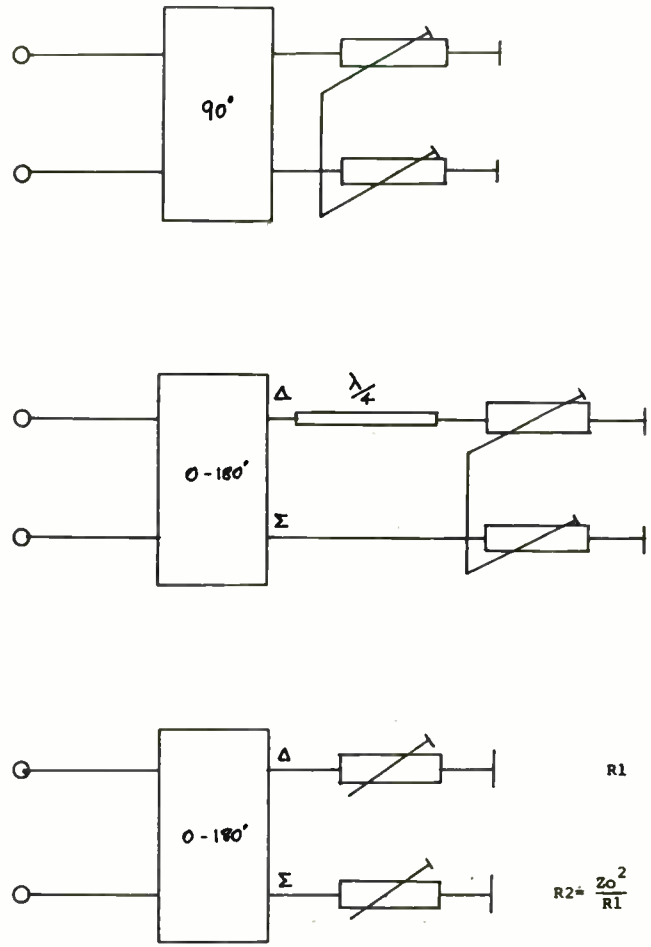
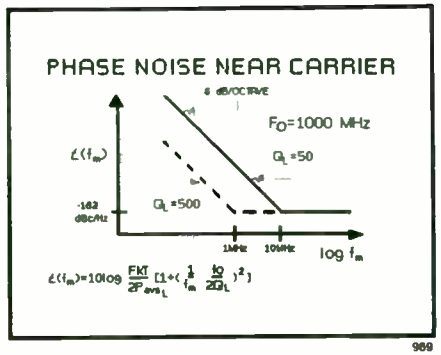


Figure 11: Hybrid coupler attenuators



Let's look at an example. If we assume a power level of +10 dBm and NF = 5 dB then the phase noise floor

$$= -177\ \text{dBc/Hz} + \text{NF (dB)} - P_{avs}\ \text{(dB)}$$

$$= -177 + 5 - 10 = -182\ \text{dBc/Hz}$$

$$f_m \gg \frac{f_0}{2Q_L}$$

For phase noise close to the carrier, the equation for shows

$$L(f_m) \approx \frac{1}{2}\,\frac{FkT}{P_{avs}}\left(\frac{1}{f_m}\,\frac{f_0}{2Q_L}\right)^2$$

Thus

$$\mathcal{L}(f_m) \propto \frac{F}{P_{avs}}\,\frac{f_0^2}{Q_L^2} \propto \frac{f_0^2}{SNR_i\ Q_L^2}$$

To minimize phase noise we must maximize signal to noise ratio and loaded Q. Also notice that low phase noise is easier to achieve at low carrier frequencies.

In the example f_0 = 1000 MHz, P_{avs} = +10 dBm, NF = 5 dB, and Q_L = 50.

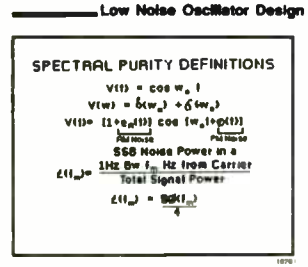
What is $\mathcal{L}$(100 kHz)?

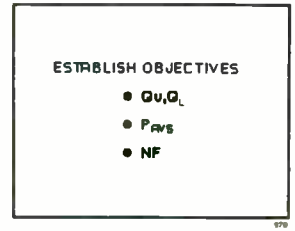
$$\approx \text{phase noise floor} + \text{peaking}$$

$$\approx -182\ \text{dBc/Hz} + 20\ \log\left(\frac{f_0}{2f_m\ Q_L}\right)$$

$$\approx -142\ \text{dBc}.$$

If Q_L = 500, this improves 20 dB to −162 dBc/Hz.





Starting with a specific close-in phase noise requirement, $L(f_m)_{required}$, then Q_L can be determined from

$$L\left(f_m \ll \frac{f_0}{2Q_L}\right)_{required} \approx \frac{FkT}{2P_{AVS}}\left(\frac{f_0}{2f_m\ Q_L}\right)^2$$

$$\therefore Q_L \text{ required} > \sqrt{\frac{FkT}{2P_{AVS}}}\ \frac{F_0}{2f_m\sqrt{L(f_m)_{required}}}$$

Having Q_L, a resonator may be selected using a rule of thumb that $Q_U \geq 2$ to 5 times Q_L.

The power level, P_{avs}, is typically set by limitations in the resonator (higher power means greater AM-FM, and potential spurious responses, aging, etc.) or by NF or power handling limitations in the active device

$$\text{Phase Noise Floor} = L\left(f_m \gg \frac{f_0}{2Q_L}\right) \approx \frac{FkT}{P_{AVS}}$$

$$\therefore P_{avs} \gtrapprox \frac{FkT}{L\left(f_m \gg \frac{f_0}{2Q_L}\right)}$$

This relationship may also give a NF requirement

$$F \lessapprox \frac{P_{AVS}\ L\left(f_m \gg \frac{f_0}{2Q_L}\right)}{kT}$$

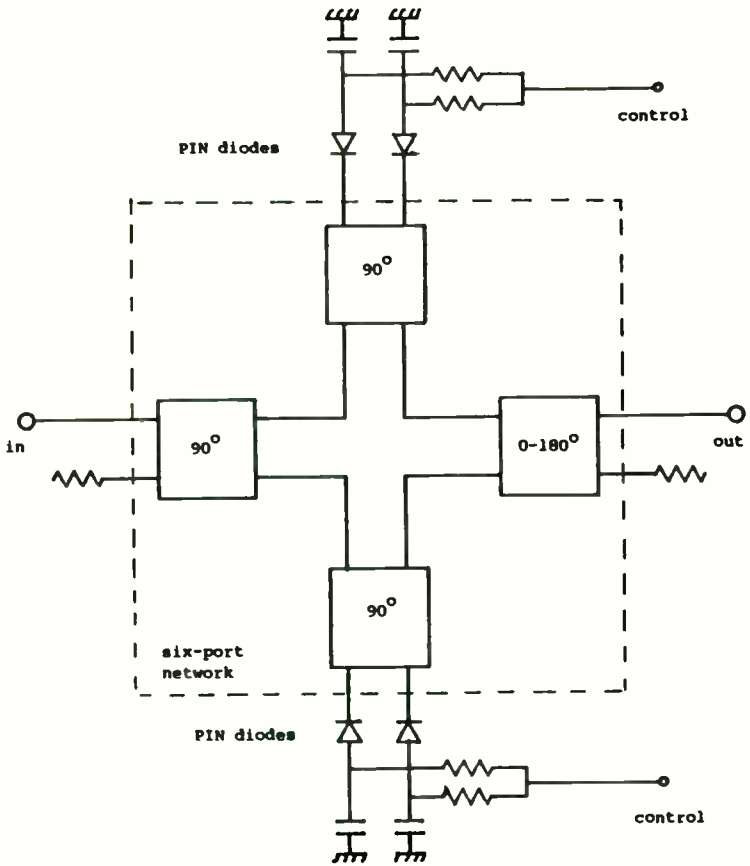


Figure 12: "Six-port" Vector Modulator

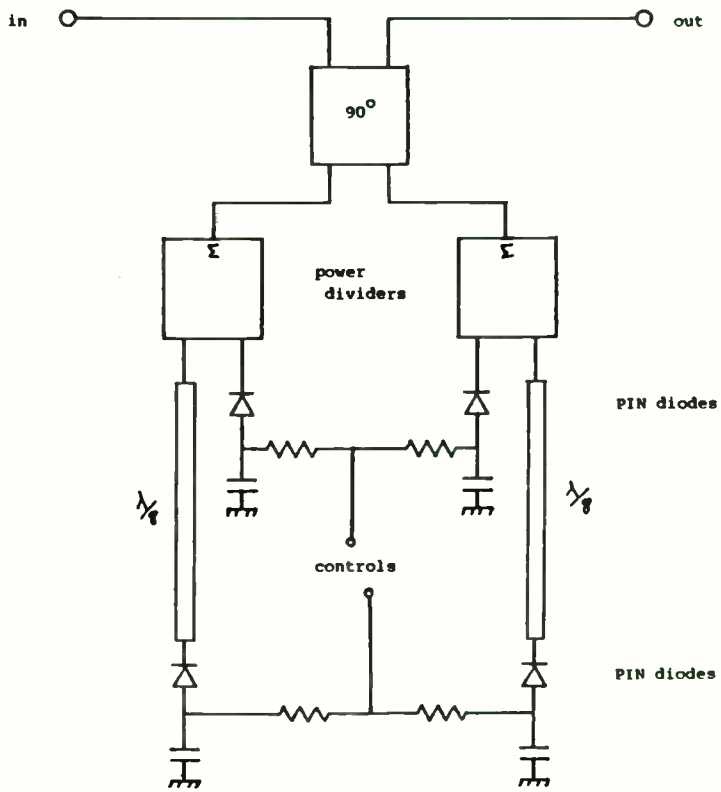


Figure 13: Reflective Delay Line Vector Modulator

Once a potential resonator has been selected, it makes sense to verify some of its parameters, notably its unloaded Q (Q_U), 1/f noise, and AM-to-FM conversion. The unloaded Q of a resonator can be measured on a network analyzer by coupling very lightly to the resonator and measuring either the 3 dB bandwidth, phase slope, or the group delay. For this purpose:

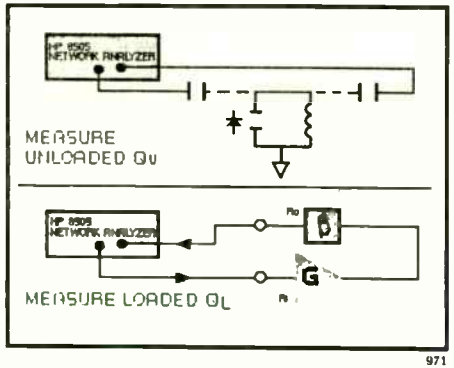
$$Q_U = \frac{f_0}{BW_{3\ dB}}$$

$$Q_U = \frac{f_0}{2}\ \frac{\delta\phi}{\delta f} = \pi f_0\, \tau_{GD}$$

where

τ_{GD} = S_{21} group delay in seconds

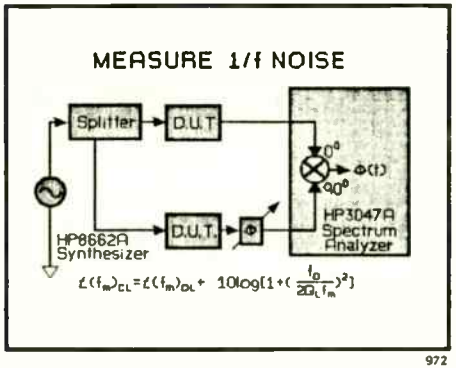
$$\tau = Q_U/f_0\pi$$

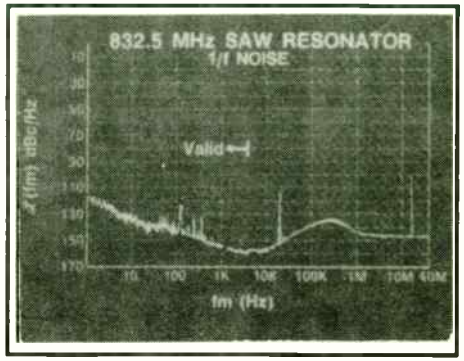


One helpful way to measure Q_U versus frequency is to set the network analyzer in the log frequency mode and draw a 6 dB/octave slope line falling off with frequency. If the group delay rises above the slope line, then Q_U is rising with frequency.

Verifying Q_L in the actual oscillator circuit is also possible, provided that the characteristic impedance Z_0 of the network analyzer is near the operating circuit impedance, or that transformers are used to match the impedances of the test system and the circuit over the frequency range, and power levels are near operating conditions.

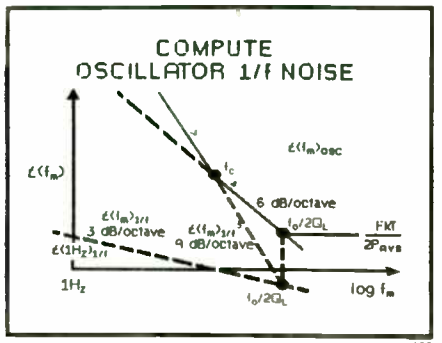
Ref. 12, 25, 26, 27





This is an example of 1/f noise measurement using the technique in the previous slide. These data are indicative of typical 1/f noise seen in SAW resonators: we've seen 5 to 10 dB better and 20 to 30 dB worse.

D. Halford has suggested a "rule of thumb" phase noise intercept of −115 dBc/Hz at a 1 Hz offset. See ref. 16.



It is possible to predict the phase-noise performance of the oscillator circuit (closed loop) by adding the white phase-noise component, FkT/$2P_{avs}$, to the 1/f component, $L(f_m)_{1/f}$, and then modifying both of these by the oscillator closed-loop gain peaking, $[1 + (f_0/f_m 2Q_L)^2]$. The total oscillator phase noise is

$$\mathcal{L}(f_m) = 10 \log\left[1 + \left(\frac{f_0}{f_m 2Q_L}\right)^2\right] \cdot \left[\frac{FkT}{2P_{avs}} + L(f_m)_{1/f}\right].$$

The components of 1/f and white phase noise of the amplifier-resonator combination are artificially separated. However, if we measure the total phase noise, $\mathcal{L}(f_m)_{OL}$, of the series amplifier-resonator open loop (with the correct terminating impedance and power levels), it's possible to predict the oscillator phase noise directly:

$$\mathcal{L}(f_m) = 10 \log\left[1 + \left(\frac{f_0}{2f_m Q_L}\right)^2\right] L(f_m)_{OL}$$

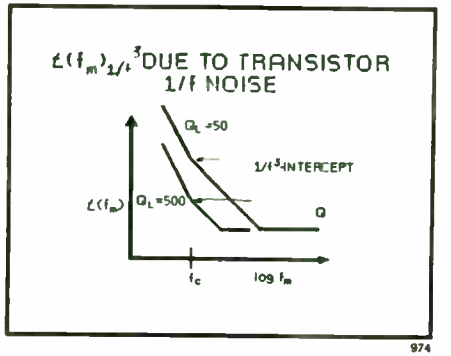
$$\mathcal{L}(f_m) = \mathcal{L}(f_m)_{OL} + 10 \log\left[1 + \left(\frac{f_0}{2f_m Q_L}\right)^2\right]$$

This phase-noise prediction can be shown more easily with a graphical approach. First, plot the phase noise due to white noise components. Then, draw $\mathcal{L}(f_m)_{1/f}$ on the same graph. Next, draw a −9 dB octave line that intersects $\mathcal{L}(f_m)_{1/f}$ at $f_m = f_0/2Q_L$. The intersection of this line with the locus of

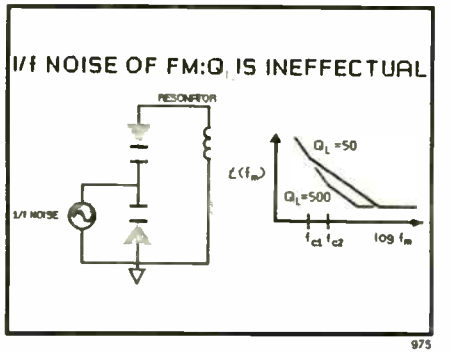
$$\mathcal{L}(f_m) = 10 \log \frac{FkT}{2P_{avs}}\left[1 + \left(\frac{1}{f_m}\,\frac{f_0}{2Q_L}\right)^2\right]$$

is f_c, the $1/f^3$ noise-corner frequency. The 9 dB/octave line then serves as the predicted value of $\mathcal{L}(f_m < f_c)$.

Ref. 41



If 1/f phase noise modulation is in the resonator or active device, then an increase in Q_L will improve the phase-noise performance in the 1/f region. This occurs because the loop peaking effect operates on 1/f noise as well as white noise as can be seen from the previous equations.



However, if the 1/f noise mechanism is frequency modulating the resonator center frequency, then no improvement of Q_L will lower phase noise in the 1/f region. If a noise source is phase modulating the oscillator, then changing the phase slope of the resonator—or changing the Q—will affect the depth of modulation.

High-Voltage HF/VHF Power Static Induction Transistor Amplifiers

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Waltham, MA 02254

The operation and performance of power static induction transistors (SITs) in HF/VHF amplifiers will be discussed in this presentation.

Unprecedented saturated CW output power levels of greater than 200 W at 225 MHz, with 6-dB power gain and 70% drain efficiency, have been demonstrated by single-ended transistors connected in the common-gate configuration. Small-signal measurements on these power SITs indicate a nearly flat 10-dB gain response from 100 MHz to 3 GHz, and a unity power gain frequency in X-band.[1,2]

Static induction transistors, which are operated in a common-source configuration, however, can provide very high gain at frequencies in the HF/VHF and lower UHF frequency bands. To accomplish this, the parasitic drain-to-gate capacitance must be neutralized.

The broadband neutralization scheme to be presented is similar to the cross neutralization scheme successfully used for push-pull triode vacuum tube amplifiers (Figure 1). In this design, the parasitic feedback capacitance, C_{PG} (capacitance plate to grid), of each active device is neutralized by adding two neutralization capacitors, externally, which are approximately equal in value to the individual parasitic feedback capacitance values. The addition of these neutralization capacitors to the circuit results in a capacitive bridge, as illustrated in Figure 1. Proper selection of the neutralization capacitors balances the bridge, thereby "nulling out" any potential feedback signals between the output and input of the balanced device. The analogous solid state SIT amplifier is shown in Figure 2.

The computed small-signal gain response and stability factor of this cross-neutralized SIT amplifier, shown in Figure 3, demonstrates the broadband performance potential of this neutralization scheme. Effective broadband neutralization depends upon judicious selection and placement of neutralization capacitors *within the transistor package* and attention to the bond wire inductance associated with connecting the neutralization capacitors to the SIT chips. The neutralization capacitors are implemented as discrete, high Q, low loss capacitors *mounted inside* the power transistor package in close proximity to the active SIT chips. Very short bond wires are used to connect them, thus *eliminating completely* the potential for resonance conditions. As shown in Figure 3, the calculated gain is approximately 14 dB across the entire 1- to 200-MHz band with a stability factor of >14. Experimental cross-neutralized SITs were fabricated in our laboratory using two, six-cell, 7-μm pitch SGSITs connected in a single balanced transistor package along with a pair of 27-pF chip capacitors mounted inside the package to provide neutralization. The amplifier was designed and fabricated using coaxial 4:1 transformers and baluns wound on high permittivity ferrite toroids. Initial power tests were performed at 100 MHz, where the amplifier exhibited 50 W CW output power with 12.2-dB power gain, as shown in Figure 4. This amplifier performance reflects the power performance in an "as-fabricated" state, without tuning to optimize the performance. The device contains enough active area (W_g = 24 cm) to deliver about 200 W of output power; however, the package which was used is only capable of dissipating approximately 100 W of average power. To establish the CW potential of this amplifier, pulsed operation at a 10% duty was examined. Figure 5 illustrates the peak power capability of this device. A peak output power level of 120 W was observed with 13-dB gain and 40% average efficiency. With a proper package and design refinements, output power levels of nearly 200 W across the band should be possible with this design.

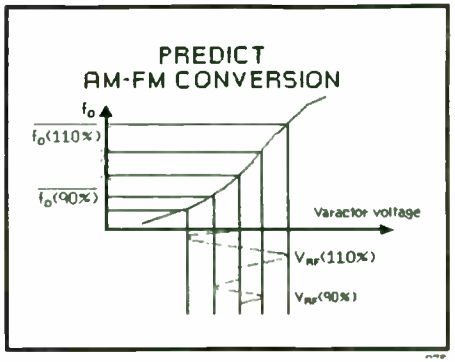
Acknowledgment

The authors gratefully acknowledge Mehdy Abdollahian, Anthony Varallo, and Marguerite Delaney for their talented work in device packaging, amplifier fabrication, and characterization; Emel Bulat, Maureen Sullivan, Charles Herrick, Steve Rose, and Theresa Rubico for device fabrication; and Drs. Paul Haugsjaa; Harry Lockwood, and Les Riseberg for their continuous support throughout this work. In addition, we thank Frank Stites of GTE Government Systems for his valuable comments and suggestions.

References

1. R. J. Regan and S. J. Butler, "High Voltage UHF Power Static Induction Transistors," Proceedings of RF Technology Expo '85, Anaheim, CA, January 1985, pp. 81-84.

2. R. J. Regan, I. Bencuya, S. Butler, F. Stites, and W. Harrison, "New UHF Power Transistor Operates at High Voltage," *Microwaves and RF 24 63*, (April 1985).



In many VCOs, the spectral purity is dominated by AM-to-FM conversion mechanisms, rather than the SNR_i and Q_L. One method to predict the AM-to-FM conversion in a diode-tuned VCO is by studying the frequency-versus-tuning-voltage characteristic. A change in the rf voltage amplitude on the resonator can affect the average bias on the varactor. A 10-percent change in resonator rf voltage corresponds to 10-percent AM on the carrier. To measure the effects of changing carrier level, one can increase or decrease the rf voltage on the resonator by changing the bias current in the active device. Measure the carrier frequency at 90-percent resonator voltage and compare this with the average carrier frequency at 110-percent resonator voltage. The peak-to-peak frequency shift due to 10-percent AM can then be estimated:

$$\overline{f_0(90\%)} \cong \frac{f_0(+\text{peak}) - f_0(-\text{peak})}{2}$$

$$\Delta f_{pk}(10\%\ \text{AM}) = \frac{\overline{f_0(110\%)} - \overline{f_0(90\%)}}{2}$$

$$K_v(\text{AM/FM}) = \frac{\Delta f_{pk}(10\%\ \text{AM})}{10\%}\ \text{Hz pk/\% AM}$$

This equation provides a solution in frequency modulation/percent AM. The percent AM, A, should be no less than the collector bias current shot noise fluctuations divided by collector bias × 100 percent:

$$A\%\ \text{AM} = \frac{\sqrt{2}\sqrt{2qI_c}}{I_c} \times 100\% = 200\sqrt{q/I_c}\%$$

where

$\sqrt{2qI_c}$ = the full collector shot noise,

and

q= the charge of an electron = 1.6×10^{-19} Coulomb

Now we can predict the closed loop phase noise contribution due to AM-FM:

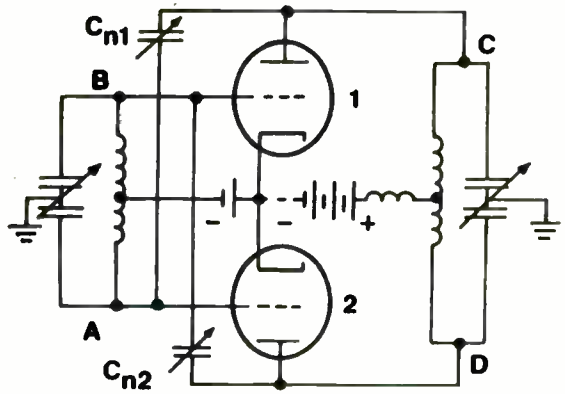
$$\mathcal{L}(f_m)_{AM} = 20 \log \left[\frac{A\ K_v(\text{AM/FM})}{2\ f_m}\right]$$

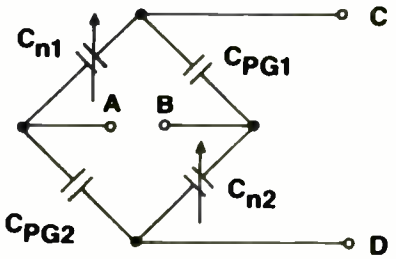
or total phase noise:

$$\mathcal{L}(f_m) = 10 \log \left\{\left[1 + \left(\frac{f_0}{2f_mQ_L}\right)^2\right] \cdot \left[\frac{FkT}{2P_{avs}} + L(f_m)_{1/f}\right] + \left[\frac{A\ K_v(\text{AM/FM})}{2f_m}\right]^2\right\}$$

Ref. 28, 29

PUSH-PULL
CROSS NEUTRALIZED AMPLIFIER

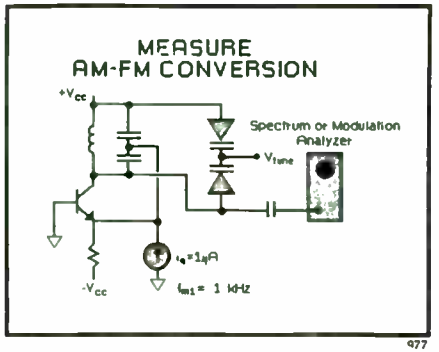




EQUIVALENT BRIDGE CIRCUIT

GTE Laboratories

Figure 1.



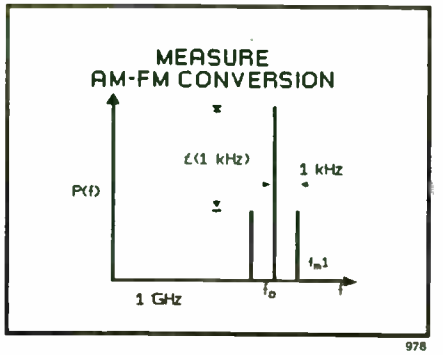
There are several methods for measuring the AM-to-FM conversion coefficient ($K_{vAM\text{-}FM}$). In one case, the resonator must be set up at the appropriate power level with the correct amount of coupling/loading, and connected to a network analyzer. By shifting the power level ±10 percent, and monitoring the center-frequency shift.

$$K_v(AM/FM) = \frac{\Delta f_{pk}(10\%\ AM)}{10\%}\ \text{Hz pk/\%AM}$$

Another method of measuring AM-to-FM conversion is to adjust the transistor bias current 10%, monitor Δf, and use

$$K_v(AM/FM) = \frac{\Delta f_{pk}(10\%\ AM)}{10\%}\ \text{Hz pk/\%AM}$$

Typically, a transistor is collector-current cutoff-limiting, so a 10-percent increase in the collector bias current will cause a 10-percent increase in the resonator voltage. The latter approach may cause a change in the active device's phase angle, but this is acceptable, since it's desirable to characterize the sum of all effects contributing to AM-to-FM conversion.



The AM-to-FM conversion can also be tested dynamically. This technique involves injecting a small, low frequency (f_i) current into the transistor's emitter. Adjust f_i until the sidebands around the carrier roll off 6 dB for each octave increase in f_i (which indicates FM):

$$P_{\%AM} = \left(\frac{\text{injected current peak}}{\text{emitter bias current}}\right) \times 100\%$$

$\mathcal{L}(f_i)$ = measured SSB-to-carrier ratio of the injected FM sidebands. From the narrowband FM approximation we have:

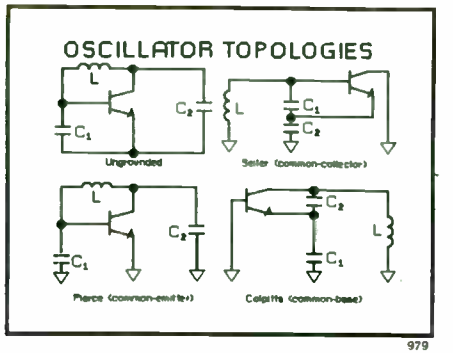
$$\mathcal{L}(f_i) = 20 \log\left(\frac{\Delta f_{ipk}}{2f_i}\right)$$

$$\Delta f_{ipk} = (2f_i)\ 10^{\mathcal{L}(f_i)/20}$$

Δf_{ipk} = peak frequency deviation indicated by these sidebands

$$\therefore K_v(AM/FM) = \frac{\Delta f_{ipk}}{P_{\%AM}}\ \text{in Hz peak/\%AM}$$

One can also measure this FM modulation directly using an 8901 modulation analyzer.



"Many oscillators can be reduced to a Colpitts configuration." The basic layout is an oscillator circuit without a ground terminal. By grounding this circuit at any of its nodes, it can be transformed into any of the other configurations. The preferred topology is one that makes it possible to visualize such things as loop gain, loop phase angle, and stopband stability.

The common-emitter (Pierce) topology is ideal for good out-of-band stability. It yields open-circuit stability at frequencies above about $f_T/3$, and can be kept stable at lower frequencies. Alternatively, the common-base (Colpitts) topology typically has negative real-part impedance at its emitter from about $f_T/5$ to f_{max}, depending on the base-to-ground parasitic inductance. The common-collector configuration, with capacitive loading on its emitter, typically possesses a negative real-part impedance at its base over a significant range of frequencies. Instability is a potential problem whenever there is a negative real part of the impedance at frequencies other than the desired oscillation frequency. The result can be spurious oscillation, squegging, parametric effects, and sharply nonlinear tuning characteristics, especially when a harmonic of the desired frequency crosses through a region of negative resistance. Refs. 9, 10, 4, 5, 6

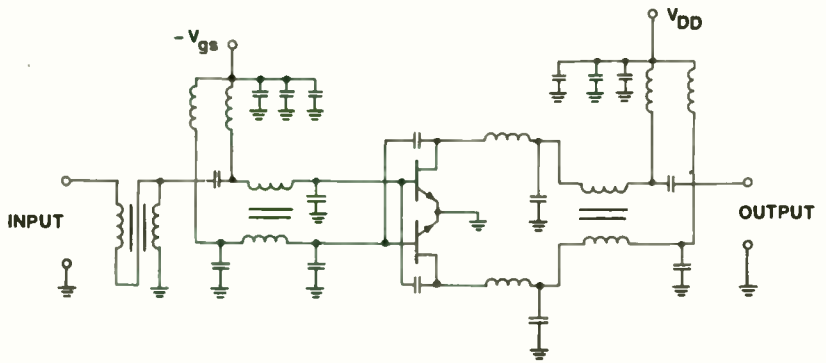


Figure 2. Cross-Neutralized Common-Source Push-Pull Static Induction Transistor Amplifier Design

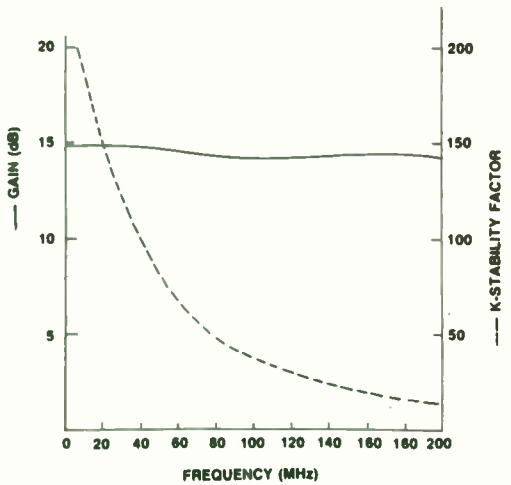


Figure 3. Computed Small-Signal Gain and Stability Factor for Cross-Neutralized Push-Pull SIT Amplifier Shown in Figure 2

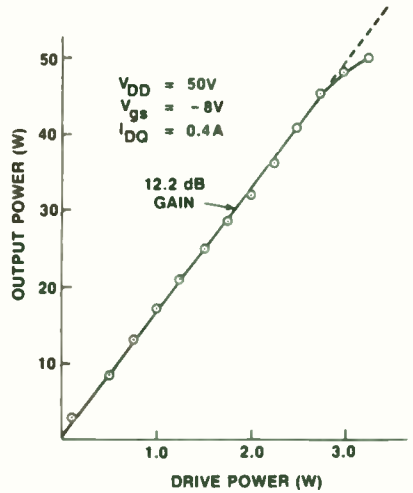


Figure 4. 100-MHz cw Power Performance for the Cross-Neutralized Push-Pull Common-Source SIT Amplifier

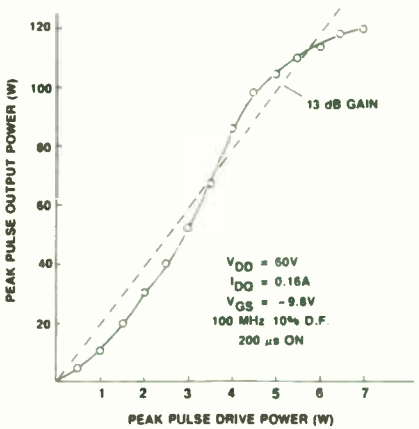
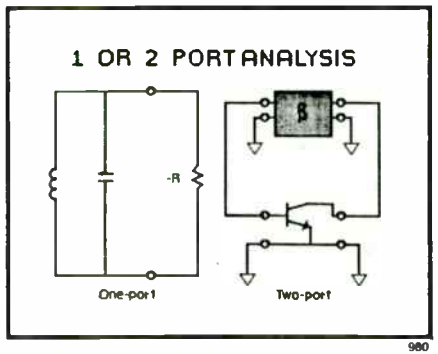
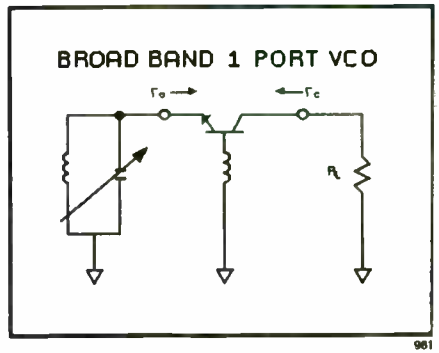
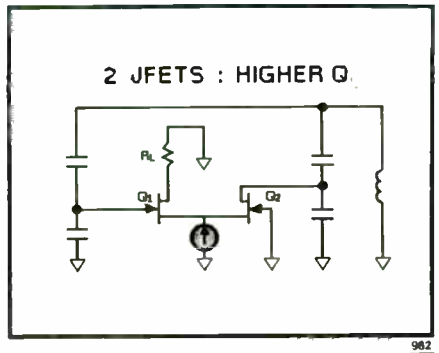


Figure 5. 100-MHz Pulsed Power (10% Duty Cycle) Performance of Cross-Neutralized Push-Pull Common-Source SIT Amplifier







Oscillator topologies can be designed as one-port or two-port configurations. One-ports (negative-resistance oscillators) have good track records in the gigahertz region. The two-port topology permits analysis and ease of visualization using feedback theory; loop gain and phase slope may be more easily derived (and measured) to predict loaded Q_L and spectral purity.

This one-port configuration is widely used in the gigahertz region with YIG-tuned oscillators and VCOs; multi-octave tuning range is a key advantage.

Despite its good points, however, this configuration has its drawbacks. It does not allow easy definition of loaded Q for the purpose of predicting phase noise, nor does it permit simple modeling of loop gain. This topology is also susceptible to spurious modes, since the conditions for the emitter relection coefficient, $\Gamma_e > 1$, leads to potential instability over a broad range of frequencies. The phase noise for this kind of oscillator can be accurately predicted by a computer method we will discuss shortly.

Refs. 17, 18, 19, 20, 21, 22, 23, 31, 32, 33

The choices are many: bipolar junction transistors, JFETs, SiMOSFETs, GaAs FETs, Gunn/IMPATT diodes, or miniature packaged amplifiers. In all cases, the selection criteria should include low noise figure at the maximum operating junction temperature; low noise figure at higher power in order to get the highest signal-to-noise ratio (SNR) possible; and low noise figure at the source impedance presented to the device. Certain warnings are also in order. Beware of large ripple occurring in small-signal S_{21} gain in the presence of a large signal at f_0; this indicates nonlinear compression. This is not a parameter that the device manufacturer will specify and must be measured on a network analyzer. Also, be wary of limitations in resonators, such as spurious content in YIG resonators ($\geq$ +10 dBm) and aging in SAW and bulk crystal resonators ($\leq$50 μW is typical for most frequency standards).

Of the devices listed above, the bipolar junction transistor is a natural for low-noise design due to its well-characterized and repeatable parameters. The characteristics of the other devices tend to be not quite so predictable. FETs, for example, exhibit significant variations in pinchoff voltage and performance with temperature. A good rule of thumb is to select f_T at least two to three times the operating frequency, and to remember that the noise figure degrades (i_n increases) as f_0 exceeds f_β.

Ref. 7

A JFET is a good choice for achieving low-noise oscillator performance at $f_0 \leq$ UHF. This performance is most likely due to the high input real-part impedance, which allows tight coupliing and little loading of the resonator (high Q_L). Concurrently, a good noise figure can be achieved with a high source impedance because the JFET input noise current (i_n) is so low:

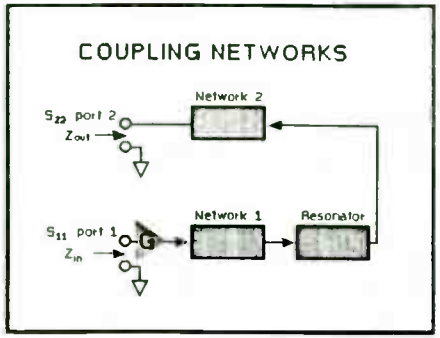
$$r_s \text{ (optimum NF)} = e_n/i_n$$

The end result is high SNR_i or very good phase-noise characteristics.

It has been mentioned that phase noise may be dominated by SNR_i and Q_L (ignoring 1/f noise for the moment). Good SNR_i and Q_L depends on the noise figure of the active device at the operating source impedance, on P_{avs}, and on the Q_L/Q_U degradation due to active device and output loading. The JFET possesses operating characteristics that enable it to achieve high Q_L/Q_U and SNR_i simultaneously.

In a two-port oscillator, there are three contributors to Q_L degradation: the input resistance of the amplifier, the output resistance of the amplifier, and the load resistance. One way to improve Q_L/Q_U and SNR_i is to use two devices in an oscillator circuit. This two-device circuit lightly loads the resonator due to the high input and output real parts of the JFET impedance. The load is isolated from the resonator by Q_1, thus removing the third contributor to Q_L degradation.

At low frequencies especially, take advantage of excess device gain to keep impedances large by using feedback. This will help to not load the resonator Q.



The purpose of an oscillator's coupling networks are: to match the input/output impedance of the active device to that of the resonator for optimum P_{avs}, Q_L, and NF; to provide enough phase shift to achieve 0-deg. phase in the angle of the loop-gain transfer function at f_0, where hopefully the loop gain is greater than 1.0 and near the maximum phase slope; and to select the desired operating frequency mode in a multimode oscillator. Some common forms of coupling networks are presented in refs. 12, 9, 10, and 37.

Three coupling network design objectives can also be stated mathematically as

$$|S_{21}|_{\text{loop gain}} > 0 \text{ dB}$$

and

$$\angle S_{21}|_{\text{loop gain}} = 0^\circ$$

for $f = f_0$ only;

and

$$|\Gamma_{\text{node}}| < 1.0$$

for $f \neq f_0$ and all nodes.

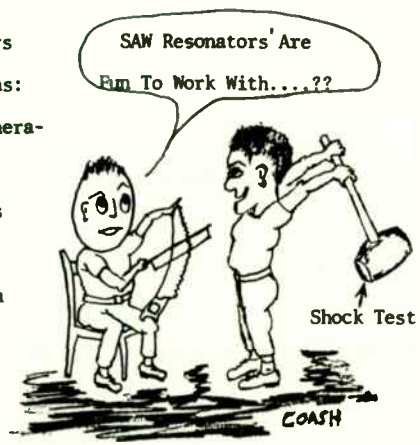
Ref. 12, 9, 10, 37, 38

Title: AN EVOLUTION INTO SAW RESONATORS (Low Power Security -- FCC Part 15)

by
Ronald J. Coash -- Notifier/EMHART, 6050 N. 56 St.
EMHART Electrical/Electronic Group Lincoln, NE 68507

SUMMARY

Surface Accoustic Wave Resonators are being used in applications such as: CATV, satellite subsystems, signal generators, security systems,garage door openers, etc. At Notifier, the SAWRs are being used in low power security systems. Few books have been written on SAWRs, so the best information to date appears in technical magazines and papers.

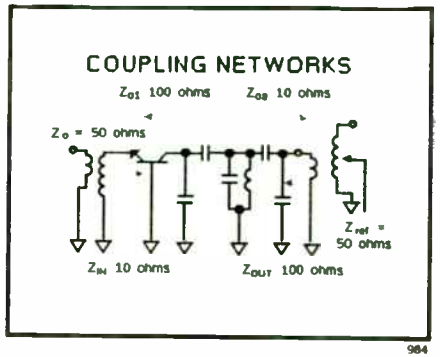


Fundamential frequencys of SAWR oscillator circuits range from 150 MHz to beyond 1,500 MHz. SAWRs exhibit characteristics of the historical bulk crystal devices, yet belong to a much different subclass of frequency stabilizers. The selection of a SAWR is more diversified than its lower frequency bulk crystal class of frequency stabilizers. Selection and evaluation are key words and are the main issues of this paper. The last page of this paper lists other sources of information on the subject of SAWR technology.

INTRODUCTION

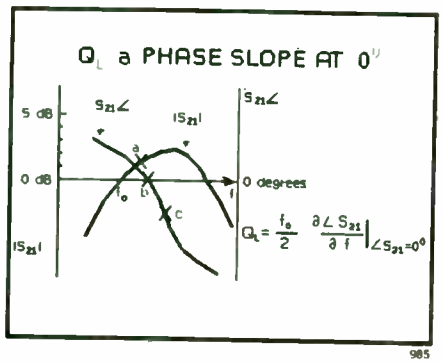
The factors involved in the use of SAWRS in short range wireless data communications are paradoxical with cost and dependability being the most important issues. Traditionally, low power (about 6,000 uV/m at 3 meters) security alarm transmitters have been limited to LC and bulk crystal devices, but some manufactures are now using Surface Accoustic Wave oscillators as the frequency stabilizing element. The range of these devices is about 200-350 feet (Null Free not Free Space Range).

1.1 Current FCC requirements have made it increasingly difficult to design and manufacture cost effective "miniture" RF transmitting and receiving devices. In several cases manufacturers are operating (or were at one time) under special wavers, thus prompting some of us to use slightly more expensive SAWR technology. Recently, costs have been reduced somewhat, thus making SAWRs more feasable with regard to FM/SAWRs being used in cost conscious designs. Many computing devices and portable radios radiate more interference (RFI/EMI) than is allowed for life safety devices under FCC Part 15. To further complicate the situation other regulations (UL 1023) require a one year battery life from a 9 volt "transistor radio battery". Formerly, Notifier manufactured bulk type crystal controlled frequency multiplier VHF transmitters that consummed more power per period of time than the present units do. In this particular case the transmitters transmit a supervisory signal once a minute for 24 hours/day. Note also that the transmitters are in the UHF range instead of previous VHF range.



The S-parameter treatment is convenient for use with network analysis. The measured S-parameter data can be used in computer modeling and analysis, and for comparing measured and predicted performance.

A coupling network can be tested with the setup shown. In this slide, Z_{in} is the reference impedance for S_{22} at the output port, and Z_{out} is the reference impedance for S_{11} at the input port. The technique is exactly correct if $Z_{01} = Z_{out}|_{Port\ 2}$ and $Z_{02} = Z_{in}|_{Port\ 1}$. Other conditions are that Z_{in} be measured with Port 2 terminated in Z_{in}, while Z_{out} be determined with Port 1 terminated in Z_{out}. These conditions are not that easy to achieve; still, if the loop is broken where the impedances are reasonably well characterized (real), and ideal (computer-simulated) transformers are employed to get different input and output reference impedances, a model develops which provides fairly accurate loop gain/ ·se data.



From the previous model we get

$$|\text{ loop gain }| \approx |\,S_{21}\,|$$

$$\angle\text{loop gain} \approx \angle S_{21}$$

The results may appear as those shown, where

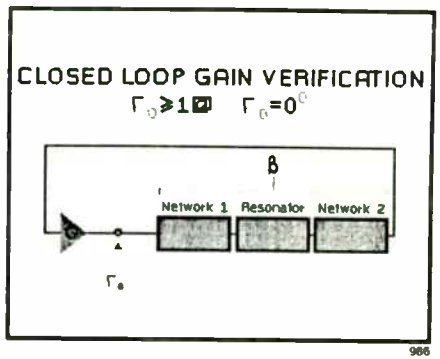
$$Q_L = (f_0/2)(\partial\phi/\partial f)\,|_{\phi = 0^\circ}$$

and

$$\phi(f) = \angle S_{21}(f)$$

It's apparent from this example that oscillation, point b, ($\angle S_{21} = 0^\circ$) will not occur at the maximum phase slope, point c. Consequently, Q_L and the phase noise will be unnecessarily degraded. There is, however, sufficient loop gain (2 dB at point a) for oscillation.

Adjustments to a coupling network make it possible to achieve maximum Q_L, that is, $\angle S_{21} = 0^\circ$ at the maximum phase slope. Coupling to the resonator can also be reduced (so that $|\,S_{21}\,| \approx$ +3 dB at $\angle S_{21} = 0^\circ$) in order to increase Q_L. Recall that this action may have deleterious effects on P_{AVS} (the power available from the source in dBm) and noise figure as functions of the source impedance.



Another test (calculated or measured) for the effectiveness of a coupling network is to close the loop and analyze the reflection coefficient (Γ) at any node. This slide illustrates this concept. Looking at the output of the oscillator, the necessary condition for oscillation is

$$\Gamma_0 > 1\,|_{\angle\Gamma_0 = 0^\circ}$$

where

$$f_0 \approx f\,|_{\angle\Gamma_0 = 0^\circ}$$

Ref. 20

1.2 Paradox/Contradictions = Strict Design Parameters (for cost effectiveness) Transmitter specifications; cigarette pack size, at least 300 ft. range, low battery detect alarm,256 system codes, 32 transmitter codes, 4 transmitter function codes, error code, 15 uA. idle current, one year battery life, one minute short supervisory transmissions (every minute of the day),8 special codes, rugged, .25% bandwidth, special scheduled transmissions, no external antenna,and do all this for the nominal sum of $15 cost (factory). Then meet FCC and UL requirements for life safety devices that have greater restrictions than do other devices not involved in life safety issues. BY THE TIME THE DIGITAL DESIGN IS COSTED THERE IS LITTLE MONEY LEFT FOR THE R.F. SECTION.

2.0 USE OF SAWR TECHNOLOGY VERSES LC CRYSTAL, etc.

2.1 What is a Surface Accoustic Wave Resonator? A SAWR is a frequency stabilizing devise which is used in much the same way as are typical bulk crystal elements, but does so at higher fundamental frequencies (150-1,500 MHz). However, the variations in the use of SAWRs used here are more extensive and the specifications vary considerably. There are various articles and papers that have been written on this subject and the purpose of this paper is to cover the somewhat obscure aspects experienced in working with SAWRs.

Since the SAWR operates on a surface phenomenum that does not appear to affect the bulk of the piezo-electric substrate, it was decided to try a truly fine idea as shown in Figure 2. The Modulator (Bulk) changes the length of the substrate and thus mudulating the spacing of the surface waves which determine the SAWR's frequency.

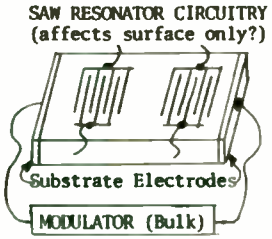


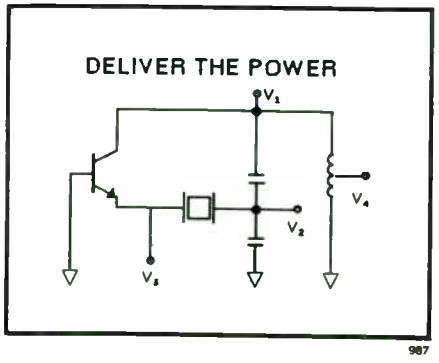
Figure 2

2.2 ADVANTAGES	DISADVANTAGES
Small size	Manufacturing tolerances
Up to +20 dBm in DIP (14 pin)	Aging>Bulk Crystal (10ppm/.1ppm)
Phase Selection (0 or 180 deg.)	Variation in Types (Selection)
Frequency Range 150-1500 MHz	Limited to above 150 MHz
Tolerance better than LC	Yeild % (Mfg.)
Rugged (Comp to VHF Bulk Xtal)	Still has harmonics
Power Disipation > Bulk Xtal	Initial tooling $4,000-6,000
FSK/FM (Wide Deviation)	Limited Number of Hybrid Low Cost Vendors
Simplifies Design	
Frequency Stability	
Lower total current than Xtal Osc.@ UHF	
Few Spurious Oscillations	
Fewer adjustments (especially at UHF)	
Reasonably Priced in Hybrid Osc. form	

(The above list is a partial one, but points out some obsecure facts See Page 9)

RESULTS OF EVOLUTION

3.0 The change from both LC oscillators and bulk crystal oscillators is a somewhat intermediate one with respect to overall characteristics. The SAWR manufactures have improved the devices over the past 3 years with respect to cost, tolerences, and yeilds. A lot of new ideas developed in piezo-electric applications-pressure sensors,active filters,etc.



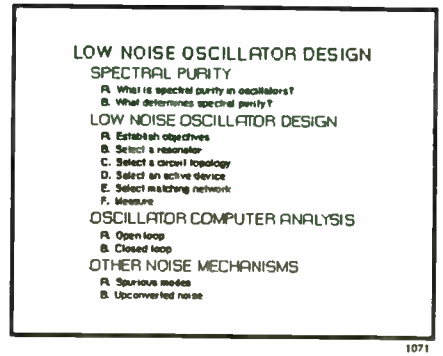
Once there is enough loop gain and the correct phase angle in a design, it's time to consider how to deliver power to the load. Power is typically taken from the resonator, but for the sake of flexibility, it should also be possible to tap signal power at any point in the oscillator loop. Tapping power at V_1, V_2, or V_4 may provide a high signal level to drive limiters and maintain a good noise floor. Node V_4 may have reduced harmonics content due to the lowpass filtering effect of the inductor. Taking power from V_3 may provide a lower noise floor due to some filtering created by the stopband rejection of the resonator crystal.

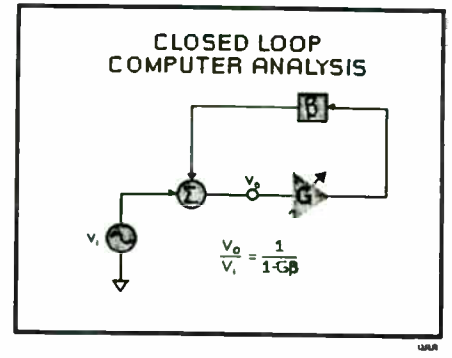
Another power-tapping technique is to reflect a load resistance, r_L, to a desired output node, such that r_L is much greater than the real-part impedance seen looking back into that node at f_0. This can be done with matching networks or transformers. As a consequence, the loop gain (and Q_L) is reduced (less than 3 to 6 dB), and the output power may not be significantly reduced.

Tapping power from the collector can provide out-of-band stability by reducing the real-part impedance as seen by the collector (common-emitter and common-base topologies). This creates heightened rejection of undesired modes.

There are many techniques for matching to a load. One method relies on series-to-parallel transformations, ref. 37.

Oscillator Computer Analysis





A computer helps to evaluate oscillator circuit output-noise spectral density (phase noise) and signal power in a closed loop format by using linear, frequency-domain analysis techniques. This approach is really just an extension of classical feedback control theory. An oscillator is a feedback amplifier whose poles of closed-loop gain transfer function have moved into the right half-plane. Feedback amplifiers may be analyzed for noise and transfer function for any degree of peaking as long as the poles remain in the left half-plane (resulting in no oscillation). If an oscillator is analyzed with its loop gain adjusted for poles very near the $j\omega$ axis, the output noise spectral density will be essentially the same as if the poles were exactly on the $j\omega$ axis (resulting in oscillation).

Since this method accurately predicts and uses actual operating power levels, then P_{AVS} does not have to be known apriori. The computer easily handles the changing NF as a function of rapidly changing source impedance near resonance since we are using actual noise generators in our modeling (not an assumed NF).

3.1 Developement of the FSK/FM hybrid oscillator (transmitter) occured with requirements in reduced size and adjustment expense. Below is one of the early circuits used for evaluation of FSK/FM SAW Resonator Oscillators.

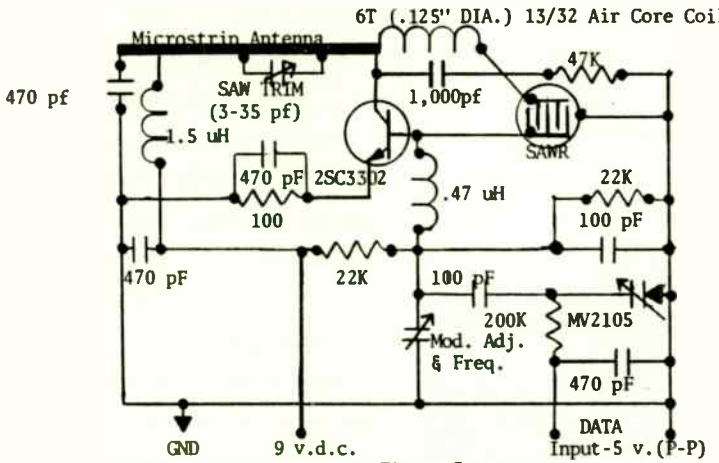
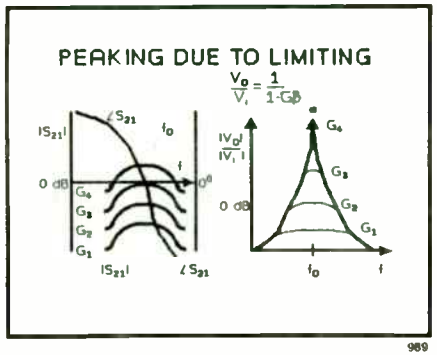


Figure 3

The circuit above was later modified so that only one adjustment is necessary to set the main frequency and the frequency deviation. In adjusting the SAW TRIM capacitor, one tends to center the main frequency too much to allow for a frequency deviation range of 90-100 kHz. The component Q and design parameters of the phasing inductors connected to the SAWR are somewhat different than expe. ted. The use of high Q coils resulted in the oscillator running intermittently i. a "free run mode" when being modulated. Reduction of coil wire size and coil size increased the pullability of the oscillator but the losses of the circuit were greater, thus requiring a different transistor bias level. The circuit components were placed in the same physical orientation as in the schematic diagram in Figure 3.

A rather basic oscillator test procedure was used: voltage variations, power supply switching, frequency and deviation amplitude measurements, etc. The most profound test was performed by placing the hand in contact with all of the oscillator components and upon removal watching the results as the preceeding tests were performed. Then the circuit was tested for maximum frequency deviation while maintaining stability, as shown in Figure 4. The object of the hand interference test is to test for oscillator recovery with and without the circuit pulled off frequency by the modulator. Variations in power supply voltage do not display the same results.

CAUTION -- The circuit involved can eventually deteriorate the SAWR and its occurance is so gradual that it is not noticed at first. Changing the bias resistors on the base circuit is necessary for better long range performance. Damage to the SAWR occured at about +18 -- 20 dBm. At about +12 dBm the centerline frequency of the SAWR used would change perhaps indicating some internal heating of the SAWR itself. The goal to obtain signal output levels of 12,333 uV/m at 3 meters with a single stage SAWR was not obtained. Therefore, a hybrid oscillator with a buffer booster stage was added to the oscillator to obtain more output and save space. Note also that marketing requirements did not allow for a separate antenna to aid in design and range requirements in the initial descrete SAWR design. Essentially the goal became almost impossible to obtain thus making it necessary to maximize all aspects of the design. Again the parameters obtained are intermediate with respect to the advantages between LC and bulk crystal oscillators. The term intermediate is used here primarily due to the manufacturing frequency tolerance of low cost SAWR devices.



989

These figures demonstrate in more detail the process which allows linear-frequency-domain computer analysis to predict closed loop phase noise. If we focus on f_0 where $\angle S_{21} = 0°$ and just modify $|S_{21}|$, then the closed loop gain becomes:

$$\frac{V_0}{V_i}(f_0) = \frac{1}{1 - G\beta} = \frac{1}{1 - |S_{21}|}$$

and we see as $|S_{21}| \rightarrow 1.0$ then

$$\frac{V_0}{V_i}(f_0) \rightarrow \infty$$

goes to infinity. Note the shape of the closed loop gain peaking at the +3 dB corner,

$$f_m = \frac{f_0}{2Q_L},$$

changes very little whether the peak is 40 dB or 90 dB or ∞. Very little is gained by focusing on very close in phase noise

$$\left(fm \ll \frac{f_0}{2Q_L}\right)$$

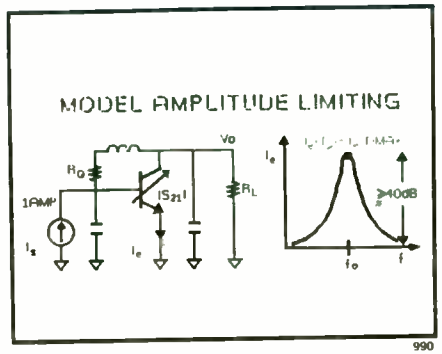
because the shape will remain a constant 6 dB/octave unless we are investigating the effects of crossing high Q spurious modes.

A basic modeling procedure for predicting parameters like phase noise, P_{OUT}, or node voltages and branch currents follows eight steps:

- choose a limiting mechanism (e.g., collector current) for modeling the oscillator. Typically, adjust $|S_{21}|$ of the active device to model the collector current cutoff limiting.
- inject a current source into any node.
- adjust the gain $|S_{21}|$ to model the limiting mechanism so that the closed-loop gain peaking is greater than 40 dB.
- monitor the emitter current at resonance during the computer analysis and scale the computer-analyzed value to the limiting current actually found or predicted in the circuit.
- scale all node voltages and branch currents by this factor. This provides output voltage, resonator voltage, and any other branch current or node voltages during oscillation.
- remove the current source and add all appropriate noise voltage and current sources.
- plot the spectral density of the output noise.
- review the ratio of the output voltage to the output noise (in a 1 Hz bandwidth) gives the predicted SNR_i, hence the phase noise:

$$\mathcal{L}(f_m) = -SNR_0(f_m) - 3\,dB \text{ (for PM only)}$$

Ref. 11



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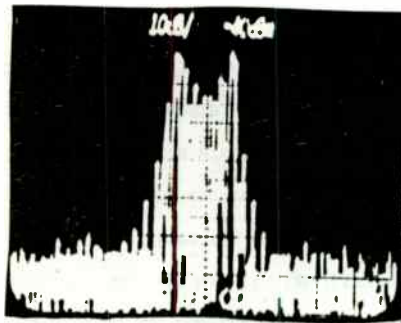
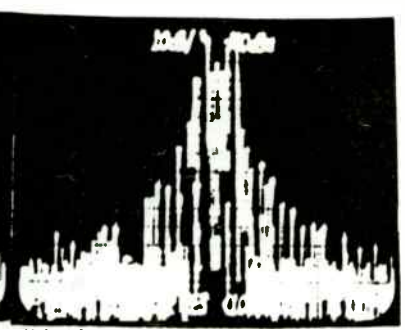
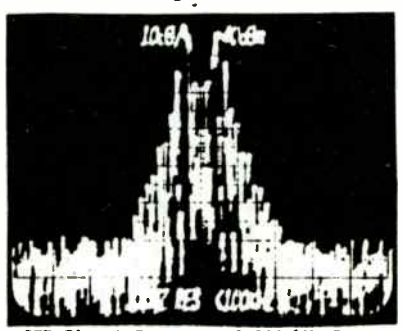
This transistor oscillator is biased for collector-current cutoff-limiting (no saturation) operation. Experience teaches us that when the transistor goes into compression then $|S_{21}|$ decreases and $\angle S_{21}$ remains approximately the same. As a result, the loop gain variation with level can be modeled through $|S_{21}|$ adjustments alone. A more sophisticated model might use full-blown large-signal S-parameters and adjust S_{11}, S_{12}, S_{21}, and S_{22} accordingly (this has not been found necessary to achieve accuracies within 1 to 2 dB).



Discrete SAWR Osc. with 180 kHz Dev.
Figure 4



Hybrid Oscillator with 100 kHz Dev.
Figure 5



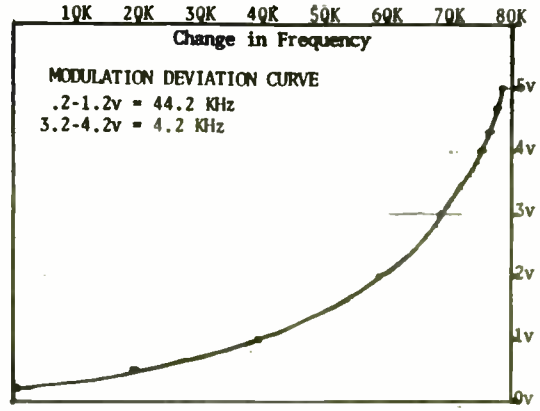
IFR Signal Generator @ 100 kHz Dev.
Figure 6

SPECTRUM ANALYSIS -- MODULATION

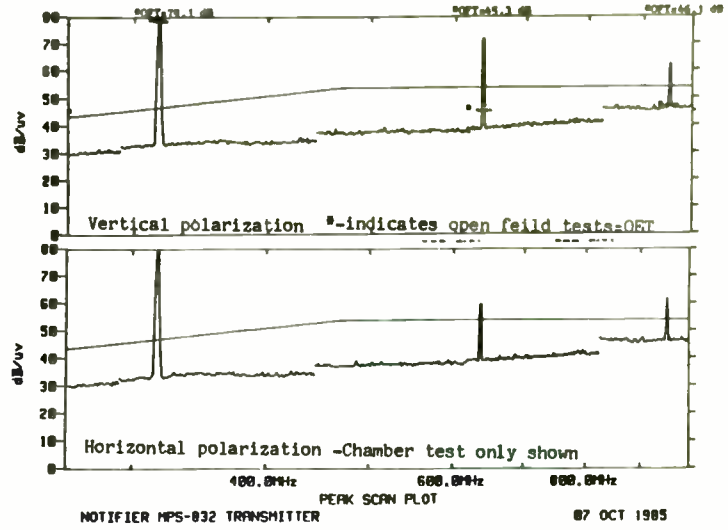
It should be noted that the SAWR manufactures recomend deviation rates of about 100 ppm and not as is shown in these figures. A typical SAWR oscillator specification sheet is on page 9. (Courtesy of RF Monolithics, Dallas, Texas)

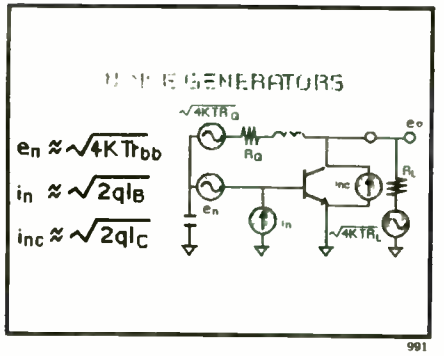
3.2 The circuit in Figure 3 was modulated with a logic (data) signal voltage of 4.6 volts = logic high and about 0.15 volts = logic low. The modulation deviation curve is shown in Figure 7. The same device could be used as a VCO local oscillator in a receiver. In this case the VCO d.c. supply did not stay stable enough over a period of time, thus a fixed SAWR oscillator is used. The particular I C used exhibited voltage reference drift that was significant.

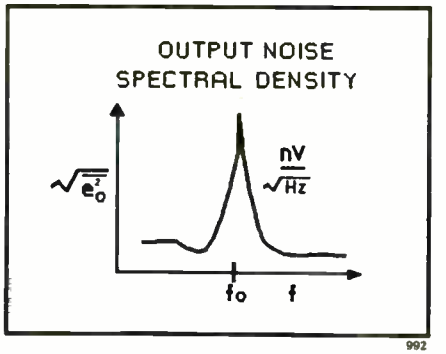
Figure 7

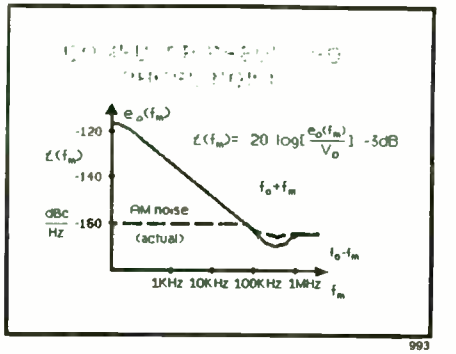


3.3 The harmonic level mentioned in Section 2.2 is somewhat varied and depends upon the output circuits. An interesting observation occured during near field measurements in a chamber @ 1 meter and open field measurements @ 3 meters, as shown in Figure 8. The asteriks designate the open field results. Also note the differences in horizontal and vertical polarization tests.









The next step in this example is to adjust $|S_{21}|$ until there is at least 40 dB peaking in output due to I_S. The exact amount of peaking is not critical, so long as

$$20 \log \frac{I_e(f_0)}{I_e(f \gg f_0)} \geq 40 \text{ dB}$$

Following this, monitor the emitter current and scale peak value of $I_e(f)$ to the actual emitter bias current, I_E

$$\text{scale} = I_E/[I_e(f)_{max}]$$

With this completed, all node voltages and branch current of interest can be predicted with

$$V_0 = \text{scale} \times V_0(f_0)_{max} = \text{output voltage}$$

$$\left.\begin{aligned} V_N &= \text{scale} \times V_N(f_0) \\ I_B &= \text{scale} \times I_B(f_0) \end{aligned}\right\} \text{ any node or branch}$$

The next step is to remove I_S, introduce all noise generators, and plot the spectral density of the output noise voltage. The computer can automatically generate appropriate noise for all lossy elements.

The use of noise current i_{nc} accounts for that component of i_n which increase as f approaches f_T ($f \gg f_\beta$).

Ref. 7, 8

Output phase noise $\mathcal{L}(f_m)$ is simply the ratio of output noise, $e_0(f = f_0 \pm f_m)$, to the output signal voltage, V_0, subtracting 3 dB for the desired phase modulation components only:

$$e_0(f_m) = e_0(f = f_0 \pm f_m)$$

$$\mathcal{L}(f_m) = 20 \log [e_0(f_m)/V_0] - 3 \text{ dB}$$

Unfortunately, this procedure gives no indication of AM noise performance. However, experience has shown that the AM noise is often within 3 to 6 dB of the phase noise floor for

$$f_m \ll \frac{f_0}{2Q_L}$$

(Courtesy of RF Monolithics)
Dallas, Texas

FIGURE 2 Typical SAW hybrid oscillator specifications

Operating Frequency:	
Fundamental output range	150 MHz to 1500 MHz
With integral multiplier	up to 6000 MHz
Frequency Tolerance:	± 10 ppm at 25° C
Temperature Stability:	Maximum operating frequency shift
Uncompensated	Less than 100 ppm for 100°C change
With integral compensation	Less than 10 ppm for 100°C change
SSB Phase Noise:	500 MHz operating frequency
at 0.1 K Hz offset	Less than − 75 dBc/Hz
at 1.0 K Hz offset	Less than − 105 dBc/Hz
at 10 K Hz offset	Less than − 130 dBc/Hz
Noise floor	Less than − 135 dBc/Hz
Power Output:	− 30 dBm to + 20 dBm
Modulation Options:	
Pulse modulation	40 dB on/off ratio standard at 50 KHz clock rate
FSK modulation	Up to 100 ppm frequency deviation at 50 KHz clock rate
Supply Voltage:	+ 5 Vdc, + 9 Vdc, + 12 Vdc ± 10% standard
Packaging:	Dual in line metal package; Surface mount metal package; Custom

Notified/ENHART at 315ppm at 2KHz Clock (also 10KHz Clock) 318MHz f_o

FIGURE 3 Free running phase noise of 567 MHz SAW resonator oscillator

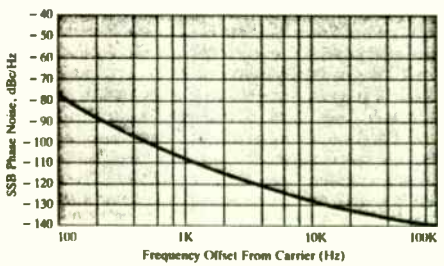
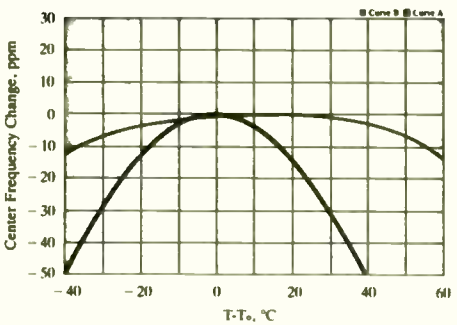


FIGURE 4 SAW Hybrid oscillator temperature performance. Curve A — uncompensated oscillator. Curve B — integrally compensated oscillator



4.0 CONCLUSIONS -- Some not so obvious SAWR characteristics -- SELECTION of SAWR

0 or 180 degrees (RS or RP) -- Depends upon active device used

1,2,3, or 4 Port -- Insertion Loss

Operating frequency note Offset PM Characteristics

Frequency tolerance

Temperature Stability of various types

2,3, or 4 Poles

Tooling Charges for new frequencies

Input and output capacitances

Unloaded Q

Turnover temperature

Bandwidth -- On FSK/FM uses

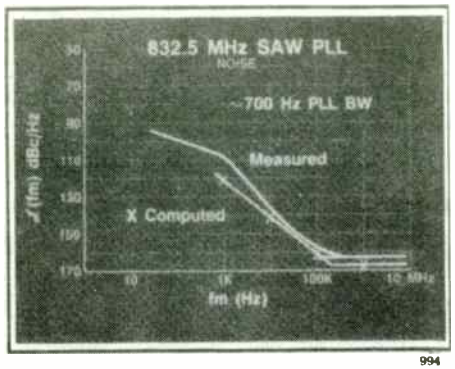
DC Breakdown Voltage

Series Capacitance -- Resistance -- Inductance

Max Power disipation (if running near limit)

There are other factors involved and awareness of the above is the purpose intended here. As an exercise, try deciding between a 0 degree and 180 degree SAWR and the benefits of each. In building an impedance inverting Pierce oscillator, one would probably use a dual gate FET and a 180 degree SAWR, only to later decide to use a 0 degree device in a hybrid circuit with a buffer stage. The point being that there are many variations in the use of SAWRs and some pre-study and planning is needed to avoid mistakes.

Sources of SAWR technology information: RF Monolithics--Dallas,TX; SAWTEK--Orlando, FL; Andersen Laboratories--Bloomfield, CT; Frequency Control Symposium; RF Design Magazine; Microwaves & RF Magazine.



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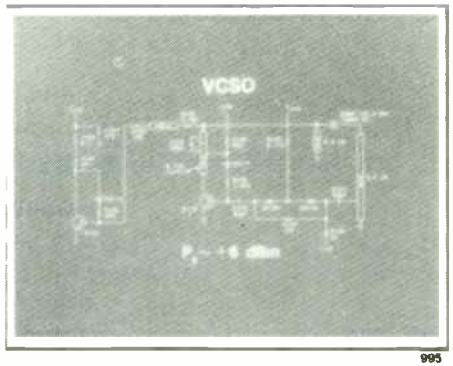

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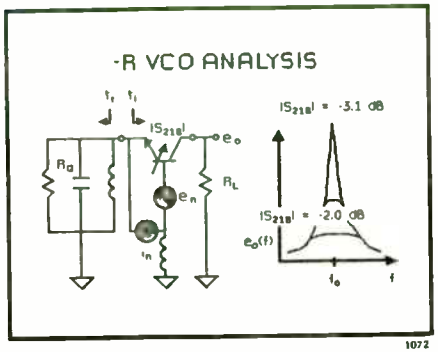

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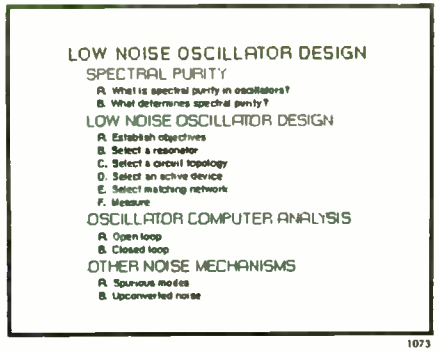

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These two figures show the computer model and a comparison of predicted results versus measured data. The computer model was even more detailed, including parasitic reactances and e_i and i_n. Small signal S-parameter data were used to model the transistors.

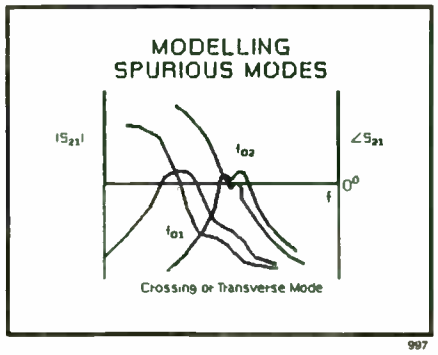
The discrepancy below 10 kHz is due to SAWR 1/f noise and PLL residual noise. The discrepancy above 100 kHz is due to noise contributions of 4 buffer-limiter stages which were not modeled; measurements in phase noise floor with the buffers removed indicate ≈ −165 dBc/Hz (computer suggests −167 dBc/Hz).

The advantages are that we have a precise and controllable experiment with which to better understand the "whys" behind the oscillator performance and predict worse case conditions.

One-port or negative resistance type oscillators may be handled similarly. The procedure involves modeling the oscillator in the manner applied to two-port oscillators, adding in all noise generators, and adjusting −R or $|S_{21b}|$.

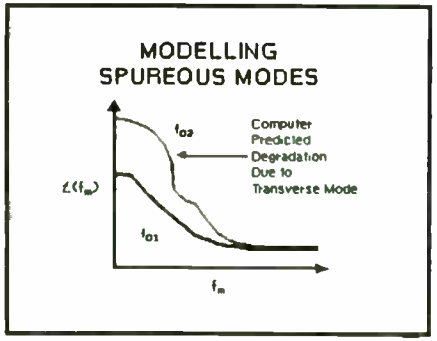
The adjustment of $|S_{21b}|$ to achieve better than 40 dB peaking can be automated if an analysis program has optimization capability. The technique requires searching for a peak near resonance and optimizing $|S_{21b}|$ for maximum peaking. It should be kept in mind that f_0 changes slightly with $|S_{21b}|$.

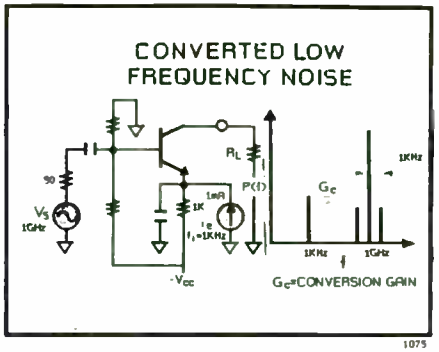
S_{21b} = common base S_{21}



Computer analysis also allows modeling spurious modes (such as transverse, crossing, and tracking modes) in a resonator (model or use measured S-parameter data). The technique consists of repeating the phase noise analysis either near (f_{01}) or coincident (f_{02}) with the undesired mode. In this way, it's possible to see the blooming effect on phase noise due to degradation in phase slope for a coincident mode, or phase noise peaking in the noise floor away from the carrier due to an adjacent mode that comes within 3 to 6 dB of the loop gain of the desired mode.

These analyses were computed from a SAWR oscillator using S-parameter data of the SAWR which has a transverse mode approximately 200 ppm above the desired mode.





A more complicated noise degradation mechanism is low-frequency noise upconverted around the carrier. Low frequency noise contributors (1/f base current noise and e_n or i_n) may cause excess emitter current noise in the audio frequency range if no attention is paid to low frequency source impedance and feedback effects. When the active device is near compression, the upconversion gain for i_e up around the carrier can be as low as −3 to −9 dB. We can measure this by injecting a low level current i_e into the emitter:

Audio upconversion gain, G_C, is

$$G_C = 20 \log \frac{i_e(1\ \text{GHz} + 1\ \text{kHz})}{i_e(1\ \text{kHz})}$$

A TRACKING IMPEDANCE MEASUREMENT SYSTEM
for Control of Tunable Networks

by
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Mgr, HF Filter/Coupler Group
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Rockwell International Corporation
Cedar Rapids, Iowa 52498
January 1986

ABSTRACT

Applications for advanced design, tunable, HF impedance matching networks and filters require accurate impedance measurements. This paper describes a Tracking Impedance Measurement System (TIMS) which provides capability for actual in-line impedance measurements. For comparison, a conventional phasing-loading discriminator provides only relative magnitude and phase angle measurements based on a reference impedance. The TIMS operates over a wide power range in the HF band yet generates virtually no noise or spurious signals. Digital outputs are updated rapidly and may be used to calculate impedance, reflection coefficient, and VSWR in real time. These features permit performance of remote impedance measurements. The TIMS also provides selectivity to reduce errors due to interfering signals.

INTRODUCTION

Impedance networks are used for antenna couplers (matching networks) and filters in the high frequency range. Figure 1 shows simplified examples of a typical antenna coupler circuit and a bandpass filter (BPF) circuit. Fixed tuned impedance networks are used for applications in which only one frequency is used such as broadcast transmitters. For applications requiring the use of several frequencies, adjustable or tunable impedance networks are needed. Manually adjustable impedance networks were used for many years and are still used for applications which require infrequent retuning. Applications requiring many frequency changes or rapid retuning use automatically tunable impedance networks.

Automatic tuning of an impedance network requires a control system and a sensing device. The control system may be a closed loop analog servo control system or a digital control system. In either case a sensing device and tuning criteria are needed. In this presentation I will be primarily discussing sensing devices. I will first review the function, application, and limitations of the conventional Phasing-Loading discriminator. I will then present a new concept in sensors for automatic tuning systems called a Tracking Impedance Measurement System (TIMS) which I will call TIMS for short. I will discuss the

The phase noise in amplifiers due to low frequency noise $i_{ne}(f_m)$ is then

$$\mathcal{L}(f_m) = 20 \log \frac{i_{ne}(f_m)}{I_e(f_0)}$$

$$-3 \text{ dB} + \text{upconversion gain}$$

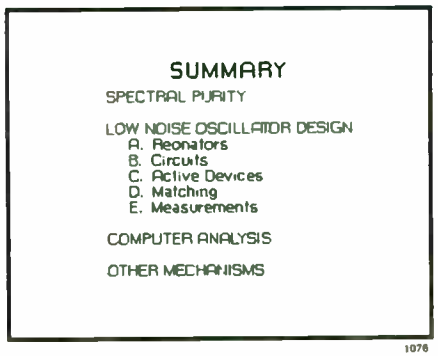
and in the oscillator add the peaking

$$\mathcal{L}(f_m) = 20 \log \frac{i_{ne}(f_m)}{I_e(f_0)}$$

$$-3 \text{ dB} + G_C + 10 \log\left[1 + \left(\frac{f_0}{2Q_L f_m}\right)^2\right]$$

To prevent these problems analyze via computer the emitter current noise spectral density of the oscillator and all buffer chains from DC to beyond f_0. Typically, the noise floor due to this mechanism should be 10 dB lower than the specification limit of that contributed by the oscillator.

There appears to be at least two kinds of 1/f noise in transistors: (1) upconverted 1/f component of base current noise; (2) 1/f phase modulation of the RF signal through the transistor. The reason these components seem separate and distinct is that component (1) should be level dependent since it is upconverted by a nonlinear mixing process. Our measurements show that the 1/f PM of active devices remain virtually constant over a significant range of RF power (from limiting to well inside the linear active region [small signal]). Also measuring the 1/f base current noise and the upconversion coefficient we find that the actual residual 1/f phase noise of the amplifier is 20 to 30 dB greater than hat predicted by upconversion.



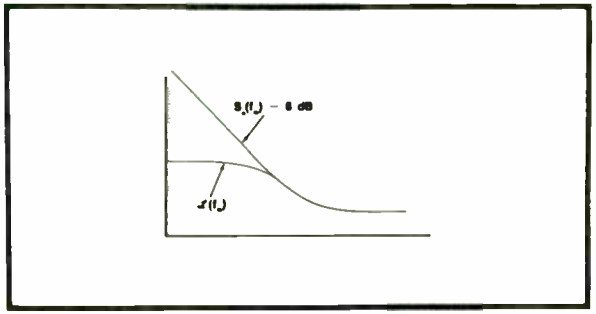
In summary some of the causes of phase noise in oscillators and what to do about them were discussed. The effects of resonator Q, resonator and device 1/f noise, and AM-FM conversion on phase noise were discussed. Oscillator topologies and active devices were looked at. Coupling to resonators and coupling to loads and their effects on noise were examined. Methods of measuring and computer modeling the causes of noise in oscillators were discussed. And lastly, mention was made of other mechanisms that can cause noise.

Appendix 1

$\mathcal{L}(f_m) = 20 \log \frac{\Delta\phi}{2}$ narrowband FM approximation

$$\left.\begin{aligned} L(f_m) &= \frac{S_\phi(f_m)}{2} \\ \mathcal{L}(f_m) &= S_\phi(f_m) - 3 \text{ dB} \end{aligned}\right\} \text{ for } \Delta\phi_{total} \ll 1$$

In this article we have assumed $\mathcal{L}(f_m) = S_\phi(f_m) - 3$ dB everywhere for simplicity. Actually as we approach the carrier $\mathcal{L}(f_m)$ flattens out:



Reason: $\mathcal{L}(f_m)$ is the power in 1 Hz band centered f_m Hz off the carrier due to PM divided by total signal power. This is what we would see on a spectrum analyzer with a 1 Hz B.W. if reference level (0 dB) was the total signal power.

$S_\phi(f_m)$ is the phase spectral density or $20 \log \Delta\phi^2(f_m)$ in the 1 Hz B.W. Here's a simple example which may clarify:

for $\Delta\phi > 1$ radian

Signal: $V(t) = \cos(\omega_C t + 10 \sin 2\pi\ 10^3 t$ or carrier with $\Delta f = 10$ kHz

fm = 1 kHz; $\beta = 10$ = mod index

function, operation, and application of the TIMS.

The TIMS was invented by Mr. Harvey L. Landt of Collins Defense Communications, Rockwell International Corporation, Cedar Rapids, Iowa. Mr. Landt holds United States Patent No. 4,506,209 issued March 19, 1985 for the TIMS. Full credit and acknowledgement is given to Mr. Landt for this design and for his assistance in the preparation of this paper.

CONVENTIONAL PHASING-LOADING DISCRIMINATOR

Tuning criteria which have been used in the past for manual adjustment of impedance networks are not easily adaptable to automatic tuning control systems. For example, finding minimum current or voltage, maximum current or voltage, or minimum reflected power are criteria that may be used in a manual tuning system, but are not easily adapted to automatic tuning systems. Figure 2 shows typical sensor signals versus tuning element position. In 2(A) a minimum is to be detected and in 2(B) a maximum is to be detected. In either case the sensor signal or error voltage is always of the same polarity and cannot be detected with a zero seeking closed loop servo control system. Figure 2(C), however, shows a sensor signal which passes through zero at the tune point and has opposite polarity on either side of the tune point. This signal can be used with a zero seeking servo control system and the system will be stable at the tune point. The conventional Phasing-Loading Discriminator provides this type of error signal.

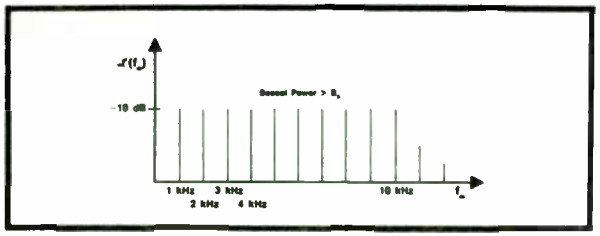
FUNCTIONAL DESCRIPTION

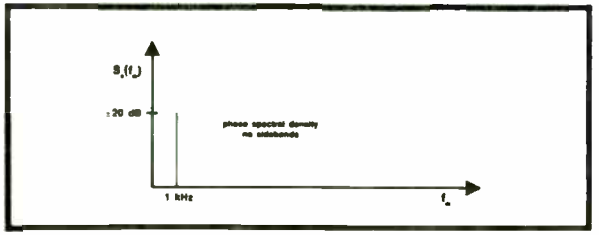
The conventional phasing-loading discriminator is placed in series with the RF transmission line at the point tuning information is desired. This is usually at the input of an antenna coupler or filter. It contains two error sensing circuits, one for phasing and the other for loading.

The phasing circuit shown in Figure 3 combines RF voltage and current samples vectorially , rectifies the vector sums, and combines the DC voltages to provide a DC output error signal. This error signal is a function of the phase angle between the transmission line voltage and current. The phasing circuit is adjusted to provide an error signal of zero volts when the phase angle is zero. A positive DC error signal may indicate the phase angle is inductive and a negative DC error signal would then indicate the phase angle is capacitive. In either case the magnitude of the error voltage is a function of the phase angle magnitude, but it is not necessarily proportional.

The loading circuit shown in Figure 4 rectifies the individual voltage and current samples and then combines the DC voltages to produce a DC output error signal. This error signal

Appendix 1





$\phi(t) = 10 \sin 2\pi\ 10^3 t$ no harmonics

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is a function of the impedance magnitude. The loading circuit is adjusted to provide an error signal of zero volts when the impedance magnitude is the desired tuned impedance, usually 50 ohms. A positive DC error signal may indicate an impedance magnitude greater than 50 ohms and a negative DC error signal would then indicate an impedance magnitude less than 50 ohms. In either case the magnitude of the error voltage is a function of the ratio of the actual impedance magnitude to 50 ohms, but it is not necessarily proportional.

The combination of the phasing and loading circuit response is shown in Figure 5 using a Z-plane which is a graphical representation with rectangular coordinates plotted as (R,jX). Note there are four basic zones separated by the R axis and the |Z| curve. The phasing and loading discriminators individually provide directional and speed control error information for a zero seeking servo control system for one of the reactive tuning elements. With appropriate logic control and servo gain and stability circuits the reactive elements can be positioned so the impedance at the discriminator location is 50 + j0 ohms.

APPLICATIONS AND LIMITATIONS

The phasing-loading discriminator is used primarily with analog servo control systems. Many automatic tuning antenna couplers have been designed and produced with this type control system in the past 30 years for use on aircraft, land vehicles, transportable shelters, shipboard, and submarines. Also automatic tuning bandpass filters have been designed and produced for many applications including high power filters for shipboard multicouplers. The phasing-loading discriminator has also been used in the last several years with automatic digital tuning control systems for antenna couplers.

Some important limitations of the phasing-loading discriminator are:

1. Not calibrated for impedance measurement
2. Susceptibility to interfering signals
3. Diode noise
4. High RF power level required

Impedance Measurement

The accuracy of the DC output signal voltage from the phasing or loading discriminator is affected by several factors such as RF power level, diode characteristics versus frequency, and sampling circuit characteristics versus frequency. Therefore the phasing and loading error signals cannot be calibrated to enable accurate impedance measurements. Referring again to Figure 5 only relative impedance information is available as described by the four zones on the graph. For example at point A, the impedance magnitude is greater than 50 ohms and the phase angle is inductive. At point B the impedance

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LIST OF SYMBOLS

f = offset frequency

FM = frequency modulation

AM = amplitude modulation

S- = scattering parameters

Q_L = loaded Q

SAW = surface acoustic wave

P_{avs} = power available from source (resonator) in Watts

$P_{AVS} = 10 \log P_{avs} + 30$ dBm

Po = output power

CE = common emitter

CC = common collector

CB = common base

Γ = reflection coefficient

ϕ = angle of loop gain

LIST OF SYMBOLS

K_v = VCO gain: Hz/Volt

τ_{GD} = group delay

I_E = emitter dc bias current

I_c = collector dc bias current

I_e = emitter AC signal current rms

f_0 = frequency of oscillation

i_{nc} = collector noise current in $A_{rms}/\sqrt{Hz}$

i_{ne} = emitter noise current in $A_{rms}/\sqrt{Hz}$

$\mathcal{L}(fm)$ = single sideband power in a 1 Hz bandwidth (due to phase noise) referred to signal power in dBc/Hz (see Appendix II)

SNR_i = signal to noise (1 Hz BW) referred to input in dB =

$$10 \log \frac{P_{avs}}{FkT}$$

L(fm): $\mathcal{L}(fm) = 10 \log L(fm)$

NF = 10 log F = noise figure in dB

F = noise factor

e_0 = output noise voltage in volts rms/$\sqrt{Hz}$

G = active device gain

r_s = source resistance

f_T = current gain-bandwidth

K_v (AM/FM) = VCO gain due to AM-FM in Hz/%AM

$\mathcal{L}(f_m)_{OL}$ = open loop phase noise

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magnitude is less than 50 ohms with a capacitive phase angle. Thus only coarse logic decisions can be made to aid the control system to adjust the tuning elements for the tune point.

Susceptibility

The conventional discriminator provides no selectivity for rejection of interfering signals conducted from the antenna through the antenna coupler to the discriminator (back door interference). Interfering signals at a different frequency coupled to the antenna from other nearby transmitting antennas can thus cause the antenna coupler to mistune.

Diode Noise

The rectifier diodes in the conventional discriminator can cause noise to be transferred to the RF transmission line. This is an important consideration for low noise transmitter systems.

Power Level

The voltage and current samples must be lightly coupled to the transmission line to minimize power loss and alteration of the transmission line impedance. Light coupling results in small sample voltages. The RF power level must be high enough so the sample voltages can sufficiently overcome the diode voltage drop and provide the necessary sensitivity for the servo control loop. The required RF power level for the conventional discriminator is usually in the 100 watt to 200 watt range.

TRACKING IMPEDANCE MEASUREMENT SYSTEM

The Tracking Impedance Measurement System or TIMS was developed to overcome the limitations of the conventional phasing-loading discriminator.

FUNCTIONAL DESCRIPTION

The TIMS shown in the block diagram of Figure 6 is an impedance measurement system consisting of a directional coupler, discriminator stage one, discriminator stage two, an A/D converter, and an I/O device.

The directional coupler is placed in series with the transmission line at the point impedance measurements are desired. It provides forward and reflected RF voltage samples to the discriminator stages. From the forward voltage sample, an injection signal is derived which tracks the signal from the signal source but is offset by 10 kHz. The injection signal is then used to convert the forward and reflected voltage samples to 10 kHz signals which are representative of the original voltage samples. The frequency of the converted signals is constant at the offset frequency of 10 kHz, regardless of the operating signal frequency. These constant frequency signals are filtered to provide selectivity and processed with low frequency circuits to derive voltage analogs of the forward

voltage, reflected voltage, and phase angle between them. These three voltage analogs are supplied to the A/D converter. An I/O device such as a microprocessor can then use the digital form of the forward voltage, reflected voltage, and phase angle to calculate the reflection coefficient, impedance, and voltage standing wave ratio (VSWR).

The TIMS overcomes the limitations previously noted for the phasing-loading discriminator.

Impedance Measurement

The TIMS automatically tracks the signal frequency and provides accurate impedance measurements rapidly when the signal frequency is changed.

Susceptibility

The TIMS provides selectivity to reject interfering back door signals.

Noise

The directional coupler contains no noise sources. It provides 30 dB of isolation between the transmission line and possible noise sources in the discriminator stages.

Power Level

The discriminator stages operate with low level signals. With appropriate signal attenuators between the directional coupler and the discriminator stages, the TIMS can provide accurate impedance measurements even with the forward power level as low as 10 milliwatts.

OPERATIONAL DESCRIPTION

Directional Coupler

The directional coupler is a balanced bi-directional assembly which provides an RF forward voltage sample and an RF reflected voltage sample. Approximately 30 dB isolation is provided between the transmission line and the voltage sample output. The directivity is greater than 40 dB. For example if the directional coupler is terminated with a 50 ohm resistive load with a forward power of 100 watts, the reflected voltage sample will erroneously indicate a reflected power of 10 milliwatts or less. The resulting VSWR error is less than 1.02:1.

Discriminator Stage One

The block diagram for discriminator stage one , which is essentially a dual channel receiver, is shown in Figure 7. The forward voltage sample is applied via a fixed attenuator to an automatic gain control (AGC) circuit which is part of the forward voltage channel. The AGC circuit controls the signal level of both the sampled forward voltage and the sampled reflected voltage. The AGC circuit in the forward voltage channel includes an electronically variable attenuator and an RF amplifier, the combination of which comprises a variable gain

Broadband GaAs Monolithic Amplifiers and Their Applications

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Introduction

NEC has recently introduced three new low cost broadband MMICs designed for medium power, low noise, and gain block applications. Each MMIC is a cascadable, multi/octave, 50 ohm device. Typical bandwidths are from 50 MHz to 3GHz with NF as low as 2.7 dB for the UPG100 and high linear power of 20 dBm for the UPG101. The third device is the NEPA1001 which is a general purpose GaAs MMIC which is similar to the UPG100 except with a higher noise figure.

Application of these amplifiers is limited only by the designers imagination. These devices are relatively simple to use, but their wide bandwidths and high fmax require care and good design technique. It is our intent to help the designer who may not be totally familiar with using these devices.

Performance Specifications: 50 to 3000 MHz

		NEPA1001*			UPG100			UPG101		
Item	units	min	typ	max	min	typ	max	min	typ	max
Linear Gain	dB	10/12		15	16			14	16	
Flatness	±dB			1.0/1.5	1.0	1.5		1.0	1.5	
Noise Figure	dB		4/4.3	4.5/5		2.7	3.2			5.5
Power Out	P1dB	7	9		3	6		17	20	
Isolation	dB	35	40		30	40		30	40	
Input R.L.	dB	6	10		7	10		7	10	
Output R.L.	dB	10	16		10	13		10	13	
Idd	mA	40	60	80	30	45	60	70	100	160
Vdd			5			5			8	
Igg	mA		4	5		0.7	1.5		1.1	3.0
Vgg			-5			-5			-5	

* NOTE: These parameters are divided into two frequency bands; .1 - 2 GHz and 2 - 3 GHz.

Fabrication of the NEPA1001

The NEPA1001is a two stage GaAs MMIC broadband amplifier using FETs with a closely spaced electrode structure. The devices are fabricated by self-alignment technology using Al side-etching techniques to obtain reproducibility of the spacing between the drain to gate and the source to gate electrodes. As a result, these spaces are reduced to .4 micron. Resistance is reduced in both electrodes and results in a cutoff frequency of 18 GHz. This process is unique in its utilization of ion-implantation. The FET's active layers are formed by using silicon

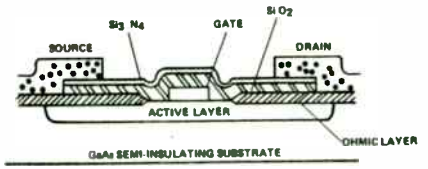


Fig. 1

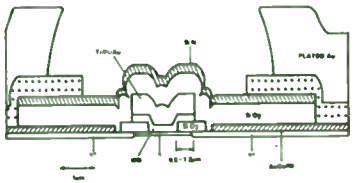


Fig. 1B

ion-implantation into a semi-insulating GaAs substrate. These implanted layers are then annealed in a hydrogen atmosphere. All metalizations on the chip are defined by using dry-etching technology. Combining these fabrication techniques results in a highly reproducible GaAs MMIC.

Fabrication of the UPG100 and UPG101

The UPG100 and UPG101 are also two stage broadband MMIC amplifiers. Fabrication of these devices is slightly different than the NEPA1001. The UPG series amplifiers employ a FET structure which has a tungsten silicide (WSI) offset gate instead of the closely spaced elecrtrode structure. Otherwise the same general process are used for both series of amplifers. The tungsten silicide structure was chosen to improve durability of the devices as well as improve yield and manufacturability. The tungsten silicide process uses what is typically known as a T gate. This process allows the deposition of other metals (Ti, Pt, Au) on top of the tungsten silicide Schottky gate. As a result, higher conductivity is possible, providing improved overall performance. Presently, this process lends itself better to MMIC fabrication than the close electrode structure. The close electrode structure features side wall etching to achieve short gate lengths. This process does work well, but is more difficult to control for complex devices. Another advantage of the WSI technology is improved protection against electrostatic discharge.

Circuit Configuration

The configuration for the UPG100 and 101 are nearly identical. The UPG100 is the low noise version and differs mainly in the type of FETs used. The first stage uses a gate width of approximately 1000 microns to improve the input return loss. The second stage uses a device that is about half the gate width of the first stage for improved output return loss. Both devices have gate lengths around .8 micron. One would expect a low noise device for the input which is typically a smaller device. Since smaller FETs exhibit a somewhat higher impedance than larger devices, a larger FET was chosen to simplify the required input matching circuitry.

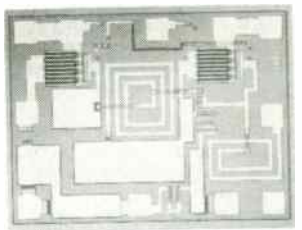


Figure 2

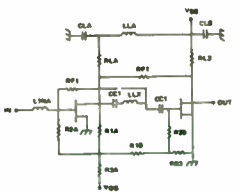


Figure 3

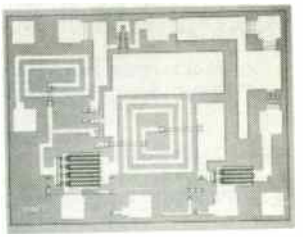


Figure 4

amplifier. The output of the variable gain amplifier is applied to another RF amplifier and then to an RF detector and bias amplifier which converts the sample forward voltage signal to a variable amplitude DC signal which is used to adjust the variable attenuator. This automatic gain control maintains the voltage level and provides a signal at the output of the variable gain amplifier which is representative of the forward power applied to the directional coupler. The combination of the fixed attenuator, the variable attenuator, and the directional coupler isolation reduce the signal to the appropriate level for the discriminator circuitry. The variable attenuator is automatically adjusted over a 56 dB range for proper operation of the discriminator with variations of the power level at the input to the directional coupler.

One output of the forward voltage channel variable attenuator circuit is an RF sample which is applied to discriminator stage two for generation of the injection signal. The injection signal is applied back to discriminator stage one where it is applied to a power splitter. One output from the power splitter is mixed with the forward voltage signal output from the variable attenuator. The output of the mixer is a 10 kHz signal which is applied to a low pass filter which passes 10 kHz. Signals above 30 kHz are terminated via a high pass filter and a resistor. The output of the low pass filter is applied to a fixed gain amplifier and then to a bandpass filter which passes 10 kHz. The signal is then rectified by a full wave rectifier to obtain the output signal EF which is a DC voltage analog that represents the voltage of the forward power applied to the directional coupler.

The reflected voltage channel also includes an electronically variable attenuator which is controlled by the AGC circuit. The operation of the reflected voltage channel is identical to the forward voltage channel operation with one exception. In the reflected voltage channel a dual gain amplifier is used between the low pass filter and the bandpass filter. When the circuit is initially used and there is a substantial amount of reflected voltage sampled by the directional coupler, then the low gain setting of the dual gain amplifier is utilized. However as the impedance network being tuned approaches the tuned condition, then the reflected sample decreases and to provide an accurate measurement, the high gain setting of the dual amplifier is used which essentially expands the scale of the reflected voltage measuring circuit. The output signal ER is a DC voltage analog that represents the voltage of the reflected power existing at the directional coupler.

The phase angle between the forward voltage and reflected voltage output signals from the respective bandpass filters is

The UPG101 uses 2 larger 1000 micron FETs for both the input and output. The larger output device is the key to the higher output power. Normally, drain currents over 60 mA are very difficult to control using internal bias circuitry. To overcome this problem, an external RFC is required to supply bias to the final stage. Even though the internal drain resistor is bypassed by an external RFC, it still serves two functions. The first is to improve output VSWR and secondly it provides improved circuit stability from high impedance loads. Failure of the RFC will not damage the device. If Vdd is lost to the choke, the drain current will be about half. At this current level the internal resistor can still safely dissipate the power.

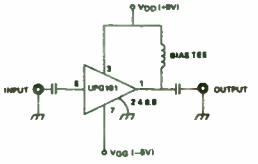


Figure 5

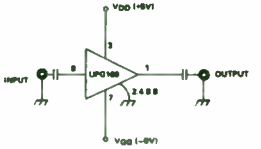


Figure 6

Since the UPG100 has a typical drain current of only 45 mA, internal bias is used and therefore an external choke is not required.

A slightly different configuration is the NEPA1001. As shown below, feedback is achieved from the drain of the first stage. The NEPA1001 is a gain block, but can be used in other applications. A low noise figure was not a design goal for this amplifier. Using this amplifier is similar to using the UPG100 in that an external RFC choke on the output is not required.

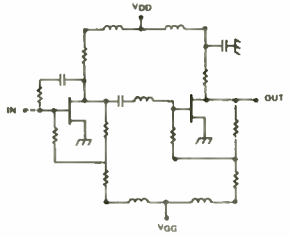


Figure 7

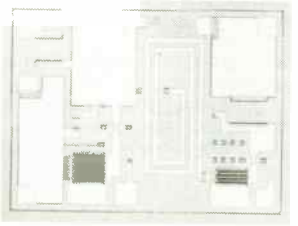


Figure 8

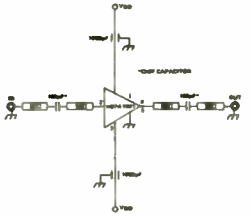


Figure 9

Unfortunately, nature's limitation to the amount of capacitance which can be achieved on GaAs necessitates external blocking capacitors. External blocking capacitors should be of good quality with low ESR and minimal parastics.

One should consider these capacitors as a series RLC network and keep in mind that their physical size could be too large at 3 GHz. Capacitors other than chip capacitors are not recommended. Leaded capacitors will have too much parasitic reactance. This will either degrade the overall performance of the amplifer or result in unexpected oscillations.

The low frequency performance is also limited by the available capacitance. The internal stages inside these amplifiers are not DC coupled. They all have a blocking capacitor to provide DC isolation in between the stages. This capacitor only serves to block DC. Peaking is provided by the inductor in between the two blocking capacitors. The other critical reactance is Cgs of the following stage. Together L and Cgs achieve a dominant pole slightly beyond 3 GHz. Unfortunately the inductor takes a lot of room also; thus complete peaking is not achieved. Typcial values for the blocking capacitors and peaking inductor are listed below.

	NEPA1001	UPG100	UPG1001
C1:	20 pf	25 pf	25 pf
L1:	3.2 nh	3.2 nh	3.2 nh
C2:	-	8 pf	10 pf

The internal blocking capacitors are the limit of the low frequency response of around 50 MHz. When using caspacitors in MMICs, the low frequency limit is a difficult problem due to the amount of space these elements require.

Digitizing the Amplifiers

These amplifiers will not perform as well as DC coupled amplifiers for digital data. This type of amplifier will distort a digital waveform. Distortions can be seen as poorly defined peaks and valleys in a 1.2 gigabit NRZ stream. Typical bandwidths required to overcome this problem are approximately 100 KHz to 1.6 GHz and up. The limitation lies mainly in the low frequency limit of the amplifier. The upper limit defines the maximum data rate the amplifier can reproduce. At this time NEC is developing a new AGC amplifer which will be suitable for high speed digital data.

Application of the UPG100 and the NEPA1001

Simplicity is always desired in any circuit. These devices require only a few external components. As with any RF circuit, good grounding technique (up to and including microwave frequencies) is of primary concern. Ground loops are traps which have left even the best of designers in a frenzy. Make sure that the ground point is really a ground and not some reactance to ground. Using a few extra plated through-holes may be expensive for board processing, but will prove to be of great value in achieving good performance. These amplifiers have considerable gain well beyond 3 GHz. The user may only intend to use the device to 2 GHz, but the grounding should be sound beyond 3 GHz. A simple test for ground loops is to note S21 of the device. If steep and abrupt responses or oscillations occur, assume grounding problems exist. We have tested quite a number of these devices and found that the response is somewhat smooth. By touching the ground plane one should not expect any changes in the response. If any changes occur, most likely there's a grounding problem. The solution to this is usually simple for a new circuit; either add more plated through-holes or relocate them. With old circuits, one can add

obtained by the phase comparator. Each channel bandpass filter output is applied to a zero cross detector that senses every time the alternating current signal crosses the zero voltage potential. The outputs of the two zero cross detectors are logic signals and are compared by a phase detector which provides a signal whose length in time represents difference in occurence of an output pulse from the two zero cross detectors. The output of the phase detector is filtered and amplified and provided as output signal "theta" which is a DC voltage analog representing the phase angle between the voltage of the forward power and the voltage of the reflected power which exists at the directional coupler.

Discriminator Stage Two

The block diagram for discriminator stage two is shown in Figure 8. The RF sample previously derived by discriminator stage one is applied to discriminator stage two and is used to generate the injection signal. The injection signal is a single sideband signal that tracks the input RF signal that is applied to the directional coupler but is offset from that input signal by 10 kHz.

The RF sample is applied to a variable gain amplifier whose output is varied by the injection signal and then applied to a power splitter. One output of the splitter is applied to a buffer amplifier, an output amplifier and pulse shaper, and a divider which divides the signal by 100 to provide the signal VRF which may be used by a frequency counter circuit to determine the input signal frequency. The second output of the power splitter is applied to a buffer amplifier and then to a signal sideband generator.

The single sideband generator uses a phase difference technique to generate the RF injection signal. The output of the buffer amplifier is applied to a broadband 90 degree RF splitter which provides an in-phase signal and a quadrature signal. The in-phase signal is applied to an in-phase mixer where it is mixed with a signal that is provided by a 10 kHz oscillator via the in-phase terminals of a 90 degree audio splitter and a 10 kHz bandpass filter and driver. The quadrature phase signal from the RF splitter is applied to the quadrature phase mixer where it is mixed with a signal that is provided by the 10 kHz oscillator via the quad-phase terminals of the 90 degree audio splitter and a 10 kHz bandpass filter and driver. The outputs of the in-phase mixer and the quadrature phase mixer are combined and the result is applied to an RF output power amplifier which provides the drive power for the injection signal. The injection signal is applied to an RF detector and bias amplifier to generate the signal to control

self-tapping screws that either add more grounding points or knock out the hot spots. Keep in mind that RF currents flow on the outside of the conductors. Transitions can be tricky. Try to choose a ground as close as possible to common to both the ground of the device and the ground of the circuit. Critical ground pointsin this case will be at the connectors and directly below the grounds of the amplifier or bypass capacitors. Having an extended path will introduce an additional reactance in series to the ground circuit. In active devices, this usually results in negative resistance. Under the right conditions, oscillations could result. Below are two circuits, one which we found acceptable, and one which was unacceptable.

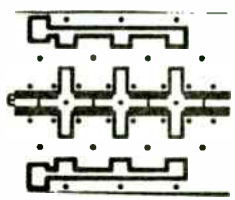


Figure 10 - GOOD

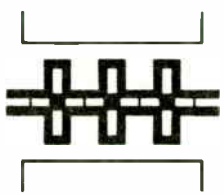


Figure 10A - BAD

Single Stage Operation - NEPA1001

The NEPA1001 is available in two types of packages. The AA package is a can type, and the FA is a hermetically sealed ceramic flat pack. The flat pack is straight forward and is a surface-mountable amplifier on microstrip. Two opposing leads are used to supply +Vdd and -Vgg. Orthogonal to those leads are another set of opposing leads which are the input and outputs. The back side of the package is the ground.

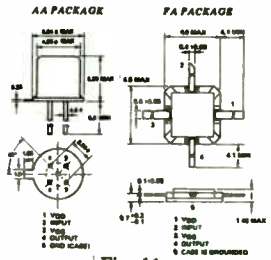


Fig. 11

Mounting of the FA package requires soldering the back side of the device. This can be accomplished in many ways and will most likely vary from one application to another. We tried two methods. One was using a device that was heat sunk to a brass block and the other was to cut a hole in the PC board to pick up the ground from the back side of the board.

The FA package was mounted on a brass block by first mounting the circuit with precut holes for the MMICs on to that block. Next the device and its location was pretinned with 93 degree low temperature solder. This solder was chosen mainly because it was available within our lab, and could have been substituted for a higher temperature. The only constraint was to choose a solder that would not require the back side of the MMIC to exceed about 230 degrees C. since the chip is die-attached by eutitic Au-Sn solder. Then the device was carefully dropped into place after the solder started to wet by applying a light pressure by hand through the eraser of a pencil. When the block cooled below the liquid phase of the solder, we carefully removed the pressure. The device has be firmly in place. Finally the last step was to solder the leads. Maximum temperature for this operation is 260 degrees C for no more than 10 seconds.

Our second approach was considerably easier, but has the disadvantage of poor thermal dissipation. This method should not be used for the previously mentioned UPG amplifiers. We started by cutting a hole for the device into the PC board. The device was then dropped into place with its leads flush with the top side of the board. The thickness of the board was chosen so that the back side of the device would be flush with the ground plane. Lastly, the back side of the device was soldered to the circuit board ground plane by regular 60/40 solder.

Mounting of the canned version or AA package is like that of a general purpose transistor. It is important to note that the case is the amplifier ground. This amplifier is also configurable for self biasing.

Self-Biasing the NEPA1001

NEC has suggested the following method for self-biasing. Since we must self bias two voltages (Vdd and -Vgg), a total of 10 volts is required. The ground must be RF ground regardless of its DC voltage level. This is accomplished by bypassing RF to ground through at least three 1000 pf chip capacitors. Single positive supply operation is realized by pulling up the potential of the ground against the Vgg terminal.

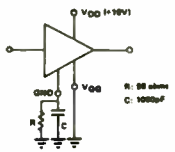


Figure 12

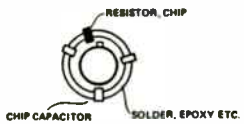


Figure 13

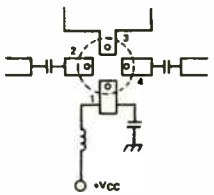


Figure 14

Negative self-biasing is also possible with the NEPA1001 by pulling up the ground terminal against the Vgg terminal (-10 volts).

the variable gain amplifier. The injection signal is applied to discriminator stage one as previously described.

A forward power sample derived from the RF forward voltage sample output of the directional coupler is applied through an RF amplifier to an RF detector. The detected signal is applied to a threshold comparator whose output digital signal FFP will indicate whether enough power is present at the directional coupler to appropriately operate the TIMS and the equipment which is being tuned.

CONSTRUCTION

The directional coupler is constructed in a metal chassis. Type N coaxial connectors are used for the transmission line connections which must conduct up to 2000 watts PEP. Type TNC coaxial connectors are used for the forward voltage sample and reflected voltage sample outputs to prevent misconnection of the high power input signal to these low power outputs. Coaxial transmission lines, shielded compartments, toroidal coupling coils, and layout techniques are used to minimize stray coupling and enhance accuracy.

Discriminator stage one is built on one printed circuit card using shielded compartments to isolate the various stages of the circuitry and control electromagnetic interference (EMI). The forward voltage and reflected voltage channels are constructed with nearly identical component layouts considering the small variations between their circuits. Special care is taken to keep the two variable attenuators nearly identical with small tolerance components so their output voltages will accurately track with each other for variations in the input power to the directional coupler.

Discriminator stage two is built on a second printed circuit card with similar shielded compartment construction.

APPLICATIONS

The first application of the TIMS was in a shipboard antenna coupler group designed to solve shipboard simultaneous operation (SIMOP) problems. Currently the TIMS is being incorporated into the design of an aircraft antenna coupler group to solve aircraft SIMOP problems. The TIMS could have applications in many advanced antenna coupler or filter developments.

SHIPBOARD APPLICATIONS

The Problem

To describe the shipboard application, I will first discuss the problem which the shipboard antenna coupler group solves. Figure 9(A) illustrates the SIMOP problem that exists when transmitting antennas are closely spaced (collocated) due to

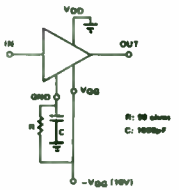


Figure 15

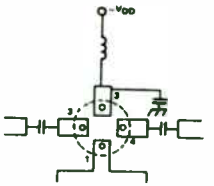


Figure 16

The required resistor for achieving self-biasing can be found by simply applying Ohm's law (remember we want to drop 5 volts):

$$R = \frac{5 \text{ volts}}{Idd}$$

In both cases a resistor value of 90 ohms is required for an Idd = 55 mA.

Self-Biasing the UPG100

Treatment of the UPG100 is schematically the same as the NEPA1001. Packaging is quite different from the NEPA1001 and requires a similar but slightly different approach. The UPG100 is an 8-pin flat pack. Input and output pins are opposite to each other. Orthogonal to those pins are 3 opposing sets of leads. In the center of each set of 3 leads are the bias supply lines (Vgg and Vdd). The outer leads are the grounds. By applying the same techniques for choosing the bias resistor for the NEPA1001, one can pull up or down the voltage for either positive or negative supplies. One should also ground all four corner leads with chip capacitors of 1000 pf or larger.

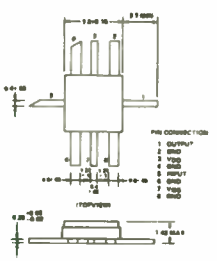


Figure 17

Remember that the bottom of this amplifier is not at ground potential relative to the circuit. Either provide a pad for all 4 leads and the back side, or prevent the DC ground of the device from coming in contact with the circuit ground. Below is the "H" shaped ground pad that we used to isolate the circuit ground from the amplifier ground. Chip capacitors were located, after the device was installed, at each leg of the "H" pad to the circuit ground.

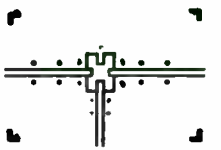
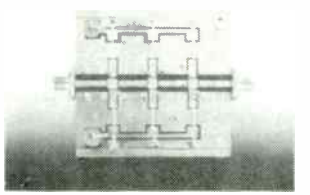


Figure 18

Cascading

Cascading these devices requires good grounding as well as good decoupling between stages. High gain in excess of 40 dB requires care. Below is an example of a typical circuit.



Chokes are recommended but not necessarily required. In this case we choose not to use the chokes in order to see how sensitive the bias line was for high gain amplifiers. This resulted in a three stage amplifier that showed no signs of bias instability. If one were to use chokes, a few turns on a ferrite core would most likely suffice. Capacitive decoupling is important. We used at least one 1000 pf chip capacitor on each bias supply as close as possible to the device. Chip capacitors were also located periodically along the main bus and where each of the bias lines converged. Flatness was very dependent on the coupling capacitors in between the stages. Our data sheet recommends 100 pf chip capacitors. We have found that many of these capacitors will exhibit intolerable reactances. First we tried 100 pf chip caps. The response showed shallow glitches (figure 19a-1). Next we tried 1000 pf (figure 19a-2). This removed the previous glitches. Since the 1000 pf capacitor improved the high end of the amplifier a lower capacitance was chosen. Finally a 500 pf capacitor was chosen (figure 19a-3) and resulted in a similar response to the previous 1000 pf chip capacitor. Clearly the parasitic reactance of the capacitors was interacting with the amplifiers. This was concluded since the effect of the amount of capacitance was opposite to the expected response.

space restrictions on board ship. A separation of only 25 feet is not unusual on a ship and substantial coupling occurs between antennas in portions of the HF range. The various transmitting systems obviously must use different operating frequencies but operation with frequencies as close as 5% of each other is often desired. Two types of coupling are of concern -- power coupling and impedance coupling.

Power Coupling: Let us first consider power coupling. Consider case 1. With system B transmitting at frequency F2, system A is automatically tuning at frequency F1. Some portion of the power radiated by the system B antenna is coupled to the system A antenna. Usually the power coupled to antenna A is 10 dB or more below the power radiated from antenna B but in the worst case it may be only 3 dB below the power radiated from antenna B. A typical antenna coupler exhibits very little selectivity to attenuate F2. The typical phasing-loading discriminator has neither selectivity nor directivity and cannot distinguish transmitter A signals from antenna B signals. The discriminator can only detect impedance magnitude and phase angle based on the voltage and current existing in the transmission line at the discriminator location. But in this case, the voltage and current are the result of the mixing of the voltages and currents for F1 and F2. Therefore erroneous discriminator output signals are detected which cause mistuning of antenna coupler A.

Now let us look at case 2. Consider that while system B was not transmitting, antenna coupler A was tuned and is now transmitting on F1. Now system B is keyed and begins to radiate power at F2. The power coupled to antenna A causes erroneous discriminator outputs as in case 1. If antenna coupler A has its automatic tuning circuits activated, for example by constant surveillance or demand surveillance, it will attempt to retune to satisfy the discriminator output signals. Then when system B is unkeyed again and stops radiating, antenna coupler A will attempt to retune to its original settings for F1.

In typical SIMOP situations a combination of case 1 and case 2 will occur mutually affecting both system A and system B. The resulting disruption of communications in each transmitting channel is evident.

A possible solution to the power coupling problem would appear to be to simply tune each antenna coupler while the others are not transmitting and then de-activate the automatic tuning controls. This method might be feasible when only two antennas are collocated but many installations have several antennas collocated. More importantly, this method does not solve the other coupling problem--impedance coupling.

Impedance Coupling: Referring now to Figure 9(B) note the equivalent circuit representing mutual impedance coupling

Input and output load pulling has shown this configuration to be unconditionally stable. This should be expected since these amplifiers exhibit a stability factor (K) of about 3, at 3.6 GHz, and greater than 20 at 100 MHz. Shown below is the performance of the previous discussion and NEC published data of three cascaded NEPA1001 amplifiers.

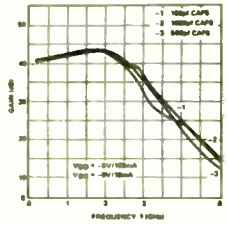


Figure 19a
(CEL)

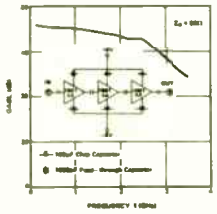


Figure 19b
(NEC)

Application of the UPG101

Much of the same precautions for handling and circuit layout apply to the UPG101 as they do to the NEPA1001 and UPG100. The package of the UPG101 is identical to the UPG100. The UPG101 requires only one additional bias point. Remember that this device is a medium power amplifier and that the drain current must be applied through an external RF choke. Most any conventional high frequency choke will work. The only precaution is that the choke must look for high impedance across the entire band.

In many cases, transformers or chokes will resonate when the wire becomes a magical length of 1/4 wave length. One approach that offers extremely good performance is to wind a 30 turn, 30 guage wire conical choke (Height = .375 mils, angle from longitudinal axis = 30 degrees) loaded with an absorbing material such as Ecosorbe MF-114. Another approach is to wind about 20 turns onto a high frequency torroid core. NEC suggests winding about 20 turns of 38 guage wire on a 1/4 watt resistor. This method works reasonably well and has the advantage of being inexpensive as well as mechanically stable. The disadvantage is that one can expect about 1 dB loss with this approach and will yield about a 11 dB return loss of the bias tee alone. The cone and the torroid provided about 20 dB return loss up to about 5 GHz with an insertion loss of about .7 dB.

It would be a good idea to check the choke by simply connecting the choke across the transmission line to ground. The design goal of such a choke should be the removal of all self resonances far enough away from the passband of the amplifier.

Self Bias of the UPG101

Self biasing the UPG101 is difficult. The high drain current would require a large resistor which may contribute large reactance for microwave work. Should a user need or attempt to use this configuratrion, CEL would like to hear your comments.

Handling the UPG and NEPA Series

Remember, active GaAs FETs are components of these devices. Static discharge and biasing precautions are a must. Also, remember that when powering-up, never apply the drain voltage before the gate voltage. The smaller signal devices, UPG100 and NEPA1001, are current-limited by a drain resistor. Limiting drain current makes the devices more forgiving to biasing errors. No doubt that the UPG101 will be less likely to take a "joke". One must take the same precautions when biasing the UPG101 as when powering any power GaAs FET device.

Conclusion

CEL is excited with NEC's development of these new MMIC's. These devices perform well and have lived up to all our expectations. NEC and CEL would like to invite the user to try these devices for whatever application they may have.

CEL is extremely well staffed with experienced sales persons and supported by a knowledgeable applications engineering group. It is the intention of CEL, together with NEC, to support the user for the successful utilization of all of our products. Should any questions arise concerning these MMIC's or other semiconductor products, please feel free to contact: Applications Engineering, California Eastern Laboratories, 3260 Jay Street, Santa Clara, CA 95054. Telephone: (408)988-3500

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between the antennas. To illustrate the problem let us ignore the power coupling. Consider that antenna coupler A is tuned correctly for F1 while antenna coupler B is tuned correctly for F2. Now while system A is transmitting, let system B retune to a new frequency F3. When antenna coupler B is tuned, the back impedance ZB looking from the terminals of antenna B to the output terminals of antenna coupler B is now different than it was when antenna coupler B was tuned for F2. ZB represents the load impedance for the equivalent T network which represents the collocated antenna system. Consequently ZC, the load impedance for antenna coupler A, is now different and antenna coupler A is no longer correctly tuned. The automatic tuning controls for antenna coupler A must be activated so it can retune to the new load impedance, but now the coupled power problem (which we ignored for illustration) may prevent correct tuning.

The combination of coupled power and coupled impedance occur in varying degrees in the HF band depending on type of antenna, separation from collocated antennas, other nearby structures, and the configuration of the antenna coupler impedance matching circuits.

The Solution

Figure 10 illustrates the solution to the shipboard SIMOP problem. A band pass filter is placed between the transmitter and the antenna coupler. The sensing device for automatic tuning is located at the RF input to the BPF instead of at the RF input to the antenna coupler. The F2 signal power coupled to antenna A is now attenuated by the selectivity characteristics of the BPF so the sensing device at the BPF input does not respond to the F2 signal. The selectivity of the BPF also reduces the level of intermodulation distortion (IMD) resulting from mixing of F1 and F2 at the transmitter.

A new problem is created by this configuration. The antenna coupler must be located above deck at the antenna base. On shipboard there is usually insufficient space near the antenna base for the BPF. Thus the BPF is located below deck, probably but not necessarily near the transmitter. A long coaxial transmission line is therefore required between the BPF and the antenna coupler. The length of the coaxial transmission line will be different for each different class ship installation. Tuning of the antenna coupler becomes the problem because the input impedance to the antenna coupler will be translated depending on the coaxial transmission line length and the operating frequency. In other words, the impedance at the input to the BPF where the sensing device is located is not representative of the impedance at the input to the antenna coupler. Therefore a new method is needed to correctly tune the antenna coupler. The TIMS provides that new method and is incorporated into the shipboard antenna coupler group.

Functional Description

The block diagram of the shipboard antenna coupler group is shown in Figure 11. The equipment uses an analog tuning system and is capable of operation with 1500 watts average and 2000 watts PEP RF input power. The tuning elements are servo motor driven vacuum variable capacitors. The directional coupler is located at the RF input to the bandpass filter. The forward and reflected voltage samples are supplied via coaxial transmission lines to the discriminator stages which are located in the control-power supply . The voltage analogs of the forward voltage, reflected voltage, and phase angle are applied via sample and hold circuits and A/D circuits to the Intel 8086 microprocessor circuit. Using these signals the microprocessor calculates the impedance which exists at the output of the directional coupler.

A calibration method is used to compensate for variations in the length of the forward and reflected voltage sample transmission lines from the directional coupler. A calibration module is included at the RF input to the antenna coupler where a phasing-loading discriminator would be located in previous antenna couplers. At initiation of a tuning cycle the directional coupler sample lines are calibrated. Tuning algorithms based on the calculated impedance at the directional coupler are used to tune the BPF. Then several known impedance RF loads are switched into the antenna coupler calibration module circuit. As each calibration load is inserted, the calculated impedance at the directional coupler is stored in memory. Subsequently during the antenna coupler tuning process, the real time calculated impedance at the directional coupler and the calibration impedances that were stored are used to calculate the impedance at the input to the antenna coupler. Tuning algorithms are used based on the calculated impedance at the antenna coupler input to control the analog tuning motor speed and direction to reach the tune point. Some of the algorithms rely on the capability of the TIMS to measure actual impedances rather than relative impedances as with the phasing-loading discriminator.

The antenna coupler group utilizes the variable attenuator capability of the TIMS for a low tune power capability. During the group tuning cycle a 6 dB pad is inserted at the input to the directional coupler to provide isolation between the untuned filter input and the transmitter output. The variable attenuator range can accomodate the 6 dB pad and the loss in the directional coupler sample coaxial transmission lines which can be up to 250 feet in length. The resulting tune power range is 50 milliwatts to 225 watts during initial tuning and 10 milliwatts to 2000 watts during surveillance tuning as a result of collocated impedance coupling. The TIMS as previously

SOLID STATE HF TRANSMITTER FOR OVER-THE-HORIZON (OTH) RADAR

Fuat Agi, Vice President Engineering, M/A-COM MPD
Donald J. Hoft, Sr. Vice President, M/A-COM, Inc.

Today there is an ever-increasing number of radar systems, both for new equipments and for improvement upgrades, which utilize solid state (SS) high power amplifiers for the transmitter. SS offers major advantages of high reliability and availability, graceful degradation, low MTTR, logistics and low life cycle cost. A well-designed SS system need never have a system outage due to the loss of the modules since the amplifier is distributed and fails gracefully. Amplifier (modules) building blocks which have failure rates measured in years, have replacement times measured in minutes thus the availability of the system is essentially 100% (approximately 1.0). Repair is often possible on-site with skill levels readily available by service personnel.

To exemplify the advancing state-of-the-art in radar SS transmitters, this paper will describe in some detail HF solid state 200 kW CW transmitter which is applicable in an over-the-horizon radar application.

200KW SS TRANSMITTER

Over-the-Horizon (OTH) Radars are currently planned in several countries for long-range (over 1000 miles) surveillance. These modern OTH systems typically utilize transmitters with 200 kW (CW) or more of power delivered to an array of 10-20 antenna radiators, see Figure 1. Thus, depending on the antenna tapering, the power output to each antenna element is between 5 and 40 kW. These systems utilize the ionosphere to reflect HF energy back to earth, range being a function of the ionosphere characteristics at the time, and the radar operating frequency. A 20 kW solid state transmitter developed for this application is shown in Figure 2. The performance is shown in Table 1 and a block diagram of the 20 kW shelter housing configuration is shown in Figure 3.

TABLE 1.

Frequency Band, Instantaneous	5-28 MHz
(Typical) Power Output, Total	200 kW CW
Antenna Taper	As required in 5, 10, 20 kW increments
Housing	Shelters of 20 kW each
Load VSWR	2:1 Max.
Cooling	Air
Dark Noise	-150 dBm/Hz
Near Carrier Noise	-93 dBc/Hz (2 Hz FM carrier)
Band Switching Time	0.3 sec.
Harmonics	-70 dBc
Phase Linearity	1 degree max. per 100 kHz band

In this way each shelter contains 20 kW of power which can be configured to delivery either 20 kW, 2 times 10 kW or 4 times 5 kW as required by the antenna system. The total system power requirements (over 200 kilowatts) is achieved with an appropriate number of shelters delivering power to the antenna array elements. As can be seen, a basic building block of the 20 kW unit is a 5 kW amplifier housed in each bay; the center bay contains the appropriate combiner, in the case shown in Figure 2 a 4:1 unit to 20

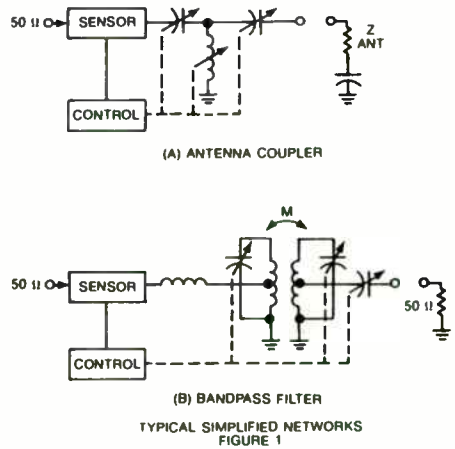
described also provides selectivity to further reduce susceptibility to the interfering signal.

AIRCRAFT APPLICATIONS

Aircraft have SIMOP problems also due to lack of space for antenna separation. We are currently implementing the TIMS into an aircraft SIMOP system. This system is for operation with 400 watts average or PEP RF input power, therefore the directional coupler can be smaller in size. Low power tuning is not a requirement so the variable attenuator is changed to a fixed attenuator and the discriminator injection frequency is changed to 50 kHz to reduce the size of the discriminator stages. The BPF and antenna coupler contain digital tuning elements.

SUMMARY

Sensing devices are needed to control automatic tuning of impedance networks. The conventional phasing-loading discriminator has been used for this purpose for many years but it has limitations for modern applications. The TIMS has been developed and patented for use as an impedance measurement system in automatically tunable impedance networks such as antenna couplers and filters. The TIMS overcomes the limitations of the conventional phasing-loading discriminator such as actual impedance measurement versus relative measurements, susceptibility to interfering signals, noise generation, and high RF power requirements. The TIMS provides accurate impedance measurements that can be used by a microprocessor along with calibration information to calculate impedances at a remote location. The TIMS has been successfully utilized in a shipboard antenna coupler group to solve SIMOP problems due to collocated antennas and is currently being implemented for an aircraft SIMOP solution.



TYPICAL SIMPLIFIED NETWORKS
FIGURE 1

kilowatts. Similarly the 5 kW amplifier is made up of individual power amplifier modules each of which provides 220 watts of output power from a push-pull configuration. Figure 4 is a detailed block diagram of the 5 kW amplifier. The transistors are derated to an average junction temperature of 120 degrees C (150 degrees C worst case) thus assuring excellent reliability. Figure 5 shows the power response of a typical 5 kW and 20 kW amplifier. Each 5 kW amplifier has its own dedicated power supply which has over-capability via redundant modules; thus providing for high reliability/availability on this critical component. BITE is provided to all power levels from the 220 W modules through the full 20 kW level and further includes a full complement of BITE functions. Maintenance is possible to the individual module (225 W) level. This transmitter is now in production at M/A-COM MPD.

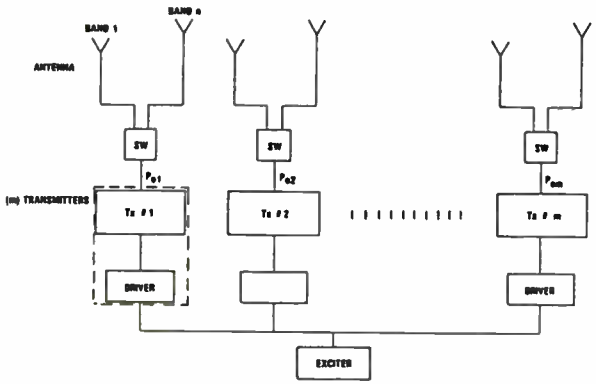


Figure 1. Typical Antenna/Transmitter Array Configuration over the Horizon Radar.

Figure 2.

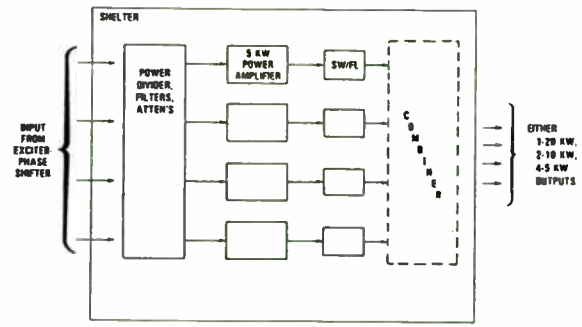
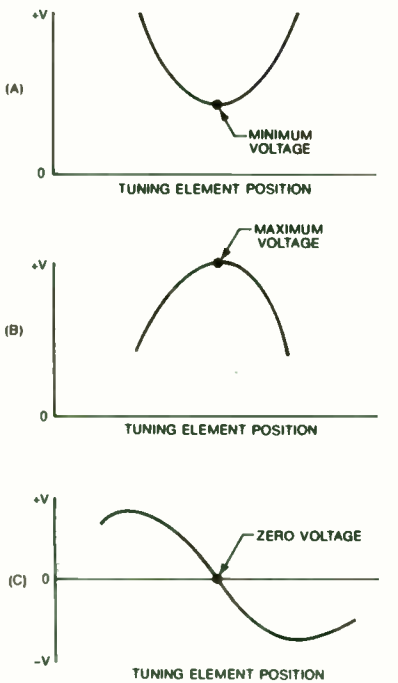
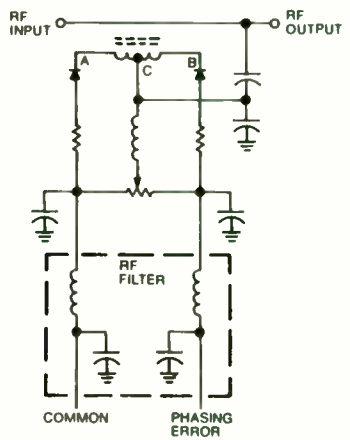


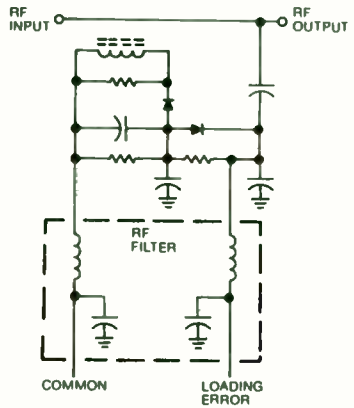
Figure 3. 20 K Watt Solid-State Transmitter Shelter Architecture.



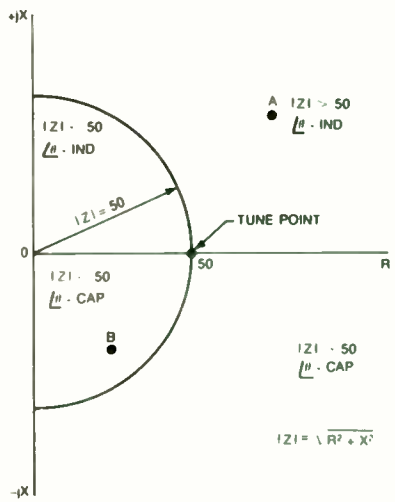
TYPICAL SENSOR SIGNALS VS ELEMENT POSITION
FIGURE 2



TYPICAL PHASING CIRCUIT
FIGURE 3



TYPICAL LOADING CIRCUIT
FIGURE 4



PHASING — LOADING DISCRIMINATOR RESPONSE
FIGURE 5

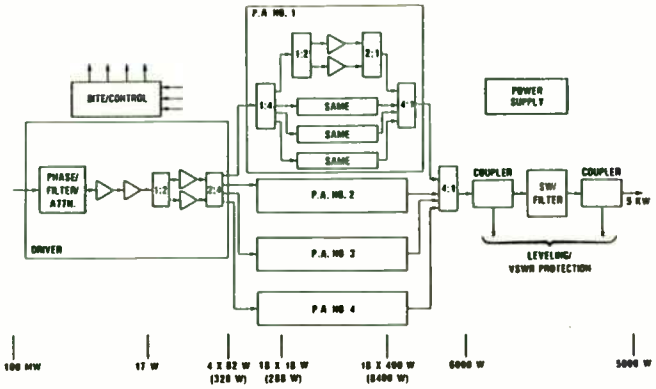


Figure 4. 5 Kilowatt Amplifier Subsystem.

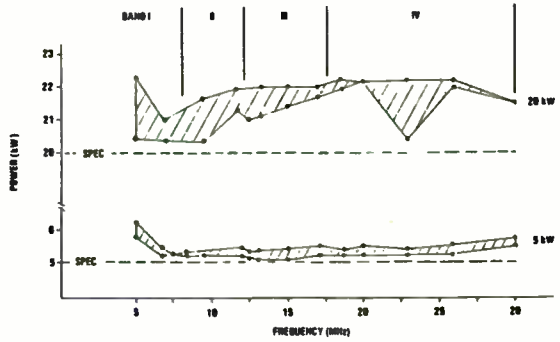
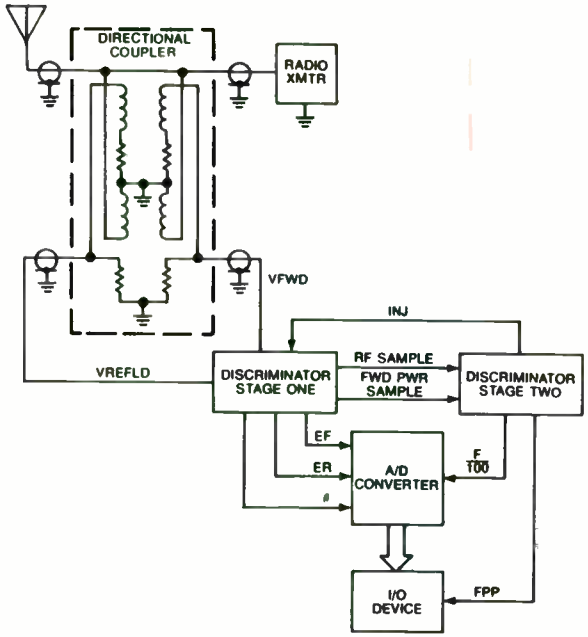
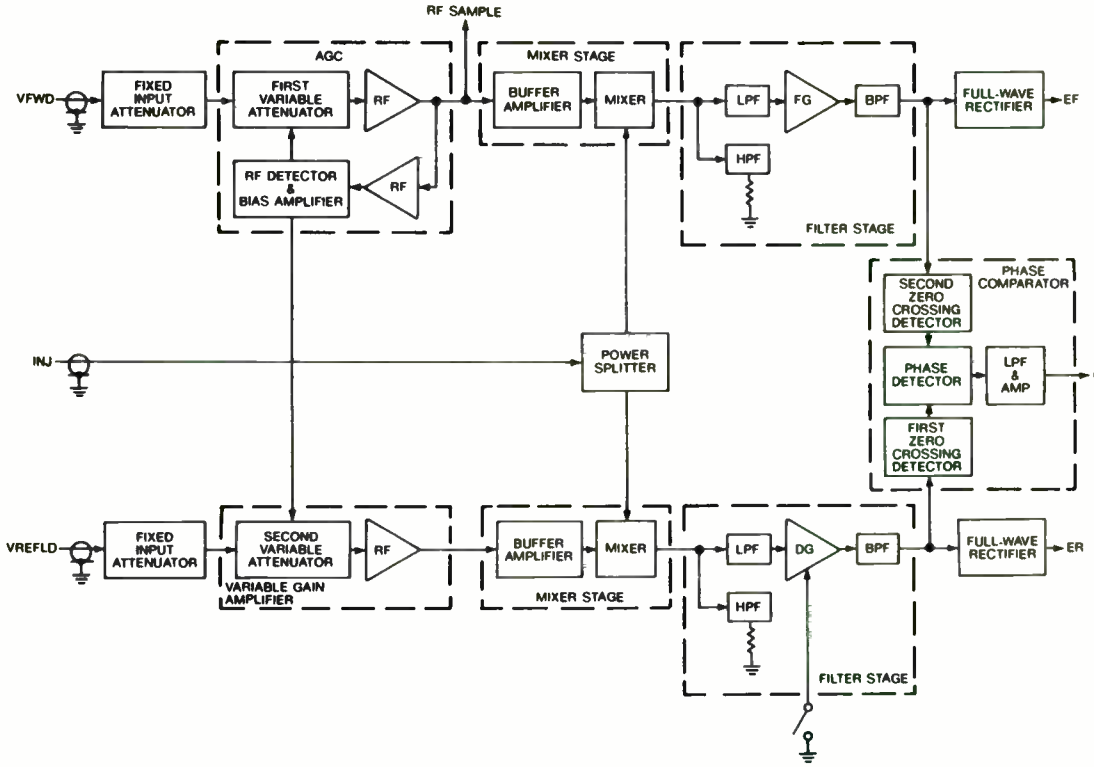


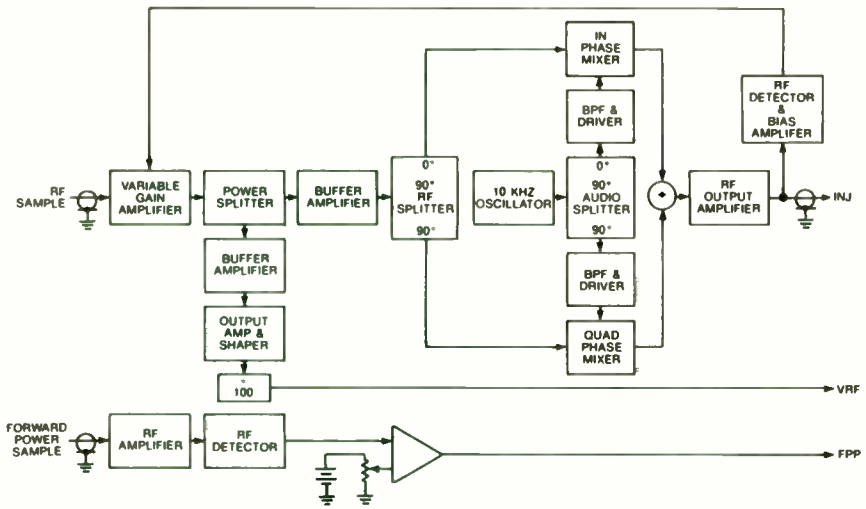
Figure 5. 5 kW, 20 kW System Performance Power vs. Frequency.



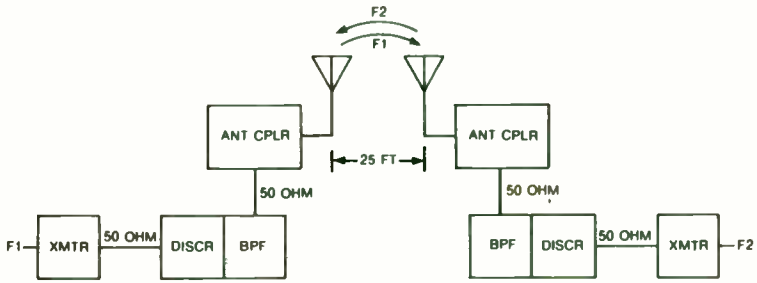
TIMS BLOCK DIAGRAM
FIGURE 6



TIMS DISCRIMINATOR STAGE ONE BLOCK DIAGRAM
FIGURE 7

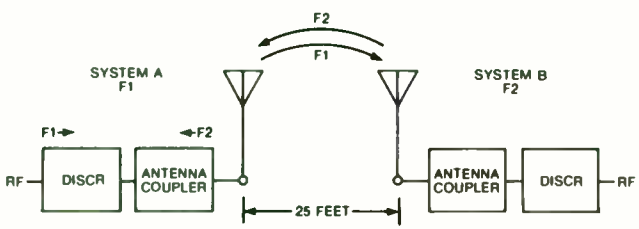


TIMS DISCRIMINATOR STAGE TWO BLOCK DIAGRAM
FIGURE 8

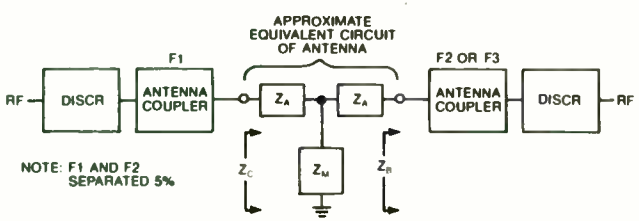


ANTENNAS MAY BE CLOSELY COLLOCATED
PREVENTS TUNING PROBLEMS DUE TO INTERFERING SIGNALS.
REDUCES IMD

SIMOP SOLUTION
FIGURE 10



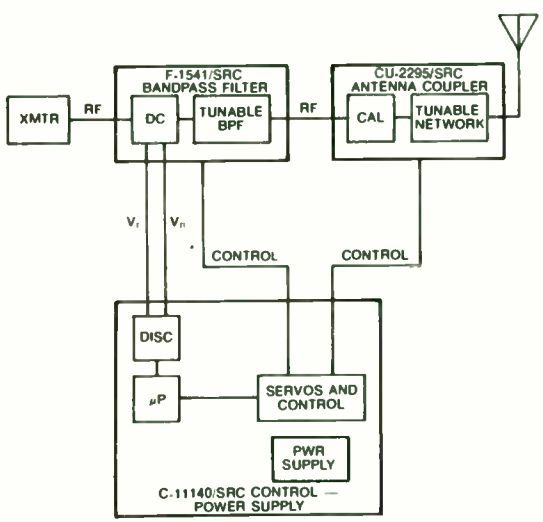
(A) COLLOCATED ANTENNAS



NOTE: F1 AND F2 SEPARATED 5%

(B) EQUIVALENT CIRCUIT

SIMOP PROBLEM
FIGURE 9



OA-9122/SRC BLOCK DIAGRAM
FIGURE 11

AN HF HIGH DYNAMIC RANGE AMPLIFIER USING FEEDFORWARD TECHNIQUES

by
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ABSTRACT

Feedforward is a distortion cancellation technique in which a sample of the distortion generated in an amplifier is coupled off, isolated, amplified, and recombined 180 degrees out of phase to cancel the remaining distortion in the output signal. This paper describes how feedforward was successfully applied to a three decade bandwidth amplifier (100 kHz to 100 MHz) to achieve a second-order output intercept point greater that +100 dBm, a third order output intercept point greater than +55 dBm, and a noise figure less than 7 dB.

FEEDFORWARD THEORY

A feedforward block diagram is shown in Figure 1. The main signal path is through the main amplifier and delay line 2 to the output. The distortion generated in the main amplifier is the source of the signal degradation and is the distortion which is cancelled by the feedforward circuit.

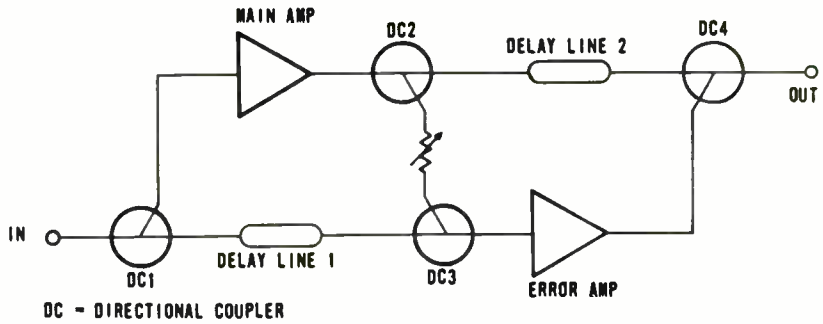

Fig. 1 - Feedforward Block Diagram

Feedforward utilizes a two loop system to accomplish the distortion cancellation. "Loop 1" shown in Figure 2A, can be recognized as the first half of the feedforward block diagram of Figure 1. "Loop 2," shown in Figure 2B, is the second half. Directional couplers are used to sample and recombine the signal and distortion to achieve the desired results.

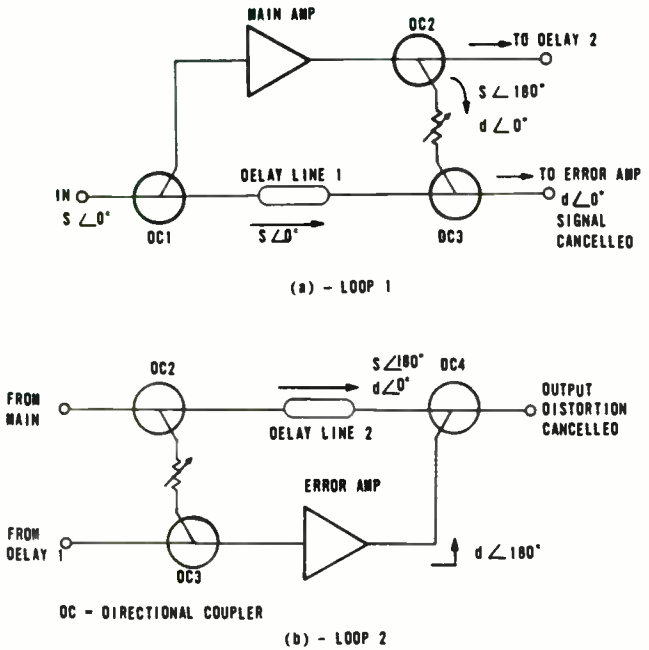

Fig. 2 – Feedforward Loops

To cancel the distortion generated in the main amplifier, it is necessary to isolate the distortion. This is the function of Loop 1 of the feedforward circuit. At the input, the clean signal is coupled off following one path through the main amplifier and the other path through delay line 1. At the output of the main amplifier, a sample of the distorted signal is coupled down to DC3 where it is recombined 180 degrees out of phase with the clean signal from delay line 1. By proper choice of circuit gain and attenuation elements in both paths, the two signals will have equal amplitudes and when combined 180 degrees out of phase the signals will cancel, thereby isolating the distortion. Maximum signal cancellation is desirable not only to obtain a "clean" distortion sample, but also to minimize the input level to the error amplifier so that it does not generate distortion. In addition to strict level control and phase requirements, the time delay of both paths must be equal for cancellation to occur. The delay line is designed to obtain this match.

The distortion cancellation is a function of Loop 2. Here, the isolated distortion at the output of DC3 is amplified by the error amplifier and coupled to the output to recombine with the distorted signal from the main path of the feedforward circuit. As with the cancellation requirements of Loop 1, the distortion from both paths must have good amplitude and delay match, and must be 180 degrees out of phase. Note that the distortion contributed by the error amplifier is insignificant due to the low signal level and so is not a concern.

CHOOSING THE RIGHT CRYSTAL AND OSCILLATOR FOR THE APPLICATION

by

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Some of the considerations which go into a decision on the choice and design of crystals and crystal oscillators are listed below:

1. Fundamental versus overtone mode crystal.
2. Parallel mode versus series mode.
3. VHF crystal versus multiplier chain.
4. Uncompensated versus TCXO or OCXO.
5. Trimable versus no trim adjustment.
6. Solder sealed package versus hybrid.
7. Voltage control required.
8. Stringent short term stability requirements.
9. Tight ageing requirements.
10. Start-up time.
11. Radiation requirements.
12. Shock and vibration rquirements.
13. Low current (battery operated).
14. Low parts count. Gate Oscillator.

In order to organize some of the above considerations, this paper arbitrarily begins with a 20 MHz , fundamental mode crystal in an HC-18 holder, to be used in an oscillator driving a receiver local oscillator chain to 400 MHz.
The characteristics of this crystal and its circuit are described and some of the options and considerations of the list are compared to this 20 MHz example.

FREQUENCY STABILITY

Assume that the oscillator has a temperature stability of ±40 PPM (parts per million) over the temperature range of -40°C to +85°C. To this must be added an ageing factor. One can conservatively assume 2 PPM ageing the 1st year of operation and a life time ageing factor of 4PPM. Using these assumptions, the worst case frequency error will be 40 + 4 or 44 PPM.

In Hertz;

$$20 * 10^{6} * 44 * 10^{-6} = 880 \text{ Hz},$$

and at the end of the x20 multiplier chain

$$20 \times 880 = 17{,}600 \text{ Hz}.$$

This frequency error would be tolerable if this fictitious local oscillator was part of a receiver with a 200 kHz I.F. bandwidth. If, however, the bandwidth were only 2 kHz,a 17600 Hz error in the local oscillator would be excessive. The narrow band assumption will be made in order to see where it leads the

DESIGN CONSIDERATIONS

AMPLITUDE

To obtain the amplitude match required from both paths of Loop 1 and Loop 2, the losses of the directional couplers and gain of the amplifiers are calculated.

For Loop 1, equal levels from both paths occur at the output of DC3 when the following equation is satisfied. (All gains and losses in dB)

$$S - D1 + G1 - D2 - D3 = S - L1 - DL1 - L3$$

where L# = absolute loss of thru path of DC#

D# = absolute loss of coupled port of DC#

DL1 = absolute loss of delay line 1

G1 = gain of main amplifier

Rearranged, this equation is one of three required for feedforward circuit design:

For signal cancellation:

$$G1 = D1 + D2 + D3 - L1 - L3 - DL1 \qquad 1$$

For Loop 2, the equation for amplitude match is

$$S - L2 - DL2 - L4 = S - D2 - D3 + G2 - D4$$

where L# = absolute loss of thru path of DC#

D# = absolute loss of coupled port of DC#

DL2 = absolute loss of delay line 2

G2 = gain of error amplifier

Rearranging gives the second equation required for feedforward design:

For distortion cancellation:

$$G2 = D2 + D3 + D4 - L2 - L4 - DL2 \qquad 2$$

An additional consideration is the desired gain of the feedforward circuit.

For gain requirements:

$$GAIN = G1 - D1 - L2 - L4 - DL2 \qquad 3$$

The solution to these equations is simplified by several design considerations. For minimum noise figure, DC1 and DC3 should have minimal thru path losses. Minimal loss in the thru paths of DC2 and DC4 is necessary for the highest intercept point. To simplify circuit design, G1 can be set equal to G2 which forces DC1 = DC4 and DC2 = DC3.

PHASE

The phase of the signals can be controlled by choosing appropriate paths through the directional couplers. The circuit diagram of a directional coupler is shown in Figure 3. When a signal enters port 1, the output at port 2 is 180 degrees out of phase with the input, whereas if the signal enters port 3, the output at port 4 is in-phase with the input. By directing the signal in the feedforward circuit through the appropriate port, the required phase is obtained.

oscillator design. The maximum error must now be restricted to about 200 Hz, or

DF, PPM = 200/400 = 0.5 PPM

This new requirement forces the design to either a much more stable crystal oscillator, or to a system in which the oscillator is locked to a stable master reference. These two approaches will be considered next.

TCXO's and OCXO's

(Temperature Compensated Crystal Oscillator and Oven Controlled Crystal Oscillators)

Before considering the two options of TCXO and OCXO, the questions of ageing and setability must be addressed. If the receiver must operate without adjustment throughout its life, then ageing will probably determine the quality of crystal oscillator required (and therefore the price, size and D.C. power). If the frequency of the oscillator can be corrected by electrical or mechanical adjustment to remove frequency error due to ageing, the frequency accuracy will be dominated by temperature rather than age. TCXO's and OCXO's will be considered with this assumption.

Briefly, a TCXO corrects the crystal frequency versus temperature characteristic by means of a compensation network which applies a correction voltage to a varicap diode in series with the crystal. An OCXO addresses the problem by controlling the temperature at the crystal with a miniature oven. Simplified schematics of a typical TCXO and OCXO are shown in Figure 1.

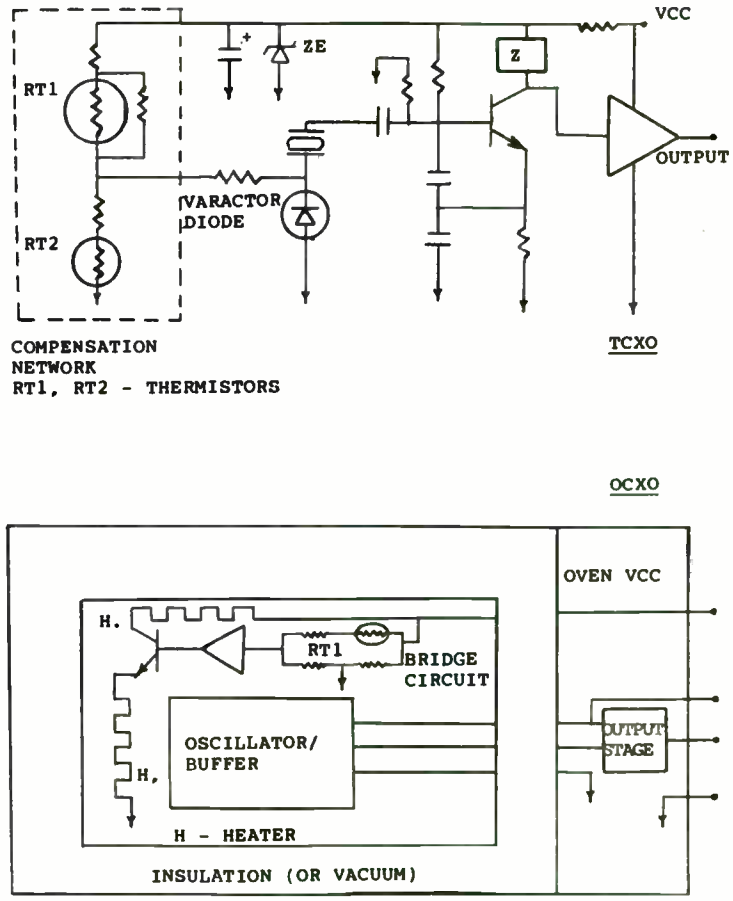


Figure 1, Simplified TCXO and OCXO

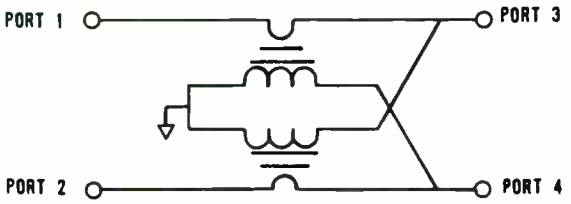


Fig. 3 - Directional Coupler

DELAY

Once the gain of the main and error amplifiers and the coupling coefficients of the directional couplers are chosen, the delay of the main amplifier path of Loop 1 is measured and matched by designing delay line 1 accordingly. Efforts should be made to minimize the delay variation versus frequency of the main amplifier path to simplify the delay line design. Similarly, delay line 2 should be designed to match the delay of the delay line path to the error amplifier path of Loop 2.

CANCELLATION REQUIREMENTS

Figure 4 shows the amplitude and phase match requirements to obtain the desired amount of cancellation. As the chart indicates, 20 dB of cancellation can be obtained with 1 degree of phase match and about 0.9 dB amplitude match. The circuit should have a gain adjustment to adjust the amplitude for a good match and a phase adjustment in the delay lines to attain the delay match. Equalizers and temperature compensation networks are sometimes necessary to obtain more stringent amplitude and phase match requirements.

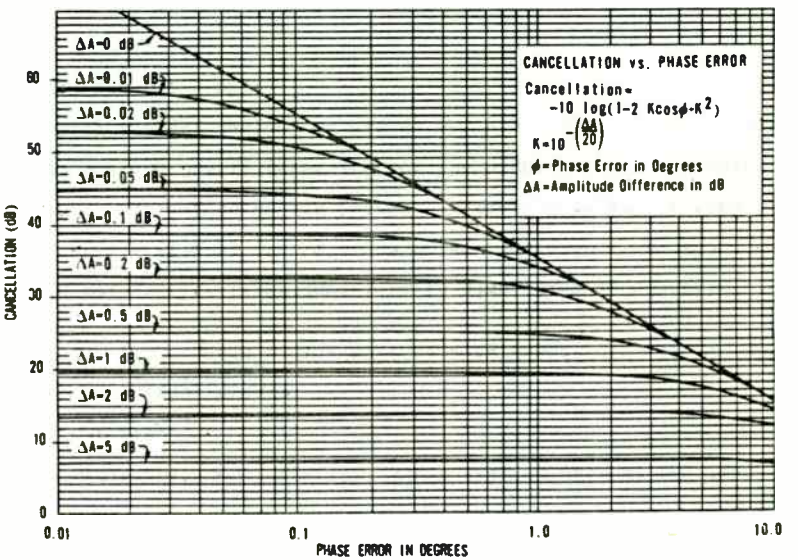


Fig. 4 - Cancellation Requirements

The new specification of .5 PPM puts the requirement somewhere in the gray area between TCXO's and OCXO's. Low cost, commercial TCXO's typically meet ±1 PPM over 0°C to 50°. The example oscillator's specification and temperature range puts the design near the border of the best that can be done with a TCXO, and consequently it would be a costly unit. OCXO's easily provide stabilities of $\pm 1 \times 10^{-8}$ over the required temperature range, and provide ageing rates less than 1×10^{-9} per day.

However, ovenized units are larger, heavier, and consume much more power than non-oven types. Representative specifications are shown in Table 1. Notice that some compromises may have to be made between requirements, performance, and price.

PHASE LOCKED SYSTEM

As an alternative, assume that this system already contains a stable master oscillator at 5 MHz. The basic crystal oscillator can then be locked to this master using a phase locked loop. Figure 2 illustrates the circuitry involved. Notice that a varactor in series with the crystal has been added in order to be able to pull (frequency shift) the frequency to exactly four times the reference 5 MHz.

Some notes concerning phase locking a crystal oscillator are appropriate.

1. The gain constant of a crystal controlled oscillator, KO, in Hertz per volt, is typically three to four orders of magnitude

TABLE 1 -- TYPICAL OCXO AND TCXO

SPECIFICATION	OCXO	TCXO
Frequency	5 or 10 MHz	5 to 50 MHz
Output Level	1 Vrms into 50 ohms	sinewave, TTL, or CMOS
Harmonic Distortion	-40 dBc	-20 dBc
Frequency Adjustment	+2.5 PPM minimum coarse mechanical. ±2x10E-7 fine ±1 PPM voltage control	±2x10E-6 minimum
Input Voltage	+ 12 V.D.C., ±10%	+ 12 V.D.C., ±5%
Frequency Stability vs Input Voltage	±3x10E-9 for ±10%	±2x10E-7 for ±5%
Frequency Stability vs Load	±1x10E-9 for ±10%	±2x10E-7 for ± 2:1 VSWR
Frequency Stability vs Temperature	±5x10E-9 -20°C to +75°C	±5x10E-7 -20°C to +60°C
Warm-Up Time	±1x10E-7 in 15 mins ±1x10E-8 in 20 mins	< 1 second
Aging Rate	1x10E-9/24 hours	1x10E-8/24 hours
Short Term Stability	3x10E-11 r.m.s Tau = 1 sec	1x10E-9 r.m.s Tau = 1 sec
Input Current	340ma. at turn-on 135ma. at 25°C 225ma. at -20°C	15 ma.
Size	2" x 2" x 4"	1" x 2" x 0.5"

FEEDFORWARD ARCHITECTURE

Other feedforward configurations are possible and should be chosen according to design requirements. Figure 5 shows a configuration commonly used for power amplifiers and is attractive because it requires less gain in the main amplifier than that of Figure 1. The disadvantage of the circuit in Figure 5 is that it has a much higher noise figure. This is due to the fact that feedforward not only cancels the distortion contributed from the main amplifier, but also cancels its noise contribution. This leaves only the error amplifier as the noise source. Since the noise contributed by the error amplifier is the sum of its noise figure and the losses incurred before it, the higher input losses of DC1 in Figure 5 will result in a much higher noise figure.

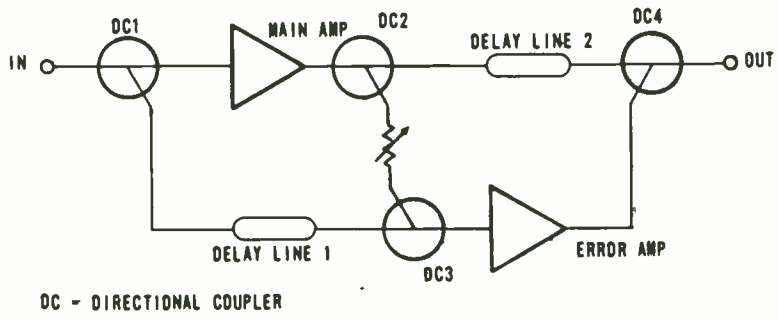


Fig. 5 - Feedforward Power Configuration

HF HIGH DYNAMIC RANGE AMPLIFIER DESIGN

This project was initiated in an effort to design a high performance amplifier suitable for HF multicoupler applications. An HF multicoupler is used at receiver sites to provide multiple outputs from a single receiving antenna and consists of an amplifier driving an n-way splitter. Because of the high concentration of both desired and undesired signals in the antenna environment, a high performance amplifier is required. It must not add excessive noise to weak desired signals nor produce intermodulation products from strong signals. The demands placed on such an amplifier are severe.

Preliminary specifications were established based on these demands and what was considered theoretically possible. A gain of around 11 dB was determined to be necessary to offset the loss of an 8-way split. The goals set for the second and third order output intercept points (OIP2 and OIP3, respectively) were based on the performance of a typical 1 watt bipolar transistor and the estimated distortion cancellation capabilities of push-pull and feedforward techniques. In particular, it was estimated that the OIP2 could be improved 20 dB from push-pull and 20 dB from feedforward and the OIP3 could be improved 3 dB from push-pull and 10 dB from feedforward. From this, the goal of +100 dBm for OIP2

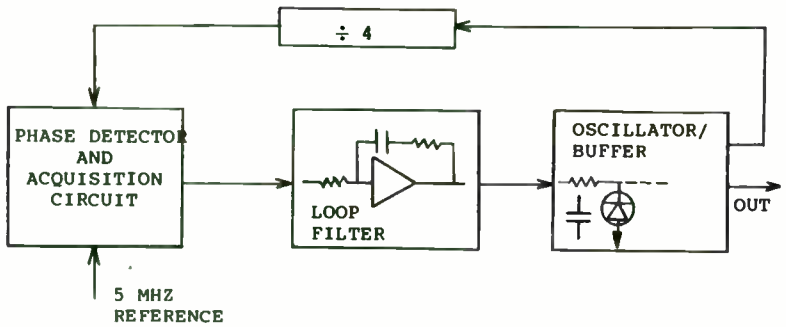


Figure 2, Phase Locking

less than that for a VCO (voltage controlled oscillator). The 20 MHz example would have an average KO of 500 Hz per volt.

2. The loop bandwidth for a phase locked loop using a crystal controlled oscillator is typically 10 to 200 Hz. Very much narrower bandwidths may cause loop phase jitter problems. Wider bandwidths are limited by frequency response roll-off caused by the narrow band nature of the oscillator.

3. The crystal oscillator must be capable of being pulled, or slewed, by an amount equal to its' temperature and ageing frequency error. This assumes that the master oscillator drift is negligible. The TCXO and the phase locked oscillator both require electronic tuning, by means of a varactor diode, or varicap. It is appropriate to discuss varactor tuning in more detail, before discussing overtone crystal oscillators because overtones have very limited "pullability."

VCXO (VOLTAGE CONTROLLED CRYSTAL OSCILLATOR

The equivalent circuit for a crystal is shown in Figure 3.

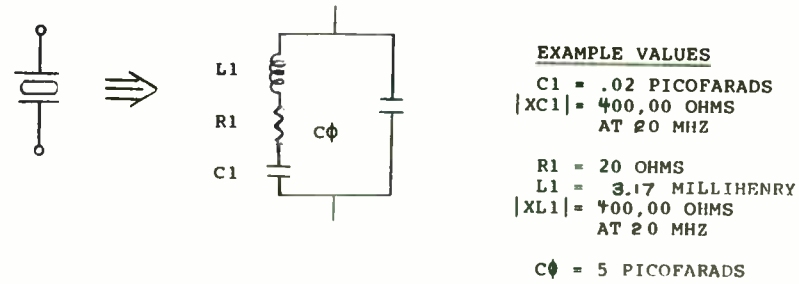


Figure 3, CRYSTAL EQUIVALENT CIRCUIT

L1, C1 and R1 represent the piezoelectric coupled mechanical resonator characteristics. CO is the capacitor formed by the crystal electrodes. Typical values for the 20 MHz crystal are shown. When the crystal is part of a complete circuit,as shown in Figure 4, oscillation occurs at a frequency above F1, where the crystal series arm presents a net inductive reactance, resonant with the capacitors and inductors in the circuit.

and +57 dBm for OIP3 was established. The noise figure was estimated to be 7 dB: 5 dB from the error amplifier and 2 dB from input losses. With these preliminary specifications, a circuit was built, tuned and tested as described below.

FEEDFORWARD

The feedforward configuration used in the HF high dynamic range amplifier was a modification of that shown in Figure 1 and is shown in Figure 6. Directional couplers DC2 and DC3 are replaced with a single directional coupler to achieve the desired results with fewer parts. A gain adjustment is placed within each loop for independent control of signal levels. With this design, three 14 dB directional couplers are used with main and error amplifier gains of 26.5 dB. This achieves the necessary cancellation in both loops and the desired gain of 11.5 dB.

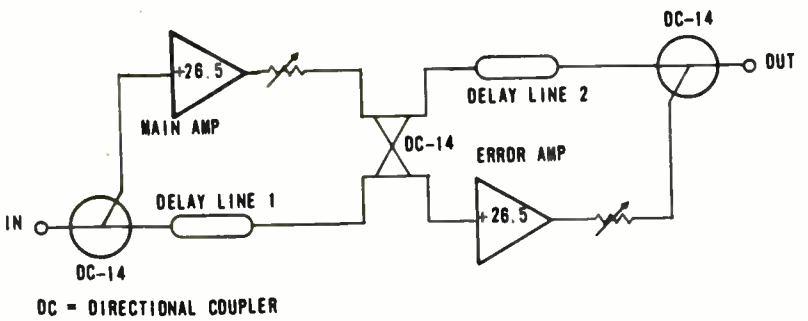


Fig. 6 - Feedforward Circuit

PUSH-PULL

Feedforward is used to cancel distortion generated in the main amplifier by 20 dB and more. However, second order output intercept points greater than +100 dBm and third order output intercept points greater than +57 dBm require a high performance main amplifier. A push-pull arrangement shown in Figure 7 is used to obtain an additional 20 dB of cancellation of the second order intermodulation product and an additional 6 dB of reduction of the third order intermodulation product. Flatness and phase linearity is improved by using 3 dB directional couplers instead of push-pull transformers. In addition, noise figure and intermodulation products are minimized by biasing amps 1 and 2 with Ic = 50 mA and amps 3 and 4 with Ic = 100 mA at +15 V. This design is used for both the main and error amplifiers bringing the total power consumption to 9 watts.

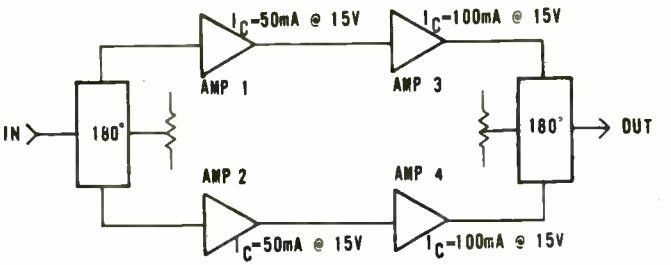


Fig. 7 - Push-Pull Arrangement for Main and Error Amplifiers

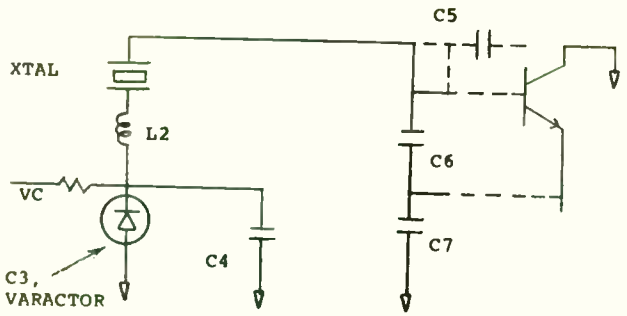


Figure 4, CRYSTAL AND CIRCUIT

The resonant frequency of the complete circuit can be calculated for any particular set of values by writing the appropriate equations for the resonant frequency and solving. This is conveniently done on a computer. Seven cases have been calculated and presented in Table 2 for typical circuit values.

In Table 2 the values of C1, C4, C6/C7, L2 and the varactor parameters (C3) are varied to show the effect on frequency pulling and linearity. A control voltage range of 1 volt to 10 volts is assumed. The frequency data is listed as; (1) PPM away from crystal series arm resonance, (2) the 1 V to 10 V frequency delta, (3) The frequency voltage sensitivity in PPM per volt, at the ends of the range.

In case 1, the difference in sensitivity at 1 V and 10 V is extreme. This results from the varactor capacity-voltage characteristic and from the loss of sensitivitiy as the crystal is pulled further from resonance. Case 2 is like Case 1 except that C1 has been halved. It is seen that the delta F is also reduced by 2, showing the direct dependence of "pullability" on C1. This is discussed in the section on overtone operation. Notice that the difference in 1 V to 10 V sensitivity is not as extreme in case 2 because the crystal is not pulled as far from series resonance. Case 3 shows that C4 reduces pulling and degrades linearity.

In Case 4 the varactor 4 volt value is changed from 30 picofarads to 15 picofarads, resulting in greater pullability and better linearity. Cases 5, 6, and 7 use a hyperabrupt varactor (gamma = .8) instead of the abrupt junction one. This yields improvement in pulling and linearity. Finally, Case 7 shows that the addition of a three microhenry series inductor (L2) further increases pulling. One note of caution. Reducing the varactor capacity results in an increase of the circuit parallel loss. In Case 6, for example, unless the crystal resistance is suitably low, the circuit may stop oscilleting at 10 volts.*

* This topic is addressed in the paper "Maximizing Crystal Oscillator Frequency Stability" Session A-2, r.f. expo 86.

RESISTIVE FEEDBACK

The amplifiers in the push-pull arrangement use Motorola's MRF587 1 watt bipolar transistors in a resistive feedback network. Negative feedback techniques are beneficial because they produce flatter gain, lower distortion, better impedance match, and temperature stability. Although resistive feedback results in a higher noise figure (5 dB versus 1.5 dB) and a lower intercept point (by 1-2 dB) than a lossless or coupler feedback network, this compromise was accepted in return for the extended bandwidth that it provided. The resistive feedback amplifier circuits are designed based on a desired gain of +14 dB per stage to bring the total gain in the push-pull arrangement to 26.5 dB. Gain flatness of the push-pull configuration with resistive feedback amplifiers is $\pm$0.1 dB from 100 kHz to 100 MHz with a return loss greater than 20 dB.

TUNING PROCEDURE

Loop 1 and Loop 2 are designed independently and fine-tuned after integrating into the final feedforward circuit. The final circuit is tested using resistive coupler test points as shown in Figure 8.

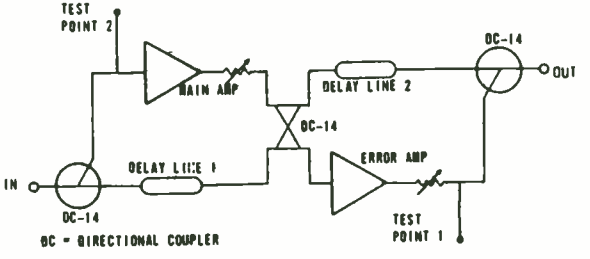


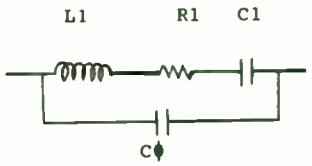
Fig. 8 - Feedforward with Test Points

Tuning the feedforward circuit is performed by using a test signal to simulate the signal that is to be cancelled in Loop 1 and to simulate the distortion that is to be cancelled in Loop 2. Cancellation of each loop is measured separately and requires a reference. For Loop 1, a reference is set up by disconnecting the main amplifier and sweeping from the input through the delay line 1 path to test point 1. Then, with the main amplifier in the circuit, the cancellation is measured by sweeping across Loop 1 from the input to test point 1. Amplitude and delay adjustments should be made to improve the match for maximum cancellation. Similarly, the cancellation of Loop 2 is measured by disconnecting the error amplifier and injecting a test signal into test point 2 through the delay line 2 path to the output to obtain the reference. Then, with the error amplifier in the circuit, the response of Loop 2 from test point 2 to the output is measured and tuned for maximum cancellation.

THE OVERTONE CRYSTAL AND OSCILLATOR

It might be asked of the model local oscillator chain, "Why start at 20 MHz?" "Why not use a 5th overtone crystal at 100 MHz, save a lot of multiplication and move the close in spurious out by a factor of 5"?

For the original stability assumption of ± 40 PPM, this might be an attractive choice. With a tight frequency tolerance, it is not, and to see why, the overtone equivalent circuit will be examined. Shown in Figure 5 below is the equivalent circuit of the same 20 MHz crystal, but for the 3rd or 5th overtone mode:



L1 = 3.17 mH; R1 = 10 TO 100 OHMS

C1; 3rd OVERTONE = $\frac{C1,\ FUND.}{9}$

$\approx$ .0022 PFD.

5th OVERTONE = $\frac{C1,\ FUND.}{25}$

$\approx$ .0008 PFD.

Figure 5, OVERTONE EQUIVALENT CIRCUIT

It is seen that the inductance remains the same, while C1 is reduced by a factor N^2, where N is the overtone, 3, 5, 7*, 9* etc. Consequently, the "pullability" of an overtone crystal is reduced by approximately the overtone number squared, compared to the fundamental mode. Typical pullability for a 60 MHz 3rd overtone would be on the order of ±30 PPM, and for a 100 MHz 5th overtone, ±10 PPM. Clearly, there is not enough pull range to use these modes in the TCXO or phase locked examples described here.

* Higher than 5th are relatively rare.

SHORT TERM STABILITY

Thus far, those systematic changes in frequency have been discussed which are due to factors such as temperature and time. Oscillator frequency is also perturbed by random, noise-like factors, and these perturbations typically are important for disturbances with time constants from microseconds to seconds. This short term stability is measured in the time domain where some type of frequency counter is the key instrument, and in the frequency domain, where spectral analysis of one form or another is used.

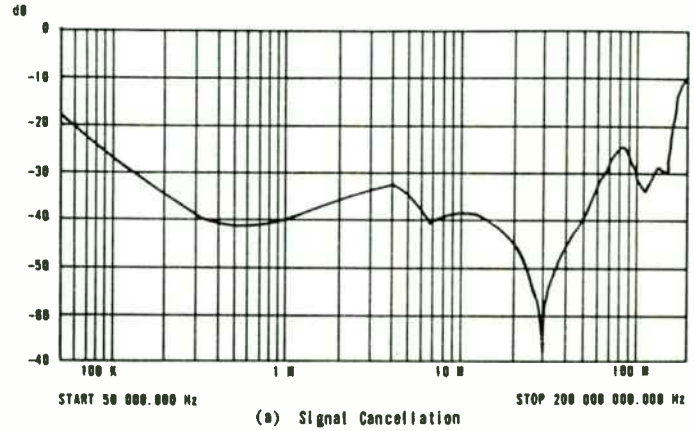
In many of these measurements it is necessary to use two oscillators, either with a small frequency offset, or locked together in a phase locked system. Some typical time domain values are listed in Table 1.

OTHER TOPICS IN CRYSTAL AND OSCILLATOR SELECTION

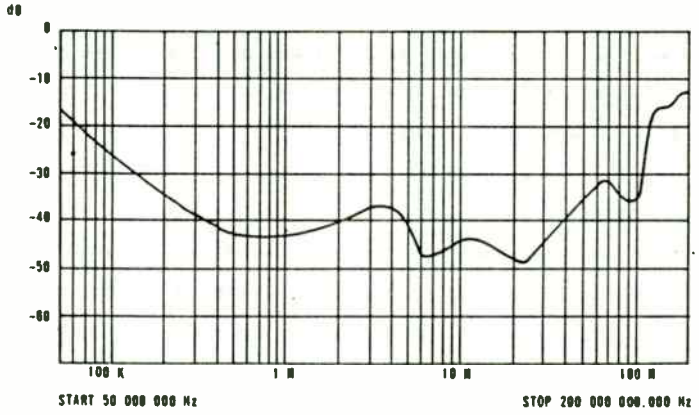
1. Clock oscillators: Miniature, self contained crystal oscillator and output buffer combinations. These hybrid units are available with output frequencies from sub-Hertz to 150 MHz. Outputs are compatible with standard logic families, TTL, CMOS, ECL. Militarized units are available with stabilities of ±50 PPM

RESULTS

Test results of the specified HF high dynamic range amplifier indicate success in attaining the specifications set forth. Figure 9 shows the cancellation curves of Loop 1 and Loop 2. As can be seen, better than 30 dB of cancellation of both signal and distortion was attained across most of the three decade bandwidth from 100 kHz to 100 MHz. The gain and return loss curves, shown in Figure 10, indicate a flat response with 11.5 $\pm$0.5 dB of gain and return loss better than 18 dB across most of the band. Figure 11 is a plot of the calculated intercept points with and without feedforward based on the intermodulation measurements of a two-tone test. The OIP2 was 10 dB higher than the expected +100 dBm due to the 30 dB of cancellation obtained from feedforward rather than the anticipated 20 dB. The OIP3 was better than the expected +57 dBm across most of the band. The noise cancellation effects are presented in Figure 12. With feedforward, the noise figure was below the 7 dB specification.



(a) Signal Cancellation



(b) Distortion Cancellation

Fig. 9 - Cancellation (Model RF 1960A)

over the temperture range -55° C to +125° C.

2. Low power oscillators: Oscillators for battery operated equipment must sometimes operate on less than one milliampere. Using AT cut crystals in the low megahertz range and special circuits this kind of requirement can be met while retaining the advantage of the AT cut crystals. For outputs in the tens of kilohertz, where looser frequency tolerances or narrower temperature ranges obtain, tuning fork crystal oscillators are available with current drains in the tens of microamperes.

3. AGC: Simple AGC control of the oscillator operating point provides many advantages. Low crystal power dissipation, important for good ageing, can be achieved while avoiding circuit start-up problems sometimes associated with very low power operation.

SUMMARY

Choosing a crystal and crystal oscillator circuit requires matching between the requirements of the application and the characteristics of the oscillator. If the oscillator must be pulled more than 10 or 20 PPM, a fundamental crystal in the 10 to 25 MHz range is probably indicated. If the ultimate in temperature stability, ageing and close-in noise is the object, a 3rd or 5th overtone, 5 MHz, ovenized unit is indicated. For small size, low cost, and nominal AT cut stability, a clock oscillator might meet the objectives.

If VHF or UHF outputs are needed a 3rd or 5th overtone crystal oscillator, operating up to 150 MHz might simplify the design.

TABLE 2 - VCXO

	CIRCUIT PARAMETERS C3, VARACTOR								FREQUENCY PULLING DELTA F, PPM				
CASE	C1	CO	4V.C	GAMMA	C4	C5	C6/C7	L2	1V	10V	DELTA	DF/DV (1V)	DF/DV (10V)
1	.02	5	30	.5	0	2	100	0	322	519	197	38	4
2	.01	5	30	.5	0	2	100	0	161	259	98	19	7
3	.02	5	30	.5	20	2	100	0	284	363	79	20	4
4	.02	5	15	.5	0	2	100	0	447	753	306	65	20
5	.02	5	15	.8	0	2	100	0	379	858	479	87	34
6	.02	5	15	.8	0	2	50	0	488	912	424	76	30
7	.02	5	15	.8	0	2	100	3	-5	680	685*	130	45

* Even greater pulling can be accomplished with a more complex circuit.

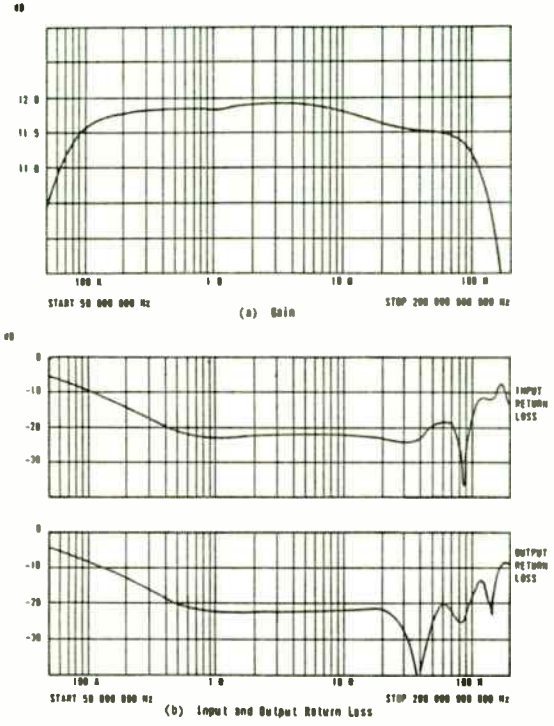


Fig. 10 - Response (Model RF 1960A)

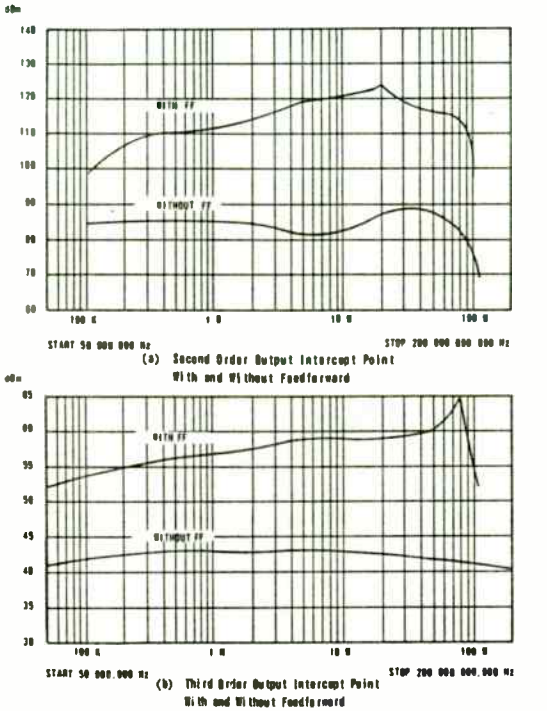


Fig. 11 - Output Intercept Points (Model RF 1960A)

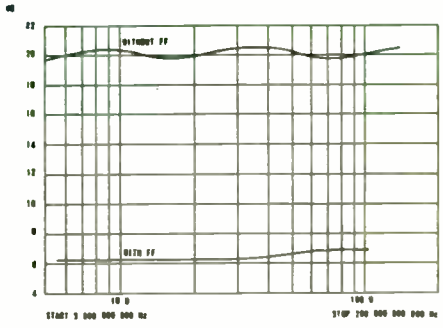


Fig. 12 - Noise Figure With and Without Feedforward

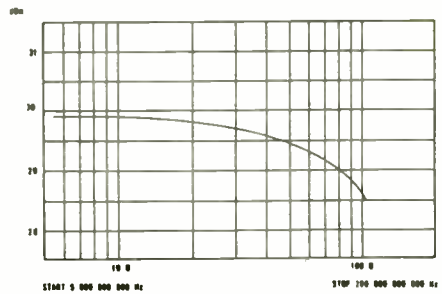


Fig. 13 - 1 dB Compression Point (Model RF 1960A)

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1. H. Seidel, "A Microwave Feed-Forward Experiment," Bell System Technical Journal, Vol. 50 Nov. 1971, pp. 2879-2916.

2. J. Dixon, "A Solid State Amplifier with Feedforward Correction for Linear Single-Sideband Applications," IEEE International Conference on Communications 1986, Ch 2314-3/86/0000-0728.

THE USE OF A COMPUTER MODEL TO DETERMINE THE COMPLEX PARAMETRIC RELATIONSHIPS OF A CRYSTAL OSCILLATOR CIRCUIT

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INTRODUCTION

The circuit modeled by the computer program is a 100 MHz Pierce crystal oscillator driving a common base buffer amplifier. The oscillator was developed by Piezo Systems for a satellite project. Because of the strict design criteria required by the customer for qualification of the oscillator, the modeling program was developed to allow design and analysis to be performed during the prototype phase of the project. As will be shown in this paper, the modeling program created an extremely valuable tool for the oscillator design and was used throughout the project for complex analysis which would have been extremely difficult and time consuming. From this analysis, some very important complex parameters of the oscillator circuit were determined. These include crystal drive, gain margin, loaded Q of the resonator, group delay of the feedback loop and phase slope. The calculation of these parameters allow a prediction of the phase noise contribution of the oscillator as a signal source.

THE COMPUTER MODEL

The computer program models the circuit in an open loop configuration. As shown in Figure 1, the loop is broken at the input to the base of the oscillator transistor. The input impedance of the oscillator transistor is included in the calculation of the collector load. Therefore, the program analysis is simply the calculation of the swept response of a two port network with a complex load determined by the relationships of the circuit elements. From the two port response, the following may be determined: the transistor stage gain with respect to the collector load, the loss due to the feedback loop network, the loss due to the power output to the buffer amp, the magnitude and phase of the collector load and the magnitude and phase of the total loop gain around the oscillator circuit.

The various gain blocks described above are broken down by using complex algebra to calculate the equivalent networks of the circuit elements. The transistor's contribution to the gain blocks is found by using S parameter data obtained for the transistor at the same DC operation point as used in the circuit. As shown in Figure 2, the circuit elements are divided into 2 gain blocks. Gain block 1 includes the crystal resonator and the two paralleled capacitors across the base of the oscillator transistor (C2 and C3). The complex impedance of the crystal includes the shunt capacitance (Co) of the crystal

RESEARCH REPORT

ON

COAXIAL CABLE LEAKAGE

AUGUST 1985

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5730 GENERAL WASHINGTON DRIVE
ALEXANDRIA, VIRGINIA 22312

Author: Brian E. Streve.

Contrary to popular belief, coaxial cable exhibits leakage of electromagnetic energy from its shield at greater than negligible levels. This report is a compilation of research initiated to determine the severity of the leakage of coaxial cable in the frequency range 2 to 30 MHz. Several types of cable, experimental and analytical methods, and numerical results are discussed.

Shielding effectiveness of a coaxial cable is the ratio of the magnetic or electric field intensity without the shield to the field intensity with the shield in place. Analytic methods and laboratory experiments yield an approximate value for shielding effectiveness but the actual realized shielding is dependent on numerous factors, some indeterminable quantitatively, such as physical orientation and installation of the cable, and the effect of neighboring objects and connections.[1]

Several methods exist to predict and determine shielding effectiveness of braided shield coaxial cable. The surface transfer impedance concept is very useful for predicting the limits of shielding effectiveness. Treating the gaps between the conductors of the braided shield as radiating aperatures yields a model at the expense of tedious mathematics. Direct measurement methods include a triaxial apparatus to measure the RF voltage and current on the shield as a function of frequency, relative measurements between cables, and absolute measurement of the field in a shielded room using calibrated antennas.

Surface transfer impedance may be thought of as the impedance through the shield of a coaxial cable. For solid metal shields energy is transferred via the diffusion transfer impedance, Z_t. It has been shown that the complex impedance Z_t can be computed for solid shields using the

enclosure and the equivalent reactive elements and series resistance of the resonator as entered at the initialization of the program. Gain block 1 represents the loss of the feedback network of the circuit. Gain block 2 includes the capacitive tap off the collector tank (C7 and C9), the coupling resistor between the stages (R13) and the input impedance of the buffer amp. The input impedance of the buffer amp was measured to be about 27 ohms resistive. Though the common base amp should be very low impedance at 100 MHz, enough positive feedback occurs through stray circuit board reactance to increase it to its measured value. The emitter degeneration resistor (R5) is included with the input impedance of the buffer amp to give the circuit element (ZIN2) of Figure 2. Gain block 2 represents the loss due to the power incident to the buffer amp through the capacitive tap (C7 and C9).

The available power gain of the transistor stage is calculated by the use of the measured S parameters of the transistor two port and the reflection coefficient of the collector load normalized to a 50 ohm system. First, the impedance of gain blocks 1 and 2 is calculated as two paralleled networks. The reactance of the capacitive tap capacitor C7 is then added in series. The collector load (ZL) is calculated by the paralleled impedance of the equivalent impedance of the gain blocks 1 and 2 and the impedance of the collector tank (L1, C5 and C6). This allows the reflection coefficient of collector load in a 50 ohm systems to be determined by the formula:

$$\Gamma L = \frac{(ZL - 50)}{(ZL + 50)}$$

The available power gain is found by the ratio of the reverse scattering coefficient of the equivalent two port to the forward scattering coefficient with respect to L. This is calculated by the use of the following formula:

$$Pav = \frac{(S_{21} \times \Gamma L) + S_{21}}{((1 - (S_{22} \times \Gamma L))(1 + S_{11}))(S_{12} \times S_{21} \times \Gamma L)}$$

Also, the input impedance of the oscillator transistor may be calculated by the formula:

$$\Gamma in = S_{11} + (S_{21} \times S_{12} \times L)$$

$$Zin1 = \frac{50 (1 + \Gamma in)}{(1 - \Gamma in)}$$

From the development of the gain blocks, the total loop gain is simply:

$$Aloop = Pav \times G_1 \times G_2; \quad \begin{matrix} G_1 \text{ is the loss of gain block 1} \\ G_2 \text{ is the loss of gain block 2} \end{matrix}$$

The above description of the analysis illustrates the completeness by which all of the circuit elements are modeled. This allows a fairly large and detailed initializaton table to be constructed for the model. The effects of individual circuit elements may therefore be examined. Table 1 lists the circuit elements available for input at initialization. The program runs in a "DO FOR" loop with each repetition corresponding to a subsequent increase in sweep frequency. Initially, the program

equation[6,8]

$$Z_t = \frac{2R_{dc}(t/d)}{\sqrt{\sinh^2(t/d) + \sin^2(t/d)}} \angle 45^\circ - \arctan(\coth(t/d)\tan(t/d)) \quad (1)$$

where:
Z_t = transfer impedance through the shield in ohms/meter
R_{dc} = DC resistivity of the shield in ohms/meter
t = thickness of shield
d = skin depth, or field penetration into the shield in meters

$$d = \sqrt{P/3.1415fu}$$

P = dc resistivity of shield in ohms/meter
f = frequency in Hz
u = absolute magnetic permeability of shield material in H/m

At low frequencies the skin depth is so large that the transfer impedance is essentially the dc resistivity of the shield.

The parameters required in Equation 1 are readily found and a numerical solution computed for solid shields. This yields a method by which measurement techniques can be judged.

Surface transfer impedance can be measured directly by causing a known current to flow through the length of the shield and measuring the voltage drop across the shield. Alternately a known voltage can be impressed across the shield and the resulting current flow measured. Accurate measurements depend on a well shielded enclosure for the test sample, accurate instrumentation and methods to measure RF voltage and current, shielding the cables to the measurement instrumentation, careful RF grounding of the test fixture and instrumentation, and care in making connections at the ends of the cable to prevent end effects from dominating the results. Smith[8], DeLorenzo[2], Simons[7], and Salt[6] have documented triaxial testers where the coaxial cable under test forms the the inner two conductors of the triaxial arrangement. The outer conductor of the test apparatus is solid to contain nearly all the energy within the fixture and prevent external fields from tainting the results.

Comparisons between values of the surface transfer impedance calculated using Equation 1 and measured values have been made using solid shield coaxial cable. The good agreement between the values gives confidence in the validity of the direct measurement technique using triaxial testers.2

The discussion of computational methods thus far has been limited to solid shields since the surface transfer impedance equation variables are readily found and solutions simple. These computations can be used to derive minimum radiation limits or maximum shielding effectiveness values for braided shields. Braided shields exhibit the diffusion transfer impedance of Equation 1 with t being equal to the braid wire diameter. Additionally, the gaps between the wires act as an array of electric and magnetic dipoles. Thus inductive (magnetic) coupling and capacitive (electric) coupling allows the fields within the coax to penetrate the shield. Cable eccentricity additionally contributes primarily to the magnetic coupling as detailed by Fowler.[3] Each of the gaps in the braid thus acts as a waveguide to transfer some of the energy from the inside of the cable to the outside. Alternately, the gaps in the braided shield can be thought of as discontinuities in a solid shield which the RF current must flow around thus producing higher field strengths than those generated by the continuous shield. Exhaustive mathematical modeling of the dipole array created by the gaps in the braid has been performed by Ikrath[4] and Vance[9]. Fowler[3] further models the effects of cable eccentricity, intershield resonance in multi-shield cable, and shield termination methods. He further proves that these effects can generate additional coupling on the same order of magnitude as the transfer impedance calculated solely from braid parameters. These models require several physical parameters of the

starts at 500 Hz below the series resonant frequency of the crystal and increases in 50 Hz steps to 2500 Hz above the series resonance frequency of the crystal. The oscillation point occurs where the "phase open loop" term goes to zero. Table 2 is the computer model's output for a 35 ohm crystal swept from 700 Hz to 2100 Hz above series resonance of the crystal. The output headings are summarized in Table 3. The explanations for the "E2" and "Ixstal" columns will follow in the next section of the paper.

CRYSTAL DRIVE ESTIMATION BY THE COMPUTER MODEL

The crystal used in the oscillator circuit is a 100 MHz, 5th overtone AT-cut. A major problem with AT-cut resonators is flexure mode coupling of other resonant responses within the crystal at fairly high drive levels. Crystal drive is the power dissipation in the resonator. It is determined by the series resistance of the crystal and the AC current through the resonant circuit by the formula: $P = I^2R$. The effect of the model coupling is pertubations in the frequency/temperature curve of the crystal. These unwanted frequency dips can cause sudden drops in frequency by as much as 2 to 3 ppm at specific temperatures over the operation range.

Figure 3 is an example of a crystal with temperature pertubations. During the design review of the crystal development for the oscillator project, a guard band of 2 mW of drive was imposed by the customer to screen the crystals for acceptance. The 2 mW drive was selected to secure against possible drive increases during the oscillator's life in the satellite. However, this estimated drive level caused frequency pertubations in most of the resonators. The yield through the screening process fell to a severely low level. Because of the computer program's ability to determine current gains around the oscillator loop, the analysis of the output parameters was used to re-evaluate a more reasonable screening level for the resonator drive. The end-of-life criterion could more accurately be determined.

For the drive prediction, a way to determine crystal current is needed. This was developed by straightforward network analysis from the output parameters of the program. The feedback network of gain block 1 is driven by the AC voltage developed at the junction of the capacitive tap C7 and C9. This AC voltage is designated "E2" by the program. E2 is calculated by the following formula:

$$E2 = I_{limit} \times G2 \times ZL$$

"I_{limit}" is the measured DC collector current of the oscillator transistor. An average value of 7.19 mA was used for this parameter. G2 is simply the actual gain ratio of the "DBG2" output parameter and ZL is as stated in Table 3. Multiplying

braid and cable to be determined in order to generate accurate computed results. Such information is not readily available thus this method of determining the shielding effectiveness of coaxial cable was not persued. Moreover, the physical orientation and installation of the cable can greatly affect the parameters of the model such as the spacing between the gaps in the braid, the size of the gaps in the braid, and the angular orientation of the braid wires with respect to the field within the cable.

Smith[8] presents a comparison of computed and measured surface transfer impedance impedance of RG-59/U cable. The impedance is composed of diffusion, inductive, and capacitive transfer impedance components. An error of approxiamtely 50% in the computed values of the transfer impedance components resulted revealing the difficulty of determining the physical parameters of the shield braid to generate an accurate model.

The information needed to make accurate calculations of the surface transfer impedance of a coaxial cable shield is difficult to obtain thus limits were calculated and direct measurements made of shielding effectiveness.

To determine the merits of double shielding, a comparison of single shielded versus double shielded cable was executed. For this comparison, single shield RG-59/U and double shield RG-223/U coaxial cable was used. The test is illustrated in Figure 1. A 50 ohm stripline was constructed to act as a radiating antenna. The stripline, terminated in 50 ohms, was then driven by the RF source in the network analyzer. The coaxial cable under test terminated in its characteristic impedance of 50 ohms was placed on top of the stripline and the energy leaking through the shield measured. Since the field near the stripline is very high and all fields must pass through the shield of the coax, interfering sources are attenuated greatly before reaching the detector, thus more accurate measurements can be made than if the minute energy emanating from the coax shield had been collected by the unshielded stripline. The results indicate an approximate 10 to 14 dB of shielding effectiveness is gained by adding the second shield. The quantity is approximate since some of the measurements were made very near the noise floor of the detection system. These measurements are relative and serve only to allow comparisons between cables. In order to determine the actual shielding effectiveness, field strength measurements must be made.

To carry out field strength measurements on double shield RG-214/U coaxial cable the antenna of Figure 2 was constructed. A receiver/generator was used as an excitation source and detection system. The cable, terminated in 50 ohms, was suspended from the ceiling in the center of the lab and driven by 10 Vrms (2 Watts) from the generator. The antenna was then used to probe the resulting field from all points on a 1 meter radius from the cable to locate and measure the maximum radiation for each test frequency. Figure 3 illustrates the test conditions and the data collected. A possible source of error in this measurement is the fact that the data was collected in an unshielded laboratory inside a steel framed building. Reflections, standing waves, RFI sources within the building and antenna VSWR contribute to the error in the measurements. However, the 100 dB shielding effectiveness derived from the measured field strength is the proper order of magnitude based on conversations with engineers at cable manufacturing facilities.[5]

To minimize sources of error and in an attempt to generate reproducible test conditions, practical field strength measurements were made on RG-214/U cable using the shielded room, calibrated EMI measurement instrumentation, and technical expertise at Honeywell Signal Analysis

Ilimit by ZL gives the maximum AC collector voltage. G2 then incorporates the loss to the output buffer. With E2 determined, the crystal current may then be calculated. At the capacitive tap, the crystal is a series element to the input of the oscillator transistor. The input impedance of the transistor and the base to ground capacitors C2 and C3 form a reactive divider. This voltage division is represented by "DBG1". G1, the actual gain ratio of "DBG1", is the value:

$$G1 = \frac{E1}{E2}$$

E1 is the voltage incident on the base of the oscillator transistor on the opposite side of the crystal. Therefore, the crystal current may be calculated by using the crystal impedance at the point of interest:

$$Ixstal = \frac{Vxstal}{Zxstal}$$; Vxstal is the voltage drop across the crystal Zxstal is the complex impedance of the crystal

$$Vxstal = E2 - (E2 \times G1) = E2 - E1$$

$$\text{therefore, } Ixstal = \frac{E2 - (E2 \times G1)}{Zxstal}$$

From this analysis, not only was an accurate crystal current determined but an easily measurable point, "E2", was found to make empirical measurements of crystal drive in the actual oscillator unit.

The voltage at E2 can be measured with a high impedance RF voltmeter. The capacitance of the voltmeter probe is approximately 2.2 pF which is only 6% of the capacitance of C9. Therefore, the loading impact to the circuit is minor. Table 4 lists the measured value of E2 for various crystals at acceptance screening. Notice that the values of the measured E2 voltage are within 5% of the E2 values predicted by the computer program. The predicted values for E2 of each crystal were determined by inserting the individual crystal parameters into the initialization of the input to the program. The calculated drive for crystal serial number 232:

$$(4.753 \text{ mA})^2 \times 39 \text{ ohms} = 881 \text{ microwatts}$$

Because of the accuracy of the predicted E2, the predicted Ixstal could be used to calculate the drive above. Since the calculated drive for the oscillator is under 1 mW, a re-evaluation was accomplished by varying the initialization table of the program by realistic end-of-life tolerances on the circuit elements and DC input. Table 5 lists impact to the drive budget of various tolerance changes of the oscillator circuit elements. Very little change is recorded by component changes due to tolerance drift. The DC input variance of the power supply is guard banded by +/-5%. By changing the DC input by +/-5% and measuring the E2 value with the RF meter, the worst case increase in drive was found to be less than 100 microwatts. Therefore, a more accurate guard band in drive was estimated to be 1.1 mW. An additional 400 microwatts was added to the guard

Center, Annapolis, Maryland. The test conditions are illustrated in Figure 4. Two 10 feet long pieces of RG-214/U were placed in the shielded room. The cables were connected together with a female to female N-type connector. Power from an RF power amplifier outside the shielded room provided the RF excitation for the test. A dummy load also outside the shielded room was used to terminate the coaxial cable under test. All connections in and out of the room were through bulkhead N-type connectors in the wall of the shielded room. Figure 5 illustrates the emissions measured at a distance of 1 meter from the two 10 feet lengths of RG-214/U at power levels of 10 watts and 100 watts. Theoretically the curves should always be separated by exactly 10 dB. However, the spectrum analyzer detection system plotter did not sample at identical frequencies for each of the power levels introducing differences in the shapes of the curves which are straight line segments between data points. Evidence of this effect is particularly evident in areas of the curves exhibiting high slopes or near maxima and minima of the curves. For example, a data point was plotted at 10 MHz for the 100 watt level but not for the 10 watt level. The slope is so large near 10 MHz that it appears the 10 watt curve does not track the 100 watt curve due to the error introduced by interpolating between data points on a rapidly changing curve. Taking sampling points into account, the areas of the curves with gradual slopes, particularly in the 2 to 5 MHz region, exhibit the 10 dB difference in field strength. Thus, if enough points are sampled to allow a smooth curve to be drawn between the data points without missing the extrema of the curves, emissions for any power level can be predicted. Figure 6 includes a third curve indicating the predicted emission level for a 1 KW signal based on the measured 100 W curve.

In an effort to obtain a numerical value for the surface transfer impedance of RG-214/U cable in order to calculate shielding effectiveness and thus emissions limits, Leonard Visser of the Belden Wire and Cable Research Center was contacted. Mr. Visser is in the process of measuring the surface transfer impedance of the complete line of coaxial cable produced by Belden. When contacted on June 11, 1985 he had not yet measured RG-214/U cable. However, his familiarity with the properties of similar coaxial cable already tested allowed him to estimate the surface transfer impedance to be in the range of 0.1 to 10 milliohms per meter over the frequency span of 2 to 30 MHz.[10]

Subsequently, Mr. Visser tested RG-214/U on July 9, 1985. The magnitude of the surface transfer impedance he measured over the frequency range 10 KHz to 500 MHz is illustrated in Figure 7. At 10 KHz the surface transfer impedance is essentially the DC resistivity of the coax shield or 4.6 milliohms per meter. The impedance reaches a minimum value (maximum shielding effectiveness) at 2 MHz and then increases with frequency.

Figure 8 illustrates the shielding effectiveness of double shield RG-214/U, single shield, triple shield, composite shield, and standard 0.012 inch thick solid copper shield semi-rigid coax. Shielding efficiencies were calculated from Figure 7 data for RG-214/U; from surface transfer impedance data presented in the Handbook of Wiring, Cabling, and Interconnecting for Electronics[1] for single, triple, and composite shields; and from the surface transfer impedance calculated from Equation 1 for 0.012 inch thick copper. Note that the triaxial composite shield cable consisting of a copper braid over a steel braid over insulation over another copper braid is superior to 0.012" thick solid copper at low frequency. This effect is attributable to the greater net thickness of the shield and reduction of

band to insure a margin. The new screening drive for crystal acceptance was reduced to 1.5 mW.

The empirical measurement technique was then used to set the oscillator for 1.5 mW drive level by increasing the power supply to arrive at the necessary E2 value. Table 4 summarizes the results of the screening test. The 1.5 mW "Ixstal" was determined by:

$$(1.5\ \text{mW})\ \text{Ixstal} = \sqrt{\frac{1.5\ \text{mW}}{\text{Xstal resistance}}}$$

The required E2 voltage is found by:

$$\frac{(\text{E2 predicted})(1.5\ \text{mW Ixstal})}{(\text{Ixstal predicted})} = 1.5\ \text{mW E2 measured}$$

The accuracy of the computer model is confirmed by the above discussion. Therefore, it should have the ability to predict some more difficult circuit parameters.

DETERMINATION OF COMPLEX CIRCUIT PARAMETERS BY THE PROGRAM MODEL

Figure 4 is a graph of four important output parameters of the program over a wide sweep of the circuit in 100 Hz increments. The various curves illustrate the operation of the Pierce oscillator. The loop gain is shown increasing to a peak at around 700 Hz above series resonance. This allows the oscillation build-up to occur before the oscillator achieves a steady state at "zero loop phase". Consequently, the Allen variance of the oscillator will decrease to a final steady time domain value. At the same time, the crystal current is seen building as the loop gain increases, peaking at 700 Hz. This corresponds to a crystal drive of 1.46 mW, almost 600 microwatts greater than the final steady state value. Again, the extra drive causes a rapid build-up of energy in the resonator to overcome the unstable loop phase at start-up. The start-up times measured for the oscillators were approximately 12 msec.

The E2 curve illustates the effect of the resonator impedance. The curve reaches a minimum approximately at series resonance of the crystal. This where the crystal has its lowest impedance and therefore loads E2 the most. As the phase approaches zero, the resonator circuit becomes increasingly higher in impedance. E2 rises until the resonator impedance reaches its maximum and E2 no longer changes. Notice that the E2 curve is very much like the passive network sweep of a crystal resonator. The phase of the loop steadily decreases to an operating point about 1400 Hz above series resonance. From Table 4, this gives an operation frequency of 100 MHz +/-2ppm for all of the series resonance frequencies listed. The oscillator indeed operates at 100 MHz. Further examination of the curves of Figure 4 allows gain margin, loaded resonator Q, and phase slope to be determined.

Just as the computer model can perform an open loop sweep of the modeled circuit, an actual empirical sweep may be accomplished. Figure 5 shows the test schematic for the empirical sweep. The circuit is broken at the input to the

the surface transfer impedance by the high initial permeability of the ferromagnetic steel braid as analyzed by Salt.[6] The three copper braids shield is superior as well as the net thickness of the three copper braids is also greater than 0.012 inch. At higher frequencies the capacitive component of the transfer impedance dominates and the shielding effectiveness decreases for both the three copper braids and the composite shield while the solid shield shielding effectiveness increases dramatically with the decreasing skin depth at higher frequencies. Also note that the shielding effectiveness of double shield coaxial cable is roughly 12 dB greater than that of the single shield with 90% coverage which agrees with the data derived from the comparative measurements previously discussed.

Figure 9 illustrates the electric field intensity generated by a 1 meter length of each cable carrying 1 KW measured at a distance of 1 meter, calculated from the shielding effectiveness curves of Figure 8 using the near field tangential electric field intensity equation for a current filament:

$$E_t = 30\alpha^2 L I \sin\Theta A_t \cos(v + \phi_r) \qquad (2)$$

where:

$A_t = [1-(\alpha r)^2 + (\alpha r)^4]/(\alpha r)^3$
L = length of current filament
λ = wavelength
I = current
Θ = angle
r = distance from current filament
$\alpha = 2\pi/\lambda$

It is evident from the data presented in Figure 9 that electromagnetic leakage at frequencies less than 10 MHz is not negligible. Approaching the question of leakage from practical viewpoint; the power that can be carried by a 1 meter length of RG-214/U without exceeding the emission limit of Figure 9 in the range 2 to 30 MHz was calculated. Incredibly, the maximum power is less than 500 microwatts.

The results of this research indicate that computational methods are good for establishing limits of shielding effectiveness and thus the level of leakage that can be expected from a coaxial cable. Practical measurements in the actual installation environment are very difficult due to interfering sources of RFI, the dependence of the measurement of the radiated fields on physical orientation of the cable, reflections and absorption of the RF energy from nearby objects and location of the measurement antenna. As shown by Simons[7] there is not good correlation between calculated and measured emissions due to these effects. Even field strength measurements made in shielded rooms are subject to the errors produced by reflections and standing waves present in such chambers. The shielded room also does not adequately simulate the actual installation of the cable.

The results of the predicted leakage calculations and actual measurements of electric field leakage from coaxial cables presented in this report are shocking when compared with the emissions limits imposed by the various standards. At modest power levels below 10 MHz, even certain types of solid shield coax do not provide adequate shielding to hold emissions below mandated limits. Fortunately, coaxial cable manufacturers have become cognizant of the engineer's need to have shielding effectiveness data in order to design equipment and systems to meet electromagnetic emissions standards and are in the process of making the data available to the RF design engineer in the form of surface transfer impedance measurements.

crystal. This occurs at the junction between gain block 1 and 2. The terminations at the circuit breaks are chosen to approximate those seen during closed-loop conditions. The input to gain block 1 is terminated by a paralleled resistor/capacitor combination equivalent to R13 and Zin2. The input to gain block 2 is terminated by a "dummy" crystal and capacitor in series to simulate the loading of gain block 1. A frequency synthesizer was used to drive the loop and a vector voltmeter was used to record phase and gain changes on either side of the open circuit. Probe A, the reference probe, measures the input to the loop, while probe B measures the phase and gain change. The vector voltmeter connects the loop in a way without completing the circuit.

The gain margin of the oscillator loop is the excess gain present in the circuit above that required for stable oscillation. By what is commonly referred to as the Nyquist criterion, the active gain and the feedback must satisfy the inequality $\alpha \times B > \text{or} = 1$. The gain margin is a guard band for this function. In other words, the excess gain allows an amount of loss due to detrimental effects such as transistor transconductance decrease or loop impedance increase. The greater the gain margin, the stronger the oscillator's ability to withstand such effects. Table 6 is the data gathered for an empirical open loop measurement of a typical 35 ohm crystal. At zero loop phase, a gain margin of 5.6 dB is calculated. Gain margin is found by the formula:

$$\text{Gmargin} = 20 \times \text{LOG}\left(\frac{B}{A}\right) - 20 \times \text{LOG}\ (\text{COS}\ \emptyset)$$

The value found on Figure 4 at the operating point is about 6 dB. This is an error of 7%. However, it should be noted that the empirical open loop sweep was done on small signal levels which may cause some error in measurement correlation.

The loaded Q of the resonator and the phase slope of the open loop are important parameters in the phase stability of the oscillator. The loaded Q of the resonator represents the actual resonance bandwidth of the crystal in the loop. By examining the crystal current in Figure 4, an estimate of the loaded Q can be made. The maximum current is 6.471 mA. The 3 dB current is 3.243 mA. Therefore, the calculated loaded Q is found by the formula:

$$Q_L = \frac{Fo}{BW_{3dB}}$$

A value of 34,305 is determined. This represents about 30% of the typical unloaded Q of the resonators which is generally true for Pierce oscillators. The phase slope is the rate of change in phase with frequency. This curve represents a transfer characteristic to frequency stability. The phase jitter of the oscillator is directly dependent on the phase slope. An operating point is found on a rather shallow portion of the curve. It may be assumed that the phase stability of the oscillator is not as great as it could be. Phase slope may be related to the loaded Q of the circuit by the following:

Shielding effectiveness calculations, used with a conservative safety margin, can prevent surprises in the EMI test lab and hold RFI in the equipment operating environment to safe levels.

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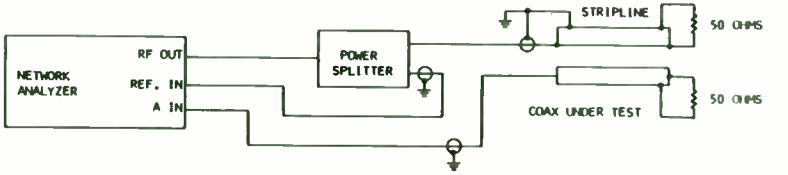


FIGURE 1

COMPARATIVE SHIELDING EFFICIENCY MEASUREMENT

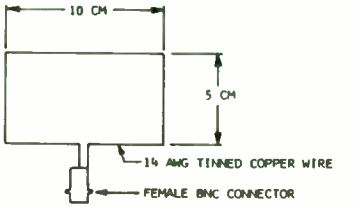
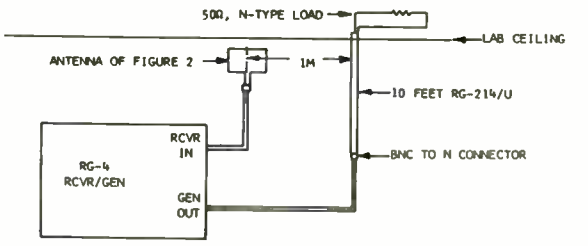


FIGURE 2

ANTENNA FOR FIELD MEASUREMENT



FREQUENCY, MHZ	SHIELDING EFFECTIVENESS, DB
12	103.3
13	101.6
14	100.0
15	99.3
16	93.3
17	89.9
18	81.6
19	88.4

FIGURE 3

RG-214/U LEAKAGE MEASUREMENTS

$$\frac{\Delta\theta}{\Delta f} = \frac{2Q_L}{fo}$$

However, the group delay of the oscillator is related by the relationship $Q = \pi \times fo \times \tau$, where τ is the group delay. The group delay through the oscillator is the propagation delay around the loop. Oscillators with large group delays exhibit very good short term stability in the time domain. The group delay is related to frequency jitter by:

$$\frac{\Delta f}{fo} = \frac{Q}{2\pi\, fo\, \tau}$$

The advantage of analyzing frequency jitter this way is that the θ and τ variables may be split into their individual components. 1) It is not in the scope of this paper to present this concept. However, the group delay can be calculated for the oscillator by the formula:

$$\frac{\Delta\theta}{\Delta f(360)} = \tau$$

This is directly proportional to the phase slope. From Figure 4, a value of 0.109 msec. is calculated at the operating point. The group delay may be determined in another way. Since the loaded Q is known, the group delay is found by:

$$\frac{Q_L}{fo\pi} = \tau$$

Again, the value of 0.109 msec. is calculated. The group delay for the oscillator has been determined in two different ways using the output parameters of the program. The loaded Q of the oscillator can allow a prediction of the phase noise response of the circuit.

The construction of the phase noise response occurs in three steps: the signal to noise floor, the noise rise due to white noise within the resonator bandwidth and the contribution of 1/f noise from the active device. The signal to noise ratio is found by the following:

$$SNR = 10 \log\left(\frac{Pavs}{FkT}\right)$$
$$SNR = Pavs - NF - 174 dBc/Hz$$

Pavs is the power available from the gain source. It can be determined by adding "DBG2", DBG1 and "DBOPLOP" from the program parameters. This represents the gain of the oscillator transistor. A value of 26.44 dB is found for the operation point of Table 2. Since no noise figure analysis was done for the oscillator amplifier, a value will have to be assumed. A value of 3.5 dB is reasonable for semiconductors of the type used in the oscillator circuit. This gives a signal to noise floor of 151 dB. The noise rise due to modulation within the resonator bandwidth can now be determined. A general formula used for this purpose is:

$$\mathcal{L}(fm) = -SNR - 3dB + 10\log\left(\frac{fo}{2fm\, Q_L}\right)$$

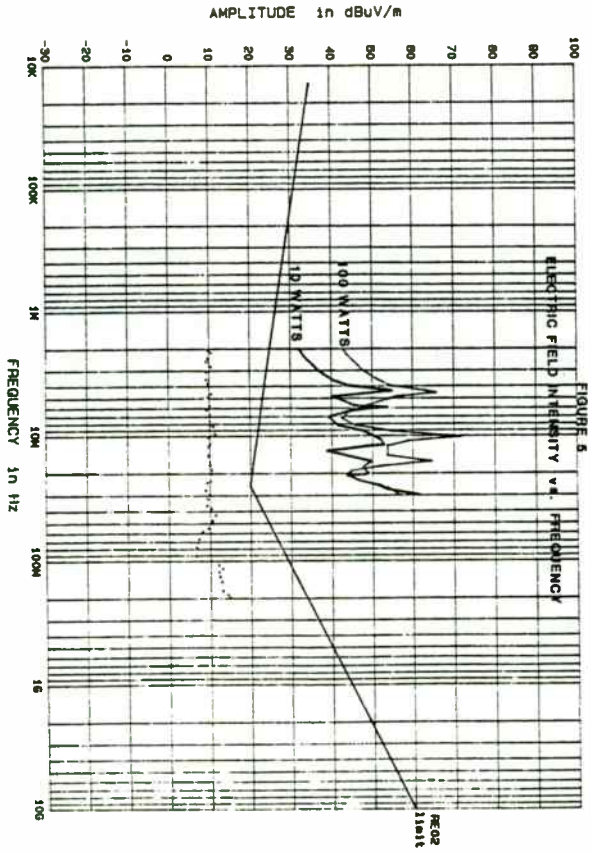


FIGURE 6

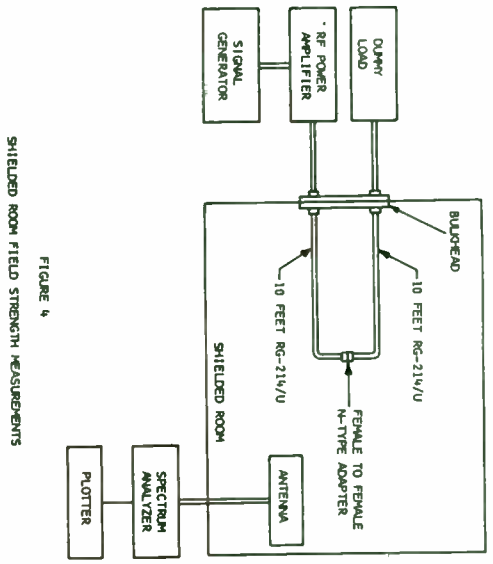


FIGURE 4

SHIELDED ROOM FIELD STRENGTH MEASUREMENTS

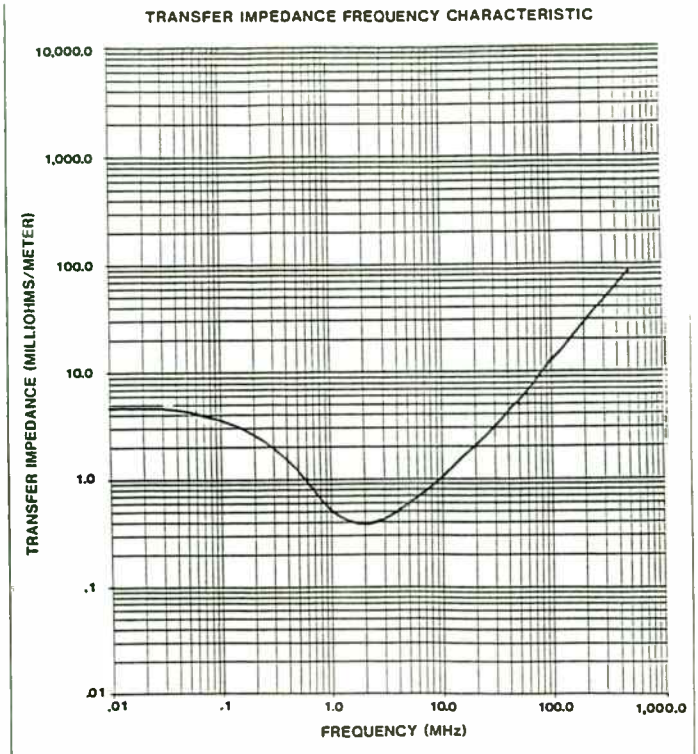


FIGURE 7

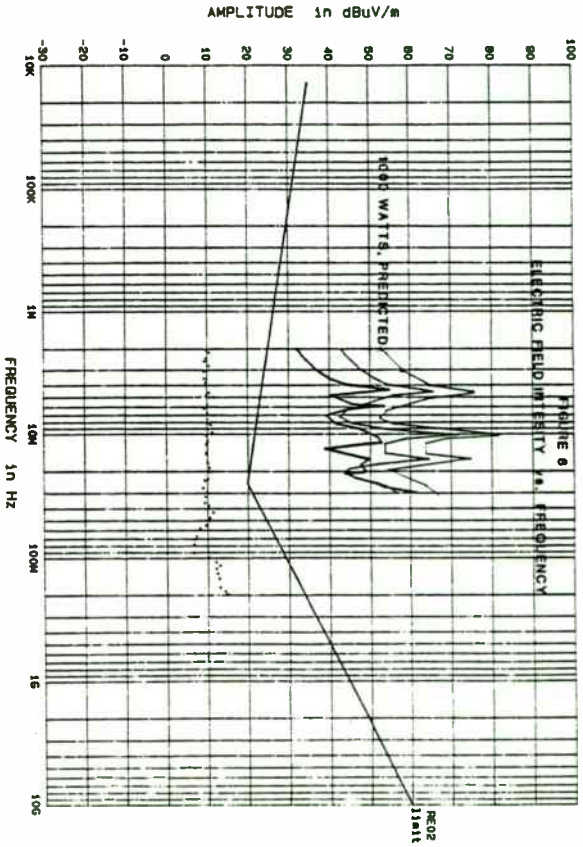


FIGURE 8

BELDEN	DATE	TRADE NUMBER
	7-9-85	8268

The formula relates the FM modulation index with the loaded Q of the circuit. 3 dB is subtracted due to AM contributions occurring simultaneously in the noise floor. Finally, the 1/f noise contribution is added. With an oscillator of this type, the major contribution of shot noise is from the transistor. The formula which can relate this contribution to the previously determined noise is:

$$(fm) = -SNR - 3dB + 10\log\left(\frac{fo}{2fm\ Q_L}\right) + 10\log\left(1 + \left(\frac{fo}{2fm\ Q_L}\right)^2\right)$$

Table 7 shows the phase noise prediction with the use of this formula to the actual measured noise of the circuit. The two predictions are based on the two loaded Q's available from the analysis. One is the 3 dB current bandwidth found from the computer program. The other is the phase slope determined from the open loop sweep of Table 6. The phase noise prediction is therefore fairly accurate both with the empirical and modeled open loop sweeps.

SUMMARY

The advantage of the computer model is clearly demonstrated by the above results. Rather straightforward network analysis produces a labor saving tool because of the computer's number handling capability. Insight gained by examining the analysis led to new empirical techniques for rather complex measurements. Because of the accurate characterization of the circuit, the operation of a Pierce oscillator was presented in graphic detail. Further examination of the output parameters allowed difficult but important circuit relationships to be determined. It is apparent that with more detailed analysis of the computer model's output, further work can be accomplished in the oscillator's design and improvement. Ultimately, the model could be generalized to meet various oscillator types and improve the understanding of crystal oscillator circuits.

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The author expresses his appreciation for the contributions of Pat Godwin to the development of the computer model.

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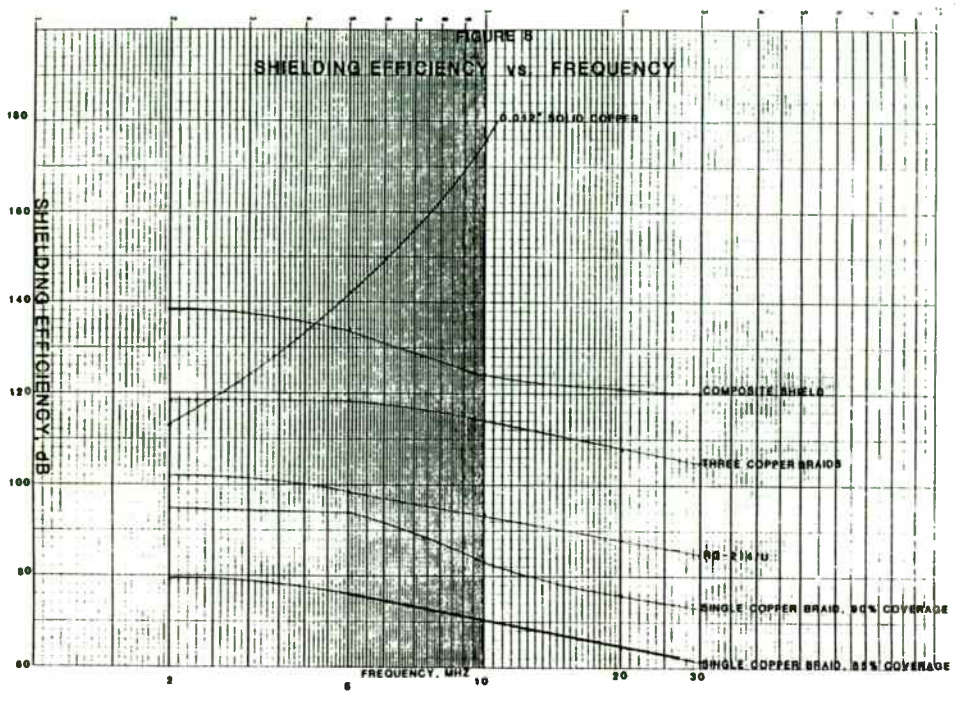

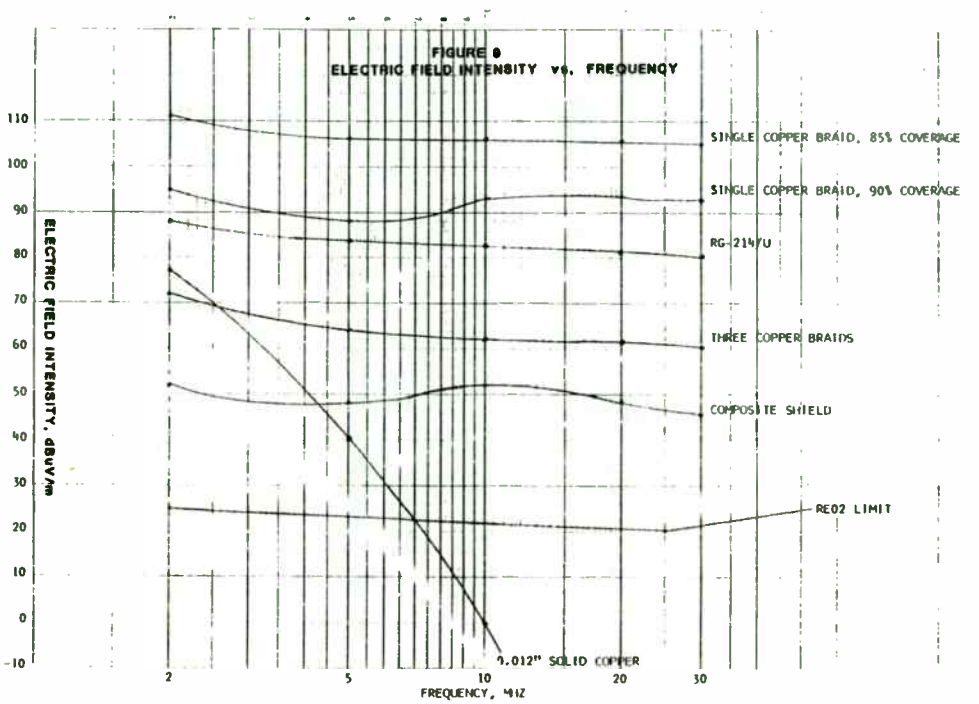

TABLE 1

C2 and C3: parallel capacitors to base of oscillator transistor

C0: stray capacitance of crystal enclosure (TO-5 style package)

C_1: motional capacitance of crystal resonator

R_1: series resistance of crystal resonator

Zin2: complex matrix of input impedance of the buffer amp

R13: coupling resistor between oscillator and buffer amp

C9: grounding capacitor of capacitive tap

R5: emitter degeneration resistor of buffer amp

C7: coupling capacitor of capacitive tap

RL1: resistance of collector tank inductor of oscillator

L1: inductance of collector tank inductor of oscillator

C5 and C6: tuning capacitors of collector tank of oscillator

F1: series resonance frequency of crystal

S_{11}, S_{12}, S_{21}, S_{22}: S parameters of oscillator transistor

FD	DBOPLOP	PHOPLOP	PIL	PHIL	DBI	PHI	DBO	PHO	E2	Ixtal	
700	9.508	44.300	119.196	-61.014	-6.2811	-120.018	-8.7509	51.162	0.313	6.471	
750	9.459	40.640	121.106	-59.870	-6.7723	-123.502	-8.4360	50.026	0.330	6.482	
800	9.373	36.992	123.333	-58.882	-7.2708	-126.646	-8.1667	48.707	0.347	6.470	
850	9.252	33.386	125.809	-58.069	-7.7708	-129.482	-7.9425	47.281	0.363	6.434	
900	9.098	29.848	128.457	-57.436	-8.2680	-132.039	-7.7608	45.808	0.378	6.375	
950	8.912	26.404	131.203	-56.980	-8.7592	-134.348	-7.6173	44.338	0.393	6.295	
1000	8.697	23.075	133.974	-56.689	-9.2422	-136.436	-7.5073	42.905	0.406	6.197	
1050	8.457	19.876	136.709	-56.546	-9.7158	-138.328	-7.4256	41.533	0.419	6.084	
1100	8.195	16.819	139.358	-56.530	-10.1789	-140.046	-7.3676	40.238	0.430	5.958	
1150	7.913	13.912	141.883	-56.621	-10.6312	-141.611	-7.3289	39.026	0.439	5.821	
1200	7.616	11.157	144.257	-56.799	-11.0724	-143.038	-7.3059	37.900	0.448	5.677	
1250	7.307	8.556	146.466	-57.044	-11.5026	-144.345	-7.2954	36.859	0.455	5.529	
1300	6.987	6.107	148.500	-57.341	-11.9219	-145.543	-7.2948	35.899	0.462	5.377	
1350	6.660	3.804	150.360	-57.674	-12.3306	-146.644	-7.3018	35.017	0.467	5.225	
1400	6.328	1.643	152.051	-58.033	-12.7291	-147.659	-7.3147	34.207	0.472	5.073	900uW
1450	5.992	-0.383	153.578	-58.408	-13.1177	-148.597	-7.3322	33.462	0.475	4.923	848uW
1500	5.654	-2.282	154.954	-58.791	-13.4969	-149.465	-7.3530	32.779	0.479	4.776	
1550	5.315	-4.061	156.188	-59.176	-13.8669	-150.270	-7.3763	32.151	0.481	4.633	
1600	4.977	-5.727	157.292	-59.559	-14.2283	-151.019	-7.4014	31.573	0.483	4.493	
1650	4.640	-7.289	158.278	-59.936	-14.5814	-151.716	-7.4276	31.040	0.485	4.359	
1700	4.306	-8.752	159.158	-60.304	-14.9267	-152.366	-7.4546	30.549	0.486	4.228	
1750	3.974	-10.125	159.941	-60.662	-15.2644	-152.973	-7.4819	30.096	0.487	4.103	
1800	3.645	-11.413	160.637	-61.009	-15.5951	-153.542	-7.5094	29.676	0.487	3.983	
1850	3.319	-12.623	161.257	-61.344	-15.9189	-154.074	-7.5367	29.288	0.488	3.867	
1900	2.997	-13.760	161.807	-61.666	-16.2363	-154.574	-7.5638	28.927	0.488	3.757	
1950	2.678	-14.830	162.295	-61.976	-16.5475	-155.044	-7.5905	28.592	0.488	3.650	
2000	2.364	-15.837	162.729	-62.272	-16.8530	-155.487	-7.6168	28.281	0.487	3.549	
2050	2.054	-16.786	163.113	-62.557	-17.1529	-155.903	-7.6425	27.990	0.487	3.452	
2100	1.747	-17.682	163.454	-62.829	-17.4474	-156.296	-7.6676	27.718	0.487	3.359	

Table 2

Notes: 1) C5 = 42pF, F1 ≈ 100 000 000 – 1200 Hertz; FD = F – F1

Table 1. Computer Model predicted response (open loop) for a 35 ohm crystal. 7/11/84

DESIGN AND ANALYSIS OF FOURTH AND FIFTH ORDER INDIRECT SYNTHESIZER LOOPS

by
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Phase locked loops are applied extensively as indirect frequency synthesizers. Most design techniques draw on the vast array of control system theory, particularly second order systems as described by Gardener[1] and others and the third order system of Przedpeiski.[2]

Many applied systems are of higher order due to spurious poles contained in loop components or filtering added to suppress the loop reference frequency sidebands. This paper presents techniques which allow design of systems with four or more poles by compensation of a three pole starting point.

The basic phase locked loop is shown in Figure 1 with a typical BODE plot. Dynamic performance is determined by the design of the loop filter. Oscillator phase noise suppression and transient response are typical design drivers. Two open loop response poles occur due to the VCO at zero frequency and the loop integrator pole, usually modeled at zero frequency. The remaining poles are contained in the loop filter and as spurious poles in other components. Setting values for the loop components to

FIGURE 1. THE BASIC PLL AND ITS BODE PLOTS

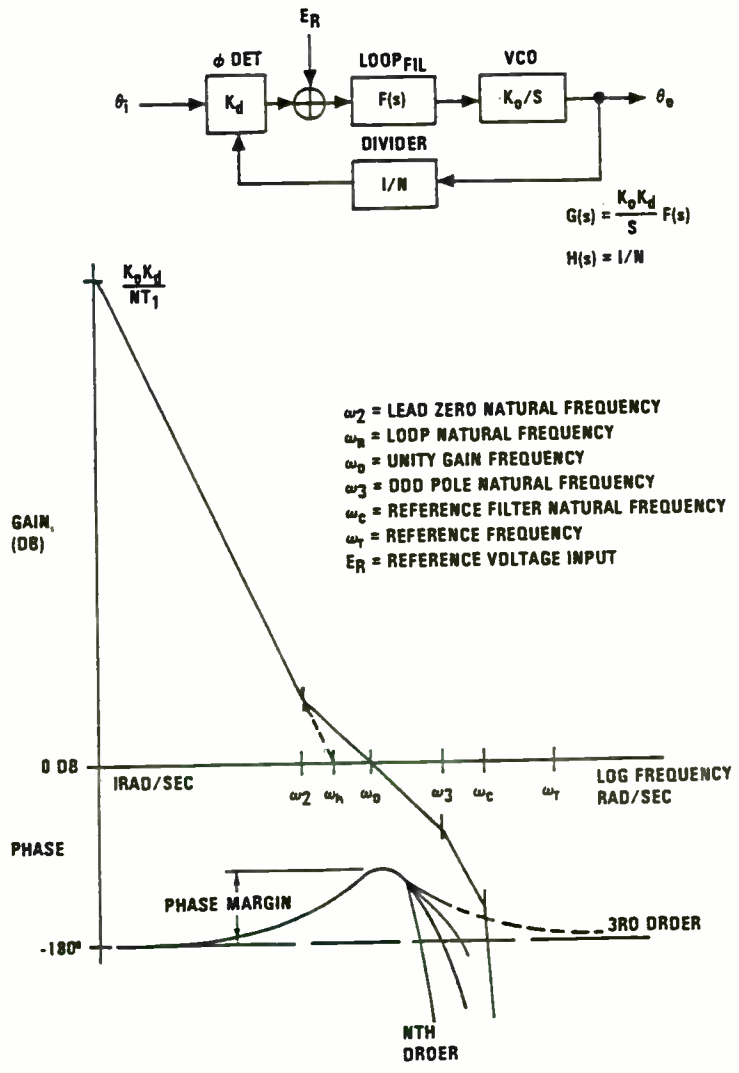


TABLE 3

FD: offset + or - from crystal series resonance in Hz

DBOPLOP: open loop gain in dB

PHOPLOP: open loop phase in degrees

PZL: absolute magnitude of collector load of oscillator transistor in ohms

PHZL: polar angle of collector load in degrees

DBG1: circuit loss of gain block 1 in dB

PHG1: phase shift associated with gain block 1 in degrees

DBG2: circuit loss of gain block 2 in dB

PHG2: phase shift associated with gain block 2 in degrees

TABLE 5

Circuit Element	Tolerance Change	Drive at Zero Phase	Frequency offset From Series
Nominal 35 ohms xtal osc.		798 x 10^{-6} watts	1500 Hz
C7 and C9	C7 +1%, C9 -1%	800 x 10^{-6} watts	1500 Hz
C5	- .166pF	820 x 10^{-6} watts	1500 Hz
C5	+0.166pF	825 x 10^{-6} watts	1450 Hz
C2 and C3	(.2 + C3) -3pF	808 x 10^{-6} watts	1500 Hz
Nominal 39 ohm crystal		840 x 10^{-6} watts	1400 Hz
Nominal 40 ohm crystal		790 x 10^{-6} watts	1550 Hz

TABLE 4

XSTAL SERIAL #	SERIES RESISTANCE	Co	Cl	Fseries	COMP. PRED. E2	COMP. PRED. Ixstal	MEASURED E2	1.5mW Ixstal	1.5mW E2
232	39 ohms	2.34pF	0.00039pF	99.998510	486 mV	4.753 mA	500 mV	6.20 mA	652 mV
237	35 ohms	2.36pF	0.00038pF	99.998530	519 mV	5.429 mA	515 mV	6.55 mA	621 mV
214	35 ohms	2.40pF	0.00040pF	99.998180	518 mV	5.486 mA	519 mV	6.55 mA	619 mV
228	34 ohms	2.32pF	0.00041pF	99.998200	522 mV	5.497 mA	521 mV	6.64 mA	629 mV
221	35 ohms	2.30pF	0.00042pF	99.998250	520 mV	5.396 mA	520 mV	6.55 mA	631 mV
232	39 ohms	2.34pF	0.00039pF	99.998280	514 mV	5.028 mA	519 mV	6.20 mA	639 mV
246	34 ohms	2.32pF	0.00036pF	99.998160	521 mV	5.533 mA	520 mV	6.64 mA	624 mV
239	34 ohms	2.28pF	0.00042pF	99.998440	523 mV	5.450 mA	523 mV	6.64 mA	637 mV
230	34 ohms	2.24pF	0.00041pF	99.998280	522 mV	5.510 mA	520 mV	6.64 mA	626 mV
215	37 ohms	2.20pF	0.00036pF	99.998580	516 mV	5.287 mA	519 mV	6.36 mA	624 mV
244	34 ohms	2.28pF	0.00042pF	99.998410	523 mV	5.450 mA	520 mV	6.64 mA	627 mV
282	42 ohms	2.16pF	0.00041pF	99.998690	511 mV	4.850 mA	518 mV	5.98 mA	638 mV
283	42 ohms	2.14pF	0.00038pF	99.998870	517 mV	4.825 mA	517 mV	5.98 mA	640 mV
291	44 ohms	2.08pF	0.00033pF	99.998990	511 mV	4.649 mA	508 mV	5.83 mA	637 mV
284	47 ohms	2.12pF	0.00040pF	99.998920	507 mV	4.452 mA	510 mV	5.65 mA	647 mV
275	42 ohms	2.18pF	0.00038pF	99.998730	511 mV	4.819 mA	517 mV	5.97 mA	641 mV
281	39 ohms	2.19pF	0.00042pF	99.998860	515 mV	5.073 mA	512 mV	6.20 mA	625 mV
265	39 ohms	2.19pF	0.00042pF	99.998640	515 mV	5.073 mA	517 mV	6.20 mA	631 mV
286	44 ohms	2.12pF	0.00035pF	99.998930	509 mV	4.719 mA	512 mV	5.84 mA	633 mV

produce a desired response is the goal of the design process. Several critical frequencies are defined on the BODE plot. Of the six shown ω_o and ω_r , are usually fixed by tuning step requirements and VCO phase noise suppression or tuning speed requirements. This leaves ω_2, ω_3 and ω_c as variables to set other performance parameters.

SPURIOUS POLES

Spurious poles are those that occur in various components usually not by design, but due to some component limitation. These Poles are not contained in the simple loop model, but do influence actual hardware performance. A typical spurious pole occurs due to the finite gain of real operational amplifiers. Figure 2 shows a loop filter with its spurious pole due to limited high frequency gain. This pole at $10\,\omega_o$ will reduce loop phase margin by 5.7 degrees. Such poles can be included in the loop design using a compensation technique.

REFERENCE SIDEBAND FILTERS

Another difference between model and hardware occurs in the use of multi-pole filters to reduce the reference frequency sidebands. These sidebands are caused by the reference frequency

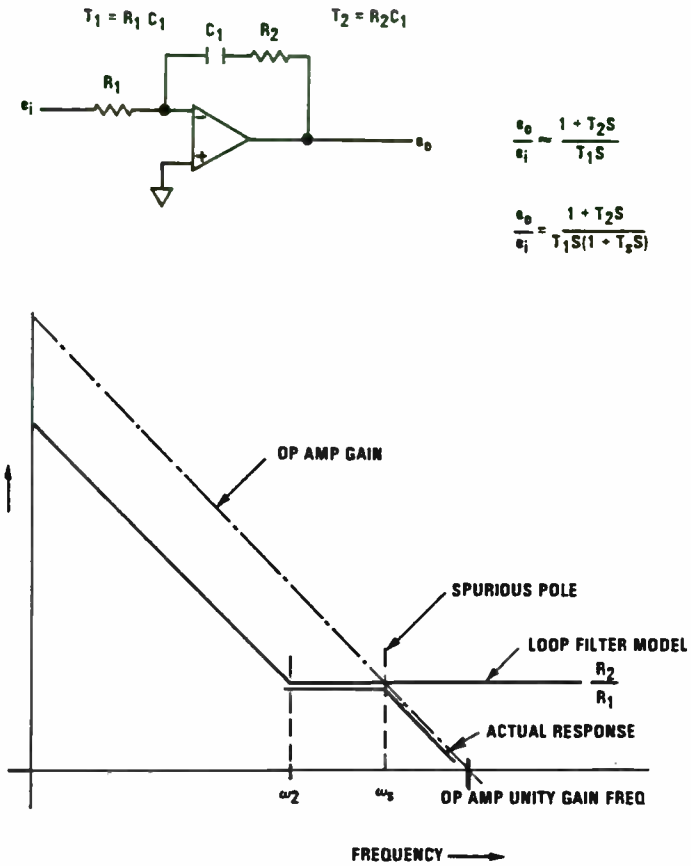


FIGURE 2. LOOP FILTER SPURIOUS POLE GENERATION

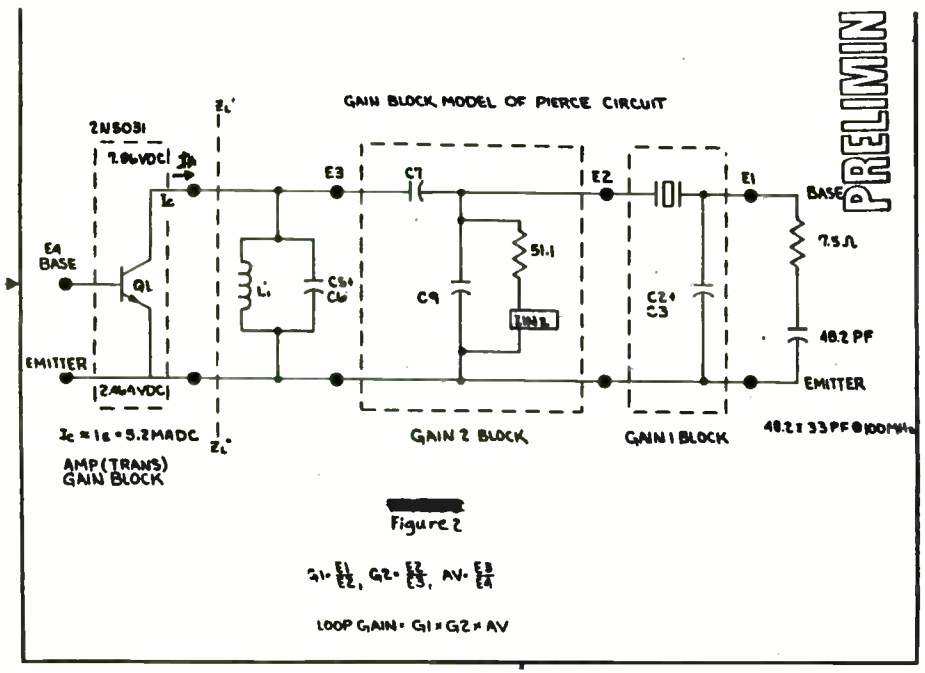


Figure 2

$G1 = \frac{E1}{E2}$, $G2 = \frac{E2}{E3}$, $AV = \frac{E3}{E4}$

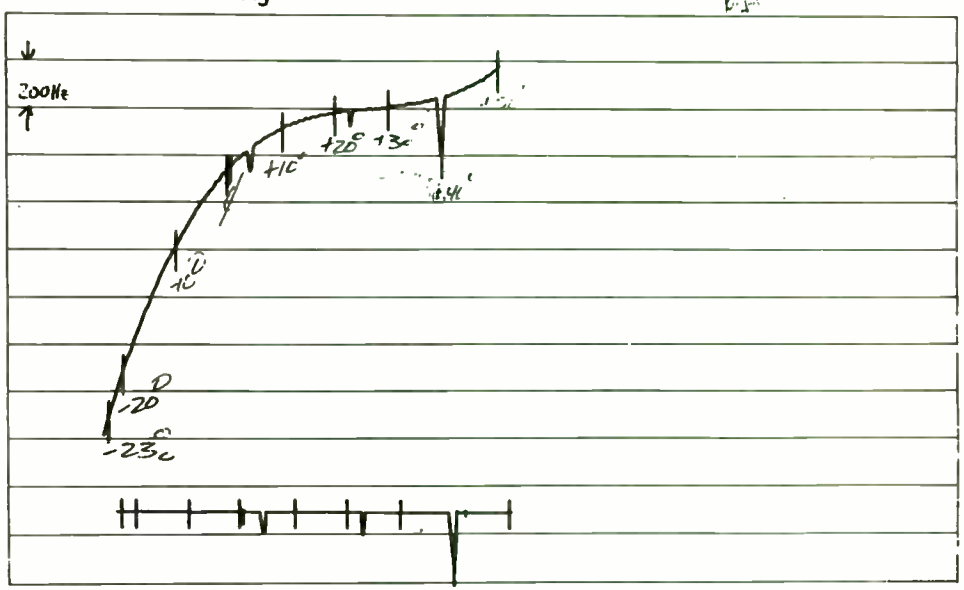
LOOP GAIN = G1 × G2 × AV

PIEZO CRYSTAL COMPANY
CARLISLE, PA 17013

FREQUENCY _____ MHz
SERIAL NO. _____ SCALE _____ PPM/DIV
DATE _____

FREQUENCY _____ AT _____
LOAD _____ pF Co _____ pF
INDUCTANCE _____ MHY Ci _____ pF
RESISTANCE _____ OHMS Q _____

Figure 3



TEMPERATURE MARKED AT 10°C INTERVALS

output of the phase detector reaching the VCO input. Filters added to reduce the sideband level are often used, but not included in the design equations. This results in a difference between calculated and actual performance due to reduced phase margin and unity gain frequency. The detailed loop model of Figure 3 shows a typical reference filter and fifth order loop configuration.

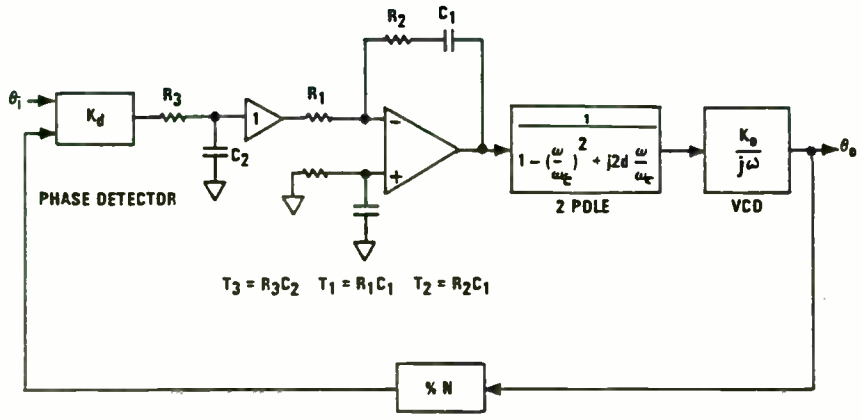


FIGURE 3. DETAILED LOOP MODEL

REFERENCE SIDEBAND LEVEL

The loop reference frequency must be several times greater than the unity gain frequency if linear continuous data analysis is to be valid. With loop gain at ω_r much less than one, the gain from phase detector to VCO output is essentially the forward gain of the loop. With a given static phase error, reference sidebands are evaluated as shown in Figure 4 for phase detectors with logic level outputs.

The input signal at ω_r consists of the fundamental component of the pulsed output of the phase detector. This is 2 times the pulse duty cycle times the peak output voltage. This voltage is filtered by F(s), the loop filter, and applied to the VCO producing phase modulation of Ko/ω_r radians per volt. If this modulation is small, less than six degrees, the sidebands will be 20 log $\Delta\theta/2$ dB below the VCO output. Output pulse width for a given static error

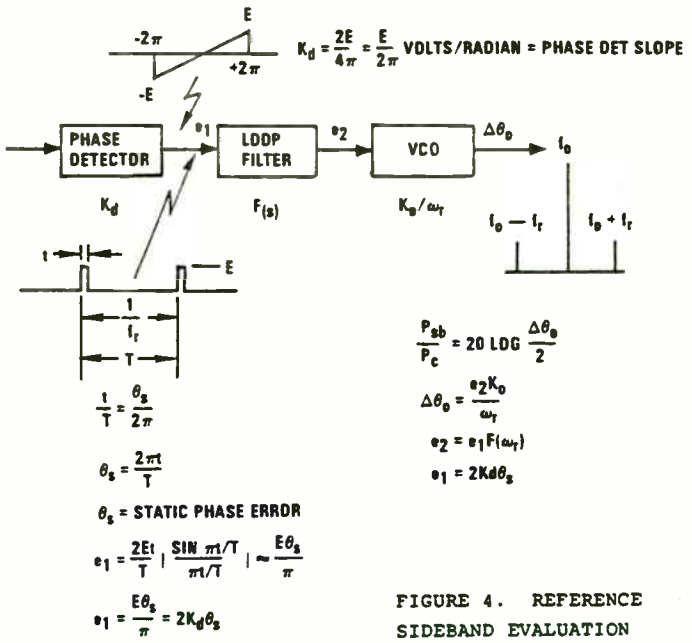
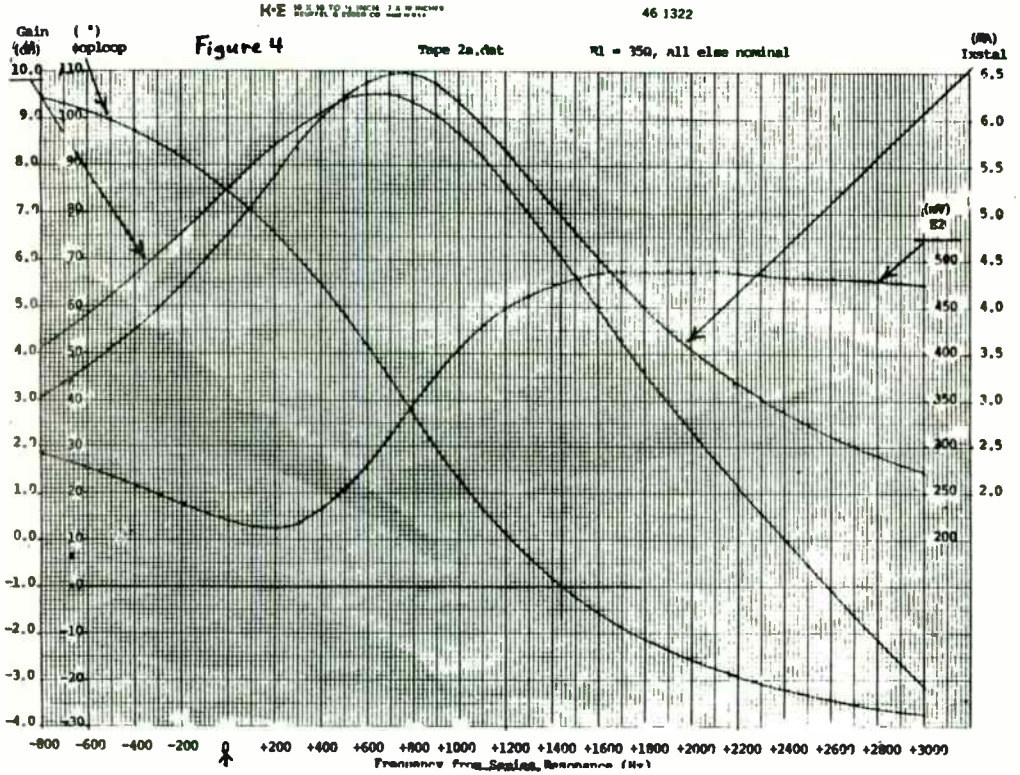


FIGURE 4. REFERENCE SIDEBAND EVALUATION



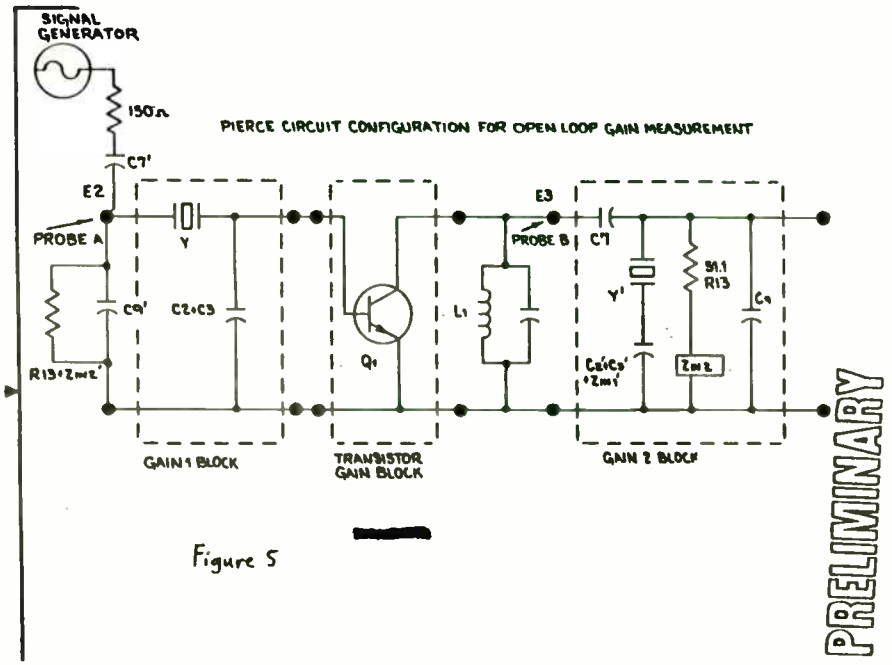


Figure 5

PRELIMINARY

is dependant on phase detector configuration. The popular phase - frequency detectors such as the Motorola MC4044 produce a pulse width approaching a constant of 10 to 20 nanoseconds at zero phase difference. Given the pulse width and loop filter characteristics, the sideband level can be determined and the filter requirements established. As the unity gain frequency ω_o and reference frequency ω_r become closer the suppression of the sidebands may require complex filter circuits. If the complex filters poles are known, the suppression can be calculated as shown in Figure 5.

THIRD TO FIFTH ORDER COMPENSATION TECHNIQUE

A third order loop is designed for optimum phase margin by locating unity gain and minimum phase at the same frequency. Figure 6 shows a BODE plot for an optimum loop. This is a good choice for tunable synthesizers since the phase margin has small variation with variable divider ratio N. This optimum can be closely approached for higher order loops by a compensation process. As the additional poles reduce gain and increase phase at the desired ω_o the loop filters T_1 and T_3 can be modified to maintain near optimum conditions. This procedure is quite successful for large separations between ω_o and ω_c, the filter cut frequency, and remains useful, but not optimum as ω_c approaches ω_o.

LOOP ORDER	REFERENCE FREQUENCY GAIN
2ND	$20 \log \frac{\omega_o}{\omega_r}$
3RD	$20 \log \frac{\omega_o}{\omega_r} + 20 \log \frac{\omega_3}{\omega_r}$
4TH	$20 \log \frac{\omega_o}{\omega_r} + 10 \log \left(\frac{1}{\left(1 - \left(\frac{\omega_c}{\omega_r}\right)^2\right)^2 + \left(2d \frac{\omega_c}{\omega_r}\right)^2} \right)$
5TH	$20 \log \frac{\omega_o}{\omega_r} + 20 \log \frac{\omega_3}{\omega_r} + 10 \log \left(\frac{1}{\left(1 - \left(\frac{\omega_c}{\omega_r}\right)^2\right)^2 + \left(2d \frac{\omega_c}{\omega_r}\right)^2} \right)$
NTH N EVEN	$20 \log \frac{\omega_o}{\omega_r} + \sum_{F=3}^{N-2} 10 \log \left(\frac{1}{\left(1 - \left(\frac{\omega_{cF}}{\omega_r}\right)^2\right)^2 + \left(2d_F \frac{\omega_{cF}}{\omega_r}\right)^2} \right)$
NTH N ODD	$20 \log \frac{\omega_o}{\omega_r} + 20 \log \frac{\omega_3}{\omega_r} + \sum_{F=4}^{N-3} 10 \log \left(\frac{1}{\left(1 - \left(\frac{\omega_{cF}}{\omega_r}\right)^2\right)^2 + \left(2d_F \frac{\omega_{cF}}{\omega_r}\right)^2} \right)$

FIGURE 5. REFERENCE FREQUENCY GAIN VERSUS LOOP ORDER

HARMONIC FILTERING AT UHF AND MICROWAVE FREQUENCIES

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The need for good filtering at a reasonable cost, size and performance is important to the designer of communications systems and/or equipment. For instance, harmonic suppression in oscillators have traditionally utilized low or band pass filter circuits to reduce distortion. These types of filters usually have well defined "skirt(s)" and high out-of-band rejection that require coupled, multi-element, high Q resonators.

At UHF and microwave frequencies, distributed elements (transmission lines of prescribed impedance) are employed to achieve an acceptable design due to their higher Q and predictability at microwave frequencies compared with standard lumped elements. However, distributed element filters also have problems. Tuning ("tweaking") multi-distributed elements in production is tedious and odd frequency reentrant modes are omnipresent. Tuning is a problem in that the lengths of the distributed elements must be altered (shortened/lengthened) in the alignment of the filter. This is not easy since the multi-resonant elements interact. The reentrant issue is one that is difficult to deal with in design and generally requires a compromise in performance to minimize its effect. By concentrating on the harmonic frequencies and the reentrant nature of distributed elements, a designer can turn a problem into a simple solution.

Before actually designing any filter using transmission lines, it is important to understand transmission line resonant circuits and their reentrant behavior. The general expression for the impedance down a dissipationless transmission line is:

$$Zin = Zo*((Zl+jZo*\tan(B*l))/(Zo+jZl*\tan(B*l))) \qquad \text{(Eq.1)}$$

where: Zo = characteristic impedance of the transmission line

B = 2*Pi/L

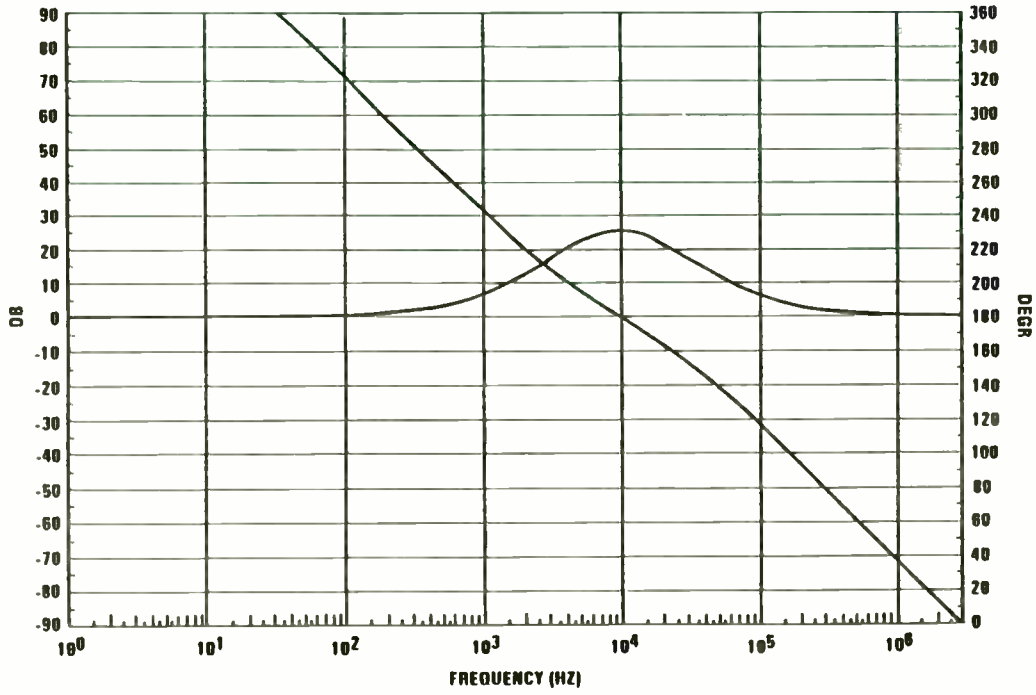
L = the frequency wavelength in the transmission line.

l = the length of the transmission line between Zin & Zl.

Zl = the load impedance on the end of the line.

To form a simple minimum loss resonant circuit, Zl can be a short-circuit (Zl=0) or Zl can be an open-circuit (Zl=00). In reality, at microwave frequencies even a good short-circuit is slightly inductive (due to its finite length) and an open-circuit is slightly capacitive (due to end fringing capacitance). Both these parasitic effects require the transmission line to be

FIGURE 6. BODE PLOT FOR AN OPTIMUM 3rd ORDER LOOP



This procedure maintains constant phase at ω_o by moving T_3 to a value which reduces its phase shift by that of a two pole filter with a given cut-off frequency and damping factor. The loop may be designed from parameters of the third order loop plus two, ω_c and d, for the filter. Any two poles, including two isolated spurious poles can be defined by a natural frequency ω_c and a damping factor d.

Figure 7 gives the design equations for third and fifth order loops. An open loop pole zero plot on the S-plane is shown in Figure 8. Here the path of two complex poles moves on constant d radials toward the origin as the ω_3 pole moves toward infinity on the negative real axis. As the real parts of the poles near equality, they become 3 pole filters with familiar names such as Butterworth, Bessel or Chebyshev. These pole locations can be normalized to the ω_3 values as shown in Figure 9. As ω_c is decreased beyond this point ω_3 moves very rapidly, due to its relatively low phase slope at ω_o, and the compensated five pole model finally fails as ω_3 goes to infinity. Now the loop becomes fourth order. This condition can be used to define a near optimum fourth order loop consisting of a second order loop plus a two pole reference filter.

slightly longer to achieve a desired Zin that would normally be predicted by Eq.1.

If Zl=0 (short-circuit load) is substituted into Eq.1 then:

Zin = Zsc = jZo*Tan(2*Pi*l/L) (Eq.2)

From the transcendental nature of Eq.2, it is apparent that the impedance of a shorted transmission line has more than one unique length; (l) for a given wavelength, (L) at which it will be series resonant at Zsc = 0, and parallel resonant at Zsc = 00. Therefore, from Eq.2, the following information can be derived:

Zsc = 0 when l = 0, L/2, L, (3/2)*L, 2*L, ...

Zsc = 00 when l = L/4, (3/4)*L, (5/4)*L, (7/4)*L, ...

If Zl = 0 (open-circuit load) and is substituted into a rearranged form of Eq.1 then:

Zin = Zoc = -jZo*Cot(2*Pi*l/L) (Eq.3)

Eq.3 is also transcendental, and it is apparent that the impedance of an open transmission line has more than one unique length (l) for a given wavelength (L) at which it will be parallel resonant at Zoc = 00 and series resonant at Zoc = 0. From Eq.3 the following information can be derived:

Zoc = 00 when l = 0, L/2, L, (3/2)*L, 2*L, ...

Zoc = 0 when l = L/4, (3/4)*L, (5/4)*L, (7/4)*L, ...

From inspection of the derived length (l) data for Zsc and Zoc, it can be concluded that the shortest or fundamental line for a distributed resonant circuit is one-quarter wavelength (L/4). This excludes l=0 because it is outside the boundary conditions for a finite resonant element.

Thus far the discussion of distributed resonant circuits has been confined to a fixed wavelength (L) or frequency with a variable line length (l). This constraint has allowed the concept of the fundamental one-quarter wavelength to be established as a basic resonant building block for a filter. From a practical stand point (l) is fixed and by definition (L) is variable across the frequency spectrum. The relationship between wavelength (L) and frequency (F) is:

FIGURE 7.

DESIGN EQUATIONS FOR THIRD AND FIFTH ORDER LOOPS

THIRD ORDER

$$T_{33} = \frac{1}{\omega_0}(\sec\phi_m - \tan\phi_m)$$

$$T_{23} = \frac{1}{\omega_0^2 T_{33}}$$

$$T_{13} = \frac{K_0 K_d}{N\omega_0^2}\left(\frac{1+\omega_0^2 T_{23}^2}{1+\omega_0^2 T_{33}^2}\right)^{1/2}$$

FIFTH ORDER

$$T_{35} = \frac{1}{\omega_0}\tan\left[\tan^{-1}(\sec\phi_m - \tan\phi_m) - \tan^{-1}\left(\frac{2d\omega_0/\omega_c}{1-\omega_0^2/\omega_c^2}\right)\right]$$

$$T_{25} = \frac{1}{\omega_0(\sec\phi_m - \tan\phi_m)}$$

$$T_{15} = \frac{K_0 K_d}{N\omega_0^2}\left(\frac{1+\omega_0^2 T_{25}^2}{1+\omega_0^2 T_{35}^2}\right)^{1/2}\left(\frac{1}{\left(1-\frac{\omega_0^2}{\omega_c^2}\right)^2+\left(2d\frac{\omega_0}{\omega_c}\right)^2}\right)^{1/2}$$

T_{nm} = Nth TIME CONSTANT OF AN M POLE LOOP
K_0 = VCO GAIN
K_d = PHASE DETECTOR GAIN
N = DIVIDER RATIO
ω_0 = UNITY GAIN FREQUENCY
ϕ_m = PHASE MARGIN
ω_c = NATURAL FREQUENCY OF TWO POLE REFERENCE FILTER
d = DAMPING FACTOR OF TWO POLE REFERENCE FILTER

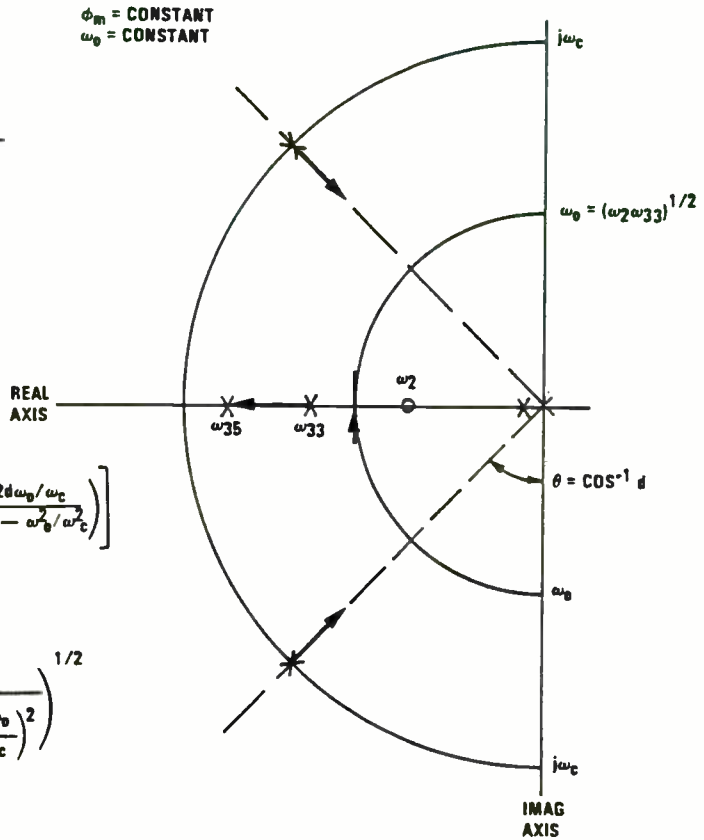


FIGURE 8. OPEN LOOP POLE ADJUSTMENT FOR THE 5th ORDER COMPENSATION WITH CONSTANT d

POLE CONFIG	OPEN LOOP		CLOSED LOOP		
	DAMPING FACTOR	ω_c/ω_3	ϕ_m	G_m	ω_T REJ AT $9\omega_0$
BESSEL	0.75	0.94	40° 50° 60°	11.7 OB 15.1 OB 17.8 OB	34 OB 29 OB 25 OB
BUTTERWORTH	0.50	1.0	40° 50° 60°	10.6 OB 12.8 OB 15.4 OB	37 OB 31 OB 24.7 OB
CHEB 3 OB	0.16	3.0	40° 50° 60°	16.9 OB 18.2 OB 21.1 OB	27.4 OB 19 OB 21.3 OB

ϕ_m = PHASE MARGIN
G_m = GAIN MARGIN

FIGURE 9. 5th ORDER LOOPS WITH SOME COMMON FILTER POLE CONFIGURATIONS

L = Vp/F (Eq.4)

where: Vp = velocity of propagation of the wave within the line.

For purposes of further discussion, the angular expression in Eq.2 and Eq.3 can be rewritten in the following form:

2*Pi*l/L = (Pi/2)*(F/Fo) (Eq.5)

where: l = Lo/4

Lo = Vp/Fo

Fo = fundamental resonant frequency

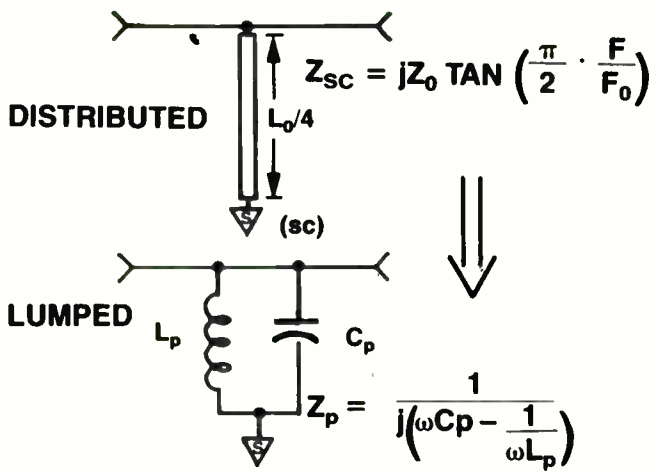


Figure 1.

Figures 1 and 2 show Lo/4 shunt transmission lines with short-circuit and open-circuit loads respectively. Their analogous lumped element equivalent is shown adjacent to them.

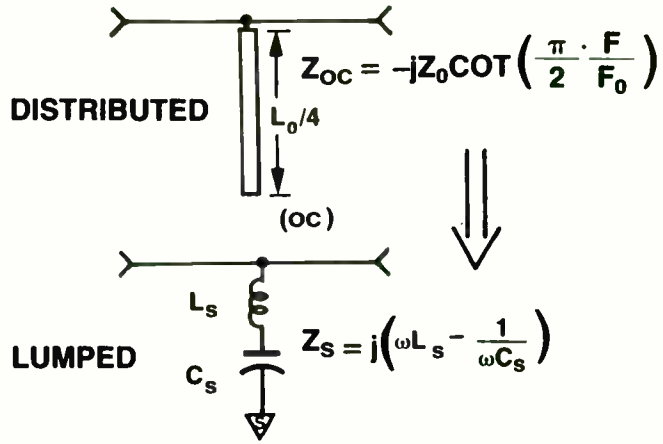


Figure 2.

FOURTH ORDER DESIGN TECHNIQUE

A fourth order loop occurs when T_3 goes to zero using the fifth order compensation technique. At this point the two pole filter has the same phase shift as the ω_3 pole in the third order loop.

This condition can be used to derive the filter characteristics for a fourth order loop. Figure 10 shows this process starting with the condition that $T_3 = 0$ and T_2 set at the third order starting point. The resulting design equations show the ratio of filter cutoff frequency to unity gain frequency set by the phase margin and filter damping factor. Figure 11 plots frequency ratio and gain margin as a function of phase margin and damping factor. Relative pole locations for this configuration are shown in Figure 12 with the progression of ω_3 from its third order position at ω_{33} through the fifth order ω_{35} range to infinity, which produces the fourth order loop. Constant phase margin and unity gain frequency are maintained by the design equations.

GAIN MARGIN

Gain margin is the open loop loss at the frequency where open loop phase equals 180°. Second and third order loops have infinite gain margins. Their loop gains can be increased indefinitely

FIGURE 10.

FOURTH ORDER LOOP AS A LIMIT FIFTH ORDER LOOP

1. 5TH $T_3 = T_{35} = \frac{1}{\omega_0} \text{TAN} \left[\text{TAN}^{-1}(\text{SEC } \phi_m - \text{TAN } \phi_m) - \text{TAN}^{-1} \left(\frac{2da}{1 - a^2} \right) \right]$
2. 4TH $T_3 = T_{34} = 0$
3. $\text{SEC } \phi_m - \text{TAN } \phi_m = \frac{2da}{1 - a^2}$
4. LET $\text{SEC } \phi_m - \text{TAN } \phi_m = K$
5. FROM 3

   $K = \frac{2da}{1 - a^2}$
6. SOLVING FOR a

   $a = -\frac{d}{K} \pm \left(\frac{d^2}{K^2} + 1 \right)^{1/2}$

GIVING THE FOLLOWING DESIGN EQUATIONS

$$T_{14} = \frac{K_0 K_d}{N\omega_0^2} \left(\frac{1 + 1/K^2}{(1 - a^2)^2 + (2da)^2} \right)^{1/2}$$

$K = \text{SEC } \phi_m - \text{TAN } \phi_m$

$T_{24} = 1/\omega_0 K$

$$\frac{\omega_c}{\omega_0} = \frac{1}{a} = \frac{1}{\left(\frac{d^2}{K^2} + 1 \right)^{1/2} - \frac{d}{K}}$$

ω_0 = UNITY GAIN FREQUENCY
ϕ_m = PHASE MARGIN
$a = \omega_0/\omega_c$
ω_c = NATURAL FREQ OF TWO POLE FIL
d = DAMPING FACTOR OF TWO POLE
$T_{n,m}$ = Nth TIME CONSTANT OF AN Mth ORDER LOOP

The impedances (Zsc and Zoc) of the distributed circuits in Figures 1 and 2 are shown plotted versus freuency in Figures 3 and 4 respectively:

Figure 3.

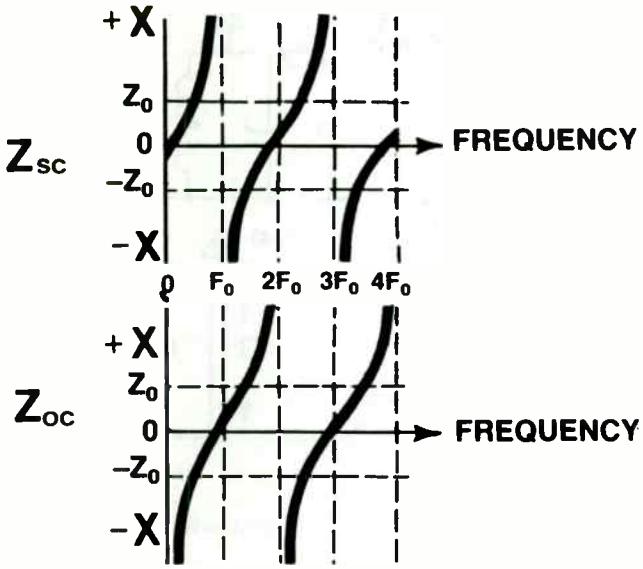


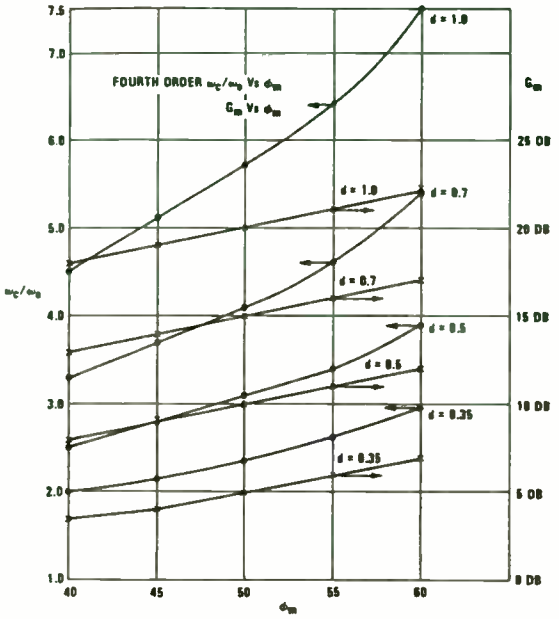
Figure 4.

The multiple parallel and series resonances are unique to distributed elements compared to their lumped element counterparts which have only one resonant frequency.

It should be apparent by now what is meant by the reentrant or periodic nature of distributed resonant elements from Figures 3 and 4 and how they can be used as repetitive band-reject filters to suppress harmonics in an oscillator application. However what might not be obvious is how to achieve parallel resonance at the fundamental oscillator frequency (F1) and series resonance at the even and odd harmonics of that frequency. The distributed circuit shown in Figure 5 is the key structure and the initial step in designing such a filter.

There is a unique characteristic about a shorted quarter-wave resonator. No matter where it is tapped along its length, it will always be parallel resonant.

FIGURE 11.



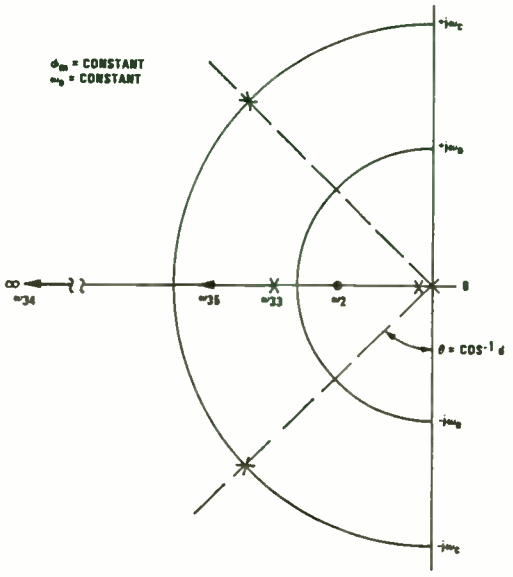


FIGURE 12. OPEN LOOP POLE LOCATIONS FOR THE 4th ORDER LOOP RESULTING FROM $T_{35} = 0$

without instability. Such loops do not occur in real systems due to the spurious poles discussed above. Loops of order greater than three have a finite gain margin. It is readily determined from the BODE plot for a given loop. The compensation technique does not control gain margin nor does it insure stable operation of all fourth and fifth order loops. As the high frequency poles move lower in frequency the 180 degree phase response moves downward and gain margin falls. Underdamped poles (d<1) aggravate this situation by increasing gain with frequency. This effect, shown in Figure 11, produces fourth order loops using d less than .3 with small or negative gain margin (oscillators). Fifth order loops with the pole arrays of Figure 9 have good to excellent gain margins.

MORE POLES

This compensation technique produces excellent results for small loop modifications which occur for high frequency spurious poles. As the complexity of the filter increases or it moves lower in frequency the resulting phase slope will move the phase minimum away from unity gain producing non-optimum loops. Decreasing gain margins will also produce unacceptable loops even when phase margin remains high. To date the process has not been applied beyond the five pole loops discussed here. In the above technique the optimum

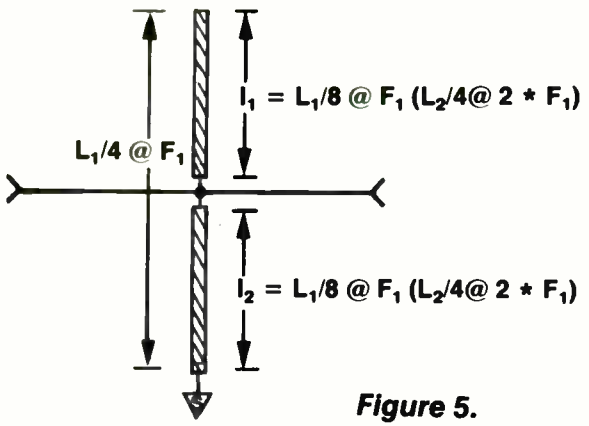


Figure 5.

The reason for this is that shorted transmission lines less than (L/4) (i.e. l2) will always be inductive and open transmission lines less than (L/4) (i.e. l1) will always be capacitive. If (l1 +l2) = (L1)/4 then the two resultant reactances (or susceptances) will be equal in magnitude and opposite in sign on the imaginary impedance axis. Thus the shunt configured circuit in Figure 5 is parallel resonant at the frequency F1. This can be readily proved by substituting l = (L1)/8 and L = L1 into Eq.2 and Eq.3 which yields:

Zsc = jZo and Zoc = -jZo

Since it makes little difference where a shorted quarter-wave transmission line is tapped to achieve a parallel resonance, the next question might be why was the circuit in Figure 5 configured such that l1 = l2 = (L1)/8? The answer to that is simple. Series resonance (band-reject) will occur: when l1 = L/4 at 2*F1, (3/4)*L at 6*F1, (5/4)*L at 8*F1,..... and when l2 = L/2 at 4*F1, L at 8*F1,..... Thus, the circuit in Figure 5 exhibits the composite impedance of that shown in Figures 3 and 4: where Fo = 2*F1.

The filter structure in Figure 5 is, however, only good for filtering "even" harmonics of the desired or band-pass frequency F1. All the "odd" harmonics (3*F1, 5*F1, 7*F1....) cannot be suppressed as easily as ALL the "even" harmonics are with a SINGLE tapped (L1)/4 distributed structure shown in Figure 5. This is due to the fact that F1 is, in a broad sense, an "odd" harmonic (1*F) and conflicts with the requirement that F1 be band-passed while the remaining "odd" harmonics (F3, F5, F7.....) be band-rejected. Thus to achieve this design constraint each "odd" harmonic requires one unique shunt (L1)/4 distributed structure tapped progressively closer to the open end of the transmission line the higher the "odd" harmonic frequency.

loop condition was taken as equal frequency for unity gain and minimum phase. If this is not optimum for a given condition the design process can begin with any reasonable value for ω_2 rather than that of the "optimum" third order loop. One choice might be the 1/f phase noise break point for a particular VCO. Lowering ω_2 will allow more complex filtering at the expense of "optimum" phase conditions.

DESIGN EXAMPLES

The utility of this technique can be tested by application to to some typical loop designs. Figure 6 is the BODE plot of an optimum third order loop with phase margin of 50°. This loop has a unity gain frequency of 10 KHz and a reference frequency of 250 KHz. Reference suppression is 47 dB. (Reference suppression is taken as gain at ω_r and does not account for N.) Figure 13 shows the effect of two spurious op amp poles at 100 KHz. Phase margin is 38 degrees rather than 50. Unity gain frequency is 9.9 KHz and gain margin is 13 dB. Figure 14 is the same loop designed as fifth order with the compensation equations, providing the desired phase margin and unity gain frequency by modification of T_1 and T_3. Its gain margin is 17 dB and reference suppression 57 dB.

FIGURE 13. 3rd ORDER LOOP WITH 2 SPURIOUS POLES

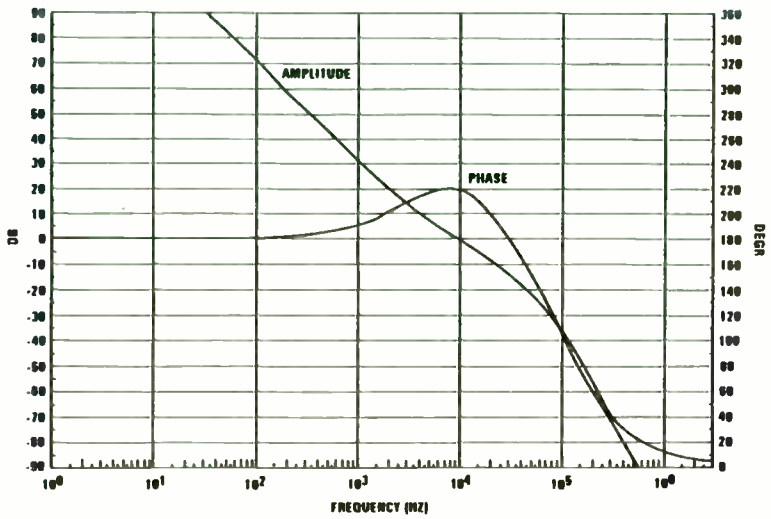


FIGURE 14. 3rd ORDER LOOP COMPENSATED FOR TWO SPURIOUS POLES

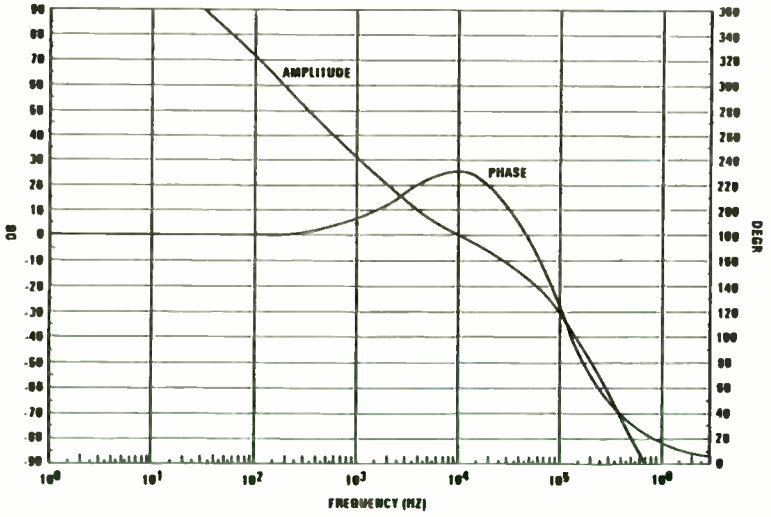


Figure 6 shows these structures graphically depicted to the 7th harmonic:

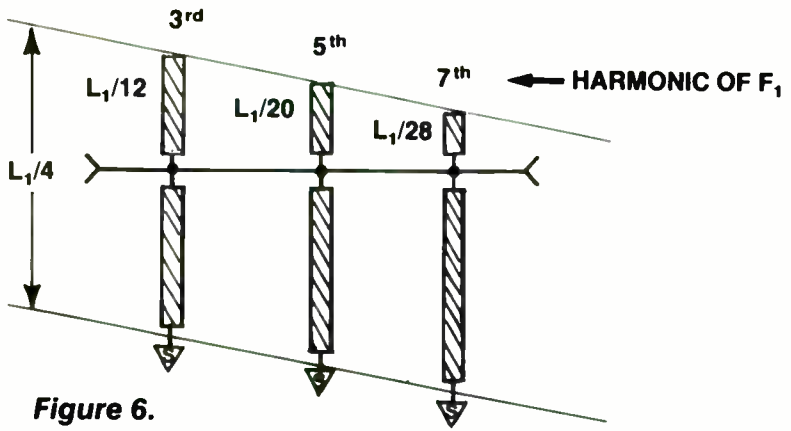


Figure 6.

The length of each of the "open" sections of the distributed structures must be L/4 (series resonance, Zoc = 0) at the desired "odd" harmonic frequencies. This open-stub length (Loc) translates to the fundamental wavelength (L1) using the following equation:

$$Loc = (L1)/(4*N) \qquad \text{(Eq.6)}$$

where: N = the "odd harmonic number (i.e. 3,5,7.....)

Combining the structure in Figure 5 with any or all of the tapped (L1)/4 structures in Figure 6 constitutes a filter that can be tailored to a prescribed harmonic suppression. The author used this technique to reduce the distortion in a 500 MHz SAW resonator oscillator. Only two (L1)/4 structures were required; the "even" one in Figure 5 and the 3rd harmonic "odd" one in Figure 6. A photograph of the transmission characteristics of this filter is shown in Figure 7.

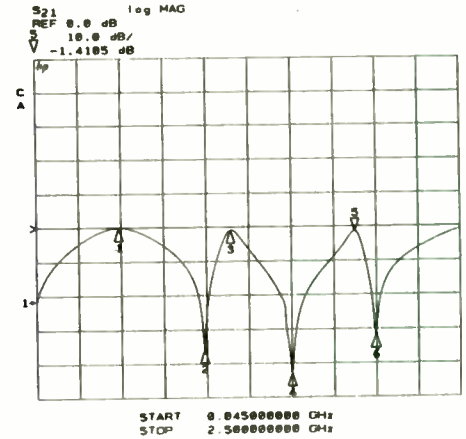


FIGURE 7.

Note the parallel resonance at the 500 MHz fundamental and the series resonance at the 2nd (1000 MHz), 3rd (1500 MHz), and 4th (2000 MHz) harmonics. Figure 8a shows the oscillator without the filter, and Figure 8b shows the oscillator with the filter. Thus, with a few shunt distributed elements, an effective yet

Figure 15 shows the same third order loop with a two pole filter at 75 KHz added to reduce reference sidebands. Note again that the phase margin and unity gain points are as desired, and the gain margin of 16 dB for this loop. Reference suppression is 65 dB.

Figure 16 shows the fourth order loop produced when ω_3 goes to infinity. Again the phase margin and unity gain are as required, the gain margin is 9 dB and the reference suppression 50 dB.

CONCLUSIONS:

A design technique for fourth and fifth order phase-locked loops has been described which accounts for common loop filter elements not found in earlier models. While not strictly optimum in the mathematical sense, the technique yields very useful results and is valuable as a design tool for the equipment design engineer. The technique is readily applied as a computer program which produces circuit component values from performance requirement inputs.[3]

FIGURE 15. 3rd ORDER WITH 75 KHz 2 POLE ADDED

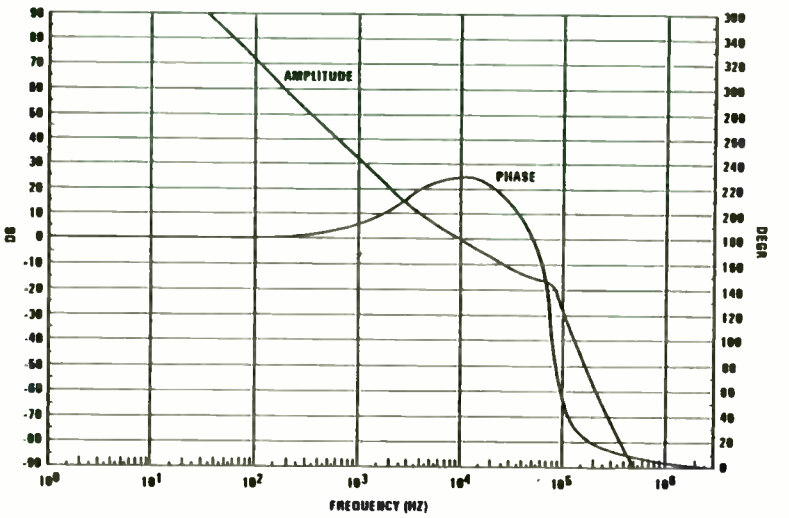
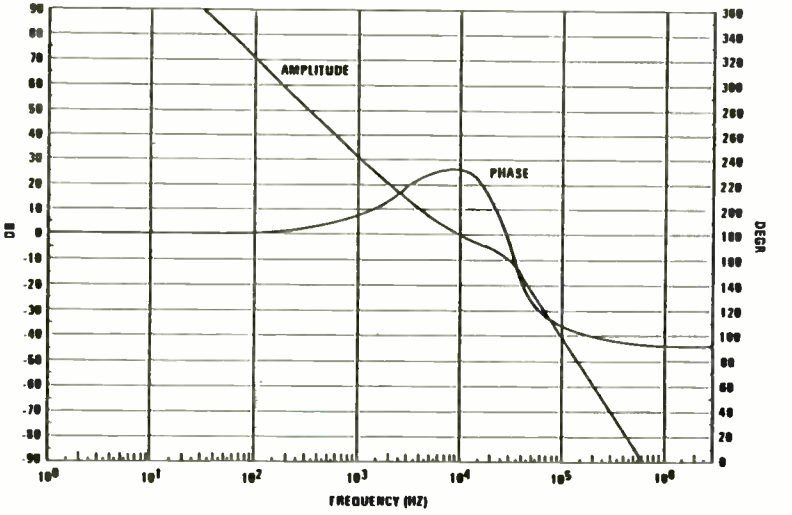


FIGURE 16. 4th ORDER LOOP WITH 31 KHz 2 POLE



simple filter can be designed without complex synthesis and fabricated without tedious "tweaking" in manufacturing.

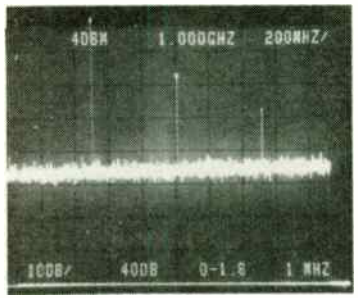


FIGURE 8a

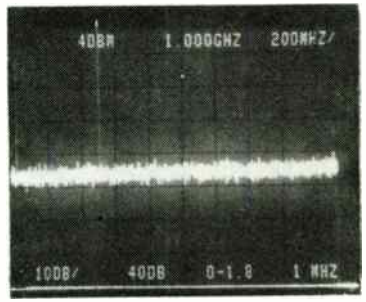


FIGURE 8b

From the filter response shown in Figure 7, it should be apparent that the harmonic attenuation (suppression) is finite (i.e. >30 dB), not infinite as predicted by Eq.2 or 3, where Zin = 0. Equations 2 and 3 are derived from Eq. 1 which assumed no loss (dissipationless line). Distributed quarter-wave (L/4) resonant lines have loss that can be calculated if the equivalent unloaded Q value is known.

The equation for the equivalent (lumped L/C) unloaded Q for an "open" L/4 resonant line can be derived by equating its derivative of impedance (with respect to angular frequency (2*Pi*F)) with the derivative of impedance of a lumped L/C series resonant circuit. The resultant of that mathematical computation divided by Rs (series resistance) yields:

$$Qu = (Pi/4)*(Zo/Rs) \qquad \text{(Eq.7)}$$

Eq.7 can be used to calculate Rs at any harmonic frequency (Fn) if Qu is known at Fn. The harmonic attenuation (An) at any Fn can be predicted by judicious use of the following equation:

$$An = Rs'/(Rs'+(Ro/2)) \qquad \text{(Eq.8)}$$

Where: Rs' = the equivalent series resistance of all the L/4 and multiple L/4 lines with series resistance at Fn.

Ro = Source and load resistance assumed equal (i.e. 50 ohms)

Applying a similar procedure as used to obtain Eq.8 an equation for insertion loss can be created as follows.

The equation for the equivalent (lumped L/C) unloaded Q for a "shorted" L/4 resonant line can be derived by equating its

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ACKNOWLEDGMENTS

The author thanks Mr. Steve Zamoscianyk for creating the program FAZLOK, which applies the compensation technique, and Mr. Paul Peloquin for extensive use of the program in generating data for this article.

derivative of susceptance (with respect to angular frequency) with the derivative of susceptance of a lumped L/C parallel resonant circuit. The resultant of that mathematical computation divided by G (parallel conductance) yields:

$$Qu = (Pi/4)*(Rp/Zo) \qquad \text{(Eq.9)}$$

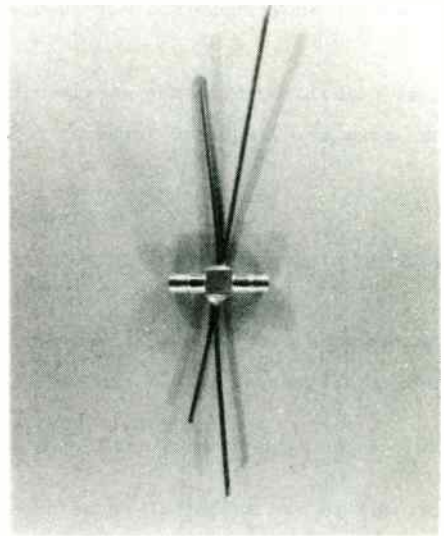
Where: Rp = 1/G = parallel resistance.

Eq.9 can be used to calculate Rp at the fundamental frequency (Fl) if Qu is known. The insertion loss (I.L.) can be predicted using the following equation:

$$I.L. = (Rp/m)/((Rp/m) + (Ro/2) \qquad \text{(Eq.10)}$$

Where: m = number of shunt (Ll)/4 resonators in the filter. (i.e. m=2 for the filter in Figure 7.)

The filter in Figure 7 was configured with .047 inch diameter semirigid coaxial cable with a dielectric constant Er = 2. Different transmission line media, whether coax, stripline, microstrip, etc. will have different Qu's. By configuring some (Ln)/4 "open" resonant lines in the desired transmission line media and making harmonic attenuation (An) measurements at each harmonic frequency (Fn), the unloaded Q's (Qu) can be calculated using Equations 7 and 8. Rs' reduces to Rs in a single (Ln)/4 resonant line. n = desired harmonic number (i.e. 1,2,3,4....).



RF-TECHNOLOGY FOR NMR IMAGING/SPECTROSCOPY

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INTRODUCTION:

Radio-Frequency (RF) technology has made an important contribution to the implementation of an exciting new medical diagnostics tool during the past couple of years: The NUCLEAR MAGNETIC RESONANCE IMAGING machine, which is able to look noninvasively inside the human body. This new technique alters the perspective of the radiologist and allows him to diagnose diseases with greater sensitivity. One of the main advantages of NMR images is their excellent soft tissue discrimination. NMR spectroscopy is now being evaluated for possible application to the non-invasive study of body chemistry. Many hospitals are in the process of installing such NMR imaging machines.

This paper reviews the NMR-system with emphasis not on the physics of the nuclear magnetic resonance effect but on the RF technology required to make it operate. Some special RF problems occurring in NMR will be discussed, especially the RF signal and kilowatt power processing.

PRINCIPLES OF NMR IMAGING:

The nuclei of certain atoms such as hydrogen and phosphorus possess both a magnetic moment and a spin angular momentum. When these nuclei are subjected to an external direct magnetic field, they align themselves in the direction of that field like compass needles. In addition, these nuclear micro-magnets are rotating or "spinning" like gyroscopes or tops with the so-called Larmor-frequency which is proportional to the magnetic field strength Bo. The proportionality factor is a physical constant, the gyromagnetic ratio, which differs greatly for various atoms. For hydrogen that ratio is 42.58 MHz/Tesla, and for phosphorus 17.23 MHz/Tesla. A magnet with a field strength of 15,000 Gauss or 1.5 Tesla operates therefore at a frequency of 63.87 MHz for hydrogen imaging. At the same field phosphorus nuclei can be detected at a frequency of 25.845 MHz. The relative sensitivity is fortunately very high for the diagnostically relevant hydrogen nucleus which is also available abundantly in the human body, mainly as part of the water and lipids (fat) in body tissue.

Magnetic resonance absorption occurs when radio frequency energy is applied at the Larmor frequency. The magnetic vector B1 of this RF field must be perpendicular to Bo, the static magnetic field, which aligns the spins and produces a macroscopic magnetic moment. B1 flips this magnetic moment vector by a certain angle depending on the magnitude and duration of the applied RF pulse. When the RF field is discontinued the transverse magnetization precesses around the axis of the external main Bo field. Hereby a RF signal is induced in the receiver coil located in the transverse plane. Spatial discrimination for the imaging process is obtained if one applies an additional, linearily varying magnetic field in the x, y and/or z-direction of a coordinate system

OEVELOPMENT OF A C BAND POWER MOOULE FOR THE MORELOS MEXICAN SATELLITE SYSTEM

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ABSTRACT

This article describes the procedures of design and characterization of power modules of 1 Watt, 3 Watt and 5 Watt intended to be used as transmission elements in RF sections of earth stations linked through the Morelos Mexican Satellite System. This article also describes the particular use of the three indicating the number of available channels for each application taking into account the essential parameters of the satellite link. These modules were developed under contract with the National Council of Science and Technology Potentially to be used in rural and private network applications in Mexico.

I. INTROOUCTION

This document deals with the effort made toward the development of high power amplifiers, based in the use of GaAsFET devices and intended to be proposed for use with the Mexican Satellite System.

We start this program by first making several low and medium power prototypes, to generate an efficient methodology for design and characterization of HPA's modules. Our main interest is to develop the technological aspects involved in the design and fabrication of this type of subsystems, based on our previous experience in the low-noise design.

II. DESIGN PHYLOSOPHY

Initially, we must select a circuit topology that allows us to satisfy the operation requirements, taken into account the final application of the amplifier. For this case, we have taken a modular approach in order to evaluate adequately each separated stage and to make any possible correction without interfering with other stages.

We have chosen to design several independents modules prior to the main HPA prototype, namely, we design: 1W, 3W and 5W modules, in order to get a better way of selecting the final circuit configuration, based on device availability and technological internal support.

inside the magnet generating the main Bo field. These fields are produced by so-called gradient coils.(1,2).

THE NMR IMAGING SYSTEM:

A block diagram of a typical NMR imaging system is shown in Figure 1. At the left the computer related instruments are seen which carry out the image processing. Between the magnet at the right-hand side and the computer the necessary electronic components are indicated: spectrometer consisting of a transmitter and receiver, a multi-kilowatt RF power amplifier, noise suppression diodes, a transmitter/receiver switch, a kW matching network, low noise preamplifier, RF amplifier etc.

THE MAGNET:

The magnet has to be located inside a shielded room so that nearby radio stations do not interfere with the small NMR RF signals. The concept of superconductivity is commercially exploited on a large scale for the first time by most of these NMR magnets. Liquid helium at a temperature of about 4 degree Kelvin (-269 degree centigrade), imbedded in a tank of liquid nitrogen, cools the magnet coil wires so that they become superconductive. Their electrical resistance is zero and a DC current induced by a power supply once will continue to flow after the supply is disconnected generating a strong magnetic static field in the order of magnitude of 0.3 to 2.0 Tesla (3000-20000 Gauss). An important requirement for a whole-body magnet is that the magnetic field is highly homogeneous over a large volume to be imaged. Any inhomogeneity translates into a picture distortion. Therefore, all magnets have shimming coils in order to homogenize the field.They are fed by the shimming power supply. The trend to higher magnetic fields is dictated by the physics of the NMR experiment which says that the signal-to-noise ratio increases with increasing field strength.

An array of x,y and z gradient coils are mounted on a cylinder inside the magnet bore in which a whole-body or a head RF coil is also located. The gradient coil carrying cylinder is covered on its inside by a copper foil shield in order to generate a well-defined electrical environment for the RF coils and for the elimination of any interference between these coils. Resistive and permanent magnets are also used for NMR imaging, but only for lower field strength (0.15-0.3 Tesla). The former require 20 to 40 kilowatts of power and therefore costly cooling systems. (3).

GRADIENT POWER AMPLIFIERS:

In order to generate the gradient fields necessary for obtaining spatial resolution of the NMR signals DC pulse currents of 10-30 A must be injected into the gradient coils. They are delivered by the gradient PAs which are 1-2 kilowatt linear audio amplifiers with a frequency range of DC to 50 kHz. The magnetic forces on the gradient coil wires produce loud acoustic noise. Therefore, provisions for acoustic damping must be implemented. The philosophy behind the pulse trains used in different NMR experiments is a science for itself. After this short discussion of the apparatus generating the magnetic field environment necessary for NMR the RF signal path will be followed.

We focused in the 3W module, because in its design and implementation, there are involved both small signal and large signal methods, that could be used in the final design. The following section will be devoted entirely to show the general design methodology, and then we will present some results and possible applications.

III. DETAILS OF 3 WATT AMPLIFIER MODULE

This module is intended to provide 3 Watts of output power at the 1dB gain compression point. In the design of this module, the main objective is to obtain a good trade-off between linearity, dc power consumption and distorsion level.

One of the goals in this design project is to get a strong correlation between computed and measured circuit performance, detecting the possible source of error in its final implementation.

The circuit configuration for this high-gain, high-power amplifier is shown in figure 1 along with the type of GaAsFET devices that will be used in its implementation. This configuration includes one balanced stage in order to increase the power handling capability of the single medium power GaAsFET.

We can see three basic building blocks in this figure, namely, the low-power two-stage block that uses cascade connection of one NE72089 with one NE69489, then there is a medium power block formed with one NE900175 cascade connected with one NE800299, and finally there is a single stage high power block that uses one internally matched GaAsFET device that provides 3.5 Watts at 6.4 GHz.

Also of importance are the 3 dB hybrid couplers that should be used in the balanced block and that will be implemented by using branch line quadrature hybrids on the same substrate used for the amplifier stage.

The basic block for the two-stage designs is shown in figure 2 and it will be used as reference in the description of the design steps that follows.

a) Design of the two-stage low-power block.

In the structure for this block is necessary to calculate the appropriate matching networks MN1, MN2 and MN3 in order to present the reflection coefficients required at the transistor input and output ports, to get maximum gain at this stage.

Due to the signal level at this point the small signal 'S' parameters of the GaAsFET can be used in the design. As a first approach, the manufacturer data sheet are used and the individual FETs are first analyzed to check for stability and available gain in the 5.9-6.4 GHz band. The result of such analysis is shown in tables 1 and 2.

The requeriments imposed to the matching networks are as follows, making reference to the results on tables 1 and 2, and regarding the values of the reflection coefficients for maximum

THE TRANSMITTER:

The pulse sequences necessary for the NMR experiment contain sinx/x or sinc-pulses which are used in order to excite a well-defined slice of the object to be imaged in such a way that the NMR signal is constant across that slice. These sinc-pulses require that the NMR transmitter as well as the RF power amplifier are linear. A block diagram of a NMR transmitter is given in Figure 2. It includes envelope feedback for linearity improvement. The NMR experiment requires the ability to change the phase of the carrier frequency in 90 degree steps which is accomplished by the multiplexer circuit shown.

A disadvantage of NMR imaging is the relatively long time required to take an image (several minutes) compared to x-ray tomography (seconds). The reason is that the nuclear spins in the samples have a relatively long relaxation time of several hundred milliseconds after excitation. One way to speed up the process is to image additional slices while waiting for the first ones to relax toward equilibrium. By applying a finite bandwidth RF pulse in the presence of a magnetic field gradient, a slice in a plane perpendicular to the gradient is excited. The modulating waveform required to produce an offset slice at a location F1 (frequency) of bandwidth Fo is a single-sideband signal which can be generated by the so-called Weaver method of SSB generation using a quadrature I-Q channel circuit arrangement. The modulating signals, generated by n-bit data words and converted to analog signals via DACs, are sine/cosine functions of the offset frequency F1 modulated by the sinc-function of the bandwidth Fo. They are applied at the corresponding PS-I and PS-Q ports of the SSB transmitter shown in the block diagram of the spectrometer in Figure 3.

THE RF POWER AMPLIFIER:

Most NMR imaging systems, especially at higher fields (1.5 Tesla), use tube power amplifiers because power levels of 5 to 15 kW are required for the excitation of the protons during whole-body imaging of heavy patients. These amplifiers are expensive, have a narrow bandwidth and require a change of the tubes after relatively short time intervals (1-2 years). Therefore, efforts are under way to replace them with solid-state amplifiers, a challenging task.

Typical pulse widths and duty cycles of NMR pulse sequences are in the range of 1-5 msec and 1-5 % respectively. Therefore, the average power levels stay relatively low. Transistor pulse amplifier design makes good use of the amazing ability of semiconductor devices to handle large power levels for short time intervals. For example a small PIN-diode in a glass package such as the Unitrode device UM-7201B has a power dissipation rating of 1.5 Watt in free air, but can handle a 20 kW pulse for 1 microsecond! Fortunately, a new technology has also arrived: The RF power MOSFET. Only this device was used because of its larger safe operating area and its higher input impedance compared to bipolar transistors.

Figure 4 shows the circuit diagram for a push-pull MOSFET power amplifier output stage for a 0.15 Tesla resistive magnet NMR system operating at 6.4 MHz. Transmission line BALUNs and 4:1 transformers have been used at input and output. With two low-cost MTM-15N45 MOSFETs (450 Volt, 15 A, 60 A peak) RF pulse power levels of 5-6 kW have been obtained in the 6 MHz frequency range with a power gain of 18 dB at 200 Vdc. In Figure 5 the output power as a function of the battery voltage is shown. These transistors (in a TO-3 can) produced still

gain at 6.2 GHz:

1) MN1 must match the 50 Ohms source impedance, to the impedance corresponding to $\Gamma g = (\Gamma in,1)^* = \Gamma ms,1 = 0.73/\underline{150}^\circ$ (8.3 + j13 Ohms),

2) MN2 must match $\Gamma in,2 = (\Gamma out,1)^* = \Gamma ml,1 = 0.601/\underline{148}$ (13.4 + j13.2 Ohms), to $\Gamma out,2 = (\Gamma in,3)^* = \Gamma ms,2 = 0.803/\underline{134.7}$ (6.2 + j20.6 Ohms),

3) MN3 must transform the impedance corresponding to $\Gamma 1 = (\Gamma out,3)^* = \Gamma ml,2 = 0.887/\underline{70.8}$ (8.9 + j69.6 Ohms), to the 50 Ohms load impedance.

Based on previous results, the circuit topology selected for MN1, MN2 and MN3 is formed by the cascade connection of short lenght transmission lines, whose electrical characteristics as well as the number of elements in the network are determined with the following equations (1):

$$Zc^2 = \frac{R1/Z2/^2 - R2/Z1/^2}{R2 - R1} \qquad (1)$$

$$\theta c = \tan^{-1} \frac{Zc\,(R2 - R1)}{R2\,X1 + R1\,X2} \qquad (2)$$

where $Z1 = R1 + j\,X1$, $Z2 = R2 + j\,X2$, and θc, are shown schematically in figure 3. Obviously, if Zc^2 is negative the impedance transformation is not possible with only one matching element, so more elements must be added. This can be acomplished by first transforming to an intermediate impedance (arbitrary) and then using the given equations and repeat this process until the right transformation is found. When this transformation is possible, then:.

$$Ze = Zc\,\frac{Z1 + j\,Zc\tanh(\gamma\ell)}{Zc + j\,Z1\tanh(\gamma\ell)} \qquad (3)$$

where, ℓ is the physical line lenght, $\gamma = \alpha + j\,\beta$ is the propagation constant with α being the attenuation constant andβ the phase constant.

Following this method, the two-stage low power design is shown in table 3 along with the microstrip dimensions for low Er substrate. The physical implementation is shown in figure 4 and its measured response appears in figure 5. This response is in agreement with the NE69489 data sheet that shows an output power of 19 dBm at the 1dB compression point. From this figure we can see that the measured gain is around 3 dB below the calculated one and by making some tuning after construction it was possible to add 2 dB more gain with flat response. The type of tuning elements required to get this improvement suggests that in the fabrication process some errors could arise causing this discrepancy in the performance. This will be discussed later.

b) Design of the two-stage medium power block.

In this block, we use small signal 'S' parameters to calculate the matching networks for linear output power in the first stage, and the load and source impedances for maximum output power are used in the second stage.

For the NE900175 the manufacturer's data are shown in table 4

2 kW at 13 MHz, the frequency of a 0.3 Tesla NMR system, and 1 kW at 22 MHz (0.5 T). The conclusion is that even MOSFETs designed for low-frequency applications such as switching type power supplies etc. are able to produce a lot of RF pulse power up to frequencies in the 20 MHz range.

The feasibility of kilowatt RF pulse generation for high field applications (20-85 MHz) was also explored. Figure 6 shows the circuit diagram of a 1.5-2 kW RF pulse power amplifier module using four MRF-150 MOSFETs. Combining four such modules with 4-way splitting and summing hybrids such as the one given in Figure 7 a 5-6 kW PA is obtained: PA-4. The output versus input power curve of Figure 8 demonstrates reasonably good linearity up to 4-5 kW at a frequency of 62 MHz. Figure 9 demonstrates a great advantage of transistor amplifiers compared to tube circuits; a much larger instantaneous bandwidth without retuning can be obtained. The 5-kW bandwidth extended from 40 to 70 MHz in this case. An interesting feature of the 4-way combiner hybrid of Figure 7 is the fact that the two input ports are operating in the push-pull mode providing all its known advantages. (Patent pending).

The number of components can be reduced drastically with the new Motorola RF power MOSFET MRF-154 which at present is expensive. A unique in-circuit combining technique was used in a 4-transistor amplifier: PA-1. Figure 10 shows the output power versus battery voltage curve demonstrating the generation of 5-6 kilowatt pulses at 62 MHz with only four transistors. This circuit delivered even 1 and 2 kW at voltages as low as 30 and 40 Vdc, a feature no tube circuit can perform. At each voltage the amplifier was driven into saturation. The same basic circuit produced 6-8 kW at lower frequencies (21 MHz, 12 MHz) with only minor changes in the input matching network and the drain-drain capacity. (Figure 11).

DIODE CIRCUITS:

High-gain wideband power amplifiers generate noise which disturbs the NMR experiment during the receiving time. In order to solve this problem the PAs are normally gated off after the end of the transmit pulse. In addition so-called noise suppression diodes can be inserted in the power cable connecting the PA to the NMR-coil. Diodes in both directions are put in parallel and series as shown in Figure 12. Their lead inductance has to be compensated by small capacitors parallel to input and output in order to avoid a power reflecting mismatch. As long as the noise voltages are less than the combined threshold voltages of these diodes the PA noise is suppressed.

If the NMR experiment is carried out in a single-coil system a transmitter/receiver T/R-switch is required. Such a circuit can be obtained by adding a parallel output connector to the arrangement of Figure 12. In order to handle the high power pulses one uses low on-resistance PIN diodes in combination with high-speed signal diodes. The third port of the T/R-switch is connected with a lambda/4 50-Ohm cable to the diode protection circuit necessary at the input of the low-noise preamplifier. This network simulates the cascade of two lambda/4 transmission lines with two CLC sections. (Figure 13). The input diodes are turned on at the beginning of a high-power RF pulse and their low impedance is then transformed into a very high impedance at the T/R-switch by the quarter wavelength transmission line. The same happens with the CLC sections.

along with its corresponding stability and gain analysis. To evaluate the NE800299 stability and liner gain capabilities, the 'S' parameters were also used giving the results shown in table 5, while for this same transistor (NE800299) load-pull measurements were made in order to obtain input and output reflection coefficients at the 1 dB gain compression point. This information is shown in table 6.

With a similar approach to that of the low-power case, the matching networks in this design were determined by using the data shown in tables 4 and 5, with the following conditions at the 6.2 GHz point:

1) MN1 is designed to match the 50 Ohms source, to the impedance corresponding to $\Gamma g = (\Gamma in,1)^* = \Gamma ms,1 = 0.917/\underline{160°}$ (22 + j8.8 Ohms),

2) MN2 has to match the reflection coefficient $\Gamma in,2 = (\Gamma out,1)^* = 0.730/\underline{104°}$ (12.4 + j37.4 Ohms) to the measured input reflection coefficient $\Gamma meas,1 = 0.731/\underline{-11.2°}$,

3) MN3 is designed in order to transform from the measured load impedance corresponding to $\Gamma meas,2 = 0.507/\underline{110°}$ to the 50 Ohms load impedance.

For the cascade connection, the circuit topology and element values, its computed response using an internal small signal circuit analysis program, and their physical dimensions on microstrip transmission lines with high Er substrate appear in table 7.

Two units with similar characteristics are needed to conform the balanced stage, so, 'A' and 'B' medium power modules were constructed and tested individually giving the results shown in figure 6. Discussion of these results will be made in a following section.

c)Design of the high-power block.

As mentioned above, in this block we use an internally matched device that requires only, 50 Ohms lines at the input and output ports, to provide 3.5 Watts at 6.4 GHz. With slight tuning adjustment, it can be possible to get an adequate performance across the frequency band. This module is shown in figure 7 and its performance appears in figure 8.

Discussion of results.

We have found in the experimental work, that some deviations between the calculated and measured responses of both the low-power and the medium-power blocks have ocurred. In order to analyze in more detail the possible causes of that discrepancies, in what follows, we take as an example the medium-power design.

The first cause of error, could arise during the characterization of the NE800299 transistor in order to obtain its load and source impedances for maximum output power. We found for one hand, a strong frequency and input power dependence on transistor impedances, and for the other hand, we have taken the reflection coefficients of the transistor at the input and output

NMR COILS:

The design of NMR coils is again a science in itself. The main problem to be solved is the generation of a very homogeneous RF magnetic B1-field orthogonal to the main direct Bo-field produced by the powerful superconductive magnet in a volume as large as necessary for whole-body imaging. Another problem occurs if one goes to higher field strengths in order to get better signal-to-noise ratios and therefore to higher frequencies where a more conventional design of a large whole-body coil becomes impossible due to self-resonance effects of the coil. The coils are normally forming a resonance circuit with some capacitors at the Larmor frequency (64 MHz for 1.5 Tesla) so that one obtains a well-defined real load impedance for the RF power amplifier after some impedance transformation. This impedance is usually 50 Ohm.

Since the dimensions of a whole-body or head coil are relatively large their inductance and therefore also their resonance impedance becomes very high too. This results in interference and detrimental coupling effects with the environment, especially the magnet and its many shimming and gradient coils. At high fields the self-resonance frequency of a coil may be even much lower than the NMR operating frequency. A solution to these problems has been found by splitting up the coil-wire in short pieces and connecting them with capacitors in such a way that each capacitor forms a series resonance circuit with its corresponding inductance piece. The conventional way to make an NMR transmit/receive antenna generating the orthogonal B1 field is to put a so-called saddle-coil pair with the associated capacitors on a plastic former which should have a low dissipation factor. A head coil has been made using this concept for carbon C-13 spectroscopy tuned to the Larmor frequency of 15.7 MHz. In order to enhance the very weak carbon signal the hydrogen protons are also excited. For this purpose a second saddle coil tuned to the frequency of 62.45 MHz was placed on the same former but mechanically shifted by 90 degrees so that its B1-field is orthogonal to that of the carbon coil. Figure 14 shows the circuit configuration of this double-coil and its matching networks. But saddle coils are not producing a magnetic field homogenity good enough for good imaging. More elaborate coil designs are described in the literature.(4).

The most important design parameter of a tuned NMR coil is its quality factor Q in the unloaded condition. It should be as high as possible, especially high compared to the loaded Q with a patient's body inside the coil. In other words, the coil losses should be determined by the unavoidable losses induced by the head or body to be imaged and not by those of the inductors and capacitors. The latter decrease drastically the signal-to-noise ratio of the NMR receiver system. Unloaded Q-factors of 300-600 have been obtained at low and high NMR frequencies. The ratio of unloaded to loaded Q is about 1.5 at 6.4 MHz and 4-6 at 64 MHz because induced body losses increase with frequency. The necessary high Q factors can be achieved by the selection of capacitors with very low dissipation factors. Teflon PC-boards have been used to implement successfully such capacitors which also must have a high breakdown voltage because RF pulses of many kilowatts are applied. Low-loss inductors are best implemented by 1/8" copper tubes. The signal-to-noise ratio can be improved drastically by using so-called surface coils for receiving the NMR-signal whereas the head or body coil is employed as transmitter for better B1-field homogenity. These surface coils are adaptively formed for different body parts and are located directly over the organ to be imaged, e.g. the eye, spine, knee etc.

connector of the test fixture, and then we tried to compensate the transmission line lenght, and also the SMA connector to microstrip interface, during the Network Analyzer calibration procedure. That could bring out some errors due to the lack of precision in the setting of the reference planes.

We will use in future works to evaluate the large signal impedances of the transistor, by first optimally match the transistor in the test fixture to get maximum output power,then disassemble the test fixture, and measure the complex conjugate input and output impedances of the transistor, in the precise reference planes, by taking out the tansistor mount and measuring the complete input and output matching network that includes bias tee, tuner and connectors, as shown in figure 9. We are starting a program just to determine how well this could be used with certain degree of confidence.

The second problem we face, consists in the errors involved during the photolitographic process. This is best illustrated in Table 8 and 9, where the actual circuit dimensions are compared against the calculated ones. We found that the sources of great errors are in the high impedance elements (narrower line), so, in the matching impedance procedure, could be better to look for low impedance matching lines, or to improve the technological aspects involved.

IV. RESULTS AND APPLICATIONS

Following the methods described in Section III, we designed and built the 5 Watt prototype shown in figure 10, whose performance at 6.2 GHz appears in figure 11.

The solid state power modules described in this article were originally intended for applications in earth stations transmitters using the Morelos Mexican Satellite System. Link calculations between Ensenada, Baja California and Mexico City were performed to define the especific applications of the 1, 3, and 5 Watt modules. Table (A) shows the results of such calculations using the following Satellite Characteristics:

Satellite Characteristics
Channel 9N, Morelos

$O_S = -8953 \frac{dbw}{m^2}$
Saturation flux density

Satellite location 113.5° W

BO = 6 dB
Output Backoff

$\frac{G}{T} = 3.1$ dB/oK
Satellite figure of Merit

$EIRP_{Sat} = 36.33$ dw
Electric isotropic radiated power of Morelos in Ensenada

Bi = 11 dB
Input Backoff

T A B L E A

PHPA Watts	GTxdB	GRx dB	G/T RES db/oK	Eb/No dB	RBW
1 Watt	50	40	19.31	5.3	30 MHz
3 Watt	50	40	19.31	6.3	30 MHz
5 Watt	50	40	19.31	10	30 MHz

Since the coil impedance is changing for different patients it is sometimes useful to place a matching network between power amplifier and coil. A LCL-circuit with a variable parallel capacitor and two stub-tuned series transmission line inductors was employed. It permits impedance matching over a large range. These RF circuits must be able to handle 1-15 kW pulses at 64 MHz. (Figure 15).

THE PREAMPLIFIER:

The NMR signals induced in the receive coils by the moving magnetic moment vectors are relatively small. Therefore low-noise preamplifiers are required which must be protected from the multi-kilowatt RF pulses by the protection circuits already discussed. Figure 16 shows a cascode circuit with two junction field-effect transistors at the input stage and a feedback damping arrangement for a low-field (0.12 Tesla, 5.1 MHz) NMR research system. The optimum source impedance was about 800 Ohm. This preamplifier was connected directly to the receive coil of a 2-coil T/R arrangement. The input impedance of the antenna was tuned to 800 Ohm. The noise figure as a function of the source resistance is shown in Figure 17 and as a function of the source admittance phase angle in Figure 18. A noise figure of 0.5-0.6 dB was obtained as minimum. The concept of feedback damping which was applied reduces the input impedance of the preamplifier so that the coil bandwidth is increased without increasing the noise considerably. This feature is not required at high fields where the body damping is much more pronounced.

The noise figure measurements have been carried out with the low-cost liquid-nitrogen method which is suprisingly accurate and permits measurements at source resistances different from 50 Ohm. The receiver output noise voltage is measured for the source resistor at room and then at liquid N2 temperature (77 degree K). The noise voltage ratio can be related directly to noise figure in dB with the curve of Figure 20. (Courtesy Dr.H.Hart, GE-CRD). This method has also the advantage that it can easily be applied to a whole system as well as for source resistances differing from 50 Ohm. For high-field systems preamplifiers with bipolar transistors have been designed in order to obtain a larger bandwidth. The design starts with the selection of a low-noise transistor which must have very high current gain, a large gain-bandwidth product and a low base bulk resistance. The optimum source resistance, the most important design parameter, can easily be determined by measuring with a receiver the relative output noise voltage for the conditions of short- and open- circuit at the preamplifier input. The ratio of the two noise voltages (short- over open-circuit voltage) multiplied with the input impedance of the input stage gives the optimum source impedance. In the frequency range of interest that impedance was about 100 Ohm. A noise matching network which degrades the noise figure can be avoided by paralleling two input transistors. This has also the beneficial effect of reducing the base resistance. A preamplifier designed with this procedure has a noise figure over a large frequency range of well below 1.0 dB and reaching 0.5 dB at some frequencies. Figure 19. (6,7).

NMR RECEIVER:

The preamplifier which may have a bandpass filter at its input in order to increase system stability is followed in the signal path by a variable gain

PHAPA = Solid state power amplifier output;
GRx = Receiving antenna Gain
GTx = Transmitter antenna Gain;
G/TREC = Figure of Merit of receiving antena
Eb/No = Energy bit per noise
RBW = Reference Bandwidth

It can be seen from Table (A) that the 5 Watt power module would provide the best characteristics of a thin route Satellite Communications link. The improvement of the Eb/No for the 1 Watt or 3 Watt module would imply the use of bigger antenna and the reduction of the reference bandwith and hence the transmission rate.

Another possible application of the 5 Watt amplifier would be in tererestrial microwave line-of-sight links as TWTA's replacement.

V. CONCLUSIONS

We have described the methodology for obtaining low-power and medium-power modules, and we have combined them in order to get a 5 Watt module whose possible applications are in satellite communications and also in terrestrial links. We will continue in the technological development of these microwave subsystems, and in this way present additional alternatives for the Mexican Telecommunications System.

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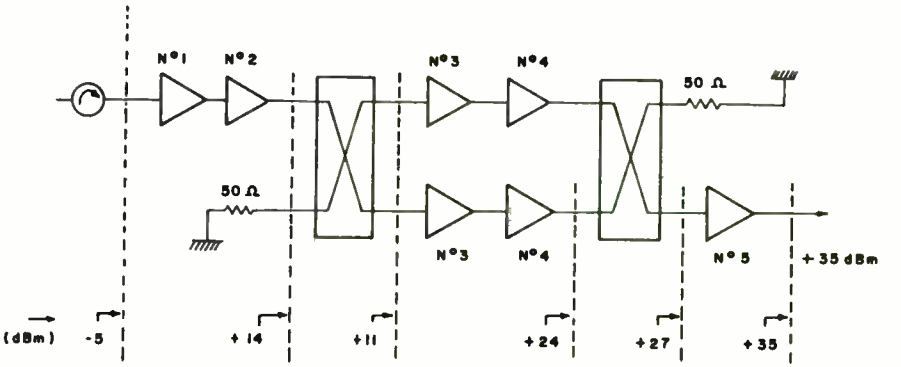

Figure 1. Circuit Configuration

RF amplifier made with a Plessey IC SL-1550. It has a gain range of 10 to 36 dB. A block diagram of the receiver itself is shown in Figure 21. It uses the ZERO-IF I-Q channel quadrature detection concept due to the fact that the complex analog NMR signals have to be converted to the digital format by two A/D converters in order to permit image reconstruction by a computer. High frequency A/D converters are not available, certainly not at a low cost.

The RF-amplifier signal is split and fed to two quadrature mixers. Their low-frequency output signal are band-limited after amplification by two low-pass filters which have a variable bandwidth. (8,16,32 kHz). The main design challenge is the front-end mixer pair which must provide a large dynamic range as well as good linearity. The maximum overall gain of the receiver is about 70 dB.

QUADRATURE EXCITATION AND RECEPTION:

Normally the B1 RF-field in the transmit head or body coil is linearily polarized. Due to the fact that the human body is electrically conducting eddy currents are generated inside the body parts which increase with frequencies. These unwanted eddy currents cause image artifacts and distortions. Their detrimental influence can be eliminated or drastically reduced by producing a rotating RF B1-field. This is done by feeding a specially designed circular RF coil on two points wich are geometrically 90 degrees apart by two equal, but 90 degrees phase-shifted signals.(5). A linearly polarized field can be generated by the superposition of two rotating fields. One of these is now interacting with the magnetic moments and spins of the protons according to the physics of the NMR experiment. Therefore, only half the RF power is required using a rotating field compared to the case of a linear one. Figure 22 shows an RF block diagram of such a system with two power amplifiers. If only one big tube PA is available one can use a quadrature power splitter made with two lambda/8 50 Ohm transmission lines and two crosscoupling capacitors which must have a reactance of 50 Ohm at the operating frequency. The quadrature coil arrangement can also be used to increase the signal- to-noise ratio by a factor of 1.4 during the receive mode of operation. (5).

RESULTS:

The results obtained by such a NMR system with its many RF circuits are images of the inside of the human body in all possible cross-sections with a discrimination not available with other means.

ACKNOWLEDGEMENT:

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#	TYPE	P_{1dB}	G_{LIN}	V_{DS}	I_{DS}
1	NE72089	+12 dBm	10 dB	3.5V	30mA
2	NE69489	+18 "	10 "	7.0V	45 "
3	NE900175	+23 "	8 "	9.0V	90 "
4	NE800299	+27 "	6 "	9.0V	300 "
5	NEZ-5964-3A	+35 "	8 "	9.0V	1200 "

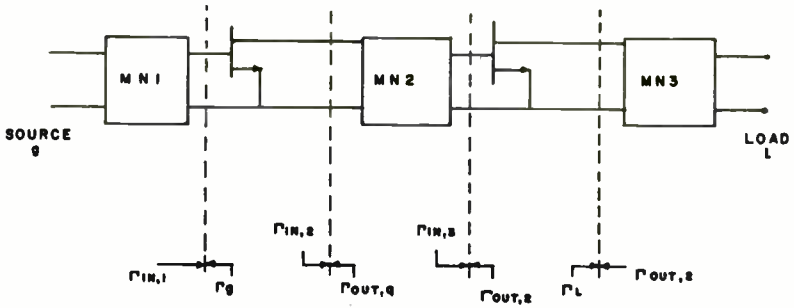

Figure 2. Basic Two-Stage Amplifier

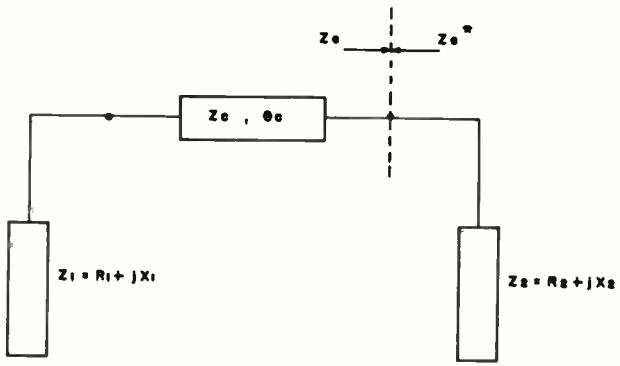

Figure 3. Impedance Transformation with Short length Transmission Line

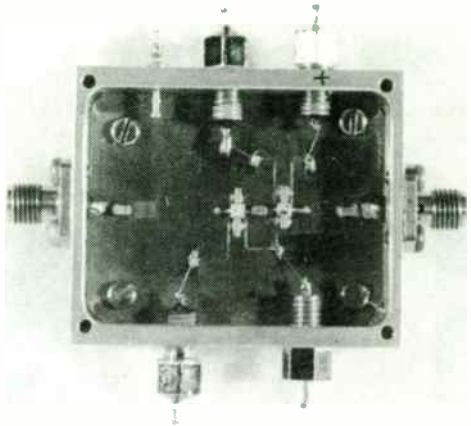

Figure 4. Photograph of Two-Stage Amplifier

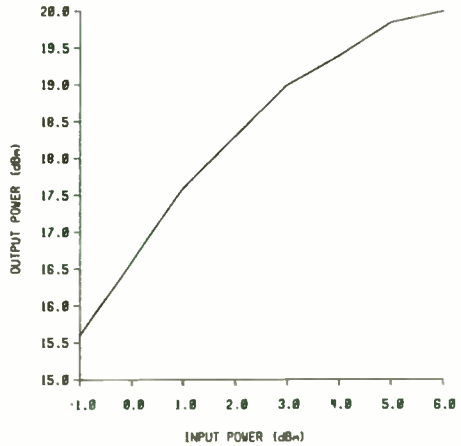

Figure 5. Measured Response of Two-Stage Amplifier at 6.2 GHz

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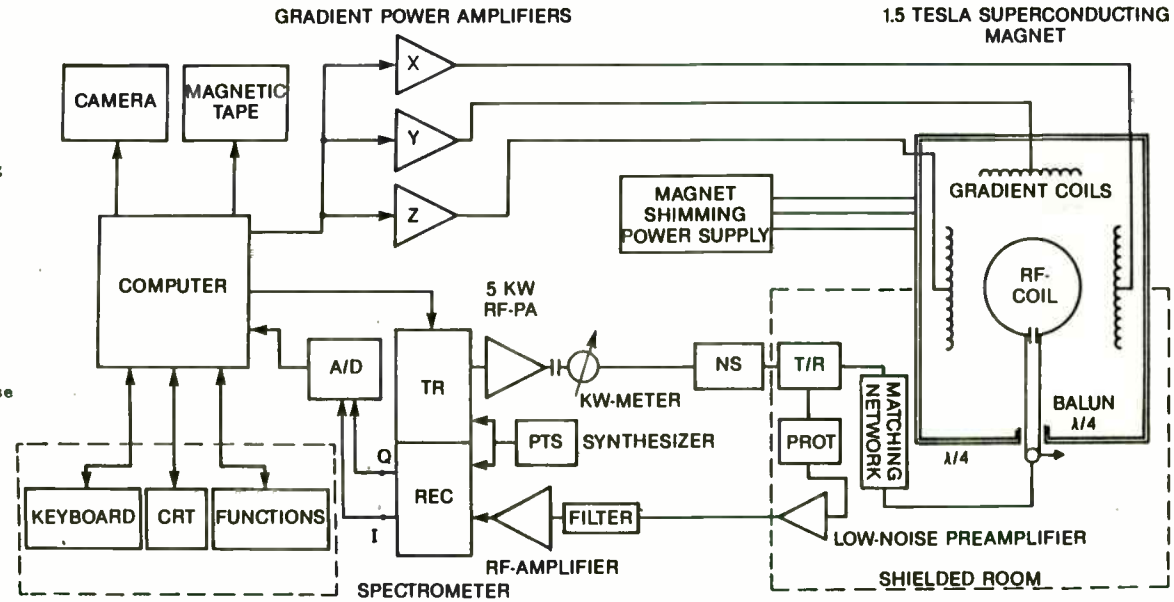


WHOLE-BODY MAGNETIC RESONANCE (MR) IMAGING/SPECTROSCOPY SYSTEM

FIGURE 1

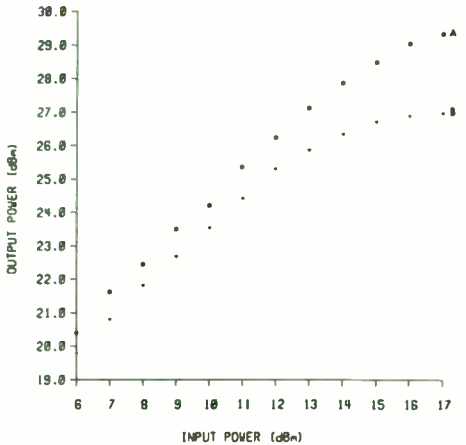
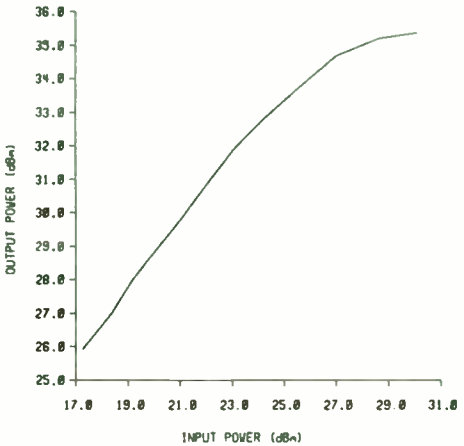


Figure 6. Measured response of Medium-Power Block



8. Measured Response of the High_Power Module

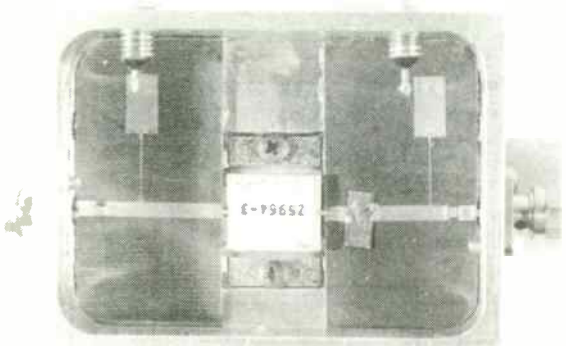


Figure 7. High-Power Block (internally matched) NEZ5964-3

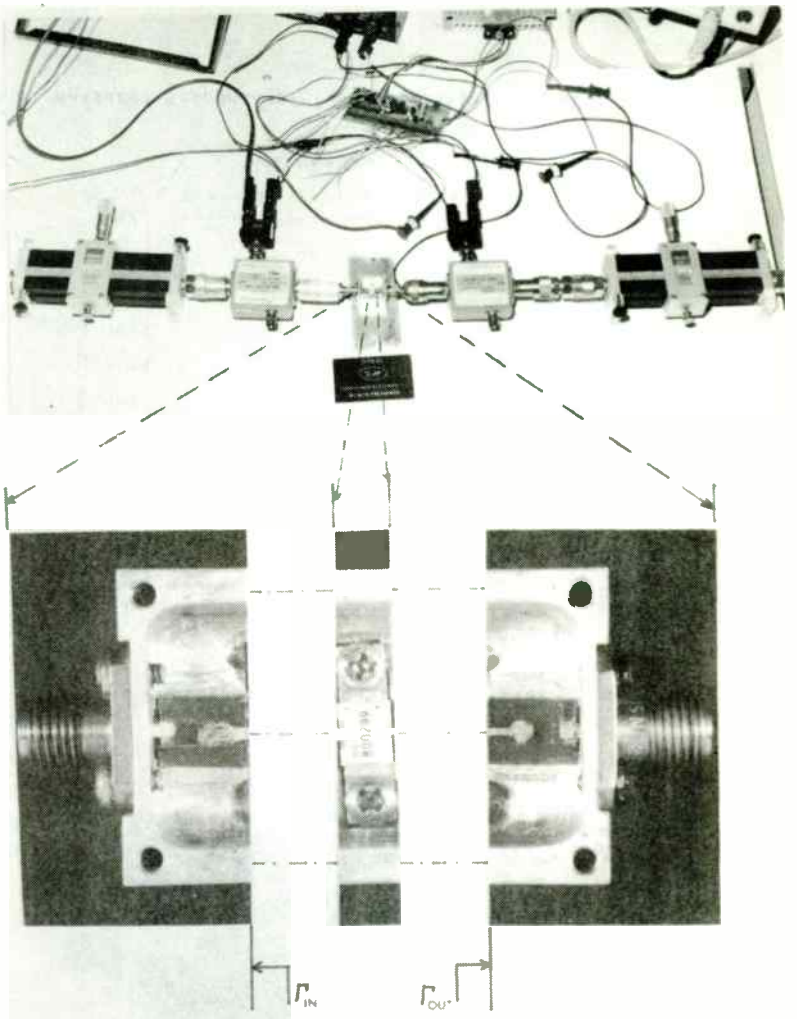
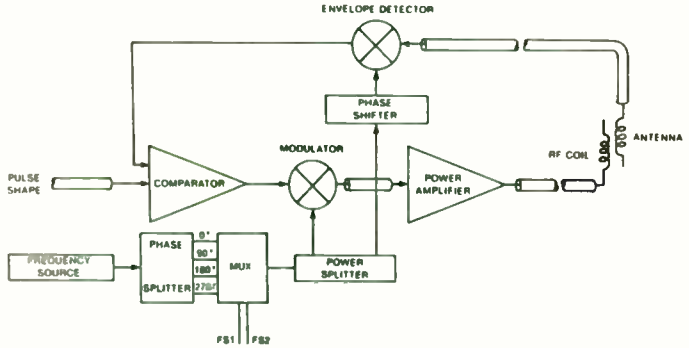
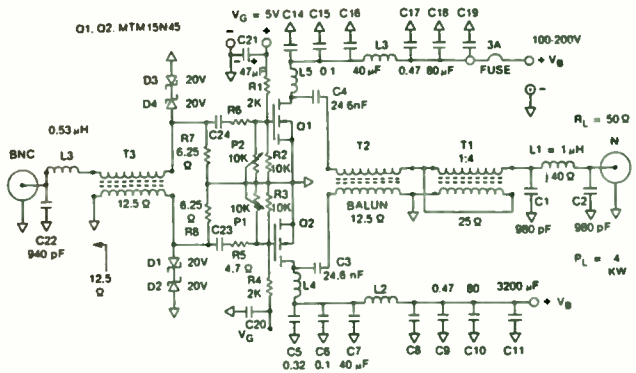


Figura 9. Source and Load Large Signal Characterization



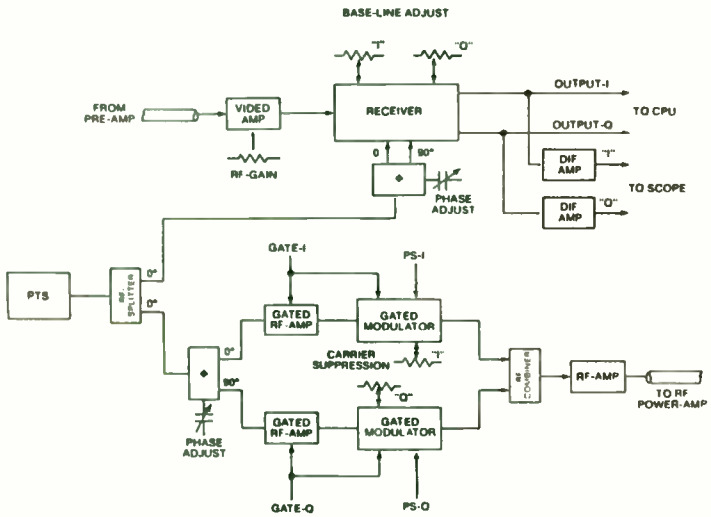
transmitter block diagram

FIGURE 2



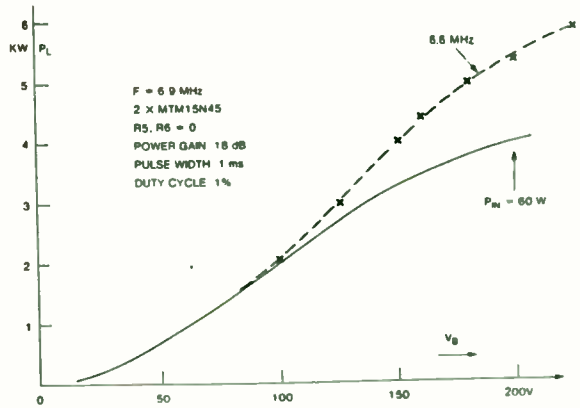
4 KW NMR RF POWER AMPLIFIER: 6.4 MHz (0.15 T)

FIGURE 4



SPECTROMETER BLOCK DIAGRAM FOR MULTISECTION MR IMAGING

FIGURE 3



NMR RF PULSE POWER VS BATTERY VOLTAGE

FIGURE 5

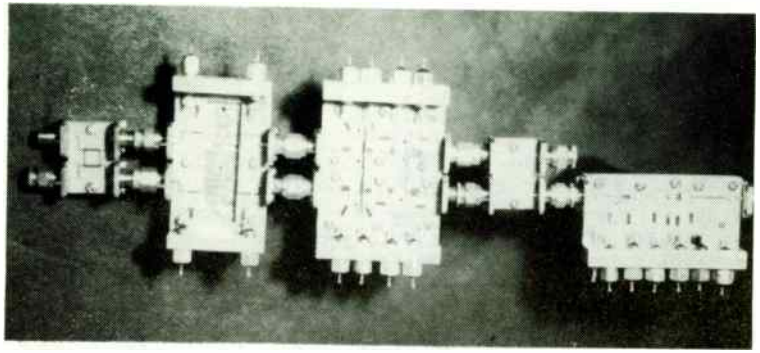


Figura 10. Circuit Topology for the 5 Watt Module

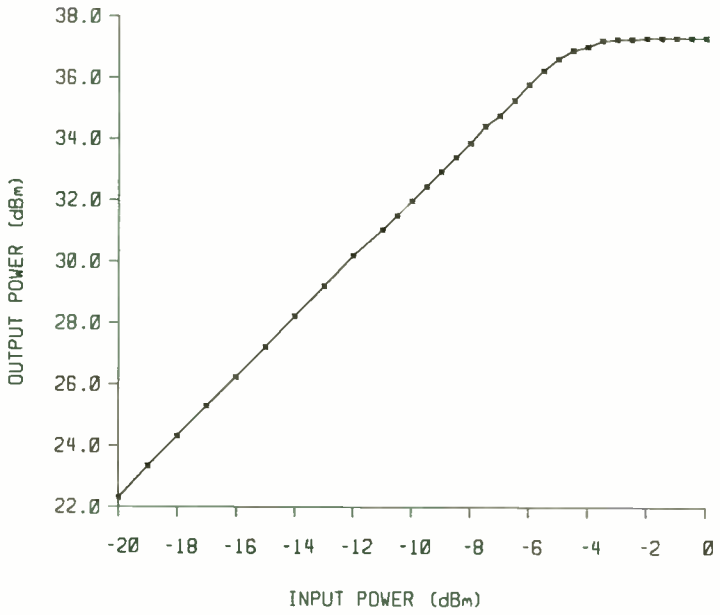


Figure 11. Measured Response of the 5 Watt module at 6.2 GHz

TABLE 1

***** NE7208 GAASFET ANALYSIS *****

S-PARAMETERS IN 50.0 OHM SYSTEM DEVICE GAIN-STABILITY DATA

FREQ	S11		S12		S21		S22		S21	K	DELTA
GHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	DB	FACT	MAG
5.9	0.608	172.	0.099	-9.	2.410	41.	0.390	-103.	7.6	1.0	0.149
6.0	0.597	-162.	0.100	-10.	2.310	36.	0.390	-117.	7.3	1.2	0.216
6.1	0.595	-151.	0.100	-10.	2.280	33.	0.390	-120.	7.2	1.2	0.252
6.2	0.592	-141.	0.100	-10.	2.270	33.	0.390	-125.	7.1	1.3	0.268
6.3	0.588	-115.	0.100	-10.	2.230	30.	0.390	-130.	7.0	1.4	0.334
6.4	0.584	-102.	0.101	-10.	2.200	29.	0.390	-139.	6.8	1.4	0.345

STABILITY CIRCLE LOCATIONS

	---- INPUT PLANE ---------				*---- OUTPUT PLANE ----------*			
FREQ	MAG	ANG	RAD	STABLE	MAG	ANG	RAD	STABLE
5.90	1.706	-166.7	0.69	OUTSIDE	2.866	116.4	1.84	OUTSIDE
6.00	1.815	169.6	0.75	OUTSIDE	3.305	136.1	2.19	OUTSIDE
6.10	1.879	159.6	0.78	OUTSIDE	3.724	142.1	2.57	OUTSIDE
6.20	1.924	150.0	0.81	OUTSIDE	4.002	148.3	2.82	OUTSIDE
6.30	2.128	125.0	0.95	OUTSIDE	6.815	158.2	5.50	OUTSIDE
6.40	2.197	112.1	1.00	OUTSIDE	8.132	167.2	6.78	OUTSIDE

STABLE REGION OUTSIDE OR INSIDE THE STABILITY CIRCLE

REFLECTION COEFFICIENTS FOR MAXIMUM STABLE GAIN

	----- INPUT PLANE ---------			*----- OUTPUT PLANE ---------*			
FREQ	GAMMA S		IMPEDANCE	GAMMA L		IMPEDANCE	GAIN
GHZ	MAG	ANG	OHMS	MAG	ANG	OHMS	DB
5.90	0.881	-166.7	3.2 +J(-5.8)	0.818	116.4	6.9 +J(30.6)	12.5
6.00	0.784	169.6	6.1 +J(4.5)	0.679	136.1	11.0 +J(19.3)	11.2
6.10	0.749	159.6	7.4 +J(8.8)	0.627	142.1	12.7 +J(16.2)	10.7
6.20	0.730	150.0	8.3 +J(13.0)	0.601	148.3	13.4 +J(13.2)	10.5
6.30	0.663	125.0	12.7 +J(24.7)	0.495	158.2	17.5 +J(8.5)	9.8
6.40	0.645	112.1	15.4 +J(31.4)	0.470	167.2	18.2 +J(4.9)	9.6

*** UNCONDITIONALLY STABLE TRANSISTOR ***

GPMAX= 10.53075DB FREQ = 6.200

CONSTANT OPERATING POWER GAIN CIRCLES

GAIN(DB)	RADII	CENTER.MAG	CENTER.ANG
2.50000	0.87554	0.10820	148.29657
4.50000	0.80376	0.16881	148.29657
6.50000	0.69037	0.26110	148.29657
8.50000	0.50575	0.39861	148.29657
10.50000	0.06207	0.59697	148.29657

PA-4: 2 KW-MODULE, 64 MHz

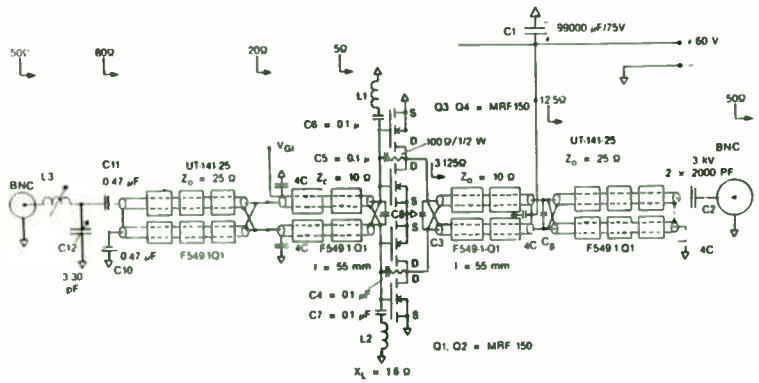
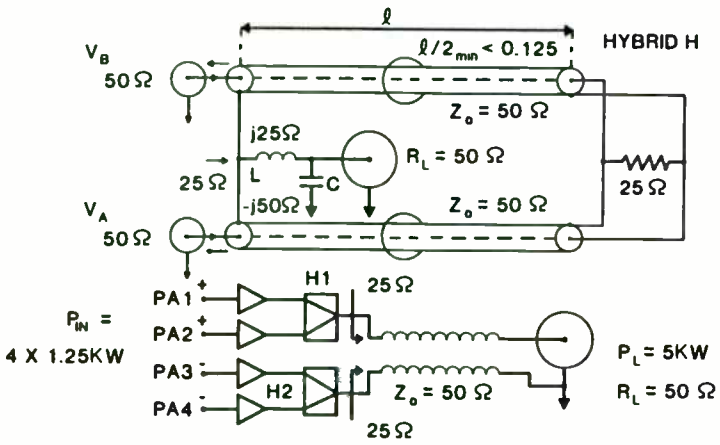
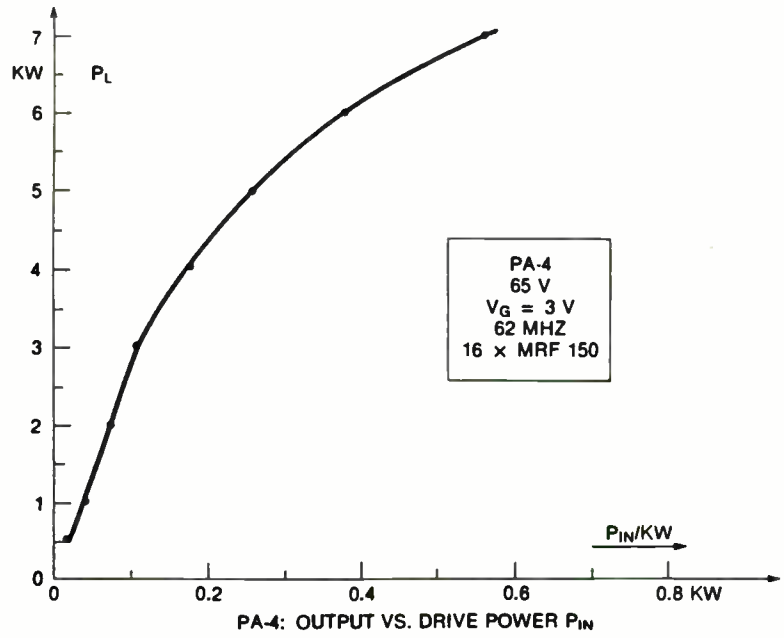


FIGURE 6



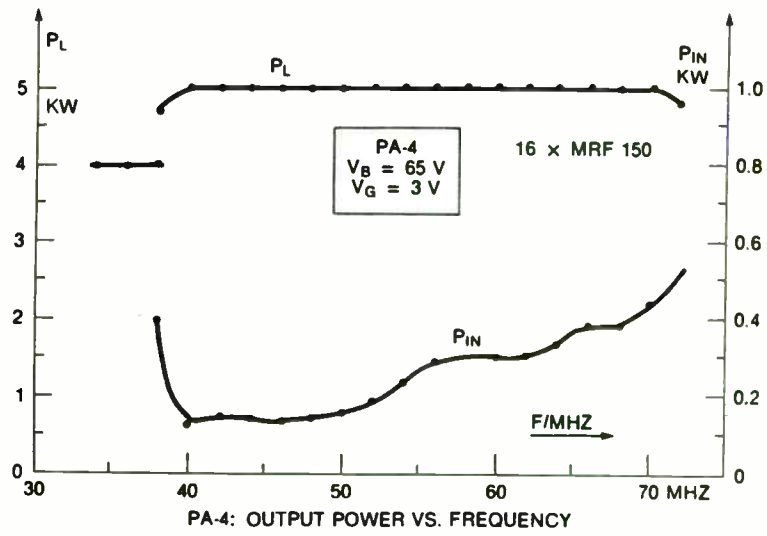
O° POWER COMBINING HYBRID

FIGURE 7



PA-4: OUTPUT VS. DRIVE POWER P_{IN}

FIGURE 8



PA-4: OUTPUT POWER VS. FREQUENCY

FIGURE 9

TABLE 2

***** NE6948 GAASFET ANALYSIS *****

S-PARAMETERS IN 50.0 OHM SYSTEM DEVICE GAIN-STABILITY DATA

FREQ	S11		S12		S21		S22		S21	K	DELTA
GHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	DB	FACT	MAG
5.9	0.805	-116.	0.039	24.	1.620	65.	0.820	-70.	4.2	0.9	0.659
6.0	0.800	-117.	0.040	23.	1.610	63.	0.820	-71.	4.1	0.9	0.655
6.1	0.795	-118.	0.041	22.	1.601	61.	0.820	-72.	4.1	0.9	0.650
6.2	0.790	-119.	0.042	22.	1.594	60.	0.819	-73.	4.0	0.9	0.646
6.3	0.785	-120.	0.043	21.	1.587	58.	0.818	-73.	4.0	0.9	0.641
6.4	0.779	-121.	0.044	21.	1.582	57.	0.817	-74.	4.0	0.9	0.637

STABILITY CIRCLE LOCATIONS

FREQ	INPUT PLANE				OUTPUT PLANE			
	MAG	ANG	RAD	STABLE	MAG	ANG	RAD	STABLE
5.90	1.272	126.7	0.30	OUTSIDE	1.244	80.0	0.27	OUTSIDE
6.00	1.282	128.2	0.30	OUTSIDE	1.244	80.8	0.26	OUTSIDE
6.10	1.292	129.7	0.31	OUTSIDE	1.244	81.5	0.26	OUTSIDE
6.20	1.303	131.0	0.32	OUTSIDE	1.246	82.2	0.26	OUTSIDE
6.30	1.315	132.4	0.34	OUTSIDE	1.249	82.9	0.27	OUTSIDE
6.40	1.327	133.7	0.35	OUTSIDE	1.251	83.6	0.27	OUTSIDE

STABLE REGION OUTSIDE OR INSIDE THE STABILITY CIRCLE

REFLECTION COEFFICIENTS FOR MAXIMUM STABLE GAIN

FREQ	INPUT PLANE			OUTPUT PLANE			
	GAMMA S		IMPEDANCE	GAMMA L		IMPEDANCE	GAIN
GHZ	MAG	ANG	OHMS	MAG	ANG	OHMS	DB
5.90	0.820	129.7	6.0 +J(23.2)	0.879	68.2	10.2 +J(72.9)	13.8
6.00	0.816	131.4	6.1 +J(22.3)	0.881	69.1	9.7 +J(71.7)	13.6
6.10	0.812	133.1	6.1 +J(21.4)	0.884	70.0	9.3 +J(70.6)	13.4
6.20	0.808	134.7	6.2 +J(20.6)	0.887	70.8	8.9 +J(69.6)	13.3
6.30	0.805	136.4	6.3 +J(19.7)	0.889	71.5	8.5 +J(68.7)	13.1
6.40	0.801	138.0	6.3 +J(18.9)	0.891	72.2	8.2 +J(67.9)	13.0

*** POTENTIALLY UNSTABLE TRANSISTOR ***
MSG= 15.79157DB FREQ = 6.200
CONSTANT OPERATING POWER GAIN CIRCLES

GAIN(DB)	RADII	CENTER.MAG	CENTER.ANG
5.75000	0.66179	0.34009	82.19690
7.75000	0.53835	0.46480	82.19690
9.75000	0.40082	0.60472	82.19690
11.75000	0.26401	0.74651	82.19690
13.75000	0.14742	0.87613	82.19690
15.75000	0.08622	0.98392	82.19690

TABLE 3

DESIGN OF THE LOW-POWER BLOCK

FREQ. LOW : 5.90 GHZ FREQ. CENTRAL : 6.20 GHZ FREQ. UPP : 6.40 GHZ
ATTENUATION : 0.10 DB/LAMBDA NUMBER OF ELEMENTS : 13

ELEMENT #	TYPE	Z(OHMS)	LENGTH (L/LAMBDA)	LENGTH (DEGREES)
1	TL	50.000	0.208	75.000
2	SC	510.000	0.000	0.000
3	TL	50.000	0.125	45.000
4	TL	30.525	0.311	111.960
5	FT	0.000	0.000	0.000
6	TL	68.243	0.046	16.560
7	SC	510.000	0.000	0.000
8	TL	68.243	0.046	16.560
9	FT	0.000	0.000	0.000
10	TL	93.375	0.090	32.400
11	TL	50.000	0.125	45.000
12	SC	510.000	0.000	0.000
13	TL	50.000	0.125	45.000

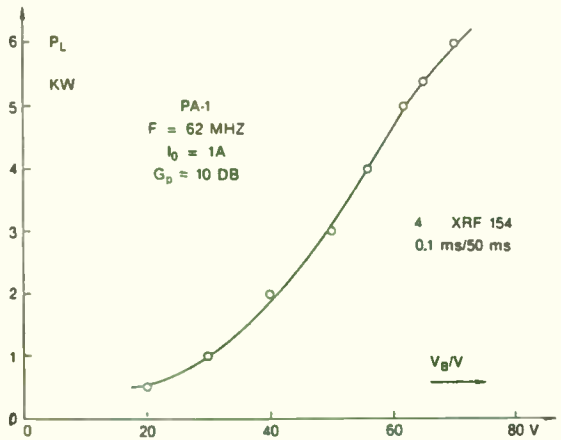
ELEMENT # 5 IS TRANSISTOR TYPE : NE7208
ELEMENT # 9 IS TRANSISTOR TYPE : NE6948

ANALIX

FREQ (GHZ)	GAIN (DB)	K (NUM)	GROUP DELAY (NSEC)	R.L.(INP) (DB)	R.L.(OUT) (DB)
5.90	17.964	2.235	0.233	5.1442	2.7004
6.00	18.675	1.720	0.284	4.6154	2.6799
6.10	18.594	1.858	0.270	4.8264	2.7233
6.20	18.549	2.041	0.230	5.2207	2.7973
6.30	17.617	2.921	0.279	6.3169	2.9112
6.40	17.050	3.498	0.461	7.1336	3.1357

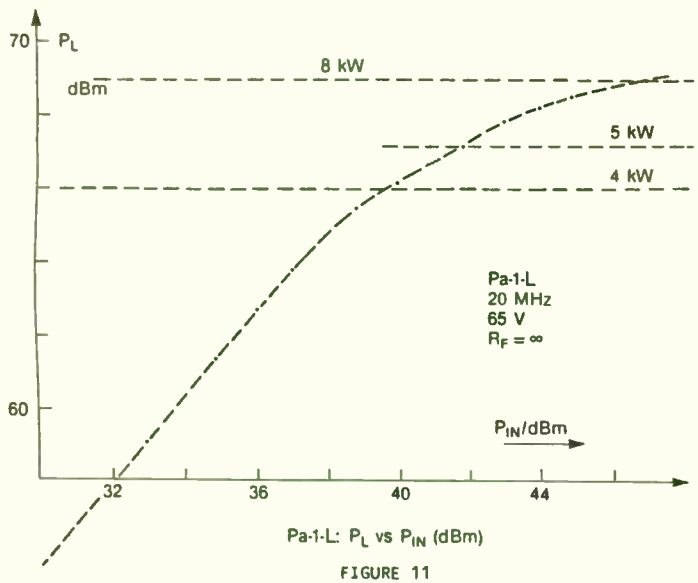
DUROID 5870 ER = : 2.30 H = : 0.7874 T = : 0.0344

ELEMENT #	TYPE	Z(OHMS)	LENGTH(MM)	WIDTH(MM)
1	TL	50.00	7.318	2.322
2	SC	510.00	1.250	0.000
3	TL	50.00	4.391	2.322
4	TL	30.52	10.689	4.631
5	FT	0.00	2.000	0.000
6	TL	68.24	1.641	1.389
7	SC	510.00	1.250	0.000
8	TL	68.24	1.641	1.389
9	FT	0.00	2.000	0.000
10	TL	93.38	3.264	0.734
11	TL	50.00	4.391	2.322
12	SC	510.00	1.250	0.000
13	TL	50.00	4.391	2.322



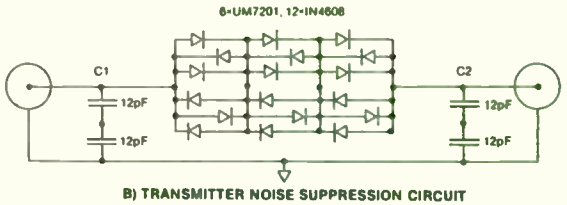
PA-1: OUTPUT POWER VS SUPPLY VOLTAGE (DC)

FIGURE 10



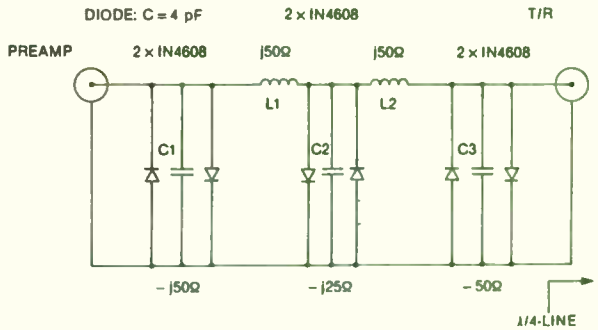
Pa-1-L: P_L vs P_{IN} (dBm)

FIGURE 11



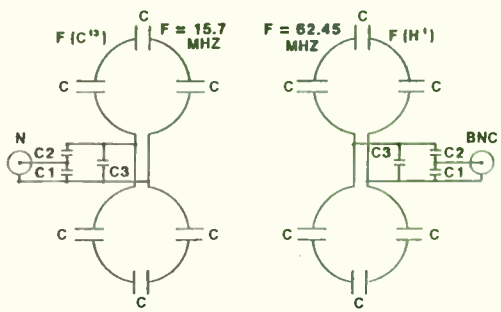
B) TRANSMITTER NOISE SUPPRESSION CIRCUIT

FIGURE 12



PREAMPLIFIER PROTECTION CIRCUIT

FIGURE 13



C^{13} AND H^1 DECOUPLER COIL

FIGURE 14

TABLE 4

***** NE9001 GAASFET ANALYSIS *****

S-PARAMETERS IN 50.0 OHM SYSTEM DEVICE GAIN-STABILITY DATA

FREQ	S11		S12		S21		S22		S21	K	DELTA
GHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	DB	FACT	MAG
5.9	0.890	-153.	0.051	-6.	1.328	44.	0.576	-107.	2.5	0.8	0.486
6.0	0.890	-154.	0.050	-7.	1.310	42.	0.580	-108.	2.3	0.9	0.490
6.1	0.889	-155.	0.050	-7.	1.304	41.	0.583	-109.	2.3	0.9	0.492
6.2	0.888	-155.	0.050	-7.	1.298	40.	0.586	-109.	2.3	0.9	0.494
6.3	0.887	-156.	0.050	-7.	1.292	38.	0.589	-110.	2.2	0.9	0.497
6.4	0.886	-156.	0.050	-7.	1.286	37.	0.592	-111.	2.2	0.9	0.499

STABILITY CIRCLE LOCATIONS

	---- INPUT PLANE ---------				*---- OUTPUT PLANE ---------*			
FREQ	MAG	ANG	RAD	STABLE	MAG	ANG	RAD	STABLE
5.90	1.103	156.2	0.12	OUTSIDE	1.635	126.7	0.71	OUTSIDE
6.00	1.103	157.2	0.12	OUTSIDE	1.619	127.5	0.68	OUTSIDE
6.10	1.104	157.8	0.12	OUTSIDE	1.610	127.8	0.67	OUTSIDE
6.20	1.105	158.4	0.12	OUTSIDE	1.602	128.1	0.66	OUTSIDE
6.30	1.106	159.1	0.12	OUTSIDE	1.594	128.5	0.64	OUTSIDE
6.40	1.107	159.7	0.12	OUTSIDE	1.586	128.9	0.63	OUTSIDE

STABLE REGION OUTSIDE OR INSIDE THE STABILITY CIRCLE

REFLECTION COEFFICIENTS FOR MAXIMUM STABLE GAIN

	----- INPUT PLANE ---------			*----- OUTPUT PLANE ---------*			
FREQ	GAMMA	S	IMPEDANCE	GAMMA	L	IMPEDANCE	GAIN
GHZ	MAG	ANG	OHMS	MAG	ANG	OHMS	DB
5.90	0.918	157.7	2.2 +J(9.8)	0.712	101.2	13.8 +J(39.2)	12.2
6.00	0.918	158.8	2.2 +J(9.4)	0.717	102.8	13.2 +J(38.2)	12.1
6.10	0.918	159.4	2.2 +J(9.1)	0.723	103.5	12.8 +J(37.8)	12.0
6.20	0.917	160.1	2.2 +J(8.8)	0.730	104.2	12.4 +J(37.4)	11.9
6.30	0.917	160.8	2.2 +J(8.5)	0.736	105.0	11.9 +J(37.0)	11.9
6.40	0.916	161.4	2.2 +J(8.2)	0.743	105.8	11.5 +J(36.6)	11.8

*** POTENTIALLY UNSTABLE TRANSISTOR ***
MSG= 14.14304DB FREQ = 6.200
CONSTANT OPERATING POWER GAIN CIRCLES

GAIN(DB)	RADII	CENTER.MAG	CENTER.ANG
4.00000	0.79946	0.20599	128.11469
6.00000	0.70549	0.30364	128.11472
8.00000	0.58267	0.43321	128.11469
10.00000	0.43677	0.59284	128.11469
12.00000	0.29042	0.77241	128.11469
14.00000	0.20561	0.95492	128.11469

TABLE 6

***** NE8002 GAASFET ANALYSIS *****

S-PARAMETERS IN 50.0 OHM SYSTEM DEVICE GAIN-STABILITY DATA

FREQ	S11		S12		S21		S22		S21	K	DELTA
GHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	DB	FACT	MAG
5.9	0.834	140.	0.066	16.	1.302	-29.	0.555	161.	2.3	0.9	0.408
6.0	0.830	138.	0.070	15.	1.300	-31.	0.560	160.	2.3	0.9	0.407
6.1	0.825	136.	0.074	13.	1.299	-33.	0.564	159.	2.3	0.9	0.404
6.2	0.822	133.	0.078	10.	1.296	-36.	0.572	157.	2.3	0.8	0.404
6.3	0.816	132.	0.082	10.	1.298	-37.	0.573	156.	2.3	0.8	0.400
6.4	0.810	126.	0.090	5.	1.290	-43.	0.590	152.	2.2	0.7	0.403

STABILITY CIRCLE LOCATIONS

	---- INPUT PLANE ---------				*---- OUTPUT PLANE ---------*			
FREQ	MAG	ANG	RAD	STABLE	MAG	ANG	RAD	STABLE
5.90	1.155	-143.0	0.16	OUTSIDE	1.587	-174.7	0.61	OUTSIDE
6.00	1.158	-141.5	0.17	OUTSIDE	1.575	-173.5	0.61	OUTSIDE
6.10	1.163	-139.7	0.19	OUTSIDE	1.566	-172.2	0.62	OUTSIDE
6.20	1.163	-137.2	0.20	OUTSIDE	1.538	-170.1	0.62	OUTSIDE
6.30	1.171	-136.1	0.21	OUTSIDE	1.543	-169.6	0.63	OUTSIDE
6.40	1.172	-130.7	0.23	OUTSIDE	1.496	-165.6	0.62	OUTSIDE

STABLE REGION OUTSIDE OR INSIDE THE STABILITY CIRCLE

REFLECTION COEFFICIENTS FOR MAXIMUM STABLE GAIN

	----- INPUT PLANE ---------			*----- OUTPUT PLANE ---------*			
FREQ	GAMMA	S	IMPEDANCE	GAMMA	L	IMPEDANCE	GAIN
GHZ	MAG	ANG	OHMS	MAG	ANG	OHMS	DB
5.90	0.880	-144.7	3.5 +J(-15.9)	0.648	-152.4	11.3 +J(-11.7)	10.4
6.00	0.879	-143.3	3.6 +J(-16.5)	0.653	-150.7	11.2 +J(-12.5)	10.4
6.10	0.877	-141.7	3.7 +J(-17.3)	0.656	-149.0	11.1 +J(-13.2)	10.4
6.20	0.879	-139.3	3.7 +J(-18.5)	0.658	-146.8	11.2 +J(-14.2)	10.5
6.30	0.875	-138.3	3.8 +J(-18.9)	0.661	-145.8	11.1 +J(-14.7)	10.4
6.40	0.878	-133.2	3.9 +J(-21.5)	0.667	-141.5	11.1 +J(-16.7)	10.7

*** POTENTIALLY UNSTABLE TRANSISTOR ***
MSG= 12.20510DB FREQ = 6.200
CONSTANT OPERATING POWER GAIN CIRCLES

GAIN(DB)	RADII	CENTER.MAG	CENTER.ANG
2.00000	0.80216	0.20561	-170.11221
4.00000	0.71071	0.30224	-170.11221
6.00000	0.59266	0.42962	-170.11221
8.00000	0.45532	0.58527	-170.11221
10.00000	0.32250	0.75869	-170.11221
12.00000	0.24651	0.93315	-170.11221

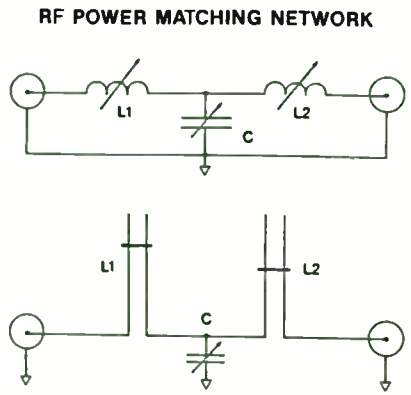


FIGURE 15: POWER MATCHING NETWORK

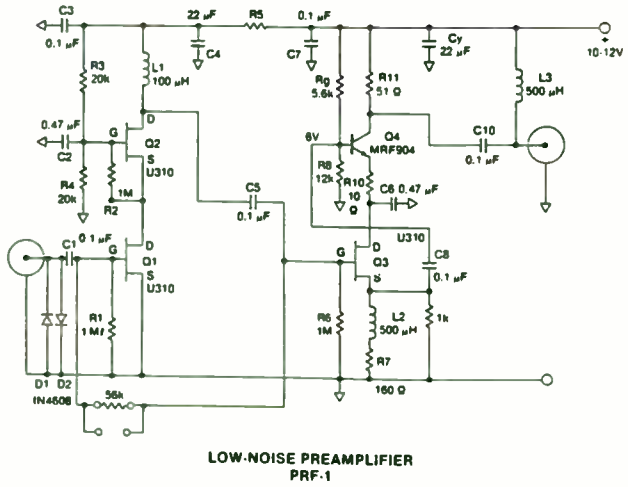
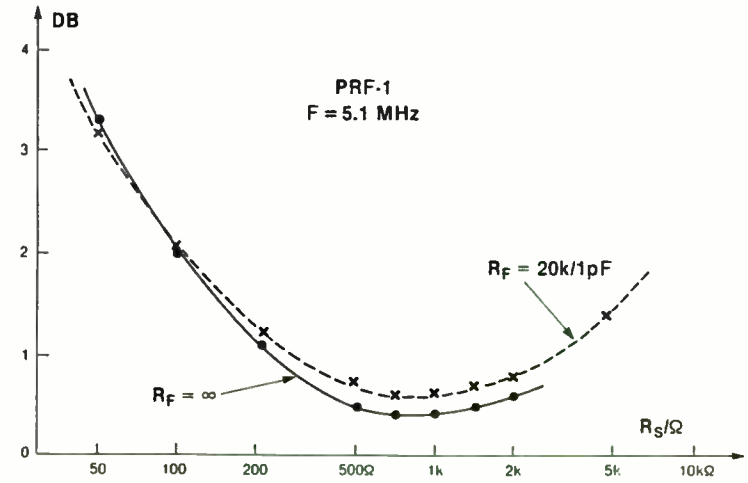
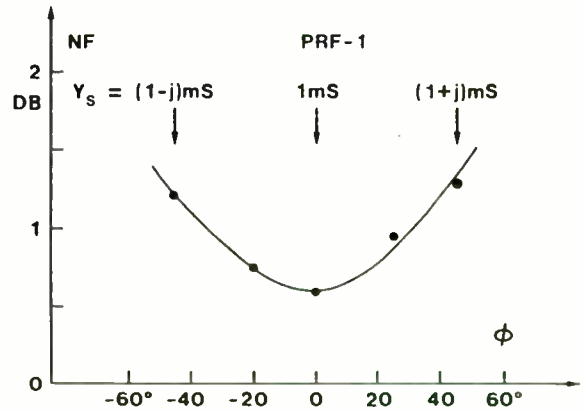


FIGURE 16



NOISE FIGURE VS SOURCE RESISTOR

FIGURE 17



NOISE FIGURE AS A FUNCTION OF THE SOURCE ADMITTANCE PHASE ANGLE

FIGURE 18

TABLE 7

DESIGN OF THE MEDIUM-POWER BLOCK

FREQ. LOW : 5.90 GHZ FREQ. CENTRAL : 6.20 GHZ FREQ. UPP : 6.40 GHZ
MICROSTRIP ATTENUATION : 0.10 dB NUMBER OF ELEMENTS : 16

ELEMENT #	TYPE	Z(OHMS)	LENGTH/LAMBDA	LENGTH (DEGREES)
1	TL	50.000	0.208	75.000
2	SC	810.000	0.000	0.000
3	TL	50.000	0.125	45.000
4	TL	13.691	0.200	72.000
5	TL	33.934	0.070	25.200
6	FT	0.000	0.000	0.000
7	TL	47.691	0.069	24.840
8	TL	17.625	0.157	56.520
9	SC	810.000	0.000	0.000
10	TL	43.375	0.227	81.720
11	TL	22.625	0.130	46.800
12	FT	0.000	0.000	0.000
13	TL	24.243	0.185	66.600
14	TL	50.000	0.125	45.000
15	SC	810.000	0.000	0.000
16	TL	50.000	0.208	75.000

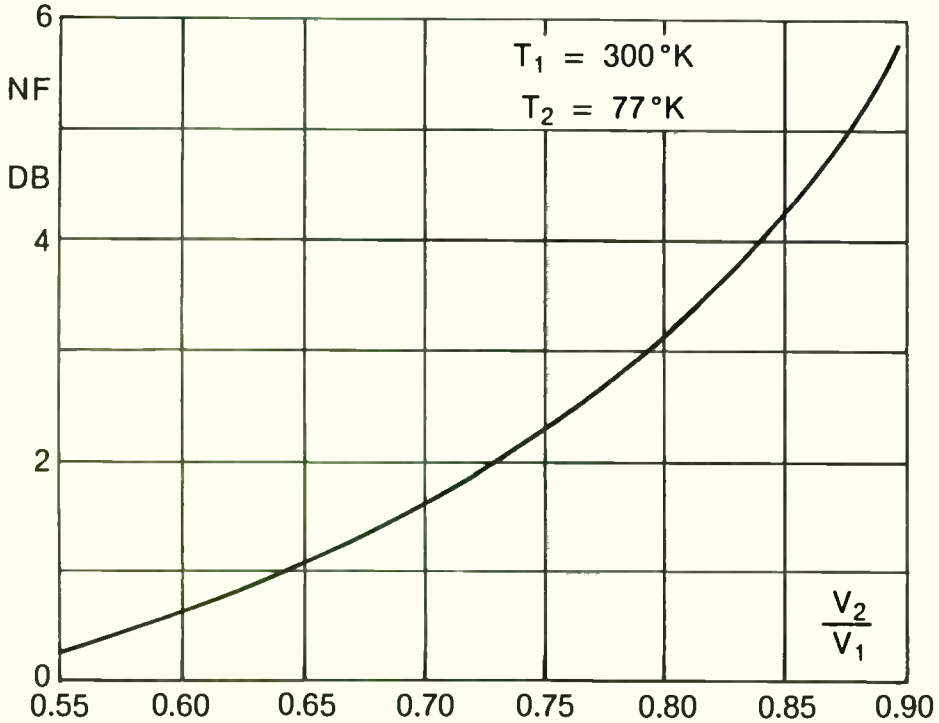
ELEMENT # 6 IS TRANSISTOR TYPE : NE9001
ELEMENT # 12 IS TRANSISTOR TYPE : NE8002

ANALIX

FREQ (GHZ)	GAIN (DB)	K NUM	GROUP DELAY (NSEC)	R.L.(IN) (DB)	R.L.(OUT) (DB)
5.90	19.691	0.662	0.931	1.5982	8.2322
6.00	21.419	0.582	0.880	2.3383	7.7162
6.10	22.193	0.636	1.015	3.4733	7.7352
6.20	22.000	0.829	0.858	5.3486	8.0659
6.30	21.106	1.086	0.761	6.5491	8.7369
6.40	19.341	1.612	1.470	10.1120	7.4513

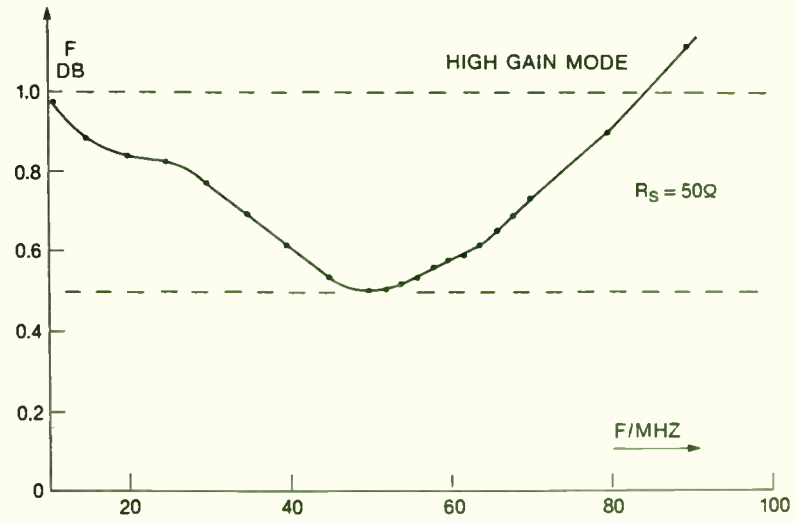
DUROID 6010.5 ER : 10.5 H : 0.635 T : 0.0344

ELEMENT #	TYPE	Z(OHMS)	LENGTH(MM)	WIDTH(MM)
1	TL	50.00	3.889	0.527
2	CS	810.00	1.100	0.000
3	TL	50.00	2.333	0.527
4	TL	13.69	3.531	4.155
5	TL	33.93	1.258	1.139
6	FT	0.00	3.000	0.000
7	TL	47.69	1.282	0.587
8	TL	17.63	2.672	3.010
9	CS	810.00	1.100	0.000
10	TL	43.38	4.178	0.717
11	TL	22.63	2.256	2.140
12	FT	0.00	4.000	0.000
13	TL	24.24	3.404	1.937
14	TL	50.00	2.333	0.527
15	CS	810.00	1.100	0.000
16	TL	50.00	3.889	0.527



LIQUID NITROGEN METHOD:
NOISE FIGURE AS A FUNCTION OF THE
NOISE VOLTAGE RATIO V_2/V_1.

FIGURE 20



LNA-V-1: NOISE FIGURE F VS FREQUENCY

FIGURE 19

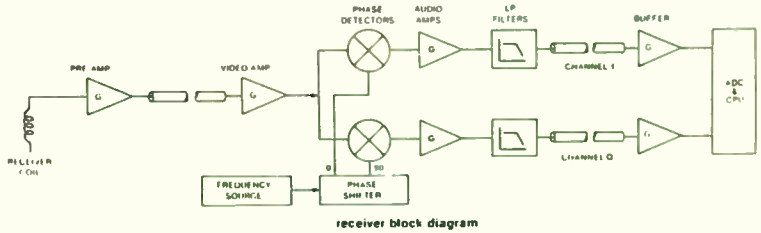


FIGURE 21: RECEIVER CIRCUIT FOR NMR

PHASE NOISE INTERMODULATION AND DYNAMIC RANGE

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Plessey Semiconductors
Cheney Manor
Swindon
England

The radio receiver lives and works in a non-benign environment. It needs to pick out a very weak wanted signal from a background of noise at the same time as it rejecta a large number of much stronger unwanted signals. These may be present either fortuitously, aa in the case of the overcrowded radio spectrum, or because of deliberate action, as in the case of Electronic Warfare. In either case, the use of suitable devices may considerably influence the job of the equipment designer.

Dynamic range is a "catch all" term, applied to limitations of intermodulation or phase noise: it has many definitions depending upon the application. Firstly, however, it is advisable to define those terms which limit the dynamic range of a receiver.

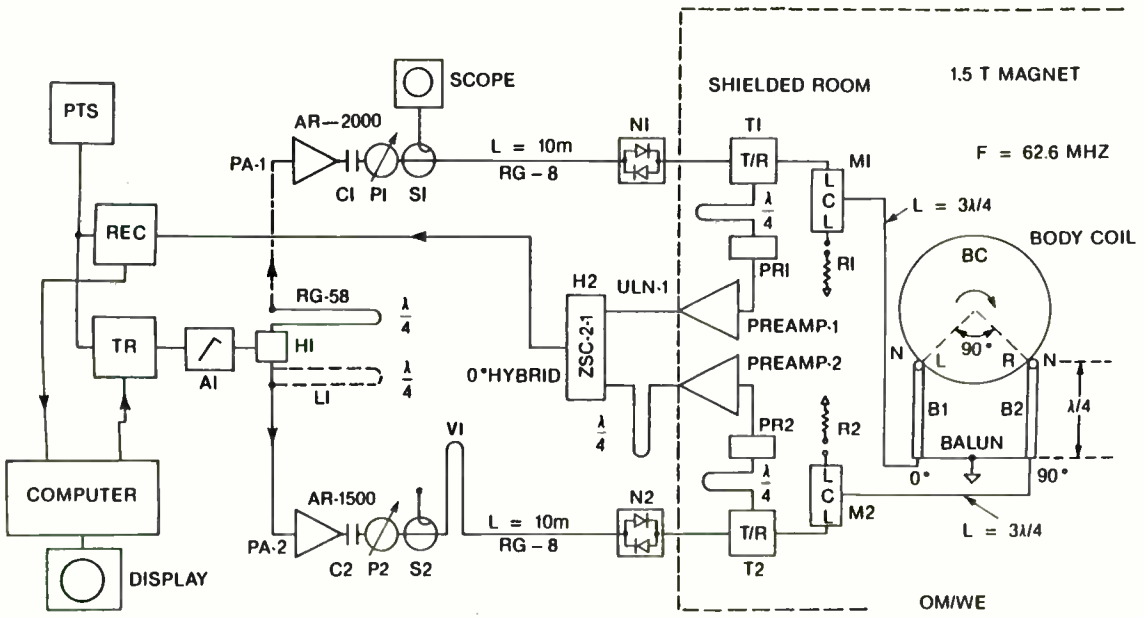
Intermodulation

This is described as the "result of a non linear transfer characteristic". The mathematics have been exhaustively treated, and Ref. 1 is recommended for those interested.

The effects of intermodulation are similar to those produced by mixing and harmonic production, insofar as the application of two signals of frequencies f_1 and f_2 produce outputs of $2f_2-f_1$, $2f_1-f_2$, $2f_1$, $2f_2$ etc. The levels of these signals are dependent upon the actual transfer function of the device and thus vary with device type. For example, a truly square law device, such as a perfect FET, produces no third order products ($2f_2-f_1$, $2f_1-f_2$). Intermodulation products are additional to the harmonics $2f_1$, $2f_2$, $3f_1$, $3f_2$ etc. Fig. 1 shows intermodulation products diagrammatically.

The effects of intermodulation are to produce unwanted signals, and these degrade the effective signal to noise ratio of the wanted signal. Consider firstly the discrete case of a weak wanted signal on 7.010 MHz and two large unwanted signals on 7.020 and 7.030 MHz. A third order product (2 x 7.02 - 7.03) falls on the wanted signal, and may completely drown it out. Fig. 2 shows the toal HF spectrum from 1.5 to 41.5 MHz and Fig. 3 shows the integrated power at the front end of a receiver tuned to 7 MHz. It may be seen that just as white light is made up from all the colours of the spectrum, so the total power produced by so many signals approximates to a large wide band noise signal. Now, it has already been shown that 2 signals, f_1 and f_2, produce third order intermodulation products of $2f_1-f_2$ and $2f_2-f_1$. The signals will produce third order products somewhat greater in number, viz: $2f_1-f_2$, $2f_1-f_3$, $2f_2-f_1$, $2f-f_3$, $2f-f_1$ and $2f_3-f_2$. An increase in the number of input signals will multiply greatly the effects of intermodulation, and will manifest itself as a rise in the noise floor of the receiver.

The amplitude relationships of the third order intermodulation products and the fundamental tones may be derived from Ref. 1, where it is shown that the intermodulation product amplitude is proportional to the cube of the input signal level. Thus an increase of 3dB in input level will produce an increase of 9dB in the levels of the intermodulation products. Fig. 4 shows this in graphic form, and the point where the graphs of fundamental power and intermodulation power cross is the THIRD ORDER INTERCEPT POINT.



1.5 TESLA NMR IMAGING SYSTEM WITH QUADRATURE EXCITATION/RECEIVING

FIGURE 22

The third order intercept point is, however, a purely theoretical concept. This is because the worat possible intermodulation ratio is 13dB (Ref. 2), so that in fact the two graphs never cross. In addition, the finite output power capability of the device leads to GAIN COMPRESSION.

Thus, it is apparent that the intermodulation produced noise floor in a receiver is related to the intercept point, and Figs. 5, 6 and 7 show the noise floor produced by various intercept points, in a receiver fed from an antenna - a realistic teat! Fig. 5 ahows that a large number of signals are below the noise floor and are thus lost; this representa a 0dBm intercept point. Fig. 7 shows a +20dBm intercept point noise floor, and it is obvious that many more signals may be received.

Becauae of the rate at which intermodulation products increase with input level (3dB on the I.P. for 1dB on the fundamental), the addition of an attenuator at the front end can improve the signal to noise ratio, aa an increase in attenuation of 3dB will reduce the wanted signal by 3dB, but the intermodulation will decreaae by 9dB. However, it is a fair comment that aerial attenuators are an admiasion of defeat, as suitable deaign does not require it!

The concept of dynamic range ia often used when discuasing intermodulation. Fig. 8 shows total receiver dynamic range, which is defined as the spurious Free Dynamic Range. Obviously an intermodulation product lying below the receiver noise floor may be ignored. Thus the uaable dynamic range is that input range between the noise floor and the input level at which the intermodulation product reaches the noise floor. In fact

EQUATION (1)

$$D.R. = \frac{2}{3} (I_3 - N.F.)$$

Where D.R. is the dynamic range in dB
I_3 is the intermodulation input intercept point in dBM
N.F. is the noise floor in dBM.

Note that in any particular receiver, the noise floor is related to the bandwidth; dynamic range ia similarly so related.

HF receivers will often require input intercept points of +20dBm or more. The usable noise factor of HF receivers is normally 10-12dB: exceptionally 7 or 8 dB may be required when small whip antennaa are used. An SSB bandwidth would have a dynamic range of 105.3 dB. The same receiver with a 100 Hz C.W. bandwidth would have a dynamic range of 114.6 dB and thua dynamic range is quite often a confusing and imprecise term.

VHF receivers require noise figures of 1 or 2dB for moat critical applicationa, and where co-sited transmitters are concerned, signals at 0 dBm or more are not uncommon. However, such aignals are usually aeparated by at least 5% in frequency and filters can be provided. Close in signals at levels of -20dBm are not uncommon, and dynamic rangea in SSB bandwidtha of about 98 dB are required.

The achievement of high input intercept points and low noiae factors is not neceaaarily easy. The uaual superhet architecture follows the mixer with some sort of filter, frequently a crystal filter, and the performance of this filter may well limit the performance. Crystal filters are not the linear reciprocal two part networks that theory suggests, being neither linear or reciprocal. It has been suggested that the IMD is produced by ferrite cored transformers, but experiments have shown that ladder filtera with no transformers suffer similarly. Thus, although ferrite cored tranaformers can contribute, other mechaniama dominate in theae components. The most probable is the failure of the piezo-electric material to follow Hook's Law at high input levels, and possibly the use of cryatal cuta other than AT could help insofar as the relative mechanical cryatal distortion ia reduced. The use of SAW filters is attractive, since they are not bulk wave devicea and do not suffer to such an extent from IMD; however, it is neceaaary to use a resonant SAW to achieve the neceasary bandwidtha and low insertion loasea.

THE Q FACTOR OF MICROSTRIP MATCHING NETWORK IN RF CLASS C AMPLIFIER DESIGN

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ABSTRACT

The Q factor of an impedance matching network incorporating microstrips as inductances has a bounded value. This paper shows how strip lengths as a function of Q are evaluated numerically with greater accuracy compared to using graphical construction on a Smith chart. An example of a 162 MHz 100-watt class C amplifier is also given.

INTRODUCTION

Microstrip has long been associated with microwave passive or active circuit design since at such frequencies a certain length of strip can be made to behave as a capacitance or inductance according to its physical dimension with respect to the electrical wavelength (λ). When designed as a transmission line, it can also be used for impedance transformation or matching between an active device and its source and load impedances.

The expressions relating impedance variation along a line terminated by a load other than Z_0, its characteristic impedance are rather simple. But their numerical evaluation requires complex hyperbolic or circular function manipulations which are still performed graphically.

Now that pocket computers incorporated with high level programming facilities such as the BASIC Language are available, the time has come for every circuit designer to do the calculations by machine with greater accuracy and less time consuming effort.

In RF Class C power power amplifier design, one often encounters low input and output transistor impedances. The simple method using 2-element L, C components to match them to the 50 Ω source and load impedances results in poor harmonic rejection and power efficiency (Fig. 1a). General practice consists of increasing the Q of the matching network by adding an inductance in series with the transistor's input/output impedances as shown in Fig. 1b.

In high frequency operation, the required inductance is rather small and its precise value becomes difficult to achieve using a conventional coil. For this reason, most practical VHF, UHF amplifiers adopt microstrip to replace this lumped constant.

In the literature[1-4], the designers often choose a certain length of strip and then try to match the transistor to the source or load with the

The design of active components such as amplifiers is relatively straightforward. Amplifiers of low noise and high dynamic range are fairly easy to produce, especially with transformer feedback, although where high reverse isolation is required, care must be taken. Mixers are however, another matter.

Probably the most popular mixer is the diode ring (Fig. 9). Although popular, this mixer does have some drawbacks, which have been well documented. These are:-

insertion loss (normally about 7dB)
high L.O. drive power (up to +27dBm)
termination sensitive (needs a wideband 50 ohms)
poor interport isolation (40dB)

The insertion loss is a parameter which may be classed merely as annoying, although it does limit the overall noise figure of the receiving system. The high L.O. drive power means a large amount of D.C. is required, affecting power budgets in a disastrous way, while termination sensitivity may mean the full potential of the mixer cannot be realised.

For the diode ring to perform adequately, a good termination "from D.C. to daylight" is required: definitely at the image frequency (LO$\pm$ sig. freq.) and preferably at the harmonics as well. Finally, interport isolation of 40dB with a +27dBm LO still leaves - 13dBm of LO radiation to be filtered or otherwise suppressed for reaching the antenna.

A further problem with the simple diode ring of this form is that the "OFF" diodes are only OFF by the forward voltage drop of the ON diodes. Thus the application of an input which exceeds this OFF voltage leads to the diodes trying to turn ON, giving gain compression and reduced IMD performance.

Fig. 10 shows a variation of this in which series resistors are added. The current flow through these resistors increases the reverse bias on the OFF diodes which gives a higher gain compression point: such a mixer can give +36dBm intercept points with a +30dBm of LO drive. Nevertheless, as is common to all commutative mixers, the intermodulation performance is related to the termination, and the LO radiation from the input port is relatively high.

Variations of this form of mixer include the Rafuse Quad MOSFET mixer of Fig. 11, which suffers with many of the same problems. Fig. 12 shows a dual VMOS mixer capable of good performance, but requiring a lare amount of D.C. power and with limited isolation of the LO injection.

Many advantages accrue to the choice of the transistor tree type of approach (Fig. 13). Here the input signal produces a current in the collectors of the lower transistors and this current is commutated by the upper set of switching transistors. Because the current is to a first order approximation independent of collector voltage, the transistor tree does not exhibit the sensitivity to load impedance that the diode ring does, and indeed, by the use of suitable load impedances, gain may be achieved. The non linearity of the voltage to current conversion in the base emitter junction of the bottom transistors is the major cause of intermodulation, but by using suitably large transistors and emitter degeneration, very high performances (+32dBm input intercept) can be achieved. The Plessey SL6440 has been described (Refs. 3, 4, 5) and uses these techniques to achieve a high standard of performance. (See Fig. 16).

aid of the Smith chart. This method is rather empirical and the Q of the network is either undefined or cannot be determined accurately. The following shows how the quality factor is related to the circuit parameters as well as strip lengths in a practical design.

DESIGN PROCEDURE

With reference to Fig. 1c, let the microstrip of length ℓ and characteristic impedance Z_O replace the lumped constant of reactance X_L of Fig. 1b. From the general low loss line equation, the normalized input impedance of the microstrip is :

$$z_{in} = \frac{z_T + j\tau}{1 + jz_T\tau} = r_{in} + jx_{in} \qquad (1)$$

where $\tau = \tan\beta\ell$, $\beta = 2\pi/\lambda$ and $z_T = (R_T + jX_T) / Z_O$

$= r + jx$

By definition,

$Q = x_{in} / r_{in}$.

We can then deduce the strip length as a function of x, r and Q, giving

$$\ell = \frac{1}{\beta} \arctan \frac{(1 - x^2 - r^2) \pm [(1 - x^2 - r^2)^2 - 4(Q^2 r^2 - x^2)]^{1/2}}{2(rQ + x)} \qquad (2)$$

Since ℓ is real, the expression under the square root must be positive, leading to the relation :

$$Q^2 < [(r - 1)^2 + x^2][(r + 1)^2 + x^2] / 4r^2 \qquad (3)$$

or $$Q^2_{max} = [(r - 1)^2 + x^2][(r + 1)^2 + x^2] / 4r^2 \qquad (4)$$

From the above expression it can be seen that the Q of a network using transmission lines as inductances has an upper bounded value. In practice, the input and output networks of a Class C power amplifier require a Q of the order of 10. This condition can generally be met without any difficulty.

AMPLIFIER DESIGN

The following example is taken from the design of a 100 Watt Class C amplifier operating at 162 MHz for ^{31}P NMR in-vivo imaging experiments. The power transistor MRF 317 has the following impedances at the rated output power :

$Z_T = 0.77 + j\ 1.4\ \Omega$ (input)

$Z_T = 1.77 - j\ 1.0\ \Omega$ (output)

By choosing strip widths equal to that of the transistor base and collector leads, respectively 5.2 mm and 3.955 mm, and using a copper clad Teflon glass PC board with the following characteristics :

Dielectric constant $\epsilon_r = 2.55$

substrate thickness h = 1.52 mm and

Copper thickness t = 35 μ

Z_O was first calculated as a function of the strip widths[6,7] then strip lengths vs Q as determined by relatin (2) were tabulated as shown in Tables I and II. For our amplifier, choosing Q = 13 for both the injput and output networks led to strip lengths of 4.2 and 11.4 cm, respectively. The latter were etched on a PC board which was designed to accommodate the power transistor as well as the matching capacitors[8] [Fig. 2].

Phase Noise

The mixing process for the superhet receiver is shown in Fig. 14, where an incoming signal mixes with the local oscillator (LO) to product the intermediate frequency (IF). Fig. 15 shows the effect of noise modulation on the LO, where the noise sidebands of the LO mix with a strong, off channel signal to produce the IF. This means that the phase noise performance of the LO affects the capability of the receiver to reject off channel signals, and thus the receiver selectivity is not necessarily defined by the signal path filters.

This phenomena is referred to as RECIPROCAL MIXING, and has tended to become more prominent with the increased use of frequency synthesisers in equipments.

The performance level requirements of receivers is dependent upon the application. Some European mobile radio specifications call for 70dB of adjacent channel rejection equating to some -122 dBc/Hz, while an HF receiver requiring 60dB rejection in the adjacent sideband needs -94 dBc/Hz at a 500Hz offset. The use of extremely high performance filters in the receiver can be completely negated if the phase noise is poor. For example, a receiver using a KVG XF9B filter with a rejection in the unwanted sideband of 80dB at 1.2KHz, would require a local oscillator with -114dBc/Hz phase noise at 1.2KHz if the filter performance was not to be degraded.

To put these levels in perspective, relatively few signal generators are adequate to the task of being the LO in such a system. For example, "Industry Standards" like the HP8640B are not specified to be good enough: neither are the HP8642, Marconi 2017/2018, or Racal 9082, all of which are modern, high performance signal generators.

All this suggests that is is very easy to over-specify a receiver in terms of selectivity, and simple synthesisers are not necessarily ideal in all situations.

The ability of the receiver to receive weak wanted signals in the presence of strong unwanted signals is therefore determined not only by the intermodulation capabilities of the receiver, but by phase noise and filter selectivity.

The usual approach to high performance syntheais has used multiple loops for good close in performance. Notable exceptions are those equipments using factional N techniques with a single loop. Nevertheless, such equipments not generally specified as highly as multi-loop synthesisers.
A vital part of the synthesisers is still the low noise VCO, for which many approaches are possible. This VCO performance should not be degraded by the addition of the synthesiser: careful choice of technologies is therefore essential. For example, Gallium Arsenide dividers are much worse in phase noise production than silicon, and amongst the silicon technologies, TTL is better than ECL.

From equation (1)

$$D.R. \quad \frac{2}{3}(I_{p3} - N.F.) \text{ dB}$$

where I_{p3} = input intercept point dBm
NF = noise floor dBm

The phase noise governed dynamic range is given by $DR_\phi = P_n + 10 \log_{10} B$
Db-tq2

Where P_n is the phase noise spectral density in dBc/Hz at any offset
B is the IF bandwidth in Hz.

(N.B. This is not quite correct if B is large enough such that noise floor is not effectively flat inside the IF bandwidth).

Ideally the ratio $\frac{DR_{IM}}{DR_\phi}$ should be 1

RESULTS AND DISCUSSION

The Class C amplifier constructed has a power gain of 10dB at 100 watts output and about 7 dB at 127 watts. The measured 3 dB bandwidth ΔF was 8.0 MHz, which is in very good agreement with the theoretical value of 8.1 MHz evaluated from the formula

$$\Delta F = F\,(\sqrt{2} - 1)^{1/2}\,/Q \quad (9)$$

where F is the operating frequency. The second solution for the strip length (ℓ_2) was discarded due to its impractical dimension. One means of reducing the required strip length consists in increasing Z_O, which implies the reduction of the strip width. As an example, halving the ouptput strip width leads to a required strip length of only 6.8 cm instead of the actual 11.4 cm. This can be achieved in detriment to the current handling capacity of the strip.

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AN-419 Motorola semiconductor Products Inc., Phoenix, Arizona, U.S.A.

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Manufacturer : Keene Corporation, Chase-Foster Division, Newark, Del. 19711, U.S.A.

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in a well designed receiver - i.e., the dynamic range limited by phase noise is equal to the dynamic range limited by intermodulation.

Certain aspects of low noise synthesiser design have been touched upon and Ref. 6 provides further information.

The performance of a receiver in terms of its capabilities to handle input signals widely ranging in input level is dependent upon the receiver capability in terms of intermodulation and phase noise. Neglect of either of these parameters leads to performance degradation, and it has been shown that specifications are not only often difficult to meet, but sometimes contradictory in their requirements.

Ref.1 Broadband Amplifiers Application Notes Appendix 3.
Plessey Semiconductors, Cheney Manor, Swindon, England.

Ref.2 Ideal Limiting Part 1 (George S.F. and Wood 3.W., Washington D.C.:
U.S. Naval Research Laboratory AD266069, 2nd October, 1961.

Ref.3 The SL6440 High Performance Mixer, P.E. Chadwick,
Wescon Proceedings Session 24, Mixers for High Performance Radio
Published by Electronic Conventions Inc, 999 North Sepulveda Blvd.
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Ref.4 High Performance Integrated Circuit Mixers, P.E. Chadwick.
Clark Maxwell Commemorative Conference on Radio Receivers and
Associated Systems, Leeds 1981. Published by I.E.R.E.,
99 Gower Street, London, WC1e 6AZ. Conf. Pub. 49.

Ref.5 The SL6440 High Performance Mixer, P.E. Chadwick.
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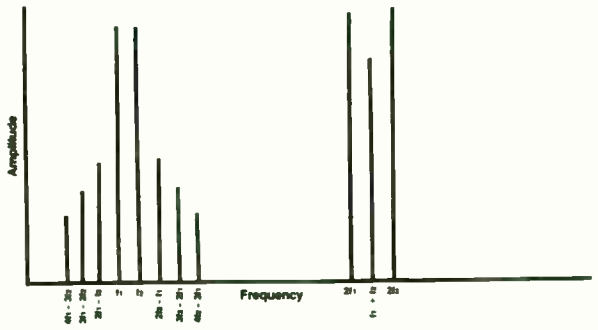
Ref6. Frequency Synthesisers. Vadim Manassewitsch, Wiley & Sons, 1980
ISBN 0-471-07917-0.



Intermodulation Products
fig 1

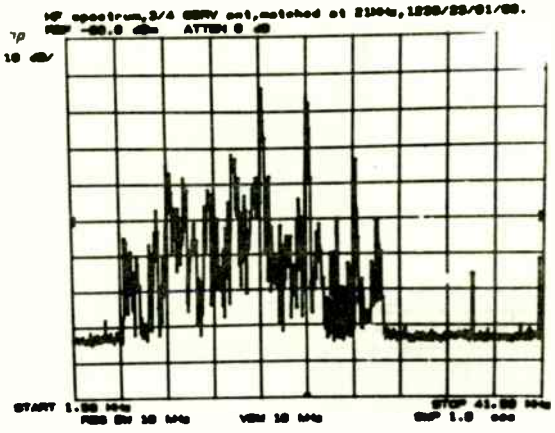


fig 2

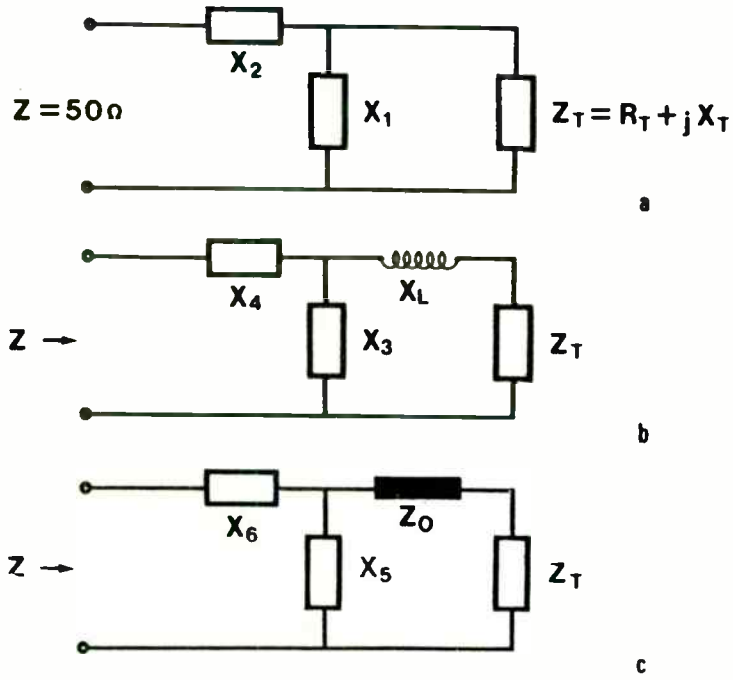


Figure 1. Basic network using X_1, X_2 to match the input/output impedance Z_T of a transistor to 50 Ω (a). Matching network incorporating an inductance to reduce harmonic frequencies (b). Inductance replaced by a microstripline with a well defined Q at high frequencies.

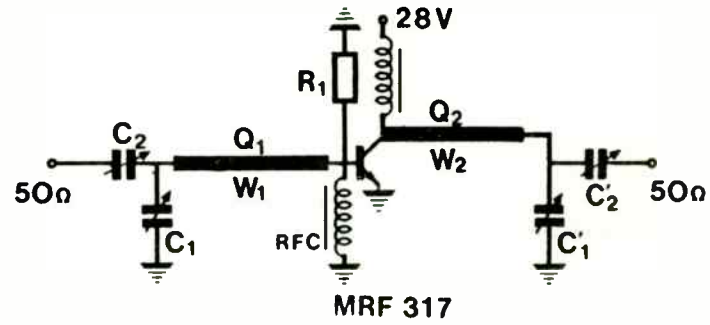


Figure 2. Typical Class C amplifier incorporating microstripline in the input and output matching network. Matching capacitors C are functions of the chosen Q of the network as tabulated in Tables I and II. R_1 (18 Ω) was inserted to improve transient response. It can be omitted for CW operation.

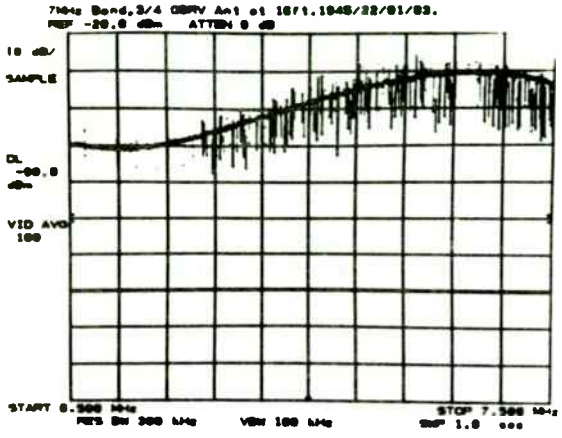


fig 3

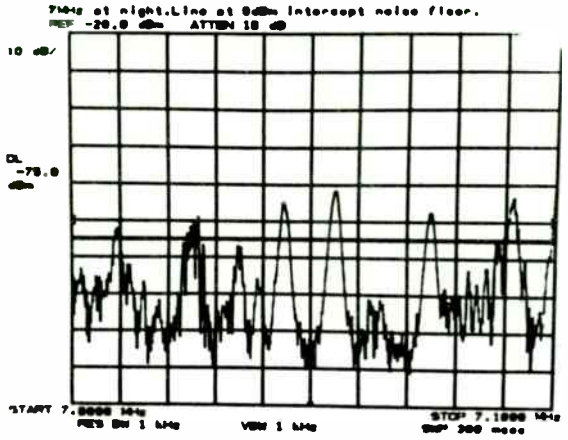


fig 5

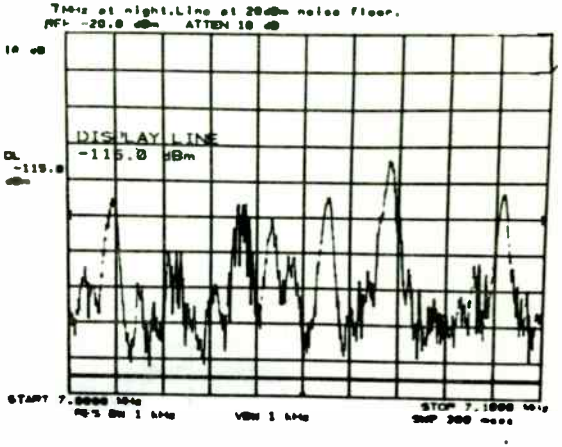
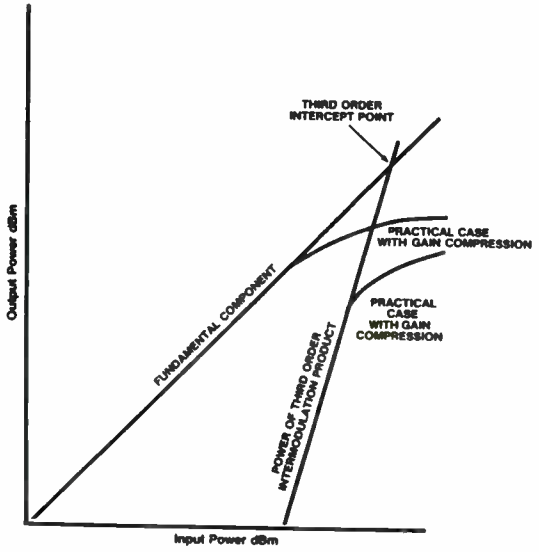


fig 7



Third Order Intercept fig 4

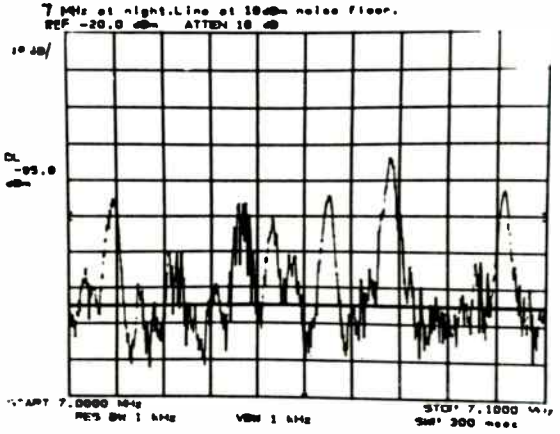


fig6

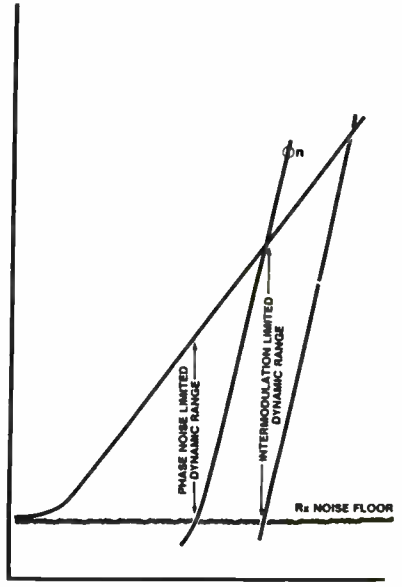


fig 8

Q	ℓ_1(cm)	C_1(pF)	C_2(pF)	R_{in}	X_{in}
28_{max}	15.2	18.8	4.1	1.53	43.30
20	7.3	47.5	7.9	0.90	18.05
13	4.2	82.7	14.8	0.81	10.59
10	3.0	112.8	25.2	0.79	7.95
	ℓ_2(cm)				
20	23.1	6.4	3.1	5.2	103.7
13	26.2	2.7	2.9	13.6	176.1
10	27.4	1.3	2.9	23.4	233.8

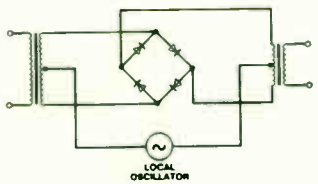
Table I. Transistor Base Lead Width = 5.2 mm, Z_O = 43 Ω

Q	ℓ_1(cm)	C_1(pF)	C_2(pF)	R_{in}	X_{in}
15_{max}	16.4	14.0	5.2	3.53	52
13	11.4	24.8	7.3	2.4	31.3
12	10.1	29.2	8.4	2.2	26.9
10	8.0	39.2	11.1	2.0	20.0
		ℓ_2(cm)			
13	21.3	7.3	4.2	6.6	86.3
12	22.6	5.8	4.1	8.4	100.4
10	24.7	3.6	3.9	13.2	131.8

Table II. Transistor Base Lead Width = 3.935 mm, Z_O = 57 Ω

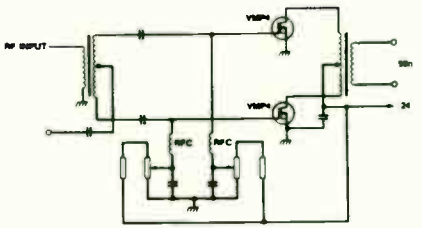
CAPTION. Tables I and II

Microstrip lengths (ℓ_1, ℓ_2) as a function of Q. R_{in} and X_{in} are the real and imaginary parts of the line input impedance. For Q less than Q_{max}, there existe two values of ℓ, R_{in} and X_{in}. C_1 and C_2 are the corresponding matching capacitances required to match R_{in} and X_{in} to the 50 Ω source or load impedance.



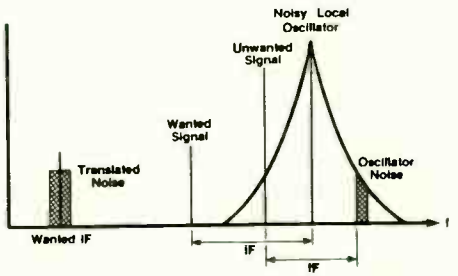
Diode ring

fig 9



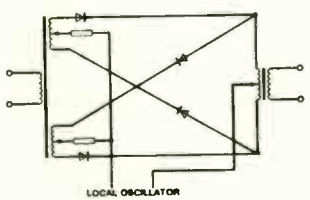
VMOS mixer

fig 12



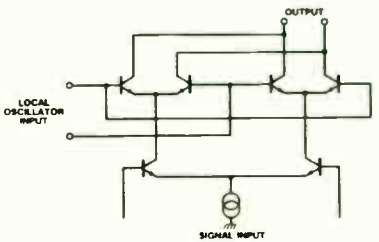
RECIPROCAL MIXING

fig 15



Resistive loaded high intercept point mixer

fig 10



The transistor tree

fig 13

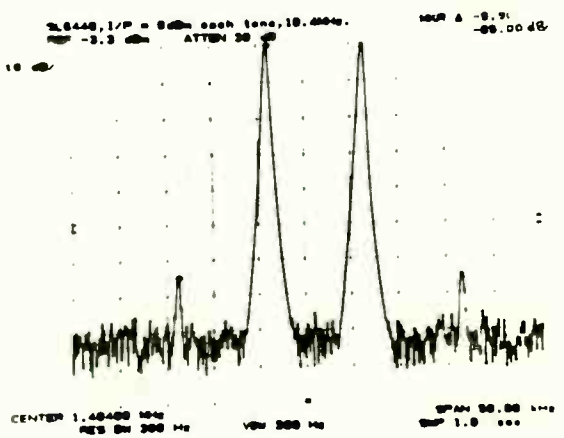
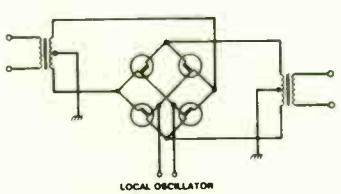
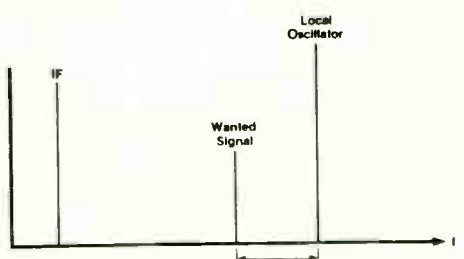


fig 16



Quad MOSFET commutative mixer

fig 11



Superhet mixing

fig 14

INTERMODULATION

Intermodulation is caused by odd order curvature in the transfer characteristic of a device. If two signals F_1 and F_2 are applied to a device with third order term in its transfer characteristic, the products are given by:

$(\text{Cos}\, F_1 + \text{Cos}\, F_2)^3 = \text{Cos}^3F_1 + 3\text{Cos}^2F_1\text{Cos}F_2 + 3\text{Cos}^2F_2\text{Cos}F_1 + \text{Cos}^3F_2$

from the trig identities Cos^3A, Cos^2A and CosACosB, this is
$\frac{1}{4}\text{Cos}^3F_1 + \frac{1}{4}\text{Cos}F_1 + 3/2\text{Cos}^2F_1\text{Cos}F_2 + 3/2\text{Cos}F_1\text{Cos}^2F_2 + \frac{1}{4}\text{Cos}F_2 + \frac{1}{4}\text{Cos}^3F_2 + \frac{1}{4}\text{Cos}F_2$
(where $F_1 = A$ and $F_2 = B$) Neglecting coefficients, the terms $\text{Cos}^2F_1\ \text{Cos}F_2$ and $\text{Cos}F_1\ \text{Cos}^2F_2$ are equal to

$\text{Cos}(2F_1 + F_2) + \text{Cos}(2F_1 - F_2)$ and
$\text{Cos}(2F_2 + F_1) + \text{Cos}(2F_2 - F_1)$

By inspection, it may be seen that frequencies of F_1, F_2, $3F_1$, $3F_2$, $(2F_1 + F_2)$ and $(2F_2 \pm F_1)$ are present in the output. Of these, only $2F_2 - F_1$, and $2F_1 - F_2$ are close to wanted frequencies F_1 and F_2.

The application of three signals F_1, F_2 and F_3, produces a similar answer, in that the resulting products are:

$3F_1, 3F_2, 3F_3, F_1 + F_2 + F_3, F_1 + F_2 - F_3, F_1 - F_2 + F_3, F_1 - F_2 - F_3, F_2 - F_1 + F_3, F_2 - F_1 - F_3, -F_1 - F_2 - F_3, -F_1 - F_2 + F_3$ in addition to the products

$2F_1 \pm F_2, 2F_2 \pm F_1, 2F_2 \pm F_3, 2F_3 \pm F_2, 2F_1 \pm F_3, 2F_3 \pm F_1$

if a greater number of signals are applied such that the input may be represented by :

$\text{Cos}F_1 + \text{Cos}F_2 + \text{Cos}F_3 + \text{Cos}F_4 \ldots \text{Cos}\, F_n$

The results of third order curvature can be calculated from:

$(\text{Cos}F_1 + \text{Cos}F_2 + \text{Cos}F_3 + \text{Cos}F_4 \ldots \text{Cos}F_n)^3$

This expansion produces terms of

$\text{Cos}(F_1 \pm F_2 \pm F_3)$, $\text{Cos}\,(F_1 \pm F_2 \pm F_4)$, $\text{Cos}\,(F_1 \pm F_2 \pm F_n)$ etc from which it can be seen that the total number of products is:

$$\frac{n!}{3!(n-3)!} = 4 \times 1/6n\,(n-1)\,(n-2)$$

(The factor of 4 appears because each term has four possible sign configurations i.e. $\text{Cos}(F_1 + F_2 + F_3)$, $\text{Cos}\,(F_1 + F_2 - F_3)$ etc) This agrees with RefA1.

By a similar reasoning, n signals produce:

$2n(n-1)$ products of the form $(2F_1 \pm F_2)$ $(2F_2 \pm F_1)$ etc and n 3rd harmonics.

Thus the total number of intermodulation products produced by third order distortion is:
$n + 2n(n-1) + 2/3n(n-1)(n-2)$ (1)

Reduction of the input bandwidth of the receiver modifies this. Consider, for example, a receiver with sub-octave filters, rather than the "wide-open" situation analysed above. In this case, the third harmonics produced by any input signals will not fall within the tune band, as will some of the products such as $F_1 + F_2 + F_3$, $F_1 - F_2 - F_3$, etc. In this case, the total number of intermodulation products is reduced. There are only three possible sets of products of the form $F_1 \pm F_2 \pm F_3$, i.e. $F_1 + F_2 - F_3$, $F_1 - F_2 + F_3$ and $F_3 - F_1 - F_2$ which can give products within the band. Note that for products to be considered, they must have an effective input frequency at the receiver mixer equivalent to an on-tune desired signal. In addition, products of the form $2F_1 + F_2$, $2F_2 + F_1$ etc are again out of band. Thus half of the $2n(n-1)$ products of this class are not able to cause problems and the total number of products to be considered is now:-

$n(n-1) + \frac{1}{2}n(n-1)(n-2)$ (2)

This result does not agree with Barrs (Ref A2) who uses the results in (1). The results in (2) are an absolute worst case, insofar as a number of the intermodulation products are out of band.

(For the purposes of this analysis, IMD in a mixer is assumed to produce an "on tune" signal. Thus not all the possible intermodulation frequencies appearing in a half octave bandwidth will be able to interfere).

The same arguments apply to narrower front end bandwidths. However, the narrower the front end bandwidth, the higher is the probability that the distribution of signals will produce I.M.D.

SORF - AN RF LOW POWER SMD ALTERNATIVE PACKAGE

A Paper for RF Technology Expo 86
by
Harry J. Swanson
Motorola Semiconductors

INTRODUCTION

This paper introduces the SORF$_{TM}$ (Small Outline RF) package which has the same mechanical case outline as the familiar SOIC SO8 (see Figure 1). In this paper the SORF package is described and its performance is compared to the Macro-X $_{TM}$ package. Thermal performance is presented emphasizing the performance in a still air 25^{o} C ambient environment. Specific characteristics of the SORF package are discussed. These outstanding package characteristics offer the RF design engineer an alternative to the conventional RF packages (such as the TO39, TO-92, SOT89 and Macro-X) and provide a true SMT package for RF low power transistors.

PACKAGE DESCRIPTION

The SORF transistor is composed of the leadframe, the transistor die, the interconnect wires and the epoxy molded body (see Figure 2). The SORF leadframe is copper and it is designed to provide an excellent RF package. In order to enhance the RF gain and broadband performance, the corner leads are internally connected through the leadframe to provide low common lead inductance and to reduce package parasitics. On one side of the package the two middle leads are the input leads and on the opposite side the two middle leads are the output leads which extend to the collector pad of the leadframe where the transistor die is mounted by forming a gold-silicon eutectic die bond. The die is connected to the base and emitter leads using 1.5 mils diameter gold wire.

Symmetry of the layout allows for parallel wirebonding and for equal length base and emitter wires. To enhance the RF performance the wire loop lengths and loop heights are minimized. The leadframe strip is then epoxy molded to fully encapsulate each individual leadframe on the strip. After the mold process, the leadframe is tin plated. Next, the individual RF transistors are trimmed from the leadframe strip and the leads are formed in the gull wing format. Figure 1 details the SORF package dimensions and mechanical tolerances.

SORF and **Macro-X** are trademarks of Motorola, Inc.

products outside the band. For example, a receiver with ±2.5% front end bandwidth tuned to 10MHz will accept signals in a band from 9.75 to 10.25MHz. Signals capable of producing a product of the form $2F_1$-F_2 must have one of the signals (F_1 or F_2) in the band 9.875 - 10.25 for a product to appear on tune. Thus the two signal apparent bandwidth is less than would be expected. Similar constraints apply to the $F_1 + F_2$-F_3 product.

Similar arguments apply to other orders of curvature. Second order curvature, for example, will not produce any products in band for input bandwidths of less than 2:1 in frequency ratio.

The actual levels of intermodulation produced can be predicted from reference A1. In practice, the situation is that the input signals to a receiver are rarely all of equal unvarying amplitude and assumptions are made from the input intercept points and the input signal density.

If a series of amplitude cells are established for given frequency ranges, such as that in table 1, then a prediction of the number of intermodulation products for any given number of input signals and amplitudes may be obtained, either from equation 1 or 2 (as applicable) or from RefA1 (for higher orders). Where the input bandwidth of the receiver is deliberately minimised, the maximum cell size in the frequency domain should be equal to the input bandwidth.

The total input power in each cell is

n Pav

where n is the number of signals and Pav is the average power of each signal.

A worst case situation is to assume that all signals in the cell are equal to the cell upper power limit boundary, e.g. if the cell amplitude range is from -40 to -30dBm, then an assumption that all signals in this cell are at -30dBm is a worst case.

If, however, it is assumed that signals will have a Gaussian distribution of input levels within a cell, then the total input power becomes:

$Pt = 0.55n\,P$

where Pt is the total power
n is the number of signals
P is the power level at the upper boundary of the cell

Because the total IMD power is the sum of all the IMD powers, the average input power is

$$Pav = \frac{0.55nP}{n}$$

The IMD power produced by third order curvature is:-

$10\log_{10}[\frac{1}{3}n(2n^2 + 1)]$ Antilog 1/10 [Pav-3(I_3-Pav)]dBm
where P_{IM} is the total power of the intermodulation products
I_3 is the third order input intercept point

Because the coefficients of the amplitudes of the intermodulation products are (depending on product)

$a^3, a^2b, ab^2, abc, b^3$

where a, b and c are approximately equal, the use of a^3 as the general coefficient is justified.

From equations 1 or 2 and 3, the total I_{MD} power and number of products may be calculated. As "n" increases in number, the number of products will mean that the resultant I_{MD} tends more to a noise floor increase in the receiver, thus reducing the effective sensitivity.

The amount of this degradation is such that the noise floor is:

$$\frac{\frac{1}{3}(n.0.55P)^3}{I_3} \cdot \frac{I_3}{(fmax\text{-}fmin)} \cdot \Delta f$$

where (fmax-fmin) is the bandwidth prior to the first intermodulating stage. Δf is signal bandwidth in a linear system.

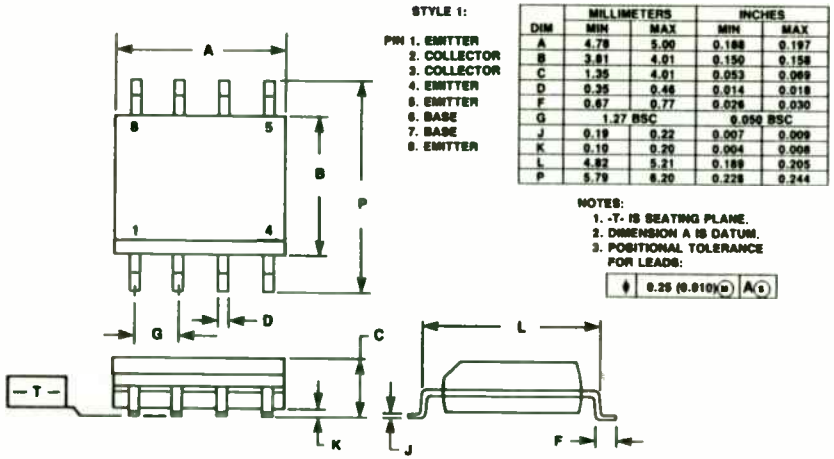
The Gaussian Factor of 0.55 is somewhat arbitrary, since errors in this assumption are cubed.

The intermodulation Limited Dynamic Range is

$\frac{1}{3}(I_3 + 174 - 10\log_{10}\Delta f - NF)$

where NF is the Noise Figure in dB.

The effects of Reciprocal Mixing are similar, except that signals may be taken one at a time. The performance is affected by the frequency separation between an "off-tune" interfering signal



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.78	5.00	0.188	0.197
B	3.81	4.01	0.150	0.158
C	1.35	4.01	0.053	0.069
D	0.35	0.48	0.014	0.018
F	0.67	0.77	0.026	0.030
G	1.27 BSC		0.050 BSC	
J	0.19	0.22	0.007	0.009
K	0.10	0.20	0.004	0.008
L	4.82	5.21	0.189	0.205
P	5.79	6.20	0.228	0.244

FIGURE 1 - SORF CASE OUTLINE DRAWING

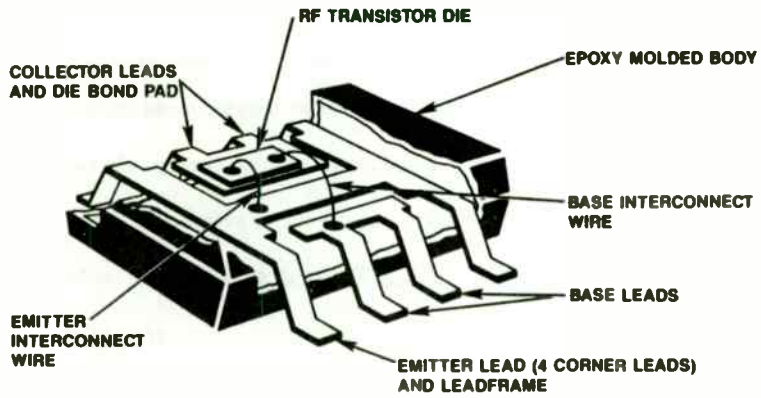


FIGURE 2 - CUTAWAY VIEW OF THE SORF TRANSISTOR

RECENT SORF INTRODUCTIONS

Two RF transistors introduced in 1Q86 are (1) the MRF8372, a 750 mW, 12.5 Vdc, 10 dB gain UHF/800 MHz Class C predriver amplifier and (2) the MRF5812, a 10 Vdc V_{CE}, 50mA I_C, 15 dB G_{NF}(typical), 2.0 dB NF(typical), 500MHz Class A low noise amplifier. These transistors' counterparts in the Macro-X are, respectively, the MRF837 and the MRF581. Table I compares the two transistors' performances in the SORF and the Macro-X packages. Note that the SORF package offers comparable performance to its Macro-X counterpart.

TABLE I - COMPARISON OF THE SORF TO THE MACRO-X

MRF8372 (SORF) VS MRF837 (MACRO-X)						
POWER DISSIPATION MRF8372 @ T_C = 75°C, DERATE ABOVE 75°C MRF837 @ T_C = 50°C, DERATE ABOVE 50°C	P_{out} (f = 870 MHz, V_{CC} = 12.5 Vdc)	G_{pe}min	G_{pe}typ	$N_C$min	$N_C$typ	
	WATTS	mW	dB	dB	%	%
MRF8372	1.5	750	8.0	10	50	60
MRF837	2.5	750	8.0	10	50	60
MRF5812 (SORF) VS MRF581 (MACRO-X)						
POWER DISSIPATION MRF5812 @ T_C = 75°C, DERATE ABOVE 75°C MRF581 @ T_C = 50°C, DERATE ABOVE 50°C	f_t (I_C=50mA)	G_{NF}min	G_{NF}typ	NF max	NF typ	
	WATTS	GHz	dB	dB	dB	dB
MRF5812	1.5	6.0	13	16	3.0	1.9
MRF581	2.5	5.0	13	16	3.0	1.9

and an "on-tune" wanted signal unless the separation is such that the oscillator noise floor has been reached. Here again, reduction of front end bandwidth reduces the number of signals.

Generally speaking, the effects of reciprocal mixing are limited to close in effects - say within ± 50KHz, unless very poor synthesisers are used.

The response at some separation f_o from the tune frequency is:$(L - 10_{log}\ 10\ \Delta f)$ dB

where L is phase noise spectral density in dBc/Hz and Δf is the IF bandwidth.

This assumes that the spectral density does not change within the receiver bandwidth: Ref1 shows this to be generally applicable for narrow bandwidths.

The intermodulation free dynamic range is defined as:

$\frac{2}{3}[I_3 - \text{noise floor}] = \frac{2}{3}[I_3 + 174 - 10_{log\ 10}\Delta f\text{-}NF]$ dB

where I_3 is the input 3rd order intercept point in dBm
NF is the noise figure in dB
Δf is the IF bandwidth in Hz

It has been claimed (Ref A3) that there is 6dB rejection of phase noise in diode commutative mixers. Thus the relationship between IMD and phase noise can be expressed as:

IMD dynamic range = phase noise dynamic range + 6dB
$= (L\text{-}10_{log\ 10}\Delta f) + 6$dB

Thus at any offset, it is important to ensure that the two dynamic ranges are approximately equal if performance is not to be compromised.

A receiver for example with an input intercept point of + 20dBm and input signals of -30dBm will will produce an IMD product at -130dBm which, for an HF receiver with a noise factor of 8dB, will be just above the noise floor, in an SSB bandwidth. The noise floor of the L.O. will need to be such that the noise is at -133dBm if degradation is not be occur, and this will be produced by a noise floor of -137dBc/Hz in the synthesiser at the frequency separation of the signals in question. Thus the high intermodulation performance may well be compromised by poor phase noise.

REFERENCES

A1 A Table of Intermodulation Products
JIEE (London) Part III
31-39 (Jan 1948) C.A.A. Wass.

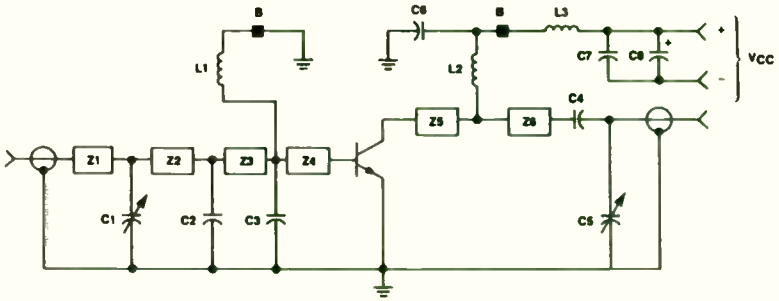
A2 A Re-appraisal of H.F. Receiver Selectivity
R.A. Barrs
Clerk Maxwell Commemorative Conference in Radio Receivers and Associated Systems, Leeds 1981. pp 213-226, Published by IERE, 99 Gower Street, LONDON, WC1E 6AZ.
Conference Publication no. 50 ISBN 0 903 748 45 2

MRF5812

The MRF5812 is fully characterized in a manner similar to the MRF581. The Transistor is RF guaranteed for 13 dB GNFmin (minimum gain at noise figure) and 3.0 dB NFmax (maximum noise figure) at 500 MHz. The transistor is characterized for S parameters and noise figure versus frequency and noise figure versus I_C (collector current). Typical noise figure performance and typical S parameters are listed in the transistor data sheet. These parameters are almost identical to the those of the MRF581.

MRF8372

The MRF8372 is tested to guaranteed RF performance at 870 MHz for 750 mW Pout (power output), 8 dB Gpe (common emitter power gain), and 50% Nc (collector efficiency) in a fixed tuned broadband test fixture which is pictured in the data sheet (see Figure 3 for the corresponding circuit schematic). Typical RF performance in the broadband test fixture is plotted in Figure 4. The test fixture demonstrates the ability to use the transistor in broadband applications with excellent performance. The MRF8372 is fully characterized in a manner similar to the MRF837 for typical performance and device impedance in the 800 MHz band (see Table II). Input and output impedance parameters show excellent low Q which enhances the ability to match the device for broadband operation.



C1, C6 — 0.8–8.0 pF JOHANSON GIGATRIM
C2, C3 — 10 pF CERAMIC CHIP CAPACITOR
C5 — 91 pF CLAMPED MICA, MINI-UNDERWOOD
C4 — 47 pF CERAMIC CHIP CAPACITOR
C7 — 91 pF CLAMPED MICA, MINI-UNDERWOOD
C8 — 1.0 μF 25 V TANTALUM
B — BEAD, FERROXCUBE 56-590-65/3B

L1, L2 — 4 TURNS, #21 AWG, 5/32" ID
L3 — 7 TURNS, #21 AWG, 5/32" ID
Z1, Z2 — 1.0" × 0.079" MICROSTRIP, Z_0 = 50 Ohms
Z3 — 0.25" × 0.079" MICROSTRIP, Z_0 = 50 Ohms
Z4 — 0.15" × 0.079" MICROSTRIP, Z_0 = 50 Ohms
Z5 — 0.30" × 0.079" MICROSTRIP, Z_0 = 50 Ohms
Z6 — 1.63" × 0.079" MICROSTRIP, Z_0 = 50 Ohms
PCB — 1/32" GLASS TEFLON, ϵ_r = 2.56

FIGURE 3 - 800/900 MHz BROADBAND CIRCUIT SCHEMATIC

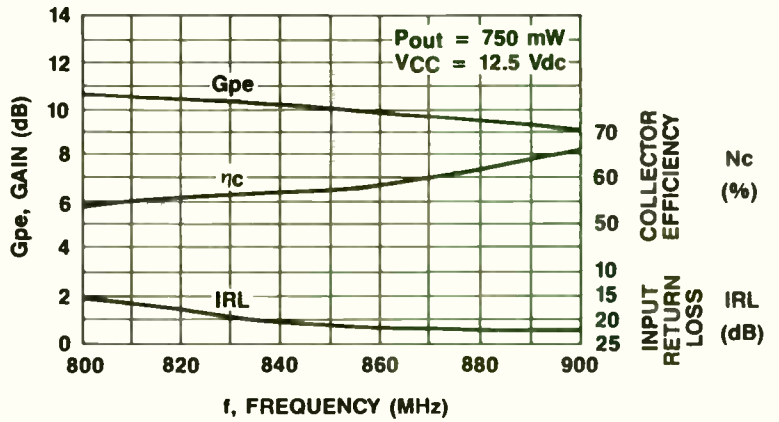


FIGURE 4 - 800/900 MHz BROADBAND PERFORMANCE

ADVANCES IN SINGLE CHIP FREQUENCY SYNTHESISERS

P. E. Chadwick
Plessey Semiconductors
Cheney Manor
Swindon
SN2 2QW

Single Chip Frequency Synthesiaers using Bipolar Technology have been available for some years. Introduced originally for T.V. tuning, devices for broadcast radio were rapidly provided and Ref. 1 provides information on the earliest of these TV devices. Developments have now pushed the upper operating frequency to over 2 GHz, but, nevertheless, these devices have hiatorically been limited to the consumer market for a number of reasons. These are:-

1. Power Consumption (150-200 mW)
2. Phase Comparison Frequency

In T.V. applications, the use of a 62.5 KHz step size for fine tuning allows the use of a fixed prescaler at the front end of the chip - Fig. 1. To achieve the small channel step size used in communications, the phase comparison frequency must be reduced to a few hundred hertz, and thus the device is no longer attractive. Nevertheless, the well tried technology of an ECL prescaler and I^2L low frequency logic has certain merits, making integration onto one chip feasible and attractive. However, existing IC processes demand current levels such that CMOS technology becomes attractive if the frequency response performance can be achieved, and recent advances have now made this possible.

The 2 micron technology introduced by Plessey has been used to introduce a new family of frequency synthesiser parts operating at VHF, with every promise of extension to the UHF band. Before describing this new family in detail, some review of existing practice is justified.

As is widely known, it is desirable to keep the reference frequency in a single loop synthesiser as high as possible consistent with multiplied reference phase noise. The use of fixed prescaling (Fig. 2) is therefore limited to wide channel spacings or narrow loop bandwidths, while alternative methods of mixing (Fig. 3) or multi-modulus division (Fig. 4) provide the majority of answers to this problem. Where multi-modulus division is used, the choice of modulus is dependent upon a number of constraints, viz:

1. Minimum divide ratio is N^2-N, where moduli are N, N+1
2. Loop delay must not exceed $\frac{N}{Fin}$
3. $\frac{Fin}{N}$ must be less than the maximum count frequency of the control circuit counters A and M

In addition, the choice of various values for N can make the programming of the synthesiser easier, insofar as, for example, the use of a 40/41 divider provides "nice" programming for a 25 KHz spacing system. The increasing use of serial data bus control with microprocessors has produced some changes in outlook here, however, as even the simplest radios now seem to have a microprocessor included.

It is in the case of the hand held radio that power consumption is especially important. Thus the pressure has been placed on semiconductor manufacturers to reduce the current drains of ICs and in the case of the VHF synthesiser, it is practicable to build a complete synthesiser drawing some 10-12 mA at 5 Volts. This is shown schematically in Fig. 5, where the power consumptions are about 4 mA each for the bipolar prescaler and the CMOS control chip.

The advances in small geometry CMOS technology have made it practical to integrate a CMOS prescaler with the CMOS control chip - Fig. 6. Amongst the advantages that accrue are the fact that there are no logic level output swings at the divider output frequency to be considered, which can require relatively large amounts of current - some 0.5 mA or so just to charge and discharge the capacitance of the transistor, bond pad, package and a gate input.

TABLE II - Z_{IN} AND Z_{OL} VERSUS COLLECTOR VOLTAGE, INPUT POWER AND OUTPUT POWER

f FREQUENCY MHz	Z_{in} OHMS		Z_{OL}* OHMS	
	V_{CC} = 7.5 V	V_{CC} = 12.5 V	V_{CC} = 7.5 V	V_{CC} = 12.5 V
	P_{in} = 150 mW	P_{in} = 100 mW	P_{out} 806 MHz = 820 mW P_{out} 870 MHZ = 635 mW P_{out} 960 MHz = 530 mW	P_{out} 806 MHz = 1.05 W P_{out} 870 MHz = 855 mW P_{out} 960 MHz = 590 mW
806	9.0 + j1.9	4.0 + j1.2	24.7 - j19.2	20.9 - j31.0
870	5.2 + j3.5	8.0 + j1.9	36.9 - j20.5	32.1 - j26.9
960	6.8 + j4.0	8.1 + j2.5	39.3 - j18.5	36.3 - j25.7

*Z_{OL} = CONJUGATE OF THE OPTIMUM LOAD IMPEDANCE INTO WHICH THE DEVICE OUTPUT OPERATES AT A GIVEN OUTPUT POWER, VOLTAGE, AND FREQUENCY.

SORF THERMAL PERFORMANCE

The SORF package offers excellent thermal performance. Thermal analysis determined that the thermal resistance of the SORF package is almost as low as that of the Macro-X package. The IR scans are performed under RF operating conditions and mounted in a manner similar to a surface mount application in which a heatsink is not employed and no considerations are made to provide a good case to heatsink interface. The transistor sustains up to 1.5 watts P_D, power dissipation which raises the T_J, die junction temperature to 150 °C at T_A = 25 °C.

Summary of IR Scan Analysis

Table III shows that the Θ_{JL} ranges from 43.4 to 47.1 °C/W and Θ_{JA} ranges from 82.8 to 87.7 °C/W at P_D ~ 1.5 watts, T_L = 80 °C, and T_A = 25 °C.

TABLE III - SUMMARY OF SORF IR SCAN ANALYSIS

IR SCAN DESCRIPTION	FREQUENCY = 870 MHz; SEE RF FUNCTIONAL CIRCUIT SCHEMATIC												
	P_{OUT}	P_{IN}	V_{CC}	I_C	P_D	T_J HS	T_J AV	T_L	T_A	θ_{JL} HS	θ_{JL} AV	θ_{JA} HS	θ_{JA} AV
	W	mW	Vdc	mA	W	°C	°C	°C	°C	°C/W	°C/W	°C/W	°C/W
SCAN #2 BIAS COND. 3	1.1	405	15	135	1.33	142	139.7	77	25	48.9	47.1	88	86.2
SCAN #2 BIAS COND. 4	1.18	460	15	146	1.47	153.5	150.8	82	25	49.6	46.8	87.4	85.6
SCAN #3 BIAS COND. 2	1.11	415	15	135	1.33	144	141.7	84	25	45.1	43.4	99.5	87.7
SCAN #4 BIAS COND. 1	1.14	410	15	142	1.4	147	146.3	83	25	45.7	45.2	87.1	86.6
SCAN #5 BIAS COND. 1	1.13	415	15	142	1.42	142	141.5	80	24	43.7	43.4	83.1	82.8

The following thermal resistances can be justified for the SORF transistor:

Θ_{JL} = 45 °C/W at T_L = 80 °C

Θ_{JA} = 85 °C/W at T_A = 25 °C

where P_D = 1.5 watts and T_J = 150 °C.

Power derating curves are shown for Θ_{JL} and Θ_{JA}, respectively (see Figures 5 and 6).

The Plessey Semiconductors NJ88C30 family represent a new generation of CMOS synthesiser parts. The prescaler is integrated onto the chip, and operation to 200 MHz is guaranteed in the NJ88C30. Other members of the family have been optimised for broadcast radio use (the NJ88C31) and here arrangements have been made to bypasa the internal 2 modulus prescaler when operating in the medium wave (520-1600 KHz) band, (Figs. 6 and 7).

These devices employ serial data programming; the commercial demand for full parallel programming is now limited to applications requiring fast frequency changing, and, in any case, in single loop synthesisers, loop dynamics are generally the largest part of the lock-up time when low (<50 KHz) phase comparison frequencies are used.

The NJ88C30 consists of an input amplifier, 2 modulus divider (15/16 division) A and M counters and a reference oscillator and divider chain. The reference divider chain is not fully programmable, but provides a number of reference frequency possibilities dependent upon the crystal oscillator frequency. In common with other CMOS oscillators using invertors, the stability is adequate for the majority of commercial applications, but is not in the highest class: typically, some 1 ppm of drift over the temperature range can be attributed to change in phase shift through the device when operating at 10 MHz. The divider chains feed the digital phase detector with outputs suitable for use in a standard charge pump low pass filter. As mentioned earlier, and shown in Fig. 7, the NJ88C31 has some changes to make it more applicable to broadcast radio applications.

In these applications, the upper frequency limit of the input divider need only be some 120 MHz, while the number of reference frequency division ratios is limited, spacings of 4.5, 5, 9, 10, 12.5 and 25 KHz sufficing for the MF and VHF broadcast bands. The provision of a 4.5 MHz output to drive a microprocessor clock input, and a standby current of under 2 mA minimise power drain requirements when the radio is switched off, even though the crystal oscillator is still required for the clock function in some radio receivers.

Although the use of analogue phase detectors has been advised for some years in order to remove the effects of the dead zone in digital phase detectors, this has not proved necessary in many synthesisers, adequate performance being obtained from the classical "charge pump" detector. An area in which the L.F. phase noise introduced by the charge pump detector is in the reception of AM stereo signals, especially on the Motorola CQAM system. However, calculations show that the spurious phase modulation introduced is about 0.03 degrees - far enough down to produce inaudibility. Note that signal to noise ratios in car radios are often subject to "specmanship" - not even a Rolla-Royce will allow the use of a 70 dB signal to noise ratio! In any case, the phase variation produces only "wandering" of the stereo image.

The difficulty in the use of the analogue phase detector lies in addressing the requirements of a transmitter synthesiser. Where the synthesiser is directly modulated, the effects of modulation at a frequency outside the loop bandwidth is to exercise the phase detector by an amount dependent upon the deviation. When large (50-75 KHz) deviations are required, a high gain analogue phase detector may well be driven into limiting, and the production of spurious outputs at the reference frequency increased.

Sonarbuoys have such modulation requirements: the reproduction of an audio band from 5 Hz to 50 KHz with such deviations is desirable, and the use of an analogue phase detector is not desirable in such a synthesiser, unless a much higher reference frequency is used. Performance of analogue integrated phase detectors at this much higher frequency (375 KHz) leaves much to be desired: the 2 micron CMOS geometry is still capable of providing adequate performance, while the market size (some 750,000 p.a. in the Western World) is attractive.

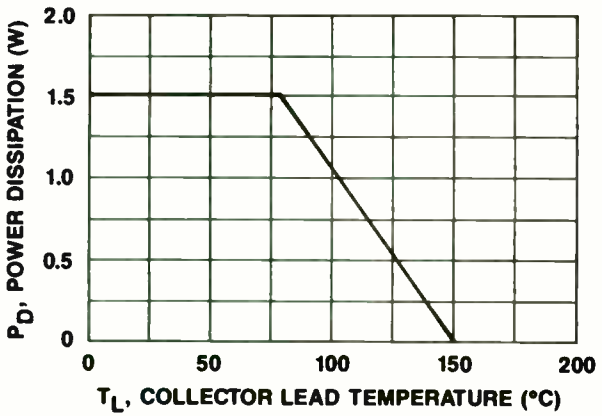


FIGURE 5 - POWER DERATING, Θ_{JL}

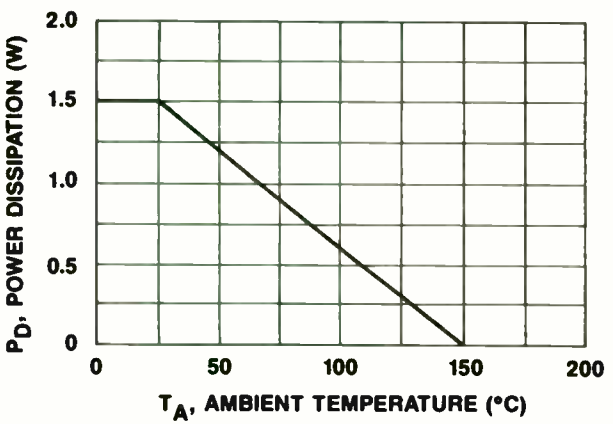


FIGURE 6 - POWER DERATING, Θ_{JA}

IR Scan Setup

The IR scan setup consisted of the following:

1. Radiometric Microscope Model RM-2A, Barnes Engineering,
2. Regulated Power Supply Model LK 342A FM,
3. Voltmeters and Current Meters to monitor bias conditions,
4. Doric Trendicator 400 Type J/^{O}C,
5. RF Functional System (see Figure 7).

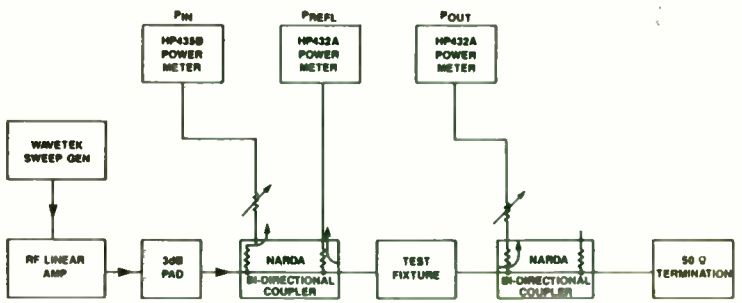


FIGURE 7 - RF FUNCTIONAL TEST SYSTEM BLOCK DIAGRAM

The provision of access to the signal input of the phase detector is useful, insofar as trouble-shooting and test is concerned. It also allows the use of an external phase detector if this is desirable, although some care may be necessary to minimise the generation of spurious sidebands by direct pick up of the logic signals on the VCO control line. The use of open drain outputs provides some reduction in noise when the outputs are not used, compared with the use of full logic swings: nevertheless, it is probably better to esrth these pins when not used. The simplicity of the synthesiser system may be seen by inspection of Fig. 8, where the use of a programmable operational amplifier in the charge pump adds an extra dimension of flexibility in terms of power consumption. The system does require, however, that the common mode rejection ratio of the operational amplifier be good, as it is this parameter which provides most of the reference frequency rejection. Offset in the device must be small, as must noise, and the loop filter design should take into account the open loop response of the amplifier in performing loop stability analyses.

It has been shown that the application of new semiconductor technologies to existing device architectures can produce a significant power and cost saving. It grows more and more impossible to predict the limits of high frequency performance of semiconductors - already, silicon bipolar technology has reached levels which only a few years ago would have been believed impossible for any solid state technology other than Gallium Arsenide. Obviously, the next stage in the development of single chip frequency synthesisers must be operation at higher frequencies, with 512 MHz being the next logical breakpoint. Meanwhile, the size, complexity and power consumption of the VHF synthesised radio can be reduced, while multiplication to the UHF bands is not impossible, on grounds of phase noise, power consumption or both. For more details on the overall phase noise benefits of multiplying see Ref. 2. Synthesiser design has come a long way in the last twenty years, and the introduction of single chip low power VHF and UHF synthesisers will provide equipment designers with a new weapon in the fight to cut cost, size and power consumption.

Ref. 1 A 1 GHz Single Chip PLL for TV, Lawton R, Gaussen P, Cowley N, IEEE-CE Digest of Technical Papers pp 122-123, June, 1982.

Ref. 2 Design Compromise in Single Loop Frequency Synthesisers. P.E. Chadwick, R.F. Technology Expo 1985, Anaheim, Cal. Proceedings published by R.F. Design, 6530 S. Yosemite St., Englewood, Co. 80111 U.S.A.

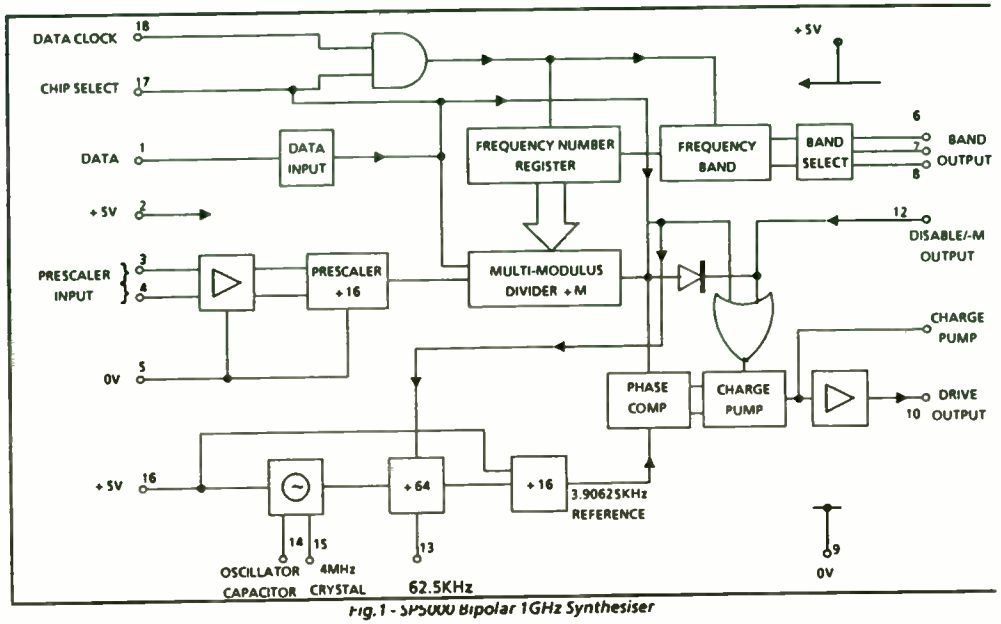


Fig.1 - SP5000 Bipolar 1GHz Synthesiser

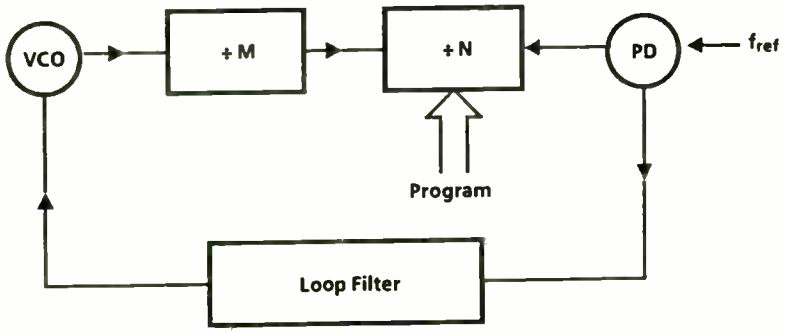
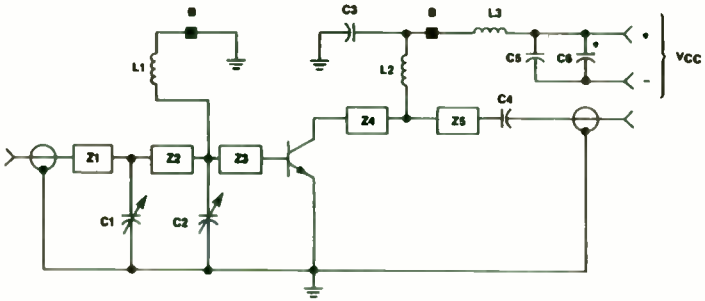


Fig.2 Use of a Fixed Prescaler

Preparation of Samples for IR Scan

The devices are decapsulated using a Jet Etch machine. Details on this machine can be found in AN938 (Motorola, Inc. Application Note). The epoxy mold is removed to expose the surface of the transistor die while the wires and package leads are kept intact and not disturbed. The package is soldered into the RF functional circuit. The circuit schematic and parts list are shown in Figure 8. The circuit employs a 2 inch x 2 inch piece of 31 mil Glass Teflon$_{TM}$ printed circuit board. The samples are mounted to the PC board as a surface mounted component. In other words, no heat sink is used and the board is subject to free air heat transfer.



C1, C2 — 0.8–8.0 pF JOHANSON GIGATRIM
C3 — 91 pF CLAMPED MICA, MINI-UNDERWOOD
C4 — 1000 pF CERAMIC CHIP CAPACITOR
C5 — 68 pF CLAMPED MICA, MINI-UNDERWOOD
C6 — 1.0 μF 25 V TANTALUM
B — BEAD, FERROXCUBE 56-590-65/3B

L1, L2 — 4 TURNS, #21 AWG, 5/32" ID
L3 — 7 TURNS, #21 AWG, 5/32" ID
Z1 — 0.3" x 0.079" MICROSTRIP, Z_0 = 50 Ω
Z2 — 0.47" x 0.079" MICROSTRIP, Z_0 = 50 Ω
Z3, Z4 — 0.2" x 0.079" MICROSTRIP, Z_0 = 50 Ω
Z5 — 0.5" x 0.079" MICROSTRIP, Z_0 = 50 Ω
PCB — 1/32" GLASS TEFLON, ϵ_r = 2.56

FIGURE 8 - IR SCAN 870 MHz CIRCUIT SCHEMATIC

Glass Teflon is a trademark of Dupont Corporation.

The collector leads are painted with flat black paint to provide a good emissivity surface. A reference line is marked on the collector leads to indicate the place where they contact the PC board on the collector microstrip line. The ability to identify this reference point is essential in acquiring accurate and consistent T_L data.

Measurement Techniques

The measurement techniques and considerations are outlined below:

T_L is measured at a point on the collector lead where it first contacts the printed circuit board closest to the package. The T_J measurements are made at three points on the active area of the die. $T_{J\ AV}$, die junction temperature average and $T_{J\ HS}$, die junction temperature hot spot are recorded in Table III. In all cases, the temperatures across the die active area are uniform (i.e. no significant hot spotting was found which indicates good die bonds and proper RF operation of the die in the SORF package). The total power dissipation of the device under steady state operating conditions is defined in the equation below:

$$P_D = P_{IN} + (V_{CC})(I_C) - P_{OUT}$$

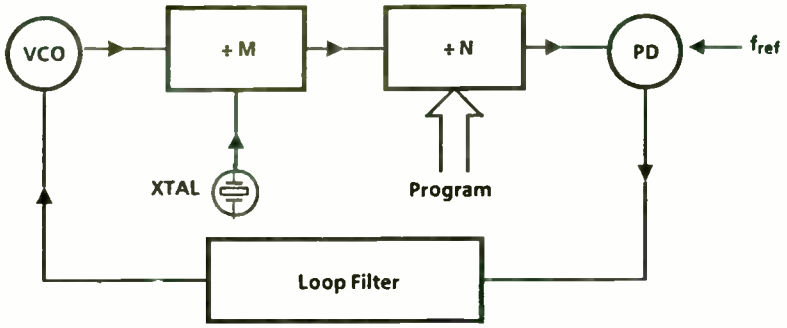


Fig.3 Mixing in the Loop

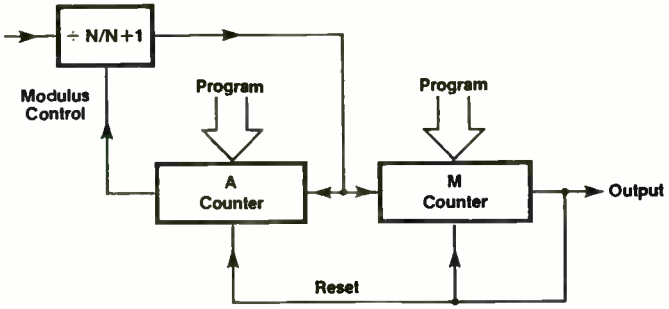


Fig.4 **Two modulus divider**

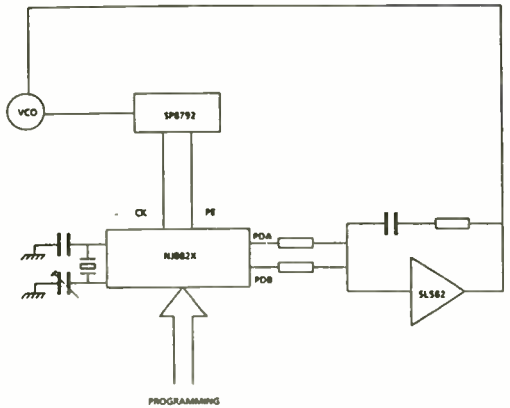


Fig. 5 MULTI-CHIP SYNTHESISER

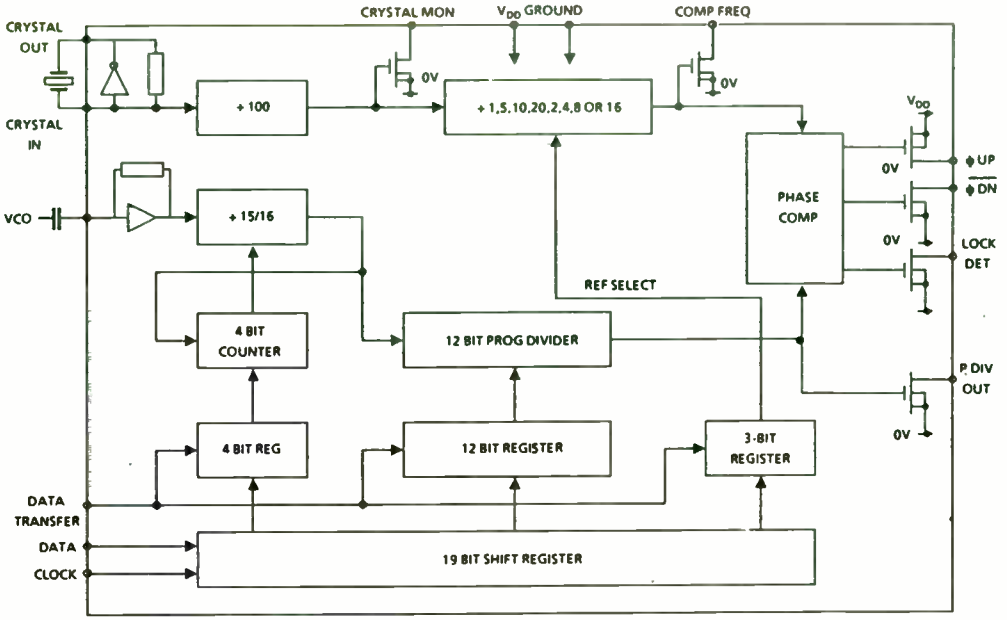


Fig.6 - NJ88C30 Single Chip 200MHz

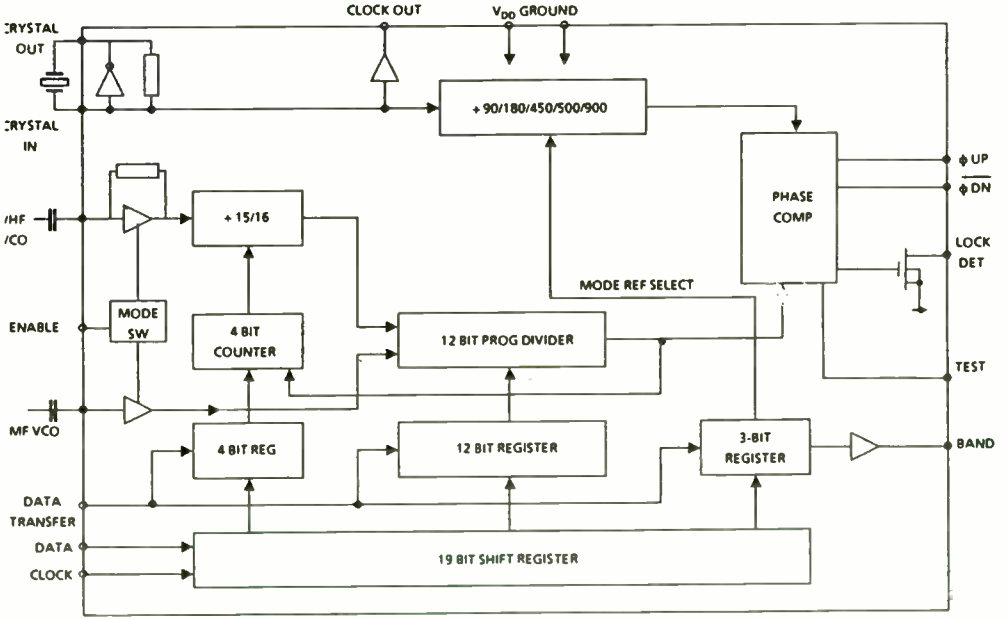


Fig.7 - NJ88C31 Broadcast Radio Synthesiser

The input return loss is greater than 20 dB; thus, it is omitted from the power dissipation equation. The data for the above parameters is in Table III. The thermal scans were done in free air or, in other words, with no forced air over the part and the printed circuit board.

Conclusions

The data demonstrates that the SORF package has nearly equivalent thermal performance to the Macro-X package. The surface mounted technique utilized in this thermal analysis makes convection and radiation the predominant heat transfer mechanisms. In a more comprehensive thermal study of surface mounted techniques, it would be desirable to evaluate the effects of air flow on the heat transfer mechanisms of convection and radiation. In a further study it would be beneficial to also evaluate the heat transfer mechanism of conductivity via a good case to heatsink interface at the collector leads.

Characteristics of the SORF Package

The preceding discussion has demonstrated that the SORF package has excellent RF properties and is a proven surface mount component (SMC) with power dissipation capability of 1.5 watts. When RF performance and a SMC is mandatory, the SORF package offers an excellent alternative to the Macro-X, TO-39, TO-92 and the TO-89.

In Table IV the RF and thermal characteristics and other noteworthy characteristics are summarized. The SORF package offers other specific characteristics which provide a more versatile package. Allowing for a maximum die size of 40 mils x 60 mils the SORF package can accomodate die that fit only in other larger and more conventional non-SM packages. This will provide the RF design engineer with an RF SMD to utilize in new designs or to upgrade to SMT in older designs.

In addition , the SORF package has an additional leadframe style in which the collector and the base pads are split; thus, it provides a package in which there are isolated collector and base pinouts. This modification of the SORF leadframe makes it feasible to assemble more than one transistor die in the same package. With an eight pin leadframe layout various applications are possible such as, complementary push-pull, push-pull (using separate but similar geometries), differential and cascade -cascode amplifiers.

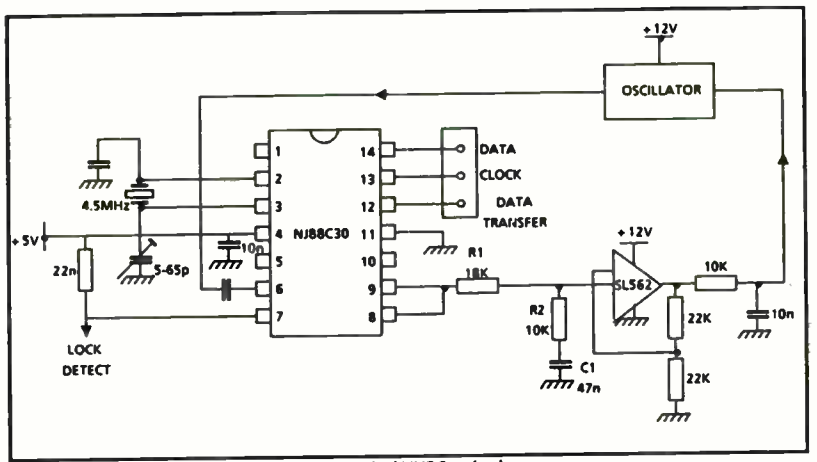


Fig.8 - Typical VHF Synthesiser

TABLE IV - SORF PACKAGE CHARACTERISTICS

Excellent RF Properties:
Low Common Lead Inductance and Package Parasitics
Symmetrical Leadframe Layout
Copper Leadframe for Excellent Conductivity
Excellent Thermal Properties:
Copper Leadframe for excellent Thermal Conductivity
Symmetrical Leadframe Layout
Large Collector Pad
Relativity Large Package Molded Periphery Around the Collector Pad
Accomodate Large Transistor Die that Fit in Other Larger Conventional Packages
Wide Common Lead Bridge for MOS Input Matching Capacitor
Modified Leadframe Available with Split Collector and Base Pads for Special Applications Utilizing Multiple Die

Another characteristic of the SORF which has creative and somewhat tantalizing possibilities is that the portion of the leadframe which interconnects the corner leads of the package is wide enough to accomodate a MOS capacior for input CQ matching (means Control Q - a terminology defined by Motorola, Inc.) . Input CQ matching is accomplished by selecting the proper shunt MOS capacitor value and series inductance interconnect wire loops to raise the device's input impedance to a higher real part while minimizing the device's input circuit Q. This aids broadband matching by reducing the number of external circuit components necessary to achieve a desired broadband performance.

Summary

The SORF package offers an excellent alternative to the many low power packages that are now being used in RF applications which are not SMC. Not only is this package a popular SM package but it also has excellent RF and thermal performance comparable to the Macro-X package. The newly introduced MRF8372 and MRF5812 are excellent examples of the capabilities of this RF low power plastic SMD. The SORF package will lead the way as SMD replaces the more conventional RF low power packages of the past and adds exciting new dimensions to RF SMT.

UNEQUAL POWER SPLIT HYBRID COUPLER

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A B S T R A C T

Presented in this paper are the design techniques for unequal power splitting hybrid branch line couplers. Nomograms are presented for different output coupling levels. The typical application of these devices is in the realisation of UQPSK modulators for high-bit-rate data transmitters.

****

I N T R O D U C T I O N

Branch line quadrature hybrids are familiar for their simplicity and multiuse. These hybrids are suitable as power splitters and combiners while maintaining isolation and matching at the input/output ports.

When a 3 dB quadrature hybrid is powered at input port 1 (Fig.1) and the output ports 3 & 4 are terminated in identical reflection type devices, power is delivered at isolated port 2. This property eliminates the requirement of a circulator for applications like PIN diode phase shifters and diode amplifiers (e.g. trapatt and tunnel diode amplifiers).

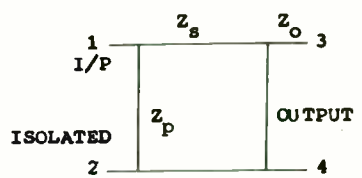

Fig.1 Quadrature hybrid

In general, hybrids for the above applications are 3 dB quadrature type, where power fed at port 1 will be divided equally with 90° phase shift. A typical example utilising the property is a balanced QPSK modulator.

HF/VHF/UHF
Power Static Induction Transistor Performance

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Introduction

A new class of JFET, the static induction transistor (SIT), is attracting a great deal of attention [1-6] because of its exceptional high-performance in the HF, VHF, and UHF frequency ranges. SITs are vertical devices, designed with very short conducting channels fabricated with low carrier concentration semiconductor material. The channel is, therefore, depleted of carriers even at low gate bias voltage levels. Conduction in this channel is controlled by inducing electrostatic fields from the gate and the drain. This explains, to some extent, the name "static induction transistor" given to these devices by Jun-ichi Nishizawa, who first demonstrated SIT operation [7]. The method of current control in an SIT is fundamentally different from that in a JFET. In a JFET, the high series resistance of the neutral channel region and the weak electric field penetration from drain to source result in saturated, pentode-like dc I-V characteristics. In an SIT the field-controlled potential barrier results in exponential dc I-V characteristics.

In addition to describing generally how SITs operate, this paper will show that SITs are extremely well suited for cw and pulsed power, high-frequency applications, especially in the HF, VHF, and UHF range; experimental single-ended devices have thus far shown very high cw and pulsed UHF power levels comparable to or higher than BJTs, MOSFETs, ISOFETs, or JFETs and push-pull balanced SITs have demonstrated high-power, high-gain, broad-band HF/VHF frequency performance. SITs are relatively easy to build and are highly reproducible. They will be used in applications where no other semiconductor devices have proved satisfactory, for example, in very efficient phased-array antenna systems, as replacements for bulky and expensive magnetrons in microwave ovens, in AM and FM radio broadcasting power amplifiers; and in high power and broadband HF/VHF/UHF power amplifiers for military applications.

At lower frequencies, very high-power SITs have already been used in ultrasonic cleaners, in low-distortion audio amplifiers having kilowatt output power capability [8] and as fast switches in a high-voltage thyristor form [9]. Fast solid state relays, dc/dc converters, laser modulators, radio transmitters, and switching power supplies are presently under consideration. The SIT has thus become an important new class of power semiconductor device.

SIT Operation

SITs are a new class of transistors having a short-channel JFET structure in which the current, flowing vertically between the source and drain, is controlled by the height of an electrostatically induced potential energy barrier under the source. This barrier develops when the channel is depleted of mobile charge carriers by reverse biasing the gate junction. The height of the barrier is influenced by both the applied gate and drain bias potentials. A two-dimensional drawing of an elementary SIT cell is shown in Figure 1a. Figure 1b shows the corresponding potential distribution along the path of electron flow in the center of the channel when gate and drain bias voltages are applied. Figure 1c is a more graphic illustration of this potential barrier and the path of electron flow. If the drain potential, V_d, is kept constant and the gate potential, V_g, is varied, the barrier height changes, producing a significant change in the drain current. The SIT differs from long-channel devices such as conventional JFETs or MESFETs because, in addition to the gate bias voltage, the drain voltage also has a substantial influence on the current, through changes in the potential energy barrier height (Figure 1b). Thus, the SIT has unsaturated (triode-like) current-voltage characteristics rather than the saturated (pentode-like) characteristic of a conventional JFET or MESFET. A set of typical SIT dc current-voltage characteristic curves is shown in Figure 2.

The SIT is a majority carrier device, therefore, its speed is not limited by minority carrier stored charge as is the case in a BJT. In addition, since electron velocities are higher than hole velocities, the channel regions are generally fabricated using n-type epitaxial material. Because, for SIT operation, these channel regions must be depleted of charge carriers at low gate bias voltages, relatively high resistivity n-type material must be used. This results in a device which exhibits high breakdown voltages. Since in silicon , electrons reach saturation velocity at high electric fields, this allows device operation at high frequencies while operating at relatively high bias voltage levels.

Electron mobility decreases with increasing temperature in a majority carrier device, thus, the SIT channel is thermally stable. High-power devices may be fabricated in the conventional manner by paralleling low-power cells, but without using ballast resistors. Ballast resistors, which prevent thermal runaway in power BJTs, increase the fabrication complexity of these devices relative to SITs. The current distribution is also different in an SIT than in a BJT. Due to the "emitter crowding" effect in bipolars, the current density is maximum at the edge of the emitter periphery (Figure 3a) This is due to the transverse voltage drop in the base. In an SIT, the current density is more uniform in a source finger of equivalent width (Figure 3b). This means that the active source area is used more efficiently in an SIT than the emitter area in a BJT. In addition, the fact that the current flows through the semiconductor bulk in an SIT and not along the semiconductor surface, such as in a MOSFET, makes the SIT less sensitive to oxide and interface defects which contributes to reliability and high radiation hardness levels.

When data rates of the two streams modulating the carrier in the QPSK modulator are different, the carrier power levels are unbalanced so as to maintain equal E_b/No of the two orthogonal carrier components for effective use of RF power. An attenuator and phase shifter to compensate for the phase introduced by the attenuator are used in the two output branches respectively as shown in Fig.2.

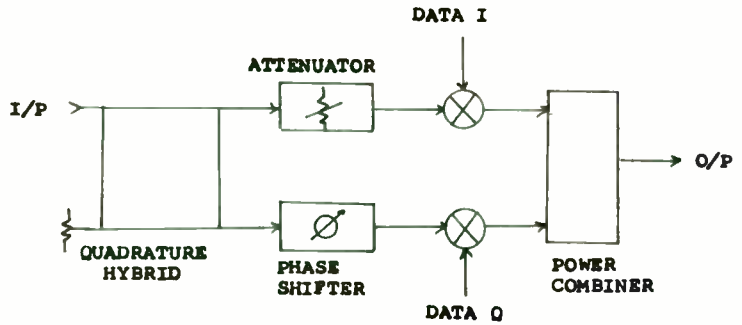

FIG.2 UQPSK MODULATOR

This arrangement increases the complexity of the circuit and is not desirable for space applications. A hybrid with unequal power division properties is a valuable tool in such applications.

The design of an unequal quadrature power divider is explained in the following paragraphs.

D E S C R I P T I O N:

The normalised voltage scattering matrix of ideal lossless hybrid with unequal power outputs, maintaining the 90° phase difference, can be represented by equation 1, where ports 1 and 2 are input and isolated ports respectively.

$$[S] = \begin{bmatrix} 0 & 0 & -jK_3 & -K_4 \\ 0 & 0 & -K_4 & -jK_3 \\ -jK_3 & -K_4 & 0 & 0 \\ -K_4 & -jK_3 & 0 & 0 \end{bmatrix} \qquad \ldots\ldots\ldots 1$$

K_3 and K_4 are the normalised voltages available at ports 3 and 4 respectively, such that power available at port 3 is

$$P_3 = K_3^2 \qquad \ldots\ldots\ldots 2$$

and power available at port 4 is

$$P_4 = K_4^2 \qquad \ldots\ldots\ldots 3$$

For a lossless hybrid

$$K_3^2 + K_4^2 = 1 \qquad \ldots\ldots\ldots 4$$

SIT Power Performance

Power HF/VHF/UHF (1 MHz to 1200 MHz) SITs have been developed and characterized and their performance demonstrated by GTE Laboratories. Devices of various sizes have been fabricated and tests have been performed under various operating conditions. Amplifiers have also been designed and tested.

Previous publications [2,3,5] have provided information about GTE SIT performance at the higher UHF frequencies. Significant advances have been made recently, however, in the performance of SITs in the lower UHF frequency range. To date, the largest cw power static induction transistor fabricated is the 12-cell (W_g = 24 cm), 7-μm pitch SIT shown in the pictorial, Figure 4a. As shown in Figure 4b, this transistor has been exercised to demonstrate up to 215 W cw at 225 MHz, with 7-dB gain and 70% drain efficiency. The terminal impedance of high-voltage power UHF SITs is comfortably high compared to more conventional transistors. This 12-cell SIT exhibits the 215-W power level while working into a 6 + j6 ohm load impedance, approximately a factor of 5 higher than a more conventional, comparably powered transistor. We therefore expect to build single-ended SITs capable of much higher output power before we reach the limiting low impedance levels of present-day power transistors. Having reached the highest practical single-ended transistor power level, we may then consider building a balanced SIT to provide another factor of 2 increase in output power performance. Of course, innovative package designs will be necessary to realize this performance in view of the very high power dissipation levels and the electrical phase length to be accommodated.

Peak pulse power performance at 400 MHz for a single-ended SGSIT using our 3-cell chip design has been demonstrated at levels up to 325 W (Figure 5a). This new device, shown in Figure 5b, with 20 cells connected (W_g = 40 cm) was operated in our test system at a 78-V power supply level in a Class AB mode with a 10 μsec on time and 10% duty cycle, pulsed drive. As indicated in Figure 5a, the terminal impedances of this device are still quite manageable. In fact, increasing the total gate width of the device by a factor of 2, to provide enough capacity for a 600-W transistor, would still result in manageable impedance levels (approx. 1 ohm).

Most of our single-ended power SITs, both for cw and pulsed operation, have been set up in the common-gate configuration. Although common-source operation promises higher gain and potentially higher output power, the drain-gate feedback capacitance results in less stable operation. Nevertheless, performance results with new SITs operated in a common-source, push-pull configuration with cross neutralization [1] have shown a high degree of stability with very attractive broad-band frequency operation and with high-gain and high-output power levels.

These experimental cross-neutralized SITs were fabricated using two 4-cell, 7-μm pitch SGSITs connected in a single, balanced transistor package along with a pair of 18-pf chip capacitors mounted inside the package to provide the neutralization. The photograph in Figure 6 shows one of these cross-neutralized common-source balanced power SITs. An amplifier was designed and fabricated using coaxial 4:1 transformers and baluns loaded with high-permeability ferrite material (Figure 7). Large signal power tests were conducted with this amplifier at frequencies over the 1- to 200-MHz band. Figure 8 illustrates the measured gain, output power and efficiency for the test amplifier. As shown on this figure an output power level of approximately 100 W with greater than 13 dB power gain has been observed from 1- to 100-MHz. The output power performance rolls off to 60 W from 100- to 200-MHz, however, the gain remains relatively flat. Swept measurements have confirmed this data and show no anomalous inflections in the response. With transistor package and amplifier modifications, output power levels in excess of 100 W are expected to be achieved across the band with this design.

Conclusion

This new device, the static induction transistor, is proving to be extremely attractive for applications which require rf power amplification. It has been shown to demonstrate high output power, high-gain, high-efficiency, and broad-band frequency operation. Additionally, it exhibits high-voltage breakdown characteristics, high terminal impedance and preliminary tests indicate a high tolerance to radiation. Coupled with a straightforward processing technology, the SIT has a high potential to advance the performance of future rf power systems.

Acknowledgment

The authors gratefully acknowledge Marguerite Delaney and Peter Palermo for their work in device packaging; Brian Devlin, Charles Herrick, Steve Rose and Maureen Sullivan for their work in device processing and Paul Haugsjaa, Harry Lockwood, and Les Riseberg for their general support during the program.

This work was supported, in part, by the U.S. Air Force Systems Command under Contract No. F33615-82-C-1702 and by the U.S. Army Communications Electronics Command under Contract No. DAAL02-85-C-0160.

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All the four branches/lines are quarter wavelength, whose impedance/admittance values are derived from the scattering matrix (1).

The admittance matrix for this unequal power split quadrature hybrid can be obtained using the transformation shown in equation 5.

$$[Y] = ([1] - [S]) ([1] + [S])^{-1} \qquad .....5$$

By substituting S-matrix and solving equation 5 we get the admittance matrix as

$$[Y] = \begin{bmatrix} 0 & jK_4/K_3 & j1/K_3 & 0 \\ jK_4/K_3 & 0 & 0 & j1/K_3 \\ j1/K_3 & 0 & 0 & jK_4/K_3 \\ 0 & j1/K_3 & jK_4/K_3 & 0 \end{bmatrix} \qquad ....6$$

The voltage ratios shown in equation 6 can be expressed in terms of power ratios as

$$r = P_4/P_3 = K_4^2/K_3^2$$

The admittance matrix is expressed in terms of power ratios as

$$[Y] = \begin{bmatrix} 0 & j\sqrt{r} & j\sqrt{1+r} & 0 \\ j\sqrt{r} & 0 & 0 & j\sqrt{1+r} \\ j\sqrt{1+r} & 0 & 0 & j\sqrt{r} \\ 0 & j\sqrt{1+r} & j\sqrt{r} & 0 \end{bmatrix} \qquad .....7$$

The hybrid constructed from equation 7 divides the power fed at port 1 into the required proportions at port 3 & 4.

The nomograms constructed from equation 7 for obtaining the impedances of series and shunt quarter wavelength of the hybrid in an easy way are given in Fig.3.

PROCEDURE TO USE NOMOGRAMS:

The impedances obtained for a 50 ohm hybrid with +2 dB imbalance in output power levels using the nomograms is explained to illustrate the procedure for the use of the nomograms.

Mark the characteristic impedance of 50 ohms on the centre scale Zo (point A). For calculation of shunt arm impedance, make point B on the left r scale at +2 dB. Intersection point C of the Z_p scale with the line

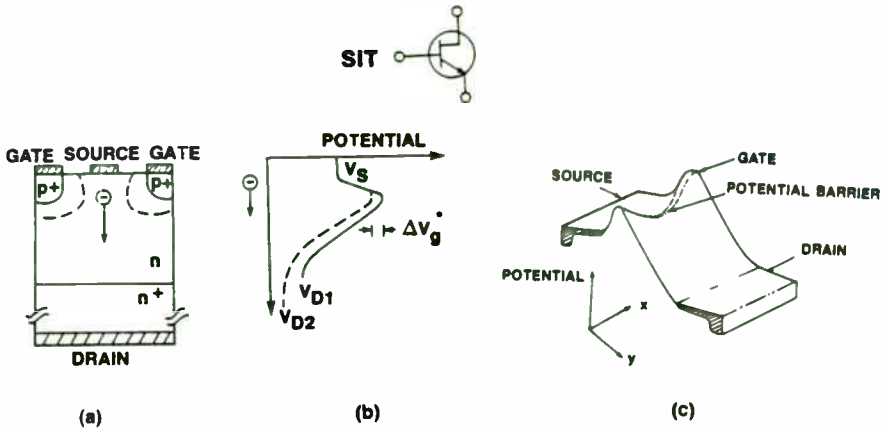

Figure 1. Elementary SGSIT cell (a), and corresponding potential distribution in center of channel along path of electron flow (b), graphic illustration of potential barrier (c).

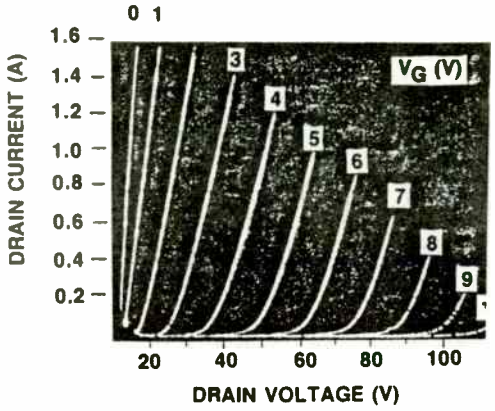

Figure 2. SGSIT DC I-V characteristics (W_S = 24 cm).

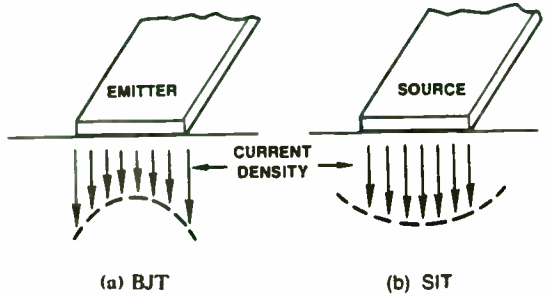

Figure 3. Current density distribution BJT vs SIT.

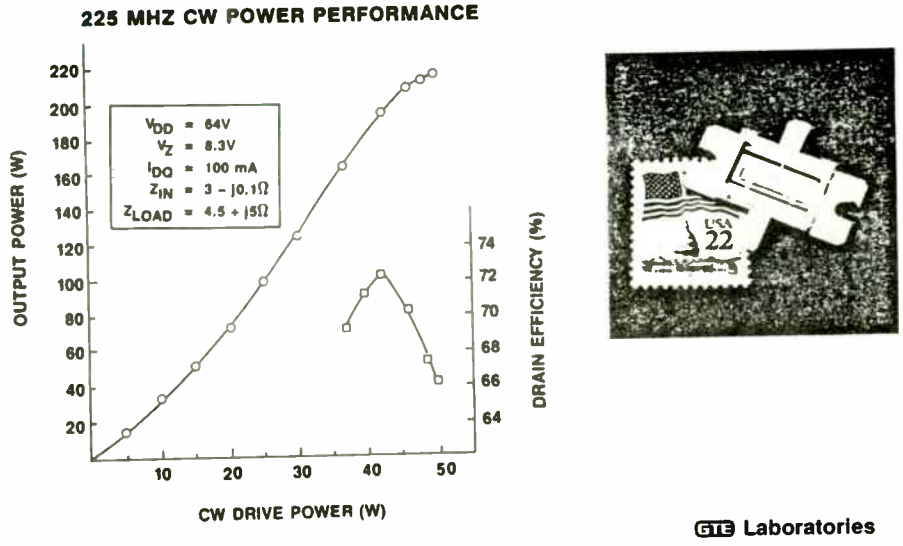

Figure 4. Performance of 12 cell (W_S = 24 cm) SGSIT.

joining points AB gives the shunt impedance. The same procedure is followed for finding series arm impedance with the right r scale.

The values obtained for Z_p and Z_s are 39.7 and 31.1 ohms respectively.

C O N C L U S I O N:

A set of nomograms are presented for finding series and shunt impedances directly. A hybrid with different output power levels is constructed from these nomograms and verified practically. The necessity of an unequal power divider maintaining 90° phase is explained.

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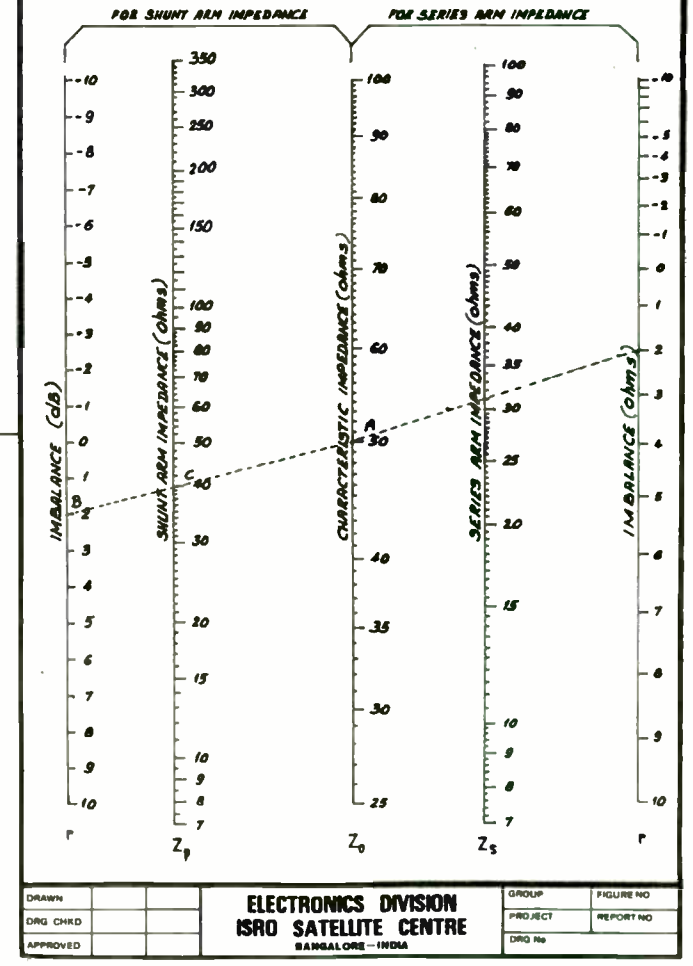
Fig.3. NOMOGRAMS FOR HYBRID CALCULATIONS



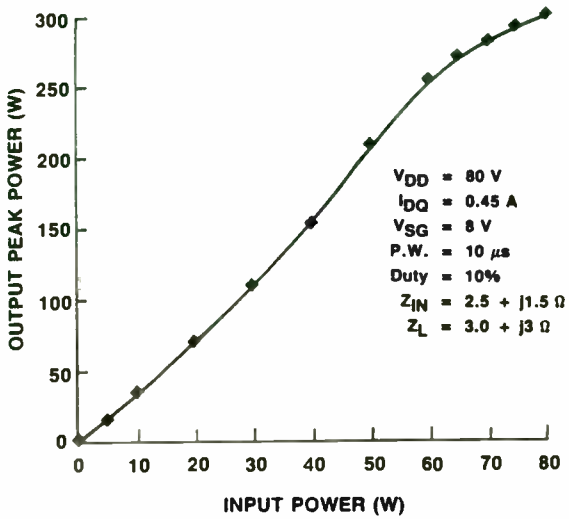


Figure 5(a). 400 MHz peak pulsed power SGSIT performance.

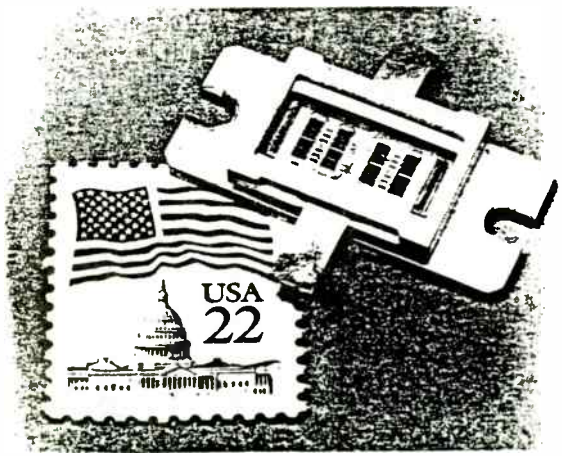


Figure 5(b). 325 W 400 MHz peak pulse power SGSIT.

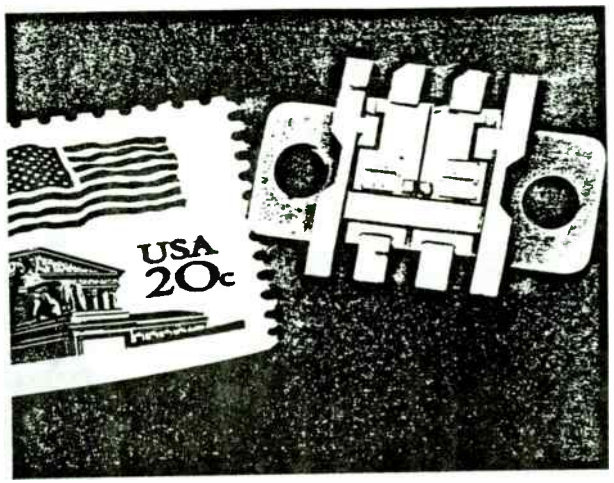


Figure 6. Cross-neutralized common-source push-pull SIT.

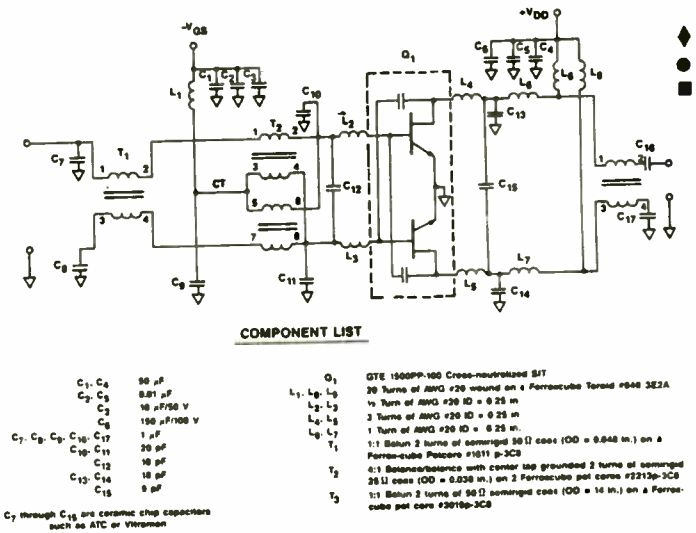


Figure 7. HF/VHF cross neutralized SIT amplifier schematic.

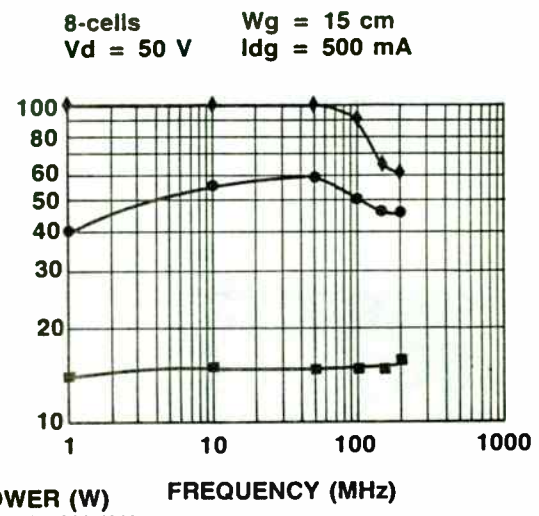


Figure 8. Broadband SIT amplifier performance.

SPHERICAL DIELECTRIC ANTENNA

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A B S T R A C T

Presented in this paper is a study of near field and far field characteristics of s dielectric sphere antenna excited by a circular cylindrical metal waveguide operating in its dominant TE_{11} mode. Many interesting results as a outcome of this study are included. The system can be used as a microwave applicator, a spotbeam antenna and as a feed for a cassegrain reflector.

****

Dielectric antennas are an important class of microwave antennas. These are quite small and capable of giving directive radiations. Various forms of dielectric antennas like the solid rods, hollow tubes, horns and spherical antennas have been studied (in parts) by many researchers. Dielectric spheres in particular have been of great interest to many researchers [1,2,3, 4,5,6 & 8], owing to the simplicity of the shape and many practical applications. Most of the researchers have examined the subject with approximate near field or far field theoretical analysis and tried to compare the results with experimental ones. This paper is an outcome of an extensive theoretical study as well as experimental studies carried out on a dielectric sphere excited by a circular cylindrical metal waveguide operating in its TE_{11} mode. The subject is divided into two categories, namely:

(1) THE SOURCE FIELD OR NEAR FIELD
(2) THE FAR FIELD OR RADIATION FIELD

1.0 SOURCE FIELD STUDIES:

The far field radiation characteristics of an antenna can be deduced from the knowledge of source field distribution. The source field can be determined by solving the electromagnetic boundary value problems over the antenna. The spherical dielectric antenna considered is made of a homogeneous lossless dielectric material and

A High Performance SAW Filterbank Achieves 80dB Rejection

by
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I. Introduction

This filter bank was designed as part of a general-purpose receiver system, which was to be able to isolate signals of differing center frequencies and bandwidths, to separate these signals from the surrounding spectrum and then to demodulate these signals. The features of the filterbank which were essential to this system were: excellent rejection, good control of bandwidth , filter selectivity, good amplitude and phase ripple and equal noise power in each channel. Surface wave filters meet these primary requirements nicely while maintaining a small outline and requiring little power.

This paper will present the specific requirements for a filterbank requiring 80dB of stopband rejection, followed by a discussion of both the electronic circuit and surface wave filter design. Results from production filters will be presented, followed by indications of improvements to these sorts of filterbanks.

II. The Requirements

The detailed specifications for this filterbank are presented in Appendix I. The essence of the filterbank is presented in the schematic shown in Figure 1. An input signal passes through a wideband roofing filter and a low-noise amplifier and then through one of nine channels

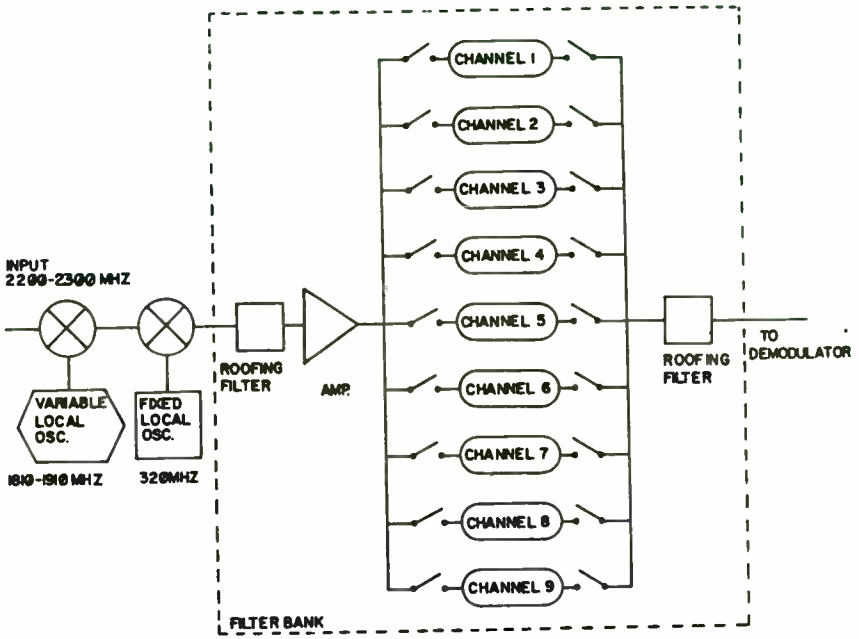


Figure 1

is excited by the TE_{11} mode fields of a circular cylindrical metal waveguide [7]. In order to ensure some degree of matching between the antenna and the waveguide and also to suppress the generation of higher order modes (to the extent possible), the interior of the circular cylindrical metal waveguide is filled over a short distance by the dielectric of which the sphere is composed. The generator end of the circular cylindrical dielectric rod thus formed inside the waveguide is conically tapered to a point (as illustrated in Fig.1) to take care of the matching between the waveguide and the dielectric structure (It has been experimentally seen that such a tapering [10] does improve the return losses). However, for the theoretical analysis and to simplify the analysis for the first degree of approximation, the higher order mode generation at the end of the waveguide is neglected and the propagating mode inside the waveguide is assumed to be only TE_{11}. The theoretical analysis for the source field components over the sphere is done by [6, 10] expressing the TE_{11} mode components of the cylindrical waveguide in spherical co-ordinates at the interface between the waveguide and the spherical geometry of the antenna, keeping the sense of 'ϕ' co-ordinate the same. These field components are further expressed in terms of spherical harmonics. Their respective amplitude-coefficients at the interface are determined using 'Fourier Legendre Series' [6, 9, 10], and the TE_{11} field components are expressed in a spherical co-ordinate system.

These fields at the interface are assumed to be the impressed fields in the sphere due to the waveguide excitation.

The fields internal to the sphere will consist of the fields due to the waveguide and the fields internal to the sphere obtained by solving the source free Vector wave equations [Straton-8].

The boundary conditions are matched at the surface of the sphere (r=a) for the field components internal to the sphere and the external field components obtained by solving the source free Vector wave equation [Straton-8] external to the sphere.

It is seen that during the various field matchings over the surface of the sphere (at r=a) on both sides of the equations, terms containing constants of

$$(m,\ n^{th}\text{order}) \text{ and } \frac{P_n^m(\cos\theta)}{\sin\theta} \text{ and } P_n^m(\cos\theta) \text{ do}$$

appear. Here $P_n^m(\cos\theta)$ is the Associated Legendre's Polynomial of first kind of degree 'n' and order 'm'. It is observed that for the six field components, six simulataneous equations are obtained.

From the six equations we see that the lowest [8,10] field mode which can exist is m=n, while for a given m,

having bandwidths from 0.1 MHz (channel 1) to 12.0 MHz (channel 8) and 25 Mhz (channel 9, direct). All channels had a common center frequency (70 MHz) and were required to have equal noise powers (for white noise, the power levels in each channel were supposed to be the same), so the insertion losses varied from 29dB for channel 1 (0.1 MHz) to 50dB for channel 8 (12.0 MHz) and 53dB for channel 9 (direct).

The most strenuous specification was the requirement for 80dB of rejection for each channel. This rejection had to be maintained from 5 MHz to 400 MHz outside seven 3dB bandwidths from the center frequency and drove most of the design, as will be discussed in section III. The next most important specification was the requirement for 50dB of insertion loss for channel 8, which put a severe constraint on the noise floor for the filterbank. These two specifications forced most of the interesting design decisions.

The requirements for precisely controlled bandwidth and shape is common to most surface acoustic wave filter designs. Since an enormous number of transmission zeros can be designed in a very small space, surface wave filters can provide excellent selectivity which is essentially independent of matching and insertion loss. Also, manipulation of these zeros can compensate for second order distortions which affect filter symmetry. The requirements of less than one dB of amplitude ripple and less than ten degrees of phase error in each channel, as well as the differential phase error specification, are also straightforward and easily satisfied with surface wave devices.

The entire operating filterbank had to meet a series of mechanical and environmental conditions including vibration and shock as well as a powered burn-in.

III. The Design Approach

A. General Considerations

The requirements for this filterbank specified nine channels, one of which was a direct channel and one of which had a 0.1 MHz bandwidth. Early analyses of channel 1 (0.1 MHz) showed that surface wave filters for this bandwidth would be much too large, so the customer agreed to supply a bulk crystal filter which met their requirements. The direct channel also needed no filter (other than an overall roofing filter to reject out-of-band noise). Probably the most important specification items were the combination of 80dB of rejection with a required 50dB insertion loss on channel 8; for an input signal at 0dBm, this puts a requirement on the noise floor to be at -130dBm. This really stems from the customer's desire to have equal noise power in each channel, so the insertion loss of the widest channel had to be considerably higher than that of the narrowest channel. Proper grounding and shielding and overall control of the noise in the circuit board was by far the most difficult aspect of the development of the filterbank.

B. Electronics

The requirement for 80dB of stopband rejection regardless of the channel selected forced the choice of dual PIN diode switches for each of the nine channels in the filterbank. These switches did not have to be

there are 12 field amplitude coefficients of (m,n),(m,n+1) (m,n-1)th order, which indicates that the boundary conditions are satisfied not for a single value of n but for n-1, and n+1 combined together. This shows that for any particular value of 'm', the electric and magnetic field components consist of an infinite number of terms for values of 'n' varying from m to ∞, thus indicating that for each value of m, there exist many corresponding hybrid modes.

However, the boundary conditions are matched for n=n, n=n-1, n+2 and a total of 16 equations are obtained for internal field amplitude coefficients. The coefficients are of (m,n), (m,n-1) (m,n+1) and (m,n+2) order. Sixteen simultaneous equations are solved for the 16 amplitude coefficients, which are in general complex. Knowing the m, nth order amplitude coefficients one can determine the internal and external (surface) source fields, which are used for far field computations. From the above treatment, it is inferred that a homogeneous dielectric sphere excited by a circular cylindrical metallic waveguide operating in its dominant TE_{11} mode can support an infinite number of hybrid modes which have all the six components of EM field, namely E_r, EΘ, EØ, Hr, HΘ & HØ. Representative near field patterns are given in Figs. 2-1 to 2-4.

2.0 FAR FIELD STUDIES:

Having obtained the source field distribution, the radiation or far field of the spherical dielectric antenna excited by a circular cylindrical metal waveguide is obtained using the famous - Schelkunoff's Equivalence Principle. An analysis of the radiation pattern and gain as a function of various parameters, viz. diameter of the sphere, frequency of excitation and relative permittivity of the material has been done. The studies are limited to X-band for experimental verification purposes.

3.0 NUMERICAL COMPUTATION & OBSERVATIONS:

SOURCE FIELD:

The source field components have been evaluated [6, 10]. The computation has been done for different diameters and relative permittivities of the dielectric sphere for various frequencies of excitation at X-band, for a lossless homogeneous sphere. The computations have been carried out for the first seven primary modes i.e. m=1 to 7 and n=1 to 7 (except m$>$n). While normalizing with respect to the maximum value of the mode out of a large number of m, n combinations, the amplitudes of the coefficients and field components for

quick because the bandwidth selection was to be by mechanical thumbwheel switches, so the diodes were chosen to give a switching time of about one microsecond at 70 MHz. Each series-shunt diode switch has an on-to-off ratio of 54dB at 70 MHz for a combined isolation of 108dB for a single channel all by itself. Since all nine channels were bussed in parallel, with all channels selected off, the isolation from bus to bus was 89dB, a 9dB margin on the 80dB specification.

The requirement of 50dB of loss for channel 8 (12.0 MHz) combined with 80dB of rejection meant that the incoming signal level had to be high enough that the 80dB rejection level was at or above thermal noise. This was accomplished by driving the SAW devices at about +20dBm with an amplifier. Additional LC roofing filters at input and output were necessary to keep the noise floor below the rejection level for channel 8 and also served to suppress SAW harmonic responses, as will be discussed below.

C. The SAW Filters

This filterbank has filters whose center frequency is 70 MHz and whose channel bandwidths range from 0.1 MHz to 400 MHz. As discussed in section IIIA, channels 2 through 8 were implemented with SAW filters whose percentage bandwidth (3dB bandwidth normalized to the center frequency) varied from about 0.4% (channel 2) to about 17% (channel 8). Since the maximum achievable bandwidth for a piezoelectric surface wave material is a function of its electromechanical coupling constant [1], different SAW substrate materials were used for different channels. Specifically, ST-X quartz was used for channels 2, 3 and 4 (0.3, 0.5 and 0.75 MHz), YX quartz was used for channel 5 (1.5 MHz) and YZ lithium niobate was used for channels 6, 7 and 8 (4.0, 6.0 and 12.0 MHz). These materials all have different temperature coefficients, but this filterbank is used in an environment whose temperature does not vary much and in a system that can adapt to differing center frequency shifts due to temperature, so the different substrate materials for each channel was not a problem.

The requirement for 80dB of stopband rejection cannot be met on narrowband quartz materials due to the presence of surface wave diffraction on these substrates; 45-50dB of stopband rejection is about the best that can be achieved with filter shape factors of around 2.5 on quartz. This means that all of the quartz SAW filters had to be implemented as cascaded pairs. The substrate material used for other channels, YZ lithium niobate, happens to be autocollimating; surface waves exhibit almost no diffraction on this material. This means that it may be possible to achieve the 80dB rejection requirement in a single filter, and indeed, the design simulations predicted that channel 8 (12.0 MHz) could be built as a single filter. Channels 6 and 7, however, had design sidelobes higher than 80dB and so these channels were designed as cascaded pairs.

Surface acoustic wave bandpass filters generally exhibit two kinds of frequency domain spurious, harmonic responses and bulkwave responses [2, 3]. The harmonic response is governed by the choice of the number of electrodes per wavelength (for example, 3 electrodes per wavelength supports the second harmonic and 4 electrodes per wavelength supports the third harmonic) and generally only the first harmonic response above the

the orders m=2 and more for all values of 'n' are almost two orders less in magnitude than those of m=1. Hence, the computation for further processing was restricted for m=1, and n=1 to 7. From the computation results, it is observed that:

(a) For all modes the external field components Er, EΘ, HØ show a cosine variation and E_{ϕ}, Hr, and H_{θ} show a sine variation with respect to 'Ø' for 'Ø' varying between $\pm$ 180°. This behaviour is independent of sphere diameter, frequency of excitation and dielectric constant.

(b) The variation with respect to 'Θ' for a fixed 'Ø' shows that for |Er| & |Hr| there exists a null at Θ = 0, i.e. no axial radial component of E & H fields exists.

For other field components it is observed that all the modes except (1,1) show an oscillatory behaviour. |EΘ| is the strongest component.

3.2 RADIATION FIELD:

The radiation field patterns, directivity and gain have been computed for the dielectric sphere antenna using the source field components, since from the source field studies [10] it is clear that no single mode will characterise the complete source field components. Hence, the far field calculation have been carried out for the vectorial summation of even, odd and all modes of the source fields. Calculations have seen done for spheres of 100, 75 & 50mm diameters at X-band for ε_r=2.1, 5,7, 10 & 15. For all mode combinations of the source field, the radiation patterns for representative cases are given in Figs. 3(a), (b) and (c).

4.0 EXPERIMENTAL STUDIES:

The experimental investigations have been undertaken in order to validate the theoretical studies. The experimental work is extended to investigate some of the practical applications of the dielectric sphere antenna under investigation. The investigation has been carried out mainly for X-band frequencies (8.2 GHz) and sphere diameters: 30, 50, 75 and 100mm and the ε_r= 2.1.

The source field components at the surface of the sphere have been measured using near field pickup probes. The variation of these source field components as a function of Θ & Ø co-ordinates is reported. The radiation field patterns have been plotted for both E&H planes. The results are reported as $|E_T|$ & $|E_p|$ patterns as a function of 'Θ' co-ordinate. Gain measure-

fundamental is large enough to be a problem. Bulkwave responses can be caused by a number of different acoustic modes generated by the transducer in addition to the surface wave. On quartz, these bulk modes generally manifest at about twice the center frequency and can be very troublesome. On lithium niobate or any other high-coupling material, a multi-strip coupler structure can be used between the transducers to eliminate bulkwave spurious. For the quartz filters, the bulk and harmonic responses were eliminated by designing one transducer to operate at 70 MHz at its second harmonic and designing the other transducer to operate at 70 MHz at its third harmonic. No other harmonic responses coincided, so the spurious responses were eliminated. The lithium niobate filters were designed to operate at 70 MHz at the fundamental using a multi-strip coupler to suppress bulkwave spurious and relied on the LC roofing filters to suppress the harmonic response.

A significant advantage of surface wave filters is the flexibility the designer has to meet specific spectral shape requirements. This filterbank required control over the minimum and maximum 3dB bandwidth, the maximum 60 and 70dB bandwidths, the symmetry of the passband and the specific value of the insertion loss for each channel. These requirements are typical of almost any surface wave bandpass filter and can be fulfilled in a straightforward manner. In addition, the choice of cascaded filters allowed the designers to implement a time domain spurious suppression trick that reduced both amplitude and phase ripple across the passband (the specifications did not require this, but it cost nothing to design in and it improves the performance.)

This filterbank has been in production for some time and the need to design the filters and their matching networks for minimal handling in a production environment was recognized from the start of the design. Accordingly, each filter design was subjected to a matching network sensitivity analysis for standard component tolerances. Only designs that were tolerant of the component variations expected were used to cut down on production line alignment and tuning time. Also, procedures were developed to keep the alignment process from becoming tedious and to streamline assembly.

IV. The Results

Figures 2-14 present data from a representative filterbank from a production run. Spectra for channels 1 through 9 are shown, and the rejection of the worst filter (channel 8) is presented from 5 MHz to 400 MHz. Notice that the filters uniformly achieve 80dB of rejection well inside seven 3dB bandwidths from the center frequency; in fact, most achieve 80dB on the monotonic skirts. This clean shape is a direct consequence of the choice of cascaded filters to achieve the rejection. Compare the narrower channels with channel 8, which was implemented with a single filter. Channel 8 showed some close-in spurious at about 72dB, but achieved 80dB within seven 3dB bandwidths. Also, Figure 12 shows the passband response of a representative filter, (channel 4). Figures 13 and 14 show the difference between two identical filter channels, one not employing the triple travel canceling scheme and the other utilizing it. All production filterbanks met the specifications outlined in section II

ment have been done using standard gain antenna substitution method, and axial ratio studies using a rotating dipole for a circularly polarized wave excited sphere antenna have also been carried out. The return loss or VSWR measurements of the antenna system is done over 7-12 GHz frequencies, using an HP8410 network analyzer. The near and far field test setups are shown in Figs. 4(a) & 4(b). The circular polarization is achieved using a septrum polarizer [10, 11].

5.0 DESIGN & CONFIGURATION OF THE ANTENNA:

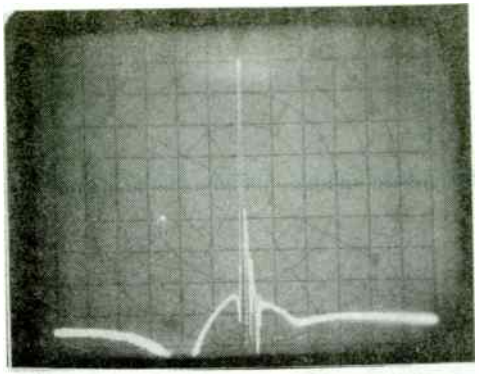
A dielectric sphere of diameter > 30mm (at X-band) is excited by a circular cylindrical metallic waveguide operating in its dominant TE_{11} mode. The mode generation is achieved by two methods: (a) a coaxial to waveguide adapter changes TEM mode to TE_{10} mode. The rectangular to cylindrical waveguide gradual transition changes the TE_{10} mode to TE_{11} mode, (b) the other method of exciting TE_{11} mode inside the circular cylindrical waveguide is to adjust the depth of a coaxial connector centre pin mounted on a circular cylindrical metal waveguide and adjust the close end of the guide with a short circuit plunger such that the input VSWR is less than 1.1. One can measure the E field configuration at the open end to make sure of the existence of the TE_{11} mode.

In both systems, the waveguide at the open end is loaded with a dielectric sphere. In order to have a smooth transition between the waveguide and the sphere, at one end of the sphere there is a dielectric cylindrical rod (the same material as that of the sphere), tapered at the end, with its outer diameter equal to the internal diameter of the circular cylindrical waveguide. The length of the rod is experimentally adjusted such that no high VSWR is observed. The cylindrical dielectric rod length is less than λ. The tapered portion is $\simeq 0.68\lambda$. This configuration is almost analogous to the situation where the waveguide is filled with the dielectric material of which the sphere is made, such that the dominant mode is TE_{11} and there are no discontinuities due to dielectric mismatches.

The near field studies have been conducted using small pickup probes [10, 12], a monopole for $|E_r|$, a small dipole for $E\theta$ & E_ϕ and a small magnetic loop for H-components. The far-field radiation studies have been conducted under the normal far field conditions. The gain is determined by comparing with a standard gain antenna while the axial ratio studies have been done using a rotating dipole. The circular polarization is achieved using a septum polarizer [10,11]. The effect of a corrugated flange at the back of the antenna has

REJECTION SPECTRUM OF CHANNEL 1

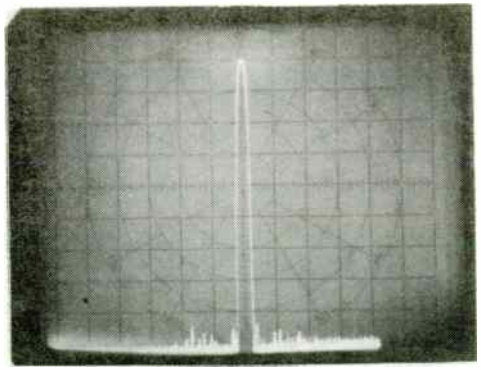
0.100 MHz



Vertical: 10dB/cm Horizontal: 60 MHz to 80 MHz linear
Figure 2

REJECTION SPECTRUM OF CHANNEL 2

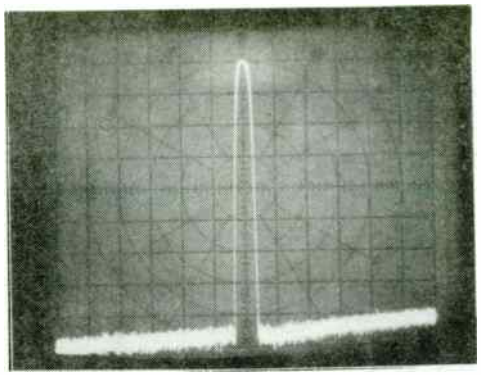
0.300 MHz



Vertical: 10dB/cm Horizontal: 60 MHz to 80 MHz linear
Figure 3

REJECTION SPECTRUM OF CHANNEL 3

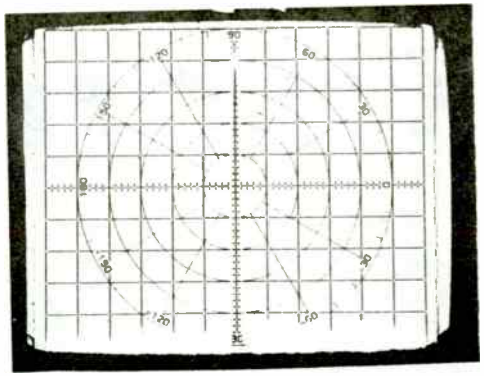
0.500 MHz



Vertical: 10dB/cm Horizontal: 60 MHz to 80 MHz linear
Figure 4

REJECTION SPECTRUM OF CHANNEL 4

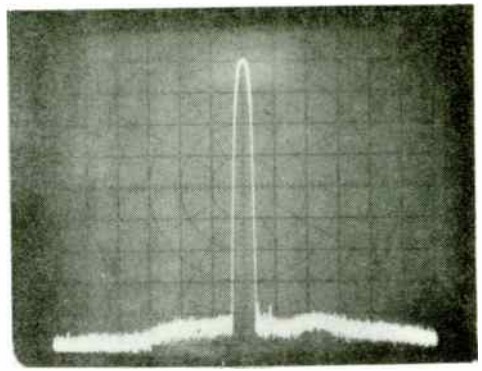
0.75 MHz



Vertical: 10dB/cm Horizontal: 40 MHz to 100 MHz linear
Figure 5

REJECTION SPECTRUM OF CHANNEL 5

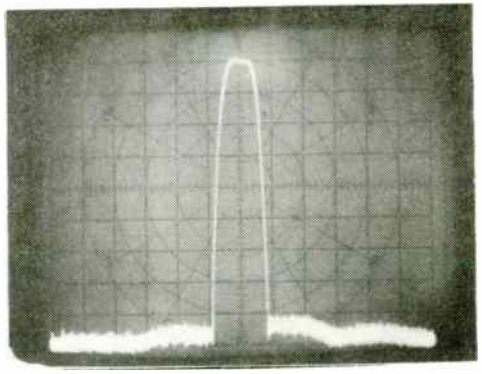
1.5 MHz



Vertical: 10dB/cm Horizontal: 40 MHz to 100 MHz
Figure 6

REJECTION SPECTRUM OF CHANNEL 6

4.0 MHz



Vertical: 10dB/cm Horizontal: 40 MHz to 100 MHz linear
Figure 7

been studied for gain and axial ratio properties. Some of the experimental results compared with the theoretical results for near field as well as far field are shown in Figs.(5) & (6), while far field experimental curves for various diameter spheres for pattern as well as axial ratio studies are shown in Figs.(7) & (8). A derived gain V/S diameter/λ curve is also given in Fig.9.

6.0 CONCLUSIONS AND POTENTIAL APPLICATIONS:

From the theoretical analysis the following observations can be made:

6.1 SOURCE FIELD:

It is possible to solve the boundary value problem for a dielectric sphere excited by a circular cylindrical metal waveguide operating in TE_{11} - mode. The theory evolved out here can be used for other popular cases, such as a dielectric sphere excited by a structure having HE_{11} - mode. The same method can be used for solving boundary value problems in ferrite spheres.

A dielectric sphere excited by a circular cylindrical metal waveguide operating in its dominant mode can sutain an infinite number of hybrid modes over its surface. The relative amplitude and phases of the modes will be different depending upon the sphere diameter, dielectric constant and frequency of excitation.

From the numerical calculations it is inferred that higher order modes are negligible in amplitude as compared to the first few primary modes.

The six source field components over the surface of the sphere show a sinusoidal variation with respect to ϕ. Er, Eθ & Hϕ show cosine variation while Eϕ, Hr and Hϕ show sine variation. All the field components and their different modes except mode (1,1) show an oscillatory behaviour with respect to θ.

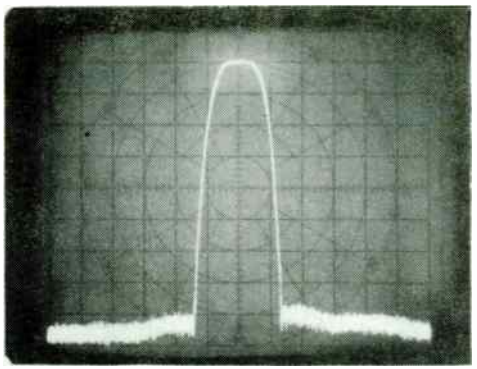
It is difficult to draw a general conclusion. However, it is seen that the dielectric sphere antenna excited by a circular cylindrical metal waveguide operating in TE_{11} - mode, will sustain an infinite number of hybrid modes. The relative amplitudes and phases of these modes will be diffarent depending upon the sphere diameter, dielectric constant and frequency of excitation.

6.2 RADIATION FIELD:

From the radiation field studies it is observed that the dielectric sphere loading increases the gain

REJECTION SPECTRUM OF CHANNEL 7

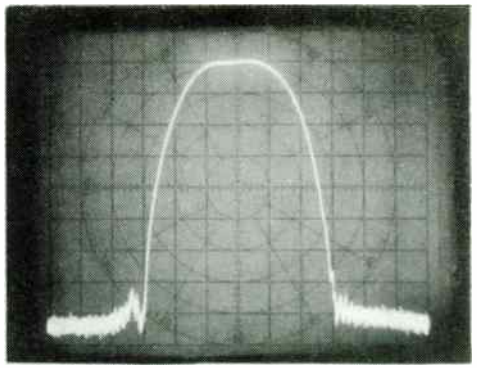
6.0 MHz



Vertical: 10dB/cm Horizontal: 40 MHz to 100 MHz
Figure 8

REJECTION SPECTRUM OF CHANNEL 8

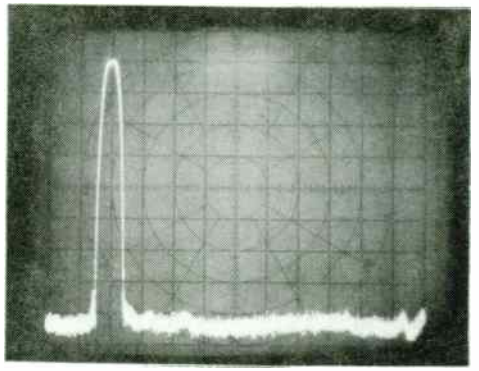
12.0 MHz



Vertical: 10dB/cm Horizontal: 40 MHz to 100 MHz linear
Figure 9

REJECTION OF CHANNEL 8 (12.0 MHz BANDWIDTH)

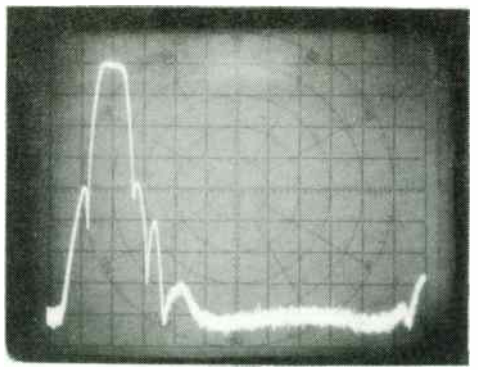
FROM 5 MHz TO 400 MHz



Vertical: 10dB/cm Horizontal: 5 MHz to 400 MHz linear
Figure 10

REJECTION SPECTRUM OF CHANNEL 9

DIRECT



Vertical: 10dB/cm Horizontal: 5 MHz to 400 MHz linear
Figure 11

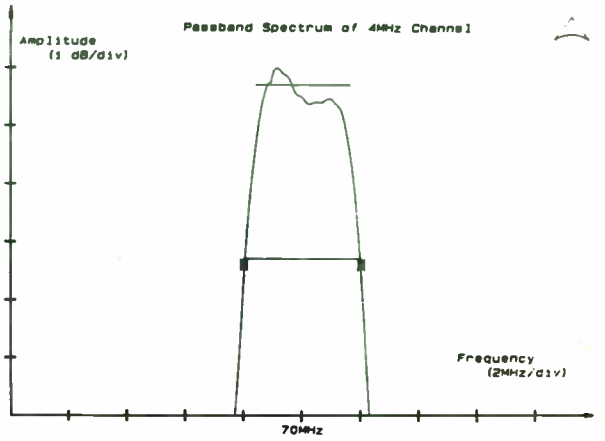


Figure 12

of a simple cylindrical waveguide and provides an E and H - plane pattern symmetry with a circular beam cross section. With increase in dielectric constant the main lobe width increases and the directivity reduces. It is seen that for a given sphere diameter and frequency of excitation there is an optimum dielectric constant for which maximum gain is obtained. Just as with increase in dielectric constant or relative permittivity, the directivity does not increase. For $\frac{d}{\lambda} \simeq 2$ to 2.1, for maximum directivity the ε_r should be $\simeq$ 2.1 - to 5.0, beyond which the main lobe width will start increasing. The sphere for a given diameter shows a resonance phenomena. The increase in frequency does not increase the gain proportionately.

6.3 EXPERIMENTAL STUDIES:

From the experimental investigations the following was found:

6.3.1 SOURCE FIELD:

Over the surface of the sphere all six EM - field components exist. All six source field components show a sinuaoidal dependance on ϕ (FIG.10).

There is a good agreement between the theoretical and experimental source field plots for spheres of diameters $>$ 2X waveguide diameter. The agreement is for a combination of certain modes and not for an individual mode. The agreement appears to be there even without probe compensation.

6.3.2 RADIATION FIELD:

There is an agreement between the theoretical [for all mode combination] and experimentally obtained radiation field plots as far as over-all pattern shape is concerned. The theoretical plots show higher side lobes and slightly wider main lobe compared to the experimental. The theoretical gain is less than the expeeimental.

From the experimental radiation field plots, it is seen that the main beam has a circular cross section with an approximate E - and H - plane pattern symmetry compared to the waveguide alone. The sphere increases the gain and compresses the beam of the waveguide pattern. Even a hemisphere compresses the waveguide pattern and increases the gain by almost 3 dB. For $\frac{d}{\lambda} = 2.1$ or more the radiation field patterns appear to be Gaussian beam pattern.

It is seen that the dielectric sphere antenna gives 1-3 dB increase in gain over a uniformly illuminated equivalent aperture, depending upon the d/λ. Optimum

SPECTRUM OF CHANNEL 2 (0.300 MHz)

WITH NO TRIPLE-TRAVEL SUPPRESSION

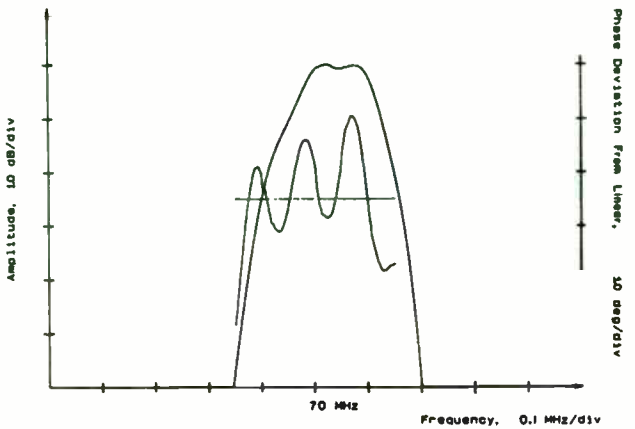


Figure 13

SPECTRUM OF CHANNEL 2 (0.300 MHz)

WITH TRIPLE-TRAVEL SUPPRESSION

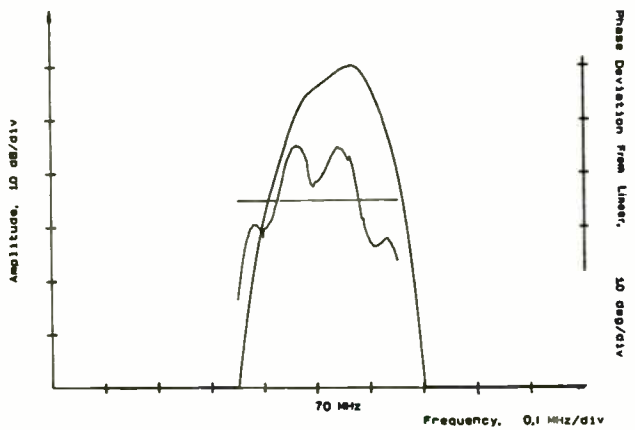


Figure 14

and Appendix I; more than 100 filterbanks were produced.

V. The Application

As can be seen from Figure 1, the filterbank was used in conjunction with a low-phase noise oscillator to form the IF section of a general purpose receiver. The operator of this receiver can select the frequency to be analyzed by choosing the synthesized oscillator's frequency and then can select the analysis bandwidth by choosing the appropriate filterbank channel. Following this module is a general demodulator module, which allows the operator to select one of a variety of demodulation techniques (AM, FM, PM and so forth).

Specifications for both the variable oscillator and for the filterbank will be presented, followed by data from the multichannel system. Interesting performance parameters will be discussed in depth.

Appendix I presents the electrical specifications for the synthesized local oscillator shown in Figure 15 and also the electrical specifications for the filterbank shown inside the dotted line in Figure 1.

Figure 15 presents the schematic of the synthesized local oscillator. It is a single phase locked loop driven by an external, low noise reference oscillator at 10 MHz (supplied by the customer). It was fabricated using microstrip circuits and only screened components (resistors, inductors, capacitors, semiconductors) were used. Figure 16 shows the phase noise for a typical production unit. All electrical specifications were met over all the environmental conditions; this includes the random vibration (whose level is about 7G RMS). Units were tested to 10G RMS for more than four hours with no degradations of any specification (including phase noise and

gain is obtained for $\frac{d}{\lambda} \simeq 2.1$ to 2.5 [Tables & Fig.9].

There is good VSWR matching for all the spherical antennas studied here over the frequency band 7 - 12.4GHz. The VSWR or return loss shows some type of resonance phenomena. The minimum VSWR$\simeq$ 1.1 while the maximum $\simeq$ 1.6 (Fig.11).

The sphere does not disturb but slightly improves the axial ratio, if excited by a waveguide with a circularly polarized signal. A choked flange at the back of the sphere reduces the side lobes, increasing the gain. The position of the flange from the open end of the waveguide can be experimentally adjusted for minimum axial ratio and maximum gain.

7.0 POTENTIAL APPLICATIONS:

The good E- and H- plane pattern symmetry with circular beam cross section, low side lobes, Gaussian beam, excellent VSWR matching with the excitor, good axial ratio for circular polarized exciting signal, focusing of the beam, small and compact size make the antenna under discussion a potential candidate for many applications as a primary antenna, secondary antenna and also a microwave applicator. A few of the applications are:

SPOT/GLOBAL BEAM ANTENNA FOR COMMUNICATION SATELLITES

The antenna can be used to provide spot and global beams for geosyncronous communication satellites, with good axial ratio and low cross polar component with E- and H-plane pattern symmetry. With the use of a proper septum the antenna can be used for orthogonal polarization transmission/reception of signals with isolation better than or$\simeq$ 30 dB. This would be a typical example of the antenna being used as a primary antenna. The small size of the antenna makes it quite attractive, especially for dual polarized global beam coverage, for $\epsilon_r = 2.1, \frac{d}{\lambda} \simeq$ 2.5 is suitable for a global beam.

SHAPED WIDE BEAM ANTENNA:

The inherent E- and H- plane pattern symmetry, good axial ratio for circularly polarized signal and excellent VSWR matching with the exciting structure properties of the dielectric sphere antenna, are used in achieving a wide beam antenna with a dip in the centre of the pattern and gains at the beam edge. The pattern is such that for a 900 KMS orbiting spacecraft the antenna gain compensates for the path loss variations. Such an antenna has been developed for onboard use on the Indian Remote Sensing Satellite for transmitting data at

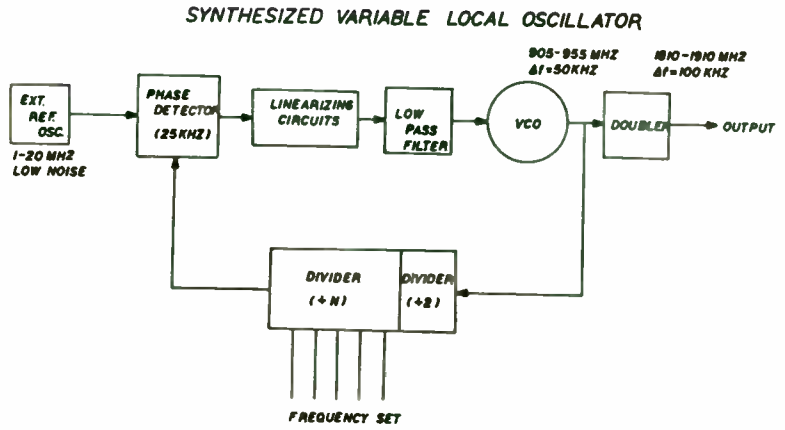


Figure 15

SYNTHESIZED OSCILLATOR PHASE NOISE

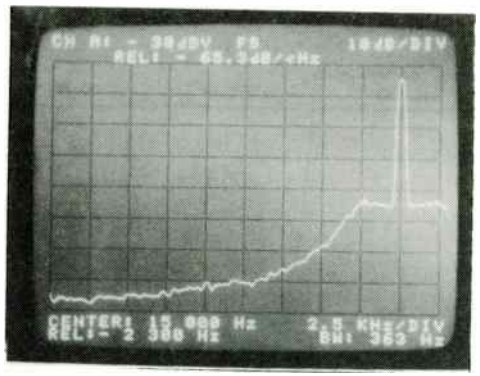


Figure 16

spurious level).

VI. The Future

The size of the filterbank presented here was 8.63 inches long by 6.5 inches wide and 0.81 inches deep. The area occupied by four of the PIN diode switches was 2.5 inches by 2.0 inches. Since the time that this filterbank was designed and built, Andersen has produced a hybridized version of the PIN diode switches that occupies an area of 1.25 inches by 0.75 inches and achieves better uniformity in a package that is less than half the size of the discrete unit. These switches were used in a four channel filterbank that measured 3.0 inches by 2.0 inches by .05 inches.

In the filterbank described here, the matching networks for the surface wave filters was external to the filter package. Since then, Andersen has produced filters with 60dB of rejection where the matching networks were hybridized and internal to the surface wave filter package. The trend toward future systems is for higher frequencies, smaller sizes and improved performances. Hybridized filterbanks achieving 80dB or more rejection at frequencies up to 1 GHz are realizable now and can be arranged to be screened to space qualification levels if desired. The combination of surface wave filters, with their ability to do complex signal processing in small sizes, and hybridized switching and amplifying networks makes small, rugged and reliable modules for the next generation of communications, radar and electronic warfare systems.

X-band. The antenna developed is a dielectric sphere (hemisphere) excited in two orthogonal circular polarizations generated using a septum polarizer. On the dielectric sphere antenna six metallic diffraction strips have been symmetrically placed. The width of the strips is experimentally adjusted such that we get around $\pm$ 65° beam width with maximum gain $\simeq$ +5 dBi at $\simeq \pm$ 65° and a null at the centre ($\simeq$ -7dB). A corrugated reflector flange has been used to shape the beam at the edges. The diffraction strips widen the beam and give a null at the centre and gain at $\pm$ 65°. The dielectric sphere maintains the E- and H- plane pattern symmetry. Since the strips are symmetrically placed the circular polarization remains unchanged. The antenna has been successfully developed. The practical antenna alongwith the pattern and the IRS Spacecraft is shown in Fig.12.

DIELECTRIC SPHERE ANTENNA AS A FEED FOR A REFLECTOR:

The antenna under discussion can be used as a prime focus feed for a reflector or a feed for a Cassegrain reflector antenna. The dielectric sphere antenna, with its good axial ratio, E- and H- plane pattern symmetry and low side lobes, can easily replace the conventional horn feed for Cassegrain reflectors.

The other applications of the dielectric sphere antenna can ba as a feed for a Compact Range Reflector and probes for near field measurements.

AS MICROWAVE APPLICATORS FOR MEDICAL USES:

Since the dielectric sphere antenna provides a focussed beam of circular cross-section with side lobes suppressed, the system can be used effectively as a microwave applicator for clinical/medical uses. A few of the applications are:

1) Applicator for diathermy (non-contact type) - the clinical technique used to achieve 'deep heating', that is inducing heat in tissues beneath the skin and subcutaneous fatty layers.

2) The system can be easily used for selective heating (re-warming) of cancer tumors in deeply cooled animals to enhance the effectiveness of tumor chemotherapy treatment. This technique is called differential hyperthermia.

3) These antennas can also be used for diagnosing and monitoring pathological cardio - pulmonary conditions.

The antenna system can be very effectively used in cases where focusing of electromagnetic energy for

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APPENDIX I

FILTER BANK SPECIFICATIONS

70 MHz nominal center frequency

Channel Number	3dB BW [1] (MHz)	IL [2] (dB)	Phase Linearity [3] max. (deg.)	Passband Ripple [4] max.(dB)	Fo (KHz)	Passband Symmetry [5]
1	0.1	29	±5	±0.5	N/A	±5%
2	0.3	34	±5	±0.5	±8.5	±8%
3	0.5	36	±5	±0.5	±8.5	±5%
4	0.75	38	±5	±0.5	±160	±5%
5	1.5	41	±5	±0.5	±160	±5%
6	4.0	45	±4	±0.5	±200	±5%
7	6.0	47	±4	±0.5	±250	±5%
8	12.0	50	±4	±0.5	±500	±5%

1. 3dB BW tolerance = ±5%, max.

2. IL tolerance = ±1dB, max.

3. Phase linearity is the phase deviation from the best linear fit over 80% of the 3dB BW.

4. Passband ripple is the amplitude ripple over 80% of the 3dB BW excluding monotonic roll off from the minimum loss point.

5. Passband symmetry calculated at 25°C by the following formula:

$$\text{symmetry} = \frac{f1 - f2}{f1 + f2} \times 100\%$$

where f1 = fo - lower 3dB frequency
f2 = fo + upper 3dB frequency
fo = 70 MHz

irradiation of biological organs is required. The comparative small size of the antenna makes it an excellent microwave applicator for clinical uses.

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mm/-

FILTER BANK SPECIFICATIONS

Rejection	80dB, minimum on all channels from 5 MHz to 400 MHz outside seven 3dB bandwidths from center frequency.
Shape Factor (all channels except 1 and 9)	60dB BW = 2.5, max. / 3dB BW 70dB BW = 3.0, max. / 3dB BW
VSWR (input and output)	1.6:1, max., over 60 to 80 MHz
Two Tone, Third Order Intermodulation	>70dB below any 2 tones within selected passband for all power levels up to -30dBm.
Input RF Power	All specifications to be met for any input power up to -30dBm. The unit shall withstand +20dBm CW without burnout.
Operating Temperatures	-20 °C to +50 °C
Channel Selection	Shall be by TTL signal according to the following table.

Channel	3dB BW (MHz)	A (MSB) 0	A 1	A 2	A (LSB) 3
1	0.1	0	0	0	0
2	0.3	0	0	0	1
3	0.5	0	0	1	0
4	0.75	0	0	1	1
5	1.5	0	1	0	0
6	4.0	0	1	0	1
7	6.0	0	1	1	0
8	12.0	0	1	1	1
9	Direct	1	0	0	1

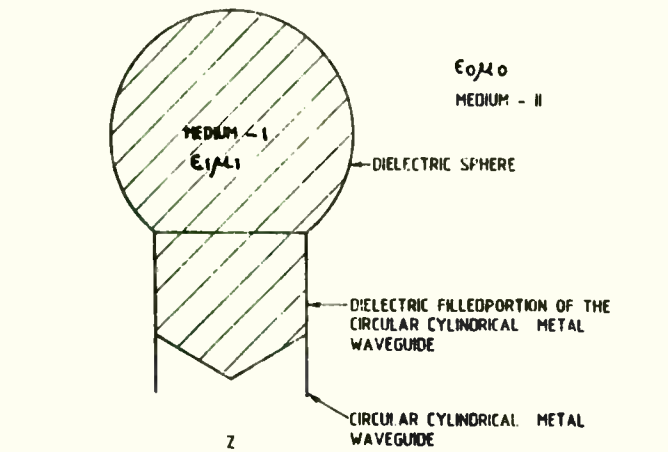
Differential Phase	Differential Phase between any 2 like filters over 80% of 3dB BW shall be 10 degrees, maximum.

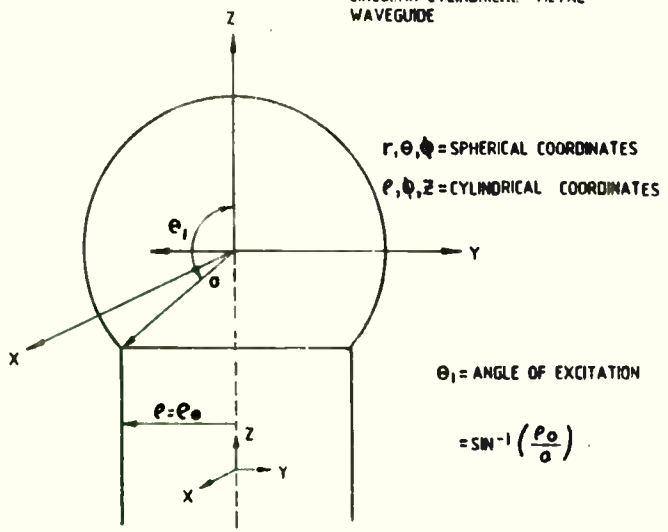
SYNTHESIZED OSCILLATOR SPECIFICATIONS

Tuning Cycle	Continuous
Tuning Range	1810.0 MHz to 1910.0 MHz in 0.1 MHz steps
Frequency Control	4 wire/digit BCD parallel logic, TTL compatible
Accuracy	Dependent upon and same as external reference
Harmonics	-40dBc
Spurious	-60dBc
Phase Stability	Using low noise, stable source for input:

Customer Supplied Source		Synthesizer Output	
Offset from Carrier (Hz)	Phase Noise* (dBc/Hz)	Offset from Carrier (Hz)	Phase Noise* (dBc/Hz)
10	-98	10	-55
100	-98	100	-55
1,000	-120	1,000	-60
10,000	-135	10,000	-80
above 10,000	-145	100,000	-95
		1,000,000	-105
		2,000,000	-115
		above 2 MHz	<-120

* Single sideband phase noise in 1 Hz bandwidth.





r,θ,ϕ = SPHERICAL COORDINATES

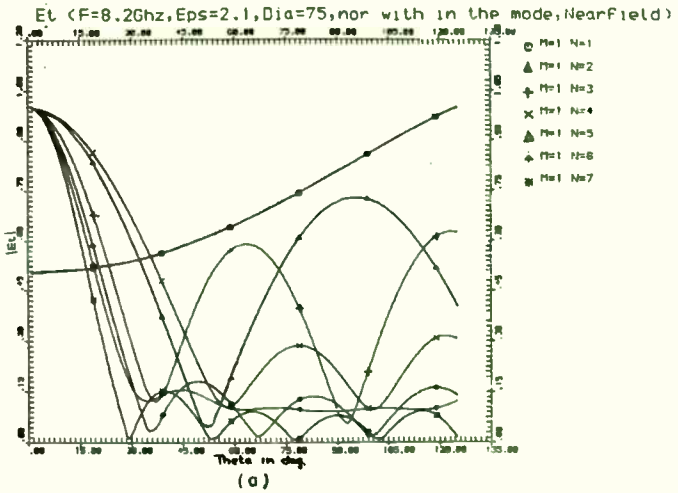
ρ,ϕ,z = CYLINDRICAL COORDINATES

θ_1 = ANGLE OF EXCITATION

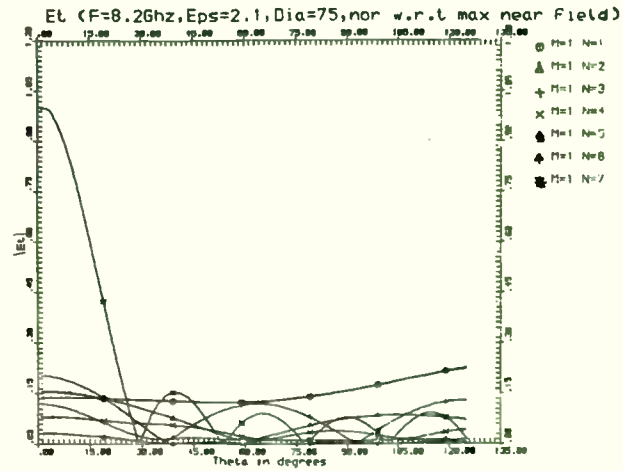
$= \sin^{-1}\left(\frac{\rho_0}{a}\right)$

FIG. 1 ANTENNA GEOMETRY

...3



(a)

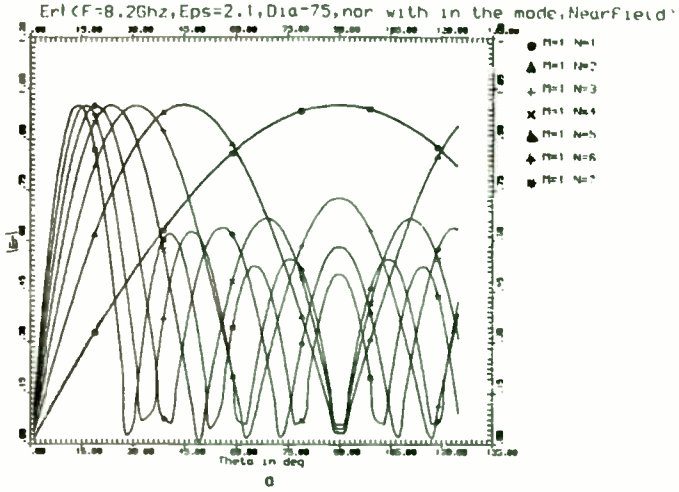


(b)

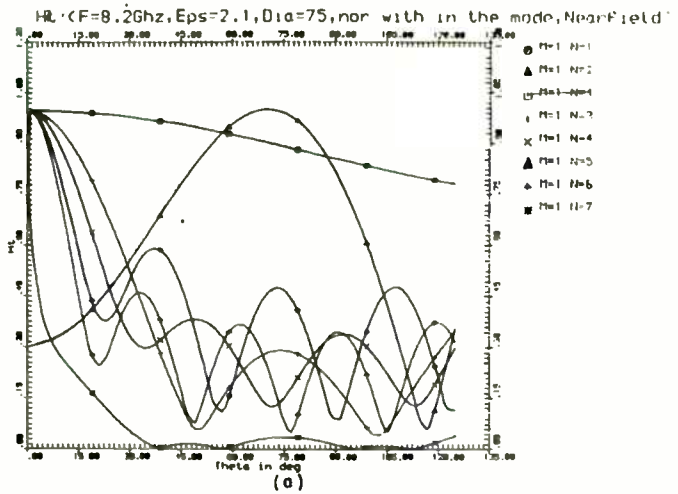
FIG 2-1

ENVIRONMENTAL CONDITIONS (OPERATING): SYNTHESIZER AND FILTER BANK

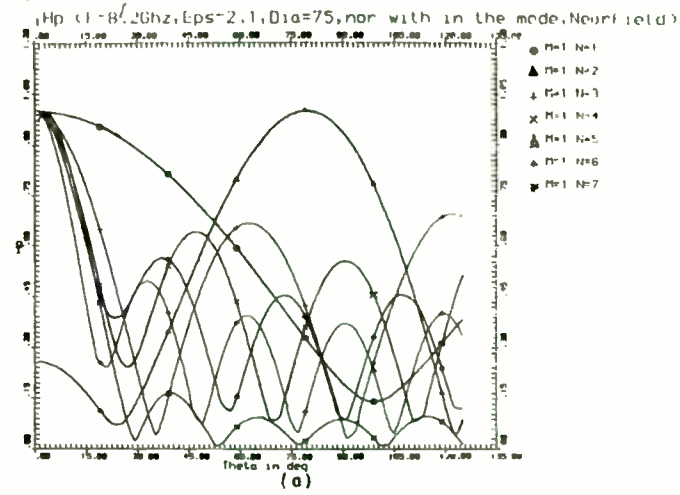
Altitude:	Sea level to 15,000 feet
Humidity:	MIL-STD-810, Method 507, Procedure I
Vibration:	MIL-STD-810, Method 514, Procedure IA, Figure 514.2-2 (W_o = 0.06 G^2/Hz from 15 to 2000 Hz)
Sand and Dust:	MIL-STD-810, Method 510, Procedure I
Shock:	MIL-STD-810, Method 516, Procedure V
Burn-in:	160 hours at +50 °C, powered



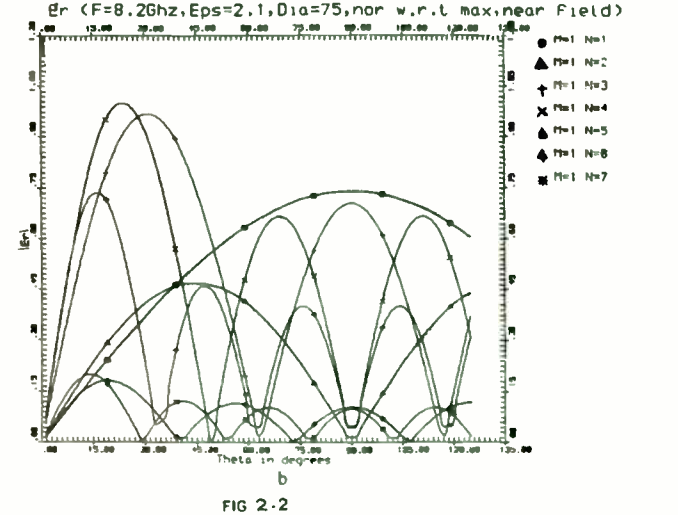
a



(a)

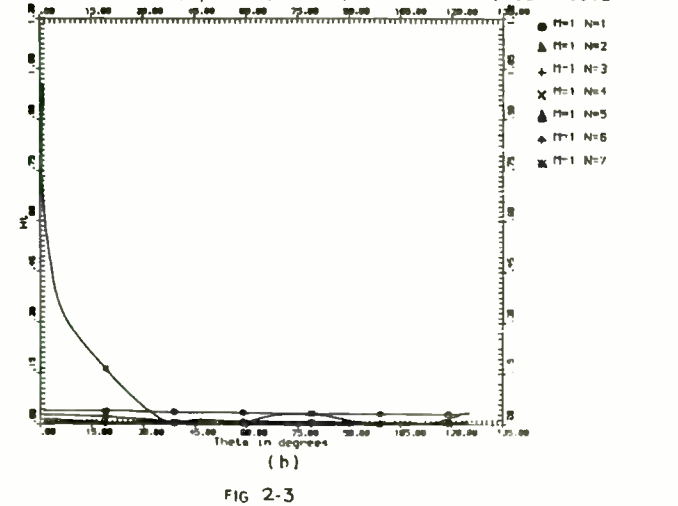


(a)



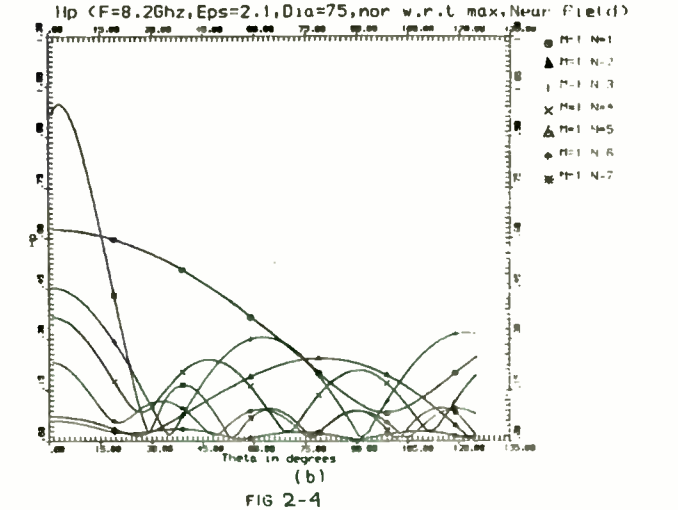
b

FIG 2-2



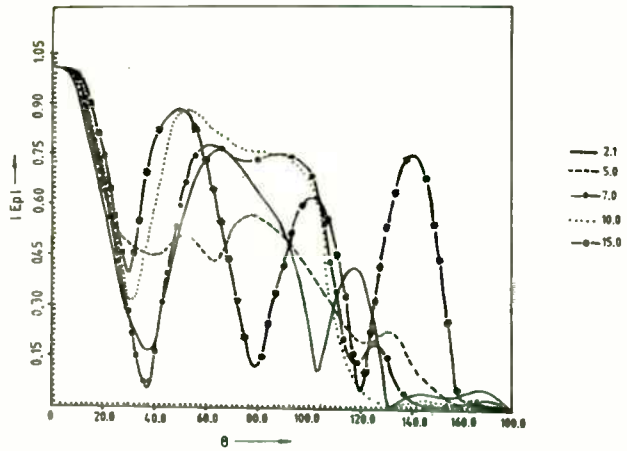
(b)

FIG 2-3

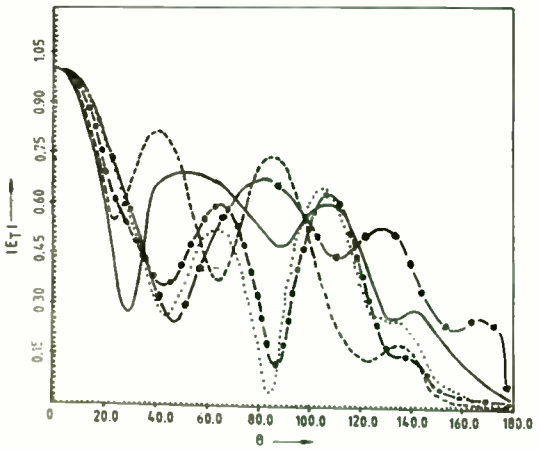


(b)

FIG 2-4

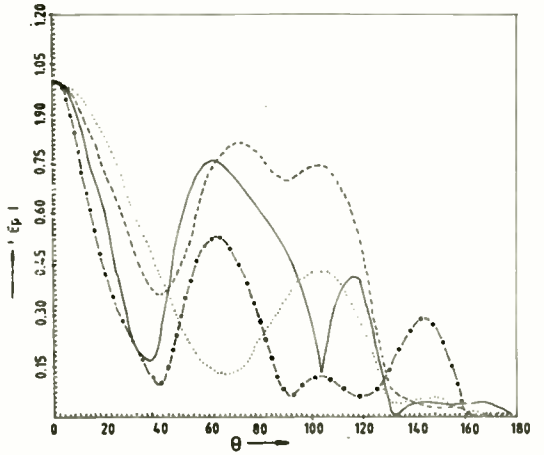


(a) Ep (F = 8.2 GHz, DIA= 75, Eps = 2.1, 5, 7, 10, 15)

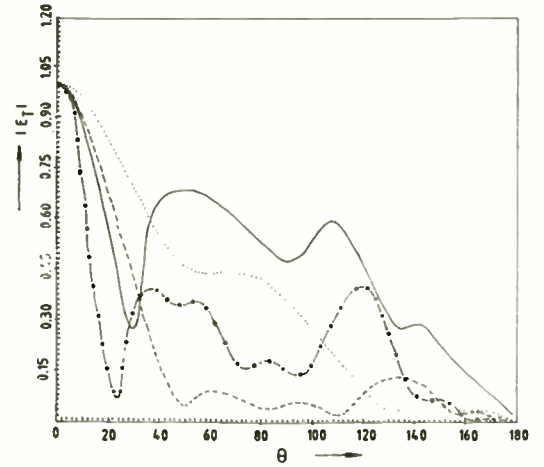


(b) E_T (F= 8.2, DIA= 75, Eps = 2.1, 5, 7, 10, 15)

FIG.3a RADIATION PATTERNS/FAR FIELD (THEORETICAL)

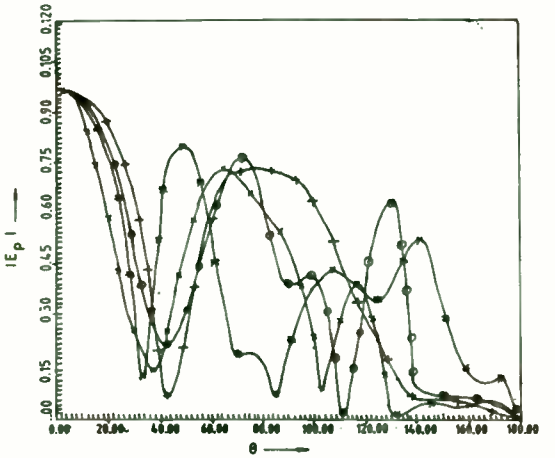


(a) Ep (F=8.2 GHz, Eps=2.1, DIA=100,75,50,30)

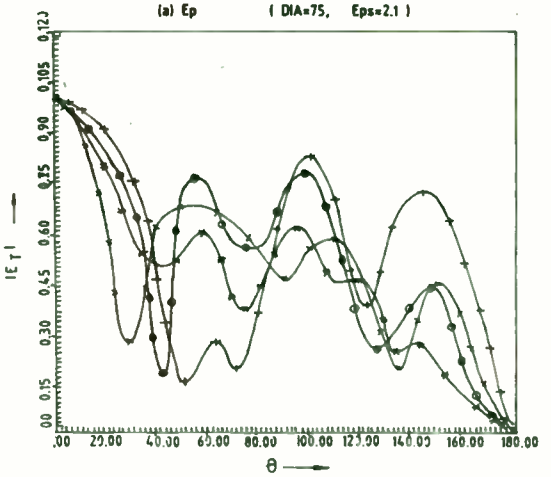


(b) E_T (F=8.2 GHz, Eps=2.1, DIA=100, 75,50,30)

FIG. 3c FAR FIELD RADIATION PATTERNS (THEORETICAL)



(a) Ep (DIA=75, Eps=2.1)



(b) E_T (DIA=75, Eps=2.1)

FIG.3b FAR FIELD RADIATION PATTERNS - THEORITICAL)

BANDPASS AND BANDSTOP FILTERS IN THE 100 TO 1000 MHZ FREQUENCY RANGE

or, "THE SEARCH FOR Q"

by

R.V.Snyder
RS Microwave Co., Inc.
November 12, 1986

1.0 Introduction

The frequency range between 100 and 1000 MHz has always posed special problems for the designer. Lumped element techniques are difficult to apply using conventional circuits because component values are of the order of parasitic levels, while distributed networks are too large for many applications.

Constructing networks which achieve economic and technical goals requires a compromise between size and Q. Certain approaches place greater constraints upon the quality of capacitive elements while others demand higher Q inductive elements. In this frequency range much can be accomplished by combining lumped and distributed components in one structure, taking the best of both. In order to do this, it is necessary to characterize inductive and capacitive elements. Surprisingly, capacitors are more of a problem than inductors, insofar as Q is concerned. Thus, some circuits employ lumped inductances combined with distributed capacitors. The "surprise" mentioned above is due to the lack of availability of high Q commercial lumped capacitors, contrary to what is indicated in the catalog of every capacitor manufacturer. Of course, some designs use lumped capacitors and distributed inductors.

In this paper we will discuss lumped minimum phase bandpass filters with essentially symmetrical skirts. These filters are interesting because most such bandpass filters require "extra" low pass or high pass elements to increase the slope of one side of the stop band or must be overdesigned with the shortcomings of the less steep skirt kept in mind.

We will discuss bandstop filters which are lumped "analogues" of distributed circuits, which would be too large for general use in the frequency range under discussion.

Examples of the various networks will be given.

2.0 Lumped Bandpass Filters

In this section, we will cover the following topics:

a. "Dumbell" or tubular types, semi-low pass
b. Capacitively coupled, semi-high pass (a la Cohn)
c. Alternating L-C for symmetrical response
d. Wide-band, i.e. greater than an octave
    1. Conventional
    2. Generalized Chebychev (for sharper skirts, smaller size, less loss)

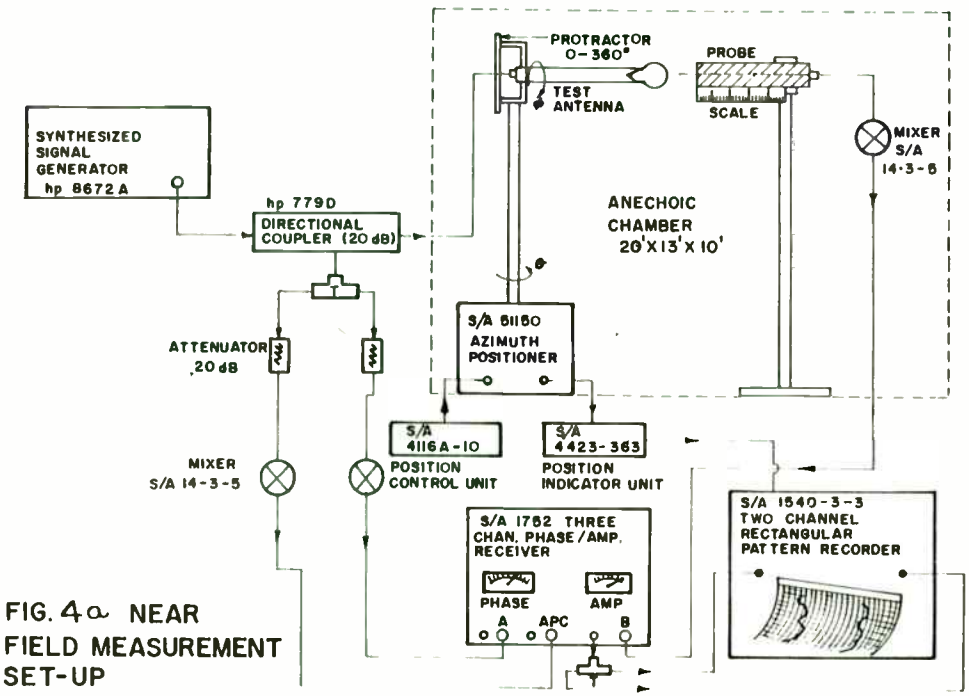


FIG. 4a NEAR FIELD MEASUREMENT SET-UP

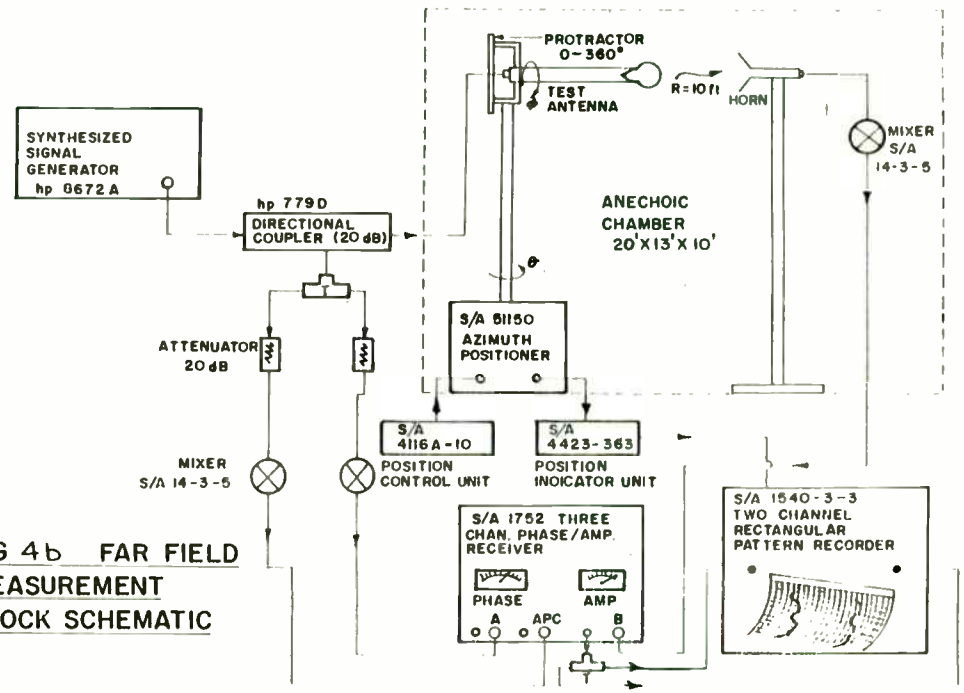


FIG 4b FAR FIELD MEASUREMENT BLOCK SCHEMATIC

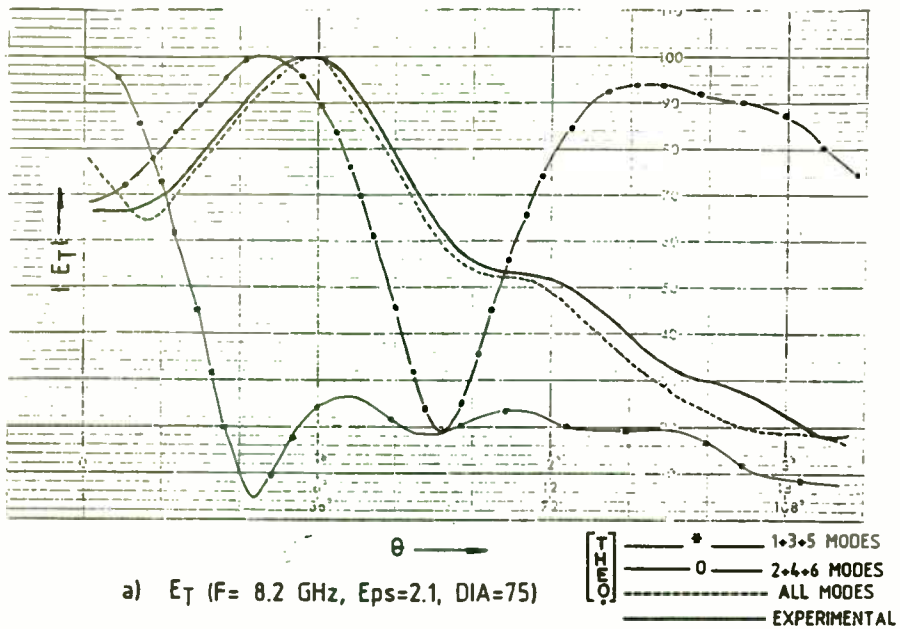
Figure 1 presents typical schematics and response characteristics for (a)-(c), above. The symmetrical response of (c) results from the alternation of the series L and C elements. Contrast the conventional network shown in Figure 2. This network is actually semi-high pass in nature, resulting in an upper stopband slope not as steep as the lower. In similar fashion, the tubular network is semi-low pass, with consequent degradation of the lower slope. The alternating approach achieves slope symmetry and thus avoids the necessity of overdesigning for a less steep characteristic on one side of the passband. Figure 3 describes the approach used for the more interesting and innovative network of (d)-2. These generalized Chebychev filters offer a small range of element impedances combined with the sharp skirts resultant from the finite frequency transmission zeroes located near the passband. Thus, these filters offer the realization advantages of conventional Chebychev filters with the sharp response of Elliptic Function designs. By realization advantage we mean that this design avoids the problem associated with a very large inductor coupled to a very small capacitor, or vice-versa. The transmission zeroes are "scientific" traps which cause great attenuation near the passband but with little effect on the passband. Figures 4 to 6 show the circuit and response characteristics for two different examples of generalized Chebychev low-pass high-pass cascades connected to achieve bandpass response. In these figures, the high attenuation near the passband edge is evident, as is the rippled nature of the stopband region. Power levels for filters of these types are relatively low, i.e. less than 10 watts for small units, somewhat higher if size can grow. Peak power levels can go to a Kw of so. Q values range from 80 for the ferrite loaded low frequency units to 500 or more for units operating in the 500 to 1000 MHz range.

3.0 Distributed element types

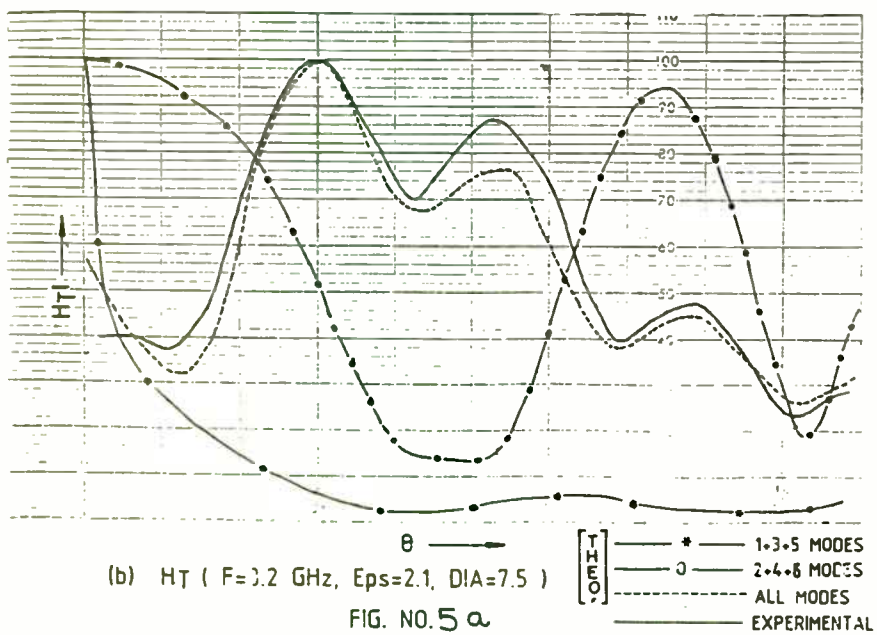
In this section, we will discuss the various types of distributed element (i.e. non-lumped element) filters that commonly are built. Our discussion will include:

a. Inductive, capacitive and iris couplings
b. Cavity filters-max bandwidth 10%, low loss,large
c. Helical resonators-small, inductively coupled
d. Printed quarter wave types.

Inductively coupled filters are typified by the helical resonator structures. Here, the resonant elements are wound coils which may be contained in a cavity. These coils have the electrical properties of a foreshortened quarter wavelength open circuited line. If the cavity encloses most of the coil, coupling from resonator to resonator occurs through an iris hole, and the inductively coupled design degenerates to an iris coupled one. Similarly, real capacitors may be used to couple the sections. As discussed in Section 2.0, inductive

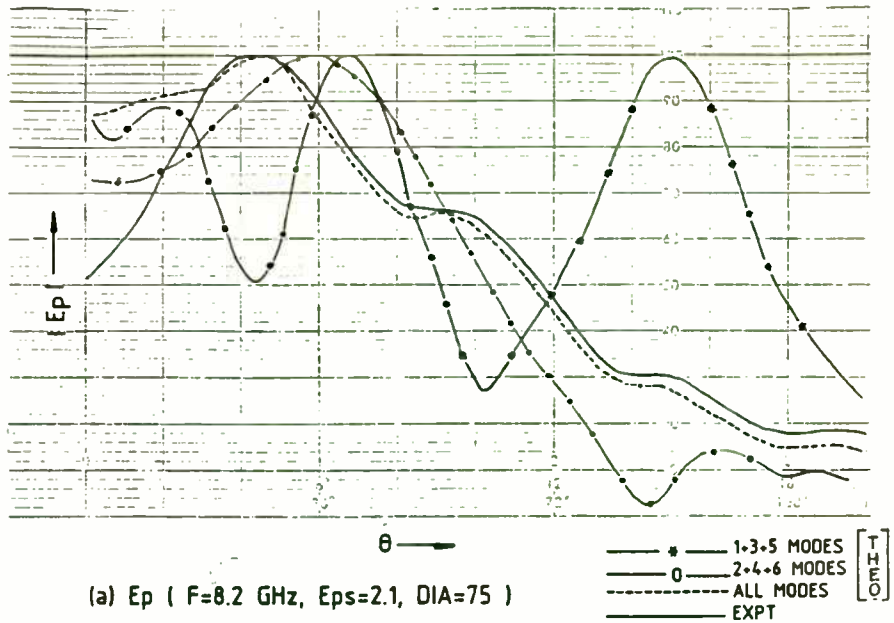


a) E_T (F= 8.2 GHz, Eps=2.1, DIA=75)

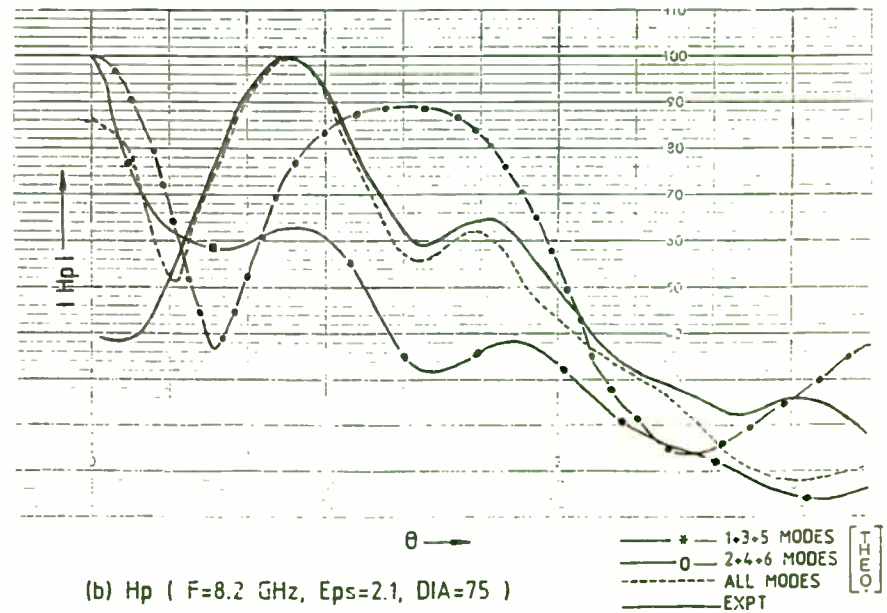


(b) H_T (F=8.2 GHz, Eps=2.1, DIA=7.5)

FIG. NO. 5 a



(a) Ep (F=8.2 GHz, Eps=2.1, DIA=75)



(b) Hp (F=8.2 GHz, Eps=2.1, DIA=75)

FIG. NO. 5 b

or capacitive coupling result in filters with non-symmetrical skirts. Proper iris configurations tend to achieve results similar to the alternating L-C design. Filters of this type are quite compact, but display Q values of only 200 to 500. This Q value is dependent upon the size of the confining cavity; however, this is limited by the incidence of unwanted or spurious modes of resonance if the size is too great.

If the resonators are effectively quarter wavelength open circuited lengths of coaxial line, and the line is constrained within a cavity, the resultant resonant cavities can be conveniently coupled with irises. Filters of this type are relatively large, but achieve unloaded Q values of 1000 to 2000. Therefore, the insertion loss of filters built using this approach is usually quite low. Also, this approach my be easily tuned by using a variable length for the center coaxial section.

A very interesting approach is the use of printed quarter wave lines in a variety of configurations. Figures 7 and 8 illustrate the design approach and response of such a filter. Although a printed design employs distributed line lengths, the dielectric loading reduces the physical size of such filters, at a cost of insertion loss. Unloaded Q levels of about 300 can be obtained. There are a wide variety of implementations available, including balanced suspended substrate, dielectric stripline, unbalanced microstrip, confined microstrip, etc. This is a study in itself. Suffice it to say that application of the technique is not indicated if the application is for a narrow band, temperature stable design or if the skirts are required to display monotonicity below 40 or 50 db.

4.0 Lumped-Distributed types

It is possible to construct filters using a combination of lumped and distributed elements. Although no general synthesis exists as a closed form design, combinations of the response characteristics of lumped and distributed elements results in compact and efficient filters. We will discuss two examples: evanescent mode and it's close relative, the comb line.

A simple comparison of the two approaches will explain why our discussion will really center on the evanescent design. The comb line filter employs coupled lines, with each line open circuit connected to a capacitor, which is in turn grounded. The equivalent electrical length of the line-capacitor combination is 90 degrees, resulting in a band pass filter response. The equivalent coupling network is derived using the assumption that a TEM wave is propagating in a slow-wave meander-line fashion through the filter. Thus, the Q of the structure is calculated from TEM assumptions and the consequent performance of the filter is based upon that calculation. Evanescent (GR. "Decaying Spirit") mode filters

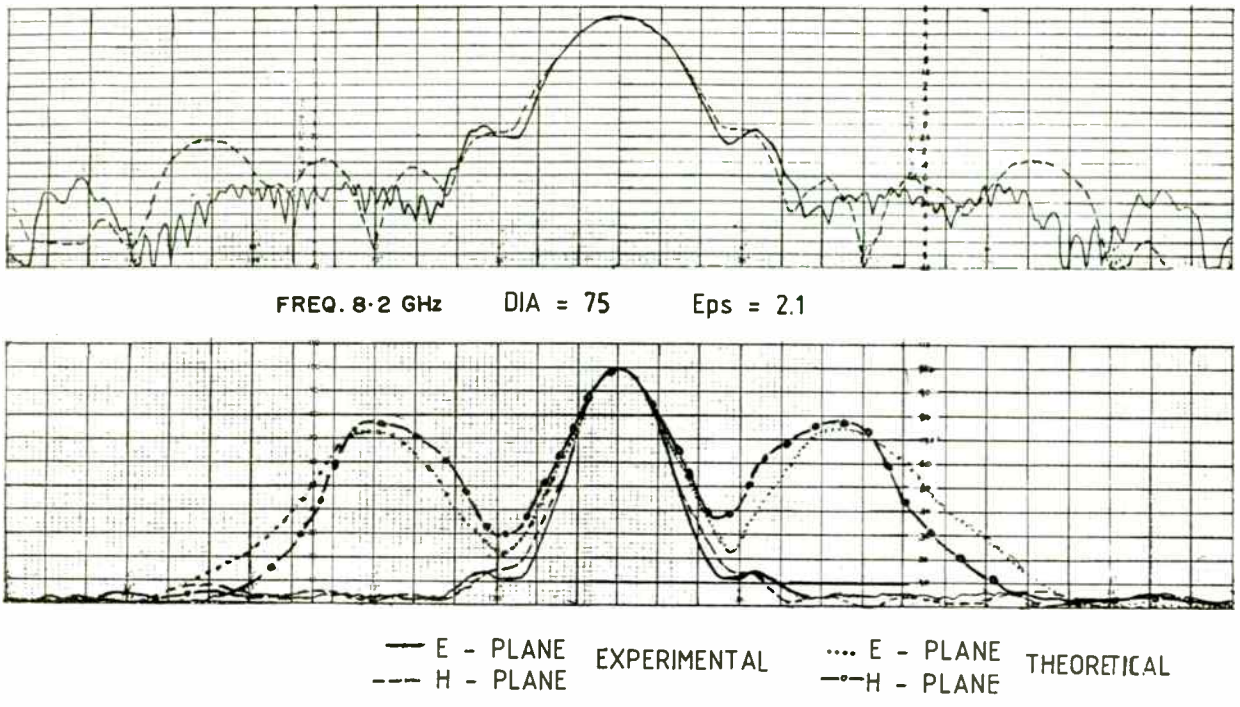


FIG. 6(a) FAR FIELD RADIATION PATTERN - EXPERIMENTAL / THEORETICAL

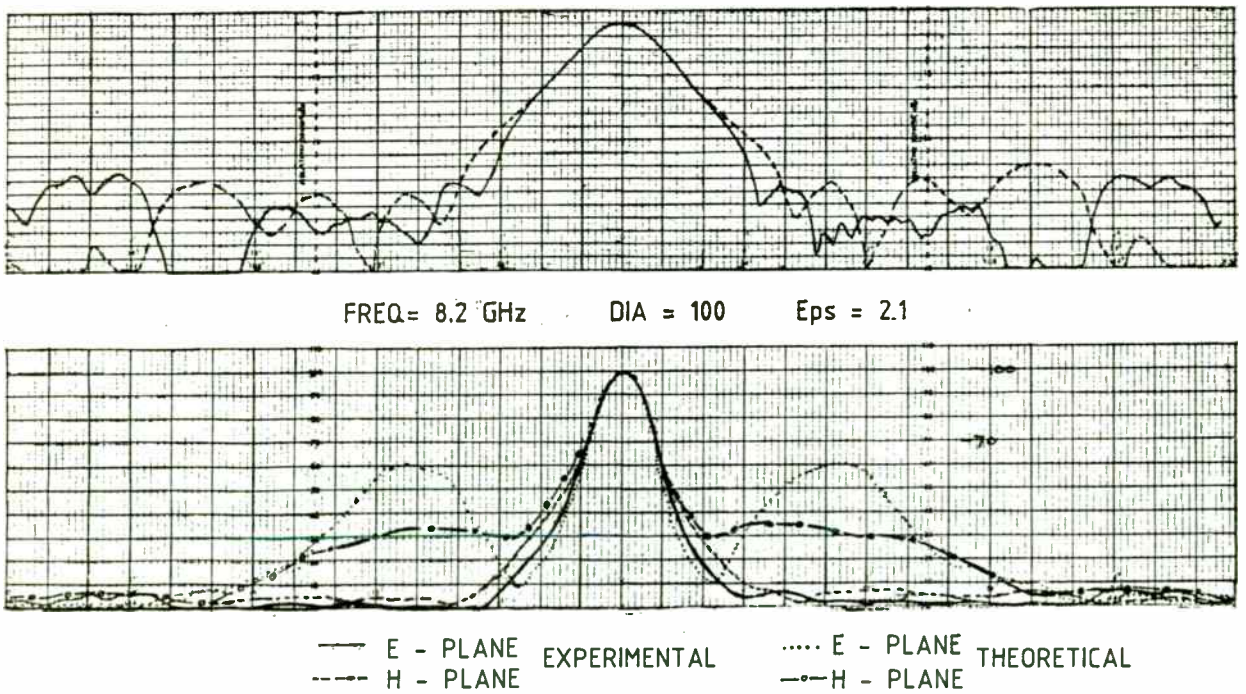


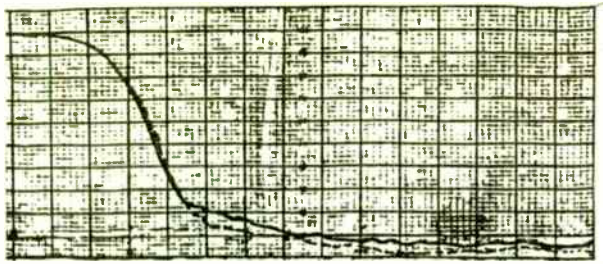
FIG. 6(b) FAR FIELD RADIATION PATTERN - EXPERIMENTAL / THEORETICAL

utilize the scattering of waves from obstactles placed in below-cutoff waveguide to form high Q inductively coupled bandpass filters. A waveguide structure has a normally high pass frequency characteristic. By this is meant that frequencies lower than the cut-off frequency cannot normally proceed from one end of the waveguide to the other. The waves encounter a high impedance proportional to the dimensions of the waveguide. Note that any empty tube is a waveguide structure with cut-off dependent upon the cross-sectional dimensions of the tube. The tube can be of any geometric closed shape, including rectangular, circular, etc. We can represent the high-impedance properties by a simple circuit. This is shown in Figure 9. This "Pi" of inductors contains three elements. The shunt inductors are proportional to the cut-off frequency of the tube, while the series element is proportional to the length of the tube. If we resonate the shunt elements with capacitors and then cascade a numer of these sections, we obtain the illustrated bandpass filter.

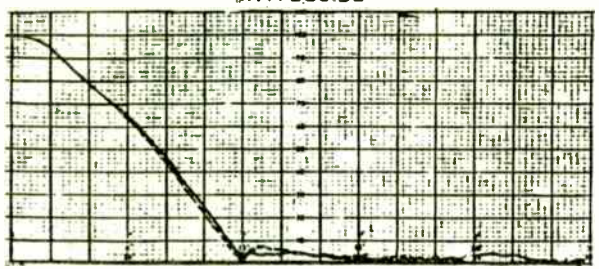
Well, so what? How does this help us to achieve superior filters? Let us look further at the properties of a rectangular waveguide. The dominant mode (lowest possible frequency of operation) propagates through the waveguide in a very low loss manner. We can say that the losses associated with resonance are very low. As we decrease the frequency below cut-off, the losses increase, but they were low to start with. Thus, although the evanescent filter operates below cut-off, the associated losses are low-as the computed Q started with a dominant waveguide mode assumption, not a TEM one. Further, the waveguide will not allow non-resonated frequencies to propagate through until a frequency well above cut-off is reached. By building the filter in a waveguide small enough (i.e. operating far below cut-off), one can build low loss filters with very high stopband to passband width ratios. In short, the evansecent filter can have very wide stopbands and is thus suited to wide spectrum applications. Such filters may be built with waveguide, connectors, pins or with combinations. Many such filters handle high power. The technique is applicable from 10 MHz to at least 40 GHz, for bandwidths from 1% to 80% Examples of both comb and evanescent filters will be given. Power levels can be as great as a few hundred watts with proper design of the resonators and loading capacitors. Q values can be 300 to 1000 for compact filters over the entire frequency range.

5.0 Equalizers

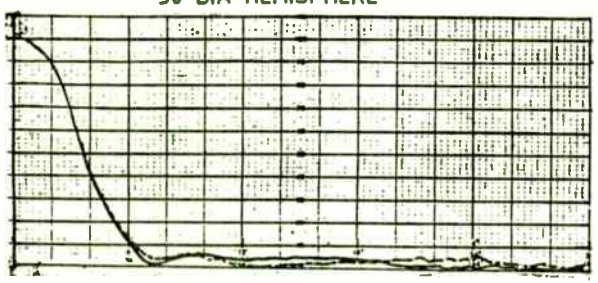
The section on bandstop filters (Sec. 6.0) will discuss amplitude equalization. Here, we will cover delay equalization of bandpass filters. We will show a slide in



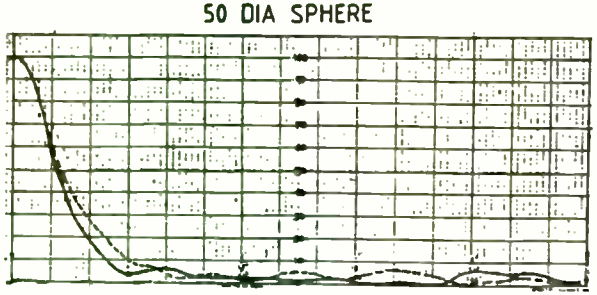
WAVEGUIDE



30 DIA HEMISPHERE



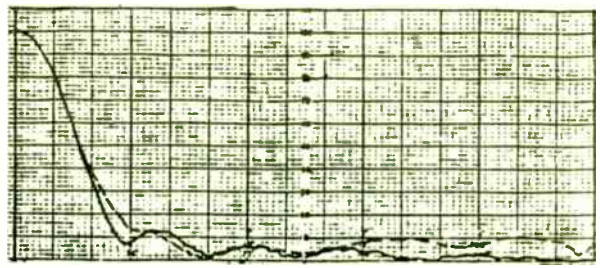
50 DIA SPHERE



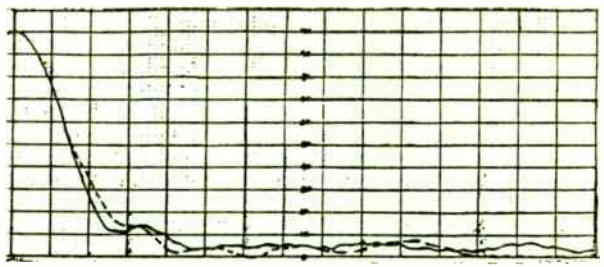
100 DIA SPHERE

E PLANE ——
H PLANE ----

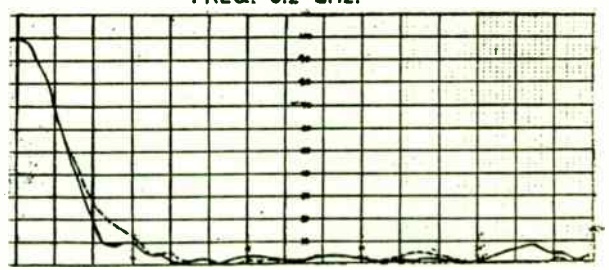
FIG.NO. 7(a) FAR FIELD RADIATION PATTERNS EXPERIMENTAL
FREQ.= 8.2 GHz Eps=2.1



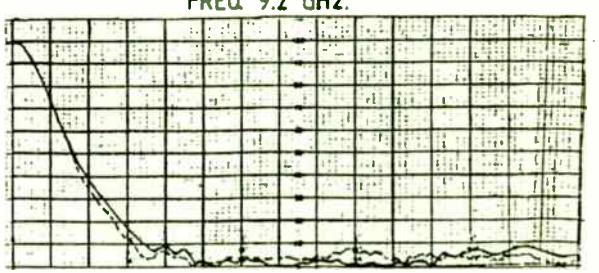
FREQ. 7.2 GHz.



FREQ. 8.2 GHz.



FREQ. 9.2 GHz.



FREQ. 10.2 GHz.

E PLANE ——
H PLANE ----

FIG. NO. 7(b) FAR FIELD RADIATION PATTERNS – EXPERIMENTAL
DIA=75 Eps=2.1

which a bridged-tee lumped all-pass network is hooked in series with a Chebychev bandpass filter. The all-pass network adds "bumps" to the group delay characteristic of the combination without affecting the amplitude shape. A 100 MHz equalized filter will be shown and discussed.

6.0 Bandstop filters.

In this section we will cover:

a. Distributed parallel coupled and capacitively coupled filters

b. Lumped bandstop filters, using low pass and high pass sections as inverters between resonators.

Figure 9A presents the schematics for both distributed and lumped bandstop filters. Figures 10 through 12 present the response characteristics for filters of this type. The lumped analogues have very similar characteristics to the distributed prototype units. Figure 13 shows a transformation from the simple open circuit case to an easier-to-build version using short circuited capacitors to foreshorten the resonators, in the same way that comb-line bandpass filters are achieved. A slide will be shown in which the basic distributed circuit is realized as a parallel-coupled air-strip line structure. This latter approach is useful when high power (several Kw) is a requirement.

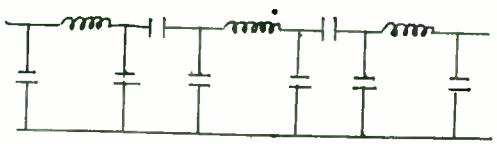
If the Q of the bandstop filter is intentionally reduced, the ultimate attenuation of the bandsop filter is reduced. As well, the stopband becomes non-reflective as the low Q circuit absorbs the energy, rather than reflecting it. This phenomena is useful for building amplitude equalizers. In this application, it is desired to have a shaped amplitude characteristic without sacrificing VSWR. Several examples will be given.

7.0 Conclusions

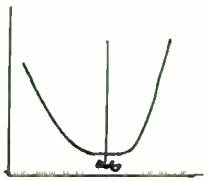
We have tried to show that diversity is the name of the game in the 100 to 1000 MHz range. Many problems are faced in achieving small size and low loss. Element Q values are critical, and commercial capacitive elements are just not compatible with the impedance levels required within the filters. Ohmic losses within the capacitors are worsened due to the low filter impedances, in some applications. A variety of techniques have been presented which should enable the budding designer to "leap" into the field, hopefully with new ideas.

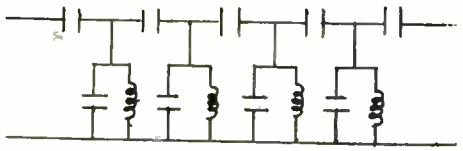
FIG. 8(a) ROTATING DIPOLE PATTERN (FREQ. 8.2 GHz)

FIG. 8(b) ROTATING DIPOLE PATTERN (FREQ. 8.25 GHz)

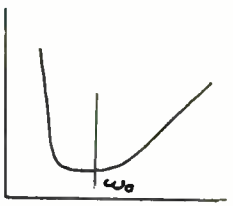


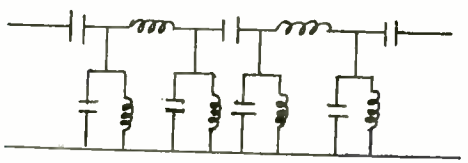
TUBULAR "DUMBELL"
BANDPASS FILTER





CAPACITIVELY COUPLED
BANDPASS FILTER





ALTERNATING L-C
BANDPASS FILTER

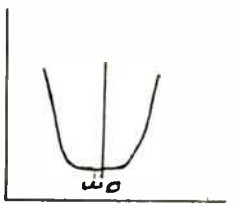


FIG. 1

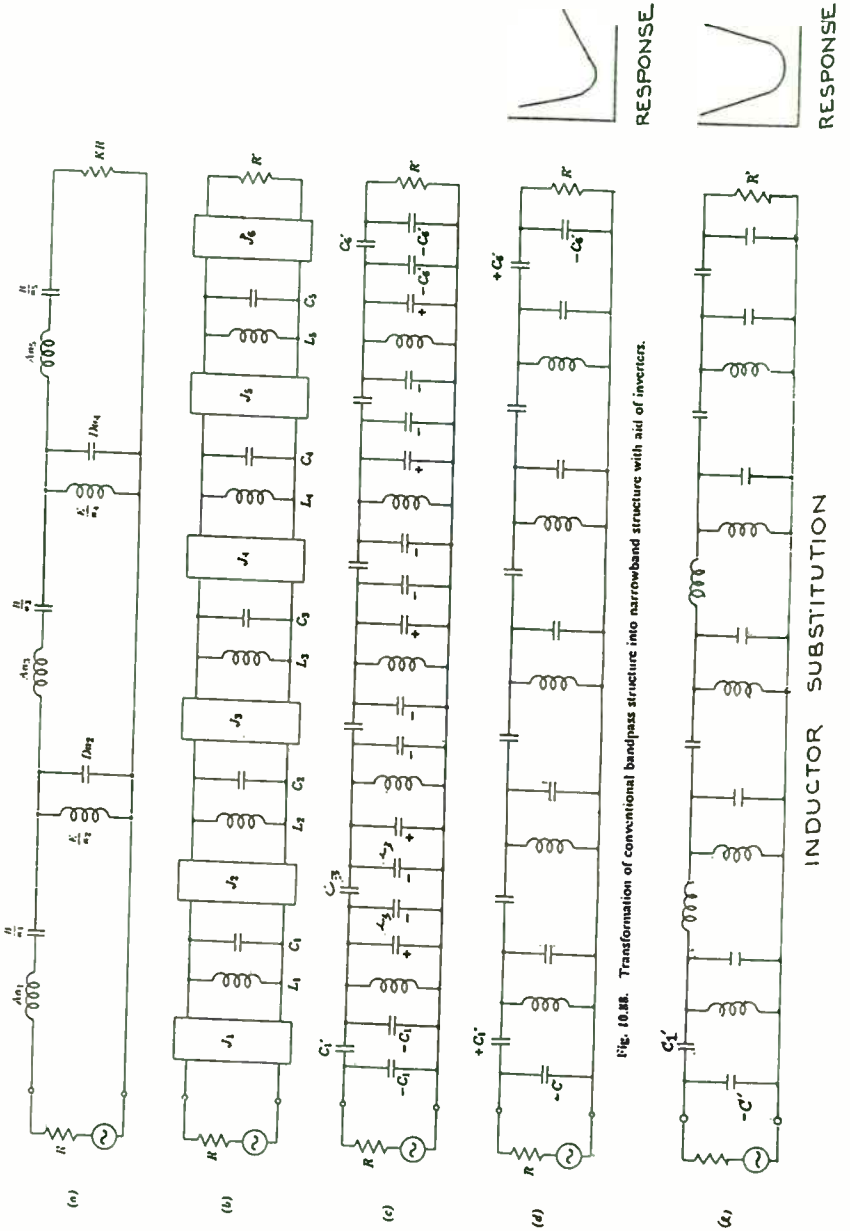


Fig. 10.88. Transformation of conventional bandpass structure into narrowband structure with aid of inverters.

FIG. 2

TABLE - I

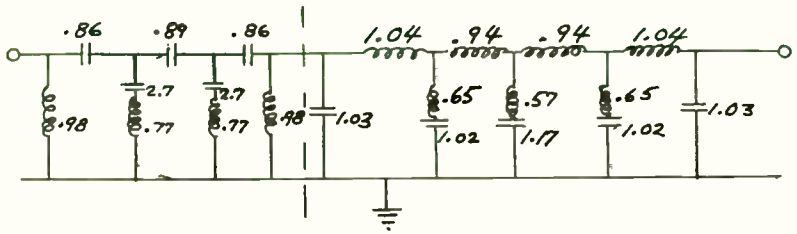
Sl.No.	DESCRIPTION	7.2 GHz	8.2 GHz	9.2 GHz	10.2 GHz
1.	WAVEGUIDE - GAIN IN DB				
	a) MEASURED	6.7	10.2	9.5	10.6
	b) UNIFORM APERTURE	7.08	8.24	9.2	10.1
2.	30mm dia - GAIN IN DB				
	a) MEASURED	10.7	13.4	10.5	12.3
	b) OPTIMISED	11.7	14.6	-	-
	c) UNIFORM APERTURE	7.08	8.24	9.2	10.1
	d) THEORETICAL	-	14.48	-	-
3.	50mm dia - GAIN IN DB				
	a) MEASURED	12.5	14.4	14.8	12.6
	b) OPTIMISED	14.5	16.4	15.4	13.7
	c) UNIFORM APERTURE	11.5	12.7	13.7	14.6
	d) THEORETICAL	-	13.25	-	-
4.	75mm dia - GAIN IN DB				
	a) MEASURED	16.0	17.6	18.0	16.3
	b) OPTIMISED	16.7	18.3	18.6	17.0
	c) UNIFORM APERTURE	15.0	16.2	17.2	18.9
	d) THEORETICAL	-	14.28	-	-
5.	100mm dia - GAIN IN DB				
	a) MEASURED	16.5	17.3	16.8	16.3
	b) OPTIMISED	18.9	17.7	17.9	16.6
	c) UNIFORM APERTURE	17.5	18.7	19.6	20.6
	d) THEORETICAL	-	16.89	-	-

T A B L E - II

Sl.No.	SPHERE DIAMETER	AXIAL RATIO IN dB		GAIN IN dB	
		WAVEGUIDE & SPHERE	WAVEGUIDE CHOKE & SPHERE	SPHERE & W/G	W/G + SPHERE & CHOKE POSITION OPTIMISED
1.	30mm dia	1.5	1.0	13.4	14.8
2.	50mm dia	1.0	0.8	14.4	16.9
3.	75mm dia	1.0	0.5	17.6	18.6
4.	100mm dia	2.0	1.8	17.3	17.9

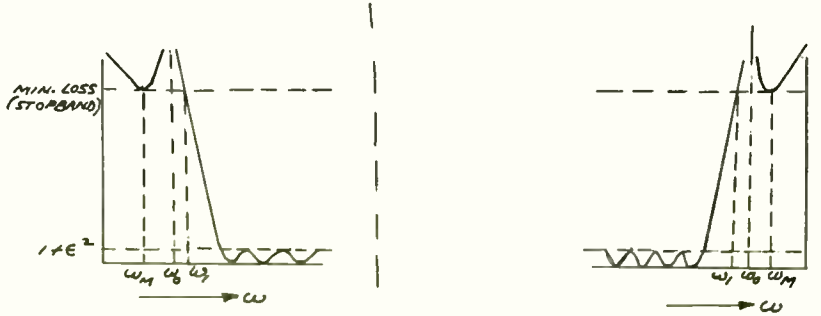
FREQUENCY : 8200 MHz

ε_r : 2.1



HIGH PASS
N = 7
MIN. α = 50 db
$\omega_0 = 0.69$
$\omega_1 = 0.75$

LOW PASS
N = 9
MIN α = 50 db
$\omega_0 = 1.23$
$\omega_1 = 1.14$



GENERALIZED CHEBYCHEV LOW PASS -HIGH PASS

BEFORE DENORMALIZATION

FIG. 3

REQUIRED PASSBAND: 20 TO 480 MHz

INSERTION LOSS: 2.5 db max

STOPBAND: 60 db min at 10 MHz and 560 MHz, up to 1200 MHz

SNYDER 2/17/86
"J ±80 MHz LP WITH N=11 AND HP WITH N=7

RL	50
PL	3.3E-07
SR	.5
	100
SC	1.28E-10
SRLCP	R= .5 L= 2.72E-07 C= 6.21E-10
	6.21E-10
SR	.5
	100
SC	1.28E-10
SRLCP	R= .5 L= 2.72E-07 C= 6.21E-10
	6.21E-10
SR	.5
	100
SC	1.28E-10
PL	3.3E-07
PC	6.1E-12
SR	.5
	100
SL	1.6E-08
SRLCP	R= .5 L= 1.17E-08 C= 6.1E-12
	6.1E-12
SR	.5
	100
SL	1.6E-08
SRLCP	R= .5 L= 9.8E-09 C= 7.2E-12
	7.2E-12
SR	.5
	100
SL	1.6E-08
SRLCP	R= .5 L= 9.8E-09 C= 7.2E-12
	7.2E-12
SR	.5
	100
SL	1.6E-08
SRLCP	R= .5 L= 1.17E-08 C= 6.1E-12
	6.1E-12
SR	.5
	100
SL	1.6E-08
PC	6.1E-12
RS	50

VS

FREQUENCY	INSERTION LOSS		RETURN LOSS		INPUT IMPEDANC
(HZ)	(DB)	ANGLE	(DB)	ANGLE	REAL +J(REACT)
1.0000E+07	-62.34	+151.8	-0.61	-74.4	2.79 37.90
2.0000E+07	-1.41	+31.5	-18.27	+97.5	50.10 -12.31
3.0000E+07	-0.52	+196.6	-22.63	-155.5	57.09 3.51
4.0000E+07	-0.44	+255.2	-26.83	+112.4	51.58 -4.36
5.0000E+07	-0.43	+289.7	-30.54	+12.1	47.17 -0.59
6.0000E+07	-0.42	+313.9	-30.96	-59.1	48.51 2.36
7.0000E+07	-0.41	+332.8	-30.86	-119.0	51.34 2.57
8.0000E+07	-0.40	+348.5	-29.02	-168.8	53.59 0.74
9.0000E+07	-0.39	+2.1	-26.60	+156.9	54.46 -2.00
1.0000E+08	-0.39	+14.4	-24.60	+133.1	53.98 -4.66
1.1000E+08	-0.40	+25.6	-23.14	+115.0	52.60 -6.67
1.2000E+08	-0.40	+36.1	-22.14	+100.4	50.82 -7.86
1.3000E+08	-0.41	+46.1	-21.51	+88.1	49.03 -8.30
1.4000E+08	-0.41	+55.6	-21.19	+77.5	47.46 -8.14
1.5000E+08	-0.42	+64.9	-21.14	+68.1	46.24 -7.58
1.6000E+08	-0.42	+73.9	-21.36	+60.0	45.42 -6.78
1.7000E+08	-0.42	+82.7	-21.82	+53.0	44.98 -5.86
1.8000E+08	-0.43	+91.5	-22.54	+47.3	44.92 -4.95
1.9000E+08	-0.43	+100.2	-23.53	+43.3	45.19 -4.15
2.0000E+08	-0.43	+108.9	-24.77	+41.6	45.73 -3.52
2.1000E+08	-0.43	+117.6	-26.20	+43.4	46.46 -3.14
2.2000E+08	-0.44	+126.3	-27.58	+50.0	47.29 -3.03
2.3000E+08	-0.44	+135.1	-28.40	+61.7	48.12 -3.22
2.4000E+08	-0.45	+144.0	-28.18	+74.6	48.84 -3.68
2.5000E+08	-0.46	+153.0	-27.12	+84.1	49.36 -4.33
2.6000E+08	-0.48	+162.1	-25.83	+88.5	49.61 -5.08
2.7000E+08	-0.49	+171.4	-24.68	+89.2	49.58 -5.81
2.8000E+08	-0.51	+180.8	-23.80	+87.6	49.32 -6.39
2.9000E+08	-0.52	+190.5	-23.24	+84.6	48.89 -6.74
3.0000E+08	-0.54	+200.4	-23.00	+80.9	48.42 -6.81
3.1000E+08	-0.56	+210.5	-23.08	+77.2	48.02 -6.60
3.2000E+08	-0.57	+221.0	-23.49	+73.9	47.79 -6.17
3.3000E+08	-0.59	+231.9	-24.23	+71.9	47.80 -5.61
3.4000E+08	-0.61	+243.1	-25.25	+72.1	48.10 -5.02
3.5000E+08	-0.63	+254.9	-26.40	+75.9	48.64 -4.52
3.6000E+08	-0.66	+267.2	-27.31	+83.7	49.35 -4.23
3.7000E+08	-0.70	+280.0	-27.55	+93.5	50.08 -4.20
3.8000E+08	-0.74	+293.6	-27.12	+101.2	50.67 -4.39
3.9000E+08	-0.78	+308.0	-26.53	+104.6	50.99 -4.66
4.0000E+08	-0.84	+323.3	-26.22	+104.6	51.02 -4.84
4.1000E+08	-0.90	+339.7	-26.36	+103.0	50.86 -4.78
4.2000E+08	-0.97	+357.4	-26.87	+100.9	50.66 -4.52
4.3000E+08	-1.07	+16.8	-27.39	+97.0	50.34 -4.27
4.4000E+08	-1.19	+38.1	-27.55	+83.6	49.36 -4.12
4.5000E+08	-1.34	+62.0	-26.65	+48.9	46.92 -3.30
4.6000E+08	-1.57	+89.2	-22.76	-0.9	43.22 0.10
4.7000E+08	-1.92	+120.9	-17.72	-43.9	40.82 7.49
4.8000E+08	-2.45	+158.7	-14.92	-80.2	44.25 16.17
4.9000E+08	-3.34	+208.5	-18.45	-84.3	47.49 11.46
5.0000E+08	-7.32	+278.3	-6.60	-57.7	22.74 22.99
5.1000E+08	-16.83	+335.0	-2.12	-103.9	15.61 61.49
5.2000E+08	-27.27	+7.1	-1.16	-133.1	20.54 112.18
5.3000E+08	-37.48	+27.6	-0.80	-152.8	39.86 198.85
5.4000E+08	-47.78	+41.9	-0.60	-167.5	132.34 414.12
5.5000E+08	-58.63	+52.0	-0.48	-179.2	1716.83 422.24
5.6000E+08	-70.63	+58.1	-0.39	+171.0	170.01 -588.91
5.7000E+08	-84.82	+59.2	-0.33	+162.7	41.14 -324.27
5.8000E+08	-103.46	+49.9	-0.28	+155.5	17.73 -229.28
5.9000E+08	-133.45	+356.2	-0.24	+149.2	9.75 -180.31
6.0000E+08	-155.09	+345.1	-0.21	+143.5	6.12 -151.48

FIG. 4

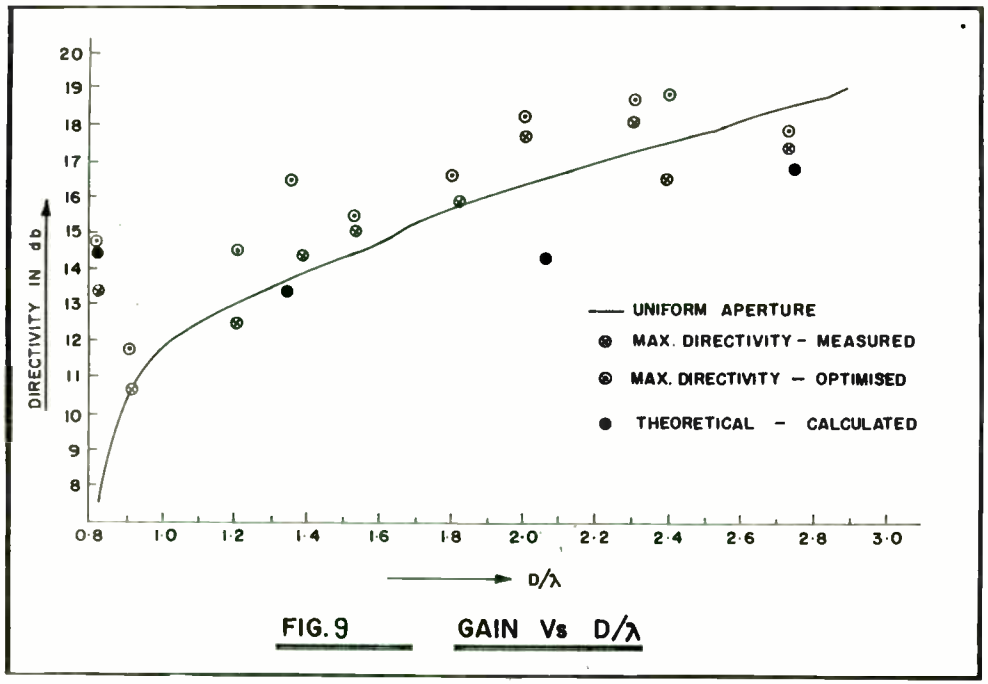


FIG. 9 GAIN Vs D/λ

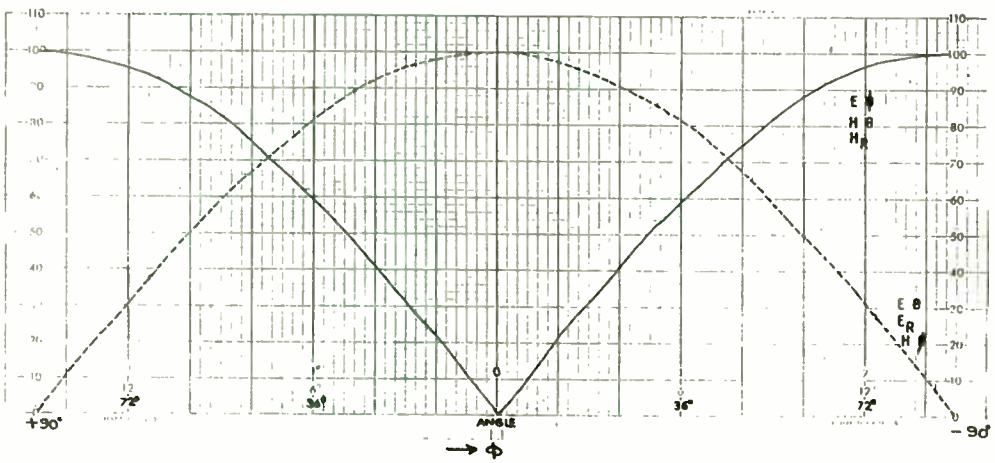
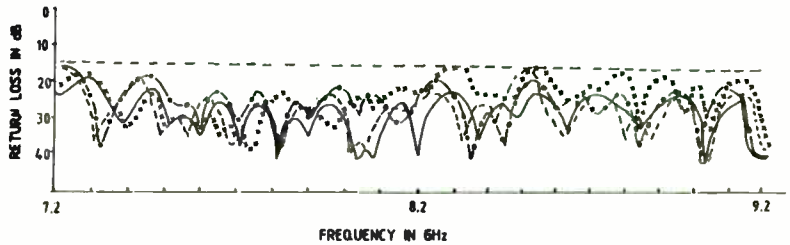


FIG. 10 VARIATION OF SOURCE FIELD COMPONENTS WITH φ



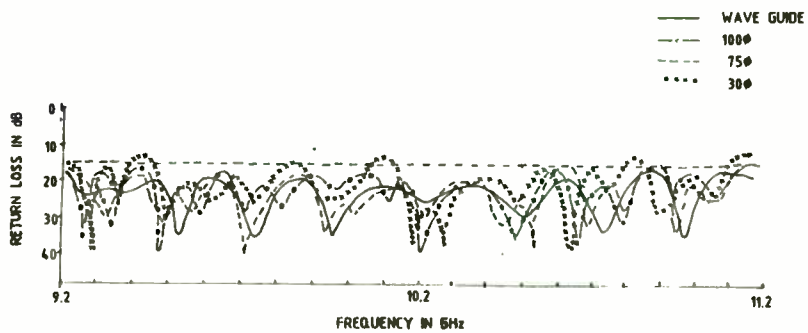


FIG. 11 RETURN LOSS OF THE ANTENNA SYSTEM

```
R. V. SNYDER     11/6/85
60 TO 160 MHZ LP WITH N=9 AND HP WITH N=7
                 RL              50
 1               PL              1.34E-07
 2               SR              .4
 0                               100
 3               SC              4.7E-11
 4               SRLCP           R= .4 L= 1.05E-07  C= 1.6E-10
 0                               1.6E-10
 5               SC              4.7E-11
 6               SR              .8
 0                               100
 7               SRLCP           R= .4 L= 1.05E-07  C= 1.6E-10
 0                               1.6E-10
 8               SC              4.7E-11
 9               SR              .8
 0                               100
 10              PL              1.3E-07
 11              PC              2E-11
 12              SL              5.12E-08
 13              SR              .8
 0                               100
 14              SRLCP           R= .4 L= 3.2E-08  C= 2E-11
 0                               2E-11
 15              SL              4.63E-08
 16              SR              .4
 0                               100
 17              SRLCP           R= .8 L= 2.8E-08  C= 2E-11
 0                               2E-11
 18              SL              4.63E-08
 19              SR              .4
 0                               100
 20              SRLCP           R= .8 L= 3.22E-08  C= 2E-11
 0                               2E-11
 21              SL              5.12E-08
 22              SR              .4
 0                               100
 23              PC              1.5E-11
                 RS              50
```

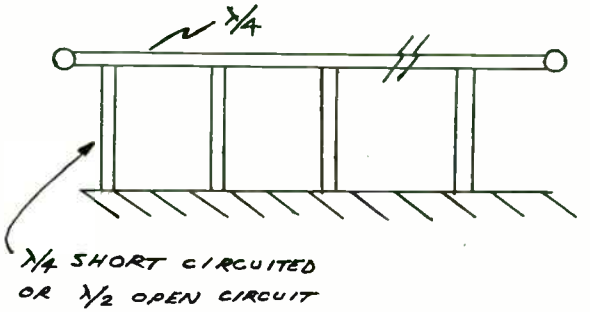
FREQUENCY	INSERTION LOSS		RETURN LOSS		INPUT IMPEDANCE	
(HZ)	(DB)	ANGLE	(DB)	ANGLE	REAL	+J(REACT)
1.0000E+07	-71.70	+122.9	-0.65	-47.5	2.24	21.97
2.0000E+07	-55.87	+158.4	-0.52	-98.9	3.55	58.34
3.0000E+07	-52.44	+198.4	-0.33	-157.6	25.17	250.46
4.0000E+07	-72.10	+283.8	-0.23	+133.2	4.15	-115.54
5.0000E+07	-17.07	+339.4	-0.84	+39.6	2.74	-17.96
6.0000E+07	-1.05	+153.0	-19.67	-8.9	40.67	1.32
7.0000E+07	-0.69	+242.3	-33.22	+25.4	48.06	-0.90
8.0000E+07	-0.63	+300.8	-20.84	+6.5	41.72	-0.87
9.0000E+07	-0.60	+347.4	-22.55	-61.8	46.21	6.10
1.0000E+08	-0.60	+28.5	-27.00	-150.7	54.00	2.37
1.1000E+08	-0.65	+67.3	-27.80	+100.7	50.60	-4.06
1.2000E+08	-0.73	+105.8	-24.48	+12.5	44.48	-1.15
1.3000E+08	-0.85	+146.2	-21.24	-40.6	43.56	4.95
1.4000E+08	-1.06	+191.6	-17.79	-51.0	41.71	8.50
1.5000E+08	-1.90	+246.9	-9.33	-67.6	32.07	22.94
1.6000E+08	-4.17	+310.4	-4.22	-114.7	35.91	64.63
1.7000E+08	-5.87	+59.6	-7.89	-126.2	61.01	47.38
1.8000E+08	-29.62	+159.0	-0.69	-158.2	53.45	248.37
1.9000E+08	-55.84	+179.1	-0.35	+177.1	977.08	-1199.40
2.0000E+08	-34.27	+308.6	-0.24	+160.3	22.97	-286.00

← COMPUTED f_0 = 95 MHZ
ACTUAL 50 dB FREQ = 44.6 MHZ

← COMPUTED f_0 = 186 MHZ
ACTUAL 50 dB FREQ = 187.3 MHZ

V6

FIG. 5



PRINTED STUB FILTER

FIG. 7

V7

```
R. SNYDER
N=6 PRINTED STUB FILTER
                 RL              50
 1               PTL             Z0= 33.25 LENGTH= 30 VELOCITY FACTOR= 1
 0                               1
 2               TR              1E+07
 0                               200
 3               STL             Z0= 63.4 LENGTH= 15 VELOCITY FACTOR= 1
 0                               1
 4               PTL             Z0= 63.02 LENGTH= 30 VELOCITY FACTOR= 1
 0                               1
 5               TR              1E+07
 0                               200
 6               STL             Z0= 86.68 LENGTH= 15 VELOCITY FACTOR= 1
 0                               1
 7               PTL             Z0= 48.68 LENGTH= 30 VELOCITY FACTOR= 1
 0                               1
 8               TR              1E+07
 0                               200
 9               STL             Z0= 90.11 LENGTH= 15 VELOCITY FACTOR= 1
 0                               1
 10              PTL             Z0= 48.68 LENGTH= 30 VELOCITY FACTOR= 1
 0                               1
 11              TR              1E+07
 0                               200
 12              STL             Z0= 86.68 LENGTH= 15 VELOCITY FACTOR= 1
 0                               1
 13              PTL             Z0= 63.02 LENGTH= 30 VELOCITY FACTOR= 1
 0                               1
 14              TR              1E+07
 0                               200
 15              STL             Z0= 63.4 LENGTH= 15 VELOCITY FACTOR= 1
 0                               1
 16              PTL             Z0= 33.24 LENGTH= 30 VELOCITY FACTOR= 1
 0                               1
 17              TR              1E+07
 0                               200
```

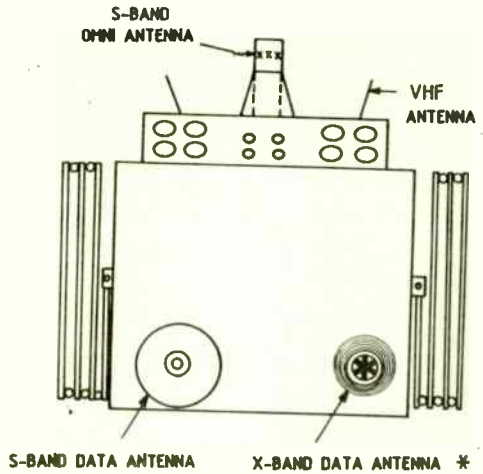
```
                 RS              50
```

FREQUENCY	INSERTION LOSS		RETURN LOSS		INPUT IMPEDANCE	
(HZ)	(DB)	ANGLE	(DB)	ANGLE	REAL	+J(REACT)
2.5000E+08	-271.01	+21.6	-0.06	-0.1	0.18	0.04
2.7000E+08	-116.91	+293.5	-0.07	-9.7	0.20	4.24
2.9000E+08	-85.95	+295.6	-0.07	-19.5	0.22	8.58
3.1000E+08	-67.56	+303.3	-0.08	-29.6	0.26	13.21
3.3000E+08	-53.26	+313.9	-0.10	-40.3	0.32	18.33
3.5000E+08	-40.18	+328.3	-0.12	-51.7	0.41	24.22
3.7000E+08	-26.45	+350.5	-0.15	-64.1	0.61	31.31
3.9000E+08	-9.65	+40.5	-0.26	-77.7	1.24	40.28
4.1000E+08	-0.77	+171.1	-0.89	-92.6	5.36	52.04
4.3000E+08	-0.44	+252.9	-4.59	-103.7	30.52	53.61
4.5000E+08	-0.53	+316.9	-11.50	-92.6	44.39	25.40
4.7000E+08	-0.40	+12.1	-16.97	-85.0	46.89	13.51
4.9000E+08	-0.32	+65.0	-25.64	-55.7	46.97	4.06
5.1000E+08	-0.33	+116.8	-25.28	+58.2	47.02	-4.37
5.3000E+08	-0.45	+169.8	-16.76	+85.0	46.77	-13.82
5.5000E+08	-0.60	+225.0	-11.32	+92.9	44.26	-25.93
5.7000E+08	-0.59	+289.6	-4.49	+103.3	29.79	-53.66
5.9000E+08	-1.04	+12.5	-0.97	+92.0	5.78	-51.44
6.1000E+08	-10.60	+139.7	-0.36	+77.2	1.69	-39.90
6.3000E+08	-27.09	+187.7	-0.24	+63.6	0.97	-31.02
6.5000E+08	-40.73	+209.1	-0.20	+51.3	0.72	-23.99
6.7000E+08	-53.80	+222.5	-0.18	+39.9	0.60	-18.14
6.9000E+08	-68.16	+231.4	-0.17	+29.2	0.53	-13.04
7.1000E+08	-86.75	+235.5	-0.17	+19.1	0.49	-8.42
7.3000E+08	-118.33	+225.6	-0.16	+9.4	0.47	-4.09
7.5000E+08	-220.73	+19.5	-0.17	-0.2	0.48	0.11

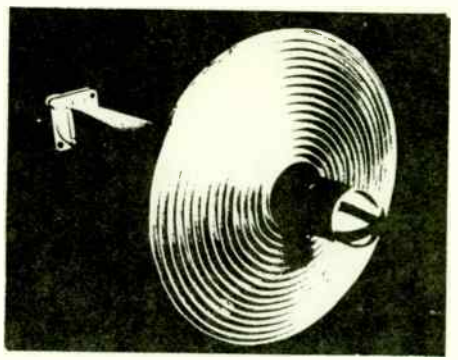
FIG. 8

V8

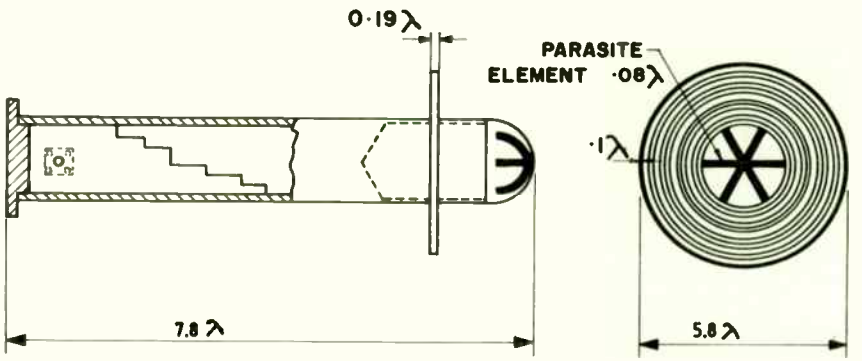
FIG 12 ANTENNA SYSTEM OF IRS



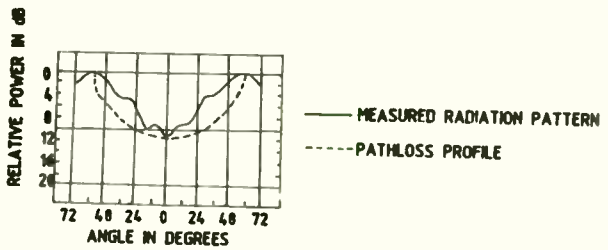
a) ANTENNAS MOUNTED ON THE EARTH VIEWING FACE OF IRS.



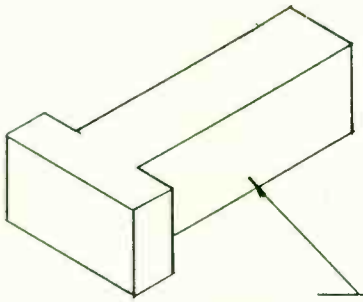
b) PRACTICAL X-BAND DATA TRANSMITTING ANTENNA



* c) SCHEMATIC OF X-BAND DATA TRANSMITTING ANTENNA

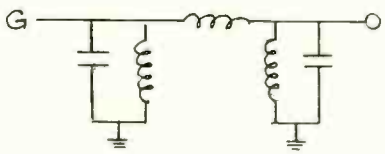


d) X - BAND ANTENNA PATTERN



BELOW CUT-OFF (f_c)

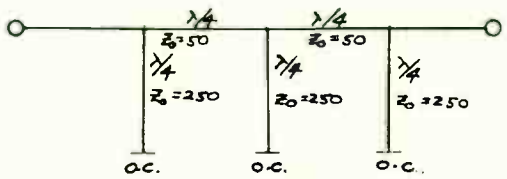
ADD CAPACITIVE PINS:



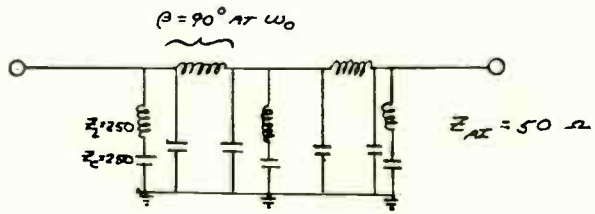
RESULT:
- INDUCTIVELY COUPLED BAND PASS FILTERS WITHOUT SPURIOUS UNTIL $f > f_c$

EVANESCENT MODE PRINCIPLE

FIG. 9



N=3 DISTRIBUTED BAND STOP FILTER



N=3 LUMPED EQUIVALENT BAND STOP FILTER

PI CIRCUITS USED AS 90° INVERTERS

PASSBAND MAINTAINED TO ABOUT 1.4 ω_0

(HIGHER ORDER INVERTERS PROVIDED WIDER PASSBAND)

CAPACITIVE PI (HIGH PASS) MAINTAINS PASSBAND DOWN TO 0.7 ω_0 BUT UP TO $2\omega_0$ OR $3\omega_0$.

FIG. 9A

V9

R. SNYDER
3 POLE DISTRIBUTED BANDSTOP FILTER

```
                RL              50
1               STL             Z0= 145.1 LENGTH= 7.5 VELOCITY FACTOR= 1
0                               1
2               TR              1E+09
0                               500
3               STL             Z0= 76.3 LENGTH= 7.5 VELOCITY FACTOR= 1
0                               1
4               STL             Z0= 85.5 LENGTH= 7.5 VELOCITY FACTOR= 1
0                               1
5               TR              1E+09
0                               500
6               STL             Z0= 76.3 LENGTH= 7.5 VELOCITY FACTOR= 1
0                               1
7               STL             Z0= 145.1 LENGTH= 7.5 VELOCITY FACTOR= 1
0                               1
8               TR              1E+09
0                               500
                RS              50
```

FREQUENCY (HZ)	INSERTION LOSS (DB)	ANGLE	RETURN LOSS (DB)	ANGLE	INPUT IMPEDANCE REAL	+J(REACT)
5.0000E+08	-0.11	+136.9	-16.44	+133.2	59.84	-13.45
5.5000E+08	-0.11	+154.2	-16.97	+115.9	54.66	-14.22
6.0000E+08	-0.08	+173.7	-19.25	+96.5	50.05	-10.98
6.5000E+08	-0.04	+196.8	-30.96	+74.8	49.19	-2.69
7.0000E+08	-0.16	+226.8	-16.30	-137.7	61.26	12.93
7.5000E+08	-1.35	+268.7	-6.07	-179.4	148.94	1.98
8.0000E+08	-5.84	+319.1	-1.45	+130.1	22.65	-103.34
8.5000E+08	-14.14	+1.8	-0.26	+87.2	1.45	-47.60
9.0000E+08	-25.78	+34.2	-0.09	+54.2	0.33	-25.58
9.5000E+08	-44.66	+60.7	-0.08	+26.0	0.23	-11.55
1.0000E+09	-140.91	+78.5	-0.08	-0.4	0.23	0.16
1.0500E+09	-43.94	+300.5	-0.09	-26.8	0.27	11.90
1.1000E+09	-25.42	+327.0	-0.12	-53.0	0.42	26.03
1.1500E+09	-13.90	+359.7	-0.31	-88.2	1.75	48.44
1.2000E+09	-5.72	+42.5	-1.57	-131.3	25.55	105.38
1.2500E+09	-1.34	+92.7	-6.32	+178.4	143.17	-4.89
1.3000E+09	-0.19	+134.2	-16.76	+137.4	60.64	-12.17
1.3500E+09	-0.07	+163.9	-30.04	-76.8	49.20	3.02
1.4000E+09	-0.11	+186.9	-19.17	-97.3	50.19	11.09

FIG. 10

V10

R. SNYDER
LUMPED 3 POLE BANDSTOP FILTER EQUIVALENT TO DISTRIBUTED EXAMPLE

```
                RL              50
1               SRLCP           R= .5 L= 2.4E-08  C= 1.05E-12
0                               1.05E-12
2               PC              2.27E-12
3               SL              1.13E-08
4               PC              2.27E-12
5               SRLCP           R= .5 L= 1.4E-08  C= 1.79E-12
0                               1.79E-12
6               PC              2.27E-12
7               SL              1.13E-08
8               PC              2.27E-12
9               SRLCP           R= .5 L= 2.4E-08  C= 1.05E-12
0                               1.05E-12
                RS              50
```

FREQUENCY (HZ)	INSERTION LOSS (DB)	ANGLE	RETURN LOSS (DB)	ANGLE	INPUT IMPEDANCE REAL	+J(REACT)
5.0000E+08	-0.05	+105.8	-20.57	-16.1	41.70	2.19
5.5000E+08	-0.03	+119.2	-24.38	-29.6	44.93	2.69
6.0000E+08	-0.02	+133.8	-34.41	-45.4	48.66	1.32
6.5000E+08	-0.03	+150.4	-31.44	+120.9	51.34	-2.36
7.0000E+08	-0.06	+169.7	-23.48	+101.1	50.85	-6.71
7.5000E+08	-0.10	+193.7	-22.62	+78.0	47.99	-6.98
8.0000E+08	-0.15	+227.7	-27.39	-148.0	53.70	2.43
8.5000E+08	-1.90	+288.0	-5.50	+158.8	123.11	-65.74
9.0000E+08	-12.63	+1.2	-0.52	+85.2	2.78	-45.94
9.5000E+08	-32.49	+45.3	-0.19	+38.2	0.61	-17.31
1.0000E+09	-102.91	+355.1	-0.17	+1.8	0.50	-0.78
1.0500E+09	-39.24	+310.4	-0.18	-32.5	0.57	14.59
1.1000E+09	-21.18	+341.9	-0.24	-67.9	0.99	33.68
1.1500E+09	-11.37	+19.0	-0.58	-106.2	4.66	66.44
1.2000E+09	-5.45	+59.2	-1.82	-147.0	57.53	148.28
1.2500E+09	-2.19	+98.8	-4.67	+173.5	182.55	-36.65
1.3000E+09	-0.65	+134.7	-10.31	+138.5	71.29	-31.77
1.3500E+09	-0.17	+167.2	-35.39	+154.8	51.56	-0.75
1.4000E+09	-0.49	+197.2	-11.17	-109.4	51.74	29.20

FIG. 11

V11

V12

R. SNYDER
DISTRIBUTED BANDSTOP FILTER

```
                RL              50
1               PTL             Z0= 145.1 LENGTH= 7.5 VELOCIT
0                               1
2               TR              1E+09
0                               500
3               STL             Z0= 76.3 LENGTH= 7.5 VELOCITY
0                               1
4               PTL             Z0= 85.5 LENGTH= 7.5 VELOCITY
0                               1
5               TR              1E+09
0                               500
6               STL             Z0= 76.3 LENGTH= 7.5 VELOCITY
0                               1
7               PTL             Z0= 145.1 LENGTH= 7.5 VELOCIT
0                               1
8               TR              1E+09
0                               500
                RS              50
```

FREQUENCY (HZ)	INSERTION LOSS (DB)	ANGLE	RETURN LOSS REAL	+J(REACT)
5.0000E+08	-0.11	+136.9	-15.48	+66.5	41.79
5.5000E+08	-0.11	+154.2	-14.04	+79.5	43.19
6.0000E+08	-0.08	+173.7	-11.13	+98.3	46.28
6.5000E+08	-0.04	+196.8	-6.97	+109.5	44.32
7.0000E+08	-0.16	+226.8	-3.47	+108.6	26.89
7.5000E+08	-1.35	+268.7	-1.39	+99.7	9.55
8.0000E+08	-5.84	+319.1	-0.46	+86.4	2.48
8.5000E+08	-14.14	+1.8	-0.14	+69.5	0.60
9.0000E+08	-25.78	+34.2	-0.07	+49.1	0.26
9.5000E+08	-44.66	+60.7	-0.07	+25.4	0.22
1.0000E+09	-140.91	+78.5	-0.08	-0.4	0.23
1.0500E+09	-43.94	+300.5	-0.08	-26.1	0.26
1.1000E+09	-25.42	+327.0	-0.09	-49.7	0.33
1.1500E+09	-13.90	+359.7	-0.17	-70.0	0.73
1.2000E+09	-5.72	+42.5	-0.50	-86.8	2.74
1.2500E+09	-1.34	+92.7	-1.46	-100.0	10.08
1.3000E+09	-0.19	+134.2	-3.58	-108.7	27.64
1.3500E+09	-0.07	+163.9	-7.11	-109.3	44.58
1.4000E+09	-0.11	+186.9	-11.24	-97.8	46.19

R. SNYDER
OPTIMIZED LUMPED BANDSTOP FILTER...NOTE SLIGHT CENTER FREQUENCY SHIFT

```
                RL              50
1               SRLCP           R= .5 L= 2.4E-08  C= 1.05E-12
0                               1.05E-12
2               PC              1.7E-12
3               SL              1.5E-08
4               PC              1.7E-12
5               SRLCP           R= .5 L= 1.4E-08  C= 1.79E-12
0                               1.79E-12
6               PC              1.7E-12
7               SL              1.5E-08
8               PC              1.7E-12
9               SRLCP           R= .5 L= 2.4E-08  C= 1.05E-12
0                               1.05E-12
                RS              50
```

FREQUENCY (HZ)	INSERTION LOSS (DB)	ANGLE	RETURN LOSS REAL	+J(REAC	FREQUENCY (HZ)	INSERTION LOSS (DB)	ANGLE	RETURN LOSS REAL	+J(REACT)	INPUT IMPEDANCE (DB)	ANGLE	REAL	+J(REACT)
5.0000E+08	-0.05	+105.8	-20.57	-16.1	41.7	5.0000E+08	-0.10	+112.1	-17.00	+154.1	64.67	-6.94
5.5000E+08	-0.03	+119.2	-24.38	-29.6	44.9	5.5000E+08	-0.12	+126.5	-16.35	+143.8	62.82	-11.57
6.0000E+08	-0.02	+133.8	-34.41	-45.4	48.6	6.0000E+08	-0.13	+142.5	-16.28	+127.9	58.47	-14.50
6.5000E+08	-0.03	+150.4	-31.44	+120.9	51.3	6.5000E+08	-0.12	+161.0	-17.46	+109.8	52.95	-13.60
7.0000E+08	-0.06	+169.7	-23.48	+101.1	50.8	7.0000E+08	-0.08	+183.6	-23.16	+88.9	49.39	-6.89
7.5000E+08	-0.10	+193.7	-22.62	+78.0	47.9	7.5000E+08	-0.16	+214.5	-19.80	-128.4	56.00	9.08
8.0000E+08	-0.15	+227.7	-27.39	-148.0	53.7	8.0000E+08	-1.44	+261.6	-6.26	-173.6	141.39	19.98
8.5000E+08	-1.90	+288.0	-5.50	+158.8	123.1	8.5000E+08	-7.42	+321.5	-1.15	+126.3	15.95	-96.70
9.0000E+08	-12.63	+1.2	-0.52	+85.2	2.7	9.0000E+08	-19.03	+10.0	-0.25	+76.8	1.15	-39.63
9.5000E+08	-32.49	+45.3	-0.19	+38.2	0.6	9.5000E+08	-37.78	+46.3	-0.18	+37.4	0.56	-16.94
1.0000E+09	-102.91	+355.1	-0.17	+1.8	0.5	1.0000E+09	-107.82	+353.1	-0.17	+1.8	0.50	-0.78
1.0500E+09	-39.24	+310.4	-0.18	-32.5	0.5	1.0500E+09	-44.46	+309.8	-0.17	-32.1	0.54	14.36
1.1000E+09	-21.18	+341.9	-0.24	-67.9	0.9	1.1000E+09	-27.13	+337.9	-0.18	-64.2	0.72	31.37
1.1500E+09	-11.37	+19.0	-0.58	-106.2	4.6	1.1500E+09	-18.06	+7.0	-0.24	-94.6	1.48	54.12
1.2000E+09	-5.45	+59.2	-1.82	-147.0	57.5	1.2000E+09	-12.25	+34.9	-0.44	-123.1	5.56	91.94
1.2500E+09	-2.19	+98.8	-4.67	+173.5	182.5	1.2500E+09	-8.09	+61.8	-0.93	-150.2	38.92	180.23
1.3000E+09	-0.65	+134.7	-10.31	+138.5	71.2	1.3000E+09	-4.84	+89.0	-2.00	-177.3	419.86	84.01
1.3500E+09	-0.17	+167.2	-35.39	+154.8	51.5	1.3500E+09	-2.19	+118.7	-4.55	+153.5	111.49	-90.92
1.4000E+09	-0.49	+197.2	-11.17	-109.4	51.7	1.4000E+09	-0.46	+153.5	-12.66	+121.9	58.45	-23.74

FIG. 12

Average Efficiency of Power Amplifiers

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ABSTRACT

Accurate prediction of the heat dissipation and power consumption of power amplifiers and transmitters requires knowledge of their average efficiency. Since the instantaneous efficiency of a PA depends upon the signal amplitude relative to the peak-envelope power (PEP), the average efficiency depends upon both the type of power amplifier and the type of signal being amplified. This paper relates average power input, power output, and efficiency to the characteristics of the PA and the probability-density functions (p.d.f.s) of the signal. The p.d.f.s for a variety of commonly used signals, including two-tone SSB/SC, single-tone AM, uniform, QAM, Rayleigh, Laplacian, Gaussian, Gaussian AM, and Laplacian AM are presented. The average efficiencies of class-A, -B, and -D PAs are then derived for two-tone and Rayleigh-envelope signals.

1. INTRODUCTION

Accurate prediction of the average efficiency and/or power consumption of a power amplifier (PA) or transmitter is required in many applications. Some examples of radio-system components and parameters that depend upon the efficiency and power consumption are:

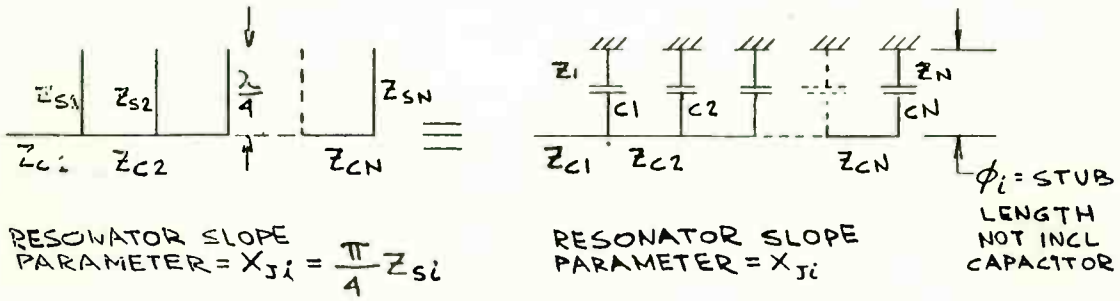
- Battery life,
- Solar-cell, battery, or generator capacity,
- Heat-sink size and weight,
- Ancillary cooling requirements, and
- Operating costs.

Knowledge of the average-efficiency characteristics allows the designer to make intelligent decisions based upon the costs and benefits of different system approaches. For example, class-D RF PAs and class-S AM modulators have better efficiencies than do class-C RF PAs and class-B series-pass AM modulators, but are also more complex and expensive [1, 2]. Knowledge of the average-efficiency characteristics of class-G PAs, envelope-tracking systems, outphasing systems, and Doherty systems is necessary to set their parameters for maximum-efficiency operation.

The efficiency of a PA generally varies with the amplitude of the signal, and usually increases to a maximum value at the peak envelope power (PEP) or maximum signal voltage. Efficiency curves for typical class-A, -B, and -D PAs are shown in Figure 1a.

Since FM and CW signals have only one amplitude level, knowledge of the efficiency and input power at PEP is sufficient. Inspection of the curves in Figure 1a shows that modest improvements in efficiency are achieved by changing the class of amplification.

In contrast, amplitude-modulated signals (including SSB, television, and



RESONATOR SLOPE PARAMETER = $X_{Ji} = \frac{\pi}{4} Z_{Si}$

RESONATOR SLOPE PARAMETER = X_{Ji}

APPENDIX:

EQUIVALENCE OF $\lambda/4$ OPEN CIRCUIT (O.C.) STUB FILTER TO SHORT CIRCUITED, CAPACITIVELY COUPLED STUB FILTER WITH EQUIVALENT STUB LENGTH PLUS CAPACITOR PHASE SHIFT TOTALING $\lambda/4$.

SEE EQS (1) – (4)

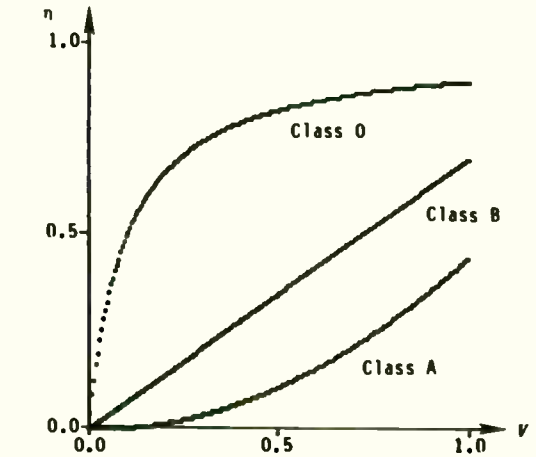
(1) $X_{Ji} = \frac{\pi}{4} Z_{Si}$

(2) $F(\phi_i) = \phi_i \sec^2 \phi_i + \tan \phi_i$

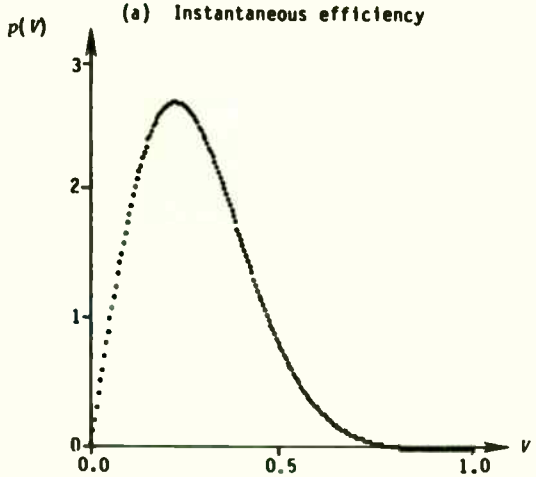
(3) $F(\phi_i) = \frac{2X_{Ji}}{Z_i}$

(4) $\omega_0 C_i = \frac{1}{Z_i \tan \phi_i}$

FIG. 13



(a) Instantaneous efficiency



(b) Probability-density function

Figure 1. Efficiency and p.d.f. curves.

multicarrier relay) and wideband signals contain a variety of different amplitudes that produce a variety of different instantaneous efficiencies. The p.d.f. for a typical multitone SSB or multicarrier envelope (Figure 1b) shows that low- and middle-level amplitudes are far more prevalent than amplitudes near PEP. At the most likely amplitude, the efficiencies of the class-A, -B, and -O PAs of Figure 1a differ considerably, hence significant improvements in the average efficiency can be expected by changing the class of amplification.

It would be natural to define *average efficiency* as the average of the instantaneous PA efficiency. However, average efficiency thus defined is an interesting indicator of PA performance but otherwise useless. A preferable definition is the ratio of the average output and average input powers; that is

$$\eta_{AVG} = \frac{P_{o}AVG}{P_{t}AVG} \quad . \tag{1}$$

Inspection of the amplifier-efficiency and signal-p.d.f. curves of Figure 1 shows that average efficiency depends upon both PA characteristics and signal characteristics. This paper develops the relationships that can be used to predict average efficiency, and gives the p.d.f.s for a variety of commonly used signals. Example calculations are performed for class-A, -B, and -O PAs.

2. CHARACTERISTICS OF SIGNALS

Signals can be classified as either wideband or narrowband. Instantane-

FIGURE 15
HIGH POWER 500 MHz BANDPASS FILTER

FIGURE 14
LUMPED ELEMENT BANDPASS
IN A TUBULAR TYPE

ous PA efficiency and input power are generally related to the instantaneous amplitude (voltage) of a wideband signal, or to the instantaneous envelope of a narrowband signal [1].

The statistical characteristics of the signal amplitude are described by its probability-density function (p.d.f.). Integration of a p.d.f. over a particular range of amplitudes gives the probability that the signal amplitude is within that range [5]; i.e.,

$$P(V_1 < V < V_2) = \int_{V_1}^{V_2} p(V)\, dV \quad . \tag{2}$$

The relationship of the p.d.f. to a signal voltage or envelope is illustrated in Figure 2. The full-wave rectified sinewave is, of course, a deterministic (rather than random) signal. Nonetheless, the p.d.f. is an appropriate means of describing the amount of time spent at each amplitude.

The p.d.f. can be derived from the waveform or envelope by using the definition of the p.d.f. to equate corresponding areas under the two curves, as illustrated in Figure 2. The "probability" of the angular-time variable θ being in an interval of width $d\theta$ is $d\theta/2\pi$. If only one of the points at which the waveform has voltage V is considered, then

$$p(V)\, dV = d\theta/2\pi \quad , \tag{3}$$

Taking the limit as $d\theta \to 0$ and rearranging produce

$$p(V) = |d\theta/dV|/2\pi \quad . \tag{4}$$

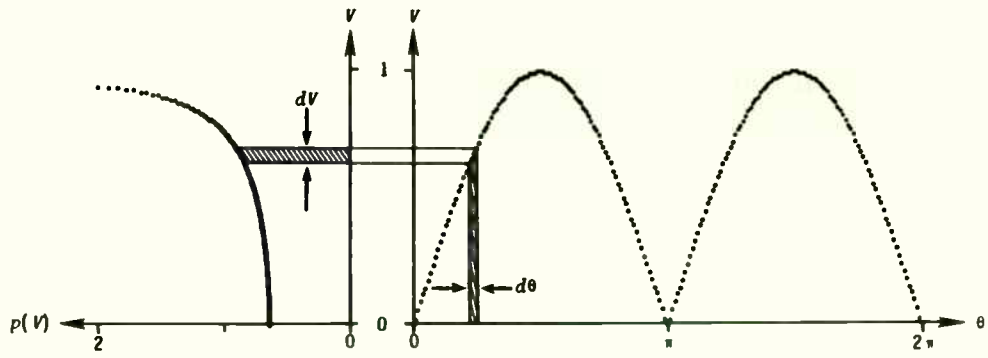


Figure 2. Derivation of p.d.f. from waveform.

A PHASE LOCK LOOP THAT WORKS - ALMOST

PART 1

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A Phase Lock Loop That Works - Almost Part 1.

So the system phase lock loop has been built. All the study and calculations are finished. The natural frequency and damping ratios have been set. The long awaited VCO is installed, and now the loop is closed.

Just as anticipated, it works. Well maybe it almost works. A few adjustments and it will be fine. Many adjustments and lots of frustrating hours later it still almost works.

Does this sound at all familiar? There seems to be a lot of phase lock loops that never fully meet the expectations of their creators. Some may have never worked at all or work only after an application of "black magic". In this article some of basic problems that keep a phase lock loop from working correctly will be examined.

Basics of Loop Problem Analysis

It is important to keep in mind that a phase lock loop is a phase/frequency domain system. The loop may be buried deep in a totally digital IC board and used to generate computer clocks for timing but it remains a phase/frequency domain system. Thus frequency measurement techniques must be employed to properly verify the operation.

Designers with a digital logic background frequently rely on clock jitter measurements observed on an oscilloscope as a primary trouble shooting tool. Unfortunately in most cases time domain observations tell only a small part of the whole story To understand and analyze the loop operation prepare to move into the frequency domain.

Three rules of experience can be used to guide loop trouble shooting and verification. These may seem at first to be almost trivial but a rigorous adherance will almost guarantee the expected PLL performance.

The first rule is that all components of the loop must work by themselves as intended. Not only must parts like the VCO and phase detector work as described in the spec sheets but they must work correctly when mounted in place on the circuit board. Most of these parts are sensitive analog components and require a bit of consideration. A phase lock loop running from a five volt logic bus surrounded by many watts of TTL or ECL circuits is in trouble already.

The second rule is that the components when connected together open loop must work perfectly. More about this later but suffice to say without perfect open loop operation, there is little hope for the closed loop.

The third rule applies in cases of modulated or pulsed signals. The loop must work as predicted for CW inputs or again there is small hope for operation with modulation.

If it can be accepted that these levels of perfection are required at each step, the PLL designer will have much higher success ratio and fewer of the almost loops.

Beginning Trouble Shooting

Phase lock loop circuits often have other extra circuits attached to them. Frequency search circuits and phase lock indicators are cases in point. These must be separated out early to get the loop down to its basics. Before a search circuit can be properly evaluated it has to be shown that the loop will

The full-wave rectified sinusoid is represented by

$$V(\theta) = |\sin \theta| \quad , \tag{5}$$

hence

$$\theta = \pm \arcsin V \pm n\pi/2 \quad , \tag{6}$$

and

$$|d\theta/dV| = (1 - V^2)^{-1/2} \quad . \tag{7}$$

Since there are four intervals in θ that make equal contributions to $p(V)$, the p.d.f. is

$$p(V) = (2/\pi)(1 - V^2)^{-1/2} \quad . \tag{8}$$

The average values of desired parameters are computed by integrating the product of the parameter and the p.d.f. of the signal envelope or voltage over the appropriate range. The average input power is therefore given by

$$P_{iAVG} = \int_0^{V_{max}} P_i(V)\, p(V)\, dV \quad , \tag{9}$$

where $P_i(V)$ is the instantaneous input power. In the absence of an analytical form for input power, interpolation in a table of measurements can be used.

Power output is proportional to the square of the instantaneous voltage or envelope. The average power output with a wideband signal is therefore

$$P_{oAVG} = \int_0^{V_{max}} V^2\, p(V)\, dV \quad . \tag{10}$$

Since the envelope of a narrowband signal modulates a sinusoidal carrier, and integration of the square of that carrier over one cycle produces a factor of 1/2, the average power output with a narrowband signal is

$$P_{oAVG} = \frac{1}{2} \int_0^{V_{max}} V^2\, p(V)\, dV \quad . \tag{11}$$

3. PROBABILITY-DENSITY FUNCTIONS

This section presents a number of p.d.f.s that are useful in the analysis of the average efficiencies of power amplifiers. As discussed subsequently, a particular p.d.f. may apply to the instantaneous voltage of a wideband signal, the envelope of narrowband signal, or both.

The p.d.f.s presented below are based upon the normalization

$$V = V_{om}/V_{omPEP} \tag{12}$$

for narrowband signals or

$$V = |v_o|/v_{omax} \tag{13}$$

for wideband signals. These normalizations conveniently limit the range of

phase lock once the VCO and reference are brought within range.
A quick analysis of whatever problems the loop exhibits may point out a course of action. But a good place to start most trouble shooting is with the components.

The three essential components of any PLL are the phase detector, the loop filter and the VCO. Usually the VCO is the most difficult hardware design of these components. The loop filter may require the most analytical work but in terms of the required parts it is usually very simple. A good phase detector is somewhere in between. The design requires a mixture of analytical effort and hardware effort to meet the PLL requirements.

What Makes a Good VCO

For most considerations in a PLL, the actual operating frequency of the VCO is not a factor. Divider delays and very high fractional ratio loop band widths may require the loop frequency in the calculations. For the average loop these are not a problem. But these are second order effects. So the VCO is considered as a loop element with an input/output transfer function.

Most literature advocates taking three or four frequency measurements by changing the control voltage and from this deriving a gain factor Kv. Kv for most loop analysis is in rad/sec/volt so any frequency change/voltage change ratios must be multiplied by 2π to convert Δ Hz/Δ volts to the value required for loop forward gain.

The few points usually recommended for frequency measurements are not enough to guarantee a design. Computer controlled measurement equipment now makes a hundred point sweep with a high resolution graph a job that can easily be done in less than a minute. The sweep should extend to the voltage limits that could ever possibly be expected in loop operation.
The graph should be examined very carefully for slope changes, flat spots or at worst slope inversions. The trace without exception must be smooth and monotonic over all input voltages. The oscillator power supply should be varied over its extremes and the graph rerun. If operation over temperature is required the graph should again be repeated.

Over the environmental extremes a simple lateral shift of the control curve can usually be corrected by the loop. Slight slope changes can usually also be handled. But extreme changes in either cannot be tolerated.

A spectrum analyzer is almost essential at this point for any serious investigation. Using a low IF bandwidth and narrow frequency sweep, the VCO output should be closely tracked across the control voltage range. Harmonicaly related spectral lines are to be expected. But lines that come and go that are not a multiple of main output should be looked into. Output variations with power supply and temperature extremes should also be checked. An oscillator does not have a little parasitic oscillation. Either it is clean or it has a problem. Any parasitic oscillation must be eliminated before using the VCO.

The VCO should also be checked over its full range for affects on the output by the load. Driving into any reasonable load the tuning must remain smooth with no breaks or discontinuities. Any tendency towards load pulling demands more isolation on the oscillator output. With a TTL output device this is as simple as adding another gate in series with the oscillator. Linear waveform units will require a pad or isolation amplifier.

Oscillator phase jitter is a parameter that is often ignored until it is too late. Logic clocks seem to exhibit a particular lack of concern. If the

values to

$$0 \leq V \leq 1 \quad . \tag{14}$$

The second normalization requires the efficiency of wideband PAs to be expressed in terms of the absolute value of the instantaneous output voltage.

The first and second moments are defined by

$$\mu_1 = \int_0^1 V\, p(V)\, dV \tag{15}$$

and

$$\mu_2 = \int_0^1 V^2\, p(V)\, dV \quad . \tag{16}$$

These quantities are the average voltage and average squared voltage, and appear frequently in average-efficiency analyses.

The *peak-to-average ratio* ξ is defined as the ratio of the peak output power or peak envelope power (PEP) to the average output power. For both wideband and narrowband signals, the normalizations produce

$$\xi = P_{o\max}/P_{o\mathrm{AVG}} = 1/\mu_2 \quad . \tag{17}$$

For full-carrier amplitude-modulated (AM) signals, the modulation peak-to-average ratio is also of interest. Since the normalized modulating voltage is limited by (11) to 1/2 (for a carrier level of 1/2), $P_{m\max} = 1/4$ and

$$\xi_m = P_{m\max}/P_{m\mathrm{AVG}} = 1/(4P_{m\mathrm{AVG}}). \tag{18}$$

Two-Tone Envelope

The full-wave rectified sinewave given by (4) and shown in Figure 2 occurs for

- Wideband amplification of a constant-amplitude sinusoid,
- Narrowband amplification of a DSB/SC signal with single-tone modulation,
- Narrowband amplification of an SSB/SC signal resulting from two equal-amplitude tones, and
- Certain types of data signals employing two-tone AFSK modulation.

The third case is the commonly used *two-tone* test signal, as is easily shown by trigonometric substitutions.

The p.d.f. of the two-tone envelope is given by (7) and shown in Figures 2 and 3. It is apparent that the amplitudes near PEP are more likely than those near zero. For deterministic signals such as this, most calculations are more easily performed in the time domain. However, the p.d.f. is useful for inclusion in numerical-evaluation programs that incorporate other p.d.f.s. Time-domain integration yields $\mu_1 = 2/\pi$ and $\mu_2 = 1/2$, hence the peak-to-average ratio is

$$\xi = 1/\mu_2 = 2 \rightarrow 3 \text{ dB} \quad . \tag{19}$$

frequency is right, the PLL must be right seems to be the rule. But this is not the entire story. Phase noise specifications may be derived from involved statistical processes but the effects of a noisy loop are obvious. Television pictures from a noisy sync scan are fuzzy on the edges. Clock gates that are supposed to arrive at a particular time occasionally don't make it. These are direct time domain examples of phase noise.

A PLL will attempt to clean up a VCO output and make it look like a replica of the input reference. But this action can only function inside the loop bandwidth. Outside the loop bandwidth, the VCO spectral output is basically unchanged. It looks like the free running output noise. A simple solution might seem to be to make the loop bandwidth as wide as possible and eliminate all noise. For a multitude of reasons this is not the solution.

The only solution that produces results is to use a VCO with the least possible noise that will fit the loop needs. At different frequency ranges, different oscillators are optimum. At a few MHz, typically current tuned RC oscillators are the noisest, LC varactor tuned oscillators are a big improvement and voltage controlled crystal oscillators are among the quietest. Figure 1 contrasts the spectral noise output of a standard current tuned RC DIP oscillator and a simple TTL varactor tuned LC oscillator. Although the observed spectral noise has AM and FM noise components, the overwelming majority of the noise power is concentrated in phase noise. The difference between the two oscillator output is obvious. The 40dB more noise from the RC oscillator was more than enough to keep a major computer system clock generator on hold until it was replaced with the LC oscillator.

Phase noise can only be properly evaluated with a spectrum analyzer. Observing time domain jitter on a clock edge for instance with an oscilloscope is a very subjective measurement. Differences between oscillator performance that can only be guessed at with an oscilloscope become as clear as the contrasting traces in Figure 1.

One last VCO characteristic that affects the loop operation is the modulation frequency response roll off. As previously mentioned the VCO is simply a block in a PLL. The output frequency is not a concern. The gain factor Kv is the DC gain factor for this block. The information that is missing is the poles and zeroes of the transfer function. This is not necessarily the same as the modulation bandwidth specifications. There does not seem to be wide spread industry agreement on the meaning and measurement of modulation bandwidth. There is virtually no information available on the actual VCO transfer function nor is there a recognized measurement method. In lieu of this the best choice is to specify a modulation bandwidth several times higher than the widest loop bandwidth anticipated. This will be disccussed in more detail later on.

A VCO must be constructed with special consideration. As mentioned, tight voltage regulation and output isolation are musts. It should be separated from digital circuits. Digital clock circuit paths should not cross the VCO layout area. Only with this type of special attention can a VCO be expected to perform as required.

A Phase Detector Check

The phase detector serves as the loop error detector providing error information for loop control. Two types of detectors are in frequent use; the balanced mixer

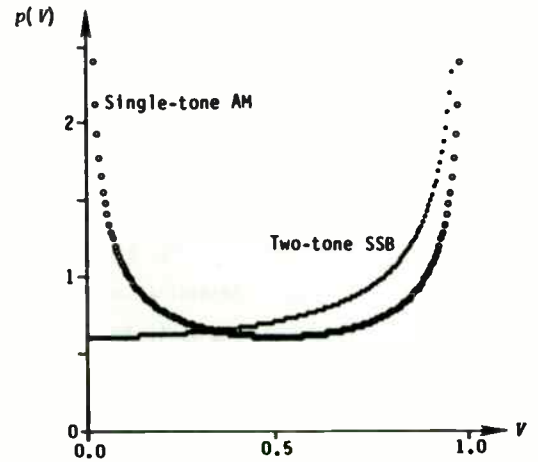

Figure 3. P.d.f.s for two-tone envelope and single-tone AM.

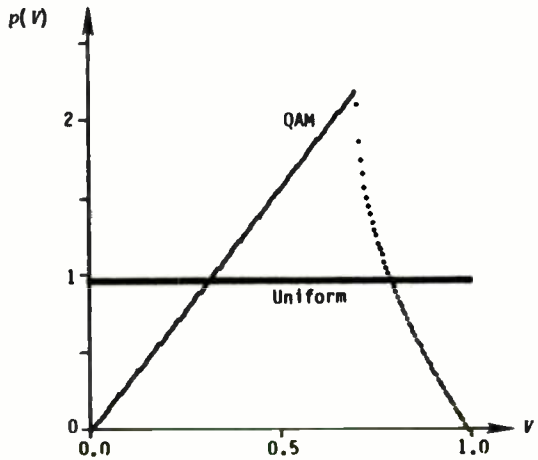

Figure 4. P.d.f.s for uniform and QAM envelopes.

Single-Tone AM

A full-carrier AM signal with 100-percent modulation by a single tone is described by

$$V(\theta) = (1/2)(1 + \sin \theta) \quad , \tag{20}$$

hence application of the method of Section 2 produces

$$p(V) = (2/\pi)[1 - (2V - 1)^2]^{-1/2} \quad . \tag{21}$$

Time-domain integration of (20) yields $\mu_1 = 1/2$ and $\mu_2 = 3/8$, hence the peak-to-average ratio

$$\xi = 1/\mu_2 = 8/3 \doteq 4.3 \text{ dB} \quad . \tag{22}$$

Uniform

When all signal amplitudes are equally likely, they are said to be uniformly distributed and have the p.d.f.

$$p(V) = 1 \quad , \tag{23}$$

which is shown in Figure 4. This p.d.f. occurs for

- The limiting case for certain amplitude companders,
- Full-carrier AM with triangular or sawtooth modulation, and
- Wideband amplification of triangular or sawtooth waveforms.

Integrals (15) and (16) yield $\mu_1 = 1/2$ and $\mu_2 = 1/3$, hence the relatively

and the logic level frequency/phase detector. Each has distinct advantages and problems.

For any detector the phase conversion function should be verified. At and near the point of intended operation the input phase differential versus output voltage graph must be smooth and linear. The graph must be monotonic and free of any hint of flat spots or slope inversions. This point is a particular problem with logic level frequency/phase detectors.

Figure 2 is a simplified version of the logic level MC4344 type of detector. Recent articles have discussed in detail sampling delays through these devices. However Figure 2 will illustrate a more major problem. Figure 2 shows two negative edge triggered flip flops with a NAND gate for feedback to a common clear line. When both Q outputs go high the gate will clear the flip flops. When both inputs are at the same frequency and the falling edges line up the detector op amp output should declare zero phase. However, the time delay through the gate and through the flip flop clear produces some curious results. Since the time delay is fixed it represents a greater phase ambiguity at higher frequencies. Thus the 4344 type detector that works well at 100KHz is in real trouble at 10MHz. Phase flat spots at zero phase produce a zero gain slope. Some units have been observed to produce a reverse gain slope across a small region. This results in positive loop feedback and a loop oscillation in the positive feedback region. The VCO output will have a seemingly incurable jitter in this situation. The phase detector is being used beyond the maximum input frequency.

The mixer phase detector does not normally display crossover flat spots. It is likely to be used for tracking filters with analog inputs and most applications above 50MHz. Since this phase detector is not a frequency discriminator, an external search loop of some sort is usually employed. To evaluate the phase detector or the PLL, this search loop should be disabled and a manual method used to establish frequency proximity. This prevents one loop from interfering with the other.

As a loop element, the phase detector's DC transfer function is the slope Ko Δ volts/Δ phase evaluated at the intended operating point. With a mixer type phase detector this is shown to be A volts/rad when the beat note output is a sine wave of peak amplitude A volts. If the output is not sinusoidal, a spectrum analyzer will provide the fourier series coefficients. For a waveform with $V = A\sin\theta - B\sin 3\theta + C\sin 5\theta$-...reference 2 shows the slope Ko at zero volts to be

$$K_o = A-3B+5C-\ldots\ldots \text{ volts/rad.}$$

This allows accurate slope determination for any waveform. However, the slope will change if the loop does not hold at crossover or if mixer offsets cause zero volts output to not represent 90° or $\Pi/2$ radians. In either case the phase detector gain is reduced as the loop operating moves away from 90°.

Neglecting any cross-over problems, the frequency/phase detector has a more constant slope Ko over its range. This is a big advantage in extending acquisition bandwidth and in demodulation schemes. The output as shown is balanced. To provide a distinct point that can be labeled as the phase detector output a differential input op amp may be used. The input low pass network is used to roll off fast logic edges that are beyond the bandwidth capabilities of the following op amp.

low peak-to-average ratio

$$\xi = 1/\mu_2 = 3 \rightarrow 4.8 \text{ dB} \quad . \tag{24}$$

Because the uniform p.d.f. is often amenable to analytical evaluation of averages, it can be a useful means of checking for proper operation of numerical-evaluation programs.

Quadrature-Amplitude Modulation

Quadrature-amplitude modulation (QAM) is an efficient means of maximizing data-transmission capability by separate amplitude modulation of the I and Q components of the signal. For example, sixteen-symbol QAM transmits four bits of information per data symbol.

In contrast to FSK, PSK, and QPSK, QAM produces a number of different signal amplitudes. For a small number of symbols, the average power and efficiency are easily evaluated by determining the specific amplitudes and their probabilities. Results for 16-, 64-, and 256-symbol QAM are given in [6].

As the number of symbols in QAM increases, the signal space becomes a uniformly filled rectangle with the peak-envelope power occuring at the corners of the rectangle. The p.d.f. (Figure 4), of this *infinitely packed QAM* signal is

$$p(V) = \begin{cases} \pi V & , 0 < V < 1/2^{1/2} \\ \pi V - 4 V \arctan(2 V^2 - 1)^{1/2}, & 1/2^{1/2} < V < 1 \end{cases} \quad . \tag{25}$$

The first and second moments of this p.d.f. are (from numerical integration)

$\mu_1 \cong 0.5411$ and $\mu_2 \cong 0.3333$. The peak-to-average ratio is therefore

$$\xi = 1/\mu_2 = 3 \rightarrow 4.8 \text{ dB} \quad . \tag{26}$$

Gaussian

The sum of a large number of well behaved, independent random variables tends to have a Gaussian p.d.f. [5]. Broadcast sound [7], certain radar and sonar pulses [7], music [8], and other signals can be assumed to be Gaussian in the absence of other statistical data. The envelope of a DSB/SC signal modulated by such sounds is also Gaussian.

Since most PAs are characterized in terms of the absolute value of the instantaneous output voltage or the envelope, it is convenient to use the single-sided Gaussian p.d.f. If the small area above $V = 1$ is ignored (which is reasonable for $\xi > 5$ dB), the average output power for a wideband signal is $\sigma^2 = \mu_2$, hence

$$\xi = 1 / \sigma^2 \quad . \tag{27}$$

The p.d.f. can now be written as

$$p(V) = (2\xi/\pi)^{1/2} \exp(-V^2 \xi/2) \quad . \tag{28}$$

The integral (14) is evaluated by converting $2VdV$ into dV^2, which produces

$$\mu_1 = (2/\pi)^{1/2} \sigma = (2\xi/\pi)^{1/2} \quad . \tag{29}$$

As shown in Figure 5, increasing the peak-to-average ratio makes low ampli-

Thus higher order mixer products are reduced before they can appear as side bands on the VCO output. This input rolloff along with any poles contributed by the op amp combine with Kv to form the complete phase detector block transfer function. In most cases these poles are inconsequential but in a wide band loop they may begin to nibble away at the phase margin.

The op amp could be eliminated and the double ended detector outputs be connected to a differential input loop filter. This has the advantage of saving parts but as will later be discussed some valuable trouble shooting and loop verification aids are greatly reduced.

Phase detectors of either type are fairly simple circuits. Their correct operation as a loop building block must again be carefully checked. A smooth, monotonic transfer curve is essential. This is the loop error detector. The loop can only correct with the degree of accuracy that this element can provide.

Loop Filter

The selection of loop filter values has been the subject of many excellent books and articles. Most of these deal with idealistic situations in which all loop parameters are available and well defined. References 3,4 and 5 are the exception in that many real world problems are clearly pointed out. The loop filter will contribute an additional pole at the origin to determine the loop type, but the order and in large part the phase margin are set by factors beyond the designer's immediate control. Through the combination of op amp poles and VCO modulation poles a type two second order loop is shown to quickly evolve to a fifth or higher order loop.

The loop filter is about the only part of the loop over which a designer has a great deal of control. Through a combination of analysis and measurement, the higher order effects may be accounted for and in many cases the loop bandwidth and phase margin re-established.

The loop filter remains though an op amp and just a few resistors and capacitors. Selection of an appropriate amplifier is important. PLL's above 25KHz in bandwidth normally will require a wide band op amp. An open loop DC gain of 100d8 or more with a first breakpoint no lower than 1KHz will keep loop phase margin degradation to a minimum. Narrower bandwidth loops do not require such wide band op amps.

The tradeoff from using a wide band op amp usually comes from its inability to provide exacting DC balance and low leakages and offsets.

Leakage currents restrict the magnitude of input resistors that may be considered. With higher leakage currents and if the input resistor value becomes to large, the resultant voltage drop can move the desired loop phase set point. Lower bandwidth amplifiers usually have much lower leakages and thus do not present a problem.

Another problem that may appear on a finished printed wiring board is bulk mode leakage through the board material. This can be a particular nuisance in a board with all the parts mounted in plated through holes. Tiny leakage currents from power supplies and other sources can combine at the op amp input and force the phase detector output to provide a balancing current. This current is produced by the phase detector output moving off ground with a resultant input/output phase offset. This problem is usually noticed when a breadboard loop filter built in some casual fashion works well with little

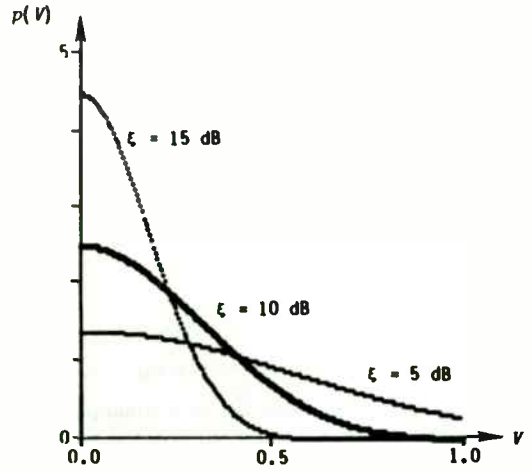

Figure 5. Gaussian p.d.f.s.

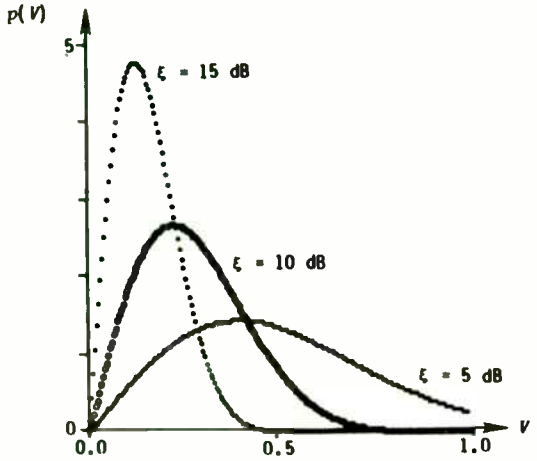

Figure 6. Rayleigh p.d.f.s.

tudes more likely. Peak-to-average ratios in the range of 10 to 15 dB are typical [8].

Rayleigh

Independent Gaussian I and Q components of equal power produce a Rayleigh-distributed envelope and a uniformly-distributed phase. The sum of independent Rayleigh phasors is itself a Rayleigh phasor, and the sum of a large number of well behaved independent phasors tends toward a Rayleigh phasor [5]. The Rayleigh p.d.f. is therefore appropriate [1, 6, 9] for the envelope of a narrowband signal in applications such as

- SSB/SC signals resulting from noise-like modulation,
- Multiple-carrier relay signals, and
- Independent-sideband (ISB) transmissions.

It is convenient to write the p.d.f. as

$$p(V) = 2V\,\xi\,\exp(-V^2\,\xi) \quad . \tag{30}$$

If the area above $V = 1$ is included, integration produces $\mu_2 = 1/\xi$. From [5] or standard integral tables,

$$\mu_1 = (\pi\,\alpha)^{1/2}/2 = (\pi/4\xi)^{1/2} \quad . \tag{31}$$

The effect of the peak-to-average ratio upon the p.d.f. is shown in Figure 6. In multicarrier-relay applications, ξ is easily related to the amplitudes and/or number of the carriers [1]. The average output power is simply the sum of the powers of the individual carriers, since they are of different

offset, but the finished product shows a phase skew.

The offset and resultant shift can be severly affected by temperature, humidity and the manufacturing processes to which the board is subjected. It can be a nuisance in a CW PLL and a disater in a pulsed or bandwidth switching loop. Leakage can also reduce the apparent DC gain. Without a pole at the origin, the loop is reduced to a high gain type one system. The phase error then shifts with frequency. Keeping the input resistors as low as possible will minimize the problem. Mounting critical elements with clinched leads in unsupported holes will also help.

As with the other loop elements the loop filter must work by itself as an integrator before including it in a PLL. Simple voltage step inputs to observe the ramp voltage, DC leakage tests for output drift and input offset measurements will verify the hardware.

In evaluating problems in a PLL remember changing filter values is probably the simplest thing that can be done. For most loops a designer does not need to retreat deep into system analysis to find the problem. If the hardware is functioning properly and the loop still doesn't work, there is probably a unknown pole or delay. Change the filter values. Drop the bandwidth and try it again. A stable bandwidth will come out of this where the loop will lock. Theory and measurement will meet. The simplicity of the loop filter provides the design slack to back the loop bandwidth down then carefully bring it back up while cataloging unkown disturbances along the way.

End Part 1 Phase Lock Loop Components

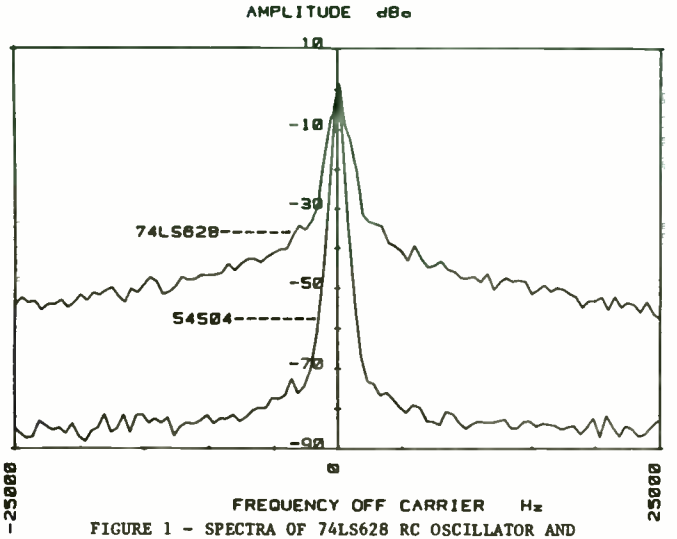

FIGURE 1 - SPECTRA OF 74LS628 RC OSCILLATOR AND 54S04 LC OSCILLATOR

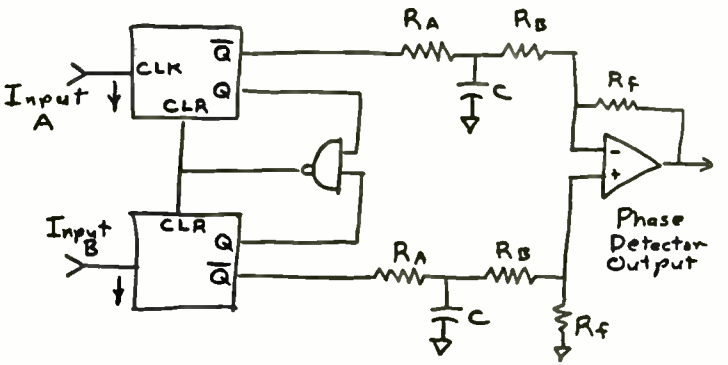

FIGURE 2 - FUNCTIONAL ILLUSTRATION OF LOGIC LEVEL FREQUENCY PHASE DETECTOR

frequencies and therefore mutually orthogonal. However, the peak power is proportional to the square of the sum of the peak voltages, since at some point in time all carriers add in phase. Given N carriers of equal amplitudes, the peak-to-average ratio is therefore

$$\xi = P_{oPEP}/P_{oAVG} = N^2/N = N \quad . \tag{32}$$

Flat-Topped Rayleigh

The probability of flat topping by a signal with a Rayleigh-distributed envelope is

$$P_{FT} = \int_1^\infty p_R(V)\, dV = \exp(-\xi_R) \quad , \tag{33}$$

where p_R and ξ_R represent the p.d.f. and peak-to-average ratio, respectively, of the original signal. The probability of flat topping is only 4.2 percent for $\xi_R = 5$ dB, and drops rapidly to 0.005 percent at $\xi_R = 10$ dB.

In most applications, satisfactory accuracy can be obtained by using the standard Rayleigh p.d.f. and ignoring the small contributions due to $V > 1$. However, when the peak-to-average ratio is very low the effects of flat topping cannot be ignored. A flat-topped Rayleigh p.d.f. [10] can then be formed from the standard Rayleigh p.d.f. and the Dirac delta function:

$$p_F(V) = p_R(V) + P_{FT}\, \delta(V - 1) \quad . \tag{34}$$

The moments of this p.d.f. must be computed numerically. In addition, special handling of this p.d.f. is required in numerical-evaluation programs to ensure accurate accommodation of the contributions of the delta function.

Laplacian

The Laplacian (also called one-sided exponential) p.d.f. (Figure 7) applies to

- Speech waveforms [11] and
- SSB/SC envelopes produced by speech modulation [9].

The gamma p.d.f. is said to be a better approximation to the true p.d.f. of speech [12], but its additional complexity is not warranted for PA average-efficiency analysis.

The Laplacian p.d.f. has the form

$$p(V) = (2\xi)^{1/2} \exp[(2\xi)^{1/2}\, V] \quad , \tag{35}$$

which produces $\mu_2 = 1/\xi$ if the area above $V = 1$ is included. The first moment is then

$$\mu_1 = \sigma/2^{1/2} = (2/\xi)^{1/2} \quad . \tag{36}$$

Gaussian AM

Full-carrier amplitude modulation by a Gaussian signal produces an RF signal with a Gaussian-AM envelope. The envelope p.d.f. is a Gaussian p.d.f. whose mean is the amplitude of the unmodulated carrier. By analogy to (28),

VCO Tests
A Design Example

As part of a design example illustrating the techniques of this article, the problems and test data for a 1 MHz type two second order phase lock loop will be traced from the component test through the final closed loop data. The first item for test is the VCO.

The VCO is a varactor tuned circuit built expressly for illustrating various problems. The graphs and pictures represent actual measured data encountered during laboratory tests. Computer controlled test equipment has been extensively employed to create accurate, repeatable high resolution plots.

Figure A plots the frequency variation around 1 MHz versus the input control voltage for the VCO. This graphs seems to show a wide range of fairly constant slope from Ø volts to + 10 volts.

However, a slope analysis using a small moving window for a least squares linear regression curve fit produces the results of Figure B. This graph plots the slope of the curve in Figure A versus the input control voltage. A careful examination of Figure A will show small flat spots at about 0, 7.5 and 9.5 volts. These are dramatically pointed out in Figure B where the slope changes drastically at these points. The slope graph highlights what might easily be missed in Figure A. Clearly this is not acceptable. A spectral examination did in fact show the presence of parasitic oscillations at these points.

After the VCO circuit problems were corrected, the data for Figure C was recorded. The corresponding slope graph Figure D shows the slope is fairly constant between 4 volts and 8 volts. Figure E is new data for high resolution frequency at 1 MHz (0 Hz delta frequency). This plot still seems smooth and completely monotonic. Figure F bares this out. The slope data shows an almost constant slope from 5.5 volts to 7.5 volts. This will nicely center the VCO at 6.5 volts for 1 MHz operation with a slope Kv = 2660 Hz/volt.

Figure G is a spectral plot of the VCO with assorted parasitic oscillations. If the IF bandwidth of the analyzer is too high during a search for unwanted oscillations they may never be found.

Figure H is the spectral plot of the finished VCO. Note the lack of any hint of unwanted oscillations and the sharp clear center frequency spectral line without wide noise skirts.

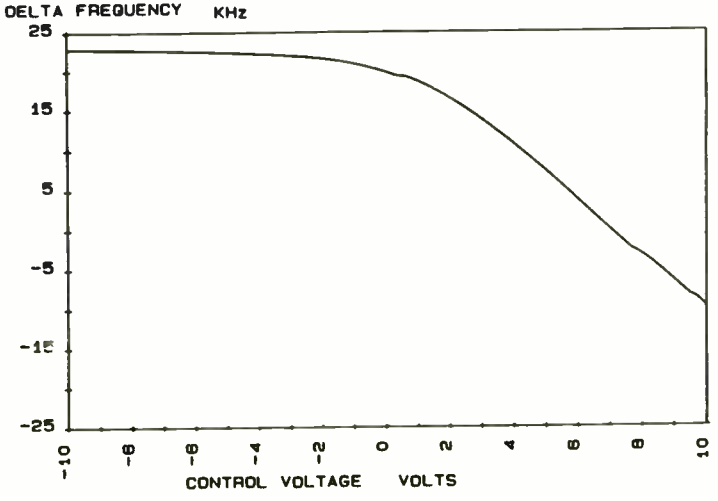

FIGURE VCO-A - TUNING CURVE OF 1MHZ VCO

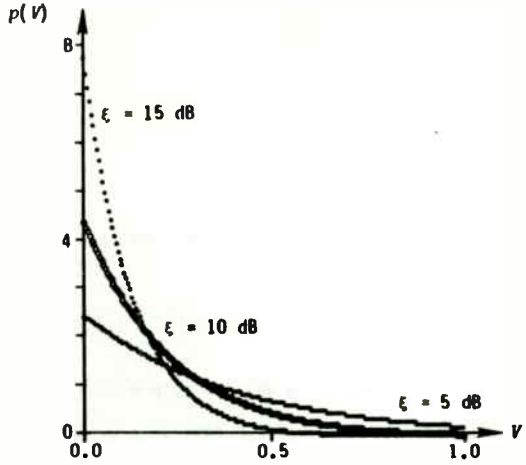

Figure 7. Laplacian p.d.f.s.

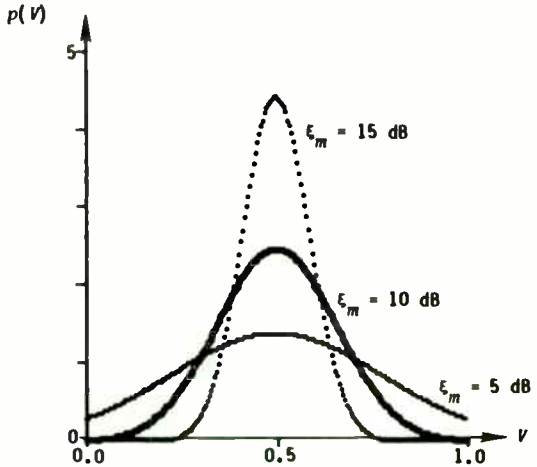

Figure 8. Gaussian-AM p.d.f.s.

$$p(V) = (2\xi_m/\pi)^{1/2} \exp[-2\xi_m(V - 1/2)^2] \quad . \tag{37}$$

The first moment is simply the carrier level; i.e., $\mu_1 = 1/2$. If the areas for $V < 0$ and $V > 1$ are included, the second moment is easily obtained by summing the carrier and modulation powers:

$$\mu_2 = 1/4 + 1/4\xi_m. \tag{38}$$

The RF peak-to-average ratio is therefore related to the modulation peak-to-average ratio by

$$\xi = 4\xi_m/(\xi_m + 1) \quad . \tag{39}$$

Gaussian-AM p.d.f.s for several modulation peak-to-average ratios are shown in Figure 8.

Laplacian AM

Full-carrier amplitude modulation by a Laplacian signal produces an RF signal with a Laplacian-AM envelope. The p.d.f. is, by analogy to (37),

$$p(V) = (2\xi_m)^{1/2} \exp[-2(2\xi_m)^{1/2} |V - 1/2|] \quad . \tag{40}$$

Laplacian-AM p.d.f.s for several modulation peak-to-average ratios are shown in Figure 9. The moments and the relationship between ξ and ξ_m are the same as those for Gaussian AM.

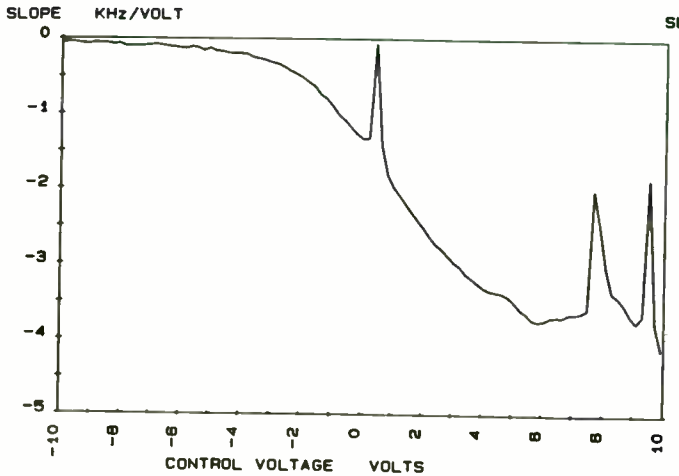

FIGURE VCO-B - SLOPE ANALYSIS OF 1MHZ VCO TUNING CURVE

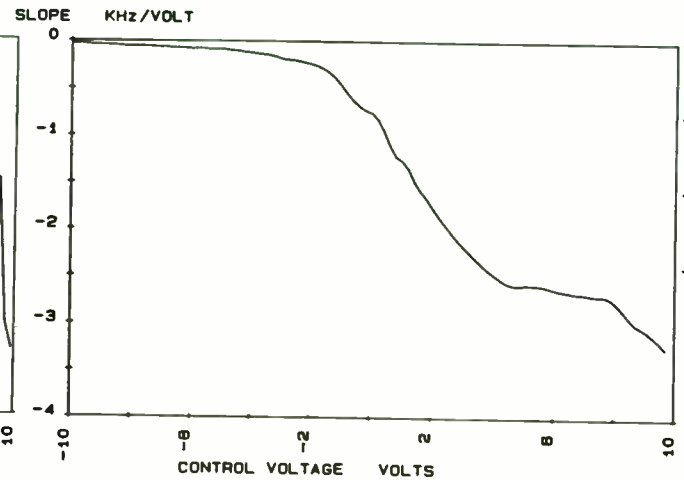

FIGURE VCO-D - SLOPE ANALYSIS OF VCO TUNING CURVE AFTER PARASITIC OSCILLATIONS WERE ELIMINATED

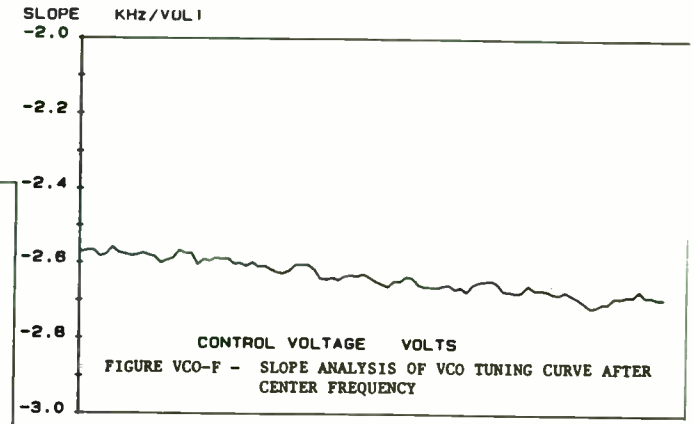

FIGURE VCO-F - SLOPE ANALYSIS OF VCO TUNING CURVE AFTER CENTER FREQUENCY

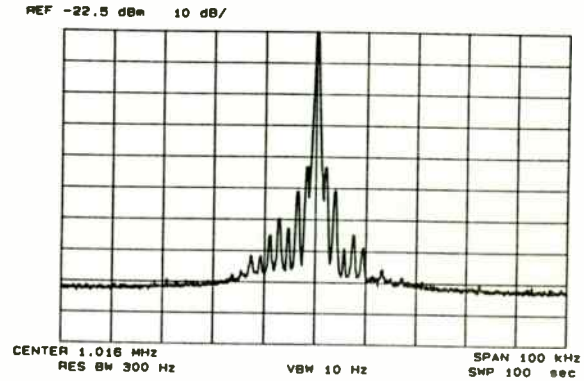

FIGURE VCO-G - VCO OUTPUT SPECTRUM WITH PARASITIC OSCILLATIONS

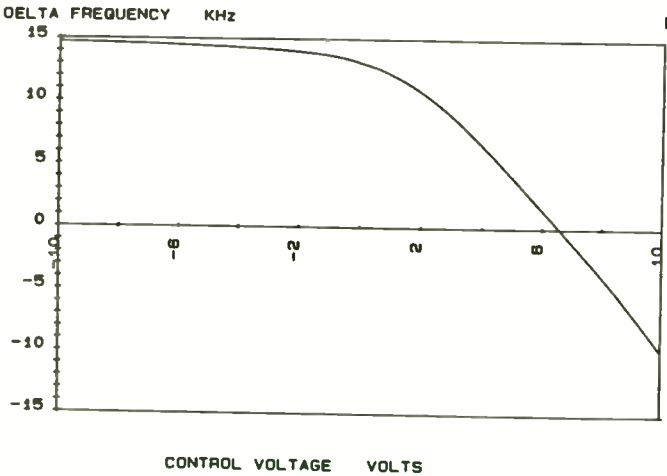

FIGURE VCO-C - VCO TUNING CURVE AFTER PARASITIC OSCILLATIONS WERE ELIMINATED

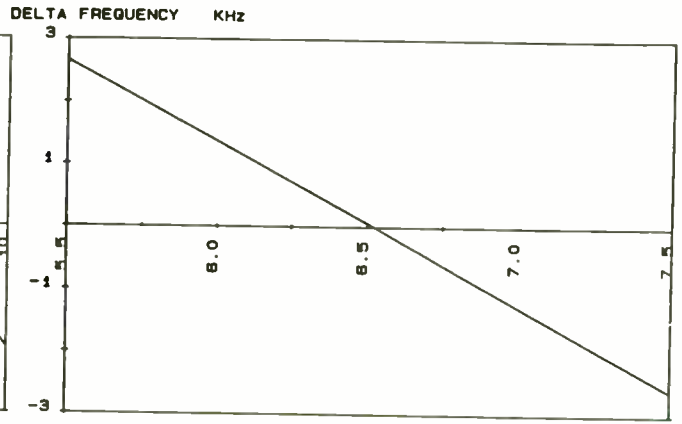

FIGURE VCO-E - HIGH RESOLUTION VCO TUNING CURVE AFTER CENTER FREQUENCY

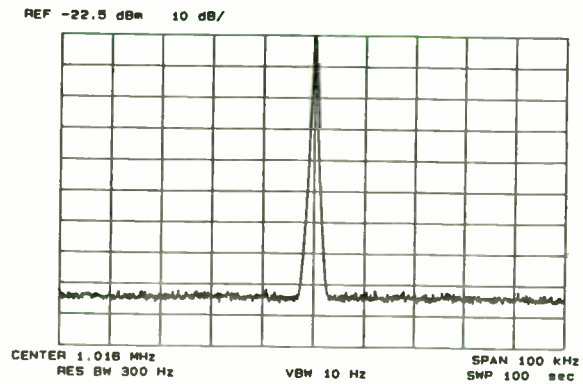

FIGURE VCO-H - VCO OUTPUT SPECTRUM AFTER PARASITIC OSCILLATIONS HAVE BEEN ELIMINATED

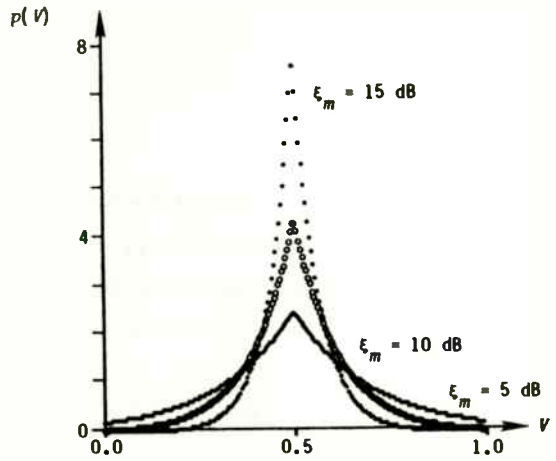

Figure 9. Laplacian-AM p.d.f.s.

PA	V_{eff} / V_{CC}	η_{AVG}			
		CW	TWO-TONE	RAYLEIGH ξ = 10 dB	RAYLEIGH ξ = 20 dB
Class A	1.0	0.500	0.250	0.050	0.005
	0.9	0.450	0.225	0.045	0.004
Class B	1.0	0.785	0.617	0.280	0.089
	0.9	0.707	0.555	0.252	0.080
Class D	1.0	1.000	1.000	1.000	1.000
	0.9	0.900	0.887	0.781	0.530

Table 1. Average efficiencies.

4. AVERAGE-EFFICIENCY CALCULATIONS

The theory and probability-density functions derived in the preceding sections are now used to calculate average-efficiency for several cases of interest. The examples include

- Class-A,
- Class-B, and
- Class-D

power amplifiers, with

- Two-tone test signal,
- Rayleigh-envelope with ξ = 10 dB, and
- Rayleigh-envelope with ξ = 20 dB.

Similar approaches can be used to calculate the average efficiency with other PAs and/or other signals.

The method used here is to relate the average input and output power to the peak-envelope output power. The average output power is independent of the PA and is obtained from (17). The results are summarized in Table 1.

Class A

In class-A PAs, the transistors are biased so that the collector current(s) are positive at all times. The quiescent current (hence dc input current) must therefore be at least as equal to the maximum output current at PEP. In addition, the true supply voltage V_{CC} is reduced to an effective supply voltage V_{eff} by the saturation voltage V_{sat} of the transistor(s). For a

Phase Detector Tests

A double balanced diode mixer will work well as a phase detector. Figure A plots the output of a TO-5 50 ohm unit with 1 MHz inputs. The response is a smooth cosine wave with a zero crossing at 90 degrees. Figure B plots the slope of the data in Figure A using a linear regression least squares fit. It is important to note that the peak slope in volts/radian at 90 degrees from Figure B is equal to the peak voltage output at zero degrees from Figure A.

Figure C provides a high resolution look at the zero crossing area. Figure D plots the phase slope for the same region. Note that the slope is constant but with some curious dips. These dips would cause an open loop gain increase of about ten percent. Most closed loops could tolerate this without serious impact.

Figure E provides a wide phase sweep of a TTL frequency/phase detector constructed of 54F00 series gates with a differential input op amp.

Figure F shows the slope is constant at 2 volts/radian over $\pm$150 degrees except for the dip around zero degrees.

Figure G provides an expanded high resolution of the crossover region. Some of the problems caused by gate delays become apparent. These delays cause the rough, bumpy appearance of the trace. Figure H shows that the slope is indeed erratic around crossover. The slope at crossover is observed to be 3 volts/radian, a substantial increase over the wide sweep value of 2 volts/radian. This 50 percent increase in phase slope would cause a corresponding increase in open loop gain. Such an increase would seriously reduce the phase margin and stability of most loops if not properly accounted for. The slope data from the high resolution graph should be used in any closed loop component or stability calculations. This phase detector with a phase slope of 2.954 volts/radian will be used for this example.

Figure I illustrates the results from another version of the TTL detector that is currently in wide use. Note the flat spot between 0 and +2 degrees. In this region the phase gain is zero or slightly positive. A loop using this detector might lock but would oscillate within this 2 degree window. If this problem had not been discovered the output from a PLL using this detector would shake and no amount of loop bandwidth adjustment would help.

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push-pull PA,

$$V_{eff} = V_{CC} - V_{sat} \quad . \tag{41}$$

For a complementary PA, V_{sat} is multiplied by 2. The dc input power and instantaneous efficiency are therefore [1, Chapter 12]

$$P_i = V_{CC}\, I_{omPEP} = \frac{V_{CC}}{V_{eff}} \cdot 2P_{oPEP} \tag{42}$$

and

$$\eta = \frac{V_{eff}}{V_{CC}} \frac{V_{om}^2}{V_{omPEP}} \quad . \tag{43}$$

The parabolic efficiency curve is shown in Figure 1. The effects of FET on resistance can similarly be reduced to a ratio of V_{eff}/V_{DD}.

The dc input current is constant, hence $P_{iAVG} = P_i$. The average efficiency is therefore

$$\eta_{AVG} = \frac{1}{2\xi} \cdot \frac{V_{eff}}{V_{CC}} \quad . \tag{44}$$

Insertion of $\xi = 2$ for the two-tone envelope gives a maximum efficiency of 25 percent, which is reduced by the ratio V_{eff}/V_{CC}. Similarly, signals with Rayleigh envelopes and 10- and 20-dB peak-to-average ratios are amplified by class-A PAs with maximum average efficiencies of 5.0 and 0.5 percent, respectively.

Class B

In class-B PAs, the transistors are biased so that each conducts current for approximately half of the time. The dc input current is $2/\pi$ times the maximum instantaneous output current [1]; the instantaneous efficiency is therefore proportional to output voltage, as shown in Figure 1. As in a class-A PA, saturation voltage produces an effective supply voltage that is lower than the true supply voltage. The instantaneous dc input power is therefore

$$P_i = \frac{4}{\pi} \frac{V_{CC}}{V_{eff}} \frac{V_{om}}{V_{omPEP}} P_{oPEP} \quad . \tag{45}$$

The ratio V_{om}/V_{omPEP} is the normalized output voltage V defined in (11) and used throughout this paper. Consequently,

$$P_{iAVG} = \frac{4}{\pi} \frac{V_{CC}}{V_{eff}} \mu_1 P_{oPEP} \tag{46}$$

and

$$\eta_{AVG} = \frac{4}{\pi \mu_1 \xi} \cdot \frac{V_{eff}}{V_{CC}} \quad . \tag{47}$$

Substitution of μ_1 and ξ for the two-tone signal yields

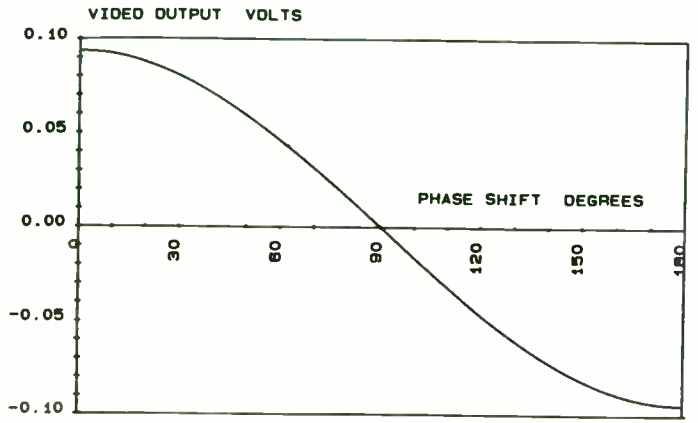

FIGURE PHASE DETECTOR-A - TRANSFER CURVE OF A DOUBLE BALANCED MIXER USED AS A PHASE DETECTOR

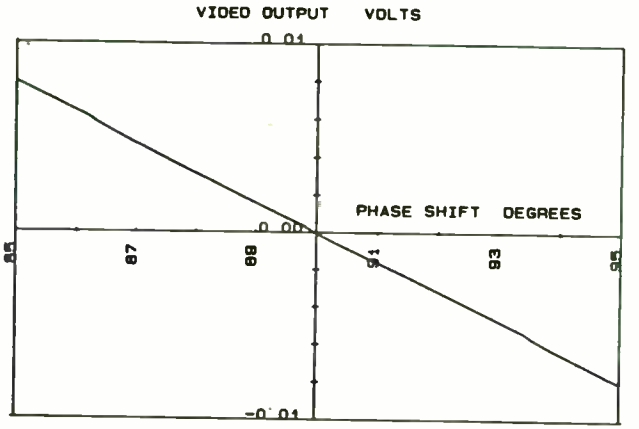

FIGURE PHASE DETECTOR-C - DOUBLE BALANCE MIXER PHASE TRANSFER CURVE AT ZERO VOLTAGE CROSSING

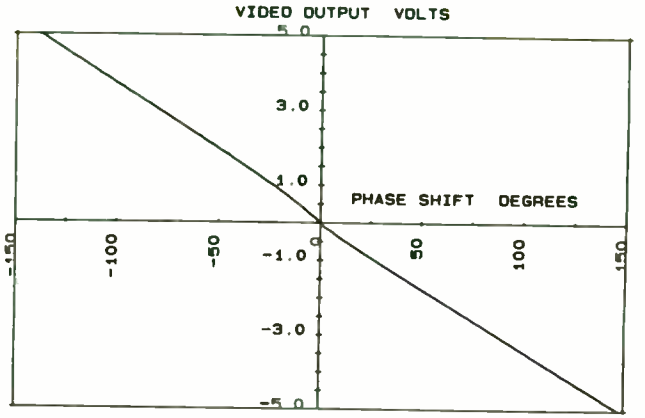

FIGURE PHASE DETECTOR-E - PHASE TRANSFER CURVE OF TTL PHASE DETECTOR

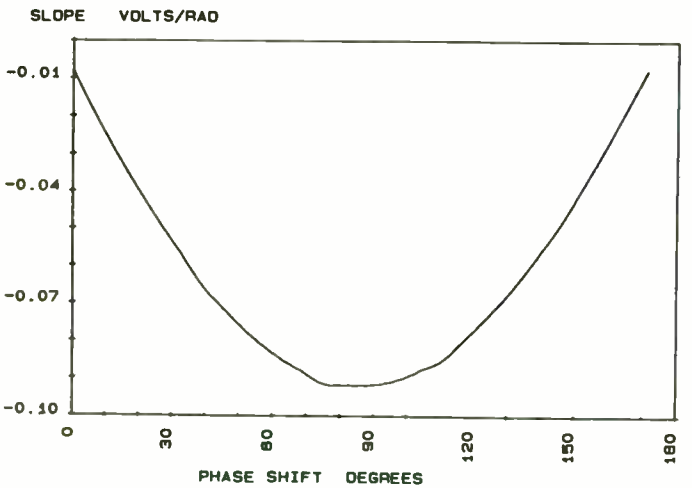

FIGURE PHASE DETECTOR-B - SLOPE ANALYSIS OF DOUBLE BALANCED MIXER PHASE TRANSFER CURVE

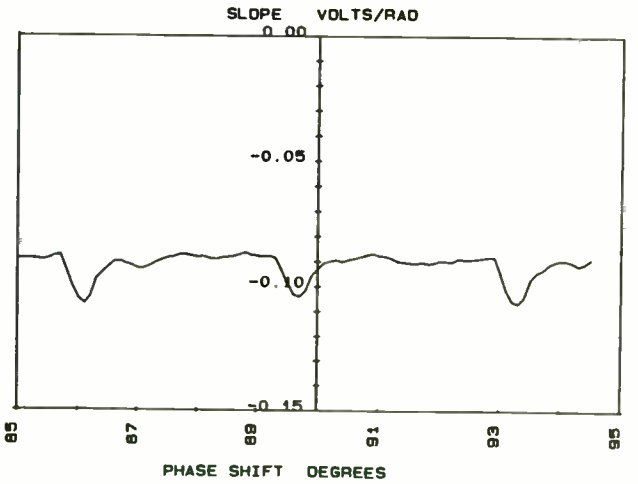

FIGURE PHASE DETECTOR-D - SLOPE ANALYSIS OF DOUBLE BALANCED MIXER AT ZERO VOLTAGE CROSSING

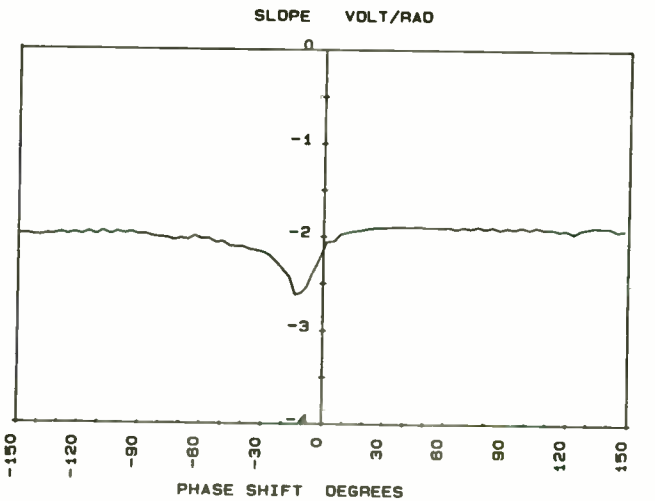

FIGURE PHASE DETECTOR-F - SLOPE ANALYSIS OF TTL PHASE DETECTOR TRANSFER CURVE

$$\eta_{AVG,Two\text{-}Tone} = \frac{\pi^2}{16}\frac{V_{eff}}{V_{CC}} \approx 0.617\frac{V_{eff}}{V_{CC}} \quad . \tag{48}$$

A substitution from (30) for the Rayleigh envelope similarly yields

$$\eta_{AVG,Rayleigh} = \left(\frac{\pi}{4\xi}\right)^{1/2} \cdot \frac{V_{eff}}{V_{CC}} \quad . \tag{49}$$

For peak-to-average ratios of 10 and 20 dB, the average efficiencies of an ideal class-B PA ($V_{sat} = 0$) are only 28 and 8.9 percent, respectively. While these represent considerable improvements over those of the class-A PA, they are nonetheless considerably smaller than the 78.5-percent efficiency at PEP.

Class D

Class-D PAs employ a pair of transistors that are driven to switch at the carrier frequency [1], followed by a series-tuned tank circuit to produce a sinusoidal output. The efficiency of an ideal class-D PA is 100 percent; however, saturation voltage, saturation resistance, and charging of the collector or drain capacitance reduce the efficiency.

The power expended in charging linear shunt capacitance is proportional to the output power and therefore reduces both PEP and average efficiencies by the same factor. The power required to charge voltage-dependent capacitance results in a power-input function [13] that must be averaged numerically.

The supply voltage of a class-D PA must be varied to produce amplitude-modulated RF signals. The effects of the BJT saturation-voltage drop are overcome by increasing the modulator output at all levels by a fixed voltage. The instantaneous input power of an amplitude-modulated class-D PA is therefore

$$P_i = P_o + \frac{2V_{sat}\,V_{om}}{\pi R} \quad , \tag{50}$$

hence its instantaneous efficiency is

$$\eta = \frac{V_{om}}{V_{om} + (4/\pi)V_{sat}} \quad . \tag{51}$$

It is convenient to rewrite the instantaneous input power as

$$P_i = P_o + \varepsilon\, V\, P_{oPEP} \quad , \tag{52}$$

where

$$\varepsilon = \begin{cases} V_{sat} \,/\, V_{effPEP}, & \text{push-pull PA} \\ 2V_{sat} \,/\, V_{effPEP}, & \text{complementary PA} \end{cases} \tag{53}$$

represents the saturation-power-loss factor. The average input power is then

$$P_{iAVG} = P_{oAVG} + \varepsilon\,\mu_1\,P_{oPEP} \quad , \tag{54}$$

and the average efficiency is

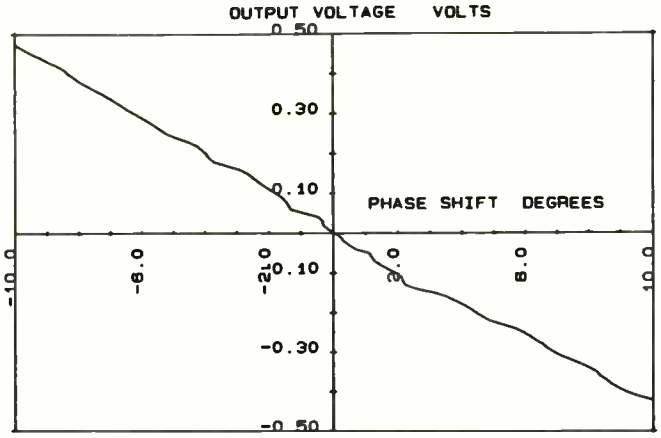

FIGURE PHASE DETECTOR-G - TTL PHASE DETECTOR TRANSFER CURVE AT ZERO VOLTAGE CROSSING

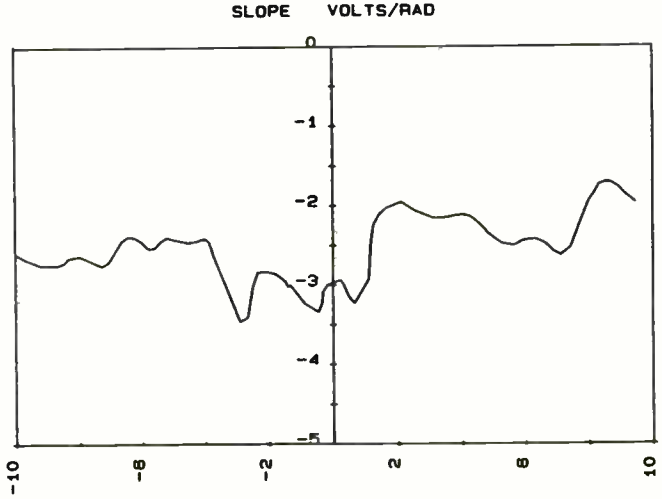

FIGURE PHASE DETECTOR-H - TTL PHASE DETECTOR SLOPE ANALYSIS AT ZERO VOLTAGE CROSSING

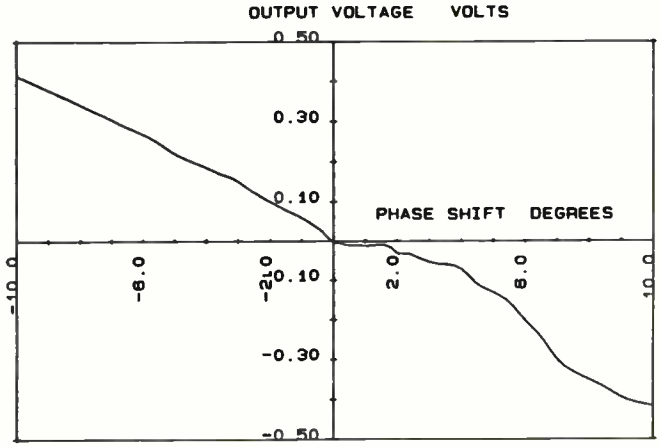

FIGURE PHASE DETECTOR-I - PHASE TRANSFER CURVE OF ANOTHER TTL PHASE DETECTOR

$$\eta_{AVG} = \frac{1}{1 + s\,\mu_1\,\xi} \quad . \tag{55}$$

Substitution of μ_1 and ξ for the two-tone envelope yields

$$\eta_{AVG,Two\text{-}tone} = \frac{1}{1 + (4/\pi)s} \quad , \tag{56}$$

hence $\eta_{AVG} = 0.887$ for $s = 0.1$. Substitution of μ_1 from (30) yields

$$\eta_{AVG,Rayleigh} = \frac{1}{1 + s(\pi\,\xi/4)^{1/2}} \tag{57}$$

for Rayleigh-envelope signals, hence average efficiencies of 0.781 and 0.530 for $s = 0.1$ and $\xi = 10$ and 20 dB, respectively. These efficiencies represent considerable improvements over those of class-B PAs.

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A 405 MHz Phased Array Antenna for Atmospheric Wind Measurement

by

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The Wave Propagation Laboratory has completed the design and construction of a phased array antenna for use at 405 MHz for atmospheric wind profiling. The steering geometry of the sequentially switched beams is shown in Fig. 1. Transmitted signals are backscattered by temperature or moisture related gradients in the radio refractive index of scales equal to one-half the transmitted wavelength. These signals are Doppler processed to extract radial air mass velocities. The measurement geometry of Fig. 1 allow horizontal velocities at heights up to 15 kilometers to be calculated. These radars are known as Wind Profiling Radars.

The 126 5-element Yagi-Uda antennas are arranged on a square grid whose axes are 45° with respect to the cardinal steering directions. For a given steering angle this arrangement allows element spacing $\sqrt{2}$ larger than that required for a broadside steered array. This feature helps minimize element interaction and reduces the number of elements required to populate a given aperture. This geometry is shown in Fig. 2.

By constraining the phase difference between rows of identically phased elements to an even, integral sub-multiple of 360°, symmetrics appear in the phasing maps which reduce the switching hardware. In this design, the element spacing $\sqrt{2}$ X in Fig. 2, is .91λ and $\Delta\phi$ is 60° resulting in an oblique beam direction of 15° from vertical. Only 15 RF coaxial transfer switches are used to synthesize the required 18 phase combinations for North, East, South, and West steering. These 18 signals are labeled A through R in Fig. 3.

The vertical beam is generated by switching around the four beam circuitry of Fig. 3 resulting in identical phasing on all of the elements. Requiring 36 RF coaxial SPDT switches, the vertical beam is more expensive than the four cardinal beams.

After the 18 signals are synthesized they are split and distributed about the array while maintaining proper phasing because of the symmetries. Uneven power splitter/combiners are used for amplitude tapering. A schematic of the whole antenna is shown in Fig. 4, and a map of the quasi-circular array of Fig. 5 shows the placement of 7 each of the 18 phases.

Computer simulations were employed in the design process. For any position in spherical coordinate space the radiation pattern of an array of isotropic radiators may be calculated from the Equation: [Tang & Burns, 1984]

$$E(\cos\alpha_x, \cos\alpha_y) = \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} A_{mn} e^{j2\pi\left(\frac{\phi mn}{360} + md_x \cos\alpha_x + nd_y \cos\alpha_y\right)}$$

This "array factor" pattern is multiplied by the pattern of the individual Yagi elements to obtain the antenna pattern of the phased array. This pattern was projected into X-Y planar coordinates and processed for display on a color graphics workstation. These simulations allowed optimization of element spacing, phasing, and amplitude tapering. These calculations were repeated after the array was constructed using amplitudes and phases measured on each of the 126 elements. The measured patterns are shown in Fig. 6.

Table 1 summarizes the antenna characteristics.

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Tang, R. and R. Burns (1984): Phased arrays. Chapter 20 from Antenna Engineering Handbook, 2nd Edition, Johnson, R. and H. Jasik, editors.

405 MHz Phased Array Antenna

Number of steering directions:	5
Oblique beam directions:	4
Azimuth:	0°, 90°, 180°, 270°
Elevation:	75°
Gain:	30 dBi
One-way 3 dB beamwidth:	6°
Effective aperture:	44 m^2
Peak power:	60,000 w
Average power:	6,000 w
Technology:	126 5-element Yagi-Uda radiators 51 R.F. coaxial switches with indicators 1 1:18 high power reactive splitter/combiner 18 1:7 uneven reactive splitter/combiners low loss foam distribution cables

Table 1

CONSTRUCTION TIPS AND ENVIRONMENT FOR DIELECTRIC RESONATOR CIRCUITS

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Sponsored by MuRata Erie N. A.
Microwave/Technical Ceramics Group
August 18, 1986

This article is directed to the design engineer who wishes to use dielectric resonators in microwave circuit applications. The resonance cavity is first discussed and then some tips on choosing a dielectric resonator are provided. The effect of the environment on the electrical parameters of the dielectric resonator is developed. This is followed by a description of temperature variation and performance. The article concludes by describing a program disk for the IBM PC that is menu driven and helps the designer choose the appropriate dielectric resonator for his or her application.

METALLIC ENCLOSURE:

The concept of a resonator is a fundamental one of physics and applies to electric circuit performance as a function of frequency. A tuned circuit provides an impedance that changes with frequency but can be described as resonant at some frequency. This means that an electric circuit has some maximum or minimum impedance; this impedance can be in series or parallel (shunt). A metal resonant cavity has a precise resonance (actually a series of resonance modes) that is due to the modes that propagate in the cavity which satisfy the boundary conditions provided by the metal walls (Reference 1).

The metal resonant cavity, like a dielectric resonator, has an infinite number of resonances (modes) that depends on the length (L) and in the case of a cylindrical resonator the diameter (D) as shown in Figure 1. Similar resonant modes exist in a dielectric resonator, but the boundary condition for the dielectric resonator is the dual of the metal cavity.

The electromagnetic waves are confined to the metal container and satisfy the boundary conditions at the walls for a perfect electrical conductor and are such that the tangential electrical field vanishes at the surface of a conductor. To satisfy this boundary condition, the resonant cavity confines the electric field in a mode that is normal to the wall surface. Modes of the resonant cavity are field descriptions that are known to satisfy this boundary condition (Reference 1).

The boundary condition for the metal cavity where the tangential electric field vanishes may be considered a **SHORT** for an electric wall. A dielectric resonator has modes that satisfy the dual condition thought of as a magnetic wall where the tangential magnetic field vanishes and may be considered an **OPEN**.

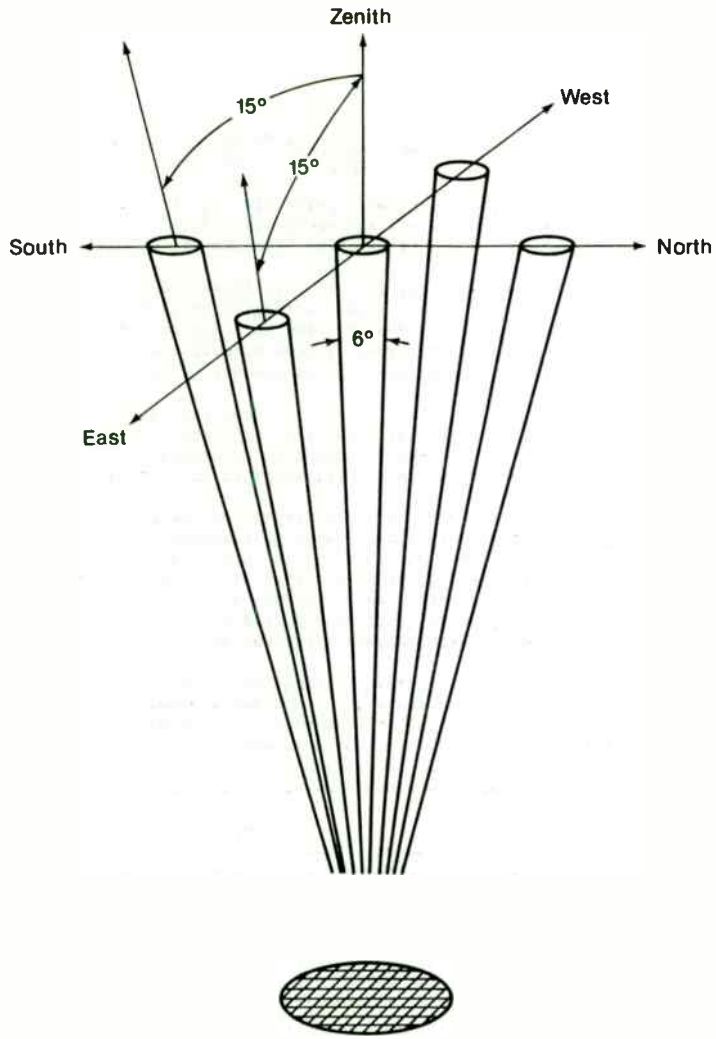
These resonant modes are best understood by visualizing the resonant cavity shown in Figure 1 as a cylindrical waveguide of diameter D which has a length L. Thus, propagation in a metal waveguide is first developed in terms of modes such as TE_{01} and the end boundary condition requires that multiple half wavelengths for the cylindrical waveguide must be set up between the end walls. This provides that the third subscript, such as TE_{011}, is understood to be the TE_{01} cylindrical mode propagating such that one half wavelength in the cylindrical waveguide is equal to the length L.

Metal waveguides can propagate electromagnetic energy above some cutoff frequency in one or more modes that satisfy the boundary conditions at the walls of the waveguide. From cutoff to about 50% above cutoff, only one mode will propagate and this is used as the frequency band for a particular dimension waveguide. Circular waveguide is an appropriate starting description for the dielectric resonator because the ratios of the different modes are similar to that of dielectric resonators. A better model is a cylindrical dielectric waveguide that propagates energy through a dielectric with fields inside the dielectric as well as outside, but the fields outside must vanish at infinity. This allows the resonant modes to be specified for some length L as if almost all of the energy were propagating along a dielectric waveguide.

BOUNDARY CONDITIONS:

A microwave dielectric waveguide, like optical fiber, propagates energy along the guide with nearly all the fields confined within. Any fields outside the waveguide satisfy the boundary condition that fields go to zero at infinity. These fields are similar to a cylindrical metal waveguide and the modes are designated with the same convention. In Figure 2 the transverse electric field (E) and magnetic field (H) of the TE_{01} mode are shown in a dielectric waveguide having a certain rod diameter and frequency (Reference 2). The electric field (E) is in the ø direction and magnetic field (H) is in the r direction.

Assuming the energy in an infinite dielectric waveguide in Figure 2 is propagating in the z direction along the cylinder as shown in Figure 1, this TE_{01} mode (transverse electric) has no component of electric field but must have an H component in the direction of propagation. The two ends of the cylinder are considered an open circuit which reflects most of the energy in



405 MHz PHASED ARRAY

FIG 1

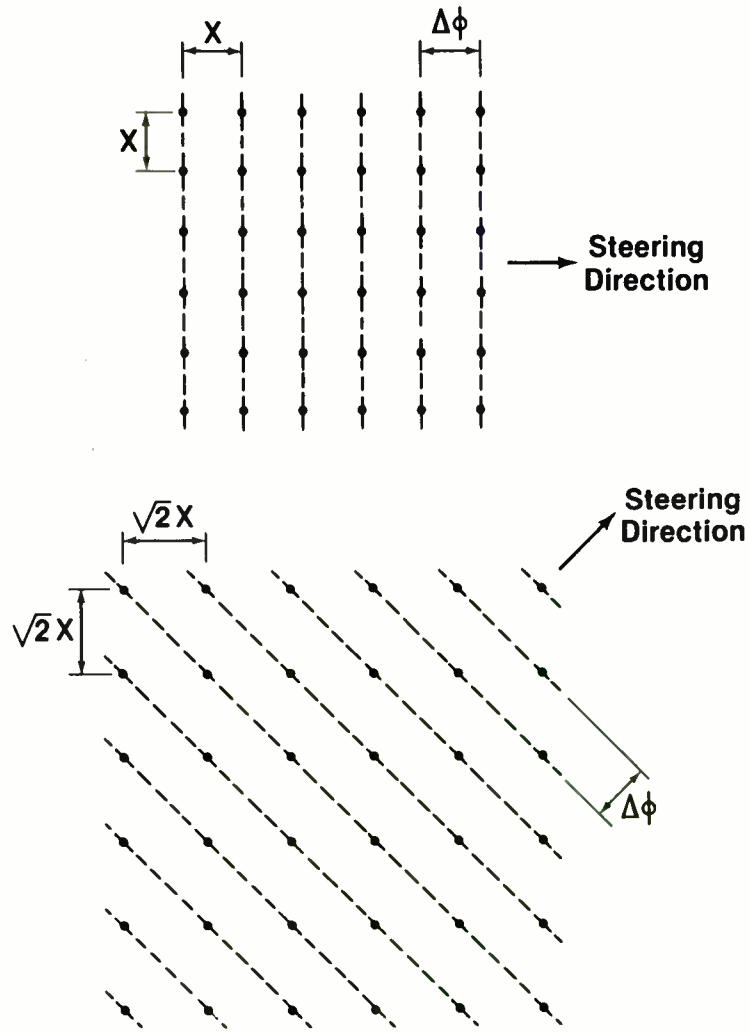


FIG 2

the dielectric waveguide back such that the fields add constructively. This happens when the length is a approximate multiple of half wavelength in the dielectric waveguide.

The perfect magnetic boundary condition is an approximation that applies to the dielectric resonator for this particular field structure. For the cylindrical dielectric waveguide, H_r and H_z are perpendicular to the boundary at the surface. The electric field E_ϕ is tangential at the surface and must be continuous across this boundary.

The permeability μ_r of the dielectric resonator is the same as the free space value μ_o. However, the approximation of a perfect magnetic conductor considers a very large permeability μ so that the magnetic field at the boundary is perpendicular to the boundary. It is applied to the dielectric resonator TE_{01} mode because the symmetry of the magnetic field requires that H_r and H_z are normal to the surface for the cylindrical geometry.

A typical configuration for the electric and magnetic field is shown in Figure 3. This is consistent with the electric field in the ϕ direction and the magnetic field in the radial direction shown explicitly in Figure 2. The magnetic field outside the dielectric resonator is somewhat dipole like as with a large component in the z direction which would be along the length of the cylinder L shown in Figure 1. The E_o and H_r component along the z axis of the cylinder are nearly zero so that a cylindrical hole of dimension D_1 has little affect on the field structure.

Thus, a dielectric resonator is a high dielectric material that has resonances inside the low loss ceramic material that stores the energy in a specific mode. A simple application is shown in Figure 4 where a resonator is placed near a microstrip which has a magnetic field propagating around the conductor and changes directions every half wavelength. The energy from the microstrip is coupled into the delelctric resonator through the magnetic field . For ϵ= 38, about 70 % of the magnetic energy is stored in the dielectric resonator and nearly all of the electric energy is stored inside the dieletric resonator (over 90 %).

The $TE_{01\delta}$ mode has a field stricture similar to a magnetic dipole as shown in Figure 3 where the magnetic field lines are directed along the axis of the dielectric resonator and couple primarily into the top and bottom of the dielectric resonator. Once the energy is coupled into the dielectric resonator, much of it is confined to the dielectric resonator in the $TE_{01\delta}$ resonant mode. The $TE_{01\delta}$ is usually but not always the fundamental mode; under certain conditions it may be the second or third mode.

The magnetic field can couple into the top and bottom of the dielectric resonator providing an H_z component. Consider the field shown in Figure 5 for the $TE_{01\delta}$ mode where the length of the resonant cavity (L) is some multiple δ of half wavelengths. The fields are drawn in a plane through the middle of the dielectric resonator as shown by OO' in Figure 2. H_r and H_z are perpendicular to the boundary and E_ϕ is parallel to the boundary. The dielectric resonator has a soft boundary condition, i.e. the tangential component of electric field E_ϕ and magnetic field H_r and H_r nearly vanishes at the boundary. The magnetic field H_z is normal to the surface at the end of the boundary of the cylinder as shown in Figure 5.

DIELECTRIC RESONATOR ON MICROSTRIP:

As the fields move down the microstrip as shown in Figure 4 and interact with the dielectric resonator, the resonator stores energy in the ceramic material at the resonant frequency and causes a deep notch in the transmission coefficient as shown in Figure 6(a). The reflection coefficient on the other hand peaks at this resonant frequency because the energy stored in the dielectric resonator couples back into the microstrip but travel in the opposite direction as shown in Figure 6(b) (Reference 3).

Assuming a lossless case the sum of the complex reflection coefficient and complex transmission coefficient must be unity (Reference 3):

$$S_{11} + S_{21} = 1 \qquad (1)$$

The real quantities representing the reflection coefficient S_{11o} and transmission coefficients S_{21o} at the resonant frequency of the dielectric resonator can be used to determine the coupling of the dielectric resonator to the microstrip by:

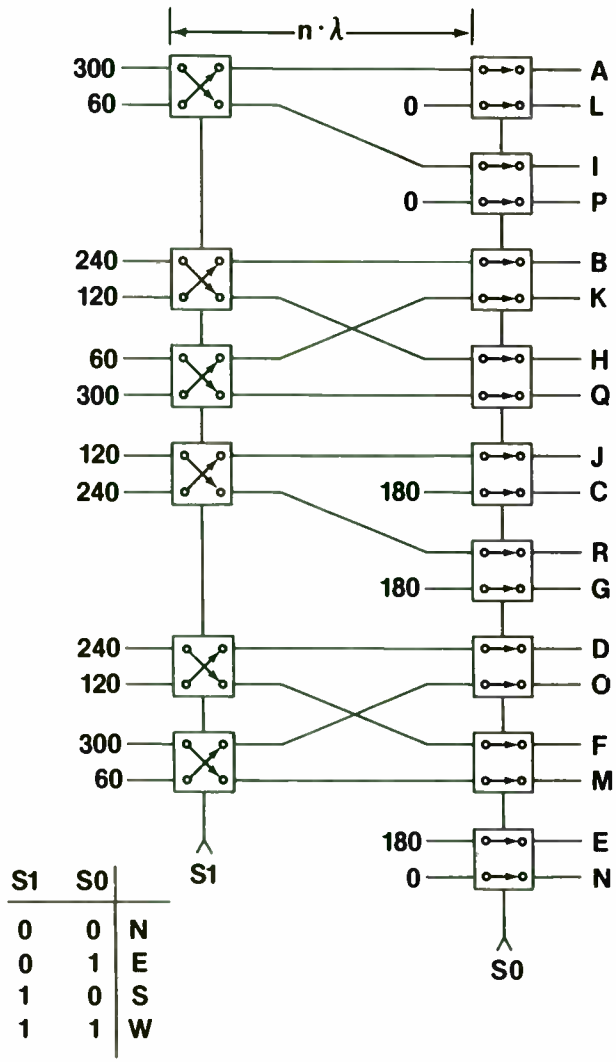
$$\beta = S_{11o}/S_{21o} = R/2Z_o \qquad (2)$$

and the width of the peak at half value is Δ f which relates to the unloaded quality factor (Q_U) of the entire system by:

$$Q_U = f_o/\Delta f \qquad (3)$$

The coupling factor β depends on the distance d of the dielectric resonator from the microstrip line and the location of the dielectric resonator along the microstrip as shown in Figure 7(a). As the distance d is increased, β decreases. Changing the length ℓ ,causes a rotation on a Smith chart of the input reflection coefficient S_{11} into the microstrip. Thus, by changing d and ℓ of the dielectric resonator location with relation to the microstrip, any impedance can be realized looking into the microstrip at the generator. This allows a matching circuit of any value to be generated by a dielectric resonator along a half wavelength microstrip line (Reference 3).

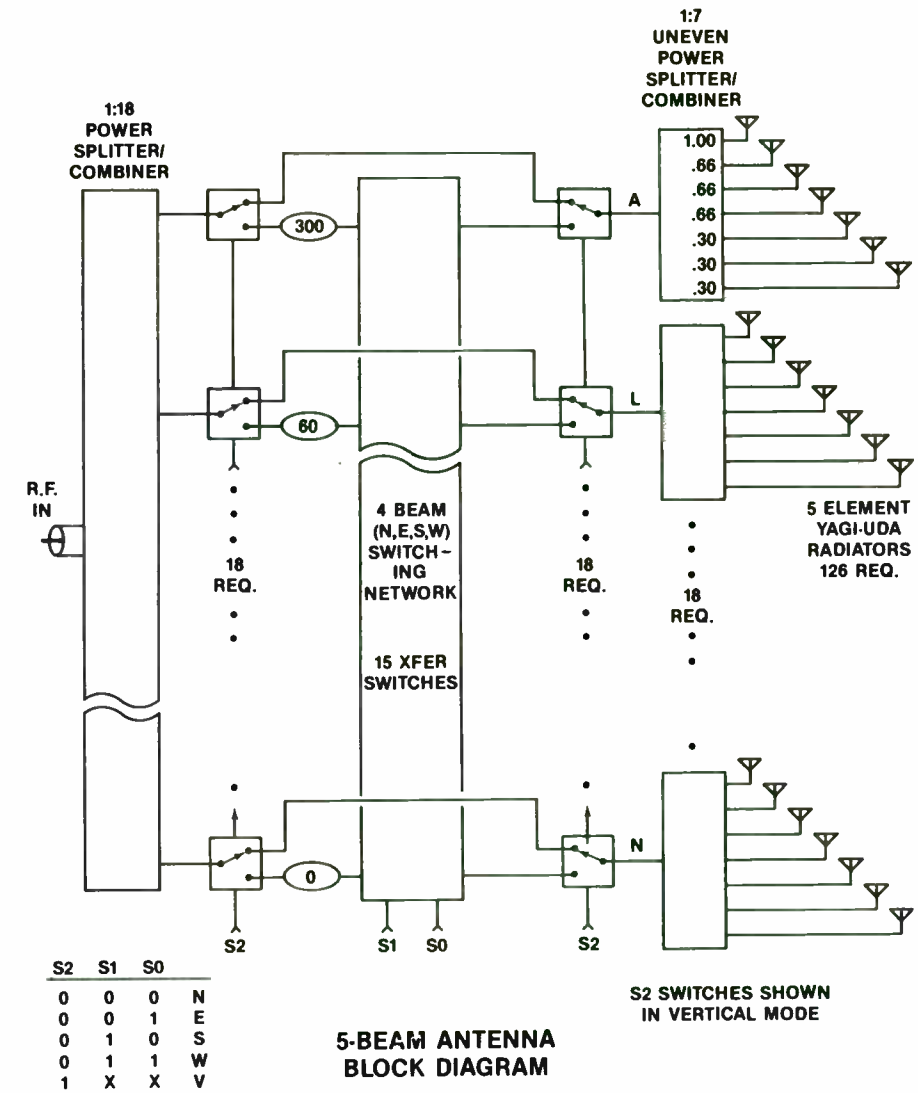
The microstrip with a dielectric resonator in Figure 7 acts as a band reject filter and can be modeled by an



S1	S0	
0	0	N
0	1	E
1	0	S
1	1	W

4 BEAM SWITCHING
(SOUTH PHASING POSITIONS)

FIG 3



S2	S1	S0	
0	0	0	N
0	0	1	E
0	1	0	S
0	1	1	W
1	X	X	V

5-BEAM ANTENNA
BLOCK DIAGRAM

FIG 4

equivalent circuit shown in Figure 7(b). A parallel resistance R, inductance L and capacitance C can be used to model the dielectric resonator coupled to the microstrip of characteristic impedance Z_o. Microwave analysis programs such as Touchstone, Super-Compact and Microwave SPICE have the capability to use parallel or series RLC networks to model these devices. However, the designer must determine the values of R, L and C from the information contained in Equations (2) and (3).

The boundary conditions at the edge of the dielectric resonator do not completely control the resonant frequency because there is energy stored in the field outside of the dielectric resonator. Thus the interface with the substrate is important to the coupling of energy into the dielectric resonator. The metal container that houses the system also becomes part of the resonant circuit and affects the resonant frequency of the dielectric resonator. A dielectric resonator in free space will have a lower resonant frequency than the same material enclosed in a metallic box. In particular, the top and bottom of the cylinder have a large effect if the metallic plate is nearby because the energy cannot couple into the top and bottom of the dielectric resonator.

The support is shown in Figure 8 that holds the dielectric resonator away from the bottom. Ideally, the resonator is equally spaced in the middle of the metal enclosure and the enclosure is as large as possible. Some tuning can be accomplished by moving the dielectric in the metal enclosure and the dimensions of the cavity become more important in the calculations of the resonant frequency.

The quality factor of the resonator Q is affected by the metallic enclosure because energy is absorbed by currents in the non-ideal conducting walls (Reference 4). The amount of surface current in the walls depends on the field structure that is affected by how far away the dielectric resonator is. Basically, the better conductivity of the walls, the higher the Q, and the lower loss within the ceramic material generates a higher Q.

MOUNTING:

Mounting the dielectric resonator on the substrate, the type and thickness of the substrates affects the resonant frequency and the loaded Q the same way the metal container and support affected the resonant frequency. The boundary condition is considered a dielectric constant of ϵ_o outside of the ceramic material so setting the dielectric resonator on the substrate changes the boundary conditions at the substrate resonator interface. In addition, since the substrate is usually thin (20 to 60 thousandths of an inch), the boundary conditions are changed considerably by the metal ground at the base of the microstrip. In particular, this affects the amount of coupled magnetic field that exists in the microstrip substrate coupling into the bottom of the resonator (see Figure 4).

The boundary conditions at a metal wall demand that the tangential electric field vanish, but the dielectric wall boundary conditions require the tangential magnetic field to be vanishingly small; a dual condition. Thus, the metal wall in close proximity to the top of a dielectric cylinder causes drastic changes in the resonant frequency. This condition often comes into effect when a dielectric resonator is placed on a thin substrate. This is the one reason that the dielectric support is used to couple the magnetic field into the dielectric resonator; the other reason is the Q of the system is affected. Since the currents in the metal enclosure cause loss and degrade the Q of the system, the dielectric resonator is best placed equally distant from the metal conductors.

Figure 9(a) shows the usual mounting method of dielectric resonators for Microwave Integrated Circuit (MIC) applications. The dielectric resonator Q_d is deteriorated by epoxy resin, therefore the amount used should be kept to a minimum. In this mounting method, the unloaded quality factor, Q_u, of the device is a function of the Q of the dielectric resonator, cavity and substrate:

$$\frac{1}{Q_u} = \frac{1}{Q_d} + \frac{1}{Q_c} + \frac{1}{Q_s} \quad (4)$$

Another way of mounting the dielectric resonator is shown in Figure 9(b) which uses a support and a plastic screw. Sometimes the screw is not used and the epoxy resin fastens the dielectric resonator and support to the substrate. The configuration shown in Figure 9(b) raises the resonator above the substrate and allows for better coupling through the ends for the magnetic field generated by the microstrip. This method provides the highest unloaded Q_u that is approximately equal to that of the dielectric resonator:

$$Q_u = Q_d \quad (5)$$

TUNABILITY:

The dielectric resonator has an inherent resonant frequency that is determined in a test chamber and is provided by the manufacturer as in Table 1. The ratio of the Length (L_r) to Diameter (D_r), is kept nearly constant at about 0.45 which is chosen for mode separation and performance considerations. The resonant frequency ranges are about 8% for each of MuRata Erie's Part Numbers listed in the table. The resonators are supplied to the lowest frequency of this range. The frequency is measured by the test configuration in Figure 10. A different cavity will have a different resonant frequency for the same dielectric resonator.

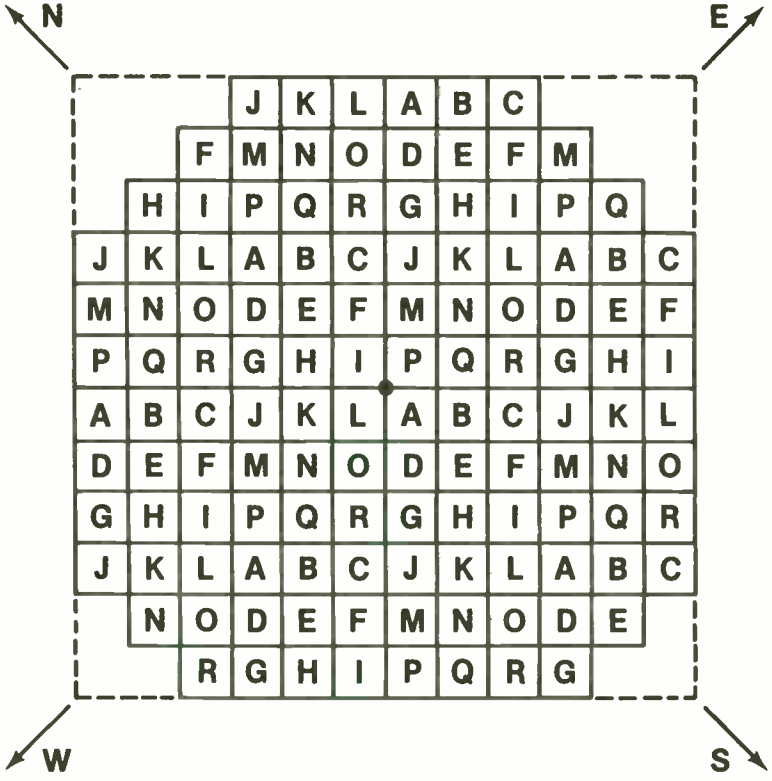
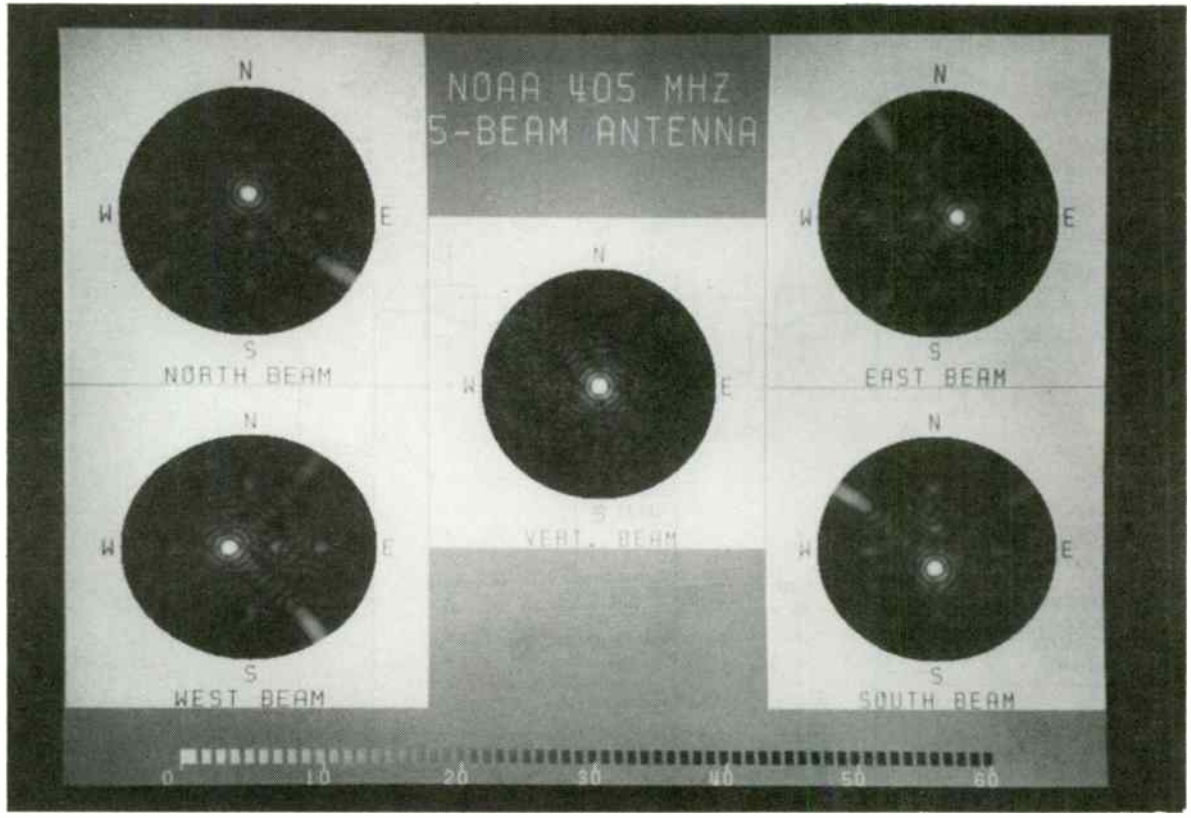


FIG 5



In Figure 10, the resonant frequency and unloaded Q are shown as a function of L_o/L_r. It is seen that for L_o/L_r greater than 3 the frequency ranges between 5.0 and 5.2 GHz and the Q_u between 8300 and 9300. For ratios of frequency L_o/L_r less than 3, variation in frequency is possible but the Q deteriorates rapidly down to 2000. This is due conductivity losses in the cavity walls.

Several methods to adjust the resonant frequency are as follows:

(1) Change the boundary conditions

a) Change cavity dimensions
b) Using tuning stub

(2) Change length L_r of the dielectric resonator.

The most typical approach is to purchase a dielectric resonator from the manufacturer that is pretuned at the lowest frequency as those shown in Table 1.

The resonant frequency can be adjusted by the use of a tuning stub as shown in Figure 11. Typically 3% variation in frequency can be achieved with acceptable Q in many applications as shown in Figure 10.

A second method of tuning is accomplished by moving the dielectric resonator along the microstrip by a distance ℓ or moving it perpendicular to the microstrip a distance d as shown in Figure 7. In general, walls that are more than 3 times the dimensions of the resonator (L_r for height and D_r for radial distances) have little effect on the resonant frequency.

A third method is to change the length of the dielectric resonator L_r physically by grinding. This increases the frequency and can be accomplished by the user or the manufacturer. The manufacturer (MuRata Erie N. A.) can supply dielectric resonators custom machined to the actual dimension. In this case a correlation test cavity should be provided by the end user.

TEMPERATURE COMPENSATION:

The manufacturer can supply a variety of temperature coefficients within a material to compensate for any variance of the substrate or metallic wall due to temperature. These structural changes will change the resonant frequency of the system. By adjustment of the TC of the resonator, the designer can compensate for these effects so as to stabilize frequency with respect to temperature.

The designer usually starts out with a 0 TC dielectric resonator and then measures the variation of the system through the desired temperature range. The dielectric resonator can then be changed to compensate for any variances.

CONCLUSION:

In this article, the physical operation of the dielectric resonator particularly on microstrip inside a metal container has been examined. The resonant frequency is slightly tunable by the location of the dielectric resonator with respect to the microstrip. The size of the container and its location with respect to the dielectric resonator, microstrip and substrate are seen to be important considerations. How does a designer determine what particular dielectric resonator to use?

A computer program has been developed for the IBM PC that stores the particular dielectric resonator dimensions available from MuRata Erie, N. A. for the designer to choose. This program has routines available that calculate the eigenvalues for a configuration from the characteristic equation (Reference 4) by an approximation from Reference 5. The program is menu driven and asks the designer for the dimensions of the cavity, the substrate thickness and dielectric constant. It then calculates the resonant value for this configuration and picks a dielectric resonator from available values for this particular design.

The designer will still have to use the dielectric resonator in a circuit to generate a matching network for an oscillator or filter, but he or she now has the dielectric resonator that is desired for a particular frequency range. The temperature compensation should be done for the system starting with a zero temperature coefficient of frequency and determining the temperature variation and then compensate for it by varying the temperature coefficient of the dielectric resonator. In short, the dielectric resonator offers a unique component in microwave circuits that have a known response at a particular frequency but little affect below that frequency. These dielectric resonators have very high Q so there is little loss in the dielectric resonator even at the resonant frequency. Some tuning is available to adjust for variations in FET or other component values. The resonator is mechanically stable and does not change with time. Many possible uses are available in microwave circuits. It is up to the designers imagination to develop and use this unique component.

ACKNOWLEDGEMENT:

The author wishes to thank T. Nishikawa, J. Fijedziuszko, R. Bonetti, and A Khanna for their technical evaluations of this paper. T. Sudo, J. Alberici and my students at the Pennsylvania State University have provided valuable insight into the information needed by design engineers.

Practical Considerations for Modulating or Pulling The Frequency of a Quartz Crystal Oscillator

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ABSTRACT

The quartz crystal for frequency control is a high Q device. This is another way of saying it doesn't like to have its natural frequency changed by external influences. Yet this is exactly what is attempted in voltage controlled crystal oscillators (VCXO's) or frequency modulated crystal oscillators.

There are parameters in both the oscillator circuit and the cyrstal that must be considered when designing a pullable oscillator. This paper will point out these parameters and try to tell the circuit designer how best to use them.

INTRODUCTION

Two factors must be considered in designing a pullable crystal oscillator. The first is the frequency deviation required and the second the linearity of the deviation. The frequency deviation is generally expressed as parts per million of the operating frequency or total Hertz from nominal frequency. The linearity can be described as the deviation from a straight line of the frequency curve versus the parameter that is controlling it. A secondary effect of the linearity is the amount the frequency is changed in either direction from some center frequency. Examples of this are shown in Figure 1A and 1B.

The oscillator circuit as well as the crystal is important in the control of these two factors. So let's first look at the oscillator circuit design.

THE OSCILLATOR CIRCUIT

I've selected the Pierce Oscillator Circuit because it is the easiest to explain and the most tolerant of errors. The basic circuit is as shown in Figure 2.

In this circuit the collector to emitter (Cce) and base to emitter (Cbe) capacitances are necessary to sustain oscillation. However, their capacitances are very temperature dependent, are not controlled by the manufacturer, and are resistive. Therefore, the performance of the circuit in Figure 2 is marginal. We can improve the performance greatly by placing fixed capacitors in parallel with these junction capacitances. The new Pierce Oscillator will now be as shown in Figure 3.

Resistors R1, R2 and Re provide for the DC bias of the transistor. Re raises the emitter off of ground potential which improves the linearity. Ce bypasses the emitter which must be at RF ground.

We can now replace the transistor with its small signal equivalent circuit. The Pierce oscillator will now appear as in Figure 4.

To simplify the circuit a few assumption can be made. First is that R1 // R2 >> hie and 1/hoe // RL >> XC2. The simplified circuit now appears as in Figure 5.

For the circuit to oscillate, Barkhausen's criteria for oscillation must

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Dimensions and Frequency Range

TABLE 1

Dr ±0.05 (mm)	Lr ±0.05 (mm)	Frequency Range*(GHz)
4.65	2.06	11.46-12.45
5.06	2.24	10.54-11.45
5.50	2.44	9.69-10.53
5.98	2.65	8.91-9.68
6.50	2.88	8.20-8.90
7.07	3.14	7.54-8.19
7.69	3.41	6.93-7.53
8.36	3.71	6.38-6.92
9.09	4.03	5.87-6.37
9.88	4.38	5.40-5.86
10.75	4.77	4.96-5.39
11.68	5.18	4.56-4.95
12.70	5.63	4.20-4.55
13.81	6.13	3.86-4.19
15.02	6.66	3.55-3.85
16.33	7.24	3.27-3.54
17.76	7.88	3.00-3.26
19.31	8.56	2.76-2.99
21.00	9.31	2.54-2.75
22.83	10.13	2.34-2.53
24.82	11.01	2.15-2.33
26.99	11.97	1.98-2.14
29.35	13.02	1.82-1.97
31.91	14.15	1.67-1.81
34.70	15.39	1.54-1.66

* Frequency is measured under the condition: Lr/Lo = 0.33

ADDENDUM

Typical Applications

Typical applications of dielectric resonators are dielectric filter and dielectric resonator oscillators. The following references are papers presented by Murata Manufacturing Co., LTD. regarding dielectric resonators.

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(c) K. Wakino, T. Nishikawa and Y. Ishikawa, "800 MHz Band Channel Dropping Filter Using TM^0_{10} Mode Dielectric Resonator" IEEE MTT-S International Microwave Symposium, IEEE Cat. No. 84CH2034-7, pp. 199-201 (1984).

(d) K. Wakino, T. Nishikawa, S. Tamura and H. Tamura, "An X-Band GaAs FET Oscillators Using A Dielectric Resonator", Proceedings of Ffequency Control Symposium (1983). (In print.)

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(f) K. Wakino, T. Nishikawa, H. Matsumoto and Y. Ishikawa, "Miniaturized Bandpass Filters Using Half Wave Dielectric Resonator With Improved Spurious Response", IEEE MTT-S International Microwave Symposium, IEEE Cat. No. 78CH1279-5, pp. 230-232 (1978).

be met. Barkhausen states that the product of the gains around the loop must be greater than or equal to one. He also states that the phase shift around the loop, at the frequency of oscillation be n(360°) whewn is any integer.

To analyze this further, let's remove the crystal and look into the two terminals that it is connected to. We see this as a two terminal circuit shown in Figure 6.

The impedance seen, looking into the crystal terminals A and B, is a negative resistance (-e) and an equivalent capacitance (C_t) which is the series combination of C_1 and C_2. We can draw this new circuit as shown in Figrue 7.

We now put the crystal back and we have the circuit shown in Figure 8.

A negative resistance corresponds to a gain. Assuming |e| > crystal resistance, then the first constant of Barkhausen's Criteria is met. In order to have the phase shift around the loop be n(360°) the crystal must be inductive to cancel the effect of C_t.

Oscillation starts by the noise generated in the transistor. This noise is fed back to the input of the transistor, in phase, and is further amplified. The crystal, which is in the feedback path, acts as a very narrow band pass filter. The filter allows only the noise to be fed back that is in the pass band of the crystal and controls the frequency of oscillation. This is the natural crystal frequency using C_t as a load.

THE CRYSTAL CIRCUIT

The equivalent circuit of the crystal in the feedback loop is shown in Figure 9, with the formulas for series resonance and parallel resonance added.

The plot of reactance vs. frequency for the fundamental mode is shown in Figure 10. Since the crystal operates inductively in the oscillator circuit, it's reactance would be somewhere between fr and fa.

Pullability and linearity are increased if we operate the crystal at close to series resonance. A good way to do this is to tune out Co with an inductor an add another inductor in series. The revised crystal equivalent circuit would then appear as in Figure 11. If we now plot the reactance vs. frequency curve it would look like Figure 12. Fa has been pulled further away from Fr which allows for more pullability along the inductive region of the curve.

Most crystals are pulled by a capacitor in series with the crystal. This is usually a varactor that can be varied by an external voltage as shown in Figure 13. As the capacitor gets smaller, the frequency of the crystal is shifted upward towards Fa.

The frequency from resonance may be calculated from the equation:

$$D = \frac{Cm \times 10^6}{2(Co + C_L)} \quad \text{parts per million}$$

The pulling sensitivity can be calculated from the equation:

$$S = \frac{-Cm \times 10^{-6}}{2(Co + C_L)^2} \quad \text{ppm/pf}$$

Another useful equation is:

$$fa - fs \cong \frac{fr}{2\,Co/Cm} = fs$$

Note the use of the $\frac{Co}{Cm}$ ratio. This is a popular expression used by the crystal industry. You want this ratio to be as low as possible to get

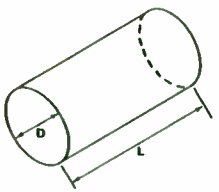

Figure 1. Cylindrical Waveguide of Length L.

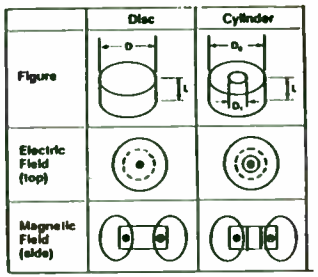

Figure 3. Typical Configuration Electric & Magnetic Fields

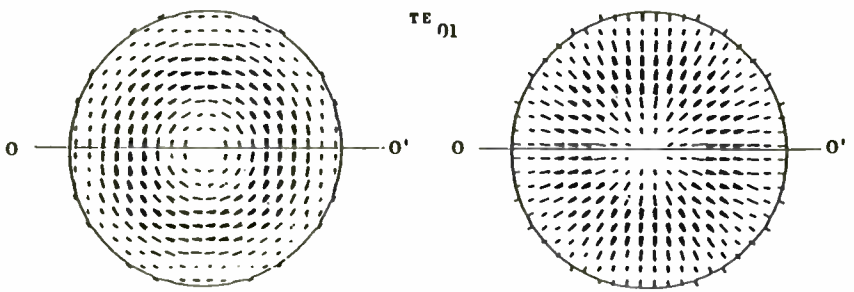

Figure 2. Transverse Electric Field (E) and Magnetic Field (H) for TE_{01} Mode for infinite dielectric waveguide.

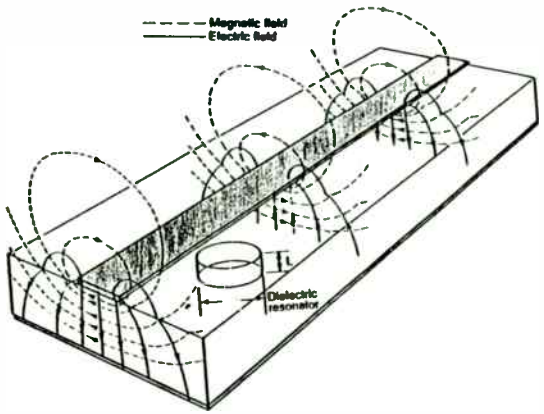

Figure 4. Fields Propagating Along Microstrip with Dielectric Resonator Nearby.

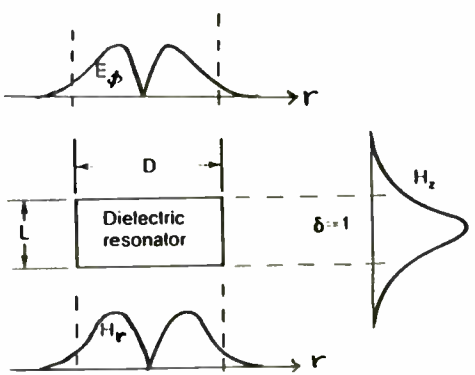

Figure 5. Approximate Field Structure for $TE_{01\delta}$ Mode in Free Space.

the greatest pullability. Typical values of this ratio for quartz crystals are 250 for fundamental mode crystals, 2500 for third overtones and 6500 for fifth overtones.

SUMMARY

We have seen how the crystal and oscillator interface and how one affects the other. The circuit should have ample gain to make certain that it oscillates when the crystal is operated in its reactive or inductive mode. The more the crystal is pulled away from series resonance, the higher is the reactance of the crystal.

For best linearity, and greatest pullability, the circuit should tune out the Co or shunt capacity of the crystal. This can be done with an inductor that resonates with Co at the series resonant frequency of the crystal.

The Co/Cm ration should be as low as possible. For greatest pullability, fundamental mode crystals should be specified. Generally, frequencies in the 8 to 25 Mhz range are preferred.

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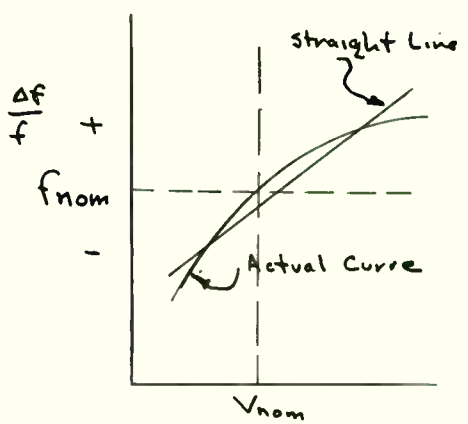
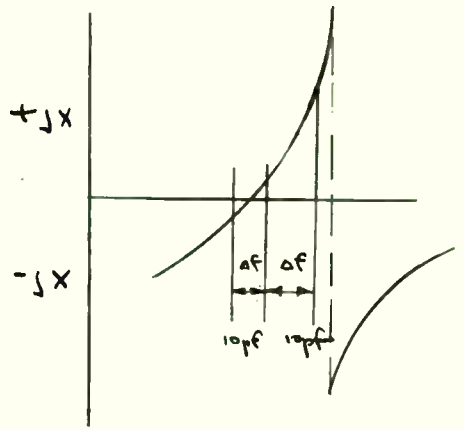


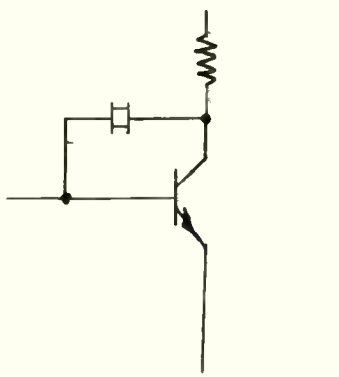
Voltage or Control Parameter

FIG. 1A



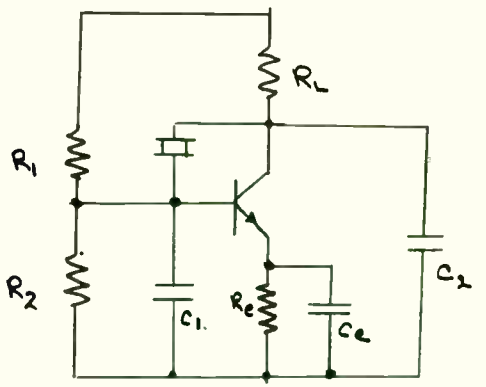
Difference in Pulling Range

FIG. 1B



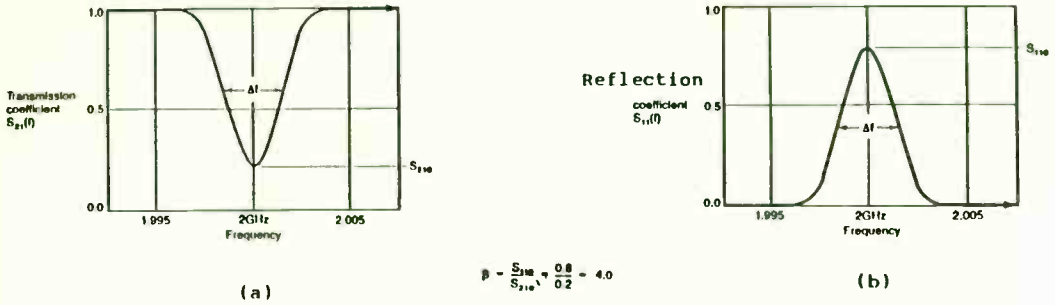
Basic Pierce Oscillator

FIG. 2



Complete Pierce Oscillator

FIG. 3



$$\beta = \frac{S_{21\,min}}{S_{21\,0}} = \frac{0.8}{0.2} = 4.0$$

Figure 6. (a) Transmission coefficient (b) Reflection Coefficient for Dielectric Resonator coupled to microstrip.

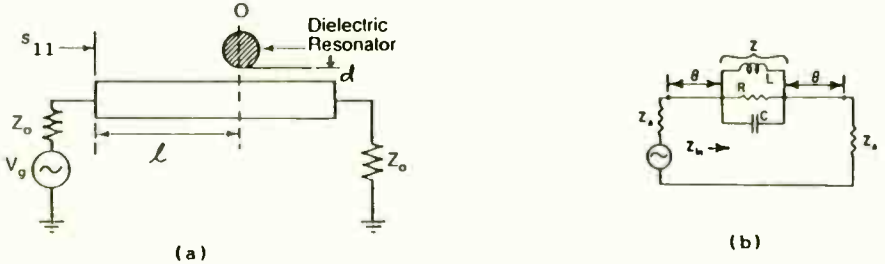


Figure 7. Microstrip of characteristic impedance Z_o coupled to dielectric resonator (a) and its equivalent circuit (b).

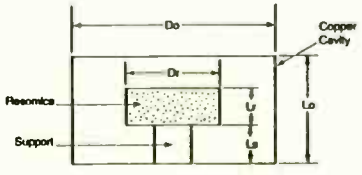


Figure 8. Test Set-up for Dielectric Resonator in Cavity

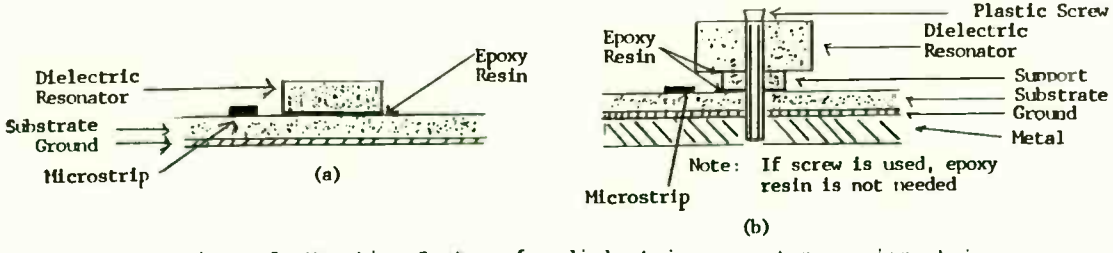


Figure 9. Mounting Systems for dielectric resonator on microstrip

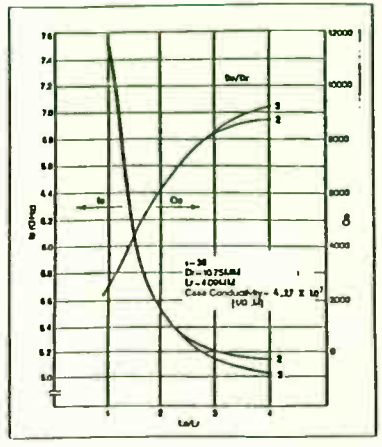


Figure 10. Illustration of the Effects of the Boundary Conditions on f_o, Q_o for U Material Resonators (ϵ_r = 38).

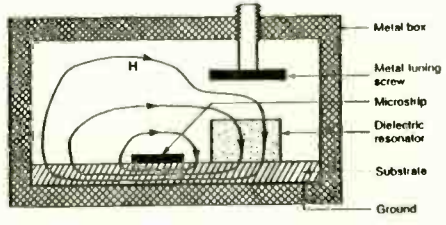
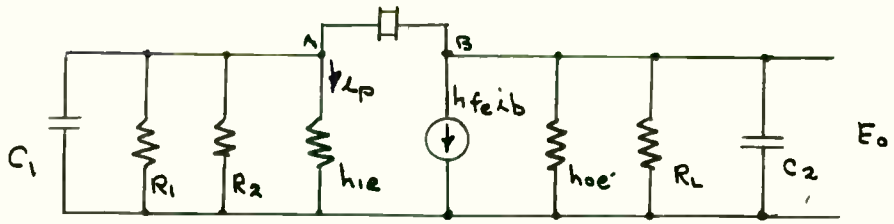
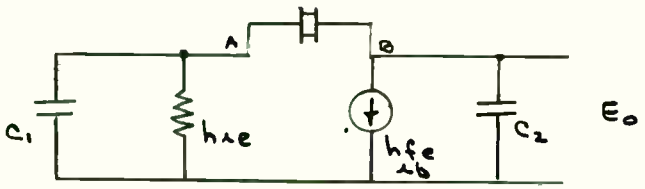


Figure 11. Dielectric Resonator on Substrate with Tuning Stub



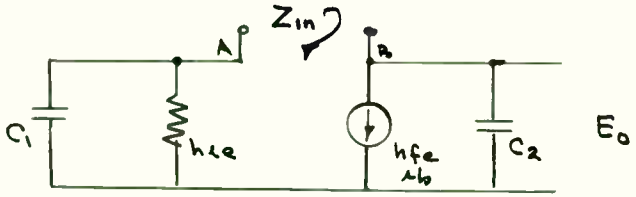
Small Signal Equivalent Circuit

FIG. 4



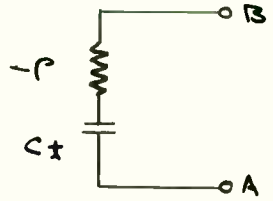
simplified Equivalent Circuit

FIG. 5



Measuring Zin

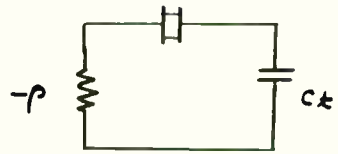
FIG. 6



$$-\rho = \frac{h_{fe}}{h_{ie}} \frac{1}{\omega^2 C_1 C_2}$$

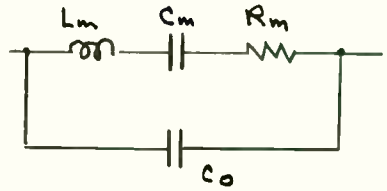
Circuit Further Simplified

FIG. 7



Pierce Oscillator Reduced to Basics

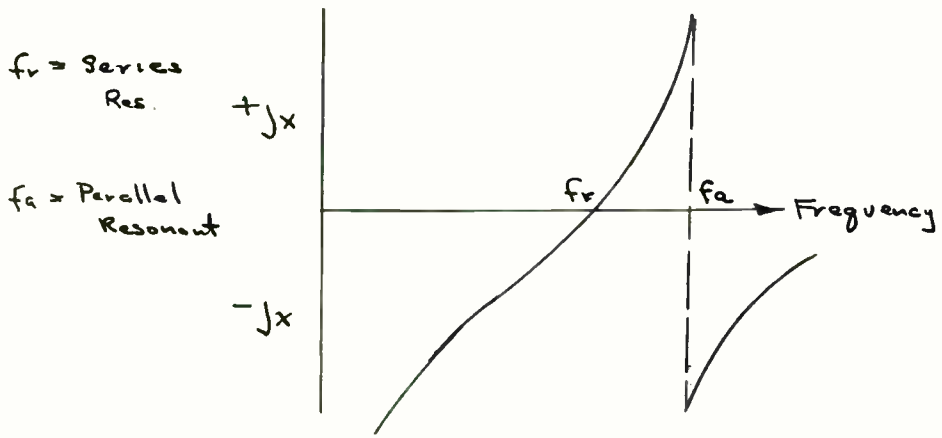
FIG. 8



$$f_r = \frac{1}{2\pi\sqrt{L_m C_m}} \qquad f_a = \frac{1}{2\pi\sqrt{L_m \frac{C_m C_o}{C_m + C_o}}}$$

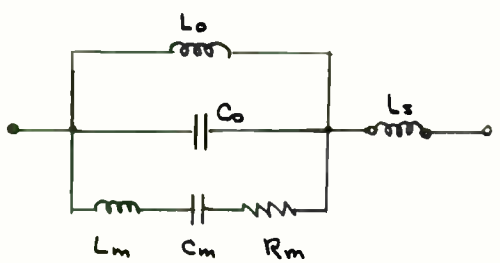
Crystal Equivalent Circuit

FIG. 9



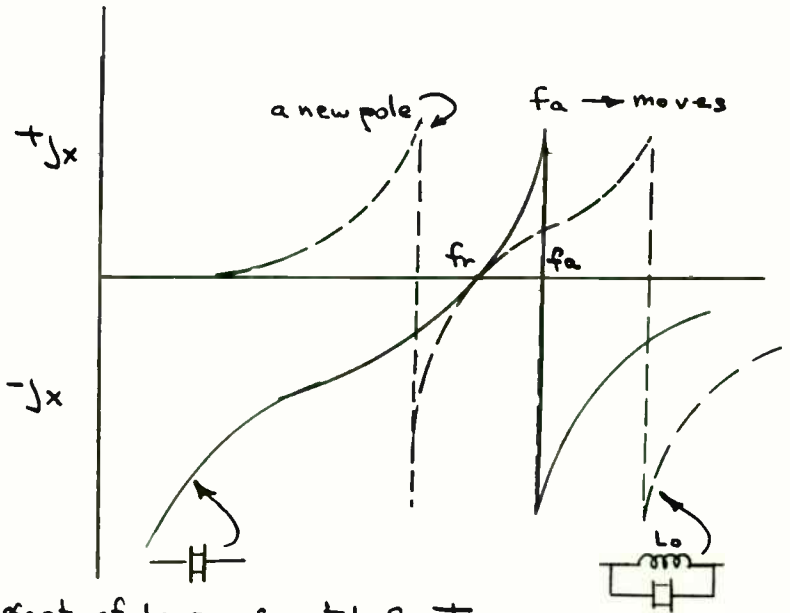
Crystal Reactance Graph vs Frequency

FIG. 10



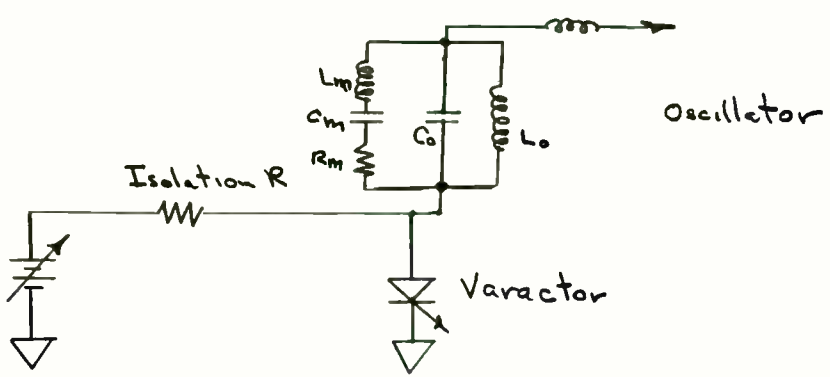
Crystal Equivalent Circuit with added inductances Lo and Ls

FIG. 11



Effect of Lo on Crystal Reactance Graph

FIG. 12



Voltage Controlled Oscillator

FIG. 13

NON-LINEARITY EFFECTS IN RF CIRCUITS

by
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Abstract

This paper illustrates how to derive a model and evaluate key non-linearities for an amplifier and a voltage controlled oscillator (VCO), using a commercially available non-linear Computer-Aided Design (CAD) program called mwSPICE™.

Introduction

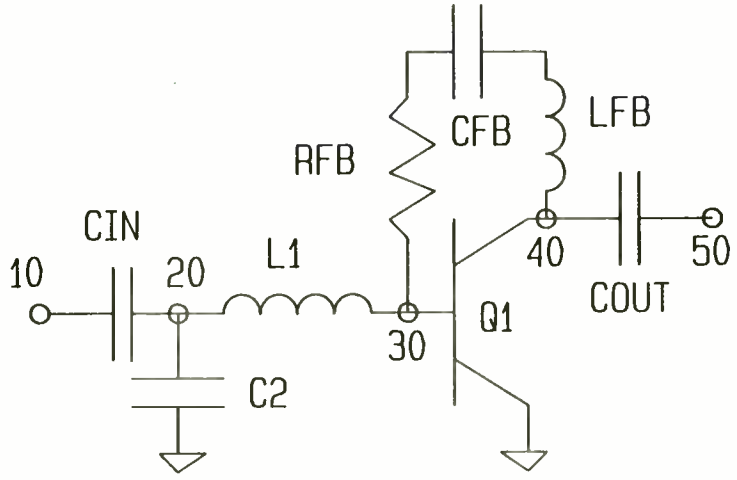
RF and microwave circuit performance can be simulated and accurately predicted using linear analysis programs, provided that the circuit elements are fairly linear. Non-linear elements such as bipolar or field effect transistors are usually modeled in a linear analysis program using small signal S-parameters, which assume the device is operating over a fairly linear region.

These linear programs do not, however, take into account the effects of temperature, harmonics (either generated by the device or introduced into the device), bias supply variations, gain compression or distortion. Some of these effects can be estimated with linear analysis programs but they are strictly done by linear approximation.

This paper focuses on how to use mwSPICE for two different devices, an amplifier and an oscillator, and evaluate device non-linearities. First, amplifier non-linearities which are evident by evaluating the power handling capabilities of a device are presented. Second, critical VCO characteristics such as start up transients, settling time, and frequency versus voltage response are evaluated to insure that steady state oscillation occurs as expected, and that the VCO is operating over a fairly linear range.

Amplifier Design

In this example we've designed a 400 MHZ to 1000 MHZ 16 DB Gain Amplifier as shown in Figure 1.



.4-1GHZ 16DB GAIN AMPLIFIER

FIGURE 1

The amplifier uses a NEC02135 bipolar transistor biased at VCE=10Volts and IC=20ma. As with any linear analysis program, the data for the transistor comes from the manufacturer's data sheet S-parameters. The gain response is shown in Figure 2 and the input and output match is in Figure 3.

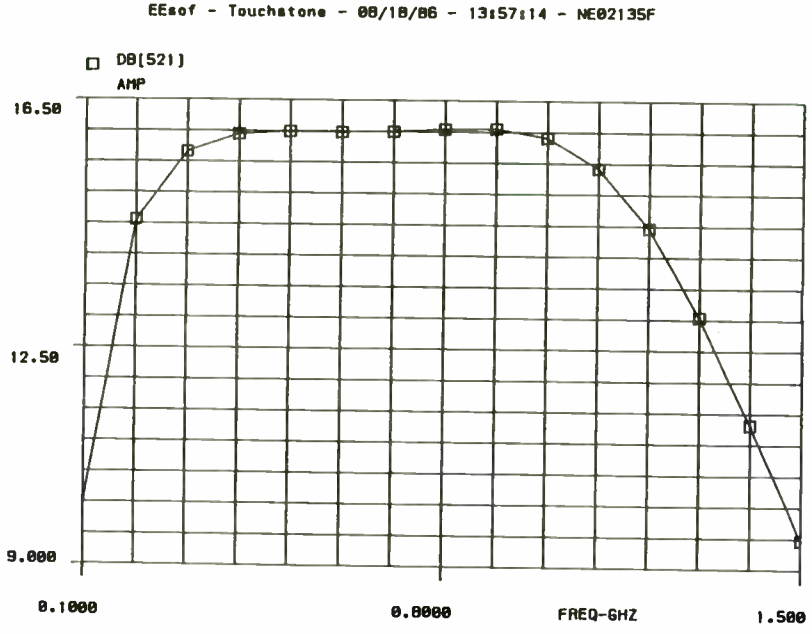


FIGURE 2

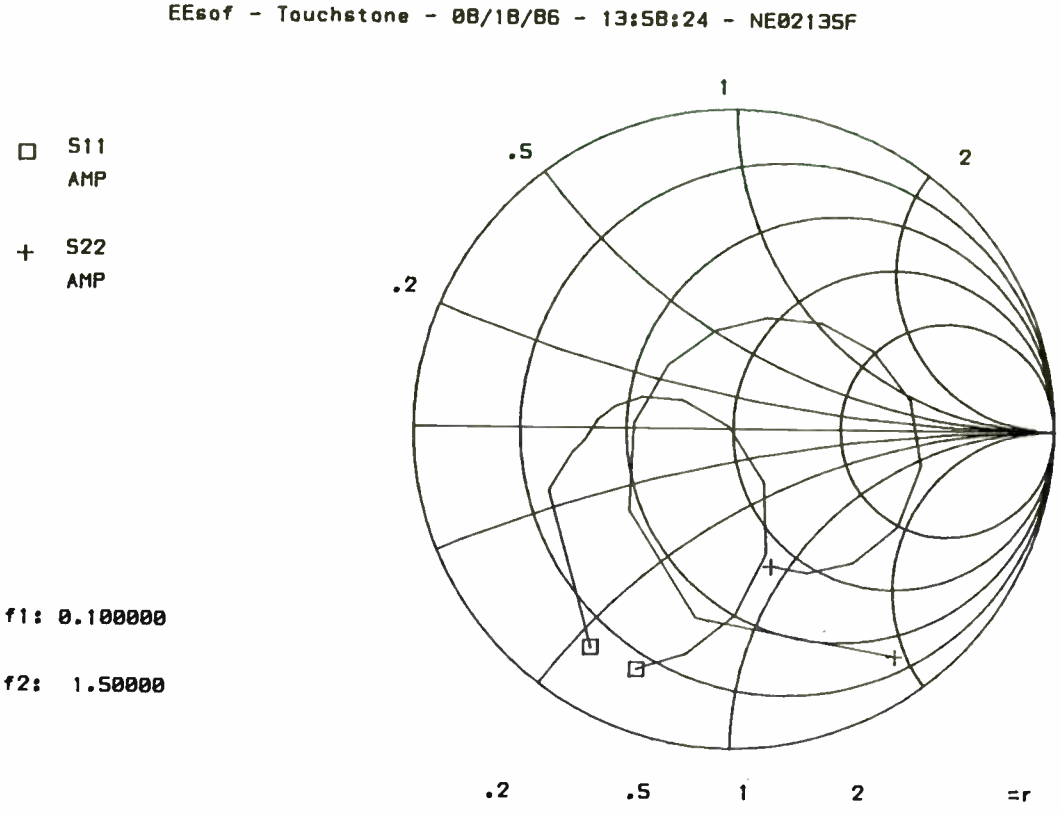


FIGURE 3

S-BAND BUTLER MATRIX FEED NETWORK

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A B S T R A C T

This paper presents the development of a compact microstrip Butler Feed Network at S-band for an eight element linear array. The feed network is developed on a high dielectric constant soft substrate incorporating the entire feed network on a 10" x 10" sheet. The network features the incorporetion of broad band hybrids and phase shifters.

I N T R O D U C T I O N:

Butler Matrix (1, 2, 3, 4) is a passive and theoretically lossless feeding network. This network feeds an array antenna with uniform distribution and constant phase difference between elements. This matrix consists of N inputs and an equal number of output ports. A signal introduced at one input produces equal amplitude excitation at all outputs but with a constant phase different between them, resulting in radiation at a certain angle in space. If the signal is introduced at an other input we will get the radiation at a different angle from the first one.

The network consists of 3 dB hybrids with phase delays in the interconnecting lines. The network has $N = 2^n$ inputs and an equal number of output ports, where n is an integer.

A sketch of an 8 element Butler Matrix is shown in Fig.1. Initially a single piece of broad band coupler and a single piece of broad band phase shifters of values 22.5° 45° and 67.5° were fabricated, tested and optimized before integerating the whole layout. This S-band Butler Feed Network was designed at centre frequency 2.15 GHz with 300 MHz bandwidth on R.T. Duriod 6010.5 0.05 (Er = + 10.5 $\pm$ .25). The measured results obtained were close to theoretical values. This network was also fed to an eight element microstrip linear array to compare the theoretical and practical performance of the beam direction.

Development of Butler Feed Network

The eight element Butler Feed Network without any crossovers is shown in Fig.2. Eight terminals are in middle and the other eight terminals are located on the four sides as shown in Fig.2. The substrate can be grooved in the middle for connections from the sides. We can put the connectors at the back also to avoid grooves in the middle. We can see that the outputs of antenna ports are in horizontal line and the inputs or beam ports are in the vertical line. The 3 dB 90° hybrid was made broadband using G.P. Riblet s(5) technique. The output characteristics, isolation and return loss of this coupler are shown in Fig.3 and Fig.4 respectively.

In order to look at the non-linear characteristics, we will construct a Touchstone/MWSpice circuit file as shown in Figure 4.

```
! 400-1000MHZ Amplifier with 16DB gain
CKT                                          ! Circuit for Touchstone/MWSpice
 CAP_CIN    10 20    C=46.7                   ! Input Network
 CAP_C2     20  0    C=6.29
 IND_L1     20 30    L=1.89
 IND_LL1    30 31    L=1.5            ! Bipolar Transistor VCE=10V IC=20MA
 S2PA_Q1    31 40 70    NE02135.S2P [MODEL=NE02135]
 IND_LFB1   70  0    L=0.3
 RES_RFB    30 33    R=235                    ! Feedback Network
 IND_LFB    33 37    L=5.60
 CAP_CFB    37 40    C=400
 CAP_COUT   40 50    C=14.7                   ! Output Network
DEF2P 10 50 AMP
FREQ                                         ! Touchstone Frequencies
 SWEEP .1 1.5 .1
OUT                                          ! Touchstone Analysis Outputs
 AMP S11
 AMP S22
 AMP DB[S21] GR1
 AMP K
MODEL                                                ! Spice Model for Q1
 NE02135 NPN
 + IS=346.5E-18
 + BF=94.57  IKF=174.9M NF=1.008  ISE=7.101F NE=1.595
 + BR=2.770  IKR=244.4M NR=1.004  ISC=2.953P NC=1.467
 + VAF=27.43 VAR=4.747
 + EG=1.11   XTI=3.0    XTB=0.0
 + RE=1.849  RB=1.2136  RC=1.742       RBM=1.0
 + CJE=4.69P VJE=558M   MJE=37.65M     FC=0.5
 + CJC=.556P VJC=316.4M MJC=34.91M     XCJC=0.35
 + CJS=.56P  VJS=.82    MJS=0.5
 + TF=18P    XTF=0      PTF=38.2  ITF=1.0   TR=.18N
 + AF=1      KF=0
 + IRB=8.2P VTF=1.5
SOURCE                                               ! Bias and RF Sources
 AMP IVS_VCC  100   0 DC=20                          ! VCC=20V
 AMP RES_RCC  100  40 R=472                          ! Collector Bias
 AMP RES_RBB1 40   30 R=7587                         ! Base bias
 AMP RES_RBB2 30    0 R=861                          ! Base bias
! RF Input Source
 AMP IVS_VIN   3    0 AC=1 TRAN=SIN(0 .63 7E9) PWR=(-40 -40 0 7E8 7E8 0)
 AMP RES_RIN   3    7 R=50                           ! Input Load Resistor
 AMP IVS_V1    7   90 DC=0                           ! Power sensing point
 AMP RES_ROUT 50    0 R=50                           ! Output Load Resistor
CONTROL
 AMP AC LIN 15 100MEG 1500MEG                        ! Small Signal Analysis
 AMP TEMP -55 25 125
 AMP TRAN 10PS 4NS 0 10PS                            ! Transient Analysis
 AMP PWR IVS_VIN RES_RIN                             ! Power Analysis
 AMP FOUR .7G V(50)                                  ! Fourier Analysis
SPICEOUT
 AMP AC V(ALL) I(ALL)                                ! Small Signal Output
 AMP TRAN V(ALL) I(ALL)                              ! Transient Output
 AMP PWR IVS_VIN 3 0 IVS_V1 10 0 RES_ROUT 50 0       ! Power Analysis Output
```

FIGURE 4

This circuit file will allow the circuit to be analyzed either in Touchstone or mwSpice. The Model section is added to characterize the device parameters for MWSpice. Also biasing must now be included along with a signal source.

The first non-linear response measured is a standard curve tracer response, Figure 5, of collector current versus collector voltage as determined by base current. In this case base current was varied from 0 to 1 milliamp in .1 milliamp steps. Also plotted is the DC load line for this circuit and the maximum limits based on the manufacturer's data sheet. The maximum VCE is listed as 12V; the maximum collector current is 70 milliamps, and the maximum power dissipation for this package style is 290 milliwatts at 25 degrees centigrade. A point of interest is that the data sheet lists S-parameters for a bias condition of VCE=10V and IC=30ma for this package which is outside of their own power dissipation limits at 25 degrees centigrade, to say nothing of 85 or 125 degrees.

If we were planning to use this amplifier with a 0 dbm input signal and expecting to get 16 DB gain, think again. Figure 6 shows that as the input power in dbm (the X axis) is increased, the gain decreases from about 16 DB at -40 DBm in, down to 11.5 DB gain with 0 DBbm in. Figure 7 shows a time domain analysis of the output waveform with 1-milliwatt (0 DBm) input. As you can see there is a significant amount of distortion on the waveform.

The phase response of this coupler is shown in Fig.5. A broad band phase shifter was designed on the basis of techniques given by Darko Kajfez(6). One-piece phase shifters of value 22.5°, 45° and 67.5° were fabricated and tested. Their response are shown in Figures (6), (7), and (8). We can see that in the case of the coupler the imbalance is within 0.3 dB throughout the frequency band. The phase is also within 92°, with slightly more variation in the lower side of the frequency. The isolation and the return loss are greater than 25 dB throughout the band. The variation of the phase values in 67.5°, 45° and 22.5° phase shifters in the 300 MHz band are + 0.5° ± 1.5° ± 3°. The actual layout of the coupler and phase shifter is shown in Fig.9(a) and 9(b). Using the coupler and phase shifters a compact integrated layout was made to fit within 10" x 10" sheet of R.T. Duroid 6010.5 dielectric. The layout is shown in Fig.(10).

Experimental Results on Butler Feed Network

The S-band Butler Feed network connected to the eight element microstrip linear array is shown in the photograph. The photograph also shows the far field pattern of this antenna fed by the Butler Matrix. Connectors to the eight inputs and eight outputs are made from the bottom.

The insertion loss of the matrix is of the order of 2.0 dB. The matrix provides a uniform illumination of the array. However, variations in the coupling ratios of the 90° hybrid couplers and difference in the insertion loss between the reference line and coupled lines of the phase shifter cause amplitude errors in the illuminations. The worst amplitude error is 1.8 dB. Phase errors in the array illuminations average ± 6° for all beams. The maximum phase variation is 12°. The return loss of input port 3L is given in Fig.11. In the 300 MHz band the average return loss is 22dB. The average isolation is 25 dB with the lowest value of 18 dB. The antenna terminals of the matrix are isolated from each other in the same manner. The average isolation is 23 dB.

POSITION OF BEAM PEAKS

We know that the normalized magnitude of the field intensity in the far field of a linear array of a isotropic sources is given by

$$|E| = \frac{\sin(n\psi/2)}{n \times \sin(\psi/2)}$$

where $\psi = \frac{2\pi d}{\lambda} \sin(\alpha) - \delta$

d = element spacing = 0.52λ in our case

λ = Wave length

α = angle from the array normal

and δ = element to element phase shift $= \frac{(2p-1)}{n} \frac{\pi}{2}$

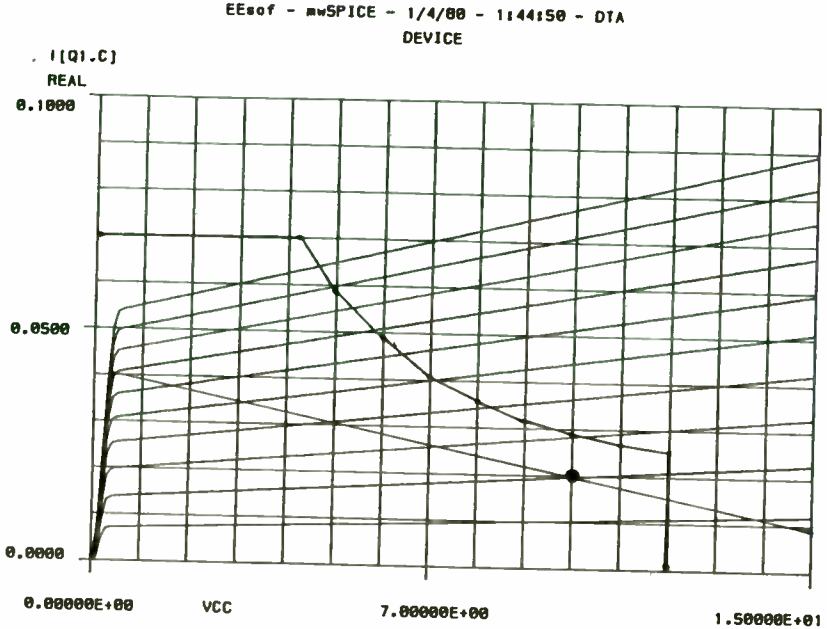

FIGURE 5

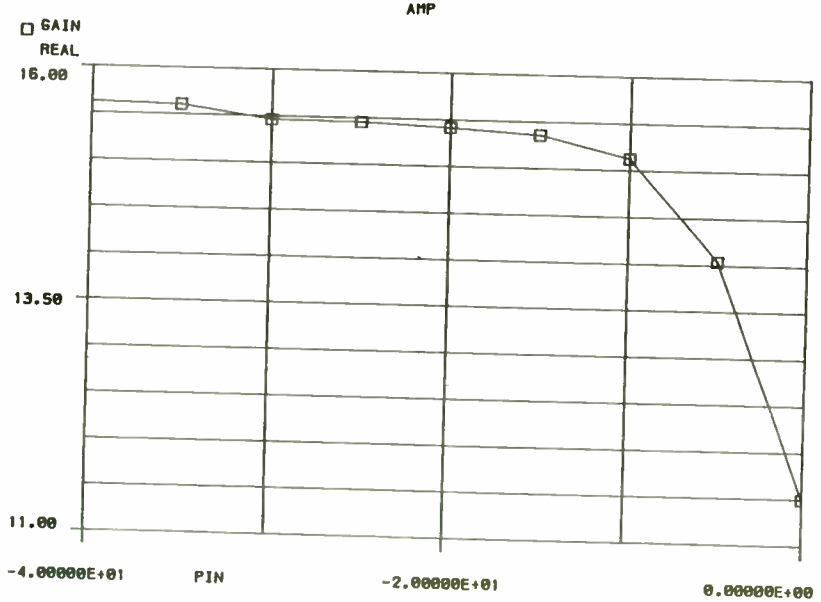

FIGURE 6

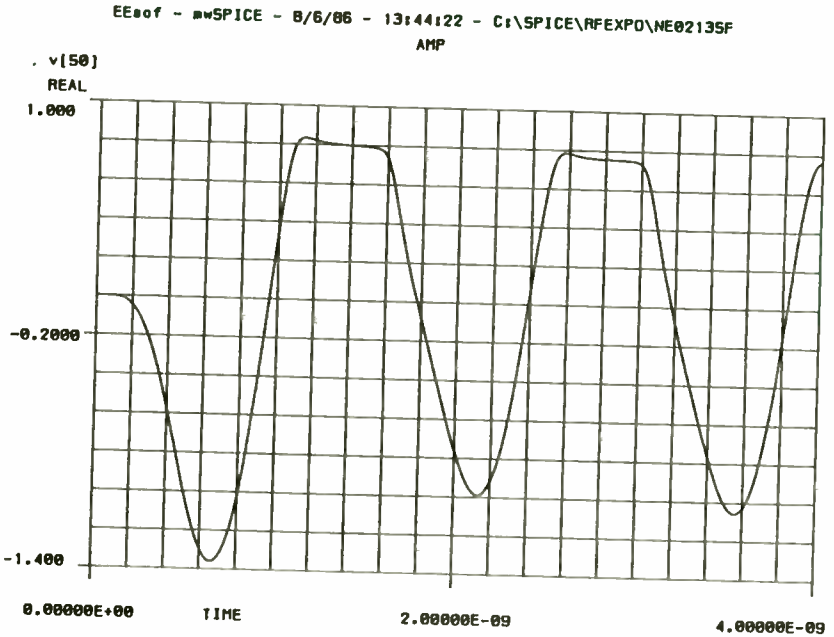

FIGURE 7

p = beam numbers = ± 1, ± 2, ±3, and ± 4 (in our case)
i.e. the position of the beam peaks are given by

$$\mathrm{Sin}^{-1}\left(\frac{\lambda}{n\,d} (nq + p - 1/2) \right)$$

The theoretical beam angles are 7°, 21°, 37°, and 57° on each side from the broad side direction.

The position of the main beam is shown in the Fig.12 which is very close to the predicted value. We also see that beam cross-over level is about -3dB which is also close to theoretical value -3.86 dB. The small variation may be due to deviation from the uniform illumination.

The first side level is -12.5 dB compared to -13.2 dB. The difference is due to error in phase values from the theoretical phases in the outputs.

CONCLUSIONS

This feed network can work well up to 300 MHz about the 2.15 GHz centre frequency. The response of the feed networks deviate a bit at the band edges due to increased amplitude imbalance and deviation of phase from 90° between the outputs of the coupler. The phase shifter also introduces phase error, though small at band edges. Slight phase error was also introduced while mounting the connectors.

Taking proper care in development and mounting, the average insertion loss and the phase variation can still be reduced from 2.2 dB and ± 6°. The band width of the matrix can be still further increased to 500 MHz by increasing the bandwidth of the coupler. The designed phase shifters can work well upto 500 MHz about 2.15 GHz.

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2. J.P.Shilton and K.S.Kelleher : Multiple beam to linear arrays , IRE-T and AP pp. 154-161, March 1961.

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5. G.P.Riblet : A directional coupler with very flat coupling , IEEE, T-MTT, Feb. 1978, pp. 70-74, correction in Sept.1978 pp.691.

6. Darko Kajfej : Flatten the response of phase shifters, Microwaves Dec.1978, pp.64-68.

And as you'd expect a fourier analysis reveals the second harmonic is only about 14DB below the fundamental as shown below.

**** FOURIER ANALYSIS TEMPERATURE = 27.000 DEG C

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(50)

DC COMPONENT = 4.244D-02

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	DB BELOW CARRIER
1	7.000D+08	9.541D-01	1.000000	
2	1.400D+09	1.929D-01	.202218	-13.89
3	2.100D+09	1.017D-01	.106567	-19.45
4	2.800D+09	8.223D-03	.008619	-41.29
5	3.500D+09	2.324D-02	.024357	-32.27
6	4.200D+09	1.263D-02	.013239	-37.56
7	4.900D+09	3.082D-03	.003230	-49.82
8	5.600D+09	5.324D-03	.005580	-45.07
9	6.300D+09	2.091D-03	.002192	-53.18

TOTAL HARMONIC DISTORTION = 23.051669 PERCENT

In Figure 8 the performance of the amplifier was analyzed at -55, 25, and 125 degrees centigrade. It can be seen that gain varies about +/-.5 DB over that temperature range. Different biasing methods could be quickly tried if temperature stability is a concern.

In this quick overview you can see that ignoring non-linearities can result in unpleasant surprises when the actual circuits are built. By using a non-linear design tool such as mwSpice we can analyze effects that would have required a considerable amount of time and equipment to bench test.

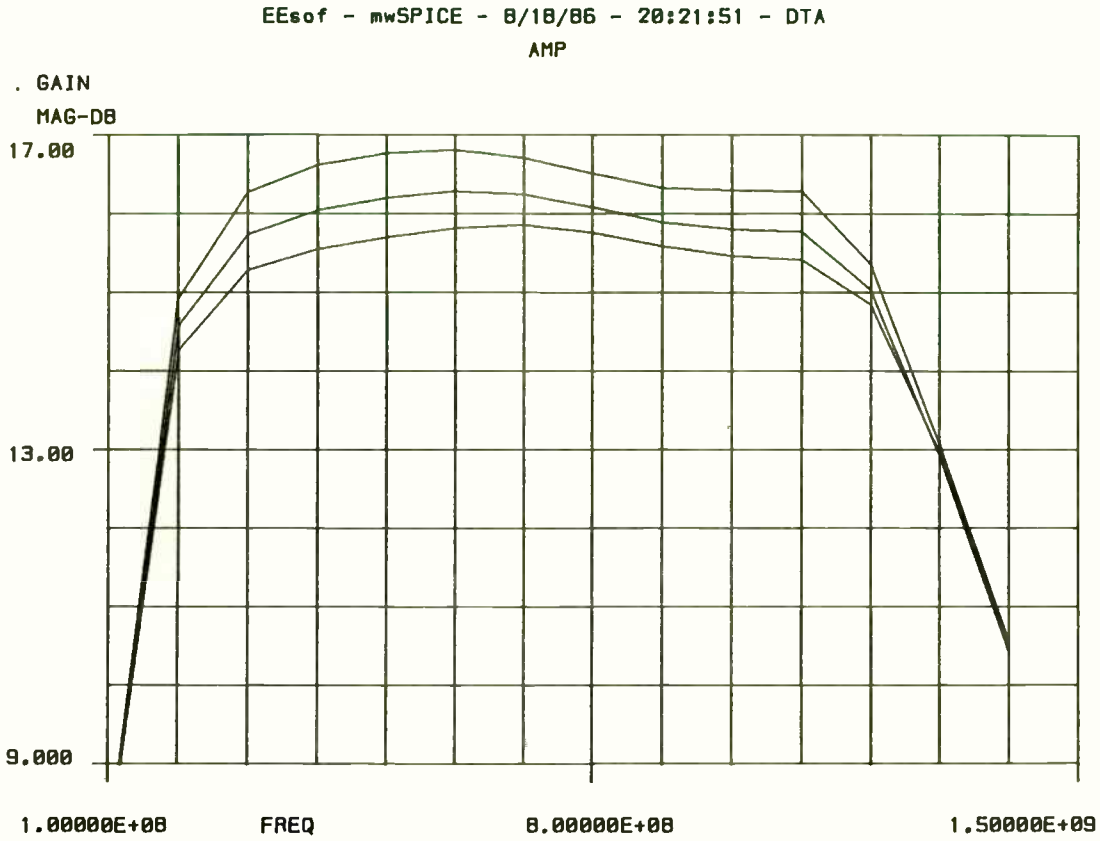


FIGURE 8

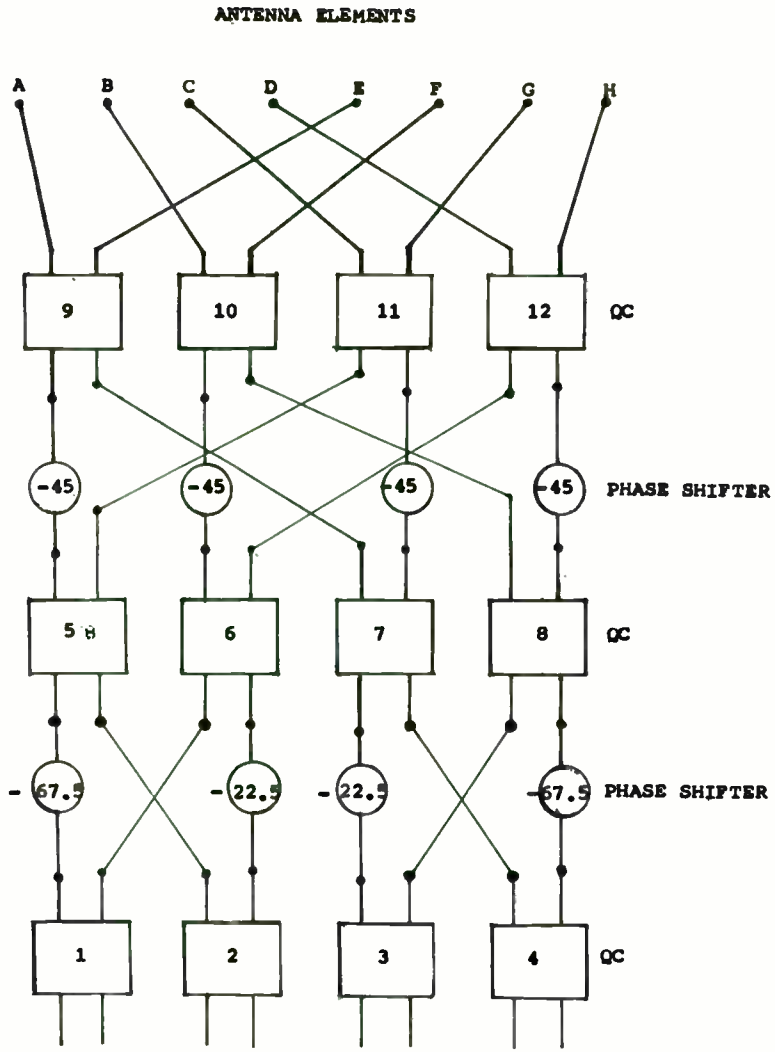


Fig.1 Eight element Butler beam forming matrix

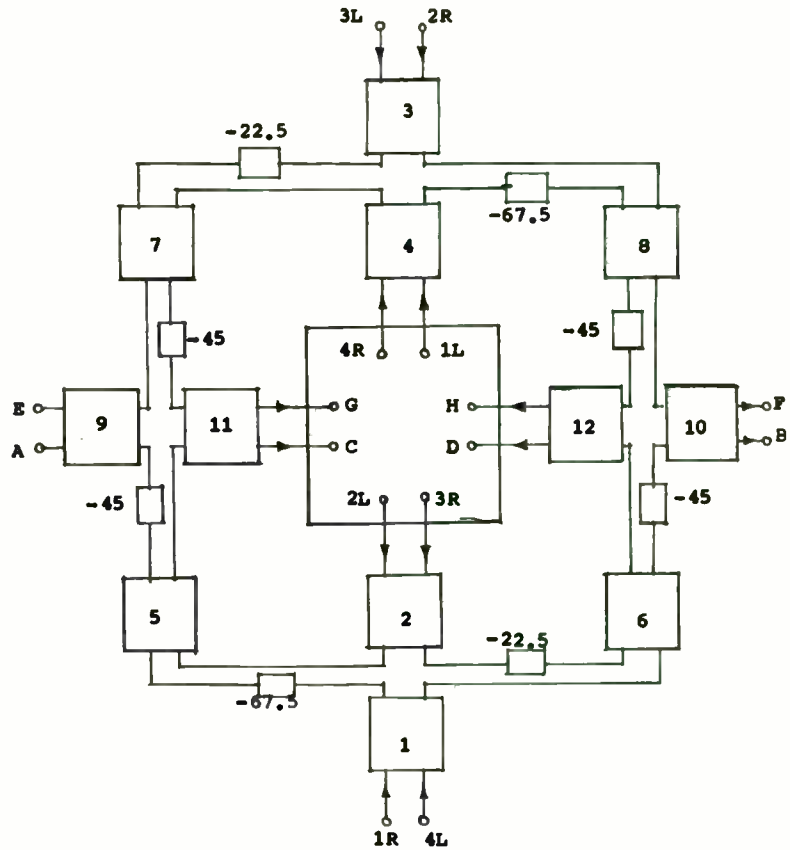


Fig.2 Butler Feed Network without Cross-overs

Voltage Controlled Oscillator, VCO

Linear analysis programs have been used in the past for oscillator design. Typically, the design procedure is to maximize the small signal S-parameters, S11' or S22', so that the real part of the device reflection coefficient becomes negative. Linear analysis programs use optimization algorithms to maximize S11' or S22', as determined by the design. So, to design an oscillator using a linear analysis program requires device small signal S-parameters to characterize the active device.

With non-linear analysis programs such as mwSPICE, device characterization consists of supplying AC and DC parameters, as well as proper biasing conditions as shown in Figure 9.

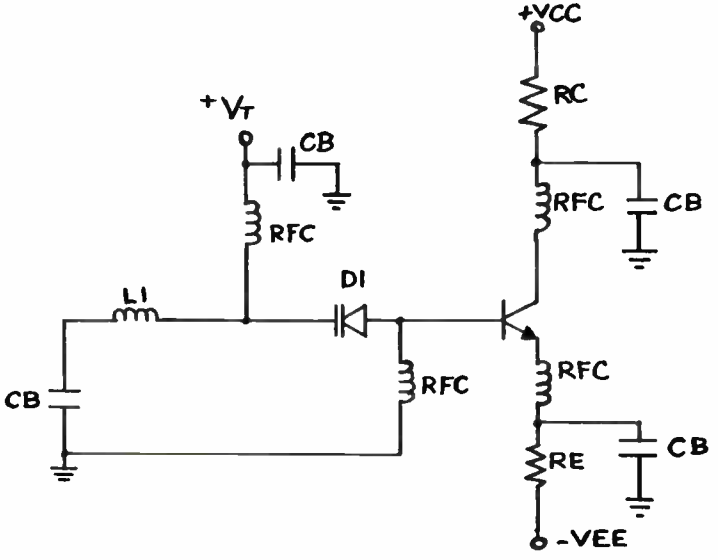


FIGURE 9 VCO Schematic

The idea of the VCO is to vary the tuning voltage applied to diode D1 which will change the junction capacitance of the diode (the diode, when used for it's variable capacitanoe properties is referred to as a varactor). This will in turn, change the resonant frequency of the equivalent resonant AC network consisting of the series inductance, the internal diode capacitance, and the transistor internal capacitance. The complete circuit description is shown in Figure 10.

```
DIM
  FREQ MHZ          OSC IVS_VEE 31 0 DC=-10
  CAP PF            OSC IVS_VCC 41 0 DC=10
  IND UH            OSC IVS_VT 20 0 DC=10
VAR                 OSC RES_RE 30 31 R=930
  CB=1000           OSC RES_RC 40 41 R=1000
  RFC=100
CKT
  CAP_CBP1 1 0 C^CB
  IND_L1 1 4 L=4.56
  IND_LRFC1 4 20 L^RFC
  CAP_CBP2 20 0 C^CB
  S1PA_D1 4 5 [MODEL=DIODE]
  IND_LRFC2 5 0 L^RFC
  S2PA_Q1 5 6 7 [MODEL=T2N918]
  IND_LRFC3 7 30 L^RFC
  CAP_CBP3 7 0 C^CB
  RED_LN 3 6 L=3.82
  RES_R2 6 0 R=1510
  CAP_CR2 6 0 C=826
  CAP_CN 3 0 C=79.6
  CAP_CBPL 3 7 C=1000
  CAP_CBPC 2 0 C=1000
DEF1P 7 OSC
MODEL
       T2N918 NPN( BF=69.47 C2=39.3 NE=1.5 IK=0.025
+ IS=1.55E-15 VA=100.0 VB=20.0 BR=0.573 C4=0.0 NC=1.5 IKR=0.025
+ CJC=1.75E-12 MC=0.120 PC=0.800 CJE=2.22E-12 ME=0.150 PE=0.500
+ RC=11.500 RB=12.000 RE=8.50 TF=2.14E-10 TR=3.27E-08 )
       DIODE D IS=1E-15 CJO=.5PF TT=.1NS
SOURCE
```

Figure 10. Circuit description of VCO

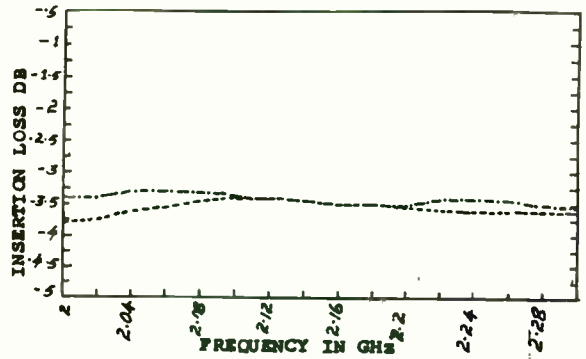


FIG.3 RESPONSE OF COUPLED AND DIRECT PORTS OF BROADBAND COUPLER

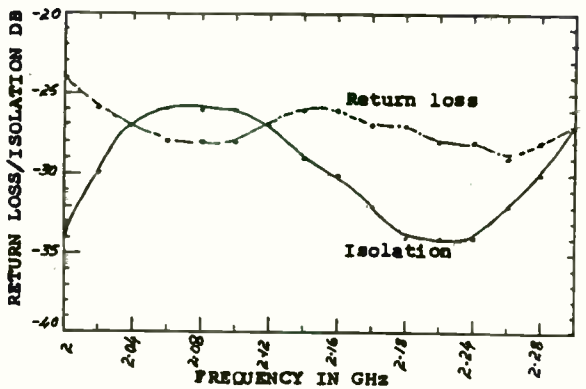


FIG.4 RESPONSE OF ISOLATION AND RETURN LOSS OF BROADBAND COUPLER

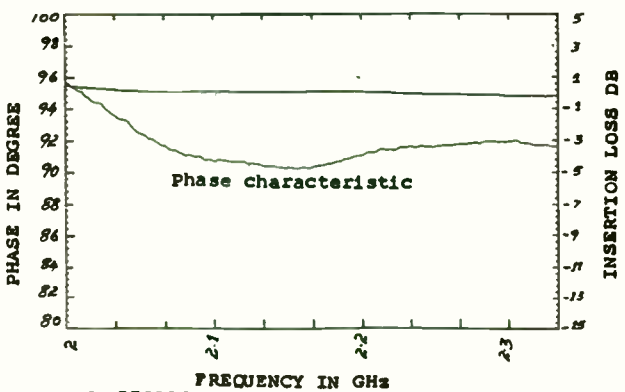


FIG.5 RESPONSE OF PHASE AND I/L OF 3 DB COUPLER

FIG.6 22.5 DEG PHA SHIF

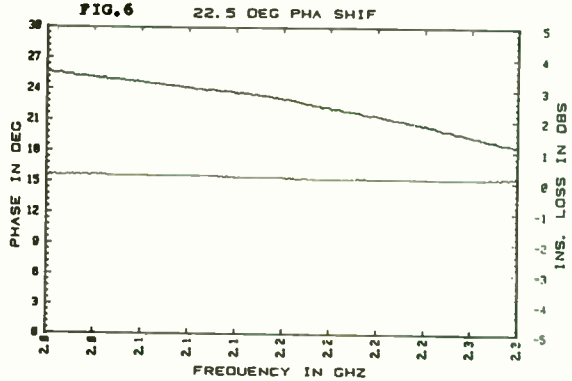


FIG.7 45 DEG PHA-SHIF

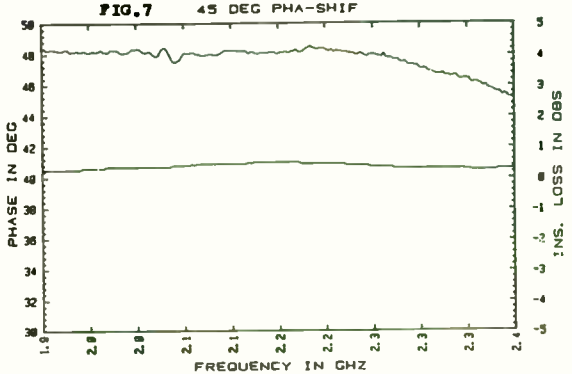
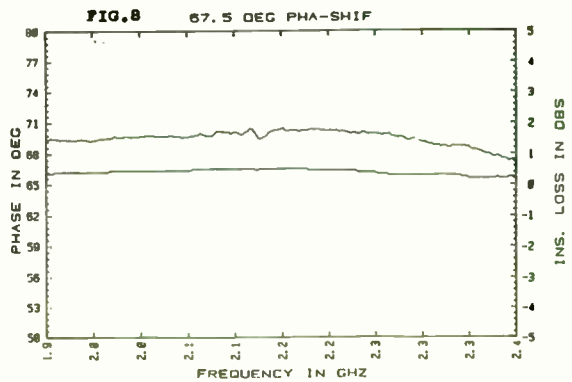


FIG.8 67.5 DEG PHA-SHIF



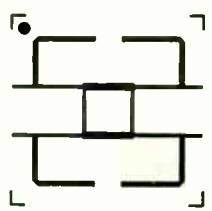


FIG.9(a) 3 dB BROAD BAND COUPLER

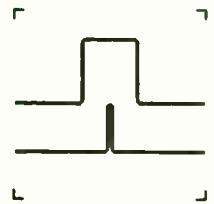


FIG.9(b) 67.5° PHASE SHIFTE

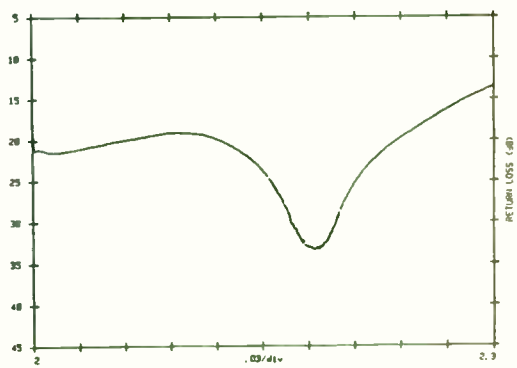


FIG.11 RESPONSE OF R/L AT 3L I/P PORT

The Gummel-Poon model for a 2N918 bipolar junction transistor is used in this example, with the parameters indicated in Figure 11.

BF=59.47	Ideal maximum forward beta
C2=39.3pf	B-E leadage saturation current
NE=1.5	B-E leakage emission coefficient
IK=0.025	Forward knee current
IS=1.55E-15	Transport saturation current
VA=100.0	Forward early voltage
VB=20.0	Reverse early voltage
BR=0.573	Ideal maximum reverse beta
NC=1.5	B-C leakage emission coefficient
IKR=0.025	Reverse knee current
CJC=1.75E-12	Zero bias B-C junction capacitance
MC=0.120	B-C grading coefficient
PC=0.800	B-C junction built-in potential
CJE=2.22E-12	Zero-bias B-E juntion capacitance
ME=0.150	B-E grading coefficient
PE=0.500	B-E junction potential
RC=11.500	Collector resistance
RB=12.000	Base resistance
RE=8.50	Emitter resistance
TF=2.14E-10	Forward transit time
TR=3.27E-08	Reverse transit time

Figure 11. BJT parameters

The initial transient solution for the VCO, shown in Figure 12, indicates sustained oscillation after approximately 8 nanoseconds. Start-up transients don't seem to be a problem.

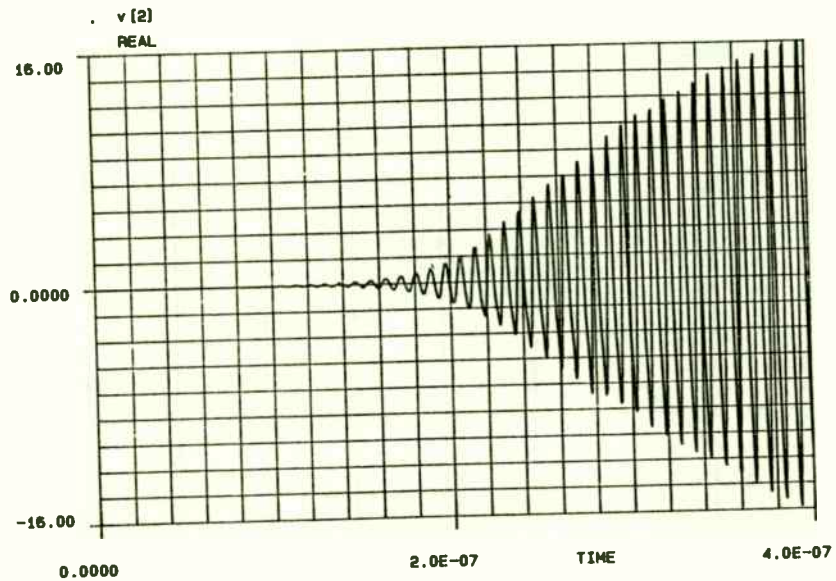


Figure 12. Initial Transient Solution

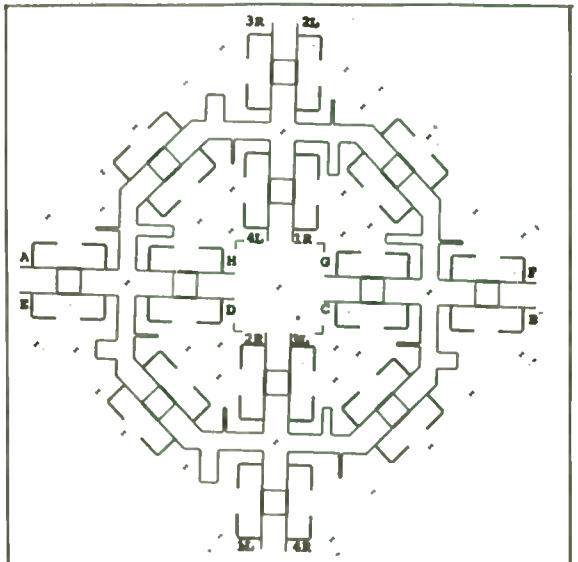


Fig.10 Actual integrated layout of Butler Feed Network for 8 element linear array.

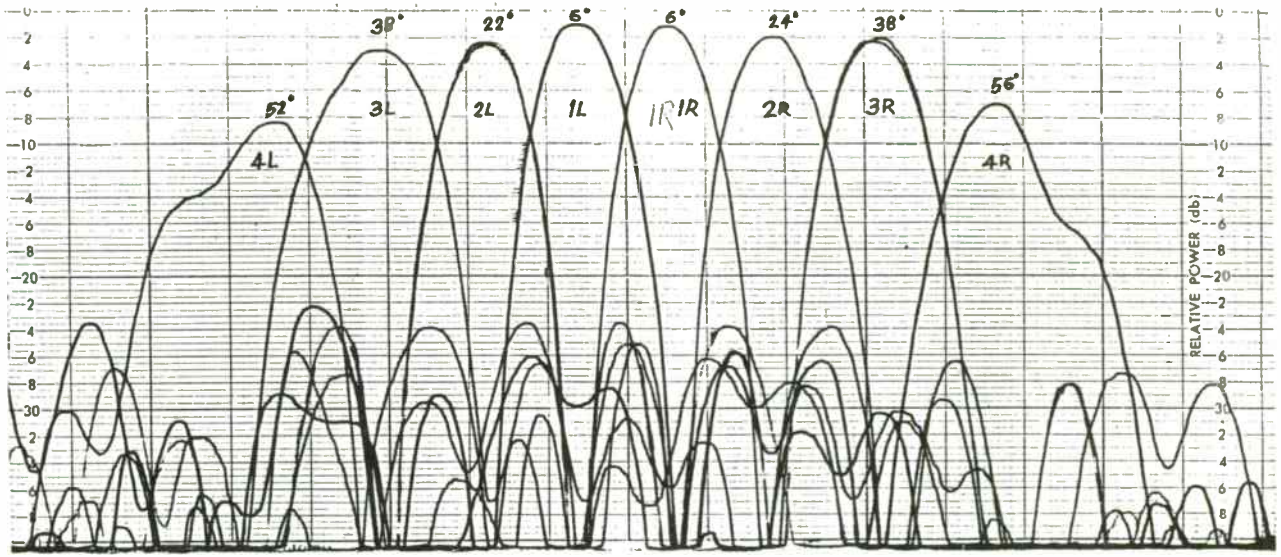
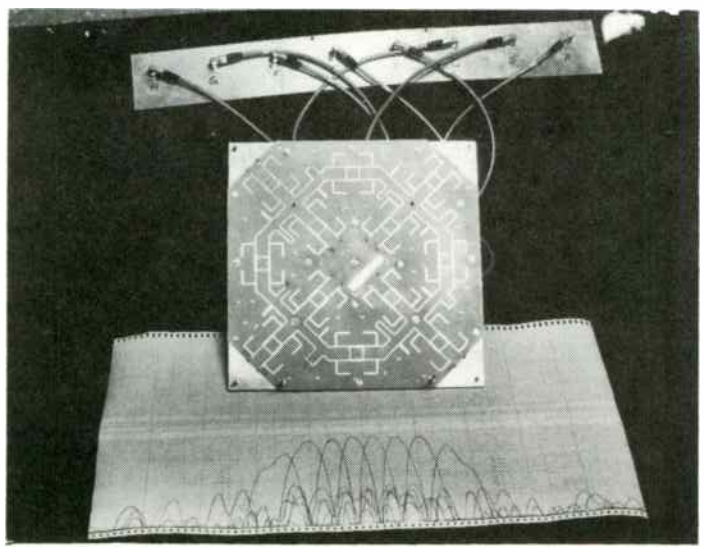
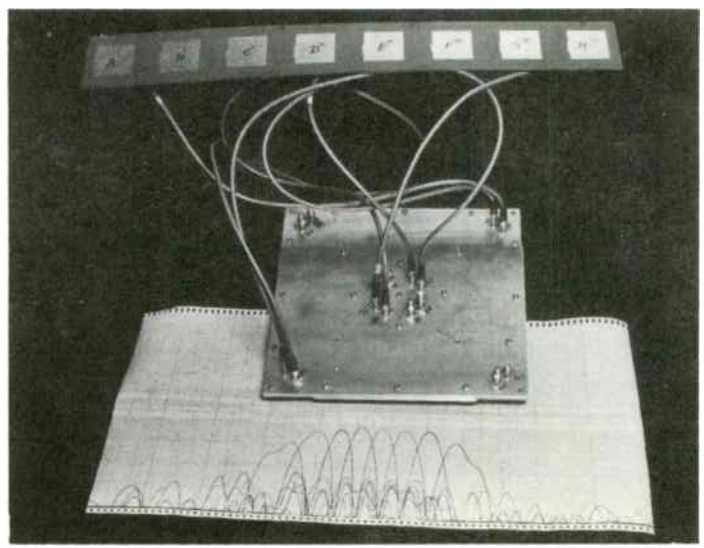


FIG.12 MAJOR AND MINOR LOBES OF ALL EIGHT BEAMS





Another parameter of concern to oscillator designers is the output power versus frequency as shown in Figure 13. By varying the tuning voltage, we can predict the output power for different frequencies of oscillation.

Figure 13. Output power versus frequency

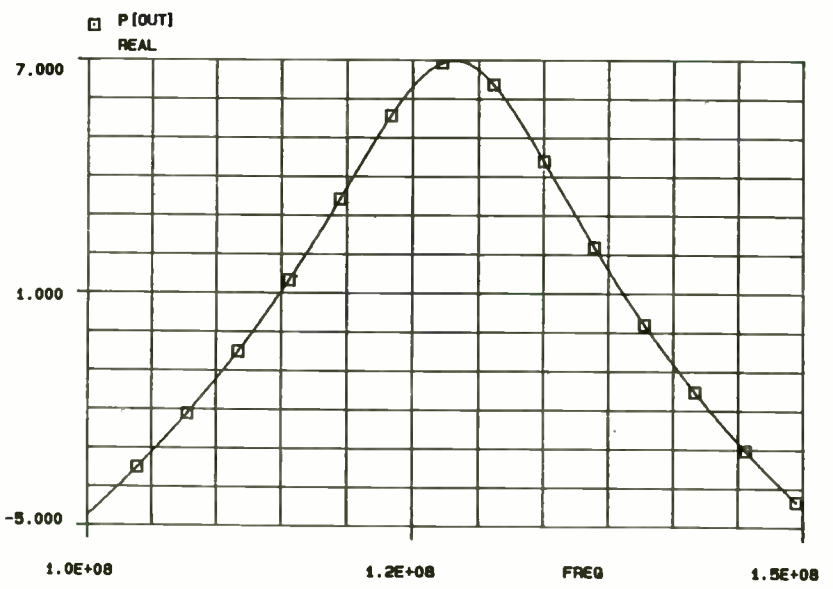


Figure 13. Frequency versus Pout

A response of the collector current versus output power, shown in Figure 14, is useful to evaluate the sensitivity of the oscillator to variations in supply current. Although mwSPICE doesn't really have a "tune" mode, alternately saving S-parameters at different collector currents allow the required data to be graphically evaluated on a single plot.

Figure 14. Oscillator power versus collector current

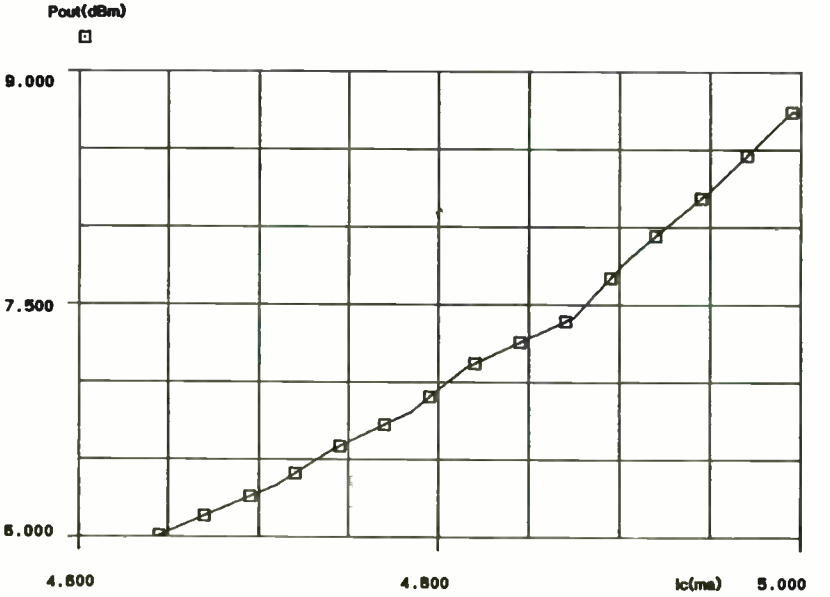


Figure 14. Ic versus Pout

P.C.MOUNTABLE MINIATURE HELICAL FILTER

by

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A B S T R A C T

This paper presents the development of a miniature P C board mountable helical filter in the VHF/UHF range. The specific development was for application in a space-borne S-Band transponder. The unit size is $45 \times 14 \times 14$ mm^3 having a 3 pole Butterworth response, giving an insertion loss of about 1.5 dB with 0.5 dB flatness of about 10 MHz and 50 dB rejection bandwidth of 150 MHz at fo = 375 MHz. This unit is tunable from 250 MHz to 400 MHz and weighs approximately 25 gms.

INTRODUCTION: In the VHF/UHF range helical resonators can be extensively used where high Q and practical size is realisable compared to other conventional types. The helix is enclosed in a highly conductive shield of square cross section. One end of the helix is grounded and the other is left open.

DESIGN CRITERIA: The main aim of this design is to realise a unit miniature in size and yet reliable.

Size reduction has been achieved primarily by the following methods:

a) By optimising the volume of the rectangular cavity and coil size.

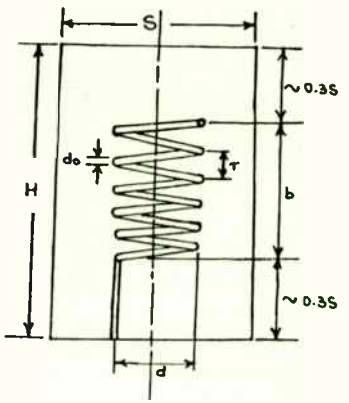
b) Eliminating input/output RF connectors by using P C solderable R F feed-through pins.

c) By using an alignment procedure which can obviate the need of tuning screws.

DESIGN REQUIREMENTS: The following specifications need to be realised.

fo	=	375 MHz
BW_{1dB}	=	17 MHz
BW 50dB	=	150 MHz

Design:- Helical Resonator with square cross section:



Summary

This is a summary of the non-linear analysis techniques that can help the RF design engineer more exactly predict circuit performance, thus reducing design time, costs and frustration.

References

1. Gary Franklin, "Oscillator Design Using the Device Line Method and Load Pull Method:, RFEXPO 86 Proceedings, pp. 251-259.
2. Hewlett-Packard Application Note 994, "A 2GHz Power Oscillator Using the HXTR-4103 Bipolar Transistor".
3. EEsof
4. Compact Software

H = Height of the cavity in inches

S = Length of one side of the square

d = The mean diameter of coil in inches

b = Height of coil in inches

do= diameter of wire in inches

T = Pitch of the winding in inches.

The following set of equations are given with these notations for a square cross section (1)

Table - 1

1) $Qun = 60s\sqrt{fo}$

2) $N = \frac{1600}{S.fo}$ the number of turns

3) $n = \frac{1}{T} = \frac{1600}{s^2 fo}$ the number of turns per inch

4) $d = 0.66S$ for $\frac{d}{1.2S} = 0.55$

5) $b = S$ for $\frac{b}{d} = 1.5$

6) $H = 1.6S$

It is found that a 3-pole Butterworth filter will satisfy the requirements.

Next $Qmin = qmin \frac{fo}{BW\ 3dB} = 37.5$

In order to have high Q, the $Qun > 10\ Qmin$

$\therefore$ Qun should be at least 375

By using the set of equations in Table 1 and taking into consideration the fabrication difficulties involved, and also keeping in view miniaturisation without deviating much from the electrical specification requirements, the following dimensions are arrived at for practical purposes.

H = 11.7 mm / S = 14 mm / d = 8.5 mm / b = 6 mm/

N = 6.5 turns approx. / n = 32 TPI / T = 0.8mm/

do = 0.3mm approx.

The insertion loss is calculated by $I.L. = 20 \log \frac{U}{U-1}$

Where $U = \frac{Qunloaded}{Qminimum}$

In this case, Qun = 375 at least.

$Qmin = \frac{37.5}{}$ $\therefore$ $I.L. = 20 \log \frac{10}{10-1} = 1$ dB approx.

The input and output of the resonator are through loops of less than a turn of 22 SWG wire and are placed perpendicular to the helix on the last turn such that loose coupling is maintained.

CONSTRUCTION:- The formers are made of Teflon in which square threads are cut to accomodate the helix coil of 30 SWG enameled copper wire. One end of the coil is grounded and the other is left open. The loops are made from 22 SWG wire. The helix and loops are bonded with

Epotek H-54 low loss dielectric compound. The entire cavity is soldered along the sides to the base plate after tuning is completed. Then, the entire unit is conformally coated to prevent any seepage of alcohol during further P.C. card assembly operations, cleaning, etc. The mechanical configuration is shown in Fig.1.

ALIGNMENT PROCEDURE:

The filter is aligned using return loss phase characteristics.

Initially all resonators are short circuited, including the output port. Initial phase reference is noted. Each resonator is tuned sequentially by closely changing the number of turns to achieve resonance of each resonator.

RESULTS:- The filter response showing the transmission and return loss characteristics, is shown in Fig.2 & Fig.3. Measured insertion loss is about 1.5 dB, weight 22 gms, size 45x14x14 mm^3.

CONCLUSIONS:

1) The same configuration holds good for different frequencies in the range 250 MHz to 400 MHz, and with a slight increase in cavity and resonator height it can be made even up to 150 MHz.

2) This filter has passed rigorous tests according to MIL-STD-202F.

3) This has been used in an S-Band TTC Transponder aboard Indian remote sensing satellites, etc.

ACKNOWLEDGEMENT:

We sincerely acknowledge the encouragement provided by COL. N. PANT, DIRECTOR, ISRO SATELLITE CENTRE, BANGALORE, for this work. Also sincere thanks are due to Mr. U. PRABHAKARAN and to Mr. R. RAMASUBRAMANYAM for useful comments.

REFERENCES:-

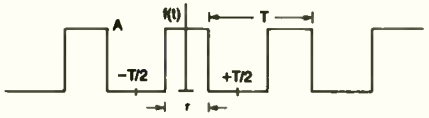
1. Handbook of filter synthesis: Anatol I. Zverov. CHAPTER 9 P.NO. 499
2. Microwave Filters, Impedance matching Networks, and coupling structures. SEC 11-05 by GEORGE. L. MATTHAEI. et. al.

A CRYSTAL CONTROLLED FREQUENCY AND AMPLITUDE CALIBRATOR

by
Dan Baker
Tektronix, Inc.

The motivation for creating this circuit was to provide a calibrator for both amplitude and frequency over a reasonable range of the HF band. Most modern receivers use frequency synthesis and would receive little benefit from a frequency calibrator. However, older receivers and spectrum analyzers need frequency calibration and virtually all receivers would benefit from a broad-band amplitude reference. This circuit accomplishes these goals with a simple design that is fundamentally accurate requiring no adjustments.

The design is based on narrow-width pulses with 1 MHZ and 100 MHz repetition rate. For a theoretical analysis, consider the following time function:



The double-sided Fourier coefficients for this function are:

$$F_n = \frac{1}{T}\int_{-\tau/2}^{\tau/2} f(t)e^{-j\omega_n t}dt = \frac{1}{T}\int_{-\tau/2}^{\tau/2} A e^{-j\omega_n t}dt$$

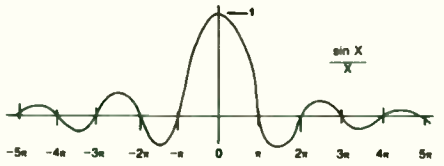
$$F_n = \frac{2A}{\omega_n T}\left[\sin\left(\frac{\omega_n \tau}{2}\right)\right] = \frac{A\tau}{T}\left[\frac{\sin\left(\frac{\omega_n \tau}{2}\right)}{\left(\frac{\omega_n \tau}{2}\right)}\right]$$

This is of the general form:

$$Fn = \frac{A\tau}{T}\left[\frac{\sin(X)}{(X)}\right]$$

where $X = \frac{\omega_n \tau}{2}$

The familiar [sin(x)]/x function is shown below:



The function is zero at integral multiples of π. The first zero occurs at:

$$X = \pi = \pi\, nF_o\tau$$

$$nF_o = \frac{1}{\tau} = \text{first null frequency}$$

A spectrum analyzer or receiver measures the magnitude of $F(\omega)$. The frequency response $|F(\omega)|$ for a rectangular pulse train is a series of impulses in the frequency domain as follows:

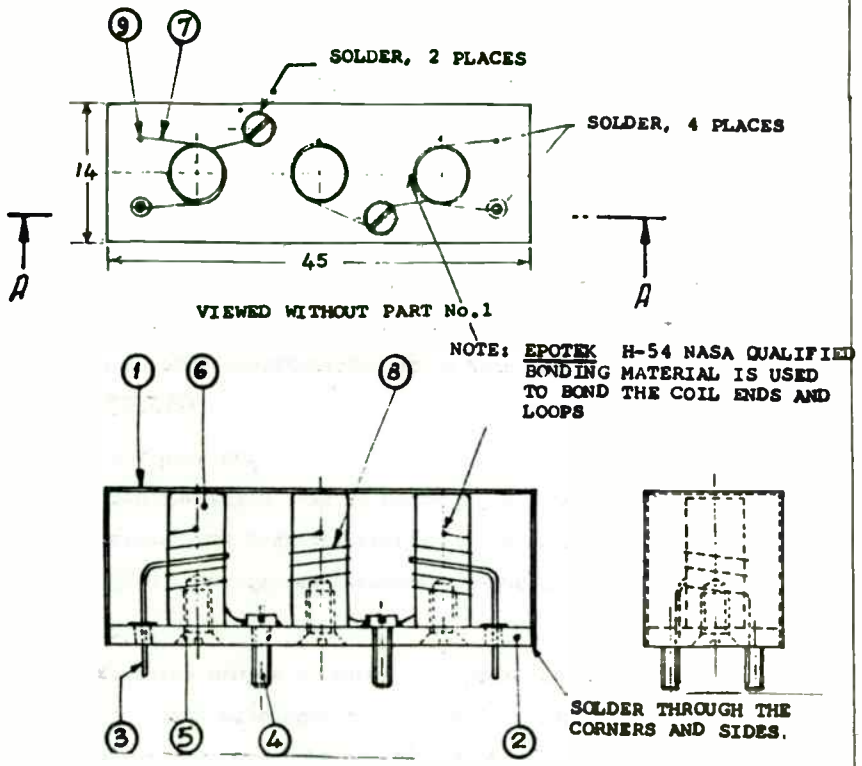
$$|F_{(\omega)}| = \sum_{n=1}^{\infty} \left|2A\tau F_o\left[\frac{\sin X}{X}\right]\right| \delta(\omega - n2\pi F_o)$$

where $X = \pi F_o n\tau$

$F_o = 1/t$ = the pulse repetition rate.

The envelope of the frequency response is dependent only on the pulse shape and not the pulse repetition rate (F_o). If the pulse is rectangular and of short duration, the resulting response may be quite flat over a portion of the frequency band before the first zero.

The circuit shown in Figure 1 generates a pulse of approximately 8 nsec in duration. The pulse duration is loosely controlled by the propagation delay through the inverter and D flip-flop. A more consistent pulse width could be obtained with a 74S04 instead of the 74LS04. However, as will be shown, this is not necessary to meet the design goals.



SECTION AT 'A-A'

Part	Qty	Description	Matl.	Remarks
1	1	CAVITY BODY	COPPER	SILVER PLATED
2	1	BOTTOM PLATE	COPPER	SILVER PLATED
3	2	RF FEED THROUGH (GLASS)		
4	2	M2 x 8 CHEESE HEAD SCREW	BRASS	SILVER PLATED
5	3	M3 x 6 C/SK SCREWS	BRASS	SILVER PLATED
6	3	TEFLON FORMER	TEFLON	
7	-	ENAMELLED COPPER WIRE	COPPER	22 SWG
8	-	ENAMELLED COPPER WIRE	COPPER	30 SWG
9	2	GROUNDING PINS		SILVER PLATED

F I G . 1 MECHANICAL DETAILS

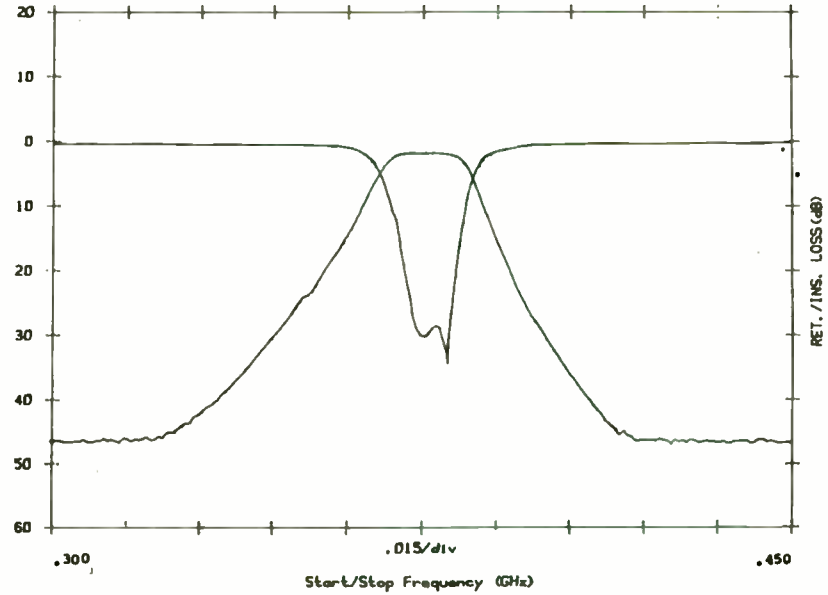
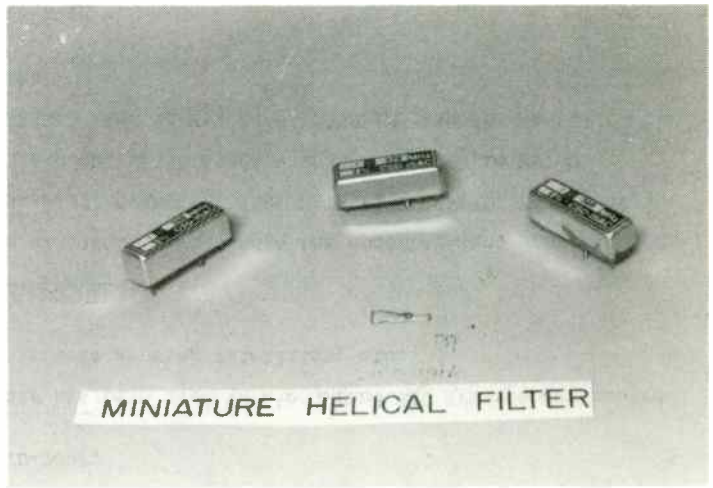


FIG.2 TRANSMISSION/REFLECTION CHARACTERISTICS AT 375 MHz



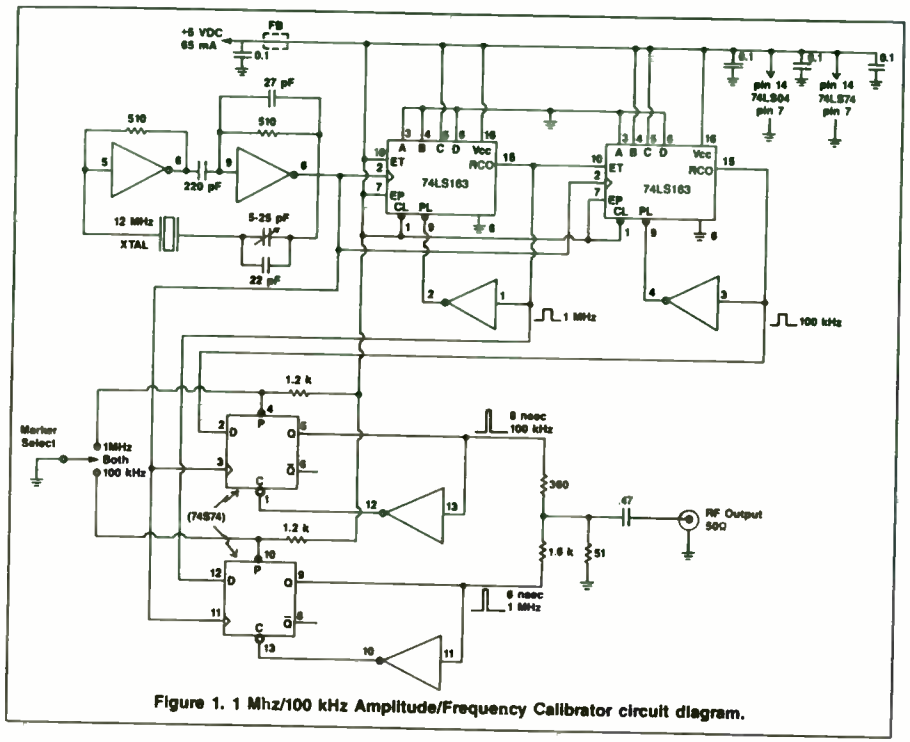


Figure 1. 1 Mhz/100 kHz Amplitude/Frequency Calibrator circuit diagram.

Figure 1. 1 MHz/100 kHz Amplitude/Frequency Calibrator circuit diagram.

An 8 nsec pulse width would provide the following flatness error at 50 MHz.

$$\text{Error} = 20 \log \left[\frac{\sin\left(\frac{50}{125}\pi\right)}{\left(\frac{50}{125}\pi\right)} \right] = -2.4 \text{ dB}$$

This is actually a worst case since 1) the pulse is typically narrower and the first zero greater than 125 MHz, reducing the error at 50 MHz, and 2) the D flop-flop is not capable of generating a very narrow rectangular pulse. The pulse is rounded and, due to slew rate limiting, better approximated by a triangular pulse. This spectrum is flatter than the (sin x)/x frequency response and this effect further reduces the amplitude flatness error at 50 MHz. The measured error of the prototype circuit was < 2dB.

CIRCUIT DESCRIPTION

To provide markers at 1 MHz and 100 kHz, two programmable synchronous counters are used. Crystals at 12 MHz are readily available and most work well in the TTL inverter oscillator shown. The trimmer capacitor is adjusted to calibrate the oscillator to a frequency standard.

The first counter divides by 12 and the second by 10. The two D flip-flops generate the 8 nsec pulses so that 1 MHz and 100 kHz markers can be generated simultaneously or separately. The 12 MHz oscillator synchronously clocks the two D flip-flops as well as the counters. This allows the 100 kHz pulses to occur precisely coincident with every tenth 1 MHz pulse. This is necessary for proper in-phase addition of the two spectra when both 1 MHz and 100 kHz markers are to be generated.

The desired output power for the calibrator is -60dBm for the 100 kHz markers and -50 dBm for the 1 MHz markers (Figure 2.)

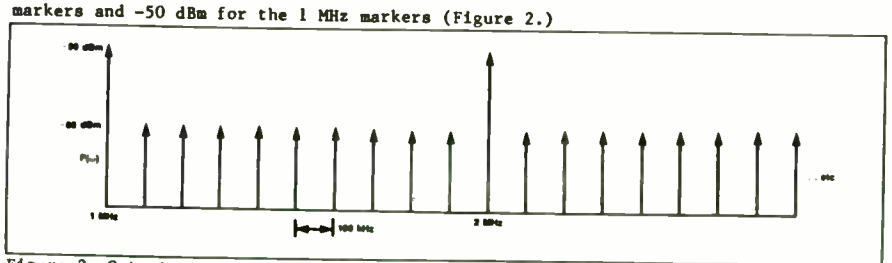


Figure 2. Output spectrum

S-BAND HIGH PERFORMANCE COMBLINE FILTER

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A B S T R A C T

This paper presents the development of an improved high performance combline filter st S-band for input/out applications of a transponder. The unit features reduced size and weight optimised with a minimum number of elements resulting in the following characteristics:

Type : Eight pole Chebyschev 0.1 dB ripple.
Rejection B.W. : $f_o \pm$ 180 MHz - 110 dB
I.L. : 1.0 dB
Ripple B.W. : 100 MHz
Sizes : 183 x 37 x 60mm
Weight : 165 GMS.

The unit is tunable from 2 to 2.4 GHz. The unit is qualified for space borne applications for 1 Watt RF power through low pressure to vaccum.

INTRODUCTION:

A high performance combline filter has been developed at S-band for applications in spacecraft telemetry. The unit features light weight, high rejection on the order of 100 dB and 40 dB down spurious response up to 18 GHz. The unit was tested for 1 Watt RF power from low pressure to vacuum. It was found to be free from RF discharges like corona and multipacting. The unit can be tuned easily to any frequency in the band 2 to 2.4 GHz used for spacecraft telemetry. The filter was constructed from two milled pieces of aluminium joined with screws. This construction makes the unit rugged enough to withstand the severe vibrational requirements of a launch pad. The thermal drift of this unit from 0 to 50°C is less than 5 MHz. A special surface polishing technique was developed to give a bright mirror-like surface finish to the aluminium blocks. This improved the RF conductivity of the surface and brought down the insertion loss to less than 1 dB.

D E S I G N:

The electrical circuit of the combline filter is shown in Fig.1. The circuit consists of coupled transmission lines of electrical length θ shorted at one end and loaded by a lumped capacitor at the other end. These coupled transmission lines are characterised by the self impedance of each resonator, Ci, and mutual capacitance of each resonator with its nearest

This is rather high for most narrowband receivers and the output may need padding for "S" meter calibration. For the 100 kHz spectral components, the required output into 50 ohms is:

$$-60\ \text{dBm} = 20 \log \frac{V_{F_0}}{224\ \text{mV}}$$

$$V_{F_0} = 224\ \mu V_{RMS} = 317\ \mu V\ \text{peak}$$

This requires an attenuator on the output of the TTL flip-flop. The values are then calculated as shown in Figure 3a. It is desired that the 1 MHz markers be 10 dB above the 100 kHz marker amplitudes. The attenuator for the 1 MHz markers is shown in Figure 3b.

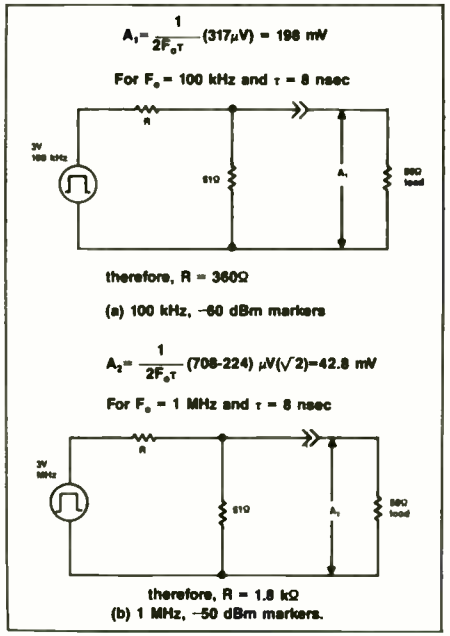


Figure 3. Determination of attenuator resistor values.

Note that when both markers are present, the 1 MHz markers will be 3.3 dB higher than the amplitude when generated alone. This is due to the in-phase addition of the 1 MHz components of both spectra.

PROTOTYPE RESULTS

Figures 4 through 8 illustrate the measured results of the prototype. Figure 4 is the double sided (sin x)/x magnitude response. Note that the first zero is slightly higher than 125 MHz indicating the pulse width is slightly less than 8 nsec.

Figure 5 shows the first 50 MHz of the spectrum and illustrates the predicted flatness error of about 2dB. Note that the 12 MHz component is too high. This is probably due to crosstalk in the hex inverter. A separate XTAL oscillator would probably eliminate this error at the expense of more parts.

Figures 6, 7 and 8 show a 5 MHz segment of the first 30 MHz. Figures 3 and 4 show the 100 kHz and the 1 MHz markers when selected separately. Figure 5 shows the composite calibrator output. Note that the marker amplitudes are about 10dB different, as predicted. Also note that the 1 MHz markers are about 3dB lower (Figure 7) when selected individually, as was also predicted.

One note of caution is in order. Receivers have a limited voltage dynamic range at their inputs. Pulses much larger than the ones used in this design can overload a receiver input. If very fine resolution markers are desired using this technique, it would be prudent to consider a chirp or other more complex technique to obtain a flat spectrum with good signal-to-noise ratio.

This circuit provides a cheap, yet quite accurate calibrator of both amplitude and frequency over the 30 MHz HF band. It can serve as a general purpose reference for a general cover receiver or spectrum analyzer.

neighbours, Cij. The values of Cij were calculated from the prototype given by Mathaie et.al (1). Finally, the physical parameters of the coupled lines were calculated using graphs provided by (2).

The prototype filter along with its element values are given in Fig.2. The value of self impedance and mutual impedance of each resonator is calculated using Mathaie's formule (1). The terminating impedance Ya=50,ohms impedance of each resonator is taken as 75 ohms and electrical length θ = pie/4. This gave the value of self and mutual capacitance as:

Self Capacitances	Mutual Capacitance
C0 = C9 = 6.175	C1 = C89 = 1.358
C1 = C8 = 3.764	C12 =C78 = 0.223
C2 = C7 = 4.710	C23 =C67 = 0.167
C3 = C6 = 4.775	C34 =C56 = 0.158
C4 = C5 = 4.786	C45 = 0.156

Finally, reactangular bars were used to construct the coupled line structure. Ground plane spacing was taken as 15mm. and t/b value was taken as 0.3. The cross section of the structure is given in Fig.3. The value of w/b and s/b were calculated using the data given (2). The lumped capacitance, Cs, was realised using a parallel plate capacitor with air as the dielectric. The physical dimensions of the capacitor were calculated using the formula:

$$C_s = \epsilon A/d$$

where A = Area of the plate

d = Separation between them

MECHANICAL FABRICATION AND SURFACE POLISHING

The filter was fabricated in two pieces. One piece consists of transmission lines coupled with one plate of the capacitance. The other piece is a cover which forms the two ground planes for the coupled lines and a ground plane for the lumped capacitance. Both pieces were milled from blocks of aluminium. They were joined to each other using M-3 screws. The launching pieces which couple the electrical energy into the combline structure were fabricated separately and fixed to the cover plate using M-2 steel screws. The structures were chemically polished. The attached photographs show the internal construction and assembly of the filter.

FILTER ALIGNMENT AND TESTING:

The centre frequency of the filter can be tuned to the desired value by adjusting the resonant frequency of the resonators. Since for a small range of tuning frequency the coupling is indepedent of frequency, the pass band will not get distorted by tuning. Each resonator centre frequency is tuned to the desired value by varying the capacitance, Cs. This is achieved by a tuning screw fixed on the cover plate, one for

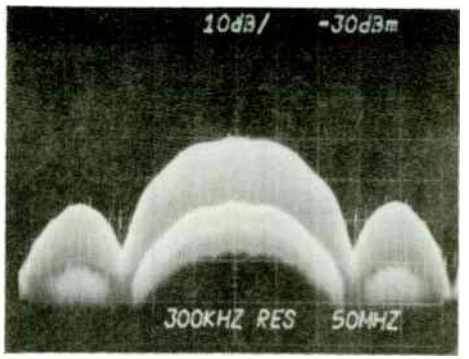


Figure 4. Double-sided (sin x)/x spectrum of the calibrator.

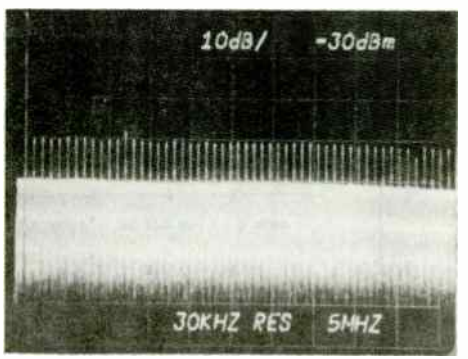


Figure 5. 0-50 MHz markers, showing approximately 2dB flatness error at 50 MHz.

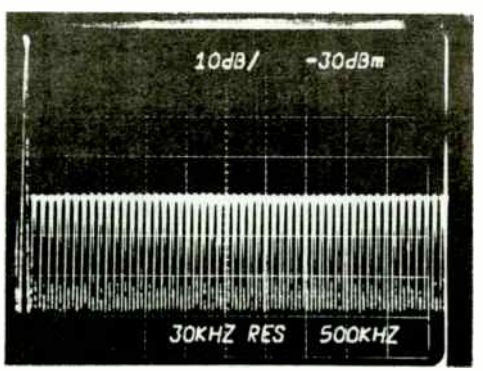


Figure 6. 100 kHz markers, from 0-5 MHz at -60dBm.

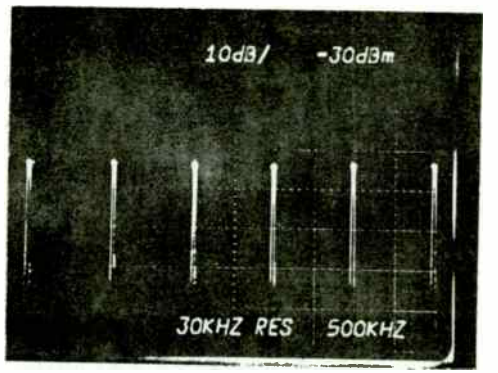


Figure 7. 1 MHz markers, from 1-6 MHz. Note level at about 3dB below -50dBm.

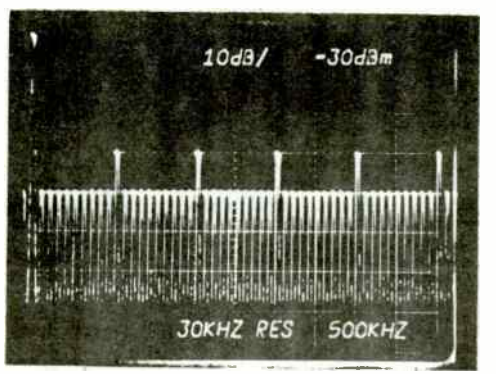


Figure 8. Both markers combined, 0-5 MHz, showing accuracy of amplitude.

for each resonator. The resonators were brought to the desired frequency by monitoring the phase of the input impedance of the filter on a network analyzer. However, minor adjustments on the launcher position give good return loss as the filter is tuned to different frequencies. The responses are shown in Fig.4. Also, the unit was tested up to 2 Watts in vacuum for power handling capability. No increase in insertion loss was observed throughout the vacuum range from atmosphere to hard vacuum.

R E S U L T S:

The insertion loss of the filters was measured on the network analyzer and found to be 0.9 dB. The rejection at ± 180 MHz away from the centre frequency was measured using a high power source and spectrum analyzer. The measured isolation was 110 dB. The return loss at the desired band was 20 dB. The overall size is 168 x 32 x 30 mm and the measured weight is 165 gms. The photo of the filter along with a similar filter provided by M/s.Delta Microwave for a similar application is given. It can be seen that a substantial reduction in overall size and weight has been achieved. The unit is found to be free from RF discharges like corona and multipacting in the vacuum range starting from atmospheric to hard vacuum for all the required operational power levels.

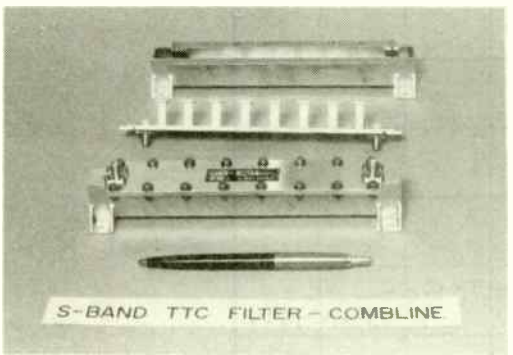
A C K N O W L E D G E M E N T

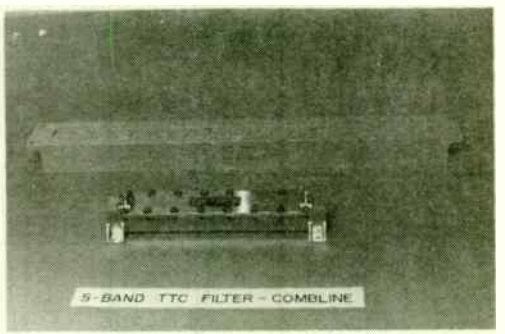
We sincerely acknowledge the encouragement provided by Col, N.Pant, Director, I.S.R.O. Satellite Centre, Bangalore, for this work. Also, sincere thanks are due to Shri.Seetharaman and Ramasubramaniam for useful comments. We are also thankful to Shri.C.Suresh of P.C.B. Lab for his help in chemical polishing of the filter.

R E F E R E N C E S:

1. Microwave filters impedance matching networks and coupling structures by G.L.Mathaei, Leo Yong and E.M.T. Jones.

2. Coupled rectangular bars between parallel plates by W.J.Getsinger, I.R.E. Trans on M T T Jan-1962 p =65-72.





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January 15, 1986

GENERAL PRICE DETERMINANTS for R.F. & Microwave Filters

by Dr. R. A. Wainwright, Chief Scientist
Cir-Q-Tel, Inc. 1/16/86

Abstract: Prudent selection of an r.f. or microwave filter in general requires a great deal of forethought.
Price is usually not an insignificant consideration. Function, however, must necessarily take precedence - it is worthwhile for anyone who must necessarily select system components to give substantial consideration to those devices that shape their system's selectivity as to frequency and/or time domain performance. Given tractable specifications then, one can consider price - it goes without saying that one may over- or under-specify the system's filtering-functional responses - both are expensive in many respects. Rational compromises are usually necessary. The following list of items has been generated as a "General Guide" for systems/subsystems engineers. Please retain this list as a "thought jogger" whenever you find it necessary to consider the use of and/or specify selective devices —— filters for use in systems. It is hoped that by reviewing this list you may be reminded of essentially all of the considerations you must weigh as a responsible engineer as you imagine/conceive/engineer/document and pass off to manufacturing "your design" for use and review by your customers. Like it or not, your name, pride, ego and reputation is inextricably connected to every device you pass on for use by others.
If this list will help you through the maze, then perhaps in some way Cir-Q-Tel will have been of good service to you - we certainly hope so. Please review this list frequently. The factors listed here are very important.

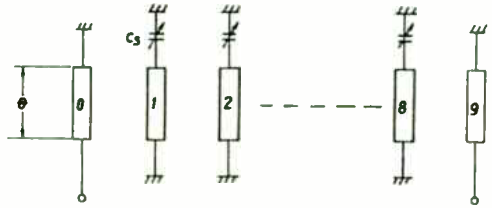
LIST OF GENERAL PRICE DETERMINANTS FOR FILTERS

Not Necessarily in Their Order of Importance
and not Necessarily All

For Lowpass, Highpass, Bandpass and Band Reject Filters

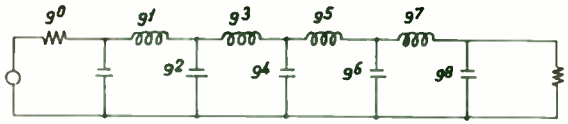
1. Topology, i.e., the general network form for realization as might relate to schematic/type of network, i.e., Lowpass, Highpass, Bandpass, Band Reject, Diplexer, Multiplexer, Reflective or Absorptive Filter, etc.
2. fo or fc and tolerances
3. Bandwidth or % BW and tolerances
4. Complexity or n, sometimes called "degree"
5. Zo
6. Connectors or connections for input and output
7. Temperature, range and stability
8. Vibration and shock environment
9. Relative humidity, salt spray, corrosion protection, mold growth, etc.
10. Altitude or pressure requirements
11. Power: peak and average, cooling provisions: conduction, convection, forced air, etc., e.g. fundamental power, harmonics and power levels of harmonics
12. Load and source impedance conditions
13. Minimum expected life of performance (MTBF)
14. Plating or finishes required
15. Mounting requirements
16. Physical form of network and container shape & size of network: filter
17. If tunable then: range, how tuned, range of tuning, control of parameters over tuning range
18. Quantity
19. Delivery: time and method
20. Warranties
21. Inspections: source, destination, qualification, sampling, etc.
22. Documentation: class, level, detail
23. Time (group delay) and phase requirements - frequency domain
24. Step and impulse requirements - time domain
25. Amplitude-Frequency requirements, including moding: absorptive loss, selectivity
26. VSWR: Return Loss-frequency requirements

(continued)



1 TO 8 ARE RESONATORS
0 AND 9 ARE LAUNCHERS

FIG.1



$g_0 = 1.0000$
$g_1 = 1.1897$, $g_2 = 1.4346$, $g_3 = 2.1199$, $g_4 = 1.6010$, $g_5 = 2.1699$
$g_6 = 1.5640$, $g_7 = 1.9444$, $g_8 = 0.8778$, $g_9 = 1.3554$.

FIG.2

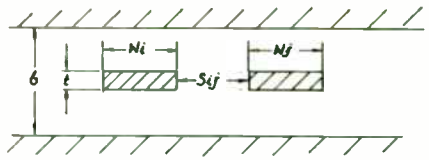


FIG.3.

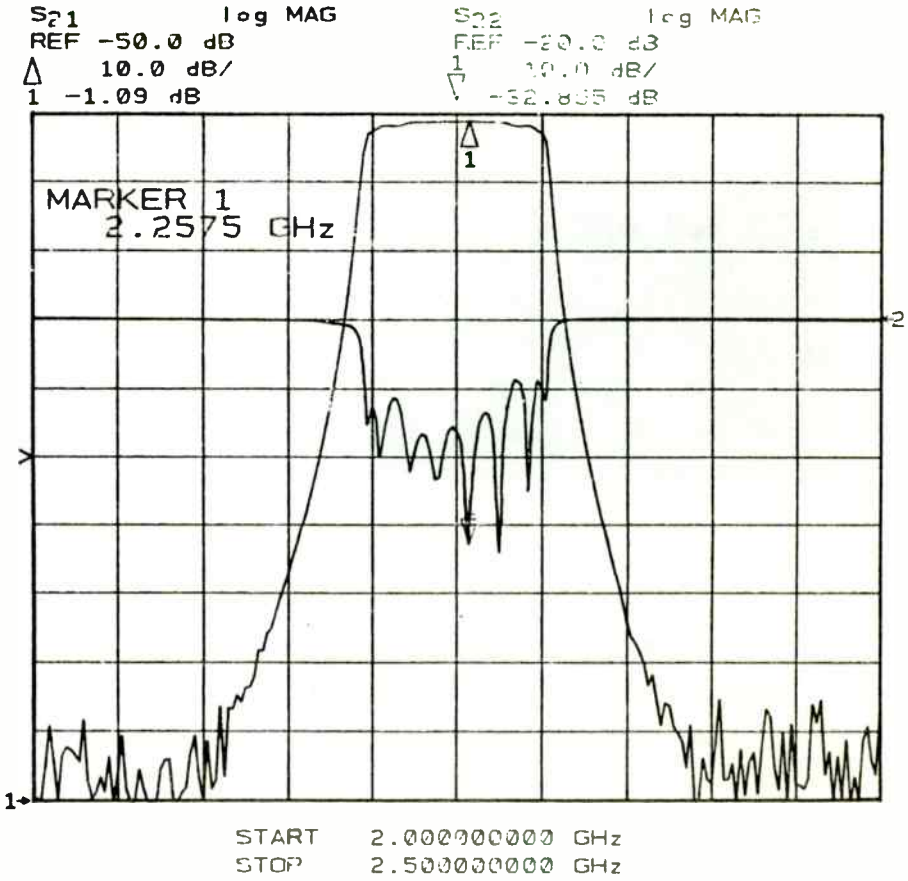


FIG.4 TRANSMISSION/REFLECTION CHARACTERISTIC OF THE FILTER.

Price Determinants (continued)

27. Leakage of r.f. energy requirements
28. Competitive marketplace influences
29. EMP specifications
30. General class of filter: Butterworth, Chebishev, Elliptic, Gaussian, etc.
31. Switching, if switching is to be used: Electromechanical/Electronic/ Mechanical
32. Ultimate rejection,necessary reject band levels and frequency "width"(s) of reject band(s)
33. Functional elements: (a) materials: metals, ceramic, plastics,
    (b) type of resonators, interdigitated, comb line, waveguide, ceramic, (possibly) SAW, etc. or for lowpass and highpass, the physical manifestation of the schematic circuit(s).
    (c) coupling means
    (d) coupling and element tolerances required; generally tolerances required may be estimated from:
    % $\pm$ tolerances: $\pm$ T (L, H): Lowpass Highpass
    $\pm$ T (B, R): Bandpass, Band Reject
    [1] $\pm$ T (L, H) $\sim$ 15/n
    [2] $\pm$ T (B, R) $\sim$ 15/2n
    Where 'n' is the number of elements/resonators: the "degree" of the network - understandably some tuning and tweaking mechanisms/ means may necessarily need to be included in the device design to compensate for unavoidable element/coupling variations.

As an aside: one must be fully aware of other methods of construction: ceramic resonators vs. waveguide resonators for example. In general a well constructed narrow band filter using ceramic resonators may well be superior in performance and lower in cost than a waveguide filter that may be suitable for the same application or a SAW filter (in quantity) may be, and usually is, substantially lower in cost and has superior time domain properties over an equivalent helical resonator filter, etc.

Noise Measurement Instrumentation

by
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INTRODUCTION

The National Science Foundation funds Cornell University to support the National Astronomy and Ionosphere Center (N.A.I.C.). The major facility of the center is the world's largest single dish, radio telescope located near Arecibo, Puerto Rico (Figure 1). Receiver and antenna systems for that installation are developed at a research and development lab located at Research Park, Ithaca, New York.

Most of the front ends for the receiver systems used at the observatory are cryogenically cooled GaAsFET amplifiers. Some masers are in use at "S" band. The expection is that the next generation receivers will be cryogenically cooled amplifiers using modulation doped GaAsFETs (MODFETS). These are referred to also as high electon mobility transistors (HEMTS). They are in the development stage. Commercial units have been promised for early or mid 1986.(1) The forecast is that receiver system noise temperature will approach or equal the performance of masers at very much reduced cost and complexity. A receiver equivalent flange temperature of 4°K at "S" band is a design goal.

Even with present GaAsFET front ends receiver performances achieve 10°K at "L" band, 15°K at "S" band, and 22°K at "C" band when cooled to ~ 16°K with a closed cycle helium refrigerator.

Efforts have been made to test such low noise devices using commercially available noise measurement test equipment. A typical system is the H.P. 8970A.(2) The manufacturer quotes a noise figure instrumentation uncertainty of ± 0.1 dB. This is a noise temperature uncertainty of 14°K. Obviously, better resolution is required to measure receivers whose noise contribution may be very much less than the instrumentation uncertainty. It was decided to develop our own computer-aided automatic noise measurement test facility. It is described herewith.

FUNCTION

An instrumentation system for the development of low noise receivers should provide for the measurement and plotting of receiver noise temperature vs. frequency. It is useful to measure and plot receiver gain vs. frequency, also. In order to optimize receiver performance these measurements need to be made for various bias and tuning conditions. Speed and accuracy are important factors.

A New Double-Balanced Mixer of High Dynamic Range Improves System Performance

by
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ABSTRACT: A new mixer technology which offers low distortions for both inputs enables system designers to significantly improve wideband system performance.

A new mixer technology (patent applied for) has been developed by Bertronics in which each input port has low distortion that is largely independent of the other port signal. This property offers the system designer significant possibilities for improving performance of high performance designs.

To utilize these advantages, this new mixer requires different operating conditions from conventional diode mixers. In order to illustrate how these conditions can be met and how this mixer can be used to advantage, we will illustrate its use in receiving and signal analysis applications.

THEORY

Figure A shows a schematic for a bridge attenuator. If R2*R1=Z*Z, then both ports are matched to Z and the attenuation is

$$V2/V1=(R1-R2)/(R1+R2+2*Z)=(R1-Z)/(R1+Z).$$

A perfect mixer would have V2/V1 proportional to another input voltage. However, synthesizing R1 and R2 to meet the above conditions would be difficult.

Figure B shows a solution to this problem. If port 2 is terminated in 0 ohms and R1||R2=Z/2, then port 1 is matched to Z and the attenuation is

$$I2/V1=(1/R1-1/R2)/2$$

$$I2/I1=(Z/R1-Z/R2)/2.$$

If V2 is a voltage source and port 1 is terminated in Z, then

$$V2/V1=(Z/R1-Z/R2)/4.$$

It is not difficult to make the conductance of circuit elements vary in proportion to a voltage. Hence, a mixer with linearity in both inputs can be constructed.

Since the minimum R1 and R2 is Z/2, the minimum losses are I2/V1=1/Z, I2/I1=1, and V2/V1=1/2. There are hidden sources of loss in linear mixers. In addition to the 3dB image loss, there is an additional 3dB loss due to the fact that the local

BASIC SYSTEM

A major part of such a system is a receiver back end (B.E.). A block diagram of a typical B.E. is shown in Figure 2. A hot and cold load standard are also required. Typically, a cold load (T_c) consists of a 50 ohm termination bathed in LN_2 which is contained in a vacuum dewar. A standard hot load (T_H) usually is a 50 ohm termination located in an oven at 100°c. Hence T_c = 77.3°K and T_H = 373.2°K. Manufacturers provide a plot of the deviation from 77.3°K and 373.2°K (T_c and T_H) vs. frequency for their particular hot/cold standard. This information defines the effect of transmission line losses in order to determine the real T_c and T_H.[3]

I. A procedure for measuring noise temperature for a given frequency is as follows (use block diagram of Figure 2 for the receiver back end):

1. Connect the Device Under Test (DUT) to the input of a Receiver B.E.
2. Set L.O. to frequency of interest.
3. Connect the input of the DUT to T_c and read V_{out_1} (First set variable IF attenuator so that V_{out_1} is within reasonable dynamic range of receiver back end).
4. Connect the input of the DUT to T_H and read V_{out_2}.
5. Calculate y factor = $\frac{V_{out_2}}{V_{out_1}}$
6. Calculate system temperature: $T_{SYS} = \frac{T_H - yT_c}{y - 1}$
7. Calculate $T_{DUT} = \frac{T_{SYS} - T_{BE}}{G_{DUT}}$

a.) T_{BE} for each frequency of interest must first be obtained by the same steps outlined in 2 through 6 above except that (in Steps 3 & 4) connections to T_c and T_H are made directly to the post RF amplifier instead of to the DUT. In Step 6 substitute T_{BE} for T_{SYS}.

b.) The gain of the DUT (G_{DUT}) is obtained as follows:

(1) Connect the Receiver B.E. to a reference load.

(2) Read Vout.

(3) Insert the DUT between the receiver B.E. and the reference load.

(4) Add attenuation until Vout = the same as previous reading for Vout.

(5) The added attenuation = G_{DUT}.

These steps, (1) through (5), must be made for each frequency of interest.

II. Some problems associated with the procedures defined above are:

1. The connecting and disconnecting of the Device Under Test is an exacting business. Errors result from imperfect connections.
2. The time to conduct all of the steps for all of the frequencies of interest is prohibitive.
3. Receiver drift over such a long period can cause errors in the results.
4. Standard hot/cold load values (T_c = 77.3°K and T_H = 373.2°K) are too high for obtaining accurate noise measurements of a very low noise receiver whose noise contribution may be $\leq$ 20° K.

oscillator input would be driven with a sine wave and the RMS value is .707 of the peak value. Notice that there are no intrinsic limitations on the conversion loss from the port controlling the conductance of the circuit elements.

THE MIXER

Figure C shows the connection diagram and preliminary specifications for the Bertronics FD50 Mixer. The bias terminals should be biased at about -20 volts (relative to the port 3 pins) to provide an impedance for ports 2 and 3 of 50 ohms. Adjustment of the bias voltages adjusts the port impedance; the greater the voltage, the lower the port impedance. Adjustment of the voltage between the bias terminals (less than 50 millivolts) provides a fine adjustment of Port 2 to Port 3 isolation. The substrate should be connected to approximately +10 volts. Both the substrate and the bias pins are high impedance inputs, and should not be subjected to static charges.

Port 1 of the FD50 mixer is an input with approximately 5 pF of input capacitance and several hundred ohms of parallel input resistance. Port 2 is an isolated winding with an impedance of 50 ohms (as adjusted by the bias voltage). Port 3 should be balanced with respect to the bias and substrate pins. It has an impedance of 50 ohms.

Ports 2 and 3 are similar in that if one is deliberately mismatched to a low impedance, then the other is resistive (VSWR < 1.5). Port 3 has response down to DC but port 2 does not. If the mismatched port impedance is not relatively low, then the conversion loss and noise performance suffer and VSWR is sensitive to port 1 signal level.

One input's distortion products are largely independent of the other input. Hence, the mixer can be modeled as two nonlinear functions of the inputs followed by a perfect multiplier (Figure D). That is why there are two sets of distortion specifications. Port 1 presents a problem for input intercept specification because this input is mostly capacitive. Therefore, we have expressed this number in volts.

Instead of conversion loss we specify a transmission constant and equation relating input and output voltages and mixer impedance. This equation demonstrates the programmability of the mixer. The conversion loss between two ports is proportional to the signal level of the third. Conversion loss is not a meaningful specification, however, as only one port is terminated resistively in normal operation.

One technique to minimize the time for measuring and plotting receiver noise vs. frequency and receiver gain vs. frequency is to use a spectrum analyzer as a substitute for a receiver back end. The spectrum analyzer can drive an X-Y plotter to produce reasonable results. This arrangement does not address problems outlined in II-1 and II-4 above. Also more sophisticated techniques are needed to provide for modifying bias and tuning parameters between tests.

THE COMPUTER-AIDED AUTOMATED SYSTEM

To answer most of the needs for fast and accurate noise and gain measurements, a computer-aided instrumentation system was developed. An Apple II E computer® and an ISAAC 91-A® interface system were procured.[4] Rather than develop our own analog to digital input-output system, we chose to select a commercially available interface. The important thing was to get on line in the shortest possible time and to have a system that requires minimal effort for modification. The ISAAC 91-A by the Cyborg Company seems to be a good choice. It is designed especially for the Apple II E. Another ISAAC unit is compatible with the IBM PC. Its "Labsoft"® software package simplifies communications with the computer. Specifications are given in the appendix. A block diagram of the control and data acquisition system is shown in Figure 3. Figures 4 and 5 are flow charts of the "Tsys" program and the "noise temp" program respectively.

A test dewar/refrigerator was assembled to provide rapid cool down and warm up times and for rapid installation of various amplifiers at the 16°K station of the dewar (see Figures 6 and 7). A receiver back end was developed which includes a switchable range low pass filter, amplifiers, adjustable attenuators and a voltage to frequency converter (V/F) output (see Figures 8 through 11). The V/F output is fed to a counter input channel of the ISAAC interface. The advantage of this technique is that it allows for rapid dumping of sampled signal levels between frequency settings. Also the V/F technique effectively averages voltage fluctuations over a specified length of sample time.

The hot load reference is provided by driving an H.P. 346B[5] noise diode through a directional coupler (-20 dB). When the diode is on, this results in a nominal noise temp. of ~ 100°K. The cold load consists of a 50 ohm termination located at the 16°K station of a test dewar, hence the cold temperature is ~ 16°K. However, transmission line losses, directional coupler insertion loss and ~ 3°K from hot load port of the coupler (when noise diode is off) result in a total T_c of ~ 30°K. Likewise actual T_H = ~ 100°

INTERFACING

Although these port impedances may seem difficult to work with at first, they can actually be used to advantage in some designs. For lower frequency applications, Port 1's high input impedance allows high signal voltage levels to be reached with little input power. For higher frequency applications, it is desirable to resonate this capacitance in order to reduce the signal power requirements.

Both ports 2 and 3 present 50 ohms and, although one of them is deliberately mismatched, the amplifiers should be designed for good noise performance at 50 ohms. Figure E shows an example of a broadband design. This circuit will have optimum noise performance if biased at the same current as one optimized for common emitter noise performance. FETs can also be used.

SIGNAL RECEPTION / ANALYSIS

Port 1 of the mixer can be used to advantage in receiver applications. For lower frequency RF inputs, the signal can be transformed up, enabling the mixer to have conversion gain (Figure F). This can eliminate the need for RF amplification and enable the system to have a low overall noise figure. The disadvantage of this configuration is that substantial LO power is required.

In heterodyne applications, the low levels of harmonics for both inputs to the mixer reduce the spurious responses of the receiver. If the IF is high, it can be matched to the amplifier with a quarter wave length transmission line (Figure G). The parallel inductor and capacitor are used to short the port at all other frequencies.

Use in direct conversion is where the mixer offers the greatest improvement over conventional mixers. The low level of harmonics of both ports (if the LO has low harmonic content) means that harmonic mixing is greatly reduced. Low level amplification at 50 ohms at baseband can present problems also. Figure H shows a practical circuit for low noise, low impedance amplification. The circuit uses very low noise transistors (PMI MAT-02) in a feedback circuit to lower the input impedance to .04 ohms. Compensation is provided by the shunt input capacitor. This compensation also lowers the input impedance at higher frequencies. Op amps could be used with a penalty in noise performance (Figure I). Here again, compensation is provided by the shunt input capacitor. This pole should be located much lower than any poles in the Op amp transfer function in order to ensure stability.

K (when diode is on) plus (T_c - ~ 3°K) ~ 127°K. These values must be calculated or measured in advance for each frequency of interest and placed in memory by the computer program.

After initialization is made the computer steps are:

1. Read the ambient temperature = (T_A)
   Read 16°K station temp. in dewar = (T_D)

   These readings are taken from voltage vs. temp. of a nonlinear diode (computer uses look up table from manufacturer's data).[6]

2. Read $T_{transmission\ line\ losses}$ + $T_{noise\ diode}$ (off) from a look up table. Add to T_D. This equals T_c for each freq. of interest.

3. Read (from look up table) $T_{noise\ diode}$ (on) and add T_c from above reading. Subtract $T_{noise\ diode}$ (off). This = T_N for each freq. of interest.

4. Read output of V/F = V_1 (first adjust "IF" attenuator for a reasonable dynamic range region of receiver B.E.).

5. Turn on noise diode (TTL noise diode drive = 1).

6. Read output of V/F = V_2.

7. Calculate y factor = $\frac{V_2}{V_1}$

8. Calculate $T_{Rec} = \frac{T_N - yT_c}{y - 1}$ for this particular freq.

9. Increment YIG oscillator (= L.O.) from predetermined steps.

10. Repeat Steps 2 through 9 for 50 frequencies in 20 MHz increments.

11. Calculate T_{DUT} for each freq. = $\frac{T_{Rec} - T_{BE}}{G_{DUT}}$

V. T_{BE} and G_{DUT} must be obtained in advance for these steps and included as information during the initialization process.

   1. T_{BE} is obtained in the same way as in Steps IV - 2 through 10 except that the DUT is bypassed and the results in Step IV - 8 = T_{BE} instead of T_{Rec}.

   2. The gain of DUT (G_{DUT}) is obtained as follows:

      a.) Connect receiver B.E. to a reference load and record in memory V_{out1} vs. frequency.

      b.) Connect DUT between B.E. and same reference load.

      c.) Add fixed attenuator to bring V^2 det. output to within a reasonable region of the dynamic range of the B.E.

      d.) Record V_{out2} vs. frequency.

      e.) Calculate G_{DUT} = added attenuation + 10 log $\frac{V_2}{V_1}$ for each freq. of interest.

VI. For DUT optimization:

   1. a.) Program computer to change I_D.

      b.) Run test data IV - 2 through 10.

      c.) Compare with previous run.

      d.) Repeat for optimum performance.

   2. a.) Program computer to change V_D.

      b.) Repeat Steps VI - 1-b through 1-d.

   3. During Runs 1 and 2 compare G_{DUT} vs. freq. as well as noise temps. vs. freq.

   4. Compromise minimum noise temp. and optimum flatness and gain of DUT.

   5. If provisions are made for external tuning of DUT,

The independence of the distortion functions of the inputs can be used to advantage in a unique AGC circuit. In a conventional diode DBM, reduction of the LO level results in drastic reduction of the third order input intercept point. This degradation in performance does not occur with the new mixer. Hence, we can reduce the gain of the mixer without affecting impedances or other parameters. Figure J shows a system with a PIN diode attenuator interposed between the local oscillator and the mixer input. If the attenuator were on the RF or IF side, noise and distortion performance would suffer. The performance of the circuit in Figure J is limited by the mixer and the IF amplifier. The amplifier can be designed for fixed gain, for instance using feedback. This allows higher performance than could be achieved with a voltage controlled amplifier.

PHASE COMPARISON

The low DC offset of the mixer suits it to use as a phase comparator. If used with a sine wave phase reference, the mixer can be used to lock onto low level signals with greatly reduced risk of harmonic locking due to its low distortion. In synthesis applications, the reduced levels of harmonics enables spectral purity to be achieved with less filtering.

CONCLUSION

We have introduced Bertronics' new mixer technology. The dissipative mixer should be considered as a new component in order to exploit its advantages for high performance system design. It offers a degree of linearity to RF and Microwave designs which was previously available only below 1MHz.

repeat Steps 1 through 4 above for each change in tuning until optimum performance is achieved.

VII. A sample plot of an optimized receiver is shown in Figure 12. Gain vs. frequency and noise temp. vs. frequency are plotted. This receiver was tested while operating at room temperature.[7]

Other less sophisticated programs are included. A system temperature measuring technique is for a more rapid measurement. As long as T_{RX} is known and the gain of the device under test is obtained (from e.g., a swept amplitude network analyzer), the T_{OUT} can be calculated readily. In many cases the T_{RX} contribution may be negligible and hence the T_{OUT} approaches the value of T_{SYS}. The hot and cold levels used during the T_{SYS} testing can be those used in the more sophisticated testing or can be a standard 77.3°K cold load and a standard room temperature load with a thermometer.

CONCLUSION

The system allows for relatively rapid testing and plotting of various noise temperatures vs. frequency. It saves countless hours in the optimization of an amplifier.

Figure 13 shows a plot of a typical cryogenically cooled GaAsFET amplifier system temperature vs. frequency. This test can be made in less than five minutes using the computer-aided automatic noise temperature instrumentation system.[8] The conventional method would require a substantial increase in testing and computing time.

The ISAAC 91-A interface system minimizes the time for developing the test facility.

ACKNOWLEDGEMENTS

Acknowledgement is given to Dr. Sander Weinreb of the National Radio Astronomy Observatory. Many of the ideas for this system were borrowed from a similar system used by the NRAO at Charlottesville, VA.[9] A discussion with Dr. Weinreb and his associates led to the development of this test facility. His group provided the low loss input transmission lines.

Mr. Andrew Ingram, graduate student in Electrical Engineering at Cornell University, developed the software to be compatible with the ISAAC interface and the Apple IIE computer. Pierson C. Mosher developed the cryogenic system. Kurt Kabelac and David VanWinkle assisted in wiring and machining. Lynn Baker provided consultation.

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Labsoft is a registered trademark of Cyborg Corporation.

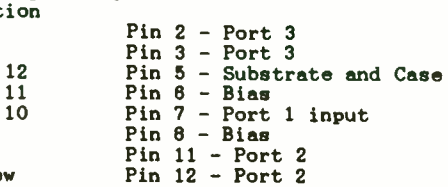
Bertronics **Model MFD50**

Preliminary Preliminary Preliminary Preliminary Preliminary

Double Balanced Mixer

FEATURES

- o Wide Bandwidth
- o High Power Capability
- o Low Distortion



Pin 2 - Port 3
Pin 3 - Port 3
Pin 5 - Substrate and Case
Pin 6 - Bias
Pin 7 - Port 1 input
Pin 8 - Bias
Pin 11 - Port 2
Pin 12 - Port 2

MAXIMUM RATINGS (Voltages relative port 3 common mode voltage)

Bias Terminals	-40	V
Port 1 Voltage	±10	V Peak AC (AC coupled)
Port 2 Voltage	±20	V
Port 2 Current	±100	mA
Port 3 Voltage	±20	V
Port 3 Current	±100	mA
Power Dissipation @ 25OC	2	Watts
Derate Above 25OC	18	mW/OC

OPERATING CHARACTERISTICS (.5-500MHz)

Port 1 Capacitance:	5 pF
Port 2, 3 VSWR @ 50 Ohms (Port 1=0V)	1.5
Isolation, Port 2 to Port 1:	40 dB
Isolation, Port 2 to Port 3:	30 dB
Isolation, Port 1 to Port 3:	40 dB
Transmission Constant T	.8
I3=T*V1*V2/Z3/(VBIAS-2.5V)	
Two-Tone Third Order Input Intercept Point:	
Port 2 or Port 3 @ 30MHz	+39dBm
Port 1 @ 30MHz	25 VRMS
Current, Bias Pins	10 uA
Current, Port 3 Pins to case	10 uA

Specifications apply with Bias pins @ -20V and case @ +10V

Figure C.

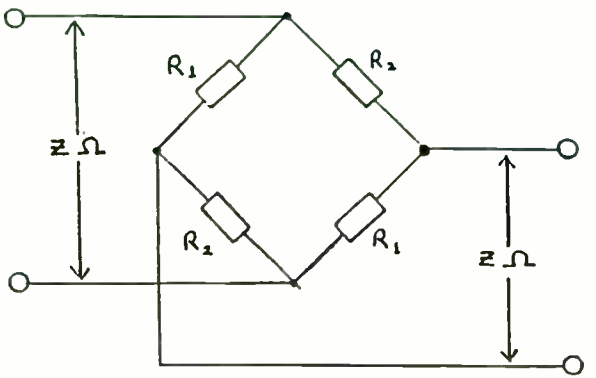


Figure A. Bridge Attenuator

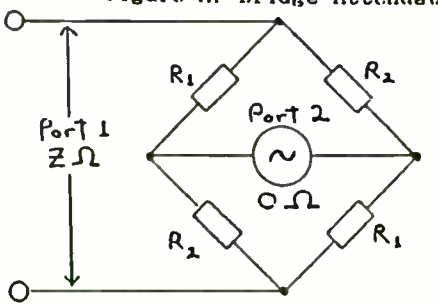


Figure B. Bridge Attenuator with low impedance port

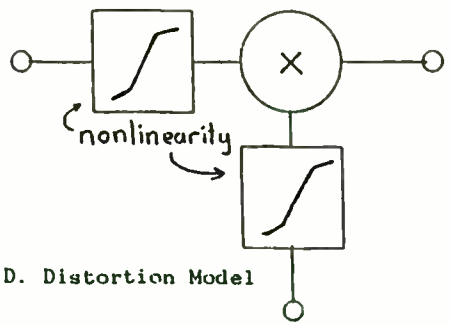


Figure D. Distortion Model

SYMBOL GLOSSARY

Symbol	Explanation
DUT	Device Under Test
G_{DUT}	Gain of Device Under Test
IF	Intermediate Frequency
LN_2	Liquid Nitrogen
L.O.	Local Oscillator
Rec. BE	Receiver Back End
T_A	Ambient Temperature
T_C	Cold Load Temperature
T_D	Dewar Temperature at 16°K Station
T_{DUT}	Noise Contribution of DUT
T_H	Hot Load Temperature
T_{REC}	Noise Contribution of Total System
V/F	Voltage to Frequency Converter
$Vout_1$	Square Law Detected Output when Rec. is connected to T_C
$Vout_2$	Square Law Detected Output when Rec. is connected to T_H
Y Factor	Ratio of $\frac{Vout_2}{Vout_1}$

REFERENCES

1 - Toshiba S 8900 Preliminary Data Sheet

2 - H.P. 8970A Noise Figure Meter Technical Data

3 - Maurey Microwave MT 7118-47 Cryogenic Termination Data Manual

4 - ISAAC 91-A by Cyborg Co., Newton, MA 02158

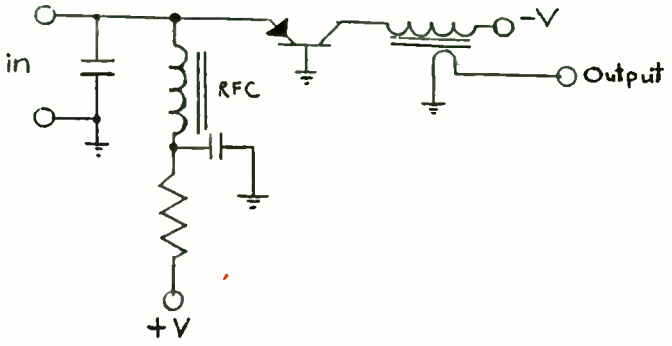
5 - H.P. 346B Noise Source Operating & Service Manual

6 - Lakeshore Cryotronics Inc. DT-500-DRC D Voltage-Temperature Characteristics

7 - NAIC Report: Dual Channel 6cm Cooled GaAsFET Receiver, March 1984, George Peter, et al.

8 - NAIC Report: Computer-aided Noise Measurement Instrumentation Manual 4-84. George Peter, et al.

9 - NRAO Electronics Division. Internal Report #212 - The Adios Analog - Digital Input Output System for Apple Computer - G. Weinreb & S. Weinreb.



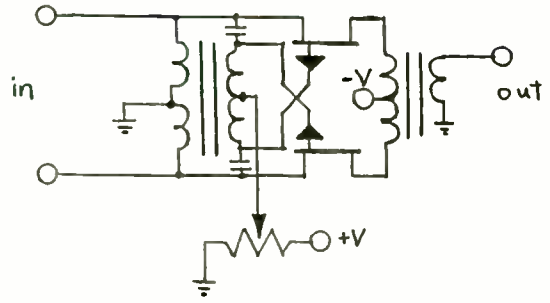


Figure E. Transimpedance Amplifiers

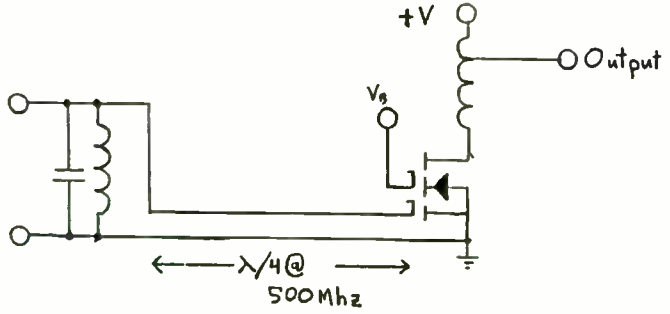


Figure G. Quarter wave matched Amplifier

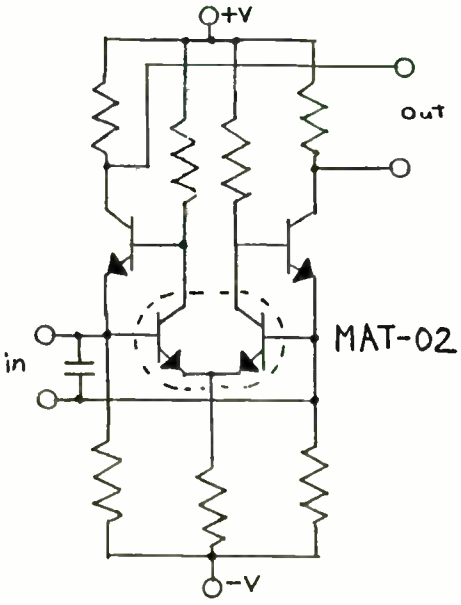


Figure H. Baseband Amplifier

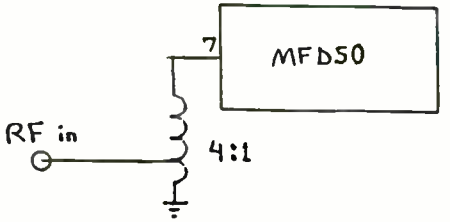


Figure F. Mixer with conversion gain

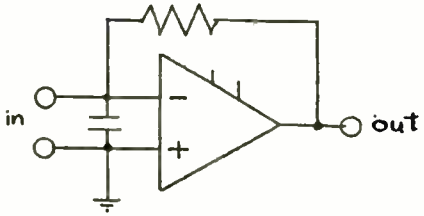


Figure I. Opamp Baseband Amplifier

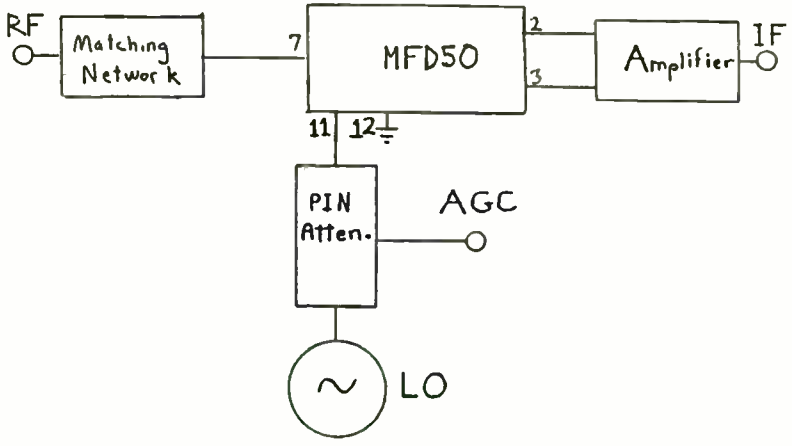
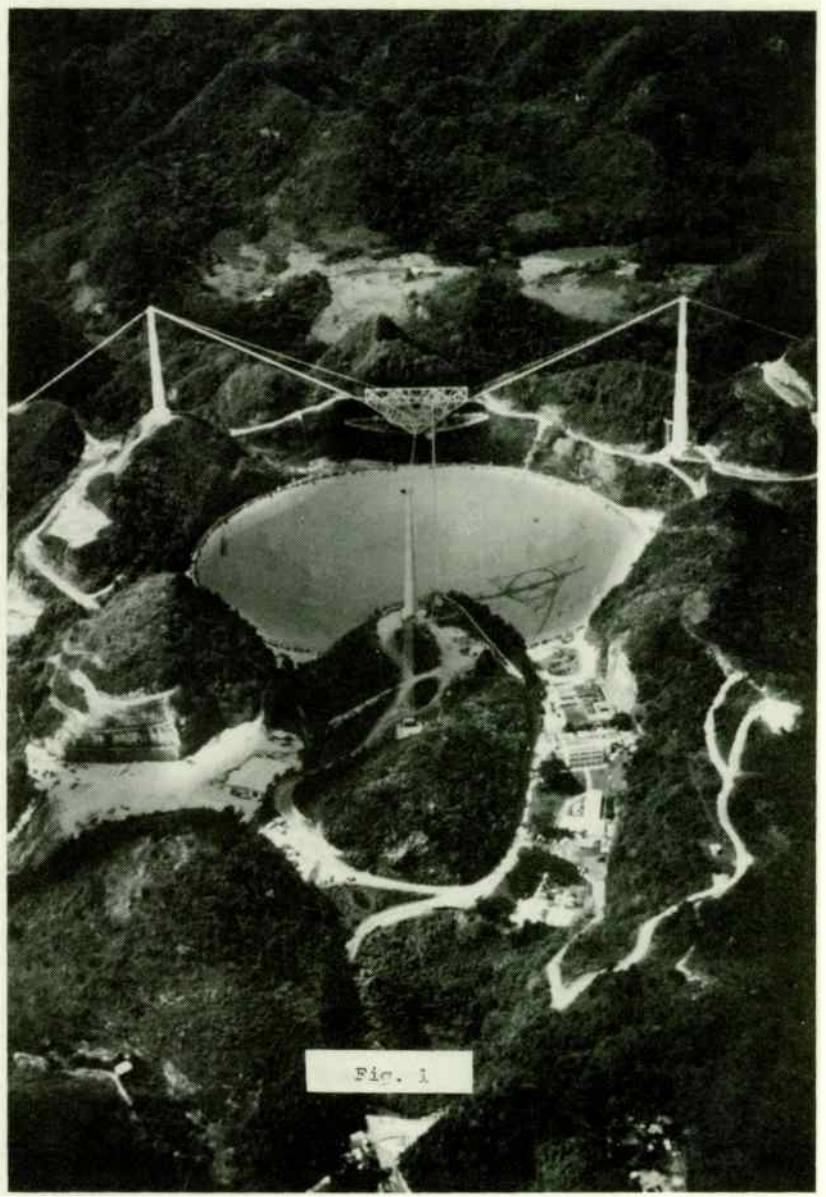


Figure J. Mixer with AGC

FIGURE	DESCRIPTION
1	Picture of Radio Telescope
2	Block Diagram Back End
3	Block Diagram Control & Data Acquisition System
4	Flow Chart Tsys Program
5	Flow Chart Noise Temp. Program
6	Test Dewar - Top View
7	Test Dewar - With Refrigerator Assembly
8	Receiver Rack
9	Receiver, Peripheral Rack, and Test Dewar
10	Receiver with Computer and Interface
11	Directional Coupler, J Line, and Noise Diode
12	Sample Plot Gain & Noise Temp. vs. Freq.
13	Plot of Cooled Receiver Noise Temp. vs. Freq.



THE TACTICAL MINIATURE CRYSTAL OSCILLATOR (TMXO)

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Piezo Technology, Inc.
Orlando, FL

The Tactical Miniature Crystal Oscillator (TMXO), Figure 1, is a high-performance frequency standard intended for use in a wide range of advanced military communications, navigation, and position-determining systems. Key advantages of the TMXO are:

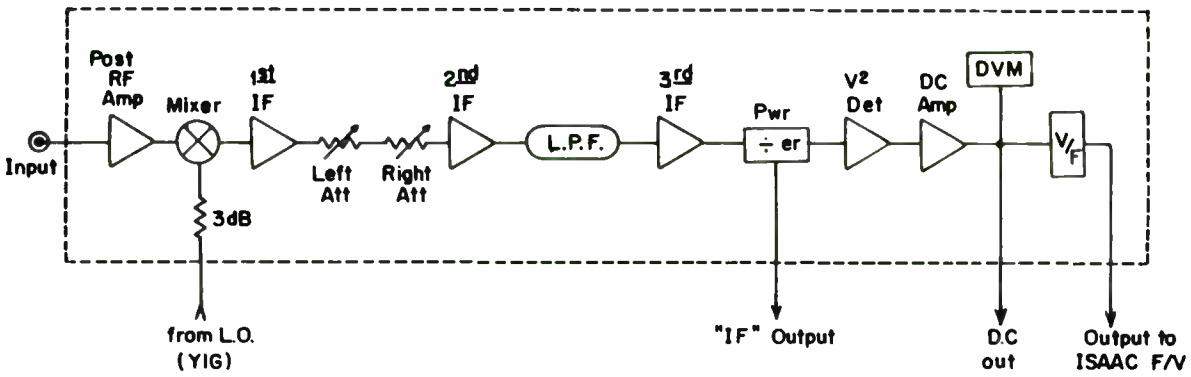
Low Power	-	150 mW typical at 25°C 250 mW max. (-55 to +75°C)
Small Size	-	1.25 in. diameter x 1.55 in. height
Low Weight	-	1.75 oz. max.
Fast Warm-Up	-	4 minutes max. (from -55°C)
Frequency Accuracy	-	$\pm$ 3 x 10^{-8}/yr., all causes

Standard TMXO frequencies are 10 MHz and 10.23 MHz.

While the TMXO is an ovenized crystal oscillator, it uses a radically different mechanical design approach to achieve an order of magnitude reduction in power and size compared to conventional ovenized oscillators. In a conventional oscillator, most of the power required is used by the oven. Reduction in power is achieved by more insulation -- and therefore a bigger oscillator. This is fine for many applications, but it does not fit the tactical military environment.

The TMXO takes a different approach. First, the size of the electronics package is minimized by hybridization. The small size makes it easier to reduce the heat loss. A special ceramic package for the cyrstal resonator gives additional size reduction. Second, a high degree of thermal insulation is provided by an evacuated enclosure. The TMXO is the first production oscillator to use this technique.

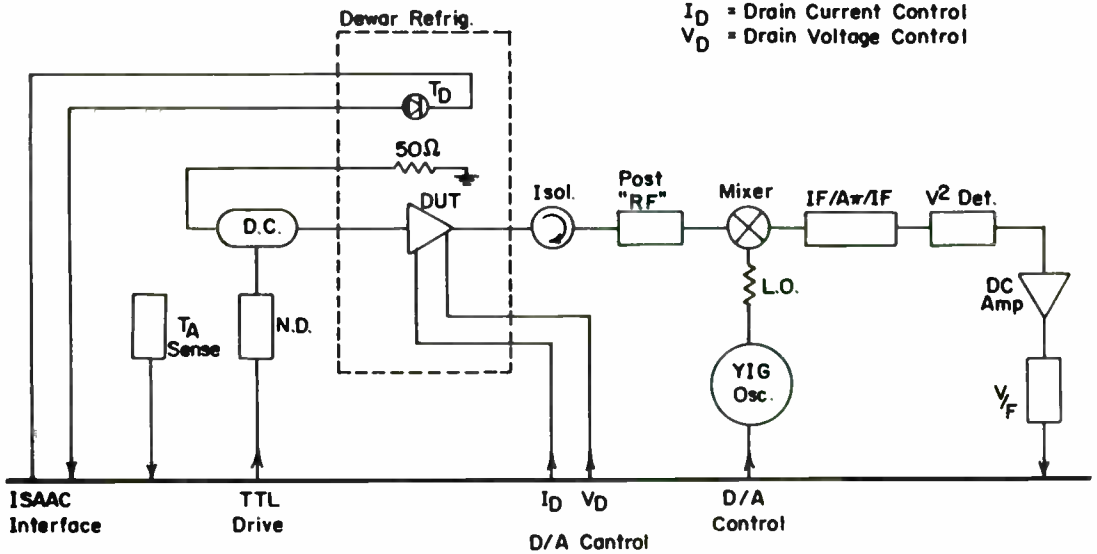
Motivated by projected tactical requirements, the present TMXO was developed at Bendix Communications Division under sponsorship of the U.S. Army Electronic Research and Development Command (now the Laboratory Command) in a series of contracts which began in 1971 [1,2]. Concurrently, its unique ceramic flatpack crystal resonator was under development at General Electric, also under ERADCOM sponsorship [3]. In March, 1985, PTI obtained a commercial license from Bendix for the TMXO, and undertook to manufacture both it and its ceramic-packaged crystal. The first PTI-made TMXO was delivered less than fifteen months later. In this paper, we shall describe the TMXO as currently manufactured; then we shall briefly discuss the Improved TMXO (ITMXO), which is being developed under LABCOM sponsorship.



RECEVER BACKEND BLOCK DIAGRAM.

Fig. 2

D.C. = Directional Coupler (20 dB)
N.D. = Noise Diode (H.P. 346B)
T_A = Ambient Temperature Sensor
T_D = Dewar Temperature Sensor
DUT = Device Under Test
I_D = Drain Current Control
V_D = Drain Voltage Control



CONTROL AND DATA ACQUISITION BLOCK DIAGRAM.

Fig. 3

Applications

The TMXO is unequalled in providing a precise frequency reference requiring only a modest input power. This combination makes it well-suited for certain battery-powered applications -- for example, a portable time transfer unit which can be synchronized from a reference clock (which might get its time reference from a GPS receiver), and which is used to set the clock of a remote system.

In a somewhat different application, the TMXO has been integrated into an existing cockpit environment, where size and weight are extremely important and where, in addition, the TMXO's high stability and fast warm-up are essential to the mission requirement.

In a third application, developed by LABCOM, the TMXO is used in conjunction with a rubidium secondary frequency standard. Its long-term stability is on the order of 1×10^{-11} per month, while the TMXO's is typically 1×10^{-10} per day, but the rubidium's power consumption is 10 to 20 watts. In one version, the rubidium is energized from time to time -- perhaps once a week or once a month. The TMXO is then set to the rubidium frequency, and the rubidium is turned off until the next week or month. This allows even better long-term accuracy than the TMXO on its own provides, without the power penalty of the rubidium. In other versions, the rubidium standard is installed in a separate equipment and is used to re-set a number of TMXO's.

Mechanical and Thermal Design

The mechanical design of the TMXO sets it apart from other ovenized oscillators. Figure 2 shows the most significant aspects of the overall assembly. Except for an optional output buffer, all of the electronics is realized by a thick-film hybrid contained in a hermetically sealed ceramic and metal octagonal package, measuring about 1 inch from flat to flat. An SC-cut quartz crystal resonator in a smaller ceramic flatpack, also octagonal, is vacuum-soldered to the underside of the hybrid, and connected by welded gold ribbons.

This assembly is supported on 6 stiff Inconel wires which extend from the ceramic vacuum header and provide the input/output connections to the hybrid. The output buffer, if used, is located on the bottom, exterior face of this header. Lateral support of the crystal/hybrid assembly is provided by 4 polyimide bumpers which press against the inside wall of the outer enclosure.

The entire assembly is evacuated to eliminate convective heat transfer. Thermal radiation is made negligible by use of a cup-shaped thermal baffle or heat shield which prevents the outer case from "seeing" the hybrid/crystal assembly. As a further measure, the shield, and the inner wall of the outer case are electro-polished and gold-plated for low thermal emissivity. As a consequence of these measures, almost all heat loss is due to conduction along the Inconel wires and the polyimide bumpers. For the former, the thermal resistance is approximately 900 K/W; for the latter, an exact figure is not

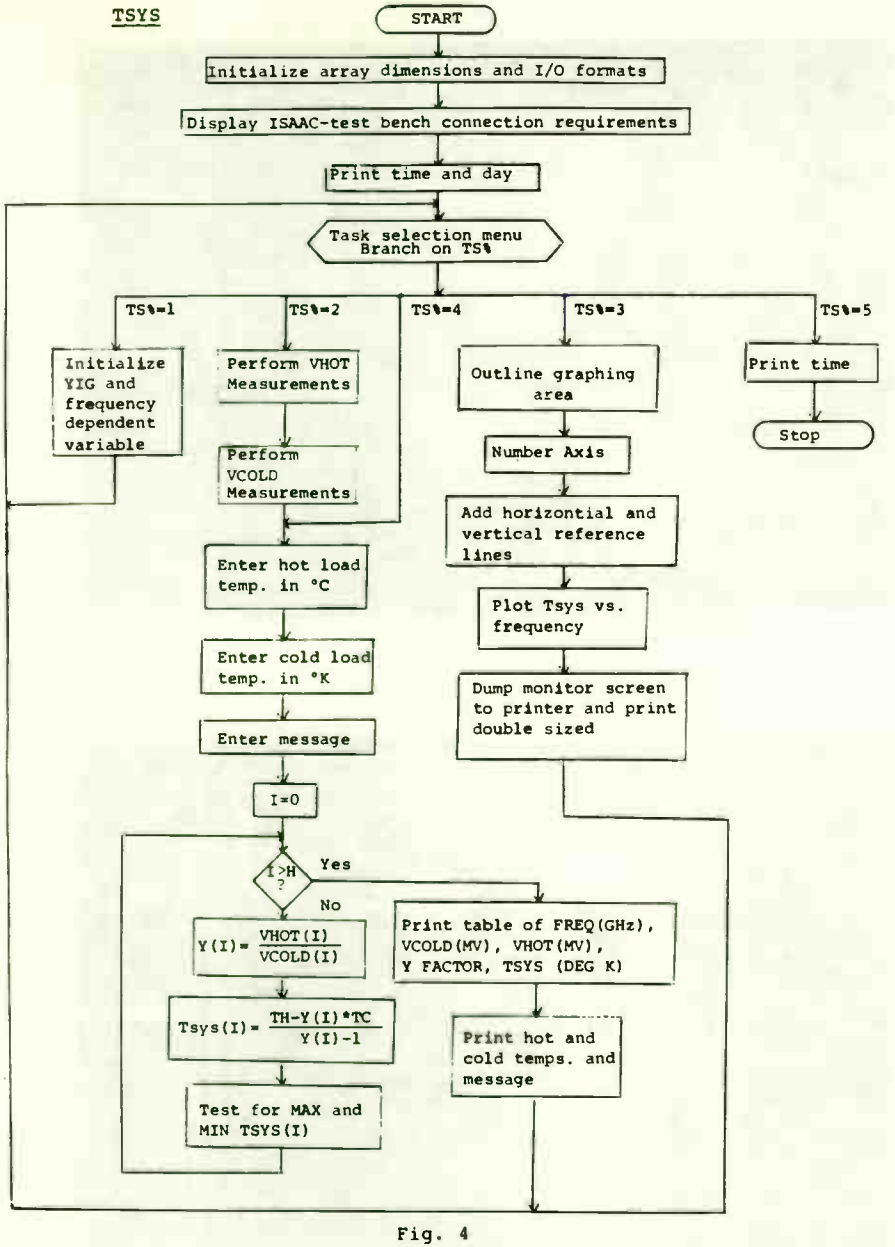


Fig. 4

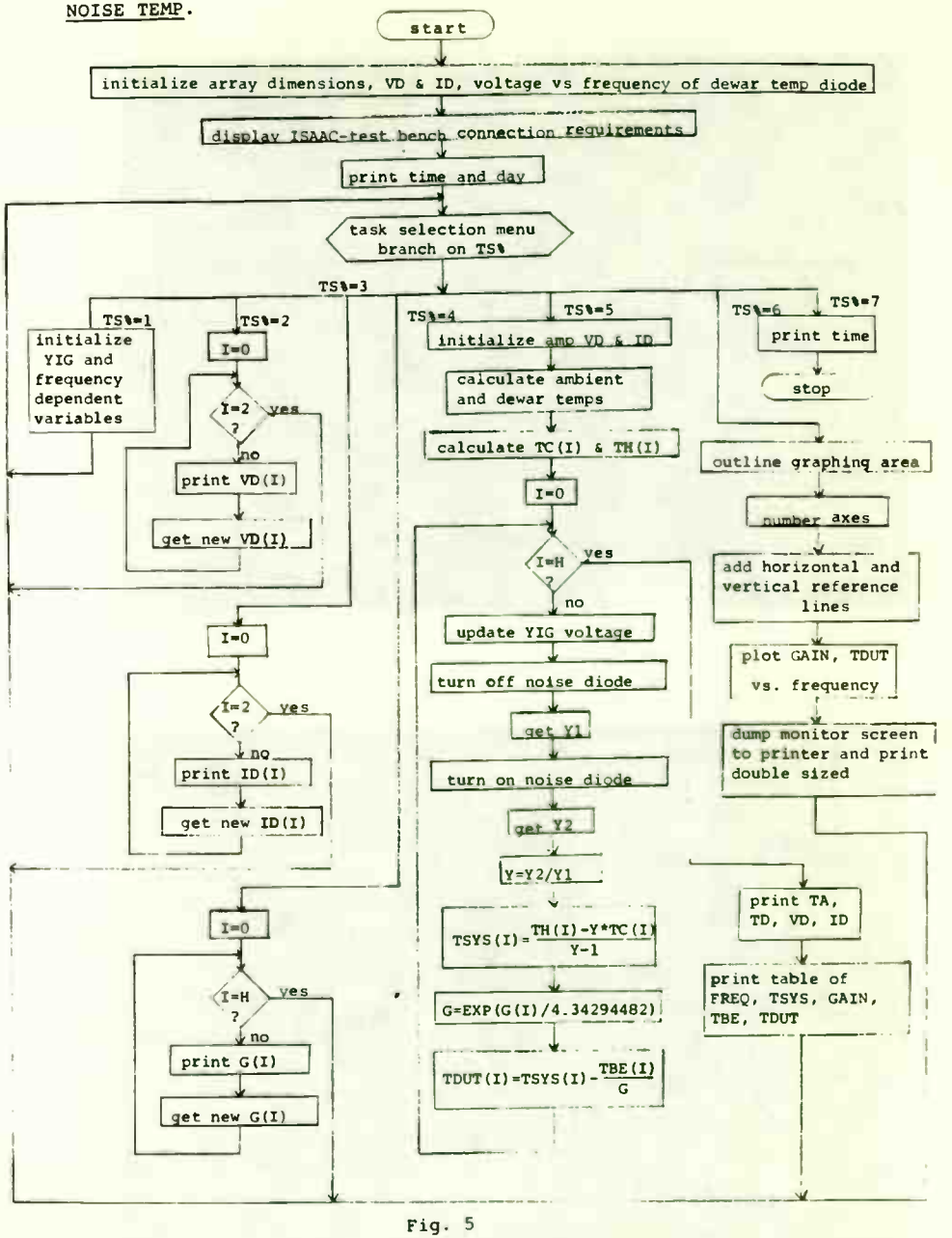


Fig. 5

easily calculated, due to small but highly significant dimensional uncertainties; however, the Inconel wires are the primary heat transfer path.

In order that gaseous heat conduction be negligible, pressure in the TMXO must remain below 10^{-3} to 10^{-4} Torr. This is assured by a number of processing steps. First, the hybrid and crystal packages are tested for hermeticity. Second, they are joined by reflow soldering in vacuum to eliminate trapped gas, which could, over time, leak into the TMXO cavity causing an increase in preasure. Third, all components are cleaned in an elaborate series of procedures. In the last stage before seal, the TMXO is outgassed in a vacuum-bake cycle. In this process, the TMXO is evacuated via its tubulation to a pressure of about 10^{-8} Torr while being maintained at a temperature of 150°C with a wrap-around heater and proportional controller.

In addition to these measures, the TMXO contains a non-evaporable, refirable getter located just above the vacuum header. The getter's purpose is to adsorb any gases liberated after seal. The getter is activated by an initial firing just prior to seal. During firing, the getter reaches temperatures up to 800°C. A heat shield between it and the header protects the latter, while the crystal and hybrid are protected by their heat shield. Hydrogen is liberated by the getter during activation, and pumping continues until this is completely removed. Finally, the OFHC tubulation is pinched off, completing the sealing cycle. All of the assembly processes are carried out under clean room conditions. In addition, a number of procedures are used to control materials and components used, and are just as important as the steps described.

Electrical Design

Principal electrical functions are the oscillator, the voltage regulator, the temperature controller and heater, and the optional output buffer. The circuit designs used are for the most part fairly conventional and will be only briefly described.

As noted earlier, all circuitry except the optional buffer is contained in the hybrid circuit module. The buffer, when used, is mounted on the outside face of the ceramic vacuum header.

Figure 3 shows the circuit of the oscillator and its voltage regulator. The regulator portion of U1, an LM10, and Q9 make up the voltage regulator.

In describing the oscillator, the standard operating frequency of 10 MHz will be assumed. The oscillator sustaining circuit contains 2 stages of gain, Q1 and Q4. The first stage, Q1, drives the pi-section filter consisting of C2, C7, C13, and L1. The crystal unit has a number of resonances, or modes. The filter must select the one which is wanted and reject the others. Thus it must pass the 3rd overtone C-mode frequency of 10 MHz while adequately suppressing the 3rd overtone B-mode which is about 9% higher in frequency. In

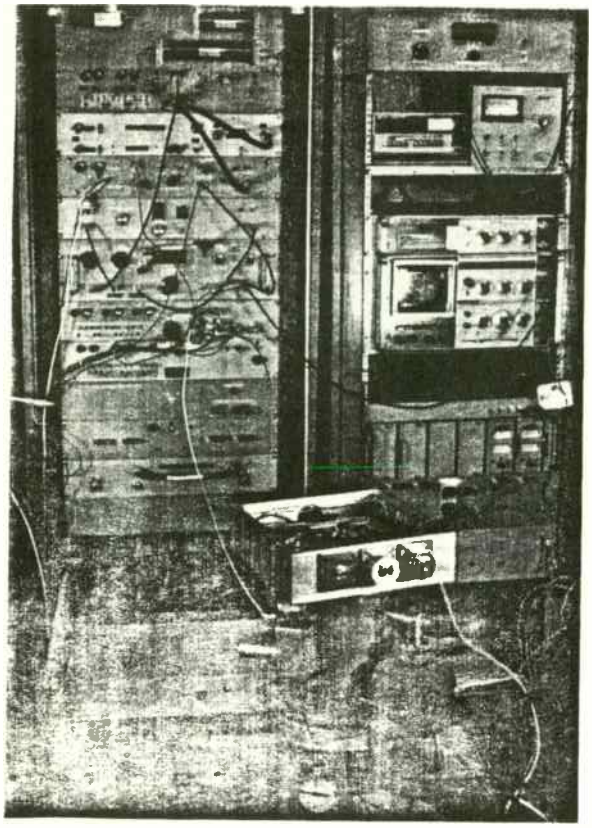


Fig. 8

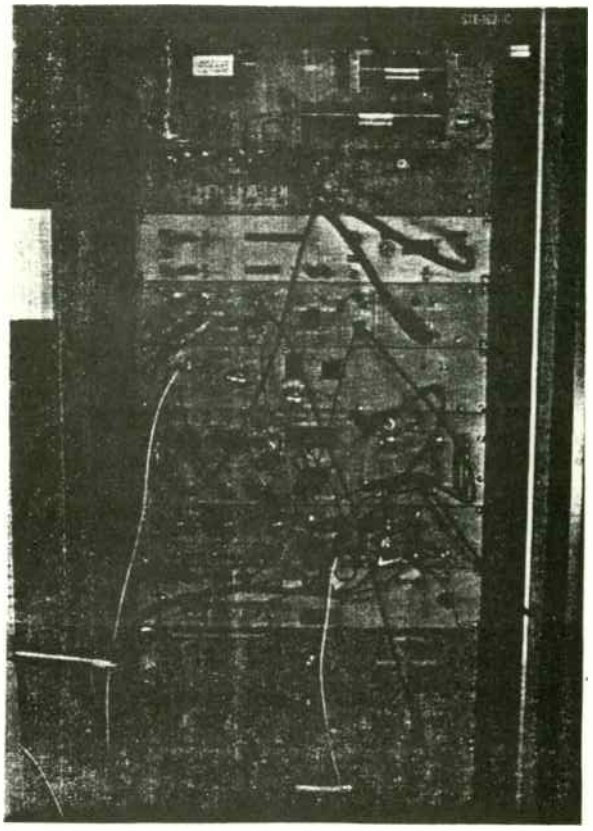


Fig. 9

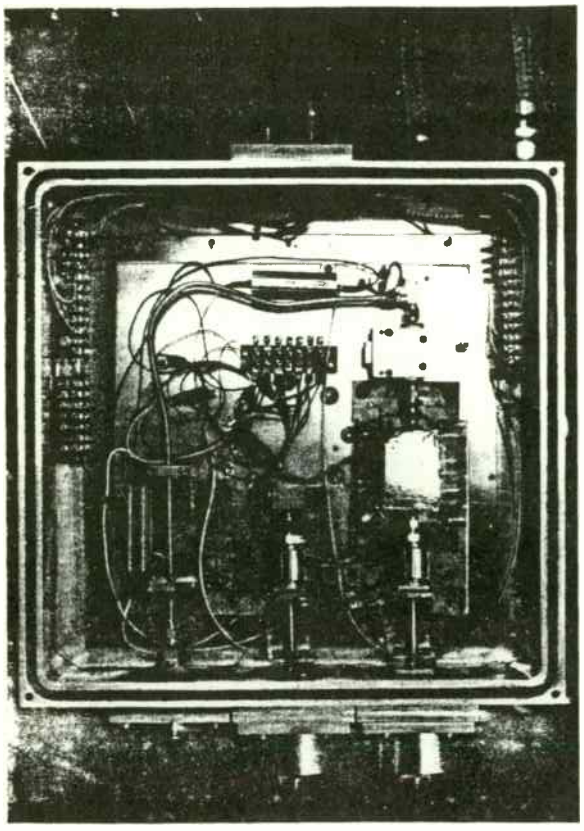


Fig. 6

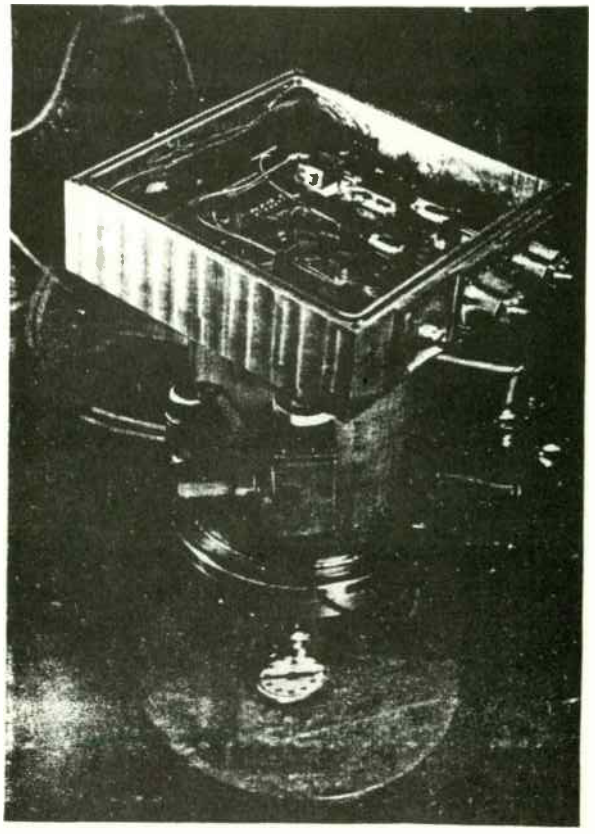


Fig. 7

addition, it rejects fundamental and fifth overtone modes. At the 3rd overtone C-mode, the phase shift through the filter is 180°.

The second stage, Q4, drives the limiter, which consists of Schottky diodes D3 and D4. The limiter feeds back to the base of Q1 to close the loop. The crystal unit is in the emitter of Q1. Away from resonance, emitter degeneration reduces the first stage gain, so that the loop gain is less than unity. At 10 MHz the series combination of the crystal, blocking capacitor C12, varactor D1, and the load capacitor is resonant, thus determining the frequency of oscillation. The value of the load capacitor is set by grounding some or all of the "Frequency Adjust" points. Varactor D1 allows external frequency adjustment of at least $\pm 1 \times 10^{-7}$. Oscillator output is taken from Q8. The resistor R22 and blocking capacitor C12 prevent the occurrence of a d-c bias across the crystal unit. This is required because the resonant frequency of SC-cut crystals is sensitive to d-c bias, and because a d-c bias can cause frequency aging due to diffusion of electrode metal into the quartz body of the resonator.

A current-efficient bias network is used to keep the power dissipation low. D5 is a constant current diode which controls the bias current. D3 and D4 are forward biased, their current ratio being set by resistors R5, R19, and R9. The same current is used to set the operating points of oscillator circuit transistors Q1, Q8, and Q3, and transistor Q7 in the temperature control circuit.

The temperature controller schematic, shown in Figure 4, is a conventional proportional controller with added power limiting. Temperature is sensed by a glass bead thermistor in a Wheatstone bridge arrangement. Bridge arm resistance is 51K ohms. The unit is set to the crystal's turnover temperature by selecting the value of the thermistor and an external resistor. Q6 is the heater transistor. Gain is provided by the operational amplifier portion of U1. Heater current is sensed as the voltage across R16. The voltage across R21 is proportional to the heater voltage. The sum of these voltages is used to maintain constant warm-up power for a range of supply voltages by setting the base voltage of Q7. When the circuit is first energized, thermistor RT1 is very high in resistance, unbalancing the bridge and driving the current through the heater to a high value. Q7 is therefore turned on, limiting the heater current to approximately 1.5 amp and the rate of temperature change to about 2°/sec. As final oven temperature is approached, the thermistor resistance drops rapidly, which acts to reduce the heater current. The base voltage of Q7 drops, and it cuts off. The bridge comes almost to balance, regulating the heater current to the value required to maintain a stable operating temperature.

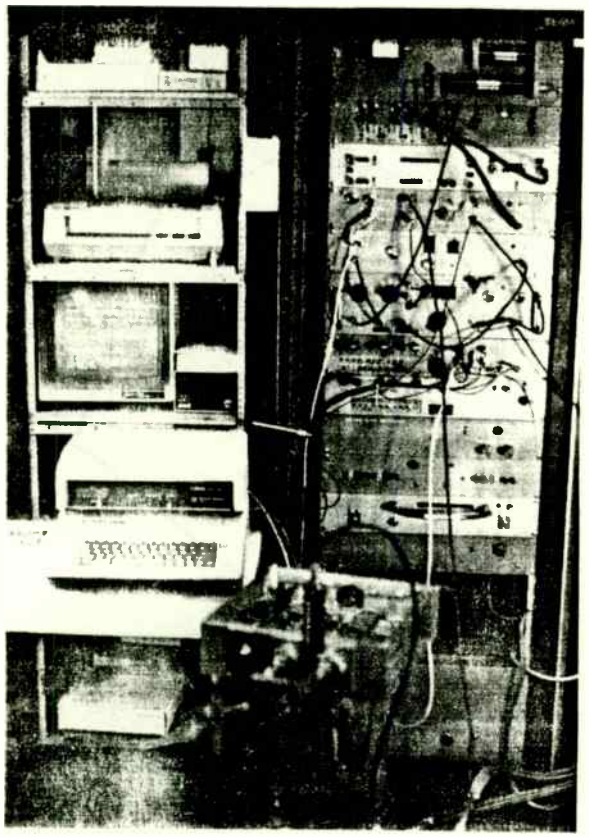


Fig. 10

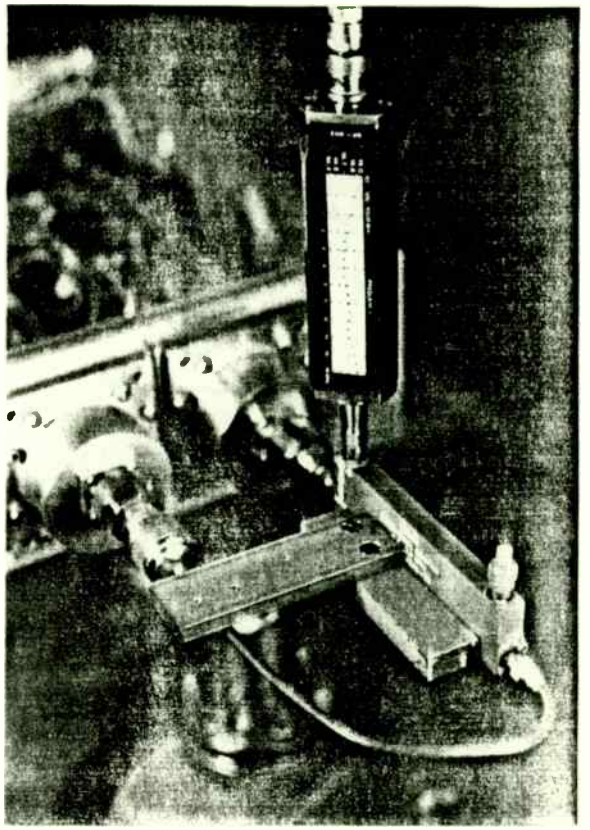


Fig. 11

Hybrid Circuit Module

Figure 5 shows a completed hybrid circuit module prior to seal. The package is a custom design consisting of a multilayer ceramic base to which a Kovar sidewall is brazed. Connections to the hybrid are via "through" metallization of the ceramic base, terminating at exterior castellations. Pins are brazed to 6 of these. During final assembly, the Inconel support wires will be welded to the pins. The lower surface of the enclosure is metallized to permit subsequent attachment of the resonator package by solder reflow.

The octagonal shape of the hybrid permits linear parallel seam sealing using a stepped Kovar lid, while providing the maximum substrate area. To four side walls are brazed small turrets which hold the polyimide bumpers.

A beryllia heat spreader is bonded to the floor of the hybrid package. The heater transistor is eutectically bonded to a central, metallized pad. This transistor is used to heat the entire hybrid/crystal subassembly; the function of the heat spreader is to reduce lateral thermal gradients in the subassembly.

The hybrid substrate is epoxy-bonded to the top surface of the heat spreader. Both the heat spreader and the hybrid substrate are octagonal, but the latter has a central hole to accommodate the heater transistor. Substrate material is 94% alumina. Metallization is thick film gold; screened-on resistors use standard, ruthenium-based inks. Chip devices are epoxy-bonded to the substrate; connections are made by thermosonic gold ball bonding. Input/output connections are also wire bonded.

Crystal Resonator

The crystal unit is a 3rd overtone SC-cut quartz resonator in a special ceramic flatpack. Figure 6 shows the resonator in its package prior to sealing. The package consists of a ceramic frame and two ceramic covers, not shown. Mounts are brazed onto metallized pads, and support the plano-convex blank at four points. The lowest mechanical resonance is above 2 kHz. Gold electrodes are used. External connection is achieved via co-fired through metallization. Sealing surfaces are metallized and gold plated. Gold gaskets are used between covers and frame. The package is sealed by thermo-compression bonding.

The SC-cut is chosen for several reasons. First, in the vicinity of turnover, the frequency vs. temperature curve of the SC-cut is much flatter than that of AT- or BT-cut crystals, reducing the oven temperature control requirements. Second, very fast warm-up can be achieved due to the SC-cut's insensitivity to thermal gradients. Third, the stress compensation inherent in the SC-cut reduces acceleration sensitivity.

Low aging is obtained by a combination of measures. Electrodes are gold. Mounts are designed for minimum stress. Stringent cleaning procedures are

POST AMP #1-1 5/18/84

TD = 13 DEG K TA = 288.091199 DEG K
VD1 = 4 VOLTS VD2 = 0 VOLTS VD3 = 0 VOLTS
ID1 = 20 MA ID2 = 0 MA ID3 = 0 MA

FREQ(GHZ)	TSYS(DEG K)	GAIN(DB)	TBE(DEG K)	TOUT(DEG K)
4.2	108.312151	12.6	160	99.5194972
4.25	100.915277	12.75	161	92.368037
4.3	99.5761708	12.9	167	91.0113857
4.35	97.5047259	13.15	173	89.123544
4.40000001	88.9786261	13.35	174	80.9331963
4.45000001	79.7263862	13.6	178	71.9564044
4.50000001	73.1402199	13.85	183	65.5988343
4.55000001	71.7695746	14.1	185	64.5722394
4.60000001	72.1413153	14.35	187	65.2731362
4.65000001	69.3786729	14.55	191	62.6793121
4.70000001	68.0493226	14.65	195	61.3653508
4.75000001	68.143501	14.75	197	61.5446819
4.80000001	69.511806	14.8	202	62.8229573
4.85000001	69.4286967	14.75	208	62.4614155
4.90000001	72.1272758	14.65	214	64.7921451
4.95000001	76.0534894	14.5	219	68.2830752
5.00000001	81.0295756	14.4	229	72.7150881
5.05000001	83.6417352	14.2	238	74.5932275
5.10000001	89.2936613	14	247	79.4604141
5.15000002	99.2047802	13.5	259	87.6356752
5.20000002	110.239198	13.2	274	97.1247238

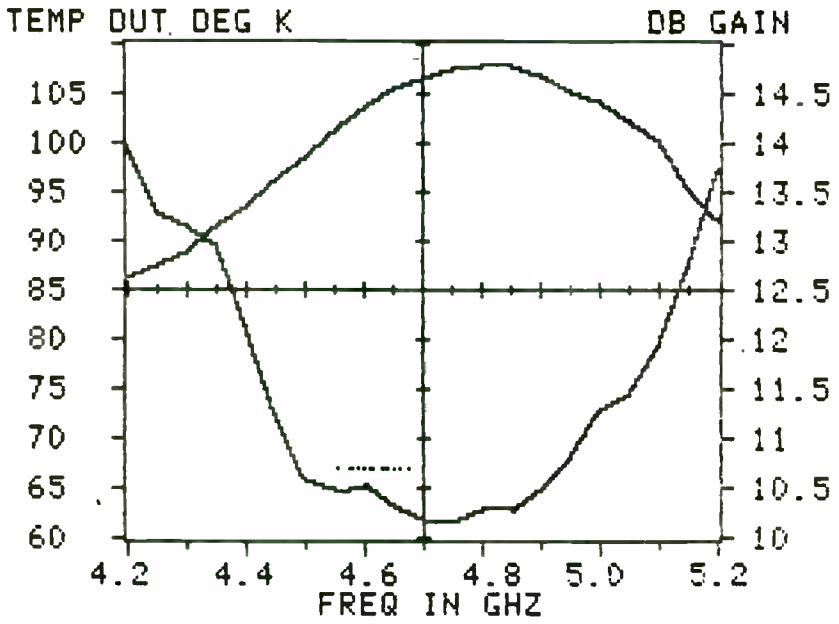


Fig. 12

FREQ(GHZ)	VHOT(MV)	VCOLD(MV)	Y FACTOR	TSYS(DEG K
2.2	313.26	100.1	3.12947053	19.6392006
2.21	301.97	96.18	3.13963402	19.1592536
2.22	302.59	95.97	3.15296447	18.5366238
2.23	316.38	100.08	3.16127098	18.1525326
2.24	342.4	108.33	3.16071264	18.1782578
2.25	371.2	117.69	3.15404877	18.4863177
2.26	416.28	132.34	3.14553423	18.8827161
2.27	425.43	135.24	3.1457409	18.873057
2.28	413.09	130.95	3.15456281	18.4624867
2.29	402.78	127.79	3.15188982	18.5865319
2.3	415.78	132.06	3.14841739	18.7481376

HOT TEMP = 296.56 DEG K
COLD TEMP = 81.4 DEG K
CH#1/30MHZ IF FILTER/VD1=1.476V/ID1=4.23MA/VD2=5.054V/ID2=6.80MA/VG1=-297V/VG2=-0.864V

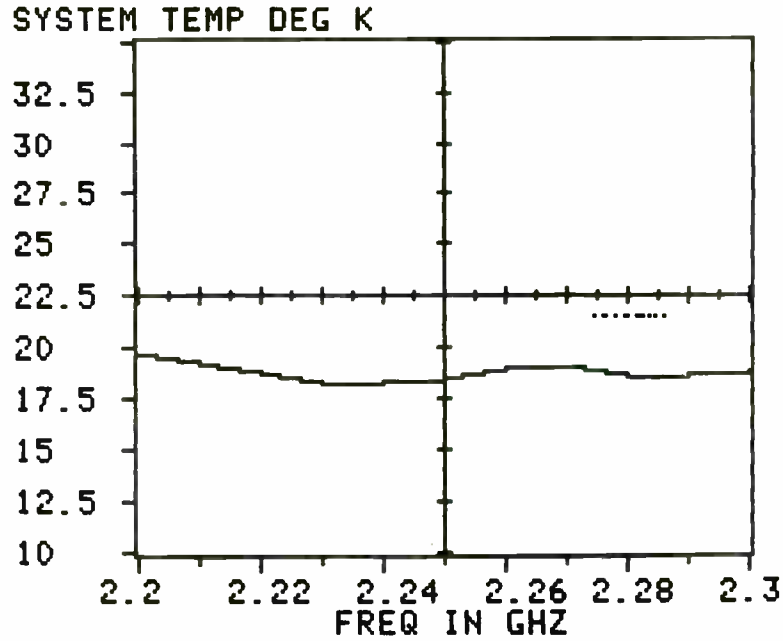


Fig. 13

employed throughout resonator processing. An extensive vacuum bake is used prior to seal to outgas all resonator components. Figure 7 gives the aging results for one of the first TMXO resonators fabricated at PTI. The rate at day 30 is less than 1×10^{-10}/day.

Performance Data

The complete TMXO specification includes a long list of detailed requirements. We wish to discuss the most important of these.

Warm-Up Time. An important feature for many applications is fast warm-up. The TMXO has a specified warm-up time, from an ambient temperature of -55°C, of 4 minutes. Table 1 shows the measured warm-up time for 4 units.

Table 1

Warm-Up Time (from -55°C)

Unit No.	Time (Minutes)
10	1.9
15	3.0
18	2.4
24	2.4

Power Consumption. The maximum specified input power, after warm-up, is 250 milliwats, excluding power required for the optional output buffer. Figure 8 shows typical values measured over the operating temperature range. The buffer power requirement depends upon the output required, but is typically 50 mW or less.

Frequency vs. Temperature. The total frequency error budget includes half-a-dozen items, of which this parameter, and long-term aging, are the two largest components. A variation of $\pm 5 \times 10^{-9}$ is allowed over the operating temperature range. Figure 9 shows a variation of $+0.1, -2.0 \times 10^{-9}$, indicating that the oven temperature has been correctly set very nearly to the crystal's upper turnover point.

Aging. The maximum specified aging rate is 2×10^{-10} per day after 30 days continuous operation. Figure 10 shows frequency change for the first 21 days for TMXO No. 10. The aging rate for days 10 to 21 is already slightly better than the specified value at day 30.

Phase Noise. Figure 11 compares the measured SSB phase noise density, $\mathcal{L}(f)$, with the specification. It should be noted that measurements are exclusive of the output buffer. In some instances, degradation may occur when logic-level buffers are used.

APPENDIX : HARDWARE SPECIFICATIONS

All specifications typical @ 23°C.

Storage temperature: 0-70°C.
Operating temperature: 10-40°C (30 min. warm up)

A/D Subsystem

Resolution: 12 bit (.025%)
Channel acquisition time: 100 microseconds
A/D conversion time: 25 microseconds
Accuracy: +/-.05% of full scale
Differential nonlinearity: +/- .025% of full scale
Temperature coefficient: +/- 75ppm/°C
Common mode rejection (differential mode): 70 dB
Input bias current: +/- 100 nanoAmps
Input impedence: < 100 picofarads
> 100 megohms

D/A Subsystem

Resolution: 12 bit (.025%)
Capacitive load: < 1000 picofarads
Accuracy: +/- .05% of full scale
Differential nonlinearity: +/- .025% of full scale
Output current: +/- 5 milliamperes
Overshoot: < 2% of full scale
Temperature coefficient: +/- 50ppm/°C
Settling time: < 5 microseconds (to < 2% of full scale)

Binary Input Subsystem

Input port: 16 bit
Input signal: (high)+ 2 Volts/40 microamperes
(low) + 0.8 Volts/0.9 microamperes
Communications: STROBE, $\overline{\text{HOLD}}$, and CLEAR TO SEND

Binary Output Subsystem

Output port: 16 bit
Fan out: 4 standard TTL loads (50 LS TTL loads)
Output signal: (high) + 3.1 Volts/2.6 milliamperes
(low) + 0.5 Volts/20 milliamperes

Binary Output Subsystem (cont.)

Communications: STROBE, GATE, CLEAR TO SEND
Communications fan out: 4 standard TTL loads
(20 LS TTL loads)

Schmitt Trigger Subsystem

Response time: 5 microseconds
Hysteresis: 20 millivolts

Counter Device (Channels 0-6)

Input signal: (high) + 2 Volts/20 microamperes
(low) +0.8 Volts/400 microamperes
Maximum count frequency: 10 megahertz (50% duty cycle)
Minimum count frequency: DC

Counter Device (Channel 7)

Maximum input voltage: 50 Volts (DC + peak AC)
Sensitivity: 100 millivolts RMS
Maximum count frequency: 2 megaHertz (50% duty cycle)
Minimum count frequency: 0.5 Hertz (sine wave)

Timer Subsystem

Accuracy: (dependent on Apple CPU clock)
Resolution: 1 millisecond

&&&

Short-Term Stability. The short-term stability is shown in Figure 12, which plots the Allan variance, $\sigma_y(\tau)$, between 0.1 and 10 sec., and is well within specification.

Improvement Program

Notwithstanding the unequalled combination of low power, frequency accuracy, and size offered by the TMXO, further improvements are needed for a number of applications. Although not all of the following are needed in each instance, these areas have been targeted:

Phase Noise

Acceleration/Vibration Sensitivity

Nuclear Survivability

Manufacturing Cost

Work in these areas are being carried out under LABCOM sponsorship of an Improved TMXO (ITMXO). This 36 month program is still in its initial stage. Tasks concern circuit design and hybrid construction, crystal unit design and processing, and overall mechanical design.

Conclusion

The present TMXO and its unique ceramic flatpack crystal are the result of many years of development by the U.S. Army and its contractors. Previously, there has been no merchant source for the crystal, which is essential to the success of the TMXO. Now, for the first time, the TMXO and its resonator are being manufactured in a single facility and sold commercially.

Acknowledgment

We would like to thank Dr. J.R. Vig, Dr. R.L. Filler, V. Rosati, and S. Schodowski of the U.S. Army Electronic Technology and Devices Laboratory for encouragement and generous support. We would also like to thank the staff members of Bendix Communications and General Electric who provided assistance and the benefit of their experience, especially E. Laszlo, R. McGill, and D. Brown of Bendix, and T. Wagner and J. Keres of General Electric.

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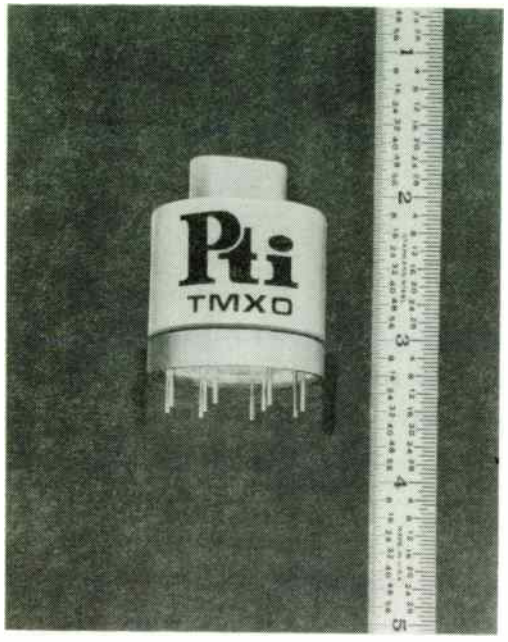

FIGURE 1. The TMXO

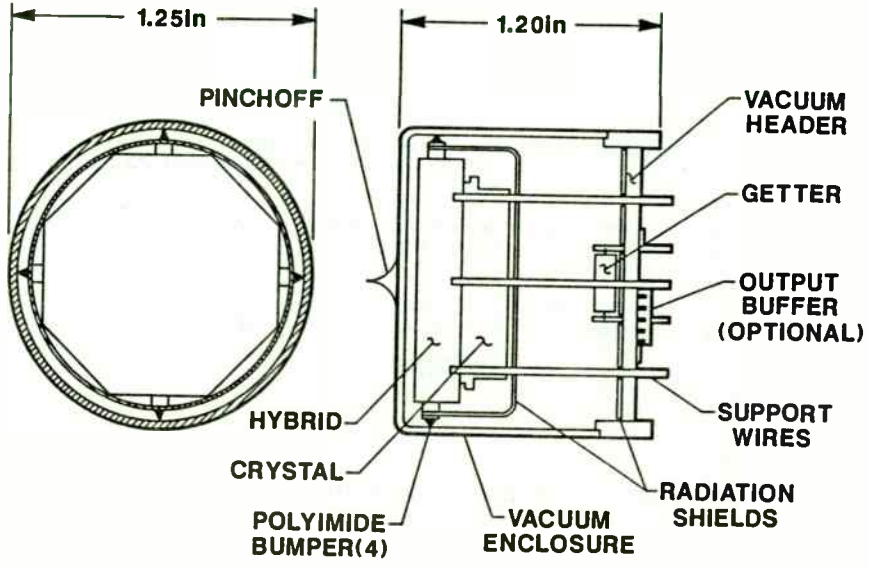

Figure 2. Simplified TMXO Construction

TEMPERATURE COMPENSATION CIRCUIT FOR SPACE DATA TRANSMITTERS

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A B S T R A C T

Temperature compensation for data transmitters used in spacecraft is a long felt requirement to maintain a constant equivalent isotropic radiated power. Presented in this paper is a simple and efficient technique which incorporates an automatic gain adjusting circuit associated with temperature sensitive components. The advantages over other types of schemes are explained. The application of this scheme is explained with the help of an X-band data transmitter qualified for on-board use in the Indian Remote Sensing Satellite.

****

I N T R O D U C T I O N:

The design of systems for space applications calls for best efficiency, as DC power is precious for spacecraft, while avoiding thermal stress on components to ensure reliable operation over the wide temperature ranges.

Efficiency and reliability are two vital parameters for a space system design. No compromize on reliability is possible in space system design as no scope exists after launching a spacecraft into orbit for repair or replacement of a system. Usage of 100% screened and tested components with proper derating will ensure that components are reliable and that circuits are designed to avoid additional stress on the components over the severe environment change, as quite a few parameters will vary with temperature. Temperature effects accumulated over all the stages of the system result in unwanted effects in alarming proportion and may even lead to failure of the system.

In an amplifier chain, for example, the drive requirements of an amplifier stage change with temperature, as base emitter voltage (Vbe) and current gain (B) of a transistor change. At low temperatures the amplifier may not have sufficient drive to give required output and at

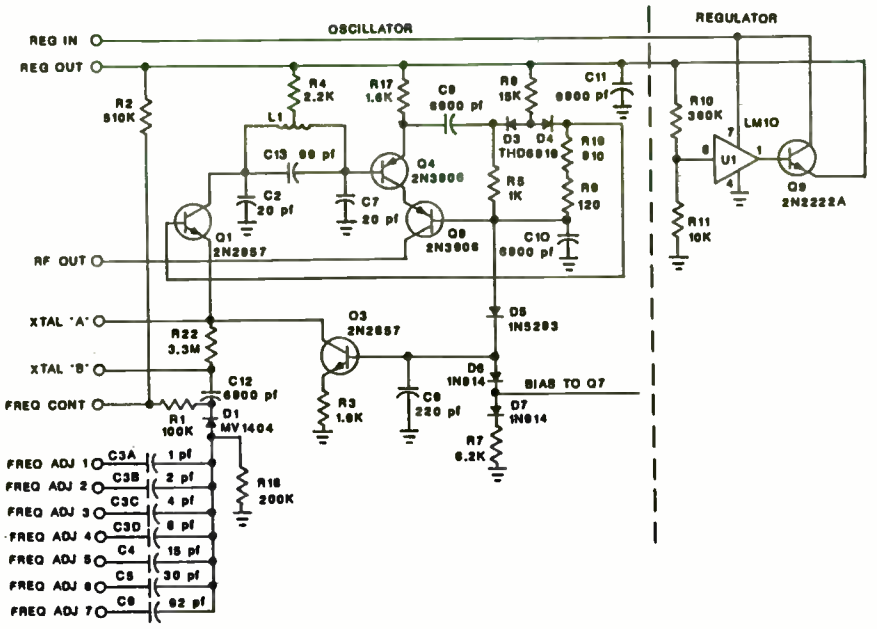

FIGURE 3. Oscillator and Voltage Regulator Circuit Diagram

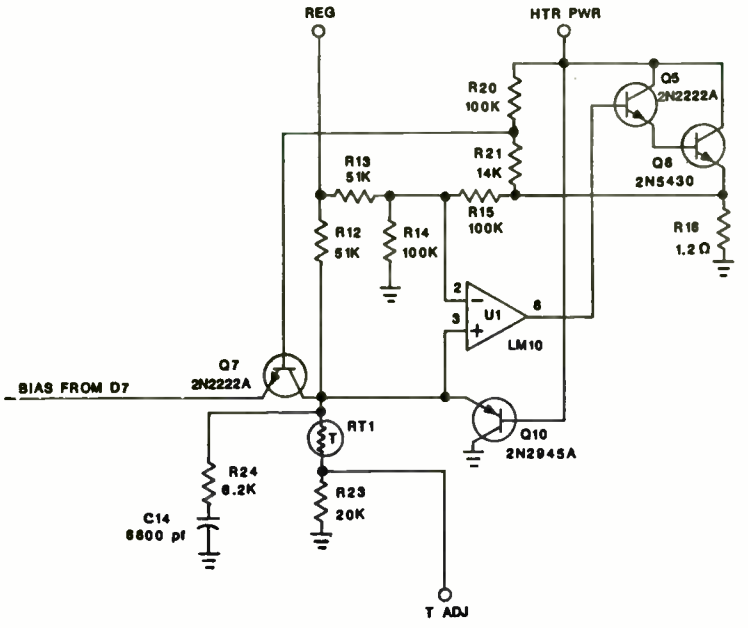

FIGURE 4. Temperature Controller Circuit Diagram

high temperature the transistor may be driven into hard saturation resulting in poor efficiency with over dissipation.

In a data transmitter the level at the input of a power amplifier, viz. TWTA, should remain constant over the temperature range to avoid phase shift changes. Power variation in each stage of a transmitter has to be minimized to overcome unwanted effect. This can be achieved by incorporating temperature compensation techniques.

COMPENSATION TECHNIQUES FOR THE DESIGN OF A TRANSMITTER:

The basic transmitter to transmit data from spacecraft uses RF amplifiers, frequency multipliers to generate microwave signals from the basic crystal oscillator used as a high stability frequency source, a modulator to enable the microwave carrier to carry the data, and final power amplifiers such as TWTA to boost the modulated microwave signal to a sufficient level so the antenna can radiate enough power to enable the ground system to capture the signal to get the data. A typical transmitter schematic is shown in the Fig.1.

All stages of the transmitter have to be designed in such a way that the level at the input of TWTA remains fairly constant over the full temperature range and no transistor or diode dissipates more power than the designed value, even at extreme temperatures. This calls for maintaining the variation in each stage within limits.

To some extent, variation in the passive component values and their effect on gain and power output can be estimated from the available data and can be taken care of in the design by providing wider band widths.

To reduce the power and gain variations resulting from various parameter changes due to temperature variation, many methods are available and their merits are discussed in the following paragraphs.

TEMPERATURE COMPENSATION IN FREQUENCY MULTIPLIERS:

The variation of the power output in frequency multipliers using step recovery diodes can be minimized by compensating for the change of lifetime of the SRD. The bias is directly proportional to the diode lifetime. The rate of change of SRD's lifetime is +0.5% to 0.7% per ^{o}C (1). This is closely matched by the rate of resistance change of a silicon resistor (sensitor).

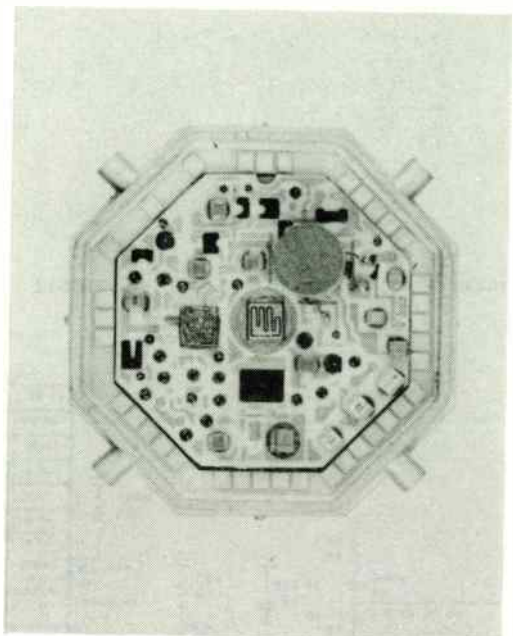

FIGURE 5. Hybrid Circuit Module Prior to Sealing

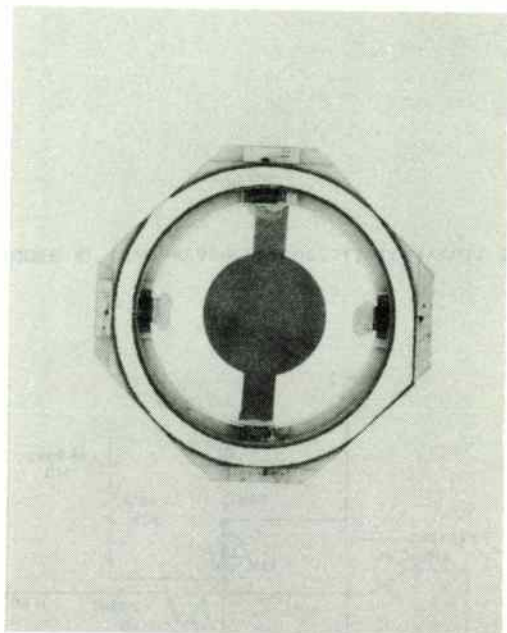

FIGURE 6. SC-Cut Resonator Mounted in Its Ceramic Flatpack. Not shown are ceramic top and bottom covers.

The multiplier can be temperature compensated simply by using a sensistor to develop the bias voltage, instead of a resistor. This type of simple compensation maintains the output variation within 1 dB over a fairly wide temperature range.

For further compensation, the power output of the driver amplifier (at input frequency) should be varied to compensate for the variation in the conversion loss of the multiplier with temperature by adjusting the gain of the preceeding stages, using temperature sensitive components in the bias/supply circuitry of the driver amplifier.

TEMPERATURE COMPENSATION IN AMPLIFIERS:

A simple and coarse method to restrict the output variation in an amplifier to some extent is to add a resistor in series to the supply voltage. This method is inefficient and also inaccurate.

The commonly used technique is to operate the power amplifier stages in Class C and to drive them fully into saturation where decrease in input level will not result in equal reduction in output level. The collector efficiency is reduced as the transistors are operated in the gain compression region. This carries the disadvantages explained earlier and cannot take care of the variation of preceeding stages totally or the variation of succeeding stages.

Another technique is to use temperature sensitive components like thermistors in the bias network of Class A stages. This cannot take care of the variation of other stages.

Since efficiency is the prime consideration for space systems, there is a need to look at other methods, such as the leveling loop approach, which is complex.

The standard leveling loops control the gain of the preceeding Class A stages by sensing output power level. Another way is to use an variable attenuator like a PIN diode attenuator to keep the output level at constant value by varying the attenuation automatically depending on output level.

The basic circuit schematics to provide autoleveling are shown in Fig.2. The necessary circuit elements include a directional coupler, detector, feedback amplifier and a PIN diode attenuator in the second approach. The directional coupler samples the RF output signal which is converted to a

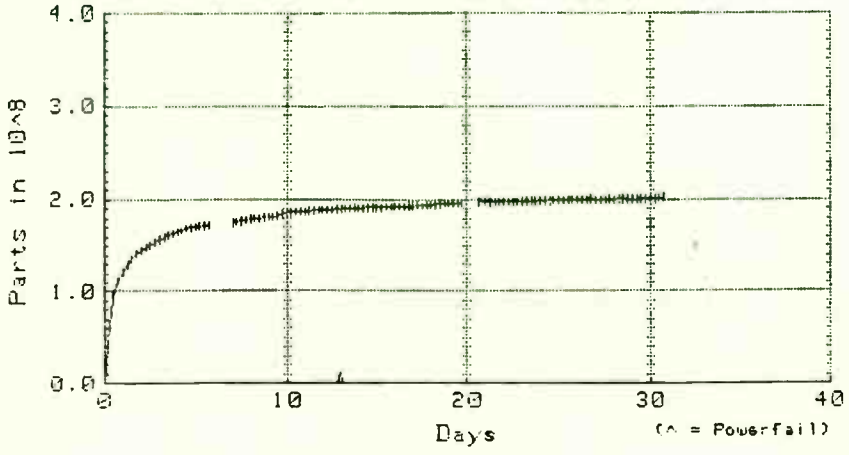

FIGURE 7. Frequency Aging Curve of a TMXO Crystal Unit. The unit is aged in a test oscillator prior to use.

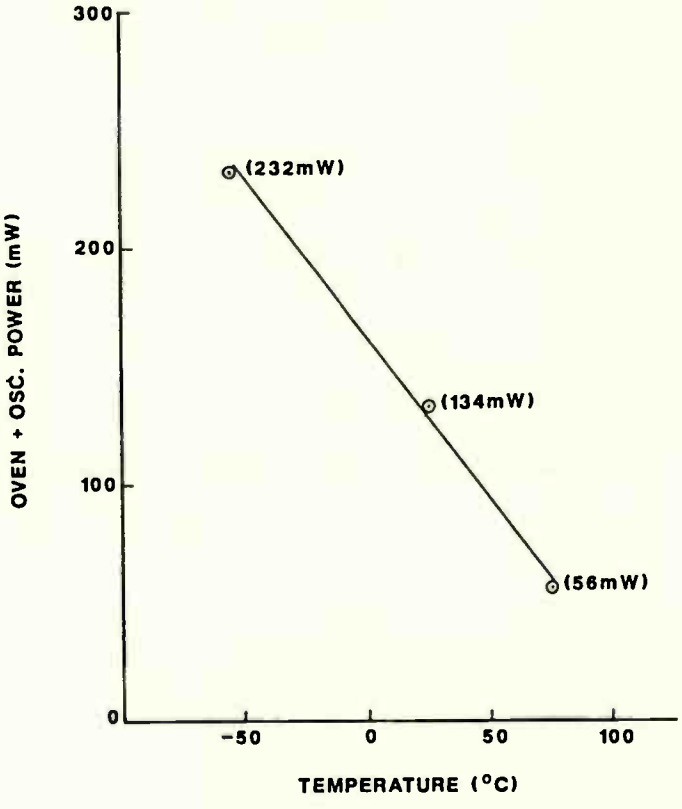

FIGURE 8. Input Power vs. Temperature, TMXO No. 10

proportionate DC signal which is amplified by the feedback amplifier, the output of which controls the bias current of the transistors to adjust the gain or the bias current through the attenuator diode to adjust the attenuation to keep the output constant. This type of leveling loop technique to keep the output constant by controling the gain or attenuation at low power level, maintains efficiency of the transmitter.

Another simple leveling loop technique (2) which maintains both efficiency and output of cascaded amplifier stages uses the voltage drop across a resistor connected in series with the collector bias network of the output transistor to control the gain of the preceeding Class A amplifier stage.

Power output and efficiency of the amplifier using this simple leveling loop are nearly flat against variations of temperature and input drive level. This approach cannot take care of the variations of succeeding stages.

This disadvantage can be overcome by incorporating a temperature sensitive resistor, viz. thermistor, to drive the reference voltage. The schematic of the amplifier circuit used to maintain the output of the final multiplier (i.e. at the input of the TWTA shown in Fig.1) is shown in Fig.3.

The cascaded amplifier section consists of one Class A amplifier driving the Class C amplifier stage. The voltage generated across resistor R_1 connected in series to the collector supply of Q_2, is compared with the reference level generated by the resistors and thermistor network by a PNP transistor (Q_3). As the collector current of Q_2 changes, the bias voltage supplied to Q_1 by the comparator/feedback amplifier Q_3 changes, resulting in a change in the gain of the Class A amplifier Q_1 and thereby the drive level to Q_2 which brings the collector current of Q_2 back to the initial value. Since output power is nearly proportional to collector current, the output level remains constant.

Any change in the drive obtained from proceeding stages tries to change the current in Q_2 and the loop adjusts the gain of Q_1 to maintain the current in Q_2, thereby keeping the output level constant. The PNP transistor Q_4 connected as a diode in the bias circuit of Q_3 compensates for the changes in the emitter base junction of the transistor Q_3 over the temperature range.

The output power can be adjusted by changing the reference voltage at the base of Q_3. The thermistor network is designed in such a way that the change in the reference voltage due to temperature variation adjusts the output power of the amplifier to compensate the power

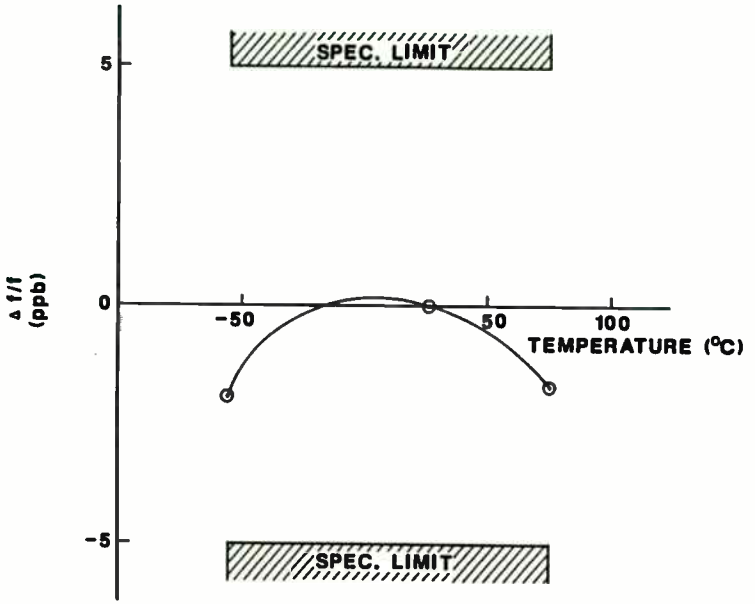

FIGURE 9. Frequency vs. Temperature, TMXO No. 10

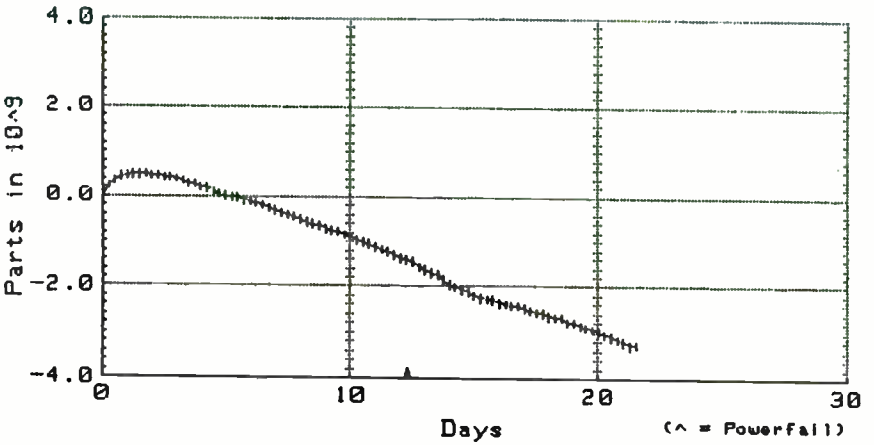

FIGURE 10. Frequency Aging Curve, TMXO No. 10

change in the succeeding stages. The temperature compensation network can be selected easily if the power variation in succeeding stages is known, else this can be estimated practically.

DESIGN OF THE COMPENSATING NETWORKS IN TRANSMITTERS

In a transmitter like the one shown in Fig.1 it is found that temperature compensation of the SRD frequency multipliers and the two stage amplifier preceeding the final multiplier, by incorporating the autoleveling loop associated with the thermistor network, is adequate to keep the power level at the input of the TWTA constant.

The first frequency multiplier can be of the order of 2 or 3 using a transistor, as the basic crystal oscillator frequency will be below 100 MHz. The following amplifiers also need not have any special compensation network and even need not be operated in hard saturation. The variation will be taken care of by the autoleveled amplifier following the second frequency multiplier.

In the frequency multiplier that uses SRDs, usage of a silicon resistor as the biasing resistor nearly compensates for the changes caused by lifetime variation with temperature. In spite of this compensation, power loss variation will be on the order of 1 dB over a $-20^{\circ}C$ to $+60^{\circ}C$ temperature range. This variation has to be taken care of by the proposed compensated leveling loop. The compensated leveling loop should be designed to take care of the variation in input level in various preceeding stages caused by the wide environment change and the loss variation in the succeeding stages. The current sensing resistor R_1 should be selected to be a low value (less than 10 ohms) as higher values drop supply voltage to the transistor, thereby reducing the available gain and power.

The Class C amplifier should be designed to have a higher compression point, i.e. to give higher power output at room temperature than normally required. In the potential divider network at the base of Q_2 a potentiometer P2 is used in place of the thermistor network (R3, R4 & R5). Resistor R6 is to limit the base current and in turn the collector current of the Class A amplifier (Q_1). This value is to be adjusted to limit the collector current within a safe limit when no input is fed and to be the normal operating current with drive at room temperature. It should be noted here that the collector current of the Class A amplifier will be maximum at no drive condition. To be on the safe side a high value can be

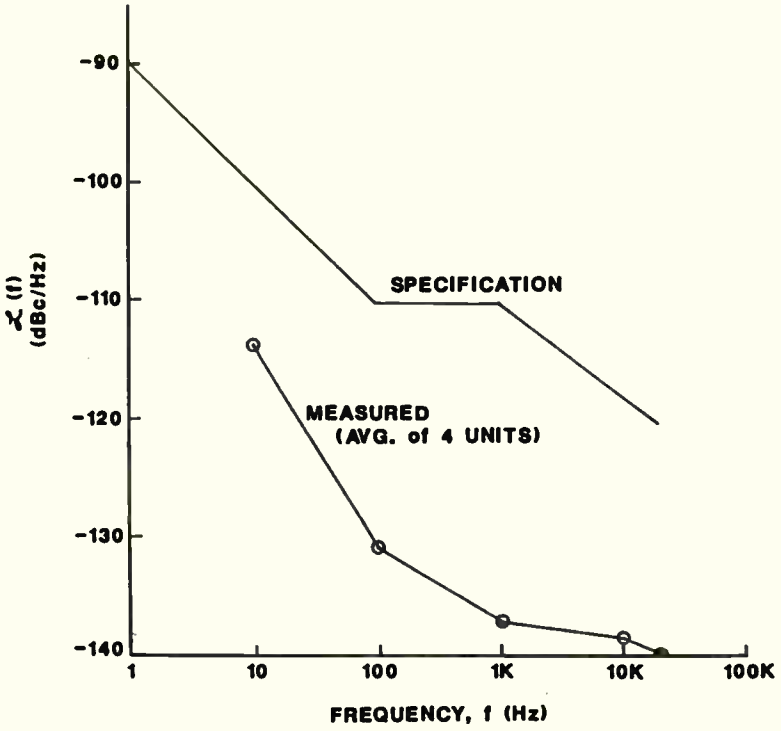

FIGURE 11. SSB Phase Noise Density (without output buffer)

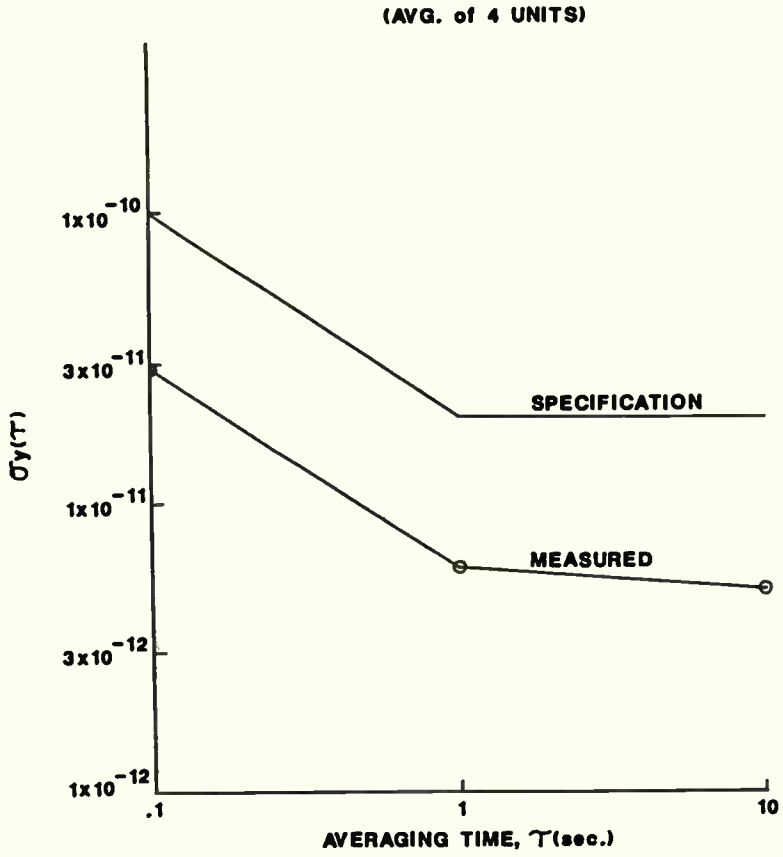

FIGURE 12. Allan Variance

choosen for R6 to start with which can be reduced after adjusting the reference voltage for the required output.

With normal expected drive to Q_1, the reference voltage at the base of Q_2 can be adjusted with the help of potentiometers P_1 and P_2 to get the required output from the Class C amplifier. The AGC action can be checked by varying the input level. To get a wider range for AGC action, if necessary the P_1 and P_2 combination may be readjusted by changing R_1. Check for the change in output level of at least $\pm$ 1 dB variation which will be higher than the expected variation in loss in the succeeding stages, by varying the potentiometer P_2.

If the loss of the multiplier and modulator at different temperatures is known, the output of the amplifier chain required to maintain the output of the modulator can be estimated and the corresponding P_2 values can be measured. If the variation is not known, or for greater accuracy the whole transmitter up to the modulator can be kept in hot and cold simulation chambers by bringing the potentiometer P_2 outside. The value of P_2 needed to keep the output level constant should be measured at different temperatures. A thermistor, resistor combination can be worked out to closely follow the resistance values required at different temperatures.

By using MSC 80064 and MSC 3000 transistors for Class A and Class C amplifiers, an amplifier chain is designed at L-band to drive an X5 frequency multiplier. A compensated leveling loop technique is incorporated in the L-band amplifier chain. The final power output is found to be within $\pm$ 0.2 dB over $-30^{\circ}C$ to $+70^{\circ}C$ against $\pm$ 4 dB input level variation to the amplifier. An isolator has to be used at the input of the Class A amplifier to take care of the return loss changes.

C O N C L U S I O N:

Different types of temperature compensation methods that can be used in designing telemetry/data transmitters for space application, where it is essential to maintain the efficiency of the system by avoiding thermal stress on components over the wide environments, are pointed out. A simple but more effective compensated auto leveling loop that controls the gain of a Class A amplifier stage, depending on the current of the final Class C amplifier, is presented. The output level is maintained constant against variations in the drive level upto $\pm$ 4 dB. The reference voltage generated by the potential divider

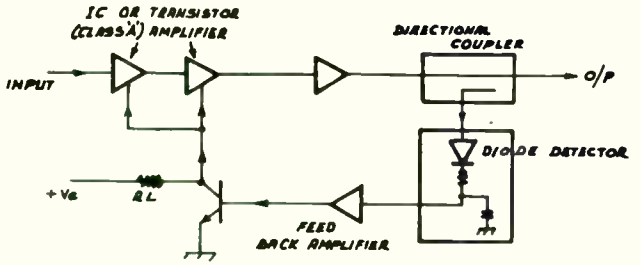

FIG. 2 a. SCHEMATIC OF AGC CIRCUIT.

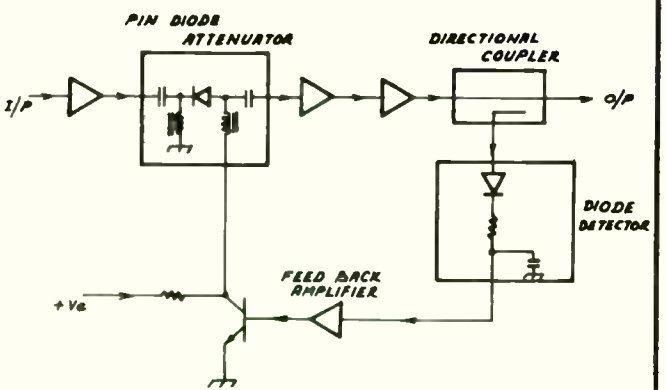

FIG. 2 b. SCHEMATIC OF AUTOLEVELLED CIRCUIT.

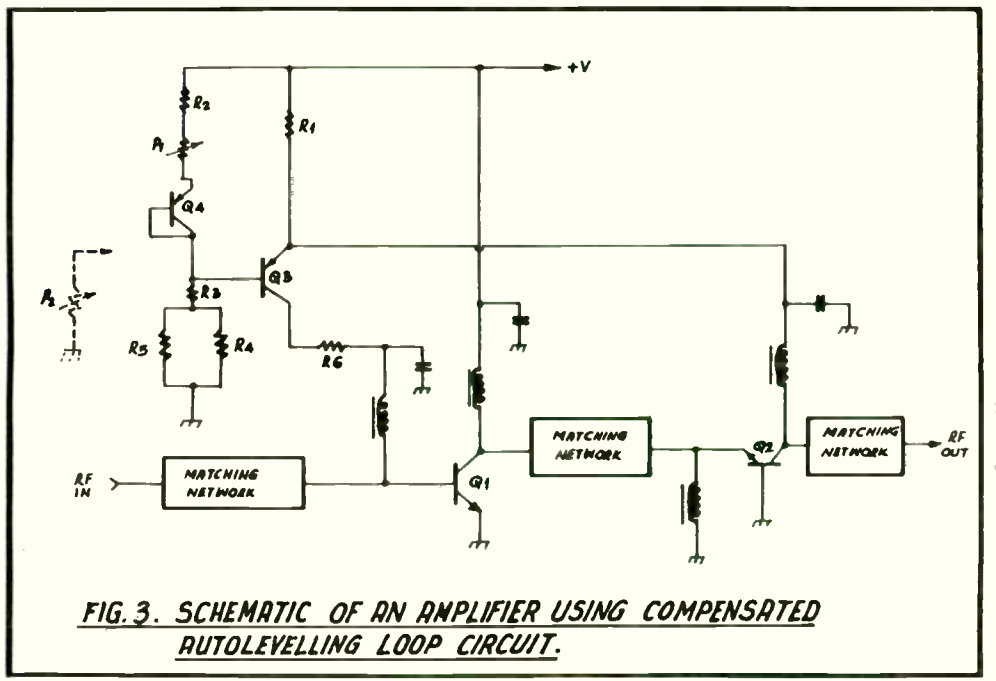

FIG. 3. SCHEMATIC OF AN AMPLIFIER USING COMPENSATED AUTOLEVELLING LOOP CIRCUIT.

DESIGN CONSIDERATIONS FOR SAWR OSCILLATORS

How to Specify a SAW Resonator From a Manufacturer

by
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INTRODUCTION

There are three different stages in designing an oscillator circuit using a SAW device: choosing the correct SAW device for the application; specifing the design parameters for the SAW device; and incorporating the SAW device into the oscillator design.

The two types of SAW devices used in oscillator designs are SAW delay lines and SAW resonators. An oscillator circuit using a SAW delay line is capable of being tuned over a frequency range of up to 1 MHz. Larger tuning ranges degrade the tuning linearity, phase noise and temperature stability of the device.[1] An oscillator circuit using a SAW resonator (SAWR) is used for fixed frequency applications. Its tuning range is related to the Q of the resonator. Increasing the Q narrows the tuning range. SAWR's typically have a Q between 5000 and 10,000.[2]

This paper focuses on the specifications for a SAWR device and the design parameters for incorporating the SAWR into an oscillator circuit. Two different oscillator designs are discribed. Their advantages and disadvantages are discussed along with the problems encountered.

DESIGN SPECIFICATIONS FOR SAW RESONATOR

To purchase a SAWR from a manufacturer certain specifications must be considered. Some of these parameters are determined by the manufacturer, others must be specified by you, the engineer. Specifications to consider include manufacture's tolerance, temperature drift, turnover temperature, aging, center frequency, phase shift, insertion loss and spurious rejection. An explanation of these characteristics is given along with some typical figures. It is important to understand these conditions because some of them affect the circuit design.

CENTER FREQUENCY: Center frequency is the resonant frequency of the SAW device. The useful frequency range of a SAWR is from 250 Mhz to 1.2 Ghz. There are SAWR's as low as 50 Mhz, but the physical size of the package is large and therefore expensive.[3] The upper end of the SAWR range is limited by the photolithographic processes. Greater resolution is required for higher frequencies.[4]

Some circuit configurations will not operate very close to the SAWR's center frequency. For this reason, it may be necessary to specify the center frequency at some offset from the operating frequency. SAW oscillator design #1 on page 11 is an example of this type of circuit.

consisting of a thermistor network is automatically varied to adjust the output level to compensate the power variation in succeeding stages. An X-band data transmitter designed with this type of temperature compensated leveling loop gave good results and was found to be very useful for space applications. It is found that a compensated leveling loop in the final amplifier chain preceeding the last multiplier is adequate to take care of all the variations caused by temperature change.

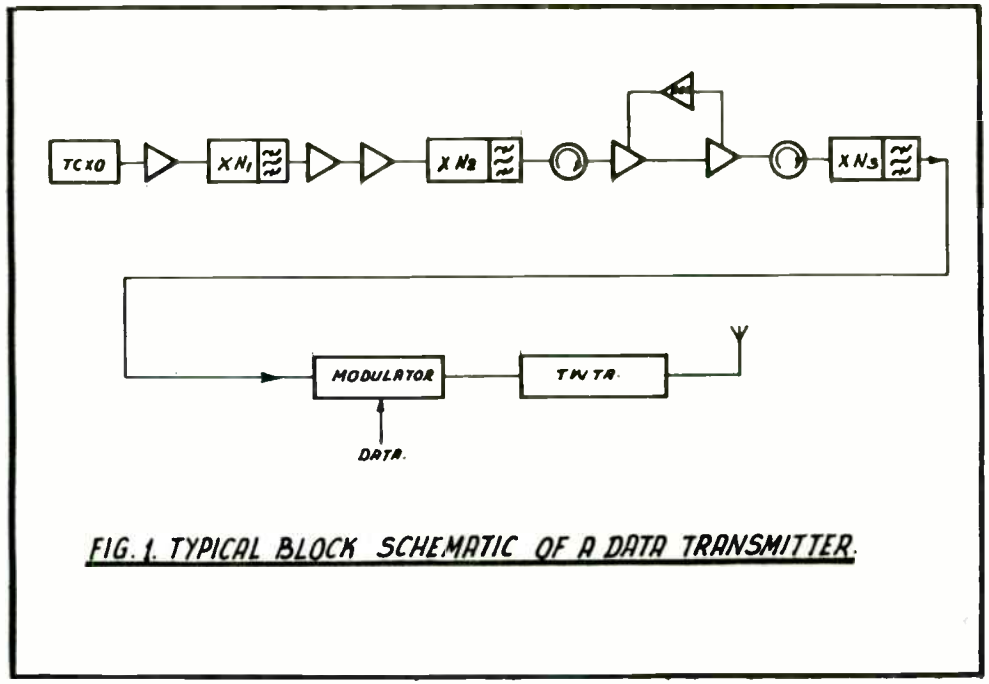

FIG. 1. TYPICAL BLOCK SCHEMATIC OF A DATA TRANSMITTER.

ACKNOWLEDGEMENTS

The authors gratefully acknowledge the encouragement from Col. N. Pant, Director, I.S.R.O. Satellite Centre and Dr. S. P. Kosta, Dy. Director (Spacecraft Electronics Group) ISRO Satellite Centre and thank other colleagues for their valuable suggestions.

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1. Harmonic generation using step recovery diodes and SRD modules - HP application note 920.

2. Leveling loop senses current and sets gain by JIM CURTIS OCTOBER 1981, Microwaves.

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MANUFACTURER'S TOLERANCE: The manufacturer's tolerance specifies the maximum amount of deviation from the center frequency allowed by the manufacturer. The larger the manufacturer's tolerance, the better the yield of acceptable devices. A better yield generally means a lower price per component. A typical manufacturer's tolerance for a SAWR device is 200 ppm (parts per million).

TEMPERATURE DRIFT: Temperature drift is the total amount of frequency deviation from the center frequency over a specified temperature range. The amount of drift is determined by the temperature coefficient of delay and the turnover temperature. Both are related to the type of substrate used to make the device and the type of cut performed on the substrate.

Temperature Coefficient of Delay: Two different substrates are commonly used in SAW devices: quartz and lithium niobate. The temperature coefficient of delay for ST-X quartz is less than 3 ppm/deg C at room temperature. YZ-lithium niobate has a temperature coefficient of delay of 85 ppm/deg C. Since ST-X quartz has a smaller temperature coefficient of delay, it is more stable over temperature. Using lithium niobate as a substrate may require an oven for temperature stability.[5]

Turnover Temperature: The turnover temperature is that temperature where the frequency deviation is minimal. A graph of frequency deviation verses temperature with a turnover temperature at +25 deg C (room temperature) is shown in figure 1. The shape of the response is parabolic with the turnover temperature at the vertex. Notice that the frequency deviation due to temperature is negative.[6]

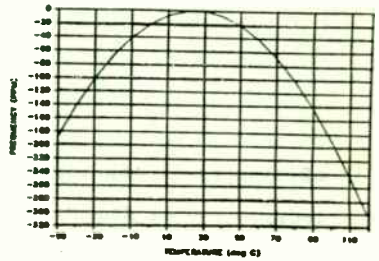

Fig. 1 Frequency vs. Temperature

For this discussion the temperature range of interest will be from 0 deg C to +70 deg C.

The turnover point of the parabola can be positioned anywhere between -25 deg C and +90 deg C.[7] The placement of this turnover point has a large affect on the amount of frequency deviation due to temperature. For example, if the turnover temperature is at +80 deg C, then the frequency deviation between 0 deg C and +70deg C is nearly linear as shown in figure 2. As temperature decreases, frequency decreases.

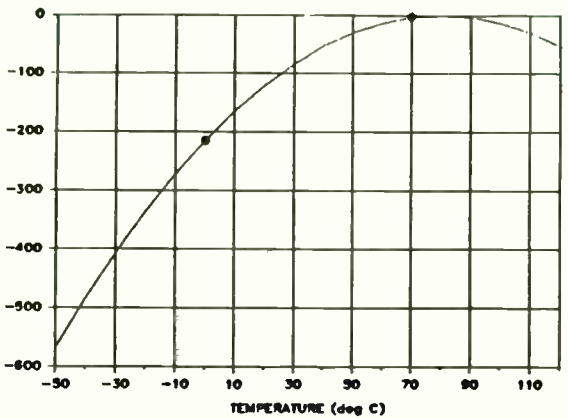

Fig. 2: Turnover Temp at +80 deg C

The amount of frequency deviation

TESTING OF NARROWBAND COMMUNICATIONS RECEIVERS - ACSB AND SSB

by

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This paper discusses the effects of adjacent channel, reciprocal mixing and intermodulation performance on narrowband Amplitude Compandored Sideband (ACSB) or Single Sideband (SSB) receivers. A test procedure will be given to evaluate this performance and the signal generator specifications will be discussed in relation to the above tests.

SPECTRUM EFFICIENCY

The Commercial Spectrum.

Over the last few years, the radio frequencies allocated to mobile radio have become very congested. Action now has to be taken to overcome these problems. In the larger metropolitan areas such as Los Angeles there are virtually no frequencies available. So what can be done? First of all, more frequencies can be released for the mobile radio users and this has been done by opening up the 800/900MHz band, primarily for cellular radio. Other action needs to be taken for such organizations as the police and fire departments, who must have secure radio channels.

The present systems employ FM in 20 KHz channels. This modulation system was implemented because of its superior fidelity, better signal to noise performance, and most important of all "hands-off operation". Unfortunately, a price was paid for this...spectrum inefficiency.

A new narrowband technology, for the commercial user, employing audio compandored single sideband techniques has now been approved. ACSB systems offer communications in a bandwidth significantly less than that used in FM systems. It can be shown that all the information from the human voice can be contained in the frequency range 300 Hz to 3.4 KHz. In fact, in SSB systems, intelligibility is still maintained with a high frequency cut off at 2.4 KHz. Research in the U.S. by Dr. Lusignon[1] and Dr. Fred Cleveland and in the U.K. by Professor W. Gosling and Dr. Joe McGeehan[2], showed that SSB could meet the needs of the VHF and UHF land mobile users. The FCC is now licensing ACSB radio systems with 5KHz channel spacing in an attempt to reduce the congestion.

Four new ACSB channels can be introduced where one FM channel previously resided. See Figure 1.

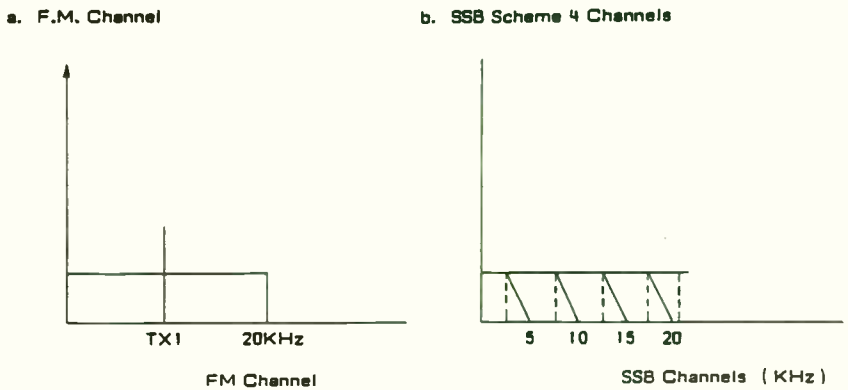


Figure 1

in parts per million due to a specific temperature is calculated using equation 1 shown below.

$$F\ (ppm) = \frac{(T-To)^2}{(Tc)^2} \qquad \text{<Equation 1>}$$

where F = Frequency deviation due to temperature in parts per million,
To = Turnover temperature in deg C,
Tc = Temperature coefficient in deg C^2 per parts per million [8],
T = Temperature of interest in deg C.[9]

For the situation shown in figure 2, the maximum amount of frequency deviation is

$$F\ (ppm) = \frac{(70 - 0)^2}{(5.45)^2}$$

$$= 165 \text{ ppm.}$$

Notice that the difference between the two extreme frequencies is substituted in for the quantity "T-To". This substitution is necessary because the turnover temperature is outside the desired temperature range.

The advantage in this example is that the frequency deviation is nearly linear with changes in temperature. This deviation is easily overcome by using a temperature compensating capacitor.

Now look at the example shown in figure 3. The turnover temperature is at +35 deg C which is right in the middle of the desired temperature range. As temperature decreases from the turnover temperature, frequency decreases. But as temperature increases from the turnover temperature, frequency again decreases.

In this example, either extreme temperature can be substituted into equation 1 for "T" since the turnover temperature is exactly in the center of the frequency range. The temperature deviation is

Fig 3: Turnover Temp at +35 deg C

$$F\ (ppm) = \frac{(70 - 35)^2}{(5.45)^2}$$

$$= 41 \text{ ppm.}$$

The advantage in this example is a low frequency deviation which can be handled within the pull range of the circuit.

AGING: Aging is the amount of frequency deviation from the desired frequency over a long period of time (years). This type of frequency change is a logarithmic function of time with most of the drift occurring in the first year.[10] For this reason, many manufacturers will only specify aging for the first year. A typical value for aging is 10 ppm/year maximum for the first year.

PHASE SHIFT: The amount of delay in degrees at the output

The Military Spectrum.

The military have used SSB at HF for many years, as it lends itself to better power efficiency, communications efficiency, security and reliability. Military systems have been developed to give the ultimate performance from both transmitter and receiver. Specifications for military equipment are more stringent than commercial. For instance, adjacent channel transmitters could be using as much as 1 KW of power while most commercial mobile radio transmitters may use only 10 watts. The military receiver, to handle such large signals, needs to have 20 dB better adjacent channel performance than the commercial equipment. See Table 1.

Table 1

Minimum FM STO As Defined by RS204C	TYPICAL FM MOBILE SPEC	MILITARY COMMUNICATIONS RECEIVER 2.7KHz B.W.	ACSB MOBILE SPEC
Usable Sensitivity 0.5µV	.5µV	<0.35µV	0.25µV
Adjacent Channel Selectivity >70 dB	75 dB	>90 dB	60 dB
Intermodulation (In Band) >60 dB	60 dB	>60 dB	N/S

FM v SSB

Figure 2 shows an FM spectrum of a carrier fc with 5 KHz of deviation (Δ f) and a maximum modulating frequency of 3.5 KHz. This results in a modulation index of approximately 1.4. The side frequency pairs can be calculated from Bessel functions. By inspection, the majority of the power is contained in the first two side frequencies resulting in a bandwidth of 14 KHz.

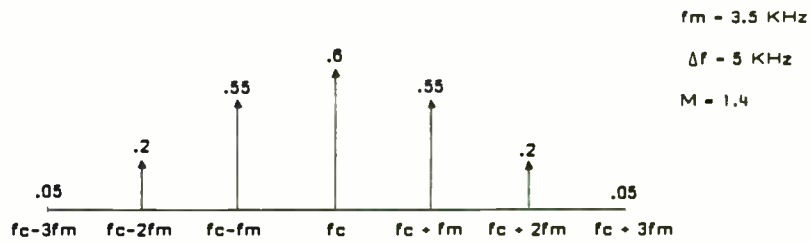


Fig 2 FM Spectrum of a carrier fc. deviation Δf and maximum modulating frequency fm.

Figure 3a shows an SSB spectrum. The carrier is reduced 60 dB below the speech sideband, (shown as an upper sideband.) The lower sideband is also reduced by at least 60 dB, resulting in the majority of the spectrum power being contained in a 2.2 KHz bandwidth.

of the device as referenced to some point (usually the input of the device) is the phase shift for the device. SAW resonators are built with either a 0 degrees phase shift or a 180 degrees phase shift (theoretically).

Phase shift for a SAWR can be specified two different ways. It can be specified at the SAW's resonant frequency or at some other frequency. The latter case is used when the circuit configuration requires a certain amount of phase shift at a particular frequency to operate. Then the phase is specified at that frequency instead of at the center frequency of the SAWR.

INSERTION LOSS: Insertion loss is the ratio of input power to output power, normally expressed in dB [11] and also related to Q.[12] If the insertion loss is high, the Q will be low and the device can be pulled farther from its resonant frequency. For a lower insertion loss, the Q will be higher and the device's pull range will be tighter. Typical insertion losses for SAW resonators range from 8 dB to 14 dB depending on the center frequency.

SPURIOUS REJECTION: Spurious rejection is a measurement of how far unwanted outputs in the frequency domain are suppressed.[13] Manufacturers usually avertise a minimum spurious rejection of 7 dB to 10 dB. Typical values are around 12 dB to 16 dB depending on the insertion loss and Q of the device.[14]

SAWR OSCILLATOR DESIGN CONSIDERATIONS

While designing a SAW resonator (SAWR) oscillator, several considerations should be kept in mind. The most important of these considerations is the way a SAWR is matched into a circuit. Oscillator stability, tuning range, and active device selection are all affected by the input and output matching networks.[15]

MATCHING IMPEDANCE: The bulk of the design effort is focused on the input and output matching elements. The matching elements must place the SAWR in the proper impedance environment, provide the additional phase shift necessary for oscillation, and tune the oscillator to the correct frequency.[16]

If the input and output matching networks present a low impedance to the SAWR device, the loaded Q of the SAWR would be relatively high, the insertion loss would be high and the tuning range for the oscillator circuit would be quite narrow. The high insertion loss requires an active device with a high amount of gain to sustain oscillation. The high loaded Q causes the SAWR device to dominate control of the circuit's frequency whereas other oscillator components have little affect. Because of the SAWR's tight control, the best possible phase noise performance is achieved.[17]

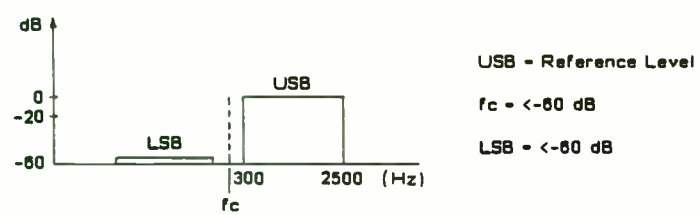
If the matching networks present a high impedance to the SAWR device, the opposite happens. The loaded Q and the insertion loss would be relatively low, and the tuning range

Figure 3b shows an ACSB spectrum with a slightly greater bandwidth due to the 3.1 KHz tone above band (TAB). Other ACSB methods have been proposed with tones in band (TIB) From the above examples, the spectrum efficiency of SSB is clear.

After reducing the bandwidth and implementing essentially an AM scheme particular attention must be paid to performance. In fact, the same performance as was achieved in the FM system should be aimed for.

Originally adjacent FM channels were geographically spaced to reduce the chances of adjacent channel inteference. This luxury can no longer be afforded because of spectrum congestion. The same will apply to an SSB or ACSB system, and with channels only 5 KHz apart particular attention must be paid to transmitter and receiver performance.

a. SSB Spectrum



b. ACSB Spectrum

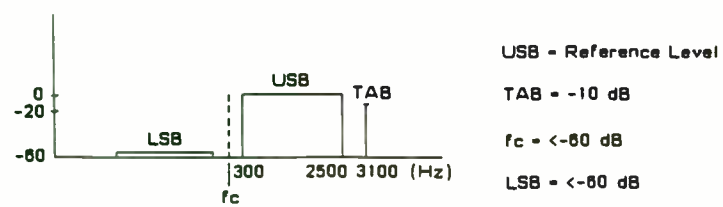


Figure 3

RECEIVER TESTING

Emphasis has already been placed on spectrum conservation by the use of SSB schemes. Correct alignment of the transmitters is, therefore, always paramount. Non-linearity in an SSB transmitter produces the same effect as over-deviation in an FM transmitter.....gross spectrum abuse. Assuming that the transmitters are correctly aligned, receiver performance must be assessed with the equivalent of a good clean radio transmitter. Consideration must, therefore, be given to the signal generator. A phase noise spec 20 KHz from carrier, good enough for present FM channel spacing, is no longer acceptable. Equal performance 5 KHz from carrier must now be sought. As will be shown later, far more stringent tests such as reciprocal mixing on narrowband CW military receivers necessitates low phase noise even closer than 5 KHz. Generator specifications relevant to the test in question will be highlighted.

ON CHANNEL TESTS

The most important of these tests, that of sensitivity will be discussed briefly. The sensitivity of the receiver must be established before proceeding to discover how strong off channel signals affect this performance.

Referring to Table 1 the performance for the SSB communications receiver for a 10 dB (S+N)/N ratio is 0.35 microvolt (-117dBm) or better. To test for this performance, a single tone only is needed. (Unlike the AM or FM receiver, the carrier is of no value.)

would be wider. A lower insertion loss does not require an active device with a high amount of gain to sustain oscillation. Because of a lower loaded Q, variations in the other oscillator components have a noticable affect on the operating frequency. Phase noise performance degrades slightly.[18]

TUNING ADJUSTMENT: Fine tuning of the SAWR oscillator should be limited to one adjustable component.[19]

MAXIMUM POWER: A good rule of thumb is to limit the power dissipated in the SAWR device to 20 milliwatts. Larger amounts of power cause strong vibrations to occur inside the SAWR that will eventually tear the aluminum transducers from the substrate. Once this separation occurs, the device is ruined.[20]

DC CURRENT: For best reliability, DC (direct current) should be kept off the SAWR device. The SAWR will operate with DC running through it but reliability degrades.[21]

PULL RANGE: The pull or tuning range is determined by the SAWR's characteristics and by the circuit's requirements. Depending on how wide a pull range is needed determines whether matching networks present a high or low impedance to the SAWR.

The oscillator circuit handles the pull range in two different ways. A course adjustment compensates for the manufacturer's tolerance by pulling the SAWR onto the desired frequency when the circuit is first built. A fine adjustment compensates for frequency drift due to temperature changes and aging over time.

If the frequency drift due to temperature is 100 ppm and the overall aging of the SAWR device is 30 ppm, then the minimum amount of fine tuning needed is 130 ppm. If the oscillator is designed for a pull range (fine tune) of 160 ppm to 200 ppm, then the circuit is guaranteed to satisfy the pull range requirement.

PHASE NOISE: Phase noise performance degrades as the deviation from the SAWR's resonant frequency increases. Figure 4 is a plot of phase noise measured 10 Khz away from the operating (carrier) frequency versus the distance between the operating frequency and the SAWR's resonate frequency of a 674 Mhz oscillator. The data for this plot is shown in Table 1.

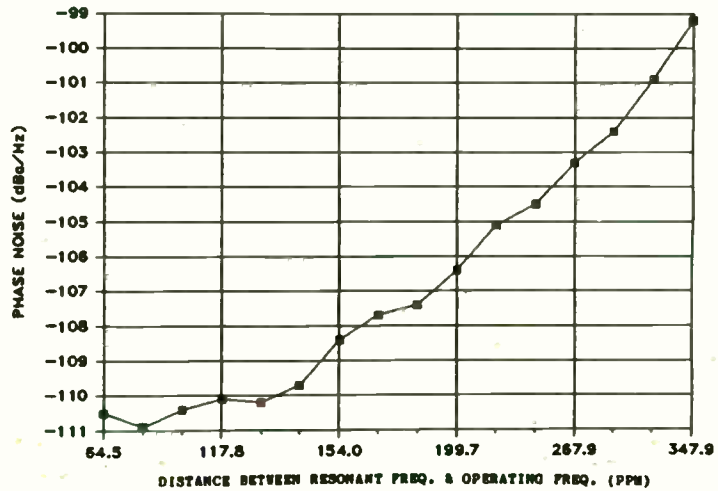


Fig. 4: Phase Noise Degradation Plot for 674Mhz Oscillator

USABLE SENSITIVITY

TEST SETUP

TEST PROCEDURE

1. Connect audio load and AC voltmeter to receiver under test.
2. Set generator RF to produce a 1 KHz (±100 Hz) beat note. Use manual RF gain, if available.
   (N.B. no modulation is needed on generator.)
3. Set generator output for approximately 1 millivolt and adjust volume for 25% of maximum rated output.
4. Reduce RF level until ratio of audio output, between signal on and off conditions is 10 dB.
5. The signal level to achieve the condition in 4, is the usable sensitivity.

Arguments have been raised over the definition of "usable sensitivity". This test procedure uses the 10 dB S/N standard as it was originally defined by EIA. However, the

paper given by Jim Eaglesen at the 1985 RF Expo defines "usable sensitivity" more accurately.

M.D.S. (Minimum Discernable Signal) is the level where the signal is just detectable. Representing 0 dB SNR, this can only be used for theoretical calculations. SNR (Signal to Noise Ratio) is the level at which a signal just becomes useful. Most manufacturers specify 10 dB SNR.

Other on channel tests are 1) AGC - determines the ability of the receiver to mantain constant audio output level with varying RF innput levels; 2) A.G.C. time constant. Fast attack times need to be used at VHF to optimize the receiver during fast fade conditions as would be experienced under mobile operation; 3) Spurious performance. Not a true on-channel test, but requires only one input signal. This is the ability of the receiver to prevent single unwanted signals from causing an unwanted response at the output of the receiver, normally caused by discrete spurii from the synthesizer mixing with other signals.

SIGNAL GENERATOR PERFORMANCE

For sensitivity testing, the most important aspect of the generator is output level accuracy. As well as the absolute accuracy specification, typically ±1 dB at -120 dBm, attention must be made to VSWR. Most modern wideband receiver front ends have VSWRs approaching 2:1 and with signal generator VSWRs of 1.5:1, errors as great as 4 dB can

be experienced at the antenna input of the receiver.

The worst case phase noise situation occurs when the device is at one of the extreme ends of the manufacturer's tolerance. To determine this point (in ppm), add together the manufacturer's tolerance, temperature drift, and aging. If the manufacturer's tolerance is 200 ppm, temperature drift 100 ppm, and overall aging 30 ppm, the worst case phase noise would occur 330 ppm away from the SAWR's resonate frequency.

AFC VOLTAGE (volts)	DELTA FREQ. (Khz)	FREQ FROM RESONATOR FREQ. (PPM)	PHASE NOISE (dBc/Hz)
0.0	15.0	64.5	-110.5
1.0	11.8	86.8	-110.9
2.0	9.1	104.3	-110.4
3.0	8.4	117.8	-110.1
4.0	7.7	130.3	-110.2
5.0	8.3	141.7	-109.7
6.0	8.9	154.0	-108.4
7.0	4.9	167.2	-107.7
8.0	12.1	181.7	-107.4
9.0	14.4	199.7	-106.4
10.0	15.1	221.4	-105.1
11.0	16.3	243.8	-104.5
12.0	17.2	267.9	-103.3
13.0	18.5	293.5	-102.4
14.0	18.2	320.9	-100.9
15.0	18.0	347.9	-99.2

Table 1: Measured Data Taken on the 674Mhz Oscillator

SAWR OSCILLATOR DESIGNS

Two different circuit configurations are discussed along with their advantages and disadvantages. The problems encountered during the design of the second circuit are also mentioned.

SAWR OSCILLATOR DESIGN #1

The circuit shown in figure 5 is designed using a 674 MHz SAW Resonator.

ADVANTAGES:

1. This design contains no tuning coils which could cause microphonics.

2. The number of parts in this circuit is kept to a minimum. Fewer parts means better reliability.

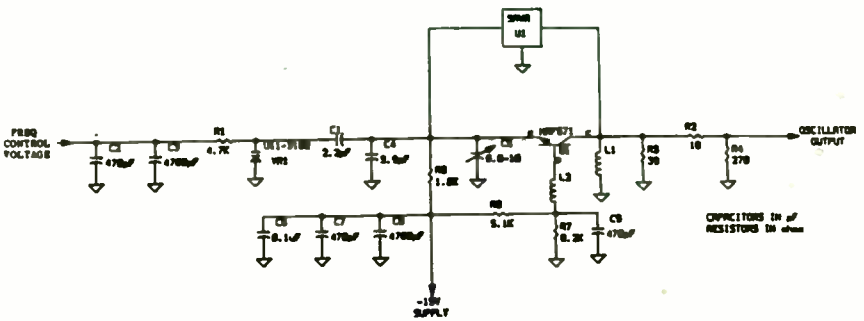


Fig. 5: Ckt Configuration for Design #1

DISADVANTAGES:

1. DC is allowed to run through the SAWR. This condition reduces the reliability of the device.

2. The circuit only oscillates on one side of the SAWR's resonant frequency.

3. If the oscillator is pulled too close to the SAWR's resonant frequency, the circuit experiences a phase reversal and "jumps" to another frequency.

4. The phase noise performance of this circuit is not as good as a circuit that can pull its operating frequency through the SAWR's resonant frequency.

In order to prevent the oscillator from jumping to another frequency, a safety region between the SAWR's resonant frequency

OFF CHANNEL TESTS

ADJACENT CHANNEL PERFORMANCE

This is a measure of the receiver's ability to differentiate between a desired signal (on-channel) and signals on adjacent channels. It is primarily a function of the IF filter response and could also be called a selectivity test. Some test methods do not use an on-channel signal generator and rely on the increase in noise level caused by a high level signal off-channel, this does not test for the true operating conditions. At 5 KHz offsets, as found in SSB receivers, reciprocal mixing tends to mask the selectivity performance.

SIGNAL GENERATOR PERFORMANCE

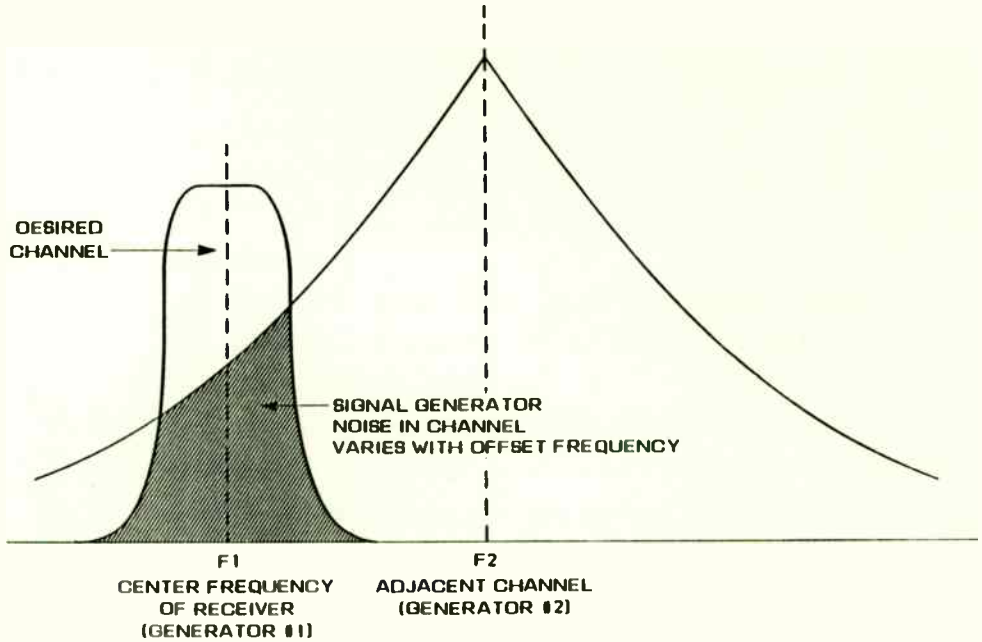
Care must be taken with the adjacent channel test to ensure that the phase noise of the off channel signal generator does not hide the true adjacent channel performance of the receiver. See figure 4. To establish if a signal generator will meet these requirements, the following facts are needed.

1. What is the adjacent channel offset on the receiver to be tested?
2. What is the IF bandwidth of the receiver?
3. What is the specified adjacent channel performance?

Inserting some typical figures for an SSB receiver, the results are as follows:

1. Adjacent channel offset = 5 KHz
2. IF Bandwidth = 2.7 KHz
3. Adjacent channel spec = 80 dB

IMPORTANCE OF SIGNAL GENERATOR PHASE NOISE IN ADJACENT CHANNEL TESTS



TYPICAL REQUIREMENTS:

For 5 KHz channel spacing phase noise should be at least -130 to -140 dBc/Hz for selectivity measurements of 90 dB and suprious signals should be down greater than 90 dB.

Figure 4

and the frequency determined by the tuning voltage is established. Through experimentation, a safety region of 100ppm was found to be satisfactory.

SAWR OSCILLATOR DESIGN #2

A different oscillator configuration is shown in figure 6. This design uses an 848 MHz SAW resonator.

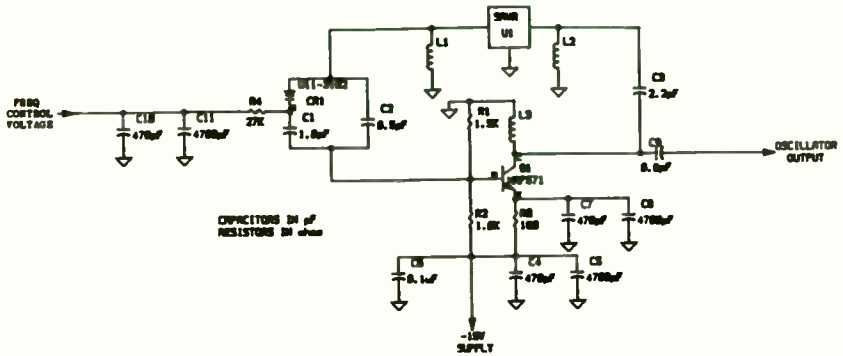


Fig. 6: Ckt Configuration for Design #2

CIRCUIT DESCRIPTION: The biasing network, resistors R1, R2 and R3, set up the necessary conditions for the MRF571 transistor. Note the use of a negative supply. This transistor is a high gain, low noise device with a transitional frequency of 8.0 Ghz at 50 mA.[22] Capacitors C7 and C8 provide an AC ground to the emitter of the transistor.

L3 is a RF choke which prevents the RF signal from shunting to ground.

The frequency control voltage is placed between capacitor C1 and varactor diode VR1. VR1 is a U11-3102 varactor diode; a part specially made for Watkins-Johnson Company. Its capacitance changes as the voltage is varied.

The input matching network consists of capacitors C1 and C2, varactor diode VR1, and inductor L1. The output matching network consists of capacitor C3 and inductor L2.

The course tune adjustment is done by varing inductors L1 and L2. This adjustment is very critical because it largely affects the circuit's pull range and amplitude response.

The fine tune adjustment is done by adjusting the frequency control voltage. The varactor diode VR1 together with capacitors C1 and C2 changes the amount of capacitance seen by the SAWR in the input matching network. This change pulls the SAWR through the circuit's tuning range.

PHASE NOISE: The single side-band phase noise performance of the 848 Mhz SAWR oscillator (free-running) is shown in figure 7.

Notice that the offset from the carrier in figure 7 is only shown up to 1.7 Khz. Beyond this offset, the oscillator's phase noise performance approached the limit of the test equipment.

The phase noise performance of the 848 Mhz oscillator at an offset of 10 Khz is about -118 dBc/Hz.[23]

The signal generator noise is specified in a 1 Hz bandwidth, but the measurement is made in the receiver's 2.7 KHz IF bandwidth. To find the difference, in dB, use the formula: 10 log IF bandwidth/1 Hz.

For 2.7 KHz, the result is 34 dB.

The required signal generator noise spec can now be calculated at a 5 KHz offset, using the formula: - receiver spec + bandwidth conversion (as above) + 10 dB measurement margin.

From the example; 80 dB + 34 dB + 10 dB

= 124dB below carrier.

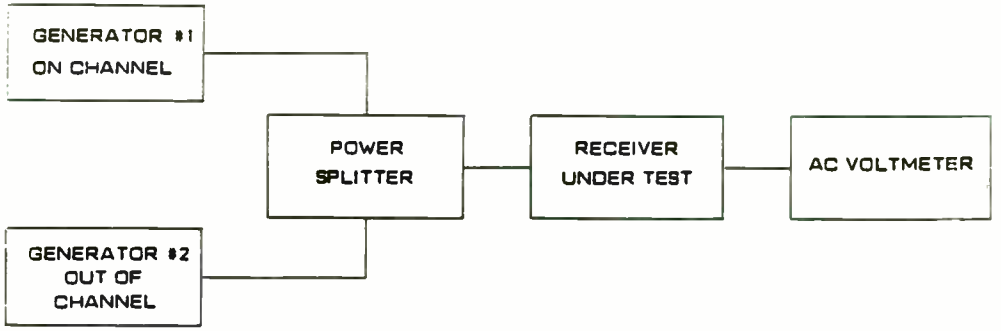
Table 2 gives the required signal generator phase noise performance against narrowband communication bandwidths and their typical 80dB measurement points. To determine how much better than the 80 dB adjacent channel spec a receiver is, even greater performance is needed from the signal generator. For example, 90 dB adjacent channel performance requires a phase noise spec of -134dBc, at a 5 KHz offset.

Table 2

Signal generator PHASE NOISE in dBc needed to measure 80dB adjacent channel performance on receivers with the following common bandwidths.

① 1 Receiver Bandwidth	② Mode	③ Equivalent Noise Bandwidth	④ 80dB Filter Response	⑤ 2 Signal Generator Performance at the offset in column 4
400 Hz	C.W.	26 dB	1500 Hz	-116 dBc
1200	RTTY	31 dB	4000 Hz	-121 dBc
2700	SSB	34 dB	5000 Hz	-124 dBc
6800	AM	38 dB	15000 Hz	-128 dBc

ADJACENT CHANNEL TEST



TEST PROCEDURE

1. Turn generator number 2 off, set generator number 1 to the receiver frequency +1 KHz. Obtain the condition for usable sensitivity, i.e. 10 dB S/N.
2. Increase the level of the wanted input signal by 3 dB.
3. Turn generator number 2 on and tune it 5 KHz away from generator 1.
4. Increase level of generator number 2 until the S/N ratio falls back to 10 dB.
5. The ratio of the unwanted signal measured in Step 4 to the reference sensitivity is the adjacent channel performance.

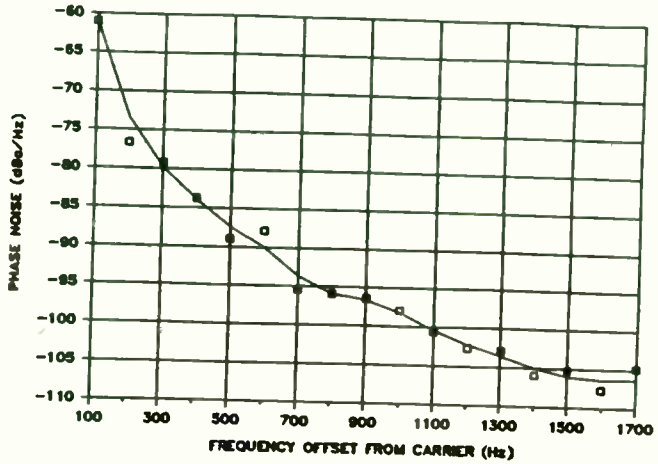


Fig. 7: Frequency vs Phase Noise Plot for an 848Mhz Oscillator

ADVANTAGES:

1. The operating frequency can be pulled through the SAWR's resonant frequency. This feature allows the best possible phase noise response to occur.

2. There is no DC running through the SAWR device.

3. Stray capacitance is tuned out by adjusting inductors L1 and L2.

4. This circuit is very reproducible.

DISADVANTAGES:

1. More components are needed to build this design. The greater number of components reduces the circuit's reliability.

2. The values of the matching network's components are very critical. Small variations in these values have a great affect on the oscillator's performance.

DETERMINING THE MATCHING NETWORK VALUES: The actual values for the matching networks depend on the circuit lay-out. After the circuit is designed and laid out on a PC board, replace matching capacitors C1, C2 and C3 with adjustable capacitors set at the designed values. Once the circuit's performance is satisfactory, replace the adjustable capacitors one at a time with fixed capacitors; rechecking the circuit's performance after each substitution.

Coupling capacitor C9 may also have to be adjustable (initially) since it influences the output matching network.

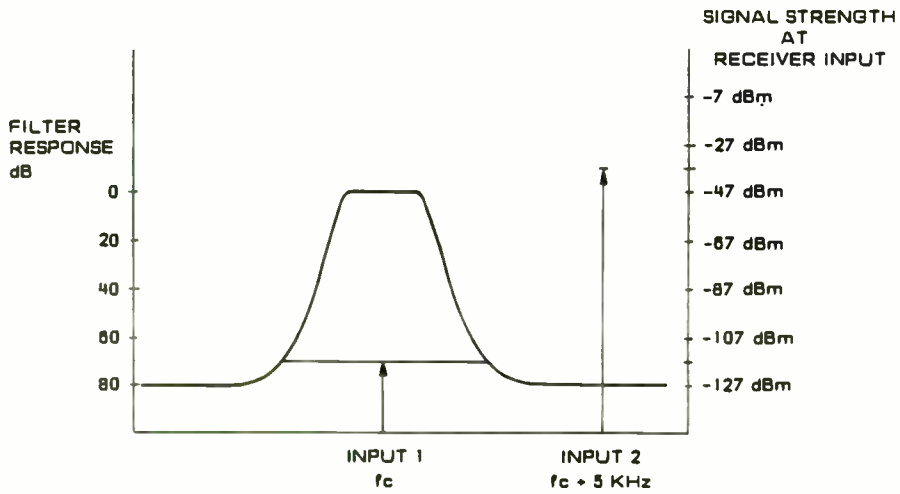
The matching inductors are refined in the same manner.

If the circuit does not oscillate, use a network analyzer in the feedback path to determine the amount of gain and phase in the loop. Be sure to zero out the cable effects before connecting the network analyzer to the oscillator circuit. Adjust the matching components until the network analyzer displays a 0 degrees phase shift and a magnitude greater than 0 dB which represents gain in the loop.

Disconnect the network analyzer and close the feedback loop in the oscillator circuit. Minor adjustments on the matching component values may be necessary to cause the circuit to oscillate.

ADJACENT CHANNEL TEST

FIGURE 5



The input to an IF filter consists of two signals, the wanted signal equivalent to -117 dBm at the antenna input and a strong -27 dBm signal 5 KHz higher. The filter offers 80 dB attenuation at a 5 KHz offset, reducing input 2 to a level of -117 dBm at the output of the filter. The adjacent channel signal will now be at the same level as the wanted signal and will continue through the rest of the receiver, interfering with the wanted signal.

RECIPROCAL MIXING PERFORMANCE

Reciprocal mixing is caused by phase noise imperfections on the receiver's local oscillator. Normally the strong local oscillator signal is mixed with a weak wanted signal to produce the IF signal. However, the mixer will perform the same for any other pair of signals separated by the IF. Reciprocal mixing is so named because the role of local oscillator and signal are reversed; a strong unwanted signal off-frequency mixes with the weaker phase noise of the local oscillator. As an example, when a strong signal 5 KHz from the receive frequency mixes with the phase noise 5 KHz from the center of the local oscillator, the result is an IF output with noise proportional to the local oscillator phase noise. See Figure 6. Until the emergence of synthesized local oscillators, with their less than perfect noise sidebands, reciprocal mixing went unrecognized. Crystal oscillators, used at VHF and UHF for frequency stability, had far better noise performance, and reciprocal mixing was well below the adjacent channel performance.

Reciprocal mixing and adjacent channel performance are very closely related. The ultimate performance of the IF filter can never be realized if the receiver local oscillator is noisy.

SIGNAL GENERATOR PERFORMANCE

The close to carrier noise performance of the generator must be at least as good as that for adjacent channel tests. If a measure of the reciever local oscillator phase noise is required, refer to Table 2.

Using the network analyzer prevents a lot of guess work by allowing the engineer to see the effects on amplitude and phase as a component's value increases or decreases.

PROBLEMS ENCOUNTERED: A few problems occurred during the testing of several oscillator circuits. They are mentioned here along with their solutions.

Squegging: Squegging is the oscillator's operating frequency modulated by a low frequency signal. The result is a mass of spurious signals. This squegging problem is solved by bypassing the transistor in such a way that the gain at low frequencies is reduced.

Matching: As mentioned earlier, the values of the matching components are very critical. If the circuit is mismatched, several different problems can occur. These problems are mentioned in the following paragraphs.

Jumping: The phase response around the center frequency of a SAWR is not always linear. The steeper the slope of the phase, the greater the frequency change is per volt. As the voltage changes, the SAWR's phase may pull through one of these nonlinear points and cause a greater frequency change to occur. This frequency change appears as a "jump" in frequency. The size of the jump depends on how much of the phase response has the steeper slope.

The jumping may not always occur at the same operating frequency or control voltage. For example, take a 674 Mhz oscillator with a SAWR resonate frequency at 674.0281 Mhz. As the frequency control voltage is decreased, the operating frequency jumps from 674.0634 Mhz to 633.8751 Mhz (a difference of roughly 40 Mhz). Upon increasing the control voltage, the operating frequency doesn't jump until it reaches 657.297 Mhz. Then it jumps to 674.205 Mhz (a difference of about 17 Mhz).

The matching networks can prevent jumping from occurring by presenting a high impedance to the SAWR device. Figure 8 shows a plot of frequency versus voltage of the same 674 Mhz oscillator (mentioned earlier) after its matching networks were changed to present the SAWR with a higher impedance. The data for this plot is shown in table 1 (page 11).

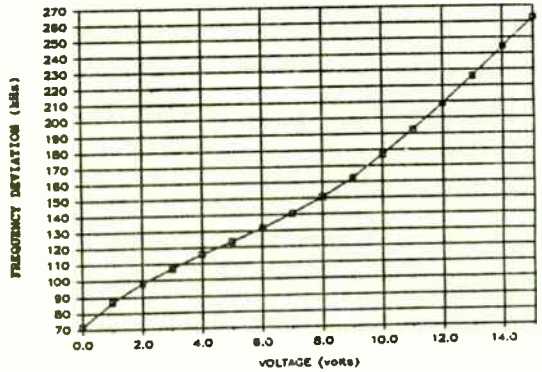
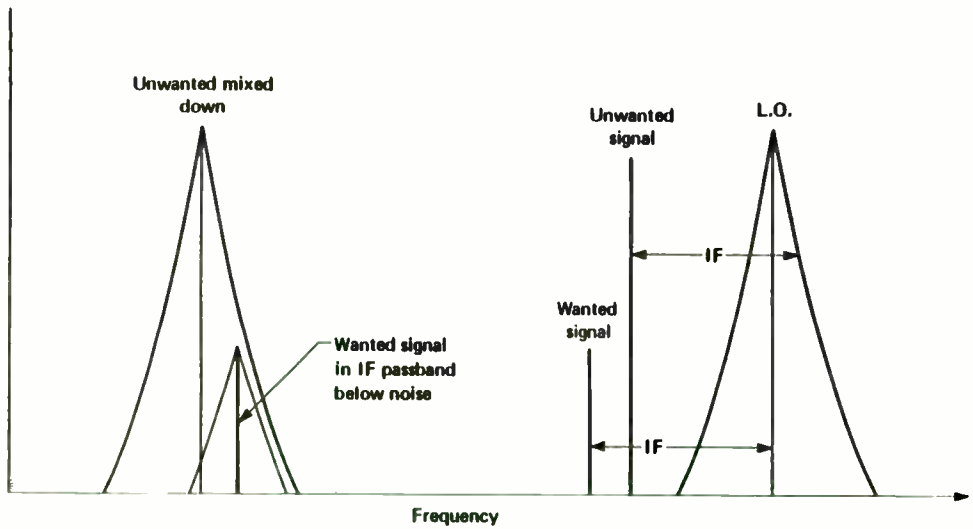


Fig. 8: Frequency Deviation vs AFC Voltage Plot for 674Mhz Oscillator

Notice that the frequency change from 13 volts to 14 volts



RECIPROCAL MIXING
Figure 6

RECIPROCAL MIXING TEST

TEST PROCEDURE

1. Tune the signal generator to the offset of interest.
2. Monitor the AF output level noise with no input to the receiver.
3. Increase the signal generator until a 3dB increase in noise at the AC voltmeter is observed.
4. Note the level obtained in 3 and add this to the noise floor of the receiver. Note: the noise floor is 10dB lower than the usable sensitivity figure. Refer to Fig. 6 and table 3.

This test should be repeated at different offsets to establish the phase noise of the oscillator and therefore, the ultimate adjacent channel performance.

Table 3

① Frequency Offset	② Input Level	③ Level with Respect to -127 dBm Noise Floor in 2.7 KHz BW	④ Receiver Oscillator Phase Noise in a 1 Hz BW
5 KHz	-55 dBm	72 dB	-106 dBc
10 KHz	-47 dBm	80 dB	-114 dBc
20 KHz	-38 dBm	89 dB	-123 dBc
100 KHz	-19 dBm	108 dB	-142 dBc

is larger than the frequency change from 6 volts to 7 volts. If this frequency change (between 13 volts and 14 volts) were even greater, it could appear as a jump in the frequency range.

Amplitude Variations: Sometimes the amplitude of the operating frequency varies over the tuning range of the circuit. For example, a 672 Mhz oscillator has a pull range of 89 Khz and an amplitude variation of 21.6 dB. After adjusting the values of the matching elements, the oscillator has a pull range of 313 Khz and an amplitude variation of 11.2 dB. Further adjustments on the matching components produce a tuning range of 122 Khz and an amplitude variation of 0.9 dB.

Frequency Range Variations: As seen from the previous example, the matching components have an effect on the tuning range of the oscillator circuit as well as the amplitude response. If the matching networks present a high impedance to the SAWR, the tuning range of the oscillator circuit will increase.

Loop-back in Tuning Range: Normally, as the control voltage increases, the frequency increases. In a loop-back situation, the frequency begins increasing as the control voltage increases but then it "loops-back" and starts to decrease. This situation is extremely undesirable because it can causes a phase-locked loop to be driven to limits in one direction, and the oscillator will never lock onto the correct frequency.

The solution to these problems is to adjust the matching components. The matching coils, L1 and L2, are the easiest to adjust.

CONCLUSION

The type of SAW device used in an oscillator design depends on the requirements of the application. For fixed frequency applications, a SAW resonator is recommended. Once the device is selected, careful consideration is given to its characteristics. Center frequency and turnover temperature are two of these characteristics that affect the way the oscillator circuit is designed.

The most difficult part of designing any SAWR oscillator is finding the appropriate matching component values. Once these values are determined, the oscillator demonstrates an excellent phase noise response, an adequate tuning range, and a minimum amount of amplitude variation.

ENDNOTES

[1] Handbook of Acoustic Signal Processing (Andersen Laboratories, 1984) Vol. IV, pp.12-13.

[2] C.K. Campbell, Surface Acoustic Wave Devices and Their Signal Processing Applications (The George Washington University, Continuing Engineering Education, 1985), p. 9.22.

[3] Robert J. Kansy, Introducing the Quartz Surface Acoustic Wave Resonator (Application Note: No. 1, RF Monolithics, Inc.), p. 1.

[4] Handbook of Acoustic Signal Processing, p. 8.

INTERMODULATION PERFORMANCE

In the strong signal environment of large metropolitan cities or where many transmitters are operational at the same time and geographically close, it is not just adjacent channel performance that is critical. Two strong signals spaced at some distance from the adjacent channel, yet within the bandwidth of the roofing filter, can mix in the front end of the receiver and produce intermodoulation products that fall in the IF passband. This test is a measure of the capability of a receiver to inhibit the generation of such in band signals.

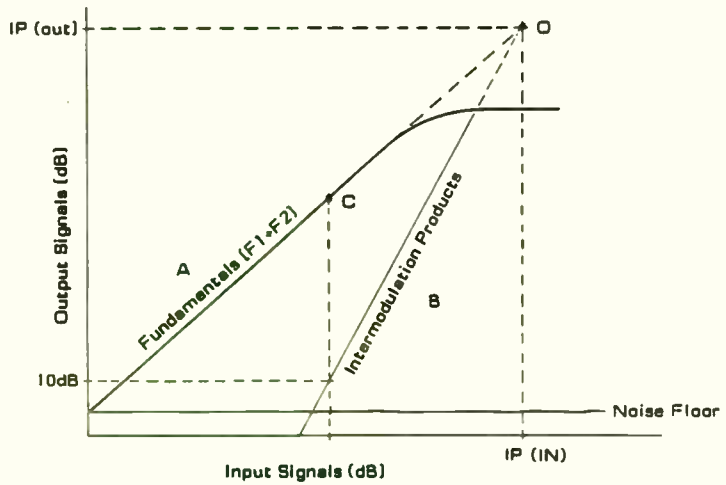
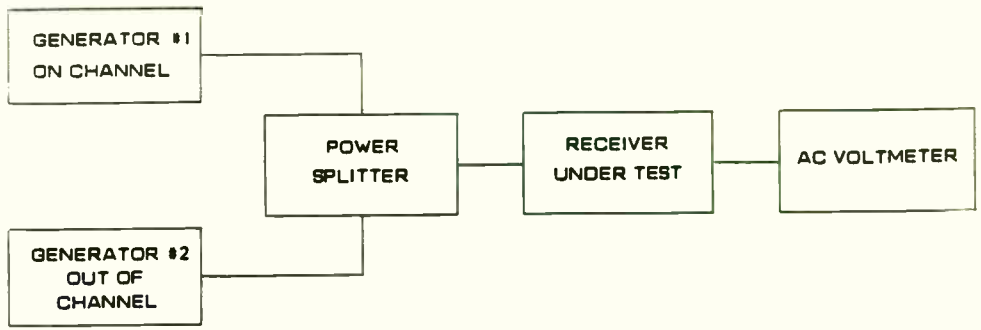


Figure 8

INTERMODULATION TEST



TEST PROCEDURE (3RD ORDER)

1. Set generator number 1 to fc + 20KHz.
2. Set generator number 2 to fc + 39KHz.
3. Increase the outputs of the two generators, keeping the amplitudes the same, until the receiver produces a 10 dB S/N.
4. The difference in level between the usable sensitivity (10 dB S/N) and the outputs of the generators to obtain the condition 3 is the intermodulation performance of the receiver.

The above relationship is more often specified as a 3rd order intercept point (I P). This can best be explained by reference to the figure.

Curve A (Figure 8) represents the signal level of one of the two fundamental signals. These signals are increased above the noise floor until a point is reached (c) where the 3rd order intermodulation product (IMP) starts to emerge from

[5] Campbell, pp. 1.6-1.8.

[6] Handbook of Acoustic Signal Processing, p. 9.

[7] Resonators & Oscillators (Brochure, Crystal Technology).

[8] The temperature coefficient, Tc, varies from manufacturer to manufacturer. For discussion purposes only, 5.45 will be used as the temperature coefficient.

[9] Equation obtained through a telephone conversation with Sawtek Incorporated.

[10] Data sheet for 180 deg quartz SAW resonator (RF Monolithics, Inc., 1984).

[11] Handbook of Acoustic Signal Processing, p. 16.

[12] Q is defined as the center frequency divided by the bandwidth (usually the 3 dB bandwidth).

[13] Handbook of Acoustic Signal Processing, p. 10.

[14] Based on data sheets obtained from Sawtek, Incorp.

[15] Frank Perkins, Jr., Designing UHF SAW Resonator Oscillator (Application Note: No. 4, RF Monolithics, Inc., 1983), p. 1.

[16] Perkins, pp. 1-2.

[17] Perkins, p. 3.

[18] Perkins, p. 3.

[19] Perkins, p. 3.

[20] Information obtained through a classroom discussion with Dr. C. K. Campbell at the George Washington University.

[21] 1GHz SAW Resonator -Application Note (Handwritten, Stantel Corp., 22 Mar 85).

[22] Motorola RF Device Data (Motorola, Inc., 1983), pp. 6-149 to 6-161.

[23] Extrapolated using data taken from a 1 KHz offset.

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1. Campbell, C. K., Ph.D., D.Sc., F.R.S.C., Surface Acoustic Wave Devices and Their Signal Processing Applications, Washington, DC, The George Washington University School of Engineering and Applied Science, 1985.

2. Handbook of Acoustic Signal Processing, Andersen Labs, 1984, Vol. IV.

3. Kansy, Robert J., Introducing the Quartz Surface Acoustic Wave Resonator (Application Note: No. 1), RFMonolithics, Inc., 1983.

4. Motorola RF Device Data, Motorola, Inc., 1983, pp. 6-149 to 6-161.

5. Perkins, Frank, Jr., Designing UHF SAW Resonator Oscillators (Application Note: No. 4), RFMonolithics, Inc., 1983.

6. Resonators & Oscillators, Crystal Technology.

7. RFM data sheet for 180 degrees Quartz SAW Resonator, RFMonolithics, Inc., 1983.

8. 1 Ghz SAW Resonator -Application Note (Handwritten), STANTEL Corp., 22 Mar 1985.

the receiver noise. When the IMP is 10 dB above the noise floor, it is at the same level as the usable sensitivity. The difference in this level and the fundamental is the value found in 4 of the test procedure. As the fundamental amplitude is increased, so does the IMP, at a rate three times faster. At the theoretical point D on the graph, the IMP and the fundamental meet. (This is theoretical as the input amplifier of the receiver will go into gain compression well before this point). Point D is the 3rd order intercept point. (IP) It can be referred to input or output. The input intercept differs from the output intercept by the small signal power gain of the stage in question. For a more comprehensive study of intermodulation refer to 3,4.

CONCLUSION

Techniques for testing receivers have not changed significantly over the last 10 years. The introduction of synthesized signal generators in the 1970's by companies such as Racal and Hewlett Packard were a major step forward. Until then, at VHF and UHF, signal generators had to be left on permanently, to ensure they were stable enough to test the crystal controlled receivers. The synthesized signal generator manufacturers were already specifying noise performance capable of handling today's 20 KHz spacings. History is now repeating itself. Todays communication systems are poised on the edge of a technology breakthrough, but the signal generators available are only able to handle the 20 KHz technology. SSB systems have been around for many years and now are becoming very popular in the commercial field. As in the 50's and 60's the test equipment presently available for such systems testing is not ideal. Racal-Dana and Hewlett Packard again lead the way with their models 9087 and 8662A. The military have actually progressed to even higher technology systems that implement frequency agile and spread spectrum techniques.

Anyone considering measuring todays communications systems must not forget the future; nor should the instrument manufacturers. Signal generators are now needed with good noise performance for narrowband systems, fast switching speed for frequency agile systems and digital modulation capability for spread spectrum.

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SIMPLE APPROACHES TO LIMITING RADIATION FROM FOIL-SHIELDED COMPUTER CABLES

by

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Electromagnetic (EM) susceptibility has typically been a difficult problem in the development of high-reliability communication, navigation, and electronic warfare equipment. The military susceptibility standard, MIL-STD-461B, outlines most government electromagnetic interference (EMI) requirements. This document is augmented by MIL-STD-462 which describes acceptable testing procedures.

Military EMI requirements can be ten times more stringent than commercial standards. These military requirements result from two prime factors. The first is that, in a typical military communications center, the equipment is installed close together creating a worse-than-normal EM environment. The second is to assure reasonable equipment immunity to a potential hostile environment due to electronic countermeasures.

Besides having to meet the more familiar EMI standards, many of these equipment must also comply with TEMPEST requirements. The TEMPEST requirements are part of a classified U. S. government security program. They deal with controlling the emission and detection of energy from communication and data processing equipment which could reveal classified information being processed by the equipment. All too often, TEMPEST guidelines for equipment installation and interconnection (part of this control of emissions) are considered adverse to typical installation criteria.

MIL-HDBK-419, although not a TEMPEST specification, contains equipment and cable shield grounding recommendations which are highly compatible with the TEMPEST guidelines and represents a more modern approach to facility design. This document clearly states that the only differences in grounding techniques between those employed at facilities processing National Security related information (RED equipments) and any other facility are the grounding configurations used to

Monolithic RF Amplifiers for Hybrid Applications

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Monolithic Gallium Arsenide ICs for RF systems have held promise for many years. Yet there has only been a modest list of product offerings of basic functions with relatively high device costs. Using these basic components has implied even higher costs associated with system insertion due to the need for external components and circuitry. This was particularly true of early transistor amplifier products that required extensive bias circuitry or decoupling components to operate. The real promise of integrated circuitry lies in reducing the number of components to minimize assembly costs and unit-to-unit variations while improving reliability and overall system performance.

GaAs Technology has now reached the level of maturity where more complex functions can be integrated onto single analog or digital ICs. With recent advances in the sophistication of technology in materials, processing, design and test, a growing number of firms are capable of designing and building GaAs ICs. Foundry, design, and test services are now widely offered. Yet standard product offerings, addressing high volume "generic" applications, have been slow to emerge. Harris Microwave Semiconductor has introduced its first two products in a line of GaAs RF ICs for receiver/transmitter and signal processing applications. These are broadband amplifiers chips covering 500 MHz to 5.0 GHz and providing general purpose gain. The HMR-10503 is a fully integrated amplifier requiring no external circuitry other than bond wires to connect the RF input , RF output, +Vdd and DC/Signal ground. The companion HMR-10502 is identical except

terminate cable shields. These configurations are applicable when the equipment involved is referenced to an equipotential ground plane. (MIL-HDBK-419 defines and describes the equipotential ground plane.)

Although the majority of MIL-HDBK-419 deals with design considerations for new facilities, implementation of recommended installation techniques in existing facilities is also described. Concerning the ground systems installed in most existing facilities, this standard states,

"... While these systems generally do not meet today's standards and requirements, they will continue to be in use for many years at existing facilities. Information on and description of these systems is therefore included for maintenance purposes only . . . . Any major building or facility rehabilitation should include upgrade of the grounding system to include use of the equipotential plane . . . . "

Relating cable shield grounding configurations to the use of a facility equipotential ground plane is fundamental to reducing EM radiation from interface cabling. With this concept in mind, a test setup was designed to study what standard approaches to EM radiation reduction could easily be implemented at older communication facilities.

The test configuration was developed with the intent of establishing a controlled, easily varied test setup. The approach chosen was to enclose each a line driver unit, a line receiver unit, and system power supply. These would then be placed in a shielded enclosure along with a cable under study. Manual scanning with a receiver system was chosen over a spectrum analyzer because a greater resolution of the E-field radiation profile was desired. Figure 1 depicts the general orientation of the cables, interface units, and test equipment. The line driver and line receiver units were secured to a copper-clad test bench bonded to the walls of the shielded enclosure and elevated one meter above the floor. This test bench acted as the equipotential plane of the test setup. The parameters to be varied during the course of testing were 1)the presence or absence of a line-terminating resistor, 2)the cable shield terminations, and 3)the use of filterpin connectors versus non-filterpin connectors.

that the bias supply decoupling capacitors are not included on-chip. These parts offer the RF systems designer/integrator a new option in system architecture and implementation at UHF frequencies and above. By cascading or individually distributing these ICs throughout the system, there is now available compact and affordable amplification is to maximize system performance. System Cost/Performance targets can be more easily met though the use of these complete IC gain blocks, with low $/dB of gain, and the relaxed performance specifications on other system functions that these amplifier ICs allow.

The Product

Fundamental in the offering of an effective GaAs IC is the basic quality of the fabrication process. Harris Microwave Semiconductor uses its DIGI-1 Process Technology. Harris has been manufacturing GaAs (digital) ICs with this process for over three years. DIGI-1 is a very high performance process technology offering the high gain required for analog circuits and the high repeatibility required for digital circuits. Repeatibility is the secret for both the low cost and consistency achieved in these RF ICs. This process uses a one micron gate length and depletion mode technology with -2 Volt pinchoff. A summary of the basic process electrical parameters is contained in Table 1.

Electrical parameters:	
Shallow implant (n)	1190 Ω/□
Deep implant (n+)	110 Ω/□
Ohmic contact	1 Ω□
Gate metal (air-bridge)	0.02 Ω□
Specifications: Transistor (1_G = 50μ)	
I_{dss} (V_{ds} = 3 V, V_{gs} = 0 V)	200 mA/mm
V_p /V_{ds} = 3 volts I_{ds} = 1% I_{dss}	-1.9 V
gmOt (V_{ds} = 3 V, V_{gs} = -0.5 V)	150 mΩ mm
BV_{gs0} (I_{gs} = 100 μA)	16 V
BV_{gd0} (I_{gd} = 100 μA)	16 V
Second metal (air-bridge)	0.02 Ω□
Diodes	
C Junction	1.6 pF mm^{-2}

TABLE 1. DIGI-1 process technology

The circuitry is designed to exploit the performance characteristics of the process technology to produce consistently achieved performance for the system application. The schematic of the HMR-10503 is shown in Figure 1. The heart of the IC is a 1 X 600 micron GaAs FET "cell". Two of these cells are isolated from each other by integral MIM capacitors. The source terminals of the RF Transistors and self-biasing implanted resistors, in series with the sources, are decoupled by additional MIM capacitors of approximately 25 pF each. Drain bias on the active RF devices is provided by additional FETs operating as current sources. Each of the current sources is shunted by an implanted resistor to minimize the bias point sensitivity to process and temperature variations. Consistent broadband RF performance is the result of a series resistor-inductor which is in shunt feedback to the RF transistor. The two stages have been designed as a system to minimize input/output VSWR, maximize gain, and maintain a controlled noise figure.

Two computer I/O cables chosen for the study were supplied by a customer as cables typically used in their communications center. The first cable tested (BRAND-REX telephone cable 11PR-24AWG 200 C) contained 13 pairs of stranded wire. These wires were not twisted pairs. The cable had only a single Beldfoil shield with a stranded drain wire surrounding the wire conductors. This cable was terminated with ITT connectors (#MS 3475L16-26S) at both ends. The overall length of the cable was 28.5 feet (8.7 m).

The second cable had 27 twisted wire pairs which were each shielded with Beldfoil and had individual stranded drain wires. In addition, the 27 pairs and their shields were collectively shielded by an overall cable shield of Beldfoil with an associated stranded drain wire. This cable was also provided by the customer and came terminated with Amphenol connectors (#3475L22-55S 8206-2) at both ends. The overall length of the cable was 29.25 feet (8.9 m).

In order to test the effectiveness of different configurations of shield terminations, the I/O cable needed to carry digital data of a standard format. For this purpose, a line driver unit and a line receiver unit were constructed in small RF-tight boxes in such a manner as to assure that emanations detected during E-field tests were produced strictly by the cable and not either unit. The line drivers and line receivers used mmeet the requirements of EIA Standard RS-422. (Balanced transmission of data was chosen because of the greater noise immunity.) The line driver unit and the line receiver unit were fitted with one 26-pin connector and one 55-pin connector on an end wall of the boxes. This permitted connection of either I/O cable to the units. The two connectors were wired in parallel with correspondingly lettered pins connected together. (Unused pins on the 55-pin connectors were left open in the boxes.) With this arrangement, one or several pairs of conductors could be used for the evaluation if need be.

The line receiver unit was also equipped with a BNC connector. This connector allowed the receive data to be monitored. The schematic (Figure 2) shows the chips

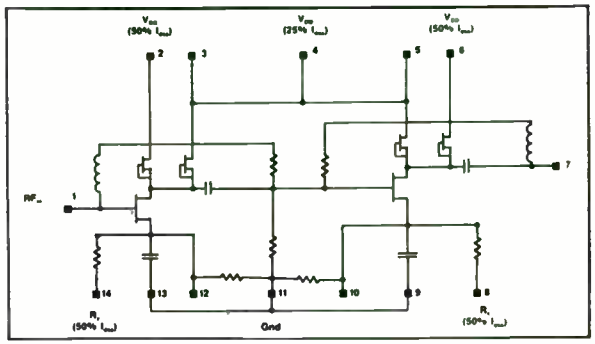


Figure 1. HMR-10503 Schematic

As seen in the schematic, two bias point options are readily available to the user. In addition to the standard 25% Idss, either or both of the two stages can be biased to 50% of the RF transistor Idss with additional wirebonds. Bonding diagrams for two of the four wiring options are shown in Figure 2.

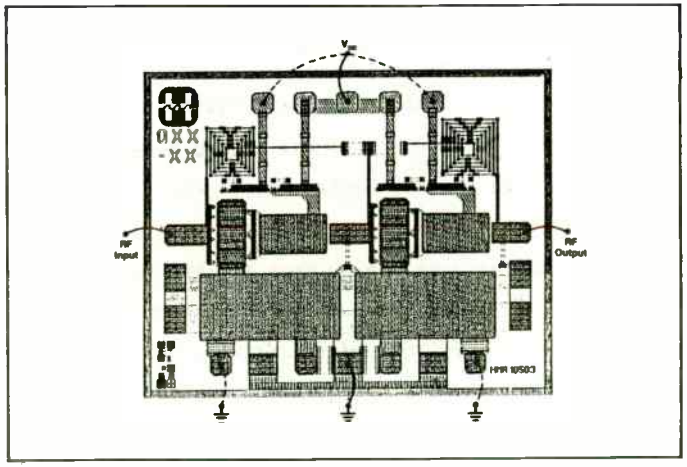


Figure 2. Wire bond diagram for HMR-10503. Solid lines are 25% I_{dss} connections (V_{DD} = +8 V). Dashed lines are additional connections for 50% I_{dss} (V_{DD} = +10 V).

Wide Band Performance

Performance of the typical HMR-10502/HMR-10503 is shown in figure 3. Frequency of operation for the ICs is 500 MHz to 5.0 GHz with extended frequency operation possible at reduced performance level. Power supply limits are from +6.0 Volts to +15.0 Volts although typical applications call for +8.0 Volts or +12.0 Volts for Vdd at 50 mA.

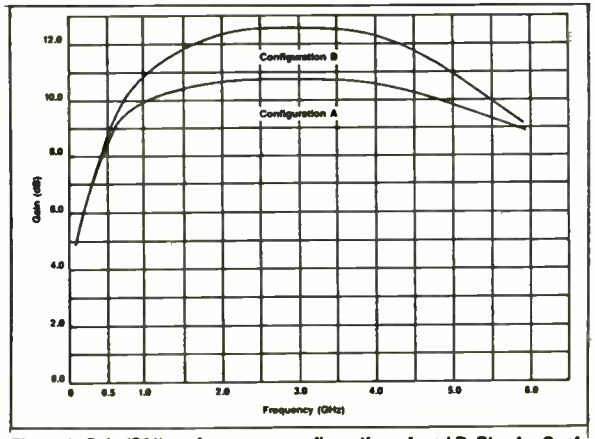


Figure 3. Gain (S21) vs. frequency, configurations A and B. Bias for Conf. A: D_{dd} = 8.0 V, I_{dd} = 50 mA; Bias for Conf. B: V_{dd} = 10.0 V, I_{dd} = 100 mA.

A minimum of 10 dB gain is readily achieved at 8 Volts and 25% Idss with 12 dB typical, (configuration A). Gain flatness is +/- 0.75 dB for the HMR-10502 over the complete 0.5 to 5.0 GHZ frequency range with two 100 pF source decoupling capacitors, one on each source decoupling port. The HMR-10503 has the same +/- 0.75 db gain flatness over a smaller 1.0 to 5.0 GHz bandwidth without optional source decoupling capacitors. Optional

used and their interconnection. Power was supplied to the circuit boards in the manner described below.

A regulated supply provided filtered +7.3v, -7.3v, and COMMON to the line driver unit (these voltages slightly exceed the devices' ratings and were considered to yield "worst-case" results). In addition to connection to the card edges, these leads were wired to three pin letters (six pins) of the multi-pin connectors. Power was then supplied to the line receiver unit via the I/O cable and multi-pin connectors.

System Grounding

Grounding of the system was treated as follows. Inside the line driver unit, three pieces of stranded wire connected the filtered COMMON of the power supply to the inside of the box, to circuit ground on the board, and to the conductors designated as COMMON from the multi-pin connectors. Inside the line receiver unit, a piece of stranded wire connected the COMMON cable conductor (at the card-edge connector) to the box. The line driver unit and the line receiver unit were each placed on insulating material on top of the test bench. These units were then grounded to the copper test bench by 0.5-inch ground straps.

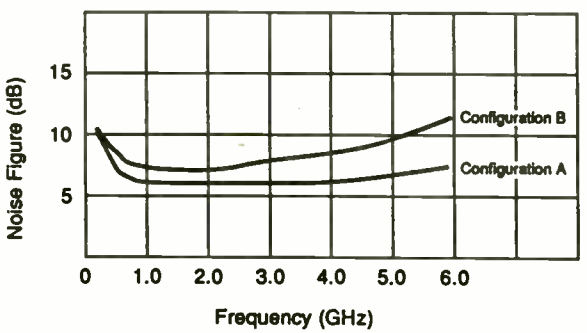
The cable shields were to be grounded at the line driver and/or line receiver units' bulkheads. Because of the Beldfoil shield construction of the cable, drain-wire connections to ground were concidered to be the simplest termination mode available. A 3.5 cm. drain wire length was used as a minimum pig-tail termination. The wire termination was then passed through the rear of the backshell to act as the shield ground termination. These shields, their drain wires, and the ground-wire connection were insulated with electrical tape so as to be isolated from the overall cable shield. 3.5 cm. wires were also used at both ends of the overall cable shield and passed through the rear of the backshells for use as this shield's ground termination. The overall cable shield, its drain wire, and the ground-wire connections were insulated with electrical tape so as to be isolated from the backshells' conductive coating.

additional source decoupling capacitors of greater than 50 pF result in full band flatness for the HMR-10503. The VSWR of the input and output is always better than 2.0:1 and typically better than 1.7:1 across the specified frequency band when assembled using nominal wirebond lengths of 15 to 25 mils.

Noise figure for either unit at 25% Idss is typically 6 db, 7.0 db maximum. When biased at 10 Volts and 50% Idss (configuration B), the noise figure is less than 10 dB and typically less than 8.0 dB. Figure 4 shows the typical noise figure at both bias conditions versus frequency.

FIGURE 4

TYPICAL NOISE FIGURE vs. FREQUENCY, CONFIGURATIONS A AND B.



The third order intercept point (IP3) versus frequency for both bias options is shown in Figure 5. The minimum of +18 dBm is achieved at the high end of the frequency band at 25% Idss. Typical third order intercept point at 50% Idss is greater than +20 dBm.

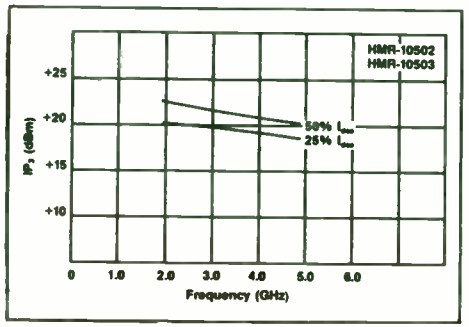


Figure 5. Third order intercept point vs. frequency.

Idd variation at either bias option is consistent unit to unit as well. Typical supply current is 50 mA plus or minus 10 mA at the low bias point for the total unit. DC supply voltage is user defined from 8 to 15 Volts depending on the specific power supply voltage availability, specific output power desired, and temperature range requirements. The basic performance characteristics of gain, VSWR and isolation are relatively independant of power supply voltage. Gain variation of gain of typically 0.03 dB/ degree C for this two stage amplifier. Flatness is maintained across wide temperature ranges. Figure 8 shows the typical gain performance at -20, +25 and +85 degrees C.

On the 26-line cable, the 3.5 cm. long ground-wires were passed through the rear of the backshells. The shield, drain wire, and ground-wire connections were then insulated with electrical tape and the backshells were replaced. When a cable was to be tested, it was suspended from the screen room ceiling. The cable was looped around the shielded enclosure as nearly to 1 meter from the screenroom walls, floor, ceiling, and test bench as possible. The cable ends were attached to the line-driver unit and line-receiver unit, which were clamped to the test bench.

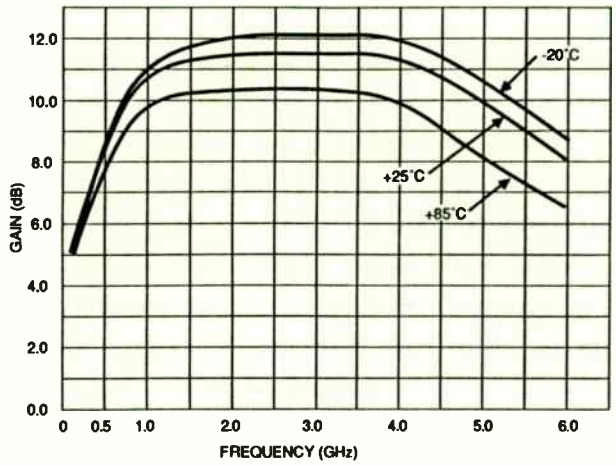
The shield ground wires were terminated in spade lugs. This permitted the shield terminations to be reconfigured by fastening the appropriate lug to the connector backshells at a cable restraint screw. For the 26-line and the 55-line cable shields, tests were performed using various shield termination configurations with and without a matching resistor present.

The antenna was positioned approximately 1 meter from the cable and 1 meter from the test bench. Figure 3 illustrates the orientation of the cable, antenna, and interface units within the shielded enclosure. Test data were repeatable, provided that the particular I/O cable under test maintained a constant orientation. If, for example, a series of tests were performed on one of the cables during which several of the parameters under study were changed and then the tests for the first parameter change were repeated, the results of the two tests would be within 3 dB of each other. If one cable was fully tested and then the other cable was fully tested, any attempts to repeat tests of the first cable would give a somewhat different radiation profile because of the different orientation of the cable with respect to the antenna and shielded enclosure. Even though the radiation profile would be different for the reconfigured cable, the relative test results remained the same.

Digital Signal Line Conduction (DSLC) Tests

Two sets of DSLC tests were performed. Both sets were run at a data rate of 9.6 kbit/sec. Test parameters were based upon the operating data rate of 9.6 kbit/sec. For these tests, high-pass filter sections were inserted at 10 kHz, 100 kHz, 1 Mhz, and 10

FIGURE 6. GAIN (S21) VS. FREQUENCY AT -20°, +25°C AND +85°C, CONFIGURATION A.
Bias for CONF. A : Vdd = 8.0V, Idd = 50mA.



Testing and Quality Assurance

To insure consistent and reliable performance, the HMR-10502 and HMR-10503 are tested and qualified under procedures similar to standard FETs produced by Harris Microwave Semiconductor. Samples from each lot are strenuously tested to qualify the lot for mechanical integrity, electrical performance, and reliability. The flow of the product assurance and lot qualification process shown in figure 7 results in product that exceeds the Element Evaluation requirements of MIL-STD-883C, Method 5008 for Class B devices.

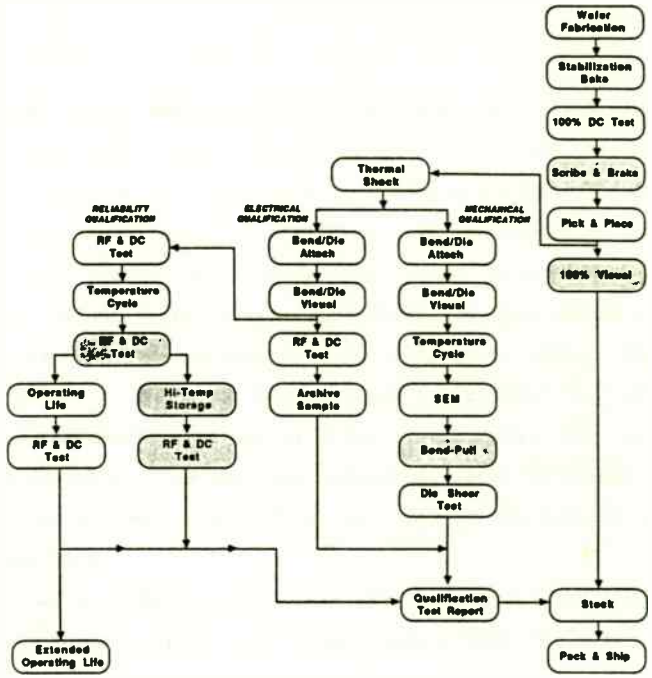


Figure 7. Product Assurance Flow

The Applications

With the combination of low cost , repeatibility, reliability and application flexibility, the HMR-10502 and HMR-10503 can be effectively inserted into many system designs. One of the most obvious applications that can use the basic utility gain characteristics of the ICs is in receiver/transmitter modules. Figure 8 is a block diagram of a typical single channel dual conversion downconverter operating in the 500 MHz to 5.0 GHz frequency range configured with distributed gain in the form of HMR-10503s to maintain noise figure and dynamic range. A significant advantage of using distributed gain is that it

instance, there was a general increase (6 - 15 dB) in emanation levels for all but the top decade (30 - 300 Mhz) when Z was omitted. The least sensitive configuration when filterpins were not used was with the shield grounded only at the source end (Figure 7). Here, the omission of Z results in additional emanations from 0.010 to 0.050 Mhz and 4 - 8 dB enhancement of frequencies from 3 - 8 Mhz and from 40 - 60 MHz.

When filterpin connectors were used with the 26-line cable, none of the grounding configurations showed variations beyond 2 Mhz attributable to the presence or absence of Z. Grounding the cable shield at both ends seemed to result in the least sensitivity of all configurations (filtered or unfiltered). For this case, the inclusion of Z prevents enhancement of frequencies between 0.300 and 1.0 MHz as shown in Figure 8.

55-Line Cable Results, Z

The effect of Z on the 55-line cable was greatest when non-filterpin connectors were used. Comparison of the unshielded ER profiles with and without Z in place is shown in Figure 9 and reveals a gross increase in emanation levels over a fairly wide spread (i.e., 10 - 25 dB from 0.010 - 10 MHz). The increases were predominantly for frequencies below 10 MHz, with the exception of a 10 dB decrease near 60 MHz and a 15 dB increase near 150 MHz, both attributable to the exclusion of Z. This configuration, with all of the shields unterminated and without filterpins, was the most sensitive to the presence or absence of Z. Of the other configurations where filterpins were not used, some were far less sensitive. Even for the least sensitive unfiltered configuration (see Figure 10), large peaks were reduced by the inclusion of Z. In this configuration, the overall cable shield is open and the individual shields are grounded only at the source end. The frequencies of interest lie throughout the profile, with 10 and 15 dB increases near 5, 16, 20, and 60 MHz attributable to the omission of Z.

Where filterpin connectors were used with the 55-line cable, the effect of Z was less obvious. The more dramatic examples are configurations with the individual shields grounded at both ends and the overall cable shield open at one end. A comparison of these test

results in reduced specification requirements, and therefore cost, for the various subsystem elements such as mixers and filters.

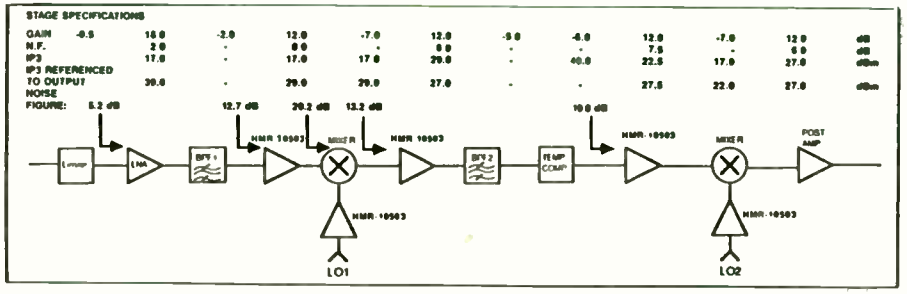


Figure 8. Downconverter Block Diagram

In this example, the input frequency is assumed to be 3.0 GHz, the intermediate frequency is 800 MHz, and the output frequency less than 150 MHz. This example converter has a reasonable frequency plan for minimizing spurious response from the mixer products. A dual conversion approach may not represent an optimum system, but does serve to illustrate the basic elements that affect system performance.

The input limiter is typically a PIN diode assembly for input protection and low insertion loss, normally a coaxial component or a substrate assembly inside the converter module. Since the insertion loss of this device degrades the system noise figure, it is important that it is appropriately specified and designed. For this example, a 0.5 dB insertion loss is assumed.

The low noise amplifier (LNA) defines the sensitivity of the receiver subsystem and therefore its specifications are key. In the typical converter, the output power capability of the first stages of amplification has little impact on system dynamic range due to the relatively low gain. A 2.0 dB noise figure in a module having 18 dB of gain is achievable at 3.0 GHz. Intermodulation performance is not a critical specification for the first stage.

The band pass filter (BPF1) defines the input bandwidth of the receiver and eliminates the "image band" for the subsequent mixer operation. Rejection of this undesired sideband is a strong contributor to the sensitivity of the receiver. Interference signals collected by the antenna in this undesired sideband must be rejected, or they become noise and distortion on the signals of interest. The modest gain levels, before the first mixer, afforded by distributed gain keeps the level of the image band signals low. Therefore the rejection requirements for the filter are minimized, saving overall subsystem volume (size) and cost. A relatively simple microstrip structure with 2.0 dB of loss would usually be adequate.

Between the filter and mixer, utility gain in the form of an HMR-10503 is inserted. The gain and intermodulation performance of this IC complement the use of a low cost mixer and the insertion losses of the mixer are overcome by the gain of the HMR-10503. The reverse isolation of the amplifier limits the undesired LO leakage of the mixer. The specified performance of most mixers is with a condition of all ports terminated in broadband 50 ohm loads. Reactive termination of the inputs or the output with a reactive load such as a filter, can frequently lead to insertion loss ripple and worsened intermodulation distortion. The low VSWR of the amplifier output properly terminates the

cases is shown in Figure 11. For these configurations, the increases were 6 - 15 dB in magnitude and occurred primarily for frequencies from 0.200 - 2.0 MHz. For the other configurations where filter-pin connectors were used, the presence or absence of Z was less critical. The least sensitive of the filtered configurations was with the individual shields grounded only at the source end and the overall cable shield grounded at both ends (see Figure 12) where the inclusion of Z reduced emanations from 4 - 9 MHz by 2 - 4 dB.

EFFECT of GROUNDING CONFIGURATION

The results of grounding cable shield terminations in various combinations are discussed below. These effects vary between the two cables and between test cases where filterpin and non-filterpin connectors were used. The simpler, 26-line cable tests are discussed first.

26-Line Cable Results, Shield Termination Configurations

For the singly-shielded, 26-line cable, the greatest shielding effectiveness resulted from grounding the shield at both ends. When non-filterpin connectors were used, grounding both ends of the shield was most effective for frequencies below 6 MHz compared to the unshielded profile as shown in Figure 13. Here, the very lowest decade (0.010 - 0.100 MHz) of emanations is completely eliminated. There is some shielding effectiveness above 10 MHz, but these frequencies are still at unacceptably high levels.

When non-filterpin connectors were used with the 26-line cable, grounding a single end of the cable shield was most effective below 1 MHz. Note the results of these test cases, also shown in Figure 13. There was a loss of shielding effectiveness (as much as 30 dB) from 1 to 20 MHz when only one end of the shield was grounded.

When the 26-line cable was connected using filterpins, the most effective grounding configuration using filterpins was where the cable shield was grounded

input of the mixer to minimize spurious performance. This amplifier would be biased at the 25% Idss level. At this bias level the HMR-10503 would have 12.0 dB of gain with typically 6.0 db noise figure.

A mixer is specified to minimize insertion loss and spurious responses. Spurious response is usually a function of the intercept point of the mixer, which is a strong function of the LO drive capability. In addition, the termination of the LO port in particular, and the RF and IF ports in general, affect the level of spurious mixing products. For reasonably broadband signals, optimization of the termination with reactive elements for all the spurious signals is extremely difficult. In addition, most mixers are specified for 50 ohm terminations over a limited LO "drive" range. This might be 3 to 6 dB around a required LO drive level of +7 to +10 dBm. An isolator would furnish the appropriate termination and isolation. The use of a buffer amplifier in gain compression, such as the HMR-10503, on the LO port also results in predictable spurious response while providing increased and stable power level to the mixer. A relatively simple low cost mixer is assumed in the block diagram analysis. Such a mixer would likely have 7.0 dB insertion loss with a +17.0 dBm third order intercept point, referenced to its input.

On the output of the mixer would be a buffer amplifier to terminate the mixer IF port and also to furnish isolation from spurious signals from the second conversion stages of the converter. This amplifier also furnishes a stable termination for the bandpass filter (BPF2) assuring minimal VSWR induced ripple in the insertion loss. This amplifier would also be biased at 25% Idss. Since the third order intercept point of the HMR-10503 is greater than +20.0 dbm referenced to the output at the IF band, the intermodulation performance is sufficient as to not degrade the subsystem dynamic range.

The second Bandpass filter (BPF2) effectively determines the converter bandwidth. This filter is typically as narrow as the desired signal bandwidth will allow. Since insertion loss is a function of bandwidth, this filter specification would have higher loss than the "frontend filter" BPF1. The out-of-band rejection is set by the need of reverse isolation. Since the HMR-10503s in the IF path each furnish 30 dB of reverse isolation, the bandwidth and number of "poles" for this filter may be reduced. A loss of 5.0 db could be expected from this filter using low-cost implementation technology.

Many converters require that gain variation over temperature be minimized. To correct for the gain variations, temperature compensation circuits are used. Usually these are included in the First IF section between the IF filter BPF2 and the second mixer. PIN Diode networks or attenuators comprised of FET "Tee" or "PI" circuits with silicon opamps for drivers are typically used. The insertion loss of this function is dependent on the amount of gain control required. For this example a nominal loss of 6.0 dB is assummed.

The input to the second mixer is buffered for the same reasons as the first mixer. The needs for good termination and isolation on the input port of the mixer is mandatory for predictible performance. Additional specification constraints on

at both ends. Comparison of the graphs of Figure 14 shows attenuation as great as 38 dB for frequencies below 7 MHz. This eliminates the lowest decade (0.010 - 0.100 MHz) of emanations, and reduces the levels of the remaining emanations.

When filterpin connectors were used with the 26-line cable, grounding one end of the cable shield was most effective below 0.200 MHz (Figure 14). It made little difference which end was grounded, but grounding only a single end resulted in a loss of attenuation (as much as 40 dB) from 0.100 MHz to 10 MHz. In each instance, there was only a narrow band of frequencies from 0.300 - 0.600 MHz where mild enhancement (maximum of 8 dB) over the unshielded profile occurred. However, when these configurations were compared to similar configurations where filterpins were not used (Figure 13), they demonstrated a drastic loss of shielding effectiveness from 0.100 - 1 MHz when only a single end of the shield was grounded. This effect is apparently not the result of the grounding configuration alone, but of the sensitivity of these configurations to the presence of the filterpins.

55-Line Cable Results, Shield Grounding Configurations

The 55-line cable, having two (sets of) cable shields, realized its greatest shielding effectiveness when both the overall cable shield and the individual shields were grounded at both ends. Figure 15 depicts these results. When non-filterpin connectors were used, the unshielded profile extended up through 300 MHz. The lowest two decades (0.010 - 1.6 MHz) of emanations were eliminated by grounding all four shield terminations. Attenuation of the radiation profile at certain frequencies above 10 MHz exceeded 20 dB.

If the individual shields are grounded at both ends (non-filterpins still used), opening one end of the overall shield does not drastically reduce the attenuation. In fact, opening both ends of the overall cable shield (Figure 15) does not result in a gross loss of attenuation, provided that both ends of the individual shields are grounded. However, termination of the individual shields is far more critical. Even when both ends of the overall cable shield were grounded (and non-filterpins were used), opening one end of the

this amplifier are associated with output power level as it relates to intermodulation distortion. In this typical system, an HMR-10503 is used with either one or both stages biased at 50% Idss of the RF transistors as described earlier. Its greater than +22.5 dBm third order intercept point is adequate to avoid degradation of the subsystem intermodulation performance. Gain would typically be +13 dB for this stage at the 50% Idss bias point.

The final mixer down-converts the first IF for distribution in the receiver subsystem. Again the performance of the mixer is dependant on the VSWR of the loads terminating the RF, LO, and IF ports. The use of utility gain blocks also satisfies the subsystem needs for this second mixer. A low cost mixer is assumed for this function. The +17 dBm third order intercept point of such a mixer is the subsystem limiting intermodulation distortion contribution. The use of a higher performance mixer would enhance subsystem performance. The HMR-10503 used as a LO buffer would furnish adequate power drive for a higher dynamic range mixer.

The post amplifier function isolates the mixer output from the converter output and establishes the output VSWR. The dynamic range specification requirements for this block are the most stringent of any of the circuits in the converter. A well designed, high intercept point amplifier is needed. This example assumes an amplifier with 12 dB of gain and a noise figure of 6.0 dB.

The example demonstrates the use of distributed gain in nominal 12 dB increments to facilitate the design of RF converters. The analysis contained on the block diagram, shows that utility gain blocks, and other RF functions of nominal performance, can result in reasonable overall performance of the subsystem. Each subsystem function, whether it be a filter or mixer, benefits from reduced component performance specifications while maintaining dynamic range. Repeatibility, consistency and compliance to design are more easily achieved with the use of distributed gain ICs and their controlled, predictable interfaces with the other subsystem functions.

The introduction of Harris Microwave Semiconductor's HMR-Series of RF IC products offers subsystem designers a unique opportunity for high performance frequency converters. Key attributes offered by amplifier stages, distributed through a subsystem design, can now affordably be inserted into communication, EW and radar systems supplying more functions in smaller packages at lower cost. The promise of more highly integrated RF IC-based subsystems can now be realized.

individual shields creates problems. Comparison of the graphs of Figure 16 shows a general loss of attenuation (especially from 1 - 10 MHz) and a slight increase in frequency spread. As the overall shield was opened at one end or the other, not only a further loss of attenuation was noted, but a drastic increase in frequency spread (greater than 1 decade in lower frequencies) as well. Figure 17 shows the radiation profile which occurs in the absence of any benefit of the overall cable shield (i.e., open at both ends). Grounding only a single end of the individual shields resulted in a slight decrease in emanation levels when just the source end was grounded and an increase in emanation levels at higher frequencies when just the load end was grounded. This enhancement of the higher frequencies occurred from 22 - 80 MHz with amplitude levels greater than those of the unshielded profile. Enhancement of emanations was a greater problem when filterpin connectors were used with the 55-line cable.

When the 55-line cable was connected with filterpins, the unshielded profile (shown in Figure 18) produced a greatly reduced radiation profile which extended only from 0.010 - 20 MHz. Several grounding configurations further attenuated these emanations, while several enhanced the emanations. This enhancement of emanations from 0.200 to 2 MHz is exhibited by some configurations where, at certain frequencies in the range of enhancement, there is an increase in emanation levels as great as 18 - 20 dB above those of the unshielded profile. These configurations were those where a cable shield was grounded at a single end, but neither the overall cable shield nor the individual shields are grounded at both ends. Note the affect on emanation levels. These grounding configurations were also the least effective from the standpoint of frequency spread. This enhancement does not result from the grounding configuration. Comparison of similar configurations where non-filterpin connectors were used (Figure 17) with the unfiltered, unshielded profile reveals that these configurations should attenuate emanations from 0.200 to 2 MHz.

Of the remaining configurations where filterpins were used, greater attenuation was effected by grounding both ends of the individual shields than by grounding both ends of the overall shield. Comparing the results showed improvements for frequencies below 6 MHz

excluding those between 1 and 2 MHz. The best grounding configurations are shown in Figure 19. These are the test cases where the individual shields were grounded at both ends and the overall cable shield was open at both ends or grounded at both ends. In these cases, there was both a large reduction of frequency spread as well as great attenuation of frequencies below 4 MHz (compare these with the unshielded profile). The addition of the overall cable shield resulted in the elimination of emanations between 2 and 4 MHz.

EFFECT of FILTERPIN CONNECTORS

Both cables were tested using filterpin connectors. The effect of these filterpins upon the ER profiles of the different grounding configurations is seen by comparing a filterpin test with its non-filterpin counterpart. For such comparisons, it is necessary to include certain bandwidth correction factors in order to account for the different bbandwidths used in collecting data. A correction factor of 12 dB should be added to the filterpin results when they are compared to the non-filterpin results within the frequency range of 0.900-30 MHz. The tests of the 26-line cable will be discussed first.

26-Line Cable Results, Filterpins

The most prominent and consistent effect of the filterpins was a general reduction of the overall frequency spread of the ER profiles as can be seen in Figure 20. When the 26-line cable was connected with non-filterpins , the ER profile spanned from approximately 0.010 - 300 MHz. Inclusion of the filterpins reduced this, allowing the profile to extend only to 20 MHz . For this configuration, with the cable shield open at both ends, the filterpins cause a slight enhancement (maximum of 9 dB at 500 kHz) of emanations from 0.100 - 2 MHz over the unshielded profile without filterpins. This is far more pronounced for other configurations.

In two instances shown in Figures 21 and 22, use of filterpins resulted in a gross enhancement of emanations between 0.100 - 2 MHz. When the cable shield was grounded at one end alone, these emanations were 10 - 40 dB higher (remember to include the bandwidth correction factor) than those of corresponding non-filterpin configurations.

When the cable shield was grounded at both ends, the filterpins caused an enhancement of the emanations from 0.250 - 4 MHz (see Figure 23). For this filterpin test case, emanations were first detected at 0.095 MHz versus 0.250 MHz. As in the other cases, the filterpins completely eliminated measurable emanations beyond 20 MHz. Also, the filterpins caused slightly less attenuation of the emanations near 16 MHz (approximately 22 dB) than the other filterpin configurations (28 - 30 dB). The overall levels near 16 MHz were about the same in all four cases shown in Figure 14.

55-Line Cable Results, Filterpins

When the 55-line cable was connected with filterpins, there was a large reduction in the frequency spread of the emanations, as well as frequent enhancement of the remaining emanations over those of corresponding unfiltered profiles. Figure 24 exemplifiess this. When filterpin connectors were not used, the unshielded ER profile spanned from approximatelv 0.010 - 300 MHz. The filterpin connectors limited the range of emanations to 16 MHz. (The correction factor of 12 dB must be added to all filterpin results between 0.900 and 30 MHz before comparison with non-filterpin tests.) In the configuration with both the overall shield and the individual shields open at both ends, this filterpin radiation profile was used as the basis of comparisons to determine enhancements attributable to the filterpins for the various permutations of sheild terminations.

The use of filterpins in all these grounding configurations increased emanation levels somewhat over those comparable cases where filterpins were not used. Of those effected, the two configurations which had the least enhancement were those where the individual shields were grounded at both ends and the overall cable shield was either open at both ends or grounded at both ends. (These results are shown in Figure 25 along with the corresponding unfiltered test configuration results.) In these cases, the use of filterpins resulted in emanations occurring approximately one-half decade lower in frequency than the unfiltered test setup counterpart.

The greatest enhancement of low-frequency emanations occurred when filterpins were used in a configuration where shields were grounded only at a single end. In these cases, gross enhancement (10 - 35 dB) of emanations resulted over the decade of 0.100 - 1 MHz. Another point of interest can be made by examining the results of the filterpin test cases shown in Figure 18. The four cases of interest have a peak emanation occurring approximately at 0.250 MHz with levels 12 - 15 dB greater than those at the same frequency for the test case where no filtering and no shielding was used (see Figure 17). The interesting aspect of this is that 0.250 MHz is the frequency corresponding to the transitional rate of the data bits.

For all grounding configurations of the 55-line cable, the filterpin connectors attenuated emanations above 20 MHz so that they were no longer detectable. It may be worth noting that emanations near 16 MHz underwent varying degrees of attenuation. This attenuation ranged in value from 50 dB (Figure 26) to 36 dB (Figure 25). The filterpins have typical insertion losses of 25 - 30 dB near this frequency.

CONCLUSIONS

Use of Z with the 26-Line Cable

The 26-line cable, having wire-pairs of unspecified characteristic impedance, presented a potential mismatch at the source end of the cable, as well as at the load end. In every test configuration, inclusion of a 100-ohm matching resistor provided at least a minor reduction of emanation levels. When filterpin connectors were used, the benefits of Z become less obvious. It is suggested that the characteristic impedance of the filterpins (10 - 100 ohms) placed at both ends of the cable predominates in the transmission line parameters by reducing the impedance mismatch at both ends of the cable. However, because there is no certainty that the filterpins will be matched from connector to connector, or line to line, it is recommended that the 100-ohm matching resistor, Z, be connected across the differential pairs of the 26-line cable.

Use of Z with the 55-Line Cable

The 55-line cable, whose wire-pairs are specified as having a 100-ohm characteristic impedance, presented a potential mismatch at the load end of the cable. Omission of the 100-ohm matching resistor generally resulted in higher level emanations with no noteworthy increase in frequency spread. When filterpin connnectors were used, improvements arising from the inclusion of Z were less obvious. Again, it is believed that the characteristic impedance of the filterpins, imposed upon the cable prior to Z, reduces the impedance mismatch. However, because of the uncertainty of filterpin pairing (line to line and end to end), it is recommended that a 100-ohm matching resistor be placed across the differential pairs at the load end of this cable.

INFLUENCE OF SHIELD GROUNDING CONFIGURATION

26-Line Cable Shield Termminations

When using the singly-shielded, 26-line cable, it was always best to ground the cable shield at both ends. A great deal of attenuation was forfeited by grounding only a single end of the shield. Some attenuation was noted at the high frequencies present when non-filterpin connectors were used. However, any appreciable attenuation due to shielding effectiveness extended only to 6 or 7 MHz for the non-filterpin test cases. When filterpin connectors were used, attenuation of emanations by the shields extended only up to 0.300 MHz.

55-Line Cable Shield Terminations

The shields of the 55-line cable were most effective when the two shields were grounded at both ends of the cable. When non-filterpin connectors were used, the influence of different shield grounding configurations were discernable up through 100 MHz. The effectiveness of shield grounding was predominant at frequencies below 6 MHz. Grounding a single end of the shields caused a loss of attenuation. Termination of the individual shields was most crucial, probably due to greater capacitive coupling between the shields and wire-pairs.

When filterpin connectors were used with the 55-line cable, shield grounding was especially important. The worst configurations were those where a shield was grounded at a single end and neither the overall cable shield, nor the individual shields were grounded at both ends. These configurations actually resulted in enhancement of frequencies (from 0.2 - 2 MHz) over the unshielded profile. This enhancement was not noted for similar grounding configurations using non-filterpin connectors,and seemed attributable to the presence of the filterpins. The effects of grounding configuration were observable only up to 20 MHz because of the large reduction of frequency spread attributable to the filterpins. The greatest shielding effectiveness resulted from grounding all of the shields at both ends. The improvement of this configuration over others was discernable only to about 3 MHz.

EFFECT of FILTERPIN CONNECTORS

Lowpass filterpin connectors proved to be the single most effective method of reducing unwanted emanations. No configuration of shield terminations was nearly as effective as the filterpins. Even with the shields ungrounded, major reduction of emanation levels and overall frequency spread were achieved through the use of filterpin connectors. From the EM shielding perspective, the advantages of this attenuation far outweigh the few disadvantages that surfaced.

From the systems perspective, the filterpin connectors are potentially undesirable in a balanced data transmission system where they may contaminate the system grounds with common-mode currents. While these currents were not actually measured, they seem to have been responsible for enhancement of emanations in some instances. When filterpin connectors were used with either cable, all shield termination configurations resulted in at least some increase in emanation levels from 0.100 - 1 MHz. Configurations where a shield was terminated at a single end were most sensitive. Use of filterpin connectors in these configurations resulted in emanation levels dramatically increased (for the above frequency range) over those of similar configurations where filterpins were not used. In fact, emanation levels of the more sensitive configurations with the filterpin connectors exceeded even those levels in the

0.1-1 MHz range of the test case where no filtering and no shielding were used. It is believed that these shield termination configurations create an effective E-Field radiator. In so doing, the shields act as an antenna, driven at either end by common-mode currents from the filterpins to ground. This effect, although extremely detremental to shielding effectiveness, can be avoided by grounding all cable shields at both ends.

Aside from the reduction of emanations by filtering, another advantage of filterpins became apparent when the effects of an impedance matching resistor, Z , were studied. Emanations resulting from a potential impedance mismatch were reduced by the presence of filterpin connectors. The filterpins are specified as having a characteristic impedance between 10 and 100 ohms. Placement of this impedance at both ends of the transmission line-pairs tends to reduce the VSWR. While they are not likely to be custom-matched from end to end, or line to line, all of the filterpins have a characteristic impedance of the same order of magnitude (also coincident with the output impedance of the RS-422 line driver).

In the final analysis, the advantages of filterpin connectors far outweigh the disadvantages. With the proper shield configuration, the inclusion of filterpin connectors results in outstanding attenuation of unwanted emanations. The shielding effectiveness of any of these termination configurations is, however, based on the use of an equipotential ground plane as suggested in MIL-HDBK-419.

The next obvious step in an evaluation of techniques to reduce radiation from cables is to drive multiple signal lines. For this test situation, a rise in radiated field strength is expected with the increase in the number of driven lines. This increase would be attributed to the fact that all the signal lines share a common shield.

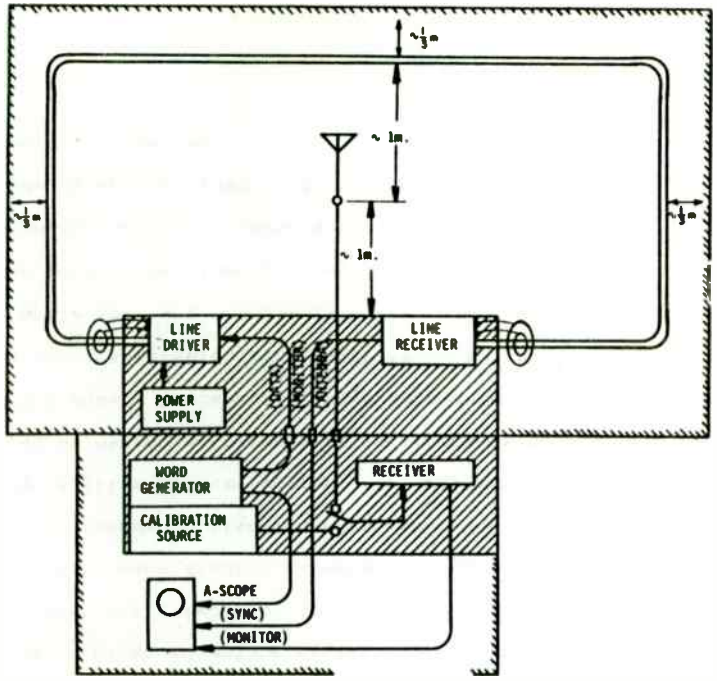


Figure 1. (U) Orientation of Cables, I/O Units, and Test Equipment

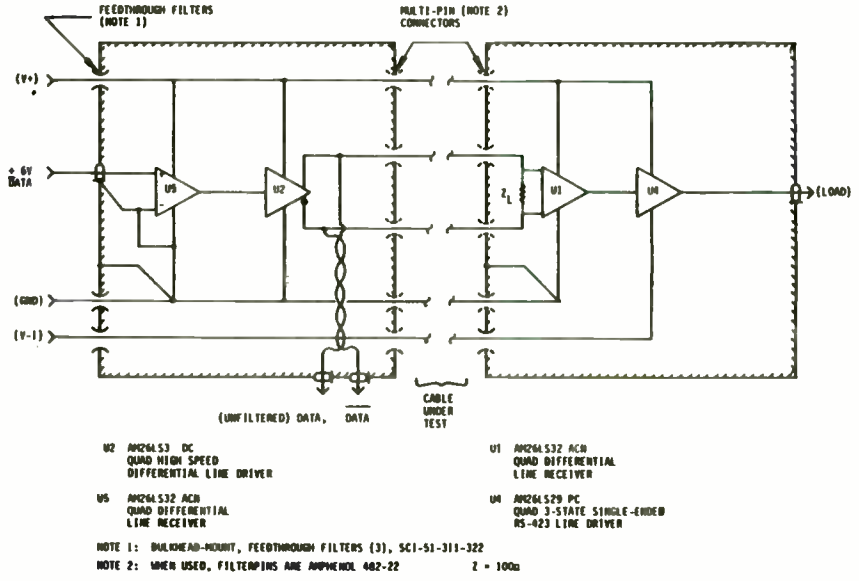


Figure 2. (U) Representation of Line Driver and Line Receiver Unit

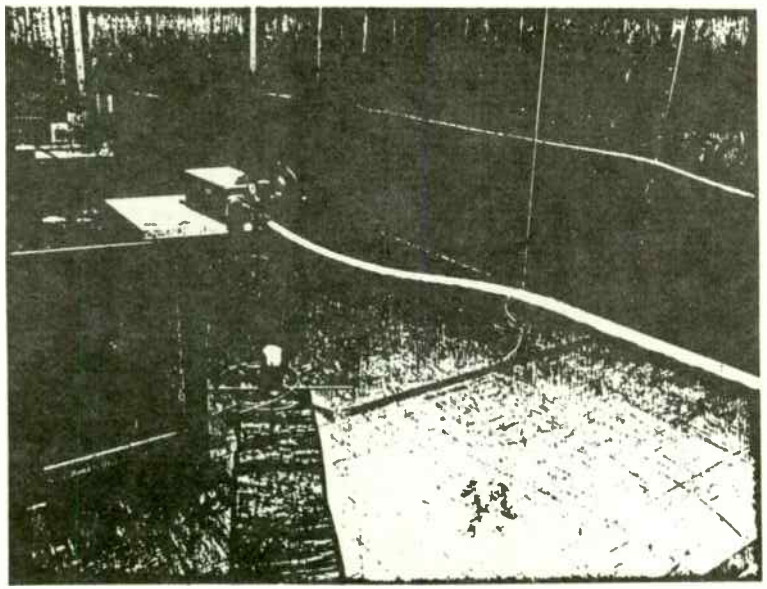


Figure 3. (U) Test Setup Depicting Relative Position of I/O Cable to the Antenna and Shielded Enclosure

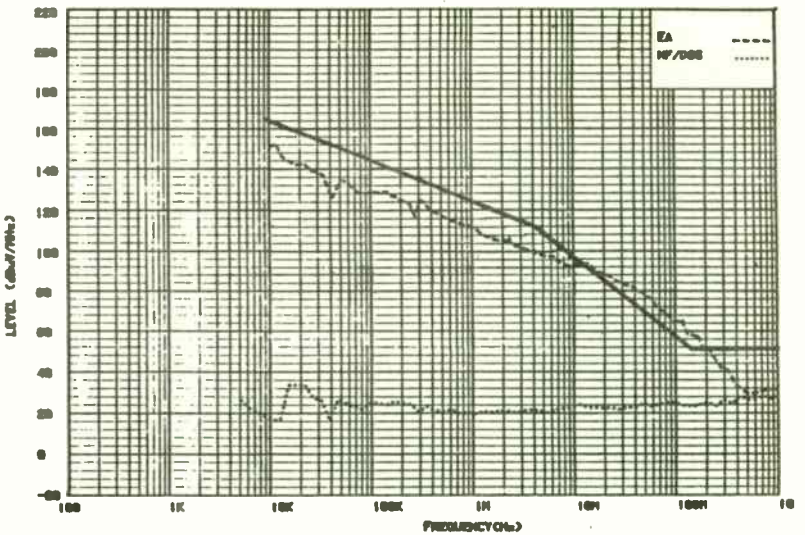


Figure 4. DSLC Test, Driver Baseband Output

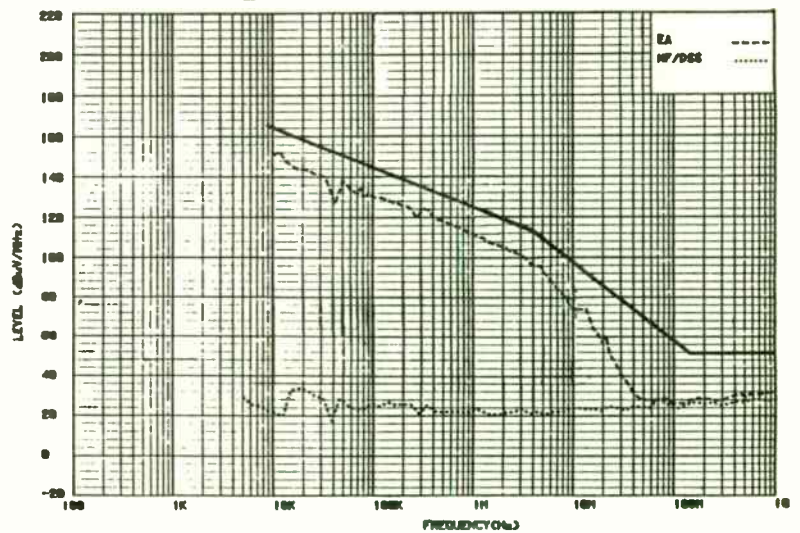


Figure 5. DSLC Test, Filterpin Baseband Output

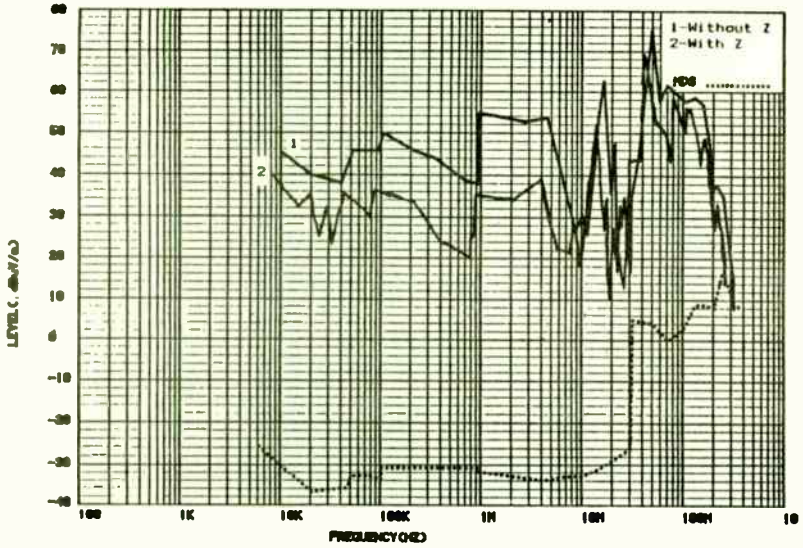


Figure 6. Affects of Z on the Radiation Profile of the Unshielded Cable.

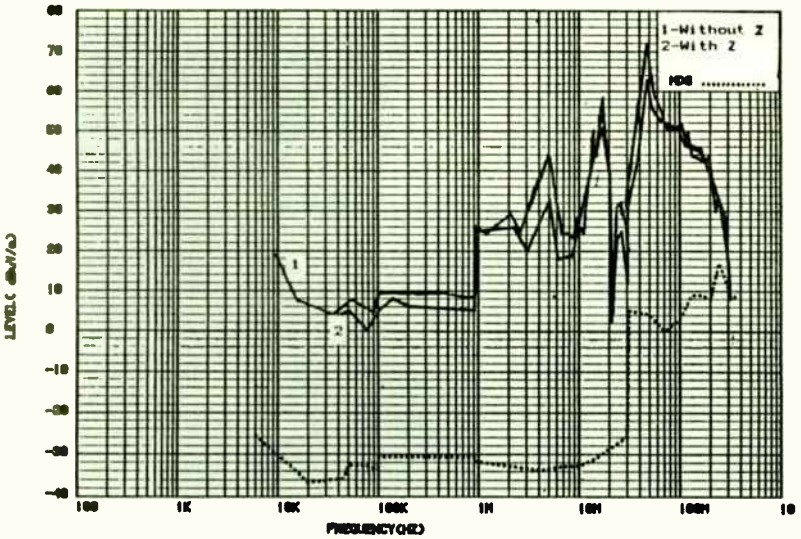


Figure 7. Affects of Z on the Radiation Profile of the 26-Line Cable with the Cable Shield Terminated at the Source.

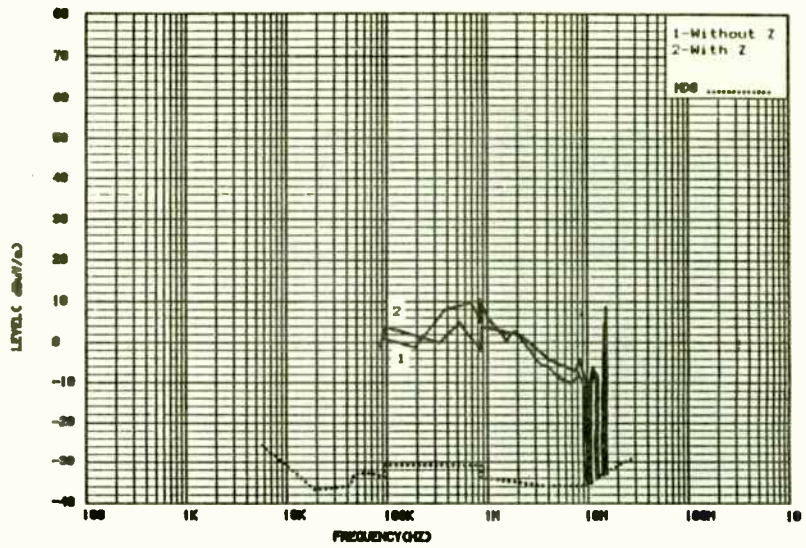


Figure 8. Affects of Z on the Radiation Profile of the 26-Line Cable with the Cable Shield Terminated at Both Ends and Filterpin Connectors Used.

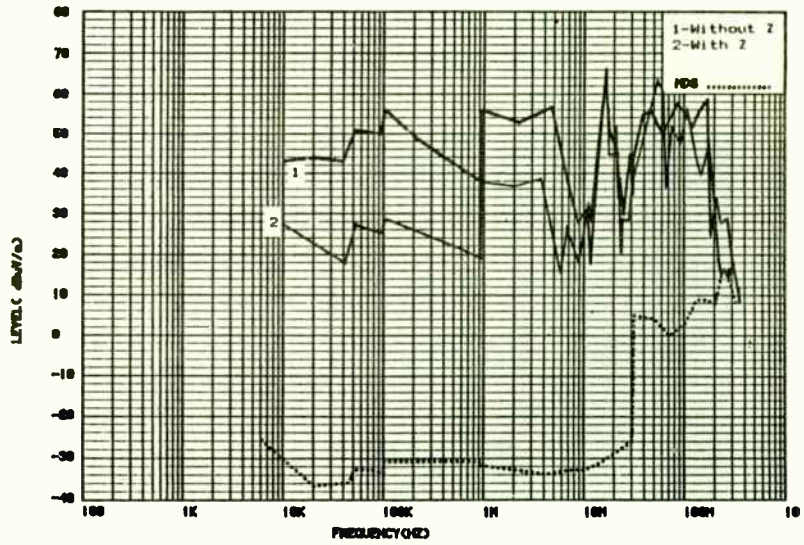


Figure 9. Affects of Z on the Radiation Profile of the Unshielded 55-Line Cable.

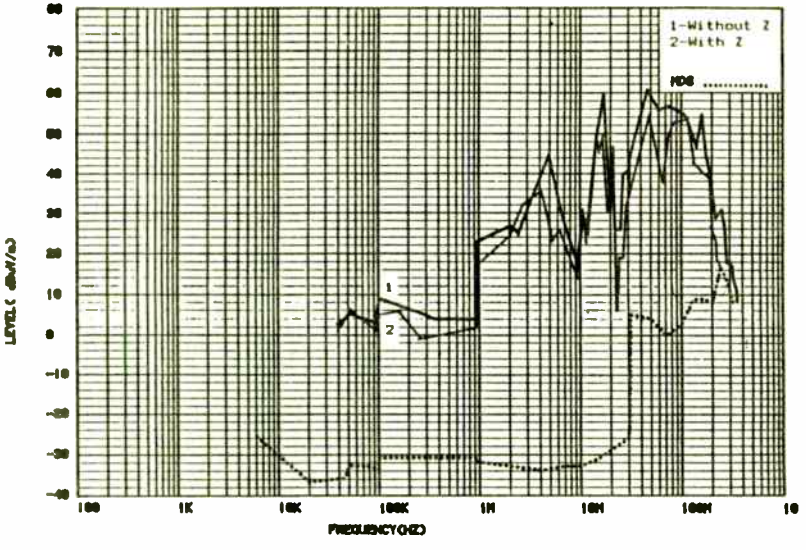


Figure 10. Affects of Z on the Radiation Profile of the 55-Line Cable with the Overall Shield Unterminated and the Individual Line-pair Shield Terminated at the Source.

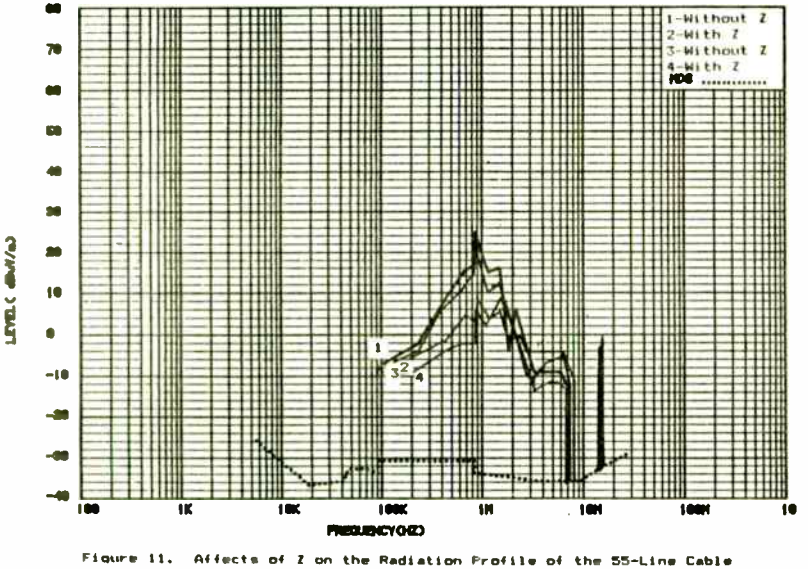


Figure 11. Affects of Z on the Radiation Profile of the 55-Line Cable with Filterpin Connectors Used. Here the individual line-pair shield is terminated at both ends and the overall shield is terminated at either the Source (1 and 2) or Load (3 and 4).

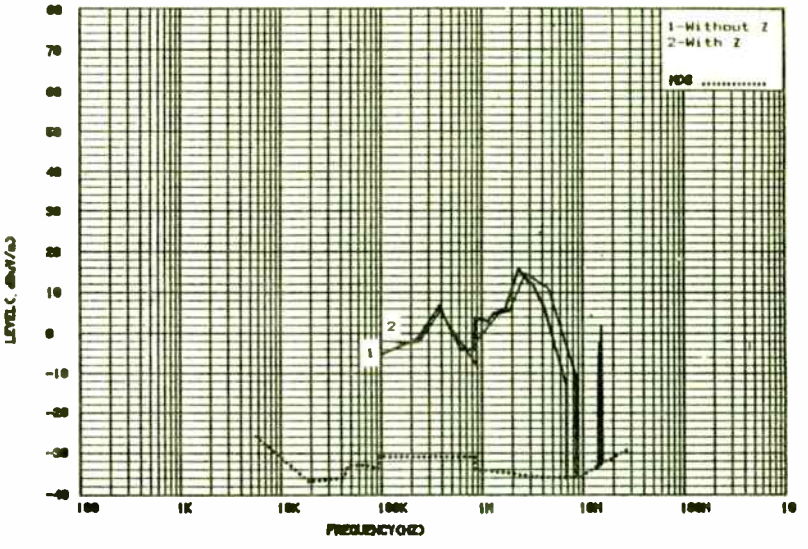


Figure 12. Affects of Z on the Radiation Profile of the 55-Line Cable with the Filterpin Connectors Used. Here the individual line-pair shield is terminated at the Source only and the overall shield is terminated at both ends.

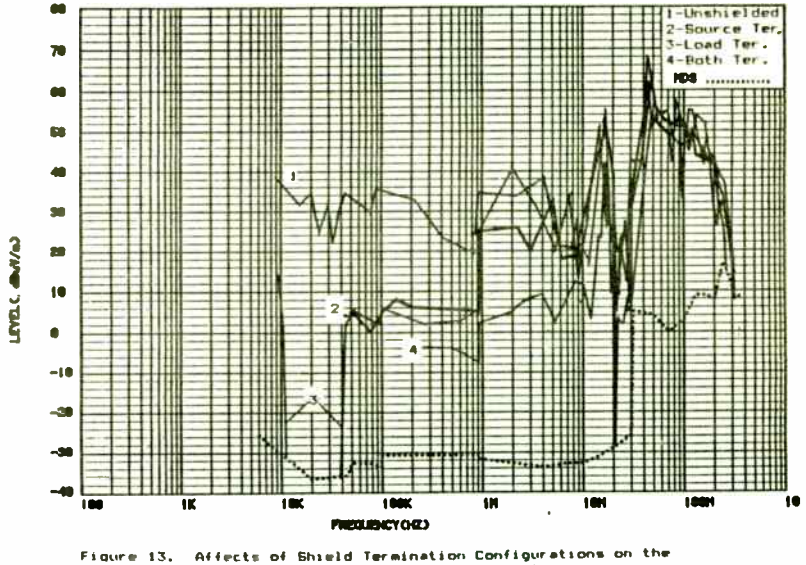


Figure 13. Affects of Shield Termination Configurations on the Radiation Profile of the 26-Line Cable.

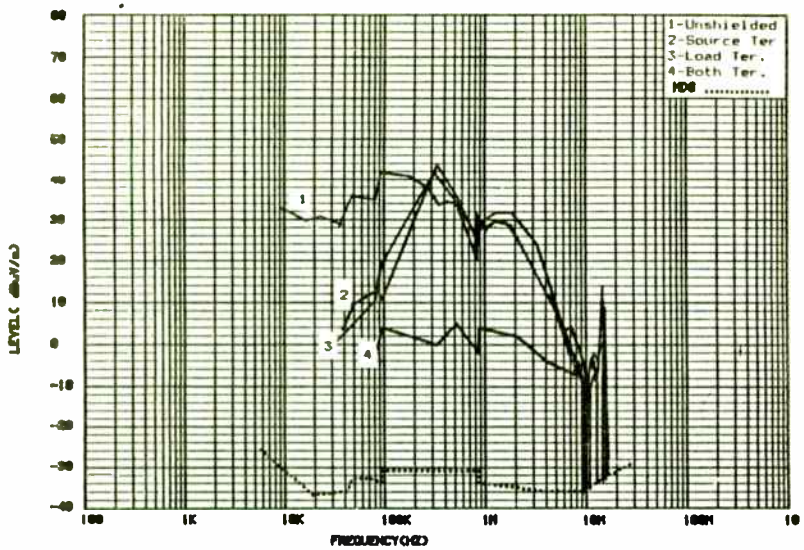


Figure 14. Affects of Shield Termination Configurations on the Radiation Profile of the 26-Line Cable with Filterpin Connectors Used.

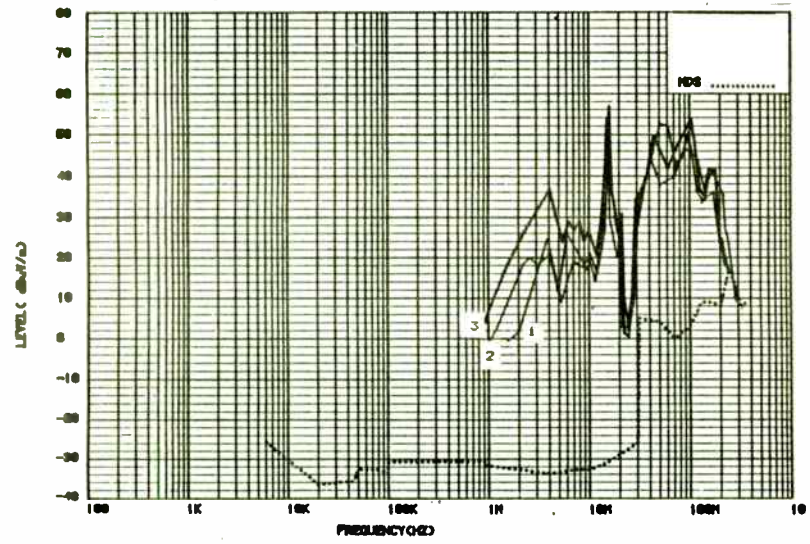


Figure 16. Affects of Shield Termination Configurations on the Radiation Profile of the 55-Line Cable. Here the profile resulting from both shields terminated at both ends (1) is compared to the cases where the line-pair shield is terminated only at the Source (2) or the Load (3) and the overall shield is terminated at both ends.

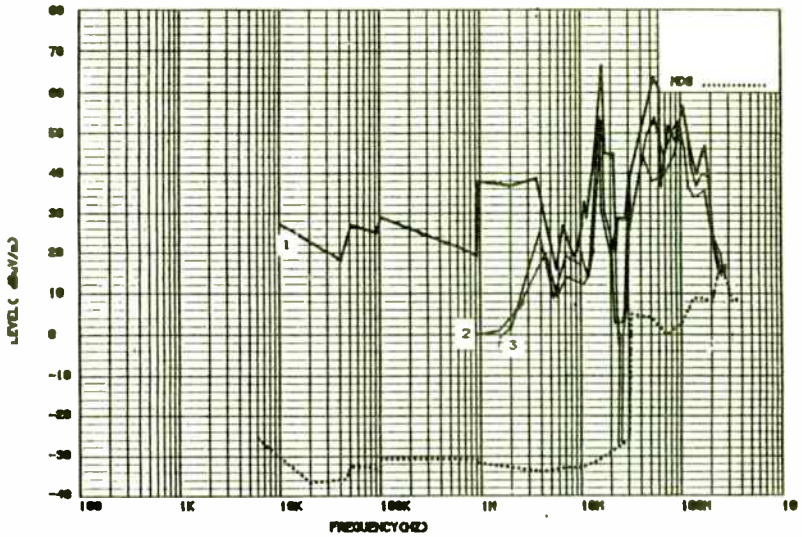


Figure 15. Affects of Shield Termination Configurations on the Radiation Profile of the 55-Line Cable. Here the unshielded profile (1) is compared to the cases where just the line-pair shield is terminated at both ends (2) and both shields are terminated at both ends (3).

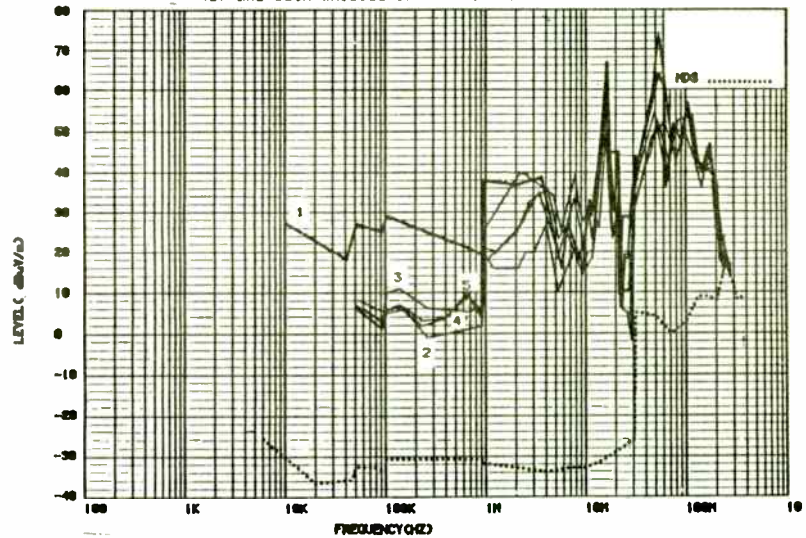


Figure 17. Affects of Shield Termination Configurations on the Radiation Profile of the 55-Line Cable. Here the unshielded profile (1) is compared to the cases where the line-pair shield is terminated at just the Source (2 and 5) or the Load (3 and 4) and the overall shield is left unterminated (2 and 3), terminated at just the Source (4), or terminated at just the Load (5).

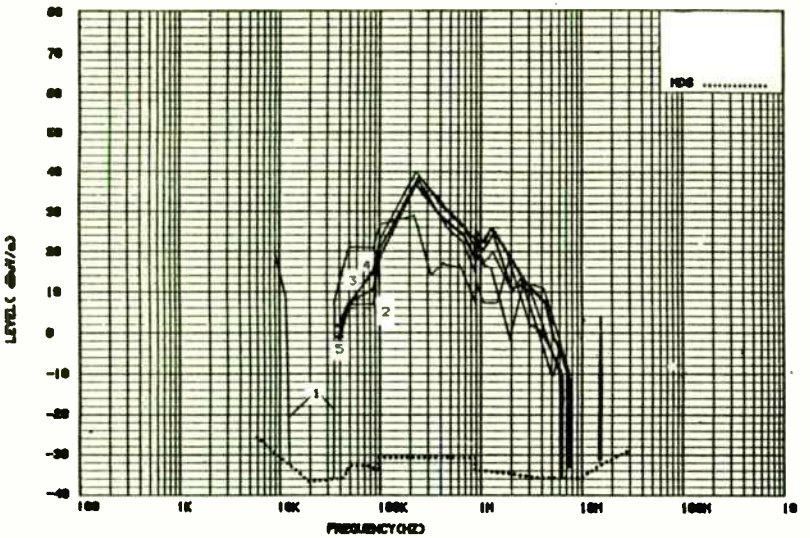


Figure 18. Affects of Shield Termination Configurations on the Radiation Profile of the 55-Line Cable with Filterpin Connectors Used. Here the unshielded profile (1) is compared to the cases where the line-pair is terminated at just the Source (2 and 5) or the Load (3 and 4) and the overall shield is left unterminated (2 and 3), terminated at just the Source (4), or terminated at just the Load (5).

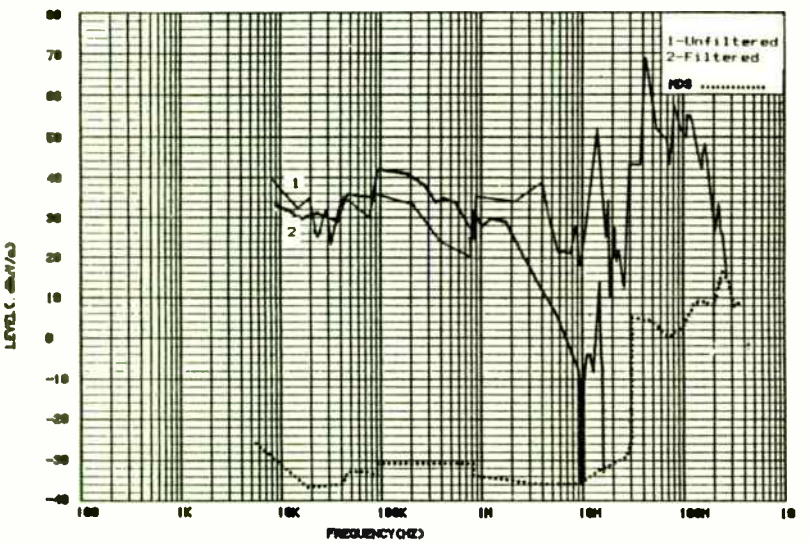


Figure 20. Affects of Filterpin Connectors on the Unshielded Radiation Profile of the 26-Line Cable.

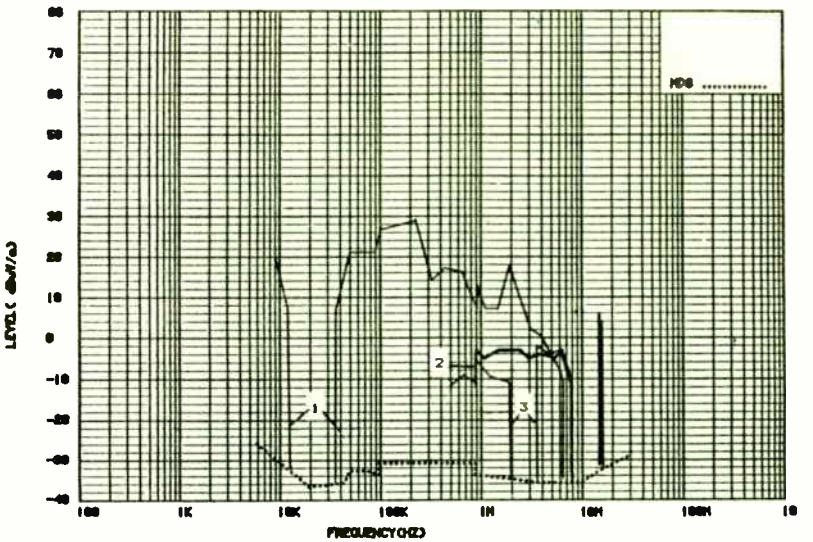


Figure 19. Affects of Shield Termination Configurations on the Radiation Profile of the 55-Line Cable with Filterpin Connectors Used. Here the unshielded profile (1) is compared to the cases where just the line-pair shield is terminated at both ends (2) and both shields are terminated at both ends (3).

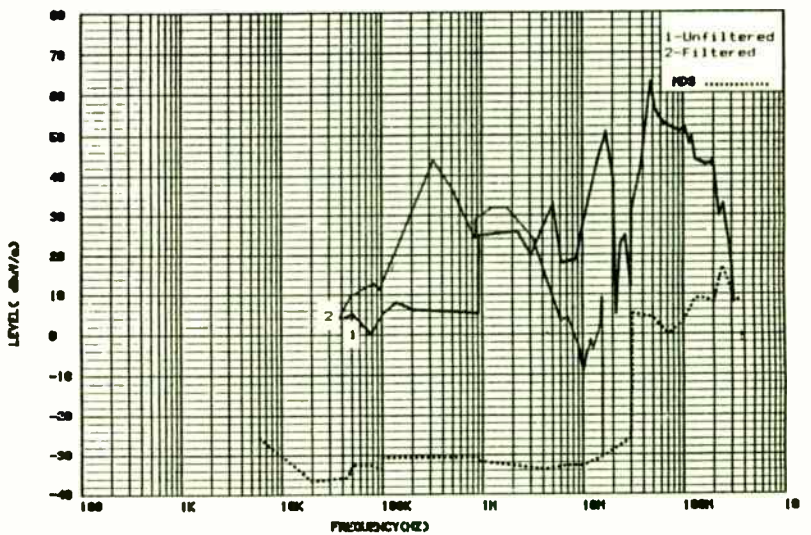


Figure 21. Affects of Filterpin Connectors on the Radiation Profile of the 26-Line Cable with the Cable Shield Terminated at Just the Source.

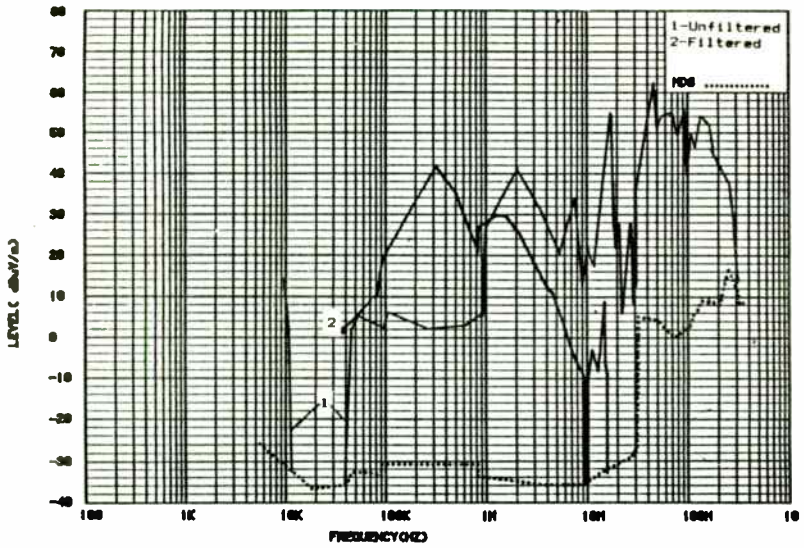


Figure 22. Affects of Filterpin Connectors on the Radiation Profile of the 26-Line Cable with the Cable Shield Terminated at Just the Load.

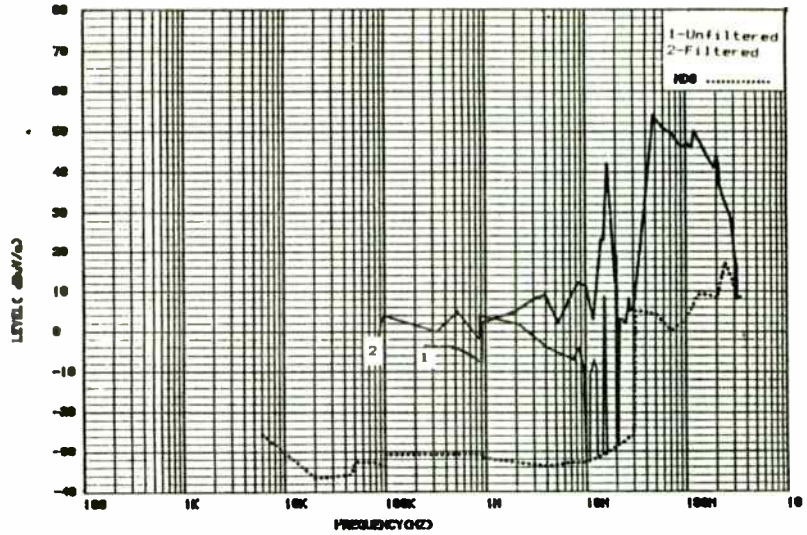


Figure 23. Affects of Filterpin Connectors on the Radiation Profile of the 26-Line Cable with the Cable Shield Terminated at Both Ends.

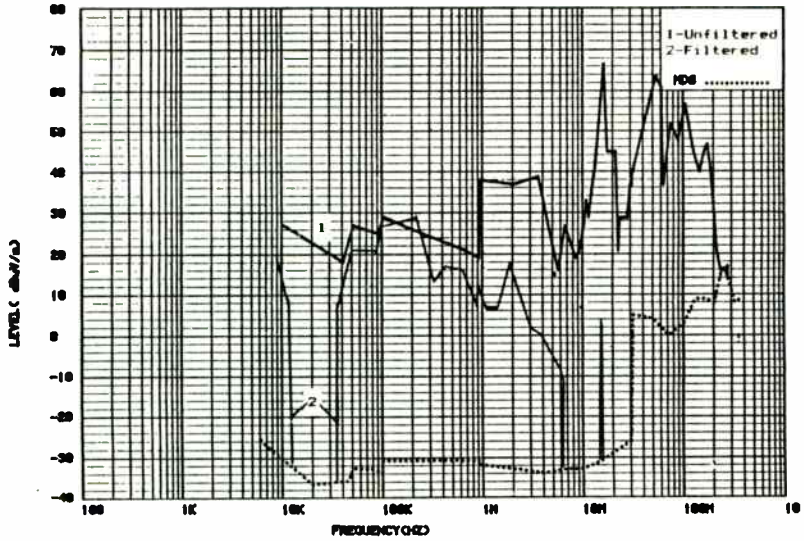


Figure 24. Affects of Filterpin Connectors on the Unshielded Radiation Profile of the 55-Line Cable.

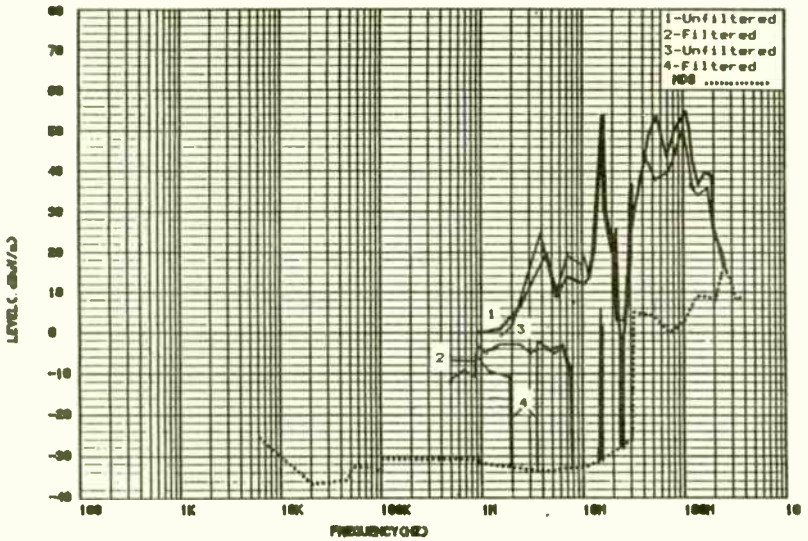


Figure 25. Affects of Filterpin Connectors on the Radiation Profile of the 55-Line Cable. Here the cases shown are with just the line-pair shield terminated at both ends (1 and 2) and with both shields terminated at both ends (3 annd 4).

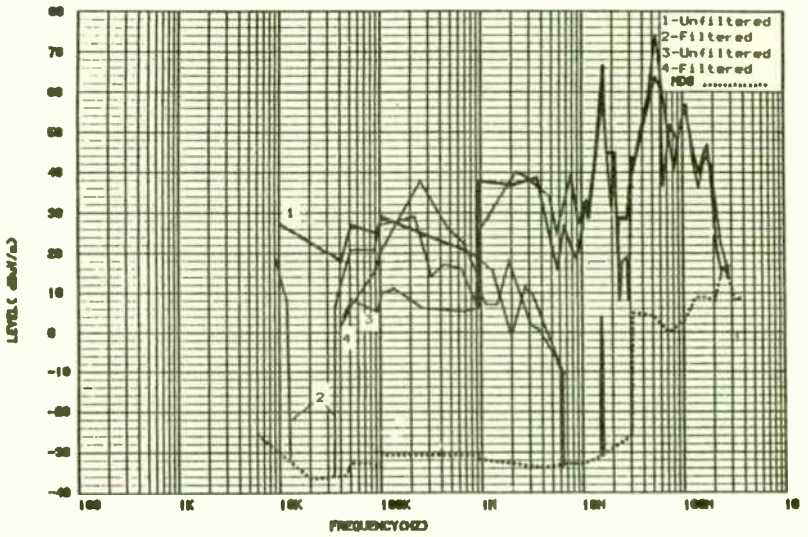


Figure 26. Affects of Filterpin Connectors on the Radiation Profile of the 55-Line Cable. Here the cases shown are for the unshielded profiles (1 and 2) compared to the profiles resulting from only the line-pair shield being terminated at the Source (3 and 4).

NEW INSIGHTS INTO 'OLD' NETWORK ANALYSIS TECHNIQUES

by
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Network Analyzers have been commonly used in the characterization of linear components such as filters, amplifiers, attenuators, switches, semiconductors, transmission lines and antennas over the RF and microwave frequency range. They measure the energy reflected from and transmitted through the device under test (DUT). By analyzing the amplitude ratios and phase differences between incident and the reflected and transmitted waves, the complete impedance and transmission characteristics of the DUT can be determined. Network analysis techniques started with slotted lines and gain-phase voltmeters at CW frequencies, but became popular as swept frequency characterization came about.

A network analyzer will always have four key parts:

1. A swept frequency source that provides the stimulus to the DUT.
2. A signal separation device that samples the incident, reflected, and transmitted signals to be measured.
3. A reciever to measure the amplitude and phase of the separated signals.
4. A display to show the data in rectilinear (Cartesian), polar or Smith Chart format.

See Figure 1. Network Analyzer Diagram

More recent network analyzers combine these elements into integrated packages for better performance and add significant enhancements. The following measurement applications areas are used to illustrate these new capabilities.

Filters

The high performance RF systems being designed are placing significant requirements on filter measurement accuracy.

One of the key elements is the frequency accuracy. Analog swept sources have great difficulty in measuring many modern filters (e.g. crystal and SAW) both because of their frequency accuracy and residual FM. Synthesizer sources are required, but at the expense of speed since they step along at CW intervals. Other techniques use a frequency counter to help guarantee accurate frequency information. Now network analyzers

incorporate swept synthesizers which offer the convenience of analog sweep and the precision of synthesizers at the same time.

SAW filter measurements are particularly difficult. Due to the different paths signals can take in the device, distortion in the frequency domain can occur which is very difficult to detect. These are called spurious time-domain responses. With their inverse Fourier transform ability, network analyzers can measure both the frequency and time-domain responses.

See Figure 2. SAW Filter Measurement in Frequency and Time Domain

Group delay measurement is often required to check for distortion. Previously, additional equipment was required that passed a modulated signal (FM or AM) through the DUT. Not only was this technique cumbersome, but often of unsuitable accuracy and repeatability from system to system. Deviation from linear phase was rarely used as a distortion parameter since it was almost impossible to equalize out the linear component of phase by simple methods. Now that network anlyzers incorporate a built-in computer, they can determine the DUT's group delay response more precisely from the phase information. This technique is fast and utilizes the accuracy enhanced data for the most accurate and repeatable results. In addition, deviation from linear phase is simple now with built-in electrical length control to balance virtually any length offset.

See Figure 3. Group Delay and Deviation from Linear Phase

Transistor S-Parameter Measurements

High frequency transistors are commonly used by RF engineers in their own designs. For the most part, they rely on manufacturers' measurements on an individual device. Typically, the set of S-parameter measurements are often incomplete leaving the user to measure his own. For these, the system measurement uncertainty can often be large. The errors due to imperfect couplers and non-ideal mismatches can add significantly. Using fixtures, adapters and cables only compounds the problem. Only by analyzing the errors and making worst-case assumptions does the designer know the uncertainties of his measurements. If these errors are large, they force him into designing with unnecessarily large safety margins. This can unnecessarily complicate things and also keep the end product from meeting its performance objectives.

Previously, the only alternative was to reduce the measurement errors by obtaining better hardware and reducing the number of adapters and cables between the measurement instrument

and the device. Generally, this isn't enough. Tuners can be employed at a particular frequency, but not over the wide bandwidths needed. Only until automatic network analyzers, driven by computers, could these uncertainties be further reduced. They offered a calibration technique called vector accuracy enhancement which used external calibration standards (open, short, load) to actually measure the measurement uncertainties and vectorially subtract them from the measurement data for very high accuracy. This was a popular technique with disadvantages of requiring a programmable network analyzer, a computer, and quite slow measurements.

Now complete vector accuracy enhancement techniques using short, open, and load calibration standards are built inside network analyzers to provide the low levels of uncertainty needed for the best device characterization. Once integrated inside, the measurement speed increased substantially allowing users the speed to see the measured parameters in real time. This technique also has the advantage of allowing very accurate measurements after adapters and in different connector types.

See Figure 4. Transistor Measurement Before and After Accuracy Enhancement

Antennae Measurements

When measuring antenna gain, match or patterns, extraneous or reflected signals can alter the data, giving erroneous results. This is why anechoic chambers usually are used to attenuate the unwanted signals.

Modern network analyzers now have the ability to transform their frequency domain data into time domain reponses using the inverse Fourier transform. With this, the unwanted reflections can be viewed and analyzed. If a particular portion of the time domain is all that is desired, a GATING function can mathematically filter out the undesired signals in time. This gated response can then be transformed back and allow analysis of the measurement in the frequency domain with the effects of unwanted reflections removed. This technique often can give results comparable to those obtained in anechoic chambers.

See Figure 5. Antenna Measurement in Frequency and Time Domain

See Figure 6. Antenna Measurement After GATING Unwanted Signal in Time and Frequency Domain

Fiber Optic Measurements

Fiber optic media is commonly used to transmit high speed

digital information. To characterize the transmission path and the components, pulse dispersion techniques using high speed pulse generators and high speed oscilloscopes are used.

Now that network analyzers can mathematically transform measured frequency domain information into the time domain, the same network anlyzer can be used to quantify the dispersion of pulses.

In summary, as the need for better network analysis by design engineers grows, so do the techniques available. Only recently have those techniques described here existed inside commercially-available network analyzers. They represent the latest steps in the steady improvement of measurement equipment to assist engineers with their design tasks.

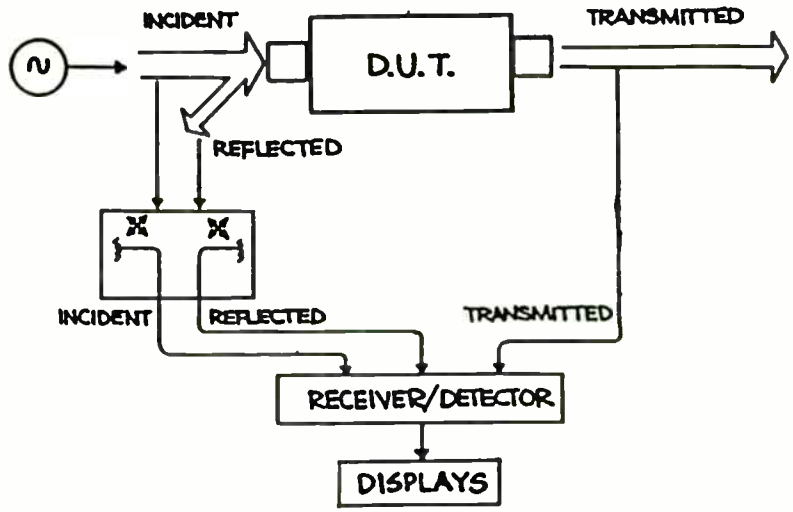

FIGURE 1. NETWORK ANALYZER

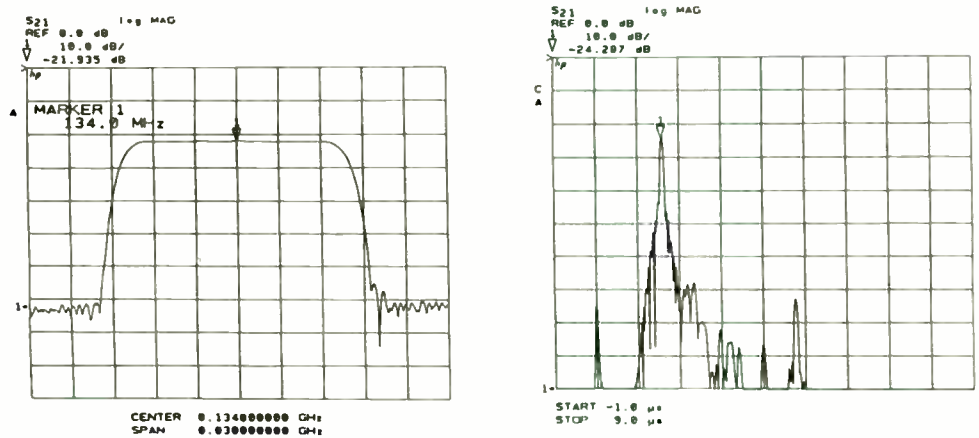

FIGURE 2. SAW FILTER MEASUREMENT IN FREQUENCY AND TIME DOMAIN

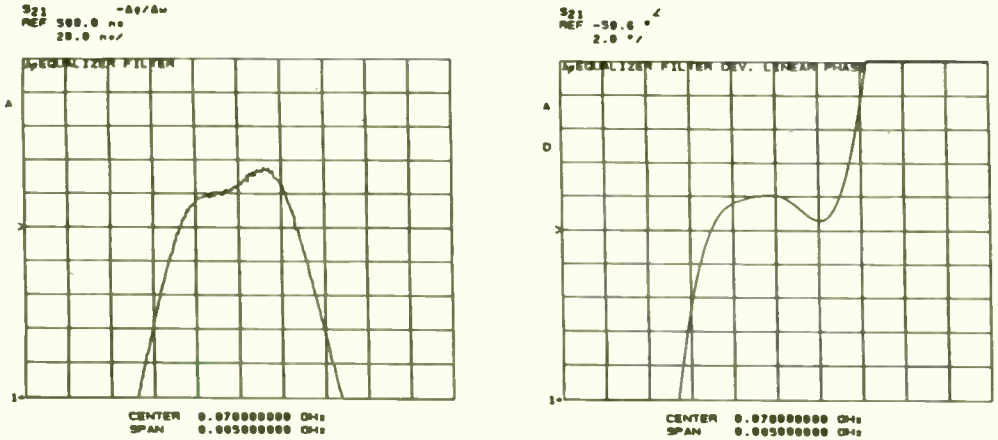

FIGURE 3. GROUP DELAY AND DEVIATION FROM LINEAR PHASE

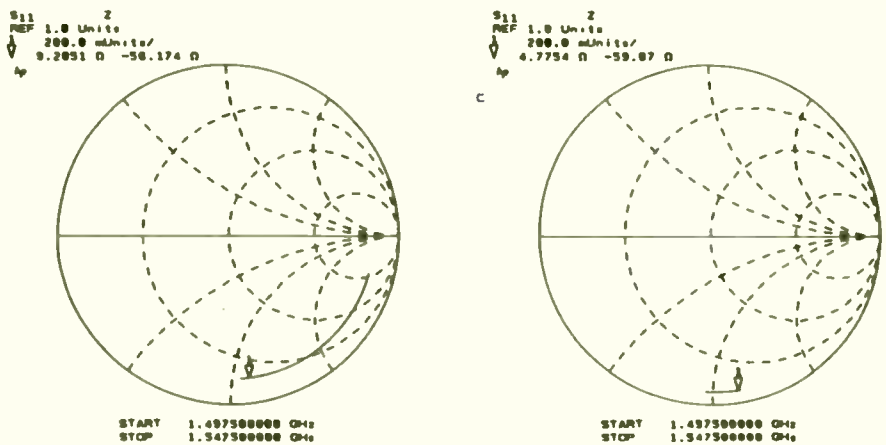

FIGURE 4. TRANSISTOR MEASUREMENT BEFORE AND AFTER ACCURACY ENHANCEMENT

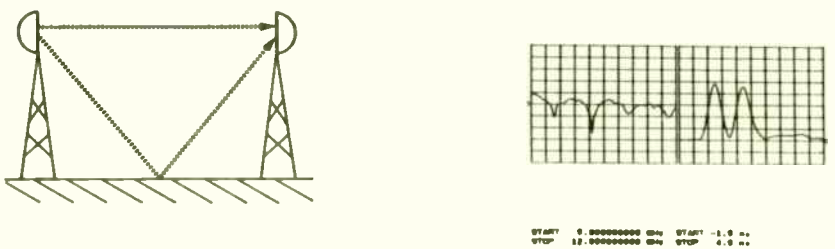

FIGURE 5. ANTENNA MEASURMENT IN FREQUENCY AND TIME DOMAIN

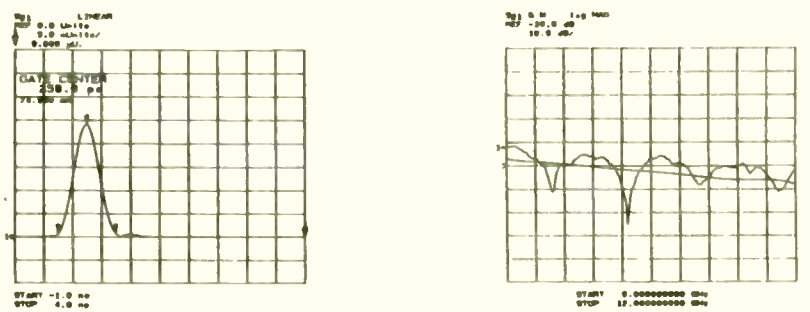

FIGURE 6. ANTENNA MEASUREMENT AFTER GATING UNWANTED SIGNALS IN TIME AND FREQUENCY DOMAIN

A BROADBAND LUMPED ELEMENT VARIABLE ATTENUATOR

by

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A bridged-T variable attenuator was realized in the 1 MHz to 500 MHz band with an attenuation range of about 13dB and a minimum return loss of 21 dB. Due to its small size, broadband operation and good match at both the ports a bridged-T attenuator was chosen.

In a bridged-T network (Fig.1.a) the two variable resistors have to satisfy the following condition for a good match at both the ports : $R_1 R_2 = Z_o$, where Z_o = characteristic impedance. PIN diodes can be used as current controlled variable resistors with resistance typically varying from 10 K ohms to 1 ohm above 20 Hz. Since the forward current in a diode is an exponential function of the voltage drop across the diode, when PIN diodes are used in the bridged-T circuit the product R_1R_2 will be an exponential function of (V_1+V_2) [1].

$$R_1R_2 = K_1 \ e^{KT/ (V_1 + V_2)},$$

where K_1 is a constant.

Hence for good match the sum of the voltage drops across the diodes has to be held constant. The DC circuit achieving this function is shown in Fig.1 (b). A_1 is a voltage follower stage which maintains a constant voltage drop across the diodes. A_2 and A_3 form control voltage stages, which vary the currents through the diodes for changing the attenuation.

Two important RF considerations in the realization of a broadband variable attenuator are (1) the design of proper layout to reduce parasitics (2) proper design of broadband DC to RF isolation elements. The attenuator was realized as per the layout shown in Fig.2 on a 31.25 mil thick Teflon fiberglass substrate with 50 ohms input and output microstrip lines. In this layout, the size of patches P_1 and P_2 has been minimised to reduce parasitics. M/S. Salford Electronics Ltd., core types P and K10 were used to realize the low frequency (1 MHz to 150 MHz) and high frequency (150 MHz to 500 MHz) chokes. One each of these high and low frequency chokes were used in series to obtain the broadband (1 MHz to 500 MHz) RF to DC islotion. Siemens type BA379 PIN diodes were used along with M/S. Johanson Chip capacitors and M/S. Pyrofilm 50 ohms chip resistors, to reduce the size. This attenuator had a minimum attenuation range of 0.8 dB to 13.8 dB with $\leq$1.2 dB response over 1 MHz to 500 MHz frequency range. It had a minimum return loss of 21 dB over the 1 MHz to 500 MHz band. The measured performance of the attenuator is given in Table I.

Table I. Measured Performance of the Bridged-T Attenuator

Freq. (MHz)	I/L (dB)	R/L (dB)	I/L (dB)	R/L (dB)	I/L (dB)	R/L (dB)
1	0.5	27	6.0	28	15.0	25
50	0.5	27	6.0	28	15.0	25
100	0.6	26	6.0	29	15.0	24
150	0.6	26	6.0	30	14.9	24
200	0.6	26	6.0	31	14.7	24
250	0.6	25	6.0	34	14.7	23
300	0.7	25	6.0	30	14.5	23
350	0.7	25	6.1	29	14.4	23
400	0.7	24	6.1	28	14.2	22
450	0.7	24	6.1	28	14.0	21
500	0.8	24	6.1	27	13.8	21

Reference: (1) Need a PIN diode attenuator ? R.S Viles Electronic Design, pp.100, Vol.25, No.7, March 29, 1977.

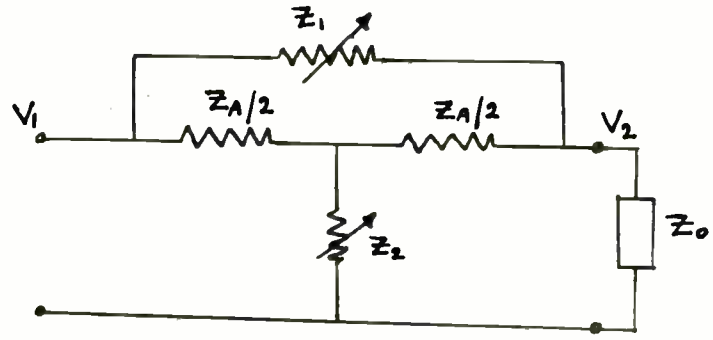

FIG.1(a). BRIDGED-T NETWORK

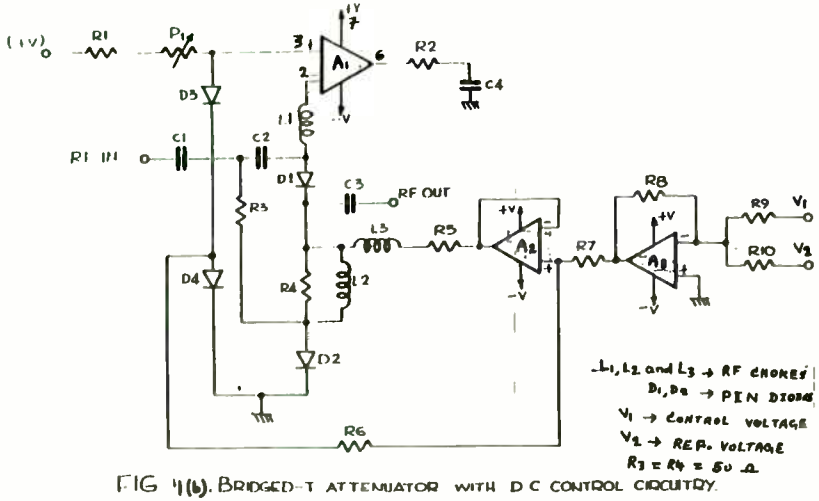

FIG 1(b). BRIDGED-T ATTENUATOR WITH D C CONTROL CIRCUITRY.

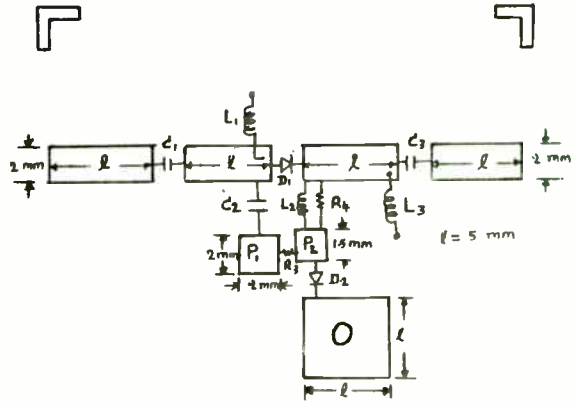

FIG.2. RF CIRCUIT OF THE BRIDGED-T ATTENUATOR

APPLICATION NOTES FOR DOUBLY ROTATED QUARTZ CRYSTALS

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SUMMARY

Piezoelectric crystal resonators are used primarily for precise frequency control and timing. The most frequently used piezoelectric material is alpha quartz (silicon dioxide). A quartz crystal acts as a stable mechanical resonator which, by its piezoelectric behavior and high Q, determines the frequency generated in an oscillator circuit. These bulk wave resonators are available in frequency ranges from approximately 1.0 KHz to 500 MHz.

For nearly half of a century two common crystalographic cuts, called AT and BT cuts, have been used extensively for most oscillator and filter applications. The electrical parameters and frequency vs temperature characteristics of these cuts are well known in the technical community.

Recently however, the dominance of the AT cut has been challenged by the newer doubly rotated crystal designs, especially in applications demanding precision frequency control. These doubly rotated designs are known as the IT and SC cuts.

INTRODUCTION

While retaining the more important advantages of the AT cut crystal, the doubly rotated units have proven to be superior in many ways. The doubly rotated cuts show less sensitivity to shock, vibration, acceleration, thermal shock and thermal hysterisis. Less sensitivity to processing and application variables such as electrode and mounting stress, and, more importantly, drive levels, have also given the doubly rotated cuts a significant advantage over the AT cut.

Many excellent papers with valuable data have been presented in preceding years, but the data was usually obtained from small quantity experimental groups. The data contained in this paper is based on larger quantities of 100 or more units of each frequency listed, and comprise only cylindrical type cold weld enclosures.

VIBRATIONAL SENSITIVITY

Although several papers have previously reported on the various influences on vibrational sensitivity, much of this initial work was performed on crystal resonators enclosed in a crystal holder known as a "ceramic flatpack".

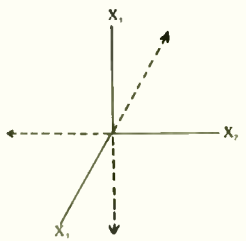
All of the crystals used for this paper were sealed in one of three types of cold weld enclosures: HC-35/u, HC-37/u or HC-40/u. All of these enclosures utilize a four point mounting configuration spaced at 90 degrees. From previous work, this mounting method appears to be optimum and correlates well with previous data from government sponsored ceramic flatpacks. Also, the static measurements of "g-tipover" on any given resonator typically correlate to less than 1×10^{-10}/g to its vibrational sensitivity measurement.

Vibrational sensitivity is a vector quantity in three dimensions, different in all axes. Measured differences can be as great as 10 to 1, but typically range from 2×10^{-9} to 1×10^{-10}. These differences are principally due to the moment of inertia acting upon the elastic coefficients of the quartz. Consistency in vector direction appears to have little correlation within a group. We have not found process differences, other than mounting and resonator geometry, to have any appreciable effect on sensitivity.

The quartz crystal resonator is, in reality, a mechanical device which, when mounted in a holder, is subject to mounting resonances. Further, oscillator design engineers must be aware of the possibility of resonances within the oscillator itself. Assuming no internal resonances within the crystal, the oscillator, or the system, the vibration gamma is flat up to 2000 Hz.

Much of our data is provided in the form of customer feedback, and is greatly appreciated for its value in comparison type measurements. Measurement techniques vary considerably from user to user, and differences in resultant gamma can arise dependent on whether the measurements were of the crystal itself, within an oscillator, or within a larger system.

CALCULATION OF VIBRATIONAL SENSITIVITY GAMMA



$$\Gamma = \sqrt{X'_1 + X'_2 + X'_3}$$

$$X_1 = (F_1 - F_2)10^{10}$$

Difference between frequency in one direction to its 180° (opposite) direction.

VIBRATIONAL SENSITIVITY MEASUREMENTS

FREQUENCY/MODE/CUT	g-SENSITIVITY
HC-35 HOLDER TYPE:	
5 Mhz/Fundamental/SC	3.9×10^{-10}/g +/- 1.0×10^{-10}/g
60 MHz/3rd Overtone/SC	3.5×10^{-10}/g (worst axis)
80 MHz/3rd Overtone/SC	$.95\times10^{-9}$/g (average)
95 MHz/5th Overtone/SC	1.9 to 7.7×10^{-10}/g
100 MHz/5th Overtone/SC	1.0 to 5×10^{-10}/g
100 MHz/3rd Overtone/SC	5 to 6×10^{-10}/g (worst axis)
118 MHz/5th Overtone/IT	3×10^{-10}/g (worst axis)
135 MHz/5th Overtone/IT	5.5×10^{-10}/g
HC-37 HOLDER TYPE:	
5 MHz/Fundamental/SC	$.4\times10^{-9}$/g
10.000 MHz/3rd Overtone/SC	Measurements have ranged from 3 to 6×10^{-10} gamma to 1.5×10^{-9} gamma
HC-40 HOLDER TYPE:	
10.000 MHz/3rd Overtone/SC	1.5×10^{-9}/g
5.000 MHz/3rd Overtone/SC	1.3×10^{-9}/g

PHASE NOISE

The doubly rotated cuts demonstrate still another area of superiority when utilized in a precision oscillator: phase noise and frequency stability.

It is well known that noise originates not only in the oscillator circuit but in quartz resonators undergoing excitation. Such "intrinsic" noise is believed to occur at various levels in all quartz resonators. While the mechanisms whereby this intrinsic phase noise is generated have yet to be identified and catalogued in their entirety, it is known that resonator Q (which is higher in the doubly rotated units) and frequency stability are inversely related in a statistical sense.

The phase noise of a signal can be measured only by a system which has equal or better noise performance. Relatively little has been published on the comparative noise performance of the AT cut vs doubly rotated resonators of similar fabrication, due in part to the fact that most crystal manufacturers are not equipped to measure the phase noise of quartz resonators. As a result, phase noise requirements appear on very few crystal drawings or specifications. However, the phase noise of crystal oscillators is intrinsically determined by the performance of the resonator. Therefore, phase noise measurements of the crystal oscillator circuits may be used to examine the phase noise performance of the crystals.

The close in phase noise of the crystal oscillator circuit is improved by the extremely high Q's developed in SC cut resonators. Also, the doubly rotated cuts may be operated, without damage or significant degradation, at substantially higher power than the AT cut, thereby directly facilitating a corresponding suppression of the white noise floor by approximately 10 dB/Hz.

Typically AT cuts will exhibit the tendency to "mode hop" or break up over the temperature vs frequency curve at drive levels in the area of 2 Mw. However, SC cuts designed for radar (CP2 applications operate at 8 Mw, and have immensely added to radar sensitivity.

Generally speaking for SC cut resonators, phase noise is 3 to 10db better than similarly prepared AT cuts. An example of a superior SC cut crystal oscillator appears below.

PHASE NOISE MEASUREMENT

5MHZ, 3RD OVERTONE, HC-40/U HOLDER TYPE:

Hz FROM CARRIER	NOISE LEVEL (dBc/Hz)
5	132.5
10	136.5
20	141.5
100	147.5
1,000	153.5
10,000	159.5
25,000	160.5

Figure 1 shows a comparison of measurements using 3rd overtone AT cuts and a 5th overtone AT cut AT 100 MHz with an average SC cut 3rd overtone performance curve.

Figure 2 shows a phase noise comparison of several 3rd overtone SC cut crystals with measurements made in different oscillators at different times with crystals from different manufacturers. Greater than 10 dB/Hz difference occurs within the phase noise performance of the SC cut oscillators vs that of the AT cut oscillators.

Conclusions to be derived would indicate a considerable difference in oscillator design, crystal design, or both.

AGING

Aging studies on AT and SC cuts (processed using similar manufacturing techniques) show that the SC typically ages into its final aging rate 5 to 10 times faster than the AT. The SC typically exhibits an improvement of 2 or 3 times in final aging rate. A 5.0 MHz, 3rd overtone SC cuts will typically reach 1×10^{-10}/day in less than 14 days.

A group of 10 MHz, 3rd overtone SC cuts, together with a group of similarly prepared 10 MHz, 3rd overtone AT cuts were subjected to repeated cold shock experiments. Soak times were approximately 10 hours of -30°C. The AT cuts showed frequency changes in parts in 10^{-7} and their subsequent aging rates were an order of magnitude poorer than prior to the cold soaks. The SC cuts however showed frequency shifts of parts in 10^{-9} and 10^{-10}, and the aging rate was not impaired.

SHORT TERM STABILITY

10 MHz/3rd Overtone/SC- cut/HC-37/u Holder Type:
500 second stability 1×10^{-9}

10MHz/3rd Overtone/SC-cut/HC-40/u Holder Type:
1 second stability 5×10^{-12}
.1 second stability 5×10^{-12}

CONCLUSIONS

Piezo Crystal Company has been investigating the advantages of doubly rotated cuts for more than ten years, and successfully manufacturing these units for the past five years. The proprietary manufacturing and testing systems developed by Piezo Crystal Company have virtually eliminated the production problems once associated with the doubly rotated cut crystals. Over 8,000 doubly rotated resonators have been fabricated to date, exclusive of several thousand "blanks only" provided for customers' final processing.

The development of the doubly rotated cuts has allowed the frequency control industry to expand its previous limitations hundredfold. The acceptance of this "new" technology in the RF world has been overwhelming. We at Piezo Crystal Company are committed to continuing the research and advancement of this technology, and sharing our gained knowledge with the technical community.

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1. D.J. Healey III and S.Y. Kwan, "*SC-cut Quartz Crystal Units in Low-Noise Oscillator Applications at VHF*", Proc. 35th Annual Symposium on Frequency Control, 1981.
2. Raymond L. Filler, John A. Kosinski, and John R. Vig, "*The Effect of Blank Geometry on the Acceleration Sensitivity of AT and SC-cut Quartz Resonators*", Proc. 36th Annual Symposium on Frequency Control, 1982.
3. Raymond L. Filler, John A. Kosinski, and John R. Vig, "*Further Studies on the Acceleration Sensitivity of Quartz Resonators*", Proc. 37th Annual Symposium on Frequency Control, 1981.
4. Grant Moulton, "*Analysis and Prediction of Phase Noise in Resonators and Oscillators*", RF and Microwave Measurement Symposium and Exhibition, 1984.
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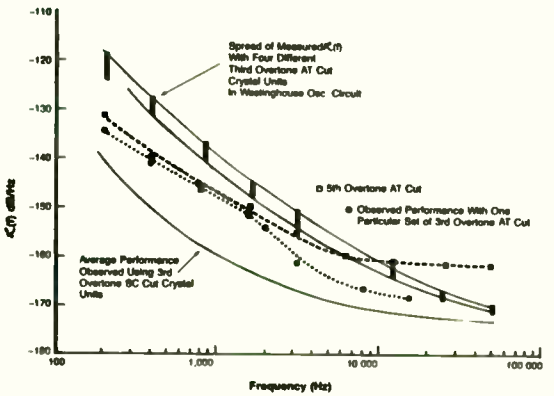


Figure 1. Comparison of ℒ(f) Displayed by Oscillator Using SC Cut and AT Cut Units Approximately 100 MHz

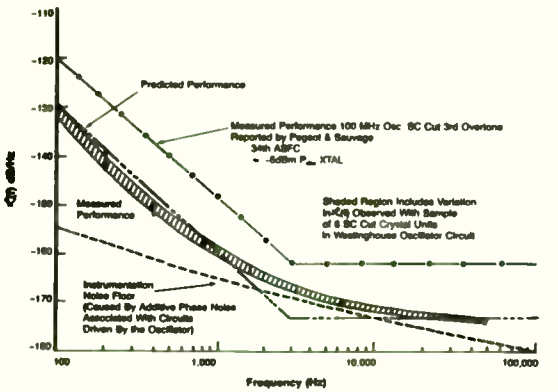


Figure 2. ℒ(f) Characteristics of Third Overtone SC Cut Crystal-Controlled Oscillators at Approximately 100 MHz

RF PLASTIC PACKAGE COMPARISON STUDY

KAMIL GRESKO

MOTOROLA INC.

SEMICONDUCTOR PRODUCTS SECTOR

DECEMBER 1985

TO-92
CASE 29
MPS571

SOT-89
CASE 345
MXR571

SOT-23
CASE 318
MMBR571
Standard and Low Profile

SOT-143
CASE 318B-01
MRF5711

Most manufacturers today are rapidly turning to use surface-mount components to utilize the full benefits of this relatively new technology. SMT's popularity has been accelerated by the development and availability of small outline semiconductor packages and device availability in these packages. Major manufacturers such as IBM, AT&T, GM and FORD are making significant investments in SMT.

The advantages and disadvantages between SMT and other technologies are already well known.

The objective of this article is to show the design engineers and other users some of the different aspects of SMT, make them aware of possible trade-offs and help them make the right decision.

Commonly cited advantages of SMT are:

* Space savings allowing smaller PC boards and total system size reduction
* Lower cost in high quantity
* Increased automation capability and wide choice of automated production equipment
* More reliable construction, better shock resistance and less sensitivity to vibrations
* Better high-frequency operation due to shorter lead lengths and interconnections

However, with decreased component and PC board size, an important factor which must be considered is thermal dissipation. Usually, the same die type is used in surface mounted devices as with conventional, "thru-hole" devices. The same bias conditions as used with the conventional devices will result in a higher die operating temperature for surface mount devices.

Consequently, miniaturization leads to thermal concentration.

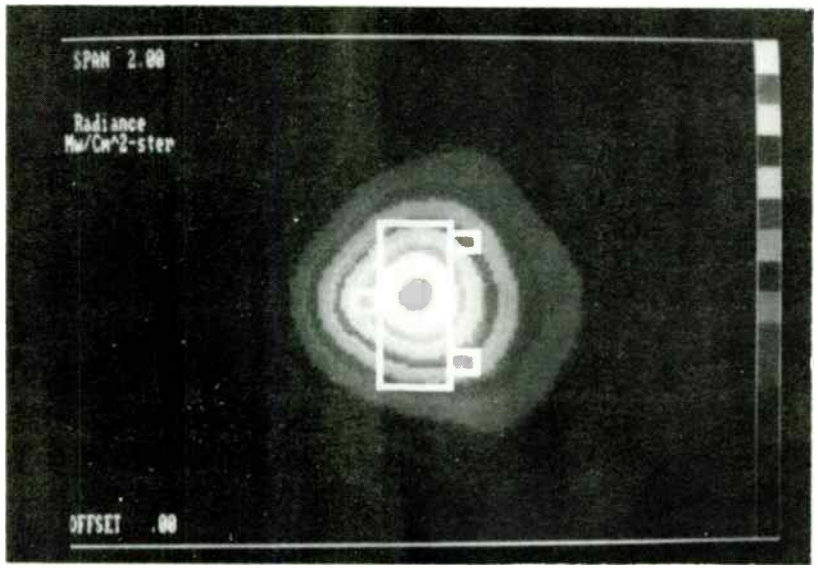


Fig. 1 Constant temperature zones surrounding SOT-23 transistor mounted on FR-5 PC board. Die temperature is 150°C.

The trade-off between the increase in component density and the concentration of thermal energy must be evaluated to avoid thermal collapse. Some of the most important information every design engineer needs to know is the thermal resistance of the package. The smaller the package is, the more important the die size consideration becomes. The following graphs, available in Motorola data sheets, describe thermal resistances for two different packages - SOT-23 and SOT-89.

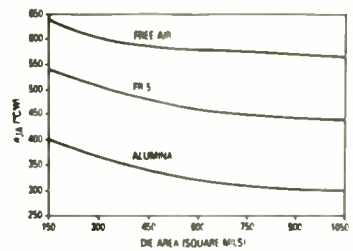


Fig. 2 Thermal resistance Θ_{JA}

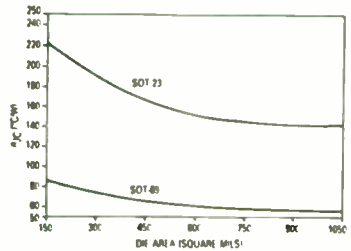


Fig. 3 Thermal Resistance Θ_{JC}

All these factors may have an influence on the choice of PCB material, number of layers, and the thickness of the BCB because Θ_{JA} is influenced by PCB material, thickness, etc.

The heat transfer from the die to the package, from the package to the PC board and then away from the board should be considered very cautiously in the design stage.

Things to be considered before starting are:

* Availability in a particular package.
* Package electrical-thermal consideration, to guarantee electrical and thermal requirements.

For example: If design of oscillator requires minimum f_T of 7.5Ghz the designer will probably refer to curve #18, which meets the requirement at collector current of 50mA. If V_{ce} is 10V the device will require power dissipation of 500 mW, obviously SOT-23 or SOT-143 are not suitable due to their power dissipation rating. The designer will have to chose between SOT-89 or TO-92 package.

Regardless of previous application devices like #12, 13, 14 curves will allow the designer to choose any package if electrical requirements are satisfied. Curve #11 shows that SOT-23 or SOT-143 is the most suitable package because a minimum power dissipation is required.

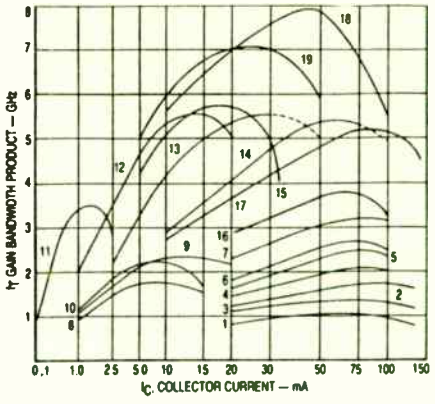


Fig. 4 Electrical parameter f_T versus collector current I_C

Other factors besides placement system and soldering methods are post assembly cleaning, visual inspection and test availability.

There are always a number of questions which must be answered in order to determine the optimal solution.

The purpose of this comparison is to find out the relative differences in performance that a particular transistor exhibits when encapsulated in the TO-92, SOT-23, SOT-89 and SOT-143 plastic packages. Package parasitic capacitances, lead frame construction and wire inductances are important factors in determining the ultimate application performance of the encapsulated transistor.

Fig. 5 TO-92 Internal Construction (Maximum die size 60 mil X 60 mil)

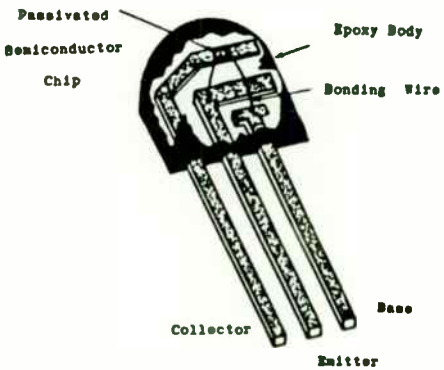


Fig. 6 SOT-89 Internal Construction (Maximum die size 60 mil X 60 mil)

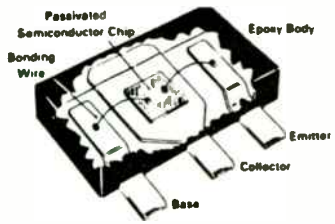


Fig. 7 SOT-23 Internal Construction (Maximum die size 30 mil X 30 mil)

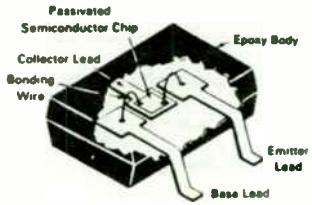
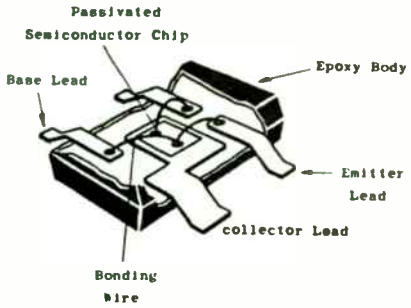


Fig. 8 SOT-143 Internal Construction (Maximum die size 30 mil X 30 mil)



An RF NPN bipolar chip which has relatively high gain and low noise characteristics at RF frequencies was chosen for this investigation. In silicon NPN transistors are usually preferred, since the electron mobility is higher than mobility of holes.

There were wafers selected from two different wafer lots and devices from each wafer were assembled in each of the four package. The intent was to obtain encapsulated transistors which were not only representative of the wafer line but which were similar enough that chip-to-chip variation was not a major question when the results were compared.

After DC testing, these four package groups of ten devices each were subsequently used for RF measurements.

RF transistors are represented by two-port networks and characterized by scattering, also known as S-parameters. S-parameters completely describe the behavior of two-port networks at RF and microwave frequencies. S-parameters are popular because they are easy to measure with modern Network Analyzers, their use in RF and microwave transistor amplifier design is conceptionally simple and they provide meaningful design information. All parameters mentioned in further consideration are measured in a 50 Ohm system, but a 75 Ohm system can be used as well. Of course, the values obtained using a 75 Ohm system measurement will not be identical to using a 50 Ohm system. It's up to the design engineer what measurement system serves his application.

Statistical processed data can be used for more advanced CAD design. On the other hand, it is very important to keep the parameters consistent over a long period of time, to guarantee the proper operation of circuit which design was based on that information. The reason to keep parameters consistent is the fact that the size of SMT PCB's is getting smaller and less space is left for relatively expensive and space consuming adjustment components.

Today's manufacturers, including Motorola, are implementing new process control methods to guarantee these parameters to full customer satisfaction.

The S-parameters for a transistor are reflection and transmission coefficients describing the input and the output in terms of power.

Transmission coefficients S_{12} and S_{21} are commonly called gains or attenuations. Reflection coefficients S_{11} and S_{22} relate to return loss, SWR and impedances.

The S_{12} parameter is the reverse transmission coefficient. Increasing magnitude of S_{12} with frequency indicates negative gain or loss due to package parasitics. In other words, S_{12} represents the output to input feedback of the transistor.

The S_{21} parameter is the forward transmission coefficient. As the frequency increases the magnitude of S_{21} decreases which indicates a decrease of insertion gain.

S_{11} parameter is the input reflection coefficient. As the magnitude of the reflection coefficient decreases the return loss and SWR improves. S_{11} indicates how well the input of a transistor matches to particular measurement system impedence. S_{11} measured in common emitter configuration is plotted in the reflection coefficient plane at specific bias conditions.

S_{22} is the output reflection coefficient. S_{22} is measured and plotted in the same manner as S_{11} except the input and the output are interchanged.

Many other parameters can be derived from S-parameters. Two figures of merit are commonly used by manufacturers to describe the transistor performance - Cut off frequency f_T and maximum frequency of oscillation f_{max}.

f_T - Cutoff frequency is the frequency where the short circuit gain $h_{fe}(\omega)$ approximates unity. The f_T is related to physical structure of a transistor by delay time τ_{ec}, which represents the sum of four delays encountered sequentially by the carriers as the flow from the emitter to the collector. Decreasing the base thickness will increase the f_T.

The other possibility to increase f_T is narrowing the collector region. However, there is always corresponding decrease in breakdown voltage by decreasing the collector width.

Therefore, every transistor is a result of compromise between high frequency operation and high breakdown voltage. The following formula is used to determine the frequency:

$$f_T = \frac{-2\,|S_{21}|}{(1-S_{11})(1+S_{22})(S_{12}S_{21})} f_m$$

S-parameters were obtained at measurement frequency f_m usually 100 MHz or 1 GHz.

f_{max} - maximum frequency of oscillation. It is a frequency where the maximum available power gain of the transistor G_{Amax} is equal to 1. G_{Amax} is the maximum power gain that can be realized without external feedback. G_{Amax} and f_{max} are measured by conjugately matching the source to the transistor input and the load to the transistor output impedance.

G_{Amax} - maximum available power gain. G_{Amax} is actually the ratio between power available from network and power available from source and is higher than the transducer gain $|S_{21}|^2$ because of the matching conditions and stability factors.

The following formula is used to determine G_{Amax} from S-parameters:

$$G_{Amax} = \frac{|S_{21}|}{|S_{12}|}(K + \sqrt{K^2-1})$$

A condition that a two-port network can be simultaneously matched with a positive real source and load is:

$K > 1$ or $C < 1$

C = Linvill factor

$$K = \frac{1 + |D|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}\,S_{21}|}$$

Where $D = S_{11}S_{22} - S_{12}S_{21}$

G_{Umax} - maximum unilateral power gain. G_{Umax} is based on the magnitude of S_{21} and the contributions of the conjugate matched networks to the input and output of the transistor.

$$G_{Umax} = \frac{|S_{21}|^2}{\left(1 - |S_{11}|^2\right)\left(1 - |S_{22}|^2\right)}$$

Where S_{11} 1 and S_{22} 1

or in logarithmic form,

$$G_{Umax} = 10\log\frac{1}{1 - |S_{11}|^2} + 10\log|S_{21}|^2 + 10\log\frac{1}{1 - |S_{22}|^2}$$

In all these unilateral assumptions, the S_{21} is set equal to zero, which makes the design procedure much simpler.

Three basic considerations are:

* Gain equal G_{Umax} regardless of noise figure
* Maximum possible gain at minimum N_F
* Design of an amplifier covering the frequency band with maximum gain and noise figure less than permissible by specification.

The meaning of f_T, f_S, and f_{max} is illustrated in the following figure. The gain rolls off at the rate of 6dB/octave.

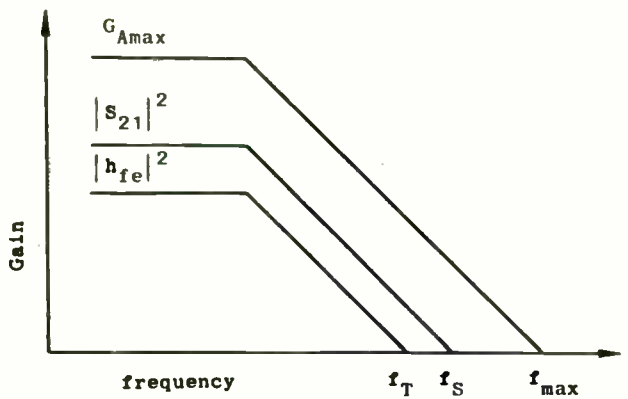


Figure 9 Frequency characteristics of G_{Amax}, $|S_{21}|^2$ and $|h_{fe}|^2$

Another parameter allowing qualitative comparison between Bipolar Junction Transistors (BJT) is the Noise Figure (NF). Expressed in dB, NF is a measure of the degradation in signal to noise ratio with passage of the signal through a given transistor.

Two sources of noise in a BJT are thermal noise and shot noise.

Thermal noise is caused by the vibration of the carriers in the ohmic resistance of the emitter, base and collector, due to their finite temperature. Some of the vibrations have spectral content within the frequency band and contribute noise to the signal.

Shot noise is a current dependent effect caused by the quantized and random nature of current flow. Current is not continuous but quantized being limited by the smallest unit of charge $q = 1.6 \times 10^{-19}C$. Particles of charge also flow with random spacing. Shot noise depends upon bias conditions.

From all that has been mentioned to this point, it is evident that right starting material and actual chip design are the most significant factors determing the transistor performance.

For better understanding of RF transistor characteristics it is necessary to use a model including all additional parasitic resistance, inductances and capacitances, which will depending on package, degrade the performance to a certain extent.

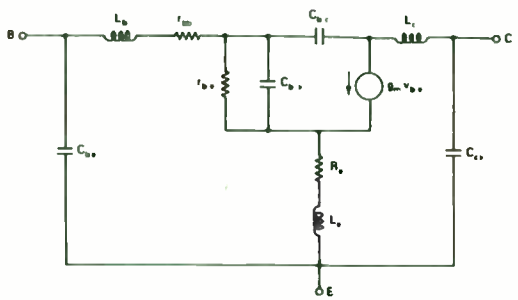


Fig. 10 A BJT common emitter model including parasitics

The resistance $r_{bb'}$ represents the base to emitter resistance. The $C_{b'e}$ capacitance is due to the junction from base to emitter. Emitter resistance R_e produces an inductive reactance across the base to emitter terminal, with increasing frequency, due to complex $h_{fe}(\omega)$. Since resistance associated with each region of transistor affect the various RC charging times, it is important to keep them to a minimum. Therefore, the metallization patterns contacting the emitter and base region must not present significant series resistance. There is always some contact resistance, but for simplicity will be left out of further consideration.

The package capacitance and wire inductance contributes most to coefficients variations at the higher frequencies. The meaning of the parasitic elements

L_b, L_e, L_C, C_{be} and C_{ce} is self-explanatory.

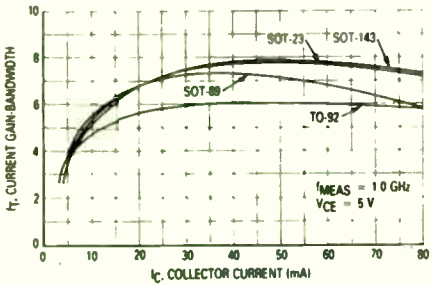
All of them are package dependent and will be determined by:

* size of a package
* material used
* lead frame construction
* lead frame material
* bonding method
* size of bonding wire

The transistor input and output capacitances are figures of merit that are commonly used and are easy to measure. Capacitance is a function of either emitter-base C_{iB}, collector-base C_{OB}, or collector-base with emitter AC wise shorted C_{CB} reverse voltages measured at 1 MHz.

All of these parameters and measurement results are compared and evaluated for all the packages in the following graphs and tables.

Current Gain-Bandwidth Product versus Collector Current



F_T VS. I_C

This graph shows the relationship between the current gain-bandwidth product and collector current (I_C) @ V_{CE} = 5.0V. The F_T values are calculated from S-parameters measured at 1.0 GHz.

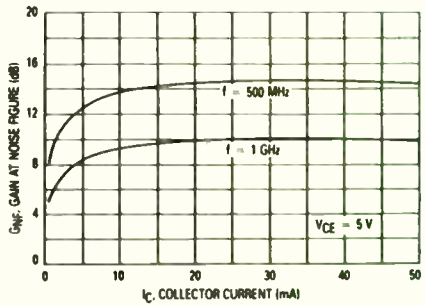
The graph shows that the SOT-23 and SOT-143 packages have the highest F_T values of all the package types and are essentially equal over the entire range of I_C. The curves are basically flat from 30 to 60 mA and have a value of approx. 7.8 GHz @ 50mA. The slight "roll off" starts after I_C reaches approximately 60 mA.

The SOT-89 package shows an intermediate value of F_T with a value of approx. 7.2 GHz @ 50 mA. The curve "rolls off" or decreases in value with an increase in I_C from 30 to 80 mA. The "roll off" is generally caused by the decrease of effective base thickness at higher current levels.

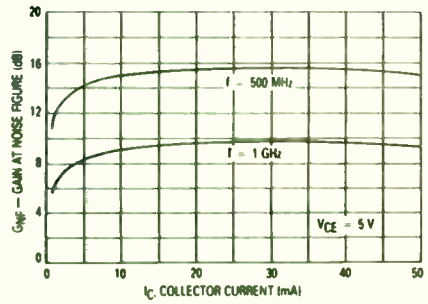
The TO-92 package shows the lowest value of F_T as a function of I_C with F_T equal to 6 GHz at 50 mA. This is approximately 2 GHz down from the SOT-23 and SOT-143 and approx. 1 GHz down from the SOT-89. The curve is flat from 30 to 80 mA. No rolloff is seen with increasing I_C, possibly due to package power handling capability.

Gain at Noise Figure versus Collector Current

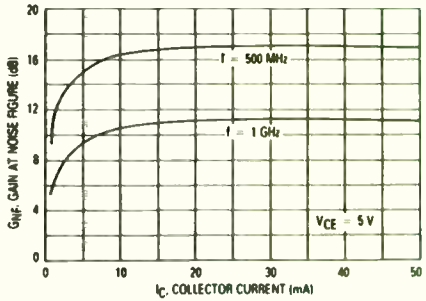
(a) TO-92 MPS571



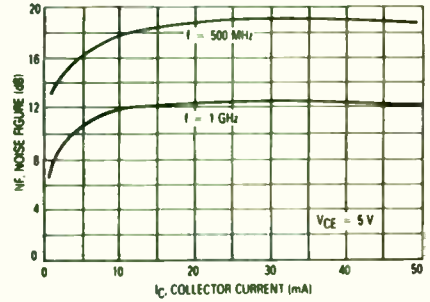
(b) SOT-89 MXR571



(c) SOT-23 MMBR571



(d) SOT-143 MRF5711



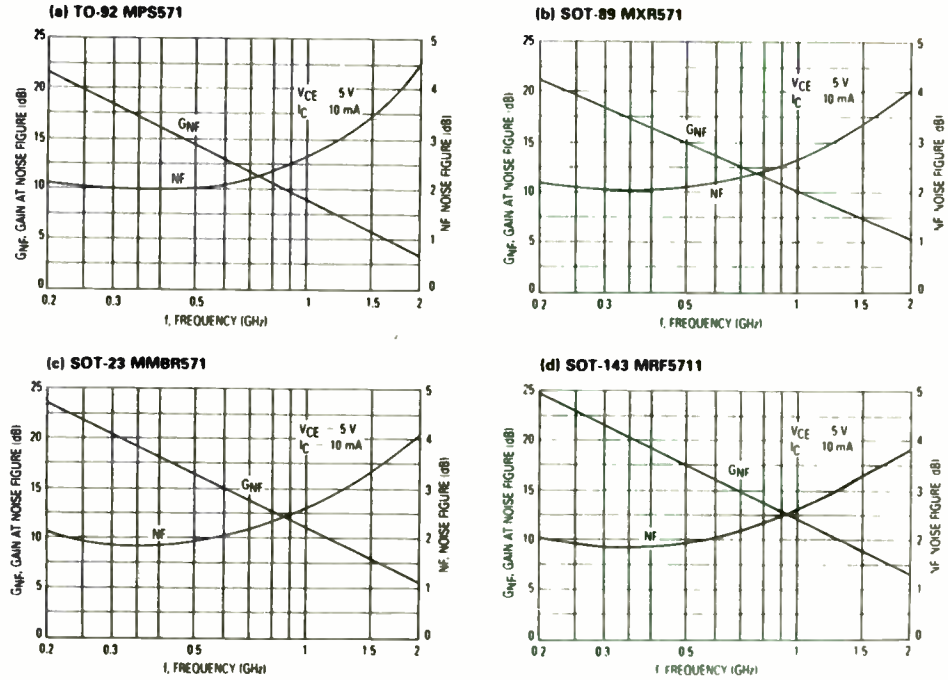
G_{NF} VS. I_C

These curves show the relationship between the gain obtained at minimum noise figure (G_{NF}) as a function of collector current (I_C) measured at the frequencies of 500 MHz and 1.0 GHz. In general, the curves show that the gain is flat for collector currents greater than 20 mA and that the gain at 500 MHz is obviously higher than the gain at 1.0 GHz for all packages.

Considering the family of curves at 500 MHz, the SOT-143 shows the highest gain with G_{NF} equal to 19 dB @ 30 mA. The SOT-23 is next in value with a G_{NF} of 17 dB @ 30 mA. The SOT-89 is next in value with a G_{NF} of 15.5 dB @ 30 mA followed closely by the TO-92 which is just under 15 dB @ 30 mA. There is a 4 dB difference between the lowest curves TO-92/SOT-89 and the highest SOT-143, with the intermediate curve SOT-23.

At 1.0 GHz, SOT-143 again shows the highest gain with a G_{NF} of approx. 12.5 dB @ 30 mA. SOT-23 is the next highest in value with a G_{NF} of approx. 11.5 dB @ 30 mA. Again, the TO-92 and SOT-89 have the lowest values of G_{NF} with TO-92 equal to approx. 10 dB and SOT-89 equal to approx. 9.5 dB @ 30 mA. It is significant to note that the family of curves at 1.0 GHz are more "compressed" than at 500 MHz; there is a spread of only 2 dB between the lowest and highest valued curves at 1.0 GHz compared to the 5 dB spread at 500 MHz.

Gain at Noise Figure and Noise Figure versus Frequency



G_{NF} VS. FREQUENCY AND N_F VERSUS FREQUENCY

Straight LINES in the graphs show the decrease in G_{NF} with frequency for all four packages with the collector current fixed at 10 mA.

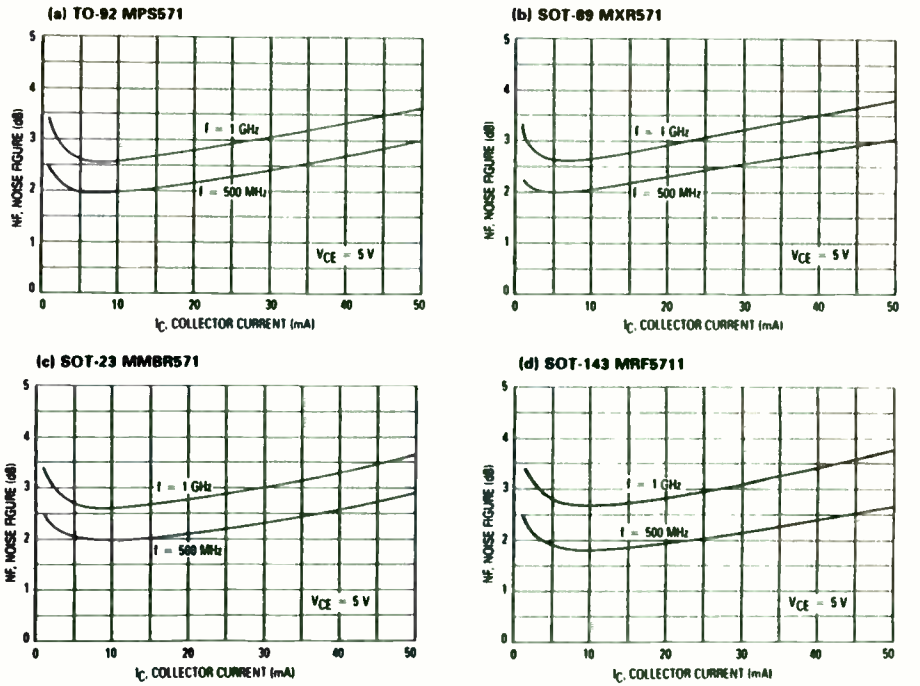
At this level of collector current, the SOT-143 shows the highest value of G_{NF} as a function of frequency although the SOT-23 is within approx. 1 dB of the SOT-143 over the range of frequencies measured to 1.5 GHz. The graph shows a value of approx. 12 dB for the SOT-143 and approx. 11 dB for the SOT-23 @ 1.0 GHz.

At frequencies less than 500 MHz, the TO-92 shows a slightly higher gain than the SOT-89. These packages reverse relative positions at frequencies greater than 500 MHz with the TO-92 having a slightly lower gain than the SOT-89. At 1.0 GHz, the SOT-89 shows a value of approx. 10 db while the TO-92 shows a value of approx. 9 dB. Over the entire range of measured frequencies, all the curves are within a 3 dB band.

CURVES in graphs show the variation of noise figure N_F with frequency for all four packages at a fixed value of collector current (10 mA). The curves show the expected result that N_F is basically flat for frequencies less than 500 MHz and increases steadily with frequency beyond 500 MHz.

All four package types are within a relatively narrow band of 0.2 dB or less over the measured range of frequencies. From all this it is evident that N_F is determined by wafer process, resistivity of starting material, and is most likely not package dependent.

Noise Figure versus Collector Current



N_F VS. I_C

These graphs show the variation of noise figure with collector current for all four packages at the two fixed frequencies of 500 MHz and 1.0 GHz.

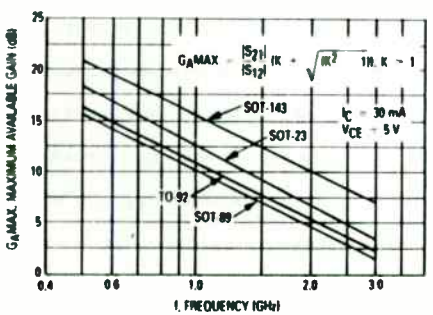
This family of curves shows the expected decrease in N_F with increasing I_C at relatively low current levels (less than 5 mA), a minimum in the region of 5 to 10 mA, and a steady increase in N_F with increasing I_C greater than 10 mA. The curves also show the expected result that the transistor N_F is higher at higher frequencies.

At both frequencies measured, the SOT-89 package appears to have a slightly higher N_F than the other packages. At a given frequency, the packages are within a maximum of 0.2 dB of each other.

At 500 MHz, the curves show a value of approx. 2 dB with I_C = 10 mA. For 50 mA, the curves show a value of approx. 3 dB for all four packages.

At 1.0 GHz, the curves show a value of approx. 2.6 dB with I_C = 10 mA. For 50 mA, the curves show a value of approx. 3.7 dB.

Maximum Available Gain versus Frequency



G_A MAX VS. FREQUENCY

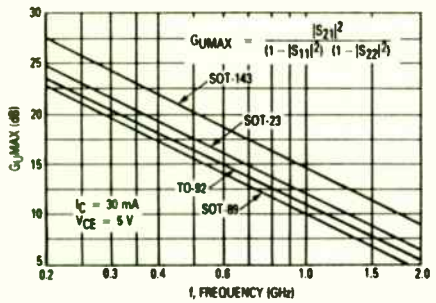
Maximum available gain G_AMAX is a gain which is calculated from S-parameters. The defining equation is shown on the graph. The curves show the expected decrease in G_AMAX with frequency.

The SOT-143 package shows the highest value of G_AMAX over frequency. The curve shows a value of approx. 21 dB @ 500 MHz.

The SOT-23 package shows the next highest G_AMAX and appears to have a slightly greater slope than the SOT-143. The curve shows a value of approx. 18 dB @ 500 MHz. Over the frequency range actually measured (500 MHz to 2.0 GHz), the SOT-23 is approximately 3 dB down from the SOT-143.

The TO-92 is the next curve down although it is very close to the SOT-89 curve. The curves are 0.8 dB apart. From the curves, the TO-92 has a G_AMAX of approx. 16.5 dB and the SOT-89 approx. 15.3 dB @ 500 MHz. The SOT-23 is approx. 2.5 dB higher than the TO-92 and SOT-89 @ 500 MHz, and approx. 1.5 dB higher than the TO-92 and SOT-89 at 2 GHz.

INSERTION GAIN versus FREQUENCY



G_{Umax} VS. FREQUENCY

Maximum unilateral power gain G_{Umax} is slightly lower than maximum available gain G_{Amax}.

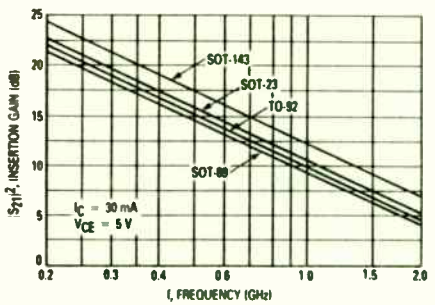
Formula defining G_{Umax} is simpler compared to G_{Amax} because it does not take stability factors into consideration. Compared to $|S_{21}|^2$ the unilateral gain is higher because input and output mismatches are taken into account deriving this number.

Again, the package performance curves are in the same order as G_{Amax}.

SOT-143 package shows the highest value of G_{Umax} over frequency, and value of approximately 20 dB at 500 MHz.

The next is SOT-23 with approximate value of 17.5 dB at 500 MHz followed by TO-92 16.5 dB and SOT-89 approximately 16 dB at 500 MHz. The curves are abut 4 dB apart.

Insertion Gain versus Frequency



$|S_{21}|^2$ VS. FREQUENCY

The insertion gain $|S_{21}|^2$ is a gain parameter calculated from the forward transmission coefficient S_{21} of the transistor. The quantity is less than G_AMAX since the gain (or decrease in loss) of the transistor achieved by input and output matching is not considered. The graph shows the decrease of insertion gain with increasing frequency.

All of the curves are approximately parallel which means that $|S_{21}|^2$ decreases at a constant rate with frequency for all four package types. The SOT-143 shows the highest value of $|S_{21}|^2$ followed by SOT-23, TO-92, and SOT-89 in decreasing order.

Considering the SOT-143 curve as a reference, the SOT-23 is approx. 2 dB down, the TO-92 is approx. 2.4 dB down, and the SOT-89 is approx. 2.8 dB down.

DYNAMIC PARAMETERS SUMMARY

Parameter	Conditions	Unit	Package			
			TO-92	SOT-89	SOT-23	SOT-143
f_T	50 mA 1.0 GHz	GHz	6.0	7.2	7.7	7.8
G_{NF}	10 mA 500 MHz 10 mA 1.0 GHz 30 mA 500 MHz 30 mA 1.0 GHz	dB	13.6 9.4 14.6 9.9	14.9 9.3 15.4 9.5	16.4 10.6 17.0 11.3	17.8 12.0 19.1 12.1
N_F	10 mA 500 MHz 10 mA 1.0 GHz 30 mA 500 MHz 30 mA 1.0 GHz	dB	2.0 2.6 2.4 3.0	2.1 2.7 2.6 3.2	2.0 2.6 2.4 3.0	1.8 2.7 2.3 3.1
G_AMAX	30 mA 500 MHz 30 mA 1.0 GHz 30 mA 2.0 GHz	dB	16.1 10.5 5.4	15.5 10.2 5.4	18.4 11.9 6.9	20.8 15.5 10.0
$\|S_{21}\|^2$	30 mA 500 MHz 30 mA 1.0 GHz 30 mA 2.0 GHz	dB	15.2 9.7 4.6	14.6 9.1 4.2	16.0 10.5 5.3	17.5 12.0 6.8
C_{ib}	1.0 V 1.0 MHz 2.0 V 1.0 MHz	pf	2.5 2.0	1.4 1.2	1.9 1.4	2.2 1.6
C_{cb}	5.0 V 1.0 MHz 10.0 V 1.0 MHz	pf	0.8 0.7	0.9 0.8	0.9 0.8	0.7 0.5

The next series of graphs are S-parameter plots for each of the four packages.

The scattering parameters are plotted as functions of frequency for a collector current value of 30 mA and a collector-emitter voltage of 5V. S-parameters for every package are listed in table form below the SMITH CHART and Polar Plot.

In the discussion that follows, each of the four S-parameters (S_{11}, S_{22}, S_{21}, S_{12}) will be considered separately.

S_{11}

This parameter is the input reflection coefficient of the transistor. This parameter, along with S_{22} which is the output reflection coefficient, can be plotted in the reflection coefficient plane as complex impedances known as a SMITH CHART.

An examination of the SMITH CHARTS for all the packages shows that SOT-89 and TO-92 have similar resistance components with a magnitude of 26 to 32 Ohms over the frequency range of 0.2 to 2 GHz. Both devices have capacitive reactance approximately equal in value for frequencies under 500 MHz. At 500 MHz and up, the reactance becomes inductive with the TO-92 increasing at a faster rate than SOT-89. At 2.0 GHz, the TO-92 has a inductive reactance of 46 Ohms while the SOT-89 has a reactance of 31 Ohms.

The SOT-23 has a resistance of 21 to 22 Ohms from 200 MHz to 2.0 GHz. The SOT-23 has a capacitive reactance of 12.5 Ohms @ 200 MHz which decreases in magnitude with frequency becoming zero at just over 500 MHz. At higher frequencies, the inductive reactance of the input impedance increases to a value of 17 Ohms @ 2.0 GHz.

The SOT-143 has the lowest value for the resistance of all the packages ranging in magnitude from 11.5 to 13.5 Ohms from 200 MHz to 2.0 GHz. The capacitive reactance with a value of 12 Ohms at 200 MHz decreases in magnitude to zero at just over 500 MHz. As the frequency increases the inductive reactance increases to a value of 18 Ohms @ 2.0 GHz.

The differences in resistive portions of input impedance are very possibly due to bonding wire length (TO-92 vs. SOT-23). Since SOT-143 uses two bonding wires for the emitter leads the resistive portion is even lower than the SOT-23.

S_{22}

As mentioned previously, S_{22} is the output reflection coefficient which can be mapped on to the SMITH CHART as a complex impedance.

The TO-92 has a resistance which decreases in value from 55 to 40 Ohms from 200 MHz to 2.0 GHz. The reactance is capacitive at 200 MHz with a value of 28.5 Ohms and decreases in magnitude reaching zero at just over 1.0 GHz. The reactance increases in inductance with frequency to a value of 22 Ohms @ 2.0 GHz. The TO-92 is the only package of all the package types which shows a positive (inductive) reactance; all other packages remain capacitive to 2.0 GHz.

The SOT-89 has a constant resistance component of approximately 50 Ohms from 200 MHz to 500 MHz. Above 500 MHz, the resistance abruptly decreases in value with frequency reaching a value of 36.5 Ohms @ 2.0 GHz. The capacitive reactance is 23 Ohms at 200 MHz and decreases in magnitude to 5.5 Ohms @ 2.0 GHz.

The output impedance of the SOT-23 has a resistance component which decreases in value from 45 Ohms @ 200 MHz to 41 Ohms @ 2.0 GHz. The reactance remains capacitive over the entire frequency range which changes in value from 25 Ohms @ 100 MHz to 3 Ohms @ 2.0 GHz.

The SOT-143 has the lowest resistance of all four package types decreasing in value from 36 Ohms @ 200 MHz to 31.5 Ohms @ 2.0 GHz. The reactance component remains capacitive over the frequency range which change sin value from 27.5 Ohms @ 100 MHz to 6 Ohms @ 2.0 GHz.

S_{21}

The S_{21} parameter is the forward transmission coefficient of the transistor. The magnitude of S_{21} as mentioned before decreases with frequency at the rate of 6 dB per octave.

The SOT-143 package has the highest value for the magnitude of S_{21} over the entire frequency range. The SOT-23 is next in value followed by the TO-92 with the SOT-89 having the lowest value. All the package types show the largest decrease in value from 200 MHz to 500 MHz.

At 1500 MHz, all of the packages have a magnitude for S_{21} between 2 and 3. The SOT-143 has highest value of 2.74 while the SOT-89 has the lowest value of 2.02. The SOT-23 has a value of 2.29 and the TO-92 a value of 2.11.

At 2.0 GHz, the SOT-143 is the only package with a magnitude for S_{21} greater than 2 (2.20). SOT-23 shows a value of 1.84, followed by TO-92 with a value of 1.70. The SOT-89 is the lowest with a value of 1.62.

The phase of S_{21} decreases for all packages with TO-92 showing the greatest overall change. It changes from 99° @ 200 MHz to 11° @ 2.0 GHz. The TO-92 phase angle is close in value to the SOT-89 for frequencies up to 500 MHz. Above 500 MHz, the phase angle for the TO-92 decreases faster than the SOT-89. Over the entire frequency range, the phase angles for the SOT-23 and the SOT-143 packages stay close together in value.

S_{12}

The S_{12} parameter is the reverse transmission coefficient. Roughly speaking, S_{12} represents the output to input feedback of the transistor. It is desirable to keep this low value at minimum.

At 200 MHz, all packages show a similarity in magnitude for S_{12}. The SOT-143 is the lowest with a value of 0.03 followed by SOT-23 which will have a value of 0.04. Both the TO-92 and SOT-89 have a magnitude of 0.05.

As the frequency increases to 500 MHz, the magnitudes all increase and begin to diverge in value. Both TO-92 and SOT-89 increase to 0.11, while the SOT-23 increases to 0.09. The SOT-143 remains the lowest in value with a magnitude of 0.05.

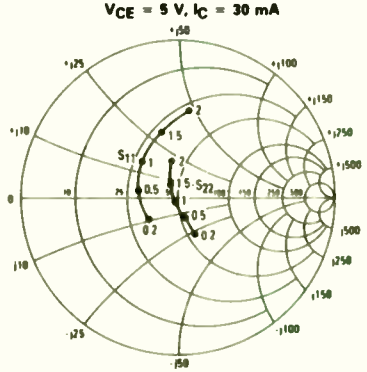
Above 500 MHz, the SOT-143 shows the smallest increase in magnitude going 0.09 @ 1.0 GHz to 0.16 @ 2.0 GHz. The SOT-23 shows the next smallest increase in magnitude going from 0.16 @ 1.0 GHz to 0.30 @ 2.0 GHz. The TO-92 and SOT-89 show the largest increase in magnitude of S_{21} from 1.0 to 2.0 GHz. They also remain very close in value. Both packages go from 0.21 or 0.22 @ 1.0 GHz to 0.36 or 0.38 @ 2.0 GHz, with the SOT-89 having the slightly larger magnitude.

Considering the phase of S_{21}, both SOT-23 and SOT-143 show the pattern of going from an initial low value @ 200 MHz, increasing @ 1.0 GHz, and reaching a lower than the initial value @ 2.0 GHz. The phase of S_{21} goes from 54° @ 200 MHz to 62° @ 1.0 GHz to 52° @ 2.0 GHz, for the SOT-143. For the SOT-23, the phase goes from 68° @ 200 MHz to 70° @ 1.0 GHz to 60° @ 2.0 GHz.

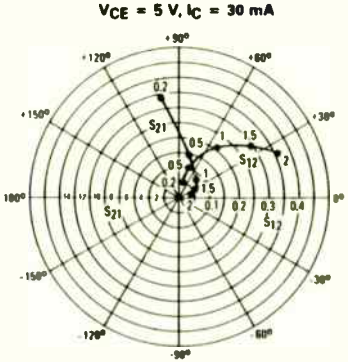
The TO-92 and SOT-89 show a different pattern. Both packages show a steady decrease in value for the phase of S_{21} as frequency increases with the TO-92 showing the largest decrease of the two. For the SOT-89, the phase of S_{21} goes from 74° @ 200 MHz to 66° @ 1.0 GHz to 49° @ 2.0 GHz. For the TO-92, the sequence is 75° @ 200 MHz to 55° @ 1.0 GHz to 23° @ 2.0 GHz.

TO-92 MPS571

INPUT/OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA



FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA

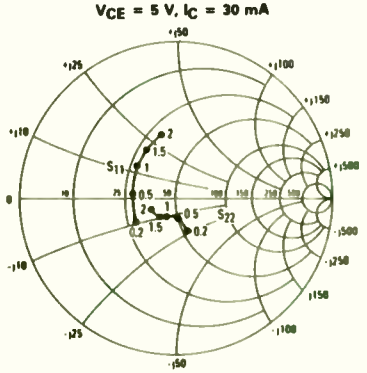


COMMON EMITTER S-PARAMETERS

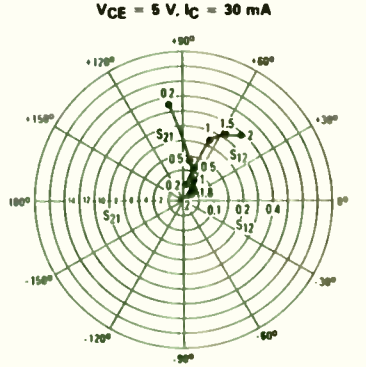
V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠φ	$\|S_{21}\|$	∠φ	$\|S_{12}\|$	∠φ	$\|S_{22}\|$	∠φ
5	5	200	0.62	−80	8.22	122	0.07	56	0.63	−44
		500	0.40	−148	4.52	87	0.11	50	0.36	−58
		1000	0.39	155	2.51	54	0.16	48	0.23	−78
		1500	0.46	122	1.86	32	0.23	42	0.15	−114
		2000	0.59	100	1.50	14	0.31	33	0.14	173
	15	200	0.33	−121	12.88	105	0.05	67	0.37	59
		500	0.28	175	5.62	79	0.10	65	0.18	−67
		1000	0.32	143	2.99	53	0.19	55	0.08	−94
		1500	0.40	117	2.14	32	0.27	42	0.07	171
		2000	0.55	95	1.74	17	0.35	30	0.196	117
	30	200	0.23	−143	13.65	99	0.05	75	0.26	−62
		500	0.23	169	5.75	76	0.11	70	0.13	−68
		1000	0.30	130	3.05	50	0.21	55	0.04	−136
		1500	0.41	106	2.11	28	0.29	38	0.12	130
		2000	0.56	85	1.70	11	0.36	23	0.26	102
	50	200	0.21	−158	13.96	96	0.05	79	0.21	−61
		500	0.23	162	5.82	75	0.11	72	0.11	−66
		1000	0.30	128	3.09	49	0.21	56	0.03	−149
		1500	0.41	105	2.11	28	0.29	39	0.12	127
		2000	0.56	84	1.70	11	0.36	23	0.27	100

SOT-89 MXR571

INPUT/OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA



FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA

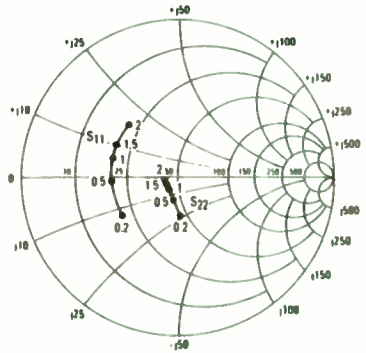


COMMON EMITTER S-PARAMETERS

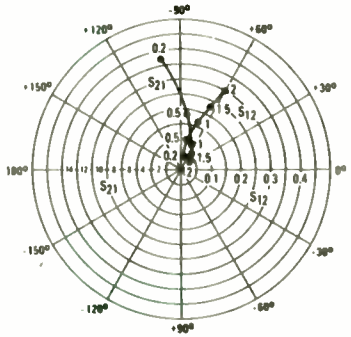
V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠φ	$\|S_{21}\|$	∠φ	$\|S_{12}\|$	∠φ	$\|S_{22}\|$	∠φ
5	5	200	0.60	−84	7.94	120	0.08	56	0.58	45
		500	0.39	−152	4.17	86	0.11	54	0.34	56
		1000	0.39	161	2.32	62	0.19	58	0.27	−71
		1500	0.44	132	1.64	45	0.26	55	0.25	−90
		2000	0.49	106	1.33	31	0.32	52	0.26	−106
	15	200	0.33	126	11.89	101	0.06	67	0.32	−63
		500	0.29	178	5.13	81	0.11	69	0.18	73
		1000	0.33	148	2.75	62	0.22	65	0.15	−99
		1500	0.37	123	1.93	47	0.30	56	0.16	118
		2000	0.42	100	1.55	34	0.37	49	0.17	−139
	30	200	0.28	−149	12.74	97	0.05	74	0.23	69
		500	0.27	174	5.37	79	0.11	73	0.13	82
		1000	0.32	144	2.85	62	0.22	66	0.13	−112
		1500	0.36	120	2.02	47	0.31	57	0.15	−132
		2000	0.40	98	1.62	35	0.38	49	0.17	−152
	50	200	0.26	162	13.03	94	0.05	77	0.18	−71
		500	0.27	169	5.43	79	0.12	75	0.11	85
		1000	0.32	142	2.88	62	0.22	67	0.12	−117
		1500	0.36	119	2.02	47	0.31	57	0.15	−137
		2000	0.40	97	1.60	35	0.38	49	0.17	−155

SOT-23 MMBR571

INPUT/OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA



FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA

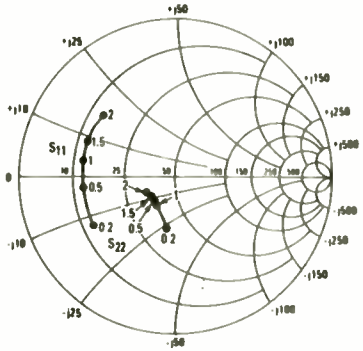


COMMON EMITTER S-PARAMETERS

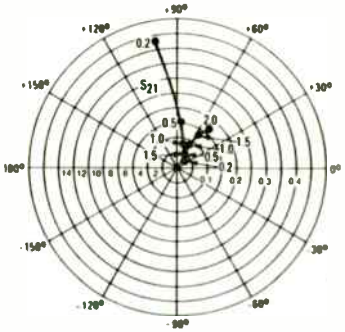
V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5	5	200	0.68	82	8.41	126	0.07	53	0.61	−45
		500	0.52	142	4.62	93	0.10	46	0.35	−60
		1000	0.50	179	2.57	72	0.14	53	0.26	−71
		1500	0.51	161	1.82	57	0.19	58	0.24	−77
		2000	0.52	143	1.48	45	0.24	59	0.22	−86
	15	200	0.46	−125	13.65	108	0.05	60	0.35	−73
		500	0.43	−169	6.03	66	0.09	66	0.17	−94
		1000	0.44	168	3.20	72	0.16	67	0.14	−111
		1500	0.45	152	2.21	58	0.22	64	0.11	−118
		2000	0.46	137	1.80	48	0.29	59	0.10	−131
	30	200	0.42	−148	14.79	102	0.04	68	0.26	−87
		500	0.41	177	6.31	84	0.09	72	0.14	−115
		1000	0.42	165	3.35	71	0.16	70	0.12	−135
		1500	0.44	151	2.29	59	0.23	65	0.11	−144
		2000	0.44	135	1.84	48	0.30	60	0.10	−157
	50	200	0.41	−159	15.14	98	0.04	73	0.21	−96
		500	0.42	179	6.38	83	0.09	75	0.13	−124
		1000	0.43	163	3.35	70	0.16	71	0.12	−143
		1500	0.44	148	2.32	58	0.23	66	0.10	−151
		2000	0.45	134	1.84	48	0.30	60	0.09	−163

SOT-143 MRF 5711

INPUT/OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA

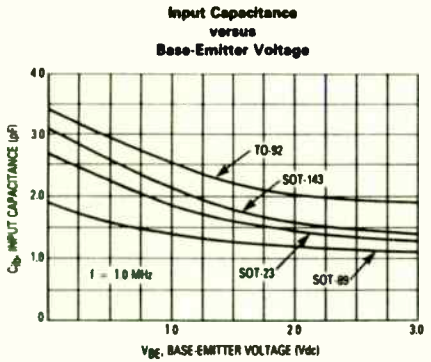


FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA



COMMON EMITTER S-PARAMETERS

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5	30	200	0.60	−150	17.22	106	0.03	54	0.34	−87
		500	0.62	−177	7.52	85	0.05	60	0.24	−130
		1000	0.62	167	4	72	0.09	62	0.22	−144
		1500	0.64	154	2.74	59	0.13	56	0.24	−148
		2000	0.63	138	2.2	46	0.16	52	0.24	−157



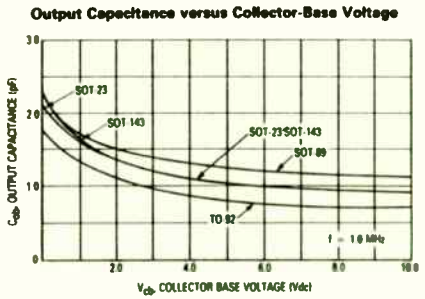
Cib VS.V_{BE}

These curves show the inverse relation of input capacitance Cib with emitter-base voltage V_{BE}.

TO-92 has the highest input capacitance while SOT-89 has the lowest due to the position of E-B lead frame surfaces which are not facing each other directly as the TO-92. The SOT-143 and the SOT-23 are intermediate in value with the SOT-143 having a greater value of Cib than SOT-23 at any given voltage. The lead frame surfaces are still facing each other, but there is less "common plates" area compared to TO-92, due to lead frame thickness.

At 0.5, the TO-92 is approx. 3 pf, the SOT-143 is approx. 2.6 pf, the SOT-23 is approx. 2.3 pf, and the SOT-89 is approx. 1.6 pf for Cib.

Of all the curves, SOT-89 has the smallest slope changing only 0.5 pf from 0.5V to 3.0V. The SOT-143 shows the greatest change in value of 1.2 pf from 0.5 to 3.0V. Both the TO-92 and SOT-23 show an approximate change of 1.0 pf from 0.5 to 3.0V.



Cob VS. Vcb

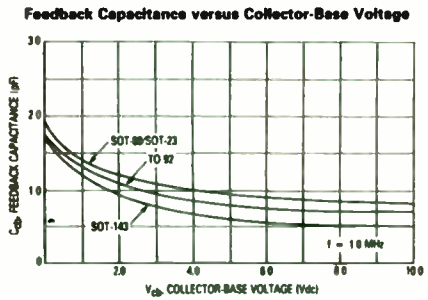
This graph shows the inverse relation of output capacitance (Cob) with collector-base voltage Vcb.

The graph shows that the SOT-89 has the highest value of Cob and TO-92 has the lowest at a given value of Vcb. The SOT-23 and SOT-143 show intermediate and essentially identical values of Cob.

At 2V, the curves show the following values: for SOT-89, approx. 1.5 pf, for SOT-23 and SOT-143, approx. 1.4 pf, for TO-92, approx. 1.1 pf.

Considering the slopes of the curves, the TO-92 shows the least change in value of 0.3 pf from 2V to 8V. Both the SOT-23 and the SOT-143 show the greatest change in value of 0.45 pf from 2V to 8V. The SOT-89 shows an intermediate decrease of 0.35 pf.

All the curves are within a 0.5 pf band.



Ccb VS. Vcb

This graph shows the inverse relation of feedback capacitance Ccb with collector-base voltage Vcb with emitter AC grounded using .1 pf capacitor.

The SOT-89 and SOT-23 curves are identical and show the highest value of Ccb of all the packages at any given value of Vcb. The SOT-143 has the lowest valued Ccb curve while the TO-92 curve is intermediate in value.

The SOT-143 shows the greatest change in value of Ccb of 0.45 pf from 2 to 8V. The SOT-23 and SOT-89 packages show the least change of 0.35 pf. The TO-92 shows an intermediate change of 0.4 pf from 2V to 8V.

All of the curves are within a 0.4 pf band.

All of these parameters Cib, Cob, Ccb and slope differences are lead frame construction dependent. Refer to figures 5, 6, 7 and 8.

CONCLUSION

The most significant difference between the four package types is the gain performance. Both as a function of frequency and collector current, the SOT-143 shows the highest gain. The SOT-23 is next in gain performance. The SOT-89 and TO-92 packages show similar but lower gain performance than the SOT-23.

Generally, RF performance is package dependent and is determined by parameters mentioned before such as size of package, lead frame construction, etc.

There are no significant differences in noise figure performance between the package types investigated. The variations measured between the different package types are small and lie within the range of variation that can be reasonably attributed to measurement error.

The input and output capacitances Cib, Cob and Ccb will vary from package to package. These variations are primarily due to internal construction of the device. These parameters are easily measured making them useful for outgoing and incoming inspections.

On the other hand S-parameters require a relatively complicated test setup and special fixturing. The S-parameters give the most comprehensive information of package differences most useful for designers. The results of these measurements can be used to calculate many other useful design parameters.

In spite of the variations in gain noted, all four packages show good RF performance. Other factors, aside from RF performance alone, such as power dissipation, cost, and board layout among others are undoubtedly relevant considerations when faced with the problem of determining which package type is best for a particular application.

ACKNOWLEDGEMENTS

I would like to thank Matt Zamora for the invaluable support he has given me by providing the vast number of measurements upon which this investigation was based. I would also like to extend my sincere appreciation to Lance Ulik and Jim Fogle for their advice and technical expertise in helping to complete this paper.

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RELIABLE OBSTRUCTED PATH COVERAGE DETERMINATION

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ABSTRACT

When the VHF or UHF terminals of a proposed circuit are so widely separated that the line-of-sight communication is not possible, the presence of a sharp, ridgelike obstruction between the terminals may improve the signal to the point where reliable communication is achieved. The strength of the received signal results from diffraction over the sharp obstacle, and varies with the signal frequency, the elevation of the circuit terminals, the location and elevation of the obstacle, and the shape of the obstacle peak. In many instances, the strength of the diffracted field exceeds the strength of a normal path field and has the added advantage of being essentially free from fading.

This paper will assist in showing how to determine the best obstructed path coverage when this is a viable alternate means to free path communication.

GENERAL COMMENTS

In the conventional use of VHF radio relay equipment, circuits have been considered satisfactory only when the path was unobstructed and stations were close enough, or sufficiently elevated, to be within radio line of sight. Under these conditions, both range and reliability were thought to be at a maximum. However, experience indicates that satisfactory communication usually can take place over a range appreciably greater than the radio line of sight, and that both range and reliability may actually be extended by the existence of an elevated obstacle in the radio path, similiar to passive repeaters used in microwave communications.

In situations where a terrain feature, such as a sharp mountain ridge of sufficient elevation, lies between the transmitter and the receiver, improved signal levels--relatively free from fades--have been observed. This phenomenon is referred to as the knife-edge effect. Circuits near or beyond the radio line of sight can be categorized as follows:

(1) The normal circuit; this may cover all types of intervening terrain, except no single terrain feature predominates. (Figure 1A)

(2) The obstructed circuit; one predominant terrain feature appears as the obstacle in the radio path. (Figure 1B)

Techniques of predictions and computation have been developed for used on obstructed radio paths for distance up to approximately 300 miles. Many obvious advantages accrue from this extension of the normal 25 to 30 mile range--

(1) No intermediate relay points are necessary; thus requirements for equipment and operating personnel are reduced.

(2) Installation and supply problems are alleviated because relatively inaccessible mountaintop locations need not be used.

(3) High circuit reliablity can be relaized, since properly engineered obstacle gain paths show a much lower fade rate than comparable line of sight paths.

(4) Operational dependability is increased, becuase fewer pieces of equipment are required.

(5) Large numbers of completely independent circuits can be established over the same path.

(6) Fewer frequencies are required for operation over long distances.

(7) Decreased chance of interference results, because of the directional characteristics of propagational path.

PLANNING OBSTRUCTED PATHS

The planning of an obstacle gain path necessarily entails detailed study of all intervening terrain. The planning and engineering of these paths is accomplished as follows:

1. Locate the desired terminal areas on suitable topographic charts (Use Geographic Quads 1X2 to start for long paths and 30, 15 or 7.5 min. for short paths).

2. Draw a line between the two most desirable points selected for the transmitter and receiver locations.

3. Locate the highest point (mountain peak or ridge line) in the intervening terrain. This high point should be as close as possible to the line drawn in 2 above.

4. Draw path profiles along the lines that connect the high point selected and each of the two desired terminals. If the profile shows multiple obstacles, repeat steps 2 and 3 above until, by slight shifts in the position of the terminals or by using other high points, only one obstacle intervenes between terminals. Then locate the tentative terminal sites.

5. Determine the expected transmission loss of the path (Figure 2).

6. From a tabulation of equipment characteristics, select an equipment combination that satisfies the service requirements as well as the propagational requirements given in 5 above.

7. Make a radio signal strength survey in one terminal area.

8. Choose a maximum signal location close to the proposed terminal site and experiment with different antenna heights to obtain the best signal strength.

9. Install station equipment at the desired site.

10. Repeat 8 and 9 above for other terminal.

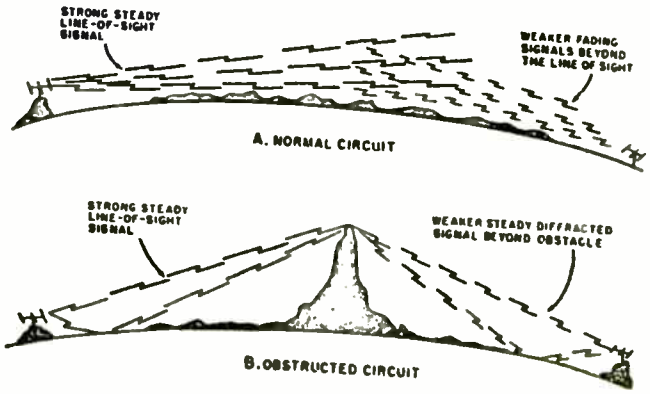

FIG 1. NORMAL & OBSTRUCTED PATHS

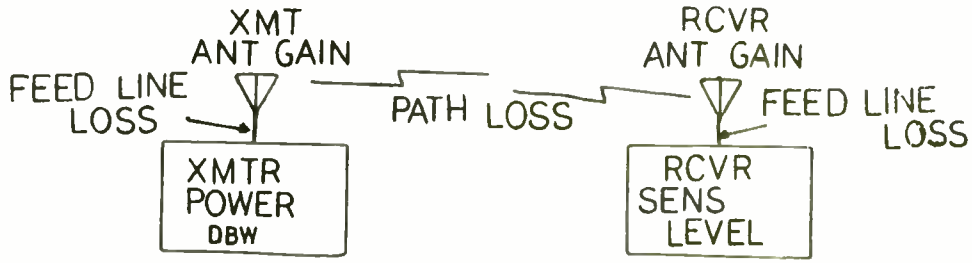

FIG 2 PATH COMPONENTS

PRELIMINARY PATH STUDIES

On a topographic map, identify the areas between which communication is desired. This map should have an altitude contour interval of no more than 100 feet. In selecting the terminal areas, consider the accessibility of the site to roads, power sources, and telephone circuits.

Determine whether a mountain peak or ridge exists between the two tentative terminal locations and whether or not it is of higher altitude than the surrounding terrain in the direction of the terminal areas. Several alternate terminal locations should be selected in the two terminal areas, such as sites A through F in Figure 3. If no such ridge or peak exists between any of the tentative sites, it may be necessary to install a relay station, and obstructed path cannot be used effectively.

Draw a line between the two tentative site locations that appear to be the most desirable. For example, if sites B and E were both terminal or relay stations in existing communications networks then they would be the most desirable due to the availability of existing services and roadways. Draw lines from each terminal location through the peak or ridge which brings the line as near as possible to terminal sites tentatively selected at the other end of the circuit. In Figure 3, for example, a line from C to F or from A to D would not cross the ridge at its sharpest point, while lines from C to D and from A to F do cross the sharp ridge crest. Lines A to F, B to E, and C to D are appropriate tentative paths for this circuit.

PROFILE PREPARATION

After selecting the path that apparently fulfills the requirements, profile drawings should be made to check the path for obstructions between each terminal and the major obstacle. To allow for the normal refraction of radio waves by the atomsphere, these profiles should be drawn on a 4/3 earth graphic scale.

Figure 4 is a graphic scale for 4/3 earth radius. This scale can be used with overlay paper on paths extending up to

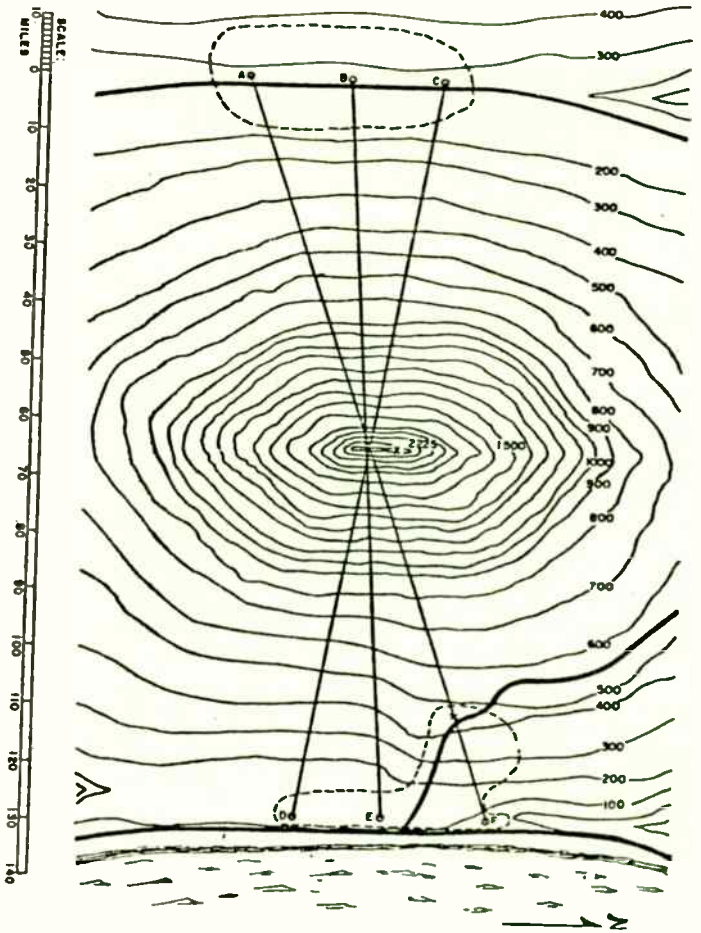

FIG. 3 CONTOUR MAP PROBLEM

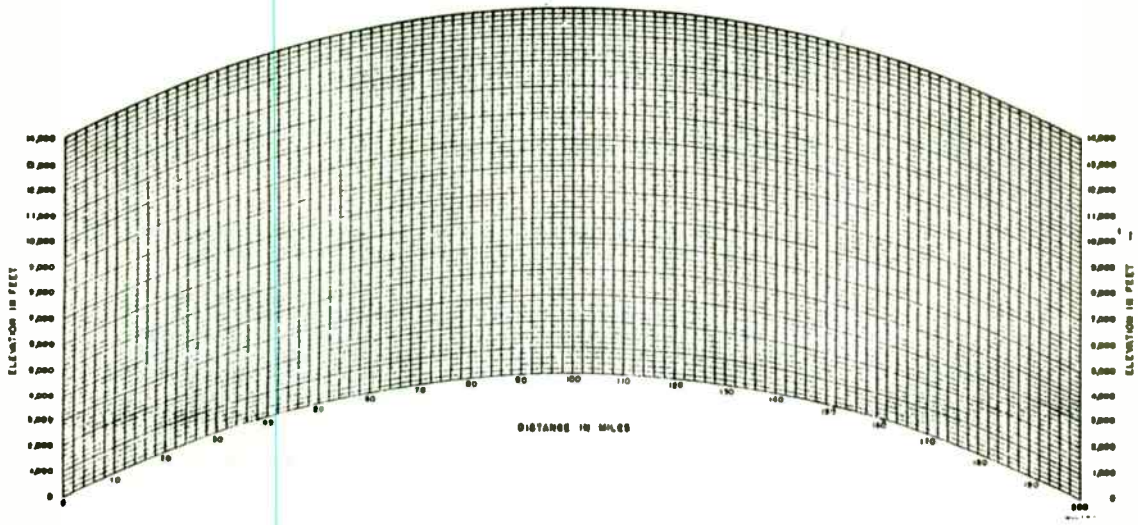

FIG 4 GRAPHIC SCALE 200MI 4/3 EARTH

200 miles. Paths over 200 miles can be profiled in the same manner as tropospheric scatter paths.

Plot the profile for path B to E, Figure 3. This profile is shown in Figure 5. From this profile drawing, it is determined that the path from terminal site B to the obstacle is clear, but that the path from terminal site E to the obstacle is shielded by a slight rise some 10 miles to the west of terminal E, and that the antenna would have to be elevated approximately 200 feet to use this terminal location. To move the terminal away from the highway, the 10 miles necessary for installation on the intervening rise would make the terminal site too inaccessible. Other paths should be investigated.

Plot the profile for path A to F (Figure 6). From this profile, it is determined that the path from A to the obstacle is clear, but that the path from terminal site F to the obstacle again is shielded by a continuation of the same rise that shielded terminal E. However, in this case, the rise is near the northwest branch of the highway, and the terminal can be located at point X along the straight line propagational path.

If no possible terminal locations were acceptable along the straight line path across the obstacle, then terminals slightly to one side or the other could be selected; however, the closer they are to the straight line path, the better the results will be. In the example, tentative sites should be selected at points A and X (Figures 3 and 6).

In selecting terminal site locations for single obstacle paths, the terminal sites should not be located too close to the obstacle (Figure 7A). Even though the profile shows only one obstacle, gently rounded obstacles (Figure 7B) attenuate the signal more than do sharply defined obstacles. Multiple obstacle paths should be avoid if at all possible since their attenuation is much greater and their path prediction is extremely critical. In Figure 7C, thepath T to Q might possibly work, since the second obstacle is near grazing. But if the obstacle were only slightly higher, or the point Q were slightly lower, the path might not be usable. Where a choice of equally sharp obstacles of different heights is available, the lower obstacle usually produces less attenuation, and is to be preferred.

The shape of the obstacle at right angles to the transmission path is unimportant, except that mountain peak

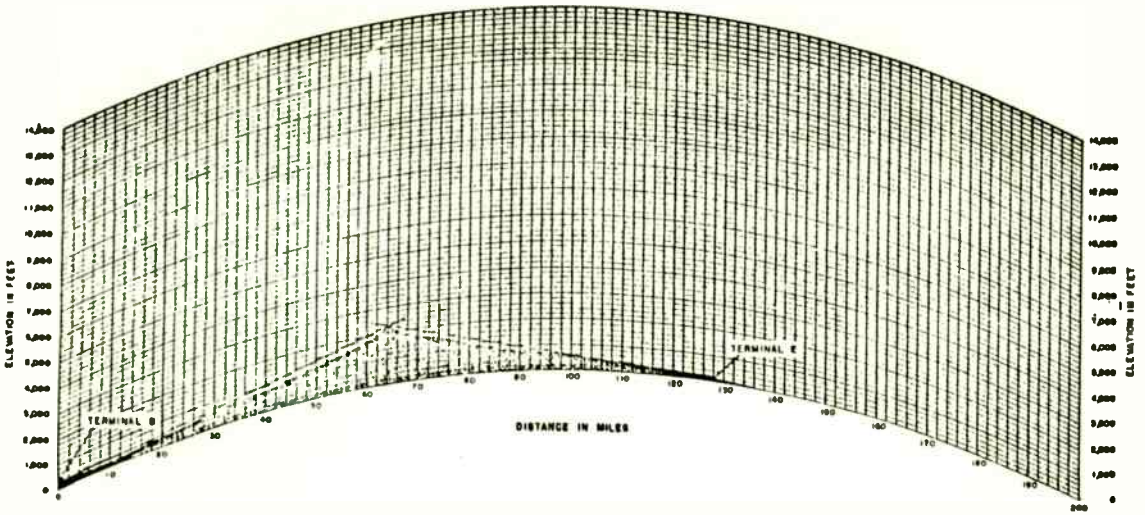

FIG. 5. PROFILE OF PATH B-E, FIG. 3

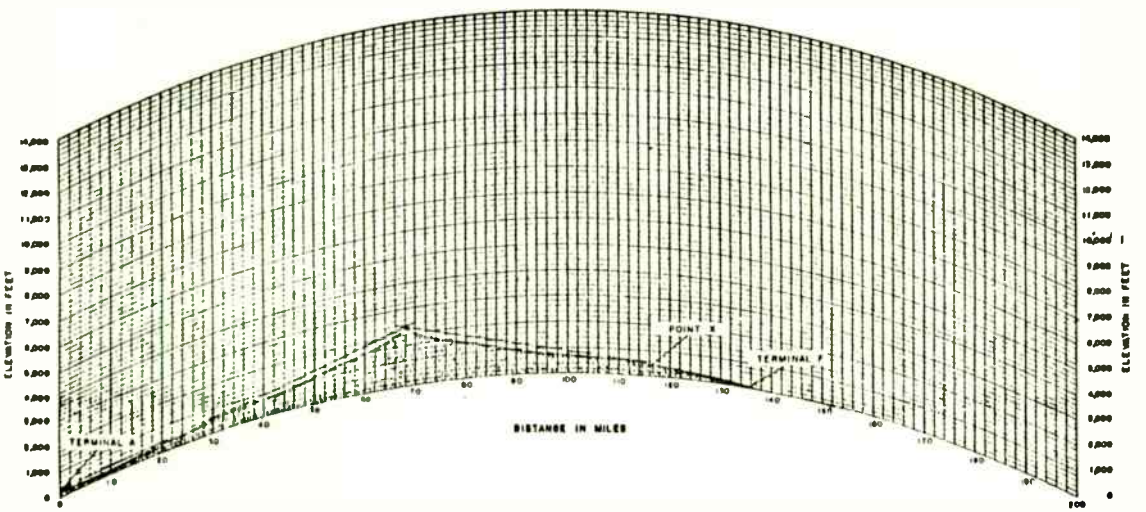

FIG 6 PROFILE PATH A-F, FIG 3

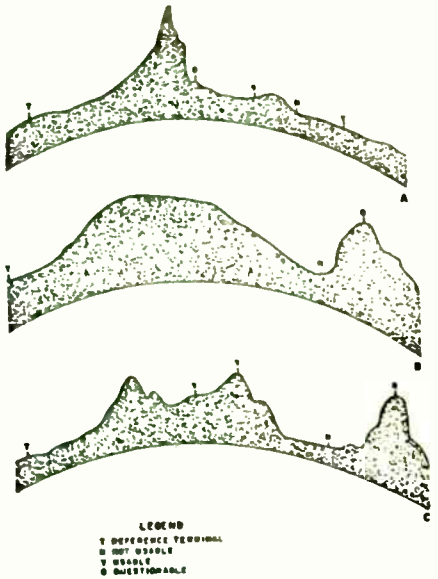

FIG 7 PROFILES

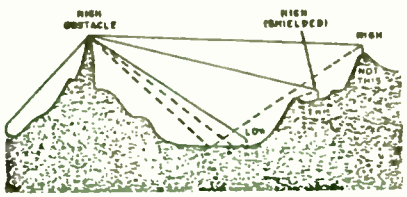

FIG 8 SITING POSITIONS

obstacles produce a more direct effect in the terminal area than do ridge obstacles. This effect is caused by the peak offering only one obstacle path, directly over the crest which is the sharpest point of the obstacle. However, a ridge may retain its curvature at the crest for a considerable distance, thus, the portion that produces the diffraction process is not critical as to position.

The obstacle height is the height of the obstacle above the average altitude of the two terminal sites. For example, if one terminal site is situated at an altitude of 300 feet above sea level and other terminal site is at 500 feet above sea level, the average altitute of the terminals is 400 feet. If the obstacle height is 2,500 feet above sea level then the actual effective obstacle height is 2,100 feet (2,500-400=2,100 feet).

Antenna tower heights must be such that the terminal to obstacle path has adequate clearance above the average terrain and the antenna must be above any heavy foreground foliage (any obstruction within the first Fresnel Zone). The following points should be considered when selecting terminal sites:

1. Neither terminal should be located closer to the obstacle than approximately two miles per 1,000 feet of obstacle height.

2. If possible, avoid terminal to obstacle paths that are over water.

3. Locate terminals at low points, unless a high elevation can be found that is shielded from any reflected paths (Figure 8). The midpath height should not be excessive.

4. Avoid any foreground obstacles, such as trees, buildings, steel towers, and guy wires.

Antenna heights must be adjusted to provide free-space clearance between each terminal and the obstacle. This clearance is determined by considering the top of the main obstacle to be a broadband relay station. Then the path from each terminal to this relay station (obstacle peak is considered in turn as a line of sight path in accordance with the criteria for determining free-space path clearance.

EXPECTED TRANSMISSION LOSS

After determining the obstacle height and path distance from the profile and contour maps, a perfromance estimate can be made for the proposed path.

The operating frequency, obstacle height, and path length must be known to compute the estimated path loss. The nomogram in Figure 9 can be used to make this estimate.

The nomogram (Figure 9) is used in the following manner:

1. Draw a line connecting the operating frequency on scale F with the path distance on scale D.

2. Connect the point where this line crosses the unscaled line X with the obstacle height on scale H.

3. Read the estimated path loss at the point where this second line intersects scale L.

This estimated path loss then is compared with the maximum acceptable path loss of the proposed equipement.

EQUIPMENT SELECTION

Equipment requirements for obstacle gain paths are determined by computing the maximum allowable path loss of the particular type of equipment and comparing this result with the expected path loss. If the maximum allowable path loss for the equipment is larger than the expected path loss, the system is good and an operable circuit should result.

The first step in computing the equipment capability is to findtherequired receiver input. The following formula is used to determine this factor:

$$IR=ND+NF+FM+TQ$$

IR= THE REQUIRED RECEIVER INPUT IN DB BELOW FREE SPACE;

ND= THE EFFECTIVE NOISE INPUT DUE TO THE RECEIVER ACCEPTANCE BANDWITH IN DB;

NF= THE RECEIVER NOISE FIGURE IN DB; AND

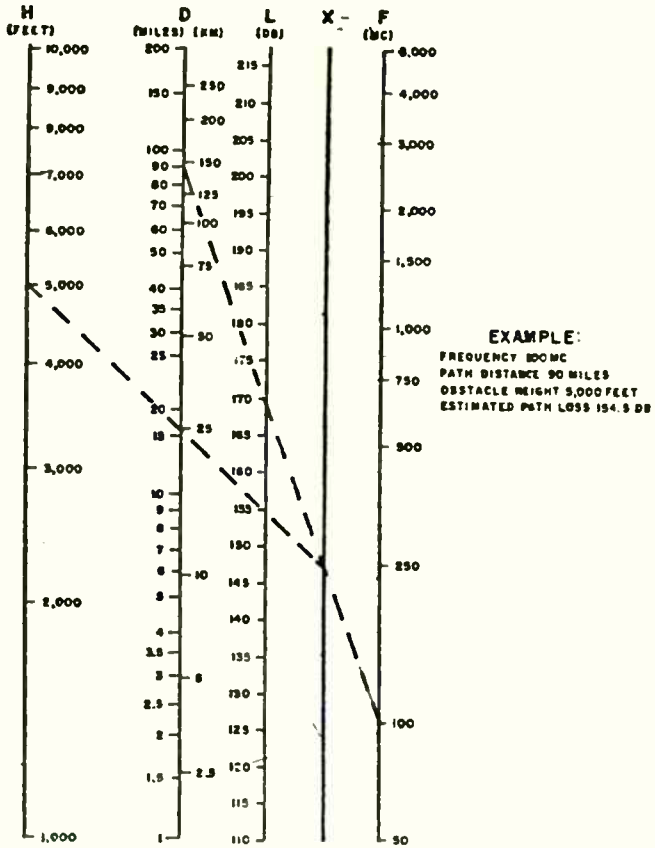

FIG.9 ESTIMATED PATH LOSS NOMOGRAPH OBSTACLE GAIN PATH

FORMULA:

$$L = 20\log(H) + 20\log(F) + 20\log(D)$$

D = PATH DISTANCE MI.
F = FREQ. MHZ
H = OBSTRUCTION HEIGHT FT.
L = EST. PATH LOSS OBSTACLE GAIN

TQ= THE RECEIVER QUIETING THRESHOLD IN DB.

Noise input. The effective noise input is directly related to the acceptance bandwidth of the receiver, and can be determined from the nomogram in Figure 10. The actual acceptance bandwidth of the receiver often is not specified, and must be approximated from data given in the equipment specifications or manual.

For direct FM receivers, the effective acceptance bandwidth can be approximated by the formula:

$$B=1.25(2M+2D)$$

where:

B= THE EFFECTIVE ACCEPTANCE BANDWIDTH;

M= THE HIGHEST FREQUENCY OF THE MODULATING SIGNAL; AND

D= THE MAXIMUM DEVIATION OF THE TRANSMITTER.

The factor 1.25 in the formula adds 25 percent to the required minimum acceptance--this 25 percent is an approximation of the safety factor built into most receivers to allow for oscillator drift or other circuit variations during operation.

In systems using PCM (pulse code modulation) FM, the receiver acceptance bandwidth is computed by the following formula:

$$B=2.5(M)$$

where:

M= THE BANDWIDTH OF THE MODULATING SIGNAL.

Noise Figure. A conservative noise Figure for most receivers is 12 dB. Other noise Figures can be found in the equipment manufacturer's manuals or specifications.

Fade Margin. The system fade margin is an arbitrary Figure set by the results of many experiments and measurements on operational systems. Normal VHF and microwave paths usually require a fade margin of

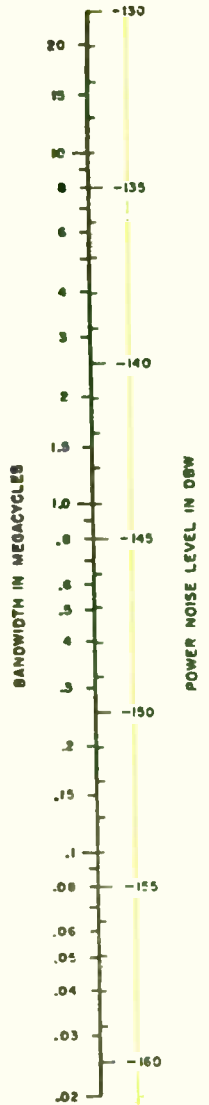

FIG 10 — BANDWIDTH TO NOISE LEVEL

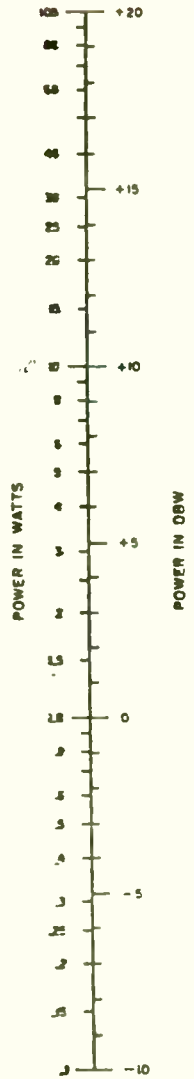

FIG 11 — POWER TO DBW

approximately 20 dB. But the obstacle gain path exhibits relatively slight fading, and the necessary margin to protect against fading is only 10 dB.

Quieting threshold. The quieting threshold represents the signal level which must be maintained to provide a usable signal over the incoming noise. For most receivers, the threshold indicates an allowance of 12 dB in this formula.

For example a radio receiver has a required receiver input of -118.5 dB, computed as follows

$$IB=ND+NF+FM+TQ$$

$$=-153.5+12+10+12$$

$$=-118.5 \text{ dB.}$$

Equipment combinations.

Various combinations of equipment in the system will have different values for the maximum allowable loss on the propagational path. The maximum allowable loss with any particular combination of equipment is computed by the following formula:

$$LM=PT+GP-LX-IR$$

where:

LM= the maximum allowable loss;
PT= the transmitter power in dB referred to 1 watt (dBw);
GP= the path antenna gain in dB;
IR= the required receiver input in dB.

Maximum transmission loss. The maximum allowable transmission loss is the greatest value of attentuation that the particular equipment combinations must overcome to provide the system with a usable circuit. This value is compared with the estimated path loss to determine whether or not the computed equipment combination will provide sufficient gain to overcome the predicted path losses.

Transmitter power. The transmitter power, referred to 1 watt, may be obtained from the nomogram in Figure 11. As an example assume a transmitter with a nominal power output of

40 watts. The nomogram shows a value of 16 dBw for this power. If the nomogram does not cover the required power Figure, then the value must be computed by the following formula:

$$PT=10\log PW$$

where:

PT= the power gain in dBw; and
PW= the maximum transmitter output power in watts.

Path Antenna Gain. This expression in the basic formula combines the apparent gains of the transmitting and receiving antennas. For example, two yagi arrays one transmitting has a gain of 6 dB and one receiving has a gain of 9 dB; the path antenna gain is the sum of both antenna gains thus the path antenna gain is 15 dB in this case.

Transmission line loss. The attenuation of the transmission line at each end of the system is computed in accordance with criteria given. The total of the losses in the transmitting and receiving transmission lines then is substituted for the factor LX in the formula.

Required Receiver Input. The value of IR, as computed above, is substituted in this formula. Note that the computation in above results in a negative number of decibels, which must be subracted in the formula for maximum allowable loss. This entails a change of sign.

SIGNAL STRENGTH SURVEY

After the tentative transmission paths have been selected and the frequency of operation has been determined, a signal strength survey should be conducted on the sites.

The exact location of the tentative terminal site must be determined in the field. If there are prominent landmarks such as road intersections, then the location of the exact site is simplified; otherwise, experience surveyors should locate the tentative site as accurately as possible from the Quads used.

Determine the azimuth of the transmission path from one terminal location and install a temporary fixed station, with directional antenna at this site. This station is used to transmit to mobile receiving equipment at the other site. Maximum transmitter power should be utlitized during this survey.

The survey can be conducted on the exact or a relatively close frequency within 10 MHz to determine if the path as theorically determined exists. It has been my experience that in some cases (especially marginal path to equipment gain ratio cases) a path does not exist although it should, and a different path does exist most likely to a different terminal site.

Spectral Shaping of Radio Frequency Waves

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ABSTRACT

This paper presents a method[1] of spectrally shaping a Quadrature Phase Shift Keyed, QPSK, signal using baseband techniques applied to an RF signal. This method does not require the use of linear modulators or amplifiers or expensive bandpass crystal filters. It results in a constant amplitude signal allowing the use of Class "C" amplification without spectrum spreading, intermodulation distortion or intersymbol interference. This technique is presently used to transmit 340K bps of data in a 350F9 classification. (99% of the transmitted energy is contained in 350 kHz of bandwidth). This method is applicable to FSK and some forms of PSK when used for digital data transmission.

[1]The theory and techniques described in this paper were developed by Martin H. Beauford and Jerry J. Norton for the OPSEIS® 8600 System with patents pending. For more information about this technology or the OPSEIS® 8600 System contact Applied Automation, Inc., Geophysical Systems Division, Bartlesville, OK 74004.

INTRODUCTION

1. Any modulation (changing the carrier) of a R.F. wave spreads the spectrum.

2. The amount of spreading is a function of:

   a) the way the carrier is changed; (type of modulation);
   b) how much the carrier is changed; (amplitude of modulation);
   c) how fast the carrier is changed; (frequency of modulation);

3. Most regulatory agencies have limits on amount of spectrum spreading.

4. Digital modulation, squarewaves, cause excessive spectrum spreading over what is needed to convey the information.

5. Present methods of spectral shaping largely consist of:

   a) filtering the modulating waveform before modulating, (baseband filtering)
   b) filtering the RF spectra after modulating. (RF bandpass filtering)

6. Both methods have serious drawbacks because of physical hardware limitations when implementation is attempted.

Presentation:

A signal frequency signal with a constant amplitude is called a CW (continuous wave) signal. It occupies zero bandwidth and does not contain any time-variant information.The only information that is carried by this signal is amplitude and frequency both of which are constant with respect to time (by definition). Because the modulation varies the signal with respect to time additional frequencies are generated.

The amount that the spectrum is spread is a function of three variables.

a) The way the carrier is changed, (type of modulation),
b) the amount the carrier is changed, (the amplitude of modulation),
c) the rate the carrier is changed, (the frequency of modulation).

Of these three, the rate at which the carrier is changed, or frequency of modulation has the greatest effect on the amount of spreading. If items a & b are held constant, the amount of bandwidth required is essentially directly proportional to the rate.

Essentially, when a CW signal or carrier (fc) is modulated with a single frequency (fm), a pair of sidebands are generated. The frequencies of these sidebands are the carrier frequency plus and minus the modulating frequency (fc $\pm$ fm). Non-linear and/or exponential forms of modulation such as phase and frequency modulation generate additional sidebands at (fc $\pm$ Nfm) (and sometimes others). N is an integer from 1 to infinity.

A complex wave form consists of many frequencies of various amplitudes and phases all of which may be changing with respect to time. Modulating with a complex waveform generates many sidebands of varying amplitudes and frequencies.

Digital modulation (modulation with square waves) causes excessive spectrum spreading over what is needed to actually convey the information, primarily because the harmonics of the squarewave also generates sidebands.

Most regulatory agencies (FCC for example) have limits on how much spectrum can be occupied and also some limits on spectral distribution. The FCC defines "occupied bandwidth" as the bandwidth which contains 99% of all the transmitted power. The reason for this definition is because the FCC is primarily concerned with adjacent channel interference, not how the user actually distributes energy within a given bandwidth (Figure 1). This definition of bandwidth is obviously much wider than the 3 dB or 6 dB bandwidth described or used in most textbooks but occupied bandwidth is probably the most important specification that all of us are concerned with in any design.

The spectral distribution of any signal must be evaluated in terms of occupied bandwidth instead of the "3 dB bandwidth". Therefore, analysis of all factors and specifications is necessary in order to determine the optimum configuration for any given application. It is possible that in some applications, the amount of spectrum used is not a restriction; however, I have never ever experienced the luxury of unlimited bandwidth. Almost every application is somewhat bandwidth limited, that is a lot of information must be crammed in a relative narrow bandwidth. Other factors such as cost, complexity, error rate, acquisition time, etc., may prevent the most efficient bandwidth technique from being employed.

In many applications, a fixed data transfer rate is the primary consideration. In simpler terms; the FCC has allocated "BW" bandwidth and I must cram "BPS" bits per second of data in that bandwidth. The ratio of BW/BPS is what might be called the "bandwidth efficiency factor". If this

factor is a relative large number, 6-10 or more, almost any form of modulation will work. It is only when the factor becomes small that circuitry becomes complex. For small factors (F < 3) it is necessary to perform some form of spectral shaping to meet FCC specifications.

Figure 2 shows a carrier at 100 MHz, AM modulated 50% with a squarewave of 50 kHz representing 100K BPS data. Observe the occupied bandwidth. The first pair of sidebands contain all the information that is necessary. The additional sidebands are not necessary and only improve the shape of the received signal. If the square wave is passed through a simple RC low pass filter turning it into a triangular wave, we obtain Figure 3. Notice the reduction in occupied bandwidth by this simple shaping. Figure 4 shows modulation by a sinewave (all harmonics removed). Note again the bandwidth reduction over the triangular waveform.

Figures 5A, 5B and 5C show an FM modulation by the 50 kHz squarewave, triangular, and sinewave using a modulation index of 1.0 (deviation divided by modulating frequency equals 1.0). Again note the bandwidth reduction by spectrally shaping the modulating waveform before applying it to the modulator.

Figure 6A shows a binary PSK modulated spectrum using same parameters as in Figure 3 (AM) and Figure 5A (FM). Note that the spreading of the spectrum is even worse for PSK than for either FM Or AM. Figure 6B shows how these sidebands don't fall off very much even at 5 MHz away; (only about 40 dB reduction). Obviously shaping the modulating waveform before modulating would show a significant improvement in bandwidth reduction, but this technique requires a linear modulator. Distortion in the modulator will cause the spectrum to spread similar to the squarewave. Linear modulators are a "PAIN", because nothing is really linear. A linear modulator is only more linear than a non-linear modulator. Feedback around a modulator is sometimes used to improve the linearity. Therefore all "linear modulators" will cause more spectrum spreading than the expected amount.

Another way to reduce spectrum spreading is to filter after modulating. Invariably this technique is more difficult to accomplish because:

a) Very sharp cut-off filters are needed.
b) They must be applied at the RF frequency.
c) They introduce phase distortion (phase is not linear over the pass band).
d) They usually ring when an impulse is applied. (They cause amplitude distortion.)

Let us now digress for a minute into some of the "other" factors previously mentioned. Most of the time an error rate is specified at a given range, power level or who-knows-what, requiring the receiver to operate at the minimum signal level. In the application I will describe later this was the case. A certain receiver-sensitivity/error-rate specification along with a minimum data rate within a predetermined bandwidth had to be met, regardless of complexity or cost. In applications such as this one, PHASE MODULATION (PM) gives the lowest error rate at a given signal level compared to other forms of modulation.

But from the standpoint of occupied bandwidth or spectrum spreading, phase modulation is probably the worst form of modulation. Figures 7A & 7B show a phase modulated spectrum generated with clocked data from a pseudo-random

data generator (repeating at 255 bits), instead of a 1/0/1/0/1/0 repeating pattern as in figure 6A & B. The first nulls occur at ± clock (or ± BPS). All the needed information is contained in the main lobe (between the first nulls). All the other lobes could be eliminated as they are not necessary to convey information. They waste power and clutter up the spectrum. It is easily seen from these pictures why PSK must have some form of spectral shaping to be acceptable to the FCC.

Phase shift keying with binary digital data can use any angle of phase shift (± x degrees from 0 degrees carrier). ± 90° gives the lowest error rate because the carrier is at a null and all of the energy is in the sidebands. It is also the worst spectrally and the most complex to demodulate for precisely the same reason. No carrier exists, and to accomplish demodulation some form of a pseudo carrier must be generated. The name bi-phase PSK is often used to describe ± 90° PSK modulation.

Let us consider a different form of bandwidth compression. Assuming we have a serial stream of data being transmitted over an RF link, at "B" bits per second rate. Instead of transmitting these bits serially one at a time, suppose we take consecutive pairs of bits (1&2, 3&4, etc) and store that pair and examine the binary representation for that pair of bits or symbol which will be (00, 01, 10, 11), and then transmit this pair of bits or symbol at one of four levels.

In the case of AM it is one of four amplitude levels; for FM one of four frequencies; or for PSK one of four phases. Because the symbol rate is one half the bit rate, the bandwidth is reduced by a factor of two, therefore bandwidth compression. This technique can be extended to eight or 16 or more levels although the complexity of the receiver to detect one of sixteen levels makes it almost impossible to achieve reliable operation. I've heard of 16 level systems but I have never seen one and have no knowledge of how well they perform.

Generally doubling the number of levels of bandwidth reduction results in a net loss of slightly greater than 3 decibels. Most articles explaining these techniques show the same error rate for QPSK as PSK but careful attention should be given to the scales. Note one scale is "Eb/No" or Energy per bit divided by noise power density. In a four-level system because the signal is two parallel bit streams, each stream has half the energy per bit as a single stream for the same RMS signal level; which is a 3 dB loss per bit. Just remember: Mother nature will not let you get something-for-nothing. If the transmitter has 10 watts output, half the energy goes to each channel.

A four level PSK is known as QPSK (Quadra Phase Shift Keying) and can transfer twice the amount of data in the same bandwidth as binary PSK.

The penalties are:

1. 3 dB loss in receiver sensitivity for the same error rate.
2. Somewhat more complex and costly transmitter,
3. Considerably more complex and costly receiver.

Advantages are:

1. Twice the data rate in the same bandwidth, or
2. 1/2 the bandwidth for the same data rate.

Essentially QPSK is two (orthogonal) bi-phase PSK signals occupying the same spectrum. Because the channels are orthogonal, their spectral envelopes are identical for random data. Their nulls and peaks occur at the same frequencies. Therefore Figures 7A & B are the spectra for QPSK and binary PSK. A pseudo-random data pattern (255 bits long) is used as the modulating signal, with both channels clocked at the same rate. It is obvious that spectral shaping will be required in order to meet FCC specifications in most applications.

Because they are orthogonal, the two channels (called the I & Q channels) are independent. Different clock and data rates can be used in each channel, in which case spectrum will be different from Figure 7. If the clock and data rates in the I and Q channels are the same, the clock (or data) phases can be different. This condition is called offset or staggered QPSK. Because the channels are independent and orthogonal, the spectrum for staggered (or offset) QPSK is the same as for non-staggered QPSK. Typically the amount of stagger or offset is 1/2 bit period but the amount of stagger or offset doesn't affect the spectrum. Figure 8 shows a QPSK modulator used for either form. Figure 9 shows how the vector sums are generated.

We will now make a comparison between standard QPSK and offset QPSK with step function changes in data and phase. In QPSK, the transmitted phase can be any one of four phases, 0°, 90° 180° or 270°. The phase change between adjacent symbols can be any amount because both channels change at the same time. When both bits change at the same time the phase change is 180°. When neither bit changes, there is no phase change and when only one bit changes the phase change is either plus or minus 90 degrees. The 180° phase change is a problem. The fastest way to change the phase 180 degrees is to go through zero amplitude. A 180 degree phase change is really an amplitude change from +A to -A. As a result QPSK is considered a form of amplitude modulation.

Normally QPSK phase shifts are 0°, 90°, 180° and 270° but some other systems advance the phase an additional small amount. However when used with RF links this technique can offset the center frequency which would make the FCC unhappy.

This step function change in amplitude (also 180° phase) causes all kinds of problems when passing through narrow band filters. The filters tends to ring changing both amplitude and phase. A phase change means the channels are not orthogonal which is interchannel interference. Also because of the amplitude changes, linear amplifiers are required to obtain high power levels.

Offset QPSK (Figure 10B) changes only one bit at a time, and therefore the phase change is either 0 or 90 degrees; never more. As a result the amplitude changes are less. A phase change (or none) occurs at each 1/2 bit cell. Also note that the rate of change of phase is the same for either form of QPSK, that is the degrees per bit cell is always 180° or less and the spectrum for both is the same. These characteristics lead us to a better way of spectral shaping that has many advantages.

modulated output is connected to a tracking PLL. The output from the VCO is the spectrally shaped output. The VCO in the PLL tracks the phase change from the QPSK modulator. The low pass tracking filter bandpass characteristics are tailored, allowing the tracking oscillator to lag the phase change from the modulator, thus the rate of change of phase of the oscillator is carefully controlled to obtain the desired spectrum. The result of this PLL technique is somewhat similar to MSK (minimum shift keying) except the phase vector is allowed to rotate more rapidly in that it has acceleration and deceleration for each shift (MSK has a constant rotational velocity). It must essentially be "stopped" each time a transition comes along. The phase then starts rotating; speeds up, and as it approaches the correct phase it slows down and stops before the next bit change occurs. If the RC time constants are adjusted to give the same rotation velocity as for MSK, (it just gets there in time for the next change), intersymbol errors exist and the main lobe is widened considerably past the first nulls.

Several problems had to be overcome before the oscillator would track at the desired rate without overshoot or too much lag. The first problem is the frequency vs phase response of the transistor amplifier. The transistor finally selected has an cutoff frequency of over 400 MHz. A high cutoff frequency allows a data rate of hundreds of kHz without excessive phase shift that would cause the tracking VCO to hunt. In the tracking mode the PLL acts somewhat similar to a first order loop, acquiring lock immediately on power up. The frequency response of a first order loop is a function of loop gain and as a result the loop gain affects the spectrum, and therefore the gain must be held constant at the correct value for the filter parameters chosen. Because a level change in either the reference or VCO output could cause phase detector gain variations; a saturating (limiting) isolation amplifier keeps the drive level to the phase detector constant. A temperature and voltage compensated VCO along with regulated supply voltages and temperature compensated bias voltages are used to eliminate other possible sources of gain variations and undesirable frequency drift.

Because all other circuit variations are eliminated, the loop filter becomes the determining factor in the spectral response.

We found some very unusual characteristics to the loop filter. A second order loop filter (figure 11A & B) was tried first. As the cut-off frequency was lowered, and damping decreased, the spectral response was improved. However, serious intersymbol and interchannel interference developed. It was found that in order not to have any interference, the main lobe (between the first nulls could not be altered. Decreasing R_2 had the greatest effect on spectrum and interference. It soon became apparent that the FCC specifications could not be met without excessive intersymbol and interchannel interference. Various other circuit modifications were tried with no avail until the question was asked "What is really needed in the loop". The answer is of course, reduced loop gain at some discrete frequencies. A series L-R-C circuit from collector to base was tried and is the answer.

This L-R-C will put a notch in the frequency response reducing the gain at that specific frequency thereby putting a notch in the spectrum. It also turns out that several notches can be incorporated and they are all essentially independent. After adding the notches, more rolloff at about 2-3 MHz was required so a single small capacitor (C2) was added between base and collector to further reduce gain at higher frequencies. Figure 13A shows the QPSK output at the intermediate frequency of 30 MHz with the maximum single R_1-R_2-C_1 filtering usable without any interference (altering the main lobe). Compare 13A against Figure 7A & B to note spectral improvement. Figure 13B is with C_2 (High Frequency rolloff) added. Note about 10 dB improvement over 13A at 2-3 MHz.

In Figure 14A the horizontal scale of 1 MHz has been expanded to 500 kHz/division to better observe the effects adding a notch. Figure 14B shows a single high frequency notch added at the 2nd lobe giving about a 10 dB reduction in the 2nd lobe.

Figure 15 is the same as Figure 14B except the horizontal scale has been changed (to 200 kHz/cm) to better observe the effects of the low frequency notch.

Figure 16A shows the notch for the 1st lobe added but tuned below the first lobe, actually into the main lobe. Note that the main lobe has been slightly widened and the first notches are deepened and spread out from Figure 15. When tuned to the lowest frequency, intersymbol and interchannel interference are generated. In Figure 16B the notch is tuned out near the 2nd lobe reducing it more. The notch is sufficiently wide that it still reduces the 1st lobe somewhat. Lowering the frequency of the notch to the high side of the 1st lobe gives Figure 16C which is well within the FCC specifications. Actually Figure 15 just barely meets FCC specs but any variations in component values due to production tolerances could make some units not meet the FCC specifications. It was deemed necessary to incorporate the two notches in order that all production units would fully comply without any problems. Figure 17 shows the final shape compared to a clear carrier. Figure 18 shows a before-after picture of the spectrum reduction.

This technique is a powerful technique in certain applications but is somewhat costly to implement. However, it is much cheaper than some other techniques such as the use of crystal filters.

Figure 21 shows the VCO correction voltage during modulation with the two L-R-C circuits disconnected. When connected severe overshoot and ringing occur but the demodulated data has a lower error rate.

Figure 22A shows decoded data with only the RC & C circuits added to the PLL to modify the spectrum. Adding the L-R-C notches adds ringing to the demodulated signal as shown in Figure 22B. The error rate is actually improved slightly by adding the notches.

The offset QPSK eye pattern is considerably diferent than the non-offset QPSK. Because only 90° phase can be changed at any given time, the eye pattern is a square rotated 45° (diamond) with the decision points midpoint on each side (Figure 19). Added noise (poorer S/N ratio) simply smears out the decision points along with the whole pattern. As the noise

gets worse the whole eye starts filling in. No noise gives almost perfect square. The rounded corners are because of bandwidth limiting in the IF amplifier. Intersymbol interference can be detected because the decision points are not on the ±45° axis. Differences in I & Q amplitudes must be resolved before intersymbol interference can be identified.

Ringing causes small circles and loops around the decision points.

Summary:

The purpose of this presentation is to make others aware of some of the problems involved in system analysis and present one solution to excessive spectral spreading. Each system is different, and an analysis is required to correctly delineate all required system performance specifications before system design can be attempted.

Some forms of modulation (transmission of information) are more bandwidth efficient than others. Some forms have lower error rates for the same signal to noise ratio than others. Error rate and bandwidth efficiency are not necessarily exclusive. However, when both are required system complexity and cost will increase. The amount of complexity, cost, error rate, bandwidth efficiency and path loss need to be evaluated and compromises must be made to optimize the system. The actual system configuration will be a result of the weight given to each parameter when the analysis is performed.

Various users will probably assign different weights to the parameters. Other parameters not mentioned previously will obviously include battery life (power consumption), susceptibility to interference, governmental regulations, number of channels, amount of data to be gathered and others. All of these must be taken into account during the evaluation phase. Often when an analysis is performed, during the analysis the user probably will change priorities or weights assigned to the parameters because much difficulty is experienced in assigning a dollar value to a parameter value. How much is a dB worth?

The technique described herein allows a maximum data rate QPSK system to be implemented at lower cost, with a better error rate and with less occupied bandwidth than other better known techniques. It is not a cure-all and will probably not be the optimum technique in most applications. I hope this presentation has opened some new doors, given new insight or possibly been of benefit to some of the participants of this conference.

REFERENCES

A "minimum" bibliography is included to give only a place to start. Too many references exist to list more than just a few. The ones listed will refer the reader to additional material if desired.

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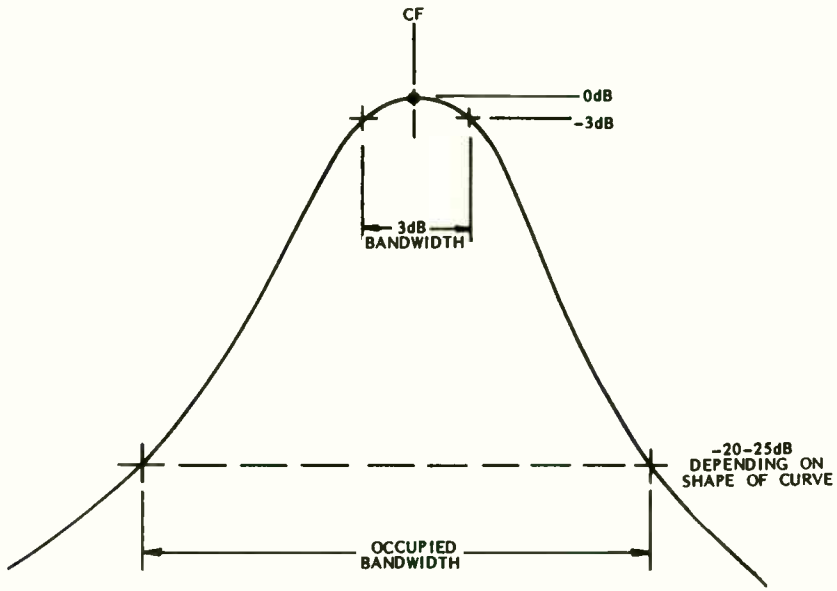


MODULATION SPECTRUM
3dB VS OCCUPIED BANDWIDTH

FIGURE 1

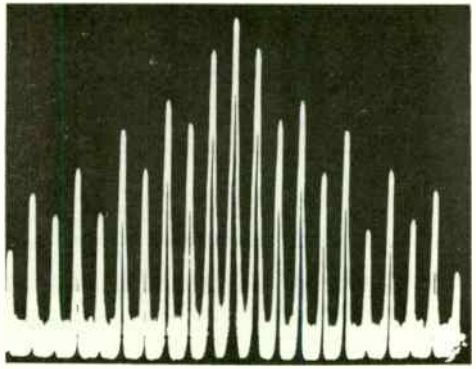


FIGURE 2
100kHz/DIV AM MODULATION 50%
SQUARE WAVE 50 kHz (100 KBPS)

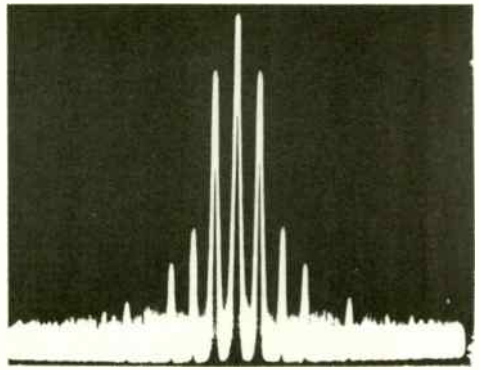


FIGURE 4
AM MODULATION 50%
SINEWAVE 50 kHz (FULLY SHAPED)
100 kHz/DIV

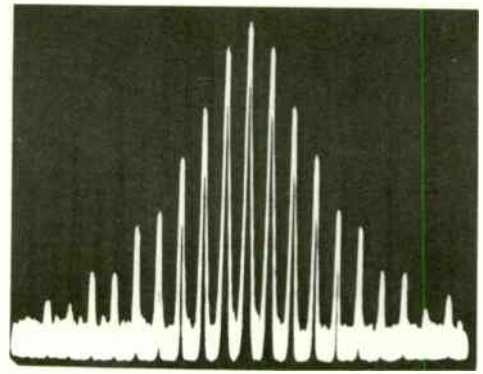


FIGURE 5B
FM MODULATION (M=1.0)
50 kHz TRIANGULAR WAVE
100 kHz/DIV

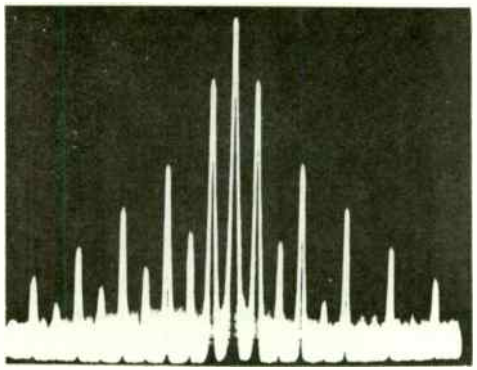


FIGURE 3
AM MODULATION 50%
TRIANGULAR WAVE 50 kHz (100 BPS shaped)
100 kHz/DIV

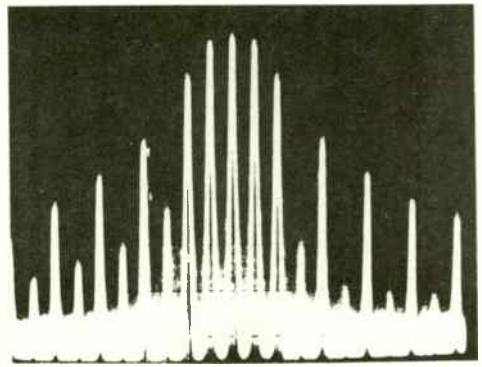


FIGURE 5A
FM MODULATION MODULATION INDEX = 1.0
50 kHz SQUAREWAVE
100 kHz/DIV

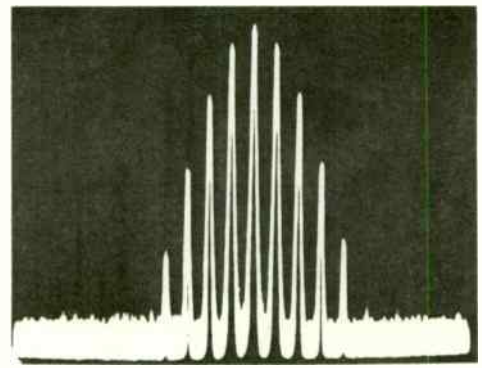


FIGURE 5C
FM MODULATION (M=1.0)
50 kHz SINEWAVE 100 kHz/DIV

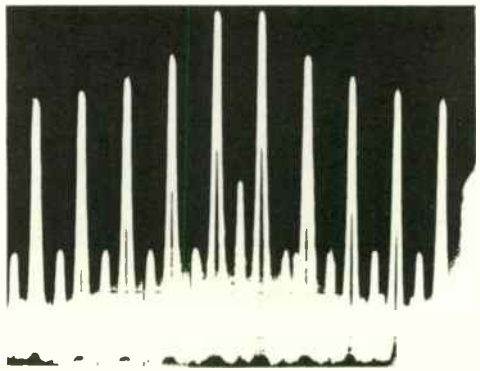


FIGURE 6A
BINARY PSK ± 90° 50 kHz SQUARE WAVE
100 kHz/DIV

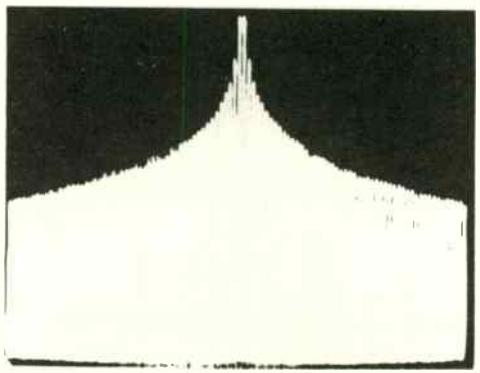


FIGURE 6B
SAME AS 7A EXCEPT 1 MHz/DIV

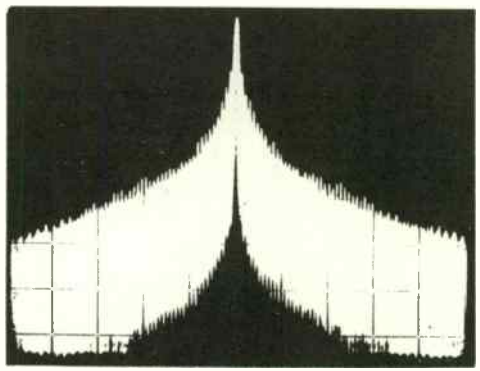


FIGURE 7A
BINARY PSK ± 90°
2 MHz/DIV HORIZONTAL
DATA RATE 170 KBPS

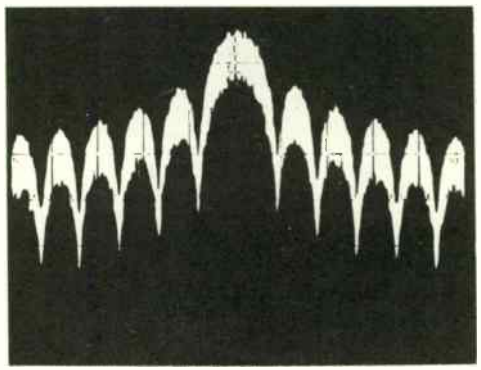


FIGURE 7B
BINARY PSK ± 90°
200 kHz/DIV HORIZONTAL
DATA RATE 170 KBPS

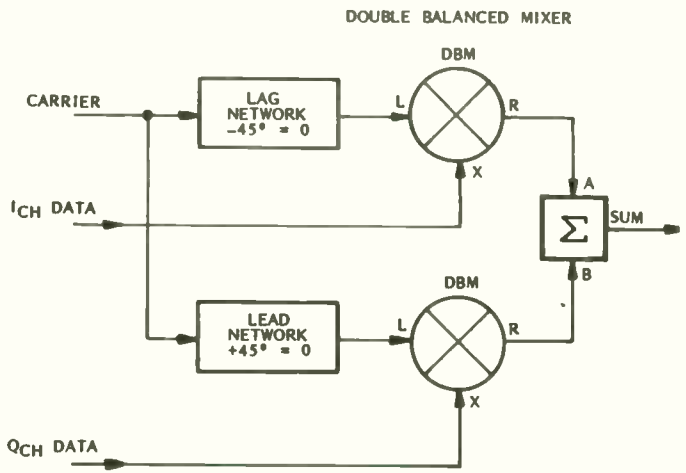


FIGURE 8
QPSK MODULATOR

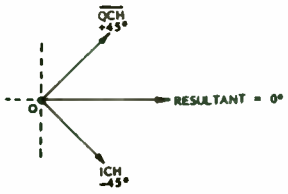


FIGURE 9A

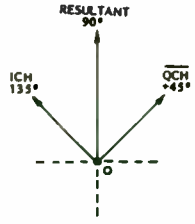


FIGURE 9B

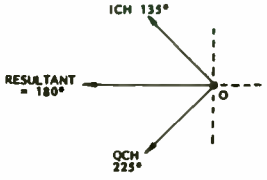


FIGURE 9C

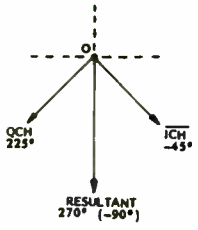


FIGURE 9D

$\overline{\text{ICH}}$ means "Not ICH" or ICH DATA = LOGIC 0

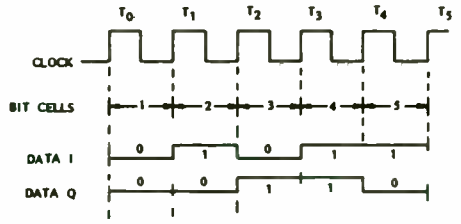


FIGURE 10A
NON-STAGGERED (STANDARD) QPSK

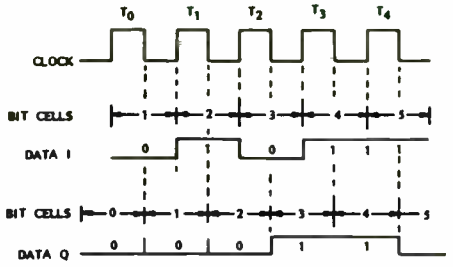


FIGURE 10B
STAGGERED (OFFSET) QPSK

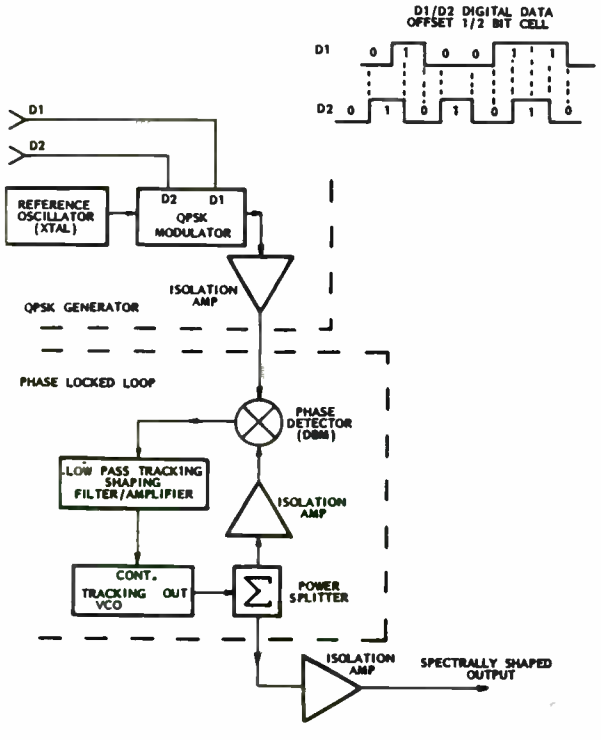


FIGURE 11

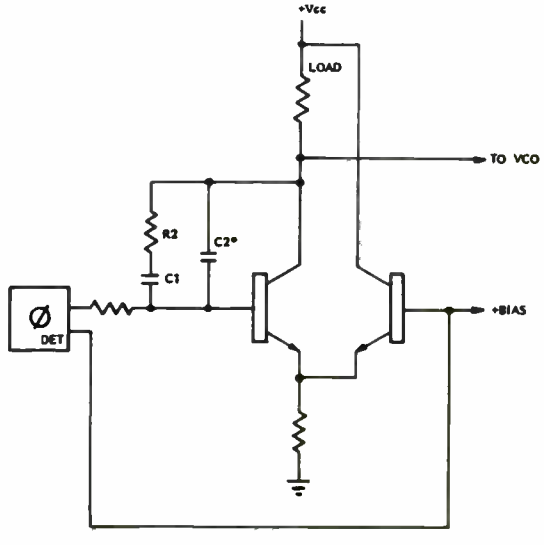


FIGURE 12
BASIC PLL LOOP FILTER/AMPLIFIER

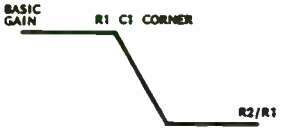
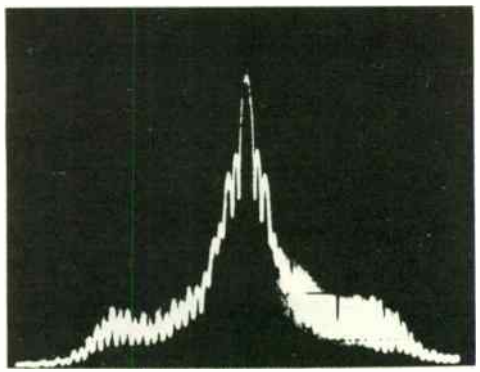


FIGURE 12A
LOOP FILTER RESPONSE

620



Refer to Figure 12

FIGURE 13A
Compare to Figure 7A & B

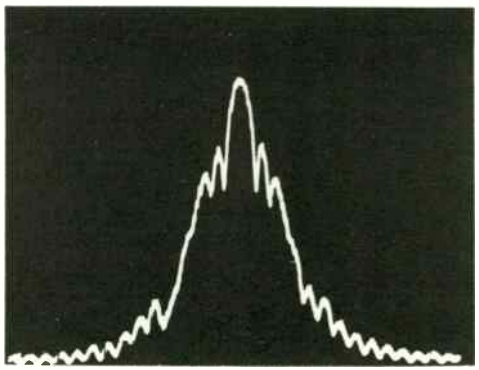


FIGURE 14A

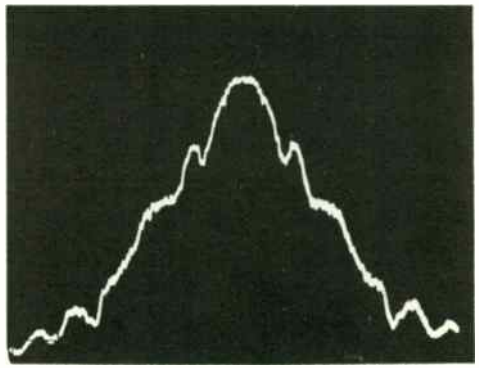


FIGURE 15
SAME AS 14 EXCEPT SCALE CHANGE

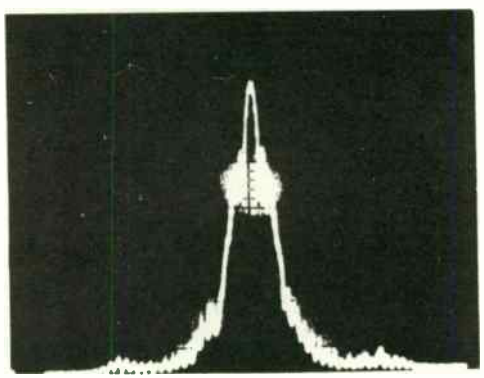


FIGURE 13B
ADDITION OF C2 REDUCTION OF 2-3 MHz TRACK

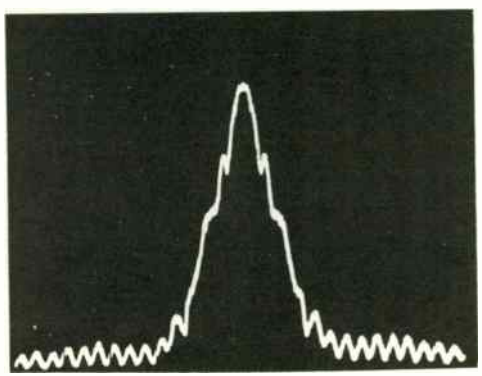


FIGURE 14B
SAME AS 14A EXCEPT 1 SERIES NOTCH ADDED

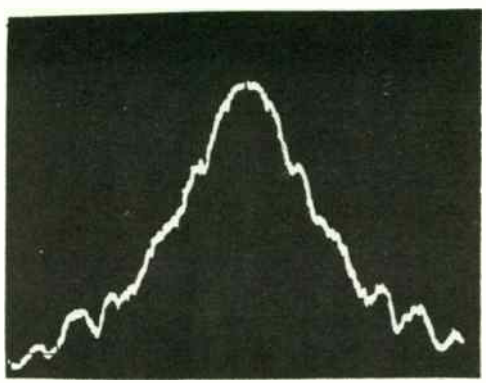


FIGURE 15A
NOTCH 2 ADDED TO LOOP FILTER

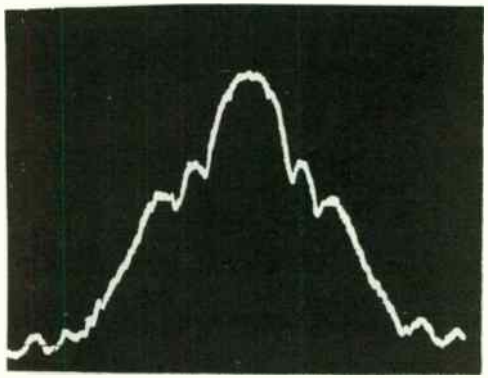


FIGURE 16B
NOTCH TUNED TO HIGHEST FREQ.

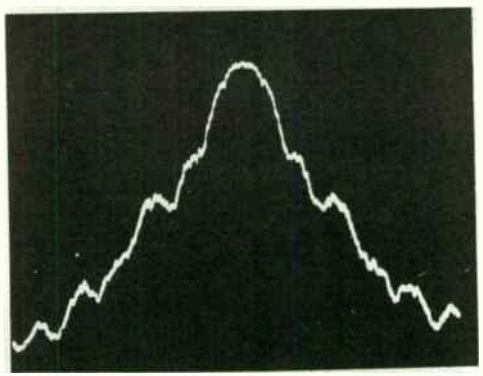


FIGURE 16C
NOTCH TUNED TO REDUCE FIRST LOBE

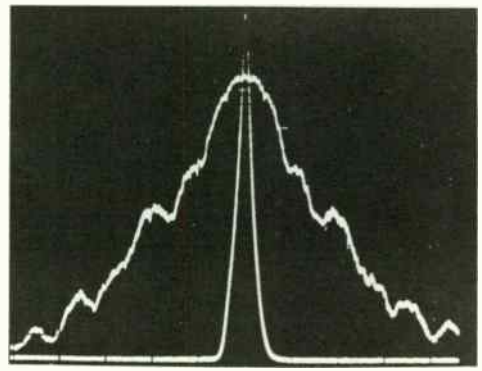


FIGURE 17
COMPARISON OF CLEAR CARRIER WITH SHAPED SPECTRUM

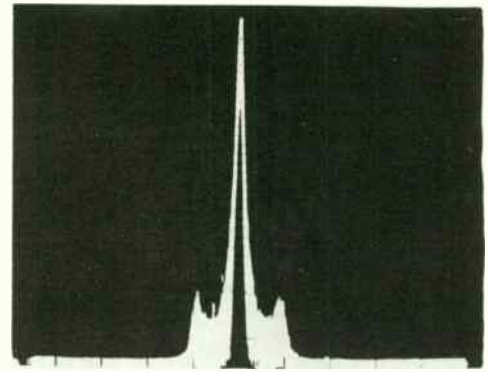


FIGURE 18
AFTER USING SPECTRUM REDUCTION TECHNIQUE

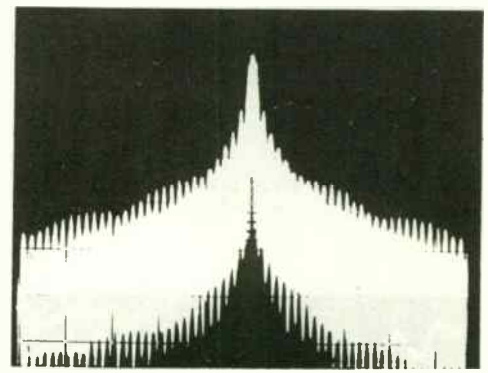


FIGURE 18B
BEFORE SPECTRUM REDUCTION TECHNIQUE

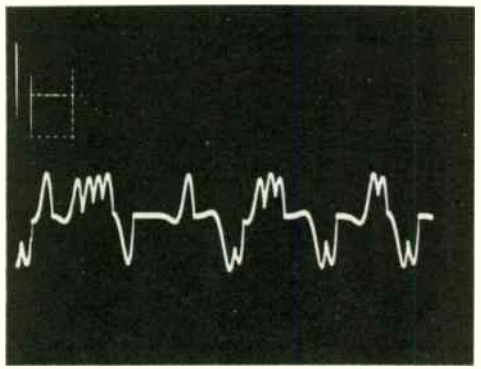


FIGURE 21
VCO CORRECTION VOLTAGE

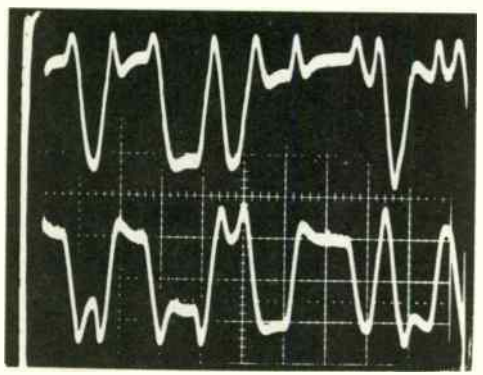


FIGURE 22 (ONE CHANNEL)

*Data made a change in the other channel during this bit period (2t).

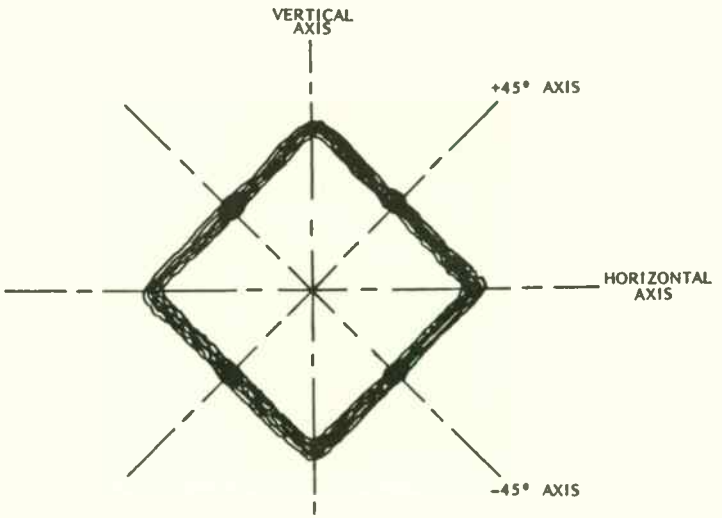


FIGURE 19
EYE PATTERN OFFSET QPSK

BROADBAND HF ANTENNA TESTING

by

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Moray B. King

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Eyring Research Institute
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Abstract

Evaluating HF (2-30 MHz) antenna performance has historically been a difficult test problem. In recent years computer modeled approximations have typically been substituted for test data, particularly to define an antenna pattern in terms of directivity and power gain under ideal conditions. These numerical approximations work well for developing a common reference frame to evaluate the relative performance of a majority of common antenna types (monopole, dipole, sloper, vee, rhombic), but are less accurate predictors of how these antennas will perform when they interact with a real ground environment. It is well recognized that current numerical electromagnetic modeling programs are limited in their treatment of ground interactions in the HF region. Therefore, the relative comparison problem is very significant when buried or ground interactive antennas are addressed. In these special cases, antenna comparison by setting modeling conditions to an idealized ground can indicate unrealistically high relative gain expectations for standard near surface antennas and overly pessimistic values for buried antennas. In fact, some modeling conditions will indicate that the buried antenna cannot work at all!

To address the requirement of making accurate performance comparisons as well as providing design feedback, a broadband antenna test system (BATS) was developed. The system, at its current stage of development, supports computer-controlled, integrated test protocols for the evaluation of all basic antenna parameters. The BATS particularly emphasizes pattern profiles, using swept frequency techniques employing fiber-optically isolated aerial platforms as well as single frequency helicopter towed beacons. Typically, 1 to 20 full-scale antennas can be measured simultaneously in a pattern test, and then compared to each other or reference standards to produce graphic plots in terms of dBr or traceable dBi. The system reduces the complete measurement period of an antenna from months to a few weeks and provides overall accuracy on the order of +/- 1 dB.

Selected References

1. IEEE Standard Test Procedures for Antennas, IEEE Std 149-1979, IEEE, Inc., New York, 1979.

2. C. A. Balanis, Antenna Theory Analysis and Design, Harper & Row, New York, 1982.

3. H. Bruekman, "Helicopter Measures Antenna Patterns," Electronics, Vol. 28, pp 134-136, November, 1955.

4. C. Barnes, Jr., "Transmitter Towed Through the Air Tests Antenna's Radiation Pattern," Electronics, Vol. 38, No. 21, pp 96-101, October 18, 1965.

5. G. E. Barker, "Measurement of the Radiation Patterns of Full-Scale HF and VHF Antennas," IEEE Transactions on Antennas and Propagation, Vol. AP-21, No. 4, pp 538-544, July 1973.

6. C. S. L. Keay and R. E. Gray, "A Simple Balloon Technique for Measuring the Radiation Patterns of Radio Aerials," Electronic Engineering, Vol. 30, pp 322-325, May 1964.

7. J. G. Steele, "Measurement of Antenna Radiation Patterns Using a Tethered Balloon," IEEE Transactions on Antennas and Propagation, pp 179-180, January 1965.

8. R. G. FitzGerrell, "Gain Measurements of Vertically Polarized Antennas over Imperfect Ground," IEEE Transactions on Antennas and Propagation, Vol. AP-15, No. 2, pp 211-216, March 1967.

9. R. G. FitzGerrell, "The Gain of a Horizontal Half-Wave Dipole Over Ground," IEEE Transactions on Antennas and Propagation, Vol. AP-15, No. 2, pp 569-571, July 1967.

10. B. Edward, "Radial Systems for Ground Mounted Vertical Antennas," QST, pp 28-30, June 1985.

11. J. W. Ames and W. A. Edson, "Gain, Capture Area, and Transmission Loss for Grounded Monopoles and Elevated Dipoles," RF Design, Part I, pp 44-45, 47, 48, 50-55, Nov/Dec; Part II, pp 12-14, 16, 17, 20, 22, 23, Jan/Feb.

12. Field Antenna Handbook, ECAC-CR-83-200, Department of Defense Electromagnetic Compatibility Analysis Center, Annapolis, Maryland, June 1984.

Selected Figures - Similar or identical to presentation slides and the figures of the paper.

Figure 1 - The broadband antenna test system components are shown in the context of three basic antenna evaluation modes.

A closed-loop, swept frequency mode drives an antenna under test and records its matching characteristics as a function of frequency. At one or more precisely located points, an electrically small broadband antenna picks up the radiated field from the antenna under test and returns it to the test van via an analog fiber optic link. The field pickup is recorded in a manner that allows direct comparison with matching data. The acquisition instrument for a closed-loop test is either a spectrum analyzer with a tracking generator or a network analyzer with an s-parameter test set.

The open-loop mode evaluates the pattern of an antenna under test by far field illumination at a series of discrete frequencies with a stable beacon transmitter having a well-defined polarization and pattern characteristic. This pattern measurement technique allows simultaneous evaluation of typically 20 full-scale reference and test HF antennas in operationally realistic environments. The absolute power gain (in dBi) of the antenna under test is tied to the predicted gain of a carefully constructed horizontal 1/2 wavelength dipole reference antenna. The dipole reference gain in the horizontal plane is transferred to a vertically polarized 1/4 wavelength monopole reference antenna by rotating the beacon axis 90 degrees and comparing the monopole versus the dipole signal levels (adapted from FitzGerrell 1967).

The open-loop mode also can be used to evaluate signals propagated from distant communications stations. Comparisons can be made between antennas in terms of signal strength and signal-to-noise ratio. If calibrated reference antennas are employed, comparisons of gain can be suggested from the data. Test antennas can be evaluated in both transmit and receive modes.

Figure 2 - This is a test configuration and a typical raw data set for a closed-loop measurement mode with a 2- to 32-MHz sweep. The FWD and REV traces (solid and short dash lines) represent the forward and reverse power levels detected by a dual directional coupler located near the feed point of the antenna under test. The SWR trace in the lower plot is calculated from the FWD and REV traces. The third trace (broken line starting at 5.50) is the field strength level received by a broadband, calibrated monopole antenna located 100 meters from the transmitting test antenna's feed point. The monopole is located on the test antenna's main beam axis at ground level (0 degrees relative azimuth, 0 degrees elevation).

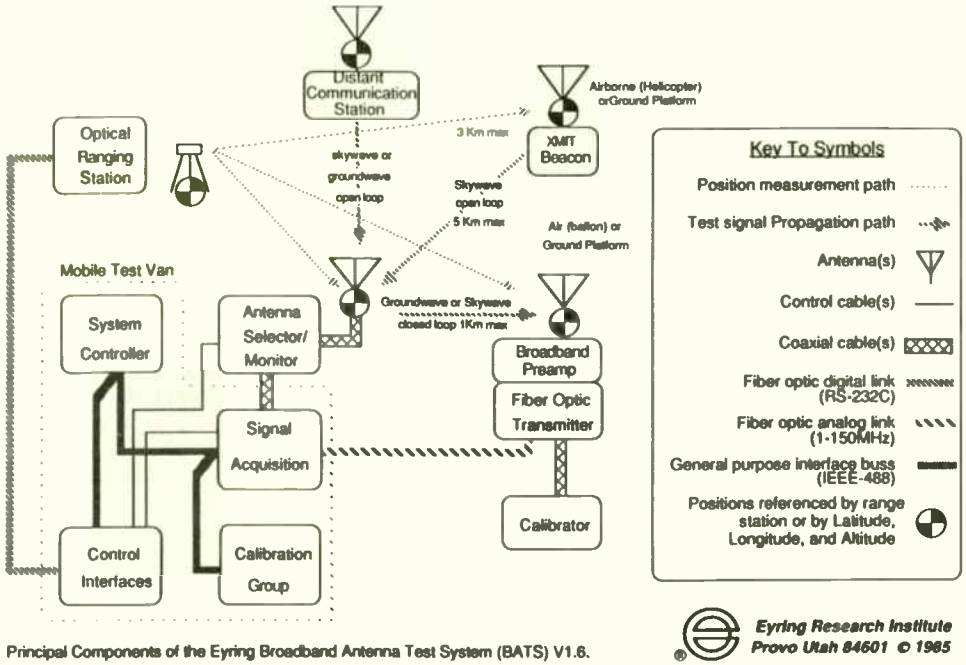
The antenna under test is a 2-element, low-profile, rapid deployment, broadband tactical HF antenna occupying an area of 25 x 200 feet with a maximum height of 2 feet above ground level. This particular antenna configuration has a usable bandwidth of over 30 MHz with an SWR of 2:1 or better.

A full correction to this data set accounts for the errors associated with cable losses, directional coupler calibration factors, and the broadband monopole response. In this example, the FWD trace corrections will produce a flat antenna input power level trace of about 18 dBm. The inflection points and slope of the FIELD trace will also change moderately. The value and units of FIELD will change significantly in converting to a corrected value in dBV/m.

Figure 3 - These are typical flight paths for antenna pattern measurements. Three types of overlapping, cross-correlating flight paths are shown. The circular flight paths are flown at flight levels that obtain azimuth patterns for four elevation angles. The slant range from the beacon to the range finder is maintained greater than or equal to 1 km (e.g., 2.3 km at 30 degrees) and is then corrected to a 1-km reference sphere centered at the antenna under test. The correction process allows comparisons to other flight levels and paths for the same antenna or between different antennas. The vertical rise and descent columns are flown at three reference points to measure antenna elevation patterns from 0 to 40 degrees. The horizontal flyover paths are flown at a constant 1-km altitude above the ground. These paths complement the vertical column flights by providing pattern information from 30 degrees to 90 degrees (zenith). Each path is flown with from one to three polarization attitudes of the beacon to allow complete response characterization (e.g., azimuth flights are flown with vertical and horizontal beacon attitudes).

Figure 4 - The beacon that is suspended below the helicopter is shown along with its three standard flight attitudes. The beacon design is patterned after the "xeledop" concept developed by Stanford Research Institute (Barnes 1965, Barker 1973). The pattern is that of an ideal elementary dipole, which allows correction of flight data amplitude as a function of beacon pattern positioning relative to each antenna under test. The beacon attitudes are described relative to the helicopter's flight path. Therefore, to measure an azimuth pattern with horizontal polarization, the beacon would be towed horizontally on azis (HOA) in a circular path. To obtain a continuation of a vertically polarized, vertical ascent elevation pattern, the overlapping flight path would be a flyover with an HOA beacon altitude.

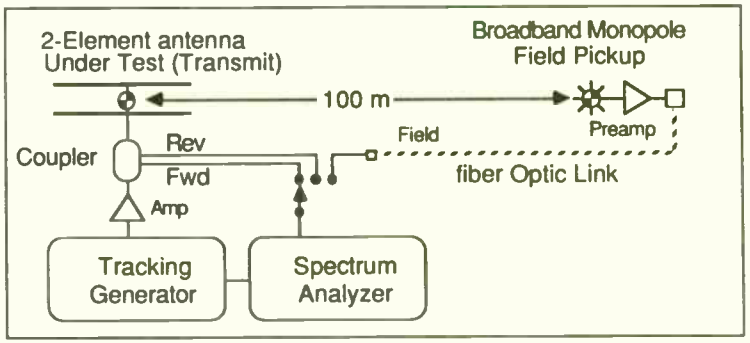
The beacon flight attitudes diagrammed in this figure are shown without a weight harness. In practice, a weight is suspended below the beacon to provide flight stability for towing velocities to in excess of 75 knots.



Principal Components of the Eyring Broadband Antenna Test System (BATS) V1.6.

Fig - 1

Closed-Loop Swept Transmission Measurement Configuration



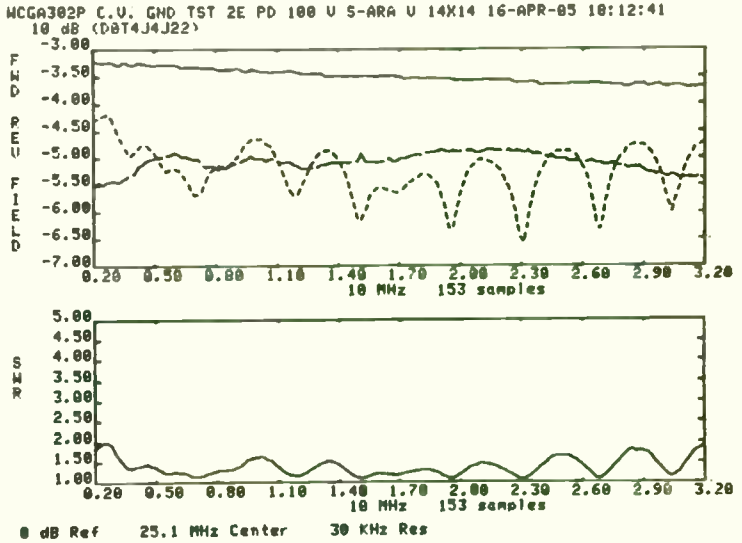


Fig - 2

Typical 1 and 2 km Flight Paths
Cedar Vally airport test site, CedarValley, Utah

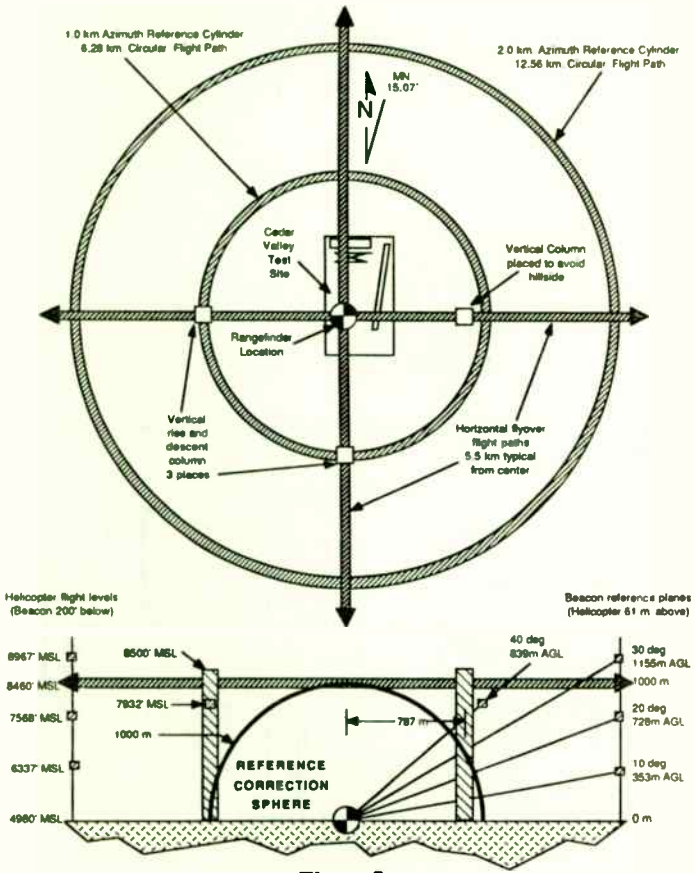
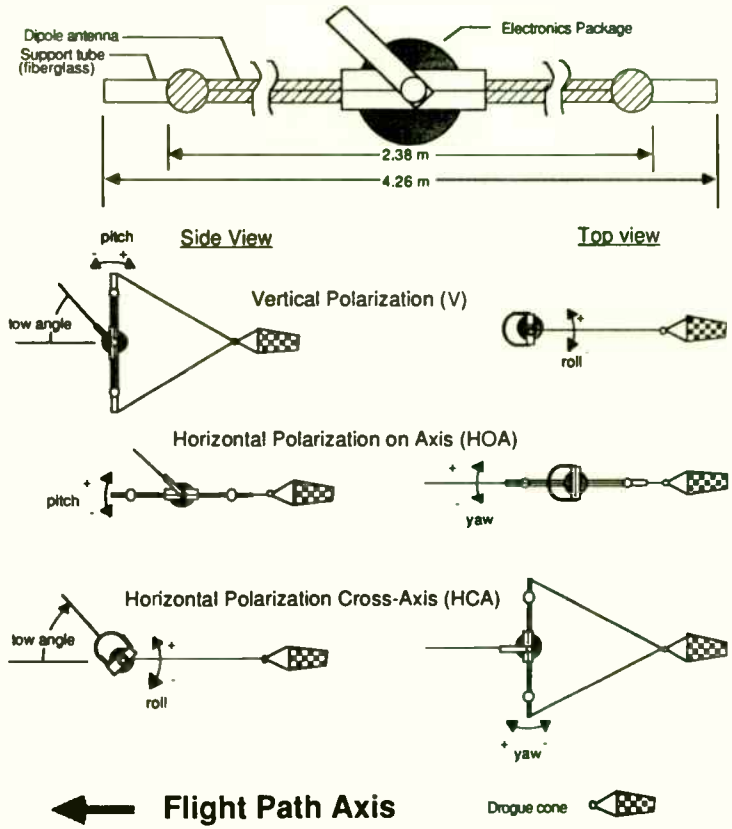


Fig - 3

Beacon Mechanical and Flight Attitudes

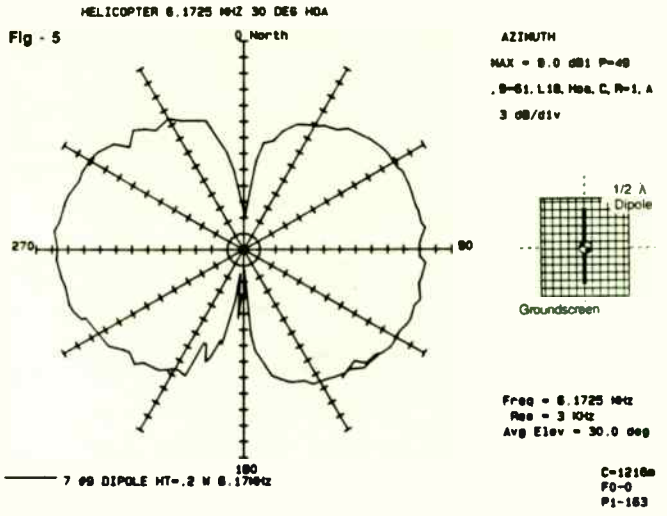


Airborne test terminal basic package
and flight modes for three polarization attitudes.

Fig - 4

Figure 5 - This is a plot of the azimuth response at a 30-degree elevation angle of a horizontal dipole illuminated by a 6.17 MHz horizontally polarized beacon flown in a 2-km circle about the test site location. The 1/2-wavelength (75.8 feet) dipole is positioned 2/10 of a wavelength (31.9 feet at 6.17 MHz) above the center of a ground screen (120 x 148 feet), approximating an ideal reflecting surface. The predicted power gain for this antenna at 30 degrees is 3.95 dBi (FitzGerrell 1967). The pattern approximates 3 dBi at a 90-degree azimuth (interpolated value 4.5 dBi) and 5 dBi at a 270-degree azimuth (interpolated value 5.5 dBi). The data set includes 163 samples with a point taken about every 2.3 degrees. Note the path overlap between the 125- and 140-degree azimuth positions.

Figure 6 - This figure is a complement to Figure 5. The 0-degree elevation position is the 90-degree azimuth point of Figure 5. The gain at a 30-degree elevation is 4 dBi toward the 90-degree azimuth point and 6 dBi toward the 270-degree point. These values are close to the Figure 5 values.



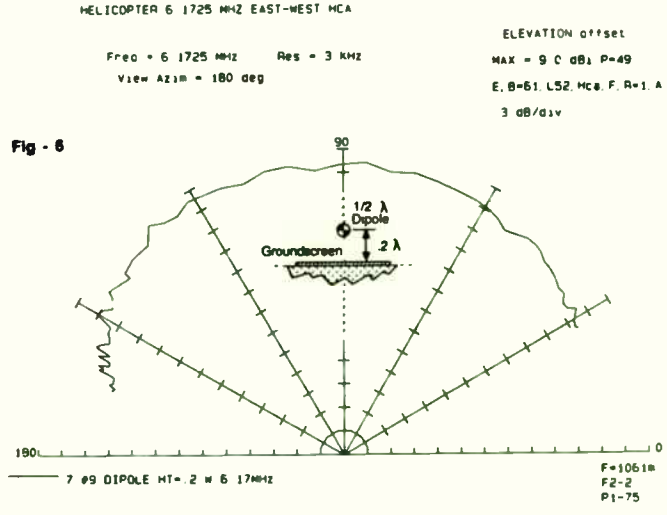


Figure 7 - This is a plot of the azimuth response pattern at a 30-degree elevation angle for a 1/4 wavelength monopole constructed with 36 radials 100 feet long (approximately 0.7 wavelength at 6.17 MHz) and 36 radials 50 feet (approximately 0.35 wavelength). At 6 MHz, the surrounding soil had a conductivity on the order of 0.006 Siemens/meter and a dielectric constant of 12.

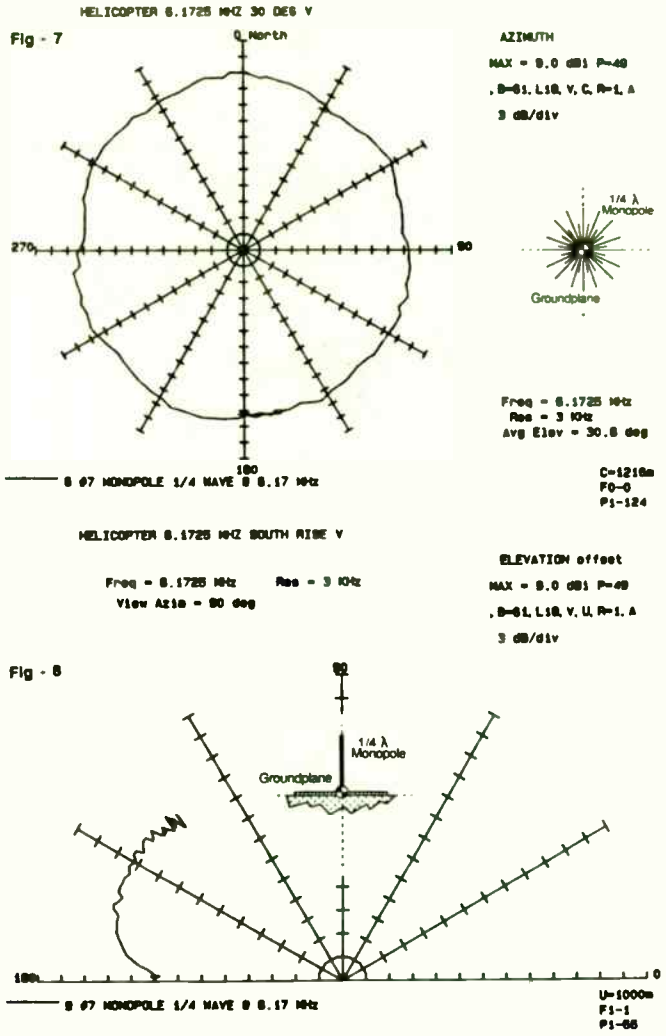
Figure 8 - This is a plot of the elevation response pattern from 0- to 40-degrees for a 1/4-wavelength monopole illuminated by a vertically polarized dipole beacon rising from the 180-degree azimuth position. This pattern suggests a response maximum of 1 dBi over an elevation angle range of 20 to 40 degrees. This is in reasonable agreement with the Numerical Electromagnetic Code modeling predictions of Edward (1985). The measured value is about 1.5 dB lower than the maximum predicted gain for the optimum elevation angle of about 23 degrees. This plot is a complement to Figure 7 which outlines the monopole configuration and environment.

Figure 9 - This is a plot of the vertically polarized azimuth response pattern at a 30-degree elevation angle for a 500-foot long vertical half-rhombic antenna. The rhombic is supported in the center by a 46-foot steel pole. This is a typical broadband tactical antenna with a 600-ohm balun feed and a 600-ohm resistive termination. It is similar in construction to the antenna described in the Field Antenna Handbook (ECAC, 1984, pp 57-58). The antenna has a 2-dBi power gain and a beamwidth of 27 degrees and a 14-dB front-to-back ratio.

Figure 10 - This is a plot of the vertically polarized azimuth response pattern at a 30-degree elevation angle for an 8-element, low-profile, rapid deployment, broadband tactical antenna. This antenna is less than 2 feet high and is deployed in a 145 x 150 foot area. This configuration has a 2-dBi power gain, a beamwidth of 25 degrees, and a 3-dB asymetry in its bidirectional pattern. Directional deployment can produce front-to-back ratios in excess of 10 dB.

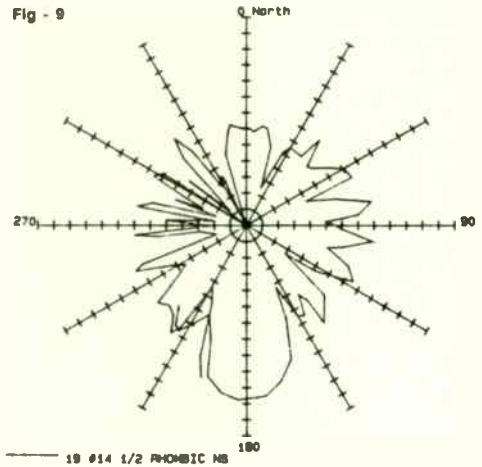
Figure 11 - This is a plot of the vertically polarized elevation response measured for an ascent column located at the 180-degree azimuth position. The peak power gain over a 0- to 40-degree elevation range is -2 dBi for this 35-foot monopole with a high performance tuner.

Figure 12 - This is a plot of the vertically polarized elevation response acquired in the same test as the monopole of Figure 11. The power gain of this 8-element, low-profile antenna has been optimized by asymetric deployment to match the tuned monopole power gain within 1 dB from 0 to 20 degrees. From 20 degrees to 90 degrees, it exceeds the monopole without a null and with a peak gain of -1.5 dBi.



HELICOPTER 15.3415 MHZ 30 AZIM V

Fig - 9

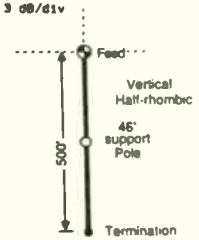


AZIMUTH

MAX = 9.0 dBi P=43.5

.B=61, L30, V, C, R=1, A

3 dB/div



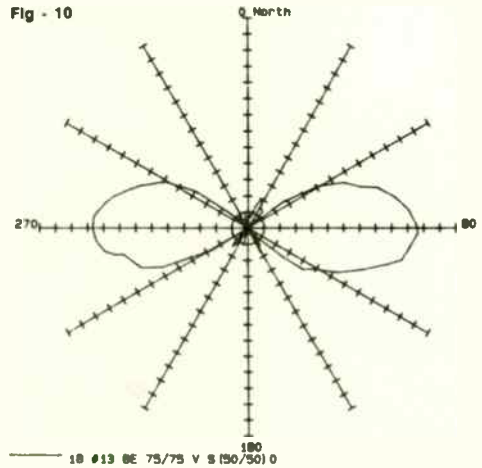
Freq = 15.3415 MHz
Res = 3 KHz
Avg Elev = 29.9 deg

C=1216e
F0-0
P1-121

19 #14 1/2 RHOMBIC NB

HELICOPTER 15.3415 MHZ 30 AZIM V

Fig - 10

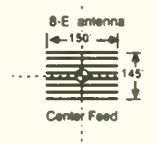


AZIMUTH

MAX = 9.0 dBi P=43.5

.B=61, L30, V, C, R=1, A

3 dB/div



Freq = 15.3415 MHz
Res = 3 KHz
Avg Elev = 29.9 deg

C=1216e
F0-0
P1-121

18 #13 8E 75/75 V S(50/50) 0

HELICOPTER 3 1925 MHZ VERT ASCENT S V

Freq = 3 1925 MHz Res = 3 KHz

View Azim = 90 deg

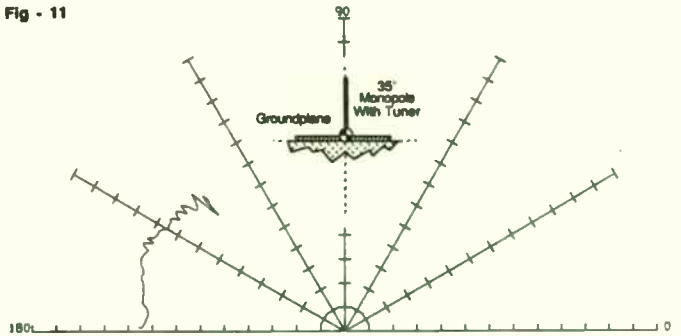
ELEVATION offset

MAX = 9.0 dBi P=46

B=61 L94 V, U R=1 A

3 dB/div

Fig - 11



9 #7 3 1925 MHZ TUNED 35' MONOPOLE

HELICOPTER 3 1925 MHZ VERT ASCENT S V

Freq = 3 1925 MHz Res = 3 KHz

View Azim = 90 deg

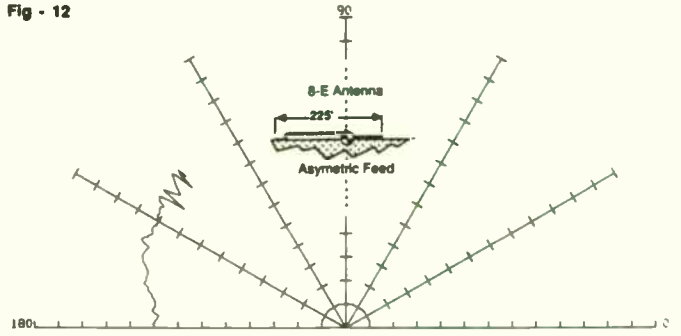
ELEVATION offset

MAX = 9.0 dBi P=46

B=61 L94 V, U R=1 A

3 dB/div

Fig - 12



21 #16 8E 150/75 V S(125)

RADIO SYSTEMS TECHNOLOGY
13281 GRASS VALLEY AVENUE
GRASS VALLEY, CA 95945
(916) 272-2203 123.3MHz

HOW TO BUILD SIMPLE

AND NOT-SO-SIMPLE

TEST EQUIPMENT IN YOUR OWN LAB

By: Jim Weir
VP Engineering, RST
Sierra College Faculty

ABSTRACT

Design data and test results on 6 pieces of test equipment intended for "home-brew" RF measurements is given. Construction details and component sources are provided for low-level crystal detectors, low-power signal splitters, resistive low-power VSWR bridges, microstrip medium-power VSWR bridges, R + jX meters, and RF front-end noise generators.

INTRODUCTION

It has not always been possible to go down to Joe's Used Equipment Emporium and buy a Q-meter or VSWR bridge that would work at 200 MHz. In matter of fact, before Bill and Dave got into the act, quite a few RF designers had to first design and build their own test equipment, and then use this home-made gear to test their new products.

It is also true that of any random group of RF engineers, over 30% will some day start their own company. A new enterprise such as this is not always flush with venture capital; at times it becomes a matter of economic necessity to "roll your own" test gear. While not quite as pretty as store-boughten test equipment, these boxes have served their intended function in my personal company for over 20 years. Although the photos (for the most part) show nice neat construction, you must remember that these particular boxes were constructed of easy-to-obtain components and manufactured for the photographs in this paper. The original pieces of gear would gladden the heart of those of you fond of webs spun by stoned spiders.

Finally, to those of you offended by my admittedly simplistic and anachronistic concepts, I commend to you the wisdom of the philosopher who said, "Those of us who do not remember the ways of the past are surely condemned to repeat them." Those of you who have been around this business for a significant fraction of a century know full well that these designs are not new. I claim neither invention, advancement of the state of the art, nor brilliant insights into these products; I, like you, am a poor workaday sluggard trying to keep the company one step ahead of the wolf in IRS clothing. Enjoy.

THE SIMPLE CRYSTAL DETECTOR

Crystal detectors have been with us since that unknown experimenter first jabbed a chunk of lead sulfide (galena) with Junior's diaper pin and noted that all of a sudden that his baby got rhythm. Further investigation showed that if any semiconductor (galena, germanium, silicon, gallium arsenide, selenium, etc.) was alloyed either by pressure (catswhisker) or by diffusion, the resultant JUNCTION would pass current in one direction only, and thus make a very good amplitude or envelope detector. In the ensuing years, we have done little other than refine the manufacturing techniques of the crystal diode, and to this day, there is no better generally available detector than the old faithful catswhisker germanium diode.

Admittedly, you can't really call a crystal detector design that uses a diode available in the late 1940's the cutting edge of technology. However, as a lab partner, I would consider this design as my most-used piece of test gear. Although the design appears to be cut-and-dried, there are a couple of subtleties that you ought to be on guard for. (See Schematic 1). AUTHOR'S NOTE -- 1N270 and 1N34 are interchangeable in all the designs in this paper.

First, the input is terminated in 47 ohms in order to work in a 50 ohm system. Yes, if you have 51 ohms in the stockroom, that would be a better match, but my company only keeps the 10% values on the shelf. Be sure that you use a carbon composition or carbon film resistor to keep the reactive part of the resistor to a minimum. I think it is obvious that if you need any other input impedance, just change the resistor to any value you please. The intrinsic impedance looking into the unterminated input is not measurable easily; the best I can say is that it is above 5K ohms (the limits of my equipment.)

The input coupling capacitor is a .001 uF. If I had intended for this detector to be used much above 150 MHz, I would have reduced this capacitor to 100 pF or so. Although at 150 MHz the .001 is well above it's self-resonant frequency, the input impedance of the diodes is so high (<5K ohms) that a little jX doesn't seem to make much difference.

The diodes are the aforementioned World War II design 1N34 (or 1N270) germanium parts. Yes, I've tried hot-carrier and Schottky barrier devices and I cannot get them to do as low a level of detection as the good old germanium diodes.

50 pF was used as the bypass capacitor simply to keep any self-resonance above 200 MHz. (A 50 pF disk ceramic with 3 mm leads has a self-resonance at about 250 MHz.). BE CAUTIOUS of fooling with the 10K - 50 pF time constant. This author grabbed what he thought was 50 pF (and what turned out to be a miniature .005 uF) to make a detector and then spent DAYS trying to figure out why his AM transmitter was both audio frequency sensitive and would not modulate worth a hill of beans.

Photo 1 shows the old-faithful open-board design. While somewhat primitive, this little rascal has been my bench companion for over 20 years. I will caution you, though, that this open-board construction bit me on the behind a couple of years ago. I was working on a 20 watt 125 MHz. transmitter, and had about 30 dB of padding between the transmitter output and this detector. One day the modulation would look crisp and clean, and the next day the whole modulation envelope was garbage. After redesigning the modulator, the output bandpass filter, the final stage feed network, the driver, and several miscellaneous stages, I noticed that simply repositioning the crystal detector made all the difference in the world. Placing tinfoil all around the detector cleared up all the distortion! The high-power RF stage had been radiating directly into the detector diode leads, and the phase of the directly radiated signal combining with the attenuated signal was a function of how far the detector was from the finals. Photo 2 shows the solution to this little problem. One question may be where to buy the brass tubing for the shield. Any hobby model shop worth their salt has a large selection of thinwall brass tubing that will fit the BNC connectors as a slip fit.

This detector can be built for less than a dollar in components for the open-faced version and less than three dollars for the closed-in version (including connectors for the closed version).

SIGNAL SPLITTER

With most transmitter projects, I like to look at the swept frequency response, the spectral analysis (for unwanted birdie products), and have a counter on the output in case I want to set a spot frequency. Without some sort of splitter, I am forever swapping coax connectors from the transmitter output to one piece of test equipment or another.

The type of splitter I have found most useful is one that is matched at the input to 50 ohms and splits the signal equally between two outputs. I also demand that the outputs be isolated from one another so that if I need to take one of the test instruments off the line for a quick check of some sort that it does not upset the other measurement. The third output I have found to be most useful is a -20 dB. coupling of the input for a frequency counter or

deviation meter. Usually, I have the transmitter padded down to the +10 dBm level by the time it hits this splitter, so power dissipation is not a real problem.

Photo 3 and Schematic 2 show the construction of a "Wilkinson" style hybrid splitter constructed from two pieces of 75 ohm coaxial cable and one balancing resistor. The -20 dB. coupler is comprised of two resistors.

As you can see from the test results on the schematic, the coupling to the output ports is remarkably constant over two octaves, but the isolation and input VSWR is rather sharply tuned. The design center frequency of this particular splitter was 125 MHz., and both input return loss and output isolation remained within -18 dB from 100 to 150 MHz.. Since the -20 dB port is resistive, you might expect it to remain fairly constant, and it does so from 50 to 250 MHz..

VSWR DETECTOR - LOW POWER

This VSWR indicator has seen yeoman work in our sweep testing of filters, first-cut antenna testing, and RF input matching. Although the resistive coupling limits the input power to a half a watt or so (due to the use of quarter-watt resistors), this little board has been in on the design of dozens of VHF antennas and amplifiers. (See Photo 4). For those of you with a neatness fixation, Photo 5 shows the circuit built into a "Hobby Shack" minibox. The circuit design is given in Schematic 3, along with a performance graph. Using all new parts, this bridge can be built for less than a dollar in components and less than $5 including connectors.

Those of you familiar with the literature on this bridge in the various radio amateur handbooks may be a bit surprised at the resistor values. Most of the articles in the handbooks use 50 ohm (47 ohm) resistors throughout the bridge; the values presented on the schematic have evolved over the years as the best compromise for open-short ratio and depth of null with a precision 50 ohm load. Once again, if you are using this bridge to make swept frequency measurements, the 10K - 50 pF time constant sets the upper audio frequency response limit. If you find that too much of your fine detail is missing from the sweep response curve, either slow the generator sweep speed down or reduce this time constant.

VSWR DETECTOR - HIGH POWER

When dealing with power amplifiers, it is nice to be able to drive a couple of watts into the input and check for match. Also, it is quite helpful to be able to take the 10 or 20 watts out of a power amplifier and check the VSWR of the antenna or load that you are driving into.

The VSWR detector shown in Photo 6 uses a microstrip directional coupler design (called a "Monimatch" by some old-timers) that first saw the light of day as a coaxial device made by inserting a thin piece of enameled magnet wire between the braid and center insulator of a piece of coaxial cable. Later refinements have allowed us to used etched circuit board and microstrip techniques to achieve the same results. See Photo 7.

The circuit and etching dimensions shown on Schematic 4 should allow the clever engineer the capability of reproducing this bridge for his own use. The open-short ratio is remarkably good for a device as simple as this one, and the bridge has been used from 20 to 200 MHz. with excellent results. Since the coupling between main line and coupled line is on the order of 20 dB., there is very little loss in the main line, and the bridge will actually work down to about a milliwatt (dependent a bit on frequency) in the main line. Upper power limit is a function of the diode breakdown voltage; using the specified 1N270, I would feel uncomfortable with more than 100 watts at VHF in the main line. Using the parts list given, this bridge can be built for less than $20, not including the cost to etch the pc board.

R + jX BRIDGE (RX METER)

Although it is nice to know the input VSWR of your new design, there are times when it would be preferable to know the input impedance as it actually exists at the frequency you actually intend to use it. For instance, perhaps the data sheet does not cover the transistor you want to use in the mode you want to use it. You must then measure the device under actual operating conditions to characterize and analyze the little rascal. Another use of the RX bridge is to measure component values using actual lead lengths used in your circuit. You'd be surprised how many picofarads a 100 pf. capacitor at 100 MHz. measures with half-inch leads (it's darn near a short circuit). It is nice, also, to be able to drive a hundred milliwatts or so of RF energy into a class C amplifier transistor to be able to measure the input impedance under actual conditions.

Most articles in the handbooks use either war-surplus antenna tuning capacitors (WW II, that is), or an unusual "differential" capacitor made by the Hackensac Capacitor and Storm Door Company of Horse Cave, Kentucky -- it is only available from Bill's Garage and Hi-Tek Component store in East Bumpoop, Tennessee, and then only on alternate Tuesdays. The one in this article uses one section of the RF tuning capacitor out of any standard FM pocket radio.

The resistive bridge is nothing more than our old friend the Wheatstone, with as much of the stray reactance as possible removed from the circuit by means of heavy wire bonding and the use of a brass ground plane behind the front of the chassis. See Photo 8 and Schematic 5.

The reactance part of the bridge is also quite simple; it is a parallel resonant circuit comprised of the aforementioned FM radio tuning capacitor and an inductor wound from #18 wire and tapped so that it could be switch-selected to various inductance values.

Once again, most circuits of this type use a sensitive 50 uA meter as the null indicator. Not only are these meters expensive, but if you happen to put in a little too much RF and the bridge is badly unbalanced, you now have your meter needle neatly wrapped around the peg of what was your meter. I much prefer to use a garden-spec op-amp and limit the current out of the amplifier into a cheap 1 mA. meter to about 150% of full scale. It will still bang against the peg if overloaded, but it will not destroy itself in doing so. Not only that, but your sensitivity is about 10 times greater with the amplifier than with the straight meter.

Calibration of the bridge is rather simple. Input an RF signal at about one milliwatt at the lowest frequency for which full-scale CCW rotation of the tuning capacitor (maximum capacitance) is nullable at some setting of the inductor. For this particular bridge, that frequency happens to be 30 MHz.. Null the meter as best as possible and use carbon comp or carbon film resistors to calibrate the 500 ohm potentiometer. I have calibration marks from 10 ohms to 2.2K ohms. Then take 20 pF. capacitors and calibrate the tuning capacitor. With the specified capacitor, you will be able to get marks from 20 to 160 pF. at 30 MHz..

To use the bridge, simply input the desired RF signal and place the bridge tuning capacitor at mid-scale directly on one of the calibration marks. Tune the bridge potentiometer to infinity and adjust the inductor switch for best null. Slightly adjust both tuning capacitor and potentiometer for the deepest null obtainable. Then place the unknown load across the load terminals and adjust the capacitor and potentiometer for null. The resistive part of the load is read directly from the calibration marks of the potentiometer and the PARALLEL EQUIVALENT reactive part of the load is the DIFFERENCE between the starting point on the variable capacitor and the final null value. If you go clockwise, your load is that many picofarads capacitive, and if you go counterclockwise, the load is that many "picofarads" inductive. (For those of you working around digital engineers, just start talking about inductance as being measured in picofarads and watch the strange looks on their faces.)

The bridge rapidly loses accuracy above 100 MHz.. This is due to the rather wide spacing of the front-panel components (see Photo 9) and the resultant parasitic inductance of the wires necessary to connect the components together. As this bridge was meant for use on a 50 MHz. project, the frequency limitation was not a great problem. If it ever became necessary to increase the frequency range of the unit, I would probably do away with the switched inductor (the cause of most of the parasitic inductance) and simply build a bridge for each frequency band of interest. One fixed inductor with this capacitor ought to be able to cover an octave of useful range without a lot of trouble.

RF NOISE GENERATOR

In the design of low-noise RF "front ends", the device of choice for final design tweaking is the good old Noise Figure Meter. This is a rather large and expensive instrument that uses a vacuum tube (or a small expensive instrument that uses a solid-state noise source) to produce an exact amount of broadband noise that may be used for an exact calculation of noise figure. The noise generator in this article will NOT give you an exact noise figure measurement, but will give you a method of tweaking your RF stage for best noise performance. Given a very short equation and a couple of fairly easy measurements (which you will have to take anyway for making up the specifications), the noise figure may be easily calculated.

As those of us who thought we knew how to design power supplies found out, a diode in reverse breakdown (i.e. a "zener") that is unbypassed for RF makes a perfectly marvelous noise generator. This noise generator makes use of the fact that a zener is wonderfully noisy and amplifies that noise in a wideband amplifier to produce about 15 dB of "excess" noise. See photo 10 and Schematic 6.

The old way to use one of these noise generators was to set the volume control of the receiver under test to a reference level, input the excess noise source, and adjust the input amplifier conditions (bias, tuning, input match, etc.) for best ratio of reference level to level with the excess noise input. The only problem was that with input changes, so changed the reference level, and thus it became an iterative sort of process -- set the reference, tune, set the reference, tune, set the reference... . This got very old very quick.

This generator, though, uses an audio oscillator to gate the noise source on and off. Now the engineer has the choice of viewing the output of his receiver on an oscilloscope and be able to look at the reference level and the excess noise level at the same time. Not only that, but by a judicious choice of gate frequency (1000 Hz.), the old standby "415" type of SWR indicator (which is nothing more than a very narrowband 1000 Hz. meter calibrated in decibels) can be used as an indicator of best noise figure. The entire noise generator is constructed on a single piece of scrap pc board (see Photo 11).

Of course, this generator cannot be used for absolute noise-figure measurements, but by knowing the bandwidth of the receiver and the input signal to produce a given signal-to-noise ratio, the noise figure may be easily calculated.

CONCLUSION

This paper was meant more as an introduction to the fledgling RF engineer into the wonderful world of making measurements on a shoestring than to the old-timer that has seen these circuits being used for years. I do NOT begrudge the purveyors of kilobuck test equipment the right to chuckle a bit at the homespun roughness of the cloth from which these test boxes were cut, but I would point out that making and using equipment like this just whets the appetite to get your hands on a really nice piece of gear.

Not only that, but it's sort of fun to see just how close I can come with one engineer using hackysack parts to Bill and Dave's boxes that have hundreds of engineers using Mil-Spec pieces. You'd be surprised; try it, you'll like it!

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1. Widin, "SWR Bridge", Ham Radio, October 1971, pp 55-56

2. Keen, "A Simple Bridge For Antenna Measurements", Ham Radio, September 1970, pp 34-38

3. Kluge, "Noise Bridge Simplifies RF Measurements", EDN, July 1985, pp 61-62

4. Willmar K. Roberts, "A Guide To F.C.C. Equipment Authorizations", published by the author, W.K. Roberts - 4637 Van Kleek Dr. -- New Smyrna Beach FL 32069 -- (904) 427-3612.

5 Helge O. Granberg, "Linear Amplifiers For Mobile Operation", Motorola applications note AN-762, 1976

6. "The ARRL Handbook", 42nd Edition (1965), "The Monimatch", pp 356, 357.

7. "An N-Way Hybrid Power Divider", IRE Trans MTT, Ernest Wilkinson, January 1960, pp 116-118.

PARTS SOURCES

1. Mouser Corporation, 11433 Woodside Ave., Santee CA 92071, (619) 449-2222. Suppliers of germanium diodes, resistors, capacitors, integrated circuits, FM radio tuning capacitors, rotary switches; general catalog available for the asking.

2. Calrad Electronics, 819 N. Highland Ave., Los Angeles CA 90038, (213) 465-2131. Suppliers of meters, chassis boxes, jacks, plugs, binding posts; general catalog available for the asking.

3. Radio Shack. Available in your own home town.

-30-

PHOTO CAPTIONS

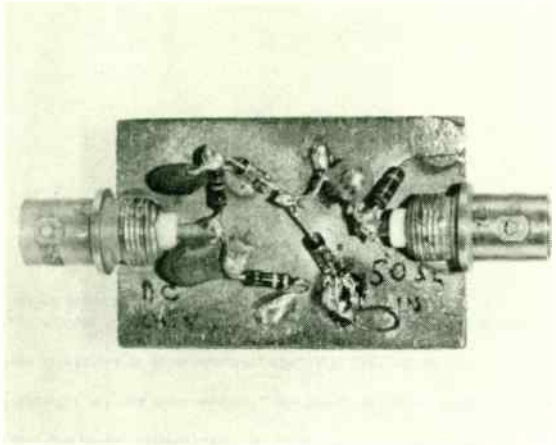


PHOTO 1 The basic, elementary form of the detector. This is Old Faithful. I've replaced her input resistor a dozen times, her diodes more than once, and she just keeps on chugging. Building this detector on a PC board scrap makes repair quite simple and frequency response excellent past 400 MHz.

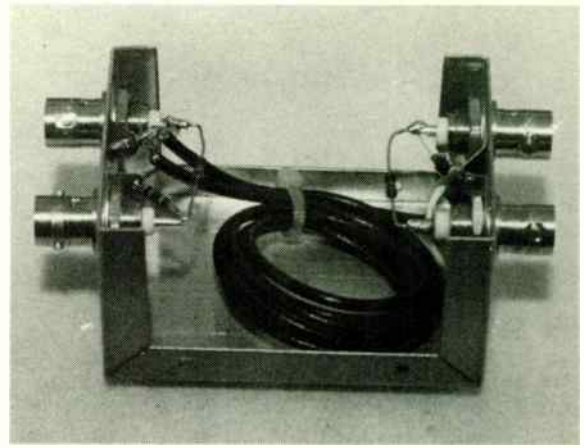


PHOTO 3. The splitter coax is shown rolled up to fit into the chassis.

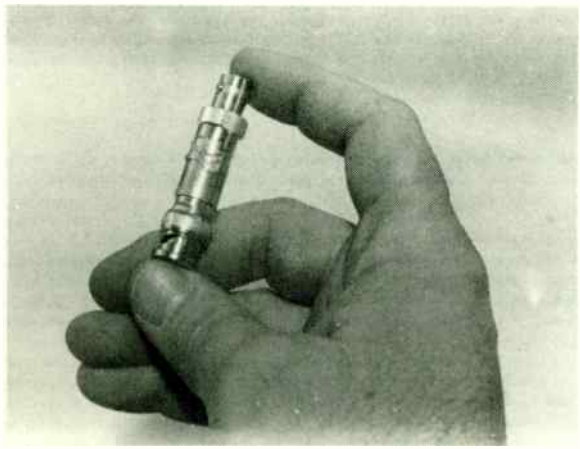


PHOTO 2. When the outside world interferes with the the detector, the only answer is to shield it. A nickel's worth of brass prevents direct radiation into the diodes.

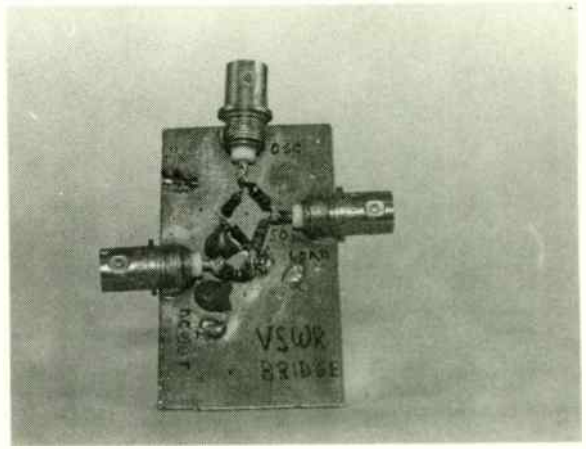


PHOTO 4. The innards of the homebrew VSWR bridge. Once again, the techniques of building homebrew circuits on scrap PC board material are illustrated.

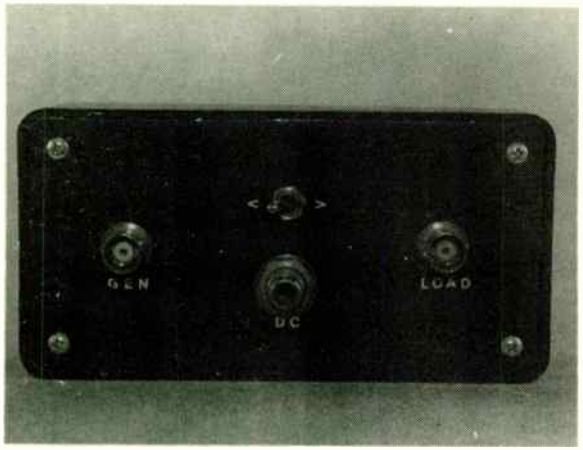


PHOTO 5. If the beancounters want to see neat, clean progress, then show them these circuits dolled up in store-boughten housing.

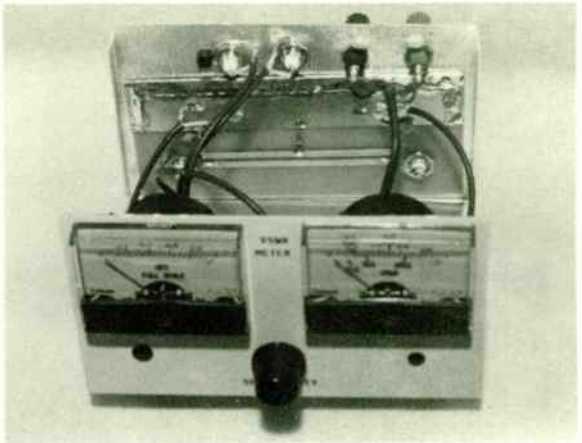


PHOTO 7 The RF coupling lines on the back of the chassis show how the microstrip design is implemented. The 39 ohm matching resistor is the central part of the photo.

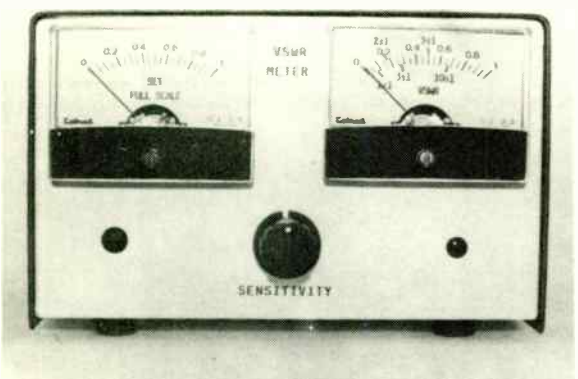


PHOTO 6. Dual meters on the faceplate make VSWR measurements a single knob task.

PHOTO 8. The Impedance Bridge will analyze parallel impedances from 20 pf to 10 ohms.

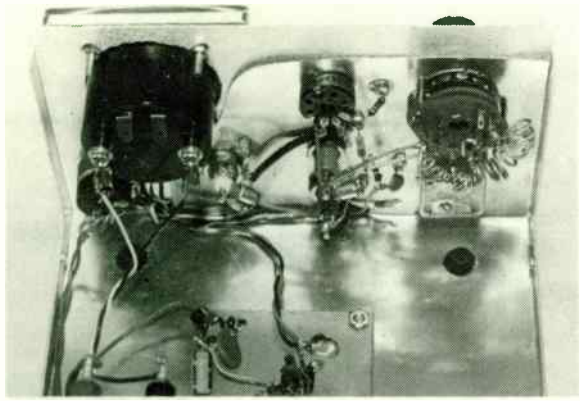


PHOTO 9 The front panel of the Impedance Bridge shows the brass ground plane below the RF front panel components. All RF ground connections are made to this brass plane.

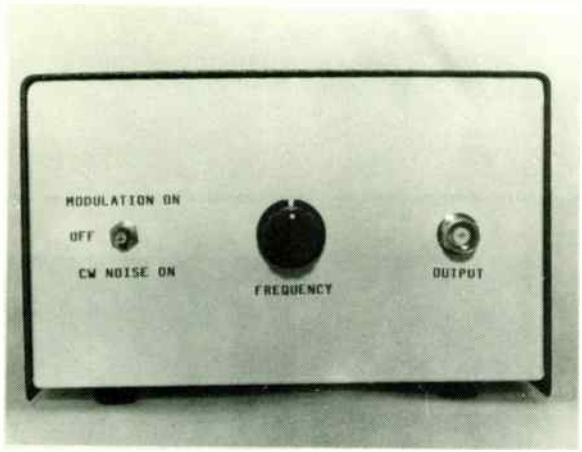


PHOTO 10 The front panel of the RF noise generator. Note that both continuous noise, modulated noise, and noise off can be selected by the front panel switch.

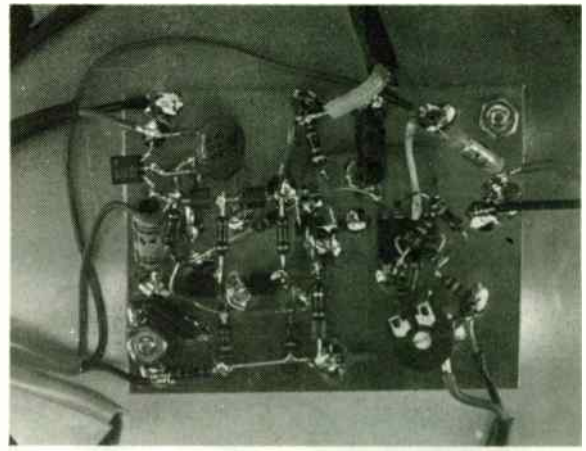
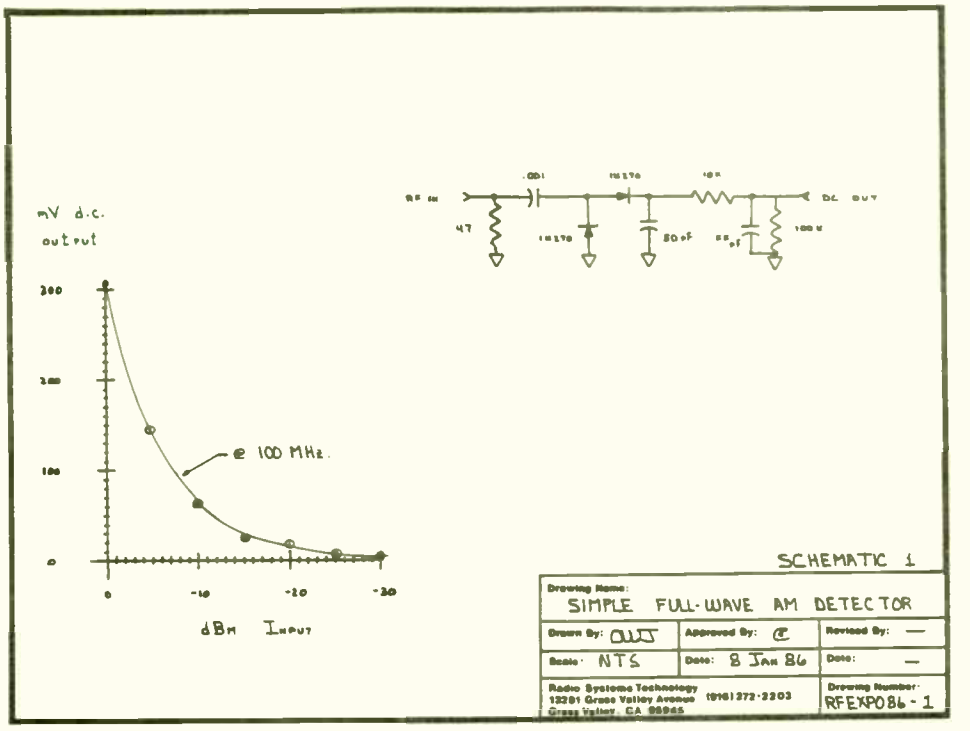
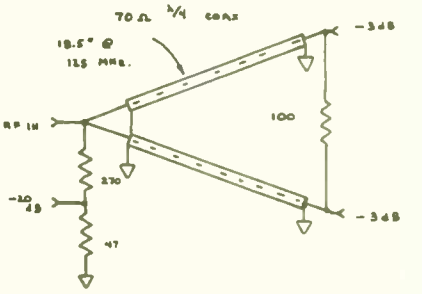


PHOTO 11 The home-brew circuit board of the noise generator. Note that all connections are made as short as possible, and that the scrap circuit board substrate is used to keep ground leads as short as possible.



SCHEMATIC 1

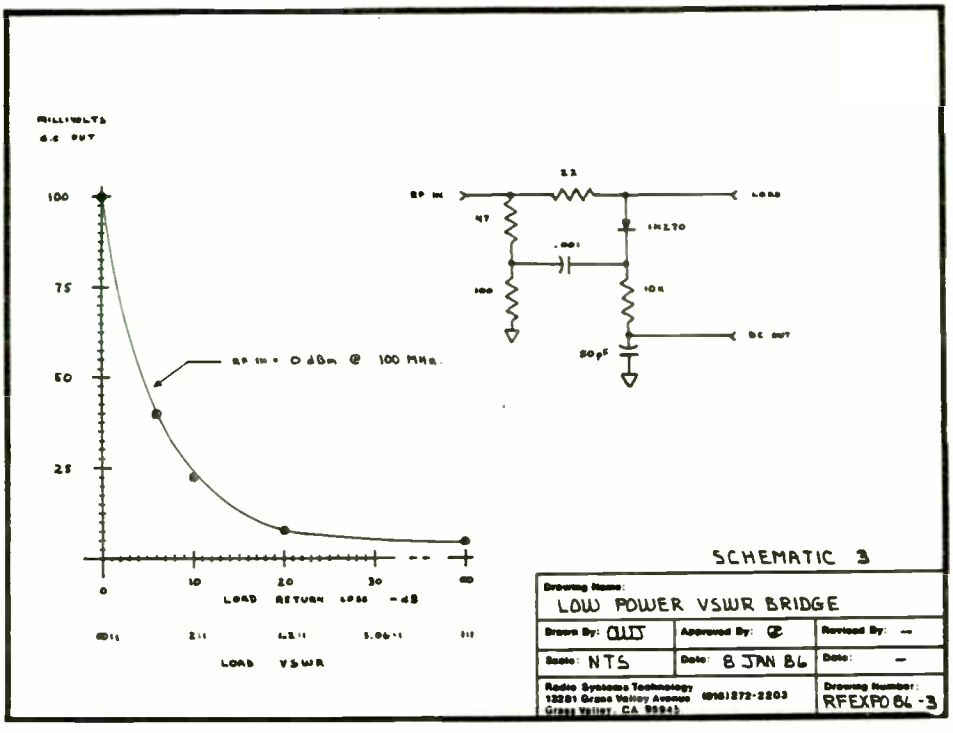
Drawing Name: SIMPLE FULL-WAVE AM DETECTOR		
Drawn By: CWJ	Approved By: @	Revised By: —
Scale: NTS	Date: 8 Jan 86	Date: —
Radio Systems Technology 13281 Grass Valley Avenue (916) 272-2303 Grass Valley, CA 95945		Drawing Number: RFEXPO86-1

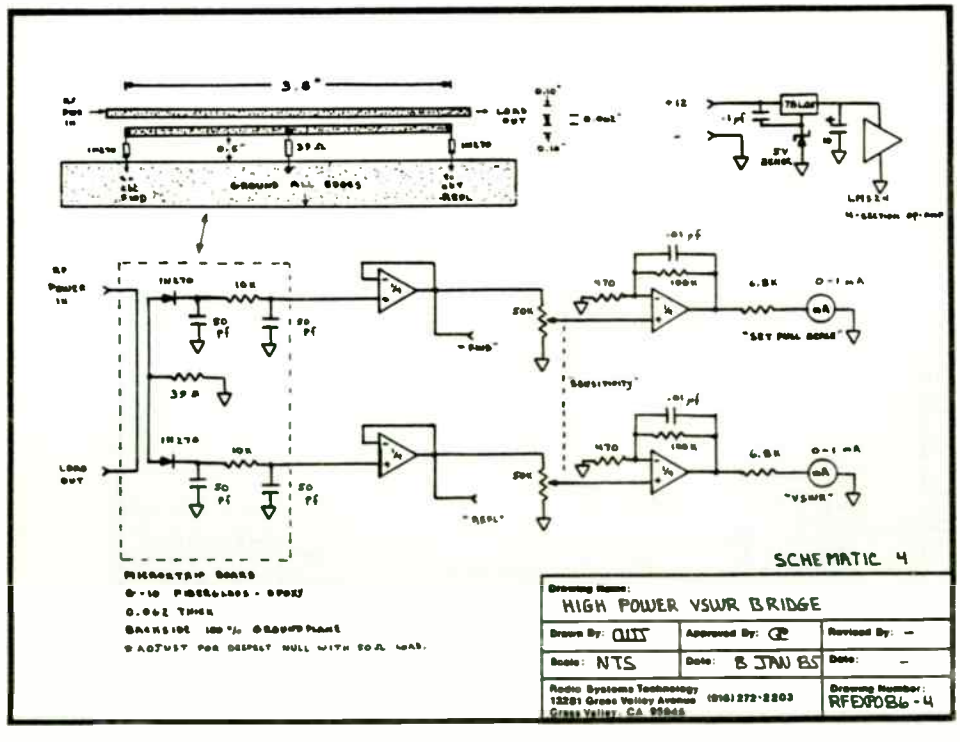


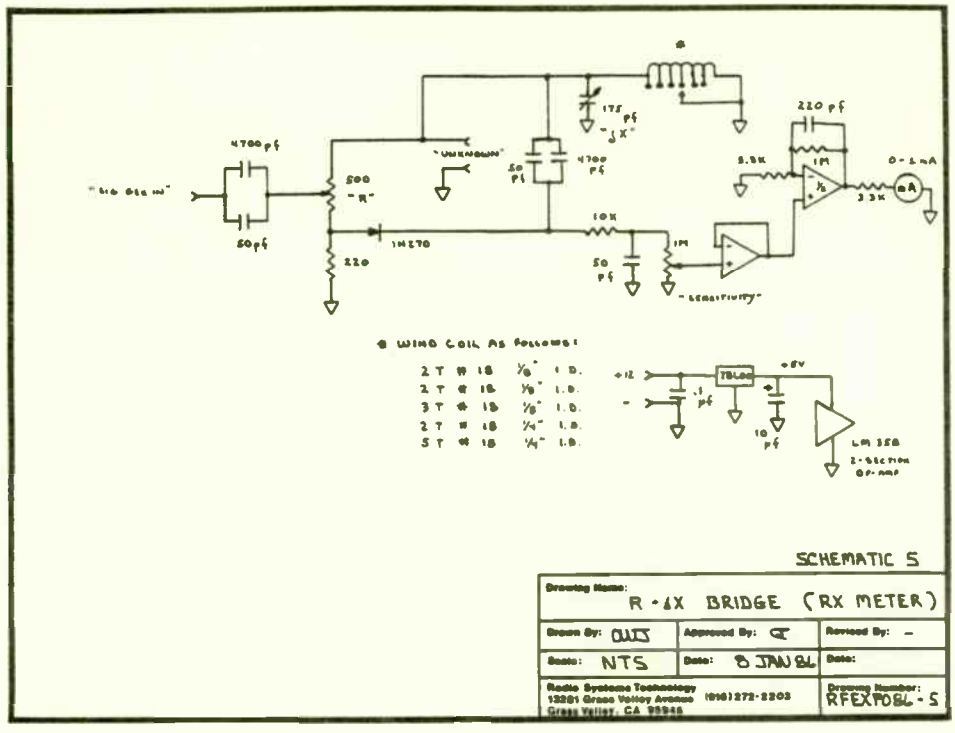
FREQ MHz.	INPUT VSWR	COUPLING @ -3dB	COUPLING @ -10dB
50	1.7:1	4.0	22
100	1.3	3.8	22
150	1.3	3.8	23
200	1.9	4.2	22
250	3.0	4.4	22
125	1.05	3.5	22

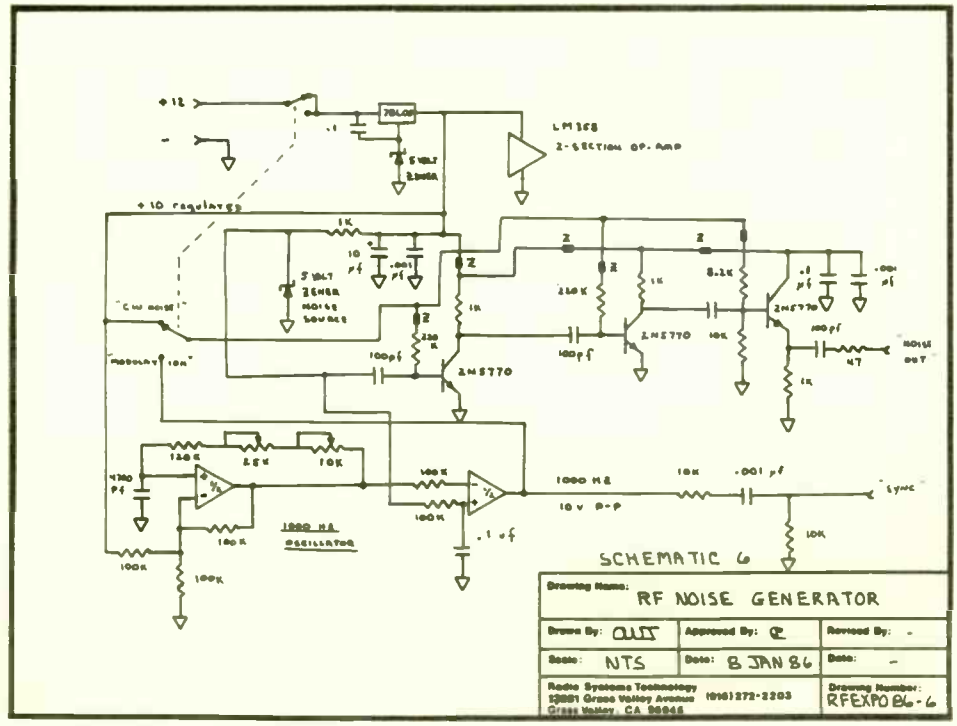
SCHEMATIC 2

Drawing Name: HYBRID POWER SPLITTER		
Drawn By: CWJ	Approved By: @	Revised By: -
Scale: NTS	Date: 8 Jan 86	Date: -
Radio Systems Technology 13281 Grass Valley Avenue (916) 272-2303 Grass Valley, CA 95945		Drawing Number: RFEXPO86-2









DISTRIBUTED 2-20 GHz MONOLITHIC GaAs FET AMPLIFIER DESIGN

by
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Introduction

Distributed or traveling-wave amplifier designs have come into new light with the advent of MMIC technology [1] [2] [3] [4]. The topology of a distributed amplifier, employing several active devices linked in a ladder structure, is practical and desirable to implement with FETs in GaAs MMIC technology. When properly designed, the distributed amplifier will have a gain-bandwidth product which exceeds the gain-bandwidth product of the individual FET devices. Considering also that the coupling structure required to tie several FET devices together is broadband, leads to amplifier designs which exceed decade bandwidth. Now with GaAs foundries becoming more popular, MMIC design is within reach of many small companies that formerly could not enter the monolithic arena.

Since tuning is generally limited on MMIC prototypes and the cost and time to build test circuits is high, the ability to accurately design and model the performance of a proposed monolithic design is vital. With highly accurate software now available on personal computers, many small companies can now afford the CAD tools available for circuit design which can greatly speed the design process, drastically reduce the cost of design, and improve circuit performance.

The purpose of this paper is to demonstrate computer-aided design techniques with the design of a monolithic distributed amplifier. Although the amplifier described here has never been built, similar designs are being pursued by several major contractors. Touchstone (TM, EEsof Inc.) is used to perform the circuit analysis and optimization.

Basic Design

The topology of the distributed amplifier (Figure 1) consists of an input (or gate) line, and an output (or drain) line, coupled together by several FET devices.

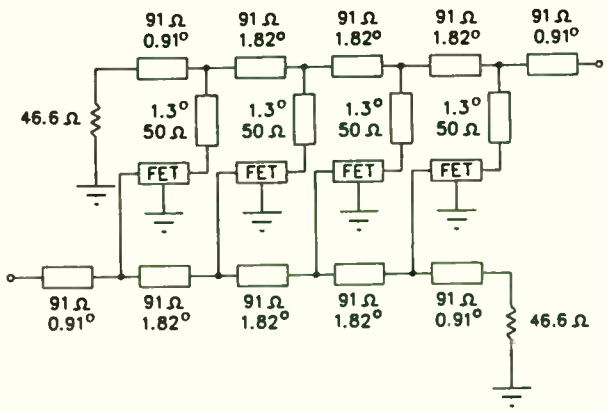

Figure 1. Basic topology of distributed amplifier showing final circuit values for 2 to 20 GHz amplifier

The gate and drain lines form artificial transmission lines, each section loaded by parasitics of a FET device. This is the key to the success of the distributed amplifier. The capacitive parasitics of the FET on both the gate and drain side are absorbed into the low pass structure of the transmission lines. This allows a very broadband match into the FET as long as the cutoff frequency of the low pass line can be made sufficiently high. The lumped inductors which normally form the series elements of the low-pass line are implemented as electrically short microstrip transmission lines. For the distributed amplifier to function correctly, the gate and drain lines must have the same phase velocity. This assurea summing of the signals at the output. Requiring that the gate and drain lines have the same cutoff frequency guarantees this. [2]

The Constant-K Line

The conatant-k transmission line model is chosen as the basis for the gate and drain lines. This lumped ladder filter is composed of several LC sections as shown in Figure 2, and exhibits a constant characteristic impedance along the line. The simplified FET model is shown in Figure 3.

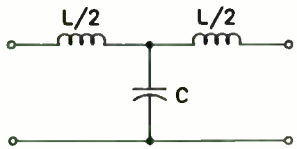

Figure 2. A section of constant-K transmisaion line.

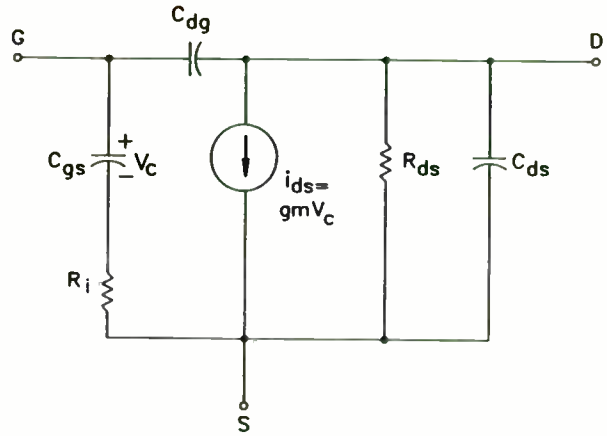

Figure 3. Simplified FET model.

If the model is split into gate and drain sections, each section can be incorporated into the gate and drain lines as the shunt capacitive portion of a transmission line section. The characteristic impedance and cutoff frequency of the constant-k line are given by (1) and (2) for an ideal line.

$$R = \text{SQRT}(L/C) \quad (1)$$

$$Fc = 1 / (\text{PI}*\text{SQRT}(L*C)) \quad (2)$$

The gate and drain lines will be lossy due to associated resistances of the FET. As mentioned before, the cutoff frequencies for the gate and drain lines should be the same, requiring that the LC product for the gate and drai lines be equal.

The FET Device

In designing an amplifier, one of the most important aspects is device characterization. Generally, a test device is developed and S-parameters are measured. These S-parameters can be used directly in the computer design, or a device model can be developed which behaves like the measured device. It can be very useful to predict the performance of a hypothetical device which is modeled by an equivalent circuit linked to the fabrication process. Computer modeling is used effectively for modification of FET design to fit the circuit application. [5] It is a major advantage in MMIC design to be able to tailor active devices to fit the application.

This paper will not explore techniques for modification of the FET design to improve circuit performance except to estimate the effect of changing the gate width of the device. A realistic FET model is shown in Figure 4.

This model is reported to match de-embedded S-parameters for a real 0.5 x 250 micron FET over the 1 to 18 GHz range. [1] Changes in the electrical parameters due to changes in gate width are generally understood and can be estimated by simple equations. The computer model to generate S-parameters for an arbitrary gate width FET is shown in Figure 5. The equation capability of Touchstone (TM) is used to relate the device parameters to the gate width.

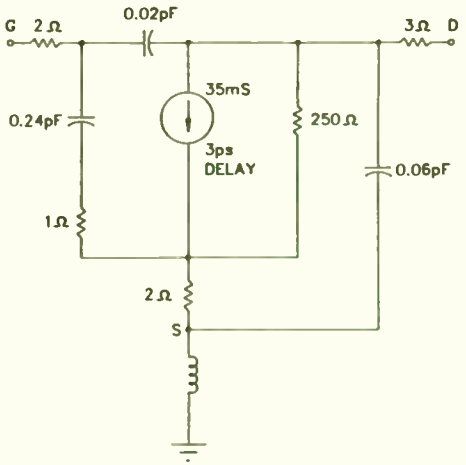

Figure 4. A realistic FET model.

```
! Figure 5:  This file is used to generate single gate and dual gate FET
! parameters for arbitrary gate width FET devices.
! For more information on model, see W. Kennan, N. K. Osbrink, "Distributed
! amplifiers: Their time comes again" Part 2, Microwaves & RF, Dec 1984

    VAR
      GATE = 300                ! gate width of device
    EQN
      GM  = 0.00014 * GATE      ! width dependent device parameters
      Cgs = 0.00096 * GATE
      Ri  =     250 / GATE
      Cdg = 0.00008 * GATE
      Rds =   62500 / GATE
      Rd  =     750 / GATE
      Cds = 0.00024 * GATE
      Cdi = 0.00008 * GATE
    CKT
    ! basic FET model structure
      RES 1 2 R=2
      CAP 2 3 C^Cgs
```

```
  RES 3 4 R^Ri
  RES 4 6 R=2
  CAP 2 5 C^Cdg
  VCCS 2 5 3 4 M^GM A=0 R1=0 R2^Rds F=0 T=3
  DEF3P 1 5 6 FETMOD
! single gate FET model
  FETMOD 1 2 3
  IND 3 0 L=.04
  CAP 2 3 C^Cds
  RES 2 4 R^Rd
  DEF2P 1 4 FET1 FET300   ! name of FET sparameter file
! dual gate FET model
  FETMOD 1 2 3
  IND 3 0 L=.04
  CAP 2 3 C^Cds
  RES 2 4 R^Rd
  FETMOD 3 5 4
  CAP 4 5 C^Cdi
  RES 5 6 R^Rd
  DEF2P 1 6 DFET ! DFET
OUT
  FET1 SPAR
! DFET SPAR
FREQ
  SWEEP 2 24 1
```

Figure 5. Computer model which generates S-parameters for FET device.

The simplified FET model is easily absorbed into the transmission lines, but does not consider feedback capacitance, which is a major contributor to performance degradation at high frequencies. The presumption here is that effective gate and drain capacitances for the realistic model still allow the desired gate and drain line performance. For some devices this may not be ture, and limited bandwidth may be required by the gain-bandwidth limitations of the matching network or to maintain stability of the amplifier. If this is found to be true, an alternative device or design may be required to achieve the desired performance.

One approach to improving the design is to incorporate dual gate FETs, with the second gate electrically grounded at RF frequencies. This combination behaves as a two-stage cascode device, which exhibits lower equivalent gate and drain capacitances, and thus extra bandwidth. [1] The design approach will demonstrate the use of single gate FETs, then dual gate FETs will be substituted to illustrate the improvement.

Observations

Understanding the factors influencing the performance of the design helps knowing what to expect as the circuit is modeled and analyzed. It also uncovers clues to improving the design. A close look at the theory of distributed amplifiers shows relationships involving time constants at the gate and drain of the FET. [2] These relationships indicate that frequency response of the amplifier is heavily influenced not only by the cutoff frequency of the gate and drain lines, but by the attenuation on the gate line. DC gain, on the other hand, is influenced by the Gm of the FET and attenuation on the drain line. There is also a relationship between optimum gate width and optimum number of FET devices used in the amplifier. [2] This could indicate that there is an optimum total gate periphery for a given distributed amplifier.

The characteristics of the constant-k line deserve some thought also. For instance, the image impedance of the line is resistive below cutoff, and reactive above cutoff. Also, it is possible to maintain a constant cutoff frequency by holding the LC product of the line constant. These facts help in understanding how to tune the amplifier.

Forming the Computer Model

The first step in modeling the amplifier is to determine the equivalent shunt capacitance at the gate and drain of the FET for the desired operating conditions. This is easy to determine if the device is unilateral, or nearly so, since the equivalent capacitances can be read from the model directly.

Most FETs are not unilateral because of the drain-gate feedback capacitance, and in fact this usually causes the device to be conditionally stable. The effective gate and drain capacitances for a non-unilateral device are modified by the "Miller" effect, where the feedback capacitance is reflected into the gate and drain circuits for a particulsr load.

When the FET is not unconditionally stable, it is a bit tricky since the equivalent capacitances cannot be determined from the simultaneous match conditions. In fact, the amplifier must be designed so that a deliberate mismatch occurs at the gate and drain in order to ensure stable operation. This limits the desired performance of the distributed amplifier since the equivalent capacitances cannot always be totally absorbed into the gate and drain lines.

A look at the general stability of the 250 micron wide FET indicates some caution is in order. The device is conditionally stable at lower frequencies, but resistive terminations lie in the stable region on both the input and output planes. Using the computer to tune a rough matching circuit helps to visualize how the FET responds to various matching elements. Because of the difficulty in matching to the FET, full decade bandwidth will probably not be possible, at least not with good gain flatness.

The tuning procedure allows a rough estimation of the equivalent capacitances at the gate and drain, 0.275 pF and 0.06 pF respectively. If the goal is a 2 to 20 GHz amplifier, the cutoff frequency of the gate and drain lines must be set higher than that, say to 24 GHz.

To make the design simpler, two additional requirements are made. First, the image impedance of the gate and drain lines will be held near 50 ohms to facilitate a broadband match to a standard load.

Second, the series inductance of the lines is held constant, making all the lumped equivalent transmission lines the same impedance and length. This second restriction requires that the capacitances of the lines also be the same, so shunt capacitors of 0.215 pF must be added to the drains of the FETs. The inductance value of the constant-k line calculates to 0.625 nH. The inductors will actually be implemented as electrically short high impedance transmission lines, say 90 ohms, and the capacitors as electrically short low impedance transmission lines, say 50 ohms. Using the equations for a short and open circuited transmission line impedances, the electrical length of the

equivalent transmission lines is found to be 1.4 degrees at 1 GHz for the 50 ohm lines and 2.5 degrees at 1 GHz for the 90 ohm lines. Linecalc (TM) is used to verify the reliability of the microstrip lines on 4 mil thick GaAs substrate.

The rough design of a complete amplifier can be put together and optimized for the desired performance. Four FETs are arbitrarily included in the circuit. The optimization criteria are chosen to flatten gain to a reasonable value, maintain a match to 50 ohm source and load, and to require gain rolloff and reflection coefficients less than unity above the band of interest. The schematic for the optimized circuit file is shown if Figure 1. The final circuit file description is shown in Figure 6.

```
! Figure 6:  This circuit file models a single gate FET distributed amplifier
! with 4 devices, with device parameters read from file FET250.S2P, 250 micron
      VAR
        L   \ 0.91455       ! length of constant-k half section inductor
        LEN \ 1.30722       ! length of drain capacitor
        ZI  \ 91.05647      ! impedance of constant-k inductance line
        R1  \ 46.59919      ! terminating impedance of constant-k line
      EQN
        L2 = 2 * L
        ZO = ZI
        R2 = R1
      CKT
        TLIN 1 2 Z^ZI E^L F=1
        S2PA 2 12 0 FET250
        TLIN 12 22 Z=50 E^LEN F=1
        TLIN 21 22 Z^ZO E^L F=1
        RES 21 0 R^R2
        TLIN 2 3 Z^ZI E^L2 F=1
        S2PA 3 13 0 FET250
        TLIN 13 23 Z=50 E^LEN F=1
        TLIN 22 23 Z^ZO E^L2 F=1
        TLIN 3 4 Z^ZI E^L2 F=1
        S2PA 4 14 0 FET250
        TLIN 14 24 Z=50 E^LEN F=1
        TLIN 23 24 Z^ZO E^L2 F=1
        TLIN 4 5 Z^ZI E^L2 F=1
        S2PA 5 15 0 FET250
        TLIN 15 25 Z=50 E^LEN F=1
        TLIN 24 25 Z^ZO E^L2 F=1
        TLIN 5 6 Z^ZI E^L F=1
        RES 6 0 R^R1
        TLIN 25 26 Z^ZO E^L F=1
        DEF2P 1 26 AMP
      OUT
        AMP DB[S21] GR1
        AMP DB[S11] GR1A
        AMP DB[S22] GR1A
      FREQ
        SWEEP 2 24 1
      GRID
        GR1 0 10 1
        GR1A -20 0 2
      OPT
      ! in band optimization
        RANGE 2 20
        AMP DB[S11] < -10
        AMP DB[S22] < -10
        AMP DB[S21] = 7
      ! out of band optimization
        RANGE 21 24
        AMP DB[S21] < 7 10
        AMP DB[S11] < 0 10
        AMP DB[S22] < 0 10
```

Figure 6. Final circuit file description.

Plots of the optimized results are shown in Figure 7, and a comparison with 3 and 5 FETs is shown in Figure 8. A comparison with 200 and 300 micron wide FETs shown in Figure 9.

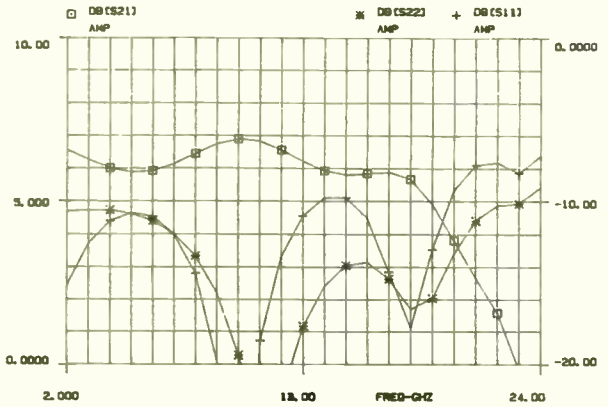

Figure 7. Single gate 2 to 20 GHz, 250 micron design, 4-FET amplifier results

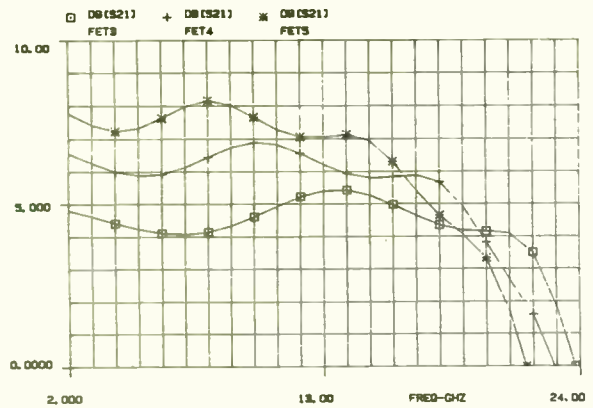

Figure 8. Three-, four-, and five-FET amplifier gain .

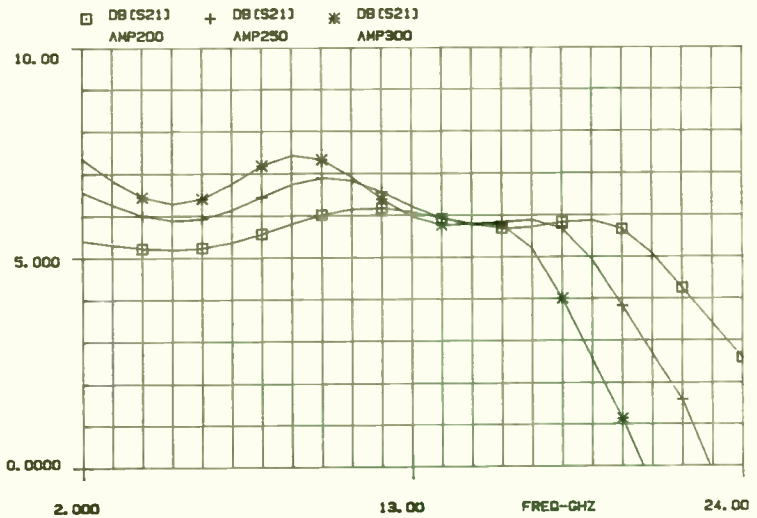

Figure 9. 200, 250, and 300 micron FET amplifier gain.

The overall bandwidth and gain flatness are indeed less than desirable. The total gain is low compared to what would be expected with a narrow band single state design, but this is normal for a distributed amplifier. The narrower bandwidth can be attributed to problems on the gate line. The gain and gain flatness can be attributed to problems on the drain line. There seems to be some tradeoff between improving the gate and drain lines. To achieve more reasonable gain flatness, the bandwidth is reduced to 2 to 14 GHz and the circuit is re-optimized. The results are shown in Figure 10.

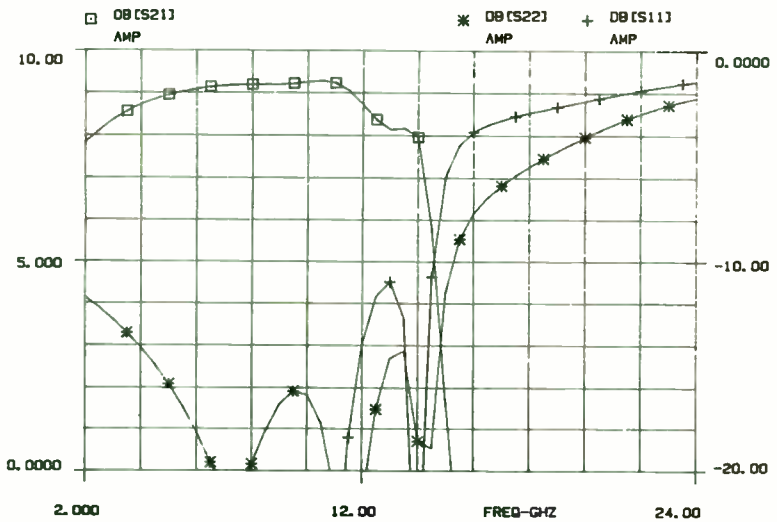

Figure 10. 2 to 14 GHz single gate amplifier results.

In an attempt to improve both the gain and flatness, dual gate FET parameters are used in the design. The dual gate FET also has the advantage of gain control by adjusting the bias voltage on the second gate. The FET parameters are generated from an expansion of the single gate FET model into a two-stage cascode model. The gate width was reduced to 200 microns to make the device more stable. Since the overall gain and bandwidth were much better, the design goals were set to 9 dB gain and 2 to 24 GHz passband. The optimized results are shown in Figure 11.

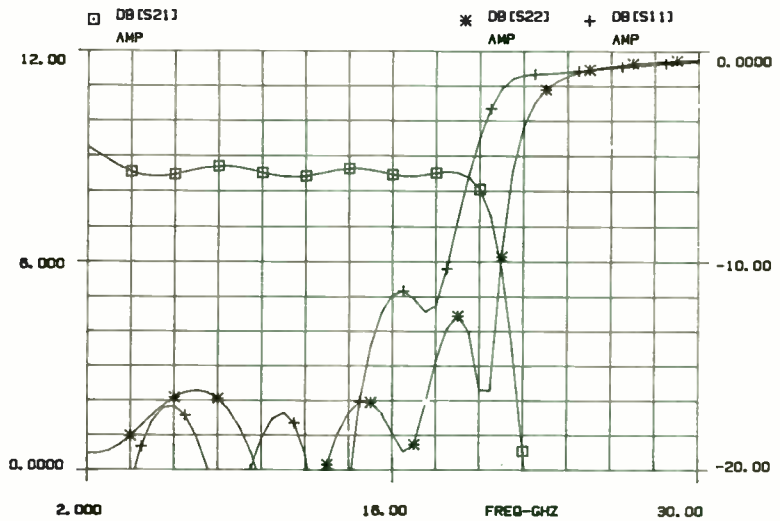

Figure 11. Dual gate amplifier results.

What About Stability

Stability is often a very difficult thing to prove. In order to properly prove stability on the amplifiers designed here, each interface of a FET to the gate and drain lines should be examined to determine the loads that each FET sees looking into the gate and drain lines. These loads can be plotted on the input and output planes for the FET to determine if they lie in stable regions. Looking at the amplifier response, the gain response and reflection coefficients at the input and output seem well-behaved, thus there is not firm reason to expect a near oscillating condition. There would be

cause for worry if there was unusual gain peaking or reflection coefficients greater than 1 at the input or output.

Conclusion

A glimpse has been given into how an engineer can use computer tools to increase the speed of design and quality of circuitry. The techniques shown are applicable to state-of-the-art amplifier designs -- a mere taste of what the powerful tools available in computer-aided design can do for you.

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