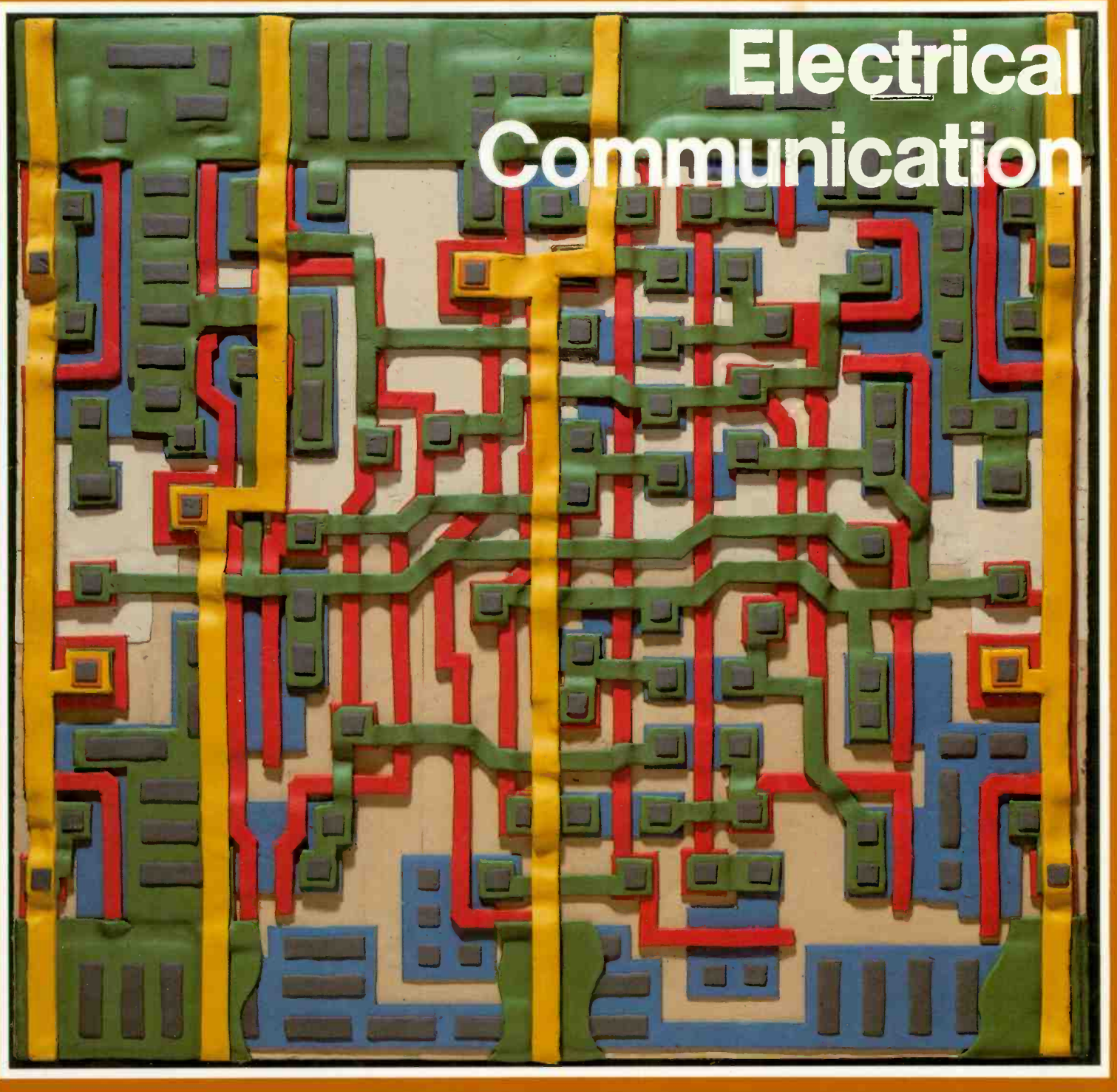

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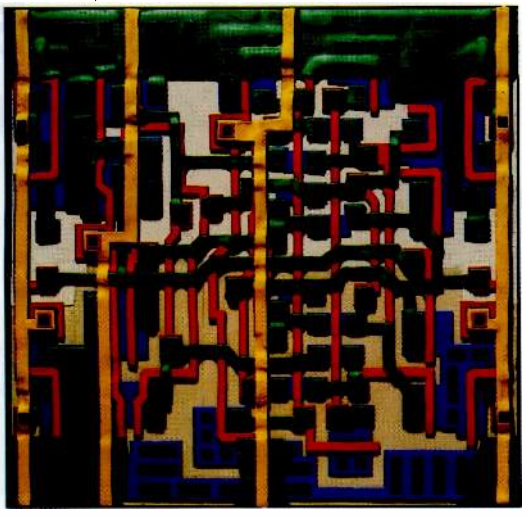
VLSI Technology

ITT



The model shown on the front cover depicts a VLSI T-type bistable implemented in 3 µm CMOS technology. This bistable, which measures less than one-fifth of a millimeter across, forms part of a standard cell library from which a variety of complex digital integrated circuits can be constructed. The various layers of modeling clay have the following color coding:

White	*n*-type silicon substrate
Stone	*p*-well
Blue	active diffusion areas in the substrate
Red	polysilicon
Green	first metal layer
Yellow	second metal layer
Orange	via connection
Grey	contact area (beneath the metallization)

Overview

VLSI (very large scale integration) is not only a revolution in semiconductor technology. It has also brought about a revolution in the design methods and architectures applied to electronic systems. VLSI is causing us to rethink the bounds of system design, and to search for more effective ways in which to use the technology in developing advanced products and services. For example, the fully distributed control architecture of ITT's System 12 Digital Exchange only became technologically and economically feasible through the implementation of VLSI. At the other end of the communication network, VLSI made possible the important transition of telephone subsets from electromechanical to electronic circuitry, and from analog to digital information format.

Another aspect of this revolution is computer-aided design, which enables us to manage the complexities of designing and laying out VLSI chips. In the days of transistors and relatively simple integrated circuits, the chip designer and the system designer lived in separate worlds. Each optimized his or her own activity as each advanced the frontiers of the respective discipline. The primary design aid was the slide rule; computer programs were barely a gleam in the eyes of a few visionaries.

During the past 20 to 25 years, these two disciplines have been forced to converge, primarily because of the exponential growth of the number of transistors that can be defined on a chip (more than a million in the laboratory). As chip complexity has increased, the trend has been to provide more system-level functionality in silicon. Thus the ITT Digit 2000* chip set represents a VLSI system that contains a sophisticated microcomputer, digital filters, and high performance amplifiers.

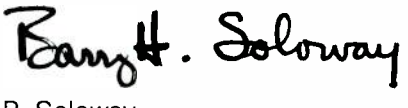
This convergence has affected the role of the chip designer and the system designer. Both have had to gain competency in logic design. In addition, the chip designer has had to master a basic understanding of systems; and the system designer now deals with both software and hardware, including semiconductor technology. But convergence has been inhibited by the very broad scope of the disciplines, ranging from atomic structures at one extreme to global telecommunication at the other. Computer-aided design is providing a solution, emerging as the language that enables the chip designer and the system designer to communicate successfully, and to work together to develop advanced products. Their primary design aid is the computer, together with a rich assortment of computer-aided design tools and a common symbology.

* A trademark of ITT System

It is therefore appropriate that this special issue on VLSI opens with a perspective on computer-aided design – the tools, libraries, and design environments that make it possible to turn system specifications into logic diagrams, and ultimately into silicon chips. We next explore the challenges facing the technologists in their quest for the one micron goal. What will we do with one micron technology and one million transistors? The answer is, conceive and design advanced architectures capable of providing the substantially improved computing power that will be required for speech, image, and knowledge base processing.

VLSI is not limited to silicon. Gallium arsenide is a semiconductor substrate material on which to define integrated circuits with higher performance and lower power consumption than those based on silicon, especially for frequencies well above one gigahertz. It also provides the means to combine optical lasers and detectors on the same chip as electronic components. This offers new degrees of freedom to system designers as the field of opto-electronics marks the latest phase in the evolution of integrated circuits.

The articles in this issue provide a cross section of VLSI activity within ITT. They also demonstrate ITT's commitment to advancing VLSI technology and using it effectively in current and future generations of equipment and systems.



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Impact of Custom VLSI Technology

The semiconductor industry forecasts that 50% of the integrated circuits used in 1990 will be application specific custom and semi-custom design circuits. ITT's broad product base makes it essential for the corporation to have state-of-the-art design and processing facilities for this key technology.

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P. Van Iseghem
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Introduction

Very large scale integration (VLSI) is considered by ITT to be one of the key technologies[1] which will have a growing impact on many product lines. New systems, like the System 12 Digital Exchange, have been developed around VLSI technology. The advanced performance of the System 12 distributed control architecture could only be realized cost-effectively by using custom designed VLSI circuits and standard microprocessors.

ITT's broad range of products and services makes it essential for the corporation to process state-of-the-art VLSI design and manufacturing facilities that can serve affiliated companies worldwide. To achieve this, the corporation has set up 14 design centers which together combine expertise in a wide range of processing technologies, enabling ITT units to use the most suitable and advanced technologies in their products. Both semi-custom and full custom design facilities are available. Silicon is the basis for most of these VLSI technologies, but ITT is also well advanced in the application of gallium arsenide circuits and has built a modern processing facility in the United States.

ITT units have developed a wide range of VLSI devices, including those for the System 12 switchport and line circuit, an echo canceler for digital local loop transmission, and a family of devices for a new digital television receiver.

It is important that the system design should be VLSI-oriented, that is, make full use of VLSI technology. Increased levels of integration are making it possible to use new architectures and algorithms.

Clearly the move towards improved architectures and smaller feature size is increasing the complexity of the task for the VLSI designer, who is also becoming involved in new aspects of the design. Within ITT, the VLSI designer is being equipped with powerful simulation tools and interactive graphics systems that perform much of the routine design work and verify it automatically, freeing the designer to concentrate on more creative design work.

Trends in Electronic Equipment

The trends in microelectronics affecting equipment design are by now well established. The current position is that integrated circuits have virtually taken over from discrete transistors, and that digital processes are rapidly supplanting the analog techniques which have been predominant up to now. The aim is to move from systems on printed boards to systems on single VLSI chips. Where production volumes are sufficient to warrant the design costs, standard integrated circuits are being replaced by application specific custom designs which make optimum use of VLSI technology. As full custom design is expensive, in many areas semi-custom design using predefined gate arrays or standard cells is taking over. Advances in this area will make semi-custom designs equal in performance to present full-custom designs.

Equipment Content

Over the past ten years, the integrated circuit content of ITT equipment has risen rapidly, and will rise even more dramatically by 1990. This illustrates the move away from mechanical parts to electronic components and then to integrated circuits. Figure 1 shows that transmission led in the application of integrated circuits and that switching followed. The first ITT design center for custom VLSI was started as part of the transmission division of STL (Standard Telecommunication Laboratories) in England in 1969. By 1976 additional VLSI design centers had been built up at the ATC (Advanced Technology Center) in the United States, BTM (Bell Telephone Manufacturing Company) in Belgium, and Deutsche ITT Industries in Germany. By 1984, design centers had also been established at SEL (Standard Elektrik Lorenz), STK (Standard Telefon og Kabelfabrik), SESA (Standard Eléctrica), FACE, ITT Network Systems Division, and ITT Aerospace.

Analog and Digital Circuits

Analog integrated circuits have benefited from advances in semiconductor processes and circuit design. Low noise, high gain processing combined with increasingly sophisticated design skills have resulted in cost-effective chips with the high dynamic range necessary for telephone transmission networks, radio receivers, and pulse code modulation repeaters (where some 40 to 90 dB of wideband gain is needed).

In many cases an analog implementation is the best or the only feasible solution, and analog skills will make steady progress yielding increased bandwidths, higher frequencies, and improved reliability. Bipolar technology has traditionally been used for analog circuits, but MOS technology is beginning to take over at the low frequency end where modest noise figures and gains are acceptable. Gallium arsenide is extending the frequency range of microwave amplification.

The ingenuity of the MOS circuit designer allows full integration of filters and amplifiers (usually switched capacitor filters) and the inclusion of analog and digital functions on one chip. The result is a higher degree of integration on each chip and partitioning in a way that is appropriate to the system and not forced on the designer by the limitations of the technology.

ITT is at the forefront of so-called mixed technologies, integrating bipolar and CMOS circuits as well as high voltage MOS and CMOS. These mixed technologies offer advanced solutions for interface chips.

However, in spite of analog advances the trend to digital systems is inexorable. In exchange for increased complexity, the digital approach offers increased reproducibility (less need for functional testing), better controllability (performance can be set by the software), and extra features (storage of information). It also allows new approaches (architectures) that are not feasible in analog designs. For example, radio receivers with digital synthesizers offer drift-free tuning and can use spread spectrum techniques to improve transmission security.

Custom Design

Standard integrated circuits can perform many of the tasks required in a system, but in many cases the best performance-to-cost ratio (e.g. highest throughput with low power and low unit cost) is achieved with a custom design circuit. Indeed, in certain cases the need to achieve maximum performance makes it essential to use custom circuits. The trend towards custom design is recognized by the semiconductor vendors who now predict that custom VLSI, which it calls ASICs (application specific integrated circuits), will grow to become 50% of all integrated circuit sales by 1990.

Economic development and production of these components is only possible with a high technological capability. ITT recognized this early on and has built up a competitive position in design methodologies, computer-aided design tools, process technology, and testing. The corporation also recognized that VLSI design capability must be made available at design centers close to the system

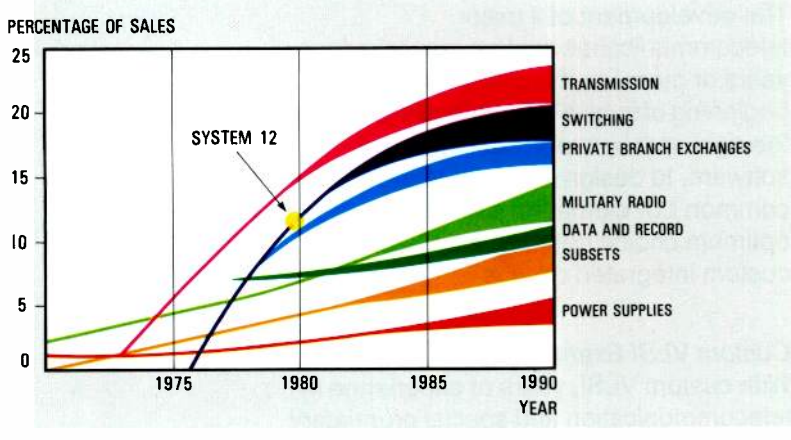

Figure 1
Impact of integrated circuit technology on various application areas.

development centers, to ensure that ITT products can take advantage of these techniques. This need and the knowledge that specialized products may have low production volumes have led to an emphasis on semi-custom design for the smaller design centers.

System Requirements

Users of ITT equipment require effective and economic solutions to their needs for network and end user products – on the world's telephone network, in the office, at home, in the factory, or in defense. VLSI technology offers increased performance and flexibility. In return modern systems make stringent demands on VLSI technology, as illustrated by the following examples.

The interfaces between equipment and the outside world are usually hostile to integrated circuit technology; motor controls, bright displays, and even telephone lines (which could contact a power line) all require high voltage technology. A satellite transceiver needs a microwave amplifier capable of withstanding nuclear radiation.

At the heart of a system and protected from the environment may be special processors for reformatting data, recognizing speech, controlling television pictures, or interpreting radar signals. Fast logic is required: a ground radar needs billions of operations per second, and high speed is more important than low power consumption; a digital television set may perform several million operations per second and low cost is paramount; a speech recognition system has similar needs to the television but may emphasize low power requirements.

ITT thus requires a broad range of technologies: gallium arsenide, silicon (bipolar and MOS), and high voltage.

VLSI-Oriented System Design

A VLSI-oriented design is one with a system architecture that makes full use of the capabilities of VLSI technology. As an example, great improvements have been made in information signal processing throughput by combining new system concepts (architectures and algorithms) with the latest VLSI technology[2].

The evolution and availability of the technologies must be carefully evaluated in order to synchronize with system design.

Table 1 – Analog and analog/digital VLSI designs

Device	Production volumes	Power available	Technology (Table 3)	Design method
Subscriber line circuit interface	high	low	G, H	FC
Subset transmission network	high	very low	E	FC
2 Mbit s^{-1} PCM repeater (copper/optical)	medium	medium	E	FC
560 Mbit s^{-1} PCM repeater	low	high	F	FC
Subscriber line circuit	high	low	A, I	FC

Table 2 – Digital VLSI designs

Device	Production volumes	Power available	Technology (Table 3)	Design method
1. Digital switching matrix (switchport)	high	low	A	FC
2. Digital subscriber loop (ISDN)	low	low	B	FC
3. Digital television	high	medium	C, D	FC
4. Speech recognition processor	high	medium	B	FC
5. Digital speech codec	high	low	B	FC
6. FDM-PCM transmultiplexer	medium	medium	B	FC
7. PCM channel bank data port	low	medium	B	SSC
8. PCM multiplexer (times 4 up to 34 Mbit s^{-1})	low	medium	E	SGA
9. Digital trunk	medium	medium	A, B	FC
10. Military radio (14 designs)	low	low	B	SGA
11. Video switch matrix	low	medium	J	FC

FC - full custom
SSC - semi-custom standard cell
SGA - semi-custom gate array

Table 3 – Semiconductor technologies

A	NMOS, low power, medium speed (4 MHz)
B	CMOS, very low power, medium speed (4 MHz)
C	Bipolar, high speed, low cost
D	NMOS, low power, high speed (17 MHz)
E	Bipolar, low noise, medium speed
F	Gallium arsenide (or bipolar wideband analog)
G	Integrated high voltage MOS/low voltage CMOS
H	Combined bipolar and CMOS, medium voltage
I	CMOS, combined analog and digital (double polysilicon)
J	CMOS, high speed

The development of a major telecommunication system may take four years or more, so it is crucial at the beginning of such a development to choose the right split between hardware and software, to design for multiple use of common LSI elements, and to make the optimum choice between standard and custom integrated circuits.

Custom VLSI Examples

With custom VLSI, years of experience in telecommunication and special proprietary

features are "etched in silicon"[3]. An excellent example is the switchport of System 12 which performs both time and space switching, has its own path memory, and contains enough intelligence to perform its own path search. The switching matrix can grow without affecting line traffic simply by adding more switchports. Another System 12 example is the line circuit, which uses analog and digital custom VLSIs with software selectable transmission and signaling parameters.

In end-user products, such as telephone subsets, volumes are high, special knowledge of administration practices is needed, and the available power is limited. ITT has used bipolar technology to design cost-effective high performance analog transmission networks that provide the electronic telephone with a speech quality superior to a carbon microphone unit. Features such as autodialing are added to the basic electronic phone by custom VLSI circuits.

Signal processing is an area of virtually insatiable demands on VLSI technology. Speech recognition and nonswitched handsfree telephony (involving fast adaption echo cancelation) require state-of-the-art VLSI technology combined with special architectures.

As an example, BTM has developed a unique cost-effective full custom approach to provide digital local loop transmission (subset to exchange) where an echo canceler is required for 4-wire operation on a subscriber pair[4]. This canceler performs many operations per second using a systolic architecture (executing a fixed set of instructions as data flows through the system).

In the area of consumer products, Deutsche ITT Industries has developed Digivision* – a digital television using a family of full custom VLSI chips resulting in a clear flickerfree picture, automatic adjustment, simplified maintenance, and special features such as a split screen. The 5-chip set consists of full custom designed VLSIs using both NMOS and bipolar technologies.

Telephone line interfaces and displays use voltages above the normal limits of semiconductor operation. ITT has paid special attention to silicon solid state devices for switching voltages of up to 200 and 400 V and has succeeded in the integration of an intelligent switch which combines 400 V switches fully-isolated from 5 V control logic[5].

The special needs of defense initially motivated a major research programme in gallium arsenide technology, with analog and digital designs being fabricated in a dedicated facility[6] in the United States as well as at STL[7]. Recently there has been great interest in gallium arsenide technology for satellite and portable communication (e.g. radio pagers).

Table 1 lists five analog circuits that are required in subsets, pulse code modulation repeaters (regenerators), and subscriber line circuits for public switching. The line circuits use two technologies as voltages are mixed or analog and digital functions are combined. All need full custom design and a total of six different technologies are used. Table 2 shows purely digital functions, some of which are semi-custom designs. Again six technologies are employed. Details of the technologies are given in Table 3. The main advantages of full custom design are outlined in Table 4.

Table 4 – Main advantages of custom VLSI

Improved overall performance
More cost-effective design and manufacture
Provision of extra features
Lower power dissipation
Increased reliability
Reduced size
Feasibility of introducing novel architectures

Design Process

VLSI design, like system design, is an exercise in the management of complexity. The link between the systems designer and the VLSI designer must be strong so that the flow from system requirements to the final product, including its VLSI chips, is smooth yet contains sufficient verification (or feedback) points. A system may contain hardware, software, microcode (firmware), user interface, documentation, and training. It results from an analysis of customer requirements, testing (animation or simulation), cost/performance tradeoffs, and tradeoffs between implementation methods, schedule, and so on.

Consider the future system design scenario[8] illustrated in Figure 2. Animation is the means of showing the customer a performance model. It is a high level simulation of test cases to check that the

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formal specification of performance is what the customer needs. As such it provides early feedback to the designer.

The next major feedback point is the verification that the detailed design is correct by checking that it meets the formal specification and can be resimulated. There will often be a series of such steps as major blocks are designed in detail and substituted one for one for their top level models. Simulation using partial models is called "mixed-mode" simulation.

VLSI design follows a similar path for both full custom[9] and semi-custom[10] design.

The work to be done in integrated circuit development falls into the following main categories: logic design, layout, fabrication, packaging, and testing. The design team must be supported by semiconductor technology evaluation, economic tradeoff data, computer-aided design tools (in particular simulation, verification, and layout), and test program development tools. Testability must be taken into account during the design process, as discussed elsewhere in this issue[11,12].

Logic design is the largest part of the process and must be done by engineers cognizant with the features offered by VLSI. Some possibilities are: logic design using structures unique to MOS technology, such as transmission and compound gates (which are unavailable in standard medium scale integration logic), and content addressable memory which offers a replacement for the time consuming design and wasted space of random logic. The latter is an example of structured design[13]. Layout is the next largest design component, and must at all times conform to a detailed set of design rules which are compatible with the semiconductor process to be used. The physical layout introduces extra parameters (parasitics) that modify performance and must be included in the final simulation.

VLSI Development/Product Cost Tradeoff

Where large numbers of a circuit will be manufactured, product cost and chip size must be minimized. The best results are obtained by full custom design tailored to the semiconductor technology. For modest volumes and performance, semi-custom techniques cut development costs by reducing the design time. Figure 3 illustrates the tradeoff between custom and semi-custom design.

The crossover between the optimum areas for custom and semi-custom depends largely on the design skills, maturity of the computer-aided design tools, and processing technology. A semi-custom approach is suited to new product start up or for custom adaptations with many similar customers. It can evolve by "custom conversion" to a cost-effective, full custom design.

Evolution of VLSI Design Methods

ITT's capability, as of 1980, for the custom design of the System 12 Digital Exchange was described previously in *Electrical Communication*[14]. Logic simulation and circuit simulation were done on a general purpose engineering computer and layout done using a dedicated interactive graphics system. The interactive graphics system was the largest capital investment and mainly benefited the layout specialists at the so-called "backend" of the design process. Over the past three years, layout productivity has improved by a factor of about 2.5 as measured in transistors per day.

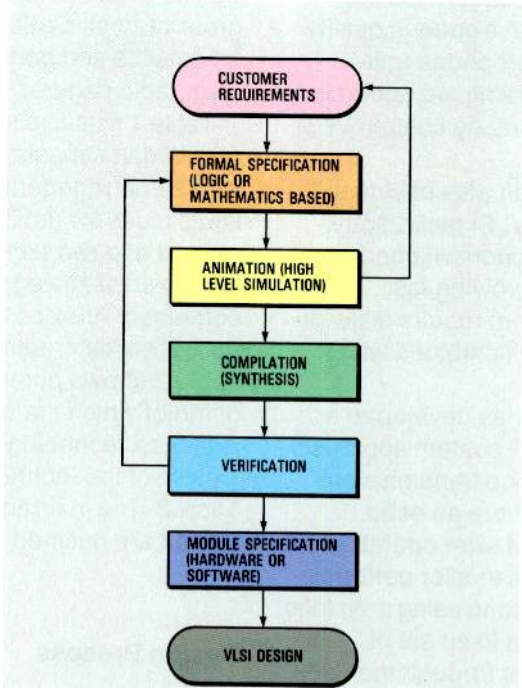
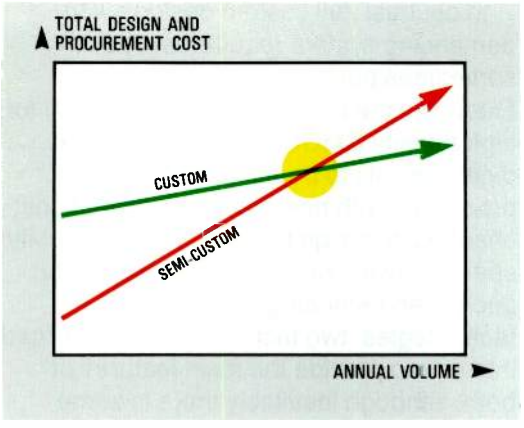


Figure 2
Computer-aided system design.

Since then, progress has been substantial in four main areas. First is the growing emphasis on semi-custom design based on libraries of gate array macros, standard cells, and large logic building blocks. Second is the increased use of automatic error-free design by symbolic layout (removing the details of technology), by structured design concepts (replacing

random logic), and by compilation (direct conversion of functional descriptions to layout). Third is the use of powerful simulators and verifiers to eliminate breadboards. Fourth, is the increased support to the design engineer who now has at his disposal a powerful engineering workstation that automatically performs many routine tasks, freeing the engineer to concentrate on the more creative side of circuit design. In other words we are moving from computer-aided design to computer-aided engineering.



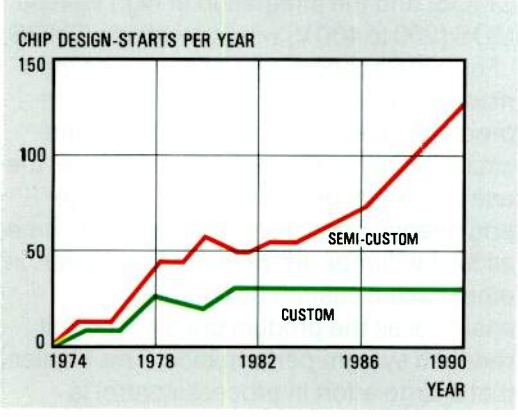


Figure 3
Design tradeoffs between custom and semi-custom VLSI devices. Top: cost as a function of production volume, and bottom: number of design starts since 1974, projected until 1990.

The ITT Environment

ITT has set up 14 VLSI design centers throughout the corporation, ranging in size from three to 50 trained staff. Deutsche ITT Industries, SEL, STL, ATC, and BTM all have facilities for complex full custom designs. Semi-custom design is performed at these and other centers of system development. Larger ITT units have started to set up satellite design centers which share facilities with and have expert assistance from a major center. The number of design starts in ITT is expected to double before 1990, so further changes can be expected.

Figure 4 illustrates the spectrum of complexities and speeds of the digital designs of Table 2 and shows one "corner" of the spectrum which can be handled by semi-custom design. Because semi-custom design results in larger chips and interconnect delays are significant, such designs are slower than full custom designs.

At the Gallium Arsenide Technology Center in Roanoke, special skills exist in microwave amplifier design; this center also cooperates with ATC on fast logic circuit design. STL has fabricated both analog and digital circuits in gallium arsenide technology.

With the variety of local design needs and local equipment (computers and graphical systems) it is a challenge to provide a flexible corporate computer-aided design system. ITT chose to write all software in a portable form and to couple both purchased and in-house computer-aided design tools using neutral data files[15].

Process Technology

As already described, ITT's system requirements make it necessary to exploit many different process technologies. Low and high voltage bipolar technology, NMOS and CMOS with high density or high speed or low power requirements, mixed technologies integrating bipolar and CMOS, high voltage MOS with low voltage CMOS, and analog and digital gallium arsenide are all being used in one application or another.

Ideally, the technologies used should be mature and highly characterized. This situation prevails in semi-custom design. Indeed it is essential for these low to medium volume products (Figure 2). Using the standard cell design approach, full characterization of the cell library helps shorten the learning curve and increase the production yield.

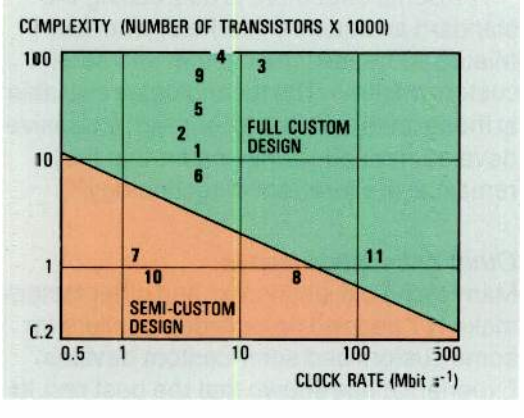


Figure 4
Spectrum of digital custom designs produced by ITT units. Numbers refer to the VLSI devices listed in Table 2.

In contrast, full custom designs with demanding system requirements do sometimes push the state-of-the-art. Examples are the higher voltages (10 V) for high density CMOS to allow analog and digital circuits to be combined; bipolar processes with new voltage optimizations; changes in design rules to improve density, speed, power consumption, or reliability; and mixed technologies. In mixed technologies, two technologies are merged into one to provide the main features of both, although inevitably there is some compromise. Typical are the integration of medium voltage bipolar (up to 70 V) with CMOS, and the integration of high voltage MOS (200 to 400 V) with low voltage CMOS.

From the economic point of view of the manufacturer, custom and semi-custom products differ from standard integrated circuits in many respects. For example, the use of custom designs requires a larger engineering effort per unit business volume as total volumes are usually much lower. In other cases, custom design may be essential as the product does not permit reduced system performance. This implies that a large effort in process control is mandatory, and that the design should reach a high level of manufacturability (tolerance to process variations).

ITT Fabrication Capabilities

One way to secure the supply of VLSI products is to manufacture them in-house. This is accomplished in ITT by ITT Semiconductors with production centers in Germany and the United States, through Mietec in Belgium, and the Gallium Arsenide Technology Center in the United States. The know-how and capabilities resulting from their development and production skills enable ITT to exploit VLSI technology. However, in view of ITT's broad product range, it would be impossible to provide all the necessary processes in-house.

ITT Semiconductors is addressing the standard and custom markets, whereas Mietec addresses the custom and semi-custom markets. The technologies available at these units are state-of-the-art; extensive development effort will ensure that they remain at the forefront of technology[16].

Other Fabrication Needs

Many technical, economic, and other factors make ITT depend on outside suppliers for some custom and semi-custom devices. Experience has shown that the best results are obtained if there is positive cooperation between ITT and the VLSI vendor. Various programmes have been set up to survey, analyze, and study the advanced process technologies used by ITT vendors even at the preproduction stages.

Development of Process Technology

Most research and development is carried out in support of the in-house production capabilities, and to ensure that future evolution will keep them at the forefront of both silicon and gallium arsenide processing technologies. More fundamental work is done at laboratories in Europe and the United States, including studies of the major issues dealing with 1 μm technology[17], reliability issues related to high voltage, highest density, and alpha particles, and a study of isolation techniques[18].

Conclusions

VLSI is a key enabling technology in the provision of new systems, network systems and end user products, features and services. It enables novel system architectures to be used and allows complex functions to be realized cost-effectively.

ITT is increasing the number of unit VLSI design centers and providing them with advanced computer-aided design and engineering support. The corporation is working on a broad range of mainstream and "niche" semiconductor technologies with fast turnaround for masks and engineering samples. As a result ITT is able to exploit VLSI technology, and to improve system architectures, design productivity, and semiconductor processes for the benefit of the many users of its products.

References

1 C. M. Herzfeld: Key Technology Steering Group Forecasts: An Introduction: *Electrical Communication,* 1983, volume 58, no 1, pp 88–92.
2 B. H. Soloway: Key Technology Steering Group Forecasts: VLSI: the Challenge of One Million Transistors: *Electrical Communication,* 1983, volume 58, no 1, pp 109–111.
3 I. A. Cermak: ITT Technology for Telecommunication: *Electrical Communication,* 1983, volume 58, no 1, pp 4–10.
4 R. Diercks, P. Guebels, and P. Six: VLSI for the ISDN Line Termination: *Electrical Communication,* 1984, volume 58, no 4, pp 411–417 (this issue).
5 W. De Kinder: Research for Future Products: High Technology: the Key to Growth: *Electrical Communication,* 1983, volume 58, no 1, pp 124–126.

6 D. G. Fisher: Status and Prospects for Gallium Arsenide Technology: *Electrical Communication,* 1984, volume 58, no 4, pp 418–426 (this issue).
7 A. J. McKnight, J. Mun, and I. A. W. Vance: Wideband Programmable Transversal Filter: *Electrical Communication,* 1984, volume 58, no 4, pp 423–426 (this issue).
8 R. L. Wexelblat: Key Technology Steering Group Forecasts: Designing the Systems of Tomorrow: *Electrical Communication,* 1983, volume 58, no 1, pp 93–97.
9 J. Danneels and M. Meinck: Methodologies for Full Custom VLSI Design: *Electrical Communication,* 1984, volume 58, no 4, pp 389–397 (this issue).
10 A. D. Close, L. Fisher, R. M. McDermott, T. A. Nix, D. M. Perrine, and J. M. Schoen: Design System for Semi-Custom VLSI Circuits: *Electrical Communication,* 1984, volume 58, no 4, pp 372–379 (this issue).
11 G. W. Jacob: Designing for Testability: *Electrical Communication* 1984, volume 58, no 4, pp 427–432 (this issue).
12 R. M. McDermott: ITT's Testability Analysis Program: *Electrical Communication,* 1984, volume 58, no 4, pp 433–439 (this issue).
13 Mead and Conway: An Introduction to VLSI Systems: Addison-Wesley.
14 J. Cornu and M. Meinck: ITT 1240 Digital Exchange: Advanced Component Technology: *Electrical Communication,* 1981, volume 56, no 2/3, pp 161–172.
15 K. R. Bennett and G. J. Lovitt: Data Modeling: the Key to Design System Integration: *Electrical Communication,* 1984, volume 58, no 4, pp 380–383 (this issue).
16 D. Beernaert: Experience in 3-micron Processing: a 10 Volt *n*-well CMOS Process: *Electrical Communication,* 1984, volume 58, no 4, pp 398–404 (this isuue).
17 F. Mohammadi: VLSI 1-micron MOS Processing: *Electrical Communication,* 1984, volume 58, no 4, pp 405–410 (this issue).
18 D. Beernaert, G. Schols, and P. Van Iseghem: Isolation Techniques for Very Large Scale Integration: *Electrical Communication,* 1982, volume 57, no 2, pp 161–166.

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Design System for Semi-Custom VLSI Circuits

The ITT semi-custom design system enables complex VLSI circuits to be designed rapidly with a high expectation of correctness on the first pass. Planned improvements will make it possible to produce semi-custom circuits that are as complex as today's full-custom design circuits.

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Introduction

To maintain a competitive position in an expanding number of markets, telecommunication and electronics companies must make effective use of VLSI (very large scale integration) technologies in their products. The level of complexity (i.e. the scale of integration) that can be achieved on a single chip tends to preclude the use of general-purpose VLSI devices. Increasingly, therefore, VLSI circuits are customized for a particular application. In addition to optimizing circuit and system performance, customization is an effective way of safeguarding proprietary design rights as it is much more difficult to copy a design containing application-specific components than one consisting of commercially available components.

As complexity increases, the cost and time required to produce VLSI circuits using full custom design techniques[1] becomes prohibitive, except for critical designs that have high production volumes. Semi-custom design was identified as a more cost-effective approach for many ITT applications. For example, a semi-custom design may be appropriate for prototyping and early market penetration; this can be followed by a full custom design to reduce costs. Anticipated advances in fabrication technology will enable semi-custom design to produce chips as complex as today's full custom chips.

Elements of Semi-Custom Design

In the present context, semi-custom design comprises two distinct forms of circuit implementation: gate arrays and standard cells. A gate array is a matrix of transistors. Customization is accomplished by laying down different interconnect paths between the transistors. Semiconductor vendors can stockpile basic arrays and individualize them at the customer's request. Advantages of gate arrays include rapid turnaround, since only partial processing is required, and reduced processing cost, since the same base layers can be used in many gate arrays. Their major disadvantage is that some transistors are not used, causing chip area to be wasted and resulting in increased costs.

Chips designed with standard cells overcome this disadvantage. A standard cell chip consists of predesigned blocks of common height but variable width which realize specific logic functions. Standard cell design places the desired blocks in rows and then connects the inputs and outputs so as to perform the required function. The resulting chip area is not as optimized as a full custom chip, for which each circuit element can be individually tailored, but design effort is greatly reduced. Standard cell designs thus fall between gate array and full custom designs in terms of the design effort that is necessary, as well as production cost.

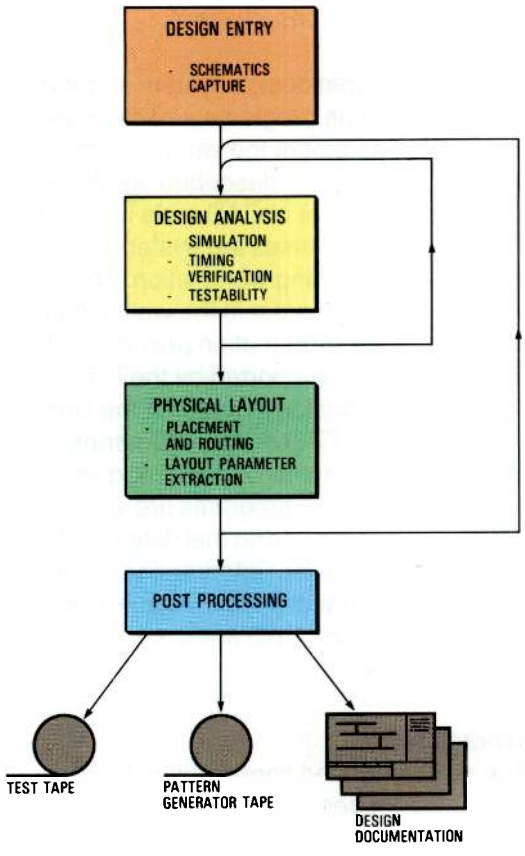

Figure 1
Semi-custom design flow.

Design System Objectives

To attain the objectives of the semi-custom design system (short turnaround times, low development costs, and first pass correctness) several goals were identified at the outset:

- Provide a totally integrated design system, linking all CAD (computer-aided design) tools and design files.
- Provide substantial tool and hardware flexibility through the use of standard programming languages and data formats.
- Use powerful workstations to improve designer productivity.
- Use well-characterized logic elements with performances that have been proved by development and testing within ITT.
- Provide user documentation and training to ensure that ITT units have adequate support in semi-custom design.
- Provide device fabrication information and support to ITT units.

The design system is not aimed solely at ITT units that are closely engaged in integrated circuit design, for which reductions in development costs and time are major goals. It also addresses the needs of smaller units, for which semi-custom techniques allow integrated circuit design to be performed without a highly trained staff or a large expenditure on CAD equipment.

Semi-Custom Design Methodology

The ITT semi-custom design system is based on a design methodology that has proved successful in many ITT projects. However, an advanced workstation-based approach replaces previous design procedures that had to be initiated manually, and required recoding of data for different design tools.

Figure 1 shows the basic elements of semi-custom design. It is sufficiently general to encompass both gate arrays and standard cell designs. The initial step is to capture the circuit in terms of application-specific primitives (i.e. the basic logic functions required for digital design). Table 1 includes examples of the logic functions provided for semi-custom design. For gate array design, the primitives are interconnection patterns of array transistors that realize the logic functions (termed macrocells). In standard cell design, a primitive is the complete graphical representation of all layers required to implement a logic function. The design is analyzed to ensure that it provides the necessary functionality, correctness of timing, and testability. Functionality is

Table 1 - Present gate array and standard cell library elements

Element	Features
Inverter	normal, high speed
Buffer	
AND	2, 3, 4 input
NAND	2, 3, 4 input
OR	2, 3, 4 input
NOR	2, 3, 4 input
Exclusive *OR*	
Exclusive *NOR*	
Multiplexer	
AND-OR-invert	
D flip flop	normal, S, R, S and R
JK flip flop	normal, S, R, S and R
D latch	normal, S, R, S and R
Half adder	
Full adder	
Bonding pads	input, output, bidirectional, and tristate

S - set R - reset

examined by simulating circuit performance, using CAD logic simulation.

Experience suggests that timing problems are by far the most significant cause of semi-custom design failure, so timing verification is a critical part of the design process. Potential timing problems are analyzed using a timing verifier, a CAD tool that checks the arrival time of signals at each design primitive. Potential problems related to setup and hold, clock skew, and race conditions are signaled to the designer.

Testability analysis evaluates the circuit from the standpoint of controllability and observability of the operation of its internal gates from the input and output pins. In addition, test vectors generated by the designer for logic simulation are analyzed to ascertain fault coverage (i.e. what percentage of circuit faults are observable with the test vectors).

When the design engineer is satisfied with the functionality, timing, and testability of the design, physical layout can proceed. This consists of suitably arranging the design primitives and routing the required interconnect. Support is provided by two APAR (automatic placement and routing) programs, one for standard cells and one for gate arrays. Since there are no constraints on the placement of standard cells, the number of wiring channels is not limited and the APAR program should run to completion. In the case of a gate array, placement corresponds to the selection of transistor sites on the predefined array to realize the required primitives. Constraints on routing channel size in gate array designs mean that the APAR program may not complete the design. Manual editing is then required, supported by the design system which ensures that circuit interconnect requirements and technology design rules are not violated.

After physical layout has been completed, the capacitance of the circuit interconnects can be determined from the layout and then used for resimulation and timing verification, a process known as back annotation. If circuit performance is found to have altered unacceptably, it is necessary to repeat the physical layout, manually edit the physical design, or even modify the logical design. The design/layout/analysis procedure is repeated until circuit performance is acceptable, then a pattern generator tape is prepared for mask making. In addition, design documentation (in the form of circuit schematics) and a test tape for circuit evaluation can be generated.

Design System Description

The semi-custom design system supports all the application programs and databases needed to implement the semi-custom design methodology described above. A comprehensive set of CAD tools is built in. The designer accesses the system via a powerful engineering workstation. The key to efficient data transfer is the well defined library of design information provided with the system, and supported by the ITT Advanced Technology Center in the United States and the ITT Europe Engineering Support Centre in the United Kingdom. Interfaces between programs are well defined and controlled so that data transfers require little or no user intervention. Several system configurations are available to adapt to existing ITT unit CAD and computer environments.

Workstation

The recommended configuration for the semi-custom design system is based on an engineering workstation, an extremely powerful engineering aid. Used with CAD tools, the workstation can be part of a distributed processing network capable of supporting the design project from conception through to final layout. Workstations can present both textual and graphic data much more rapidly than standard graphics terminals connected to mainframes. At an extra cost, workstations can support color graphics for such applications as editing of gate array layouts. Printers are supported and plotter drivers are available.

Although the workstation is the preferred alternative, it was recognized during development of the semi-custom design system that it was impracticable to provide a workstation for each designer immediately. Thus the system has been structured to allow for a gradual evolution from mainframe-based systems to workstations. The ITT developed tools are designed to be compatible with both mainframes and workstations, and preference is given to software vendors that provide similar portability.

Design Tools

The semi-custom design system includes CAD tools that aid the engineer throughout the design cycle, from logic design to physical layout. Some operate on logical data, others on physical data. ITT translator programs enable netlists to be generated to

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bridge the gap between logical and physical tools (a netlist is a description of the connections between the logic primitives necessary to realize the required circuit functions). The netlist feeds directly into the APAR programs for both gate array and standard cell applications. Additional netlist formats are available for test pattern verification and testability analysis programs.

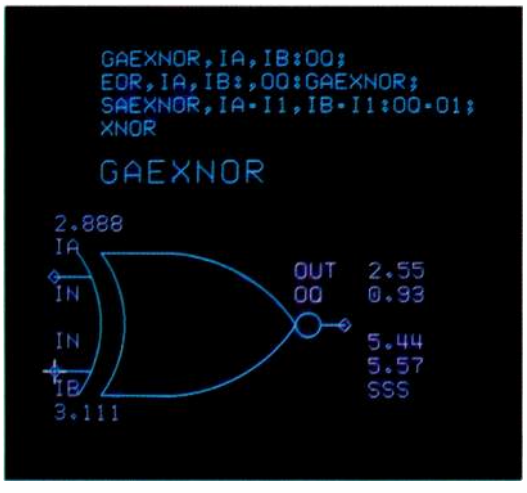


Figure 2
A sample logic symbol showing the physical attributes attached to the symbol and pins.

Design Libraries

The semi-custom design system includes all the logical and physical libraries and technology files required to complete semi-custom designs.

The logical libraries created for schematics capture contain symbolic representations (standard logic symbols) for each of the primitives in the system. Figure 2 shows one of the logic symbols in the ITT library, including the attached property values. Each logic symbol contains timing information derived from the associated layout through circuit simulations. Timing information is used by both the logic simulator and the timing verifier in the semi-custom design system. Translation is done through neutral formats. Library elements are verified and validated with regard to their electrical performance, layout, and intended function using test structures that resemble real applications.

Physical libraries for the gate arrays and standard cells were laid out on a standard integrated circuit interactive graphics system. It is important to note that the layouts for standard cells were derived from the macrocells designed for the gate array family. Thus the standard cells and gate array macrocells are logically and electrically equivalent. A design can be entered and simulated for either a standard cell or gate array implementation, without the need for translation between array and cell primitives or resimulation. Netlists derived from the schematic can drive either the standard cell or the gate array APAR programs. Physical layout information (input/output connection locations, overall size, etc) was used to create data files for the APAR software.

The library of elements includes simple logic gates as well as clocked logic. One, two, three, and four input *AND/NAND/OR/NOR* gates, inverters, flip flops, and input/output pads are among those represented. All are constructed using the ITT 3 μm, two-layer-metal CMOS process. Table 1 lists the elements currently in the library.

Interfaces

Interfaces between various programs within the system and to other design systems are through ITT defined neutral formats for network and graphics data: the neutral network description format and the neutral graphic description format[2]. Translator programs to provide interfaces between these neutral formats and various CAD tools have been developed by ITT units and are supported by the Advanced Technology Center and the ITT Europe Engineering Support Centre.

System Configurations

Three design system configurations are available, all supported within ITT. They differ in the hardware and software used; two are based on commercially available workstations, the third on a terminal connected to a mainframe. All three use common APAR programs for placement and routing.

Design Tools

As already mentioned, CAD tools support the engineer throughout the design cycle, from logic design to physical layout. Tools operating on logical data include schematics capture, logic simulation, and timing verification programs; tools operating on physical data include APAR programs and layout editors. The logic simulator and timing verifier are linked directly with the schematic capture software through a common database. The other tools are linked through the neutral formats.

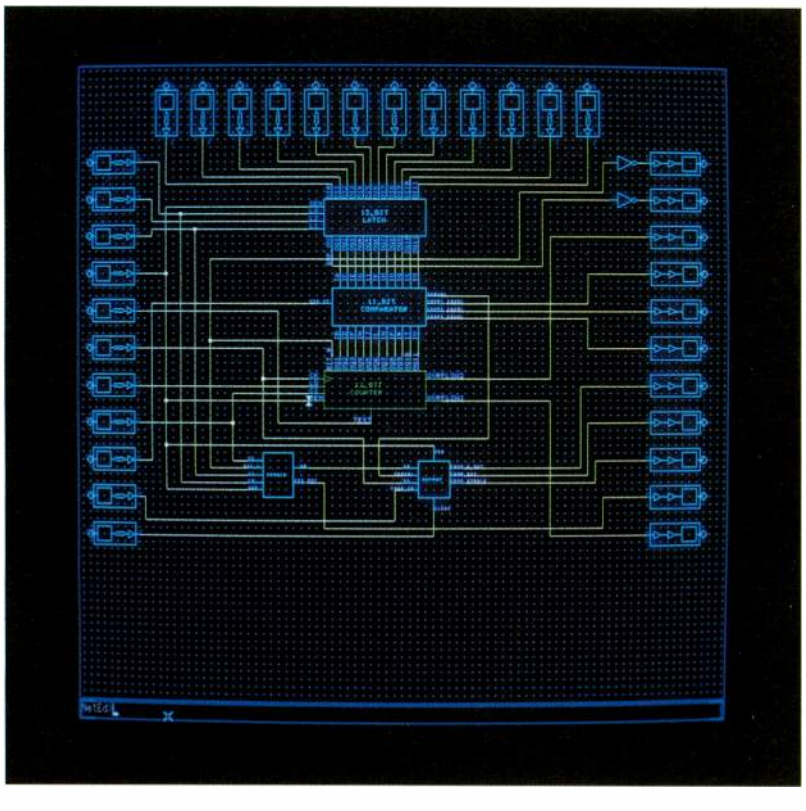
Schematics Capture

Schematics capture enables the engineer to enter a design graphically, eliminating the need for drafting and coding of netlists. Design change is simplified with this interactive tool since primitives and groups of primitives can be moved, deleted, copied, and rotated with ease. Connectivity is retained during changes when appropriate. Schematics capture provides both a graphic description and a logical description of the design. Figure 3 is an example of a design using a schematics capture package. Schematics capture also checks the design and warns the engineer if there are any dangling nodes (unconnected pins), outdated primitives (cells or macrocells that have been modified but not updated on that particular design), or inconsistencies (e.g. two signals applied to one node).

The schematics capture system supports a hierarchical design approach, making it easier to conceptualize and understand the design by partitioning the circuit into functional blocks. These blocks can in turn be partitioned into more specific blocks until the lowest level of detail (the logic primitives) is reached. Hierarchical design also makes simulation easier, since the engineer understands design behavior on a block-by-block basis. The level of detail displayed on the workstation is a function of the position in the hierarchy of the block being displayed. It is possible to display the next lower level of the hierarchy with a single command.

One of the most important assets of a schematics capture system is its ability to generate a netlist from the graphic design. The netlist is *guaranteed* to match the schematic, complete with assigned pin names and the circuit reference, to each instance of a primitive.

Figure 3
A hierarchical design entered into a schematics capture system.



Logic Simulation

The logic simulator applies designer-supplied stimuli to a circuit expressed as a collection of logic primitives interconnected in accordance with the netlist. Simulation is carried out to verify correct circuit function. The initial state of each node in the circuit can be specified. The logic simulator comprehends nine logical states, which are combinations of three logic levels (high, low, and unknown) and three *strengths* (driving, resistive, and high impedance). During logic simulation, the logic state of the nodes in the circuit is computed as a function of the initial conditions, input stimuli, and time. The logic simulator displays the output of selected nodes in a variety of forms. Data formats can be expressed as binary, hexadecimal, octal, or decimal numbers, and/or as waveforms.

Logic simulators supported locally on a workstation can dramatically improve an engineer's productivity. These simulators allow the engineer to interact with the simulation, modify the simulation conditions, and view the design while performing the simulation. This is extremely useful in tracking logic errors, since the sheet that contains the error can be viewed, a node can be highlighted, and its waveform displayed. Events can be checked for spikes and race conditions. Such conditions may render the simulator results invalid, but more importantly they identify circuit design problems. Figure 4 is an example of the application of the logic simulator to the 12-bit counter of Figure 3. In this example a spike was detected during logic simulation. It was possible to go to a lower level of the counter's hierarchy (as shown in the figure), highlight the problem node, and examine its waveform.

Timing Verification

The timing verifier is similar in concept to the logic simulator except that it looks for timing errors. The program extracts parameter values such as setup and hold

times, and guides the engineer in eliminating the fatal errors that can result from race conditions, clock skews, and delay problems. The timing verifier probes selected nodes during one user-defined master clock cycle. It is a local interactive tool, which makes stimuli changes and output probing easy and fast. Figure 5 illustrates the application of the timing verifier to the circuit of Figure 3. This highlights a potential timing problem in one of the counters caused by the carry-in and clock signal changing in violation of defined setup and hold times.

Test Pattern Verification

The test pattern verifier, as its name implies, analyzes a test pattern (set of input vectors) to determine its effectiveness in detecting potential physical faults introduced during fabrication or packaging. It uses ITT's SIMLOG simulator, and operates on the principle of determining what the device output would be *IF* a particular fault were present on a particular node. If the output would differ from the output in the absence of the fault, then that fault is said to be "detectable".

The number of possible faults in the fabrication of a VLSI device is virtually infinite (broken connections, open connections, shorted connections, missing devices, etc); to limit the analysis to a manageable size, and to ease computational complexity, potential faults analyzed are those that cause a node to stay at a constant logic value (stuck-at-*0* faults and stuck-at-*1* faults). The analysis is performed by resimulating the design with the given test pattern for each potential stuck-at fault and comparing the resultant output with the fault-free output. The result of this analysis is a report of the percentage of simulated faults that produce a different output (percentage of detectable faults).

Even with potential faults limited to stuck-at faults, there are still literally thousands to be analyzed. Rather than exhaustively simulating all such faults, they are selected at random for analysis and statistical techniques are used to estimate the actual percentage of detectable faults. The confidence bounds of this estimate can be determined based on the number of faults analyzed.

Testability Analysis

Testability analysis is used to evaluate a design's logical structure and to determine

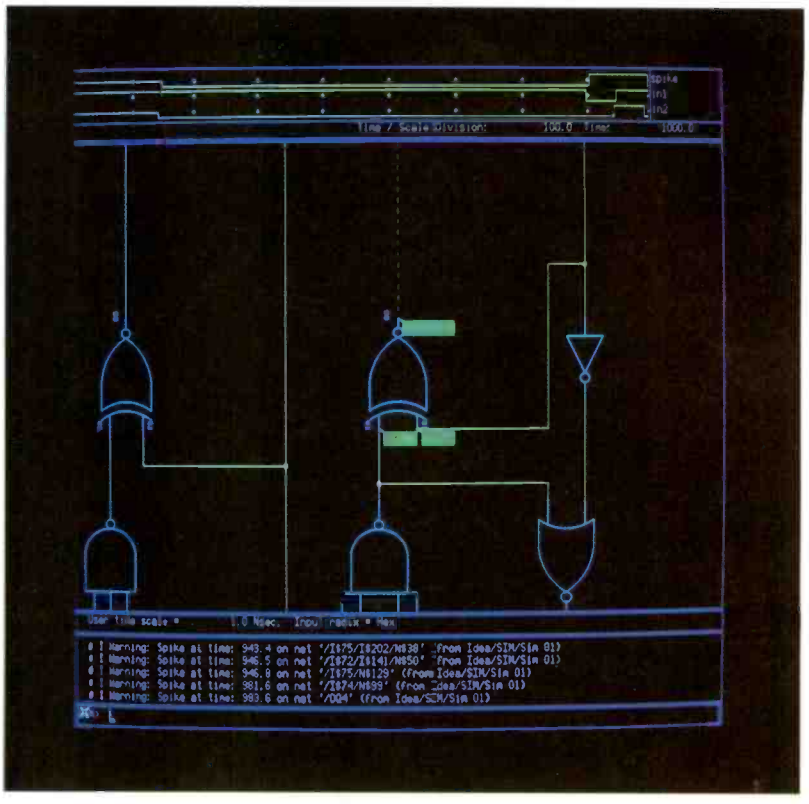


Figure 4
Example of logic simulation output including a warning of the presence of spikes.

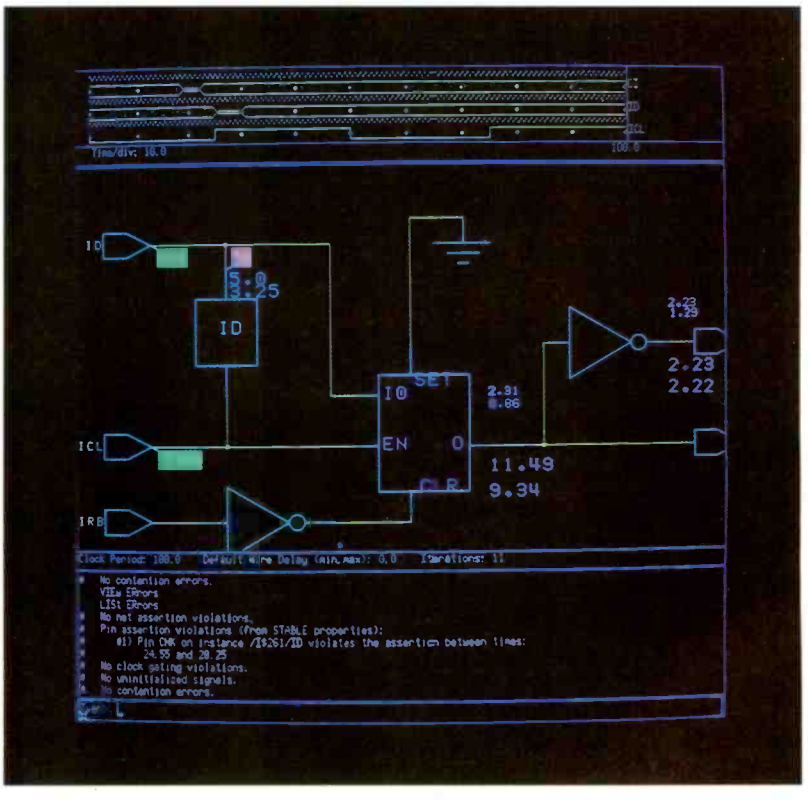


Figure 5
Application of the timing verifier to the circuit of Figure 3. The potential error is listed under pin assertion violations. (The input signals violate a declared property or requirement of the logic primitive.)

how easily potential internal faults can be detected. Complex sequential designs are notoriously untestable since the effect of a fault is not immediately apparent. Designers strive to ease the testing task by incorporating test points which partition the design into less complex sequential modes. The ITT testability analysis program[3] is used to evaluate the result of such activities.

As a companion process, the testability analysis program also attempts to assist the engineer in the partitioning process by conducting a "what-if" analysis: What would be the testability if the signal path were intercepted (i.e. made directly controllable or observable at the input/output pins) at specific points? The engineer is provided with an analysis of the effect of such potential path interceptions for consideration during modification of the design to improve testability.

Automatic Placement and Routing

This is accomplished by two specialized layout programs, one for standard cells and one for gate arrays. Both the standard cell and gate array APAR programs are netlist and design-rule driven. The netlist used is automatically generated from the validated logic schematic via the neutral network description format and ITT interface programs. Since both APAR programs are design-rule driven, it is not possible to have design-rule violations in the final layout, provided the original chip image, macrocells, and cells are correct.

System Status and Evolution

In early trials the ITT semi-custom design system has demonstrated its ability to provide very short design times, compared with a full-custom approach. Of particular importance are the effectiveness of the man-machine interface and the fast response time of the system.

The other advantage of semi-custom compared with full custom design derives from the use of predefined and characterized cells, verification tools, and netlist-constrained layout tools to ensure design correctness. Characterization of circuits based on the cell library and CAD tools is now underway to confirm cell models prior to full scale use of the system, and to confirm the effectiveness of the design verification tools.

Complementary to the design system is a wafer sourcing strategy that permits streamlined logistics for obtaining prototypes and production parts, and a documentation and training curriculum that provides adequate user support to ITT units.

The design libraries will be updated periodically with new cells that will produce more compact structures and increase design flexibility. Developments are also underway to provide the ability to combine cells into block libraries, to provide automatic block routing, and to provide for automatic tailoring of cell dimensions to cell parameters. This evolution of the design system will allow the design of successively more complex chips at the 3 μm level. As technology progresses towards 2 μm and 1.5 μm feature sizes, new design libraries based on these processes will be introduced that will bring the level of chip complexity up to or beyond today's most complex full custom chips.

Conclusions

A fully integrated design system is crucial to the effective exploitation of semi-custom design techniques in order to reduce design development time and costs. The ITT semi-custom design system provides an integrated set of CAD tools implementing all portions of the design process from schematics generation to mask generation, and working within a computer/terminal environment that is optimized to engineers' productivity. A set of design libraries is available in which cell layouts and performance are fully verified and based on design rules compatible with state-of-the-art CMOS processing.

This system provides ITT units and research centers with a fully supported design capability for the rapid design of medium complexity VLSI chips, as well as the capability for evolution to higher complexities in the future.

References

1 J. Danneels and M. Meinck: Methodologies for Full Custom VLSI Design: *Electrical Communication*, 1984, volume 58, no 4, pp 389–397 (this issue).

2 K. R. Bennett and G. J. Lovitt: Data Modeling: the Key to Design System Integration: *Electrical Communication*, 1984, volume 58, no 4, pp 380–383 (this issue).

3 R. M. McDermott: ITT's Testability Analysis Program: *Electrical Communication*, 1984, volume 58, no 4, pp 433–439 (this issue).

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Data Modeling: the Key to Design System Integration

Integrated design systems require well defined data interfaces through which information can be communicated. A data analysis technique normally associated with database design has been used to develop sequential data formats for a VLSI design system.

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Introduction

Very large scale integration (VLSI) technology presents challenges to both hardware design engineers and to the designers of CAD (computer-aided design) systems. As the scale of integration increases so also does the complexity of the design task. Designing circuits that incorporate hundreds of thousands of transistors requires new design methods and new CAD tools to capture, process, verify, and manage design data.

The challenge to the CAD system designer is therefore to provide a design system environment within which existing and planned CAD tools for VLSI development can be integrated and into which new design tools may be introduced easily and effectively. A tool interfacing strategy was required for a new CAD system[1] which would support semi-custom VLSI design approaches based on the use of predefined standard cells or gate arrays.

Design System Integration

A computer based design system for the support of a task as complex as that of VLSI circuit design will, of necessity, be subdivided. Each part, in itself a tool, supports a particular stage or aspect of the overall design task such as design capture, simulation of a circuit's behavior, or verification of design rules. The semi-custom design system required many such tools, some developed in-house and others bought in. (Over a period of time, alternatives will become available for some tools.) Furthermore, these tools may be distributed over different computers; for example, some may be run on workstations and others on mainframe computers.

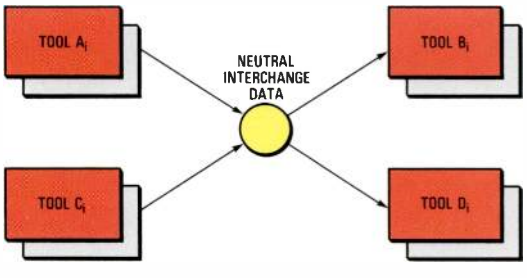


Figure 1
Interface requirements in an integrated design system.

Interfacing Strategy

Interfaces are required between such tools to enable relevant data to be passed between them.

Figure 1 illustrates the selected interface strategy. Four tools are shown, each of which is one member of a set of tools of somewhat similar function. Data generated by tool Ai or Ci is passed to tools Bi and Di in such a way that if Ai is replaced by Aj then any disturbance to the rest of the system is minimized. The tools are not tightly coupled by their data interfaces; instead they communicate with each other via neutral (tool independent) interchange data. Using this strategy, the introduction of tool Aj only requires a simple translator program between Aj and the neutral interchange data, assuming that sound data analysis techniques have been used to produce the definition of the interchange data.

Standard Telecommunication Laboratories (STL) used a data modeling technique to design these data formats.

Data Analysis Techniques

In the past, formalized data analysis techniques have usually been associated with the design of schemas for databases and have reflected the type of data structure which the particular databases supported (e.g. hierarchical, networked, or relational); each of these data analysis techniques has its own type of data model.

The term "data modeling" is not yet widely understood. VLSI data models are not models of a particular VLSI chip, since it is the various types of design data that model a chip at several abstract levels. One type of design data is represented in Figure 2, which is a schematic of a hierarchical network of cells.

Codd's work on relational algebras was the foundation of relational models of data in which data is held in simple tables[2]. His concepts for the organization of data may be applied to any data analysis task irrespective of the eventual physical organization of interchange data in a system and therefore allow implementation decisions to be taken after the data analysis stage. It was for this reason that the relational data modeling technique was chosen.

Practical Application of Data Modeling

To apply the data modeling technique successfully, the following analysis and design stages must be carried out:

- requirements analysis
- data dictionary generation
- data model construction
- data formats definition.

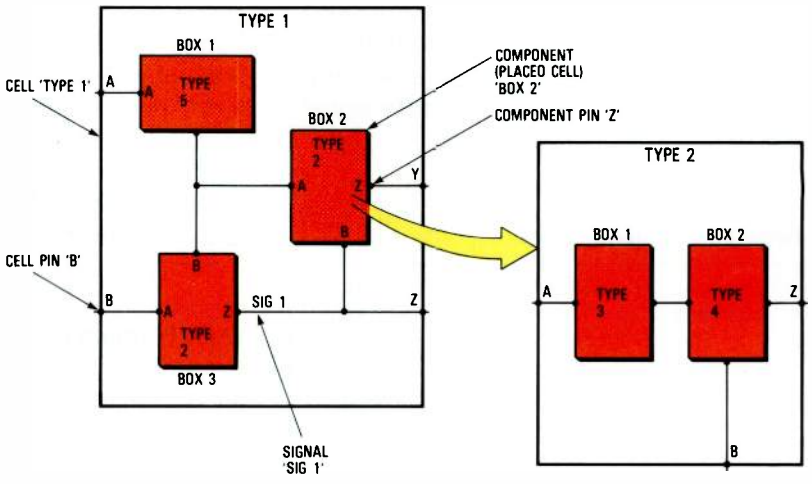
Requirements Analysis

Before attempting any implementation, a well defined and agreed requirements specification is essential. Data being transferred between tools was identified as being either network (electrical) data or graphical (mask layout) data. It was agreed that there was no immediate requirement for a single format that would cover both types of data. Each format was therefore modeled separately.

The NNDF (neutral network description format) was required to describe electrical networks and to be able to hold additional tool specific data, which might need to be associated with the basic network data. It was required to support hierarchical design, as illustrated in Figure 2. The requirement that the format be fast and easy for tools to read and write was found to be incompatible with a requirement for easy manual input. This conflict was resolved by designing a separate neutral network description language for manual input, which may be compiled into the NNDF.

Requirements were also defined for an NGDF (neutral graphical description format).

Figure 2
Entities for a hierarchical network of cells.



Data Dictionary Generation

Precise definitions of elementary pieces of data are recorded in a data dictionary. However, generation of the data dictionary is not as simple as it first appears as there is a degree of choice over the level of visibility shown. It was decided that certain items of VLSI data (i.e. those that are specific to a particular tool) should not be identified as individual data elements. The method invented was the concept of attributes. Each attribute relates to a physical entity (e.g. component pin attribute) and consists of two elements – attribute name and attribute value. For example, the dictionary defines *component pin attribute name* and *component pin attribute value* as data elements, but users of the tools must know the meanings of the possible values that they can take. The attribute method conceals items and would be regarded as wrong by most database designers. However, it is very powerful and eliminates the need to update the data dictionary continuously and to extend the data model every time a new tool has to be integrated.

Data Model Construction

Having defined a dictionary of data elements, the data model is constructed. In

practice the generation of a data dictionary and data model was an iterative process that involved several review and rework stages before agreement was reached. However, subsequently there has been very little change in the models, or the formats that were generated from them.

The first stage in the construction of a relational data model is the identification of entities. Consider the requirements for a hierarchical network of cells as illustrated by the example in Figure 2. Five types of entity are identified: *cell, cell pin, component, component pin,* and *signal*. The term *cell* is used for a cell definition (its proforma) whereas *component* is used for an instance of a cell (an instantiation). The entity *signal* is an interconnected net of pins.

Table 1 — Component data

Calling cell name	Component name	Placed cell name
Type *1*	Box *1*	Type *5*
Type *1*	Box *2*	Type *2*
Type *1*	Box *3*	Type *2*
Type *2*	Box *1*	Type *3*
Type *2*	Box *2*	Type *4*

A number of data elements may exist for each type of entity. The data model depicts the relationships between these data elements which are inherent in the data and are independent of data storage or processing. The data model represents these relationships, as shown in Figure 3 where the two key data elements *A* and *B* are separated from the dependent ones *C, D,* and *E* by the green band.

Relationships between data elements can be determined by careful analysis. As an example, consider the three data elements for the component entity. *Calling cell name* (e.g. Type *1*) is the name of the cell in which the cell is placed. *Component name* is the instance name of the component (e.g. Box *2*). *Placed cell name* is the name of the cell which is placed (e.g. Type *2*). A simple table may be constructed giving data for each of the components shown in Figure 2 (see Table 1). Each row in the table represents one component. No single data element value may be used to identify any one component uniquely. However, the combination of *calling cell name* and *component name* is always unique. This is formally defined in the data model (Figure 4) where the component

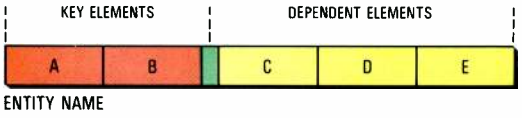


Figure 3 Relationship representation for an entity.

entity is shown to have two key data elements and one dependent data element.

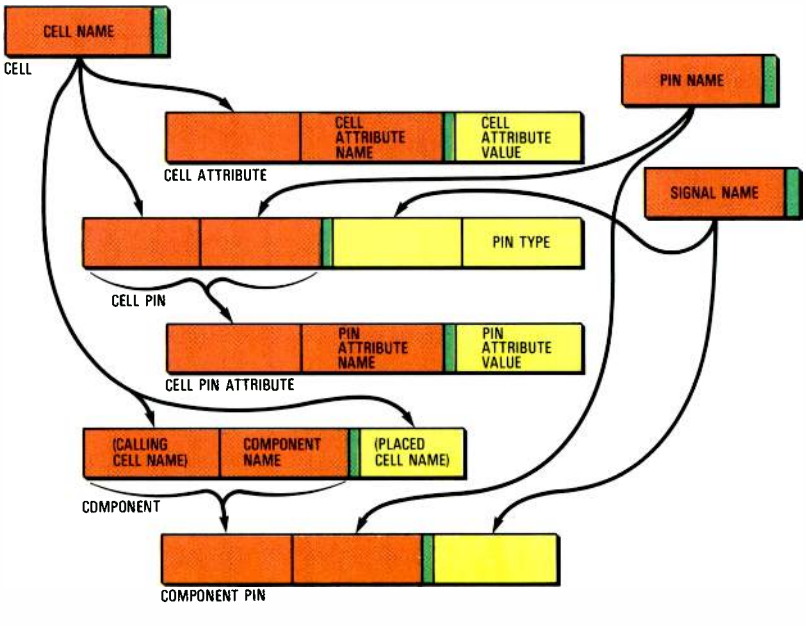
Once entities have been identified and the relationships between their data elements have been established the data model may be produced.

Figure 4 is about half the size of the full NNDF data model, but illustrates the important principles. The model supports a hierarchy of cells to any number of levels and allows cells and cell pins to have attributes. The full NNDF and NGDF data models were developed jointly by CAD designers from STL and ITT using this technique and have been fully documented.

Data Formats Definition

Once data models have been produced and an implementation strategy has been defined it is a simple task to define interchange data formats unambiguously and rigorously. The method employed was to generate a Jackson structure diagram of the format identifying the sequence and iteration of the record types which are perceived as being necessary to implement the data model. Typically a separate record type is created for each grouping of data elements into a key. As the formats are fixed length records (for portability), other record types are used for dependent data elements with continuation record types as required.

Figure 4 Data model for a hierarchical network of cells.



Experience with VLSI Tool Integration

The work described here was carried out as part of a computer-aided VLSI design project led by ITT's Advanced Technology Center in the USA with the participation of Bell Telephone Manufacturing Company, Belgium, and the ITT Europe Engineering Support Centre and Standard Telecommunication Laboratories in England.

The data models provided a good basis for a rigorous review of the interfacing requirements. Once agreement had been reached, the data models were finalized and data format definitions produced.

A number of translator programs have been implemented between tools and the neutral data formats. These programs provide the required interfaces between the set of tools and they enable the tools to be integrated into the design system for semi-custom VLSI devices[1]. The formats have proved to be stable throughout the development period.

Conclusions

Relational data modeling has been used as the basis of a sound data analysis technique which has enabled the requirements of neutral interchange data to be carefully studied and rigorously documented. This type of data modeling was appropriate, even though relational database techniques were not used. The technique usefully decouples the task of information analysis from the detailed specification of formats, and its wider application should be considered.

The electronics industry as a whole would benefit from the wider availability of neutral data interfaces between CAD tools.

References

1 A. D. Close, L. Fisher, R. M. McDermott, T. A. Nix, D. M. Perinne, and J. M. Schoen: Design System for Semi-Custom VLSI Circuits: *Electrical Communication* (1984), volume 58, no 4, pp 372–379 (this issue).

2 E. F. Codd: A relational model of data for large stored data banks: *Communications of the Association for Computing Machinery*, June 1970, volume 13, no 6.

Keith R. Bennett was born in Cheam, Surrey, in 1943. He obtained a BSc in Physics from the University of Hull in 1965, then joined STC where he worked on microelectronic equipment practices. In 1966 he joined ICT (later to become ICL) to work on computer-aided design of electronic systems. Since 1975 he has worked for STL, leading computer-aided design developments for printed boards. Major developments were a tool interfacing system and an in-house schematics capture system. More recently Mr Bennett has been concerned with general considerations of CAD interfacing for VLSI.

Graham J. Lovitt was born in 1943 in Epping, Essex. He studied mathematics at Imperial College and applied physics at Enfield College of Science and Technology. He joined STL in 1964 where he has worked on a variety of projects ranging from the mathematics of thin evaporated film deposition to the software development support system for System 12. In 1983 Mr Lovitt joined the STL CAVD group which was formed to continue the development of VLSI CAD tools.

Design of a 3-micron CMOS Cell Library

A new CMOS standard cell library has been designed for producing more complex and higher speed semi-custom VLSI circuits using the emerging 3 μm technologies. The library has been designed to be compatible with *p*- and *n*-well CMOS processes, one- and two-layer metallization, and suitable single- or double-sided cell autolayout software.

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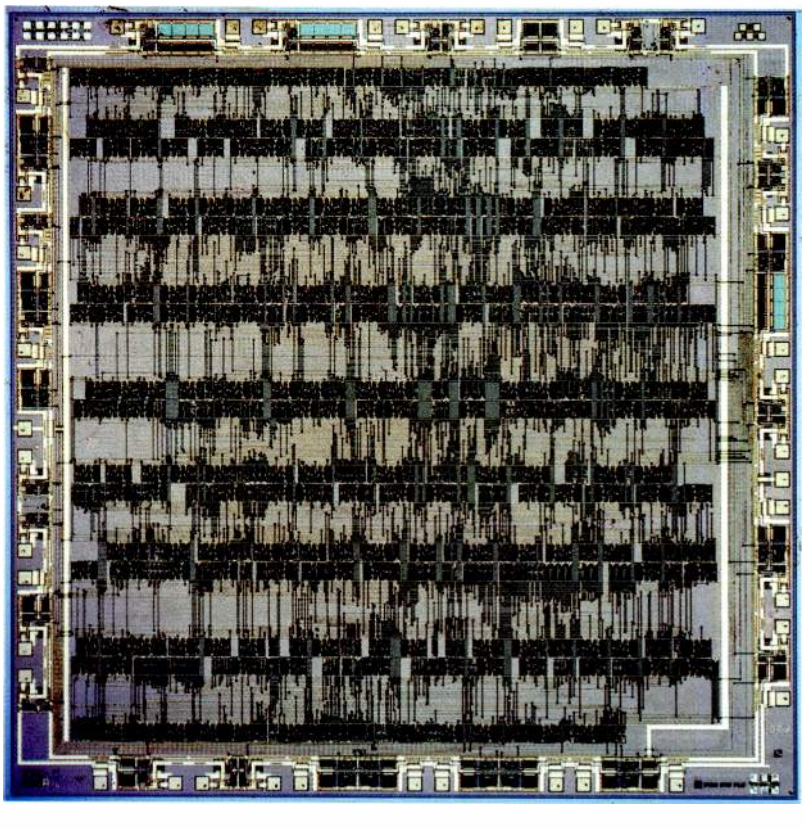
Introduction

A standard cell library with an automatic layout program provides an effective means of producing low risk, cost-effective semi-custom VLSI (very large scale integration) devices in comparison with full custom design or uncommitted logic arrays. The principal benefits of standard cells are:

- smaller die size than uncommitted logic arrays
- reduced risk of design errors, and hence design recycles, by the use of proven cells
- shorter layout times than full custom design
- flexibility to introduce new cells to meet particular application needs
- capability of being produced by a number of semiconductor manufacturers.

Typical chip produced using an autolayout program and a standard cell library.



Automatic layout software enables a manufacturing tape to be produced in two weeks from the date of final logic approval. Autolayout software currently in use within ITT and affiliated companies can typically produce a 1 400-gate circuit with a 44 mm^2 die size using the ITT 5 μm CMOS cell library. Standard Telecommunication Laboratories (STL) designed this 5 μm CMOS cell library in 1980. It has since been used for more than 14 circuits ranging in complexity up to 1 700 gates and 4 MHz operation. Various circuits have been successfully manufactured by seven independent suppliers.

In early 1983 it appeared that 3 μm CMOS (complementary metal oxide semiconductor) technologies had matured to the stage at which a new cell library could be developed to take advantage of the speed and density improvements offered by this process.

Objectives

At the outset of the programme the following objectives were set down as desirable and probably achievable:

- Operation at 8.2 MHz to serve applications associated with European group pulse code modulation multiplexers operating nominally at 8.192 MHz.

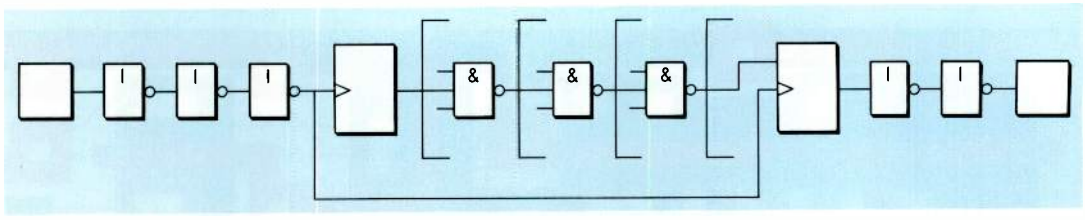


Figure 1
Critical paths in a typical system.

- Compatibility with *p*- or *n*-well processes. While it was recognized that there was strong interest in ITT for an *n*-well cell library because of its slightly higher performance, it was felt that *p*-well processes were generally more mature, especially in semiconductor companies traditionally associated with low volume, customer designed products and as such should be easier to manufacture.
- Compatibility with single- and two-layer metal processes. The introduction of a second level of metal for interconnect instead of the highly resistive polysilicon eliminates a major source of timing problems. However, two-layer metal MOS technologies are less mature and more expensive than single-layer metal technologies which can still service the lower performance applications.
- Capability of being manufactured by several manufacturers.
- Complexity of around 2500 gates.
- Compatibility with Calmos and Calmp automatic layout software, the two main programs used in ITT and the semiconductor industry.
- Suitable for use by nonexpert designers by reducing the number of pitfalls normally associated with cell library design, in particular the layout dependent ones. This mainly affected the design of latch circuits.

System Analysis

In designing a cell library it is not sufficient simply to declare the operating speed as 8.2 MHz. Before commencing the electrical design of the logic gate it is necessary to establish its required delay and drive capability, which in turn makes it necessary to decide on the number of gates between latches and to estimate the electrical load connected to its output. This load consists of the input capacitance of the gates it drives (fanout) and the capacitance and resistance of the polysilicon and aluminum tracks that connect them (interconnect load). These are shown in Figure 1. The interconnect length depends on the die size which itself depends on the gate count.

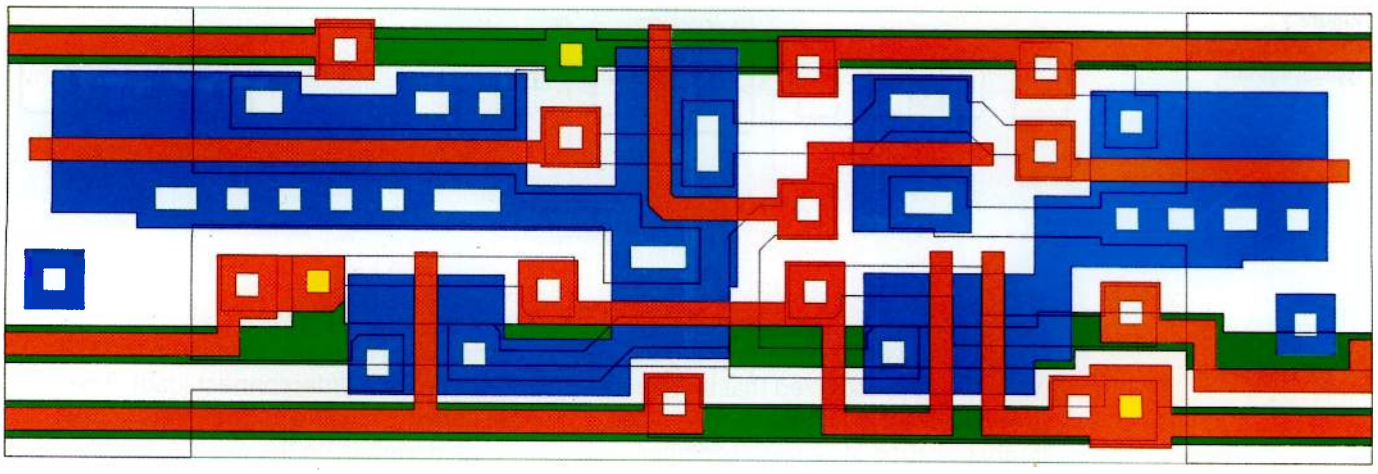
The main aim of electrical design is to determine the dimensions required for the transistors in the circuit. In an MOS (metal oxide semiconductor) transistor, the ratio of the width to length of the channel determines its minimum resistance and hence the speed at which the load capacitance can charge or discharge. At STL, electrical design is performed using a version of the Spice electrical simulation program which has been modified to improve its accuracy and ease of use.

It should be noted that the autolayout programs used place cells in horizontal rows with corridors between them for interconnect. Usually metal is used for the horizontal sections of interconnect, and polysilicon for the vertical sections.

Initial Design Cycle for Single-Layer Metal Interconnect

The first design cycle attempted to achieve 8.2 MHz operation for a 6.35 mm die with four gates between latches and a fanout of three from all elements. The latch was assumed to have a 2-gate delay setup time and a 2-gate delay to output.

Based on observations with the previous cell library with regard to how Calmos placed and connected cells together, the interconnect load was initially taken to be 6 mm of metal plus 6 mm of polysilicon. However, this configuration cannot achieve the required speed of operation. Although the required average gate delay is only 15 ns, the 6 mm of polysilicon has a resistance of 75 kΩ in the technologies under consideration which, together with a typical interconnect capacitance of 1 pf, gives rise to a delay for each gate of about half that of the 122 ns available for the whole clock period!



Typical cell layout: the circuit shown is a 2-input NAND gate.

Final Design Decision

After many design iterations the following system parameters were found to achieve the desired clock rate under worst case conditions: a 5.5 × 5.5 mm die and an interconnect load of 5.1 mm of metal plus 1.27 mm of polysilicon. In addition there would be three gates between latches, and a fanout of three from each element.

To achieve the desired gate performance it was necessary to adopt a buffered gate architecture, as shown in Figure 2. This minimizes input capacitance, which otherwise rises substantially for gates with large numbers of inputs, and provides sufficient gain to achieve adequate drive for the design load and delay.

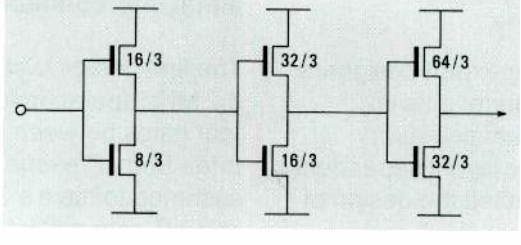


Figure 2
Circuit diagram of the buffer chain for each gate. Transistor dimensions are shown as length/width in μm.

Performance with Two-Layer Metal

Using the same assumptions as above but substituting a second layer metal for polysilicon, the predicted system performance, again using Spice, rises to 16 MHz. This is because the interconnect resistance drops to almost zero, and the second metal capacitance to the substrate is approximately half that of polysilicon because of increased dielectric thickness between the top layer of metal and the silicon substrate ground plane.

As a result of this dramatic improvement in performance it becomes possible to increase either the gate count or the number of gates between latches or the fanout of each gate. These options are likely to prove attractive since it is not possible to achieve this improved frequency performance for the clock and output buffer circuits using straightforward semi-custom design techniques.

There are three principal reasons for the performance limitations of the clock and output buffer circuits. First, the minimum achievable delay between the final latch and the output buffer is 45 ns using a standard latch with a 20 pf off-chip load. Second, the final latch has to be of a standard size so that the assumptions on which this high internal achievable clock rate are based are not violated. Although these restrictions can be overcome using methods which are well known to custom VLSI designers, they are rather complicated for use with semi-custom design. Finally, assuming that the clock input to the chip is from transistor-transistor logic, the minimum achievable delay between the clock input pin and an internal latch is 15 ns. Assuming that the setup time for data arriving at the next chip in the system is 20 ns, then the minimum clock period is 80 ns, or about 12 MHz.

Characterization Details

In designing this 3 μm cell library, the performance of a gate was determined by simulating three such gates connected in series coupled with appropriate loads, and measuring the response of the last one. This makes it possible to measure the gate behavior under realistic conditions. Some cell libraries are characterized using ideal

input waveforms which have the effect of dramatically improving the response time of the gate. However, such input waveforms are not encountered in practice and consequently the stated performance is never achieved.

Design Rules

VLSI design rules are the minimum dimensions of the features of a layout (track widths, spacings, overlaps, round contacts, etc). Each semiconductor manufacturer has his own set of design rules which reflect his particular processing capability (some can reproduce finer features than others). In order to produce a layout which can be made by more than one manufacturer, it is necessary to create an "umbrella" design rule set. This is done by first selecting manufacturers with similar technologies and obtaining their design rules (which are generally jealously guarded in a similar manner to trade secrets). After careful study and discussions with the manufacturers, the umbrella rule set is formulated based on the capabilities of the equipment in use, in preference to simply adopting the largest value for each rule which would result in an unacceptable increase in chip area and degradation in electrical performance.

Some 28 companies in the world claim a 3 μm CMOS process capability. Of these, 14 were contacted as possible sources of this library, the others being ruled out on technical or commercial grounds. Design rules were obtained from six of these companies and used as the basis for the STL umbrella rules.

Layout Techniques

To achieve compatibility with *p*-well and *n*-well CMOS processes, the design rules and cell layouts incorporate both wells. Similarly, to achieve one- and two-layer metal process capability, each cell is designed with both present; the second layer of metal is used to duplicate the relatively high resistivity polysilicon for interconnection purposes. All that is necessary to produce the correct mask set for a particular technology and wafer manufacturer, after completion of the layout, is to specify which layers are required to the program that produces the mask making machine tape.

p-Well versus *n*-Well Performance

To quantify the differences between these two processes, the performance of a simple inverter was characterized using Spice to determine the speed tradeoff and the optimum ratio of device sizes for a library intended for sourcing with either process. Table 1 summarizes the findings for typical process parameters (e.g. gate oxide thickness, threshold voltage). The differences in performance are in fact less than the variation in performance resulting from the spreads of the process parameters.

In addition, consideration was given to the compromise in layout area as a result of adopting dual well rules. Table 2 summarizes the well-related design rules for each process. While there is a noticeable difference in these rules, the effect was predicted as an increase in die size of less than 50 μm on a 1 400-gate circuit of about 6.1 × 6.1 mm (i.e. insignificant compared with the area taken up by interconnect using autolayout software).

Current Status

The library contains 25 logic elements and five peripheral buffer elements. The logic members may be summarized as follows:

- inverter up to 4-input NAND and NOR gates

Table 1 – Comparative performance of a small inverter

Optimized for	*Wp* (μm)	*Wn* (μm)	t_r/t_f (ns)	
			p-well	*n*-well
p-well	6	3	8.0/8.5	—
n-well	8	3	—	5.7/6.0
Dual standard	8	3.5	6.5/7.5	5.5/5.2

Wp - width of *p* channel
Wn - width of *n* channel
t_r - rise time of output voltage waveform
t_f - fall time of the output voltage.

Table 2 – Comparison of diffusion spacing rules

	Typical *n*-well process	Typical *p*-well process	STL design rule
Diffusion outside well – minimum clearance (μm)	10.0	13.0	14.5

Table 3 – Cell library elements

Inverters	
IC3020A	Low capacitance inverter
IC3021A	Standard inverter
IC3022A	Double driver
AND-NANDS	
IC3024A	2-input NAND
IC3025A	3-input NAND
IC3026A	4-input NAND
OR-NORS	
IC3030A	2-input NOR
IC3031A	3-input NOR
IC3032A	4-input NOR
IC3035A	Exclusive NOR
Flip-flops	
IC3058A	Buffered NOR latch
IC3059A	Transparent latch
IC3060A	T type; reset with control
IC3061A	T type; set, reset with control
IC3062A	T type; reset
IC3063A	T type; set, reset
IC3070A	D type; reset
IC3071A	D type; set, reset
IC3072A	D type; no set or reset
IC3073A	D type; set
IC3074A	D type; D to VDD: set, reset
IC3075A	D type; D to VDD: reset
IC3076A	Parallel input D type; reset
Flip-flops (cont)	
IC3077A	Parallel input D type; set, reset
IC3078A	Parallel input D type; no set or reset
IC3079A	Parallel input D type; set
Special functions	
IC3080A	Half adder
IC3081A	Full adder
IC3084A	T gate buffered clock
IC3090A	Matrix gate NOT [A · B + C · D]
IC3091A	AND-OR select
IC3093A	Grid gate NOT [(A + B) · C]
IC3094A	Matrix cell NOT [A · B + C]
IC3108A	Via cell manual
IC3109A	Via cell auto kon
IC3110A	Contact cell manual
IC3112A	Contact cell auto kon
IC3115A	Feed cell for Calmos/Calmp
Peripherals	
IC3170A	Pad VSS cell
IC3171A	Pad VDD cell
IC3180A	Inverting CMOS input buffer
IC3181A	TTL input buffer
IC3188A	Bidirectional buffer; TTL input
IC3191A	Bidirectional buffer; CMOS input
IC3192A	Output buffer
IC3197A	Tristate output buffer

– varieties of latch

– other combinational functions (e.g. full adder, multiplexer).

A complete list of the currently available cells is given in Table 3. All logic elements have a similar drive capability (5 ns pf^{-1}), similar input capacitance (0.01 pf), and similar internal delay (5 ns), which greatly simplifies circuit design using this library.

At the time of writing (April 1984), the library is complete and has been checked using the CAD software written by ITT for custom VLSI circuits. An elaborate test chip has been designed which exercises all the major parameters of each cell. The results from this test circuit are expected by mid-1984 when the guaranteed cell library will be available for use throughout ITT together with a new user's handbook.

Conclusions

It has been possible to design a multisourceable 3 μm cell library capable of 8.2 MHz operation in single-layer metal technology for realistic 2000-gate systems. This appears to be the practical limit for single-metal technologies. The introduction of two-layer metal technology raises the speed limit to 12 MHz, but to achieve even higher speeds will require semi-custom VLSI designers to adopt more sophisticated design techniques.

Christopher P. Lincoln was born in April 1949 at Chatham, England. He graduated from Southampton University in 1970 with a BSc in electronics. On graduating he joined the LSI design group at STL where he has been involved in silicon LSI design and CAD. Mr Lincoln is now manager of the VLSI design automation group in the VLSI Technology and Design Methods Division.

Methodologies for Full Custom VLSI Design

As the complexity of integrated circuits continues to increase at a rapid pace, new design methodologies and tools are essential to ensure correct, cost-effective design. The goal is to be able to produce a correct chip design from the initial functional specification with minimal human interaction.

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Introduction

Over the past 20 years there has been a dramatic increase in integrated circuit density, manufacturability, functional capability, and operational speed. This improved performance has led to LSI and VLSI (large scale integration and very large scale integration) circuits being used routinely in telecommunication equipment, military systems, computers, alphanumeric terminals, calculators, wrist watches, audio and video equipment, automobile control systems, and so on. The application of LSI and VLSI circuits provides an excellent opportunity to reduce a system's size, weight, power requirements, and number of components, while improving reliability and maintainability. At the same time it simplifies system manufacture. Perhaps one of the most striking advantages of using custom LSI and VLSI circuits is that they enable increasingly complex equipment to be designed and produced cost-effectively.

Today there are at least three different forms of custom LSI and VLSI devices: gate arrays, standard cell circuits, and full custom design circuits. Each approach has merits and the choice is primarily based on trading off nonrecurring costs and development time against recurring or manufacturing costs. The advantages of gate arrays and standard cell designs are covered elsewhere in this issue[1, 2].

The choice between various custom LSI or VLSI circuit techniques must be based on a full analysis of each approach. In effect, a short proposal is generated for each alternative. This might include a gate array, a standard cell design, and a full custom design, as well as industry standard integrated circuits configured to produce the correct function. If total cost is the overriding factor, a breakeven analysis is employed to determine the most cost-effective approach[3, 4]. However, if the full capability of a given semiconductor technology must be realized in terms of size, power, weight, reliability, speed, and performance, there is no substitute for full custom design LSI and VLSI devices.

Twenty years ago integrated circuit design was the province of a handful of experts who were familiar with processing technology, along with logic design and circuit design. The design methodology was based on the use of paper and pencil, with a slide rule or calculator as the only tool.

Today the integrated circuit topology is designed on interactive graphics terminals connected to computers. Instead of a polygon being drawn by hand, the coordinates are stored in computer memory enabling it to be plotted. In addition, when the design is complete, the computer can drive optical pattern generators or electron beam mask making machines to produce reticles and masks.

Current Design Methodologies for Full Custom VLSI Design

Once the system design has been completed and verified, the methodology used to develop a full custom VLSI chip that meets the system requirements follows a planned, interactive flow with three major phases: a feasibility study; the design itself; and analysis of the resulting chips.

Phase 1: Project Feasibility Study

Program Definition: Statement of Work
Any custom VLSI design starts with an overall feasibility study which determines whether the system requirements can be met within the overall project limits, such as circuit performance, production volume, chip area, and development schedule. It is a critical phase in the design as any misunderstanding, incorrect assumption, or error in a calculation can make the difference between a successful design and an unsuccessful one.

Determining the feasibility of a complex VLSI project requires a sixth sense to grasp the key issues involved in implementing a newly defined system in silicon. In most cases it can be tackled by defining a block diagram consisting of elements which have some similarity with successful past designs.

Circuit Conception
The top level block diagram has to be detailed section by section. Each section will be of a particular type of circuit, and may well form part of a standard cell library of simple gates and macro blocks such as counters, programmed logic arrays, shift registers, operational amplifiers, comparators, and analog-digital converters.

Any circuits that are not part of such a library must either be developed or derived from other sources. All new and derived circuits require extensive simulation to prove their suitability for the particular application.

Circuit and System Simulation
In addition to detailed characterization of the subcircuits, the overall system performance must be simulated. This requires the definition and specification of all subsystem interfaces and, more important, of the overall system functioning in accordance with a generic specification. In this area the key problems are optimum system partitioning within the constraints of system stability, available technologies, and optimal performance. Some parts of the system may require the use of bipolar technology, while others are better suited to MOS technology. This interactive optimization process involves a variety of simulations from general block level behavior to very detailed analog or digital behavior.

Feasibility Report
A first feasibility report can be produced after the chip architecture and its environment have been defined, including all the necessary interfaces to the rest of the system. It consists of a preliminary system partitioning, including an indication of the likely VLSI circuits and their links to the system. This is followed by a more detailed schematic description of the VLSI architecture indicating the key problem areas with respect to either circuit design or technology. Next comes an estimate of the approximate placement of macroblocks and of the package and pin configuration. A component count and classification then leads to an estimate of the chip area. Using these estimates, the cost of the circuit can be predicted. Finally, resources can be allocated and an overall schedule defined for the entire VLSI development project.

Worst Case Analysis
Poor device yields during manufacture are not necessarily the result of the technology or manufacturing process. In some cases a marginal design can cause major rejects amongst dice with no manufacturing faults. The most serious cause of marginal performance is the presence of parasitic effects, such as thyristors or MOS channels through the field oxide, which alter the gain and increase power dissipation. They cannot be simulated because they are not part of the design; this also makes them difficult to detect. Less dramatic, but even harder to locate, are the parasitic couplings at multilayer crossings or as a result of the capacitance between long, closely spaced lines.

Mismatch between a vendor's process and the design parameters could lead to a large drop in the manufacturing yield of VLSI devices. To ensure that this does not occur, extensive simulation is required, taking into account the limits of the processing technology and of the operating conditions. The result may be that the mask will have to be adjusted slightly to suit the process of a particular vendor. Parameters which frequently vary from vendor to vendor include mobility, bulk factor, and interconnect resistance. The evolution to smaller device geometries worsens the situation as the divergence between parameters increases and the simulation models become less accurate.

Phase 2: Custom VLSI Design

Integrating more and more transistors into a single chip has well recognized advantages, but system complexity is not reduced and is

now centralized into one component. As a result, many of the hardware problems inherent in any complex electronic system are now being passed on to the VLSI circuit designer.

Two organizational structures can be used to cope with the complexity of VLSI design. One is to subdivide the work into system design, circuit design, circuit layout, and testing. This has the advantage of splitting the overall multidisciplinary problem into smaller tasks requiring specific skills, and allows work to proceed in parallel. The drawback is that it introduces interface and communication problems.

The alternative organization involves a team of multidisciplinary experts who perform all the circuit design, simulation, layout, verification, test, and debugging tasks under the coordination of a project leader. This reduces communication and interface problems but requires a higher level of skills throughout the group. If this approach is to be used successfully, long-term design strategy must be based on the use of powerful design tools.

Interactive Graphics System

As the computing power of an interactive graphics system steadily increases, making it possible to carry out more complex tasks, the selection of a particular system becomes very difficult. The man-machine interface is particularly important. In addition, the system must be able to draw rapidly, efficiently manage workfiles containing thousands of data blocks, and convert data into various formats as quickly as possible.

Layout Methodology (Figure 1)

Before layout is started, accurate documentation has to be generated containing all the specifics of the circuit diagrams down to the last detail, such as all connections (the netlist), gate width/length ratios, and transistor types. Interactive simulations and circuit modifications are frequently required to ensure that the design fully meets the operating specification.

Next a broad outline of the integrated circuit is defined. The input/output constraints are taken into account from the outset. In most cases the pin-out sequence is completely defined, although the exact positioning may change during layout. Maximum chip outlines are defined to make sure that the die fits the chosen package.

Block layout is the next stage. It is a major task to fit together individual blocks with all their mutual interconnect in the optimal way, particularly as there is some uncertainty as to the area of individual blocks. Chip planning is an interactive procedure which requires considerable designer insight, judgment, and skill. It is the essential difference between full-custom design and semi-custom chip planning and routing using heuristic algorithms. Routing is indeed the key to high density VLSI design.

Following block layout is the actual design, at the transistor level, of cells that do not already exist in a cell library for the specific technology. Also, existing cells may have to be reworked to fit the pinning or boundary constraints.

The crucial layout task is the assembly of all cells to produce the chip. Essentially it consists of connecting the active areas, but the large numbers of lines and

Workstation for interactive graphics design.

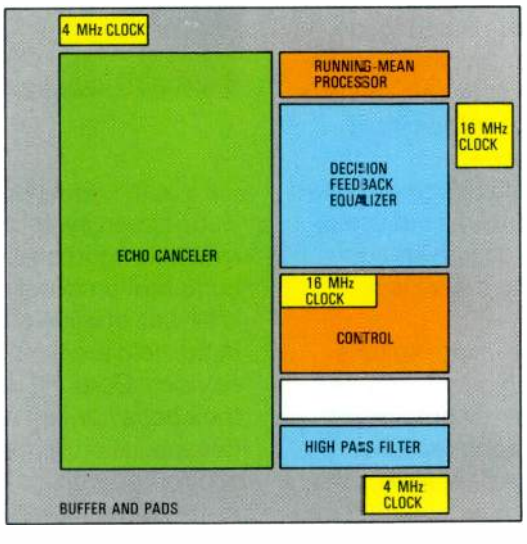


Figure 1
Example of layout methodology for chip planning.

the long interconnection lengths (on the micron scale) make it time consuming even when using computer layout aids.

Layout Verification

Various tools have been developed to detect *any* layout errors that remain after the layout stage. Layout rule verification programs check the correct implementation of the layout rules. Netlist verification programs then check that the layout is correct according to the circuit diagram. If these tools show zero errors on a 100% coverage (which is not always possible), there is a good chance that the chip will be functional, but they do not guarantee that it will operate in accordance with the specification. This can only be accomplished by tools that check electrical performance.

In digital circuits there are ways of checking critical timing performance which might be affected by the time constants of interconnect capacitance or resistance from polysilicon crossover. However, analog circuits are much more complicated to debug, especially if bandwidth limitations and breakdown voltages are important. It is necessary to take into account gate overlap, crossover capacitance, field inversion, layout-dependent device parameters, and so on. The toughest problems are caused by the inevitable parasitic effects, since they are not included in any design or diagram, or in any verification program. They are normally only detected during wafer analysis. However, they can generally be eliminated by skilled design personnel.

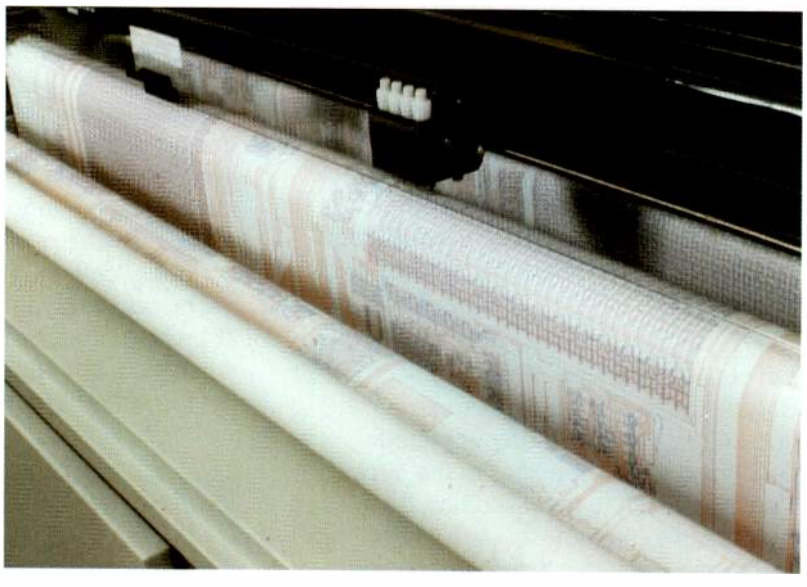
Phase 3: VLSI Analysis and Reliability

It is practically impossible to design a complex VLSI without introducing errors at some stage. They may be related to the concept, circuit layout, or technology. The fundamental problem in VLSI debugging is that the person with most of the circuit know-how – the designer – is psychologically the worst at finding his own errors. It is therefore worthwhile to use a group of engineers with design and technological expertise to debug less obvious chip errors.

VLSI analysis starts by using process validation module tests to check whether the technology was correctly processed, thereby giving some assurance to the technology-design interaction. Next, characterization by automatic test programs gives a good indication of the locations of less-obvious errors; major errors (such as power shorts and connection failures) are generally found at the wafer stage.

When the error zone has been located, real failure analysis can start using macro- and microscopic, visual, and electrical methods. More powerful fault-finding tools are being developed to cope with the problems which will occur as the scale of integration increases. Inevitably further integration and advanced technology and design techniques will introduce novel failure mechanisms. Although new automatic CAD (computer-aided design) tools will certainly improve the correctness of the design, they will not reduce parasitic faults.

One of the main challenges is reliability analysis. We stand at the advent of a period when only fundamental research leading to new analysis methods will allow us to make correct statements about failure mechanisms, infant mortality, and failure rate. At present reliability can only be specified in relative terms; chips are better or worse than a comparable reference. In view of the need for high reliability in all VLSI-based systems, accurate absolute reliability figures are essential. An added complication in defining reliability is that all analyses of failures from burn-in, life test, or in the field are based on encapsulated devices. Opening devices might change their behavior, but even assuming that decapsulation is not critical, one is confronted with a die which may have a history of multiple failures.



Final debugging on critical layout areas which cannot be found by the CAD tools is done by check plots.

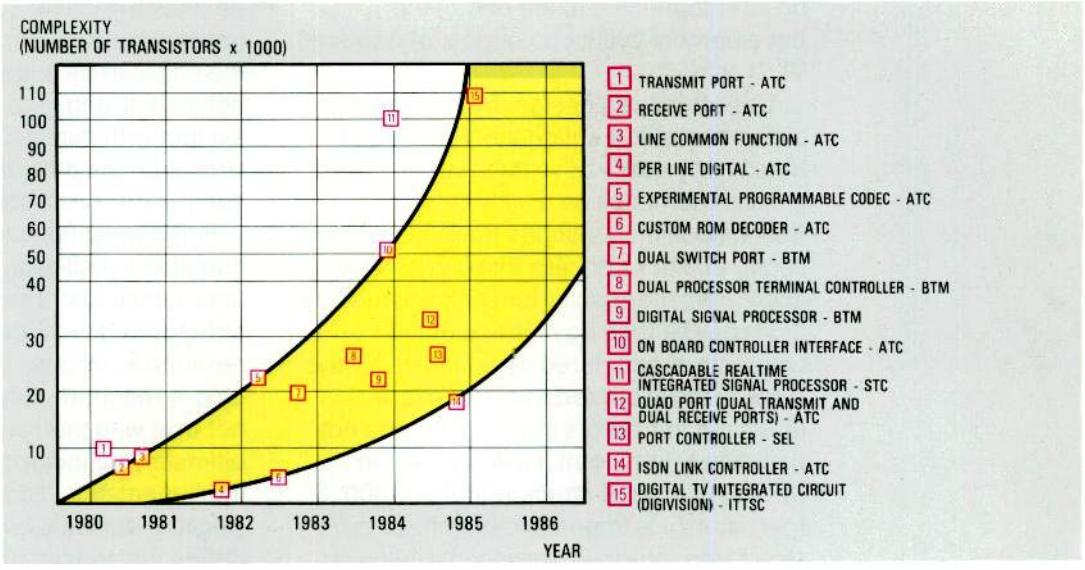


Figure 2
Evolution of VLSI and VLSI chip complexity.

It may be impossible to trace the original cause of a fault because it triggers further faults which lead to shorts, hot spots causing extra leakage, device performance changes, and potentially to fatal burn-out. In addition, characterizing the technology is difficult because most tools require the availability of wafers or big test structures. However, the introduction of scanning electron microscopy and laser-based equipment into the field of wafer analysis has resulted in a fundamental upgrade in the arsenal of tools for VLSI analysis.

Design Methodology Trends and Computer-Aided Design Tool Enhancements

Using modern design methodologies, digital VLSI circuits with 50000 transistors – about 17000 gates – can be designed. However, the problem is a great deal more difficult for more complex circuits. The drive towards higher density and complexity[5] is illustrated in Figure 2. Larger and more complex circuits are necessary to meet the sophisticated system requirements of ITT units worldwide.

The full custom design methodologies and tools in use today are hard-pressed to reduce the total labor required to complete a design, to reduce total development time, and ensure error-free designs. Many of today's development problems arise from the sheer number of logical elements and structures that must be handled in the course of a typical design. Some of the problems that become apparent as we go to larger and more complex VLSI chips are:

- deriving a correct chip architecture from a written specification
- managing increased design complexity
- coping with rapidly evolving semiconductor manufacturing processes
- achieving rapid and adequate logic simulation
- providing adequate device testability in the design
- achieving a sufficient level of design verification to eliminate errors.

Other problems include those of escalating computer run times, high design costs, long development cycles, and fabrication recycles resulting from corrections to design errors. Enhancements to the design methodology and improved CAD tools can reduce or eliminate these problems.

Structured Design

Structured design is being used increasingly in the development of VLSI circuits[6]. Design is done 'top-down', starting with a high level block diagram of the function to be implemented. Functional blocks are identified one-to-one with structural units which, in turn, correspond to a single contiguous area on the chip. The signals on any set of "connectors" at the boundary of a functional block are related by a clean functional description. In addition, the behavior of high-level blocks constructed from lower-level blocks can be precisely derived from the behaviors of the more primitive blocks. This allows a large VLSI circuit design to be divided into smaller, more manageable chunks that can

be interconnected at the end of the development cycle to produce the required VLSI chip.

This structured design methodology is based on implementing the VLSI circuit function by successive levels of functional block decomposition. Hierarchical decomposition continues until we reach a library of blocks or cells that can be used to implement the specific function and provide the required topology. The general concepts of structured design have always been partially utilized, but with a few thousand transistors in a circuit it was not particularly important. However, when dealing with VLSI structures of 100000 transistors it is imperative to enforce a structured top-down design discipline so that designers do not get lost in a maze of small interconnected functions.

Structured design encourages increased use of 'predesigned' lower-level elements from a library of blocks or from elements generated by small silicon compilers. This full custom design methodology is sometimes called "hybrid" or "pseudo-custom" design. Blocks take the form of random access and read-only memory, programmed logic arrays, finite state machines, function-specific registers, and so on. When viewed from afar, this VLSI system appears as a hierarchy of building blocks placed together to allow the system to perform the correct functions. Time is not spent on optimizing each individual block; the only interest is in the overall system performance. The top-down design approach, the use of elements from a block library, and silicon-compiler-generated elements should reduce development time, development labor, and error rates.

Functional Modeling

As VLSI systems become more complex, initial specification of the chip function becomes much more difficult. It is also difficult to proceed from a written specification to a VLSI chip implementation strategy. For these reasons it is important to use a more formal specification that succinctly conveys pertinent information. The future may see a behavioral language being used to specify the functions of a VLSI chip in a manner analogous to that being considered for software development[7]. In the beginning the behavioral language will simply permit animation of the specification, making it possible to see how it operates functionally, although not in "real time". Eventually it will be possible to link a behavioral language to general purpose silicon compilers so that the chip can be implemented from the behavioral language description of a VLSI system with minimal human interaction. However, the attainment of this level of automation is still some years away.

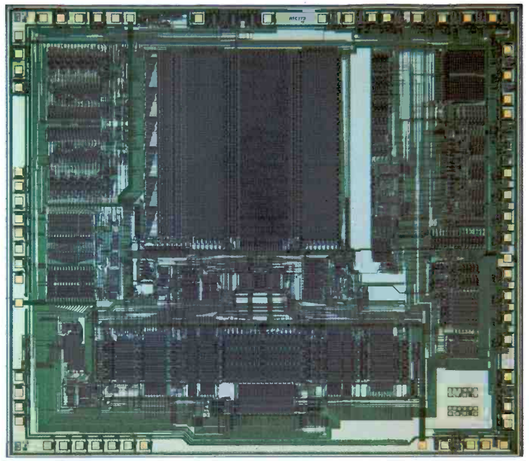
In the meantime, to ensure that the complex specification has been fully understood and the silicon implementation strategy and architecture will perform the required functions, a functional model of the chip is required. Functional modeling does not deal with the specific gates that will ultimately be incorporated into the circuit implementation. However, at a higher level (register-transfer level) it is possible to define the architecture and hierarchy of the chip as a group of functional models which, when connected together, produce the desired system performance. When the VLSI system has been modeled as functional blocks, the entire system can be simulated to determine whether the implementation of the attributes called out in the specification are correct. In fact, one advantage of functional simulation of a VLSI system is that it could be turned over to a potential customer for analysis and experimentation. The customer could help to develop test sequences that would fully exercise the functional model and determine whether it meets the system requirements.

An additional advantage of functional modeling is that each functional module can ultimately be replaced by its specific logical implementations. This gives rise to mixed mode simulation in which functional models of some parts of the system work with logical models of others. If the simulation output is still correct, it shows that the decomposition process was performed correctly. It also speeds up simulation (i.e. reduces computer run-times) because functional modules can be simulated much more rapidly than detailed logical models. Functional modeling capabilities exist on most present engineering workstations, and are being added to ITT's SIMLOG simulator.

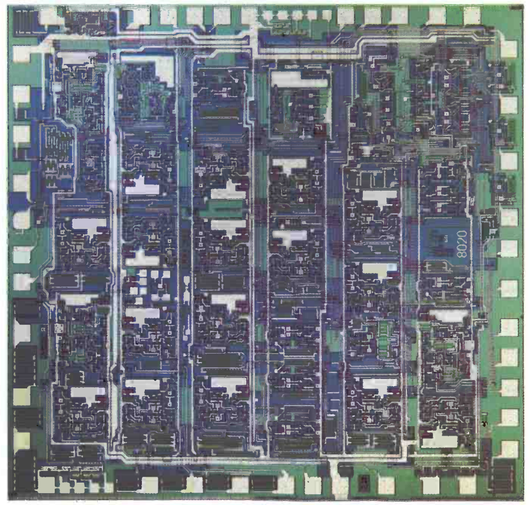
Schematics Capture and Neutral File Formats

Some of the older tools that are in use produce multiple design files which have to be checked to ensure that they agree. These data files include the circuit schematic, the netlist (table of circuit interconnect), and associated models

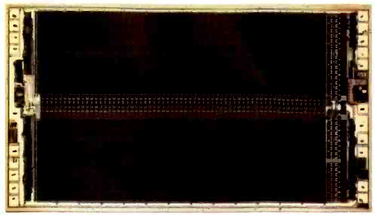
A selection of VLSI circuits designed and manufactured by ITT and affiliated companies. These illustrate the wide range of processing technologies available within ITT.



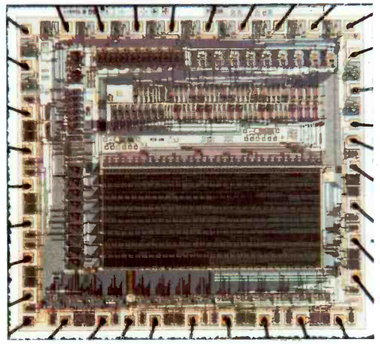
System 12 on-board controller interface for lines and trunks; 3 μm NMOS; 50000 transistors; 7.6 × 6.6 mm (ATC).



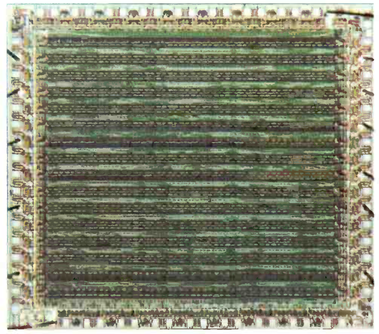
Subscriber DC loop controller; 30 V bipolar; 20 operational amplifiers, 7 comparators and logic; 5.2 × 5.4 mm (ATC).



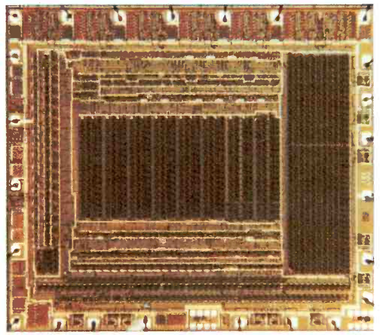
16 kbit static RAM; 3 μm NMOS; 103000 transistors; 3.4 × 6.0 mm (STC).



ROM decoder for 16-bit frequency control words; 5 μm CMOS; 4.1 × 4.6 mm (ATC).

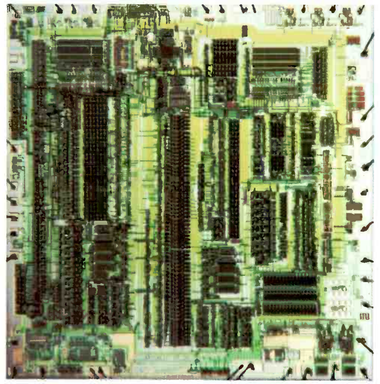


Programmable counter; 5 μm CMOS; 6000 transistors; 5.80 × 5.05 mm (AOD).

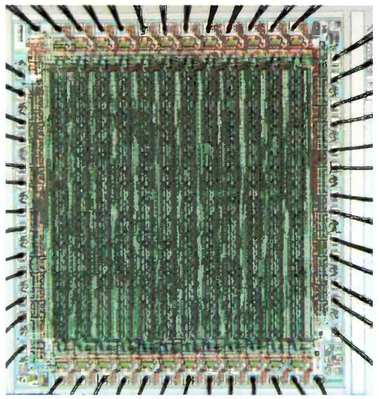


Dynamic shift register with reconfigurable taps; 5 μm ISO-CMOS; 11000 transistors; 4.7 × 5.3 mm (ATC/ITT-Raleigh).

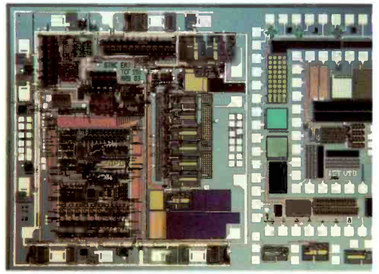
64 kbit dynamic RAM; 3 μm NMOS; 135000 transistors; 3.0 × 7.1 mm (STC).



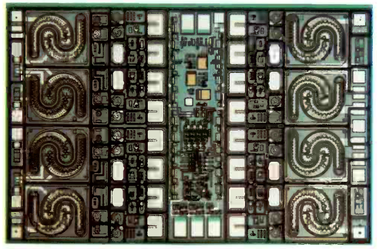
Programmable codec based on digital signal processing; 4 μm ISO-CMOS; 23000 transistors; 6.1 × 6.4 mm (ATC/ITT-Raleigh).



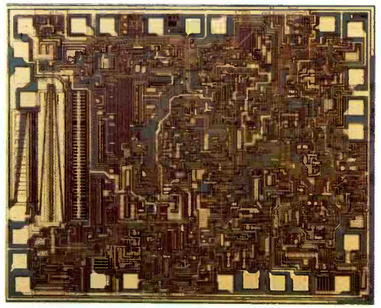
Control circuit; 5 μm CMOS; 4000 transistors; 4.5 × 4.0 mm (AOD).



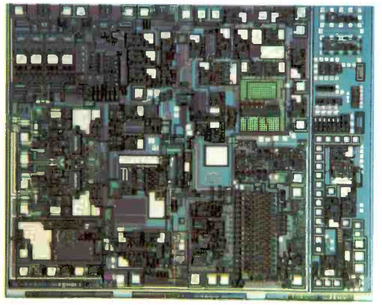
Linear to A-law/μ-law converter and remote metering for use in transcoder; 3 μm ISO-CMOS; 7000 transistors; 3.0 × 3.3 mm (BTM).



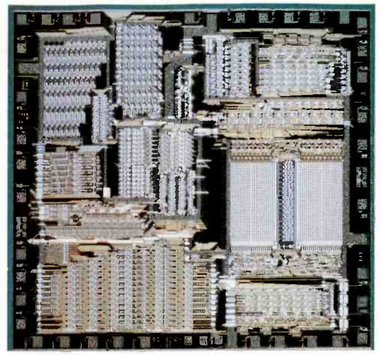
High voltage switch for ringing and test access; 300 V TRIMOS and 15 V CMOS; 24 transistors at 300 V and 200 transistors at 15 V; 4.23 × 2.75 mm (BTM).



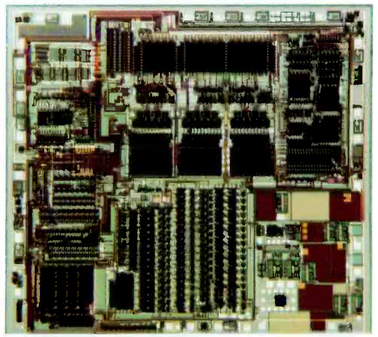
Line interface preamplifier; bipolar linear; 3.6 × 3.9 mm (STL).



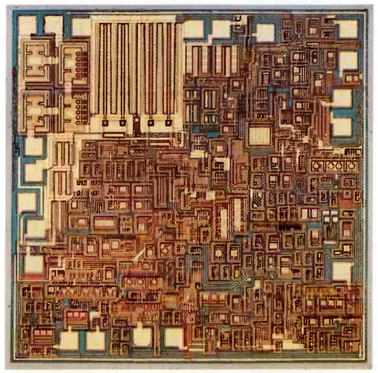
Line interface for transmit and receive functions; 70 V bipolar and 15 V CMOS; 600 transistors at 70 V and 1800 transistors at 15 V; 5.6 × 5.5 mm (BTM).



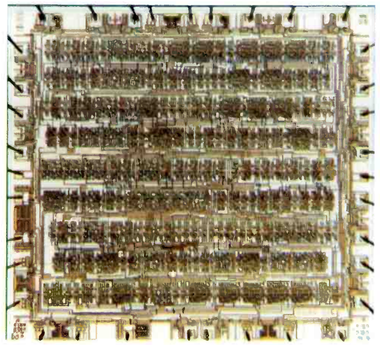
Programmable audio processor unit; 2.4 μm NMOS; 50000 transistors; 5 × 6 mm (ITT Semiconductors).



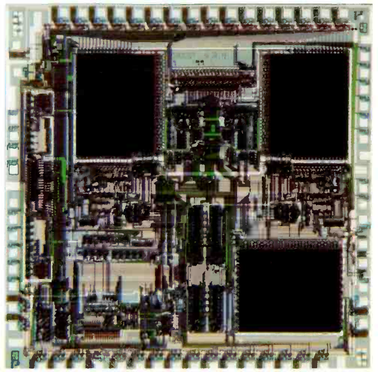
Digital codec; 3 μm ISO-CMOS; 22000 transistors; 5.80 × 5.30 mm (BTM).



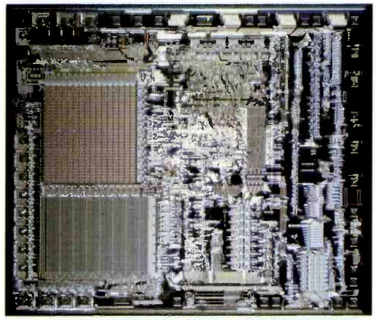
Tone ringer and loudspeaker amplifier; bipolar linear; 3 × 3 mm (STL).



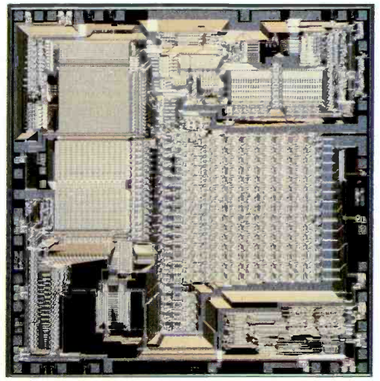
Bitplexer using digital signal processing; 7 μm CMOS metal gate; 4.95 × 4.50 mm (SESA).



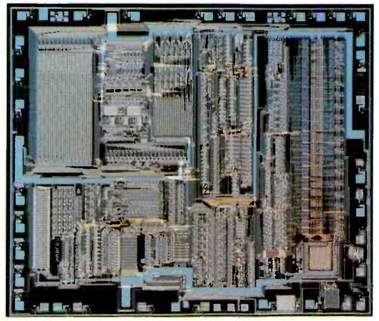
System 12 dual switch port; 3 μm NMOS; 20000 transistors; 6.08 × 6.16 mm (BTM).



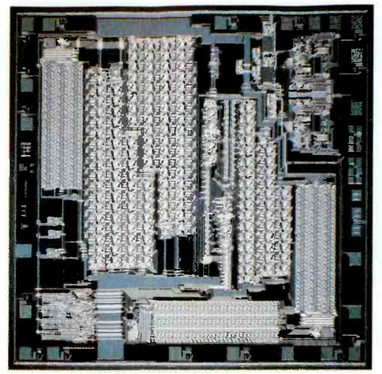
Eight-bit one-chip microcomputer with peripheral hardware; 2.4 μm NMOS; 50000 transistors; 5 × 6 mm (ITT Semiconductors).



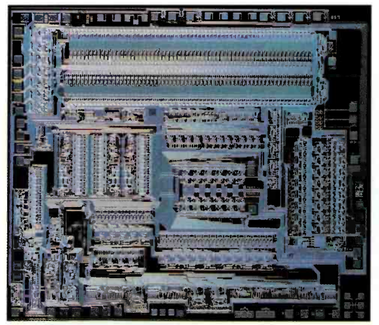
Digital video processor unit for Digivision; 2.4 μm NMOS; 50000 transistors; 5 × 6 mm (ITT Semiconductors).



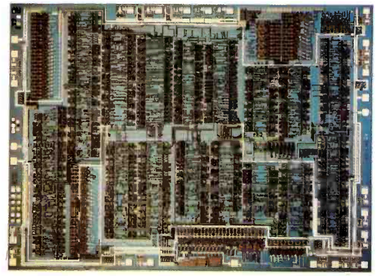
Two channel audio analog/digital converter; 2.4 μm NMOS; 50000 transistors; 5 × 6 mm (ITT Semiconductors).



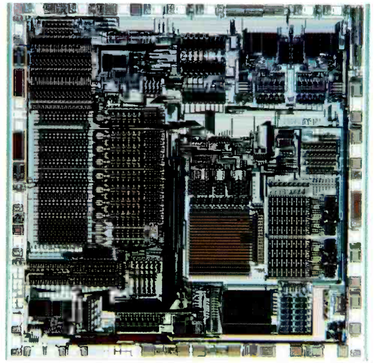
Programmable controller for TV receiver synchronization and deflection; 2.4 μm NMOS; 50000 transistors; 5 × 5 mm (ITT Semiconductors).



High speed coder/decoder for Digivision; triple diffused bipolar with collector isolation; 10000 transistors; 5 × 6 mm (ITT Semiconductors).

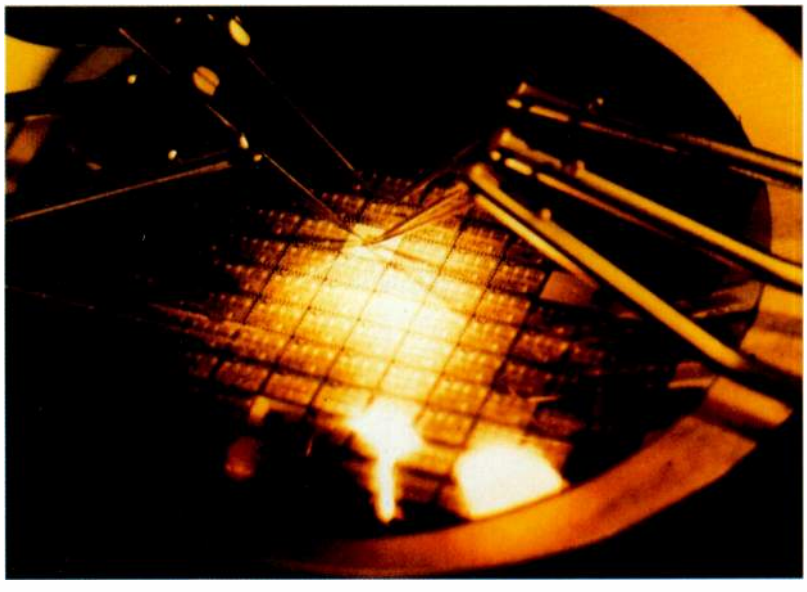


Voice level controlled attenuator; 5 μm ISO-CMOS; 7.0 × 4.9 mm (STL).



Dual processor terminal controller for System 12 line circuit; 3 μm ISO-CMOS; 23000 transistors; 5.96 × 6.02 mm (BTM).

(computer definitions of each circuit element) that define the logic simulation. They also contain associated models that define individual unique circuit simulations, chip topology, and various additional inputs needed for the design verification programs. A great deal of time and effort is spent in checking these design files against each other, and they are sources of errors. To unify and eliminate as many databases as possible, schematics capture on engineering workstations provides an opportunity to reduce the number of design files to two: the network description in *neutral network description format,* and the topology description in *neutral graphical description format.*



First wafer analysis is done at a probe station on process validation model inserts and on critical parts of the VLSI circuit.

The circuit schematic is entered onto the engineering workstation in a hierarchical fashion, and is in turn used to produce schematics and the netlist that is linked with the other tools in neutral network description format, eliminating the need for multiple data files. The graphical database, in neutral graphical description format, comes from automatic design tools or an interactive graphics system. Schematics capture enhances the use of hierarchy because it is impossible to show 10000 gates connected to each other on the normal video display unit. Designers are forced to use hierarchy in defining blocks and decomposing the blocks to the gate level. Therefore, schematics capture complements structured design and the extensive use of hierarchy. The engineering workstation also provides the capability for local simulation and timing verification of small modules to ensure that the elements being hooked up are consistent with respect to clock and signal timing.

Testability Analysis

Testability is an important, although sometimes neglected, aspect of VLSI development. It is not at all difficult to design a VLSI circuit that provides essentially the correct function but cannot be tested practically in a manufacturing environment, and is thus of no use to the system manufacturer. General testability issues are covered elsewhere in this issue[8]. However, it should be pointed out that ensuring adequate testability during logic design is an essential responsibility of the chip designer. Programs like the ITT testability analysis program[9] can help in determining controllability, observability, and the optimum positioning for test points.

The ITT simulator SIMLOG provides statistical test pattern verification. Using logic simulation vectors as the basis for developing test vectors, it is necessary to determine the degree of fault coverage that these test vectors provide. The higher the coverage, the greater the confidence that the test will in fact weed out defective chips at incoming inspection. Without statistical test pattern verification, the test pattern verification program would run for an inordinately long time and require enormous computer resources.

Symbolic Layout and Hierarchical Symbolic Layout

The more irregularly structured circuit cells are topologically designed today on an interactive graphics terminal with each structure being 'laid out' by the operator. A program currently being experimented with (CABBAGE) provides facilities for hierarchical symbolic layout. In this case the specific design rule-dependent structures are not input; rather the general configuration of elements and their rough topological relationship and interconnect are sketched out. The program is then able to, in effect, compile a process-dependent implementation with compaction in both the X and Y directions. Compaction is performed in accordance with design rules held in a separate file. If the rules change, the file is changed and compaction can be performed again. This approach allows a structure to shrink gracefully as semiconductor processes evolve. Futhermore, the hierarchical symbolic layout program allows a number of cells to be interconnected and compacted as a

large block, increasing designer efficiency, reducing errors, and producing blocks that are more independent of technology.

Chip Planner

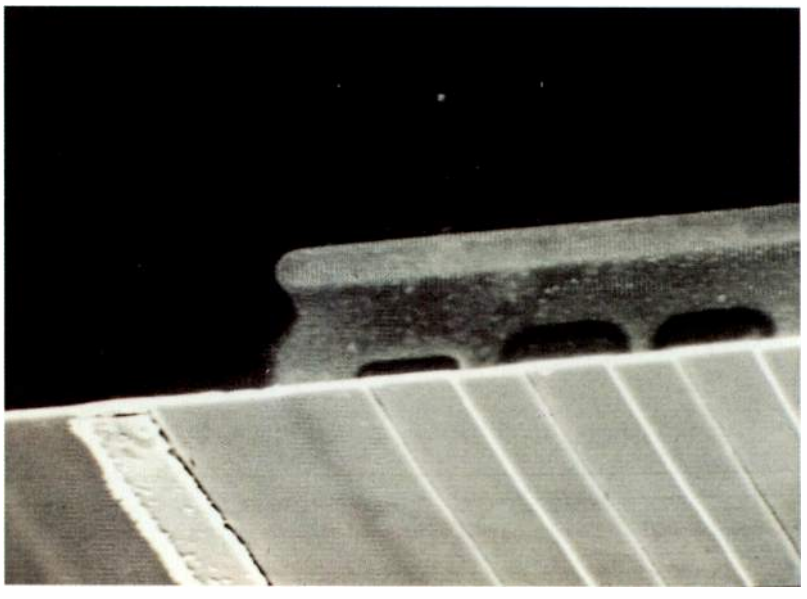
A hierarchical design facility – the chip planner – is being developed in ITT to provide designers with a graphical computer terminal for describing the large modules that go into the design of a full custom integrated circuit. Modules can have any shape made up of orthogonal lines; as the chip design evolves, their size and shape can also be changed. Using the neutral network description format logic description from schematics capture, the signal buses, power and ground planes, etc, are sketched into the topological plan to interconnect the modules. The chip planner provides congestion analysis to guide the designer in areas where additional space has to be allowed to achieve a better placement. The output of this program in neutral graphical description format feeds the block router.

Block Router and Silicon Compilers

ITT is developing a block router for automatically hooking up and placing blocks to design the final topology of a full custom circuit. Blocks are entered into the block router program using the neutral graphical description format. Initial block placement is based on information from the chip planner. The block router allows interactive routing and placement of critical paths and power lines, if required. It also automatically routes the remaining connections and verifies manually routed material based on netlist information received in neutral network description format. However, the router cannot rearrange or compact the layout – it can only route according to the netlist. If blocks are placed too close for routing, they must be moved apart manually so the router can do its job. This program also attempts to maximize the signal routing in metal so that the interconnect resistance of the polysilicon layer is minimized.

After the entire chip has been routed, parasitic capacitance information is back-annotated into the logic simulator database so that logic simulation and timing verification can be performed again using delay information derived from the actual chip topology.

Special purpose silicon compilers are being generated for the design of some very specific blocks, usually the more standard structures such as read-only memory, random access memory, and programmed logic array configurations. These compilers are used to control the overall configuration of this structure and compile based on a separate file that defines the design rules for a specific process. The programs also permit the contents of read-only memory and programmed logic arrays to be loaded automatically so that the contents of these blocks do not have to be specified manually. It is expected that more general-purpose silicon compilers, able to handle random logic and registers, will be available before the end of the decade. Until then, however, the more random blocks will be developed using hierarchical symbolic layout or interactive graphics design systems.



Scanning electron microscope analysis of cross sections is used to verify the VLSI technology.

Conclusions

Full custom VLSI design can provide a cost-effective system implementation with extraordinary reductions in weight, size, and power, while at the same time achieving the highest circuit performance and reliability for any given semiconductor process. The design methodology used in ITT is well suited to the design of chips with between 50000 and 100000 transistors. Various ITT laboratories are working on enhanced design methodologies and CAD tools that will make it possible some day to design structures that incorporate several hundred thousand transistors in an organized, efficient, and cost-effective way.

The opportunities for using these large VLSI structures are limited more by our imaginations than by the technologies that will be available in the coming years.

References

1 A. D. Close, L. Fisher, R. M. McDermott, T. A. Nix, D. M. Perrine, and J. M. Schoen: Design System for Semi-Custom VLSI: *Electrical Communication,* 1984, volume 58, no 4, pp 372–379 (this issue).

2 C. P. Lincoln: Design of a 3-micron CMOS Cell Library: *Electrical Communication,* 1984, volume 58, no 4, pp 384-388 (this issue).

3 E. L. Grant and W. G. Ireson: Principles of Engineering Economy: *Ronald Press Company,* New York, NY, pp 240–245, 4th edition.

4 R. F. Privett and P. Van Iseghem: Impact of Custom VLSI Technology: *Electrical Communication,* 1984, volume 58, no 4, pp 364-371 (this issue).

5 J. Cornu and M. Meinck: ITT 1240 Digital Exchange: Advanced Component Technology: *Electrical Communication,* 1981, volume 56, nos 2/3, pp 171–172.

6 C. Mead and L. Conway: Introduction to VLSI Systems: *Addison-Wesley Publishing Co,* Reading, MA, USA, October 1980, pp 88–90.

7 R. Balzer, T. Cheatham, and C. Green: Software Technology in the 1990's: Using a new Paradigm: *The Computer,* Institute of Electrical and Electronics Engineers, November 1983, pp 39–42.

8 G. W. Jacob: Designing for Testability: *Electrical Communication,* 1984, volume 58, no 4, pp 427–432 (this issue).

9 R. M. McDermott: ITT's Testability Analysis Program: *Electrical Communication,* 1984, volume 58, no 4, pp 433–439 (this issue).

Johan Danneels was born in Aalter in 1949. He graduated in electromechanical engineering from the Katholieke Universiteit Leuven, Belgium, in 1972 and received a PhD degree in applied sciences from the same university in 1976. He joined the BTM central laboratory in 1976 where he is now head of the microelectronics laboratory. In 1983 Dr Danneels obtained the degree of Master in Business Administration from Boston University in Brussels.

M. Meinck was awarded BS and MS degrees in electrical engineering from the Polytechnic Institute of New York. After a period designing analog circuits and digital logic he worked for General Instruments and then Singer on the development of custom LSI circuits. For the past eight years Mr Meinck has worked at the ATC managing the design of LSI chips, hybrid circuits, and printed boards for the System 12 development. He is at present director of product development engineering, supervising the development of semi-custom and full custom VLSI devices for a wide range of ITT products.

Experience in 3-micron Processing: a 10 Volt *n*-well CMOS Process

The advanced line circuit of System 12 demands high complexity, minimum power consumption, high performance, and high reliability of the integrated circuits. A 3 μm 10 V *n*-well CMOS process has been developed to produce the custom chips necessary in this system and offers a range of other possible applications.

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Introduction

A number of different processes have been used for the System 12 advanced line circuit: CMOS (complementary metal oxide semiconductor), NMOS (*n*-channel MOS), a high voltage process, and BIMOS (bipolar-MOS) technology. Small dimensions and critical design rules have been used for CMOS and NMOS processing to achieve a small chip area coupled with high manufacturing yield. In the course of this work a 10 V custom CMOS process has been developed to a stringent set of design rules.

CMOS technology with a minimum feature size of 3 μm was chosen for high device density, minimum power consumption, and high performance of the devices. The minimum size device has a 3 μm gate length, 3 μm width, and shallow junctions. Packing density has been enhanced with 7 μm metal pitch, 7 μm isolation pitch, 6 μm polysilicon pitch, 3 μm contact size, and three levels of interconnect: two layers of polysilicon and one of metal. The second polysilicon layer also forms the upper plate of a switched capacitor structure. The digital parts of the circuit use minimum size devices and are biased between 0 and 5 V. The analog circuitry uses a 5 μm gate length and can be biased between 0 and 10 V.

Further characteristics of this process are:

- modular approach to processing with existing technologies makes it easy to introduce special features such as polysilicon resistors, depletion devices, and buried contacts
- shrinkable to 2.4 μm
- expitaxial substrate can be used to suppress latch-up if the design is sensitive to latch-up.

Development

Figure 1 shows the main activities involved in process and device development. In development of the 3 μm processes, good dimensional control is needed. This is achieved by optimized isolation technology, photolithographic methods, and dry etching methods.

Optimized Isolation Technology

In normal recessed oxide isolation processing, the silicon surface is thermally oxidized and silicon nitride is deposited. The Si_3N_4/SiO_2 double layer is etched outside the active device regions, followed by field oxidation.

The fact that the thermal oxide under the silicon nitride is exposed at the periphery and that it does not prevent oxygen diffusion during the growth of the recessed oxide, will result in the so-called 'bird's head' and 'bird's beak' phenomena. The bird's head affects the surface topology and the bird's beak limits the packing density due to the slowly increasing oxide thickness at the field oxide edge. Both phenomena therefore limit the use of LOCOS (local oxidation of silicon) and isoplanar techniques for VLSI (very large scale integration) processing.

Boron ions, implanted in the field region to prevent parasitic channel formation, diffuse laterally during subsequent field oxidation. This diffused boron profile reduces the active device area and causes device performance degradation, such as

undesirable substrate bias effects. In order to minimize these effects, low temperature processing is needed. BTM (Bell Telephone Manufacturing Company) has optimized the LOCOS process for 3 μm MOS technology to minimize the limitations imposed by bird's beak, bird's head, and diffused boron profile on the packing density and high performance of its VLSI circuits for telecommunication. Optimization has made the LOCOS technique suitable for fabricating devices with polysilicon gate lengths down to 1.5 μm, and for low temperature processing.

At the beginning of the field oxide growth, oxygen diffuses laterally through the oxide under the nitride layer, the so-called pad oxide. This results in the formation of the bird's beak shown in Figure 2. A thinner pad oxide results in a shorter bird's beak. The length of the beak could also be minimized by using higher temperatures to keep the time of the surface controlled oxidation reaction short, but this approach is unfavorable for VLSI processing.

The influence of a native oxide as pad oxide has been evaluated. With a 2 nm thick native oxide, the bird's beak length has been found to depend on the nitride film thickness. For a thick silicon nitride film (200 nm) the nitride layer is not lifted up by the oxidation force, resulting in a transition region about 65% shorter than in conventional LOCOS processes.

However, the shape of the bird's beak can cause step coverage problems (Figure 2b). A thick layer of Si_3N_4 will introduce crystal defects in the silicon due to high intrinsic stresses in the silicon nitride. Reducing the nitride layer thickness lengthens the bird's beak and reduces the number of crystal defects. For nitrides between 30 and 90 nm thick, the bird's beak is shortened again and the silicon is dislocation free.

This bird's beak shortening reaches a minimum for a nitride layer of 30 nm. At the minimum the bird's beak length is more than 65% shorter than the conventional one, and the slope in the transition region is no longer a problem for step coverage owing to the lower rigidity of the thin nitride layer (Figure 2c). The thickness of the nitride layer corresponding with the minimum for the bird's beak length depends slightly on the field oxidation temperature. A nitride thinner than 20 nm is no longer sufficient to protect the active areas against field oxide growth at a temperature of 900°C.

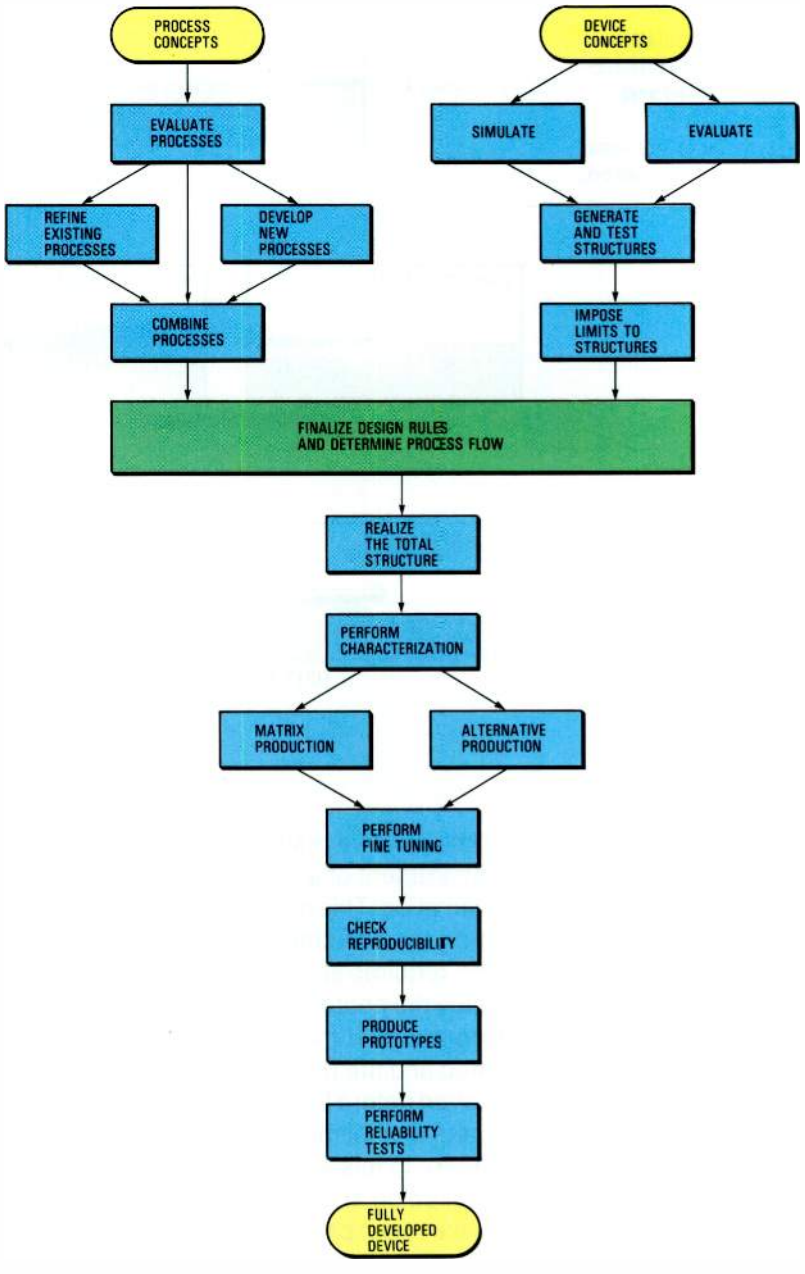

Figure 1
Flowchart of the main activities involved in process and device development.

With this optimized LOCOS technique a field oxide of 700 nm grown at 900°C results in a bird's beak of 0.3 μm, which is sufficient to process a 1.5 μm technology when normal scaling rules for such a process are taken into account.

Optimized Photolithographic Methods

Positive resist layers have a better photolithographic resolution than negative ones; BTM's 3 μm processing is done totally in positive resist. However, some drawbacks have had to be overcome.

Normal positive resist layers are not as resistant as negative resists to high dose implantation, an effect related to temperature. Deterioration of the photoactive component in the resist can form nitrogen under a hardened upper layer

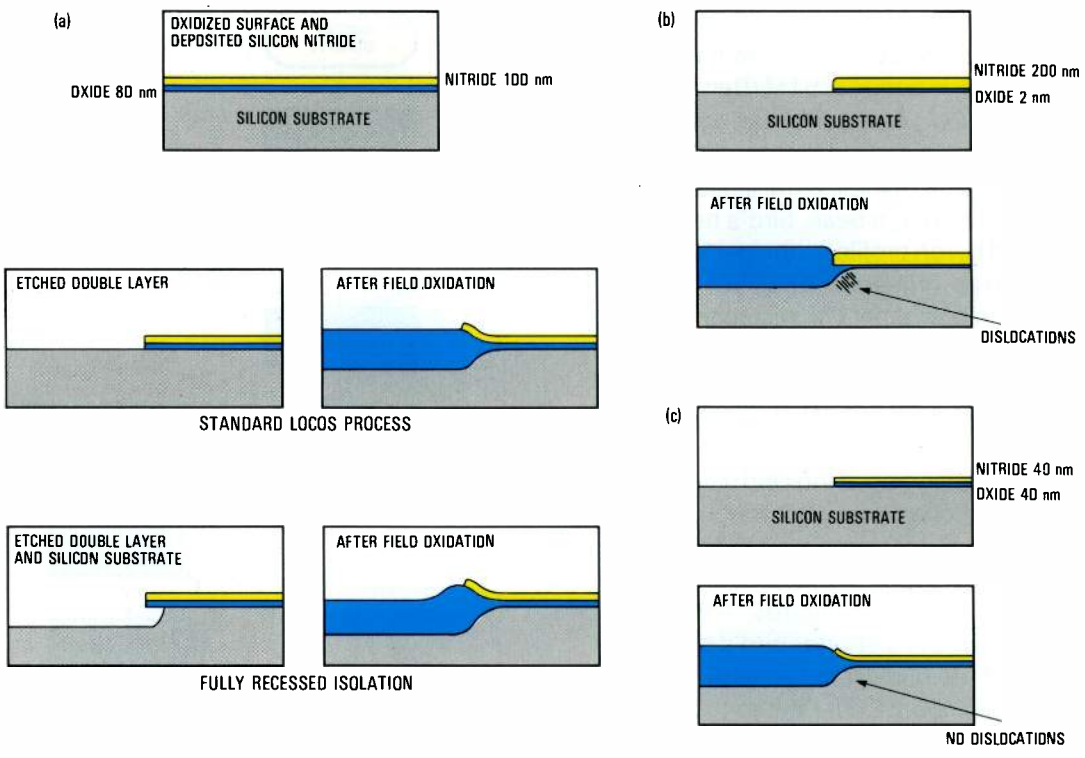

Figure 2
Optimized isolation technology. Formation of bird's head and beak showing (a) normal formations, (b) minimal formation, and (c) optimal formation.

and the positive resist layer cracks under bombardment of a high dose, high energy implantation. This problem can be solved by cooling the substrate during implantation, which requires special machinery, or by treating the photoresist before implantation. Using the latter method, the pattern is formed and the photoactive component removed before the hardened upper layer is formed, thus eliminating the formation of nitrogen. In this way high doses can be implanted on a well-defined and controlled positive resist pattern with high resolution.

A method has been developed to apply a second positive resist layer on top of an already patterned first positive resist layer, which is not normally possible. The second resist layer can also be patterned by another masking step, allowing self-aligned source and drain diffusions without counterdoping the polysilicon. The method uses plasma hardening and a high temperature treatment of the first resist layer and a clean, high temperature treatment of the second layer.

The positive resist layer has to be protected against dry etching, which occurs strongly in the reactive ion mode. Plasma treatment of the resist has been developed to make the resist more resistant to the dry etch method.

Optimized Etch Methods

Very dense structures and high complexity require close dimensional control at all stages of production, which is achieved by optimized photolithographic and etch methods (Figure 3) for all critical layers. Dry etch methods are used for nitride, polysilicon, oxide, and aluminum.

The dimension of the first polysilicon layer defines the gate length of the transistor, for which an anisotropic polysilicon etching method has been developed. This dry etching technique is optimized for high selectivity over the thin gate oxide and for precise dimensional control. Negative slopes on inside corners are not allowed on top of this polysilicon layer, which prevents shorts in the second polysilicon lines near the first polysilicon edge, and improves the step coverage of the following layers. The second polysilicon layer is etched isotropically to avoid over-etching and maintain dimensional accuracy. Both polysilicon etching methods have been developed in a parallel plate reactor with an SF_6/He gas mixture. They ensure very little dimensional loss and high oxide selectivity, so that etching will stop on the underlying thin gate or capacitor oxide.

The contact method is based on low temperature processing of the flow glass, a single contact mask, and dry etched contact holes. A key factor in this technology is the dry etched contact hole, with a positive slope to improve the step coverage of the aluminum layer, and a high selectivity over the silicon. This is done by developing a plasma in a parallel plate reactor with a CF_4/O_2 gas mixture. Optimized process

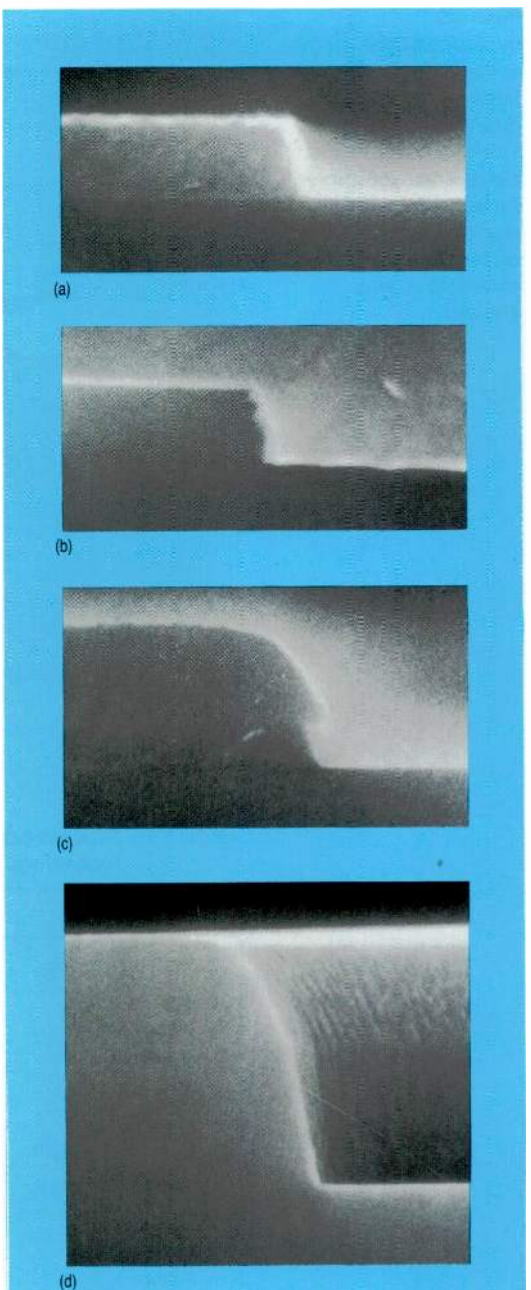

Figure 3
Optimized dry etch methods: (a) dry anisotropic polysilicon etching, (b) dry isotropic polysilicon etching, (c) dry aluminum etching, and (d) dry oxide etching.

conditions tune the process to a selectivity of over 20 to 1 and a positive slope of 70 for a 5 to 7% phosphorus-doped and flowed glass layer.

Dry etching of the aluminum layer is necessary to prevent undercutting of the thin aluminum lines. This method is based on the physics of chlorine plasmas and results in an (an)isotropic etched aluminum line with minimum undercut and high selectivity over the underlying oxide (7 to 1).

Optimized Switched Capacitor Technology

The 3 μm CMOS process uses a thin switch capacitor oxide for several applications, which requires high uniformity and breakdown strength. A switched capacitor technology has been developed with high capacitance ratio accuracy, low voltage and temperature coefficients, and minimum parasitic capacitances, achieved by tight process control of grain size and doping of the polysilicon, and an optimized oxidation technology.

Device development started with simulation of the different structures needed to optimize the various process parameters. Process parameters were characterized against device parameters using a variety of simulation models. Structures such as transistors, contact chains, resistors, and capacitors were also experimentally simulated by processing a matrix of all variations in the process and the dimensions. This showed the exact behavior of all devices under a variety of conditions. In this way electrical characteristics, limitations, and technological feasibility can be determined for a proposed structure. Indeed, ways of extending the limits of the technology can be found, such as the addition of anti-punchthrough layers, or the introduction of epitaxial layers to improve latch-up characteristics.

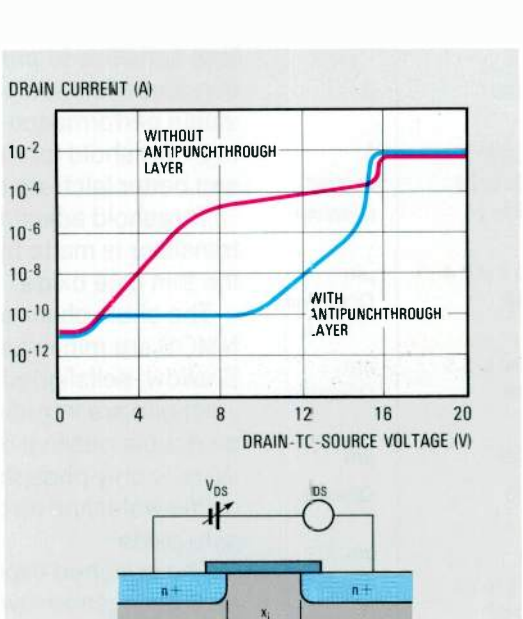

Figure 4
Influence of the anti-punchthrough layer.

The introduction of an anti-punchthrough layer suppresses the punchthrough condition of *n*-channel devices down to much smaller dimensions (Figure 4). The depth of the *n*-well junction is developed so that n^+ to p^+ spacing can be scaled towards 10 μm and the dimensions of the *p*-channel device reduced by at least 20% for the same working voltage.

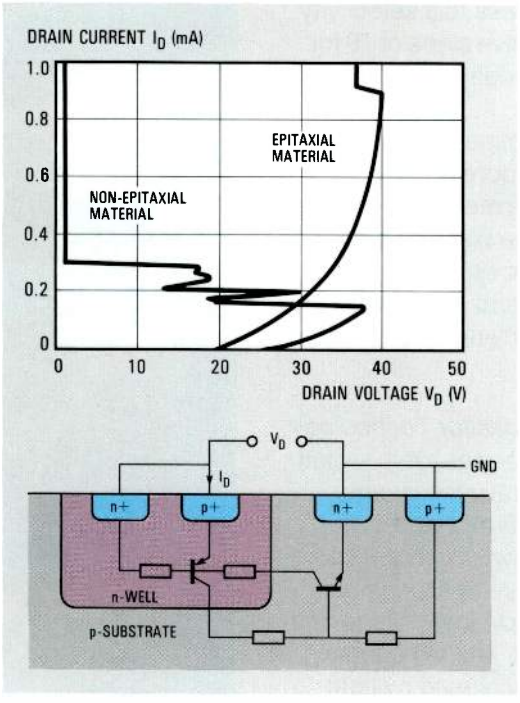

Figure 5
Influence of the epitaxial layer on latch-up characteristics. The graph shows the current-voltage curves for epitaxial and non-epitaxial materials. The latch-up structure is also shown.

Parasitic latch-up phenomena can occur in CMOS if the dimensions are scaled down. The *pnpn* structure provides for a potential latch-up condition, where lateral *pnp* and vertical *npn* transistors form a feedback loop when latch-up conditions are met (Figure 5). An epitaxial layer on top of a highly doped substrate reduces the current gain, and the holding current needed to sustain latch-up is increased. This holding current is now potentially greater than the power supply current and latch-up cannot be sustained. By using a modular approach, CMOS can be processed on epitaxial material without changing the processing, giving improved latch-up characteristics for high reliability.

If dimensions are scaled and the operating voltages are not scaled, undesirable effects occur which degrade the performance and reliability of devices. Hot carriers can be trapped in the gate oxide and result in threshold instability and transconductance degradation. Graded source and drain junctions can be introduced to reduce the peak electric field at the drain when scaling down devices.

Table 1 – Process parameters of 3 μm CMOS technology

Parameter	Value	Units
Substrate resistivity	35	Ω cm
n-well		
– well depth	4 to 4.5	μm
– sheet resistivity	1500 to 1800	Ω/square
Field		
– thickness	0.9	μm
– bird's beak length	0.6	μm
Gate oxide thickness	425	Å
Polysilicon 1		
– thickness	6000	Å
– slope	80 to 90	degrees
– sheet resistivity	20	Ω/square
Interlevel oxide thickness	800	Å
Polysilicon 2		
– thickness	5000	Å
– slope	60 to 70	degrees
– sheet resistivity	20	Ω/square
n^+ junction		
– junction depth	0.3 to 0.4	μm
– sheet resistivity	50	Ω/square
p^+ junction		
– junction depth	0.4 to 0.5	μm
– sheet resistivity	40	Ω/square
Passivation layer thickness	0.9	μm
Contact resistance	25	Ω/square
Metal		
– thickness	1.1	μm
– slope	60 to 70	degrees
– sheet resistivity	0.03	Ω/square
Passivation	0.5	μm

Processing

The 3 μm CMOS uses a shallow *n*-well technology which can be further shrunk to 2.4 μm. The *n*-well dose must be high enough so that only one field implant is necessary. This field implant is introduced by implanting boron on a double positive resist layer, or by a BF_2 implant. The threshold of the *p*-channel transistor is made by counterdoping the *n*-well with a boron implant. This makes the structure less sensitive to punchthrough. Well concentration and profile are optimized for stable performance of PMOS, sufficiently high threshold for the field oxide transistor, and better latch-up characteristics.

Threshold adjustment of the *n*-channel transistor is made by implantation through the thin gate oxide.

The short-channel effects in PMOS and NMOS are minimized by shallow junctions. Shallow, selfaligned source and drain junctions are introduced by implantations on double positive resist layers. As a result there is only phosphorus doped polysilicon on the wafer and no boron can enter the thin gate oxide.

The switched capacitor technology uses an 800 angstrom switched capacitor oxide between the first and second polysilicon layers and an isotropic dry etch process,

with high selectivity over the oxide, to etch the second polysilicon layer.

The contact method, based on low temperature processing of the flow glass, a single contact mask, and dry etched contacts, realizes excellent step coverage. The metal is dry etched to improve the uniformity of the width over the high steps in the double polysilicon process and for reproducibility reasons. Phosphorus-doped glass is used as a passivation layer.

Table 1 summarizes the process parameters. This high performance process uses a 425 angstrom gate oxide and a low body effect for the *n*-channel transistor, necessary for the analog designs. An annealing process is introduced to reduce the trap density in the thin gate oxide.

An 18 μm epitaxial layer grown on a highly doped *p*-substrate is used for improved latch-up characteristics. The thickness of the layer is optimized so that no boron diffusion from the p^+ substrate interferes with the *n*-well junction.

The anti-punchthrough layer is introduced as a low dose, high energy boron implant underneath the gate oxide and the source and drain junctions of the *n*-channel transistors. No additional masking step is required.

The graded source and drain junctions are introduced by using low dose phosphorus and high dose arsenic as source and drain implantations in the *n*-channel transistors.

Table 2 summarizes the typical device parameters for both *n*- and *p*-channel devices; the figures are given for non-epitaxial material without an anti-punchthrough layer. The transistor current-voltage characteristics are well behaved up to 13 V. No short-channel effects on the threshold voltage are seen up to 2.5 μm effective length. The length and width reductions are very small mainly because of the shallow junctions and optimized isolation technology.

Power dissipation in CMOS comes from diode leakage, subthreshold leakage of the active devices, and subthreshold leakage of the parasitic field MOSFETs. The process is optimized to minimize these leakage currents.

Introducing an anti-punchthrough layer raises the punchthrough voltage of a 3 μm *n*-channel device to above 15 V.

The same processing used on the epitaxial material improves the latch-up characteristics and does not significantly change the device parameters.

Products

The 3 μm CMOS process is used in the System 12 line circuit, a state-of-the-art subscriber line interface circuit which contains three custom integrated circuits per line and two integrated circuits per eight lines. Three devices are designed in this 10 V, 3 μm CMOS technology: the transcoder and filter, digital signal processor, and dual processor terminal controller.

The transcoder and filter is a complex mix of high density digital hardware and high performance analog circuitry with two main functions: a transcoding function, multiplexed for up to 32 channels every 125 ms, and the generation of click-free metering bursts (burst frequency is 2.5 Hz, metering frequency 12 or 16 kHz, and the output level of the signal is 7 V peak-to-peak). More than 2000 transistors are integrated in less than 9 mm^2.

Table 2 — Device parameters of 3 μm CMOS

	n-channel	*p*-channel	Units
Threshold	0.8 ± 0.2	0.8 ± 0.2	V
Length reduction	0.5 to 0.6	0.6 to 0.7	μm
Width reduction	0.2 to 0.4	0.2 to 0.4	μm
Gain	22 to 31	55 to 100	μA V^{-2}
Field threshold	17	18	V
Junction breakdown	19	19	V
Punchthrough voltage	13	17	V
Body effect	0.2	0.55	$V^{1/2}$
Subthreshold slope	0.9	0.09	V/decade
Subthreshold slope field oxide	1.2	0.7	V/decade
Bulk concentration	0.4×10^{15}	6×10^{15}	ions cm^{-3}

The dual processor terminal controller is a high density, high performance digital integrated circuit; only 5% of the area is analog, with more than 23 000 transistors integrated in about 36 mm^2. The chip uses 5 V CMOS technology and has an internal clock rate of 4 MHz. The circuit interfaces several line and trunk functions and two terminal control elements. It provides all required digital line and control functions and incorporates features to aid line circuit diagnostics.

The digital signal processor has 22 000 transistors on a 5.4 × 5.9 mm chip; 15% of the area is analog. The integrated circuit uses 10 V internally and a 2 MHz clock rate on most of the circuitry; 4 MHz is used on

certain parts. It provides the following functions:

- analog-digital conversion of the transmitted and received voice signals
- receive and transmit gain control
- echo cancellation
- interfacing between line side and switching side for control data
- metering signal synchronization control
- hit timing.

All chips are characterized by processing a matrix of electrical test results against the specifications. The results are used for the evaluation of product yield and further optimization of processing and device parameters.

Most of the chips processed in this technology have large areas and special attention must be paid to mask quality; enhanced control of the process conditions and the process environment is necessary for sufficiently high yields.

Conclusions

The CMOS technology developed for the System 12 line circuit achieves high density combined with high performance and enhanced reliability. Devices have been designed and tested with a minimum feature size of 3 μm, *n*-well double polysilicon construction, and 10 V operation; they are suitable for telecommunication and linear circuit applications.

Dirk Beernaert was born in Zwijnaarde, Belgium, in 1953. He graduated from the University of Ghent in physical engineering in 1976. After working for two years at the university in technical physics and statistics he joined BTM in 1979 where he has been engaged in the development of new MOS processes for telecommunication products. Mr Beernaert is currently in charge of a group dealing with VLSI MOS processing and will join Mietec as head of a technology-engineering group.

VLSI 1-micron MOS Processing

Close attention to substrate characteristics, isolation techniques, gate design, and interconnect methods are necessary to produce MOS devices with a feature size of 1 μm. Scaling rules must be taken into account in the development of new processes and enhancements to device structures.

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Introduction

Between 1971 and 1981 MOS (metal oxide semiconductor) technology advanced from 10 μm to 2.5 μm minimum feature size. Functional throughput rate, an indicator of process technology as well as system complexity, has increased with the advance in technology (Figure 1). Today's figure of merit of 0.5×10^{12} gate Hz cm^{-2} is expected to increase to 10^{13} gate Hz cm^{-2} by the late 1980s. The result of this progress has been the introduction of such advanced products as a photographic flash processing chip using 25 000 transistors, incorporating fast multipliers able to perform multiplication in 20 ns.

MOS device scaling theory offers a methodology for designing devices and processes for high-density, high-performance circuits. The procedure involves scaling down lateral and vertical dimensions and supply voltage by a scaling factor S of more than one, while increasing the substrate doping. Scaled devices have higher currents, lower capacitance, and a power-delay product that is reduced by the cube of the scaling factor. However, supply voltages have been kept at 5 V, thus ensuring transistor-transistor-logic compatibility, maintaining operating margins, and saving the effort required to establish new standards for circuit and board design. Table 1 shows the scaling laws that have been used to predict MOS performance as a function of scaling factor.

The non-scaling of voltages combined with the reduction in device lateral dimensions affects device characteristics in several ways because of the high fields. As device dimensions become smaller, an understanding of the effects caused by changes in both lateral and vertical dimensions becomes crucial in evaluating device parameters. The following are the most important mechanisms affecting small-geometry devices:

- velocity saturation (mobility degradation as a result of scatter limits)
- mobility degradation caused by the increasing perpendicular field (surface scatter limit)
- source/drain parasitic resistance and contact resistance (these effects can be modeled as effective transconductance degradation)
- finite inversion layer capacitance (effective electric field will be confined at the gate oxide and hence reduce transconductance)
- substrate current and hot-electron limitations (susceptibility to snapback and transconductance degradation, respectively)
- charge sharing under gate (reduction of threshold voltage).

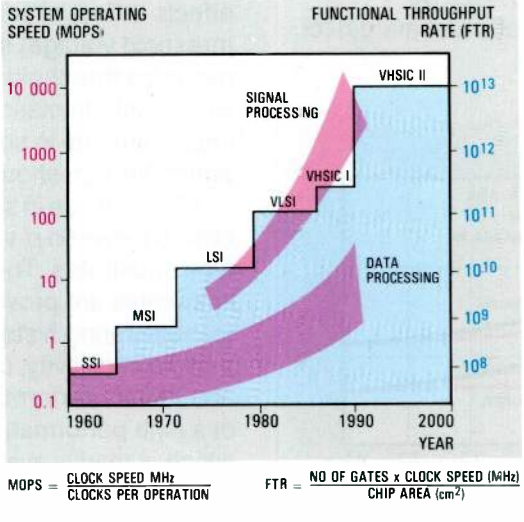


Figure 1
Functional throughput rate as technology advances from small and medium scale integration, through large and very large scale integration, to very high speed integrated circuits.

Table 1 — Three scaling laws for projecting MOS performance as a function of scaling factor

Parameter	Constant field scaling	Constant voltage scaling	Quasi-constant voltage scaling
Dimensions	$1/S$	$1/S$	$1/S$
Doping	S	S	S
Voltage	$1/S$	1	$S^{-½}$
Current	$1/S$	S	1
Power	$1/S^2$	S	$S^{-½}$
Current density	S	S^3	S^2

The scaling factor S is greater than one.

Figure 2 shows the effect of scaling on MOS transistor gain for *n*-channel and *p*-channel devices, assuming constant field scaling, constant voltage scaling, and realistic voltage scaling. Constant field scaling provides the highest gain.

The recent attention to CMOS (complementary MOS) technology and circuit techniques for mainstream devices has occurred for two reasons. First, a diverse set of circuit design requirements is being met by various CMOS capabilities. Second, the cost of processing CMOS is becoming comparable to that of NMOS (*n*-channel MOS) and bipolar technologies. The reduction of active power in CMOS circuits is probably the single most important reason for their use, especially as the power dissipation limit imposed upon commonly available packaging technology is only about one watt. Reliability problems caused by high temperatures, and migration caused by high current densities, can be dramatically reduced in low power CMOS devices.

Another advantage of CMOS technology over NMOS is ease of design. Commonly used "ratioed" NMOS circuits are designed using transistors with chosen lengths and widths to balance the current between transistors. This balance must be maintained to provide sufficient margin for process variations and changes in operating temperature, voltage, and load.

Flexibility in transistor geometry selection makes CMOS technology ideal for gate arrays and standard cell libraries. Fast CMOS devices can be designed using high-density dynamic logic circuits that are less complicated than comparable NMOS or PMOS (*p*-channel MOS) dynamic multiphase-clocking logic. VLSI CMOS circuits may use two to three times as many NMOS as PMOS transistors in the circuit design, and achieve packing densities comparable to NMOS circuits.

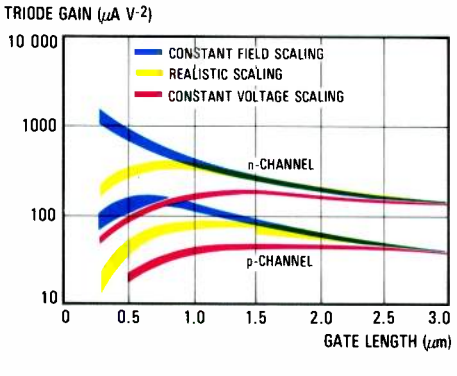


Figure 2
Triode gain of scaled MOSFETs versus patterned gate length for *n*-channel and *p*-channel devices assuming constant field scaling, constant voltage scaling, and realistic scaling.

Device Limitations

The process design of 1 μm minimum feature size MOS devices is governed by scaling rules, which make it necessary to evaluate such device fabrication and performance areas as silicon substrate, isolation, gate module and back-end module, employed during the process design.

Substrate

Both electrical and material characteristics are important to the selection of a substrate. The choice of substrate resistivity depends upon scaling requirements, lowering of junction capacitance, threshold voltage adjustment, suppression of latch-up in CMOS, and snapback in NMOS by better collection of substrate current. Well selection in CMOS depends upon lower well resistivity for latch-up improvement, well surface concentration for threshold adjustment, and well depth (which controls lateral diffusion of the well and hence imposes restrictions on the design rules). Junction capacitances in the well should be reduced to increase transistor speed, body effects (effect of substrate voltage bias on threshold voltage) should be controlled to minimize threshold voltage variations, and well substrate static leakage and improvements in source/drain junction punchthrough should be evaluated.

A major issue in substrate selection is the choice between *p*-well/*n*-type and *n*-well/*p*-type substrates. The advantages of *p*-well substrates are proven reliability and manufacturing history, reduced alpha particle sensitivity, closer match with NMOS and PMOS performance, and the existence of a high performance *npn* bipolar transistor which is readily available using the well structure (Figure 3). However, the *n*-well

process offers such advantages as compatibility with NMOS processes, better performance, reduced latch-up sensitivity, and the availability of a relatively low cost, good quality substrate. The recently introduced twin well process makes it possible to optimize both NMOS and PMOS transistors, although at the expense of increased process complexity and a less readily available substrate.

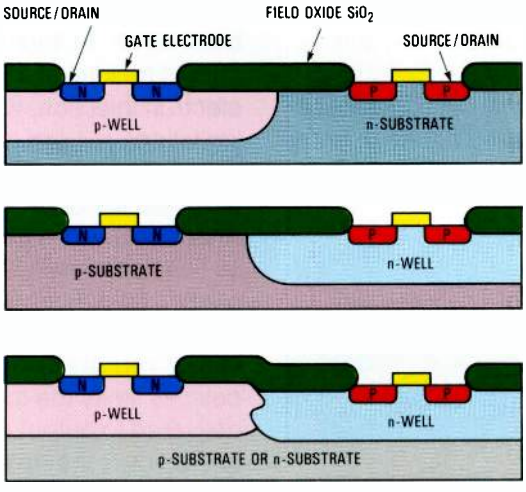


Figure 3
Cross sections of (a) *p*-well, (b) *n*-well, and (c) twin-well structures.

An advanced version of this technology reduces latch-up by using a high resistivity *p*-epitaxial layer on a p^+ substrate, or a high resistivity *n*-epitaxial layer on an n^+ substrate. The use of epitaxial and buried n^+ layers favors fabrication of high performance bipolar MOS devices which benefit from bipolar transconductance in sense amplifiers. The choice of well/substrate polarity depends on a complex set of interacting tradeoffs encountered during design. For high voltage applications, such as electrically programmable read-only memory and electrically erasable programmable read-only memory, *n*-well offers effective collection of substrate current. Similarly, fabrication of dynamic random access memory using a *p*-channel memory array on *n*-well CMOS technology takes advantage of negligible hot-electron shifts. In contrast, static random access memory favors the use of *p*-well and polysilicon load resistors. Logic devices may take equal advantage of both technologies.

The effect of defects in the silicon substrate must be taken into account. As device dimensions continue to shrink, yields can be affected by warpage of silicon causing: distortion of photolithographic superimpositions (resulting in shorts or closed contacts); resistivity changes generated by oxygen thermal donors (shifting threshold voltages of MOS transistors); excessive leakage current caused by degradation of the characteristics of a number of devices even if the leakage of each device is within the limit of tolerance; and functional failure caused by crystallographic defects. The generation of these defects depends upon the high temperature processing steps, the method of introducing and concentrating impurities in the silicon wafer, and the role of oxygen precipitation in producing stacking faults, dislocations, and thermal donors.

For example, thermal oxidation of silicon is known to promote the growth of stacking faults and dislocations. Mechanical damage, impurity centers, crystal growth defects, and ion implantation damage create stacking fault nuclei. It has been observed that steam oxidation produces more oxidation-induced stacking faults than are found with dry oxidation, which correlates with the higher oxidation rate in steam. For a specific process design, both device performance limitations and defect generation from the foregoing causes need to be considered.

Isolation

As device geometries are scaled down to the micron and submicron ranges, isolation technology is receiving more attention. Isolation technology should provide a defect free, planar surface, without an additional photomasking step. It should also be compatible with existing VLSI processing techniques. A suitable isolation technique should increase packing density (consuming less available active area), reduce the narrow channel effect (undesired variation of threshold voltage), minimize parasitic leakage caused by the field transistor ($n^+ - n^+$ or $p^+ - p^+$ separation rule), and decrease sidewall parasitic capacitance (to increase speed). Apparently no single technology can offer all of these performance enhancements, so the selection of an isolation technology depends upon device and circuit design limitations. Figure 4 summarizes various isolation technologies.

Conventional LOCOS (local oxidation of silicon) with self-aligned field threshold implant has become a standard technique for device isolation in MOS silicon gate technology. As device dimensions approach 1 μm, both geometric and performance limitations make it essential to

reconsider this choice. New processes such as sealed interface local oxidation, trench and backfill isolation, direct moat isolation, and sidewall masked isolation, have been identified as possible successors. The common problem with LOCOS is the formation of a "bird's beak" around the perimeter of the Si_3N_4 mask caused by the diffusion of oxygen and the growth of SiO_2 under the edges of Si_3N_4 film during thermal oxidation. This transition region reduces the available active area.

Sealed interface local oxidation is a simple modification of LOCOS. Oxygen diffusion under the edge of the Si_3N_4 is prevented by passivating the silicon surface with a thin layer of deposited nitride prior to formation of the usual Si_3N_4-SiO_2 bilayer.

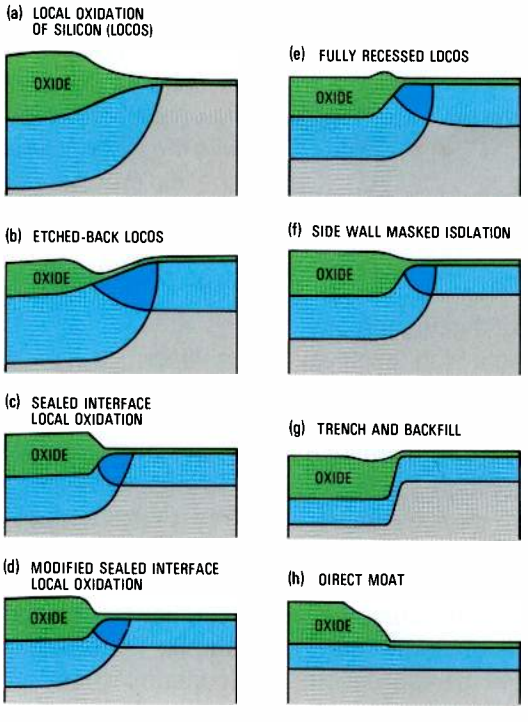


Figure 4
Cross sections of various isolation technology alternatives (a) LOCOS, (b) etched-back LOCOS, (c, d) sealed interface local oxidation, (e) fully recessed LOCOS, (f) sidewall masked isolation, (g) trench and backfill, and (h) direct moat.

In trench isolation, a slot is etched in the substrate and backfilled with oxide or polysilicon. Planarization is done by etch-back of the oxide or polysilicon.

In sidewall masked isolation, the use of Si_3N_4 frames to limit oxidation of nonrecessed-silicon areas produces a bird's-beak-free transition region. However, it is more complex than LOCOS. These recent technologies, which have still to mature, as yet only indicate possible future directions.

Gate Module

Gate module design requires optimization of such variables as threshold voltage, subthreshold current, punchthrough, body factor, source-drain junction capacitance, sheet resistance of junctions, short-channel effects, junction breakdown voltage, and hot-electron generation.

Scaling of device geometries to provide the required dimensions for 1 μm CMOS dictates a gate oxide thickness of 150 to 300 angstroms. However, this requires a detailed understanding of oxide properties such as hard-wired short defects (pinholes) and latent defect density (intrinsic quality of oxide), which is a time-dependent dielectric breakdown. In addition, the grown oxide should be immune to radiation and hot-electron injection, which are severe limitations at 1 μm geometries. Transistor gain increases as the dielectric thickness is reduced, although there is a diminishing return unless the power supply can be scaled to maintain a low normal surface electric field. For some applications the voltage may not be scaled, and channel carrier velocity saturation for short-channel devices limits the total current that can be delivered to output drivers or bus line drivers over the operating voltage range. Transconductance cannot be increased by reducing the channel length or dielectric thickness.

Hot-carrier injection is another point of concern during the design of micron- and submicron-geometry devices. The existence of a high electric field near the drain causes the substrate and gate currents to increase, thereby degrading the transconductance of the transistor and reducing long-term reliability. The hot-carrier effects are small enough in PMOS not to cause immediate concern. To alleviate high-field constraints, a self-aligned lightly doped drain transistor has been proposed. This is an important way of reducing punchthrough, increasing source-drain junction breakdown voltage, lowering substrate current, and reducing hot-electron injection. The concept of enhancing a lightly doped drain by double implantation is shown in Figure 5, where reduced n^+ concentration underneath the gate improves overlap capacitance, suppresses electron injection in the saturation region, and prevents threshold voltage roll-off of the MOS transistor.

Back-end Module

Interconnects already tend to dominate the chip area of certain VLSI logic circuits. For fine-line circuits, the additional resistance and capacitance introduced by

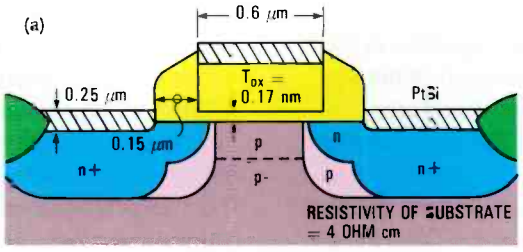
interconnections and contacts can significantly affect noise margins, output current drive capability, and the risetimes of critical signal paths. As the minimum feature size is made smaller, the cross-sectional area of interconnect is also reduced. At the same time, higher levels of integration allow the chip area to increase, causing interconnect to become longer.

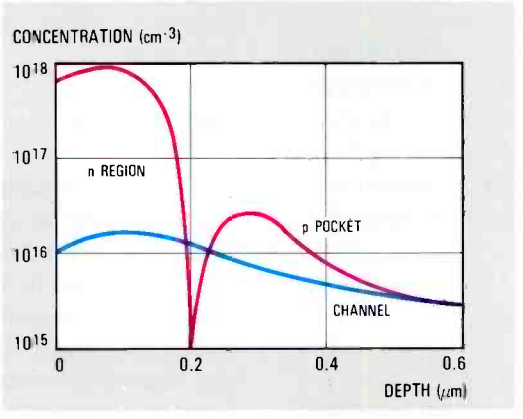
The net effect of this "scaling of interconnect" is an appreciable RC time delay. Figure 6 compares interconnect time delays (versus the chip area) with gate delays. For very large circuits even aluminum may not have a low enough resistivity. A multilevel interconnect scheme of aluminum or refractory metals offers significant advantages, including greater device density, shorter interconnect, and relaxed design rules, at the expense of introducing process complexities such as tapering and planarizing of structures by reactive ion etching, resist erosion etch, damage oxide etch, and low temperature flow of doped oxide.

An important question regarding multilevel metalization is the suppression of "hillocks" by adding metals such as copper into the aluminum film. Mixing copper and aluminum creates difficulties in dry etching of the fine lines; process complexity must be balanced by yield improvements as a result of reducing intermetal shorts caused by hillocks.

Another area of concern is the electromigration of interconnecting aluminum lines. Device scaling leads to increased current density in contacts and metal lines. Table 1 depicts the effect of various scaling laws on the power consumption and current density of the MOS transistor. The mean time to failure of aluminum lines is greatly affected by current density; the constant voltage scaling law will increase current density by the cube of the scaling factor, which is a major reliability concern. Moreover, if chip area is kept constant, chip temperature is bound to increase as device dimensions are decreased. Under worst case conditions the power per device will increase in line with the scaling factor, and for constant chip area the number of devices per chip will be increased as the square of the scaling factor. Hence chip power and junction temperature rise over ambient will be proportional to the cube of the scaling factor.

It has been shown that leakage failures resulting from silicon migration at the leading edge of the contact dominate under high current, high temperature conditions. Junction depth, contact width, and spacing to the diffusion edge strongly affect leakage





(b)

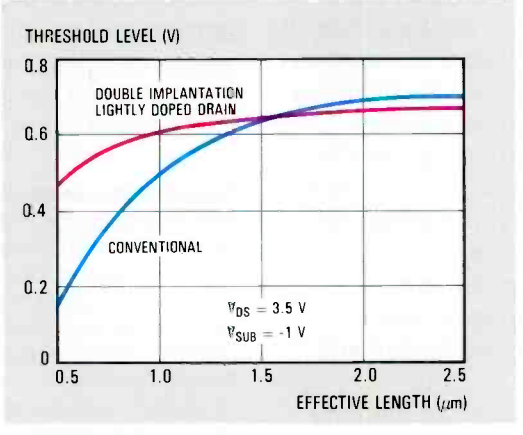


Figure 5
(a) Double implantation lightly doped drain cross section. All implants (n^+, n, p) are self-aligned to the gate. (b) V_t fall-off in fabricated conventional and double implantation lightly doped drain devices.

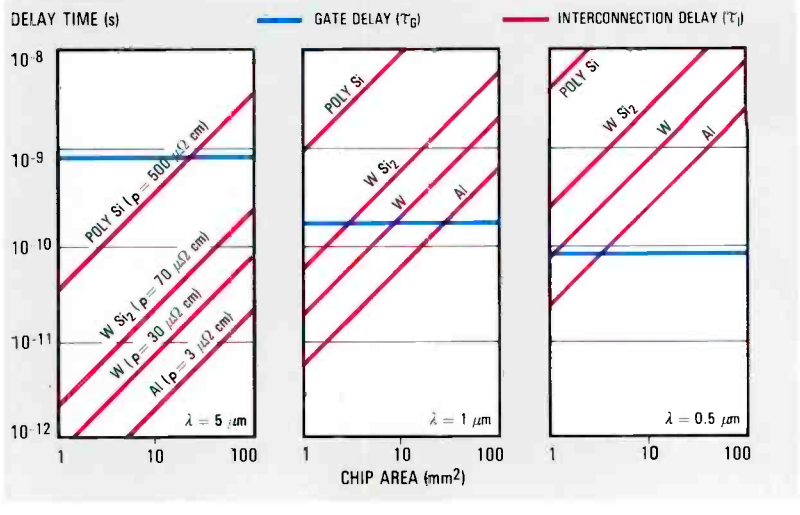


Figure 6
Interconnect time delay versus the chip area for heavily doped polysilicon, WSi_2, W, and Al for minimum feature sizes λ of 5 μm, 1 μm, and 0.5 μm.

failure rate. However, open metal failures resulting from aluminum migration at the edge of the contact have been observed under low current, low temperature conditions (for deep junctions). Aluminum step coverage controls the mean time to failure in this case. The use of a metal barrier (tungsten) eliminates leakage failures, as well as sensitivity to junction depth variations. In this case, aluminum electromigration at the edge of the contact becomes the dominant failure mechanism. Techniques such as Si/PtSi/W:Ti/Al and Si/PtSi/TiN/$TiAl_3$/Al have also proved effective in reducing silicon migration into an aluminum line, and hence at improving contact reliability.

Future Technologies

The industry has long sought an insulating substrate for silicon integrated circuits. Improvements in speed and power, and immunity to alpha particles can be achieved by fabricating MOS transistors on sapphire or SiO_2 insulating substrates. Sapphire is a rather costly substrate and has a poor silicon-sapphire interface. Silicon-on-SiO_2 takes advantage of the lower cost of silicon substrates with 0.5 to 0.1 μm of grown SiO_2. Conversion of deposited polysilicon to single crystal silicon is achieved by employing such techniques as laser, electron beam, graphite strip heater, and incandescent lamp.

Vertical stacking of transistors has long been the dream of integrated circuit manufacturers. Recently, employing a *p*-channel device on top of an *n*-channel device has resulted in an extremely dense static random access memory cell by eliminating the traditional *n*-channel/*p*-channel device isolation problem. However, two important issues regarding silicon-on-insulators should be addressed: the first is the complexity of interconnections in stacked transistors; the second is the removal of substrate current generated within the body of isolated transistors.

Conclusions

The process design of 1 μm minimum feature size MOS devices is governed by scaling rules which make it essential to evaluate device fabrication and performance areas such as the silicon substrate, isolation technique, gate module, and back-end module employed during the process design. A set of design rules for the fabrication of 1.25 μm CMOS circuits has been developed and documented. New process and structure enhancements as well as new physical models need to be considered for devices with geometries of 1.25 μm and below.

Farrokh Mohammadi received a BS degree in electrical engineering from the Technological University of Tehran, Iran, in 1975, and MS and PhD degrees from Stanford University, California, in 1976 and 1980, respectively. From 1978 to 1980 he was engaged in wafer process engineering of MOS and bipolar integrated circuits at Stanford University, then joined National Semiconductor where he coordinated an integrated circuit fabrication process for high-density MOS memory products. Until recently Dr Mohammadi was a key participant in the ITT Advanced Technology Center's 1 µm CMOS process development programme.

VLSI for the ISDN Line Termination

An important step in the evolution towards an integrated services digital network is development of the U-interface which provides a level *1* connection between the line terminations at the subscriber and exchange ends. Initially the U-interface for System 12 will consist of four VLSI chips, but as 1.5 μm technology becomes established these will be replaced by a single chip.

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Introduction

The System 12 Digital Exchange has been designed to facilitate the addition of ISDN (integrated services digital network) capabilities. This is possible because the distributed control architecture can accommodate any type of data or speech communication, as long as the bandwidth does not exceed that of the digital switching network. Already ITT units are well advanced in the development of hardware and software for the implementation of ISDN features on System 12 exchanges. Needless to say, this will greatly enhance its value to telecommunication administrations worldwide. In 1987 the German Bundespost will introduce ISDN commercially for many thousands of subscribers.

However, the implementation of an ISDN requires a considerable amount of signal processing because of its comprehensive features. As a result, no cost-effective solution can exist without the use of VLSI (very large scale integration) technology. Indeed, the evolution towards an ISDN will be one of the driving forces pushing both analog and digital signal processing beyond today's limitations in VLSI.

Impact of VLSI on the ISDN

Figure 1 illustrates the considerable impact that VLSI technology will have on a future ISDN. The reduction of electronic circuitry from, say, 30 printed boards, each with an average of 100 medium and large scale

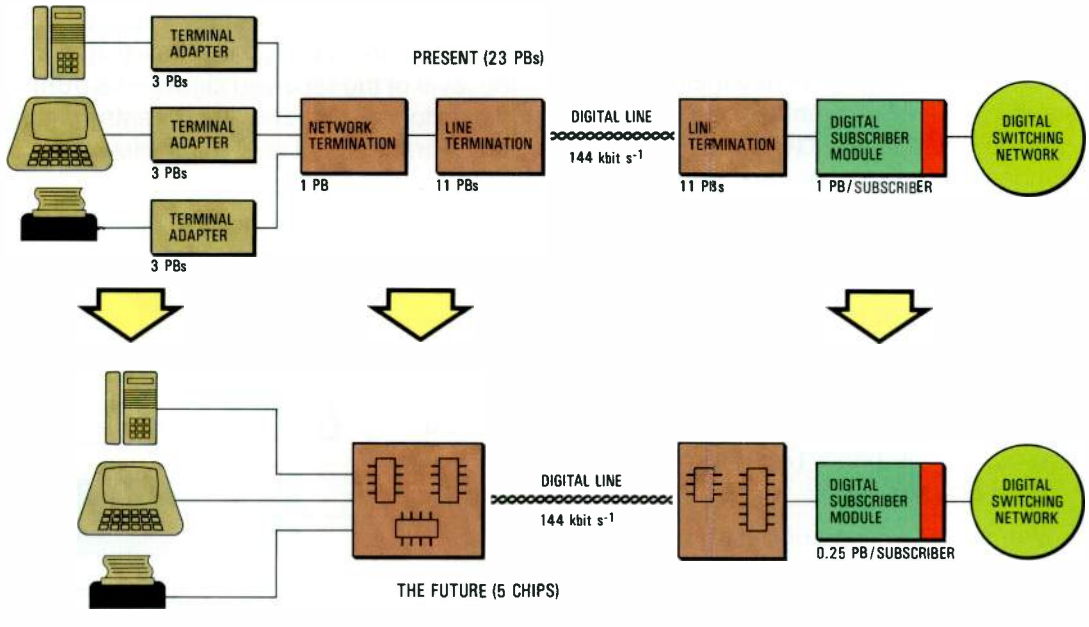

Figure 1
Impact of VLSI technology on the evolution towards an ISDN
***top:* present implementation using printed boards, and**
***bottom:* future implementation based on only five VLSI chips.**
PB - printed board.

integration devices, to perhaps five VLSI devices is essential to reduce size and power dissipation.

However, this engineering exercise is not simply a matter of integrating a few boards with small scale integration gates into one VLSI circuit. The total number of equivalent gates to be integrated is estimated at 30000. Moreover, some of the functions involve high speed and high resolution analog-to-digital conversion. All this is especially true in the line termination function.

Line Termination Requirements

The ISDN needs a full duplex, 144 kbit s^{-1} physical connection from one end to the other. Because the ISDN is being introduced into the existing telephone network, analog lines with a practical bandwidth of 4 kHz are initially being used for this connection. Thus in accordance with the OSI (open systems interconnection) concept, which defines different hierarchical levels of interfacing, the first objective is to realize a physical connection capable of transporting data reliably at this bit rate (Figure 2). Realizing a physical connection (or a connection at OSI level *1*) requires a transmission method, bit and frame synchronization, and activation and deactivation procedures.

The interface which realizes this level *1* connection between two line terminations (one at the exchange and one at the subscriber end) is known as the U-interface. Hence the line termination is called the UIC (U-interface circuit).

As the U-interface has not been standardized by CCITT, some administrations have defined their own standards. The first U-interface to be realized is that for the German Bundespost's ISDN field trial. It will have the following main characteristics:

- Information transfer at 144 kbit s^{-1} in three channels: *B1* for speech or data at 64 kbit s^{-1}, *B2* for data at 64 kbit s^{-1}, and *D* for low speed data and signaling at 16 kbit s^{-1}.
- Activation and deactivation procedures with a low frequency (7.5 kHz) carrier and level detector.
- Word and bit synchronization with inserted synchronization word (11 symbols).

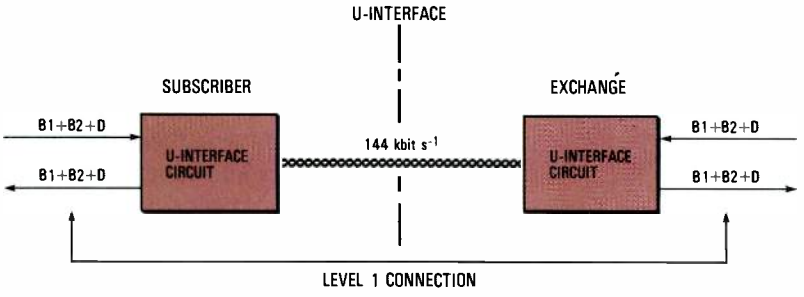

Figure 2
U-interface between the subscriber and exchange in an ISDN.

- 4B/3T-code, a ternary block code which converts a group of four bits into a group of three ternary symbols (−1, 0, 1).
- Scrambling.
- Remote feeding of at least one ordinary telephone set, which is of course a telephony standard.

U-Interface Circuit VLSI Device

To meet the requirements of the UIC, a transmission method was designed by Standard Elektrik Lorenz AG, Standard Telecommunication Laboratories Limited, and Bell Telephone Manufacturing Company using the results of simulations and hardware tests. Only the main features are outlined here[1].

The difficulty mainly arises from the need to use existing telephone lines for sending data at 144 kbit s^{-1} in full duplex from one end to the other. In fact the UIC is a two-wire full duplex modem for 144 kbit s^{-1}. Several problems (Figure 3) had to be overcome in designing the circuit. Because the 2-/4-wire conversion is done by an analog hybrid, an important part of the signal which is to be transmitted to the far end is also reinjected into the receive path. In the worst case (i.e. long lines) the level of echo is −6 dBm and the level of the received signal −46 dBm. That is to say, the ratio of the wanted signal to unwanted signal is −40 dB. However, to

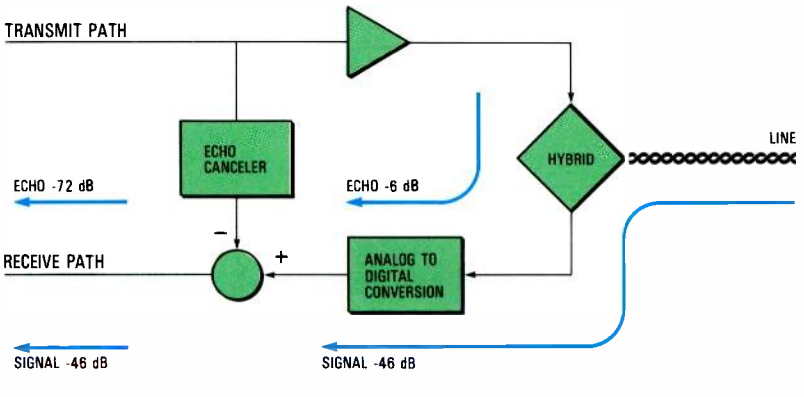

Figure 3
Problems of 2-/4-wire conversion and line attenuation in the ISDN line termination.

be able to receive data with the specified bit error rate of 10^{-6} requires a signal-to-noise ratio of 26 dB. Thus a first problem was to reduce the unwanted signal by more than 66 dB. This was achieved by using a 50-tap transversal adaptive echo simulator with a digital summation point to remove echo in the receive path.

- adaptive transversal decision feedback equalization
- transversal correlation
- other calculations.

Because of the stringent requirements on the UIC, a vast amount of digital signal processing is required, as shown in Table 1.

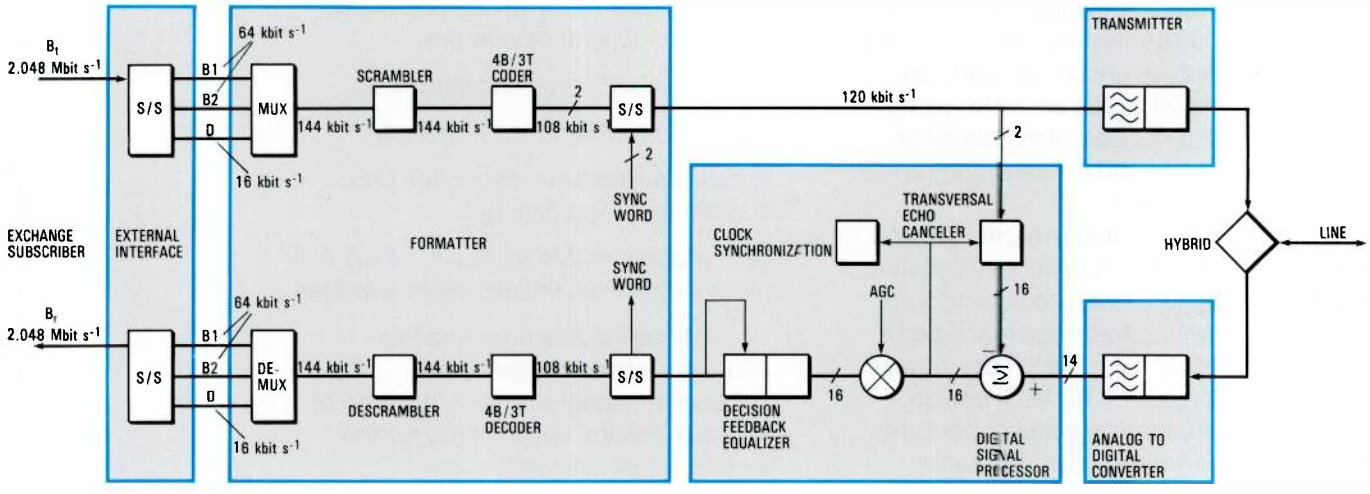

Figure 4
Block schematic of the System 12 UIC.
AGC - automatic gain control
S/S - serial-to-serial converter.

On the other hand, the far end signal is attenuated and intersymbol interference is generated by group delay distortion on the telephone line. An adaptive decision feedback equalizer has been incorporated to equalize the far end signal, and a 4B/3T coding scheme used to lower the bandwidth on the line.

Finally, timing information has to be transmitted from one end to the other. Bit and frame synchronization are achieved by transmitting a synchronization word from one end to the other where a digital correlation phase locked loop is applied.

Figure 4 is a functional block diagram of the UIC. The circuit is divided into five building blocks: external interface, formatter, digital signal processor, transmitter, and analog-digital converter.

New Architecture for Digital Signal Processors

The digital signal processor has to perform the following functions:

- adaptive transversal echo cancelation
- adaptive transversal precursor equalization

All this processing has to be done in one symbol cycle of 120 kHz and, because the maximum clock available is 15.36 MHz, only 128 timeslots are available.

To realize the required functions with commercially available digital signal processing chips, about 10 chips would be required. Therefore a chip architecture had to be found which is closely adapted to the characteristics of the application. Almost all processing can be reduced to the calculation of an inner product (the result of the summation of a first operand with a second operand formed by multiplication): for example, transversal filter processing can be divided into consecutive additions of inner products:

$$E_T(i) = \sum_{k=o}^{n} C_k T(i-k) \quad : \text{transversal filter}$$

or

$$E_T^o(i) = C_o T i$$

$$E_T^1(i) = E_T^o(i) + C_1 T(i-1) \quad : \text{recurrence}$$

$$\vdots$$

$$E_T^j(i) = E_T^{j-1}(i) + C_j T(i-j) \quad \text{expressions for transversal filter}$$

$$\vdots$$

$$E_T^n(i) = E_T^{n-1}(i) + C_n T(i-n)$$

Table 1 – UIC signal processing requirements

50 times	32-bit addition
150 times	16-bit addition
190 times	2 × 16-bit multiplication
5 times	16 × 16 bit multiplication

The required signal processing is very regular, a feature that was used in designing the UIC digital signal processor.

It is impossible to develop a VLSI circuit with, say, 50000 transistors, one device at a time. Only a regular layout structure can make such a VLSI circuit possible; using this approach, a key part of the circuit is designed just once and re-used many times wherever it is needed.

Bearing this VLSI design technique and the regular algorithm in mind, two possible methods of digital signal processing were studied: a bus-structured approach and a serial systolic approach. Both have regular structures, as required for VLSI design.

The bus-structured processor performs all calculations serially using the same processing element, so that each bit of a word is processed in the same way; there is thus concurrency in space and distribution in time. In contrast, in the systolic approach the filter is partitioned into 50 equal cells for the 50 filter taps; all calculations are performed at the same time but distributed in space, giving distribution in space and concurrency in time.

Bus-structured Processor

To cover all functions the bus-structured processor consists of two closely coupled Von Neumann-like processors each working at the maximum possible bus cycle frequency (Figure 5). The characteristics from the user's point of view are:

- two 32-bit arithmetic and logic units
- dual port random access memory
- three-bus structure: instruction bus, address bus, and data bus
- user programmable microcode read-only memory in which the algorithm is written
- instructions include one- and two-address instructions: addition, subtraction, addition and subtraction of absolute values, add-multiply for the inner product calculation, and multiplication
- immediate, direct, and indexed addressing modes
- throughput of 15.36 million instructions per second

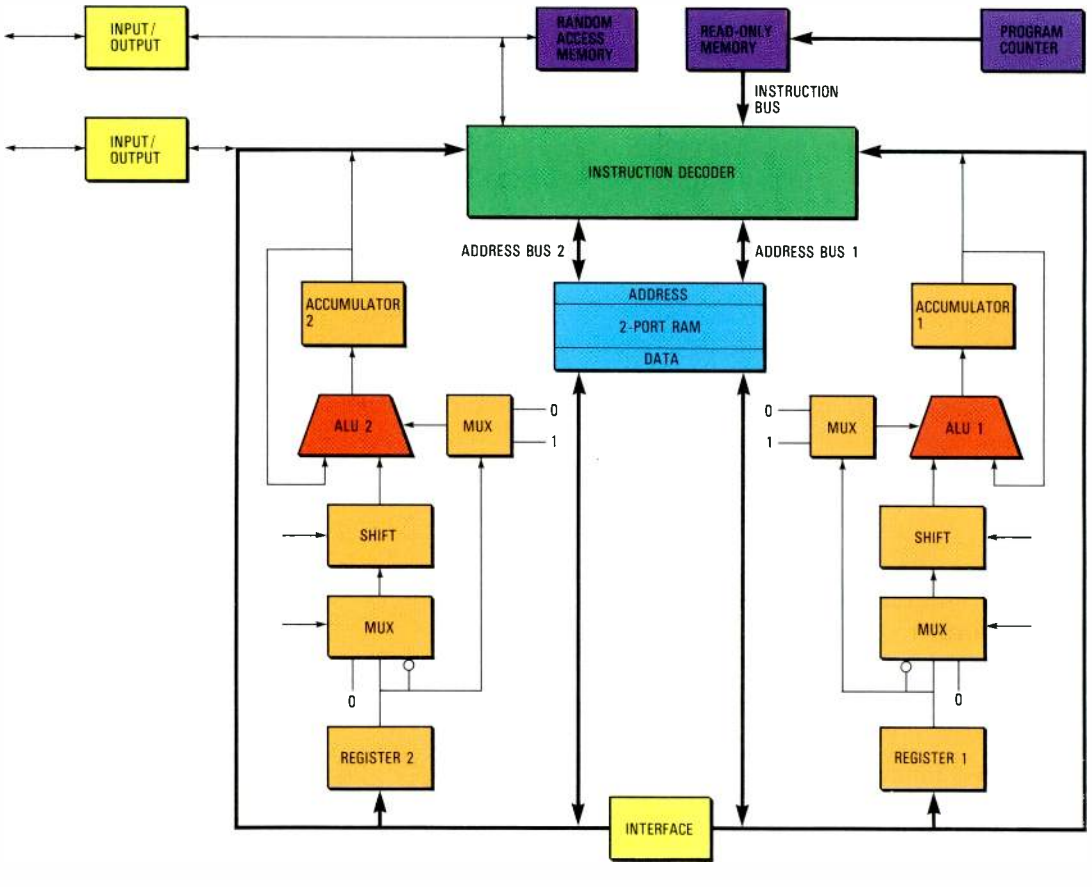

Figure 5
Block schematic of a bus-structured processor.
ALU - arithmetic and logic unit
MUX - multiplexer.

– computer-aided design tools for generating the read-only memory contents (microcode).

The main design characteristics are:

– 15.36 MHz clock rate

– design based on the principle of a crosswise data path and control path as commonly used in microprocessors

– pipelining in control and data paths

– clock and control signals centrally generated and distributed over the chip, giving a lot of communication and interconnection

– microcode test program can be included in the read-only memory.

After the system concept (i.e. instruction set, data path, overall timing, etc) has been fixed, the layout methodology starts with the construction of a chip plan based on the building blocks: read-only and random access memory, data path, controller, address decoder, and instruction decoder. The building blocks are then designed within the constraints of the chip plan so that the regularity of the design is reflected in the regularity of the building blocks. A drawback of this approach is that because there are only two levels of interconnection (polysilicon and metal), a fair amount of chip area and design time are required to achieve a good routing scheme. However, by setting up a detailed chip plan much of the interconnect routing can be forecast and included in the cells, so that when the cells are placed next to each other (abutted) the interconnections are made automatically. Even when this abutment technique is used there will be a need for buses running over the chip.

Serial Systolic Processor

This processor is based on the systolic principle as described by Kung[2]. The word systolic is derived from the medical world. In the systolic processor data is pumped by a clock through the cells while being processed. The principle is shown in Figure 6 for a three-tap transversal digital filter. The functional block diagram is simply mapped on silicon. One cell is used for each tap, and each cell calculates the basic inner product. As shown in the space-time diagram (Figure 6b), while *Ti* flows from cell C*0* to C*2* the inner product *TiCi* is calculated, and while these inner products

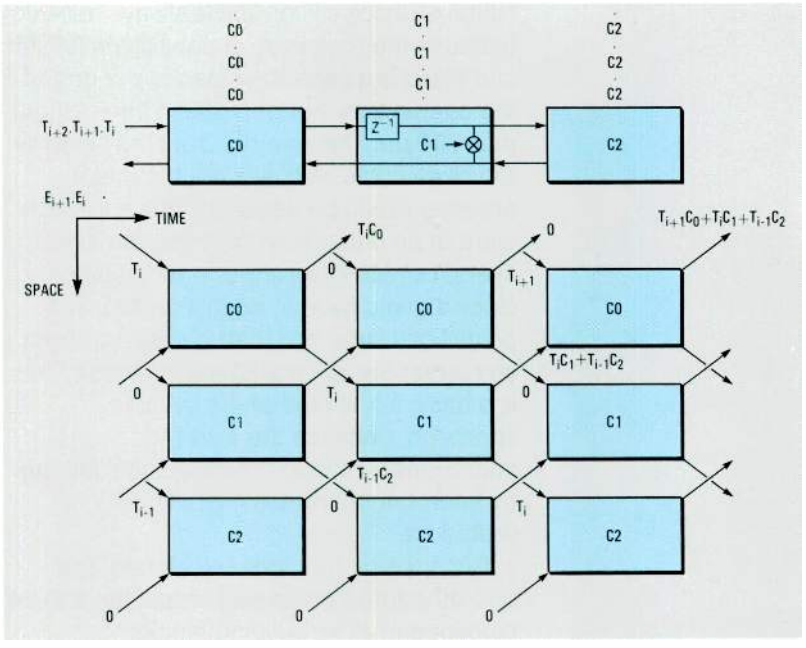

Figure 6
Principle of serial systolic processing.

flow from cell C*2* to C*0* they are accumulated resulting in the filter output at cell C*0*.

The main characteristics from a user point of view are:

– fixed algorithm defined by the cell hardware

– basic cell which performs 32-bit inner products.

From a design point of view the characteristics are:

– 4 MHz clock rate

– only clock signals and power are distributed over the chip

– only local interconnection and communication

– cell design

– little additional hardware is required to implement serial testing.

Choice of Processor

It was decided to use the serial systolic approach for digital signal processing in the UIC for the following reasons.

The clock rate of 15.36 MHz for the bus-structured processor poses severe problems using standard 3 μm *n*-well, double polysilicon, single metal CMOS technology. Clock and control distribution is impossible at 15.36 MHz with only one metal layer. Polysilicon can only be used for local interconnection because of its delay. A

Sigma-delta modulator.

signal on a polysilicon line is always delayed because the resistivity of polysilicon is high and there is a capacitive load at the end of the connection. For polysilicon lines longer than 500 μm, the delay is about the same as the clock cycle. A costly double metal process would be needed if this approach were to be chosen. In contrast, the serial systolic processor runs at 4 MHz and only clock signals have to be distributed. The polysilicon layer can then be used without any problems for local interconnection. This is a basic advantage of the systolic approach, because the area for interconnection and the delays introduced by interconnection are major VLSI problems.

Because of the higher clock rate, the bus-structured processor would have to be pipelined in all its building blocks: instruction fetching, instruction decoding, control path, data path, and data fetching and storage. This overall pipelining makes it necessary to have a global overview of the total digital signal processing. Essentially the complexity of the design is decided at the chip level since it is not easy to divide the problem of chip design into partial problems.

For the serial systolic processor the situation is much easier. Once the systolic concept has been defined, design of the total processor only requires one cell to be defined, which is far less complex than a chip.

Another advantage is related to present VLSI design practice. Functional verification of the bus-structured processor must be done on the whole chip, whereas in the serial approach it can be done at the cell level. In principle, the database consists of one cell and the placement of the cells. Today's computer-aided design tools are capable of handling the serial design, but would be hard pressed to develop a chip based on the bus-structured approach.

12-bit Analog/Digital Converter

Another challenge was to implement a 12-bit linear A/D (analog/digital) converter for band-limited signals of up to about 100 kHz on a chip. There were to be no external components and no component trimming. Also the technology had to be compatible with the 3 μm *n*-well CMOS technology used for the digital part of the UIC.

The need for a 12-bit A/D converter arises from the UIC design requirement for a digital summation point to cancel the echo. This decision was taken to avoid the need for a D/A converter as well as an A/D converter in the case of an analog summation point for converting the echo simulation and canceler error, respectively. Also it offered greater signal processing flexibility. The disadvantage is the need for a 12-bit A/D converter.

The A/D converter uses the principle of sigma-delta modulation[3] in which an oversampled 1-bit A/D converter is followed by a decimation filter which connects the 1-bit pulse density signal to a 12-bit-parallel word output (Figure 7). The 1-bit A/D converter includes a second-order noise shaping filter which shifts the quantization noise of the converter out of the band. The digital decimation filter acts as a passband filter and as a down sampler to the required sampling rate.

The same sigma-delta modulation principle is used in the latest System 12 line circuit. In implementing the sigma-delta modulator, a thorough study was carried out[3] which was also applicable to the UIC application. The main difference was the band of interest which differs by a factor of 10. Because of the oversampling principle used, it was necessary to scale the oversampling rate by a factor of 10 to achieve the same performance.

The system study was proven to be correct by realizing the line circuit sigma-delta modulator with a switched capacitor technique for the second-order noise shaping filter. Because this is the most critical part of the UIC, test vehicles were made to check the ability to achieve an oversampling frequency of 16 MHz. Two different approaches to implementing the noise shaping filter were used, one with a resistance-capacitance network and one based on the switched capacitor technique used for the line circuit sigma-delta modulator. Both approaches have advantages: the resistance-capacitance solution is simpler but the filter function is not well controlled, while the switched capacitor solution requires high speed operational amplifiers. Some work remains to be done on both approaches, mainly on layout artwork in order to get even closer to the theoretically achievable limits of the sigma-delta modulator.

Conclusions

Two of the most critical areas of the UIC design are the realization of a vast amount

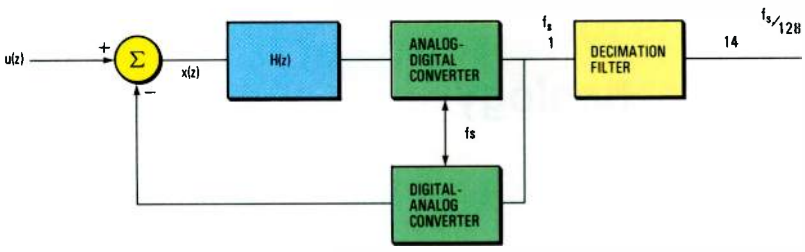

Figure 7
Block schematic of a sigma-delta modulator.

of signal processing on silicon, and the implementation of high speed analog functions. Total integration of the UIC would require a VLSI device based on 3 μm CMOS *n*-well, double polysilicon, single metal technology to achieve a device count of 100000 transistors on a chip with an area of just 120 mm^2. The maximum required clock rate is 16 MHz, and the power consumption 350 mW. About 20% of the circuitry is analog and 80% digital.

A chip of this complexity is not feasible with present technology. To ensure that the UIC is available for the ISDN fields trials which are scheduled for mid 1985 in several European countries, the UIC will initially be realized as four VLSI chips. This approach will be far more cost-effective than the equivalent printed boards. However, before ISDN can be introduced commercially in 1987, as is the intention in Germany, improved silicon technology will be necessary: 2.0 μm or even 1.5 μm CMOS.

References

1 H. W. Renz and L. Gasser: System 12: Transmission Method for Digital Subscriber Loop and Hardware Implementation: *Electrical Communication,* 1984, volume 59, no 1/2 (to be published).

2 H. T. Kung: Let's Design Algorithms for VLSI Systems: *Caltech Conference on VLSI,* January 1979.

3 K. Shenoi and B. P. Agrawal: Specification Based Design of Sigma-Delta Modulator for A/D and D/A Conversion: *Institute of Electrical and Electronics Engineers Transactions on Communications,* March 1983, no 3, pp 360–370.

Rudi Dierckx was born in Wilrijk, Belgium, in 1956. He studied industrial engineering at the Katholieke Industriele Hogeschool in Antwerp, where he graduated in 1978. He then read electrical engineering at the Catholic University of Leuven, obtaining a degree in 1981. Following a period of military service, Mr Dierckx joined the Research Center of BTM to undertake feasibility studies relating to the implementation of VLSI designs. He is also interested in VLSI architectures and digital signal processing.

Pierre-Paul Guebels was born in Lubumbashi, Zaire, in 1953. He studied electrical engineering at the Catholic University of Leuven, graduating in 1977 as a Dipl-Ing. He then joined the Laboratoire de Microelectronique in Leuven as a research engineer working on analog MOS circuits, switched capacitor filters, and MOS modeling. In 1980 he moved to the Research Center of BTM to design custom integrated circuits for telecommunication equipment. Mr Guebels is at present head of the BTM feasibility group.

Paul Six was born in 1951 in Leuven, Belgium. He studied electrical engineering at the Catholic University of Leuven where he was awarded a degree and then a doctorate in 1973 and 1980, respectively. Between 1973 and 1978 he worked as a research engineer at the ESAT laboratory, before joining the research staff of BTM in 1978. Initially he was involved in the reliability of integrated circuits, but for the past three years has been responsible for developing CAD tools for the design and verification of integrated circuits. Dr Six is at present head of the CAD group for integrated circuits.

Status and Prospects for Gallium Arsenide Technology

Gallium arsenide integrated circuits have been shown to perform well in ultra high frequency and data rate applications. With the establishment of manufacturing capability, the application of gallium arsenide integrated circuits to a wide range of military and commercial systems applications is now a reality.

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Roanoke, Virginia, United States of America

Introduction

The trend in advanced electronic systems is towards increasing integration at ever greater frequencies and data rates, as illustrated in Figure 1. By the end of the 1980s, the frequencies of analog circuits will approach 100 GHz and the speed of digital logic circuits will be around 10 Gbit s^{-1}. In addition, both high frequency analog and high speed digital functions will be on the same integrated circuit chip, as indicated by the overlap in Figure 1. To achieve a high level of integration under these demanding performance conditions requires new technology. Gallium arsenide (GaAs) promises to fulfill this requirement.

GaAs has semiconducting properties that offer better device performance than silicon. Electron mobility is about five times higher, offering higher speeds and an extended frequency response. The bandgap is 0.3 eV higher, allowing higher temperature operation. GaAs wafers can be obtained in semi-insulating form, giving good device isolation and lower capacitance. The greater mobility and lower capacitance give high speed with considerably lower power consumption (factors of 10 to 100 lower). Also GaAs transistors have been shown to be 10 to 1 000 times more resistant to radiation damage than silicon transistors. Finally, GaAs is compatible with other group III–V materials such as InAs (indium arsenide), AlAs (aluminum arsenide), GaP (gallium phosphide), and InP (indium phosphide), giving the materials flexibility necessary to develop special purpose optical (e.g. lasers) and electrical devices on the same chip.

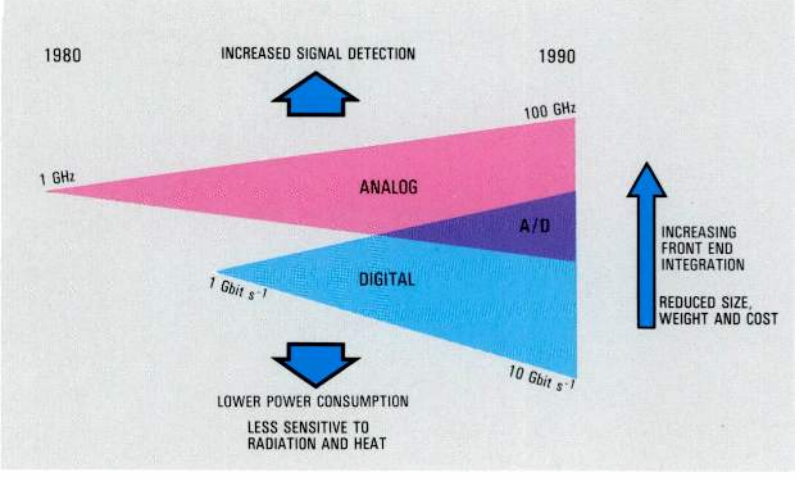


Figure 1
Schematic diagram showing advanced electronic system trends in the decade of the 1980s.
A/D - combined analog and digital.

Relative Application of GaAs and Silicon

Table 1 is a simplified comparison of the four basic transistor types: D-MESFET, E-MESFET (depletion or enhancement metal semiconductor field effect transistor), bipolar, and MOSFET (metal oxide semiconductor field effect transistor).

GaAs D-MESFETs are referred to as normally-on devices because current flows and power is consumed unless a sufficiently large negative voltage is applied to the gate. This technology is particularly important for microwave applications in the 2 to 20 GHz range and for high speed digital applications above 1 Gbit s^{-1}. In contrast, GaAs E-MESFETs are normally-off devices as no current flows when the gate voltage is turned off. This technology is still in the early stages of development, but its demonstrated capability for *both* high speed

Table 1 — Relative characteristics of transistors for high frequency and high speed applications

Transistor type	Preferred semiconductor	Relative maturity	High frequency properties		High speed properties		
			Maximum frequency	Minimum noise	Maximum speed	Minimum power	Maximum complexity
D-MESFET	GaAs	2	1	1	1	2	2
E-MESFET	GaAs	3	2	2	2	3	1
Bipolar	silicon	1	2	3	2	3	3
MOSFET	silicon	1	3	4	3	4	4

1 - high 2 - medium 3 - low 4 - not suitable for high frequency application

and low power consumption will be increasingly important in high speed, high complexity (> 1 000 gate) circuits. Silicon bipolar is a mature technology applicable to medium speeds or frequencies (generally less than 1 Gbit s^{-1} or a few GHz). Silicon MOSFET technology is mature and applicable to VLSI (very large scale integration) circuits, but is confined to low speed applications (generally less than 100 MHz).

The relative application of GaAs and silicon integrated circuit technologies is illustrated in Figure 2 with reference to an advanced electronic transmitter-receiver system. GaAs basically serves a 'front-end' function where the bandwidth is extremely large and real-time data processing rates are very high. The more mature silicon technology continues to serve the lower speed data processing needs of the system.

Status of GaAs Technology

The primary factor limiting the development of GaAs integrated circuits has been a lack of high quality standard sized wafers. Great strides have been made in the past three years, and 50 and 75 mm diameter wafers with good insulating properties are now readily available. Furthermore, these wafers are of sufficiently high quality that active devices (e.g. transistors) can be made by direct ion implantation, an efficient and uniform process. Epitaxial growth, which used to be essential, is now used primarily for special devices.

Full realization of the high speed potential of GaAs requires transistor gate lengths of 1 μm or less. Such demanding geometries are now routinely achieved for circuits of modest complexity, using contact photolithography with ultraviolet light. One micrometer geometries for high complexity circuits are now possible with recently developed 10:1 projection wafer stepper aligners in which each die is exposed individually. Geometries of less than 0.25 μm can be obtained by direct write electron beam lithography.

To fabricate circuits as described requires the ultimate in clean room conditions. Clean rooms of at least class 100 (under 100 particles of 0.3 μm or larger per cubic foot) are required. Also, temperature must be controlled to within ± 1 °C and relative humidity to within ± 3%.

Figure 3 summarizes the design, fabrication, and testing of GaAs integrated circuits, and indicates what clean room conditions are required.

Numerous analog (microwave) and digital prototype circuits have been demonstrated by a variety of companies. A 3-stage monolithic low noise C-band (5 to 6 GHz) amplifier with 20 dB gain has been designed at ITT Gilfillan and made at the ITT GATC (Gallium Arsenide Technology Center). Formerly, circuits of this type were made in

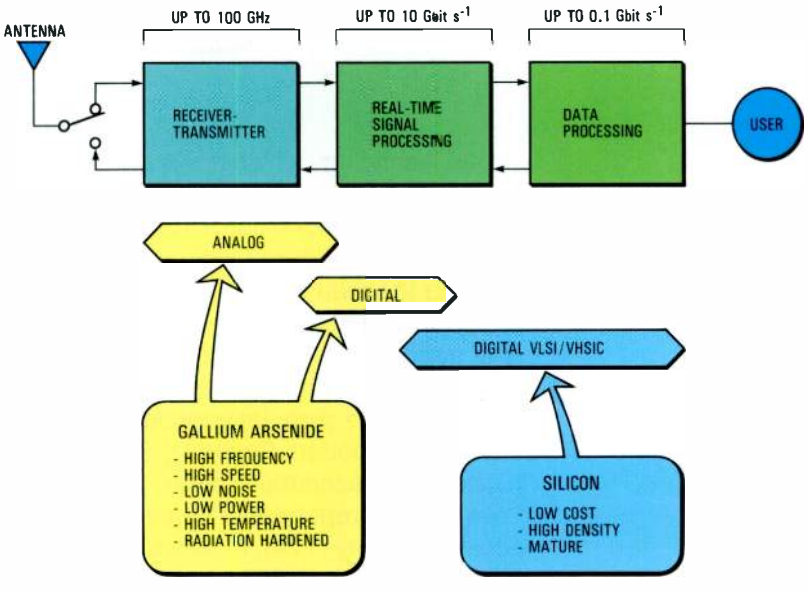


Figure 2 Schematic diagram of an advanced electronic system showing the relative application of GaAs and silicon integrated circuit technology. VHSIC - very high speed integrated circuit.

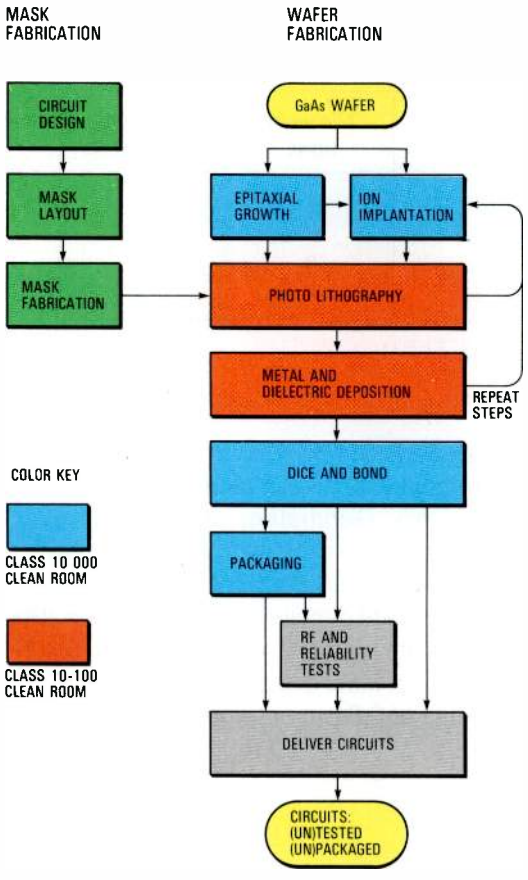


Figure 3
Flow diagram of the GaAs integrated circuit fabrication process.
RF - radio frequency.

hybrid technology which required many bond wires to connect the individual transistors, resistors, capacitors, and inductors. Monolithic technology makes it possible to produce small, low cost, reliable microwave circuits for high volume and/or high performance applications.

Several medium scale integration circuits and a few large scale integration circuits have been reported. Recently, STL (Standard Telecommunication Laboratories) reported a 128-bit random access memory (1 240 transistors) with a 2 ns access time, an 800 ps write time, and a power consumption of only 80 mW.

A wideband programmable transversal filter with a clock rate of 830 MHz which combines analog and digital functions, has been designed by STL, and successfully fabricated by both STL and ITT. Filtering is achieved by a sample and hold delay line with variable tap weights[1]. The filter serves as the frequency selection section of the integrated communication navigation identification avionics system being developed jointly by ITT Avionics Division and Texas Instruments. Thus, GaAs technology has progressed to the point at which GaAs integrated circuits are key elements in major advanced electronic systems.

Prospects for GaAs Integrated Circuits

The technology development for GaAs integrated circuits has been motivated primarily by the needs of military systems companies for high speed, high frequency circuits. Phased array radar systems utilizing thousands of individual transmit/receive integrated circuit modules will be available within the next few years. Such systems would not be economically feasible without GaAs technology.

Sophisticated broadband electronic countermeasures systems utilizing GaAs technology are now in advanced stages of development within ITT. With an ever increasing array of enemy threats, the need for ultra high speed real-time data processing is enormous. Advanced multifunction communication, navigation, and identification systems are now possible, owing to the availability of circuits such as the transversal filter described earlier.

Space, weight, and cost savings and the need for increased reliability are forcing more and more integration. Millimeter wave radar and communication systems in the 30 to 100 GHz range are being used for low probability of intercept short range communication needs and for high spatial resolution radar systems. As frequencies increase, component dimensions shrink to sizes that make hybrid mounting nearly impossible. Integrated circuit technology will make these systems feasible.

The total market for GaAs integrated circuits is expected to grow rapidly, exceeding one billion US dollars by 1988. Military applications will continue to dominate the market for some years, but commercial applications are increasing rapidly, and by 1988 may exceed military needs. Numerous commercial circuits are already under development.

Direct broadcast satellite receivers at 12 GHz for home users will be implemented in GaAs technology to achieve the necessary cost goals. The need for high data rate transmission over fiber optic communication links is increasing rapidly. Commercial systems with data rates of 1.2 Gbit s^{-1} are expected in a few years. Ultra high speed computers utilizing GaAs integrated circuits are under development, particularly in Japan. The high frequency front end of portable cellular radio units operating at 900 MHz may be fabricated in GaAs to achieve low power consumption.

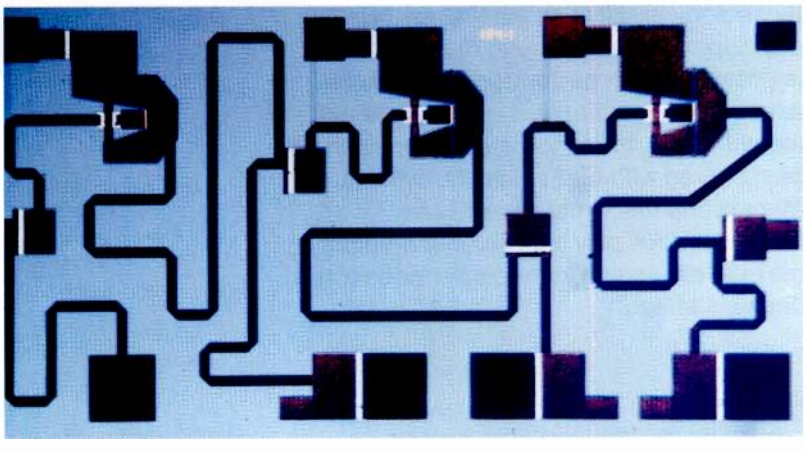
Several companies either have built or are building dedicated facilities for

producing GaAs integrated circuits. The ITT GATC in Roanoke, Virginia, is one such company. The ITT facility is colocated with the ITT Electro-Optical Products Division which produces GaAs night vision goggles and fiber optic components. With class 10-100 clean rooms, ion implanter, epitaxial growth, dry processing, and submicron photolithography facilities, this pilot line will be capable of producing a wide range of state-of-the-art digital and analog GaAs integrated circuits.

Future Technology

The technology for the GaAs D-MESFET is by now well established for gate lengths of about 1 μm. Further increases in speed and reductions in noise will be achieved as the gate length is reduced. Devices with gate lengths as short as 0.14 μm have been demonstrated in the laboratory. The self-aligned gate technology for automatic placement of short gates within the narrow source to drain spacing will make it practical to manufacture short gate FETs. A member of ITT's technical staff (while at Cornell University) measured a gate delay of only 15.4 ps from a D-MESFET fabricated with self-aligned gate technology and electron beam lithography to produce a gate length of 0.3 μm.

A 3-stage GaAs monolithic C-band (5 to 6 GHz) low noise amplifier.



The capability of E-MESFET technology to provide high speed with low power consumption has been established. Now the challenge is to utilize this advantage to produce LSI and VLSI chips. To achieve this with high yields will require further advances in GaAs material uniformity in order to obtain the necessary tight tolerance in switching voltages from gate to gate.

The advent of molecular beam epitaxy with the capability for growing precise layers of GaAs and other group III–V compounds that can have a thickness of less than a few hundred angstroms has led to new high speed transistors. High electron mobility transistors achieve higher speed by utilizing electron transport through an extremely thin (about 500 angstroms), high mobility undoped GaAs layer.

Other multiple layer devices that may find practical application are the heterojunction bipolar transistor and the junction field effect transistor. It has been shown at the ITT GATC that junction field effect devices grown by metallorganic chemical vapor deposition have better noise properties and higher breakdown voltages than normal MESFETs.

All of these multiple layer devices have been demonstrated in the laboratory. The challenge is to develop manufacturing processes for such complex devices. Cassette load, production type molecular beam epitaxy machines should help greatly in this effort.

Molecular beam epitaxy or metallorganic chemical vapor deposition multiple layer technology will also make it possible to fabricate opto-electronic integrated circuits in which optical devices such as lasers and photodetectors can be combined with high speed circuitry on the same chip. Such devices will have wide application in fiber optic communication systems.

Regardless of the device technology employed, important factors in future development are high speed packaging and testing. Cross coupling and parasitic losses at high frequencies and speeds make packaging particularly difficult. In the microwave integrated circuit area, test methods and equipment are well established. However, the testing of high speed digital integrated circuits (above 1 Gbit s^{-1}) needs considerable development.

Finally, the reliability of GaAs integrated circuits must be better established. This effort will build on the established reliability base for discrete GaAs devices in both military and commercial applications.

Conclusions

Ever since the advent of integrated circuit technology over three decades ago, GaAs has held great promise owing to its inherently superior semiconducting

ITT Gallium Arsenide Technology Center facility in Roanoke, Virginia.

properties. This promise is now being fulfilled. With over 60 companies worldwide now engaged in GaAs integrated circuit development, technical progress and the number of applications have been increasing rapidly. Good results on a number of relatively complex circuits, both digital and analog, have provided a sufficiently high confidence level to motivate significant manufacturing efforts. Established manufacturing capability will make low cost commercial applications feasible and will increase reliability in high performance military applications.

The common question as to whether GaAs or silicon will dominate in the future is not particularly relevant at this time. The important question is how existing technologies can complement one another. Silicon technology is mature and will be the workhorse of the industry for years to come. Further, owing to such developments as the very high speed integrated circuit, or VHSIC, the performance of silicon integrated circuits will continue to improve, but be limited by fundamental properties.

By comparison, GaAs integrated circuit technology is still at an early stage of development so continued rapid improvements in performance can be expected. Accordingly, it is now clear that many high performance applications can be best served with GaAs. Finally, by including other group III–V materials, GaAs technology will play a key role in meeting the ever expanding technology needs of the decades ahead.

Reference

1 A. J. McKnight, J. Mun, and I. A. W. Vance: Wideband Programmable Transversal Filter: *Electrical Communication,* 1984, volume 58, no 4, pp 423–426 (this issue).

Dennis G. Fisher obtained a PhD in electrical engineering from the University of Minnesota in 1968. He was a member of the technical staff at the RCA David Sarnoff Research Center, where he developed photodetectors utilizing GaAs and other III–V compound materials. In 1977 he joined ITT Electro-Optical Products Division where he directed the development of GaAs image intensifiers. In 1981 Dr Fisher started the project which led to the establishment in 1983 of the ITT GATC of which he is the director.

Wideband Programmable Transversal Filter

The high operating speeds associated with integrated circuits that use GaAs substrates have been used to develop a filter which operates to very high clock frequencies. A clocked analog delay line is configured as a transversal filter capable of processing signals at frequencies up to 1 000 MHz.

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J. Mun
I. A. W. Vance
Standard Telecommunication Laboratories Limited, Harlow, England

Introduction

Filters are always required in communication systems, and the provision of suitable high frequency filters is a traditional problem. A monolithic filter developed at STL (Standard Telecommunication Laboratories) uses a sampled analog technique to achieve both high frequency operation and wide dynamic range. This integrated circuit has been fabricated using a GaAs MESFET (metal semiconductor field effect transistor) process which incorporates devices with 1 μm gate lengths and has a 10 μm metal pitch.

The circuit design provides for three alternative filter responses: high pass, low pass, and band pass. The cut-off frequency of the filters is programmable simply by altering an external clock frequency.

Filter Design

A transversal filter is programmed in the time domain in order to produce a filter response in the frequency domain. It consists essentially of an analog delay line made up of a number of clocked delay stages; the time delay in each stage is controlled by an external clock. The delay line is tapped after each delay and the signal is weighted (multiplied by a coefficient). The weighted signals are then summed to produce the filter output. Figure 1 shows a low pass filter as an example; the required impulse response is of the sin x/x type.

One delay line may feed more than one set of tap weights to give more than one filter response output simultaneously. The filter response is calculated using the fact that the Fourier transformation of the tap weights in the time domain (that is the

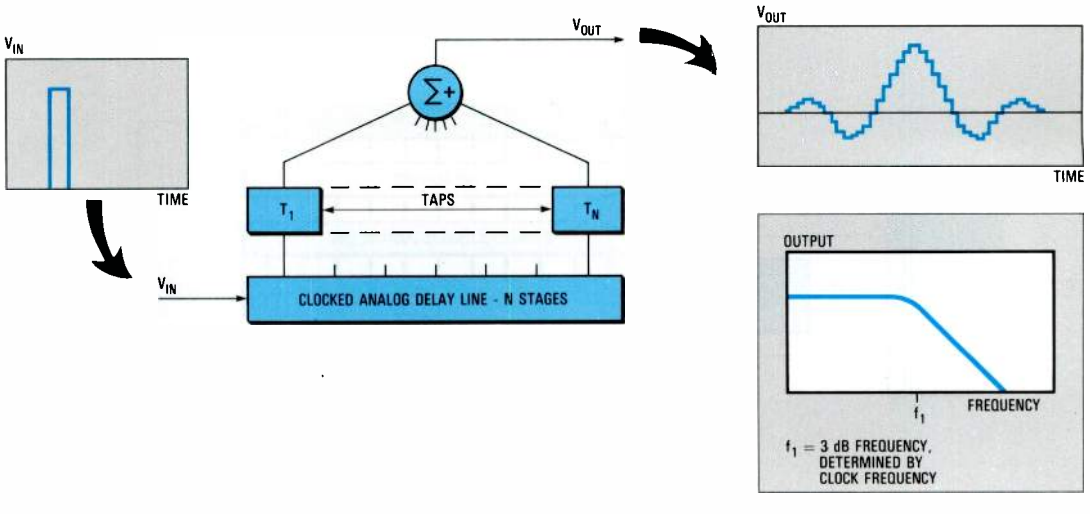


Figure 1
Concept of the transversal filter showing the required sin x/x response.

impulse response) is the required frequency response. Hence the shape of the filter is determined by the values of the tap weights and the position in the frequency spectrum is determined by the clock frequency.

The filter described here uses a 7-stage delay line and has three sets of tap weights, enabling three so-called half-band filter responses to be obtained: low pass, band pass, and high pass (Figure 2). The particular shapes are chosen to give a more precise filter characteristic when used in combination. The output from the band pass filter is phase shifted by 90° and added to either the low pass or high pass outputs. The combined filter then has a flat passband and a better shape factor (rate of change from passband to stopband). Furthermore, aliased responses* can be canceled by this technique.

The delay line consists of a series of cascaded sample and hold circuits, each realized as a GaAs MESFET switch followed by a storage capacitor. The storage capacitors are fabricated as a MIM (metal-insulator-metal) structure using the two layers of gold metallization and polyimide insulation which are standard in the STL GaAs process. After each delay stage a source follower buffer delivers the signal to another set of similarly constructed capacitors which differ in value such that a proportion of the signal in each delay stage is added together to give the output.

Figure 3 shows the overall construction of the chip. A differential delay line is used to simplify the switching of tap weights between positive and negative values and also to give better clock cancellation at the output. A balanced signal (a normal and an inverted version of the waveform) is derived from the input and delivered to the delay line; the outputs from the differential sets of weighting capacitors are each summed in an output amplifier. A clock driver circuit is also provided on the chip.

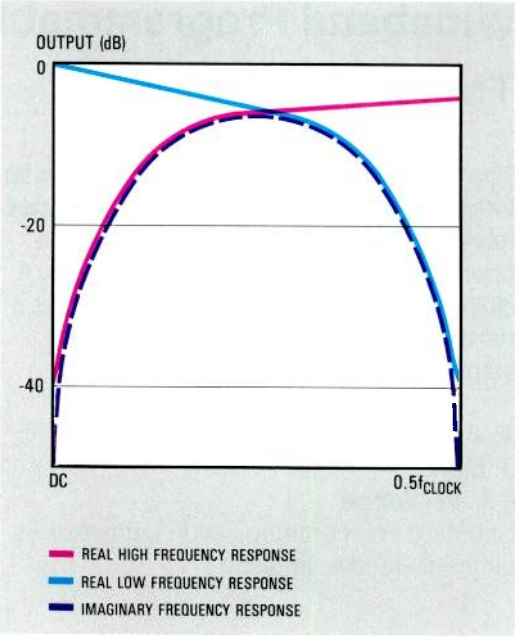


Figure 2
Required design frequency responses.

It can be seen that the entire design may be made from just three types of component: the MESFETs, MIM capacitors, and epitaxial resistors. The technique is thus compatible with a simple GaAs process originally designed mainly for digital applications.

Gallium Arsenide Technology

The process used to fabricate these filters uses six masking steps on a 2 inch (51 mm) diameter semi-insulating GaAs wafer. Fabrication consists of implanting the wafers with a thin layer of silicon ions and annealing this implant to give a doped active layer on the surface of the wafer. Transistors are

* Unwanted passbands caused by signals mixing with the clock frequency.

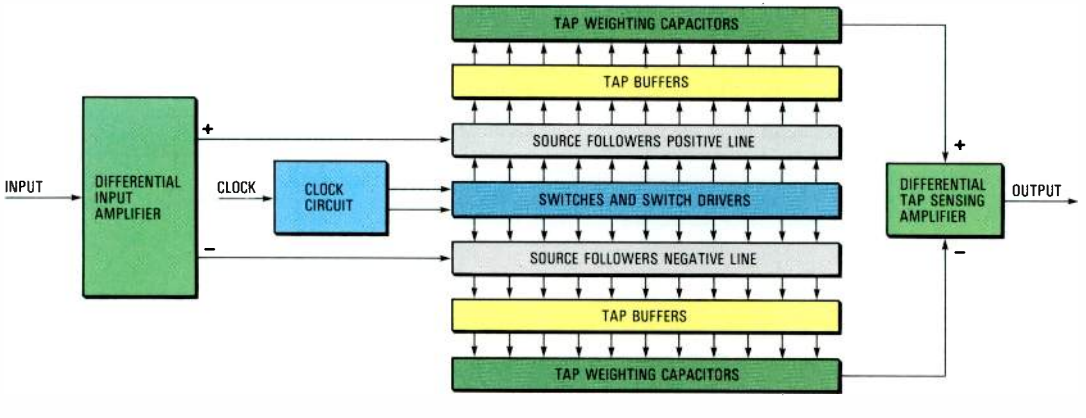
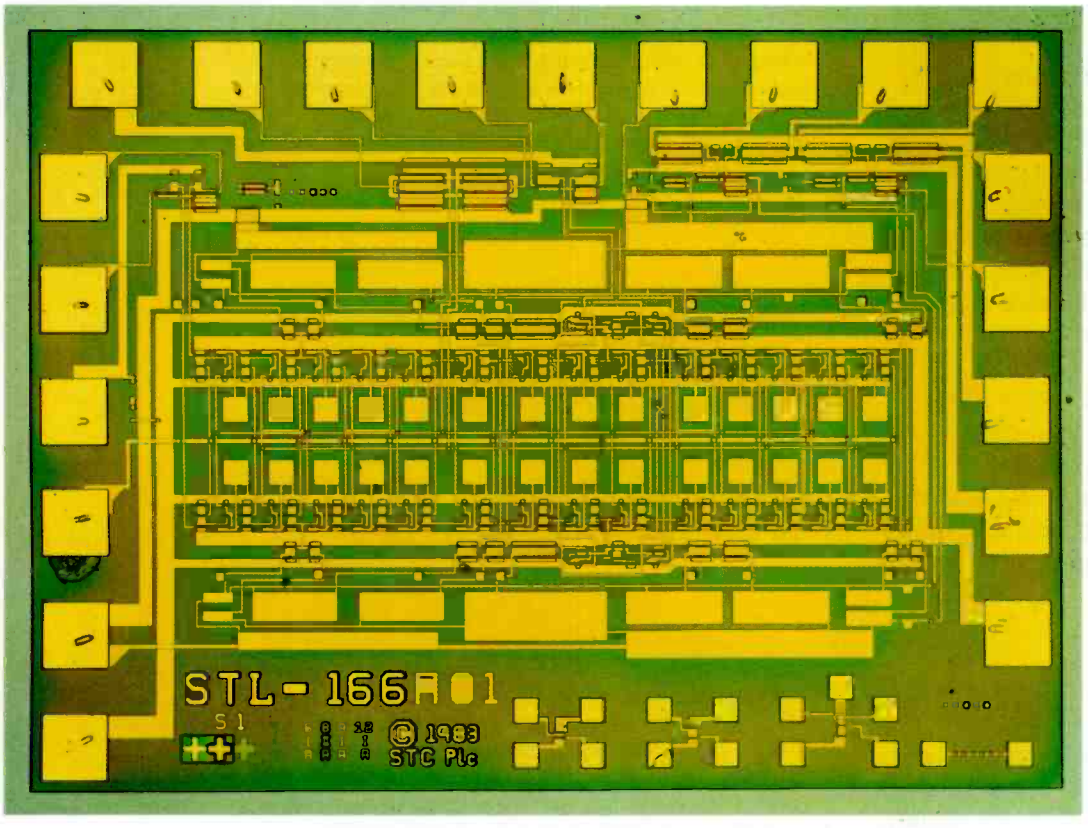


Figure 3
Block schematic of the monolithic transversal filter.



Fabricated integrated circuit filter. The larger dimension is 2.5 mm; the delay line can be seen at the center.

formed by two metallization steps. First gold-germanium and nickel are deposited to form the source and drain regions of the FETs; second a chromium-gold layer is added which forms the Schottky barrier gate of these devices. Each metal layer is evaporated onto the wafer and delineated using standard photolithographic techniques. Transistors are isolated from each other by bombarding all other areas of the wafer with protons, thereby rendering the areas between devices nonconducting. The capacitors are formed together with the second level of interconnect metal by a further deposition and patterning of chromium-gold on top of an insulating layer of polyimide. The use of proton isolation gives an essentially planar structure and the relative simplicity of the process, especially as it involves neither epitaxial crystal growth nor any diffusion, enables large complex circuits to be fabricated.

Results

Operation of experimental filters has been achieved at clock frequencies ranging from 10 MHz to 1000 MHz. Figure 4 shows the frequency responses obtained from the three modes of operation of the filter. In this figure the wanted response is that between the zero frequency point (left side) and half the clock frequency, the so-called Nyquist frequency; the passbands shown between the Nyquist frequency and the clock frequency are an unwanted aliased response which is inherent in half-band filters. In practice, as noted above, the imaginary filter may be combined with either the high pass or low pass filter in a system in order to eliminate the unwanted aliased passband. The attenuation curves of the fabricated filter correspond closely to the theoretically predicted responses for the number of taps used. Within the wanted passbands, the dynamic range measured as a ratio of the peak signal level before compression to the noise floor in a 100 kHz bandwidth is over 90 dB. A high yield of working circuits was obtained from the processing.

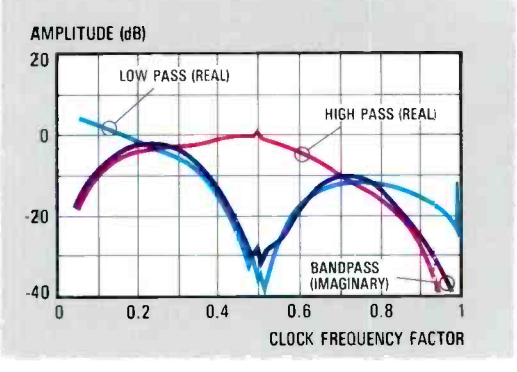


Figure 4 Measured filter responses in the low pass, high pass, and band pass (imaginary) regions. The clock frequency is 10 MHz.

Conclusions

The transversal filter developed at STL shows for the first time that it is possible to realize the radio frequency filtering circuit function in integrated circuit form. This is of critical importance to the production of compact, highly reliable radio systems. Further work is aimed at increasing the complexity of the circuitry so that more complex filtering functions can be realized on one chip.

The techniques used here are also applicable to other circuit functions such as correlators and very fast analog-to-digital converters. Commercial production of GaAs circuits in general, and this type of high speed analog component in particular, will start during 1985.

Acknowledgment

The authors wish to acknowledge the important contributions to this work made by Mr C. R. Ward, at ITT Avionics, Nutley, New Jersey.

A. J. McKnight was born in 1961 in Aberdeen, and graduated in electrical engineering from the University of Glasgow in 1981. He joined STL the same year where he has been involved with the transversal filter development since its inception. He built the first breadboard filter, carried out the computer simulations, and implemented the design on GaAs.

J. Mun was born in 1943 in Macau and graduated in electrical engineering from the University of Aston in 1968. He was awarded a masters degree in microwave engineering from University College, London, in 1969, and joined STL the same year. Mr Mun has worked for many years on transferred electron devices in GaAs and InP. He was responsible for the development of GaAs MESFETs leading to integrated circuits, and is now manager of the GaAs integrated circuit department.

I. A. W. Vance was born in 1947 in Bristol, and joined STL on graduating from the University of Liverpool in 1968. He was subsequently awarded a masters degree from the University of Aston. Mr Vance has worked in radio engineering and in technology applications; he is at present division manager for subsystems technology at STL.

Designing for Testability

With the increasing complexity of VLSI chips and systems, it is necessary to design them to be testable in order to contain rising test costs and provide high quality products.

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Introduction

As advances in semiconductor device technology increase circuit densities, more and more entire logic functions are being performed within each monolithic package. Since the end user is only interested in the overall function of the package, designers provide the lowest number of input and output leads necessary to achieve normal operation. This results in many internal nodes being inaccessible (i.e. their status cannot readily be controlled or observed). Consequently, a long sequence of test patterns must be used to check device performance adequately.

M. Feuer[1] observed that "Even for an early microprocessor ... an exhaustive test set would contain over 10^{32} patterns; at 1 μs per input pattern, the test time would be more than 10^{20} years!" This led to the conclusion that exhaustive testing is impractical and that "functional" test patterns should be used. However, the generation of functional test patterns for complex circuits can be a major task requiring many man-weeks of test engineers' time and/or hundreds of computer hours. It is now realized that the best way of economically testing devices that contain long or complex internal logic chains is to design them to be testable. This is primarily achieved by improving observability and controllability and/or self testing.

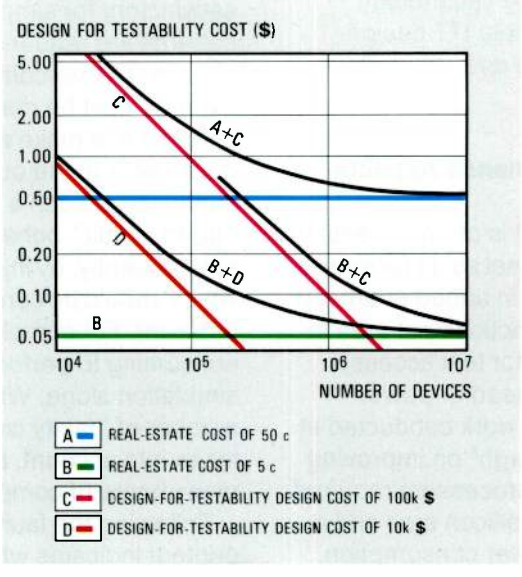


Figure 1
Cost of designing for testability as a function of production quantity.

Designing for Testability Costs

Test costs have become a substantial part of product cost. For example, test costs for memory have increased from 10% to over 35% of the total device cost as density has increased from 4 K to 64 K memory per chip[2]. Two costs must be considered: the cost of testing the physical device and the cost of generating a satisfactory test program. However, these are not the only device testability related costs; additional end product costs may arise as a result of inadequate device tests[3,4].

Since designing for testability can affect both test time and test equipment requirements, it can influence test costs by several orders of magnitude. However, increasing testability also involves a cost in added design effort and/or additional circuit chip area, usually referred to as real estate. Examination of the probable cost of designing for testability as a function of the quantity of devices to be produced is enlightening. Figure 1 illustrates the effect of additional real estate costs of 5 cents per device and 50 cents per device, as well as added design costs of $ 10000 and $ 100000. Consideration should not be given only to the maximum ($A + C$) and minimum ($B + D$) cases since it may be desirable to minimize real estate costs even at the expense of an increase in design cost, to obtain the most beneficial result for high quantity production.

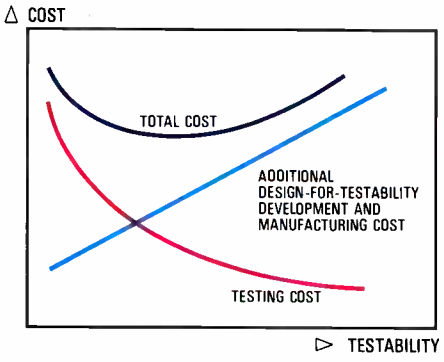


Figure 2
Typical cost of designing for testability as a function of test cost relation (cost vs the extent of implemented testability).

The more testability that is provided, the lower the resultant test cost. Figure 2 demonstrates the need to design just enough testability into the device to be at the minimum point of the total cost curve. Design for testability cost tradeoffs must therefore be performed to achieve this optimum solution. The following steps are necessary:

- define alternative implementations
- calculate the predicted test cost for each alternative
- calculate the additional design cost for each alternative
- calculate incremental continuing costs (added components, real estate)
- compare additional design and/or product costs against test cost savings
- select optimum alternative.

Testability cost tradeoff is readily accomplished since the design for testability costs and corresponding savings can both be quantified. One of the activities of the ITT Advanced Manufacturing Technology Center test group is to help ITT design teams to carry out these cost tradeoffs.

Overhead and Performance Aspects

As already mentioned, it is often necessary for some chip area to be set aside for special test functions, resulting in added overhead (e.g. loss of gates or functions per area or allocation of some pins for test access). Sometimes there are speed or power penalties. For example, work conducted at the University of Edinburgh[5] on improving the testability of signal processors required a 4% increase in active silicon area and a 9% increase in chip power consumption.

Motorola's MC6804P2 8-bit single chip microcomputer, which has built-in self testing to improve testability, uses 5% of the silicon area for specific test logic[6]. Texas Instruments evaluated two schemes to obtain better testability for their TMS7000; both required additional area and one required a 10% increase in execution time[7]. ITT designers concerned with designing for testability have also found it worthwhile to pay the relatively small cost and/or performance penalty.

Relationship of Test Stimuli Generation and Fault Coverage to Circuit Testability

Two types of test stimuli are widely used for testing digital circuits: functional test patterns and pseudorandom patterns. A third type, entailing the application of all possible input combinations of test patterns, is referred to as an exhaustive test; it can be extremely time consuming. However, it has recently attracted great interest since it can achieve startling results when specific "design for testability" rules are applied.

Functional Test

The objective of testing is to determine whether a circuit functions properly (i.e. is free from defects or faults). This may be done by applying a series of functional test patterns to the inputs of the device under test and determining its performance by observing the output.

To conduct an adequate test, it is not sufficient to apply test patterns that determine whether the device is performing its intended functions. Additional patterns are needed to ascertain that it does not perform unintended functions. While this is satisfactory for simple circuits, too many patterns are required to test complex circuits. To overcome this problem, an attempt must be made to find a set of test patterns that make all possible faults observable at the output. To determine the adequacy of such a set of test patterns, "good circuit" behavior is simulated and subsequently, by injecting all possible faults which should be considered, "faulty circuit" behavior. For complex circuits, it is time consuming to perform "good circuit" simulation alone. When the required number of "faulty circuit" simulations is taken into account, the simulation can take many hours of computer run time.

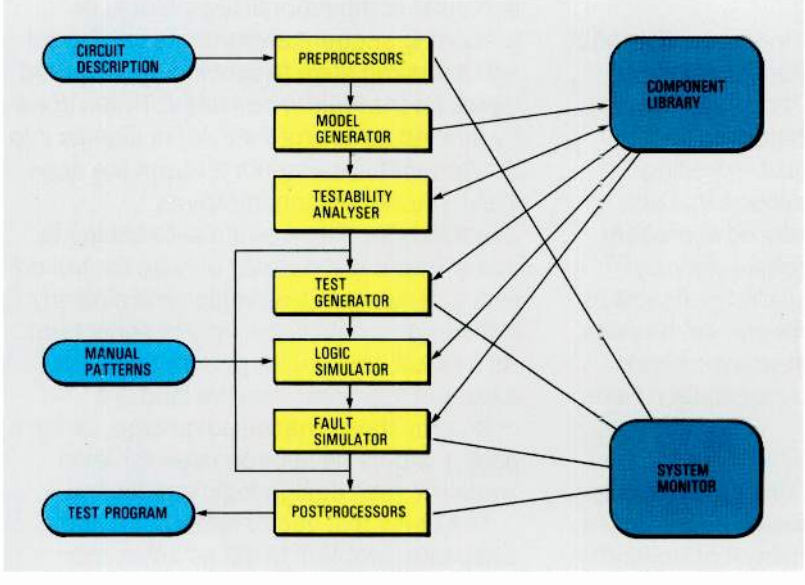
Following the fault simulation runs, a printout indicates which faults have not

been detected. It is then usually necessary to add additional test vectors until the desired fault coverage is achieved. In many cases, however, even after additional test vectors have been included, not all faults are detected as parts of the circuit are untestable. This is usually a result of inadequate observability or controllability of internal nodes. The circuit must then be restructured to ensure that an adequate test can be performed, and the simulations repeated.

To enable potential testability problems to be identified at an early stage, several testability analysis programs have been developed. These help the designer to determine whether any part of the circuit is untestable before unnecessary simulation effort is expended. These programs are not only of value in functional testing, but are also applicable to other test methods.

It is becoming common practice in many companies to let the design engineer perform a testability analysis as part of his overall design activity. At Standard Elektrik Lorenz, for example, a testability analysis program has been integrated with other software packages (Figure 3) so that comprehensive test programs can be generated efficiently[8].

Figure 3 Integration of testability analysis and test program generation.



Several engineering workstation vendors are also incorporating testability analysis programs into their products, and in future design engineers may find it easier to implement testability at the initiation of the design.

Probabilistic Test

To avoid costly functional test program preparation, another type of test stimuli generation has been gaining increasing acceptance, namely, the utilization of pseudorandom test patterns. However, long test vector sequences may be required to perform an adequate test[9] unless specific design for testability rules are observed[10]. Data compression is used to cope with the large volume of data. This may be accomplished using linear feedback shift registers, resulting in a single word output, referred to as a *test signature,* after all test vectors have been applied[11,12]. This technique is especially attractive for self testing.

Exhaustive Test

Test patterns for exhaustive and pseudo-exhaustive testing are easily obtained since they merely require *all* possible input combinations to be applied. The major disadvantage is excessive test time, since sequential circuits require $2^n \times k^2$ test vectors for a k-state circuit, unless specific "design for testability" rules are applied. Techniques such as partitioning and segmenting enable pseudo-exhaustive tests to be performed with excellent results[13,14].

For example, after slight modification an arithmetic logic unit/function generator was exhaustively testable with 324 test vectors compared with the 2^{14} that would have been required otherwise. Thus, by applying design for testability techniques, high fault coverage can be assured and test program generation costs are almost eliminated since there is no need to prepare a functional test program and fault simulation runs are not required.

It can be seen that test program generation costs and achievable fault coverage depend considerably on design for testability, and that tradeoffs must also be made between appropriate programming and design for testability costs.

Design for Testability Strategies

Techniques used in designing for testability can be divided into three major categories: techniques that make internal functions of the circuit more observable and controllable, techniques that make a large circuit more testable by partitioning it into smaller and more readily testable subcircuits, and finally built-in self testing

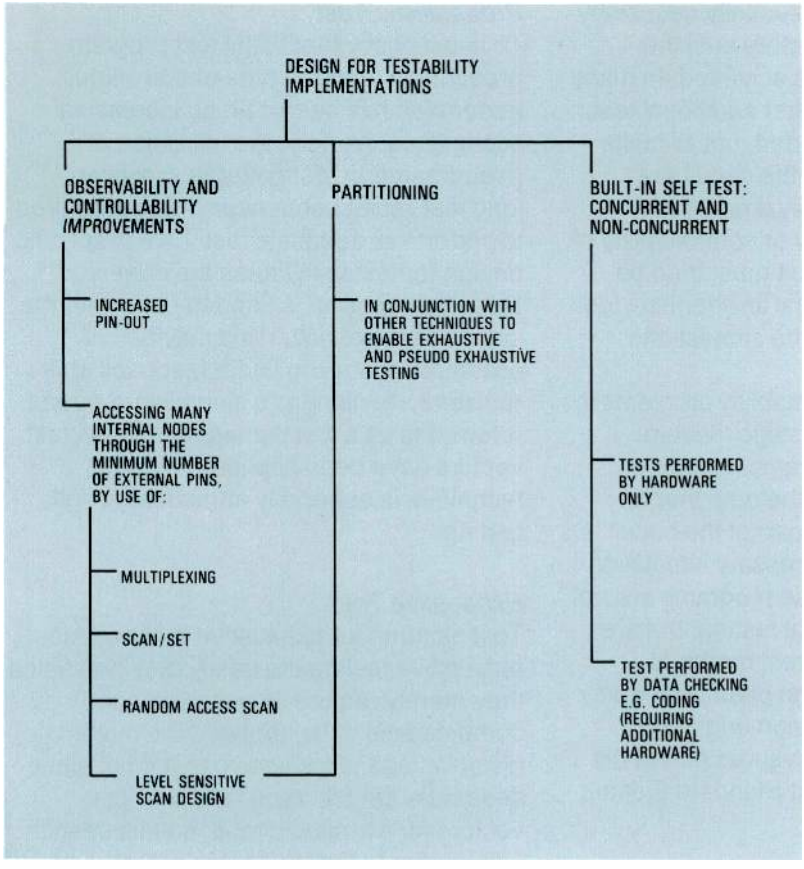


Figure 4
Three main implementations of designing for testability.

which enables the circuit to test itself without necessarily requiring extensive external stimuli or observation. Of course, techniques can be combined, as is frequently the case for built-in testing.

Figure 4 lists the techniques that are being most widely considered at present. However, many other techniques exist[15]. Because they are particularly applicable to VLSI (very large scale integration) devices, scan design and the built-in logic block observation technique are described here.

Scan Design

One of the earliest scan design techniques – level sensitive scan design – combines partitioning and observability/controllability improvement features[16,17]. Its operation is most readily understood by referring to Figure 5. Since it is easier to test combinatorial logic than a mixture of combinatorial and sequential logic, in its simplest form level sensitive scan design partitions combinatorial logic from sequential logic. It furthermore enables the sequential logic elements, in effect, to be switched out of their normal circuit environment into a test mode environment in which all sequential circuits are connected in sequence to form a long shift register. This replaces the difficult task of finding appropriate test vectors to test "buried" internal sequential circuits with a simple single shift register test.

When the circuit is switched into the test mode, the state of each sequential element will be a function of the previous output state of the combinatorial logic to which it was connected. Thus, when the content of the shift register (made up of these sequential elements) is shifted out, it is possible to observe the states that existed at specific internal combinatorial logic nodes just prior to the test operation, resulting in improved observability.

Conversely, if it is desired to test a particular combinatorial logic block, its preceding sequential elements can be set into a desired state to provide the required inputs for the logic to be tested. This is done by shifting an appropriate set of signals into the sequential elements through the scan input, thus achieving improved controllability. The major disadvantage is that all internal nodes can only be controlled with a serial input test vector and similarly the output is obtainable only in serial form. As a result, test vector generation is not easy and test times may be long. To overcome the former disadvantage, random pattern inputs have been used for level sensitive scan design logic self testing[18].

The serial test vector application and evaluation problem is not as severe for some of the other scan techniques, among

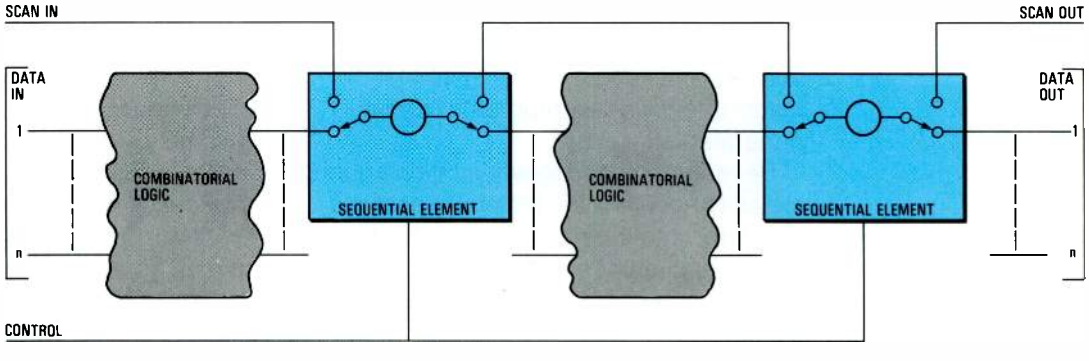


Figure 5
Block schematic of level sensitive scan design.

them random access scan[19], scan set[20], and mixed serial and parallel scan readouts. Each has its own advantages and disadvantages, but when correctly implemented the test quality that can be economically achieved on very complex circuits is higher than would be possible without these techniques.

Built-in Logic Block Observation

This technique is especially attractive for VLSI circuits as device testing does not necessarily require expensive external test equipment; furthermore the chip can test itself at its normal operating speed[21,22]. A simplified block diagram is shown in Figure 6. Basically four separate operations are performed:

- Circuit elements are interconnected in a similar way to level sensitive scan design, to perform their intended logic function (indicated in black).
- When combinatorial logic block *1* is to be tested, sequential elements *A* are internally interconnected to form a linear feedback shift register which serves as a pseudorandom pattern generator. The generator provides input signals to exercise logic block *1*. Sequential elements *B* are also interconnected as a linear feedback shift register to function as a signature analysis register, facilitating the comparison of actual circuit response signatures with a set of internally stored known "good circuit" response signatures. This test mode is shown in red.
- When combinatorial logic block *2* is to be tested, sequential elements *B* are used as a pseudorandom pattern generator and sequential elements *A* as the signature analysis register (green).
- An optional fourth mode is available in which all sequential elements are interconnected to form one shift register which then allows them to be used in a scan-in scan-out mode (blue).

By utilizing built-in logic block observation, the best features of scan design and real-time testing are combined with the advantage of not requiring costly functional test pattern generation.

Conclusions

Since test costs now represent a substantial part of the cost of a product, and as adequate testing of complex devices is essential to achieve the required quality, designing for testability must be given appropriate priority. In ITT, designing for testability has played a major role in the development of new advanced array processors developed at the Advanced Technology Center in Shelton, and of custom VLSI designs produced at Bell Telephone Manufacturing Company, Antwerp, and in many other units. Thus, it has been widely recognized that designing for testability can reduce costs, increase quality, and improve maintainability, thereby enhancing the satisfaction of users.

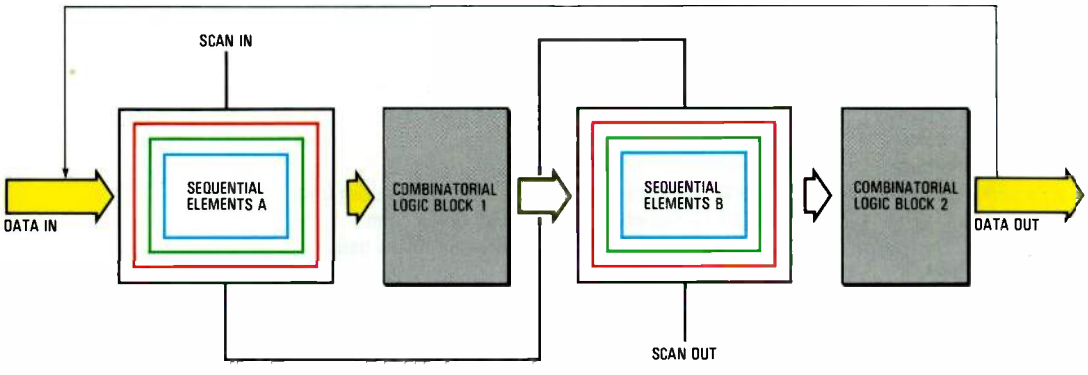


Figure 6
Block schematic of built-in logic block observation.

References

1 M. Feuer: VLSI Design Automation: An Introduction: *Proceedings of the Institute of Electrical and Electronics Engineers,* January 1983, volume 71, no 1, p 6.
2 G. A. Perone, R. S. Malfatt, J. P. Kain, and W. I. Goodheim: A Closer Look at Testing Costs: *1982 International Test Conference,* November 1982, pp 574–578.
3 G. W. Jacob: ATE Throughput Predictions for Test Planning: *1980 International Test Conference,* November 1980, pp 203–209.

4 G. W. Jacob: Preparation of Product Test Plans: *1981 International Test Conference,* October 1981, pp 340–347.
5 A. F. Murray, P. B. Denyer, and D. Renshaw: Self-Testing in Bit Serial VLSI Parts: High Coverage at Low Cost: *1983 International Test Conference,* October 1983, pp 260–268.
6 J. Kuban and B. Bruse: The MC 6804 P2 Built-in Self Test: *1983 International Test Conference,* October 1983, pp 295–300.
7 T. Stridhar and S. M. Thatte: Concurrent Checking of Program Flow in VLSI Processors: *1982 International Test Conference,* November 1982, pp 191–199.
8 S. Voigt and U. Apel: Testability Analysis of Digital Circuits in Support of Design and Automatic Test Generation: Presented at the *1st European Workshop on Design for Testability,* Toulon, 1982.
9 J. Savir and P. H. Bardell: On Random Test Pattern Length: *1983 International Test Conference,* October 1983, pp 95–106.
10 J. Savir, G. Ditlow, and P. H. Bardell: Random Pattern Testability: *Proceedings of the 13th Annual Fault Tolerant Computing Symposium,* June 1983, pp 80–89.
11 J. E. Smith: Measures of Effectiveness of Fault Signature Analysis: *Institute of Electrical and Electronics Engineers Transactions on Computers,* June 1980, volume C-29, pp 510–514.
12 R. David: Testing by Feedback Shift Registers: *Institute of Electrical and Electronics Engineers Transactions on Computers,* July 1980, volume C-29, pp 668–673.
13 E. J. McCluskey and S. Bozorgui-Nesbat: Design for Autonomous Test: *Institute of Electrical and Electronics Engineers Transactions on Computers,* November 1981, volume C-30, no 11, pp 866–879.
14 E. J. McCluskey: Built-In Verification Test: *1982 International Test Conference,* November 1982, pp 183–190.
15 T. W. Williams and K. P. Partner: Design for Testability – A Survey: *Proceedings of the Institute of Electrical and Electronics Engineers,* January 1983, volume 71, no 1, pp 98–112.
16 E. B. Eichelberger and T. W. Williams: A Logic Design Structure for LSI Testability: *Proceedings of the 14th Annual Design Automation Conference,* June 1977, pp 462–468.
17 S. das Gupta, P. Goel, R. G. Walther, and T. W. Williams: A Variation of LSSD and its Implication on Design and Test Pattern Generation in VLSI: *1982 International Test Conference,* November 1982, pp 63–66.
18 E. B. Eichelberger and E. Lindbloom: Random Pattern Coverage Enhancement and Diagnosis for LSSD Logic Self Test: *IBM Journal of Research and Development,* May 1983, volume 27, no 3, pp 265–272.
19 H. Ando: Testing VLSI with Random Access Scan: *Digest Papers Compcon,* February 1980, pp 50–52.
20 J. M. Stewart: Future Testing of Large LSI Circuit Cards: *1977 Semiconductor Test Symposium,* October 1977, pp 6–17.
21 B. Koenemann, J. Mucha, and G. Zwichoff: Built-In Logic Block Observation Techniques: *Institute of Electrical and Electronics Engineers Test Conference 1979,* October 1979, pp 37–41.
22 W. Daehn and J. Mucha: A Hardware Approach to Self Testing of Large Programmable Logic Arrays: *Institute of Electrical and Electronics Engineers Transactions on Computers,* November 1981, volume C-30, no 11, pp 829–833.

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ITT's Testability Analysis Program

Testable designs ensure product quality and reduce production and life cycle costs. ITTAP – ITT's testability analysis program – supports the evaluation and enhancement of design testability.

R. M. McDermott
ITT Advanced Technology Center, Shelton, Connecticut, United States of America

Introduction

The mounting of increasingly complex VLSI (very large scale integration) circuits in packages with a limited number of pins makes it essential to improve the techniques for producing testable designs. In prior generations of equipment using discrete or small scale integration components, it was feasible (albeit costly) to ignore testability at the chip or printed board level, relying instead on access to intermediate nodes of a design to isolate faults. With devices containing thousands of gates in packages with 20 to 40 pins, access to intermediate nodes is severely limited, and the cost of assuring that all of these gates are operating correctly can be extremely high unless the device is designed to be testable. Improving a design's testability requires techniques that increase access to internal nodes through limited input/output pins (i.e. optimize the effectiveness of added test input/output pins).

The cost of implementing a testable design can be extremely high unless specific design constraints are enforced, or computer-aided design tools are provided to assist in evaluating and enhancing testability. A number of testability analysis tools have been developed[1 to 5], but few really address the task of assisting in the *enhancement* of a design's testability. ITT's testability analysis program has been designed specifically for this purpose.

Design for Testability

A testable design provides for rapid and easy detection of an abnormality in the operation of a circuit. The term abnormality is used intentionally, since it is assumed that the design is correct and only the presence of a physical fault causes improper operation. Such a definition also implies that correct operation of the design is known *a priori,* so that an observed difference implies the presence of a fault.

With highly complex designs, particularly memory and/or sequential designs, the observation of a difference is extremely difficult. Consider, for example, a faulty memory bit; the effect of this fault may not be observed until that bit is referenced, and the fault is such that this memory state is opposite to the expected state. Similarly, a fault in a sequential device may not be observed until the effect of the fault is clocked out and its state is different from the fault-free state.

Design for testability is a design method intended to ease the task of observing the effect of a physical fault, particularly in sequential designs. A number of approaches have been developed, ranging from simple approaches such as adding resets to sequential devices, to the LSSD (level sensitive scan design) approach[6] for setting sequential devices to specified states and subsequently observing their next state. The *ad hoc* (add reset) approach is highly effective in easing the task of determining the expected proper operation of the design, but does not directly address the detection of potential faults. The LSSD approach is an 'ideal' design for testability solution, in that it addresses both the task of defining correct operation and the task of observing the effect of potential faults; it is also compatible with automatic test generation algorithms. However, performance and size penalties make LSSD unsuitable for many designs, and compromise approaches have been developed[7]. Regardless of the implementation, the aim in all these design for testability techniques is to facilitate both the setting and observation of internal states.

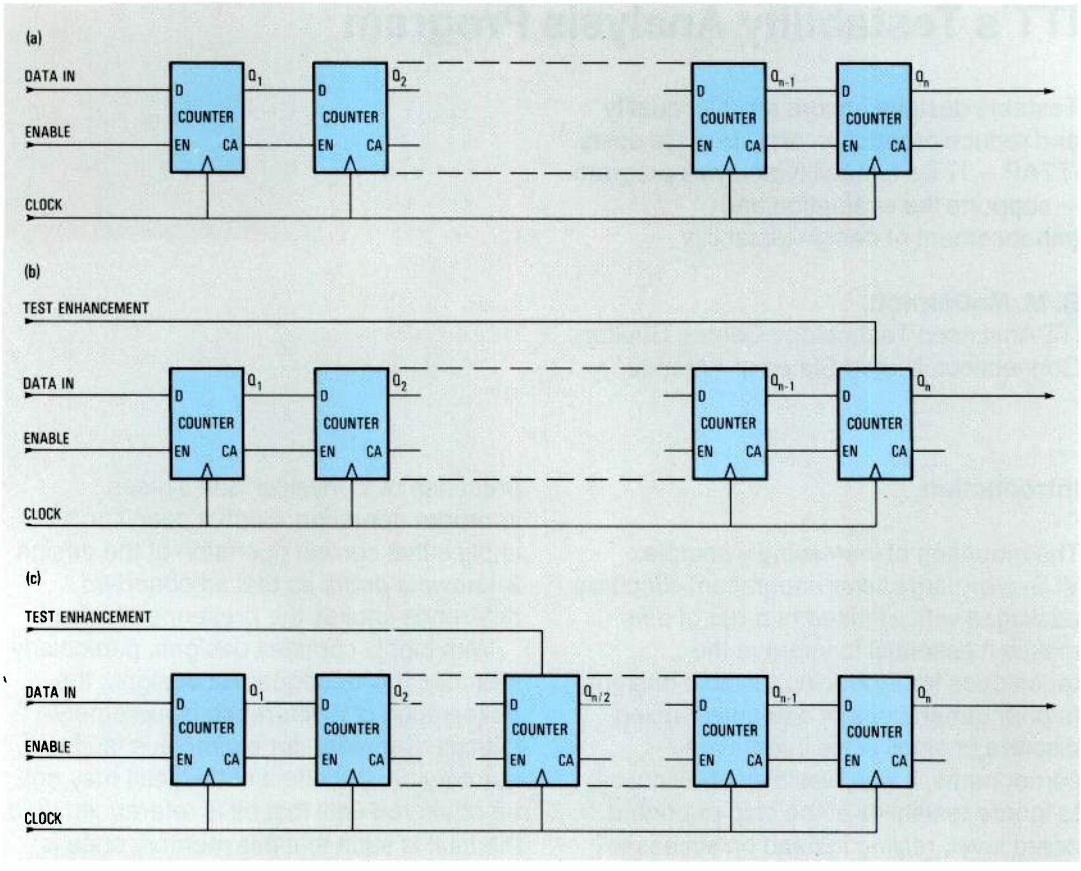


Figure 1
Testability of an *N*-bit counter.
(a) Length of test is of order *N*.
(b) After modification to improve the 'most untestable' node, the test length is reduced to order *N*-1.
(c) After modification to improve overall testability, the test length is reduced to order *N*/2.

Testability Measures

No standard, context-free measure exists for assessing a design's testability. There are, however, two standard terms of reference for evaluating a design's testability in terms of the classical design for testability guidelines:

- ease of setting internal states (controllability)
- ease of observing internal states (observability).

ITTAP, ITT's testability analysis program, evaluates a design's testability in terms of the number of different combinations of states required on the input nodes to set an internal device's state to a particular logic value (difficulty to control to 0 (DC0), and difficulty to control to 1 (DC1)), and the number of different combinations of states required on the input nodes to propagate the internal state to the output nodes (difficulty to observe (DOBS)). A design's input and output nodes are defined by the packaging: for an integrated circuit, the nodes are the input and output pins; for a printed board, the nodes may be the edge-connector pins or specified test points on the board itself.

These measures are defined for each internal node of the design, and the overall testability of the design can be defined as a combination of measures. Again, there are no standards for determining a composite measure; depending on the context, one may define an algorithm based on sums, minima/maxima, products, etc. In ITTAP, the design's overall testability is defined in terms of the average of the internal nodes' measures:

Nodal measures:

$DC0_i$ = Difficulty to control node i to 0
$DC1_i$ = Difficulty to control node i to 1
$DOBS_i$ = Difficulty to observe the state of node i.

Overall measures:

$$DC0 = N^{-1} \sum_{i=1}^{N} DC0_i$$

$$DC1 = N^{-1} \sum_{i=1}^{N} DC1_i$$

$$DOBS = N^{-1} \sum_{i=1}^{N} DOBS_i$$

Overall testability:

$$T = (DCO + DC1 + DOBS)/3.$$

The algorithms used in ITTAP to calculate the testability measures for common logic devices[2] are similar to most testability analysis tools in use today, including SCOAP, TMEAS, COPTR, and CAMELOT.

Improving Testability

Regardless of the specific algorithms used to calculate the testability measure for the design, computer-aided design tools provided for testability analysis must provide not only a report on the analysis results, but also sufficient information to assist the designer to improve a design's testability. Few, if any, existing testability analysis tools directly address this task, and some tools inadvertently mislead the engineer.

Consider, for example, an *N*-bit counter, as shown in Figure 1 (a). In relative terms, the difficulty of controlling the *i*th stage state is of order (*i*) (i.e. node Q_i requires 2^i clock cycles to change state), and the difficulty of observing the state at the *i*th stage is of order (*N*-*i*). If the testability analysis tool merely reports the measures for the nodes, one might be inclined to address the nodes that are most difficult to test in the attempt to improve testability. As one testability analysis program vendor states, 'The quickest way to improve the observability of a circuit is to place test points at those nodes that are most difficult to observe'[5]. Using this approach, node Q_1 would be made an observable test point; or, in terms of controllability, node Q_N would be made directly controllable, as shown in Figure 1 (b). While this is intended to improve testability, it is not the mechanism that should be used to improve the *overall* design's testability! If Qn is made directly controllable, or Q_1 directly observable, the difficulty measure decreases only from order (*N*) to order (*N*-1). If, however, as shown in Figure 1 (c), the *N*/2 stage is made directly controllable (even though node Qn/2 might not have been flagged as a problem node), the overall difficulty measure decreases from order (*N*) to order (*N*/2), or, in more meaningful terms, the required test time is halved.

While the determination that the *N*/2 stage is the appropriate point to partition the design is relatively clear in this simple example, more complex design enhancements may be less obvious. Consider, for example, a circuit presented in the description of the CAMELOT program for testability analysis (Figure 2)[1]. The analysis indicated that the $\overline{Q}$ outputs of the JK flip-flops were difficult to observe. After reviewing the schematic, it was determined that adding a test point at X would be an effective enhancement. While this test point is effective in addressing the 'worse' nodes, the authors demonstrate that breaking the paths at the links 1, 2, and 3 provides a more significant improvement. (Observing link 3 improves the observability of the worse nodes, as well as a few other nodes, and hence its cumulative effect on the design's testability may be greater than monitoring point X). The selection of links 1, 2, and 3 as potential test points required engineering intuition, since the output of the testability analysis program did not list these nodes as problem areas. Similarly, in Figure 3 (presented in the description of the COPTR program[5]), the Q2 flip-flop is analyzed to be a device that should be directly controlled, even though the program itself does not identify Q2 as being particularly difficult to control.

Testability analysis tools, as these examples demonstrate, can be very useful in assessing the effects of changes proposed to improve the testability of a design. The identification of key nodes as potential test points for such an assessment is, however, usually left to the designer.

Testability Enhancement Aids

To improve the effectiveness of a testability analysis tool, a companion program should be provided to assist the engineer in selecting key nodes for modification to enhance the design's overall testability. Key nodes are those that have the greatest cumulative effect on the design's controllability and/or observability.

ITTAP is such a process. Initially, in 1981, ITTAP[2] was a modified version of SCOAP[3], and merely produced the tables of testability measures for each node. In 1982 it was enhanced to include not only the nodal testability measures, but also a list, in priority order, of the nodes that would have the greatest cumulative effect on testability.

Identification of the nodes that have the greatest cumulative effect is straightforward: it is based on automating the 'what-if' analysis the engineer would perform with a standard testability analysis program. The design is iteratively processed for each node at the highest level of the hierarchy, to determine the resultant testability if that node were included as a directly controllable/observable input or output pin. The 'what-if' analysis is performed twice: what if the node were directly controllable (i.e. forcing a value from the input pins); and what if the node were directly observable (i.e.

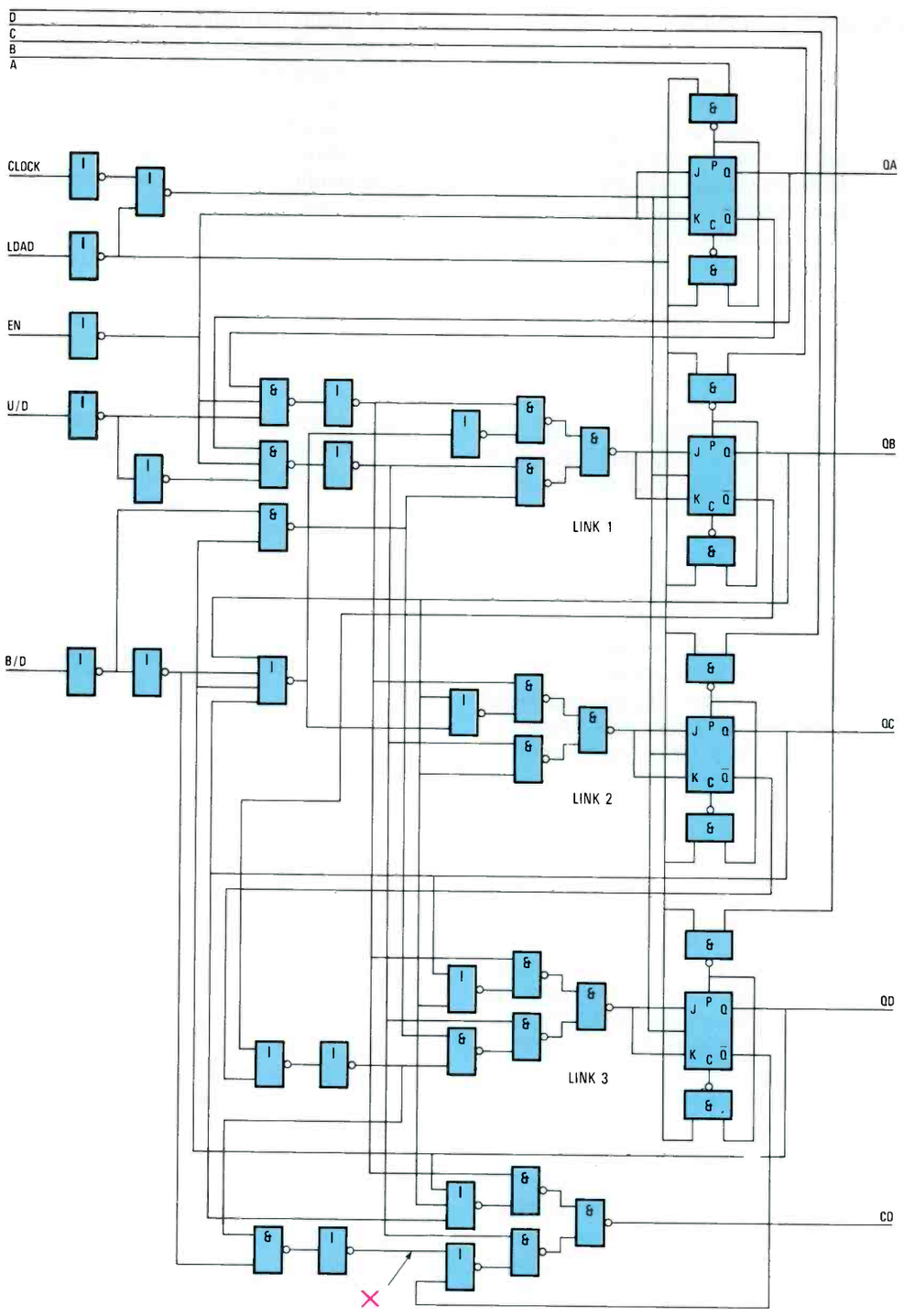


Figure 2
Up-down counter circuit used in a description of the CAMELOT program[1].

monitored as an output pin). Figure 4 is the flowchart of this process.

In the case of the CAMELOT and COPTR circuits, for example, each node on the schematic, one at a time, is assumed to be a possible test point and the resultant testability is computed; after all the nodes have been processed in this manner, the nodes producing the best testability are reported to the user. In the case of the *N*-bit counter example, each node in the schematic is analyzed; nodes within the individual counter blocks are included in the computation of the testability measures, but not in the list of nodes for consideration as potential test points.

The designer is presented with the list of key nodes for a determination as to whether

it is feasible (based on performance impact) to modify these nodes. The program does not redesign the circuit, but points out recommended changes for improved testability. Redesign of the circuit may involve the addition of blocking or forcing gates to provide direct control of an internal node, changing sequential devices to daisy-chained LSSD devices, multiplexing internal signals to an output pin, etc.

ITTAP includes algorithms for computing the testability measure; however any other testability analysis tool could be used in this testability enhancement scheme, provided that such an exhaustive evaluation is cost-effective. ITTAP is particularly cost-effective in that it uses a 'selective trace' concept similar to that used in event-driven simulators. When a node is considered for inclusion as a test point, only the nodes affected by this node are re-evaluated. This approach provides built-in efficiency: nodes that affect only a few other nodes are processed quickly, whereas nodes having a large effect take longer to process (i.e. ITTAP spends time only on those nodes which warrant consideration).

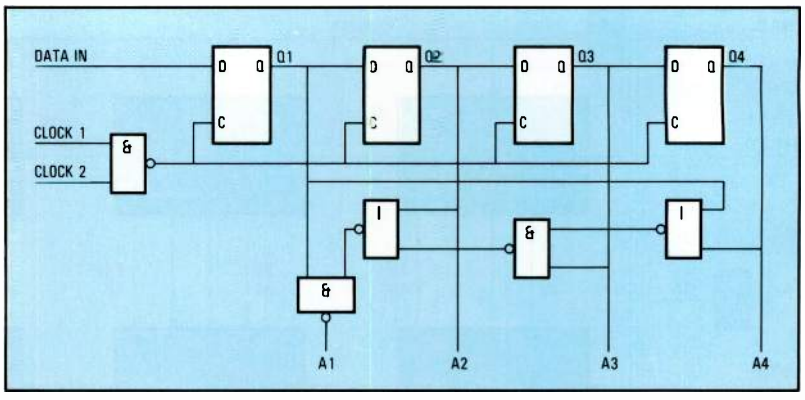


Figure 3
Shift register circuit presented in a description of the COPTR program[5].

Results

When applied to the examples discussed above, ITTAP successfully identified the *N*/2 node as having the most impact on the *N*-bit counter's testability, identified links 1, 2, and 3 as key nodes for improving the CAMELOT circuit, and identified Q2 as a key node for the COPTR circuit. (Possibly owing to a difference in the methods of calculating testability, ITTAP recommended link 1 as the best node for modification, and after link 1 was included as a test point, link 3 and link 2, in that order; in the COPTR circuit, ITTAP identified Q3 as a slightly better choice than Q2). The key fact, however, is that ITTAP *automatically* identified these key test points while other testability analysis programs require detailed manual analysis.

ITTAP was also applied to a real integrated circuit design (Figure 5, circa 1977) that had been used as a training circuit for ITT designers. As part of a training course, senior test engineers were asked to analyze a design in order to find ways to improve its testability. The consensus of the test engineers was that the 12-bit counter should be partitioned into three 4-bit counters for improved controllability, and the 12-bit comparator should be monitored at intermediate points for improved observability. As an initial test in 1982, ITTAP was used to analyze the same design (Figure 6), with the following results:

- The two nodes recommended by the senior test engineers for improved controllability were the first two nodes recommended by ITTAP.
- The two nodes recommended for improved observability were the first two nodes recommended by ITTAP.

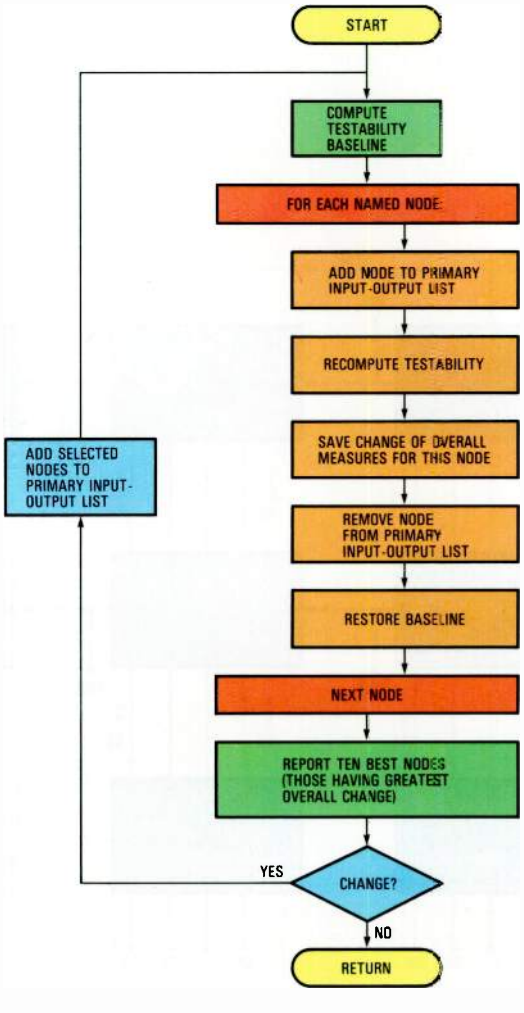


Figure 4
Testability enhancement algorithm (repeated twice – key nodes for improved controllability, key nodes for improved observability).

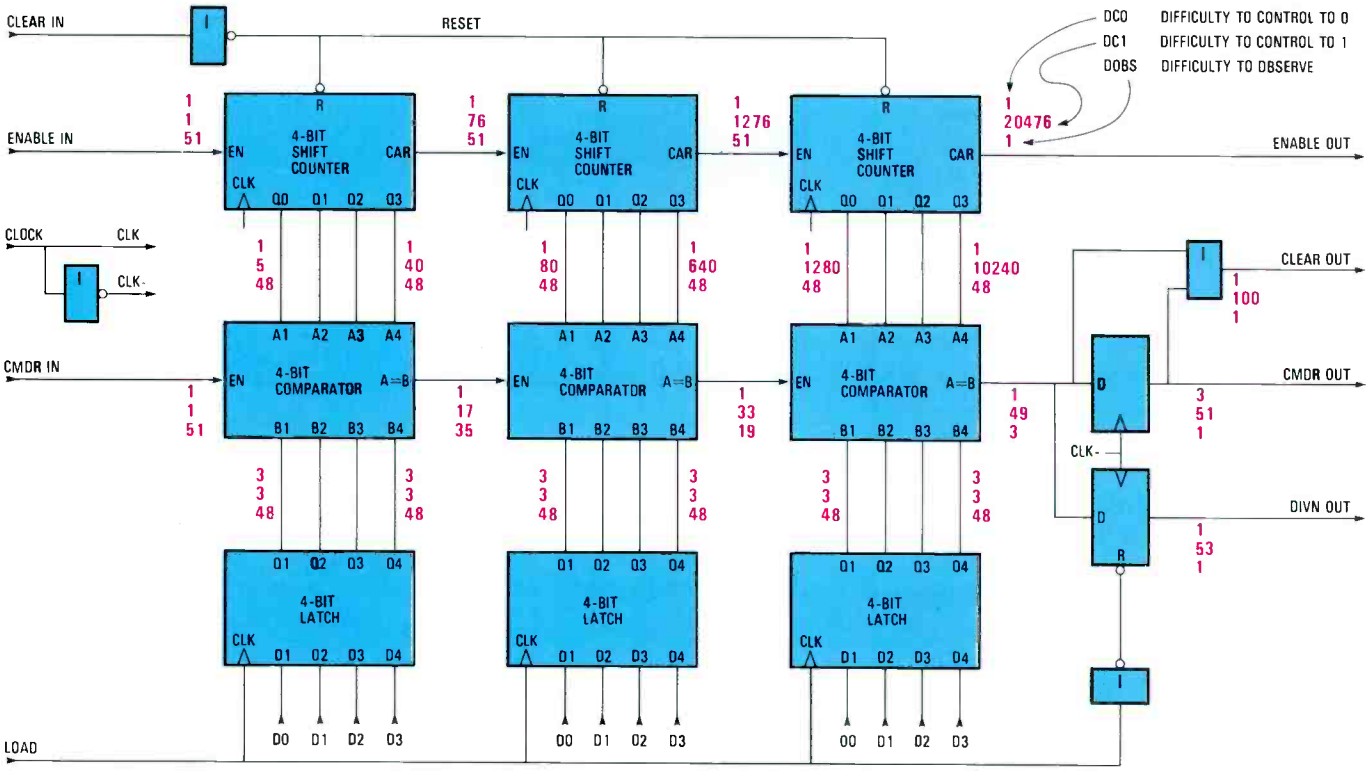
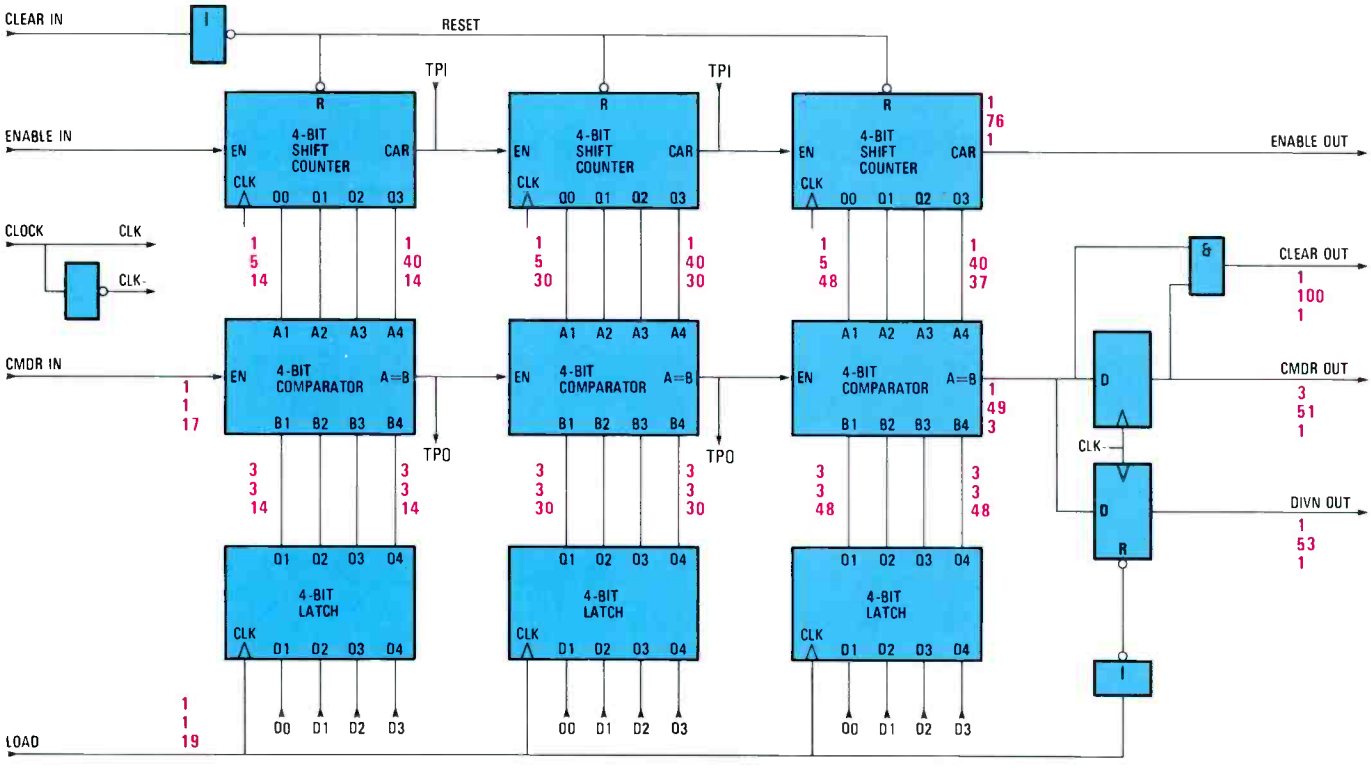


Figure 5
12-bit modulus counter – nodal testability measures.

Figure 6
12-bit modulus counter – average testability after adding CO4 and CO8 as PI, and CM4, CM8 as PO.



- After the recommended nodes were included as test points, the ITTAP analysis showed that subsequent changes would have minimal effect on the design's testability.
- The exhaustive analysis for each of the 50 named nodes, including the re-evaluations after selecting the recommended nodes, required less than 30 seconds of central processor time on a Prime 750 computer.

Conclusions

Most available testability analysis programs are useful in assessing the testability of a design; the differences between them are in the criteria and algorithms used to define the testability measure.

To be an effective tool for assisting in the improvement of a design's testability a program must be capable of not only assessing the testability measures, but also *automatically* identifying the nodes which have the greatest impact on these measures. The ITT testability analysis program provides this capability and has been demonstrated to be consistent with the results of expert test engineers for improving design testability.

References

1 R. G. Bennetts, C. M. Mauder, and G. D. Robinson: CAMELOT: a Computer-aided Measure for Logic Testability: *Institution of Electrical Engineers Proceedings,* September 1981, Volume 128, Pt.E, No. 5, pp 177–189.

2 D. K. Goel and R. M. McDermott: An Interactive Testability Analysis Program – ITTAP: *Proceedings, 19th Design Automation Conference,* June 1982, pp 581–586.

3 L. H. Goldstein: Controllability/Observability Analysis for Digital Circuits: *Institute of Electrical and Electronics Engineers Transactions,* 1974, CAS-26, pp 685–693.

4 J. Grason: TMEAS – a Testability Measurement Program: *Proceedings, 16th Design Automation Conference,* June 1979, pp 156–161.

5 T. Kirkland and V. Flores: Software Checks Testability and Generates Tests of VLSI Design: *Electronics Magazine,* March 10, 1983.

6 E. B. Eichelberger and T. W. Williams: A Logic Design Structure for LSI Testability: *Proceedings 14th Design Automation Conference,* June 1977, pp 462–468.

7 G. W. Jacob: Designing for Testability: *Electrical Communication* (1984), volume 58, no 4, pp 427–432 (this issue).

Robert M. McDermott was born in Brooklyn, New York, and received a BEE degree from City College of New York, an MS degree in systems analysis from George Washington University, and an MS degree in computer science from the Polytechnic Institute of New York. After serving as a communications officer in the US Army for five years, and as a test engineer at the US National Security Agency for three years, he joined ITT in 1978. He is at present manager, computer assisted design, at the ITT Advanced Technology Center in Shelton, Connecticut.

VLSI Packaging

Increased pin counts, speed, and power dissipation require changes in VLSI packaging materials, processes, and shapes. Plastic packaging is gaining ground relative to hermetically sealed devices, particularly for less stringent applications.

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Introduction

Packaging is the most expensive stage in semiconductor manufacture for LSI and VLSI (large and very large scale integration) devices, as well as for discrete transistors and diodes. At the same time, most failures of a mature semiconductor device are caused by the packaging. Thus semiconductor packaging must offer an optimal compromise between reliability and cost. The package provides the mechanical and electrical interface between the chip and the printed board, as well as protecting the chip and helping heat dissipation.

The progress towards smaller feature sizes and increased complexity is leading to higher pin counts, greater power dissipation, and higher bit rates or operating frequencies. In addition, smaller feature sizes increase the sensitivity of the chip surface to mechanical damage and corrosion.

Today packaging decisively affects the electrical performance of high speed VLSI devices. In the case of standard VLSIs, packaging is a task for the semiconductor manufacturers as such components are purchased by the user in packaged form. A different situation exists for custom VLSI devices. It makes sense for system houses to design, package, and test such devices in-house. This approach simplifies the interface to the semiconductor manufacturer and allows packages to be optimized. On the other hand, it forces system houses to deal with all the problems involved in packaging.

Packaging Objectives

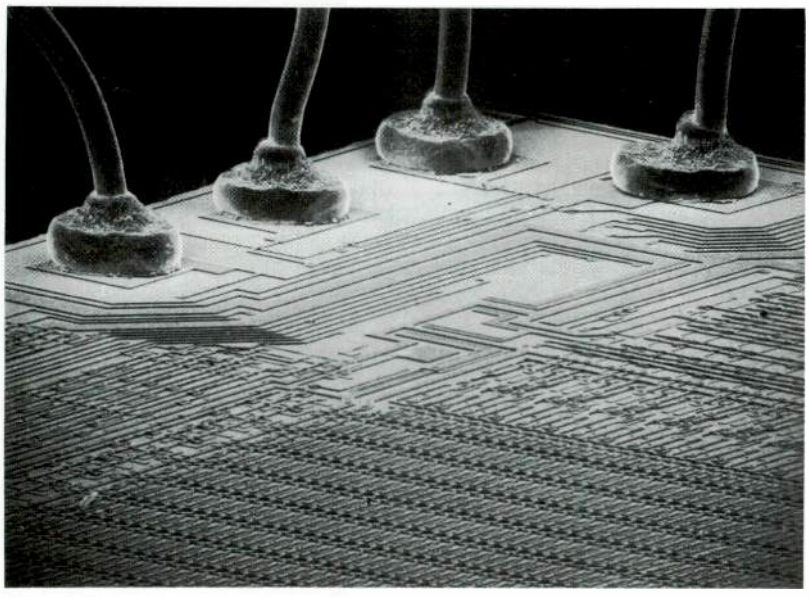
As already indicated, the package mechanically and chemically protects the chips and bond wires, and helps dissipate heat. In addition it facilitates complete functional testing and acts as an interface between the micro connections on the chip and macro connections on the printed board. Finally it simplifies mechanical manipulation during the assembly of printed boards.

During the selection of packaging materials, processes, and shapes, the characteristics of the chip, printed board, and board assembly process must all be taken into account.

Interconnection Between Chip and Package

The connection between chip and package serves for mechanical fixing, heat dissipation, and electrical connection. Normally the chip is bonded to the package base, so the connection has to provide high thermal conductivity without generating unacceptably high mechanical stress. Silicon has a low thermal expansion coefficient. Figure 1 shows that none of the commonly used packaging materials combines low thermal expansion with high thermal conductivity.

At present, the most important packaging materials are alumina and kovar. Beryllium oxide ceramic has a high thermal conductivity, but is expensive and poisonous and therefore rarely used. Recently, aluminum nitride ceramic materials have been developed; these have coefficients of thermal expansion close to that of silicon, and thermal conductivities as good as, or even better than, beryllium oxide. It has to be seen whether such materials come into practical use for VLSI packages.



Gold-wire bonds.

At present, VLSI chips are bonded to the package using either solder or adhesives. In the case of soldering, the bottom of the chip and package base are both coated with a thin layer of gold; gold-silicon eutectic with a melting point of 390°C is used as the soldering material. Solder bonding produces a good mechanical bond with a high thermal conductivity, but the rigid connection creates mechanical stress which can affect the electrical parameters or even cause the chip to crack. Thus soldering is advisable only for chips with an area of less than 30 mm^2.

Polyimide adhesives with a silver filler are generally used for adhesive bonding, which is a low-cost process. The plasticity of the adhesive prevents mechanical stress, but the thermal conductivity is low and the adhesive is unstable above 400°C. Adhesive bonding should therefore be avoided where high-temperature package sealing is used.

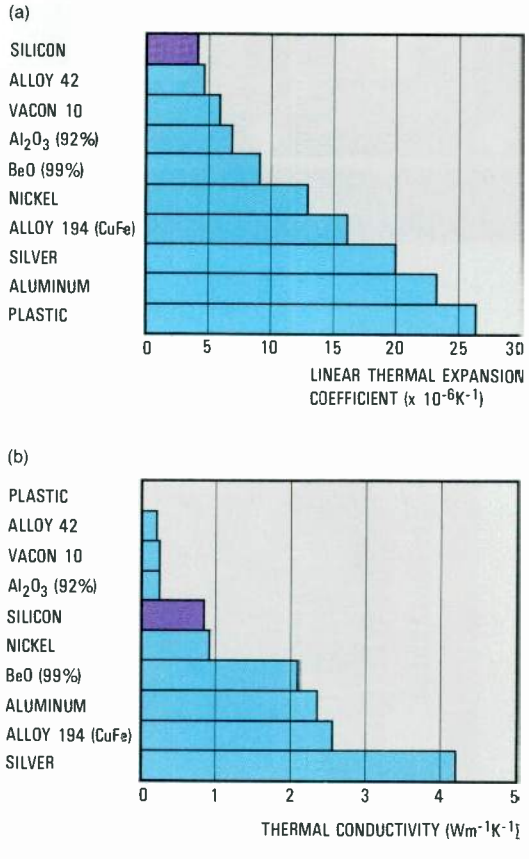


Figure 1
Characteristics of typical VLSI packaging materials (a) coefficient of thermal expansion and (b) thermal conductivity.

Electrical Connections

VLSI chips incorporate pads for electrical connections at the chip periphery: generally they are of evaporated aluminum with a thickness of 1 to 2 μm. Their dimensions are between 0.1 × 0.1 mm and 0.14 × 0.14 mm. Gold or aluminum wires are used for wire bonding. In the former case, a small ball is made by melting the wire end in a flame. This ball is then connected to the pad by thermal compression at about 200°C.

The strength of this connection exceeds 0.05 N. However, at temperatures above 370°C, gold-silicon eutectic forms so that gold-wire bonding is only feasible if the package sealing temperature is below 370°C. Furthermore, above 200°C an intermetallic aluminum-gold compound forms at the boundary between aluminum and gold – the so-called "purple plague" effect. This compound is brittle and can cause breakage, making gold-wire bonding unsuitable for applications where the junction temperature normally exceeds 200°C.

Aluminum wires are bonded ultrasonically. The bond strength is around 0.02 N, but depends very much on the bonding conditions. Careful production control, the need to orientate the bonding tool, and the lower bonding speed make this technique considerably more expensive than gold-wire bonding. Also, aluminum-wire bonding is not suitable for plastic packaged VLSI devices because of high adhesion between plastic and wire, low bond strength, and the danger of wire corrosion.

Wire bonding is carried out serially and requires precise adjustment between bond pad and bonding tool. If this is done manually, yields are low, particularly in the case of high pin counts. To overcome this, VLSI bonding is mainly performed by automatic bonders. Their high cost is

justified by high production yields and a considerable improvement in reliability.

The steady increase in pin numbers has led to a concerted search for a parallel interconnection technique. At present TAB (tape automated bonding) is the most promising parallel interconnection method, and has been studied extensively at the ITT Advanced Technology Center in Shelton and Bell Telephone Manufacturing Company in Ghent. TAB uses protruding metal bumps on the chip interconnection pads and precisely etched interconnection "lead frames". A 25 μm high gold bump is created galvanically on each aluminum pad (Figure 2). The "bumping" is done on the silicon wafer before separation into chips and is therefore relatively inexpensive. Next a copper tape foil is precisely etched into a lead frame and gold plated. Sprocket holes enable the foil to be precisely adjusted to the chip. A heated press tool then makes a thermocompression bond to all pads on the chip simultaneously. After this inner lead bond, full electrical testing of the chip is possible, ensuring a higher yield for the final packaging process. The next step is the outer lead bond between the lead frame and package pads.

TAB gives a bond strength of 0.5 N or more and a precise wiring geometry. It also produces a low and controlled characteristic impedance of the interconnection between package and chip. However, the high cost of TAB equipment and chip tooling limits its use to high volume production.

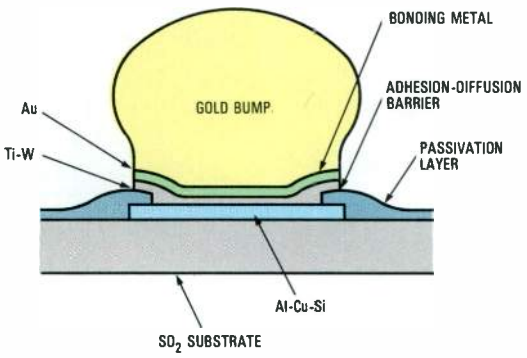


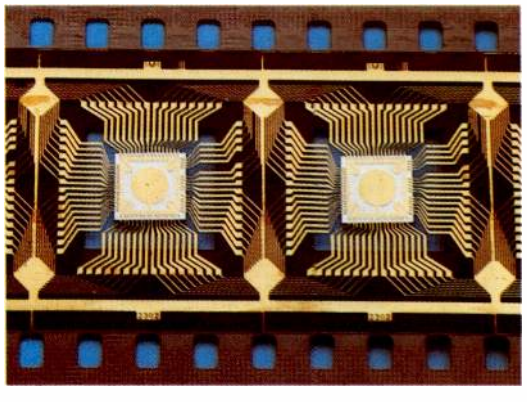
Figure 2
Tape-automated bonding pad (cross-section).

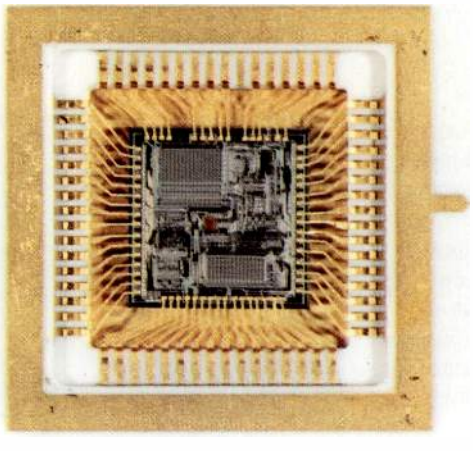
Mechanical and Chemical Chip Protection

The chip surface must be protected against mechanical and chemical damage during manufacture and in operation. The metal interconnections on the chip surface are particularly sensitive to such damage. This sensitivity increases considerably as feature sizes decrease. MOS circuit gates require additional protection against Na^- and K^-ions.

Normally two-stage protection is used: a passivation layer on the chip surface and the package itself. The chip passivation layer consists of a thin layer of glass applied directly to the semiconductor wafer to protect the chip against damage during testing, chip separation, and bonding. Normally vacuum-deposited SiO_2 (or Si_3N_4) layers with a thickness of between 1 and 2 μm are used. The higher the surface temperature during deposition, the better these layers are. Good results have been achieved with layers deposited at about 800 °C.

VLSI circuits with feature sizes below 3 μm do not allow such high temperatures to be used after the diffusion stages because of the high diffusion gradients needed. Plasma deposition of Si_3N_4 at wafer temperatures of 200 °C is preferred for VLSI devices. Currently available materials do not provide perfect chip passivation. In particular, the quality of the passivation layer must be improved for high quality





Tape-automated bonding
top: **lead frame with bonded semiconductor chips, and** ***bottom:*** **bonded chip with inner and outer lead bonds.**

plastic encapsulated VLSI devices. Cracks and pinholes in the passivation layer allow moisture to corrode the metallization. Very good passivation layers have recently been achieved at BTM and at Deutsche ITT Industries.

Even if perfect chip passivation is achieved, pad corrosion remains. Prior to wire bonding, the passivation layer has to be removed at the bond pads. Pads with gold-wire bonds are particularly sensitive to galvanic corrosion. One major advantage of TAB is that the gold bump prevents such pad corrosion.

Package Materials

High reliability and long lifetimes under adverse conditions require hermetically sealed packages. The base part of VLSI packages consists of alumina which, together with the lid, forms a cavity that houses the chip and bond wires. The package is sealed using low melting point glass or soldering. Electrical connections between the outside and the cavity are made by thick or thin film metal layers. The main reliability problems are caused by humidity which can be sealed in, particularly during glass sealing. Humidity can also enter the cavity through leaks, so fine leak testing of hermetically sealed VLSI devices is advisable.

Non-destructive humidity testing of hermetically sealed packages can be done by measuring the dew point using a technique developed at the Standard Elektrik Lorenz Research Center in Stuttgart. The leakage current of a diode at the input or the output of a VLSI is measured as a function of temperature. As the leakage current increases at the dew point, the curve of leakage current versus temperature gives a good indication of the amount of sealed-in moisture (Figure 3). A dew point below −20°C is required to ensure high reliability.

In cases where the reliability and ambient condition requirements are less stringent, plastic encapsulation can be used. Here the chip is bonded to a kovar lead frame using gold-wire bonding. Finally the chip, bond wires, and part of the lead frame are covered by a plastic material. All plastic material is permeable to water to some extent, allowing water to penetrate to the chip, especially at the interface between metal and plastic. The time constant of water penetration depends upon the material, geometry, and temperature. Generally it is about 1 000 hours. Humidity together with impurities in the plastic material can cause chip corrosion. Power dissipation in chips that are in operation normally increases the chip temperature, thereby reducing humidity at the chip surface and preventing galvanic corrosion. However, this is only the case as long as the chip operates continuously. The danger of corrosion rises dramatically during intermittent operation[1].

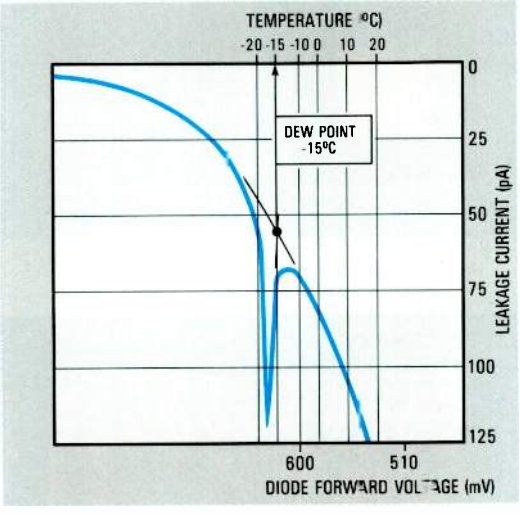
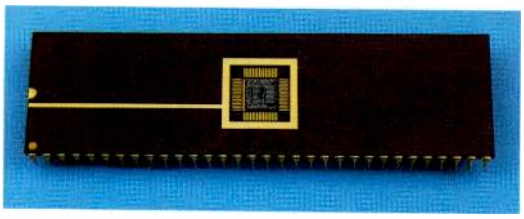


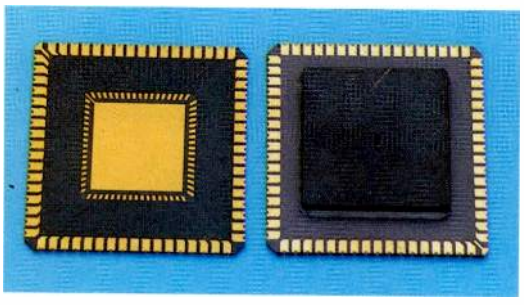
Figure 3
Dew point measurement based on measuring the leakage current of an input diode as a function of the ambient temperature.

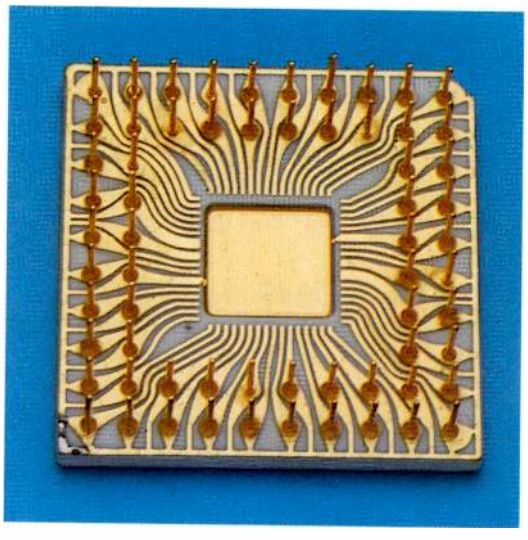
The direct connection between the chip surface and plastic material also produces mechanical stress because of the mismatch in the thermal expansion coefficients of silicon and plastic (Figure 1). This mismatch can also cause breakage of lead connections. Plastic packages have been produced by Deutsche ITT Industries for many years, and have achieved good reliabilities.

Connection from Package to Printed Board

The package type and material must be matched to the printed board technology, particularly with respect to the shape, pitch, and location of the pins. Low pitch requires expensive printed board technologies, while a high pitch might result in unacceptably large package dimensions. As the use of different printed board and package materials causes mechanical stress, most VLSI packages use flexible leads or pins. Leads of low-pitch packages show poor mechanical stability because of limitations in the pin dimensions, possibly resulting in increased production costs.







VLSI package types top: dual-in-line package with 64 pins, center: chip carrier with 68 pins, and bottom: pin grid package with 64 pins.

The present state of the art of printed boards allows two or three interconnection lines to pass between two solder connections with a 2.5 mm pitch. A pitch reduction to 1.25 mm no longer allows feeding through of interconnection lines. Thus long lines of solder connections with a pitch of 1.25 mm on the board results in blocking of interconnections. It might be difficult to desolder large area packages without impairing the printed board, thereby adversely affecting repairability.

Package Types

Three main types of package are used for VLSI devices. The dual-in-line package has become a worldwide standard for VLSIs with up to 24 pins. Pins are arranged in two rows with a pitch of 2.54 mm. Standard printed boards can mount these packages without difficulty. However, this type of package becomes rather large when there are more than 48 pins.

The chip carrier can be considered as a square dual-in-line package with connections on all four sides at a pitch of 1.25 mm. Package area increases with the square of the pin number, so the dimensions become too large when there are more than 100 pins. As normal printed board technology does not allow interconnection lines to be fed between solder connections with a pitch of 1.25 mm, the area of the printed board underneath the package cannot be used for interconnections.

The leads of leaded chip carriers are fragile, so leadless chip carriers have been introduced. Their use is recommended if the other components on the board are also leadless. If there are more than 32 pins, stress problems occur as a result of mismatch of temperature or thermal expansion coefficient between package and board.

For high pin numbers the pin grid package is technically the best solution. The pins are rather rugged and arranged in a two-dimensional grid with a pitch of 2.54 mm; package area is proportional to the pin number. The printed board area underneath the package can be fully utilized for interconnections. The pins reduce any stress between package and board to tolerable values. At present the main disadvantage of this package is its high price.

Performance of Different Package Types

Figure 4 shows the areas of different package types as a function of the pin count. For high counts, pin grid packages require the least printed board area. However, for high speed systems the lengths of the interconnection lines between chips are even more important. Signal delay time between two semiconductor chips on a printed board depends on the lengths of the signal lines within the package and on the boards, as well as on the dielectric constants of the package and board materials.

The signal transmission speed on a conductor in an alumina package is a factor of three lower than for a line in free air. On epoxy multilayer printed boards, this factor is 1.6. If, for example, 12 VLSI devices are interconnected on one printed board, the maximum length of interconnection lines

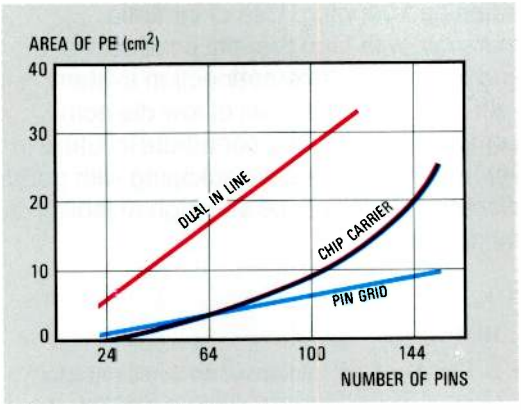


Figure 4
Printed board area required by the dual-in-line, chip carrier, and pin grid VLSI packaging techniques.

and the signal delay will depend on the pin count and type of package. Figure 5 shows the signal delays on the longest signal lines, assuming that connections exist between all 12 VLSI devices on the board. The pin grid package offers the least printed board area and lowest signal delay when there are a large number of pin connections.

Both printed board area and signal delay can be reduced by decreasing the packaging pin pitch, but this leads to more severe requirements on the printed boards and the manufacturing process and thus to higher costs. It could also cause reliability problems as a result of galvanic corrosion between pins at the package surface.

Thermal Problems

In large electronic systems, VLSI devices are normally connected to printed boards, which are themselves plugged into racks. Heat from the chip is carried via the leads to the printed board and via the package surface to the surrounding air. If the power dissipation per printed board is below 5 W, the temperature difference between package surface and ambient air can be kept below 20°C. Higher power dissipation requires additional cooling using fans or cooling fins, for example. Printed boards based on ceramics or enamelled steel considerably improve heat dissipation. As the failure rate of VLSI dramatically increases with chip operating temperature, heat dissipation becomes a severe problem for complex very high speed systems. The volume used for heat dissipation has to be kept small to keep signal wire lengths short, so the method of cooling determines the speed-complexity product of the system. In the same way as water cooling is used for high speed computers, liquid cooling might also be used in future for VLSI devices in telecommunication systems.

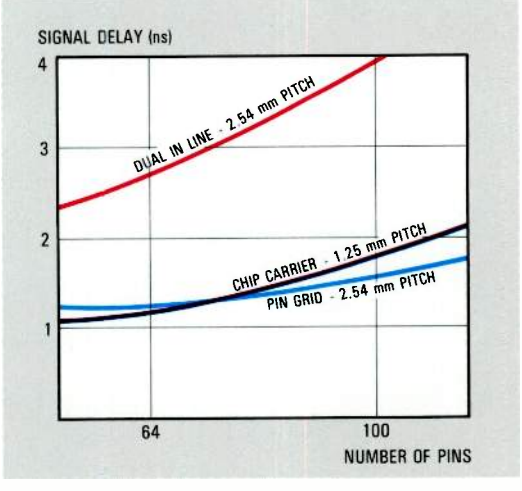


Figure 5
Maximum interconnection line delays between 12 chips on a printed board using the dual-in-line, chip carrier, and pin grid packaging techniques.

Future Trends in VLSI Packaging

Materials

For VLSI devices with up to 64 pins the trend is towards plastic packaging. Improvements in plastic materials and in chip surface passivation have led to a major reduction in the field failure rates of plastic packaged VLSI devices. A major problem with such devices is that from time to time production lots exhibit unexpectedly high failure rates resulting from changes in plastic materials and imperfect chip passivation layers. Thus qualification and lot acceptance by accelerated life tests must be performed far more carefully than with hermetically sealed devices. There is general agreement that a 1 000 hour test at 85°C and 85% relative humidity (85/85 test) is a fair equivalent of a 20-year operating life under benign field conditions. Unfortunately the long duration of this test does not allow it to be used for acceptance testing. Work is now under way in ITT to modify the pressure cooker test method so that good correlation with the 85/85 test can be achieved. It is expected that pressure cooker tests will become the accepted method for lot acceptance testing.

New Packaging Materials

Materials such as polyimides or silicones that provide a water repellent surface could further improve the reliability of plastic encapsulated VLSI devices. It is also possible to replace plastic by a water impermeable material such as low melting point glasses. Direct glass encapsulation of transistors and small scale integrated

circuits has been used at Standard Elektrik Lorenz for quite some time, and it is anticipated that its use can be extended to VLSI circuits. Under adverse ambient conditions this technique could offer the reliability of hermetically sealed devices at the cost of plastic packaging.

For complex, very high speed applications, hybrid packaging might be the way to go. The extension of a ceramic package base in such a way that it can accommodate several chips has been used for some time in applications where small size is mandatory even at the expense of high cost. To make such solutions economical it is necessary to achieve a low cost, high density interconnection system on the substrate and to ensure repairability. This means that it must be possible to replace a VLSI chip from the substrate at low cost without impairing reliability. Tape-automated bonding is a good candidate for such hybrids because of the capability of complete chip testing and burn-in after inner lead bonding. Use of ceramic materials with high thermal conductivities and a multilayer interconnection system with insulating materials of low dielectric constant will hopefully contribute in future to achieving high density packaging with good electrical performance and high reliability at moderate cost.

Reference

1 D. Stroehle: Plastic-Encapsulated Semiconductor Components for Telecommunication Systems: *Electrical Communication*, 1982, volume 57, no 2, pp 152–156.

Hans Reiner was born in 1927 in Stuttgart, Germany. He studied physics at the University of Stuttgart where he obtained the degree of Dipl-Phys in 1951. The same year he joined SEL where he is now manager of the Telcom Systems Technology Division of the SEL Research Center. He is visiting professor at Karlsruhe University and chairman of the professional group on VLSI quality and reliability of the Nachrichtentechnische Gesellschaft.

Video Codec for Broadband Communication

New broadband services require codecs for the transmission of combined video, sound, and data. A codec design to be implemented in VLSI CMOS technology uses differential pulse code modulation to halve the bit rate.

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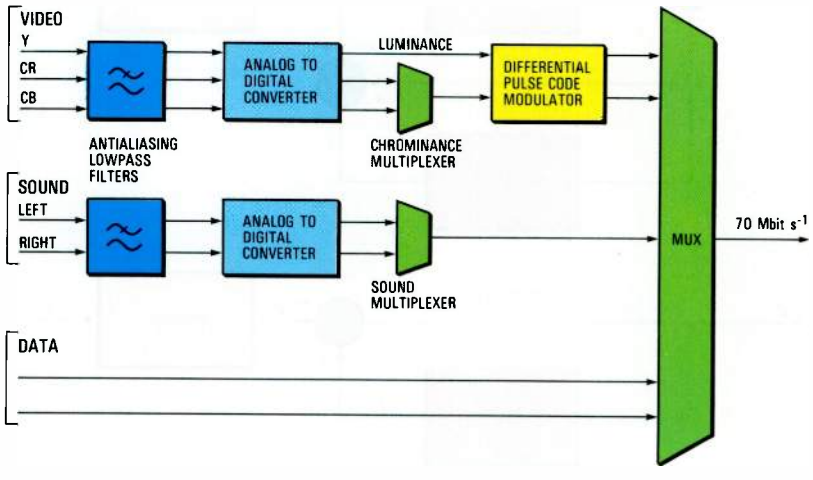
Introduction

Optical fibers offer a communication network which includes new broadband services such as television distribution, videophone, and videoconference, in addition to telephone and data services. Very large scale integration (VLSI) technology is ideally suited to the design and production of the large number of video codecs demanded by these new services.

Broadband communication systems are needed which transmit two video signals with sound and additional data channels, within the fourth-order European PCM (pulse code modulation) hierarchy operating at 140 Mbit s^{-1}. A transmission rate of about 70 Mbit s^{-1} for each television channel can be achieved by using DPCM (differential pulse code modulation). Television coding at bit rates below about 70 Mbit s^{-1} is not considered here because of the higher cost of producing such a codec and the reduced picture quality. An appropriate design of the DPCM codec reduces the bit rate by a factor of two while maintaining the required high picture quality. To allow integration of services in addition to television, some integrated services digital network and 2 Mbit s^{-1} channels should be available. In videoconferencing, these additional channels could be used for the transmission of graphics, text, or other data.

Interactive distribution services other than television also require broadcast sound distribution and videotex. Interactive television distribution allows the subscriber to select two channels out of the set of available channels by controlling a broadband switch in the central exchange. This needs a link from the subscriber to the central exchange for remote control information. The proposed exchange configurations require multiplexing of the subscriber signals in two stages. Prior to the exchange stage each of the video signals, with accompanying sound and data, is multiplexed into a 70 Mbit s^{-1} data stream. Following the exchange stage, two 70 Mbit s^{-1} data streams are combined for transmission on the subscriber link.

Figure 1
Block diagram of a 70 Mbit s^{-1} video codec.



Video Codec

The video codec has to digitize television and sound signals and apply DPCM in order to reduce the bit rate for the television signals. Further, television signals with sound and additional digital data have to be multiplexed into a 70 Mbit s^{-1} bit stream. A block diagram of the video codec is shown in Figure 1. Component coding of the television signal is assumed, providing a luminance signal Y and two chrominance signals $CR = R - Y$ and $CB = B - Y$. The analog signals are lowpass filtered to avoid aliasing and then converted to digital form. A reduced number of transistor functions for implementation can be achieved by an

appropriate choice of sampling frequencies. Based on the allowable complexity, sampling frequencies of 10.125 MHz for luminance and 3.375 MHz for chrominance were chosen. These sampling frequencies provide a picture quality which is higher than that given by composite coding with PAL. Each video sample is quantized to 8 bits. The application of DPCM reduces the number of bits per sample to four. The two chrominance signals are multiplexed and transmitted sequentially to simplify design.

Two television sound channels are foreseen, allowing the transmission of either one stereo signal or two mono channels which could carry different languages. Each sound channel is sampled at 32 kHz and linearly quantized to 16 bits. To simplify the multiplexing scheme, sound and all additional data channels are transmitted synchronously; sound and data clocks can be derived by division from the net clock of 139.264 MHz. Because the video signal is not synchronized to the net clock, a frame structure is required which reserves sufficient frame space for the video signal. Figure 1 shows the functional blocks of the television coder at the transmit side. The television decoder at the receive side performs the inverse operations in reverse order.

The aim is to integrate the video codec into the minimum number of chips. Initially only digital sections such as the DPCM codec, multiplexer, and demultiplexer will be realized using custom designed chips. Future investigations will be directed at VLSI implementation of the other parts, which at present use standard components.

DPCM Codec

The bit rate of the video signal is reduced by DPCM codecs[1]. The basic DPCM system is shown in Figure 2. By subtracting a prediction value $\hat{s}$ from the input sample s, a prediction error e is formed which is then quantized and coded for transmission. At the receiver, the sample s is reconstructed by adding the prediction value to the quantized prediction error e'. Prediction is based on reconstructed samples s' at both transmitter and receiver to give the same prediction values.

The simplest predictor uses the previous sample, which can be realized with a single delay element. Better prediction is achieved by using two-dimensional predictors, which requires a delay line. Two-dimensional linear predictors and a quantizer table with 16 representative levels are necessary to achieve the required picture quality.

Most of the transistors in the DPCM integrated circuit are required for the delay line. As an example, the luminance signal requires 540 samples of 8 bits to be stored. Using four-transistor dynamic random access memory cells for the delay line, the complexity of delay control is relatively low.

One speed bottleneck in the DPCM codec is the recursive loop. Very fast arithmetic hardware is required to calculate the prediction value and complete the loop in one clock period. To simplify prediction, weighting factors are restricted to powers of two, allowing multiplication by hardwired shift operations. Even then the time-critical path consists of one register, one subtractor, two adders, and the logic for quantizer and limiter. For a clock frequency of 10.125 MHz the total delay of all functions has to be less than 98 ns.

Timing constraints can be further relaxed by modifying the DPCM codec as shown in Figure 3. Insertion of a selector (Figure 3) allows receiver and transmitter functions to be performed by a single circuit. A delay estimate has shown that the realization of this modified DPCM codec requires a CMOS technology which ensures a delay of less than 1.3 ns for an inverter with a fanout of one[2]. The characteristics published by semiconductor manufacturers indicate that a 2 μm technology can meet this requirement.

In conclusion, by modifying the architecture and optimizing the logic, an integrated circuit realization of the DPCM

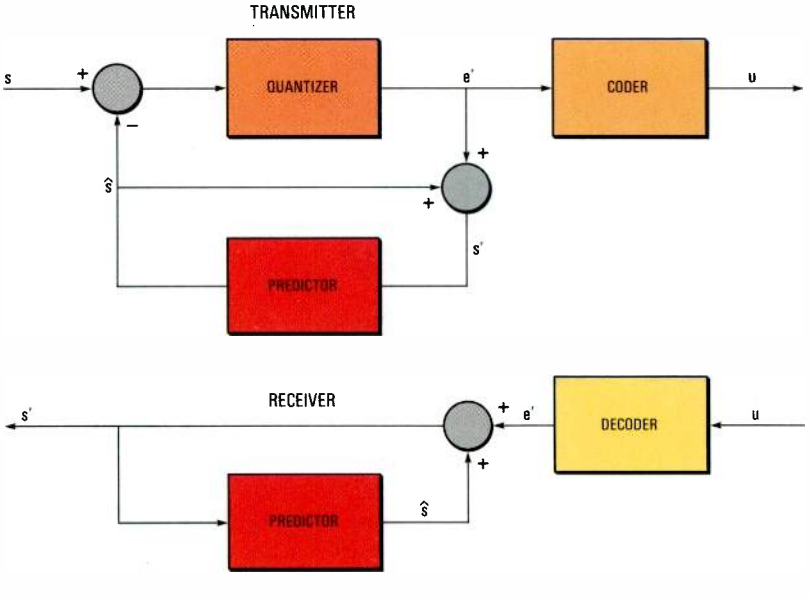


Figure 2
Block diagram of a DPCM system.

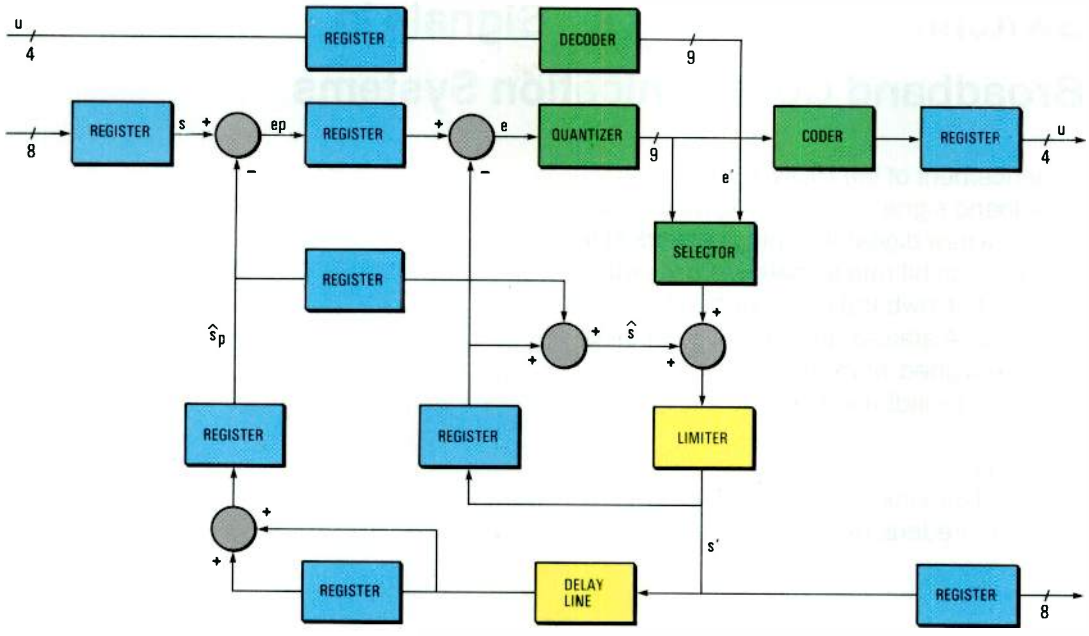


Figure 3
Functional blocks of luminance DPCM codec in its modified form.

codec is possible using available CMOS technology.

References

1 A. N. Netravali and J. O. Limb: Picture Coding: A Review: *Proceedings of the Institute of Electrical and Electronics Engineers*, March 1980, volume 68, pp 366–406.

2 S. Drews, P. Pirsch, and K. Schaper: Circuit Technique for VLSI Design of a Video Codec: *Conference Record ICC '84*, Amsterdam 1984.

Peter Pirsch was born in 1942 in Hanover, West Germany. He was awarded an Ing-Grad from the Fachhochschule Hanover in 1966, and Dipl-Ing and Dr-Ing degrees from the University of Hanover in 1973 and 1979, respectively. He worked in the television department of Telefunken between 1966 and 1973 when he joined Hanover University as a research assistant, and then a senior engineer. From 1979 to 1981 he spent a sabbatical leave working in the visual communication research department of Bell Laboratories. Dr Pirsch joined the SEL Research Center in Stuttgart in 1983 as head of the signal processing department.

Switching of 140 Mbit s^{-1} Signals in Broadband Communication Systems

Enhancement of the ISDN to carry broadband signals of up to 140 Mbit s^{-1} will require a new digital switching network able to carry high bit rate signals yet work with existing narrowband and wideband networks. A state-of-the-art MOS circuit is being designed which is suitable for switching broadband signals.

D. Böttle
Standard Elektrik Lorenz Research Center, Stuttgart, Federal Republic of Germany

Introduction

Digital broadband switches will be among the key electronic components in future broadband communication systems. They will be used for the switched distribution of television and audio signals and for switching video signals for videophone and videoconference services. High quality digitized video signals require bit rates of 70 or 140 Mbit s^{-1}, but it is not easy to realize high speed exchanges that are small, economic to produce, have a low power dissipation, and can serve up to 10000 subscriber loops. In SEL's Research Center, engineers are solving these problems.

ITT's System 12 Digital Exchange is suited to the switching of narrowband and wideband signals, and will be enhanced into a broadband exchange capable of switching 140 Mbit s^{-1} signals by adding a broadband switching network. Central control, supervision, and maintenance functions will be performed by the existing or modified System 12 exchange. This will be an economic solution because hardware and software for the centralized functions need not be duplicated in principle for narrowband and broadband switching. All that is necessary is to add System 12 software modules for the detection and transmission of signaling information relating to the broadband services.

The task of path finding through the broadband switching network will, however, be implemented by control processors within the broadband switching unit if orders to set up or release connections are received from the narrowband exchange. Therefore the structures and capacities of narrowband switching networks are fully independent of those of broadband switching networks and can be optimized separately in each case.

VLSI Circuit for Broadband Switching

The requirement for switching high speed signals in circuits with low power dissipations can only be met by using VLSI (very large scale integration) circuits in a suitable semiconductor technology. A switching circuit for 140 Mbit s^{-1} signals is being designed in state-of-the-art CMOS technology. This technology provides gate delay times and rise and fall times which are sufficient for pulse periods corresponding to 140 Mbit s^{-1}. Advantages of this technology are that it is economic and has a low power dissipation, particularly if the circuits or parts of them operate at low frequencies or if the switching matrix crosspoints are switched off.

In principle, however, MOS is a high impedance technology which makes it difficult to drive high speed signals on long lines with high capacitances. This problem can be partially solved by increasing the channel width of the output transistor on the chip. Another way of minimizing the problem is to reduce the lengths of the connection lines between chips. Thus a compact system design (e.g. multichip equipment practice) is advantageous. In any case the number of connection lines between chips must be minimized to achieve a low power system. This, in turn, means maximizing the number of

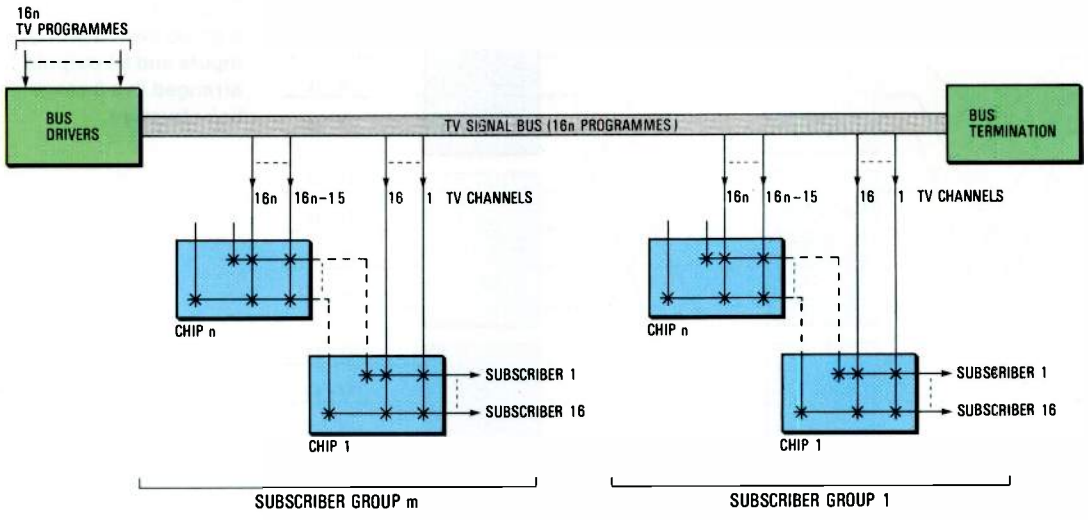


Figure 1
Modular structure of a television network with 16*n* programs and 16*m* subscriber loops.

crosspoints that are integrated on each chip. The complexity of the integration of switching structures is, however, limited by the number of pins and the cost of packaging.

The chip contains a total of some 1400 gates, which is not particularly high for a custom designed circuit. However, a higher complexity would require more than 68 pins, thus increasing packaging costs. It would also greatly complicate testing because of the increased number of possible switching states.

Chip Design

The switching chip being designed by SEL consists of a space matrix with 16 input lines and 16 output lines and 16 matrix extension inputs suitable for 140 Mbit s^{-1} signals. In addition a control part includes decoders for addressing the crosspoints, memory for holding the switch off or switch on information, and interface circuits that allow a microprocessor bus to be connected directly to the switching chip. It is also possible for the microprocessor to check the state of each crosspoint via the signaling interface.

The control part integrated in the chip consists of about 800 gates operating at low frequencies compared with 600 gates in the switching part operating at 140 Mbit s^{-1}. The calculated power dissipation of the chip, which is to be packaged in a 68-pin leaded chip carrier, is less than 1.5 W.

Applications

The chip is a generic component suitable for many high speed switching applications. Switched television distribution networks and videophone switching networks with just a few or many lines can be built up using this chip. The various applications require different connection structures between the 16 × 16 matrix chips. Network blocking is not allowed in television distribution networks because each subscriber wants to receive any selected program at any time. The most obvious nonblocking structure is a single-stage network. Sixteen television programs represent the 16 input signals for the switching circuit, and the 16 output signals are connected via a transmission system to the subscribers' television sets. If more than 16 television programs are required, several switching chips must be cascaded without increasing the fanout of the chip output drivers, as this would reduce the maximum signal speed. Minimum fanout is achieved by using additional extension inputs and additional crosspoints, one for each output. Therefore (16 × 16) + 16 crosspoints are required.

Figure 1 shows the modular structure of a switched television distribution network which can be extended to carry more television programs on a larger number of subscriber lines. The offered television programme signals must be amplified by bus drivers, and the inputs of the switching circuits are connected to the bus. A group of *n* chips in cascade is able to supply 16 subscribers with one program each, individually selected out of 16*n* programs. Thus *m* groups of *n* chips can each supply 16*m* subscribers. To cater for high numbers of subscriber loops (around 10000) about 30 separate program bus systems are required.

In videophone switching networks about 0.1% probability of blocking is allowed,

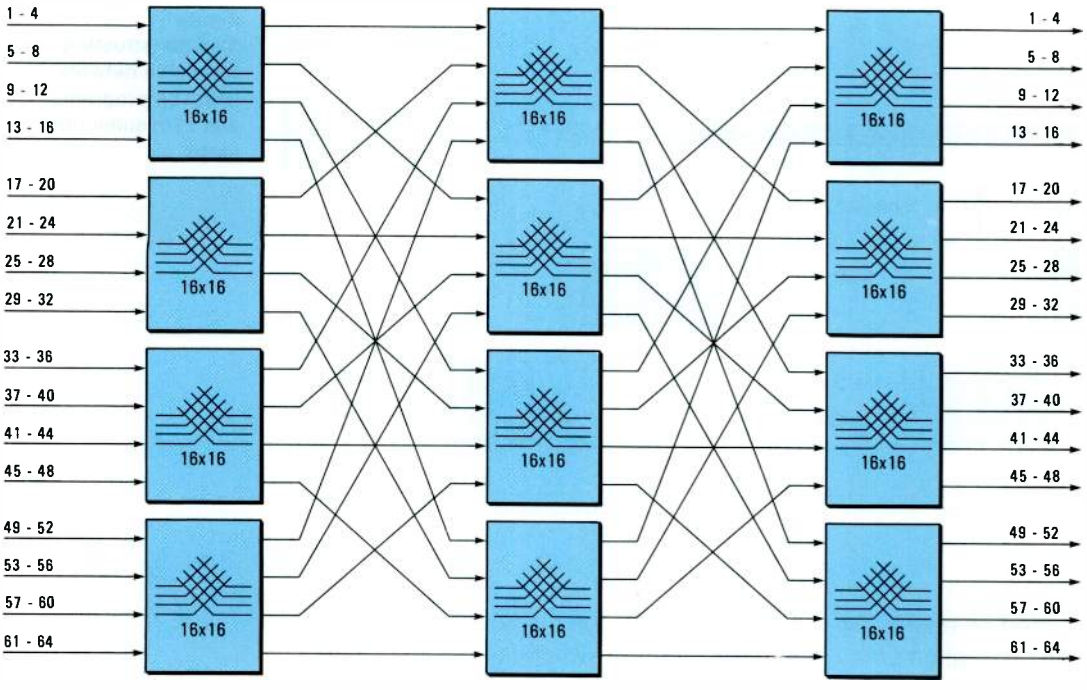


Figure 2
A group switch with 64 inputs and 64 outputs arranged in a 3-stage link structure.

making it different from television distribution systems. Thus multistage network structures can be used. A single-stage structure with 10000 bidirectional lines would require about 390000 16 × 16 switching circuits, making it completely uneconomic.

A network with up to 10000 lines has been designed using a multistage structure with about 2500 16 × 16 switching circuits. It has been assumed that the traffic of one videophone subscriber is about 0.02 erlang, which is lower than telephone traffic today. Under this assumption a fully modular structuré has been designed. The complete network consists of 32 groups of eight access switches and four planes each with 48 group switches. One group switch has 64 input lines and 64 output lines and is built up of 12 switching circuits arranged in a 3-stage link system, as shown in Figure 2.

The 3-stage structure was preferred to a single-stage structure because only 12 circuits (16 × 16) instead of 16 are required. A further advantage of this structure is that it minimizes fanout. Each circuit output has to drive only one circuit input, thereby maximizing the allowed signal speed. The probability of blocking is nearly zero and is therefore low enough for videophone applications.

Although path finding through the 3-stage network is more difficult than through a single-stage network, a one-chip microprocessor is sufficient to control path setup. Path control processors are needed in any case for path finding between the group switches or access switches. In common with System 12, the complete switching network will be controlled by distributed or decentralized processors, which also helps in realizing a modular network. The various control processors are interconnected by signaling lines. Each processor is attached to a network section and has to find a free path and to give further orders via the signaling lines to the successive processors.

Although the switching circuit has been custom designed, it is a universal component for switching networks in digital broadband communication systems.

Conclusions

A broadband switching network will be necessary to switch broadband signals for anticipated new services such as television distribution and videoconferencing. SEL is developing a generic custom design VLSI circuit which can switch various types of broadband information. The structure of the network will depend on the data being switched, but control and maintenance of the broadband switch can be provided by System 12 exchanges.

Dietrich Böttle was born in 1945 near Stuttgart. He studied communication engineering at the University of Stuttgart, graduating as a Dipl-Ing. He joined SEL in 1970 where he was engaged in basic developments for advanced switching and transmission systems. At present Mr Böttle is head of a laboratory in the SEL Research Center responsible for the development of broadband switching exchanges.

This Issue in Brief

Privett, R. F.; Van Iseghem, P.
Impact of Custom VLSI Technology
Electrical Communication (1984), volume 58, no 4, pp 364–371

VLSI technology is affecting many of ITT's product lines in telecommunication, office systems, defense, and industrial products. It makes new system architectures feasible, such as distributed processing and electronic line circuits in System 12, and adds features to existing system designs while reducing size, weight, and power consumption, and increasing performance and reliability. ITT has spent considerable effort and resources in order to exploit VLSI technology effectively, with the result that the corporation has facilities to design and partition systems to make the maximum use of the technology, to design chips in the minimum of design iterations, to keep abreast of the latest semiconductor fabrication processes and packaging techniques, and to test VLSI products both as components and as parts of the system.

Close, A. D.; Fisher, L.; McDermott, R. M.; Nix, T. A.; Perrine, D. M.; Schoen, J. M.
Design System for Semi-Custom VLSI Circuits
Electrical Communication (1984), volume 58, no 4, pp 372–379

As the complexity of integrated circuits increases, the cost and time required to produce full custom design VLSI circuits become prohibitive for all but a few applications where large numbers will be produced. In many cases semi-custom design is more cost-effective and reduces development time. The authors describe a semi-custom design system developed for use by ITT units worldwide. It offers an integrated set of computer-aided design tools for all aspects of VLSI design from schematics capture to mask generation. These tools are backed up by design libraries of proven cell layouts. Anticipated advances in fabrication technology will make it possible to use this system to design semi-custom chips that are as complex as many present full custom design VLSI circuits.

Bennett, K. R.; Lovitt, G. J.
Data Modeling: the Key to Design System Integration
Electrical Communication (1984), volume 58, no 4, pp 380–383

Sequential neutral data formats are being used to interface CAD tools used for VLSI design. To ensure a stable life for the format definitions in a rapidly changing development world, rigorous, precise, and flexible definitions were required. The application of a relational data modeling technique normally associated with database schema design was used to derive these definitions. The practical aspects of applying the technique are described by the authors in the context of system integration of the VLSI CAD tools. The technique also has great potential in the design of most if not all computer systems concerned with data generation and transfer, since the results of an analysis using the technique can be understood and verified by the users of the system.

Lincoln, C. P.
Design of a 3-micron CMOS Cell Library
Electrical Communication (1984), volume 58, no 4, pp 384–388

Over the past three years STL has exploited the benefits of a 5 μm CMOS cell library and autolayout software to produce a large number of semi-custom integrated circuits. In 1983 it was felt that a new cell library could be developed taking advantage of the emerging 3 μm CMOS technologies to maintain a competitive semi-custom design capability. The author discusses the requirements for such a cell library and outlines the design strategies that were evaluated to achieve these objectives. The result is a multisourceable cell library suitable for circuits up to 8.2 MHz and 2500 gates in single layer metal technologies, or more in two-layer metal technologies.

Danneels, J.; Meinck, M.
Methodologies for Full Custom VLSI Design
Electrical Communication (1984), volume 58, no 4, pp 389–397

Over the past 20 years the complexity of integrated circuits has increased dramatically with the introduction of LSI and then VLSI technologies. The design of such circuits is a lengthy and complex process which would have been impossible without computers and computer-aided design tools. Further advances in the scale of integration depend on the development of new design methodologies and tools which will enable designers to produce full custom designed chips with between 50000 and 100000 transistors. The authors look at the strategies and tools being used and developed within ITT to realize the goal of producing such large circuits cost effectively.

Beernaert, D.
Experience in 3-micron Processing: a 10 Volt *n*-well CMOS Process
Electrical Communication (1984), volume 58, no 4, pp 398–404

Custom integrated circuits for the System 12 evolutionary line circuit have been designed using 3 μm CMOS technology with *n*-well construction and 10 V operation. The devices combine high performance and reliability. The author discusses the development of the various device technologies and processing methods used. Optimization of isolation technology, photolithographic methods, etching methods, and switch capacitor technology are considered in detail. Processing methods are then explained, and the article concludes with a summary of the products used in the state-of-the-art System 12 subscriber line interface circuit.

Mohammadi, F.
VLSI 1-micron MOS Processing
Electrical Communication (1984), volume 58, no 4, pp 405–410

The progress of MOS technology from 10 μm to 2.5 μm minimum feature size over the past decade has brought about dramatic improvements in performance and increased circuit complexity; this is typified by advances in memory products. The quest now is to produce reliable, high yield components with a minimum feature size of 1 μm, requiring scaling laws to be taken into account. Device performance at such high densities places stringent requirements on substrate material, isolation techniques, gate module design, and interconnection methods. Each of these areas is discussed in the article, and present trends and future developments are considered.

Dierckx, R.; Guebels, P.; Six, P.
VLSI for the ISDN Line Termination
Electrical Communication (1984), volume 58, no 4, pp 411–417

System 12 is designed to take advantage of ISDN facilities as they become technically feasible. Already many administrations are planning the introduction of ISDNs, and a number of field trials will commence in 1985, with commercial introduction scheduled for 1987 in some countries. A key factor is the development of a suitable ISDN line termination. Initially the U-interface circuit for System 12 will be realized as a set of four chips to meet the introduction time scales. However, as 1.5 μm CMOS technology becomes established, this chip set will be replaced by a single chip, bringing performance benefits.

Fisher, D. G.
Status and Prospects for Gallium Arsenide Technology
Electrical Communication (1984), volume 58, no 4, pp 418–422

Gallium arsenide (GaAs) has several semiconducting properties that are superior to those of the conventional semiconductor, silicon. GaAs technology has progressed to the point where complex microwave integrated circuits and ultra high speed LSI circuits have been demonstrated. The status of GaAs integrated circuit manufacturing, systems applications, and future markets is discussed by the author. The primary motivation for GaAs technology development has been the need for high performance circuits in military applications. Now many commercial applications are emerging. The prospects are excellent for continued performance improvement with sophisticated devices utilizing other GaAs-like materials.

McKnight, A. J.; Mun, J.; Vance, I. A. W.
Wideband Programmable Transversal Filter
Electrical Communication (1984), volume 58, no 4, pp 423–426

Gallium arsenide integrated circuits have advanced to the point where construction of circuits containing hundreds to thousands of components is possible. This article describes an analog transversal filter of the classical type based on an analog delay line tapped at intervals with weighting and summing components to give the desired response. These are all realized monolithically. The advantages of the GaAs substrate are seen in the speed of operation (over 1000 MHz) and the wide dynamic range (over 90 dB in a 100 kHz noise bandwidth). Such a filter enables signals with bandwidths of up to 500 MHz to be processed, and thus represents the fastest flexible filtering technique available in any technology today.

Jacob, G. W.
Designing for Testability
Electrical Communication (1984), volume 58, no 4, pp 427–432

Semiconductor devices and systems containing them have become so complex that it is difficult and costly to test them adequately. The solution is to design them to be testable. In this article the author considers testability cost trade-offs, outlines the interrelationship of test programming and designing for testability, and presents several methods of designing for testability.

McDermott, R. M.
ITT's Testability Analysis Program
Electrical Communication (1984), volume 58, no 4, pp 433–439

Increasing device complexity requires improved techniques to ensure testable designs. Testability is related to access to internal nodes of the device for both observation and control, in addition to its operational input and output connections. The article describes the use of ITTAP, ITT's testability analysis program developed for evaluating and enhancing design testability. Unlike other methods, this program automatically identifies nodes for improving testability. Measurement and improvement of testability are discussed, and the effectiveness of ITTAP is demonstrated by comparing results with independent assessments carried out manually by senior test engineers.

Reiner, H.
VLSI Packaging
Electrical Communication (1984), volume 58, no 4, pp 440–446

The ever greater complexity of VLSI devices is resulting in increases in pin count, power dissipation, and chip area. Furthermore, the increase in speed because of the smaller feature sizes leads to more stringent electrical requirements on the packaging. For high reliability under adverse ambient conditions, hermetic sealing is mandatory. However, for less severe requirements, plastic encapsulation is proving a cost-effective alternative. It is expected that improvements in plastic materials and in chip surface passivation will further enhance the reliability of plastic-packaged VLSI devices. Packaging materials and processes, as well as package shapes, will have to be modified to cope with the demands of future VLSI devices.

Pirsch, P.
Video Codec for Broadband Communication
Electrical Communication (1984), volume 58, no 4, pp 447–449

Current perspectives on broadband communication services make the realization of highly integrated video systems particularly important. This article describes the design of a video codec to be implemented in CMOS technology. The system enables transmission of one video signal at approximately 70 Mbit s^{-1}, using differential pulse code modulation.

Böttle, D.
Switching of 140 Mbit s^{-1} Signals in Broadband Communication Systems
Electrical Communication (1984), volume 58, no 4, pp 450–452

Existing digital exchanges have been designed to carry narrowband and, in some cases, wideband signals in an ISDN. However, a number of new services will require the switching of broadband signals at up to 140 Mbit s^{-1}. Examples are television broadcasting and videophone service. The author describes an architecture for a generic custom MOS chip in state-of-the-art technology which will be used to switch broadband signals. This broadband switch will be suitable for building up modular switching networks with varying numbers of stages, depending on the application.

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