VOLUME 11 □ NUMBER 10 IEEE spectrum OCTOBER 1974

IEEE spectrum

articles

departments

the cover

Artist Charles O. Bennett depicts how NASA's Viking Lander will look after touchdown on Mars. Scheduled for launch late in 1975, Viking will take approximately ten months to rendezvous with the "red" planet—the success of the mission, however, will be largely dependent on the systems described in the article beginning on page 42.

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spectral lines

A sensitive topic

When we decided to tackle the article about the three Bay Area Rapid Transit (BART) engineers (p. 69), our colleagues told us it would be a "no-win" situation for *Spectrum*. The case, now under litigation, presumably could be "won" by one side or the other, they noted, but *Spectrum*, if it published the article, would make friends on neither side. However, our objective wasn't to make friends or to curry favor, so we forged ahead, hoping to illuminate issues of some consequence to members of IEEE.

The BART story has two parts, one technical and the other nontechnical. It would be convenient if the two could be treated separately, but such is neither practical nor desirable, in view of their mutually inextricable nature. Furthermore, the nontechnical side involves not only professional ethics and employment practices, but factors such as procurement practices and regulations.

The article in this issue, while it is intended to focus on ethics and employment practices, of necessity reflects a good part of BART's technical history, insofar as it is perceived by the three engineers and certain other interested parties. But this article is *not* intended to provide an analysis of BART's past operational modes, nor to reflect its current operational status or to speculate about its future. We leave that for a subsequent article (or articles) now under research by staff writer Gordon Friedlander and others.

Notwithstanding, it would be surprising if the case, scheduled to come to trial on the 25th of this month, were conducted without considerable attention to the technical aspects. In this regard, interested observers have wondered how the court will weigh the degree to which the three engineers were correct in their original concerns. Have subsequent events borne out these concerns? Have their actions and the publicity afforded these actions had an effect on the BART system itself? Specifically, would the independent investigations of BART's design and operational history have been commissioned if the engineers had not, inadvertently or otherwise, brought the issues to the public?

Completely aside from the outcome of the court case are ramifications such as these:

- How does the practicing engineer—or engineering manager for that matter—establish his loyalties? Unquestionably there is a hierarchy ranging from self and family to company, the profession, community, country, and humanity itself. How does the engineer rank order these? Is his evaluation a matter of personal ethics, professional ethics, or both?
- Can the practicing EE, who is usually employed by an institution or corporation, hew to his loyalties when they conflict with the objectives of his employer without jeopardizing his job?
- Is it possible for an engineer to disagree with his employer, take his case before the public (or to some other "higher authority"), and still expect to be retained by that employer?
- Assuming that the foregoing is possible, is it practical, or would not the probable outcome of such a situation be ostracism of the "offender" or, at best, his involuntary "lateral arabesque" to an inconsequential position?

These basic questions will probably be scrutinized, implicitly if not explicitly, during the ensuing litigation. Yet it is highly unlikely that the outcome will provide a range of definitive legal precedents or even a clear cut set of guidelines in the very complex arena of professional employment practices.

A project the size and scope of BART was bound to encounter serious technical "bugs" (in addition to political and financial problems). Such technical trials and tribulations have been well publicized, in scope if not in depth, by newspapers and also the broadcast media.

During BART's recent past, several independent consultants have been engaged to provide the following analyses of the system's design and/or operations:

- The Battelle Memorial Institute, in 1971, submitted a two-volume study to BART (*Spectrum*, March 1973, p. 34).
- Beckers, Burfine and Associates sent a copy of a study it conducted to the BARTD Board of Directors on January 12, 1972.
- A. Alan Post, legislative analyst for the California State Senate, commissioned a study that culminated in a report issued November 9, 1971 (*Spectrum*, March 1973, p. 32). A second report was issued in October 1973, and still another in March of this year.
- The Brobeck-Oliver-Lovell "Blue Ribbon Panel" was commissioned by the California State Senate Public Utilities and Corporations Committee in December 1972, and submitted its report on January 3, 1973 (*Spectrum*, April 1973, p. 40).

In the meantime, the reliability of BART is evidently improving during revenue service in at least one respect—the burnishing of the wheels and rails is decreasing the associated contact resistance and thus, perhaps, obviating the need for the auxiliary "scrubbing" operation once suggested and tried (*Spectrum*, March 1973, p. 37). At the same time, several of the modifications of the system recommended in one or more of the above-mentioned reports have been undertaken. *Spectrum* will report on the status of these in a near-future issue.

Donald Christiansen, Editor

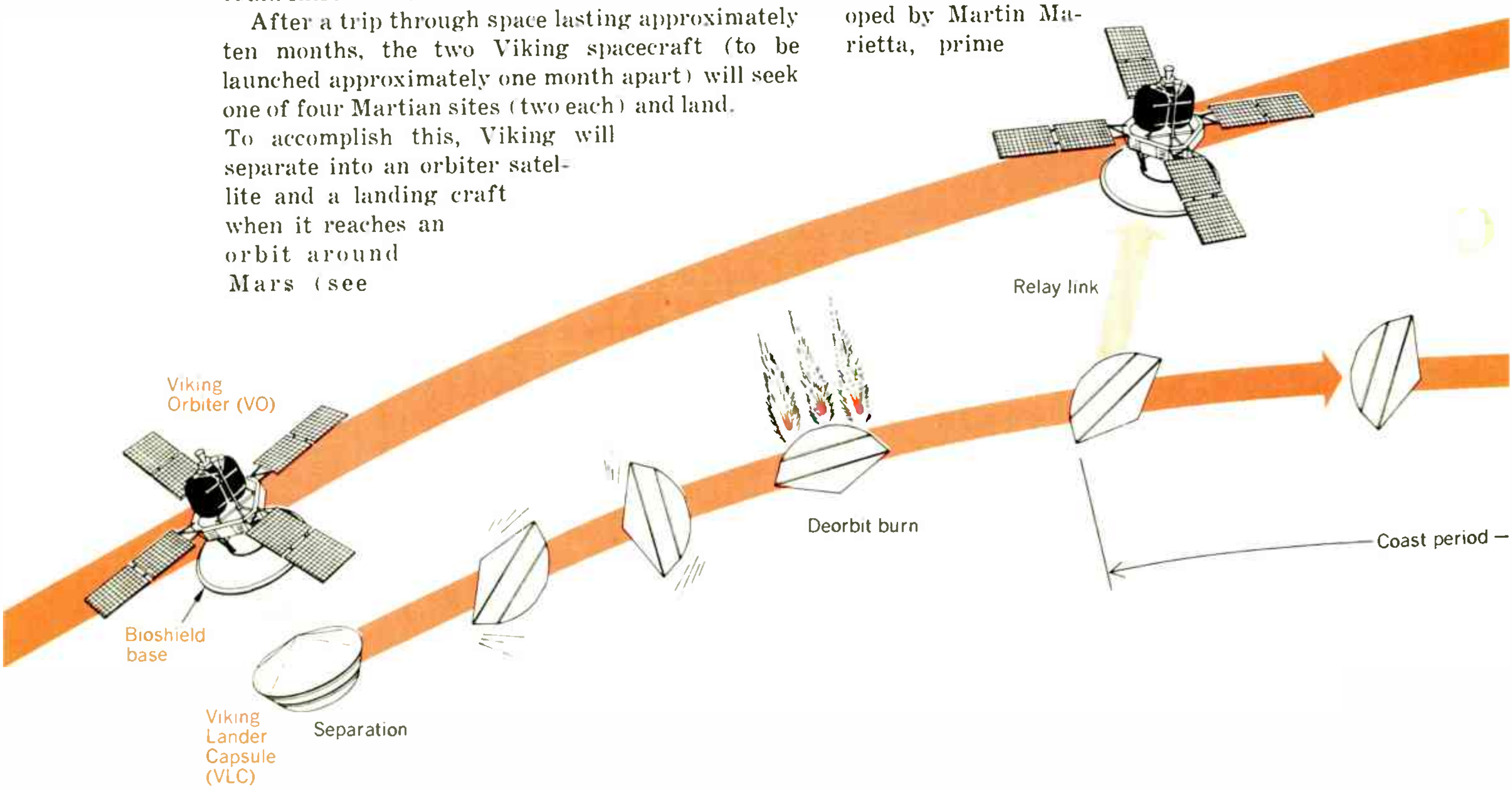
Automatic checkout for missions to Mars

Unmanned extraterrestrial landings call for reliable premission testing of complex guidance and communications systems

P. M. Norris and C. W. Rea
Martin Marietta Corporation

On the heels of some of the most dramatic results obtained to date from unmanned spacecraft (see Box, page 45), the U.S. National Aeronautics and Space Administration (NASA) is scheduled to launch two Viking spacecraft from Cape Kennedy, Fla., in the fall of 1975 to answer the centuries-old question of whether life once existed, now exists, or could exist on Mars.

After a trip through space lasting approximately ten months, the two Viking spacecraft (to be launched approximately one month apart) will seek one of four Martian sites (two each) and land. To accomplish this, Viking will separate into an orbiter satellite and a landing craft when it reaches an orbit around Mars (see illustration). In carrying out this extraterrestrial unmanned landing—a more difficult feat than close-orbit or flyby missions—Viking will employ two radar systems (one for determining altitude, the other for such parameters as velocity, drift, and attitude), and two communications systems (one as a direct link from both orbiter and lander to Earth, the other a one-way relay link from lander to orbiter). To obtain maximum reliability from these critical systems, sophisticated automatic checkout equipment has been developed by Martin Marietta, prime



In the fall months of 1975 NASA will launch two Viking spacecraft, one month apart, toward Mars. To help in this exploration, the Viking Orbiter (VO) will collect data both during approach and while orbiting Mars, and maintain communications with the earth and the Viking Lander Capsule (VLC). After separation from Orbiter, the Lander will enter the Martian atmosphere protected against aerodynamic heating by an aeroshell, which also causes deceleration. Further deceleration occurs by parachute after the aeroshell has been ejected. The Lander then separates from the parachute and protective cover at about 1500 meters above the Martian surface, and completes the soft landing using its own terminal-descent engines. During descent, aeroshell instruments will analyze the structure and composition of the Martian atmosphere. On the surface, the Lander will collect and transmit to the earth data on biological, organic, meteorological, and seismic properties of Mars, and cameras will be used to transmit panoramic, three-dimensional, high-resolution color images of the planet to earth.

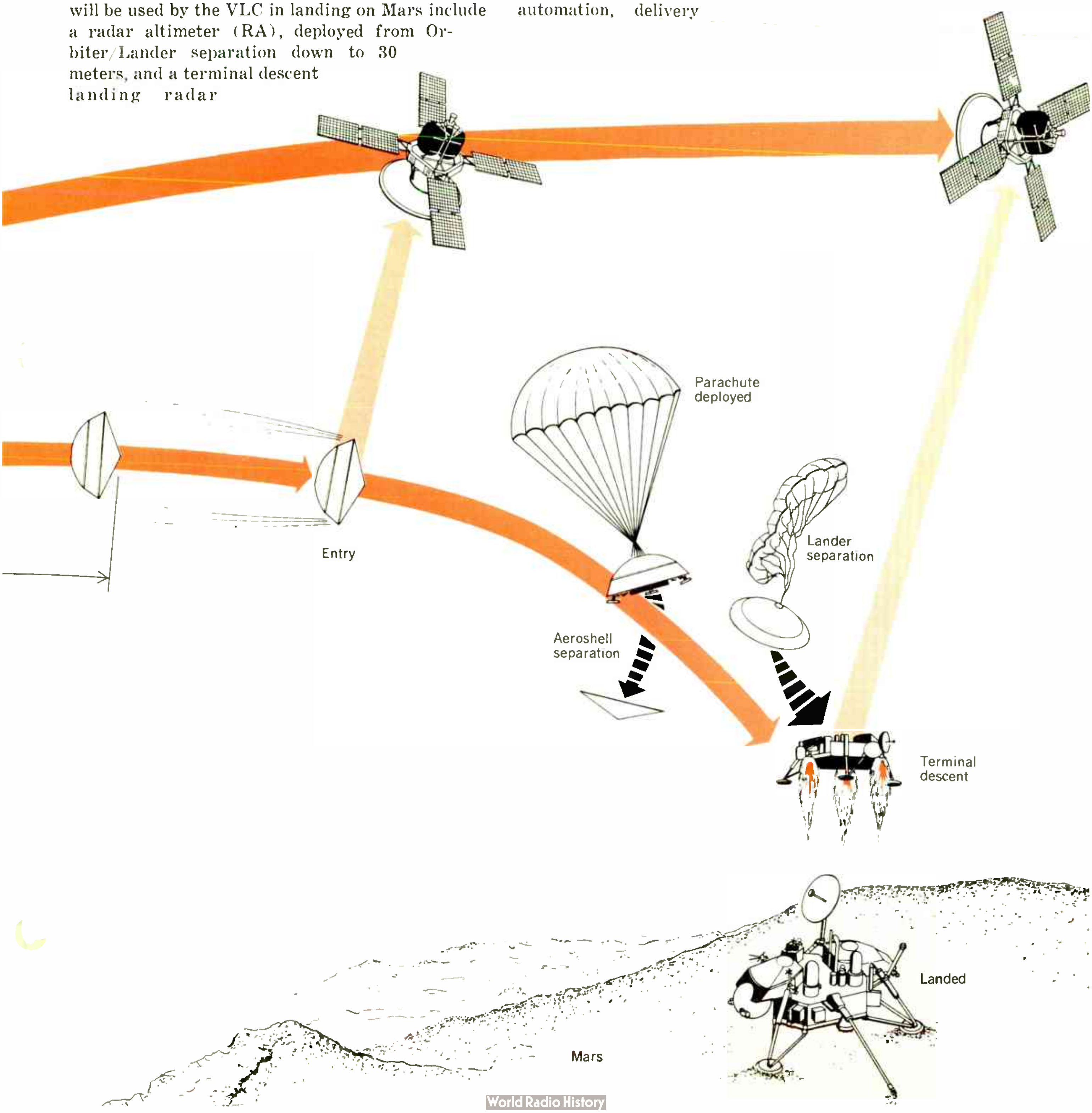
contractor for the Viking program. Consisting of a computerized mobile test system to check out the Viking Lander Capsule (VLC), the Viking system test equipment (STE) is being used to support acceptance and environmental testing in Denver, Colo., compatibility tests with the Viking Orbiter (VO) at Jet Propulsion Laboratories in Pasadena, Calif., and for assembly and prelaunch checkout at Cape Kennedy, Fla.

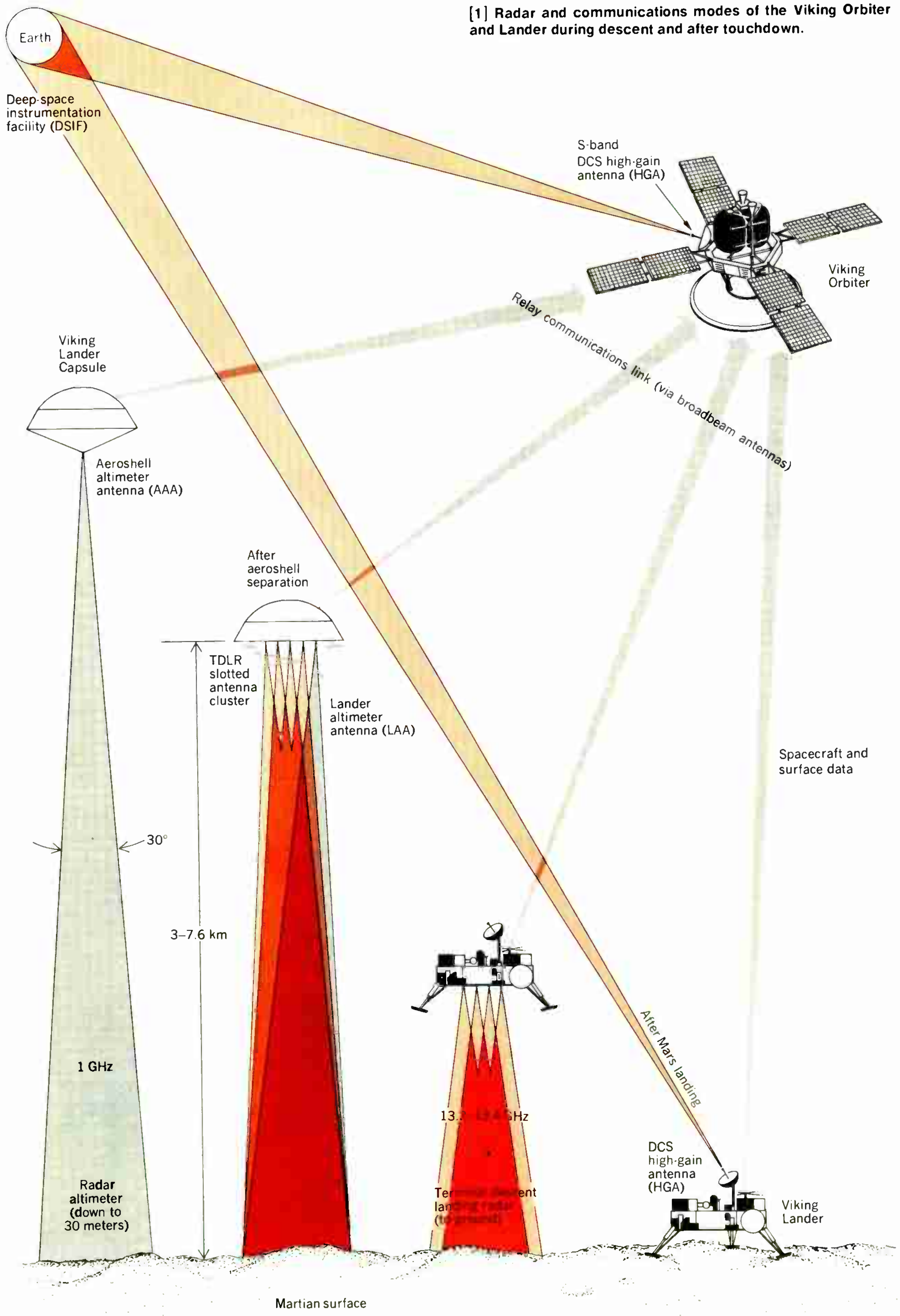
Critical systems . . .

When the Viking spacecraft finally rendezvous with Mars, the 200 million mile distance to Earth will require nearly 45 minutes to complete a two-way communications link. Hence, the deorbit and touchdown of the Viking Lander Capsule will have to be fully automated. The two radar systems that will be used by the VLC in landing on Mars include a radar altimeter (RA), deployed from Orbiter/Lander separation down to 30 meters, and a terminal descent landing radar (TDLR) from aeroshell separation down to the Martian surface (see Fig. 1). In addition, a direct communications subsystem (DCS) will link Earth with both Orbiter and Lander (after touchdown), and a relay communications link (RCL) will join Lander and Orbiter both during descent and after landing.

. . . need critical testing

The Viking system test equipment represents some of the latest advancements in computer-controlled RF simulation and testing. During inception of the STE, Martin Marietta gave serious consideration to the cost-effectiveness of new development versus modification of off-the-shelf components and equipment. Each system was considered in relation to system requirements, degree of automation, delivery





[1] **Radar and communications modes of the Viking Orbiter and Lander during descent and after touchdown.**

lead time, cost, operator skill level, etc. Based on over two years of operating experience, the present system configuration is considered to be versatile, accurate, and capable of meeting the original system goals (see Fig. 2, left-hand side).

At the heart of the Viking STE is a Honeywell H-632 computer, which is housed in an equipment van, with the balance of the test equipment located close to the Lander during system testing (see Fig. 3). In its function of acquiring, processing, decoding, and recording large volumes of Lander engineering and science telemetry data, the STE

- Performs aperture and go/no-go limit checks
- Monitors (with error change detection) and provides discrete stimuli via hardlines
- Acquires analog data via hardlines into a 255-channel multiplexer and A/D converter
- Inputs and outputs digital data via 35 channels
- Uses a compiler processing unit to test Viking radars and communications subsystems automatically
- Controls and communicates with the Lander computer via a 16-kbit/s uplink/downlink system

The STE software consists of both on-line and off-line systems. The on-line system is made up of an executive, schedulers, data monitor systems, and an interpreter; the off-line system features a Viking test language that uses near-English verbs, a translator, a data file configuration control, off-line processing of science data, and file-management programs.

In operation, for example, the STE responds to the stimulus of the radar altimeter with the aid of the computer; in turn, the RA receiver detects the response and updates the Lander guidance, control, and sequence computer (GCSC), which then is monitored by the STE computer, thus closing the loop. This sequence of events is characteristic of most Lander STE subsystems, and may be used to simulate all manner of entry, descent, and landing problems.

How the Viking will land

A major component of the Viking Lander is its guidance and control subsystem, which serves to coordinate all on-board equipment with the VLC guidance, control, and sequencing computer (GCSC). As can be seen in Fig. 2 (right-hand side), the RA and TDLR radars continually update the guidance and control subsystem during descent, and play a critical role in obtaining a successful landing.

Unmanned spacecraft 1974—an instrumentation success!

This year, scientists are not only getting glimpses of other planets up close for the first time, but also demonstrating the huge success of the instrumentation packages being deployed by recent unmanned space shots. By way of comparison, an oceanographic instrumentation expert recently admitted that only one of 13 sensors designed for a large deep-sea experiment worked, a dismal performance that speaks more about the funding differential between space and ocean exploration than about degrees of difficulty.

Launched on March 2, 1972, and April 5, 1973, respectively, spin-stabilized *Pioneers 10 and 11* each carry 30 kg of instruments on their "grand tour" of Jupiter and planets beyond. Included in this instrumentation package are radioisotopic thermoelectric generators (the first time ever used), 13 panels to detect interplanetary particles, a helium-vector magnetometer, optical asteroid–meteroid detectors, a plasma analyzer, a cosmic-ray telescope, a trapped-radiation detector, a charged-particle instrument, a Geiger-tube telescope, an infrared radiometer, an ultraviolet photometer, and an imaging photometer. Despite unexpectedly strong radiation encountered during Pioneer 10's flyby of Jupiter on December 3, 1973, all instruments continued to function, and some of the most dramatic shots ever seen of any planet were returned to Earth. Pioneer 11 is expected to pass Jupiter on December 5 of this year, and then go on to Saturn in 1979.

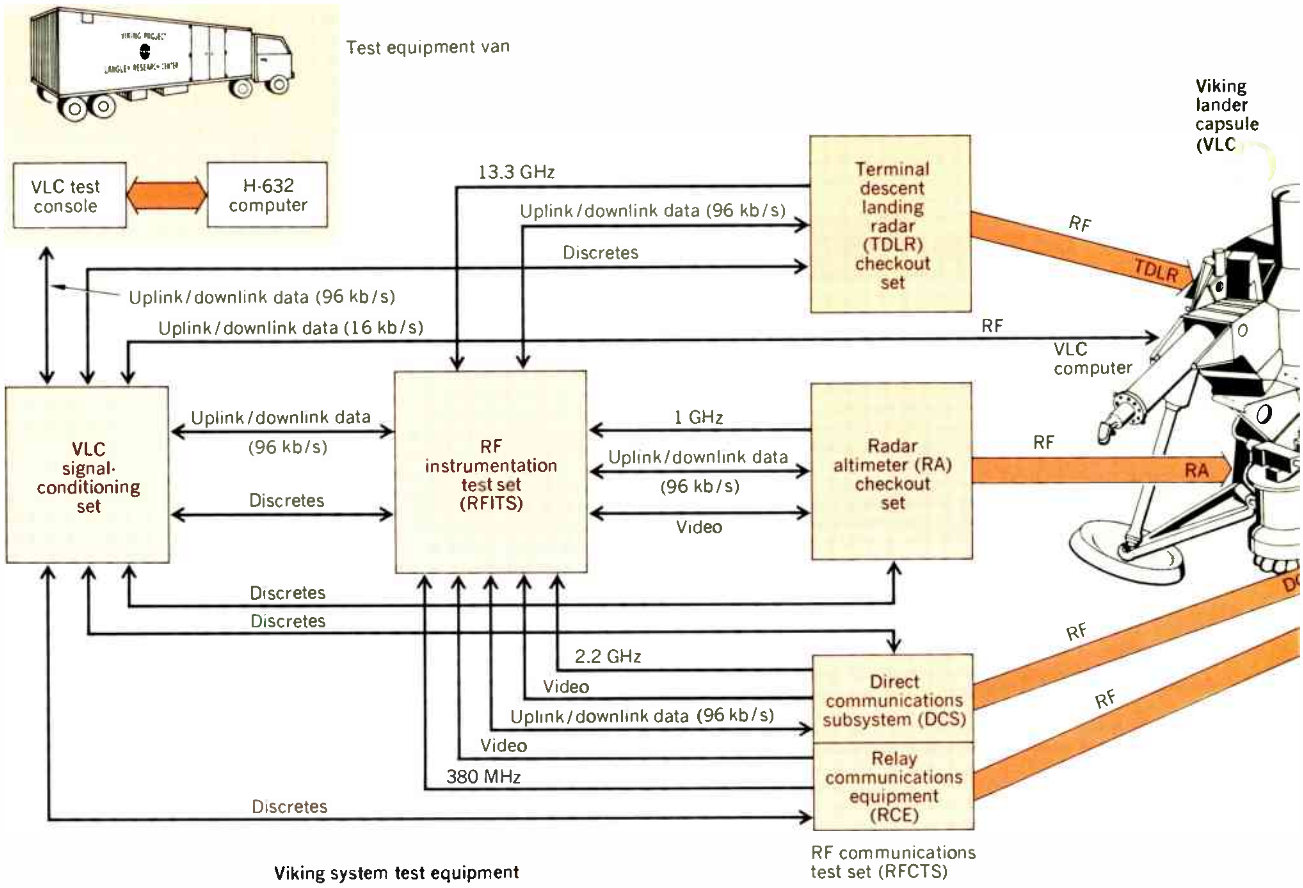
Mariner 10, which was launched into space from Cape Kennedy on November 3 of last year, has thus far been the only space vehicle to return data from two planets. Passing Venus on February 5, Mariner then used a "slingshot" effect produced by that planet to propel its way toward Mercury, which it passed on March 29, the first such visit by any spacecraft. Several Earth-controlled adjustments have since created an orbit that will cause Mariner to re-rendezvous with Mercury on September 21. So far, voluminous data have been received from Mariner 10, resulting from studies of solar-wind interaction via magnetic-field, plasma, and charged-particle experiments, as well as far-UV spectroscopy to detect atmosphere, IR sensing of thermal radiation, *S*- and *X*-band occultation/Doppler-shift science experiments, and video coverage via television cameras.

Other spacecraft launched this year include a geosynchronous weather satellite *(SMS-1)* over the Atlantic Ocean—with two more scheduled for later this year—and a new communications satellite (the *ATS-6*), which can cover the entire continental U.S. and will serve as a relay station for the upcoming Apollo/Soyuz flight.

Scientifically, the Viking spacecraft described in this article is the most complex ever built, with 65 kg (144 lbs) of instruments on the Orbiter and 67 kg on the Lander. While the Orbiter carries two high-resolution TV cameras, an IR spectrometer, and an IR radiometer, the Lander will deploy two facsimile "stereo" cameras, a one-cubic-foot biology lab capable of automatically performing three different life-detection experiments on soil samples obtained from a boom-mounted collector head, a gas chromatograph/mass spectrometer for identifying gases and organic compounds, three meteorology sensors, a seismometer, an X-ray fluorescence spectrometer for inorganic chemical analysis, magnets, and a retarding potential analyzer to measure ionospheric ions and electrons. In addition, there is a separate *X*-band Orbiter/Earth link solely for science data transfer, an upper-atmosphere mass spectrometer on the aeroshell, solar-energy panels on Orbiter, and two 35-watt nuclear-fueled generators to recharge Lander batteries for at least 90 days.

The success of Viking's instrumentation package cannot fail to have a profound effect on the planning of future unmanned—and perhaps manned—spacecraft missions. In view of NASA's philosophy of automating as many functions as possible on even manned space flights, it remains to be seen how man the observer/decision-maker will be deployed on future treks into space!

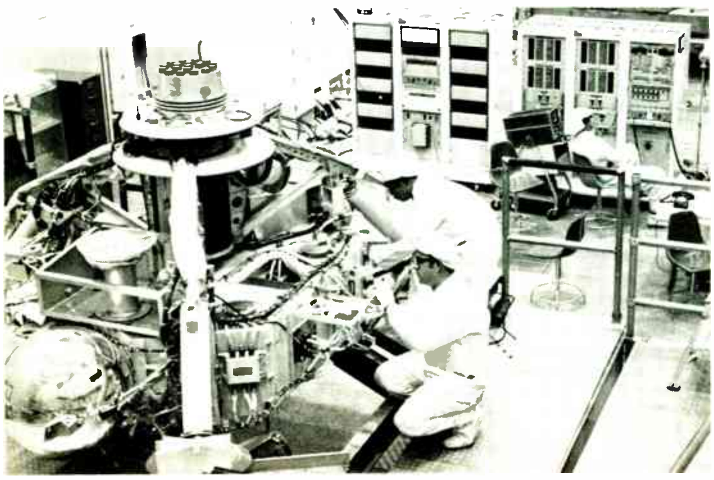
Marce Eleccion



[2] Viking RF system test equipment and its relation to the Lander guidance and control subsystem.

The *radar altimeter* is a 1-GHz pulse radar, and operates in four modes during the Lander descent (see Table I). Since the aeroshell is needed to protect the VLC in the initial phase of entry, two antennas are used in the RA: the aeroshell altimeter antenna (AAA), which resides in the aeroshell and is ejected as part of this structure, and the Lander altimeter antenna (LAA), which is used for the remainder of the descent until about 30 meters altitude.

[3] Viking STE as deployed in an actual checkout of the Viking Lander Capsule.



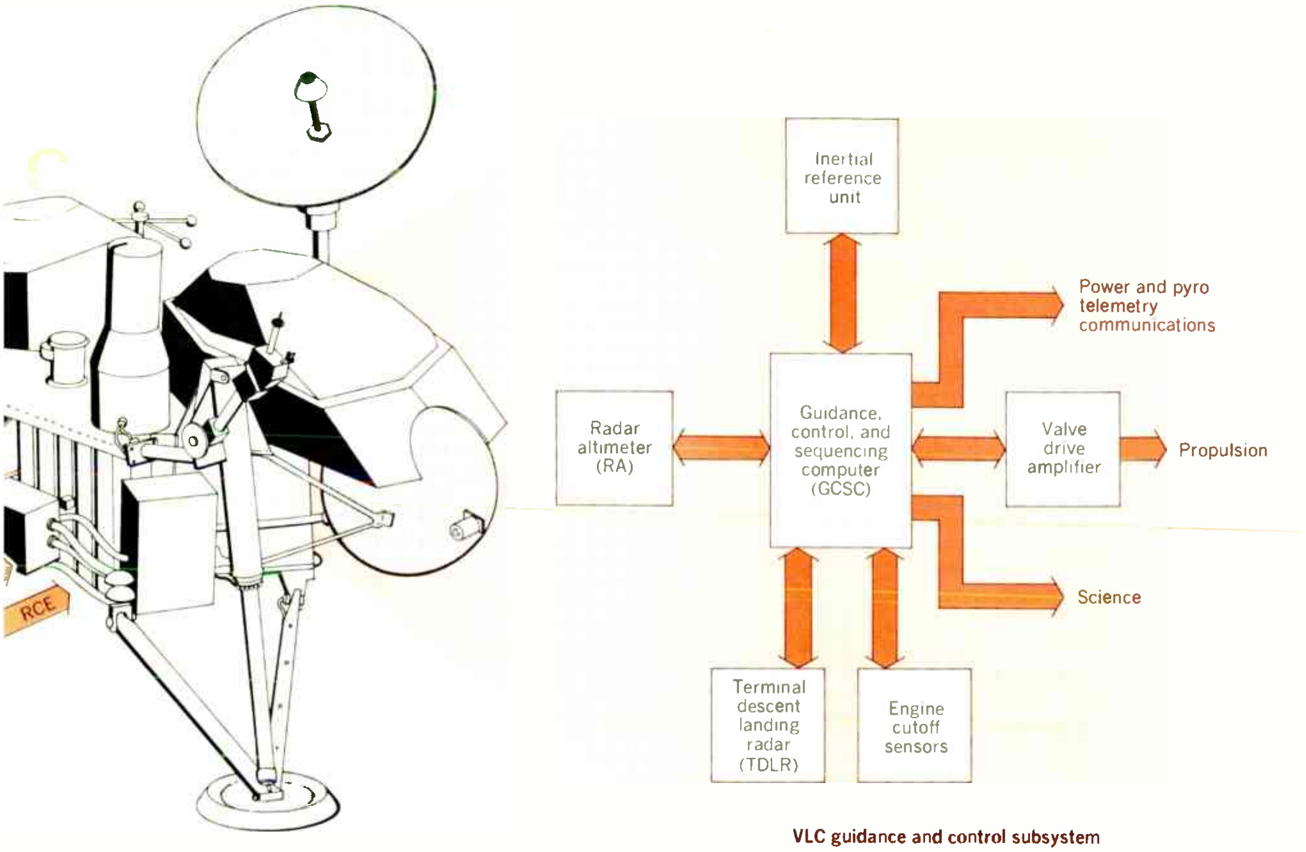
Since the LAA becomes operational immediately after aeroshell ejection, the aeroshell itself will be detected as a false target. The radar altimeter therefore must be able to discriminate between the falling aeroshell and the Martian surface.

Whereas the radar altimeter measures altitude, the *terminal descent landing radar*—which also becomes operational upon aeroshell ejection—determines such parameters as velocity, drift, and attitude. Derived from the Surveyor and Lunar Excursion Module radar systems, the TDLR consists of four independent Doppler radars and has an antenna cluster of four individual two-beam arrays, one of which is used for transmitting and one for receiving. The individual radars are solid state and operate at 13.2–13.4 GHz, employing mechanical and frequency diversity between the four beams. The symmetrical cluster of phased arrays radiates the four beams at an angle of 21 degrees from a perpendicular to the plane of the array.

The four independent TDLR radars—which operate until the Lander touches down—consist of 150-mW

I. Radar altimeter characteristics

Mode 1	Pulse Width	PRF	Antenna	Approximate Altitude
1	6 μs	700 pulses/s	AAA	3000–140 000 meters
2–3	700 ns	5600 pulses/s	LAA	450–7600 meters
4	50 ns	5600 pulses/s	LAA	30–750 meters



VLC guidance and control subsystem

Implementing TDLR checkout

The checkout set path-loss simulation capability, P_1, of the TDLR radar is defined as follows:

$$P_1 = \frac{(4\pi)^2 H^2}{\delta_0 \cos \theta}$$

where H equals altitude; δ_0, the reflectivity coefficient; and θ, the angle of incidence. The TDLR checkout set varies parameters of the equation to simulate the distance, velocity, and surface conditions of a Mars landing.

The STE test computer generates discretes (see Fig. 2), which are used to set the TDLR checkout set test configuration. The discretes select the pairs of beams to be tested (1 and 3 or 2 and 4), digital data, RF power data, frequency, and rate of acceleration. These parameters simulate the variations of H, δ_0, and θ in the path-loss equation. In addition, the tracking filter is tested through variations in center frequency and signal bandwidth simulating the VLC approach to the Martian surface.

A Doppler spectrum simulator (DSS) is used to generate a simulated spectral return for use in static and dynamic testing of the TDLR. The Doppler parameters are programmable by external digital words from the STE test computer or from digital words generated by the front panel manual switches. These controls provide Doppler frequencies from 0 to ±25 kHz, bandwidths of 3 to 999 Hz, and RF level attenuation from 0 to 60 dB programmable, and to 85 dB with a variable attenuator.

The TDLR checkout set provides maximum test flexibility. Although the checkout set is capable of full remote operation by the STE test computer, manual operation is provided for all functions. Full manual operation allows static problems to be generated but not dynamic problems.

The TDLR checkout set has self-test capability so proper operation can be assured prior to TDLR testing. The DSS contains a 13.3-GHz oscillator with an adjusting level that may be used for complete testing of the RF functions with the aid of a spectrum analyzer. A self-test feature tests all logic modes.

The complete operation of the TDLR checkout set may be monitored from the front panels. All discrete commands, whether remote or manual, are displayed. All uplink digital words from the STE test computer (including TDLR digital response) and all downlink words are displayed on the control display panel. This display includes TDLR tracking data and the Doppler frequency error between the stimulus and TDLR response.

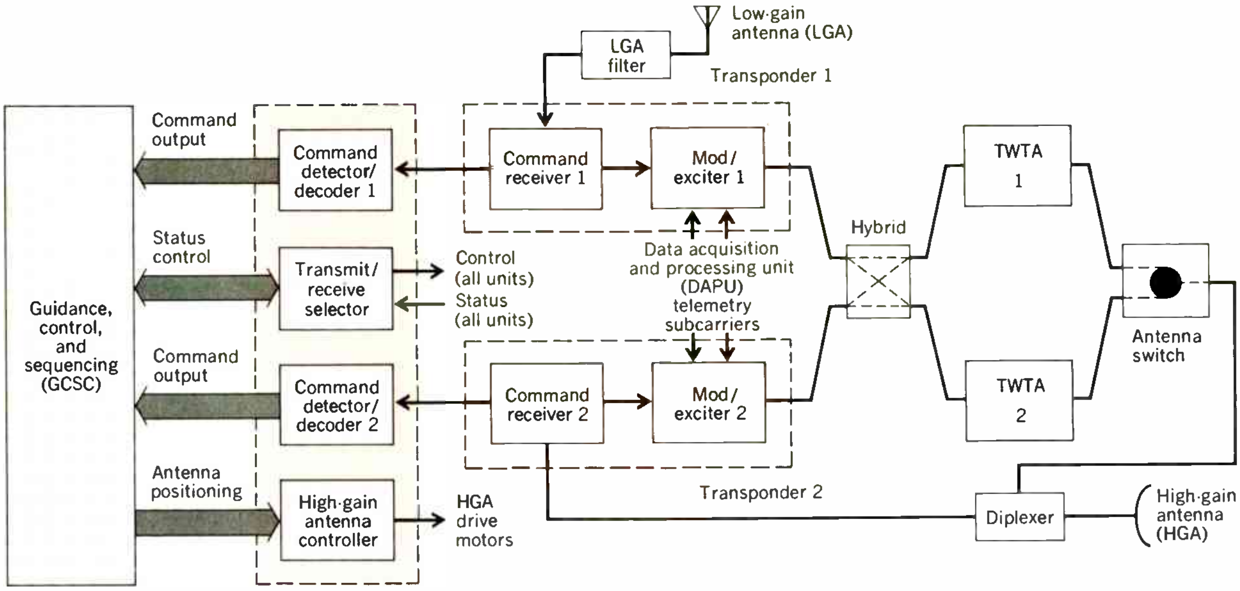
Typical TDLR dynamic accuracy tests*

Center frequency	Bandwidth	Path Loss
20 kHz–60 Hz	850 Hz	134–103 dB
2.5 kHz–100 Hz	75 Hz	130–99 dB

*All ramps performed at both 1.25 kHz/s and 1.65 kHz/s.

Typical TDLR acquisition sensitivity tests

Center Frequency	Bandwidth	Path Loss
20 kHz	850 Hz	140 dB–160 dB
2.5 kHz	65 Hz	140 dB–160 dB



[4] The Lander direct communications subsystem.

CW (continuous-wave) oscillators, zero-IF receivers, and solid-state Doppler trackers. The frequency and mechanical arrangement produce cross-coupling isolation of better than 56 dB, and the variable-bandwidth characteristic of the trackers allows radar operation over a wide Doppler range. Receiver characteristics permit operation from a minimum path loss of 47 dB to a maximum of over 130 dB.

Although the TDLR will track Lander descent down to ground level, the terminal descent rockets quit firing at about five meters from the surface so as not to disturb the landing site. In operation, the TDLR tracker will cover a nominal velocity range of 2 ft/s to 710 ft/s (or approximately 60–20 000 Hz) and accelerations to 1.65 kHz/s.

Viking communications

The two RF communications systems to be used on the Viking spacecraft are essential in closing the link between both Earth and Mars and Orbiter and Lander.

The VLC *direct communications subsystem*—to be used only after touchdown—is described in Fig. 4. This system contains two command receivers, one coupled to a high-gain antenna (HGA) and the other to a low-gain antenna (LGA). Transmission is accomplished through either of two modulator exciters stimulated from the data acquisition and processing unit (DAPU), with outputs amplified by either of two

II. Direct communications subsystem test requirements

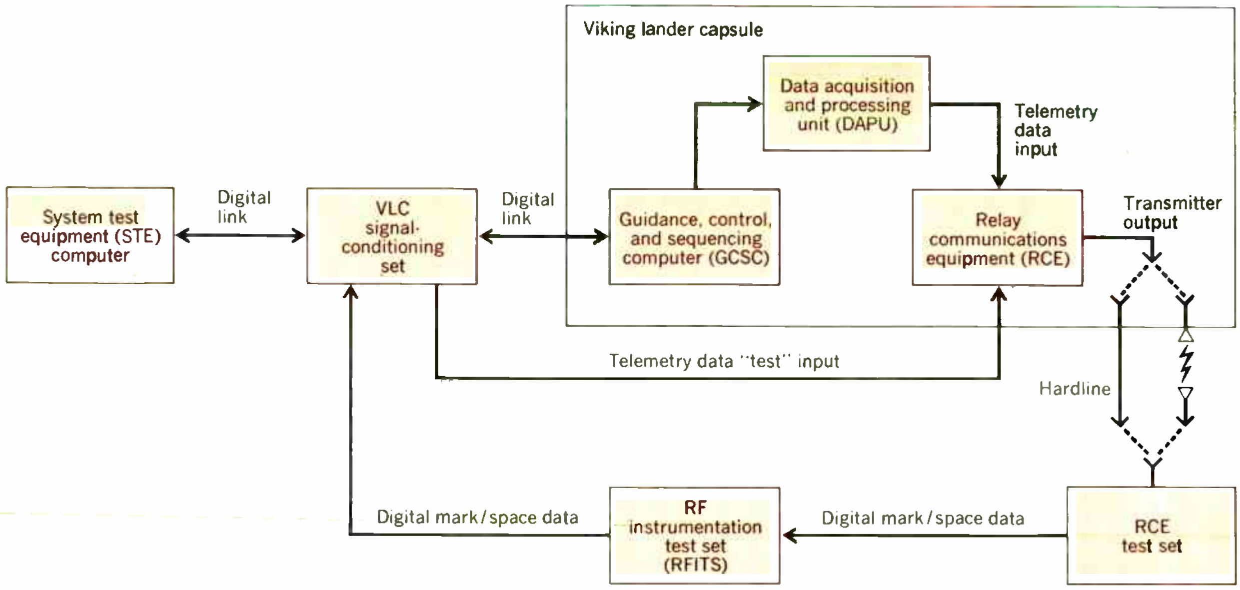
Requirement	Typical Value
Measure DCS transmitter output	+43 dBm
Measure DCS transmitter frequency	2294.629630 MHz
Measure DCS frequency stability	±0.2 ppm
Measure DCS threshold	−147 dBm to −154 dBm
Measure bit error rate	1×10^{-5}
Measure dynamic range	Threshold to −80 dBm
Measure tracking range	±120 kHz
Measure tracking response	18 Hz/s–400 Hz/s
Receive and demodulate downlink transmission	72-kHz science subcarrier 12-kHz engineering subcarrier
Measure DCS modulation indices	Ranging: 0.45 rad Science: 0.8 rad Engineering: 0.45–0.8 rad
Measure DCS transmitter phase noise	3.4 degrees rms

Details on DCS checkout

In the Viking DCS RF communications checkout mode, transmitter power is measured in the RFCTS by a resident power meter similar to the serial digital downlink signal produced by the RA checkout set to the STE computer. Frequency measurement is accomplished in the RFITS, and DCS best-lock frequency, tracking, and response are measured by programming the test transmitter voltage-controlled crystal oscillator. This is accomplished under computer control in two ways: a linear ramp may be selected to smoothly change the test transmitter frequency, or a digital command may be used to establish a specific frequency.

DCS receiver sensitivity is established as with the RA: a programmable attenuator varies the test transmitter output level to either the HGA or LGA and the STE computer monitors an "in-lock" discrete from the DCS electronics.

Bit error rate may be established for the test set in a self-test mode under precisely controlled conditions or under simulated operating conditions with equal precision. The modulation indices and residual phase errors are determined by calibrating the RFCTS with its test transmitter and receiver, then measuring the VLC DCS signal. These measurements are made with a true rms voltmeter in the RFCTS and the data serially downlinked from that STE. DCS static phase error and AGC voltages are displayed on RFCTS displays and also downlinked to the STE computer through the conditioning test set.



[5] Detail of the RCE RF communications checkout scheme of the Viking Lander.

traveling-wave-tube amplifiers (TWTAs).

The signal itself is transmitted to Earth through the HGA controlled by the Lander's GCSC. This downlink signal to the deep-space instrumentation facility (DSIF) on Earth—made up of a worldwide large-antenna network—is either phase coherent with the uplink DSIF signal or may be generated by an internal frequency source, and consists of a composite telemetry source. In the case of phase-coherent operation, the DCS translates the DSIF signal by a fixed ratio of 221/240. The composite command DSIF signal received by the Lander DCS is then demodulated and detected, with the DCS command decoders supplying the GCSC command data, bit sync, and in-lock signals.

During its cruise, the Orbiter RF subsystem receives the same DSIF signal the VLC does after it lands.

The *relay communications link* includes both the Lander and Orbiter RF subsystems, and uses broadbeam antennas on both the VLC and VO to transmit Lander engineering data from separation to entry by intermittent data transmission, as well as engineering and entry science data from entry to parachute deployment by continuous transmission (intermediate power level and low bit rate), and from parachute deployment to landing by continuous transmission (high power level and low bit rate). Immediately after landing and until the Orbiter sets over the Mars horizon, Lander engineering and surface science data, including video imagery, will be transmitted to Orbiter at the high power level.

Details on RCE checkout

In the Viking RCE RF communications checkout mode, power levels and frequency are measured by a power meter residing in the RCE test set and by a counter in the RFITS. On request of the STE computer, the test set also demodulates frequency-shift keying (FSK) science data and sends the data to the telemetry data conditioner for further processing.

Specifically, the RCE transmitter RF power is +30.5 dBm, +39.5 dBm, or +44.3 dBm, depending upon the mode of operation. The test set measures these levels within ±0.5 dB by appropriately configuring a switching chassis consisting of various attenuators, amplifiers, etc. FSK modulation with mark and space frequencies of 381.063303 MHz and 380.863303 MHz, respectively, is transmitted at a rate of 10^7 bits per day from the RCE to the Orbiter relay subsystem.

In addition to the other parameters mentioned, the RCE portion of the RFCTS can determine incidental AM and FM. As a self-check feature, the UHF test transmitter resides in the RCE test set and may be used to simulate RCE subsystem characteristics in all phases of flight, entry, and landing configurations.

During actual Lander RCE checkout, the only manual operations are preparatory in nature and consist of properly tuning the receiver to the approximate RCE frequency, selecting the proper receiver bandwidth, etc. Once these conditions are established or verified, the system is placed under STE computer control and testing becomes automatic.

Using the Viking test system

As can be seen in Fig. 2, the Viking system test equipment utilizes three distinct checkout capabilities: the TDLR and RA checkout sets, and the RF communications test set (RFCTS). Each of these test capabilities is configured and monitored by computer-controlled discretes through the VLC signal-conditioning set, with the RF instrumentation test set (RFITS) serving as a buffer between the flight equipment checkout sets and containing frequency-measuring equipment, a computing counter, voltmeter, function generator, etc. In this way, common RA, TDLR, and communication equipment measurements are conveniently utilized.

The RFITS contains interface and downlink timing circuits to coordinate data from the three checkout sets. (The data collected in RFITS come from two asynchronous sources: the STE computer and check-

Implementing RA checkout

Mathematical analysis has indicated that the power envelope of radar altimeter signals returning from the Martian surface may be approximated by (see illustration)

$$1 - e^{\frac{-(t - t_d)}{\tau_1}} \Bigg|_{t_d \le t \le t_d + \tau}$$

where τ_1 is a variable time constant for the leading edge, t_d is the return delay time, and τ is the radar pulse width. The trailing edge of the return signal may likewise be approximated by

$$e^{\frac{-(t - t_d - \tau)}{\tau_2}} \Bigg|_{t_d + \tau \le t \le t_d + 10\tau}$$

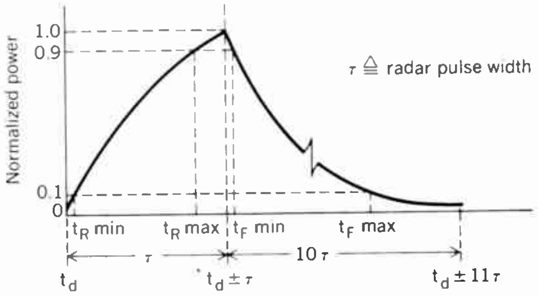
where τ_2 is a variable trailing-edge time constant.

This return signal is generated by the radar altimeter return simulator (RARS) in the RA checkout set. A signal representing the false target (aeroshell reflection) is also generated by the RARS.

These signals are generated by processing a 1-GHz signal produced by a 1-GHz voltage-controlled oscillator. To simulate the Martian surface, decorrelation of the return is required. These characteristics are approximated by a noise modulation assembly. The pulse rise and fall characteristics are achieved by a modulation assembly consisting of a linear modulator, RF switch, and other components. The signal output level is established by a 110-dB digitally controlled attenuator.

The aeroshell return is processed in a simular manner and combined with the surface return to form the RARS output.

Normalized mean power envelope.



out set internal sources.) Uplink data are modified and buffered by timing and signal conditioning so that the uplink data processors may properly format the data for use by the checkout sets. Uplink data words to RFITS are 32 bits long, whereas uplink words to the checkout sets may be from 5 to 15 bits in length, depending upon the parameter controlled.

The ability of the RA and TDLR checkout systems to simulate signals modeling the Martian surface has already been demonstrated (see Boxes, pp. 47 and 50). With present technology and the availability of microwave components, such systems are easily developed to be computer-controlled and virtually fully automatic, depending only on the level of automation desired.

In developing the direct communications and RCE (relay communications equipment) subsystems, however, a minimum of new RF design was initiated, and equipment was used that had generally been in existence for many years. In this case, the development requirements were primarily those of modifying off-the-shelf equipment in the form of transmitters, receivers, etc., and implementing suitable interfaces with the other STE hardware.

In operation, the DCS checkout portion of the RFCTS simulates the deep-space instrumentation facility interface with either the Orbiter or Lander DCS subsystems. The RFCTS also measures pertinent parameters of the DCS components; Table II itemizes just a few of the many test functions performed—sufficient to demonstrate the versatility of computer-controlled testing.

The RCE portion of the RFCTS simulates the Orbiter radio relay system and, in conjunction with the RFITS, monitors the UHF RCE transmitter signal for power output levels, frequency, and spectral quality (accomplished visually). A basic block diagram of the RCE and checkout systems can be seen in Fig. 5. The STE computer has dual interface capability with the VLC equipment, as well as providing a data downlink with received RF data; thus affording a thorough test of flight components. It should be noted that RCE checkout can be implemented through either a hardline or an air link.

By STE computer control of the GCSC and DAPU, the flight RCE may be stimulated. The RCE checkout set receives and demodulates the signal, downlinking the data through the RFITS and VLC signal-conditioning set to the telemetry data conditioner and, finally, to the STE computer.

The authors wish to acknowledge the assistance of other members of the Viking team who participated in the preparation of this article. Particular thanks go to C. Brudos for his interest and encouragement; to B. Preston and R. Rung for extensive editing; to W. Kamsler, M. Doty, D. Rivers, H. Summers, K. Vest, and J. Wahnish for their review and technical suggestions; and to W. Goslee and W. R. Jones of the NASA Viking Project Office and E. N. R. Nelson of Kennedy Space Center for their contributions.

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Claxton W. Rea has been in aerospace electronic design since 1956. At Martin Marietta, he is responsible for the design of terminal descent landing radar (TDLR) automated RF checkout equipment for the Viking Lander. He has also been responsible for the design of power systems, instrumentation, and telemetry equipment used on the Titan series of missiles and booster rockets. Mr. Rea was graduated from the University of Colorado with a B.S.E.E. in 1951.

HVDC to illuminate darkest Africa

By 1975, electric energy will be produced in northwest Mozambique in one of the largest hydroelectric systems under construction

Over the course of many years, the "dark continent" has been steadily brightened by large-scale power-development schemes that are thrusting Africa into the forefront of contemporary technological progress. Across a sparsely populated land mass where the often inhospitable "back of beyond" resists any form of technological intervention, high-voltage dc (HVDC) transmission from points of power generation to load centers—because of relatively low transmission losses over long distances—becomes a logical choice.

Faced with the awesome demographic and geographic constraints of one of its African colonies, the Portuguese Government, about ten years ago, began extensive investigations into the possibility of commercial development of the Zambezi River valley in northwestern Mozambique (or, currently, Portuguese East Africa). A narrow gorge of the river, called "Cabora Bassa," seemed the ideal site (Fig. 1) for construction of a multipurpose dam for

- Generating low-cost electricity to develop the area's rich mineral resources
- Regulating the river flow for flood-control purposes
- Irrigating widespread agricultural areas

Further, financing of the project could be amortized by the sale and transmission (over a distance of 1400 km) of large surplus blocks of electricity to the neighboring Republic of South Africa.

Needless to say, the Portuguese Government proceeded with its project and, commencing next year, electric energy will be generated in one of the largest hydroelectric schemes presently under construction on the African continent. (Its chief competitor in scope is the Inga power complex in Zaïre, which will ultimately have a generating capacity of more than 4000 MW. However, development of this output is not expected for decades and the project consists of a number of dams and related power stations, none of which will exceed a generating capacity of 4000 MW.)

Scope and "hardware" of the scheme

Any hydroelectric project is a true interdisciplinary venture in every sense of the word, entailing the close collaboration of electrical, mechanical, structural, and civil engineers—plus the best efforts of geologists, hydrologists, agronomists, and economists. The physical hardware that is the "concrete" product of the intensive Portuguese planning includes a high dam, the necessary substations, converter stations, and specially designed conductors and transmission towers to carry the high-voltage direct current.

To accomplish one of these objectives—the planning, design, and construction of the converter stations for the world's longest and highest-voltage dc line, the German companies AEG, BBC (including the Swiss Brown, Boveri), and Siemens entered into a joint-venture arrangement as members of the international ZAMCO consortium to which the Cabora Bassa contract was awarded. Indeed, about a decade ago, these three companies had formed the "Arbeitsgemeinschaft HGU" (high-voltage dc transmission working group) for a common R&D effort into all areas of HVDC.

Now, a closer look

The first phase of Cabora Bassa involves building a power plant with an output of more than 2000 MW, on the southern bank of the Zambezi. Nearly all of the generated power will be transmitted from this plant to South Africa (Fig. 2). A second power station, with nearly the same output capacity, will be constructed, at a later date, on the northern bank, and this will make Cabora Bassa the largest individual hydroelectric power station in Africa.[1]

During early studies, both ac and dc transmission were considered, including four systems at 400 kV, two systems at 500 kV, and two systems at 750 kV. Comparisons indicated that the optimum cost would be attained with a dc voltage in the range of 1000 to 1100 kV. However, a voltage of ±533 kV was eventually selected.[1]

The power plant and substations will be erected in three stages: the first includes three turbine-generator sets and four converter groups to be ready for commercial operation by mid-1975; the second stage consists of the installation of an additional turbine-generator and two more converter groups for operation by the beginning of 1977; and, by early 1979, a fifth turbine generator—plus the seventh and eighth converter groups—should be on the line to complete the final phase.

The dam and its appurtenances

The double-curved Caborra Bassa dam is being built between granite and gneiss walls in the steep canyon, or gorge, previously mentioned. It will have a height, from base to crest, of about 164 meters, and a crest length of 303 meters.[2] The impounded reservoir,

M. Klein Brown, Boveri & Cie. AG
J. Linnenkohl AEG-Telefunken
H. Heidenreich Siemens AG

or lake, will have a surface area of 2700 km² (667 000 acres), a length of about 250 km, a storage height of approximately 140 meters above the downstream level, and a reservoir capacity of some 52 000 million cubic meters (41.5 million acre-feet).

The powerhouse, which is now in the final stages of construction, is formed by a cavern (underground gallery) 220 meters long by 29 meters wide by 57 meters high. It will contain five Francis-type turbines directly coupled to vertical-shaft generators (see Fig. 3 for further details).

The block transformers are housed in a separate cavern that lies parallel to the powerhouse cavern. Each transformer group (consisting of three single-phase transformers) is connected with its appropriate generator through a sloping tunnel. The electricity generated will be carried from the transformer cavern, through a vertical shaft about 120 meters in height, to a surface platform by means of 220-kV single-core oil-filled cables. From this platform, overhead transmission lines will lead to the Songo substation, a distance of about 6 km.

[1] A downstream view of the Cabora Bassa gorge of the Zambezi River in the northwest of Africa's Mozambique. This photograph was taken while the Cabora Bassa dam was under construction in November, 1973.

The substations

The Songo substation is situated on a plateau that is almost 900 meters above sea level; it was chosen because of its favorable geographic and climatic conditions. This substation is presently equipped with a double 220-kV bus bar system that will be extended by a third bus bar in the future. Single feeders connect the eight converter transformer banks, the two ac filter circuits, and the two auxiliary transformers to this bus. At the dc side, eight six-pulse converter groups are series-connected in a bipolar arrangement.

Four groups per pole produce a transmission voltage of ±533 kV. (With a rating of 240 MW—133 kV, 1800 amperes per group—the total capacity of this converter substation will ultimately reach 1920 MW.) This power will be transmitted 1400 km to the Apollo substation that is situated near Pretoria and Johannesburg, South Africa.

The Apollo substation is arranged similarly to that at Songo. The power will be fed to the 275/400-kV network of the Electricity Supply Commission (Escom), the major utility of South Africa.

When this HVDC link goes on the line in 1975, it will incorporate the longest transmission line ever built—and will be the first long-distance HVDC transmission system (Fig. 4) to use outdoor-type oil-cooled and -insulated thyristor converter valves. When the final stage is completed, Cabora Bassa will have the highest transmission voltage and power per bipole used, to date, in an HVDC link.

Converter/inverter/rectifier stations

As previously mentioned, the transmission voltage of ±533 kV is obtained by connecting four converter bridges, with a rated voltage of 133.3 kV each, in series to form one pole. (This arrangement was requested by the client because of the limitations of the mercury-arc technique that was state of the art at the time of working out the call for bids in 1967. In the course of contract negotiation, however, the client opted for the later thyristor alternative offered by ZAMCO, but the original voltage arrangement remained unchanged.) The installation schedule calls for the power scheme to operate at ±267 kV in the first stage, at ±400 kV in the second stage, and at ±533 kV in the third and final stage. But the rated current will be 1800 amperes in all three stages.

On the dc side, each converter group is equipped with a bypass switch and with a shunting disconnector. Because of the thyristor technique used, no bypass valve was considered necessary. The converter groups are individually connected to the dc bus by means of a set of polarity reversal disconnectors which are effective in case of persistent line faults. While one pole continues to operate at its rated power, the faulty line is disconnected, the converter groups of the corresponding station pole are individually reversed in polarity, and the station pole is then paralleled to the unfaulted one. Thus, transmission is continued nearly in full nominal capacity, in monopolar operation, using ground return. Individual polarity reversal of bridges was chosen to avoid the necessity of increasing the insulation to ground of half of the converter groups.

The equipment and design of the inverter station at Apollo are identical to those of the rectifier station at Cabora Bassa. Provision is even made for power-flow reversal to allow for the possible development of the African systems.

At Apollo, the ac system voltage is 275 kV. To compensate for the reactive power of the converters and give the total station a leading power factor, Escom will install two capacitor banks besides the ac filters.

The arrangement of the dc circuit—i.e., four valve groups in series per dc pole—together with the insulation characteristic of the thyristor valves, requires a strict and efficient overvoltage protection scheme. With the arrester arrangement designed for Cabora Bassa, the overvoltage protection of the HVDC station equipment is based mostly on the valve arresters, directly connected in parallel to each valve (type *B*). These arresters secure overvoltage protection under all possible circumstances, and under combined fault conditions. In principle, they protect the whole station, provided the converters are in normal operation.

To protect against possible overvoltage stresses at non-current conditions, the bridge arresters (type *C*) and the phase-to-phase arresters (type *A*) are added.

To achieve maximum security, the protective levels of all arresters have been statistically defined and were coordinated with the withstand levels of the equipment by means of statistical methods.[3]

Special attention was paid to the external insulation inside the converter station such as post insulators, bushings, and suspension insulators. Intensive long-term tests have been conducted to find optimal shapes of insulator sheds. A specific creepage distance of about 30 mm/kV was chosen.

The critical thyristors

Each converter transformer bank consists of three single-phase units with OFAC (oil-forced, air-cooled) cooling. In order to obtain 12-pulse operation, the transformers are connected alternately in star–star (Y–Y) and star–delta (Y–Δ) configurations. Because of the parallel connection at the ac side and the series connection of the converter bridges, the converter transformers had to be designed for four different dc potentials, while the phase-to-phase voltage at the valve side is equal for all transformers (Fig. 3). To compensate ac voltage variations and to achieve an optimal control angle of the valves, the transformers are equipped with on-load tap changers.

Many investigations had to be performed to prove the integrity of the oil-paper insulation for the high, mixed dc–ac voltage stresses. The dc level of the valve winding against ground of the highest bridge is 466 kV, and the BIL (basic insulator level) is 1550 kV. The smoothing reactors with similar insulation have to withstand a dc voltage of 533 kV.

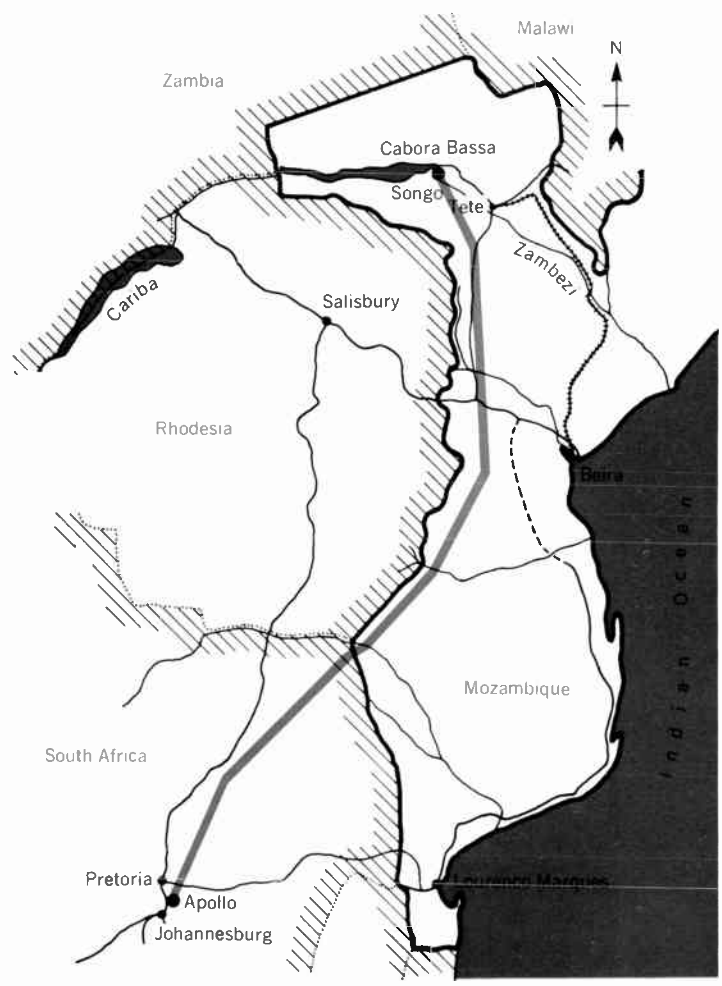
Because of the equal phase-to-phase voltages at both windings, only one single-phase unit from each vector group is necessary as a spare, which is of the type with the higher dc insulation on the valve side.

In this project, the thrystor technique of the previously mentioned German–Swiss high-voltage dc technique working group is used. The design is the result of a long sequence of research and development work on components, valve models, and experimental valves. Tests under near-service conditions were carried out in the world's most powerful HVDC test plant at Mannheim-Rheinau, Germany, with definitely good results.[4]

For economic reasons, an outdoor installation of the valves was chosen for this project taking into consideration the good climatic conditions in both terminal stations. One converter bridge consists of three twin valve units. As in transformer techniques, a steel tank is used for housing all integral parts of two bridge arms which are connected to one ac phase. The necessary connections are brought out through bushings as with transformers. Transformer oil is used for insulation and cooling.

Each valve unit is installed on a platform insulated against ground potential by post insulators. The difference in bridge potentials resulting from the series connection is taken into account by graded external insulation of the platforms. This makes possible the use of identical valve units throughout the system and a free interchangeability, an important advantage

[2] Route of the overhead dc transmission line of the Cabora Bassa hydroelectric project. The line will extend over 1400 km from its origin at the Songo substation in Mozambique to the Apollo substation in South Africa. The surplus energy delivered is expected to finance this project.



pairs of thyristors in series. Their individual grading and gating circuits make up a tier, together with a combination of nonlinear reactors. Furthermore, capacitors for compensation of stray capacitances have been provided.

Grading and damping, necessary for equalizing and limiting the static and dynamic voltage stresses of the thyristors, are achieved by a pair of antiseries-connected CADs (controlled avalanche diodes) paralleled to each thyristor pair in addition to the use of capacitors and resistors. These CAD elements limit the peak voltage arising from transient overvoltage conditions.

The magnetic-type firing system for the thyristors consists of a bushing-type triggering cable which represents the primary winding of a series of ten toroid-shaped pulse transformers centered around the cable. Each pulse transformer has 28 center-tapped secondary windings which transmit the firing pulses to the 28 gating circuits of each half-tier, fed through the triggering cable.

For the second and third stages, advantage will be taken of thyristors with higher blocking capability while the principle of full interchangeability will be maintained.

Control and protection equipment

The control of the Cabora Bassa HVDC scheme is based on the principle of marginal current control. This means that normally the rectifier station operates with current control and the inverter station functions with extinction-angle control to minimize the reactive power demand at the receiving end. The inverter is also equipped with a current controller, whose reference value is reduced by a marginal current value compared with the reference value of the rectifier. This enables continuous energy transmission in certain fault cases, with reduced power.

The functions of the control equipment can be divided into different parts, each of which corresponds to a definite part of the transmission system: substation control for setting the power to be transmitted; dc pole control for setting the current reference value, current control, and voltage control; and bridge control with firing-angle and extinction-angle control and signal processing.

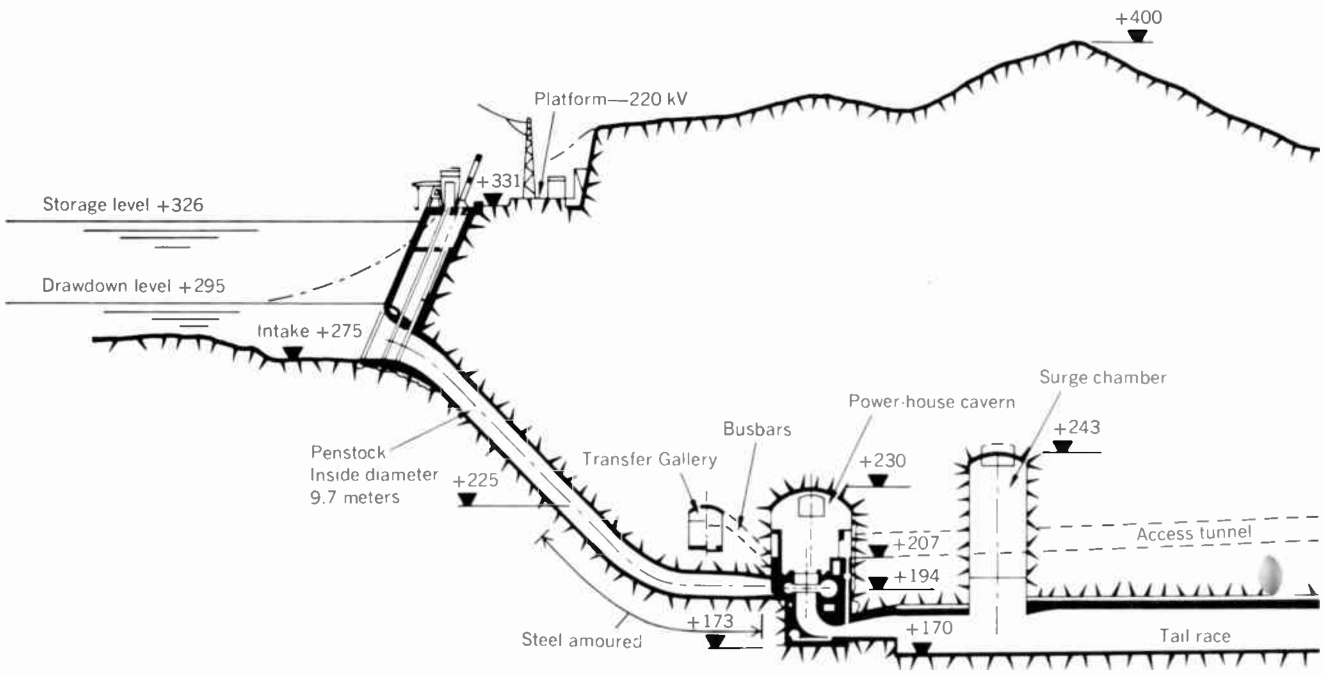
The station control gives the power reference value depending on a hand-set power demand. This power demand is given to a master power controller comparing the switching conditions of the HVDC system and power station and coordinating the rate of change of dc power with the possible rate of change of the generated power. Taking into consideration these figures, the power reference value is ascertained for each dc pole separately.

Because of the importance of this equipment for operation and protection, the current controller is duplicated for each dc pole—one covering the actual value obtained from dc transformer in the smoothing reactor, and the other covering the actual value measured in the connection to the grounding electrode. Both controller outputs are compared and the one demanding a lower current becomes effective.

Voltage control is performed by adjusting the transformer ratios with tap changers in the inverter station, which normally operates the extinction-angle control. With the help of the transformer tap changers in the rectifier station, the firing angle α will be kept within 16° ± 3°, and the ideal no-load voltage can be limited to a predefined value. A special device ensures that all tap changers of one dc pole will have the same position and will be operated simultaneously, only.

The most important element for converter control is the gate-control system for sending the firing pulses to the different valves under normal and fault conditions. Under normal operating conditions, α is given by the dc pole control, in the rectifier substation. In the converter control of the inverter substation, either the firing angle α or the control angle γ required by

A longitudinal view of the Cabora Bassa power plant.



the extinction-angle control is selected. Furthermore, the control angle can be controlled externally, which is necessary for protection purposes and for carrying out certain control programs. All elements of the firing system are monitored continuously.

If, in operation, the actual extinction angle becomes smaller than a minimum value, the extinction-angle control provides a signal that initiates the immediate firing of the next valve and reduces the link current to prevent further commutation failures.

For the overcurrent protection of the thyristor valves, two main elements are effective:

• The current controller in case of faults on the dc line, shifting the converter into inverter operation, thus reducing the fault current and discharging the line.

• The differential protection of single converter bridges and dc poles in case of faults within the converter station area. This differential protection evaluates the currents in the converter transformers, in the smoothing reactor, and in the ground side of the pole, respectively. If the sum of the currents on the ac side exceeds the value of the dc side by a given constant value, overcurrent diverters of the corresponding converter bridge are initiated and the bridge is taken out of operation.

Detection of dc line faults is undertaken by

1. Fault detection with the help of rate-of-exchange measurements on the incoming travelling waves.
2. Differential line protection by comparing currents at the beginning and at the end of the dc line.
3. Open-wire detection by comparing the current reference value with the actual value.

In case a dc line fault is indicated, the direct current will be brought to zero and an automatic restarting circuit initiated. Three starting attempts, beginning with zero line current and voltage, are performed after certain reduced dc-line voltage. If all restarting attempts are unsuccessful, the signal "parallel operation of the dc poles" is given; in other words, the dc pole involved can be switched over to the sound pole by the operator.

The switching "on" and "off" of the converter bays can be done manually or automatically, ensuring the correct sequence of cooperation between auxiliaries, valve control, and isolator and breaker operation. Switching "off" can be executed by means of three different programs: "normal switching off," initiated by hand operation; "rapid switching off," caused by automatic control—with a somewhat different program for valve control, thereby saving time for the entire procedure; and "emergency switching off," started simultaneously by the differential protection and by providing tripping signals to the overcurrent diverters, ac breaker, and bypass switch.

Transmission lines

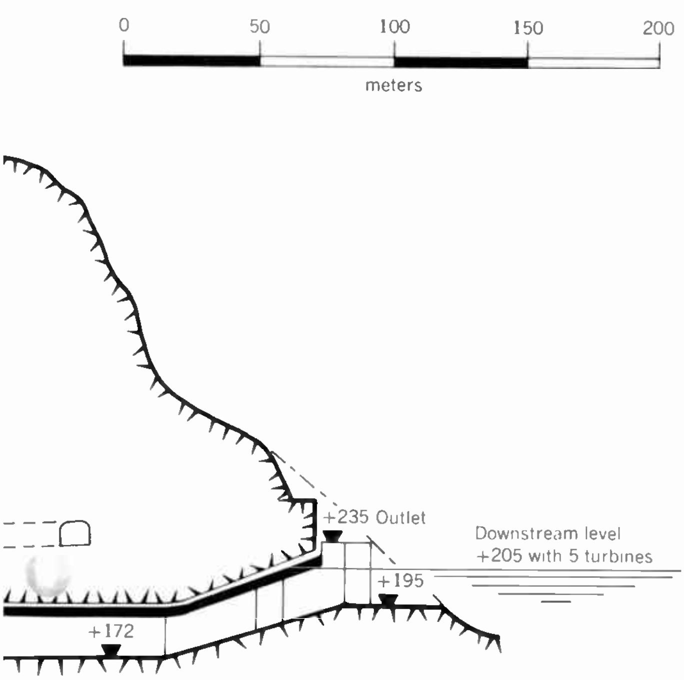
To obtain a high degree of transmission reliability, two monopolar lines were erected, running in parallel at a distance of about 1 km apart. The spans are about 425 meters between towers. Insulators are of the antifog glass type, with long leakage paths (specific creep lengths of 23 to 27 mm/kV). To avoid corona and radio-interference problems, quadruplex bundles of ACSR (aluminum core, steel radial) conductors of $4 \times 565/29.5$ mm^2 cross section were used. Lightly insulated ground wires, because they form the second conductor for the power-line-carrier system, are used for telecommunications purposes.

Telecommunication system

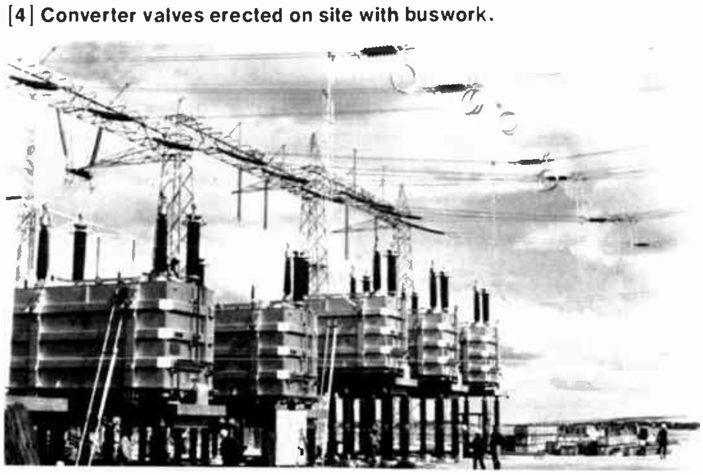
The operation of the Cabora Bassa HVDC transmission system is not exclusively based on telecommunication facilities. However, a communication link between the converter stations will considerably improve its operational properties.

It has been found that because of the very long distance between the converter stations, a power-line-carrier (PLC) link is a most economical and reliable means for telecommunication, using a power conductor and the ground wire.

The normally used pole-to-pole coupling is not feasible here since the distance of about 1 km between the poles would cause extraordinarily high attenuation. Using two independent lines, two completely sepa-



[4] Converter valves erected on site with buswork.



rated PLC-transmission systems could be provided resulting in a high service reliability. Important information is transmitted twice, each transmission independent of the other. This information mainly includes reference values for current control, control signals for switching bridges "off" or "on," polarity reversal and paralleling of a station half for emergency operation, operation conditions and switching positions, information about faults such as rectifier blocking at ground faults, and differential protection. For special information such as current reference values, high-speed channels are available. Furthermore, direct telephone and telex connections are provided.

Since the entire transmission line is about 1400 km in length, two relay stations are needed, each located approximately 300 km from the respective converter station. For the external sections of the lines, a relatively high transmission frequency of 300 kHz was chosen (due to the noise level coming from the converter stations) so that a favorable signal-to-noise ratio is obtained. For the center section of the line, which is not influenced by the converter noise, a low transmission frequency was chosen (40 to 88 kHz) so that it is possible to bridge the remaining 800 km without intermediate amplification.

AC filters are provided in both terminal stations of the HVDC transmission system to absorb the harmonics produced in static converter operation. At the same time, the filters provide part of the fundamental reactive power required for conduction period, control, and commutation. The filter circuits are rated according to their fundamental current and the characteristic harmonic currents occurring in 6- or 12-pulse operation. A special requirement was imposed by the specification that the individual harmonic voltages should not exceed 1 percent of the fundamental line voltage and by the relatively small fundamental reactive power, which necessitated accurate filters and high reactor quality factors.

Each filter system has a total fundamental reactive power of 400 MVA and is subdivided into two identical stages, each having single-tuned shunt filters for harmonics of the fifth, seventh, eleventh, and thirteenth order, and a damped high-pass filter for higher harmonics.

For the accurately tuned three-phase filter circuits, preference was given to a star (Y) connection with grounded star-point to permit favorable insulation grading. Here, the inductances, comprising coreless, oil-insulated reactors, are located at the star-point.

Each phase of the tuned filter circuits can be set with a high degree of accuracy, automatically or manually, to the particular resonant frequency, by means of the reactor tap changer. This allows compensation of changes in capacitor values due to temperature variations and manufacturing tolerances in the reactors and capacitors.

Grounding electrodes

To maintain a monopolar operation during a persistent fault on one line pole, the grounding electrode near each converter station is rated for a continuous operation with 1800 amperes. In case of a paralleled converter station poled to one line, the grounding electrodes have to carry 3300 amperes. This operation mode is contractually limited to a time period of 72 hours. Depending on the failing pole, the polarity of the electrodes is given. Therefore, each of the electrodes has to be suitable to operate as an anode or cathode. In addition, the grounding electrodes have the function of carrying the small asymmetrical current between the converter station poles during normal operation.

By geophysical measurements, suitable sites for the grounding electrodes were chosen. In the vicinity of the Apollo substation, a small valley was found to be the most favorable area on which to construct a grounding electrode.

Near the Songo substation, an extremely good conducting soil layer at a depth of 30 to 60 meters was found suitable to anchor a rod-type grounding electrode. Three rods consisting of graphite conductors will connect the two grounding electrode lines running in parallel between the Songo substation and the grounding electrode site.

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Manfred Klein is head of the Project Group Cabora Bassa for Brown, Boveri & Cie. in Mannheim, Germany, where he has been involved in the design and execution of the Cabora Bassa project since 1968. He participated in the project's layout and in HVDC system development work. Manfred Klein received the Ing. Grad. degree (energy techniques) from the Staatliche Ingenieurschule Essen (now Gesamthochschule Essen), Germany, in 1965.

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Horst Heidenreich is in charge of the execution of the Cabora Bassa project for the Siemens Company, Erlangen, Germany. He has been involved in the design and construction of the HVDC test plant at Mannheim-Rheinau, Germany, since 1965. He joined Siemens in 1955, at which time he worked on HVAC plants and static and rotary converters. From 1952 to 1955, he headed the electrical department of a utility power station. Mr. Heidenreich received the electrical engineer degree at Mittweida, Germany, in 1952.

Making up the collective mind

Decision analysis, by combining inputs from diverse and often dissident sources, seeks the best risks for industry or government

A hurricane is bearing down on New Orleans. At the ready is a Government-operated aircraft equipped with silver-iodide cloud-seeding apparatus. The question: To seed or not to seed . . .

According to a Stanford Research Institute analysis of Project Stormfury, the U.S. Department of Commerce's experimental program to modify hurricanes, seeding probably reduces peak wind velocities moderately and resultant property damage substantially. But the SRI report also points out that no one can prove seeding didn't actually make things worse.

Should seeding be implemented, a disgruntled victim could later claim his property damage had been increased. On the other hand, if seeding is not attempted, someone else might well sue the Government for not doing everything possible to protect the city's population.

What to do?

Such dilemmas are not uncommon in today's complex world. Of course, leaders and public officials have been making decisions through the ages, and they have often had to take substantial risks. Think of Hannibal, or Columbus, or Lincoln. But the massive intrusion of modern-day technology into questions of sweeping public concern has tended to increase associated complexities beyond the capacities of individual decision-makers. At the same time, technology has also tended to raise the ante while increasing the frequency of the gamble.

Things happen faster today. Response times must become ever shorter. Yet the complexity of contemporary problems makes effective response impossible without the collaboration of many people of different backgrounds. In Washington, it is not uncommon to see sociologists, engineers, scientists, politicians, businessmen, and labor leaders all serving on a committee as Government advisors.

Given the complexity of modern social services, political problems, and technical hardware, it is not surprising that the young discipline of decision analysis has enjoyed a surge of interest and influence. Decision analysis seems to be an idea whose time has come. But is it a fad, or a truly effective, viable approach to solving problems? In assessing that question, let us consider the consequences of some key decisions made in recent years *without* benefit of decision analysis.

Bumper-to-bumper bungles

Perhaps one of the United States' most critical and illuminating experiences with piecemeal decision-making has been in transportation policy. Following World War I, it became the national dream to own a car and a home in the suburbs. And manufacturers, weaned by trucking from dependence on rail lines, dispersed their production facilities across the landscape. The Government obliged by financing highway construction on a grand scale. At the same time, the demand for ever-faster transportation and the interests of national defense led to the heavy subsidization of airlines.

In its preoccupation with these newer, rather glamorous modes of conveyance, the Government continued its tight regulatory control of the railroad industry while withholding financial aid. Starved for needed maintenance and modernization funds, the railroads began to atrophy. A similar fate befell intraurban mass transportation, also a victim of aggressively indifferent Government.

We have, as a result, seen cities plagued with automotive arteriosclerosis while their centers suffer decay in the wake of a massive industrial/residential exodus. Even more ominous, almost everyone has become the victim of potentially lethal air pollution, largely caused by the proliferation of internal combustion engines.

Alarmed by deteriorating air quality, the U.S. hastily responded by mandating automotive emission controls so stringent that they could only be achieved (under the present state of the art) by greatly increasing fuel consumption. Manufacturers were legally required to equip new cars with such devices just in time to coincide with a worldwide fuel shortage and the melancholy discovery that oil reserves are decidedly finite.

These experiences make it painfully clear that we must have a more orderly procedure for dealing with problems, a process that can more fully account for the potential consequences of our decisions. Decision-analysis techniques appear eminently suited to fill this need.

Harnessing the human element

An elementary analysis of group decision-making suggests a tradeoff among three common human traits:

- Greed—because whatever people want, they seem to want all they can get.
- Impatience—because whatever they want, they want it now rather than later.
- Fear—because whatever people want, they want it without risk.

These motives are not usually described in such blunt terms for we like to consider ourselves guided by loftier and nobler purposes. But just as psychiatry

Myron Tribus Xerox Corp.

teaches that individual emotional health means facing inner drives squarely and honestly, I believe our social health also requires an understanding and acceptance of primitive conflicts, no matter how base they may at first appear.

Since we cannot satisfy our greed, impatience, and fear all at once, we are forced to trade one against another. This is why we need a better method for group risk-taking. But is decision analysis the answer? Why not some other approach? Is there a better way?

A better method—at the very least—should not contain the flaws recognized in existing systems, and it should not introduce new flaws. Actions and objectives should never be obviously at cross purposes with one another. An improved decision-making scheme must satisfy four requirements. It should be:

- Precise
- Honest
- Universally applicable
- Internally consistent

These requirements alone are not sufficient for success, but failure to satisfy them will make a logical process invalid. A further discussion and mathematical representation of these four requirements is presented in the box below. Also identified is the logical structure that underlies the decision-analysis concept.

As a field of inquiry moves from science to engineering, acceptance depends upon experience. After all, a theory can be everything except useful—and still be scientifically valid.

Putting promise into practice

During the last four years, I have had the good fortune to work with Ron Howard, Jim Matheson, Carl Spetzler, and Ed Cazlett of Stanford Research Institute. I've watched them develop the techniques required to turn decision analysis from a science into an engineering tool encompassing three distinct phases (Fig. 1).

In the deterministic phase, the good analyst earns his pay, for he must render explicit that which was intuitive before. It is at this point that ambiguity is removed. Sensitivity analysis reveals which variables are important, which are under our control, which are consequences, and which variables are part of the environment.

In the probabilistic phase, the variables not under

Four musts and a maybe

There are four minimal requirements for acceptability of a decision-making process. While their presence will not guarantee success, their absence generally assures failure. Briefly stated and defined, these requirements are:

- *Precision*—At the very least you should be able to distinguish what is said from what is not said. What is said should be an assertion. For that assertion, there should be a unique denial. Ambiguity exists when it is not possible to formulate a denial to an assertion.

The meeting of this requirement may be verified with Boolean algebra, which was designed to test the logical consistency of assertions. If statements cannot be expressed in Boolean symbols, they are ambiguous. (But the ability to express ideas in Boolean algebra does not *guarantee* freedom from ambiguity.)

- *Honesty*—The validity of a statement is always contingent on the validity of other statements. The "other statements" should be made explicit. If the context is changed, the validity of a given statement may change.

This requirement is satisfied by using a Boolean algebra which employs only conditional statements of the form $(A|B)$ . . . "A is true, given B is true.":

- *Universality*—To avoid special-purpose and *ad hoc* procedures, the system of discourse must permit the weighing of the importance of statements of widely disparate topics (it must be possible to compare apples and oranges).

Universal comparability can be achieved only by attaching real numbers as weighting factors for Boolean symbols.

- *Internal consistency*—If a numerical measure, say θ, is to be assigned to a compound statement, AB, conditional on C, that measure should not be assigned independent of the measures assigned to A and B separately, conditional upon C.

The requirement that the measure assigned to (A and B) conditional upon C should depend on what is said about A and B, individually, requires a functional relation. It has been shown[1] that only 11 functions can possibly exist and that all but two of these may be eliminated either on grounds of redundance or because they lead to self-contradictions in special cases. The remaining two functions are symmetric in A and B and are of the form

$$\theta(AB|C) = F[\theta(A|BC), \theta(B|C)]$$

where F is an analytic function of the two variables, $\theta(A|BC)$and $\theta(B|C)$. This final requirement is assured if the assignment of real numbers θ, must obey

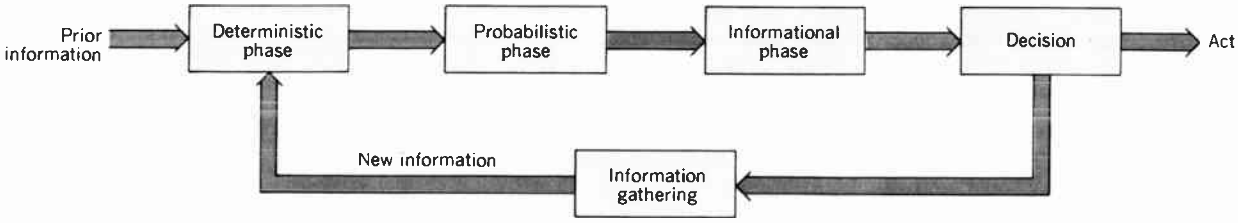
$$\theta(AB|C) = F[\theta(A|BC), \theta(B|C)] = F[\theta(B|AC), \theta(A|C)]$$

In summary, these four defined requirements are characteristics most people would like to see exhibited by an inferential decision-making process. However:

- It is not clear they can be obtained.
- While most people will say they want them, they don't really want all of them all of the time.

The case is quite analogous to our desire to see that the courts administer equal justice to all, except when we ourselves are guilty and brought to trial!

While it is not clear that adherence to the four requirements can be guaranteed, any decision process that obviously violated one or more of them would command little support from scientifically educated people. Agreeing that such violations should not



[1] **Formal decision analysis, analogous to a feedback loop, consists of three main "phases." The decision-maker is always permitted to ask, "Is it worthwhile to learn more?" before committing himself to a final course of action.**

control are examined and represented by probability distributions. This phase is unique to decision analysis. Probability distributions serve to encode our knowledge in the one way required to avoid violating the fundamental requirements.

But decision analysis makes its most important contribution in the information phase, for having represented knowledge as probability distributions, and having drawn a mathematical model of the system under consideration, the method permits the user to see whether it is worthwhile to find sharper probability distributions. *Decision analysis raises the question: Is it worthwhile to learn more?*

In any risk situation, be it poker, government policy, or engineering design, the question is, Should we proceed on what we know or invest time, money, and other resources to gain more knowledge? If we had the knowledge, would it be worth the expense?

Thus far, no other approach to decision-making has provided an alternative way to treat this problem.

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knowingly be tolerated (which is not the same as guaranteeing that they won't occur) amounts to specifying a great deal, for it turns out that the functional equations just introduced have unique solutions.[1] Therefore, it is useful to see what limitations on allowable logical processes result from applying the four requirements as constraints.

One solution to the functional equations is:

$$F[\theta(A|BC), \theta(B|C)] = \theta^m(A|BC)\theta^m(B|C)$$

where m is a constant not equal to zero. Putting $p = \theta^m$ converts the result to the more familiar form

$$p(AB|C) = p(A|BC)p(B|C) = p(B|AC)p(A|C)$$

Consistency also requires that the numerical measure assigned to an assertion must be functionally related to whatever is assigned to its denial—i.e., there must be a transformation

$$p(\sim A|C) = T\{p(A|C)\}$$

where $T\{\ \}$ represents a transformation. This leads to the familiar result[1]

$$p(A|C) + p(\sim A|C) = 1, \ p \geq 0$$

The arguments leading to these equations do not involve repeated trials, frequencies of occurrence, ratios of favorable to total number of outcomes, or any other typical justifications often used with probability. The functional relations among the p's arise from the four requirements. The interpretation placed upon the p's is that they represent a unique code in which to discuss partial knowledge—i.e., how to describe what is known about propositions A, B, etc., when you know something but you don't know everything. According to this treatment, there do not exist different kinds of probabilities, just different kinds of knowledge (frequencies of past events, symmetrical systems, etc.). Each type gives rise to a particular technique for assigning numerical values to p. The equations must be obeyed if the four requirements are to be met (Fig. A).

If it is accepted that the symbol p represents an "encoding of knowledge," the problem still remains of translating knowledge into the code. Classical statistical methods provide numerous encoding techniques when knowledge consists of data gathered by repeated trials of the same event. But classical statistical methods offer no clue for encoding other types of information. For example, we may know the total amount of paper used and the number of original copies placed upon a copy machine and wish to encode this specific knowledge as a probability distribution for the number of copies per original. The knowledge is impersonal (it can be communicated from one person to another unambiguously), but it is only partial knowledge about the question: "How many copies are made per original?"

Recognizing that this kind of problem is characteristic of many problems in statistical physics and decision-making, Edwin T. Jaynes proposed a principle which he called "the principle of minimum prejudice," The idea is quite straightforward: Since there are many probability distributions that agree with the partial knowledge, the problem is reduced to choosing one distribution over all others. This criterion of choice implies that something is to be maximized (subject to the constraints implicit in the given knowledge).

Claude Shannon first demonstrated (in 1948)[2] that entropy S defined by

The Stanford group has developed analysis techniques to a point where the pattern of application is easy to follow (Fig. 2). This closer look at the deterministic phase brings the specific tradeoffs among greed, impatience, and fear into sharp focus. Here an explicit treatment of three things is required for a comprehensive analysis:

- The mathematical model representing the system under consideration
- The values that will be used to judge the system tradeoffs
- The time preferences that measure impatience

It is in the latter two areas that decision analysis should make its most important contribution, for it provides the only means by which the questions of risk preference and time preference can be carefully examined.

We still don't have all the tools we need. But good computer programs are now under development to analyze decision trees, consider recurrent situations, simulate decision situations, and help encode knowledge.

Even with our present, relatively crude tools, some valuable contributions have been made. Illustration is drawn from my own knowledge and the experiences of a few close associates.

[2] On closer examination, the deterministic phase breaks down into three models. Decision boundaries, alternatives, outcomes, and system variables are defined or established in the structural model; judgments used to evaluate tradeoffs dominate the value model; and impatience is accounted for in the time preference model.

Hurricanes and fire hazards

In 1970, Stanford Research Institute completed the previously mentioned analysis for the U.S. Department of Commerce dealing with the issue of whether a hurricane should be seeded in an attempt to decrease its potential for damage.[6] The analysis considered whether seeding really helps diminish the fury of a hurricane, the probable variation in damage with wind speed, the effect of natural variability, and even legal consequences.

The first strong evidence for the effectiveness of seeding was obtained from experiments on hurricane Debbie, August 18 and 20, 1969. Debbie was seeded

Four musts and a maybe *(Continued)*

$$S = -k\Sigma p_i \ln p_i$$

measures what is *not known* if all that *is known* is a probability distribution (p_i represents the probability assigned to the occurrence of the i^{th} outcome). When knowledge is *deterministic* (one of p_i's = 1, and the others = 0), the entropy is zero. Otherwise the entropy is positive and the less that is known, the larger the value of the entropy.

Dr. Jaynes used this property of the entropy measure to form the basis for his principle of minimum prejudice[3]:

> *The minimally prejudiced probability distribution is that which is consistent with the given information and which maximizes the entropy, S.*

Based on the fundamental ideas of R. T. Cox[4] and Dr. Jaynes' applications in physics, information theory, and decision analysis, Fig. A is just the foundation of a larger structure (Fig. B). Dr. Jaynes recognized that if the measure p was indeed an encoding of statistics is to provide rules for *encoding* knowledge. And p should not be used to represent frequencies.

Such concepts as random variable, ensemble, superlot, and population would no longer be regarded as statistical theory foundations. On the other hand, theory based in subjectivity was also rejected. The break with previous philosophies was profound. If the assignment of a set of numbers to a set of probabilities is the central task of statistics, then a criterion is necessary to decide which probability assignment (out of all possible assignments) is the "best" one. Prior to Dr. Jaynes' work, the issue wasn't stated this way—although assigning values to p has been the central business of statisticians for over two centuries.

The combined development of statistical mechanics, statistical inference, plus formal definitions excluding four fatal flaws lead to the basic equations for decision analysis[1] and further extend the pictorial representation (Fig. C). Note, however, that value theory is shown hanging in mid-air. At present, decision analysts are forced to use values or utilities arrived at by "reasonable" if not obviously "rational" grounds. Although this is the field's principal theoretical weakness, there are no visible logical alternatives that do not involve a violation of the four requirements. This is why decision analysis has a unique claim on our attention—*M.T.*

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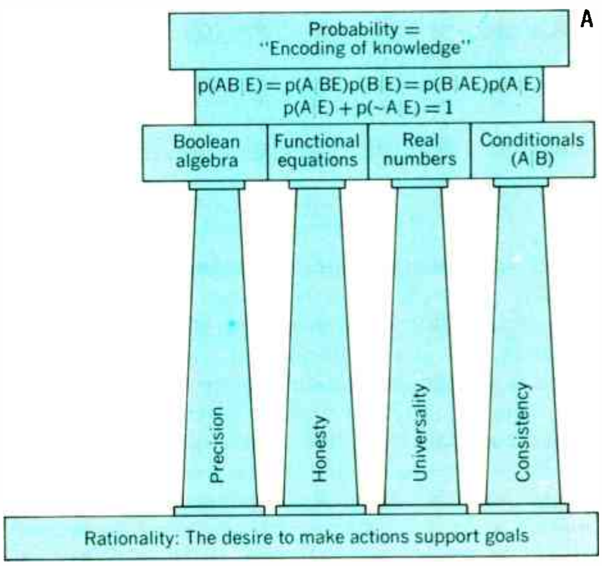
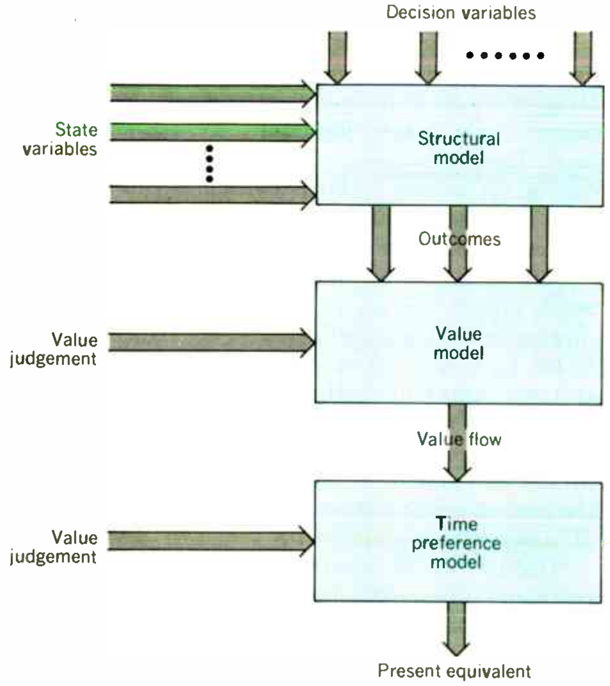
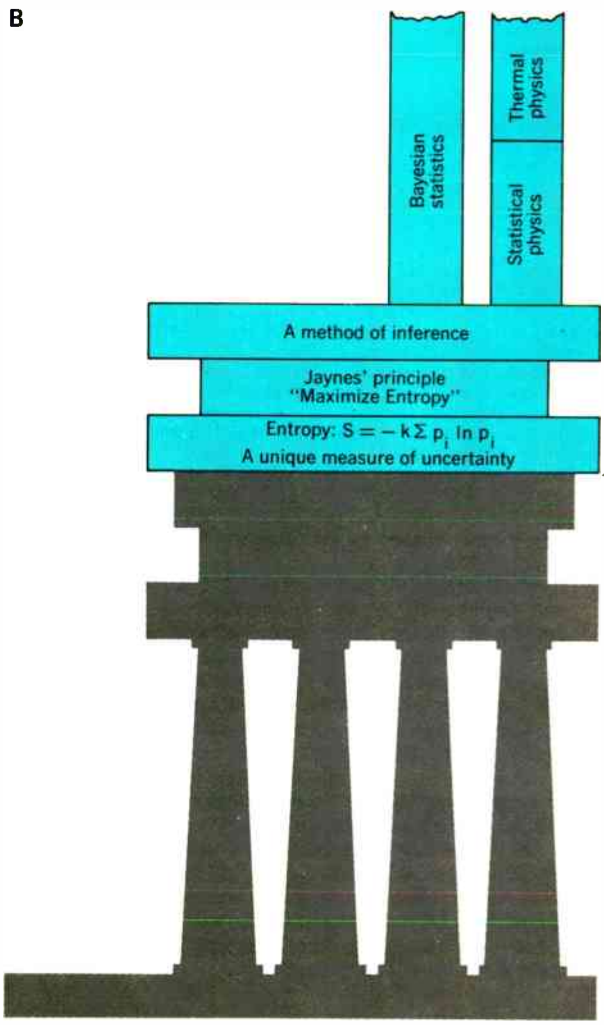


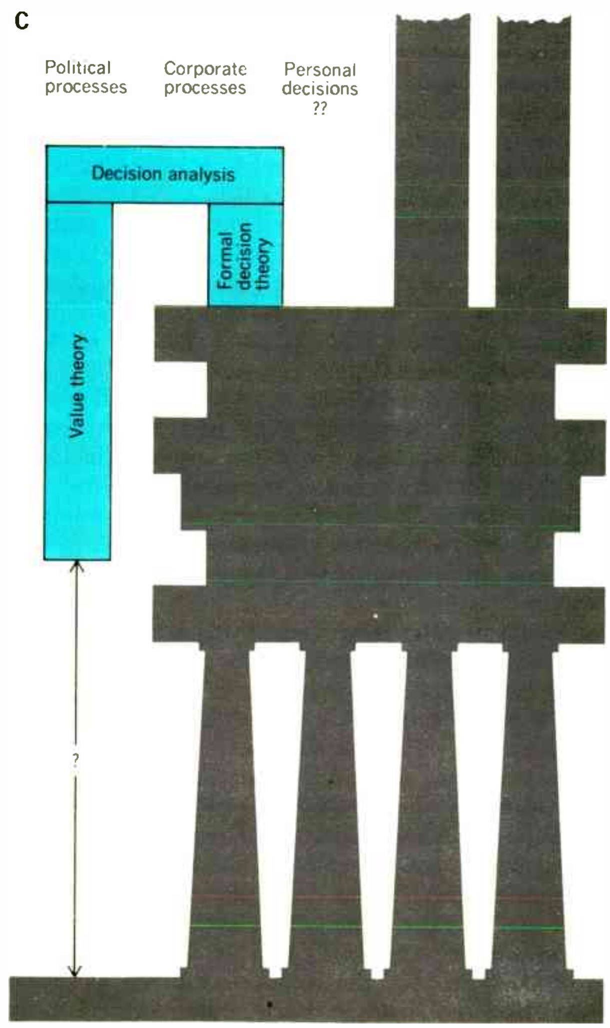


with massive amounts of silver iodide, and peak wind speed reductions of 31 and 15 percent were consequently observed. This evidence, combined with other data, led to the conclusion that "the probability of exceeding a particular amount of property damage is always greater if the hurricane is not seeded than if it is seeded."

But the *decision* to seed cannot be made on this basis alone. Potential legal responsibility for the damages caused by seeded storms has limited Government experimentation to seagoing hurricanes, far from population centers. However, the Stanford report observes that the public may hold the Government responsible for not seeding a severe hurricane, which implies that a responsibility cost should also be attached to the alternative of not seeding. Such a cost would strengthen the implication of the analysis in favor of permitting seeding.

Another recent application of decision analysis involved setting flammability standards for the Flammable Fabrics Act and clearly demonstrated that using a decision-analysis framework could reduce the passion of a debate while keeping it focused on the main issues. In the Flammable Fabrics Act, the U.S.





Congress created an advisory group composed of six consumer advocates, six manufacturers, and six distributors. Members were chosen largely on their ability as lobbyists, used to debating one another in the usual public forums. But once impaneled, their initial confrontations were not very effective and certainly not very enlightening.

Then, decision analysis was introduced. This made it possible to sort out the different parts of the problem and to put them together in a coherent way, taking into account territory where knowledge was insufficient and also identifying those areas where inadequate data did not have to block progress. When the results of the analysis were presented to the advisors, the meetings began to settle down to a more constructive series of sessions.[7]

While exact standards were not derived from this initial effort, decision paths were established that defined the steps leading to a burn injury. Important variables outside the control of sleepwear manufacturers were also identified. For instance, as perceived costs rise for "safe" manufactured items, more and more parents will make garments themselves using materials that do not meet safety standards.

These two examples taken from my Governmental experience serve to illustrate the two possible outputs of a decision analysis: a numerical result (as it was in the hurricane analysis) or the development of a language and philosophy that enables people to cooperate rather than quarrel.

Making believers

As a welcome replacement for pot luck, hunches, politicking, and unvarnished speculation, decision analysis must still overcome several barriers that presently limit its application. These problem areas are similar whether the arena is government or industry, and education heads the list.

Far too few people understand decision analysis. Their reaction tends to be much like the reaction of many people to the computer when it first appeared in the mid-50s. There were those who opposed it for all sorts of reasons while others worshiped whatever came out of the machine.

Beyond the development of an educated clientele is the issue of overcoming some ingrained corporate habits. For example, very few people (including management) really accept the meaning of the word "risk"—that is, "absence of certainty." Risk implies that there is a difference between a *decision* and an *outcome*. But there is often a tendency to "pay only for results."

Another barrier is the lack of understanding of elementary probability theory and a general distaste for things statistical. One fellow put it to me very directly: "I would rather talk about things I know than mess around with these statistics." He said he didn't want to appear before his management talking about statistical distributions, because he feared they would think he didn't know how to do his job!

Indeed, in typical corporate and governmental situations the best tactic may well be to present your case as though you really knew everything—and then make sure no one really acts as though that were true. How to keep the bosses' confidence when you don't have confidence in the situation yourself is as old a problem as human organization.

But there is yet another roadblock of more subtle and formidable proportions. In any organization, there exists an ill-defined "power structure"—various people who play key roles in any decision-making process. The introduction of a new technique always carries the potential threat to change this structure. This threat to existing procedures posed by a new system must not be overlooked.

One of my corporate colleagues, Richard Smallwood, puts it this way: "The people within the organization must have confidence in the analysts as well as the basic precepts of decision analysis. For while it is based upon an underlying axiomatic structure that is very attractive, the actual practical application of decision analysis involves many assumptions. The people who will be affected must be convinced that the analyst making these assumptions will act reasonably and without prejudice.

"Once we begin to introduce decision-analysis concepts and terminology into the actual communication within the organization, a whole new set of problems arises. For example, the question of incentives that will encourage the exchange of unbiased states of information is a difficult problem."

While managers must learn to trust the process, decision analysts themselves must realize that you can't simply approach a manager and ask him what his risk aversion coefficient is or what it should be for the corporation! Nor should an analyst become upset if he tells a decision-maker, "The chances are six out of seven against you," only to be told, "Go ahead, take the seventh!"

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Microcomputer software makes its debut

A first look at the hidden half of microcomputer-based design: the programs that can make or break a system

"We want the microcomputer that offers the most programming power." That's the conclusion of one experienced designer of microcomputer-based CRT terminals, convinced after hard experience that good software is essential to his work.

For the engineer who is a first-time user of microcomputers, software costs can seem almost invisible. The task of learning to program a new machine is so challenging and absorbing that the engineer may find himself looking back on a completed microcomputer-based system design, amazed at the hours of programming that have accumulated.

The long-term experience of computer people is that more than half the design cost of an operating computer system lies in the software portion of the design. For microcomputer applications, with software resources only beginning to develop, programming tends to take up a very large portion of the overall design effort.

That doesn't mean that software-based designs are more difficult than those based on hardwired logic. For example, one Bell Labs test system engineer didn't know anything about microprocessors until he started a project that was to include one of the devices. He and his coworkers soon discovered the tiny computers were easier to work with than their regular logic circuits. Filled with confidence, they wrote their programs, had them "burned" into programmable read-only memory chips, and then wired their test rig together. With very little further effort—it worked!

On the negative side, neophyte users soon discover that the microcomputer world is a Tower of Babel. Every microcomputer manufacturer has invented his own unique machine architecture, and with it goes a unique set of software tools. To switch from one brand of microcomputer to another means that the user has to start from scratch. Previous programs are useless, and there is a whole new language to learn before new programming can begin.

If all this sounds familiar, please notice that history is being relived, with the microcomputer industry now moving through many phases identical to those of the computer industry of the 1950s.

Old computer hands have long known of the language barriers between different computer systems, but they too face some unexpected experiences when they begin to work with microcomputers. Used to working—in large computers and minicomputers—through software operating systems that occupy tens of thousands of bytes of memory, experienced programmers are often surprised to rediscover how much they can accomplish with only 1000 bytes of microcomputer memory.

Howard Falk Senior Associate Editor

One group, at RCA, developed a program to simulate a car—on a TV screen—going through a maze, while keeping track of the travel time. The whole program took 800 memory bytes.

A 1000-byte assembly language program takes an experienced microcomputer programmer about a week to write and debug. But the longer the program, the less efficient the process becomes. Thus, it might take two months to write and debug a 4000-byte program.

One of the toughest tasks is defining the techniques to use in writing the program. That is a task somewhat equivalent to laying out a printed circuit board, and it is time-consuming. Some system designers estimate that—including program design, writing, and debugging—about two program instructions per hour can realistically be produced.

Actually, almost everything that can be said of basic microcomputer software concepts and practice holds equally well for minicomputers and large computers. Microcomputers are true computers like any others, and are capable—given a large enough memory, and adequate peripheral equipment—of performing the same kind of computational tasks as minicomputers or large computers. In fact, it is widely believed that computer systems containing multiple microprocessors may eventually be the preferred way to handle complex tasks now performed by large computers.

The programmer who is used to large computers will find that, with microcomputers, he has to be more conscious of minimizing his use of memory space and of meeting strict execution-time requirements. Such optimizing efforts are important because microcomputer systems are often designed to go into mass production.

When software development costs are spread over many systems—in consumer goods, hundreds of thousands of units of a given microcomputer system may be produced—the software design strategy necessarily concentrates on such factors as minimum use of memory space, or maximum speed of operation, and emphasizes the controls that designers must have over the system. Lower design costs for software become a secondary consideration.

In this article, software for microprocessor-based

Microcomputer software basics

To program a microcomputer, a list of coded instructions is prepared. Each instruction includes an *operation code* and a memory location where that code is to be stored.

Every microcomputer is designed to accept a specified list of operation codes—usually called an *instruction list* (or set). Based on the accumulated past experience of system designers and computer programmers, these instruction lists include an assortment of operations designed to allow the computer to handle efficiently the diverse tasks expected of it.

In the microcomputer, the instructions exist in binary code form as strings of zeros and ones. It is possible to program a microcomputer in binary code—commonly called *machine language*—but the process is very time-consuming, particularly when almost inevitable program alterations and corrections have to be made.

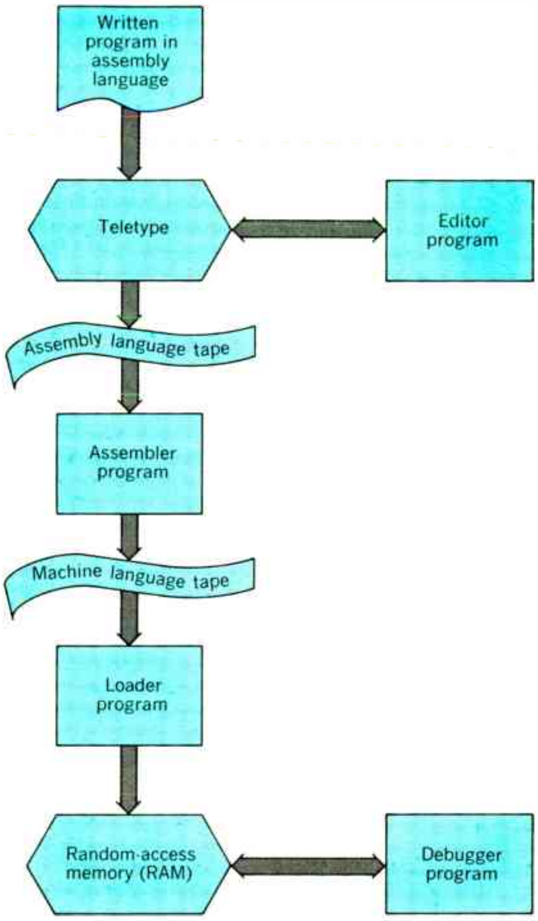
To speed the programming process, and make the microcomputer a practical system component, an *assembly language* is a necessity.

In assembly language, each operation code is a mnemonic code like ADD, STORE, or JUMP. A special program called an *assembler* converts these mnemonic codes into the binary machine code. The assembler also assigns and keeps track of memory locations. This allows the programmer to use simple reference numbers—like 10, 15, or 20—to identify his instructions, while the assembler program converts these to actual memory locations, as needed.

With the help of an assembly language, the prospective microcomputer user can write down his instructions, telling the computer exactly what sequences of operations to follow. But having in hand a piece of paper with a written assembly-language program, the user is still faced with the task of getting his program into the microcomputer.

Let us assume that his object is to put the program into semiconductor memory chips containing the random-access memory (RAM) used by the microcomputer. A general series of steps to accomplish this goal are shown in Fig. 1. Programs, depicted as rectangles, include an *Editor*—which controls the entry, correction, and tape-recording of the assembly-language program. At the center of the figure is the *Assembler* program, which converts the assembly language statements into machine language. The *Loader* program reads memory addresses and operation codes from the machine language tape and enters them into the semiconductor random-access memory. After the program, in machine language, has been loaded, the *Debugger* is used to make any corrections necessary to assure that operation is satisfactory.

The tapes shown in Fig. 1 are usually punched paper tapes, but other recording media—such as magnetic tape cassettes and floppy disks, as well as conventional computer cards, tape, and disks—can serve equally well. In some systems, editing and assembly are combined, and there is only one, machine language, tape.



systems is discussed. A step up the computer-size ladder is the one-board minicomputer—the Digital Equipment Corporation PDP-8A, for example, and the General Automation LSI-16, both of which were designed as condensed versions of full-size minicomputers.

The table on pages 80 and 81 displays many of the software resources currently being offered by microcomputer manufacturers. The most important of these to present-day microcomputer users are probably the assembler programs.

The assembler: a basic software tool

Two general types of assembler programs are available for microcomputers: *Cross-assembler* programs run on minicomputers or large computers; *self-assembler* programs run on the microcomputer itself.

Every microprocessor now produced has one or more accompanying cross-assembler program. Often the chip manufacturer writes a cross-assembler even before the microprocessor chips are physically available; this allows programming effort to get under way as soon as the basic microprocessor architecture and instruction list are determined. Using a *simulator* program, a mini- or larger computer can be used to check out and debug many features—but not necessarily all aspects—of assembled microcomputer programs.

Cross-assemblers are often run on time-sharing facilities, and microcomputer manufacturers frequently arrange to make versions of their cross-assemblers available on one, or more, commercial time-sharing services. With a teletype or CRT console, the user can

(Continued on page 82)

Some currently available microcomputer software

Microcomputer Systems	Cross-Assembler	Self-Assembler	Editor
Control Logic L-series modules	Batch version, runs on PDP-8 source tape, $120 (object tapes and documentation also available for all programs)	Compatible with cross-assembler source tape, $120	Source tape, $60
Digital Eqpt- Corp. MPS Series Modules	A paper tape system is used to assemble source code on a PDP-8 and proviee binary output for the MPS processor		Editor is PDP-8 based
Intel MCS-4 MCS-8 MCS-80	Written in ANSI standard Fortran IV; source deck, $1250; now used on many systems, including IBM, CDC, and Univac, Time-sharing versions now up on several commercial systems. Offers macro and conditional assembly capabilities	Versions for MCS-8 and -80 are compatible with the cross-assemblers. MCS-4 version is not compatible. Available only to development system users. No charge	Editors run on MCS-8 and -80. Manipulate strings, search, and substitute. Available only to development system users. No charge
Motorola Semiconductor Products MC6800	Runs on Tymshare system; macro capabilities are in development	None	Source statement text editor runs on GE Tymshare system
National Semiconductor IMP-4 IMP-8 IMP-16	Batch version in ANSI Fortran IV for IBM and other computers. Offers conditional assembly. Source deck, $1250. Similar, noninteractive time-sharing version now up on Tymshare, and GE systems	Available for IMP-8, -16. Similar to cross-assembler. No cost; comes with prototyping system purchase	Source editor for paper tape for IMP-16. No charge; comes with prototyping system
Raytheon RP-16	Batch version in Fortran—for Datacraft 6024. No price policy set yet. Time-sharing version in APL up on APL-plus system	Planned	Uses host-computer editing facilities
RCA Cosmac	Batch version in standard, simple Fortran for IBM machines. Has macros and conditional assembly. More powerful time-sharing version up on Tymshare system. No pricing policy yet	In development	Uses host-computer editing facilities. Editor in development
Rockwell International PPS-4 PPS-8	Available for GE time-sharing, Tymshare, IBM batch, and several other systems. No price set yet	Applied Computer Technology, Inc., provides assembler for PPS-4	None
Signetics 2650	Batch version in Fortran II for IBM, Xerox, other machines. Time-sharing version also	None	Uses host-computer editing faciliteis
Toshiba TLCS-12	Batch version only, in Fortran II	Written in Fortran II	Under development

Loader	Debugger	Simulator	Other Programs
Absolute type source tape, $15	Memory dumps and modification source tape, $30	None	PROM programmer, source tape, $45 User's library offers math and other programs
Binary tape bootstrap loader	Resides in MPS memory, used during application program development	None	Program to load, verify, and modify PROM programs is PDP-8 based. Duplicator program copies and verifies eight-channel paper tapes
Part of system "Monitor" program. Available only to development system users. No charge	Part of system "Monitor" program. For MCS-4 and MCS-8: memory dump and modify. For MCS-80: breakpoints; dump and modify for both registers and memory. Available only to development system users. No charge	Simulators written in Std. Fortran IV for MCS-8 and -80. Debugging uses source program symbols, $750	" Monitor" programs offer elementary operating system with I/O capability. No charge to users PL/M, a higher-level language written in Fortran IV for MCS-8, -80, $1250 A user's library offers many programs. Member fee is charged
—	—	Written in Fortran IV. Available on Tymshare system. Allows timing of calculations, and interactive control of execution	In development
Relocatable linking loader offers memory map and error messages; for IMP-16. Absolute loader PROM; includes bootstrap capability; for IMP-8, -16; no cost with system	Debugger offers snapshots, dumps, breakpoints, memory search, alteration of registers, and memory	None	Subroutines include math, code conversion PROM programmer Teletype I/O, and card reader I/O, in PROM for IMP-8, -16. User's library planned
Absolute loader, no charge to users	In development	None	In development
Absolute loader in hardware	Time-sharing package offers symblolic debugging. Dump and modify for memory in standalong debugger	Time-sharing package offers simulation facility	"Monitor" program in PROM form; others in developmen
None	Debugging comes with cross-assembler facilities	Simulator comes with cross-assembler facilities	Some macros and subroutines No pricing policy yet
Absolute loaders, bootstrap loader	Simulator includes debugging features	In batch and time-sharing versions. Written in Fortran II. No pricing policy yet	About 15 arithmetic and utility routines, including keyboard scanning
Relocatable loader	"Teletypewriter service" program includes some debugging capabilities	Batch-processing version written in Fortran II	Floating-point arithmetic; exponential, trigonometric, and log functions. Higher-level language similar to PL/M is under development

type in his assembly language program, making corrections along the way, as indicated by an interactive editor program. Other cross-assembler versions are written for use with various minicomputers and large computers.

Cross-assemblers are popular because most microcomputers are not configured to handle assembler operations conveniently, while larger computers, equipped with more adequate printers and more memory space, offer the programmer many conveniences.

Like cross-assemblers, self-assemblers are written with a definite computer system in mind. The operation of a self-assembler is highly dependent on the input-output equipment that surrounds the microprocessor. This specific system dependence can sometimes cause problems.

Several features of assemblers are potentially important to microcomputer users. For instance, *relocatable* assemblers allow the memory locations for the machine language program to be transparent to the user. Some assemblers—known as *absolute* assemblers—always start the machine language program storage at the same, fixed memory location; others offer several alternative starting locations and allow some limited linking of program segments in different locations.

Relocatability is a convenience that eases the programmer's task, but it is not an essential feature for many applications.

A *conditional* assembly feature is available with some assembler programs. This allows the user to decide which of the various sections of the program will be assembled and to choose the most efficient order for assembly.

Macro capabilities in an assembler program allow the user to use a single assembly-language instruction to call a specified sequence of machine language instructions. This can be a very powerful tool when certain sequences are repeated during a program. For example, in an instrument operation program, calibration macros can be a great programming time-saver.

Cross-assemblers are generally written in a widely used computer language like Fortran, so that they can be easily adapted to many different time-sharing and batch-processing systems. In general, use of simpler and more standard Fortrans—such as the one specified by the American National Standards Institute (ANSI)—minimizes the problem of getting the assembler to run on a new system.

Programs that edit, load, and debug

Editor programs work together with a teletype, or CRT keyboard, to enable the user to type his assembly language statements on the keyboard, while making any needed changes by brief, typed commands. For example, such commands might be used to add a single character, delete a group of lines, or search for a line containing a certain combination of characters. Editor programs are often an integral part of the larger computer systems used to run microcomputer cross-assemblers.

Loader programs accept machine language code, usually in the form of punched cards or punched paper tape. The loader output may go directly into random-access memory (RAM) or into a device that burns the code into a programmable read-only memory (PROM). Sometimes separate programs are used to convert the machine code for PROM burning.

Some loaders are only capable of handling absolute modules of code, destined for prespecified memory locations. Other, more elaborate loaders can link together various code modules and fit them into available memory space in a flexible manner. Then, if an error is found, only the small number of instructions in a single code module need be rewritten.

Along with this linking and relocation capability, these more sophisticated loaders provide such added tools as memory maps—showing where various programs and program-segments are physically located—as well as appropriate error messages, when a faulty program cannot be properly loaded.

Bootstrap loaders can place a program into memory when the microcomputer system is "empty"—in the sense that it contains no previous program information at all. In some systems, a loader program is made available in PROM memory form. To get the system started, it often includes a bootstrap routine that is activated by hitting a reset button or keying in a single instruction. In addition, the program is used for loading and for displaying memory contents and the contents of microprocessor registers.

Display capabilities are important in program debugging. Debugger programs allow the user to manipulate and observe assembled programs. When a program malfunction occurs, debuggers provide such conveniences as printouts, called "dumps," of register contents, or of selected areas of memory.

Snapshot or breakpoint stops may also be provided. With these, the user can specify the conditions under which he wants to examine memory or registers. For example, he may specify that a breakpoint will occur when a given memory location is accessed, or when a specified code appears in a register.

Debugger programs can also allow the user to change the contents of processor registers and memory locations, to start program execution from any point in the program, and to search memory for the location of specified contents.

Simulating microcomputer operation

Even after a microcomputer program is assembled and debugged, the user does not yet know whether it will truly do the job for which it was written. Most users seem to feel that the only practical way to find out is to wire together the integrated circuit packages, connect them to the system equipment, turn on the power, and see if the program will run properly.

Because of the relatively low cost of microprocessors and other microcomputer equipment, this direct approach usually makes good engineering sense.

In some special situations, it may be worthwhile to simulate the system hardware before it is actually produced. Microprocessor manufacturers, concerned about developing effective system architecture, often find simulation programs easier to manipulate and less expensive to alter than MOS chip designs. Similarly, microcomputer system designers who plan to specify their own custom-made microprocessors find use of simulation programs a necessary design step.

Generally, the more accurate the simulation, the more expensive the simulator program, and the longer

If I only had a benchmark!

With so many different architectures and different program instructions, how can one microcomputer's software power ever be compared to another? One way is to select a meaningful problem; program and run it on different, competing machines; and compare the results.

As yet, few benchmarks for microcomputers are available. The most significant to come to our attention is run by Charles Popper of Bell Telephone Laboratories. His benchmark test uses a standard quicksort algorithm that manipulates a list of values into ascending or descending order. Up to 256 8-bit bytes are sorted using programs that contain the equivalent of about 50 PL/M statements.

The benchmark results found that, with assembly language programs, the RCA Cosmac processor used 181 bytes of memory and the Intel 8080 used 192 bytes, while the Intel 8008 used 347 bytes. Using the PL/M language, the Intel 8008 required 495 bytes.

Even the benchmarking procedure, which sounds eminently fair and equitable, has its drawbacks. The benchmark just cited concentrates on memory operations and character manipulation, but many microprocessor applications are oriented toward input-output and bit manipulation.

Benchmark problems can be chosen so they favor one microcomputer over another, since every machine has its own special strengths and weaknesses. Furthermore, the results depend heavily on the cleverness of the programmers.

The following three examples are not proper benchmarks since they all involve small, simple routines using little code, and can therefore give only a very limited picture of machine performance. We present them as comparison problems that serve to illustrate how very similar results can be obtained with different machines.

Programs were written to implement these problems on the Intel 8080, the Motorola MC6800, and National Semiconductor's IMP-16.

The first comparison problem assumes A and B are positive 8-bit binary numbers. If $A \geq B$, the program is to compute $C = A - B + 2$. If $A < B$, it is to compute $C = B - A + 2$. Random-access memory locations ADDRA, ADDRB, and ADDRC are to contain A, B, and C. The flow chart specified for the solution is shown to the right.

Results for this problem depend on whether $A - B$ is a positive or a negative number. The three machines used from 8 to 15 bytes of memory and from 12 to 39.2 μs to execute the programs.

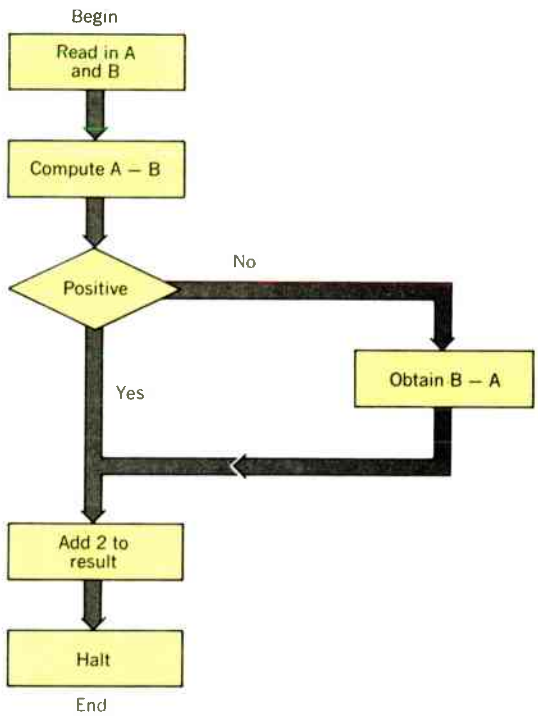
In the second problem, 8 bits of data (b_8 through b_1) are to be entered into one of the microprocessor's registers, and the one-bit furthest to the left is to be located. If b_8 is the one-bit furthest to the left, the integer 8 is to be entered in a second register; if b_7 is the furthest-left one-bit, integer 7 is to be entered, etc. If b_8 through b_1 are all zeros, the second register should be left with zero.

Solutions for this problem used from 10 to 14 bytes of memory. Execution times varied, depending on the nature of the data, with minimum times ranging from 18.5 μs to 36.4 μs.

The third problem involves a list of consecutive data entries stored in random-access memory. The address of the first list entry in memory is denoted ALIST. A second memory address denoted ENTRY contains a number n—between zero and 255—that signifies the location, in the list, of a desired entry. The entry is to be obtained and added to the microprocessor accumulator.

Memory space used for this problem varied from 6 to 13 bytes, with execution times running from 13 to 34 μs.

Comparison arithmetic problem.



it takes that program to run. Near the point of diminishing returns, the engineer must decide whether he is better off checking his programs on actual hardware, or trying to get more refined simulation.

Simulation of input-output (I/O) operations is particularly difficult. For example, the actual time taken by the processor for any given I/O computation is significant, because peripheral devices—like a tape reader or a disk—require data transfers within strict time limitations if they are to operate efficiently. To simulate these I/O operations, the program must keep track of simulated "real time," and this is difficult and costly to program.

Design control of overall aspects of microcomputer system accuracy can be nicely handled by simulation techniques. Error budgeting is, for example, a potentially spiny problem that is readily handled by simulation. In a given system, the required output accuracy can usually be attained by using more accurate sensors, or more accurate computation, or more accurate A/D conversion, etc. Proper error budgeting finds the mix of component accuracies that will produce the required overall system accuracy at lowest cost.

Microcomputer users generally have to contend with fixed-point arithmetic and 4- or 8-bit words. That is, the program must specify the location of the decimal point in each set of calculation numbers. Floating-point arithmetic moves these decimal points automatically, but this facility is not yet available for most microcomputers. A simulation program known as a fixed-point scaler can help considerably with this decimal point location problem. The output of the program is a matrix that indicates—for each set of computation numbers—the dynamic range of the numbers during the computations, and where the decimal points should be located.

Programming at higher levels

With a higher-level language, the user issues a relatively small number of quite general commands—Fortran statements are of this type—and the microcomputer translates these commands into specific machine code steps, hopefully producing the desired results. This translation process is carried out by a special program called a compiler.

In fact, there is only one higher-level language now available to microcomputer users—the Intel PL/M language.

Tests on sample programs are said to indicate that a PL/M program can be written in less than 10 percent of the time it takes to write the same program in assembly language. The main reason for this savings in time is the fact that PL/M allows the programmer to define his problem in terms natural to him. For a program that selects the largest of two numbers, the PL/M programmer need only write: If $A > B$, then $C = A$; else $C = B$.

But to many hardware designers the notion of higher-level languages seems misplaced and distorted. As one engineer put it, "... languages like PL/M have only a marginal value. It is not really difficult to program microcomputers in assembly language. Using PL/M necessarily means supporting a time-sharing terminal, which may be a substantial expense for many small groups and firms." Other users seem to have little confidence that a compiler can produce machine code that does an efficient enough job of bit manipulation to save memory space or speed computation.

Most of the applications software now written for microcomputers is quite naturally being done by users, rather than manufacturers. Some fairly standard routines—like those for scanning a keyboard—are being offered by the manufacturers, mainly as sales incentives to potential customers. Intel (see Box below, left) has organized a cooperative library for user programs.

Users complain that computation on microcomputers is hampered by a lack of mathematical utility routines. Since requirements of different users for such routines vary widely, some microcomputer manufacturers—for example, Signetics—are working on libraries of arithmetic utility routines, such as multiples, variable length multiples, divides, and multiple precision arithmetic. These routines are each being written in several different versions. Some are for maximum speed of execution, others for compactness, so they can be stored in very limited memory space.

Careful records are important

Hardware-oriented engineers tend to discount the importance of careful software documentation. Their first impulse is often to use as little energy as possible to assure that their microcomputer programs will operate correctly. In the debugging stage, this generally means patching a programmable read-only memory to make it do the job.

As Dick Lee, of Boonton Electronics, puts it: "When the original programmer is gone, leaving behind nothing but a program listing, somebody has to sit down and conceptally recreate the program from the listing. That is a difficult, time-consuming job. Until he actually builds up a flow chart, he can't be sure that when he tries to modify the program, he won't introduce some logical fault. Such faults may be subtle and not show up until the system is out in the field. Then, bingo!"

Many users feel that a printed program listing provides an adequate record that can be handled like any other engineering drawing, with revisions and change notices. In truth, only the person who wrote the listing knows the reasoning behind the program, and he may easily forget. To understand a program well enough to make meaningful changes, a programmer needs a flow chart, and a written description of the program strategy can be a great help, as can line-by-line comments on assembly language programs.

The first microcomputer user's library

Users' program libraries have been a familiar part of the computer scene since the SHARE organization began to collect and make available programs written by IBM employees and customers.

Starting early this year, the first microcomputer user's program library was organized by Intel Corporation. The library is divided into three sections, corresponding to use of the three principal Intel microcomputers: the MCS-4, MCS-8, and MCS-80.

Membership in each of these three sections is available "to any interested person or organization" for a yearly fee of $100 per section. The fee will be waived for users who submit a program to the library.

Documentation for each library program includes function, required hardware and software, details of user-program interaction, and a listing of the program.

Among the programs now available through the library for the MCS-4 machines are: AND, OR, and XOR subroutines; an 8-bit multiply, 8-bit divide, decimal addition and subtraction; Chebyshev approximation; 64-bit arithmetic; elementary functions including sin, cos, tan, e^x, and log; conversion of binary code to and from binary-coded-decimal; and teletype read and punch routines. For the MCS-8 machine, there are programs for binary search, floating-point arithmetic, floating-point input-output conversion, processor state restoration in interrupts, 8- and 16-bit multiply and divide, and teletype read and punch. All these MCS-8 programs will also be available for the MCS-80 machine.

A similar library is being planned by National Semiconductor Corp. for users of their IMP-4, -8, and -16 microprocessors.

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Competing display technologies struggle for superiority

A comparison of display media, including light emitters and controllers and CRTs, reveals which are best for what

Competition among established and evolving display technologies is becoming ever more fierce as pressures mount to reduce display costs and bulk. And the increasing use of displays to interface humans and computers—displays that also emphasize digital address, linearity, and intrinsic memory, as well as low bulk —adds strong impetus for the technological refinement of large-display designs. In fact, unless the newer, easily integrated planar techniques can be improved beyond the present state of the art, both technically and economically, the inevitable result may be that displays will be the bulkiest and costliest components of terminal electronic apparatus.

A comparison of display media

The advantages, disadvantages, and suitable application areas for the leading types of active and passive displays are summarized in Table I. The table includes both light emitters and light controllers (light valves), and beam-addressed and matrix-addressed displays. It is clear from Table I that no single type of display is a panacea.

In small-display applications—calculators and digital instrument readouts, for example—evolving display technologies such as liquid crystals and light-emitting diodes have made impressive inroads.

The large-display battlefield is more one-sided. The CRT is hard to beat for large displays. A look at its advantages in Table I indicates why this is so. The CRT's main disadvantage, however, is bulk, a characteristic that may become even more of a disadvantage as advances in silicon integrated circuits reduce the bulk (as well as cost and power consumption) of the digital, and much of the analog, circuitry that is used with displays.

In large displays, the CRT also has the advantage over many of the newer display media of beam addressability. Beam addressing, in general, uses either electron or optical beams, with suitable scanning and modulating techniques, to make spot sequential contact with individual display elements. Beam addressing works well, as in a CRT, when the display medium responds rapidly to brief excitations without saturating, requires no threshold, and may use linear responsive elements. Beam addressing is not suitable, however, for matrix displays that require a threshold voltage (the firing voltage at which a picture element changes state) and/or a strongly nonlinear response characteristic in order to allow electrical isolation of discrete picture elements.

Ronald K. Jurgen Managing Editor

A need for matrix addressing

If beam addressing cannot be used, then separate connections can be made to each of the picture elements in a low-resolution display in order to address it. But with medium- and high-resolution displays (more than 10 000 picture elements), the separate connection approach becomes uneconomical and cumbersome. Matrix addressing of some sort then becomes almost mandatory.

Matrix addressing uses two or more arrays of conductors, mutually orthogonal, arranged in a row and column fashion. In one form of matrix addressing, known as coincident selection, any one display element is excited by activating the row and column corresponding to that element. This technique requires the existence of a threshold in the display medium. The needed number of interconnections to the display is reduced by this technique but, even so, connecting one transistor driver to each X and Y line or conductor is impractical for large displays.

In large displays, conductors can be divided into groups. For example, the X axis and Y axis can each be divided into 32 groups in two ways for a total of 64 groups per axis for a 1024×1024 conductor matrix with as many as 1 000 000 picture elements. One driver is then associated with each group rather than with each element so that the total number of drivers is reduced drastically. And further reductions in needed drivers are possible through other logical and combinatorial multiplexing schemes.

Matrix addressing has proved to be the best approach to flat-panel, or planar, direct-view displays. It permits relaxing of requirements for both high peak brightness and high-speed spot addressing by combining storage with line-at-a-time excitation. Storage may be intrinsic to the medium itself, or may be provided in the addressing matrix, or both.

Matrix techniques can run into cost-complexity disadvantages and are not easily applicable to all non-beam-addressable display technologies. High drive-power requirements for large gas-discharge displays, for example, can be challenging, particularly when highly sophisticated multiplexing schemes are used requiring extremely precise discrimination among picture elements. And matrix addressing of LEDs for large displays requires lowered duty cycles which, in turn, decrease LED brightness. Technological progress in both solid-state displays and in inte-

grated circuits, however, is showing promise for solving these, and other, basic matrix-addressing problems.

New LEDs with internal storage

Large displays using LEDs cannot be justified economically at the present time. The semiconductor material (and its processing) that would be needed for such displays is costly. Even if these costs could be reduced considerably, the large number of data points that would have to be addressed (seven data points—one for each segment of a seven-segment digit, for example) would still be formidable. Since multiplexing of an LED display is limited, because of the duty-cycle problem already mentioned, to about 200 multiplexed points with presently available device efficiencies, other addressing techniques have been tried. For example, a logical memory external to the LED can be provided for each data point.

A better, and possibly more economical, solution is to incorporate the memory function into the LED itself. Two new LEDs under development do precisely that. They have bistable mechanisms that provide a means for internal storage. Reduced drive currents are also

I. A comparison of advantages and disadvantages of leading types of active and passive displays

Type of Display	Advantages	Disadvantages	Applications
CRT	Bright, efficient, uniform, all colors, gray scale, functional scanning, low cost, reliability can be high (>20 000 hours), intrinsic, memory is possible at expense of gray-scale capability	Bulk*, high voltage, memory is needed for gray scale or interactive graphics†, nondigital address* flicker, jitter	Large displays, small- and large-group viewing, console, projection
Scanned laser	High resolution uniformity, functional scanning, good contrast, color	Low power efficiency, costly overall system bulk, low brightness	Large and high-resolution displays, small- and large-group viewing, projection and virtual image
DC gas discharge	Bright (if display resolution is limited), range of colors, gray scale, functional scanning, low cost per element, potential for long life	High drive power, line memory required, limited number of scanning lines ($\lesssim$250)	Indicators, small and medium displays, small-group viewing, flat panel
AC gas discharge	Bright, range of colors, inherent memory, threshold for switching, low cost per element, potential for long life, selective erase	No gray scale, questionable compatibility with IC technology, relatively high drive power, expensive overall display system	Indicators; small, medium, and large displays; small- and large-group viewing, flat panel
LED	Bright; red, yellow, and green; IC compatibility; small size; reliability (>10^6 hours)	Cost per element is fundamentally high and proportional to area, low power efficiency	Indicators and small displays, individual viewing, flat-panel and virtual image
Electroluminescent	Cost per element can be low, gray scale, various colors, high brightness	No internal memory, weak to modest thresholds, not compatible with ICs, lack of uniformity, uncertain reliability	Small and medium displays; individual and small- and large-group viewing; flat panel
Electrochemiluminescent	Good brightness and contrast, wide-angle viewability, sharp threshold, IC compatible, some gray scale, red and green, potential low cost, rapid address	Power for auxiliary illumination (ultraviolet), uniformity in large panels, reliability of only 2000 hours, long recovery time (seconds)	Indicators; small, medium, and large displays; individual and small-group viewing, flat panel
Field-effect liquid crystal	Good contrast in bright ambient, low power, IC compatible, low cost per element, some with intrinsic storage, uniform	Limited temperature range (—10 to +75°C), reliability not established, may require memory (one memory element per picture element), low switching speeds (tradeoff in drive power versus speed), restricted viewing angle	Small, medium, and large displays; individual and group viewing; flat panel
Electrophoretic	Good contrast in bright ambient, low power, possibly IC compatible, expected low cost per element, uniformity, intrinsic memory, range of colors, wide-angle viewability	Low switching speeds (tradeoff in drive power versus speed), no gray scale, weak threshold, stability and reliability unknown	Indicators; small, medium, and large displays; individual and small-group viewing; flat panel
Erasable light-addressed light valves	High resolution, uniform, gray scale, overall low cost per element, inherent memory, functional scanning	May be slow, useful only for relatively fixed displays, bulky total display system, require special optical systems	Large and high-resolution displays, small and large-group viewing, projection and virtual image

*Flat-panel CRTs are being developed, but not all problems are solved.
†External frame memory has become relatively inexpensive and of high quality. Selective erase is possible.

For the analog fan, all is not lost

So much attention is being paid these days to digital displays, whether they are for instruments, watches, or large control panels, that those who prefer analog displays may have good reason to feel they are members of a new minority group. But there is some indication that new analog displays are being developed with techniques intended originally for digital applications.

Simpson Electric Company of Elgin, Ill., for example, recently announced a solid-state electric indicating meter. It has no moving parts and the electric signal is displayed by a linear array of light-emitting diodes. All the LEDs physically situated below the signal level are "on," so that the appearance of the display is somewhat like a wall thermometer.

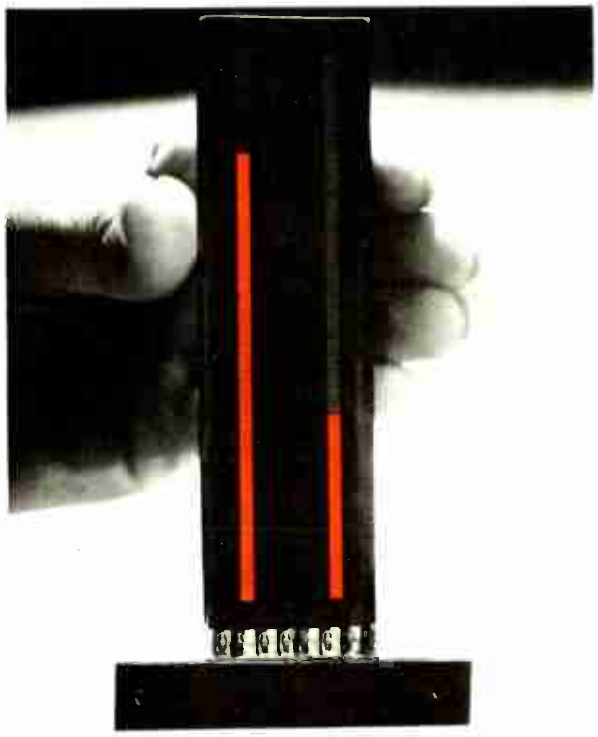
Known as the ANA/LED Indicator, the new meter is intended for use as a panel meter. It is self-contained in that it accepts an analog electric signal typical of any D'Arsonval electric meter and, by means of its internal conversion circuits, produces a proportional display of the signal level. The meter requires an external power supply of about 2.4 watts to power the LEDs and provide minimal power for other circuit requirements. Therefore, the meter does not replace the conventional D'Arsonval meter but, rather, provides an alternative in areas where certain characteristics of the moving-coil instrument are undesirable or even intolerable. Its main advantage is that it is a trend indicator with both a zero and a full-scale value as contrasted with a digital panel meter, which does display absolute terms but is a poor trend indicator. The digital meter's flickering numbers can be irritating to some observers and it does not define full scale readily.

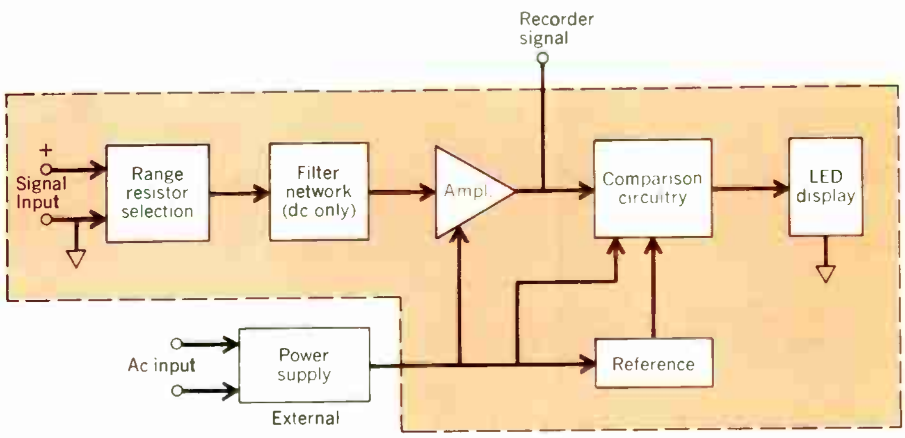
The Simpson meter is shown in Fig. 1 and its block diagram in Fig. 2. The input signal is subdivided by a range resistor network, filtered in the case of dc, and is then amplified with a gain of 100 to provide a 0- to 5-volt signal. This signal provides the input to the comparison circuitry and also to an external pin connection for recorder inputs. Each LED is turned on when the amplified signal equals or

[1] Simpson Electric's new ANA/LED indicator (left) has a direct-reading linear LED scale. Response is virtually instantaneous with no overshoot.

[2] Circuit for the ANA/LED indicator (below) incorporates a sample ladder resistor network and op amps.

[3] Burroughs' bar graphs display (right) is a gas-discharge device that needs only six active drivers for both bar graphs.





becomes higher than its reference voltage. The power supply is external to the ANA/LED package.

The meter contains 53 LEDs—50 for scale graduation, one for overrange, one for reverse polarity, and one to indicate zero.

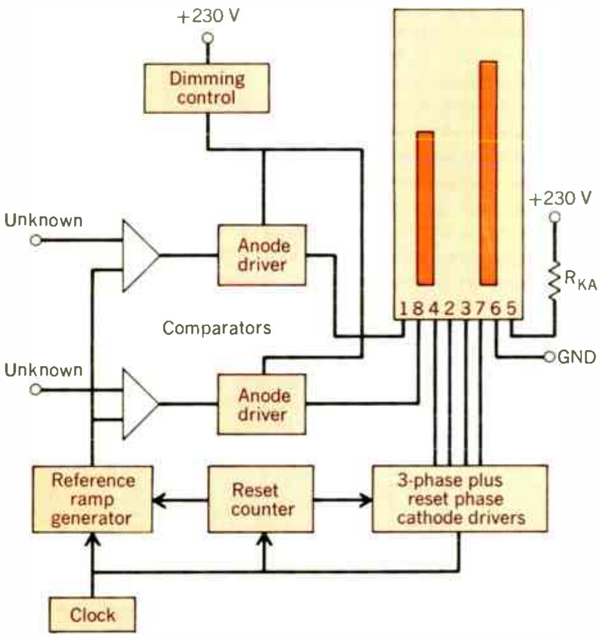
Another manufacturer, Burroughs Corporation, of Plainfield, N.J., announced recently an analog display for instruments in the form of a bar graph. The flat panel indicator, shown in Fig. 3, is actually two separate bar graphs, each containing 100 elements. It is based on the Burroughs Self-Scan plasma panel. The display needs only six active drivers to operate the two independent information channels. A typical drive circuit is shown in Fig. 4.

The display elements of both bar graphs are bussed together in a three-phase arrangement. Operating in a scanning mode and refreshed at 70 Hz or greater the panel presents a flicker-free display to the viewer.

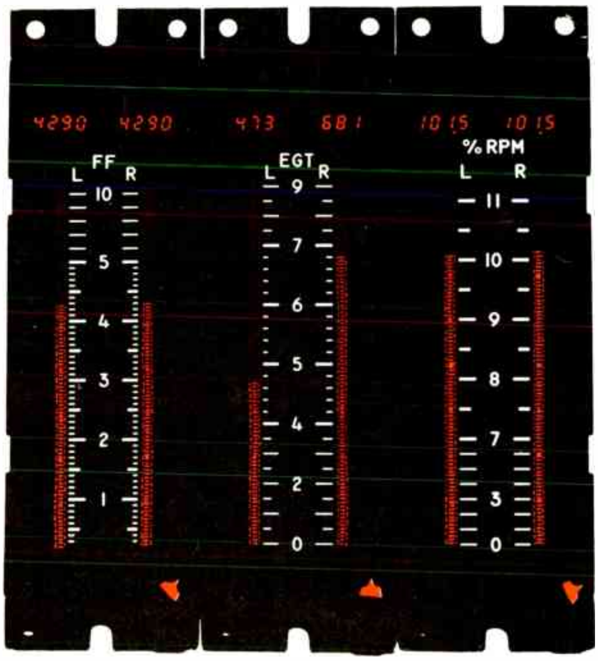
Suitable logic external to the display device is used to generate a reset pulse and 100 clock pulses in a three-phase sequence (Fig. 4). The display anodes are switched on at reset time and are switched off at the appropriate clock count, thus determining the height of the bar. Switching is usually accomplished by comparing an unknown signal with a reference voltage ramp.

Another vertical scale type of instrument using LEDs was first reported in *IEEE Spectrum* in November of 1972 (pp. 21–22). It was developed by General Electric Company for application in aircraft instruments. A major challenge was the need to obtain readable light levels for the LEDs when the ambient illumination could reach 10 000 footcandles. Three solid-state instruments that were developed are shown in Fig. 5. They display rate of fuel flow in pounds per hour, exhaust gas temperature in °C, and fan speed as percent of rated full-scale r/min.

Figure 6 shows a block diagram of the fan speed system.[1] The input is an ac signal with a frequency that is proportional to fan speed and is 100 percent of full scale at 70 Hz. The input circuitry attenuates 400-Hz noise and doubles the frequency. A phase detector drives the variable control oscillator (VCO) that operates at 8400 Hz (120 times input frequency) when the input is at full scale. Crystal-controlled oscillators and logic circuits give precise tim-

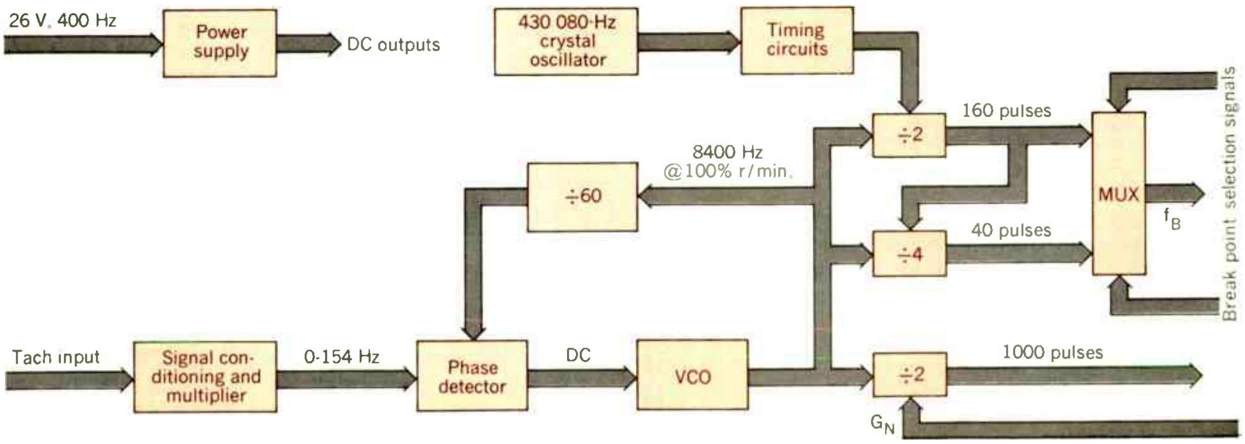


[4] A typical drive circuit for the Burroughs' display has the components shown.



[5] Three solid-state vertical scale instruments are combined in GE's LED display for aircraft applications.

[6] A block diagram of the circuitry used for signal conditioning for one of the three displays: fan speed.



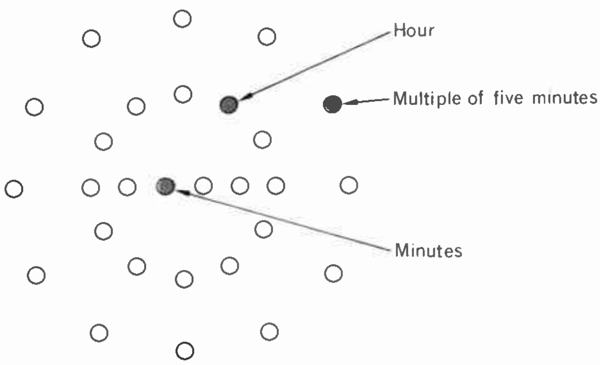
ing used for generating numeric and bar graph pulse trains. At full scale, the 8400-Hz output is gated by a 0.238-second signal and divided by 2, thus resulting in a numerical pulse train of 1000 pulses.

Generation of the bar graph pulse train is complicated by the fact that the scale is nonlinear with a four-fold expansion from 70 to 110 percent to increase readability in the region where engine performance is most often monitored. Two sets of pulses are used. One pulse train of 160 pulses comes from using a gate of 0.038 second on the 8400-Hz signal and dividing by 2. Further division by 4 results in a pulse train of 40 pulses. Breakpoint selection signals are sent from the control and driving electronics to choose the appropriate train. The first 28 pulses correspond to the 28 LED bar segments from 0 to 70 percent and are obtained from the train of 40 pulses. Above 70 percent, to 110 percent, the other pulse train is selected to achieve a change in scale.

To obtain maximum brightness of the displays, several techniques were used. Since brightness level of gallium arsenide phosphide LEDs has a negative temperature coefficient of about 1 percent per °C, maximum use of complementary metal oxide semiconductor (CMOS) circuitry was made to keep power dissipation low. The discrete driver LED interface was optimized. And pulse enhancement was used to obtain maximum brightness from the LEDs.

These few examples are illustrative of what may or may not be a trend in new displays—going analog where desirable, but with modern techniques. As a case in point, at the time of this writing, Seiko Time Corporation has just announced that it will concentrate on producing quartz-crystal *analog* wristwatches with conventional hands. The company will also produce digital wristwatches but feels that the digital market is basically a limited one that will level off at some future date at a relatively low percentage level of the total wristwatch market.

A hybrid approach to analog displays for watches in which the digital-to-analog conversion is based on logic in the human head is shown in Fig. 7. Suggested by E. I. Gordon of Bell Laboratories, the watch display would have an outer circle with a single indicator (e.g., an LED) for multiples of five minutes, an inner circle for the hour, and a row of four for the minutes. Only three LEDs (or liquid-crystal elements, etc.) need be on at any one instant. In the example shown, the time is 12 minutes after one o'clock.



[7] **Hybrid watch display could use LEDs, liquid-crystal elements, or other display means.**

REFERENCE

1. Skovholt, R. L., "Solid state vertical scale instruments," *Proc. of the SID*, vol. 15, first quarter 1974, pp. 33–40.

One man's solution to the paper shortage

The inevitable result of the ever-increasing deluge of printed information and the ever-decreasing supply of raw materials may be that the use of paper will become economically prohibitive and ecologically despicable. This is the provocative opinion of Robert V. Pole of IBM Research Laboratory, San Jose, Calif. In a lecture presented at a University of California, Berkeley, seminar held in conjunction with the 1974 Society for Information Display International Symposium in May of this year, he said that the only escape from the paper dilemma is to relegate the paper-bound mode of information dissemination to nonpaper displays—displays that would replace books, journals, memos, and letters.

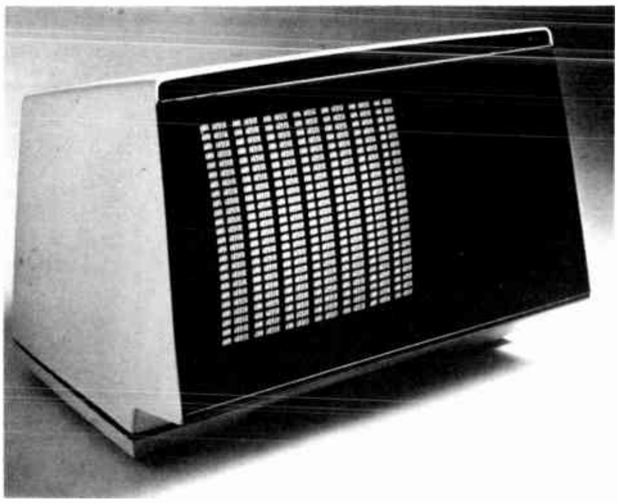
A quality replacement for the printed page, in Dr. Pole's view, would need a resolution of at least 250 lines/inch (10 lines/mm) which, for the size of a standard letter, would necessitate displaying about 6 million resolvable spots—and preferably more. The display would also need to modulate, or selectively absorb, ambient light in a manner similar to the way a printed page does. Other desirable features would be erasability, storage (at least temporary), interactive capability, and portability of the screen (reusable soft copy). The display would not need to be fast, would require no motion, and could have moderate life (if inexpensive enough).

The only way to realize a display meeting all of these requirements, according to Dr. Pole, is to address a light-sensitive screen optically—that is, a light screen that has some source of its own gain. The obvious display, a CRT, would not be capable of 6 to 10 million spots per field with reasonable life and cost. A laser-addressed display, however, would be more viable. And, Dr. Pole says, at present there is only one acceptable laser that operates continuously, delivers reasonable power, and operates outside the visible spectrum so that ambient light would not affect the display screen—the helium-cadmium laser. It is basically a low-power unit operating at two wavelengths, 325 and 443 nm, and capable of several milliwatts of cw power in reasonable size. However, its cost is still too high (one to several thousand dollars retail).

A laser display system of this type would require a high-resolution deflector, a modulator, and the previously mentioned light-sensitive screen with storage and gain. Suitable deflectors (mechanical) and modulators are already available. What is most needed is the screen with gain. Research toward that goal is underway and, if successful, in Dr. Pole's words, "an exciting new display technology may be in the offing."

possible for refresh operation to produce a flicker-free output with adequate brightness. And the new units are optically sensitive enough to permit a light pen to be used for writing in or reading out stored information.

One of the new LEDs is called a Thyropter. Under development by Ferranti Ltd., the gallium phosphide LED operates, according to research workers at Ferranti, by optical feedback between a diffused p-n junction and a high-resistivity region grown into the epitaxial layer. In operation, the resistivity of the layer is such that only a small current can flow



Read-only CRT terminal from Ann Arbor Terminals, Inc. is a low-cost, multicharacter display that handles data rates up to 1620 characters per second.

This report is based freely on information presented at the 1974 International Symposium of the Society for Information Display held in San Diego, Calif., May 21–23, and on a symposium on information display techniques held by the University of California, Berkeley, in conjunction with the S.I.D. meeting.

The writer, is particularly indebted to the following participants in those meetings: J. B. Flannery, David A. Hodges, D. E. Liddle, and Robert V. Pole.

Table I is D. E. Liddle's and J. B. Flannery's version of several tables that appeared in the article, "New display technologies—an editorial viewpoint," by E. I. Gordon and L. K. Anderson in the July 1973 issue of *Proceedings of the IEEE*. The section of this report entitled, "The impact of LSI technology," represents the thinking of David A. Hodges.

through the device at low voltages. As the voltage is increased, a point is reached when enough current is flowing to produce light from the diffused p-n junction. This light affects the barrier at the interface between the high-resistivity and epitaxial layers, causing more current to flow and resulting in a negative-resistance characteristic. Typical turn-on currents are of the order of 1 mA at 8–11 volts with hold-on voltages of 2–4 volts. Workers at GE Electronics Lab, however, suggest that current filament conduction is responsible for the device operation.

For a Thyropter display, the individual LEDs are connected in an X–Y matrix. For normal operation, the diodes are all forward biased with about 7 volts dc. They are addressed by turn-on and turn-off pulses of ±5 volts. Because of the mechanism of operation, the LEDs are affected by external illumination, but this is not a problem in normal light ambients if contrast enhancement filters are used. This same sensitivity to light, however, does mean that a light pen can be used to switch an LED into the "on" state. The data read in can then be read out electrically, as well as being used to display an image.

The second new LED development, at Sharp Corporation, takes advantage of the fact that a four-layer, p-n-p-n junction LED can be processed so that it has a negative-resistance characteristic. The concept has been incorporated into a dual-color LED lamp. A gallium-arsenide infrared LED, the surface of which is deposited with phosphorus material to convert the infrared to visible green, is mounted in the same package with a gallium aluminum arsenide LED of visible red.

A light pen equipped with two visible LEDs on its end can be used with the Sharp display to select either the red or the green color in any one picture element on the display panel. A 14- × 15-element array using the dual-color LEDs has been constructed experimentally.

The impact of LSI technology

Progress in silicon integrated circuits has brought rapidly decreasing costs per unit functional capability. And monolithic integrated circuits are entering application areas such as imaging, data storage, and A/D conversion. The following are some of the new developments that are significant ones for the display field.

In semiconductor memories—which can be used in display systems in refresh stores, data transmission buffers, and scan converters—random-access MOS memory components of 4096-bit capacity are already available and volume prices may be only 0.1 cent per bit within the next 2–3 years. Using 4k-bit components, a display refresh store for 40 lines, 80 characters per line, requires only eight IC components, and consumes about 2 watts of power.

LSI microprocessors are making possible program-controlled information processing on character data at rates in the range of 10 000 to 100 000 characters per second with presently available 8-bit microprocessors.

Monolithic A/D converters, as might be used for converting analog information into digital display, of 8–12 bits accuracy and 1-μs to 1-ms sample conversion times may become available in the near future at a cost of $1 to $20 in volume.

Present-day, gas-discharge panels require 50- to 200-volt drive signals. Discrete component circuits have been used for drive functions because integrated circuits with this capability are not readily available. But the IC capability exists via high-voltage diode ICs, dielectric isolation techniques, and/or double-diffused MOS transitor techniques.

Displays of the future

Although new display technologies will be forthcoming in the years ahead, it is not likely that any new display medium will be the best answer for all applications. What does look more probable than it has at any time in the past is that large-area, flat-panel displays will be developed, with the considerable help of integrated circuits and/or display media with self-storage. But they still have a long way to go before they can be justified economically.

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Consumer protection with teeth

A year old and fully staffed, the U.S. Consumer Product Safety Commission has become a watchdog with a bite

Take a 35-year-old assistant professor of electrical engineering, add intense personal interest in consumer protection, and then supply him funding through the National Science Foundation for research on effective methods, materials, and media for upgrading consumers' technical sophistication.

Next create a powerful Government agency concerned with product safety and sorely in need of experienced commissioners to handle uncharted responsibilities and sensitive situations. Finally, heat everything in a broth of corporate unrest concerning private product-related litigation that has increased dramatically over the last decade.

Such experience, needs, and pressures are very real, and they combined to make R. David Pittle the fifth of five commissioners on the Consumer Product Safety Commission (CPSC) October 10, 1973. His consumer-oriented commitments before nomination included not only the NSF-funded research at Pittsburgh's Carnegie-Mellon University, but also the presidency of a local volunteer group, the Alliance for Consumer Protection. Aware of the Alliance and the activist role played by Dr. Pittle, Ralph Nader recently described him as "the only engineer in the U.S. who 'picketed' for the consumer."

Returning to Newark College of Engineering for the fifth annual Product Liability Prevention Conference—this time as keynote speaker—Commissioner Pittle was careful to mention tasks unfinished and roads not (yet) taken, but it was obvious that the CPSC has come a long way in its first 15 months of operation.

A foundling enterprise last summer, not yet fully staffed or organized, the CPSC is now an effective Government agency, which can ask for—and get—prime television time to bring hazardous products to the public's attention. Through the same medium, the Commission is also promoting a toll-free telephone "hot line" (800-638-2666) for consumers wishing to report product-related problems or suspected dangers.

Calls are taken by special operators during normal business hours. When they are off duty, a taping system records all incoming messages.

I. A product banned

The full weight of the Commission came down recently on one item indigenous to nearly every auto repair shop and the garages of many weekend mechanics: a rubberized, plastic-sheathed trouble light (with extension cord) that can be hung from hood or chassis to illuminate dingy work spaces.

A soft plastic forms the barrier between bare hands and bare metal, but this insulation can be easily pushed aside, leaving live portions of the underlying receptacle exposed. Compounding the hazard is a lack of brand information on the offending light.

The manufacturer was finally identified as A.K. Electric, Brooklyn, N.Y., and a nationwide alert was issued over television and radio at the end of August. An official court-sanctioned ban followed a few days later.

Another common appliance, color television, has also come under the Commission's watchful eye. Starting with a simple request, which generated little of the needed data, the CPSC has now subpoenaed all manufacturers making or selling color TVs in the U.S. for accident information relating to fire and shock hazards. The Commission is expected to make its full intentions in this area known through the Federal Register sometime this month, and will probably have selected a team to develop formal color TV standards by December.

Not all the actions thus far undertaken by the CPSC are so obviously beneficial, or even welcomed by the public the Commission is pledged to protect. Bicycles now outsell automobiles in the U.S., and on July 1, 1974, the CPSC announced mandatory safety regulations for bicycles introduced into interstate commerce on or after January 1, 1975.

II. The number one hazard

Although the CPSC has accumulated evidence placing the bicycle as number one on its product hazard index, many bicycle enthusiasts fear that the new standards will effectively ban light, ten-speed bikes or make them so costly that few could afford them. Commissioner Pittle, however, believes that the new rulings will stand as an example of the way Government safety standards substantially reduce injuries at minimal cost or inconvenience to industry and consumers. He claims a CPSC staff analysis shows that the standards will, at most, add only a few ounces and a few dollars to complying bikes while reducing injuries by tens of thousands. Of course, automobile seat belt interlocks, promoted and mandated by the National Highway Traffic Safety Administration, in much the same manner, are now about as popular with motorists as straitjackets are with mental patients.

Lightweight bikes are definitely providing transportation, recreation, and at least some immediate relief from the energy crisis for a growing army of devotees. Any regulation that even hints at turning the sleek racers into balloon-tired "newsboy specials" is probably in for some very rough going.

III. Prevention vs. litigation

These examples of recent CPSC activities underline the Commission's orientation toward *prevention* of injury rather than compensation of the injured. Commissioner Pittle endorses the Commission's role in this respect and provides a carefully reasoned personal theory to explain why little faith has been attached to private product liability litigation for preventing consumer product accidents.

Addressing the conference, Commissioner Pittle explained that "product liability is a post-injury mechanism. It is not triggered until someone is injured, and in most cases will not serve a preventive function unless *many* persons have filed lawsuits." Delays attributed to this process were termed "understandable but intolerable." And Commissioner Pittle acknowledges that "in certain instances, manufacturers may find it less costly to pay damages than to produce safer products."

Another unwelcome characteristic of product liability litigation is its lopsided impact on industry. Since companies cannot predict the extent of product-related injury or the number of successful lawsuits, Commissioner Pittle expects that "they may well gamble by producing products that, although inexpensive, pose high degrees of hazard."

An emotion-filled courtroom is, of course, not the ideal platform for a reasoned and dispassionate analysis of the risks associated with a particular product. "Lawsuits will continue to be win-lose propositions," claims Commissioner Pittle, "dealing mainly with the interaction of one person with one product at one point in time. Parties to a lawsuit are concerned with the particular factual nuances of their case and not with the more general aspects of risk associated with the product at issue. There is no systematic follow-up to determine whether the defect which caused the plaintiff's (consumer's) injury has been corrected."

IV. Protection or paternalism?

But there are critics who see the CPSC as either a threat to the status quo, or a misguided (though perhaps well-intentioned) "mother hen" that will end up costing consumers dearly for any protection it may afford. Rudolph Janata, an attorney with Wright, Harlar, Morris and Arnold, remarked during a conference panel discussion that "our adversary-jury system of determining tort liability rests upon a principle that is basic to human nature and morally inescapable—that one who causes injury to another should fairly and adequately compensate him for that injury. This is a principle which carries built-in protections for plaintiff and defendant alike."

Seeking to counter "despair" and "a defeatist mentality" among defense lawyers and manufacturers, Mr. Janata's comments were not totally unexpected. Far more illuminating were the remarks of conference speaker Margaret Dana, newspaper columnist and long-time consultant on consumer attitudes. She is keenly aware, from readership feedback, that consumers are particularly anxious about the cost of safe products and potential curtailment of acceptable options in the marketplace. Ms. Dana concludes, "Already there is some resentment toward the preemption of consumers' right to *choose* what level of performance they want, when any regulatory body issues a mandate before taking the time to find out how consumers feel about it."

V. Setting standards

Actually, if the CPSC functions as Commissioner Pittle describes it, the public has and should continue to have a very strong influence on any final list of product specifications. Since the Commission is generally prohibited from drafting safety standards by itself, it must publicly invite interested persons outside the Commission to develop a proposed consumer product safety standard.

Regulations require such "offerors" to indicate clearly how they will involve consumers in the development of a safety standard. Offerors must also demonstrate technical competence and a willingness to comply with the Commission's conditions for standards development.

Through various appeals, a pool of about 2000 volunteers has been identified by the Commission, thus providing offerors with a source of willing helpers who have no economic stake in influencing the final standards. These potential contributors are largely consultants, faculty, housewives, and members of public interest lawfirms. Some cash is available to help offset an offeror's costs should his proposal (offer) be accepted. But this apparent generosity has proved a real stickler.

Implementation of the offeror concept has not been totally successful thus far. Commissioner Pittle admitted that the first CPSC negotiations for an architectural glass standard broke down when joint offerors—the National Consumers League and the American Society for Testing and Materials—insisted on a provision guaranteeing funds for the salaries of technical consumer representatives who might spend substantial time away from their normal employment.

Technicalities have also been responsible for some recent unfavorable headlines about how the Commission "capitulated" to industry objections to a proposed 1974 ban on fireworks. Actually, Commissioner Pittle explains, "After publication of a regulation, persons adversely affected have 30 days to file objections. If objections are filed and raise sufficient matters of fact or law, a hearing *must* be set at which evidence can be presented and a decision reached." The fireworks ban has been postponed—presumably due to normal administrative procedures—but once these hearings are over the ban could still go into effect by next July 4.

But even assuming a flawless effort by the CPSC, manufacturers will still face gloomy and disappointed consumers as part of the normal business day. Some insight into this matter was provided by a specialist serving one of the United States' biggest retail operations: Sears Roebuck, Inc.

VI. A moving target

As quality assurance engineering department manager for Sears, Robert W. Peach proposed to a conference general session that at least some consumer gripes are traceable to rising expectations in a fast-moving marketplace. To illustrate, he asked his audience to consider the significance of a complaint against mechanical adding machines—that they are "noisy and slow"—at two points in time: five years ago, and today when they must compete with solid-state pocket calculators. Where once there may have been genuine concern for defects or lubrication problems, perhaps there remains only the frustrated recognition that something much better and cheaper is now available.

In another session dealing with appliance quality, Robert H. Meyerhans, vice president and director of corporate product safety and reliability for the Fedders Corporation, acknowledged that few consumers appreciate the meaning of reliability as it applies to a given appliance type. Although significant differences can exist between competing brands, top- and bottom-line models from the same manufacturer were credited with similar life expectancies. While the free-spending customer may gladly shell out for convenience features, he'll wind up with the same motors, bearings, belts, and relays as his more thrifty neighbor.

Don Mennie

New product applications

Pattern recognition allows use of handwritten characters in data-entry system

The "computer pen," initially developed by Stanford Research Institute, will be commercially available by the first quarter of 1975. Called Alphabec-70, the system is capable of recognizing 16 handwritten characters—all ten digits and six additional control symbols.

The system translates the handwritten characters into suitable codes for computer processing. ASCII is the code selected by the manufacturer, but the user may devise his own code for four of the control symbols.

Alphabec-70 "recognizes" the characters written by the operator, by sensing the up-down and left-right movement of a specially developed ball-point pen. Preprocessor and microprocessor units, along with read-only and random-access memories, perform the necessary operations to recognize the written characters and to convert them to computer-usable codes. A readout device displays the recognized symbols, while an audio-response system utters the name of the recognized character for aural verification.

The manufacturer claims that the visual and aural outputs eliminate errors in data entry, by providing the user with early detection and correction of such errors. However, performance statistics indicating the average percentage of correct character detection for various types of handwriting are not available yet.

In spite of this, the manufacturer has already been planning an advanced version of the Alphabec-70 system. This Version II may be programmed to reduce redundancies in the data field and to provide computer-assisted data validation.

The computer-coded output of the Alphabec-70 can be stored in a solid-state memory with a capacity of 500 16-character entries, or recorded on cassettes, when a larger storage capacity is required. The output may also be transmitted over voice-grade telephone lines to a remote data-processing facility.

The vendors of the Alphabec-70 system anticipate that the system will eventually replace many of the 700 000 keyboard data-entry devices now in use. The Alphabec-70 may also expedite field data collection in various utilities and eliminate, according to its promoters, many error sources and delays in data processing, stemming from retranscription of documents.

For further information, contact Xebec Systems Inc., 566 San Xavier Ave., Sunnyvale, Calif. 94086.

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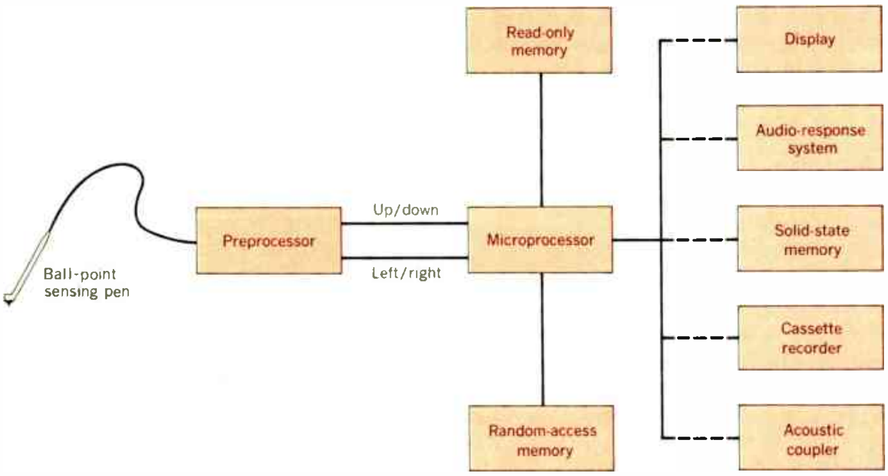
[1] The Alphabec-70 "handwriting recognizer" data-entry system, manufactured by Xebec Systems Inc, in which visual display and audio response of the recognized character permit error detection. Output can be stored or transmitted for processing.



[2] The ball-point pen "front end" in the Alphabec-70.

Microwave couplers employ novel sandwich construction, save cost and size

A family of lightweight 3-dB microwave couplers, featuring an unusual packaging technique that completely seals the coupler structure, is offered by the manufacturer at almost half the cost of similar devices.

Stripline sandwich construction is used. Coupled quarter-wave (quarter-pi) networks are printed on both sides of a thin dielectric film, thermally bonded between two metal-clad (one side only) cover boards. Gold-plated connectors are then attached to the coupler subassembly; both connector and center pins are made of beryllium copper. The assembly is RFI-shielded and then encapsulated in a thermosetting polyester compound. The case material and stripline assembly have nearly identical thermal expansion coefficients eliminating the tendency of the engaged center pins to separate from the printed circuit board at temperature extremes.

The quadrature (90°) couplers cover a frequency range from 500 MHz to 12.4 GHz; five models are offered that span this frequency range in octave bandwidths. Two variations of the five models are available: the QHM-2-*AG series has its mutually isolated port pairs located diagonally across the coupler; the QHM-2-*BG series has its outputs on the same side of the coupler. Both coupler series operate over the same frequency ranges and feature ±0.5-dB output-to-output amplitude equality; 90 ± 1.5-degree output-to-output phase quadrature; 20-dB isolation (typical); and 0.3-dB insertion loss (typical). VSWR of both series is 1.2:1, and average power capability is 50 watts. Small-quantity prices for all models are $60 each. Delivery is from stock to one month, ARO.

For more information, write Merrimac Industries, Inc., 41 Fairfield Pl., W. Caldwell, N.J. 07006.

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