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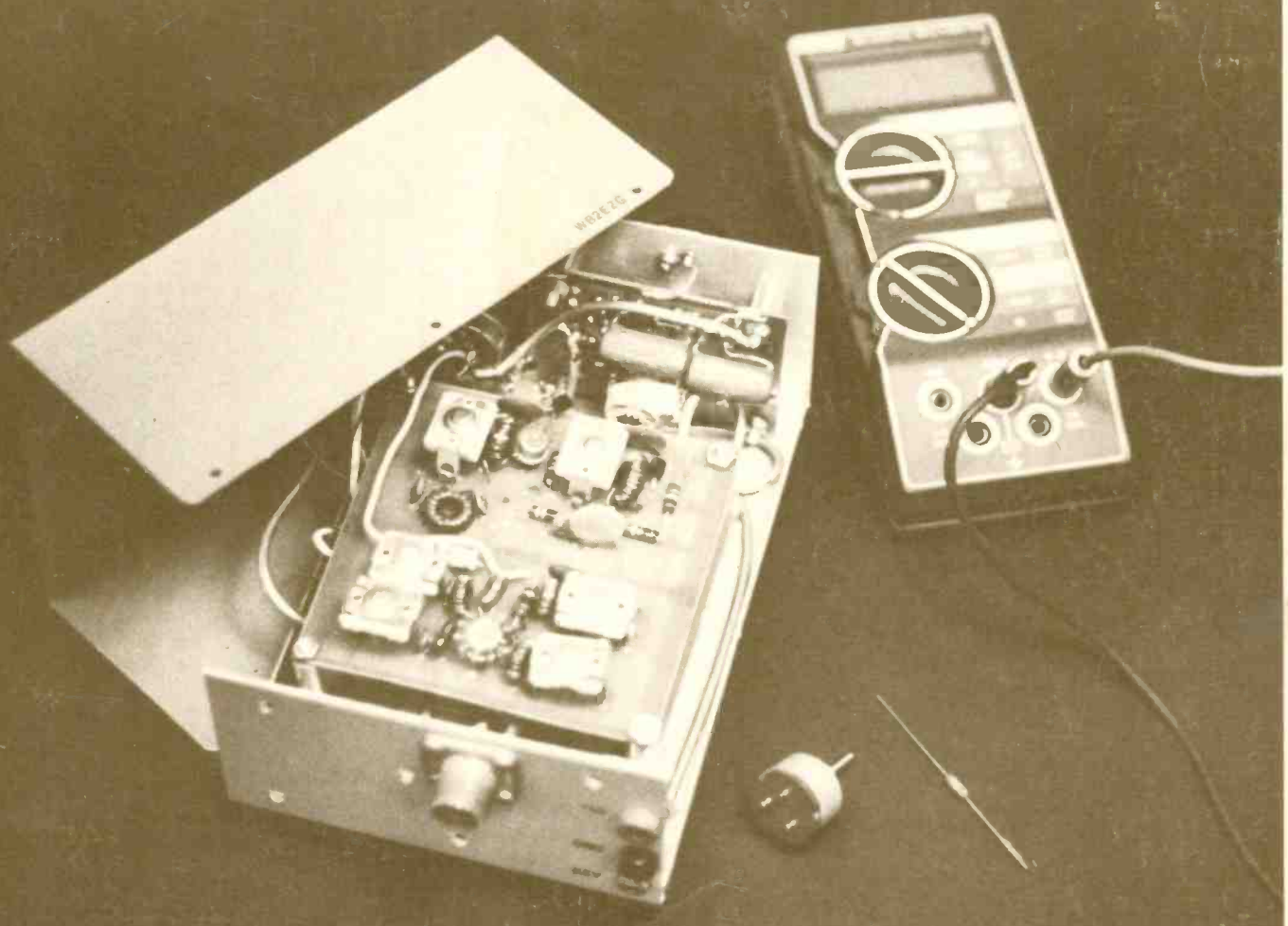
Designer's Casebook Number 4



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Designer's Casebook

PREPARED BY THE EDITORS OF Electronics

Fourth in a continuing series of selected Designer's Casebook sections of Electronics Magazine. This edition includes Electronics issues from January 18, 1979 through June 5, 1980. Also included are feature articles and items from Engineer's Notebook of particular interest to the circuit designer.

Price: $5.00 North America
$12.00 outside North America
Printed in U.S.A.

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1221 Avenue of the Americas
New York, New York 10020

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Standard ICs provide raster scan interface

by Serge Poplavsky
University of New South Wales, Kensington, Australia

One master oscillator and a few counters, flip-flops, and gates make a baud-rate clock with a sync generator that produces horizontal and vertical pulses for noninterlaced raster scanning of a cathode-ray tube. In it, standard integrated circuits are used to generate rates up to 38.4 kilobauds (the upper limit of most generators is only 9,600 bauds) and sync pulses for producing 312 lines at a 50-hertz refreshing rate (or 260 lines for a 60-Hz rate). Thus the circuit is a low-cost solution to building an important part of any data terminal.

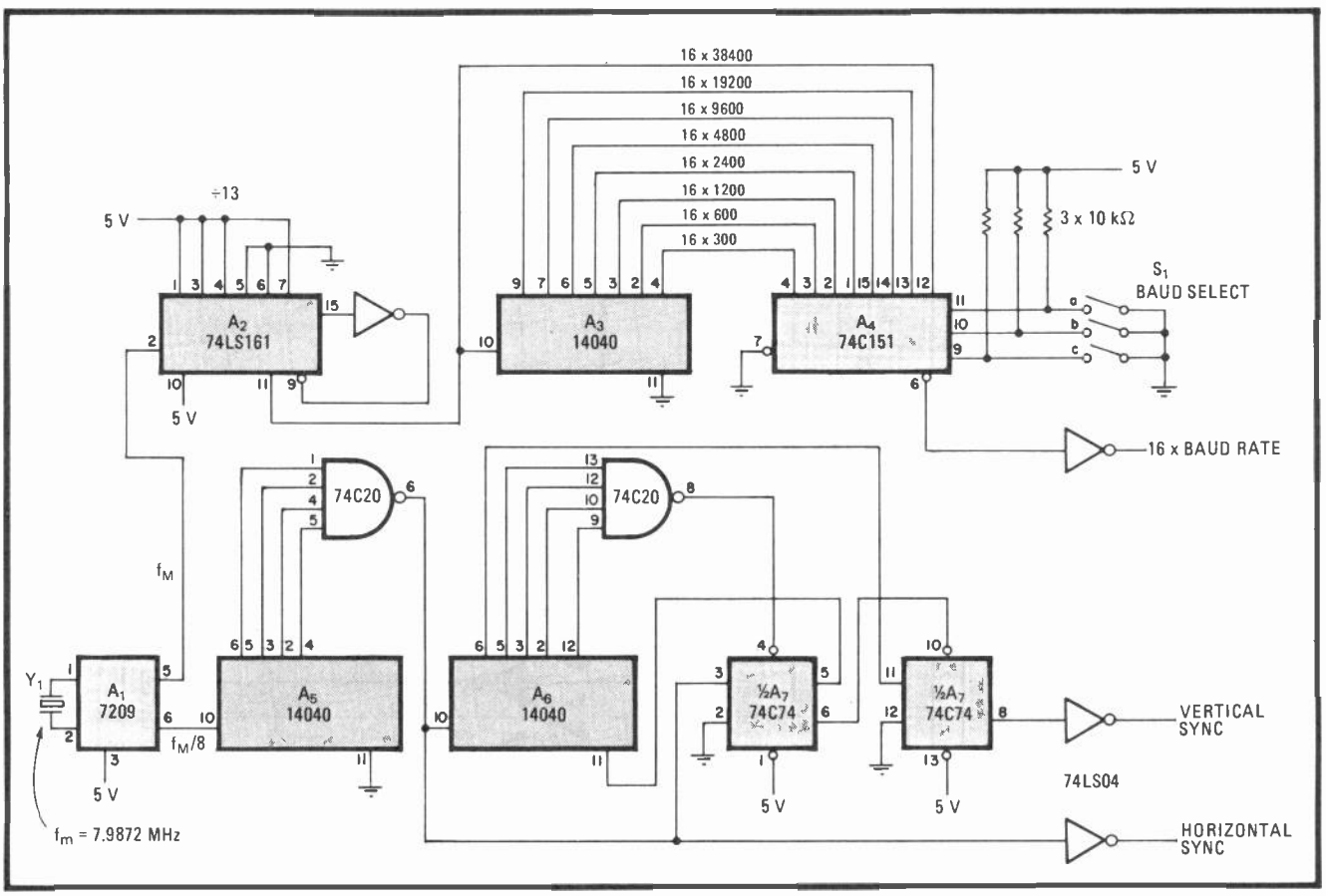
All clock rates are derived from one crystal-controlled oscillator, A_1, which uses the 7209 and a crystal cut for 7.9872 megahertz. The master clock frequency is then divided by 13 by A_2, the 74LS161 presettable counter. A_2 generates a frequency 16 times 38.4 kilobauds, suitable for interfacing with universal asynchronous receiver-transmitters or similar modems.

This frequency is further divided by A_3, the 14040 binary counter. Thus, rates extending from 16×300 bauds to 16×19.2 kilobauds will appear at its output.

S_1, which is used in A_4, the 74C151 one-of-eight-line multiplexer, selects the baud rate desired. When all switches are open, a rate of 300 bauds is selected. Closing switch a, the least significant bit (i.e., binary number 1), selects a baud rate of 600, and so on.

The horizontal sync pulses for the cathode-ray tube are derived from A_5 and a four-input NAND gate, which generates a frequency of 15,600 Hz, each pulse lasting 4 microseconds. The vertical sync frequency, either 50 or 60 Hz, is obtained from A_6–A_7 and a four-input NAND gate.

Dividing the horizontal sync pulses by 312 or 260 (for 50 or 60 Hz, respectively), the binary counter, A_6, which in this case is wired as a divide-by-312 device, drives two flip-flops (A_7). A_7 resets the counter and generates vertical sync pulses, each 256 μs long. □



Versatile. Using standard integrated circuits, combination baud-rate generator and sync generator for CRT works up to 38.4 kilobauds and can be wired to generate sync pulses suitable for a 50- or 60-Hz refreshing rate. All frequencies are derived from one oscillator.

Gates replace PROM in Intellec-8 bootstrap loader

by Simon Gagné and Bernard Boulé
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In what may be the most cost-effective solution yet for implementing a bootstrap loader for Intel's popular Intellec-8 development system, logic gates are used to replace the jump-to-monitor routine stored in a programmable read-only memory (PROM).[1] This simple method of automatically accessing the system's monitor, or executive-control routines, is possible because the set of 8-bit logic signals required at the data bus to access the monitor on power-up can be easily generated.

In the Intellec-8, the monitor is located at address 3800 (hexadecimal). Therefore, a jump instruction is used to advance the program counter from location 0 to 3800H. To avoid the manual programming required after each power-up, the previous solution was to use a PROM programmed with the instruction (C3 00 38).

The logic signals required on data bus lines D_0–D_7 for achieving the three-byte jump instruction are shown in Fig. 1a. The output of each flip-flop in the three-stage 74175 shift register, previously used to enable the PROM, together with simple logic, can synthesize this sequence.

When the outputs of the shift register (Q_1, Q_2, and Q_3) alone are stepped with system clock $\overline{DBIN}$, they generate the signal pattern shown in Fig. 1b. Comparison of Fig. 1a and 1b reveals that the identical patterns of lines D_0–D_1 and D_6–D_7 can be generated by forming the logic function $\overline{Q}_1 + Q_3$. It is also seen that bits D_3, D_4, and D_5 are identical to the Q_2 output of the shift register and the D_2 bit is identical to the Q_3 output, so that the Q_2 and Q_3 signals can simply be connected to these corresponding data lines through noninverting buffers. To make the final circuit, which appears in Fig. 2, operational, switch S_1 need only be placed in the monitor position for automatic loading on power-up. □

References
1. "PROM adds bootstrap loader to Intellec-8 development system," *Electronics*, April 27, 1978, p. 126.

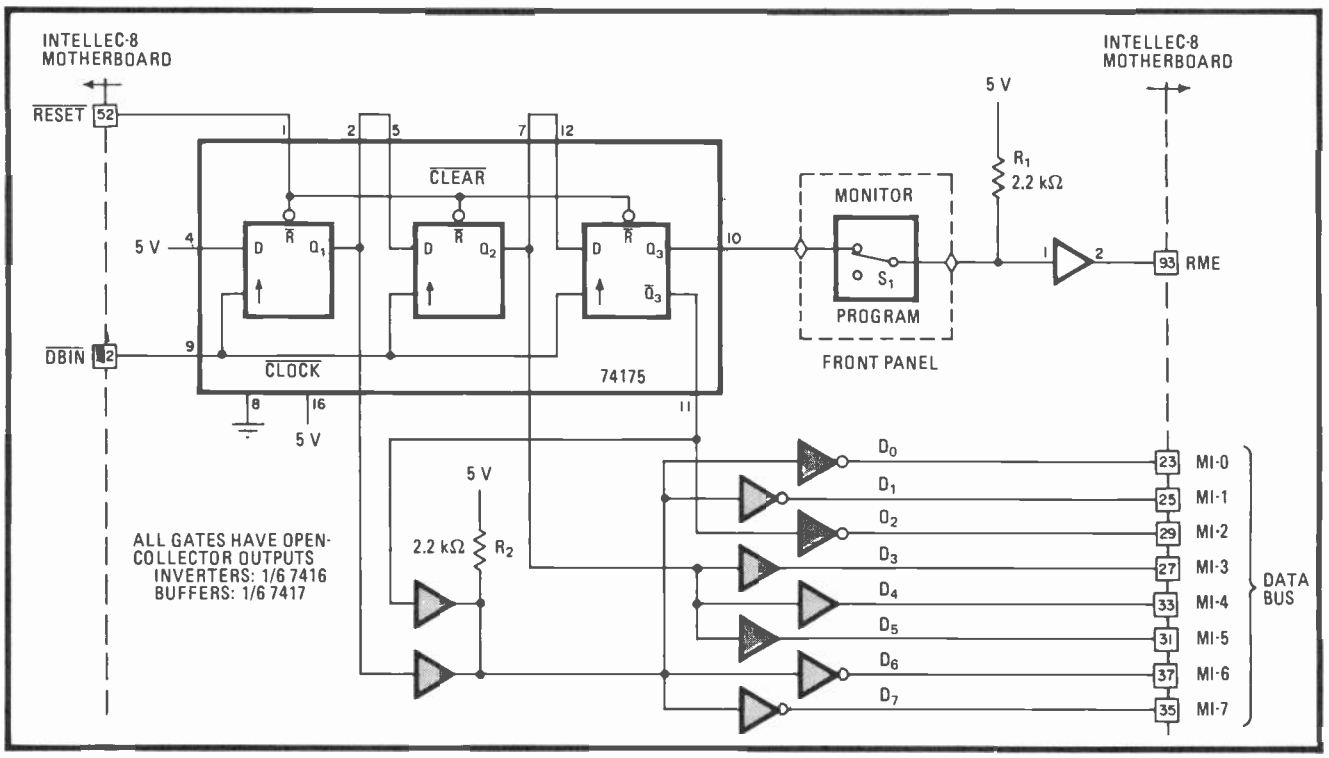
(a)

Instruction	Op code	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
JMP 3800H	C3	1	1	0	0	0	0	1	1
	00	0	0	0	0	0	0	0	0
	38	0	0	1	1	1	0	0	0
(AFTER JMP)	FF	1	1	1	1	1	1	1	1

(b)

Condition	Q_1	Q_2	Q_3
RESET	0	0	0
AFTER FIRST $\overline{DBIN}$	1	0	0
AFTER SECOND $\overline{DBIN}$	1	1	0
AFTER THIRD $\overline{DBIN}$	1	1	1

1. Synthesis. Table outlines logic sequence required on data bus for achieving jump operation in order to enter Intellec-8's executive program (a). Outputs of clocked three-stage shift register of basic circuit generate signals (b), which can be used to synthesize D_0–D_1 and D_6–D_7 signals if function $\overline{Q}_1 + Q_3$ is formed with logic gates. Q_2 output is by itself identical to D_3, D_4, and D_5. Q_3 output is identical to D_2.



2. Implementation. Circuit for accessing system's monitor uses open-collector logic gates, which replace programmable read-only memory in original configuration. Circuit is armed by placing front-panel switch S_1 in monitor position before each power-up of system.

Circuit phase-locks function generators over 360°

by Lawrence W. Shacklette
Seton Hall University, South Orange, N. J.

This circuit locks a low-cost function generator without a voltage-controlled-oscillator (VCO) input to a second inexpensive generator having such a phase-reference feature. A J-K flip-flop, two one-shots, two comparators, and an operational amplifier are linked in a feedback arrangement that includes the programmable generator as the VCO in a phase-locked loop (PLL). The resultant circuit provides a selectable phase shift between generator outputs over the range of 0° to 360°.

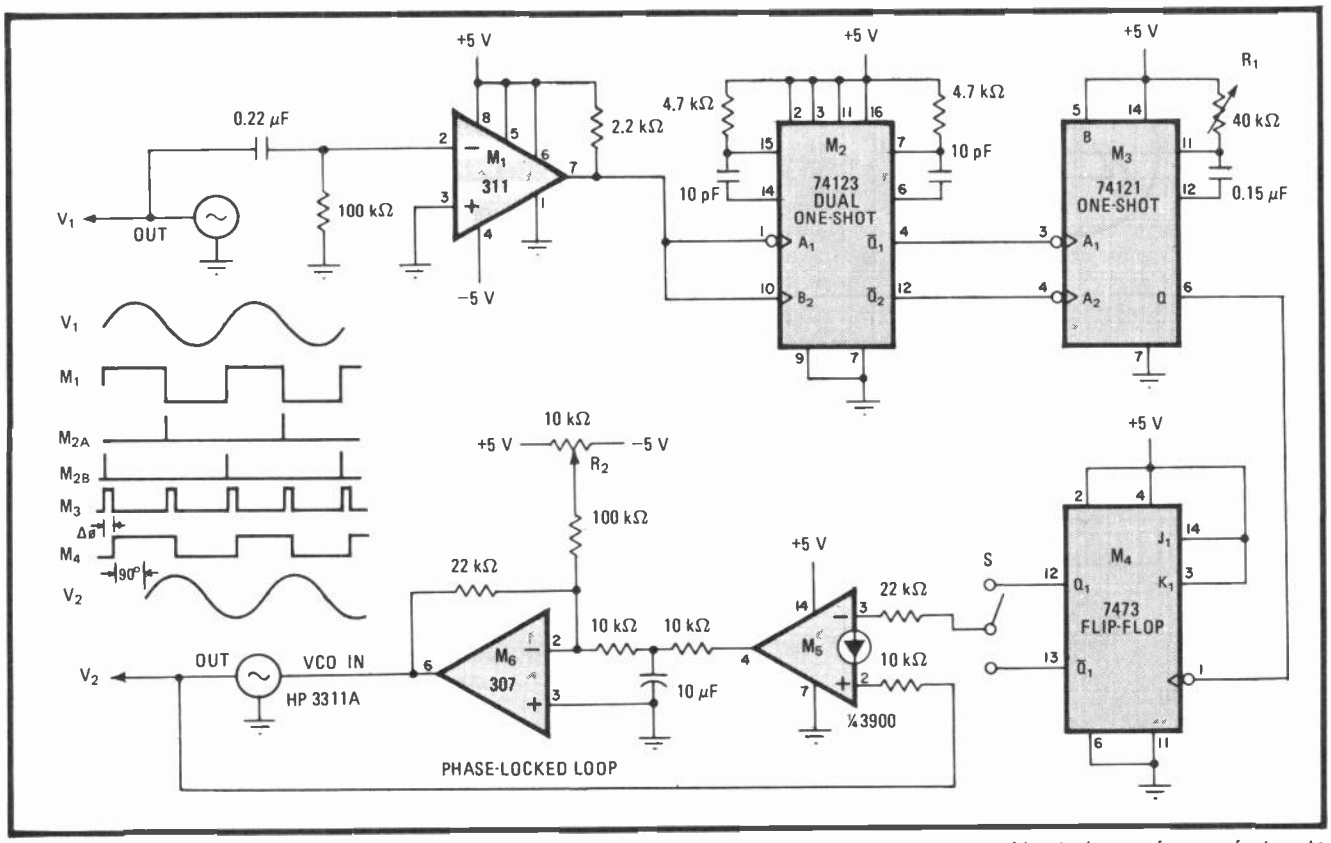
In operation, the output of the low-cost generator, v_1, passes through a high-pass filter to a zero-crossing detector that employs a 311 comparator (M_1), as shown. A dual monostable multivibrator and J-K flip-flop follow. Although these two devices can be eliminated, they enable the phase-locked loop to be operated at the center of its locking range for any phase shift. This arrangement ensures that two often desired phase angles, 0° and 180°, fall within the capture range of the PLL, so that if locking is lost, it will be automatically regained.

The outputs of the dual one-shot, M_2, wired so that each fires on opposite edges of the signal applied to its inputs (see timing diagram), are fed to the OR input of M_3, whose on time is selected by potentiometer R_1. Thus R_1 controls the amount of phase shift.

M_3 produces two pulses for each cycle of v_1 and triggers the J-K flip-flop, M_4, on each negative edge. The flip-flop thus produces a square wave with a frequency equal to v_1, but shifted in phase by up to 180°. An additional shift of 180° can be obtained by using switch S to connect the Q output of M_4 to the inverting input of the 3900 Norton amplifier.

The adjustable-phase square wave serves as a reference signal for the phase-locked loop, which is composed of the 3900, a low-pass filter, a buffer (307), and a VCO (the second function generator, a Hewlett-Packard 3311A). The input signal to the VCO is a negative dc voltage that is the inverted sum of the filtered output of the 3900 and the voltage selected by the offset control, R_2. By turning the generator's front-panel control or R_2, the free-running frequency of the loop can be adjusted.

Because the reference signal is a square wave, the PLL will lock onto either the fundamental of v_1 or its odd harmonics. Selection of a particular harmonic is made by adjusting the free-running frequency to the approximate value of the harmonic desired. Half-multiple harmonics ($\frac{1}{2}f_1$, $\frac{3}{2}f_1$, $\frac{5}{2}f_1$, etc.) can be produced at v_2 by breaking the $\overline{Q}_1$–A_1 connection between M_2 and M_3 and tying A_1 to +5 volts. Even harmonics can be obtained by using the remaining flip-flop in the 7473 as a divide-by-2 counter, and placing it between the output of the VCO and the 3900's noninverting input. □



Phase-locked. Comparators, one-shots, and flip-flop combine to provide stable locking of generators without phase-reference feature to those having a VCO input. R_1 and S are used to select phase of v_2 with respect to v_1; phase can be adjusted from 0° to 360°. M_2 and M_4 ensure that locking is regained if it is lost, and R_2 controls lock frequency, which may be set to integer or half-integer harmonics of v_1.

Coordinate converter aligns piezoelectric positioner

by Lawrence E. Schmutz
Adaptive Optics Associates, Cambridge, Mass.

Piezoelectric tilt elements of the kind used to position laser beams and optical scanners can be aligned with the help of this circuit, which converts the transducer's high input driving voltages, normally resolved in X-Y coordinates, into corresponding coordinates (a, b, c) in a nonorthogonal three-axis system. Only one quad operational amplifier and two resistor-array packages are used for the transformation.

The geometry of many popular piezoelectric positioning elements (a), as for example the Burleigh Instruments' PZ-80, is such that:

$$x = c - a \qquad y = b - \tfrac{1}{2}(a + c) \qquad 0 = a + b + c$$

Solving these equations simultaneously for a, b, and c yields:

$$a = \tfrac{1}{2}x - \tfrac{1}{2}y \qquad b = \tfrac{2}{3}y \qquad c = -\tfrac{1}{2}x - \tfrac{1}{3}y$$

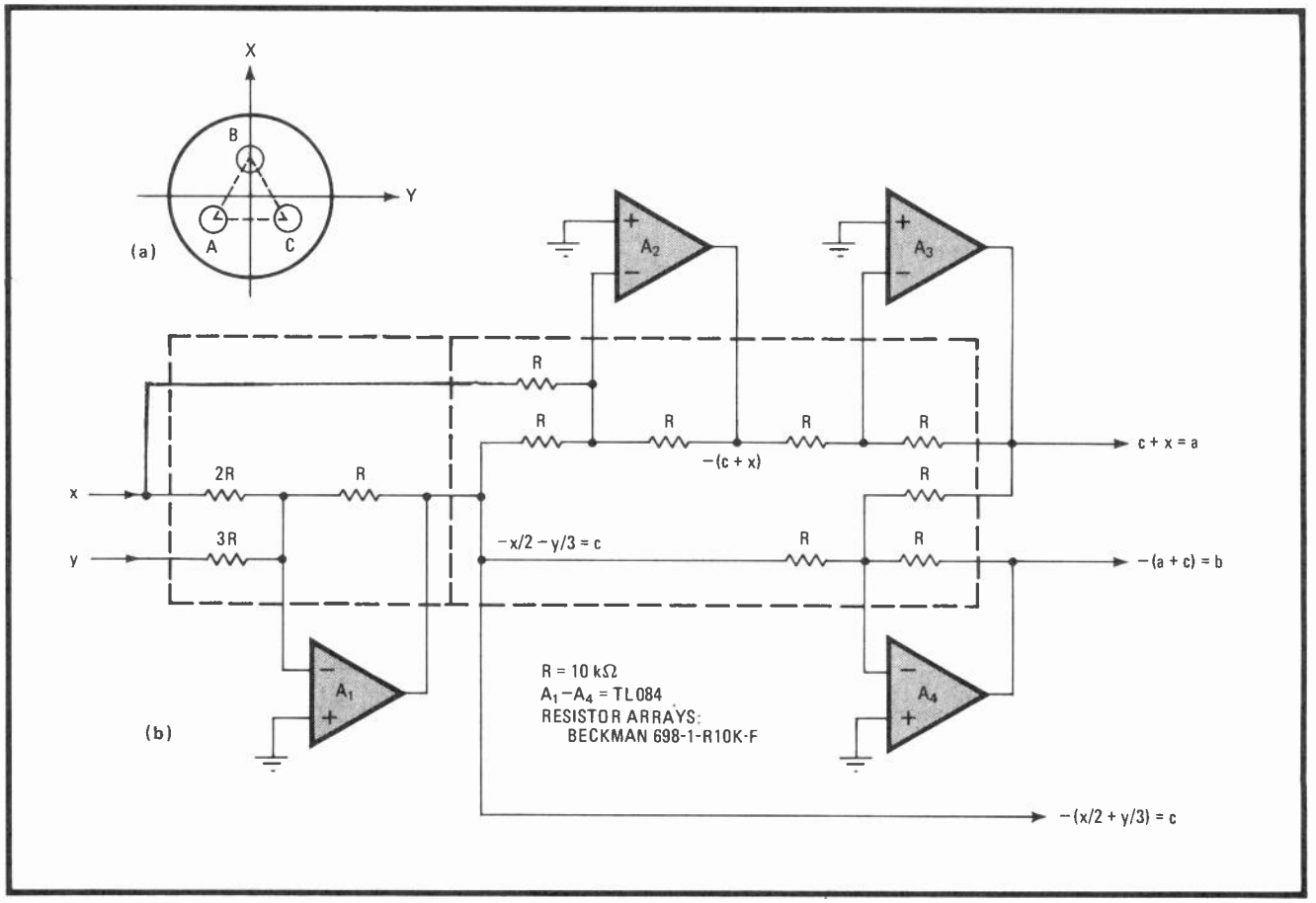
Simplifying further:

$$a = c + x \qquad b = -(a + c) \qquad c = -(x/2 + y/3)$$

The last set of equations is easily implemented by using precision resistors to set the gain of several op amps (b).

Resistor arrays in dual in-line packages will perform the transformation accurately, for their elements have a tolerance of ±0.5%. The overall circuit uncertainty becomes ±1% when two arrays are configured as shown. To ensure that the circuit occupies no more space than that taken by three dual in-line packages, the resistors are grouped in their respective arrays as shown by the dotted lines.

The TL084 op amp is more than adequate for the circuit accuracy desired, since in most applications the piezoelectric devices operate in the lower audio-frequency range. □



Beaming true. Input information for positioning laser beam, normally presented in X-Y coordinates, must be converted into three-axis coordinates for many piezoelectric transducers (a). One op amp and two precision resistor arrays perform the transformation (b).

Acoustic protector damps telephone-line transients

by Gil Marosi
Intech Function Modules Inc., Santa Clara, Calif.

By limiting the transients on telephone lines, this acoustic shock protector prevents those sudden high sound levels that can damage the ear badly enough to cause loss of hearing. It holds the maximum peak-to-peak voltage at the receiver of a telephone headset to 50 millivolts.

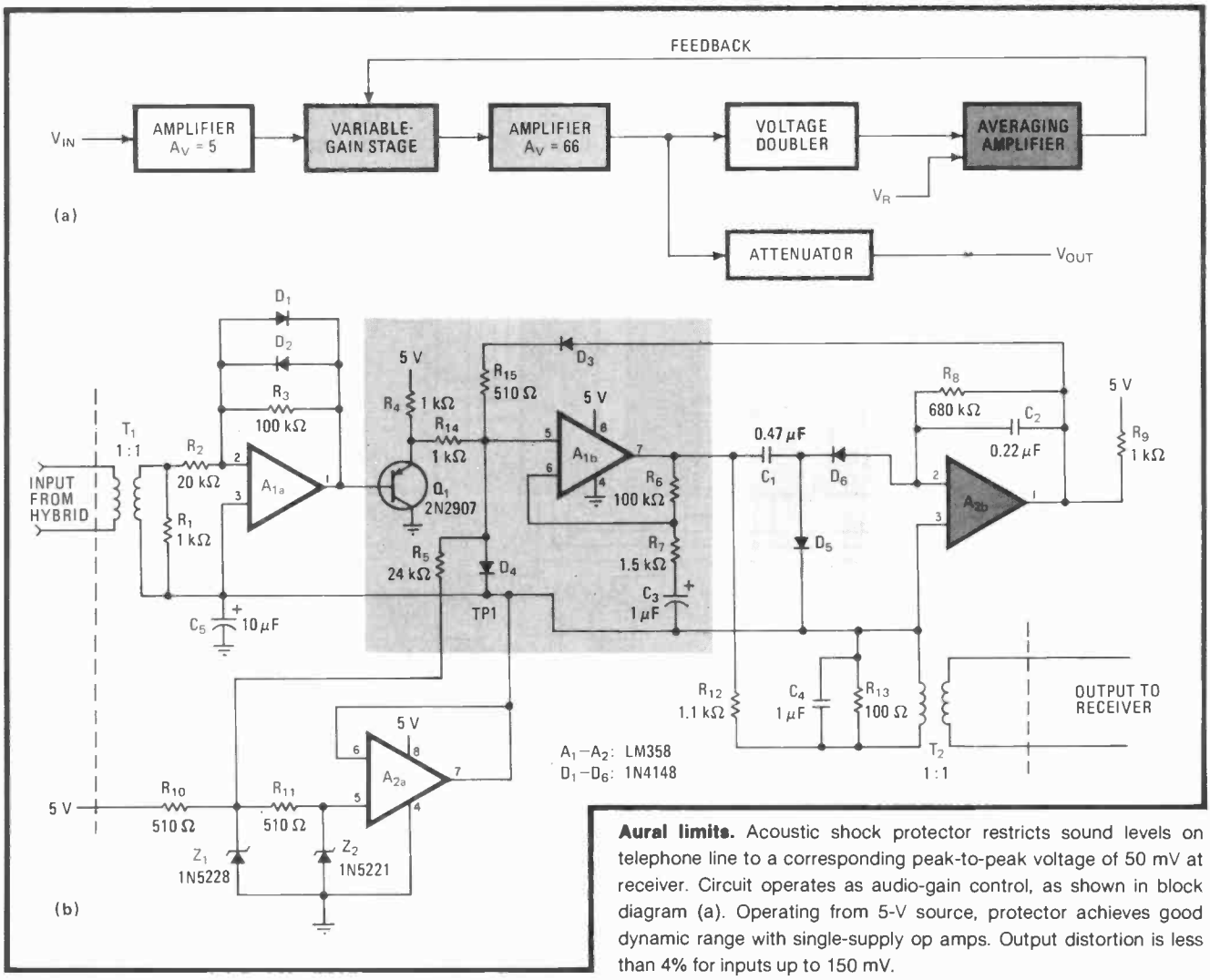
A four-terminal device, the shock protector is inserted between the receiver side of the telephone hybrid and the receiver proper. A block diagram of the circuit, which operates from a single 5-volt supply, is shown in (a). Input signals are amplified by a factor of 5 and applied to a voltage-controlled, variable-gain stage. Because this stage also attenuates the signal to the degree indicated by the actual level of a feedback signal, further amplification may be needed, and is available, to retain the loop's gain margin. A voltage doubler then converts the amplifier signal to a dc voltage. This voltage is compared with a preset reference at the inputs of an averaging amplifier.

The output of the averager, which is essentially an integrating network, is connected to the variable-gain stage. As the input voltage from the hybrid becomes greater, so does the feedback voltage, and thus still more attenuation is provided for the variable-gain stage.

As for the actual circuit (b), transformers T_1 and T_2 isolate the protector from the floating telephone line, so that the circuit operates from a 5-v supply referred to ground. A_{1a}, one half of an LM358 operational amplifier, provides the required amplification of the input signal. D_1 and D_2 clamp A_{1a}'s output to 0.7 v and introduce the signal to buffer Q_1. This transistor, along with R_4–R_7, R_{14}, D_4, A_{1b}, and C_3, make up the variable-gain stage.

Zeners Z_1 and Z_2 and op amp A_{2a} bias A_{1a} and A_{1b} so that input signals to those stages swing about a quiescent point of 2 v. The circuit thus provides maximum dynamic range. Note that most op amps require a 12-v supply to achieve a comparable range.

Q_1's output is converted to a current with the aid of R_{14}. Current flows through D_4, which operates as a current-controlled variable resistor. D_4 is biased through



Aural limits. Acoustic shock protector restricts sound levels on telephone line to a corresponding peak-to-peak voltage of 50 mV at receiver. Circuit operates as audio-gain control, as shown in block diagram (a). Operating from 5-V source, protector achieves good dynamic range with single-supply op amps. Output distortion is less than 4% for inputs up to 150 mV.

R_5 such that its nominal resistance is 500 ohms.

The voltage at the noninverting input of A_{1b} is amplified and applied to the voltage doubler (C_1, D_5, and D_6). A_{2b} and its associated circuit perform the averaging function that provides a feedback current to the variable-gain stage. The gain from input to output is unity until the amplifier's input threshold—set at 50 mV—is exceeded. The acoustic shock protector then operates as an automatic gain control for inputs up to 150 mV. The output distortion up to that point does not exceed 4%. Beyond 150 mV, however, the protector simply clamps the output to 50 mV p-p without regard to distortion.

Because the phone receiver is an inductive device, its impedance increases with frequency. C_4 is placed across R_{14} to compensate for this rise in impedance. The overall gain of the acoustic shock protector is thus held flat to within 1 decibel from 300 hertz to 3 kilohertz so long as the output of A_{1b} is below 600 mV or so. □

Time-shared counters simplify multiplexed display

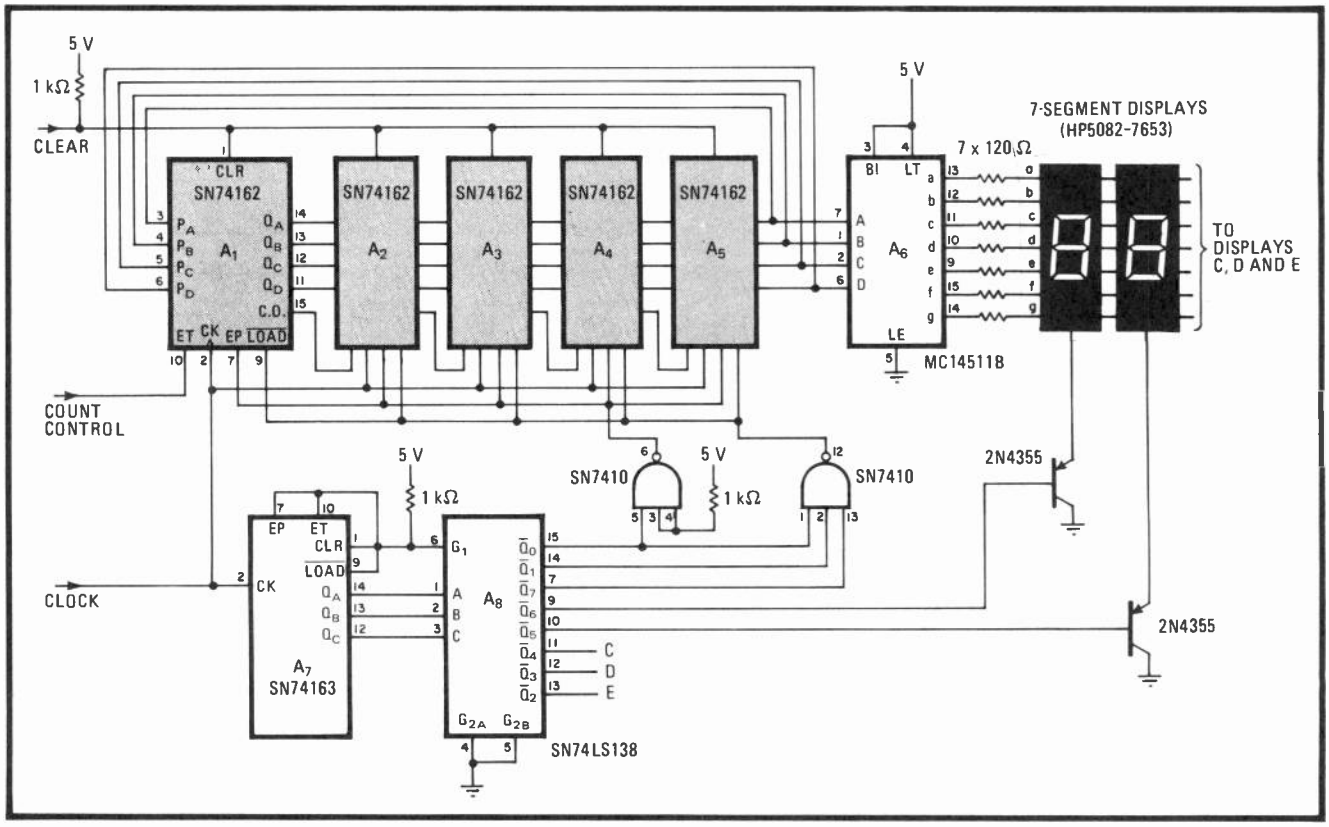
by Darryl Morris
Northeast Electronics, Concord, N. H.

Although multiplexed display circuits reduce the number of components otherwise required for decoding on a per-digit basis, additional hardware is then needed to select and multiplex various lines to the display. But if a display is driven by a frequency counter, as is often the case, the counter itself can be made to perform the multiplexing with only minimal extra circuitry.

Multiplexing is done by using a master clock having several times the frequency of the normal clock, depending on the number of digits to be multiplexed, and by time-sharing the counters between the count and display mode. In the count mode, the $\overline{\text{LOAD}}$ and enable-P (EP) inputs of the counters shown are high and A_1–A_5 function as a conventional cascaded counter circuit under control of the enable-T (ET) input of A_1. The counter circuit advances one count for each clock period during which the count control line is high.

During the display mode, the control line and $\overline{\text{LOAD}}$ input of A_1–A_5 move low. The counters now accept data at their preload inputs, P_A–P_D. Because the preload inputs are connected to each preceding set of a counter's outputs, A_1–A_5 operates as a 4-bit-wide recirculating shift register when clocked. Thus, the contents of each counter is rotated past the seven-segment decoder (A_6) during its display interval, and the appropriate digit in the display is strobed by the mode controller, A_7 and A_8.

This technique offers the best saving in chip count when the count rate is slow or numbers are to be displayed only after the counted event has terminated. □



Time-shared. Counter circuit switches between count and display modes without selector devices. Counter operates as 4-bit-wide recirculating shift register. Master clock frequency is assumed to be several times that used for the counting circuits.

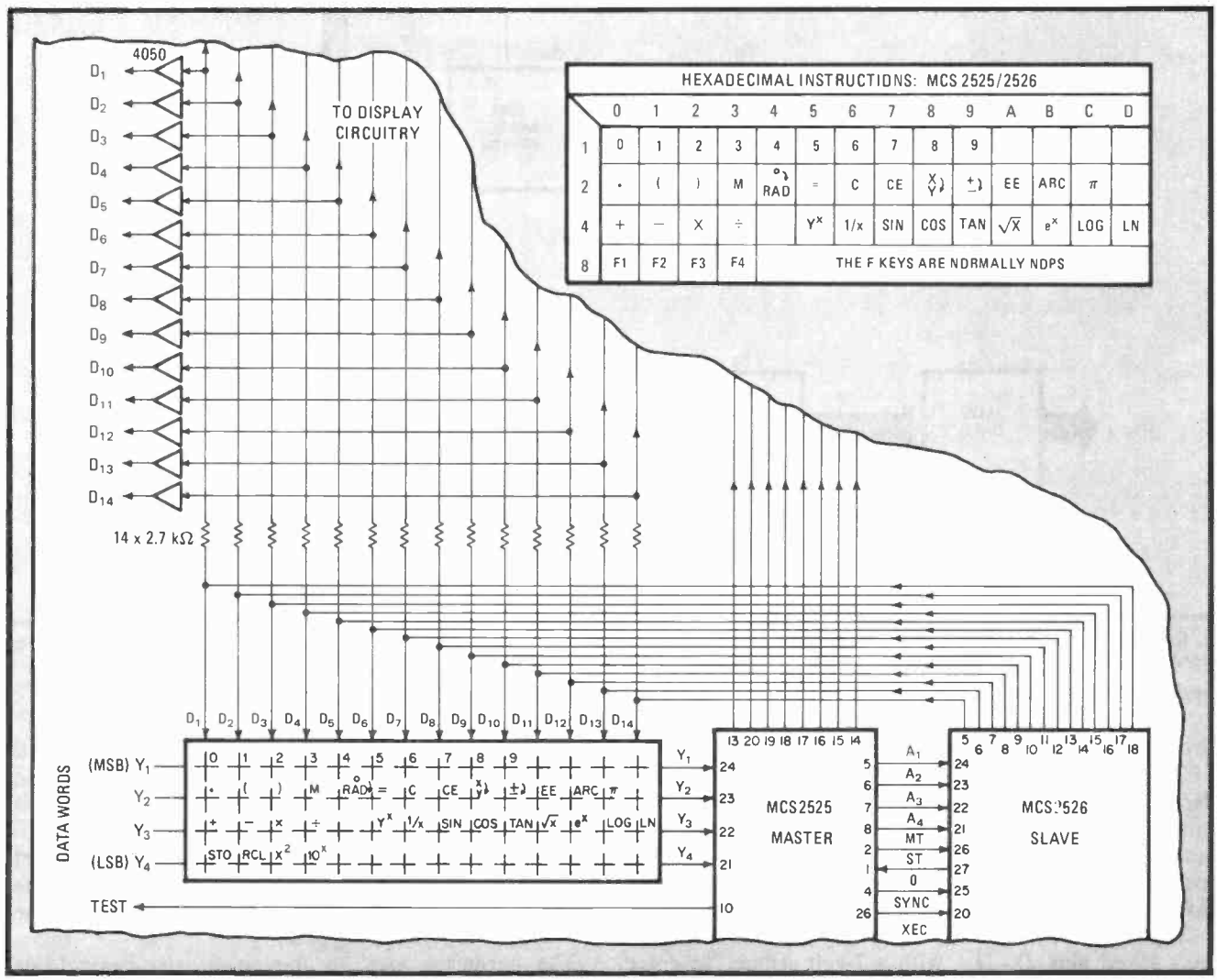
TTL and C-MOS interface unites microprocessor with calculator

by Bert K. Erickson
Fayetteville, N. Y.

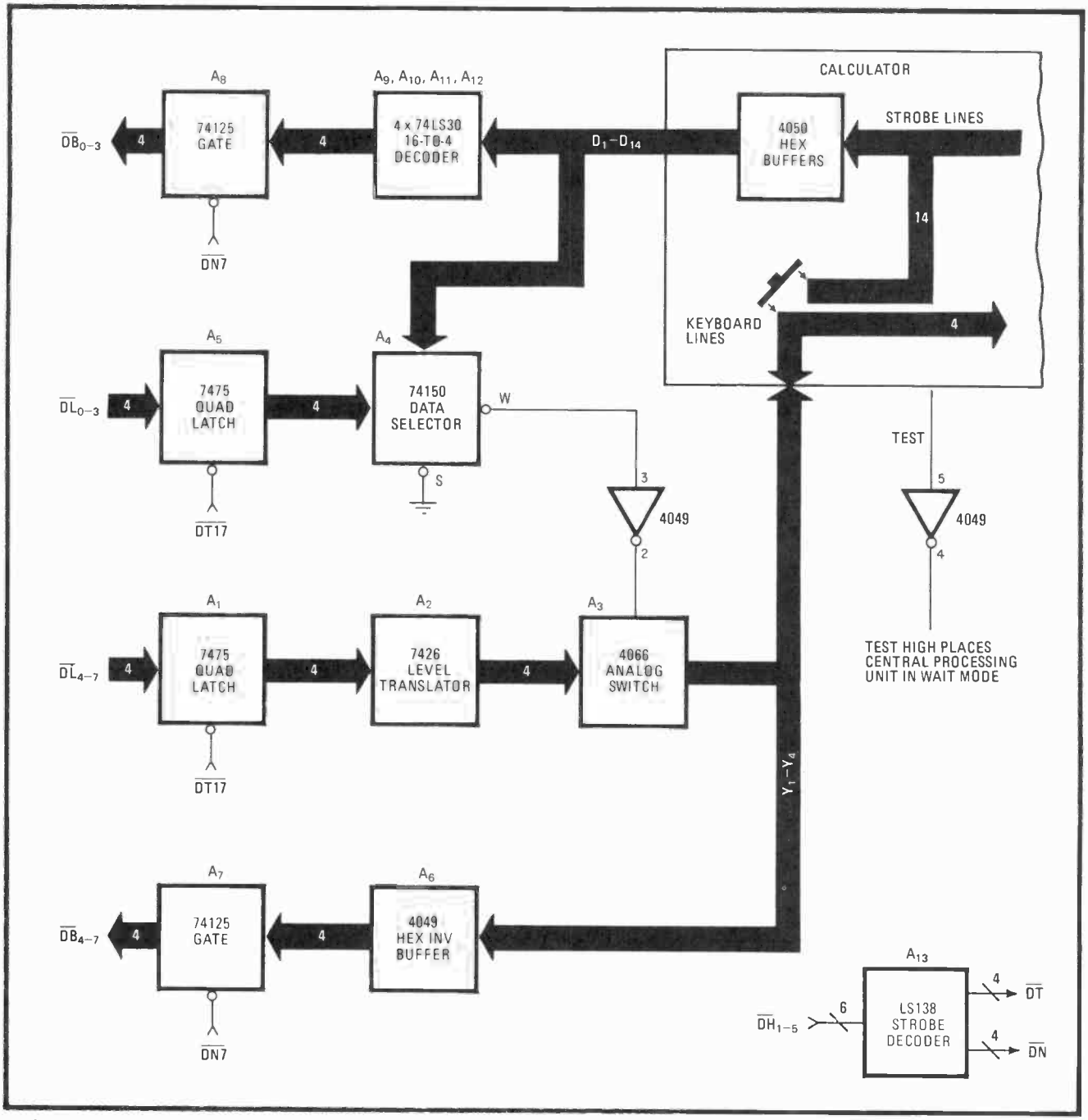
This interface combines a general-purpose scientific calculator, which performs rapid arithmetic operations, with the extensive memory of 8-bit microprocessor-based systems into a system that has the advantages of both. Here, the calculator can program or be programmed exclusively by the microprocessor; ultimately, of course, it is programmed by software residing in system memory. Alternatively, the calculator can be used for its normal purpose. Using transistor-transistor-logic and complementary-metal-oxide-semiconductor devices, the interface costs less than $20 dollars.

Virtually any microprocessor can be united with any calculator, assuming the calculator's keyboard can be accessed. In general, the keyboard scanning lines will be connected to the calculator's corresponding display driver pins and to the microprocessor system through appropriate circuitry. A two-key roll-over feature that inhibits data entry when two keys are depressed simultaneously should be included. Several lines from the microprocessor will be connected to the keyboard so that microprocessor instructions can be entered into the calculator.

Figure 1 shows how a typical calculator (MOS Technology's two-chip MCS2525/2526) was initially modified to interface with a microprocessor. A set of buffers (4050) serves as the link between the strobe lines and the



1. Lines of command. MCS2525/2526 calculator chip pair sends instructions to 8000 microprocessor through appropriate 4050 buffers when corresponding key is depressed. Alternatively, microprocessor can program calculator when half of data word is introduced at Y_1–Y_4; other half of data word and calculator's strobe circuits generate D_1–D_{14} signals at keypad, so that key closures are simulated.



2. Control. Interface transmits keypad instructions to 8000 processor and also aids in simulating key closure for calculator programming by 8000. Accompanying sample program for displaying digits sequentially has built-in delay instructions to slow input-data rate, so that a keyboard scan can be completed for each word entered at the calculator. Two-key roll-over protection is also provided.

input to the microprocessor for programming by the MCS2525/2526. The 2.7-kilohm resistors are used to decouple the calculator from the buffer input in order to minimize loading of the MCS2525/2526. Decoupling resistors should also be placed in series with the calculator's input lines, Y_1–Y_4, where microprocessor instructions (data words) to the 2525/2526 are entered.

The MCS2525/2526 automatically scans the calculator's keyed pins, D_1–D_{14}, with a 7-volt strobe. To enter an instruction from the microprocessor, a keypad closure is simulated from the data entered at lines Y_1–Y_4 and on lines D_1–D_{14}. By applying the first 4 bits of the 8-bit data word at the Y lines and by introducing the last four bits at the D lines, key closure is simulated. For example, to enter digit 5, line Y_1 must be brought high while D_6 is being strobed (an instruction corresponding to hexadecimal number 15, as shown in the particular instruction set for this microprocessor-calculator). Alternatively, the microprocessor can be programmed by depressing the appropriate key on the keypad.

The hardware used to implement the keypad-line coding is shown in Fig. 2. For generating calculator instructions, the upper 4 bits of the data word, which are eventually applied to Y_1–Y_4, is latched into A_1. The

output of A_1 is shifted in level by open-collector gate A_2, and the 7-v strobe is applied to the keyboard lines by analog switch A_3.

A_3 is switched on by selector A_4 through the 4050 buffers, and A_4 is scanned in the same sequence as the columns of the keypad. The input line selected for enabling A_3 at the proper time is determined by the lower 4 bits of the data word stored in A_5. Information stored in the microprocessor can now be processed by the calculator, providing the instructions are applied to Y_1–Y_4 at a slow rate (the time it takes to depress a key manually). Time delays are therefore required, since the microprocessor can generate instructions much faster than the calculator can scan the keypad. The delays are provided by the program itself.

If the microprocessor is to be controlled by the calculator, its keypad rows are interrogated by A_6 and applied to the input port of A_7. The keyboard columns are scanned and applied to the input port of A_8.

As for the actual programming of the calculator by the microprocessor (in this case an 8000), a sample program is shown in the table. This program generates the digits 1 through 9 on the calculator's display in succession. When all digits are displayed, they blink three times. The sequence then repeats. Though this subroutine has little practical value, it demonstrates several characteristics of the software required for programming.

The program, stored in random-access memory, is switched to the starting address on page 0, and the restart address is entered on the keypad. The program is then initiated with an interrupt request to the microprocessor, which may be entered from the keypad if one of the unused function keys is wired appropriately for the interrupt code required.

The RST 6 branch instruction provides the calculator with ample time to complete a keypad scan between program steps. To absolutely prevent instructions from arriving at the calculator's input while an instruction is being executed, the test pin of the MCS2525/2526 can be connected to the microprocessor's wait input. Instructions A8, 35 simulate the two-key roll-over feature mentioned earlier. □

MICROPROCESSOR/CALCULATOR TEST PROGRAM: SEQUENTIAL DIGIT DISPLAY

Label	DH register	DL register	Op code	Mnemonic	Comments
RST 6	01	30	5F	OUT 17	
		31	10	INR C	
		32	48	JNZ	
		33	31	31	Keyboard scan delay
		34	01	01	
		35	07	RET	
		·	·	·	
		·	·	·	
RST 7	01	38	0E	MVI B	Set first digit
		39	11	11	
		3A	26	MVI E	Set digit count
		3B	1D	1D	
		3C	C1	MOV AB	
		3D	1E	MVI D	Set display time
		3E	E0	E0	
		3F	35	RST 6	
		40	18	INR D	Display sequence
		41	48	JNZ	
		42	3F	3F	
		43	01	01	
		44	A8	XRA A	Release digit
		45	35	RST 6	
		46	08	INR B	
		47	C1	MOV AB	
		48	BC	CMP E	Enter and display next digit if zero is not set
		49	48	JNZ	
		4A	3D	3D	
		4B	01	01	
		4C	06	MVI A	Enter clear
		4D	26	26	
		4E	35	RST 6	
		4F	A8	XRA A	Release clear
		50	35	RST 6	
		51	3D	RST 7	Repeat subroutine

Synchronous counters provide programmable pulse delays

by R. E. S. Abdel-Aal
Sunderland Polytechnic, Sunderland, England

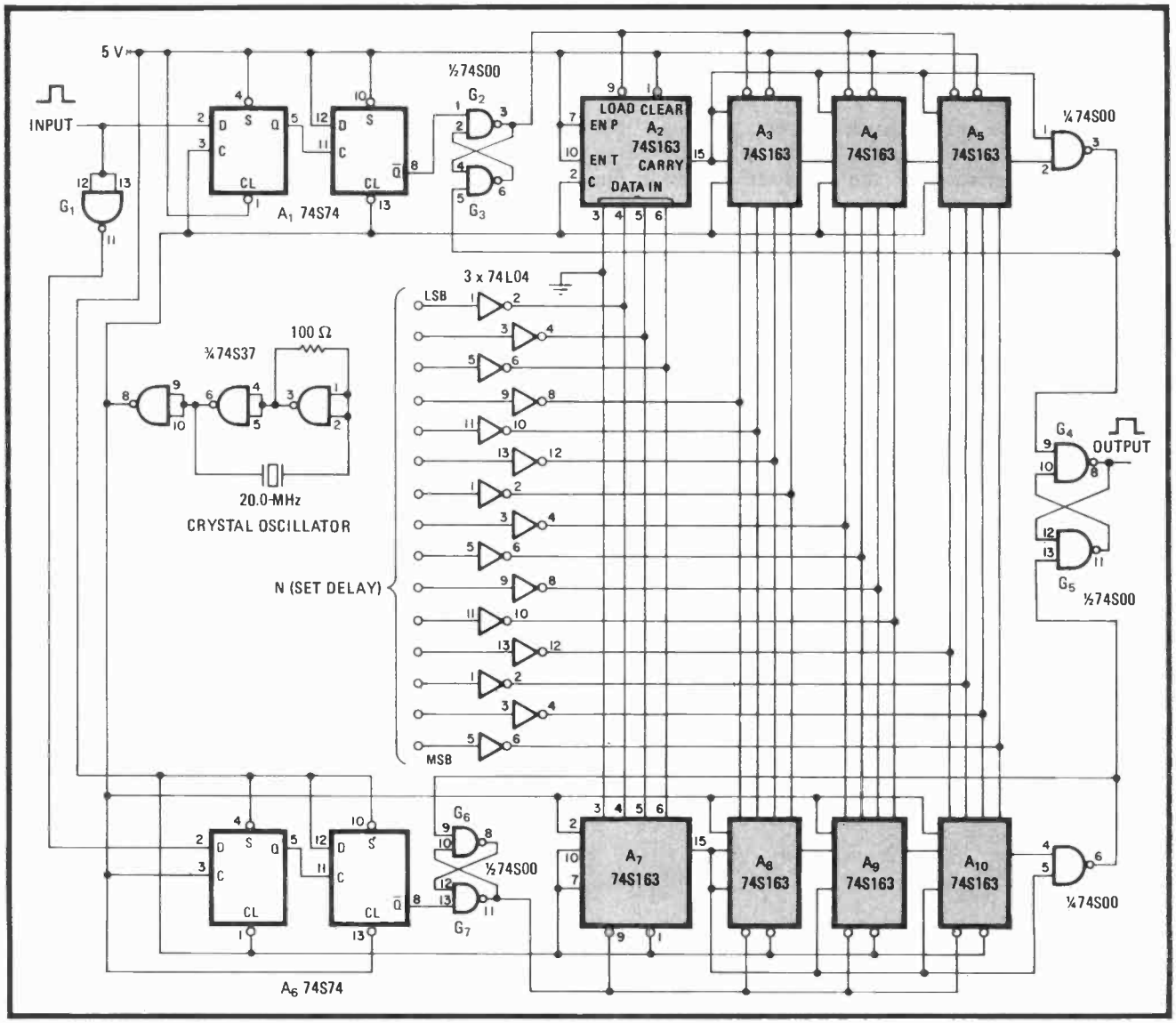
In this circuit, cascade counters are digitally programmed to provide pulse delays of 50 nanoseconds to 3.25 milliseconds, accurate to within 50 ns. Selected by a 15-bit binary number, N, the delays can be ordered in 100-ns steps.

Two chains of synchronous counters, driven by a 20-megahertz clock, delay the input pulse's leading and trailing edge separately. Input pulses, which are asynchronous, are first applied to a dual D flip-flop, A_1, as shown. A_1 generates a single negative-going clock pulse when triggered by the 20-MHz clock. The pulse is used to set the bistable latch, G_2–G_3, thus enabling counters A_2–A_5 to delay its leading edge.

A_2–A_5 are wired to perform a fast look-ahead operation for the high-speed multistage counting required. To eliminate glitches that might upset the counter, the carry outputs of both A_1 and A_5 are brought to a NAND gate and then to G_2–G_3. This ensures the latch will be reset and the desired N value loaded into the counter only after the previous delay period is ended, despite the differential delays that exist in the signal path.

The input pulse is inverted by G_1 and applied to flip-flop A_6 for the counters that provide delay on the trailing edge of the pulse, A_7–A_{10}. G_6–G_7 and A_7–A_{10} perform the function identical to G_2–G_3 and A_2–A_5.

In actual operation, both counter chains are programmed by the set-delay lines, which are connected to their data-in ports. The delay time is given by $T = 50(1 + 2N)$ ns. At the end of the delay period, N is



Two-edge retardation. Counter chains, of which one starts counting on arrival of the positive edge of an input pulse, the other on its negative edge, use a 20-MHz clock to provide repeatable delays of 50 ns to 3.25 ms on both edges of signal. Delays produced are accurate to within 50 ns. Amount of delay is selected with 15-bit word (M). Width of input signal to be processed must be at least 60 ns.

loaded into both counter chains. Note that the circuit is wired such that the N inputs must be active high, ensuring that maximum delay will correspond to a value of N that, when read as a number in standard binary form, is maximum.

Upon the arrival of the leading edge of the input pulse, A_2–A_5 count up, starting from the number loaded. Similarly, A_7–A_{10} count up on the trailing edge of the pulse. The carry pulse generated by A_5 signifies the end of the delay period. This signal is united with the carry pulse generated by the trailing-edge counter A_{10}, at flip-flop G_4–G_5. The signal at the output of G_4–G_5 thus has the same width as the input pulse, but is delayed by a period of time proportional to the number N. □

Counter delivers data in signed or complemented form

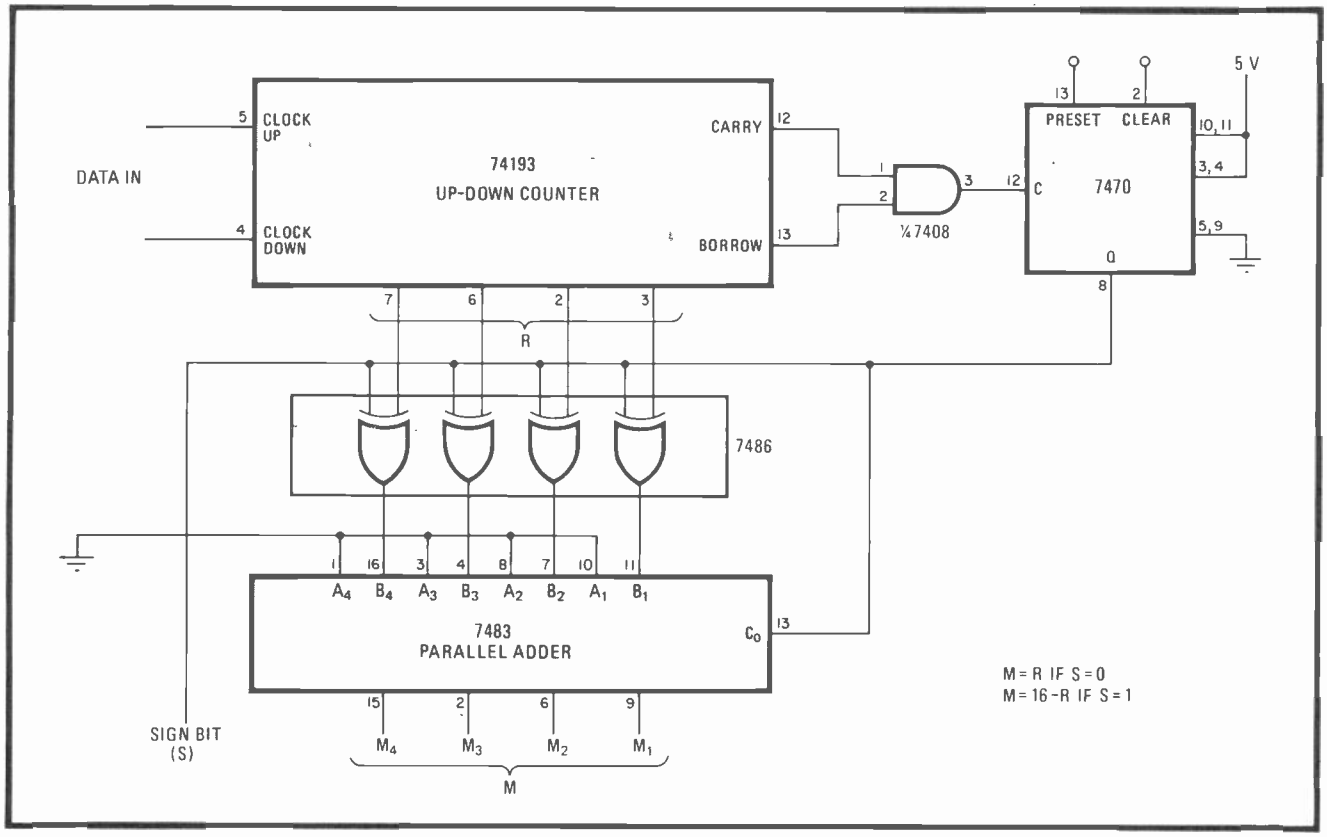
by N. Bhaskara Rao
U.V.C.E., Department of Electrical Engineering, Bangalore, India

Adding one chip to the basic digital-averaging circuit proposed by Frazier [*Electronics*, Nov. 9, 1978, p. 114] forms a data counter whose outputs express a negative number not only by its magnitude and sign, but by its 2's complement as well. Expressing numbers in the latter form enhances the circuit's usefulness by allowing direct interfacing with computer circuits.

The circuit shown works differently from Frazier's, which generates a sign bit and reverses the direction of the count when the counter is about to move down through zero. Instead, the 74193 is allowed to go below zero, where its R output becomes 15 and the state of its borrow output changes, thereby clocking the 7470 flip-flop. The 7470's Q output, which is the sign bit, S, then moves high.

The sign bit and the R bits are applied to the 7483 4-bit full adder (not part of the original circuit) through the 7486 exclusive-OR gates. The 7483 and 7486 together form an add-or-subtract unit. As a result, the output of the adder, M, will be equal to R if the 74193 indicates it holds a positive count (S = 0), and will be equal to 16 − R if the 74193 has gone negative (S = 1).

If S = 0, the R bits, as seen at the output of the 74193, will represent the binary equivalent of the number. Any negative number will be represented by its 2's complement value and an enabled borrow bit. □



Number forms. Availability of any number in both binary equivalent or magnitude-sign forms enhance circuit's interfacing capability. Data generated by 74193, expressed as binary number (R bits), is converted into magnitude-sign form by add-or-subtract unit 7483–7486. R represents the 2's complement of any negative number when counter steps down through zero.

C-MOS oscillator has 50% duty cycle

by Bill Olschewski
Burr-Brown Research Corp. Tucson, Ariz.

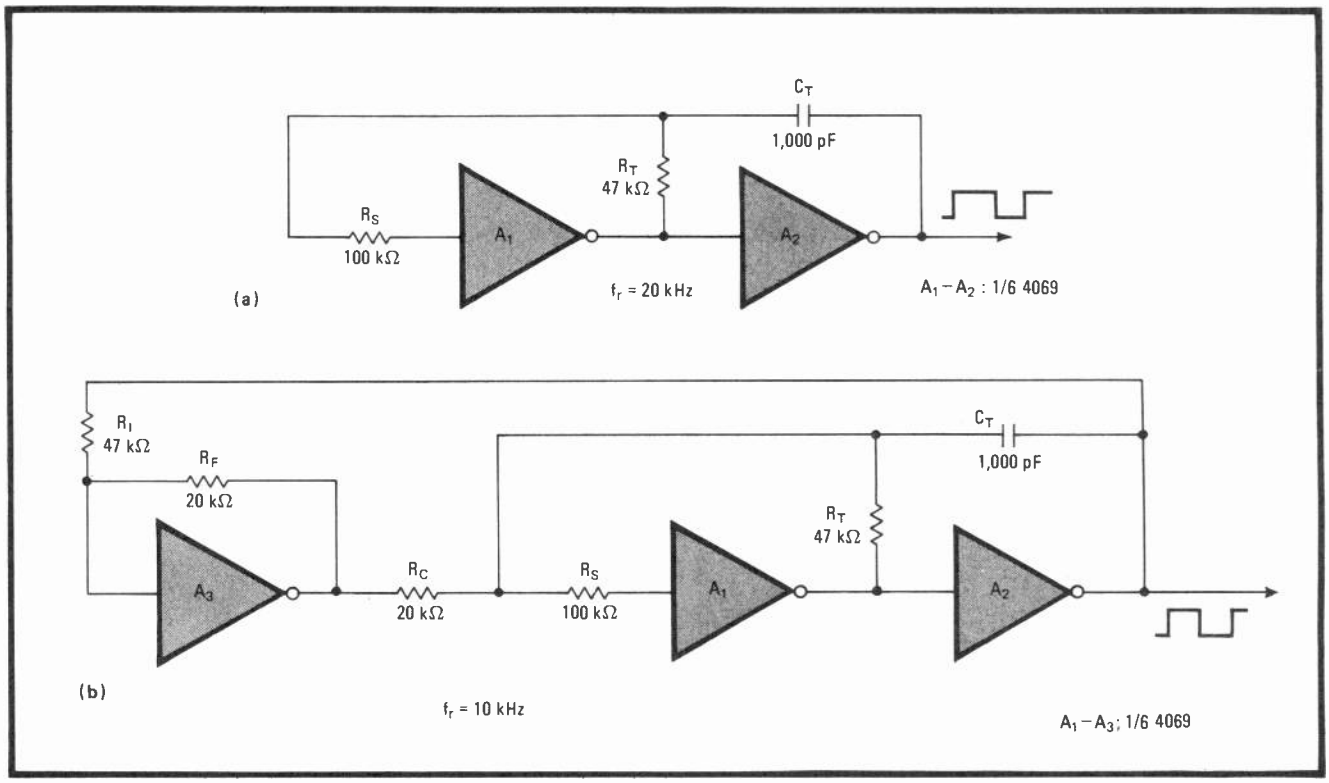
Astable multivibrators built with complementary-metal-oxide-semiconductor gates suffer one major drawback—their duty cycle may vary from 25% to 75% because of the variations of each gate's switching-threshold voltage (V_{TH}). Variations in the V_{TH} can be canceled and the desired square-wave output therefore attained by adding a C-MOS inverter and three resistors to the basic circuit. The gate-resistor combination uses negative feedback to perform the compensation.

The standard astable multivibrator is shown in (a) of the figure. Running at a frequency ($f = \frac{1}{2}R_TC_T$) that is almost independent of the individual gate used, the circuit nevertheless has an unpredictable duty cycle because of a V_{TH} that can vary by up to 40% on either side of $V_{DD}/2$, where V_{DD} is the supply voltage. If a 50% duty cycle is required, either this circuit must be followed by an edge-triggered flip-flop, or each circuit must be individually adjusted using two trimpots and a diode (see RCA application note ICAN-6267).

The circuit in (b) eliminates these drawbacks. Inverter A_3 creates a second negative-feedback path around A_1 (the signal flow through R_T constitutes the prime path). A_3 is operated at a low closed-loop gain, much like an operational amplifier working in the linear portion of its characteristic. As a result, A_3's inverted threshold voltage can be combined with the negative feedback voltage and injected into A_1. If the ratio R_F/R_I equals the ratio R_C/R_T, complete cancellation of threshold errors between A_1 and A_3 can be obtained. It is assumed that A_1 and A_3 are contained in the same package along with A_2 and that their V_{TH}s are essentially equal.

Since A_3's gain must be set so that its output will not saturate with a $\pm 40\%$ variation of V_{TH}, resistor values must be selected so that $R_I/R_F = 2.33$. At the same time, the correct gain for A_3 is set when $R_CR_I = R_FR_T$. In these circumstances, and ignoring stray and input capacitances, the multivibrator's operating frequency will be $f = 1/R_TC_T$ and the duty cycle will be 50%.

Note that the operating frequency, in this case 20 kHz, is twice that of the standard astable circuit using the same values of C_T, R_T, and R_S because of the second feedback path. □



Right on. Standard astable multivibrator using C-MOS gates (a) has unpredictable duty cycle because of variable switching-threshold voltages. Adding inverter and three resistors (b) creates second negative feedback path around A_1, forcing A_1 and A_2's switching point to half the supply voltage, so that 50% duty cycle is attained and square waves are produced.

Epitaxial phototransistor with feedback has fast response

by Vernon P. O'Neil
Motorola Inc., Discrete Semiconductor Division, Phoenix, Ariz.

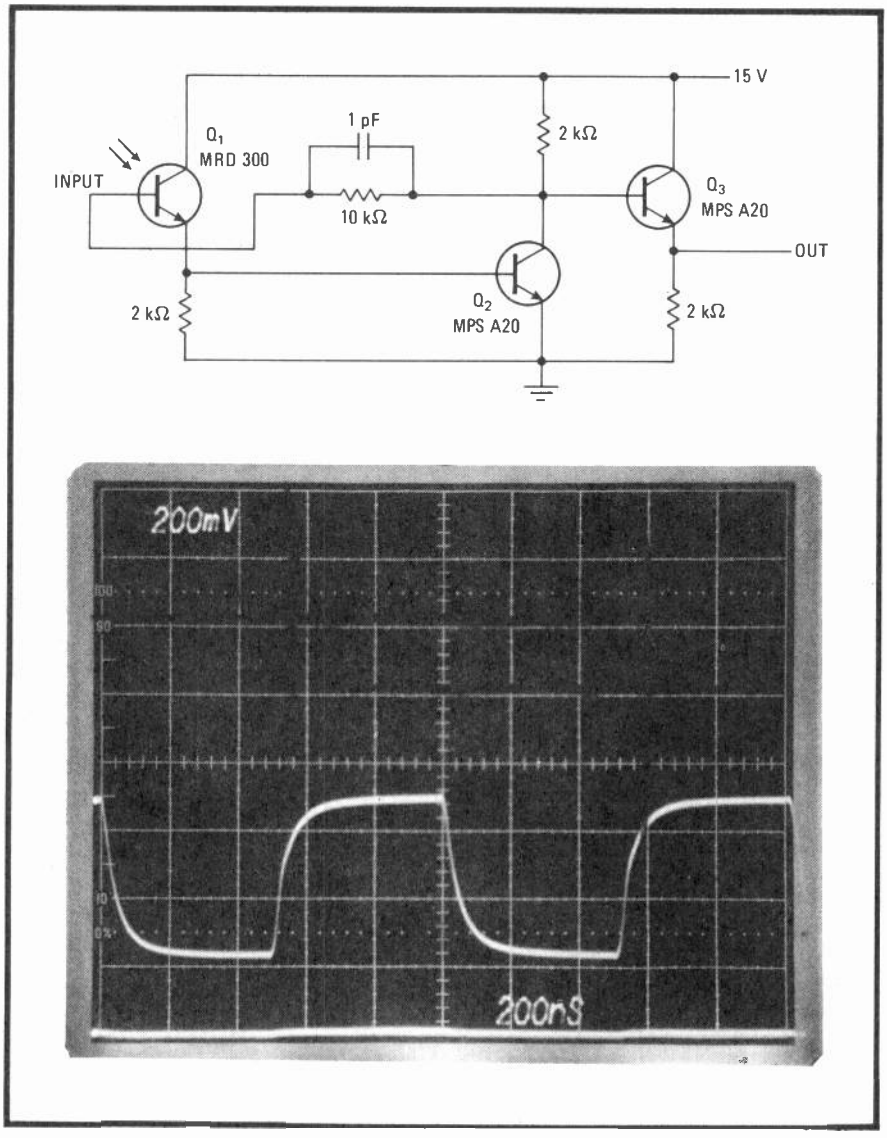
A high-gain negative-feedback loop will reduce the response time of an epitaxial phototransistor to 100 nanoseconds—a significant improvement over several schemes previously suggested.[1,2,3] Because of its construction, the epitaxial device all but eliminates the diffusion of carriers into its depletion region from the bulk collector region, which slows a conventional non-epitaxial phototransistor's operating speed. And added feedback reduces the input-signal swing across the collector-base junction to 1% of what it is normally, further reducing the input-capacitance charge and discharge times.

The MRD 300 phototransistor shown in the circuit has a typical rise time of 2.5 microseconds and a fall time of 4 μs if operated in the conventional emitter-follower configuration. In this modified circuit Q_2 serves as the feedback amplifier that keeps the base of the phototransistor at an almost constant voltage for changes in input-signal level. Thus the effective input capacitance that must be charged and discharged is reduced. Q_3 serves as a buffer. Note that using feedback that is negative enables the switching times to be maximally reduced without fear of creating instability (that is, oscillations can be generated with circuits using positive feedback).

With this circuit, both the rise time and the fall time of the phototransistor are reduced to 100 ns. The output voltage is equal to the product of feedback resistance (10 kilohms) and the collector-base photocurrent. The photograph shows a typical output waveform.

As for the phototransistor itself, it can be hard to determine from data sheets if one is epitaxial or not. The best way to find out is to consult the manufacturer. □

References
1. "Why not a cascode optocoupler?", Electronics, March 2, 1978, p. 132.
2. "Why not a cascode optocoupler? Here's why not", Electronics, April 27, 1978, p. 154.
3. "Bootstrapping a phototransistor improves its pulse response", Electronics, Aug. 17, 1978, p. 105.



Speedy. Collector-to-base capacitance of phototransistor Q_1 is reduced by employing epitaxial device (MRD 300) and high-gain negative feedback (Q_2), so that operating speed can be increased. Emitter-follower Q_3 provides low-impedance output. Photograph shows typical output response.

Hybrid servo system minimizes hunting

by C. V. Rajaraman
ISRO, Trivandrum, India

Although the shunt comparator circuit of Vojnovic[1] is simple and tends to reduce the overshoot and hunting problems inherent in a high-speed digital servo system, difficulties may arise when the servomechanism is continually called upon to follow small changes in position. Digital subtraction circuits, on the other hand, will increase system stability but are more expensive and very complex. But the two most popular techniques for synthesizing the control circuit—the no-shunt comparator method and the aforementioned subtractor method—can be combined to form a hybrid system that is more accurate than the first and less complex and costly than the second.

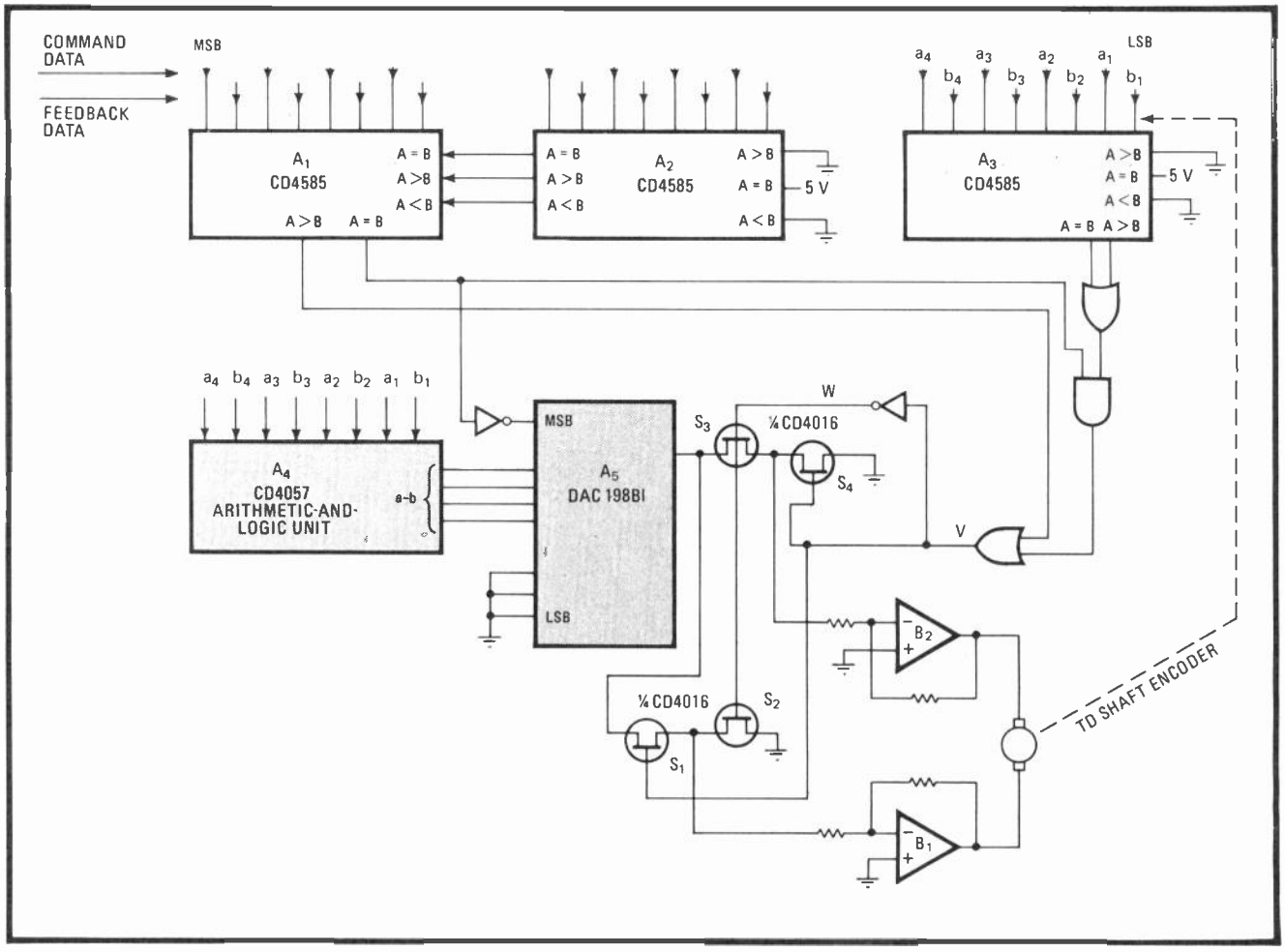
As shown in the figure, A_1 and A_2 compare lines 5–12 (the coarse bits) of a 12-bit command input with their feedback-data counterparts, which are derived from the motor position by a shaft encoder. Comparing the coarse bits in this manner enables the system to converge quickly on the desired position.

At the same time, the low-order (fine) bits of the command word are compared by A_3, and A_4 is programmed to find a~b, the difference between the two 4-bit binary words. The a~b result is then transformed into an equivalent analog signal by the digital-to-analog converter, A_5. Using the d-a converter allows a precise voltage to be applied to the motor, instead of the constant-magnitude (logic 1) signal that a comparator-type circuit would generate whenever there was an a~b offset of any value. Thus the motor has little tendency to overshoot its intended mark.

As for transferring the voltage from the converter to the motor, V moves high either when the coarse-bit comparison yields A = B and the state between the fine bits are such that A = B or A > B, or when just the coarse-bit comparison yields A > B.

Under these conditions, S_1 and S_4 turn on, and operational amplifier B_1 moves high to drive the motor. Under any other bit-comparison condition, W moves high and turns on S_2, S_3, and B_2, to drive the motor in the other direction. □

References
1. B. Vojnovic, "Shunt comparator stabilizes high-speed digital servo," Electronics, March 16, 1978, p. 149.



End of search. Comparators and subtractor in servo position motor without oscillations. Comparison of high-order bits enables motor to converge on desired location. Fine-bit comparison with a d-a converter resolves precise feedback voltages to minimize overshooting.

Peak detector recovers narrow pulses accurately

by Jerome Leiner
Loral Electronic Systems, Yonkers, N. Y.

This peak detector can accurately process input data pulses as narrow as 50 nanoseconds and as high as 3 volts. The recovered voltage is always within 1% of the input signal's true value.

In the circuit shown, emitter-coupled logic generates a −0.2- to −3-volt signal for input into amplifier A_1. Assuming a pulse with a 50-nanosecond width and a rise and fall time of 5 ns, that leaves storage capacitor C_4 only 45 ns in which to charge. The LH0024 op amp used for A_1 has wide bandwidth and a high slew rate to accommodate the fast charging required.

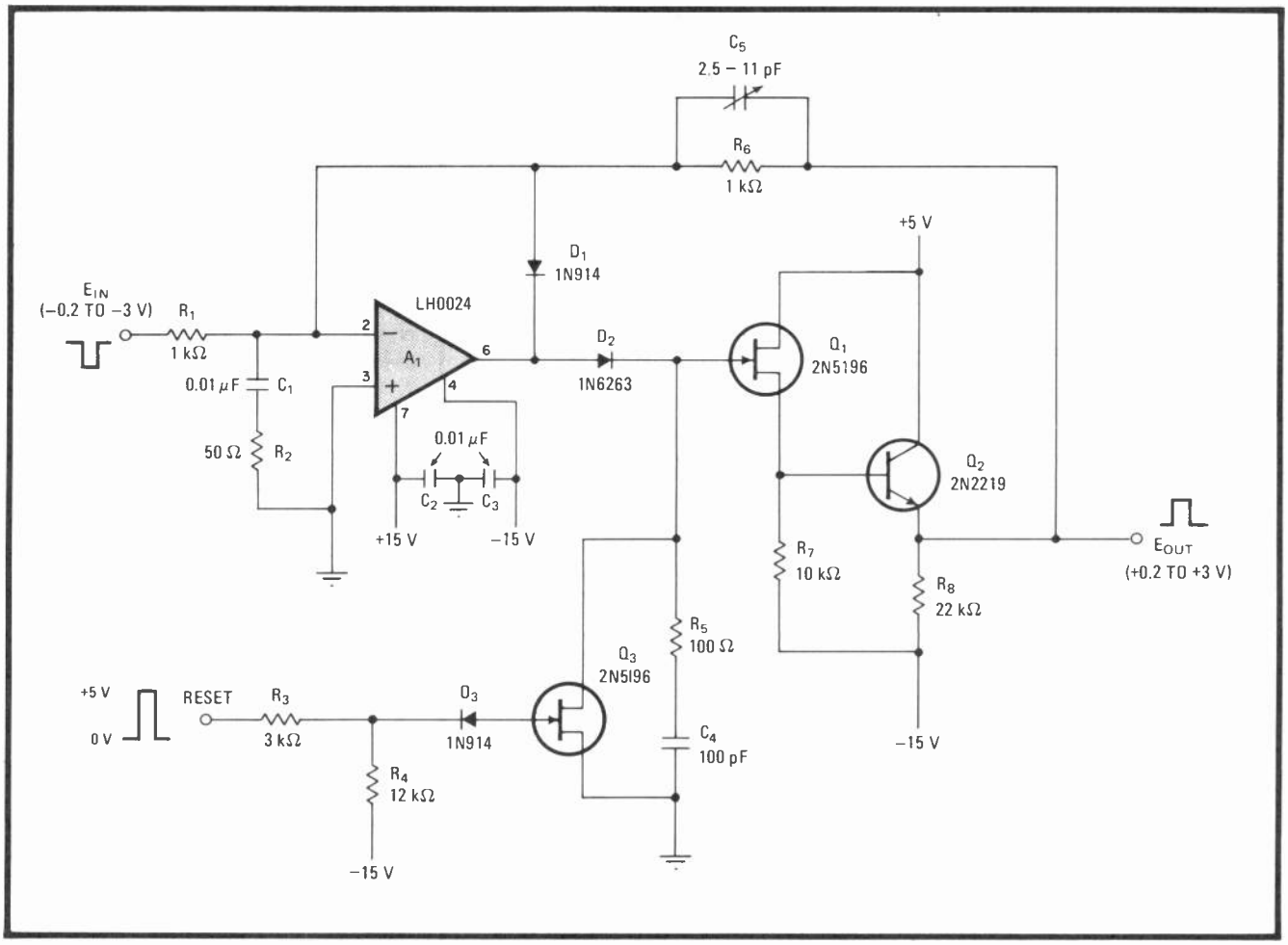
Q_1 acts as a buffer to prevent C_4 from discharging through R_7 between system reset pulses. The voltage at Q_1 appears at Q_2 and is fed back to A_1, to be compared with E_{in}. When E_{out} reaches E_{in}, D_2 becomes back-biased and the stored charge is held until C_4 is intentionally discharged by the reset signal. D_2 remains back-biased during discharge.

A_1 is normally used as an amplifer, and so it will be driven into negative saturation whenever the input signal drops below the output level. D_1 prevents this by clamping the amplifier output.

C_1 and R_2 provide A_1 with input- and feedback-signal stabilization. C_5 compensates for A_1's input capacitance. Note that if C_1R_2 were placed at the output of A_1, a larger charging current would be required for a given input signal. Because this current is usually limited, A_1's effective slew rate would be reduced.

The peak detector is optimized by shorting D_2 and then adjusting C_1, R_2, and C_5 for minimum overshoot and ringing on a series of fast data pulses. □

Fast and precise. Using one op amp, one transistor, and two field-effect transistors, peak detector recovers data pulses having amplitudes of up to 3 volts and widths as narrow as 50 nanoseconds. Output voltage is within 1% of the input data's true value under all signal conditions.



Optoisolator initializes signal-averaging circuit

by J. Ross Macdonald, *Department of Physics and Astronomy, University of North Carolina, Chapel Hill*

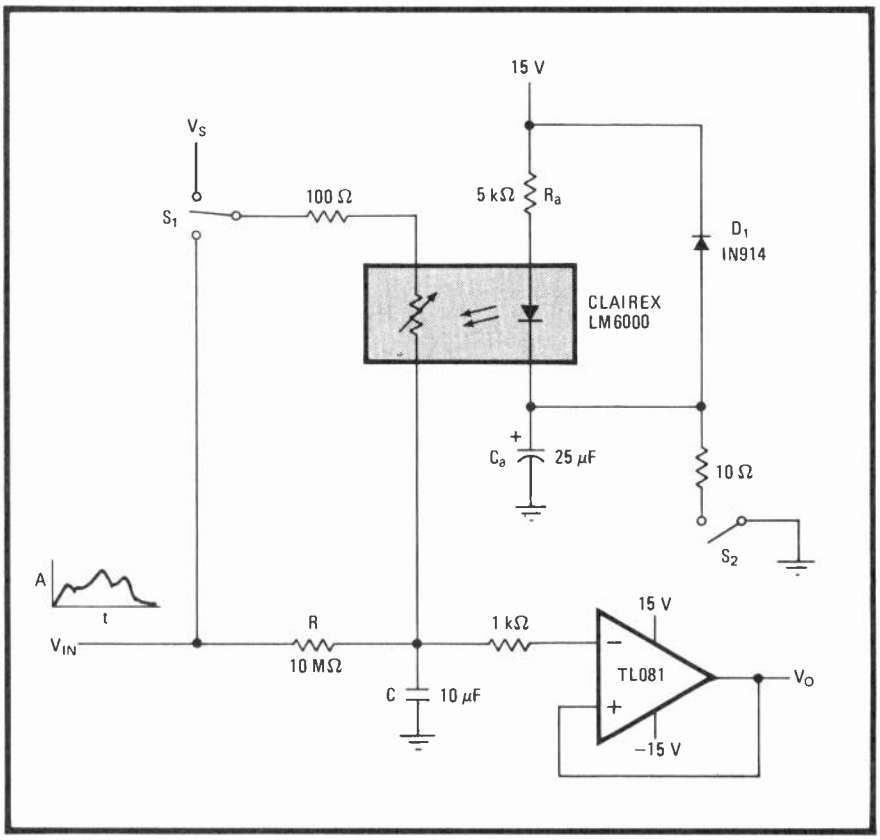
Long-term averaging circuits require an initializing voltage on their capacitive storage element in order to become almost immediately operational on power up. Here, an optoisolator is used to quickly charge the capacitor with a voltage derived either from the input signal itself or from any dc voltage, the two sources most widely used. The optoisolator circuit is superior to an initializer that uses a relay, which, besides having the disadvantage of being electromechanical, also draws power continuously.

In a circuit that averages a signal over a long period (see figure), the resistor-capacitor (RC) time constant may be on the order of a minute or more. Thus, the output of the averager (V_o) during the time t = 0 − 1 minute is considered to be the circuit's transient response to the input signal, where t is measured from the time that power is applied to the circuit. In most cases, especially when the circuit is part of a more complex system, it is not feasible to wait that long before the RC network starts generating a true average value.

The difficulty may be circumvented by using an optoisolator and a switch, S_1, to charge C on power up. Assume it is desired to charge C from a dc voltage, V_s. When power is applied, C_a, which may be 25 microfarads or more, is charged through R_a. Consequently, as current flows through the photodiode, the value of the photoresistance element in the LM 6000 optoisolator is reduced from more than 10^9 ohms to about 1 kilohm. Thus, in a few tens of milliseconds, C charges to V_s through the element, if S_1 is placed in the V_s position. As C_a becomes fully charged, the resistance of the element quickly increases to at least 10^9 ohms, and the circuit is ready to operate in its intended averaging mode

When power is removed, C_a discharges through D_1, so that the on-off power cycle can be repeated fairly rapidly. C also discharges slowly through R. This action is of little consequence in circuit operation on a subsequent power up. Note that S_2, a momentary-contact switch, allows the resetting process to be repeated at any time, even while the circuit is active.

To initialize C from the input signal, it is only necessary to connect S_1 to V_{in} prior to power up (or at any time if S_2 is utilized). Otherwise the initializing operation is the same as before. □



Speedy average. Optoisolator enables long-term averager to operate almost immediately after power up by presenting an initializing voltage to circuit's sampling capacitor, C. Charge is introduced through isolator's low-resistance photoelement. Either a dc voltage or the input signal can be used as the initializing source.

Five-state LED display monitors paging system

by D. F. Fleshren
Springfield, Va.

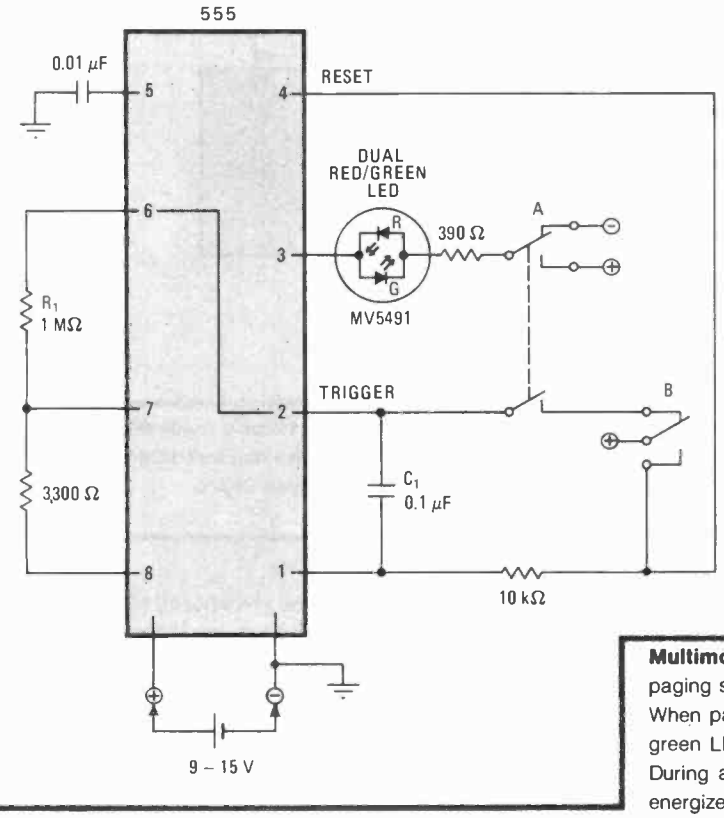
This paging station circuit uses a single red- or green-light-emitting diode to alert the user to any of five distinct paging conditions. It is a simple, extremely easy-to-build monitor designed to be part of a large paging system. Two relays and a 555 timer send a signal to the LED (a Monsanto MV5491 or Xciton XC5491) to produce the following signals:

- Off (no power) indicates that paging has been cut off to that station or the region in which it is located.
- Steady green signifies that the station is operational, but is not being paged.
- Steady red is the individual station's paging signal.
- Flashing green tells the user that all stations in the system are being alerted.
- Flashing red signals an emergency situation to all monitoring stations.

An external signal triggering relay A controls the color of the LED, changing it from its green (idle) condition to red. Relay B is excited when all stations are to be called. This second relay puts the 555 timer in the astable mode, changing the LED's usual dc state to an on-off oscillation of about 7.5 hertz at a duty cycle of 50%. The frequency of oscillation can be adjusted by suitably selecting R_1 and C_1. In the emergency red flashing mode, both relays must be tripped by external signals.

This circuit can readily be adapted to signal a single panel-mounted lamp. To derive the five operating modes, the relay contacts must be replaced by the contacts on a suitably wired rotary switch.

Supply voltage for the 555 may vary from 9 to 15 volts; with a 12-V supply, current drain is about 40 milliamperes. □



OPERATING MODES FOR 5-STATE MONITOR

Condition	Typical application	Relays operated	Lamp display
1	power off	none	off
2	power on, circuit idle	none	steady green
3	paging	"A" only	steady red
4	all zone paging	"B" only	flashing green
5	emergency announcement	A and B	flashing red

Multimode monitor. Module indicates the state of a multizone paging system using red/green LED, 555 timer, and relay contacts. When pager is off, both LEDs are extinguished. When pager is idle, green LED turns full on. If monitor is paged, red LED turns full on. During all-zone paging and emergency announcements, relays are energized for timer so that red or green LED flashes.

Rate multiplier controls noninteger frequency divider

by Michael F. Black
Texas Instruments Inc., Dallas, Texas

Frequency dividers capable of dividing by integer and noninteger values can be built inexpensively from very few parts now that synchronous binary rate multipliers are available on single chips. To increase the resolution of the noninteger value, the rate multipliers are simply cascaded.

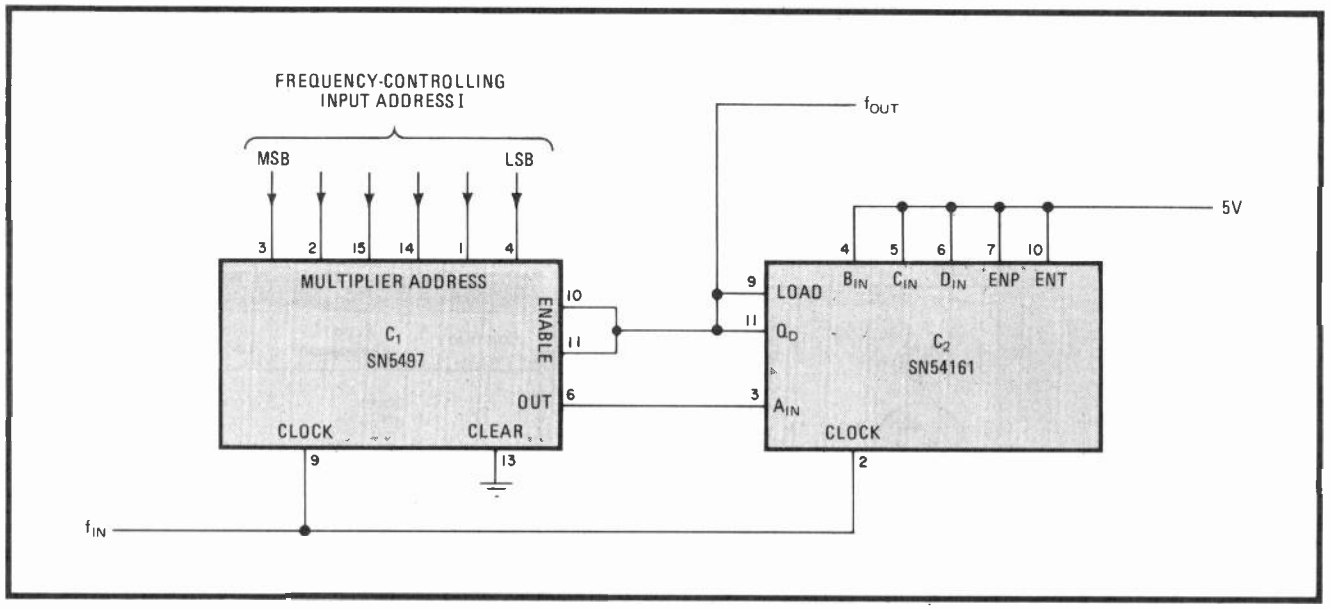
The ratio at which division is performed is set in an indirect manner by the 5497 rate multiplier. This number lies between two values preset in the 54161 synchronous counter, n and n − 1. The circuit divides the input frequency by a ratio directly proportional to the time the counter spends in the n mode versus the time it spends in the n − 1 mode.

The number of input pulses rate multiplier C_1 passes to synchronous counter C_2 is proportional to input address I. In this instance the counter is preloaded at either 14 or 15 by inputs A_{in} through D_{in}. C_1's output (pin 6) is connected to the counter's input A_{in}. Address I consequently controls the percentage of time the counter spends at divide values n = 2 and n = 3.

The rate multiplier's pulse-train output frequency is $f = f_{in}(I/M)$, where M is the size of the rate multiplier (in this case $2^6 = 64$). This particular circuit configuration results in $f_{out} = M(f_{in})/(nM - I)$. The actual divide ratio is $n' = n - (I/M)$.

The value of M determines the size of the available frequency step. The circuit as shown has been used to set f_{out} from 4 to 6 megahertz in steps of about 30 kilohertz; adding one more six-line rate multiplier would bring the step size down to about 400 hertz. Frequency steps in hundredths of a hertz can be easily obtained by cascading more multipliers.

This divider circuit will generate the exact number of clock pulses per second desired, but there will be some phase jitter, with $\Delta\phi = 360/n$. □



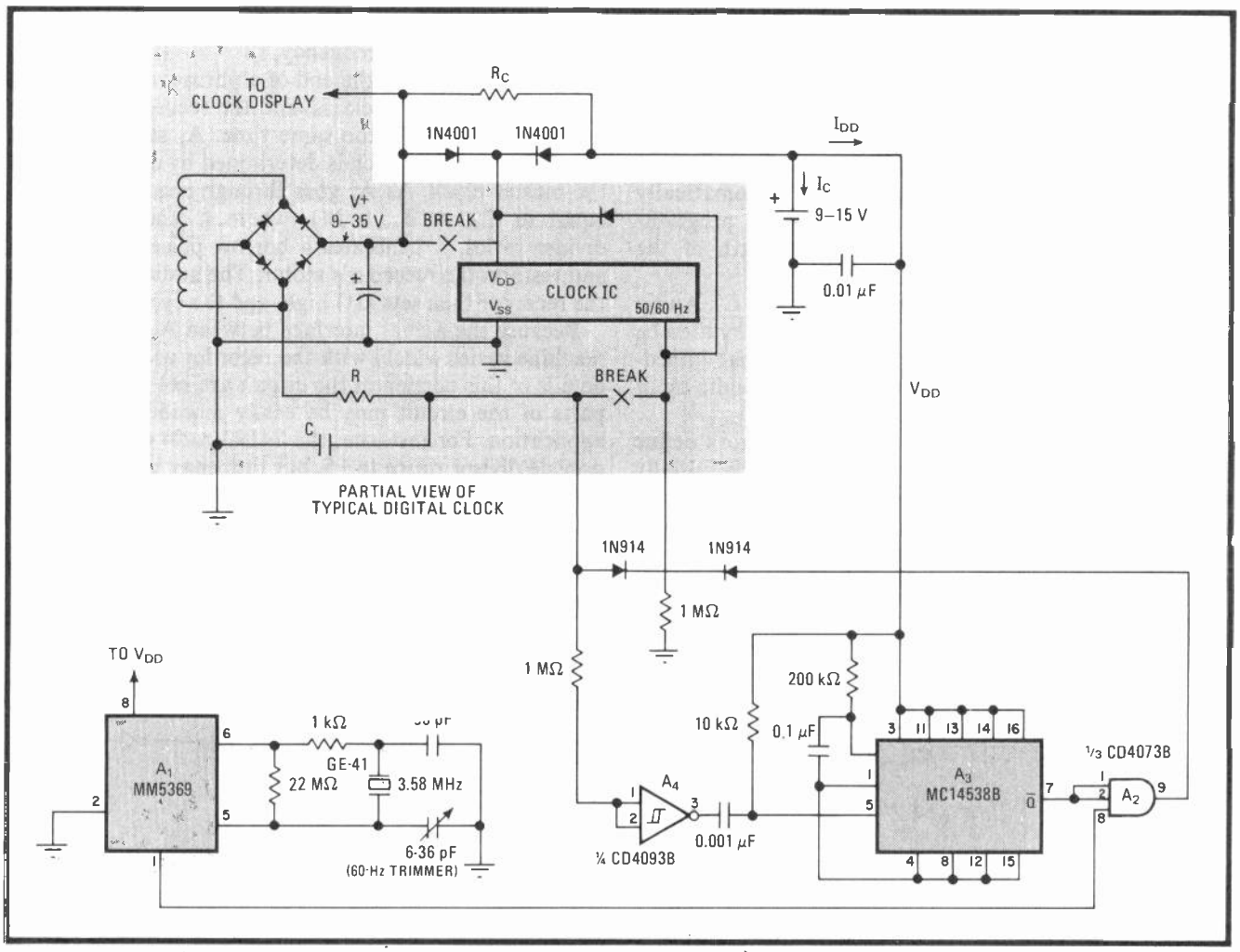
Continuous division. Synchronous frequency counter uses rate multiplier in two-chip circuit to program circuit's divide ratio at any value. Output frequency is proportional to the time spent between two preset divide values, n and n − 1. Multipliers can be cascaded for step-size resolution all the way down to hundredths of a hertz. The amount of phase jitter at the output, in degrees, equals 360/n.

Standby crystal time base backs up line-powered clock

by William D. Kraengel, Jr.
Valley Stream, N.Y.

This battery-powered, crystal-controlled time base provides accurate and glitch-free performance when it takes over as the 60-hertz frequency standard that drives a digital clock during a power outage. The cost of the unit is about $7.

More long-interval timing circuits would probably use the ac power line as a time base because of its long-term average-frequency accuracy (1 part in 10^7), were it not



Standby standard. Battery-powered, crystal-controlled time base, having sufficient accuracy for most short-term applications, takes over clock-driving duties of digital chronometer in event of ac power loss. Unit uses 3.58-MHz oscillator, which is divided down to 60 hertz.

for the transients and blackouts that occur frequently. This back-up time base takes over smoothly in such instances and has sufficient accuracy over a period of several hours to satisfy all but the most demanding applications.

The standby time base uses a low-cost crystal oscillating at 3.58 megahertz, which is generally the frequency required for the color-burst circuits in standard television receivers. The frequency produced by the crystal's programmable oscillator-divider chip, A_1, is 60 hertz. This signal is fed to one input of an AND gate, A_2, which is activated if line power is lost.

During normal operation, the battery is trickle-charged (I_c) by the clock's supply through R_c, at a rate of 0.01 C, where C is the capacity of the battery in ampere-hours. R_c is equal to $(V^+ - V_{bat})/(I_c + I_{DD})$, where I_{DD} = 2.5 milliamperes. The digital clock must be modified slightly, as shown, in order to lengthen the charge life of the battery. Thus the digital clock's display will be blanked while the battery is the power source.

Meanwhile, one-shot A_3, configured as a missing-pulse detector, is triggered by Schmitt trigger A_4 at the beginning of each cycle of the ac input.

The one-shot's pulse width is 20 milliseconds, slightly longer than the period of the 60-Hz line input. Thus, A_3 is continually retriggered, and so A_2 is disabled.

With a loss of line power, the battery takes over the supply chores. A_3 times out, and then A_2 is enabled, so that the 60-Hz signal derived by the crystal circuit drives the digital clock's timing chip. The maximum length of time between the power outage and the first clock pulse from the standby unit is 8.3 milliseconds.

Almost the reverse action occurs when the ac line power is restored. When the filter capacitor in the clock's power supply recharges enough for the line pulses to rise above the set threshold of the Schmitt trigger, the one-shot is triggered, and the AND gate is disabled. As the voltage across the filter capacitor rises further, the power source duties revert back to the digital clock's power supply. □

Controller halts playback when taped voice pauses

by N. Bhaskara Rao
U.V.C.E., Department of Electrical Engineering, Bangalore, India

Few typists can transcribe a dictated message or speech without stopping the tape recorder from time to time. The illustrated circuit stops the recorder automatically at the end of a sentence or other pause. Its programmable halt time is proportional to the length of the preceding playback segment.

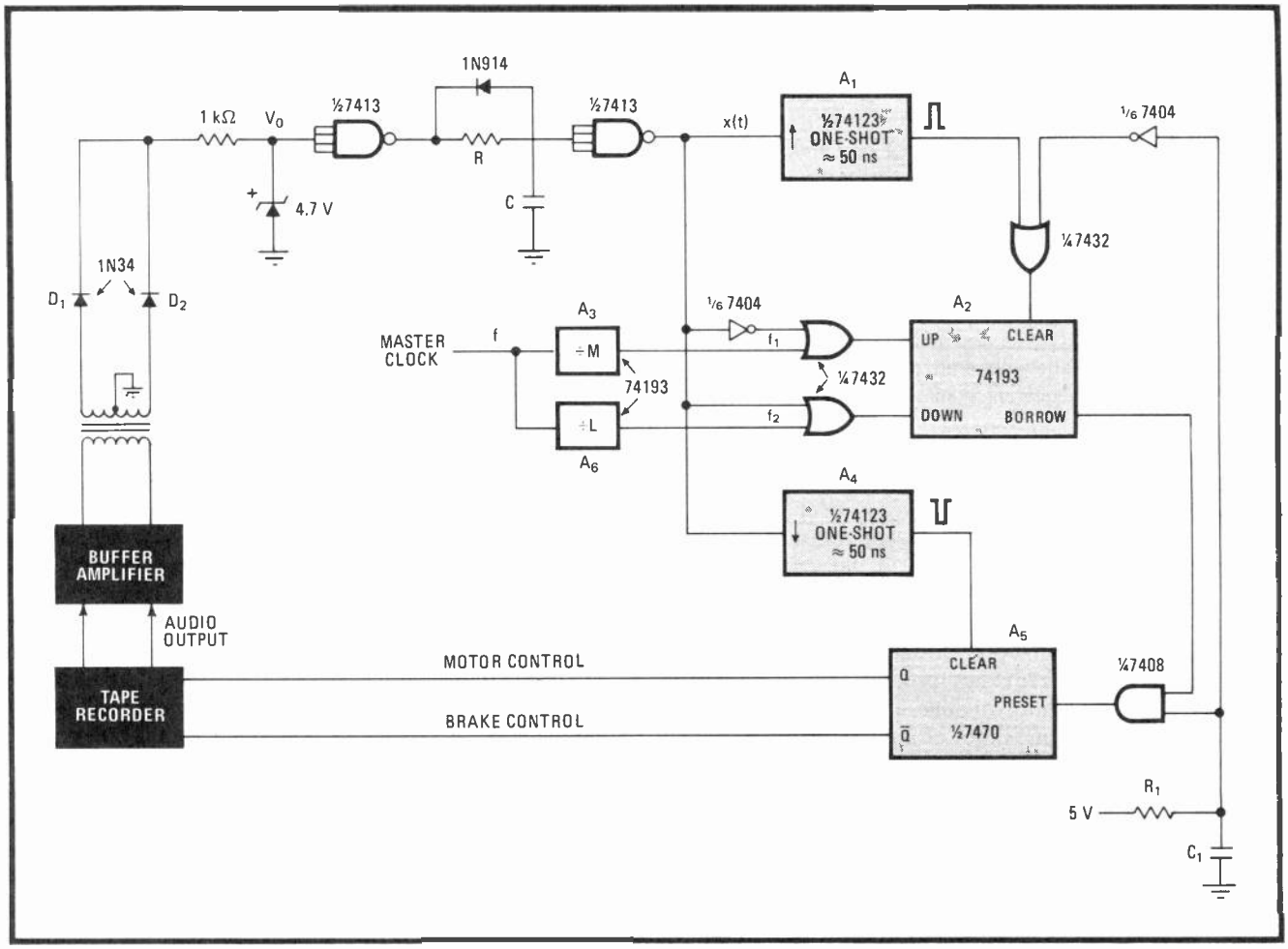
The circuit is preset on power up by R_1 and C_1. Audio signals from the output of the tape recorder may then be fed into a buffer amplifier having a low output impedance, so that a dc voltage proportional to the audio input is produced by the full-wave rectifier, D_1 and D_2.

The 7413 Schmitt triggers and an RC network define the time delay, T. The voltage at x(t), which is initially set high by the audio signal, goes low when V_o is low for a period greater than T, so that any pause in the audio signal triggers the recorder-halting circuit. The delay time selected may be varied for the particular application by adjusting one or both elements of the RC network.

As one-shot A_1 is triggered by x(t), A_2 is cleared and starts to count up. If the time during which x(t) is high is T_{on}, then the output of A_2 at the end of that period is given by $N = f_1 T_{on}$, where f_1 is derived from divider A_3 and the master clock frequency, f.

As x(t) goes low at the end of a phrase, one-shot A_4 is triggered, flip-flop A_5 clears, and the recorder's motor is braked to a halt. At the same time, A_2 starts to count down at a rate, f_2, which is determined by divider A_6 and the master clock. As A_2 goes through zero after a time equal to $T_{off} = T_{on}(L/M)$, where L and M are the divider ratios, it generates a borrow pulse that sets A_5 and restarts the recorder's motor. The audio output from the recorder then sets x(t) high, and the cycle repeats.

Because the actual interface between A_5 and the tape machine varies widely with the recorder used, the wiring details of this portion of the circuit are not shown. Other parts of the circuit may be easily modified to suit the application. For instance, the 74193 ratio counters each provide divisor ratios to 15, but they may be replaced by dividers that provide any value of L and M. □



Pausing for write time. Unit brakes tape recorder's drive after each sentence of taped message to provide transcription secretary with time to write information. Circuit uses up-down counter to derive a halt time proportional to the length of the preceding playback period.

Micropower regulator has low dropout voltage

by Kelvin Shih
General Motors Proving Ground, Milford, Mich.

Designed specifically to regulate the output of lithium batteries, which have a low terminal voltage at low temperatures, this circuit provides a stable 5.0 volts at 10 milliamperes for an input voltage as low as 5.2 v.

The low dropout voltage of the regulator (5.2 − 5.0 = 0.2 v) is attained in part by operating the circuit's output transistor in the common-emitter mode. As a result, its collector-to-emitter voltage drop is much lower than the base-to-emitter drop of transistors operated as emitter followers in standard regulators. And, because it uses a low-power operational amplifier operating from a single supply, and a low-current, low-voltage zener diode for the voltage reference, the regulator's idle current is only 250 microamperes.

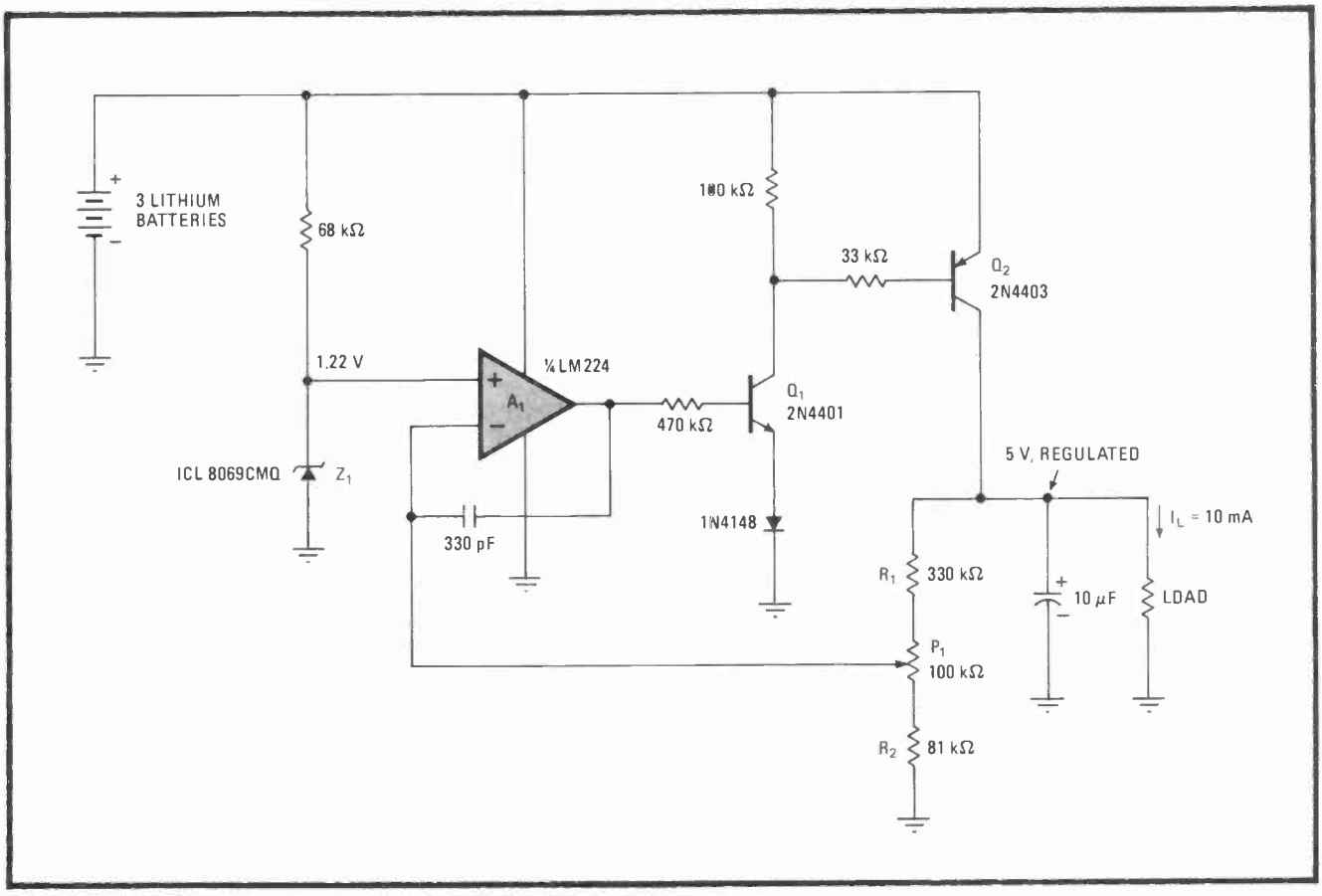
Three lithium batteries drive the regulator shown in the figure. Their terminal voltage is usually 3 v per cell at room temperature, but it will drop to 2 v at −40°C.

Z_1 provides a low-voltage reference (1.22 v) to the noninverting input of the LM224 op amp, A_1. The Intersil ICL 8069CMQ zener has been selected because it requires only 50 μA of bias current and has a temperature coefficient of better than 50 parts per million/°C.

The 1.22-v reference is compared to the output voltage from a divider network (R_1,R_2, P_1), which is used to trim the output voltage to the desired value. Any voltage difference appearing at the output of A_1 drives transistor Q_1, and thus determines the drive current to Q_2. As a result, Q_2 conducts more heavily if the output voltage is low, or limits the application of battery voltage to the load if the output voltage is high.

There will be no observable change of output voltage for an input voltage variation between 5.2 and 10 v, over the temperature range of −40°C to +70°C. □

Dropout minimum. Voltage regulator for lithium batteries maintains 5-volt output for a minimum input voltage of 5.2 V. Output voltage is constant over the temperature range −40°C to +70°C. Using a low-power op amp operating from a single-ended supply, and a low-current zener, the circuit holds the idle current to 250 μA, well below the 2 to 10 mA required by standard regulators.



Missing-pulse detector handles variable frequencies

by Joe Lyle and Jerry Titsworth
Bendix Corp., Aircraft Brake and Strut Division, South Bend, Ind.

Virtually all missing-pulse detectors require an input signal of fixed frequency in order to operate satisfactorily. They malfunction when the input frequency varies because their circuits employ detection networks that have a fixed time constant. Through the implementation of inexpensive voltage-to-frequency and frequency-to-voltage converters to derive an average, or reference, frequency that tracks the input signal, this circuit can pinpoint missing pulses without being affected by input frequency variations.

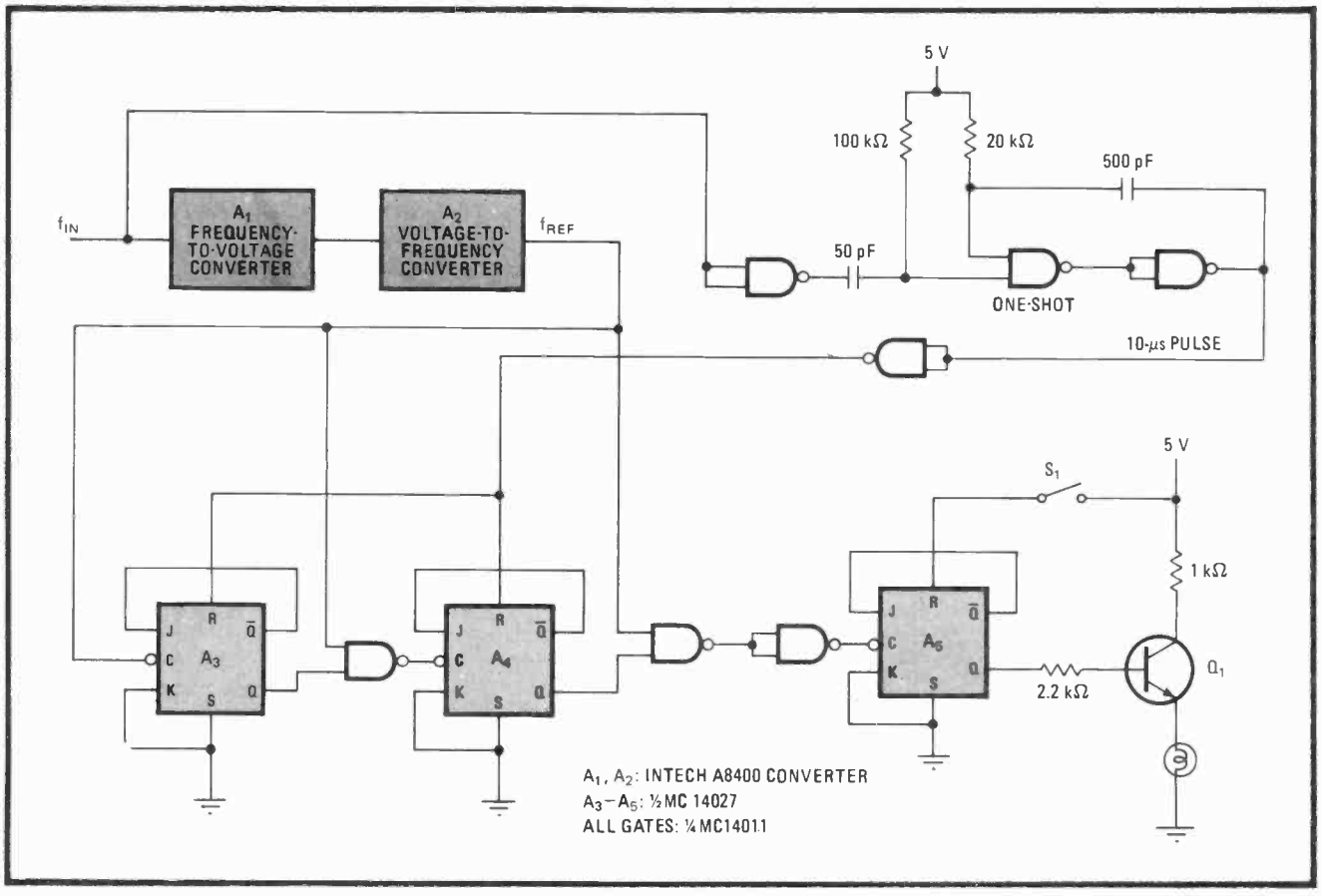
As shown in the figure, A_1 and A_2 establish the reference frequency, f_{ref}, using input frequency f_{in}. Missing pulses do not change the reference because of the integrating capacitors within the converters. Meanwhile, the three NAND gates comprising the one-shot produce pulses of 10 microseconds in duration, with a frequency determined by the input signal.

The chip labeled A_4 is clocked by f_{ref} and A_3 through a NAND gate. As long as the input train is continuous, the Q output of A_4 is low. If a missing pulse is detected, however, the one-shot will not generate a pulse to the reset pin of A_3, and the Q output of A_3 (which is also clocked by f_{ref}) will go high to clock A_4. A_4 and f_{ref} will then switch A_5's Q output to high.

This turns on transistor Q_1 and the pilot lamp glows. Switch S_1 is used to reset the circuit after a missing pulse has been detected. Note that circuit operation remains independent of the input frequency, since the arrival of f_{ref} and the 10-μs pulse at A_3 is synchronized to f_{in}.

The circuit should be calibrated by setting A_1 for an output voltage of 10 when a 10-kilohertz input signal is applied. Similarly, A_2 should be set to generate a 10-kHz signal for a 10-V input. □

Synchronous. The circuit detects the missing pulse independently of the pulse train frequency. Voltage-to-frequency and frequency-to-voltage converters derive a reference frequency whose average remains the same for small anomalies occurring in the pulse train: converters' integrating capacitors hold f_{ref} steady despite missing pulses. The reference in this way serves as a synchronous clock.



Charge pump cuts compandor's attack time

by Devlin M. Gualtieri
Allied Chemical Corp., Morristown, N. J.

Integrated-circuit compandors such as the Signetics NE570 could be more effective in high-fidelity noise-reduction schemes if it were not for one built-in shortcoming: their slow attack time permits large input signals to overdrive the device's compressor and thereby create distortion. But by adding a quad operational amplifier, a diode, and a few resistors, the compandor's attack-to-decay ratio (which is internally set at 1:5) can be dynamically controlled. Specifically, the attack time can be decreased for a given decay period. This concept can be extended to any charge-storage circuit, such as a sample-and-hold module, to speed voltage-level acquisition for a given set of circuit parameters.

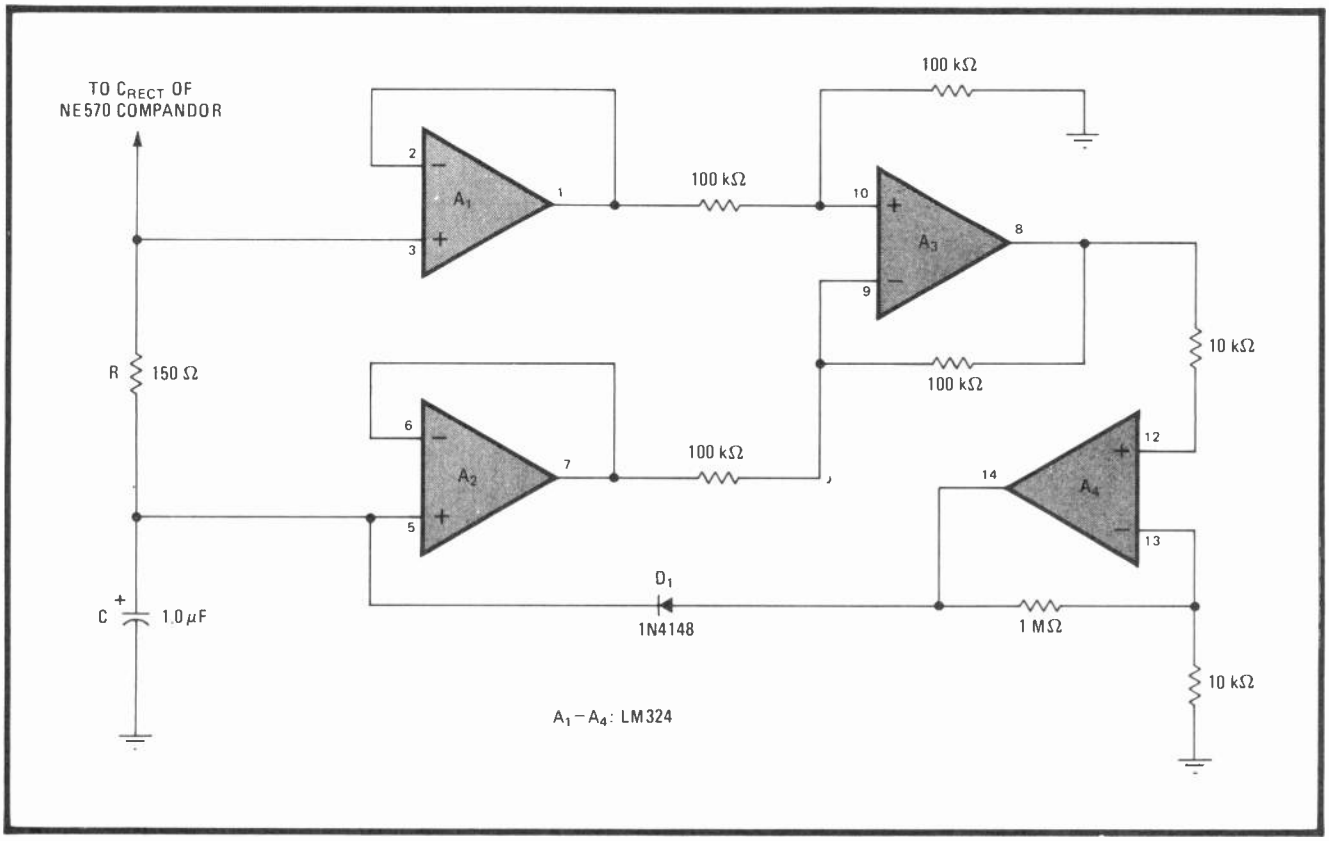
The NE570 contains a full-wave rectifier, a variable-gain stage, and other peripheral circuits. The rectifier converts an audio-input signal into a pulsating direct current, which is averaged by an external filter capacitor, C, connected to the compandor's C_{RECT} terminal. The average value of the signal determines the gain of the variable-gain stage.

The compandor's attack and decay times are inversely proportional to the value of the filter capacitor. Thus attack time could be reduced simply by substituting a smaller capacitor for C. But the circuit's purpose is to reduce attack time without using a smaller C, because the third-order harmonic distortion generated when the compandor processes low- and medium-amplitude signals increases as the value of C decreases. The effective capacitance of C during charging is reduced by using this circuit as a pump to charge C more quickly for large input signals, thereby shortening attack time without appreciably reducing the average capacitance of C.

The averaging capacitor is connected to the compandor's rectifier through a 150-ohm resistor, R. At low signal levels, the LM324 quad op amp is not active, so that R contributes only 0.2% additional distortion to what would normally be expected with C alone.

When the rectifier processes a large signal, the relatively large voltage drop across R activates the circuit. Differential amplifier A_1–A_3 generates a large voltage at the input to A_4. This causes A_4 to charge C through D_1 at its short-circuit value of 40 milliamperes. C is effectively charged at 40 volts per millisecond, which corresponds to an attack time of less than 0.1 ms.

The threshold of the enhanced attack rate, which is set by the quiescent 1.3-v drop across C and the 0.7-v drop across D_1, is approximately 0.1 v root mean square (−20 dBm) with respect to the rectifier input. □



Dynamic. Circuit for decreasing NE570's attack time for large signals uses a quad operational amplifier for quick charging of compandor's averaging capacitor, C, in this way reducing its effective value. The fundamental waveform distortion from the compandor output is substantially reduced as a result, but third-harmonic distortion for low- and medium-amplitude signals is not substantially increased.

Annunciator control uses only passive components

by John A. Haase
Fort Collins, Colo.

Combining relays with other passive components, this circuit provides time delays of anywhere from milliseconds to minutes without the need for the polarizing potentials normally required by monostable multivibrators. Such an electromechanical arrangement is ideally suited to the implementation of a practical call controller, or annunciator.

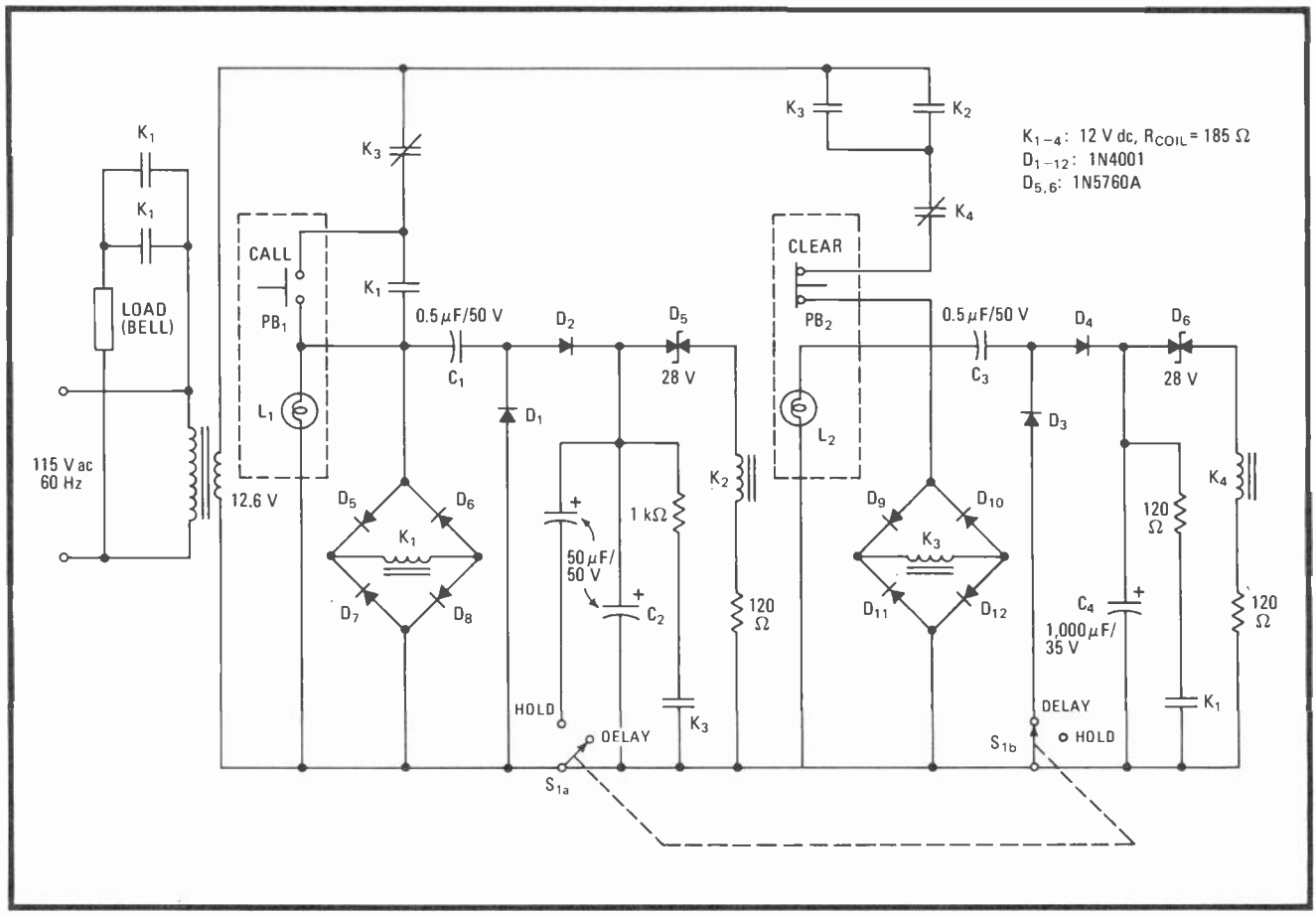
Delays are produced by first generating a staircase voltage. Pushing button PB_1 momentarily latches relay K_1 and energizes its bell circuit. The bridge circuit used with each relay permits the use of an inexpensive dc relay.

Call-indicator lamp L_1 then lights, and supply voltage is applied to C_1, C_2, D_1, and D_2, which make up the staircase generator. The step interval of the rising output voltage, V, at the junction of D_2 and C_2 becomes $\Delta V_o = C_1E(10^3)/C_2$ millivolts per cycle, where $E = 12.6(1.414) = 18$ volts. Note that the diodes are considered passive elements in this application, as their characteristic curve, per se, is not utilized in the generation of the staircase waveform.

Circuit constants are selected so that D_5, which serves as a comparator, breaks down after 155 cycles (2 seconds), when output voltage V reaches 28 v. Relay K_2 is then energized, enabling K_3 to close and lamp L_2 to light, because the alternating voltage is applied to a second delay circuit through one of the normally open contacts of K_2. At the same time, voltage to relay K_1 is removed, since the normally closed relay contact of K_3 (in K_1's energizing path) opens. Simultaneously, C_2 is discharged by K_3's closed relay contact (in series with the 1-kilohm resistor).

Relay K_3 remains closed for 80 seconds to prevent repeated (and most times annoying) calls. At that time, the output voltage across C_4, generated by the second staircase waveform, steps to 28, whereupon D_6 breaks down and relay K_4 is energized. Relay K_3 then opens and the path of relay K_1 is reactivated to accommodate call requests, while C_4 discharges.

Call requests may be extended to 4 seconds by placing switch S_1 in the hold position. In this mode, relay K_4 does not come into play, so the user must wait an infinite inhibiting time before initiating a second call request. Under this condition, push button PB_2 must be depressed to clear the circuit so that it can respond to calls. □



Charged delay. Electromechanical relays and other passive components form charge pump that generates a time-dependent staircase voltage, V, for call controller. By suitably selecting diodes D_5 and D_6 so that their breakdown voltages conform to some preset value of V, the circuit provides delay. Depressing PB_1 rings bell for 2 seconds. inhibits circuit for 80 seconds to prevent quick second requests.

LEDs track signal level in visual data monitor

by Michael O. Paiva
Teledyne Semiconductor, Mountain View, Calif.

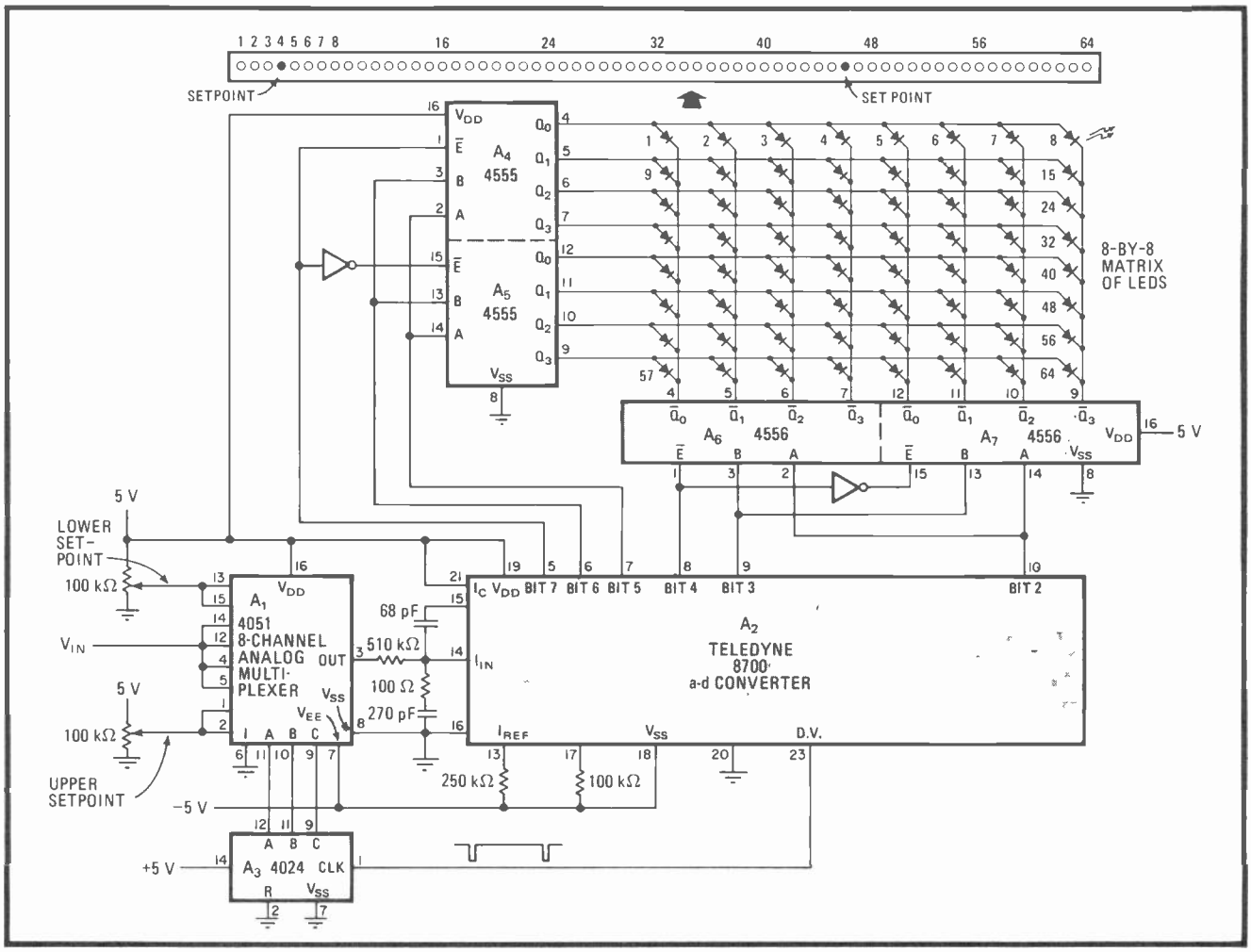
In this circuit, a matrix of light-emitting diodes is combined with an analog-to-digital converter and multiplexing logic to form a dual-setpoint meter. The LEDs are used to track changes in the input data and display the setpoints. The unit may be considered a variation of the analog panel meter; it will find many uses in industrial control applications where it is necessary to observe quick changes while determining whether data is within a preset range. By adding a dual comparator to the circuit, an alarm can be sounded when the input level goes outside the range.

The signal to be tracked, V_{in}, and the upper and lower setpoint voltages are applied to an eight-channel multiplexer, A_1. The a-d converter, A_2, samples channel 1 first. After the conversion, pin 23 of A_2 goes high and advances the binary counter, A_3. A_3 then addresses the second channel of the multiplexer, and so on, until each channel is scanned in sequence.

Bits 2 through 8 of the a-d converter, representing the binary equivalent of the voltage sampled, drive A_4–A_7, which are wired as two one-of-eight decoders. Thus each voltage is converted into a control signal that drives one diode in the eight-by-eight-diode matrix.

The setpoint voltages are sampled twice during each scan cycle (each is connected to two input channels), while the input signal, V_{in}, is connected to four channels and so is scanned four times per cycle. Thus the brightness of the LED corresponding to V_{in} is twice that of the setpoint LEDs, making it easy to differentiate between the three signals.

The circuit's worst-case response time is two scan cycles. A_2 has a conversion time of 1 millisecond, so that the display will require 2 ms to follow a change in V_{in} and 4 ms to follow any change in the setpoint potentials. Because of this high refresh rate, no flicker will be observed on the LED display. □



Visualizing voltage. Eight-by-eight-LED matrix and C-MOS logic form analog dual-setpoint meter. Setpoint potentials and data voltage V_{in} are each introduced into multiplexer and scanned in sequence, then converted into control signals that light the appropriate LEDs in the matrix. Setpoint LEDs are half the brightness of the LED representing V_{in} because they are sampled at half the rate.

Cascaded C-MOS blocks form binary-to-BCD converters

by Haim Bitner
Seforad-Applied Radiation Ltd., Emek Hayarden, Israel

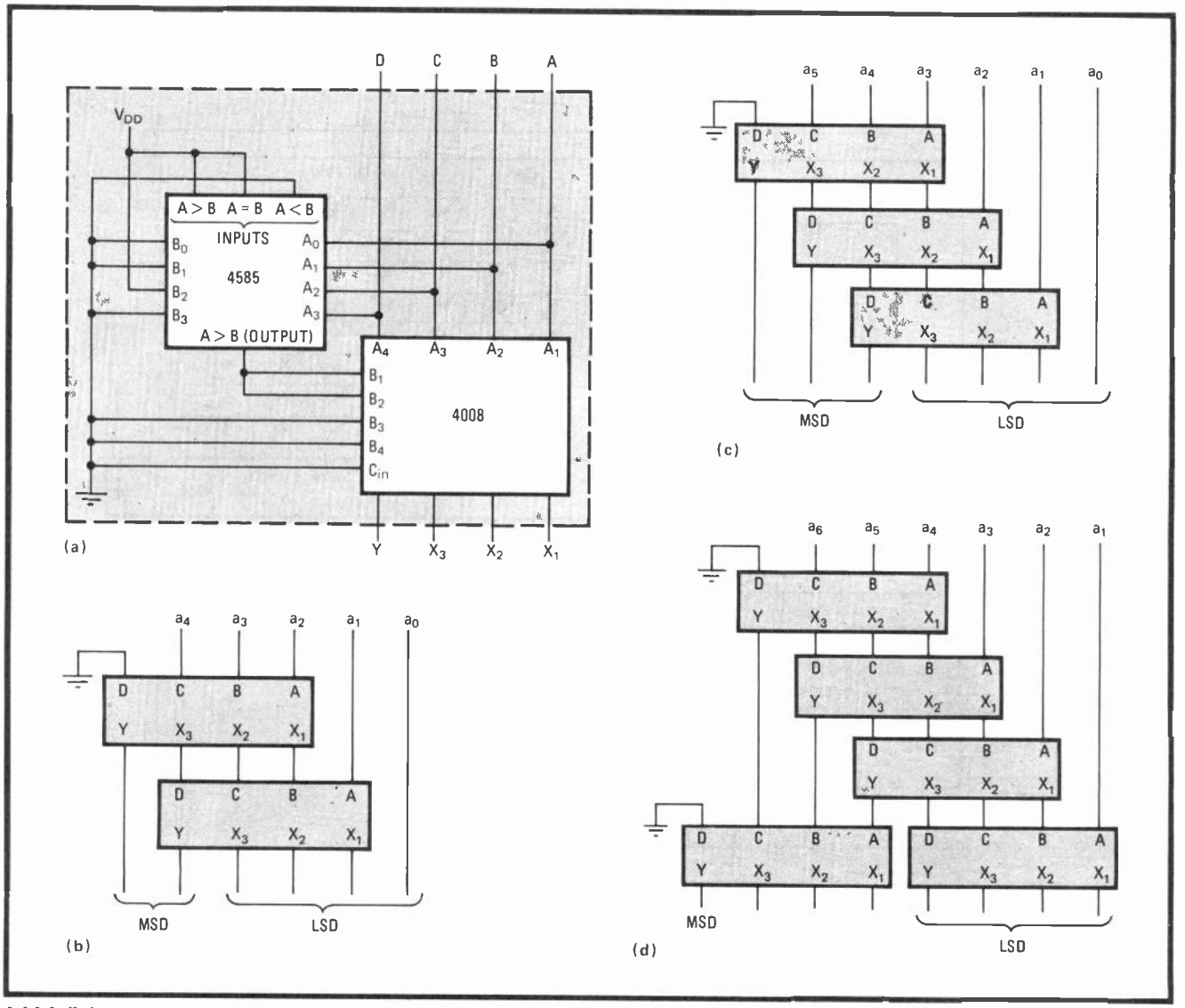
Low-power complementary-metal-oxide-semiconductor adders and comparators are easily combined to form this 4-bit binary-to-BCD converter. When the basic adder-comparator blocks are cascaded, the converter can be expanded to turn n binary input bits into a binary-coded-decimal output. The circuit is simpler than one using counters, and read-only memories are eliminated.

Comprising the basic 4-bit converter block (a) are the 4008 full adder and the 4585 comparator. The binary inputs are introduced at A–C, with A being the next to least significant bit, and D grounded. The BCD output appears at X_1–X_3 and Y of the 4008. The LSB input bypasses the unit and becomes the LSB output.

The 4585 compares the input bits to a binary number (0100) which is hard-wired to pins B_0–B_3. Thus the output of the 4585 is low if the number at A–D is less or equal to 4. The X_1–X_3 outputs of the 4008 are then identical to the input bits.

If the input number becomes greater than 4 (that is, greater than 0100), the 4585's output moves high, and so binary number 0011 is placed on the B_1 and B_2 inputs of the 4008 adder. Thus, 3 is added to the input number and the Y output of the 4008 goes high, indicating the most significant digit is active.

By cascading units, 5-bit (b), 6-bit (c) and 7-bit (d) converters can be built. The method can be used to extend indefinitely the number of bits processed. Note that the value of the least significant input bit (a_0) is numerically equal to its BCD-equivalent and so passes straight from input to output in all cases. □



Add infinitum. Low-power binary-to-BCD converter (a) requires only C-MOS adder and comparator for processing 4 bits. Unit is so configured that basic building blocks can be easily combined to form 5-bit (b), 6-bit (c), and 7-bit (d) converters.

Bidirectional optoisolator puts two LEDs nose to nose

by Forrest M. Mims III
San Marcos, Texas

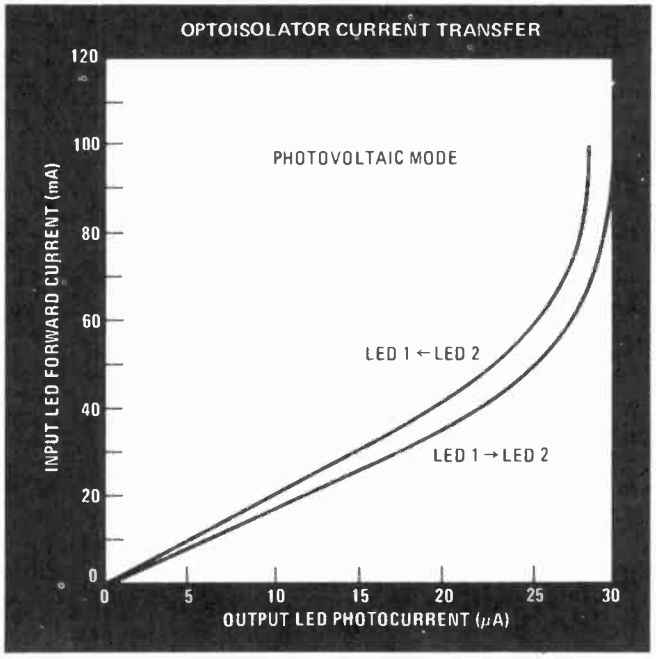
As conventional optoisolators employ a separate source and sensor, they can transfer current in only one direction. A few photodetectors and electroluminescent diodes can double as both a source and sensor, however, and when they are suitably connected they offer users a convenient way to build a low-cost bidirectional optoisolator, as shown here.

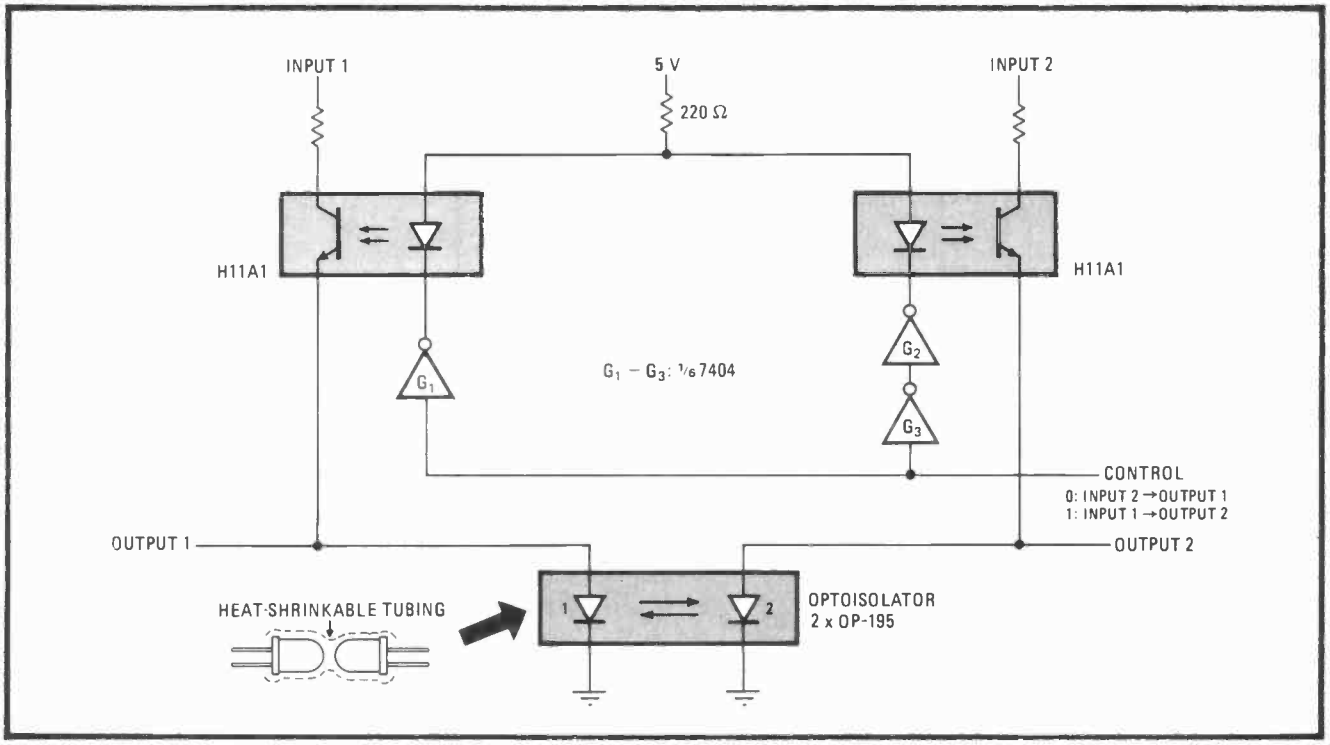
Two OP-195 LEDs, which have gallium-arsenide-silicon infrared emitters, can be made to transfer signals in either direction if they are placed nose to nose in a short length of heat-shrinkable tubing and secured in place by heating the tubing. Alternatively, the LEDs may be quite far apart if they are coupled by a plastic or glass-fiber waveguide.

In either case, the current transfer ratio (I_o/I_{in}) for the pair, with proper biasing, will be 0.06% for an input current of 20 milliamperes. This ratio is far too low for many applications but is good enough for some specialized roles where a bidirectional path is required. In any case, the output signal can be amplified or buffered, as necessary.

A logic-control voltage and two H11A1 optoisolators serve as the input/output port selector. Whichever of the OP-195 devices is designated the output diode may be connected in the reverse-biased photo-conductive mode or the unbiased photovoltaic mode. In the latter case, the output device is not biased. The response of the optocoupler operating in this mode for a given signal-input current is shown in the plot. Note the device linearity is completely adequate for duplex voice communication.

The photovoltaic current transfer ratio is virtually identical to that for photoconductive operation up to an input current of 20 milliamperes. The ratios begin to depart considerably above 40 mA. □





Either way. Standard light-emitting diodes encased in heat-shrink tubing can be made to function as a bidirectional transmission link. Alternatively, LEDs may be coupled through optical fibers. Control circuit for selecting input/output port arrangement is simple, using two optoisolators and three inverters. Circuit's current-transfer ratio suffices for many small-signal applications.

Notch filter and meter measure power-line harmonics

by Henno Normet
Diversified Electronics Inc., Leesburg, Fla.

Valid measurements of core loss in power-line transformers and various other magnetic devices require total harmonic distortion (THD) levels under specified limits—usually 3%. This inexpensive circuit determines the THD present in a 60-hertz waveform, over the range of 0 to 10%. Here, a notch filter is used to eliminate the voltage source's 60-Hz fundamental component, allowing an ac voltmeter to measure the remaining harmonic components.

The adjustable-Q Wien-bridge notch filter discussed in a previous article[1] proved to be best adapted for this application. Resistors R_{11} and R_{12} of the bridge (see shaded portion of figure) are selected to give the notch filter a Q of 10. The resulting null is sharp enough to pass a 180-Hz signal without attenuation, the lowest harmonic to appear as a component of distortion.

Component selection for the rest of the filter is also important to the achievement of good notch depth. C_1 and C_2 should be matched within 1%, and high-accuracy resistors used where indicated by asterisks. Metal-film resistors and polycarbonate capacitors help keep frequency drift and aging to a minimum.

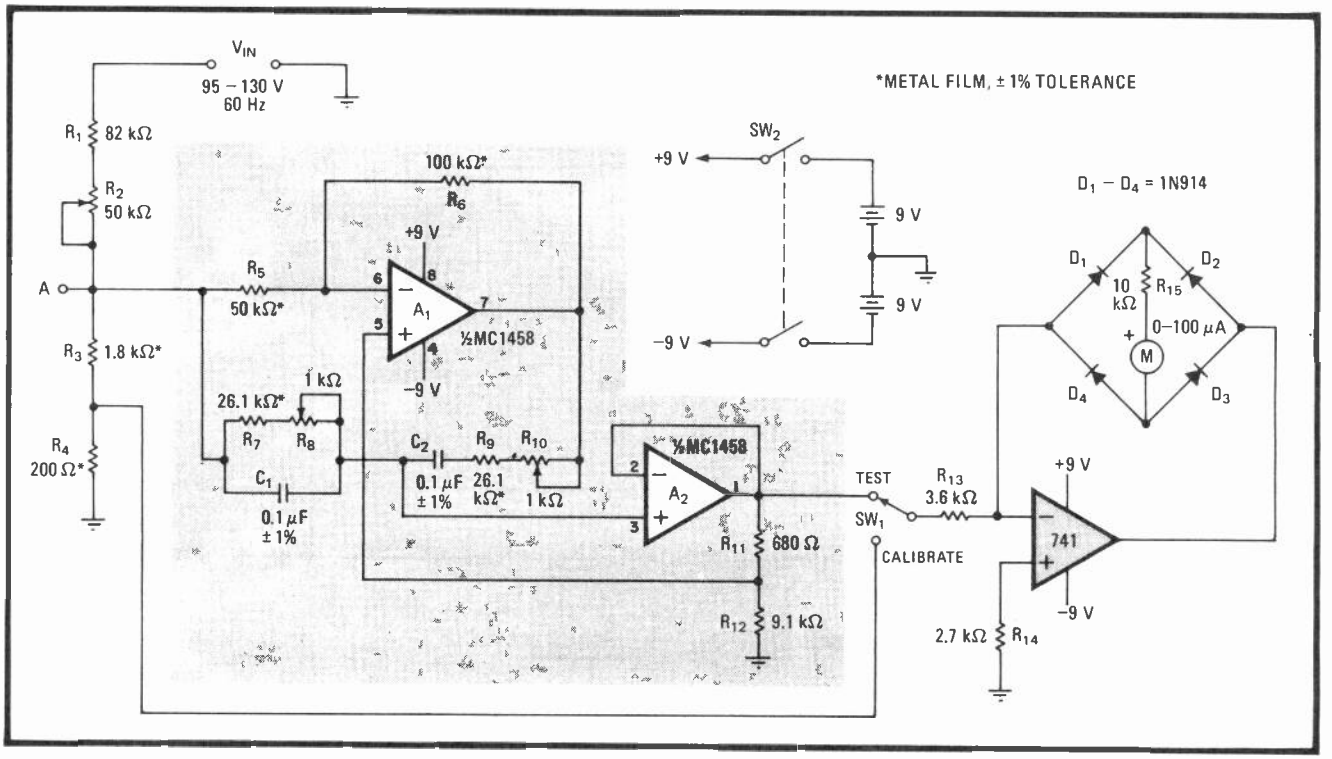
For initial balancing of the bridge, a low-distortion 2-V signal at 60 Hz is applied at point A. With SW_1 in the test position, R_8 and R_{10} are adjusted for a zero reading on the meter, M. If an audio oscillator is not available as a signal source, full line voltage may be applied to the input terminals, in which case R_8 and R_{10} are adjusted for a minimum reading on the meter.

In operation, SW_1 is first placed in the calibrate position and line voltage applied at the circuit input, V_{in}. R_2 is then adjusted for a maximum (full-scale) reading.

The switch is then placed in the test position, whereupon the input signal passes through the notch filter. Percent of THD may then be read directly. Note that the accuracy of the reading depends upon the accuracy of the 10:1 voltage divider, R_3 and R_4.

The definition of THD requires that both the calibration and measurement procedure be carried out with a root-mean-square-responding meter. However, in the 0–10% distortion range, a less costly average-responding meter will provide 10% accuracy, which is acceptable in most applications. □

References
1. "Wien bridge and op amp select notch filter's bandwidth", *Electronics*, Dec. 7, 1978, p. 124.



Handling harmonics. Wien-bridge notch filter rejects 60-Hz power-line fundamental frequency so that total harmonic distortion present in signal can be measured. Meter measures THD over 0-to-10% range. An rms-responding meter should be used, but an average-responding meter is acceptable. Results are displayed in percent, with an accuracy directly proportional to the tolerance of resistors in divider R_3–R_4.

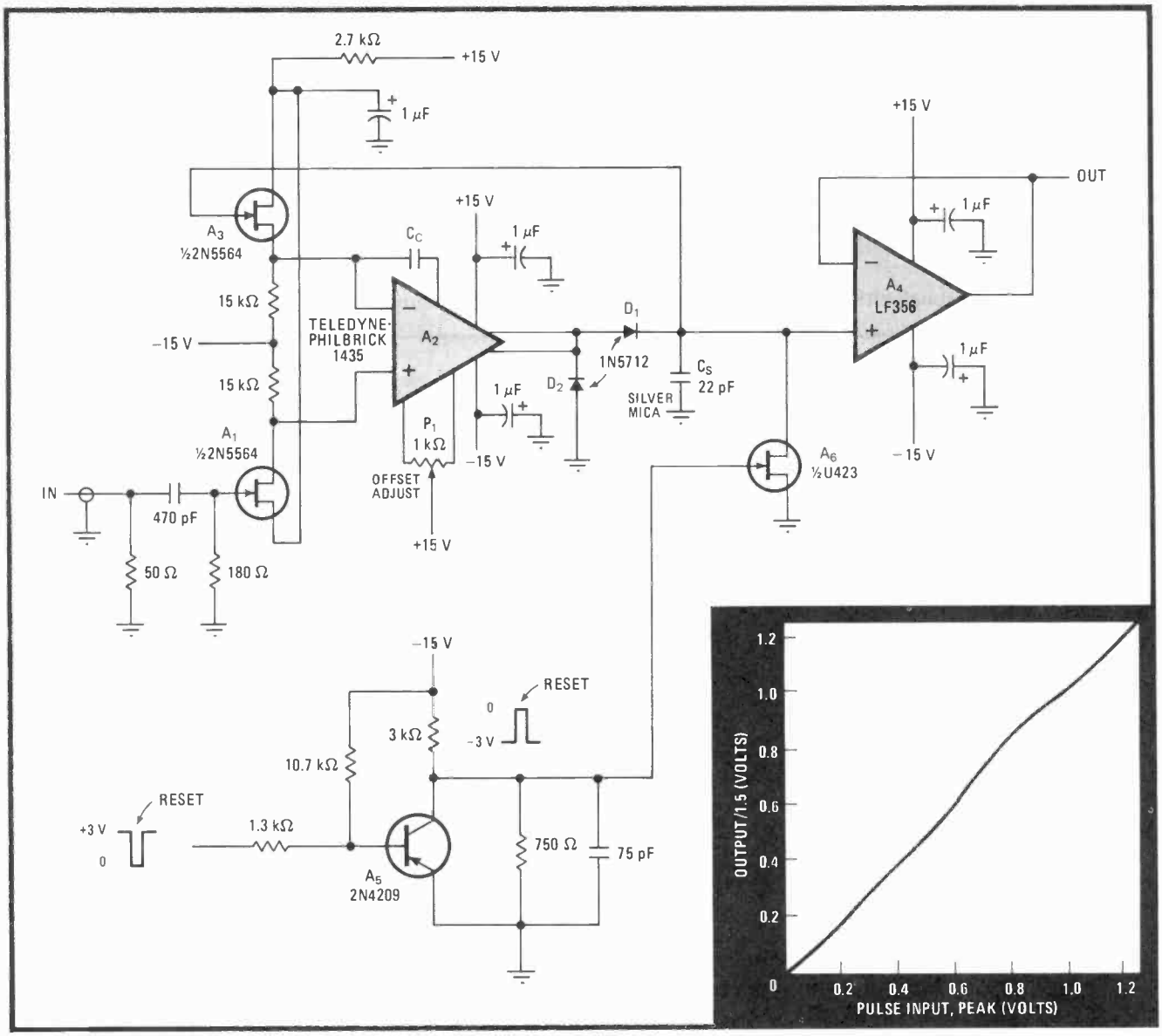
Wideband peak detector recovers short pulses

by Saul Malkiel
Advanced Technology Systems, Roselle, N. J.

Using a Schottky-barrier diode for detection and a wideband operational amplifier, this peak detector recovers data pulses as narrow as 10 nanoseconds in the range of 0.1 to 1.3 volts. The circuit's linearity as a percentage of the full scale output is 4%.

The input signal, whose rise time is assumed to be a minimum of 10 ns, is applied to one side of the differential source follower, A_1-A_3, via a 50-ohm coaxial cable. A blocking capacitor removes any baseline shifts. The output of this JFET follower is then applied to the wideband amplifier, A_2. The amplifier has a gain-bandwidth product of 1 gigahertz.

The output of the amplifier switches on diode detector D_1 so that a charging current can be delivered to storage capacitor C_s. When there is overshoot, source follower A_3 is turned on more heavily than A_1 so that A_2 may be driven negative. D_2 then comes into play, acting to limit the amplifier's negative excursion. The excursion, coupled through D_1's shunt capacitance, reduces the



Narrow capture. Wideband amplifier and fast diode detect pulses having widths as small as 10 ns. Output-to-input voltage linearity of circuit is 4%, and linearity is virtually independent of pulse width. Response is illustrated in curve at bottom right.

Phase-locked loop aids in measuring capacitance

by Ronald E. Pyle
Tracor Inc., Austin, Texas

In this circuit, a phase-locked loop (PLL) aids in measuring an unknown capacitance to within 1% of its true value, over the range of approximately 10 picofarads to 1 microfarad.

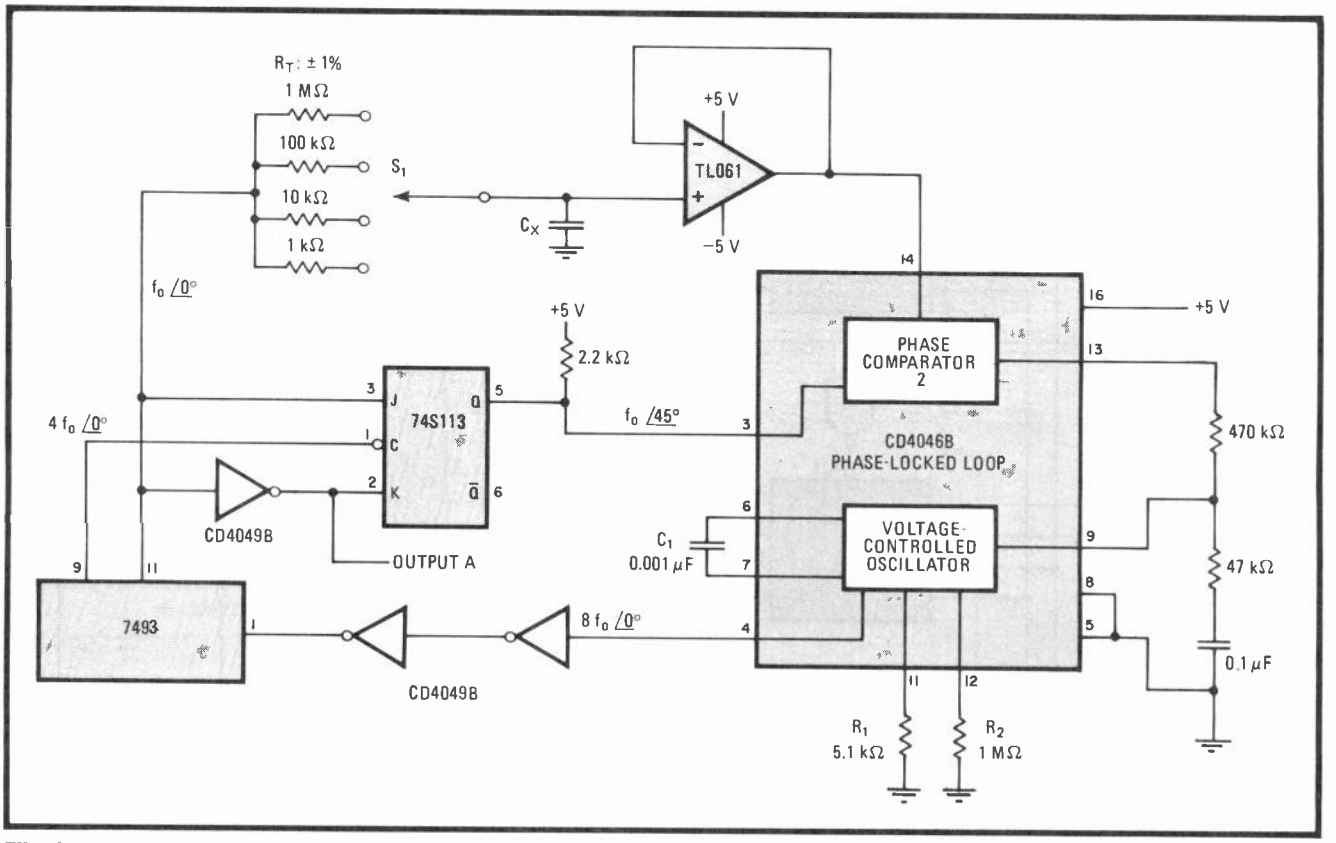
As the figure shows, the unknown capacitance, C_x, is part of low-pass filter R_TC_x. The filter's output serves as one input to the PLL's phase comparator, the other input being derived from the loop's voltage-controlled oscillator (VCO). Circuit operation is based on the principle that the phase lag at the filter's output is 45° at f_o, the filter's center frequency. The PLL thus acts to generate a frequency having a 45° lag on the other port of its phase comparator, locking the loop. The output frequency of the oscillator at locking represents an index of the capacitance measured.

The output frequency of the VCO in the CD4046B PLL passes through a buffer and is divided by 2 and 8 by the 7493 4-bit counter. These signals are next routed to the 74S113 J-K flip-flop, which generates a wave shifted 45° with respect to the input signal on the J port.

The flip-flop's output is then compared with the filter's output signal at phase comparator 2 of the 4046B. This comparator is an edge-controlled network that indicates 0° phase difference between the input test signal and the VCO-derived signal, when locking is achieved. The 4046's locking and capture range is approximately two decades, which is what makes it possible to measure the wide range of capacitances mentioned above. Suitable selection of R_1 and C_1 extends the measurement range still further.

A frequency counter measures the output of the circuit in the locked condition as $f_o = 1/2\pi\ R_TC_X$. From this the unknown capacitance can readily be determined. Look-up capacitance tables plotted as a function of f_o and R_T can be readily constructed for rapid checking. Alternatively, extra hardware may be added to convert the frequency into a capacitance value directly, thus forming a self-contained digital capacitance meter. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.



Filtering an answer. A phase-locked loop finds the center frequency, f_o, of low-pass filter R_TC_x, thus enabling determination of test capacitance C_x, from $f_o = \pi\ R_TC_x$. The VCO derives an output whose phase lag matches that of the lag at the filter output at the PLL's comparator, so that locked state is achieved. The VCO output, f_o, thus represents an index of the capacitance measured.

LED dot/bar driver simplifies solid-state scope

by Forrest M. Mims III
San Marcos, Texas

The design of this solid-state scope is simplified by use of a one-chip driver to address the rows of the light-emitting-diode matrix comprising the scope's display. The circuit is a viable alternative to a scope that has previously been described.[1]

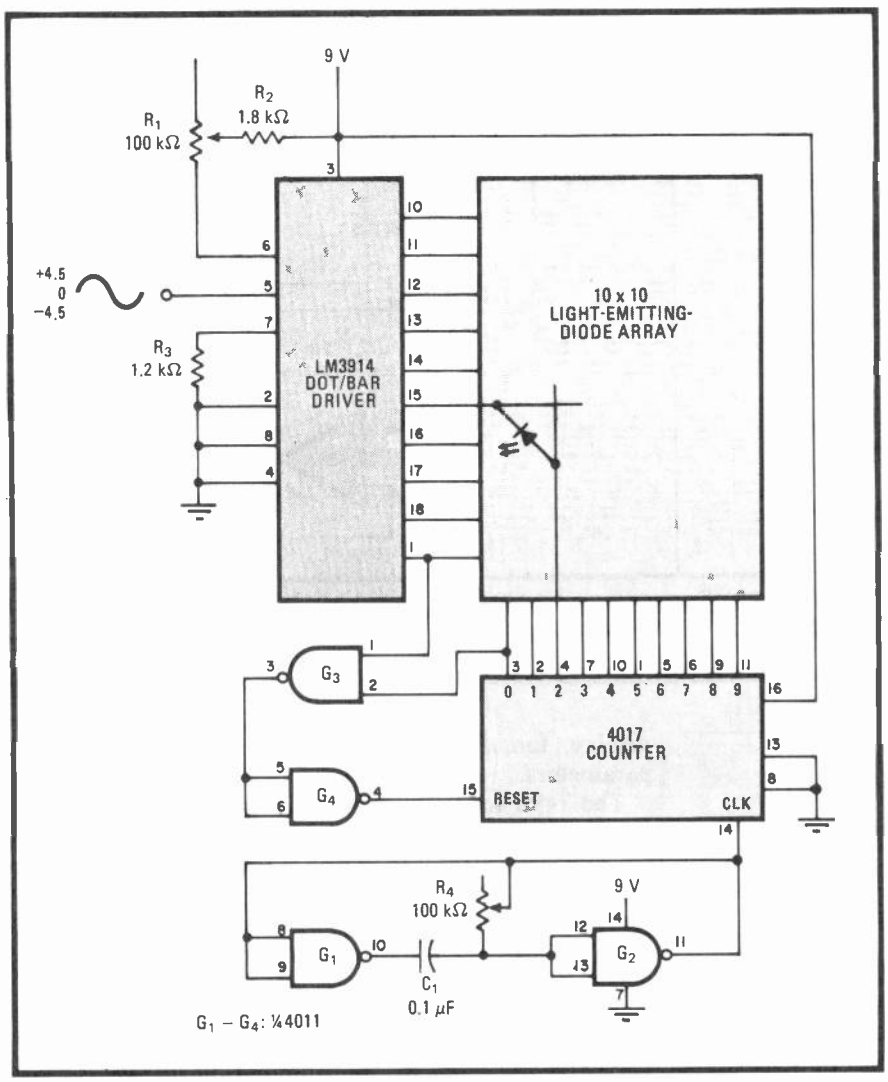
The unit will handle input signals in the audio-frequency range. Signals to be displayed are applied to pin 5 of the National LM3914 dot/bar driver and resolved to one of ten active-low output levels. Note that R_3 provides a programmable current control for all LEDs in the display. Thus, current-limiting resistors are not required at each output port of the driver. Pin 7 is connected to an internal 1.2-V reference so, as a result, current through R_3 is approximately equal to one tenth the LED current; thus, with R_3 = 1.2 kilohms, the LED current becomes equal to 10 milliamperes.

The 4017 Johnson counter and accompanying gates comprise the scope's horizontal-sweep circuit. The sweep oscillator driving the counter is made from half a 4011 quad-NAND gate, G_1 and G_2, its frequency controlled by resistor-capacitor combination C_1–R_4. In this way, the instantaneous input voltage is resolved to 1 LED in 100. G_3 and G_4 provide automatic triggering of the sweep.

As for the LED display itself, bar arrays that contain 10 diodes each are easier to use and provide a more uniform display than discrete diodes, and are therefore recommended. Another option is to employ miniature matrix arrays of five by seven dots. At least one firm, IEE Inc. (7740 Lemona Ave., Van Nuys, Calif. 91405), offers such displays that can be mounted adjacent to each other without a gap in the LED columns.

Both the vertical and horizontal driving sections of the basic scope can be readily expanded. For instance, five cascaded counters and five cascaded dot/bar chips can drive a 50-by-50-diode matrix, forming a scope with a display resolution of 1 LED in 2,500. □

References
1. Vernon Boyd, "LED bar-segment array forms low-cost scope display," *Electronics*, Nov. 24, 1977, p. 128.



Drive center. One-chip dot/bar driver reduces complexity of vertical scanning portion of scope having light-emitting diode display. Horizontal scanning portion uses G_1 and G_2 for clock, wired as astable multivibrator, and 4017 counter. Display resolution is 1 LED in 100.

Bridged-T selects filter's notch frequency and bandwidth

by P. V. Ananda Mohan
Indian Telephone Industries Ltd., Bangalore, India

If a bridged-T network is used in place of the Wien bridge in the notch filter proposed by Fellot,[1] both the bandwidth and the frequency may be independently adjusted. The bridged-T approach has been explored previously[2] as an extension of some work carried out on parallel-T notch filters, and, as illustrated here, the technique offers an excellent way of building units that are simple and versatile.

R_N and R_Q comprise the balancing arms of the bridged-T network (note A_1 is a unity-gain buffer) as seen in (a). In this configuration, the circuit's transfer function is:

$$e_o/e_i = [ns^2+\omega_o^2]/[s^2+3(1-q)s\omega_o+\omega_o^2]$$

where n and q are selected by R_N and R_Q, respectively, and $\omega_o = 1/RC$. Note that $0 \leq n, q \leq 1$, and that the frequency of the notch is

$$\omega_n = \omega_o/n^{1/2}$$

Therefore for this circuit ω_n will always be equal to or greater than ω_o.

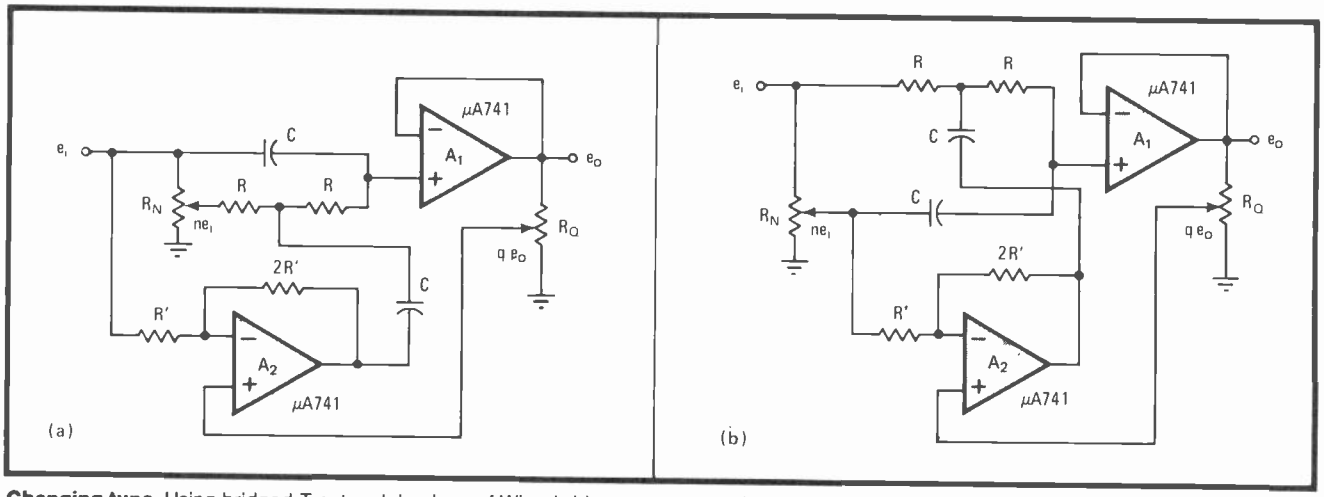
The bandwidth is adjusted with R_Q, and Qs greater than 1,000 will be realized when high-gain operational amplifiers are used. In general, Qs will be higher than can be achieved with parallel-T networks. The notch depth is at least 50 decibels throughout the operating range. R_N and R_Q must only be at least 10 times smaller than R to achieve the stated filter characteristics.

By modifying the circuit slightly, as in (b), the transfer function becomes:

$$e_o/e_i = [s^2+n\omega_o^2]/[s^2+3(1-q)s\omega_o+\omega_o^2]$$

and the notch frequency ω_n is made tunable for frequencies below ω_o, so that $\omega_n = \omega_o n^{1/2}$. □

References
1. Dominique Fellot, "Wien bridge and op amp select notch filter's bandwidth," *Electronics*, Dec. 7, 1978, p. 124.
2. "An Active RC Bridged-T Notch Filter," *Proc. IEEE*, August 1977, p. 208.



Changing tune. Using bridged-T network in place of Wien-bridge arrangement in notch filter enables independent control of filter's bandwidth and frequency. Circuit can be configured for tuning filter above (a) or below (b) its natural radian frequency $\omega_o = 1/RC$.

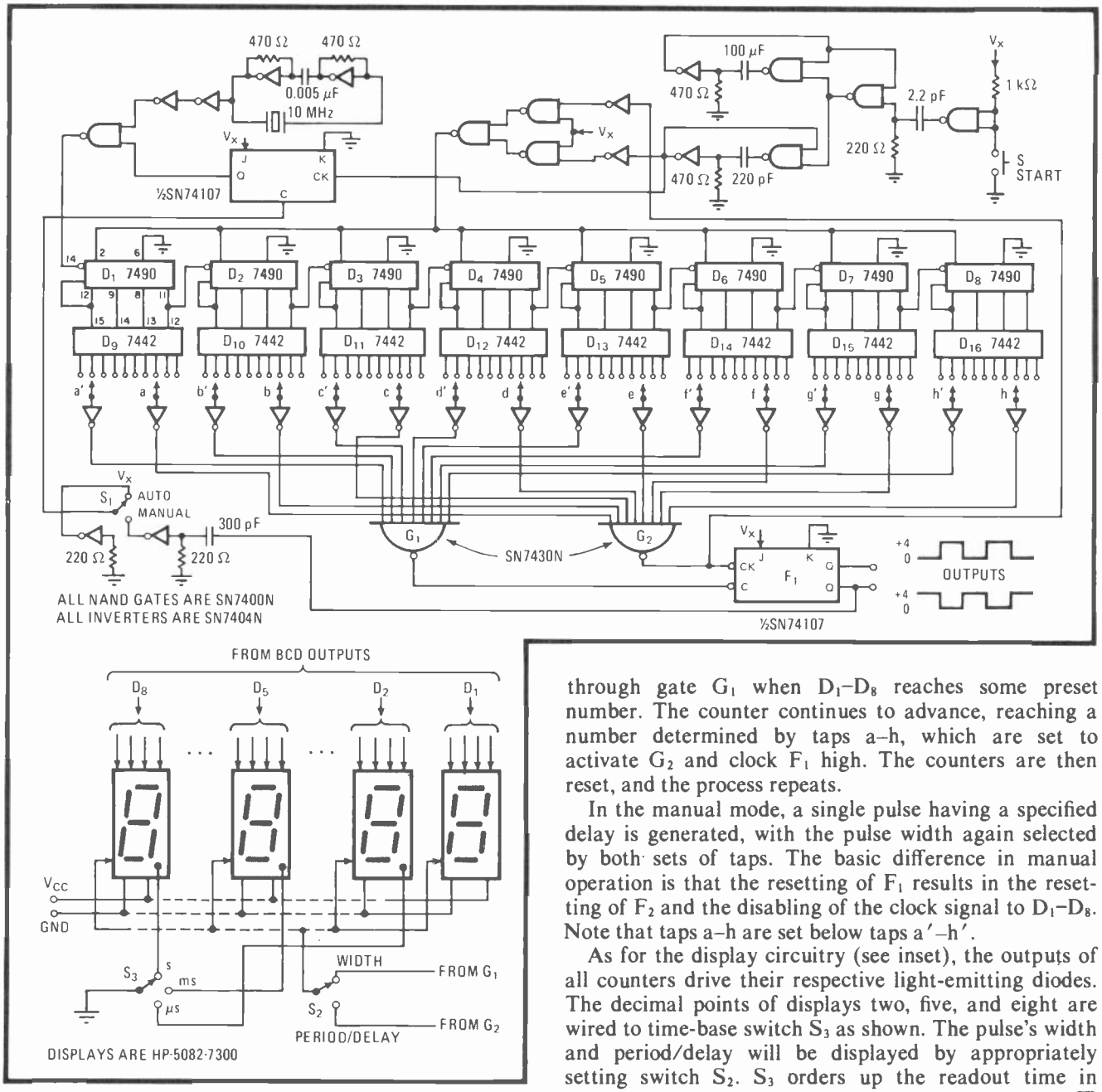
Wide-range pulse generator displays timing parameters

by C. L. Bhat and R. C. Yadav
Bhabha Atomic Research Center, Srinigar, India

In this circuit, cascaded decade counters provide adjustable pulse width, period, and delay from 0.1 microsecond to 10 seconds. This generator contains an LED digit display, too, for direct readout of the various pulse parameters.

The 7490 counters, D_1–D_8, serve simultaneously as a frequency divider and preset counter unit. Depressing the momentary-contact switch S resets D_1–D_8 and gates the 10-megahertz clock through to the counters, whereupon they advance upward from zero.

When operated in the automatic mode (switch S_1), the unit will generate pulses with repetition frequency and width controlled by the clock frequency and the position of two sets of taps at the output of the 7442 4-to-10-line decoders. Here taps a′–h′ bring output flip-flop F_1 low



Watching width. Pulse generator provides adjustable width and period over a 0.1-microsecond-to-10-second range. A single pulse of specified delay may also be generated. LED-digit display gives direct readout. Wiring of display-switching circuitry (inset) is simple.

through gate G_1 when D_1–D_8 reaches some preset number. The counter continues to advance, reaching a number determined by taps a–h, which are set to activate G_2 and clock F_1 high. The counters are then reset, and the process repeats.

In the manual mode, a single pulse having a specified delay is generated, with the pulse width again selected by both sets of taps. The basic difference in manual operation is that the resetting of F_1 results in the resetting of F_2 and the disabling of the clock signal to D_1–D_8. Note that taps a–h are set below taps a′–h′.

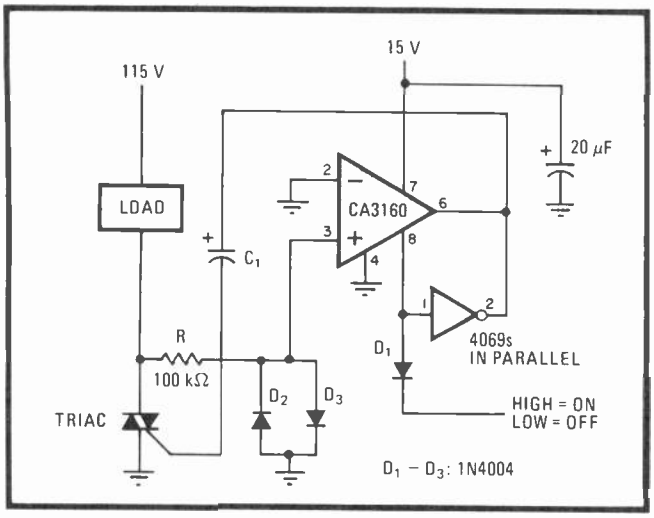
As for the display circuitry (see inset), the outputs of all counters drive their respective light-emitting diodes. The decimal points of displays two, five, and eight are wired to time-base switch S_3 as shown. The pulse's width and period/delay will be displayed by appropriately setting switch S_2. S_3 orders up the readout time in seconds, milliseconds, or microseconds. □

C-MOS triac trigger cuts parts count

by Hul Tytus
Tytus & Co., Cincinnati, Ohio

Integrated circuits made to trigger triacs often consume large amounts of power and require biasing schemes substantially increasing the number of components in the circuit facing the ac load. But by using a C-MOS operational amplifier, the circuit shown can deliver a peak current of 100 milliamperes to the triac, draws an average current of only a few milliamperes and uses a minimum of parts.

Circuit operation is based on the fact that the output of a C-MOS device acts as a current source or sink. As the ac-input voltage rises up through zero, the CA3160 generates a positive-going current pulse of a preset magnitude and charges C_1, which determines the triac's



Diminutive driver. C-MOS operational amplifier, operated from a single supply, minimizes power drain and parts count in triac trigger that can source 100 milliamperes. C-MOS inverters may be placed in parallel with op amp for circuit to drive heavier loads.

pulsing time. As the ac line voltage completes a half cycle and drops through zero, C_1 discharges through the op amp, which now serves as a current sink, so that the triac is again fired.

Note that several 4069 inverters can be placed in parallel with the op amp's strobe (pin 8) and normal outputs to drive heavier loads. Pin 8 and D_1 may also serve as a control terminal, enabling operation with 4049s permanently wired into the circuit.

The maximum rated trigger current of the triac should equal the minimum current the 3160 and 4069s are capable of sourcing. The pulse time for the triac—typically measured in microseconds—should equal the time necessary for the ac supply to generate the necessary conduction voltage across the triac, plus t_T max, the maximum trigger time for the triac. The value of capacitance required for a given trigger current, I, triac pulse time, t, and maximum trigger voltage, V_T, is given by:

$$C_1 = I\,t/(0.75\,V_{dd} - V_T)$$

where V_{dd} is the op amp's supply voltage. □

One-chip gyrator simplifies active filter

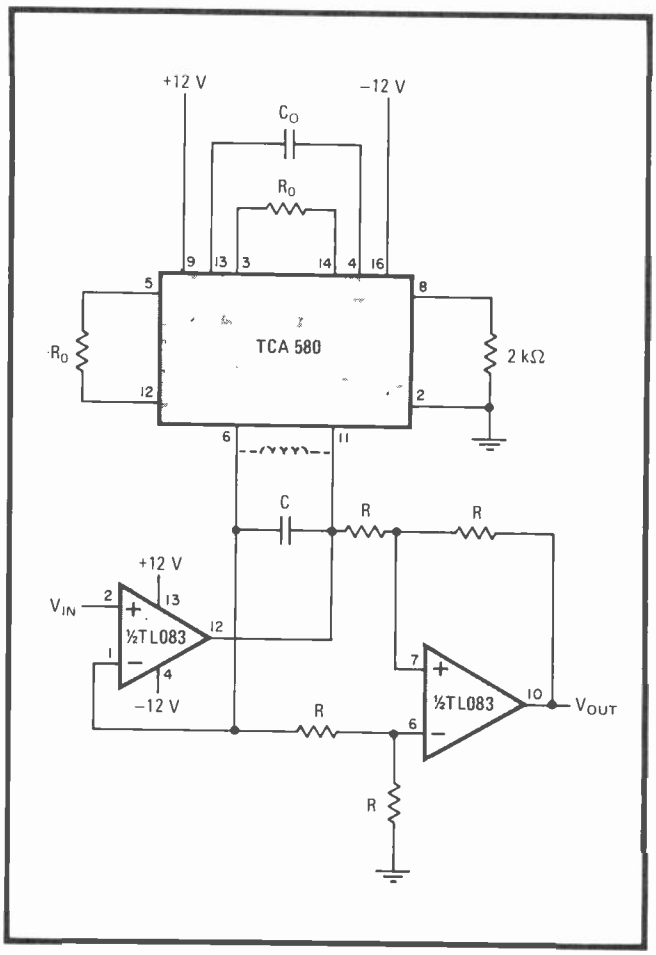
by Kamil Kraus
Rokycany, Czechoslovakia

Now that gyrators, or impedance inverters, are available on a single integrated circuit, active filters with both high input impedance and few component-sensitivity problems can be easily built in a small area with a minimum of parts. This one uses only one other active component—a dual operational amplifier—to provide low-pass, high-pass, bandpass, or band-reject response at reasonable cost over the dc range to 10 kilohertz.

The low-cost TL-083 op amp has been selected for use in the circuit because of its virtually negligible input-offset voltage and input-bias current. These characteristics are required to achieve a high input impedance over the range of interest and to realize the optimum response of the filter.

The Signetics TCA 580 gyrator simulates the relatively large inductor needed for the required LC (passive) network. The inductance across pins 6 and 11, and thus in parallel with capacitor C, is $L = C_0R_0^2$. The resonant (center) frequency of the LC combination, in turn, is $f_0 = 1/2\pi\,(LC)^{1/2}$, with its quality factor $Q = R(C/L)^{1/2}$. Thus the filter, which is shown configured on the bandpass mode, can be made to work at any frequency and Q, once its components are suitably selected.

The circuit can be transformed into a low-pass filter if its output is applied to an integrator whose time constant is RC. Similarly, it will function as a high-pass filter if its output is applied to a differentiator whose time constant is RC. For band-reject operation, C must be placed in series with the simulated inductor. □



Optimal. Gyrator and operational amplifier comprise a simple two-chip bandpass filter with high impedance and state-of-the-art stability. Filter configuration remains the same for high-pass and low-pass operation; only an external differentiator or the integrator, respectively, need be added. For the band-reject mode, C is placed in series with a simulated inductor.

Switching converter raises linear regulator's efficiency

by Sadeddin Kulturel
Istanbul, Turkey

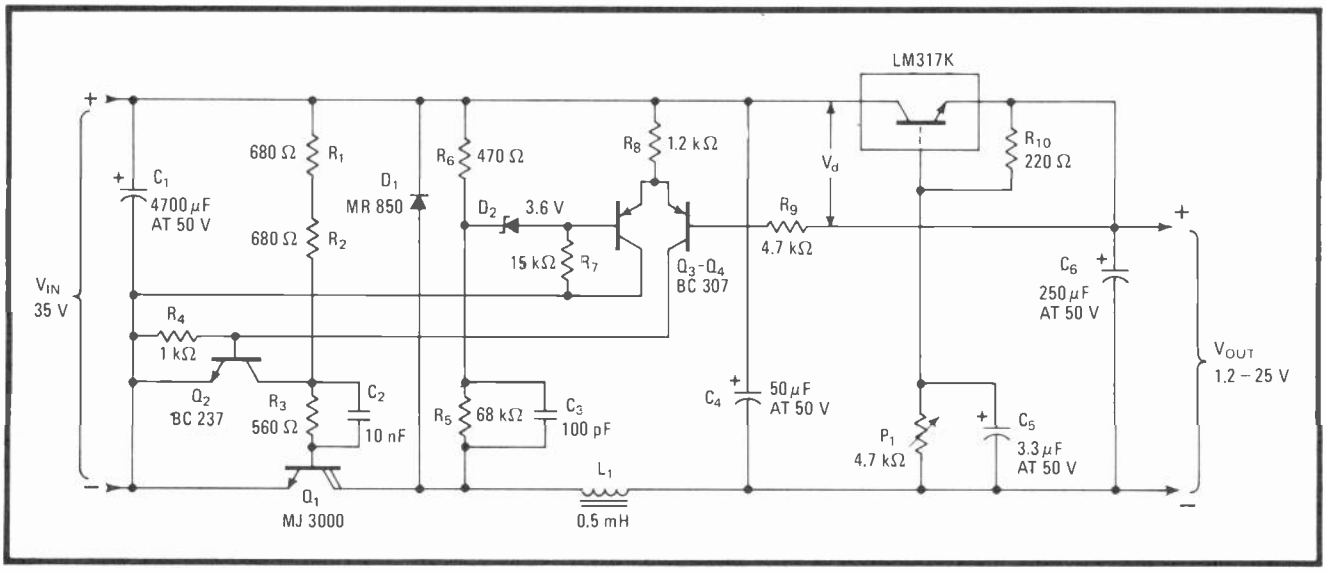
The low ripple and fast recovery of a series-pass voltage regulator can be attained at the high efficiency of a switching regulator if both are combined. In this circuit, the performance is achieved by using the switching circuit as a preregulator for the linear element.

As shown in the illustration of the general circuit, which is designed to transform the 35-volt raw input into a well-regulated output, heat dissipation across the LM317K series element can be reduced if it is made to handle a switched, rather than a continuous, input. Here, the switching regulator is formed by transistors Q_1–Q_4, D_1, and L_1. During power up, Q_1, driven through R_1–R_3, is brought into saturation. Q_2 remains off and Q_3 is turned on.

Switching occurs when V_d equals 3.6 volts, which is D_2's zener voltage. Q_4 then turns on, as does Q_2, and Q_3 is turned off.

As Q_2 turns on, Q_1 switches off, and because of the positive voltage spike created by L_1, load current is momentarily forced through D_1 as V_d decreases. When V_d reaches the lower hysteresis threshold of Q_3 as established by R_5 and R_6, Q_2 and Q_4 turn off, and Q_1 turns on, completing the switching cycle. With the supply's negative path restored, V_d rises until it reaches V_2, and the process is repeated.

The linear regulator can be of any type, including a three-terminal, nonadjustable device. Note that a switching current regulator can be formed if the regulator is replaced by a resistor. In that case, the switching current will be $I_S = V_Z/R$. □



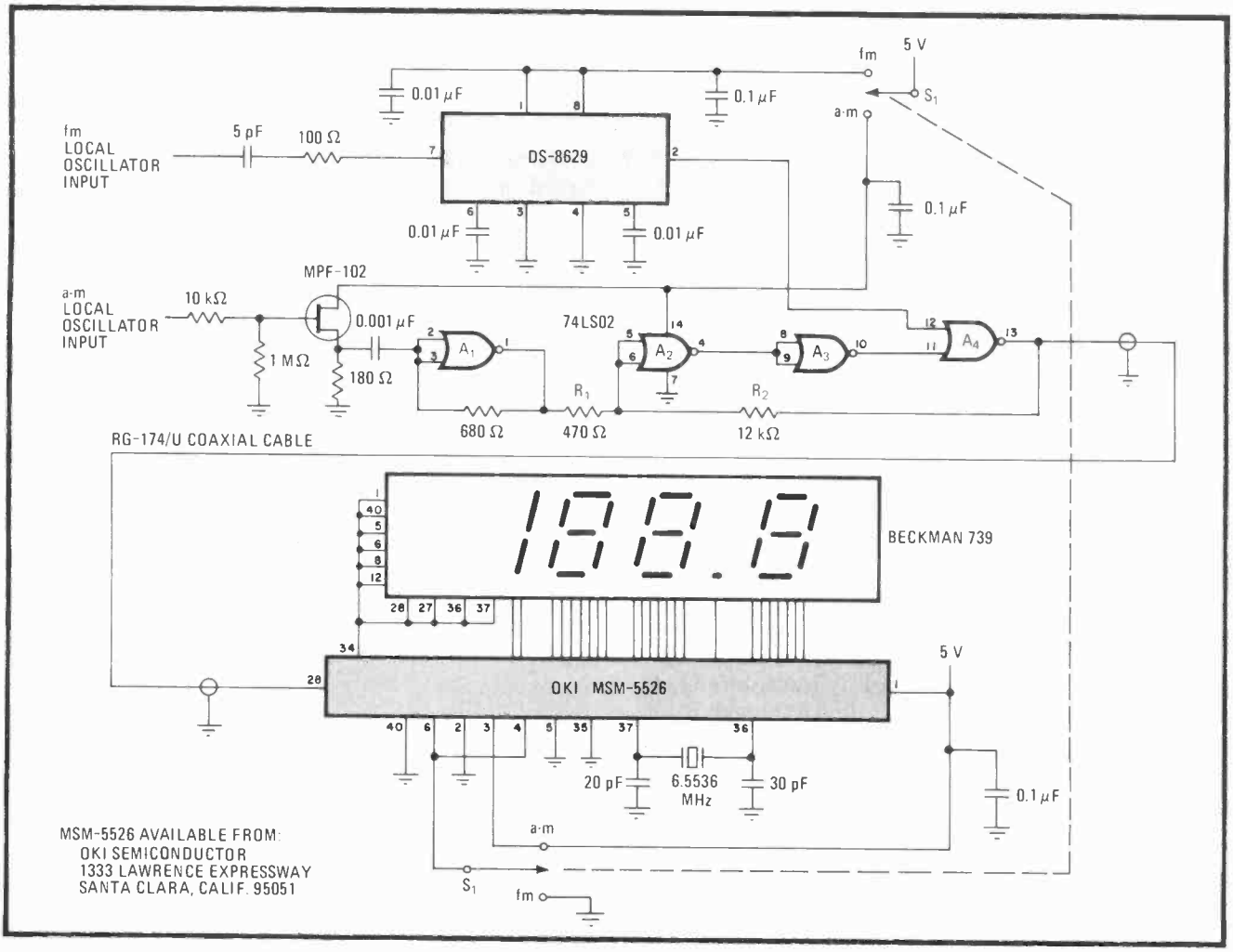
Mixed mode. Switched and linear regulators are combined to form a unit that has the advantages of both—low ripple, fast response, and high efficiency. Here a switched circuit serves as a preregulator for the linear series-pass element, the LM317K.

LSI counter simplifies display for a-m/fm radio

by Gary McClellan
Beckman Instruments Inc., Fullerton, Calif.

The design of a display providing a direct readout of any frequency tuned by an a-m/fm radio is made simple with this circuit, which uses a large-scale integrated counter-driver to determine the frequency of the receiver's local oscillator. The counter is unique in that it contains circuitry that subtracts the receiver's intermediate frequency from the local oscillator frequency in order that the true channel frequency may be found. The combination of this counter, a one-chip prescaler, and a 3½-digit liquid-crystal display makes for a compact and relatively low-cost unit.

The circuit is housed in two separate modules, one containing the preamplifier, prescaler, and logic, and the



I-f compensation. MSI and LSI chips reduce cost and complexity of display for a-m/fm radio. MSM-5526 counter has circuitry for subtracting receiver's i-f frequency (see table) from radio's local oscillator input so that the true channel frequency may be displayed.

other the counter and LCD components. In this way, the first module can be mounted on the receiver's radio frequency assembly (keeping unwanted pickup to a minimum), and the other may be placed at any convenient spot for viewing.

In the a-m mode, signals are applied to the MPF-102 field-effect transistor. The input impedance of this stage is high, and consequently loading of the local oscillator is minimal. A_1 operates in its linear region and thus serves to amplify the local oscillator signal.

Schmitt trigger A_2–A_4 squares up the signal to transistor-transistor–logic levels, then applies it to the MSM-5526 counter. R_1 and R_2 set the hysteresis of the trigger.

The MSM-5526 contains a read-only memory that may be programmed with any i-f value (see table). Also contained is the subtraction circuitry discussed previously, and the necessary decoders/drivers for presenting the 3½-digit Beckman LCD with the difference frequency in kilohertz. Generally, the local oscillator will always lie above the incoming frequency in the modern a-m receiver, as reflected in the table. The same condition holds true most of the time in fm receivers, but there is a provision for achieving a positive offset if one of the older receivers is being used. Note that if all programmable pins are set at logic 0, an i-f of 455 kHz for a-m

MSM-5526 INTERMEDIATE-FREQUENCY OFFSET

Display mode	Input-pin state				Offset (a-m in kHz, fm in MHz)
	2	3	4	5	
a-m (pin 6 high)	H	H	H	X	−452.5
	L	H	H	X	−454.5
	H	L	H	X	−456.5
	L	L	H	X	−465.5
	H	H	L	X	−467.5
	L	H	L	X	−469.5
fm (pin 6 low)	H	H	H	H	10.68
	L	H	H	H	10.71
	H	L	H	H	10.75
	L	L	H	H	10.79
	H	H	L	H	10.82
	L	H	L	H	−10.58
	H	L	L	H	−10.60
	L	L	L	H	−10.61
	H	H	H	L	−10.62
	L	H	H	L	−10.63
	H	L	H	L	−10.65
	L	L	H	L	−10.66
	H	H	L	L	−10.69
	L	H	L	L	−10.70
	H	L	L	L	−10.72
	L	L	L	L	−10.73

and 10.7 MHz for fm will be subtracted.

In the fm mode, the receiver's local oscillator is applied to the DS-8629 prescaler. This prescaler has high sensitivity, and the local oscillator need only be capable of supplying a minimum of 12 mV at 100 MHz.

The DS-8629 divides the incoming frequency by 100. Then the signal is gated through to the counter via A_4. In this configuration, an i-f equal to 1/100 the fm receiver's nominal value (10.7 MHz) is subtracted from the input frequency to the counter, and the result is displayed in megahertz.

A number of practical considerations must be taken into account when building this display. Specifically, the presence of the prescaler will introduce a typical shift of 500 Hz in the read-out frequency. The error may be eliminated entirely by simple adjustment of the 30-picofarad air-variable trimming capacitor, located at pin 36 of the counter.

The first module should be shielded from the receiver's tuner if noise in the fm mode is to be held to a minimum. Housing the module in an aluminum enclosure will suffice in most cases. And although the liquid-crystal display will tend to generate less noise than many light-emitting-diode displays now available, shielding it may also be necessary in extreme cases.

Both modules should be coupled via a coaxial cable. Otherwise a broadband hiss may be heard when the unit is placed in the a-m mode. □

Balanced modulator chip multiplies three signals

by Henrique Sarmento Malvar
Department of Electrical Engineering, University of Brazilia, Brazil

Three signals can be multiplied by a one-chip double-balanced modulator, a device normally capable of mixing only two. In this case, the third input is introduced at the bias port of Fairchild's μA796, enabling the unit's transconductance to be varied at an audio rate, which effects modulation. Although the technique reduces the bandwidth and dynamic range over which the device can operate, the three-input mixer will still be useful in many applications, notably for generating discrete sidebands and synthesizing music.

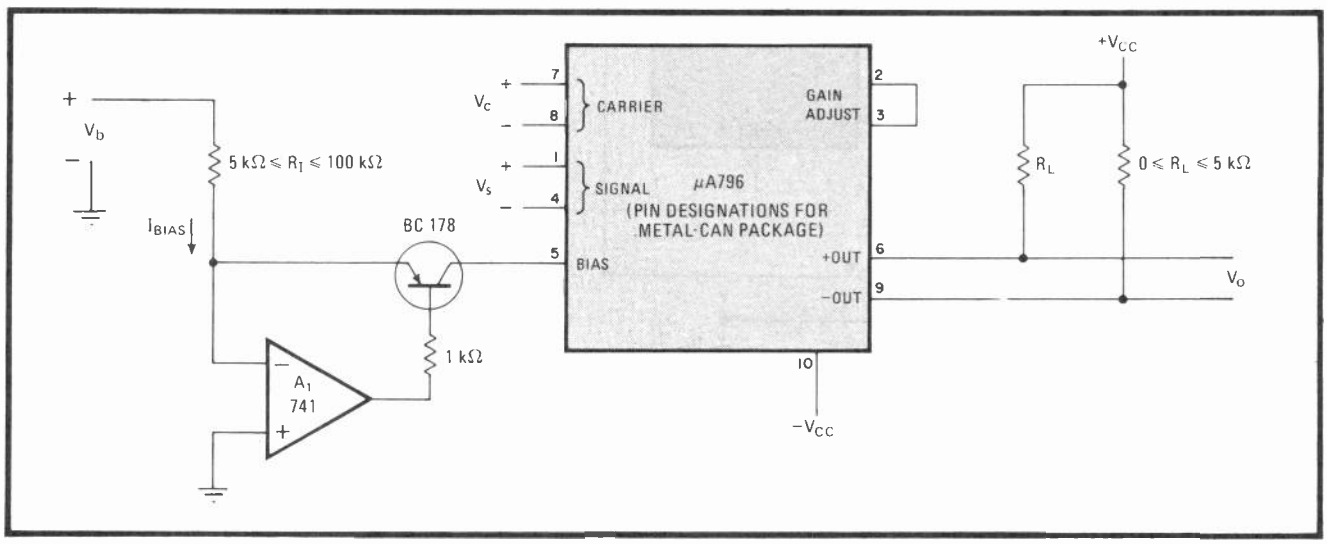
The output voltage from the mixer, V_o, is the product of a carrier switching function, V_c, and a modulated signal, V_s. Because the bias signal, V_b, controls the conductivity of transistors that are effectively in series with the usual modulating signal, it is simply regarded as a second modulating signal such that $V_o = kV_bV_cV_s$, where $k = 0.00064R_L/R_1$ over a small dynamic range and the voltages are in millivolts.

Note that V_c and V_s may be positive or negative but that V_b must always be positive to prevent the reverse-biasing of the internal transistors connected to pin 5. When V_b is negative, A_1 blocks the application of negative voltage by turning off the BC 178 transistor.

Note also that k will vary nonlinearly with the amplitude of V_c and V_s, and in order to keep k within 1% of its given value, both voltages must not exceed 8 millivolts root mean square. V_b will not affect k if $I_{bias} << 1$ milliampere. Unfortunately, k also is sensitive to temperature changes ($-0.67\%/°C$), and this factor can limit the circuit's effectiveness in high-accuracy applications.

The output frequencies generated by the mixing process will be $|f_c \pm f_s|$, and $|f_c \pm f_s \pm f_b|$, where the f subscripts correspond to their voltage counterparts. There will be no output if any of the driving signals are disconnected.

Signal inputs V_c and V_s may have an f_c or f_s of one megahertz at the maximum. The third input, V_b, will be band-limited to 20 kilohertz, however, because of the relatively poor frequency response of the 741. □



Biased mixer. A balanced modulator can be configured to multiply three signals by introducing the third signal to the bias port. The bias current, which normally sets the dc operating point of device, is varied at an audio rate to effect linear modulation over a small dynamic range.

Hyperbolic clock inverts time

by Keith Baxter
New Haven, Conn.

Instruments designed to measure speed must contain circuits for converting a time function, t, to units of 1/t in order to calculate rate. This circuit aids in plotting the hyperbolic curve (1/t) using relatively few parts and, notably, having no need for logarithmic dividers.

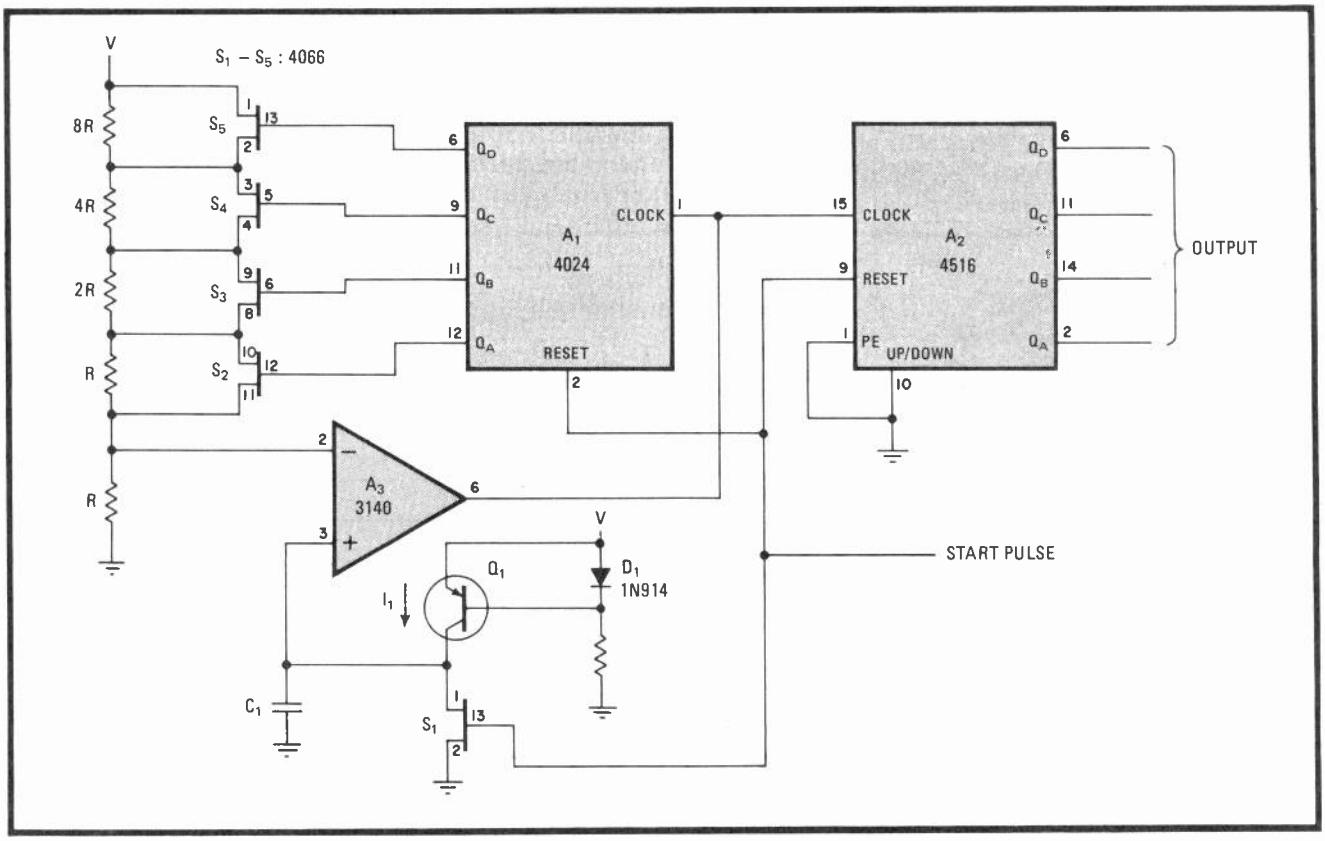
As shown in the figure, a start pulse triggers transmission gate S_1, initiating the measurement cycle. At that time, A_1 and A_2 are reset. Current I_1 thereupon charges C_1 linearly, and thus a ramp voltage is applied at the noninverting input of A_3.

When the ramp voltage reaches 1/16 volt, the potential at the lowermost tap on the resistor voltage divider A_3 moves high and advances counter A_1. At this instant, the total elapsed time is $\frac{1}{16}(C_1/I_1)$ V.

Switch S_2 is then activated, so that the second resistor in the ladder is shorted. Thus the voltage at the inverting port of A_3 increases to 1/15 v. When the ramp voltage reaches this value, A_3 again moves high and fires A_2. This action occurs at an elapsed time of $\frac{1}{15}(C_1/I_1)$ V. The process continues as A_1 counts to 15 in a binary sequence and either all combinations of the resistor ladder are shorted or the measurement cycle ends (start pulse held at logic 1). It is assumed the data will be stored in a latch prior to the start pulse, because A_2 will be reset. At that time, A_2 will have counted down with each clock from A_3 to provide an output corresponding to an elapsed time of $1/t\ (C_1/I_1)$ V, where t may assume integer values from 1 to 15. Note that comparable circuit action cannot be realized easily with an astable multivibrator operating as a fixed-frequency source for stepping A_2; that is, the circuit is not performing a time-to-frequency conversion.

The contents of A_2 at the termination of the measurement cycle provide a direct indication of an object's speed. The factor $(C_1/I_1)V$ may be adjusted to 1 by suitable choice of component values or set to a multiplicative constant as required. Also, to reduce the voltage divider increment, the resistor ladder may be expanded by cascading counters and their appropriate circuitry. □

Time twist. Circuit inverts time function, t, to 1/t in order to measure speed. Note that unit does not perform a standard time-to-frequency conversion. Ramp voltage derived from current generator is compared with resistive-ladder voltage at A_3, and A_1–A_2 are clocked each time the ramp exceeds changing ladder potential. Output of down counter, A_2, yields rate.



Optoelectronic alarm circuit is time-sensitive

by Forrest M. Mims III
San Marcos, Texas

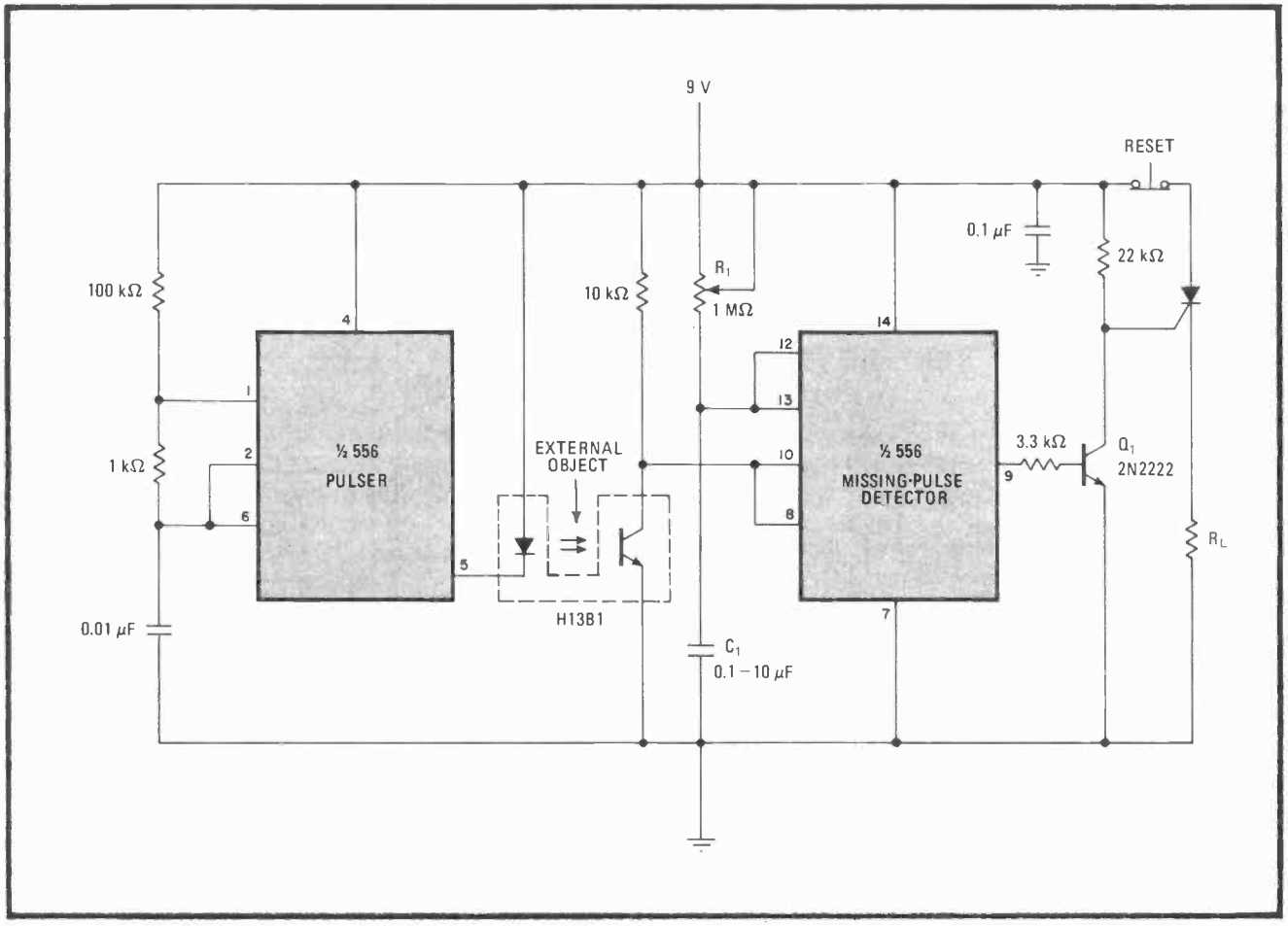
Using an optoelectronic slot switch and a 556 dual timer operating as both a pulse generator and missing-pulse detector, this circuit generates an alarm when an opaque object blocks the light input for longer than a preset time interval. It has many applications and is especially useful when united with a slotted disk to monitor motor speed stroboscopically, indicating when the steady-state rotation rate is too high or low. It can also be used on the production line for checking the width of materials.

Generally, the output of the pulser periodically activates the light-emitting diode of the H13B1 switch. Other sensors may be used; Darlington photosensing transistors, though, are the most sensitive. In this case, the pulser's operating frequency is set at 1.42 kilohertz, but it may be suitably selected by replacing the 100-kilohm resistor at pin 1 with a potentiometer.

As shown, the H13B1 is built with a slot of several millimeters separating its LED from the output phototransistor so that objects can be placed in the air gap between them. When the slot is not blocked, the phototransistor continuously resets the missing-pulse detector. Should the light path be blocked, pin 8 will remain high and the threshold voltage at pin 12 will fall at a rate determined by the adjustable R_1C_1 time constant.

Depending on the value of this constant, which can be selected for delays from microseconds to seconds, the detector will generate a step voltage if it is not reset within that period. The signal is then inverted by Q_1, which in turn fires the silicon controlled rectifier to drive the load, R_L.

Light block. Pulser operating as astable multivibrator triggers LED in slot switch so that missing-pulse detector is periodically reset. Interruptions in light beam caused by external object cut off reset pulses, causing circuit to generate alarm if interval exceeds preset time.



Digital phase meter displays angles in degrees or radians

by Tagore J. John
Meerut, Uttar Pradesh, India

In this unit, the phase angle between two signals is measured and displayed digitally, and so the instrument is less costly than its counterparts that use precision linear circuits and expensive meter movements. The angle can be displayed in degrees, radians, or grads (400 grads = 360°). The accuracy of the instrument is ±1 least significant count, independent of signal differences in amplitude or wave shape.

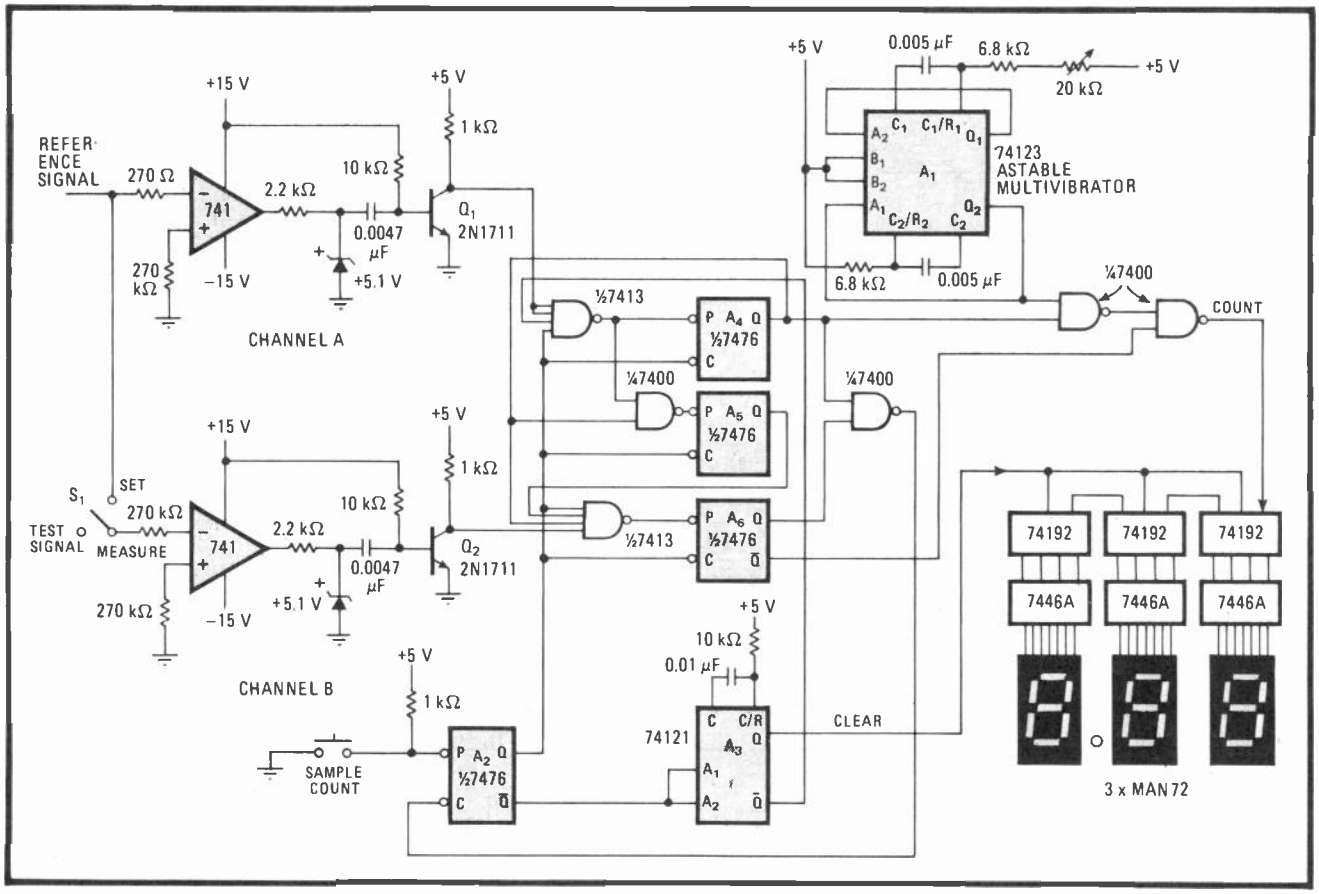
Generally, the reference and test signals are applied to channel A and channel B, respectively, as shown in the figure. Q_1 and Q_2 generate short pulses (i.e. less than 30 microseconds) to the counting logic as each signal passes upward through its zero-crossing point. To initiate the counting cycle, the logic circuit simply gates the output of an oscillator through to the 74192 counters on the first zero-crossing pulse from Q_1. The zero-crossing pulse from Q_2 terminates the count. The number displayed thus represents the phase difference expressed in the desired units, provided A_1's frequency is appropriately selected.

The instrument is calibrated by placing S_1 in the set position, introducing a reference signal, and depressing the sample-count push button as A_1 is adjusted for a display output of 360 (if output in degrees is desired), 400 (in grads), or 628 (in radians).

In normal operation, depressing the sample-count push button initiates the count cycle. Flip-flop A_2 is preset and fires one-shot A_3, whereupon the display is cleared.

Q_1's first pulse sets flip-flops A_4 and A_5 and gates A_1's output through to the 74192 counters. With a pulse from Q_2, flip-flop A_6 is set, and the output of the NAND gate driving the counters is disabled. Meanwhile, A_2 is cleared in order that the unit may then be readied for a new sample count.

The phase angles will be displayed directly. Provision should be made, however, for activating the decimal point to the right of the left-most digit when radians are displayed. □



Digital differential. Phase angle between two signals is determined to within ±1 least significant count. Using standard chips, angle is digitally measured and can be displayed in degrees, radians, or grads, provided frequency of counting oscillator, A_1, is appropriately selected.

Single-step exerciser aids 8085 debugging

by Scott Nintzel
Medtronic Inc., Minneapolis, Minn.

The ability to step through a microprocessor-based program is a virtual necessity during its debug and test phases. But certain processors, such as the 8085, require a minimum input frequency of 1 megahertz, so that stepping cannot be achieved merely by using a clock whose frequency corresponds to the rate at which the user wishes to move through the program. With two flip-flops, some logic, and a simple switch arrangement, however, single-stepping can be carried through without disturbing the basic operation of the processor.

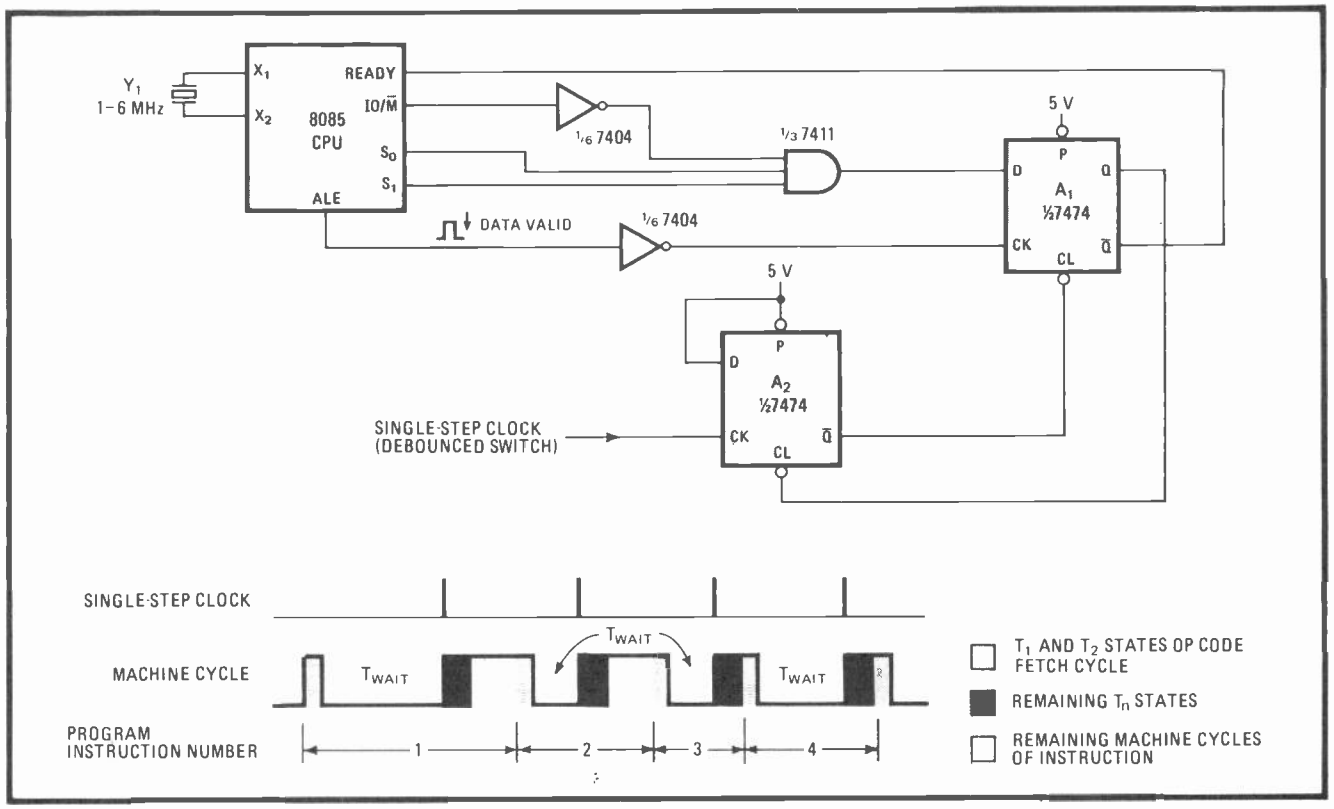
Every 8085 instruction requires at least one machine cycle, each of which in turn consists of several parts known as T states. The first cycle of each instruction is referred to as the op code fetch cycle. Single-step operation can be attained by adding an integral number of waiting cycles or T_{wait} states to the op code fetch cycle with the single-step circuitry.

Operation is clarified in the figure and the timing diagram. Immediately after a system reset, the central processing unit of the 8085 processes the first program instruction through state T_2 of the op code fetch. The address-latch enable (ALE) line then moves low.

Lines IO/$\overline{M}$, S_0, and S_1 of the CPU are examined at this time. Because the 8085 is in the fetch portion of the cycle, IO/$\overline{M}$ will be low and S_0–S_1 will be high, so flip-flop A_1 will be set. Thus the CPU's ready line will be brought low, and the 8085 will enter the wait state. Therefore, in the initial case, instruction 1 of the program will not be completed until a single-step command is received.

Then, A_2 clears A_1, the ready line is brought high, and the remaining T_n states and machine cycles are executed, as are the T_1 and T_2 states of the next instruction cycle. At this time, the machine reenters the T_{wait} state and remains there until cleared, as discussed previously.

A debounced switch or slow-running clock made from gates can be used to generate the single-step command, and total chip count for the unit should not exceed three ICs. Note that A_2 is required to ensure that A_1 clears quickly enough to allow capture of the subsequent fetch cycle. Without A_2, the pulse width of the single-step clock might be too long, and disturb the setting of A_1. □



Walking through. Simple single-step controller for debugging 8085 routines places CPU in wait state between program instructions. Processor is made to execute last part of one instruction and first part of next before halting, thereby advancing one location at a time.

Electronic sink simulates load for testing power supplies

by Henry Santana
Hewlett Packard Co., Loveland Instrument Division, Loveland, Colo.

The bank of bulky, high-power load resistors normally required to check the current-delivery capability of various power supplies can be eliminated by this programmable load. Able to simulate an equivalent resistance as low as a few milliohms and handle input powers up to 50 watts, this compact unit, which uses operational amplifiers and transistors to limit the amount of current it will sink, serves as a good general-purpose device for production-line testing. It can be built for $40.

The idea behind the circuit is explained with the aid of (a). Neglecting the on-resistance of transistor Q_1, and considering that a virtual ground exists between the inverting and noninverting inputs of operational amplifier A_1:

$$V_1 = V_{in} = K\alpha V_2 \qquad 0<\alpha<1 \qquad (1)$$

where K represents the gain of A_2, α is selected by a potentiometer, and V_2 is a floating supply required to maintain the necessary bias on the control transistor. Also note that $V_2 = I_{in}R_a$. When this expression is substituted in Eq. 1, it is seen that:

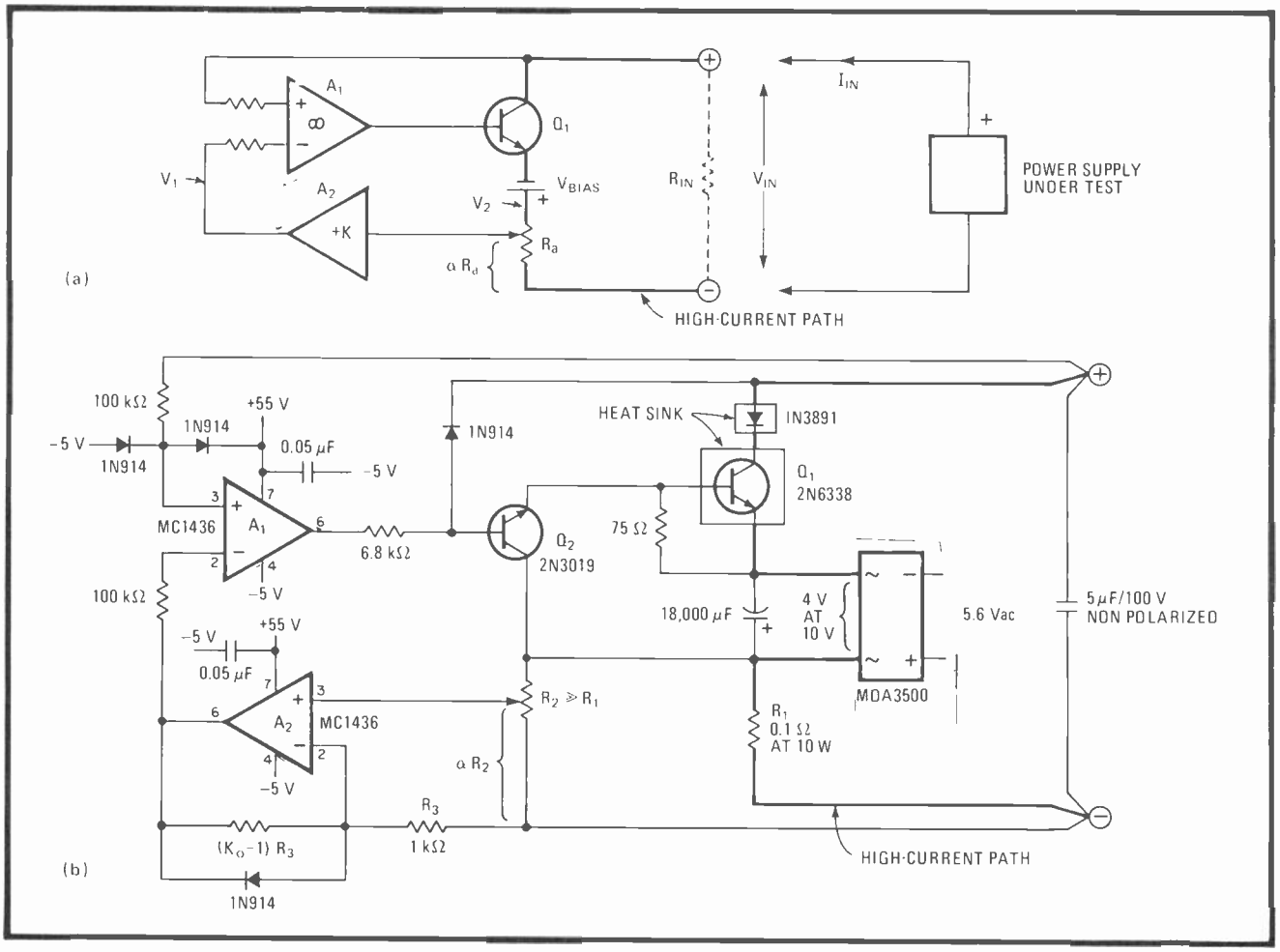
$$R_{in} = V_{in}/I_{in} = K\alpha R_a \qquad (2)$$

and therefore the resistance seen by the power supply under test can be set by R_a.

The circuit required to implement the idealized configuration is shown in (b). High-voltage op amps are used for A_1 and A_2 to handle the large input potentials expected. Q_2 has been added in order to supply adequate drive current to the output (control) transistor. R_a in (a) is represented by R_1 and R_2 in (b), where the value of R_1 is made small in order to minimize the voltage (V_2) needed to bias the control transistor.

If the gain of A_2 is selected for K = 500, R_{in} can be made to vary from approximately 0 to 50 ohms. If R_2 can be selected digitally, any resistor value in this range can be automatically ordered up. The unit can withstand a maximum input voltage of 50 volts and input currents up to 10 amperes, though the maximum input power cannot exceed 50 watts, as mentioned previously.

The components in the path of high current should be mounted on suitable heat sinks, for the power dissipated is approximately $P_d = (5 + V_{in})I_{in}$. □



Equivalent resistor. Suitably configured op amp and power transistor combination (a) will function as a programmable electronic load. Practical implementation of idealized circuit is shown in (b). Unit handles a maximum power input of 50 watts.

Single a-d converter cuts cost of droopless sample-and-hold

by Carl Andren
Harris Corp., Electronics Systems Division, Melbourne, Fla.

Because leakage currents cause droop, sample-and-hold circuits with capacitors as storage elements cannot retain a sampled voltage indefinitely. This is the major reason designers, to improve sample-and-hold performance, have resorted to converters combining analog-to-digital and digital-to-analog converter functions. But a single a-d device can be made to perform both functions alternately, thus cutting the cost and complexity of the two-converter scheme. Only one operational amplifier and a solid-state switch are needed in addition.

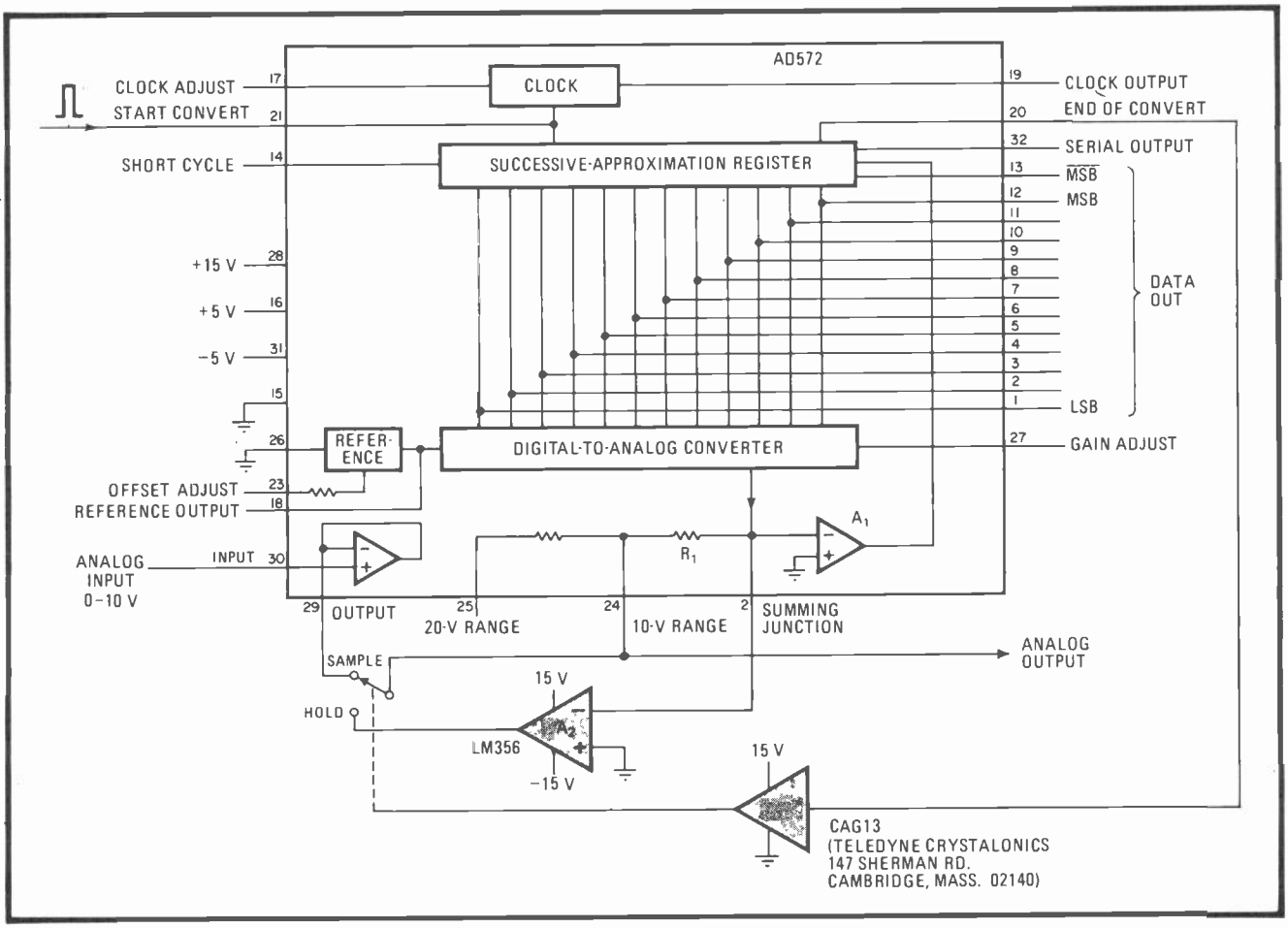
The more popular forms of a-d converter use a successive-approximation register that—with the aid of a self-contained comparator and a d-a converter—generates a digital estimate of the sampled analog voltage. When the comparison has been approximated to the least significant bit, the measurement is ended and an end-of-conversion signal is generated. If the unit is then configured as a latched d-a converter, the sampled analog voltage may be recovered and held indefinitely (assuming that one input of the comparator is accessible).

As shown, in the normal a-d conversion mode of a representative device like the AD582, a start-convert pulse initiates the measurement. An analog voltage, applied across resistor R_1 in the summing junction of comparator A_1, can then be sampled.

The successive-approximation register generates a 12-bit equivalent of the analog voltage and also drives the d-a converter that is connected to A_1's summing junction. The d-a converter then attempts to null A_1's output, whereupon the end-of-conversion signal (EOC) is generated. The sampling period takes a nominal time of 2.5 microseconds.

In this circuit, the EOC signal energizes a solid-state relay (CAG13) so that the converter can be switched to the holding mode. R_1 is then placed at the output of an op amp, A_2.

A_2's output maintains A_1's summing junction at a voltage null so that the output voltage becomes the potential across R_1—that is, the sampled voltage. Note that the switch resistance and A_2's input-bias current are taken into consideration for both modes and therefore they are not, for all practical purposes, sources of error in the measurement. □



Inverting the converting. This analog-to-digital converter, when it is combined with an op amp and switch, can provide d-a function on the hold portion of sample-and-hold cycle, thereby reducing cost and complexity of the usual two-converter (a-d–d-a) scheme. No sampling-peak capacitor is required in the converter sampling technique, so that the sample-voltage droop is eliminated.

Gray-code counter steps torque motor

by Thomas L. Clarke
Miami, Fla.

The positional accuracy of a simple stepping-motor system is limited by the response of its mechanical drive. This drawback can be eliminated electronically by using a position sensor and a counter working in Gray code to control the motor. The mechanical-drive circuit can be simplified with digital logic to reduce system errors and nonlinearities. A four-state Gray-code counter enables the system to move smoothly from its starting point to the desired position.

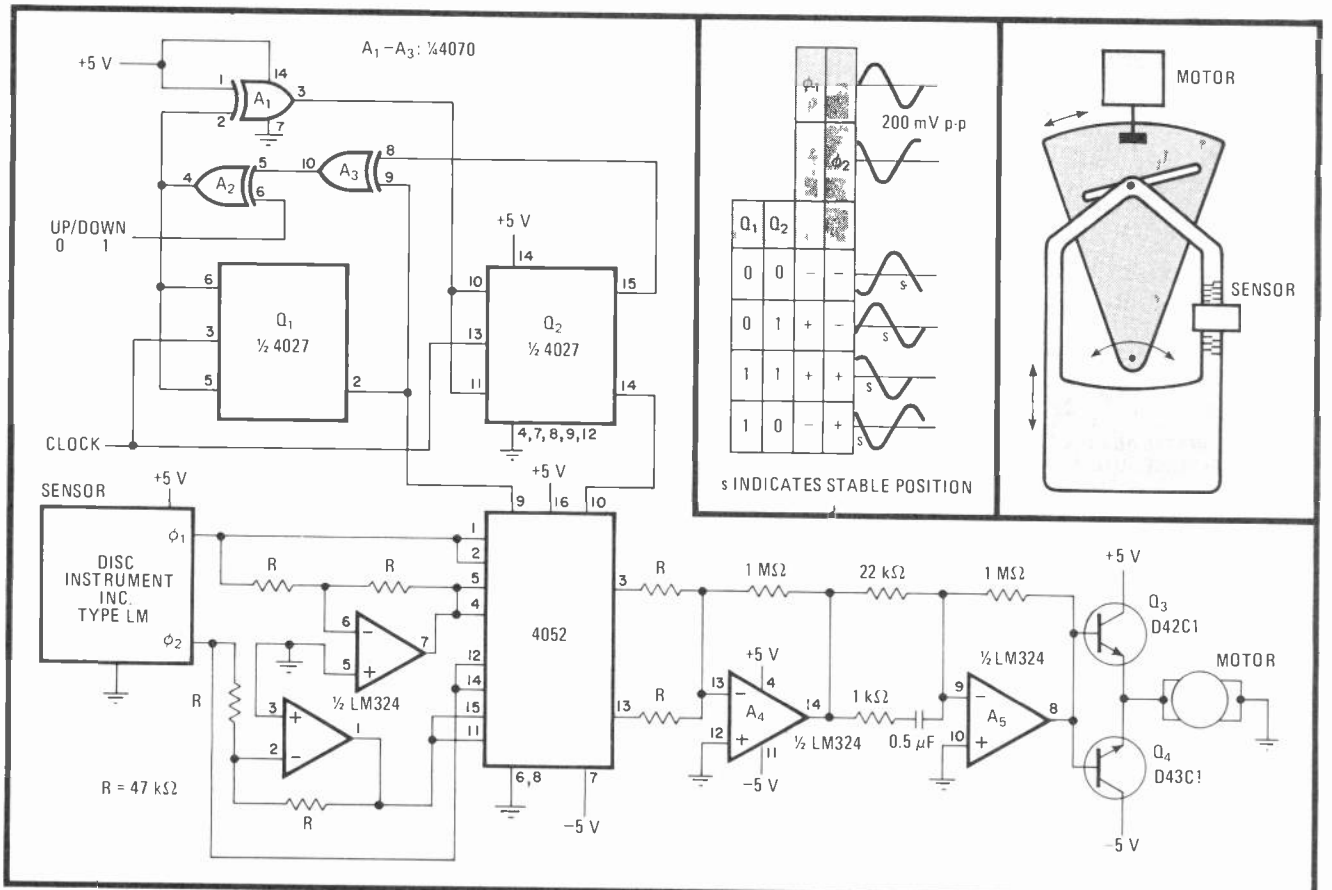
In this circuit, the summed quadrature outputs of a photoelectric sensor and the counter (see inset) set the position of the system. With suitable clock signals, the counter is advanced one location, causing the motor's position to change and the output from the sensor to vary accordingly. Thus the system is rotated 90° for each clock signal.

This circuit is intended for visual setting of a desired position through manual control of the clock and up/down inputs. For automatic tracking, the sensor's output must be compared to the desired position with additional circuitry in order to generate those signals.

Flip-flops Q_1 and Q_2 and exclusive-OR gates A_1–A_3 comprise the up-down Gray-code counter. The direction of the counting is determined by the logic state at the up/down input.

The output of the counter changes on the positive transition of each clock pulse. Depending upon the state of the counter, either the normal or inverted sine-wave outputs of the sensor are summed at the output of the 4052 four-input multiplexer. As a consequence, the output from A_4 forces the system to a new position, which is reflected at the sensor as its output steps a quarter cycle. The motor is driven through Q_3 and Q_4 by a positional signal that progressively advances or recedes (depending upon the state of the up/down counter) by a quarter cycle.

A minimum settling time of a few milliseconds is set for the system by the lead-compensation components between stages A_4 and A_5. Lead compensation is required in this situation because the system response is that of a double integration network that acts to saturate Q_3 and Q_4. The open loop would tend to be sluggish without the lead compensation, which reduces the effective system gain at low frequencies. □

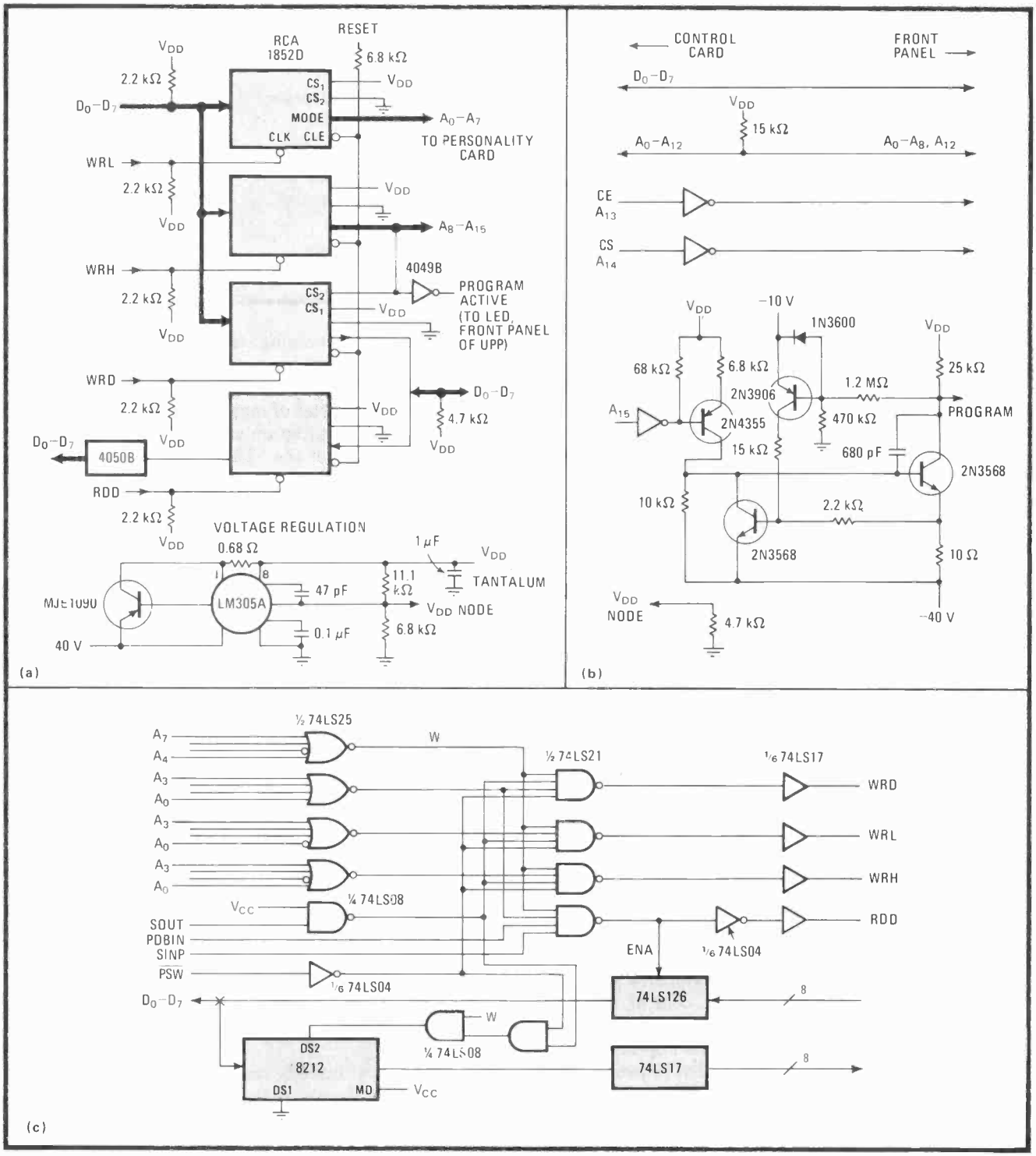


Smooth. Four-state Gray-code counter Q_1–Q_2 provides signal that, when summed with output of optical sensor by 4052 multiplexer and op amp A_4, generates quadrature output for smooth stepping of motor in quarter-cycle increments. Compensation network between A_4 and A_5 prevents saturation of Q_3 and Q_4, eliminating sluggish system response by reducing effective gain at low frequencies.

Software-based controller simplifies PROM programmer

by R. F. Hobson
Simon Fraser University, Burnaby, British Columbia, Canada

While Intel's popular Universal PROM Programmer (UPP) works effectively in its intended capacity as a system development tool, it has two major drawbacks. First, the so-called personality cards that are required for manually programming each type of programmable read-only memory are expensive and much too complicated to build. Second, it is restricted to Intel PROMs, so that the newer complementary-MOS erasable-PROM



Burning softly. Complexity of control board (a) and personality cards (b) in universal PROM programmer are reduced if software-based controller leads system's host computer through various read/write burn-in phases. Personality card is shown for the IM6604 PROM. S-100 bus interface (c) units UPP to 8080 host processor. Small program (table) guides 8080 through write-and-verify sequence.

WRITE-AND-VERIFY SEQUENCE: IM6604 E-PROM

Write/Verify Routine

Statement			Comment
COUNT:	DS 1		
WRITE:	PUSH	B	
	PUSH	PSW	
	CALL	DOUT	; LATCH DATA BYTE.
	XRA	A	
	STA	COUNT	; INITIALIZE COUNT.
	POP	PSW	
	CALL	ADDRL	; LATCH ADDRESS.
	CALL	INFO0	; INITIALIZE CRT.
WLP:	CALL	PULSE	; SEND A PROG PULSE.
			; VERIFY
	MOV	B,A	; SAVE DATA BYTE.
	LDA	COUNT	
	INR	A	; BUMP UP COUNT.
	STA	COUNT	
	CALL	READ	; GET CELL CONTENTS.
	CMP	B	; COMPARE WITH DATA.
JZ	BURN		; EXIT IF VERIFIED.
	CALL	INFO1	; UPDATE CRT.
	LDA	COUNT	
	CPI	030H	; PULSE LIMIT . . .
	MOV	A,B	
JC	WLP		; EXCEEDED?
	STC		; IF SO EXIT.
	POP	B	
RET			
BURN:	. . . . .		; LAST WRITE OK,
			; BURN AND EXIT.

Pulse Routine

Statement			Comment
PROG	EQU	80H	; CONTROL BIT.
PULSE:	PUSH	PSW	
	PUSH	B	
	MOV	A,D	; ADDR/CTL BYTE.
	ORI	PROG	; SET PROGRAM BIT.
	MVI	B, OEH	; SET 14MS COUNT.
	CALL	HOUT	; START PROG PULSE.
	CALL	MSDLAY	; HOLD IT.
	XRI	PROG	; CLEAR PULSE BIT.
	CALL	HOUT	; RESET PROG PULSE.
	MVI	B, 07H	; 7MS COUNT.
	CALL	MSDLAY	; WAIT (2/3 DC).
	POP	B	
	POP	PSW	
RET			

chips cannot be programmed. The personality cards can be simplified and the UPP peripheral device made more versatile, however, if a software-based controller guides the system's host computer through the various read/write phases required to program and verify the contents of PROMs.

The basic UPP interface has eight data-input and eight data-output lines, along with read-data, read-acknowledge, and read-status ports. Also included is a write-data line, a write high-address and write low-address line, and an interrupt line. A pulsed control signal required for programming each PROM location is handled via a 4-bit 4040 microprocessor on a control card in the UPP.

The best way to simplify such a peripheral is to have the host computer provide the timing, control, and logic necessary for programming, reading, and verifying the contents of PROMs and E-PROMs. The complexity of the UPP's control card is then reduced to that shown in (a) of the figure, where the 4040-based setup is replaced by four C-MOS I/O chips (RCA 1852D).

The host computer consequently sees one input port and three output ports. The input port is used for returning the contents of a selected memory word. Two of the output ports are used for latching address and control information; the remaining output line is used for a data-output latch.

Of the 16 PROM-address lines available, 12 are used to address up to 4 kilobytes of memory. The remaining four lines can be used for program and chip control. Consider the personality card of the 512-by-8-bit IM6604 PROM, for example (b in figure). There, line A_{15} is used for a program pulse enable, A_{14} and A_{13} are used for chip select and chip enable, respectively, while line A_{12} is used for a strobe pulse. The popular 27XX E-PROM series would require only two control lines. Because the 27XX chips are powered by 5 volts, while C-MOS devices require 10 V for programming, the 27XX's personality card would interface to the host computer through open-collector devices.

In general, then, a personality card will consist of a bidirectional data bus, the required number of address lines, and a pulser circuit. It is thus used mainly to route the bus lines to the proper front-panel pin positions on the UPP. The pulse circuit must be designed to be reset by the UPP's front-panel reset button. This can be accomplished by connecting the reset line to the 1852D's CLE inputs. For completeness, the program control line (on the control card) is also connected to the program LED on the front panel.

A typical S-100 bus interface for the modified UPP is shown in (c). I/O ports 32, 33, and 34 have been decoded for a data strobe (read), write low-address, and write high-address, respectively. Interface software must include a timing subroutine and program pulse and verification routines particular to the PROM that is programmed.

As for the programming required, the sequence in the table outlines the steps necessary for the write-and-verify operation in the IM6604. The program is written for the host 8080A microprocessor. □

What to look for in logic timing analyzers

More channels, assorted speeds, display options, novel triggering schemes ensure there's an instrument for every digital timing problem

by Martin Marshall, *Marshall Enterprises, San Francisco, Calif.*

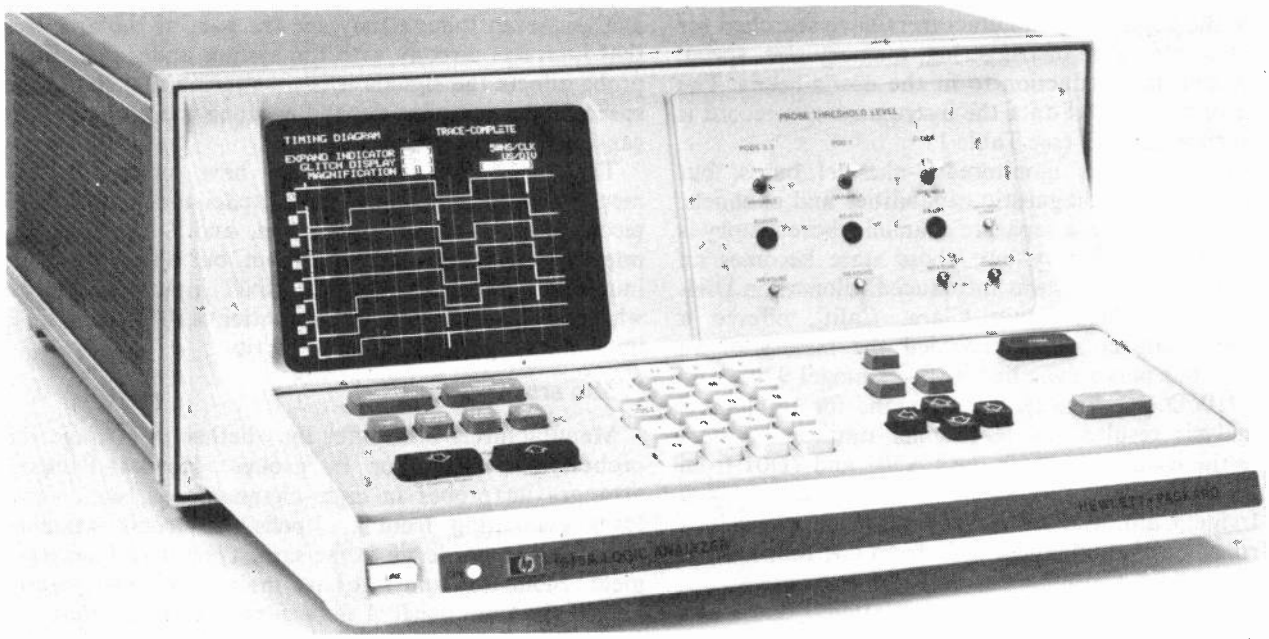
☐ Logic timing analyzers have learned a lot of new tricks in the six short years of their existence. From the start their high-speed asynchronous clocking marked them as the instruments of choice for solving hardware-related problems like short-duration glitches, skewed signal arrival, and intermittent timing failures. Software troubles are usually taken on with logic state analyzers that synchronize their clocking with the clock of the system being tested and thus are 5 to 10 times slower. But sometimes problems that appear to be software-generated are in fact hardware-related and require the more detailed analysis possible with the faster asynchronous instrument.

Small time windows

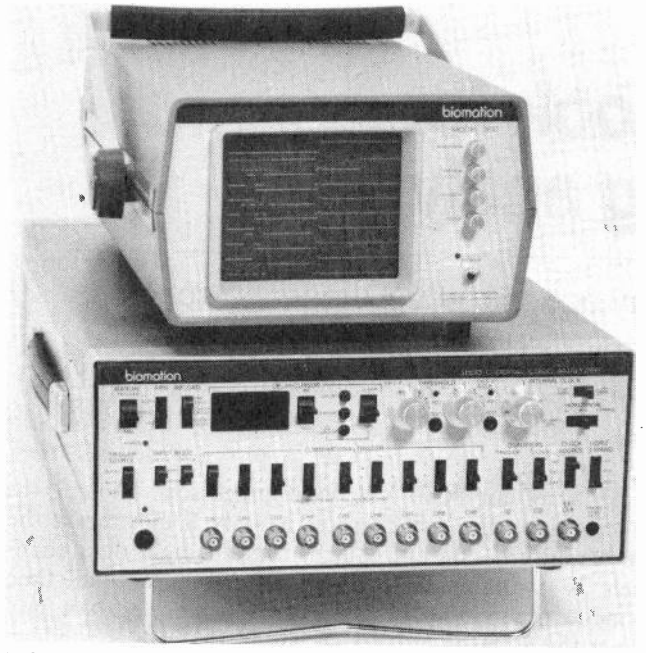
Most currently available logic timing analyzers are capable of both synchronous and faster asynchronous operation. In either mode, the analyzer monitors digital signals on address, data, or control lines, confirming proper word construction on a bit-by-bit basis.

An example of the need for a timing analyzer's inherent speed advantage appears upon examining the status activity of an 8080-type microprocessor. Though the microprocessor itself operates at only 2 megahertz the status information multiplexed onto its eight data channels is available only within a 50-nanosecond time window occurring between system clock cycles. Not only must the 8 status bits arrive within that 50-ns window, but two sync lines must change state as well. To examine the skew of these signals properly, the 50-ns interval should be broken down into five 10-ns samples. This is possible only if the analyzer is running at a 100-MHz sampling rate. A state analyzer running synchronously at 2 MHz cannot perform this kind of analysis, as the skew of the signals would not be magnified sufficiently.

Examining the timing relationships of a microprocessor to its peripheral chips, or of timing within non-microprocessor-based systems, brings up further examples. Even a slower microprocessor such as the 1-MHz 6800 chip features input/output data hold times in the 10-ns range. Faster, newer chips like Nippon Electric's high-speed version of the Advanced Micro Devices AMD 2900 can be added to the list of examples. Such a bipolar chip, with its 60-ns instruction cycle time,



1. Grabbing the glitch. In addition to data, the timing analyzer displays fast transients or glitches that can affect the system's operation. The glitch detection circuit stretches the duration to one sampling interval. Glitches can be seen above at the center and right side of the CRT.



2. Separate CRT. Logic analyzers often require an oscilloscope or a separate CRT for timing display. The 100-MHz Biomation 9100 D offers eight data channels, a sync channel, and choice of clock or trigger qualifier channels. It has a word depth of 1,024 words.

demands the high speed of the timing analyzer.

Another advantage timing analyzers have over most state analyzers is their ability to detect glitches. These infrequent transients are too short for detection at synchronous sampling times, but they affect system operation nonetheless. Special latching circuitry detects glitches as short as 5 ns in duration and stretches the transients to one sample interval for recording by the analyzer. Figure 1 shows several waveforms containing glitches captured and displayed using this circuitry.

Evolution of the timing analyzer

Since the beginning, manufacturers have searched for the best combination of triggering, memory size, speed, display, and data reduction to fit the user's needs. The number of channels of data the instrument can record is also of prime concern (see Table 1).

The earliest units monitored 8-channel buses, but users needed more diagnostic capabilities and channels. The trigger qualifier, a separate channel whose history is not recorded in memory but whose state becomes an added trigger criterion, was introduced. Biomation Division of Gould Inc., Santa Clara, Calif., offered a 9-channel analyzer which recorded the history of an 8-channel bus plus a sync line, with its model 920D and model 9100D (see Fig. 2). User demand for 16-channel bus analysis resulted in 16-channel timing analyzers such as the Biomation 1650; the LA501 and 7D01 from Tektronix Inc., Beaverton, Ore.; model 740 from Moxon Inc., Irvine, Calif.; the 50D16 from BP Instruments Inc., Cupertino, Calif.; and model 1850 from E-H International Inc., Oakland, Calif.

The latest increase in channel population is due to the synthesis of timing and state analysis in the Biomation K100D and the 1615A from Hewlett-Packard Co., Colorado Springs (Colo.) division. The reason for the combination of instruments is that timing analysis need only be done on a single bus, whereas state analysis may usefully include more than one bus. The HP 1615A offers 8 channels for timing analysis and assigns 16 channels to state analysis; this allows monitoring of a 16-bit address bus plus an 8-bit data bus.

The K100D's 16 channels can perform timing and/or state analysis; with an optional adapter, the unit can be configured as a 32-channel data domain instrument. This permits the monitoring of a 16-bit address bus and a 16-bit data bus, or an address bus, an 8-bit data bus, and various control lines within the system.

How fast is fast enough?

Manufacturers have differed on how fast a timing analyzer should be, with some even presenting the user with a choice of speeds in different products. The first timing analyzers operated at 10 MHz, but none manufactured since then are slower than 20 MHz. Today's units run at 20, 50, 100, or even 200 MHz—which is the proper selection? The answer, of course, depends upon the speed of the equipment that the user wishes to analyze. The user must determine the minimum time interval to be resolved in the system. Often skew factors in the hardware logic of the system, rather than the clock rate presented on the bus, determine this figure.

If that minimum interval is 50 ns, then a 20-MHz analyzer such as the HP 1615A, Biomation 920D, or Moxon 740 (Fig. 3) is the answer. If it is 20 ns, then one of the 50-MHz analyzers such as the Biomation 1650, E-H 1850, or E-H 1320 can be considered. At 10 ns there is the 100-MHz Biomation K100D and Biomation 9100D; and at 5 ns, or 200 MHz, the Biomation 8200. The Tektronix plug-in timing analyzer, model 7D01, is chameleon-like with respect to speed. It is configurable for 20 MHz on 16 channels, 50 MHz on 8 channels, or 100 MHz on 4 channels.

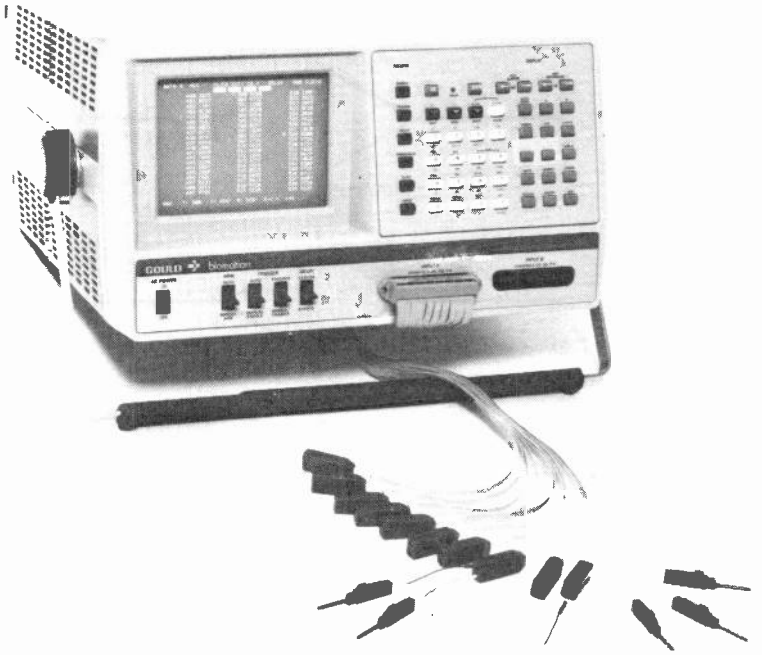
Probes are sometimes a forgotten component of logic analysis, even though they are the part of the analyzer that interacts directly with the system under test. Each probe affects the signals it is monitoring and limits the speed of the analyzer, depending upon the probe's input capacitance and impedance.

The faster timing analyzers have probes in the megohm impedance range and capacitances of 5 to 15 picofarads. Tektronix, Biomation, and E-H all specify impedances higher than 1 megohm, but E-H specifies its impedance at the analyzer's BNC input connectors, whereas Tektronix and the Biomation K100D have their impedances specified at the probe tip.

Probe arrangement

Manufacturers also differ on whether to arrange the probes individually or in groups. Hewlett-Packard arranges its probes in eight-channel pods, with short leads emanating from the pods; Tektronix attaches somewhat longer leads to the same type of pod arrangement. Biomation and E-H have individual probes beginning at the front panel of the analyzer, claiming that this allows easier connection of physically divergent parts of the system at the same time. Tektronix and Biomation

3. Analyzers evolve. This Moxon 740 timing analyzer can monitor up to 16 channels of data at a 20-MHz sampling rate. The elimination of numerous front-panel switches and addition of a CRT were two evolutionary changes in logic analyzer design.



4. Hybrid probes. Each Biomation K100D probe has a hybrid circuit providing a high-impedance input for high-speed signal monitoring. The K100D performs state as well as timing analysis and features an extensive array of triggering and display capabilities.

K100D analyzers reduce the degradation of high-speed signals by using hybrid circuits close to the point of probing. Tektronix places the hybrid circuitry in the probe pod; the K100D puts one in the tip of each individual probe (Fig. 4).

Triggering is the key

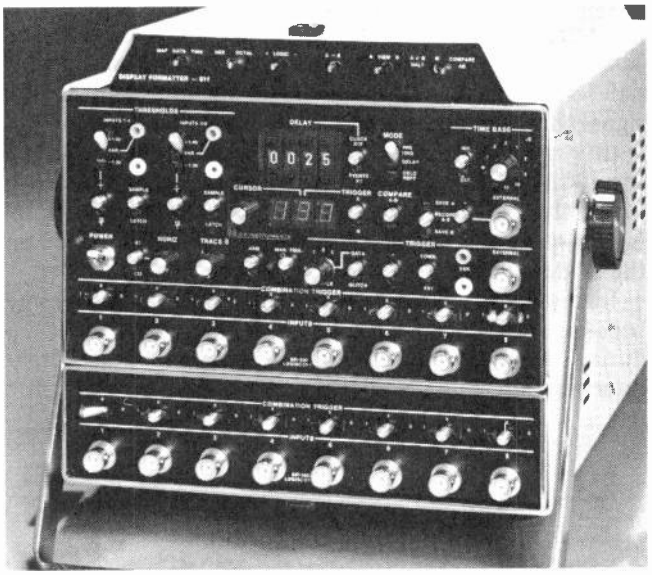
Although speed is a major factor in excluding some timing analyzers, final selection requires evaluating the analyzer's ability to trigger, its ease of use, and its ability to reduce the captured data into an intelligible display. The first of these criteria, triggering, has become an art form nearly as sophisticated as the programming techniques it unravels.

The earliest and simplest triggering criterion is the parallel word trigger. All of the analyzers have it. If the analyzer is connected to a 16-bit address bus and the selected trigger word comes along, the analyzer stops recording and its memory stores pretrigger information up to its capacity.

Clock delay was the next feature added. With it, the user can examine the program in blocks, using the same trigger word. Examining sequential blocks of program is made possible by increasing the clock delay on successive analyzer recordings (Fig. 5).

However, programs invariably contain subroutine loops and even nested loops, and potential trigger words occur many times on successive passes. To allow the analyzer to pick apart these loops, a pass counter was added to the triggering section. The pass counter delays recording into memory by counting trigger word occurrences, rather than clock cycles, to allow triggering on the nth pass through a subroutine. Nearly all the latest timing analyzers have this feature.

Only two, however, can make use of on-board sequential word triggering. These are the Biomation K100D and the HP 1615A. Sequential word triggering is a very useful technique for selecting a unique program path out of a seemingly ambiguous set of paths. The analyzer will

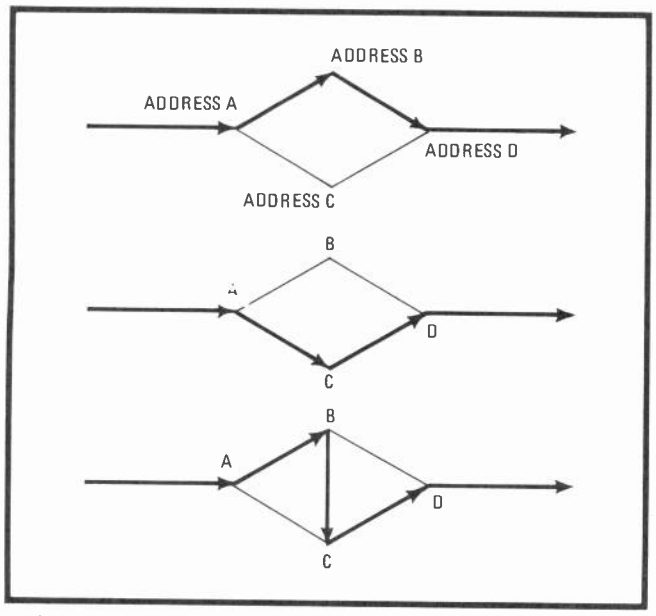


5. Trigger tactics. The BP Instruments model 50D16 16-channel timing analyzer's triggering capabilities include parallel word, clock delay, and events delay. The last two permit examination of a sequential program block or subroutines by increasing trigger delay.

trigger on word B, but only when it is preceded by word A. In hardware terms, word A arms the analyzer and word B (or the nth occurrence of word B) triggers it.

In software terms, one can picture a program path through a subroutine beginning with word A and ending with word D. Between A and D, there are three distinct paths by way of words B and C. These are ABD, ACD, and ABCD (Fig. 6). The three paths can be distinguished by triggering on sequences of words BD, AC, and BC, respectively.

In a typical application, words A, B, C, and D are



6. Separating address flow paths. Sequential triggering can be used to sort out program paths that are otherwise indistinguishable to the logic analyzer. In practice, sequential triggering can be used to define key I/O maneuvers such as a particular subroutine.

16-bit addresses in a microcomputer program. When triggered, the analyzer's memory will store a listing of the program's address flow. The K100D can take the extra step of qualifying the analyzer's trigger on sequential 18-bit words, allowing one to include control line signals in the trigger as well as a 16-bit address bus.

HP's model 1615A performs sequential triggering somewhat differently. Its 8-channel timing bus can arm its 16-channel state analysis bus, or vice versa. Triggering on successive 16-bit address words is not included on the model 1615A.

Intermittent failures are the most troublesome because they occur infrequently and do not show up during normal repetitive measurements. To combat intermittent logic problems, a number of analyzers include a trigger-on-noncomparison mode.

The mode works like this. The unit captures a normal block of data from a suspected portion of the program, using trigger criteria X, Y, and Z, and transfers it into a second reference memory inside the analyzer. Next, using the noncomparison mode, the analyzer will first wait for data that meets criteria XYZ. When that data arrives, it will compare the captured data with the normal data in its reference memory. If the data is different, the instrument triggers. If not, it re-arms itself and waits for criteria XYZ to recur.

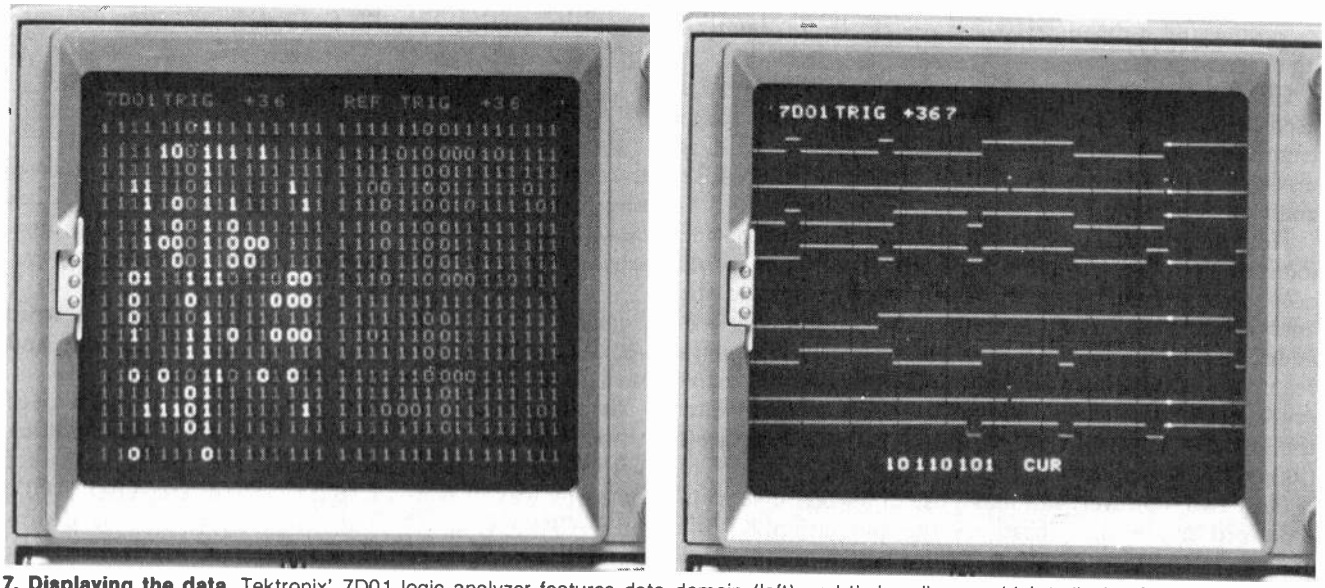
Reducing the captured data

Biomation's K100D adds a useful twist to this process. It can define both the channel width and the word depth of the memory used for comparison. For example, suppose an unusual combination of data in subroutine A is suspected of causing a jump to an incorrect address. If the data in subroutine A is always changing, then it is possible to limit the comparison to just the 16 address channels, even though the analyzer is simultaneously recording the data bus.

Next, given that subroutine A is 103 addresses long, the comparison can be limited to just those 103 words in the reference memory. This is most useful in the likely case that subroutine A is accessed from any of a number of different places and exits into other subroutines. In other analyzers, the length of the comparison memory is fixed, but the number of channels compared can still be limited very simply by pulling the probes off the unwanted channels.

Trigger on disappearance

Another convenient triggering feature shared by the E-H 1850 and Biomation K100D is the ability to trigger on either the appearance or disappearance of the trigger word. This is helpful in triggering on the end of a message using the system's message-valid signals. For example, it may be that three control lines must go high in order that a peripheral device receive a message on a



7. Displaying the data. Tektronix' 7D01 logic analyzer features data domain (left) and timing diagram (right) display formats. It offers a vertical line, or cursor—the bit makeup of the data word it intersects is displayed at bottom (right). Trigger word position reads out at top.

LOGIC TIMING ANALYZERS COMPARED

Manufacturer and model	Maximum speed (MHz)	Channels	Memory depth (words)	Triggering: 1st appearance or disappearance	Triggering: Clock delay	Triggering: Event delay	Triggering: Parallel word	Triggering: Sequential word	Triggering: No. clock qualifiers	Triggering: No. trigger qualifiers	Reference memory	Digital holdoff (samples/time)	Built-in CRT	Display format
Biomation K100D	100	16[a,b]	1,024	yes	yes	yes	yes	yes	2	2	yes	14 samples	yes	T, A, B, O, H, S
920	20	9	256	no	yes	yes	yes	no	1	1	no	none	no	T
1650/116	50	16	512	yes	yes	no	yes	no	1	2	yes	none	no	T, O, H, M
9100D	100	9	1,024	yes	yes	yes	yes	no	1	1	no	none	no	T
8200	200	8	2,048	yes	no	no	yes	no	no	no	no	none	yes	T
B P Instruments 20D	20	8	256	no	yes	no	yes	no	no	no	no	none	no	T
50D16	50	16	510[c]	yes	yes	yes	yes	no	no	5	yes	3 samples	no	T, B, O, H, M
E-H International 1850	50	18	512	yes	yes	yes	yes	no	1[g]	3[g]	yes	4 samples	no	T, B, O, H, M
Hewlett-Packard 1615A	20	8[a]	256	yes	yes	yes	yes	yes	6	no	no	15 ns to 2 μs	yes	T, B, O, H[f]
Moxon 740	20	16	64	no	yes	yes	yes	no	1	no	no	none	yes	T, B, O, H
745	20	16	1,024	no	yes	yes	yes	no	1	no	no	none	yes	T, B, O, H
Tektronix 7D01F/7704	100	4	1,016	no	yes[d]	yes[d]	yes	no	1	2	yes	10 ns to 300 ns	yes	T, B, O, H, S, M[e]
	50	8	508	no	yes[d]	yes[d]	yes	no	1	2	yes		yes	
	20	16	254	no	yes[d]	yes[d]	yes	no	1	2	yes		yes	

Notes:
[a] 16-state channels included
[b] 32-state channel option
[c] 2,046-word memory option
[d] Delay feature option
[e] ASCII character option
[f] Glitch only included
[g] With optional probe pod

T = timing
B = binary
O = octal
H = hexadecimal
M = mapping
S = search
A = ASCII

separate 8-bit data bus. To find the end of the message, the unit can be triggered when the three control lines go from 1-1-1 to any other state. The easiest way to do this is to set the analyzer to trigger on the first disappearance of the trigger word 1-1-1.

Glitch filtering

The timing analyzer's equivalent to the oscilliscope's trigger holdoff feature is called digital filtering, glitch filtering, or digital trigger holdoff. It simply requires that the trigger word remain valid for more than one sampling interval. It is especially useful when examining three-state buses or systems that are insensitive to very short glitches. In these cases one may be sampling at five times system clock speed and yet not want to generate a false trigger on a glitch that is only a fifth of a system clock interval in duration.

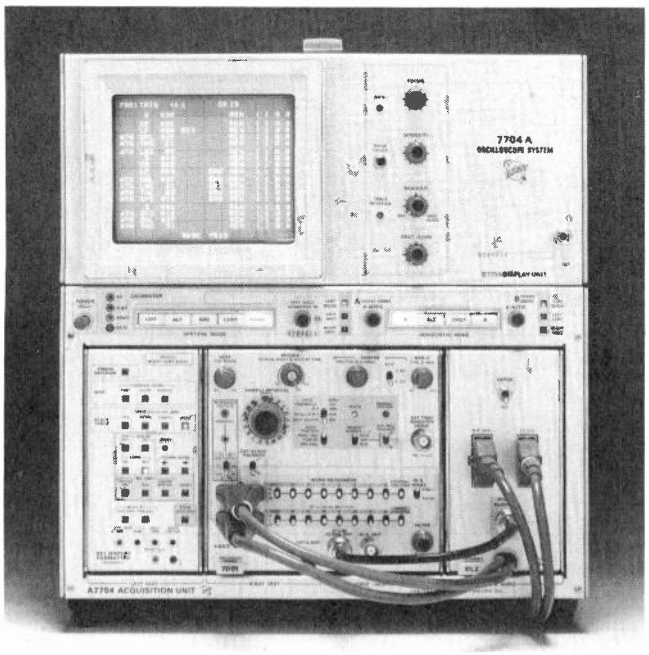
E-H's model 1850 will digitally filter a trigger word for up to 4 samples, whereas Biomation's model K100D will filter for up to 14 samples. HP's 1615A filters a trigger from 15 ns to as long as 2 microseconds; Tektronix' model 7D01 will filter from 10 to 300 ns.

Interpreting the analyzer's data often depends on the display method chosen. This means the captured data must be reduced into more convenient forms.

The first timing analyzers offered only a timing diagram display. However, manufacturers soon realized that their timing analyzers would also be used for state analysis, so they included data domain display formats such as binary, octal, and hexadecimal representations of the data (Fig. 7, left). Most timing analyzers currently available have these display modes, along with other auxiliary display features.

Cursor calculations

One of the most useful of these is the cursor. This is a vertical line superimposed on the CRT that not only helps align the raw data vertically, but is also helpful in calculations. For example, the position of the cursor in the analyzer's memory is read out digitally on the CRT (Fig. 7, right), as is the position of the trigger word. To find the time difference between two points, the cursor



8. ASCII format. The optional ASCII character display converts 7-bit ASCII information into letters, numbers, and symbols for direct interpretation of program statements. This feature is helpful in debugging software-generated problems.

position readings are subtracted after placing the cursor successively over the two points.

Biomation's model K100D has two cursors and reads out their difference in position and time directly. The two cursors are also used to define the word depth of the comparison memory for the trigger-on-noncomparison (or the comparison) mode.

Horizontal magnification in the timing diagram mode has become another standard feature. The magnification factor is displayed digitally on the CRT on the Tektronix and Hewlett-Packard models. It registers automatically on the time line transversing the middle of the Biomation K100D's CRT screen.

The time line is a row of dots showing sample intervals, with intensified dots every five markers and digital readout of the location of the first, last, and center sample displayed. Expansion factor readout is also given. Previous Biomation analyzers and the E-H model 1850, also have a horizontal expansion feature, but the magnification factor is not read out on the CRT.

ASCII display mode

An optional feature worth considering is an ASCII character display offered by both the Tektronix 7D01 and Biomation's K100D. This mode displays 7-bit ASCII information directly as ASCII characters on the CRT. The Tektronix unit uses a separate plug-in ASCII module in place of the normal formatter (Fig. 8). The K100D houses ASCII circuitry inside its mainframe.

These two analyzers also provide a search mode for scanning the analyzer's memory for a user-specified word. This feature is useful when observing the number of passes through a given subroutine, for checking access to portions of a program, and for finding unnecessarily long loops. The word can be keyed in on the K100D; the 7D01 selects it from among those words in the analyzer's reference memory.

The number of occurrences of the searched-for word is read out digitally on the K100D's CRT, and an asterisk is placed next to each such word in a data domain listing of the data. Repeatedly pushing the 7D01's search button and counting the number of button pushes on one sweep through the memory gives the number of occurrences of the searched-for word.

Strictly speaking, a logic analyzer's usefulness lies in its data acquisition and data display features. But as the analyzer's sophistication increases, so does the possibility of error in control settings. To combat this, HP, Biomation, and Moxon have gone to keyboard control of the instruments' functions, with the result that the front panel of the logic analyzers look more like computer terminals than oscilloscopes or minicomputers.

Keyboard entry complements the use of a microprocessor inside the analyzer to perform self-checking as well as calculation and display functions. On older timing analyzers, the user's memory of trigger and control settings was mechanical, indicated by the position of the switches on the front panel. Keyboard-controlled models display the settings on the CRT either in menu format, as in the HP 1615A, or in a status display mode, as in the Biomation K100D.

The microprocessor inside both units performs the housekeeping chore of making sure the key connections are operating at each startup. The Biomation K100D's microprocessor performs the additional function of controlling an error light on the instrument's front panel. It goes on whenever the operator makes a mistake in entering control settings.

Future timing analysis

From probes to display output, the logic timing analyzer has come a long way since 1973. Further improvements will probably be in the area of finding smarter ways to reduce the captured data. Perhaps data-reduction schemes such as Hewlett-Packard's signature analysis techniques [*Electronics*, March 1, 1977, p. 89] may be implemented.

Another possibility is the addition of an RS-232 interface capability so that the analyzer can be used for remote analysis. This could permit a centrally located diagnostic center to perform and interpret tests using a telephone modem. Such a center could take advantage of computer-aided diagnosis and a factory service team to locate problems remotely. The on-site technician would only be needed to position the probes.

Timing analyzers may also eventually use on-board programmable read-only memories to store previous trigger settings and comparison data tables. This would allow a measurement to be repeated by a single press of a button, avoiding the resetting of every function on a complex analyzer.

The complexity of logic timing analyzers must expand along with the complexity of the digital designs they are intended to debug. And since highly skilled personnel remain in short supply, future analyzers are bound to use microprocessors to do more and therefore ask less of their operators. □

Analog ICs divide accurately to conquer computation problems

Housed in dual in-line packages, the hybrids can multiply, divide, or take the square root

by Yu Jen Wong, *Burr-Brown Research Corp., Tucson, Ariz.*

☐ Although analog dividers are basic building blocks in a wide variety of applications, until recently they remained bulky, very limited in operating range, and prohibitively expensive. Within the past two years, though, they have profited from the kinds of technological and design advances that have characterized the progress of integrated circuits in other areas.

Now, dedicated analog dividers are available in dual in-line packages, and their low price—typically less than $20—has gone hand in hand with performance that has improved by orders of magnitude. Burr-Brown Research Corp., for instance, makes a hybrid precision divider, the 4291, with a guaranteed maximum error of less than 0.25% over a 100/1 denominator voltage. With optional external trims, the error may be held to 0.10% over a 1,000/1 range.

What is an analog divider?

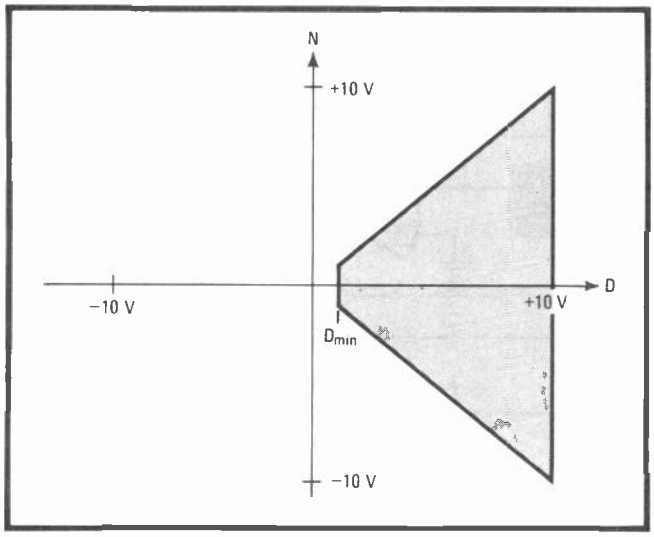
Analog dividers are widely used in such applications as ratiometric measurements, percentage computations, transducer and bridge linearization, automatic level- and gain-control systems, voltage-controlled amplifiers, and analog simulations. They may be thought of as black boxes having two inputs and one output and the transfer function given by the equation:

$$E_o = K(N/D)$$

where:

E_o = output voltage
K = a constant
N = numerator input
D = denominator input

For most commercial packaged dividers, K is internally set at 10. Since the divisor can never pass through zero, D is always unipolar. Because N can be bipolar, the divider will operate in two of the four quadrants, as shown in Fig. 1; it is therefore called a two-quadrant divider. Dividers that are designed for operation with N of one polarity are called one-quadrant dividers. At this point, no commercial four-quadrant divider exists, because it is impractical, though not impossible, to design one that would accept bipolar denominator voltages with a dead zone around zero.



1. Operating region. The shaded area represents the operating region of a two-quadrant divider. A one-quadrant divider will perform in either the top or bottom half of the shaded area. Below D_{min}, the denominator exhibits unacceptably large errors.

There are two limiting conditions for every divider. First, the absolute value of N must be smaller than that of D to prevent the output from saturating beyond 10 volts. Second, a lower limit, D_{min}, is always specified for the denominator below which the divider will exhibit unacceptably large errors. These two conditions define the operating region of a divider (the shaded area in Fig. 1). For one-quadrant dividers, the operating region is either the top or the bottom half of the operating region of a two-quadrant divider.

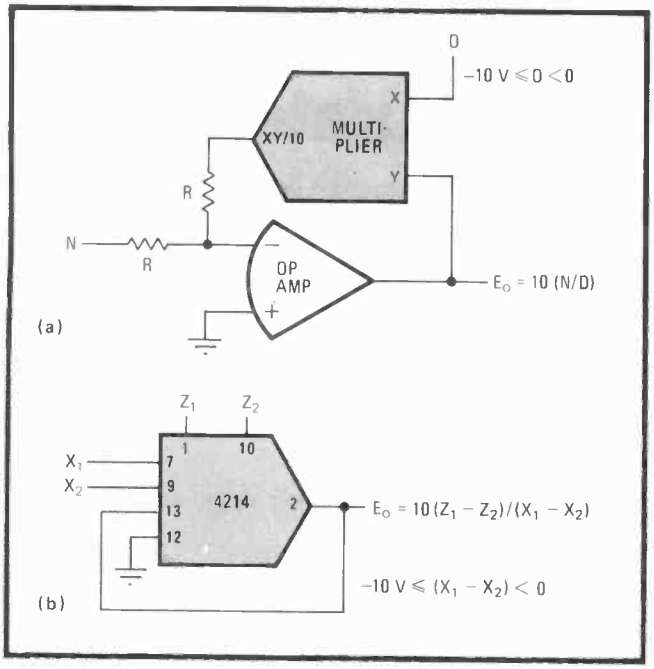
Performing division with multipliers

The oldest and perhaps still the most common method of performing analog division is to connect a multiplier in a feedback loop of an operational amplifier (Fig. 2a). An extra op amp is not needed with commercial packaged multipliers, since their output op amps can be employed through external pin connections.

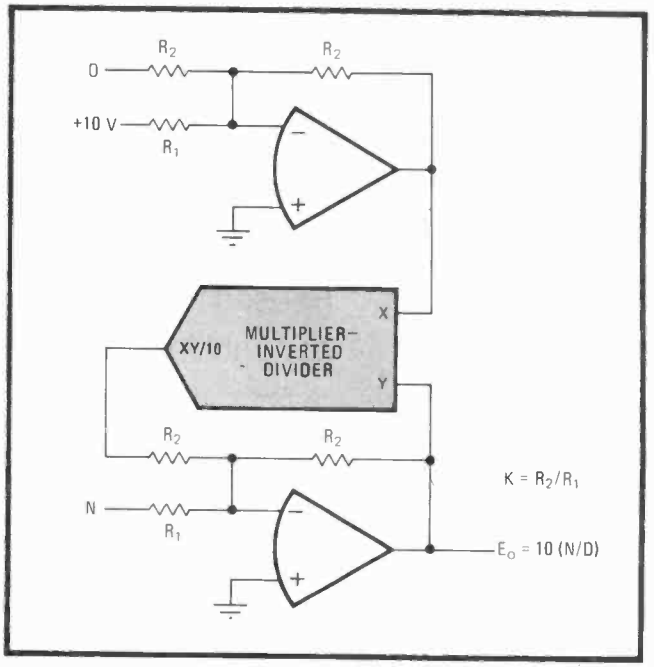
Figure 2b shows a 4214 transconductance multiplier connected as a differential divider. One limitation of the multiplier–inverted divider (MID) is its limited divisor range. The divider error that limits the ranges can be estimated by:

$$\epsilon_d \doteq 10(\epsilon_m/D)$$

where ϵ_m is the multiplier error specified by the manufac-



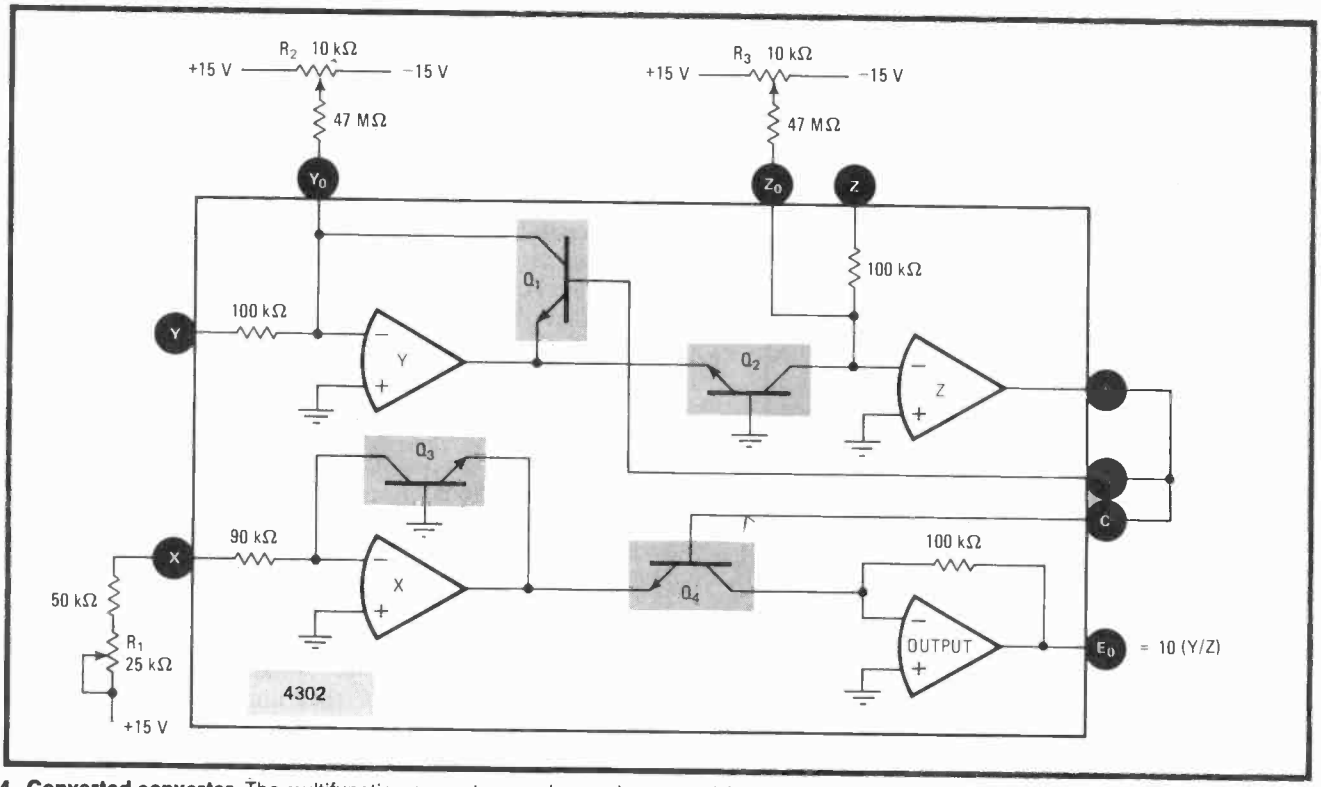
2. Economizing space. An analog divider can be constructed by connecting an analog multiplier in the feedback loop of an op amp (a). Packaged multipliers (b) do not require that extra op amp to be pin-programmed for performing division.



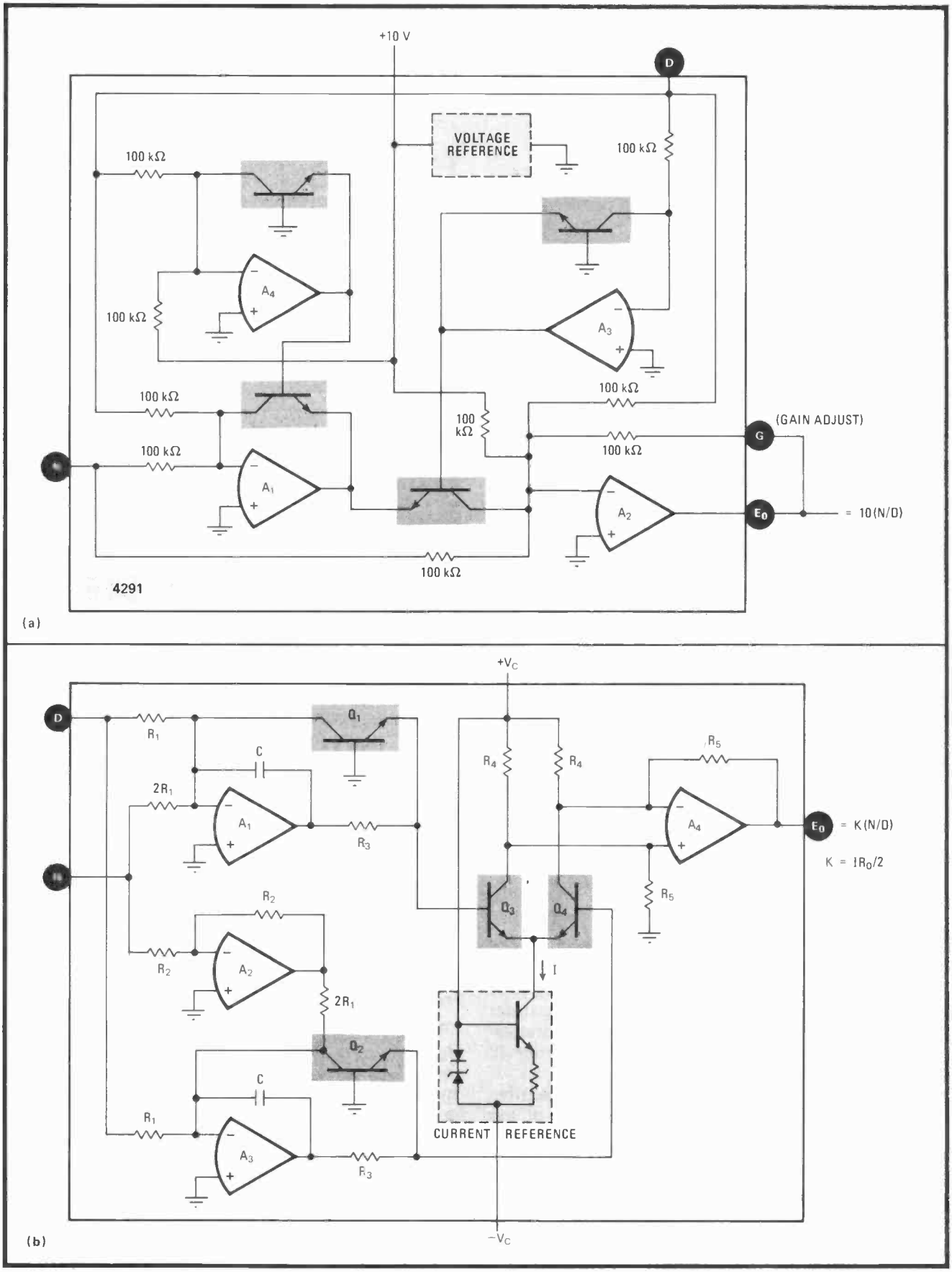
3. More accurate. The multiplier–inverted divider exhibits improved accuracy when connected in the manner shown. The error equation is given approximately by $\epsilon_d = 10\epsilon_m/(KD)$, where K is the ratio of R_2 to R_1 and can be used to optimize the divisor's range.

turer and D is the denominator voltage. With a 0.5% transconductance multiplier, the divider error will go as high as 5% when D goes down from 10 to 1 v. Hence, for practical purposes, these dividers are accurate only over a 10/1 denominator range.

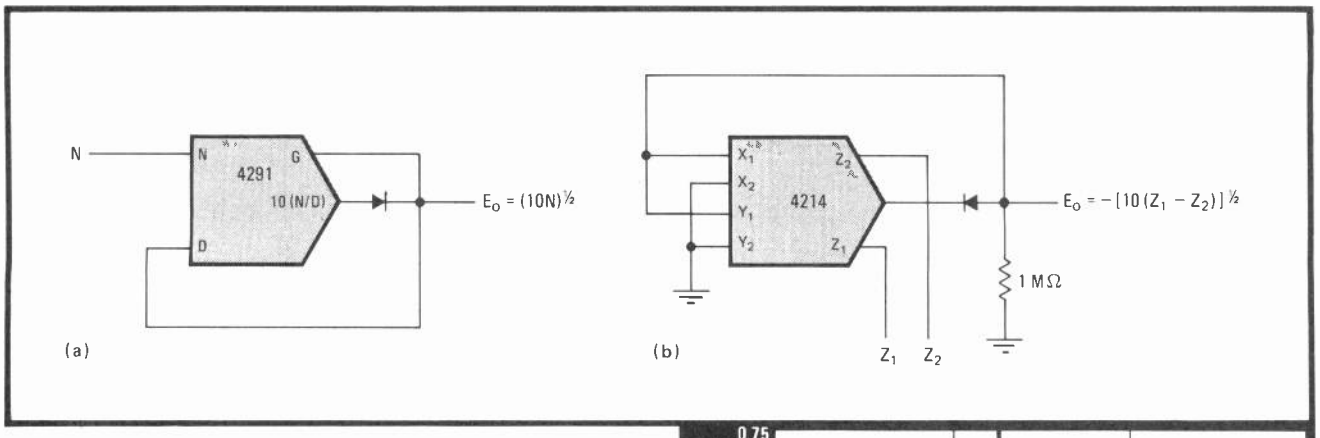
The divider error can be reduced by shifting the level of and preamplifying the divisor input and then shifting back at the output stage. In Fig. 3, with K defined by the ratio R_2/R_1, the divider error given by $\epsilon_d \doteq 10\epsilon_m/D$ will be reduced by a factor of K. However, the divisor input is thus limited to $-20/K$ volts. When $K = 2$, the divisor will swing within the same range of 0 to -10 v. In other

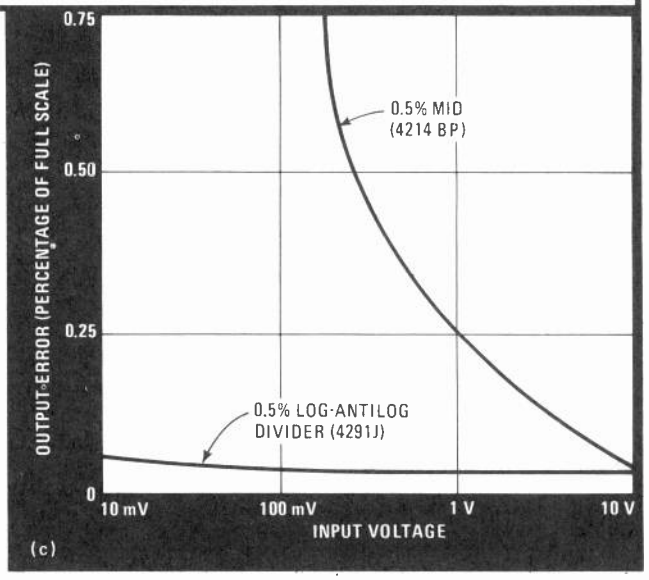


4. Converted converter. The multifunction converter may be used as a precision one-quadrant divider with a maximum error of 0.25% over a 100/1 denominator range. The maximum error can be reduced to 0.1% over a 1,000/1 range by using potentiometers R_2 and R_3.



5. Divider IC. The four op amps and the four logging transistors shown in the functional diagram (a) are rearranged and the voltage reference is replaced by a current reference to form a log-antilog divider that maintains a constant-level bandwidth with decreasing divisor voltages (b).





6. Taking the square root. Implementing either the multiplier–inverted divider (a) or the log-antilog divider (b) for finding the square root is a matter of the degree of accuracy wanted. Typical error curves for the two types are shown in the graph (c).

words, the divider error can be cut in half without sacrificing the divisor's dynamic range. With K greater than 2, say, K = 10, the divisor is limited to the range of 0 to −2 V.

One-quadrant divider

The well-known multifunction converter (MFC), through different external connections, can be used as a precision divider whose accuracy and dynamic range greatly exceed that of a multiplier–inverted divider. It is, however, good for one-quadrant operation only, whereas the MID is a two-quadrant divider.

The functional diagram of this converter is shown in Fig. 4. Its transfer function is given by:

$$E_o = X(Y/Z)^m$$

where m is determined by two external resistors and can range from 0.2 to 5. The circuit can be analyzed by applying to each of the four transistors used to achieve the logarithmic relationship, Q_1–Q_4, the Ebers-Moll equation:

$$V_{be} = (KT/q)\ln(I_c/I_s)$$

where:

V_{be} = base-to-emitter voltage
K = Boltzmann's constant (8.62×10^{-5} electron-volt/K)
T = absolute temperature
q = charge of an electron (1 eV)
I_c = collector current
I_s = emitter saturation current

Solving the equation for each of the four transistors simultaneously yields the converter's simple transfer function. This procedure assumes that the four transistors are matched, so that I_s and T are the same for all four equations.

The multifunction converter is capable of operating over a 100/1 denominator range with an error of less than 0.25%. At low input-signal levels, the offset voltages and bias currents of the Y and Z op amps contribute most of the errors. By trimming them out with potentiometers R_2 and R_3, the maximum error can be reduced to 0.1% over a 1,000/1 dynamic range. R_1 is used to trim out gain errors.

The 4291 analog divider has been optimized as a log-antilog divider. It is specified to be the most accurate two-quadrant, self-contained divider available in IC form. It operates in principle very similarly to a multifunction converter, but has several additional features. For one, it contains an internal level-shifting circuit for two-quadrant operation. For another, it is laser-trimmed to hold total error to less than 0.25% over a 100/1 dynamic range. In addition, both linearity compensation and an on-board temperature-compensated reference are provided.

Precise for two quadrants

The divider's functional circuit diagram is given in Fig. 5a. Q_1–Q_4 are the four logging transistors, which are always laid out on a monolithic chip along a thermal equilibrium line. Their geometries are specially designed for maximum conformity to a logarithmic output. In fact, log-conformity error is less than 0.05% over four decades of collector current from 100 microamperes to 10 nanoamperes. Thus, the divider can maintain its accuracy over many decades of denominator voltages.

The error sources at low input levels are mainly due to the offset voltages and bias currents of the numerator and denominator input op amps, and not to the logging transistors. Optional trims are usually provided by manufacturers in order to eliminate the offsets and bias

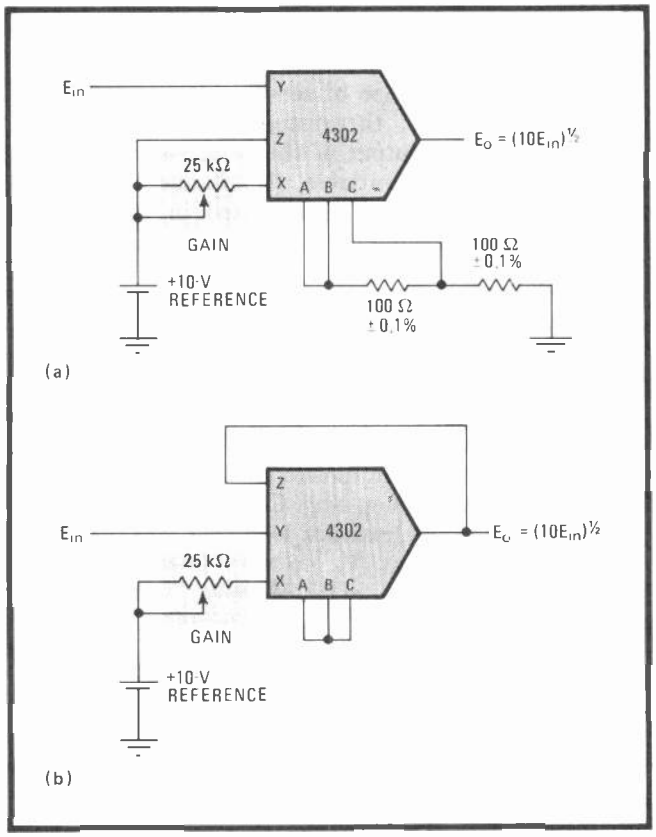
currents that are inherent in all op amps.

As with the multifunction converter and the multiplier–inverted divider, the bandwidth of the log-antilog divider decreases almost linearly with divisor voltage level; for example, a 400-kilohertz divider at a 10-V divisor voltage will become a 4-kHz divider at a 100-microvolt divisor voltage. By rearranging the four logging transistors and the four op amps and replacing the voltage reference by a current reference, a log-antilog divider whose bandwidth remains constant at high level even with decreasing divisor voltages can be realized (Fig. 5b).

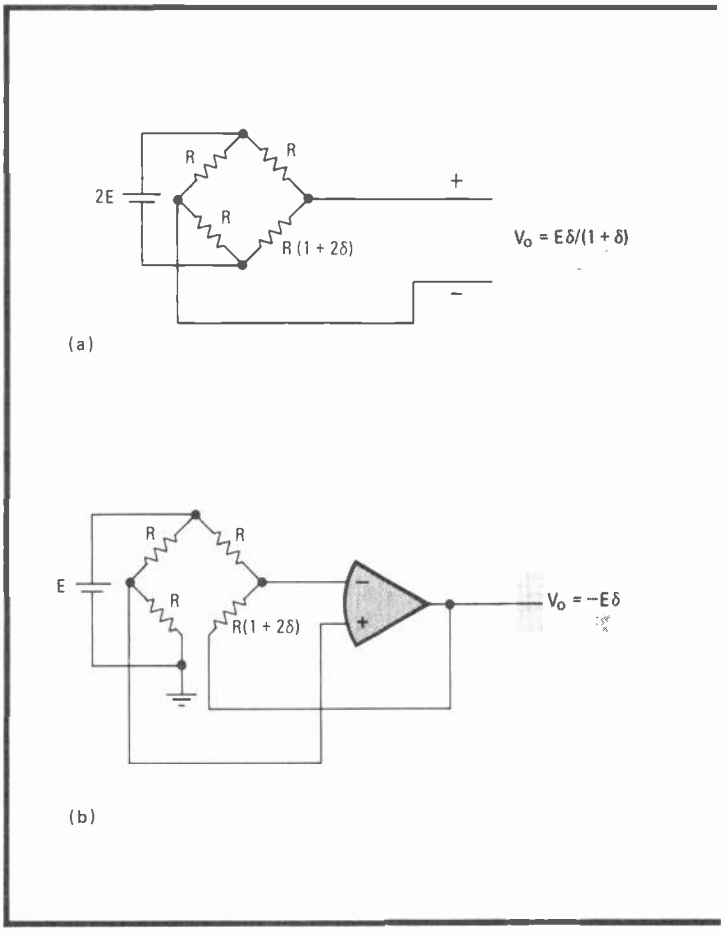
Notice that the current through the output stage (Q_3, Q_4, and A_4) is determined by the reference current, I, and remains constant. If I is set high, the divider's bandwidth will stay fairly flat from a 10-V divisor voltage down to 100 mV and then start to drop gradually, at a much slower rate than the circuit in Fig. 5a. Using 741-type op amps and setting I equal to 200 μA, typical component values are:

R_1 = 50 kilohms R_4 = 10 kΩ
R_2 = 10 kΩ R_5 = 100 kΩ
R_3 = 33 kΩ C = 33 picofarads

As mentioned before, the offset voltages and bias currents of the op amps should be nulled out for low-signal operations. Unfortunately, with a reference current in place of a reference voltage, this divider circuit cannot be readily used as a three-input multiplier-divider to perform $E_o = XY/Z$.



7. Another approach. The multifunction converter (here, the 4302) may also be used as a square-rooter. To implement the transfer function, $E_o = X(YZ)^m$, m can be set equal to ½ (a) or to 1 (b), with the other connections appropriately made.



8. Linearizing bridges. The Wheatstone bridge has a nonlinear output dependent on the input variable (a). It may be linearized by using an op amp in a feedback loop (b), a multiplier–inverted divider (c), or an MID with an instrumentation amplifier (d).

One application of a precision divider is computing the square root of an input signal, often required in process-control systems. If the divisor's input is connected to its output terminal, the divider's transfer function, that is, $E_o = 10N/D$, becomes:

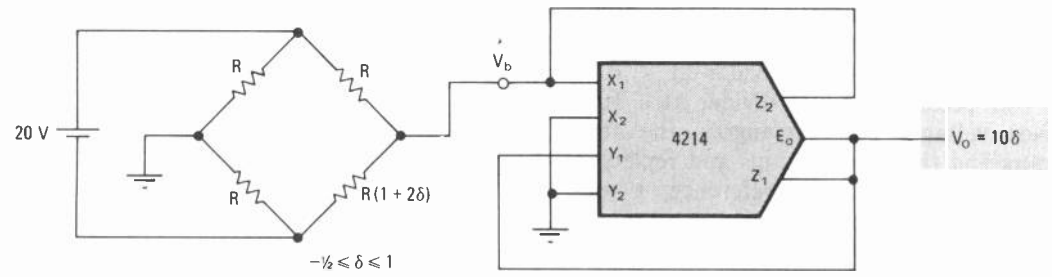
$$E_o = 10(N/E_o) = (10N)^{1/2}$$

The output is now proportional to the square root of the input, N.

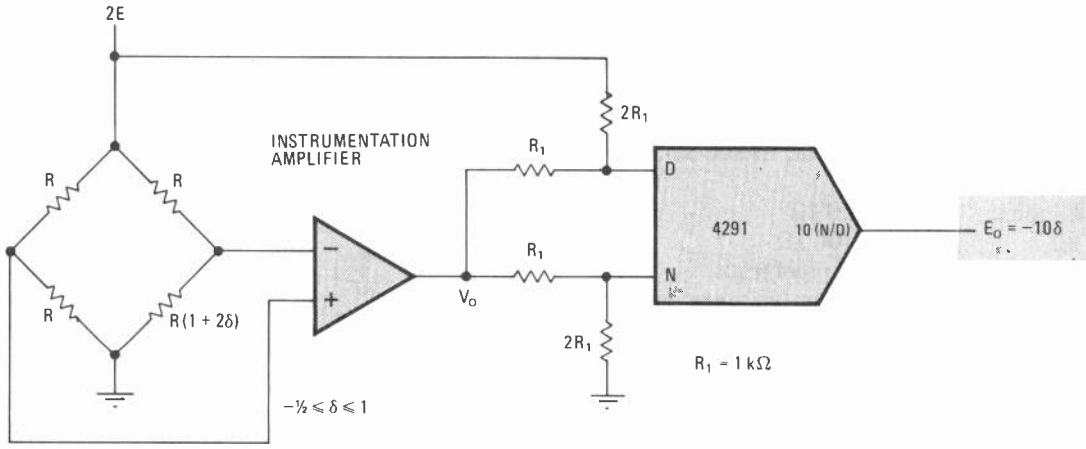
Square-rooters

Square-rooters employing a multiplier–inverted divider and a log-antilog divider are shown in Fig. 6a and 6b, respectively. Since E_o is always unipolar, adding a diode at the output of the divider will help prevent the square-rooter from saturating to the opposite supply voltage, which is occasionally caused by power-supply transients. In Fig. 6b, a 1-megohm output load may be necessary to turn on the diode, because the input impedances of the divider are so high (about 10 MΩ) that, without the load, practically no current will flow through the diode.

The square-rooter's accuracy is strictly dependent upon the accuracy of the divider employed. With a multiplier–inverted divider, the accuracy is poor at low input voltages. The error-versus-signal voltage can be estimated from:



(c)



(d)

$$E_o = (10E_{in} + 10\epsilon_m)^{1/2}$$

where E_o and E_{in} are the square-rooter's output and input voltages, respectively, and ϵ_m is the multiplier error specified by the manufacturer. For example, for a 0.5% multiplier, ϵ_m = 50 mV maximum, and therefore the square-rooter's error would be 25 mV maximum at E_{in} = 10 V, but would be 109 mV maximum at E_{in} = 500 mV.

Figure 6c compares the typical error curves of square-rooters built with a multiplier–inverted divider and those made with a log-antilog divider. Typical errors would normally be much lower than in the graph. As can be seen, if small-signal accuracy is critical, a precision divider like the log-antilog type should be used.

With an external voltage reference, a multifunction converter may also be used to build a square-rooter. There are two ways to implement this function. The straightforward method is to set m = ½ with two matched resistors and connect X and Z to a 10-V reference (Fig. 7a). Then the output voltage becomes:

$$E_o = 10(Y/10)^{1/2} = (10Y)^{1/2}$$

Alternatively, m can be set to 1 as in Fig. 7b and the X input connected to a +10-V reference. By shorting Z to the output, E_o, the transfer function becomes:

$$E_o = 10(Y/E_o) = (10Y)^{1/2}$$

The accuracy of this square-rooter is about equal to that of a log-antilog divider.

The familiar Wheatstone bridge is widely used in measuring the resistance of sensors like strain gauges, pressure transducers, thermistors, and servo motors. Unfortunately, the output of the bridge is a nonlinear function of the input variable, the change in the resistance being measured. As illustrated in Fig. 8a, the output voltage, V_o, is related to the input variable, δ, by:

$$V_o = E\delta/(1 + \delta)$$

where 2E is the bridge supply voltage.

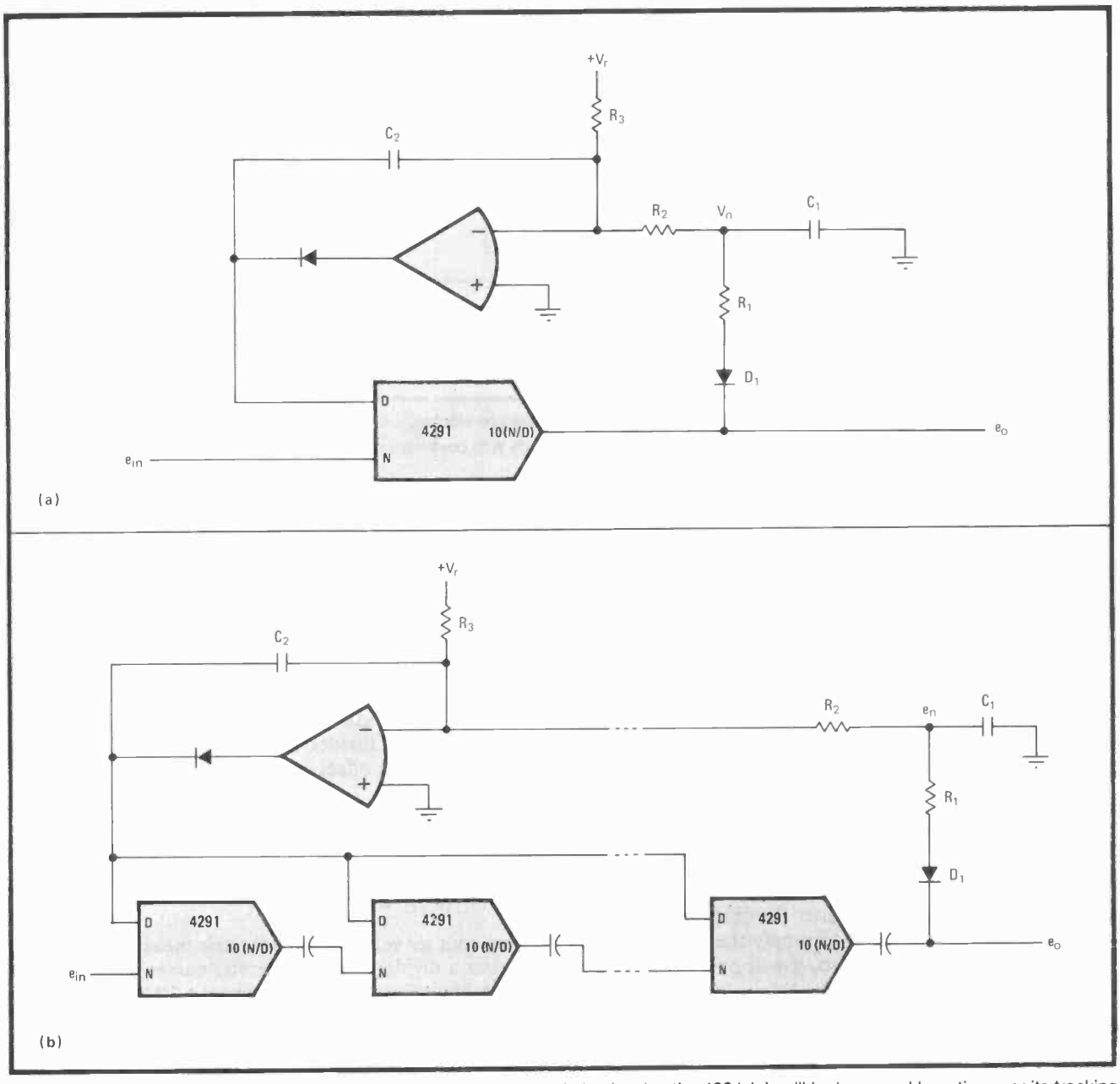
Linearizing the bridge

Because direct measurement and manipulation of nonlinear data is often undesirable, a circuit is needed to first linearize the bridge function. The simplest method of linearization uses an op amp. Connecting the variable-resistance arm in the feedback loop (Fig. 8b) causes the output of the op amp, V_o, to vary linearly with the variable, δ. Thus, $V_o = -E\delta$. However, some inexpensive bridges are packaged in four-terminal boxes and therefore will not work with this method, which requires five terminals.

A low-cost multiplier–inverted divider with differential Z inputs can, however, implement the inverse of the bridge function and linearize it. In Fig. 8c, the output voltage of the bridge, V_b, is given by:

$$V_b = 10\delta/(1 + \delta)$$

and the multiplier–inverted divider provides the transfer function, $V_o = 10V_b/(10 - V_b)$. The series connection of these two nonlinear circuits results in a linear function,



9. Controlling gain. The bandwidth of a 40-dB automatic-gain-control circuit using the 4291 (a), will be increased by n times, or its tracking range by n times, by cascading n dividers in the feedback loop shown in (b). The 400-kHz bandwidth, however, cannot be exceeded.

that is, $V_o = 10\delta$.

If the bridge supply voltage is single-ended, rather than floating as in Fig. 8c, an instrumentation amplifier is needed to convert the two output terminals of the bridge to a single output. The amplifier can be used effectively to compensate for bridge voltage variations. By inverting the signal such that $V_o = -E\,\delta/(1+\delta)$ and using four resistors to sum the bridge voltage with, and divide it by, V_o (Fig. 8d), the divider's denominator and numerator voltage become:

$$D = \frac{2R_{iD}}{3R_{iD}+2R_i}(E+V_o)$$

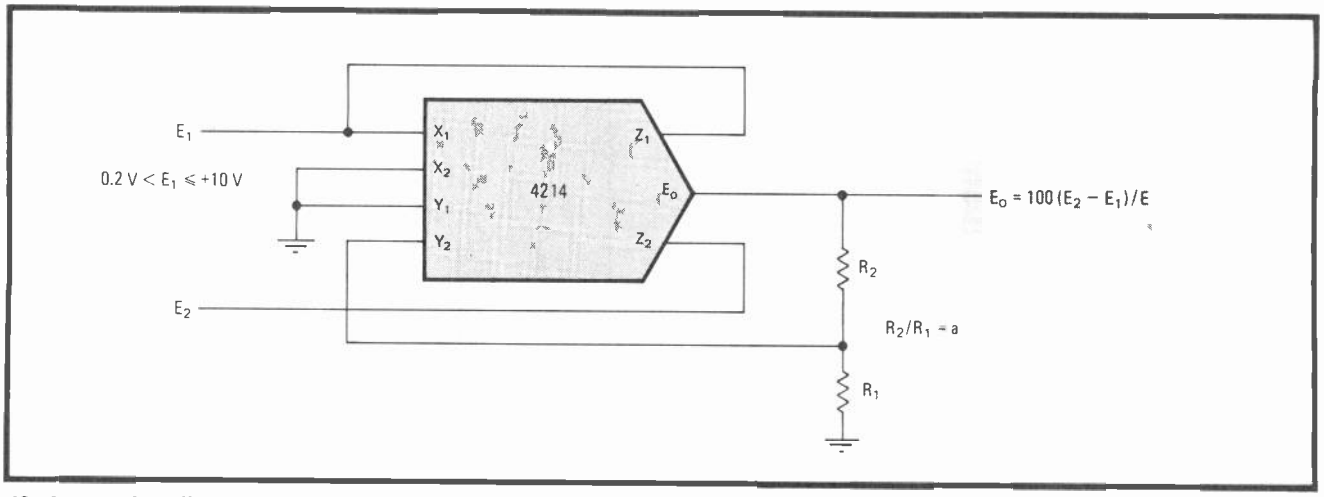
$$N = \frac{2R_{iN}}{3R_{iN}+2R_i}V_o$$

respectively, where R_{iD} is the input impedance of the divider's denominator input and R_{iN} is that of the numerator input.

The cleverness of this circuit becomes clear when D and N are substituted into the divider's simple transfer function, $E_o = 10N/D$. The bridge voltage, 2E, and the input impedance, R_i ($= R_{iN} = R_{iD}$), cancel out, resulting in $E_o = -10\delta$. Therefore, the output is independent of the bridge supply voltage. When R_1 is much smaller than R_i, the circuit is insensitive to the value of R_i.

Controlling the gain automatically

To compensate for amplitude fluctuations of any given signal, nothing less than a well-designed automatic-gain-control circuit will do. A good AGC circuit is one that can keep the output constant over a wide dynamic range of



10. A natural application. Direct readouts in percentage of such parameters as efficiency, distortion, gain/loss, and error are easily obtained by connecting a 4214 in a configuration that provides an output of 1 V = 1% with deviations measured up to ± 10%.

input signal levels (tracking range). Analog dividers are excellent candidates for such appplications.

The tracking range of an AGC is directly related to the denominator's operating range of the divider employed. For example, if a divider has a divisor operating range from 10 V down to 100 mV, the AGC circuit associated with it will track ac signals over a 40-decibel range.

Figure 9a shows an AGC circuit using a two-quadrant log-antilog divider. The divider serves as a voltage-controlled amplifier whose output increases with a decrease in divisor voltage. Diode D_1 rectifies the output voltage, e_o. Low-pass filter R_1–C_1 produces a negative voltage, V_n, proportional to the negative peak of e_o. The integrator, comparing V_n with a positive reference voltage, V_r, determines the divisor voltage of the divider.

Automatic gain control is achieved thus: as the input signal, e_{in}, increases, e_o tends to increase, pushing V_n further negative. This increases the integrator's output voltage, which is connected to supply the divisor's input. As the divisor voltage goes up, it will pull e_o back down until it reaches an equilibrium.

Typical values for audio applications are:

$R_1 = R_2/10 = R_3/10 = 1\ k\Omega$

$C_1 = 10C_2 = 10\ \mu F$

$V_r = 0.3$ V

These values will provide a 2-V peak-to-peak output amplitude, which can be reset by adjusting either R_3 or V_r. For subaudio frequencies, an increase in the values of both C_1 and C_2 is necessary.

The upper frequency limit is determined by the bandwidth of the divider, and the bandwidth of most dividers decreases with decreases in divisor voltage. This means that the bandwidth of the AGC will decrease with input signal voltages.

As an example, with a divider's 3-dB bandwidth specified for 400 kHz at a 10-V divisor voltage, the bandwidth will be, as a rule of thumb, 40 kHz at a 1-V divisor voltage and 4 kHz at a 100-mV divisor voltage. With these specifications, a 40-dB AGC circuit will operate over a 40-dB signal range only up to 4 kHz and over a 20-dB range up to 40 kHz. Although it can function up to 400 kHz, the circuit will have no practical tracking range at those frequencies.

The bandwidth of the AGC circuit can be expanded by cascading two or more dividers in the feedback loop (Fig. 9b). For the 40-dB example, each of the dividers operates actually over 40/n dB, where n is the number of dividers cascaded. The bandwidth of the AGC circuit will thus be increased by n times, but will, of course, never exceed the divider's maximum bandwidth of 40 kHz. The cascading technique will also increase the tracking range of the AGC circuit by n times; that is, two 40-dB dividers will yield an 80-dB AGC circuit. Ac coupling at the output of each divider is recommended to eliminate unwanted divider offset voltages.

Taking ratios

For ratiometric applications, a divider naturally comes to mind. Percentage measurement:

$$E_o = 100(E_2 - E_1)/E_1$$

is just another version of ratiometric measurement, but it requires a divider with differential numerator inputs and adjustable gain (from the nominal 10 to 100). With low-cost IC dividers, it is practical to provide direct readout in percentages of such parameters as efficiency, distortion, gain/loss, error, and so on.

Figure 10 shows a percentage measurement circuit employing a differential multiplier–inverted divider. The circuit, which provides 1 V = 1%, is capable of measuring ± 10% deviations. Wider deviations can be measured by decreasing the ratio of R_2/R_1, and narrower variations by increasing the ratio. If the dynamic range of E_1 is too wide for a multiplier–inverted divider to handle, a log-antilog divider may be employed, but an extra operational amplifier will be needed to take the difference $E_2 - E_1$.

The percentage circuit can also be used to sort components by first converting the component's parameter into a voltage and comparing it with a reference. A comparator at the output of the percentage circuit may then be set to separate units beyond a specified limit. □

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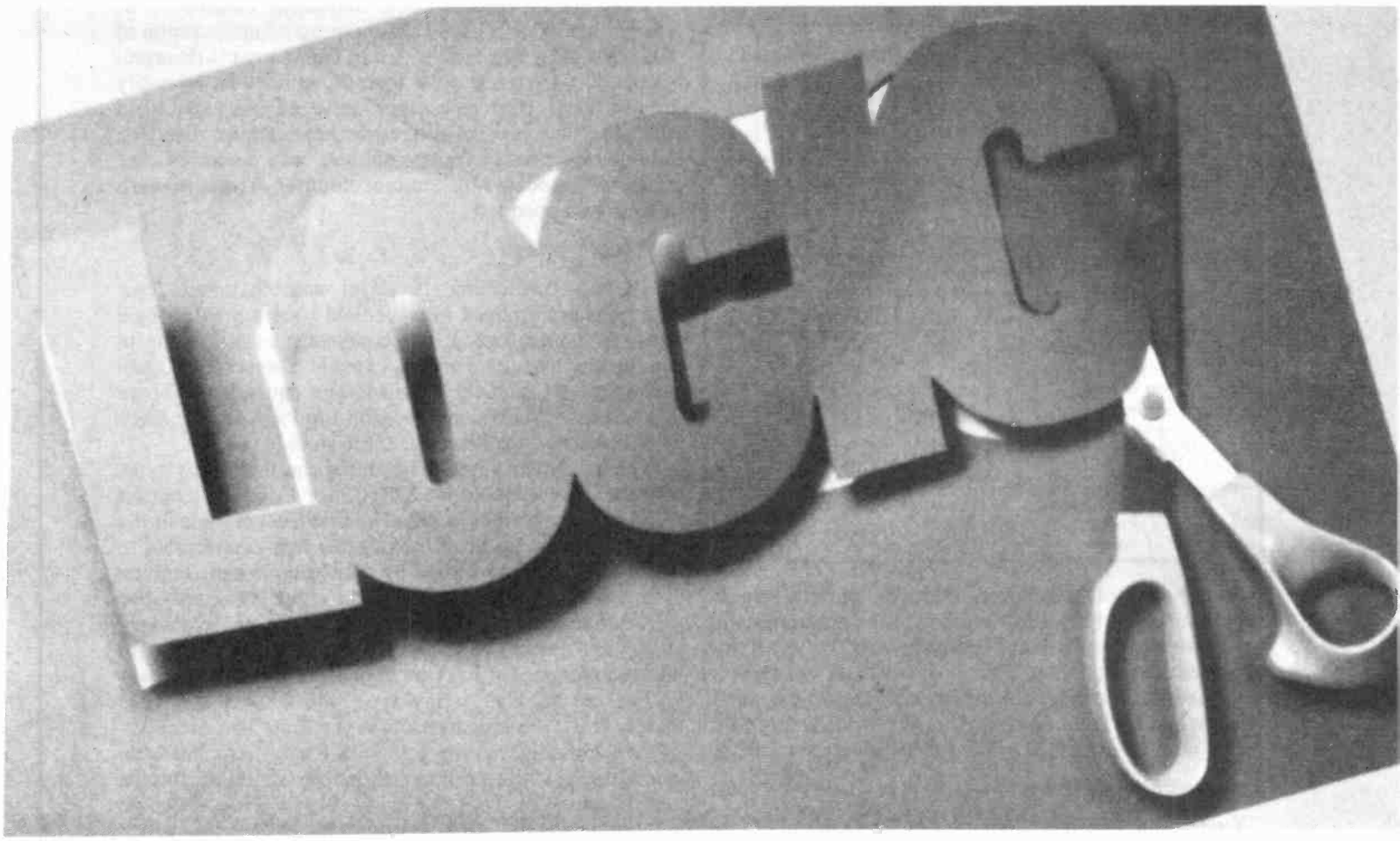
2. J. G. Graeme, "Designing with Operation Amplifiers: Applications Alternatives," McGraw-Hill, New York, 1977.



Field-programmable arrays: powerful alternatives to random logic

Bridging design gap, TTL-compatible logic family is described in Part 1 of a two-part article

by Napoleone Cavlan and Stephen J. Durham, *Signetics Corp., Sunnyvale, Calif.*

☐ With the steady growth of integrated circuit technologies, hardly a day goes by without the news that yet another chip has made scores of discrete TTL packages obsolete. Yet, though large-scale integration is packing entire system architectures onto a few chips, it is still impossible to complete a design without some discrete logic to hold the framework together.

The increase of LSI has thus created the need for efficient ways to bridge the gaps between large functional islands. Because of complexity, performance, or uniqueness, these bridges have evolved into nontrivial random-logic configurations that still rely on clusters of small- and medium-scale integrated circuits, whose fixed functions never quite fit the problem. Now Signetics Corp. has attempted to meet the need with a field-programmable logic family.

The family spans three ranges of complexity: at the low end are the field-programmable gate arrays (FPGAs); covering the middle range are the more complex logic arrays (FPLAs); and finally there are the logic sequencers (FPLSs). These last, most complex elements have built-in registers and enable the designer to proceed from state diagram directly to hardware. The family, summed up in the table on p. 110, is compatible with TTL and operates from a +5-volt supply.

The devices provide a powerful and compact alternative to random logic, replacing discrete gates, wires, and connectors, with significant savings in board space,

FIELD-PROGRAMMABLE LOGIC FAMILY

Device	Organization	Device	Inputs	Outputs[1]	Chip enable ($\overline{CE}$)	I_{CC} (max)	Delay (max)	Availability	Package[2]
FPGA	• AND/NAND	82S102 82S103	16	9 OC 9 TS	yes	170 mA	35 ns	now	N
FPLA	• AND-OR/NOR	82S100 82S101		8 TS 8 OC	yes		50 ns	now	N, F
FPLA	• AND-OR • Self-enable output	82S106 82S107		8 OC 8 TS	no		70 ns	4Q79	N
FPLS	• AND-OR • Complement array • 6-bit state register • 8-bit output register	82S104 82S105		8 OC 8 TS	yes[3]		90 ns	4Q79	N, F

[1] OC = open collector TS = three-state
[2] N = plastic F = Cerdip
[3] $\overline{CE}$ input may be optionally programmed as preset.

power, and cost. Moreover, since all devices can be programmed and modified in the field (as programmable read-only memories can) using readily available programming equipment, the logic can be changed to meet new customer requirements or specifications, or to recover quickly from design errors—after delivery to the field—without expensive printed-circuit-board retooling.

Programming options

Depending on their complexity, members of the programmable logic family have internal AND gates, OR gates, S-R flip-flops, true or complement buffers, and exclusive-OR (EXOR) gates. Those elements can be combined to perform single-level, double-level, and sequential logic functions—all by blowing fuse links.

There are other fuse options in output structures for the entire logic family, too, since either active-high or active-low functions can be generated without additional hardware or signal delay. Finally, the family is well suited to bus-organized environments such as microprocessor systems, since all its members offer, in addition to open-collector outputs, three-state outputs whose signals are in the high-impedance state until activated by a chip-enable input.

All the logic elements perform standard logic functions that can be represented by augmenting conventional logic symbols with a few new definitions so that they can represent multiple-input gates (see "How the FPLF defines logic," p. 65).

The gate arrays

The simplest member in the family is the field-programmable gate array, which performs single-level logic functions. The equivalent logic diagram for the FPGA is shown in Fig. 1. The two gate arrays currently available are open-collector (82S102) and three-state output (82S103) versions of the same array, which comprise nine NAND gates fuse-selectively connected to 16 common inputs by true/complement buffers.

Fuses in the FPGAs allow individual outputs to be complemented to AND, so that by proper manipulation of the input polarities, and by using De Morgan's theorem, AND, OR, NAND, and NOR logic functions can be easily implemented. The parts thus serve as universal logic elements that can be tailored to applications requiring random logic, as in fault monitors, code detectors, and address decoders for microcomputer systems with memory-mapped I/O.

The logic arrays

Devices performing two-level combinational logic functions are grouped into the field-programmable logic array (FPLA) category. These elements are a step up in complexity from gate arrays, capable of generating AND-OR, AND-NOR, and their De Morgan equivalents. There are at present two array types in the FPLA family, each with either open-collector or three-state outputs.

The equivalent logic diagram of the first array type, the open-collector output 82S101 (or three-state output 82S100), is shown in Fig. 2. The first level of logic in the device is made up of 48 AND gates fuse-connectable to any of 16 common inputs by true/complement buffers. The second logic level consists of eight OR gates—one per device output—each capable of being selectively coupled to any of the 48 gates. Finally, fusing options are included for generating true or complementary outputs.

The second logic array type, the 82S106/107, has nearly the same organization as the first. The exception is that an additional OR gate with fixed inputs has been added to generate an internal enable command for the output structure. That self-enable is generated whenever any of the AND gates become logically true, which occurs when the external input code matches the internal AND-gate program. In the absence of such a match, all device outputs are unconditionally disabled. The self-enable signal is available externally—the chip-enable input ($\overline{CE}$) pin on the 82S100/101 becomes an open-collector output called $\overline{FLAG}$. Because of this feature, the 82S106/107 can be viewed as a content-addressable programmable read-only memory, ideally suited to modifying data in large ROMs, as will be shown in the second part of this article.

Shared gates

Both array types benefit from the second level of logic. The advantage here is that the AND gates can be shared—OR gates can couple with up to 48 AND gates. Also, a key advantage of this arrangement over single-level logic is that it allows editing—disconnecting invalid AND terms from the OR array and replacing them with spare AND gates (Fig. 3).

Open-collector versions of both gate-array and logic-array devices can form wired-AND outputs in order to expand the number of AND gates available on a single chip. This solves the problem that is posed by applications exceeding the resources of a single device. The only restriction is that the expanded outputs have to be programmed to be active-low.

By far the most powerful members of the family are the field-programmable logic sequencers (FPLS), which add on-chip registers to arrays of AND and OR gates. The

How the FPLF defines logic

For the most part, schematic representation of logic in the field-programmable logic family follows conventional notation—the devices include AND, OR, and exclusive-OR (EXOR) gates, as well as set-reset (S-R) flip-flops and true or complement buffers. To simplify the representation of fuse-link programmability, however, the FPLF schematics use a matrix arrangement with cross-point coupling to represent intact fuse links.

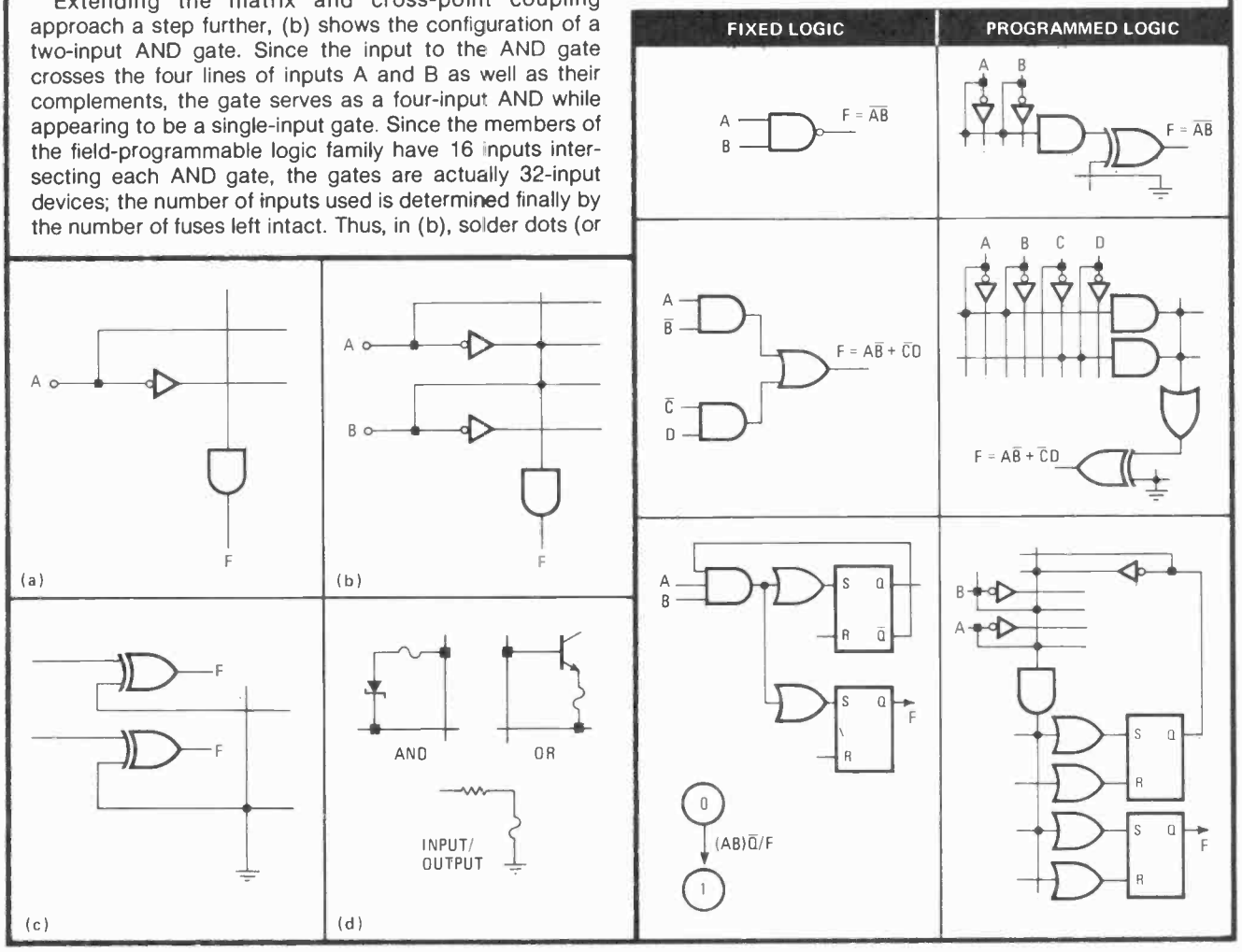
For example, (a) in the figure shows a typical input and AND gate of a gate array. The square "solder dot" represents a fixed internal connection. Both the line from input A and the line from the output of the inverter intersect the vertical input line of the AND gate; in actuality, fuse links make both connections. An intact fuse link is represented by a round solder dot. Blowing either of the fuse links will determine whether the input to the AND gate is A, or its complement, $\overline{A}$. (Leaving both fuses intact holds the output of the AND low, whereas blowing both fuses results in a "don't care" situation, an output that is independent of either input.)

Extending the matrix and cross-point coupling approach a step further, (b) shows the configuration of a two-input AND gate. Since the input to the AND gate crosses the four lines of inputs A and B as well as their complements, the gate serves as a four-input AND while appearing to be a single-input gate. Since the members of the field-programmable logic family have 16 inputs intersecting each AND gate, the gates are actually 32-input devices; the number of inputs used is determined finally by the number of fuses left intact. Thus, in (b), solder dots (or intact fuse links) create the logical equation $F = \overline{A}B$.

The exclusive-OR gates on all outputs of the logic-family devices allow programming for either active-high or active-low output signals. As shown in (c), a fuse link grounding one of the two inputs of an EXOR gate results in an active-high output; blowing the fuse results in an output that is active-low.

The details of the fusing mechanisms are shown in (d). AND gates have a fuse in series with a Schottky diode, while OR gate fusing uses an npn transistor. The fuses for the true/complement input buffers and active-high/active-low outputs are in series with resistors.

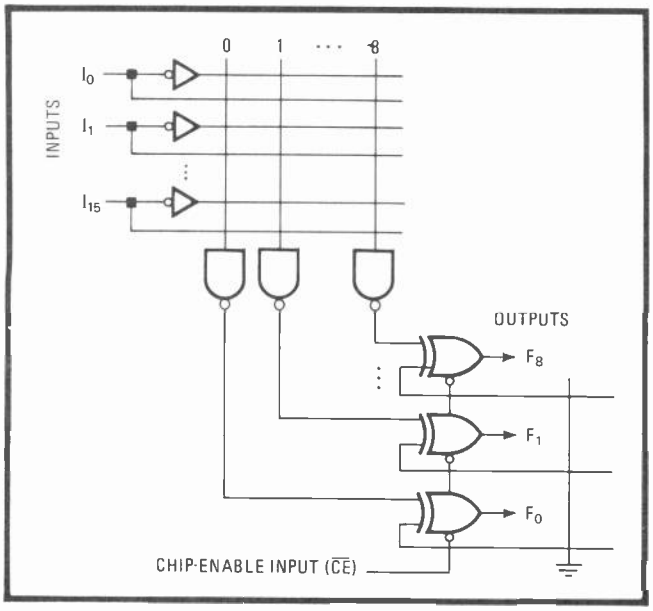
The analogy between fixed and programmed logic is best shown by the examples in the table. The first example is typical of the single-level logic to which the gate array is applicable. The two-level logic of the second example is satisfied by the logic arrays. Finally, the registered state machine that executes the state transition of the third example is a candidate for the field-programmable logic sequencers.



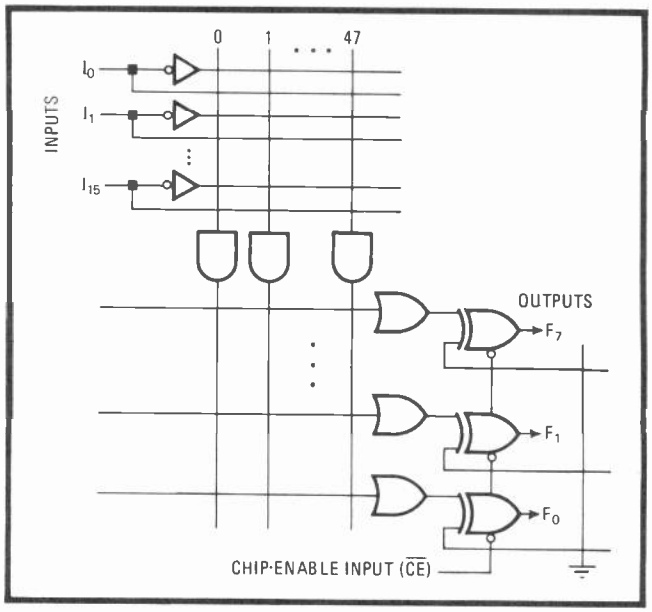
sequencers are actually self-contained state machines, since they can be programmed to perform any synchronously clocked logic sequence.

State machines, whose general structure is shown in Fig. 4a, usually take two forms: Moore machines, in which the output is a function of the present state only; and Mealy machines, whose output is a function of both the present state and the present input.

Figure 4b shows the basic architecture of the open-collector output 82S104 (or three-state output 82S105),



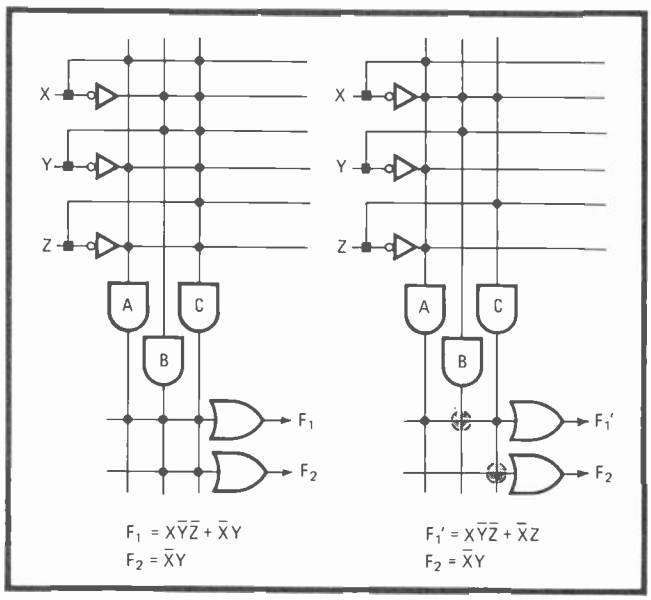
1. Gate array. The simplest device in Signetics' field-programmable logic is the gate array, capable of single-level logic. Any of 16 inputs can connect to nine NAND gates by true/complement buffers. Since outputs can be complemented to AND, manipulating De Morgan's theorem makes the device a universal logic element.



2. Double deep. The field-programmable logic array carries out two-level combinational logic. The 16 inputs couple to 48 AND gates, which in turn connect to any of nine OR gates. Either true or complement outputs are provided.

the first members of the FPLS family. With the FPLS, a user may program any logic sequence that can be expressed as a series of jumps between stable states triggered by a valid input condition I at clock time t. The number of states in the sequence depends on the length and complexity of the desired algorithm.

A typical state diagram is shown in Fig. 5. The state from which a jump originates is called the present state P, and that at which it terminates is the next state N. A jump always causes a change in state, but may or may not cause a change in the machine's output F.



3. Editing. The logic array's programmable OR gates allow sharing of AND gates, as with gate B at left. The OR array also allows easy editing of logic statements when design changes are made; note how spare gate C at right was used to modify output F_1 to F_1'.

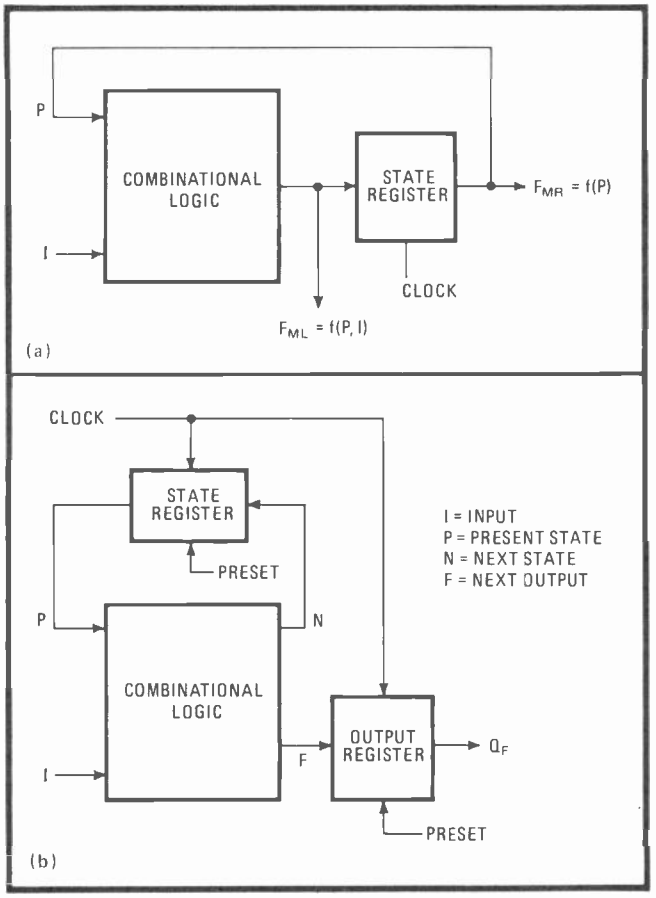
All states are arbitrarily assigned and stored in the state register, where the clock and next-state information from the combinational logic are the inputs. State jumps can occur only when transition terms are true. A transition term is, by definition, the logical AND function of the clock, present state, and valid inputs; hence, $T_n = t \cdot I \cdot P$. However, since the clock is actually applied to the state register, it may be removed from the equation. When T_n is true, a control signal is generated that, at clock time t, forces the contents of the state register from P to N and, if necessary, changes the contents of the output register.

FPLS organization

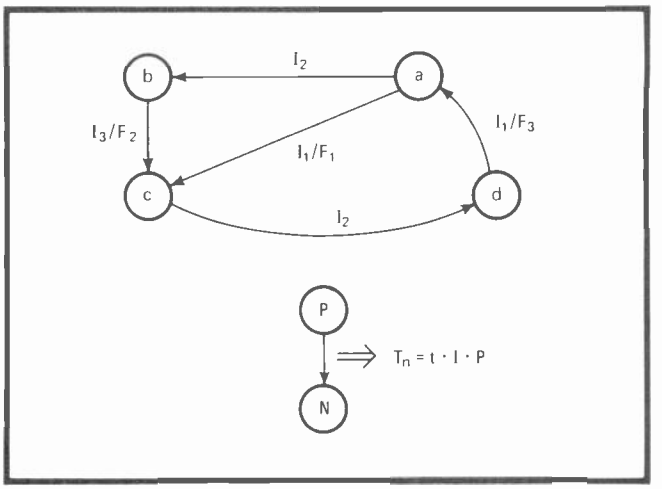
The architecture of the 82S104/105 is a natural extension of the static logic structure of the FPLA. It accepts 16 input variables and provides eight output functions. It has a 6-bit state register and an 8-bit output register; all the internal registers are automatically preset to logic 1 when power is applied. The FPLS provides for 48 transition terms, which can be selected to be either true or complementary.

A look at the equivalent logic diagram of the FPLS (Fig. 6) shows its extension of the static FPLA. The AND and OR gate arrays of the latter have been expanded to control the set and reset (S and R) inputs of six flip-flops (the state register) and to monitor the register's contents over an internal feedback path. Also, an independent 8-bit output register has been added to store output commands generated during state transitions and to hold the output constant during state sequences involving no output changes.

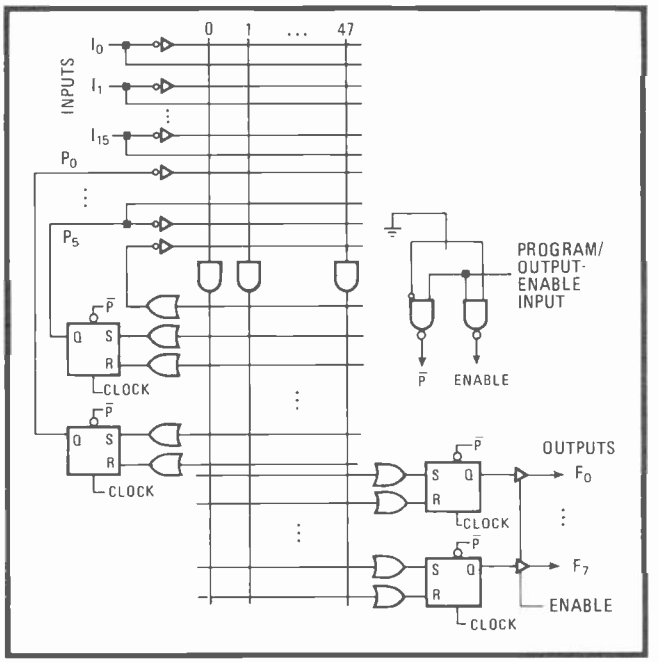
The AND array comprises 48 positive AND gates, each with 44 input connections from a set of true/complement buffers. The AND gates are used to form logic products of 16 external inputs (I_0 to I_{15}) with six present-state (P) inputs fed back from the state register. The gates are



4. State machine. A state machine (a) takes either a Mealy or Moore form. The architecture of the field-programmable logic sequencer (b) is that of a self-contained Mealy machine, where the output is a function of both the present state and the present input.



5. State diagram. Example of a state diagram (a) with four states—A, B, C, and D. $I_1 - I_3$ are jump conditions, which trigger output changes $F_1 - F_3$. A state change (b) gives rise to transition term T_n, which is logical AND of clock t, input I, and present state P.



6. Sequencer. The field-programmable logic sequencer has 16 outputs, 48 AND gates, and 28 OR gates, plus 14 flip-flops that serve as state and output registers. Either an asynchronous preset input or an output-enable input is available as a programming option.

therefore called transition terms because, like the transition terms in state diagrams, they issue next-state commands.

The OR array contains 28 positive OR gates, each with 48 input connections to all 48 AND gates. The outputs of the ORs drive the set and reset inputs of the 14 S-R flip-flops that are state and output registers.

The FPLS is made still more flexible by a complement array comprising a single 48-input OR gate that drives an inverter, which then feeds back into the AND array. The complement array forms a bridge between the AND and OR arrays for generating NAND functions of input-jump conditions; the user programs it in such a way as to suit each transition term.

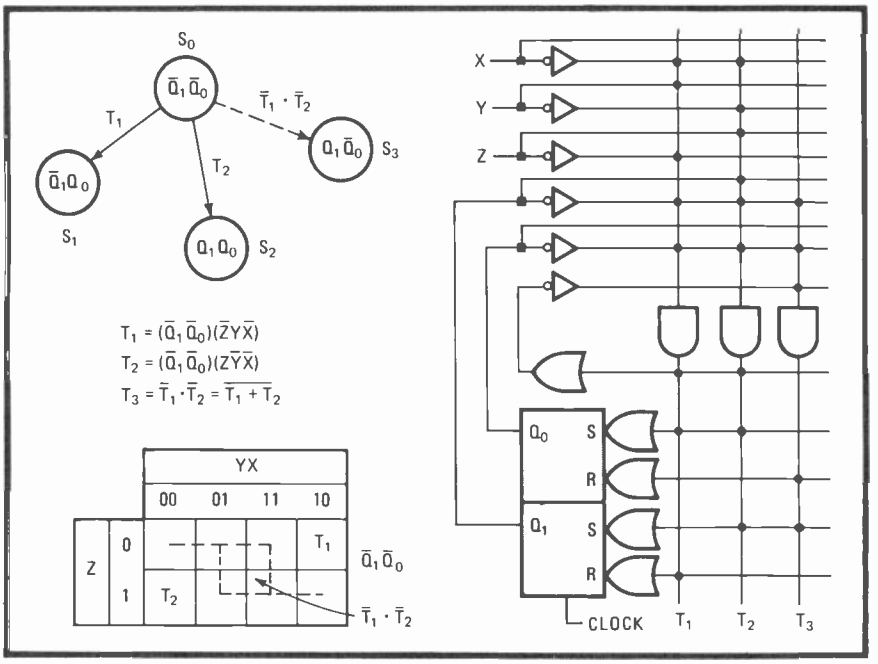
De Morgan's theorem

De Morgan's theorem to reduce logic terms can be easily implemented with the complementary array so that the most use is made of the AND gates. For example, if the transition term is $T = (Q)(\overline{X} + \overline{Y} + \overline{Z})$, where Q is the output of the state register and $\overline{X}$, $\overline{Y}$, and $\overline{Z}$ are inputs, three AND gates in the FPLS are required. However, De Morgan's theorem changes the transition term to $T = (Q)\,\overline{XYZ}$, which requires only two AND gates.

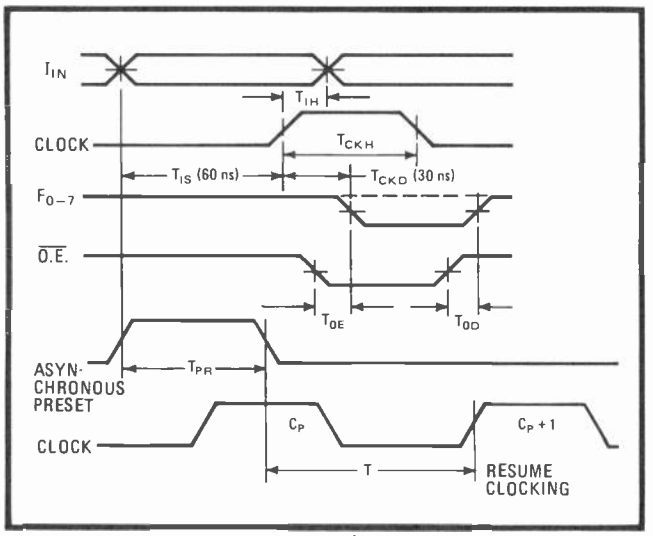
The complementary array is also an efficient means of aborting a clocked sequence in the absence of valid jump conditions. As Fig. 7 shows, considerable minimization of AND gates is possible when the detection of valid jumps involves many complements of jump functions, especially as the number of variables increases.

All clocked S-R flip-flops that make up the state and output registers offer the option of asynchronous presetting to all 1s. The 64-state total that can be represented by the state register is adequate in most cases to chart algorithms involving fewer than 48 nonredundant transitions. The register accepts next-state commands (N) from the OR array and supplies present-state information (P) to the AND array.

The output register is similar to the state register, except it has eight states for servicing eight output functions. It accepts the next-output commands F_0–F_7



7. Complementary. Use of AND gates in the FPLS is greatly reduced by the complement array, a single 48-input OR gate driving an inverter that feeds back into the AND array. In this example, the default jump from state S_0 to S_3 is reduced from three AND gates to a single gate T_3.



8. Timing. Minimum clock duration for the FPLS is 20 nanoseconds. Minimum width of preset input, which overrides clock, is 40 ns. Normal clocking resumes with the first full clock pulse following a negative clock transition after the trailing edge of the present signal.

from the OR array and then reflects its contents to the device outputs through the buffered Q outputs of each of the flip-flops. Also, as an added feature to enhance fault isolation, driving input I_0 to +10 volts will route the contents of the state register (P_0–P_5) directly to outputs F_0–F_5 without any alteration of the contents of the output register. However, the feature is not recommended for use in a normal mode of operation (as in a Moore machine). This is because it increases the device's maximum current by 5 to 10 milliamperes and thereby lowers the maximum ambient temperature rating of the package by approximately 5°C.

As a final programming option in the 82S104/105, a pin can function as either an active-high asynchronous preset (pr) or an active-low output enable ($\overline{OE}$). The output-enable function forces all outputs to logic 1 (or to high impedance in the 82S105) and is normally used when the device is sharing a bus. It does not inhibit clocking of the internal registers. The asynchronous preset option, on the other hand, is useful when the logic sequence requires an immediate state-independent return to initial conditions. The state register and output register can also be synchronously preset independently of one another by dedicating that function to one of the input variables in conjunction with a single transition term and a clock pulse.

Timing constraints

The maximum clock rate of the 82S104/105 can be inferred from its timing diagram (Fig. 8), which shows worst-case delays and setup requirements during a typical I/O cycle. Using stable external inputs as a reference, the device can be clocked after a minimum setup time of 60 nanoseconds. The next output (as well as the next internal state) will be valid 30 ns after the positive edge of the clock, giving a total I/O delay of 90 ns. Since both output enable and disable delays are also 30 ns, when the $\overline{OE}$ pin is used its signal's edge should occur prior to or coincidentally with the clock in order to avoid increasing I/O delays.

The asynchronous preset option includes a clock lockout feature that eliminates the potential hazard of spurious clocking. But, as the timing diagram shows, when using the lockout feature it is possible to miss one clock pulse, which may be prohibitive in some applications.

Field-programmable logic, Part 2

Sequencers and arrays transform truth tables into working systems

by Napoleone Cavlan and Stephen J. Durham
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☐ Because of its power and flexibility, the Signetics field-programmable logic family is ideal for replacing the discrete logic normally used to interface large-scale integrated devices, as shown in Part 1 [July 5, 1979, p. 109]. The examples of applications that follow show how to exploit its special features.

In designing with these gate and logic arrays and logic sequencers, the user need concern himself only with generating truth tables associated with the state diagrams or sets of Boolean logic equations that define his function. The one restriction is that he must use logic symbols corresponding to the status of fuse links.

As indicated in Fig. 1, an extra set of symbols is needed to describe all the states of FPLF gates corresponding to all combinations of blown and unblown fuse links. Once ordered into truth tables, the user-defined functions are then directly mapped onto standard program tables furnished with FPLF elements, whose fuses are then blown by a logic-type programmer. As the user gains experience, he can manipulate logic variables intuitively and can eventually implement algorithms directly on the program tables with only the device schematics for reference. (The formal step of deriving state diagrams and logic equations will not be considered here.)

Because of their simple and uncommitted structure, FPLF elements are suited to a wide variety of applications, several of them already well documented. The following examples illustrate the typical use of each logic element and match devices with applications.

Bus translator

Signetics' Instructor 50 microcomputer system is built around the 2650 microprocessor; but for compatibility with other systems and peripheral devices in the hobbyist market, it interfaces to the S100 bus, which is based mainly on 8080 microprocessor signals. Yet to carry out the seemingly unwieldy task of bus translation, only a single FPGA is needed. The gate array translates the logical combinations of timing, enable, and control signals supplied by the 2650 and its I/O hardware into control signals entirely compatible with the S100 bus definitions, as shown in Fig. 2.

The programmable feature of the FPGA is strategically invaluable in this case since the S100 bus is not yet totally standardized. The FPGA permits easy adaptation of the interface to changes in specifications, which are subject to arbitrary manipulation by manufacturers in the hobby arena.

Two-level logic

The logic arrays add a second level of combinational logic to the gate arrays, and thus another level of versatility. AND/OR combinations of the FPLAs are well suited to carrying out polynomial equations and the like, as shown in the next example.

In systems that transfer large blocks of data, a cyclic redundancy check (CRC) scheme can significantly improve data integrity. The technique appends a check word to a transmitted sequence of data, and the receiving end uses that word to check for errors. A cyclical division of the transmitted data by an industry-standard polynomial generates the CRC word; the remainder from the division forms the check word.

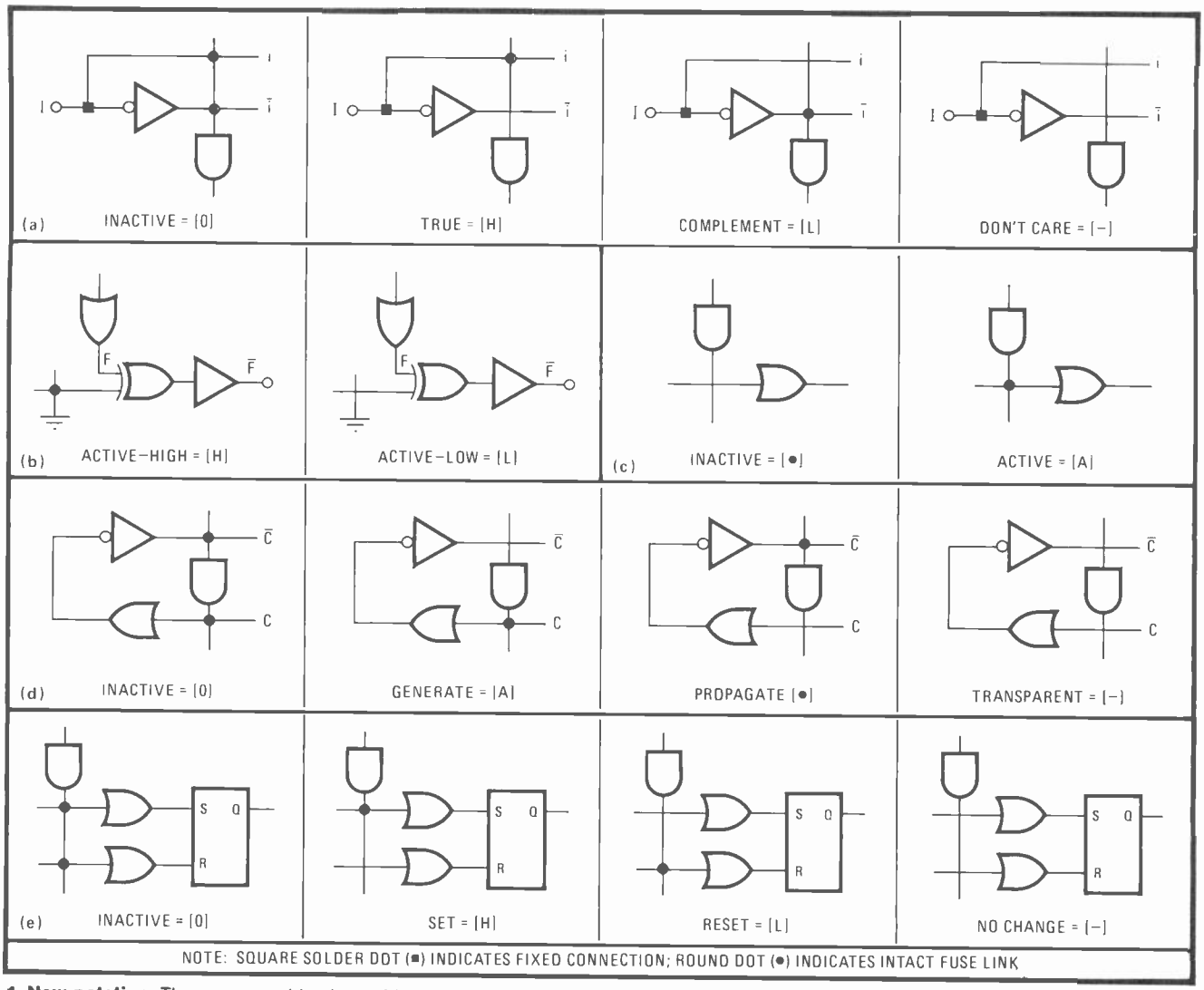
Polynomials lend themselves to serial manipulation, and serial CRC generation and checking are easy to implement. But in a multiple-line data system with parallel organization, a considerable amount of hardware may be needed for parallel-to-serial conversion. Moreover, the multiple-bit clocking for each word carries an inherent speed loss—a factor of 8 for a byte-oriented system. A parallel CRC generator-checker circuit is the answer, developed from the set of logic equations describing the function of the circuit in the form of a state machine.

The general design of the CRC circuit is shown in Fig. 3a, along with the logic equation set for the popular CRC polynomial $P(x) = x^{16}+x^{15}+x+1$. Figure 3b shows that the entire byte-wide parallel CRC generator-checker circuit can be implemented with only five chips: two 8-bit latches, two FPLAs, and an FPGA. The FPLAs contain the set of logic equations controlling the flip-flop inputs, which are expanded from EXOR form to sum-of-products form. In Fig. 3a, variables N_0–N_{15} represent the next CRC word after clocking, based on the current word B_0–B_{15} and the present input byte D_0–D_7.

CRC generation begins by driving the RESET line low to initialize the latches to zero. Pulsing the clock line then transfers the first byte of the data block in at D_0–D_7. Subsequent bytes are clocked in the same way. The cyclic nature of this design places no limit on the size of the data block that can be processed. During data transmission, the 16-bit CRC word is available at outputs B_0–B_{15} after the last data byte has been clocked in; it is appended as two check bytes to the data in the block.

Checking

The circuit is used in the check mode when receiving data containing CRC characters. The last 2 bytes in the data block received are CRC send characters. They too are clocked in and contribute to form a final receive pair of CRC characters, which, for error-free transmission, must both be zero. If an error has occurred, B_0–B_{15} will be nonzero. The FPGA will detect the nonzero condition and generate an error signal. This parallel CRC format can operate on data blocks at speeds in excess of 5.7



1. New notation. The many combinations of blown and unblown fuse links in the field-programmable logic family require new notation. The four possibilities for AND gates are shown in (a), while those for exclusive-OR outputs are in (b). The combinations for OR gates are in (c). The complement array in the logic sequencers is detailed in (d). Finally, OR gates controlling the flip-flops in sequencers are in (e).

megabytes per second.

An interesting use for the FPLA is in changing data at a few locations of a read-only memory (see "How to patch a read-only memory," p. 74).

The abilities of the field-programmable logic sequencer are well demonstrated by its use as a controller for a cartridge-tape transport. In this example, one chip replaces many—a distinct advantage if the controller is to be packed on a single-board microcomputer. Although the chip's function is complex, it can be programmed methodically and worked directly from a flow chart.

Controller routines

The controller executes fixed routines in response to status and input commands that may originate from an input/output bus or a monitoring station. Its outputs operate the velocity servo that drives the cartridge, form I/O status signals, and enable writing of data. The input and output signals of the one-chip controller are shown in detail in Fig. 4.

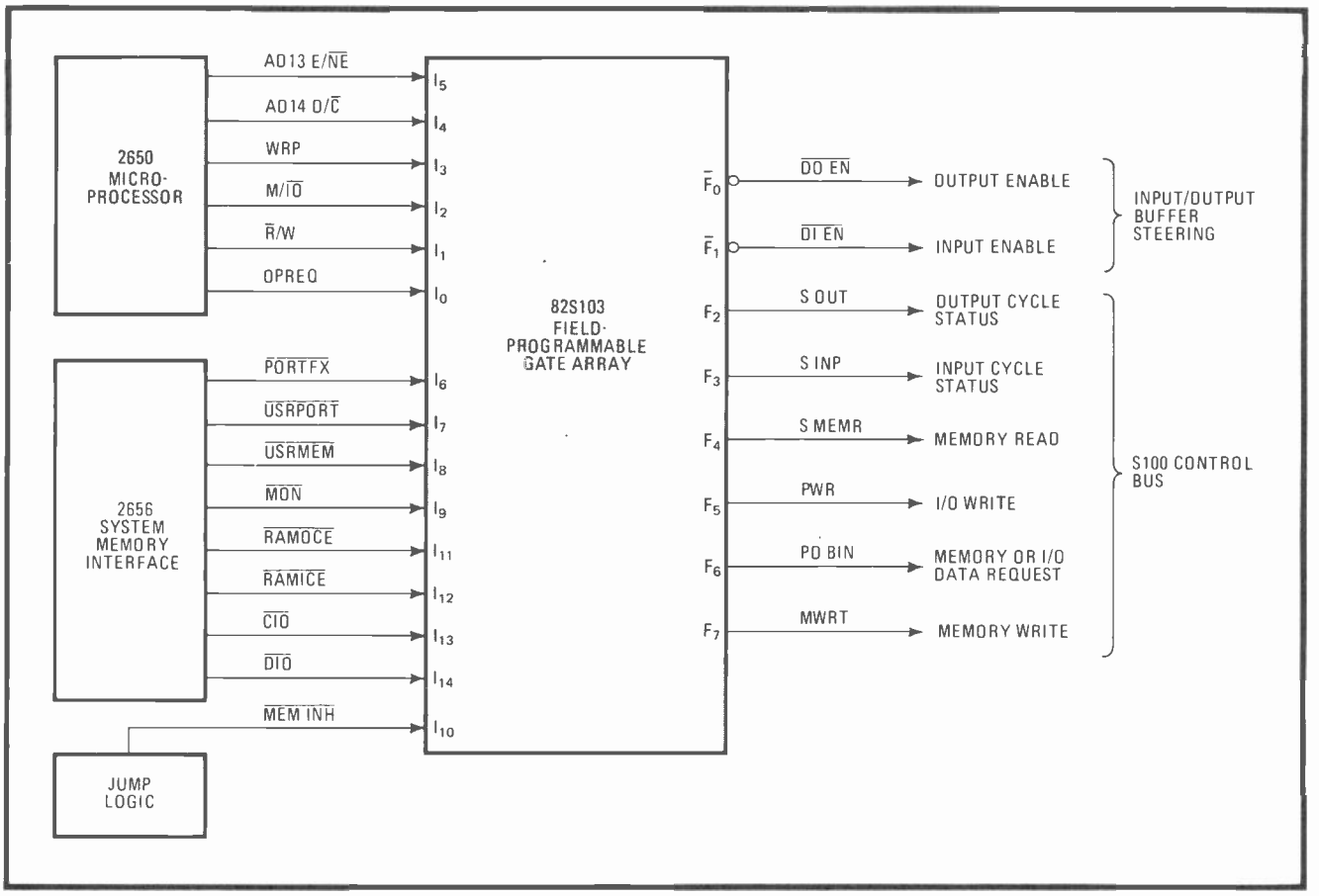
The controller carries out these eight routines:

- Move tape fast-forward.
- Move tape slow-forward.
- Move tape fast-reverse.
- Move tape slow-reverse.
- Bring tape to load point when cartridge is inserted.
- Rewind tape to load point.
- Rewind tape to beginning and eject cartridge in response to unload command.
- Rewind tape to beginning and eject cartridge in response to auto-unload true condition.

The routines could be represented concisely in a conventional Mealy state diagram, but that often obscures the actual machine function. Flow charts are more easily understood, where input variables, machine states, and output functions are given variable names. Such a chart is shown in Fig. 5.

Diagramming the flow

What would be transition terms in a Mealy state machine become true/false statements regarding the system inputs (taken one at a time) in the chart. The correlation is most obvious in the simple example in Fig. 6. The flow chart in (a) shows a conditional change from



2. Translator. Getting S100 bus signals, which are mostly 8080 microprocessor signals, out of a 2650 microprocessor calls for a field-programmable gate array. One 82S103 translates signals from the 2650 and its companion 2656 interfacing chip to the hobby bus.

state A to state B. The conditions in the flow chart's diamonds must be simultaneously satisfied for the state change to occur. The conditions take on variable names, and for this example, which arbitrarily assumes a 4-bit state register, three inputs, and two outputs, the corresponding state diagram is shown in Fig. 6b.

The transition from A to B denotes a jump from 10 (1010_2) to 13 (1101_2) and an output transition to 2 (10_2) at the next clock pulse if the combination $X_n = 4$ (100_2) is true. The transition is synthesized by forming a transition term $T = P_3\overline{P}_2P_1\overline{P}_0I_2\overline{I}_1\overline{I}_0$ and using term T at the next clock pulse to generate next-state and next-output commands for the state and output registers, respectively. For the state register, flip-flops N_0 and N_2 are set by connecting T to set lines S_0 and S_2, and flip-flop N_1 is reset by coupling T to the R_1 reset line. Similarly, for the output register bit F_0 is reset and bit F_1 is set by connecting T to corresponding flip-flop reset (R_0) and set (S_1) lines.

Controller conditions

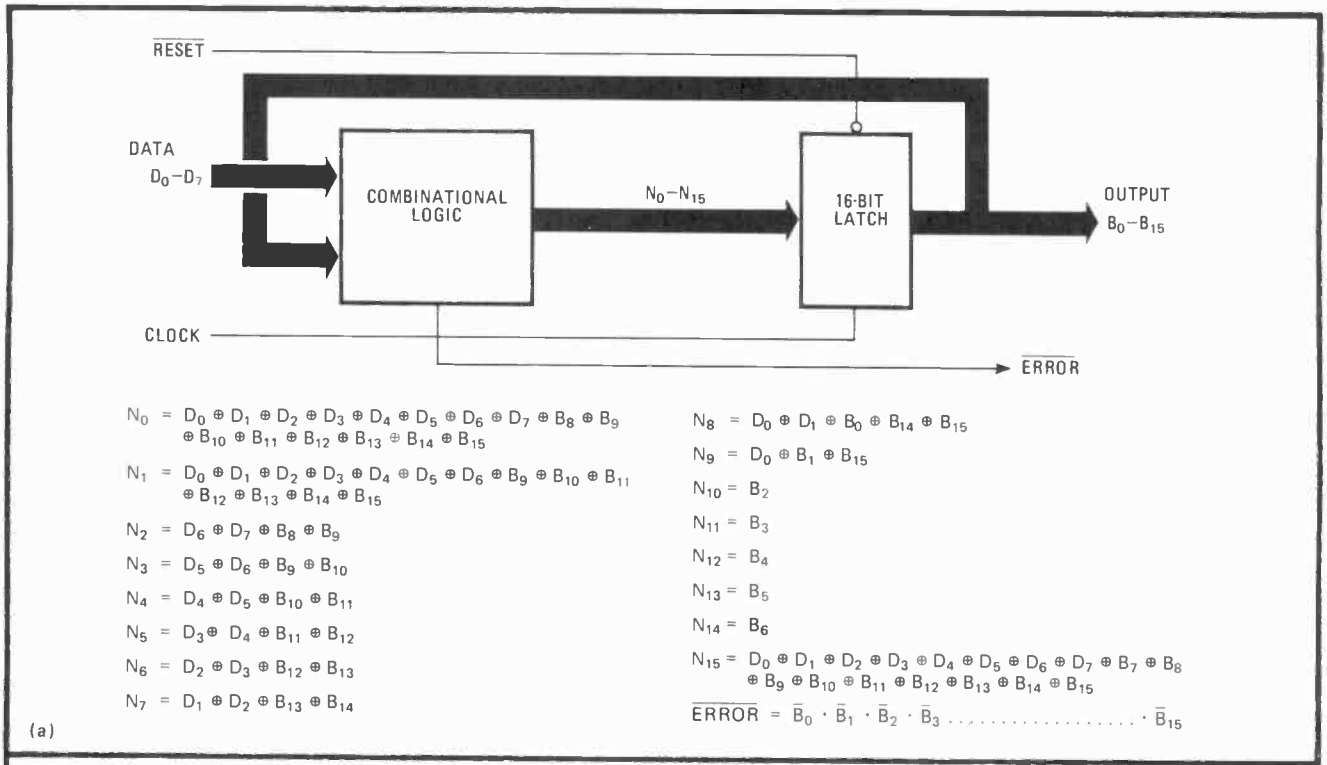
Referring again to the controller flow chart, it can be seen that whenever the tape-drive power is turned on, or when an interlock is opened, the transport must be stopped. That is achieved by an input signal to the controller called $\overline{\text{INTRDY}}$ that resets the state register with an unconditional jump to state 1 or STOP. When that occurs, all outputs on the FPLS chip become inactive, WRITE is inhibited, and speed and direction are arbitrarily set to SLOW and REVERSE. From the STOP state, operation into any mode ocurs by state and output jumps when all of the intervening conditions are simultaneously satisfied.

As an example, writing at normal speed will occur with a jump from state 1 to state 3, which requires that the following criteria be satisfied:

- The data cartridge is in place; therefore CIP is true.
- The drive has been addressed; SEL is true.
- The tape has been commanded to run; TR is true.
- The controller is not in state 6; state 6 is false.
- The tape should move slowly; therefore $\overline{\text{FAST}}$ is true (an active-low signal).
- The tape should move forward; $\overline{\text{FWD}}$ is true.

In tracing the jump between these states two things must be noted. First, the commands RWD, UNL, and TR are mutually exclusive, so that when either is true the others can be considered false or "don't care." Second, after TR = true, the condition (State = 6?) is inserted to indicate invalid jumps to states 2 and 3, which could originate from state 6 with an AUTO UNL false. Clearly, these should be avoided to inhibit honoring requests for read slow (or fast) forward while stopped at the end of the tape. So, the (State = 6?) condition is a reminder to avoid programming 6 → 2 and 6 → 3 state jumps in the FPLS. A similar argument holds for (State = 7?) and (State = 11?) conditions.

After data has been either written or read, the tape drive is commanded to stop by TR false, which causes a



$N_0 = D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus B_8 \oplus B_9 \oplus B_{10} \oplus B_{11} \oplus B_{12} \oplus B_{13} \oplus B_{14} \oplus B_{15}$

$N_1 = D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus B_9 \oplus B_{10} \oplus B_{11} \oplus B_{12} \oplus B_{13} \oplus B_{14} \oplus B_{15}$

$N_2 = D_6 \oplus D_7 \oplus B_8 \oplus B_9$

$N_3 = D_5 \oplus D_6 \oplus B_9 \oplus B_{10}$

$N_4 = D_4 \oplus D_5 \oplus B_{10} \oplus B_{11}$

$N_5 = D_3 \oplus D_4 \oplus B_{11} \oplus B_{12}$

$N_6 = D_2 \oplus D_3 \oplus B_{12} \oplus B_{13}$

$N_7 = D_1 \oplus D_2 \oplus B_{13} \oplus B_{14}$

$N_8 = D_0 \oplus D_1 \oplus B_0 \oplus B_{14} \oplus B_{15}$

$N_9 = D_0 \oplus B_1 \oplus B_{15}$

$N_{10} = B_2$

$N_{11} = B_3$

$N_{12} = B_4$

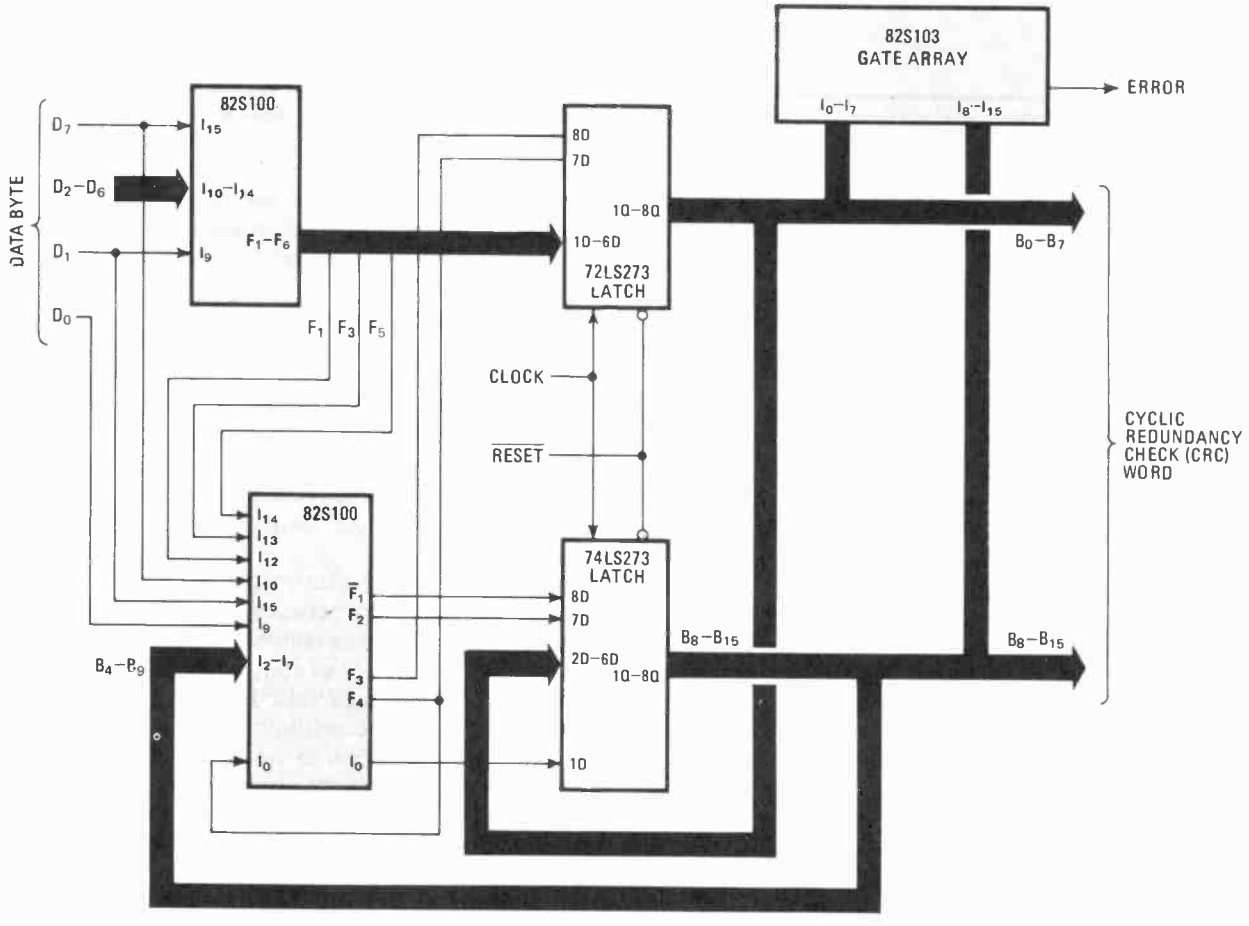
$N_{13} = B_5$

$N_{14} = B_6$

$N_{15} = D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus B_7 \oplus B_8 \oplus B_9 \oplus B_{10} \oplus B_{11} \oplus B_{12} \oplus B_{13} \oplus B_{14} \oplus B_{15}$

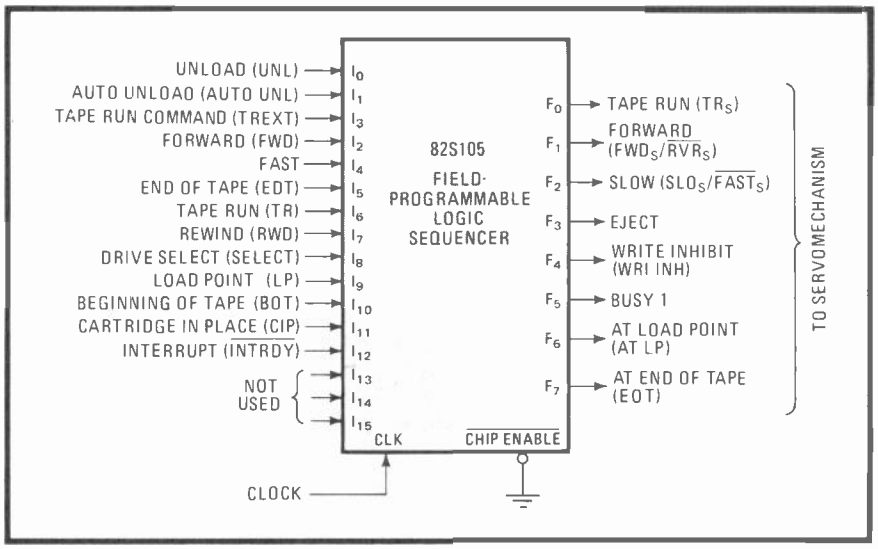
$\overline{ERROR} = \overline{B}_0 \cdot \overline{B}_1 \cdot \overline{B}_2 \cdot \overline{B}_3 \cdots \cdot \overline{B}_{15}$

(a)

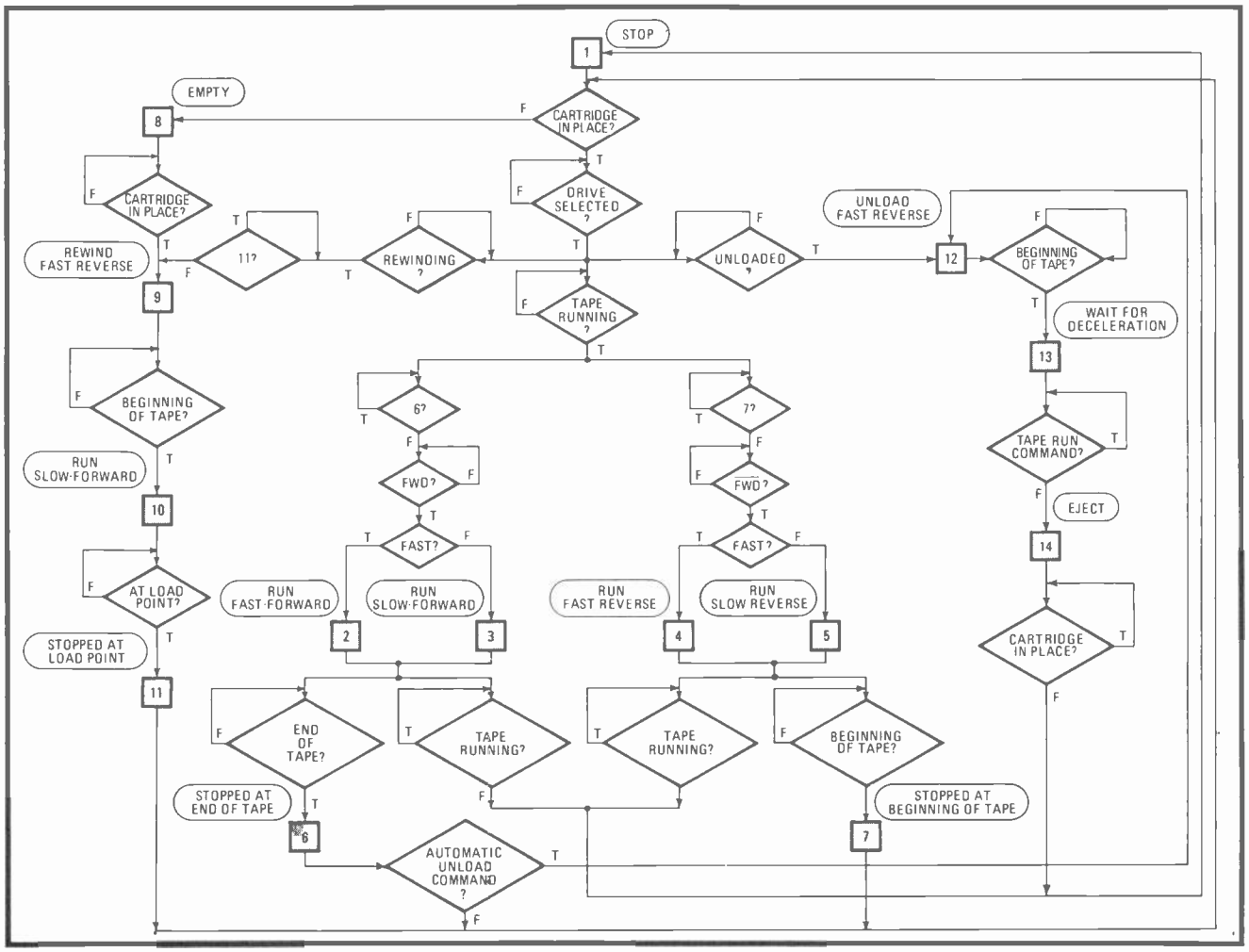


(b)

3. Error-free. The technique of using a cyclic redundancy check (CRC) word for error-free data transmission requires complex logic to generate the word (a). A pair of logic arrays, two latches, and a gate array (b) do the job, which usually requires a boardful of chips.



4. Tape controller. A field-programmable logic sequencer like this tape controller can perform extremely complex tasks. The 82S105 receives commands from an input/output bus or monitor, and provides all the necessary signals for driving the tape-transport servo-motor mechanism.



5. Goes with the flow. The first step in designing the controller is preparing a flow chart of the operation. The chart is much easier to understand than a state diagram or Mealy machine, yet provides all the information needed for programming the logic-sequencer chip.

jump from state 3 (RUN SLOW FORWARD) tc state 1. By similar arguments, the tape drive can be run either fast or slow in either forward or reverse directions by jumping to states 2, 4, and 5.

When the end of tape is reached (EOT true), the tape drive is stopped. That is implemented by jumps 2 →6 or 3 →6. Once in state 6, the tape drive can no longer move in the forward direction because of the State 6 false condition preceding states 2 and 3. If AUTO UNL is true, the drive will automatically rewind (state 12), wait for tape to decelerate (state 13), eject the tape cartridge (state 14) and stop. If AUTO UNL is false, the drive must

How to patch a read-only memory

It is a shame to throw away read-only memories. But often firmware-based systems must commit control programs to large mask-programmed ROMs, only to have a design revision requiring a new program—and a new ROM. If no pin-compatible, user-programmable ROM is available, the customer could end up waiting out the 5-to-10-week turnaround time for the new mask parts—and throwing away his inventory of old ROMs.

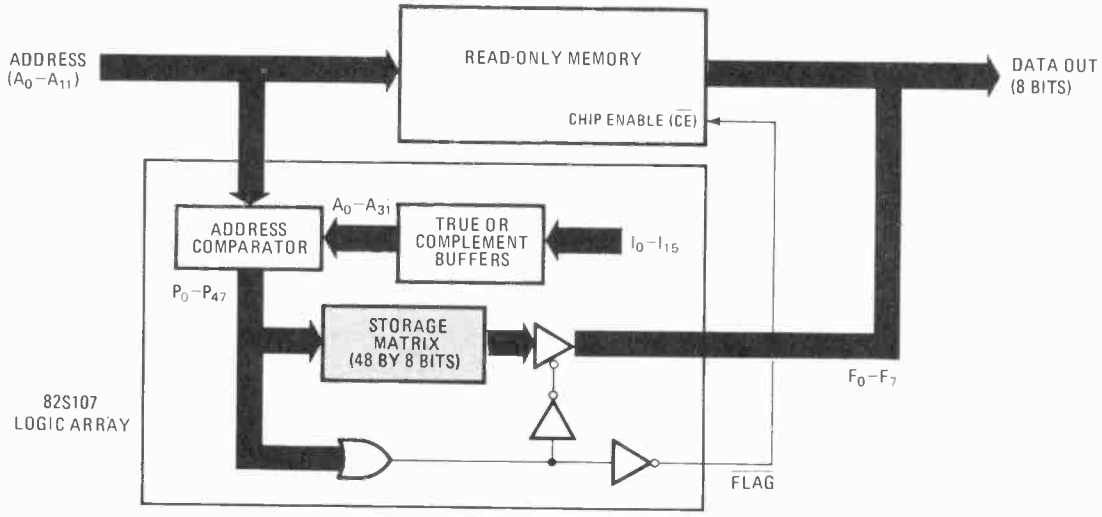
One way to save an obsolete ROM (or even PROMs—it hurts to throw them away, too) is by patching, which redirects certain addresses to an adjunct smaller memory. This can be done most efficiently with an 82S107 field-programmable logic array.

As a ROM patch (FPRP), the FPLA becomes a programmable, content-addressable PROM that continually monitors the address bus. As shown in the figure, when the FPRP encounters a match that signals a correction of data, its flag output ($\overline{FL}$) disables the ROM, and new data from the FPRP is put on the output bus. If, for example, address 750 were to be given new data A9, address 5FE were to be given 7F, and addresses 0A4–0A7 were all to be reassigned B4, the FPRP would be programmed as in the table. For a 12-bit address, only inputs I_0–I_{11} are used, and the remaining four, I_{12}–I_{15} then become "don't care." (Incidentally, inputs I_0 and I_1 in the second product term are also "don't care" because they define an address block of four locations.)

The address comparator can patch up to 48 non-overlapping addresses anywhere within a memory field of 64 kilobytes. Block addressing is possible, too, using the FPRP's true or complement input buffers. Moreover, the number of addresses can be expanded by hooking several devices in parallel and wire-ANDing their flag outputs.

Since the outputs of the ROM patch primarily define a byte of memory data rather than a set of logic functions, output polarity is not controlled. Also, to maintain compatibility with the gate array, the FPRP generates its self-enable signal with a fixed multiple-input OR gate; the only disadvantage of that method is addresses (AND terms), once programmed, may no longer be deleted.

The ROM patch affords a recovery strategy effective in several design situations, including modifications of dedicated application programs, operating systems, assemblers, and monitor routines. It also permits on-site optimization of system parameters, in accordance with, say, environmental variables, and allows custom function options and product-line diversification. The customer need only allot board space next to the mask ROM for an FPRP; no parts are actually used until program changes are required after the product is in the field.



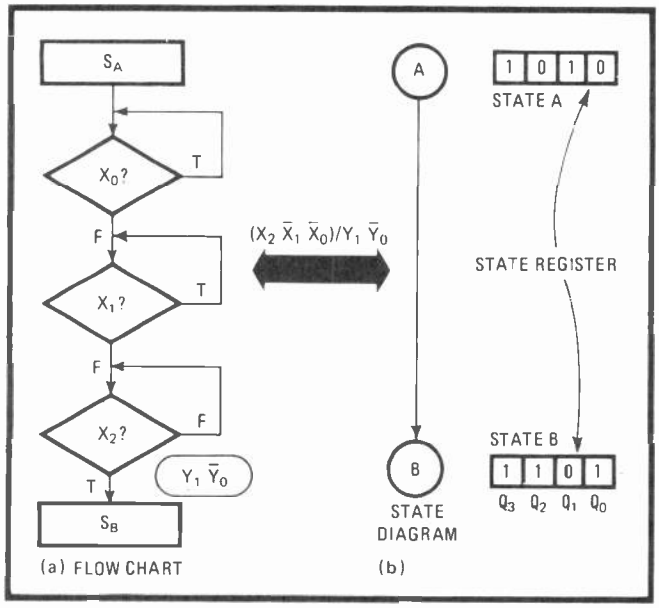
PROGRAM TABLE FOR ROM PATCH

Input address	Product term No.	Comparator input 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Active level H	H	H	H	H	H	H	H	Output data
																		Output function 7	6	5	4	3	2	1	0	
750	0	–	–	–	–	L	H	H	H	L	H	L	H	L	L	L	L	A	•	A	•	A	•	•	A	A9
5FE	1	–	–	–	–	L	H	L	H	H	H	H	H	H	H	H	L	•	A	A	A	A	A	A	A	7F
0A4–0A7	2	–	–	–	–	L	L	L	L	H	L	H	L	L	H	–	–	A	•	A	A	•	A	•	•	B4
		A_{11}															A_0	D_7							D_0	

wait for either a rewind command (RWD), an unload command (UNL), or reverse command (FWD).

If the tape is moved in the reverse direction until the beginning (BOT), the drive is stopped. This is implemented by a jump from states 4 or 5 to state 7. Once in state 7, the tape drive can no longer move in the reverse direction because of the state 7 false condition preceding states 4 and 5. The tape will remain stopped at the beginning until TWD, UNL, or FWD commands are given.

If no cartridge is in place (CIP false) when the tape drive is turned on, the controller will jump from state 1 to 8, and signal EMPTY. When a cartridge is installed,



6. Flow chart to state diagram. Simple transition from state A to state B is shown in flow chart (a). Three inputs (X_0,X_1,X_2) and two outputs (Y_0,Y_1) are assumed. The contents of a four-bit state register show the transition from state A (1010_2) to state B (1101_2).

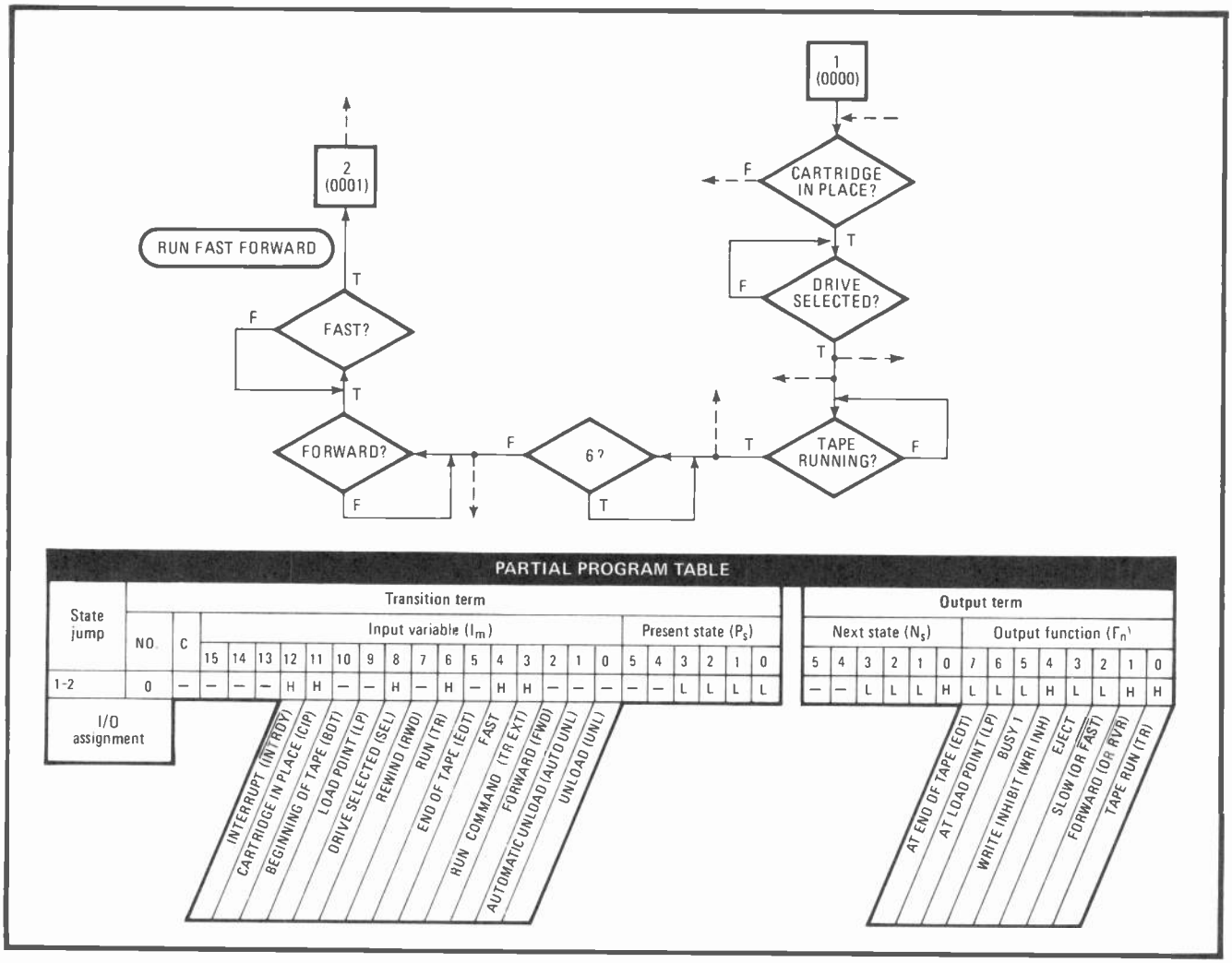
CIP = true implements a jump from state 8 to 9. In state 9 the tape will rewind in fast reverse until a BOT mark is reached. BOT true implements a jump from state 9 to 10. The tape now runs at slow speed in the forward direction until the load point (LP) is reached. LP true implements a jump from state 10 to 11 indicating STOPPED AT LP. From state 11, forward, reverse, or unload commands can be executed, but not rewind, because of the state 11 condition preceding state 9. That keeps RWD from being needlessly repeated.

State jump

A single state jump is shown in detail in Fig. 7. The transition is from state 1 to 2. In the latter, the controller is required to enter the READ FAST FORWARD routine from STOP when:

- CIP is true.
- SEL is true.
- TR is true.
- State 6 is false.
- FWD is true.
- FAST is true.

In response to this jump, the controller outputs that must change to issue the appropriate commands are run (TR),



7. Detailed state jump. The transition from state 1 (STOP) in the tape cartridge controller to state 2 (READ FAST FORWARD) is shown in flow-chart form. That part of the logic sequencer coding of the state jump is shown below, including transition and output terms.

TABLE 1: COMPARISON OF DESIGN ALTERNATIVES FOR TAPE CONTROLLER

Parameter	Field-programmable logic sequencer	Discrete logic	Monolithic Memories Inc.'s Programmable Array Logic
Chip count	1 chip	6 chips	14 chips
Circuit-board area	0.84 $in.^2$	2.13 $in.^2$	3.78 $in.^2$
Power (typical)	0.60 W	1.36 W	4.8 W
Speed	90 ns/state	132 ns/state	105 ns/state
Voltage	+5 V	+5 V	+5 V
Cost (high-volume production)	$12	$14	$48

TABLE 2: PROGRAMMING EQUIPMENT FOR THE FIELD-PROGRAMMABLE LOGIC FAMILY

Type	Manufacturer	Model	Field-programmable device				Availability
			Gate array	Logic array	ROM patch	Logic sequencer	
Logic	Signetics	FP-103	•				now
		FP-104		•	•	•	
	Curtis	PR-100		•			
		PR-100A		•	•		
	Data I/O	10		•	•		
Memory	Data I/O	17,19	•	•	•	•	3Q79
	Sunrise Electronics	SM100		•	•		now
			•			•	in development
Hybrid	Stag	PPX-Plus		•	•		now
			•			•	in development

forward (FWD), and fast (FAST).

The flow chart of the controller routines is complete with 14 states and 36 state jumps (including synchronous reset). As such, four state-register flip-flops sufficiently represent all states. All state jumps can be directly programmed into the chip from the flow chart. All state jumps occur on the leading edge of the clock.

The advantage of a controller built with the FPLS is best shown by a comparison to discrete logic, which would comprise PROMs, latches, and gates, using the same state diagram as for the FPLS. Table 1 compares the FPLS controller with a discrete implementation as well as with Monolithic Memories Inc.'s Programmable Array Logic chips, in several aspects.

Programming

The key to design flexibility with programmable logic is the availability of programming equipment. The need for PROMs in this equipment has led to a large number of memory programmers being offered by several manufacturers. Generally, they operate with personality card sets that meet the requirements of various PROM technologies. Suppliers have already begun developing sets compatible with memory programmers for logic devices. Hardware is expected to be available by the end of the third quarter of this year.

For the concept to work, the logic devices must be manipulated as memory chips are—by defining the desired fusing pattern in terms of an address-data relationship. Although this tends to obscure the logic function of the device, which is not visible on the program table, it is sure to provide low-cost programming equipment that can be manned by low-skilled labor.

Logic programming is another possibility, and low-cost equipment is already available from Signetics. Logic programmers allow direct entry of the logic function from the program table; no reference to the device logic diagram is necessary, and the user need not specify the status of each individual link in a device. Such programmers are more convenient for engineering use during the initial design phase, but with their high programming speed—about 10 seconds per device—can also be effective in production. Their only drawback is that they are dedicated machines and cannot program PROMs.

Some manufacturers offer a hybrid type of PROM programmer that can also be configured to do logic programming. Table 2 shows the various options available to prospective users now, or in the near future. □

Supersensitive measurement demands critical input design

The more esoteric sources of current and leakage must be taken into account when counting electrons

by Robert Miles, *Keithley Instruments Inc., Cleveland, Ohio*

☐ The success of the ongoing quest for electronic devices that do their jobs with less current at lower voltages brings with it an attendant problem: that of convenient measurement of these extremely low currents, voltages, and charges.

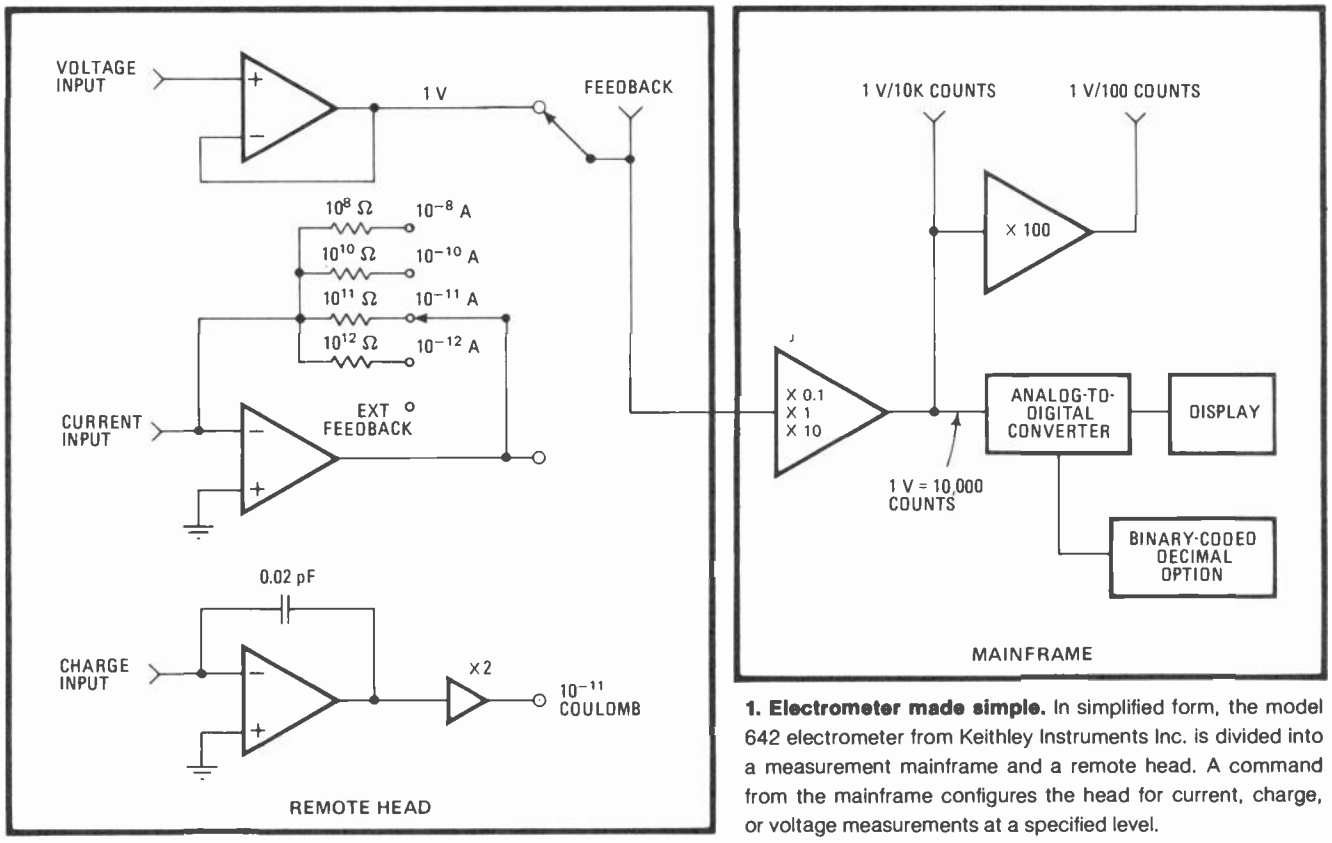
Recent improvements in MOS field-effect transistors and the development of complementary-MOS logic, bipolar FETs, and MOS FET operational amplifiers have reduced input and operational current requirements by decades. The widespread use of these and related devices with input currents in the picoampere range has increased the demand for ultralow-current and ultrahigh-impedance measurements.

Many other situations exist that require convenient, low-current measurements, such as the examination of semiconductor current-voltage relationships, low-level photodetector response, and other phenomena in specialized applications of physics and chemistry. The design of a portable, solid-state instrument such as the Keithley model 642 electrometer [*Electronics*, Dec. 7, 1978, p. 159] shown in Fig. 1 embodies the concepts and techniques necessary to make measurements at these levels and so bears close examination.

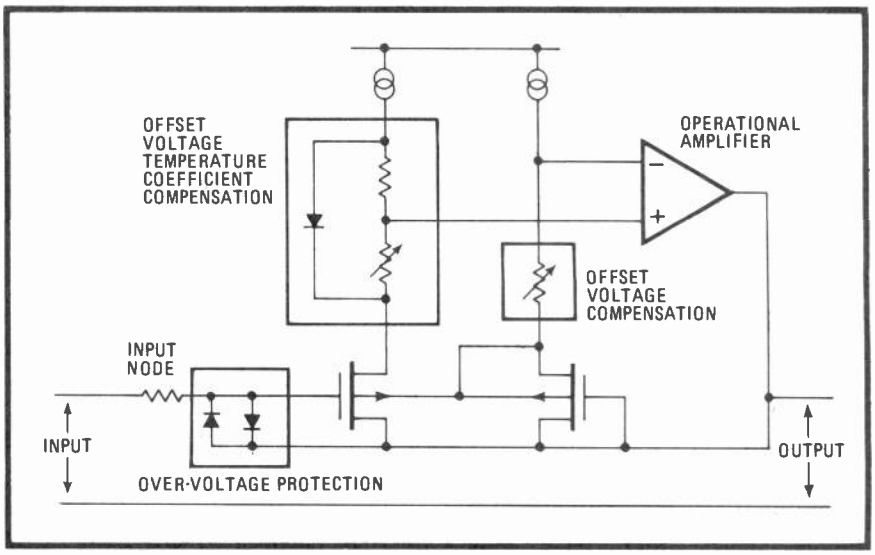
Extremes

Basically, an electrometer is a refined direct-current multimeter. It can be used for virtually any task normally performed by a conventional multimeter. But its input characteristics permit it to perform voltage, current, resistance, and charge measurements far beyond the realm of the conventional multimeter.

An electrometer's input resistance is very high, typically above 10^{14} ohms and sometimes as high as 10^{16} Ω. Offset current at the input is typically 5×10^{-14} ampere



1. Electrometer made simple. In simplified form, the model 642 electrometer from Keithley Instruments Inc. is divided into a measurement mainframe and a remote head. A command from the mainframe configures the head for current, charge, or voltage measurements at a specified level.



2. More for less. In addition to providing less expensive circuitry, the use of MOS field-effect transistors in the electrometer's input circuit allows compensation for offset voltage and its temperature coefficient. Both compensation networks can be independently located in either source lead.

or lower. These characteristics allow voltage measurement that causes only an extremely small amount of circuit loading. Electrometers are capable of monitoring current levels down to the theoretical limits imposed by the level of the input offset current: the Keithley 642's most sensitive current scale reads 200 femtoamperes full-scale. Full-scale charge readings on the instrument's 4½-digit display go from 10^{-10} to 10^{-12} coulomb; currents below 10^{-15} A are generally best measured using the charge function and a strip-chart recorder to monitor the analog output. In this way, resolutions of 10^{-17} A can be achieved. Its high input resistance and low current offset also enable the electrometer to measure resistances from ordinary levels up to extremely high values.

At these levels of measurement, the user must always be sure that the interconnecting structure that carries the signal from the current or voltage source being measured to the input connector of the electrometer does not contribute to or otherwise degrade that signal.

Detection

Central to any electrometer design is the active input device that detects the voltage imbalance at the input junction (or input node). A number of useful criteria exist for the selection and evaluation of such devices: the input gate current and resistance, the offset voltage stability with time and temperature, the voltage and current noise, and the complexity of any associated circuitry needed.

The electrometer input devices most widely used today are MOS FETs, but it is difficult to obtain them with input gate currents below 10^{-14} A. For the model 642, a minimum input current requirement of 5×10^{-17} A was established (about 300 electrons per second).

Other instruments capable of measuring inputs at this level employ a vibrating capacitor, or reed, as the input device. These capacitors and their associated circuitry are relatively costly, and the circuitry presents additional performance problems. The forward gain block in a vibrating reed configuration consists of an alternating-current amplifier with multiple poles in its response when mapped in the complex frequency plane. The amplifier's stability is easily compromised if there is an additional pole in any feedback network.

A solid-state input device, on the other hand, with an output response down to dc, permits the use of an integrated circuit operational amplifier with only a single, dominant pole in its response. Its performance stability with feedback is therefore much better than that of the vibrating reed circuitry. Its overall cost is lower, as well.

Plugging the leaks

The MOS FET input gate current is lowered by dealing with two of its major leakage mechanisms: that of the header and the leads. Special die processing and packaging eliminates all unguarded leakage paths save that of the silicon dioxide gate insulation. The MOS FET die is mounted on an alumina substrate which in turn is affixed to a TO-8-package metal header. The use of the alumina substrate avoids committing the header to the MOS FET substrate, so each lead in this package passes through a glass feed-through insulator and is both shielded and guarded from all other leads by the header. Guarding is a construction technique wherein all potential leakage paths from the conductor being guarded are interrupted by another conductor that is driven (by a low-impedance source) to the potential of the guarded conductor.

Another advantage in using MOS FETs is that they allow compensation for offset voltage and its temperature coefficient. In the 642 electrometer, the input MOS FET is operated as a source follower, with another MOS FET providing a gate-to-source voltage reference; each MOS FET's source is driven by a constant current supply, as shown in Fig. 2. The operational amplifier gain block is then driven from the dual MOS FET source. The offset-voltage temperature coefficient is cancelled by a portion of the forward voltage of a silicon diode mounted in close proximity to the input MOS FET. A fixed-source resistance is used to cancel any residual MOS FET offset or diode forward voltage. With this configuration, a voltage-offset temperature coefficient of 30 microvolts/°C is obtained; vibrating-reed input devices typically have a temperature coefficient of about 100 μV/°C.

In the light of the sensitive input characteristics of any

Three measurement demons

Heat. In a resistor, the kinetic energy of molecules produces motion of electrical charges. These charge movements result in noise called Johnson, thermal, or heat noise. In theory, the power available from this motion is constant and given by:

$$P = 4kT\Delta f$$

where k = Boltzmann's constant, T = temperature in kelvins, and Δf = the noise bandwidth in hertz over which the measurement is being made. Metallic conductors approach this theoretical noise level; other materials produce more noise than theory predicts. From the equation, Johnson voltage noise (E, in volts root mean square) developed in a resistor, R, can be found:

$$E = (4kT\Delta fR)^{1/2}$$

and Johnson current noise (I, in amperes rms) becomes:

$$I = (4kT\Delta f/R)^{1/2}$$

Pressure. Piezoelectric currents are generated when mechanical stress is applied to certain insulating materials, notably ceramics and other crystalline material. Teflon and some other plastics used for insulated terminals and interconnecting hardware exhibit what is known as a space charge effect, wherein an applied force creates a change in capacitance and thus a charge redistribution. The behavior is the same as for piezoelectric materials: a physical force creates a current.

Friction. Triboelectrically generated currents result from the creation of charges at the interface between a conductor and an insulator due to frictional forces at the interface, as in the case of a cable that is moved. The mechanism involved is one of rubbing off electrons, creating a charge imbalance and thus a current flow. Low noise cables are available that have a conductive coating (usually graphite) at the metal-insulator boundary, reducing this effect significantly. Currents down to 1 picoampere can be measured using cables treated in this manner. Rigidly securing the cable from any movement will permit its use down to a few femptoamperes. Rigid airline coaxial cable such as GenRad GR874 series is suitable down to 0.1 fA. Below this current level, special connection schemes and the use of high quality insulators such as sapphire are required.

electrometer, input over-voltage protection is essential. Silicon diodes can be used to limit the input-to-guard potential during input overload, but an additional leakage source at the input is the price paid. Available devices reduce this leakage to 10^{-14} or 10^{-15} A.

To obtain better leakage characteristics, the junction characteristics of diodes made from other materials were examined. Experimentation showed that gallium phosphide (GaP) diodes had better leakage characteristics at low voltages, with both forward and reverse bias.

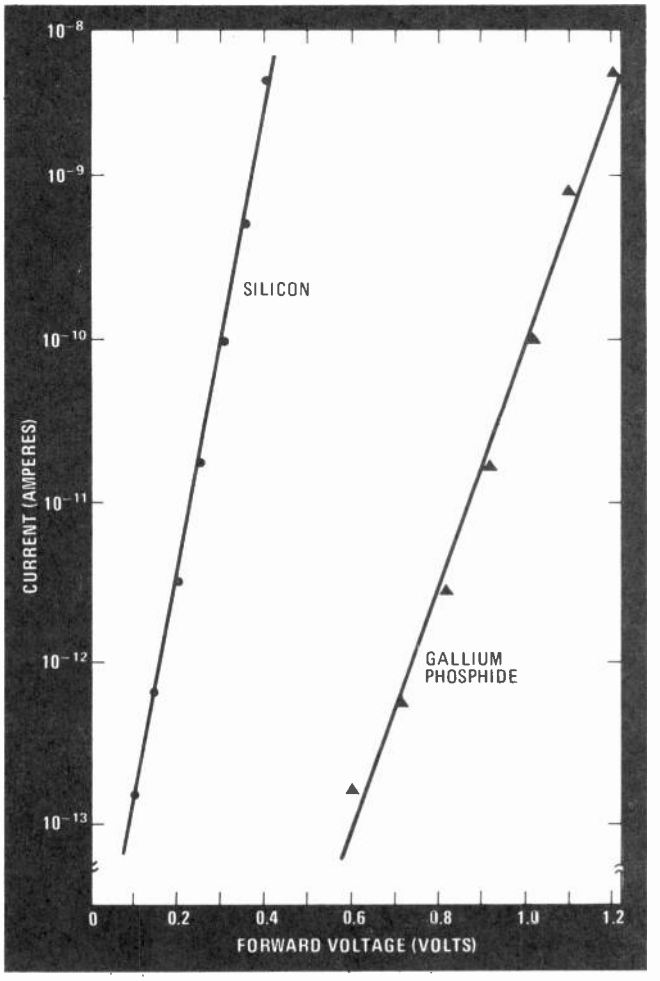
Johnson noise

A more important concern is the impact of the input protection device on the instrument's input current noise. To minimize Johnson current noise (see "Three measurement demons") that could degrade input resolution, particularly in the charge function, the resistance across the amplifier input must be maximized. A number of sources contribute to input resistance, including structural insulators, the input MOS FET, and the input protection device. Of these, the resistance of the input protection device is the most significant.

Evaluation of available silicon and gallium phosphide diodes yielded the characteristic current-voltage plots shown in Fig. 3. By extrapolating these plots, an estimate of the junction resistance at zero forward bias for silicon (7.5×10^{12} Ω) and gallium phosphide (3.9×10^{16} Ω) was obtained.

Although these figures have not been rigorously verified for very small forward bias voltages, they serve to indicate the superiority of GaP, which is borne out in the actual performance of the 642. The GaP diodes are connected back-to-back in the instrument and mounted in a guarded package similar to that used for the input MOS FET. The resistance in series with the input (see Fig. 2) limits the input overload current.

The selection of an insulating material to mechanical-



3. Si vs GaP. The choice of gallium phosphide rather than silicon diodes for overvoltage protection is dictated by GaP's higher junction resistance. Estimates of both diode types' resistances near zero forward voltage are obtained from the slope of the plots shown.

TABLE 1: PROPERTIES OF INSULATING MATERIALS

Material	Volume resistivity (ohm-centimeters)	Resistance to water absorption	Minimal piezoelectric effects	Minimal triboelectric effects
Sapphire	$10^{16} - 10^{18}$	■	■	□
Teflon	$10^{17} - 10^{18}$	■	■	■
Polyethylene	$10^{14} - 10^{18}$	□	■	□
Polystyrene	$10^{12} - 10^{18}$	□	□	■
Kel-F	$10^{17} - 10^{18}$	■	□	■
Ceramic	$10^{12} - 10^{14}$	■	□	■
Nylon	$10^{12} - 10^{14}$	■	□	■
Glass epoxy	$10^{10} - 10^{17}$	■	□	■
Polyvinyl chloride	$10^{10} - 10^{15}$	■	□	□
Phenolic	$10^{5} - 10^{12}$	■	■	■

Key: ■ Very good in regard to the property; □ Moderately good in regard to the property; ■ Weak in regard to the property

TABLE 2: COMMON THERMOELECTRIC POTENTIALS

Materials	Potential (microvolts/°C)
Cu – Cu	0.2
Cu – Ag	0.3
Cu – Au	0.3
Cu – Cd/Sn	0.3
Cu – Pb/Sn	1 – 3
Cu – CuO	1,000

ly support and electrically isolate the input node is a key element in the performance of any electrometer or low-current instrument. Material properties that must be considered are volume resistivity, water absorption, and susceptibility to piezoelectric and triboelectric effects (see "Three measurement demons"). Table 1 compares these properties for many commonly available insulating materials. Not only is sapphire an excellent choice for its insulating properties, but it provides a rigid mounting surface for the input node. Its performance in the 642 was further enhanced through the use of guarding.

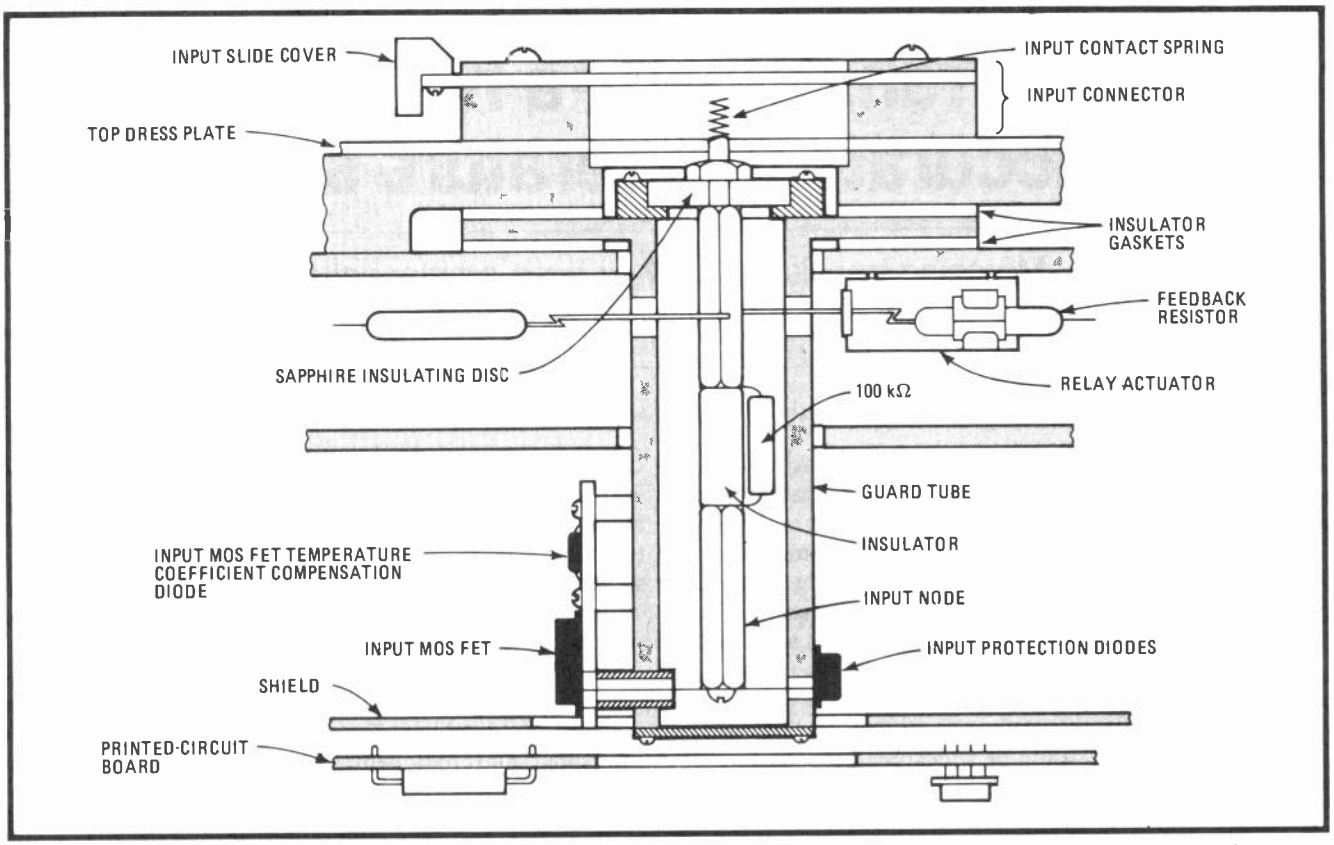
As important as the input device, input protection, and insulation are to the operation of the electrometer is their structural configuration. In the 642's remote head, the input node (Fig. 4) is a rod-like conductor that runs downward from the input connector to the MOS FET input device and its protecting GaP diodes. A guard tube surrounds the conductor coaxially and a sapphire insulating disk supports the conductor at the connector end. The input devices at the opposite end are mounted on the guard tube. Minimizing the volume surrounding the input node reduces the ion-chamber effect caused by background radiation.

Feedback connections are made through holes along the length of the guard tube. Feedback elements are used to convert the input current or charge to a voltage that can in turn be transformed by an analog-to-digital converter into a numerical value for display. The high-value resistors used for current-to-voltage conversion are mechanically supported by their glass enclosure; a special relay mechanically manipulates a lead from the resistors so that it contacts the input node through a hole in the guard tube. Charge-to-voltage conversion is accomplished by connecting a specially constructed sapphire-insulated, air-dielectric capacitor to the node in much the same way as are the high-value resistors. The feedback elements and the relay actuators are mounted radially on two levels along the length of the guard tube and normal to it.

Avoiding ionization

The rest of the remote-head electronics are on a printed-circuit board at the bottom of the enclosure; this circuitry is shielded by a metal plate to prevent it from ionizing air in the region around the input node.

Within the realm of low-current measurement, ionizing radiation can be a significant source of error currents. As noted, the susceptible portion of the struc-



4. Heading off trouble. Careful design and solid construction of the 642's remote head prevent problems from a number of sources: piezoelectric and triboelectric potentials, electromagnetic coupling, alpha radiation, and vibration, among others.

ture is the air volume between the input node and the guard tube, which in effect forms an ion chamber.

The air ionization along the path of an alpha particle greatly exceeds that caused by any other constituent of background radiation. Since alpha particles will not pass through metals of any appreciable thickness, the only possible alpha sources that can affect measurements are the metals used to construct the node and guard—a fact that has been experimentally verified. Similar sources of low-level radiation have recently been credited with causing soft errors in charge-coupled devices and dynamic MOS memories.

The alpha-particle emissions of various materials have been measured; this data was consulted in designing the 642. Domestic lead produces many alpha particles, but there is no detectable activity above background for cadmium, so cadmium-plated, low-lead brass was used throughout the remote head. Cadmium solder was used in place of tin-lead solder for structural and electrical connections in the vicinity of the input node to further minimize alpha radiation. Other low-alpha materials are gold and silver.

Although thermoelectric potentials do not normally present problems in high-impedance circuits, they can be a factor when operating at high voltage sensitivities. They develop at the junctions of dissimilar metals, a fact that is made use of in thermocouples. The potentials are a function of the metals' properties, their impurities, and the temperature gradient across the junction. Table 2 lists some typical thermoelectric potentials.

With careful mechanical design, these error sources can be reduced or eliminated. When dissimilar-metal junctions cannot be avoided, heat sinks can be arranged so as to reduce the temperature gradient across them.

By dividing an electrometer into a mainframe with the controls and display and a separate remote input head, the sensitive input circuitry can be located directly at the signal source, and the path over which low-level signals must travel can be minimized. This separation also removes the instrument's operator from the measurement environment, where he might inadvertently affect the sensitive circuitry.

Physical integrity

Rigid construction of all parts of the remote head serves to reduce or eliminate spurious input signals due to vibration or distortion. A sealed environment and an internal, replaceable or rechargeable dessicant help to maintain the integrity of the remote head's internal insulators and high-impedance circuitry. (The external insulators that support the input node must be kept clean since contamination or high humidity may degrade the insulator's surface resistivity or, in the case of contamination by ionic chemicals, weak "batteries" between two conductors may form. The guarded insulator minimizes the effect of shunt resistance in the former case, but has no effect in the latter.)

A contaminant not normally considered is light. At ultralow current levels, photoemission—predominantly from solid-state components—can become significant. For the 642, this problem is addressed by using opaque glass feed-through insulators for such devices' leads. □

Transistors—a hot tip for accurate temperature sensing

Matching transistors by their base-emitter voltage and dc gain ensures consistent operation from unit to unit

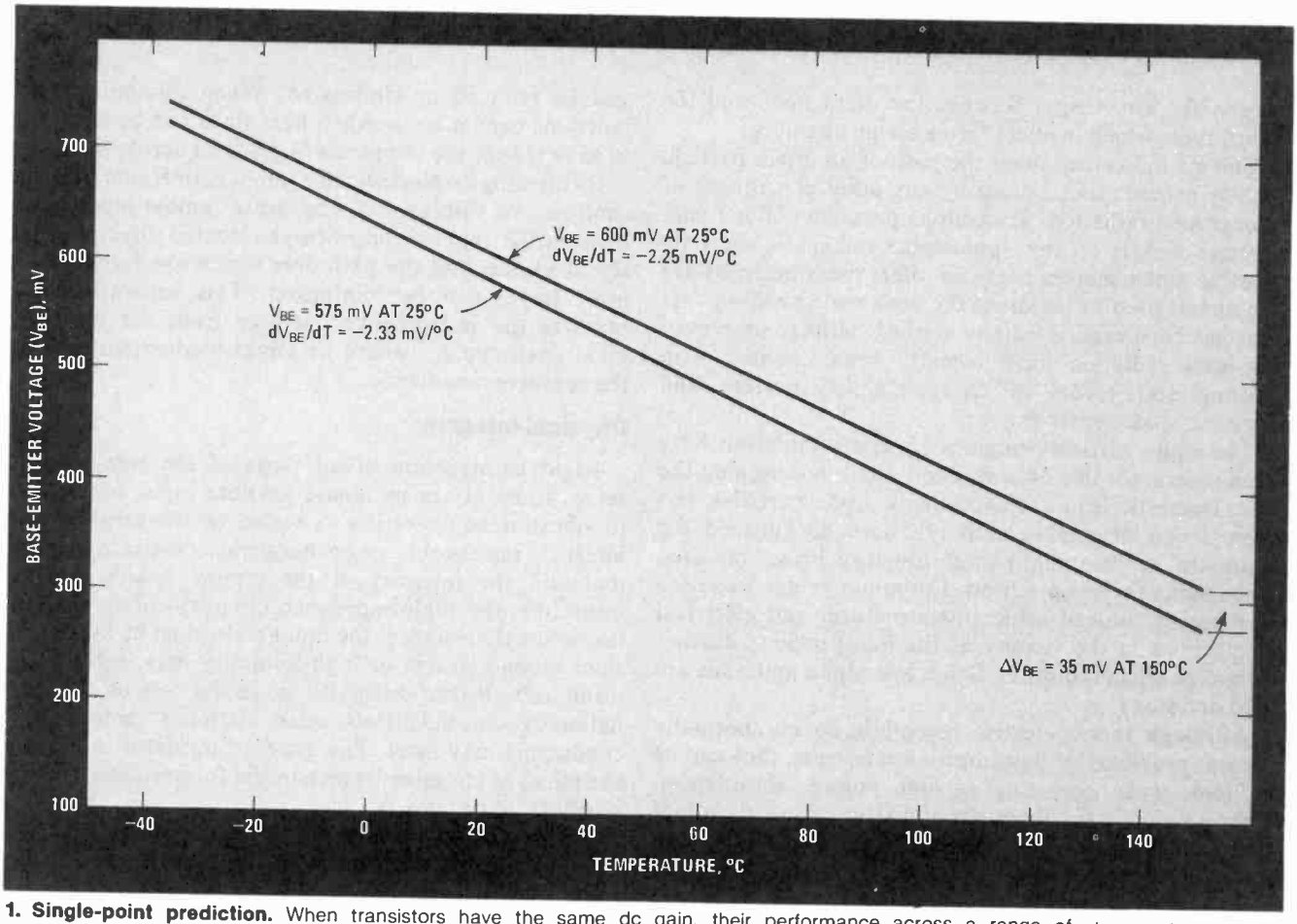
by Pat O'Neil and Carl Derrington, *Motorola Semiconductor Products Inc., Phoenix*

☐ Transistors would seem to be ideal temperature sensors. Their low cost, their ability to operate consistently over long periods, and their sensitivity and linearity recommend them for this use. For some time, in fact, temperature measurements have been made using the base-emitter voltage of forward-biased transistors.

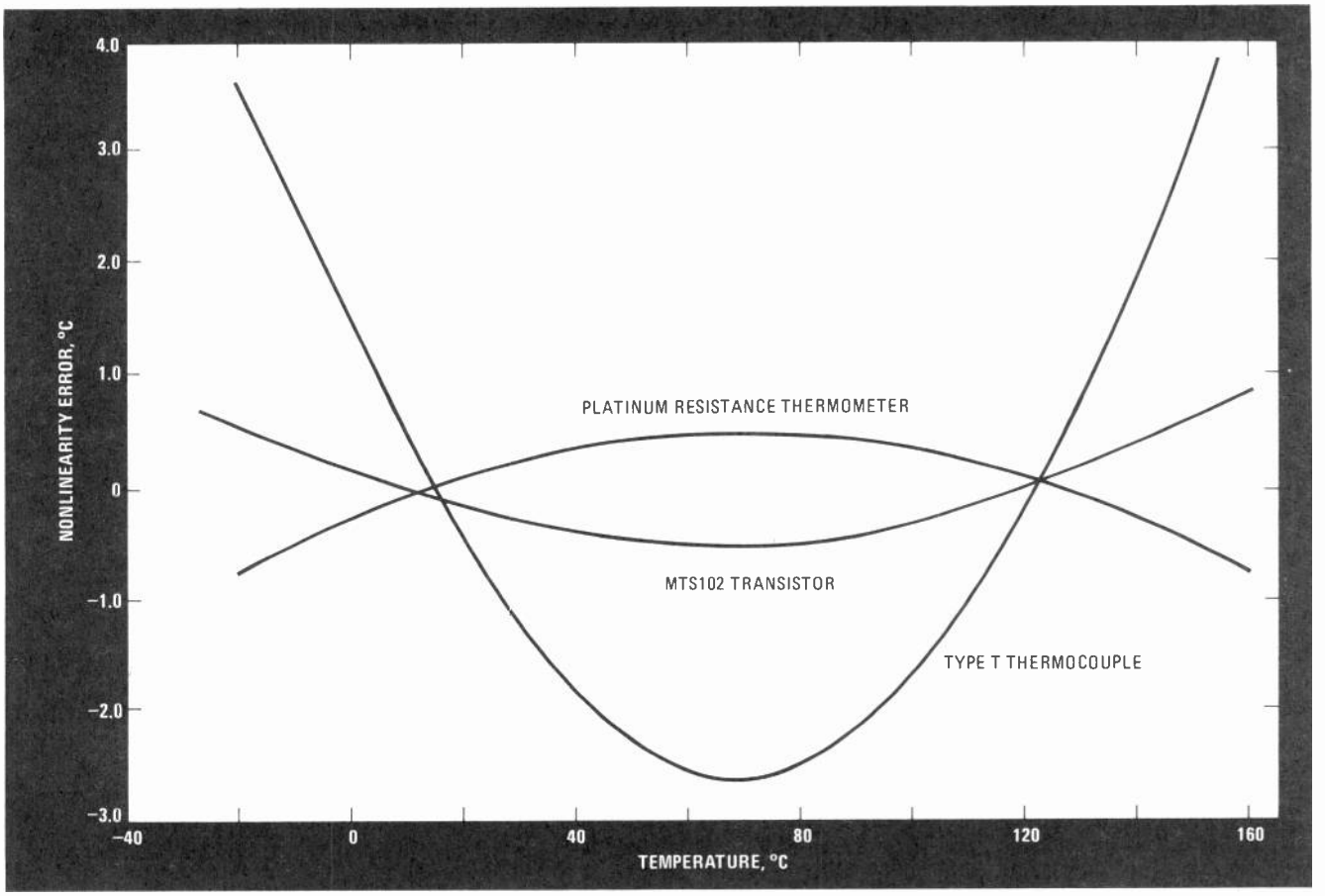
The big problem in using transistors in this application has been that of finding transistors with characteristics matched closely enough to allow them to be used interchangeably. If it were not for this difficulty, their use as temperature sensors would be widespread indeed.

The quest for interchangeable semiconductor sensors has led manufacturers to build monolithic integrated circuits whose output is the difference of two junctions with differing current densities or ones that employ laser trimming to equalize circuit parameters. Although these techniques do provide interchangeable devices, they do so at a cost that prohibits their use in throwaway applications—monitoring the curing temperature of concrete with imbedded sensors, for example.

But the improvements in production line capability that make large-scale integration possible also make it possible to produce discrete transistors with tightly controlled and matched geometries. Motorola's MTS family is a transistor series selected specifically for temperature sensing applications. It consists of three



1. Single-point prediction. When transistors have the same dc gain, their performance across a range of temperatures can be predicted by measuring their base-emitter voltage at a specific temperature. Variation in V_{BE} can result in large errors.



2. In context. Although they are inherently nonlinear, transistors perform quite admirably when compared to other devices. Between -40° and + 150°C, the MTS102 rivals more expensive platinum resistance thermometers and easily outshines type T thermocouples.

transistor types: the 102, 103, and 105, which provide guaranteed accuracies to within ±2°, ±3°, and ±5°C, respectively, over the range from −40° to +150°C.

Transistors with these accuracies are obtained by screening transistors for matched direct-current gain and base-emitter voltage at room temperature, using a constant collector current of 100 microamperes. For any type within the family, the base-emitter voltage (V_{BE}) must be within a specified tolerance; nominal V_{BE} may be any value from 580 to 620 millivolts. For example, the V_{BE} of an MTS102 is matched to a tolerance of ±3 mV and the nominal figure, say 600 mV, is printed on its package. Any MTS102 can be used to replace another with the same V_{BE} with the stated ±2°C accuracy maintained. In matched lots of 10,000, the sensors are priced at 27 to 66 cents apiece, depending upon the temperature tolerance.

Electrical consistency

For any given series of transistor temperature sensors, it is necessary to specify only the relevant and measurable electrical characteristics—V_{BE} and the direct current gain at some temperature—to ensure consistent operation within a known tolerance from sensor to sensor. Furthermore, circuits can be built using such transistors that provide accuracies within ±0.01°C. The design of these circuits requires an understanding of the temperature dependence of the transistors' measured parameters. The best route is an examination of the equations that describe a transistor's operation.

The base-emitter junction of a transistor can be regarded as a simple pn junction diode. If a constant current, I_F, is forced through the junction in a forward direction, then its relation to the measurable junction voltage, V_J, is given by the Shockley equation:

$$I_F = I_{sat}e^{qV_J/kT-1} \quad (1)$$

where k is Boltzmann's constant, q is the net charge in coulombs, T is the temperature in kelvins, and I_{sat} is the saturation current.

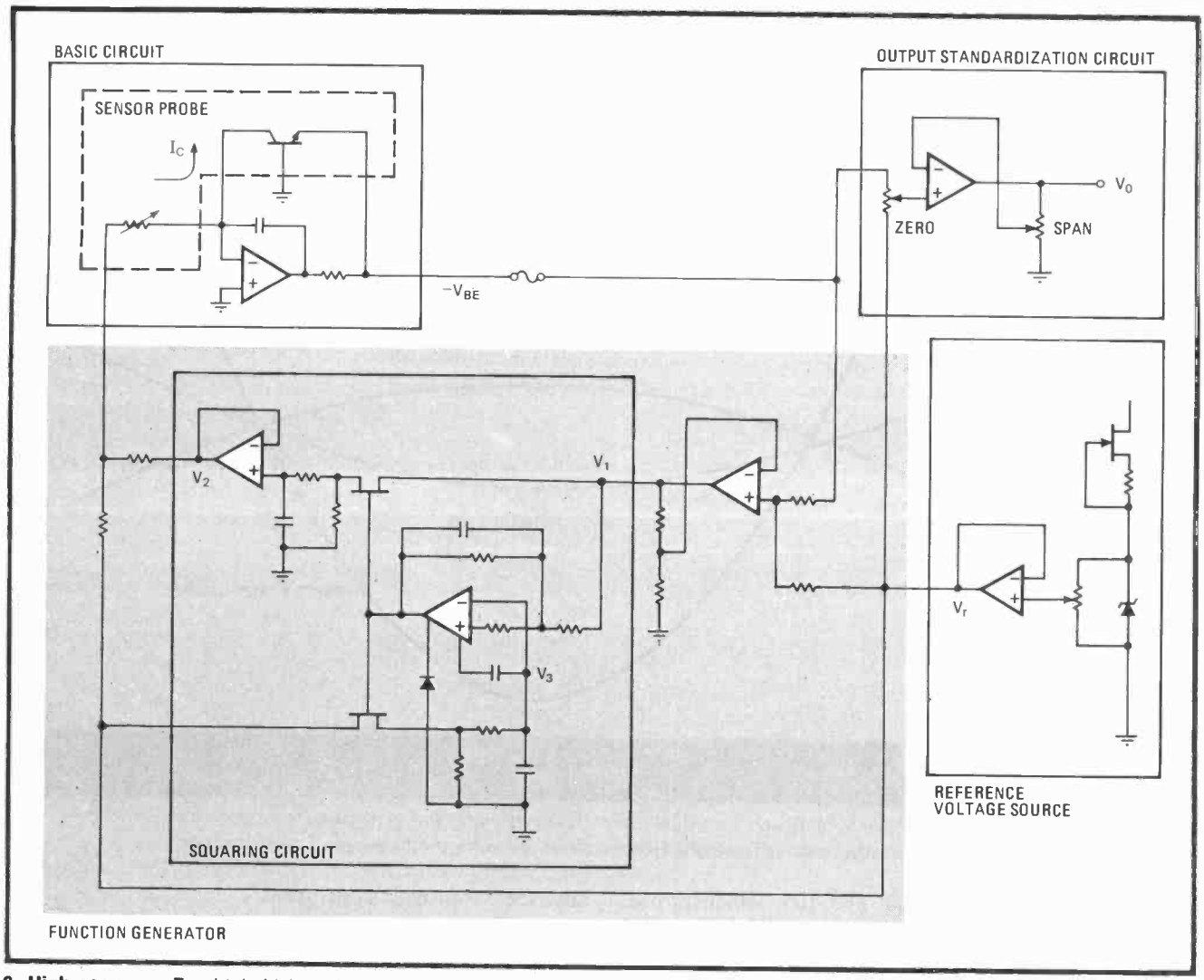
When the junction voltage is sufficiently large (that is, when the diode is sufficiently forward-biased), the −1 term in the exponent can be ignored and the equation can be expressed in terms of V_J:

$$V_J \cong (kT/q)\ln(I_O/I_{sat}) \quad (2)$$

With I_F held constant, if all other terms in the equation were independent of temperature, the junction voltage would be directly proportional to the thermal voltage expression kT/q and thus to temperature T. Unfortunately, the saturation current is composed of two temperature-dependent currents: that due to the hole diffusion, I_p, and that for the electrons, I_n. The hole-diffusion current is given by:

$$I_p = qA(D_p/L_p)p_{no}$$

where A is the area of the device, D_p is the diffusion constant for the holes, L_p is the diffusion length for holes



3. High accuracy. To obtain high performance, the collector current of temperature-sensing transistors can be varied in accordance with temperature (reflected by base-emitter voltage) raised to some power. The squaring circuit shown performs this function.

in the n region, and p_{no} is the equilibrium hole concentration in the n region.

The last term, p_{no}, is temperature-dependent and is defined by:

$$p_{no} = n_i^2/N_D$$

where N_D is the concentration of donor atoms imparted to the material by doping and n_i^2, the square of the intrinsic concentration, is given by:

$$n_i^2 = N_c N_v e^{-E_G/kT}$$

The terms N_c and N_v are the equivalent concentrations of conduction and valence states for the doped material; E_G is the potential of the energy gap between bands in electron volts.

Defining saturation

The equation for I_n is similar to that for I_p, with appropriate substitution of n terms for p terms: D_n is the diffusion constant for electrons, L_n is the diffusion length for electrons, and N_A is the concentration of acceptor atoms.

Adding the equation for I_p to the equivalent equation for I_n results in the following expression for the saturation current:

$$I_{sat} = I_p + I_n = qAN_cN_v e^{-E_G/kT} g \qquad (3)$$

where g represents $[D_p/(L_pN_D)] + [D_n/(L_nN_A)]$. Substituting this expression into Eq. 2 gives:

$$V_J \cong E_G/q + (kT/q)\ln[I_F/(qAN_cN_vg)]$$

Again, this seems to result in a directly linear relationship of voltage to temperature. But the terms D_p and D_n are both related to temperature-dependent terms: the thermal velocities of holes and electrons. Furthermore, this dependence need not be identical. So while the quantity represented by g above can be obtained by a measurement of V_J at a specific temperature, finding that two V_Js are equal at that temperature in no way guarantees that they will be equal at another.

Fortunately, there is the familiar dc gain term for the transistor, h_{FE}. This term represents the relationship:

$$h_{FE} = I_n/I_p = [D_n/(L_nN_A)]/[D_p/(L_pN_D)]$$

If the dc gains of two transistors are equal, it means that I_n and I_p vary in the same way with respect to one

Bounding the error

The curves in Fig. 1, which are used to set a tolerance for V_{BE} that limits the temperature measurement error, assume a linearity for transistors that does not exist, as experience proves. A demonstration that these linear curves form the boundaries of possible error is required for confidence in their use.

The assumption that the transistor's V_{BE} is linear leads to the following expression for the approximate value of V_{BE} ($\tilde{V}_{BE}$):

$$\tilde{V}_{BE} = \tilde{V}_{BE1} + (dV_{BE}/dT)(T - T_1)$$

Since the measured curve is not linear, the error in the above expression can be minimized by using the following linear regression coefficients to adjust measured values:

$$d\tilde{V}_{BE}/dT = \{(V_{BE} - \{V_{BE}\})(T - \{T\})\}/\{(T - \{T\})^2\}$$
$$\tilde{V}_{BE1} = \{V_{BE}\} - (dV_{BE}/dT)(\{T\} - T_1)$$

where the symbols $\{\ \}$ indicate the average value of the enclosed quantity within the operating range.

If T_1 is now chosen to be the average temperature in the range from $T_1 - \Delta T$ to $T_1 + \Delta T$, the above equation can be restated as:

$$d\tilde{V}_{BE}/dT = (r/3)(k/q) - (V_{go} - V_{BE1})/T_1 - (r/2)(k/q)(T_1/\Delta T)^2[1 - f_1(1 + \Delta T/T_1)(1 - 2\Delta T/T_1) + f_2(1 - \Delta T/T_1)(1 + 2\Delta T/T_1)]$$
$$\tilde{V}_{BE1} = V_{BE1} + (r/2)(k/q)T_1(1 - f_1 + f_2)$$

where

$$f_1 = (1 + \Delta T/T_1)/[2(\Delta T/T_1)\ln(1 + \Delta T/T_1)]$$
$$f_2 = (1 - \Delta T/T_1)/[2(\Delta T/T_1)\ln(1 - \Delta T/T_1)]$$

An examination of these expressions indicates that a simple bounded estimate of the error resulting from the assumption of linearity is obtained by joining the extreme points of the V_{BE}-versus-temperature curves, as has been done in Fig. 1. At temperature T_1, the resulting error is:

$$\Delta\tilde{V}_{BE} = (r/2)(k/q)[(1 + \Delta T/T_1)\ln(1 + \Delta T/T_1) + (1 - \Delta T/T_1)\ln(1 - \Delta T/T_1)]$$

another. So if two transistors have equivalent h_{FE} and V_J (which, for a transistor rather than a diode, is the base-emitter voltage V_{BE}), they will react in the same way with temperature variation. Thus they will be interchangeable for temperature-sensing applications.

Inherent nonlinearity

While defining the base-emitter voltage and dc gain does ensure similar operation, the inherent nonlinearity of the transistor must be considered if devices are to operate within a desired tolerance. Starting with the linear equations above, it is possible to move into the world of real, nonlinear operation to see how these parameters dictate actual performance.

For a transistor, I_F in Eq. 1 is actually the collector current I_C. If the summation term is expressed as a function of temperature, T, raised to some power r, substituting Eq. 3 for I_{sat} in Eq. 1 yields:

$$I_C = A'T^r e^{-qV_{go}/kT} e^{qV_{BE}/kT \cdot 1} \quad (4)$$

A′ represents the pre-exponential constants qAN_cN_v, and the band-gap potential of silicon at 0 K (V_{go}) multiplied by charge q has been substituted for the more general term E_G.

When the collector current is constant and V_{BE} is sufficiently large that the -1 term in the exponent of Eq. 4 can be ignored, it is possible to express V_{BE} in terms of a specific base-emitter voltage, V_{BE1}, known at temperature T_1:

$$V_{BE} = V_{BE1}(T/T_1) + V_{go}(1 - T/T_1) - r(kT/q)\ln(T/T_1)$$

This represents the basic relationship governing the operation of the transistor as a temperature sensor. Taking this equation's derivative with respect to temperature naturally gives the rate of change of V_{BE} with respect to temperature, usually referred to as the temperature coefficient:

$$dV_{BE}/dT = -rk/q - (V_{go} - V_{BE})/T$$

For the MTS series of transistors, an empirical version of this equation has been determined using a V_{BE} of 600 millivolts at 25°C:

$$dV_{BE}/dT = -2.25 + 0.0033(V_{BE} - 600)\ \text{mV/°C}$$

Figure 1 plots this equation when the actual V_{BE} is 600 mV and when it is 575 mV. Comparison of the two curves shows that variation in V_{BE} can result in measurement errors of as much as 15°C. Fortunately, it can be shown (see "Bounding the error," above) that specifying the maximum change in V_{BE} at the extreme points of the curve limits the possible measurement error.

Measured nonlinearity for a typical MTS102 transistor is shown in Fig. 2, along with typical nonlinearity curves for a type T thermocouple and a platinum resistance thermometer. Calculating the regression coefficients for a least-squares fit to a straight line (R^2 = 1.00000 for a perfectly linear device) yields a value of 0.99866 for a type T thermocouple and 0.99999 for the MTS102 and the platinum resistance thermometer. This indicates that the transistor is far superior to the thermocouple and equal in capability to the more expensive platinum thermometer for this range.

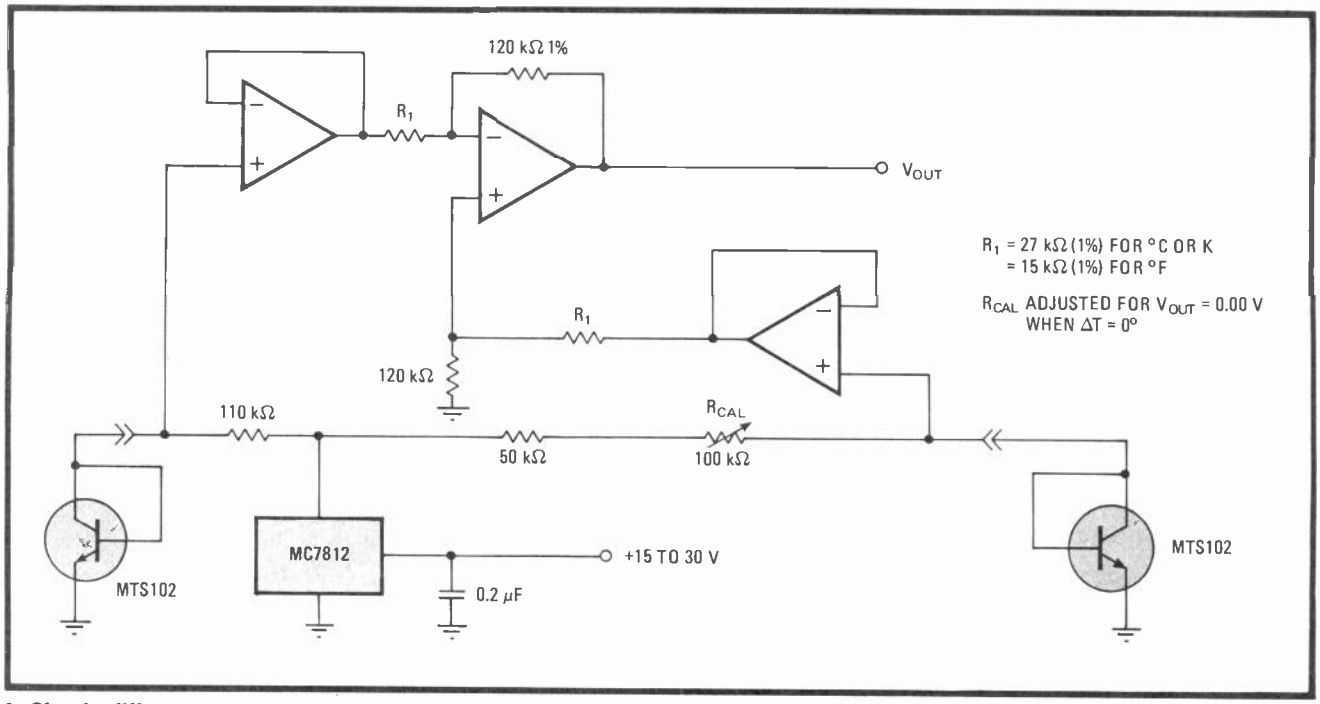
Circuits improve accuracy

There are, of course, many applications in which the error due to the nonlinearity shown would be unacceptable. For such cases, it has been found that the operation of transistor temperature sensors can be improved if the collector current I_C is forced to react in accordance with this equation:

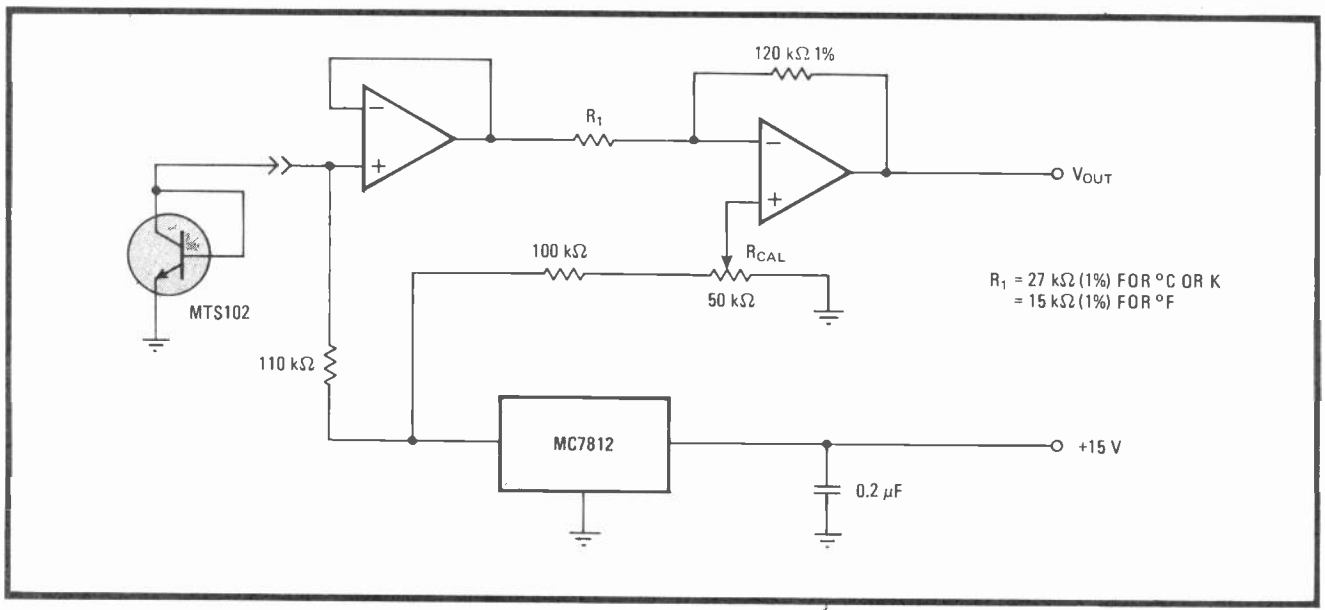
$$I_C = I_{C1}(T/T_1)^x$$

where I_{C1} is the collector current at T_1. The theoretical value of x at which nonlinearity ceases is r, the exponent of T in Eq. 4.

Using this concept, practical circuits have been built in which a standard transistor used as a sensor yielded accuracies within ±0.1°C (see Fig. 3).[1] Using a more



4. Simple difference. Differential temperature readings, frequently needed in process controlling, can be inexpensively obtained using the configuration shown. The same circuit could also be used to set an alarm when temperature stability is critical.



5. Even simpler. A single transistor version of the circuit shown in Fig. 4 requires even fewer components. Since the transistor itself is inexpensive, it and others like it can be left in place and the remaining circuitry built into a portable meter.

complex and precise squaring circuit and three-point calibration, ±0.01°C uncertainty can be achieved. It is also interesting to note that the worst-case error occurs when x is equal to zero (that is, when I_C is constant), as has been assumed throughout the preceding analysis.

Since it is possible to match transistors so that their responses track variations in temperature, there are many low-cost designs that are commercially viable. For example, Fig. 4 shows a design for a differential temperature sensing system that could easily be used for process monitoring. The output voltage of Fig. 5 can become the input to a digital multimeter that displays temperature in kelvins or degrees Centigrade or Fahrenheit.

Design engineers faced with the task of devising new systems for monitoring and controlling temperature would do well to bear in mind three important advantages of the transistor temperature sensor. First, it can be used interchangeably and is low enough in cost to be disposable. Second, the high sensitivity of this type of sensor provides a potential for increased accuracy, which can be realized by conditioning the collector current. Third, the transistors' relatively high output and span can often eliminate the need for amplifiers. □

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Floating current source drives automatized test fixture

by Richard M. Fisher
ADT Security Systems, Clifton, N. J.

This generator provides a programmable current to drive any load, making the unit ideal for production-line testing. Because the constant-current source floats—that is, is not connected to ground—it can drive loads energized either by positive or by negative potentials of as much as 90 volts.

The output current is resolved to 50 microamperes by the 10-bit input to a digital-to-analog converter (a). The maximum current that can be delivered to the load is slightly more than 50 milliamperes.

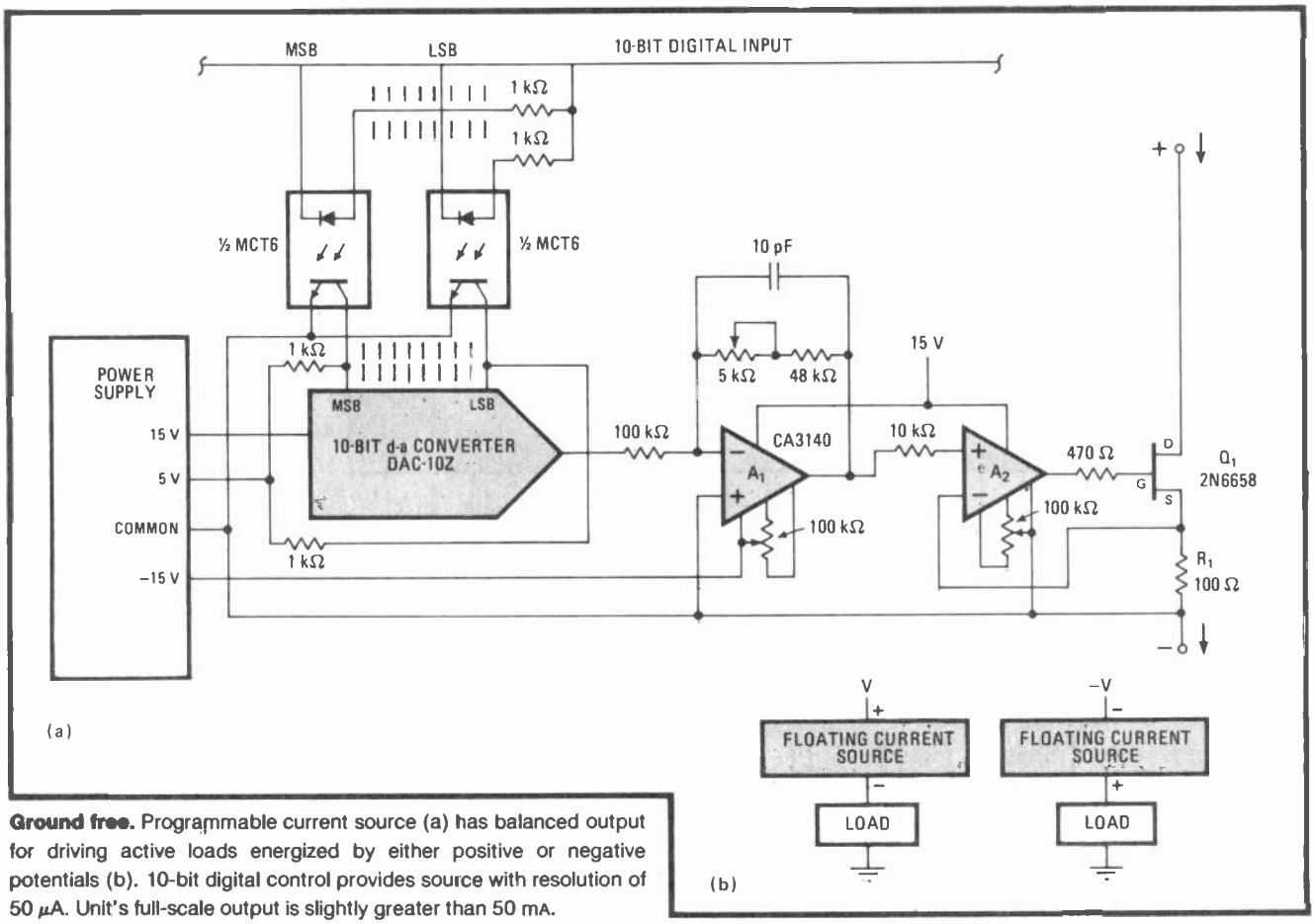
As shown, the 10-bit command input is transferred to the d-a device through optocouplers, thus isolating the DAC-10Z from ground paths under virtually all conditions. Note the 5-, +15-, and −15-V potentials for the generator are obtained from circuitry associated with the isolated secondary winding of the transformer in the power supply.

Operational amplifier A_1 inverts and scales the output of the d-a converter. The maximum output voltage from the converter is −9.99 volts and results in a full-scale output voltage of 5.115 V from A_1. A_2, in conjunction with R_1 (= 100 ohms), thus provides a full-scale output current of 51.150 mA.

The V-groove MOS field-effect transistor, Q_1, serves as a voltage-to-current converter. Q_1 performs the conversion at high accuracy, because the V-MOS device requires no gate current.

As for using the current source, implementation is easy with any energizing potential. If the device—the load—under test is driven by a positive voltage (b), it is necessary to connect the generator's positive output to the supply voltage. The negative port of the generator is brought to the load.

For negative potentials, the situation is similar, with source's positive terminal being connected to the load as shown. The negative port is connected to the supply voltage. □



Ground free. Programmable current source (a) has balanced output for driving active loads energized by either positive or negative potentials (b). 10-bit digital control provides source with resolution of 50 μA. Unit's full-scale output is slightly greater than 50 mA.

Counter banks stagger radar's pulse rate

by Prakash Dandekar
Tata Electric Companies, Bombay, India

In many radar applications, the instantaneous pulse-repetition frequency must be varied in an orderly fashion to improve the read-out accuracy of the system's moving-target indicator. Considerable circuitry is usually required to achieve the so-called staggered operation, but as shown here, two sets of synchronous counters can be easily connected to control the prf over any range, while providing superior MTI performance.

Normally, designers resort to transmitting pulses at each of three selected periods only, in order to simplify circuitry. Specifically, a popular technique is to transmit a group of three 1-microsecond pulses spaced at 1, 1.1, and 1.2 milliseconds repeatedly. When this is done, however, the filtered output of the MTI is not uniform and so—aside from causing discontinuities in the curve of MTI filter output versus target velocity—this method creates blind velocity points, or ranges over which velocity cannot be determined accurately.

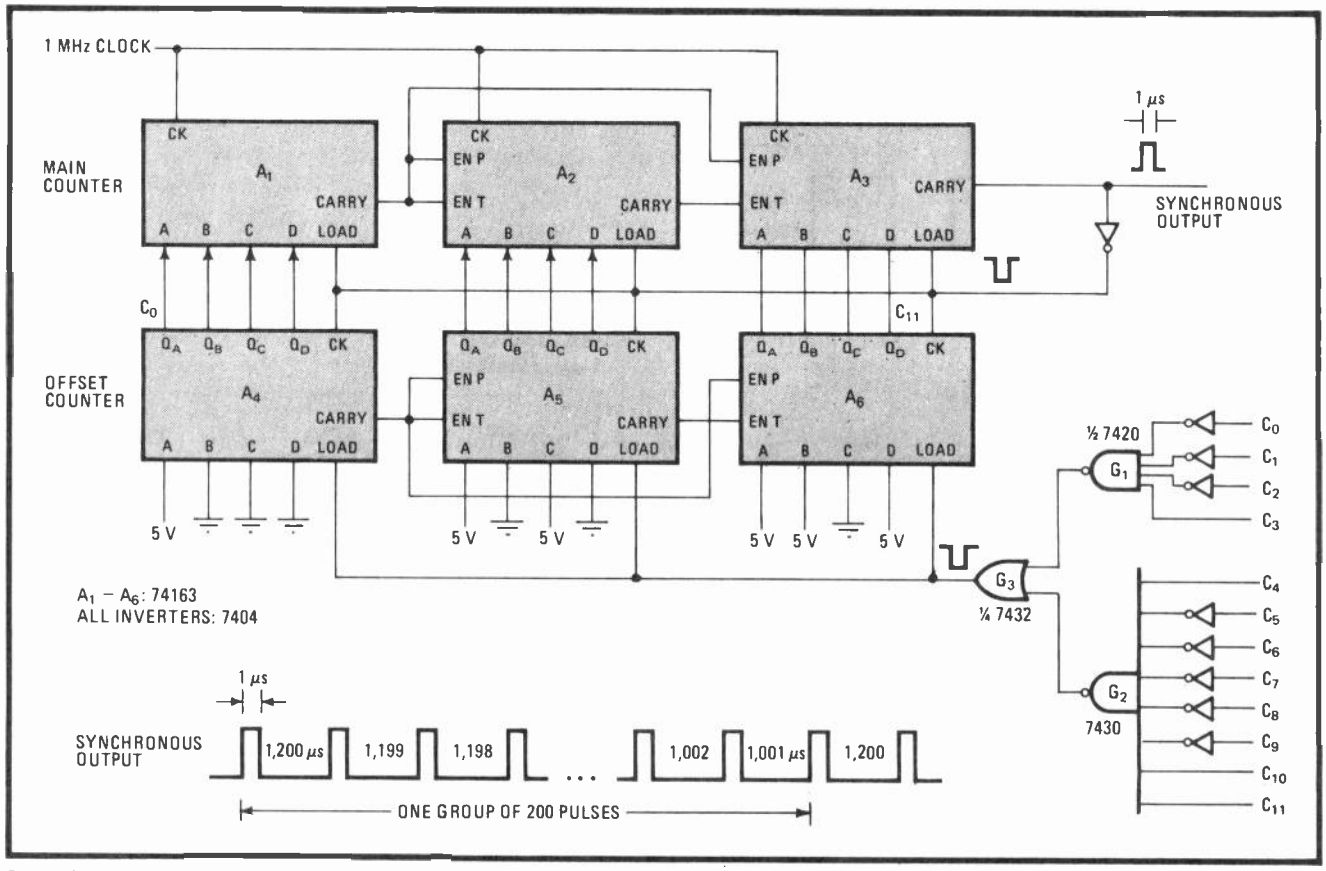
With this circuit, a perfectly smoothed response is achieved by increasing the number of staggered pulses per given time. Thus in this case, a group of 200 pulses, each having a time between pulses of $(1{,}201 - M)$ micro-seconds, where M denotes the Mth pulse of 200, are generated.

As shown, 12-bit counters A_1–A_3, comprising the main counter chain, advance at a 1-megahertz rate. When the counter reaches its maximum, the carry output of A_3, serving as the synchronous output, is generated.

The same signal is used to preset the main counter to a 12-bit binary number, N, which is determined by the state of the offset counter A_4–A_6. Because A_4–A_6 is also clocked, this unit is incremented with every sync pulse, so during each cycle the main counter is initialized at a higher value than it was previously. Thus the repetition time is reduced by 1 μs on each pass.

Note that the offset counter is initialized at a minimum value of $B51_{16}$ (see A–D inputs of A_4–A_6) and advances to a maximum of $C18_{16}$ ($= 2^{12}$) before it is reset by logic gates G_1–G_3. Thus, the difference between the counter's maximum and minimum is 200 counts, meaning the instantaneous pulse-repetition rate will vary from 1,200 to 1,001 microseconds. The maximum and minimum values may be easily changed, however, so that any pulse-repetition frequency range can be set.

When the counter reaches 3,096, corresponding to a rate of 1,001 μs, A_4–A_6 is loaded with $B51_{16}$. The rate becomes 1,200 μs once more, and the cycle is repeated. □



Smooth staggering. Two 12-bit counter chains generate a group of repeating N pulses spaced at $(1{,}201 - M)$ μs, where M denotes the Mth pulse of N. for incremental staggering of the radar-pulse rate. Master clock sets absolute value of maximum pulse-repetition frequency.

Compact industrial ammeter measures 10-ampere peaks

by Paul Galluzzi
Beverly, Mass.

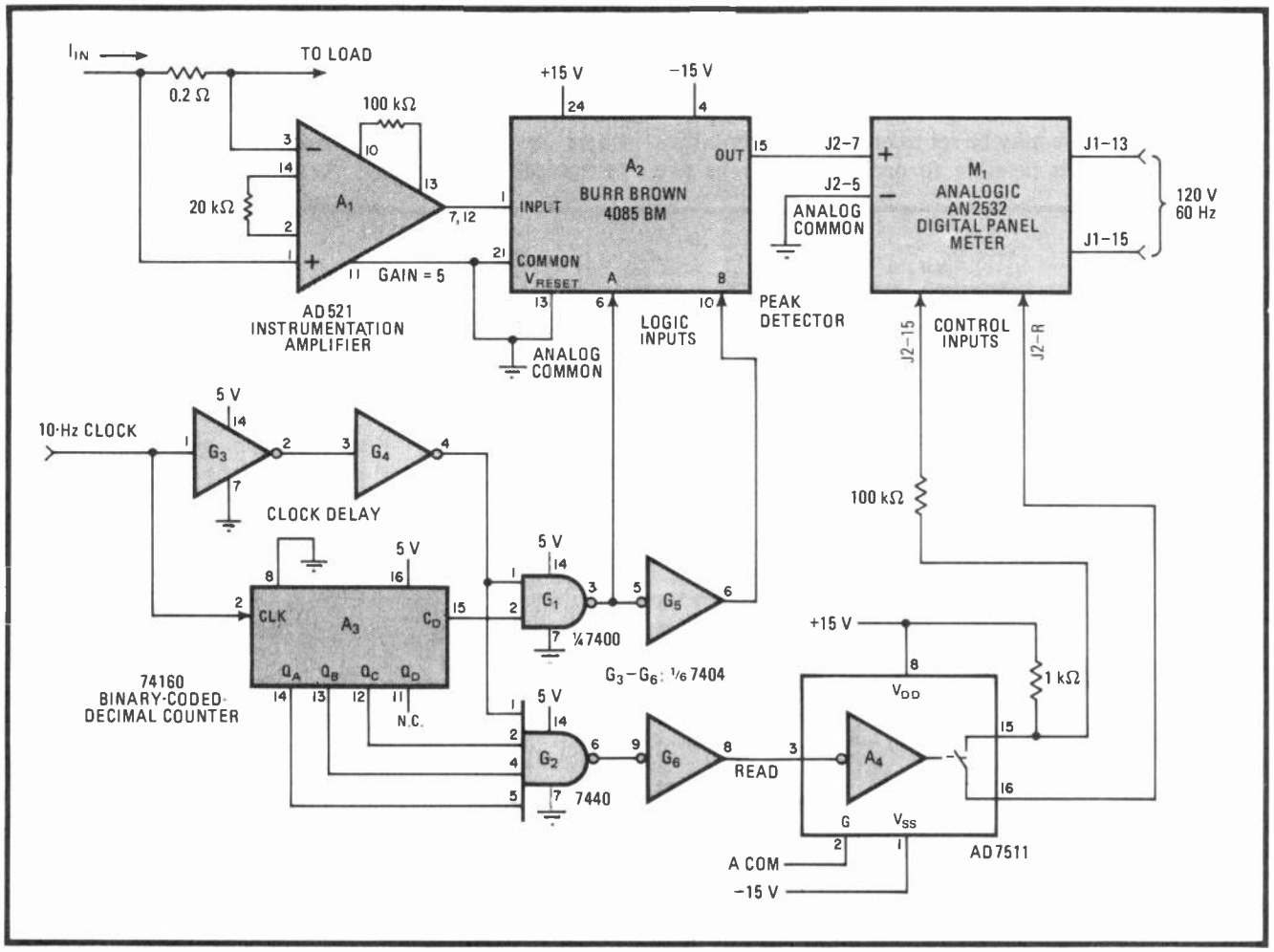
A self-contained sample-and-hold amplifier and a digital panel meter make this device small, rugged, and suitable for measuring peak currents in industrial applications. Although not inexpensive (it can be built for about $65 in small quantities), it is an easy to build, accurate, and reliable peak-reading ammeter.

The 0–10-ampere pulses to be measured are converted to a voltage by instrumentation amplifier A_1, such that the input to peak detector A_2 swings 1 volt for each ampere at the circuit's input. A_2's output voltage then drives digital voltmeter M_1.

The timing pulses for A_2's sampling cycle are derived from a 10-Hz clock signal by gates G_1–G_6 and binary-coded-decimal counter A_3. The decoded clock pulse introduced at gate G_2, along with the delayed clock pulse from G_3 and G_4, form the read pulse for sampling the output of the peak detector for a 50-millisecond interval, and holding that reading for the remainder of the one-second cycle.

During that time, clock inputs A and B reset A_2 to zero. Flutter caused by the 50-ms sampling pulse cannot be detected visually. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.



Rugged and reliable. Ammeter using hybrid sample-and-hold amplifier, digital panel meter, and standard logic components is ideally suited for measuring pulses of peak current in hostile environments. Readout is in peak amperes, accurate to 0.1% over −25° to 85°C.

Current source for I²L saves energy

by Stephen H. Nussbaum
Data/Ware Development Inc., San Diego, Calif.

To capitalize on the low-power advantages of integrated injection logic (I^2L), a power source that also dissipates relatively small amounts of energy is required. This switched-mode supply provides programmable currents of up to 300 milliamperes at 2.3 volts to boards utilizing I^2L loads, with an overhead of only a few milliamperes needed for running the circuit.

The voltage-current characteristics of I^2L devices resemble those of the standard switching diode, whose operation is determined by the amount of driving current available. It is therefore necessary to drive these loads with a current source. Although a single high-value resistor in series with a voltage source would serve to deliver constant current, large amounts of power would be dissipated in the resistor. The difficulty is overcome with this circuit.

Q_1 and its associated components provide a reference current for the complementary-MOS quad analog switch, A_1, in the reference-resistance subcircuit. The R_2C_3 combination helps to stabilize the output against changes in input voltages.

A_1's switches are wired together such that its equivalent series resistance may be set to one of two values by a control signal. It is possible to order as many as five current levels with this switch if additional programming inputs are introduced.

A_1, with the aid of R_3, serves partly as a current-to-voltage converter, so that low-power oscillator A_2 sees the reference current as a representative voltage at its inverting input. This potential will cause Q_2 to switch on periodically. R_4 provides positive feedback for hysteresis, thus controlling the rate at which A_2 and Q_2 are switched—16 kilohertz, in this case. The 10 to 30 millivolts of hysteresis also appears at the output, but this poses no problem with I^2L loads.

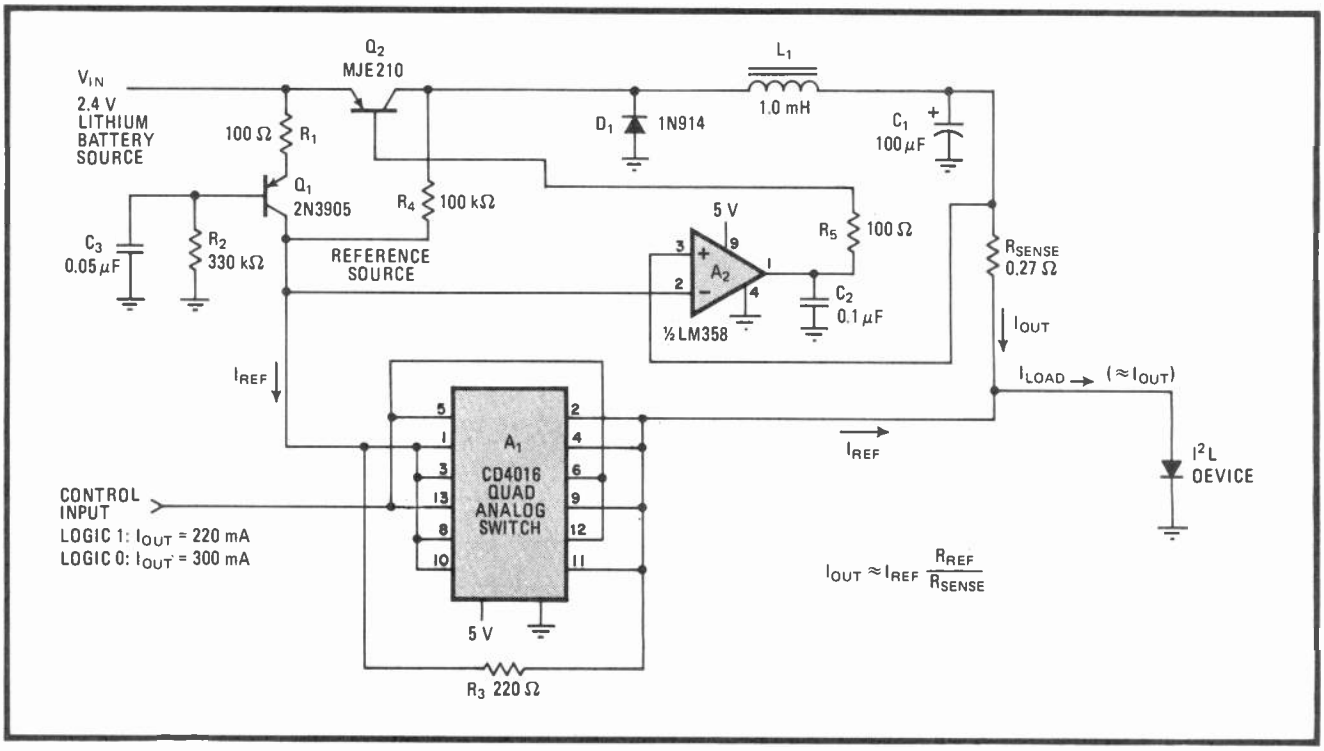
L_1 and C_1 comprise the switcher's required storage elements, acting to release energy to the load through R_{sense} when Q_2 is off. R_{sense} is part of a feedback network used to set I_{out}.

Because the reference current and the output current at summed at the output node, A_2's input sees only the difference of these currents scaled to a voltage by their respective resistors, R_{sense} and R_{ref}. Thus the output current is set solely by the feedback loop. As a consequence of this arrangement, $I_{out} \approx R_{ref} I_{ref} / R_{sense}$. The efficiency of the supply is maximized by using a lower value of R_{sense}, a faster op amp for A_2, and a storage inductor (L_1) with as little dc resistance as possible.

With R_3 = 220 ohms and with I_{ref} = 0.60 mA, I_{out} = 220 mA if a logic 1 is applied to the control input. I_{out} = 300 mA for a logic 0. These values can be changed by suitable selection of I_{ref}, of course, but R_3 may also be varied. Note that:

$$R_{ref} = [(r_{on}/n)R_3]/[(r_{on}/n)+R_3]$$

where n = number of switches and r_{on} = on-state resistance of one switch in A_1, typically 600 Ω. □



Injecting current. Switching source delivers constant current to members of low-power I^2L logic family without wasting much power. Small reference current, C-MOS switches, and low-power oscillator contribute to circuit efficiency. Two-level current source, which generates up to 300 milliamperes at 2.3 volts, can provide one of five current values if additional programming inputs are introduced at switch A_1.

High-speed generator pulses ECL loads

by Andrew M. Hudor Jr.
Department of Physics, University of Arizona, Tucson

Serving the needs of designers and technicians who work with high-speed digital circuits, this inexpensive two-chip pulse generator is invaluable in trouble-shooting emitter-coupled logic. Besides generating signals having frequency and duty cycles that are adjustable to its complementary outputs, the versatile generator also provides two ports at which pulses with a constant 50% duty cycle are available.

One section of a 10116 ECL line receiver, A_1, is used as an RC oscillator[1] whose period is determined by the potentiometer P_1 and the capacitor selected by the frequency-range switch. With the values shown, the oscillator frequency can be varied from a few hundred hertz to more than 50 megahertz. The output of the oscillator is then buffered and squared up by a Schmitt trigger, A_2, which is the second section of the line receiver.

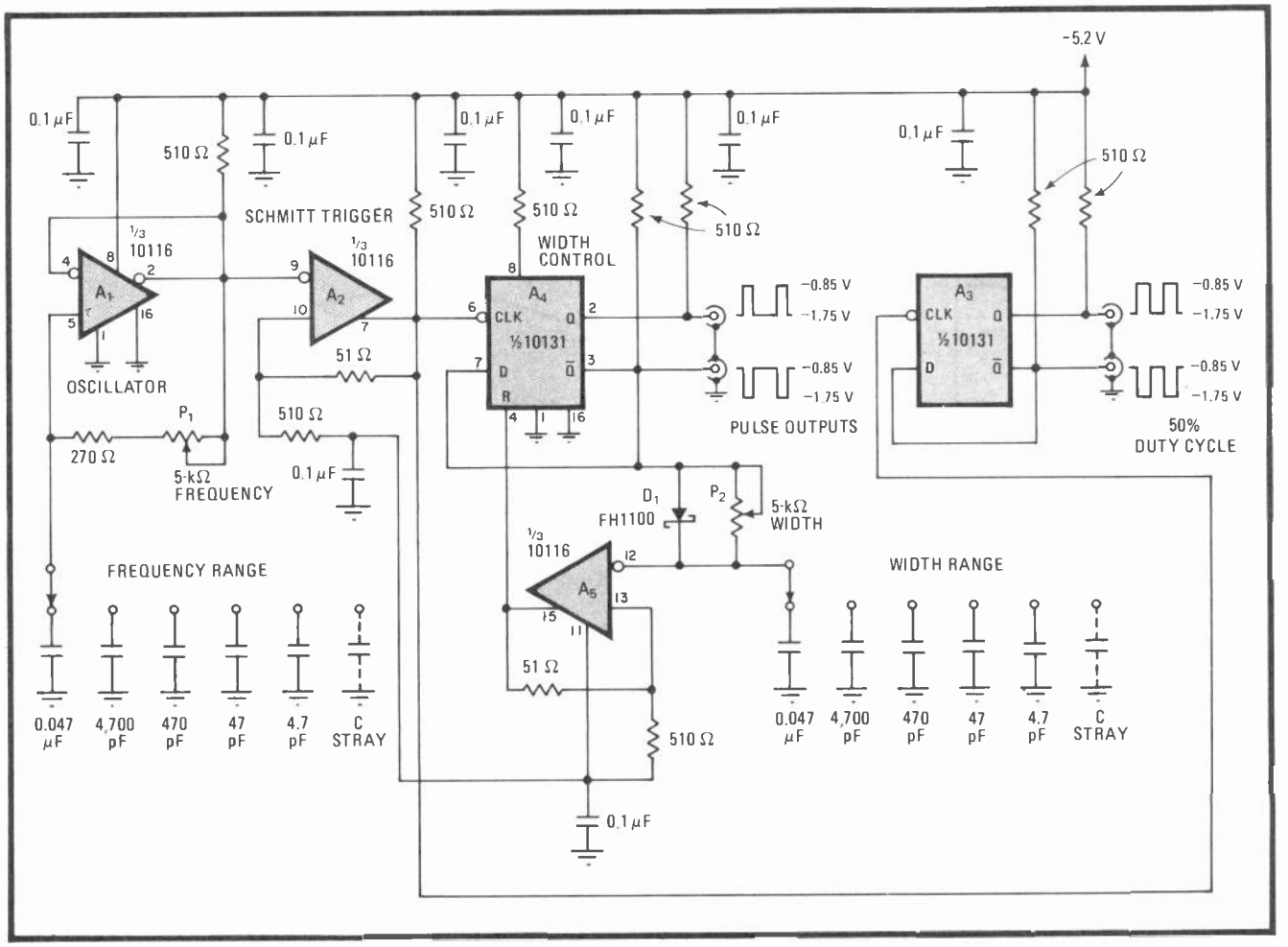
A_2's output toggles both sections of a 10131 dual-D flip-flop, A_3 and A_4. A_3 provides for a 50% duty cycle output, while A_4 and the remaining section of the receiver, A_5, form an adjustable one-shot multivibrator. Here, A_5 serves as a second Schmitt trigger.

The Q output of A_4 is fed to the input of the Schmitt trigger through an RC integrator formed by P_2 and the capacitor selected by the width-range switch. When Q toggles low, the input to the A_5 trigger slowly rises as the capacitor charges. When the trigger level is reached, the Schmitt trigger's output goes high, resetting A_3 and A_4, and the process is repeated.

The time it takes for the integrator to reach the trigger level defines the pulse width. With the values shown, widths from 15 nanoseconds to 10 milliseconds can be selected. Upon resetting of the flip flops, Schottky diode D_1 allows the capacitor to discharge rapidly. The width control allows adjustment of the duty cycle from nearly zero to 50%. For applications where a duty cycle greater than 50% is required, the complementary output should be used.

If desired, a buffer can be easily added at A_3 and/or A_4 in order to drive 50-ohm lines directly. □

References
1. William A. Palm, "ECL IC oscillates from 10 to 50 MHz," *Electronics*, Circuit Designer's Casebook 14D, p. 109.



Speedy. Line receiver and dual flip-flop generate high-frequency pulse trains for emitter-coupled logic. Signals to 50 MHz having widths that are adjustable from 15 ns to 10 ms appear at generator's complementary outputs. Circuit also provides output at duty cycle of 50%.

Dual light-emitting diode synthesizes polychromatic light

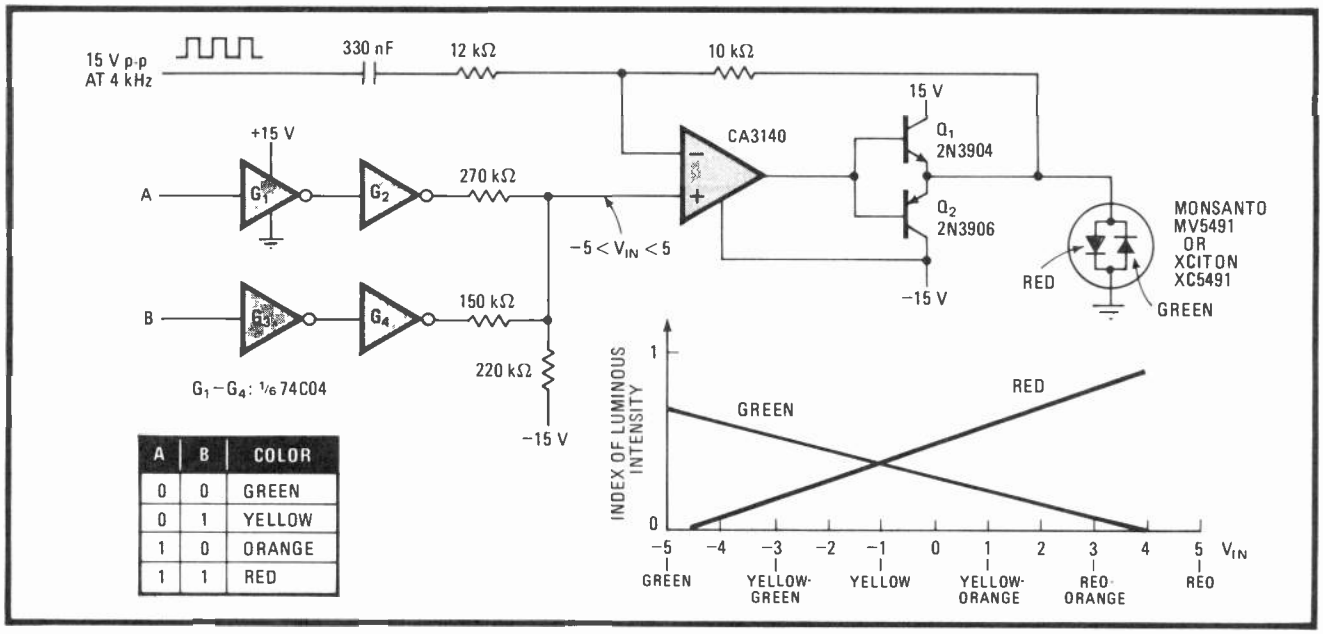
by Leonard M. Smithline
Ithaca, N. Y.

By controlling the drive to each element of a dual red or green light-emitting diode so as to mix the red and green lights in varying quantities, this digital circuit synthesizes four distinct hues from the two primary optical colors. With a slight modification, it can also make the diode vary gradually from green through yellow and orange to red in response to an analog input.

The LED used here may be either the Monsanto MV5491 or the Xciton XC5491 (Fig. 1). The diodes inside either device are wired back to back and so cannot be driven simultaneously. They therefore need a multiplexer circuit to drive them at a fast enough rate for them to appear to be on simultaneously. Here a 4-kilohertz square wave provides the desired chopping action. The relative proportions of drive to the green or red LED are controlled by adding a dc bias to the square-wave drive at the noninverting input of the CA3140 operational amplifier, as shown.

Thus, the states of A and B determine the color perceived by the mixing process, as seen in the table. Alternatively, an analog signal can be applied to the noninverting input of the op amp, whereupon the circuit response will be as shown in the graph.

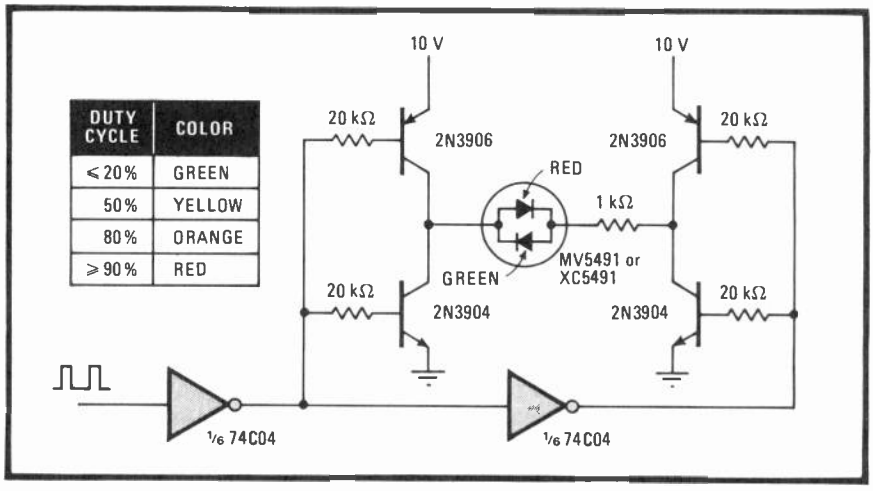
For a thorough mixing of colors, the primary light sources should not only be viewed simultaneously (as



A	B	COLOR
0	0	GREEN
0	1	YELLOW
1	0	ORANGE
1	1	RED

1. Thoughts of hue. Multiplexer's 4-kHz square wave, suitably offset with dc bias controlled by states of A and B, provides desired drive to each element of green/red photodiode for deriving perceived four-color output. Alternatively, analog signal may be applied to noninverting input of op amp for effecting gradual change in color, from green through red. Circuit response in either case is given in table and graph.

2. Color cycle. Generation of yellow and orange from red and green light may also be achieved through control of duty cycle of pulses driving light-emitting diodes. Pulse-width modulation requires only single supply.



DUTY CYCLE	COLOR
≤ 20%	GREEN
50%	YELLOW
80%	ORANGE
≥ 90%	RED

Maximum-length shift register generates white noise

by Henrique Sarmento Malvar
Department of Electrical Engineering, University of Brasilia, Brazil

Using a circuit based on a maximum length sequence generator,[1] this simple unit inexpensively provides a source of white noise over a range of up to 200 kHz. It is far superior to generators that use a reverse-biased base-to-emitter transistor junction, which provides quasi-white noise over a very limited portion of the spectrum. Using two integrated circuits comprising a 25-stage shift register, it can be built for less than $6.

A_1 and A_2 form the n-stage shift register driven by clock G_1–G_2, with A_1 an 18-stage device and A_2 being eight stages in length. A_1 and A_2 are driven simultaneously but out of phase with respect to each other.

The output from stage 7 of A_2 and the last stage of A_1 is applied to G_3 in the feedback loop G_3–G_4, so that a register sequence length of 2^{n-1} clock periods is obtained. Note that G_4 provides signal inversion, so that on power up (the all-zero output state of A_1 and A_2), the noise generator will be self-starting.

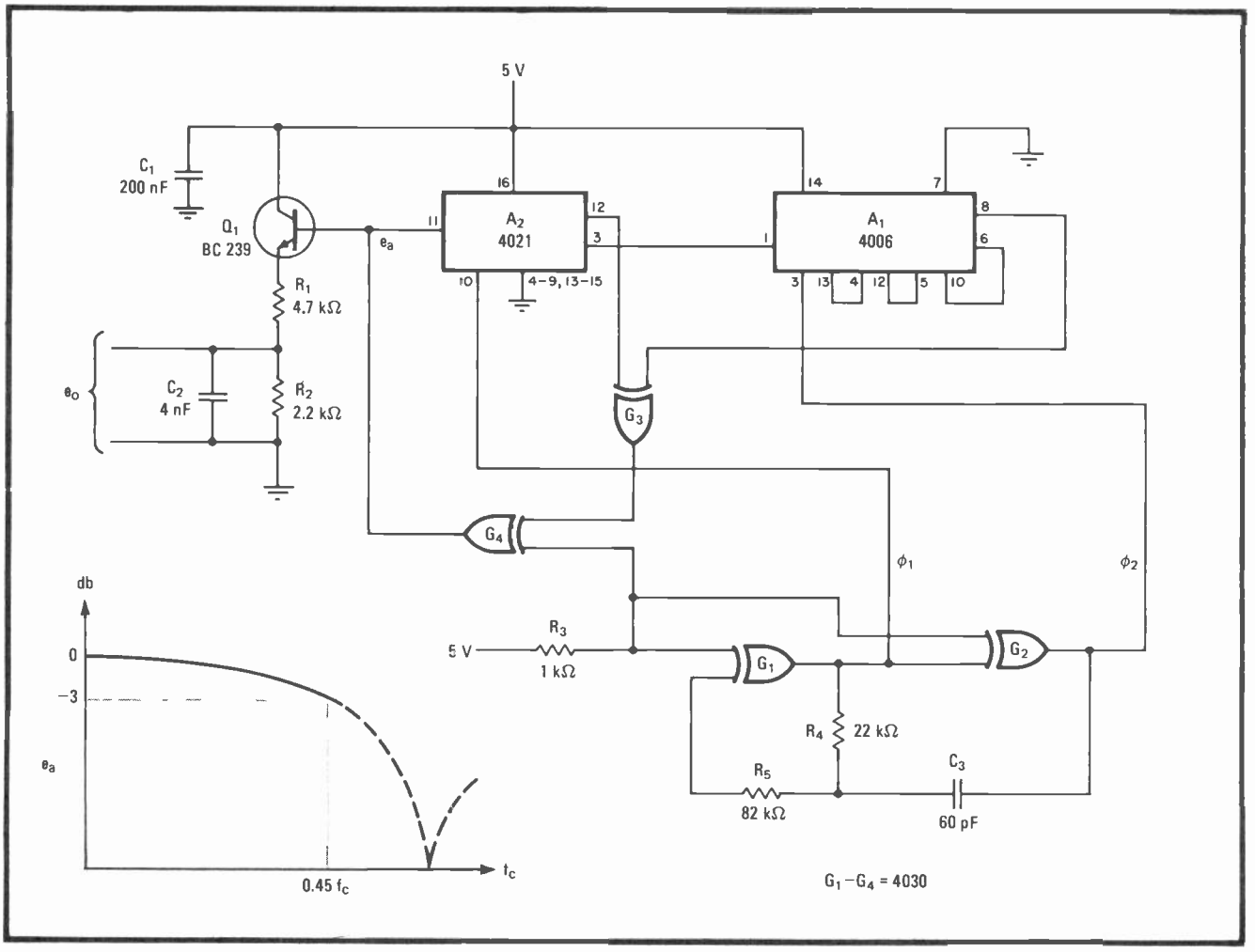
It can be shown that the spectrum of the signal at the output of A_2 will contain several discrete frequencies, separated by $f_c/(2^{n-1})$, where f_c is the clock frequency, in this case 200 kHz. Because n is large, the separations between the discrete frequencies become so close (here, it will be 0.006 Hz with a sequence period of 150 seconds), that the spectrum may be considered continuous. So although the noise is pseudorandom because of the method used to produce it, the difference in the spectral properties of the noise as compared with the ideal is minimal.

As for the amplitude of the output envelope, it will vary with frequency as $(x^{-1} \sin x)^2$, where $x = f/f_c$. Here, the -3-dB point will occur at $f = 0.45\ f_c$, as shown in the curve at the lower left of the figure.

Q_1 serves as a buffer. The network $R_1R_2C_2$ is a low-pass filter that has been added for an application requiring noise to be confined (bandlimited) to the audio frequencies. Its -3 dB point occurs at 25 kHz. □

References
1. I. H. Witten and P. H. C. Madams, "The Chatterbox-2," Wireless World, Jan. 1979, p. 77.

Spectrum spread. 25-stage shift register creates closely spaced signals of discrete frequency for generating pseudorandom white noise over wide range. Spectral response of source (bottom left) is flat from dc to 0.45 f_c, where f_c is the clock frequency.



12-hour clock tells time out loud

by William S. Wagner
Northern Kentucky University, Highland Heights, Kentucky

Combining a program written for the 6800 microprocessor and a four-chip interface, this system expresses clock time as an equivalent sequence of audio tones. Like the audio voltmeter previously described,[1] it allows determination of time when the clock face cannot be seen.

In this method, the exact time—expressed as xxyy, where xx denotes hours and yy denotes minutes—is converted to a series of tones of short duration (dits) to represent quantities extending from 1 to 9. The quantity 0 is represented by a single tone (dah) of a relatively long duration. A long pause separates hours from minutes. Thus, for example, a time of 02:41 would yield an audio output of dah, pause, dit-dit, long pause, dit-dit-dit-dit, pause, dit.

Three frequency dividers (A_1–A_3), two gates (G_1–G_2), and a few passive components comprise the clock-to-microprocessor interface. The actual clock signal is derived from the highly accurate 60-Hz power line.

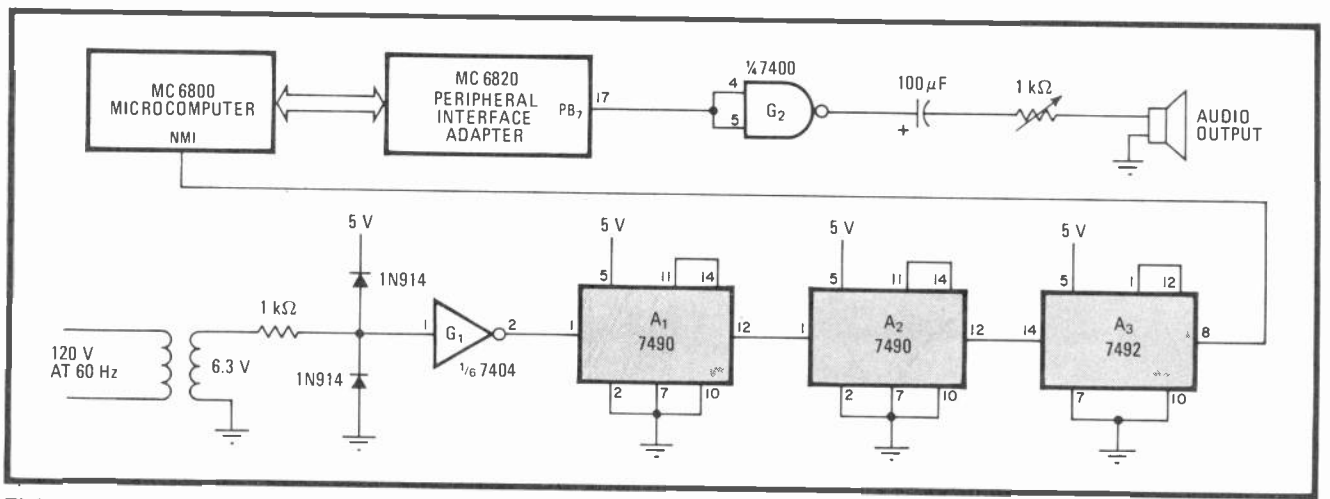
A_1 and A_2, each a divide-by-10 chip, and A_3, wired as a divide-by-12 device, produce a pulse with a 20-second period from the line input. This pulse serves as the 6800's hardware interrupt, which initiates the program and the generation of time markers exactly three times every minute. Other intervals can be selected by appropriate action of the divider ratio.

The clock is set to any desired starting time with software, where the initial hour is stored at program address 0002, minutes are stored in 0001, and seconds in 0000. Although seconds are not made audible, they are required in the program for updating the minutes unit once every three sampling periods.

When an interrupt is received, the initial time, expressed in hours and minutes, is converted to a set of four 4-bit binary-coded words in steps 0023–00A0 and is checked to determine if each word represents a 0 or an integer from 1 to 9. At this point the program determines whether short or long tones are to be transmitted. The instructions commencing at 0053 set the time interval between the processing of each individual word and between hours and minutes.

After the clock routine (01A0–01D6) increments the minutes and hours units as necessary, the dit and dah subroutines (at 0100 and 0120, respectively) are initiated. The program then halts and waits for a system interrupt, whereupon the process repeats. □

References
1. William S. Wagner, "Digital voltmeter has audible output," *Electronics*, March 29, 1979, p. 120.



Tick tones. Microprocessor-based chronometer periodically derives audible time markers. System generates a pulse code, with numbers 1 to 9 represented by string of short tones and a zero represented by a long tone. Long pause between digits separates hours from minutes.

6800 PROGRAM FOR AUDIO CLOCK

Address	Mnemonic	Address	Mnemonic	Address	Mnemonic
0000	(STORAGE)	0073	PULA	0134	ASLA
0001	"	0074	ASLA	0135	ASLA
0002	"	0075	PSHA	0136	ASLA
0003	LDX FF04	0076	BCS 17	0137	ASLA
0006	STX 8802	0078	BRA 1A	0138	PSHA
0009	WAI	007A	LDA 08	0139	JMP 0053
000A	BRA FD	007C	JSR 0100	0140	LDX 03FF
0020	STX 0015	007F	BRA E8	0143	ORAB 7F
0023	LDS 00C0	0081	LDA 04	0145	STAB 8002
0026	PSHA	0083	JSR 0100	0148	LDAA 25
0027	ANDA 70	0086	BRA E6	014A	DECA
0029	BGT 03	0088	LDA 02	014B	BNE FD
002B	JMP 0120	008A	JSR 0100	014D	DEX
002E	PULA	008D	BRA E4	014E	BEQ 03
002F	ASLA	008F	LDA 01	0150	COMB
0030	ASLA	0091	JSR 0100	0151	BRA F0
0031	PSHA	0094	LDAA 02	0153	PULA
0032	BCS 0C	0096	LDX FFFF	0154	ASLA
0034	PULA	0099	DEX	0155	ASLA
0035	ASLA	009A	BNE FD	0156	ASLA
0036	PSHA	009C	DECA	0157	ASLA
0037	BCS 0E	009D	BNE F7	0158	PSHA
0039	PULA	009F	PULA	0159	JMP 0094
003A	ASLA	00A0	LDS 10	01A0	LDX 0000
003B	PSHA	00A2	LDX 15	01A3	LDAB 03
003C	BCS 10	00A4	RTS	01A5	SEC
003E	BRA 13	00A5	JMP 0140	01A6	BSR 0E
0040	LDA 04	00FD	JMP 01A0	01A8	LDAB 60
0042	JSR 0100	0100	PSHA	01AA	BSR 0A
0045	BRA ED	0101	LDX 00FF	01AC	LDAB 13
0047	LDA 02	0104	ORAB 7F	01AE	BSR 06
0049	JSR 0100	0106	STA 8002	01B0	BSR 15
004C	BRA EB	0109	LDAA 25	01B2	BSR 13
004E	LDA 01	010B	DECA	01B4	DEX
0050	JSR 0100	010C	BNE FD	01B5	RTI
0053	LDAA 01	010E	DEX	01B6	LDAA 00,X
0055	LDX FFFF	010F	BEQ 03	01B8	ADCA 00
0058	DEX	0111	COMB	01BA	DAA
0059	BNE FD	0112	BRA F0	01BB	CBA
005B	DECA	0114	LDX 1FFF	01BC	BCS 01
005C	BNE F7	0117	DEX	01BE	CLRA
005E	PULA	0118	BNE FD	01BF	STAA 00,X
005F	PSHA	011A	PULA	01C1	INX
0060	ANDA F0	011B	DECA	01C2	TPA
0062	BEQ 41	011C	BNE E2	01C3	EORA 01
0064	PULA	011E	RTS	01C5	TAP
0065	ASLA	0120	LDX 03FF	01C6	RTS
0066	PSHA	0123	ORAB 7F	01C7	DEX
0067	BCS 11	0125	STAB 8002	01C8	STS 10
0069	PULA	0128	LDAA 25	01CA	LDAA 02
006A	ASLA	012A	DECA	01CC	BEQ 05
006B	PSHA	012B	BNE FD	01CE	LDAA 00,X
006C	BCS 13	012D	DEX	01D0	JMP 0020
006E	PULA	012E	BEQ 03	01D3	INC 0002
006F	ASLA	0130	COMB	01D6	BRA F6
0070	PSHA	0131	BRA F0		
0071	BCS 15	0133	PULA		

Cupless anemometer has diode wind-sensor

by J. P. Scoseria
Montevideo, Uruguay

Working well as a differential thermometer, this simple circuit can also be used to find wind speed by detecting the difference in junction voltage between two forward-biased diodes. Here, one junction is heated to a fixed temperature, and the other's temperature-dependent junction potential is made to vary with the cooling effect of the wind. Being totally solid-state, the unit eliminates all mechanical difficulties. The unit can also function as a psychrometer, or humidity indicator, if the heated junction is wetted down instead.

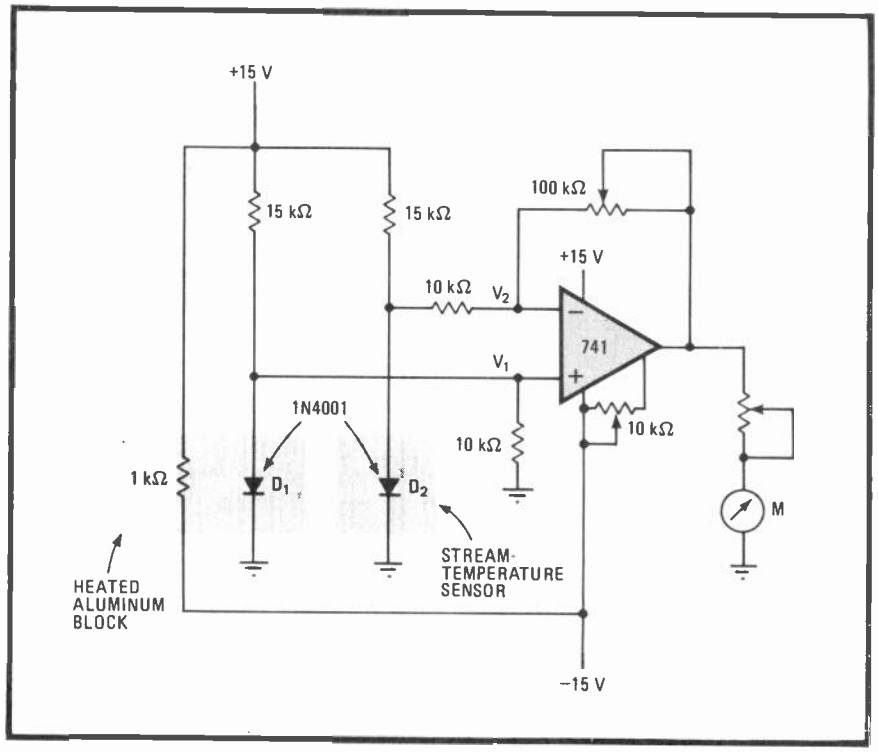
Diode D_1 and a resistor are situated within the confines of a small one-of-a-kind aluminum enclosure built for this circuit. D_1 is heated by the power dissipated by the resistor. The enclosure maintains a constant temperature throughout, independent of environmental changes, as in an oven. Although the absolute temperature reached by the diode junction is of little importance in this circuit, it will be a direct function of the power supplied to the block, the area of the block available for heat transfer, and its heat transfer coefficient.

The same general considerations exist for the stream-temperature sensor, D_2, which is placed in a similar aluminum block to reduce temperature variations due to changes in wind speed (settling time ≈ 2 minutes). Here, however, the power supplied to the block is small, being about 1 milliwatt to activate D_2, and heat variations reach the junction from the outside.

Generally, the output from the 741 op amp is $e_o = K(V_1 - V_2)$, where K is a constant and V_1 and V_2 are functions of the temperature associated respectively with the heated block sensor and the wind speed. The voltages across both D_1 and D_2 drop by 2.5 millivolt for each degree Celsius rise, and so $V_{d1} \approx 0.7 - 2.5(10^{-3})T_f$, and $V_{d2} \approx 0.7 - 2.5(10^{-3})T_w$, where temperature T_f corresponds to V_1 and T_w to V_2. As a result, $e_o = K(-2.5)(10^{-3})(T_f - T_w)$, and so the output of the op amp will be proportional to the temperature difference. The current that flows through ammeter M will thus vary linearly with temperature.

The relation between the wind's cooling factor and temperature is nonlinear, however, and because the initial zero-wind current in meter M is a function of the block temperature (and thus block size), and because the sensor temperature, and D_1 and D_2 are not driven from true constant-current sources, the calibration will not be uniform for any two units.

Although it would be ideal to have access to a wind tunnel for calibration, good results can be obtained with the aid of an automobile. Placing the sensor on the auto's antenna, with the meter set at maximum for zero wind speed, the unit can be calibrated satisfactorily on a windless day by noting M's output as a function of the car's speed. □



Ceaseless wind. Temperature difference between heat oven surrounding diode junction D_1 and stream sensor D_2, whose junction temperature varies with wind speed, is reflected as a change in current at M. Unit can be satisfactorily calibrated with auto's speedometer on a calm day.

Solar-powered regulator charges batteries efficiently

by G. J. Millard
Volcanological Observatory, Rabaul, Papua New Guinea

For use with solar panels, this simple and efficient regulator circuit provides an energy-saving solution to charging batteries of the lead-acid type commonly found in automobiles. Not considering the cost of the solar cells, assumed to be at hand for use in other projects, the regulator alone is under $10.

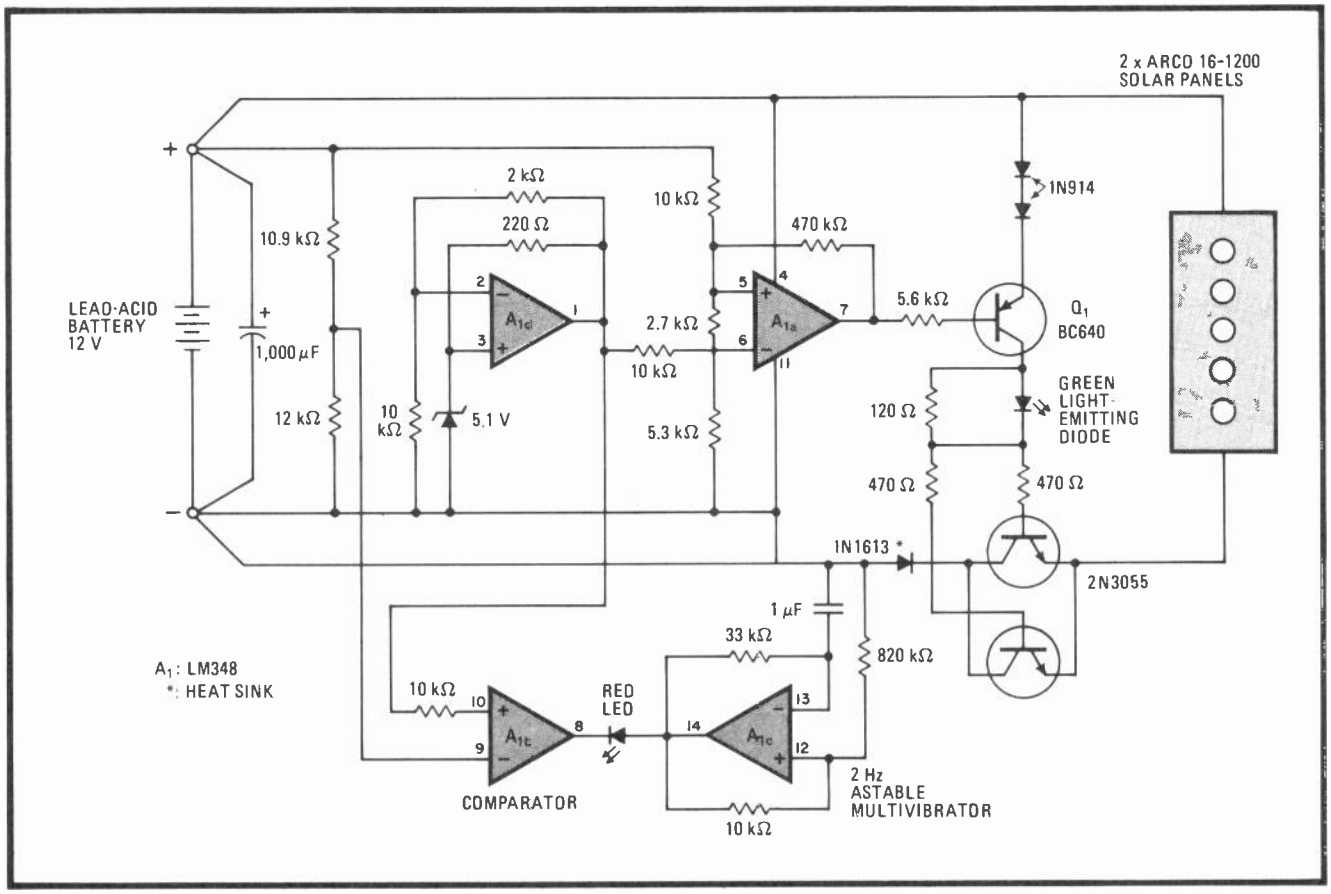
Unlike many other shunt regulators that divert current into a resistor when the battery is fully charged, this circuit opens the charging path so that the resistors can be eliminated. This method is extremely advantageous when solar panels are used, for large resistors would otherwise be required to dissipate the high power levels typically encountered.

When the battery voltage, e_o, is below 13.5 volts (normally the open-circuit potential of a 12-V battery), transistors Q_1, Q_2, and Q_3 turn on and charging current flows from the solar panels as required. The active green light-emitting diode indicates the battery is taking charge.

As e_o approaches the open-circuit voltage, op amp A_{1a} switches Q_1–Q_3 off. This condition is maintained until such time as the battery voltage drops to 13.2 V, whereupon the charge cycle repeats.

If the battery voltage should continue to fall from 13.2 to approximately 11.4 V, indicating a flat battery, A_{1b} switches low, causing a red LED to flash at a rate determined by the astable multivibrator A_{1c}, in this case oscillating at a frequency of 2 hertz. A_{1d} provides a reference of 6 V to maintain the switching points at the 11.4- and the 13.2-V levels.

The circuit will handle currents to 3 amperes. To draw larger currents, it is necessary to increase the base currents of Q_2 and Q_3 so that these transistors will remain in saturation during the charging periods. □



Light charge. Regulator for handling currents produced by solar panels charges lead-acid batteries without wasting excessive power. Circuit cuts off current to battery when its open-circuit voltage is greater than 13.5 V, eliminating need for dissipating power in resistors. Green LED indicates battery is charging. Flashing red LED indicates battery is flat (battery voltage below 11.4 V) and refuses to take charge.

Tunable equalizers set amplitude and delay

by P. V. Ananda Mohan
Indian Telephone Industries Ltd., Bangalore, India

Equalizing networks providing constant amplitude and/or delay over a wide range of frequencies are easily realized by utilizing the feed-forward and feed-back techniques of these tunable circuits. More specifically, a parallel-T arrangement of resistors and capacitors as shown in (a) makes it possible to select the equalizing delay with a single potentiometer. Equalization and selection of amplitude can be attained by adding a single operational amplifier stage of variable gain (b) to the basic circuit. If the parallel-T is made tunable (c), the equalizer's center frequency can be adjusted with very little difficulty.

The circuit that is illustrated in (a) is so configured that its transfer function is that of an all-pass network having a roll-off dependent on circuit Q, or:

$$\frac{e_{out}}{e_{in}} = \frac{s^2 - s(\omega_o/Q) + \omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

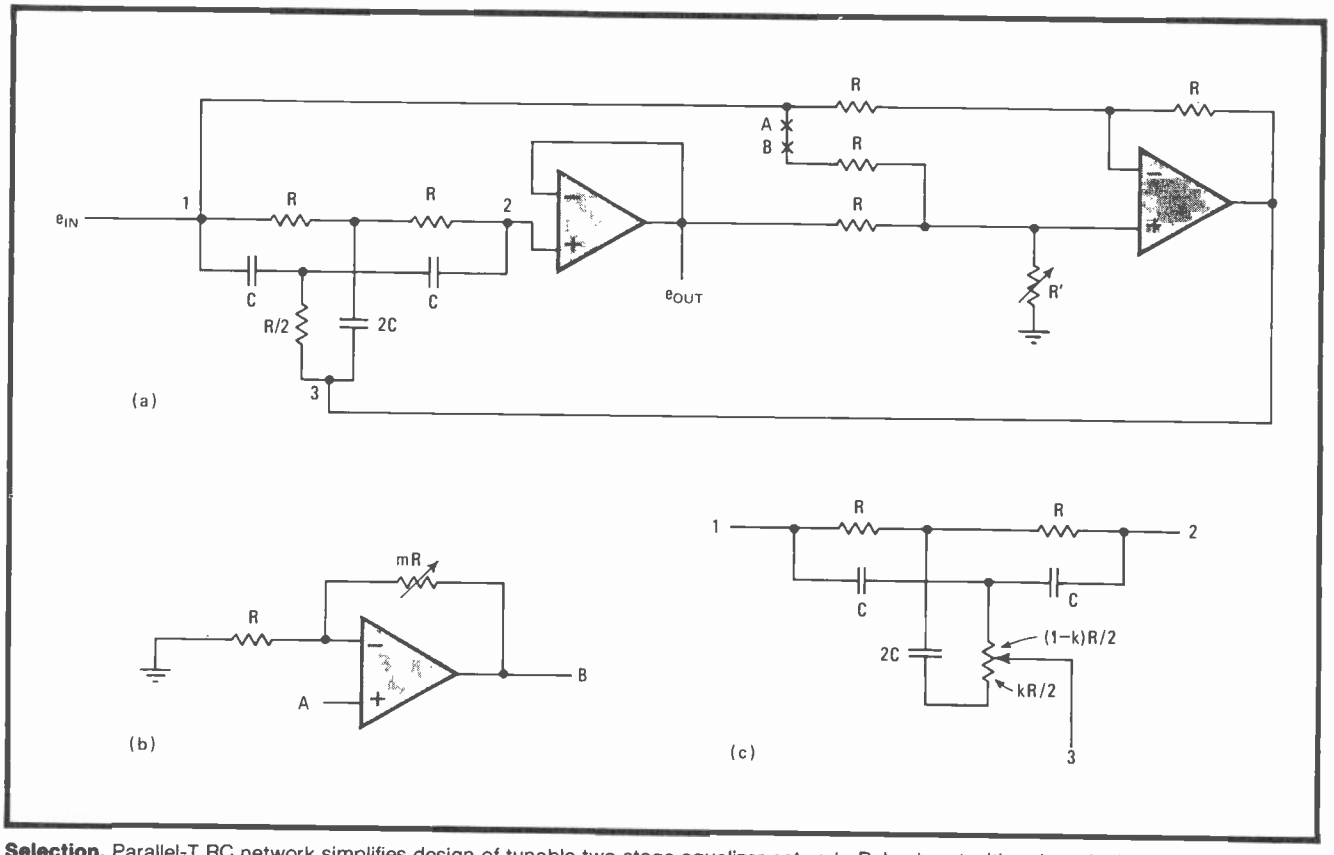
where $\omega_o = 1/RC$ and $Q = 1/4 + R'/2R$. The amount of delay is selected with potentiometer R′, as the amount of phase shift introduced by the RC network is:

$$\theta = t - 2\tan^{-1}[\omega\omega_o/Q(\omega_o^2 - \omega^2)]$$

where θ will vary little about ω_o, provided ω is sufficiently removed from ω_o.

If the op amp circuit (b) is placed between ports A and B in (a), the equalizer's gain at mid-frequency ω_o becomes $G = (2R'm)/R - 1$, and so the gain may be set by varying R′ and/or m. Note that the delay is still a function of R′ and that G will not vary significantly over a wide range of frequencies.

The center frequency of the equalizer may be adjusted if the parallel-T network shown in (c) replaces the network in (a) enclosed between points 1 and 3. In this case, $\omega_n = \omega_o/(1 - K^2)^{1/2}$ and $Q = (1/4 + R/2R)/(1 - K^2)^{1/2}$, where K is the fraction of the total resistance of P_2, as measured from its lower end. □



Selection. Parallel-T RC network simplifies design of tunable two-stage equalizer network. Delay is set with only a single control element, R′ (a). Amplitude equalization or adjustment in network's center frequency is attained by adding op amp (b) and tunable RC (c), respectively.

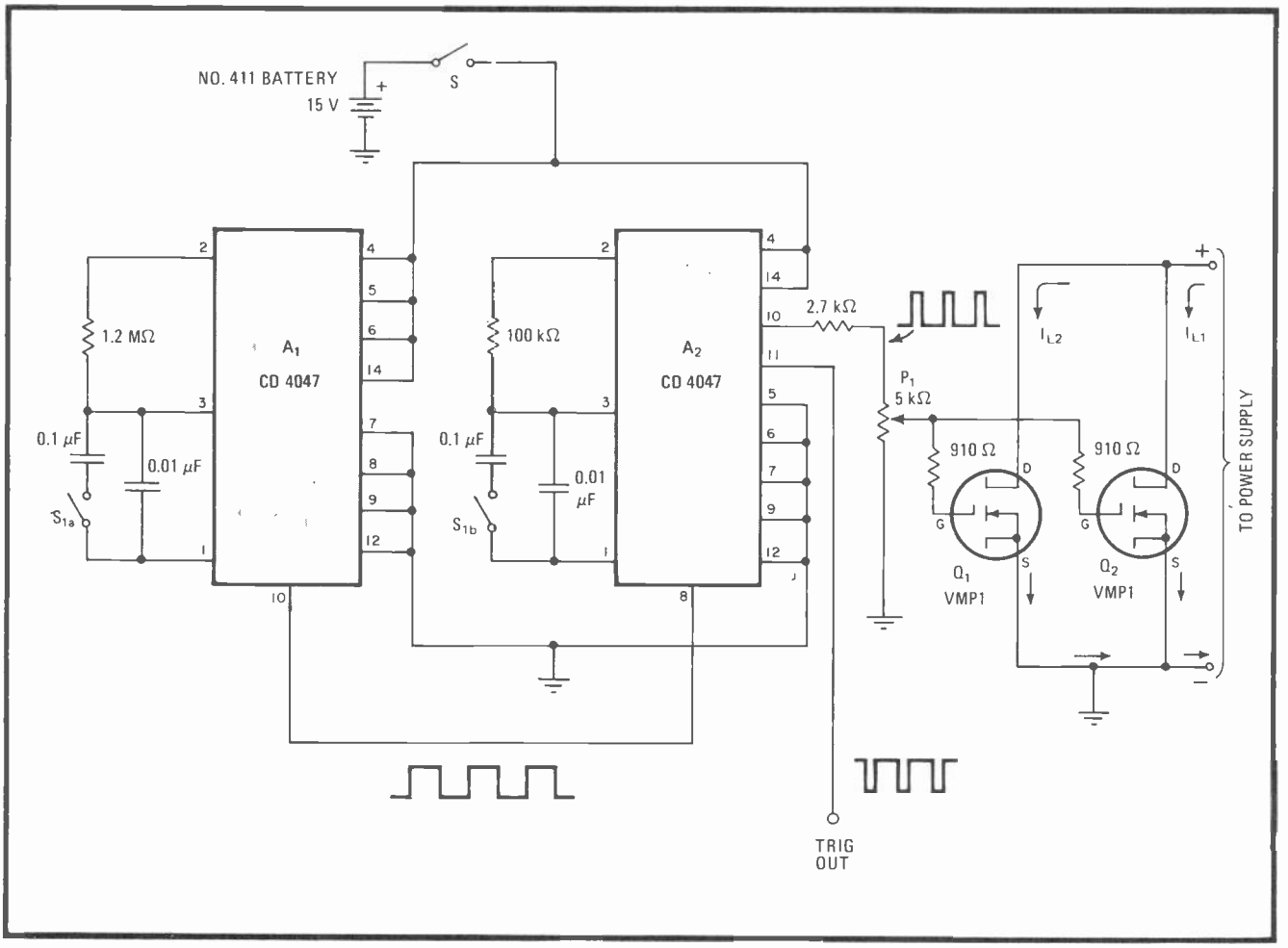
Switched load checks power supply response

by William M. Polivka
Department of Engineering, California Institute of Technology, Pasadena

The transient response of a power supply is easily checked with the aid of this pulse loader, which periodically places a short circuit across the supply's output in order to simulate sudden load changes. Using complementary-MOS integrated circuits and V-groove MOS power transistors, the compact, self-contained unit runs on a battery, so that it presents no ground-loop problems to the supply under test.

As shown in the circuit for the pulsed load, astable multivibrator A_1 and one-shot A_2 set respectively the frequency and the width of the pulses that switch on load transistors Q_1 and Q_2. S_1 selects either of two combinations of frequency and width—in this case, 2 hertz at 25 milliseconds or 20 Hz at 2.5 ms. Note that a low duty cycle is required to reduce heat dissipation in Q_1 and Q_2. A trigger signal for driving an oscilloscope or other instrument to observe the supply's response appears at pin 11 of A_2.

Potentiometer P_1 sets the point at which Q_1 and Q_2 fire, so that the magnitude of the pulsed supply current passing through the load transistors can be selected from zero to the maximum capability of the V-MOS devices. Each field-effect transistor handles 2 amperes at 12 volts, values that derate to 400 milliamperes at 60 V. Moreover, an increase in supply loading may be attained simply by adding transistors in shunt at the output of the unit, as required. □



Load dynamics. Low-cost tester, with aid of scope, finds transient response of power supply by ordering periodic increase in supply current to simulate load changes. A_1 and A_2 set frequency and width of switching waveform. $Q_1 - Q_2$ sink current proportional to setting of P_1.

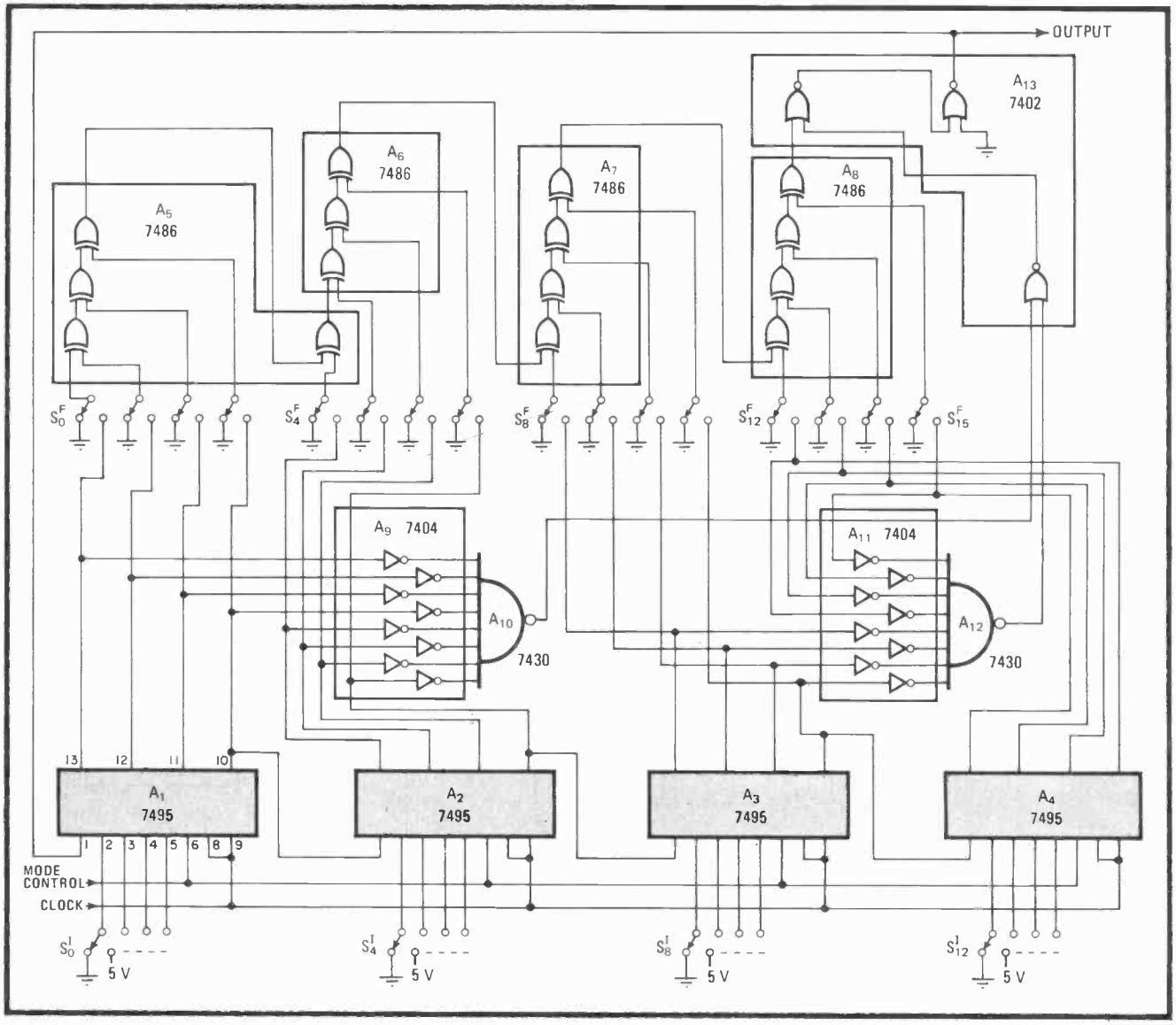
Pseudorandom generator has programmable sequence length

by Ajit Pal
Indian Statistical Institute, Calcutta, India

Providing a pseudorandom binary sequence of order i in the range of 2 to 16, this generator will find many uses in fault-detection and speech-scrambling equipment. Any sequence having a maximum length of $2^{16}-1$ can be generated. If the sequence can be selected electronically, instead of mechanically by means of a manual-switching arrangement as shown, the unit will be extremely useful in automatic-test environments.

The pseudo-random sequence is produced with the aid of a 16-bit shift register and appropriate circuitry for providing a feedback signal to the register's first stage. A_1–A_4 are the 4-bit registers that comprise the 16-bit stage, wired to shift bits from left to right on every system clock. A_5–A_7, connected at the register's outputs, and A_8 are exclusive-OR gates used to generate the feedback signal, which is determined by switches S_i^F. The switch positions are set in accordance with the primitive polynomial of the binary sequence to be generated. Note that the settings of the switches in the figure correspond to a sequence of length $2^{15}-1$, or an equivalent primitive polynomial of $x^{15}+x+1$.

A_9–A_{13} detect the all-zero condition of A_1–A_4 and ensure that the register will not be locked in that state on power-up or during normal operation. The mode control input otherwise allows A_1–A_4 to be set at any point in the sequence as determined by the S_i^I switches. □



Selection. Switches S_i^F and A_5–A_8 derive suitable feedback signal so that shift register A_1–A_4 can generate a pseudorandom binary sequence of selectable length. A_9–A_{13} detect register's all-zero state and prevent register lock-up by generating logic 1 bit to A_1–A_4 input during power-initialization period. Switches S_i^I initialize registers at any point in a sequence that may extend to $2^{16}-1$ bits.

Reducing the dropout voltage of programmable regulators

by Carlo Venditti
The Charles Stark Draper Laboratory Inc., Cambridge, Mass.

A programmable regulator's dropout voltage—the minimum allowable potential between its input (V_{in}) and output (V_{out})—can be improved by adding an external output stage and negative feedback. The resulting regulated output voltage (E_{out}) not only approaches V_{in} more closely, but the the current-drive capability is also better, thanks to the outboard power-transistor stage.

The design technique used to achieve this improved performance is described here for Fairchild's popular μA78MG regulator, which has a nominal dropout voltage of 3.0 volts. As shown in the figure, a change in V_{in} causes V_{out} to increase temporarily. The corresponding increase at E_{out} that is applied to the control input of the μA78 forces V_{out} lower, toward the value it had initially. If the resistor network R_1 to R_3 is optimized, E_{out} can be brought to within 1.5 V of V_{in}.

Consider the case where the output voltage E_{out} is to be kept at 12.5 V $\pm$50 mV for a V_{in} ranging from 14 to 15.5 V. When V_{in} is at 14, V_{out} cannot be above 11, owing to the dropout voltage of the regulator. Thus with an output voltage of 12.5, the voltage at the base of Q_1 is 13.1 (0.6 V higher).

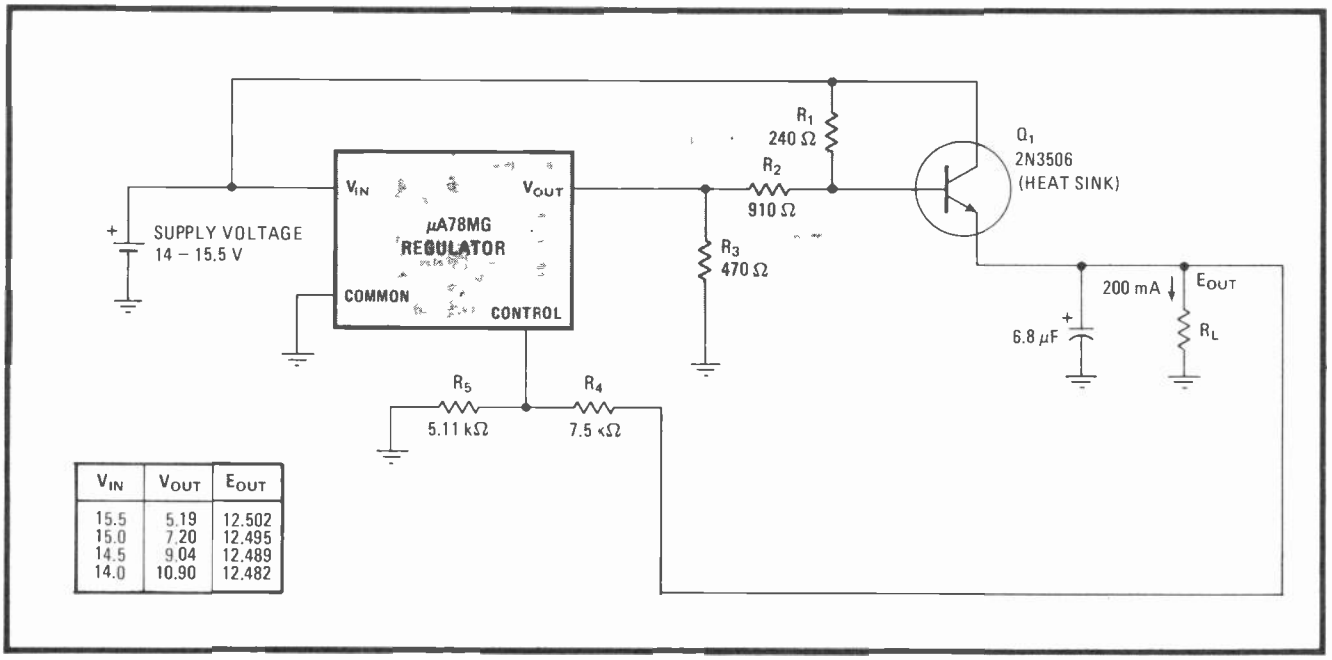
Now R_1 can be selected to pass a given value of transistor base current, I_b, of say, 1.2 milliamperes, and a current through R_2 of perhaps twice this value (2.4 mA), plus a small amount to account for variations in I_b. Thus $R_1 = (14-13.1)V/3.75\ mA = 240\ \Omega$, and $R_2 = (13.1-11)V/2.4\ mA = 910\ \Omega$.

The next condition to be addressed is the case where V_{in} assumes a value of 15.5 V, so that R_3 may be determined. Because V_{out} ultimately decreases with an increase in V_{in}, V_{out} should be made to move to its minimum value so that the maximum dynamic range of the circuit is realized. From the data sheet of the μA78, $V_{out(min)} = 5.0$ V. Note that changes in V_{out} are scaled by the R_2/R_1 ratio, and these resistors ensure that a change of 910/240 = 3.8 V occurs for every 1-V increase in V_{in}.

Thus the current through R_2 at this time will be $(13.1-5.0)/910 = 8.8$ mA, and assuming the minimum (quiescent) current of the regulator is 2 mA, the current through R_3 is $(8.8+2.0) = 10.8$ mA. Therefore $R_3 = 5/10.8 = 470\ \Omega$. The table summarizes the actual dynamic performance of the regulator. Note the apparent dropout voltage of the regulator has been reduced to $14.0-12.482 \approx 1.5$ V when V_{in} is at its minimum.

The junction temperature of the on-chip power transistor is $T_j = \theta_{JA}P_T + T_A$, where θ_{JA} is the junction to ambient thermal resistance (80 Ω, see data sheets) and T_A is the ambient temperature. Thus, assuming T_A = 25°C, T_j = 35°C, well below the 125°C thermal shutdown temperature of the μA78.

A check on the chip's temperature will confirm that the regulator's thermal shutdown point has not been reached. The temperature reaches a maximum when V_{in} = 14.0. At this voltage, the regulator's output current is



V_{IN}	V_{OUT}	E_{OUT}
15.5	5.19	12.502
15.0	7.20	12.495
14.5	9.04	12.489
14.0	10.90	12.482

Closer. Outboard power transistor stage, and resistor pad R_1–R_3 set E_{out} to within a few volts of V_{in}, so that $(E_{out}-V_{in})$ is below μA78's dropout value. Q_1 also provides increased current capacity. Table summarizes dynamic range attained for example using technique discussed in text.

20.8 mA, and the output power is 20.8 (14 − 11) = 62.5 mW. The quiescent current is 4 mA (see data sheets), and the quiescent power drain becomes 4(14 V) = 56 mW. As a consequence of these figures, the total output becomes P_T = 118 mW. □

Doubling the character rate handled by CRT controllers

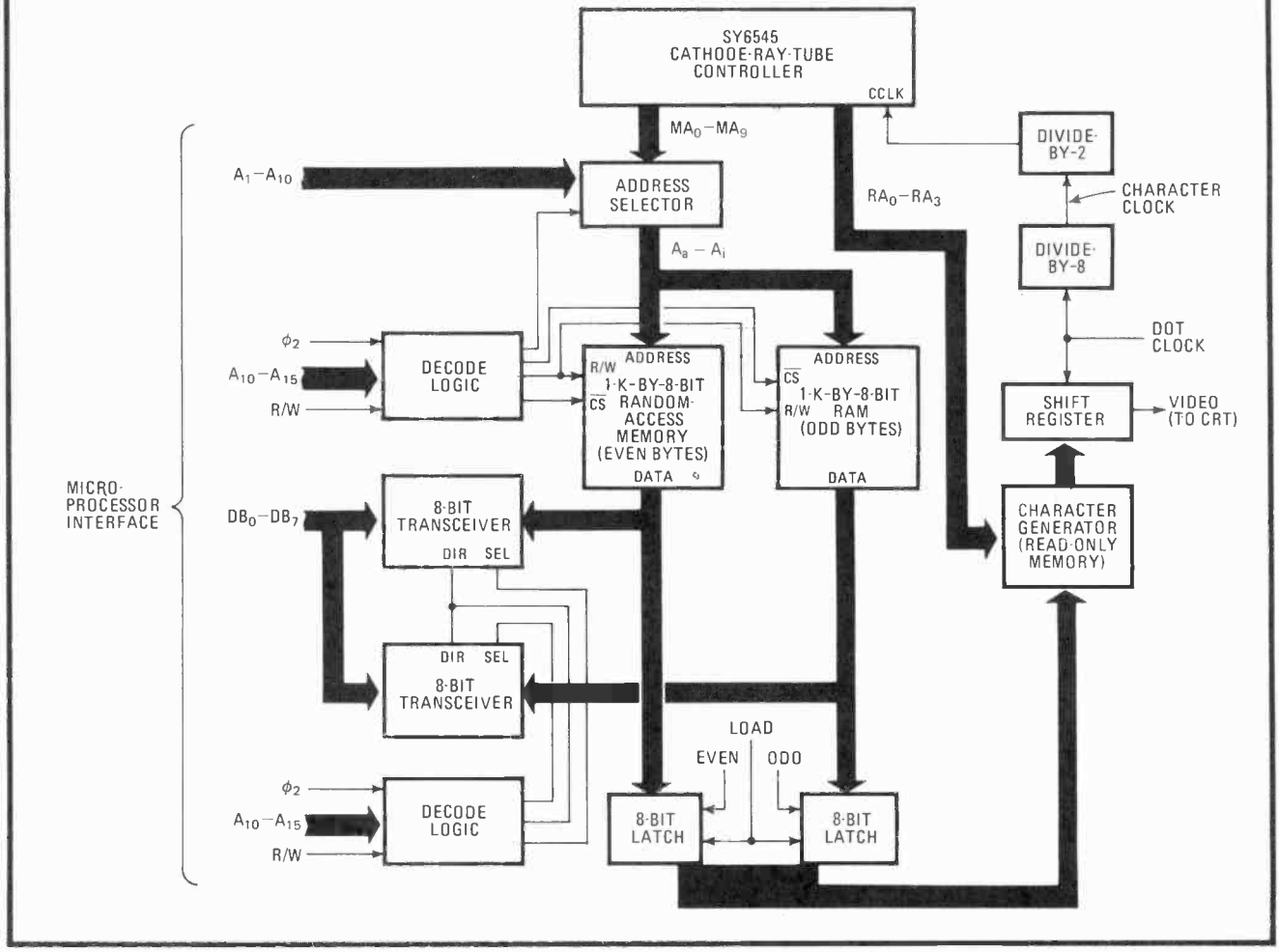
by Conrad J. Boisvert
Synertek Inc., Santa Clara, Calif.

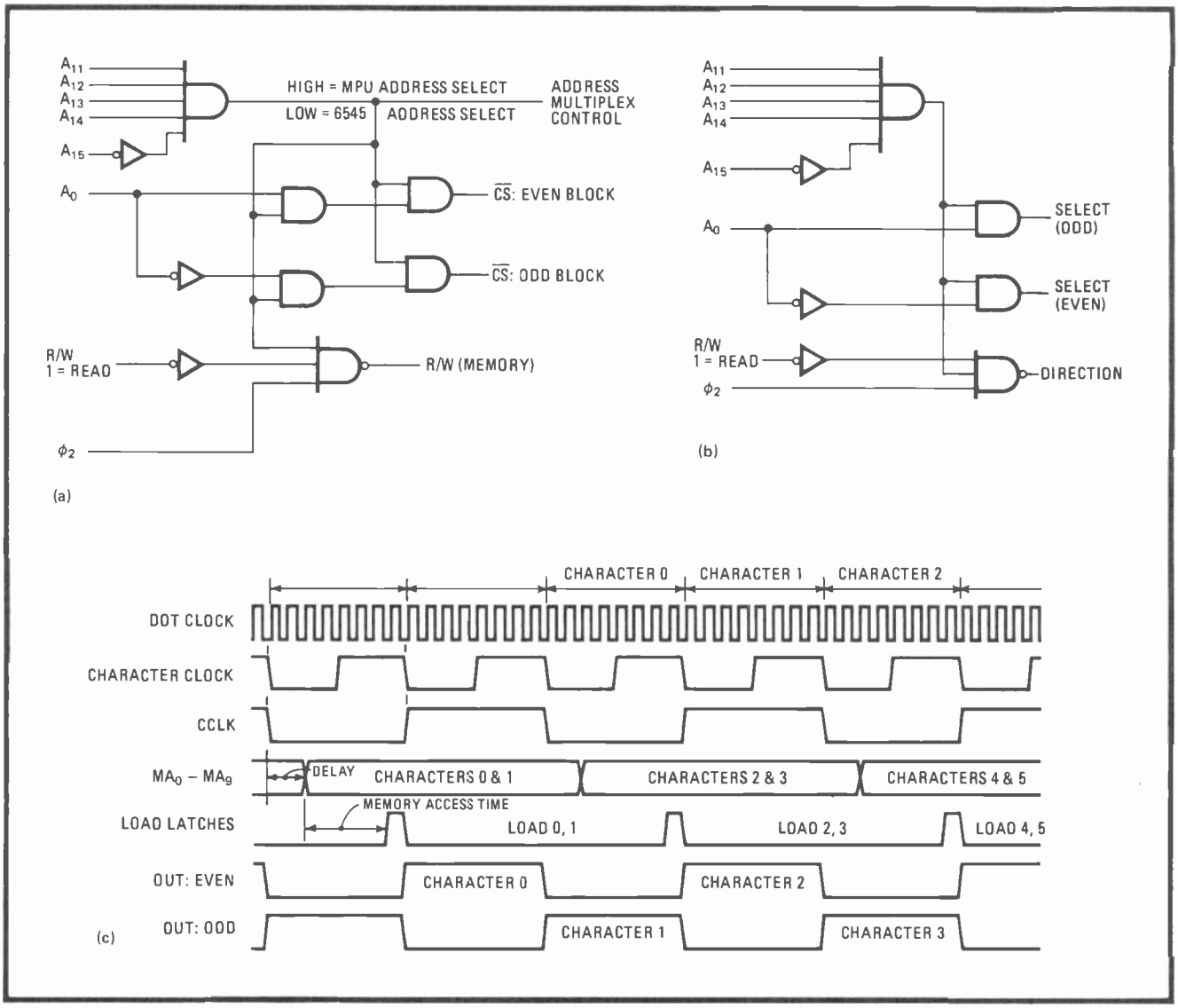
Controllers that transfer display information from a microprocessor to a cathode-ray tube can be made to operate at effective character rates in excess of the normal maximum value. Specifically, by accessing 2 bytes of data per fetch and implementing logic to apply the characters to the display one at a time, the effective character rate can be doubled. The technique is applied here to the Synertek SY6545 chip, although the principle can be extended to most of the popular controllers.

The system architecture necessary for doubling the effective character rate is shown in the block diagram. The memory scheme gives the microprocessor overriding priority in selecting the video-display memory. Other configurations could be implemented, but this is the simplest and focuses attention on the more significant aspects of the method. Also note that the video-display memory is assumed to be 8 bits wide (ASCII coding requires only 7 bits) and that 8 horizontal bits define one character.

A key circuit point is that the SY6545 address lines, MA_0–MA_9, are routed through the address selector block to memory addresses A_a–A_i of both the odd and even memory blocks. In this way, as the SY6545 steps through its states, the two memories are accessed simultaneously. Memory addresses A_1–A_{10}, on the other hand, are routed through A_a–A_i, with the memory address line, A_0, selecting either the even or odd memory, but not

BLOCK DIAGRAM OF CRT CONTROLLER SYSTEM





Hardware. Logic for increasing character rate handled by CRT controllers uses readily available gates. Circuitry for memory control (a) and data transceivers (b) adapts system for two-character fetch and display. Timing diagram (c) details system operation.

both. Thus, a dual-port memory is configured, accessing the data memory as a 1-K-by-16-bit block, and the microprocessor as a 2-K-by-8-bit block.

The logic required to control the memory is shown in Fig. 2a. The chip-select lines $\overline{CS}$ must always be low if the microprocessor is not addressing memory. A_{11}–A_{15} correspond to the decoded memory-map location of the addressed memory, with A_0 used to select either the odd or the even block. Under these conditions, the address selector (Fig. 1) is activated. The R/W signal may then be applied to the memories.

Similar logic for controlling the data-bus transceivers is shown in Fig. 2b. Here, the transceiver's odd or even select outputs are energized after inputs A_{11}–A_{15} have settled. The transceivers are deactivated and the microprocessor data bus isolated from the video display if A_{11}–A_{15} do not match the decode pattern.

The timing diagram clarifies the system operation (Fig. 2c). Note the character clock, which normally drives the SY6545's CCLK pin directly, is divided by 2 because two characters must be fetched per cycle.

The horizontal registers associated with the character total, the display, the sync position, and the sync width will be affected by the aforementioned modification, and steps must be taken to alter the way in which they are programmed. In any case, the value programmed must be half the value that is normally entered. For example, to achieve a display of 80 horizontal characters per line, the number 40 must be programmed into the horizontal display register.

Finally, external logic must be incorporated into the system to achieve a cursor output signal that will be active for each character handled. This function may be implemented with three NAND gates.

The SY6545's cursor output is first combined at one NAND gate with the even latch-select signal of Fig. 2b and the negated output of the PA0 port signal of the SY6520 peripheral interface (not shown). PA0, the cursor signal, and the odd latch-select signal are combined at the other NAND gate. Both gate outputs are joined at the input of the third (two-input) NAND, whose output represents the modified cursor signal. □

Low-cost fiber-optic link handles 20-megabit/s data rates

by A. Podell and J. Sanfilippo
Loral Electronic Systems, Yonkers, N. Y.

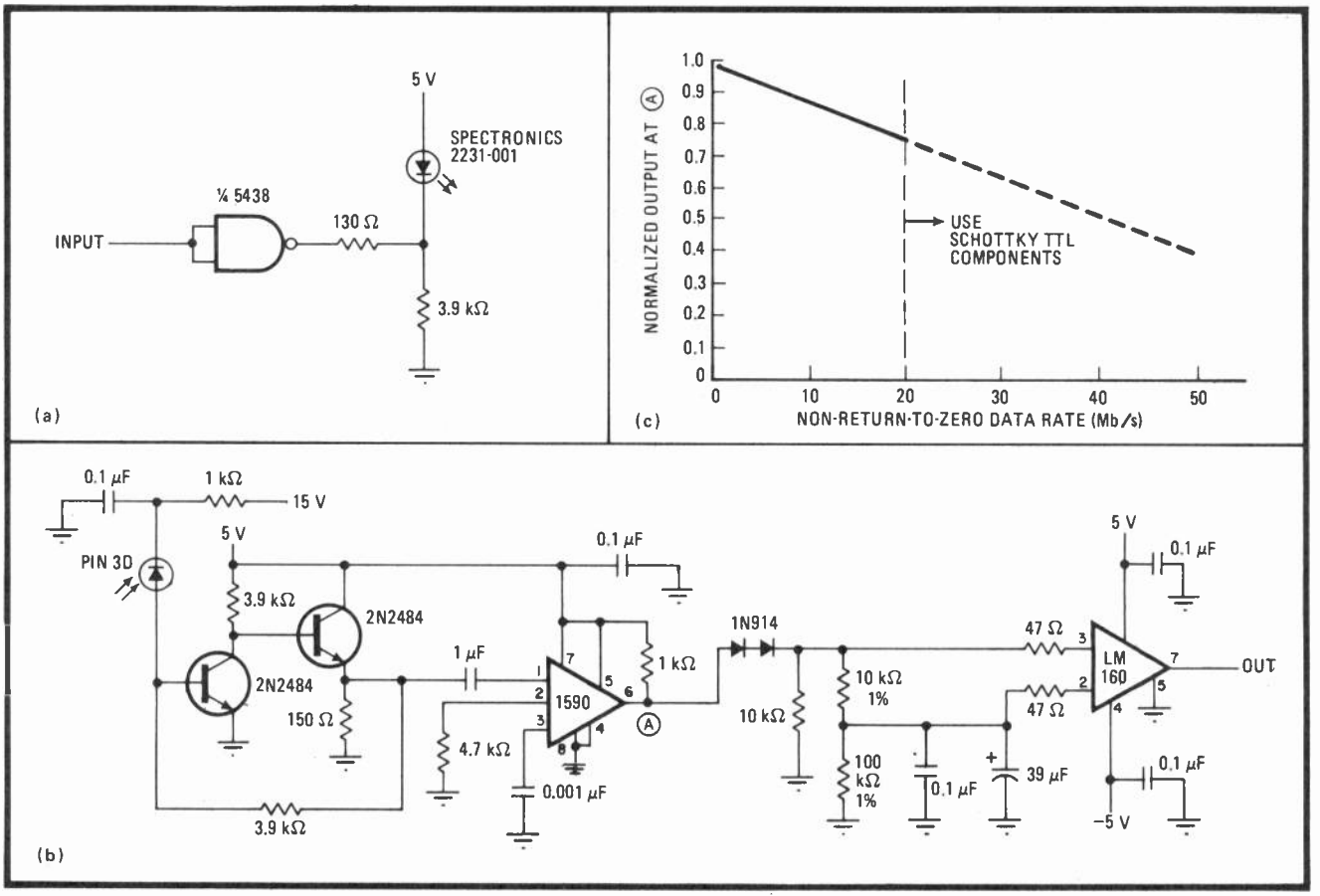
Providing an inexpensive link for the transmission and detection of digital signals over short distances, this fiber-optic system handles data rates in excess of 20 megabits per second. The system, which can be built for about $90, including cable, processes all types of data—a continuous-wave clock waveform, a burst of N clock cycles, handshaking signals, or a non-return-to-zero (NRZ) stream.

A TTL driver and a light-emitting diode serve well as the transmitter, shown in (a). The 5438 TTL driver is a two-input, open-collector NAND gate selected for its low power dissipation and 48-milliampere current-sinking capability. The LED is a gallium-arsenide device operating at 910 nanometers and provides 2 milliwatts of optical power at a forward current of 100 milliamperes. The 130-ohm resistor sets the current through the LED at about 30 mA, and so the output power is about 0.6 mW in this circuit.

The receiver (b) is also simple and sensitive. The output from the p-i-n photodiode (labeled the PIN 3D device) is several microamperes. This current is converted into a voltage by a two-transistor transimpedance amplifier. The 2N2484 transistors selected give low input capacitance, an adequate gain-bandwidth product, and the ability to detect small currents. Amplifier output is about 25 millivolts.

The MC1590 video amplifier that follows greatly boosts signal levels over a wide band (c). Two 1N914 diodes drop the output offset voltage of the single-ended amplifier, nominally at 4 volts, to within the input range of the LM160 comparater. The comparator's threshold is set by a simple voltage divider. The capacitors, across pin 2 and ground, combined with the 100-kilohm resistor, form a low-pass filter providing a threshold that varies with the comparator's supply voltage.

As for the electro-optical interface, the LED, which is contained in a TO-46 package, is easily mounted in an inexpensive window bushing made by AMP, model 530563-1. The PIN 3D photodiode can be mounted in



Light bits. Simple data transmitter (a) and a receiver (b) form the nucleus of a fiber-optic transmission system that is capable of handling all types of digital waveforms. Link operates over a wide band of frequencies (c). Cost of the 10-meter-long unit, including cable, is under $90.

the same type of connector if desired. The need for delicate mounting adjustments is avoided here by using a fiber bundle of sufficient diameter, in this case 45 mils. Galite 2000 cable is satisfactory, and Valtec, Rank Industries, and others produce similar bundles.

The Galite cable has 210 fiber elements having an attenuation of 450 decibels per kilometer at 910 nm and a bandwidth-distance product of 15 megahertz/km. For a 10-meter-long link, therefore, the cable loss will be 4.5 dB and the bandwidth will be 1 gigahertz. With the measured loss of 1.5 dB in the LED-to-cable interface and a cable/detector interface loss of 3.9 dB, the total loss amounts to 10 dB. Thus, the 0.6-mW output of the LED is reduced to 0.06 mW at the receiver.

Transmitter layout is not critical in a one-way link. Duplex operation will require electrical isolation between transmitter and receiver components. There are several precautions to take in constructing the receiver. Notably, the lead from the anode of the detector diode to the transimpedance amp must be kept as short as possible. The output of the receiver should be isolated from all previous stages to prevent unwanted pickup. A ground plane is not a necessity, but is recommended for processing data rates greater than 10 megabits/s.

The link's signal-to-noise ratio is slightly less than 40 dB, implying a bit-error rate above 10^{-8}. The system is operational over a temperature range of $-40°C$ to $100°C$, and a supply variation of 4.5 V to 5.5 V. □

Line-frequency converter transforms 50 Hz into 60 Hz

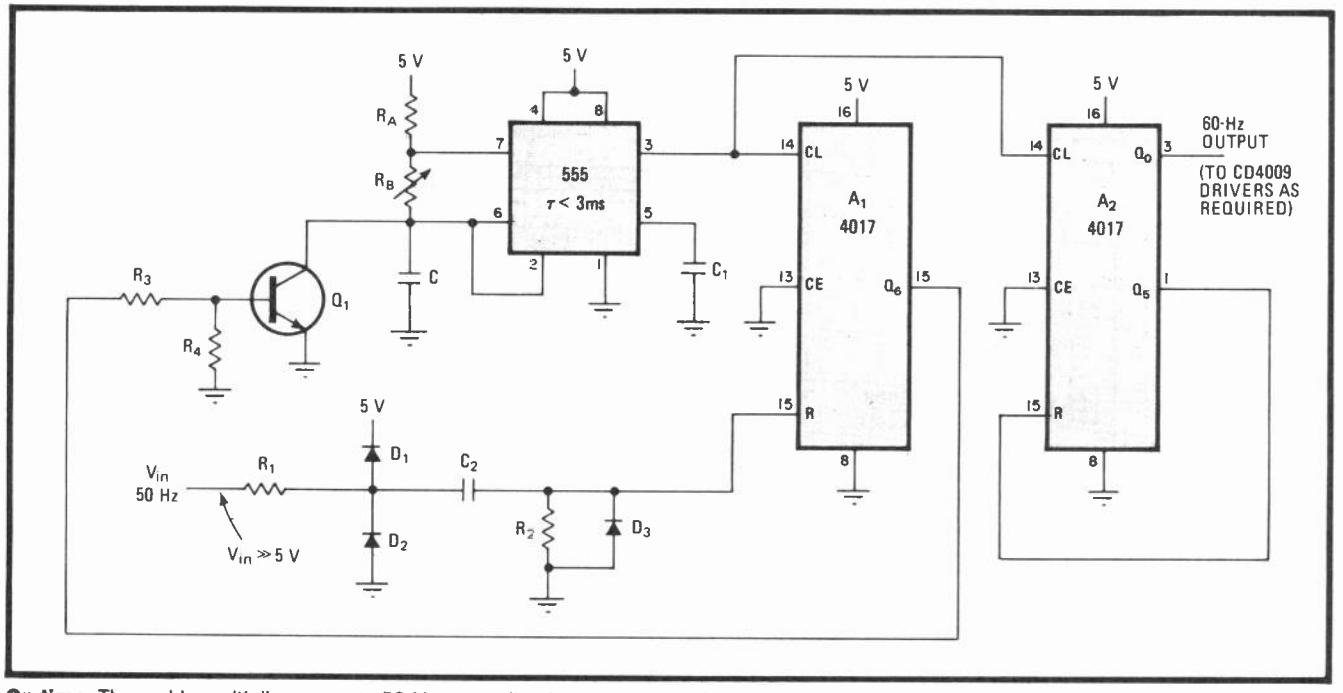
by Juan E. Piquinela
Montevideo, Uruguay

Low-power equipment driven from the 60-hertz power line can usually be expected also to work properly at 50 Hz—that is, except for electric clocks and other time-keeping devices, to which many a traveler outside North America will attest. For such devices, a circuit that provides a multiplication ratio of 6:5 for generating a 60-Hz output from a 50-Hz input is required. Such a low-cost, low-power circuit is shown here.

The 555 timer, operating as an astable multivibrator at 300 Hz, provides the 4017 counter, A_1, with six count-pulses for every reset pulse from the 50-Hz line. The timer's period of oscillation—about 3 milliseconds—is not critical as long as six of its cycles are completed in less than 20 ms, the period of the 50-Hz line frequency.

On the sixth pulse, Q_6 of A_1 moves high and disables the timer through transistor Q_1 by shorting capacitor C. Thus, independent of the period set for the 555, its average frequency is $50 \times 6 = 300$ Hz. At the positive zero-crossing of the line voltage that occurs shortly after the sixth pulse, A_1 is reset through $R_1 - R_2$, C_2, and $D_1 - D_2$, and the process repeats.

Counter A_2 provides a divide-by-five function at 300 Hz, thereby generating an output frequency of 60 Hz. C-MOS drivers or transistors can provide increased current capability as required. □



On time. Three-chip multiplier converts 50-Hz power-line frequency into 60 Hz for devices used in the U. S. A_1 generates six pulses for every 50-Hz cycle, forcing 555 timer to generate average frequency of 300 Hz. A_2 provides divide-by-five function on 555 waveform.

Electronic security lock has nonvolatile latch memory

by Ray Oakley
Plessey Semiconductors, Irvine, Calif.

Nonvolatile quad latches serve as the memory bank in this electronic security lock, which can be programmed with any one of more than 65,000 possible four-digit combinations. The number of combinations that can be selected for opening the lock can be greatly increased, simply by cascading the latches and their corresponding control circuitry.

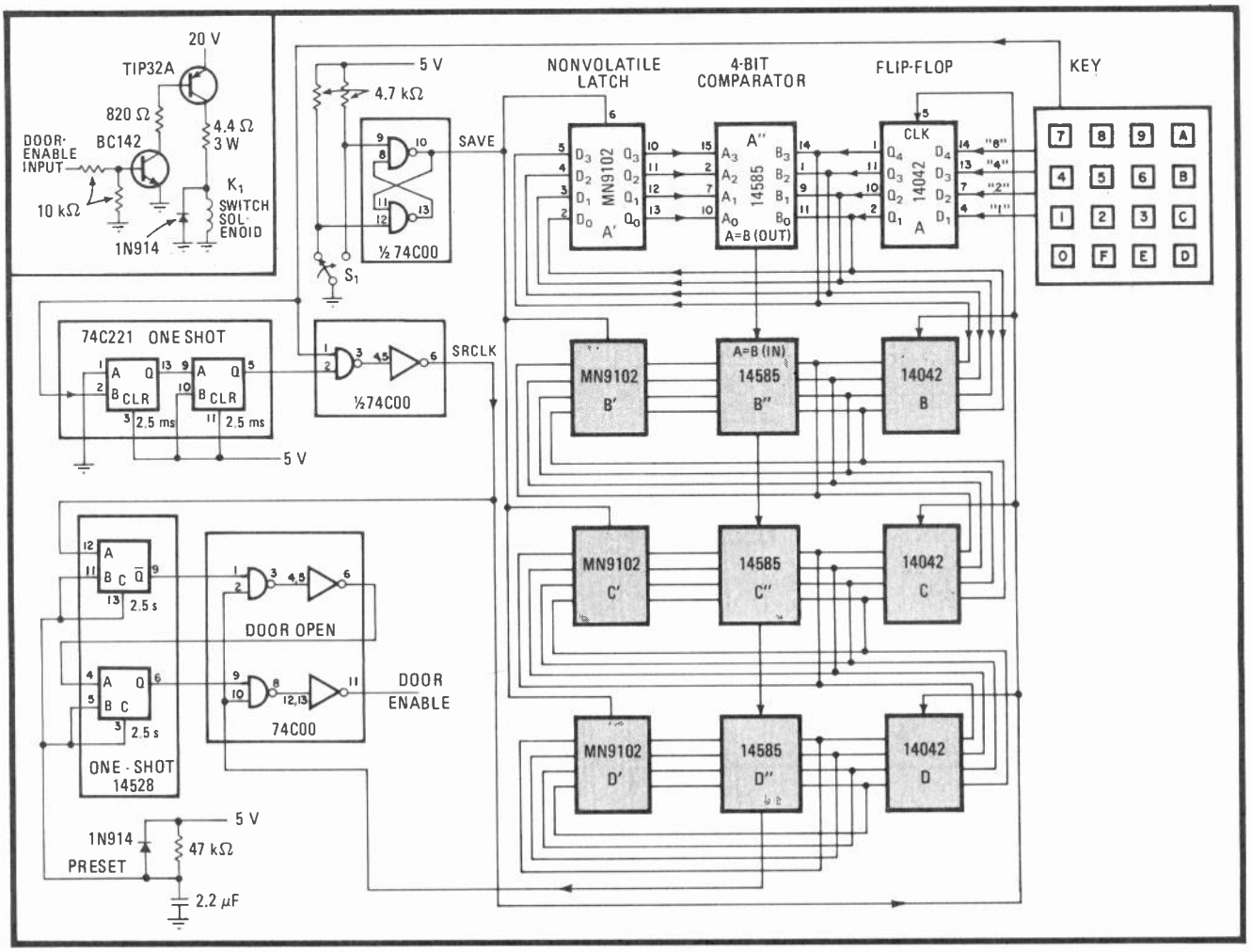
The desired four-digit combination is stored in the Plessey MN9102 latches by first entering the number via the keyboard, which provides a hexadecimal output. If the code were 3579, digit 3 would first be introduced to the D input of flip-flop A. At the same time, the signal KEY, which indicates contact closure, is generated. KEY produces clock signal SRCLK, generated by a monostable multivibrator, which prevents keyboard bounce and which clocks 3 into A.

Because the outputs of each flip-flop, n, are connected to the D inputs of the next flip-flop in the line, n + 1, the successive introduction of the remaining digits translates the digit 3 from A to flip-flop D, with the end result that 5 will be in flip-flop C, 7 in B, and 9 in A at the conclusion of the sequence. The outputs of A to D are also connected to latches A′ to D′, respectively, and so by activating switch S_1 momentarily in order to generate the $\overline{\text{SAVE}}$ signal, the digits can be stored in their corresponding latches.

Data can be retained in the latches for at least one year in the absence of applied power (+5, −12 volts). Typically, 10 million save operations can be made before device performance is affected.

In actual operation, the first digit keyed in is compared with the 9 stored in A′, at comparator A″. Assuming the first digit keyed is a 3, there will be no output from the A = B port of the comparator. Neither will there be any output from B″ or C″ as the digits 5 and 7 are entered.

As the final digit, 9, is entered, however, digit 3 is placed in D, 5 moves to C, and 7 is stored in B. All comparators therefore indicate A = B, and a door enable signal is generated, thereby activating K_1 after a user-selected delay provided by the 14528 one-shot. □



Hardened. Four-digit combination is kept in security lock's latch memory. Data will be retained in low-cost latches for at least one year in the absence of applied power. Matching input code entered via keyboard energizes relay K_1 after user-specified delay.

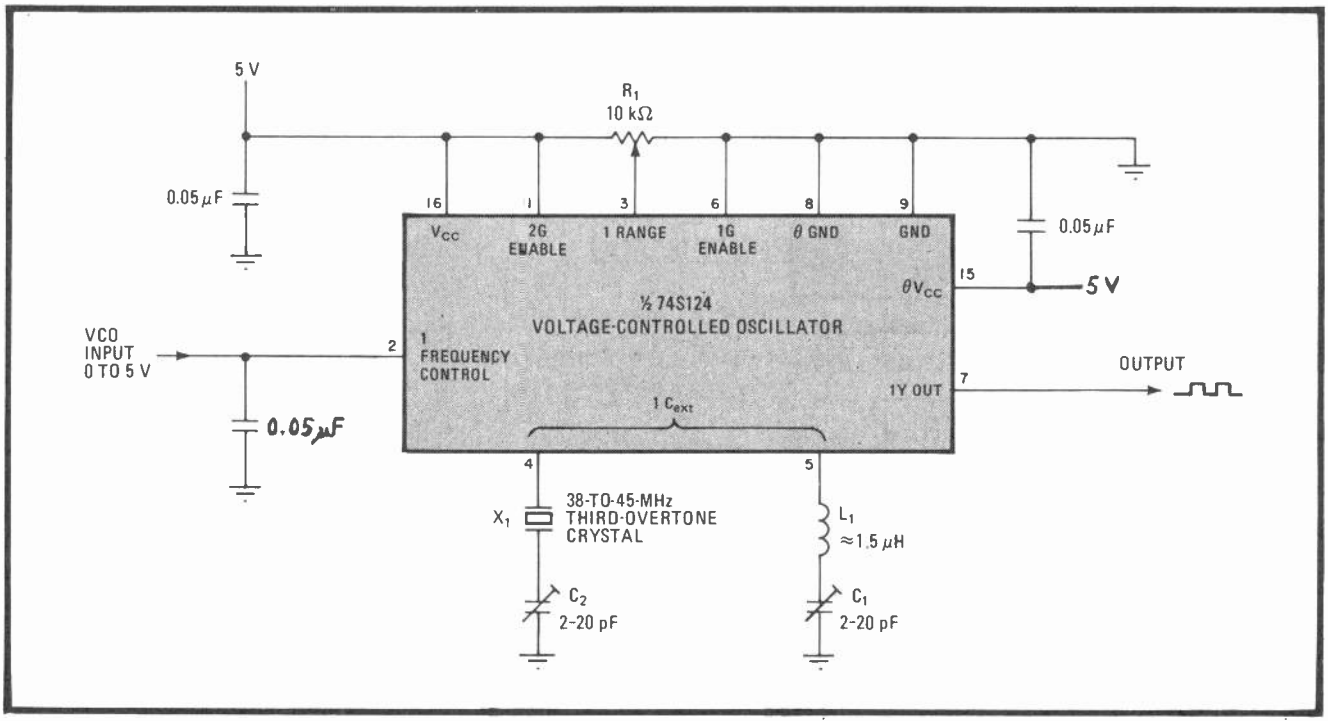
LC network adapts PLL for crystal-overtone operation

by R. J. Athey
National Research Council, Ottawa, Canada

Although Texas Instruments' popular 74S124 oscillator serves reliably in most instances as a crystal-controlled phase-locked loop, problems arise when overtone crystals are utilized for high-frequency (20 megahertz and above) operation. The difficulties may be overcome by adding an LC network in order to retain adequate system gain for oscillation at the required overtone and dampen oscillations at the fundamental frequency. This technique thereby forces the loop to lock onto the crystal's third-order output.

Although the range over which the PLL responds will be limited to about 1 kilohertz for a 0-to-5-V input signal, the method affords repeatable results and will enable use of the 74S124 beyond the normal limits imposed by fundamental-mode crystals. As shown in the figure, L_1 and C_1 are selected to be series-resonant at the desired overtone frequency. Assuming L_1 is 1.5 microhenries, a C_1 value of 2 to 20 picofarads will be adequate for tuning over the range of 38 to 45 MHz required in this particular application. The Q of both L_1 and C_1 should be reasonably high.

C_1, along with R_1, serves as a gross frequency control. Unfortunately, the setting of R_1C_1 will be rather critical. Although the range over which R_1 is effective as a tuning element for a given C_1 is narrow, a miniature carbon potentiometer will have sufficient resolution for making adjustments. C_2 provides an offset for the desired third-overtone frequency. In general, the circuit will work satisfactorily for crystals working to 60 MHz. □



Order of oscillation. Addition of L_1C_1 adapts TI's voltage-controlled oscillator for use as a high-frequency phase-locked loop utilizing an overtone crystal. LC network eliminates crystal's strong fundamental response, forces loop to lock onto slab's third-order output.

Tone detector sharpens digital filter's response

by Steve Newman
Los Angeles, Calif.

Using digital techniques to set the center frequency and the passband, this circuit will serve as a precision tone detector or as a control (transmission) gate for digital bandpass or band-blocking filters. The circuit elements can be easily cascaded to provide as great a degree of selectivity as required.

The general scheme is outlined in (a). Up counters A_1 and A_2 are preprogrammed to generate a carry signal

after N or M input pulses of f_{in}, respectively, where N is equal to or less than 16 and N is greater than M. The period of the reference signal f_{ref}, which is t_{ref}, determines the time each counter is enabled.

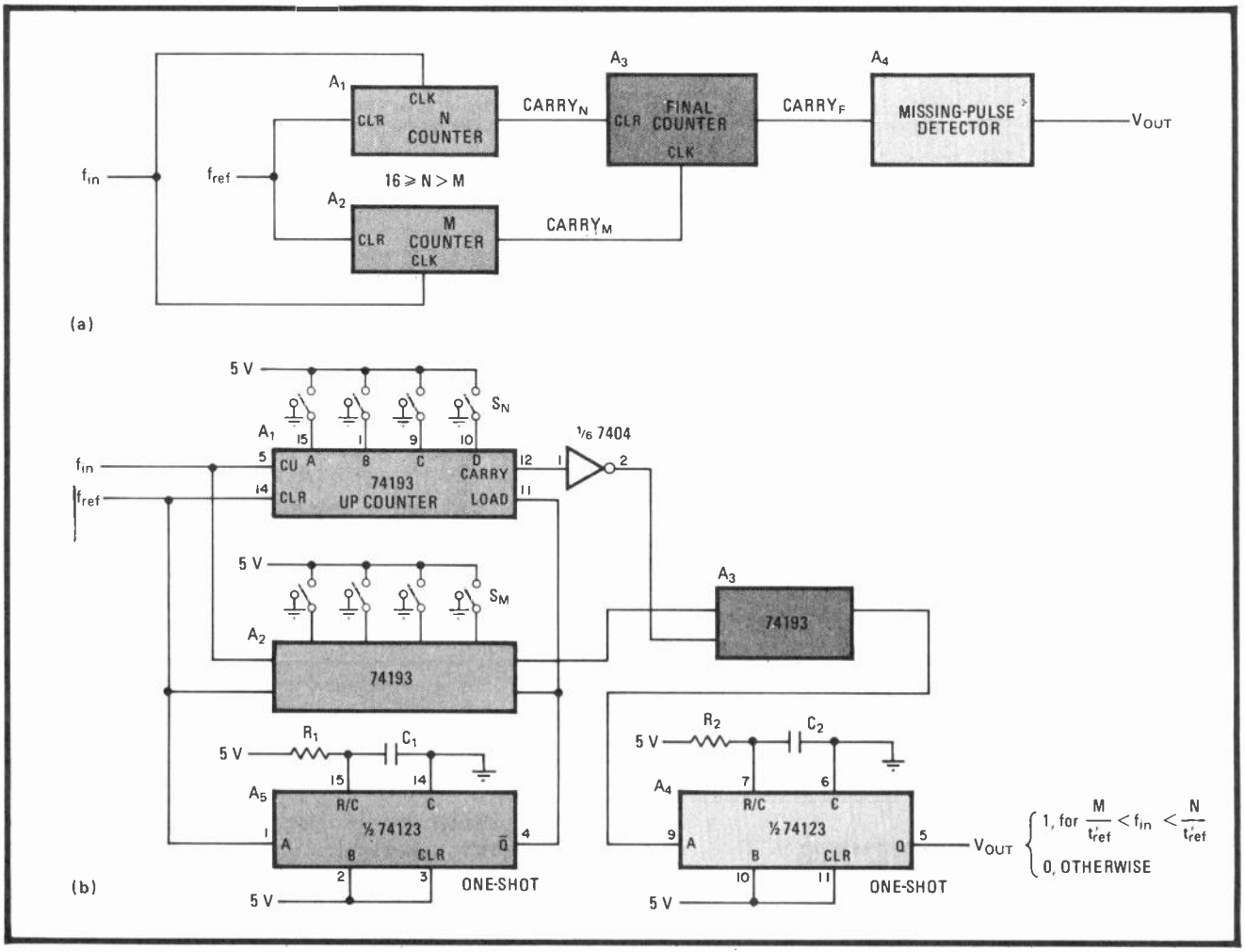
The output of the M counter clocks the presettable counter A_3, while the output of the N counter is connected to its clear input. Thus if M or more pulses occur during the time $\frac{1}{2}t_{ref}$, hereafter called t'_{ref}, the final counter generates carry pulses periodically (this circuit is intended to detect tones of fairly extended duration only). As a result, the output of the missing-pulse detector, A_4, can be forced high.

If, on the other hand, the incoming frequency is greater than N/t'_{ref}, presettable counter A_3 is always reset before it can produce a carry pulse. Thus A_4, which requires a steady stream of pulses to keep it active, is forced low. If f_{in} is less than M/t'_{ref}, A_3 again cannot produce a carry pulse because there are no clock pulses from the M counter. Thus, V_{out} will be high only for the case where $M/t'_{ref} < f_{in} < N/t'_{ref}$.

The actual circuit is shown in (b). A_1 and A_2 are enabled at the instant f_{ref} moves low. A_3 and A_4 assume the same functions described in (a). If the detection process must be sped up, A_3 can be preset so that it generates a carry for every Pth pulse from A_2, in the range 1 to 15. In general operation, however, A_3 is not preset.

At the start of the measurement cycle, f_{ref} initiates the process whereby one shot A_5 presets A_1 and A_2 to their switch-programmed values (switches S_N and S_M are active low). The reference frequency is selected in conjunction with S_M and S_N to provide almost any desired passband.

For example, if a frequency between 9.5 and 10.5 kilohertz (f_{in}) must be detected, M can be arbitrarily selected to be 9 and N = 10. A t'_{ref} = 0.95 millisecond is then required (f_{ref} = 526 hertz at 50% duty cycle). Note the time constant R_1C_1 must be much less than t_{ref}.



Logical boundaries. Tone detector sets limits of desired frequency range digitally. Using counting technique, circuit rejects tones whose frequencies are too high or low. Detector generates output only for $2M/t_{ref} < f_{in} < 2N/t_{ref}$, where f_{in} is input frequency, M and N are the Mth and Nth pulses that generate a carry from the M or N counters, respectively, and $t_{ref} = 1/f_{ref}$, where f_{ref} is the reference frequency.

R_2C_2 must just exceed $240/f_{in}$ to cover the case where M = 15 and N = 16, whereupon as many as 240 input pulses are required to detect the tone. Under these conditions, however, the bandpass will be only 3% of the center frequency, f_o.

If greater selectivity is desired, a pair (or more) of 74193 up counters can be simply cascaded without upsetting the basic operation of the M and N counter chains. With two counters in each chain, the range of M and N can be expanded to 256, whereupon a bandpass of only 0.2% of f_o can be selected. □

D-a converter simplifies hyperbolic clock

by R. H. Riordan
Cybec Electronics, Bentleigh, Australia

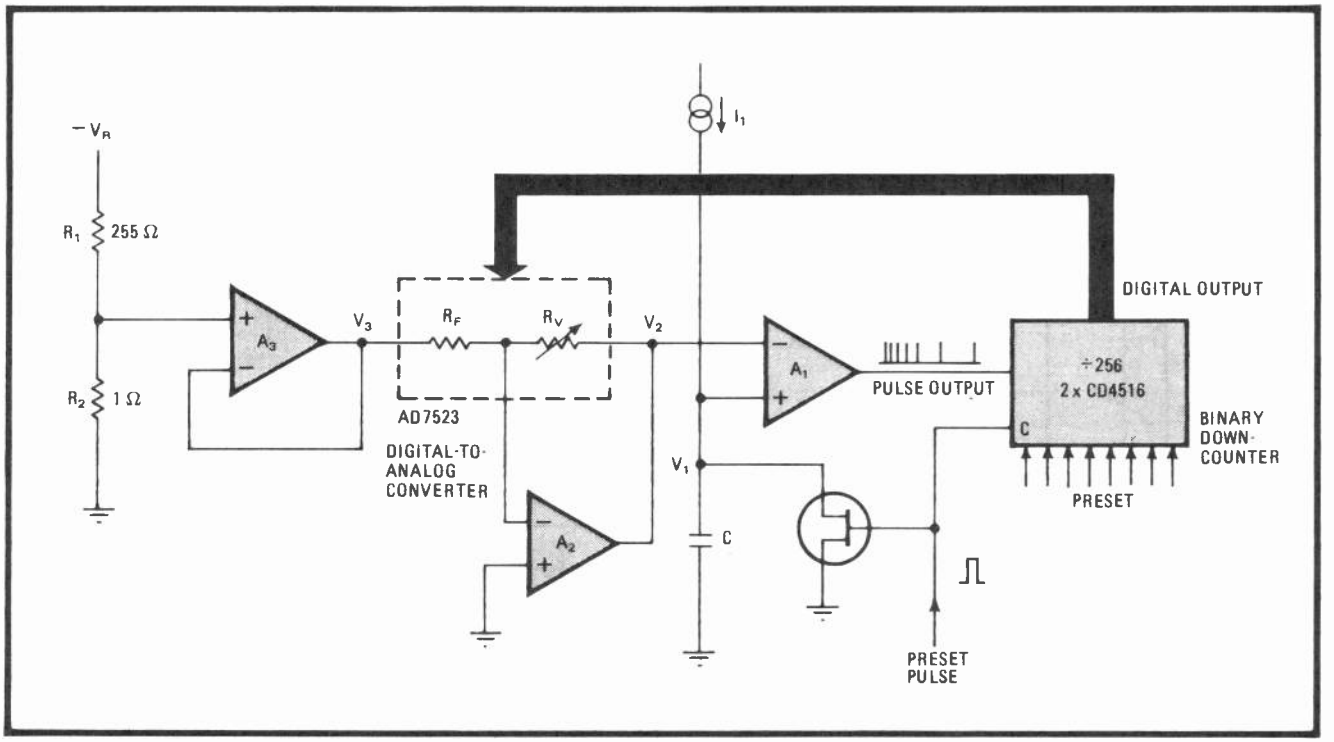
The hyperbolic clock circuit proposed by Baxter [*Electronics*, July 5, p. 132], which transforms a time function, t, into units of 1/t in order to measure rate, can be made more compact by employing a one-chip digital-to-analog converter. Using the converter's monolithic ladder of 255 equivalent resistors in place of Baxter's discrete network for scaling provides greater resolution for a circuit of a given size and is easily modified for applications requiring a decimal output.

Initially, voltage V_1 is set to zero and the 8-bit binary counter formed by cascading two C-MOS 4516 chips is preset to a count of 255. The converter is equivalent to a fixed resistor R_f and a variable resistor R_v, where $R_v/R_f = 256/N$ and N is the output count of the 4516. The converter is connected in the reverse of the normal configuration, so that $V_2/V_3 = -R_v/R_f = -V_3(256/N)$. But $V_3 = -V_{ref}/256$, so $V_2 = V_{ref}/N$.

At first, $V_1 = 0$ and $V_2 = V_{ref}/255$. At $t = 0^+$, current generator I_1 starts to charge capacitor C_1, and V_1 begins to rise linearly with time. Whenever V_1 climbs above V_2, comparator A_1 generates a clock pulse, decrementing the counter and causing V_2 to rise above V_1 again. For any given count N, a clock pulse will be generated at a time t when $V_1 = I_1t/C = V_{ref}/N$. Thus, until the counter reaches zero, the count at any instant will be proportional to the reciprocal of the elapsed time.

This circuit, as well as Baxter's, has a potential weakness in that if a single-step cycle does not result in V_2 rising above V_1, a lock-up condition will occur. This danger is eliminated if a separate clock signal is provided for the counter, with A_1 used only to enable the 4516s.

If decimal timing signals are required, it is a relatively simple matter to replace the d-a unit and the counter with their decimal-output equivalents. If a different step range is required, it can be selected accordingly by changing only R_1 and R_2. R_1 and R_2 are also used to set the desired count range. □



Turnabout. Clock inverts time function, t, in order to measure rate. D-a converter's ladder network, driven by counter, generates stepping function that is compared to ramp voltage V_1 at A_1. V_1's linear increase and V_2's monotonic rise are almost equal initially, but rates of rise diverge hyperbolically, so that counter is stepped at 1/t intervals. R_1 and R_2 set step size; I_1 sets scaling factor.

Switching preamp improves a-d converter sensitivity

by Peter Bradshaw
Intersil Inc., Cupertino, Calif.

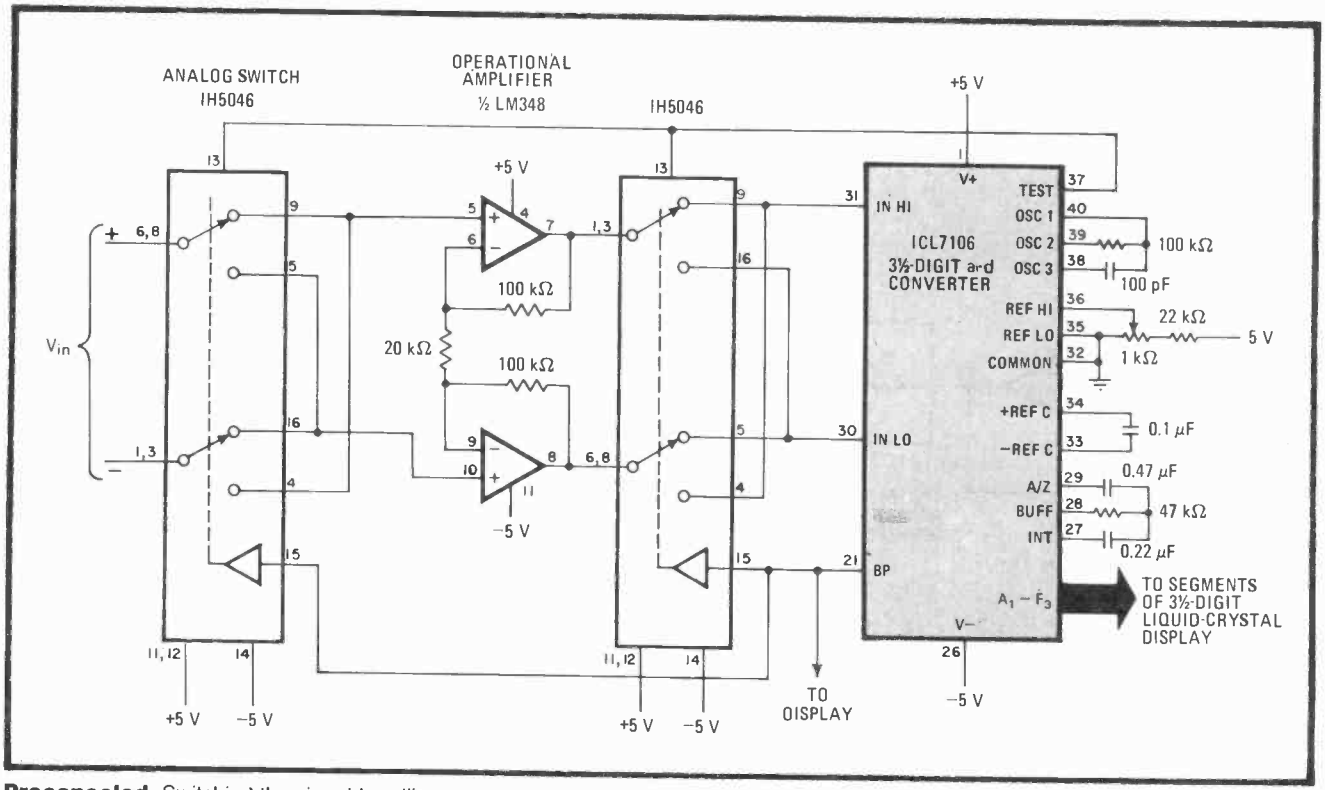
The low-signal resolution of even the best analog-to-digital converters, including those equipped to eliminate input-offset disturbances, is limited by the noise generated at the inputs. But the resolution, and thus the true sensitivity, of a converter can be inexpensively improved by an order of magnitude if a switched, differential amplifier is employed at the input to precancel offset errors without affecting the normal conversion process.

The technique is illustrated for Intersil's ICL7106 3½-digit autozero converter/display driver, which normally handles signals over the range of 100 millivolts to 2 volts. In such a converter, the small input noise voltage trapped on the autozero capacitor during a conversion sets the aforementioned lower signal-handling limit. The noise (which is caused by the equivalent noise resistance at the input, not a component of the signal) can be minimized to a great degree with preamplifiers having low offset voltage, but this can be a rather expensive solution to the problem.

As shown, an alternative approach is to use the liquid-crystal-display backplane (BP) drive output of the ICL7106 to synchronously switch one half of the low-cost LM348 quad operational amplifier via analog switches so that, over a switching cycle, the input of the converter sees no instantaneous change in the magnitude or polarity of sample voltage V_{in}. Offset voltages, including that of the op amp, on the other hand, are virtually canceled because an equal but opposite noise component (average value is near zero) is applied to the IN HI (and IN LO) ports of the converter over a given interval. In this case, the switching (BP) signal is set at about 60 Hz, but this can be varied by suitable selection of the RC components at pins 38 and 39 of the ICL7106. In this configuration, excellent performance is obtained for input signals from 10-20 mv full scale.

Most dual (matched) op amps will be suitable for the switching task, but it is important that both the positive and negative slew rates of the device be reasonably close. Op amps having significant crossover distortion (such as the LM124/324) should not be used.

The CD4053 or the Intersil IH5046 will serve well as the analog switches. In the case of the 4053, 1⅓ devices will be required. Only one double-pole, double-throw switch is contained in each 5046, however, and so two of these devices would be required. □



Precanceled. Switching the signal-handling op amp at 60-hertz rate virtually eliminates input-offset errors of converter, thereby improving sensitivity. Converter's input sees no instantaneous change in V_{in} during switching cycle, and normal conversion process is not affected. But offset voltage at input is alternately fed to (+) and (−) ports; thus equivalent noise voltage over cycle is near zero.

Ramp generator has separate slope and frequency controls

by Henrique Sarmento Malvar
Department of Electrical Engineering, University of Brazilia, Brazil

Isolating with four analog switches the frequency-determining portion of the circuit from that controlling the charging and discharging of its RC integrator, this ramp generator achieves independent selection of slope ratio and repetition rate. Such a unit is useful in a music synthesizer, where timbre must be changed without affecting a note's fundamental frequency..

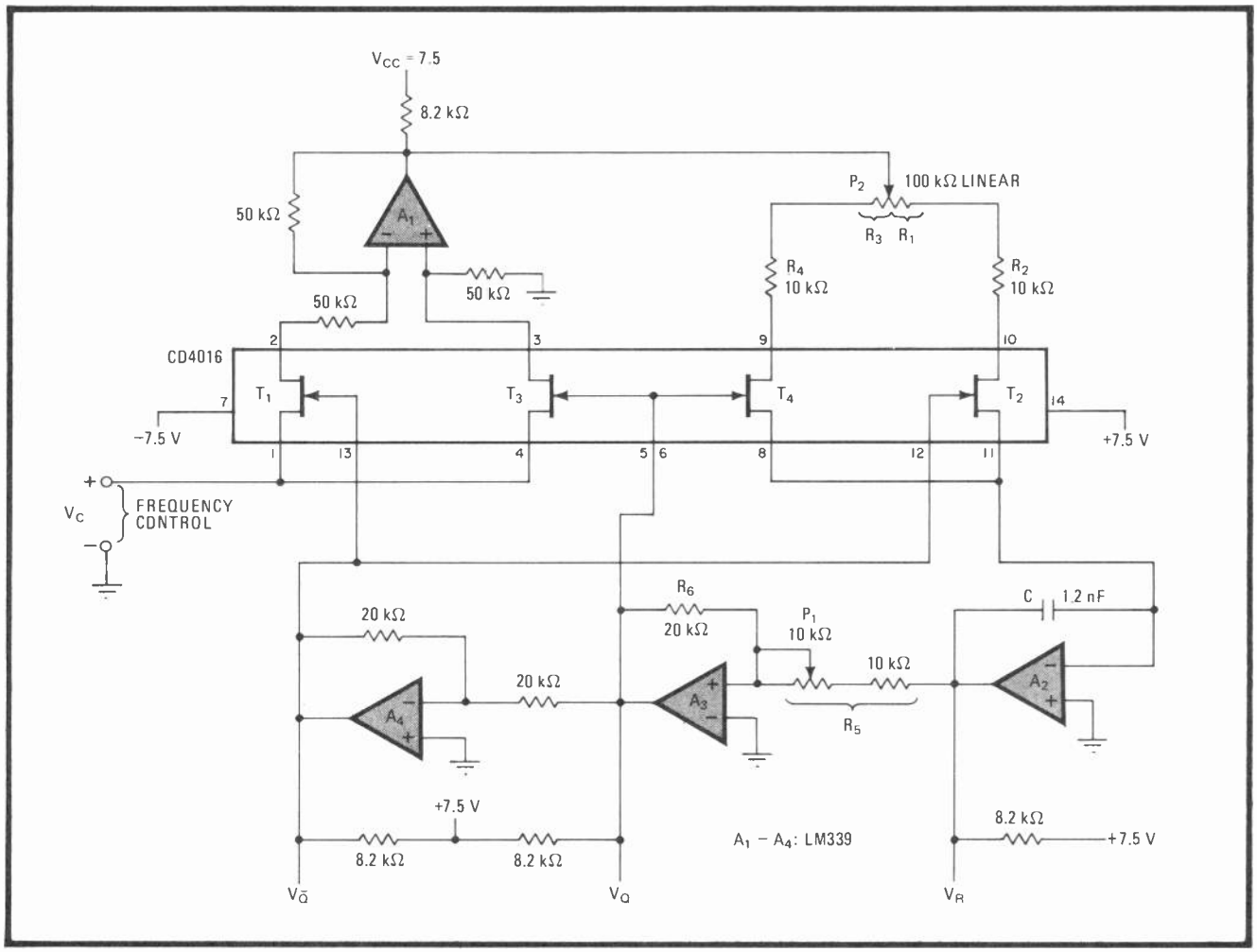
Analog gates T_1 and T_2 are initially switched on, and therefore V_c is applied via operational amplifier A_1 to the integrator built around A_2 (see figure). Thus, $-V_c$ appears at the inverting input of A_2, and its positive-going output reaches voltage V_H in $T_1 = 2V_HC(R_1+R_2)/V_c$ seconds, where $V_H = V_{cc}R_5/R_6$.

At this time, A_3 switches on and A_4 goes off. T_1 and T_2 are thus disabled, and T_3 and T_4 are brought high so that $+V_c$ is applied to the integrator. The output at A_2 thus falls linearly toward $-V_H$, where time $T_2 = 2V_HC(R_3+R_4)/V_c$.

The frequency of the ramp is given by:

$$f = 1/(T_1+T_2)$$
$$= R_6V_c/[2CR_5V_{cc}(R_1+R_2+R_3+R_4)] = kV_c$$

where k is a constant (in the approximate range of 1 kHz/V) that can be adjusted with potentiometer P_1. Because R_1+R_3 is a constant, it is seen that an adjustment in potentiometer P_2 will affect the slope ratio, but not the frequency. With the values shown, the slope ratio can be selected from 1/11 to 11. The slope ratio is given by $T_1/T_2 = (R_1+R_2)/(R_3+R_4)$. □



Separation. Transmission gates T_1–T_4 separate the portion of the ramp generator that determines the frequency from the circuitry that sets the charge and discharge times of its integrator, so that the up/down slope ratio and frequency can be independently selected. The inexpensive circuit, which costs less than $10 and works in the audio range, is a useful timbre control in music synthesizers.

One-chip power amplifier controls dc motor's speed

by Kuang-Lu Lee and Dennis Monticelli
National Semiconductor Corp., Santa Clara, Calif.

Circuits for regulating the speed of small dc motors need not be expensive or complicated now that one-chip power operational amplifiers are available. In fact, using the power device (such as the LM13080) in a simple negative-feedback configuration provides better regulation than many speed controllers now on the market. In addition, common-mode rejection of power-supply transients is large.

As shown in (a), the circuit's reference voltage is established by D_2 and R_3 and filtered by R_5 and C_1. D_1 simply serves as a common-mode level shifter for the inputs of the op amp. Negative feedback around the op amp provides the contolled-voltage drive to the motor. Thus:

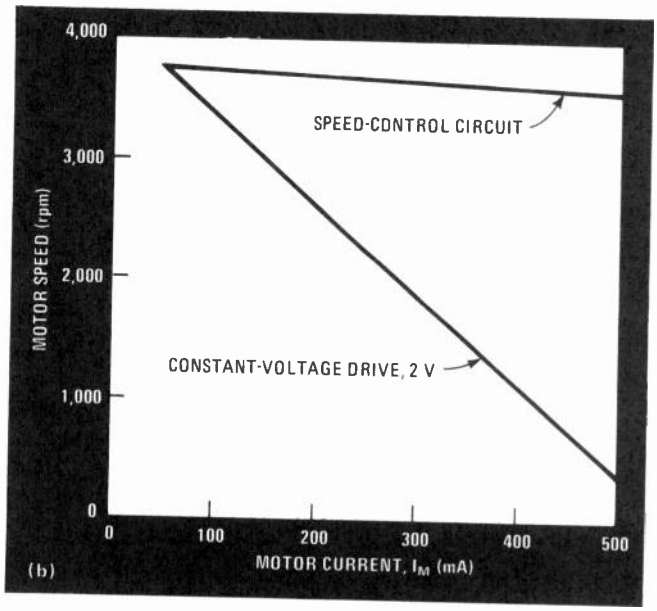
$$V_{motor} = (V_{D2} + I_m R_3)(R_2/R_1) + V_{D2}$$

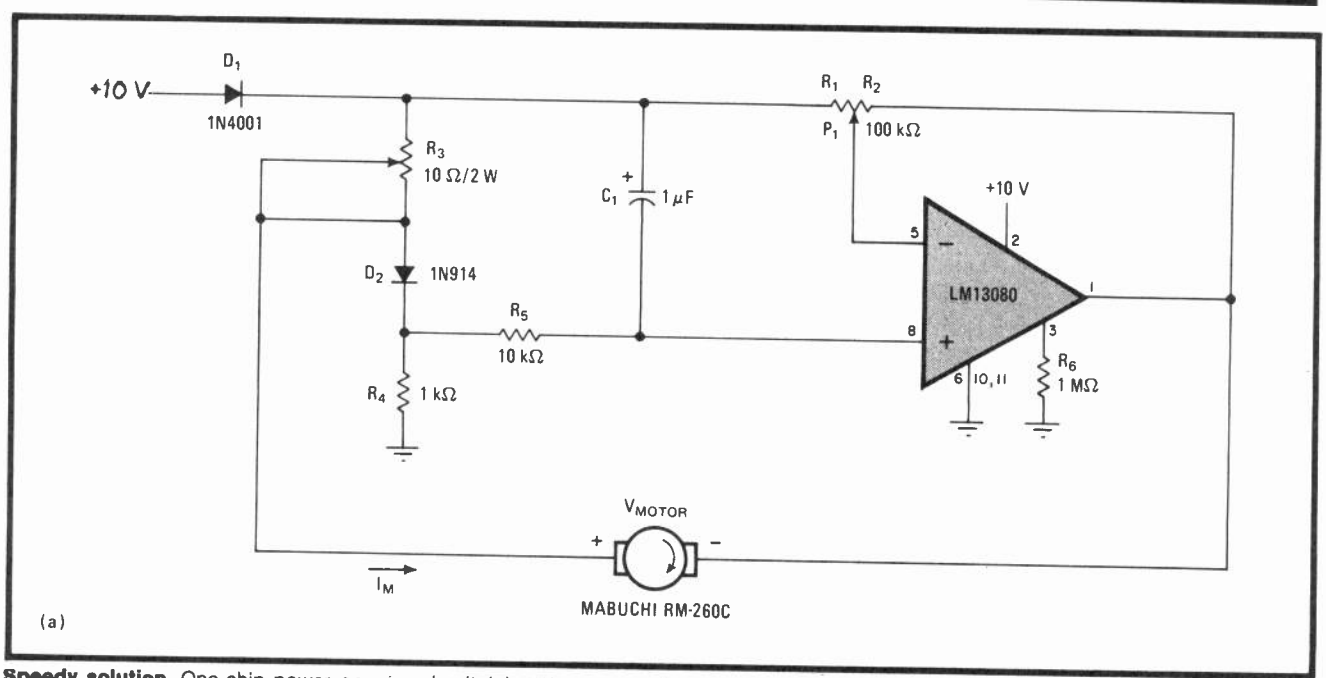
where V_{D2} is the forward voltage drop of diode D_2 and I_m is the current through the motor.

As the motor load increases, I_m increases, and this results in a corresponding increase in V_{motor}. To accommodate large changes in load, V_{motor} varies considerably. The amp therefore needs a 10-volt source voltage to provide sufficient swing, current, and power dissipation for most small motors. Powered by such a source, the LM13080 will handle up to 2 watts in free air and can deliver 0.5 ampere.

The optimum settings for potentiometers P_1 and R_3 are those that provide stable regulation. They are found empirically with the actual motor to be used. P_1 is first adjusted experimentally so that the motor will provide slightly fewer than the desired number of revolutions per minute. R_3 is then increased until a minimal loss in speed is observed for a substantial increase in motor load. Note that excessive positive feedback via R_3 will cause instability. Because the adjustments of P_1 and R_3 interact, it will be necessary to readjust both until the best settings are obtained.

The circuit's performance for a small motor is shown in (b). Note its superior performance with respect to a popular configuration that drives the motor from a constant-voltage source. □





Speedy solution. One-chip power op-amp circuit (a) makes simple, low-cost speed control for small dc motors. Circuit affords excellent common-mode rejection. Controller's rpm-vs-load performance (b) is superior to that of circuits utilizing a constant-voltage drive.

Peak-reading millivoltmeter responds instantaneously

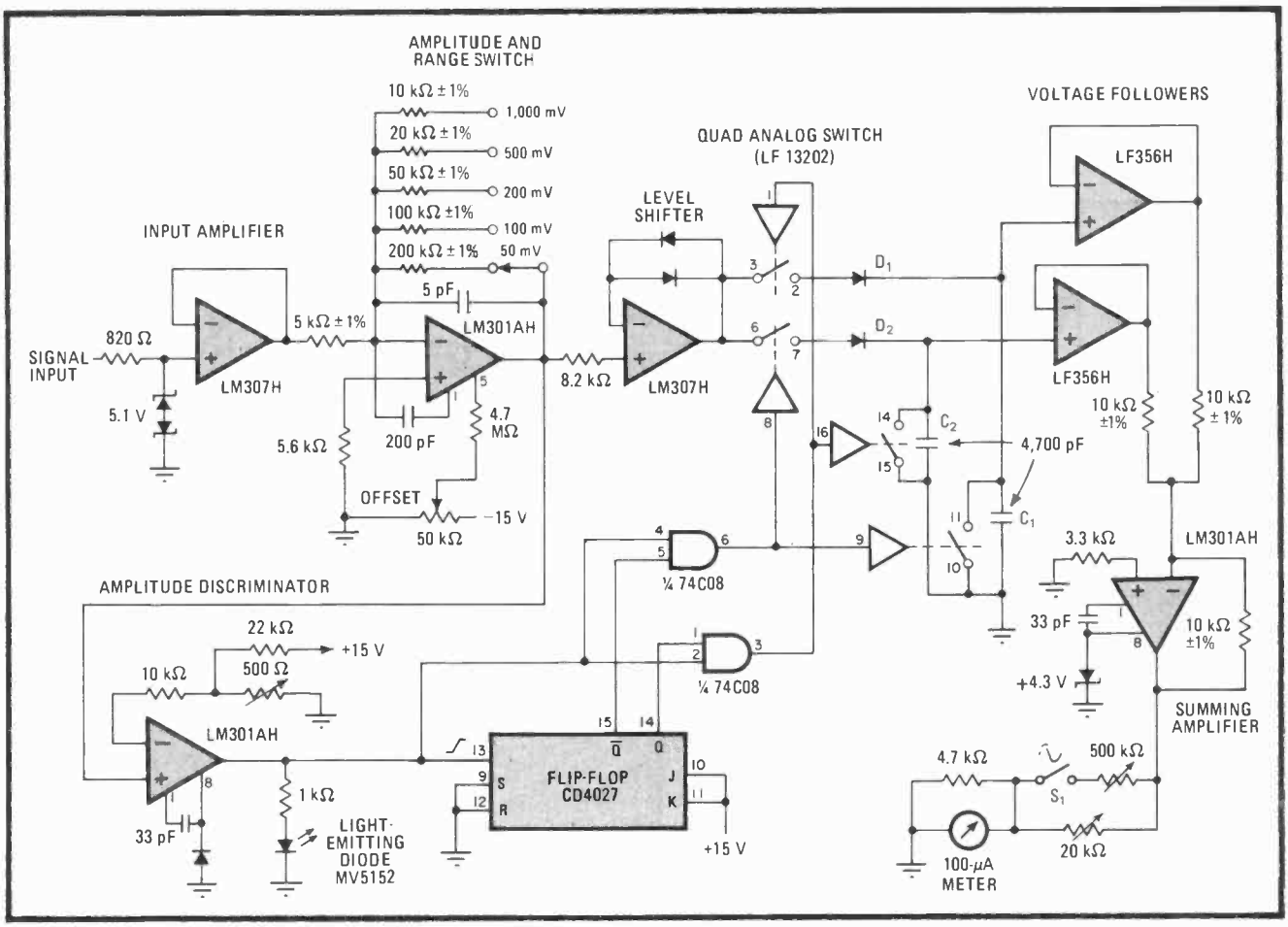
by William J. Mundl
Department of Psychology, Concordia University, Montreal, Quebec, Canada

Requiring but a single pulse or cycle of a sine, square, or triangular wave in order to determine its peak value, this millivoltmeter-microammeter will serve as a respectable substitute for an oscilloscope, oscillographic recorder, or other instrument that must deliver an instantaneous response. Such a low-cost unit is extremely useful in biomedical applications, where the amplitude of certain electrophysiological variables of small magnitude has to be closely monitored.

The millivoltmeter processes either negative-going pulses or the negative portion of the incoming waveform. The signal voltage first passes through the LM307 input amplifier and through the LM301 range amplifier (see figure). The level shifter that follows imparts a positive offset to the signal to compensate for the voltage drop of charging diodes D_1 and D_2, which transfer the peak value of the wave to holding capacitors C_1 and C_2. The voltages on C_1 and C_2 are then alternately applied to the input of the LM301 summing amplifier; any change in the amplitude of the input signal will thus be instantly reflected at the output.

Capacitor switching is achieved with a quad analog switch (LF13202), which in turn is driven by a toggled 4027 flip-flop that is triggered by the input signal and the LM301 amplitude discriminator. The 500-ohm potentiometer is used to set the input trigger voltage at any point near zero, a necessary condition for detecting small input voltages.

As C_1 is charged, C_2 is discharged, and vice versa. Thus the stored voltage on C_1 or C_2 is constantly and quickly updated without the need for a discharge cycle. Note that the zener diode at the input to the summing amplifier prevents it from overdriving the output meter.



1. Quick update. This meter requires only one negative pulse or half cycle of sine-, square-, or triangular-wave input to determine peak current or voltage amplitude. The applied signal charges capacitors C_1 and C_2 alternately, so that either can update immediately without the need for a separate discharge cycle. The meter's range is 0 to 1 V or 0 to 100 μA. The output meter reflects instantaneous changes.

The output microammeter may be calibrated in millivolts through the use of its associated 20-kilohm and 500-kilohm potentiometers. Switch S_1 must be closed in order to measure sinusoidal waveforms.

Although this meter has been used mostly for measurement tasks below 100 hertz, it will work over a wide range of frequencies and thus is suitable for general-purpose audio-rate applications. As shown, the meter is useful for square waves to 8 kilohertz, sine waves to 10 kHz, and pulse widths down to 15 microseconds. □

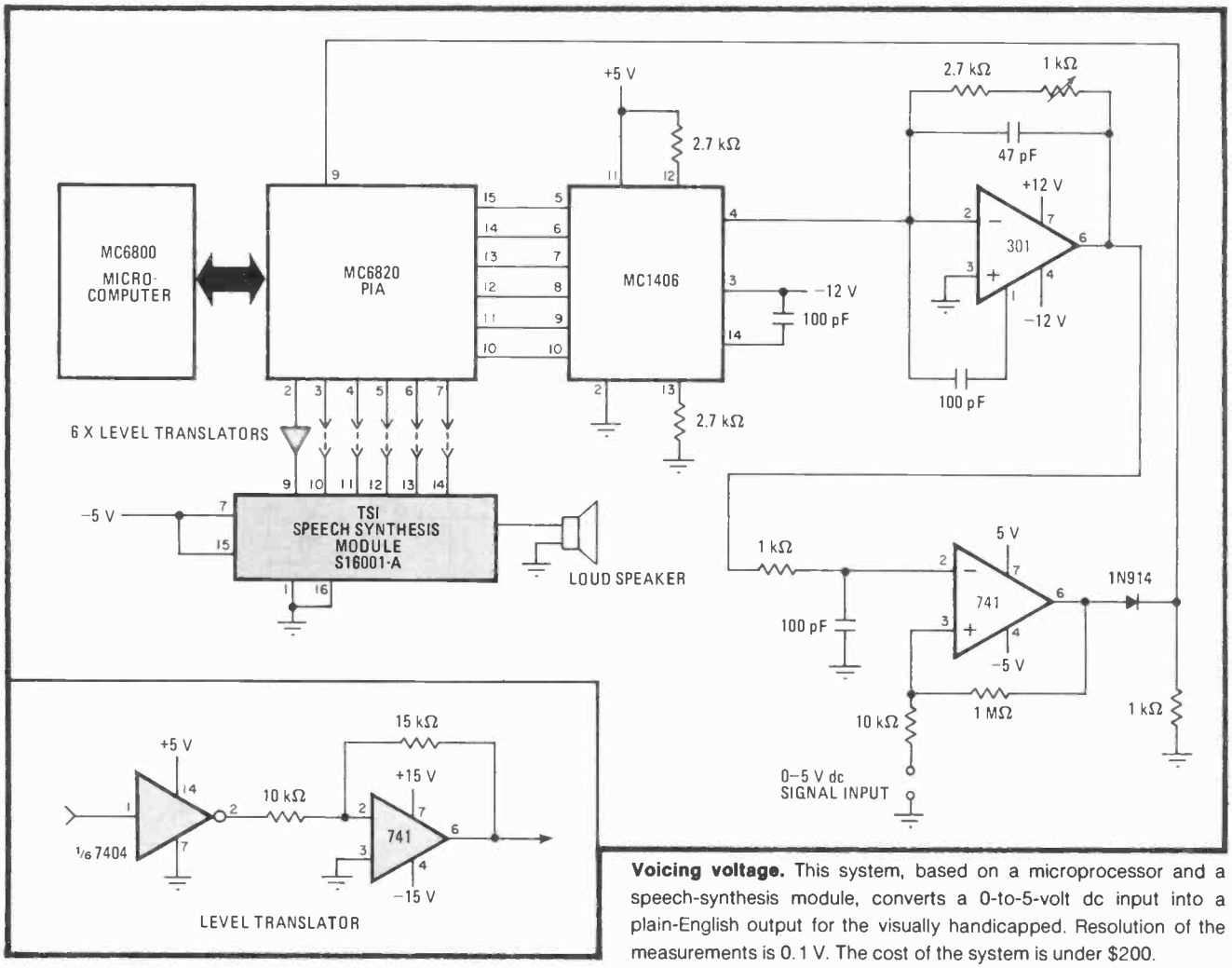
Talking meter voices dc voltage readings

by William S. Wagner
Northern Kentucky University, Highland Heights, Ky.

A relatively low-cost ($150) speech-synthesis module, combined with an interface and a small program written for Motorola's 6800 microprocessor, will convert a dc input signal of 0 to 5 volts into a plain-English output with a resolution of 0.1 v. Thus the meter will be very useful to visually handicapped technicians.

The system is configured in much the same manner as the audible voltmeter previously described, which generates a set of short and long tones corresponding to the voltage measured.[1] But in this instance, the S16001-A speech-synthesis module (from Telesensory Systems Inc., 3408 Hillview Ave., Palo Alto, Calif. 94304) serves as the output device. As a consequence, the software necessary to perform the voltage-to-audio conversion is much less, because it is handled by the synthesizer's internal circuitry.

As shown in the figure, the 0-to-5-v dc test voltage is compared with the output of the 6-bit 1406 digital-to-analog converter at the inputs of the 741 operational amplifier. If there is a voltage difference, the digital input to the 1406 is adjusted, under program control, until the voltage difference is minimized. The binary-coded-decimal word at the output of the 6820 peripheral interface adapter then represents the digital equivalent of the voltage measured. This word addresses the speech-synthesis module, which generates the corresponding voice response. Typical outputs will be heard as "three



Voicing voltage. This system, based on a microprocessor and a speech-synthesis module, converts a 0-to-5-volt dc input into a plain-English output for the visually handicapped. Resolution of the measurements is 0.1 V. The cost of the system is under $200.

6800 TALKING-VOLTMETER PROGRAM					
Address	Mnemonic	Address	Mnemonic	Address	Mnemonic
0000	LDX 7F04	002B	TAB	0059	LDX FFFF
0003	STX 8000	002C	ORAB 20	005C	DEX
0006	LDX FF04	002E	STAB 8000	005D	BNE FD
0009	STX 8002	0031	LDX 0055	005F	DECA
000C	LDB FF	0034	DEX	0060	BNE F7
000E	CLRA	0035	BNE FD	0062	PULA
000F	STAB 8002	0037	ANDB 0F	0063	ANDA 0F
0012	LDX 0055	0039	STAB 8000	0065	TAB
0015	DEX	003C	LDAA 02	0066	ORAB 20
0016	BNE FD	003E	LDX FFFF	0068	STAB 8000
0018	TST 8000	0041	DEX	006B	LDX 0055
001B	BPL 06	0042	BNE FD	006E	DEX
001D	DECB	0044	DECA	006F	BNE FD
001E	ADDA 01	0045	BNE F7	0071	ANDB 0F
0020	DAA	0047	LDAB 33	0073	STAB 8000
0021	BRA EC	0049	STAB 8000	0076	LDAA 04
0023	LDS 00B0	004C	LDX 0055	0078	LDX FFFF
0026	PSHA	004F	DEX	007B	DEX
0027	LSRA	0050	BNE FD	007C	BNE FD
0028	LSRA	0052	ANDB 1F	007E	DECA
0029	LSRA	0054	STAB 8000	007F	BNE F7
002A	LSRA	0057	LDAA 02	0081	JMP 000C

point seven," "one point oh," and "oh point nine."

The 66-instruction program is fairly simple. The first four steps initialize the system. The instructions contained between addresses 000C and 0021 make up the digital-voltmeter portion of the routine, where the aforementioned comparison and minimization of voltages at the inputs of the 741 op amp take place.

At minimization, the BCD word is stored in accumulator A at location 0024, which is the second location of the speech-synthesis section of the program. The analog equivalent of the most significant digit of voltage is then voiced at location 0039.

After a short delay to allow time for the word to be read, the word "point" is brought to the module's input register at 0047 and announced at location 0054. Following a second delay, the least significant digit of voltage is similarly presented to the output register at 0068 and transmitted at location 0073. The program then returns to the digital-voltmeter section of the routine. □

References

1. William S. Wagner, "Digital voltmeter has audible output," *Electronics*, March 29, 1979, p. 120.

Delay circuit replicates pulses of variable width

by John H. Davis
Warm Springs, Ga.

Unfortunately, the simple and well-known circuit used to provide true pulse delay—whereupon the first of two one-shots connected in series sets the delay time desired and the second is set to generate a pulse having the same width—cannot be used if the input pulse width is variable. Fortunately, however, pulses of variable width can easily be handled by adding only a quad NOR gate and a few RC differentiators to a modified circuit, as shown here.

Differentiator R_1C_1 provides a positive-going spike from the rising edge of the input pulse to be delayed, in returns to its low state. As long as $\tau_{A1} = \tau_{A2}$, the time during which I is high will always be equal to the width of the input pulse, assuming the delays are equal to or exceed the input pulse width. Pulses that are very much shorter than the set delay time will be reproduced less accurately.

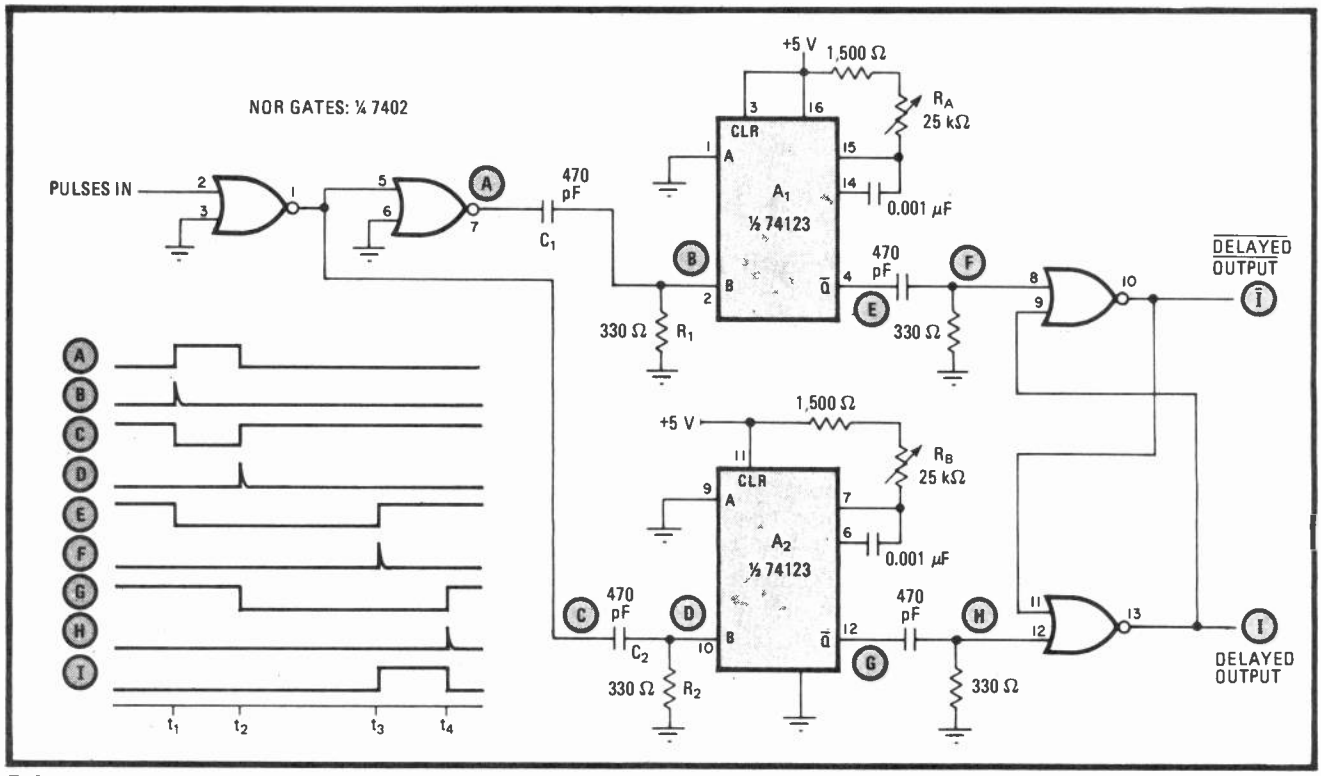
This circuit provides delays over the range of 1 through 20 microseconds, but it is a simple matter to change timing components to achieve times into the millisecond region. Note that the maximum delay that may be set will be limited to the shortest repetition period in the pulse train and in practice should be set to a value less than this to allow for the one-shots to recover.

The circuit is equally suitable for implementation with positive or negative logic. Adjustment is simple. With positive logic, R_A should be set for the desired delay. A train of pulses of nominal width is then introduced at the input, and the I port is monitored with a scope while R_B is adjusted so that the pulse width at the output is equal to that at the input. The circuit will then automatically be calibrated for input pulses having any width. The calibration procedure is similar with negative logic, except that then it is easier to adjust R_B first.

Alternatively, both one-shots may be set for equal delay, but in practice this procedure will cause inaccuracies for very narrow input pulses. In any case, it will be advantageous if circuitry can be configured to program R_A and R_B simultaneously, so that the circuit has only one control. □

for the desired delay interval selected by potentiometer R_A. When the Q output returns to its high state, the RS flip-flop at the output, formed by two NOR gates, is set and the I port moves high.

One-shot A_2 is triggered by the falling edge of the input pulse through differentiator R_2C_2, and thus its $\overline{Q}$ output goes low for a time (set by R_B) equal to A_1's delay interval. When A_2's $\overline{Q}$ output returns high, the NOR latch



Delayed duplication. Parallel-connected one-shots and NOR gates provide set delay and maintain width of pulse, independent of its value. Low-cost unit will thus be useful for automatically synchronizing blanking pulses in TV systems and for similar applications.

Frequency discriminator has ultra-sharp response

by S. J. Collocott, *CSIRO Division of Applied Physics, National Measurement Laboratory, Sydney, Australia*

Most rudimentary circuits for discriminating between two frequencies or two bands of frequencies sacrifice selectivity to simplicity. But this simple circuit, which uses just a frequency-to-voltage converter and a couple of general-purpose comparators, can differentiate between two frequencies separated by only a few hertz.

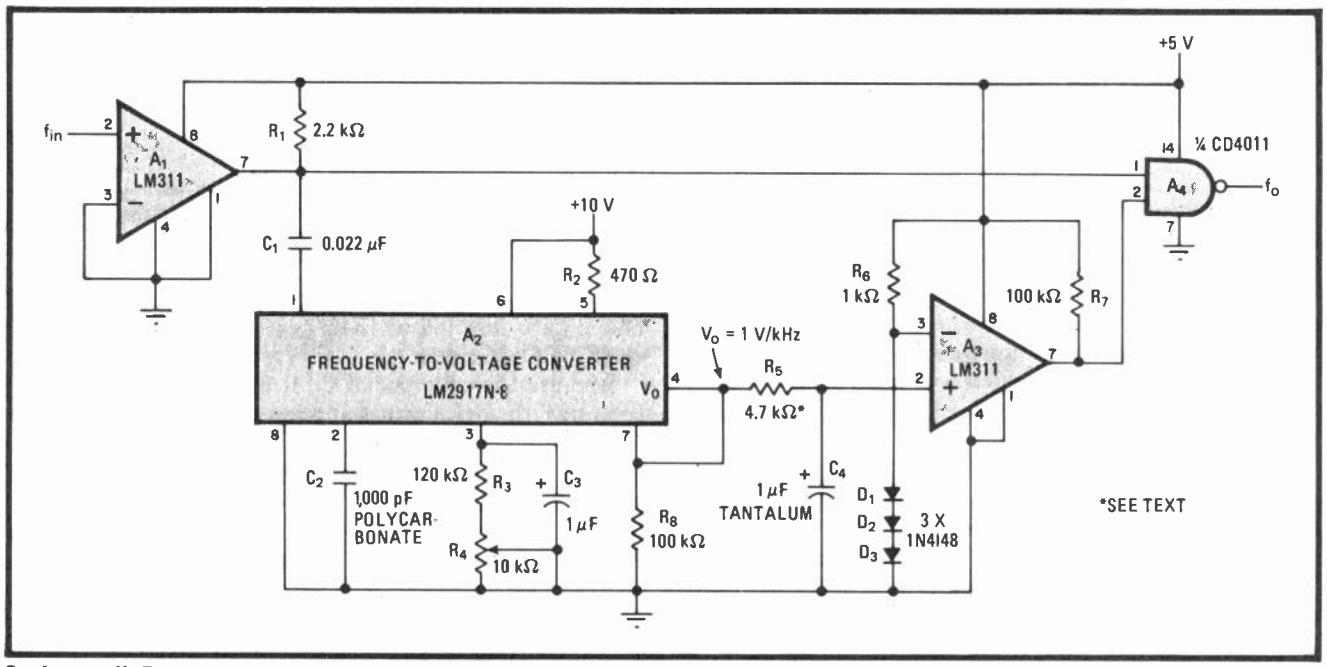
In this application, the circuit rejects all frequencies below 2.1 kilohertz, while passing others, although it is a simple matter to modify the discriminator to handle signals at any frequency. Input signals are introduced into the LM311 comparator (A_1), which operates as a zero-crossing detector. Its output is then applied to one input of a dual NAND gate and A_2, the LM2917 frequency-to-voltage converter.

The converter, which drives the noninverting input of comparator A_3, generates an output of one volt for each kilohertz applied at its input. Thus, when f_{in} is less than 2.1 kHz, the output of the converter is less than 2.1 volts, and A_3 (whose noninverting input is biased at 2.1 V by diodes D_1–D_3) is low. Therefore, output gate A_4 is disabled. If f_{in} moves above 2.1 kHz, A_3 will go high and enable A_4, thereby permitting f_{in} to appear at the output.

The sharpness of the cutoff, which is determined by the transfer function of A_3, is approximately 1 Hz. The response time of the circuit is adjusted by C_3 and R_5C_4. These components act to control the integration time at the output, ensuring that a steady dc voltage is attained after a nominal number of periods of f_{in}. If a fast response time is desired, R_5 and C_4 should be deleted.

The circuit is made to handle signals at any frequency by applying a variable control voltage at pin 3 of A_3, in lieu of the D_1–D_3 and R_6 combination. And the discriminator can be used in other modes, to reject high frequencies, for example, or as a bandpass discriminator.

The discriminator that rejects high frequencies may be realized by simply reversing the inputs to A_3. For bandpass applications, A_3 is replaced by a dual comparator, where the low- and high-cutoff frequencies are set by control voltages on the inverting and noninverting inputs of the comparators, respectively. A_4 must then be replaced with a triple-input NAND gate. □

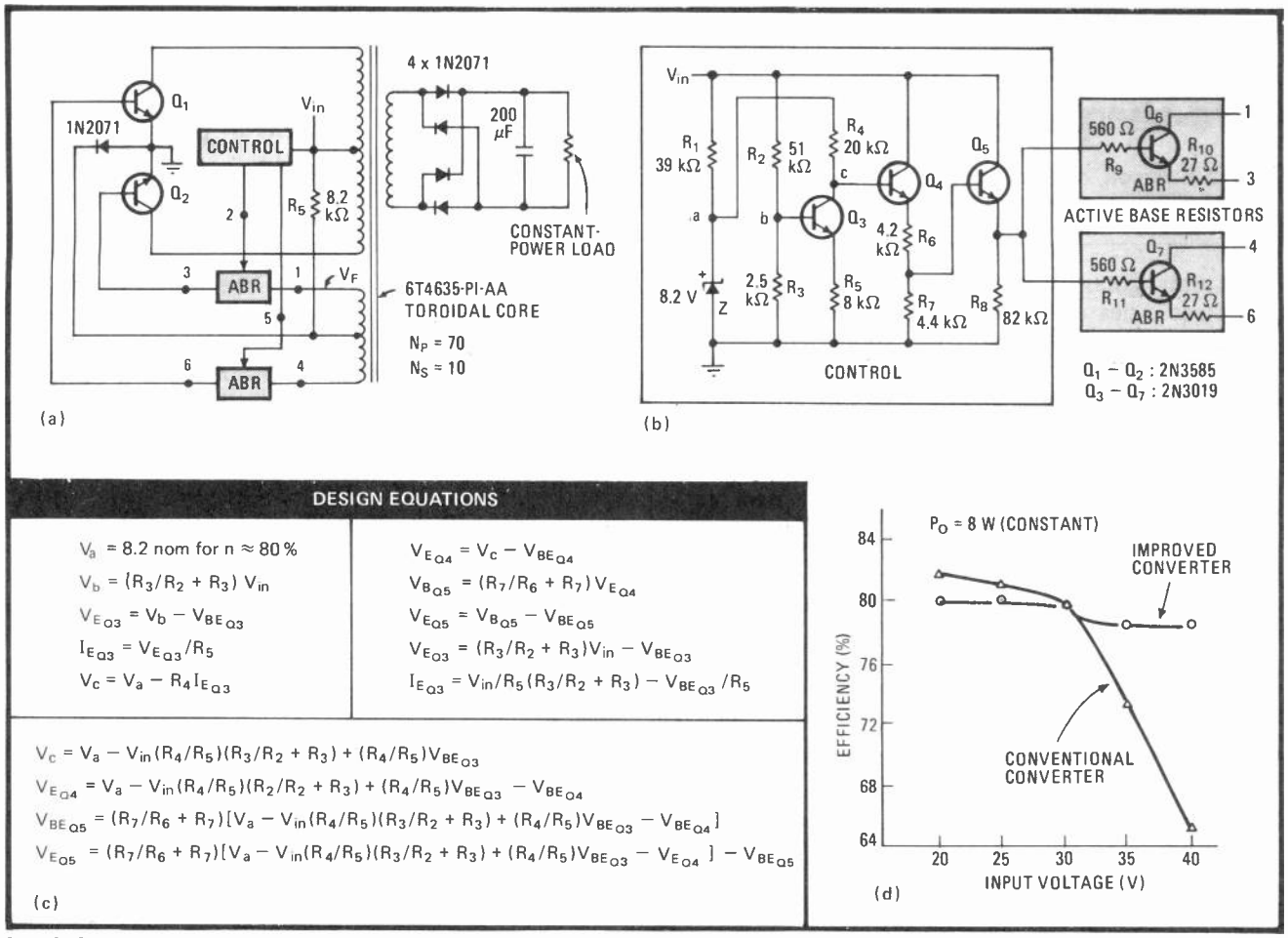


Cycle cutoff. Frequency-to-voltage converter and comparators combine simplicity and selectivity in this frequency discriminator. Transfer function of LM311 determines sharpness of cutoff, in this case being 1 hertz. Circuit can be made to handle signals at any frequency if variable voltage is introduced at pin 3 of A3. Discriminator, configured in high-pass mode, can easily be modified for low-pass or bandpass duties.

Dc-dc converter maintains high efficiency

by P. R. K. Chetty, *Department of Electrical Engineering, California Institute of Technology, Pasadena*

A simple control circuit enables this design to overcome the major drawback of the conventional dc-dc converter—its inability to maintain high efficiency over a wide range of input voltages. Varying the base drive to the converter's power-switching transistors as the inverse square of input voltage in order to achieve a near-constant ratio of output power to circuit losses, this unit attains efficiencies of 78% to 80% for $20 < V_{in} < 40$.



Leveled. High efficiency of conventional dc-dc converter (a) is maintained with control circuit (b) that generates base drive to switching transistors Q_1–Q_2 in inverse proportion to input voltage. Equations (c) aid design. Typical performance (d) is plotted.

In the ordinary converter (a), which would not include the control block shown and where a fixed resistor, R_b, would be substituted for the active-base-resistor block, an increase in V_{in} causes efficiency, n, to drop off as the inverse of the square of input voltage. As may be seen, this loss results because:

$$R_b = V_F/2I_b = [V_F\, n(V_{in} - V_{ce\,sat})hfe_{min}]/2P_o$$

and $V_F = K\, V_{in}$, where R_b is selected to drop half of the feedback voltage, V_F, P_O is the desired output power, $V_{cc(sat)}$ and hfe_{min} are the collector-to-emitter drop and current gain, respectively, of either power transistor, and k is a constant dependent on the turns ratio. Thus, combining the two equations above, it is realized that n is approximately equal to $1/V_{in}^2$, keeping other variables constant.

It can be further shown that if R_b is made to vary as approximately V_{in}^2, the efficiency will be a maximum at any given input voltage. Equivalently, efficiency will be maximum if the base drive to the switching transistors Q_1–Q_2 is made inversely proportional to V_{in}.

Although the circuit required to exactly satisfy Eq. 1 would be complex, a relatively simple configuration (b) will provide acceptable performance when it is added to the basic converter. Here, a three-transistor controller (component values given for P_o = 8 W) and two active-base-resistor networks drive Q_1–Q_2.

As V_{in} increases, the voltage at point b increases. R_2 and R_3 are selected so that V_b is about 1 volt at $V_{in\,min}$, enabling Q_3 to operate in active region.

Because the collector of Q_3 is biased from a reference (point a), the drive signal applied to Q_4 is a function only of the voltage applied to Q_3's base. When the voltage at point B increases, the potential at point C decreases. Thus Q_4–Q_5, biased in its nonlinear i_b–e_c region, drives switching transistors Q_1–Q_2 through Q_6–Q_7 with less base current. As a result, the resistance between points 1–3 (and 4–6) will vary approximately as V_{in}^2.

Only one operating variable must be determined empirically, the voltage at the base of Q_5, $V_{B\,Q5}$. Breaking the circuit at this point to connect a variable-voltage source, the user sets V_{in} to its minimum expected value. The variable-voltage source is then set to saturate Q_1 and Q_2 for a constant P_o, and its value (V_{b1}) noted. The procedure is repeated to find V_{b2} for $V_{in\,max.}$.

Now the design procedure may be initiated using the equations in (c) to determine R_6 and R_7, given that $V_{E\,Q5}$ equals V_{b1} at $V_{in\,min}$ and is equal to V_{b2} at $V_{in\,max}$. Experimental results for P_o = 8, $15 < V_{out} < 35$ and $20 < V_{in} < 40$ are tabulated (d) versus the performance of a conventional converter. □

Hall-probe adapter converts DMM into gaussmeter

by Henno Normet
Diversified Electronics, Leesburg, Fla.

Using a constant-current dc source to maintain the specified accuracy of a Hall probe, this circuit adapts a 3½-digit multimeter for measuring magnetic flux density. The DMM can thus be made to measure densities of 20 kilogauss or more with a resolution of 10 gauss, and this accuracy is more than adequate for all but low-level leakage checks.

The current source built around the 723 voltage regulator will deliver upwards of a constant 50 to 210 milliamperes to the Hall probe (F. W. Bell BH-705 or Siemens FA22e, etc.), ensuring that the internal resistance of the probe, which changes with the field strength encountered, has little effect on the accuracy of the measurement. The linearity of the voltage-versus-flux response will be dependent on the probe's load resistor, R_1, whose value will be a function of the type of probe used (see individual data sheets).

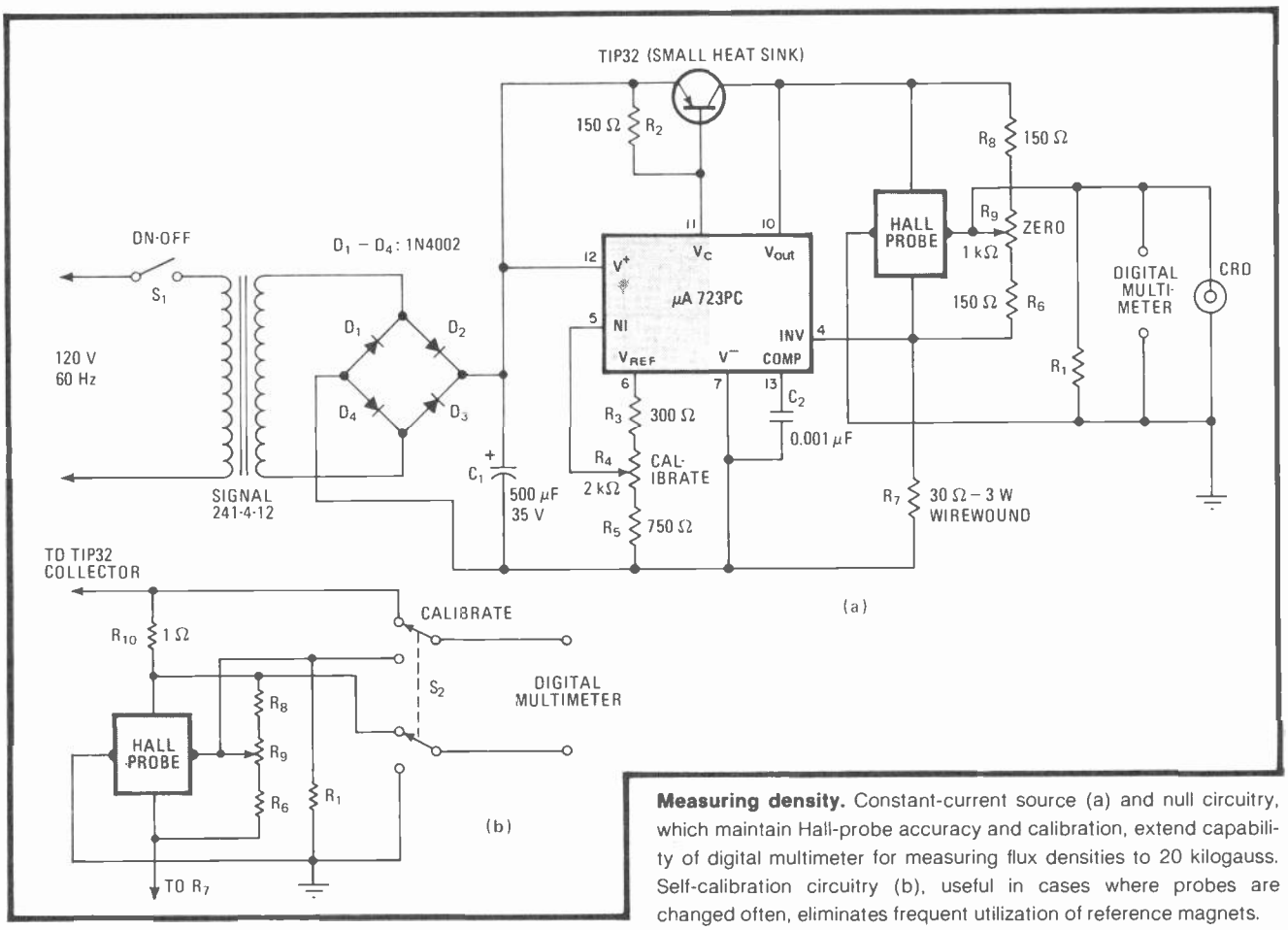
Typical values will range from 3 to 10 ohms. Even with an optimum load, however, most probes will become nonlinear above 10 kilogauss, and at 15 kilogauss the error is considerable. High-flux-density probes are available at increased cost.

To calibrate the adapter, the DMM is set to its 200-millivolt dc range. With the probe isolated from any magnetic field, potentiometer R_9 is adjusted for a zero reading on the DMM. The probe is brought into the field of a calibrated reference magnet, and potentiometer R_4 is adjusted so that the DMM displays a matching value. At these settings, the probe will deliver exactly 10 mV per kilogauss of flux density measured.

The adapter, in conjunction with an oscilloscope, will measure and display ac or pulsed fields; recalibration is not necessary. When used with a scope set for a vertical-channel gain of 10 mV per centimeter, the vertical axis calibration will be 1 kilogauss/cm.

A self-calibration feature that permits the unit to be calibrated without a reference magnet (after the initial adjustment) may be secured by adding a current shunt in the control-current circuit, plus a double-pole, double-throw switch, as shown in (b). This feature is useful when Hall probes are changed frequently.

Calibration is simple. Once the calibration constant for any given probe is determined (see the procedure above), it is only necessary to set switch S_2 in the calibrate position and adjust R_4 for an identical reading on the DMM when that probe is employed. □



Measuring density. Constant-current source (a) and null circuitry, which maintain Hall-probe accuracy and calibration, extend capability of digital multimeter for measuring flux densities to 20 kilogauss. Self-calibration circuitry (b), useful in cases where probes are changed often, eliminates frequent utilization of reference magnets.

Autocorrecting driver rights pulse polarity

by Shlomo Talmor
Hartman Systems, Huntington Station, N. Y.

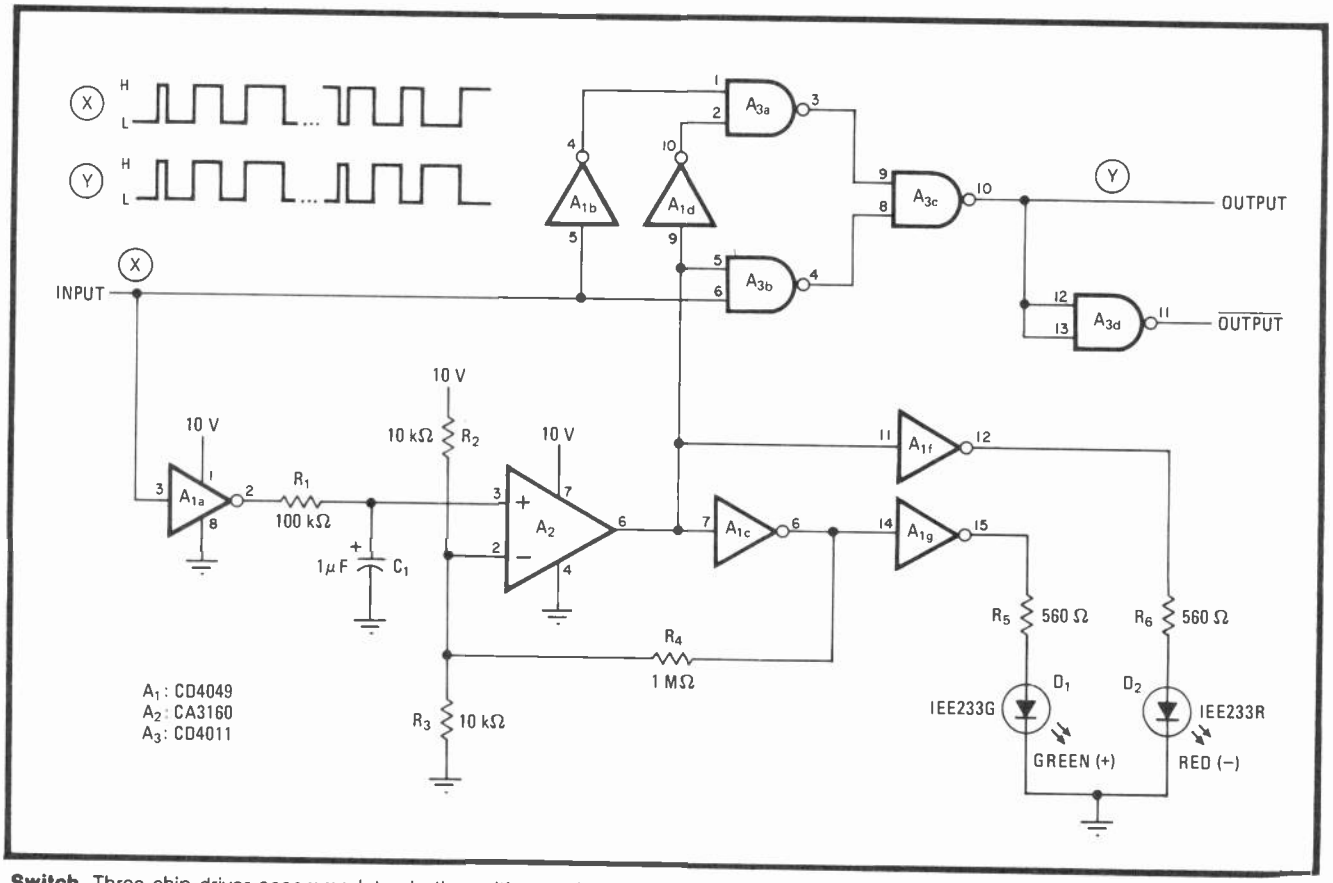
This circuit provides positive-going output pulses for corresponding input signals of either polarity without the need for any manual intervention (that is, polarity switches). Utilizing a simple RC integrator, the unit automatically propagates positive-going signals having a duty cycle of less than 50% through to the output and inverts signals that have a duty cycle of greater than 50%, or are negative-going. The circuit is particularly useful in instrumentation and test-facility applications, where the polarity of the signal emanating from a port is often both positive- and negative-going at different stages of a complicated test sequence.

As shown in the figure, input pulses having a width and rate in the range of 1 microsecond to 1 millisecond are applied through inverter A_{1a} to integrator R_1C_1, thereby developing a dc voltage across the capacitor. Thus, operational amplifier A_2 goes high for positive-going input pulses having a duty cycle of less than 50%. A_{1b} and A_{1d}, along with NAND gates A_{3a} to A_{3c}, therefore propagate the input signal through to the output without an inversion.

If the duty cycle is greater than 50%, or if the incoming pulses are negative-going, the voltage developed on the integrating capacitor will be below 5 volts, which is the potential applied to the inverting input, and A_2 goes low. A_{1b}, A_{1d}, and A_{3a} to A_{3c} then act to invert any negative-going wave at the input to a positive one at the output and vice versa. In the case where the duty cycle is 50%, inverter A_{1c} provides the necessary hysteresis to A_2 for proper switching.

Light-emitting diodes D_1 and D_2, with A_{1f} and A_{1g}, provide visual indication of pulse polarity. Both the red and green diodes will light softly when the input signal has a duty cycle approximating 50%.

The range of the pulse width handled can be extended, at the expense of a lower rate, by increasing R_1. The response time of the circuit will of course be lowered. The supply voltage can vary from 5 to 15 volts, but if it is less than 7.5 v, a 15-kilohm resistor should be placed in series with pin 6 of A_2 in order to properly drive the rest of the circuit. □



Switch. Three-chip driver accommodates both positive- and negative-going input signals, converting them both into positive-going output. Circuit propagates positive-going signals having a duty cycle less than 50% through to the output while inverting all other signals.

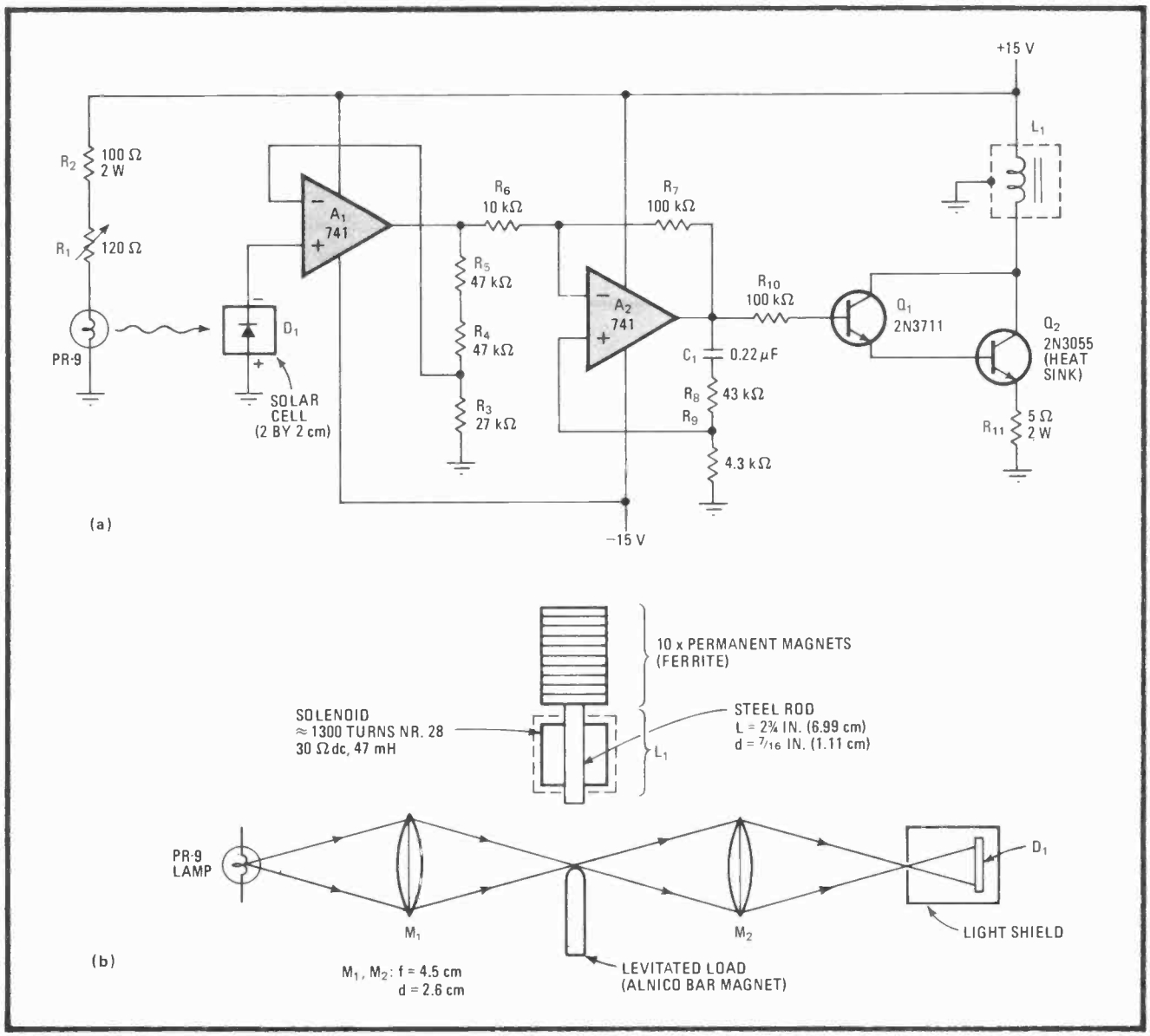
Magnetic levitator suspends small objects

by Bob Leser
Desert Technology, Las Cruces, N. M.

This circuit is a modern solution to the problem of securing frictionless bearings for small rotors and levitating small magnetic objects a few millimeters in space. Operational amplifiers replace the tubes used in earlier approaches, and an optical arrangement replaces the radio-frequency induction circuit originally used to position the object.

Potentiometer R_1 (a) sets the current through the PR9 lamp and thus its brightness and the gain of the position-sensing circuit. R_1 thus provides a fine adjustment of the position of the magnetic object that is suspended beneath the levitation coil L_1. The optical position-sensing circuitry (b), which should be mounted horizontally under L_1 if possible, includes two lenses to focus the beam via the levitated load to solar cell (photodetector) D_1. The light shield, with an aperture of approximately 3 millimeters, effectively eliminates background light. The suggested focal lengths and lens diameters are shown; as a check on the optics system, the beam should be aligned to yield a short-circuit current of 4 to 25 microamperes in D_1.

As for the basic circuitry, D_1's output is amplified by about 5 by operational amplifier A_1 and is then introduced to A_2, which is the all-important servo-loop stage. C_1, R_8, and R_9 provide positive feedback of the high-frequency components of the positioning signal. The stage thus generates the voltage derivative of the amp's output, preventing oscillations in the closed loop that would otherwise occur because of the lack of damping in



Rising rotors. Levitator circuit (a) suspends 1-in. steel spheres up to 2½ millimeters off reference surface. Optical arrangement (b) sets object distance. Details of levitation coil construction are outlined. Permanent magnets set ultimate levitation range.

the position servo portion of the circuit. Any closed-loop oscillation will be manifest as vibration of the levitated object.

Output stage Q_1 to Q_2 is a discrete darlington pair that drives L_1. The coil itself has 1,300 turns around a steel rod 2.75 inches long and 7/16 in. in diameter. A stack of 10 small permanent magnets atop the coil provides a bias field extending the range of levitation beyond that which would be normally attained. The coil is surrounded by a grounded shield to reduce the amount of stray coupling to the op amp inputs.

The most stable closed-loop condition is set by adjusting Q_2's collector voltage to about 7.5 volts by altering the levitation distance between the sensing optics and L_1. Levitation distances in this circuit range from about 20 millimeters for a small Alnico bar magnet to 2½ mm for a steel ball with a diameter of 1 in. □

C-MOS counter sets divider's modulus

by Arie Shavit
Kiriat Tivon, Israel

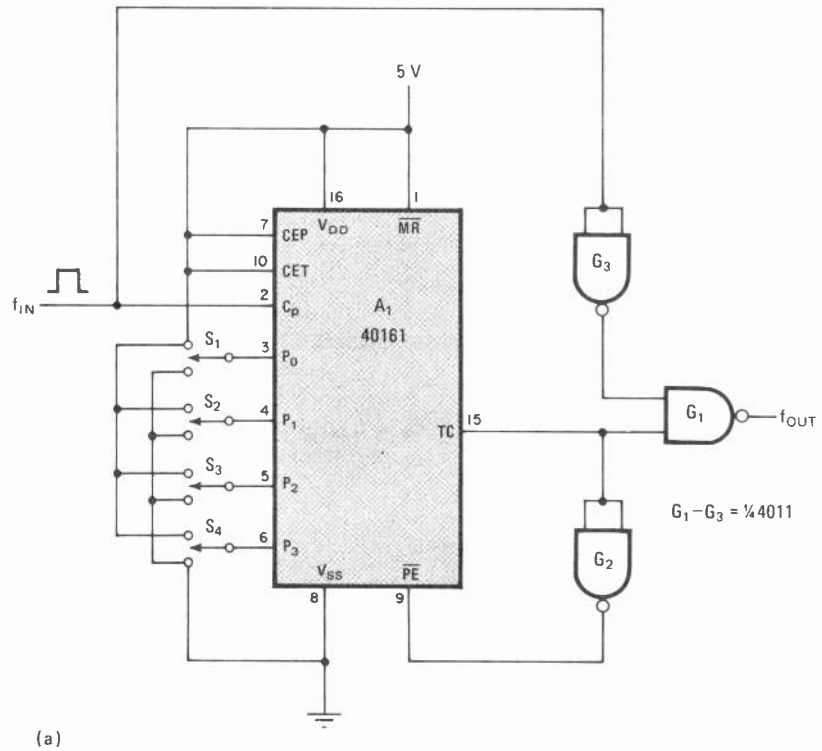
The cost and power consumption of Albing's C-MOS variable-modulo divider[1] can be reduced even further with this circuit, which uses logic gates and four low-cost binary switches to replace one counter and the multiple-pole selector, respectively. Although the counter's modulus is set with the binary elements, thereby sacrificing the convenience of ordering up values in the familiar decimal form, the ease of interfacing the counter to microprocessor-based control systems is immensely enhanced. Divider ratios of from 1 to 16 can be selected.

The 40161 synchronous binary counter, A_1, which has parallel-load capability, is stepped by input frequency f_{in}, as shown in (a). Switches S_1–S_4 set the binary representation of 16 − n at the parallel-load inputs P_0–P_3, where n is the desired divider ratio, as shown in (b).

Output pin TC of A_1 moves high after n cycles of f_{in}. Thus the output signal from gate G_1 is a pulse of short duration having a frequency of $f_{out} = f_{in}/n$. TC is then inverted by gate G_2 and used to reset the counter.

Gate G_3 comes into play if a modulus of 1 is set. Under these conditions, TC remains high and f_{in} serves to gate itself to the output. □

References
1. Bradley Albing, "C-MOS counter-decoder pair sets divider's modulus," Aug. 30, 1979, p. 140.



Binary code				Divider ratio n
S_4	S_3	S_2	S_1	
1	1	1	1	1
1	1	1	0	2
1	1	0	1	3
1	1	0	0	4
1	0	1	1	5
1	0	1	0	6
1	0	0	1	7
1	0	0	0	8
0	1	1	1	9
0	1	1	0	10
0	1	0	1	11
0	1	0	0	12
0	0	1	1	13
0	0	1	0	14
0	0	0	1	15
0	0	0	0	16

(b)

Binary breakup. Single counter and three gates simplify design of variable-modulo divider (a). Binary switches S_1–S_4 set counter to 16 − n, where n is desired divider ratio (b). Output of gate G_1 is a pulse with a frequency equal to $f_{out} = f_{in}/n$, for $1 \leq n \leq 16$.

Foldback limiter protects high-current regulators

by A. D. V. N. Kularatna
Ratmalana, Sri Lanka

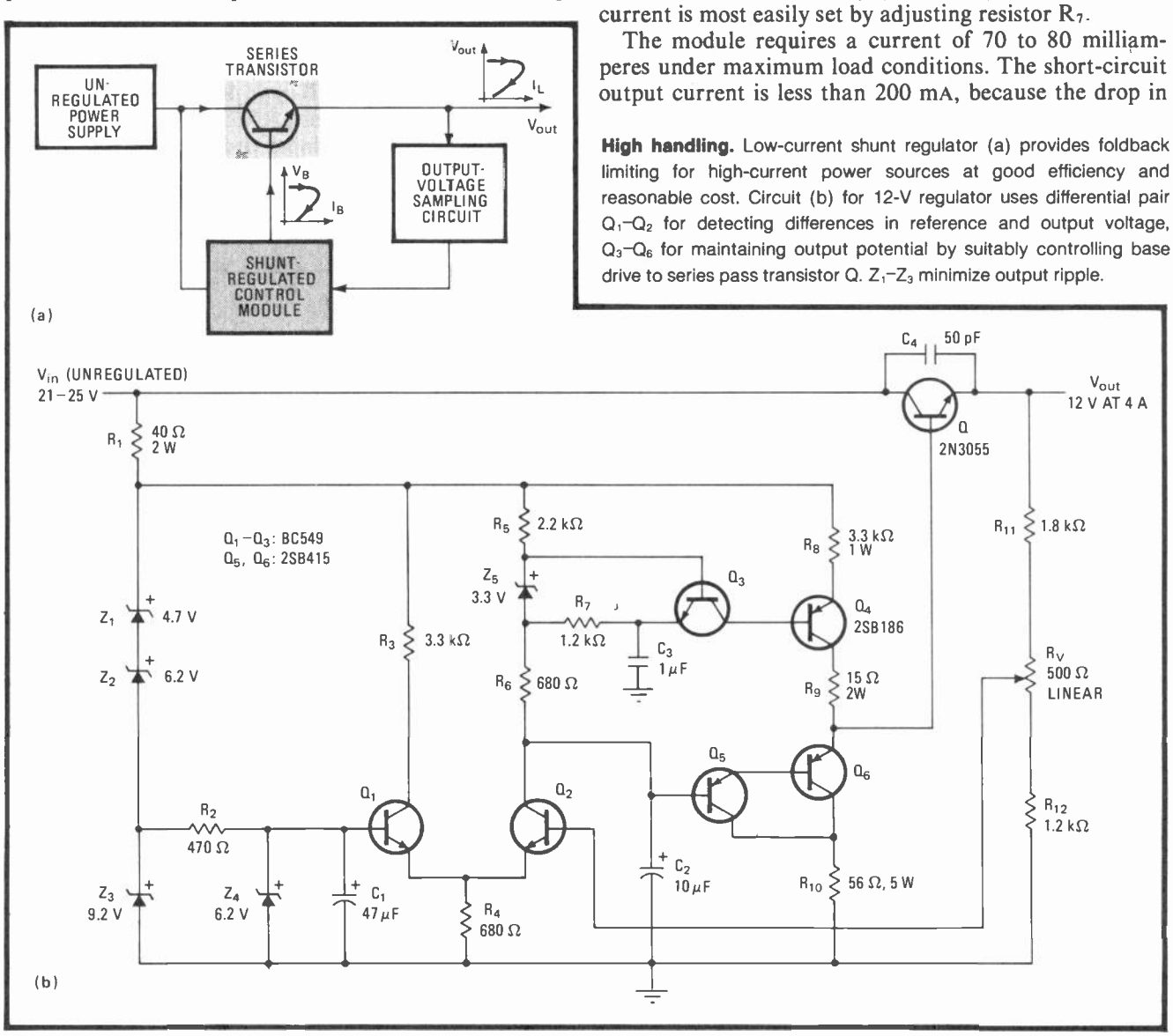
This circuit provides foldback protection for a series-regulated source that has to deliver high current. Because it requires no current-monitoring resistor, the circuit achieves wide dynamic response at good efficiency. It draws only 2% of maximum load current and its cost is reasonable.

Here, a low-current shunt-regulated module (a) provides the overload protection. This module is configured into the conventional regulator system to work as a switch, in which role it quickly turns off a series-pass transistor when the load current exceeds some predetermined value.

The circuit details are explained with the aid of the diagram (b) for a representative regulator designed to deliver 12 volts at 4 amperes. Transistors Q_1 and Q_2 form a differential amplifier, which compares a 6.2-V reference to a potential derived from the 12-V output through potentiometer R_V. Shunt elements Q_5–Q_6 act to maintain the potential at the base of Q constant for any load condition by taking up the difference between the set and the actual base drive.

It is necessary that the current source Q_3-Q_4 be set to I_L/h_{fe} for proper tracking, where I_L is the maximum load current and h_{fe} is the current gain of Q. The value of the constant current, I, is $h_{fe\,Q4}\,(V_{Z5} - V_{be\,Q3})/R_7$, so that the current is most easily set by adjusting resistor R_7.

The module requires a current of 70 to 80 milliamperes under maximum load conditions. The short-circuit output current is less than 200 mA, because the drop in



High handling. Low-current shunt regulator (a) provides foldback limiting for high-current power sources at good efficiency and reasonable cost. Circuit (b) for 12-V regulator uses differential pair Q_1–Q_2 for detecting differences in reference and output voltage, Q_3–Q_6 for maintaining output potential by suitably controlling base drive to series pass transistor Q. Z_1–Z_3 minimize output ripple.

output voltage switches transistor Q_2 off. The voltage across zener diode Z_5 is then reduced to a very low value, and this action in turn lowers the voltage at Q_6 and cuts down the base drive to Q.

Zener diodes Z_1–Z_3 were added to improve the ripple characteristics of the supply. As configured, the source has an output ripple of 6 mV peak to peak.

The shunt regulator module can be easily configured for any output voltage mainly by selecting the appropriate zener-diode values. □

Remote controller sets universal motor's speed

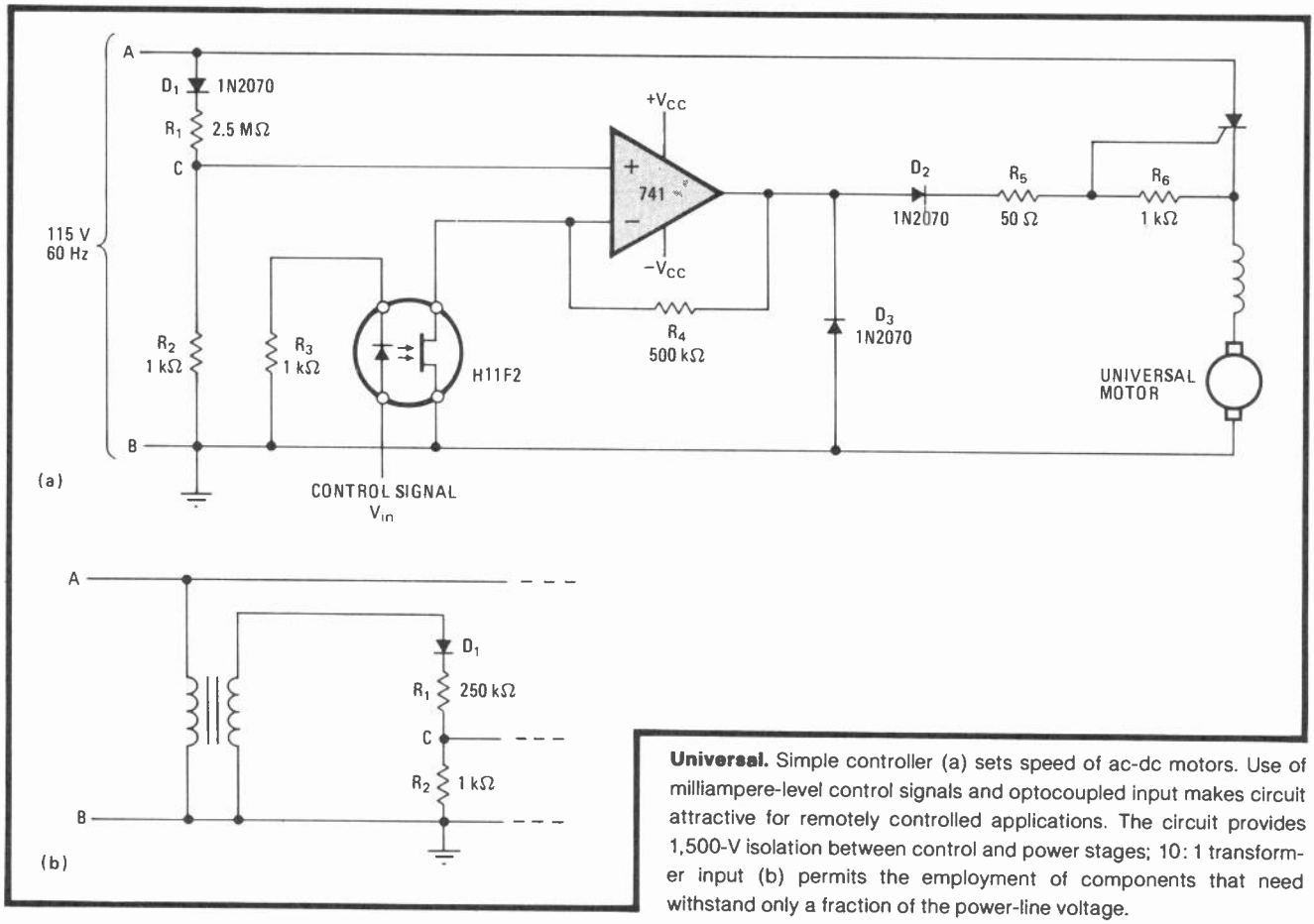
by Hari Herscovici
Cordis Corp., Miami, Fla.

The speed of an ac-dc motor is easily set with this circuit. Millivolt-level input voltages drive its variable-speed control amplifier through an optocoupler that is isolated from the rest of the circuit to permit its use in remotely controlled applications.

Control signals in the range of 0 to 3 volts are applied to the optoisolator (GE H11F2) as shown (a). The resistance between the drain and source of the device's field-effect transistor varies with input voltage V_{in}, and so the gain of the 741 operational amplifier, which amplifies the rectified 60-hertz power-line input, is controlled accordingly.

When the instantaneous output of the op amp is greater than the motor's counter electromotive-force voltage, diode D_2 conducts and thus the silicon controlled rectifier is switched on. Power is thereby applied to the motor. The greater the difference between the op amp's output and the counter emf voltage at any instant, which indicates motor speed is lower than programmed, the earlier in the cycle the trigger pulse to the SCR occurs.

Diode D_1 and resistors R_1 and R_2 have been selected so that the circuit will withstand a reverse voltage of 200 V. If a transformer-based input circuit (b) is substituted, however, it is only necessary for D_1 to have a reverse-breakdown value of 20 V. □



Universal. Simple controller (a) sets speed of ac-dc motors. Use of milliampere-level control signals and optocoupled input makes circuit attractive for remotely controlled applications. The circuit provides 1,500-V isolation between control and power stages; 10:1 transformer input (b) permits the employment of components that need withstand only a fraction of the power-line voltage.

High-voltage regulator is immune to burnout

by Michael Maida
National Semiconductor Corp., Santa Clara, Calif.

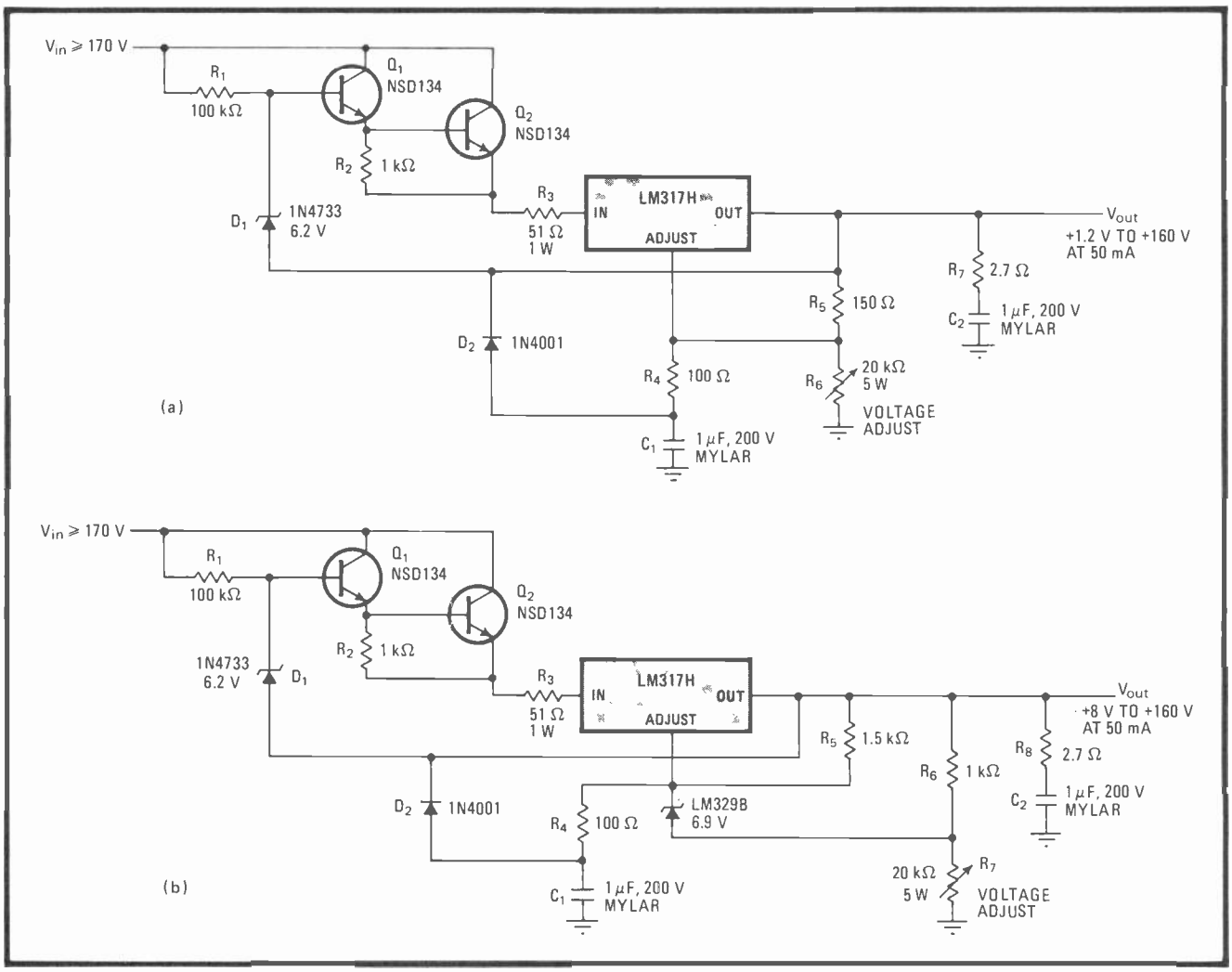
The floating-mode operation of adjustable three-terminal regulators in the LM117 family make them ideal for high-voltage service. Because the regulator sees only the input-output differential—40 volts for the LM117—its voltage rating will not be exceeded for outputs in the hundreds of volts. But the device may break down if the output is shorted unless a circuit can be developed for withstanding the high voltage typically encountered and the output current is limited to a safe value in the event of a dead short.

The circuit surrounding the regulator will serve to solve the problem. Zener diode D_1 maintains a 5-V input output differential over the entire range of output voltages from 1.2 to 160 V. Because high-voltage transistors inherently have a relatively low β, a Darlington arrangement is used to stand off the high input potentials.

The zener diode's impedance will be low, so that no bypass capacitor is required directly at the regulator's input. In fact, no capacitor should be used if the circuit is to survive a short at the output. Resistor R_3 limits the short-circuit current to 100 milliamperes. The RC network at the output improves the circuit's transient response, as does bypassing the adjustment pin. R_4 and D_2 protect the adjustment input from breakdown, if there should be a short circuit at the output.

The approach shown in (b) will serve well in precision regulator applications. Here a LM329B 6.9-V zener reference has been stacked in series with the LM317's internal reference to improve temperature stability and regulation.

These techniques can be employed for higher output voltages and/or currents by either using better high-voltage transistors or cascoded or paralleled transistors. In any event, the output short-circuit current determined by R_2 must be within Q_2's safe area of operations so that secondary breakdown cannot occur. □



Skirting shorts. Three-terminal regulator (a), configured for high-voltage duties as a consequence of operating in the floating mode, is protected by appropriate circuitry against burnout due to shorts. LM329B zener (b) and minor changes improve stability and regulation.

Bipolar current mirror scales, inverts signals

by Henry E. Santana
Hewlett Packard Co., Loveland, Colo.

A pair of operational amplifiers and a few resistors build this precision current mirror. Though simple and low in cost, the circuit excels the usual designs because it not only offers true bipolar operation but also can scale and/or invert any ac or dc input signal.

Input currents are applied to op amp A_1, which is biased by V_{ref}. If I_{in} is generated by a constant current source, V_{ref} may be brought to zero. Otherwise, it should be set to some arbitrary value to maintain circuit bias.

A current-to-voltage converter at the input and a voltage-to-current converter at the output comprise the current mirror. As a consequence of the configuration, the voltage appearing at the output of A will thus be:

$$V_{A1} = V_{ref} + I_{in}R_1$$

for $R_1 >> R_2$ and R_L. The voltage applied to the output circuit is therefore:

$$V_2 - V_1 = I_{in}R_1$$

Writing the nodal equations for V_L, V_3, and V_4 yields these results:

$$I_L = -V_L(1/R_2 + 1/bR_2) + V_3(1/bR_2) + V_2(1/R_2)$$
$$V_3 = A_2(s)\,(V_L - V_4) = (GB/s)(V_L - V_4)$$
$$V_4 = V_1[a/(1+a)] + V_3[1/(1+a)]$$

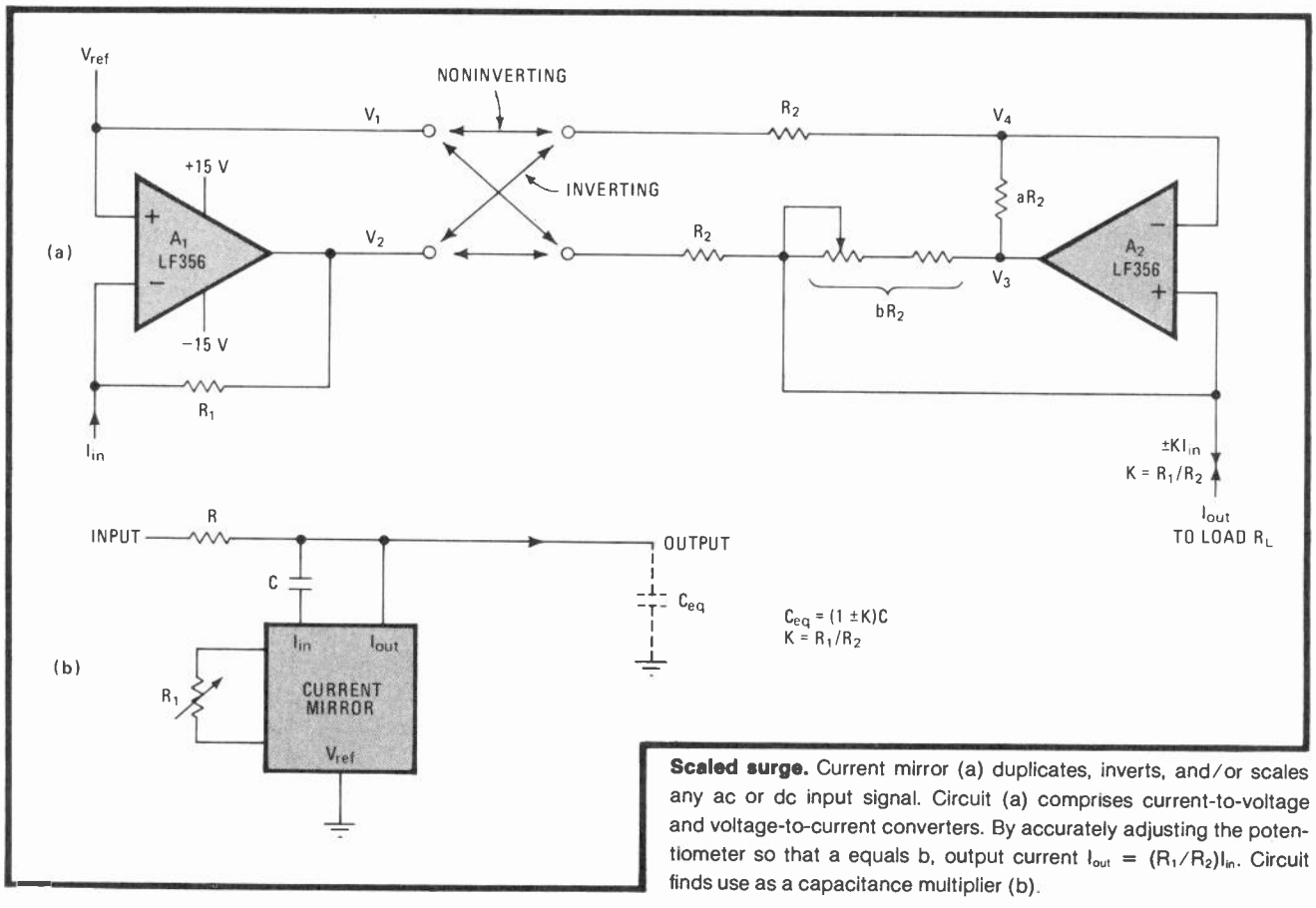
where GB is A_2's gain-bandwidth product. Substituting V_3 and V_4 into the equation for I_L, it is seen that $I_L = (R_1/R_2)I_{in}$, given that $a = b$ and $s << GB/(1+b)$.

The output impedance can be set, within limits, by selection of aR_2 and bR_2. The output impedance is:

$$Z_o(s) = \left[\left(\frac{a}{1+a}\right)\left(S+\frac{GB}{1+b}\right)R_2\right] \div \left[S+\left(\frac{a-b}{1+a}\right)\left(\frac{GB}{1+b}\right)\right]$$

Since a must equal b for the circuit to work, this equation simplifies to $Z_o(s) = [1/(1+a)]\{1 + [1/1+a)]GB/s\}\ R_2$, and no other assumptions about resistor ratios are made.

In addition to its use as a scaled current mirror, the circuit will find other not-so-obvious applications. Such an example is its use as a capacitance multiplier (b). □



Scaled surge. Current mirror (a) duplicates, inverts, and/or scales any ac or dc input signal. Circuit (a) comprises current-to-voltage and voltage-to-current converters. By accurately adjusting the potentiometer so that a equals b, output current $I_{out} = (R_1/R_2)I_{in}$. Circuit finds use as a capacitance multiplier (b).

Digital phase shifter covers 0° to 360° range

by J. W. V. Storey
Dept. of Physics, University of California, Berkeley

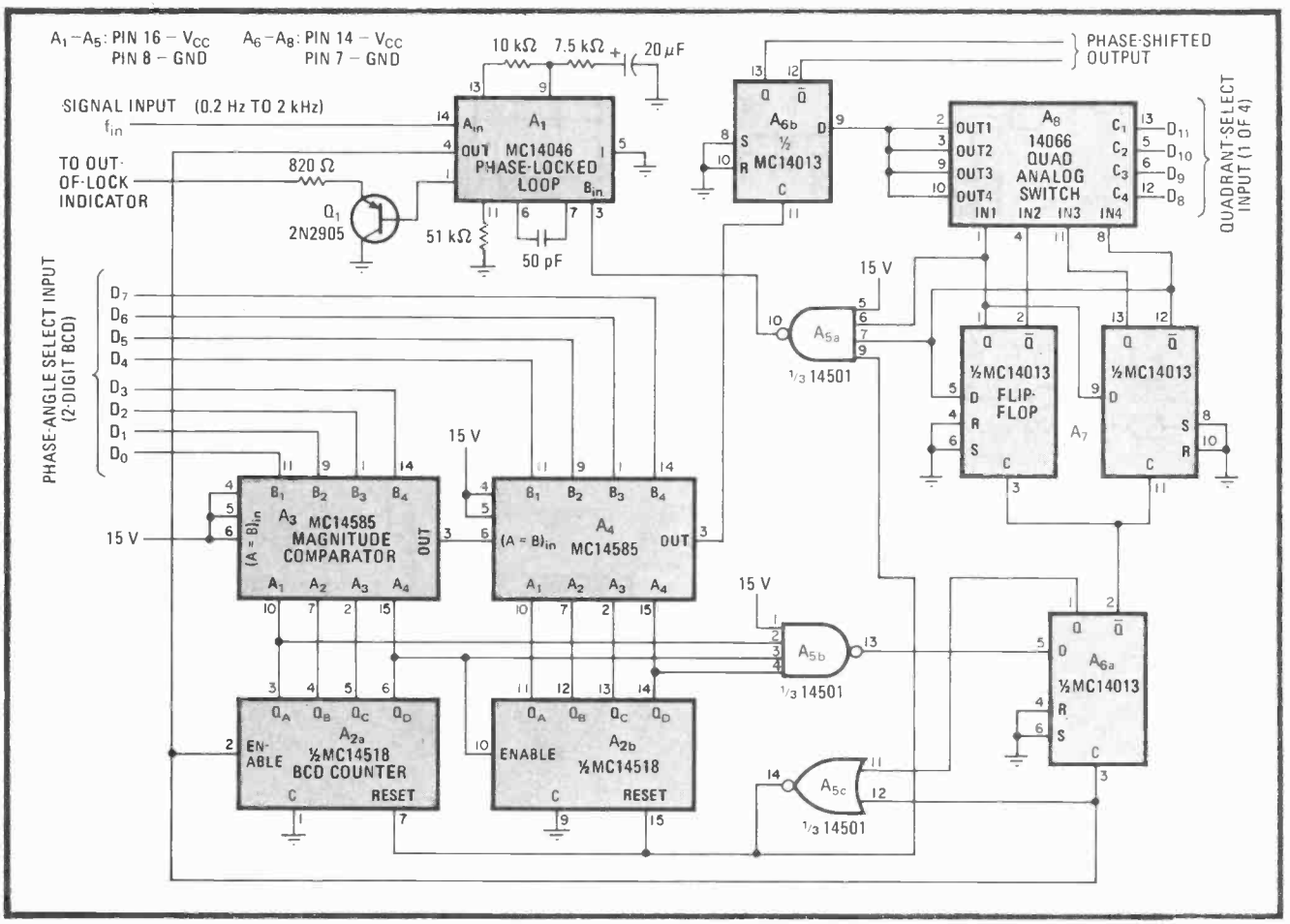
Offsetting the phase of a signal by digital means over the range of 0° to 89° in any quadrant, this low-power circuit is particularly useful in data-recovery systems that employ synchronous detectors. Unlike most RC phase shifters, the value set is independent of the input frequency.

The input reference signal is first introduced to the 14046 phase-locked loop. Its output, which is set to generate a frequency 360 times that of f_{in}, is then applied to the 14518 binary-coded decimal counter, where it is divided by 10. A second, cascaded counter, A_2, divides A_{2a}'s output by 9, the 89th count of a 90-step cycle being detected by A_{5b}. A_2 is then reset to zero on the 90th count by A_{6a} and A_{5c}.

The signal at the output of A_{6a} is thus at a frequency equal to $4f_{in}$. Flip-flop A_7 performs a divide-by-four operation on this signal, at the same time generating four quadrature outputs. Meanwhile, A_{5a}, which generates one pulse per cycle of f_{in}, locks the PLL in phase with the zero count of A_2. Note that the operation of this divider chain is unaffected by the setting of the digital input lines.

The desired phase is selected by applying the appropriate digital signals D_0–D_7 in binary-coded decimal form. Thus, the output from A_3 and A_4 moves high when A_2 counts to that number and clocks flip-flop A_{6b}. This action occurs four times per each cycle of f_{in}. The appropriate quadrant, available at A_7, is selected by digital inputs D_8–D_{11}, the active quadrant corresponding to which one of the lines is high. Flip-flop A_{6b} thus produces a symmetrical square wave at f_{in} having a phase shift equal to the number of degrees specified plus 0°, 90°, 180°, or 270°. There is an additional phase shift of 0.5° at all settings because of the way the PLL is operated to achieve lock. The error can be eliminated by adding an inverter between the output of A_{5a} and the B input of A_1.

With the component values shown and a 15-volt supply, the circuit will operate over the range of 0.2 hertz to 2 kilohertz. Thumbwheel switches with 1-megohm pull-down resistors are used to set the phase-angle input lines. A four-position switch can be used to select the quadrant. With slight modification, the circuit will find application as a digitally controlled ignition timing system for internal-combustion engines. □



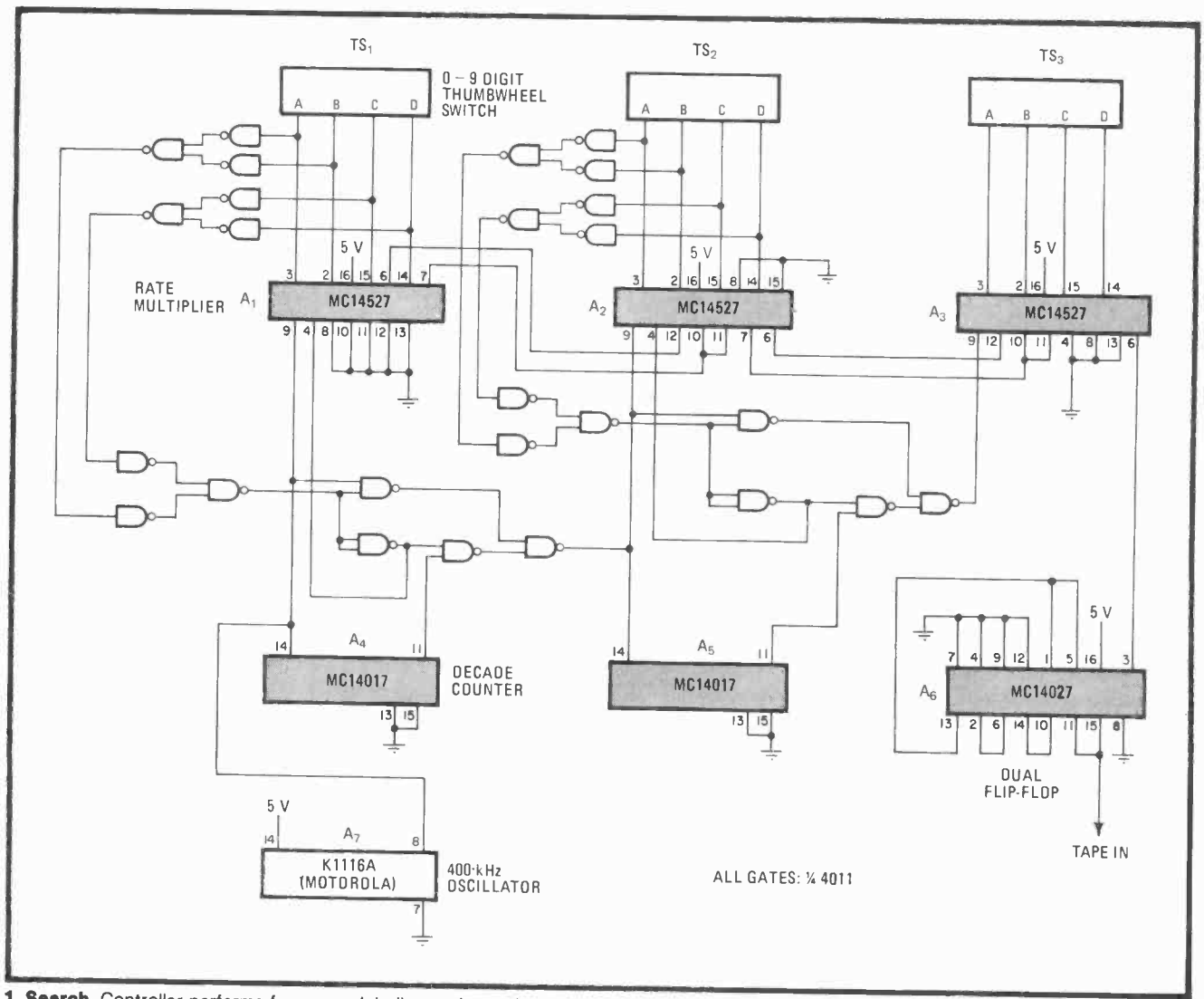
Discrete degrees. Circuit sets 0° to 360° phase shift of reference signal by digital means. Digital inputs D_0–D_7 determine displacement over 0° to 89° range, D_8–D_{11} set quadrant. Output is thus 0° to 89° signal shifted by an additional 0°, 90°, 180°, or 270°.

Frequency-marking controller indexes tape segments

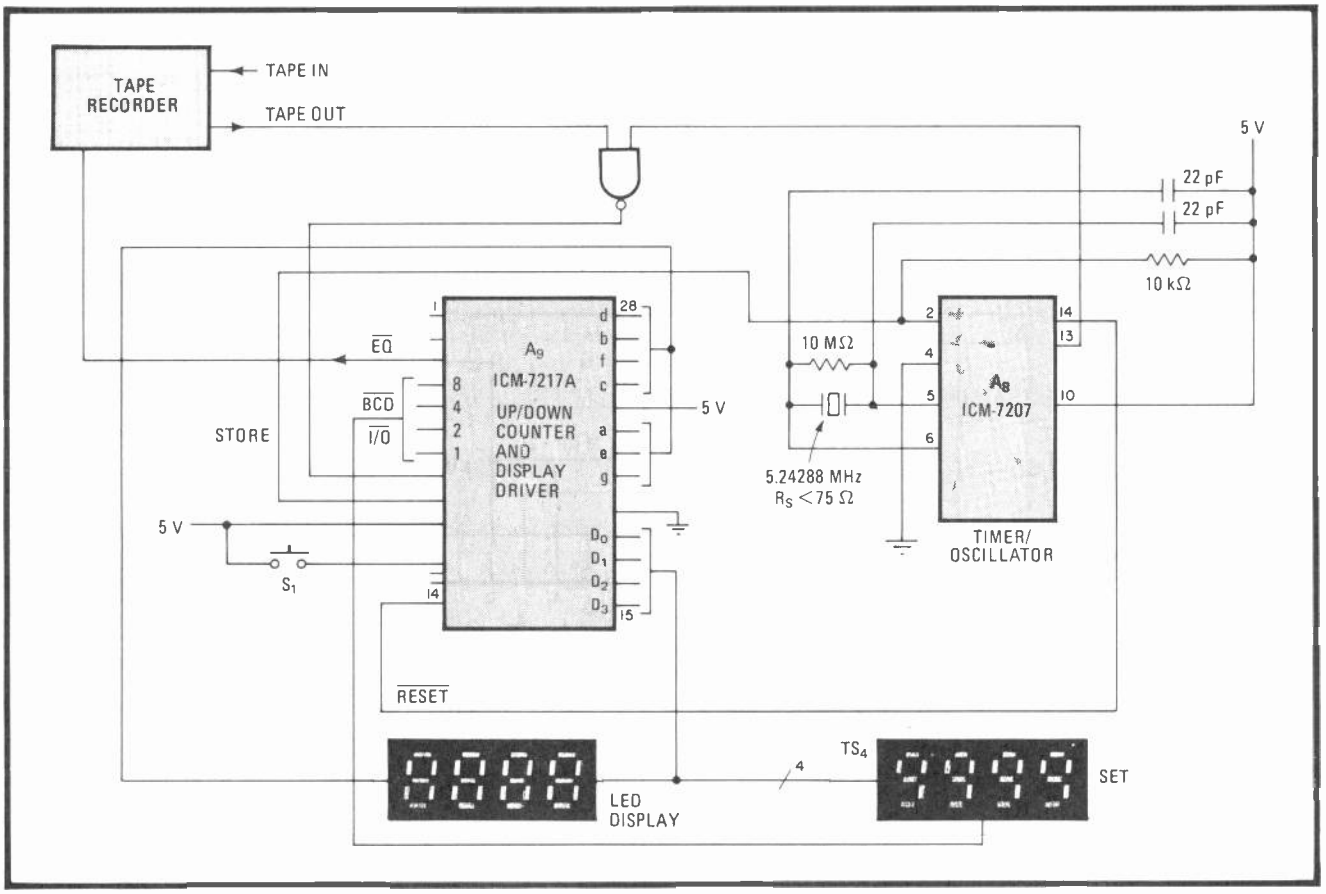
by Joe Lyle and Jerry Titsworth
Bendix Corp., Aircraft Brake and Strut Division, South Bend, Ind.

Tape recorders with footage counters are virtually useless for providing accurate tape markers, mainly because of the slippage created by the electromechanical counter-capstan arrangement generally employed. This controller, which indexes the tape with a frequency-labeling technique during record and stops the recorder at any preselected point during playback, offers the user an easy way to label and isolate any desired segment.

The unit is divided into two subcircuits, for frequency synthesis and for control. In the synthesis portion, thumbwheel switches TS_1–TS_3 are used to set the desired frequency that is to be placed on tape. The 14527 rate multipliers A_1–A_3 and their associated gates multiply the output of the K1116A oscillator by 0.001 to 0.999, thereby delivering frequencies in the range of 400 hertz to 399 kilohertz, in 400-Hz steps, to the input of the divide-by-four flip-flop. Thus, frequencies from 100 Hz to 99.9 kHz (100-Hz steps) are presented to the tape recorder. Because of the audio response of the typical recorder and the limits of the readout circuit used, frequencies of up to 9,900 Hz can be placed on tape. Thus the user may introduce a report number or test number with a frequency burst of selectable duration that directly corresponds to that test (that is, a frequency of 400 Hz will mark the start of test number 400).



1. Search. Controller performs frequency labeling and searching functions to mark, isolate tape segments, respectively. Frequency synthesis portion injects tape markers over range of 100 Hz to 99.9 kHz, in 100-Hz steps.



2. Retrieve. Control portion compares number corresponding to frequency selected to that generated by tape on playback, halts recorder when both are equal. TS_4 sets the test number to be retrieved. LED display provides real-time readout of frequency measured.

The desired test is easily isolated on playback with the aid of the 7217A up-down counter/display driver, which is located in the control portion of the circuit. Thumbwheel switch TS_4 is used to set the test number at which the recorder is to be halted.

Pressing switch S_4 loads the corresponding number into the device's on-board register. As the tape advances during playback, the 7217, which serves as a frequency counter, compares the gated output of the recorder with the number that has been preset. The 7207A provides a 1-second gating time, after which it resets the 7217A's counter to zero. The LED display provides a real-time readout of the frequency measured.

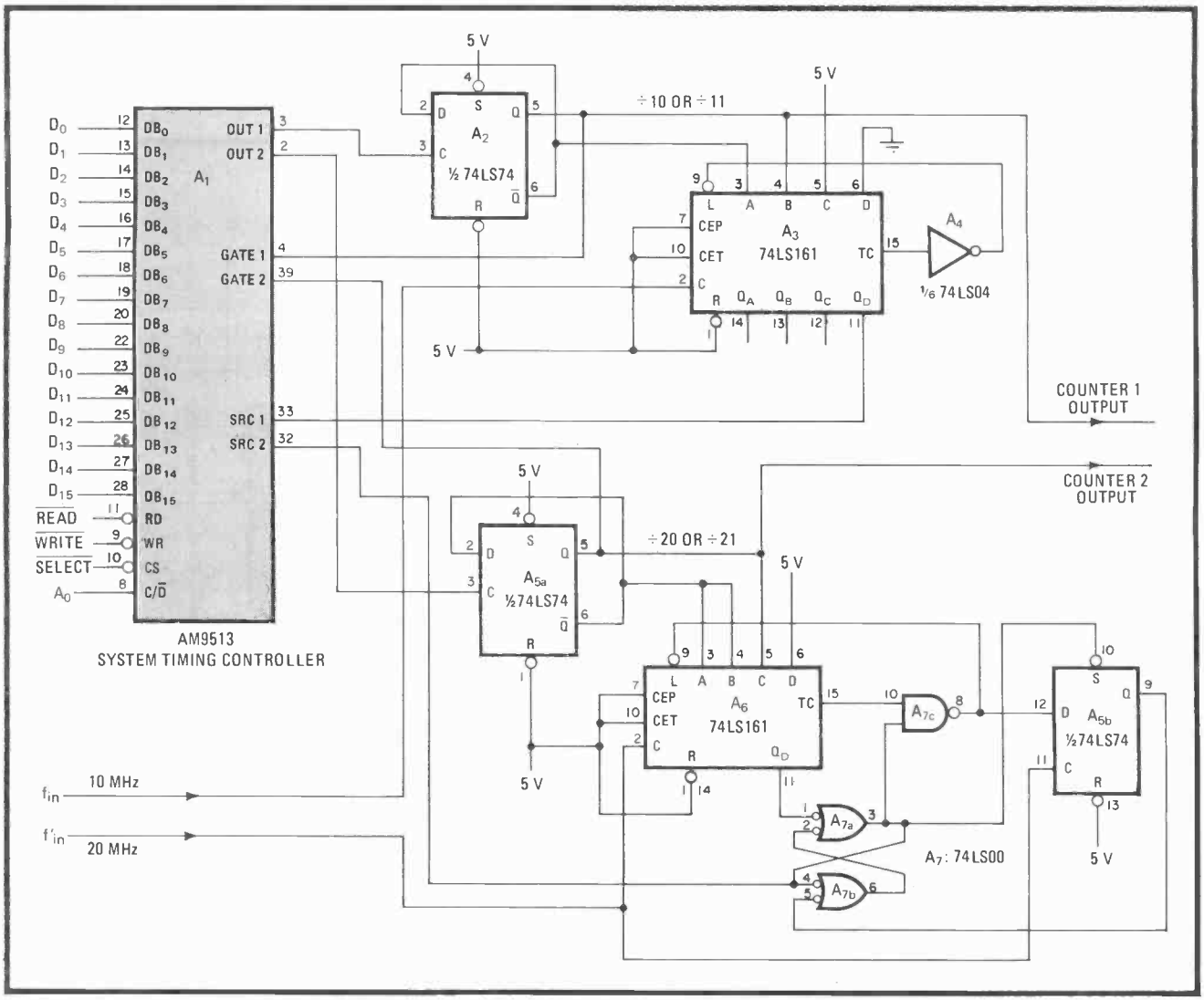
Thus the equal (pin 3) output of the counter moves low if the tone matches the preset number. This signal is used (with appropriate logic) to halt the recorder. □

High-frequency operation with the AM9513 controller

by Terence J. Andrews
Vega Precision Laboratories, Vienna, Va.

The maximum source frequency of the Advanced Micro Devices' AM9513 system timing controller may be extended from 7 MHz to 20 MHz with this circuit. By resolving timing intervals to 50 nanoseconds, the circuit significantly enhances the 9513's usefulness as a multiple programmable frequency divider. The improvement relies on the concept of swallow counting,[1] whereby the controller is made to operate synchronously with an external high-frequency clock. In particular, this circuit illustrates how the controller is configured to provide frequency division at 10 and 20 MHz as an example.

Here, the resolution obtained by either 10- or 20-MHz clocking can be selected as desired. A_2–A_4 achieve operation at 10 MHz. Register 1 of the 9513 is first loaded via its 16-bit data bus with $01F5_{16}$, which instructs the



Resolving divisors. Swallow-counting improves resolution of AMD's 9513 system timing controller, thereby permitting pulse-train division at high frequency. Contents of the controller's load and hold registers set the divisor. Operation at 10 or 20 MHz can be chosen.

device to utilize incoming signals at pin 33 (SRC_1) as its system clock and pin 4 (gate 1) to select either the device's hold or its load register for reloading each of the unit's five 16-bit counters upon receipt of a terminal count.[2] Counter 1 counts down in binary-coded-decimal fashion, with the contents of the load and hold registers determining the divisor.

In this application, only counters 1 and 2 of the device are used. Counter 1 begins to count down from a preset number on the rising edge of SRC_1. SRC_1 in turn is driven by the 10-MHz clock through frequency divider A_3. A_3 is programmed as a 10's complement counter and divides f_{in} by either 10 or 11.

However, counter 1 is loaded with the contents of the load register if Q of toggled flip-flop A_2 (and thus gate 1) is low; otherwise, the contents of the hold register are loaded into counter 1. Thus when counter 1, which holds the contents of the load register, steps down to zero, A_2 orders A_3 to divide by 10; when the counter steps down from a value preset by the hold register, division is by 11. Because in this feedback arrangement there is a change of state at OUT 1 each time the counter reaches 0, it is seen that the contents of both the load and hold registers determine when A_2 is toggled and thereby determine the divisor. Although the numbers loaded into the hold and load registers of the timing controller are in the BCD form, the AM9513 can be programmed to count binary numbers as well.

To determine the divisor, N, multiply the contents of the hold register by 11 and the load register by 10 and add the results. Because the loading of 0001 into either register will cause improper operation, 0011 must be used instead. For example, if division by 301 is desired, the hold register should be loaded with 0011 (not 0001) and the load register with 0018 (not 0029). If 0000 is loaded into either register, a divisor of 10,000 will be the result. □

References

1. The TTL Applications Handbook, "Swallow Counters," Fairchild Camera and Instrument, August 1973.
2. AM9513 Applications Sheet, Advanced Micro Devices, 1979.

Removing residual voltage in dc generator

by C. W. Bray
Memphis State University, Memphis, Tenn.

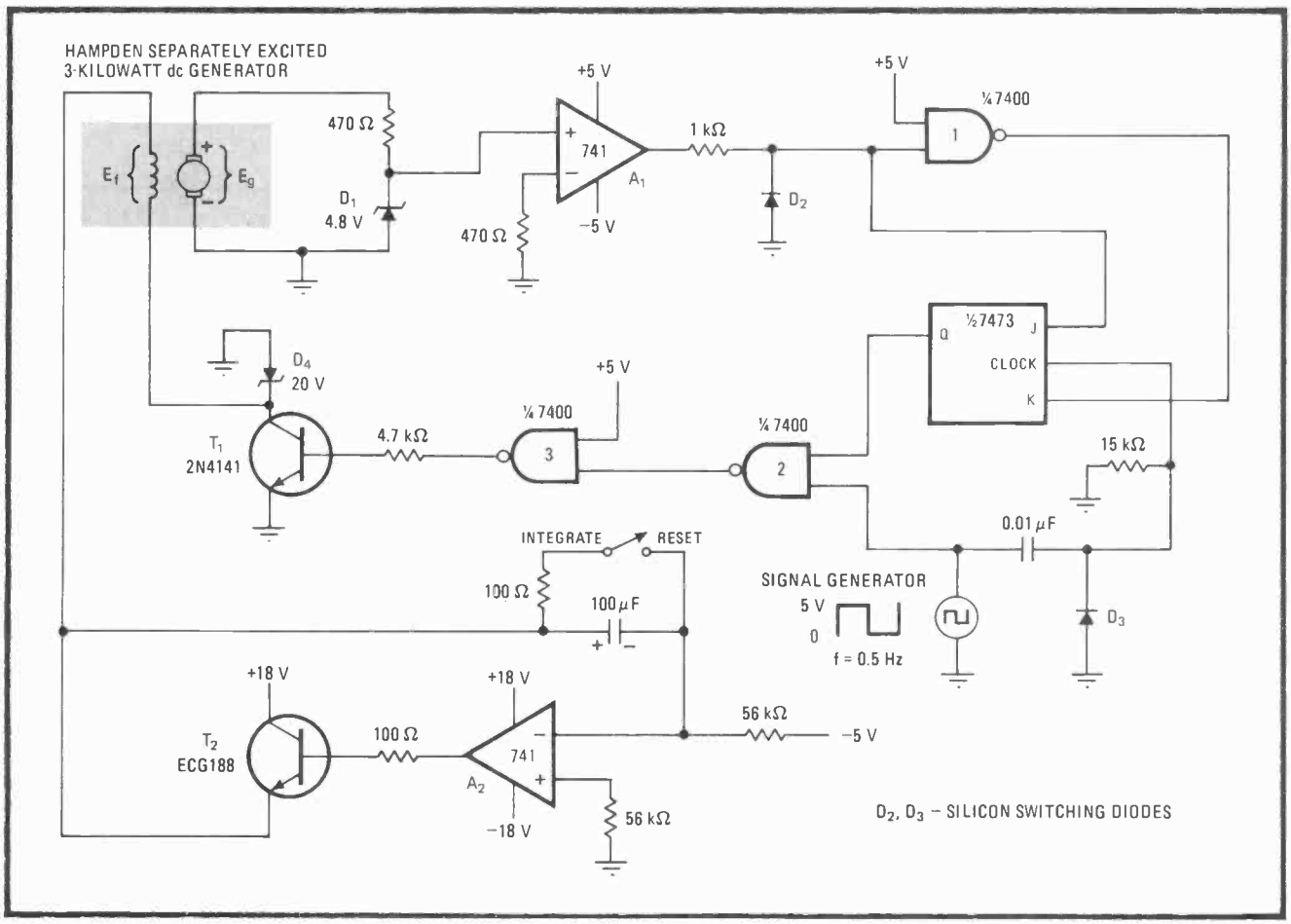
The dc gain (Eg/Ef) of a separately excited generator is an important parameter in its computer model or transfer function. However, direct measurement of this gain is often obscured by residual magnetism in the armature. The magnetism produces an unwanted dc voltage (several volts in a multikilowatt generator) that opposes the normal armature voltage induced by current in the field coil. With the circuitry shown, the output voltage due to residual magnetism can be reduced to a value less than 100 millivolts.

Assume the residual voltage to be canceled has a positive polarity. If the 5-volt square-wave source (shown in the lower right) is low, then gates 2 and 3 hold transistor switch T_1 off. The positive generator output is sensed by the comparator, A_1, which switches to its positive state. This output and its complement are used to set a J-K flip-flop.

When the square-wave voltage goes high, a positive pulse is applied to the clock input of the flip-flop. This drives the Q output of the flip-flop high, which, along with the positive square-wave voltage, turns T_1 on, allowing current to pass through the field winding.

This current causes a voltage opposing the residual voltage to appear across the armature winding. The cycle repeats in synchronism with the square wave's period, until the output of the comparator goes negative (when the average residual voltage is close to zero or negative).

An increasing excitation voltage is provided by the integrator circuit A_2. The time constant selected for the integrator must be long enough so that each increment in field current will be small enough to prevent establishing residual voltage of the opposite polarity. Also, the frequency of the square wave should allow the field current to reach steady state during the time that the field is energized. □



Residual removal. Synchronously switched current through the field coil of a dc generator will create a voltage opposing the machine's unwanted residual output. Transistor, T, is switched on by a positive-going square wave to cancel the undesired voltage.

Moving-dot indicator tracks bipolar signals

by Ted Davis
Riverton, Ill.

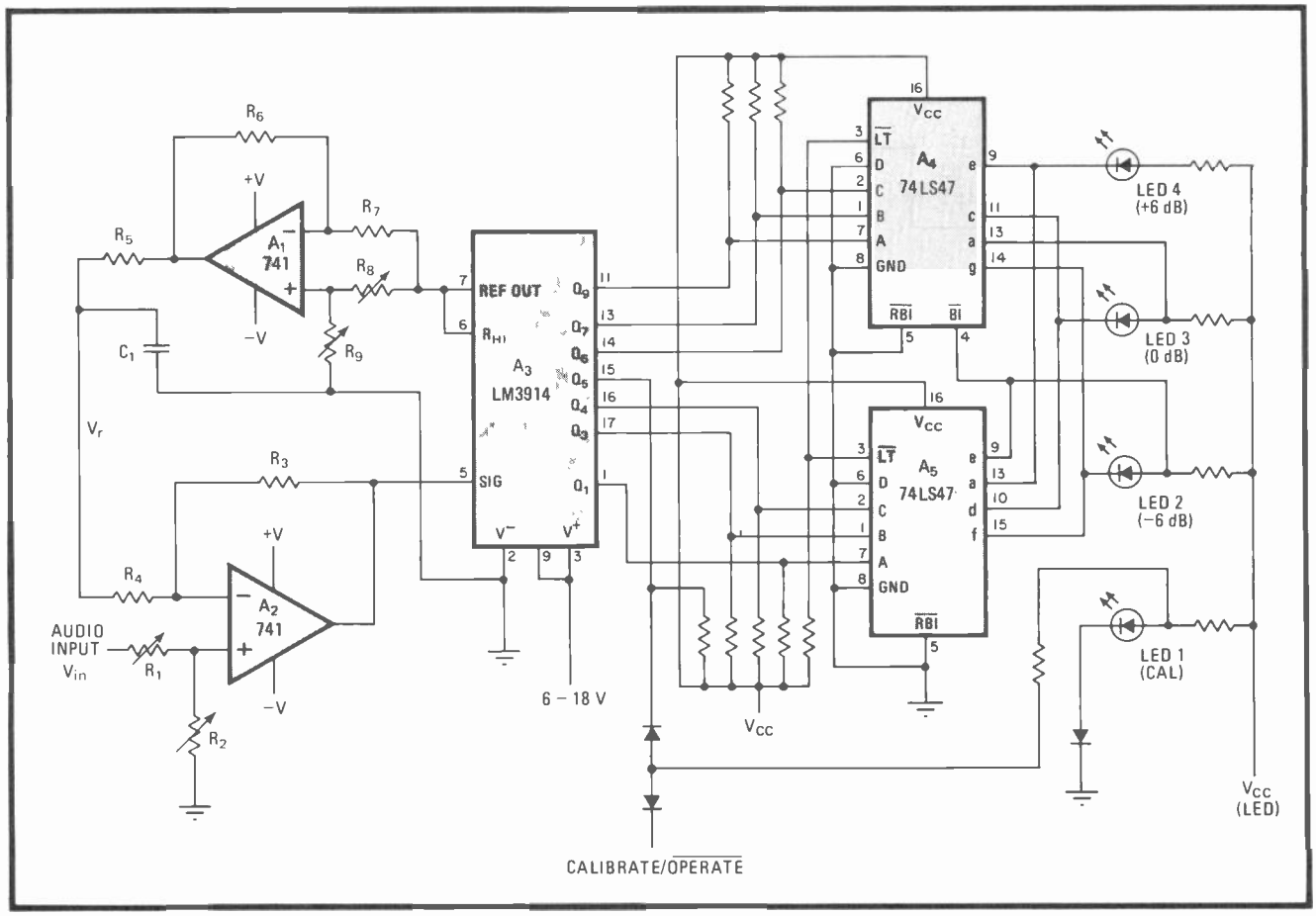
Although bar- or dot-display chips are a simple means of indicating the instantaneous value of a signal, they respond only to unipolar levels, a definite drawback in processing audio-frequency signals with asymmetrical (bipolar) inputs. If reduced resolution is acceptable, one solution is to offset the audio voltage to the display chip. In this way it will be centered at half scale to allow for positive and negative signal excursions. Such a method is implemented in the scheme shown here.

The circuit is configured to detect signal changes in 6-decibel steps, making it useful for audio-level monitoring. Other steps may be ordered by rewiring the output circuit appropriately. The unit may also be used as a bin-sorter or percent-change indicator for ac inputs or, with removal of capacitor C_1 and consolidation of resistors R_4 and R_5, dc inputs.

Operational amplifier A_1 applies a reference voltage to the inverting input of A_2 so that it and the LM3914 bar/dot display may be offset by the desired amount. The value of the reference voltage, which is derived from the LM3914, is $V_r = 1.25[-2R_9/(R_8+R_9)+1]$ assuming that $R_6 = R_7$ and the reactance of C_1 is negligible. The offset signal thus applied to the signal input (pin 5) of the LM3914 is V_rk, where $k = R_3/R_4$.

Assuming also that $R_5 = R_3 - R_4$, the offset voltage can be made to vary linearly from -1.25k to $+1.25$k and be centered at any value simply by adjusting R_8 and R_9. To set the value at the mid-level digital output of the LM3914 dot or bar display, for example, R_8 and/or R_9 is varied so that Q_5 trips and, through the 74LS47 BCD-to-seven-segment decoder/driver, dims light-emitting diode 1. The user should then back off on the setting until Q_5 goes high again and then move the corresponding potentiometer halfway towards the position that would dim the LED once more.

Superimposed on the reference signal will be the component added by the audio signal, which at the



Plus and minus. Input of bar- or dot-display chip LM3914 is biased at user-set dc level so that it will respond to bipolar excursions of ac signals. Three LEDs serve as moving-dot indicator with a resolution of 6 dB. Truth table outlines circuit operation.

TRUTH TABLE: SIGNAL-LEVEL INDICATOR

INPUT V_{in}	A_4										A_5										LED			
	D	C	B	A	$\overline{RBI}$	$\overline{BI}$	a	c	e	g	D	C	B	A	$\overline{RBI}$	a	d	e	f		2	3	4	
below 10%	0	1	1	1	1	1	0	0	1	1	0	1	1	1	0	0	1	1	1				λ	(+6 dB)
10% to 20%	X	X	X	X	X	0	1	1	1	1	0	1	1	0	0	1	0	0	0			λ		(0 dB)
20% to 40%	0	1	1	1	1	1	0	0	1	1	0	1	0	0	0	1	1	1	0		λ			(−6 dB)
40% to 60%	0	1	1	1	1	1	0	0	1	1	0	0	0	0	0	1	1	1	1		ALL OFF			(underrange)
60% to 70%	0	0	1	1	1	1	0	0	1	0	0	0	0	0	0	1	1	1	1		λ			(−6 dB)
70% to 90%	0	0	0	1	1	1	1	0	1	1	0	0	0	0	0	1	1	1	1			λ		(0 dB)
above 90%	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	1	1	1	1				λ	(+6 dB)

X = don't care Input voltage V_{in} normalized to full scale at pin 5 of LM3914

output of A_2 is equal to $V_{in}R_2(k+1)/(R_1+R_2)$. Thus positive and negative excursions of the ac signal will be detected by the LM3914. The scale factor is adjusted by applying the user-standard audio level to the input and adjusting R_1 and/or R_2 until the 0-dB LED just lights up.

The truth table outlines the overall operation of the circuit as a function of signal level. Note that the e segment of the low-order 6 shunts LED 2 in order to resolve a switching conflict between the 4 and 6 outputs. The 6 is also used to blank the high-order decoder when a negative-going 0-dB level is detected.

The values of the current-limiting and pull-up resistors depend on the logic family utilized; for TTL devices, 1-kΩ components will suffice throughout. Care must be taken to ensure that the voltages developed at the e output satisfy the noise-margin requirements of the BI input of A_4; that is, the total sink current at e must not raise the voltage above the maximum logic 0 level and the drop across LED 2 in series with the sink transistor must exceed the minimum logic 1 level. R_8+R_9, in parallel with R_7, set the sink current of the outputs of the LM3914.

The programmed current must be high enough to saturate the output transistors given the pull-up resistors used. The values of most of the other resistors are determined by the values of R_7 through R_9. The value of C_1 is determined by the value of R_4 and the lowest frequency of V_{in}. □

Low-level modulator sweeps generator over narrow range

by Ralph Tenny
George Goode & Associates, Dallas, Texas

A typical function generator's ability to sweep over a 1000:1 range of frequencies by means of an externally applied 0-to-10-volt modulating signal certainly enhances its usefulness. But sometimes narrow-range sweeps on the order of kilohertz are also needed, to check the response of a precision resonant circuit, for example. The problem is that, in most cases, the unit's front-panel controls cannot provide the required resolution. The one-chip circuit shown here, however, enables the setting of any dc voltage and provides for sweeping the control signal over a minimum of ±0.1% of its value so that modulation of the preset center frequency will yield a proportionally small frequency variation.

Operational amplifier A_1 serves as a 6-V source for biasing the inputs of A_2–A_4 at half the supply voltage, enabling the circuit to operate from a single supply (a). A_2, an integrator, and A_3, a voltage comparator operating with heavy feedback, generate the 100-hertz triangle wave needed to sweep the generator and the x input of the oscilloscope used to display the response of the circuit under test. A_4 is a simplified Howland Pump[1], or bilateral current generator, which takes part of the sweep signal and uses it to modulate the preset dc voltage that drives the function generator.

When switch S_1 is placed in the manual position and R_3's arm is positioned at its extreme end (toward R_2), the signal at the modulation output is dc, its amplitude determined by the setting of potentiometer R_2. R_2 is thus used to set the center frequency of the function generator.

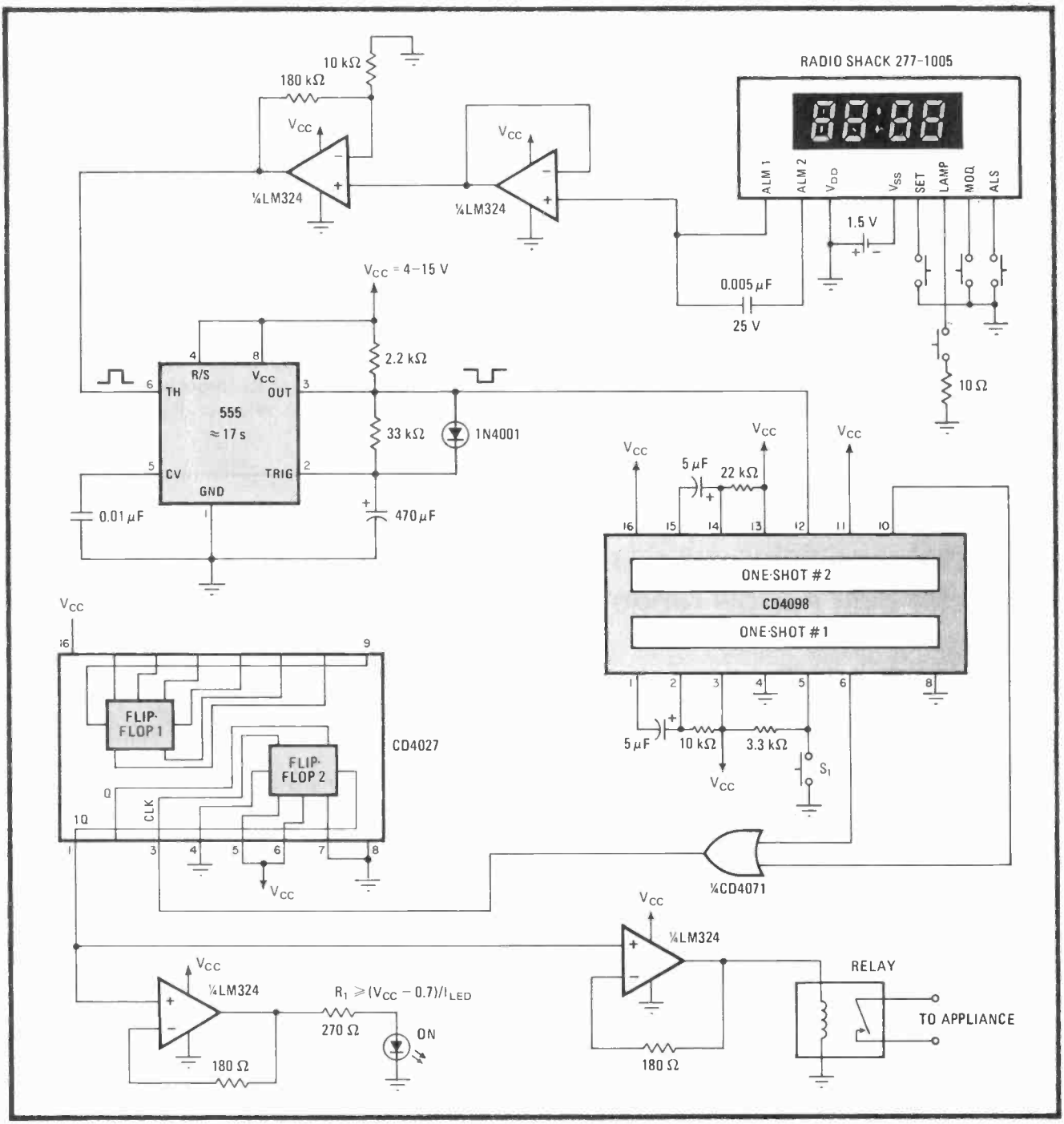
The dc value is modulated by placing S_1 in the sweep position and adjusting R_3 for the desired frequency sweep. Note that R_3 approximates a summing junction for the preset dc level and a fraction of the sweep voltage in this application.

The setup in (b) illustrates a typical application for the circuit, whereupon it is necessary to characterize the response of a quartz crystal that has resonant and antiresonant frequencies less than 3 kHz apart. The frequency counter should be driven by the trigger output of the function generator to avoid interference with the crystal drive. The function generator's output is isolated from the crystal by a large resistor. A low-capacity oscilloscope probe should be used, and the effect of the probe's capacity on the measured crystal frequency taken into consideration. A manual control switch allows the operator to measure the resonant and antiresonant frequencies

by pressing the momentary-contact switch connected to the MOD input so that the hour digits flash. The SET switch is then pressed and held momentarily until the desired hour is displayed. The procedure is repeated for the minute display. A similar procedure sets the calendar day and date. Pressing the MOD and SET switch simultaneously starts the clock running.

To set the alarm time, the switch connected to the ALS port must be pressed twice within 3 seconds. The SET switch is then pressed and held until the desired alarm hour appears on the display. Again, ALS is pressed and SET is held for the setting of the minutes. Pressing ALS once more will display the alarm time momentarily, then the display will return to actual time.

When the alarm time equals the actual time, ALM 1 and ALM 2 of the clock module generates a burst of 15 pulses, occurring at 1-s intervals for 15 s. This signal drives the 555 timer, which, configured as a non-retriggerable monostable, generates a 17-s pulse for setting the 4027 JK flip-flop through the dual 4098 one-shot. The flip-flop can then switch the relay on or off, depending on the quiescent state of one-shot 2 of the 4098. Depressing S_1 changes the relay state from active-high to active-low, and vice versa. □



On time. Archer LCD alarm-clock module allows direct and precise setting of time to activate or shut off appliances. Pulsed alarm-signal output, not directly suitable for turning external devices on or off, passes through C-MOS interface so that relay is switched.

Semiconductor thermometer is accurate over wide range

by Larry G. Smeins
Hewlett-Packard Co., Loveland Instrument Division, Loveland, Colo.

Reducing the circuit complexity and simplifying the calibration of thermometers that use the base-emitter drop of a transistor to detect temperature changes, this circuit provides readings accurate to within ±2°C over the range of −40°C to +150°C. Using the low-offset, low-drift characteristics of National's micropower LM-10 operational amplifier and Motorola's MTS-102 temperature sensor, the thermometer will compete with the more expensive platinum-resistance units.

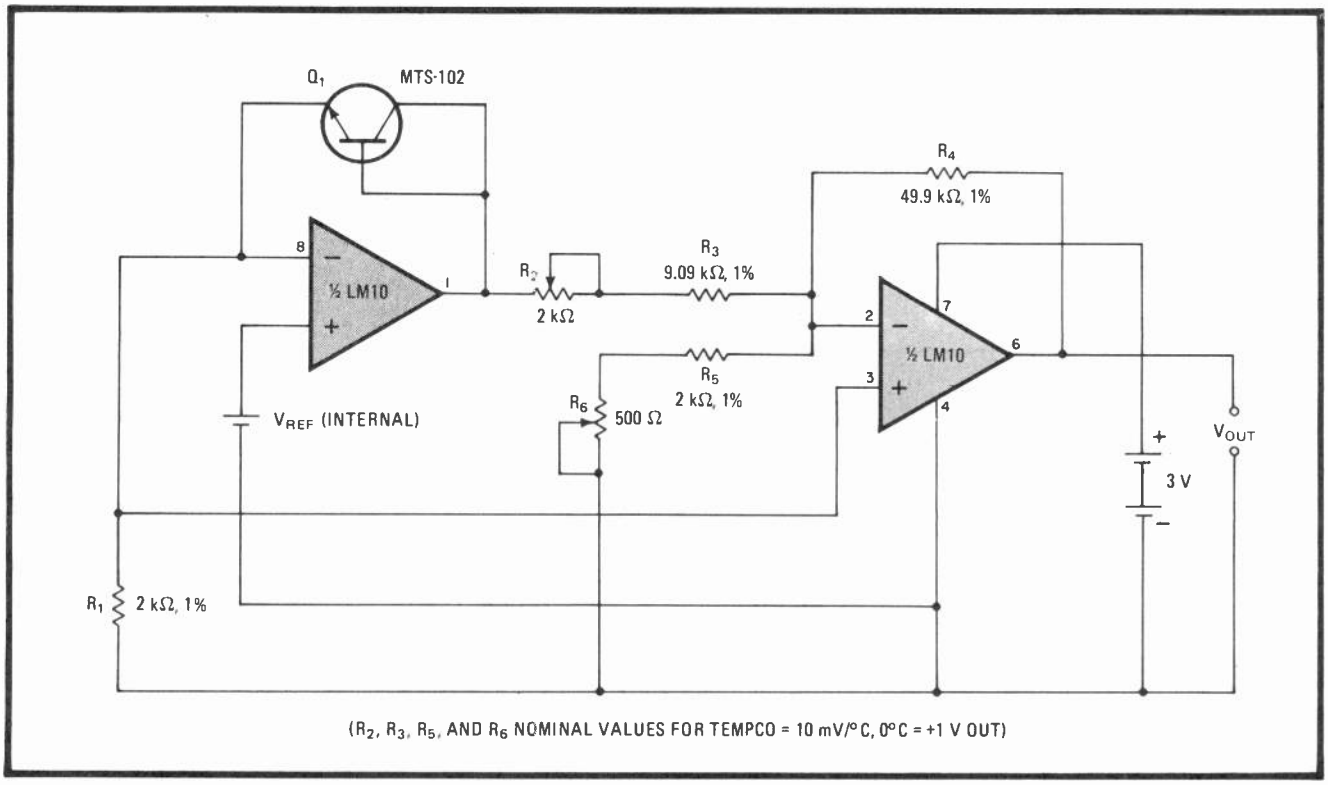
The LM-10 is used to bias, scale, and zero the MTS-102 sensing transistor, thereby removing the need for a separate constant-current bias source for the sensor and an additional scaling and nulling circuit. Further, the well-defined characteristics of the MTS-102 permit single-point calibration of the thermometer.

The MTS-102, Q_1, is placed in the feedback loop of the LM-10 reference amplifier. A constant-current bias is created by V_{ref} across resistor R_1 giving I_{bias} = 0.2 V/2kΩ = 100 μA. The voltage at the output of the reference amplifier will thus be $V_{ref} + V_{be}$. The second stage of the LM-10 is configured to provide a gain that is constant with respect to the temperature coefficient of the V_{be} drop and to subtract V_{ref} and V_{be} from the output at any desired reference temperature.

For a typical MTS-102, the V_{be} is 600 millivolts at 25°C, and its temperature coefficient is −2.25 mV/°C. The actual temperature coefficient for a particular device is thus TC = −2.25 + 0.0033(V_{be}' − 600) mV/C, where V_{be}' is the measured base-emitter drop for the given sensor at 25°C. A corresponding offset voltage therefore appears at the output of A_1.

The gain-controlling elements of A_2, resistors R_2–R_4, can be set so that the circuit's output-voltage-to-temperature slope will be correct for any sensor. The actual gain will be $R_4/(R_2+R_3)$. Once the gain is set, R_5 and R_6 are adjusted to null the offset and yield the desired output voltage at any calibration temperature within the operating range of the circuit.

For very accurate calibration, a reference temperature source should be used to keep Q_1 at 25°C. The V_{be} of Q_1 can then be measured with a digital voltmeter and R_2 and R_3 set to null the offset. R_5 and R_6 are then set to yield an output voltage corresponding to the value that should be measured at 25°C. Using this technique, the calibration will be accurate to within ±1°C.



Hot number. Micropower op amp and semiconductor made specifically for temperature-sensing applications reduce complexity and calibration procedure of thermometers that use V_{be} of transistors to detect temperature changes. Accuracy of device, no worse than ±2°C over the range of −40°C to +150°C, and its simplicity enable it to compete with much more expensive units.

A simpler alternative is to set R_2 and R_3 to correspond with TC associated with the nominal V_{be} of the particular MTS-102 device used, zeroing the circuit at a reference temperature provided by an ice bath. Each MTS device is marked with their respective $V_{be} \pm 2$ mV. This technique will provide calibration accuracy to ± 2°C. Either technique will provide accuracy to 4°C for all interchanged devices marked with the same V_{be}. But interchangeability accuracy will vary to a greater degree with the MTS-103 and MTS-105 devices.

The circuit will also work with a conventional silicon transistor, such as a 2N3904, but for calibration purposes, its V_{be} should be measured between at least two points because it is not a specified parameter. The circuit is relatively insensitive to power supply voltage and it will operate satisfactorily over 2-to-40-V range. □

Linear sense amplifier raises sensitivity of touch keyboard

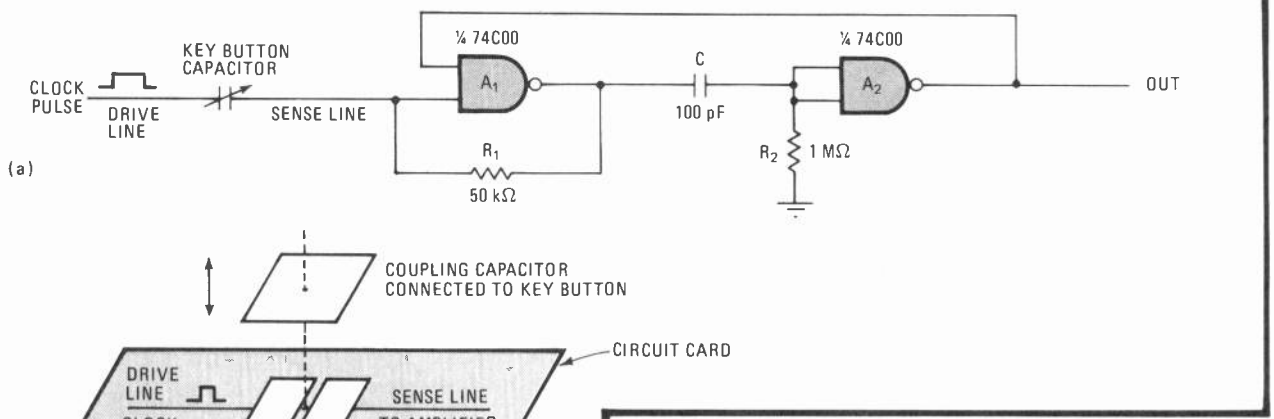
by Jerry Dahl
IBM Corp., Research Triangle Park, Raleigh, N. C.

Keyboards relying on hand capacitance to simulate contact closure require a sense amplifier to detect the capacitive changes and thus determine when a key is depressed. Using one half of a complementary-MOS gate array, where one gate is operated in a linear mode to detect currents as low as 50 microamperes, this sense amplifier is not only simple and inexpensive but sensitive as well.

A_1 of the 74C00 quad NAND gate (a) serves as the amplifier, with A_2 functioning as a latch. A_1 is ac-coupled and operates as a self-biasing current-to-voltage converter with a gain of 50 millivolts/μA. Its open-loop gain falls above 100 kilohertz, so the drive-line clock should have a frequency of about 10 kHz. For higher gain, A_1 can be cascaded with other stages within the feedback loop R_1.

When signals having an amplitude of at least 50 μA are coupled to the sense line via the coupling capacitor connected to the keybutton, A_1 goes high and triggers A_2 for about 70 μs. A_2 operates as a one-shot and thus it does not need to be reset.

The construction of the key module capacitor is shown in (b). The coupling capacitor is connected to the keybutton directly. The circuit-card pads are coated with a thin insulating epoxy covering that serves as the dielectric. When the keybutton is depressed, the clock pulse on the drive line will therefore be coupled to the sense line through the electric field of the capacitor. □



Transfer. Low-cost sense amplifier (a) operates logic gate A_1 as linear current-to-voltage converter to increase sensitivity of touch keyboards. Latch A_2 is a one-shot. Construction of keyboard module capacitor (b) is simple.

Level shifter builds high-voltage op-amp block

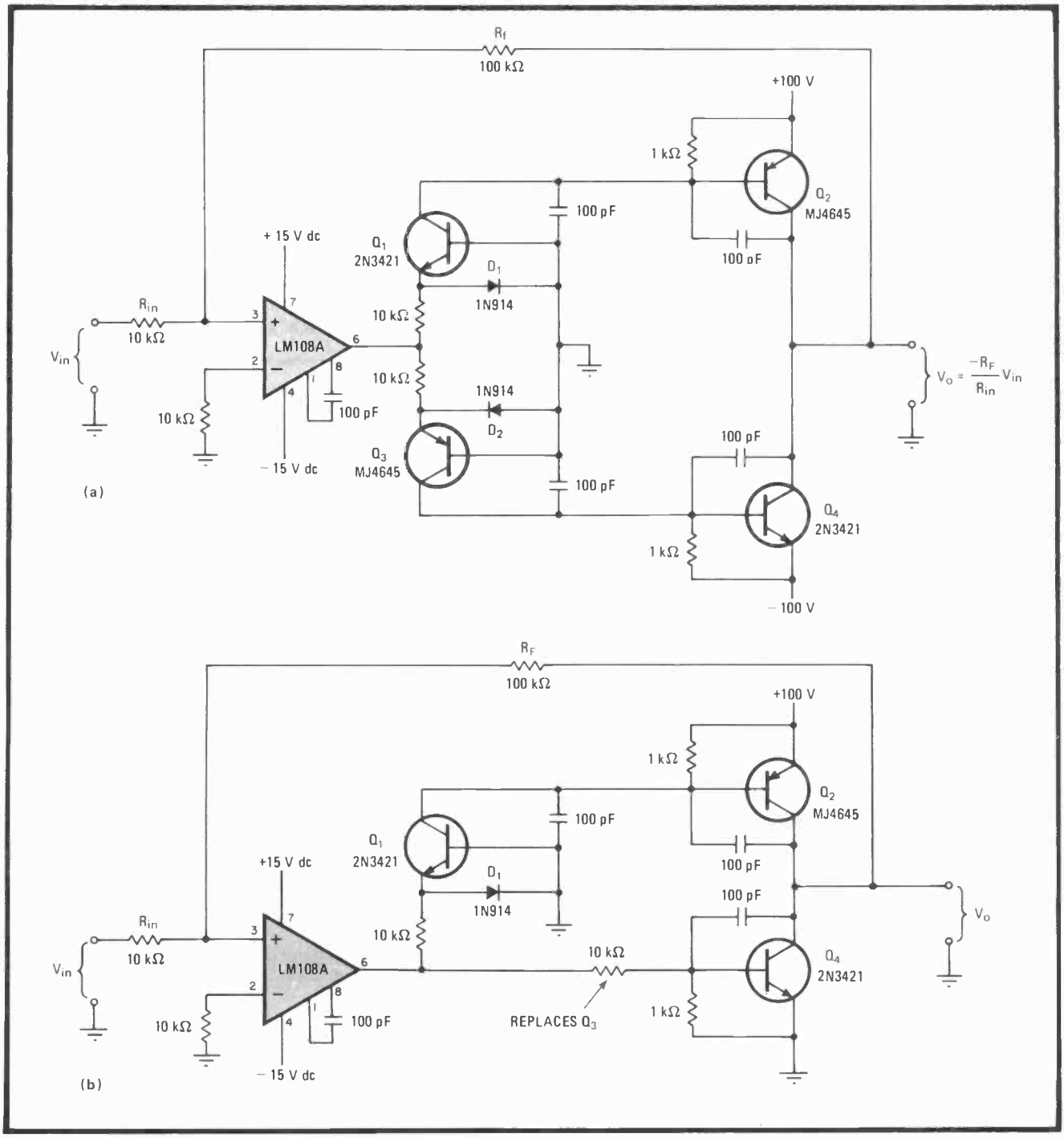
by Leon C. Webb
Ball Corp., Aerospace Systems Division, Boulder, Colo.

Placing a level-shifting network inside the major loop of an operational amplifier adapts it for high-voltage applications. The output swing of the circuit, which can be in the hundreds of volts, is limited only by the breakdown voltage of the active devices (in this case, transistors) used. At the same time, the op amp is isolated from high potentials, even in the absence of its ± 15-volt supply voltages, by the attenuator formed by the amp's gain-

controlling resistor and the input resistance of the circuit and by the clamping action of the circuit's common-base stages.

The method can be applied to op amps that will generate either bipolar or unipolar voltage swings. As shown in (a) for the general voltage amplifier, which generates a bipolar swing, the op amp's output is transformed into an emitter current that flows through either transistor Q_1 or Q_3, depending upon the polarity of the output voltage from the LM108A. As a result, a corresponding base current is applied to either transistor Q_2 or transistor Q_4, respectively, thereby turning it on to a greater or lesser degree. Thus, V_o assumes a value equal to a $-10V_{in}$, where the voltage multiplication holds true for $-10\text{ v} < V_{in} < 10\text{ v}$.

If only a unidirectional output is desired, the configuration shown in (b) will suffice. This circuit, which delivers only positive output voltages, has the same transfer function (that is, $V_{out} = -10\ V_{in}$) for $-10\text{ v} < V_{in} < 0$ v. If a negative-only voltage output is required, stage Q_1 is replaced by a 10-kΩ resistor. The level-shifter's supply voltage must also be negative. □



Translation. Level-shifter adapts operational voltage amplifier (a) for high-voltage duty. Output swing of circuit is limited only by the shifter's supply voltage and the breakdown voltage of transistors used. For unidirectional output swings (b), simplified circuit will suffice.

Converter in feedback loop improves voltage regulation

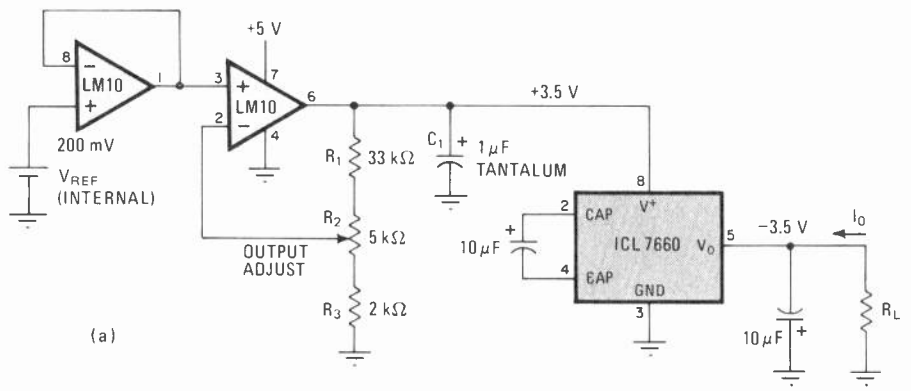
by David Abrams
Winchester, Mass.

One of the most frustrating experiences a designer faces is to discover that his TTL or complementary-MOS circuit, which he intended for single-supply operation, actually requires a minus potential at some miniscule current for one or two of its integrated circuits. A new chip, Intersil's 7660 voltage converter, now enables the designer to obtain the minus voltage at low currents from a positive supply without the need for a transformer or other complicated inverter circuitry, and at low cost. In addition, placing the converter in a feedback loop that includes the chip's power—or driving—source permits a degree of voltage regulation that is not possible with the conventional stand-alone driver configuration.

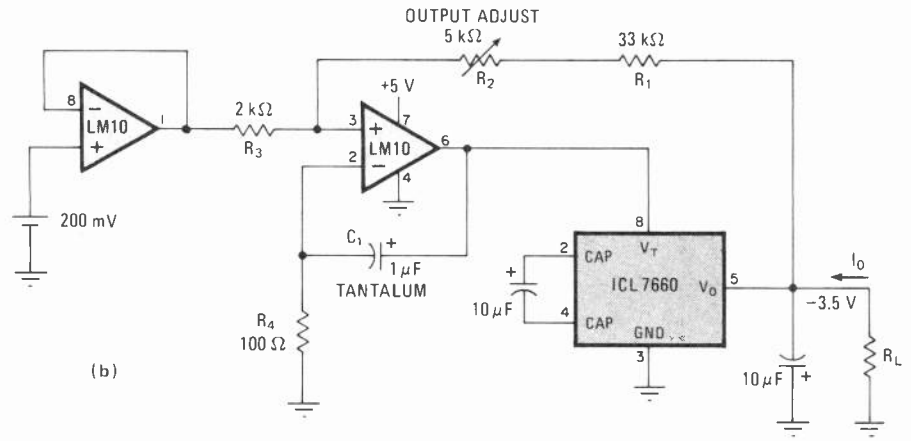
As shown in (a), the 7660 can supply −3.5 volts to a single chip in a C-MOS or TTL system. The chip requires +3.5 V, which is generated by the LM10 operational amplifier from the +5-V supply. Although some other low-voltage op amp and an external reference could be substituted, the LM10 will run off a single supply, has its own reference, and has an output stage that can swing within ½ V of the supply while delivering −20 milliamperes to the 7660.

Though this circuit performs well at very low load currents, its output voltage drops rapidly as load currents increase (see table) because its output impedance is fairly high. At a no-load output voltage of −3.5 V the converter exhibits an output resistance of about 100 ohms, but it will increase 50% for V_{out} = 2 V. This value will render the 7660 useless in systems where more then a few milliamperes are required.

By adding a single resistor and configuring the circuit to the topology in (b), however, the converter can be made to perform much as an ideal voltage source for



R_L (kΩ)	I_O (mA)	V_O
∞	0	3.50
10	0.34	3.45
6.8	0.47	3.37
4.7	0.74	3.36
3.3	1.02	3.34
2.2	1.60	3.30
1.5	2.22	3.26
1.0	2.97	3.20
0.68	4.48	3.08
0.47	6.12	2.94
0.33	8.23	2.73
0.22	10.38	2.48
0.15	13.50	2.06



R_L (kΩ)	I_O (mA)	V_O
∞	0	3.50
4.7	0.76	3.50
3.3	1.06	3.50
1.5	2.35	3.50
1.0	3.20	3.50
0.68	5.06	3.52
0.47	7.02	3.42
0.33	9.38	3.19
0.22	12.13	3.02
0.15	17.42	2.81

Regulatory loop. Intersil's 7660 voltage inverter provides a negative output from a positive source without transformers (a), but voltage regulation is poor. Placing the 7660 in a feedback loop that includes the driving source (b) improves operation markedly.

loads of 1 kilohm or greater. The regulation for loads less than 1 kΩ will be much superior to that in (a), as seen in the table.

Here the circuit works as an inverting amplifier with a gain of -17.5, which is set by $(R_1+R_2)/R_3$. The converter provides a gain of -1, requiring that the noninverting input of the op amp be used as the summing junction. Thus the circuit can still be run from a single supply because the LM10's input common-mode range includes the negative supply (ground, in this case).

R_4 and C_1 provide local feedback around the op amp to stabilize the loop. Without these components, the delay between input and output voltage changes of the 7660 would cause the output of the LM10 to oscillate between ground and +5 V.

In operation, the feedback loop will force the op amp to try to hold the negative output voltage constant. Even at the higher currents, the output resistance is half of what it is in (a).

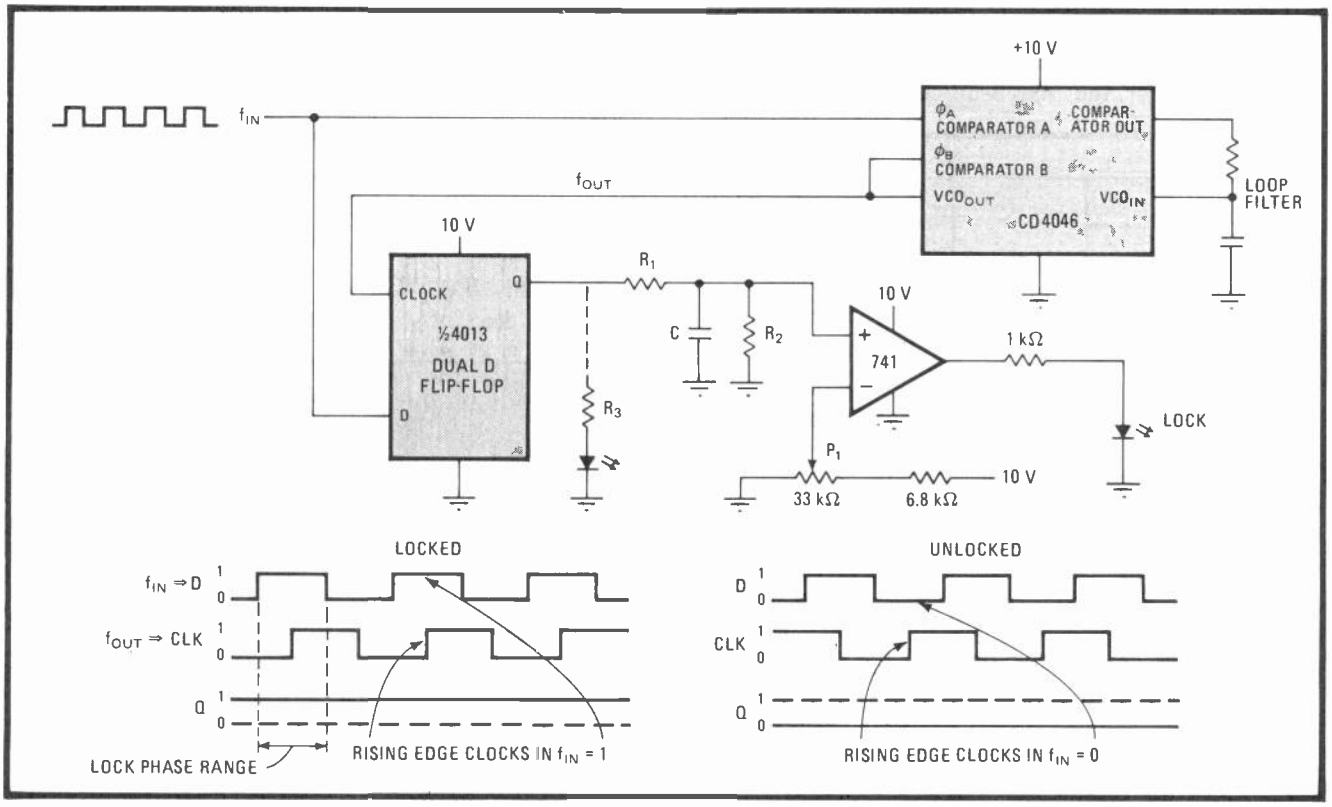
The circuit may also be used to supply negative voltages other than −3.5 V. If higher voltages are desired, it is necessary to choose a supply voltage for the LM10 that will provide sufficient output from the op amp under the expected load conditions. In this case, the effective voltage gain of the 7660 drops from −0.99 V to zero, and so the output voltage of the op amp must rise as the load current increases in order to compensate for the loss of gain. □

PLL's lock indicator detects latching simply

by Steve Kirby
Department of Electronics, University of York, England

Much less complex than some of the previously described lock indicators for phase-locked loops,[1] with no need to derive and utilize a multiple of the input frequency[2] for phase-comparison purposes, this circuit is easier to set up and use. It sacrifices nothing in the way of accuracy and offers other advantages, such as the ability to lock onto harmonics of the input signal.

The locking technique is illustrated for the C-MOS CD4046 PLL, whose output leads the input by 90° when the lock state is achieved. The loop's capture ratio is such that lock can be maintained for a square-wave input signal no greater than +90° and no less than −90° out of phase with respect to f_{out}. The 4013 D flip-flop detects phase differences by clocking the state of f_{in} at f_{out}'s rising edge. Assuming the PLL and its associated loop filter are working properly, a steady Q = 1 at the output of the flip-flop indicates the PLL is in or will shortly be in the lock state. The noninverting input of the 741 comparator will then rise to 10 volts through integrator



Monitor. Only two chips, flip-flop and comparator, are needed to detect lock condition in phase-locked loop. Rising edge of f_{out} clocks in logic 1s to D input of flip-flop under lock condition, causing A_1 to go high and LED to light. Output of flip-flop is otherwise a random train of pulses, causing the voltage at the noninverting input of A_1 to drop below P_1's threshold, bringing A_1 low and turning off the LED.

R_1R_2C, and its resulting high-going output will light the light-emitting diode.

If the PLL no longer locks on frequency, the phase of f_{in} with respect to f_{out} will be random. The output of the flip-flop will thus be a train of variable-width pulses. The comparator input thus drops to approximately 5 V, and because potentiometer P_1 sets the inverting input at approximately 7 V, A_1 moves low, extinguishing the LED.

The lock detector will lock onto higher harmonics of f_{in}. With a 50/50 mark-to-space square-wave signal, locking has been observed to the fifth harmonic.

If a less precise indication is tolerable, lock detection can be achieved with even fewer parts by placing an LED at the output of the flip-flop and eliminating the comparator circuitry. Resistor R_3 should be selected to hold the LED dim for the out-of-lock condition. □

References

1. J. A. Connelly and G. E. Prescott, "Phase-locked loop includes lock indicator," *Electronics*, Sept. 5, 1974, p. 112.
2. R. P. Leck, "Logic gates and LED indicate phase lock," *Electronics*, May 29, 1975, p. 106.

Three-chip logic analyzer maps four-input truth table

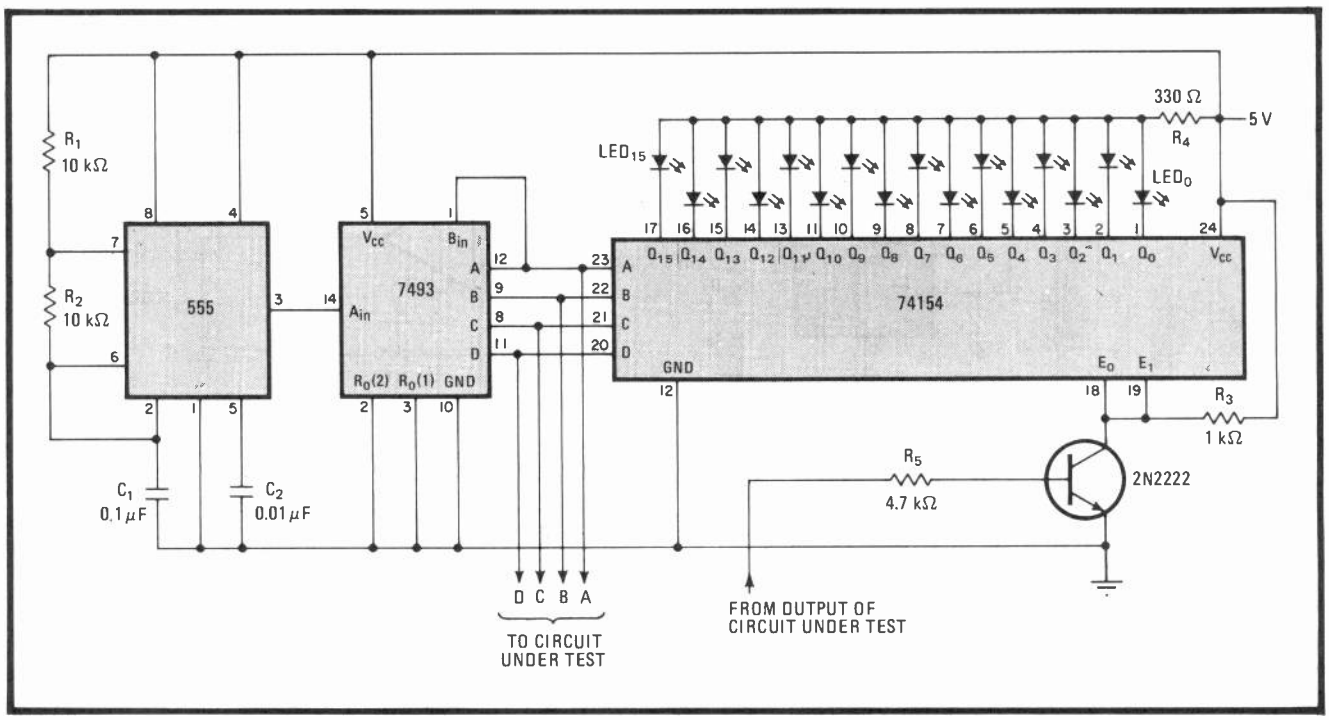
by C. F. Haridge
University of Ottawa, Ontario, Canada

Providing an extremely simple and low-cost alternative to the use of an oscilloscope, this logic analyzer will determine the truth table of circuits with as many as four inputs. The state of the circuit for a single monitored output is displayed by a four-by-four array of light-emitting diodes arranged in a Karnaugh-map configuration. Resistor-, diode-, and transistor-transistor-logic circuits can be checked directly, and only one input/output buffer is required to check complementary-MOS designs.

The analyzer's three basic functions—timing, scanning, and display—are achieved with only three chips: the 555 oscillator, the 7493 4-bit counter, and the 74154 4-to-16-line decoder. The 555, running at a minimum frequency of 480 hertz to eliminate display flicker, clocks the 7493 through its 16 states continuously. As a result, a binary sequence of 0–15 periodically drives the four inputs of the circuit under test. These logic signals are also applied to the decoder chip. Consequently if the instantaneous output of the circuit point under test is high for any given set of input variables A–D, the LED corresponding to the 4-bit output number of the 7493 will light up.

The analyzer may be easily expanded to test circuits having more than four inputs by adding the appropriate number of counters, decoders, and LEDs. The clock frequency must also be increased to minimize flickering in the display.

A higher clock frequency will reduce the on-time of each LED, however. In order to compensate for this reduced brightness, resistor R_4 must be made proportionally smaller. □



Logic functions. Low-cost logic analyzer, complete with light-emitting diodes arranged in Karnaugh-map configuration, monitor four-input circuit response. RTL, DTL and TTL circuits may be checked directly; only one I/O buffer is needed for C-MOS designs.

PSK modulator resolves phase shifts to 22.5°

by Noel Boutin
University of Sherbrooke, Quebec, Canada

Requiring little more hardware than the circuit proposed by Chawdhury and Das[1] and eliminating the software entirely, this phase-shift-keyed modulator offers an even more versatile and less expensive solution to sending binary data over long distances. One of its great advantages is that carrier phase shifts can be resolved to 16 bits—22.5°.

Only three low-cost chips and a means for generating four-input binary data are required, as shown. The carrier signal is first divided by 16 and applied to the CD4015 eight-stage shift register. Because the register is clocked by the carrier at a rate 16 times that of the signal to be shifted, a discrete eight-phase version of the carrier appears at the output of the register, each shifted by 360/16 = 22.5° from its neighboring stage. These signals are then introduced to the CD4051 multiplexer.

The first 3 bits of each of the modulating data inputs, A–D, address the CD4051 also. Thus any desired phase shift from 0° to 157.5° may be selected (see large table). The eight remaining values, from 180° to 337.5°, may be selected with the aid of the D input, which at the output of the last stage of the register inverts the phase of the signals that have already been generated.

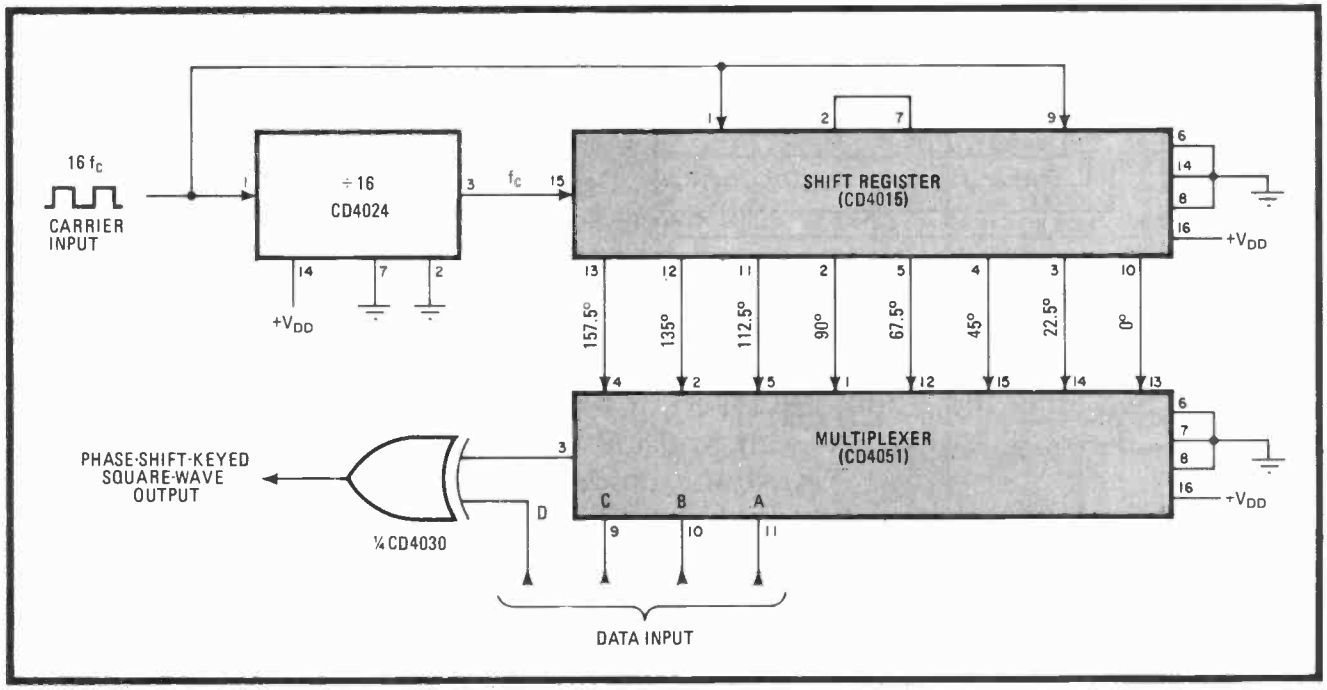
There may be instances where it is desirable to transmit fewer than 16 levels. The small table summarizes the A–D states required to achieve this. □

References
1. F. B. Chawdhury and J. Das, "8085 performs PSK modulation for data-line transmission," *Electronics*, Jan. 31, 1980, p. 108.

DATA				φ
D	C	B	A	
0	0	0	0	0°
0	0	0	1	22.5°
0	0	1	0	45°
0	0	1	1	67.5°
0	1	0	0	90°
0	1	0	1	112.5°
0	1	1	0	135°
0	1	1	1	157.5°
1	0	0	0	180°
1	0	0	1	202.5°
1	0	1	0	225°
1	0	1	1	247.5°
1	1	0	0	270°
1	1	0	1	292.5°
1	1	1	0	315°
1	1	1	1	337.5°

NUMBER OF PHASE LEVELS	A	B	C	D
2 φ	0	0	0	DATA
4 φ	0	0	DATA	DATA
8 φ	0	DATA	DATA	DATA
16 φ	DATA	DATA	DATA	DATA

Multiphase. Three-chip circuit performs PSK modulation on square-wave input, resolving carrier shifts to 22.5°. First three bits of modulating data inputs select shifts from 0° to 157.5°, with D input required for higher values. Truth tables summarize operation.



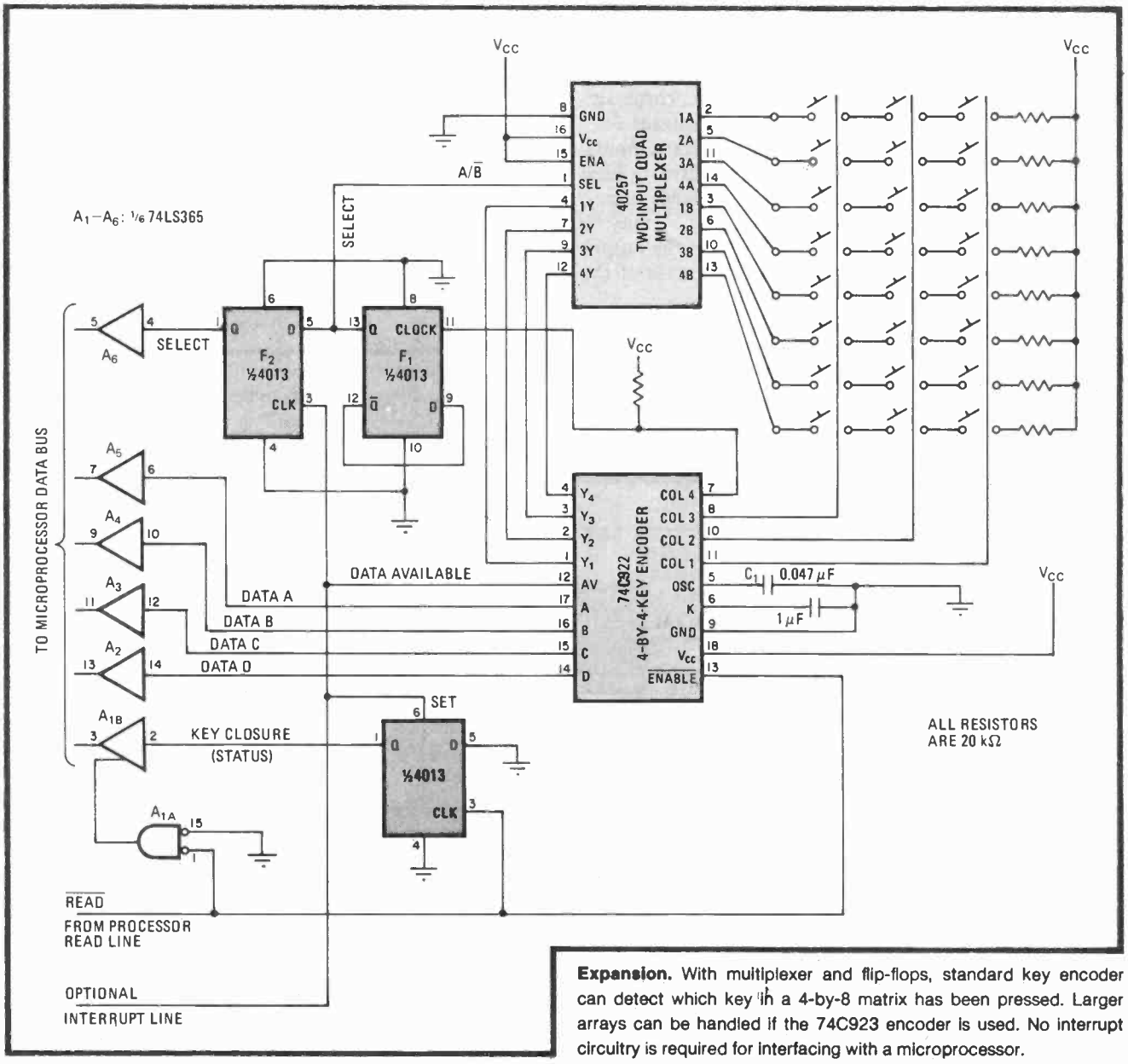
4-by-4 matrix chip encodes larger arrays

by James H. Nixon
Southwest Research Institute, San Antonio, Texas

With this circuit idea, the standard encoder for a 4-by-4–matrix keyboard can be made to handle arrays as large as 4 by 8. In fact, arrays as large as 4 by 10 can be readily accommodated if a 5-by-4-line encoder, such as Motorola's 74C923, is used. Interfacing with a microprocessor is easy and the generation of interrupts is not required.

As seen in the circuit example of a 3-by-8-line encoder, the 74C922 scans keyboard columns 1 through 4 (pins 7, 8, 10, and 11) at a rate set by its internal oscillator components and C_1. Each line is grounded in sequence until a key closure forces one of the row sense lines low, which in turn drives the data-available line high and halts the scanning process until the key is released. Meanwhile the appropriate input of the key encoder corresponding to the key pressed is brought high and the results of the row-column detection appear at the analog-to-digital outputs of the 74C922.

Each time the column 4 line is scanned, pin 7 of the key encoder moves high and clocks the 4013 flip-flop, F_1, causing the complementary-MOS 40257 data selector to switch between rows 1 to 4 and rows 5 to 8. The output from F_2 and A_6 thereby indicates which of the two row sets was accessed. The key closure line indicates if the data has been previously read and thus prevents redundant entries to the processor. □



Expansion. With multiplexer and flip-flops, standard key encoder can detect which key in a 4-by-8 matrix has been pressed. Larger arrays can be handled if the 74C923 encoder is used. No interrupt circuitry is required for interfacing with a microprocessor.

Time-shared analog bus multiplexes audio signals

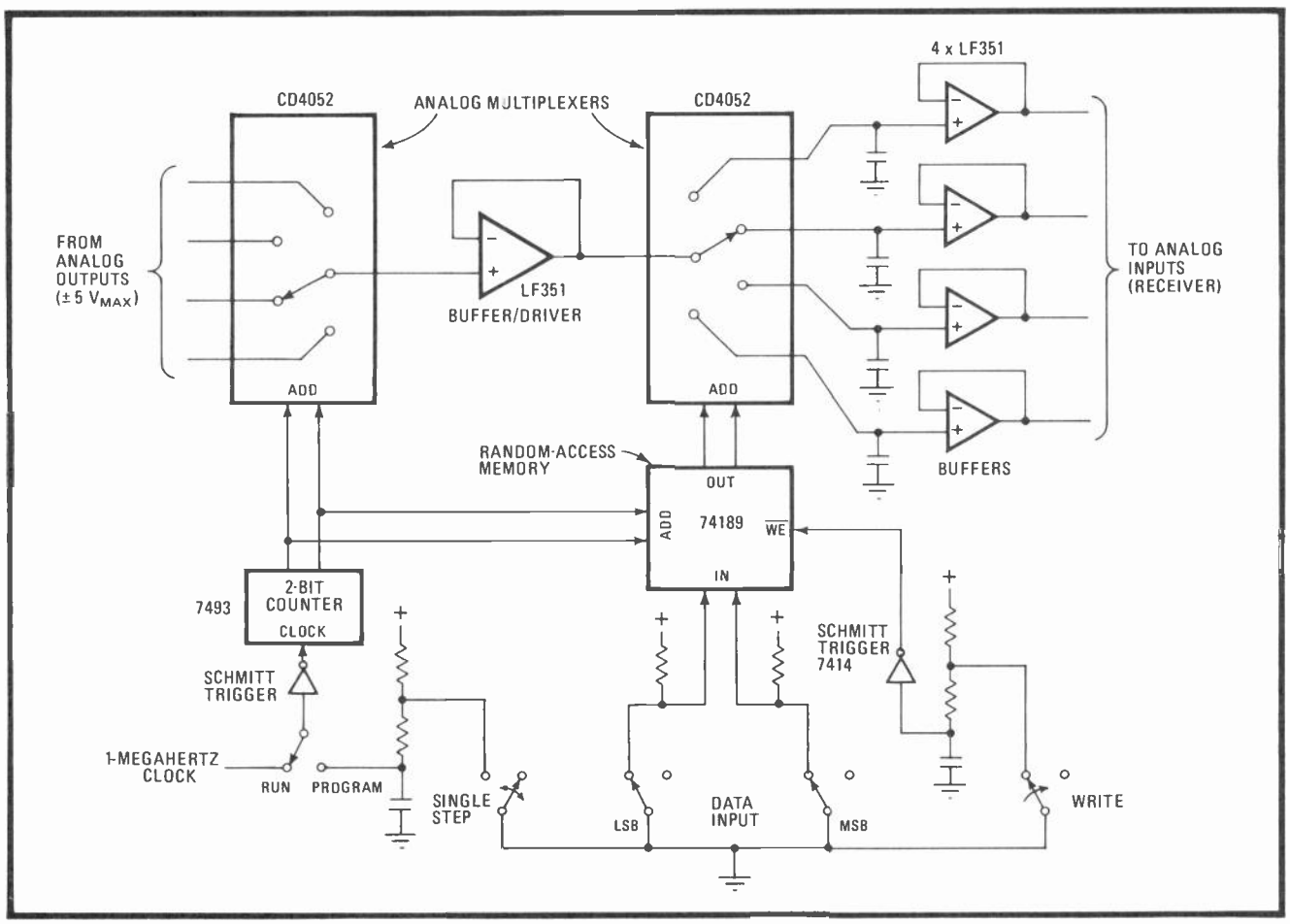
by Colin Johnson
Madison, Wisc.

A multiplexed analog bus can be easily realized by means of complementary-MOS analog switches and rudimentary sample-and-hold circuits. Thus the advantages gained by the time-division multiplexing of digital signals—mainly the multichannel sharing of processing hardware—may be also secured for audio waveforms.

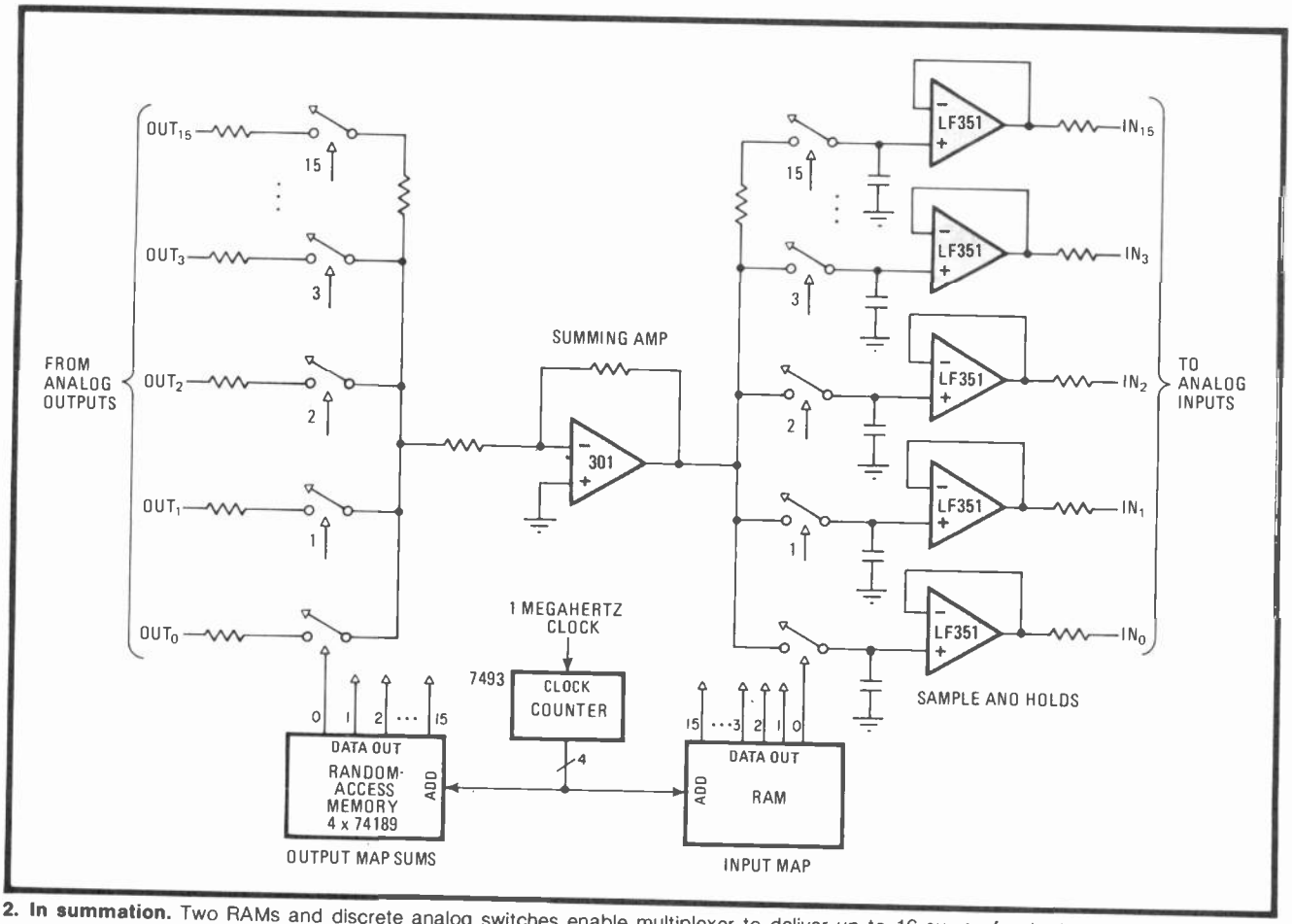
Each analog driver output is connected to the bus through an analog switch. Each analog receiver input is attached to the bus via a simple capacitor/operational-amplifier sample-and-hold stage. As each output is switched onto the bus, the corresponding inputs it is connected to are also engaged. During this aperture time, the hold capacitors are charged. The specific input/output map is stored in a random-access memory. If a computer is available, a memory-mapped scheme lets the user implement changes easily and affords convenient cataloging of any patch on a mass-storage device.

C-MOS analog multiplexers serve as the central switching element in the four-channel multiplexer shown in Fig. 1. These devices are bidirectional and have separate TTL-level address inputs, enabling the switching of analog input signals in the range of ±5 V.

The bus technique is not confined to a four-input multiplexer, of course, and many other configurations can be constructed. Figure 2 shows a design using discrete analog switches and a summing amplifier that mixes 16 unique sums of outputs to any number of 16 inputs. Multiplexing is done at 62.5 kilohertz in this case (47 KHz if an additional 250-nanosecond settling time is permitted). This sampling frequency is sufficient to process audio signals below 20 KHz without significant distortion. When tape recording and other baseband equipment is used, a low-pass filter will be required to eliminate the switching noise that is generated. □



1. Four by four. Analog multiplexers combine four analog signals over a common bus. Counter, driven by 1-MHz clock, sequentially selects analog outputs and sends signals over bus to receiver. RAM containing input/output map delivers signals to required port.



2. In summation. Two RAMs and discrete analog switches enable multiplexer to deliver up to 16 sums of outputs to any number of 16 receiver inputs. Number of sums is proportional to length of RAM. Multiplexing is done at 62.5 kHz to ensure coverage of audio band.

Implementing interrupts for bit-slice processors

by Vern Coleman
Advanced Micro Devices Inc., Sunnyvale, Calif.

Interrupt detection and handling at the microprogram level can be easily implemented in the Am2900 bit-slice processor family thanks to versatile components like the Am2914 priority interrupt encoder and others. The interrupt scheme can generally be extended to other systems at the cost of additional circuitry.

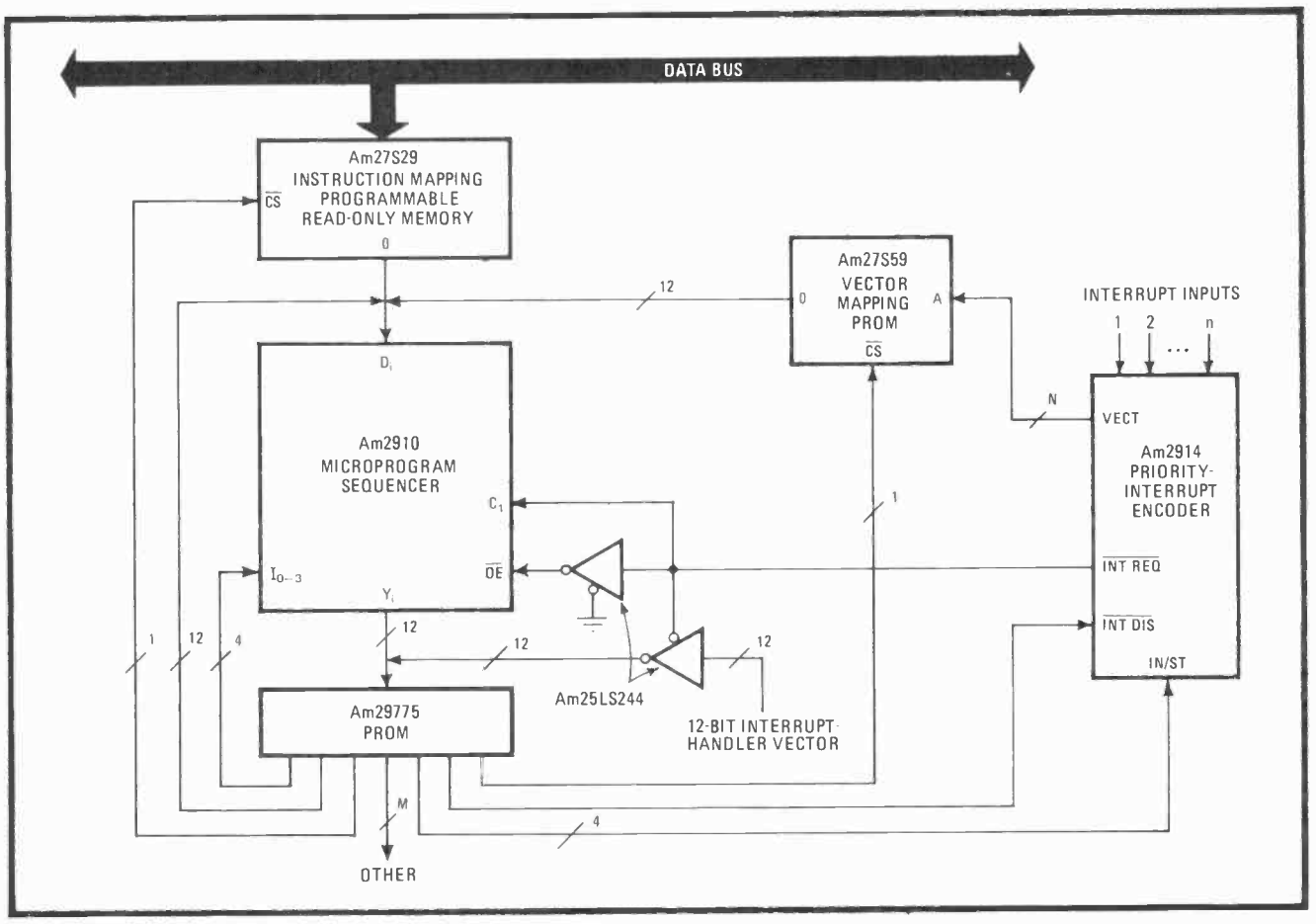
As shown in the figure, the components required are the 2914, the 2910 microprogram sequencer, a 29775 programmable read-only memory, and two separate PROMs for mapping instructions from main memory and interrupt vectors from the 2914 into starting addresses for the 2910.

If an interrupt is detected by the 2914 as the 2910 executes an instruction, the interrupt-request output of the encoder moves low. This action turns off the carry input of the 2910, for all practical purposes causing the sequencer to halt for a microcycle. It also causes any data that would normally appear at the Y_i outputs to be stored in the sequencer's program counter.

The interrupt request also forces the output of the sequencer into a high-impedance state. This allows an interrupt-handling vector to be applied at the Y_i outputs, thereby addressing the first instruction of the interrupt routine in the microprogram memory.

The 2914 is thus instructed to place an interrupt vector on its output port. The same word in microprogram memory also enables the output of the vector-mapping PROM to allow decoding of the interrupt vector. The result is then applied to the D inputs of the 2910 while it does a jump to the appropriate subroutine. Thus the first address of the interrupt routine is brought in, and the address to which the previously executed program is to return after the interrupt is serviced is stored away. If there is a point in the microprogram routing where no interrupts are to be allowed, a logic 0 can be applied to the interrupt disable input pin on the 2914.

The microcode for handling interrupts is shown in the table. The first entry commences with address I. This vector instructs the 2914 to execute a jump to subroutine if its condition code input is low. The encoder is then commanded to place its interrupt vector associated with the current interrupt request on its output port. At this time, it may be desirable to disable any further inter-



Interrupt address	Am2910 instruction	Am2914		Vector-mapping PROM	Data-mapping PROM
		Instruction	Interrupt disable		
I	CJS	Read vector	0	0	0
I + 1	–	Clear interrupt, last vector read	0	1	–
I + 2	–	Enable interrupt request	1	1	–
I + 3	CRTN	–	1	–	–

Stop. Standard elements of the Am2900 family are easily configured to provide interrupt capability for bit-slice microprocessors. Architecture is applicable to stacked interrupt systems. Microcode for handling interrupts (see table) is fast and simple.

rupts, in which case the appropriate pin should be brought low, as explained above. A logic 0 is also placed on the vector-mapping PROM while a logic 1 is placed on the data-mapping PROM's output-enable lead and the pipeline output-enable of the 29775. Thus the vector-mapping PROM will be the sole source of any input to the D port of the 2910.

At address I+1, the interrupt associated with the previous vector read into the 2914 may be cleared, and the vector-mapping PROM disabled by bringing its output-enable lead high. At address I+2 and subsequent addresses, the 2914 may be commanded to accept any interrupt by use of the enable interrupt request. The vector-mapping PROM is first disabled with a logic 1 signal. At this time the interrupt-disable pin of the 2914 is deactivated. At the end of the interrupt routine, an exit is achieved via the conditional-return instruction of the 2910. A logic 0 should be simultaneously applied to the condition-code inputs of the sequencer.

There is nothing that precludes the use of this architecture in a stacked-interrupt system. The number of interrupts that can be stacked is limited by the depth of the 2910. It is only necessary to issue a simple command to return from the subroutine utilized to the main program, for each stacked interrupt. □

Protected regulator has lowest dropout voltage

by Thomas Valone, *A-T-O Inc., Scott Aviation Division, Lancaster, N. Y.*
and Kelvin Shih, *General Motors Proving Ground, Milford, Mich.*

Providing an output of 5 volts at 10 milliamperes for an input of only 5.012 V, this regulator is ideal for use in many micropower applications, such as regulating the output of lithium batteries that drive low-power detection and recording instruments in the field. The circuit is useful in high-current situations also, as it can deliver up to 1 ampere at 5 V for an input of only 6.0 V. Short-circuit protection in this instance is provided by a single V-groove MOS field-effect transistor.

Contributing to the low-dropout characteristic of the circuit is the 2N6726 output transistor, which has a large junction area that allows a lower emitter-to-collector drop than most other devices, including Darlington arrangements. Thus the input-to-output voltage differential, 12 millivolts, is 6% that of one of the best low-dropout regulators reported to date.[1]

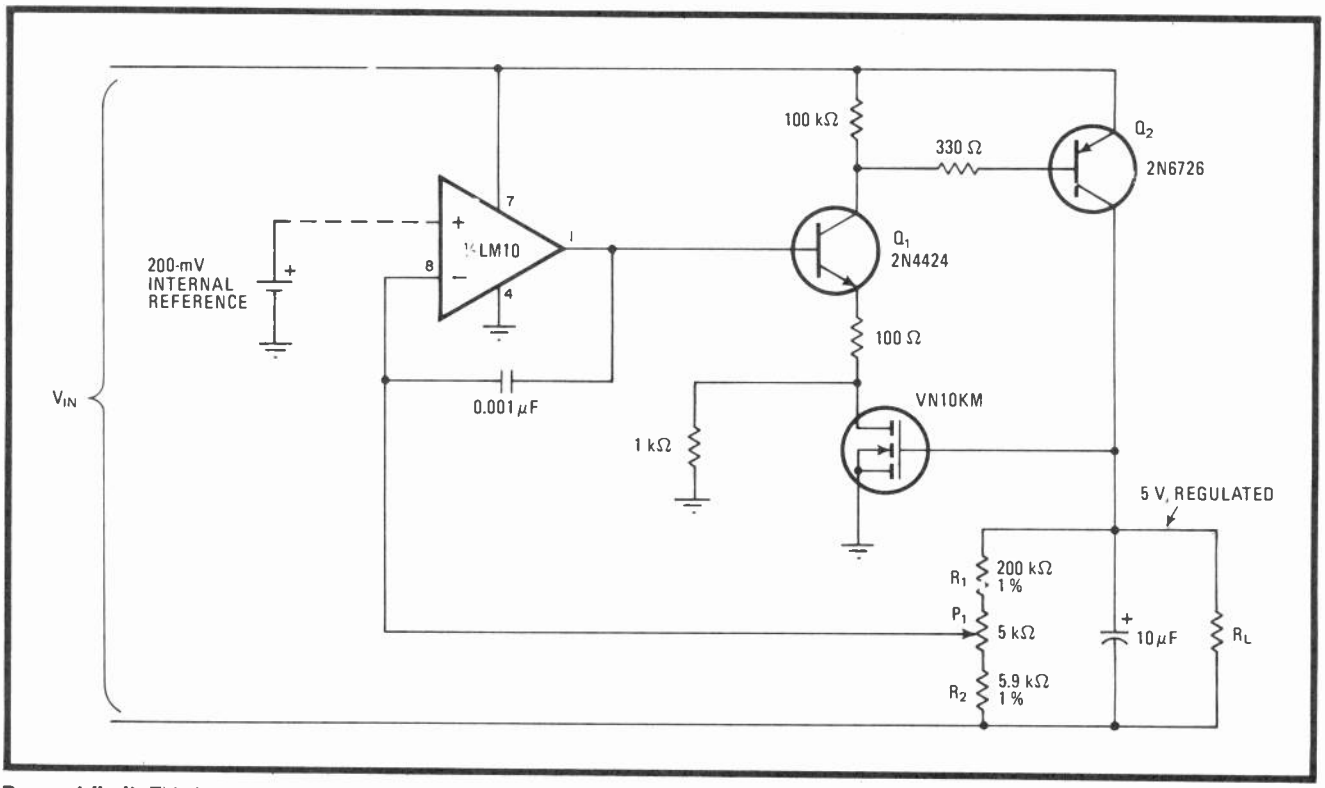
The input-to-output differential is only 350 mV at a load current of 500 mA. The 2N6726 is physically a small transistor but can dissipate 1 watt safely without a heat sink.

Short-circuit protection is provided by a Siliconix VN10KM, which presents a resistance of less than 10 ohms to the emitter circuit of the 2N4424 drive transistor under normal conditions. However, when the output is shorted to ground or excessive current is demanded, the drain-to-source resistance of the FET rises, safely shutting down the pass transistor. This characteristic can be used to advantage in adjustable current limiters, where the trip point is set by the input voltage. This method, incidentally, is more effective than any transistor foldback technique.

In operation, the LM10CH reference amplifier compares the voltage set by potentiometer P_1 to its internal 200-mV reference and through Q_1 acts to minimize voltage differences at the amplifier's input. With suitable selection of the component values in divider network R_1–R_2, the circuit will regulate over any voltage from 1 to 40 V. The operational-amplifier half of the LM10CH is available for other uses.

The load regulation is to within 0.3% for the range 0 to 100 mA and to within 1% for the range 100 mA to 1 A. The regulator's idle current is 320 μA. □

References
1. Kelvin Shih, "Micropower regulator has low dropout voltage," *Electronics*, April 12, 1979, p. 130.



Dropout limit. This low-power regulator, using output transistor operating in common-emitter configuration and having large junction area, can deliver 10 mA at 5 V for an input voltage only 12 mV higher and up to 1 A at 5 V for a 6-V input. Input-to-output voltage differential is only 650 mV at load currents of 750 mA. The V-MOS field-effect transistor provides short-circuit protection in such instances.

Foldback limiter has minimal parts count

by Michael G. Lyngsie
MG-EL Consultants, Copenhagen, Denmark

Providing virtually the same function as the foldback limiter proposed by Kularatna,[1] but using a minimum of parts, this circuit delivers a well-regulated 24 volts at a maximum of 4 amperes. The circuit is extremely rugged and will meet all but the most demanding industrial requirements.

In operation, transistor Q_1 operates as a differential amplifier to detect changes in output voltage and at the same time to keep track of the reference voltage, V_Z, which is constant as long as $I_E R_6 < V_o - 6.8$. The power-Darlington stage Q_2–Q_3 that follows serves as the series-pass transistor and its associated driver.

If there is a short circuit at the output or the load requires excessive current, I_E will also increase because Q_2 and Q_3 must be driven harder. This action causes Q_1 to draw off a corresponding current that is normally delivered to the zener. Thus the zener voltage must fall, and foldback limiting is initiated. The quiescent current that will flow during foldback ($V_o \approx 0$) is solely dependent on R_1, which re-initializes the supply upon removal of the overload condition. R_1 can be made as large as desired, with the only limitation being that I_{R1} must be greater than the sum of the leakage current (I_{leak}) through capacitor C_5, and I_{DC}.

Placing the series-pass transistor, Q_3, in the negative rail offers two distinct advantages. First, the device can be operated in the common-emitter configuration, enabling Q_3 to provide voltage gain and current gain. This enhances the dynamic range of the circuit. Secondly, most industrial equipment utilizes a negative ground, and so the power transistor can be directly mounted anywhere on the chassis for efficient cooling and the problem of electrical isolation can be eliminated. Furthermore, regulation is extremely fast because the only capacitors in the circuit are associated with the input filter (C_1) and output bypass networks. Foldback action is not very fast, though, because of the large value of C_2. This capacitor can be made an order of magnitude smaller without sacrificing stability.

The output voltage will be held constant to 100 millivolts with this arrangement. Other voltages can be selected by altering the voltage-divider chain R_3–R_4–R_5. The maximum output current is approximately:

$$I_{max} = (V_o - 6.8)h_{fe\ Q2}h_{fe\ Q3}/R_6$$

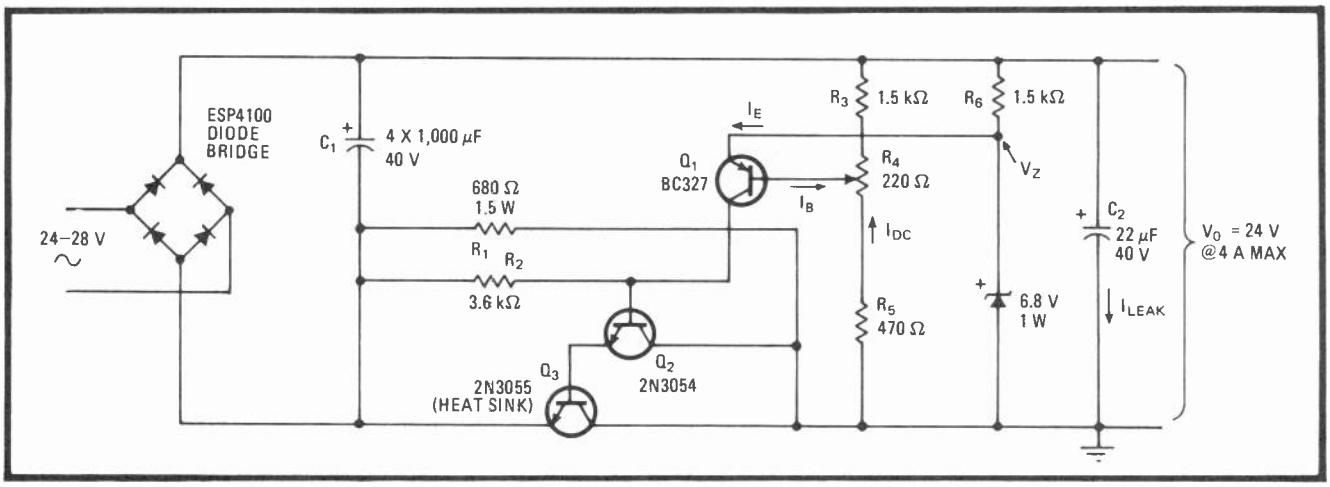
neglecting I_B and the current flowing in R_2.

The circuit develops a slight positive temperature offset of 0.4 V after warmup, due to the positive temperature coefficient of the zener diode. If this offset proves to be annoying or unwanted, a forward-biased 1N4001 can be placed in series with the zener to eliminate the problem.

It is recommended that four 1,000-μF capacitors be used for C_1, instead of a single 4,000-μF device because of the high ripple currents (and heat generation) that will be encountered. Output ripple is only 20 mV peak to peak at 3.5 A. If desired, the ripple may be more than halved by the addition of another 1,000-μF capacitor at the input. □

References
1. A. D. V. N. Kularatna, "Foldback limiter protects high-current regulators," *Electronics*, Jan. 31, 1980, p. 98.

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.



Rudimentary. Simple but rugged and reliable foldback limiter delivers 24 V ± 100 mV at a maximum of 4 amperes. Output ripple is only 20 mV at 3.5 A and may be reduced further simply by placing additional capacitors at input. Placing series pass element, Q_3, in ground lead gives circuit good dynamic range and simplifies solution of classic mounting-vs-isolation problem in dealing with cooling of the power transistor.

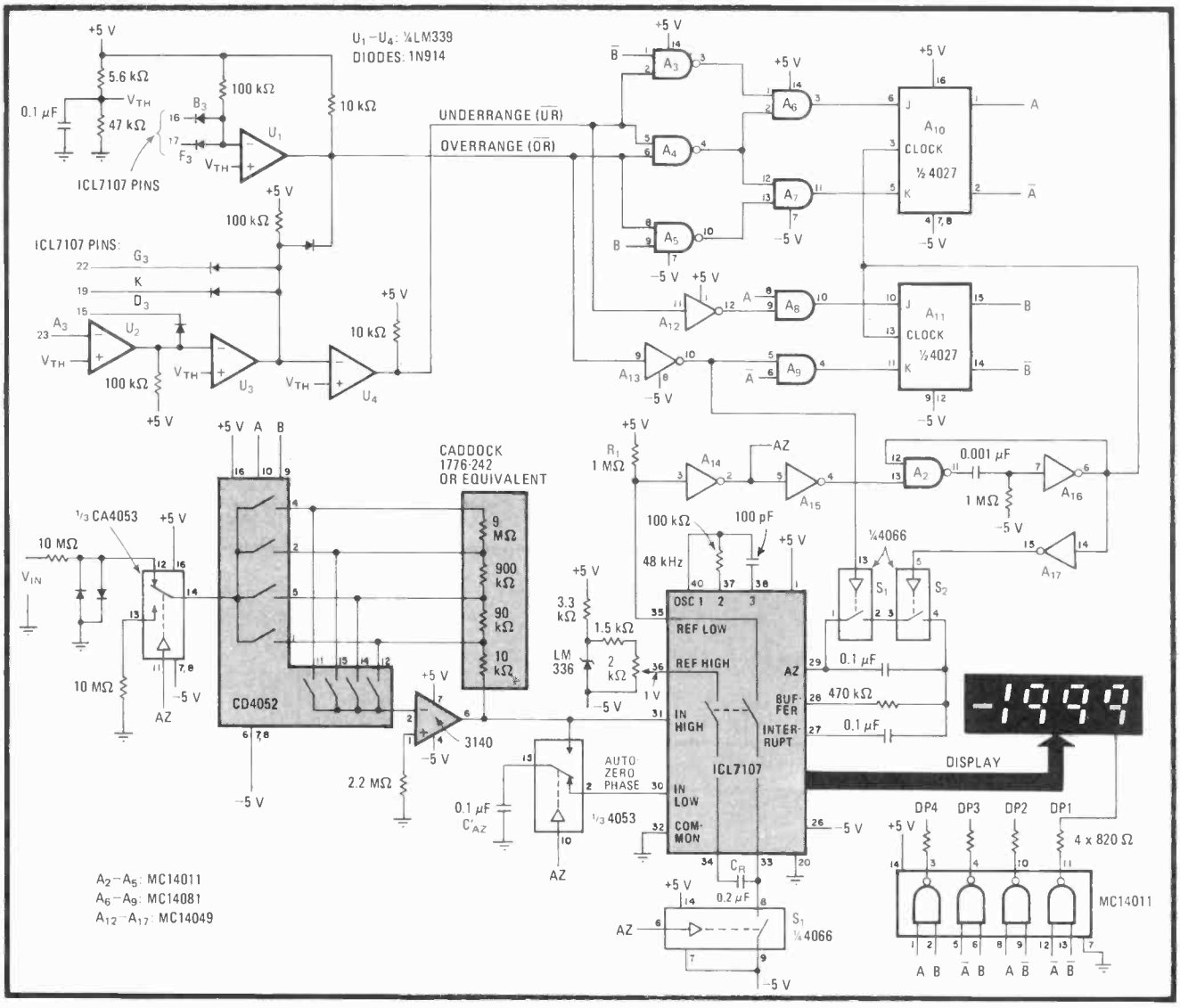
Low-cost autoranger scales DVM over four decades

by L. Y. Hung
Boston, Mass.

Autoranging capability can be added to a digital voltmeter with this circuit, which costs less than $25. Built around a dual-slope integrating analog-to-digital converter to ensure greatest measurement accuracy, the unit scales a 3½-digit voltmeter over a range of four decades (±1 to ±1,000 volts dc) without the need for complex feedback circuitry.

In operation (see figure), signals to the input are applied to the ICL7107 a-d converter through the range switch formed by the 4052 multiplexer and the attenuator that includes the CA3140 comparator and its accompanying decade resistor network. During each 333-millisecond measurement cycle, the converter proceeds to eliminate the error caused by the comparator's offset (autozero phase), stores the input voltage (integrating phase), and displays the difference, in terms of a voltage, between the integration time and the time required to discharge a reference potential from capacitor C_R (display phase). The autorange circuit (A_3–A_{13}) that follows tracks both underrange and overrange conditions with the aid of a suitable detection circuit. It generates the appropriate signals for controlling the range switch and thus the gain of the attenuation network.

The autorange circuit determines underflow or overflow at the initial portion of the autozero phase. During this time, the voltage on pin 35 of the converter drops momentarily. The drop switches gate A_{14} and thereby closes switch S_1, an action that brings pin 35 to logic 0 and completes the charging cycle for C_R. The rising edge of the AZ signal that clocks the range switch is delayed about 1 millisecond by A_2 and A_{16}, providing sufficient time to stabilize the display and to check for the underrange and overrange conditions.



Searching. DVM autorange circuit uses A_3–A_{14} to detect underflow and overflow conditions by examining the output state of ICL7107 a-d converter, then sets gain of input attenuator network over four decades through 4052 range switch. Circuit cost is under $25.

The range switch is an up-down counter. It will count down one state if an overrange signal is present and up one state if an underrange condition exists, over the binary range 00 to 11. The discharge path provided by switches S_2–S_3 reduces the residual charge on C_{AZ} during the de-integrating phase; otherwise continuous rocking between two adjacent scales may occur.

As for underrange and overrange detection, only one quad comparator need be connected to the ICL7107, as shown at the upper left. Both signals are derived from the converter's seven-segment outputs. Underranging occurs if the displayed number is less than 200; for overrange, the number must be greater than 1,999.

A blank display on digit 3 indicates the overrange condition. A blank output on digit 4 and either a 1 or a 0 on digit 3 signifies underrange. In equation form:

$$\overline{UR} = \overline{\overline{OV} \cdot G_3 \cdot \overline{K} \cdot (\overline{A}_3 + D_3)}$$

where A_3, D_3, and G_3 are the display segments of digit 3 and K is the converter's thousands multiplier. □

Improved burglar alarm discourages auto thieves

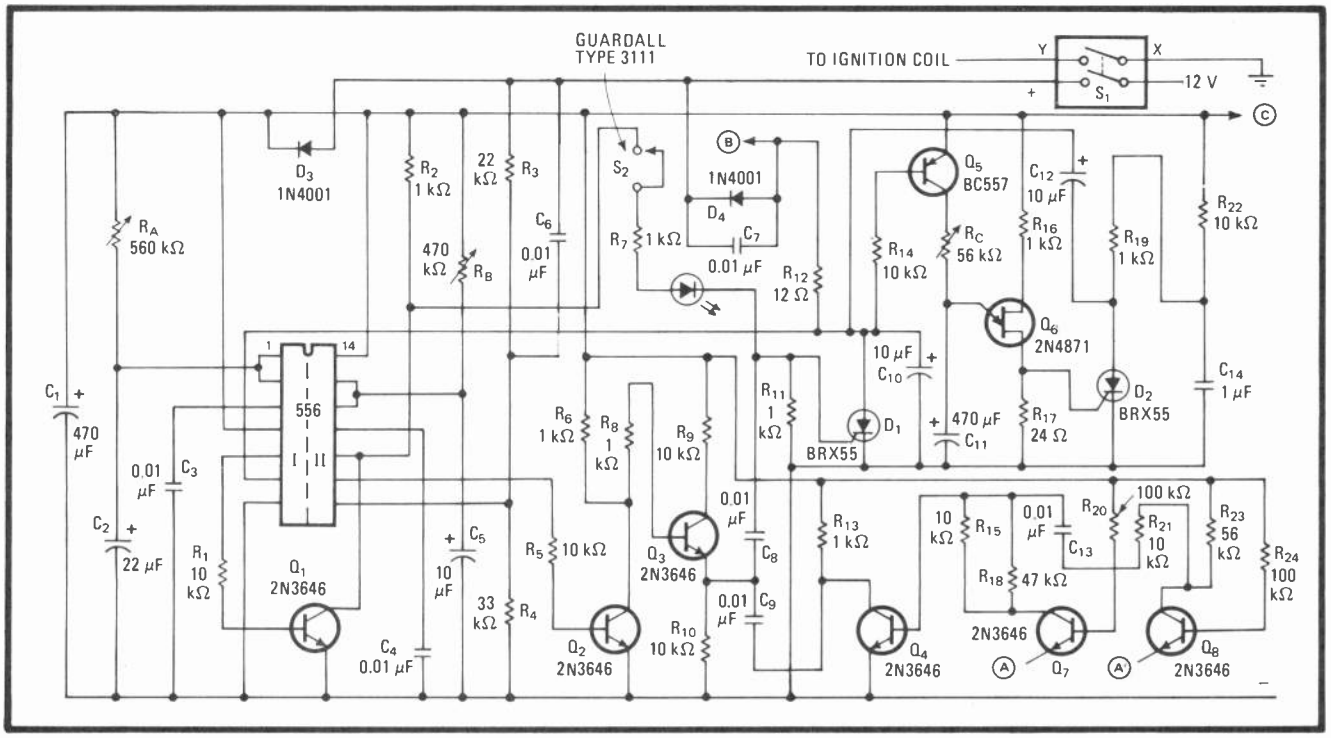
by Jose S. Correa de Quieros
Engineering Faculty, University of Oporto, Portugal

Inexpensively detecting an increase in battery current—like that caused by the car's courtesy light—this automobile burglar alarm competes on a cost-vs-performance basis with any of the commercial all-electronic devices now available. The alarm also senses and responds to severe mechanical shocks of the kind caused by breaking glass. Standby current is only a few milliamperes.

Closing switch S_1 arms the alarm through device I of the 556 dual timer after a time determined by R_A and C_2, enabling the driver to exit from the auto without triggering a false alarm. This switch also grounds the ignition coil so that it is impossible to start the engine.

Device II of the timer serves as the battery-discharge sensor. Voltage divider R_3–R_4 detects the small drop in the nominally set voltage at pin 8 (trigger input) of the 556 due to any current flow exceeding a few milliamperes. Q_2 and Q_3 then turn on (or D_1 and Q_4, if lamps, radios, tape players, or other loads connected to point A or A′ are disconnected by the thief), firing D_1 and Q_5 after a time determined by R_B and C_5. The horn relay at point B is then energized and timer Q_6 initialized. R_B and C_5 should be set to provide a delay of 5 seconds or so to enable the owner of the vehicle to enter and disarm the alarm. After a time set by R_c and C_{11} (maximum is 20 seconds), D_2 fires, resetting D_1 and the horn relay.

Capacitor C_1 and diode D_3 develop a dc average of the pulse train that is required to power the auto's clock via point C, effectively preventing the pulses from generating a false alarm. Severe mechanical shocks are detected by switch S_2, which is set with the aid of a screwdriver and a light-emitting diode that turns on when the switch elements make contact. When S_1 closes in actual operation, D_1 fires immediately to set off the alarm. □



On guard. Auto alarm detects small increases in battery current such as that caused by courtesy light activated by burglars, setting off horn relay after specified delay. Switch S_2 senses mechanical shocks of the kind caused by breaking glass and sounds alarm immediately.

LR oscillator indicates inductance directly

by John Jamieson
Technical Analysis Corp., Atlanta, Ga.

Inductance measurements accurate to within ±10% may be made simply if the inductor is connected into the frequency-determining portion of this low-cost LR oscillator. Component values have been selected so that the oscillator's period, in seconds, equals 0.01 times the coil's inductance in henries, over the range from 0.5 millihenry to at least 10 H. Thus the inductance can be read directly from a period/frequency counter connected to the circuit's output.

A_1 of the TL084 operational amplifier serves as the integrator in the basic oscillator, with A_2 a Schmitt trigger having trip points at one sixth and five sixths of the supply voltage and A_3 a 1-to-20 voltage divider. A_4 derives a voltage reference equal to half the supply voltage for driving A_1, A_2, and A_3.

A_3 delivers a current into A_1 of magnitude $i_L = (1/L)\int V_L dt$, where V_L is the initially negative output voltage of A_3 and L is the inductance under consideration. As a consequence, the output of A_1 is a ramp of voltage $V_o = RV_Lt/L$, where resistor R controls the gain of the stage, and t is time. Thus V_o rises linearly until A_2's trigger point is reached, whereupon it switches and brings V_L high so that V_o begins to decrease linearly. The cycle is repeated when the Schmitt's lower threshold point is reached.

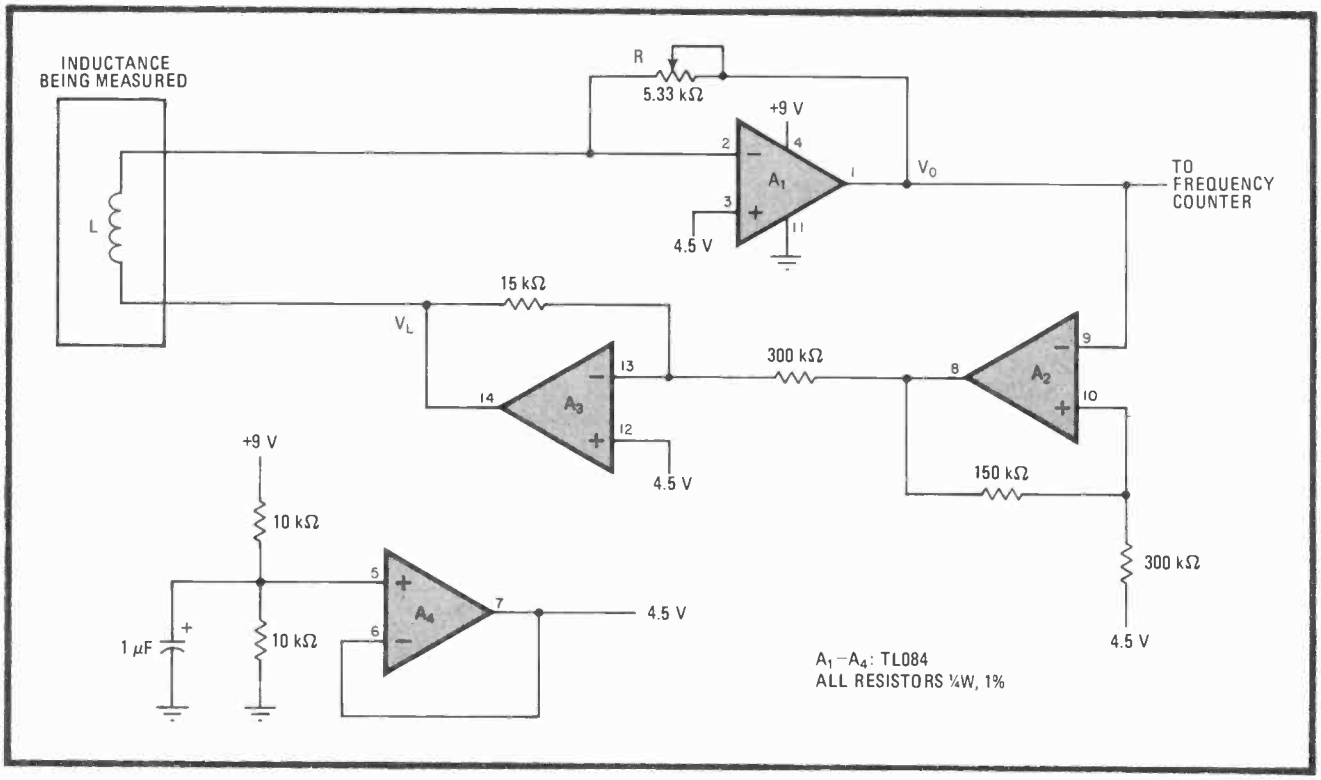
Selecting the period of oscillation to fall in the area of $t = \tau/4$, it is seen that $V_o = (RV_L\tau)/(4L)$, or $L = (RV_L\tau)/(4V_o)$. Because $V_L \approx V_o/13$, then $L \approx R\tau/52$. With R adjusted so that $R/52 = 100$, $L = 100\tau$.

The preceding analysis assumes that the ohmic resistance of the inductor is small. For each ohm of resistance present below 10 Ω, there will be an approximate decrease of 0.1% in the accuracy of the measurement.

For inductors with considerable resistance, it will be noted that:

$$i_L = (1/L)\int V_L(1-e^{-R_Lt/L})dt$$

where R_L is the resistance of the inductor, and so it can be shown that $L = (-R_L\tau/4)\log_e(0.9975R_L)$. Thus to find the inductance, it is necessary to measure its resistance, R_L; place the inductor in the circuit; and note the frequency of oscillation, τ. L may then be calculated. □



Self-measuring. Inductance of low-resistance coils is measured to within ± 10% by noting frequency of LR oscillator of which the inductor is a part. Frequency counter may be used to indicate inductance directly, since period of oscillator, in seconds, is 1/100 of the inductance value in henries. Procedure is slightly modified for inductances having high impedance, most of which is ohmic for units having low hysteresis.

One-chip multiplexer simplifies eight-trace scope

by Sam Curchack
EDO Corp., Government Products Division, College Point, N. Y.

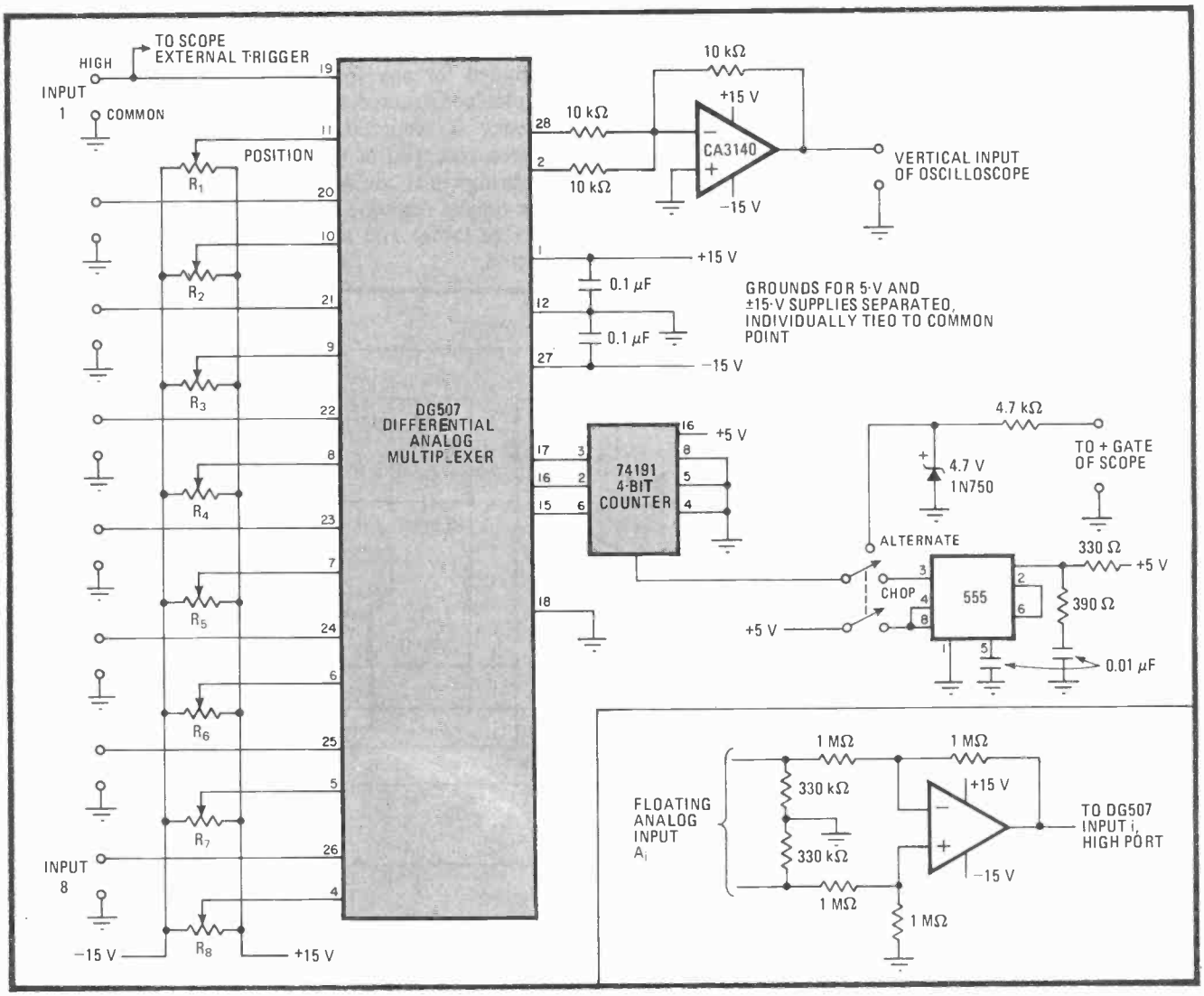
Displaying eight analog signals simultaneously with only a single-trace oscilloscope, this switching circuit can be built for even less ($35) than the one proposed by Wright.[1] Circuitry is simplified, too, by the use of a one-chip, eight-channel differential multiplexer. And unlike most other arrangements, this unit is more versatile, having a chopped-mode and alternate-mode option and trace-positioning controls for each analog input.

In the chopped mode, which can be used at sweep speeds up to 50 microseconds/centimeter, all traces are referenced in time to input 1, which is the signal used to trigger the scope. Operational amplifiers (see inset) may be added for handling floating inputs. The 555 timer, operating as an astable multivibrator, switches the 74191 4-bit counter at a 9-μs rate, the sampling-bit time. This action in turn sequentially switches the DG507 multiplexer. As each input is selected, it is added to the dc output voltage of its positioning potentiometer (R_1–R_8).

At sweep speeds of 1 millisecond/cm and faster, the unit's alternate-mode option may be used. The 555 is deactivated and each analog input is switched in turn at any sweep speed selected by the user. The resulting display, devoid of most switching transients, is somewhat cleaner than can be achieved in the chopped mode. All other settings remain the same. A gating signal is required to synchronize the 4-bit counter, however. This signal is supplied by the scope's +GATE port.

More than 8 traces can be displayed on a dual-trace scope. With an additional 8-trace switching unit of the type previously described, 16 traces can be displayed. A large screen scope such as the Tektronix 7603 will be required for suitable resolution in this case. □

References
1. George O. Wright, "Eight-trace scope display checks analog or digital signals," *Electronics*, Aug. 4, 1977, p. 108.



Sweep switch. Low-cost circuit displays eight analog signals on single-trace scope with aid of one-chip analog multiplexer. Alternate-mode (flicker-free above 200 μs/cm) and chopped-mode options are available. Each trace may be individually positioned on screen.

Test set characterizes FET's AGC response

by John Dunn
Bertan Associates, Syosset, N. Y.

The relationship of a field-effect transistor's gate-to-source voltage (V_{gs}) to its drain-to-source resistance (R_{ds}), and consequently its suitability for use in automatic-gain-control circuits, can be found with the n-channel FET tester described here. Making the FET's R_{ds} a part of one leg of a Wien-bridge oscillator makes it possible for a technician to correlate the bridge's instantaneous output frequency with a bridge-generated voltage that corresponds to the applied V_{gs}. Because the frequency is related to R_{ds} by a simple equation, R_{ds} may be readily plotted against V_{gs}.

Operational amplifier A_1 and zener diode D_1 maintain a voltage of about 7.5 volts for the FET's source, with its uncommitted drain connected into the circuit such that under steady-state conditions the Wien bridge built around A_3 is balanced at any given frequency for:

$$R_{ds}/(R_{fb}+R_{ds}) = (j\omega C_aC_b)/[j\omega R_aC_a(1+j\omega R_bC_b)+(1+j\omega R_bC_b)+j\omega C_aC_b]$$

Because $\omega = 1/(R_aR_bC_aC_b)$, the condition for balance simplifies to:

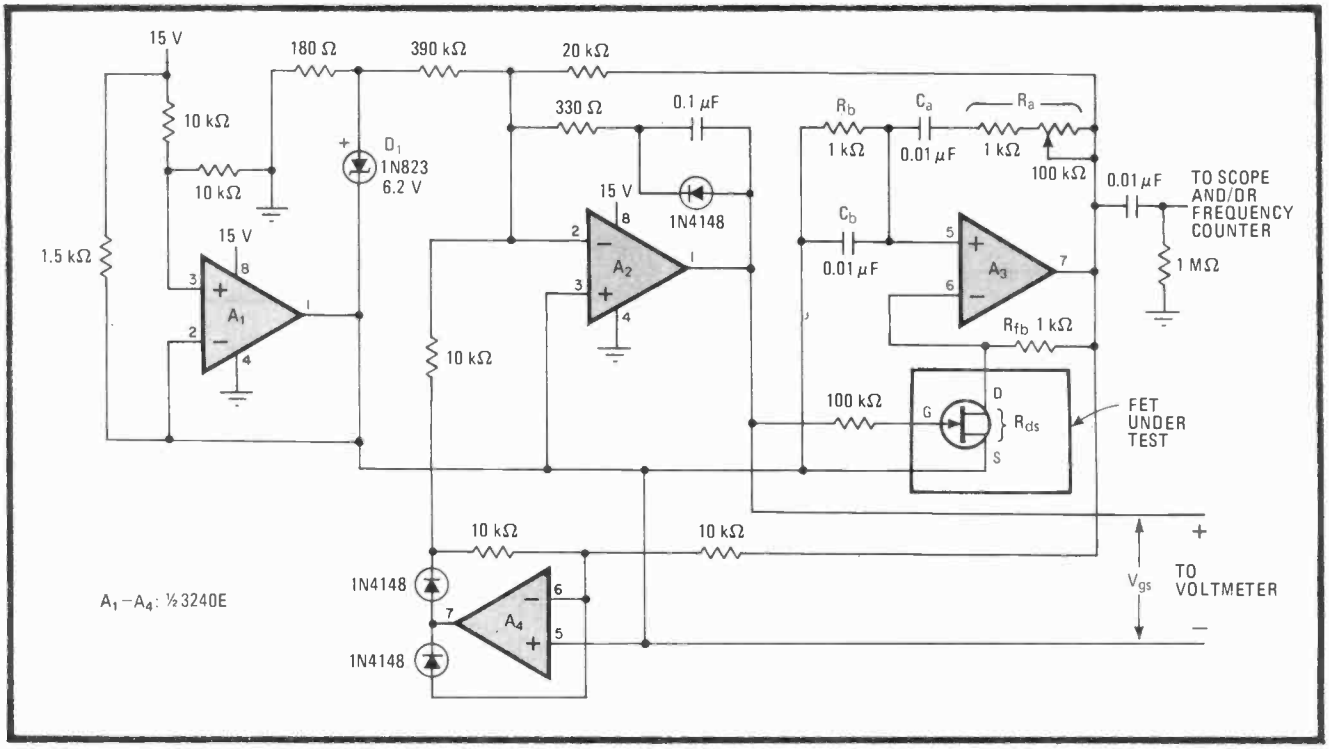
$$R_{ds} = R_{fb}/[(R_a/R_b)+(C_b/C_a)]$$

Noting that $R_a = 1/(\omega^2R_bC_aC_b) = 1/(4\pi^2f^2R_bC_aC_b)$, where f is the frequency of the oscillator, then $R_{ds} = R_{fb}/[1/(4\pi^2f^2R_b^2C_aC_b)+(C_b/C_a)]$. Thus R_{ds} may be determined for any frequency selected by R_a, and the AGC plot constructed if the corresponding V_{gs} for that frequency is recorded. Note that the required gate-to-source potential of 0 to −7.5 V is derived from the Wien bridge itself via A_2 and A_4.

The typical response of a Motorola MPF4391 is tabulated (see table) and may be used to check the tester's operation. □

AGC RESPONSE OF MPF4391 FET

V_{gs}	Frequency, Hz	R_{ds}, Ω
0	2149	17.9
−0.5	2303	20.5
−1.0	2465	23.4
−1.5	2656	27.1
−2.0	2893	32.0
−2.5	3207	39.0
−3.0	3683	50.8
−3.2	3936	57.6
−3.4	4314	68.4
−3.6	4836	84.5
−3.8	5604	110.3
−3.9	6199	131.7
−3.95	6560	145.2
−4.0	6949	160.1



Charting gain. Tester, with n-channel FET placed in leg of Wien-bridge oscillator, helps find relationship of FET's drain-to-source resistance (R_{ds}) to its gate-to-source voltage (V_{gs}), and thus its suitability for use in automatic-gain-control circuits. The common variable is frequency, which has an effect on R_{ds} via feedback voltage V_{gs}. The typical response of Motorola FET (table) aids in checking out the tester.

Fm decoder improves SCA subcarrier detection

by Robert F. Woody
Christiansburg, Va.

The 67.5-kilohertz subcarrier required for subsidiary communications authorization (SCA) service in the fm band can be recovered by a decoder that needs only two chips and one discrete amplifier. And it can be built for less than $10. Besides using fewer parts than existing designs, this circuit provides higher output and offers greater versatility.

As an illustration of its advantages, the 4046 phase-locked loop in the decoder provides an output level approximately equal to the fm level at its input, thereby generating adequate drive to succeeding stages. In addition, the PLL's filter also serves as the deemphasis filter, thus eliminating the need for a separate network. Finally, upon loss of the subcarrier, the circuit generates a signal that can cue a recorded message to the audience receiving SCA service.

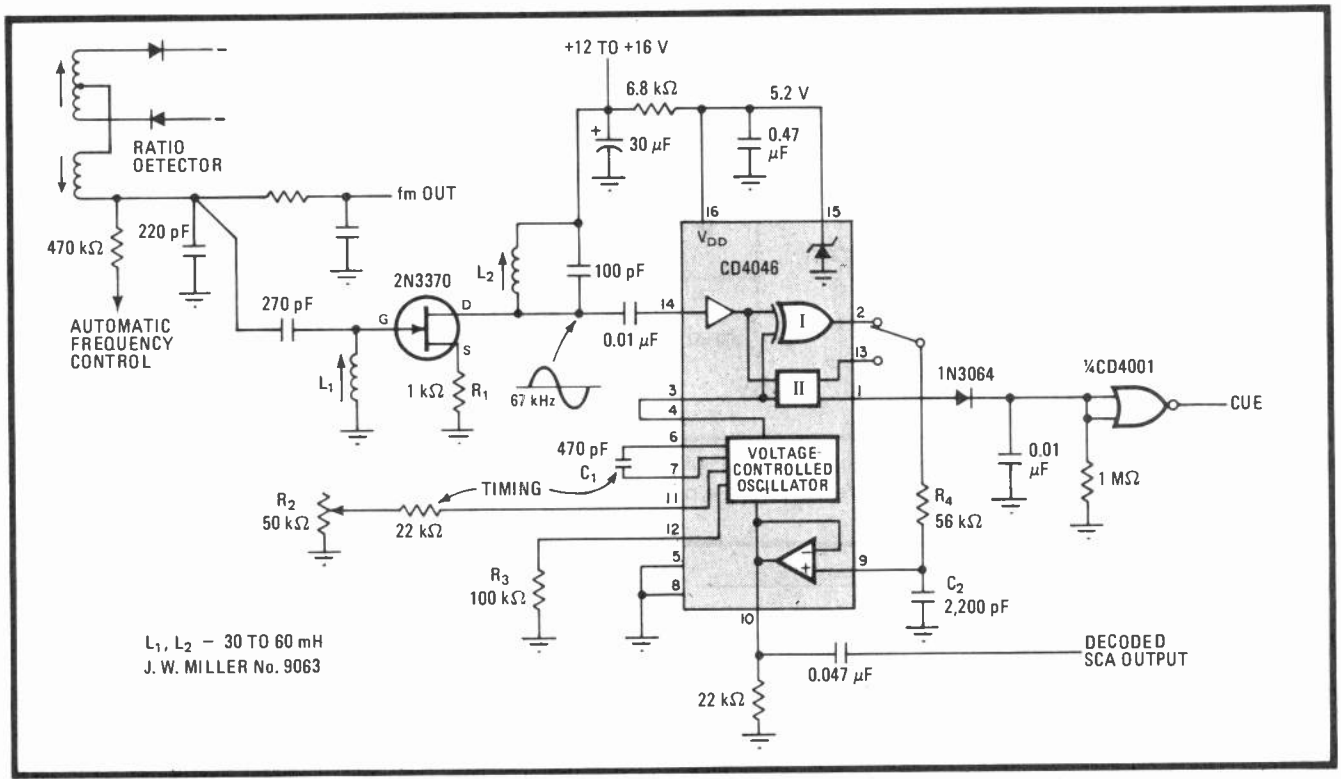
The decoder is attached to an fm receiver at its ratio-detector output, ahead of the deemphasis filter. For best performance, it is recommended that the signal be taken from a stereo receiver because its bandwidth, which is designed to be broad for the stereo carrier, provides good reception of the 67.5-kHz SCA signal.

The 2N3370 tuned field-effect-transistor amplifier separates the low-level subcarrier from the other program material, including the very strong stereo carrier. Resistor R_1 yields maximum amplifier gain at 1 kilohm. This resistance can be increased to reduce the amplifier's gain for fm receivers that deliver high-level output signals. Values to 5 kΩ are within the amp's range.

The CD4046 PLL performs the decoding. C_1 and R_2 set the loop's center frequency. R_3 sets the conversion gain (volts/radian) of the PLL's voltage-controlled oscillator. Increasing R_3 makes the VCO less sensitive to input-voltage changes. Decreasing R_3 reduces the SCA output level.

C_2 and R_4 comprise the low-pass filter. As placed in the circuit, these elements also deemphasize the SCA signal at high frequencies, the amount of deemphasis being about 3 decibels at 1.3 kHz.

A string of pulses is emitted from pin 1 of the 4046 when the PLL is in lock. The pulses are rectified by the 1N3064 diode and filtered by the 0.01-microfarad capacitor. Thus a dc level is derived. Should the subcarrier disappear, however, the level will fall and the CD4001 NOR gate will go high. This signal can be used to cue the playing of recorded messages, such as typical commercial advertisements. □



Simple service. Improved fm decoder for detecting SCA subcarrier yields higher output, uses fewer parts, provides good selectivity and cue option. Requiring only two chips, and one tuned amplifier for separating the stereo from the SCA subcarrier, it costs less than $10.

Low-cost logarithmic amp works over one decade

by Christopher S. Tocci
Becton-Dickinson Medical Systems, Westwood, Mass.

If extremely high precision is unnecessary and if the required dynamic range spans no more than one decade of input voltage, then this logarithmic amplifier will serve the application well. Use of a simple exponential generator, which is ultimately required to convert a voltage into its base-10 logarithmic equivalent, makes it possible to build the amp for a mere $3 to $4.

The overall system is shown in (a), with the schematic of the exponential generator shown in (b). Voltage divider R_1–R_2 applies 0.5 volt to RC combination R_3C_1 through op amp A_2 on power-up in order to initialize the exponential growth process. As C_1 charges, the output of A_2 increases as shown in the curve until the Schmitt trigger, A_3, which has a switching threshold of 10 v, fires, turning on field-effect transistor Q_1 and discharging C_1 to about 1.0 v. The process then repeats, with switching occurring at a rate, τ, determined by C_1 and R_2. The op amp must have a minimum slew rate of:

$$dV_o(t)_{max}/dt = (1/\tau)\, e^{t/\tau}|_{t=\tau} = (10 \log_e 10)/\tau = 23.03\, f_s$$

where f_s is the switching frequency. Thus at a switching frequency of 10 kilohertz ($C_1 = 0.01\ \mu F$, $R_1 = 4.32\ k\Omega$) the slew rate must be at least 0.23 v/microsecond.

During each switching cycle, the exponential output is compared at A_1 to the instantaneous input voltage, V_c, that is to be converted into its corresponding logarithm. A_1's on time, D_{V_p}, is thus related to input voltage V_c by:

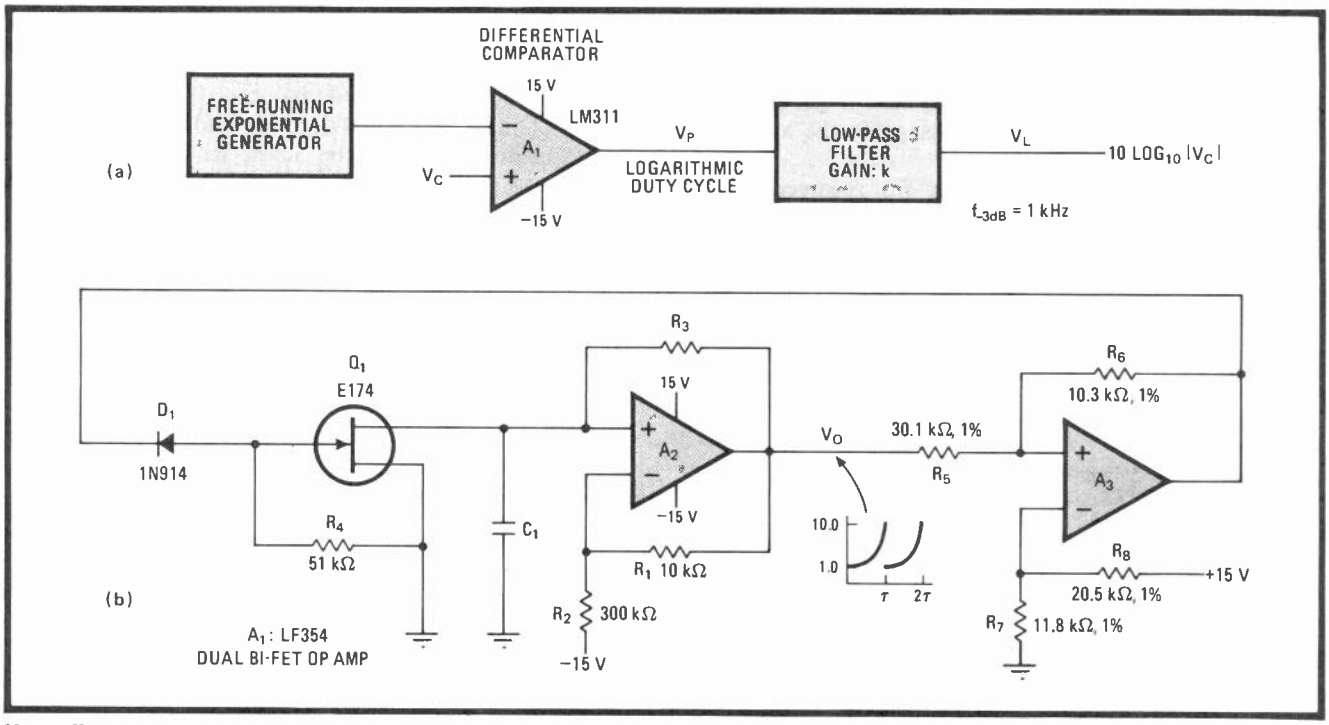
$$D_{V_p} = (t_{on}/\tau)\ 100 = \tau \log_e |V_c|/\tau = 0.434 \log_e |V_c|$$

where output voltage V_p corresponds directly to D_{V_p}, ignoring a scale factor.

The active low-pass filter of gain k that follows, which should be at least a third-order type for the best results, then finds the average value of V_p from:

$$V_L = \overline{V_p} = k(0.434) \log_e |V_c|$$

Choosing k such that $k(0.434) = k(V_{p\,max}/\log_e 10) = 4.34$, it is seen that $V_L = 10 \log_{10} |V_c|$ for $1 \leq V_c \leq 10$. □



Naturally. Low-cost generator provides exponential waveform of sufficient accuracy in amplifier that takes logarithms over one decade of input voltage. Filter averages pulse-width–modulated equivalent of V_c produced by differential comparator, A_1, for $V_L = 10 \log_{10} V_c$.

Hall sensors and flip-flop sustain pendulum's swing

by John Karasz
Sperry Corp., Great Neck, N. Y.

This circuit offers a simple way to control and sustain oscillatory motion in a simple pendulum and in many other types of mechanical oscillators. Using Hall-effect sensors to detect the instantaneous position of the pendulum and to call for delivery of an energy burst through a flip-flop to keep it swinging, the circuit is a good alternative to the complicated electromechanical arrangements frequently employed. The cost of the entire circuit is also

relatively low, making it especially attractive.

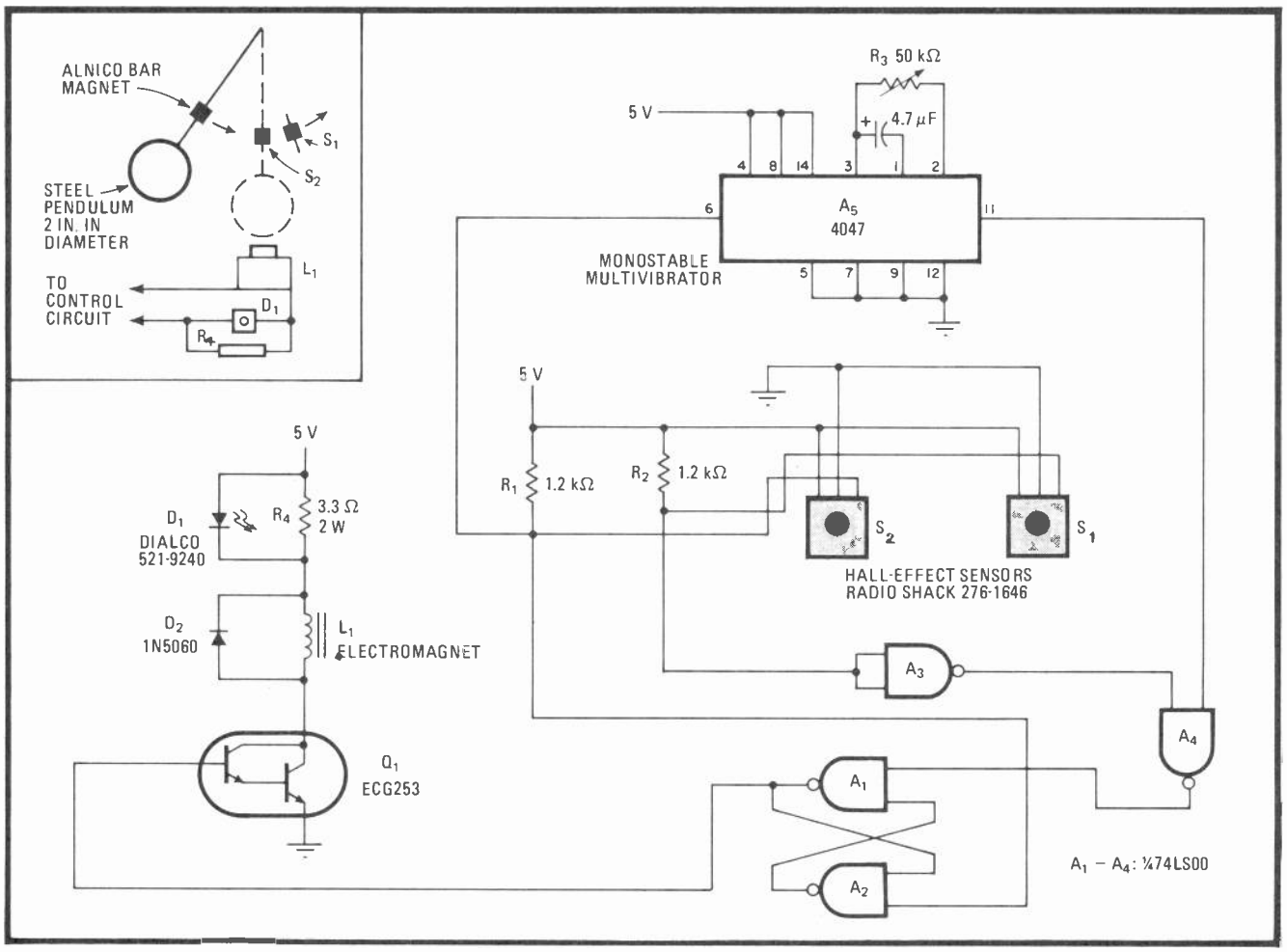
When the small permanent alnico magnet that is part of the pendulum support rod comes into sufficiently close proximity to Hall sensor S_1, the sensor generates a negative-going pulse. This pulse sets the R-S flip-flop formed by two cross-coupled 74LS00 NAND gates, A_1 and A_2. The Q output of the flip-flop, now at logic 1, energizes electromagnet L_1, thereby delivering energy to the pendulum via the field between the steel pendulum bob and L_1.

When the pendulum bob reaches the lowest point in its trajectory, L_1 is deenergized by the negative-going pulse generated by sensor S_2, which clears the flip-flop. Simultaneously, one-shot A_5 is triggered. Hence, as long as the Q output of A_5 remains active low, the flip-flop cannot be retriggered because gate A_4 cannot move to logic 0. This action prevents L_1 from energizing and thus creating any drag effect on the pendulum. Also, it conserves power by limiting the time L_1 is on.

In order to initialize the circuit at a relatively small pendulum swing, the period of the one-shot should be set for $t = T/4$, where T is the natural period of the pendulum. Because the oscillation frequency of a simple pendulum is $\omega^2 = g/L$, where $\omega = 2\pi f$, $g = 32.2$ feet per second squared, and L = the distance from the point of support to center of mass of the pendulum bob, it may be seen that $T = 2\pi(L/g)^{1/2}$, and so t should be in the range of 0.32 to 0.36 s in a practical configuration, for T = 1.44 s.

As for component considerations, L_1 is constructed from 100 feet of AWG 24 enameled wire wound on a steel core 1 1/16 inch long and 3/8 in. in diameter. The alnico magnet is situated only about 0.45 in. above the top surface of the pendulum bob—in terms of metric units, approximately 12 millimeters away. The magnet is 3 mm wide, 3 mm high, and 8 mm long. The clearance between the magnet's pole face and the Hall-effect sensor's surface should be between 1/32 in. and 1/16 in. for best results. A small decoupling capacitor (0.033 μF, disk ceramic) is connected between the supply lead and ground of the 74LS00 chip to keep circuit transients caused by S_1 or S_2's firing from inadvertently setting the flip-flop to the wrong state.

Light-emitting diode D_1 serves as a visual monitor, being lit when L_1 is energized. When mounted at the base of the electromagnet, it facilitates a qualitative check on the performance of the system. □



Keep swinging. Hall-effect sensors detect instantaneous position of pendulum, direct flip-flops A_1-A_4 to generate energy pulse via field between L_1 and pendulum bob in order to keep pendulum moving. One-shot A_5 prevents flip-flop refiring in any given cycle, thus stops pendulum drag, and conserves energy. Inset illustrates physical relation of bar magnet to pendulum and interface elements.

Sampling filters simplify converter's offset measurement

by Dennis Knowlton, *National Center for Atmospheric Research, Research Aviation Facility, Boulder, Colo.*

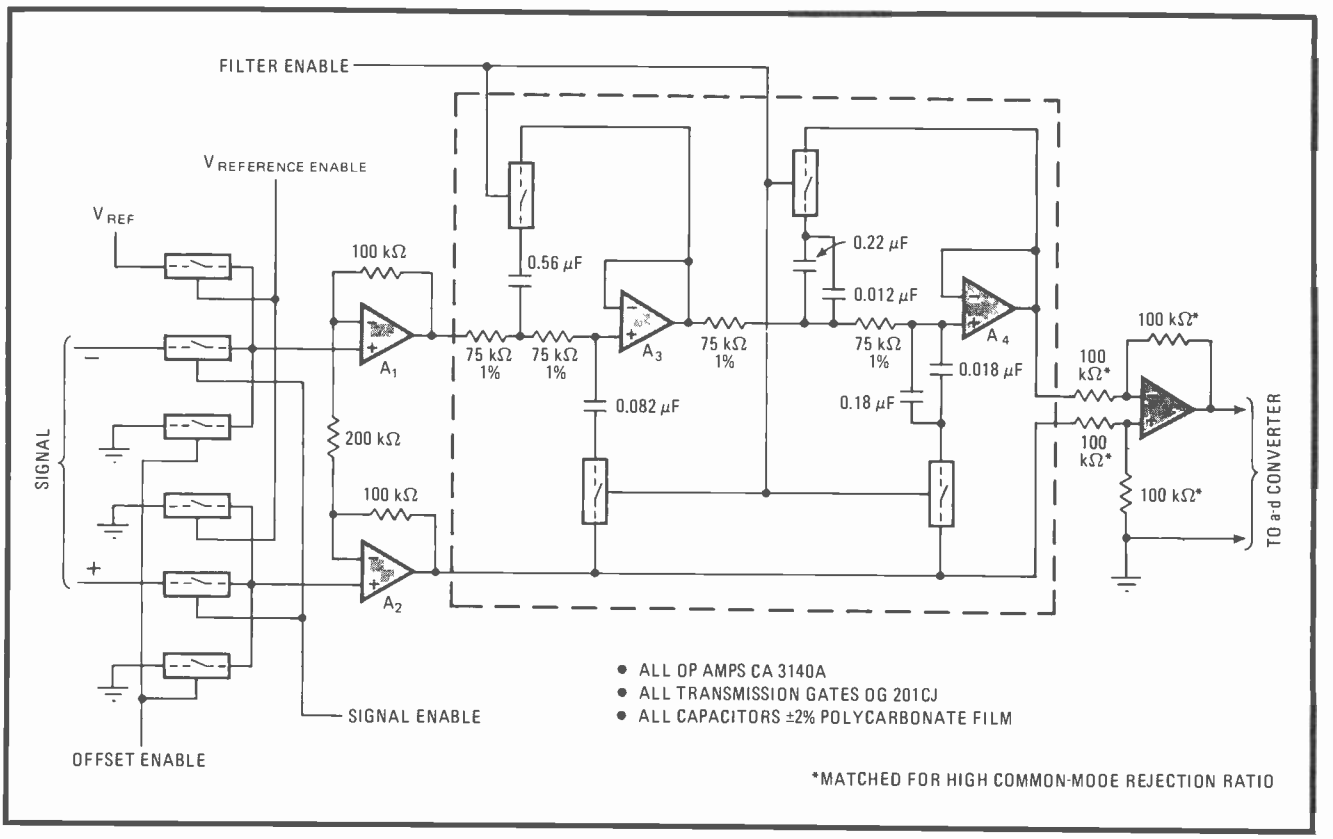
A microprocessor-based data-acquisition system has difficulty in making corrections for input offset and gain drift when it uses active filters to remove the effects of aliasing, or system noise. In such circumstances, the filters' frequency response and settling time vary as a function of the sampling rate and the magnitude of the input signal. However, the difficulties encountered with these sampled-data systems may be overcome by means of a switched aliasing filter, so that the anomalies in filter response may be virtually neglected and the offset and gain drift may be readily determined under software control.

In the typical input stage leading to the system's a-d converter, the noninverting ports of op amps A_1 and A_2 are periodically switched to ground and to a reference voltage so that the circuit can be isolated from all external stimuli and its inherent offset and gain determined. This scheme eliminates potentiometers and the requirement for precision components. It also leaves the measuring task to the software routine, where time and temperature have no effect on system accuracy, and where the data can be corrected for actual gain and offset by means of look-up tables.

Because of sampling, however, the filter's frequency-domain response becomes a factor and thus a significant amount of signal data can be lost during the filter's settling time. Switching the filter out at a very slow rate compared with the signal sampling rate, and doing so at a low duty cycle, eliminates the problem.

The key to the success of the circuit lies in the fact that in the standard active filter, the only energy-storage elements are capacitors. Switching these elements out of the circuit periodically transforms the filter into one that has a very high cutoff frequency; thus the filter is essentially out of the circuit and its op amps' offset and gain drift can be easily measured. When the capacitors, which store the instantaneous value of the driving signal, are switched back into the circuit, they perform their basic filtering function. Thus, assuming the use of fast op amps, a high-speed a-d converter, and low-leakage capacitors in the filter, the signal-path response of the filter is unchanged; yet, offset and gain drift can be determined.

Shown in the circuit example is a simple four-pole filter built around A_3 and A_4 whose components are selected to reject aliasing noise at 10 hertz. Signal-path sampling is done at 50 Hz and capacitor switching at 0.1 Hz for a duration of 12 microseconds. The input and output stages of the circuit all utilize standard differential amplifiers. □



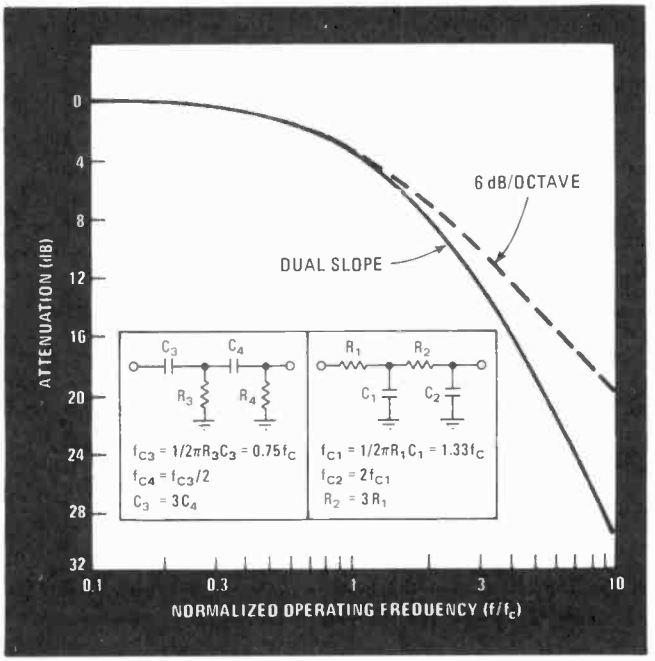
Indeterminate. Aliasing filter A_3–A_4 for data-acquisition system makes it impossible to ascertain input offset and gain drift unless it is itself of the sampling type. Filter's signal-path response will be unchanged, but stages' inherent imperfections can then be measured.

Dual-slope filters optimize speaker's crossover response

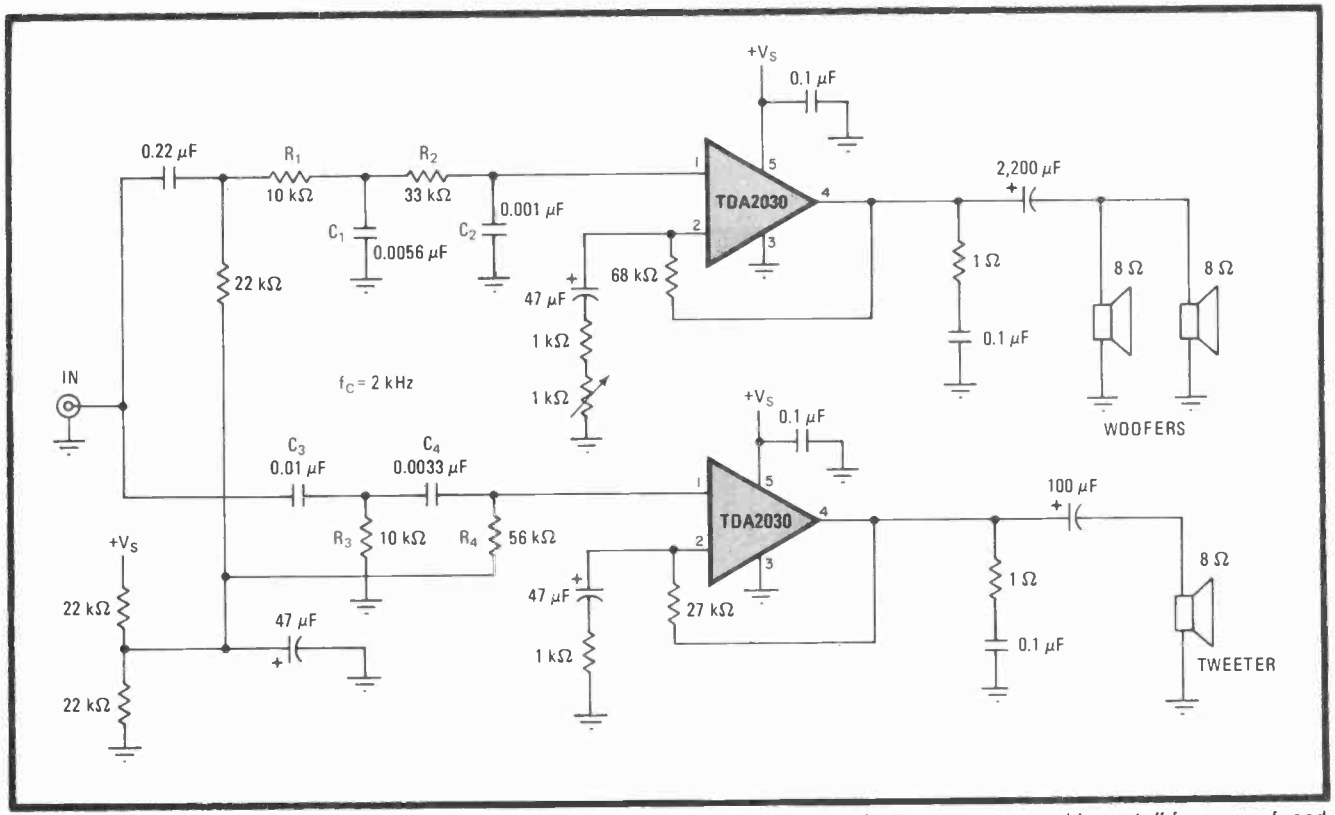
by P. Antoniazzi and A. Hennigan
SGS-ATES Electronic Components, Milan, Italy

The crossover response, and thus the overall performance, of a two-way high-fidelity loudspeaker system can be significantly improved with these high- and low-pass networks. Staggering two cascaded RC filters in the woofer channel yields a slope of 6 dB/octave near the cutoff frequency, f_c, and a notably steeper 12 dB/octave beyond f_c. When combined with the complementary (inverted response) output of the tweeter section, optimum crossover characteristics are achieved at low cost and without audio-frequency discontinuities at f_c.

In general, many simple low-pass networks can provide a 6-dB/octave response at frequencies approaching f_c from the low side. When a single-pole filter is used, however, as is still done on occasion, the maximum roll-off beyond f_c can never be greater than 6 dB/octave. Unfortunately, the typical loudspeaker does not have a linear enough response to handle high-level signals (de-



2. Response. Dual-slope filter, using staggered RC networks, virtually eliminates drop-off in audio output at the cutoff frequency of hi-fi speakers, while providing a roll-off of greater than the usual 6 dB/octave. Equations for woofer and tweeter sections summarize design.



1. Distortionless. Staggered low-cost, low-pass filters in woofer channel achieve slope of 6 dB/octave approaching cutoff frequency f_c and 12 dB/octave above f_c without introducing quadrature phase shift and accompanying distortion produced by loudspeakers. When combined with complementary output of high-pass section, system achieves crossover characteristic devoid of audio discontinuities at f_c.

graded by only 6 dB/octave) at its high-frequency limits, and so distortion results.

With second-order filters (12 dB/octave), a loss of audio usually occurs at the crossover point. This phenomenon is caused by the $+90^\circ$ phase shift of the low-pass network, which when combined with the -90° output of the system's high-pass filter tends to cancel the audio output.

Using a third-order Butterworth filter solves both of the aforementioned problems, yielding a flat response from dc to near f_c, steep cutoff (18 dB/octave) above f_c, and a gradual phase change across the band of interest. But this method is expensive, requiring two or three op amps and a large number of external components.

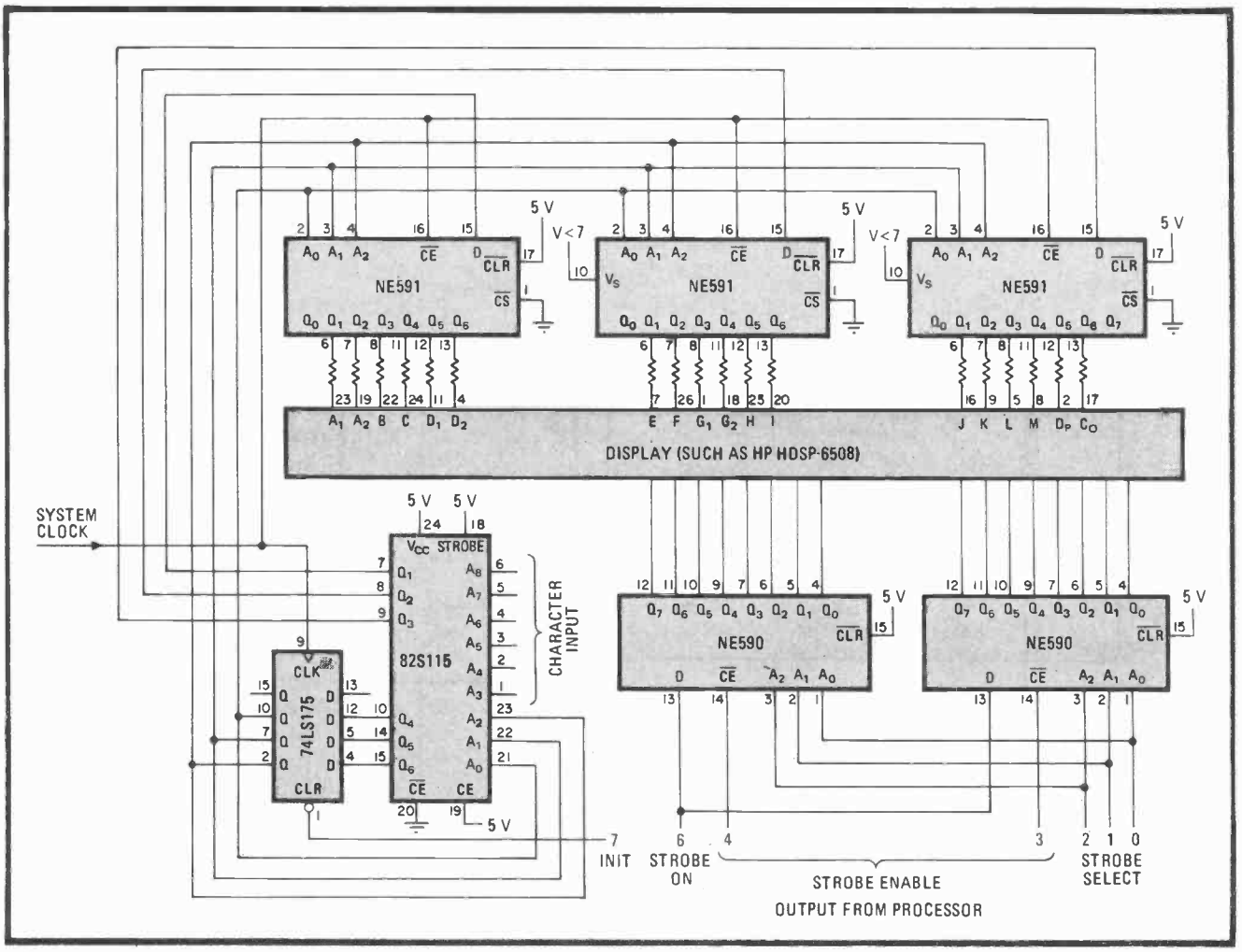
The dual-slope crossover network (Fig. 1) provides a viable answer to the problem. Staggering the responses such that the cutoff frequency of the first RC network is one half that of the second, attenuation at the crossover frequency will be 3 dB as in other systems, but the phase shift at f_c will be 60°; thus the cancelation problem typical of second-order filters is avoided. This circuit is ideally suited to active loudspeaker systems.

The plotted response of the woofer section is shown in the curve, which is complete with the required design equations. Corresponding equations for the tweeter are also included. □

Low-cost alphanumeric decoder drives British-flag display

by S. Cash Olsen
Signetics Corp., Sunnyvale, Calif.

Converting 64-character ASCII into an 18-segment ("British-flag") display font, this microprocessor-controlled alphanumeric decoder is a low-priced ($12) alternative to circuits costing up to five times as much. Most 18-segment displays (from Hewlett-Packard, Monsanto, and others) may be driven directly. And with the addition of high-breakdown output transistors to the driving circuitry, vacuum fluorescent panels and similar displays

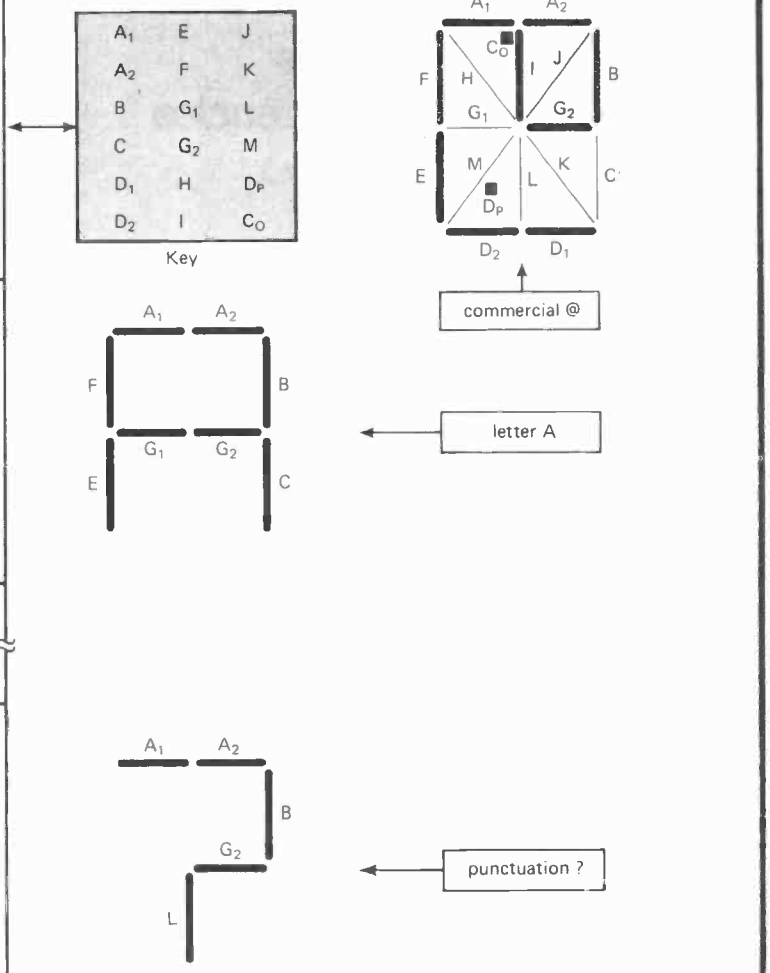


Charting characters. Low-cost alphanumeric decoder converts ASCII symbols into 18-segment display representation. Segment information, stored as table in 82S115 PROM, is clocked out in 3-bit segments over six states for each character, placed in display via NE591 drivers at any location by NE590 strobe latches. PROM character-generation table outlines method utilized to create symbols.

READ ONLY MEMORY CHARACTER GENERATION

Address	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
000_8	0	0	1	X	X	X
001	0	1	0	1	1	0
002	0	1	1	1	1	0
003	1	0	0	1	1	0
004	1	0	1	0	0	0
005	1	1	0	1	0	0
006	1	1	1	1	0	0
007	1	1	1	X	X	X
010	0	0	1	X	X	X
011	0	1	0	1	1	0
012	0	1	1	1	1	0
013	1	0	0	1	1	0
014	1	0	1	1	1	0
015	1	1	0	0	0	0
016	1	1	1	0	0	0
017	1	1	1	X	X	X
⋮	≈		⋮			≈
770	0	0	1	X	X	X
771	0	1	0	1	0	0
772	0	1	1	1	0	0
773	1	0	0	1	0	1
774	1	0	1	0	0	0
775	1	1	0	0	0	0
776	1	1	1	0	0	0
777	1	1	1	X	X	X

Symbol



requiring high voltage may be accommodated, also.

In general operation (see figure), the microprocessor coordinates character selection, strobe-timing, and overall control duties with the aid of the NE590 strobe drivers, the NE591 peripheral display drivers, and the 74LS175 quad latch. When suitably addressed, the 82S115 512-word-by-8-bit PROM, which stores all the ASCII characters, delivers a logic-state table corresponding to the character selected via the clocked 74LS175 and the NE591s.

The PROM functions both as a character-request look-up table and as a state machine, with the quad flip-flop holding the current machine state. Bit 7 of the processor initializes the state to zero at the beginning of a character-decode cycle.

Logic signals corresponding to the character desired are then applied to pins A_3–A_8 of the PROM, and the device is clocked through seven states (see table) so that the desired segments are excited. The display is then strobed and the character thus placed in any desired location via command from pins 0 to 6 of the processor via the strobe latches, each latch of which is enabled separately. This process is repeated for up to 64 characters, the maximum that may be placed on the display at any given instant. Thereafter, as in all multiplexed displays, only one character is enabled at any time. All characters will appear to be displayed continuously, however, because of the high scanning rate.

As seen in the table, during each clocked state the PROM generates 3 bits of segment information. Six such states define the character produced. Thus only three display segments switch during each NE591 latching period, substantially reducing load transients and large load-current variations, which tend to cause difficulty in circuits of this kind. Only six of each NE591's eight outputs are used, to reduce power dissipation. Note that each device handles 6 of the total of 18 display segments for each character.

As the circuit is digital, neither layout nor component values are critical. The clock frequency, typically less than 5 MHz, should have a minimum pulse width (t_w) of 100 ns, however, in order to ensure proper display and strobe latching. □

Contact tester quantifies open-, short-circuit tendencies

by Steven Nirenburg and Wunnava V. Subbarao
Florida International University, Miami, Fla.

Many present-day electronic systems, being modular in nature, rely heavily on connector blocks to hook the various functional units together. As such, it is becoming increasingly important to detect any momentary open-circuit or short-circuit tendencies of the system at the connector—especially in high-vibration environments—both in production-line testing and during actual operation. This tester detects both, while indicating if either condition persists beyond a given time preset by the user.

Consider the detection of an open-circuit tendency of contact S_1, as shown in the figure. For the purposes of discussion, the open-circuit condition is arbitrarily chosen to be one in which the resistance across S_1 is greater than 10 ohms for a period equal to or greater than 100 microseconds.

On system reset, the 74192 counters and 7476 flip-flops are brought to logic 0. If S_1 is closed, voltage V_1 will be near zero and the outputs of comparators G_1 and G_2 will be high. Light-emitting diode D_0 then glows, indicating the contact is closed.

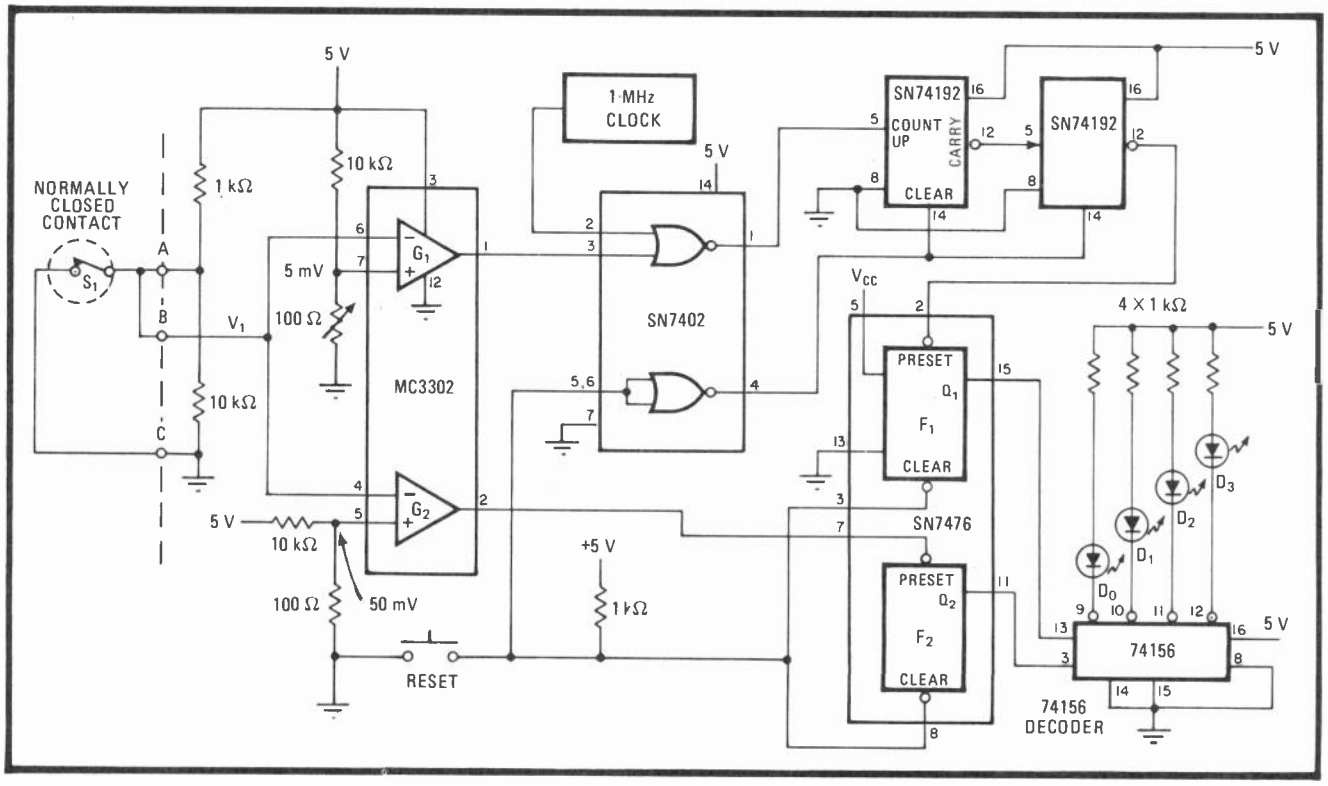
If S_1 is momentarily opened or shows any contact deterioration, V_1 rises slightly above ground potential, forcing G_1 low and gating the output of the 1-megahertz clock through to the counters. Thus should the contact deterioration last for 100 μs, 100 clock pulses will be counted and the resulting carry pulse generated from the second 74192 will set flip-flop F_1. And if the ohmic resistance across S_1 goes above 10 Ω, V_1 will rise above 50 millivolts, forcing G_2 low and flip-flop F_2 high.

Thus D_1 will glow if F_1 is set and F_2 is clear. D_2 will glow if F_1 is clear and F_2 is set. D_3 will light if both F_1 and F_2 are set, so that the predetermined open-circuit time and resistance of S_1 may be readily recorded.

Short circuits are readily detected by connecting points A and B across the normally opened contact under test. When the contact is open, V_1 is near zero and the system remains in the reset position, lighting up D_0. If shorted momentarily, S_1 will cause either D_1, D_2 or D_3 to light. For the values shown in the figure, D_1 will glow if the short circuit exceeds 100 μs or more; D_2 indicates if S_1's resistance is less than 1 MΩ; D_3 illuminates if both of the aforementioned conditions exist.

By changing the clock frequency or the counting limit, any time interval can be preset. Similarly, the impedance at which the circuit responds may be selected by adjusting the threshold voltage at G_2. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.



Connection. Tester for block connectors, pc boards, and cable assemblies indicates if duration of open or short circuit in circuit pin or lead exceeds preset time and checks relative magnitude of resistance across switch or broken wire. Four LEDs indicate state of affairs.

Reducing a PLL's phase jitter

by R. P. Leck
Bell Laboratories, Crawford Hill, Holmdel, N. J.

The design of a phase-locked–loop frequency multiplier is sometimes constrained by its loop-damping and bandwidth requirements. In this case, harmonics related to the loop's input frequency are present at the output of the loop's phase detector, generating excessive sideband noise and thus excessive phase jitter. This occurs as a result of modulating the voltage-controlled oscillator with the filtered output of the phase detector. Adding an extra break, or corner, frequency to the PLL's filter response reduces this sideband noise, however, by reducing the modulation index at the loop's VCO.

A block diagram of a typical PLL frequency multiplier is shown in (a). Detector A_1 compares the phases of the input signal, f_1, and a divided-down VCO signal, f_2, and generates a voltage proportional to the phase difference between the two. This signal, after passing through low-pass filter A_2, is applied to the VCO, A_3, to alter its output, f_{vco}. As a result, the phase difference between f_2 and f_1 is minimized. The loop is in the locked state when f_1 equals f_2.

The level of the sidebands that appear at the loop's output as a result of frequency-modulating the VCO with the filter's output are related to the modulation index of the harmonics; for a PLL multiplier, the index is given by:

$$\theta_o(s) = NK_oF(s)V_d/s$$

where N is the loop's divider constant, K_o is the voltage-to-frequency control function of A_3 divided by N, F(s) is the transfer function of the loop's low-pass filter, and V_d is A_1's output voltage. Reducing the numerical value of F(s) reduces the modulation index, $\theta_o(s)$. The net effect is a reduction in the sideband noise at the loop's output.

The transfer function of the active loop filter typically used in PLL circuits (b) is:

$$F_2(s) = (s\tau_2+1)/s\tau_1$$

where $\tau_1 = R_1C$ and $\tau_2 = R_2C$. Adding the capacitor C′ across R_2 as shown in (c) creates a second-order filter whose transfer function is given by:

$$F_3(s) = (s\tau_2+s\tau_3+1)/(s^2\tau_1\tau_3+s\tau_1)$$

where $\tau_3 = R_2C'$.

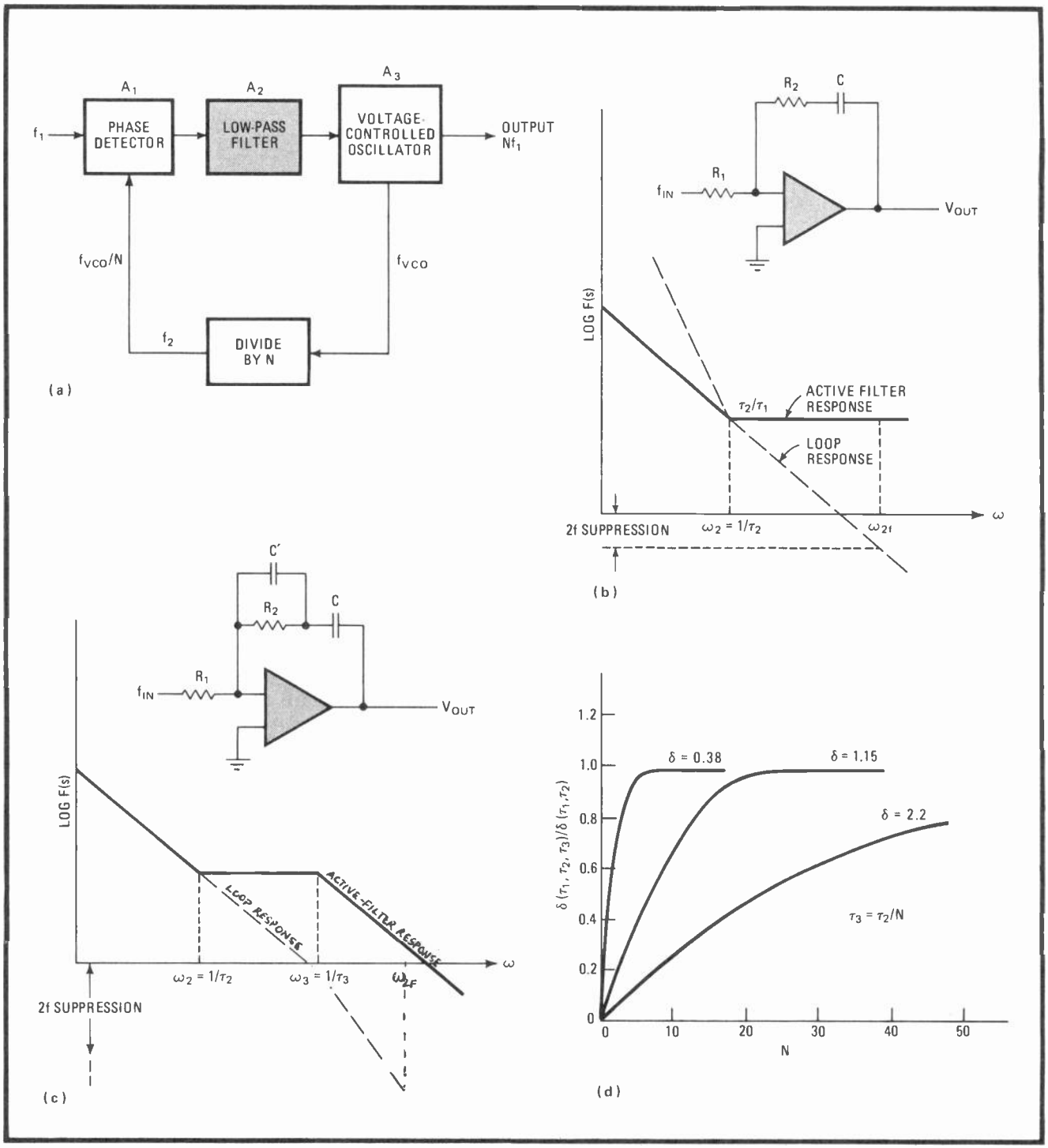
Note the corresponding curves of the filter's and PLL's open-loop response. If the harmonics in question are all above the added pole frequency, $\frac{1}{2}\pi\tau_3$, they will be attenuated because the magnitude of $F_3(s)$ will be less than that of $F_2(s)$. At ω_{2f} in (b), there is no additional suppression beyond whatever exists as a result of the low-pass filter and the integrating effects of the VCO. The attenuation of the unwanted harmonics is increased with the addition of C′.

It will be observed that adding C′ creates a network with certain third-order characteristics that under some conditions can be unstable. However, as long as the loop gain of the originally unconditionally stable second-order loop is unchanged after C′ is added and provided that the slope at which the loop's log-magnitude plot crosses the unity-gain axis does not exceed −40 dB per decade, the new loop will behave more like the second-order one from which it derived. Both conditions are normally met in practice.

Placement of the additional breakpoint affects the loop's damping factor, δ. As indicated in (d), the effects upon the damping start to become noticeable as τ_3 increases. From these curves, it is seen that a second-order loop with a damping of about a factor of 1 would have an approximately equivalent second-order damping of about 0.975 when $\tau_3 = \tau_2/20$.

As an example of how to use these curves as a design aid, consider a requirement for a PLL frequency multiplier with a damping factor of 1.2 and a bandwidth of 100 Hz. A standard second-order loop is designed to these specifications, but its output is found to contain excessive phase jitter (sideband noise). So a damping of 0.38, 1.15, or 2.2 is selected from (d) and the loop redesigned using the second-order equations customary in designing basic PLLs.

In this case, a damping factor of 2.2 is chosen. N, and hence C′, is determined by first calculating the ratio $R = \delta(\tau_1,\tau_2,\tau_3)/\delta(\tau_1,\tau_2)$. Given a required damping $\delta(\tau_1,\tau_2,\tau_3)$ of 1.2 and a desired damping $\delta(\tau_1,\tau_2)$ of 2.2, R = 0.55. From (d), N = 21.2 for R = 0.55. Then $\tau_3 = \tau_2/N$ and $C' = \tau_3R_2$. Placement of this value of C′ across R_2 in the loop's filter reduces the phase jitter to acceptable levels while maintaining the original damping and bandwidth requirements. □



Breakpoint. When operated as a frequency multipler, phase-iocked loop's phase detector (a) can generate harmonics that appear at circuit output. Conventional low-pass filter (b) cannot provide sufficient harmonic suppression. Incorporating capacitor C′ (c) adds break frequency to filter response, enables increased rejection of harmonics, and reduces PLL's phase jitter. Effects of τ_3 on second-order damping are plotted (d) to aid in design example discussed in text.

Digital voltmeter has audible output

by William S. Wagner
Northern Kentucky University, Highland Heights, Ky.

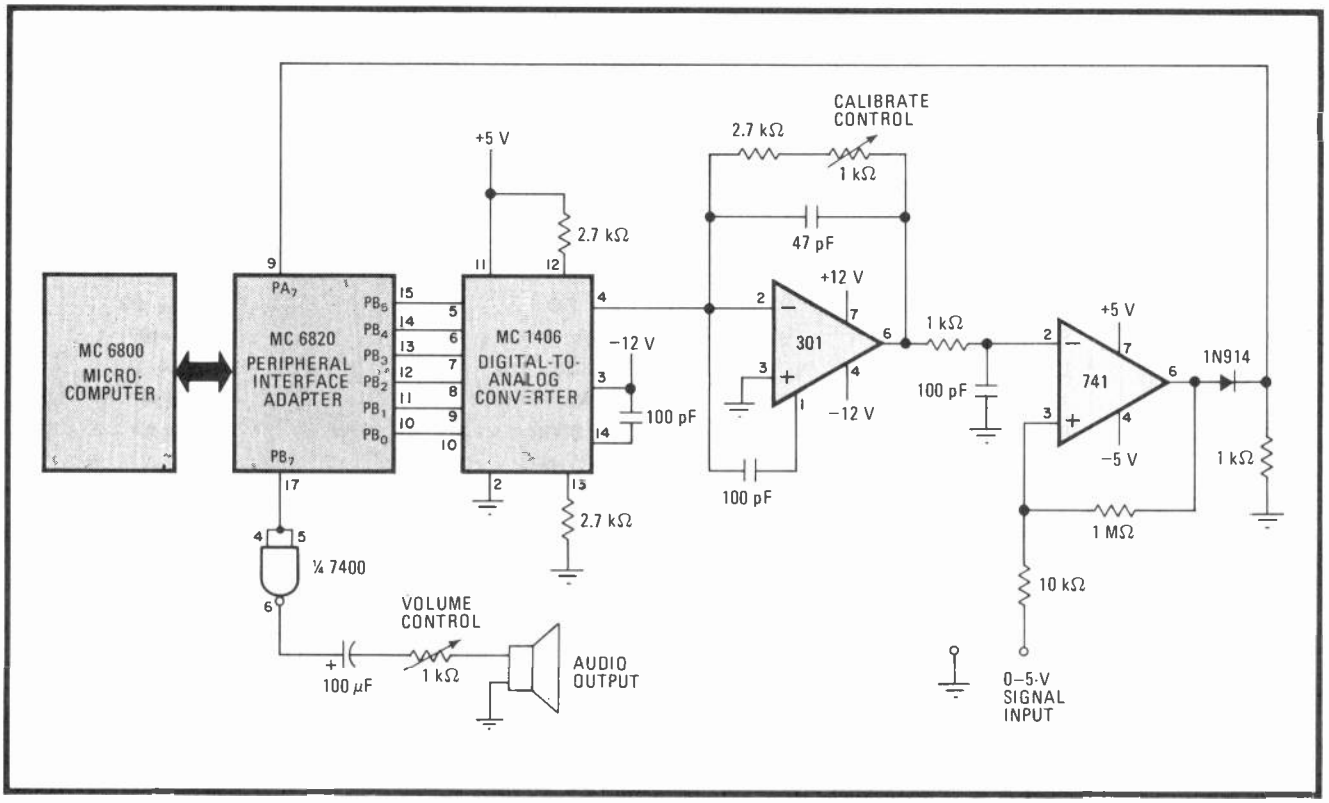
Using a program written for the 6800 microprocessor, and an appropriate interface, this system converts a 0-to-5-volt dc signal into an equivalent sequence of audio tones. Thus, the system will be particularly useful to visually handicapped technicians who troubleshoot logic circuits, as well as in applications where it is not practical to read the voltage from a standard voltmeter's display face.

The voltage to be measured is converted to a series of tones of short duration (dits) to represent quantities extending from 1 to 9. The quantity 0 is represented by a single tone (dah) of relatively long duration. A decimal point is represented by a pause. Thus, for example, 2.5 V yields an equivalent audio output of dit-dit, pause, dit-dit-dit-dit-dit. An 0.3-V signal yields dah, pause, dit-dit-dit. And a 4.0-V signal generates dit-dit-dit-dit, pause, dah. The resolution of the measurement is about 0.1 V.

As implied in the figure, the 6-bit MC 1406 digital-to-analog converter is used in a feedback loop with the 741 operational amplifier for tone generation. The dc input signal is compared to the voltage at the inverting port of the 741. If there is a voltage difference, the digital input to the MC 1406 is adjusted, under program control, until the voltage difference is minimized. The binary word at the output of the MC 6820 peripheral-interface adapter then represents the dc voltage, and is converted to an audio output by the remainder of the program. The frequency and length of the individual tone, the time interval between digits, and the rate at which the dc input signal is sampled are all controlled by the software.

The program requires 250 bytes of memory. The first four instructions initialize the program. The instructions contained between addresses 000C and 00021 comprise the digital-voltmeter part of the routine. Steps 0012 through 0016 set a built-in delay in order to allow the analog portion of the interface sufficient time to update. The instructions commencing at 0018 cause the program to jump to the audio portion of the program (addresses 0023 through 00A0) when the aforementioned match of input and d-a voltages occurs.

In the analog part, the dc voltage is converted to a final 6-bit binary-coded word and stored in an accumulator. Each bit is checked to see whether it is a 0 or an



Potential cure. Microprocessor-based system transforms logic-range voltages into coded series of audio tones for technicians who are unable to observe standard voltmeters. The resolution of the measurements, limited by interface's d-a converter, is 0.1 volt.

6800 PROGRAM FOR AUDIO VOLTMETER					
Address	Mnemonic	Address	Mnemonic	Address	Mnemonic
0000	LDX 0004	005C	BNE F7	010C	BNE FD
0003	STX 8000	005E	PULA	010E	DEX
0006	LDX FF04	005F	PSHA	010F	BEQ 03
0009	STX 8002	0060	ANDA F0	0111	COMB
000C	LDB FF	0062	BEQ 3F	0112	BRA F0
000E	CLRA	0064	PULA	0114	LDX 1FFF
000F	STAB 8002	0065	ASLA	0117	DEX
0012	LDX 0055	0066	PSHA	0118	BNE FD
0015	DEX	0067	BCS 11	011A	PULA
0016	BNE FD	0069	PULA	011B	DECA
0018	TST 8000	006A	ASLA	011C	BNE E2
001B	BPL 06	006B	PSHA	011E	RTS
001D	DECB	006C	BCS 13	0120	LDX 03FF
001E	ADDA 01	006E	PULA	0123	ORAB 7F
0020	DAA	006F	ASLA	0125	STAB 8002
0021	BRA EC	0070	PSHA	0128	LDAA 25
0023	LDS 00B0	0071	BCS 15	012A	DECA
0026	PSHA	0073	PULA	012B	BNE FD
0027	ANDA 70	0074	ASLA	012D	DEX
0029	BGT 03	0075	PSHA	012E	BEQ 03
002B	JMP 0120	0076	BCS 17	0130	COMB
002E	PULA	0078	BRA 1A	0131	BRA F0
002F	ASLA	007A	LDA 08	0133	PULA
0030	ASLA	007C	JSR 0100	0134	ASLA
0031	PSHA	007F	BRA E8	0135	ASLA
0032	BCS 0C	0081	LDA 04	0136	ASLA
0034	PULA	0083	JSR 0100	0137	ASLA
0035	ASLA	0086	BRA E6	0138	PSHA
0036	PSHA	0088	LDA 02	0139	JMP 0053
0037	BCS 0E	008A	JSR 0100	0140	LDX 03FF
0039	PULA	008D	BRA E4	0143	ORAB 7F
003A	ASLA	008F	LDA 01	0145	STAB 8002
003B	PSHA	0091	JSR 0100	0148	LDAA 25
003C	BCS 10	0094	LDAA 02	014A	DECA
003E	BRA 13	0096	LDX FFFF	014B	BNE FD
0040	LDA 04	0099	DEX	014D	DEX
0042	JSR 0100	009A	BNE FD	014E	BEQ 03
0045	BRA ED	009C	DECA	0150	COMB
0047	LDA 02	009D	BNE F7	0151	BRA F0
0049	JSR 0100	009F	PULA	0153	PULA
004C	BRA EB	00A0	JMP 000C	0154	ASLA
004E	LDA 01	00A3	JMP 0140	0155	ASLA
0050	JSR 0100	0100	PSHA	0156	ASLA
0053	LDAA 01	0101	LDX 00FF	0157	ASLA
0055	LDX FFFF	0104	ORAB 7F	0158	PSHA
0058	DEX	0106	STA 8002	0159	JMP 0094
0059	BNE FD	0109	LDAA 25		
005B	DECA	010B	DECA		

integer from 1 to 9, so that it can be determined if short or long tones are to be produced by the dit and dah subroutines, respectively. The instructions commencing at 0053 sets a time interval between the processing of the first and second integers of the measured voltage, and the instructions starting at 0094 set the time interval between readings, or samples.

The actual short-tone subroutine extends from addresses 0100 to 011E. The instructions specified from 0101 to 010F determines the length and frequency of the

short tones. Addresses 0114 through 0118 set the time interval between dits.

There are two subroutines for the generation of long tones. One is called (address 0120) when the first integer of the voltage measured is 0. The second is called (0140) where the second integer is 0. Both contain instructions for setting the length and frequency of the long tone. □