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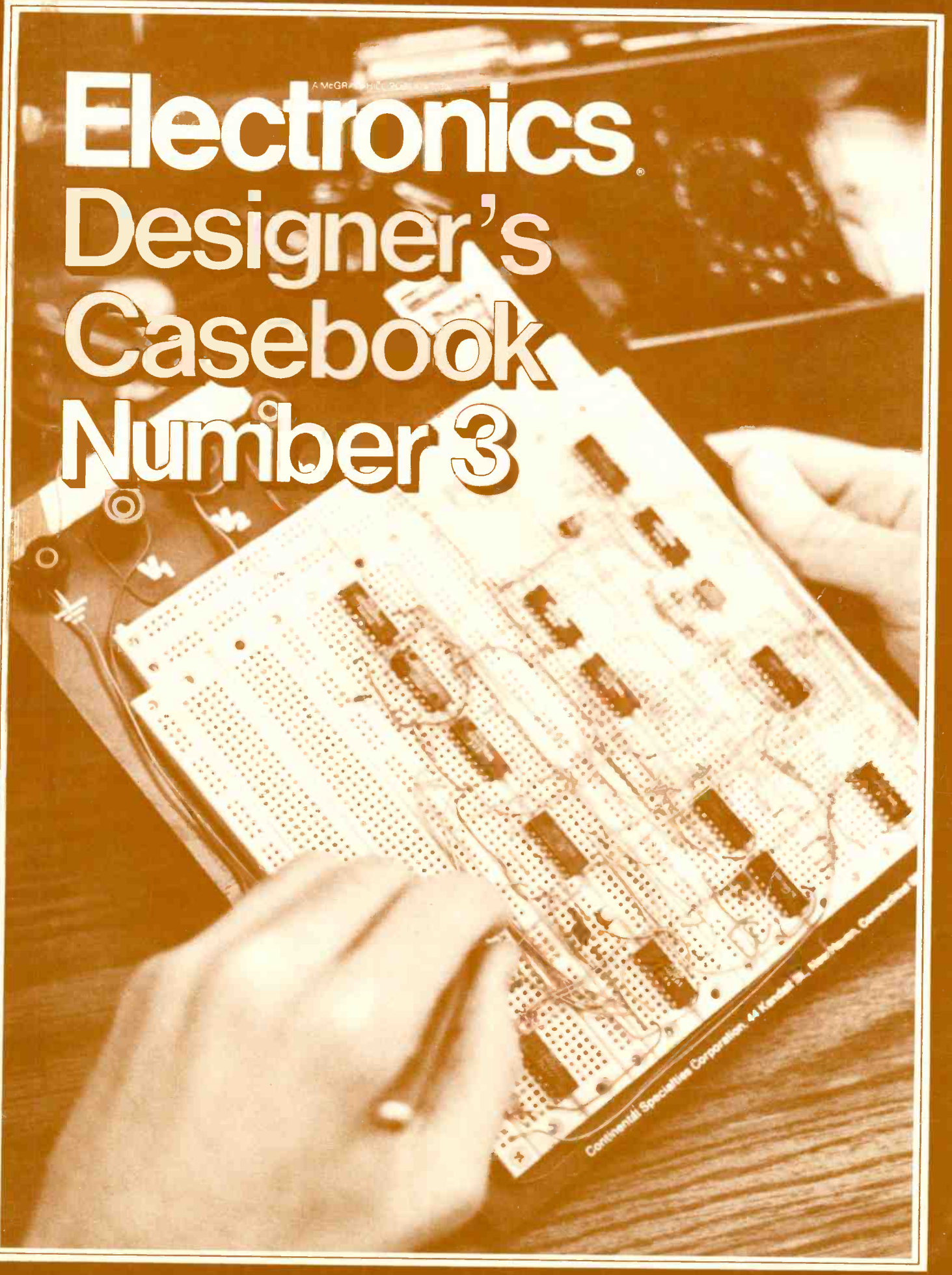

DESIGNER'S CASEBOOK

PREPARED BY
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Electronics

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EPROM achieves nonuniform data-channel sampling

by B. Bowles and T. U. Nelson
Chamber of Mines of South Africa, Johannesburg

In some multiplexed data-acquisition systems, adequate bandwidth is not always available for transmitting every channel at the rate required by the fastest channel. It is therefore necessary to sample some channels at a higher speed than others, each at a rate equal to at least twice its highest frequency. A nonuniform sampler circuit is thus required.

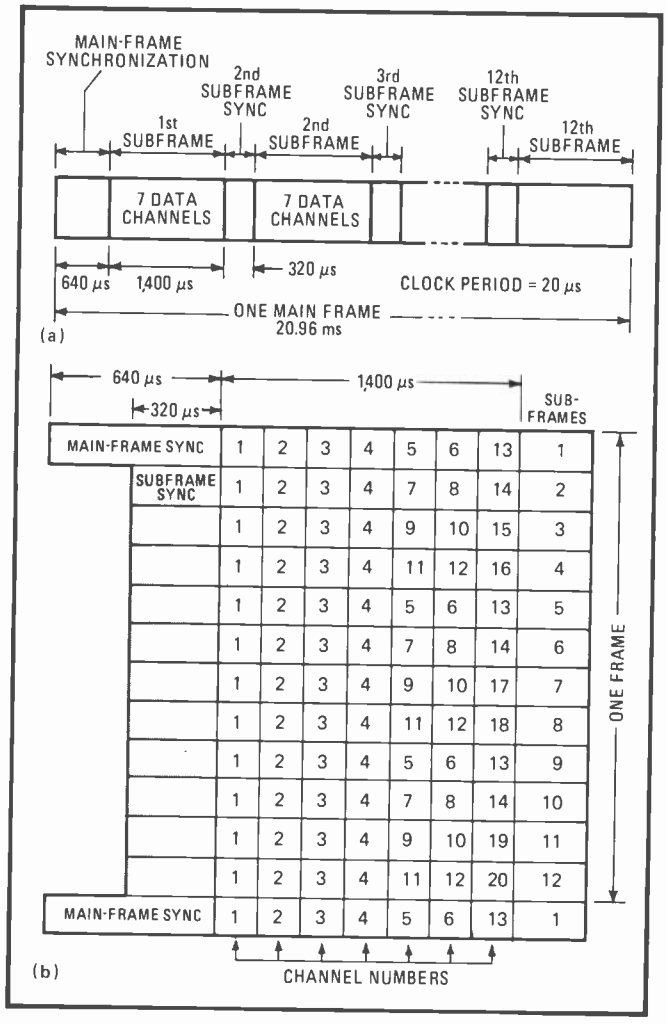
A circuit built with an erasable programmable read-only memory forms an effective nonuniform sampler. The erasable PROM is programmed so that a sequential scan of its memory locations results in the selection of a channel sequence determined by the bandwidth requirements of each channel. In this way, the transmission rate of any channel is made proportional to its bandwidth. Using the erasable PROM and the associated circuitry to generate the sequence is more practical than using the usual array of analog switches or the well-known shift-register–diode-matrix circuit, especially when the number of channels is large or the sequence is complex.

To understand the design problem, first consider the channel format for a typical multiplexed pulse-code-modulation system as shown in Fig. 1a. Each analog channel of this 20-channel system requires 10 clock periods—8 clock periods for quantizing a data word, plus 2 clock periods preceding the word that are required for internal timing in the circuit processing the data. Any 7 of the 20 channels are periodically multiplexed as a block, or subframe. Twelve such subframes form one main frame, as shown. Since each subframe, except the first, is preceded by a synchronization pulse 16 clock periods long, and if the clock frequency is assumed to be 50 kilohertz (period of 20 microseconds), the sync time will be 320 μs. The mainframe sync pulse occurring before subframe 1 is 32 clock periods, or 640 μs, long. It takes 200 μs to sample each channel or, equivalently, 1,400 μs to sample each subframe.

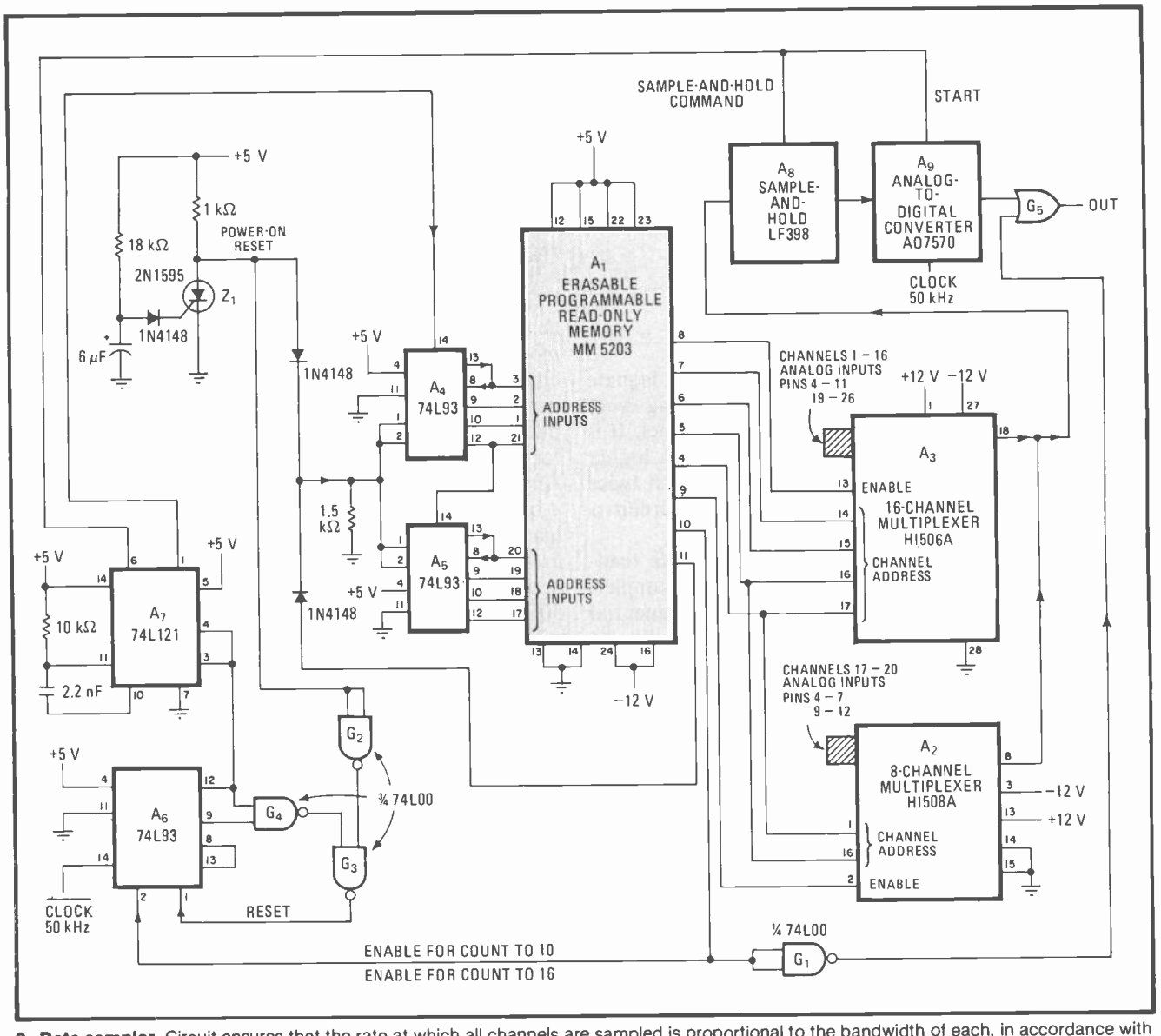
In this case, each channel has the following bandwidth: channels 1 through 4, 163 Hz; channels 5 through 14, 47 Hz; and channels 15 through 20, 16 Hz. Note that the total frame time, about 21 milliseconds, is three times greater than the highest bandwidth of any channel sampled, to prevent fold-over distortion (from sampling theory, 2 is the minimum ratio required). With this arrangement, the sampling rate of channel 1 through channel 4 will be 4 times that of channels 5 through 14 and will be 13 times that of channels 15 through 20, as shown in Fig. 1b.

The format can be realized by the circuit shown in Fig. 2 if the PROM is programmed, beginning at location 3, with the channel numbers shown in Fig. 1b. Programming proceeds from left to right, subframes 1 to 12. Both locations 1 and 2 of the PROM, each representing a subframe, and the programming of certain nondata bits are subject to special considerations, which will be discussed shortly.

Circuit operation is easily explained. Basically, any of 20 channels is selected by sending the channel number from the 256-word-by-8-bit erasable PROM (A_1) to the address inputs of an 8- and a 16-channel multiplexer (A_2 and A_3, respectively). The contents of each channel are then passed to the output of the circuit in prescribed order. The first 16 channels are handled by A_3, the remaining four by A_2.



1. Data format. Typical requirements for a multiplexed PCM system are shown. Any 7 channels of this 20-channel system are multiplexed in 12 subframes, such that the sampling rate of each channel is proportional to its bandwidth (a). Transmission format for this system (b) can be found once the channel bandwidths are known (see text). Data sampler can generate this or any other format desired.



2. Data sampler. Circuit ensures that the rate at which all channels are sampled is proportional to the bandwidth of each, in accordance with the requirements of sampling theory. The erasable PROM can be programmed so that any desired channel sequence can be transmitted via the 16-channel multiplexer; the transmission rate for each channel will in this way be easily controlled.

On power up, thyristor Z_1 resets counters A_4 through A_6, thereby selecting the first PROM location. A_4 and A_5 will be placed in the standby mode and A_6 will be placed in the count-to-16 mode, because the PROM is programmed to generate a logic 0 at pin 10 of A_1. When Z_1's anode voltage drops to zero, A_6 begins to count, and this initiates the master sync cycle.

After 16 counts, the one-shot (A_7) fires and increments A_4, and therefore the second memory location of the PROM is selected. The second location is programmed so that its contents are identical to that of location 1, and consequently, 16 counts later, the third memory location is selected. This location contains the address of the first multiplexer channel.

Pin 10 of A_1 has moved high, thereby enabling G_5, and setting A_6 into its count-to-10 mode. Note that the multiplexers are addressed by 6 bits of A_1, not 8; the remaining 2 bits are required for the system sync-control circuit comprising G_1, G_5, and pin 10 of A_6.

Meanwhile the one-shot initiates the sample-and-hold command and resets A_9. The contents of channel 1 then appear at the input of A_9. At the second positive clock edge after the cessation of the pulse emanating from A_7, the most significant bit of data appears at the output of A_9 and thus at the circuit output. A_3 is now in the count-to-10 mode (caused by pin 11 being high). A_4 and A_5 are again incremented by A_7 after the monostable is triggered by pulse 10 of A_1. A_5 and A_6 select the next PROM address, which is 2 in this case. This process is repeated until all seven channels have been selected.

At the next memory location, the PROM must be programmed so that a 0 once again emanates from pin 10, to set A_6 into the count-to-16 mode once more and to generate a logic 1 at the system output by means of G_1 and G_5. Triggering A in this way sets the stage for the generation of a subframe sync pulse and the selection of the first channel in the second subframe after 16 pulses have been counted by A_1. The selection process continues

until all the subframes have been scanned.

The location representing subframe 12 should be programmed so that a logic 1 appears at pin 11. This resets the counters and selects the first memory location in A_1, as before. The system generates the main-frame sync pulse again and the entire process is repeated. □

Phase-locked generator converts, filters most inputs

by Peter Reintjes
Research and Design Ltd., Morehead City, N. C.

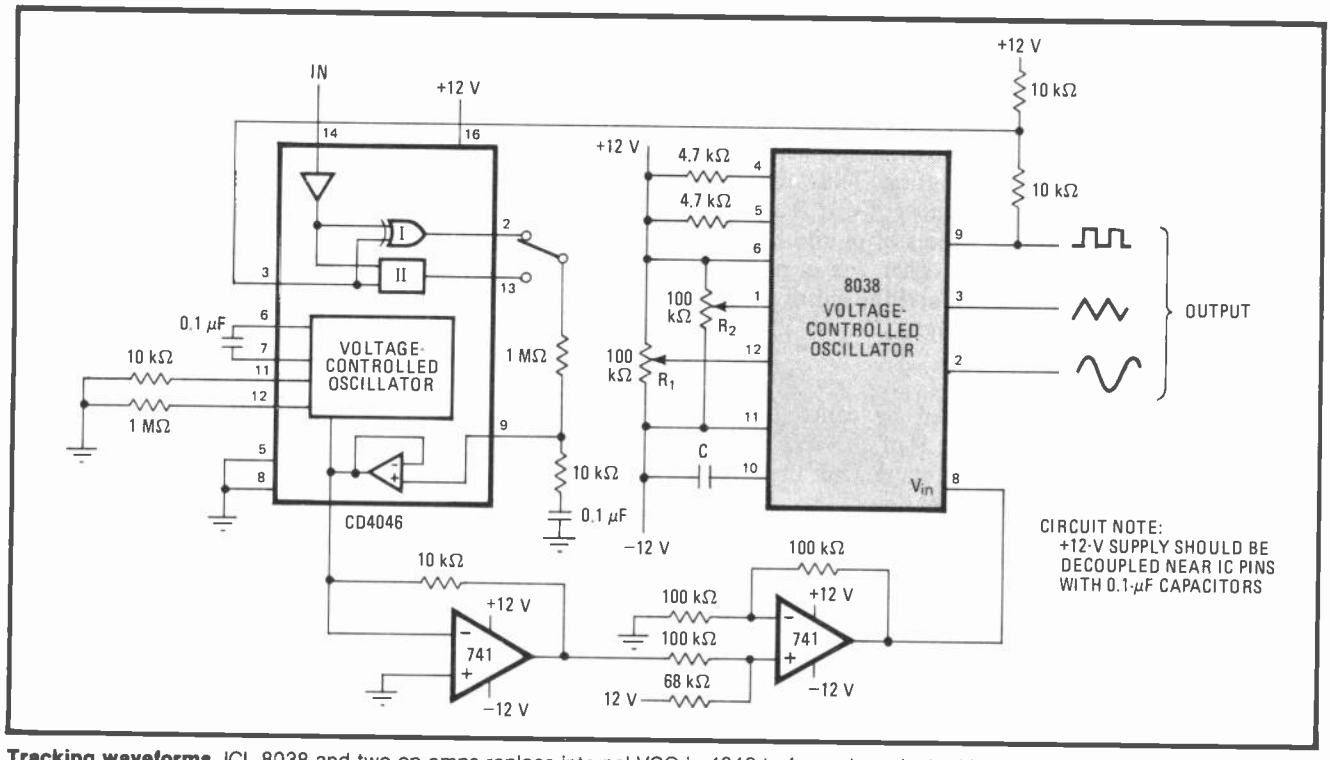
Replacing the voltage-controlled oscillator in the RCA 4046 phase-locked loop with the popular Intersil 8038 waveform generator forms a circuit that produces sine, square, and triangular wave voltages capable of tracking almost any input signal. Besides performing its prime function of waveform conversion, the circuit serves as a high-Q filter. With a harmonic distortion of only 0.5%, it finds the fundamental frequency of any signal.

The performance of this circuit far exceeds that of a conventional filter, which always adds a phase shift to the incoming signal. Also, traditional filtering methods are often of little use when the fundamental frequency must be recovered from an unpredictable input signal.

Connecting the 8038, which is itself a voltage-controlled oscillator, to the 4046 as shown in the figure does not affect the normal operation of the phase-locked loop. The only difference in the basic PLL circuit is that the 8038 generates sine, triangular, and square waves and drives the 4046 in place of the loop's internal VCO. The output waveshapes are unaffected by the harmonic distortion present on the input signal. Capacitor C sets the center frequency of the 8038 (a value of 0.047 microfarad corresponds to a frequency in the audio range). The frequency-capture range of the circuit, which is determined by the 4046, remains 1,000 to 1. The generator's maximum operating frequency is about 700 kilohertz.

To secure precise locking, the comparators in the 4046 should be driven by the square-wave output of the 8038. If the input waveform is a pulse, phase comparator I should be used. For unpredictable or high-noise signals, phase comparator II is more suitable.

Any phase difference between the square-wave output of the 8038 and the input signal is amplified by two 741 operational amplifiers and then fed back to the VCO to increase or decrease its frequency, as the case may be. Although the internal VCO of the 4046 is not used, it must be enabled by grounding pin 5 of the device so that its voltage-follower will be active. If matched resistors are used at pin 4 and 5 of the 8038, the sine-wave output distortion can be reduced to 0.5%. Potentiometers R_1 and R_2 aid in minimizing the distortion. □



Tracking waveforms. ICL 8038 and two op amps replace internal VCO in 4046 to form phase-locked-loop waveform generator that can be used to recover fundamental frequency of any input signal or to convert the control signal to sine, square, and triangular waves. The generator's maximum output frequency is about 700 kHz. R_1 and R_2 are adjusted for minimum output distortion.

Programmed module automates transducer's linearization

by C. Viswanath
Indian Institute of Science, Bangalore, India

As a consequence of its unusual transfer function, the Analog Devices 433 J/B programmable multifunction module finds wide use in performing vector operations, generating trigonometric functions, raising a number to an arbitrary power, and linearizing the response of transducers used in medical and industrial electronics.

The module's transfer function is:

$$e_o = \frac{10}{9} V_y \left(\frac{V_z}{V_x}\right)^m = P \qquad 0.2 \leq m \leq 5.0$$

Programming of the exponent, m, contained in the transfer function, which is necessary to generate the required operations, is done more quickly and accurately with a digital-to-analog converter and two field-effect transistors than with a potentiometer, the component most often used. Digital selection of the exponent is particularly useful where an automatic test sequence must be generated from a microprocessor to multiplex several transducers, each requiring a different m. With this circuit, the value of m may be adjusted throughout the entire specified range, in increments of 0.1.

A circuit used for transducer linearization is shown in the figure. The technique used for linearizing a transducer's transfer function (Q) is to control m so that it varies inversely with the known exponent (n) contained within the transducer's characteristic equation. Thus, when the output voltage from the transducer $(V_z)^n$ has been processed by the 433 J/B, the effects of m and n on the output voltage will cancel each other (as a result of multiplying P and Q to obtain e_o), and the entire transfer function is then simply expressed by:

$$e_o = K V_z$$

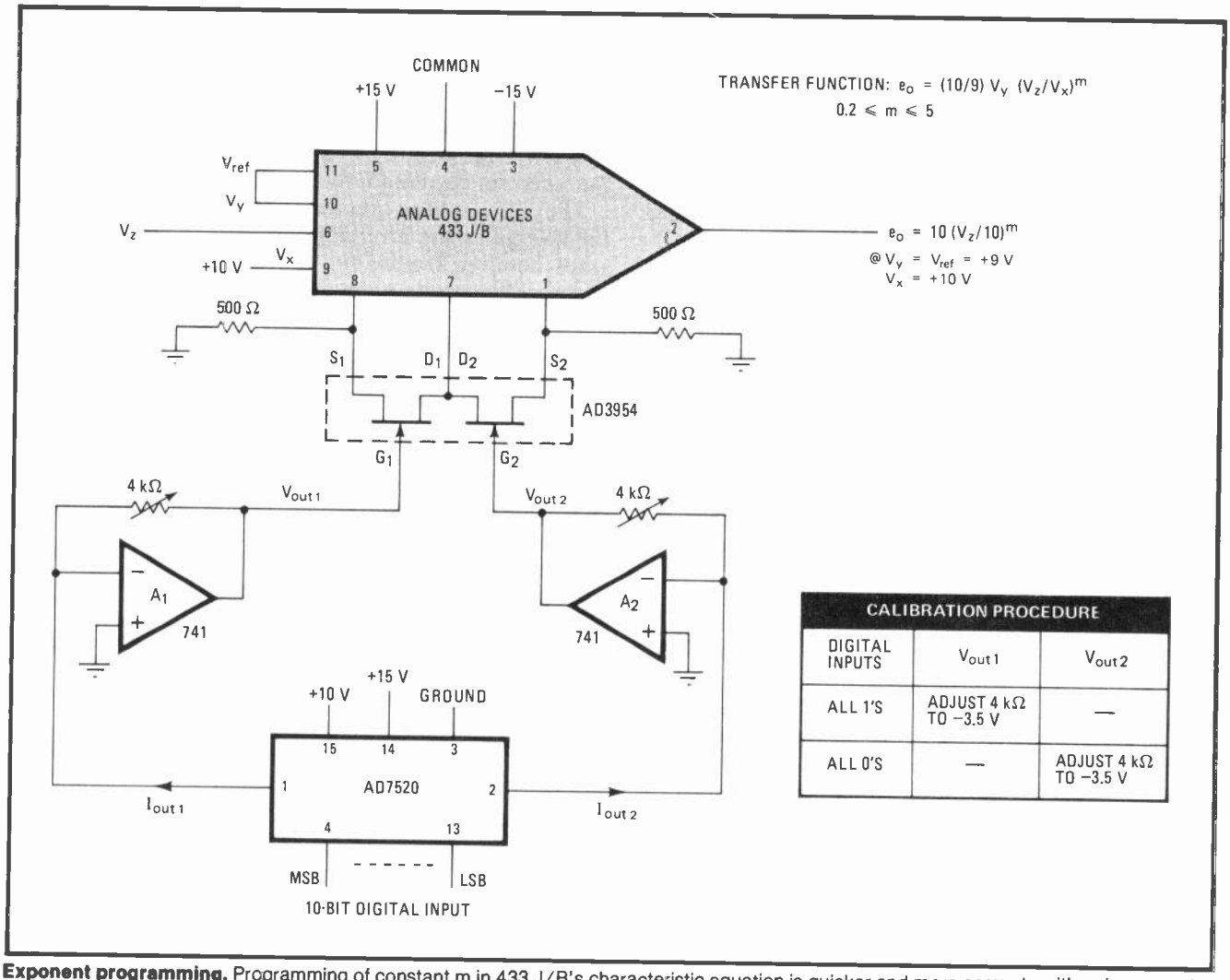
The value of m is programmed by controlling the resistance between pins 1, 7, and 8 of the 433 J/B by means of the AD3954 dual-FET stage and the 10-bit AD7520 d-a converter. The combination of the converter and the dual FETs is thus intended to serve as a digitally controlled potentiometer.

Two binary-weighted current sources, the magnitudes of which are dependent on the 10-bit input and the sum of which is constant (equal to I_{out1} plus I_{out2}), drive operational amplifiers A_1 and A_2. The magnitude of I_{out1} and I_{out2} are determined by the reference voltage at pin 15 of the converter.

A_1 and A_2 convert the currents to voltages V_{out1} and V_{out2}, respectively, and drive the gates of the dual FET. The FETs operate as voltage-controlled resistors and are

PROGRAMMING OF EXPONENT M

M	DIGITAL INPUT MSB LSB
0.2	0000000000
0.3	0000010100
0.4	0000101010
0.5	0001000000
0.6	0001010100
0.7	0001101010
0.8	0010000000
0.9	0010010100
1.0	0010101010
1.1	0011000000
1.2	0011010100
1.3	0011101010
1.4	0100000000
1.5	0100010100
1.6	0100101010
1.7	0101000000
1.8	0101010100
1.9	0101101010
2.0	0110000000
2.1	0110010100
2.2	0110101000
2.3	0111000000
2.4	0111010100
2.5	0111101010
2.6	1000000000
2.7	1000010100
2.8	1000101010
2.9	1001000000
3.0	1001010100
3.1	1001101010
3.2	1010000000
3.3	1010010100
3.4	1010101010
3.5	1011000000
3.6	1011010100
3.7	1011101010
3.8	1100000000
3.9	1100010100
4.0	1100101010
4.1	1101000000
4.2	1101010100
4.3	1101101010
4.4	1110000000
4.5	1110010100
4.6	1110101010
4.7	1111000000
4.8	1111010100
4.9	1111101010
5.0	1111111111



CALIBRATION PROCEDURE		
DIGITAL INPUTS	$V_{out\,1}$	$V_{out\,2}$
ALL 1'S	ADJUST 4 kΩ TO −3.5 V	—
ALL 0'S	—	ADJUST 4 kΩ TO −3.5 V

Exponent programming. Programming of constant m in 433 J/B's characteristic equation is quicker and more accurate with a d-a converter and FETs that operate as voltage-controlled resistors than with a potentiometer. This circuit linearizes the response of transducer voltage V_z if the 433 J/B is programmed so that m is the inverse of exponent value n contained in the transducer's transfer function.

selected to provide good tracking throughout the 0-to-−3.5-volt input-voltage range.

If all 10 bits of the AD7520 are set to logic 1, corresponding to an m value of 5.0, $I_{out\,1}$ will equal 1 milliampere, and $I_{out\,2}$ will equal 0. Thus $V_{out\,1}$ should be set to a full-scale output (−3.5 v), and $V_{out\,2}$ should be set to 0. Similarly, $V_{out\,1}$ must be set to 0, and $V_{out\,2}$ to −3.5 v, when all inputs are set to logic 0, corresponding to an m of 0.2. The 4-kilohm potentiometers are provided for calibration purposes.

The table outlines the inputs to the d-a converter required for any value of m from 0.2 to 5. □

Dc-dc power supply has reference-unit stability

by J. Brian Dance
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The stability of the voltages generated by adjustable dc-dc power supplies is usually no greater than ±100 millivolts, even when the voltages are derived from fixed-voltage regulators. In cases where extreme stability is sought, it is best to design a circuit that utilizes a voltage-reference source instead. Such a circuit, shown in the figure, can provide a 0-to-20-volt output that is within ±5 millivolts of the set value and virtually independent of the current drawn by the load. The supply delivers a maximum of about 1.5 amperes, has a built-in thermal shutdown safeguard, and is protected against short-circuit conditions.

The Precision Monolithics REF-01 voltage reference unit in the circuit provides an extremely stable 10 v across a 10-turn helical potentiometer, R_1, as shown in the figure. This pot, which has a calibrated vernier, sets the output voltage, which will always be equal to twice the value of any voltage derived from the reference source. The linearity of the potentiometer is 0.1%, and

this ensures that the output voltage may be set to within a few millivolts of its desired value. For verniers with a scale of 0 to 10, the output voltage will be equal to twice the vernier reading once the entire circuit is calibrated.

R_2 is included in the circuit for trimming purposes. It is used to calibrate R_1 at an output voltage of 10 v. If the gain-controlling elements in the circuit, R_3 and R_4, are close-tolerance components, trimming may be neglected. If R_2 is omitted, and R_3 and R_4 have a 5% tolerance, the voltage at pin 6 of the REF-01 will be within 50 mv of 10 v.

The slider arm of R_1 drives the noninverting port of the LM358 operational amplifier, which operates in the linear region even though it uses only a single-source supply. The gain between the input of the op amp and the output of the circuit is equal to 1 + (R3/R4). Thus the voltage appearing at the output of the LM295K amplifier is twice the value of the voltage appearing at the input of the op amp; since the input voltage is a function of a stable reference, the output voltage is also stable.

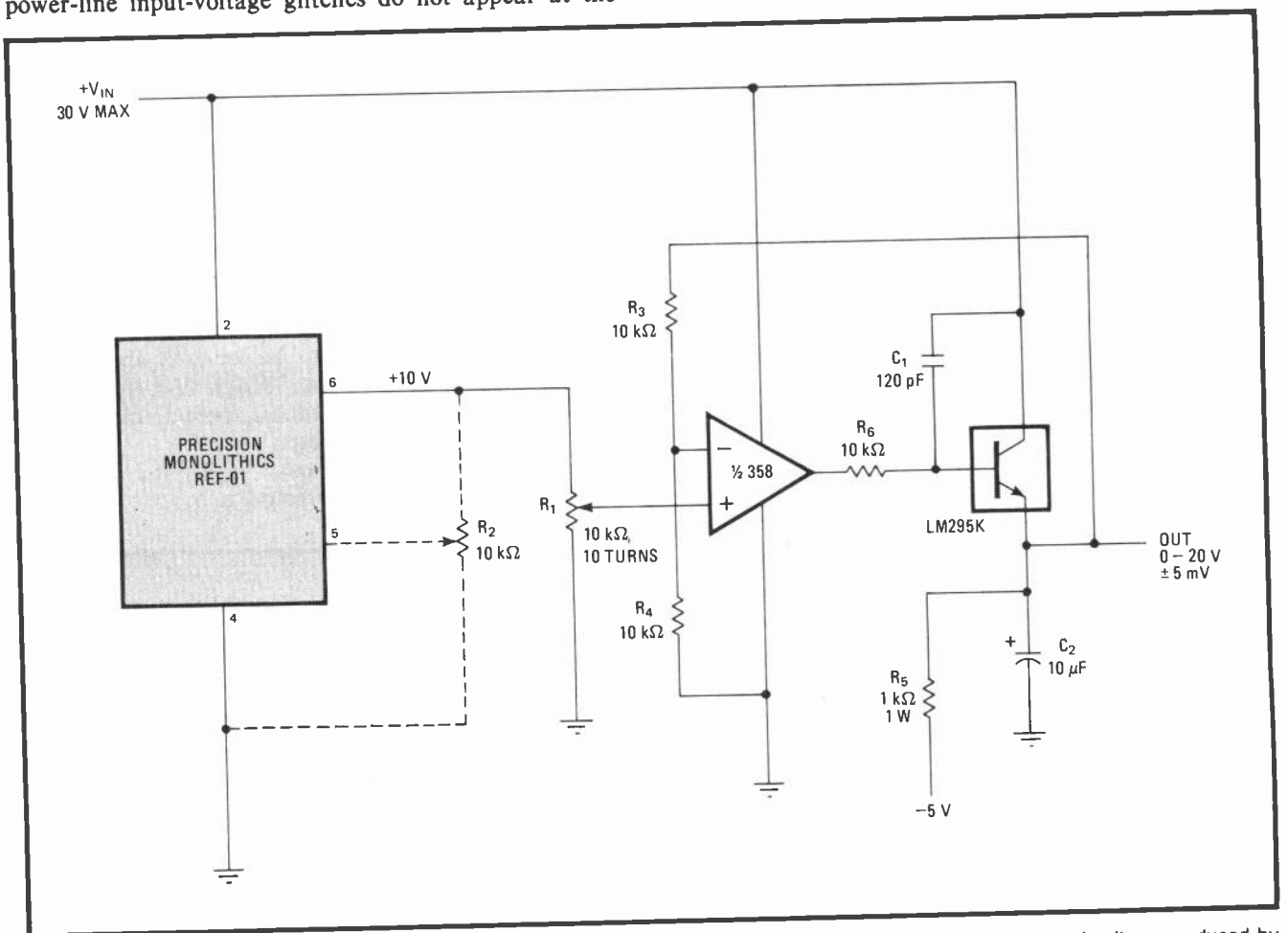
The LM295K, although shown as a single transistor element in the figure, is actually a high-gain linear power amplifier. Its open-loop gain is 1 million, and it is capable of delivering a maximum of 1.5 A to the load.

C_1 and C_2 are added to the circuit to ensure that power-line input-voltage glitches do not appear at the output or cause unwanted oscillations. R_5 provides a path for the amplifier's quiescent current flow; if it is omitted, the output voltage will climb to 9 v at R_1's minimum setting. The use of a −5-v bias supply can be avoided if R_5 is connected to ground, but the minimum output voltage will rise to approximately the product of the quiescent current (5 mA maximum) and R_5.

The 358 amplifier operates in the linear region even if the voltage at the inverting port falls to zero. Most op amps, however, require bias from a dual supply (positive and negative voltages) in order to operate in the linear region, and this fact should be considered when contemplating the use of a different op amp.

A current of 1 A taken from the output port produces a voltage change of less than 1 mv. A change of 10 v on the power-line input voltage results in only a 10-mv change at the output, and this figure can be reduced even further by placing a suitable resistor in series with pin 2 of the REF-01 and the supply voltage and connecting a 15-v zener diode from pin 2 to ground.

The temperature stability of the circuit has not been measured, but, depending on the class of REF-01 used, it will lie in the range of 3 to 20 parts per million per °C. Output noise at very low frequencies is extremely small. □



Precision. Rock-stable voltage reference source enables generation of extremely stable output voltages. Current and voltage produced by REF-01 source is independent of load current demands; thus output voltage, once set, will not vary more than ±5 millivolts.

Scanned keyboard activates eight-tone generator

by Albert Helfrick
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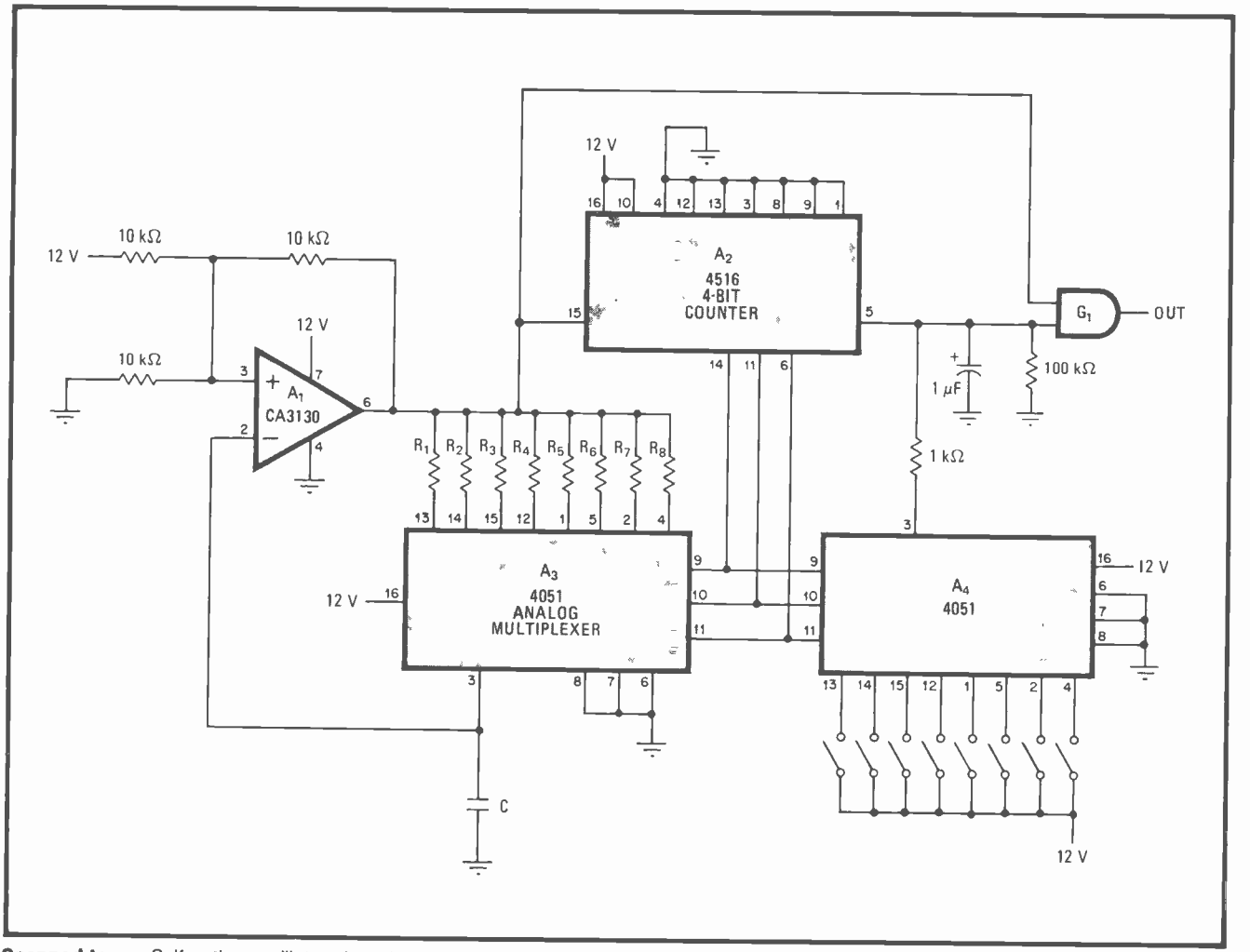
This keyboard-activated eight-tone generator owes its simplicity to a single oscillator, which makes possible the scanning of the keyboard and simultaneously functions as the tone generator. As a result, its device count is low and its cost is minimal.

Circuit operation is easily understood. The CA3130 operational amplifier, A_1, is configured as a relaxation oscillator, its frequency controlled by R_iC. R_i lies in the 100-to-500-kilohm range, and C is 0.01 microfarad or so for frequencies in the 1-to-10-kilohertz range. The oscillator has excellent frequency stability as a result of the operational amplifier's extremely high input impedance and the complementary-metal-oxide-semiconductor output circuit.

A_1 drives the 4516 4-bit counter, A_2. As the counter increments, it scans each input port of two analog multiplexers, A_3 and A_4. A_3 sequentially places all resistors, R_1 through R_8, in the oscillator circuit, enabling A_1 to generate exactly one cycle of each frequency determined by each R_iC combination. At no time is there any output from G_i, however.

Meanwhile, multiplexer A_4 is scanned to determine whether any keyboard switches are closed. If any switch should be depressed, a logic 1 will emanate from pin 3 of A_4, freezing the counter and enabling G_1. A_1 will then oscillate at the frequency determined by the particular value of R that is in the oscillator circuit when the counter halts. Since the counter cannot advance while the key switch is closed, and simultaneously closing any



Scanned tones. Self-gating oscillator, A_1, advances counter and with aid of multiplexer A_3 sequentially places R_1–R_8 in series with C so as to control frequency. Op amp's high-input impedance and C-MOS output ensures high oscillator stability. No signal appears at output until a keyboard switch is closed, when A_4 freezes counter and activates G_1, enabling generation of the single desired frequency.

other key will have no effect on the output frequency, the circuit has in effect a built-in lock-out feature.

The time required for the system to latch to any particular frequency is a function of both the number of frequencies that can be selected and the actual frequencies of oscillation. The maximum acquisition time works out to approximately:

$$t = \frac{1}{f_1} + \frac{1}{f_2} + \ldots \frac{1}{f_i}$$

where each f_i is equal to $1/0.69\ R_iC$. For eight frequencies in the kilohertz range, t equals about 8 milliseconds, which is an acceptable period of time for manual keystroke applications. □

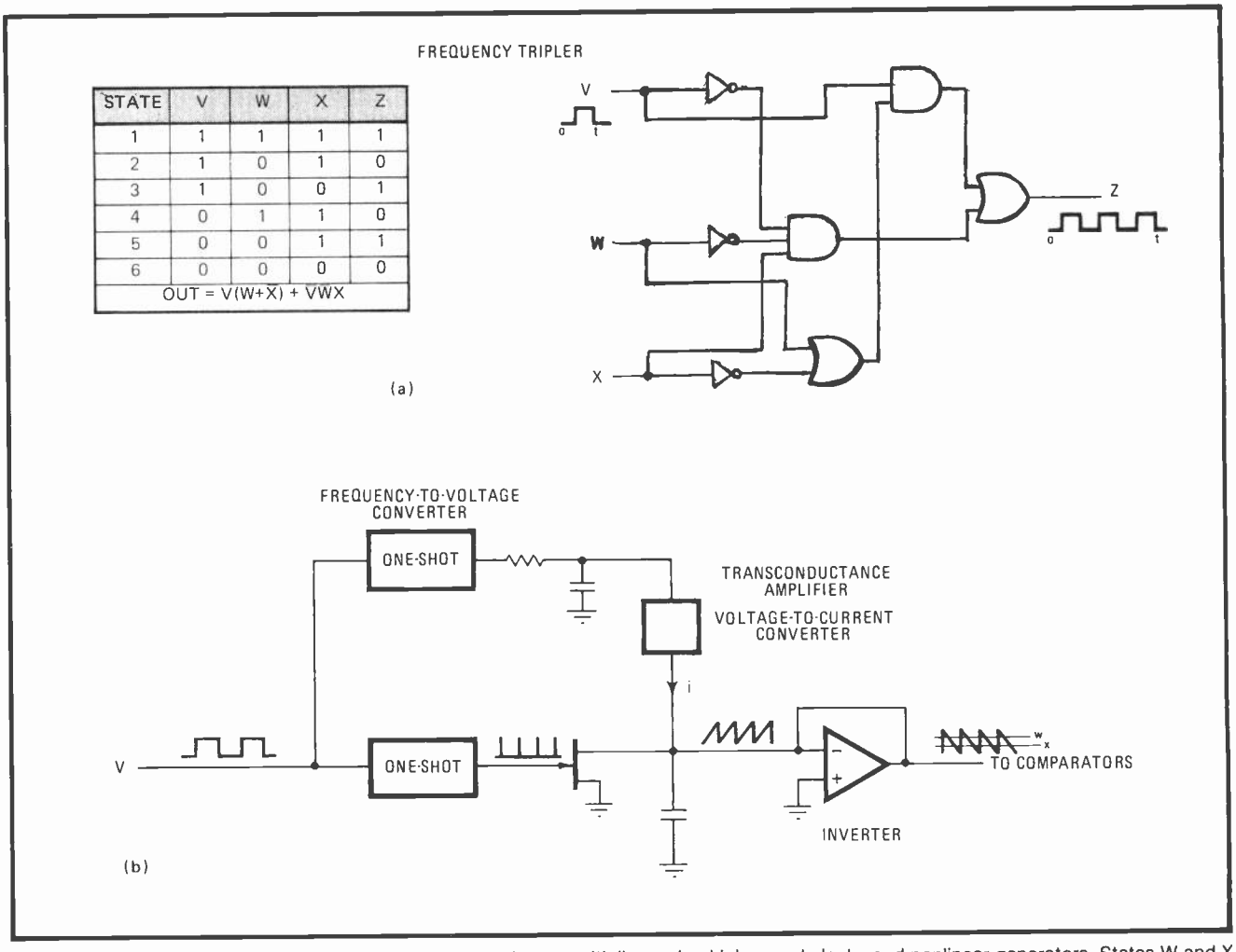
Frequency multiplier uses combinational logic

by R. J. Patel
Tata Institute of Fundamental Research, Bombay, India

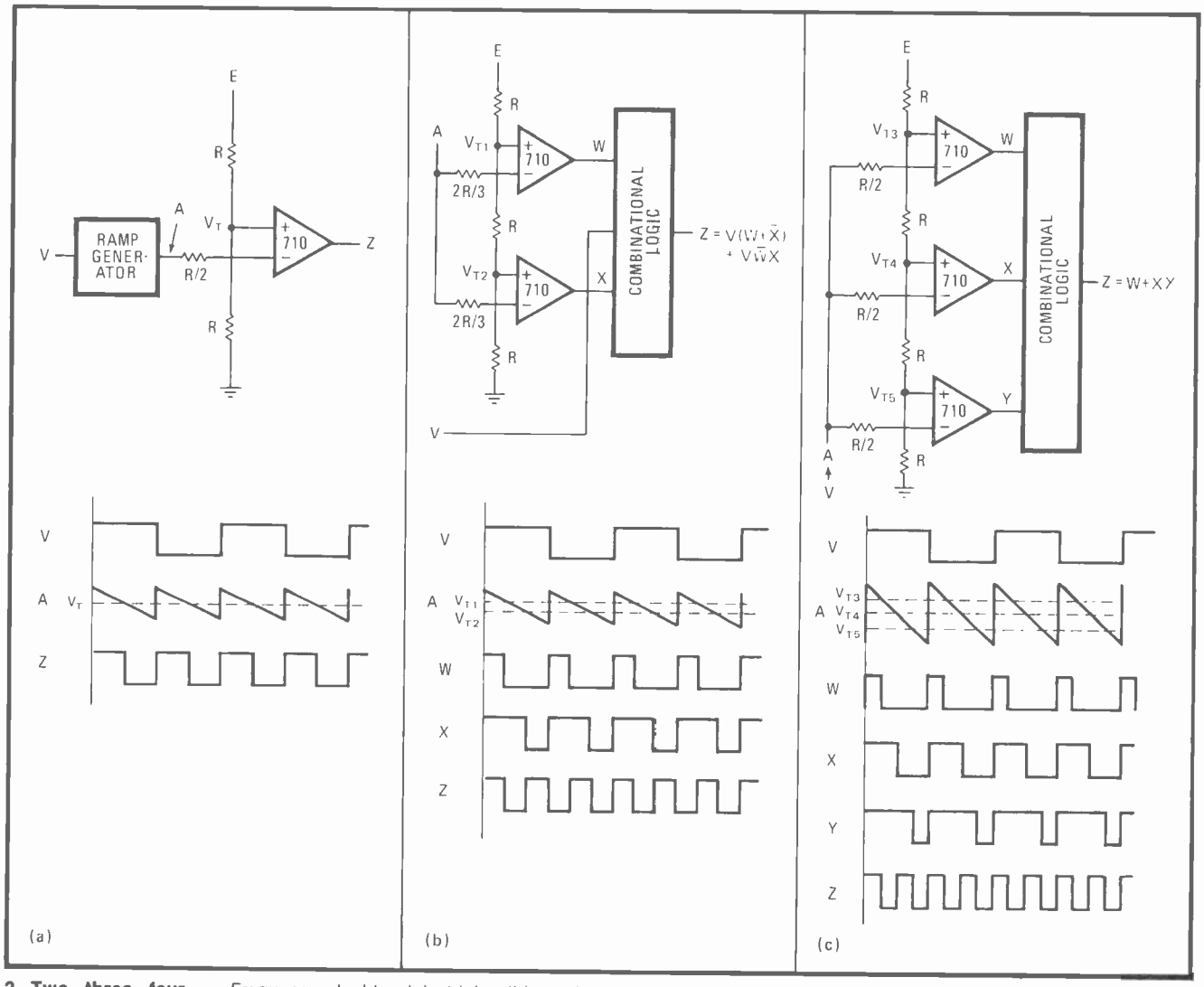
Relying on a technique that uses digital logic rather than high-speed system clocks or nonlinear generators to perform frequency multiplication, these circuits derive a square wave with an output frequency of up to four times that of the input signal. Extremely easy to understand and implement, the general method used in synthesizing these combinational-logic circuits is useful for achieving practical high-order frequency multiplication of up to eight times.

Since frequency-doubler circuits are relatively simple and well-known configurations exist, the logic technique is shown in Fig. 1 for a frequency tripler. For the logic circuit to perform tripling, the waveform at Z must traverse three full cycles, or six half-cycles (represented by states 101010), during the time of one input cycle (represented by 111000) at V. Thus the circuit must detect six different logic states, and so a minimum of three input variables, V, W, and X, is required.

Note, however, that the input signal at port V is the



1. Multiply by 3. Digital frequency multiplier is an alternative to multipliers using high-speed clocks and nonlinear generators. States W and X are derived from V, although transformation cannot be done digitally (a). Ramp and comparators can generate the required digital voltages from V, however (b). Use of linear ramp allows easy determination of the threshold levels that must be detected to switch logic elements.



2. Two, three, four.... Frequency doubler (a), tripler (b), and quadrupler (c) are easily synthesized with combinational logic and comparators. Technique can be extended to multiply by up to eight circuits. Number of comparators in multiply-by-N counter is N − 1; threshold value V_T has value of ME/N if ramp is linear, where M is the comparator number and E is the supply voltage.

only waveform available, and therefore signals W and X, whose logic states for a particular V are not yet known, must be derived from V itself. The particular values of W and X may be assigned to the truth table once it is realized that the duty cycles of the three input variables are different and that the logic states of the dependent variables, W and X, must change at a faster rate than the independent variable, V. Once the logic states are assigned, the Boolean equation may be determined and the circuit synthesized with simple logic gates. Although several combinations of W and X may be assigned to a given V, the end result should be virtually the same in the Boolean expression. However, it is important to assign the logic 1 states to W and X before the 0 states are assigned to them, for reasons that will shortly become obvious.

Variables W and X not only change with the state of V, but also vary with time when V is constant, as shown. Therefore, W and X cannot be derived directly from V in the digital domain. However, a negative-going ramp voltage whose sweep rate is equal to twice the input frequency can, with the aid of operational-amplifier threshold detectors, synthesize the digital signals required at W and X for the doubler (a), tripler and quadrupler, as shown in Fig. 2. The timing diagram details the circuit operation, obviating the need for a description of each logic circuit.

There are several well-known ways to generate the negative ramp voltage required, many of them constructed with multivibrators and op amps. The block diagram of such a ramp generator is shown in the lower portion of Fig. 1. Use of a linear ramp of the type shown allows easy determination of the threshold levels that must be detected in order to switch the logic elements at the proper times.

Generally, the number of comparators in a circuit will be equal to N − 1, where N is the multiplication factor, whose maximum practical value is 8. The threshold voltages will be equally spaced if a linear ramp is used, each voltage being equal to ME/N, where M is the comparator number and E is the supply voltage. □

Diodes and integrator brake small motors dynamically

by Stephen Wardlaw
Yale-New Haven Hospital, Dept. of Laboratory Medicine, New Haven, Conn.

Alternating-current motors used in position-sensing circuits must be quickly braked and stopped if the system is to retain its positional accuracy. In the case of a small shaded-pole motor, a dc source connected directly to its field winding brakes it dynamically by rapidly dissipating its kinetic energy. But if not turned off in time, the source will overheat the motor.

A safer way is to derive the dc voltage through a silicon controlled rectifier, a diode, and a resistance-capacitance network. Moreover, such a circuit costs less than an electromechanical switch and is simpler than a thermal-delay or momentary-contact switch.

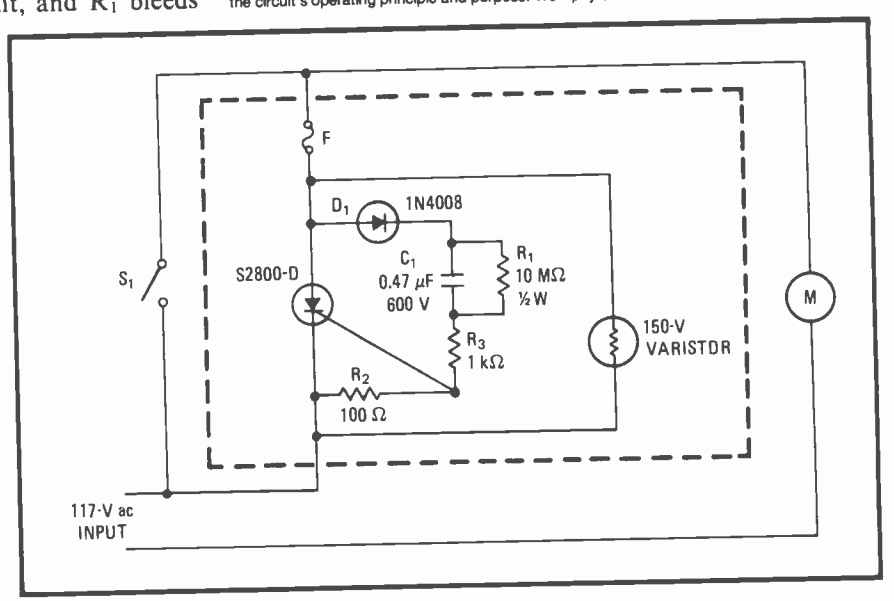
As shown in the figure, the braking unit (within the dotted lines) must be placed in parallel with a manual electronic switch, S_1, that is used to trigger the braking of motor M. With S_1 in the normally closed position, no voltage appears across the braking unit, and R_1 bleeds off any charge being stored in capacitor C_1.

When braking is desired, S_1 is activated and thus opened, so that the positive half-cycle of the line voltage will appear across D_1, C_1, and R_1–R_3 and the SCR will be triggered. This action, in addition to enabling a strong pulse of direct current to flow through the motor windings, partly charges C_1.

When the line current drops through zero and into its negative half-cycle, the SCR turns off and remains in that state until the ac input reaches its positive half-cycle again. The process is repeated until C_1 is charged to near the peak value of the line voltage, at which time direct current will cease to flow. The SCR will not turn on again, because D_1 will be permanently back-biased.

The 150-volt varistor helps to suppress line spikes. The fuse, F, is included as a safety precaution and will open if for some reason the braking unit continues to enable the power line to feed a relatively high direct current through the motor winding. Using the component values shown, the braking unit will enable the line to supply a pulsating dc to the motor for approximately 1 second—more than enough time to completely brake any small motor with a rating of up to ¼ horsepower or so. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.



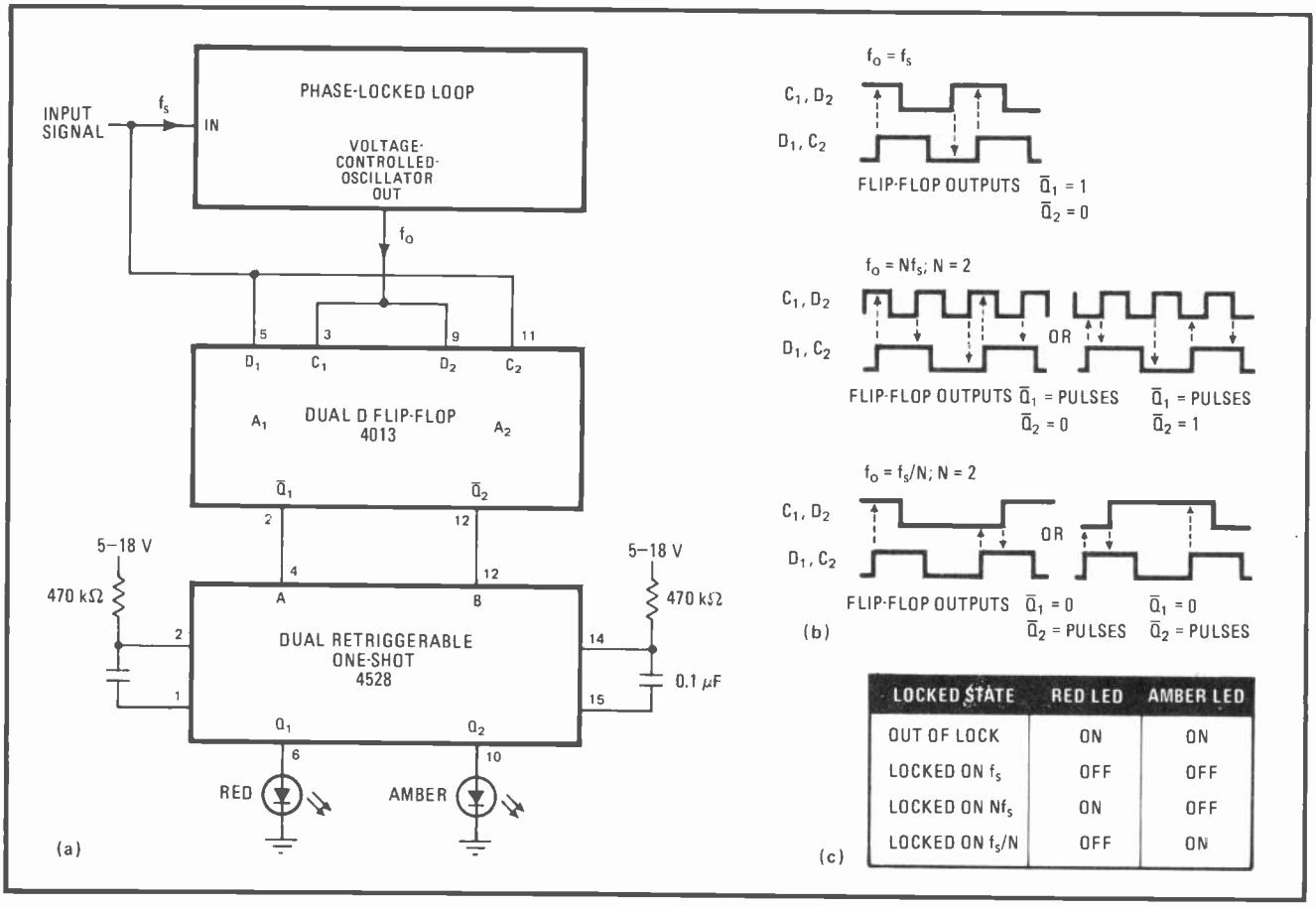
Fast reaction. S_1 initiates motor braking. Positive half-cycle of input voltage appears across D_1, C_1, R_1–R_3, firing SCR and enabling direct current to flow through small shaded-pole motor. C_1 charges to nearly peak value of input voltage during succeeding positive half-cycles, terminating process.

D flip-flops sense locked state of PLL

by L. W. Shacklette and H. A. Ashworth
Seton Hall University, Department of Physics, South Orange, N. J.

This circuit uses a dual D flip-flop to sense the locked state of many popular phase-locked loops, such as the Signetics 562 and 565. By adding a dual one-shot–light-emitting-diode combination to the flip-flops, the circuit visually indicates locking for the conditions where the output frequency, f_o, is locked to the input signal (f_s), to its harmonics (Nf_s) or to its subharmonics (f_s/N).

The circuit shown in (a) determines whether a fixed



(c)

LOCKED STATE	RED LED	AMBER LED
OUT OF LOCK	ON	ON
LOCKED ON f_s	OFF	OFF
LOCKED ON Nf_s	ON	OFF
LOCKED ON f_s/N	OFF	ON

Lock detector. Monitor (a) detects the existence of a phase difference between f_s and f_o and can thus differentiate between three locked conditions, because circuit is also sensitive to ratios f_s/f_o, $f_s/2f_o$, and $2f_s/f_o$ (b). Table (c) summarizes circuit response.

(that is, locked) relationship between f_s and f_o exists by employing both flip-flops in a simple phase detector. The f_s signal drives the D input of flip-flop A_1 and the C input of A_2, and the f_o signal emanating from the voltage-controlled-oscillator output of the PLL drives C_1 and D_2. The design of the phase detector accommodates a PLL having a phase comparator that can generate an upper and lower f_s-to-f_o phase displacement of 180° and 0°, respectively, for the locked condition. The comparator does this by deriving an f_o that is displaced 90° with respect to f_s when the loop is in the center of its range.

The circuit response for a constant f_o and f_s may be understood with the aid of (b). Because the D flip-flops read the data signals (D_i) on the positive edge of each clock (C_i), whenever the data frequency f_{di} equals the clock frequency, f_{ci}, $\overline{Q}_1$ and $\overline{Q}_2$ of the 4013 remain fixed at either logic 1 or logic 0, depending upon whether the signals at C_i and D_i are in phase or out of phase. In either case, the output from the corresponding edge-triggered one-shot in the 4528 will be zero.

When f_c is an integer multiple of f_d, or f_d is an integer multiple of f_c, there will be a pulsed output signal from one of the output ports of the 4013 and a corresponding signal at the 4528 to light the LED. Note that because the one-shot is retriggerable, its output will be constantly at logic 1 for a pulsed input signal. The output (logic 1 or logic 0) from the other port of the flip-flop will be constant. When f_o and f_s are out of lock, each flip-flop reads random 1s and 0s, causing pulsed output signals to appear at both ports of the 4013. The table (c) summarizes circuit operation.

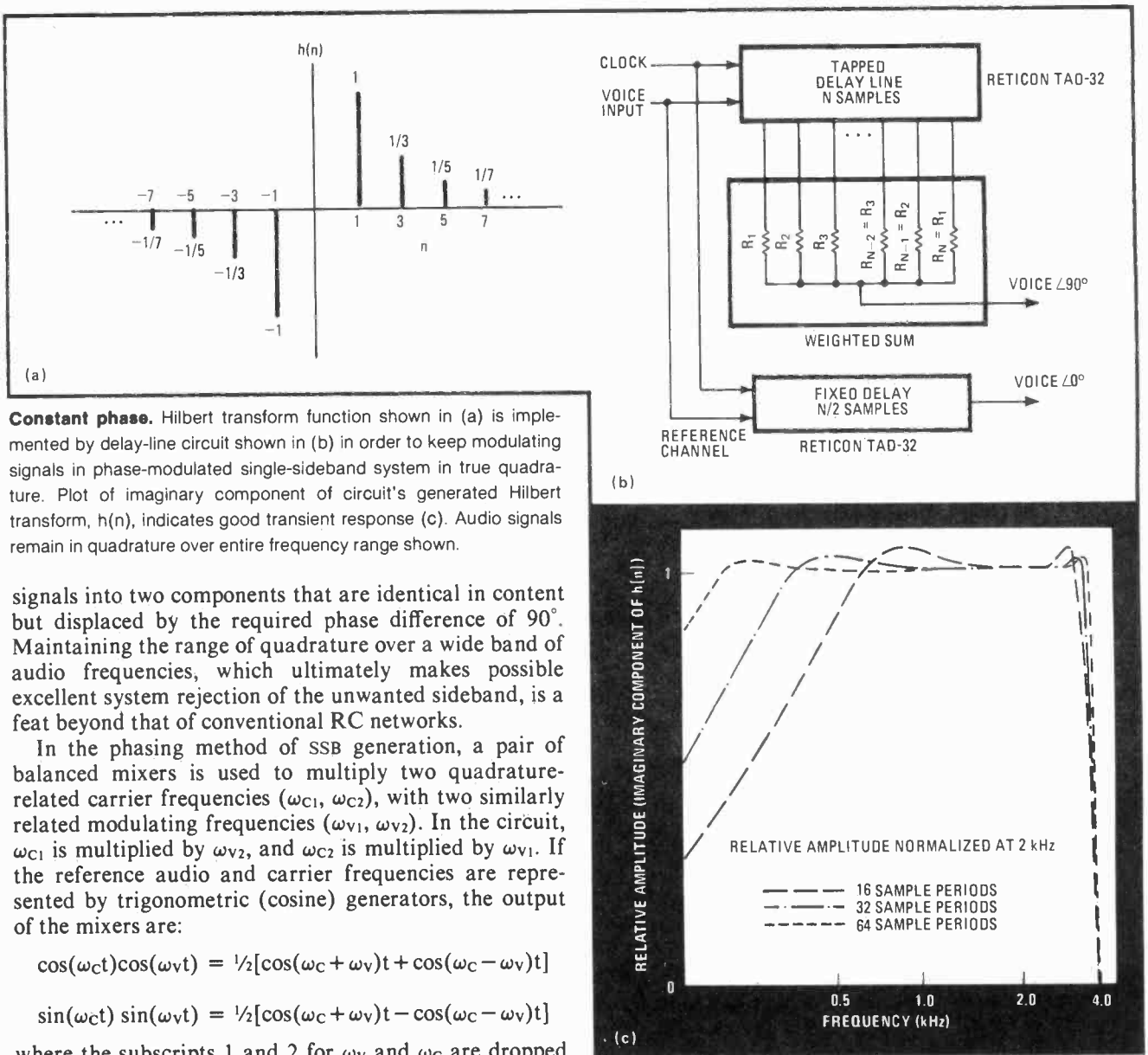
In cases where it is necessary to detect only the condition $f_o = f_s$, a simpler monitor can be constructed using only a single D flip-flop and one LED that is connected to its $\overline{Q}$ output. The LED will light whenever $f_o \neq f_s$. □

Delay lines help generate quadrature voice for SSB

by Joseph A. Webb and M. W. Kelly
University of Canterbury, Christchurch, New Zealand

The major difficulty faced by designers when trying to generate a single-sideband signal by the phase-shift method—that is, obtaining the modulating signals in quadrature over a wide band while achieving good transient response—may be overcome by implementing the well-known Hilbert transform with two clocked analog delay lines and a resistor weighting network.

This simple circuit splits the modulating (audio)



Constant phase. Hilbert transform function shown in (a) is implemented by delay-line circuit shown in (b) in order to keep modulating signals in phase-modulated single-sideband system in true quadrature. Plot of imaginary component of circuit's generated Hilbert transform, h(n), indicates good transient response (c). Audio signals remain in quadrature over entire frequency range shown.

signals into two components that are identical in content but displaced by the required phase difference of 90°. Maintaining the range of quadrature over a wide band of audio frequencies, which ultimately makes possible excellent system rejection of the unwanted sideband, is a feat beyond that of conventional RC networks.

In the phasing method of SSB generation, a pair of balanced mixers is used to multiply two quadrature-related carrier frequencies (ω_{C1}, ω_{C2}), with two similarly related modulating frequencies (ω_{V1}, ω_{V2}). In the circuit, ω_{C1} is multiplied by ω_{V2}, and ω_{C2} is multiplied by ω_{V1}. If the reference audio and carrier frequencies are represented by trigonometric (cosine) generators, the output of the mixers are:

$$\cos(\omega_C t)\cos(\omega_V t) = \tfrac{1}{2}[\cos(\omega_C+\omega_V)t+\cos(\omega_C-\omega_V)t]$$

$$\sin(\omega_C t)\sin(\omega_V t) = \tfrac{1}{2}[\cos(\omega_C+\omega_V)t-\cos(\omega_C-\omega_V)t]$$

where the subscripts 1 and 2 for ω_V and ω_C are dropped because the sine and cosine functions are 90° out of phase. The output of each mixer is then added or subtracted to obtain the upper ($\omega_C+\omega_V$) or lower ($\omega_C-\omega_V$) sideband, as desired. Remember, however, that quadrature between the audio and carrier frequencies must be maintained for optimum response.

The discrete Hilbert transform of any signal, that is:

$$h(n)=\frac{1-e^{j\pi n}}{\pi n}=\frac{1-\cos\pi n}{\pi n}$$

corresponds to a 90° phase shift of all its frequency components, and thus by implementing this function the quadrature relationship for the audio channels is maintained. Attaining quadrature for carrier signals is simple, since the ω_C signal has virtually zero bandwidth.

The discrete Hilbert transform is defined from plus to minus infinity, although truncation is needed for physical realization of the function. The truncated impulse response of this function is illustrated in (a).

The required response may be generated with the delay-line circuit shown in (b). A Reticon TAD-32 charge-coupled device is used for the delay line. The weighting resistors are selected so that the circuit will generate the product of the truncated function, h(n), and a smoothing or weighted function, W(n), where $W(n)=\cos^2 n\pi/N$. Each resistor is selected so that $R(n)=h(n)W(n)$. Note that the $\cos^2$ function is defined from +90° to −90°, not from plus to minus infinity.

The reference voice channel is delayed by N/2 samples for the audio channels to remain in true quadrature. At a clock frequency of 8 kilohertz, the delay amounts to 4 milliseconds for 64 samples.

The plot of the imaginary component of h(n) in (c) of the figure illustrates the excellent transient response of the circuit. As can be seen, relatively few samples are needed for good performance. In these tests, the clock frequency was 8 kHz. For telephone-quality voice signals, N = 32 is sufficient, and N = 64 represents excellent performance. Since the Hilbert transform is symmetrical, that is, $f(t)=-f(t)$, quadrature is perfect over the entire frequency range shown. □

Unity-gain buffer amplifier is ultrafast

by James B. Knitter and Eugene L. Zuch
Datel Systems Inc., Canton, Mass.

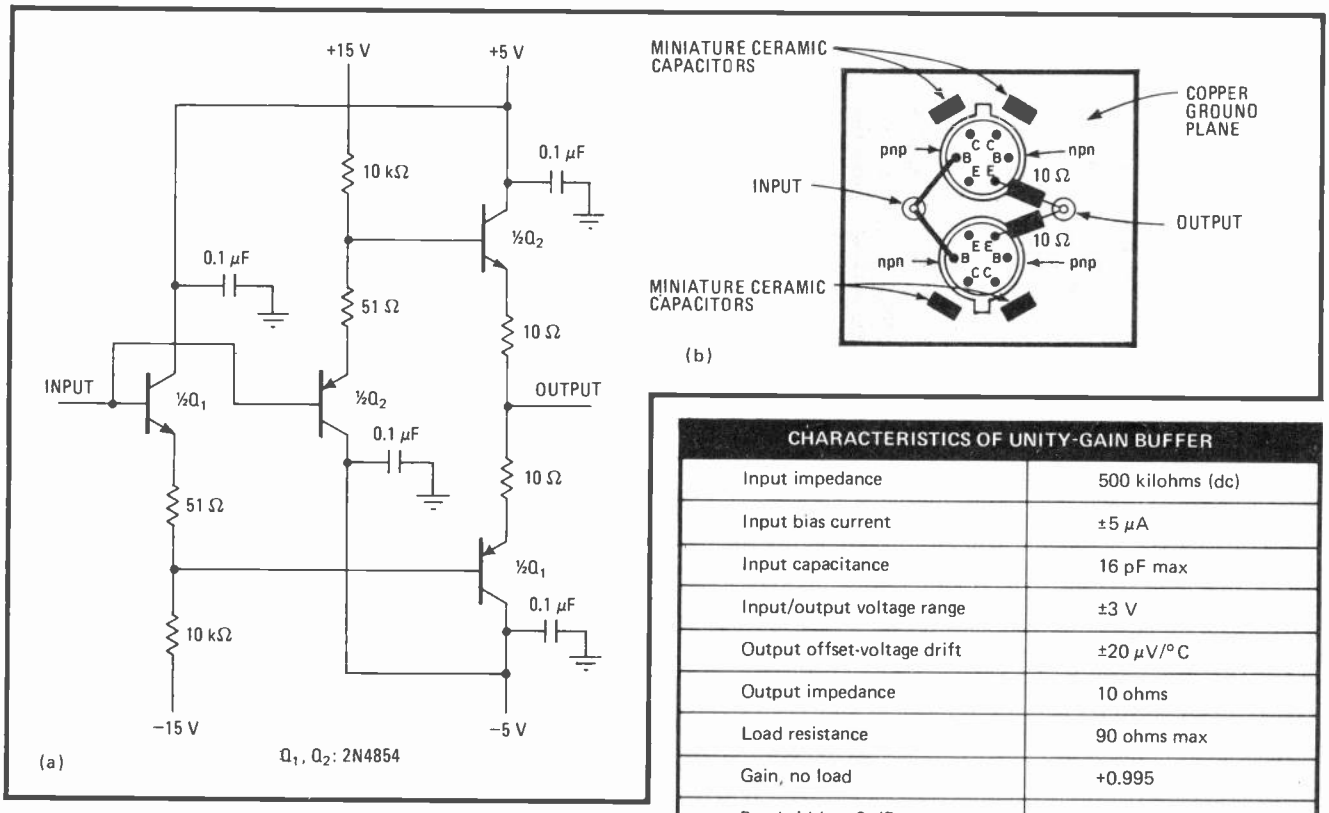
Applications where transmission-line drivers, active voltage probes, or buffers for ultrahigh-speed analog-to-digital converters are needed can use a stable buffer amplifier capable of driving a relatively low-resistance, moderate-capacitance load over a wide range of frequencies. The circuit shown in (a) fulfills these requirements. With a bandwidth of 300 megahertz, it exhibits no peaking of its response curve, having a gain of virtually 1 (0.995) under no-load conditions and 0.9 under a maximum load of 90 ohms.

The circuit is a variation on a basic emitter-follower network, which is inherently capable of wideband performance. However, no feedback loops are needed anywhere within the circuit to boost the gain at the high frequencies, and dispensing with them contributes to the stability of the circuit. Also, using two matched npn-pnp transistor pairs ensures close tracking between input and output voltages (a task normally addressed by suitable feedback circuitry) as well as low offset-voltage drift (20 microvolts/°C).

The complementary-transistor pairs are 2N4854s wired for active current sourcing and sinking so that bipolar input signals can be processed. Each transistor has a typical β of 100. With the npn and pnp input-bias currents tending to cancel each other, the resultant input-bias current of the amplifier is ± 5 microamperes.

Layout is critical to the stability of the circuit. The buffer should be constructed as shown in (b). The two transistor pairs are mounted close together, in holes drilled in a copper-clad circuit board as shown. The flanges on the TO-99 cases encapsulating the 2N485s should be soldered to the copper, which serves as a ground plane. The collector of each transistor must be bypassed by a 0.1-microfarad ceramic-chip capacitor mounted close to the transistor. This is done by standing the capacitors on end, with the bottom contact lead soldered to the ground plane and the top contact lead soldered to the collector.

All leads must be less than ½ inch in length and be as



Wideband buffer. Emitter-follower configuration yields unity gain from dc to 300 megahertz. Absence of feedback in circuit contributes to buffer stability. Use of matched npn-pnp transistor pairs ensures almost perfect input/output signal tracking (a). Component layout is critical for circuit stability (b).

CHARACTERISTICS OF UNITY-GAIN BUFFER	
Input impedance	500 kilohms (dc)
Input bias current	±5 μA
Input capacitance	16 pF max
Input/output voltage range	±3 V
Output offset-voltage drift	±20 μV/°C
Output impedance	10 ohms
Load resistance	90 ohms max
Gain, no load	+0.995
Bandwidth, −3 dB	300 MHz
Power supply, quiescent	±15 V dc at 1.5 mA ± 5 V dc at 4.5 mA
Power consumption	90 mW

directly wired as possible. One-eighth-watt resistors are used throughout and are soldered to the transistor leads as close as possible to the case. For clarity, not all components are shown. For coupling to or from the amplifier, subminiature radio-frequency connectors can be mounted at the input and output ports of the buffer.

Typical characteristics of the unity-gain buffer circuit are listed in the table. □

Dual charge-flow paths extend pulse repetition rate

by J. Klimek
Pretoria, South Africa

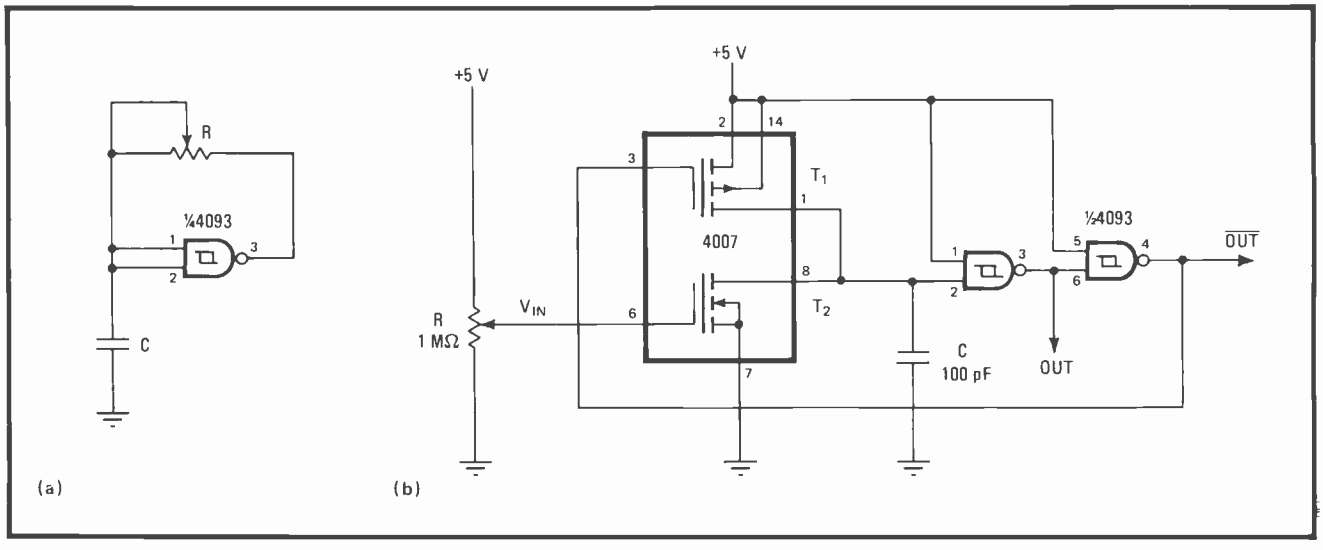
Although the basic, one-gate pulse generator shown in part (a) of the figure cannot be beaten for convenience in general test applications, it has a relatively narrow repetition-rate range, typically only a few tens of kilohertz. But with a few modifications (b), the repetition rate for a narrow-width pulse train can be extended from dc to 1 megahertz or so.

The range of the pulse generator is increased because the timing capacitor is charged and discharged through separate paths. This operation decreases circuit-switching times and enables the circuit to oscillate over a wide band of frequencies. Gate T_1 is one sixth of the 4007 chip, which contains three n-channel and three p-channel enhancement-mode transistors; it charges capacitor C for as long as pin 1 is high. For the circuit configuration shown, the charging period is a fraction of a microsecond.

When T_1 is switched low by pin 4 of the 4093, C discharges through T_2, the current source-sink whose value is controlled by R. Once C is discharged, T_1 switches high again and the process repeats.

In this instance, when 0.7 volt $\leq V_{in} \leq$ 3.4 volts, the corresponding repetition rate varies from dc to 1 MHz. The pulse width, which is about 0.5 microsecond, may vary by as much as a factor of 2, depending on the particular 4007 used. But whatever the value, it will be constant throughout the 0-to-1-MHz range.

To minimize the phase jitter that may occur at low frequencies because of the small charge current involved, the circuit should be placed inside a metal enclosure. In line with the low-frequency consideration, a low-leakage capacitor is also recommended. □



Simple improvement. The range of a standard Schmitt-trigger pulse generator (a) can be easily extended by adding one 4007 gate array to circuit (b). New circuit charges and discharges timing capacitor C through separate paths, enabling the circuit to generate a narrow-width pulse train (0.5 microsecond) over 0 to 1 MHz for an input voltage ranging from 0.7 to 3.4 V.

PROM adds bootstrap loader to Intellec-8 development system

by Bernard Boulé and Simon Gagné,
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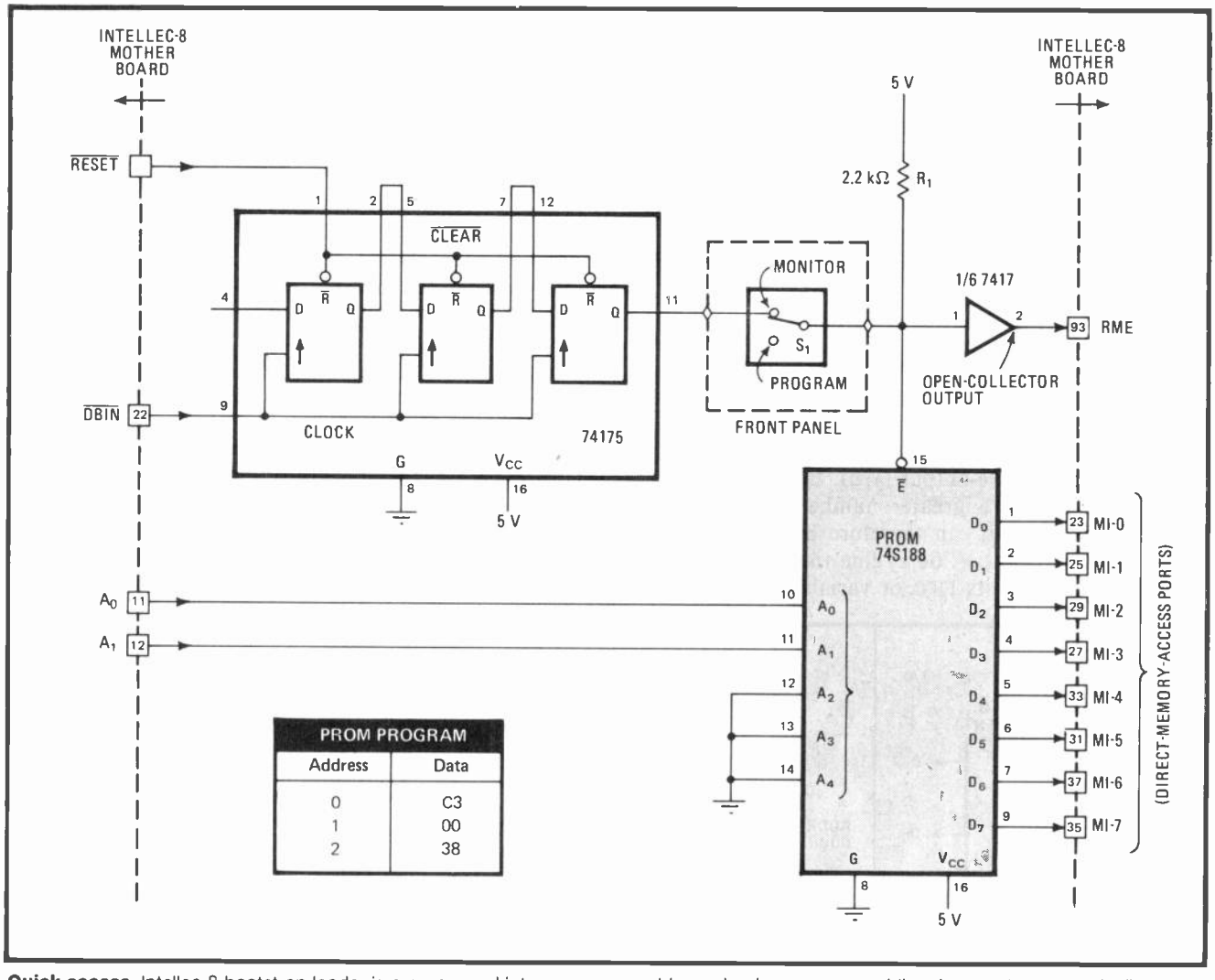
This three-byte bootstrap loader program will enable users of Intel's popular microcomputer-development package, Intellec-8, to immediately and automatically access the system's monitor, or executive-control routines, on power-up. The bootstrap is stored in a programmable read-only memory external to the system.

In normal operation, the Intellec's 8080 microprocessor is reset on starting up, thus clearing the system's



PROM PROGRAM	
Address	Data
0	C3
1	00
2	38

Quick access. Intellec-8 bootstrap loader is programmed into a programmable read-only memory, enabling the user to automatically enter a system monitor at location 3800H on power-up. The PROM's contents are dumped into the system's direct-memory-access ports on three successive data clocks (DBIN). The PROM operation in no way affects the system's random-access memories (not shown).

program counter. Program execution then proceeds from memory location 0, but the monitor is located at starting address 3800H. Therefore, to enter the monitor, a jump instruction (programmed as C3 00 38) must be written into the first three locations of the system's random-access memories starting at location 0 after each power-up. Manual programming is a bothersome task, requiring that the memory-access port be activated and that each address be entered, loaded, and then incremented as the contents of each (C3, 00, 38) are set and loaded into memory.

An easier way to enter the monitor is to program the jump instruction into a 74S188 PROM and dump its contents directly into memory during power-up, as shown in the figure. Although only 3 of the 32-word-by-8-bit device's locations are used, the low cost of the PROM and the convenience afforded by the modifications overshadow the waste of the 29 unused locations. The only other consideration with this circuit is to ensure that the system's RAMs will not be disturbed in any way by the PROM.

The PROM is programmed with the data shown in the table. With S_1 in the program position, the PROM's output lines (D_0–D_7) are disabled and the PROM can be loaded. Pull-up resistor R_1 ensures that the RAM memory enable (RME) line is active, so that any program loaded into RAM at address 0 can be run without interference stemming from programming the PROM.

S_1 is then placed in the monitor position. Immediately after a system reset, the three flip-flops in the three-stage 74S175 shift register and the RME line are reset. At the same time, the output of the PROM is enabled. Upon the arrival of the first three normally occurring system, or data-byte, clock pulses (DBIN), lines A_0–A_1 are incremented and the contents of the PROM are read into system memory. On the third pulse, the output of the shift register goes high, releasing the RME line and disabling the PROM, which remains inactive until a new reset cycle occurs. □

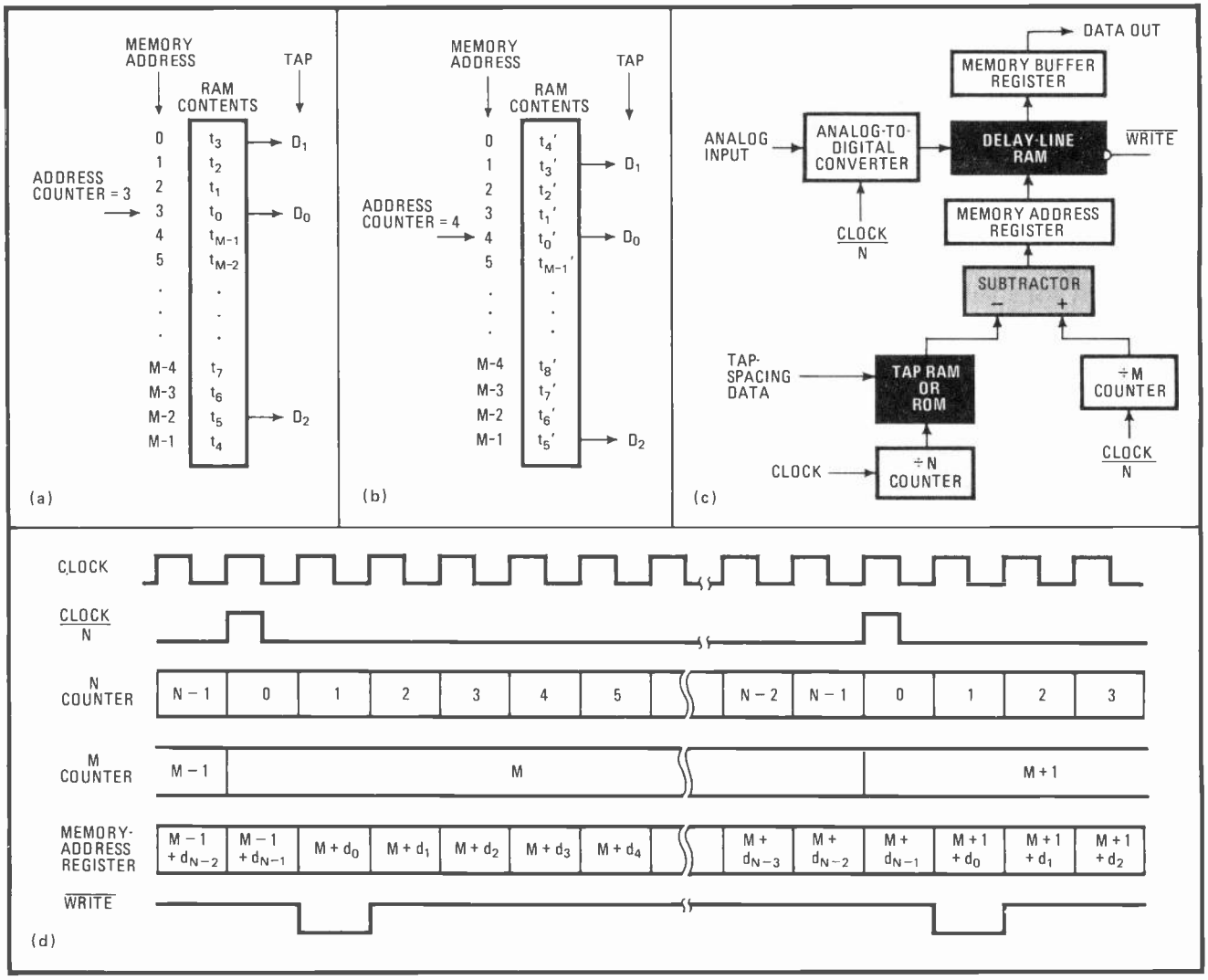
RAMs reduce chip count in programmable delay lines

by Scott M. Smith
University of Texas, Applied Research Laboratories, Austin, Texas

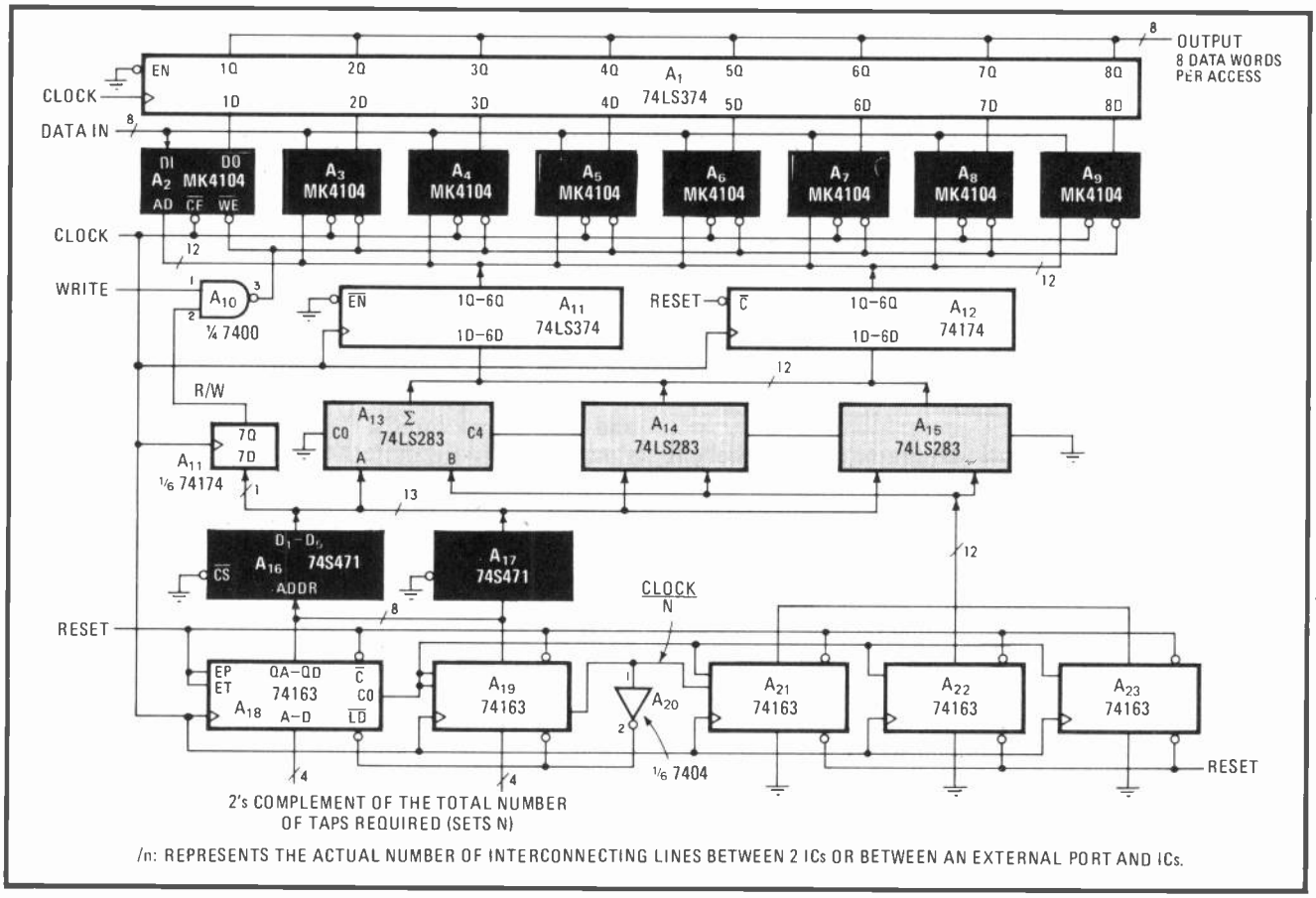
First-in, first-out buffers or variable-shift registers are most often used for the storage elements in digital programmable-tap delay lines (that is, one or more shift registers with multiple-output taps). But random-access memories can store a greater number of samples per integrated circuit and can therefore be used to reduce the total device count. A delay line that uses RAMs will cost much less than its FIFO or variable-length register counterparts if the total number of samples handled is fairly large.

Quite unlike a standard shift register, in which input data is introduced at its standard-input port (first location) and then shifted through, a RAM must have its input data introduced at each individual location. The reason is obvious: the contents of the RAM cannot be shifted, but merely accessed by the system's address counter. Therefore, input data must be entered into the particular RAM location that corresponds to the present location of the address counter.

The memory map in Fig. 1a shows how a delay line is mapped onto a RAM having a length of M words and yields an insight into the factors involved in designing a practical circuit. Three output taps, D_0–D_2, are desired in this example. D_0 represents the zero-delay tap. The RAM address counter points to location 3, which contains



1. Super-long tapped delay. Memory map shows how an N-tap delay line is mapped onto an M-word RAM (a). Input data may be introduced into RAM by incrementing counter and placing sample there. Oldest data sample is destroyed and existing samples are redefined (b). Block diagram of system outlines procedure used to write data, examine output taps (c). Waveform diagram details timing constraints (d).



2. Great capacity. Eight-bit-wide programmable-tapped delay line is implemented with Mostek MK4104 random-access memories as shown. Each delay line is the equivalent of a 4,096-bit shift register. User may specify a total of 255 output taps with any desired spacing.

t_0, the most recent sample in the delay line. The next most recent sample is t_1, with t_{M-1} being the oldest sample. D_1 and D_2 are taps delayed three samples and five samples, respectively, with regard to D_0.

The value corresponding to memory address 3 (t_0 = logic 1 or logic 0) would appear at D_0 if that tap were requested. Similarly, the sample at memory address 0 would be fetched if D_1 were to be requested, and the sample at address $M-2$ would be fetched if D_2 were requested.

Figure 1b shows how a new sample would be inserted into the delay line. The counter would be incremented, pointing to location 4 as shown, and the new sample would be written into the location, thus shifting the oldest data sample (t_{M-1}) out of RAM. The memory contents of RAM would otherwise be unchanged; each memory address would be simply redefined as being one sample older. If D_1 were queried, the sample at memory address 1 would be fetched; when D_2 were requested, the sample at location $(M-1)$ would be fetched.

The block diagram shown in Fig. 1c more clearly explains how data is written, and taps are specified and read. A divide-by M counter driven by a clock running at $1/N$ times the system clock frequency is required for pointing to the most recent sample (D_0). Also required is a tap RAM or ROM, which is programmed so that its output is equal to the distance in time (that is, the number of samples) each user-specified output tap is from the most recent sample, t_0. Thus, the spacing between taps is specified. A divide-by-N counter (where N is the number of taps) is needed to address each tap in a sequence that is selected by the user. Note that the N counter must move through one complete cycle for each increment in the M count. The subtractor determines the numerical difference between the tap distance and the zero-delay location and stores the result in the memory address register in order to access the memory address desired. The delay-line RAM is then accessed to obtain the data sample corresponding to the tap selected, or to write in a new data sample. Then the sample that has been read is stored in the memory buffer register, to be shifted out in serial form.

The timing considerations for the circuit are shown in Fig. 1d. As may be observed, provision should be made to ensure that the M counter advances before any new data (write) is stored in RAM, if necessary, to allow the oldest sample to be read before it is overwritten. There are no other major considerations. The taps may be accessed in any order and are selected by appropriate programming of the tap delay memory (tap ROM). The maximum shift rate (the frequency with which new samples are placed in memory) is $f_{s\,max} = 1/Nt_{c\,min}$, where $t_{c\,min}$ is the minimum cycle time of the system.

Figure 2 shows a design example that uses an 8-bit-wide programmable tapped-delay line. The RAM memories, each holding 4,096 1-bit words, form a 4,096-word-by-8-bit array. A_1 is the memory buffer register, A_2–A_9 is the RAM delay line, the memory address register is

A_{11}–A_{12}, and A_{13}–A_{15} is the subtractor. The tap ROMs are implemented by A_{16}–A_{17}. The divide-by-N counter is implemented by A_{18}–A_{20}. Two hundred and fifty-five output taps may be specified. A_{21}–A_{23} is the divide-by-M counter. Note that bit 7 of A_{11} buffers the read/write definition bit from ROM. □

Low-cost watch crystal excites ultrasonic burst generator

by Daniel F. Johnston
University of New Brunswick, Fredericton, N. B., Canada

A small pulse-burst ultrasonic generator having excellent frequency stability can be formed by uniting the miniature quartz-crystal time base found in an electronic wristwatch with an integrated-circuit divider and one logic gate. This circuit will deliver a fixed frequency output of selectable burst width, and it is thus tailor-made for many portable instruments such as underwater location beacons and depth-finding (sonar) devices. The current drawn by the circuit is typically several microamperes.

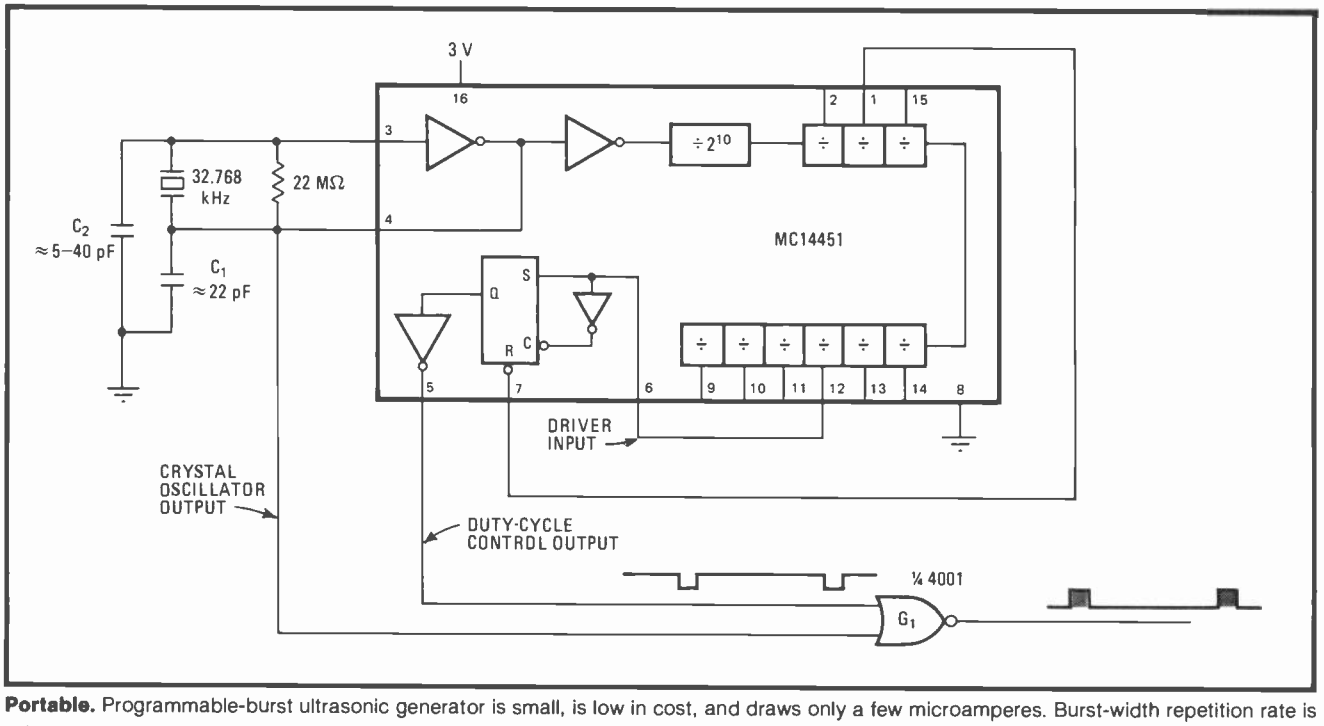
The generator is shown in the figure. The standard quartz crystal operates at 32.768 kilohertz, is readily purchased, and costs only a few dollars. Crystals from 17 to 150 kHz can be obtained at slightly higher cost if other frequencies are desired.

The IC divider is the MC14451, a low-cost divider-and-duty-cycle-controller built with complementary-metal-oxide-semiconductor technology that may be powered by a source of from 1.3 to 3.0 volts. The device contains an 19-stage binary divider (with taps available at any register port from 2^{11} to 2^{19}, inclusive), and a buffered flip-flop circuit for duty-cycle, or burst-width control.

The crystal is placed in a conventional oscillator circuit, as shown, with one inverter of the MC14451 serving as the active positive-feedback element. C_1 and C_2 in the oscillator are trimmed to achieve the required accuracy and are on the order of 22 picofarads for C_1 and 5 to 40 pF for C_2. The output of the oscillator is simultaneously fed to the MC14451 and G_1.

The crystal oscillator signal appearing at the output of G_1 is gated by the duty-cycle control output of the MC14451. To select the burst-width repetition rate, the appropriate buffered output of the divider must be connected to the driver input of the duty-cycle flip-flop, pin 6. Another buffered output, whose output period corresponds to twice the required burst width, must be connected to the duty cycle reset port, pin 7. The duty-cycle control output will toggle as required, switching low for the interval specified by the reset line at a rate controlled by the driver-port signal. The output from G_1 will therefore be a burst of a constant frequency.

Current consumption of the circuit is only 5 μA when a 32-kHz crystal is used and only twice that for a 65-kHz crystal. Thus the circuit can be powered by a small-capacity battery. □



Portable. Programmable-burst ultrasonic generator is small, is low in cost, and draws only a few microamperes. Burst-width repetition rate is selected by connecting the appropriate buffered output of the tapped binary divider in the MC14451 to pin 6. Burst width, adjustable from about 31 milliseconds to more than 1 second, is selected by connecting a second buffered output to pin 7 of the device.

PROM converts push-button command to binary number

by Marco A. Brandestrini
University of Washington, Center for Bioengineering, Seattle, Wash.

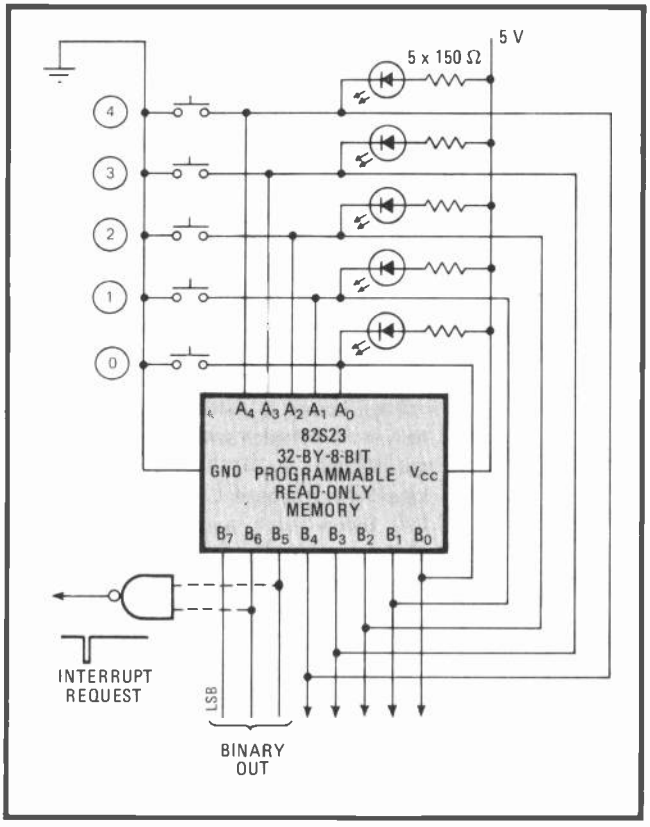
A programmable read-only memory can be used to convert a decimal-input command from a one-of-five momentary-contact-switch array to its equivalent binary number, thus forming a circuit with countless uses in logic- and microprocessor-control applications. The circuit is superior to systems using a thumbwheel switch to digitally set the binary number and is more reliable than single-switch arrays using an all-mechanical arrangement. Variations and extensions of this idea are limited only by the size of PROMs available.

The basic idea is to connect the PROM's output lines, B_0–B_4, to their respective address inputs, A_0–A_4 so that any input signal may be latched and the resulting signal at the output will remain active after a given key is released (see figure).

The PROM, here the Signetics 82S23, should be programmed as shown in the table if the output code is to be the binary equivalent number of the decimal input signal. In order to force the output to a given state after the circuit has been turned on (power up), inputs A_0–A_4, usually all high, can be programmed to actuate any of the five output combinations. The truth table shows how the PROM is programmed for state 0 after power up. Of course, any input-output relation may be programmed into the PROM as desired.

Circuit operation is simple. If, for example, the 0 key is depressed, a logic 0 appears at address A_0 (all input and output ports are active low). The resulting output at

Key-stroke commands. Circuit converts decimal-input command to its equivalent binary number. Momentarily depressed key is sensed by PROM and displayed by light-emitting diode. Outputs of PROM are wired to inputs and actuate latching. Interrupt generation is provided for microprocessor applications.



PROGRAMMING OF THE PROM

DECIMAL INPUT NUMBER	INPUTS A_4 A_3 A_2 A_1 A_0	OUTPUTS B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0
	0 0 0 0 0	1 1 1 1 1 1 1 1
	0 0 0 0 1	
	0 0 0 1 0	
	0 0 0 1 1	
	0 0 1 0 0	
	0 0 1 0 1	
	0 0 1 1 0	
	0 0 1 1 1	
	0 1 0 0 0	
	0 1 0 0 1	
	0 1 0 1 0	
	0 1 0 1 1	
	0 1 1 0 0	
	0 1 1 0 1	
	0 1 1 1 0	
4	0 1 1 1 1	0 0 1 0 1 1 1 1
	1 0 0 0 0	1 1 1 1 1 1 1 1
	1 0 0 0 1	
	1 0 0 1 0	
	1 0 0 1 1	
	1 0 1 0 0	
	1 0 1 0 1	
	1 0 1 1 0	
3	1 0 1 1 1	1 1 0 1 0 1 1 1
	1 1 0 0 0	1 1 1 1 1 1 1 1
	1 1 0 0 1	
	1 1 0 1 0	
2	1 1 0 1 1	0 1 0 1 1 0 1 1
	1 1 1 0 0	1 1 1 1 1 1 1 1
1	1 1 1 0 1	1 0 0 1 1 1 0 1
0	1 1 1 1 0	0 0 0 1 1 1 1 0
POWER UP	1 1 1 1 1	0 0 0 1 1 1 1 0

OUTPUT PORTS

B_0 moves low, and this signal is fed back to its corresponding input, keeping A_0 low after key 0 has been released. A light-emitting diode monitoring the A_0 port glows, indicating that the line has been activated.

If a second key is depressed, all of the PROM's open-collector output lines move high temporarily, clearing the output (see table), and the new key position is latched. The temporary logic 1 state is sensed by the NAND gate shown and produces an interrupt request—which is useful in microprocessor applications. □

RC-discharge clock makes a-d encoder logarithmic

by V. Ramprakash
Electronic Systems Research, Madurai, India

This analog-to-digital converter produces a 12-bit digital output that represents the natural logarithm of an input audio signal in the 1-to-1,000-millivolt (60-decibel) range. It is useful for monitoring slow changes in many natural processes. The circuit also may be adapted for use as a combination voice compander and encoder in a digital communications system.

Operation is based on the principle that the discharge rate of a voltage stored across a resistance-capacitance network is proportional to the logarithm of the ratio of the instantaneous to the initially applied voltage. When the voltage across the RC network is used to control the gating time of a counter, the counter's output is a binary-coded decimal number equal to ln V_i, where V_i is the input voltage.

The voltage across a discharging capacitor, V_c, in an RC network is given by:

$$V_c = V_r e^{-t/RC}$$

where V_r is the initial voltage. This equation, when transposed, becomes:

$$t = -RC \ln(V_c/V_r)$$

Let t_i represent the time it takes the capacitor to discharge from V_r to the input voltage V_i. If during this time a down counter is gated while being clocked at frequency f_c, the number of counts reached will be:

$$n_d = f_c t_i = -f_c RC \ln(V_i/V_r)$$

More generally, if the down counter is initially at a count of n_i, then the net count n_n after time t_i will be:

$$n_n = n_i - n_d = n_i + f_c RC \ln(V_i/V_r)$$

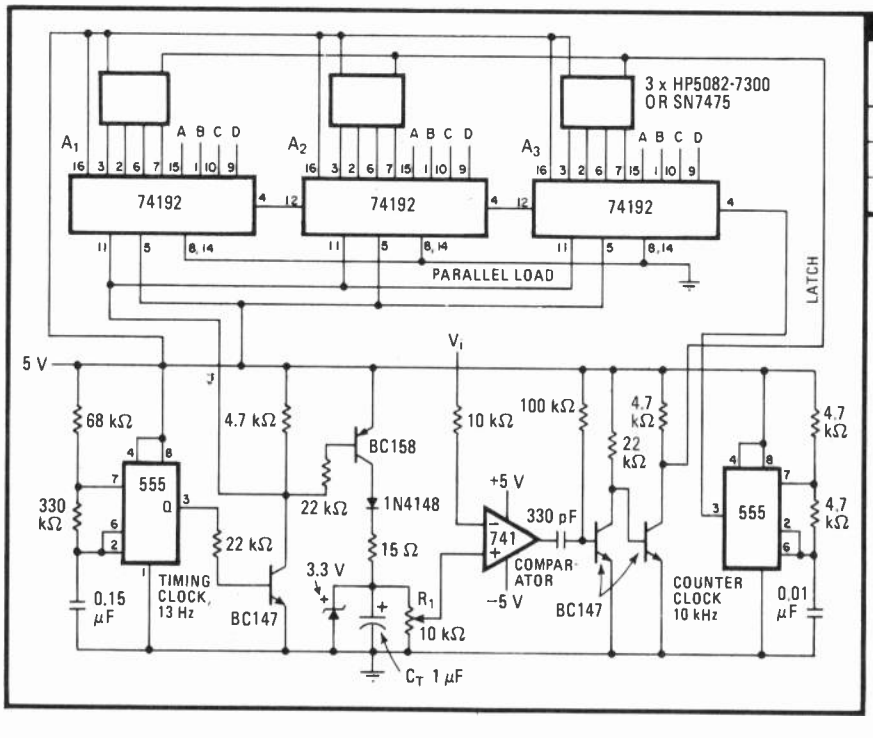
Letting V_r = 1,000 mv and n_i = 690, we arrive at:

$$n_n = 690 - 100 \ln 1000 + 100 \ln V_i = 100 \ln V_i$$

which can be reduced to $n_n = \ln V_i$ with appropriate scaling in a practical circuit.

The circuit shown in the figure implements the derived equation. When the output of the 555 timing clock is high, the 74192 up-down counter is loaded with the number 690 as shown in the table. At the same time, capacitor C_T is charged to 3.3 volts. R_1 facilitates the scaling of this voltage so that the potential as seen at the noninverting input of the comparator is 1 v.

When the output of the timing clock moves low, the 74192 begins to count down at a 10-kilohertz rate and C_T begins to discharge. As the voltage at the noninverting input drops below the sample voltage, V_i, the



LOADING OF 74192 UP-DOWN COUNTER

COUNTER	NUMBER	CODING A	B	C	D
A_1	6	1	1	0	0
A_2	9	1	0	0	1
A_3	0	0	0	0	0

Natural processing. Circuit is logarithmic a-d converter and digital encoder in one. Voltage across C_T, which decays exponentially at start of each sampling cycle, controls gating time of 74192 counters, ensuring logarithmic response. Counters are preset to 690 before each encoding to eliminate constant-coefficient terms inherent in circuit's transfer function, so that output from counter is n = ln V_i.

comparator output moves low and generates a latch pulse for the BCD-to-seven-segment displays, or 4-bit latches, as required. Thus the contents of the counter are stored in either the display or the latches. The sequence is then repeated. Note that a decimal point is located in the most significant display (corresponding to counter A_1) so that the natural logarithm of a 1,000-mV input signal will be correctly displayed as 6.90.

The low-frequency clock limits the input signal sampling rate to 13 hertz. However if the clock frequency is increased to 5 kHz or so, and the clock counter is replaced by one that can run at a few megahertz, the circuit will serve as an excellent speech encoder. □

Switching-mode controller boosts dc motor efficiency

by Jay C. Sinnett
U. S. Environmental Research Laboratory, Narragansett, R. I.

On-site monitoring equipment that makes use of a variable-speed dc motor places a special premium on the efficient use of the instrument's battery supply, because current drain is often high. This motor-speed controller circuit, which works on the principle of the highly efficient switching-mode power supply, saves energy and thus reduces circuit losses associated with the motor.

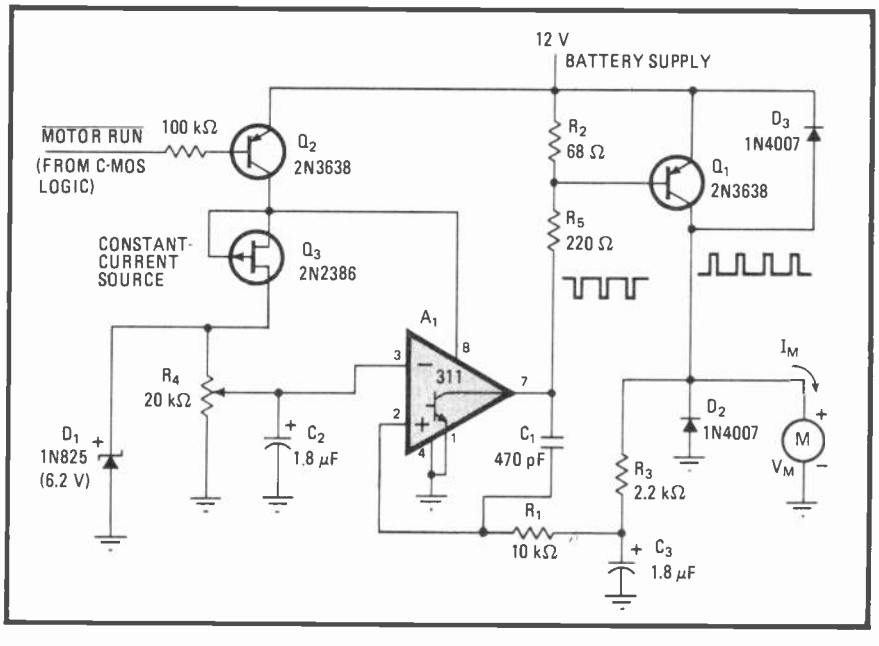
In this circuit, large, low-duty cycle pulses of supply current set up continuous currents in a small (0.01-horsepower) motor that are almost equal in magnitude to the peak current drawn by the supply, thereby contributing to circuit efficiency. As a typical example, almost 200 milliamperes of continuous motor current can flow when the average battery current drain is 100 mA, for an output voltage of 3.5 volts.

A_1, a voltage comparator, serves as both an oscillator and a duty cycle element in the controller, as shown in the figure. C_1 and R_1 provide positive feedback to A_1, enabling it to oscillate at about 20 kilohertz. The duty cycle, which can be from 10% to 70% of one 20-kHz period, is controlled by the negative feedback loop formed by Q_1, R_1, C_3, and R_3.

When the system's control signal, $\overline{\text{MOTOR RUN}}$, is asserted low, Q_2 turns on and applies power to the entire circuit. Pulses emanating from A_1 are amplified and inverted through Q_1 and pass through the motor, M. R_4 and D_1 set the average voltage supplied to the motor and thus largely determine the motor speed.

Note the absence of a capacitor at the output, which would normally be required to filter the pulsed signals and enable the motor to run smoothly. If a capacitor were used, it would have to be large in value and therefore large in size and costly as well. Instead, diode D_2 is placed in the circuit for filtering, enabling the pulsed energy to be stored by the motor's inductance in the field surrounding the windings. Between pulses, when Q_1 is off, little battery current is drawn, but the motor current is relatively large, since the amplitude of the current decays slowly through D_2.

Note also that although D_1 provides a stable, accurate reference, the average voltage fed back from the motor's terminals is affected by the forward-voltage drop of D_2. The drop varies with temperature and the current drawn through it and so reduces the absolute accuracy with which the output voltage can be set. However, resettability and stability are both very good with respect to battery voltage variations, and in applications where the temperature variations are minimal, the drawback will be unimportant. For example, the current variations due to even a 4-v supply-voltage change will be less than 2%.□



Less drain. Dc motor-speed control, which works on principle of switching-mode power supply, ensures minimum circuit losses. Duty cycle of pulsed output, 10% to 70% of one cycle at 20 kHz, drives motor, keeping battery current to minimum. Motor's inductance stores and filters pulses, essentially replacing filter capacitor normally used.

High-accuracy calibrator uses band-gap voltage reference

by Henno Normet
Diversified Electronics, Leesburg, Fla.

The Analog Devices' AD581J voltage reference can be used to build a low-cost and extremely accurate voltage calibrator for oscilloscopes that either do not have one built in or have one of inadequate accuracy. If this calibrator is battery-operated, the unit can be built for under $15.

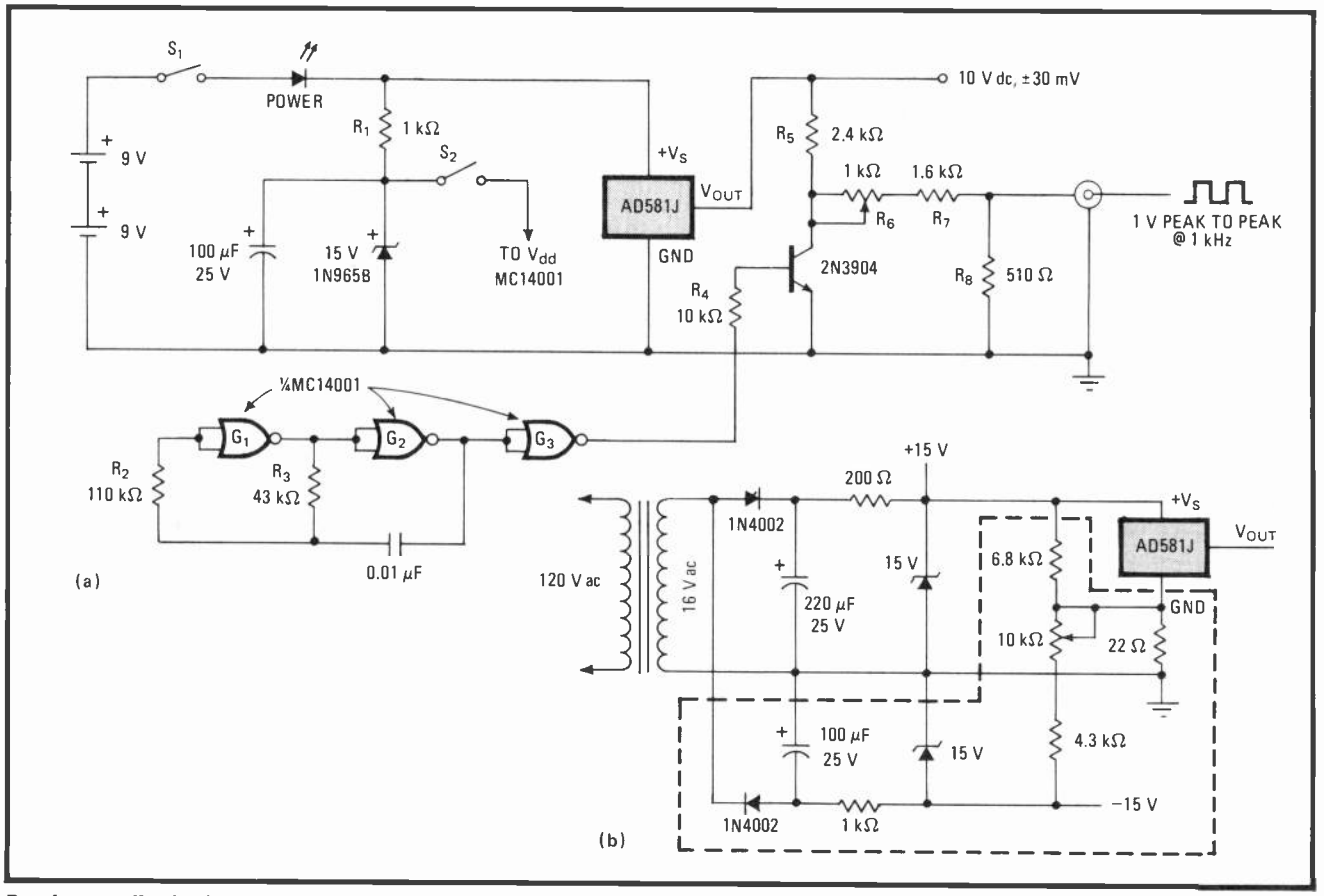
The calibrator generates a 1-volt peak-to-peak square-wave signal that is accurate to within better than 0.5%, owing its long-term accuracy to the band-gap technology used in the voltage reference. The reference voltages produced by the band-gap method are more temperature-stable than that produced by a zener diode, because the method makes use of the inherently constant potential that exists between adjacent electron energy levels in the semiconductor material of the integrated circuit itself. Here, the potential across selected energy bands is used to derive a 10-v reference that will vary no more than ±13 millivolts over the temperature range of 0°C to 70°C (for the 581L, the variation would only be 2.5 mv).

In this circuit, the output of a 1-kilohertz square wave is scaled to 1 v with the aid of the reference as shown in (a). An astable multivibrator, G_1–G_2, is used as the square-wave oscillator. R_2 compensates for input-threshold and power-supply variations, so that the duty cycle can be maintained at approximately 50%.

G_3 is used to improve the shape of the square wave that drives the 2N3904 switching transistor. The collector voltage for powering the transistor is derived from the band-gap voltage reference.

To eliminate the errors due to the transistor's offset voltage, R_6 is used to adjust the output for a collector swing of 0.005 to 1.005 v so that the difference voltage of 1 v peak to peak will appear at the output.

A dc digital voltmeter can be used for accurate adjustment of the output voltage, contributing to the ease with which the circuit can be calibrated. Accurate peak-reading ac voltmeters are not readily available, and



Precise amplitude. Scope calibrator generates 1-V square wave, accurate to within 0.5%, with aid of AD581J band-gap voltage reference (a). Unit may be powered by two 9-V batteries. Current drain is 6 mA. Ten-volt reference voltage is available at output jack for voltmeter calibration, etc. If more than occasional use is contemplated, the unit should be powered from the ac mains (b).

root-mean-square voltmeters will not yield accurate results if the output is not perfectly symmetrical (having a duty cycle of 50%).

To calibrate the circuit, it is necessary to open S_2, which disables the 1-kHz oscillator by removing the supply voltage to G_1–G_3. R_6 is then adjusted for an output voltage of 1.005 v. Then S_2 is closed, the input of G_1 is grounded and the output voltage is measured again. The difference between these two readings should be exactly 1 v. The two-step procedure should be repeated as necessary; R_6 should be adjusted for a voltage slightly removed from the 1.005 v originally set, then G_1's input grounded, and so on, until a difference voltage of 1.000 v is obtained.

Two 9-v batteries will provide many hours of operation. Battery drain is approximately 6 milliamperes. Typical units will work well down to a supply voltage of about 12 v.

If more than occasional use is anticipated, the unit should be powered from the 120-v ac line, as shown in (b). A bipolar (15-v) supply is derived from the power-line voltage, and a fine-trim circuit added as shown inside the dotted line, so that the set accuracy of the 581J's 10-volt output may be improved. □

In-range frequency detector has jitter-free response

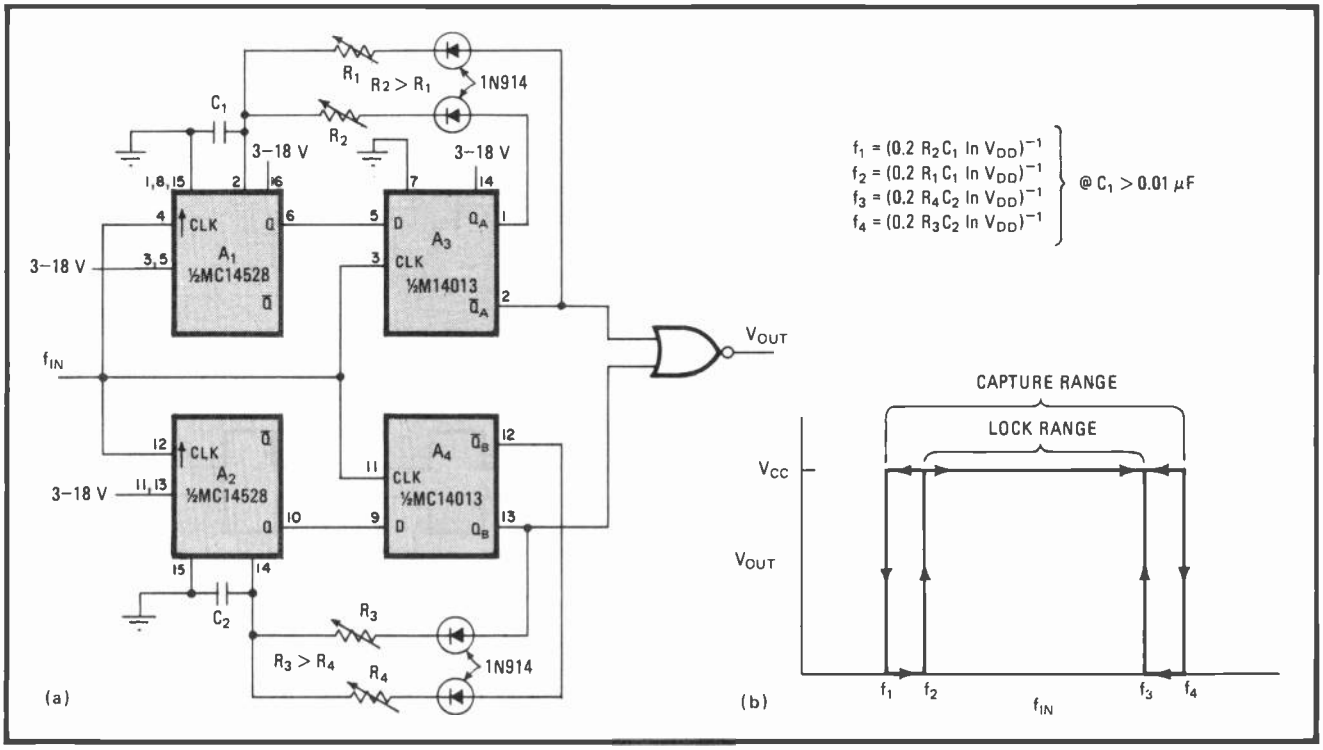
by A. J. Nicoll
Instromedix Inc., Beaverton, Ore.

This simple circuit will detect when an input signal falls within a specified frequency range and is thus ideal for use as an out-of-tolerance alarm or as a rudimentary phase-locked loop. It could also be called unusual, since it uses hysteresis to provide separate lock and capture ranges that eliminate the jitter of the circuit's logic-level output.

The diagram shown in (a) and the hysteresis curve shown in (b) help make the circuit's operation clear. A_1 and A_2 are two retriggerable one-shots. Their pulse widths, and therefore their maximum frequency of operation, are controlled by R_1–R_4. Whether R_1 or R_2 controls the width of A_1 and R_3 or R_4 controls the width of A_2 depends upon the state of the A_3 or A_4 D-type flip-flops.

Assume R_1 and R_4 are the controlling elements as an input signal of arbitrary frequency, f_{in}, arrives to trigger both one-shots simultaneously. The positive transition of f_{in} then fires A_1 and A_2, as shown. The next positive-going transition will trigger both A_1 and A_2 again while clocking the previous output states, which were generated before retriggering, into A_3 and A_4.

If this second transition occurs before either one-shot has returned to its time-out state, a logic 1 will be clocked into its respective flip-flop, changing the state of that flip-flop. Once the flip-flop moves from a 0 to a 1, the pulse width of the one-shot will be controlled by one



Within limits. Circuit (a) detects whether input signal is within user-set frequency range f_2–f_3 (b). Flip-flops enable selectable hysteresis so that circuit, once locked, will not change state until f_{in} moves below f_1 or moves above f_4. Lock and capture ranges are controlled by R_1–R_4. Hysteresis eliminates jitter that would normally occur at output if f_{in} were near f_2's or f_3's edges.

of the two timing elements, R_2 and R_3.

The curve (b) shows more clearly how the lock and capture ranges are controlled by R_1–R_4, where f_1–f_4 are equal to the reciprocals of the pulse widths determined by C_1–R_1 or –R_2 and C_2–R_3 or –R_4. A_3 will move high when f_{in} rises above f_2, and it will not move back to its initial state until f_{in} falls below f_1. Similarly, A_4 will change from a 0 to a 1 when f_{in} rises above f_4, and it will change back to a 0 only when f_{in} falls below f_3. The amount of hysteresis acting upon f_1–f_2 and f_3–f_4 can be chosen by simply selecting the appropriate resistance values for R_1–R_4.

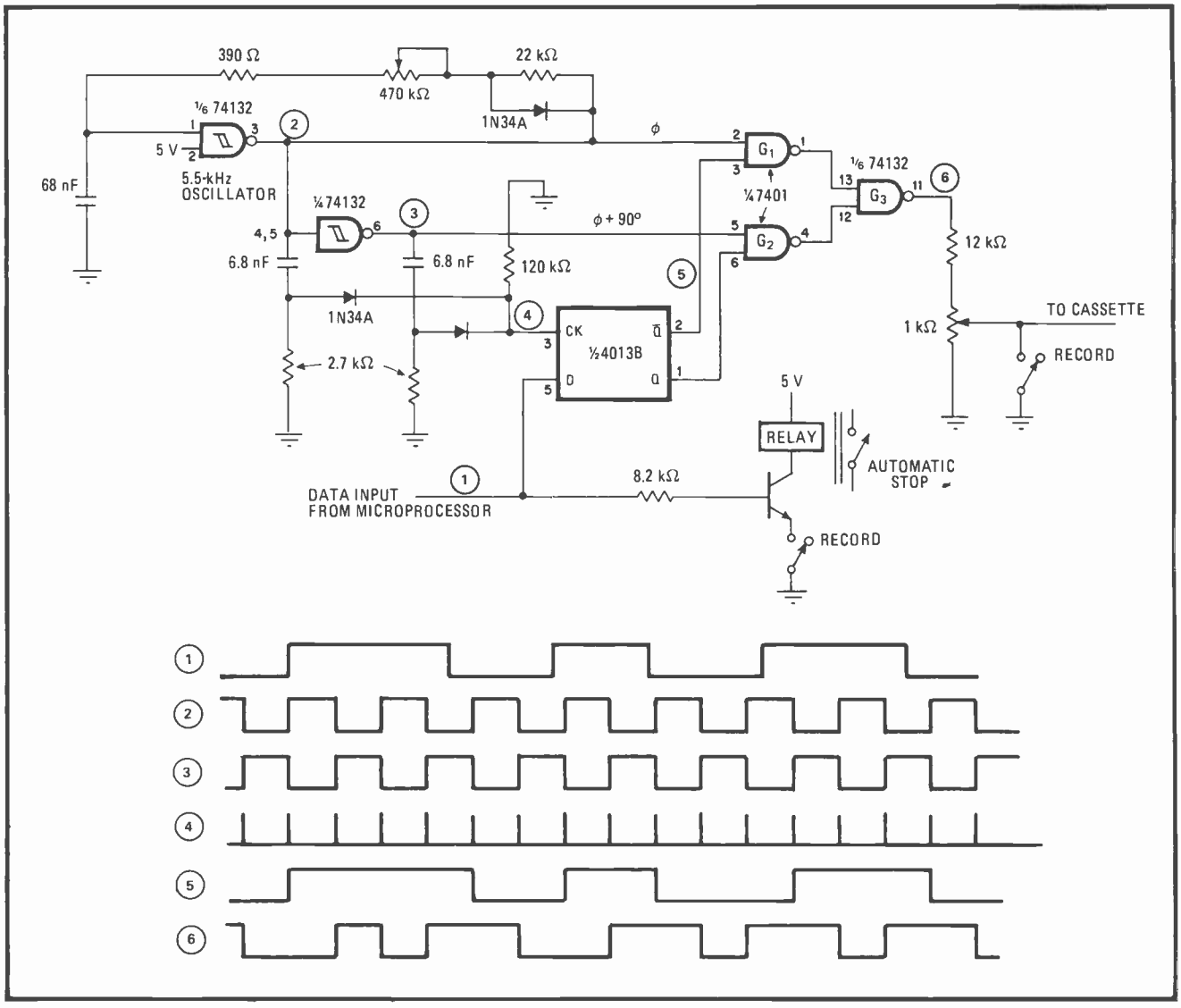
The NOR gate output moves high when f_{in} is within the set limits of f_2–f_3. It will not move low again until the input frequency falls below f_1 or above f_4. If desired, an OR gate can be used instead of a NOR gate, since both the Q and $\overline{Q}$ outputs are available in D-type flip-flops. □

Processor-to-cassette interface helps slash data-storage cost

by Pawel Mikulski
Finlux Television, Lohja, Finland

It doesn't pay to buy an expensive mass-storage device to store data handled by an inexpensive microprocessor-based data system. Storing data on a cassette tape recorder or reading data from one is a viable alternative, however, and these low-cost interfaces will provide an economical solution to the data-storage and -retrieval problem for read/write speeds of up to 4,000 bauds.

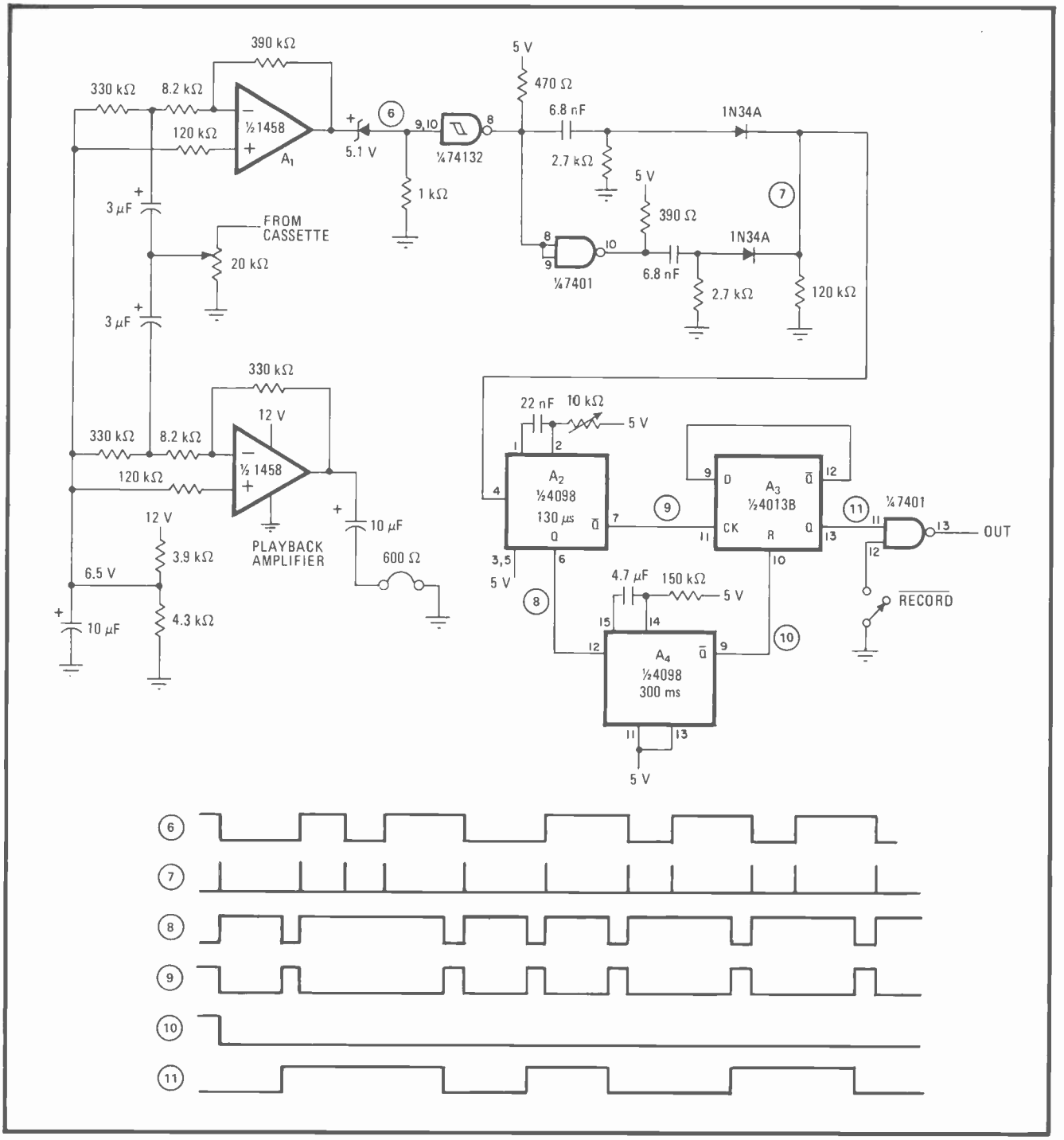
Microprocessor data is phase-modulated by the trans-



1. Inexpensive. Low-cost microprocessor-to-cassette interface can be used with tape recorder to form economical data-storage system. Interface converts input to pulse-modulated waveform so that data may be easily stored in cassette recorder.

mitter interface as shown in Fig. 1, in order that it may be stored in the recorder in a form that may be easily retrieved. The input signal drives G_1 and G_2 and, depending on the logic value (0 or 1), will determine if either phase ϕ or $\phi+90^\circ$ (both generated by a 5.5-kilohertz oscillator) appears at the output of G_3. This signal is then stored in the cassette. The transmitter timing diagram clarifies circuit operation.

Data played back to the receiver (Fig. 2) is applied first to A_1 and then to a Schmitt trigger/comparator (74132). A_2, a retriggerable one-shot, is fired on every rising and falling edge of the input signal and thus will stay high if the input signal pulses are separated by less than 130 microseconds. A_2 drives A_3, a D-type flip-flop wired as a T device, so that the output will be a replica of the data signal originally recorded. A_4 is a time-out one-shot, which moves high ($\overline{Q}$) if data input should cease for more than 300 milliseconds. Circuit operation can be clearly visualized with the aid of the receiver's timing diagram. □



2. Retrieved. Data is recovered after passing through receiver interface using process essentially inverse to one used at transmitter. One-shot A_2 is used to convert input signal to two complementary 130-μs waveshapes. One waveform drives a second one-shot, A_4, which in turn resets A_3, while the other waveform drives its clock input. Timing diagram details operation. Output is a delayed version of the original signal.

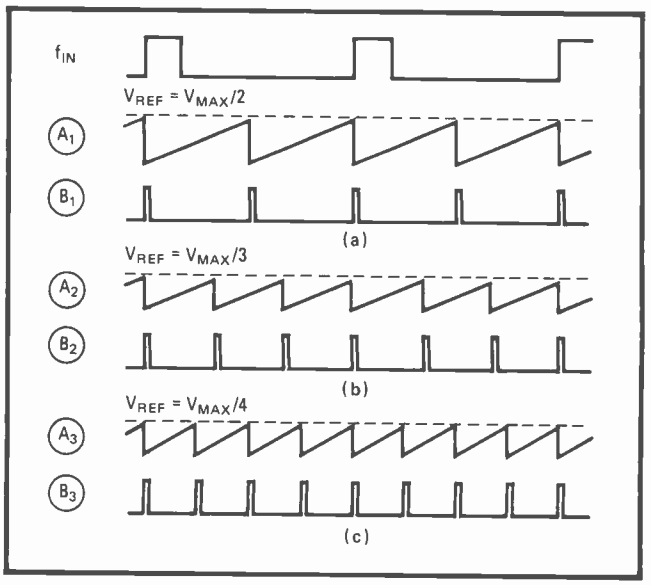
Programmable multiplier needs no combinational logic

by Noel Boutin
University of Sherbrooke, Electrical Engineering Department, Quebec, Canada

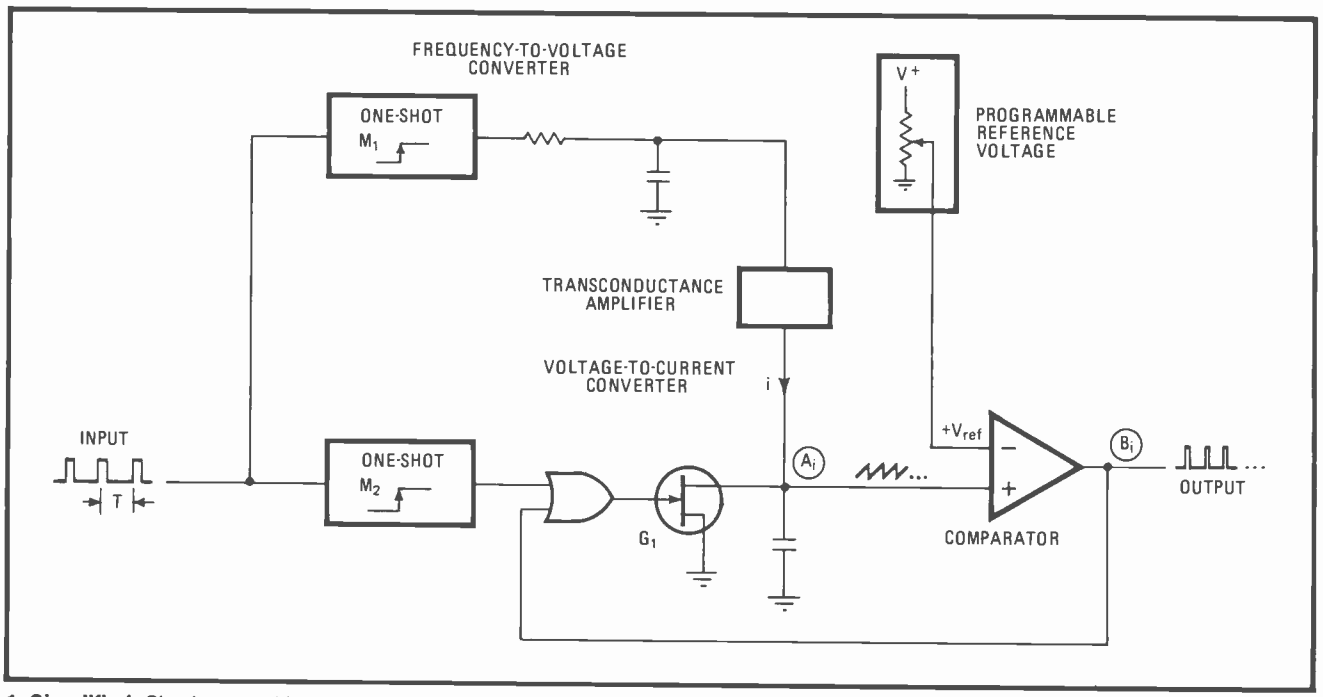
The frequency multiplier circuit proposed by R. J. Patel [reference is to circuit shown on page 8] can be vastly simplified for applications where the duty-cycle of the output waveshape must or may be kept low. Specifically, no combinational logic is needed for a frequency multiplication of N, and only one comparator is used in place of the N − 1 comparators required in Patel's circuit. A programmable voltage reference, which can be just a potentiometer, a digital-to-analog converter, or a keyboard [*Designer's Casebook*, Dec. 22, 1977, p. 80], can be used to set the multiplication ratio desired.

The modified circuit is shown in Fig. 1. Two one-shots are fired on the positive edge of each input pulse, f_{in}. The input signal may have almost any duty cycle.

Emanating from the transconductance amplifier is a sawtooth waveform, which has a period determined by M_2. The one-shot drives one input of an OR gate that switches gate G_1 on at regular intervals. Connected to the other input of the OR gate is the output of a comparator, which turns on G_1 and resets the ramp whenever the value of the sawtooth amplitude exceeds the value set by the programmable reference voltage at the comparator's inverting port. This operation is shown in the timing diagram of Fig. 2 for multiplication ratios of 2, 3, and 4, respectively. Thus frequency multiplication is achieved by the feedback signal from the comparator, not by the use of combinational logic, which derived the output wave from the input signal in Patel's circuit. The



2. Two, three, four... Frequency doubler (a), tripler (b), and quadrupler (c) are easily synthesized by adjusting the ratio V_{max}/V_{ref} with the programmable reference source. Output signals are pulses, but may be converted to square waves by adding a flip-flop operating as divide-by-2 counter to comparator output.



1. Simplified. Circuit can achieve frequency multiplication without using logic or more than one comparator (see text). Multiplying signal is derived from input wave and comparator, which periodically resets sawtooth each time the ramp itself exceeds a present reference voltage.

number, N, of equally spaced spikes that appears at the output of the comparator during each period of the input signal is given by $N = V_{max}/V_{ref}$, where V_{max} is the maximum voltage that would be reached if the feedback signal were not present.

If a symmetrical output (square wave) is required, a flip-flop operating a divide-by-2 counter can be added to the output of the comparator. It will also be necessary to adjust the multiplication ratio to twice the desired value (2N) in order to recover a square-wave output frequency of Nf_{in}. □

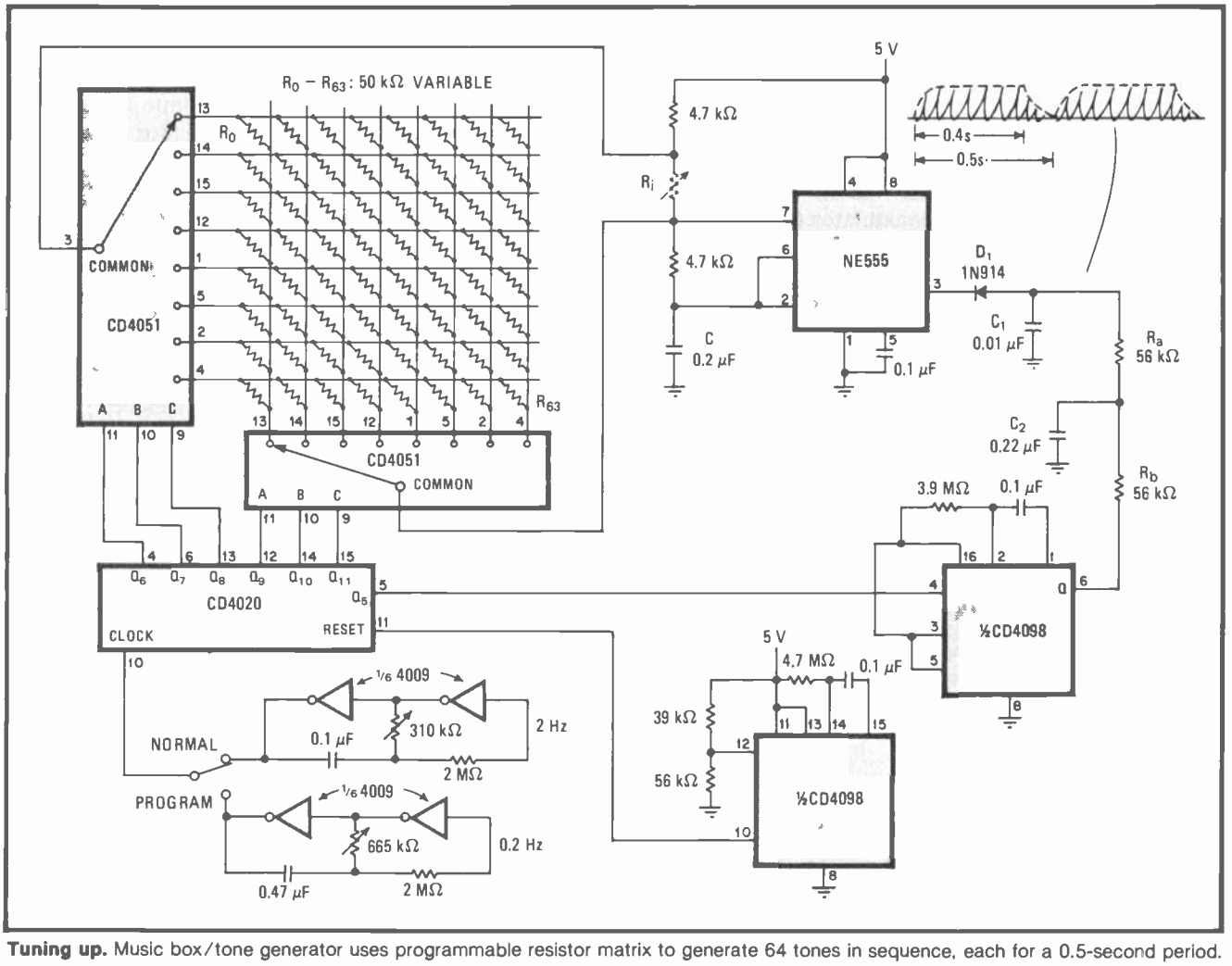
Resistor matrix orchestrates electronic piano/tone generator

by Hsi Jue Tsi
National Taiwan University, Taipei, Taiwan

Combining an eight-by-eight-resistor matrix that is programmed to generate 64 different frequencies with control circuits that send each tone in sequence for half-second intervals, this unit makes a tuneful electronic music box. It can also serve as a programmable tone generator for testing purposes, in which case the number of tones may be extended to 512.

In this circuit, the resistor timing element in an astable multivibrator is periodically switched to a new value every half second with the aid of a multiplexer circuit. Serving as the multivibrator (or tone generator) is the versatile 555 timer, which can generate frequencies over a range of 100 hertz to 5 kilohertz.

Timing resistors are switched into the R_iC network with the aid of two CD4051 multiplexers, as shown. Each device has three address ports that are updated by a 4020 counter, which is in turn stepped by an oscillator normally running at 2 Hz. If, for example, all outputs of the 4020 are low, the common ports of the 4051s will be



Tuning up. Music box/tone generator uses programmable resistor matrix to generate 64 tones in sequence, each for a 0.5-second period. Oscillator clocks 4051s, which in turn place each of 64 resistors in timing network of 555. Output of timer is shaped by a 4098 one-shot and suitable integrator network for click-free output during switching. Matrix can be programmed in 10 minutes if counter is available.

connected to row 1, column 1, of the matrix and R_0 will be in the 555's timing loop. As the counter steps through all locations, R_1–R_{63} in turn set the frequency of the 555.

The output of the 555 is a train of square waves. To avoid the key clicks that occur each time the frequency of a tone is changed, the square wave is rounded off, being converted to a sawtooth wave with D_1, R_aC_1, and R_bC_2. Note that the 4098 monostable multivibrator connected to R_b aids greatly in controlling the attack-delay characteristic of each waveform at the output; it applies a gradual turn-on bias to D_1 initially and then a turn-off bias after about 0.4 second. This 4098 is driven by the 4020. R_b and C_2 integrate the 4098's output pulse, then C_2 discharges, enabling the device to bias the diode as described. A second 4098 one-shot is used to reset the 4020 so that resistor R_0 will be immediately accessed on power-up.

Programming of the resistor values can be tedious, but with practice it can be done in 10 minutes. A frequency counter connected to the output of the 555 is helpful. Despite the harmonics in the 555's output, the counter will read the fundamental frequency of a given tone.

First, it is necessary to switch to the program clock. This clock will advance the 4020 counter once every 5 seconds and gives the user time to adjust each R_i for the particular output frequency desired during that span. Two passes over the 64 tones should be adequate.

If a counter is not available, a piano or tuning fork will be needed and tuning will have to be done by ear, requiring an extremely long programming time. Means will also have to be found to single-step the 4020.

For more demanding applications, the number of tones can be expanded to 512 by adding another CD4051 and the appropriate number of resistors. □

Double-balanced mixer has wide dynamic range

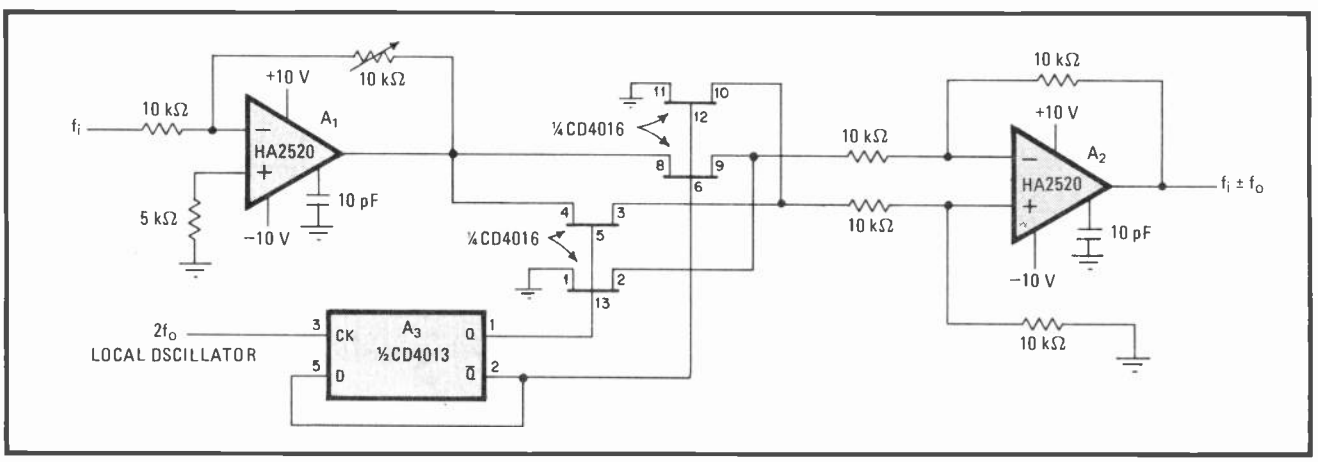
by Carl Andren, Eric Heinrich, and William Mosley
E-Systems Inc., St. Petersburg, Fla.

This double-balanced mixer is ideal for use in frequency-division-multiplexed systems and because of its extremely wide dynamic range will also find use as the baseband mixer in phase-shift-keyed demodulator circuits. Operating linearly on input signals extending from 5 microvolts to 5 volts at frequencies from dc to 1 megahertz. the circuit owes its wide range to a combination of factors, notably a balanced output-stage configuration, low offset voltages in its switching circuits, low local-oscillator feedthrough, and the low-noise output of the active devices used. The mixer has the additional advantages of a very low output impedance and extreme stability over a wide temperature range.

The mixer is shown in the figure. A_1, serving as a wideband buffer amplifier with selectable gain, routes input signal f_i toward A_2 through the CD4016 quad analog switches. The CD4016, which contains four transmission gates, is turned on through A_3 by a local oscillator signal (which equals, in this case, $2f_o$), alternately switching A_2 between its inverting and noninverting modes. This action varies the gain of the amplifier from +1 to −1, so that the amplifier performs a chopping (mixing) operation on the input signal.

The input signal, f_i, is thus translated into a frequency of $f_i \pm f_o$ at the output of A_2. Mixer balance is achieved by using the combination of a symmetrical driving source for the switches (Q and $\overline{Q}$ output of the 4013) and a symmetrical input circuit for amplifier A_2. Thus the local oscillator (carrier) will be effectively suppressed at the output—feedthrough will be 60 decibels below the amplitude of the f_i signal. Double balancing ensures that the input-signal feedthrough will also approach the −60-dB value.

An added benefit of A_2's balanced input circuit is that the switch-transient feedthrough is reduced. This is because the pulses introduced to both ports of the op amp are about equal, and because the differential input voltage is therefore near zero, the output of A_2 is approximately zero for these transient components. □



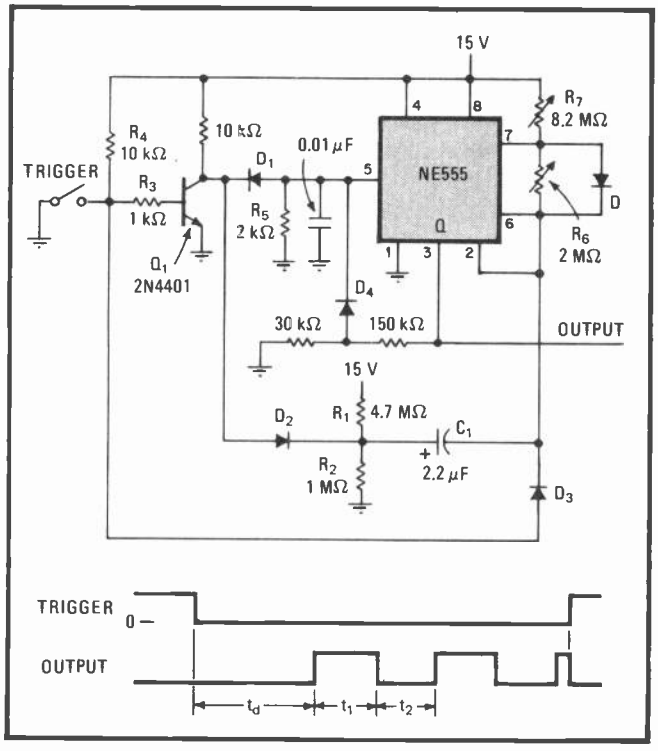
Dynamic. Mixer operates linearly over input-signal range extending from 5 μV to 5 V. Double-balanced circuit reduces local-oscillator and input-signal feedthrough to −60 dB below f_i. Switch-transient feedthrough is reduced by A_2's balanced input circuit.

Timer's built-in delay circumvents false alarms

by Kamalakar D. Dighe
American Instrument Co., Silver Spring, Md.

A single 555 timer operating as an astable multivibrator can be used to set its own delay time before turning on, thereby circumventing the most annoying problem encountered with threshold-detector and industrial-alarm circuits—how to distinguish between an actual trigger signal and one that is generated by noise. With this circuit, a wide range of delay periods can be selected to negate the effects of noise spikes.

The circuit requires one transistor and several diodes to function, as shown in the figure. During the quiescent (no-trigger) condition, Q_1 is biased on, D_1 clamps pin 5 of the timer to the approximately 0.8 volt, and D_2 is back-biased. The R_1–R_2 voltage divider maintains the positive plate of capacitor C_1 at 2.5 v and the R_3–R_4 divider ensures that there is 1.5 v at the negative plate (D_3 is forward-biased). Thus the initial voltage across C_1 is 2.5 − 1.5 volts, or 1 v. Under these conditions, pin 6 is at a higher voltage (1.5 v) than the control voltage (V_c) at pin 5, and so the output of the timer at pin 3 is driven low, back-biasing D_4.



Sure-fire. Circuit can differentiate between real and noise-generated alarm signal by waiting a user-specified time before turning on. Frequency and duty cycle of astable multivibrator can be tailored for optimum response from loudspeaker or other audio-alarm monitor.

The delay period begins when the trigger or alarm input, represented by a switch, is grounded. Q_1 turns off, and the collector voltage climbs to 15 v, back-biasing D_1 and bringing pin 5 to 3.8 v (the voltage depends on R_5, which is in parallel with two 5-kilohm resistors internal to the 555).

Meanwhile, D_2 becomes forward-biased, with the result that approximately 14.5 v is applied at the positive plate of C_1, a step rise of approximately 12 v above the previous voltage. D_3 is now back-biased; the step voltage is therefore transferred to the negative plate of C_1, and pins 2 and 6 of the timer jump to 13.5 v.

Because the threshold voltage (13.5 v) is still larger than the control voltage (3.6 v), the output of the timer remains low. However, C_1 now starts to charge through R_6 and the discharge transistor within the timer. If the voltage at pins 2 and 6 reaches one half of the control voltage before the trigger input is removed, the output will move high. The time it takes the capacitor to charge to ½ V_c (that is, the delay time) is given by:

$$t_d = R_6 C_1 \ln \frac{V_m}{V_m - (V_f - V_i)}$$

where V_m is the maximum voltage, V_f is the final voltage on C_1, and V_i is the initial voltage across C_1. In this case, V_m = 14.5 v, V_f = 14.5 − ½V_c = 12.7 v, and V_i = 1.0 v. At the end of the delay period, the timer begins to oscillate at a frequency and duty cycle that can be set by the user.

When the timer's output is high, D_4 is forward-biased and the V_c voltage is clamped to approximately 2 v. C_1 is now discharging through R_7, and when the threshold voltage at pins 2 and 6 equals 2 v, the timer output moves low, reverse-biasing D_4 and restoring pin 5 to 3.6 v.

The time the output is high is given by:

$$t_1 = R_7 C_1 \ln(V_o/V_f)$$

where V_o is the initial on-state voltage of C_1 (14.5 − 1.8 = 12.7 v), and V_f is the final voltage on C_1 (14.5 − 2.0 = 12.5 v).

When the output moves low in the cycle, C_1 starts to charge through R_6. When the voltage at pins 2 and 6 drops from 2 to 1.8 v, the timer output goes high, the discharge cycle begins, and the cycle is repeated until the trigger signal is removed. The time the output is low is given by:

$$t_2 = R_6 C_1 \ln \left[\frac{V_m - (V_{f2} - V_i)}{V_m - (V_{f1} - V_i)} \right]$$

where V_{f1} = 14.5 − 1.8 = 12.7 v and V_{f2} = 14.5 − 2.0 = 12.5 v. □

Audio blanker suppresses radar-pulse and ignition noise

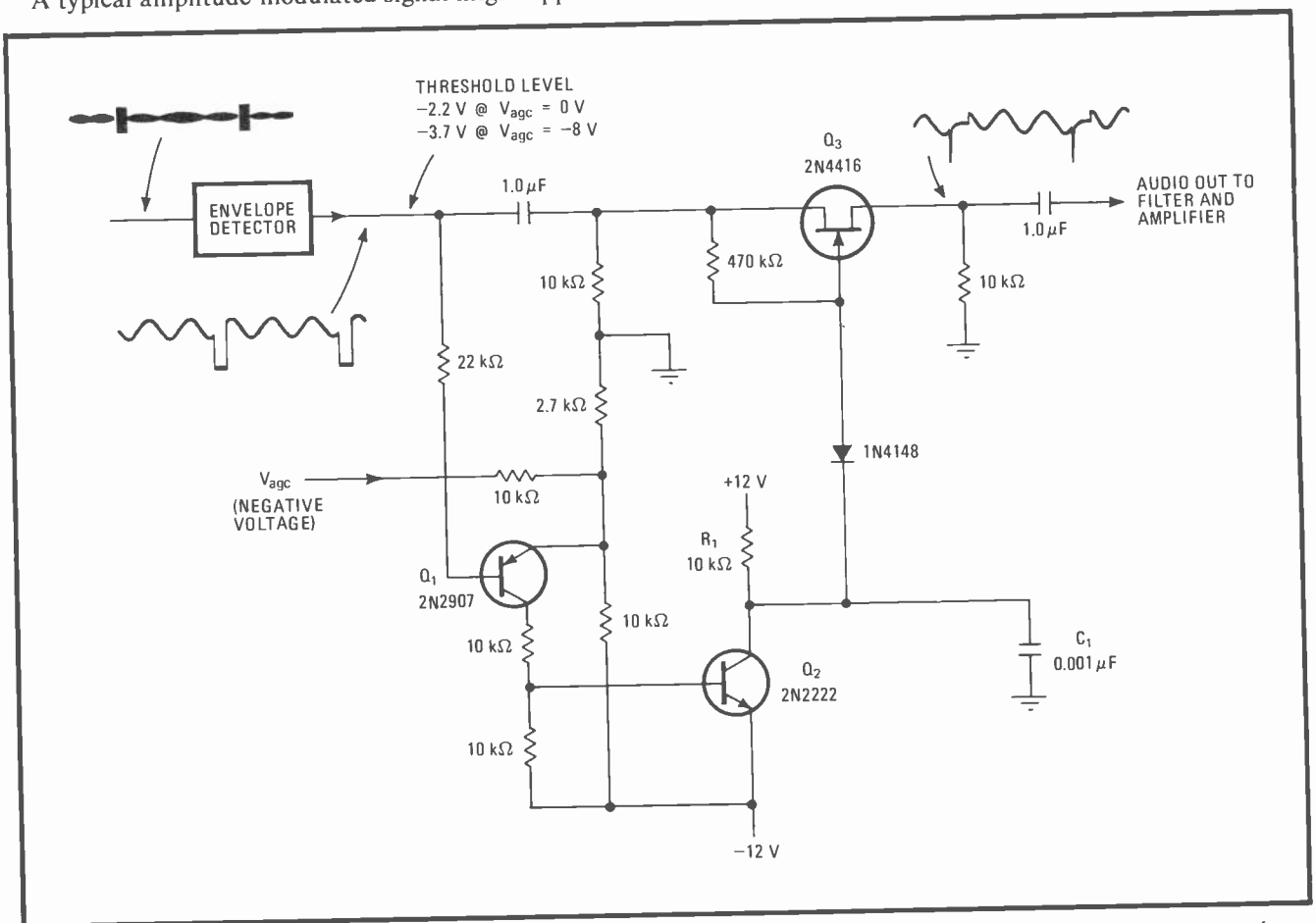
by Carl Andren
E-Systems Inc., St. Petersburg, Fla.

This simple audio-stage noise blanker will reject most repetitious, pulse-type interference, like radar and automobile ignition spikes, that often plagues a-m receivers. The circuit is both less costly and far less complex than the radio-frequency stage blankers employed in some of the more sophisticated receivers, and though not as effective in eliminating interference, it outperforms the more commonly used noise-limiting audio-clipping circuits.

The blanker shown in the figure detects whether the amplitude of an offending pulse train at the output of the receiver's envelope detector exceeds a set threshold and then disables the output stage if necessary. Waveform diagrams are shown at several circuit points to help clarify operation of the blanker.

A typical amplitude-modulated signal might appear at the input of an a-m receiver as shown in the upper left of the figure, where a 20-megahertz radio-frequency wave, modulated 30%, is overridden by radar pulses 20 decibels greater in amplitude. A time-magnified portion of the a-m detector output, after passing through an inverting operational-amplifier stage, would appear as shown, where the maximum amplitude of the pulse would be limited by the saturating level of the intermediate-frequency amplifier. Only two offending pulses are shown for clarity, but this detected signal contains a pulse train of sufficient amplitude and repetition rate to generate a substantial pulse noise and so impair the readability of the signal.

The interfering spikes increase the effective modulation percentage to well over 100%. The blanker is triggered into operation when the modulation peak exceeds 140%, whereupon Q_1 and Q_2 switch on and disable signal-gate Q_3 for the duration of each spike. The 140% threshold has been experimentally determined as the point at which the interference caused by the blanking operation itself is still less than the interference generated by the offending pulse train. Note that to ensure that the blanking action occurs at the set modulation peak independently of signal-level changes, the receiver's automatic-gain-control signal is introduced at the



Spike eater. Audio-stage noise blanker, although not as effective at eliminating pulse-type interference as rf-stage blankers, outperforms noise-limiter/clipper circuits. Blanking occurs when spikes raise effective modulation percentage over 140%. Receiver's agc signal is introduced to emitter of Q_1 to ensure that the blanking action occurs at the set modulation point independent of input signal amplitude.

threshold bias point at the emitter of Q_1.

Q_3 operates with no applied dc voltage so that no switching transients will be generated by the blanking action to impair circuit performance. Q_2, R_1, and C_1 have a fast-attack, slow-decay characteristic. Q_3 is thus gently turned on after a spike has passed so that the popping and clicking sounds that often accompany the operation of a blanking circuit that processes a randomly occurring train of spikes will be further suppressed.

The results of the blanking action are shown at the output of Q_3, where it is seen that only brief transients appear. The signal is slightly distorted, but the distortion is barely audible. There is a great improvement in noise reduction, however. □

Four-function calculator times long intervals accurately

by Steve Newman
Hospital of the Good Samaritan, Los Angeles, Calif.

Time intervals extending up to several years can be set with the aid of an inexpensive four-function calculator and an integrated-circuit divider. This timer is accurate to within a few seconds per year. The only requirements for the calculator are that it have at least an eight-digit display, a minus-sign indicator at the left-most position of the display, and a continued-operation mode, which allows subtraction of a given number repetitively by depressing a single key (usually the equal-sign button).

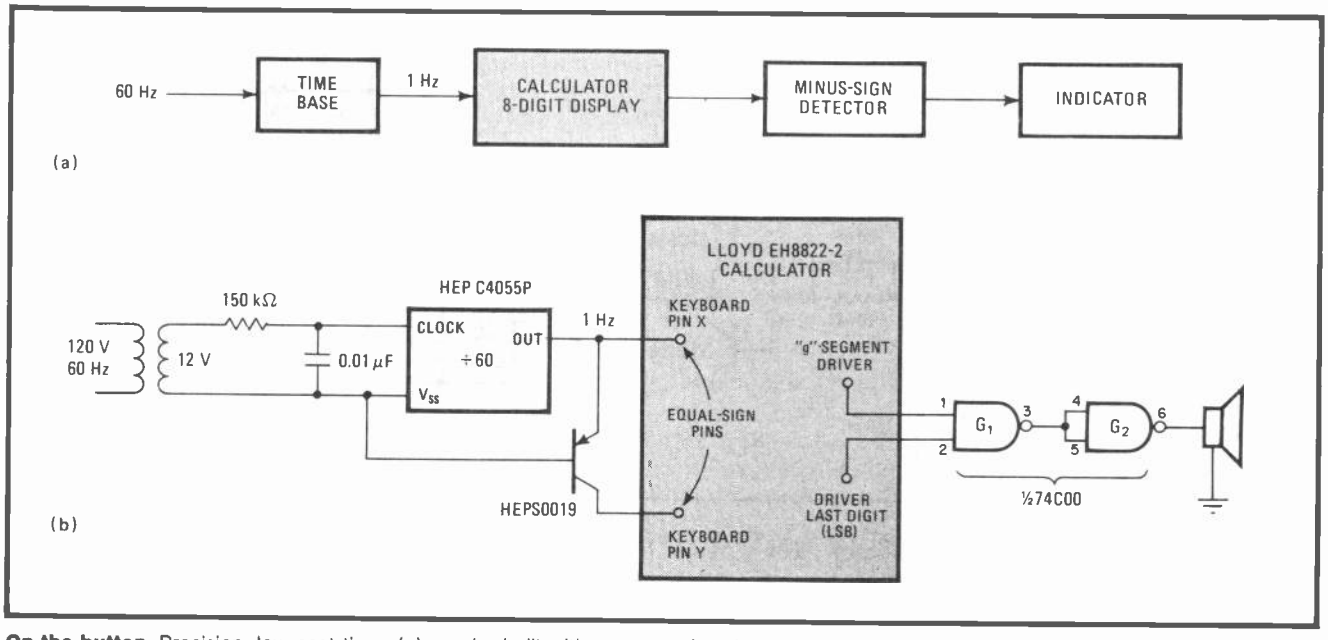
The time interval is set by keying in the desired value, expressed in seconds. For instance, if the timer is set to go off in 3 days, 10 hours, 54 minutes, and 33 seconds, the number 298,473 is entered. (With an eight-digit display, an interval of 10^8 seconds, or 38 months, can be set.) Next, the -1 command is keyed in. The calculator is now programmed to subtract 1 from the displayed value each time the equal-sign key is activated and then to display the new value.

To decrement the count at proper intervals, a precise time base is required, and the calculator's keyboard pins must be made accessible. In this case, a divide-by-60 counter, the HEP C4055P, is used to derive a 1-hertz signal from the 60-Hz power line, as shown in the figure. This clock drives the transistor switch connected across the pins corresponding to the equal-sign key, which are closed when that key is depressed in normal operation.

The timing interval begins when the time base is activated. The displayed number is decremented for each pulse emanating from the C4055P, so that after N seconds the calculator will display zero, and after N + 1 seconds it will display -1.

The minus-sign output, which is part of the display circuitry, provides a convenient way to detect the end of the set timing interval. Here, the g-segment pin corresponding to the minus-sign key is brought to one input of a NAND gate, G_1, as is the lead corresponding to the left-most digit of the display. An identical gate, G_2, follows, so that the entire logic function is that of an AND gate. This function is suitable for driving positive-logic circuits or devices.

Pulses emanate simultaneously from both the minus-sign pin and the last-digit driver port when the calculator first displays a minus value, and for every result thereafter. The first pulse may thus be used to turn on an alarm. Because many calculators scan the display at a frequency of a few hundred hertz, an audible output can be obtained if a loudspeaker is connected to G_2. □



On the button. Precision, low-cost timer (a) can be built with most any four-function calculator and integrated-circuit divider (b). Keyboard pins corresponding to equal-sign button must be accessible. Circuit is accurate to within a few seconds per year.

Ultrasonic pulser needs no step-up transformer

by Paul M. Gammell
Jet Propulsion Laboratory, Pasadena, Calif.

When a transducer is used in a pulse-echo ultrasonic system of the kind that is excited by high-voltage impulses at a low duty cycle, the device often requires the services of a bulky, step-up line transformer and switching circuits that must withstand the full supply voltage. The ultrasonic pulser shown in the figure, however, generates a 300-volt pulse train at a low-duty cycle (about 1/20,000 of a cycle rise time at 2 kilohertz) without the need for a transformer and without placing an excessive voltage on the switching devices.

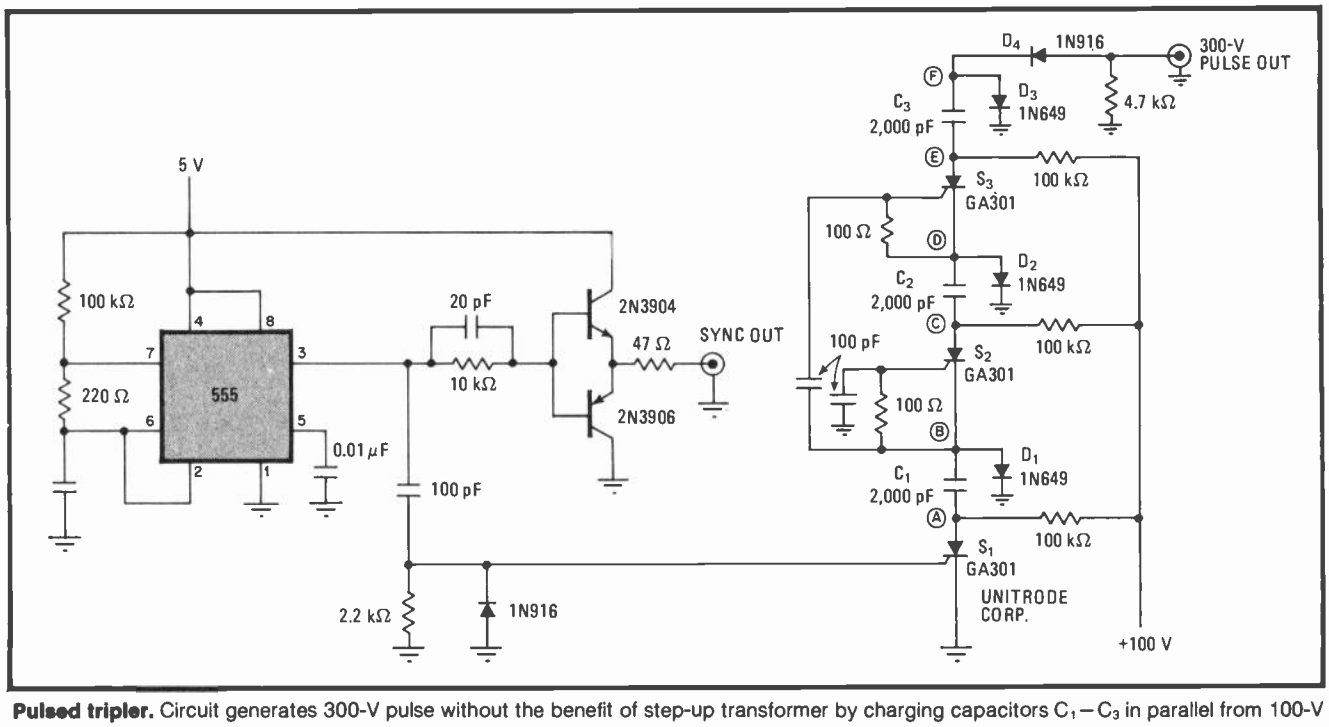
Used in place of the transformer supply is a voltage tripler circuit that arranges for each of three capacitors, in effect arranged in parallel, to be charged by a 100-v dc input voltage. The circuit then places the capacitors in series during discharge so that the output voltage is three times the input voltage. Moderately priced ($6) silicon controlled rectifiers with a fast, 10-nanosecond rise time serve as the switching elements and need withstand only 100 v each. Furthermore, since the power drain is modest, merely a few tens of milliamperes, a small power supply of the kind intended for glow-discharge displays is suitable.

As for the operation of the circuit, at times when no signal is applied to the gate of S_1, as during a power-up, S_1–S_3 are off and C_1–C_3 charge up through their respective 100-kilohm resistors and diodes, D_1–D_3.

A positive-going signal applied to the gate of S_1 by the 555 timer, which operates as an astable multivibrator at 2 kHz, turns S_1 on, pulling point A from +100 v to ground. The 555, with the aid of the Q_4–Q_5 line driver/buffer, generates a waveform at the sync output that precedes the pulse to S_1 by 2 microseconds or so and thus is suitable for triggering a scope.

Because the voltage across C_1 cannot change the instant S_1 switches, point B also changes by 100 v, moving from ground to −100 v. Point B was clamped close to ground potential by D_1 during the charge period but is free to make negative excursions after the period ends. S_2 then turns on. The RC network connected to the gate of S_2 limits gate current to a safe value and allows the SCR to return to the off condition when required. With S_2 on, points B and C assume the same potential of −100 v. Because C_2 is charged to 100 v, point D is pulled to −200 v.

The cathode of S_3, which is connected to point D, also assumes a value of −200 v, while the gate is at −100 v for a brief instant. S_3 thus turns on. In a like manner described above, point F is pulled to −300 v. The fall in voltage from 0 to −300 v happens in 20 to 30 μs, then decays back to zero at a rate determined by the output load resistance and capacitance. D_4 has been incorporated to isolate the particular receiver used in the system from any noise generated in the pulser's high-voltage



Pulsed tripler. Circuit generates 300-V pulse without the benefit of step-up transformer by charging capacitors C_1–C_3 in parallel from 100-V source and then discharging them in series. Output has repetition rate of about 2 kHz and a rise time of only 20 to 30 ns.

supply and also to minimize the loading of the receiver by the pulser during receive (echo) time slots. The high-speed, low-voltage diode used for D_4 is adequate in most cases, since it never needs to stand off more than a few volts unless a highly reactive echo signal is reflected back into the pulser. The resistor at the output of the circuit provides a dc return path for the output pulse.

The use of slow diodes for D_1–D_3 does not preclude obtaining pulses of fast rise times at the output. Because C_1–C_3 are fully charged when a pulse is commanded, there is practically no current flowing through D_1–D_3; hence, there are no stored carriers.

Additional voltage-multiplying stages may be added as required, using the technique described here. The rise time at the output will increase slightly for each new stage added. □

Up-down ramp quickens servo system response

by R. E. Kelly
Southwest Research Institute, San Antonio, Texas

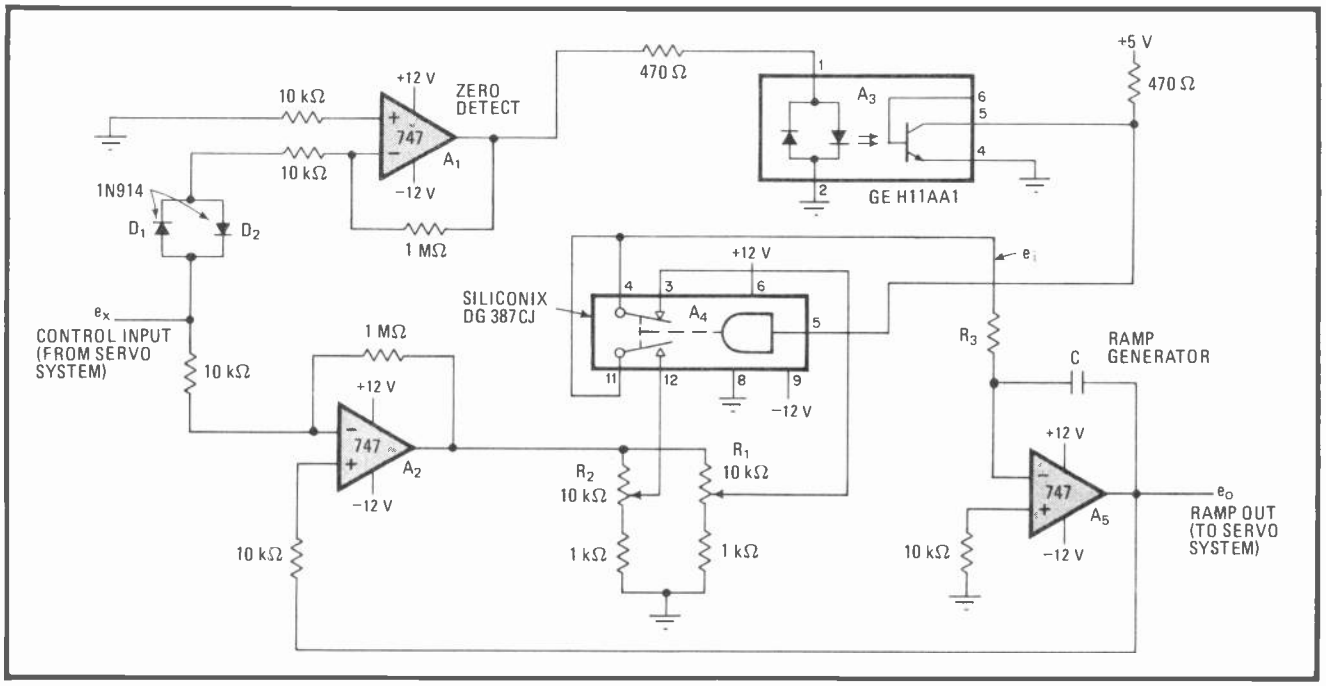
Servo systems often require a ramp waveform to control both the acceleration and deceleration rates of heavy loads, but all too often system complexity and reaction time are increased because only a positive-going, fixed-slope ramp is available for performing the dual function. Using a dual-polarity ramp generator that allows individual selection of both the up- and down-ramp rates, such as that shown in the figure, ensures optimum servo system response at low cost.

Command-input voltage derived from the servo system's joy-stick (control) position is applied to operational amplifiers A_1 and A_2, as shown. Diodes D_1 and D_2 provide a 0.7-volt drop of the input signal before it is introduced to A_1.

When the control-input voltage is above or below zero by more than 0.7 v, the system load must be accelerated to a position corresponding to that control voltage. A_1 detects that the input voltage is other than zero and switches phototransistor A_3 on, which in turn switches A_4. Meanwhile, A_2 will switch from a positive voltage to −12 v if the control voltage is equal to or greater than the ramp's output voltage. A_3 provides a high-impedance input for A_1 and an output signal suitable for driving transistor-transistor or similar logic. A_4 is a solid-state, single-pole, double-throw relay that initiates an up-ramp waveform whose slope is partially controlled by the value of R_1.

The positive-going ramp emanating from A_5 will move the system load toward its desired position, and as that occurs, the servo system's feedback voltage will act to reduce the control-input voltage. When the input voltage moves within 0.7 v of ground, A_1 moves low and A_3 turns off. A_4 now initiates a down-ramp waveform to decelerate the system to a stop at a rate determined partially by R_2.

The ramp generator, A_5, is an op-amp integrator that produces waveforms whose rate is proportional to the input voltage, e_i. This voltage, in turn, is set by R_1 or R_2. The time-dependent voltage output from the ramp generator is approximately equal to the voltage across C. C is charged by a steady current $I = e_i/R_3$, so that:



Placement. Up-down ramp generator with selectable-slope capability can efficiently position heavy servo-system loads. Key to operation is solid-state relay A_4, which switches from up ramp to down ramp to decelerate load when it zeros in on terminating position.

$$e_o = e_i\, t/R_3C \qquad (1)$$

because $e_o = e_c = It/C$.

Equation 1 is useful for setting the values of R_3 and C needed for a given ramp slope. For example, assume that the maximum positive-going or negative-going ramp rate must be 20 V/second and that e_i is 12 V maximum. Then, from Eq. 1, $20 = 12/R_3C$ and therefore $R_3C = 0.6$. Assuming a nominal value of 0.33 microfarad for C, R_3 is then equal to 1.81 megohms.

Using the component values shown in the circuit allows a linear ramp to be generated over a 10 : 1 frequency range. Note that once the component values for the maximum ramp rate are determined, the actual ramp rate may be selected by setting R_1 and R_2 for the corresponding value of e_i. □

Twin regulators deliver constant voltage and current

by Ladislav Grýgera and Milena Králová
Tesla-Popov Research Institute, Prague, Czechoslovakia

Cascading two μA723 precision voltage regulators in such a way as to enable them to monitor both output voltage and load current yields a circuit that can generate a constant-voltage, constant-current output. Output voltage can be adjusted over a range of 0 to 15 volts at a load current that is selectable from 0 to 3 amperes with the configuration shown.

In this circuit, output voltage is controlled by A_1, which monitors load voltage with the aid of the associated network that is connected to the ports of its error-voltage amplifier (pins 4, 5, and 6). Any change in load current is detected by A_2, which acts to generate a signal at its V_{out} port.

The current-limit input of A_1 is then activated, and thus the current-limiting transistor internal to A_1, which acts as a shunt across the error amplifier, can control the amount of driving current supplied to pass transistor Q_1 at the set output voltage.

The output voltage is adjusted by R_1. The value of R_1 required is approximately 1 kilohm for each volt appearing at the load R_L. Because $R_2 = R_3$,

$$V_{out} = K_1R_1V_{ref1}$$

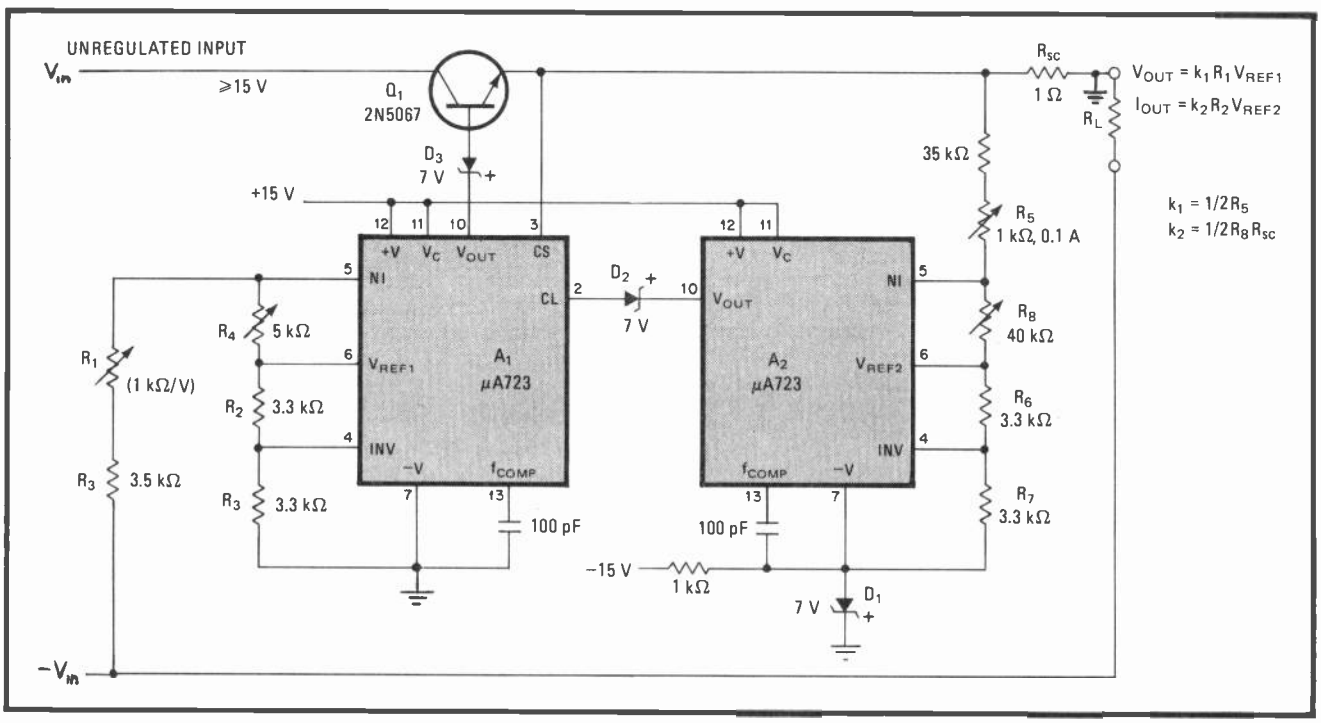
where $K_1 = 1/2R_4$.

Output current is adjusted by R_5, the value of which will increase 1 kilohm for every 100-milliampere increase in load current. Assuming $R_6 = R_7$, then it can be shown that:

$$I_{out} = K_2R_5V_{ref2}$$

where $K_2 = 1/2R_8R_{sc}$.

Zener diode D_1 allows selection of the output current down to zero. Diodes D_2 and D_3 provide well-defined switching thresholds for A_1 and Q_1 to enhance the circuit's response time to a changing output current and/or voltage. □



Steady. Cascaded regulators, one for monitoring load voltage, the other for current, form circuit that generates constant-voltage, constant-current output. Current and voltage are adjustable from zero. Maximum output voltage is 15 V; current limit depends on Q_1's rating.

Photodiode and op amps form wideband radiation monitor

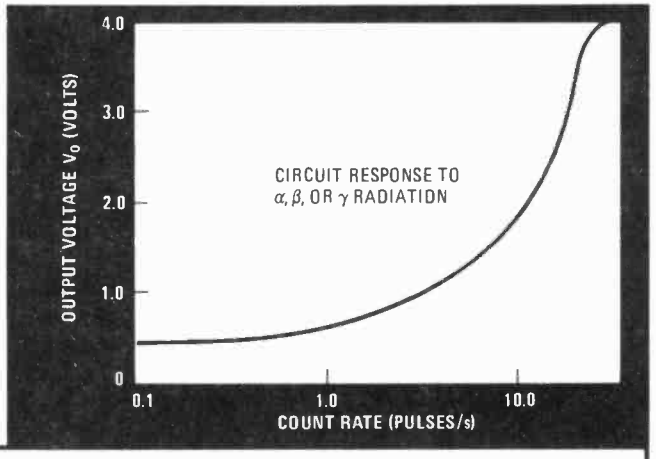
by Grzegorz Hahn
Institute of Nuclear Research, Swierk, Poland

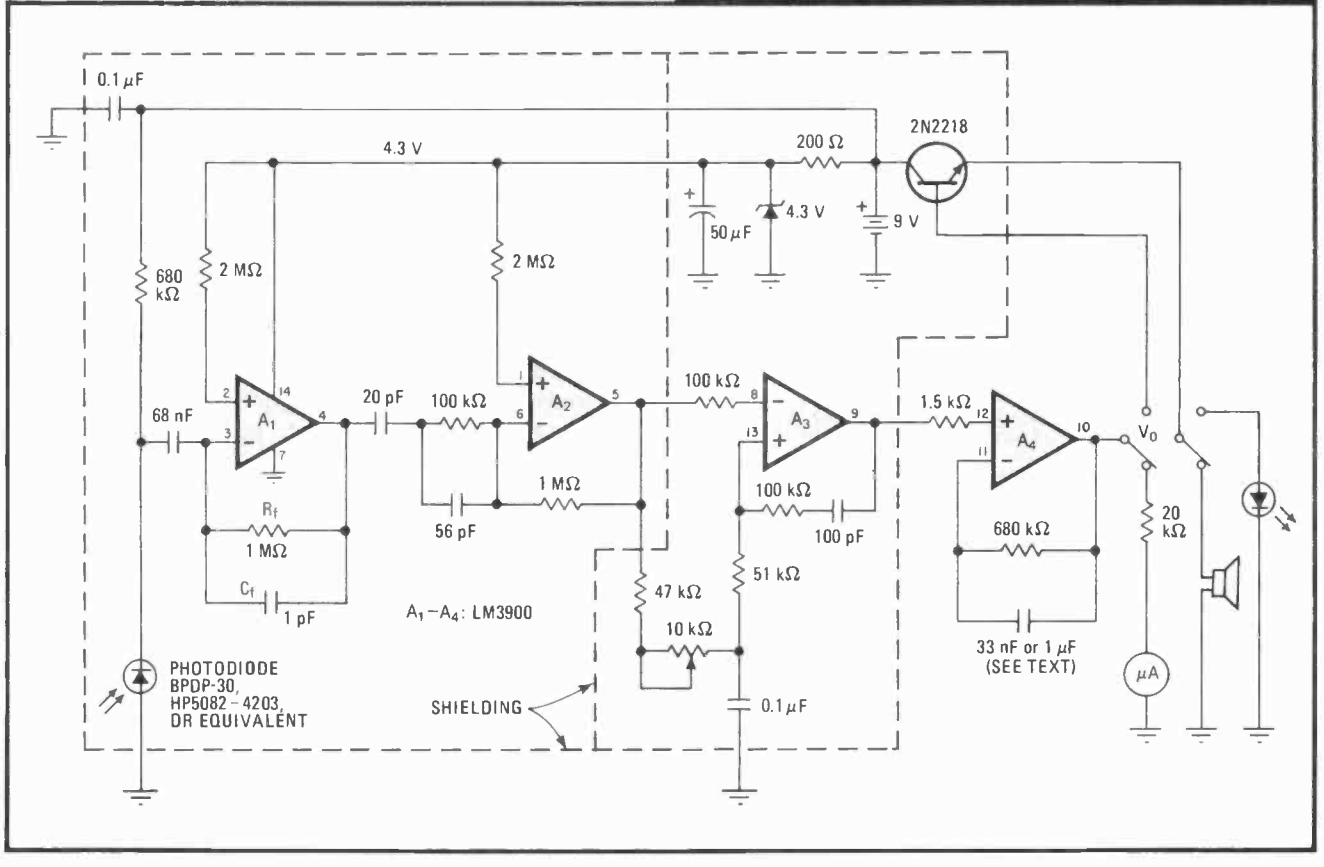
A sensitive radiation monitor may be simply constructed with a large-area photodiode and a quad operational amplifier. Replacing the glass window of the diode with Mylar foil will shield it from light and infrared energy, enabling it to respond to such nuclear radiation as alpha and beta particles and gamma rays.

The general circuit is shown in Fig. 1. The HP-5082-4203 device is a p-i-n photodiode, called that because there is a thin layer of undoped, or intrinsic, material between the p and n type regions of the diode. The intrinsic material acts to lower junction capacitance, so that the device has a higher frequency response than a standard photodiode, making possible the detection of beta particles and gamma rays (alpha particles could be detected with a standard photodiode).

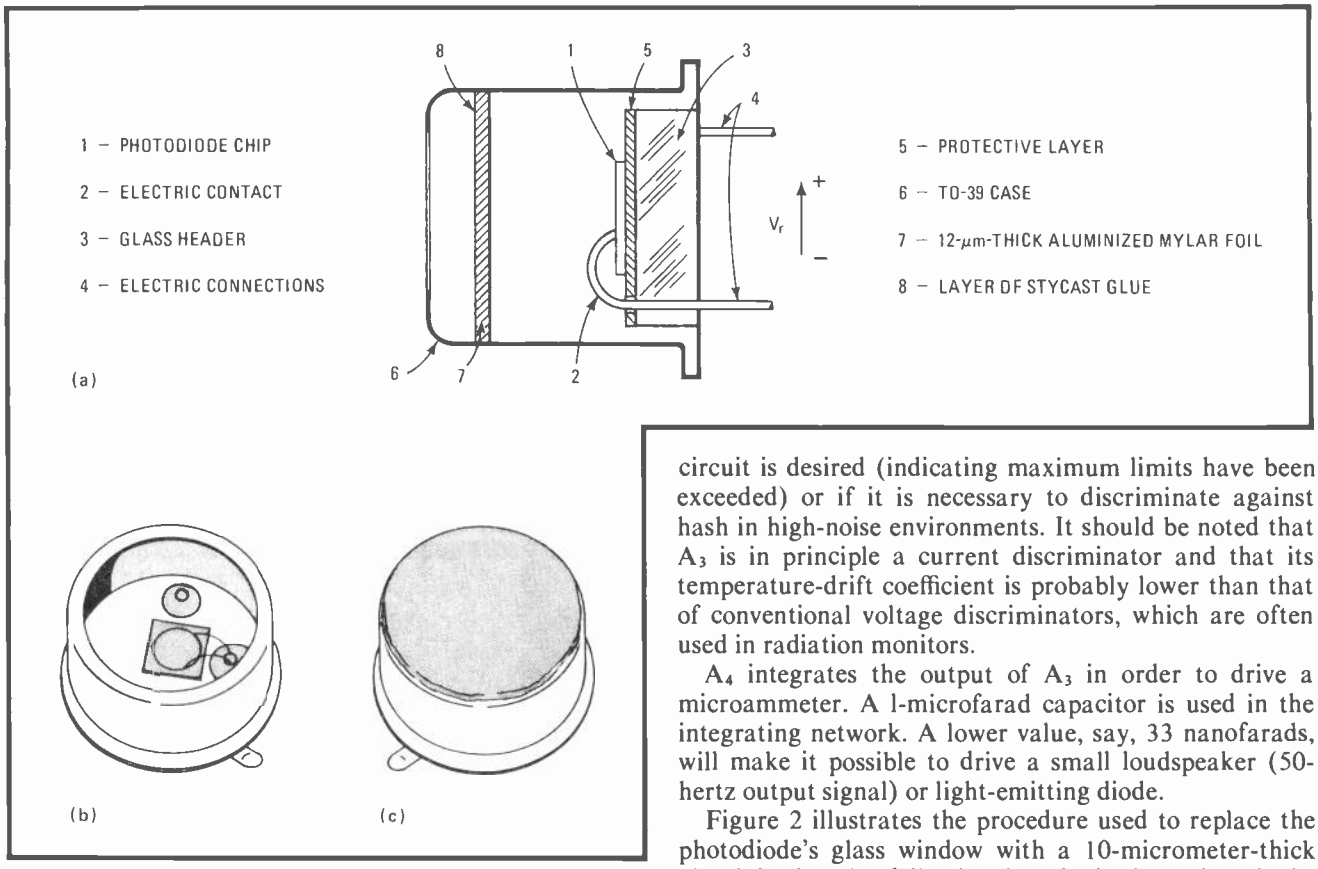
As a consequence of the p-i-n semiconductor structure, the device bandwidth is large. Hole-electron pairs, and thus charge (Q), can be accumulated across the photodiode by all forms of ionizing radiation. When the junction is shielded from visible and infrared light, the photodiode output is a function of the nuclear-type radiation only.

The junction charge generated by the ionizing radiation is $Q = \Delta E/\epsilon$, where ϵ is the ionizing constant of





1. Energy count. Broadband characteristics of p-i-n photodiode enables it to respond to α, β, and γ radiation when pn junction is shielded from visible and infrared wavelengths. Op-amp circuit amplifies and integrates pulses for meter or loudspeaker. Circuit has uniform response to radiation, independent of energy class.



2. Adaptation. Glass window of photodiode (a) must be removed and replaced by opaque material to shield pn junction from light. Top of photodiode case is first cut out (b) by turning lathe, then layer of aluminized Mylar foil is secured in place (c) with Stycast glue.

silicon (3.66 electronvolts at 300 K), and ΔE is the energy stored across the active region of the photodiode. The output voltage from integrator A_1 is thus:

$$V = (Q/C_f)\,(1 - e^{-t/RfCf})$$

where t is measured from the instant ΔE appears across the junction and R_fC_f is the time constant of the integrating network. A_2 is a quasi-Gaussian filter that shapes the pulse in order to inprove the signal-to-noise ratio of the small output signal at A_1. A_3 generates a rectangular pulse with a width proportional to the input amplitude for every signal that exceeds a threshold set by the user.

The threshold control is used if a radiation alarm circuit is desired (indicating maximum limits have been exceeded) or if it is necessary to discriminate against hash in high-noise environments. It should be noted that A_3 is in principle a current discriminator and that its temperature-drift coefficient is probably lower than that of conventional voltage discriminators, which are often used in radiation monitors.

A_4 integrates the output of A_3 in order to drive a microammeter. A 1-microfarad capacitor is used in the integrating network. A lower value, say, 33 nanofarads, will make it possible to drive a small loudspeaker (50-hertz output signal) or light-emitting diode.

Figure 2 illustrates the procedure used to replace the photodiode's glass window with a 10-micrometer-thick aluminized Mylar foil. The photodiode shown here is the BPDP-30, a European make, but most photodiodes made in the U. S. are very similar.

As shown in Fig. 2b, the top of the TO-39 case containing the window must be cut away with a turning lathe. Care should be taken not to touch the pn junction within. Sharp edges are then filed smooth with care. The new window is then secured to the edges of the device by means of black Stycast glue (available from Emerson and Cuming Inc., Canton, Mass.). Figure 2c is a view of the completed diode.

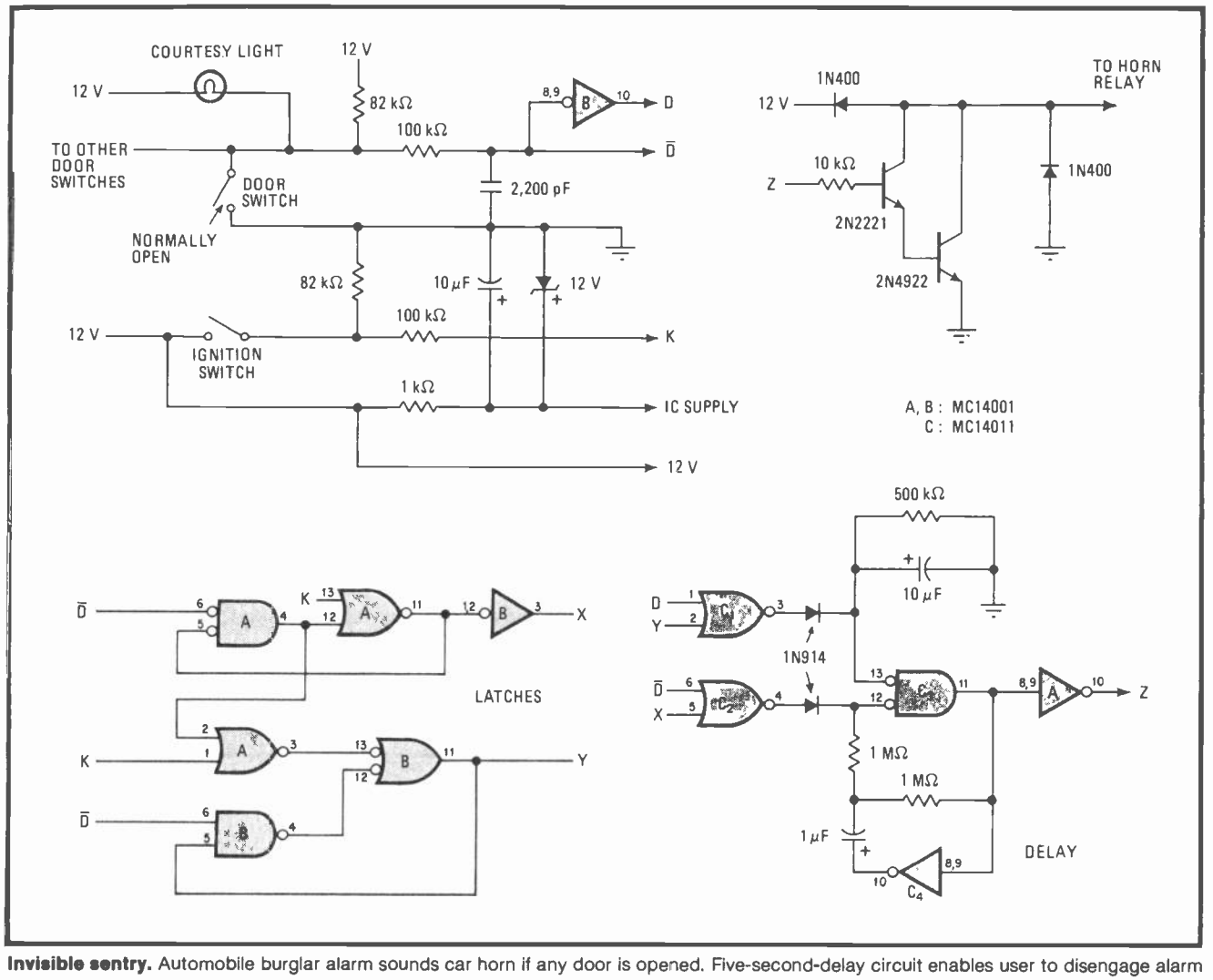
The circuit response is seen in the upper part of Fig. 1. Note that this device is a radiation monitor, as opposed to a radiation meter, and so cannot distinguish between α, β, and γ radiation. Because of the photodiode's wide bandwidth, each energy class generates the same output voltage for a given radiation intensity. Thus the monitor is intended for use where an *a priori* knowledge exists of the type of energy to be encountered. □

Vehicle-intruder alarm has automatic set/reset switching

by M. B. Horan
Derby, England

Providing fully automatic operation at negligible stand-by current, this low-cost burglar alarm for automobiles will sound the horn if any door is opened. No alarm-set switch is required on the body of the automobile: there is a built-in time delay between the opening of the door and the sounding of the alarm, which gives the driver time to activate the ignition circuit and so disengage the alarm. Resetting the circuit requires only that the driver open a car door before the ignition key is removed, thereby engaging the alarm circuit.

The alarm has been designed using complementary-metal-oxide-semiconductor logic, because it is inexpensive, rugged, reliable, and available, requires only a few



Invisible sentry. Automobile burglar alarm sounds car horn if any door is opened. Five-second-delay circuit enables user to disengage alarm just by turning on ignition. Alarm is reset by opening car door before ignition circuit is disengaged.

microwatts of power, and has good noise immunity. The circuit is simple, as the figure shows. Only six connections are required to interface it with the auto—two for the ignition, two for the door switches, and two for the horn relay.

The circuit must distinguish between several asynchronous events encountered in normal operation and store their present states so that:

- The horn will sound approximately 5 seconds after the time any door is opened, provided the ignition switch is not engaged.
- Once the horn sounds, it will continue to do so, independent of the position of any door.
- The alarm can always be reset by engaging the ignition switch.
- If the door is opened with the ignition on, and then the ignition is turned off and the door subsequently closed within 5 seconds, the horn will not sound.

In order to perform these tasks, the circuit implements the function:

$$Z = (D+Y)(\bar{D}+X)$$

where $X = K+DX$, $Y = K+DX+\bar{D}Y$, and K is true high for ignition switch-on, D is true high for an open door, and Z is true high for detection of an intruder.

Implementing the logic for the condition where one is entering the vehicle is simple. The equation given becomes more involved, however, because the circuit must allow the operator to leave the auto while setting the alarm without triggering the horn. The logic to implement this fourth condition is controlled by two latches, one of which generates the secondary variable X and the other generating Y. X is set high, also allowing Y to be set high when the condition occurs. Latch Y remains high, ready to reset on the opening of any door. Latches X and Y and the door signal are then gated to preset the alarm signal.

The alarm-gating signal (Z) is actually generated once the 1-microfarad capacitor in the delay oscillator discharges below gate C_3's logic-1 point, about 5 seconds after the X signal arrives at C_2. The inverting-gate astable multivibrator, C_4, modulates the horn at 1 hertz to enhance effectiveness as an alarm signal. Other components are included in the circuit for protection against switching transients. □

Tuning-meter muting improves receiver's squelch response

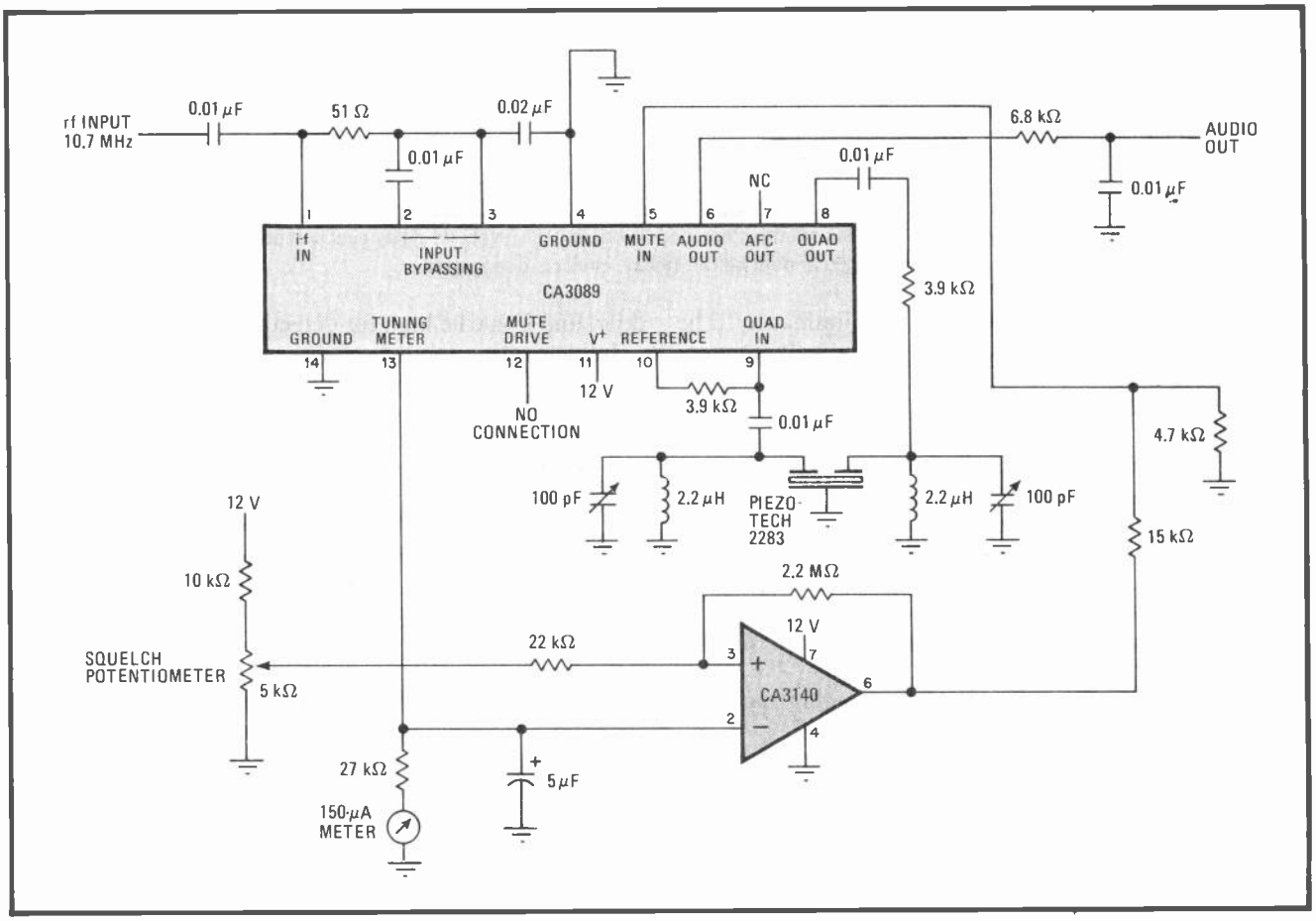
by Albert Helfrick
Aircraft Radio and Control Division, Cessna Aircraft Co., Boonton, N. J.

Although the CA3089 FM/IF system offers the advantages of one-chip simplicity, good limiting capability, high gain, and excellent linearity when used in wideband fm-broadcast receivers,[1] its audio-channel muting performance, and thus its squelch response, suffer in narrow-band applications, especially at low signal levels. Utilizing the output voltage from the device's tuning-meter port to drive the audio-muting control circuit through an operational amplifier greatly improves squelching, particularly for signals whose amplitudes are barely detectable.

The circuit configuration of a typical limiter-discriminator designed for a modulation deviation of ±5 kilohertz is shown in the figure. As in many discriminators, a crystal serves for the high-Q tuned circuit and so makes possible the high audio recovery required in a narrow-band configuration.

The internal muting action of the CA3089, though sufficient for wideband service, lacks the speed and precision necessary for narrowband operation, because the system's effectiveness is a function of the characteristics of the detector's frequency-determining elements connected to pins 8, 9, and 10, as well as the gain distribution of the entire receiver. Narrowband receivers usually make full use of the system's available sensitivity by having as much gain as possible before the detector so that limiting occurs on noise, and the small-bandwidth characteristics of the CA3089 circuit are similar. At low signal levels, this limiting causes the squelch circuit to be almost useless. In some of the recommended circuits for frequency discriminators, the squelch circuit will not operate at all.

Driving the mute-control amplifier from the tuning-meter port (pin 13) instead ensures that the tuned circuit and the chip's gain distribution have no effect on squelch



Silence. Circuit derives voltage for squelch-control amplifier from CA3089's tuning-meter port, whose output is linear over 5 to 10,000 μV. Op amp provides gain for surefire operation. Configuration provides positive squelch response, even at low signal levels, by bypassing the combined nonlinear response of tuned circuit and mute-drive circuit internal to the CA3089.

operation. The meter-output voltage, taken from the unit's three intermediate-frequency amplifiers and their level detectors, has a constant characteristic—that is, it is independent of the tuned circuit used. In fact, the response is virtually linear for input signals ranging from 5 to 10,000 microvolts.

The high input impedance of the low-noise CA3140 op-amp comparator will not load down pin 13, and its gain enables the squelch circuit to operate in a surefire manner. The CA3140 is used as a comparator with a variable threshold set by the squelch potentiometer, as shown. A voltage divider at its output ensures that no more than about 5 volts can be applied to port 5—anything higher would cause latchup in the CA3089, which might cause excessive power dissipation.

The CA3140 can operate with a common-mode voltage equal to that of the negative supply, and it may therefore be operated from the same power source as the CA3089. □

References

1. J. Brian Dance, "One-chip for demodulator has improved response," *Electronics*, Dec. 22, 1977, p. 78.

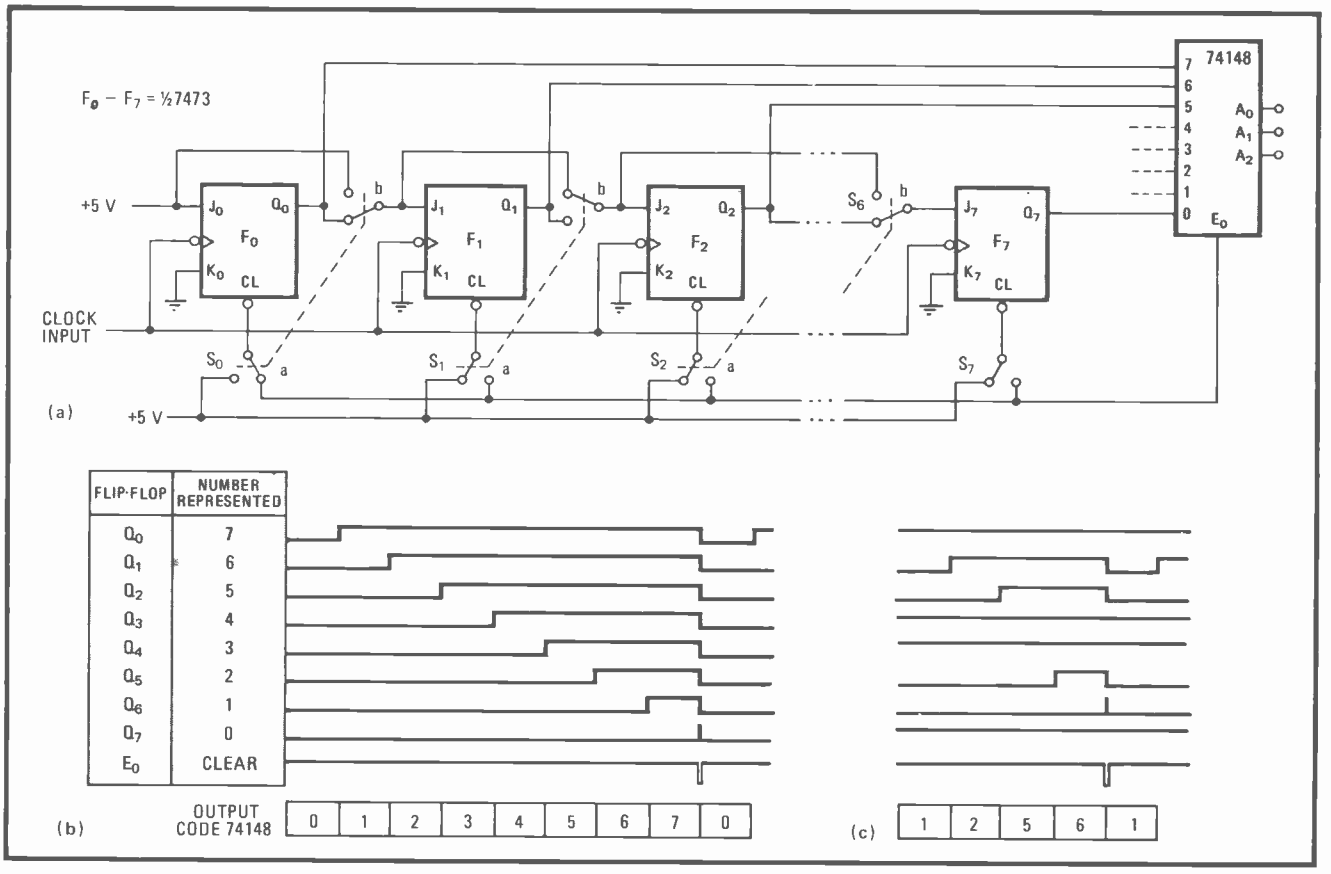
Cascaded flip-flops set periodic-sequence generator

by Carlos Correia and Cidálio Cruz
University of Coimbra, Portugal

This circuit, which generates a periodic sequence of nonconsecutive binary numbers, will serve well as an address generator in multiplexed data-communications systems. Using several J-K flip-flops whose outputs drive a priority encoder, the circuit produces a selectable, monotonically increasing output code having zero dead time (no lag) between numbers. Implementing this circuit is far simpler than modifying a standard binary-counter circuit, which is more useful in applications where the numbers to be generated are consecutive.

As shown in (a), a double-pole, double-throw switch is required for all but the last flip-flop desired, which requires a single-pole, double-throw switch. In this case, eight flip-flops are used — thus the numbers 0 through 7 can be generated.

When each flip-flop is active (Q disconnected from the J port of its succeeding 7473 flip-flop and its clear port connected to E_0 of the 74148), the sequence generator will advance in order from 0 through 7, as shown in (b). At the end of the sequence, when all inputs to the 74148 are high, E_0 moves high, clearing all flip-flops and



Chosen order. Periodic-sequence generator (a) produces selectable, monotonically increasing binary output code (b) having zero dead time. Any number can be omitted from the sequence (c) by using double-pole, double-throw switches to disconnect Q output of the flip-flop corresponding to that number from succeeding flip-flop and bringing its clear port to 5 V.

initializing the sequence at its first number.

Note that any number can be omitted from the sequence by connecting the Q output of the flip-flop that corresponds to that number to the J port of the next flip-flop and then connecting its clear port to 5 volts. For instance, the sequence 1, 2, 5, 6, seen in (c), is generated by disabling flip-flops 3, 4, and 7.

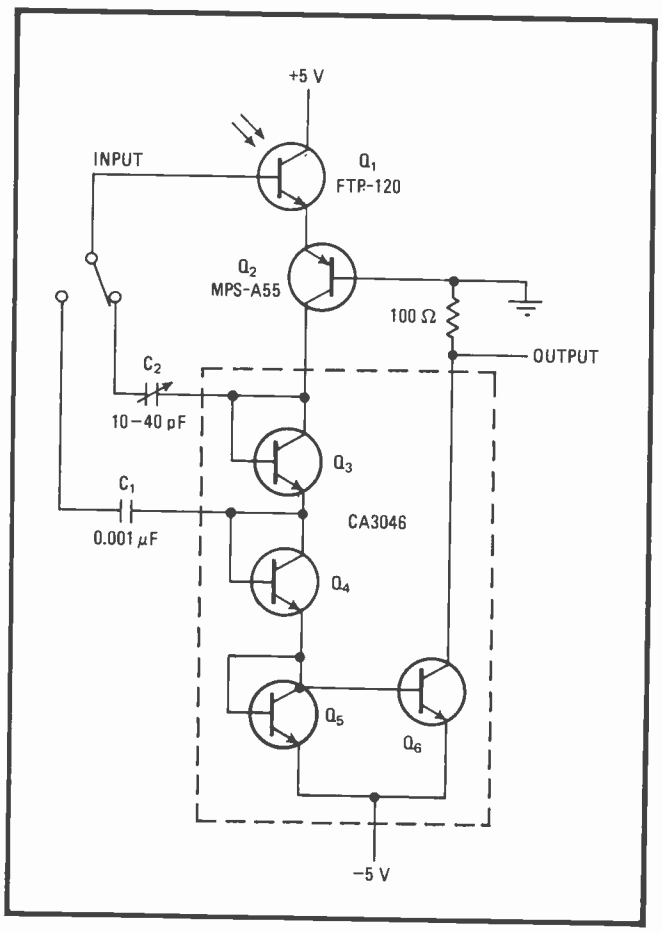
A sequence having a maximum word length of 10 can be generated if a 74147 is used in place of the 74148. However, the E_0 signal is not available in the former device, and therefore to derive that signal each input of a 10-lead NAND gate must be connected to all flip-flops, with its output connected to the switches.

The maximum clock rate is determined by the propagation delay times encountered by the signal that clears the flip-flops. For the circuit shown, the delay time is about 95 nanoseconds, which yields a maximum clock rate of 1 megahertz. If Schottky flip-flops are used, the delay is 44 ns, corresponding to a clock rate of approximately 2.2 MHz. □

Bootstrapping a phototransistor improves its pulse response

by Peter J. Kindlmann
Engineering and Applied Science Dept. Yale University, New Haven, Conn.

Although the operating speed of a phototransistor cannot be improved simply by connecting a second one in the cascode configuration [*Electronics*, March 2, p. 132, and April 27, p. 154], its response may be improved by employing a standard transistor in a bootstrap circuit in order to reduce the effective value of the phototransistor's junction capacitance. By introducing bootstrap feedback to the base of the input optodevice, the switching speed of a cascode-connected phototransistor can be increased by as much as 10 times over that of a uncompensated one.



Compensation. Junction capacitance of Q_1, which is not sufficiently reduced despite cascode connection (Q_1, Q_2), is greatly lowered by applying feedback to base. This allows a rapid discharge of Q_1's base-to-emitter capacitance during signal conditions, which acts to increase the phototransistor's high-frequency response.

Phototransistor Q_1 and Q_2, a pnp transistor, form the conventional cascode arrangement, as shown in the figure. Generally, when an input signal is detected, the photocurrent step produced begins to charge the capacitance associated with Q_2's base-emitter and base-collector junctions. The voltage across the base-emitter junction has a magnitude comparable to that across Q_2's base-emitter junction, and therefore a way must be found to compensate for the two V_{be} drops produced, in order to ultimately reduce the effective junction capacitance of the phototransistor.

In theory, the V_{be} drops may be cancelled by making use of the pn drops across two forward-biased diodes of comparable transconductance. Here, diode-connected transistors Q_3–Q_5, which are part of the CA3046 transistor array, are available for use. Using the CA3046 ensures that these transistors will be closely matched.

Feedback from Q_4's collector to Q_1's base through C_1 constitutes the normal bootstrap path, supplying an in-phase current to Q_1's base. This causes a rapid charge of the junction capacitance, and therefore the input photocurrent sees a lower value of capacitance than actually exists. Because Q_1 has a β of several hundred, its base-emitter transconductance is less than that of the lower-β devices, Q_4 and Q_5, used in the feedback path. As a result, the amount of feedback is well below unity loop gain (undercompensated condition).

By using Q_3, however, with feedback applied through C_2, an additional pn drop is gained and compensation becomes almost perfect. For a given quiescent photocurrent, C_2 should be adjusted to a value just above that which will cause oscillation in the circuit.

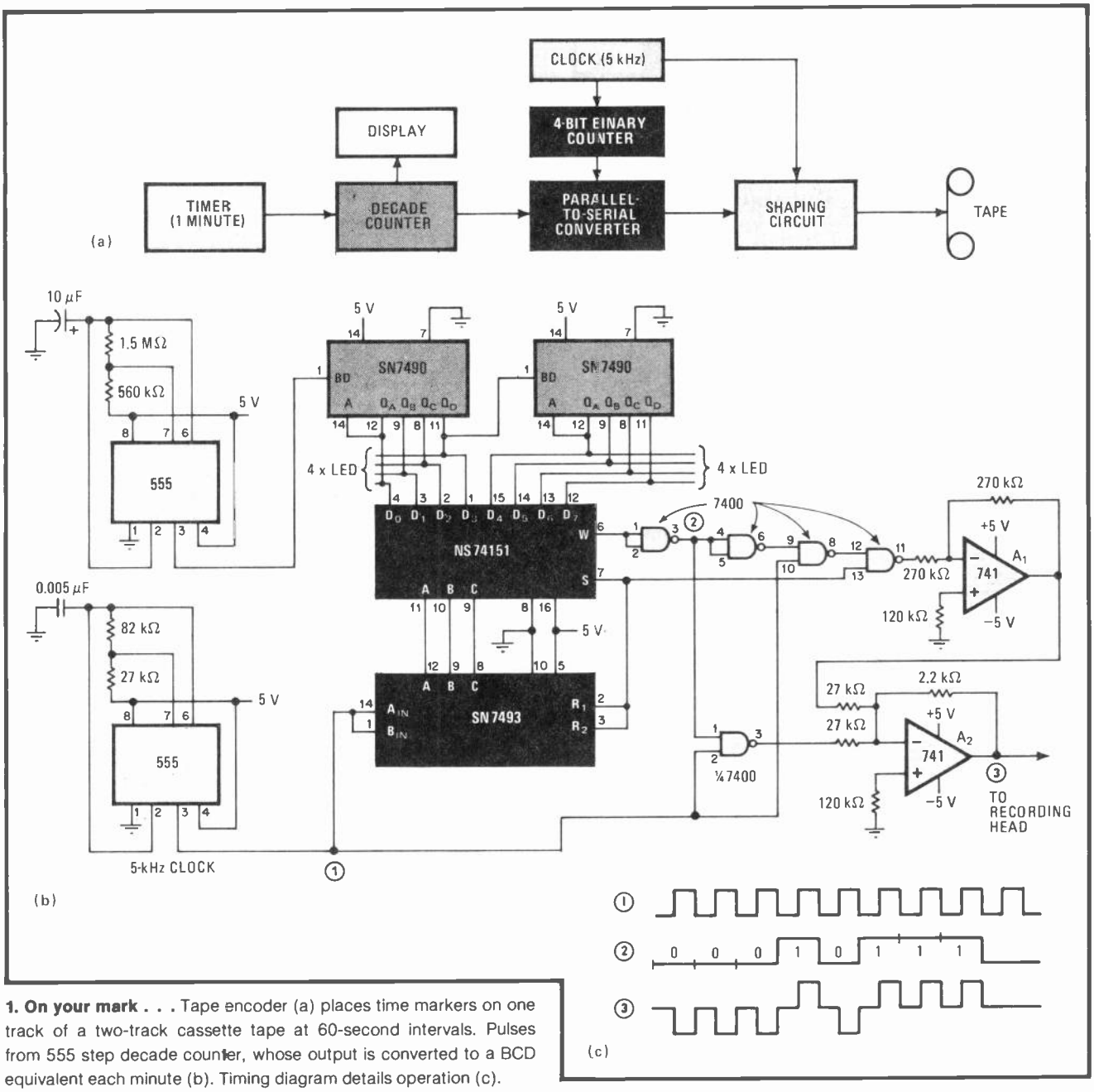
Fairchild's FTP-120 (Q_1) has a typical rise time and fall time of 18 microseconds when used in the typical emitter-follower configuration specified for a 100-ohm load. With C_1-path compensation, the switching time is about 5 μs. With C_2-path compensation, the switching time is about 2 to 3 μs. □

Time-encoding system formats cassette tapes

by Fathi Saleh and Benham Bavarian
Abadan Institute of Technology, Abadan, Iran

Using operational amplifiers and standard digital elements to place 1-minute markers on a stereo cassette tape, this formatter is extremely useful when implemented in simple data-recording and control systems. Also shown here is a rudimentary decoder circuit, and the information required to utilize the markers for controlling any cassette's stop, play, fast forward or rewind functions for more advanced systems.

Figure 1a gives the block diagram of the tape formatter, which was used with the JVC MC-1820R recorder. The timing signals are recorded at the expense of one track of the tape, leaving the other track for monaural sound or data recording. It might have been possible to add a thin head to the recorder in order to record marker signals and at the same time make possible two-channel



1. On your mark . . . Tape encoder (a) places time markers on one track of a two-track cassette tape at 60-second intervals. Pulses from 555 step decade counter, whose output is converted to a BCD equivalent each minute (b). Timing diagram details operation (c).

data recording, but this was not tried.

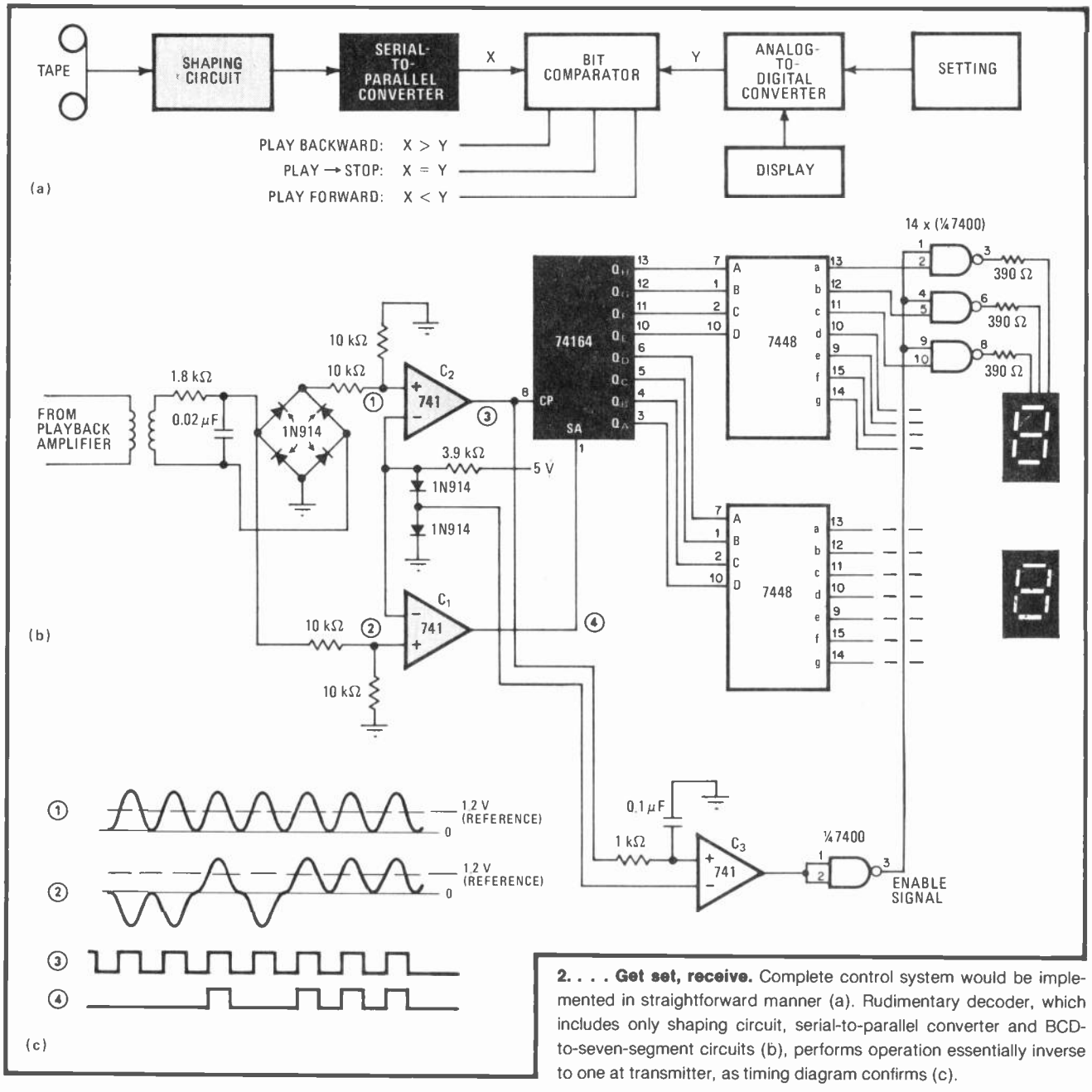
As shown in Fig. 1b, the recording system uses a 555 timer to generate a pulse every 60 seconds, two 7490 decade counters that are stepped by the timer to yield required 8-bit patterns, eight light-emitting diodes to monitor the number generated, a parallel-to-serial converter (74151) that is clocked at 5 kilohertz by a second timer, a 4-bit counter (7493), and shaping circuitry.

Pulses emanating from the 1-minute timer advance the 7490s. The output of these devices is introduced to the 74151, which is being clocked at a 5-kHz rate through the 7493. The output of the 74151, after passing through a NAND gate, appears as shown in the timing diagram (Fig. 1c).

Recombining the 5-kHz clock with other summing-circuit (A_1) signals yields an output at A_2 having a 50% duty cycle. This output returns to a logic 0 when the output from the 74151 is a logic 1 and moves high for a logic 0 output from the 74151. The signal is a two-digit binary-coded-decimal character which advances from 0 to 60 minutes. The return-to-zero format is used here so that one may differentiate between the zero-state and the no-signal levels. This format also simplifies the design of the decoding circuits.

The playback (decoder) circuit is shown in Fig. 2. The block diagram (Fig. 2a) shows a complete control system, but the system, although straightforward, encompass more circuitry than can be shown here.

The basic decoder is shown in Fig. 2b. Passing through the shaping circuit is the output from the tape recorder. This input signal is compared with a 1.2-volt reference at C_1, enabling the original bit pattern recorded to be recovered at its output. Meanwhile, the original clock



2. . . . Get set, receive. Complete control system would be implemented in straightforward manner (a). Rudimentary decoder, which includes only shaping circuit, serial-to-parallel converter and BCD-to-seven-segment circuits (b), performs operation essentially inverse to one at transmitter, as timing diagram confirms (c).

pulses are regenerated at C_2 by comparing the rectified 1s and 0s of the bipolar return-to-zero input signal with the 1.2-v reference. The bit pattern output from C_1 is connected to the 74164 serial-to-parallel converter, which is stepped by the output of C_2.

Thus the output of the 74164 is a binary-coded-decimal equivalent of the marker-input's value. The seven-segment displays that follow indicate the time, in minutes, corresponding to the last marker detected. □

Digital logic multiplies pulse widths

by N. Bhaskara Rao
U.V.C.E., Department of Electrical Engineering, Bangalore, India

Using logic elements to multiply the width of incoming pulses by a value selected by the user, this circuit is simple to build and provides a higher accuracy-to-cost ratio than its analog counterpart. It should therefore find numerous uses in synchronous systems, and although its prime function is to provide a multiplication factor of greater than unity, it can generate smaller values as well.

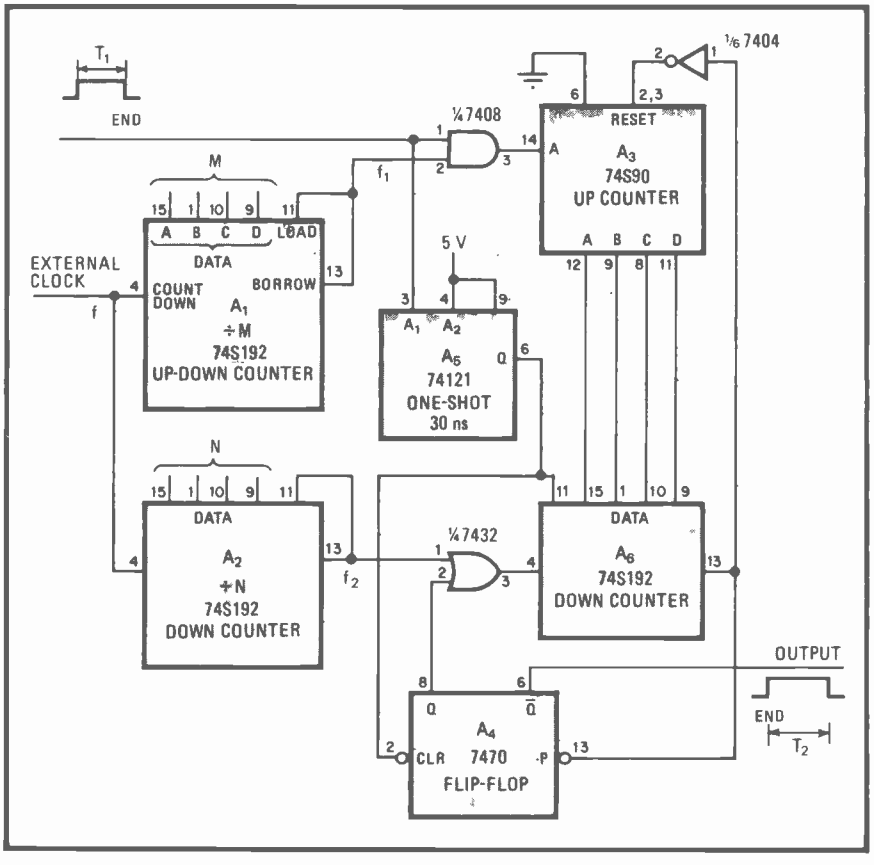
The figure will help make circuit operation clear. The multiplication factor is selected by presetting two 74S192 down counters, A_1 and A_2. Initially, counter A_1 is set to a value, M; A_2 is preset to a second value, N; A_3 is zero; and the Q output of flip-flop A_4 is high.

An incoming pulse of width T_1 (the signal to be multiplied) switches on the 7408 AND gate and enables A_3 to count to a number determined by f_1, which is derived from an external clock having input frequency f. Thus, at the end of the pulse, the counter contains the number f_1T_1. Note that $f_1 = f/M$.

When the trailing edge of the pulse arrives, A_5 is triggered and presets A_6 with the number contained in A_3. Meanwhile, A_4 is cleared (Q=0) by A_5, and the OR gate is thereby activated so that counter A_6 can initiate counting from its preset value. Note that A_6 is driven by A_2, the divide-by-N down counter, and that $f_2 = f/N$.

The time taken for A_6 to reach zero from its preset value is thus $T_2 = (f_1/f_2)T_1 = (N/M)T_1$. At this time, the output from A_6's borrow port clears A_3 and presets the flip-flop. Therefore the time between the flip-flop's move to logic 0 (at the trailing edge of the input pulse) and the time its Q output moves high again is T_2.

The output signal is not derived until the input pulse's trailing edge arrives. The multiplication factor, N/M, can thus be set to any value greater or less than unity because the conversion is carried out after a delay. Needless to say, f should be much greater than T_1 for accurate pulse-width multiplication. □



Width multiplier. Circuit has no analog elements. Multiplication factor is determined by ratio of N to M, set by user. A_6 is preset to f_1T_1; stepped to zero at f_2 rate, it signals flip-flop. Time between state changes of flip-flop is $T_2 = (N/M)T_1$.

Negative-output regulator tracks input voltage

by Gil Marosi
Intech Function Modules Inc., Santa Clara, Calif.

By using an astable multivibrator in a flyback arrangement to develop negative voltages from positive ones, this regulator ensures that its output tracks the input, such that $V_O = -V_{in}$. The voltage-controlled circuit requires only three active devices, all of them transistors.

Q_1 and Q_2 form the free-running oscillator, as shown in the figure. With Q_2 on, the V_{in} voltage is impressed across resistor L, causing the current through L to increase linearly. The peak value of current reached before Q_2 turns off will be directly proportional to the magnitude of the output voltage developed across capacitor C_4.

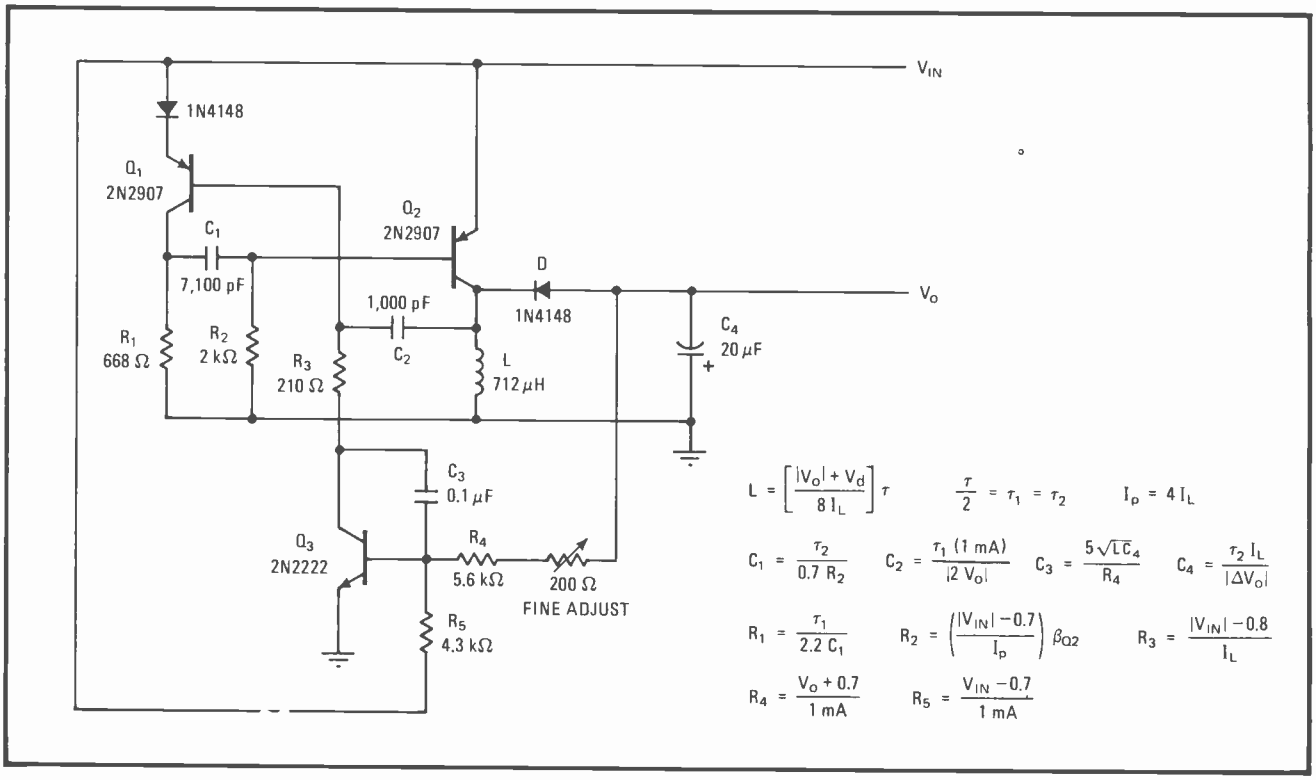
During the time the current through the inductor increases, no voltage can be developed across C_4 because diode D is back-biased. When Q_2 switches off, however, the collector voltage drops from V_{in}, and the capacitor charges to a negative voltage. This occurs because the charging current through the coil makes D turn on, thereby causing a negative voltage at the output.

The field across L then begins to collapse and D is biased on, placing the output voltage ($V_o + V_d$) across L, where V_d is the diode drop. The current through L must then fall linearly to zero. This completes one cycle of the flyback operation.

The input voltage is next compared with the output voltage at the summing node, at the base of Q_3. This transistor amplifies the voltage difference and transforms it into a current that is used to control Q_2's turn-on time. Thus if V_{out} should fall, the control current will act to increase the on time of Q_2, thereby increasing the peak current through L and so raising the output voltage. This analysis assumes that V_{in} emanates from a stiff source—that is, an increased current demand will not cause a drop in V_{in} because of an increased voltage drop across the source's internal impedance.

Without Q_3, the load regulation would be directly proportional to a change in load current (I_L) and so a 10% change in I_L would cause a 10% change in load voltage V_L. Q_3 ensures that such a change in I_L causes only a 0.2% change.

Component values are given for a circuit that operates with an $I_L = 20$ milliamperes, a $V_o = -5$ volts, and an astable multivibrator operating at 50 kilohertz ($\tau = 20$ microseconds). Equations are given in order to facilitate the design of regulators for specific parameters. □



Flyback follower. Regulator uses astable multivibrator Q_1–Q_2 and inductor to generate negative output voltages from positive inputs while also ensuring that $V_{out} = -V_{in}$. Differential amplifier Q_3 serves to develop feedback control voltage to readjust on time of Q_2 and thus voltage developed across L and C_4 when $V_{out} \neq -V_{in}$. Component values are given for $I_L = 20$ mA, $V_o = -5$ V, and f = 50 kHz.

Controller selects mode for multiphase stepping motor

by Oldrich Podzimek
Electrical Engineering Research Institute, Prague, Czechoslovakia

Offering a selection of the most common stepping modes, these circuits are an inexpensive solution to the problem of torque control in four- and five-phase motors. The mode can be changed simply by the flip of a switch.

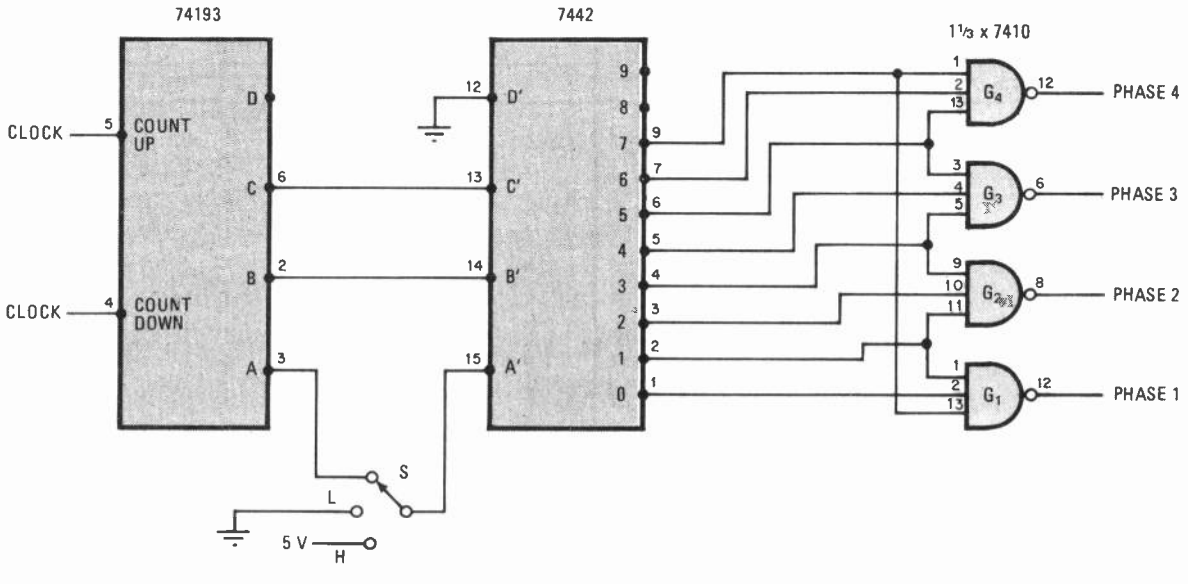
The basic circuit is the same for either stepping motor. It consists of a 4-bit binary-coded-decimal counter, a BCD-to-decimal converter, and several gates that serve as phase detectors.

The four-phase controller is shown below. The 74193 counter advances with each input-clock pulse at a frequency determined by individual requirements. Note that the 74193 can count up or down and so may be used to step the motor in the opposite direction if desired.

As the counter increments or decrements, the output of the 7442 4-to-10-line decoder switches in a manner dependent on switch S. If S connects port A′ of the 7442 to the A port of the 74193, the decoder's output will move from 0 to 7 in sequence. Otherwise, the output will switch to even values every other count (S connected to logic 0) or switch to odd values (S connected to logic 1).

A combinational logic circuit using gates G_1–G_4 converts the 7442's output to phase information in order to drive the motor. As can be seen in the truth table, either one or two windings of the motor will be active at any given time.

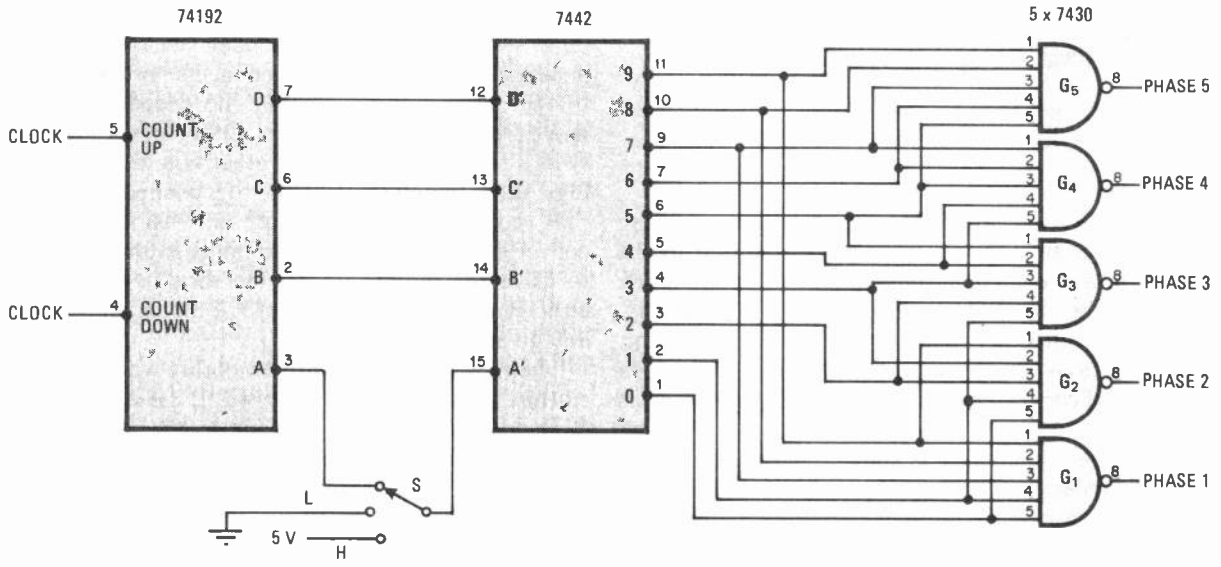
The motor will step most smoothly when S is connected to A. When S is connected to L, the step angle will be doubled, and only one of four motor windings will be excited at any given instant, thereby improving the efficiency of the step operation for a given torque. Note that when S is in the H position, the step angle will be the



COUNTER OUTPUT				A					L					H				
				PHASE				Z	PHASE				Z	PHASE				Z
A	B	C	D	1	2	3	4		1	2	3	4		1	2	3	4	
0	0	0	0 OR 1	1	0	0	0	0	1	0	0	0	0	1	1	0	0	1
1	0	0	0 OR 1	1	1	0	0	1	1	0	0	0	0	1	1	0	0	1
0	1	0	0 OR 1	0	1	0	0	2	0	1	0	0	2	0	1	1	0	3
1	1	0	0 OR 1	0	1	1	0	3	0	1	0	0	2	0	1	1	0	3
0	0	1	0 OR 1	0	0	1	0	4	0	0	1	0	4	0	0	1	1	5
1	0	1	0 OR 1	0	0	1	1	5	0	0	1	0	4	0	0	1	1	5
0	1	1	0 OR 1	0	0	0	1	6	0	0	0	1	6	1	0	0	1	7
1	1	1	0 OR 1	1	0	0	1	7	0	0	0	1	6	1	0	0	1	7

Z = SWITCHED OUTPUT OF 7442 (DECIMAL EQUIVALENT)

1. Multimode. Step controller uses up-down counter, decoder, and logic to control excitation of four-phase motor windings. Switch S selects one of three possible operating modes, ranging from smooth-stepping to high-torque.



COUNTER OUTPUT				A						L						H					
				PHASE					Z	PHASE					Z	PHASE					Z
A	B	C	D	1	2	3	4	5		1	2	3	4	5		1	2	3	4	5	
0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	1	0	0	1
1	0	0	0	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	2	0	1	1	0	0	2	0	1	1	1	0	3
1	1	0	0	0	1	1	1	0	3	0	1	1	0	0	2	0	1	1	1	0	3
0	0	1	0	0	0	1	1	0	4	0	0	1	1	0	4	0	0	1	1	1	5
1	0	1	0	0	0	1	1	1	5	0	0	1	1	0	4	0	0	1	1	1	5
0	1	1	0	0	0	0	1	1	6	0	0	0	1	1	6	1	0	0	1	1	7
1	1	1	0	1	0	0	1	1	7	0	0	0	1	1	6	1	0	0	1	1	7
0	0	0	1	1	0	0	0	1	8	1	0	0	0	1	8	1	1	0	0	1	9
1	0	0	1	1	1	0	0	1	9	1	0	0	0	1	8	1	1	0	0	1	9

Z = SWITCHED OUTPUT OF 7442 (DECIMAL EQUIVALENT)

2. Multiphase. Controller for stepping five-phase motors is similar to that for four-phase case. Five 5-input NAND gates and some additional wiring are the only new changes required for enabling up to three phases of a motor to be excited simultaneously.

same as in the preceding case, but two motor windings will be active at any time, power input will be doubled, and 41% greater torque will be obtained.

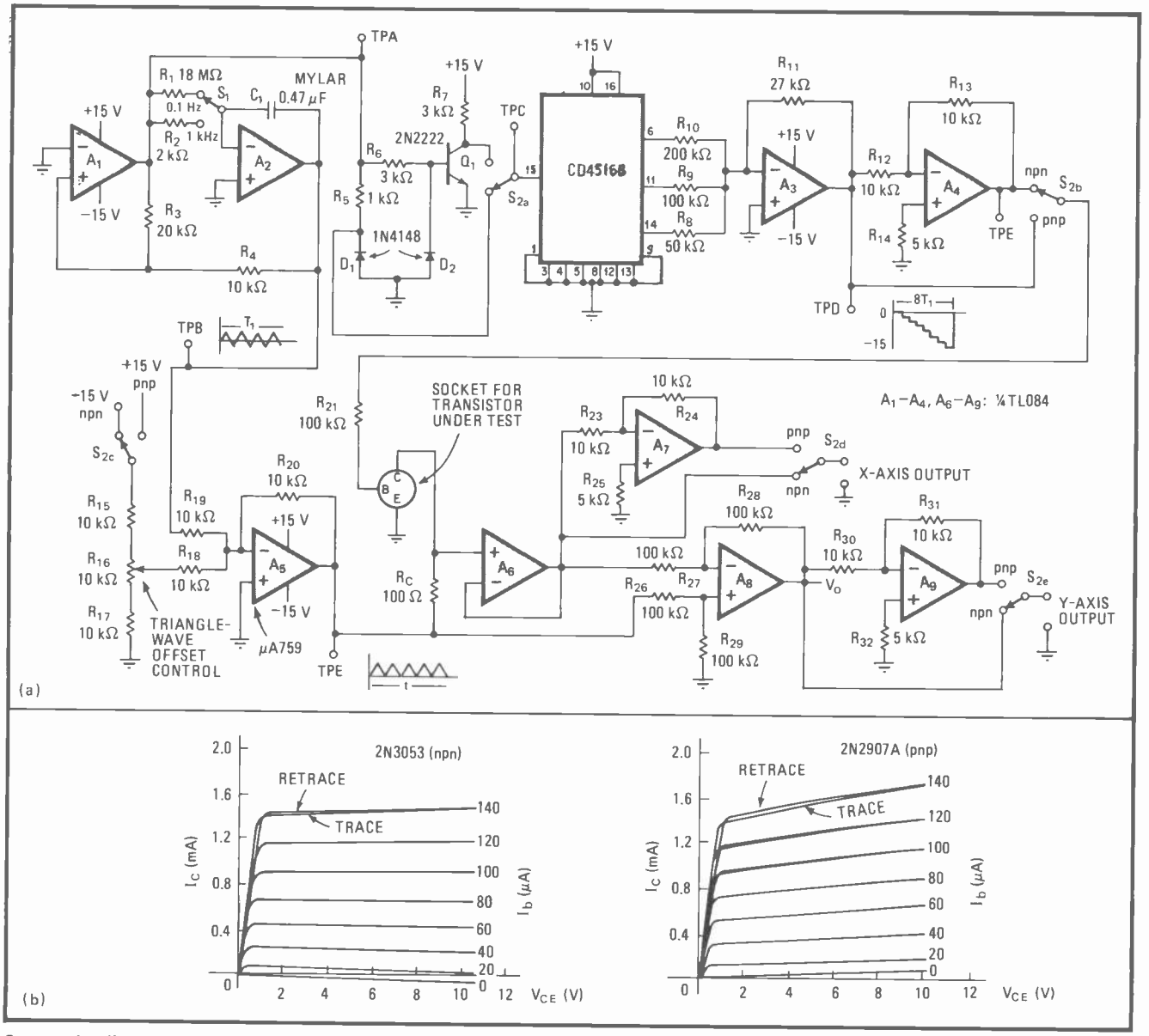
A similar circuit suitable for stepping five-phase motors is shown above. In this case, either two or three phases of the motor are excited simultaneously. This circuit can be extended to solve a general m-phase motor problem. □

Op amps and counter form low-cost transistor curve tracer

by Forrest P. Clay Jr., Clarence E. Rash, and James M. Walden
Old Dominion University, Department of Physics, Norfolk, Va.

For a curve tracer, this relatively simple circuit is unusually inexpensive. Used to test small-signal bipolar transistors as well as junction diodes, it generates the waveforms needed to display or plot their characteristic curves on an oscilloscope or X-Y plotter, interfacing directly with either. Operational amplifiers, one transistor, and a single binary counter are the only active devices needed.

Central to the circuit is a current generator made up of an op amp driven by the counter. It supplies eight levels of base current in sequence to the transistor under test. Op amps A_1 and A_2, with the aid of the R_1-R_2-C_1 timing network, initially produce both square and triangular waves at test points A and B (TPA and TPB), respectively. S_1 selects the waveform frequency—either



Current family. Tracer produces set of eight curves of collector current vs collector voltage from npn or pnp transistor under test. Diodes may also be checked in circuit's pnp-transistor mode (a). Representative curves are plotted using X-Y recorder (b). Note temperature effects seen on the retrace portion of curves for higher values of I_b and I_c.

1 kilohertz for output onto an oscilloscope or 0.1 hertz for plotting with an X-Y recorder.

The waveform at TPA is then shaped by D_1–R_5 or D_2–R_6 into a clock pulse suitable for the 4516 binary counter. The signals emanating from the Q_a, Q_b, and Q_c ports of the counter, when fed into a binary-weighted summation network (R_8–R_{11}), produce an eight-step staircase waveform at the output of A_3 or A_4, depending upon whether a pnp or npn transistor is under test. The actual base current value is determined by appropriate selection of R_{21}. The collector current can be calculated from $I_c = V_o/R_c$.

Both the collector-biasing voltage for the transistor under test and the linear-deflecting voltage for the X-axis output to the scope are derived from the triangle wave. The first voltage is obtained by using S_{2c} and R_{16}, which permit the proper dc component to be added to the triangle signal.

Note that the Y axis is stepped at one eighth of the rate at which the X axis is scanned. Thus, if the sampling rate is 1 kHz, each of the eight current levels is swept at a rate 125 Hz, well above the rate at which flicker is detectable on a scope.

The circuit is easy to use. Simply place ganged switch S_2 into whichever position is correct for the type of transistor being measured (npn or pnp); place the transistor into the test socket; and apply circuit power. To test a diode, insert its anode and cathode leads into the emitter and collector sockets, respectively, and put S_2 in the pnp mode.

Figure 1b shows two representative families of curves the circuit produced on an X-Y recorder for the two types of bipolar transistor. □

Envelope generator sets music-box timbre

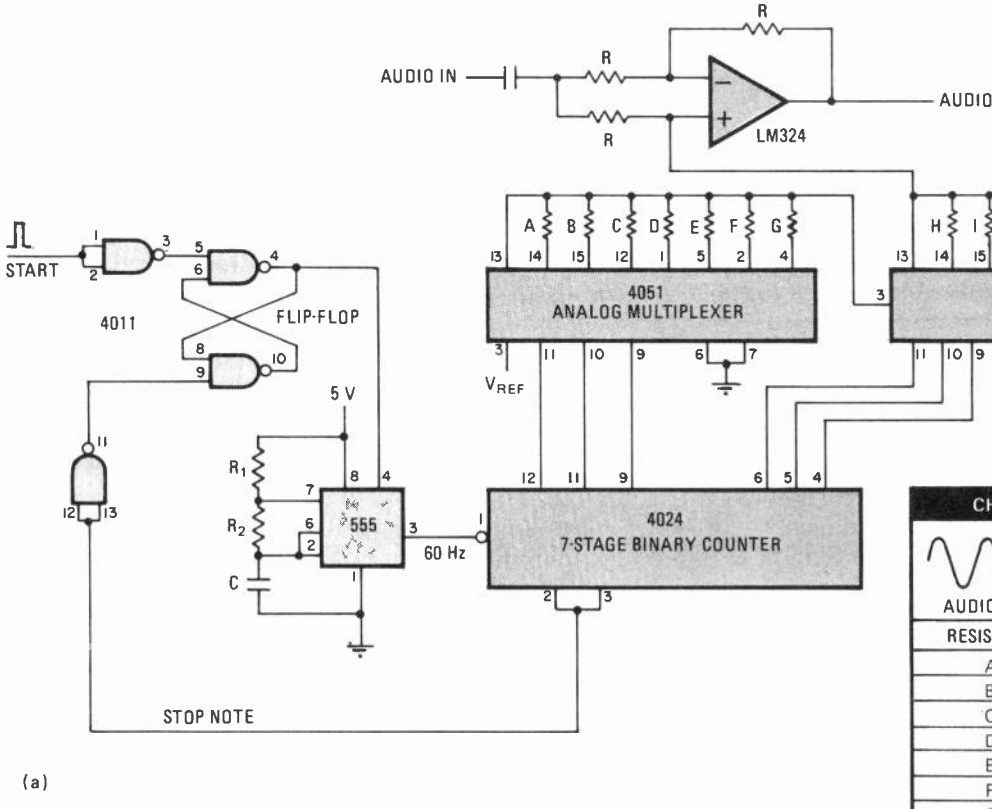
by Ken Dugan
General Telephone & Electronics Corp., Clearwater, Fla.

An electronic door bell sounds unlike an electronic music box or telephone ringer because its notes have different attack, sustain, and decay times—in other words, a different envelope. By using just a binary counter and a programmable weighted-resistor network, this simple circuit generates the envelope required to transform a continuous tone into a chime or a signal of almost any other timbre. The circuit can be readily expanded to generate a wave of any complexity.

As shown in (a), the unit is basically an operational amplifier that operates as a subtracter, with the weighted-resistor network connected to its noninverting port (the switched leg). To generate an envelope, a start pulse sets the flip-flop and fires the 555 timer, which is wired as an astable multivibrator. The timer, which in this case is running at 60 hertz, steps the 4024 counter.

The binary-counter outputs address the 4051 analog multiplexers, and resistors A–N are connected one by one between the noninverting port of the LM324 op amp and ground. Thus the multiplexers control the output envelope, modulating the sine wave so that when the resistance switched into the noninverting port is zero, there is maximum output, but when the resistance is equal to R, there is no audio output. At the end of the sequence, the flip-flop is reset.

Tabulated in (b) are the resistor values needed to generate a chime, or bell sound. The envelope required for a perfect chime is logarithmic (fast attack, no sustain, long delay), but the envelope is approximated by a simple sloping line as shown; otherwise many resistors and multiplexers would be needed. □



CHIME GENERATION	
AUDIO IN	AUDIO OUT
RESISTOR	% R
A	1.5
B	3
C	4.5
D	6
E	7.5
F	9
G	10.5
H	12.5
I	25
J	37.5
K	50
L	62.5
M	75
N	87.5

(b)

Sound control. Weighted resistor network, multiplexers, and counter can derive almost any sound from sine-wave input by controlling shape of envelope (a). Multiplexers, stepped by counter and 555 (whose frequency is determined by R_1-R_2-C), introduce resistors A–N to noninverting port of op amp in sequence. Repetition rate is controlled by occurrence of start pulses. The table (b) lists resistor values required for generation of chimes, or bell sounds.

VCOs generate selectable pseudo-random noise

by James D. Long
Aerojet ElectroSystems Co., Azusa, Calif.

In this circuit, several voltage-controlled oscillators, whose outputs are summed in order to generate a suitable feedback voltage to their inputs, are used to generate pseudo-random noise over band limits that can be selected by the user. Using VCOs makes possible a transfer function that is closer to the ideal and ensures that the circuit has better amplitude-versus-temperature stability than conventional generators, which rely on special and often expensive diodes to produce noise over a wide band. This generator will be suitable for many applications, producing random noise over a bandwidth of three octaves, with a crest factor (ratio of peak to true root-mean-square voltage) of three.

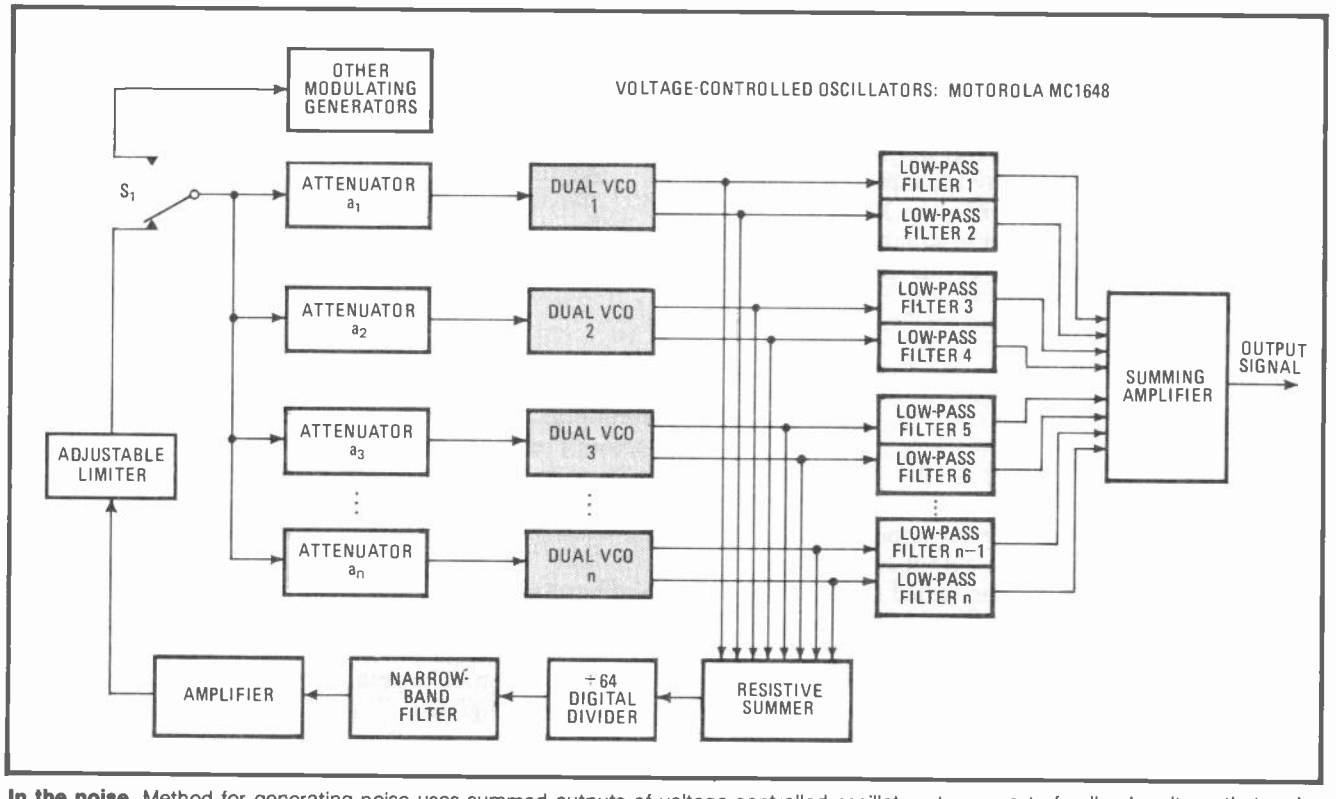
The key to circuit operation is to generate a random feedback voltage to the bank of VCOs so that their output frequencies vary randomly, thus in effect producing noise. This task can be accomplished with the circuit shown in the block diagram. Note that the frequency of the feedback (modulating) voltage is unimportant so long as the maximum modulating frequency is less than any oscillator's output frequency.

A single VCO usually retains its linear input-voltage-to-output frequency characteristic over less than one octave. The three-octave bandwidth can be realized by operating several VCOs over adjacent frequency bands (staggered tuning). Low-pass filters remove the higher-order harmonics contained in the square-wave outputs of the oscillators and the signal appearing at the output of the summing amplifier is similar to random noise.

The feedback signal required to generate the random noise is derived by first combining the output of all VCOs in a resistive summing network. The output from the summer is a signal that contains zero crossings occurring at random intervals.

A divide-by-64 circuit detects threshold crossings and brings the summer signal down to a frequency range consistent with the requirement that the highest modulation frequency be much less than the total output frequency of the VCOs. A narrowband (Q=5) LC filter then smooths these random amplitudes into a continuous signal for the VCOs' inputs. With proper scaling factors provided by the amplifier, the desired range of random frequencies can be generated.

Each VCO is biased to its appropriate geometric-mean frequency and operates there if the modulation amplitude is zero. Attenuators a_1 through a_n allow independent control of the deviation range of each VCO, and the adjustable limiter permits control of the peak deviation frequency. The function of the adjustable limiter is to ensure that the oscillators do not deviate beyond their prescribed frequency bands. If the VCOs' band edges are aligned so that no overlaps nor gaps occur between adjacent bands, the distribution of frequencies at the output of the summing amplifier will be uniform. Alignment of the band edges is not difficult.



In the noise. Method for generating noise uses summed outputs of voltage-controlled oscillators to generate feedback voltage that varies randomly with time, thereby causing frequencies of oscillators to vary in the same manner. System provides uniform noise output over three octaves, with a noise-voltage crest factor of three. Generator can produce other waveforms if appropriate modulating signals are applied.

This generator can produce signals other than noise. Switch S_1 may be used to apply any modulating signal to the VCOs' inputs. For example, a sawtooth input signal will generate a swept-tone output. If the VCO has an inhibit input, it can be selectively activated so that pulsed tones can be generated. □

Multiplier, op amp generate sine for producing vectors

by Jerald Graeme
Burr-Brown, Tucson, Ariz.

To compute trigonometric functions of the kind that produce a vector from its X and Y components, a system needs to be supplied with signals that are proportional to the sines of the applied X and Y dc-voltage inputs. A multiplier, operating as a signal squarer, and an operational amplifier, serving as a subtracter, will process the X or Y component more simply than other circuits now generally used. With these components, the desired waveform response for either input—the positive half of a sine function—can be approximated to within 5% of a perfect waveform, a value well within the limits that yield good computational accuracy.

Using the multiplier and the op amp to generate the sinusoidal transfer function is much easier than using diodes in complex circuits to synthesize the nonlinear response by producing a piecewise-linear approximation. Also, this circuit produces the sine response over the required $-90°$ to $+90°$ quadrant using one less multiplier than existing analog circuits,[1] which generate the approximation by means of a long mathematical series or an equivalent method.

The circuit shown in (a) processes the dc input voltage that corresponds to either the X or Y component of the vector. The BB4213AM has a transfer function of $G = X'Y'/10$, where X' and Y' are the inputs; it is made to square the input voltage, e_i, when the X' and Y' ports are connected. The output of the squarer is then introduced into the inverting port of the BB3500 op amp, with e_i fed to its input, so that:

$$e_o = 3.86\left(e_i - \frac{e_i^2}{10}\right) \qquad (1)$$

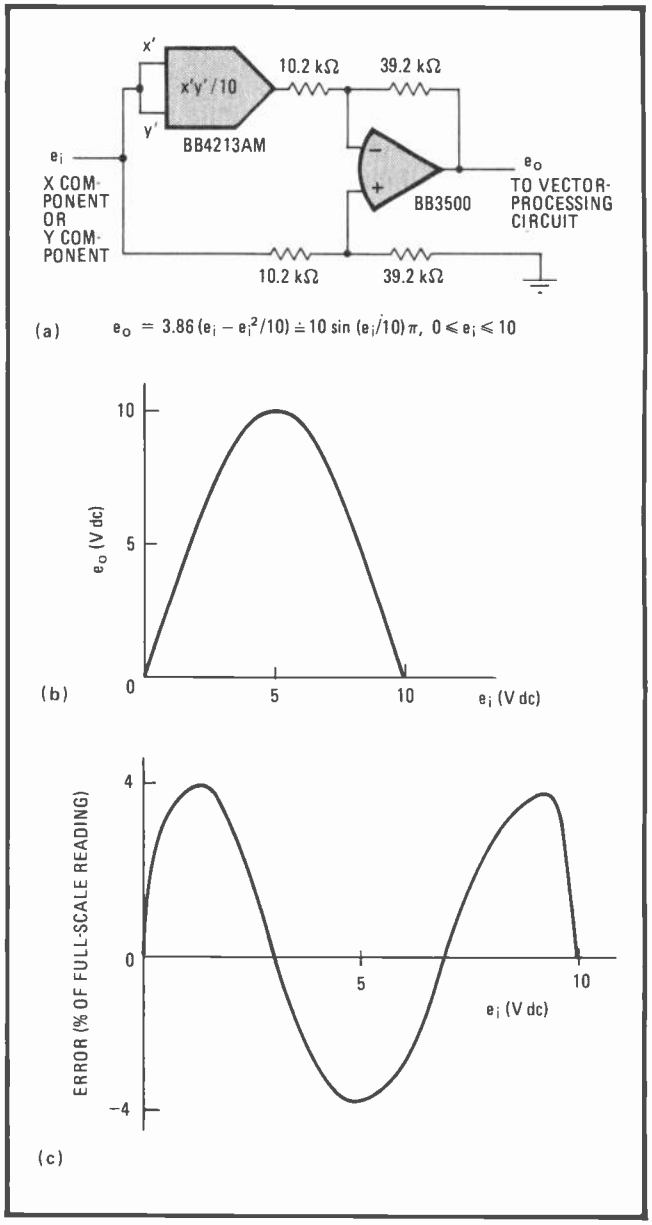
But Eq. 1 can be expressed by:

$$e_o \triangleq 10 \sin\left(\frac{e_i}{10}\pi\right), \quad 0 \leq e_i \leq 10 \qquad (2)$$

which results from a simple series approximation. This can be confirmed in the actual output-versus-input voltage plot (b). Equation 2 may be scaled for other input-voltage ranges by changing the gain of the op amp.

Note that term 2 in Eq. 1 (representing the actual output response) has a second-order exponent, whereas a Taylor-series, which would yield a closer approximation to a sine wave, would have a third-order exponent of considerable magnitude in term 2. In spite of this difference, however, Eq. 1 is reasonably accurate as evidenced by the error-curve plot (c), which peaks at 4% of full scale. Dominant distortion is related to the second and third harmonics that are present at the output.

An additional error term of up to 1% is introduced by the inherent nonlinearities in the multiplier circuit's transfer function. The error introduced by the op amp, however, is negligible. □



Coordinates. Squaring and subtraction (a) of input wave from itself produces a series approximation to a half sine wave (b). Two such circuits, given X and Y coordinates in the form of dc-voltage inputs, can generate output for systems suitable for computing vectors. Approximation error (c) for half sine is within 5%.

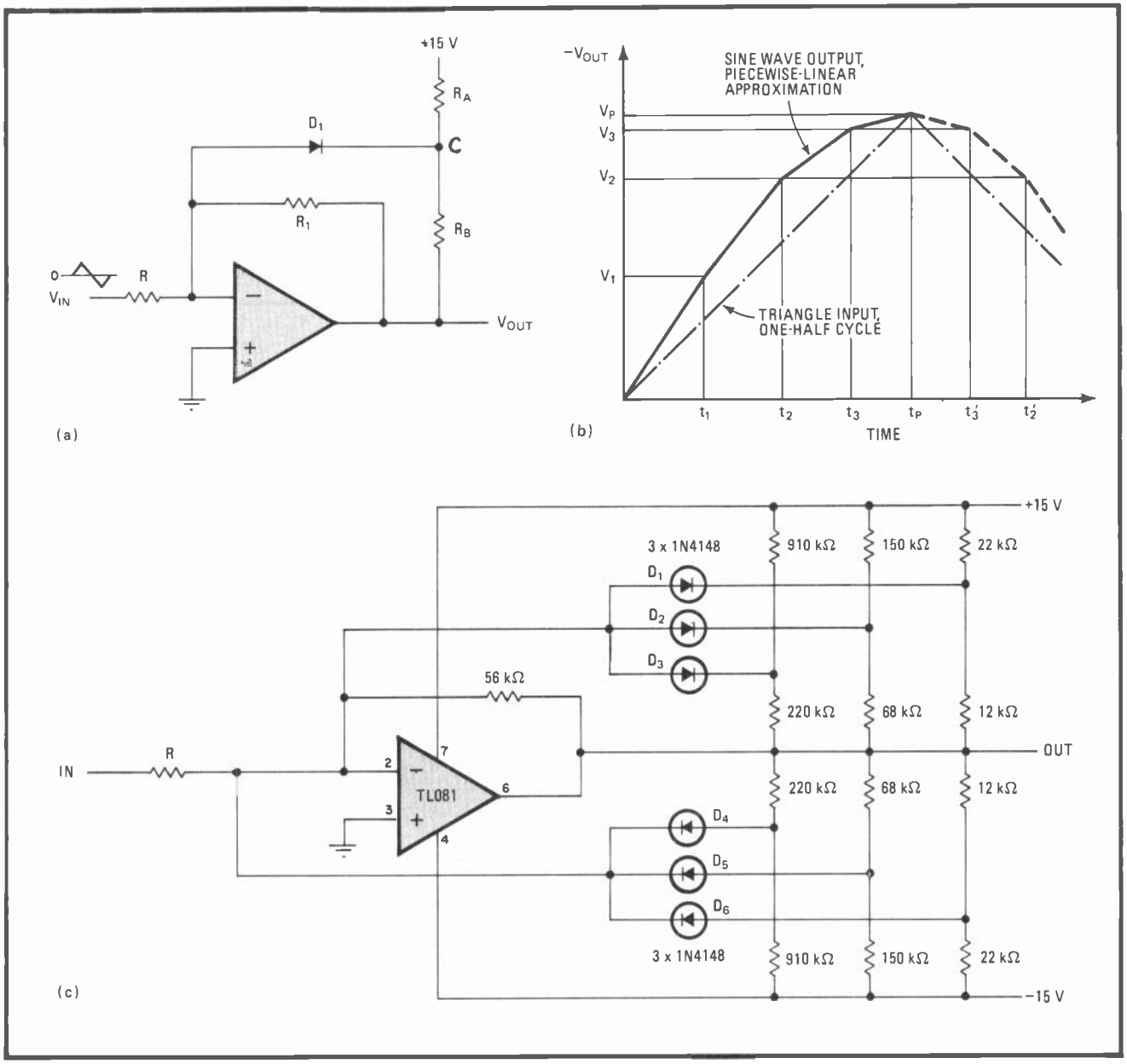
References
1. Burr-Brown, Model 4213 Product Data Sheet, PDS366, 1976.

Diode-shunted op amp converts triangular input into sine wave

by Giovanni Righini and Franca Marsiglia
Florence, Italy

Finding applications in low-frequency function generators, linear voltage-controlled oscillators, and, in general, wherever it is necessary to have an output with a constant amplitude that is independent of frequency, this converter transforms a bipolar triangular wave into a sinusoidal output having a total harmonic distortion of less than 1%. The circuit uses a single operational amplifier and several diodes placed across its input and output ports to synthesize a transfer function that decreases the amplifier gain as output voltage increases. Thus it generates a piecewise-linear approximation of a sine wave for corresponding changes in triangular-signal amplitude.

The principle upon which the converter operates is simple, as shown in (a). If the input voltage to the op



Segmented sines. Diode and resistors (a) reduce op amp gain when output signal falls, placing point C at 0.6 volt. Circuit can be expanded to generate piecewise-linear approximation of half a sine wave (b) from triangle wave when other diode-resistor networks are added (c) to reduce gain further with increasing input voltage. Adding D_4–D_6 networks permits generation of other half cycle of sine wave.

amp is such that the output voltage is positive, diode D_1 does not conduct and the amplifier gain will be R_1/R. But when a positive input voltage from the triangular input is applied to the inverting port, the output will go negative and D_1 will conduct when point C reaches a threshold value of -0.6 volt.

In effect, if the internal impedance of the diode is neglected so long as it is conducting, resistor R_b is in parallel with R_1, and the amplifier gain is reduced to $R_1R_b/(R_1+R_b)R$. The change in gain occurs at point V_1 on the transfer function (b).

By placing additional resistor-diode networks that include D_2 and D_3 at the output of the op amp (c) and by selecting resistor values appropriately, the voltage at which conduction occurs for each diode can be set. So, for each progressive rise of the triangular voltage the transfer function can be extended to points V_2 and V_3. A good approximation to a half sinusoid can be obtained by using four segments for every quarter of a (sine wave) period, as shown.

To process the negative-polarity portion of the triangular wave (which is required to generate the other half of the sine wave), resistor-diode networks including D_4, D_5, and D_6 are placed in the circuit. Note that the diodes will conduct in sequence as the op amp's output voltage exceeds the predetermined positive values.

The component values have been selected to produce three segments corresponding to end-point values of $|V_1|=4.35, |V_2|=7.7, |V_3|=9.15$. V_P is limited by the maximum voltage of the input signal. Only resistors having a tolerance of 5% or below should be used in this circuit, to keep distortion to a minimum.

The gain of the op amp is most conveniently controlled by varying R and can be selected to handle a wide range of input voltages—from a few tens of millivolts to tens of volts. R should be about 1.8 kilohms for input voltages of 1v peak to peak and should be trimmed to minimize sine-wave distortion at the output.

The frequency response of the circuit will exceed 30 kilohertz when the TL081 op amp is used. □

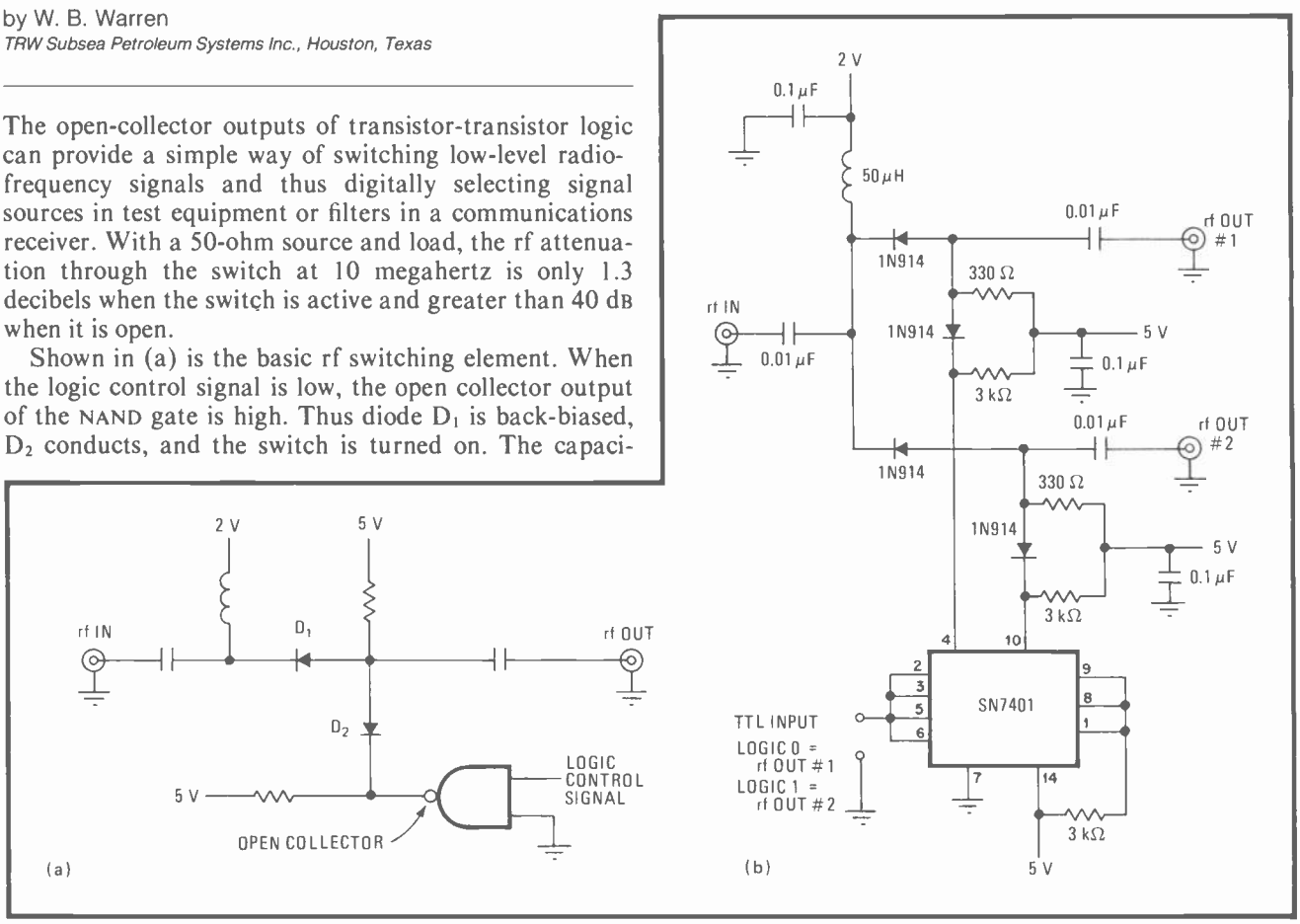
Open-collector logic switches rf signals

by W. B. Warren
TRW Subsea Petroleum Systems Inc., Houston, Texas

The open-collector outputs of transistor-transistor logic can provide a simple way of switching low-level radio-frequency signals and thus digitally selecting signal sources in test equipment or filters in a communications receiver. With a 50-ohm source and load, the rf attenuation through the switch at 10 megahertz is only 1.3 decibels when the switch is active and greater than 40 dB when it is open.

Shown in (a) is the basic rf switching element. When the logic control signal is low, the open collector output of the NAND gate is high. Thus diode D_1 is back-biased, D_2 conducts, and the switch is turned on. The capacitance of the open-collector output of the logic element will not affect circuit operation, since the reverse-biased D_1 prevents the element from shunting the rf path.

When the control signal is high, the open-collector output is low and D_1 conducts, forcing the dc voltage at



Digital rf switch. Logic signal is capable of switching low-level radio-frequency signals without significant attenuation, if open-collector transitor-transistor-logic element is used (a). Basic idea can easily be extended to single-pole, double-throw rf switch (b).

the junction of the diodes to a low value. The voltage across D_1 is therefore not sufficient to keep it conducting (that is, it is reverse-biased), and the rf signal cannot appear at the output.

The application of the basic element to a single-pole double-throw rf switch is shown in (b). Logic control for the SPDT switch is provided by two 7401 open-collector NAND gates. □

Converters simplify design of frequency multiplier

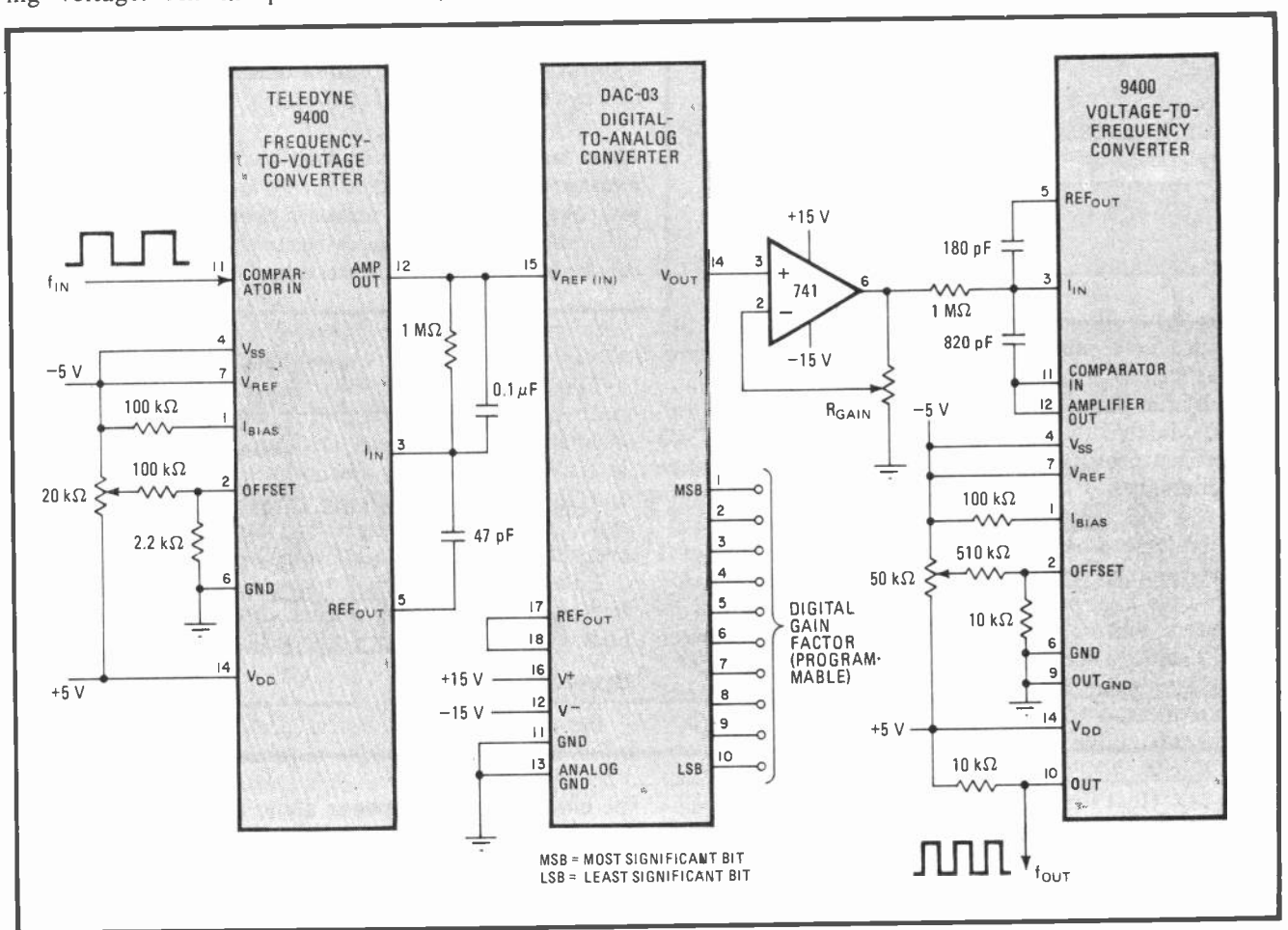
by Michael K. McBeath
Burroughs Corp., Goleta, Calif.

By using a programmable digital-to-analog converter in combination with frequency-to-voltage and voltage-to-frequency converters, this circuit can multiply an input frequency by any number. Because it needs neither combinational logic nor a high-speed counter, it is more flexible than competing designs, uses fewer parts, and is simpler to build.

As shown in the figure, the V-f converter, a Teledyne 9400, transforms the input frequency into a corresponding voltage. An inexpensive device, the converter requires only a few external components for setting its upper operating frequency as high as 100 kilohertz.

Next the signal is applied to the reference port of the DAC-03 d-a converter, where it is amplified by the frequency-multiplying factor programmed into the converter by thumbwheel switches or a microprocessor. The d-a converter's output is the product of the analog input voltage and the digital gain factor.

R_3 sets the gain of the 741 op amp to any value, providing trim adjustment or a convenient way to scale the d-a converter's output to a much higher or lower voltage for the final stage, a 9400 converter that operates in the voltage-to-frequency mode. The 741 and R_3 can also be used to set circuit gain to noninteger values. The V-f device then converts the input voltage into a proportionally higher or lower frequency. □



All numbers. Circuit uses frequency-to-voltage-to-frequency conversion, with intermediate stage of gain between conversions, for multiplying input frequency by any number. Digital-to-analog converter is programmed digitally, by thumbwheel switches or microprocessor, for coarse selection of frequency-multiplying factor; 741 provides fine gain, enables choice of non-integer multiplication values.

Zero-sensing counter yields data's magnitude and sign

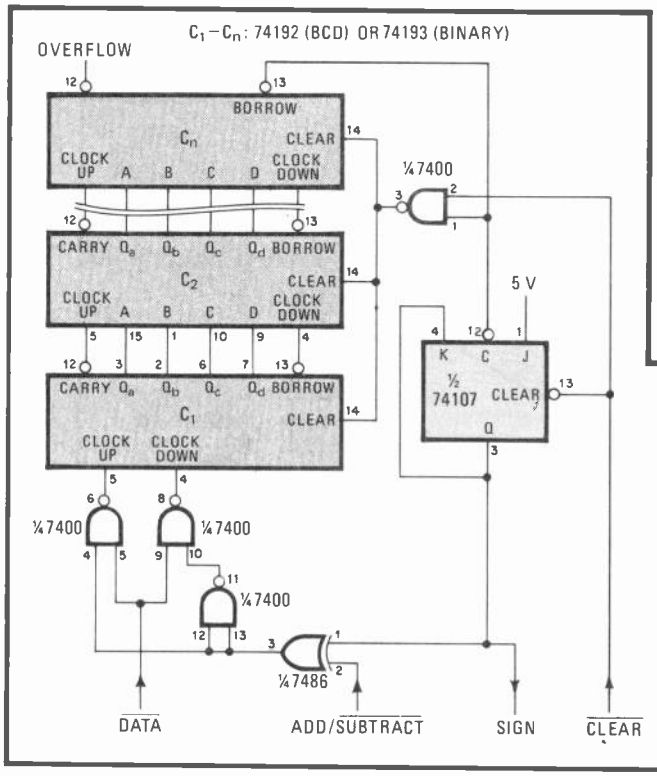
by Gary A. Frazier
Richardson, Texas

Upon sensing when an ordinary up-down counter is about to count down through zero, this circuit reverses the direction of the count to enable it to express a negative number by its magnitude and sign, instead of by the more usual but less convenient 2's complement. The circuit similarly represents positive integers, making it easy for any stored value to be handled directly by such data-system devices as digital-to-analog converters or microprocessors.

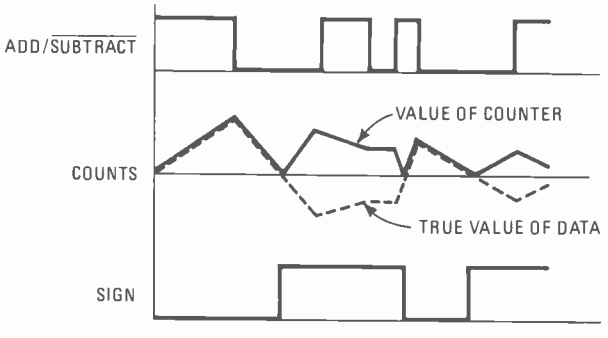
The unit shown in the figure has been found particularly useful in a digital-averaging application. Data is sampled during an interval in which the ADD/$\overline{\text{SUB}}$ line is toggled at some frequency, which in this case varies with time, as shown. Any data in phase with the ADD/$\overline{\text{SUB}}$ signal will accumulate in the n-stage counter (count-up mode), and digital noise will be averaged out (subtracted). The output of the counter is sampled at the end of the data-collection interval.

If the contents of the counter should ever decrease to zero, a borrow pulse is generated by the most significant counter, C_n, and toggles the flip-flop. In turn, the NAND gate connected to the clock-up port of C_1 is enabled. In this way, the output of the counter is mirrored about 0, as shown in the timing diagram, and is equal to the absolute value of the difference between the number of the add-to and the subtract-from counts. The sign bit is set each time the data actually drops below zero.

Note that when using the up-down counter, it is necessary to keep the counter cleared while the $\overline{\text{BORROW}}$ is low to avoid difficulties should the clock-up line suddenly become disabled while the clock-down line is activated. Otherwise, a decrement will take place. The frequency and symmetry of the ADD/$\overline{\text{SUB}}$ waveform is arbitrary so long as the counter does not overflow on any half cycle of a sampling interval. □



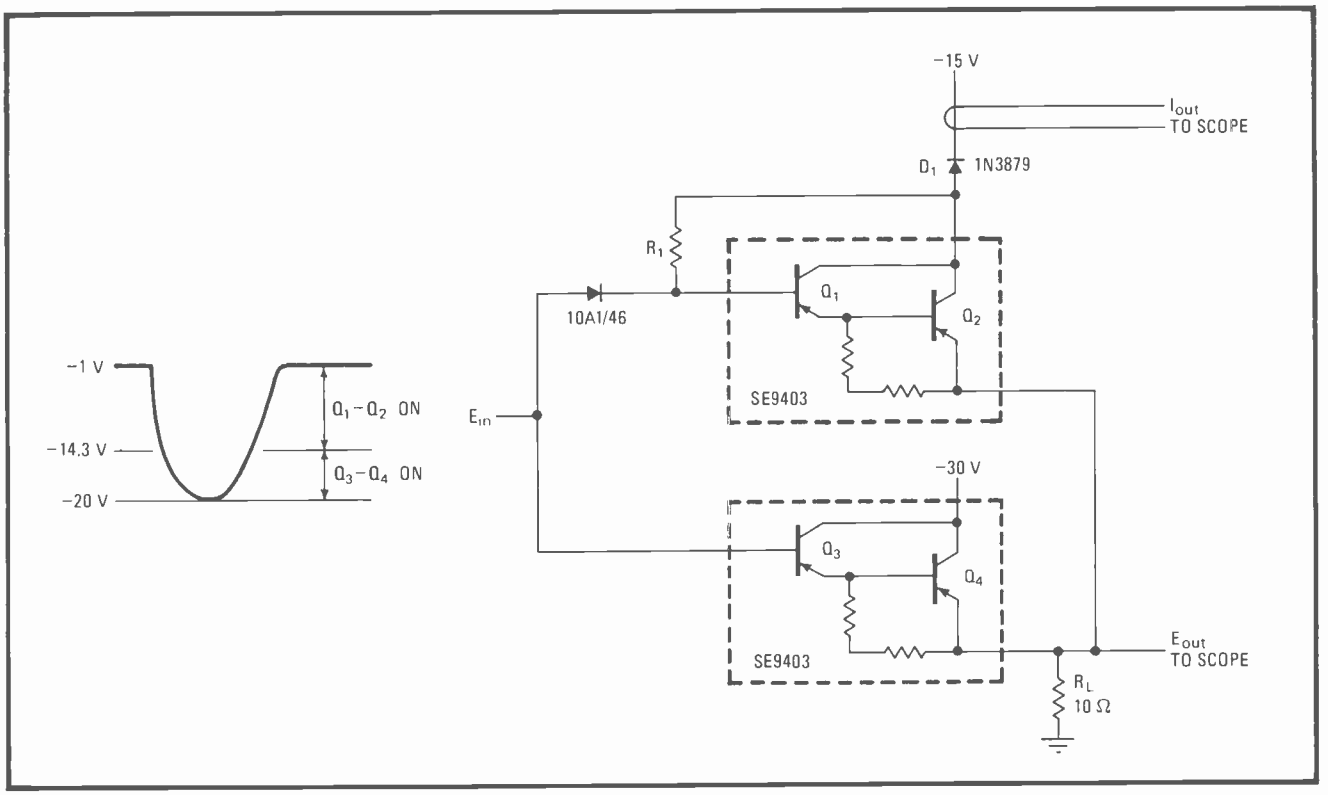
About face. Circuit inhibits up-down counters C_1–C_n from decrementing below zero, instead forcing them to count up and mirror the result of a negative-number addition in binary form. A negative-sign bit is also generated. Thus, all numbers are suitable for direct handling by a d-a converter or other data-system device.



Demand-switched supply boosts amplifier efficiency

by Jerome Leiner
Loral Electronic Systems, Yonkers, N. Y.

The efficiency of high-power audio amplifiers operating in class B will be improved by up to 80% at low power levels if the supply voltage can be switched from a low to a high value as the power demands on the amplifier increase. Using the automatic-switching circuit described here ensures a lower heat dissipation than would be possible with an amplifier that delivers a low-power output from a single high-voltage supply, which is the



High efficiency. Audio power amplifier switches from Darlington pair Q_1–Q_2 and low-voltage supply to Q_3–Q_4 and high-voltage supply only when power output demands increase. Circuit thereby eliminates the need for amplifier to dissipate excessive heat, a condition that occurs when an amp with a single high-voltage supply is used to process a low-amplitude input signal.

most common situation. The increased efficiency of this power amplifier can produce considerable savings in its weight and size and also reduces the amplifier's heat sink requirements.

The amplifier is designed to switch from the low- to the high-voltage supply as the audio signal level passes up through the low-voltage supply level. The switchover is made with virtually no perturbation in the output current up to as high as 25 kilohertz. At higher speeds, any waveshape distortion can be reduced by implementing negative feedback around the amplifier. Both supply voltages can be derived from one source, with the low voltage taken from a selected tap on the power transformer.

Several circuit configurations were tried, among them a cascaded emitter follower, a series transistor configuration, and the parallel transistor arrangement shown in the figure. The cascaded emitter follower and the series configuration performed adequately below 10 kHz. At higher frequencies, however, the effects of carrier storage produced by the first two arrangements caused large perturbations in the output current. The parallel arrangement finally adopted has virtually no storage problem and appears to be the most useful at higher frequencies.

For simplicity, the operation of one half of a complementary-output stage (see figure) is described. A half-sine wave that swings from −1 to −20 volts is the input-signal source in this case.

When the input level is at −1 v, current flows through D_2, R_1, and D_1. Thus the input base of Darlington pair Q_1–Q_2 is one diode drop lower than the base of Q_3–Q_4. As a result, Q_1–Q_2, which uses the −15-v supply, is on and Q_3–Q_4 is off.

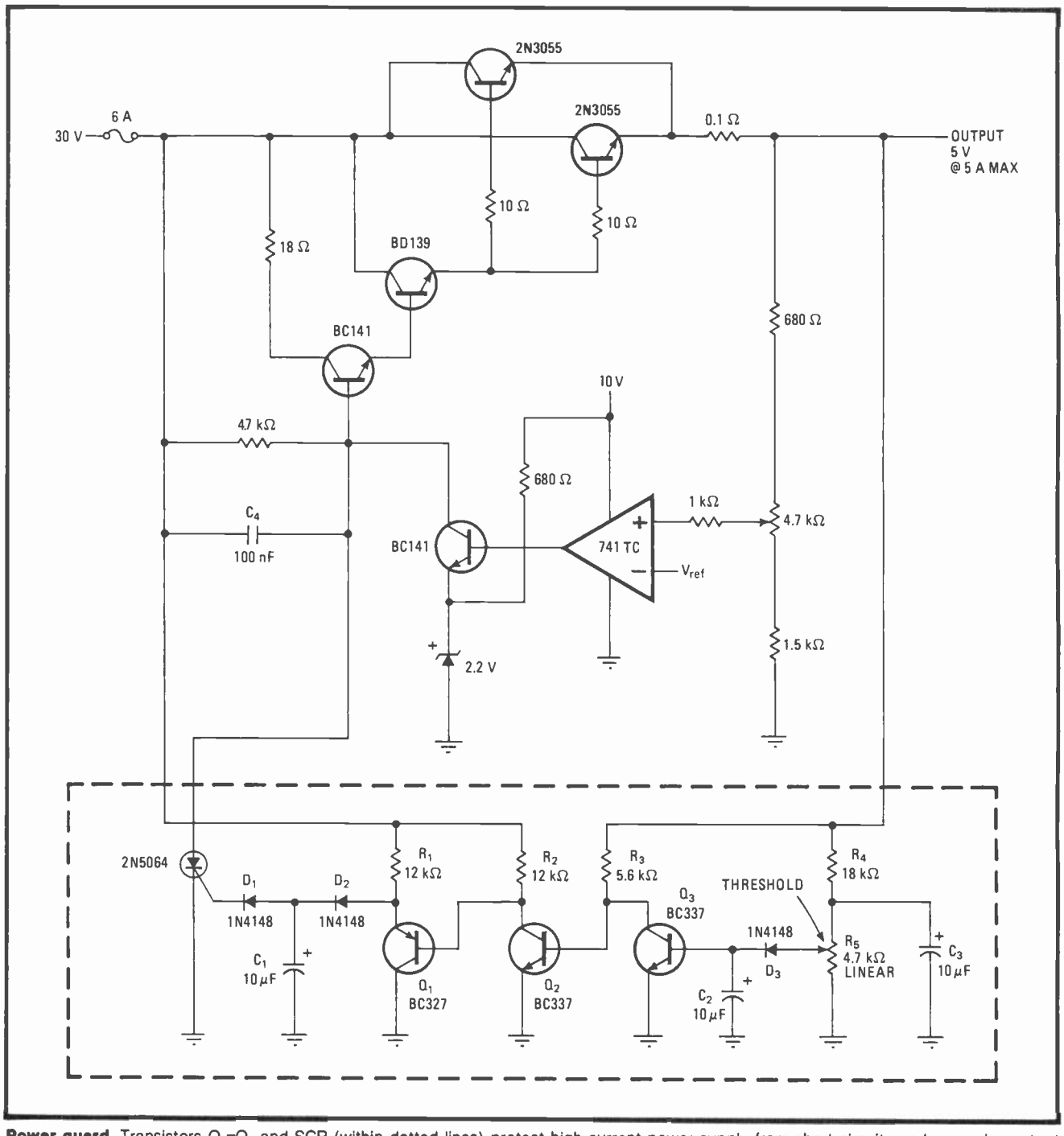
When the input signal reaches within one diode drop of the low-voltage power supply, D_2 begins to turn off and Q_3–Q_4, which uses the −30-v supply, starts to turn on. As Q_3–Q_4 moves into the linear region, Q_1–Q_2 begins to turn off, so there is a smooth transition of current in the load. Q_3–Q_4 stays on until the signal polarity reverses; when the signal passes through the low-voltage supply level, Q_1–Q_2 goes on and Q_3–Q_4 goes off. □

Fast-acting voltage detector protects high-current supplies

by Jorges S. Lucas
Engeletro, Belo Horizonte, Brazil

Protecting a regulated, nonswitching power supply against both short circuits and overvoltages can be difficult, especially if the supply is to deliver high currents. Should either condition occur, this circuit will act quickly to protect the supply, and its load as well, by deactivating the series or shunt pass element in the regulator and thus forcing the output current and voltage to zero.

A typical high-current power supply (5 volts at 5



Power guard. Transistors Q_1–Q_3 and SCR (within dotted lines) protect high-current power supply from short circuits and excessive output voltage. On occurrence of either event, Q_2 turns on, disabling Q_1 and enabling SCR to fire, shutting down supply's regulator.

amperes), which is modified slightly to accommodate the protection circuitry (dotted lines), is shown in the figure. When a short circuit occurs at the output, Q_2 goes off, which in turn disables Q_1. The voltage at the gate of the silicon controlled rectifier then rises at a rate determined by the time constant of elements R_1, D_1, D_2, and C_1. This delay prevents the SCR from triggering when power is first applied to the circuit. The SCR then fires, disabling the BC141/BC139 transistors in the power supply and shutting down the regulator.

Q_3, on the other hand, detects when the output voltage climbs above a user-set threshold. Once the threshold is exceeded, Q_3's base voltage rises at a rate determined by the time constant of elements C_2, R_4, D_3, and threshold potentiometer R_5 (delay must be provided for the reason discussed previously).

Q_3 then turns on. Q_2 and Q_1 react accordingly, and the SCR fires, as it did for the short circuit. Normal circuit operation may be restored simply by turning the power supply off and removing the abnormal condition, then switching on the supply again. □

Optoisolators slash cost of three-phase detector

by G. Olivier and G. E. April
Concordia University and Montreal Polytechnic Institute, Canada

Optically coupled isolators replace transformers in a zero-voltage detector for synchronizing the firing of a thyristor in three-phase control applications, making this circuit cheaper, less bulky, and simpler than most competing designs. Moreover, the optoisolators eliminate the need for a low-pass filter, required in standard detectors for eliminating spurious zero-crossings caused by the thyristor's switching transients. They also provide high-voltage isolation and present much lower capacitive coupling to the circuit than a standard transformer, in fact presenting about as low a coupling as double-shielded types.

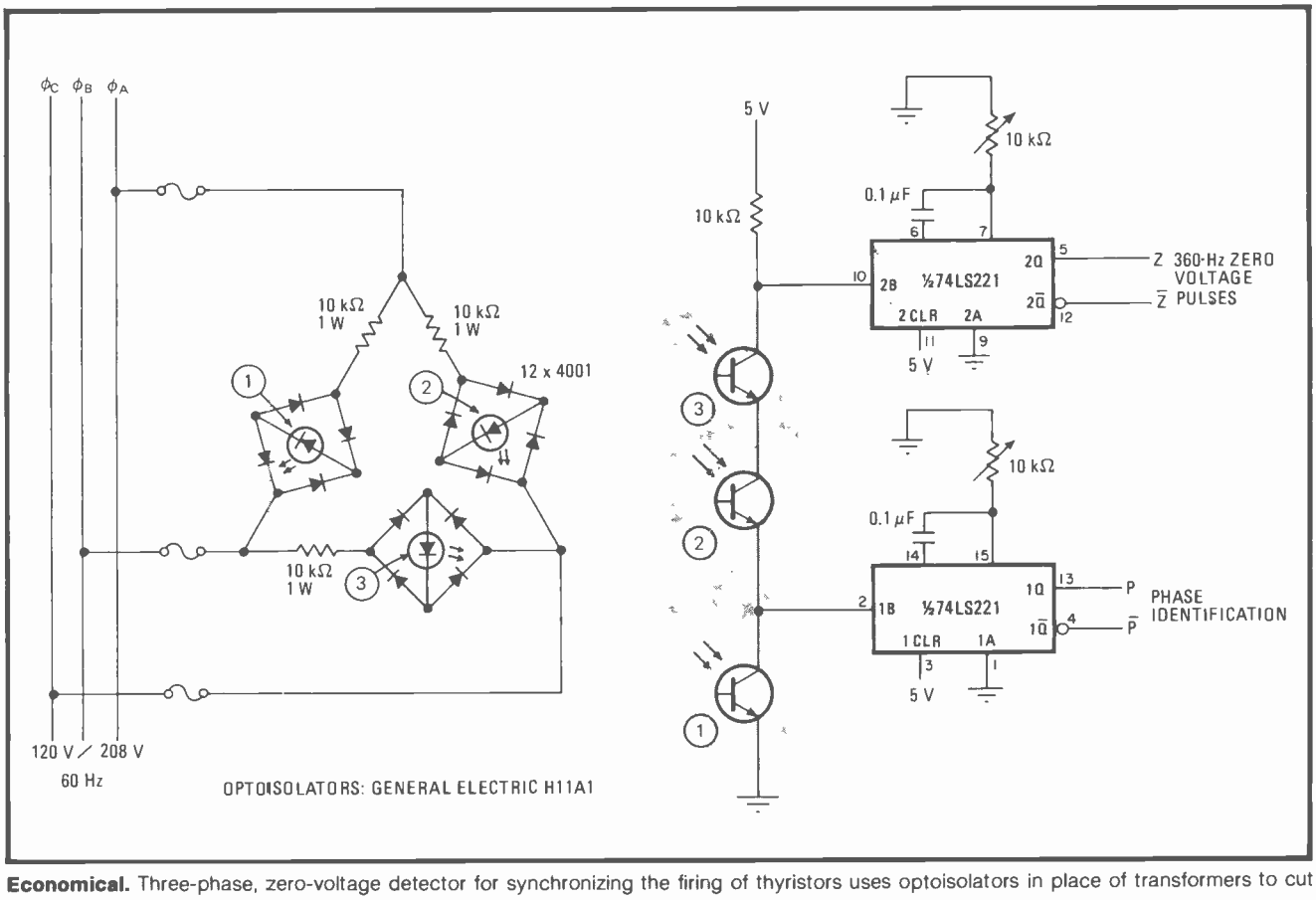
As shown in the figure, a light-emitting diode (contained in the GE H11A1 optoisolator) is inserted in each of three legs of a delta network. Each LED is wired to four standard diodes in a bridge arrangement, to enable it to respond to both polarities of the power-line input.

During most of the cycle, all phototransistors are on. At times when the voltage between any two lines is within 0.7 volt of zero, however, no current will flow through the LED connected across those lines. Therefore its corresponding phototransistor will be off, causing pin 2 of the 74LS221 one-shot to fire and a phase-identification pulse (P) to be generated twice every cycle.

In the case illustrated, the phototransistors are wired so that a pulse will be generated at the output each time the input voltage, as measured across ϕ_a and ϕ_b, passes through zero. Note that the one-shot should be adjusted so that the trailing edge of the output pulse corresponds to the actual zero-crossing point.

Identification pulses are also generated for all three phases collectively and these can be accessed, if required, at the zero-voltage pulse output, Z. These pulses occur three times as often as P.

Because at least one LED is conducting at any one time, no transient will normally be generated, so no low-pass filter is needed. Furthermore, the phototransistor's slow response of a few microseconds acts to suppress any transients that might occur near the zero-voltage points, thereby increasing the circuit's noise immunity. □



Economical. Three-phase, zero-voltage detector for synchronizing the firing of thyristors uses optoisolators in place of transformers to cut cost and bulk. Optocouplers provide circuit with high-voltage isolation and lower capacitive coupling than transformers.

One-chip oscillator generates in-quadrature waveforms

by Juan R. Pimentel
Department of Electrical Engineering, University of Virginia, Charlottesville

A quad operational amplifier, working as an oscillator, can generate in-quadrature signals for triangular or square waves, thus eliminating the need for phase-locked loops or other synchronous circuits in applications requiring either wave to be shifted by 90°. The low-cost circuit works over a wide range, thanks to a technique borrowed from Graeme[1] that uses op amps in an oscillator to generate in-quadrature sine waves.

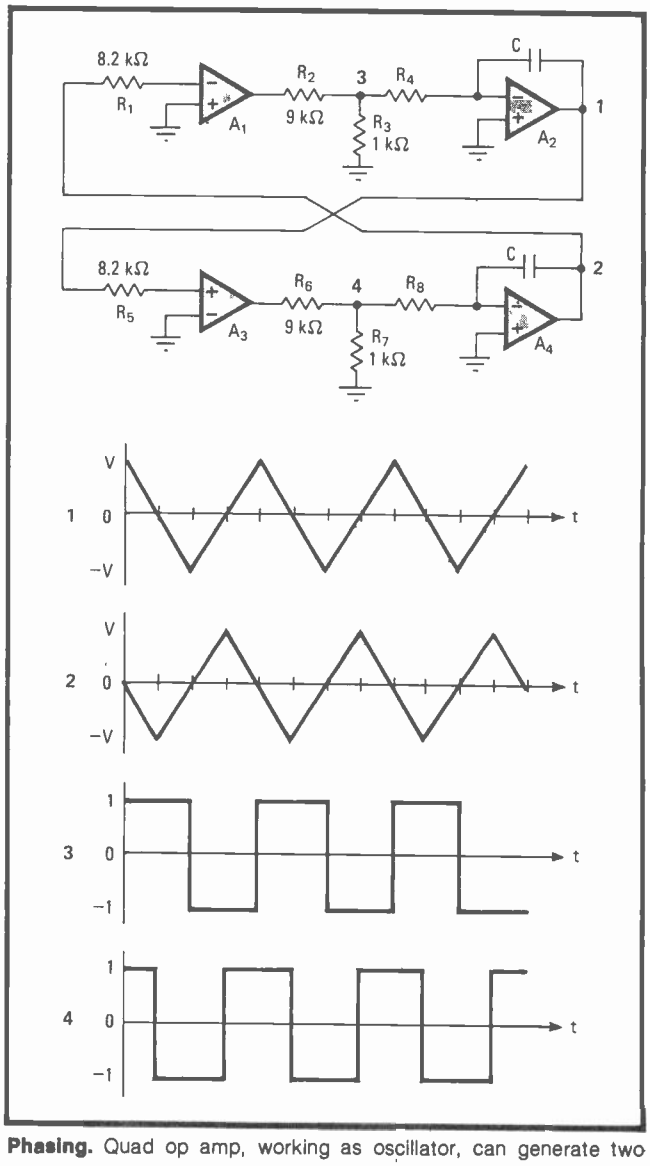
Op amps A_1 and A_3 function as comparators, and A_2 and A_4 as integrators, as shown in the figure. Resistors R_2, R_3, R_6, and R_7 are selected so that 1 volt appears across R_3 and R_7 when A_1 and A_3 are saturated (any other voltage could be chosen).

Circuit operation is simple. If A_3 is saturated at its negative power-supply value, the voltage across R_7 will be -1 v. The voltage at the output of integrator A_4 will then have a positive slope and increase linearly with time, because the input signal is introduced to A_4's inverting port.

When A_4's output passes through zero, the voltage across R_3 will reach -1 v, causing A_2's output to increase linearly (positive slope). Similarly, when the output of A_2 passes through zero, the voltage across R_7 will reach $+1$ v, causing A_4's output to decrease linearly in the negative direction. This operation will repeat, yielding the waveforms shown below the circuit diagram.

The time required to complete one cycle is $T = 4RCV$, and so the frequency of oscillation is $f = \frac{1}{4}RCV$, where $R = R_4 = R_8$ and V is the power supply voltage. These equations assume a peak output of ± 1 v at points 3 and 4. □

References
1. J. G. Graeme, G. E. Tobey, and L. P. Huelsman, "Operational Amplifiers—Design and Applications," McGraw-Hill, 1971.



Phasing. Quad op amp, working as oscillator, can generate two triangular- or square-wave outputs that are separated by 90°, thereby eliminating the need for phase-locked loops or other synchronous circuits. Frequency can be controlled by appropriate selection of resistors and capacitors associated with integrators A_2 and A_4.

One-button controller issues step, run, and halt commands

by Robert Dougherty
Dunedin, Fla.

The logic signals to step, run, and halt a computer or other appropriate digital device or system may be generated by this circuit, which is operated by just a single push button. The only active devices used are a dual one-shot and a dual flip-flop.

The step command is generated each time the push button is depressed momentarily. The run command occurs if the button is held down for a time exceeding about 180 milliseconds. This time represents an excellent compromise between circuit speed and accuracy. A much shorter duration means the circuit may fail to differentiate between the step and run commands and may generate the run command when the step command is desired, or vice versa. Also, repeatedly pressing the button rapidly to initiate step functions will generate the run command if the duration is set for much more than 180 ms. Finally, the computer will be halted if the push button is depressed momentarily when the circuit is in the run mode.

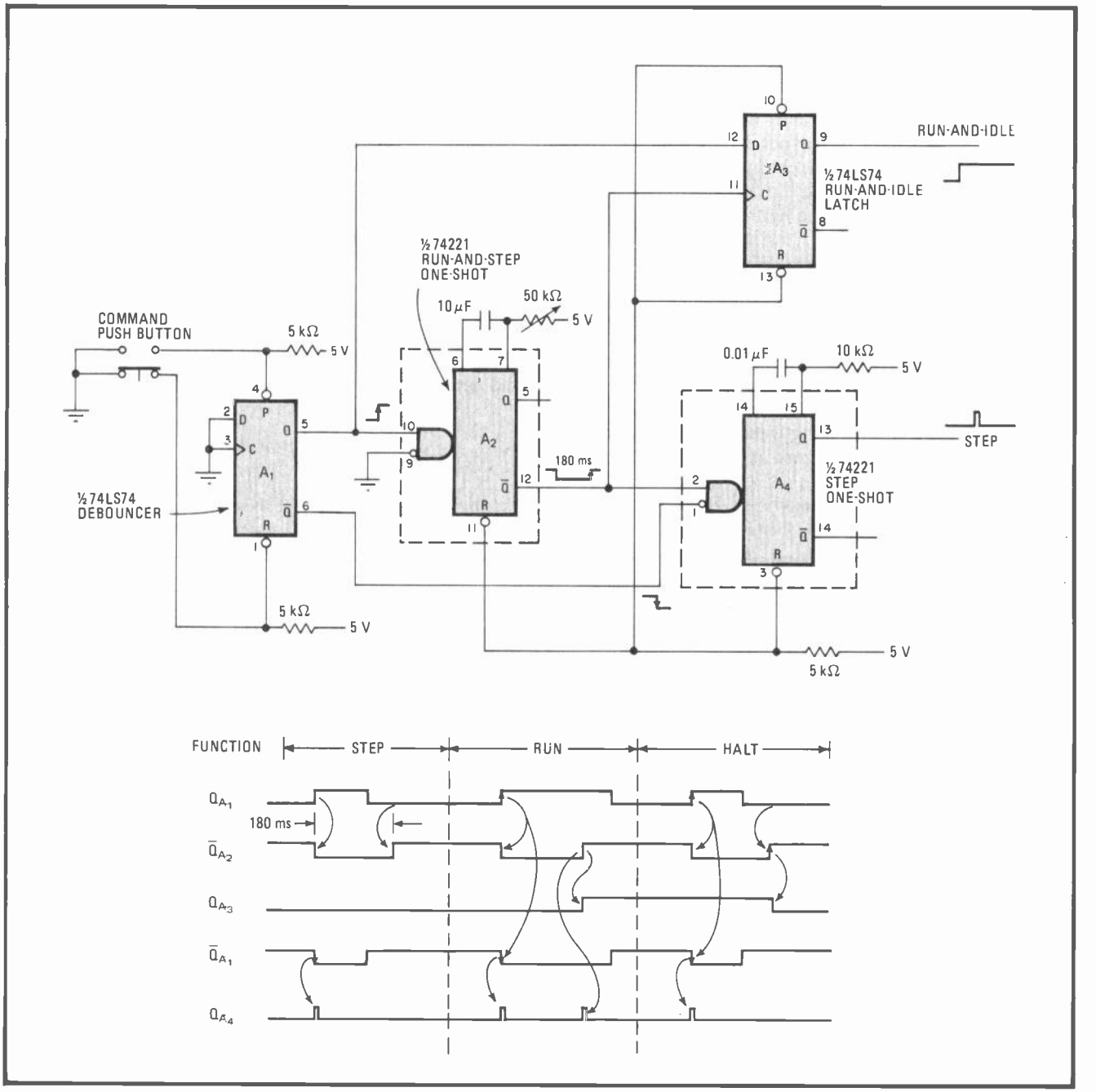
As shown in the figure, A_1 acts as an effective switch debouncer for the push button. For a step command,

poking the button quickly will cause the Q output of A_1 to go high and fire A_2, the run-and-stop one-shot. A_1 is also fed to A_3, the D input of the run-and-idle latch. At the same time, the $\overline{Q}$ output of A_1, which moves low, will fire the step one-shot A_4, yielding the step function.

The sequence of events just discussed also describes the initial portion of the run command, whereby the step pulse is used to manually advance the computer's program counter by one. The run pulse then commands the computer to rapidly execute succeeding steps automatically. The $\overline{Q}$ output of A_2 moves high 180 ms after the push button is depressed. The positive-going, or trailing, edge of this pulse then clocks the state of the push button (as detected by A_1) into A_3.

If the button has been released before time-out, a zero appears at the Q output of A_3. But if the button is activated, A_3 moves high and the run command is executed by the computer.

A press of the button will cause the circuit to halt the machine if it is in the run mode, by clocking in a logic 0 to the run-and-idle latch. Note that the step pulse generated at the start of the halt sequence, as shown in the timing diagram, is of no consequence, since when the step is received, the machine is already in the run mode and will override that command. □



Touch control. One push button and two ICs single-step a computer's program counter or control run and halt operations. Button-depression time and present mode of controller determine the command generated. Timing diagram details circuit operation.

Wien bridge and op amp select notch filter's bandwidth

by Dominique Fellot
Thomson-CSF, Gentilly, France

The band over which a notch filter provides rejection of unwanted frequencies can be selected with this circuit, which uses a Wien bridge plus an operational amplifier with fixed gain. Such a circuit represents one of the simplest configurations for easily adjusting the selectivity of the filter, which has a notch depth of nearly 60 decibels, independent of component precision.

Circuit operation is most easily described with the transfer function shown in the figure, which is:

$$\frac{V_o}{V_i} = \frac{1-R^2C^2\omega^2}{1-R^2C^2\omega^2+j3(1-k)RC\omega} = \frac{1-x^2}{1-x^2+j3(1-k)x} \quad (1)$$

where $x = \omega/\omega_c = f/f_c = RC\omega$, ω is the frequency of interest, f_c is the center frequency of the notch filter, and k is the percentage of the output voltage from A_1 that is introduced at the noninverting input of A_2. This transfer function has a transmission zero at $f_c = 1/2\pi RC$, which is the center frequency of the notch.

The amount of phase shift provided by the Wien bridge (A_1 and the RC components), from Eq. 1, is:

$$\tan\phi = [-3(1-k)x]/(1-x^2) \quad (2)$$

The width of the rejected band at the −3-dB points can be easily expressed with respect to k by setting $\phi = 45°$, so that Eq. 2 becomes:

$$|\tan\phi| = 1 = [3(1-k)x]/(1-x^2)$$

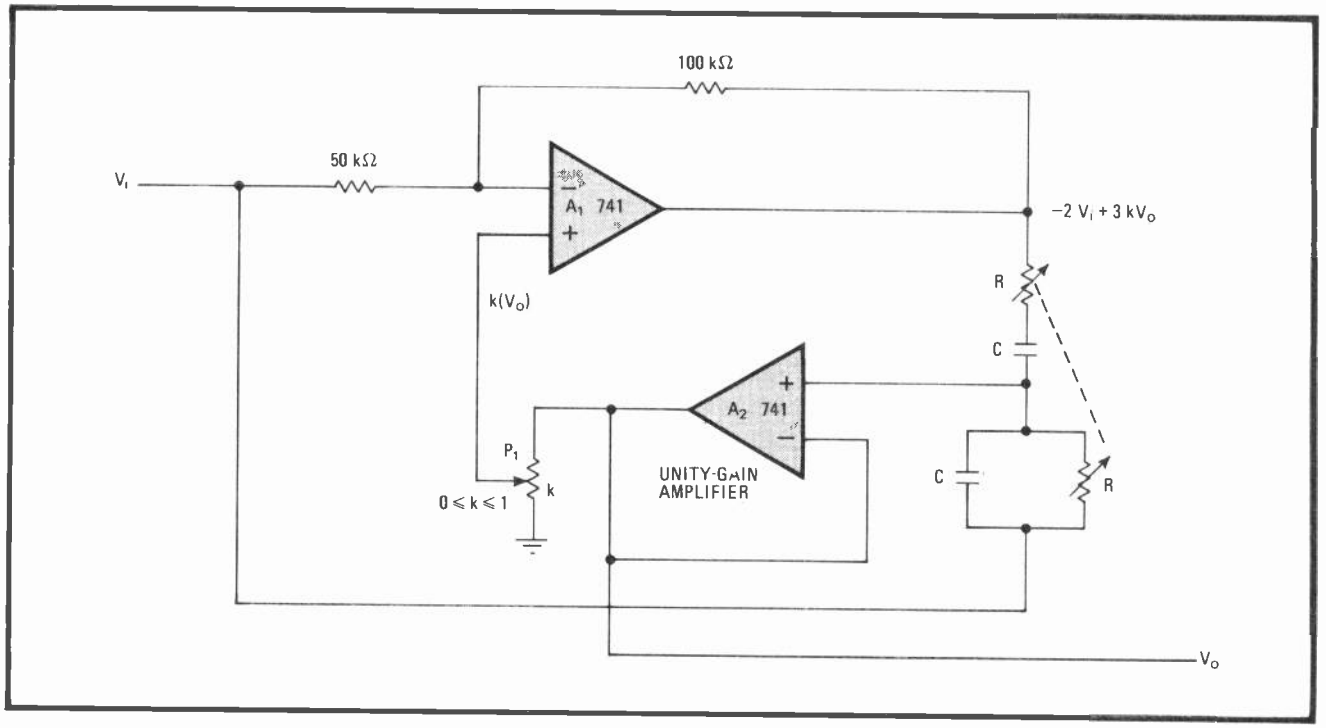
or:

$$k = (x^2+3x-1)/3x, \text{ for } x<1 \quad (3)$$

where $x = f_r/f_c$ and f_r is defined as the difference in frequency as measured at the −3-dB points. Thus, for example, if $f_c = 10$ kilohertz and the desired $x = 0.9$ (or $f_r = 9$ kHz), then k must be set at 0.93.

It will be noted that although the transfer function for the popular twin-T variety of notch filter (not shown) is almost identical to that in Eq. 1 (the constant 3 is replaced by the number 4), in practice, the twin-T is not very easily adjusted. This is because a greater number of components must be trimmed, and more careful adjustments made, to achieve the desired degree of selectivity and notch depth required. □

Selectable stopper. Notch filter, which operates at up to 200 kHz, uses modified Wien bridge to select bandwidth over which frequencies are rejected. RC components determine filter's center frequency. P_1 selects notch bandwidth. Notch depth is fixed at about 60 dB.



One-chip comparator circuit generates pulsed output

by Virgil Tiponut and Daniel Stoiciu
Timisoara, Romania

Generating a steady stream of pulses rather than the usual logic 0 or logic 1 output when triggered, this special comparator circuit is useful in many control applications. The one-chip circuit is perhaps the simplest way to build what is essentially a low-cost switched oscillator.

A 711 dual comparator serves as a Schmitt trigger and rectangular-wave generator, as shown in the figure. The Schmitt trigger (A_1, R_1, and R_2) has switched levels V_h and V_l, given by:

$$V_h = \frac{R_1}{R_1+R_2} V_H$$

$$V_l = \frac{R_1}{R_1+R_2} V_L$$

where V_H and V_L are the high and low output voltages, respectively (at pin 10), $V_H = V_s - 0.75$, and V_s is the comparator's strobe voltage.

The outputs of each comparator are connected in the wired-OR configuration. When the control voltage, V_i, is greater than the user-set reference, V_{ref}, the output of A_2 is low. Thus the output voltage, V_o, is determined by the signals at the input to comparator A_1.

A_1 will then begin to oscillate. The output V_o will move high to V_H because of the small differential voltage that exists across the input of A_1, charging C through D_1 and R_3. When the voltage across C, V_f, approaches V_H, A_1 switches, bringing V_o low. C then discharges through D_2 and R_4 until the voltage across C drops below that at the noninverting input. V_o then moves high again, charging C, and the process repeats.

Circuit operation may be visualized with the aid of the waveforms shown. A_1's switching times, T_1 and T_2, are given by:

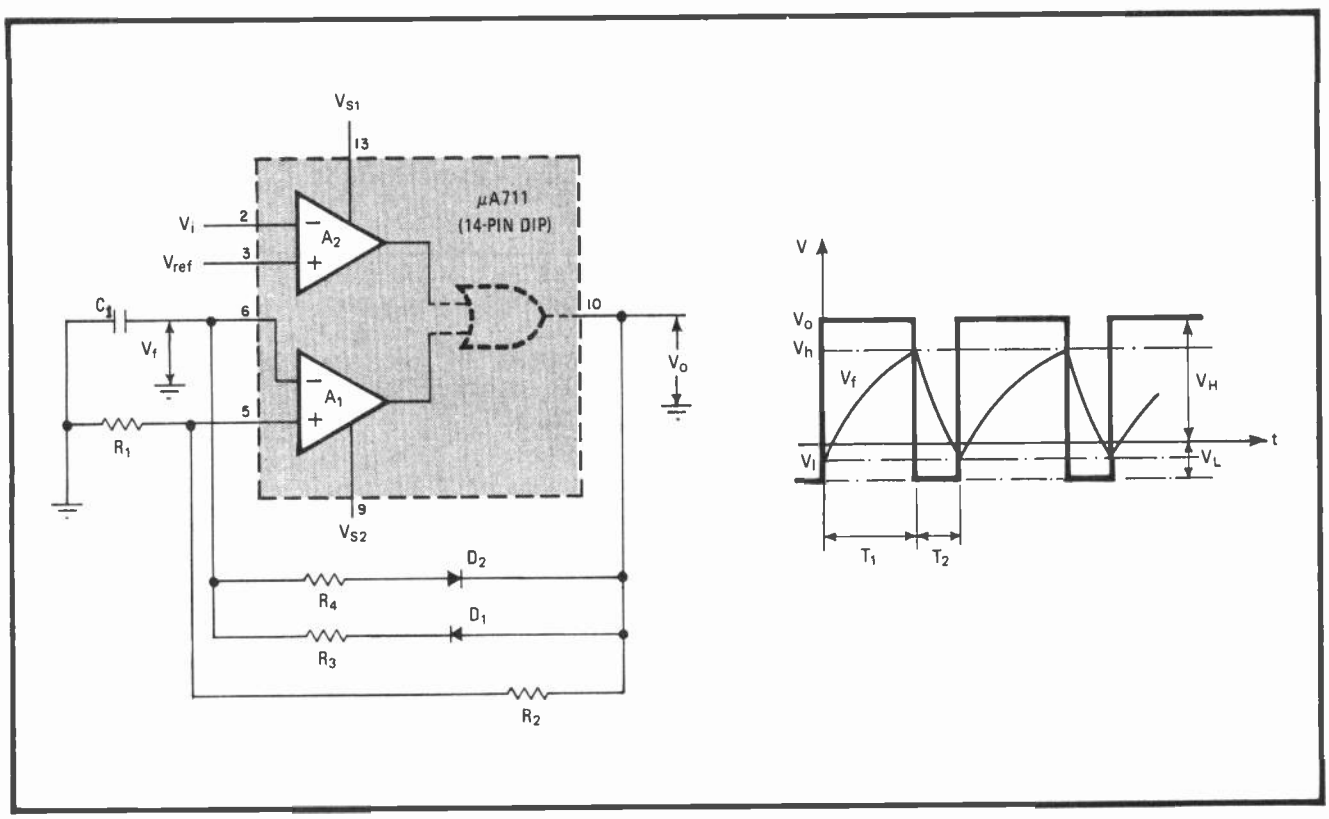
$$T_1 = C_1 R_3 \ln [(V_l - V_H)/(V_h - V_H)]$$

$$T_2 = C_1 R_4 \ln [(V_h - V_L)/(V_l - V_L)]$$

neglecting the output resistance of the comparator.

Oscillation ceases when V_i is less than V_{ref}. V_o then moves high permanently, since A_1 is prevented from affecting the output state. □

Pulsating comparator. One 711, wired as Schmitt trigger and oscillator, generates continuous train of rectangular waves when fired by control voltage, V_i. Output voltage V_o otherwise assumes logic 1 (high) state (when $V_i < V_{ref}$). Waveforms detail circuit operation.



Removing the constraints of C-MOS bilateral switches

by W. Chomik and A. J. Cousin
Department of Electrical Engineering, University of Toronto, Canada

Two major limitations imposed on the popular complementary-metal-oxide-semiconductor 4016 switch may be overcome with this circuit. As well as allowing the signal magnitude to exceed the power-supply voltage, it enables unipolar control signals to switch bipolar input signals. Only a second switch and an inverter need be added to a standard circuit to remove these operating constraints on the signal-handling gate.

Usually, the signal voltage to be passed through a single switch must be limited to between $V_{DD}+0.7$ volt and $V_{SS}-0.7$ v, where V_{DD} is the positive supply (drain) voltage and V_{SS} is the minus supply (source) voltage. Otherwise, the signal voltage will cause the forward biasing of the diode between the substrate and channel of one MOS field-effect transistor, and the gate may be destroyed.

This problem might arise if the power-supply value applied to some active element in a circuit happened to lie outside the voltage range that could be applied to the switch ($V_{DD}-V_{SS}$), dictating that the gate must be protected from input and control signals that saturate to the supply level.

Furthermore, many circuits, especially those containing operational amplifiers, use bipolar supplies. The resulting signals to be processed are likely to be bipolar as well. Yet the channel-voltage constraints inherent in the design of the 4016 (that is, the fact that the logic 0 control voltage, V_{SS}, must be at or below the most negative signal voltage, and the logic 1 control voltage, V_{DD}, must be at or above the most positive signal voltage) means that bipolar supplies and control signals must also be applied to the switch if these bipolar signals are to be passed. Unfortunately, too, many systems use digital control signals that are unipolar, and so logic-level shifters are needed also, to make this signal symmetrical with respect to ground.

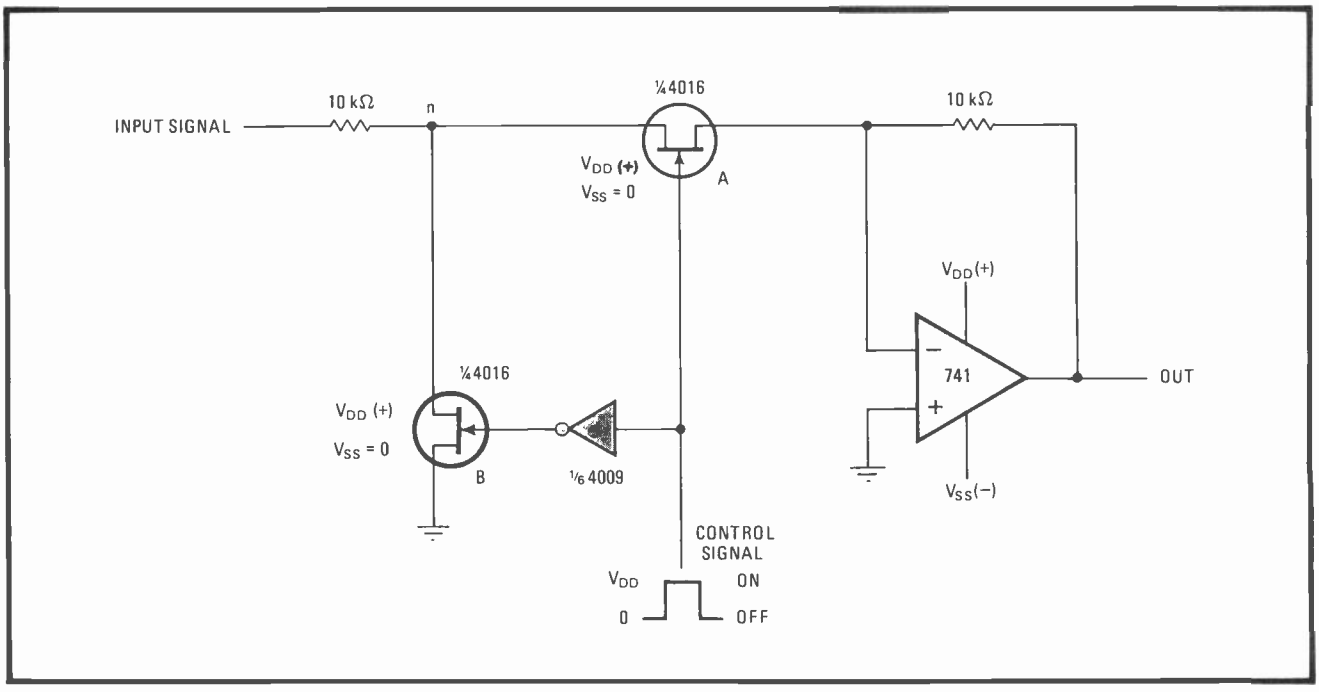
With the addition of a second bilateral switch and an inverter to a standard op-amp circuit, as shown, the signal-handling switch can operate from a single power supply and be driven by unipolar logic at the control input in order to pass bipolar signals. Moreover, the signal can lie outside the $V_{DD}-V_{SS}$ limit of the switches.

The channel voltage of both switches is set by fixing their drain potentials at the virtual ground of the op amp or to circuit ground, depending on which switch is on. Because the virtual ground never strays from true ground by more than a few millivolts, the switches will be protected from burn out, as their channel-voltage limit will never be exceeded.

When switch A is on and switch B is off, node n will be essentially at ground potential. When B is on and A is off, the signal is removed from the op amp's input, but node n will still be at ground (through B), and the same channel-voltage conditions will prevail.

Note that the actual input voltage to the gate at node n will never drop more than a few millivolts below the minimum control voltage, even if the input signal is negative. Thus, the gate's channel-voltage constraint is always met. □

No limitations. Inverter and gate B enable switching of bipolar input signals by unipolar control signals at gate A and also allow magnitude of input to exceed gate's supply voltage. Node n is held near to ground at all times, so that channel-voltage limit of gate is never exceeded. Magnitude of signal at node n never exceeds control-signal potential, enabling gate to switch properly.



Diodes adapt V-f converter for processing bipolar signals

by Jerald Graeme
Burr-Brown Research Corp., Tucson, Ariz

Two diodes and one operational amplifier will enable a voltage-to-frequency converter to process bipolar input signals, thus adapting it for operation in absolute-value circuits. Using the integrator of the converter eliminates at least one of the op amps normally required for such absolute-value converters. Moreover, the approach is simpler overall than ones that bias the converter's inputs at a value midway between supply voltage and ground.

When input signal e_i is positive (see figure), diode D_1 becomes forward-biased and D_2 is reverse-biased. Op amp A_1, which isolates the signal from the offset and bias currents of the V-f converter, then acts as a noninverting amplifier with a gain of $1+R_2/R_1$; it creates an integrator feedback current equal to $i_f = 10e_i/R_3$, provided that $R_4 = (R_1+R_2+R_3)R_3/(R_1+R_2-R_3)$. The voltage $e_i(1+R_2/R_1)$ at the inverting input of the V-f converter is then transformed into a corresponding frequency.

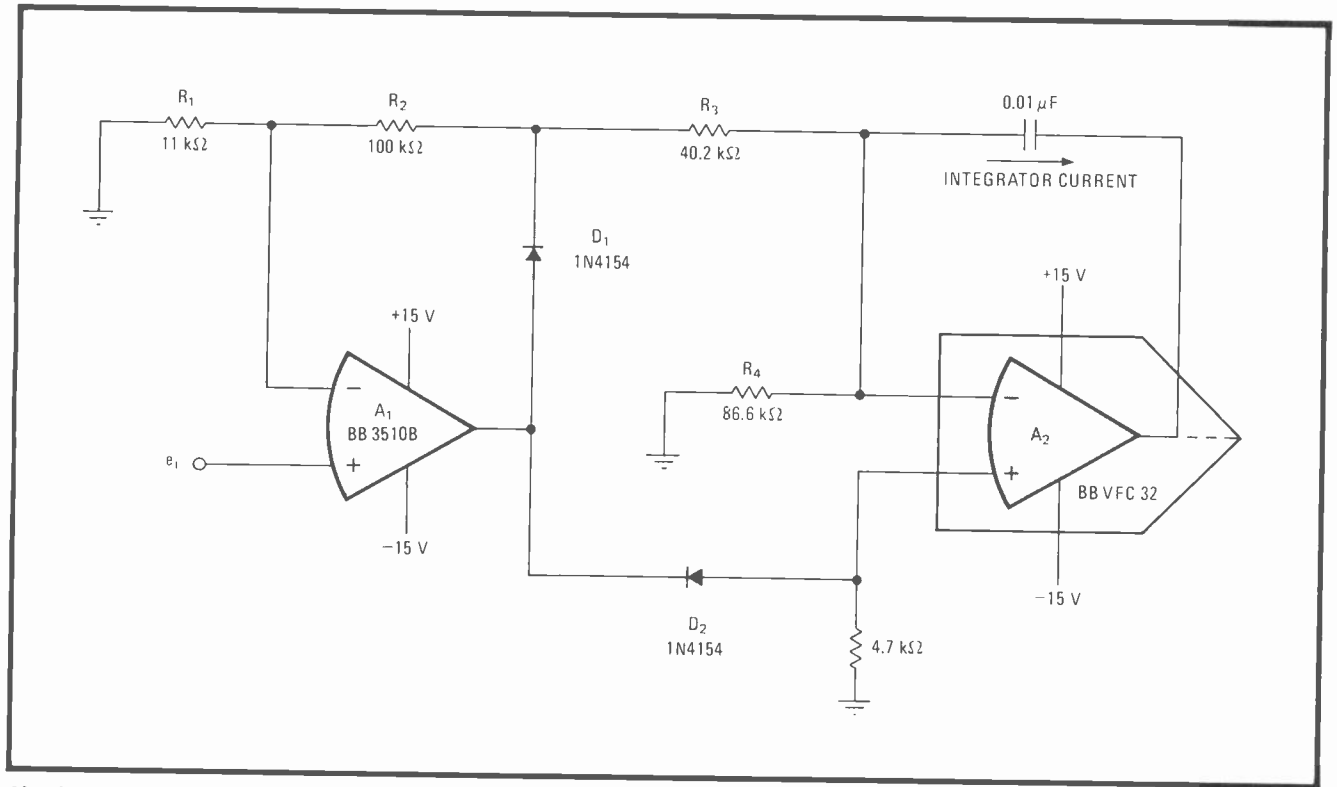
For negative values of e_i, D_1 is back-biased and D_2 is forward-biased, enabling the op amp's output signal to be applied to the noninverting input of the V-f converter. In this configuration, the gain is negative, so that the integrator current generated has the same polarity as before. Thus the V-f converter cannot distinguish positive and negative voltages having the same magnitude, and so generates the same frequency for both signals.

If D_1 and D_2 are replaced with the emitter-base junctions of any general-purpose transistors and the transistors' collectors are used to drive lamps or other indicators, the polarity of the input signal can be displayed. Care should be taken to avoid reverse emitter-base breakdown caused by large input-signal levels by placing diodes in series with the base of each transistor.

The accuracy of the converter is determined by the same factors as affect conventional absolute-value circuits: resistor-ratio matching and the op amp's input offset voltage.[1] It is most important that the R_1–R_4 resistor values be correct for a given gain, as they have a part in equalizing circuit gain for both signal polarities.

The op amp offset voltage must also be minimized. The standard trimming procedure will in effect remove any offset at the point where the diodes switch. The offset at the output of the V-f converter can then be removed by trimming its integrator circuit. □

References
1. J. Graeme, "Applications of Operational Amplifiers—Third Generation Techniques," McGraw-Hill, 1973.



Absolute switchover. D_1 and D_2 switch on alternately as polarity of input signal changes, thus maintaining direction of integrator current. V-f converter cannot distinguish between signal polarities of the same magnitude and so generates the same frequency for both.

Prescaler and LSI chip form 135-MHz counter

by Gary McClellan
La Habra, Calif.

Combining a prescaler designed for very high frequencies with large-scale integrated circuits and a few other devices builds a multifunction frequency counter capable of working at 135 megahertz. The counter, which uses complementary-metal-oxide-semiconductor and emitter-coupled-logic chips, has many desirable qualities, including the ability to measure the period of a waveform, moderate power consumption (100 milliamperes, including displays), good sensitivity (16 millivolts at 135 MHz), and portability.

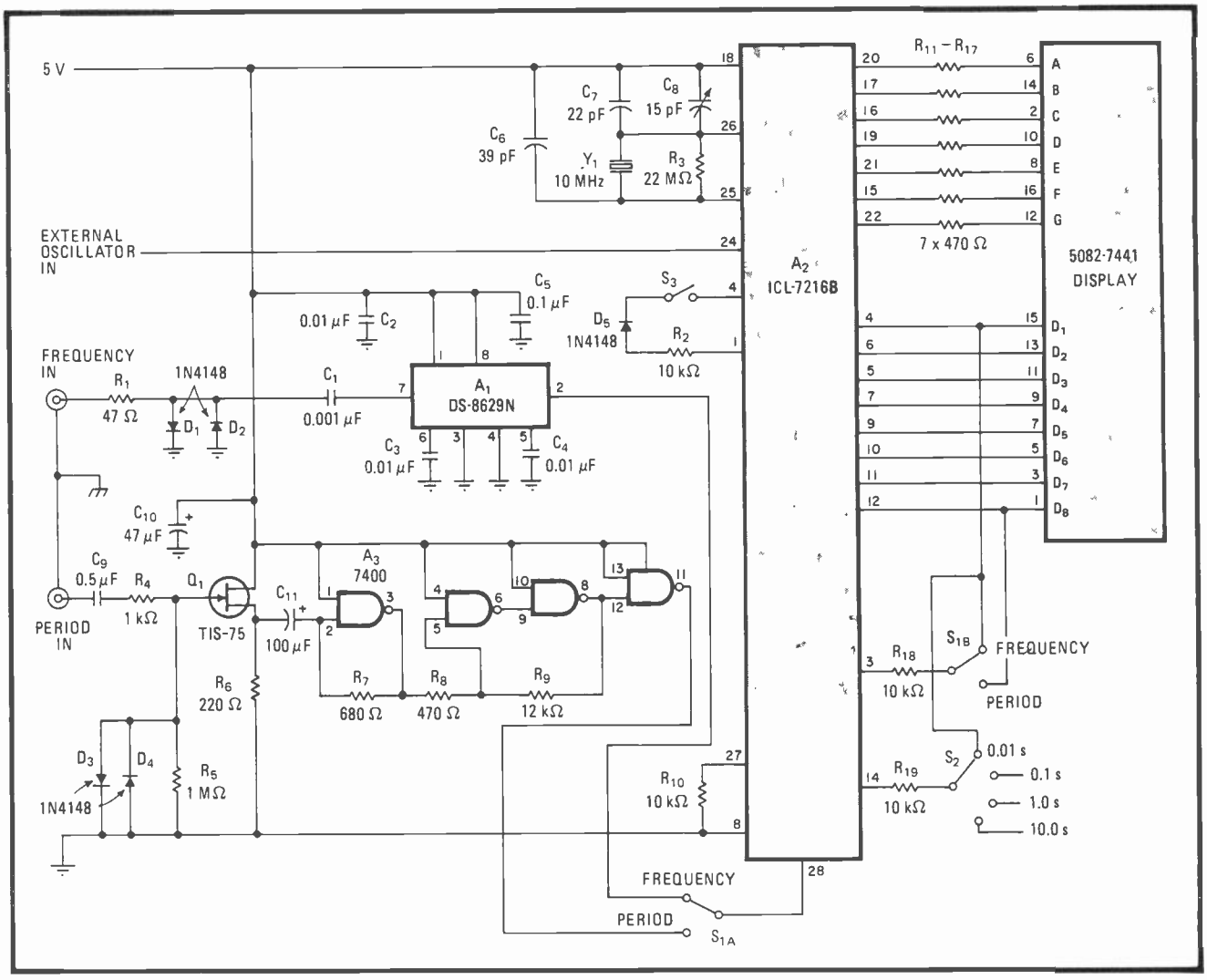
In the frequency mode (selected by switch S_1), signals at the input are limited by the resistance-capacitance network and two diodes (see figure) so as to prevent overloading of A_1, the National DS-8629N prescaler. A_1 amplifies the signal and divides it by 100, and then it is counted by A_2, the Intersil ICL-7216B.

The ICL-7216B contains a counter, a display multiplexer, a seven-segment decoder, and digit and segment circuits for driving A_3, the HP 5082-7441 display. The chip also provides timing for the system, including the necessary oscillator circuitry and frequency dividers to generate the gate, latch, and reset pulses for multiplexing the display and controlling the sampling interval (selected by S_2).

In the period mode, input signals are limited in order to protect Q_1, an impedance converter. A simple preamp and Schmitt trigger, A_3, converts the signal to appropriate levels for A_2.

The counter also has provision for an external oscillator input. When properly used with an external 10-MHz standard, it makes measurements with a high degree of accuracy. S_3 enables the measurement.

Calibration is easy. A signal of known frequency is connected to the frequency input (a 100-MHz signal is ideal), and the 15-picofarad capacitor, which is in parallel with crystal Y_1, is adjusted for a matching counter reading. Accuracy is not greatly affected by the supply



Counting high. Three-chip circuit uses prescaler and LSI chip in frequency counter capable of operating at 135 MHz. Circuit draws total of 100 milliamperes, has good sensitivity, is portable. Counter should be built on double-sided pc board for best performance.

voltage, as the counter holds to within two counts of the displayed frequency over 4.5 to 5.5 volts.

The counter is best built on a double-sided printed-circuit board. Parts layout is not critical, with the exception of the input leads, which should be positioned away from the display. Also, A_1 should have foil running on its underside, to act both as a heatsink and as shielding. □

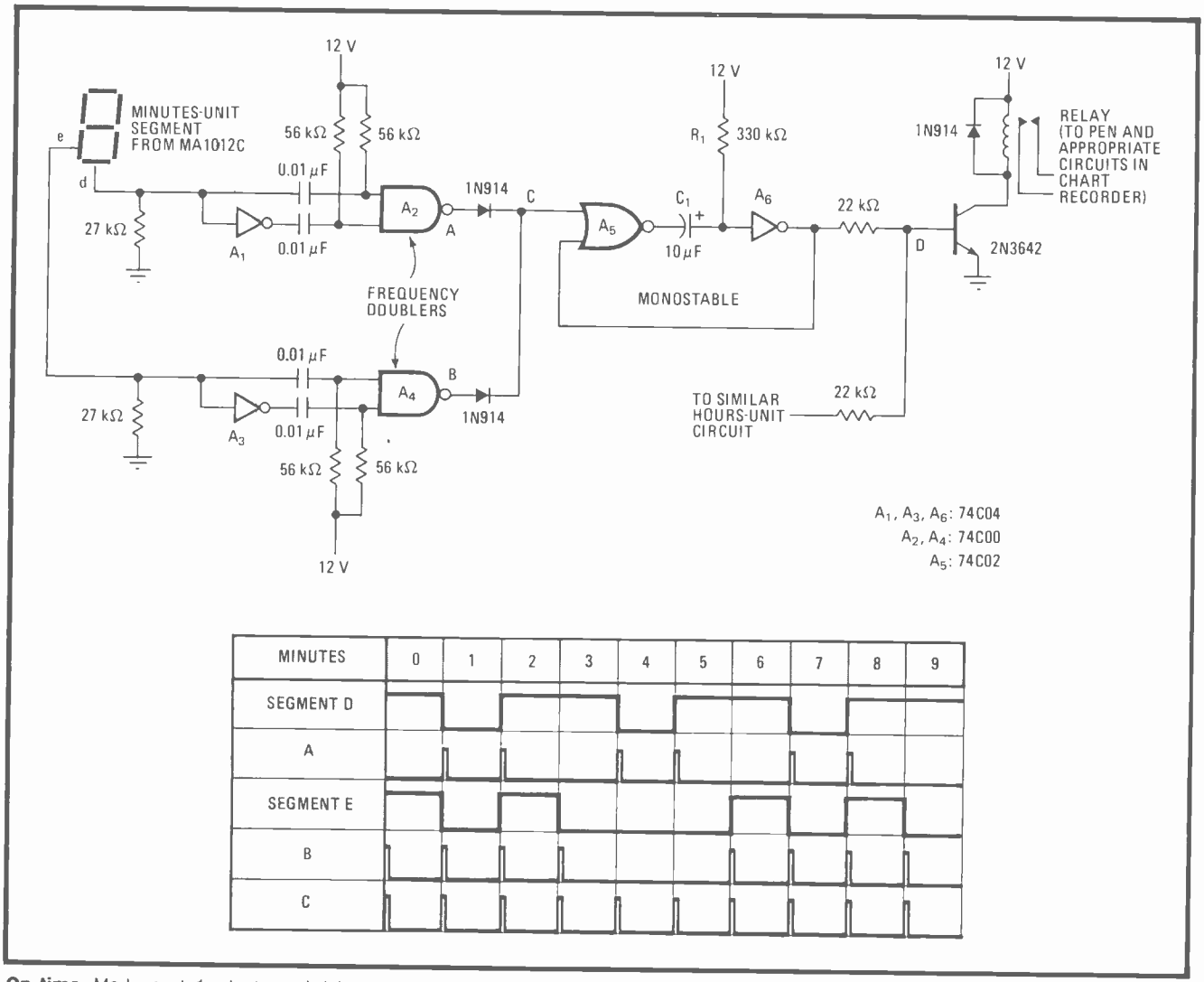
Clock module supplies chart-recorder time markers

by G. J. Millard
Volcanological Observatory, Rabaul, Papua, New Guinea

Utilizing the display segments of a standard digital clock module—or more precisely, the signals that drive them—this circuit enables a chart recorder to mark intervals of 1 minute or 1 hour or both. Use of an already built electronic clock, such as National Semiconductor's popular MA1012C, guarantees a chronometer that is accurate, simple to construct, and low in cost ($25).

The 1-minute markers are developed from the signals that drive segments d and e of the minutes-unit display in the MA1012C. These signals, which are readily accessible, drive two frequency doublers, A_1–A_4, that in turn produce a pulse at point C every minute. The pulse then triggers a one-shot (A_5, A_6, R_1, C_1), which switches the relay on for 2 seconds.

If desired, markers can be generated at 1-hour intervals by connecting segments d and e of the hours-unit display to a similar circuit, the output of which is connected to point D. To differentiate between the minute and hour markers, the relay on-time should be set at 4 seconds by making R_1 in the corresponding circuit 680 kilohms. □



MINUTES	0	1	2	3	4	5	6	7	8	9
SEGMENT D										
A										
SEGMENT E										
B										
C										

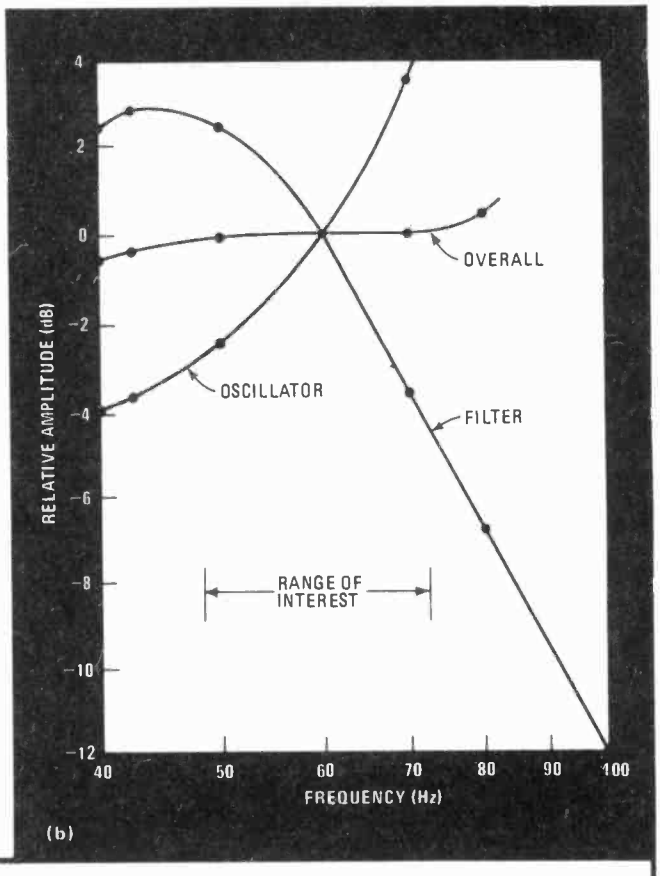
On time. Markers at 1 minute and 1 hour are derived from signals that drive segments d and e of minutes-unit and hours-unit display, respectively, in MA1012C clock module. Relay's on-time is controlled by R_1C_1. Timing diagram details operation for minute markers.

Filter levels output swing of Wien-bridge oscillators

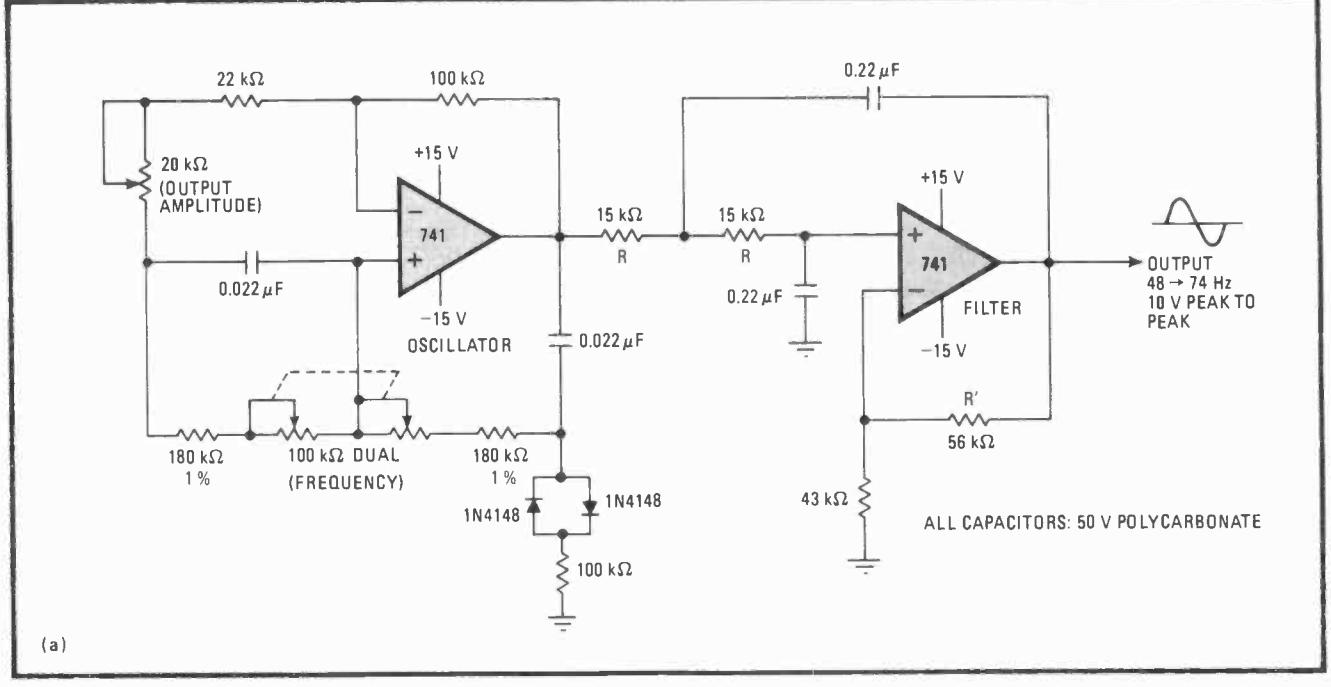
by Maxwell G. Strange
Goddard Space Flight Center, Greenbelt, Md.

Although the output of a tunable Wien-bridge oscillator normally exhibits a large change in amplitude as a function of frequency, a standard active filter will hold it to within ±0.2 decibel over a ±20% frequency range. In this application, the filter's response is set to compensate for the amplitude variation of the oscillator. Most alternative amplitude-stabilization circuits tend to draw high power, create appreciable sine-wave distortion, or stabilize slowly.

The technique can be easily implemented at any frequency over the operating range of the oscillator, since the filter's component values are easy to calculate, being inversely proportional to frequency. The circuit shown was designed to control the speed of a 60-hertz



Stability. Active filter's roll-off characteristics compensate for oscillator's inherent amplitude change with tuning, keeping output level within ±0.2 dB in range of interest. Sine-wave distortion is also dramatically reduced—from 1% at oscillator output to 0.1%.



synchronous motor over a range of 48 to 74 Hz. It is used to adjust the tape speed of a recorder in the lab to that of an airplane's recorder so that the data can be recovered from airborne equipment that lacks a frequency-regulated power source.

Two diodes and a resistor at the oscillator's output provide soft limiting in order to confine the amplitude swing of the sine wave. The signal is then passed through the low-pass filter. To flatten the output amplitude, the filter's cutoff and its damping factor, adjusted by R and R′, respectively, are set to compensate for the oscillator's amplitude variations. In general, the slope of the filter's amplitude response is made equal in magnitude but opposite in sign to that of the oscillator's response.

The graph shows the overall output to be expected compared with the individual oscillator and filter responses. In addition to amplitude compensation, the filter provides good rejection of harmonics. Third-harmonic distortion is an order of magnitude below that achieved by the oscillator alone. □

Smoke-detector chip generates long time delays

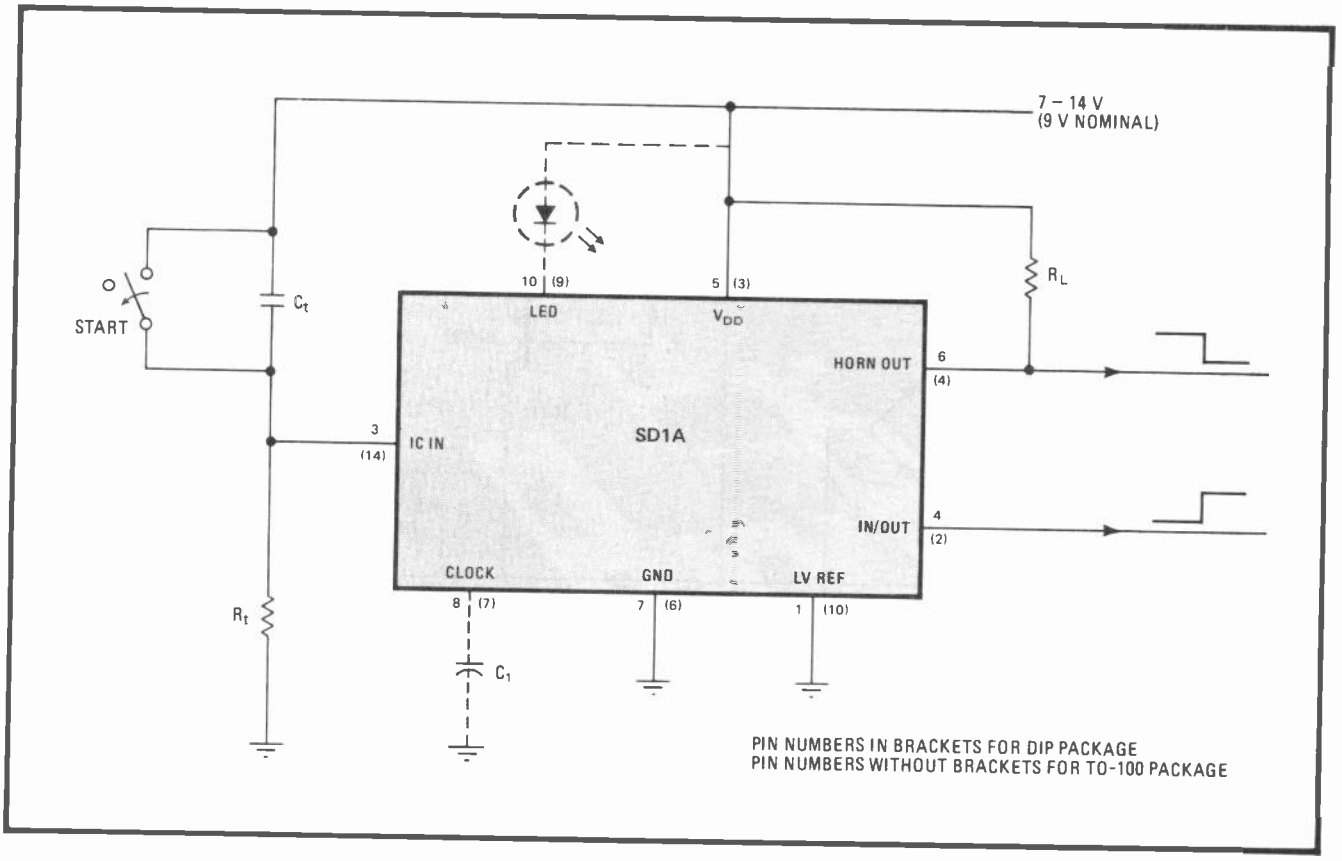
by J. Brian Dance
North Worcestershire College, Worcs., England

Long, repeatable time delays are attained with this circuit, which uses a single low-power complementary-metal-oxide-semiconductor chip usually found in smoke-detection systems. A small number of additional passive elements are used, though only three of them—the timing components and a load resistor—are actually required for operation.

Unlike more popular timers such as the 555, the Supertex SD1A can provide long time delays because it does not load down the timing components. The input impedance of its comparator input, to which the timing components are connected, is 10^{13} ohms, enabling timing resistors of up to 10^{12} Ω to be used. To avoid problems associated with capacitor leakage, however, resistor values of up to 2.5×10^{10} Ω and a 10-microfarad non-electrolytic capacitor have been used to yield time constants of 10 hours or more.

When the start switch is opened, capacitor C_t charges through resistor R_t (see figure). The timing period ends when the potential at the junction of R_t and C_t has fallen to half the supply voltage. The period is approximately $0.69R_tC_t$. This time can be varied by placing a potentiometer (50 kilohms to 50 megohms) between pin 2 (pin

A smoking timer. Special-purpose chip, for smoke detectors, can serve as one-shot, providing longer delays than popular timers, such as the 555. SD1A's input does not load timing network, enables setting of time constants to more than 10 hours. Versatile chip also has provisions for flashing LED to check chip operation during long time intervals and for sounding alarm (R_L) if battery voltage is low.



12 of the dual in-line package) and the supply.

At the end of the timing period, the voltage at the input/output port rises to $V_{DD} - 0.5$ volts. The horn output falls to near zero, serving as a current sink for the load, R_L, which may be an alarm or just a resistor. The horn output can sink at least 300 milliamperes.

A light-emitting diode connected to the appropriate port of this versatile chip can be made to flash every 40 seconds during the timed period if a 10-microfarad capacitor is connected to the clock pin. The flashing provides a useful indication that the circuit is operating during long timing periods. The frequency of the flashing is controlled by the value of C_1 or can be adjusted by connecting a potentiometer between the clock pin and V_{DD} for decreasing the period or between the clock pin and ground for increasing the period.

The SD1A also includes a circuit for sounding the alarm every 40 seconds if the supply voltage is low (below 7 V). Here the low-voltage reference pin, LV REF, has been grounded so as to disable this feature.

The cost for the SD1A is $2.50 in the TO-100 package version, and $2 in the DIP. The manufacturer does not yet have authorized distributors for the device, however, and thus at this time the SD1A can only be purchased in lots of 50 or more directly from Supertex, 1225 Bordeau Dr., Sunnyvale, Calif. 94086. □

Opto-isolated detector protects thyristors

by Charles Roudeski
Ohio University, Athens, Ohio

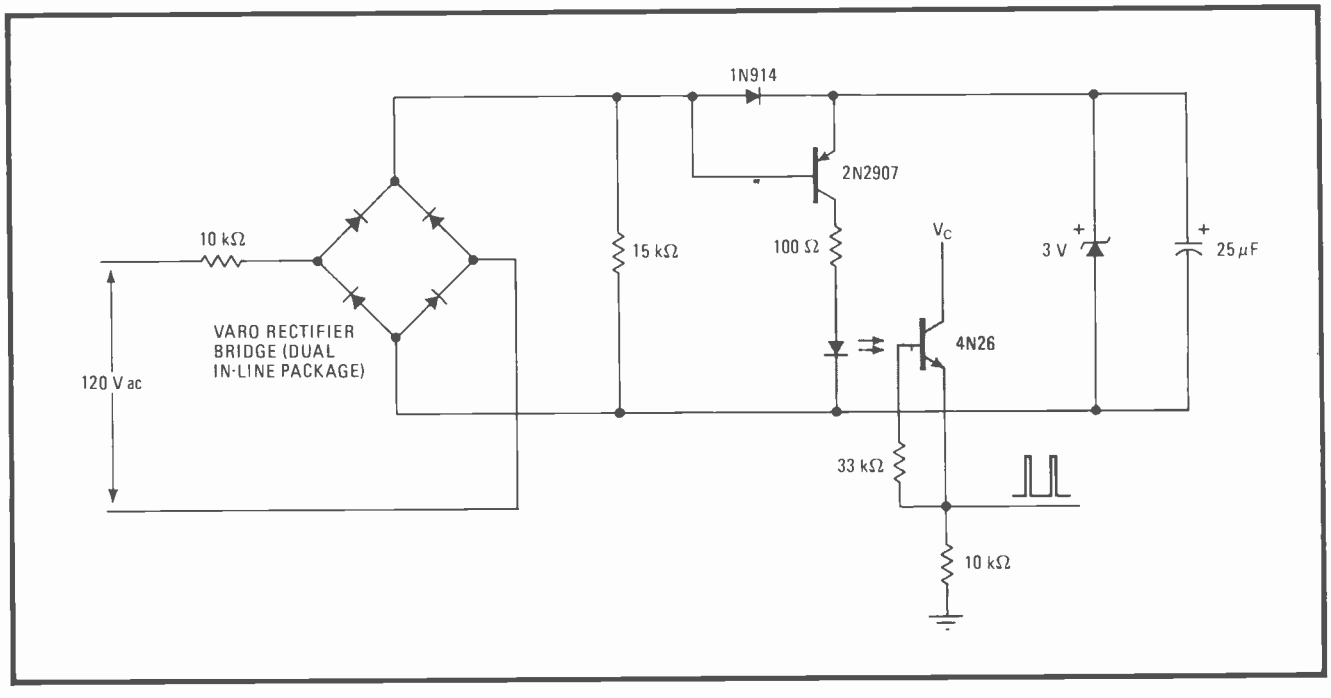
Although gating a thyristor with short pulses greatly reduces the gate and driver dissipation, failure of the driving logic can turn on the thyristor full time, possibly destroying it, the driver, and their supply. Described here is an opto-isolated zero-crossing detector that generates a 100-microsecond pulse each time its 60-hertz power-line input traverses through zero. Besides isolating for the logic element, the circuit terminates the generation of pulses if almost any detector component fails.

Most of the line voltage (see figure) is dropped across the 10-kilohm input resistor before it is rectified. The 25-microfarad capacitor charges during most of the 60-Hz cycle, but the 2N2907 transistor is held off by any full-wave rectified voltage above 2.3 V.

As the line voltage drops to about 4.5 V, the transistor begins to turn on and the capacitor discharges through the 4N26's photodiode, sourcing about 14 milliamperes. This produces a pulse centered about the zero crossing. Wider pulse widths are obtained by reducing the value of the 15-kΩ resistor. If a longer rise time is tolerable, the 33-kΩ resistor in the base lead of the optocoupler's phototransistor can be eliminated.

The 3-V zener establishes the reference voltage for the circuit. □

Protection. Zero-crossing detector uses optocoupler for gating of thyristors by power line. Output pulses, produced 120 times per second as input voltage traverses through zero, last 100 μs. Output of 4N26's phototransistor will be zero if most any element in detector fails, thereby protecting thyristor, driver, and supply from damage that would be caused by activating the thyristor continuously.



Industrial counter handles widely varying intervals

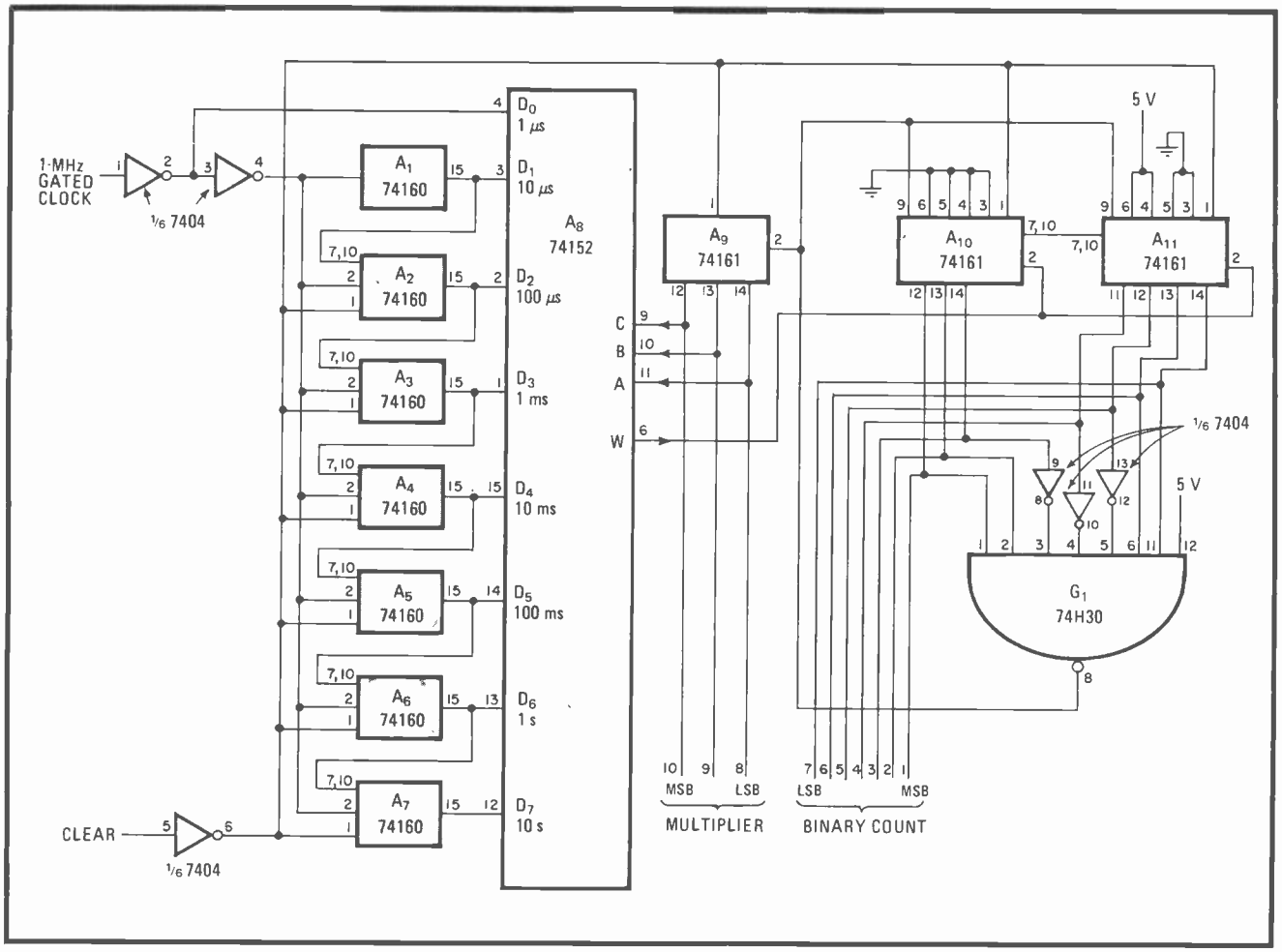
by Rudolf E. Six
The Detroit News, Electronics Department, Detroit, Mich.

The time intervals between consecutive events in industrial processes can often vary over several decades, creating a problem if their values are to be stored in a microprocessor-based system. Normally, a great many input/output ports would be needed to handle, say, the 24 significant bits needed to represent a 10-second interval measured with a 1-megahertz clock. But this counter requires only 10 output lines to represent intervals ranging from 1 microsecond to 10 seconds, making it easy for a 16-bit data system to process a 24-bit binary number.

Wiring a set of 4-bit counters, A_1–A_7, as a one-decade divider is what makes it possible for fewer lines to be used. At the start of a measurement, a string of 74160 counters immediately begin to divide down a gated 1-MHz clock signal into seven decades of time ranging from 1 microsecond to 10 seconds in duration, as shown. The outputs of A_1–A_7 are then presented to A_8, the 74152 eight-to-one multiplexer.

A_{10} and A_{11}, two 74161 binary counters, are incremented once each microsecond until their combined count reaches 99. G_1 moves low at this time. On count 100, G_1 moves high and presets A_{10}–A_{11} to a count of 10, and steps the multiplier counter A_9. A_9 enables A_8 to advance to the next decade position (D_i to D_{i+1}). A_{10}–A_{11} now counts at one tenth of the rate it did before A_8 was stepped to D_{i+1}.

The process continues until such time that the measurement interval is terminated. On the seven binary-count lines will be a binary-equivalent number that is



Line reduction. Counter that measures time interval between two events over a range of 1 microsecond to 10 seconds needs only 10 output lines to display the results and store them in a microprocessor-based system. System resolution is adequate for most applications but may be increased if an extra 74161 is cascaded with the A_{10}–A_{11} counter, at a cost of three more output lines.

related to the number of pulses in the gated clock signal. The actual (decimal-point) magnitude in microseconds, milliseconds, etc., is determined by the remaining three multiplier output lines, which indicate the decade value (D_0–D_7) as a three-bit binary number.

For example, an output of 01010001 on the binary lines combined with an output of 001 on the multiplier lines indicates a time interval of 810 μs between two events. After the computer has stored the information, a clear signal resets all the counters.

The resolution of the system (1 μs at the low edge, 10 s at the high end) is adequate for most applications, but it may be improved if an additional 74161 counter is cascaded to the A_{10}–A_{11} circuit. This extension will increase system accuracy by 1 bit, but then three additional output lines will be required. □

Three LEDs display response of null-detector circuit

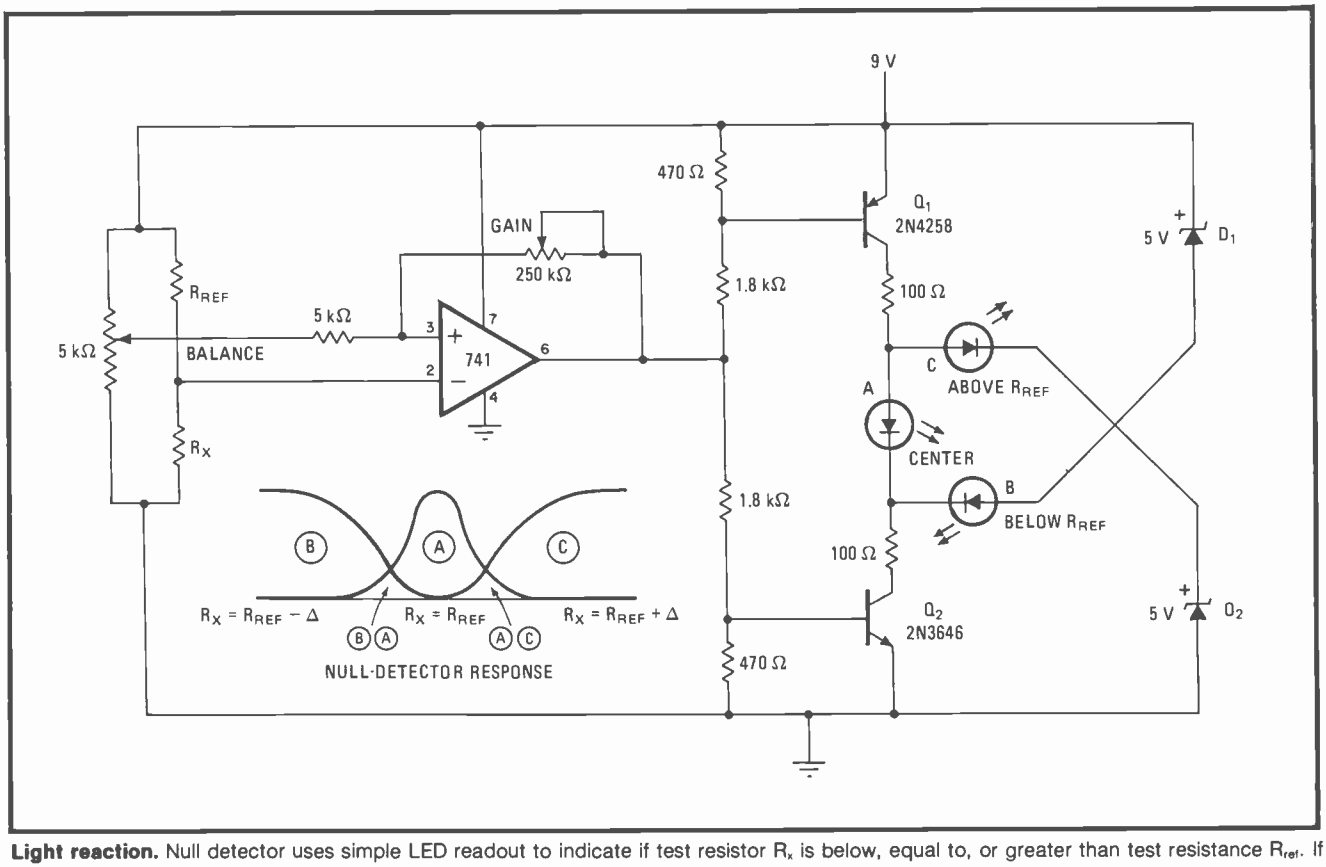
by William A. Palm
Magnetic Peripherals Inc., Minneapolis, Minn.

Three light-emitting diodes provide a visual readout for this null-detector/bridge circuit that can be used to match resistors to within 0.5%. The LED display is better suited for production-line measurement purposes than an output meter, is lower in cost, and takes up less space.

Circuit operation is straightforward. Transistors Q_1 and Q_2 will both be on when bridge resistor R_x, the resistor to be tested, is approximately equal to R_{ref}, the reference resistance, because the differential voltage at the input ports of the 741 operation amplifier is near zero. Thus the output of the 741 assumes its midrange value of 4.5 volts, and LED A turns on. At this time, the voltage dropped across A and the 100-ohm collector resistors connected to Q_1 and Q_2 ensure that D_1 and D_2 cannot conduct, and so B and C cannot light.

When the differential voltage at the inputs of the op amp increases or decreases because of a change in R_x, one transistor will turn off, and this action will divert all current through LED B or C instead, depending on the polarity of the input voltage.

The null-detector response is illustrated within the circuit diagram. Note that there is no single step-transition from one region to another, but rather two small regions where two LEDs may be on simultaneously. These regions correspond to a value of R_x that is about 0.5% to either side of R_{ref}. □



Light reaction. Null detector uses simple LED readout to indicate if test resistor R_x is below, equal to, or greater than test resistance R_{ref}. If $R_x = R_{ref}$, 741 output sits at midpoint value of 4.5 volts and LED A lights. Otherwise, output of 741 turns off one transistor, diverts current from other transistor through B or C, depending on polarity of input voltage difference. Null-detector response is illustrated.

Biaxial modulators double data-system transfer rate

by Robert J. Stetson
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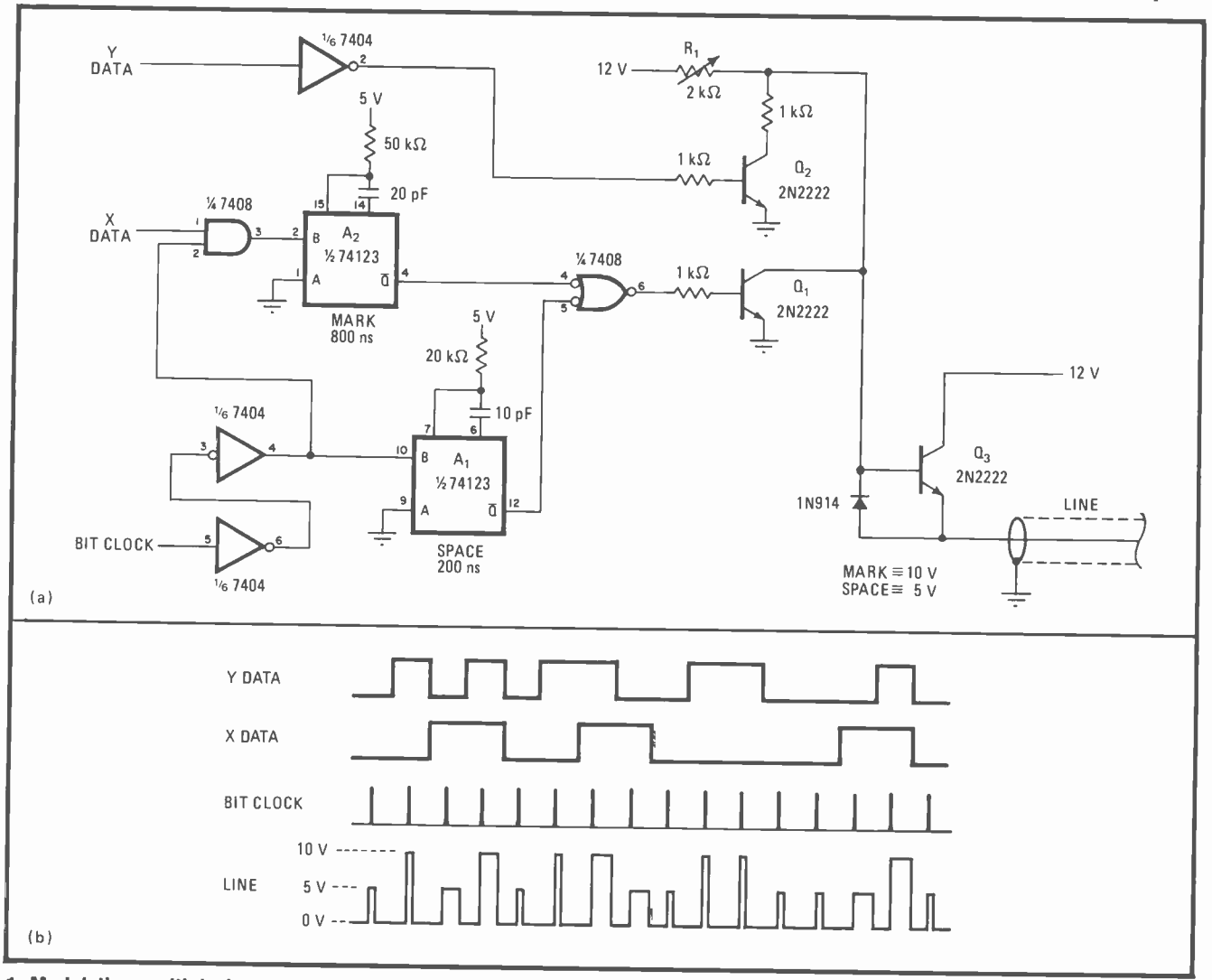
The information-handling capacity of simple data systems will be doubled if a scheme employing both pulse-width and pulse-amplitude modulation is used to multiplex data through the transmission line. More specifically, a one-cable, single-channel system can be expanded to two channels, enabling data to be sent at twice the original bit rate. Such a biaxial modulation circuit is far more economical than those using separate cables and transmitter-receivers for each channel and is less complex and costly on a per-channel basis than those using synchronous eight-channel digital multiplexers. The biaxial transmitter and receiver are simple to build.

Figure 1a shows a transmitter suitable for transferring data through a line at 4,800 bauds per channel, or 9,600 bits of data per second for two channels. The X- and Y-input data, which are non-return-to-zero (NRZ) pulse trains, operate at the same baud rate and are synchronized with the bit clock. The latter is framed at the midpoint of the data, as shown in the timing diagram (Fig. 1b).

The width of the pulse emanating from transistor Q_1 and therefore from the output line is a function of the X-input data. Q_1 normally conducts with no input signal. Generally, the bit clock periodically fires A_1, a one-shot with an on time of 200 nanoseconds, and thus a 5-volt, 200-ns pulse appears at Q_1 if X and Y are at logic 0.

When the X data is high, however, a bit clock pulse

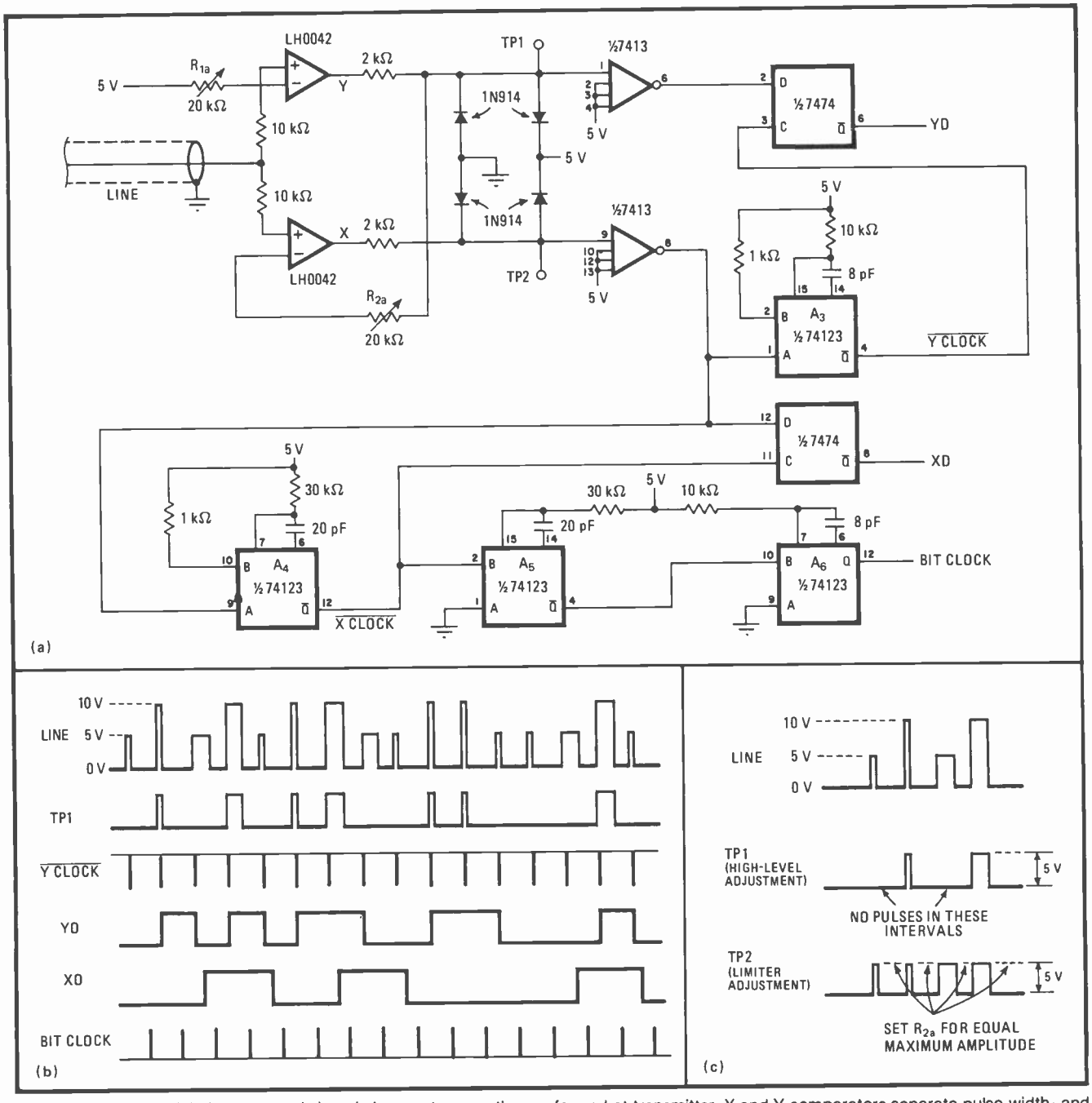


1. Modulation multiplexing. Two-mode modulation permits low-cost data multiplexing. Pulse-width modulation of X data combined with pulse-amplitude modulation of Y data doubles the capacity of one-cable systems (a). Timing diagram (b) details modulation processes.

sends A_2 high for a period of 800 ns, overriding A_1. The result is that the output of Q_1 is a pulse-width-modulated waveform having a width of 800 ns at 5 v for a logic 1 input at the X port and a pulse 200 ns wide at 5 v for a logic 0 at the X port.

The output of Q_2 and the line, on the other hand, is pulse-amplitude-modulated by data on the Y port. When the Y input is high, and X = 0, the output of the signal line will be 10 v for a period of 200 ns after the arrival of the bit clock signal. If both X and Y are high, the line output will be at 10 v for 800 ns. The four possible X-Y input combinations are summarized in the timing diagram. The PWM-PAM signal that is to be sent over cable to the receiver appears at the line output, as shown.

The line signal is first introduced to the receiver end of the system through two LH0042 precision comparators (Fig. 2a). The 10-kilohm resistors limit the input current to well below the comparators' rated maximum of 200 microamperes. The Y comparator clips the signal, so that only the 5-to-10-v portion is seen at test point 1 (TP1). Note that the Y data is demodulated but not yet in the form it was originally at the transmitter, that is, reconstructed. The diode bridge at the input of the 7413s serves as a combination limiter and zero-crossover network to aid in signal recovery. The output of one 7413 fires the 74123 one-shot, A_3, producing the $\overline{Y}$



2. Recovery. Demodulation process is largely inverse to operation performed at transmitter. X and Y comparators separate pulse-width- and pulse-amplitude-modulated signals, generate XD and YD with aid of several one-shots and flip-flops (a). Timing diagram (b) aids in understanding the circuit's reconstruction operation. Two circuit adjustments optimize receiver performance (c).

$\overline{\text{CLOCK}}$ signal to regenerate the Y data (YD).

The PWM portion of the receiver derives its signal from the X-data input component. The line signal is applied to the D input of the 7474 to generate the XD signal. The 7474 is also clocked by the same input signal through the 74123 one-shot, A_4, on the positive edge of each output pulse of the $\overline{\text{X CLOCK}}$.

The positive-going edge of the $\overline{\text{X CLOCK}}$ signal occurs 400 to 600 ns after A_4 fires. If the line-input signal is a logic 0 (200 ns wide), a space will be clocked in at the D input of the 7474 storing the XD data. If, on the other hand, the X input is at a logic 1 (800 ns wide), a mark will be clocked through, since the X pulse will still be present on the arrival of the $\overline{\text{X CLOCK}}$ signal. The trailing edge of $\overline{\text{X CLOCK}}$ also fires A_5 and A_6, two monostable multivibrators, for 400 to 600 ns. This enables the bit clock signal, which originated at the transmitter, to be recovered also, as shown in the timing diagram (Fig. 2b).

To set up the most efficient circuit, a scope is required. Also, the X and Y data inputs should be initially tied to ground at the transmitter. The scope should then be connected to the signal line cable and R_1 adjusted for a peak amplitude of 5 v. After a logic 1 is applied to the Y input, the signal line pulses should rise to at least 10 v.

At the receiver end, the scope should be connected to TP1 and R_{1a} adjusted as seen in Fig. 2c. Next, the scope should be connected to TP2 and R_{2a} adjusted as shown. A slight shift between the X and Y data output will occur, basically because of the internal-timing method used to recover the data. The output data will otherwise be a replica of the original information transmitted. □

Go/no-go tester checks optocoupler's transfer ratio

by S. Ashok
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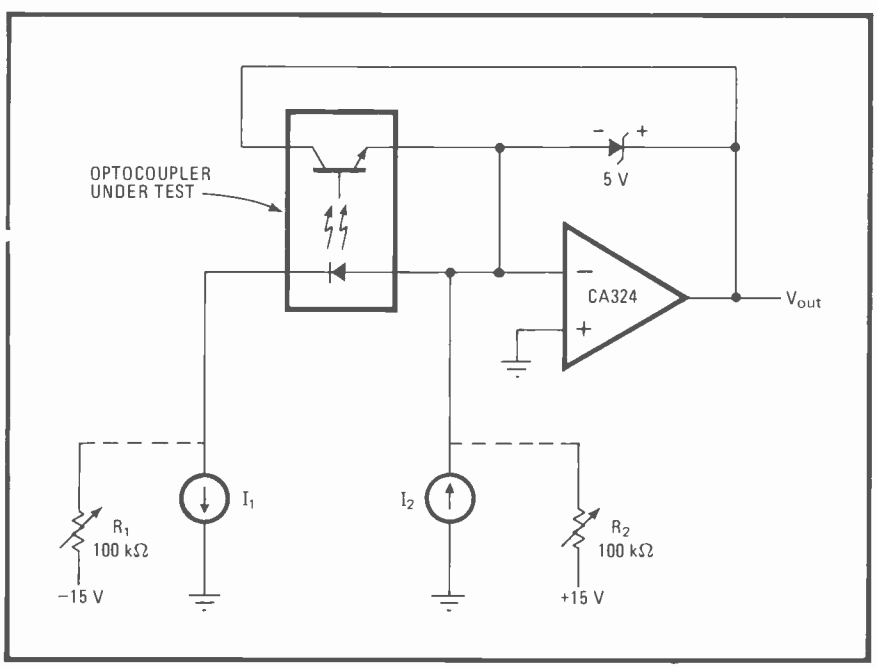
This extremely simple circuit performs a go/no-go test on the quality of an optocoupler. Here, an operational amplifier and a zener diode are used to determine if the most fundamental parameter of the optocoupler, its forward current-transfer ratio, α (which is the ratio of the phototransistor's output current to the photodiode input current), is greater or less than a preset value.

The operation of the circuit is based on the principle that the phototransistor tends to saturate if the current forced into its collector lead is less than α_i, where i is the photodiode current, and that it tends toward avalanche breakdown if the current is higher than that amount. The forced current is $(I_1 - I_2)$, where I_1 and I_2 are current sources. The preset value of α corresponding to these currents will thus be $(I_1 - I_2)/I_1$. Adequate current sources for I_1 and I_2 can be implemented by using variable resistors returned to +15- and −15-volt supplies as shown in the figure.

Typically, the phototransistor breakdown voltage is greater than 5 v, so that if the value of α is lower than the preset figure (bad optocoupler), the current into the zener-transistor combination will be greater than α_i, the 5-v zener will break down, and V_{out} will then go to 5 v (logic 1). If on the other hand, α is higher than the preset value (good optocoupler), the phototransistor will saturate and there will be a logic 0 at the output.

Note that the polarity of I_2 should be reversed if optocouplers with Darlington outputs are tested, because Darlington circuits have an α that is greater than unity.



Light test. Op amp and zener diode check optocoupler quality by determining if its forward current-transfer ratio, α, is above or below preset value. If α is above value set by current sources I_1 and I_2, phototransistor saturates and $V_{out} = 0$, indicating good element. Otherwise, the zener breaks down, and $V_{out} = 5$, indicating bad device.

Low-level-light detector checks optical cables fast

by Edward W. Rummel
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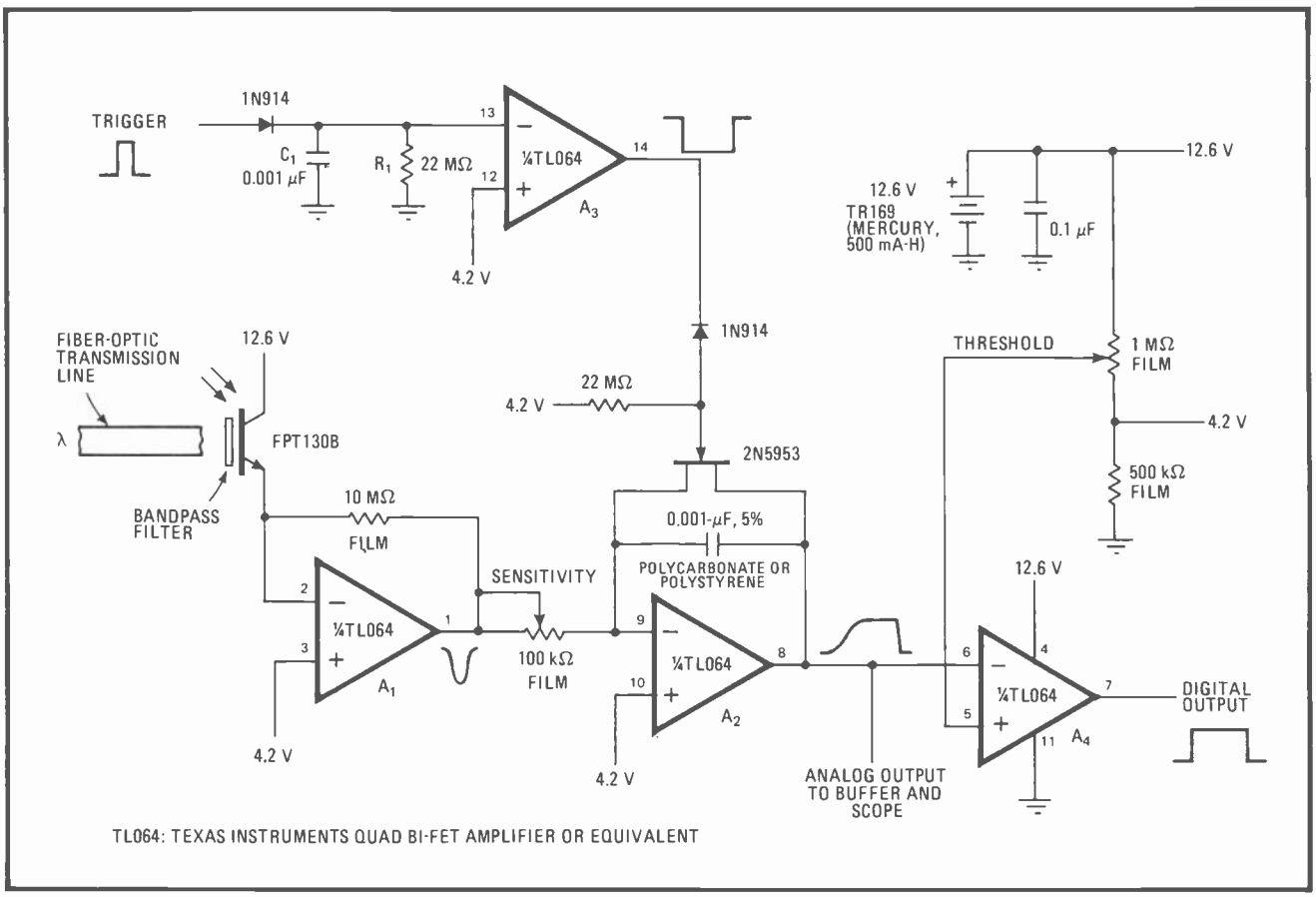
A standard phototransistor and a quad operational amplifier can be used as a total-energy detector of pulsed-light signals that propagate through fiber-optic communications systems. Such a circuit is especially useful for checking and comparing the condition of long fibers when the light intensity at the source is kept constant. Alternatively, it may detect changes in light intensity or pulse widths with a given fiber.

Current from the Fairchild FPT130B phototransistor drives A_1, a bipolar–field-effect-transistor op amp that serves as a current-to-voltage converter with an extremely high input impedance (see figure). The phototransistor has high sensitivity and a low dark current—only 10 nanoamperes flows for zero radiant-input flux. It has been given a flat lens to facilitate the addition of fiber-optic couplers, spectral band-pass filters, and so on.

This input configuration enables the circuit to give a linear response to light levels ranging from 100 to 10,000 ergs per square centimeter, provided each pulse in a given train has a width of no less than 10 microseconds. The phototransistor's low parasitic capacitances contribute to the high response speed of the circuit. The low input bias current (0.4 nanoampere) and high slew rate (3.5 volts per microsecond) of A_1 and subsequent bi-FET amplifiers also contribute to the speed and accuracy. The 100-kilohm trimming resistor at the output of A_1 is provided to eliminate the variations in sensitivity caused by the 2:1 gain spread of the combination of the phototransistor and the optical components.

A_2 is a standard RC integrator that produces a voltage directly proportional to the total light energy received. As both A_1 and A_2 operate in the inverting mode and are on the same bi-FET chip, offset voltages appearing at the output of A_1 are virtually canceled by the input offset voltage of A_2. The cascade connection of A_1 and A_2 shown also allows a high degree of freedom in the choice of source voltages for the circuit.

The low input-bias current of the bi-FET amplifiers makes it feasible to use low-value, and hence low-cost,



Light monitor. Phototransistor and bi-FET op amps form $5 light detector useful for checking optical communications systems. Circuit responds linearly to light levels in the range of 100 to 10,000 erg/cm². Circuit runs for 500 hours from a 12.6-V mercury battery.

polycarbonate capacitors. The low leakage of these capacitors preserves system accuracy. In order to limit long-term integration errors that are introduced by ambient and steady-state light or by dark-current and bias-current leakage, A_2 must be held in the reset mode by the n-channel junction FET, whose gate is connected to A_3 through a diode. Therefore, the input signal cannot be sampled continuously. The integrator is activated by applying a trigger to the JFET through A_3. A_3 stretches the trigger pulse with the R_1C_1 integrator. With the circuit values as shown, a 10-millisecond integration time will be generated from a 10-microsecond pulse.

A_2's output may be observed directly, or it can be compared to a fixed level (go/no-go indicator) through the use of A_4. The low bias current in bi-FET amplifier A_4 enables the use of a low-current resistive divider network for establishing bias and threshold levels. This in turn keeps the circuit's operating current low, enabling the circuit to work for 500 hours on a small 12.6-volt battery.

The output duration at A_4 is approximately equal to the duration of the pulse stretcher minus the time taken by the integrator to reach A_4's threshold level. The input to A_3 and the output A_4 can be made compatible with complementary-metal-oxide-semiconductor logic-level requirements by proper choice of supply voltage. □

Pilot-lamp controller stabilizes crystal oven

by Dwight D. Brown
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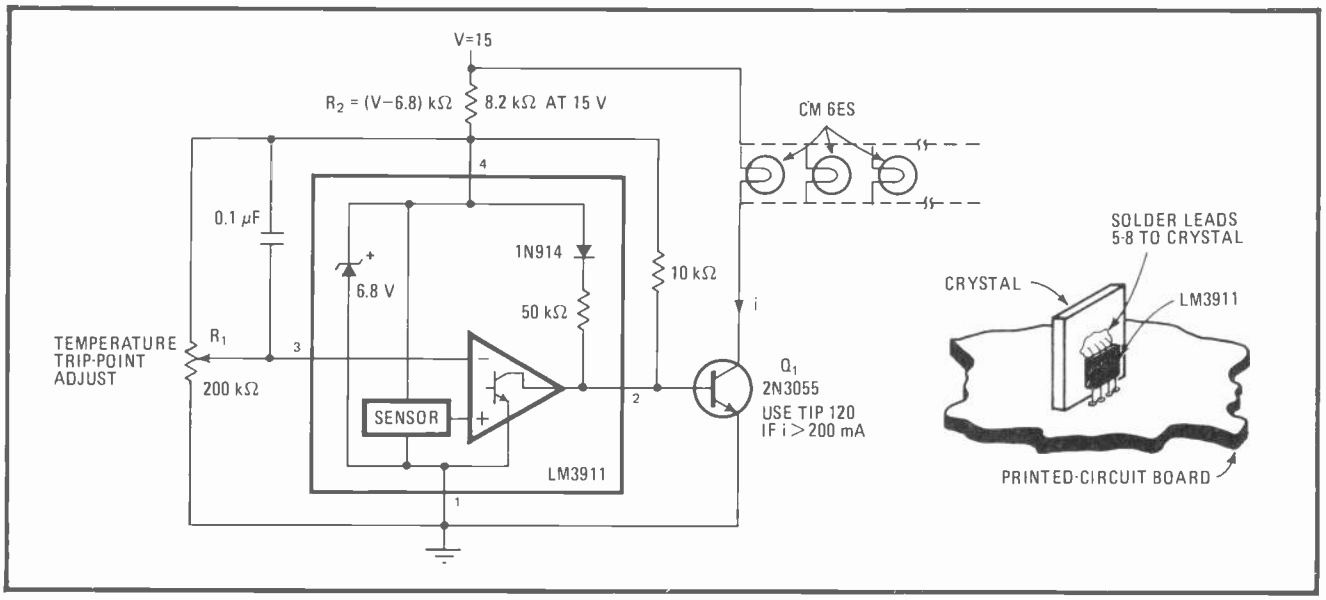
Crystal oscillators and phase-locked loops often need a temperature oven to retain maximum frequency stability, but the ones available are either expensive or use special components not readily at hand. The oven (left, below), however, uses low-cost parts such as standard pilot lamps for the heater elements and a one-chip control and sensing circuit that can maintain the temperature to within 0.5°C of the set value. The oven can be built for $7 or $8, the major cash outlay being for the oven's enclosure.

The LM3911 temperature controller is the heart of the circuit. It contains a temperature sensor, a stable voltage reference, and an operational amplifier. The sensor, which exhibits a temperature change of 10 millivolts per degree kelvin, is connected directly to the noninverting input of the op amp. Its output voltage is compared with the voltage set externally by the temperature trip-point potentiometer, R_1.

If the oven temperature increases above the trip point, the voltage from the op amp begins to fall. Consequently, the current emanating from transistor Q_1 decreases, and so does the pilot lights' filament current. Current continues to decrease until the oven temperature falls sufficiently to be detected by the sensor. At that time, the voltage at the noninverting port of the op amp falls, op-amp output voltage increases, and filament current increases. The process is continuous.

The LM3911 provides sufficient base-current drive for a transistor with modest gain, such as the 2N3055. This transistor will drive four Chicago Miniature 6ES lamps. If more lamps or lamps with a higher current are required for generating high oven temperatures, Q_1 should be replaced with a Darlington-pair npn power transistor, such as the TIP20.

When two lamps are used, the circuit can be set to an



Light adjustment. Crystal oven uses low-cost pilot lamps for heat source, $2 integrated-circuit temperature controller (left). Current through lamps, and thus temperature generated, is a function of the actual oven temperature and the temperature set by read: R_1. Temperature-critical elements of crystal oscillator should be placed close to LM3911 (right). Unused pins of LM3911 are soldered directly to crystal holder.

oven temperature between 22°C and 43°C, for a 1.5-by-2-by-3-inch enclosure and an outside temperature of 20°C or more. Stable operation is reached in less than 10 minutes from a cold start. For each additional lamp in the circuit, the oven temperature will increase a maximum of 10°C or so.

The most temperature-critical circuit elements should be placed close to the LM3911, near the center of the oven housing. If a crystal oscillator is housed, it should be in direct contact with the LM3911. The temperature controller is available in several package types. In all cases, pins 1 through 4 are used to make circuit connections. If the eight-pin, dual in-line package is the one employed, unused pins 5 through 8 should be soldered directly to the crystal holder, as shown in (b).

Almost any material may be used for the oven enclosure. However, the inside surface of the selected case should be covered with asbestos or some other insulating material. A 1/16-inch-thick layer of the insulating material, glued to the inside of the cover, will suffice.

The component values shown in the circuit assume a 15-v supply voltage, but other voltages can be used by changing the value of R_2 to equal $(V-6.8)$ kilohms. The pilot lamps should have an operating voltage slightly below the supply voltage used. □

Tester determines solar cell's sunlight-gathering efficiency

by Sudarshan Sarpangal
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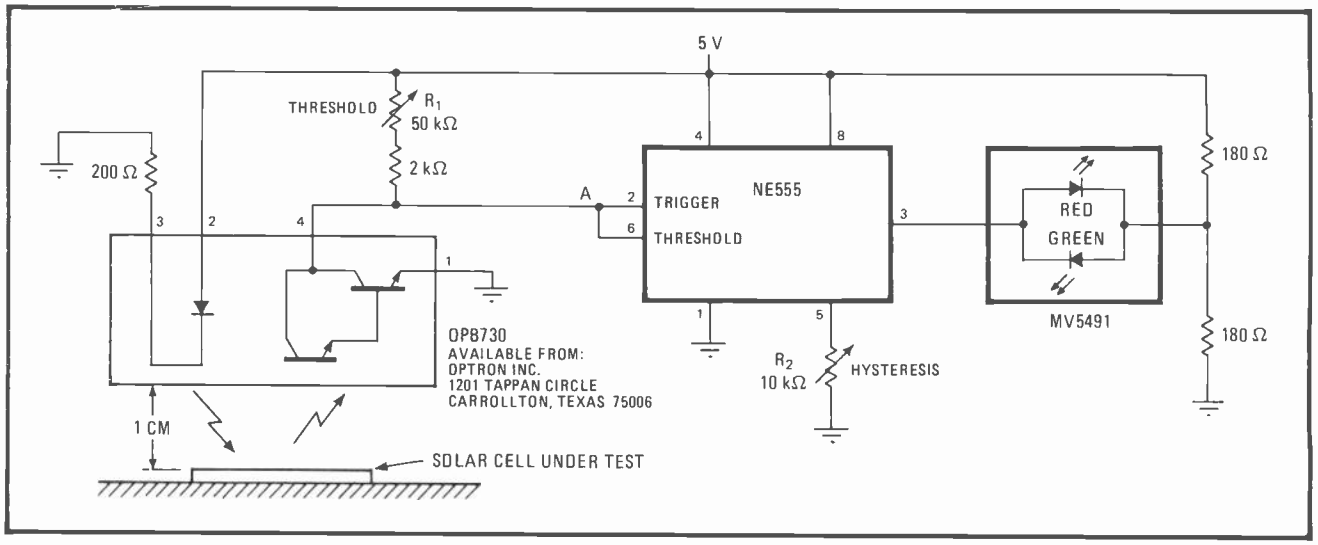
The low-cost circuit shown in the figure performs a go/no-go test on the light-gathering efficiency of solar cells by checking the quality of its antireflection coating. A light-reflective transducer, a universal timer, and a dual light-emitting-diode package form the checker, which can be useful in production-line testing.

The overall conversion efficiency of a solar cell is directly proportional to the amount of sunlight converted to electricity, which in turn is equal to $K(1-R)$, where K is a constant and R is the reflectivity factor of the cell's antireflection coating. R can be expected to lie in the range 0.015 to 0.03 for space applications. An R equal to 0.05 would be considered undesirable.

In this circuit, the reflective transducer (OPB730), which is actually an infrared photodiode transmitter and a photo-Darlington transistor receiver, discovers whether the value of R exceeds preset limits. Then it uses the 555 timer and the red-green light-emitting diode array to display the results.

The OPB730 should be placed 1 centimeter from the cell's antireflection surface. Both should be contained in a test fixture that shields them against external light.

Part of the infrared energy emitted by the optical device will be reflected by the solar cell's coating, which is very often titanium, zirconium, or cerium dioxide, (TiO_2, ZrO_2, or CeO_2, respectively), and this reflected energy will be detected by the photo-Darlington transistor in the receiver. If the antireflection coating is of relatively high quality (little reflection), the voltage at point A will climb above the preset limit set by R_1, and the output of the 555, which is configured as a Schmitt trigger, will go low. Then the green LED will glow, indicating a good solar cell. If the antireflection coating is substandard (high R), the output voltage from the photo-Darlington output of the receiver will be relatively low. If the voltage is below the preset limit, pin 3 of the timer will go high and turn the red LED on. □



Light work. Circuit performs qualitative check of solar cell's efficiency by determining if relative value of its antireflection coating exceeds preset limits. R_1 sets limits, R_2 controls hysteresis in 555 timer, which operates as Schmitt trigger. If coating is of relatively high quality, Schmitt trigger moves low, lighting green LED. Otherwise, output voltage from OPB730 will be low, and red LED will glow. Circuit cost is under $10.

Interfacing an auto-ranging DVM to a microprocessor

by Steve Hui and John Richartz
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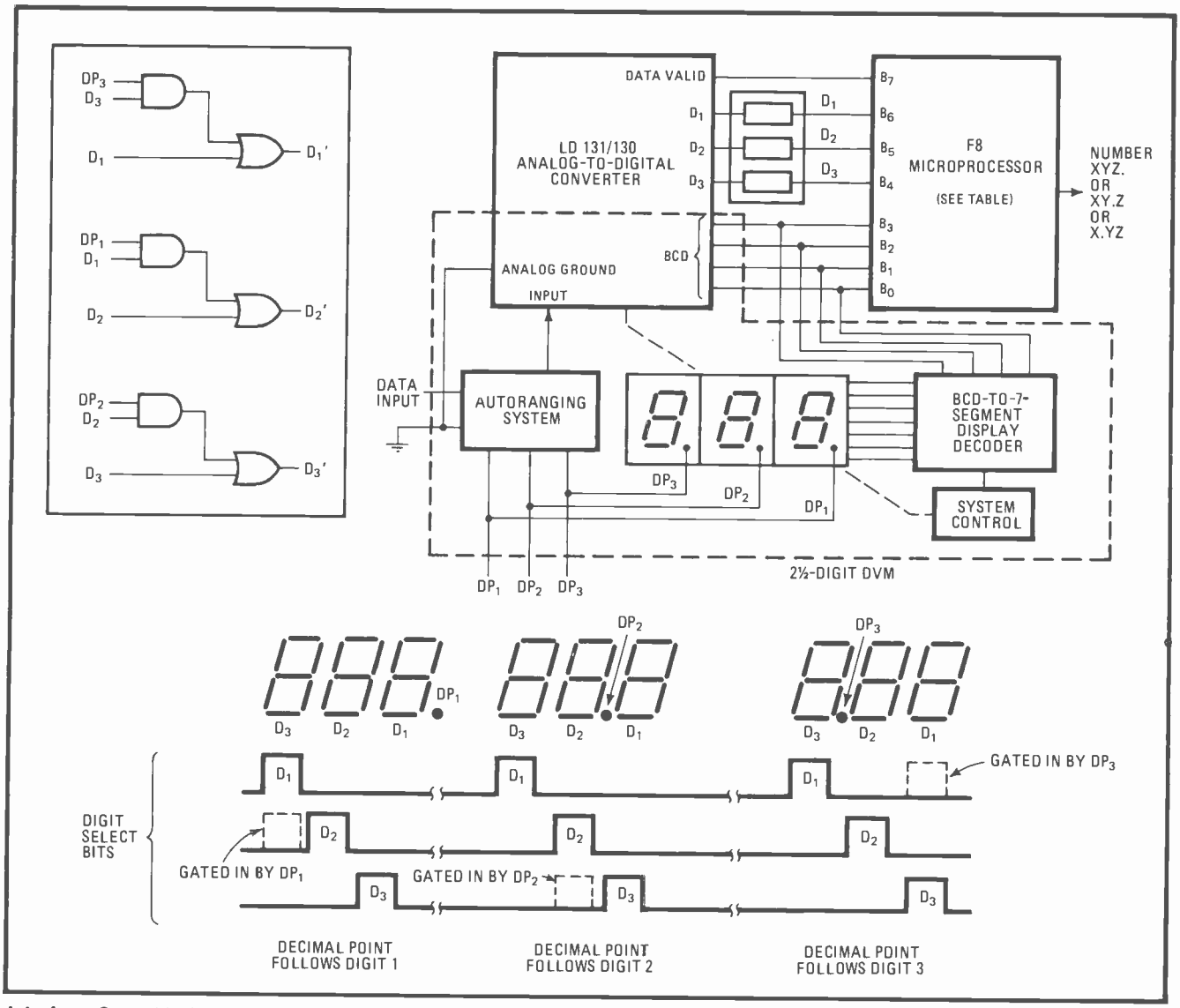
Several logic gates and a few bytes of instructions provide all the hardware and software needed for building an interface between an auto-ranging digital voltmeter and a microprocessor. This circuit enables an 8-bit processor to read the magnitude of any voltage measured by a 2½-digit DVM. The accompanying decimal-point information contained in the input data is recovered with a combination of AND and OR gates and a simple program.

The hardware portion of the system is shown in the figure. The auto-ranging DVM circuit contained within the dotted line is a standard data system. Generally, any data introduced to the DVM is first converted by the LD131 analog-to-digital converter into binary-coded-decimal form, one digit at a time, in order to drive the display decoder and thus the numeric displays. The decimal-point data is introduced into the displays directly by means of lines DP_1–DP_3.

However, when the F8 8-bit microprocessor reads any data generated by such a system, the decimal-location information cannot be directly introduced into it because



Interface. Several logic gates and small program will unite auto-ranging DVM to microprocessor. Decimal-point information is recovered at output of F8 by connecting each digit-select line (D_1–D_3) of a-d converter to two port bits of F8 through AND-OR gate interface, and by using simple software to detect resultant conditions shown in timing diagram. A storage scope helps check the digits' movement through the circuit.

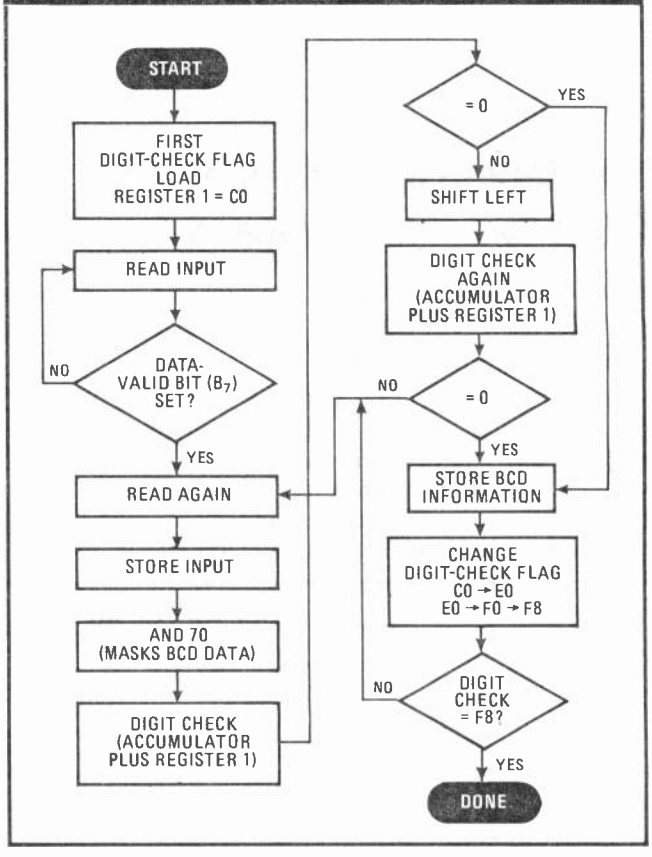
there are too few input ports available. An obvious solution might be to use a 16-bit microprocessor, but this is not efficient, either from a device-cost or a programming standpoint.

But although decimal-point data cannot be placed on the BCD data lines (B_0–B_3) of the F8, the information may be placed on lines B_4–B_6. B_4–B_6 would otherwise perform their single function—accepting command data from the LD131's digit-select lines (D_1–D_3), which enables the processor to read the digits in sequence. Now, however, each digit-select line with a gated-in decimal-point signal is coupled to two ports on the F8, not just one as before, in the manner apparent from the module (see left of figure). This hardware connection enables a simple program to be written for the F8 that will separate the digit-data from the decimal-point data.

As indicated by the timing diagram, if the decimal point occurs after the least significant bit (digit 1), lines D_1 and D_2 assume a logic 1 state during the digit-1 time interval; if the decimal point occurs after digit 2, lines D_2 and D_3 move to logic 1 during the digit-2 interval; if after digit 3, lines D_1 and D_3 go high. In other words, if the decimal point occurs after digit i, then lines, d_i and d_{i+1} move high at the same time (for $i = 3, i+1 = 1$).

The software should be written so as to easily recognize the unique output condition for each decimal point location as described above. It can do so by performing several rapid comparisons of the data lines, to determine which of them are simultaneously high. The flow chart given in the table outlines the algorithm used. □

FLOWCHART: DVM-TO-MICROPROCESSOR INTERFACE



Waveform integrator averages over variable elapsed times

by Ron Vogel
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Finding the long-term average voltage of a waveform is much more difficult when the signal averaging must be done over a variable rather than a fixed time. But the average value of any signal sampled over an interval of 1 minute to 2 hours can be found easily with this circuit, which performs the task with the aid of an integrator-oscillator, an up-down counter, and a digital-to-analog converter. The basic transfer function relating output voltage V_o to input voltage V_{in} at time t:

$$V_o = \frac{1}{t}\int_0^t V_{in}(t)dt \qquad (1)$$

is generated when feedback is implemented and when circuit constants are selected with care.

For the circuit to perform integration, a simple feedback loop is required. A voltage-controlled oscillator is used to drive an up-down counter in this circuit, and the counter, in turn, has an effect on the VCO frequency. The frequency of the VCO is determined by V_{in} and reference voltage V_{ref}. The oscillator is so configured that its output frequency (point A) is:

$$f_o = \frac{K_1 V_{in}}{V_{ref}} = \frac{K_1 (V_{in} - V_{out})}{V_{ref}} \qquad (2)$$

where K_1 is a constant. Thus the up-down counter increments at a rate of f_o when V_{in} is positive and decrements at the same rate when V_{in} is negative.

The contents of the counter at any time t is therefore:

$$B = \int_0^t f_o dt = K_1 \int_0^t \frac{V_{in} - V_o}{V_{ref}} \qquad (3)$$

Now, the ramp- and output-voltage equations are:

$$V_{ref} = K_2 t \qquad (4)$$

$$V_o = K_3 B \qquad (5)$$

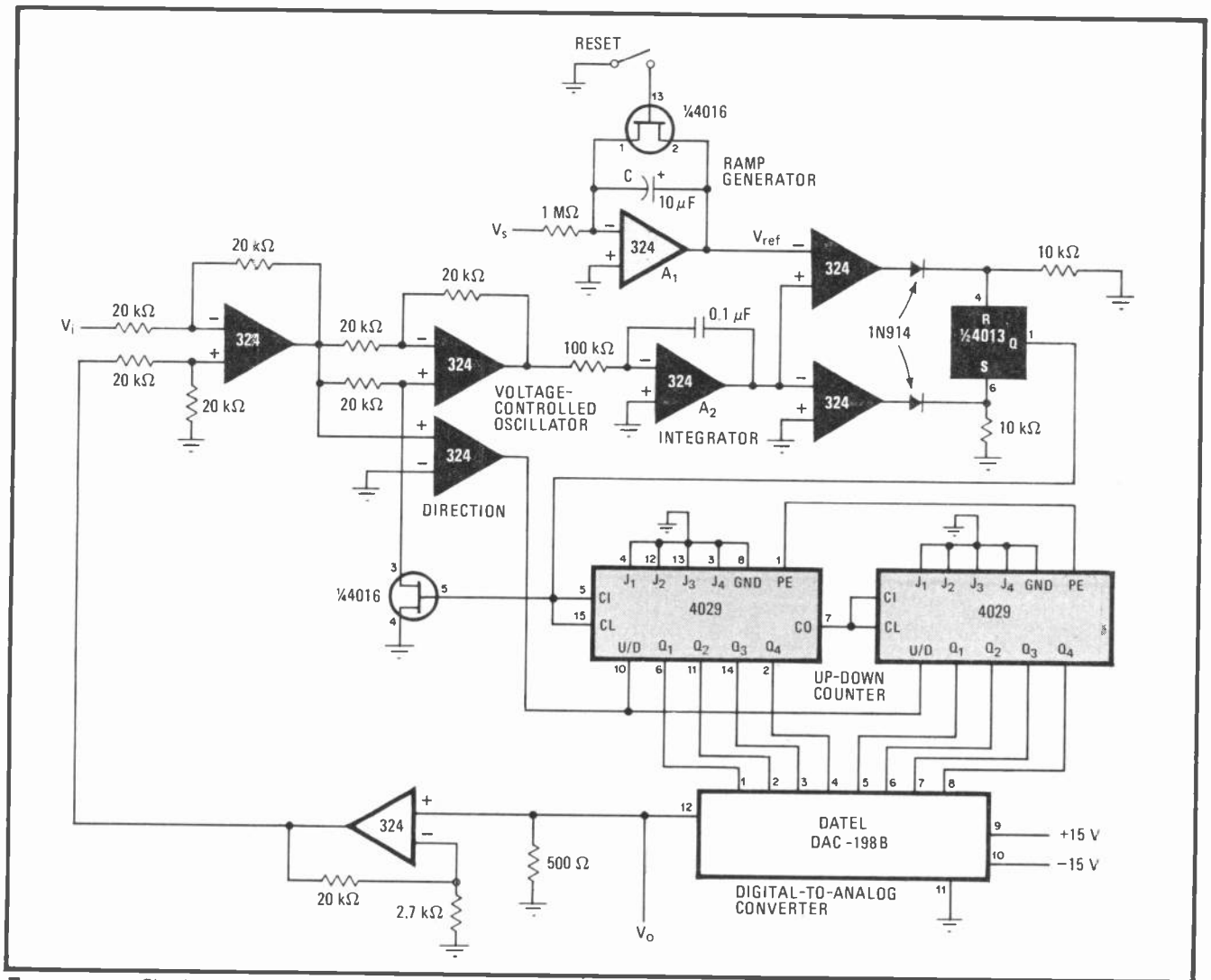
where K_2 and K_3 are, respectively, the initial amplitude of the ramp and the proportionality constant of the d-a converter.

When Eq. 4 is substituted into Eq. 3 and thence into Eq. 5, and when circuit constants are selected so that $K_1 K_3 = K_2$, then:

$$V_o = \int \frac{V_{in} - V_o}{t} dt \qquad (6)$$

Differentiating and rearranging this equation yields:

$$V_o + t\frac{dV_o}{dt} \equiv \frac{d}{dt}(V_o t) = V_{in} \qquad (7)$$



True average. Circuit finds average voltage of waveforms sampled over interval of 1 minute to 2 hours. Averaging time is determined by C. Averaged voltage is in digital form at the output of the up-down counter, in analog form at the output of the d-a converter.

and this equation reduces to Eq. 1 when integrated.

The actual circuit uses all standard components. The ramp generator (A_1) is a standard integrator circuit, which is reset at the start of a timing interval. In this application, however, the integrator requires a low-leakage integrating capacitor. A maximum integration time of 1 hour can be achieved with a 10-microfarad capacitor and an integrator input voltage of 0.03 volt.

The voltage-controlled oscillator is somewhat unusual. Any input voltage, positive or negative, will cause integrator A_2 to ramp in the positive direction starting from the initial V_{in} potential and will also drive the 4013 flip-flop high. The logic 1 generated at the Q output will increment or decrement the counter. When the ramp voltage from A_2 reaches V_{ref}, the flip-flop will be reset, generating a feedback voltage that causes A_2 to ramp in the negative direction at the same rate it rose. When the ramp reaches ground potential, A_2 prepares to integrate V_{in} once more. The instantaneous value of V_{in} is again introduced into the integrator, and the process is repeated until the ramp generated by A_2 fails to reach the signal produced by A_1, which is slowly rising toward the positive supply voltage; this will be recognized as the end of the sampling interval. The contents of the 4029 counter or Datel 198B d-a converter can, of course, be observed at any time. The averaged voltage will be in digital form at the output of the counter or may be obtained in analog form at the output of the d-a converter.

In practice, the minimum value of V_{ref} should always be above ground potential. The lower limit, in general, will be determined by the response time and frequency capability of the particular VCO used. The ramp slope can then be selected so that V_{ref} will be less than the supply voltage for the longest averaging time expected. Of course, since V_{ref} cannot start from zero, an error will be observed at the output when the analog signal is first processed (that is, for small values of t).

The highest frequency at which the VCO can cycle is 10 kilohertz. At this rate, the maximum measurement error will be 1% after 2 minutes if the maximum averaging time is 1 hour. Accuracy will improve with time and will be directly proportional to the VCO frequency. □

Digital sample-and-hold speeds a-d conversion time

by T. L. Sterling
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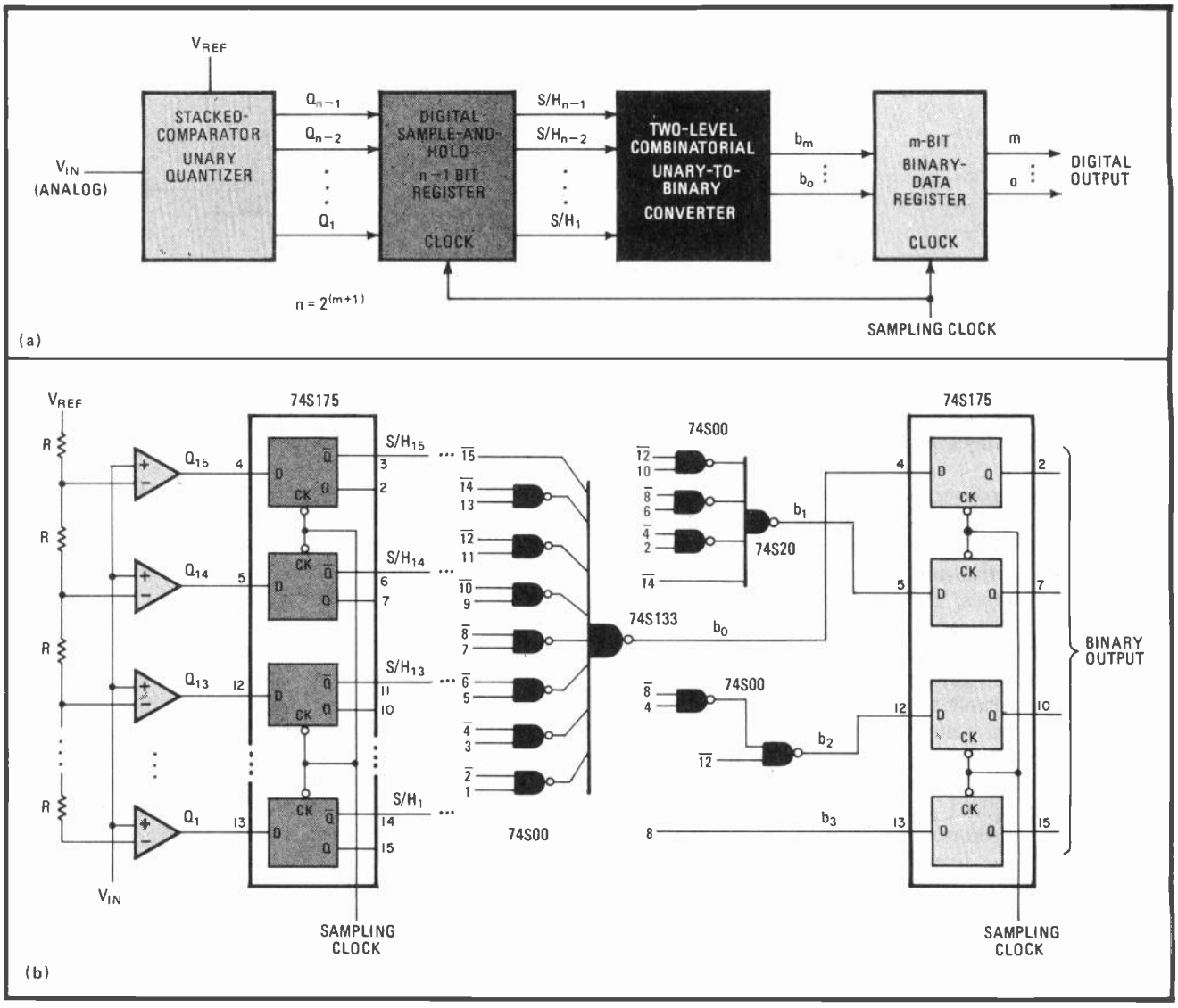
A set of comparators and latches serves as the sample-and-hold quantizer for this analog-to-digital converter. As a consequence, the circuit offers a faster conversion time than those converters using standard, relatively slow and expensive sample-and-hold units that work on the principle of storing a sampled voltage on a capacitor.

In this circuit, the analog signals are immediately transformed into a digital signal by the comparators, then stored by the latches, and finally converted into binary form with combinational logic. This scheme saves the extra time required by a counting-type encoder to change the analog signal to its binary equivalent.

This stacked-comparator technique, as it is called, is especially convenient in high-speed, small-word applications, where it provides reasonable accuracy. The overall system is shown in (a), with the actual circuitry for a 4-bit a-d converter shown in (b).

The comparators convert an analog-input signal into a digital signal with a resolution proportional to the number of threshold voltages in the comparator circuit. The output line of any comparator will move high when



Jammed pipeline Analog-to-digital converter (a) that uses comparators and latches for sample-and-hold quantizer can perform fast conversions at relatively low cost. Comparators and latches perform parallel, or jam, transfer of unary (base-1) data (b) as previous sample is processed by output register (pipeline operation). Unary-to-binary converter uses combinational logic.

the analog signal amplitude exceeds its associated threshold voltage.

The cumulative output of the 15 comparators is a unary (base-1) representation of the quantized signal. As the input signal varies, only one output line can change at any one instant. This setup provides a maximum error of one digit when sampled, which is equivalent to an error of one least significant digit of a binary-signal representation. Furthermore, because the output of the quantizer closely tracks the analog input (the delays are slight and constant for each comparator), it is possible to simultaneously sample the output of all comparators using digital storage elements. The sampling and storage of data are provided by a high-speed clock and a set of 74S175 high-speed latches, respectively. One flip-flop is required for each output line that is sampled.

The unary data stored in the latches is converted to a binary-equivalent number with the aid of combinational logic and stored in the output register. The numbers at the input to each gate refer to the inverted (or noninverted) outputs of the sample-and-hold flip-flops. Both sets of latches are loaded simultaneously. This is a serial, or pipeline, configuration, but no time is lost in processing one sample at a time, because the input and output latches process two consecutive samples, n+1 and n, respectively, independently of each other.

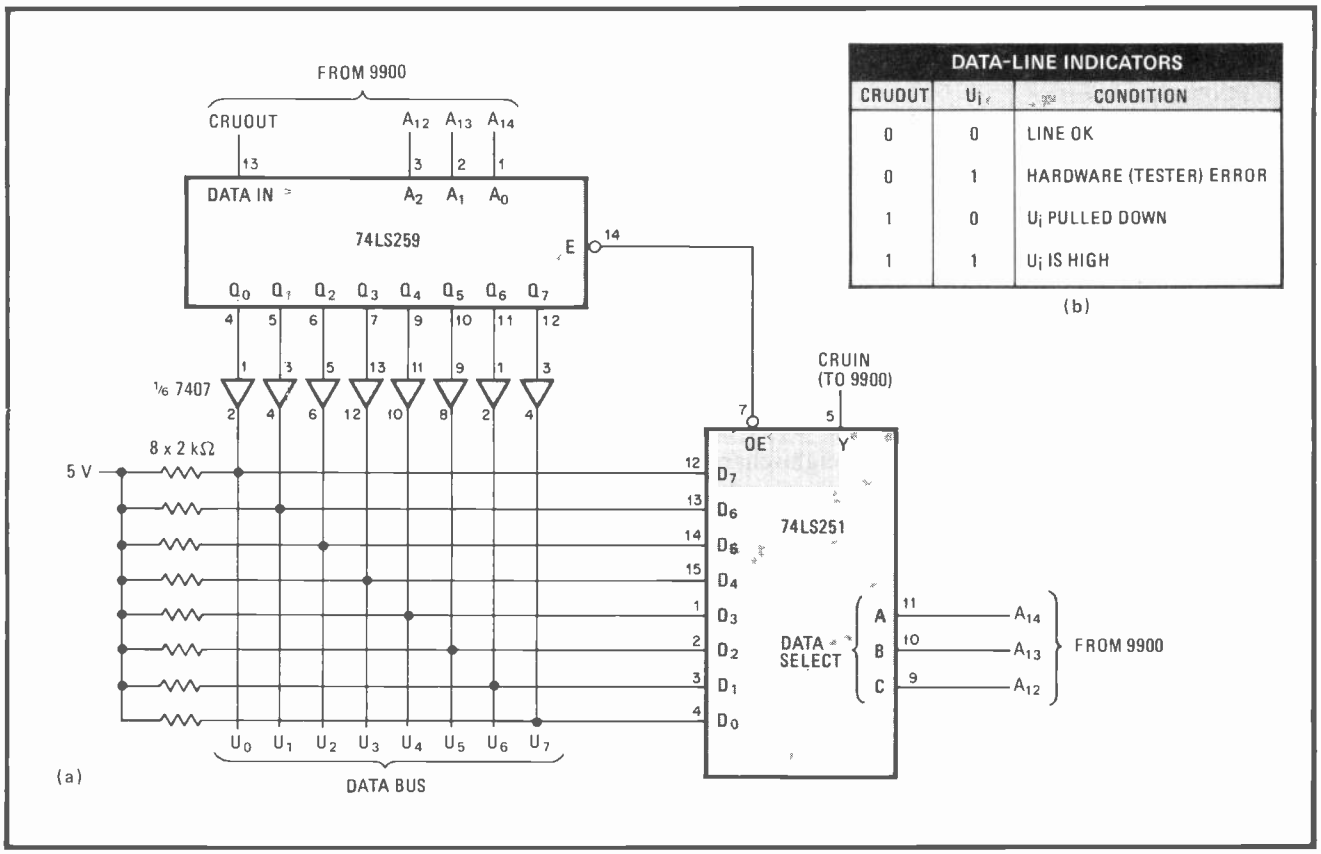
The sample rate is limited by the propagation delay of the two registers and the unary-to-binary converter. For the devices shown, a typical clock rate is 40 nanoseconds plus the delays imposed by circuit-layout capacitance. □

9900 simplifies design of bidirectional I/O module

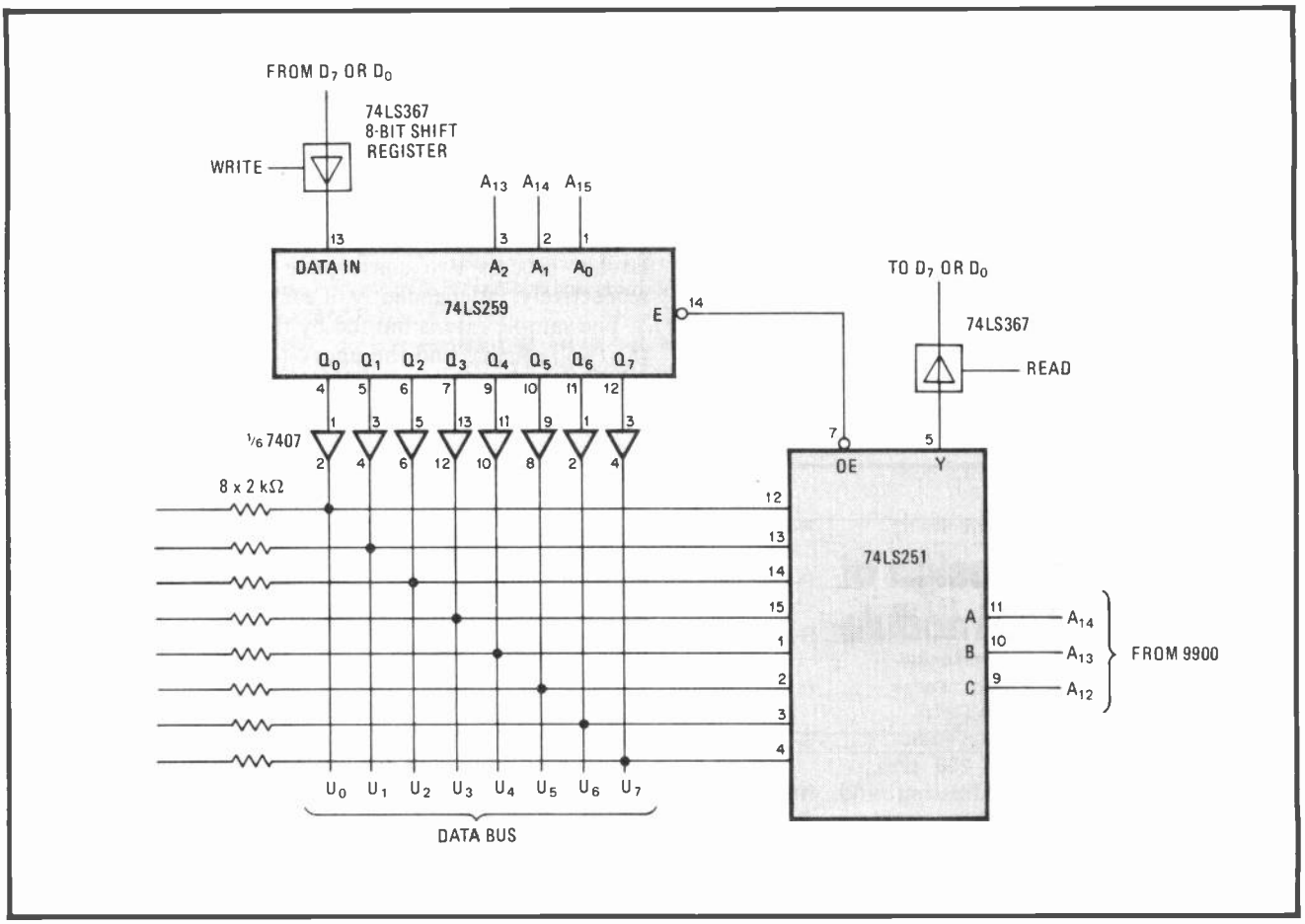
by Henry Davis
American Microsystems Inc., Santa Clara, Calif.

By combining standard addressing and multiplexing logic with the unique interface structure of the AMI 9900 microprocessor, a truly bidirectional input/output module may be realized. This read/write unit is especially suited to digital test systems, but it will find applications in many general-purpose systems as well because of its low cost and the ease with which it can be interfaced with the microprocessor.

Design of the bidirectional module is simplified because the structure of the 9900's communications-register unit makes it possible to handle the data-bit stream efficiently with a minimum of software. The CRU supplies up to 4,096 input and output bits that can be directly accessed and may be addressed either individually or in fields of 1 to 16 bits. The 9900 employs three



1. Two-way street. Bidirectional I/O interface uses standard TTL addressing and multiplexing logic (a). The 9900's architecture simplifies both hardware and software. I/O can detect several output-line states, notably pull-down conditions due to short circuits on data bus (b).



2. Easily mated. I/O unit can interface with other processors, such as the 6800. Software requirements will be more stringent, however; they must provide for serial-to-parallel and parallel-to-serial conversions. Also, each bit must be mapped into one byte.

dedicated I/O pins (CRUIN, CRUOUT, and CRUCLK) and has 12-bit capability (lines A_3–A_{14}) of the address bus for interfacing with the CRU system. The processor instructions controlling the CRU (SBZ, SBO, TB) can respectively set, reset, or test any bit in the CRU array or move the bits between memory and CRU data fields.

In the circuit example in Fig. 1a, the 9900 is used to perform an 8-bit parallel-to-serial conversion for data that is to be written on the data bus, from the microprocessor through the 74LS259 addressable latches. During all read operations, the 9900 converts the serial data stream emanating from the 74LS251 eight-channel multiplexer (which receives the bus data) into a parallel word so that it may be processed.

As for the software, the bit instructions SBZ, SBO, and TB control a single processor-to-I/O data line, selecting the address corresponding to the bit desired and executing the required bit setting or bit test, as the case may be. Multibit transfers are implemented by the processor using the LDCR and STCR instructions.

Whether in the read or write phase, the starting address of the CRU field to be transferred should first be loaded into the base-address register. This address is the least significant bit of the CRU field to be acted upon by the software. Next, data should be transferred in the appropriate direction (system memory to I/O interface or interface to memory) by reading or writing each I/O line in succession, under automatic processor control. The LDCR output of the CRU initializes the shift of the desired field from the memory to the I/O, through a register in the 9900, if in the write phase. The bits corresponding to the field to be transferred are then shifted out onto the CRUOUT line, which is connected to the 74LS259. The noninverting, open-collector buffers (7407s) protect the latches from short circuits on the data bus.

To use the I/O module for read-in, a logic 1 (high) must be written onto the corresponding output line to be examined (from the processor through the 74LS259). This will cause the 7407 to be pulled low if the data bus line is at logic 0. The CRUIN line can then be read using the STCR instruction.

The CRUIN line may be used to verify an output condition, making it easy to detect short circuits on the data bus. The procedure is to set all lines high, lower each in succession, and then read the lines to check for multiple lows. The table (Fig. 1b) outlines the various input/output conditions.

The circuit may be easily modified to work with other processors. For instance, Fig. 2 depicts such an arrangement for the 6800 microprocessor. A greater burden is placed upon the software here, because the program must perform the serial-to-parallel and parallel-to-serial conversions. □

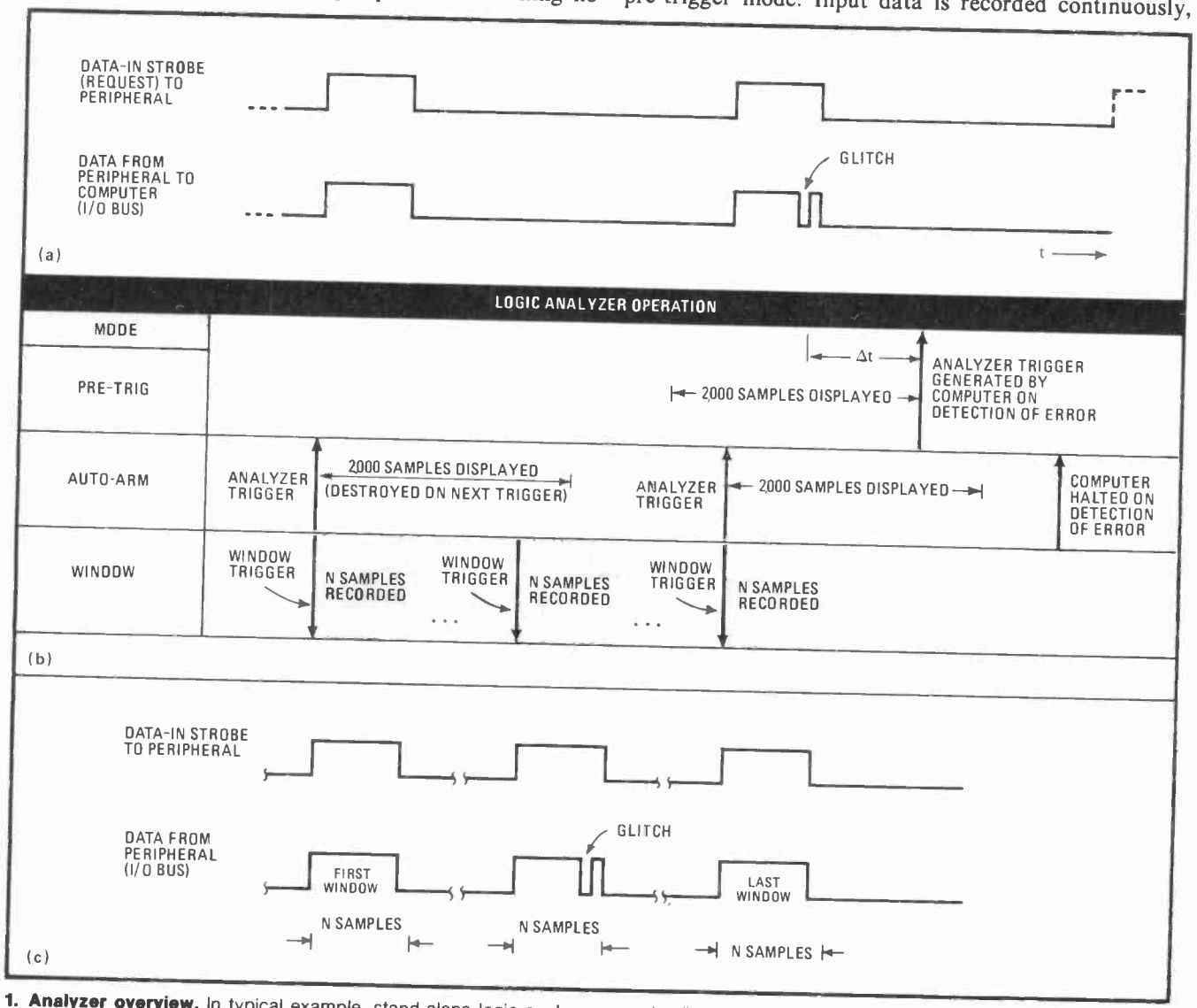
Window generator increases logic analyzer's capability

by Colin Gyles
Canadian Marconi Co., Montreal, Canada

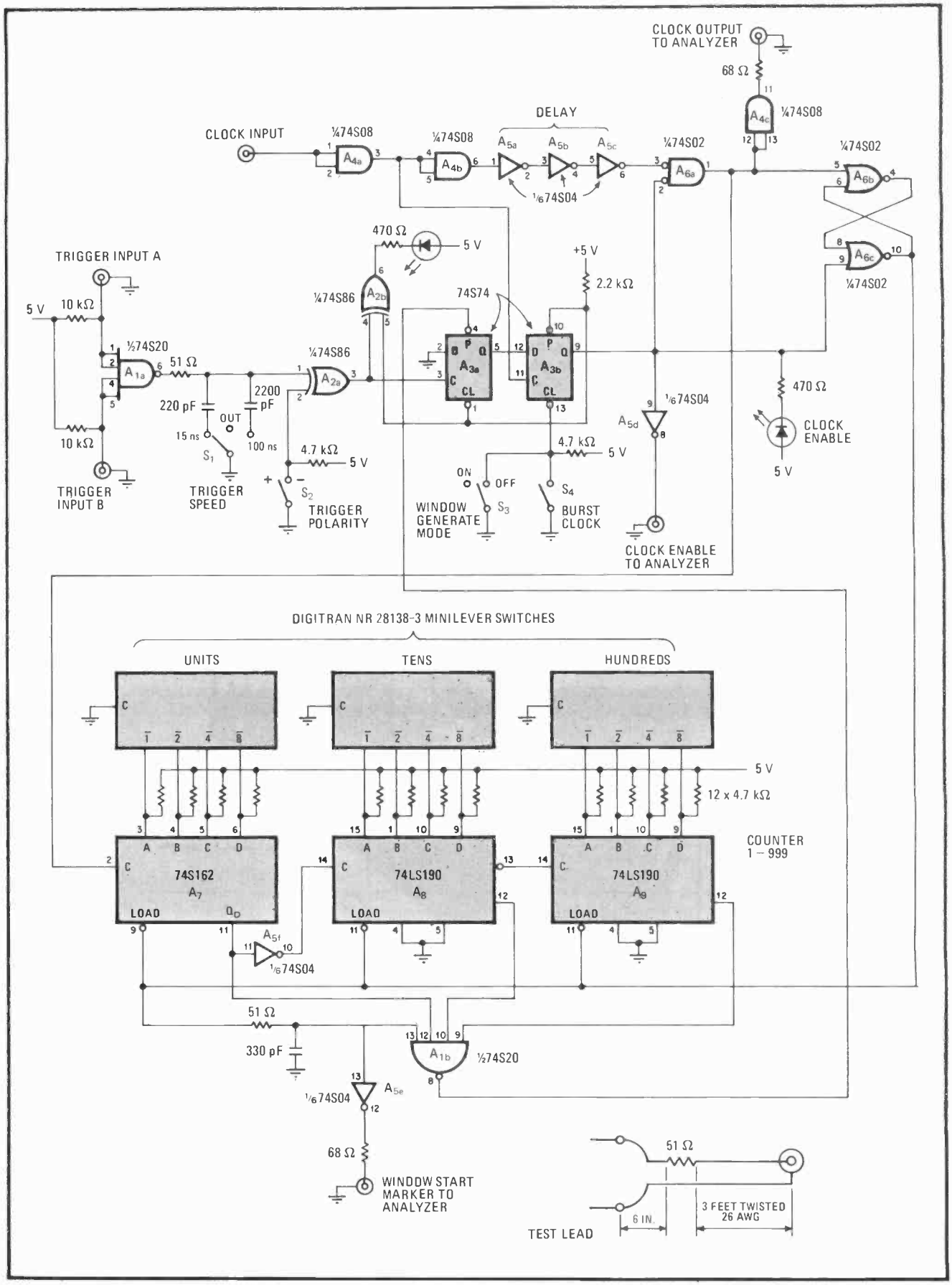
Although the diagnostic power of the logic analyzer is unparalleled for troubleshooting digital systems, its ability to detect the type of errors that lead to intermittent circuit failures leaves something to be desired. For example, the analyzer would have difficulty in detecting a random error in a computer system that passed data in short bursts separated by longer periods containing no relevant information. In such instances, this circuit vastly increases the recording range of analyzers of the time-domain variety, such as the Biomation 8100D.

It is necessary to understand the operation of a stand-alone analyzer to appreciate the difficulties involved in the display of certain data errors. In the example shown in the timing diagram of Fig. 1a, a strobe or similar data-request signal is sent from a computer or other control unit to a peripheral device. The peripheral then sends the data requested to the computer through the latter's I/O port. Note that the data has a glitch, perhaps caused by noise, so that when checked by the computer it is found to contain an error.

There are two methods of recording the error with an analyzer. The first method makes use of the analyzer's pre-trigger mode. Input data is recorded continuously,



1. Analyzer overview. In typical example, stand-alone logic analyzer records glitch in the last word received on computer I/O bus only, because of limited record range (a, b). Record range is vastly extended with window generator, which produces bursts of clock pulses during data-strobe time, permitting many data words to be recorded. Errors occurring in other than the last word received can thus be detected (c).



2. Window generator. Data-in strobe from control unit (computer) drives trigger inputs, initializing record period as circuit generates N clock periods, 1 microsecond wide, to analyzer through clock-output port. The value of N may be selected from 1 through 999.

and the analyzer is made to display the events causing the glitch. In the case of the 8100D, it displays the sequence of states that occurred in the interval, 2,000 sample units long, immediately preceding the trigger generated by the computer when the error was detected. Each sample unit corresponds to the period of the sampling rate of the analyzer's internal data clock. Thus, if the clock period is 20 ns, the events occurring up to 40 μs before the trigger can be displayed.

Needless to say, the larger the required recording range, the poorer the resolution and the harder it is to determine where an error occurs. And if the computer is so occupied with other duties that it cannot generate a trigger quickly enough after the error has occurred, the error will be missed altogether. Thus the time Δt, shown in Fig. 1b, must be minimized.

The second error-detection method uses the analyzer's auto-arm mode, which when triggered by an error records the following 2,000 samples. The circuitry is then rearmed. If a second trigger should occur, the analyzer destroys the previously recorded data and overwrites it with 2,000 new samples. The results of its operation are illustrated in Fig. 1b, with the trigger generated by the leading edge of the data-in strobe. With this method, the required range over which the analyzer records is small, so that the resolution will be high.

The error-detection problem cannot be solved satisfactorily by either method when the error is not contained within the last word received in a data stream (Fig. 1c). This condition might occur if the computer were making check-sum error determinations on a block of data from a paper-tape reader, where the results of the check would be revealed after the data word was read. In most instances, it would be impossible to display the error, since the time between strobes for a reader might be 100 milliseconds or so, but the strobe width might be only 1 microsecond.

Thus, to record a block of, say, 10 words, the record range would be 10(100 ms) = 1 second, but the resolution would be only 1/2,000 = 0.5 millisecond, and it is safe to conclude that an error lasting 1 μs would not be detected. Ideally it would be desirable to record the period in the vicinity of each strobe, where the error would occur, while holding the analyzer's internal clock off during the remaining time.

Therefore to detect the error, it is necessary to generate windows greater than 1 μs wide by a counter delivering N pulses to the external clock input of the analyzer after each window trigger, where N could be selected by the user. Then, on receipt of a trigger from the computer, due to detection of an error, the analyzer will stop recording (assuming pre-trigger mode) and display 2,000/N windows. The recording range would be equal to 4 seconds if N = 50 (that is, R = 100 ms [2,000]/50) for a resolution of 20 ns (equal to the analyzer's clock rate). This is an improvement of 100,000 times over the 40-μs recording range previously shown to exist for the same resolution.

The window-generator circuit for attaining the desired range magnification is shown in Fig. 2. The clock input is driven by a square-wave generator to provide the desired sampling interval. The logic analyzer is clocked by the signal emanating from the clock-output port. When a transition of the required polarity occurs at either of the trigger-input ports, the unit counts N clock pulses to the logic analyzer, N being set by the digital switch, which has a range of 1 to 999. During the time of the N-clock pulse burst, the trigger-input port is disabled.

The end result of the unit's operation is that N samples are clocked into the analyzer after each window-generator trigger. If the analyzer is set in the pre-trigger mode, then on receipt of an analyzer trigger from the computer, the recording will stop, displaying the last 2,000 samples, made up of 2,000/N windows side by side.

The window-start marker output may be fed to any one of the eight analyzer channels. This pulse is one clock period wide at the start of each window so that each frame may be identified at will. The clock-enable output can be recorded on a second logic analyzer to measure the time between window frames, if desired.

Note that the analyzer can be used in all trigger modes while using the window generator. In any of the post-trigger modes, the recording is complete when all 2,000 samples have been taken. If there are not a sufficient number of window triggers, the analyzer will hang up. The burst-clock switch is therefore included to enable the recording cycle to be completed manually whenever there are too few triggers to record the 2,000 samples.

The circuit relies mostly on sequential logic, as shown. S_1 and S_2 select the trigger speed and polarity, respectively. A positive transition at A_{3a}'s clock input brings its Q output low. At the next positive transition of the clock input, A_{3b} moves low. A_{4b} and A_{5a}–A_{5c} provide delay, in order that A_{6a} be enabled when the clock input is low. This is to prevent generation of a narrow clock-output pulse, which could upset the analyzer operation. The clock-output port now follows the clock-input signal. The circuit is designed to minimize the delay from the trigger-input pulse to the time the first clock-output pulse appears.

Just prior to the first clock at A_{6a}, the flip-flop A_{6b}–A_{6c} was set, which enables counters A_8 and A_9 to be loaded with the digital switches. A_7 is loaded during the first positive clock-input transition. This data is the 9's complement of what is displayed. A_{6c} is then set high, and the counters are free to advance from their set values up to 999, at which time the counters enable A_{1b} and preset A_{3a} to logic 1.

During the next clock input, A_{3b} moves high. The delay provided by A_{4b} and A_{5a}–A_{5c} disables A_{6a} before the clock-input transition arrives at its input, thus ensuring that no narrow glitches can be produced at clock output, as mentioned previously. The logic present at the output of A_{3b} then sets A_{6b}–A_{6c}, removing the preset signal from A_{3a} so that the trigger can be enabled for the next window.

Lead lengths should be minimized when building the circuit. The test lead for the trigger-input port should be built carefully also. It should not exceed 4 feet in length. A 51-ohm resistor on the hot side of the test lead will minimize ringing and reflections of energy from probed

circuits. Twisted-pair wires should be used to avoid undesirable coupling effects.

The circuit can work up to 60 MHz, with a one-count error between 33 and 60 MHz, which simply increases the window size by one. The size of the window does not substantially affect circuit accuracy. □

Synchronous pulsing cuts three-phase motor's dissipation

by D. J. Greenland
Cambridge, England

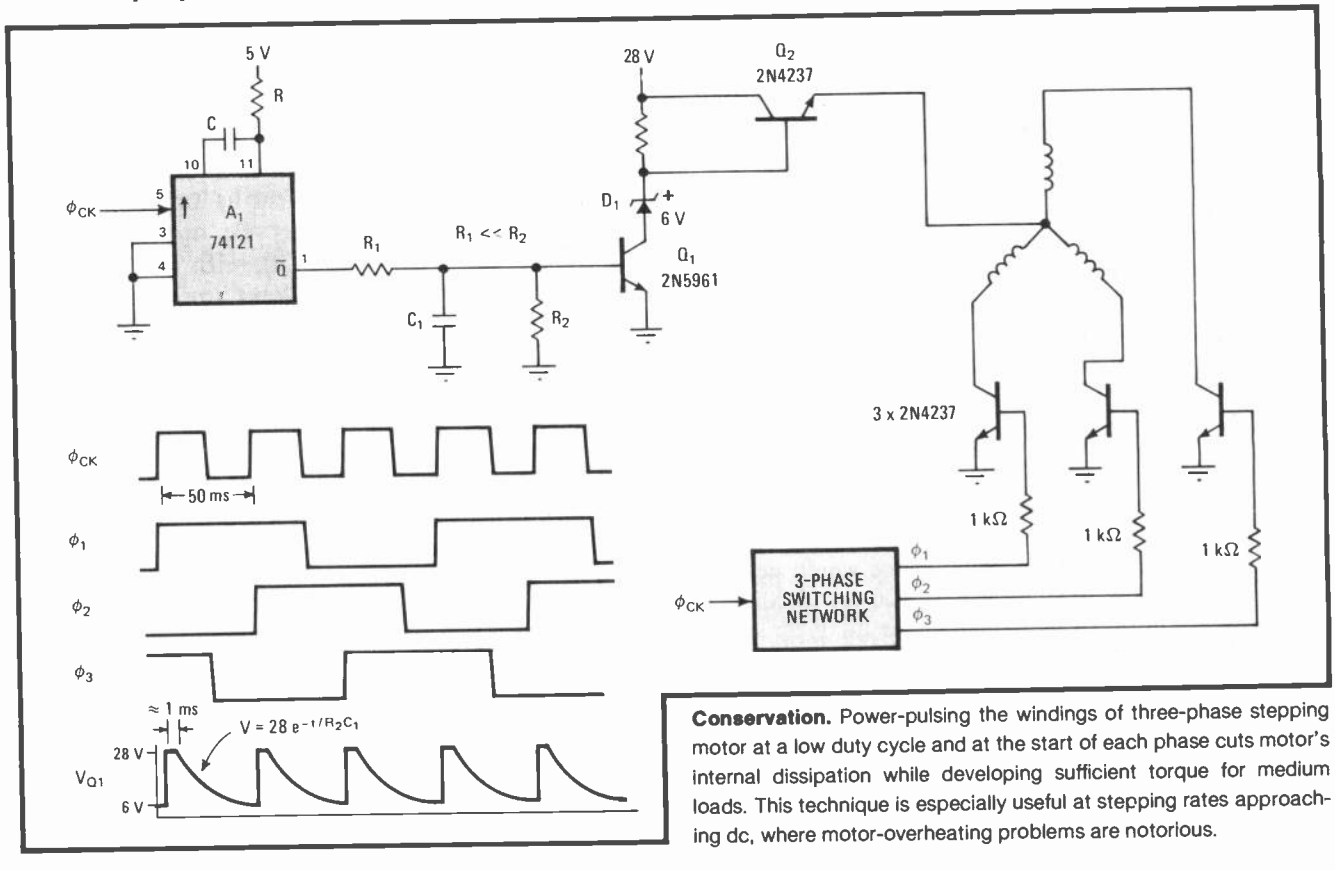
At very low clock rates, below 20 hertz, the windings of a three-phase motor dissipate excessive power. But this problem may be overcome if the motor is not heavily loaded—that is, the torque is less than 20 gram-centimeters. The circuit described here momentarily switches on the motor's supply line synchronously with the phase-generator clock pulse that activates each winding in sequence. Pulsing the windings at a low duty cycle and at the start of each phase increases circuit efficiency, yet enables the motor to develop sufficient torque.

Consider the savings in power. If each winding has a dc resistance of 15 ohms and is periodically energized from a 28-volt source, the power dissipated by each winding as the clock rate approaches zero is $P = (28)^2/15$, or 52.26, watts. Even when working at 20 hertz, or a 50-millisecond period, each winding would be energized for the same 50 ms or so and the power consumed per phase would be $P = (28^2/15)(50)(10^{-3}) = 2.61$ w. But if the energizing time can be reduced to 1 ms, say, the power consumed will be $P = (28^2/15)(1)(10^{-3}) = 52.26$ milliwatts.

The energizing time, T_e, is controlled by elements R and C of the 74121 monostable multivibrator, A_1, as shown in the figure. The one-shot is driven by the same phase generator clock, ϕ_{CK}, that also drives the three-phase switching circuit. (Since many well-known arrangements exist for deriving the required phase voltages for the windings, the actual schematic for the network is not shown here.)

A_1 fires on the positive edge of ϕ_{CK} and generates a 1-ms pulse that charges C_1, switches Q_1, and brings its collector to 28 v. Q_2 then turns on, driving the particular windings that happen to be activated at that instant by the switching network. The $\overline{Q}$ output of A_1 then moves back to 1 after the 1-ms interval and C_1 discharges through R_2 exponentially. C_1, R_1, and R_2 are selected once the frequency of ϕ_{CK}, R, and C are known.

It should be mentioned that at clock rates above 1 kilohertz, this circuit offers no power-saving advantage. This is because the period of 1-kHz waveform is 1 ms, comparable to the duty cycle required to reduce the dissipation for the 20-Hz clock previously discussed. □



Conservation. Power-pulsing the windings of three-phase stepping motor at a low duty cycle and at the start of each phase cuts motor's internal dissipation while developing sufficient torque for medium loads. This technique is especially useful at stepping rates approaching dc, where motor-overheating problems are notorious.

Small interface simplifies processor interrupt routine

by Robert Shanafelt
Los Altos, Calif.

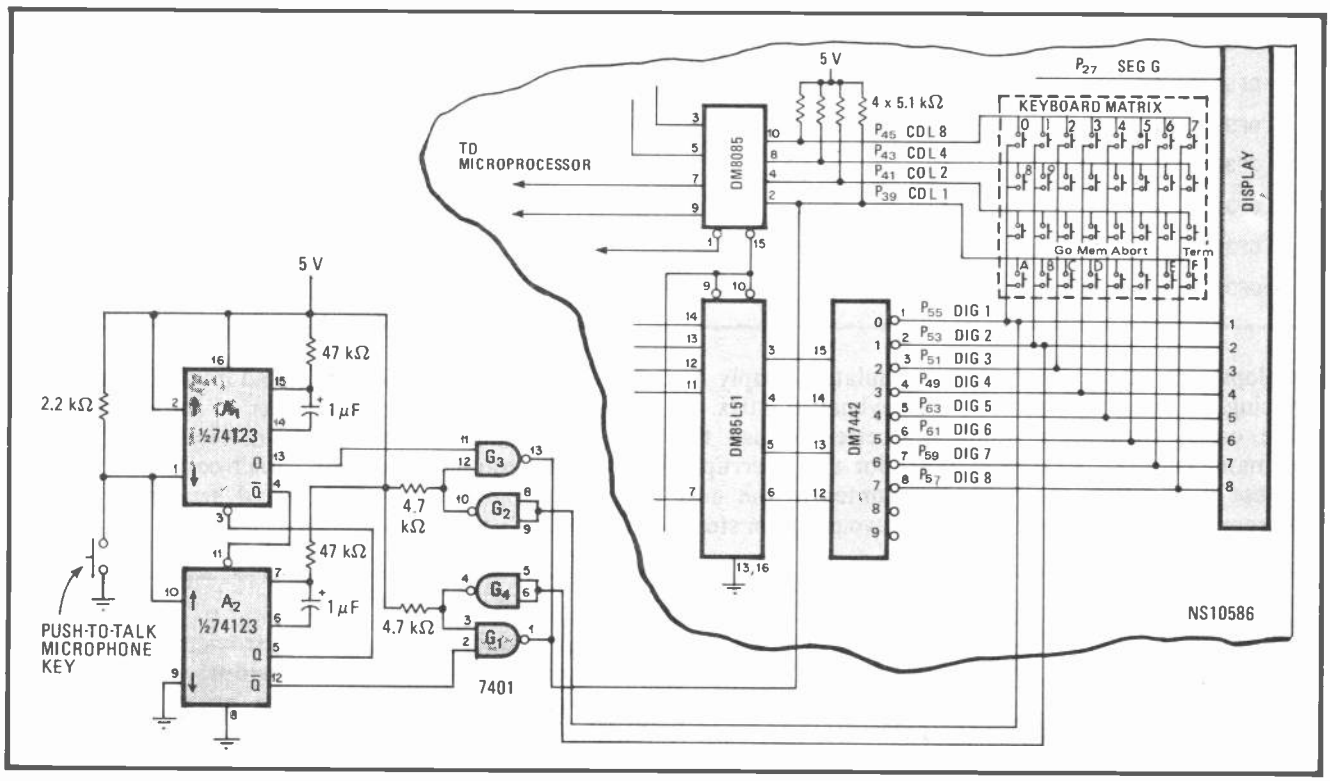
The closing and opening of an assigned key triggers an exit from the memory-resident display- and keyboard-strobing routine supplied in National Semiconductor's popular SC/MP keyboard kit. But often the SC/MP microprocessor needs to respond to a signal not initiated through the keyboard, such as a transmit/receive interrupt when the kit is used to control a transceiver. A way out of this difficulty is to transform the interrupt command into a simulated key closure by means of a small hardware interface. Built out of a dual one-shot and four NAND gates, this interface not only simplifies hardware design but also keeps the amount of software that will be needed for servicing the interrupt to a minimum.

As indicated by the figure, depressing the microphone key initiates the transmit interrupt request to the NS10586 keyboard-to-microprocessor board that comes with the kit. The event causes A_1 to generate a positive-going, 16-millisecond pulse. This pulse first combines at NAND gate G_3 with the digit-1 strobe from G_2 that interrogates keys A, 8, and 0 (line P55) of the keyboard matrix. The result is then transferred through the wired-OR logic configuration of G_1–G_3 to column 1 on the matrix (line P_{39}). At column 1 a negative-going pulse is produced that is synchronous with the digit-1 strobe and is identical to the pulse that would be generated if the A key on the keyboard matrix were depressed.

When the microphone key is released, A_2 generates a positive-going pulse for long enough (16 ms) to overcome the effects of switch bounce. The transfer of this pulse to line P_{39} is similar to the process previously described, except that gate G_4 is activated instead of G_3, corresponding to activation of the B key.

The program required to produce the interrupt request is shown in the table. It is written so that a light will turn on when the circuit is in the transmitting mode and will turn off when the circuit is in the receiving mode. In advanced applications, the program steps that turn on the light could be replaced with coding that would fetch the transmitting frequency corresponding to the channel input, display it, and present it to the frequency synthesizer for the transmitter, while the code that turns off the light could be replaced with coding that would do the same jobs for the receiver.

An advantage of this scheme is that during program



Simulated keyboard interrupt. Two one-shots and four NAND gates transform transmit/receive command into an apparent keyboard closure for SC/MP microprocessor. Only three interconnections to the microprocessor board are required. The small interface simplifies hardware design and keeps the amount of software needed for servicing the interrupt to a minimum (see table).

SC/MP INTERRUPT ROUTINE

RAM location	Code	Mnemonic	Comment
0F20	C4	LDI	
0F21	01	01	
0F22	37	XPAH	*Load 0184 into P3 register, which is starting point of keyboard strobe and display routine.*
0F23	C4	LDI	
0F24	84	84	
0F25	33	XPAL	
0F26	3F	XPPC	*Start keyboard strobe and display routine*
0F27	90	JMP	*Jump if either GO, TERM, or MEM key pushed*
0F28	00	00	
0F29	C4	LDI	
0F2A	0A	0A	*Test if A key pushed*
0F2B	60	XRE	
0F2C	9C	JNZ	*If not A, jump to 0F33*
0F2D	05	05	
0F2E	C4	LDI	
0F2F	00	00	*Set flag 1 low (turn light off)*
0F30	07	CAS	
0F31	90	JMP	*Jump to 0F20*
0F32	ED	−19	
0F33	C4	LDI	
0F34	0B	0B	*Test if B key pushed*
0F35	60	XRE	
0F36	9C	JNZ	*If not B, jump to 0F20*
0F37	E8	−24	
0F38	C4	LDI	
0F39	02	02	*Set flag 1 high (turn light on)*
0F3A	07	CAS	
0F3B	90	JMP	*Jump to 0F20*
0F3C	E3	−29	

development, interrupts may be simulated simply by pressing the A or B buttons on the keyboard matrix. In some cases, though, it would be better to use the command keys GO, MEM, and TERM for the interrupts, because they return the program counter to the next program step instead of skipping over two program steps. In the latter case, a JUMP command might be needed for repositioning the program counter to the desired location, depending upon the program requirements. Note that in no instance could the ABORT command be used, because program execution would terminate on this instruction. □

Badge reader checks for production defects

by K. C. Herrick
ESI Electronics Corp., San Francisco, Calif.

Though production testing of electronic products usually involves only a set of simple individual tests, the repetitive measurements that must be made require much manual switching to connect the test circuit to identical points in each device. The small perforated-card (badge) reader described here, however, will eliminate much of the labor of constructing test-set fixtures by enabling a single set of cards, each of which is individually coded

for a specific test, to set all switches automatically.

The most useful type of badge reader for testing purposes is the bed-of-nails variety. In this reader, an array of metal pins is clamped against an inserted card to sense hole or no-hole status at all possible hole positions simultaneously. Typical readers contain 100 to 240 hole positions and include a switch at each position that is activated if a hole exists there. Actuation of the reader either is automatic, using a solenoid, or requires a spring-release, which is cocked by prior actuation of a card-ejection lever. The readers are readily available from AMP, Sealectro and others, and some are available on the surplus market.

A hand punch can be used to punch holes in a card in any desired configuration. A set of cards is then prepared for each test performed. Only a single reader need be used if the reader's sensing and control circuits are connected to standardized connectors. The specific test setup for each item to be checked is then configured with mating connectors so that the reader can be easily plugged into the desired test jig.

The reader's sensing switches may be wired in almost any configuration, because both sides of each switch are isolated. In general, however, it is advantageous to create a switching matrix that is bused along one axis, yielding, for example, 10 individual switches making contact to each of 12 buses. Far fewer wires need be brought to a connector when the busing technique is used.

The usefulness of a small card reader may be illustrated with a simple example in which 15 identical circuits have to be tested on each item. Each circuit is to have one balanced input port and one output port. Bipolar circuit potentials must be applied and measured. Because the input to each circuit is balanced, input signals must be applied separately. Only the input lines and power line may be bused. Also, 15 diodes must be tested for their forward voltage drop and the peak-inverse voltage they can withstand.

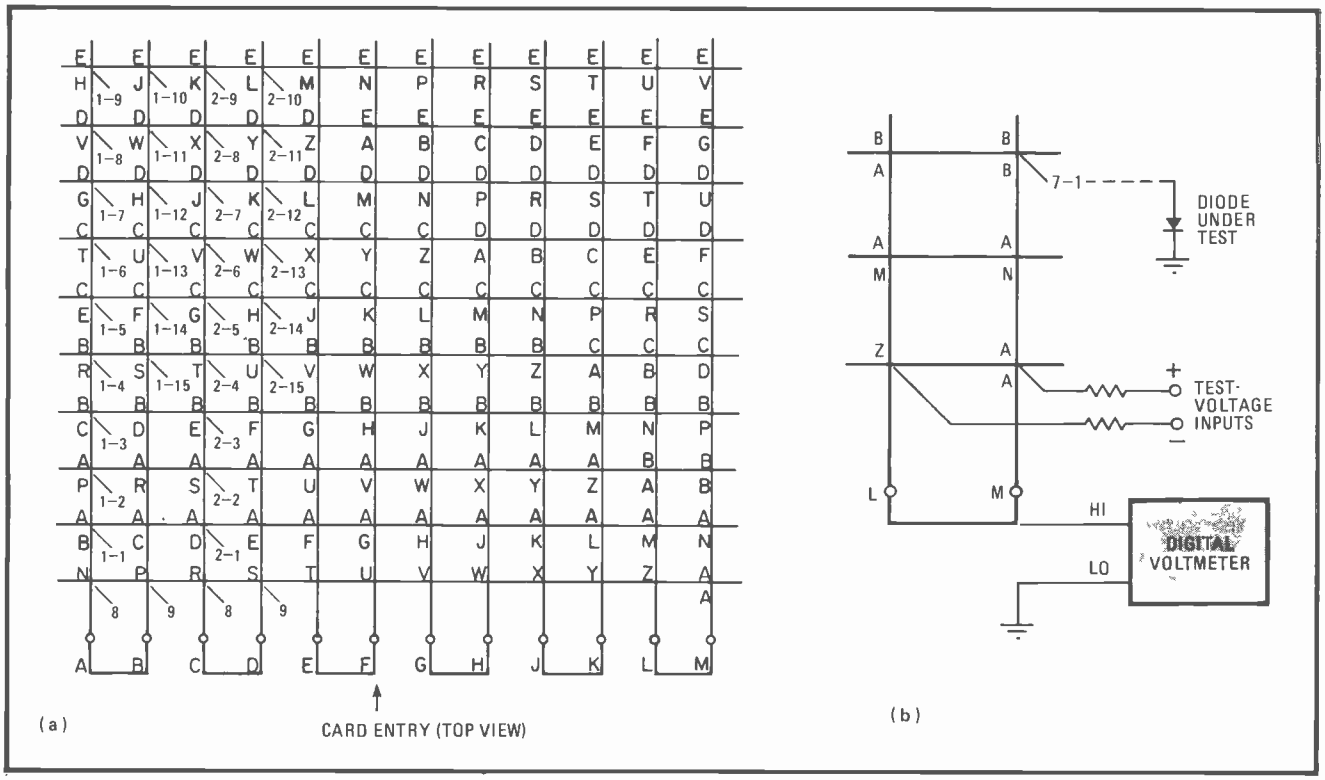
Wiring up a conventional manual-switch test jig would require much labor and several multiposition switches. Consider how the card reader would be used instead.

Each of the 15 circuits may be looked upon as a black box with seven leads, of which the first two represent the input port, the third and fourth go to measuring instruments, and the fifth represents the output. Each of the 15 diodes can be accessed via the sixth (cathode) and seventh (anode) terminals.

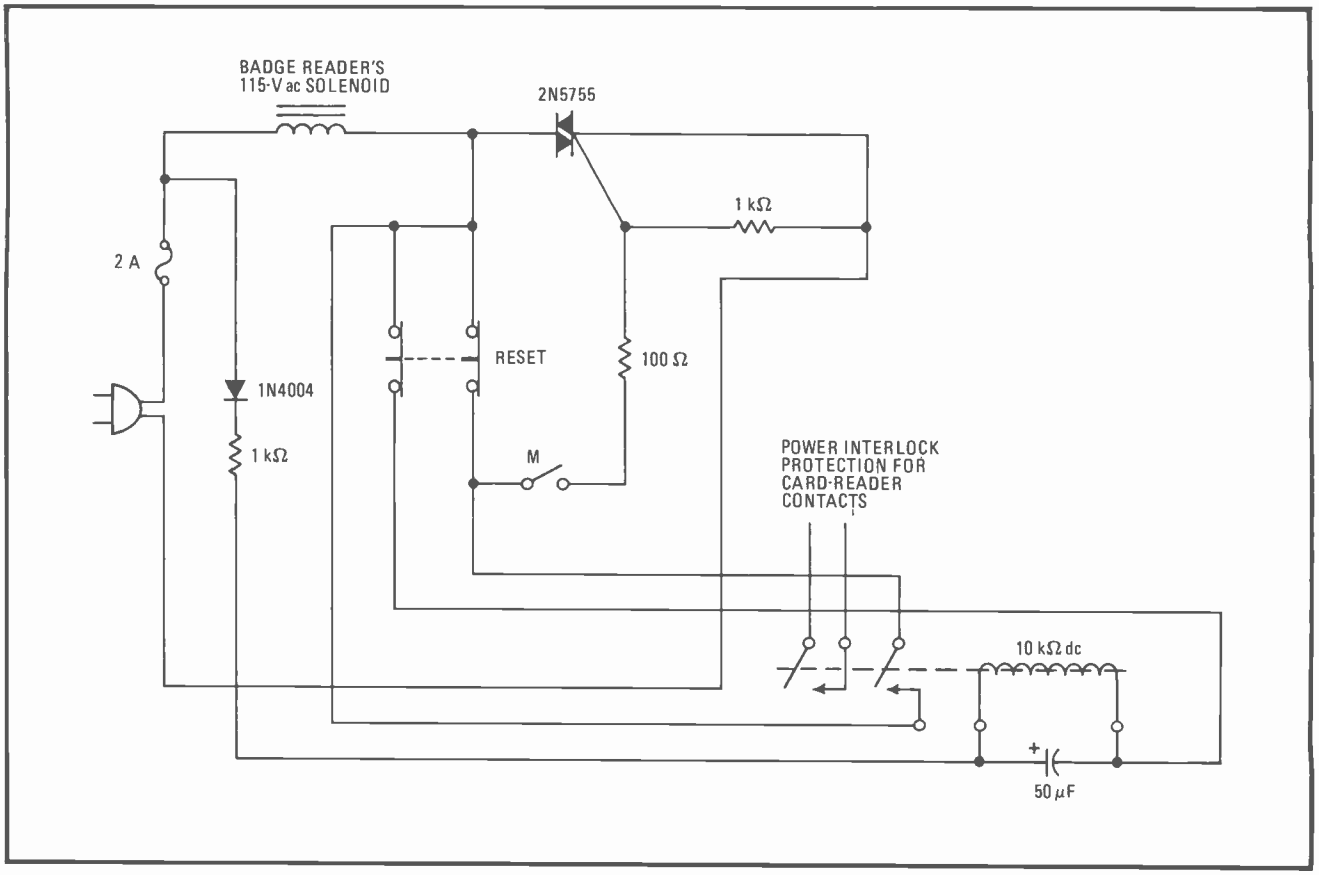
A 12-by-10-switch matrix (Fig. 1a) may be used in this example. The matrix lines or points are designated by letters or letter pairs A–Z or AA–EV, each of which denotes a bus or switch point. Note that columns are bused, but switch contacts in the rows are individually connected to the wire denoted by the letter or letter pair. The leads of each circuit to be connected to a switch or bus are given by a designation in the area below and to the right of a given cross-point.

Conductor 1 of each circuit is assigned numbers 1–1 to 1–15. Conductors 2 through 7 are similarly assigned n–1 to n–15. Because each bus has only 10 contacts, two buses must be assigned to accommodate all leads 1 and 2. Thus lines A and B of the matrix are tied together, and so are lines C and D.

The signal source driving the circuits' input designated 8 and 9 is not connected directly to the buses, but rather



1. Automatic. A 12-by-10-switch matrix formed by card-reader contacts can be used to make production line test-jig checks (a). Programmed cards switch in balanced line inputs (and outputs) of seven-port circuits under test (see text), to be driven by external sources 8 and 9 at lines A through D on matrix. Setup for checking diodes' forward voltage drop and inverse withstanding value is shown in (b).



2. Reader actuator. Control circuit for card reader that uses solenoid, such as Sealectro's model 0811-012-007, has relay delay that protects reader contacts from excessive current should a short circuit exist in test jig. The relay also prevents pitting of reader's sensing switches if contacts make or break with current flowing. M represents reader microswitch that is activated by insertion of card.

to the field of the matrix, as shown. Then leads 1 and 2 of the individual circuit boards are connected to the assigned matrix points.

Now, by punching a card at points AB, AD, N and S, an input signal of a given polarity can be applied to leads 1 and 2 of circuit board number 1. By punching a second card at AB, AD, P and R, a voltage of the opposite polarity is applied. In this way, all input connecting is done by punching four holes in one card—two to select the signal polarity and two to select the individual circuit board to be tested.

A circuit's measurement leads (3 and 4) and output lead (5) may be accessed in a similar way, but because polarity need not be considered, test circuits may be connected via the matrix buses. For instance, the output device at lead 5 (perhaps a load or a meter) can be connected to buses E and F, with leads 5 of the individual circuit boards connected to T, AF, AU, etc. Similarly, buses G and H should be tied together and then connected to a meter (lead 3), and buses J and K should be tied together and connected to the measuring instrument at lead 4.

Columns L and M of the matrix are used for diode measurements. One side of each diode is grounded, and its free end is connected to the matrix field. Extra contacts are available for applying two polarities of test signal, and a digital voltmeter can be connected to buses L and M. The circuit is as shown in Fig. 1b.

If holes AA and BB are punched on a card, the forward drop for a diode will be measured by the digital voltmeter. If a second card is punched at Z and BB, the diode's reverse voltage will be measured.

For card readers that are operated by a solenoid, a permanent control circuit should be built. The one in Fig. 2 serves well for a popular Sealectro reader.

With the example setup, all tests are done using 30 cards and separate meters for 3, 4, and diode testing. A single meter could be used for all measurements if 92 cards were used: a set of 30 cards would be required to access output lead 5, each of which, in addition to having its normal complement of holes, would require a hole at V and a 3 hole in matrix column G or H. A second set of 30 cards would access output lead 4. These cards would resemble the first set, except that hole X and holes in columns J and K would have to be punched in addition. A final set of 32 cards would require holes only in columns L and M for testing the diodes.

Blank cards can be obtained from at least one supplier (AMP), premarked with matrix-hole locations. AMP also sells a hand punch. These accessories have on occasion been offered with surplus readers also.

The cost of a new badge reader could run from $150 to $350. Surplus units can be obtained for as low as $50, and some of these units with cards and punches are available from the author. □

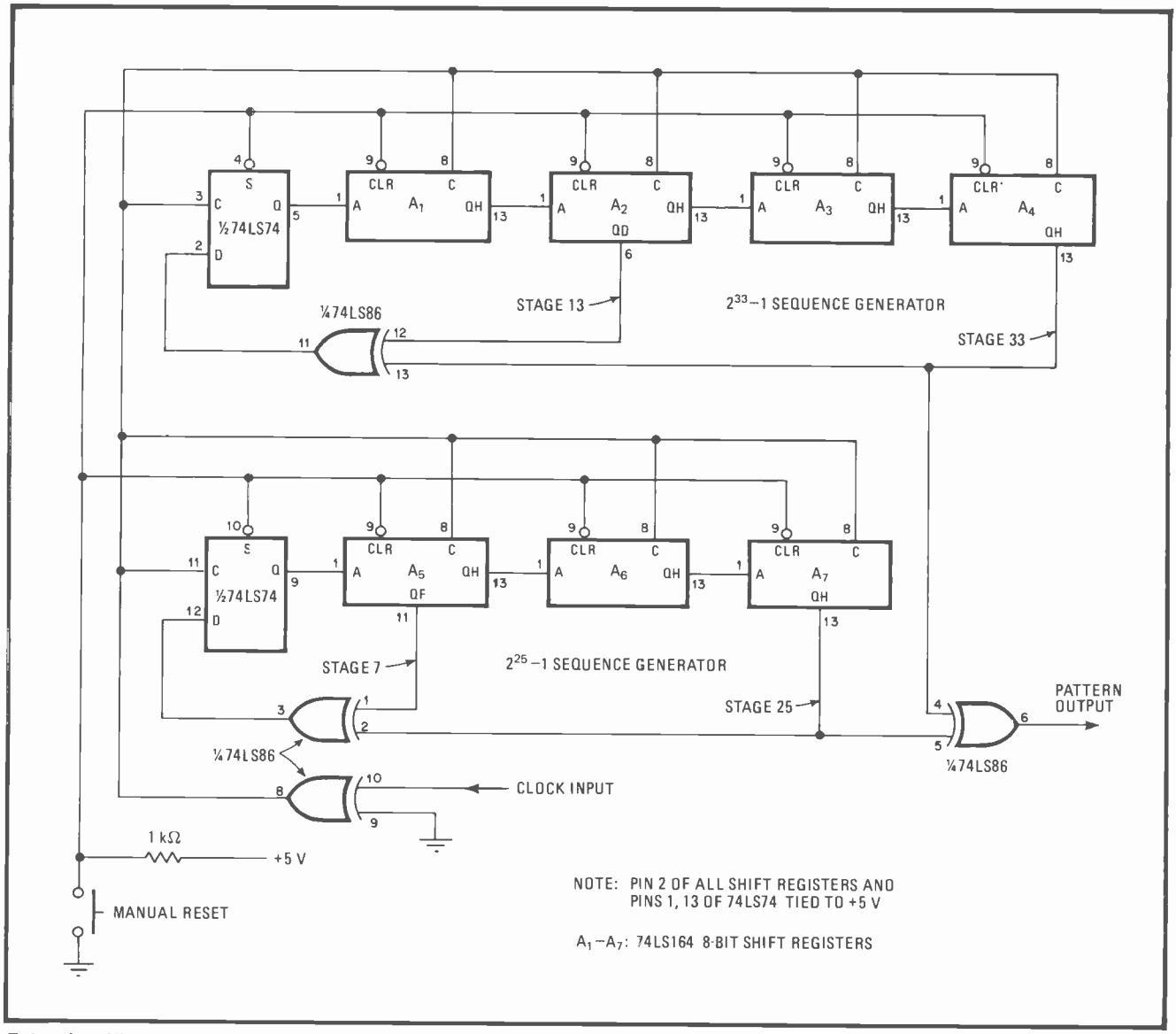
Uniting number generators for long bit patterns

by Leonard H. Anderson
Sun Valley, Calif.

The length of a pseudo-random bit pattern can be predictably extended if the rules for combining two or more available sequence generators of given length are known and applied. Fortunately, the interface required for combining number generators is extremely simple, often consisting of no more than one logic gate.

Maximal-length sequence generators that use shift registers normally have periods of $2^n - 1$, where n represents the number of registers used. Every such sequence has a numerical length that is odd, but few lengths are prime (that is, most often the number can be factored). It is a property of the register to have recurring factors that depend on the n^{th} multiple. The table shows the maximum length for any n and the factors common to every n^{th} multiple from 2 to 47.

These factors enable the designer to determine whether combining two or more generators of given length will increase the total sequence length: two generators having common factors tend to generate similar patterns during



Extension. Nine-package circuit combines 33-stage and 25-stage pseudo-random sequence generators in order to extend pattern length to 2.88×10^{17} clock periods. Generators' outputs are merged with one exclusive-OR gate. Combining generators of any length for long bit patterns is possible, provided rules for applying bit-pattern data (see table) to n-stage registers are known.

portions of their individual cycles, causing a departure from the pseudo-random output expected.

The factors for all sequence lengths have been found by first factoring n, then finding all the possible products of any and all factors, and finally consulting the table for the n^{th}-multiple sequence length. For a $2^{24}-1$ generator, $n = 24 = 2 \cdot 2 \cdot 2 \cdot 3$. The n-factor combinations of 2·2·2·3 are 2, 3, 4, 6, 8, 12, and 24; thus, sequence length factors are 3, 7, 5, 3, 17, 13, and 241, respectively.

Now, if a $2^{24}-1$ generator is connected in series (cas-

BIT-PATTERN DATA – n-STAGE PSEUDO-RANDOM GENERATORS

n	Sequence length	Sequence length factors common to every n^{th} multiple
2	3	3
3	7	7
4	15	5
5	31	31
6	63	3
7	127	127
8	255	17
9	511	73
10	1023	11
11	2047	23 89
12	4095	13
13	8191	8191
14	16,383	43
15	32,767	151
16	65,535	257
17	131,071	131,071
18	262,143	19
19	524,287	524,287
20	1,048,575	5 41
21	2,097,151	7 337
22	4,194,303	683
23	8,388,607	47 178,481
24	16,777,215	241
25	33,554,431	601 1801
26	67,108,863	2731
27	134,217,727	262,657
28	268,435,455	29 113
29	536,870,911	233 1103 2089
30	1,073,741,823	331
31	2,147,483,647	2,147,483,647
32	4,294,967,295	65,537
33	8,589,934,591	599,479
34	17,179,869,183	43,691
35	34,359,738,367	71 122,921
36	68,719,476,735	3 37 109
37	137,438,953,471	223 616,318,177
38	274,877,906,943	174,763
39	549,755,813,887	79 121,369
40	1,099,511,627,775	61,681
41	2,199,023,255,551	13,367 164,511,353
42	4,398,046,511,103	5419
43	8,796,093,022,207	431 9719 2,099,863
44	17,592,186,044,415	397 2113
45	35,184,372,088,831	631 23,311
46	70,368,744,177,663	2,796,203
47	140,737,488,355,327	2351 4513 13,264,529

caded) with a 2^6-1 generator, a $2^{30}-1$ generator will result. Most often, the feedback connections between generators will not be known, so the method used to combine these generators (to be described shortly) might prove handy. However, in this case, combining the generators in the manner to be shown will not increase total sequence length either, because all factors of the 2^6-1 generator (that is, 3, 3, 7) are common to the $2^{24}-1$ generator previously analyzed.

Replacing the 2^6-1 generator with one that delivers a 2^9-1 bit stream will increase the total sequence length by only 73, as shown in the table, since the sequence length is 511 = 73·7, and 7 is still common to a factor of the $2^{24}-1$ generator. A generator having a higher order of n is thus needed to effect a significant increase in sequence length. Combining even-n generators should be avoided, however, because of the recurrence of the factor 3 at n multiples of 6 and 18, and a recurrence of factor 5 at multiples of 20. Factor 7 occurs at n = 21, also.

Only nine chips are required for a pseudo-random generator circuit that combines a $2^{33}-1$ bit stream with a $2^{25}-1$ one, as shown in the example in the figure, where the circuit arrangements for both generators are individually known. Note that both generators are merged via only one exclusive-OR gate.

The total pattern length is 2.88×10^{17} clock periods. Using a 10-megahertz clock, the pattern does not repeat for 333,600 days, or 913.347 years. □

Optically isolated scope probe eliminates ground loops

by Yishay Netzer
Haifa, Israel

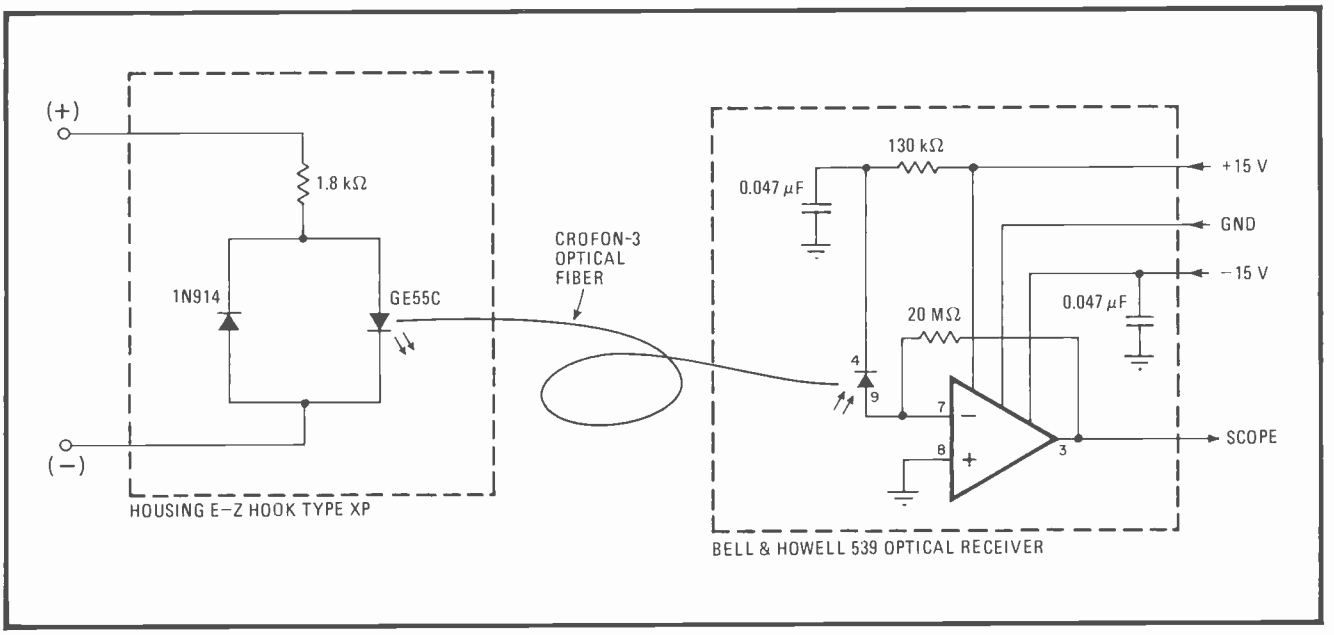
The infrared-light-emitting diode and optical receiver in this oscilloscope probe can detect an input signal while keeping the scope galvanically isolated from the circuit under measurement. In this way the probe eliminates any electrical interference caused by ground loops and by stray energy transmitted through supply lines. The probe has reasonable bandwidth and sensitivity, but is most useful for transferring signals in the audio range to the scope.

As shown in the figure, the head of the probe contains the LED, plus a series resistor that determines the sensitivity. Unipolar input signals generate a current through the GE55C LED, causing it to emit light of an intensity that is linearly proportional for signals greater than 1.6 volts (the LED's voltage drop). If the measured signal has no dc component, an offset (bias provided by a battery) must be applied at the input, and the composite signal should be capacitively coupled to the LED. The LED's output is then coupled by a plastic fiber-optic bundle to the 539 receiver located at the scope end, where the light is converted back into a voltage and coupled to the scope.

The probe's input impedance is understandably low. However, if a battery can be fitted into the probe head, it can serve as a supply for an active optical transmitter having high input resistance, high sensitivity, and wide bandwidth as well.

The packaged unit is lightweight and on first glance appears to be an ordinary scope probe. The probe has a bandwidth of 10 kilohertz. Voltage gain for the unit is 1 for input signals exceeding 1.6 V. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.



On the beam. Optically isolated probe transfers input signals to scope using light-emitting diode and light-sensitive receiver, thereby eliminating most electrical interference. Probe works over 10-kHz bandwidth, has linear response for input signals exceeding 1.6 V.

Single-wire pair multiplexes power and data for display

by Tommy N. Tyler
Powers Regulatory Co., Denver, Colo.

Using one decade counter per digit, this circuit multiplexes both power and data to a remote digital display over a single pair of wires. Implementing the circuit with a complementary-metal-oxide-semiconductor counter ensures the multiplexer draws only microwatts of power, a level that can be easily supplied by the circuit's power-storage element while data is being sent.

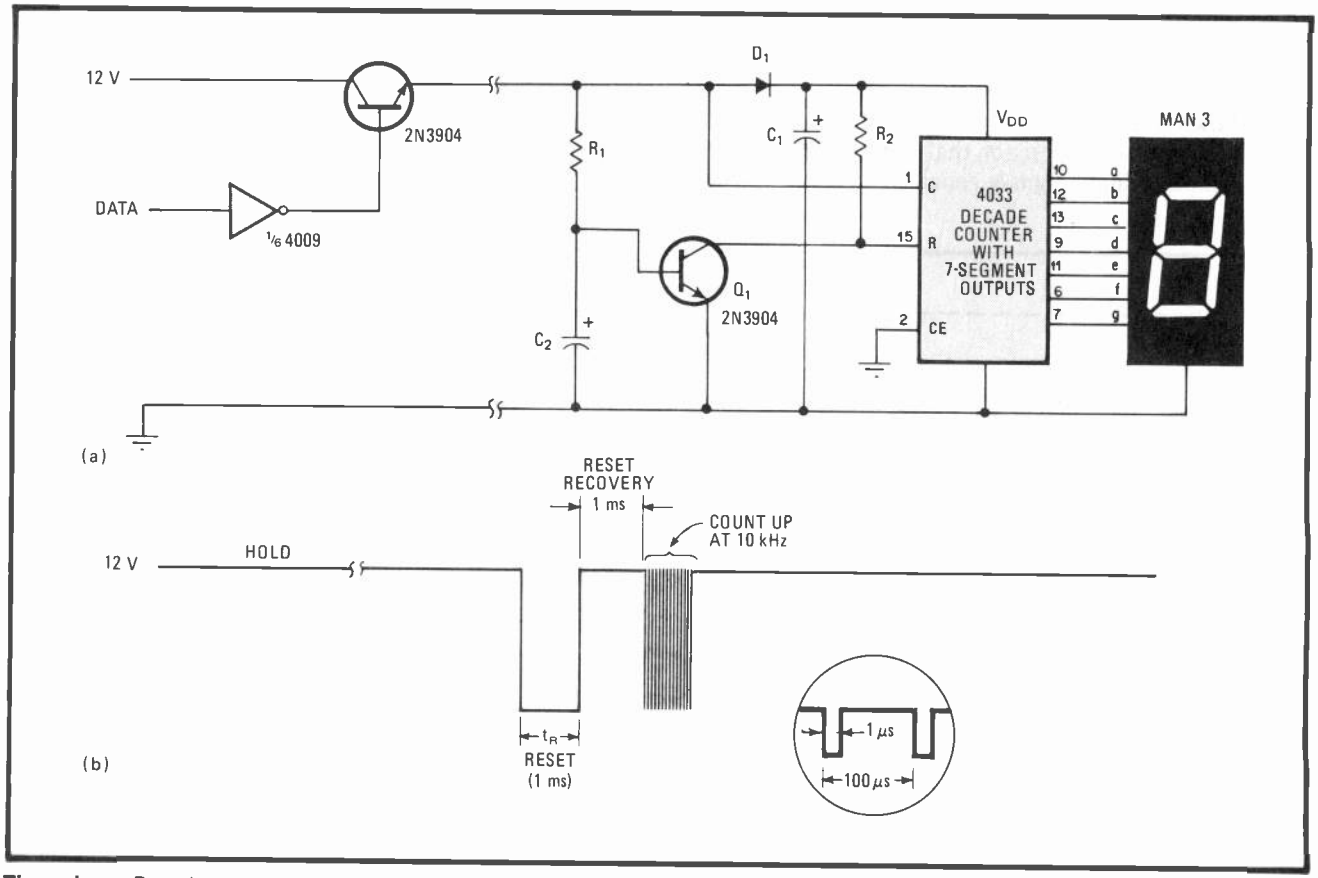
The arrangement required for a single digit is shown in (a). The circuit automatically initializes the display at zero on power up.

During the hold time (b), power is supplied to the 4033 counter via D_1, and C_1 charges up to the supply voltage. Following the hold interval, Q_1 turns off, allowing R_2 to pull the reset pin high, clearing the counter. The reset is accomplished by holding the line voltage low just long enough for C_2 to discharge and turn off Q_1. C_1 maintains power to the 4033 during this time.

After 1 millisecond, Q_1 turns on, and the number to be displayed is transmitted through the data line as a series of pulses with a 10-kilohertz burst frequency. These are sent directly to the counter's clock input. (Note that they are too narrow for the reset circuit to respond to.) Then the hold interval is repeated.

The display reading is updated by resetting the 4033 to zero and initiating a count again. By keeping the duty cycle of the data pulses very low, the display's supply voltage will remain essentially constant.

Multiple-digit displays require additional 4033s to be cascaded. With a 1-megahertz burst frequency, a four-digit display can be updated in 12 milliseconds, more than sufficient for ordinary viewing if the number of updates is at least two per second. Assuming four updates per second, the display will be steady 95% of the time. The 4033 will source 5 milliamperes per segment when operated at 9 volts, enough to produce fairly bright displays when MAN-3 devices are used. RCA application note ICAN-6733 provides extensive information on interfacing the 4033 chips with various displays. □



Time share. Decade counter enables multiplexing of power and data lines with a single-wire pair (a). Power stored in C_1 during the first portion of the cycle energizes 4033 during the time data is sent. The hold-count timing cycle (b) clarifies operation.

Digital strain gage eliminates a-d converter

by N. Bhaskara Rao
U.V.C.E., Electrical Engineering Department, Bangalore, India

An up-down counter and several logic elements are used here to transform signals from a strain-gage transducer into a corresponding digital output suitable for driving a display. Replacing the analog-to-digital converter normally required for this application, the counter circuit not only costs less but, more importantly, uses standard logic devices normally found at hand in the lab.

A 555 timer, A_1, is used as an astable multivibrator (see figure) whose on time is $T_a = 0.685(R_1 + R_2)C$ and whose off time is $T_b = 0.685R_2C$, where R_1 and R_2 are the resistances of two discrete transducer elements mounted on a common surface. Their values vary directly with the amount of strain applied. In this case, the nominal values of R_1 and R_2 are 120 ohms. Resistor r is a 2-Ω potentiometer that is used to zero the circuit (no output from the 555) under no-strain conditions.

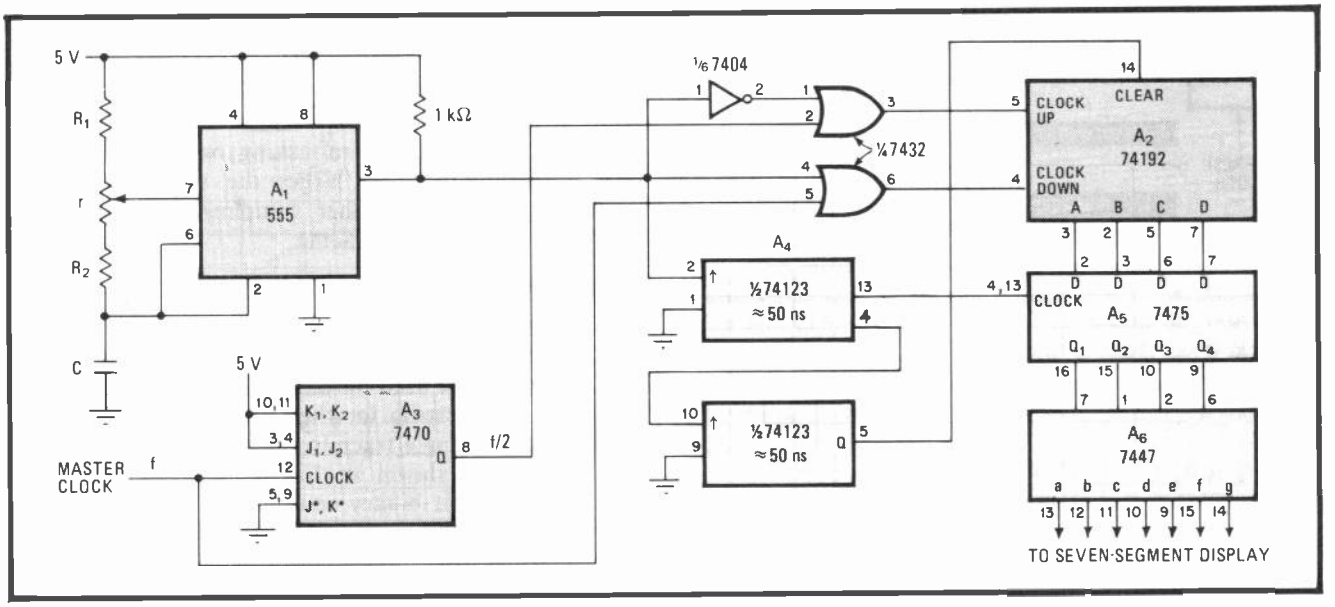
R_1 and R_2 are wired so that $R_1 - R_2$ becomes a positive value when a strain is applied to them. When the output of A_1 is high, the 74192 counter (A_2) advances up at a rate of f/2, where f is the circuit's master clock frequency and f/2 is derived from flip-flop A_3.

When A_1 is low, the 74192 counts down at a rate of f. Thus, at the end of one cycle, the net counter reading will be $N = T_a(f/2) - T_b f$, or:

$$N = 0.685f(R_1 - R_2)C/2 = K(R_1 - R_2)$$

where the scale factor, K, equals 0.3425fC. Therefore the amount of stress becomes known when $R_1 - R_2$ is determined. K can be set to any value by the proper choice of f and C. As seen from the equation, the sensitivity of the circuit increases as K is made larger.

As A_1 moves high at the start of the next cycle, one half of the 74123 dual one-shot, A_4, is triggered and clocks the 7475 quad latch, A_5. Thus the latch stores the contents of A_2. A_6 converts the 4-bit binary input into a seven-segment output for the display. The other one-shot in A_4 then clears A_2, and the new count cycle begins. □



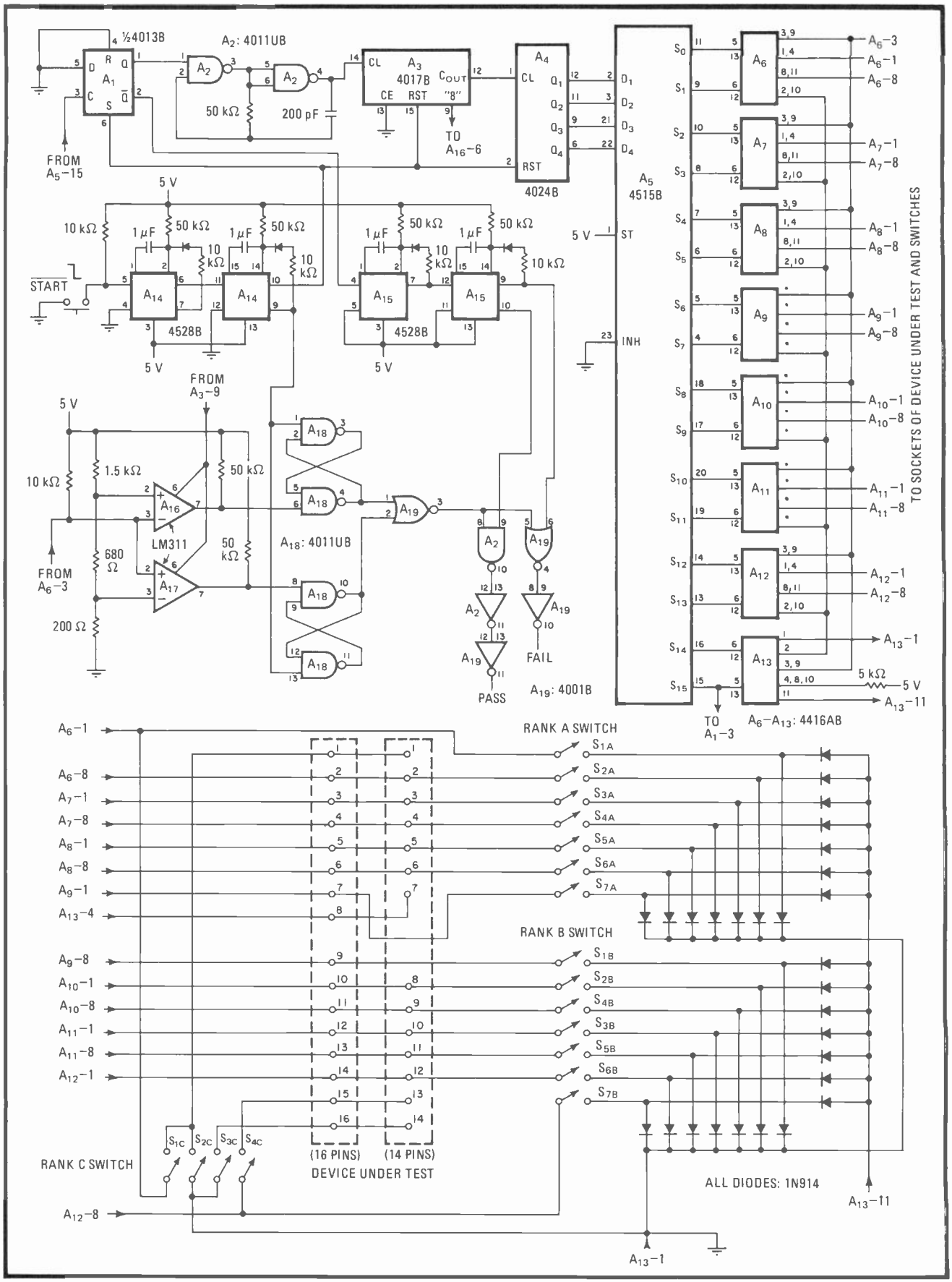
Stress test. Digital circuit transforms resistance change of strain-gage transducer R_1–R_2 into corresponding index without need for standard a-d converters. Number displayed represents $R_1 - R_2$ scaled to a factor, K, that is equal to 0.3425 fC.

C-MOS tester checks for assembly errors

by Joseph G. Gaskill
Solid State Scientific Inc., Montgomeryville, Pa.

Detecting most faults in complementary-metal-oxide-semiconductor devices due to errors in packaging or because of burnout while in actual operation, this tester can check virtually all the elements in the present C-MOS logic family. The unit needs only to perform a set of simple open and short tests at each pin of the device to quickly check for chip failures.

Assembly-related rejects and in-circuit failures are



Checking C-MOS. Tester checks for defects in C-MOS 4000 series devices. Device under test is placed in the appropriate test socket, the rank switches set as given in table, and the start button depressed. Test results appear as active-high signal at pass or fail output.

SWITCH SETTINGS FOR C-MOS TEST SET

Device	Switch rank A							Switch rank B							Switch rank C			
	1	2	3	4	5	6	7	1	2	3	4	5	6	7	1	2	3	4
4000B	■	■						■							■		■	■
4001B								■							■		■	■
4001UB								■							■		■	■
4002B						■		■							■		■	■
4006B		■						■	■						■		■	■
4007UB				■	■			■							■		■	■
4008B															■		■	■
4009UB												■			■		■	■
4010B												■			■		■	■
4011B								■							■		■	■
4011UB								■							■		■	■
4012B						■		■	■						■		■	■
4013B						■		■							■		■	■
4014B								■							■		■	■
4015B								■							■		■	■
4016B								■							■		■	■
4017B															■		■	■
4018B															■		■	■
4019B															■		■	■
4020B															■		■	■
4021B															■		■	■
4022B						■									■		■	■
4023B								■	■						■		■	■
4024B								■	■		■			■	■		■	■
4025B								■							■		■	■
4026B															■		■	■
4027B															■		■	■
4028B															■		■	■
4029B															■		■	■
4030B								■	■						■		■	■
4033B															■		■	■
4035B															■		■	■
4040B															■		■	■
4041UB								■	■						■		■	■
4042B															■		■	■
4043B												■			■		■	■
4044B		■													■		■	■
4046B														■	■		■	■
4049UB	■		■		■			■		■		■				■		
4050B								■		■		■			■	■	■	
4051B															■		■	■
4052B															■		■	■
4053B															■		■	■
4060B															■		■	■
4066B															■		■	■
4068B	■					■		■	■						■		■	■
4069UB								■							■		■	■

Device	Switch rank A							Switch rank B							Switch rank C			
	1	2	3	4	5	6	7	1	2	3	4	5	6	7	1	2	3	4
4070B								■							■		■	■
4071B								■							■		■	■
4072B						■		■	■						■		■	■
4073B								■							■		■	■
4075B								■							■		■	■
4076B															■		■	■
4077B								■							■		■	■
4078B	■					■		■							■		■	■
4081B						■		■							■		■	■
4082B						■		■							■		■	■
4093B															■		■	■
4160B															■		■	■
4161B															■		■	■
4162B															■		■	■
4163B															■		■	■
4401B						■		■							■		■	■
4402B						■		■	■						■		■	■
4404B						■		■			■				■		■	■
4411B						■		■							■		■	■
4412B						■		■							■		■	■
4416B						■		■							■		■	■
4426B						■		■	■		■				■		■	■
4428B						■			■		■				■		■	■
4433B						■		■	■		■				■		■	■
4441UB	■			■		■		■			■				■		■	■
4445B				■				■			■			■	■		■	■
4446B														■	■		■	■
4449UB	■												■		■		■	■
4502B															■		■	■
4510B															■		■	■
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4512B															■		■	■
4516B															■		■	■
4518B															■		■	■
4520B															■		■	■
4522B															■		■	■
4526B															■		■	■
4527B															■		■	■
4528B	■													■	■		■	■
4531B															■		■	■
4543B															■		■	■
4555B															■		■	■
4556B															■		■	■
4582B															■		■	■
4584B													■		■		■	■
4585B															■		■	■

predominately caused by or result in internal shorting of wires between leads or open bonds to device pads and packaged posts. The detection of these failures is relatively simple for C-MOS chips because each input and output port is connected to two diodes internal to the device, one forward-biased with respect to the positive supply voltage and the other back-biased with respect to the negative supply. Hence it is necessary only to check whether each diode is opened or shorted. This, in principle, is simple to do.

Most C-MOS devices have at least 10 active ports, however, and consequently it becomes a problem to detect failures in many diodes while performing the minimum number of measurements. The proposed solution arrived at for testing C-MOS devices having up to 16 pins is shown in Fig. 1.

Briefly, A_2 serves as a gated oscillator operating at 100 kilohertz for stepping A_3, the 4017 decade counter, when the start button is pressed. A_3 generates a strobe for circuit timing and also advances A_4, the 4024 binary counter, so that each location of the 4515 1-of-16-line decoder can be addressed.

The decoder sequentially steps once through A_6–A_{13}, the quad analog gates, each of which is wired as a double-pole, single-throw switch. The output ports of the 4515 can thus provide a voltage for testing the diodes at all pins of the device under test.

Any transmission-gate output port connected to a shorted diode will move low. Open diodes will cause the output to float. The results of each individual diode test are monitored by window comparator A_{16}–A_{17}. The comparator's output is then latched by A_{18} and passed into either the pass or fail gate at the output.

Switches S_{1A}–S_{7A}, S_{1B}–S_{7B}, and S_{1C}–S_{4C}, the so-called rank switches, which are connected to the test-socket pins, must be set accordingly to check the particular device desired. Required switch closures are presented in the table for all 14- and 16-pin 4000-series devices produced by Solid State Scientific Inc.

Note that the 28-diode matrix connected to the rank switches must be individually switched into the circuit of the particular device under test. The matrix is wired so that if there are any unused (inactive) pins in the device, the diodes will simulate the device's diodes; the open-short test may therefore be performed at each pin of the device without generating an erroneous response (that is, an open-circuit indication). □

What happens to semiconductors in a nuclear environment?

For designers who must select components to survive high-energy radiation, it's important to know how each type reacts

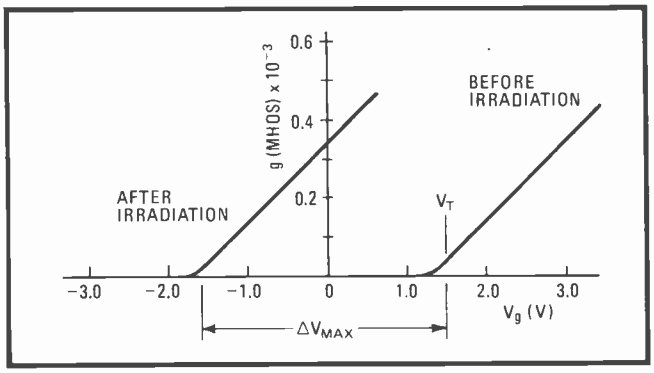
by David K. Myers, *Fairchild Camera and Instrument Corp., Mountain View, Calif.*

☐ Of all the many ambient conditions to which semiconductor devices are exposed, from a computer's air-conditioned room to under an automobile's hood, none is as demanding as the nuclear radiation encountered in certain military and space environments or in the nuclear industrial field. Unhardened digital electronic equipment can fail when exposed to ionizing radiation doses of as little as 10^3 rads (Si)—out in space, for example, in the Van Allen Belt—or to a neutron fluence of as little as 10^{11} neutrons per square centimeter—near a nuclear reactor, say. (Rads (Si) stands for roentgens absorbed dose in silicon, while a fluence is defined as the time integral of neutron flux.)

Anyone engaged in designing circuitry for use in such environments must be knowledgeable about their differing effects on different semiconductor technologies. Exposure to high-energy radiation introduces primary structural defects into semiconductor materials (and hence changes their electrical characteristics) in ways that depend partly on the duration and type of incident radiation and partly on that particular semiconductor material's resistivity, impurity types and concentrations, temperature, and carrier-injection levels.

The nuclear environments to be considered here are:

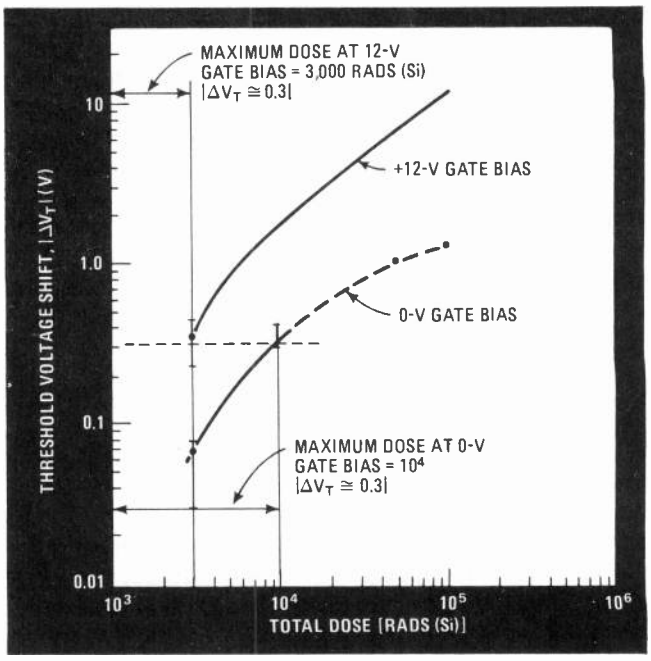
- Fast neutrons, which can permanently degrade gain in both bipolar and metal-oxide-semiconductor devices and increase the saturation voltage of bipolar transistors.
- Steady-state ionizing radiation (the total dose), which can increase leakage current in bipolar devices and alter threshold voltages in MOS and particularly complementary-MOS devices.
- The transient ionizing dose rate, which at a high enough level generates photocurrents in all reverse-biased pn junctions, causing changes of logic state in bipolar digital circuits and latch-up in C-MOS devices.



1. Radiation shift. In MOS and C-MOS devices, ionizing radiation alters gate turn-on voltage, changing the operating point radically. In the MOSFET curve shown, a threshold voltage change of almost 3 V is observed after exposure of the devices to ionizing irradiation.

Neutron effects

In general, it is only when neutron levels rise to 10^{10} to 10^{12} n/cm² (E = 10 kiloelectronvolts) that silicon devices start exhibiting changes in their electrical characteristics. The base transit time and the base width of a bipolar transistor are the main physical parameters affected by exposure to fast neutrons, as can be inferred from the degradation in current gain (h_{FE}). Modern semiconductor manufacturing methods measure neither of these parameters directly, but do control h_{FE} and the gain bandwidth product (f_t), from which base width can be deduced.



2. Radiated RAM. Threshold-voltage shifts are a function of radiation dosage and bias conditions for 4,096-bit n-MOS random-access memories. Units with gate bias fail at lower radiation levels than zero-biased units. A 0.2-to-0.3-V change in V_T induces failure.

TABLE 1: COMPARING THE RADIATION SUSCEPTIBILITY OF VARIOUS SEMICONDUCTORS

Radiation environment \ Semiconductor technology		Discrete bipolar transistors and J-FETs	Silicon controlled rectifiers	TTL	Low-power Schottky TTL	Analog integrated circuits	C-MOS	n-MOS	Light-emitting diodes	Isoplanar II ECL
Neutrons (c/nm^2)		$10^{10}-10^{12}$	$10^{10}-10^{12}$	10^{14}	10^{14}	10^{13}	10^{15}	10^{15}	10^{13}	$>10^{15}$
Ionizing radiation	Total dose (rads (Si))	$>10^4$	10^4	10^6	10^6	$5\times10^4-10^5$	10^3-10^4	10^3	$>10^5$	10^7
	Transient dose rate (rads (Si)/s) (upset or saturation)	–	10^3	10^7	5×10^7	10^6	10^7	10^5	–	$>10^8$
	Transient dose rate (rads (Si)/s) (survival)	10^{10}	10^{10}	$>10^{10}$	$>10^{10}$	$>10^{10}$	10^9	10^{10}	$>10^{10}$	10^{11}
	Dormant total dose (zero bias)	$>10^4$	10^4	10^6	10^6	10^5	10^6	10^4	$>10^5$	$>10^7$

Burnout by EMP

An electromagnetic pulse from a nuclear event can couple into a system's cables and antennas and create voltage/current spikes that may fuse the metalization on a semiconductor surface. Usually the interconnect system on a semiconductor device is a thin metal layer, only 10,000 angstroms or so thick, and will fuse at a current density of 10^6 amperes per square centimeter. Most integrated-circuit metalization stripe widths are designed to keep the current density below 10^5 A/cm^2 during normal operation, including worst-case testing.

EMP-induced burnout of semiconductor junctions is therefore a serious problem. But while it is a failure mode of semiconductor devices, it originates in the system design and not in semiconductor selection or reliability. The electromagnetic pulse must be shielded, filtered or shunted to ground.

Data available from Government laboratories and semiconductor manufacturers on semiconductors subjected to neutron irradiation indicates that double-diffused, epitaxially constructed integrated circuits, both digital and linear, will function within their original specification limits to neutron levels of 5×10^{13} n/cm^2 (E = 1 megaelectronvolt). This holds for diode- and transistor-transistor logic, as well as for low-power Schottky TTL. MOS circuits, whether n- or p-channel or C-MOS, are majority-carrier devices and not susceptible to neutron irradiation below 10^{15} n/cm^2.

The total ionizing dose

A steady state of ionization increases bipolar transistor leakage current most markedly in low-current, large-area devices. But even under worst-case conditions, these increased leakages are not enough to cause circuit failure at radiation levels below 10^5 rads (Si). Indeed, in many cases, bipolar integrated circuits have functioned well at levels in excess of 10^7 rads (Si). Tests run on DTL, TTL, and low-power Schottky TTL circuits reveal radiation-induced changes only above 10^6 rads (Si).

The effect of a total ionizing dose on MOS devices is more drastic. It permanently changes the crucial threshold voltage, V_T, which is applied to the gate of a MOS field-effect transistor to create the source-to-drain conduction path or channel. This change can be attributed to the buildup of a trapped positive charge in the gate-oxide insulator and to the creation of fast surface states at the interface of the silicon and silicon dioxide. The result is a marked shift in the operating point of a device (Fig. 1).

Recent radiation tests indicate that n-channel MOS dynamic random-access memories are very sensitive to ionizing radiation, having a nearly 100% failure rate at 3,500 rads (Si), regardless of manufacturer. For instance, the major failure mode of 4,096-bit dynamic n-MOS RAMs is the incidence of decoders stuck in the logic 1 state, which in turn is due to changes in threshold voltage that exceed the operating design tolerance.

Most current n-MOS test data is derived from these 4-k RAMs, but other large-scale integrated circuits like 16,384-bit RAMs, microprocessors, and similar complex n-MOS chips are also sensitive to continuous ionization, being manufactured according to similar design rules and processing. Failure threshold is 1,700 rads (Si) for 4,096-bit dynamic RAMs and 1,000 rads (Si) for n-MOS microprocessors.

Precise threshold voltage changes in n-MOS units are a function of dose and bias, as shown in Fig. 2. Under a normal +12-volt gate bias, shifts in V_T of 0.2 to 0.4 v have been observed at 3,000 rads (Si). Circuit analysis indicates that the n-MOS electrical designs will tolerate a change of 0.2 to 0.3 v in V_T without failing. Tests of MOS devices at zero gate bias (again, see Fig. 2) show they will fail only with the approximately 0.3-v shift in V_T caused by a dose of 10^4 rads (Si).

Radiation-induced shifts in threshold voltage similar to those described for n-MOS also occur with C-MOS semiconductors. The operating design tolerance $|\Delta V_T|$ is usually 1 v for commercial C-MOS products, indicating that a dose of 10^4 rads (Si) is required to cause failure. Actual cobalt-60 irradiations of Fairchild Isoplanar

TABLE 2: RADIATION SUSCEPTIBILITY OF EMITTER-COUPLED LOGIC

Data source	Northrop	Sandia	Fairchild
Pulsed ionizing radiation			
Narrow-pulse transient failure level	3×10^8 rads (Si)/s	no tests performed	$5-7\times10^8$ rads (Si)/s
Wide-pulse transient failure level	$1.1-1.4\times10^8$ rads (Si)/s	"	no tests performed
Permanent-damage failure level	not determined — greater than 1.5×10^{11} rads (Si)/s	"	10^{11} rads (Si)/s maximum level (flash X-ray equipment*)
Neutron/gamma permanent damage			
Mean neutron failure level	2.2×10^{15} n/cm^2 (1 MeV equivalent)	1×10^{15} n/cm^2 (1 MeV equivalent)	1×10^{15} n/cm^2 * (1 MeV equivalent)
Total gamma dose	6.6×10^6 rads (Si)	2.5×10^7 rads (Si)	10^7 rads (Si)*
Observed neutron failure-level range	$1.9-2.6\times10^{15}$ n/cm^2 (1 MeV equivalent)	1×10^{15} n/cm^2 * (1 MeV equivalent)	1×10^{15} n/cm^2 * (1 MeV equivalent)
Device type tested	MC1678L 4-bit counter	custom IC fabricated by TRW	Isoplanar II, ECL F100101, F100117, F100102, F100141 and kit parts
Transistor gain-bandwidth product (f_T)	2.0–2.5 GHz	1.5 GHz	4.5–5.5 GHz

*Maximum radiation exposure level; no failures were observed at this level.

C-MOS and other available C-MOS devices cause device failures at above 5×10^4 rads (Si).

If the C-MOS design margin for V_T is reduced for electrical performance reasons, then the radiation tolerance would be sacrificed. This is the case for certain C-MOS circuits with a V_T of about 0.2 V, which all fail at approximately 2,000 rads (Si).

In general, improved tolerance of ionizing radiation could be realized by use of hardened oxide manufacturing techniques and circuit design modifications. However, though increasing the circuit V_T operating tolerance would raise the ionizing radiation failure threshold, it would also adversely affect the power, speed, component density, chip size, and yield.

Loss of memory and latch-up

A transient dose of ionizing radiation creates a photocurrent in any reverse-biased pn junction, such as the collector-base junctions of transistors and the pn junctions used for isolation in standard bipolar integrated circuits. These photocurrents can be large enough to cause digital circuits to change state, from a 1 to a 0. But though they may change the content of memories, they cause no permanent failure. For some programs, logic upset is acceptable, but survival at the specified transient radiation dose rate is required. Tests show that DTL, TTL, and low-power Schottky TTL devices will change logic state above a dose 5×10^6 rads (Si)/s and survive 10^{10} rads (Si)/s.

These transient photocurrents can induce another phenomenon, known as latch-up, in those types of IC that can be driven into silicon-controlled-rectifier action or second breakdown. In this situation, they force the device to latch into one state and remain there until the power is interrupted or the circuit destroys itself.

Such radiation-induced latch-up has not been observed in digital or linear bipolar ICs employing double-diffused epitaxial fabrication methods and operating within specifications. Fairchild has had over 140,000 low-power DTL devices tested by outside contractors to levels of approximately 10^{10} rads (Si)/s without a true latch-up failure. Nor has any been observed in TTL, Schottky TTL, or bipolar operational amplifier and comparator circuits.

Latch-up of triple-diffused ICs does occur. But this technology has not been used to manufacture commercially available circuits for over five years.

MOS resistance to latch-up, on the other hand, varies with the process used. The problem has not been found to afflict n-MOS devices, which lack the fourth junction necessary for SCR action. But junction-isolated C-MOS ICs, which have that fourth junction, have been observed to latch up at dose rates as low as 3×10^8 rads (Si)/s. When operated at 5 V in the latch-up state, C-MOS devices return to normal operation after the power has been interrupted. But when operated at 10 V, they fail catastrophically because of latch-up.

It is worth noting that the latch-up dose-rate level of C-MOS devices varies with the manufacturer, device function, and chip design: there is a very uniform susceptibility to latch-up for devices with the same function from the same manufacturer.

For bipolar devices, it is different. The radiation tolerance of a generic bipolar family can be determined by testing sample parts of the family, since circuit design rules and manufacturing processes are constant throughout. This theory has been tested and verified on low-power Schottky TTL ICs manufactured by Fairchild Semiconductor.

Low-power Schottky parts made by other IC firms have been tested using the same radiation criteria. These results, with the Fairchild data, add to the overall confidence that a specific bipolar part type has a specified radiation tolerance irrespective of its source.

Only limited testing has been reported on the radiation tolerance of high-speed emitter-coupled logic. A data summary of ECL failure threshold levels for various radiation environments is presented in Table 2. Nevertheless, a preliminary comparison of ECL with a number of other types of ICs and discrete semiconductor devices (Table 1) indicates that ECL easily excels them all in radiation tolerance. □

Easy impedance matching opens the digital door to analog delay lines

Widely available new models, designed for simple interfacing, can replace complex arrangements of logic gates; a few basic rules are the guide to practical implementation

by Larry Garde, *Magnetic Peripherals Inc., Minneapolis, Minn.*

☐ A new breed of delay line is attracting digital designers, for the units are designed to minimize the interface impedance-matching considerations that proved so resistant to solution in earlier attempts at logic applications. Moreover, the new lines boast incremental tappings and come in the familiar 14- and 16-pin dual in-line packages, rather than the bulky, oddly shaped packages of earlier models. Thus, it is much easier to make use of their inherent large bandwidth to process such discontinuous-boundary waveshapes as digital and switching signals.

A standard product

The tapped delay lines in DIPs are widely available and can replace complex arrangements of logic gates. They can drive or be driven by transistor-transistor logic, emitter-coupled logic, and other digital families that are capable of delivering sufficient drive current. Happily, a knowledge of only a few basic rules is required for practical implementation of these devices.

Several manufacturers now make what may be regarded as the industry-standard tapped delay line. The table gives typical characteristics for versions that introduce a signal delay of 10 to 150 nanoseconds. No matter who the maker or what the delay time, cost is about $12 apiece, dropping to $3 in lots of 1,000 or more.

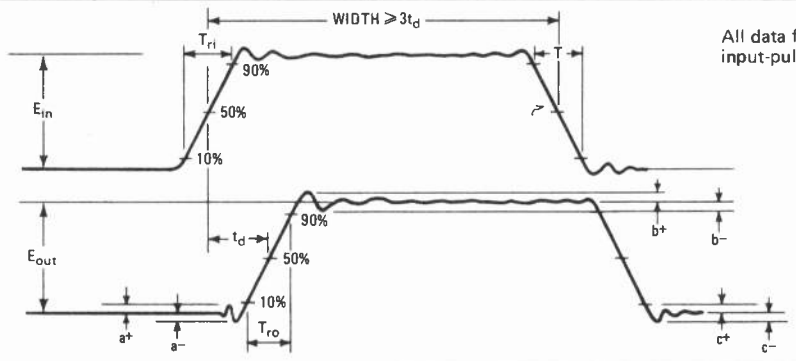
Standard delay lines have either a 50- or 100-ohm characteristic impedance, suited for ECL or TTL respectively. They require terminating resistors, which first were mounted on the printed-circuit board, external to the delay line. However, this arrangement often created more problems with capacitive loading, reflections on the line, and so on. Now many of the standard delay lines have built-in terminators.

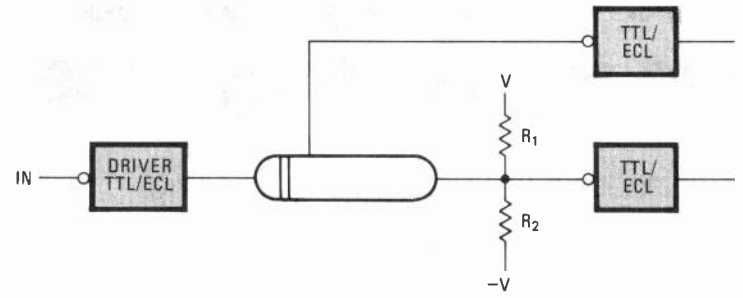
For the units that still require add-on termination, a single resistor or the Thevenin-equivalent (two-resistor) arrangement may be used. The two-resistor termination is designed to reduce the current load on the unit driving the delay line.

Delay lines may be customized to provide a desired set

TYPICAL DELAY-LINE CHARACTERISTICS

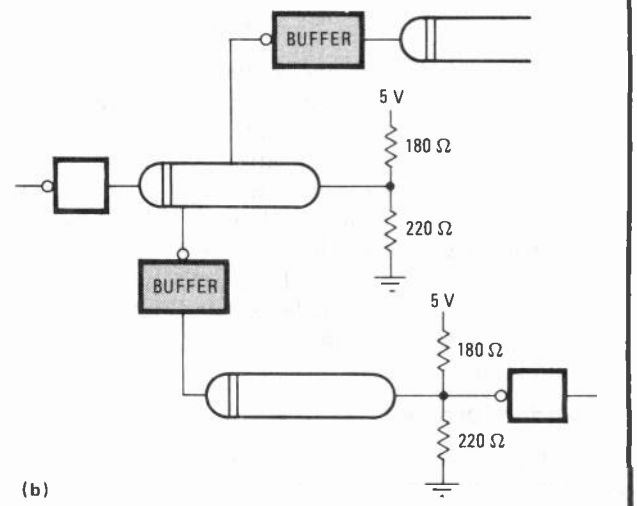
t_d Total delay (ns)	t_t Tap delay (ns)	Maximum rise time (ns)		Dc resistance input to output (Ω)	Distortion (%)			Impedance (Ω)	Total attenuation (%)	Total temperature coefficient delay (ppm/°C)
		Input T_{ri}	Output T_{ro}		Prepulse (a)	Pulse (b)	Postpulse (c)			
10 ±1.0	1.0 ±0.25	3.0	5.0	1.0	± 13	± 13	± 13	100 ±10% 50 ±10%	2	100 (0°–85°C)
20 ±2.0	2.0 ±0.25	3.5	7.0	1.0	± 12	± 12	± 12	↓	↓	↓
30 ±2.0	3.0 ±0.3	3.5	7.3	1.5	± 10	± 10	± 10	↓	↓	↓
50 ±2.5	5.0 ±0.5	5.0	11	2.5	± 15	± 15	± 15	↓	↓	↓
100 ±5.0	10 ±1.0	6.5	23	1.4	± 13	± 13	± 13	↓	↓	↓
150 ±7.5	15 ±1.5	8.0	30	1.7	± 13	± 13	± 13	↓	↓	↓





(a)

Power	+V	+5	−5	−2	+2
	−V	0	0	−5	−3.2
TTL	R_1 (Ω)	180	—	—	—
	R_2 (Ω)	220	—	—	—
ECL	R_1 (Ω)	—	120	50	50 Ω to ground only
	R_2 (Ω)	—	82	—	—



(b)

1. Termination. Two-resistor, or Thevenin-equivalent, arrangement (a) reduces the load on TTL or ECL drivers while providing 99-ohm termination for a 100-ohm delay line (TTL-driven) or 50-ohm termination for a 50-ohm line (ECL-driven). When cascading delay lines from intermediate taps, buffers are required (b), since it is necessary to avoid unwanted reflections caused by mismatching.

of tappings, but they are readily available in a wide range of delays varying from 10 to 500 ns. The taps are usually spaced at T/10 increments, where T is the overall delay at the line. The overall delay accuracy to be expected for lines having a specified delay greater than 50 ns is 5%, with a tap accuracy of 10%. For lines of less delay, overall accuracy varies from 7% to 10%, and tap accuracy varies from 10% to 25%.

The overall line errors are not cumulative at the taps, however. Thus, if a 100-ns line has been designed to have 10 equally spaced taps, the actual delay may vary from 95 to 105 ns, but each tap will be calibrated to within ±1 ns of its 10-tap increment.

The latest development in delay lines in DIPs is one with built-in TTL drives, TTL interface chips driving each output pin, and internal terminating resistors. While such a design eases interface problems, its quantity cost is about three times that of the standard, noninterfaced types. Thus it pays to know the ground rules for interfacing the standard delay lines.

Four considerations

The questions that must be answered when designing digital applications of delay lines are often more practical than theoretical. At least, they are of a sort whose answers are not directly provided by the manufacturer. Fortunately, learning the design guidelines is not difficult, and other information can be gained by careful measurements and experience.

To begin with, TTL and ECL present somewhat different interfacing problems. Also, certain precautions must be taken when cascading delay lines. Third, it is necessary to find the equivalent capacitance produced by external wiring across a delay line's tap in order to determine the loading effect, or alternatively it is necessary to determine the maximum length of the external wiring connecting a tap to a logic element. Finally, other characteristics of the standard delay lines, not listed in the table, may be design considerations.

The proper interfacing

One or more taps of the delay line usually face the inherently asymmetrical input circuit of a TTL device, yet this logic element has a minimal effect on delay-line loading. During the logic 1 input condition, a TTL gate presents an impedance above 50 kilohms. This impedance is so far in excess of the 100-Ω terminating impedance of the delay line that it causes little loading. During the logic 0 condition, input impedance is about 4 kΩ, so there is virtually no loading. The Schottky-TTL gate's input impedance is about 45 kΩ during the logic 1 state and about 2.8 kΩ during the logic 0 condition.

Asymmetrical loading will become a problem when more than three Schottky gates or more than four standard TTL gates are driven by the delay line. Three Schottky loads will increase the signal's rise and fall times about 2% at the output of a 100-ns delay line, and four standard loads will increase the times about 10%.

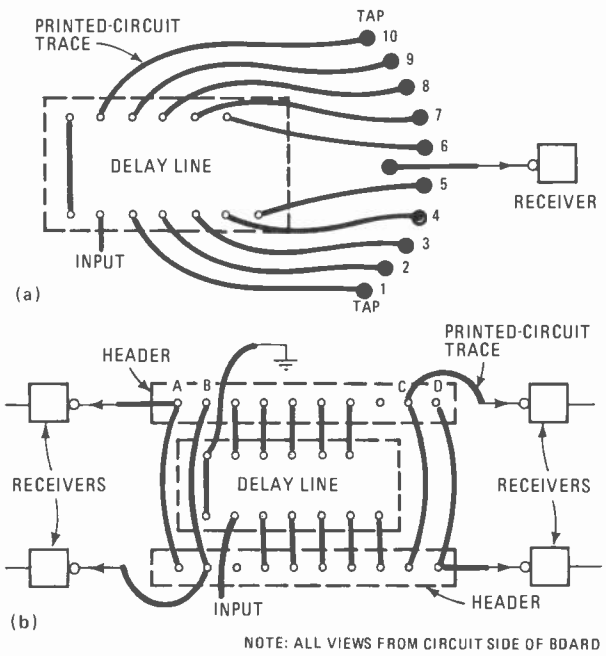
When terminating a delay line in any TTL application, the best approach is a 180-Ω resistor and a 220-Ω resistor connected in series between the positive supply and ground with their junction connected to the input of the delay line (Fig. 1a). This method limits the load current of the delay-line driver to 30 milliamperes, and it provides a 99-Ω termination for the delay line.

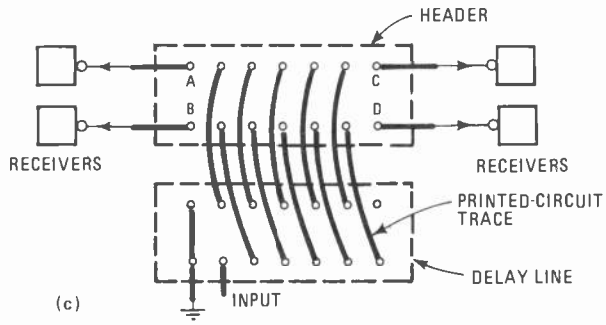
For ECL powered by a single −5-volt power source, 82-Ω and 120-Ω resistors configured the same way provide suitable termination. When the ECL is powered by such dual supplies as −5 v and −2 v, a single 50-Ω resistor between the output of the delay line and the

Making connections

The physical connections between a delay line and any logic element pose no particular problems, but there are choices to be made. An inexpensive method is first to bring all taps to plated-through holes on the printed-circuit board and then to connect flexible jumpers (not shown) from each gate input to the desired tap point. The holes can be arranged in a semicircle, as shown in a.

Two other methods use terminal blocks, or headers, installed next to the delay line (b and c). There is easy connection between the header's solder pins and each tap by pc-board traces. While more expensive than the first method, these approaches are more convenient from a production standpoint, save board space, and reduce stray capacitance because of their shorter leads.





−2-v source will do. When using +2 v and −3.2 v, a single 50-Ω resistor between the delay line's output and ground will suffice.

When it comes to driving a standard 100-Ω delay line, the choice is clear. Buffered Schottky-TTL gates can handle more current and have shorter propagation times than standard TTL, and using these gates is the best choice. Tipping the balance in their favor are their high current capability and a cost below that of ECL. It is best to use ECL elements to drive 50-Ω delay lines.

The trick in cascading

A related termination problem is the cascading of delay lines. Cascading results in an increase in the output signal's rise and fall times according to:

$$t_r = (t_{in}^2 + t_1^2 + t_2^2 + \ldots t_n^2)^{1/2}$$

where t_r is the total rise or fall time, t_{in} is the rise (or fall) time of the input signal, and $t_1 \ldots t_n$ is the respective rise (or fall) time of each delay line. Note that the rise and fall times of any individual delay line vary directly as its length.

When cascading delay lines from intermediate taps, a buffer (Fig. 1b) will prevent unwanted reflections caused by mismatch. The buffer removes the loading effect without causing any signal distortions.

Determining maximum lengths for external wiring and the related capacitance across a tap can be a simple job. The maximum wire length between a tap and a gate can be found if the impedance of the delay line and the delay time are known. For the purposes of illustration, assume a microstrip configuration where the foil (trace) is separated from a ground plane by 0.03 inch of pc-board material. The capacitance of the wire under these conditions is known to be 2 picofarads per inch.

Some calculations

The capacitance across a given delay line of impedance Z_o and delay t_d is given by:

$$C = 100\, t_d/Z_o$$

where C is given in picofarads if t_d is given in nanoseconds, and Z_o is measured in ohms.

For a typical case where t_d = 10 ns and Z_o = 100 Ω, C will be 10 pF. A 0.5-in. wire of the type described above presents a 1-pF load to the delay line. This capacitance, which is 10% of C, would become significant as viewed by any of the 10 taps along the line.

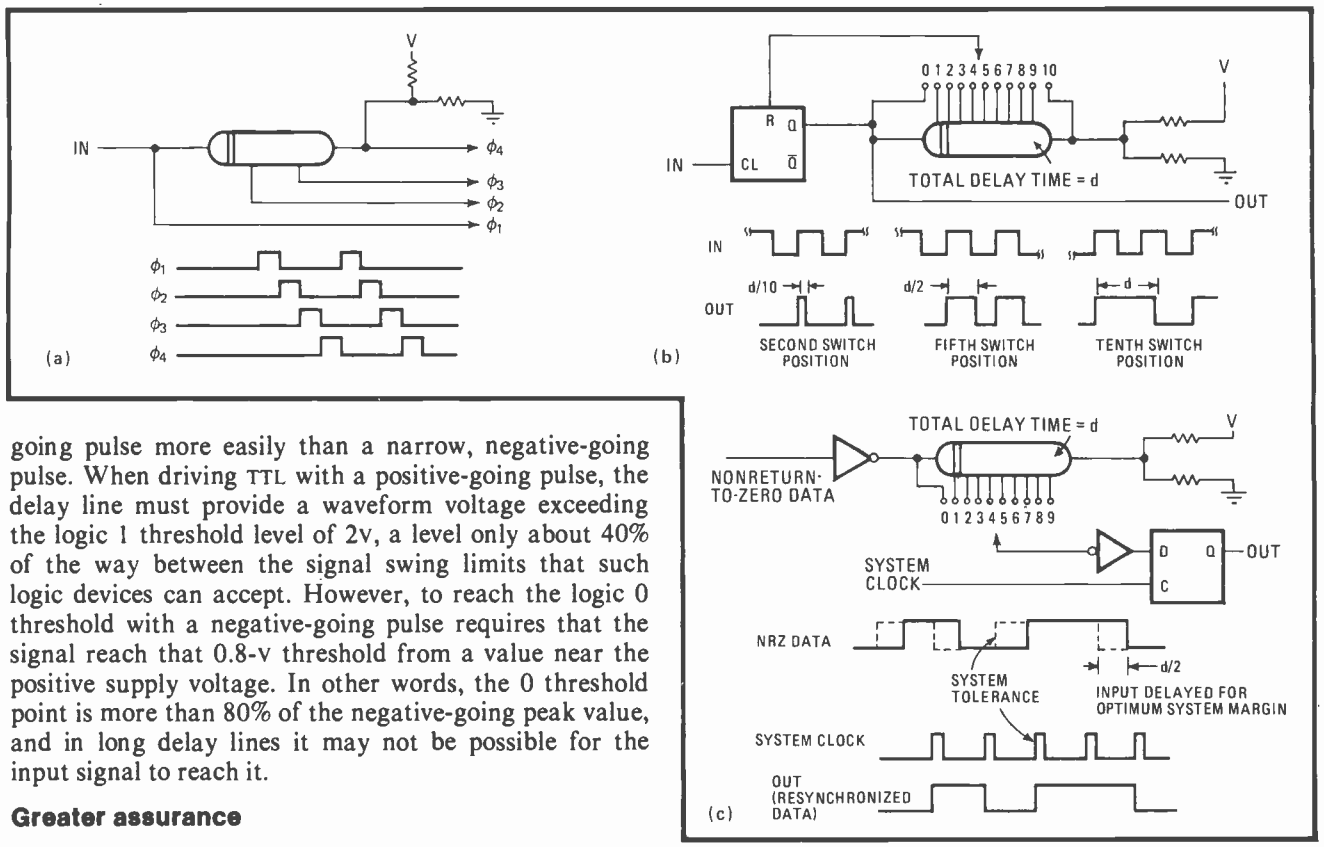
Similarly, a 150-ns delay line would have an equivalent capacitance of 150 pF. In this case, a wire as long as about 7 in. (a 14-pF load) could be connected to a tap before response would be noticeably affected.

There are several other points to consider when designing analog tapped delay lines in DIPs into digital applications. These arise from delay-line characteristics that show up in use.

Applying a voltage at any point on a delay line has no effect on its delay properties if the delay line does not contain a ferrite core. Of course, the voltage may itself affect the input signal or its driver adversely.

Temperature changes have a relatively small effect on delay time, amounting to about 2% over the range from 0°C to 85°C. However, the effect on rise and fall times over the same range amounts to more than 15%. These figures were determined experimentally from tests on a 100-ns delay line.

The standard delay line handles a narrow, positive-



2. Applications. Analog delay lines have large bandwidth; thus they may be used to process digital waveforms. A basic phase-delay circuit (a), a pulse shaper (b), or a data resynchronizer (c) may be constructed often more simply than all-digital networks.

going pulse more easily than a narrow, negative-going pulse. When driving TTL with a positive-going pulse, the delay line must provide a waveform voltage exceeding the logic 1 threshold level of 2v, a level only about 40% of the way between the signal swing limits that such logic devices can accept. However, to reach the logic 0 threshold with a negative-going pulse requires that the signal reach that 0.8-v threshold from a value near the positive supply voltage. In other words, the 0 threshold point is more than 80% of the negative-going peak value, and in long delay lines it may not be possible for the input signal to reach it.

Greater assurance

Using a positive-going pulse where possible provides greater assurance that the output pulse will have sufficient amplitude to drive the gates. Moreover, the variation of the pulse width at the delay line's output taps will be minimized because the effective rise and fall times as measured at the 40% point are less than at the 80% point.

Signal degradation is no problem with ECL, because such logic elements supply high drive currents. Thus the length of the delay line will minimally affect the waveform properties.

The pulse frequency has an effect on the delay line's output only if the frequency is so high that a given pulse is distorted because of reflections on the line caused by a previous pulse. The width of the narrowest pulse that can be delayed by a particular delay line and still achieve at least 85% of its original amplitude can be shown to be:

$$t_p = t_R + \frac{(t_f - t_r)}{2}$$

where t_p is the input signal's pulse width measured between its 50% amplitude points, t_R is the delay line's rise time measured between the 10% and 90% amplitude points, t_f is the input signal's fall time measured between the 90% and 10% amplitude points, and t_r is the input signal's rise time measured between the 10% and 90% amplitude points. When t_f and t_r are equal, the minimum width of an input pulse must of necessity be equal to the delay line's rise time if it is to pass to the output relatively undistorted.

Delay lines may be put to good use in any area of logic circuit design where timing relationships are important or where the time interval involved is less than the system clock period. Thus, phase-delay circuits, pulse formers, and data resynchronizers are perhaps best implemented with a delay line. Examples of these circuits are shown in Fig. 2.

Simpler solution

The fact that the delay line was conceived for analog applications does not impede its usefulness in these digital applications. For example, the all-digital solution to the simplest circuit of Fig. 2, the phase-delay circuit, will be far more complex than need be. To obtain the total delay time required, either the delay time through many gates will have to be used, or else a clocked digital shift register arrangement will be needed.

As clock times get shorter, it will become necessary with either method to consider individual logic-gate propagation times. The futility of using such circuits will soon become apparent. For example, a standard 7400 TTL inverter has a typical propagation time of 10 ns, but a maximum of 20 ns. Therefore, the total propagation time through a string of such gates is almost impossible to calculate accurately even with the several excellent approximation equations that exist. If a clocked shift register is used instead of the delay line, the timing problems do not disappear, and, in addition, the circuit becomes complex.

This is a perfect example of where a delay line with selectable taps should be used. The all-digital solutions to the other two circuits present similar problems, so delay lines are the best route for similar reasons. □

Why switching power supplies are rivaling linears

Use of power transistors instead of a bulky transformer keeps efficiency high, size small, and power consumption low

by Malcolm Burchall, *Gould Inc., Electronic Components Division, El Monte, Calif.*

☐ Today's switching regulated power supplies are beginning to compete with linear types for the system designer's vote. They certainly deserve it if efficiency, small size, and low power consumption are what he wants most. And sometimes, in the context of a particular system's overall requirements, they may still be the better choice despite their greater noise, slower transient response, higher ripple, and generally higher price.

The virtues of the switching power supply stem from its smaller size. Its vices, on the other hand, stem from what makes that smaller size possible: the substitution of a high-frequency switching system based on power transistors for the bulky 50-to-60-hertz input transformer of the linear supply.

Approximately 80% of the linear supply's bulk is accounted for by three components: the input transformer, the reservoir electrolytic capacitors, and the heat sinks (Fig. 1). The transformer provides input/output isolation and reduces the relatively high input voltage to a level more nearly matching the required dc output level. The reservoir electrolytic capacitors perform two functions: they store enough energy to keep the output in line with the specifications in the event of short interruptions in the input, and they filter the raw, rectified dc from the rectifiers to an acceptable level. The heat sinks are needed to cool the power-dissipating components (rectifiers and series-pass transistors).

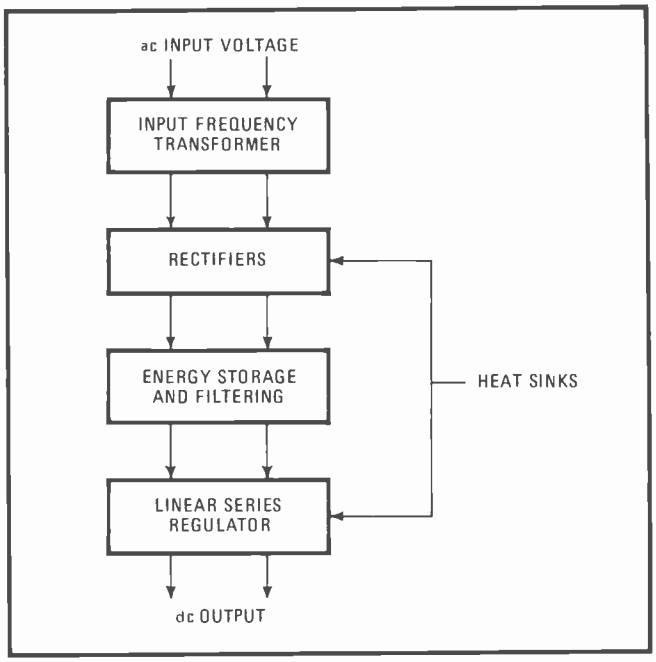
In the switching regulated power supply, most of the bulky components are replaced by solid-state circuits (Fig. 2). The switching system uses power transistors that turn on and off at rates of 20 kilohertz or more, the ratio of their on to off time being determined by a detector-amplifier configuration. This high-frequency operation allows smaller components to be used for the energy-storage capacitor, rectifiers, and filtering network. Being small, all these elements dissipate less heat and therefore need less—sometimes nothing—in the way of heat sinking than their larger linear counterparts.

Efficiency, size and weight

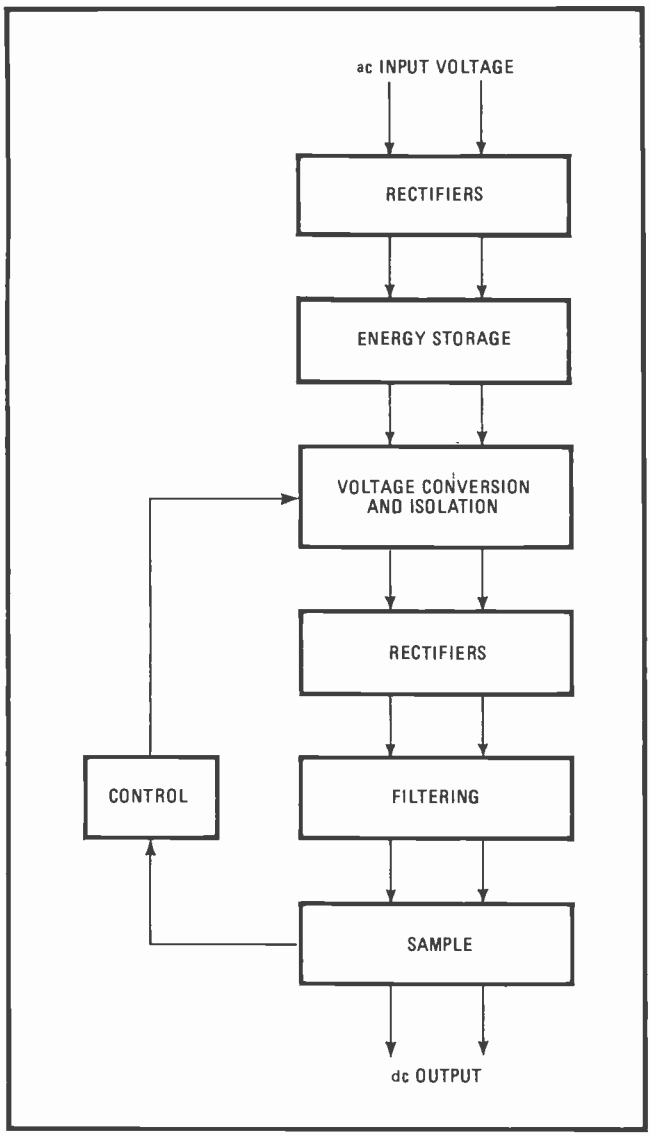
All other things being equal, then, linear power supplies have lower efficiencies. The usual efficiency for a good linear under nominal operating conditions is about 50%, and even the best of the new high-efficiency linears achieve only 53% to 56%.

Switchers, on the other hand, typically have 75% efficiencies, with some claims as high as 85%. To provide an output of 100 watts, a 133-w input is required of a switcher, while 200 w, at least, would be needed for a linear. The linear supply's efficiency is also highly dependent on the input line voltage, unlike the efficiency of the switcher, which is considered a theoretically lossless pulse-width-modulated device. As such, it acts as a dc-to-dc transformer that keeps output power constant by compensating for an increase in input voltage by a decrease in input current.

Another consideration is power loss density, or the power dissipation of a given group of components expressed in terms of their volume. For similar types of equipment, the maximum power loss density is determined by the temperature rating of the components used, the ambient temperature, and the method of heat extraction used (convection or forced cooling). Theoretically, this means that a switcher producing 100 w of output power with an internal loss of 33 w can be one third the size of a linear power supply that has an



1. Conventional. Sizeable linear power supply consists for the most part of large input transformer, bulky electrolytic capacitors, and large heat sinks for the rectifiers and regulator.



2. Competition. In switching supplies, solid-state circuits replace the large linear supply components. High-frequency operation makes it possible to use smaller, yet costlier, devices that fit in a tighter package, dissipate less heat, and yield higher efficiencies.

internal loss of 100 W for the same output.

In terms of power per unit weight, the average linear unit delivers 10 to 12 watts per pound, whereas switchers can provide 25 W/lb or even 50 W/lb if convection-cooled. In terms of power per unit volume, even a high-performance linear provides only ½ watt per cubic inch, while the average switcher puts out up to three times as much: 1 to 1½ W/in.^{3} With fan cooling, as much as 2½ W/in.^{3} is achievable in switching units, while very high-performance, military-specified units can reach densities as high as 3 or even 4 W/in.^{3}

In view of their comparative efficiency, size, and weight, switchers seem to have the edge on linears. The price picture is less clear.

The true cost

In the low-power, high-voltage range, linear supplies still cost less than the switching types. For an output voltage of 5 V, also, they are almost invariably cheaper up to 100 W, but switchers are almost invariably cheaper above 200 W. However, the specifier should remember that the true cost to a system of the power supply unit includes all the other components—fans, heat sinks, and so on—that may be required to enable the system to function at its optimum level. And this kind of overhead is heavier for linears.

As they increase in power, switching units become less expensive in terms of dollars per watt (Fig. 3). And with an increase in output voltage, which has little effect on linear pricing, they cost still less—a 200-W switcher at 24 V sells for less than a 200-W model at 5 V.

In the future, moreover, as the technology of switching power supply design matures, prices are bound to drop. Linear power supplies, on the other hand, being long past the developmental stage, are more likely to rise in price as the cost of their materials and labor goes up.

Performance

As always, the goal is to pay only for those performance factors needed in a given application. For instance, a designer who needs a very-low-noise 500-W supply must put up with the higher price and inefficiency of a linear unit. But if a small, highly efficient 50-W supply is required, then only a switcher will do, despite its higher price and higher noise.

Above a 5-V output, the efficiency gap between the 75% switcher and the 50% linear begins to narrow, so that at higher voltages some switchers and linears are competitive. But it is rare to find a linear that will work below a 100-V line input unless it has been specially designed to do so—and that would be at an even greater sacrifice in efficiency.

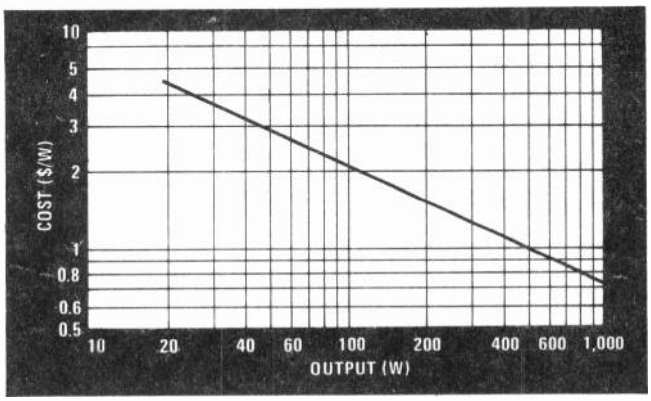
Switching units cover a wider range of line voltage conditions and accordingly are better protected than linears against brownouts. They normally regulate within a specification of a ±20% change in line voltage, whereas linear units are typically restricted to regulation within a ±10% change in line voltage.

The storage capacitor

Another aspect of performance is the switcher's ability to sustain a missing cycle in the line voltage. This is because its efficiency is not dependent on the voltage level of its energy-storage capacitor. That voltage can be at a relatively higher level than in a linear supply, where maximum efficiency is achieved by specifying the voltage on the storage capacitor at a level just above that of the output voltage.

Specifying this capacitor for the switcher is a simple matter because of the well-known relationship between the energy a capacitor can store and its size. Since this energy is proportional to CV^2, the same energy can be stored in a capacitor of 1/100 the size, if the voltage is increased by a factor of 10. In linear supplies, various schemes to store the energy can be used, but they usually require an auxiliary higher-voltage capacitor to store the extra energy for dumping into the normal reservoir capacitor when necessary. The extra capacitor makes the unit even bulkier.

Further aspects of performance affect the total error band. Under this head come those design parameters and



3. What price power? The larger their power output, the less expensive switching power supplies become in terms of their cost per watt. The graph assumes 100-quantity price and middle-of-the-road specifications for fully encased switching units.

TRADEOFFS IN CHOOSING A SWITCHING OR LINEAR REGULATED POWER SUPPLY

Parameter	Switching power supplies	Linear power supplies	Remarks
Volume/watt	excellent	poor	approximately 3:1 switcher-to-linear advantage
Weight/watt	excellent	poor	approximately 3:1 switcher-to-linear advantage
Power levels	unlimited in practice	not normally above 500 W	switcher has less waste heat; higher power is possible
Noise	acceptable	excellent	linear not always better — care in design required
Versatility	excellent	good	switcher has wide line-voltage tolerance and brown-out protection
Error band	acceptable to good	acceptable to excellent	depends on the amount of ripple noise and transient response
Reliability	acceptable to excellent	acceptable to excellent	depends on quality of design and components

the component ratings that between them set the tolerance level of the supply's output-voltage within a plus and minus band.

Transient response, ripple, temperature stability, setting capability, load regulation, and line regulation, all contribute to the total error band and are useful criteria for choosing between linear power supplies and switching power supplies.

In recovering from a momentary transient, switching units are on the order of 10 to 20 times slower than linears. A linear recovers in tens of microseconds, while it takes a switcher hundreds and sometimes even thousands of microseconds to recover. For rates of change of load current slower than 0.1 ampere per microsecond, transient amplitude deviations become detrimental for the switcher, producing deviations on the order of 1% to 2% per 10% of load change, whereas linears produce negligible deviations because of their faster response time. On the other hand, for very fast rates of change of load current, in excess of 1 A/μs, the output inductance of the power supply becomes the limiting factor, and here switchers can actually be better than linears. In these circumstances, the length of the power leads to the load and local decoupling at the load normally control the transient voltages seen by the load.

It is to be noted, though, that in digital systems, typically one logic circuit turns on as another turns off, so that the average load remains fairly even. The transients caused by these relatively minor load variations are small in amplitude and so of little consequence in power supply choice.

The switching functions within a switching power supply create an inherent ripple that is normally worse than in linears. That has always been the switcher's flaw. However, the ripple has a limited effect on power supply choice, since it is usually buried in the total system noise. Most digital circuits can tolerate a total error band of at least $\pm 5\%$, which compares favorably with the $\pm 0.5\%$ ripple commonly observed in switchers. The usual industry standard for switching power supplies is 50 mV or 1% peak to peak.

As far as temperature stability and load- and line-regulation and setting-capability tolerances are concerned, these are functions of component quality and of the design techniques used in both the switcher and linear supplies. No basis for comparison between switchers and linears exists here.

The same can also be said of current limiting. Both linears and switchers contain current-limiting circuitry and are fairly well protected against that hazard.

However, the two kinds of supply differ in the way they fail in response to excessive output-voltage variations. In this situation, linears normally have a catastrophic effect on their loads because they end up in an overvoltage condition. Still, it is easy enough to design an overvoltage crowbar circuit for them. This circuit consists of a threshold device that senses when an output overvoltage occurs and at once connects a high-current, fast-acting circuit, or crowbar (usually a silicon controlled rectifier) across the output terminals. Switchers, on the other hand, normally tend to fail downwards to an undervoltage condition. For those cases where they may end up in an overvoltage condition, a protective circuit for shutting them down can be provided that operates at much smaller currents than in linears.

To sum up, then, in terms of the total-error band, the choice between a linear and a switcher is a hard one, even with the latter displaying the worse ripple.

Switch-on surges

There is a tendency to think that line-current switch-on surges created by switchers are much worse than those created by linears. Actually, the switch-on surge in a switcher is usually confined to the first one or two charging current pulses, whereas in a linear, the switch-on surge current required to demagnetize the transformer core can last for as many as 20 pulses if the 50–60-Hz transformer is switched off and switched on again at the worst possible phase relationship. With the large switchers, soft-start circuits are provided that spread the current over several smaller pulses rather than the just one or two charging pulses. This makes the switchers even more attractive for tackling the surge problem.

Finally, for both the linear and the switcher, the sole criterion as far as radio-frequency- and electromagnetic-interference tolerances are concerned is whether either supply can meet typical international specifications such as the VDE 0875 EMI and RFI Specifications. □

Standard symbols let designers grasp logic operation quickly and easily

ANSI Y32.14 specifies set of symbols for clearly depicting logic, from gates to systems

by Bill King, *Hewlett-Packard Co., Santa Clara (Calif.) Division*

☐ The more complex integrated circuits become, the greater the detail in which designers and technicians need to understand their workings. To give them that information at a glance, manufacturers must depict the logic operation of their chips clearly and concisely.

In 1973, therefore, the American National Standards Institute approved and published ANSI Y32.14, which set the logic-symbol specifications for most devices—notably gates, flip-flops, and counters—and for systems containing them. But few users are familiar with the standard, because so far it has been adopted by only two manufacturers—by Hewlett-Packard Co. and, to some extent, by Texas Instruments Inc. Nonetheless, since ANSI does set standards for IC makers, its symbolism is likely to become widely accepted.

ANSI Y32.14 specifies:

- Definitions for the basic logic elements.
- Logic symbols, which show the defining shapes corresponding to the logic function performed.
- Qualifiers, which consist of letters, numbers, or arrows placed inside the logic-device symbol to indicate its logic function or special properties.
- Indicators, which show primarily if the input and output are active high or low.
- Dependency notation, which defines the logic-state relationship between the inputs required to activate the device.
- Control and contiguous blocks, which integrate with gates, flip-flops, and other elements to form shift registers, counters, and other commonly used devices.

TABLE 1: BASIC LOGIC ELEMENTS

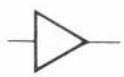
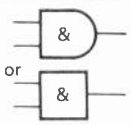
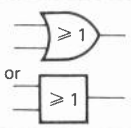
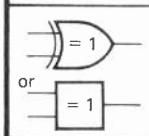
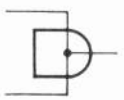
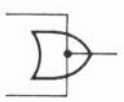
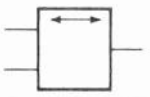
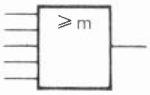
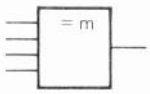
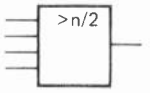
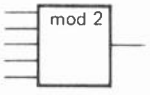
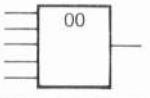
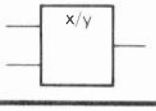
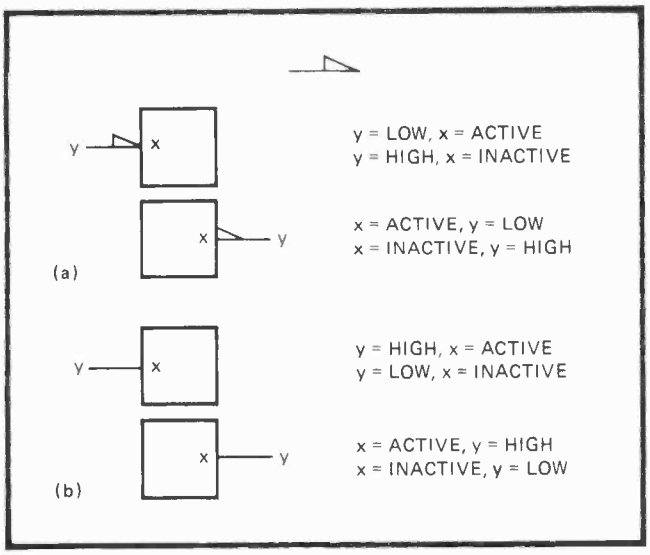
Symbol	Function	Description
	amplifier	The output will be active only when the input is active (can be used with polarity or logic indicator at input or output to signify inversion).
	AND	The output will assume its indicated active state only when all its inputs assume their indicated active levels.
	OR	The output will assume its indicated active state only when any of its inputs assume their indicated active levels.
	exclusive-OR	The output will assume its indicated active level if, and only if, only one of the inputs assumes its indicated active level.
	wired-AND	This is a connection of outputs of two or more elements that are joined together to achieve the effect of an AND function.
	wired-OR	This is a connection of outputs of two or more elements that are joined together to achieve the effect of an OR function.

TABLE 2: SELECTED QUALIFIER DESIGNATIONS

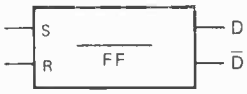
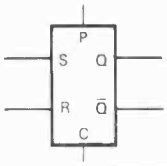
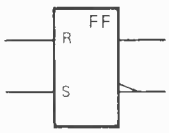
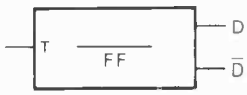
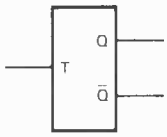
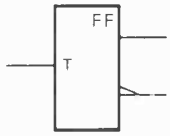
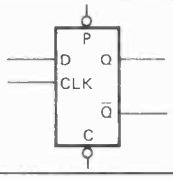
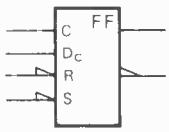
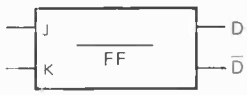
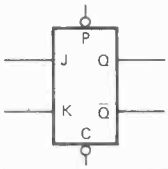
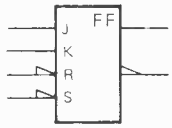
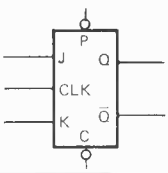
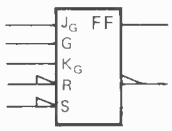
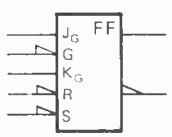
Symbol	Description
	Bilateral switch: a binary-controlled circuit that acts as an on-off switch to analog or binary signals flowing in both directions.
	Logic threshold: output will assume its active state if m or more inputs are active.
	m and only m: output will be active when m and only m inputs are active (for example, exclusive-OR).
	Majority function: output will be active only if more than half the inputs are active.
	Odd function: output is active only if an odd number of inputs are active.
	Even function: output is active only if an even number of inputs are active.
	Signal-level converter: input levels are different from output levels.



1. Polarity convention. Indicator symbol (top) signifies that corresponding inputs or outputs are active low (a), thereby characterizing circuit operation without use of labeled outputs. The absence of the symbol (b) indicates inputs and outputs are active high.

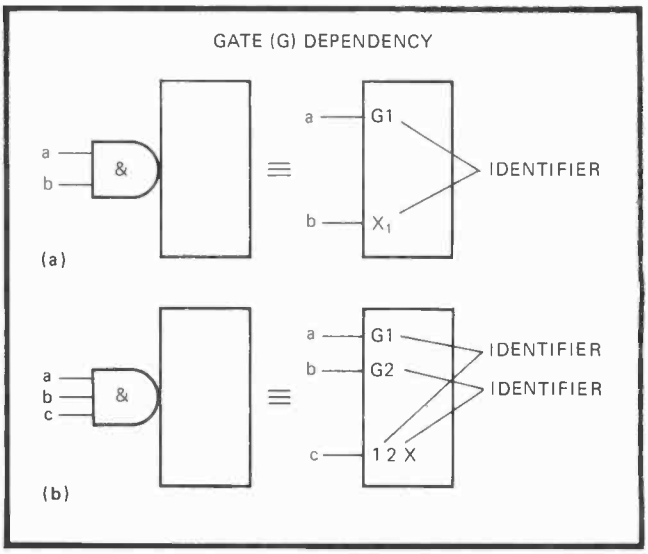
Table 1 gives the definitions of the basic elements—the amplifier, AND, OR, exclusive-OR, wired-AND, and wired-OR circuits—and their logic symbols. Note that the AND, OR, and exclusive-OR can be shown by their assigned shape or by a rectangle, since the presence of an identifying symbol within those elements specifies the device function. The inverting function for these elements (that is, inverter, NAND, or NOR) is indicated by placing the negation symbol (a small circle) at the corresponding output ports of the devices—the same symbol used currently. In addition to specifying the function of a logic element, qualifier symbols are used for classifying logic blocks. Table 2 shows the symbols

TABLE 3: FLIP-FLOP SYMBOLISM

Flip-flop	Original symbols	Previous standard MIL-STD-806B	ANSI Y32.14 Control designations description for flip-flop	
R-S				R S | Q $\bar{Q}$ l l | n.c. n.c. l h | h l h l | l h h h | undetermined
T				Toggling occurs with every clock pulse.
D				Data output follows data input; input is gated by C.
J-K				J K | Q $\bar{Q}$ l l | n.c. n.c. l h | l h h l | h l h h | toggles
J-K (gated)				J and K inputs are gated by C.
J-K (master-slave)	—	—		Outputs are dependent on the negative-going edge of the clock.

n.c. = no change

2. Dependency notation. Block-diagram equivalent of two-input AND gate (a), which drives one-shot, provides quick overview of circuit operation. Identifier indicates dependency between inputs a and b, showing data on b is gated in by a. Approach to coding up three-input AND gate follows logical extension of method (b).

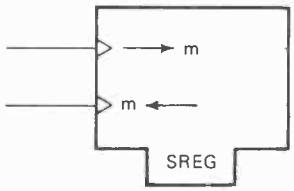


for some of the most widely used ones.

The polarity indicator symbol, shown in Fig. 1 (top), establishes the active states of the input leads required to switch on the logic element or indicates whether the output leads are active high or low. Any input or output so labeled is active low (a). Otherwise, the inputs or outputs are active high (b).

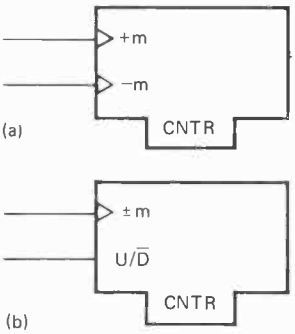
Although this symbol provides the same information as the negation symbol, it offers the advantage of visually representing the signal polarity required to activate the device. Furthermore, it eliminates the inconsistent labeling of logic devices. For example, the inverted

TABLE 4: COMMON CONTROL-BLOCK DEFINITIONS



Shift register block

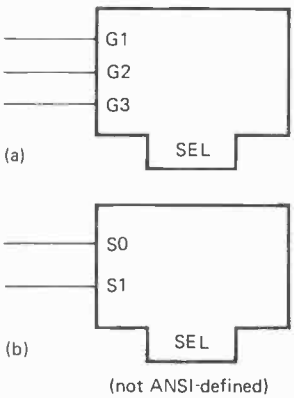
This symbol is used with an array of flip-flop symbols to form a shift register. The data will shift to the right (→) or to the left (←) on the positive-going edge of the input signal.



Counter block

This symbol is used with an array of flip-flops or other circuits serving as a binary or decade counter. In (a), the positive-going edge of an input to either the +m or −m input causes the counter to count upward or downward m times.

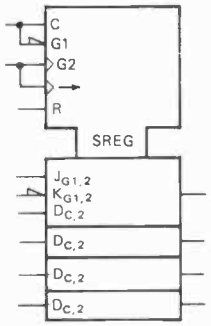
In (b), a positive-going edge of an input to the ±m port will cause the counter to increment or decrement m times depending on the input to the up-down control (U/D̄).



Selector block

This control block is used with an array of OR symbols to provide for the gating lines (a) or selection lines (b). The gating lines have an AND relation with the respective input of each OR function: G1 with the inputs numbered 1, G2 with the inputs numbered 2, etc. The selection lines enable the input designated 0, 1, . . . n of each OR function.

TABLE 5: COMMON DEVICE BLOCKS

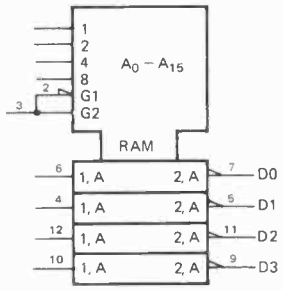


- **4-bit universal shift register**

This shift register has four parallel data inputs (D_C) and two synchronous serial data inputs (J, K). The control block contains those enable lines that will select the way data is loaded into the register. Data entry into the D flip-flops is dependent on C and G2 ($D_{C,2}$). A high input at C and a high at G2 will enable a parallel load on the positive-going edge of G2.

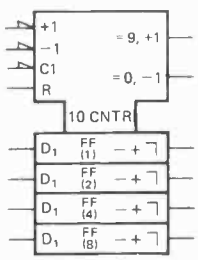
A serial load into the J-K flip-flop is dependent on G1 and G2 ($J_{G1,2}$, $K_{G1,2}$). When there is a low input at G1 and a high input at G2, data is loaded serially and shifted one position to the right on the positive-going edge of G2.

The device resets when there is a high present at the reset.



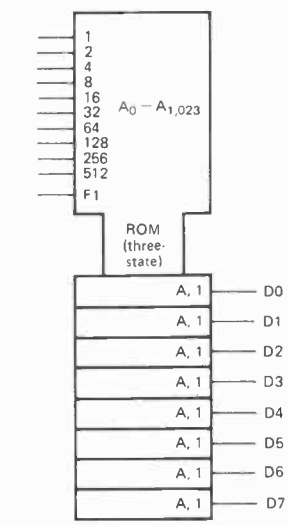
- **Random-access memory**
(without identical input/output pins)

Address selection is determined by the 4-bit address input codes in the upper left corner of the control block. These address codes are weighted to correspond to the possible address (A_0–A_{15}). G1 and G2 are the read/write enable. A low on pin 2 will enable data to be read into the chip in the memory location addressed; a high on pin 3 will enable the chip to output data from the particular memory location addressed. The inputs on the lower left corner of the symbol are labeled 1, A. This indicates that the information will be stored in the memory location addressed. 2, A on the outputs indicates that the data will be written from the memory location when G2 is enabled.



- **Presettable decade counter**

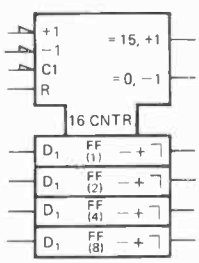
The counter control block is used to show the common inputs to a presettable decade up-down counter. The symbol "+m" means to count up by m and "−m" means to count down by m. (Note: if m = 1, it may be omitted.) The "=9, +1" symbol is the carry output or the terminal count up when the count equals 9. The "=0, −1" symbol is the borrow output or the terminal count down when the count equals 0. C1 is the control input for the D flip-flops and R is the master reset. When C1 is enabled, it loads all four flip-flops (D_1) in parallel. The presence of the output delay indicator is used to indicate that the D flip-flops are master-slave. Flip-flop weights are indicated in the parentheses. The symbol "10 CNTR" indicates that the counter is modulus 10.



- **Read-only memory**

This is a read-only memory with 1,024 addresses. Address selection is determined by the 10-bit address input in the upper left corner of the control block.

F1 is the three-state enable line. A high signal on this line will enable the outputs. A, 1 on the outputs indicates the dependency on the three-state enable and the memory location addressed.



- **Presettable binary counter**

Same as above except that the carry output is indicated with "=15, +1," indicating that the terminal count up occurs when the count equals 15. The symbol "16 CNTR" indicates that the counter is modulus 16.

output of a flip-flop is normally designated $\overline{Q}$, and the inverted R and S inputs have negation symbols at their ports, rather than being labeled $\overline{R}$ and $\overline{S}$. These ports will now be labeled Q, R, and S with appropriate polarity indicators. This change can be seen in Table 3, which shows the development of flip-flop symbolism.

Block form

By providing for dependency symbols and one-block devices, ANSI Y32.14 makes it easier for system designers to understand the operation of large circuits. So-called control blocks, which group the common control inputs, can be joined to contiguous blocks, which depict the remainder of the circuit (an array of gates, flip-flops, etc.). A combination of control and contiguous blocks forms a device block.

Figure 2 shows the application of dependency symbols. Dependency is indicated by subscripts, prefixes, or suffixes. For example, in the case of D_1, the 1 indicates a logic connection between the input, D, and a control line assigned the numeral 1. In prefix form, the notation becomes 1D; in suffix form, D1.

In the simple example of Fig. 2a, a two-input AND gate drives a one-shot multivibrator. The equivalent dependency for the gate is shown to the right. G1 is an input, through which data on line b is gated into the device. The 1 identifies the existence of the relationship between lines a and b, with the letter G defining the type of relationship (AND-gate dependency). The appropriate letter identifies other relationships: A (address), C (control), F (free, or three-state), or V (OR-gate).

Figure 2b, an extension of Fig. 2a, shows how a circuit having a three-input AND gate is coded. G1 and G2 are the gating inputs for data on line c, as indicated by the 1,2 of the input 1,2 X.

Symbol buildup

ANSI's recommended control blocks include a shift register, a counter, and a selector, all of which are shown in Table 4. The lower figures of the counter block and of the selector block are not part of ANSI's standard, but they have appeared occasionally in the literature and so are included for reference.

When these control blocks are united with contiguous blocks, such as flip-flops, then entire devices can be built. Several are illustrated in Table 5. ❑

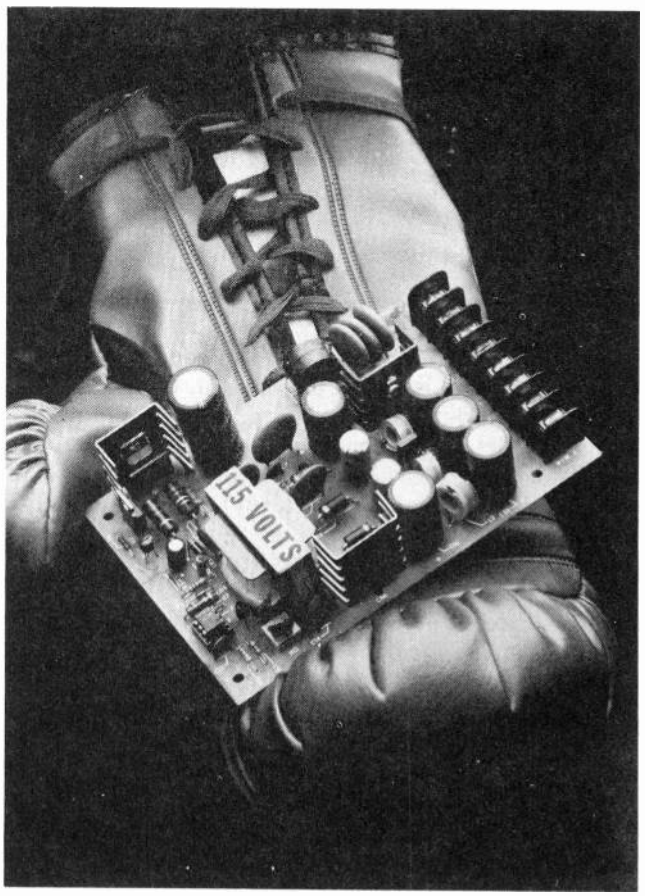
Flyback converters: solid-state solution to low-cost switching power supplies

For the user, close attention to design detail will yield a high-performance system with low production costs

by Robert J. Boschert, *Boschert Inc., Sunnyvale, Calif.*

☐ Long a fixture in high-power applications like mainframes and their peripherals, the solid-state switching power supply is only now making its mark in low-power applications where the low-cost linear supply predominates. Momentum for this thrust comes from simplified switcher designs that lower the cost of converting an ac input to multiple dc outputs.

Typically, most switching converters have been custom designs, tailored to solve a particular problem or set of problems. When equipment makers ran into size, weight, or cooling restrictions as they designed supplies into their gear, they ordered the custom switchers.



1. The big punch. The OL25 switcher measures 2.5 by 4 by 6 inches and weighs 12 ounces; yet it delivers a hefty 25 watts of switching power. An adaptation of the flyback converter, the design minimizes both magnetic and semiconductor costs.

With the new standard converters, these manufacturers are finding they can profit from such advantages as improved portability and the elimination of cooling fans, without sacrificing economy. Thus switchers are beginning to show up in volume in such low-power applications as microcomputer systems, home-computer video terminals, and small commercial computer systems.

Minimizing cost

The new switchers may be the product of a common design philosophy, but their different makers do not agree on how to minimize costs. Nor do they agree on what cost-performance tradeoffs to make in most cases. The original-equipment manufacturer, faced with this controversy, can resolve it for his particular applications—but only if he is familiar with some of the basic design considerations in this field.

What he will find for his consideration is such designs as the Boschert OL25 series. These general-purpose, low-power switching supplies are designed to compete directly against linear supplies by reconciling the lowest possible cost with acceptable performance in most cases.

These switchers (Fig. 1) are an adaptation of the flyback, or ringing choke converter, generally used in television receivers' horizontal circuits, xenon flash units, and other very low-cost applications. Other techniques are used by other switcher manufacturers, but the flyback approach minimizes the costs of both magnetic and semiconductor components. The new Boschert line attacks the problem of high regulation costs by novel power-control methods.

The initial choice

In theory, all switchers are alike; in practice, their designers can choose among a number of basic approaches (Fig. 2). Usually they select the one that provides the required performance with no need for added components or a major engineering effort. Often, a better decision is to select a lower-cost and -performance basic circuit and to design in the higher performance with an engineering effort that also seeks to minimize production costs.

Since the switcher essentially is an electronic system rather than a traditional power supply, it should be evaluated as a system, rather than as the sum of its

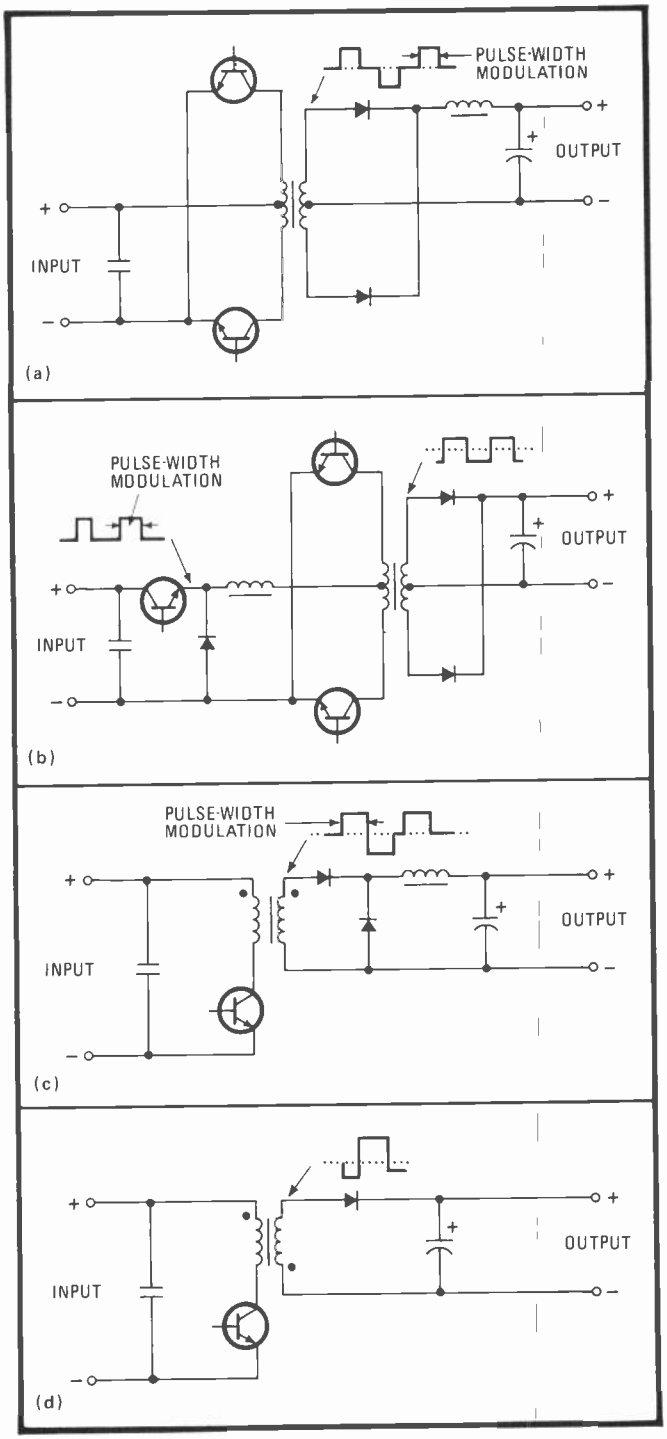
components. Coming into play are such considerations as consolidation of functions, regulation and ripple filtering, the number of power stages, and energy storage.

Most applications require multiple power outputs. Major savings may be achieved combining a function necessary for each output stage in a shared circuit. For example, the filtering required after the power switch might be combined into a filter circuit at the outputs.

The OEM designer may find that he must allow for tradeoffs in regulation and ripple to take advantage of the switcher's benefits without cost penalties. For example, the designer of a digital system wants a precise +5-volt output to power most of the system.

Almost all switchers directly sense the +5-v output and regulate it to ±1% in order to keep it well within the typical digital component tolerance of ±5%. However, auxiliary outputs usually are semi-regulated: that is, they are dependent upon the regulation provided by the control circuitry for the ±5-v output.

The rationale for semi-regulation is that acceptable performance for low- and medium-power uses can be achieved on the auxiliary outputs without added power-handling stages. One circuit then can regulate all input voltage effects for all outputs, and acceptable load regulation can be met by minimized output impedances.



2. Switching converters. Low cost makes the quasi-square-wave converter (a) attractive. For medium power, the two-stage switchers (b) excel. Forward and flyback converters (c and d) require clever design to offset their higher-priced parts.

A fact of life

Ripple in switching power supplies tends to raise designers' emotions, for it is inescapable. The fast switching characteristics of these units means the phenomenon is inherent, so it is pointless to strive for the lowest possible ripple at any cost.

However, every converter output has a filter, which generally can be designed to reduce ripple to an acceptable level at a nominal cost. Ripple voltage levels within 2% of the dc output voltage usually are low enough for the ripple to become buried in the normal system noise.

In most high-power applications, semi-regulation on auxiliary outputs does not suffice. Therefore, the basic converter's cost should be minimized, and the savings should be used for such performance-improving functions as a linear post-regulator and a filter on each auxiliary output. The quasi-square-wave converter of Fig. 2a is the choice here, because it requires only one power conversion, minimizing semiconductor costs.

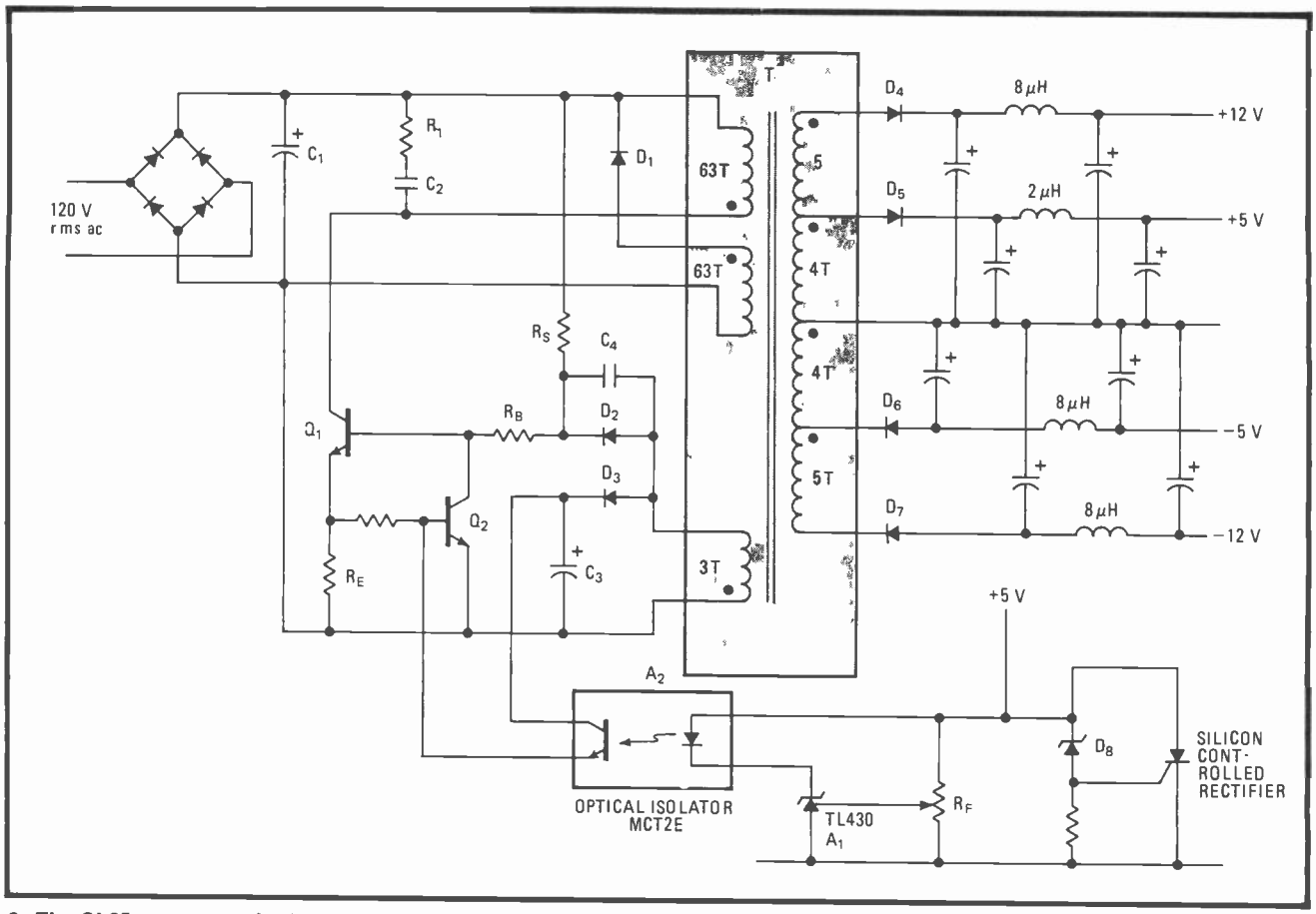
For medium-power applications, the two-stage switcher (Fig. 2b) is the best choice, because its improved power conditioning makes semi-regulation practical. Post-regulators are eliminated and filtering requirements are minimized, but at the expense of additional semiconductor devices in the basic unit.

However, the costs of medium-power semiconductors are reasonable, and the two-stage design shown trades off the cost of added devices against savings down the line. Also, it needs only one primary inductor, whereas the quasi-square-wave unit needs one for each output.

Where flyback fits in

Forward and flyback converters (Figs. 2c and d, respectively) could be used for medium-power applications, but they are too expensive at present component costs. A forward converter needs a large inductor in each output for energy storage. A flyback converter does not need such inductors, but its utilization of power semiconductor devices is less efficient, requiring the use of relatively expensive components.

For low-power applications, efficient utilization of components is less urgent, because the low-power semiconductor devices used are relatively inexpensive. Moreover, the OEM designer can choose a switcher from a number of converters with a single power switch and



3. The OL25 power supply. A novel control circuit to adjust current flow during operation is governed by a feedback from the +5-V output through A_1 and A_2 to transistors Q_1 and Q_2. The ±5-V outputs are regulated; the ±12-V are semi-regulated.

one output change.

Forward converters have been preferred over flyback switchers because of their relatively higher performance. However, a flyback-based power supply can offer equivalent performance to a forward unit if its designer plows back part of the savings in magnetic and semiconductor costs into design improvements. The savings in output inductors more than offsets the slight increase in transformer complexity needed to combine the isolation and storage functions.

Low-cost energy

Yet this more complex double-duty transformer contributes heavily to the flyback converter's major advantage: lower-cost energy storage. Often overlooked as so fundamental a fact of switcher design, energy storage represents a large chunk of total system costs, as well as being a key to the unit's efficiency.

Energy is stored when the power-switching transistor turns on and is delivered to the load when the transistor turns off. Switch-control regulation thus replaces the highly inefficient energy-dissipation techniques used to regulate linear power supplies.

However, most switchers must store their energy in expensive magnetic components. By storing energy in the isolation transformer, the flyback converter eliminates this component expense. Moreover, it needs the fewest components for each basic power-handling function. In fact, one component suffices for each function, because the flyback converter is a single-ended circuit.

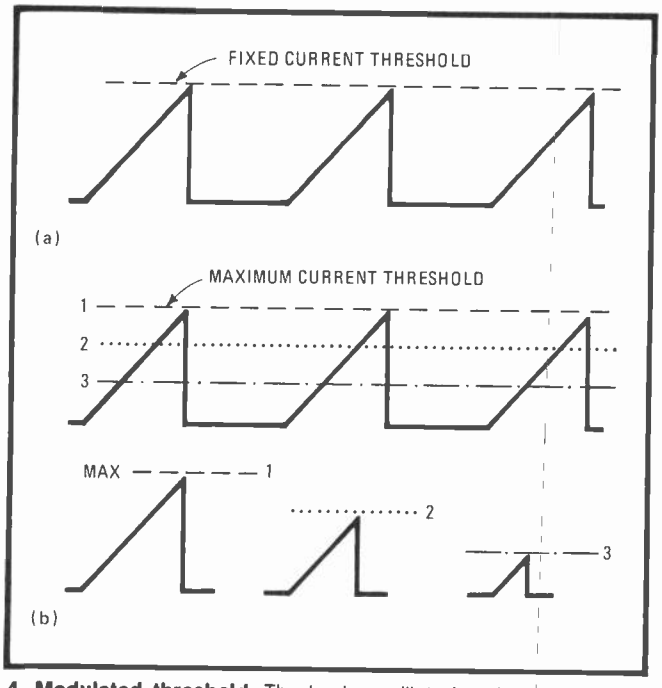
As the Boschert OL25 series shows, the result can be a versatile design (Fig. 3) that provides 25 watts maximum in four continuous outputs over worst-case line-power conditions. The basic model has ±5-v regulated outputs and ±12-v semi-regulated outputs. A modular design approach allows outputs to be tailored for optional voltages throughout a ±40-v range.

The main challenge in flyback design is to minimize the cost of the control circuitry. In general, controlling the output power is achieved by a blocking oscillator power stage that changes state whenever total positive feedback gain from the switching section through the transformer exceeds unity. The blocking oscillator then usually delivers a fixed amount of power.

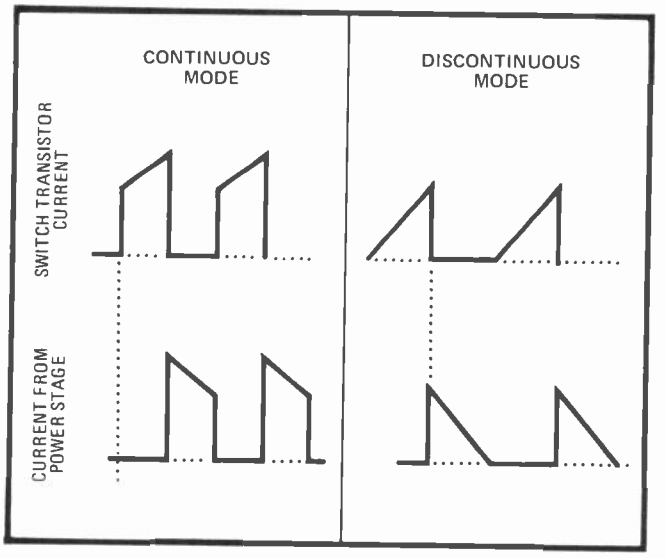
Controlling the power

The OL25 operates as a blocking oscillator under the following control law: output is linearly proportional to current flowing in the primary circuit at the time transistor Q_1 in Fig. 3 turns off. The simplifying assumption is made that output power is independent of input line voltage and operating frequency, so far as the control loop is concerned. Then the control-loop model for the power stage is simply a current source driving the output capacitances.

To adjust power flow during operation, the OL25 implements a novel control circuit. The new technique provides excellent regulation resulting in significant



4. Modulated threshold. The basic oscillator's primary current is limited by a fixed threshold (a), but the OL25's circuit (b) implements a modulated threshold technique that results in a variable duty cycle; hence, the power outputs are constantly regulated.



5. Flux modes. The OL25 converter operates in the discontinuous flux mode because of better cost tradeoffs, despite the greater average power delivery in the continuous mode operation. Also, the continuous mode operation requires complex control circuitry.

savings in the components required for control circuitry. Moreover, the circuitry occupies little more than 10% of the total board area.

In a basic blocking oscillator (Fig. 4a), primary current rises linearly until a preset current threshold is reached, then drops to zero until the end of the cycle. In the OL25 (Fig. 4b), the current threshold is modulated, resulting in a variable duty cycle and power adjustment. The control circuit is designed to home in on that duty cycle, ensuring proper regulation. The circuit programs the current level at which the power-stage feedback exhibits a gain greater than unity. Thus, switching proceeds at the proper duty cycle.

Greater stability

In addition to reducing cost, the technique enhances stability. It results in a 90° phase lag of output currents at high frequencies, instead of the 180° shift characteristic of direct duty-cycle control.

This primary current control simplifies feedback compensator design. Switching frequency for this design is around 20 kilohertz, and operating frequency is inversely proportional to the output power.

The blocking oscillator turns on when the energy stored in the magnetic field of transformer T_1 in Fig. 3 is approximately zero. It turns off at an energy level determined by the base drive voltage, the emitter resistor R_E (the current-sense resistor), and the primary inductor. Stored energy is released to the outputs via rectifiers D_4 through D_7. When the energy in T_1 has been drained to approximately zero, the switching cycle repeats.

Transistor Q_1 provides the desired adjustment of power flow. Q_1 and Q_2 are part of a current-limiting circuit that varies the duty cycle. The adjustment is governed by feedback from the ±5-v output through amplifiers A_1 and A_2, so that a rise in voltage above +5 v produces a compensating reduction in output power and voltage.

Q_1 saturates and the transformer-inductor primary current starts its linear climb. The current increases until the rising voltage across R_E reduces the base current enough for Q_1 to operate in the linear class A mode. Q_1's constant-collector-current characteristics cause current limiting, so the rate of change of current in T_1 decreases; the voltages across the primary and base windings decrease; and Q_1 is driven off.

Now the energy stored in T_1's magnetic field must escape. The voltage on the windings reverses in polarity and increases in magnitude until a decay current path is found. The output rectifiers D_4 through D_7 conduct before input rectifier D_1 conducts. D_1 clamps the leakage inductance spike on the primary switch to the input source voltage.

Q_1 remains off until all energy is drained from T_1 and the output rectifier currents go back to zero. T_1 then rings back with the primary inductance and C_2's capacitance until Q_1 is again biased class A and turns on to repeat the cycle. Output power is a linear function of the current flowing in Q_1 as it comes out of saturation.

Lowering control costs

A major savings was achieved in the feedback control circuit by using +5-v–compatible integrated circuits. One is an adjustable zener diode, the TL 430, a 3-pin package used as an error amplifier. The conventional control circuit is a 16-pin integrated circuit. The other is MCT2E, an optical isolator that does double duty as an optoisolator and as part of the control circuit.

The TL 430 (A_1 in Fig. 3) meets the requirements for feedback control in switching regulators with on-chip functions like the high-gain operational amplifier and a voltage reference. In this application, the +5-v output provides both power and feedback signal. The TL 430's 2.75-v internal reference voltage is compared with the

output feedback signal at the wiper of potentiometer R_F.

The optoisolator, A_2, provides the necessary ac line isolation. The alternative would be placing a small transformer in the control loop. In the main power path, T_1 provides the required isolation.

A_1, A_2, and the current-limiting circuit control the amount of power flowing to the secondary. A_1 operates as an inverting transconductance amplifier. When the +5-v output voltage rises, A_1 drives the light-emitting diode in A_2 harder, thereby controlling the current through the latter's output transistor.

The current from A_2 prebiases the base of Q_2, reducing the current required to turn that transistor on. When Q_2 is biased on by a rise in voltage across resistor R_E, Q_1 turns off. The result is output regulation through adjustment of peak current and thereby output power.

The silicon controlled rectifier to the right of A_1 in Fig. 3 is part of a temperature-stabilized crowbar circuit that provides over-voltage protection. The circuit acts as a short when the 5.1-v zener diode, D_8, is overcome and the voltage at the SCR gate exceeds 0.8 v. The SCR selected assures the high rate of current change needed to discharge the output capacitances.

Accounting for filters

Each output filter in Fig. 3 is shown as a π-section filter with an inductor. This is not a general requirement, but it may be needed in some applications to minimize ripple on one or more outputs. Hence, the output stages are designed to accept a small air-core inductor and the additional capacitor required by a π-section filter.

The input filter is standardized. It has sufficient capacity to maintain maximum power output for 16 milliseconds after a line-power interruption.

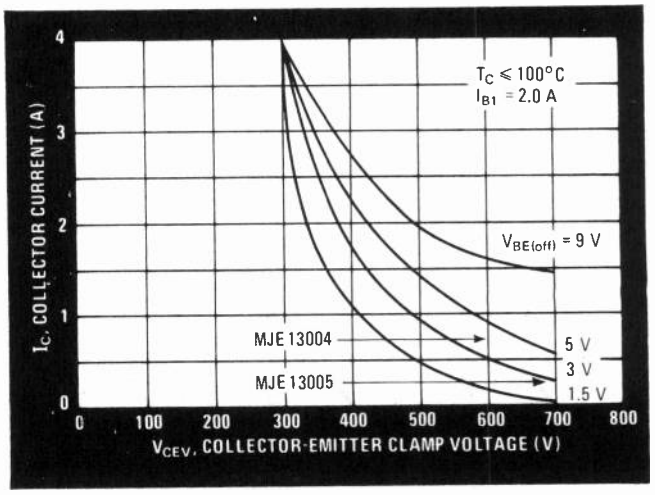
For energy storage, the flyback converter's transformer must be designed in as a multi-winding inductor rather than as a transformer. All power-inductor parameters become critical, and the winding geometry must be planned carefully to minimize leakage inductance.

In designing the transformer-inductor, some general criteria must be met. The magnetic circuit path is usually gapped in the one place where energy is stored. For the most part, the path operates over a flux density range from zero to maximum, typically 3,200 gauss for power ferrite at 100°C.

Core size determines the number of turns and the turns ratio can be derived from a steady-state design equation. For the Boschert OL25, an Electrical Plastics M1187-2 core is used. The turns for the primary and secondary coils are shown in Fig. 3.

The OL25 converter operates in a discontinuous flux mode. This provides a better cost tradeoff then the continuous mode since it reduces the volume of the magnetics components, and control-circuitry costs.

In the continuous mode, the ac flux is small compared to the dc component. Hence the current flowing in the switch transistor at turn-off is much the same as at turn-on, and the average power delivered to the load is greater than for discontinuous operation for a given peak transistor current (Fig. 5). However, the continuous mode requires relatively complex oscillator and control circuitry, shooting costs up.



6. Safe operation. Q_1 was chosen from Motorola's MJE 13004 family of power transistors because it exhibited a reverse bias that allows a proper margin of safety in the converter design. The 75-W npn transistors are designed for high-speed switching applications.

Selecting the power switching transistor (Q_1 in Fig. 3) is a matter of determining the required duty cycle. The limiting factor is the safe operating area of Q_1's reverse bias. Consider the steady-state design equation:

$$\frac{\text{volts} \times \text{seconds}}{\text{turns}}(\text{on}) = \frac{\text{volts} \times \text{seconds}}{\text{turns}}(\text{off})$$

for the on and off states of the ac-power-line input side of the converter. If just the primary winding of the transformer-inductor is considered, the number of primary turns drops out, and the voltage stress on Q_1 can be analyzed.

Using two equations

The voltage stress equals the source voltage plus the primary flyback voltage. If on time equals off time (a 50% duty cycle), flyback voltage equals source voltage. Thus, Q_1 must hold off twice the source voltage plus any spike voltage due to leakage inductance.

On the other hand, keeping the duty cycle as high as practical reduces the amount of current the transistor must pass. The switch current's dc component is:

$$I_{Switch} = \frac{\text{power output}}{V_{in} \times \eta \times \text{duty cycle}}$$

where η is efficiency. These two equations give voltage-current tradeoffs for various power levels and transistor specifications.

Since reliable operation is the most important consideration, peak voltages must be kept within the limits of presently available low-cost transistors. Compensating for the increases in input voltage by reducing the duty cycle accomplishes this.

One OL25 version for 110-v application operates at a 40%-50% duty cycle, and another version for 220-v application operates at a 20%-25% duty cycle. For both, the transistors are selected from the Motorola MJE13004 family of 75-w npn silicon power transistors. Designed for high-speed switching in inductive circuit applications, the MJE13004 has the reverse-bias safe operating area shown in Fig. 6. □

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