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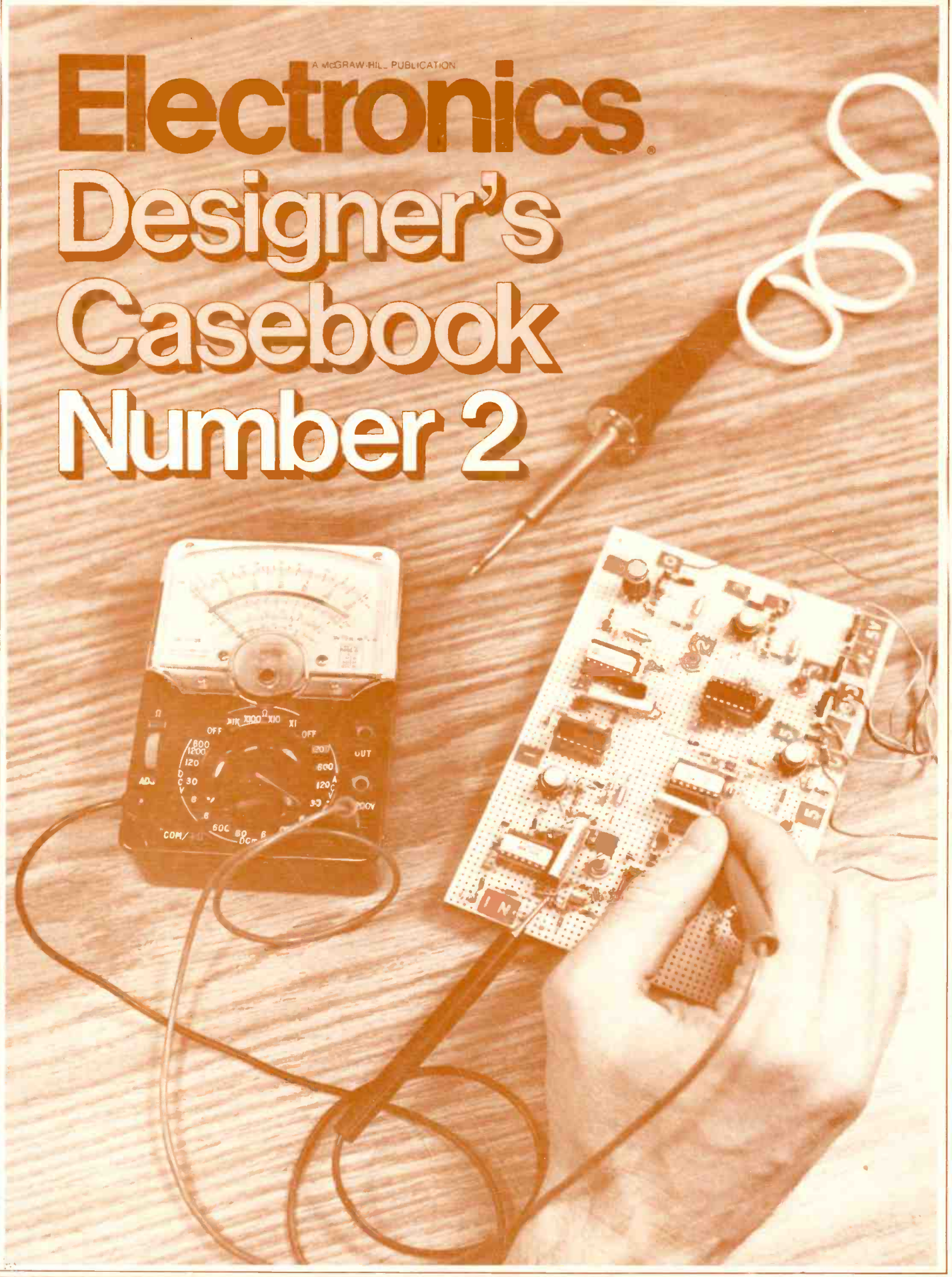
Electronics

Designer's Casebook Number 2



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DESIGNER'S CASEBOOK

PREPARED BY THE EDITORS OF Electronics

Second in a continuing series of selected Designer's Casebook sections of Electronics magazine. This edition includes Electronics issues from March 31, 1977 through February 2, 1978. Also included are feature articles and items from Engineer's Notebook of particular interest to the circuit designer.

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McGraw-Hill, Inc.
1221 Avenue of the Americas
New York, New York 10020

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Saturable core transformers harden latch memories

by Gordon E. Bloom
IRT Corp., San Diego, Calif.

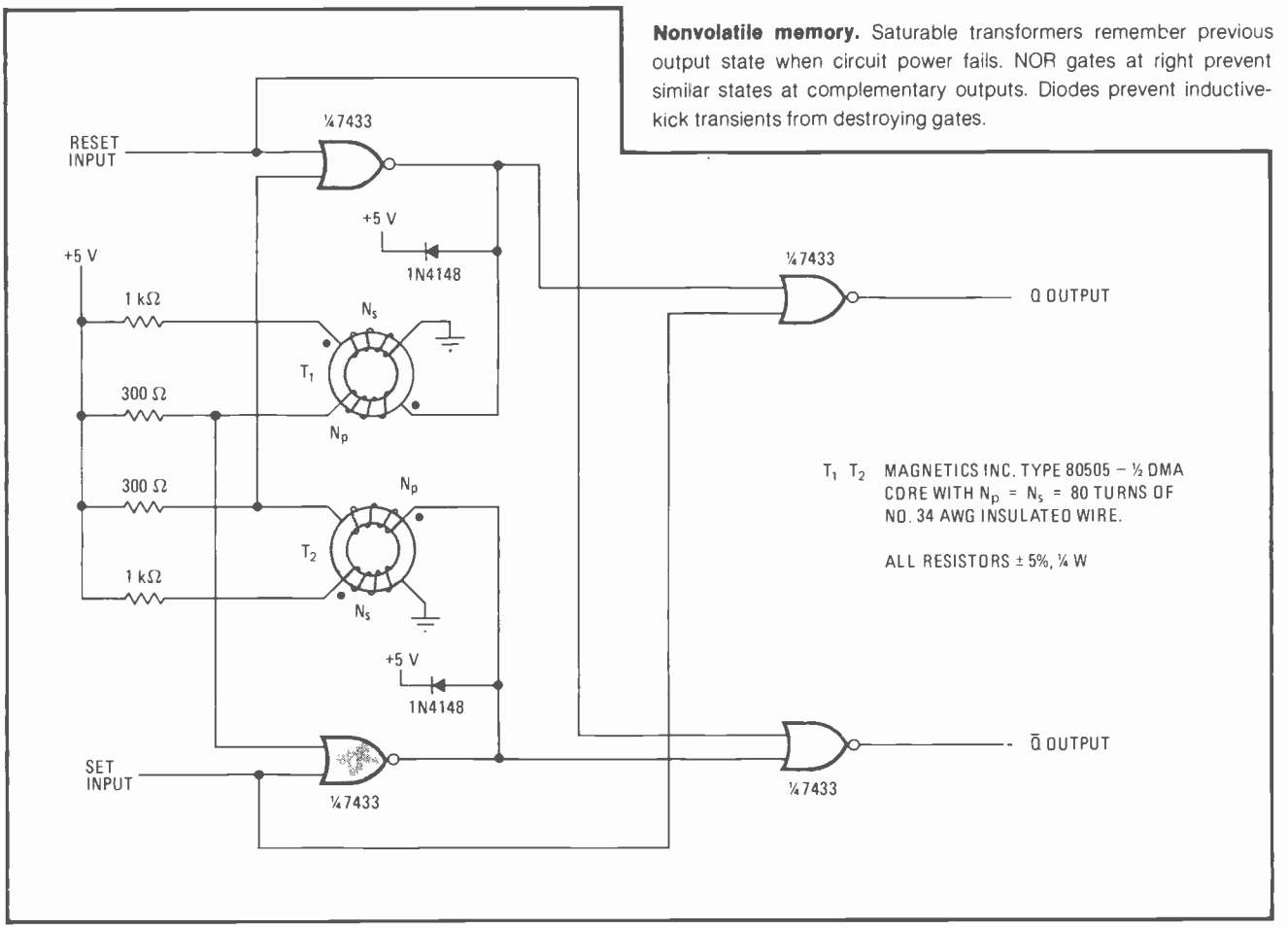
In certain critical applications, the loss of data in latch memories caused by supply and command-line failures or transients can be disastrous to system operation. However, at a slight sacrifice in switching speed, a memory-hardening circuit that uses saturable transformers can make the memory latch nonvolatile and insensitive to false command signals.

As shown in the figure, the subminiature saturable transformers are placed in the feedback paths connecting two NOR gates, which occupy half of a 7433 quad package. The transformers are incapable of an immediate state change, and because they stay magnetically biased without a voltage supply, they provide a reference state to which the memory latch returns when the power is reapplied.

The output voltage of each transformer is a function of its magnetization state (set by a gate output) and a power-up pulse, which attempts to examine this state. Each transformer is biased at all times—one in positive saturation (low-resistance core condition) and the other in negative saturation (high-resistance core condition). If power is lost, the magnetization state of each core is unchanged and remains so indefinitely. When power returns, a voltage is induced into the primary of the transformer that is in negative saturation. This voltage then drives the associated gate, restoring the original conditions at the latch outputs.

Transistor-transistor-logic gates are used. Resistor values have been chosen to ensure that primary-to-secondary coupling of the transformers produce currents that are sufficient to bias the core properly on its hysteresis curve, yet that do not overdrive the gates. In addition, the total flux capacity of the cores permits adequate switching time, while placing no undue restiction on the normal set and reset timing relationships during normal operation.

When a bit is initially stored in this circuit, the set or reset pulse must have a minimum width of 35 microseconds, and pulses must be separated by a minimum of



Nonvolatile memory. Saturable transformers remember previous output state when circuit power fails. NOR gates at right prevent similar states at complementary outputs. Diodes prevent inductive-kick transients from destroying gates.

65 μs. Should power fail during operation, the power-supply fall time must be much less than 35 μs; otherwise, the latch may lose its contents. The same rise-time constraints accompany power-up.

The circuit may be implemented with other logic families, but choice of component values must take into consideration the family's impedance and switching characteristics. □

Special PROM mode effects binary-to-BCD converter

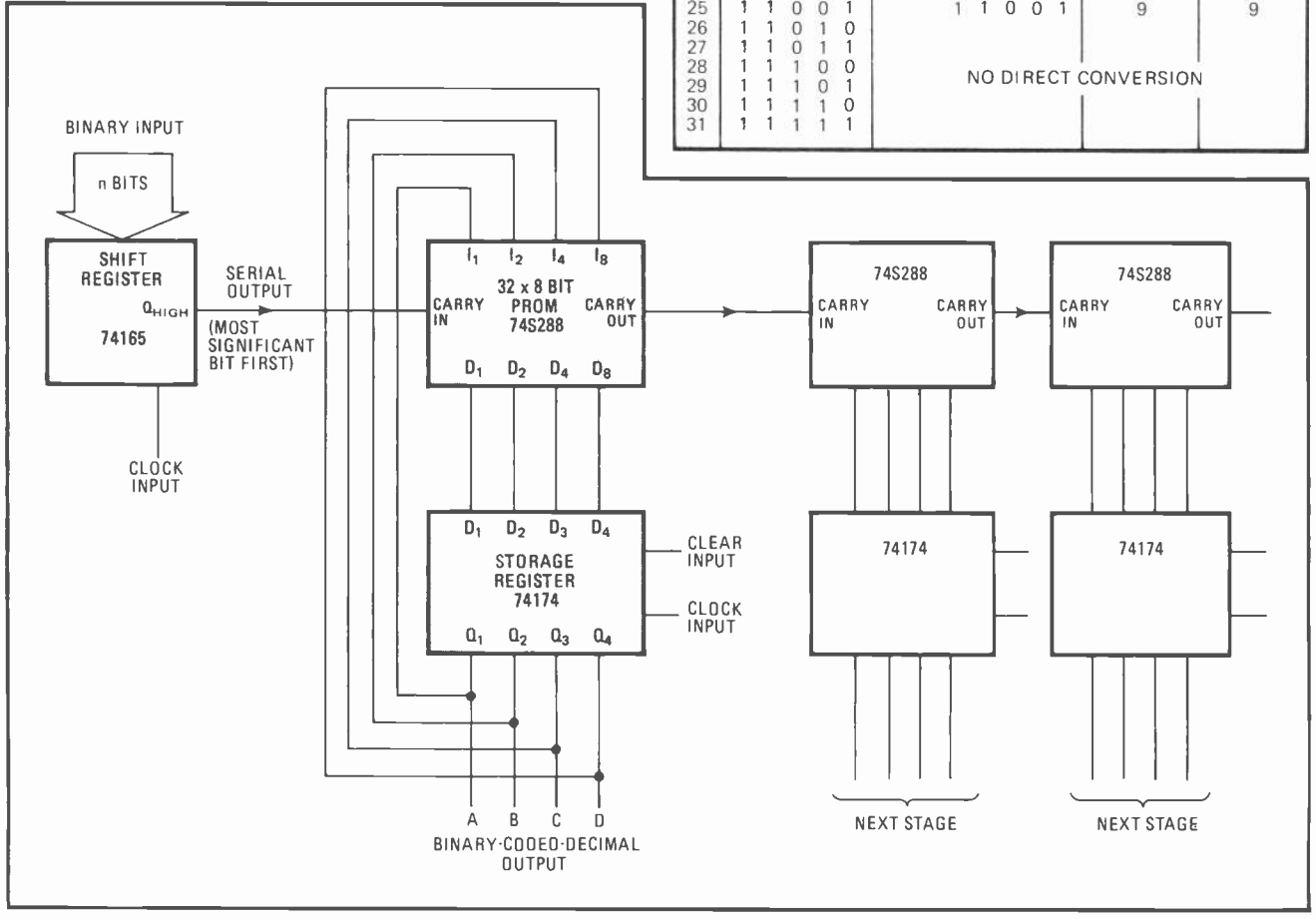
by D. M. Brockman
The Boeing Co., Seattle, Wash.

Computer software converts a binary number to its binary-coded-decimal equivalent by algebraically summing each bit, starting with the most significant bit, and doubling the result of each addition. The method is the equivalent of a binary shift register where a shift doubles the value of the register contents.

But a shift register cannot do the job alone. To make a hardware binary-to-BCD converter also requires a storage register and a programmable read-only memory that is operated in an unusual mode. The circuit is especially advantageous when processing large binary numbers, since PROMs may be simply cascaded for additional

BINARY/BCD CONVERTER PROM TRUTH TABLE

n	BCD in (address) $C_1\ I_8\ I_4\ I_2\ I_1$	BCD out (contents) $Q_7\ Q_6\ Q_5\ C_0\ D_8\ D_4\ D_2\ D_1$	Function input	Function output
0	0 0 0 0 0	0 0 0 0 0 0	0	0
1	0 0 0 0 1	0 0 0 1 0	1	2
2	0 0 0 1 0	0 0 1 0 0	2	4
3	0 0 0 1 1	0 0 1 1 0	3	6
4	0 0 1 0 0	0 1 0 0 0	4	8
5	0 0 1 0 1	1 0 0 0 0	5	$0 + C_0 = 1$
6	0 0 1 1 0	1 0 0 1 0	6	2
7	0 0 1 1 1	1 0 1 0 0	7	4
8	0 1 0 0 0	1 0 1 1 0	8	6
9	0 1 0 0 1	1 1 0 0 0	9	8
10	0 1 0 1 0			
11	0 1 0 1 1			
12	0 1 1 0 0	NO DIRECT CONVERSION		
13	0 1 1 0 1			
14	0 1 1 1 0			
15	0 1 1 1 1			
16	1 0 0 0 0	0 0 0 0 1	$0 + C_1 = 1$	1
17	1 0 0 0 1	0 0 0 1 1	1	3
18	1 0 0 1 0	0 0 1 0 1	2	5
19	1 0 0 1 1	0 0 1 1 1	3	7
20	1 0 1 0 0	0 1 0 0 1	4	9
21	1 0 1 0 1	1 0 0 0 1	5	$1 + C_0 = 1$
22	1 0 1 1 0	1 0 0 1 1	6	3
23	1 0 1 1 1	1 0 1 0 1	7	5
24	1 1 0 0 0	1 0 1 1 1	8	7
25	1 1 0 0 1	1 1 0 0 1	9	9
26	1 1 0 1 0			
27	1 1 0 1 1			
28	1 1 1 0 0	NO DIRECT CONVERSION		
29	1 1 1 0 1			
30	1 1 1 1 0			
31	1 1 1 1 1			



BCD converter. Storage register in feedback loop with programmable read-only memory allows continuous updating of the memory's contents. Multidigit conversion, if necessary, is relatively simple because cascade stages are connected by one lead only.

digits. The circuit speed is typically a few megahertz.

The circuit of the converter is shown in the figure. After loading the 74165 shift register, which accepts either parallel or serial data, an n-bit binary word is serially clocked into the carry input of the 74S288 256-bit PROM. This 32-by-8-bit memory has input and output stages that accept or generate BCD data.

The unusual features in the PROM's use are that its contents are updated in each clock cycle and that the updating forms the circuit's desired equation:

BCD output = 2(BCD input) + carry input

The PROM's truth table shows the BCD output for a given BCD input plus carry input. Any BCD sum exceeding 9 will generate a carry output, thus permitting multidigit conversion if the carry output is brought to the carry input of the next stage of the circuit. If the most significant bit of the n-bit number is shifted out first to the PROM, then after n clock pulses, the resulting BCD-equivalent number will be at the output of all the 74174 storage registers.

The output of each storage register is the input for its PROM, and its content is that of its PROM during the previous clock period (ignoring the carry out). The circuit can convert a 20-bit number to its BCD equivalent at speeds of at least a few megahertz. □

Automatic gain control has 60-decibel range

by Neil Heckt
The Boeing Co., Seattle, Wash.

An automatic-gain-control circuit with an input range of 60 decibels (20 millivolts to 20 volts) can be built using a junction FET as a voltage-controlled resistor in a peak-detecting control loop. The circuit exhibits a quick response of 1 to 2 milliseconds and a delay time of 0.4 second.

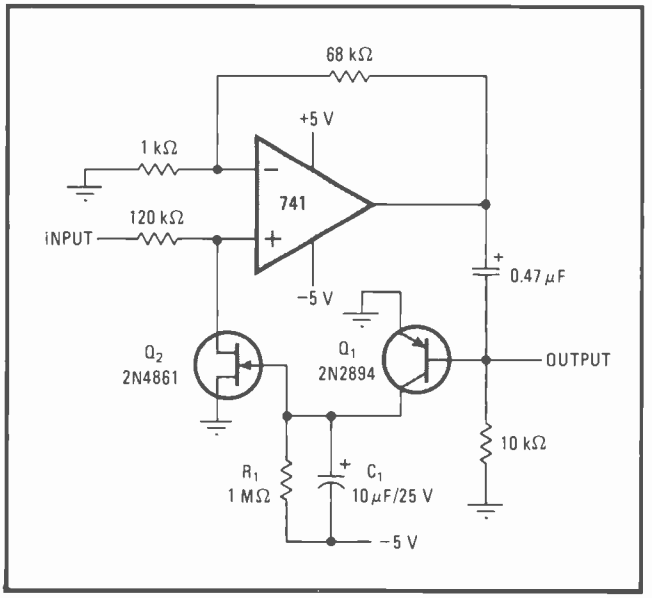
As shown in the schematic of Fig. 1, the 2N4861 n-channel field-effect transistor Q_2, connecting the noninverting input of the operational amplifier to ground, determines the closed-loop gain of the system. Negative base-voltage peaks from the output of the op amp, beyond V_{BE} of Q_1, turns Q_1 on, and its collector current then charges capacitor C_1.

The voltage across C_1 determines the channel resistance of Q_2. Since the range of this resistance is 120 ohms to more than 10^8 ohms, the 60-dB range of the circuit is easily realized.

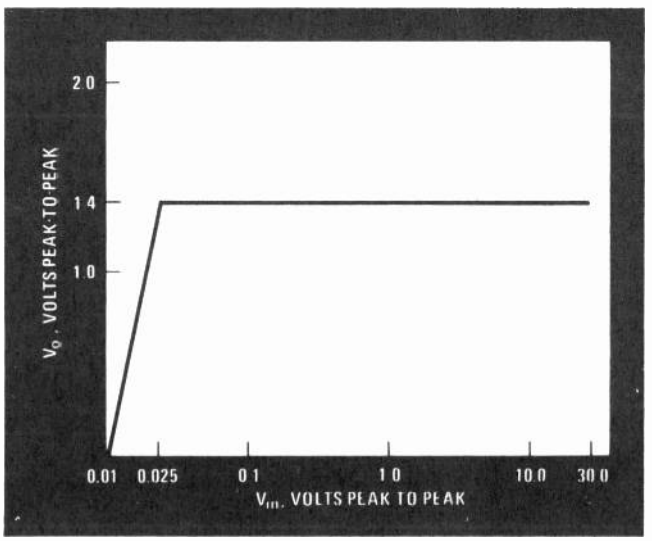
In the absence of an input signal, capacitor C_1 discharges through resistor R_4, cutting off Q_2. It is the C_1-R_4 combination that determines the delay time of the circuit. The collector current of Q_1 and the value of C_1 determine the circuit's attack time.

The op amp can be a 741 or any general-purpose device. Even with input signals of 20 v peak to peak, the maximum signal at the device's input is 25 mv peak to peak. Thus it is possible for the input voltage to be greater than the supply voltage.

The op amp's output is ac-coupled to the base of Q_1 because the dc operating point of its output varies with the changing output impedance of Q_2. To avoid dc bias difficulties when coupling to subsequent stages, the circuit's output is taken from the base of Q_1. Figure 2 shows the gain-control behavior of this circuit throughout its dynamic range. □



1. Audio AGC. Input voltage for distortionless output is from 20 millivolts to 20 volts in this quick-response AGC circuit. The input signal can have greater magnitude than the supply voltage because the maximum signal across the FET is 25 millivolts.



2. AGC characteristics. The output voltage is approximately 1.4 volts over a 60-dB range. A wider dynamic range would be possible if the off/on-resistance ratio of the FET were greater.

Frequency-controlled gate makes high-Q filter

by Noel A. Sivertson
Denver, Colo.

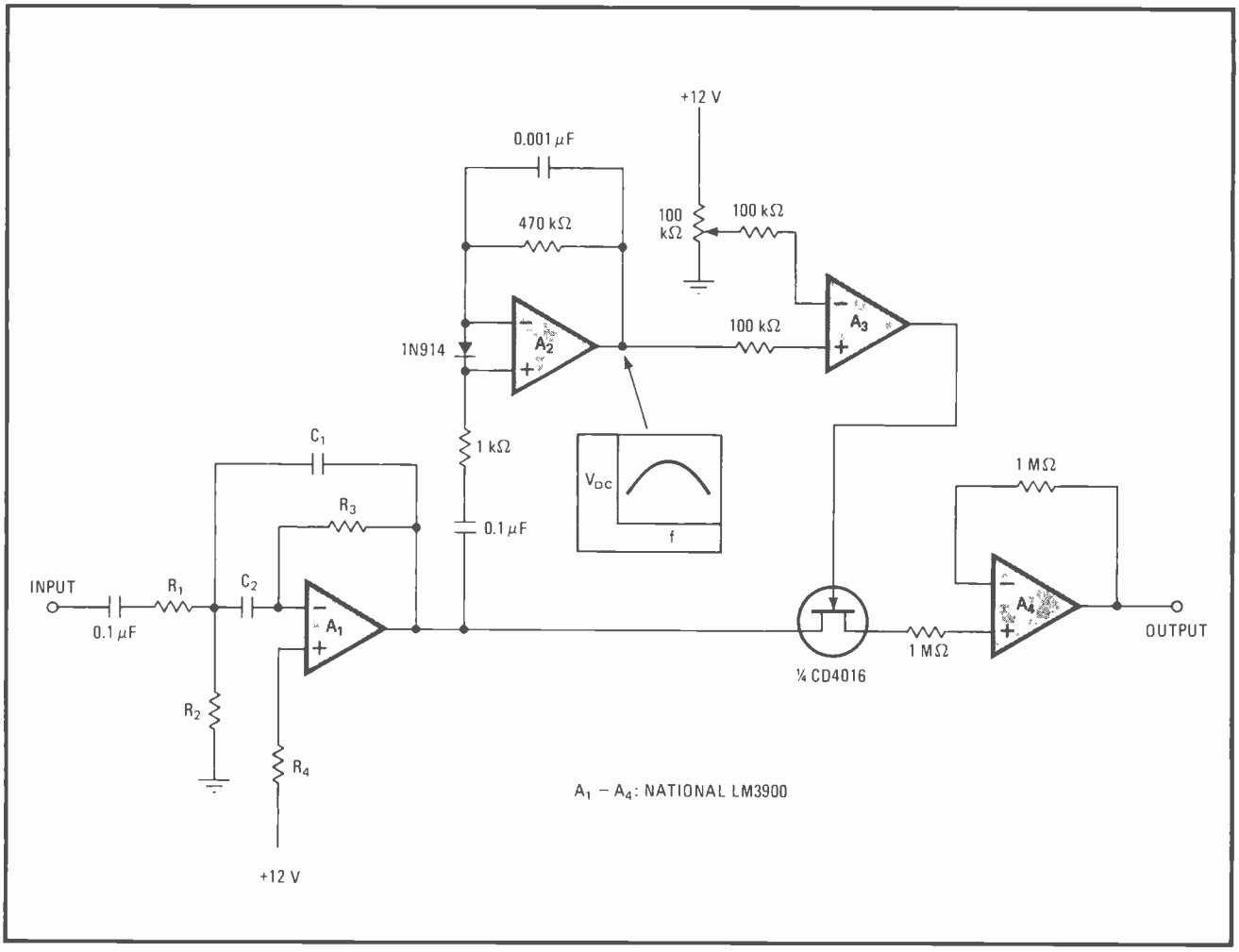
A bandpass filter in conjunction with a frequency-controlled gate provides a highly selective filter at low cost. Its high Q is especially useful for single-frequency discrimination, where conventional filters falter.

The circuit utilizes the response of the bandpass filter itself to pass desired signals, and it absolutely rejects all other frequencies. As indicated by the figure, input signals encounter A_1, a standard bandpass filter. Resistors $R_1 - R_4$ and capacitors C_1 and C_2 determine the filter center frequency and bandwidth, and their values are selected accordingly. The output of A_1 is then presented both to A_2, which serves as a peak-rectifier detector, and to the input of the CD4016 analog transmission gate. The output of A_2 is a dc signal having an amplitude that is proportional to the filter's transmission coefficient—that is, the filter's center frequency produces the largest dc output. This output represents the envelope of the filter response.

A_2's output is compared to a user-determined reference voltage at A_3, and when it exceeds this reference voltage, A_3 signals the transmission gate to transfer its input signal to the output. Thus comparator A_3 is in effect a bandwidth adjustment control.

Depending on the quality of the band-pass filter, the ultimate bandwidth of the circuit could be as sharp as a few cycles. To retain this sharpness, however, it is required that the signal be of a reasonably constant amplitude at the input to the circuit.

This circuit has also been used in an amplifier-squelching device and to control the range of a sweep oscillator. □



Gated filter. Circuit uses pass-band response of ordinary filter in generating voltage reference for gate switching. Transients caused by gate switching in the audio range are not detrimental to circuit performance but may cause concern at higher frequencies.

Decoders drive flip-flops for clean multiphase clock

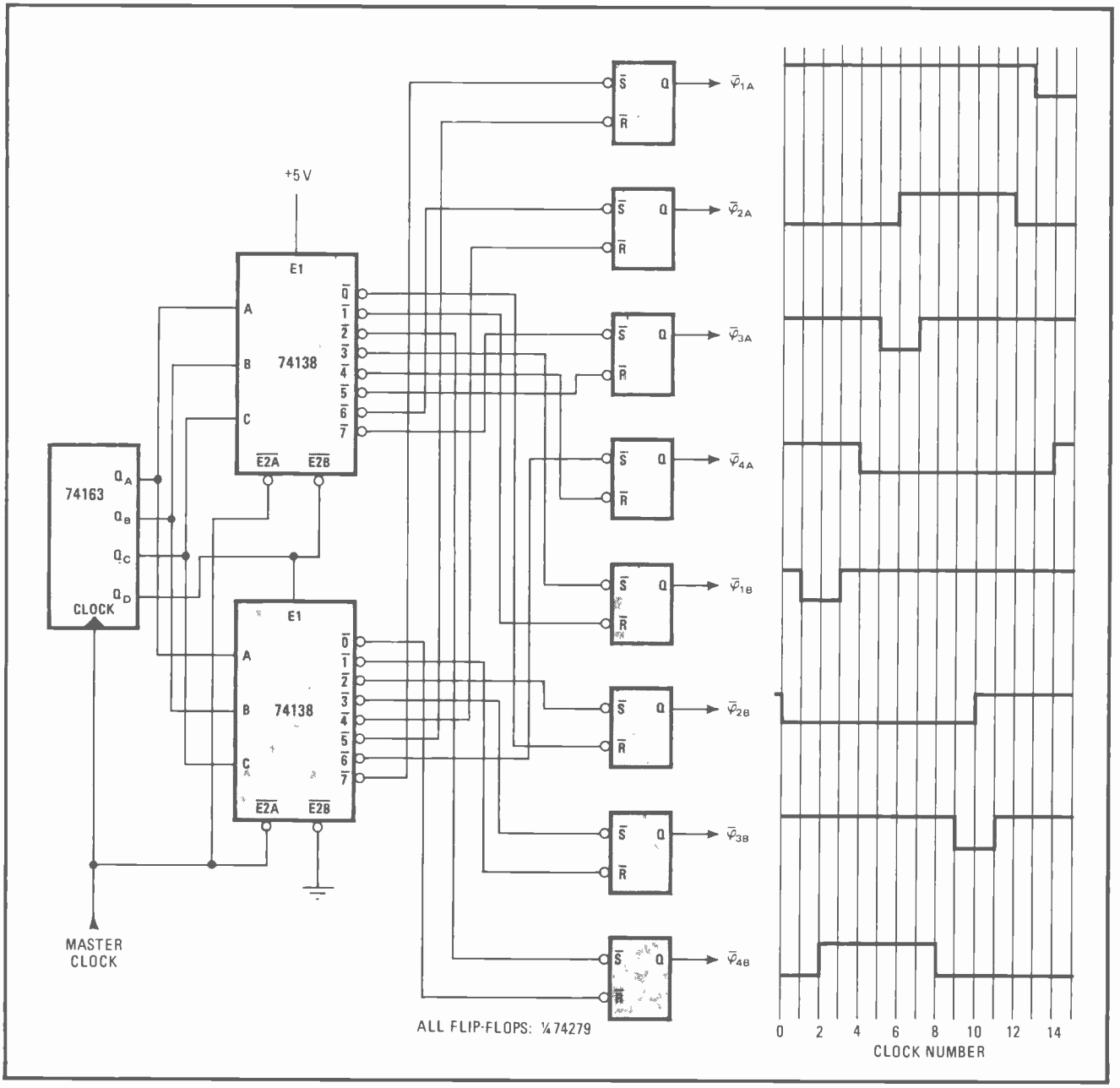
by Craig Bolon
Massachusetts Institute of Technology, Cambridge, Mass.

A multiphase clock suitable for driving circuits with strict timing requirements, such as charge-coupled-device memories, can be built with a counter, decoder, and set/reset flip-flops. This clock can generate any number of outputs at any duty cycle, yet never suffers from the drift and "glitches" encountered in most multiphase designs. Although each signal is phase-locked to a master clock, its timing and duty cycle can be set independently of the others, permitting great flexibility.

The figure shows a typical application—an eight-phase clock designed for driving parallel banks of Intel 2416 CCD memories. A master clock drives the 74163 synchronous 4-bit binary counter. The binary output is then presented to the combinational logic of two 74138 1-of-8 decoders.

The decoders count one pulse on the rising edge of each clock. The first decoder counts eight pulses (0–7) before its outputs are held high by the Q_D output of the binary counter. The second decoder is then enabled and counts an additional eight pulses, after which the 16-count sequence is repeated.

Each decoder output controls an R/S flip-flop by setting or resetting it at the desired moment. Thus, the



Multiphase clock and waveforms. Master clock can be stopped or started at any point in cycle without affecting the phase relationship at all. Skew in output waveforms can be limited to propagation delay of one gate, provided that edge-triggered flip-flops are used.

master clock assures synchronous operation, and the strictly sequential nature of the decoder output keeps it glitch-free for all time.

The clock waveforms are shown to the right of the circuit. Phase 2A of the clock, for example, is generated by setting a flip-flop on count 6 of the 16-count cycle ($\overline{6}$ of the first decoder) and resetting it on count 12 of the cycle ($\overline{4}$ of the second decoder). The number of phases can easily be increased by expanding the binary counter and adding decoders and flip-flops. □

Noise-reducing filter switches time constants

by Martin V. Thomas
Boston University Medical Center, Boston, Mass.

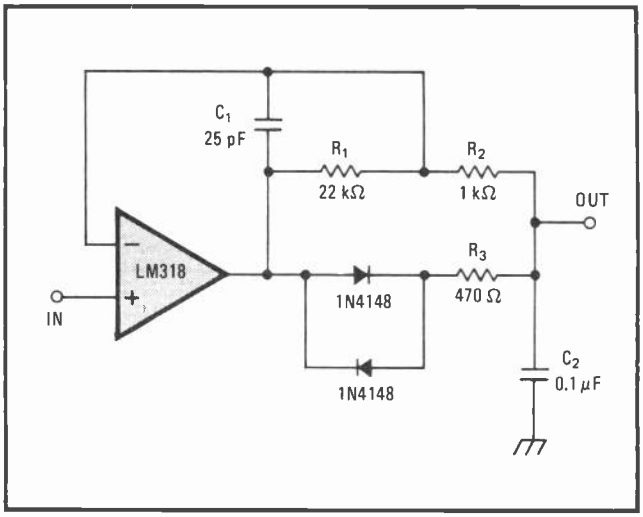
To reduce high-frequency noise in a signal waveform without significantly distorting the signal is often beyond the capacity of conventional low-pass filters. For this purpose, a piecewise-linear filter is far more effective, especially for complex waveforms such as square waves and sawtooth signals.

The circuit shown in Fig. 1 achieves this improvement in signal-to-noise performance and has been used for the precise determination of input-signal amplitudes in the presence of noise. It makes use of the fact that although signal amplitude varies significantly with time, the variation of the root-mean-square value of the superimposed noise with time is smaller and relatively constant. The filter normally has a comparatively long time constant, T_1, but switches to a shorter time constant, T_2, whenever the input signal exceeds a certain threshold. Thus, the circuit allows large transients to pass through it relatively unaffected but filters out smaller variations (noise).

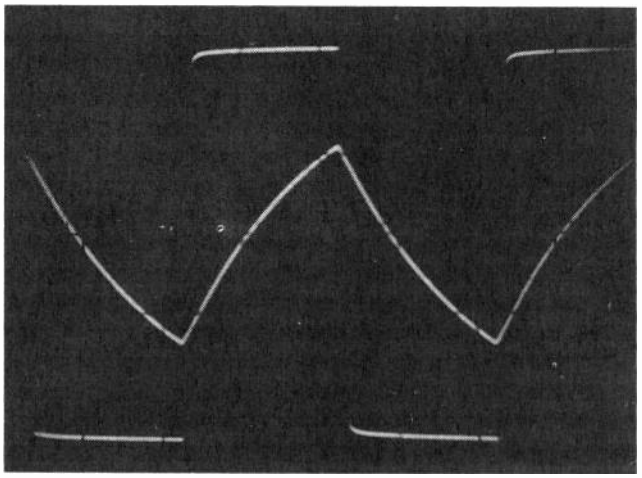
Input-signal voltages to the operational amplifier appear immediately at the junction of resistors R_1 and R_2, so that the normal response time of the circuit is $R_2 \cdot C_2$, or 100 microseconds. If the input is constant or slowly changing in amplitude, there is essentially no difference in voltage between the output and the resistor junction. Low frequencies pass to the output, and noise is reduced by the long time constant of the circuit.

A diode is switched on, however, if the voltage at the junction exceeds the output voltage by $0.7 \cdot R_2/(R_1 + R_2)$ volts, or 30 millivolts in this circuit. Diode switching is possible because of the output voltage lag produced by the RC circuit, and it occurs if a rapidly changing voltage is brought to the op amp's input. An additional current path is established through R_3, and the time constant of the circuit becomes approximately $R_3 \cdot R_2 \cdot C_2/(R_1 + R_2)$, or 2 microseconds, assuming R_3 is much less than $R_1 + R_2$. This allows the high-frequency transient to pass through to the output, virtually undistorted. Although any noise superimposed on the signal at this time passes through also, the circuit's average signal-to-noise ratio for the entire band of frequencies is much higher than can be expected with conventional circuits.

Outputs of the filter with a 1-volt, 5-kilohertz square wave input are shown in Fig. 2. The square wave is



1. Dual-value response-time filter. For best performance, C_2 is made relatively large. R_3 maintains stability by limiting charge current, C_1 prevents oscillation in feedback loop.



2. Square-wave response. Square-wave output is result of circuit's use of a short as well as a long time constant. If filter uses only long time constant, overfiltered triangular waveform results. Full square-wave output yields higher signal-to-noise ratio.

undistorted since both time constants are utilized. The superimposed triangle wave shows the resulting distortion if the long time constant alone is used.

The filter's time constant and diode switching threshold can be varied within a reasonable range. Under some conditions it may be desirable to limit the input signal bandwidth to the inverse value of the short time constant, in order to minimize distortion caused by overshoot. □

Sample-and-hold and op amp form special differentiator

by John Nolte
University of Colorado Medical Center, Denver, Colo.

A sample-and-hold module and an operational amplifier can form a differentiator circuit that is especially useful at very low frequencies. In both accuracy and noise immunity it leaves conventional differentiators far behind, even when they are built with highest-quality components, i.e. low-drift, high-input-impedance amplifiers and high-value, low-leakage capacitors.

High-frequency noise, which can upset the operation of the common RC differentiator, is no problem with this "digital" circuit because its gain is independent of the noise frequency. In addition, its frequency of operation is set simply by adjustment of the sampling frequency. The circuit is therefore capable of a wide frequency response, quite unlike its analog counterpart, in which the components selected to reduce high-frequency noise also narrow the frequency response.

In essence, this circuit solves the equation for the slope of a line. The equation may be expressed as:

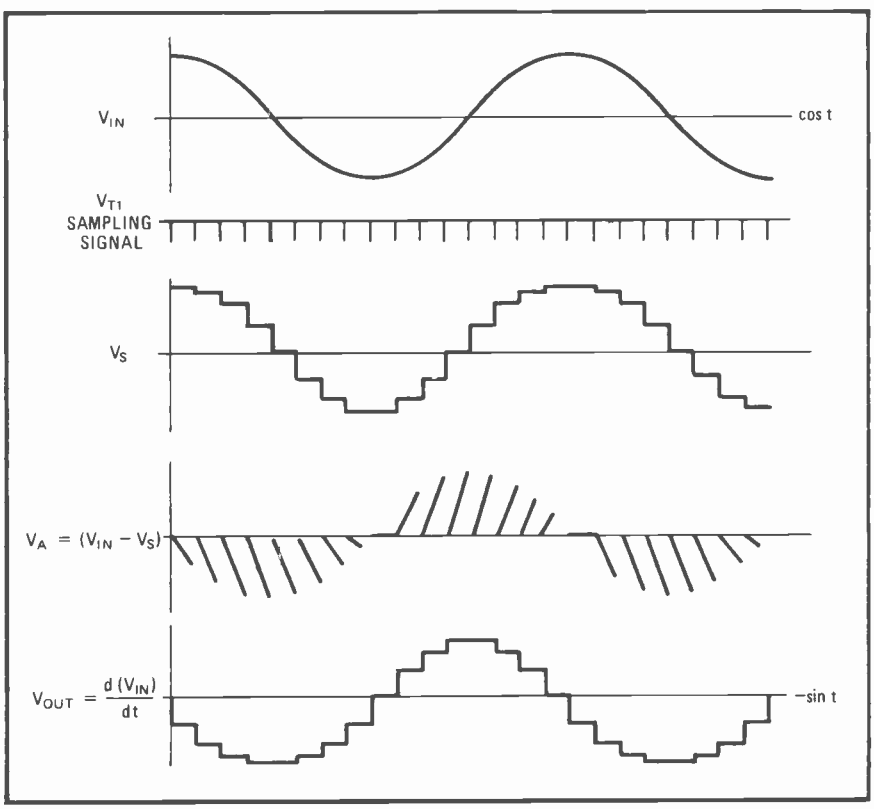
$$E_f = d(e)/dt$$

where E_f is the final output voltage at the time immediately before the next sample, and d(e)/dt is the change in input voltage between sampling intervals, or the derivative of the input signal with respect to time. The output waveforms in Fig. 1 indeed confirm this equation. How is the output generated?

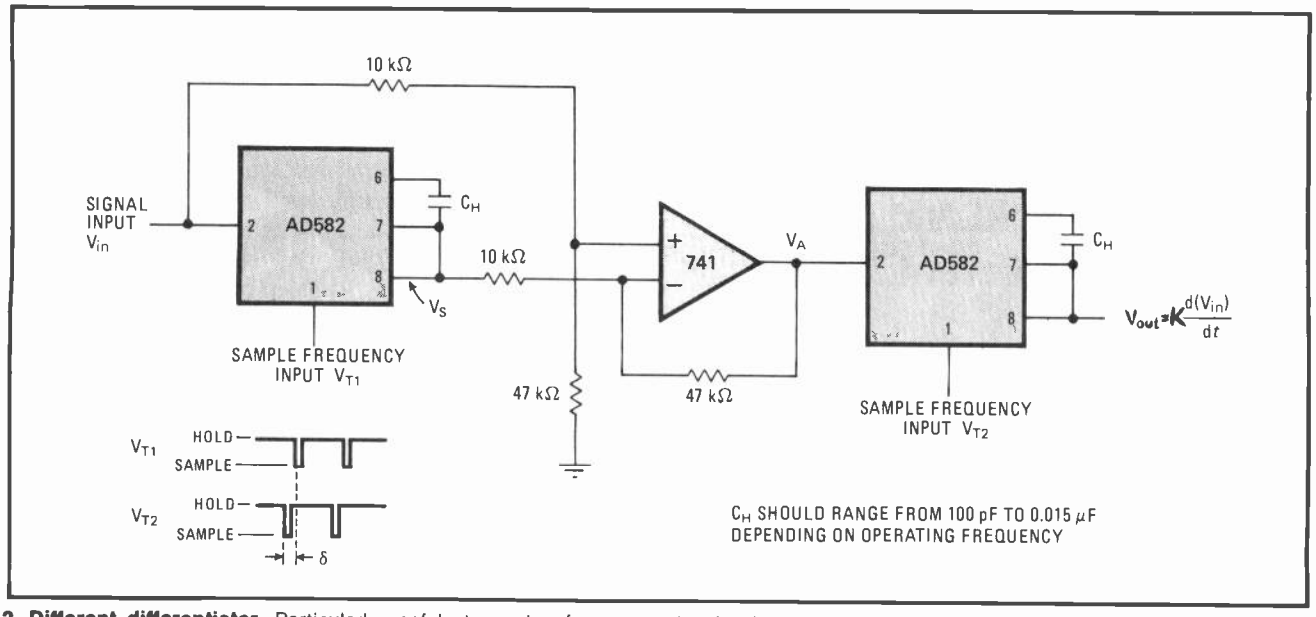
As shown in Fig. 2, the input signal V_{in} at pin 2 is sampled at a frequency introduced at pin 1 of the AD582 sample-and-hold device. The output of this device charges capacitor C_H with the instantaneous V_{in} potential at the sampling instant; therefore the output signal V_s is a staircase approximation to V_{in}, for a small sampling time with many samples taken per input frequency. (For clarity's sake the waveforms in Fig. 1 show a disproportionately low sampling frequency.) The difference between V_s and the original input frequency V_{in} is amplified by the 741 operational amplifier.

During each sampling period, the difference between these two signals is zero, making the output of the 741 (V_A) also zero. However, during each hold period, the output of the op amp rises to a value proportional to the change in input voltage with time. This proportionality is more or less linear, because of the small change in V_{in} versus V_s during a single sample period.

The output of the 741 is therefore a sawtooth waveform with an envelope (formed by the sawtooth peaks) approximating the derivative of V_{in}. To yield a true staircase approximation of the derivative, a second sample-and-hold device can be used to sample the peaks



1. Sample waveforms. Input signal V_{in} (shown here as cos *t*) is sampled at rate V_{T1}, and sample-and-hold output V_S is a sawtooth with an envelope that is the derivative of V_{in}, or $-\sin t$. Final sample-and-hold produces staircase of derivative, V_{out}.



2. Different differentiator. Particularly useful at very-low-frequency signals, this differentiator uses a sample-and-hold and a difference amplifier to obtain the slope of the waveform. Second sample-and-hold recovers peaks of differentiated waveform. Negative pulse train (duty cycle approximately 1%) for sampling signals can be generated by a 555 timer circuit.

of the sawtooth, thus removing the unwanted components generated by the first sampling module.

For reasonable accuracy in differentiating a signal, the sampling frequency should be at least a few times, but preferably on the order of 100 times, greater than the input frequency. Decreasing the sampling frequency will lower the input frequency that produces a full-scale or maximized-value output. □

FET pair and op amp linearize voltage-controlled resistor

by Thomas L. Clarke
Atlantic Oceanographic and Meteorological Laboratory, Miami, Fla.

A matched field-effect transistor pair can be combined with an operational amplifier and a few resistors to form a circuit in which one FET's drain-to-source resistance (R_{ds}) bears a precisely linear relationship to a control voltage (V_c). Though a single FET can serve as a voltage-controlled resistor, the relationship of R_{ds} to the gate-to-source voltage (V_{gs}) is nonlinear.

The basic idea in this circuit is to control V_{gs} through a feedback loop that senses if the amount of current flowing through the FET, and hence its R_{ds}, is of the proper value. As shown in Fig. 1, this is accomplished by deriving a signal from half of the FET and applying it to a "summing" node at the inverting port of an op amp.

The output of the op amp is connected to the gate of the FET, thus forming a closed loop. The resulting change in V_c causes a proportional change in R_{ds} because the op amp is a linear device, and because input voltages are compared to a fixed voltage (V_{ref}) at the noninverting terminal. Depending on the configuration, R_{ds} can be made proportional to V_c or its reciprocal.

In the circuit to be seen at the left of Fig. 1, R_{ds} varies in proportion to the reciprocal of the control voltage, as is indicated by the following equation:

$$R_{ds} = |V_{ref}|R_c/(|V_d|-|V_{ref}|)$$

where V_{ref} is assumed to be between 0 and V_c. A voltage divider may be used to derive V_{ref}. Moving V_{ref} to the drain of the FET, as in the circuit to the right, the following equation holds:

$$R_{ds} = |V_{ref}|R_c/|V_d|$$

where V_{ref} should be a well-regulated source, since it may have to supply considerable current. These equations are based on the facts that V_c draws current from the negative input of the op amp through R_c and that this voltage drop results in current flow into the terminal by the FET. The application of Kirchhoff's law then yields the above relationships.

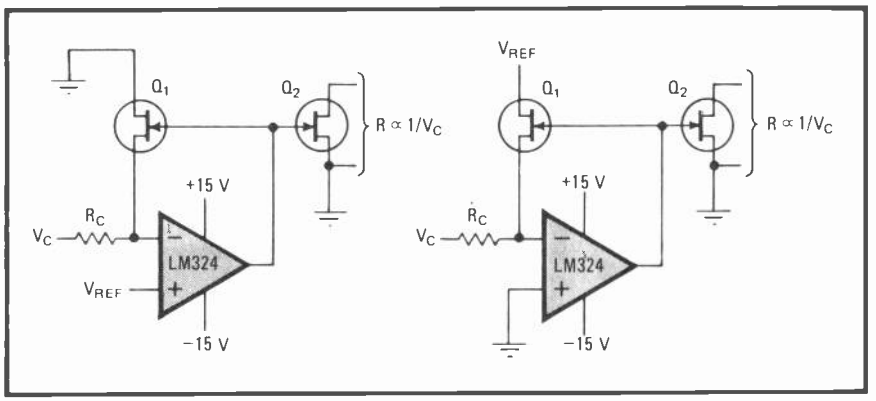
As shown in the circuit at the left of Fig. 2, R_{ds} may also vary in direct proportion to the control voltage. Therefore, the relationship becomes:

$$R_{ds} = R_d|V_d|/(V-|V_d|)$$

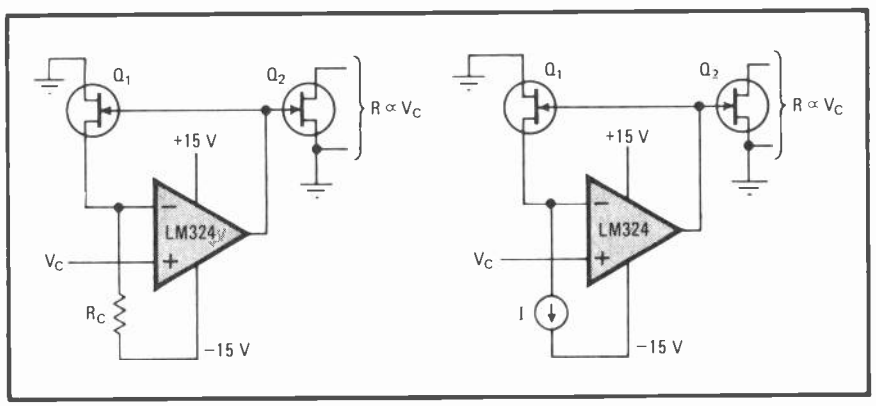
where V_c is greater than $-V_p$ but less than 0 v. This circuit, while not as linear as those of Fig. 1, can be improved significantly by replacing R_c with a current source, I, as shown at the right of Fig. 2. The relationship then simply becomes:

$$R_{ds} = |V_d|/I$$

The circuits are built with Siliconix 285 dual FET chips and LM324 op amps. Use of high-speed op amps such as the LM318 would permit more rapid variations of resis-



1. Voltage-controlled resistance. Unused half of FET Q_2 can function as voltage-controlled resistor in external circuits. R_{ds} is inversely proportional to control voltage in both circuits. V_c values are negative for n-channel FETs, positive for p-channel FETs.



2. Direct proportional control. R_{ds} varies linearly with V_c in both circuits. If V_c exceeds V_{ref} or breakdown voltages of FET in either figure, a resistor should be inserted between output of operational amplifier and gate of FET to prevent burnout.

tance. No stability problems are encountered because the FET introduces negligible phase shift in bandpass frequencies of the op amp. Optimal results are obtained, of course, with FETs formed on a common substrate, and if desired, p-channel devices may be used for positive control voltages. □

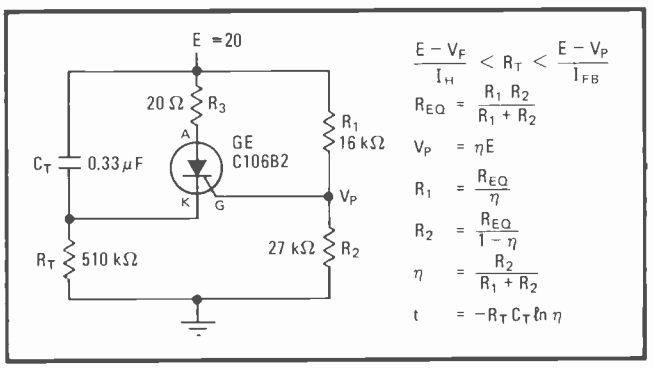
SCRs make serviceable relaxation oscillators

by Larry P. Kahhan
Princo Instruments Inc., Southampton, Pa.

Few designers realize that a silicon controlled rectifier can be used as a relaxation oscillator, just like its sister thyristor, the programmable unijunction transistor. The circuit arrangement is much akin to the PUT oscillator, as shown in the figure.

When power is applied, capacitor C_T charges, and the voltage across resistor R_T decreases exponentially. When the voltage across R_T, which is the cathode voltage of the SCR, drops to 0.6 volt less than the gate voltage, the SCR turns on. This turn-on produces current flow through C_T and a voltage spike across R_3.

Since the large value of R_T prohibits there being sufficient current to maintain conduction, the SCR immediately turns off, and C_T begins its charge cycle again. The period of oscillation is approximately given by $t = -R_T C_T (\ln \eta)$, where η is the fraction of the supply voltage that is applied to the gate, or $R_2/(R_1 + R_2)$. The high-impedance (500-kilohm) sawtooth-waveform output is available at the SCR's cathode, and a pulse waveform appears at its anode. The output impedance at this point is less than 20 ohms. If a high-current pulse is desired, a pulse transformer might replace R_3.



Programmability. An SCR oscillator retains the features of a unijunction-transistor circuit, including programmability of the firing point. Values shown yield an oscillation frequency of about 15 Hz. Gate-to-cathode voltage drop is neglected in the equations.

Design equations in the figure outline the criteria for oscillation. Values for SCR on-voltage, holding and forward blocking currents may be obtained from the data sheets. □

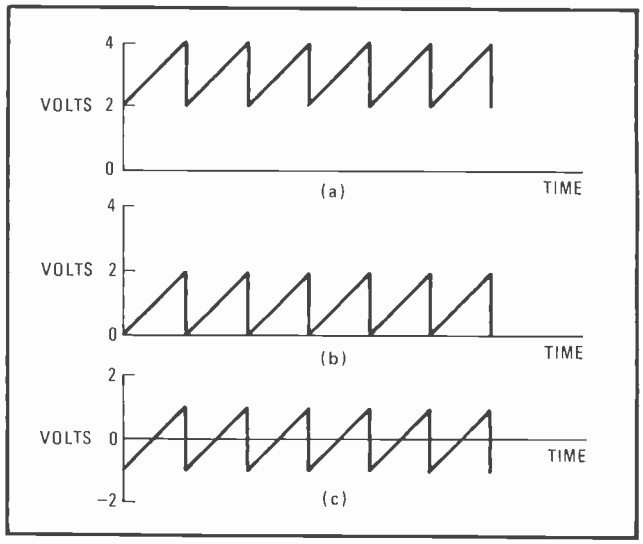
Automatic clamp controls symmetrical wave-form offset

by George O. Wright
Washington, D.C.

It is often necessary to shift the dc level or offset of a signal. Driving transistor-transistor-logic circuits, for example, requires positive-only signals, but sometimes circuits may need negative-only signals, or symmetry of a wave form about a given dc level may be required. An inverting operational amplifier, an integrator, and a half-wave rectifier can be used to form such an offset control simply and inexpensively.

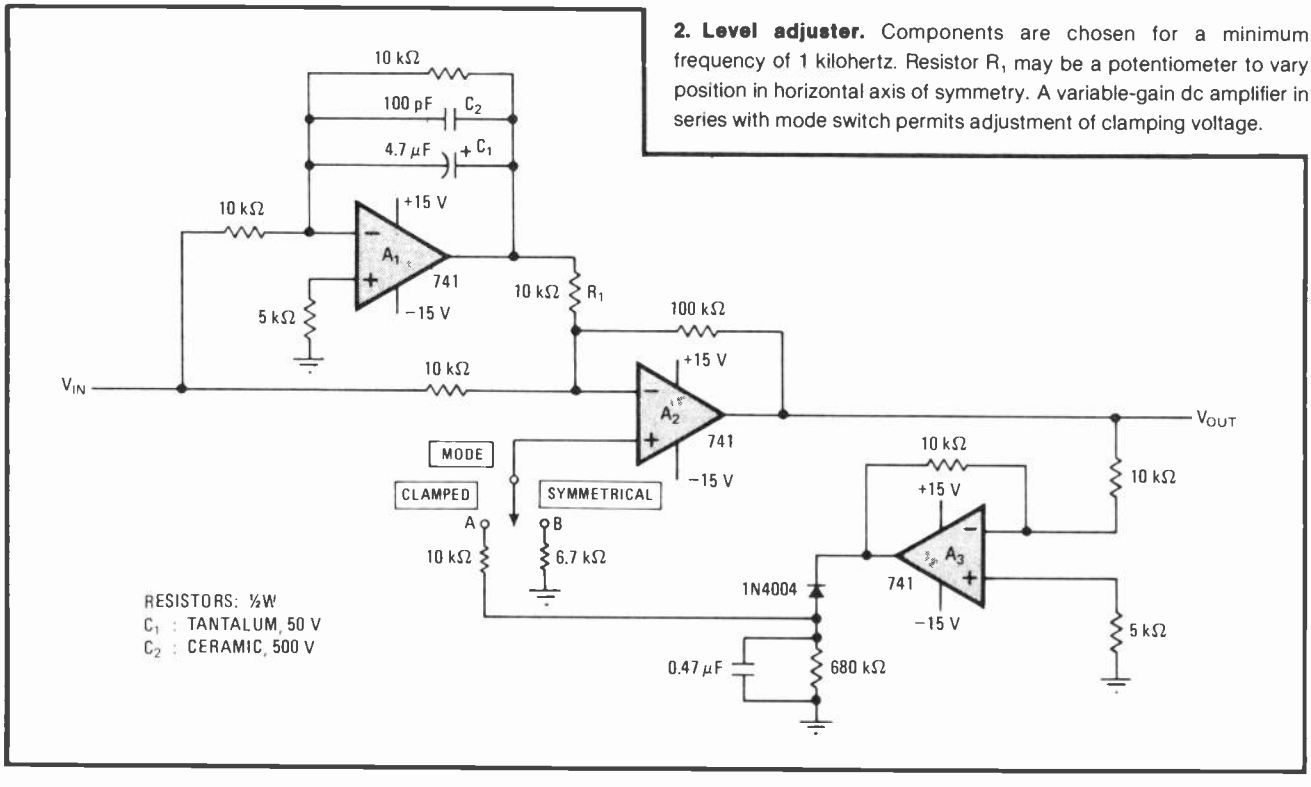
At the flick of a switch, this circuit clamps the input level at almost any desired value (Fig. 1). Operation of the circuit is based on the principle that the dc value of any periodic wave form can be found by integration. Since the input is dc-coupled, the integrator output V_{dc} will be equal to the dc component of the signal plus any initial dc offset. As a consequence of its integrating operation, the circuit can generate an output symmetrical about the zero axis.

As shown in Fig. 2, the input signal, which may be a sine, triangle, square or ramp wave form, is summed with the inverted output of the integrator A_1 at the inverting input of op amp A_2. The input wave form at this point is displaced downward by an amount equal to its integrated voltage value V_{dc}.



1. Symmetry or clamping desired? Input ramp at (a) is clamped to zero (b) or is symmetrical about zero (c). Circuit may be modified so that clamping to nearly any voltage level is possible.

To clamp the output at 0 v, the mode switch is placed in position A. The reference level at the noninverting input of the differential amplifier A_2 becomes minus half its initial peak output swing because of the signal's subsequent peak detection at the output of A_3. Operation of amplifiers A_1 and A_2 assure that the initial signal to



2. Level adjuster. Components are chosen for a minimum frequency of 1 kilohertz. Resistor R_1 may be a potentiometer to vary position in horizontal axis of symmetry. A variable-gain dc amplifier in series with mode switch permits adjustment of clamping voltage.

A_3 is symmetrical about 0. The polarity of the output voltage depends on the orientation of the diode—for the direction shown, it is positive-going.

To clamp the output at some other value than 0 v, the mode switch must again be placed in position A, and a dc amplifier must also be inserted in the loop between the rectifier output and the noninverting input of op amp A_2 to control the value of the reference signal.

If the mode switch is placed in position B, the output will always be symmetrical about the zero axis, no matter what the original input level is. This operation is roughly equivalent to removing the integrator from the circuit and placing a capacitor in series with the input lead to block the dc component of the signal.

Component values in the integrator circuit shown will effectively process signals of 1 kilohertz and higher, up to the frequency limit of the op amp. In general, the circuit will process almost any signal that is symmetrical about a horizontal axis. The exception is pulse trains of single polarity: their short duty cycle makes a symmetrical output impossible because the dc component is less than half the peak value. In this case, R_1 may be adjusted to provide the desired output level, which can be varied over a small range. □

Bi-FET devices improve absolute-value amplifier

by Dan L. Vogler
Lintech Electronics, Albuquerque, N.M.

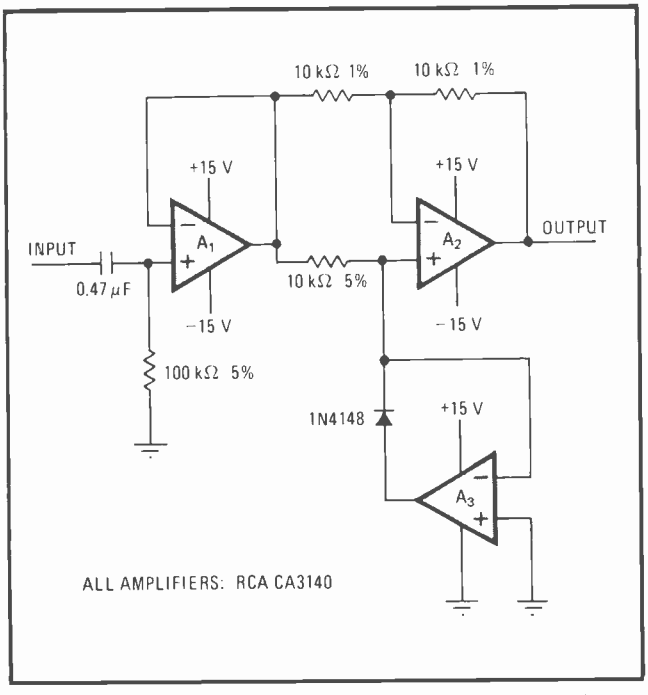
An absolute-value amplifier, also known as a precision full-wave rectifier, which features wide bandwidth and dynamic range, can be built with high-impedance operational amplifiers to produce a circuit that is more reliable than those implementing the usual phase-cancellation technique. The low input current and wide frequency range of the CA3140 bipolar/field-effect-transistor op amps eliminate the gain and phase-shift errors encountered in other designs.

As shown in the figure, op amp A_1 serves as a unity-gain buffer, op amp A_2 has a gain of $+1$ during the positive half-cycle of the input wave and a gain of -1 during the negative portions, and A_3 in association with the diode forms a precision clamp.

During the positive portion of the input signal equal voltage is present at both inputs of A_2. The op amp behaves as a unity-gain follower, as determined by the feedback elements.

During the negative portions, however, the clamping action of A_3 with the diode prevents the voltage at the noninverting input of A_2 from going negative, effectively tying the pin to ground. Op amp A_2 therefore either operates in the inverting mode or else multiplies the signal by a factor of -1.

Precision resistors for the gain-controlling elements of op amp A_2 assure no greater than 2% deviation from the desired gain. The clamping circuit of A_3 can accurately process signals down to -0.3 volt below the negative supply rail of the amplifier, which in this case is ground.



Precision full-wave rectifier. Op amp A_3, which ensures A_2 follows positive voltages and inverts negative ones, has single-ended power supply to minimize slew time and maximize stability. Power-supply pins are decoupled with 0.47-μF capacitors.

The result is an absolute-value amplifier which has a dynamic range exceeding 90 decibels and a bandwidth exceeding 1 megahertz. When this circuit is used in conjunction with a peak detector or integrator network, it becomes an invaluable building block in ac-to-dc conversion applications. □

555 timer IC freezes digital panel meter display

by Howard M. Berlin
Wilmington, Delaware

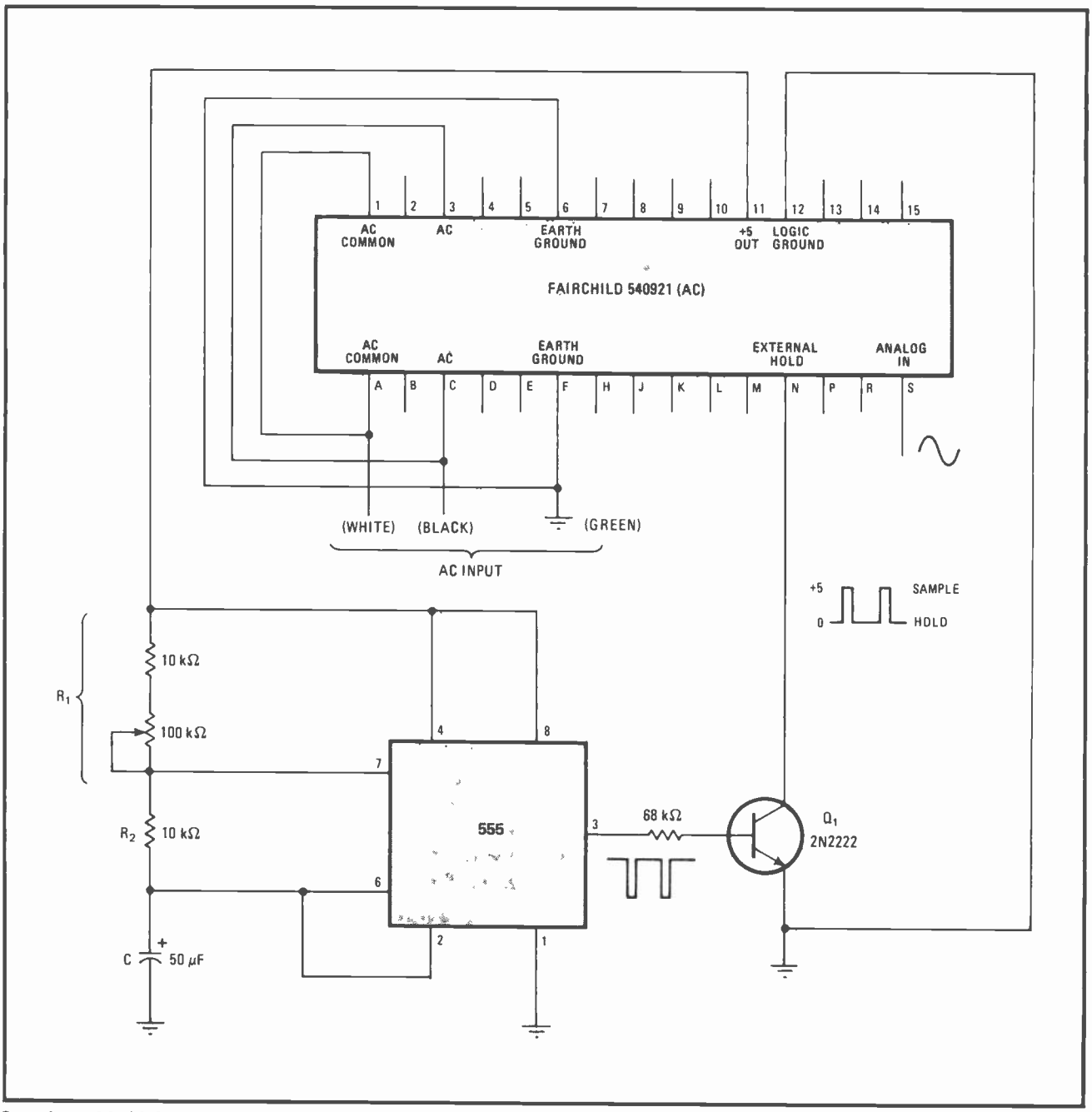
Connecting a 555 timer as an astable multivibrator produces a sample-and-hold circuit that will increase the display time of many digital panel meters. This increase is an advantage in situations where the displayed value changes rapidly, making it difficult to determine an average reading. For example, a sensor monitoring pressure changes near a source of mechanical vibration can produce readings on a 4½-digit DPM that vary as much

as ±10 digits in a quarter second, making a visual approximation virtually impossible.

When used with a DPM with an external-hold input such as the 4½-digit Fairchild 540921, the 555's signal overrides the internally controlled sampling period at pin N of the meter (see figure). The external-hold port is level-sensitive, so it is desirable to sample the test signal for short times. The output of the timer is a pulse train with a duty cycle of $d = (R_1 + R_2)/(R_1 + 2R_2)$, which can approach 100%, and a frequency of $f = 1.443/C(R_1 + 2R_2)$ hertz.

The 555 output is inverted by transistor Q_1 so that a logic 1 is periodically presented to the external-hold input to sample the input analog voltage at pin S for a time that is small compared to the total sampling time. When the collector of the transistor is at logic 0, the sample is held and displayed for the number of seconds determined by the ratio d/f. With the values shown, the signal can be displayed for times ranging from 0.7 to 4.2 seconds. Updating is possible every 1 to 4.5 s.

Power for the timer is obtained from the meter, and the current drain is only 4 milliamperes. The circuit has been used for controlling several DPMs simultaneously, with additional transistor circuits connected to pin 3 of the timer. □



Sample-and-hold timer. A 555 extends the display period to relax hyperactive digital panel meters. The display can be frozen for 0.7 to 4.2 seconds, and updated every 1 to 4.5 seconds. Power for the circuit can be obtained from the DPM's 5-volt supply or a battery source.

Intelligent multiplexer increases processor efficiency

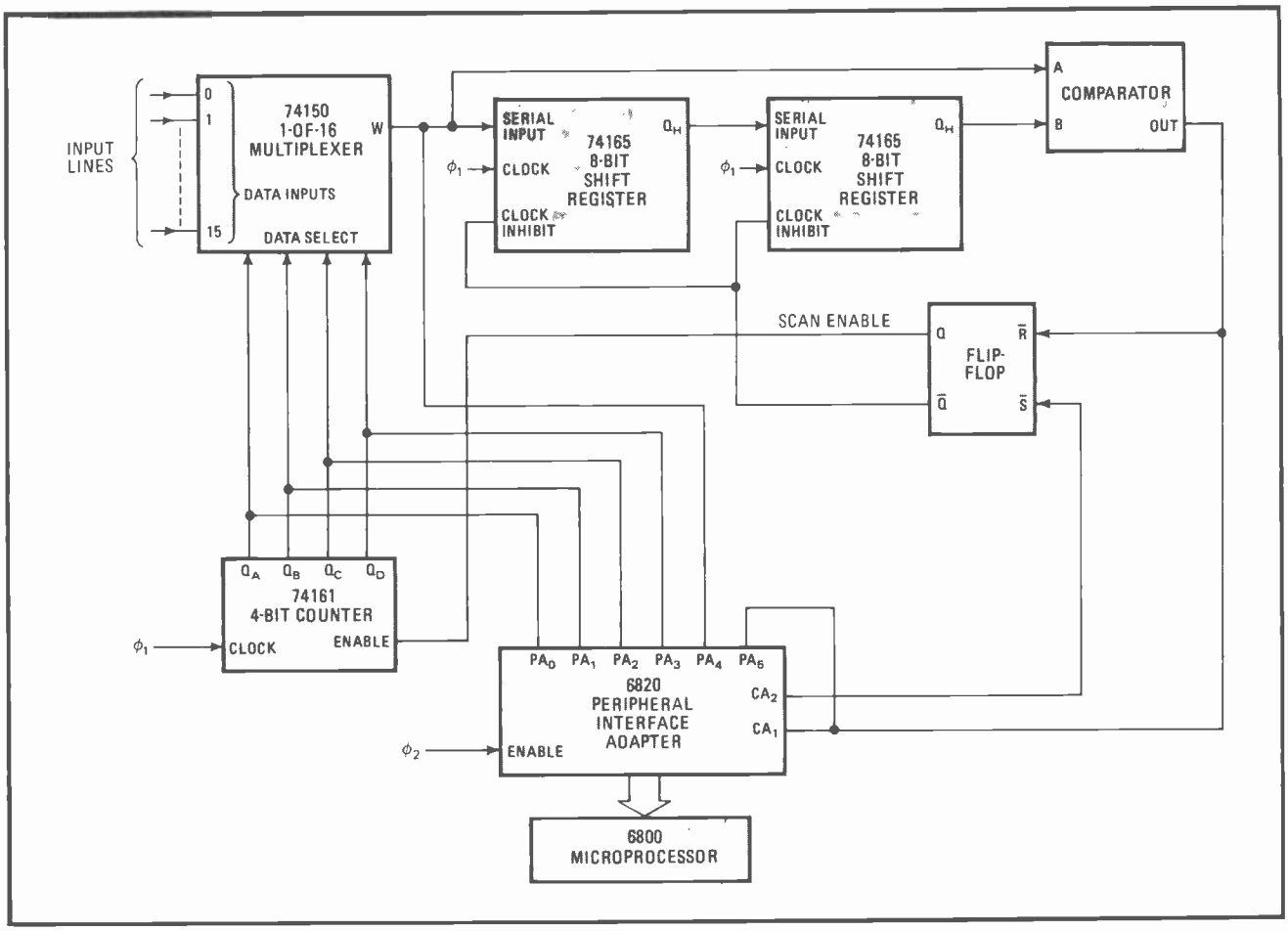
by Edward Harriman
Boston, Mass.

The most efficient way to multiplex data into a computer is to initiate interrupts only when necessary. This circuit does just that. It polls the input lines and only in the event of an input change does it interrupt the processor, otherwise freeing it to attend to other tasks and therefore speeding overall system operation.

Shown in the figure, the circuit has worked successfully with the Motorola 6800 microprocessor. The hardware includes a 74150 1-of-16 multiplexer, a 74161 4-bit counter for encoding each line, and two 74165 8-bit shift registers for recording the previous state of each line. These elements, in conjunction with a standard comparator and $\overline{RS}$ flip-flop, control the actions of a 6820 peripheral interface adapter feeding the microprocessor.

To initialize the system, the microprocessor loads the 16-bit shift register (the two 74165 devices) by performing 16 read operations. The counter, which like most of the circuit is cycled by the system clock, selects each of the multiplexer's 16 input lines in turn. Assuming the system was initialized at line 0, on the 17th read operation the input of that line appears at the multiplexer's output and is fed to the comparator to be checked against the previous 0 line bit now stored in the last stage of the 16-bit shift register. If the comparator detects a difference in the two logic levels, it generates an interrupt to the processor through the peripheral interface adapter and also resets the flip-flop. This forces the scan-enable line low, disabling the counter.

Meanwhile, whether or not there has been a change from the previous state, the multiplexer's output is stored in the shift register. After 16 scans, the output of the last stage of the shift register is again compared to the present state of the input location 0. The loading and



Smart controller. Sixteen lines are multiplexed to microprocessor, which performs input update only when notified of a state change on any line. The 6820 peripheral interface adapter is programmed to generate interrupt on negative transition of CA_1, which in turn generates negative-going CA_2 to advance counter by one. For eight input lines, an eight-input multiplexer and just one shift register would be used.

comparison operation takes place each scan for every input line.

If an interrupt is generated, the microprocessor, through prior programming, reads the location of change and the new data through the peripheral interface adapter. This operation also sets the flip-flop by generating a negative-going pulse from the control line CA_2. The pulse sends the flip-flop's Q output high for at least one cycle, enabling the 4-bit counter to advance one count, regardless of the state of the comparator that initiated the halt. The microprogram is written to observe if this second scan encounters a change in the state of the next location—a more efficient procedure than releasing the microprocessor immediately. This is done by testing line CA_1, the interrupt-status control line, which is connected to the comparator output. □

ICs slash component count in Costas loop demodulator

by Carl Andren
E-Systems Inc., St. Petersburg, Fla.

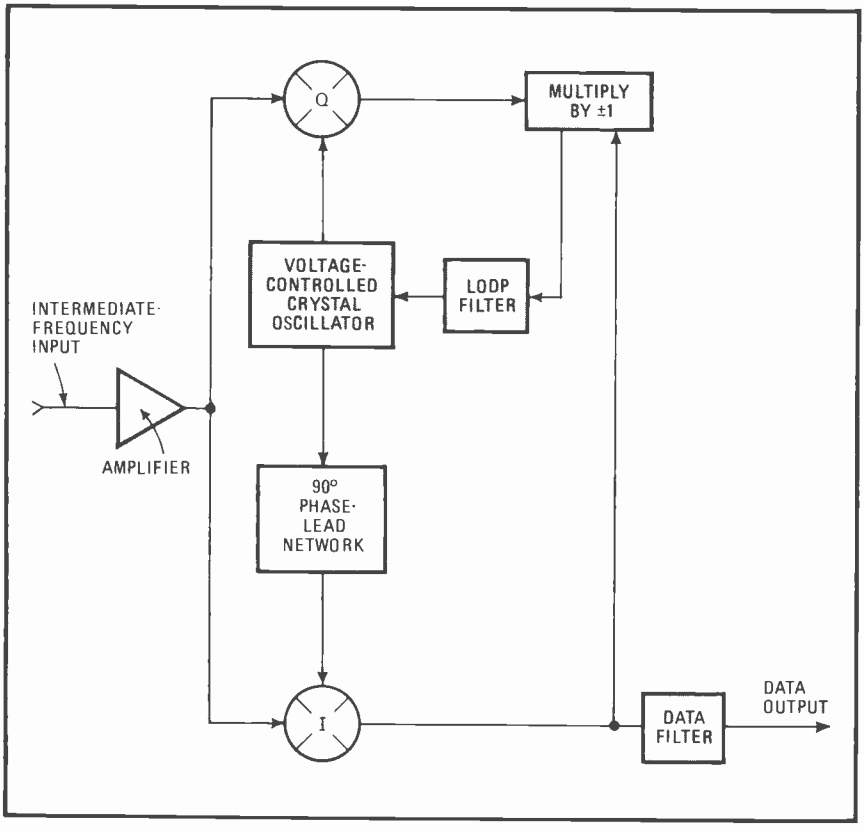
Just three integrated circuits can build a Costas phase-locked loop that will detect differential phase-shift-keyed modulation. The Costas loop is named after its inventor, who first detected it with a PLL by regenerating the carrier in a double-sideband suppressed-carrier signal. The loop allows tracking of the desired frequency in a high-noise environment while ignoring carrier phase reversals caused by modulation.

The Costas loop (Fig. 1) has an input signal split into two channels. The in-phase channel (I) demodulates the data, and the quadrature channel (Q) tracks frequency and phase of the carrier.

The key to the loop's operation is the multiply-by-±1 function, which inverts the phase of Q's output signal upon detection of a carrier phase reversal. This inversion is reflected in the feedback signal and maintains lock in the voltage-controlled crystal oscillator. The I channel, which detects the phase change, determines if the Q-channel output is to be inverted or multiplied by unity.

In the demodulating circuit of Fig. 2, the two CA3089 frequency-modulated intermediate-frequency systems and the MC1558 operational amplifier take over the Costas loop functions. This circuit was optimized for a data rate of 9.6 kilobits per second in a system with an intermediate-frequency bandwidth of 40 kilohertz.

The CA3089s replace more than 70 devices usually needed for the Costas loop. A_1 fills the Q-circuit function, while A_2 is wired to serve as the I circuit. The high-gain limiting amplifiers of A_1 and the monolithic two-pole crystal-filter in conjunction with the IN5462 varactor make up the voltage-controlled crystal oscillator. The loop filter consists of the RC network that drives the varactor. The MC1558 (A_3) serves the multiplier function. Data filtering is accomplished by capacitive loading (4,700 picofarads) at the output of A_2 in



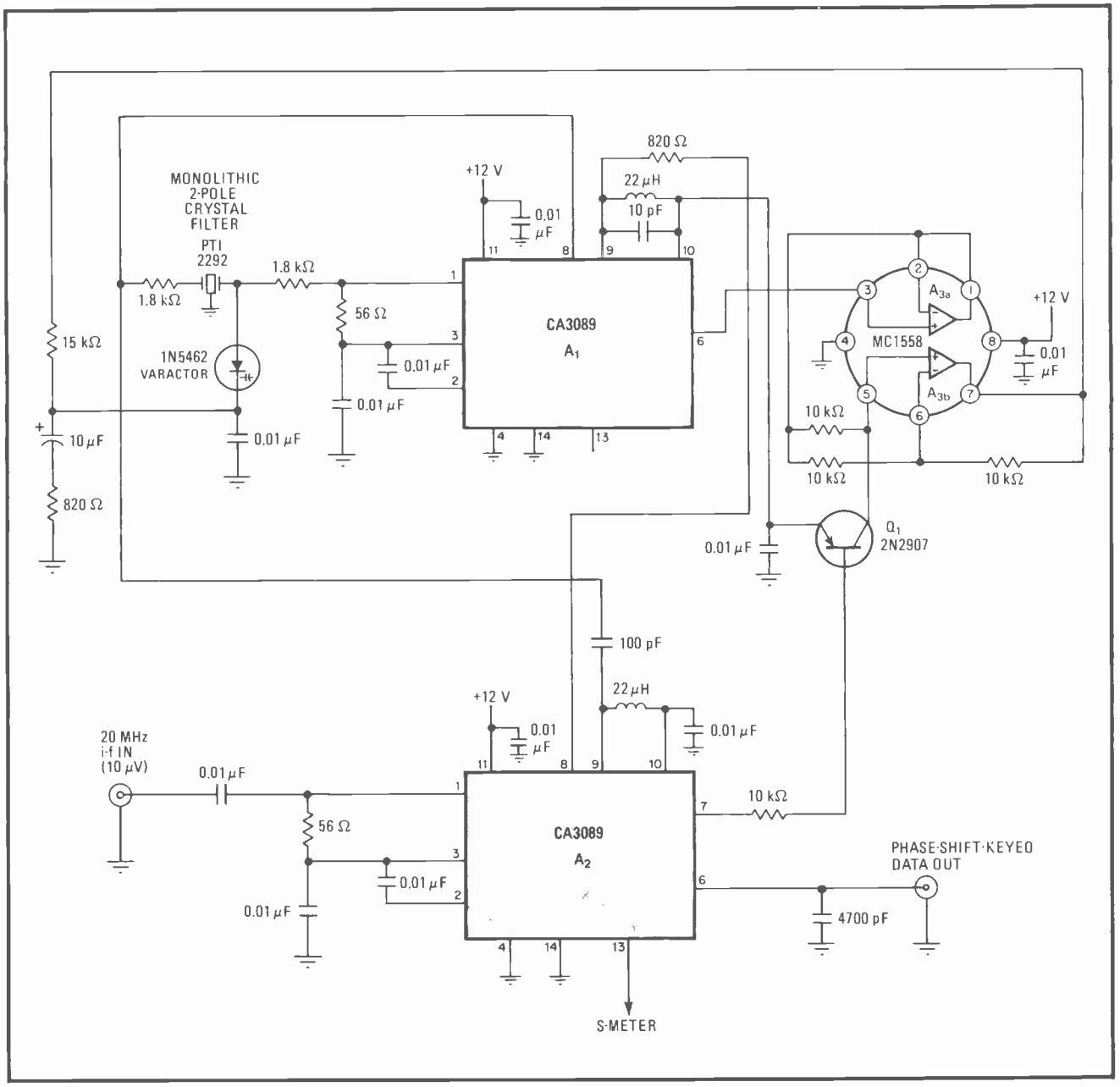
The Costas loop. An intermediate-frequency input signal is compared to the voltage-controlled crystal oscillator signal, and two quadrature signals are generated. The output from the Q (quadrature) channel is multiplied by ±1 depending on phase detected by the I (in-phase) channel. The feedback loop facilitates tracking of the carrier frequency in high-noise environments and maintains locking despite phase reversals of the carrier caused by modulation.

conjunction with the device's output impedance.

At the input of A_2, an i-f signal at 20 megahertz is amplified by the device's high-gain amplifiers, which provide three stages of amplification before presentation at the I-channel quadrature detector or mixer. A simple output buffer in this detector links it with the Q-channel quadrature detector in A_1, thus driving the mixers in both devices with virtually no phase difference.

The I-channel mixer is a balanced transconductance amplifier, biased relative to pin 10 of A_2. It is driven by the i-f input signal, as well as by the oscillator through a 90° phase-lead network. Its output drives two amplifiers in A_3; A_{3a} is in the feedback loop to the oscillator, and A_{3b} controls the multiply function through a transistor. The noninverting amp A_{3a} drives the op amp A_{3b}. The gain is −1 when transistor Q_1 is on and +1 when the transistor is off.

The multiplier's action causes a feedback voltage that varies the oscillator's frequency through the varactor in the tank circuit of the oscillator, and phase lock is readily accomplished. The phase shift of the oscillator's amplifier network is about 360° at 20 MHz, and the crystal filter element has no phase shift at its center frequency—thus allowing smooth operation near the lock frequency. The loop filter is designed to provide the correct loop damping and gain coefficients needed for proper operation. □



2. Differential-PSK demodulator. Two CA3089 phase-locked loops vastly reduce hardware needed for Costas loop demodulator. The circuit detects differential phase-shift-keyed signals with an i-f input of 20 megahertz. With proper attention to rf grounding and shielding, the detector can operate with signals as low as 10 microvolts. An S meter can be connected to pin 13 of A_2 for indicating signal strength.

Self-gating sample-and-hold controls oscillator frequency

by Peter Reintjes
Research and Design Ltd., Morehead City, N.C.

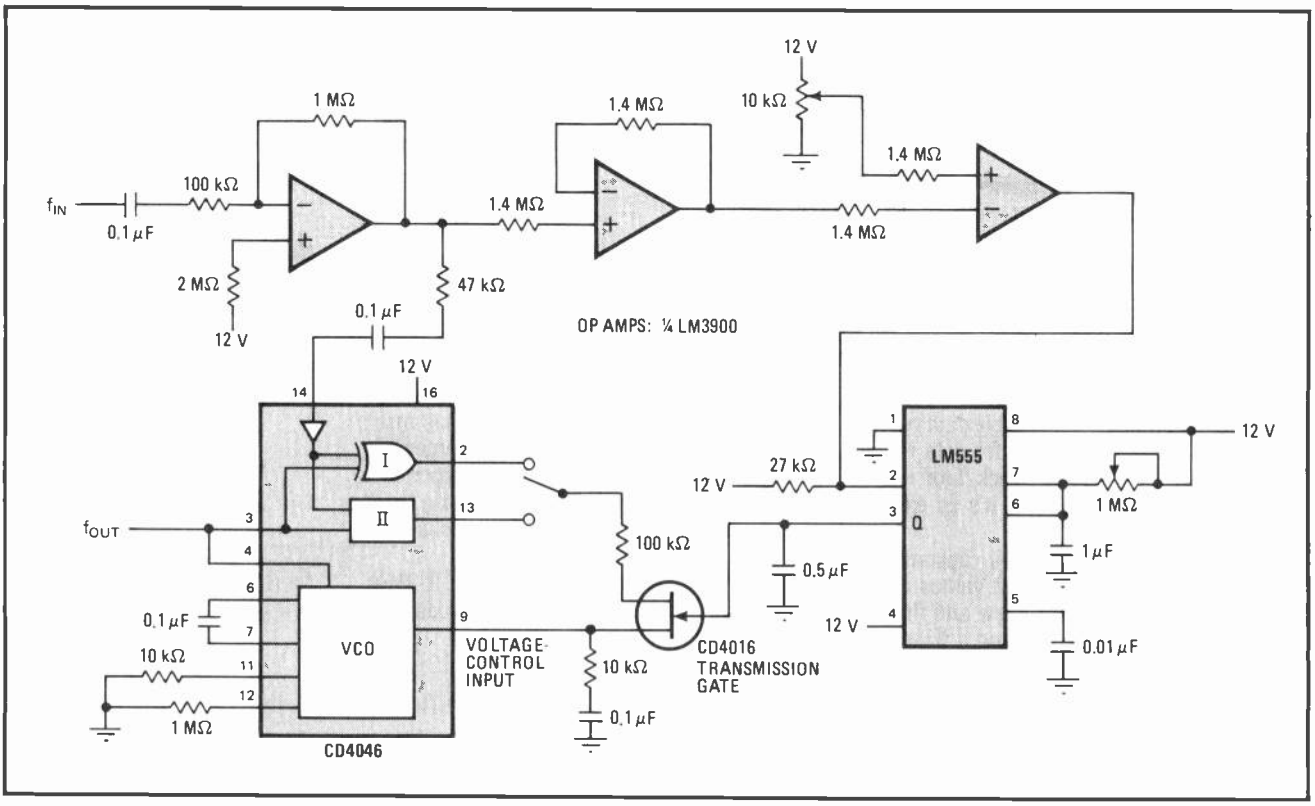
A phase-locked loop in conjunction with a transmission gate serving as a sample-and-hold device can remember the frequency of a short-duration signal by providing a constant feedback voltage to a voltage-controlled oscillator. The circuit is useful for electronic-music synthesis and tuning radio oscillators by remote push button, as well as other applications.

The circuit can sample and hold frequency bursts without the error introduced when the direct conversion of an input frequency to a voltage or digital quantity is attempted. As shown in the figure, a relatively high-level, short-duration alternating-current input signal is amplified, buffered and compared to a user-determined reference by the three operational amplifiers in the LM3900 device. The output of the last stage drives the 555 timer, which serves as a monostable multivibrator (one-shot). The input signal also drives the CD4046 phase-locked loop.

As the one-shot periodically fires in response to the input signal, the transmission gate conducts, completing the feedback loop in the PLL. This permits the output of a selected comparator in the PLL to feed the voltage-controlled oscillator at pin 9. The output of the comparator is a function of the difference between input and VCO output frequencies; the resulting current charges the RC network in the feedback loop consisting of the 10-kilohm resistor and the 0.1-microfarad capacitor. The final dc voltage, across pin 9, controls the VCO frequency and becomes constant when the input and VCO frequency match.

When the amplitude of the input signal fades, thus signalling the end of the burst, the feedback loop is opened because the 555 no longer fires. The voltage across pin 9 remains, however, because the high-input impedance of the VCO terminal prevents negligible leakage by the RC network. Therefore the VCO continues to oscillate at the same frequency indefinitely. The high input impedance provides a good "hold" characteristic.

Comparator 1 in the PLL, an exclusive-OR gate, should be used for high-noise input sources for optimum performance. Comparator 2 is an edge-detecting device and may be used for most other conditions. The LM555 sampling period is adjustable from 10 milliseconds to 1 second. The supply voltage on all devices may range from 5 to 15 volts. □



Self-gated sample-and-hold. Input-signal burst closes feedback loop in PLL, locks it to incoming frequency. Removal of input opens loop but causes no change in VCO frequency because of RC network, which stores unchanging voltage to drive oscillator.

Full adders simplify design of majority-vote logic

by Zhahai Stewart
Penfield Engineering, Boulder, Colo.

A majority-vote circuit—one with an output state determined by the logic states of the majority of its input variables—can be implemented by 4-bit binary full adders to yield lower chip counts or cost advantages than with standard designs using programmable read-only memories. The adders are easily combined to synthesize circuits used for decision-making or time-and-event-counter applications.

The circuits described use the 7483 full adder, but other adders that provide a similar logic function can be used. Each bit adder in the 7483 (Fig. 1a) has inputs A_i, B_i, and C_i; the outputs are S_i and C_{i+1}. Each adder is cascaded internally by connecting the C_i ports together.

The characteristics of the device are such that there will be a logic 1 output from the sum (S_i) terminal of each adder if one input is high or all three inputs are high. The carry output (C_{i+1}) of each stage will assume the high state if any two inputs or all inputs are high. This is the basic design tool used in the design of any n-bit majority gate.

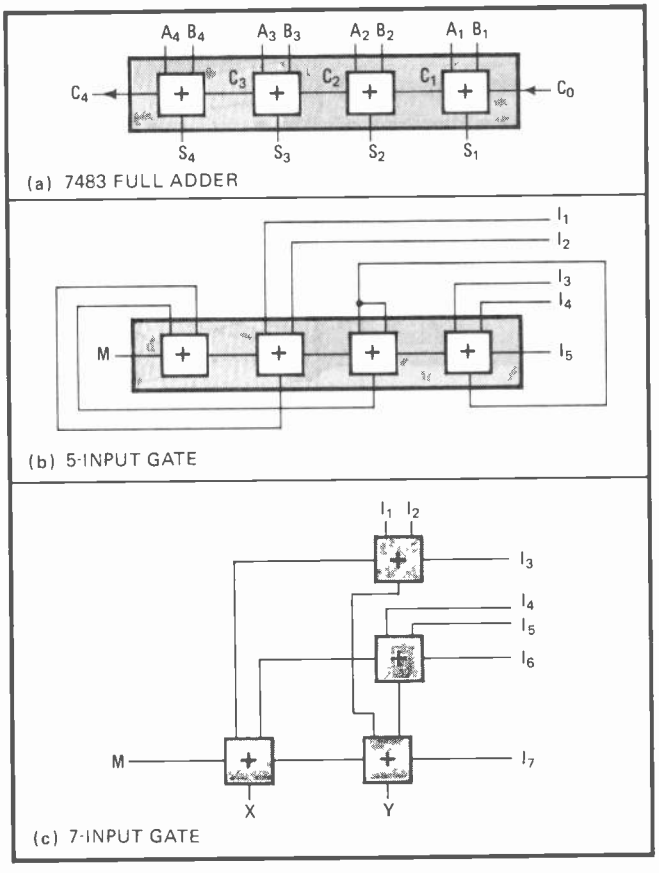
Only one adder is needed to form majority gates with as many as five inputs. For example, a three-input device can be built by introducing the input variables to A_3, A_4, and B_4 of the 7483, while tying all other inputs high to form the "trivial case" solution. In reality, only one quarter of the adder is used to full advantage. The output, taken from the carry-out port of the adder, will be high if any two of the three inputs are high.

Figure 1b shows an implementation of a more important case, the five-input gate. Output M is high if any three of the five inputs are high. The seven-input circuit (Fig. 1c) is a simple extension of the five-input case using the design rules outlined above, but it cannot be built using a single 7483 because its internal-carry connections are not accessible. While the adders cannot be directly cascaded, a majority gate of any size may be easily built as design experience is gained.

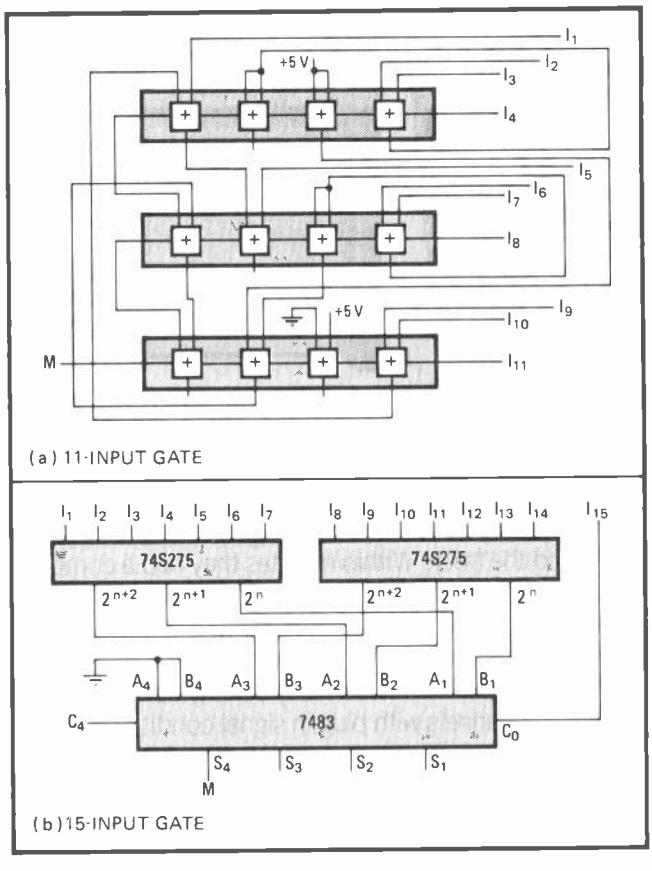
When the number of inputs is small, a PROM can generate the required gate function for slightly greater cost and design effort. However, when the number of input variables is greater than 10 or so, the use of adders will provide clear-cut advantages. An 11-input gate constructed from three adders is easier to design than with a PROM. (Fig. 2a).

When the number of inputs becomes very large, it is

1. Binary-adder majority gate. A single 7483 full adder (a) or similar device can be wired to produce up to a five-input majority-vote circuit. Five-input (b) and seven-input (c) gates are built using adders' truth table as the primary design tool.



2. No need for PROMs. Implementation with adders offer advantages over PROM designs when number of inputs exceed 10 (a). Tree networks can replace adders for additional ease in wiring when the number of input variables is higher (b).



advantageous to search for devices with characteristics similar to the adder and use them to reduce wiring and design headaches—and, in many cases, to minimize chip count. In Fig. 2b, a 15-input gate is implemented using two 74S275 "Wallace trees" and a full adder; the 74S275 provides the function of four adders without the external wiring. When connected to the external adder, space and cost are minimized.

If the carry bits of the Wallace tree are wired low, each tree output will yield the binary sum of the number of input variables that are high. Alternatively, the X, Y, and M outputs of two 7-bit devices (example in Fig. 1) may provide the binary sum to the external adder, where Y is the least significant bit. The output of both trees are then added directly by the 7483, with the result that M will be high if eight or more inputs are high. □

Glitchless TTL arbiter selects first of two inputs

by Yukihiro Mikami
Ottawa, Canada

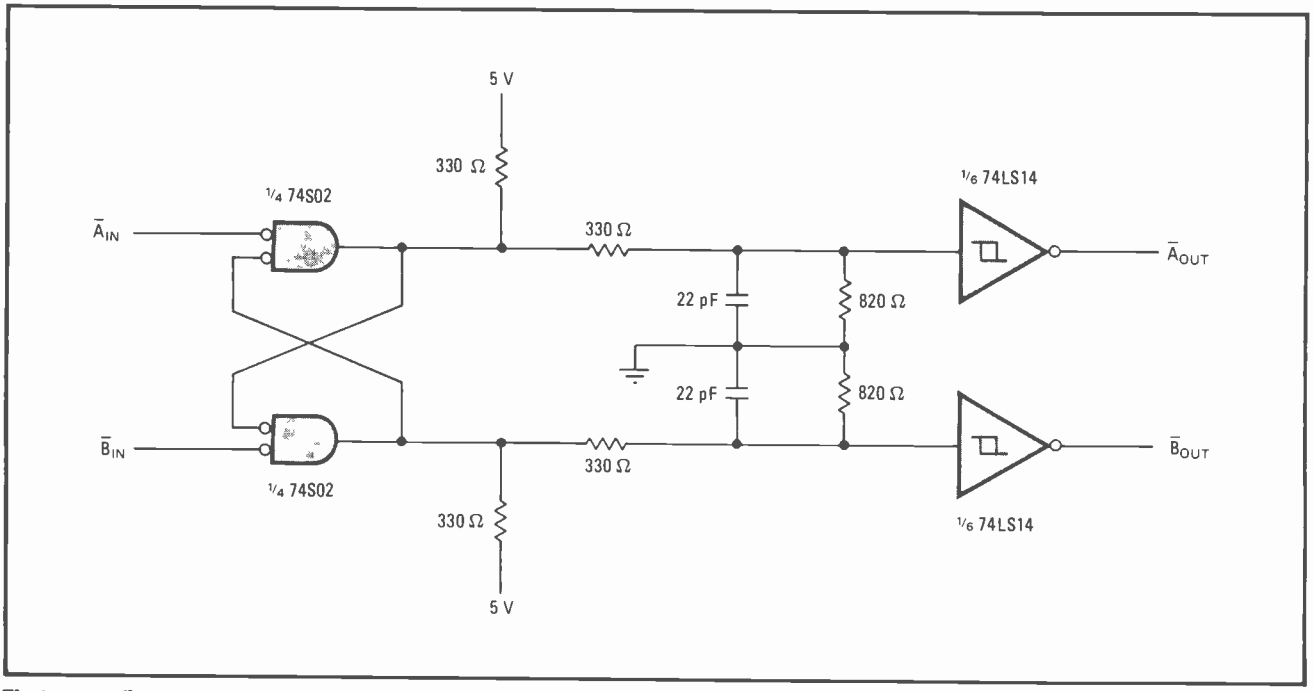
Failure to differentiate between independently timed asynchronous signals only a few nanoseconds apart can cause glitches in standard transistor-transistor-logic circuits that spell disaster to system operation. Once the glitch is detected, it must be eliminated, so that an arbiter circuit like the one described here is essential in applications like dynamic memory controllers.

As shown in the figure, the 74S02 cross-coupled NOR latch will respond to a signal on request line A or B. The signal arriving first will appear on the corresponding output line. With simultaneous inputs, however, a single-pulse glitch, a sinusoidal oscillation, a metastable-state response (0.8-to-2.1-volt unassigned or guard-band region), or a combination of such responses may occur at each output for an indefinite period before the gate decides to switch into its desired state.

An RC network and Schmitt-trigger buffer eliminate these undesirable responses from the circuit outputs while minimizing the decision time. The amplitude of the glitch or oscillation is essentially filtered or damped, as the case may be, by the RC combination of the 330-ohm resistors and the 22-picofarad capacitor.

The resistors also combine with the 820-Ω resistor at the input of either Schmitt trigger to form a voltage divider. This divider effectively raises the positive-going switching threshold at this point by 0.6 to 2.1 v. Thus there is no spurious response, even for a 3-v glitch, a 1.5-v peak-to-peak oscillation, or a metastable-state response at the NOR gate output. The circuit responds with an output when the transient dies away, as the latch may then decide which signal came first. In the event of the arrival of two truly simultaneous signals, the gate would render an arbitrary decision.

Nonsimultaneous signals appearing at the appropriate output of the NOR gate will pass through the deglitching circuit relatively unaffected. Typical propagation delay of the arbiter is 20 nanoseconds for nonsimultaneous inputs and 25 ns for simultaneous input signals. □



First come, first served. The input signal arriving first passes to an output, while simultaneously arriving signals produce an eventual output but no glitch. The resistor network raises the threshold of the Schmitt trigger, and the RC combination reduces glitch amplitude.

Single C-MOS IC forms pulse-width modulator

by Mark E. Anglin
Novar Electronics, Barberton, Ohio

A pulse-width modulator can be constructed with a single complementary-metal-oxide-semiconductor integrated circuit if the IC's field-effect transistors control the duty cycle of a free-running oscillator. The output resistance of the FET varies almost linearly with input voltage over portions of its characteristic curve, permitting the circuit to be used for applications in switching power supplies and analog conversion in data-communications systems.

This circuit uses a CD4007 dual complementary pair plus an inverter device, which comprises three n-channel and three p-channel enhancement-type MOS transistors. As shown in the figure, inverters I_1 and I_2, each formed by two gates in the 4007, themselves form an astable multivibrator in conjunction with resistor R and capacitor C. The frequency of oscillation of the multivibrator is given by:

$$f = 1/1.4\,RC$$

The 1-megohm resistor, left in the figure, limits the feedback current into I_1. This prevents the input circuit from burnout and the inverter from switching prematurely and affecting the desired frequency of operation.

The two remaining gates in the 4007, one n-channel and one p-channel gate, are connected across the output of I_1 and R. This network is designed to modify R and thus control switching times t_1 and t_2.

The oscillation (switching) times for this device may be expressed by two equations:

$$t_1 = RC \ln [(V_{dd} - V_{tr})V_{dd}]$$

and

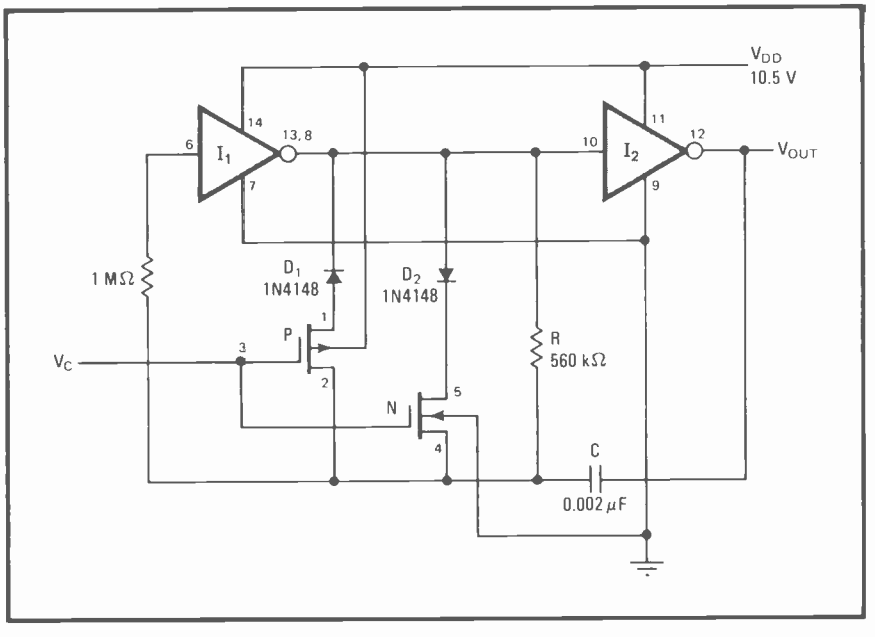
$$t_2 = RC \ln (V_{tr}/V_{dd})$$

where t_1 is the on time and t_2 is the off time of the oscillator, V_{tr} is the threshold voltage at the gate's input, and V_{dd} is the supply voltage.

When the oscillator's output is high, diode D_1 may conduct. The p-channel output resistance will be in parallel with R, neglecting the diode's forward resistance. The p-channel gate's output resistance will decrease as V_c decreases.

Similarly, when the oscillator's output is low, D_2 may conduct, and the n-channel output is placed in parallel with R. The n-channel's resistance will decrease as V_c increases. The duty cycle of the oscillations (in other words, control of the on and off times) is variable from 1% to 99% of the operating frequency. The duty cycle is directly proportional to the amplitude of the control voltage V_c, over a moderate range.

The component values in the figure yield an oscillation frequency of 1 kilohertz. The change in oscillation frequency as a function of duty cycle is minimal; although the basic frequency of oscillation is modified by the FETs across I_1, the output impedance of one always increases, and the other's decreases proportionately, for any value of control voltage V_c. Thus, the average resistance shunted across R during a cycle is constant. □



Single IC modulator. Pulse-width modulation is achieved by varying duty cycle of free-running oscillator in accordance with input voltage V_c. Output impedance of FETs shunts switching-time element R, permitting adjustable duty cycle.

Comparators replace mechanical set-point meter

by Louis A. Perretta
HNU Systems Inc., Newton, Mass.

A standard ammeter and a simple comparator circuit can replace the expensive and bulky mechanical dual-set-point meters used for most process control applications. This electronic circuit provides higher efficiency at low cost and can be built on a printed-circuit card. With a slight modification to the basic circuit, a double high set point and a double low set point may be established—a feature that is not available from the mechanical meter.

The mechanical meter used for industrial purposes contains internal relays and a 115-volt power supply to drive them, as well as a meter that triggers when its pointer or indicating device comes into contact with the high or low set points on the meter dial.

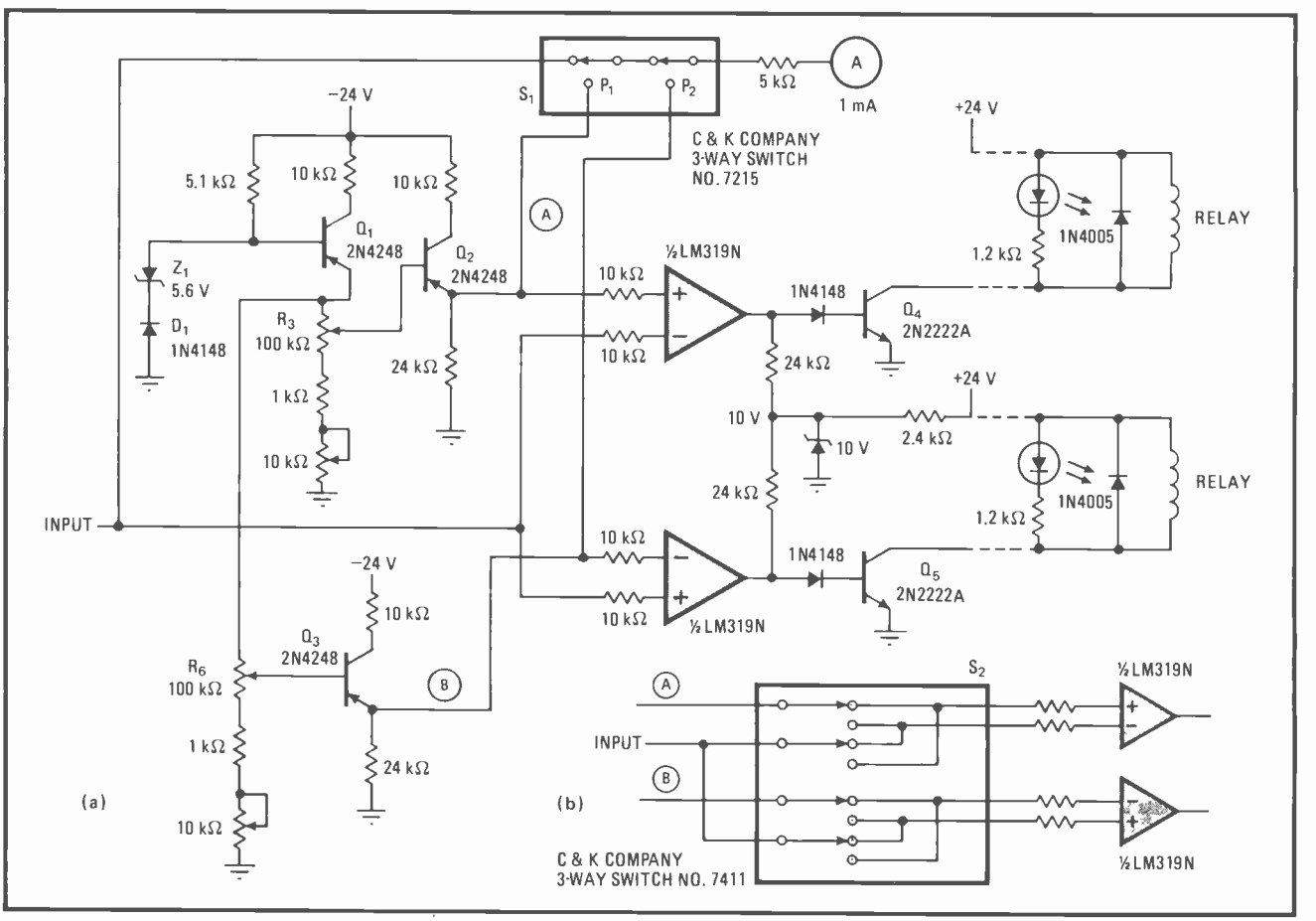
In the electronic circuit shown in the figure, the mechanical set control is replaced by two potentiometers, transistors Q_1 through Q_5, and the LM319 operational amplifier. A 1-milliampere meter indicates conditions at the output of the monitored circuit. The meter is no longer part of the relay triggering circuit, and the relays no longer need a power supply. If the circuit is to control heavy loads, relays must be employed, but they draw only little power from output transistors Q_4 and Q_5 and can be placed far from the metering circuit.

In normal operation, an input signal is applied to each of the two op amps in the LM319, which compares it to a previously set (high- and low-point) reference. In the circuit, the reference voltages are adjustable from 0 to -5.6 v. This is made possible by the biasing arrangement at Q_1, in which diodes Z_1 and D_1 are configured to supply a constant -5.6 v at its emitter. The voltage across potentiometers R_3 and R_6 thus may vary between two references, one at -5.6 v and the other at -0.6 v, so that the input to the comparator can vary between -5 v and ground.

When the input voltage, as set by the meter, exceeds the high or low reference, the appropriate output of the LM319 fires and switches either transistor Q_4 or Q_5, which closes the proper relay.

The high and low reference points may be set by using the meter. Switching switch S_1 to P_1 removes the metering circuit from the input signal, and the meter then displays the high-point reference voltage, which can be adjusted by R_3. With S_1 moved to position P_2, the desired low-level voltage may be adjusted with potentiometer R_6.

The voltage drop across zener diode Z_1 and the



Mechanical to electrical conversion. Implementation of dual-set-point meter using standard meter and comparator circuits (a) is low-cost and reliable. When a three-way switch is added to circuit (b), double high and low set points can be set.

number of standard diodes (D_1) determines the range of reference voltages possible. Reversing diode polarities and changing Q_1, Q_2, and Q_3 to npn devices produces positive reference voltages.

To establish double high set and low set points, a four-pole, three-way toggle switch is placed in the path of transistors Q_2 and Q_3 and the input of the op amp, as the lower part of the figure shows. □

High-impedance op amp extends 555 timer's range

by Ronald Zane
University of California, Los Angeles, Calif.

The period of oscillation of the 555 timer can be increased 20 times or more if the timing components are replaced by a feedback loop containing a transistor and a very-high-impedance input operational amplifier configured as an integrator. The circuit is an inexpensive way of generating timing periods of hours or days to control industrial processes, to turn on lights in the home for burglar protection, and for like applications.

As shown in the figure, resistor R_5 and capacitor C combine with the CA3140T op amp to make the integrator that controls the period of oscillation in the 555. The very low offset current of this op amp (typically 3 picoamperes but no greater than 30 pA) permits accurate integration of very low input currents (100 pA). Thus it ensures excellent control over the actual oscillation times.

The timer, operating in its astable-multivibrator mode, produces a change of state at pins 3 and 7 each time the input signal requirements are met at the threshold and trigger ports of the device. The output moves low when the input at the threshold terminal is greater than two thirds the supply voltage V_s. It stays low until the trigger input detects decay of the input signal's voltage to less than one third of V_s. Then the output assumes a high state.

Transistor Q_1 switches in accordance with pin 7 of the 555; point E_1 will be at ground when Q_1 is on, and at $V_s/2$ when Q_1 is off, because of the voltage divider made up of R_1 and R_2. The voltage at E_2, $V_s/4$, is determined by the divider made up of R_6 and R_7 (R_1, R_3, and R_4 in series hardly affect the calculation).

When Q_1 is on, the current through R_5 at the inverting input of the op amp is thus:

$$I = \frac{(V_s/2 - V_s/4)\,R_4}{R_5(R_3+R_4)} = \frac{V_s\,R_4}{4R_5\,(R_3+R_4)}$$

and when it is off, the current is:

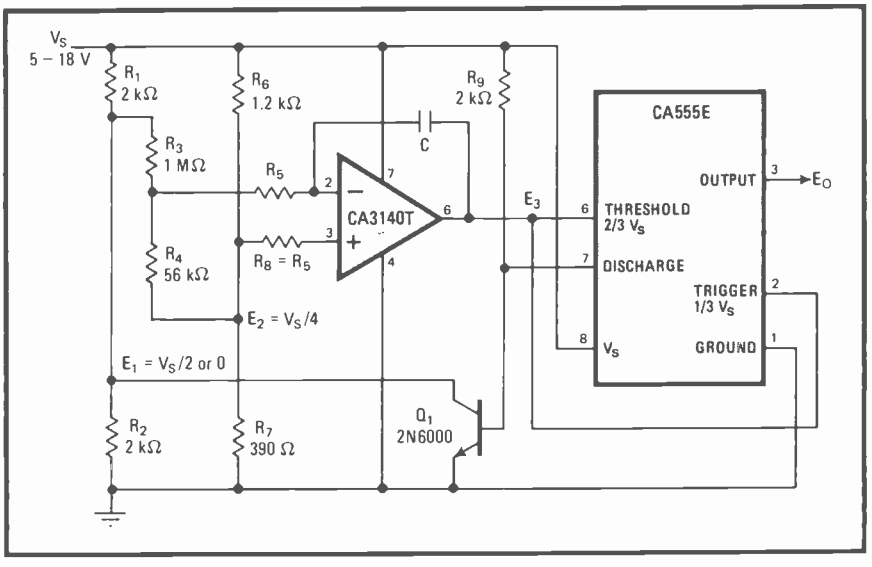
$$I = \frac{(0 - V_s/4)\,R_4}{R_5\,(R_3+R_4)} = \frac{-V_s\,R_4}{4\,R_5\,(R_3+R_4)}$$

The magnitudes of these currents are the same. The integrator then operates on this input current. Because its output is $E_3 = dV_s/dt = I/C$ by definition, and because E_3 switches between one third and two thirds of the supply voltage each cycle, the oscillator's period is:

$$t = \int_{1/3}^{2/3} \frac{C}{I}\,dV_s \frac{8(R_3+R_4)\,R_5C}{3R_4} = 50\,R_5C$$

The low offset current of the op amp allows R_5 to assume values in the hundreds of megohms. Even when R_5 equals 110 MΩ, the current through it is 1.8 nanoamperes, far exceeding the op amp's offset current.

If R_5 is 110 MΩ and C is 1 microfarad, the 555's period is 5,500 seconds. Since R_5 and C can be increased, periods of 10 hours or more may be realized with inexpensive components. If a 510-MΩ resistor and a 10-μF capacitor is used in the integrator, the oscillation period will be 70 hours. The bare 555, which may use a maximum timing resistance of 20 MΩ, coupled with a 10-μF capacitor for its timing capacitance, would have an oscillation time of only 280 seconds. □



Time-magnification. Oscillation frequency of a 555 may be lowered 20 times or more if a low-input-current, integrating op amp is used to replace timing components. One oscillation every few days is possible if a high-value capacitor, C, is used in integrator.

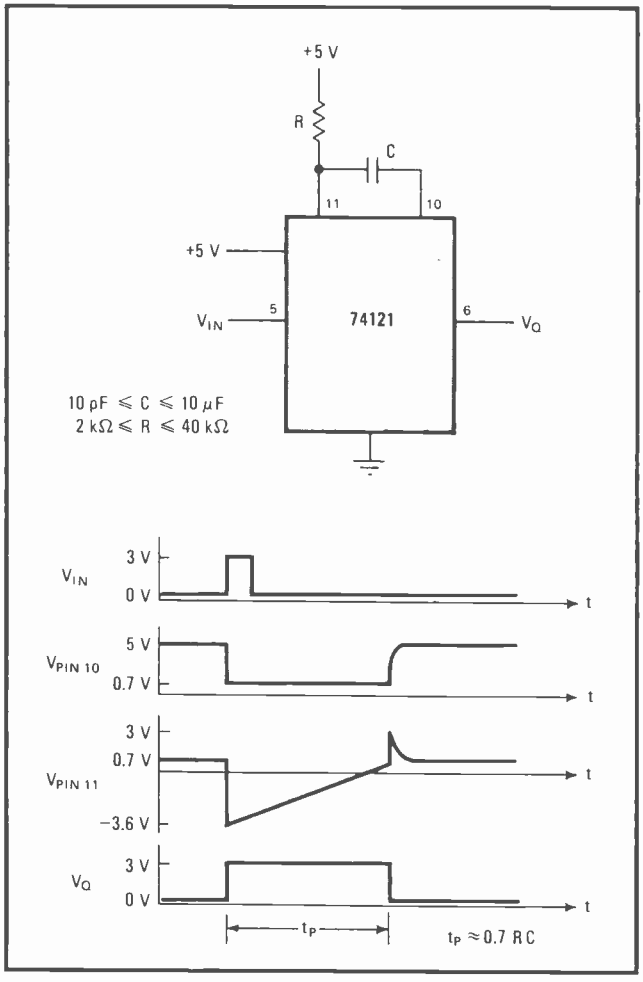
One-shot multivibrator has programmable pulse width

by Stephen C. Armfield
MCI Inc., Fort Lauderdale, Fla.

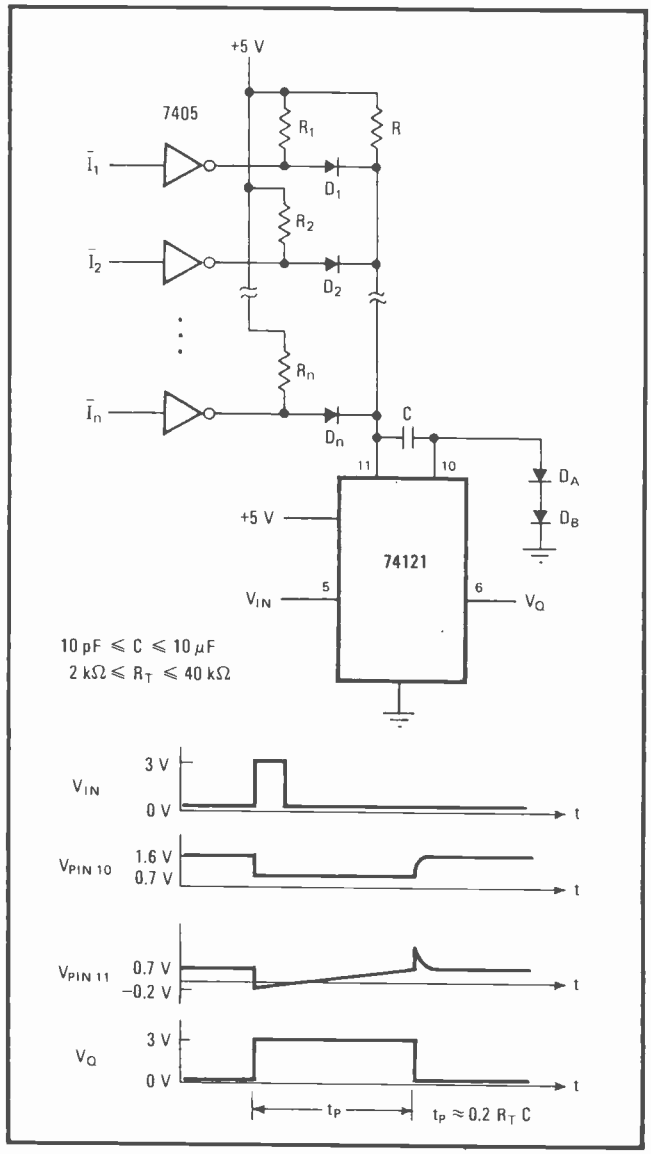
The pulse width of a monostable multivibrator can be varied by digital control of its timing network. Using diode-modified gate circuits solves the interface problems inherent in driving the RC port with unipolar devices, while permitting the selection of resistors that shunt the timing capacitor to control its charging time.

As shown in the timing diagram in Fig. 1, a negative voltage is generated at pin 11 of a standard 74121 transistor-transistor-logic multivibrator although positive supply voltages are applied to the device. As a consequence of a triggering signal, the voltage at pin 10, which started at 5 volts, drops to 0.7 v. The voltage at pin 11 also drops by the same amount; since its initial voltage was only 0.7 v, however, its final voltage is −3.6 v. Thus, the timing (RC) network cannot be directly driven by standard TTL configurations.

With the use of diodes D_a and D_b, pin 10 can be clamped to about 1.6 volts without disturbing circuit operation, and the negative excursions at pin 11 will be restricted to a few tenths of a volt, as shown in Fig. 2. The 7405 open-collector gates can then be used in conjunction with isolating diodes D_1 through D_n to alter the charging rate of C. The alteration is accomplished by



1. Standard configuration. TTL circuits alone cannot control the duty cycle of a one-shot directly because negative voltage is generated at timing port during normal operation. Reduction of this voltage to low level permits adjustment of pulse width.



2. Pulse width variation. The use of diodes D_a and D_b clamps pin 10 of one-shot, permits TTL to drive and control the duty cycle. Actuating isolation diodes D_1 to D_n alters the charging rate of C, providing a choice of duty-cycle times.

activating the desired digital inputs I_1 through I_n, which permit conduction through the isolating diodes, and consequently, shunting of resistance by resistors R_1 through R_n. The equivalent resistance is:

$$\frac{1}{R_T}=\frac{1}{R_1}+I_1\left(\frac{1}{R_1}\right)+I_2\left(\frac{1}{R_2}\right)+\ldots I_n\left(\frac{1}{R_n}\right)$$

where I_1 through I_n is equal to 1 or 0, corresponding to logic 1 or logic 0.

The current required by the clamping diodes D_a and D_b is 20 milliamperes or so and is supplied by a transistor internal to the multivibrator. If the increased power consumption can be tolerated, this programmable one-shot can be useful in many digital applications. □

Resistor-controlled LC network drives tunable discriminator

by John W. Newman
U. S. Army Electronics Materiel Readiness Activity, Warrenton, Va.

A single potentiometer can adjust the fixed-tuned circuits that determine the mark-and-space frequencies in an audio-frequency-shift-keyed discriminator. This can be accomplished if the potentiometer controls the feedback current that passes through the inductor of each LC combination. Such calibrated single-control tuning is an advantage when reception of any one pair of several widely used shifts is necessary, because the mark-and-space filters do not have to be individually and repeatedly set by a frequency counter or by some other instrument.

A LaPlace analysis of a current-driven tuned circuit will show the dependence of the resonant frequency on the amount of feedback. The tuned circuit in Fig. 1 has a transfer function that is:

$$A(s)=\frac{s+R_L}{s^2+R_Ls+1}$$

Feedback provided by the second amplifier is:

$$B(s)=\frac{K}{s^2+R_Ls+1}$$

where K is the amplifier gain, a function of the potentiometer setting, and may be positive or negative in value. The complete transfer function becomes:

$$H(s)=\frac{s+R_L}{s^2+R_Ls+1-K}$$

The denominator of this equation, which is of major importance in this analysis, is of the form:

$$s^2+(AQ)s+\omega^2$$

where A is a constant, Q is the circuit's selectivity or quality factor, and ω is the radian frequency of the circuit. Thus it is observed that $\omega=(1-K)^{1/2}$. This assumes that bandwidth and gain of the circuit are independent variables.

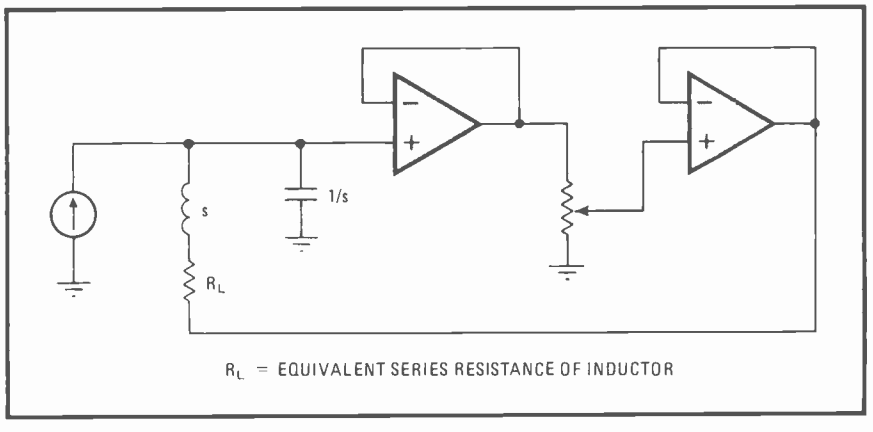
Analysis of the feedback loop containing a tuned circuit that is driven from a voltage source is somewhat more complicated, but the results are similar. For the actual voltage-driver circuit in Fig. 2, the transfer function is approximately:

$$H(s)=\frac{(s+R_L)}{R_4[s^2+s(R_L+{}^1/R_4+{}^1/R_5)+1\pm K]}$$

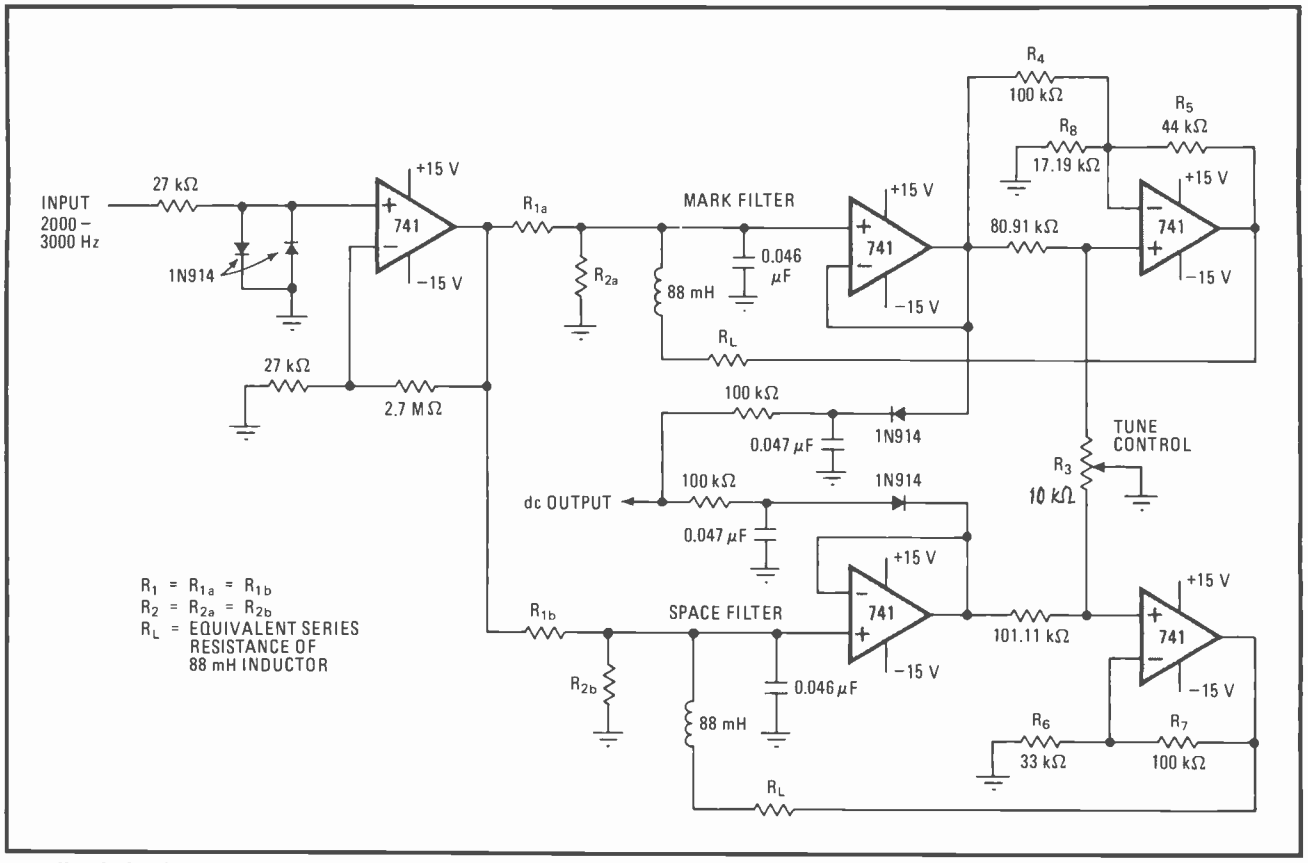
where the radian frequency term is the same, but the value of Q depends largely on resistors R_1 and R_2, and the value of K is dependent on R_3.

Determination of R_1, R_2, and R_3 is most important for circuit optimization of Q and transient response. After limiting of the 2-to-3-kilohertz input signal by the first operational amplifier, the 14-volt output signal must be reduced by one half by the voltage divider consisting of R_1 and R_2. This will prevent overdrive of subsequent stages containing two identical tuned circuits with equivalent impedance Z_x. In addition, the dc output of the circuit is a function of the relationship of the mark-and-space frequency to the frequency of each tuned circuit (and thus Z_x, R_1, and R_2).

An unloaded (no-feedback) Q of about 100 is to be expected at 2,500 Hz from each resonant circuit, providing a Z_x of 138,200 ohms. It is reasonable to set a loaded Q of 25, providing a bandwidth of 100 Hz. Resistor R_2 is selected for a Q of 50 so that the parallel equivalent of Z_x, R_1, and R_2 reduces the Q to 25 and



1. Current analysis. Resonant frequency of tuned circuit is affected not only by L and C values but also by magnitude of feedback current through inductor. Potentiometer may control gain of amplifier and thus resonant frequency. Circuit is simpler to analyze but yields results similar to voltage-driven discriminator network described in text.



2. A discriminating network. Resistor-tuned filters provide one-control adjustment of mark-and-space frequencies. Shifts are continuously adjustable from zero to 1 kilohertz at a center frequency of 2,500 hertz and are linearly proportional to potentiometer setting.

RESISTOR-TUNED DISCRIMINATOR		
POT ROTATION	FREQUENCY (Hz)	
(%)	MARK	SPACE
0	2,500	2,500
10	2,549	2,451
20	2,598	2,401
30	2,647	2,352
40	2,697	2,302
50	2,747	2,252
60	2,797	2,202
70	2,847	2,152
80	2,897	2,102
90	2,949	2,051
100	3,000	2,000

yields the desired voltage division. Thus, R_2 is equal to 138,200 Ω, and R_1 is equal to the parallel combination of Z_x and R_2, or 69,100 Ω.

The resonant frequency of the mark-and-space filters is directly determined by R_3. With the potentiometer's resistance at a minimum as measured from the junction of the 101-kilohm resistor and the noninverting input of the 741 op amp, the noninverting gain for the mark filter is 0.44, which nullifies the inverting gain of 0.44 from the following amplifier stage. Thus the mark resonant frequency remains at 2,500 Hz. Feedback through the space resonant circuit is zero, and it is also resonant at 2,500 Hz. When R_3 increases, the inverting gain for the mark filter becomes greater than the noninverting gain and the mark resonant frequency increases. The feedback signal through the space resonant circuit decreases the space resonant frequency. The maximum input signal available across R_3 is 0.09 times the output signal; at this setting the op amp gain is 4. The lowest resonant frequency is thus $(1 - 0.36)^{1/2}$ (2,500) = 2,000 Hz. Conversely, the mark filter has a maximum frequency of $(1 + 0.44)^{1/2}$ (2,500) = 3,000 Hz.

The table shows the relationship of the potentiometer setting to the mark-and-set frequency pairs. The resonant frequency of the mark filters should be trimmed to a center frequency of 2,500 Hz by R_8. The space filter's lower limit should be trimmed by R_6 or R_7; the mark filter's upper limit should be set by R_4 or R_5.

The dc output is derived from intermediate op amps in conjunction with half-wave rectifier networks. The output voltage will always be positive for received mark frequencies and negative for space frequencies, permitting a suitable source for transistors that will drive radio teleprinter relays and similar equipment. Rejection of off-frequency mark-or-space signals is excellent. Mark-and-space frequency pairs can be within 100 Hz of each other while still providing good circuit performance. □

Nonmaskable interrupt saves processor register contents

by Ivars P. Breikss
Honeywell Inc., Test Instruments Division, Denver, Colo.

Linking a battery-powered random-access memory to the nonmaskable interrupt input available on many microprocessors will save the contents of the memory registers in a microprocessor system during power loss. The NMI input is used to initiate a software routine that, when alerted to a power loss by such means as a power-line relay, stores the contents of the registers in the RAM and then disables the RAM's inputs. These registers require such protection of their status if the microprocessor is to continue execution of the program at the point at which it left off when power failure occurred.

The data-save circuit may be implemented as shown in the figure, using two 5101 complementary-metal-oxide-semiconductor RAMs in conjunction with the 6800/6820 combination of microprocessor and peripheral interface adapter. Since each RAM is organized as a 256-word-by-4-bit array, this 8-bit system requires two of them, configured as a 256-word-by-8-bit device. A set-reset flip-flop, built by cross-connecting two C-MOS two-input NAND gates, controls the data-enable port of the RAMs. The flip-flop and the RAMs are powered by a 4.5-volt battery if the main power is lost.

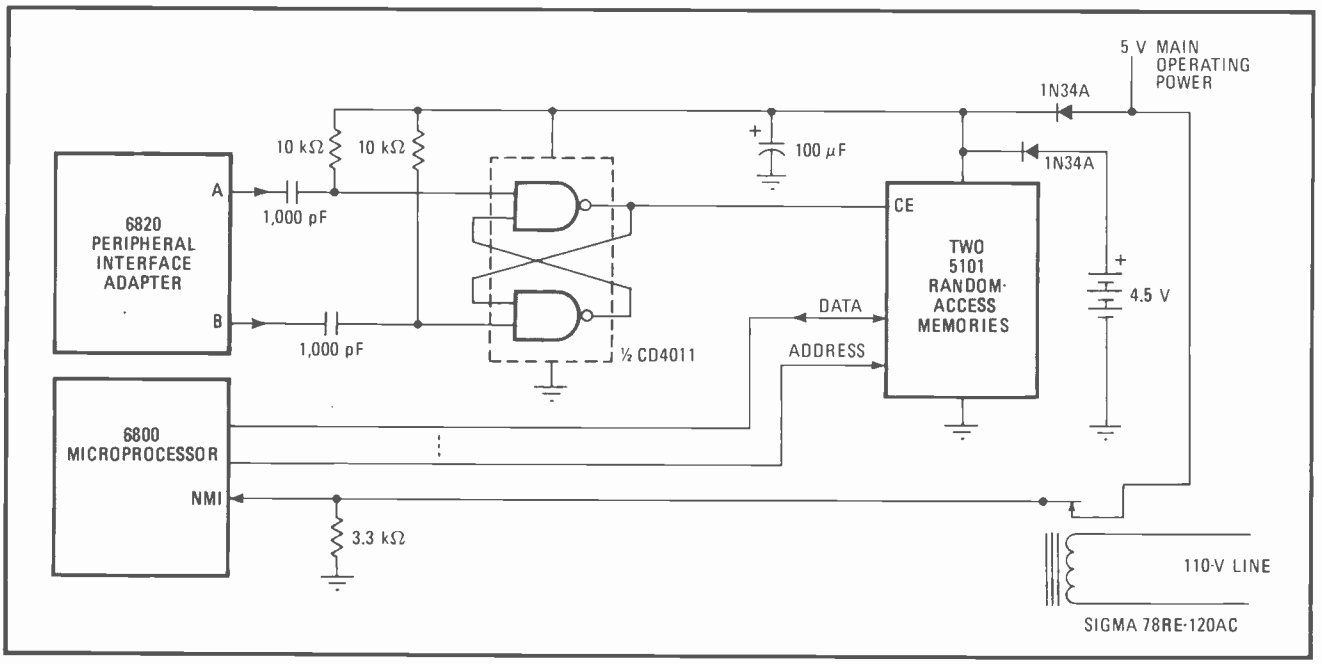
During system startup, a pulsed logic 1 signal is generated at the A output of the PIA through software control. The negative-going edge of this pulse sets the flip-flop and drives the control-enable lead (CE) of the RAMs. This allows desired system parameters, which may have taken hours to determine initially, to be stored in the RAM for protection from power failure.

During a power-down cycle, the address and data lines of the RAM will usually assume random logic states for several milliseconds. This condition is likely to destroy or modify the contents of the RAM unless a logic 0 is applied to the CE input at least a few microseconds before the main power is lost.

A loss of line voltage causes the relay to open; once the operating voltage drops below 4.5 V the battery immediately assumes the power-delivery chores to the RAM and flip-flop. Loss of voltage to the microprocessor and PIA occurs approximately 25 ms later; a pulse must be delivered to the CE port of the RAM before that time.

Relay dropout initiates the NMI sequence. The NMI input, which was at 5 V, drops rapidly. The negative-going transition terminates normal program execution and initiates the interrupt sequence. During this time, an output pulse is generated at port B or the PIA. Its negative edge clears the flip-flop, disabling the RAM by removing its CE signal. This occurs before operating power collapses; thus the RAM's content is not upset. Capacitive coupling between the PIA and the flip-flop is employed to prevent false triggering which may occur during power loss.

This circuit is exceptionally reliable and consumes little power. A small 4.5-V battery will store 256 8-bit words for more than a year if necessary. □



To the rescue. Should power to microprocessor or PIA fail, data in their registers is stored in battery-powered RAMs for protection. Control-enable line of RAMs is enabled during normal operation, disabled on power-down to prevent modification of RAM contents.

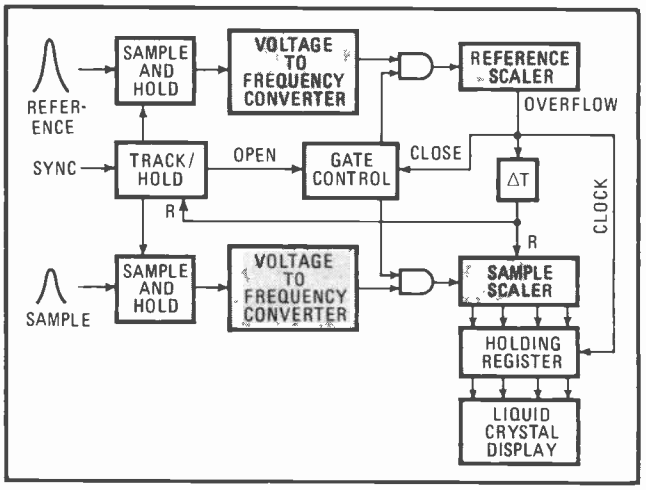
Digital normalizer derives ratio of two analog signals

by James H. McQuaid
University of California, Lawrence Livermore Laboratory, Livermore, Calif.

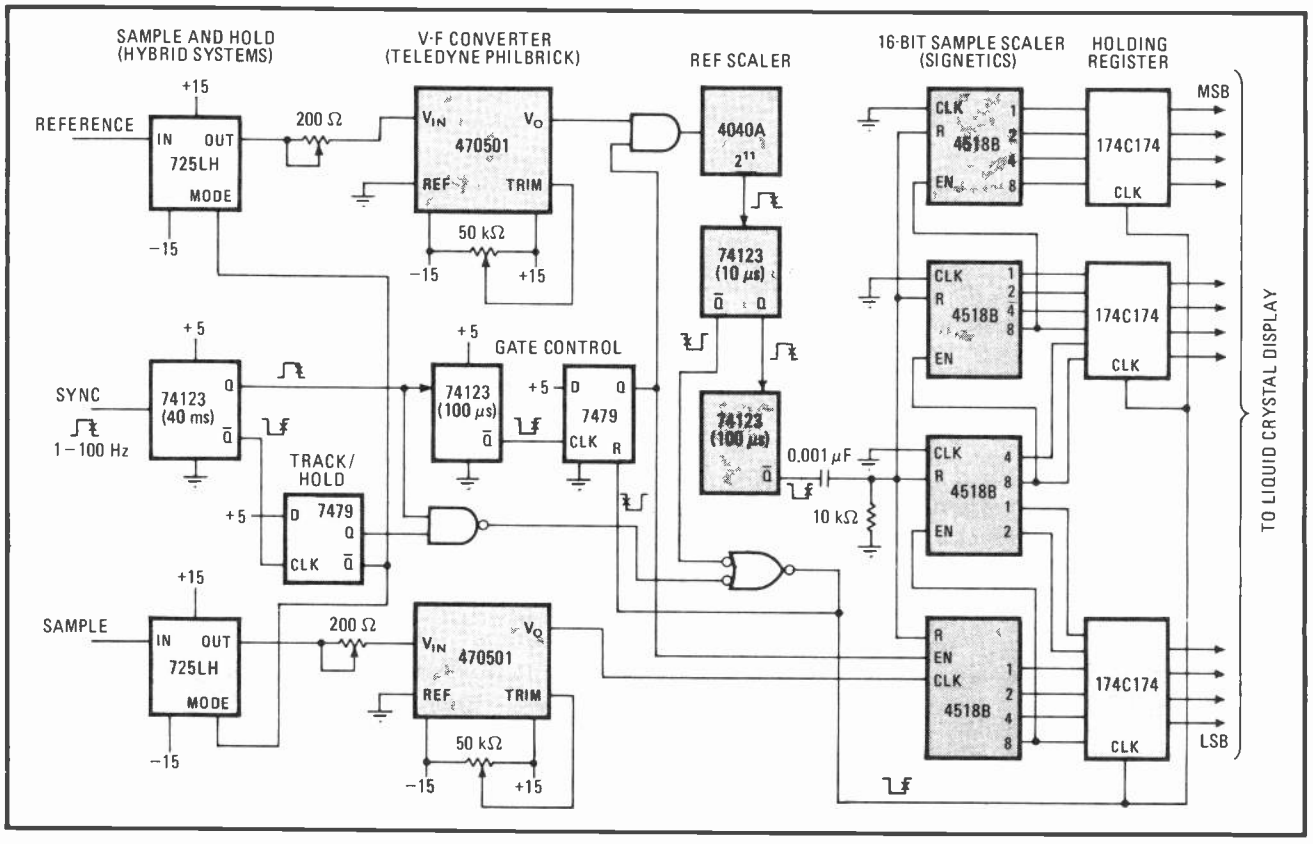
The absolute value of a voltage or current at a circuit point is frequently less important than the ratio of that quantity to a reference. This circuit compares two analog signals by using a high-accuracy digital technique for normalizing the reference voltage, thus simplifying circuitry and avoiding the use of analog dividers or microprocessors. It is invaluable in many light-chopping applications, such as lasers, where the measurement of light intensity at a specific frequency must take into account total source-intensity variations. It is also useful in atmospheric physics when measuring the concentration of a specific gas in a mixture by infrared techniques in which the intensity of the beam is subject to drift.

As shown in the block diagram (Fig. 1), the reference and sample signals are each introduced to a sample-and-hold circuit. Peak-detection circuitry in this device, in conjunction with track-and-hold logic, which controls the sample rate, produces a voltage output that is presented to their respective voltage-to-frequency converters. Each converter's output is a pulse train with a frequency directly proportional to the input voltage.

The track-and-hold logic and associated gating circuits simultaneously initialize both scalar circuits and allow the output pulse train of both converters to be counted. When the count in the reference scaler exceeds its capacity, an overflow pulse is generated that closes the gating circuit; at this time, the contents of the sample scaler are clocked into the holding register and then sent to the display. The contents of the reference scaler are regarded as a unit voltage, and the reference scaler



1. Ratio meter. Voltage comparison of analog sample to time-dependent reference uses analog-to-digital converters. Voltages are converted to frequency and counted. Reference count normalized to unity serves as gating signal to count number in sample counter. Output of circuit yields ratio of sample to reference voltage.



2. Digital normalization. Circuit detects relationship of analog sample amplitude to reference voltage by digital means. Several one-shots are used to obtain proper timing and gating. Circuit uses C-MOS devices where possible to reduce power consumption.

controls the gating time to the sample scaler. Thus the contents of the holding register will normally be some fraction of the unity-set voltage. The sample scaler and sampling circuits are then reset, ready to process the next sample.

As shown in Fig. 2, the sample-and-hold devices are Hybrid Systems 725LH devices, which are accurate to within 0.01% and have a droop rate of 15 millivolts per second using their internal holding capacitor. The sync input used to control the sampling period is a 5-volt, 1-to-100-hertz pulsed voltage. The converters are Teledyne Philbrick 470501 devices with an upper limiting frequency of about 1 megahertz. This frequency is produced at an input of 10 v, and the device's voltage-frequency characteristic is linear to 0.005%. The converter may be easily calibrated with its 50-kilohm trimmer potentiometer and the 200-ohm rheostat at the output of the 725LH device.

The 4040 reference scaler is a 12-bit binary counter. After reaching its counting capacity (4,096) during a given sampling period, it clocks the contents of the Signetics 4518B into the 174C174 C-MOS holding register while resetting the gating circuits. The sample scaler capacity (16 bits) and the large reference scaler capacity (12 bits) ensure a high counting accuracy, typically to within 0.1%. In addition, the larger capacity of the sample scaler allows the signal amplitude to exceed the reference amplitude while the correct ratio is still displayed.

The ΔT function in the block diagram is a small but important part of the circuit. It is implemented as shown in Fig. 2 with a number of one shots to achieve correct timing and edge triggering for data transfer. The digitizing time for the circuit shown is 4 milliseconds. Greater speed (with less accuracy) can be easily achieved by reducing the number of bits in the reference scaler. For instance, a digitizing time of 250 microseconds may be achieved with an 8-bit reference scaler. □

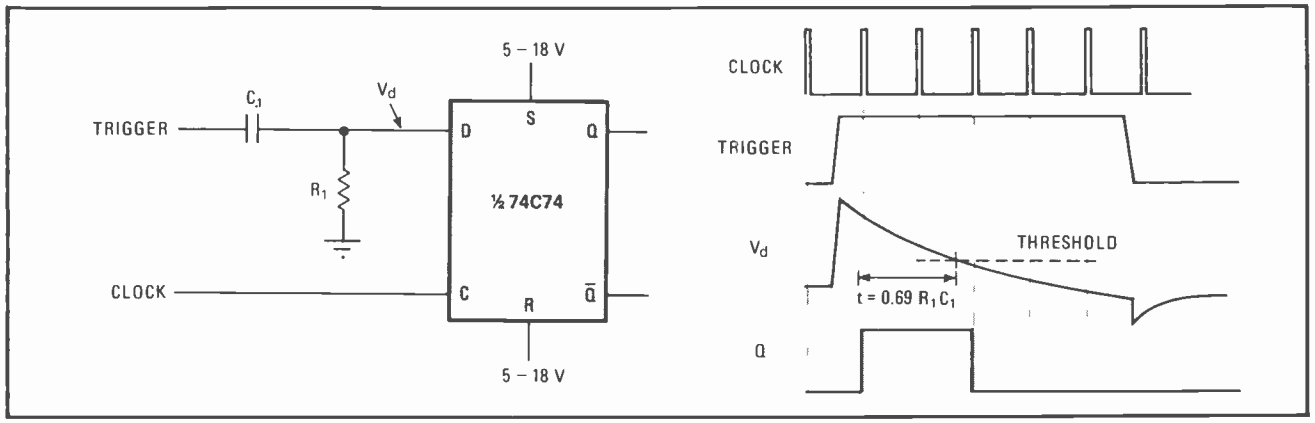
Differentiator and latch form synchronous one-shot

by Chacko C. Neroth
Amdahl Corp., Sunnyvale, Calif.

Many logic circuits require all operations to be synchronized with the system clock, including the firing of monostable multivibrators, even though the input signals to the one-shot are time-independent. However, a synchronous one-shot may be implemented using a D flip-flop and a differentiator network. In essence, the circuit substitutes a differentiator at the D input for a timing network in the one-shot in order to provide either immediate or time-delayed synchronous operation upon the arrival of a suitable trigger.

As shown in the figure, a positive-going input signal is applied to the D input of the 74C74 complementary-metal-oxide-semiconductor device through the resistance-capacitance network R_1C_1. The state of the flip-flop, which depends on the logic level at the D input during a clock pulse at the C input, assumes a 1 value at the arrival of the first clock. The output remains high until the voltage across the resistor has decayed below the 1 threshold of the D input (because of capacitor discharge), and the next clock occurs at the C input. Thus, assuming the clock period is high compared with the R_1C_1 period, the approximate pulse width, or on time, of the flip-flop is equal to $0.69\ R_1C_1$; the exact width of the pulse is an integral number of clock periods during which the D input is high.

The logic threshold of the C-MOS device at the D input is almost proportional to the supply voltage; therefore the pulse width output is relatively insensitive to supply voltage variations. For best results, the resistance-capacitance network should be selected to ensure that a decay in voltage across the resistor reaches the threshold level at the D input halfway between clock periods. Operation with negative-edge triggers is possible if R_1 is connected to the positive supply line instead of ground. □



Monostable controller. Synchronous multivibrator is formed by differentiator and flip-flop, permitting initialization of clocked system by asynchronous data. Pulse width of multivibrator is determined by time constant of differentiator and clock rate.

Fast-attack detector optimizes ultrasonic receiver response

by Paul M. Gammell
Jet Propulsion Laboratory, Pasadena, Calif.

A radio-frequency amplifier with low output impedance greatly enhances the performance of an ultrasonic receiver. The low impedance, achieved by an open-collector output configuration, permits design of a detector having a fast rise time and somewhat slower fall time—characteristics important for high-accuracy distance-measuring applications. This inexpensive circuit is a wideband receiver with good overload-signal recovery. It has many pulse-echo uses, including nondestructive evaluation and depth finding, and performs well in biomedical ultrasonic applications.

As shown in the figure, a pulsed signal is simultaneously applied to a transducer and transistor amplifier Q_1. The transducer is one of many commercially available devices that will convert a typical 200-volt, 0.1-to-1-microsecond pulse into an ultrasonic (compressional) wave aimed at a distant target. The echo from the transducer, with an amplitude on the order of 1 to 10 microvolts, may return only microseconds later. Q_1 must therefore recover quickly from the large initial pulse in order to respond to the echo signal.

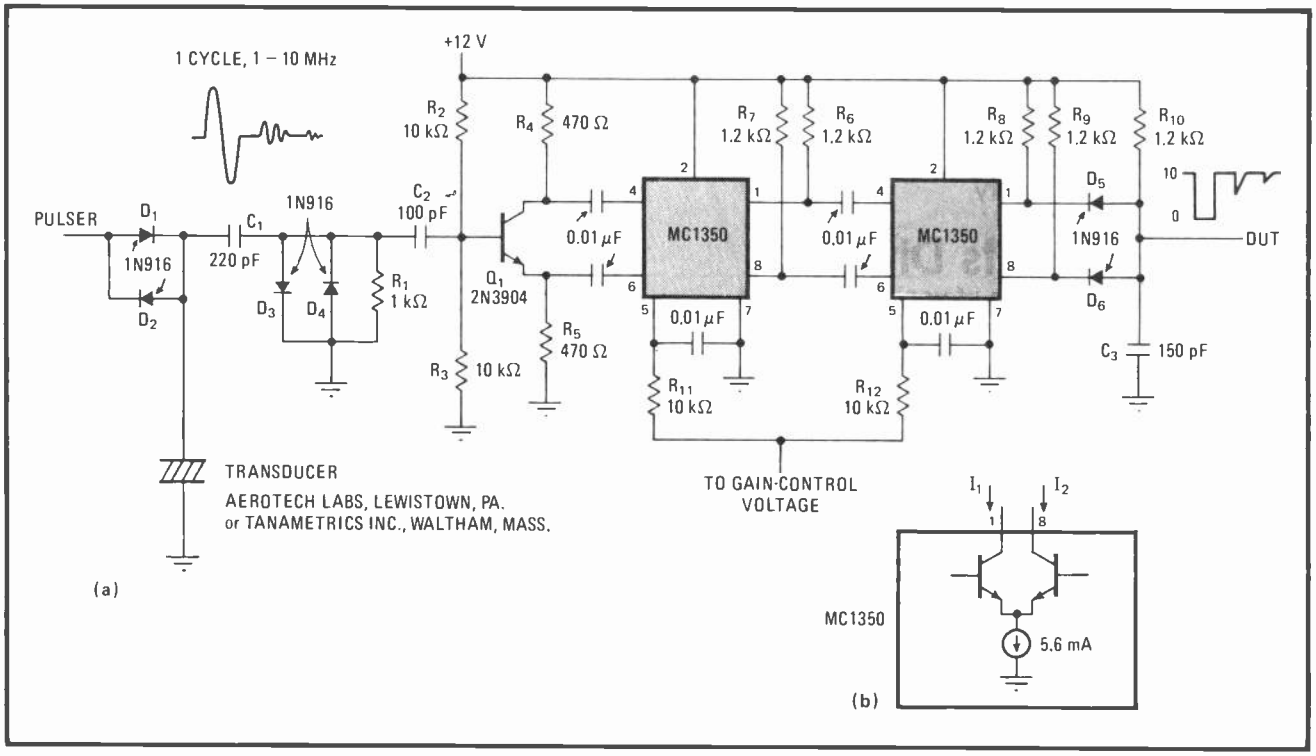
Components C_1, C_2, and D_1 through D_4 aid in isolating the amplifier circuits from the high-voltage pulse. Resistor R_1 improves the transient recovery by draining off any charge present on C_1 and C_2 that remains because D_3 and D_4 have not sufficiently bypassed the pulse to ground.

Q_1 is saturated by the initial pulse. Diodes D_1 and D_2 isolate the pulsed current from Q_1 (and the transducer) after the pulse drops below 0.7 v, thereby keeping the nonthermal noise contributions of the pulser out of the receiver. Q_1 drives the MC1350 radio-frequency/intermediate-frequency amplifier with a phase-split signal to increase the effective gain of the circuit and aids in isolating it from the pulser. To achieve a circuit gain of more than 50 decibels, a second MC1350 amplifier is added.

The output of the second amplifier drives a diode detector composed of D_5 and D_6 and the filter $R_{10}C_3$. Fullwave rectification is essential for optimum resolution, since the echo may be shifted 180° by the reflecting surface producing it.

A simplified equivalent circuit of the output stage of the MC1350 is shown at the bottom of the figure. A fast rise time for incoming signals is achieved by discharging C_3 through the 1-kilohm impedance of one of the output transistors. The longer fall time needed for a smooth

Pulse-echo receiver. Circuit (a) responds to wideband radio-frequency signals with good signal-handling capability. Time-dependent gain control is provided for sophisticated sonar applications. Choice of low-impedance rf amplifier (b) optimizes response.



echo envelope is attained by recharging C_3 through R_{10}. In some applications, it is desirable to provide a control to vary the fall time by adjusting C_3 and to reject echoes of small amplitude by varying R_8, R_9, and R_{10}.

At small signal levels, an approximate square-law response is provided by the logarithmic characteristic of the 1N916 diodes. The sum of currents I_1 and I_2 in the MC1350 is 5.6 milliamperes typical, as specified by the manufacturer. The currents determine the operating point of the diodes. With the circuit values shown, a quiescent current of approximately 0.8 mA flows through each of the diodes D_5 and D_6.

Although integrated circuits are widely available that perform low-level detection, the desired detector characteristics can be more easily achieved with the circuit described. Furthermore, a stable (oscilloscope) baseline and a large dynamic range are easier to attain if the detector is driven by a reasonably high rf voltage source. The amplifiers in this circuit make this possible by providing adequate predetection amplification.

The signal at the output has a well-defined leading edge suitable for determining time differences between the pulse and its echo with an oscilloscope. A 10-v offset occurs at the output. It may be removed with a base-line restorer circuit consisting of a decoupling capacitor, a resistor tied to 12 v, and a germanium diode to clamp the baseline to about 0.3 v. Another approach uses a differential amplifier.

For sophisticated systems, a time-dependent gain control can be added to the rf amplifiers. A 0-to-12-v ramp voltage, the amplitude of which depends on the range and anticipated attenuation of the echo, can be applied to pin 5 of the devices through R_{11} and R_{12}, which control the distribution of stage gain. The ramp voltage should be positive and decrease with time to provide a gain that increases with time. If pin 5 is grounded, the amplifier operates at full gain. Although the ramp is usually synchronized with the transmit pulse, it may be synchronized with other sources, such as the surface echo from an attenuating target. □

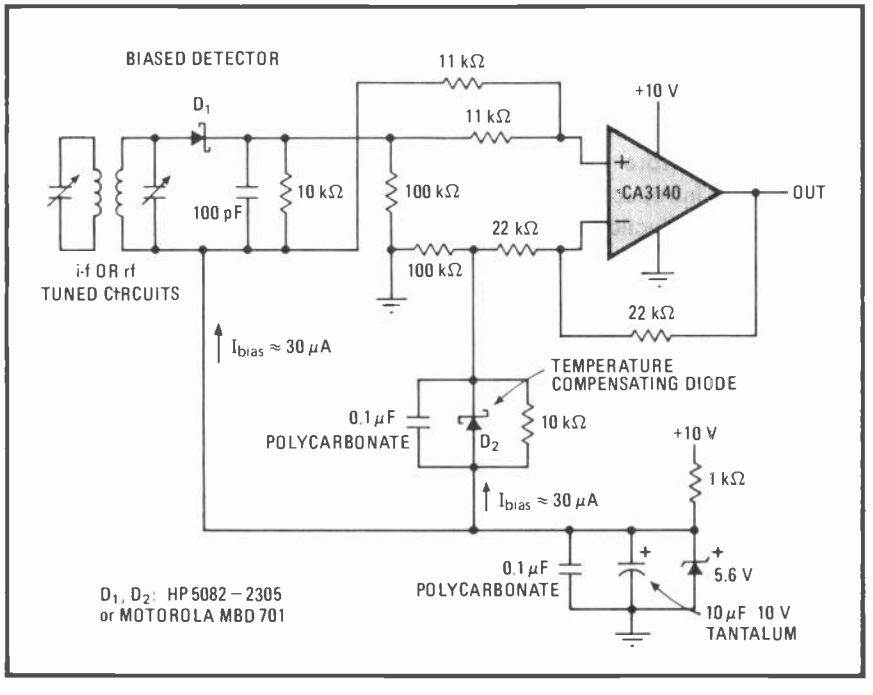
Biasing the diode improves a-m detector performance

by Antonio L. Eguizabal
Vancouver, British Columbia, Canada

The sensitivity, dynamic range, and linearity of a standard amplitude-modulation diode detector improve if the diode is biased into its conducting region. Sensitivity and dynamic range increase because the incoming radio-frequency signal does not encounter the barrier-potential voltage of the diode before the onset of rectification. Linearity improves because the biasing voltage shifts the operating point of the diode into the linear portion of its characteristic curve.

As shown in the figure, signals are applied to D_1, a Schottky diode that can be used at frequencies approaching 1 gigahertz. It has a low barrier potential (0.35 volt), about one half that of conventional silicon diodes, and allows linear operation at a lower biasing voltage than is possible with conventional diodes.

A 5.6-v zener and the voltage divider composed of the 10-kilohm resistor and D_1 send 350 mv across D_1, making it conduct. The voltage drop across D_1 is in effect eliminated for rf signals, making possible the detection of millivolt-level signals. The demodulated signal appears across the resistance-capacitance filter



Tweaked detector. Even the old reliable a-m detector can be improved. Increased sensitivity, linearity, and dynamic range are obtained by dc biasing diode D_1 into conduction, to eliminate voltage drop as seen by rf driver. D_2 provides temperature compensation.

composed of the 100-picofarad capacitor and the 10-kilohm resistor.

Most diode detectors are used in conjunction with automatic-gain-control circuits to produce a constant audio output over a wide dynamic range. To ensure minimum response time of the diode detector, which is required when driving the agc, direct coupling between the two is necessary. Temperature compensation is therefore needed to eliminate drift caused by small temperature-dependent offset voltages.

A second Schottky diode and an operational amplifier, the CA3140, provide this function. Diode D_2 is biased similarly to D_1, with the result that voltage changes caused by temperature variations are almost identical across both devices. The CA3140 operates as a unity-gain wideband amplifier. It has a high common-mode rejection ratio and draws low input-biasing currents, qualities required in a good buffer amplifier.

The noninverting port of the op amp accepts the demodulated signal from the RC filter. The temperature-variable voltage drop across D_1 tends to increase the output voltage, but this is countered by an identical voltage across D_2 at the inverting port. Thus the net voltage change at the output as a function of temperature is approximately zero. Note that the op amp is operating with a single-ended power supply, which assures that D_2 is used in a temperature-compensating capacity only and does not upset the operation of the rf detection circuit.

This detection circuit can respond to a 10-mV rf input signal, and its dynamic range is 10 to 15 decibels greater than that of conventional diode detectors. In addition, the linearity of the circuit, especially at low levels, is noticeably better. □

Maximum voltage detector needs no a-d conversion

by Ronald Lumia
University of Virginia, Charlottsville, Va.

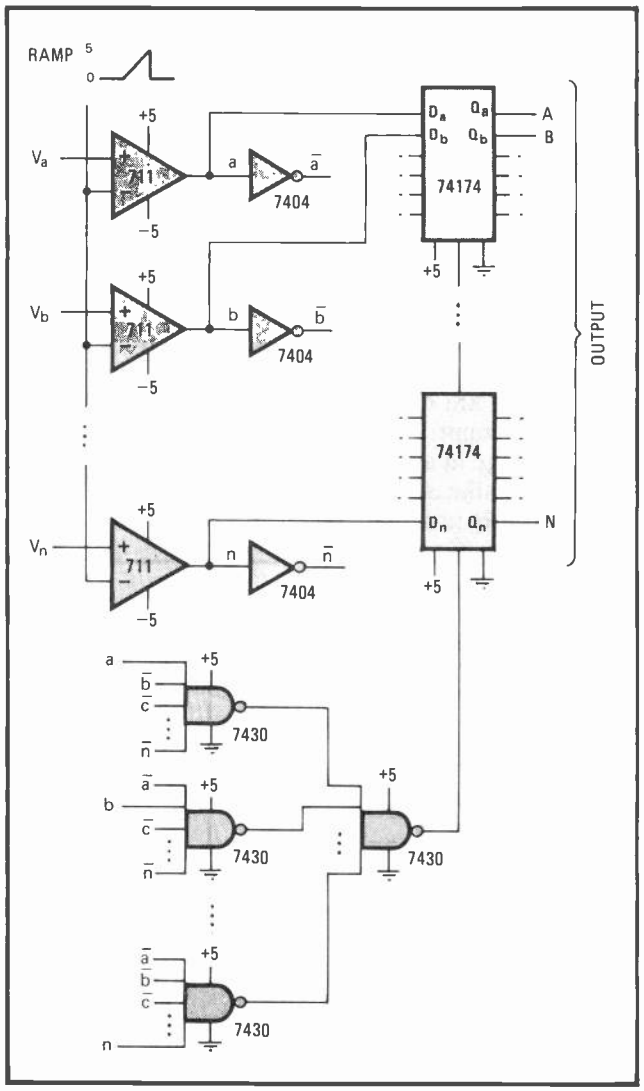
A detector that determines which of a set of analog voltages has the greatest positive value is useful for pattern-recognition systems and other classifying schemes. Only the relative magnitude of the input voltages is important in these applications, so that costly analog-to-digital converters are not needed.

As shown in the figure, a sample set of voltages is introduced at the noninverting port of a bank of 711 dual differential voltage comparators, which initially switch each amplifier high. All inverting inputs are driven by any monotonically increasing waveform, such as a ramp voltage.

Each comparator switches into the low state as the ramp voltage exceeds the particular sample voltage connected to its input, until only one comparator remains in the high state. The signal at this op amp input has the greatest amplitude in the sample set.

The combinational logic at the 7430 NAND gate array then generates a pulse to the 74174 device, clocking the lone logic 1 signal from the op amp input into the D input of its associated flip-flop and presenting it to the processing device. By this time, the ramp voltage has returned to its minimum value, and the next sample set may be again introduced.

As shown, the range over which the sample-set voltages may be detected lies between zero and 5 volts. This range may be changed by suitable adjustment of the ramp and supply voltages to the comparators. The use of complementary-metal-oxide-semiconductor logic circuits is advised when the operating voltage to the comparators exceeds 5 volts. □



Maximum-voltage detector. Relative maximum of sample set $V_1 - V_n$ is determined by ramp generator and logic circuit. Sample voltages drive all comparators high if values lie above the minimum ramp voltage. Logic detects lone op amp remaining high during the ramp sweep and clocks that state to its D flip-flop.

Modular switch array includes priority encoder

by Thomas L. Sterling
Sigma Consultants Inc., Virginia Beach, Va.

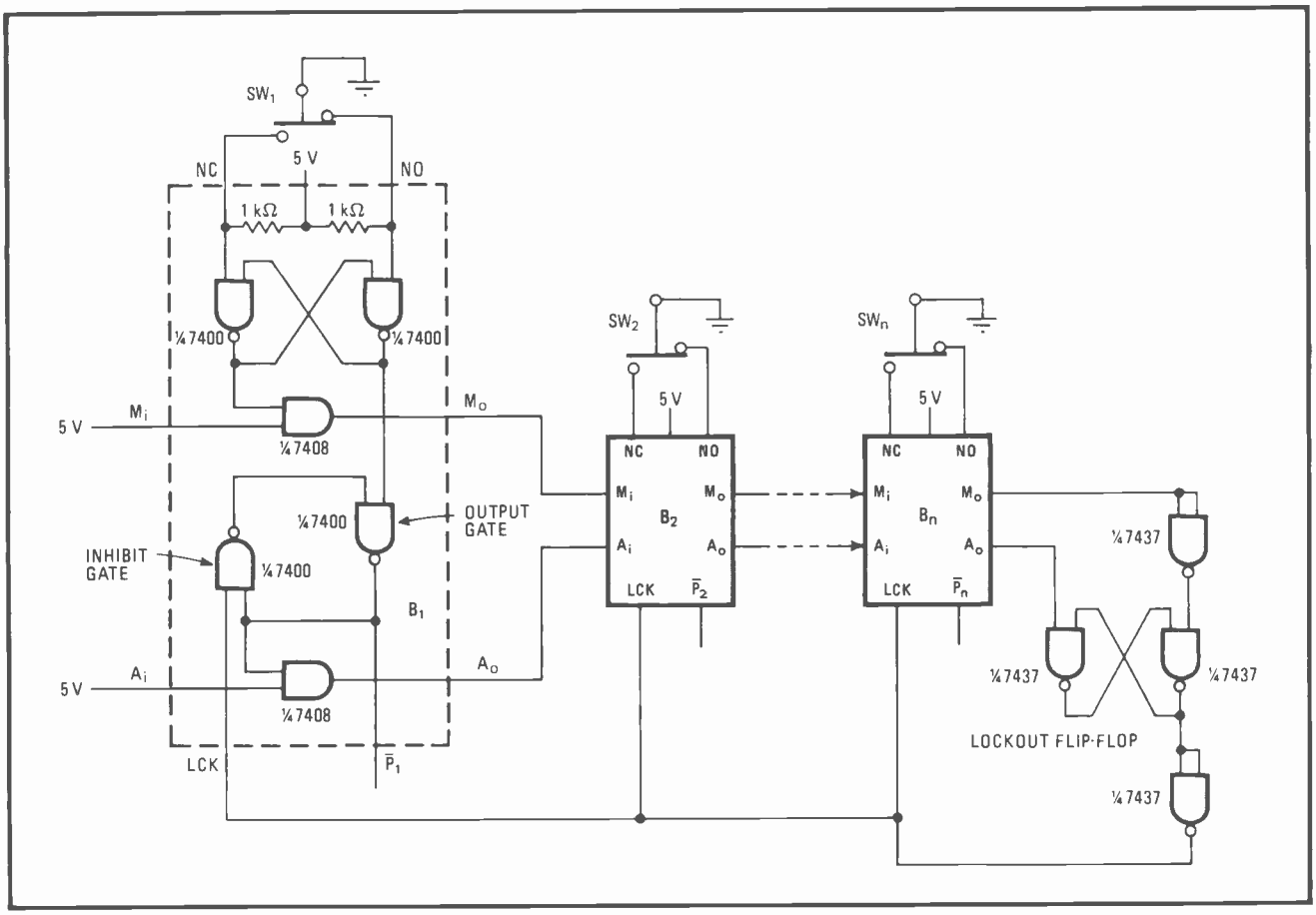
The output ports of this momentary-contact switch array respond to the first command received, and the circuit locks out all subsequent commands, providing a time-sequence priority scheme often needed in industrial systems. The low-cost circuit prevents simultaneous switch depressions from spoiling system operation, and the modularized design technique employed makes it fairly simple to implement.

The structure for this switch array is shown in the figure. A number of single-pole, double-throw switches (SW_n) are individually interfaced through the same number of switch buffer modules (B_n) to a single set-reset flip-flop at the output of the last module. This flip-flop generates a lock-out signal to ensure that only one module at any given time can be in the active state.

Each module contains its own SR flip-flop, a gated output driver with inhibit circuitry, and two AND gates. The flip-flop is configured to circumvent switch contact bounce and has its inputs connected to the normally open (NO) and normally closed (NC) contacts of each switch. The inverting output is combined with the M_i input signal through an AND gate to derive the M_o output. The noninverting output of the flip-flop is applied to the gated output driver. Each module is cascaded by connecting the M_o and A_o ports to the M_i and A_i ports of the next buffer.

Depressing any switch drives the $\overline{P}_i$ output of its associated module low. The M_o and A_o ports of the last buffer module in the chain move low at this time, permitting generation of the LCK signal.

The inhibit gate in each module will prevent the output gate from going low, irrespective of the state of the input flip-flop, if the buffer module output, $\overline{P}_i$, is inactive. If the buffer module is active, the inhibit gate will be inactive, independently of the state of the LCK



Priority encoding. First switch to close captures its output buffer. Circuit disables all other buffer output lines by generating a lockout (LCK) signal. Release of switch or switches automatically resets circuit. The truth table of the switch array is illustrated.

TRUTH TABLE FOR SWITCH ARRAY BUFFER															
Time	SW_1	SW_2 . . .	SW_i . . .	SW_R . . .	SW_{n-1}	SW_n	$\bar{P}_1$	$\bar{P}_2$ . . .	$\bar{P}_i$ . . .	$\bar{P}_k$ . . .	$\bar{P}_{n-1}$	$\bar{P}_n$	M_{on}	A_{on}	LCK
t_0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
t_1	0	0	1	0	0	0	1	1	0	1	1	1	0	0	1
t_2	0	0	1	1	0	0	1	1	0	1	1	1	0	0	1
t_3	0	0	0	1	0	0	1	1	1	1	1	1	0	1	1
t_4	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
t_5	0	0	0	1	0	0	1	1	1	0	1	1	0	0	1
t_6	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0

output. The lockout flip-flop is not reset until the M_o signal at the last flip-flop moves high again. This occurs when the switch is released.

Once the switch first depressed is released, all module outputs become inactive, even if other switches were activated after a particular module had been set. Only after all switches are released can one of the buffers become active again. The operation of the switch array is shown in the illustration.

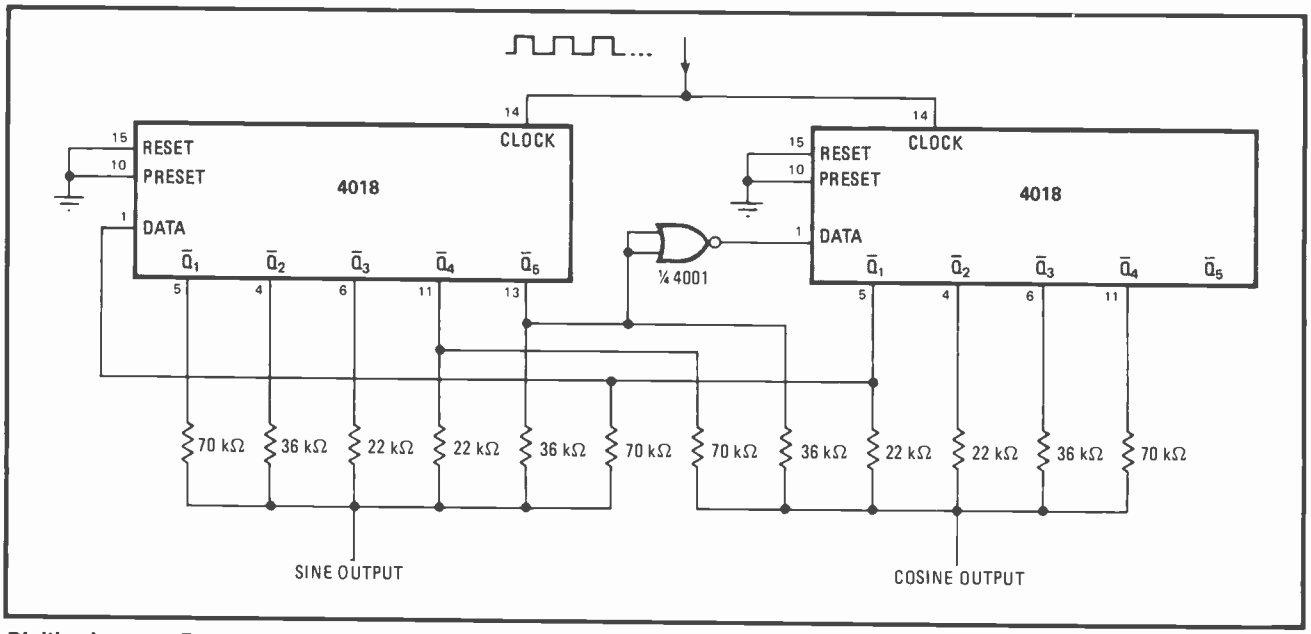
This design can accommodate up to 30 switches. This limit on their number is set by the driving capability of the inverter driver of the lockout flip-flop. □

Ring counter synthesizes sinusoidal waveforms

by Timothy D. Jordan
Texas A & M University, College Station, Texas

A digital circuit composed of only two counters and a weighted resistor network is as good at producing sine and cosine waveforms as many quadrature oscillator networks. Because matched components are not used, design considerations are radically simplified.

Use of the digital technique eliminates many components. The upper frequency limit of the oscillator is 250 kilohertz, and it is not affected by the frequency limitations of operational amplifiers, because no op amps are used. Tweaking the oscillator is not necessary, because no special circuitry is needed. And the sine and cosine waveforms are equal in magnitude at every frequency, because no integrating or differentiating circuits are used. It is even possible to transform the circuit into a digital-to-sine-wave converter with little modification, if



Digitized waves. Frequency dividers and weighted resistor network generate sine and cosine waveforms. The 4018 counters divide input frequency by 12. First counter provides 12-bit approximation of sine function. Second device lags by 90°, producing cosine waveform.

the counters' parallel input ports are used to accept binary signals.

As shown in the figure, two cascaded 4018 complementary-metal-oxide-semiconductor integrated circuits wired as a single ring counter are driven by the master clock. The 4018s divide the input frequency by 12. The digital clock advances the ring counter by one count on the positive clock transition, and each output port moves from the high to low state sequentially.

The resulting current through the weighted resistor network at the counter's output produces a 12-step approximation of a sine wave. The output stages of the second 4018 produce a cosine wave, since it is delayed three clock periods, or one quarter of a cycle, with respect to the first counter.

The first appreciable harmonics to appear at the output are the 11th and 13th, and they may be filtered out with a passive resistance-capacitance filter. Identical filters should be used for each counter so that the phase shift introduced is equal for both output waveforms. The input frequency may be as high as 3 megahertz; above 1 MHz, no filtering is necessary. □

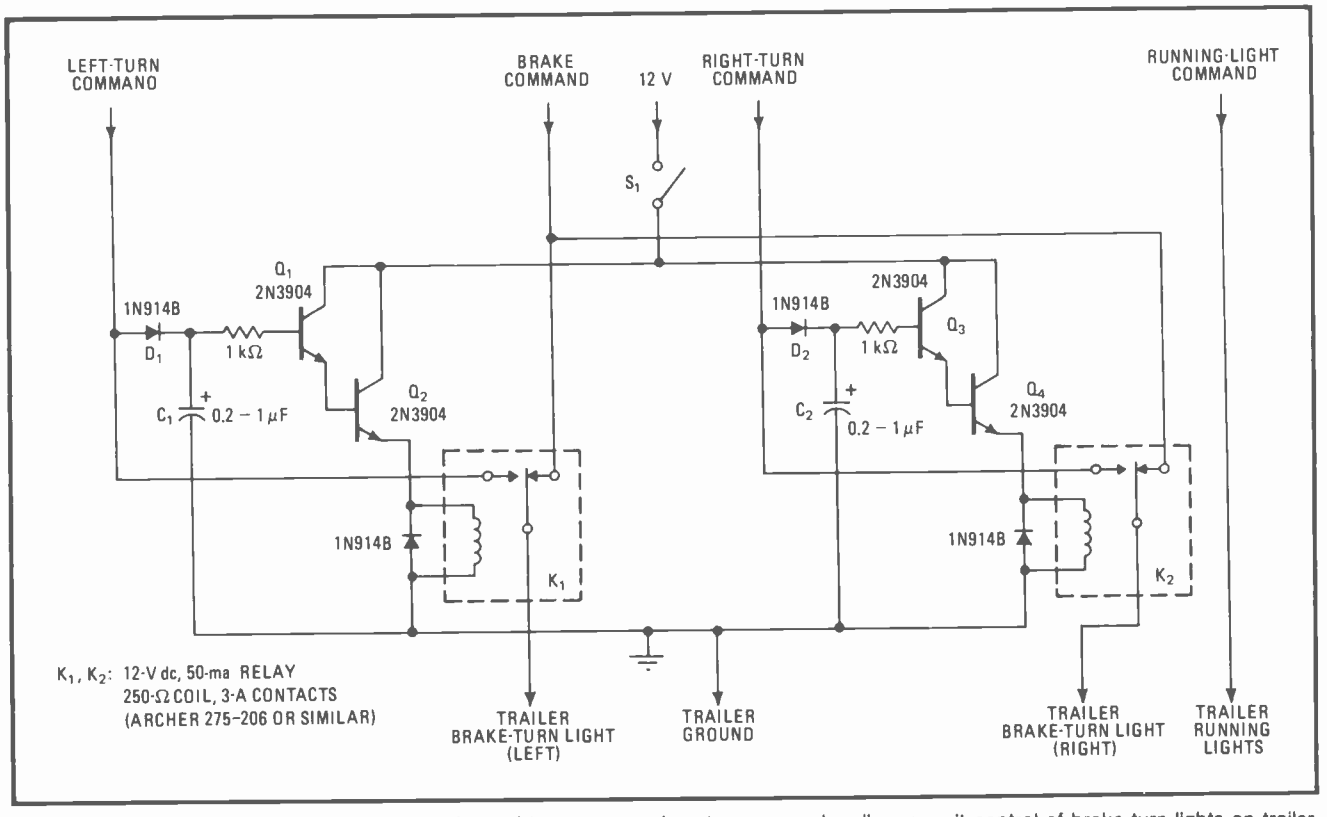
Darlington-switched relays link car and trailer signal lights

by M. E. Gilmore, and C. W. Snipes
Florence, Ala.

New cars with separate turn and brake signals—a safety feature—require a special circuit to properly drive the combination turn-and-brake lights on a trailer; otherwise, if the trailer lights are connected to the brake command, the turn signal will not work, and connecting the lights to the turn command will not yield a brake signal. But two relays and low-cost transistors will combine the signals onto a common bus again, ensuring that the trailer's lights respond to both commands.

As shown in the figure, the brake-command line is normally connected to the trailer lights through relays K_1 and K_2 during normal operation. However, a left- or right-turn command will turn on the respective Darlington amplifier, Q_1Q_2 or Q_3Q_4, thus activating K_1 or K_2. The turn signal is then routed to the lights.

Capacitors C_1 and C_2 charge to the peak amplitude of the turn signal, which flashes at one to two times per second. C_1 and C_2 should therefore be selected to hold the relay closed between these flash intervals (0.5 to 1.0 second), but no longer. If the capacitance is too large, the brake signal cannot immediately activate the trailer lights after the turn signal is canceled. Diodes D_1 and D_2 prevent capacitor discharge through the left or right turn-signal lines, respectively. □



Auto-to-trailer interface. Relays multiplex brake and turn commands onto common bus line, permit control of brake-turn lights on trailer. Darlington amplifiers provide high command-line isolation and sufficient drive for the relays.

Monolithic timers form transducer-to-recorder interface

by T. George Barnett
Laindon, Essex, England

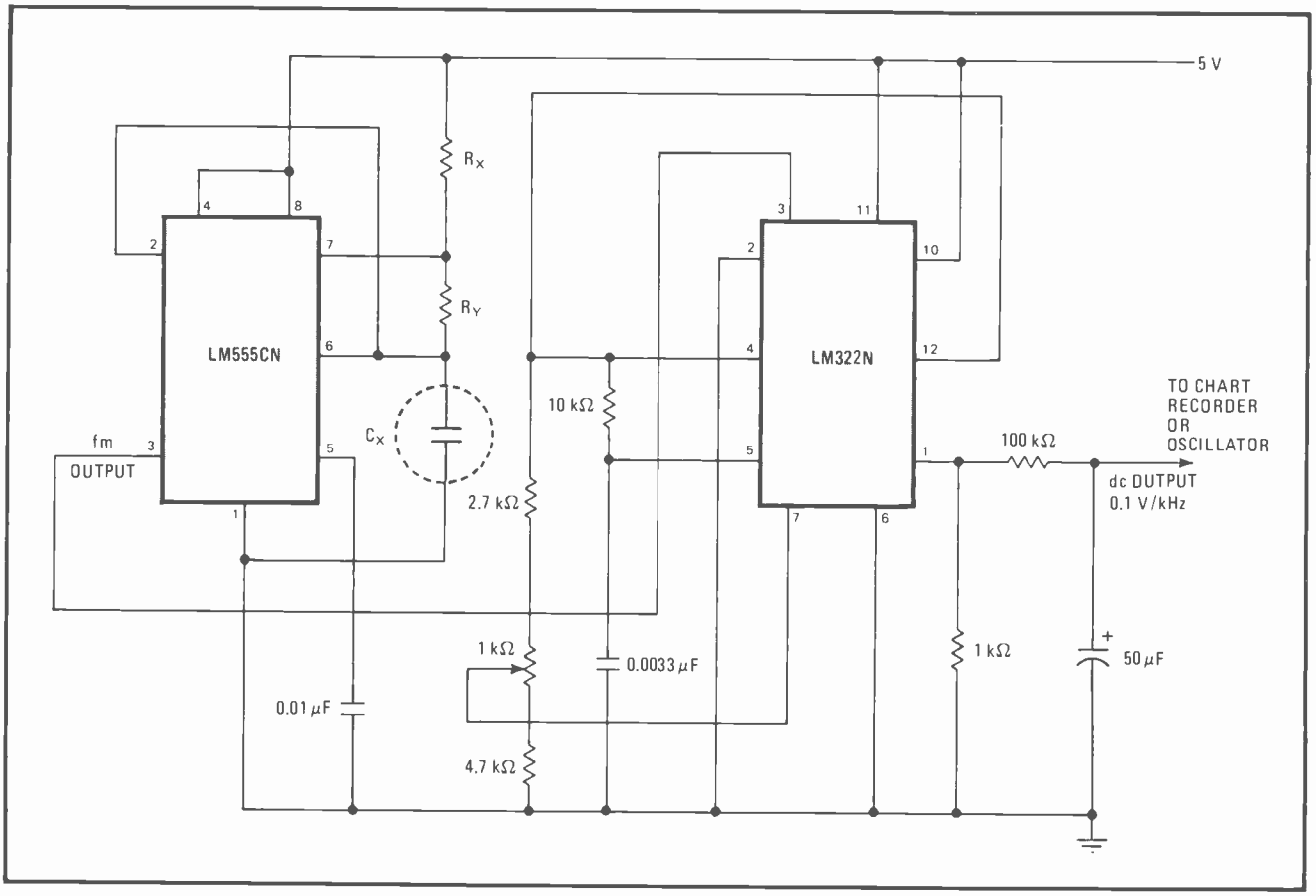
Capacitive transducers often require an expensive capacitance bridge to transform sensed capacitance variations into a voltage for presentation on a chart recorder or oscilloscope. A circuit using two monolithic timers can provide both a capacitance-to-voltage interface and a simple and accurate method for measuring the transducer capacitances.

As shown in the figure, the transducer serves as a capacitive frequency-determining element for the 555 timer. This makes it possible to measure transducer capacitances indirectly, while isolating the transducer from the scope or chart recorder to minimize the loading effect. The LM555CN timing device is connected in the astable mode, its free-running frequency set by R_x, R_y, and C_x. The transducer, typically in the range of 0.001 to 100 microfarads, is element C_x in the timing network.

As the transducer capacitance varies in response to the physical parameter being measured, the output frequency of the 555 varies linearly. The ratio of R_x to R_y sets the duty cycle, which depends on the frequency range desired.

The output of the 555 is presented to the LM322N timer. This circuit, wired as a monostable multivibrator, and combined with the one-pole resistance capacitance filter, forms a frequency-to-voltage converter. The dc output voltage varies linearly with the input frequency, and has a slope of 0.1 volt per kilohertz. The linearity is within 0.2% over the output voltage range of 0 to 1 v.

A 1-kilohm potentiometer connected to pin 7 of the 322 adjusts the output pulse width, serving to calibrate the system to a specified voltage at 10 kilohertz or some other frequency. To ensure linearity, the collector of the output transistor, pin 12, is fed to pin 4 (V_{REF}), so that the amplitude of the pulse at pin 1, the emitter of the output transistor, is constant. The period of the one-shot should be much less than the period of the astable multivibrator for best results. □



Transducer-to-recorder interface. Two timers determine transducer capacitance, perform capacitance-to-voltage conversion for chart recorder, while isolating transducer from output-circuit loading. Transducer placed in timing network of 555 astable multivibrator determines its frequency. LM322 one-shot, which should have a much shorter period than the multivibrator, transforms frequency into voltage

Resistor-controlled selector simplifies CB channel synthesis

by Peter Saul
Ferranti Electronic Components Division, Lancashire, England

This selector, which can derive up to 256 channels for citizens' band or amateur-radio applications, combines the convenience of single-control tuning with the versatility of digital frequency synthesis. A potentiometer replaces the binary-coded-decimal thumbwheel or rotary switches normally used to tune a band about any frequency initially set by a synthesizer external to the circuit. There are no special layout requirements.

Although some excellent circuits have been developed using a slotted disk and optosensors, there are mechanical problems involved in making the disk and sensor mountings, and the systems are generally too complex and costly. In addition, these systems do not return to the set frequency after a power-down. This circuit overcomes those drawbacks.

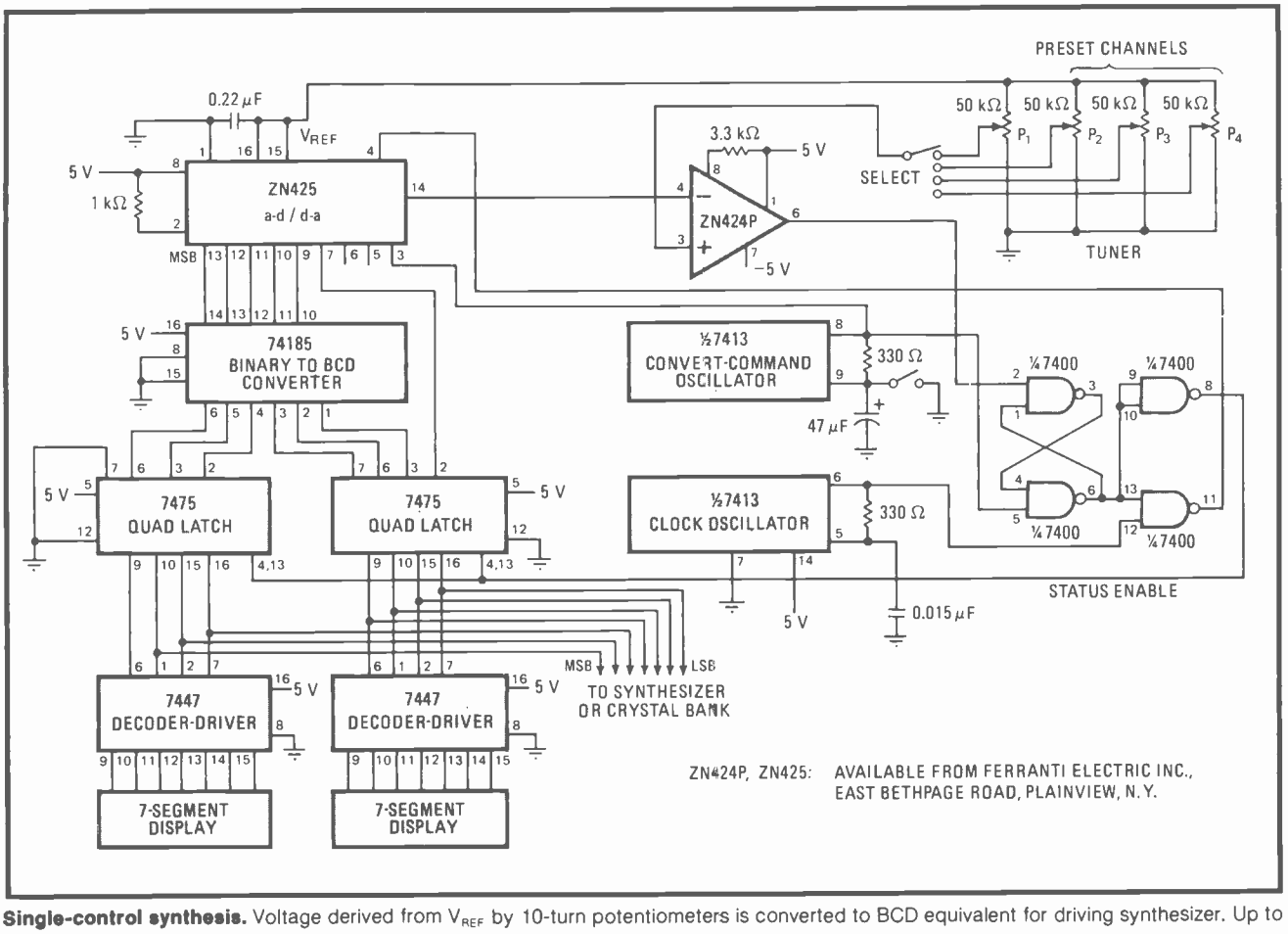
The system uses a potentiometer with 10 turns or more, an analog-to-digital converter, and straightforward logic designs as shown in the figure. A good choice for the analog-to-digital converter is the Ferranti ZN425E, which has an on-chip counter.

A voltage derived by P_1 (in the tuner circuit) from the on-chip voltage, V_{REF}, is applied to the noninverting input of the ZN424P low-noise, high-gain amplifier. The voltage must be converted to its BCD equivalent by the a-d converter.

The conversion begins as the ZN425 starts counting in binary after the initialization from the convert-command oscillator. The counter is advanced by the clock oscillator, which is gated through the 7400 array. As the counter advances, a linear ramp voltage is generated at its output at pin 14. This signal is introduced to the noninverting port of the ZN424. When the ramp voltage exceeds the voltage set by P_1, the output of the op amp falls, resetting the flip-flop in the 7400 and terminating the count. This process is repeated 70 times per second.

The 7475 latches capture the data and drive the 7447 decoder and drivers so that the channel number, from 0 to 63, may be displayed. The 7-bit word also drives the synthesizer. For 256 channels, two additional 74185 converters are needed, as are an additional 7475, 7447, and seven-segment display. The actual frequency of the channel is determined by the design of the oscillator in the synthesizer.

The circuit returns to its initially set channel after power-off or power failure, because the same comparison voltage appears at the noninverting input of the ZN424P. Temperature and voltage stability are good,



Single-control synthesis. Voltage derived from V_{REF} by 10-turn potentiometers is converted to BCD equivalent for driving synthesizer. Up to 64 channels are generated by 74185 and ZN425. Additional BCD converters, latches, and displays are needed for a 256-channel synthesizer.

provided good-quality potentiometers are used. Under extreme combinations of temperature and voltage changes, a one-channel shift has been observed, but that is not a serious problem. In addition, it is extremely difficult to set the frequency between channels. Power drain from the circuit is 350 milliamperes, but it may be reduced considerably if low-power transistor-transistor logic replaces the standard devices. □

Double-ended clamp circuit has ideal characteristics

by Keith Wilson
Herga Design and Development Ltd., London, England

The quad operational amplifier and the analog multiplexer in this dual-threshold clamp circuit give it ideal characteristics—in particular, razor-sharp clamping. Two op amps in the array serve as comparators, determining the relationship of the input signal amplitude to the high and low reference levels, and the multiplexer passes one of the three signals, depending on the op amps' decision. The absence of feedback networks simplifies design and optimizes performance and ensures that component values and layout will not be critical.

The ideal characteristics of the clamper are made possible mainly by the use of op amps. They permit independent adjustment of upper and lower clamp points and simplify the solution of any temperature-compensation problems. In addition, the op amps will detect millivolt-level differences between the input signal and the set thresholds, so that the multiplexer will accept signals within the thresholds and pass them undisturbed to the output but will block signals exceeding the thresholds.

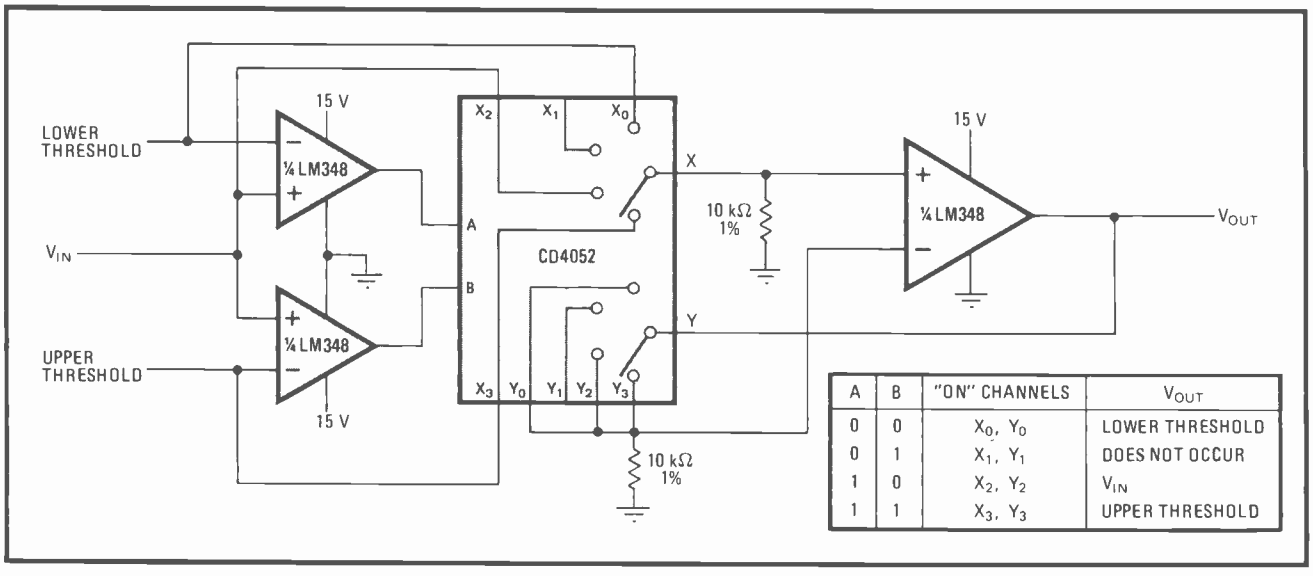
As shown in the figure, an input signal is introduced to the noninverting ports of two op amps making up one half of the LM348 device. The high and low reference levels are applied to the inverting input ports. The op amps, operating as comparators, run at open-loop gain and are powered from a single-ended supply. Both drive the CD4052 differential four-channel multiplexer.

Each comparator may be in one of two states at any given time. Therefore, in combination, both comparators may assume one of four possible states. The control signals from the comparators are applied to the A and B inputs of the multiplexer, which routes the input signal, the upper threshold voltage, or the lower threshold voltage to the output amplifier. Thus a hard clamping action takes place. Between the limits of the clamping levels, circuit response is linear, as can be determined from the truth table at the bottom of the figure.

Changes in the channel resistance of the multiplexer switches are caused by supply voltage and temperature variations, but are due chiefly to the amplitude variations of the input signal. The purpose of the output amplifier circuit is to compensate for the amplitude distortion introduced by the multiplexer switches.

Without compensation, the signal encounters a voltage divider composed of the switch resistance and the 10-kilohm resistor at the input to the output amplifier (added to improve switch linearity). By using another 10-kΩ resistor and the remaining switch in the 4052, the gain of the op amp can be made to increase proportionately to switch resistance.

Supply voltage changes amounting to several volts cause negligible change at the output of the op amp. Temperature variations create errors amounting to only a few millivolts. □



A	B	"ON" CHANNELS	V_{OUT}
0	0	X_0, Y_0	LOWER THRESHOLD
0	1	X_1, Y_1	DOES NOT OCCUR
1	0	X_2, Y_2	V_{IN}
1	1	X_3, Y_3	UPPER THRESHOLD

Dual-threshold clamper State of comparators driving analog multiplexer ports A and B determines which of three inputs appears at V. Circuit response is linear between threshold limits. Truth table describes circuit function.

555 timer isolates equipment from excessive line voltage

by R. J. Patel
Tata Institute of Fundamental Research, Bombay, India

Instruments and appliances can be easily damaged when the line voltages that power them become excessively high or low, but a voltage-sensing circuit using the 555 timer will disconnect the equipment from the power lines if the set limits are exceeded. This circuit offers a better alternative for protecting instruments than a voltage stabilizer circuit, which is usually effective for detection and compensation of short-term variations only.

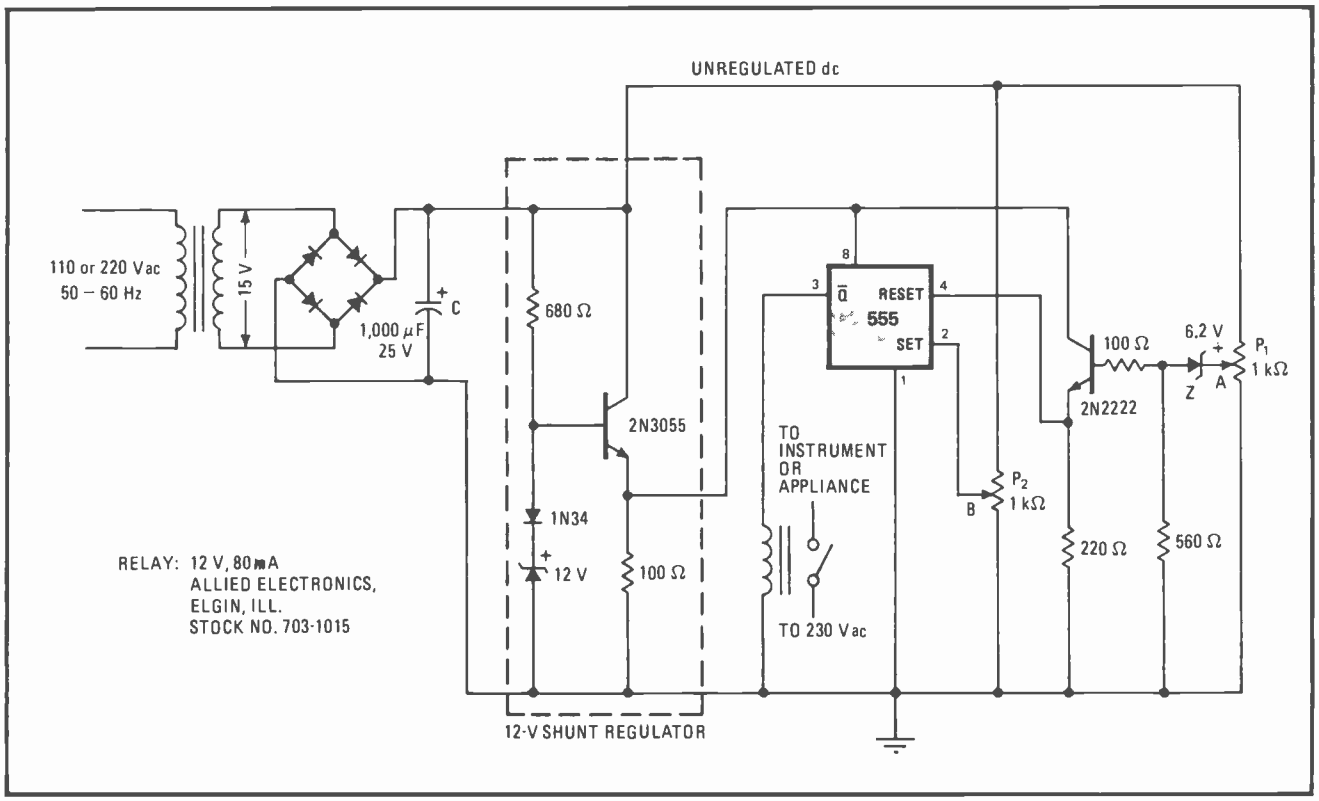
As shown in the figure, the line voltage is converted to approximately 15 volts by the step-down transformer, whose turns ratio is determined by the magnitude of the incoming voltage at the primary winding. This voltage is rectified, then filtered by capacitor C and applied to a 12-v regulator in order to bias the timer and the 2N2222 sense transistor. The magnitude of the unregulated voltage varies proportionally with the line voltage, as is to be expected, and this voltage is continually sampled by potentiometers P_1 and P_2, the upper and lower threshold controls.

The 555 timer is used in the bistable mode, and its state is a direct function of the voltages on its set and reset ports, pins 2 and 4, respectively.

Under normal conditions—that is, when the supply line voltage is within the set limits—the unregulated dc voltage at point A is sufficient to fire zener Z, saturating the transistor. Pin 4 of the timer rises rapidly to 12 v; when this voltage exceeds two thirds of the 12-v bias voltage on the timer, or 8 v, pin 3 moves high and the relay is energized.

If the ac line voltage is below the low set value, the voltage at A is below the value needed to fire the zener, and the relay is de-energized. When the line voltage shoots above the set upper limit and the dc voltage at pin 2 exceeds one third of the 12-v supply voltage, the relay is de-energized as pin 3 moves low.

The upper and lower set limits can be set with an accuracy of ±5 v of the true ac line voltage if precision potentiometers are used. There is no set-point hysteresis, because of the avalanche breakdown characteristics of the zener Z. Any transients generated by the power line are rendered harmless by the large filter capacitor C. □



Line-voltage monitor. 555 timer circuit senses if ac line voltage is above or below set limits, then de-energizes line relay if necessary, removing power from equipment. Simple circuit uses set-control potentiometers P_1 and P_2 to monitor unregulated dc voltage, whose value is directly proportional to the ac line voltage. Timer and 2N2222 transistor require the regulated power source.

Resettable electronic fuse consists of SCR and relay

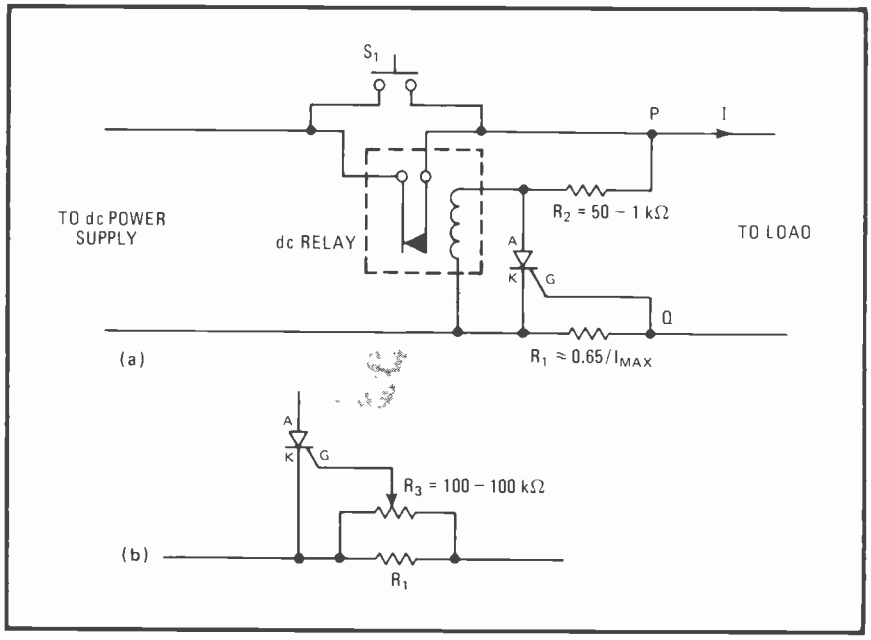
by Russell Quong
Palos Verdes, Calif.

Most direct-current power supplies rely on a circuit breaker, current-sensing circuit, or fuse for current-overload protection, but this simple resettable-fuse circuit has advantages over all three. Built around a silicon controlled rectifier and a line relay, it is faster than a circuit breaker, less complex than most current-sensing circuits, and never in need of replacement.

How the circuit operates is evident from (a). Momentarily depressing S_1 closes the relay so that current flows from the supply to the load. In normal operation, the voltage across points PQ will be equal to the nominal supply voltage, and the normal operating voltage will appear across the relay winding. The relay and resistor R_2 are selected according to the dc supply voltage used and the relay's rated coil voltage, respectively.

Excessive current to the load causes a voltage drop across R_1 greater than 0.65 volt and switches on the SCR. The anode-to-cathode voltage of the SCR in the conducting region is approximately 2 v. This voltage, also across the relay coil, is far below the relay's holding voltage. Consequently, the relay opens, disconnecting the load from the supply. The relay may be reset by depressing S_1 again.

If a variable threshold point for SCR switching is desired, the SCR's gate can be connected to R_1 through potentiometer R_3. Resistor R_1 is calculated as before. □



Electronic fuse. SCR and relay form resettable fuse for dc power supplies. When I_{max} is reached, SCR turns on, opening relay and disconnecting power from load. Depressing S_1 reinitializes circuit (a). SCR switching point may be adjusted with R_3 (b).

Versatile phase detector produces unambiguous output

by L. E. S. Amon and B. Lohrey
University of Otago, Department of Physics, Dunedin, New Zealand

A dual monostable multivibrator and integrator network forms a detector that not only measures phase difference between two signals throughout the entire 360° range, but also produces an unambiguous output signal for various phase-advance and -retard conditions by generating a voltage and slope output combination that is unique for every angle.

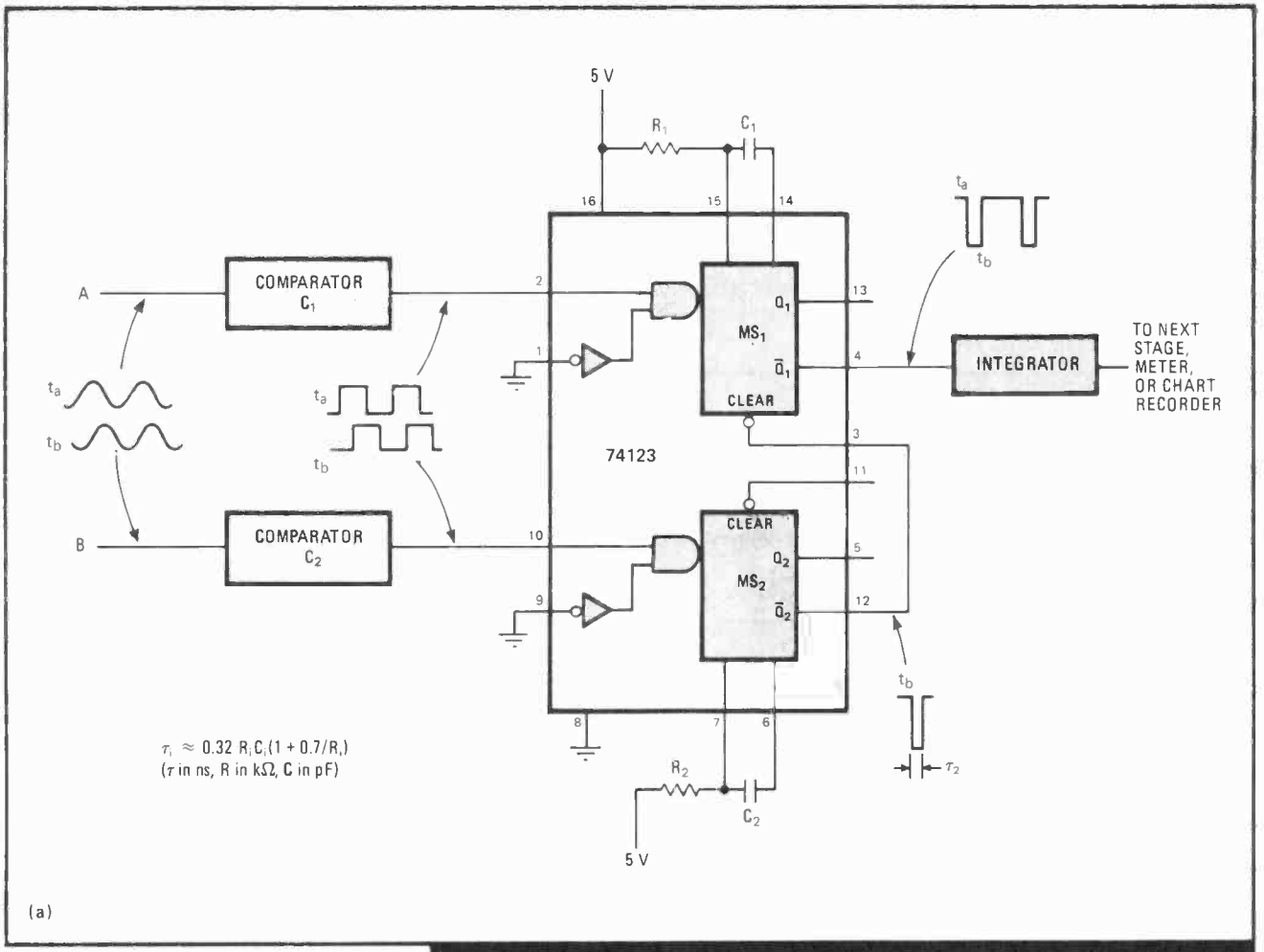
As shown in (a) of the figure, a positive zero crossing of reference signal A triggers the comparator C_1 and one-shot MS_1 at time t_a, where MS_1 is one half of the 74123 device. This one-shot, in the retriggerable mode and set so that its pulse width τ_1 is greater than T_a, the period of the reference signal, stays on until comparator C_2 and one-shot MS_2 are fired by signal B at time t_b. The narrow pulse produced by MS_2 resets MS_1.

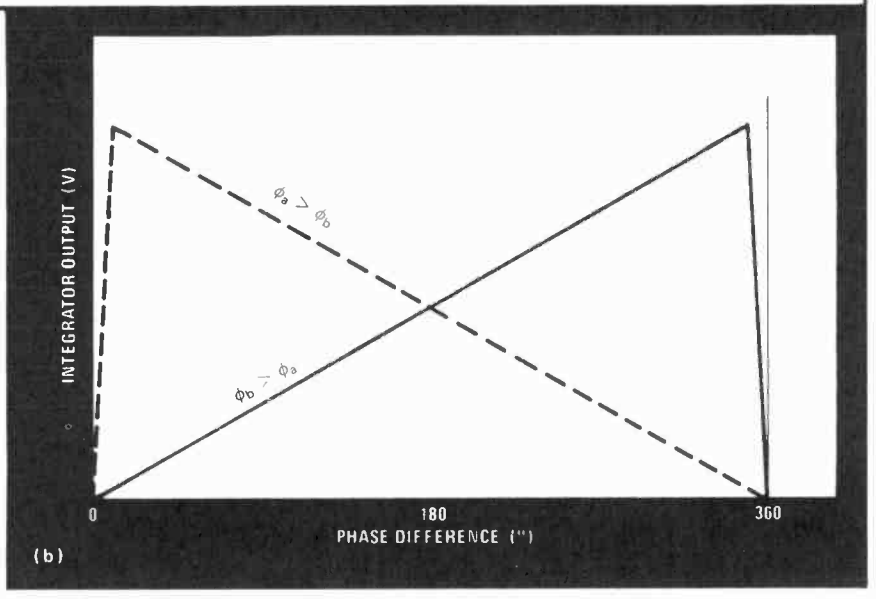
The phase of B with respect to A may be related to the duty cycle of the output signal from MS_1. The duty cycle may be expressed by:

$$W = \frac{t_b - t_a}{T_a}$$

The output signal may be converted to a dc voltage by the integrator network connected to the output of MS_1. Alternatively, the phase may be measured digitally [see *Electronics*, Dec. 20, 1973, p. 119].

As shown in (b), an increase in the dc output of the integrator occurs when the phase angle of B increases





360° phase detector. Dual one-shot and integrator yield unambiguous voltage and slope output combination for changing pnase-lead or phase-leg angles (a). Output from integrator increases when B leads A, decreases when A leads B(b).

with respect to A. The output decreases when the phase angle of B decreases with respect to A. Thus the frequency relation of B to A may be determined from the slope of the integrator's output if the two signals are of similar but not identical frequency.

When the two signals are not harmonically related, their phase relationship will change with time. The circuit is therefore useful as a phase-modulation detector for applications in communications receivers.

Further versatility can be achieved by placing frequency dividers at the input ports of the phase detector to achieve a full-scale output at N × 360°. The sensitivity can be increased, on the other hand, if both of the input frequencies are multiplied by N. This reduces the range of phases that yield an identical output voltage to 360°/N. □

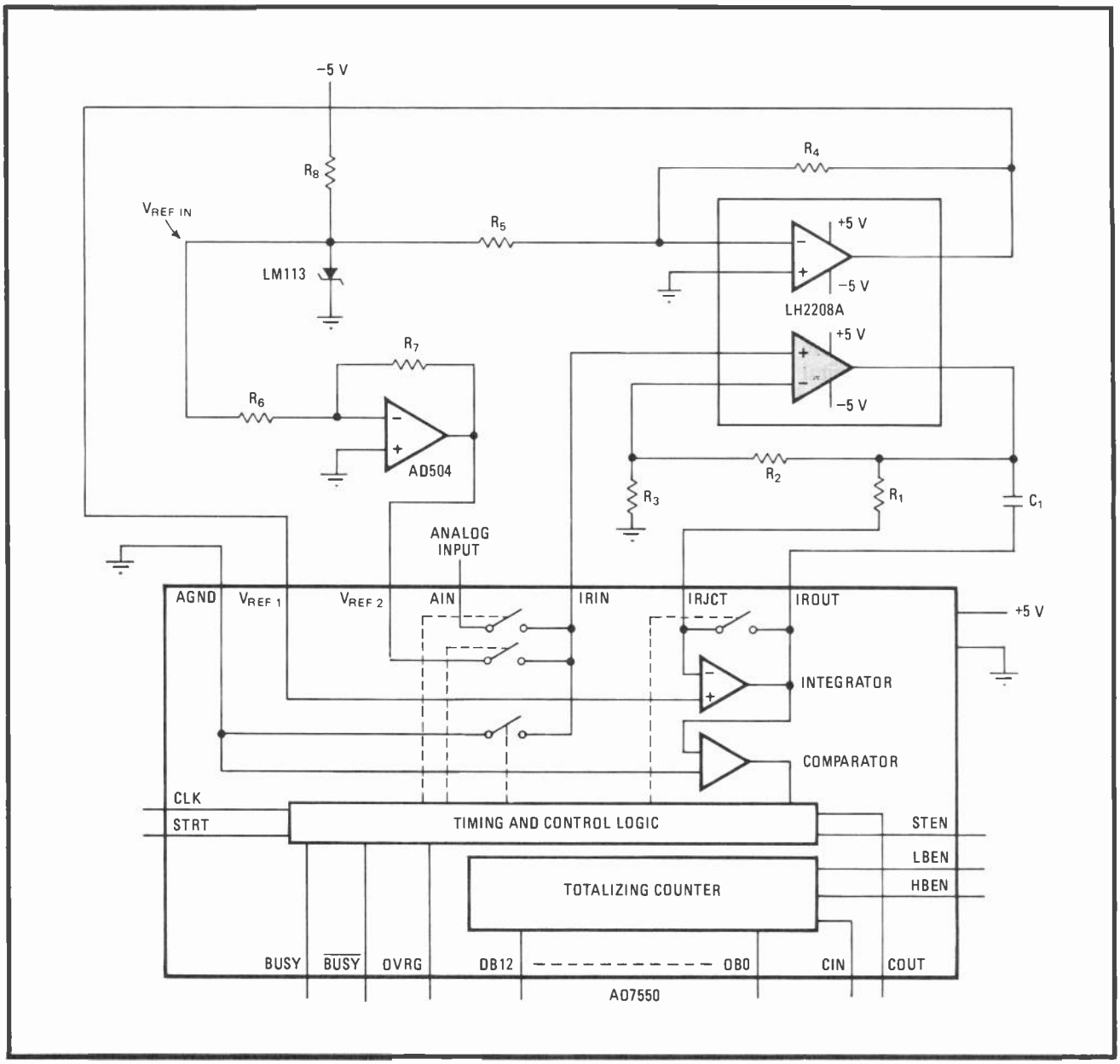
Buffer improves converter's small-signal performance

by Will Ritmanich
Precision Monolithics Inc., Santa Clara, Calif.

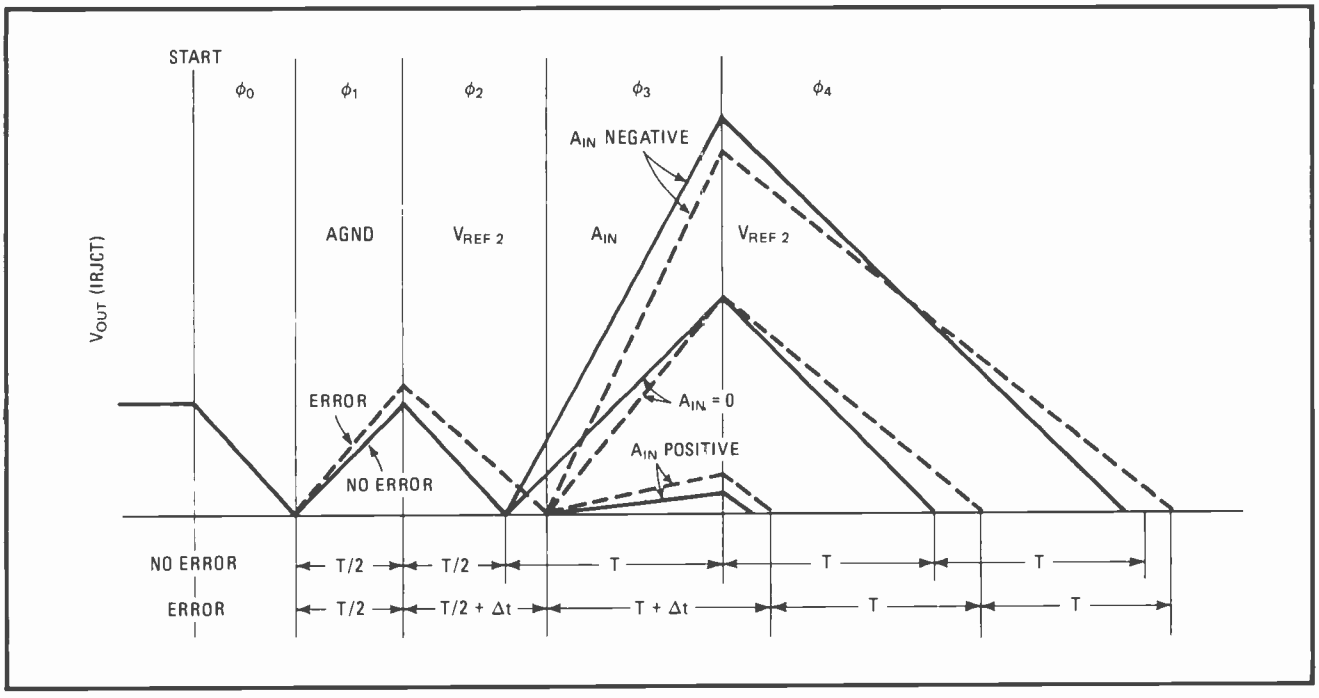
If an operational amplifier is placed in the integration and error compensation loop of the popular AD7550 analog-to-digital converter, the converter can measure microvolt-level signals without errors being introduced by its own or the op amp's offset-voltage drifts. Adding this buffer also increases the impedance of the signal (input) port of the converter, allowing it to be driven from high source impedances.

To understand why an external buffer can improve converter performance, it is necessary to know how the converter processes the input signal. The AD7550 uses the quad-slope integrating method, an improved version of the often-used dual-slope method.

A shortcoming of the dual-slope type is that errors at the input of the integrator due to noise or comparator



1. Improved performance. AD7550 accurately measures even microvolt-level analog voltages if op-amp buffer is placed in converter's integrator and error compensation loop. Converter views offsets as just another error that has been introduced in integrator loop.



2. Four-phase integration. AD7550 uses quad-slope method to detect most errors, including op-amp offset voltage drifts. This method eliminates error by measuring comparator trip-time delay, Δt, converting Δt to a voltage and subtracting the voltage at end of cycle.

offset drift show up as errors in the digital output word. The quad-slope method detects all AD7550 offset-voltage errors, converts them to a digital equivalent during the integrating cycle, and subtracts them from the final count at the end of the cycle.

Normally, a ground signal, a reference voltage, or an analog input is connected through the converter's integrator input (IRIN) terminal to the integrator junction (IRJCT) port. As shown in Fig. 1, the buffer is connected between the terminal and the port, in series with integrating resistor R_1. The choice of signal is determined by internal logic-controlled switch settings.

Before a four-phase a-d conversion begins, a reference voltage, $V_{REF\,2}$, is applied to the inverting input of the integrator, resulting in a negative-going ramp at the integrator's output port. The ramp resets the output to zero. When the output voltage is equal to the comparator's trip voltage, phase ϕ_1 is initiated.

At this time, a digital counter starts and the integrator is connected to input AGND to determine whether the converter's negative supply voltage is at ground potential. If not, an error voltage is generated that is proportional to the difference.

The output of the integrator rises proportionally to the error voltage until the counter stops counting system clock pulses, at fixed interval T/2, (Fig. 2.) Then ϕ_2 is initiated. The accumulated voltage on the integrating capacitor, C_1, is proportional to AGND × T/2.

During ϕ_2, the integrator is connected to $V_{REF\,2}$ and any error voltage on this signal. The output of the integrator falls at a rate proportional to the error until the comparator trip point is reached. If there are no errors, the counter stops after time T; otherwise, the trip time is delayed by Δt.

ϕ_3 then begins, starting a second counter that ultimately displays the digital equivalent of the analog input voltage introduced during the phase. $V_{REF\,2}$ is again applied during ϕ_4, and the counter continues to run until the integrator falls below the comparator trip point. $V_{REF\,2}$ is normally equal to $2V_{REF\,1}$, and the converter detects any difference.

Because ϕ_1 through ϕ_3 occupy a total period of 2T if there are no errors, any errors detected during these phases must show up as a delay in trip time by Δt. Since the charge gained during ϕ_3 by the integrating capacitor is proportional to $A_{IN\,av} \times T$, and the charge lost will be equal to $V_{REF\,2} \times \Delta t$ during ϕ_4, then the number of counts (N) relative to the normalized (full-count) time is equal to:

$$\Delta t/t = A_{IN\,av}/V_{REF\,2} = N$$

and is displayed directly. Thus any offset error in the buffer will not affect system accuracy, because it will be viewed as an additional (series-introduced) error existing during ϕ_1 through ϕ_4. At the same time, the amplifier can still be used to boost small-signal input voltages.

The gain of the amplifier may be determined by resistors R_2 and R_3 and is equal to:

$$G = \frac{(R_2 + R_3)}{R_3}$$

To maintain the proper relationship between $V_{REF\,1}$ and $V_{REF\,2}$, resistors R_2 through R_7 are employed in the circuit and are determined by the equations:

$$V_{REF\,1} = (R_4/R_5)V_{REF\,in}$$

and:

$$V_{REF\,2} = \frac{R_7}{R_6}\frac{R_2 + R_3}{R_3}V_{REF\,in} = 2V_{REF\,1}$$

$V_{REF\,1}$ and $V_{REF\,2}/2$ should be within 6% of each other at all times. Otherwise, in ϕ_2 and ϕ_4, during which time

$V_{REF\,1}$ is compared with $V_{REF\,2}$, error voltages will be generated that the converter cannot compensate for.

This conversion technique requires a stable reference voltage at the V_{REF2} terminal of the AD7550, and therefore the LM113 zener diode is used with the low-offset AD504 op amp for the greatest accuracy. □

Timer and converter generate slow ramp for chart recorders

by David Wingate
London Hospital Medical College, London, England

A long sweep time increases the effectiveness of an X-Y chart recorder in monitoring slow system changes. An astable multivibrator operating at low frequency and a versatile digital-to-analog converter can be used to generate an extremely linear, low-frequency ramp for the X axis, and at low cost, too. Although many good chart-recorder systems have the ability to hold down the distance the pen traverses to 0.02 centimeter per second, this circuit can limit it even further—in the neighborhood of 1 centimeter per hour, if needed.

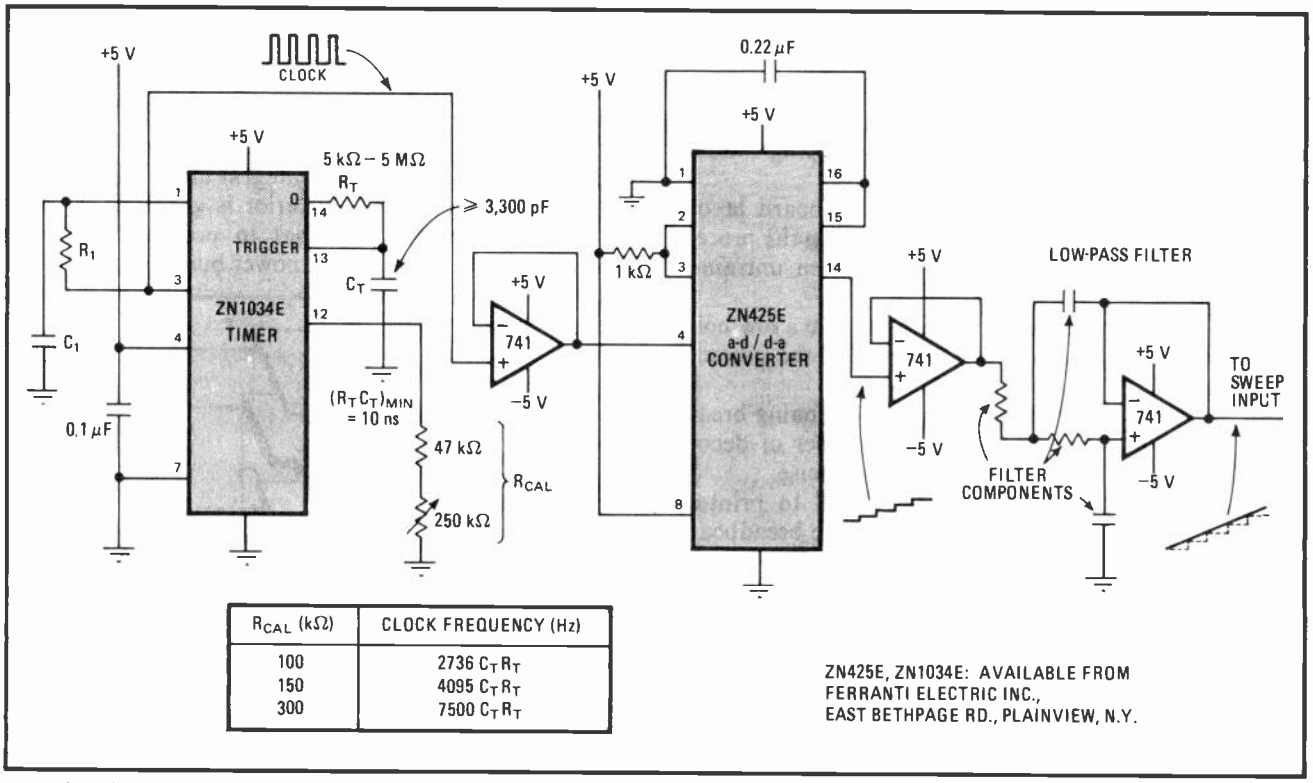
In this circuit, the rate of increase in the ramp voltage produced by the converter is controlled by the frequency of the timer. As shown in the figure, the clock for the circuit is the Ferranti ZN1034E precision timer, operated in the astable mode. This device is somewhat unusual in that the pulse width of the oscillations produced is controlled by R_1C_1 but the frequency of oscillation is controlled by combination $R_TC_TR_{cal}$. The second combination is part of the astable network, detecting the fall of the output pulse and retriggering the timer, and thus controlling its basic repetition rate.

R_T and C_T are held constant, with R_{cal} the variable resistor. The table in the figure shows the relation of R_{cal} to the pulse frequency. The pulse width is not critical for timebase applications, but it can be varied if required. The width equals $0.6\ R_1C_1$ seconds, where R is expressed in kilohms and C is expressed in picofarads.

After passing through a buffer stage, the clock drives the binary counter in the Ferranti ZN425E d-a converter, which is wired to serve as a ramp generator. The rate of increase in the magnitude of the ramp voltage is a function of the clock frequency; since the output rises incrementally, a staircase approximation of a ramp is generated. After passing through a buffer, the ripples in the staircase waveform are smoothed by a standard low-pass filter tuned to the clock frequency.

By increasing the capacity of the converter from an 8- to a 12-bit device, it is possible to generate a ramp voltage having even greater resolution. The circuit has served well in an application involving prolonged recording of biomedical and biological data, but, many other nonmeasurement applications are possible. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.



R_{CAL} (kΩ)	CLOCK FREQUENCY (Hz)
100	$2736\ C_TR_T$
150	$4095\ C_TR_T$
300	$7500\ C_TR_T$

ZN425E, ZN1034E: AVAILABLE FROM
FERRANTI ELECTRIC INC.,
EAST BETHPAGE RD., PLAINVIEW, N.Y.

Slow time base. Low ramp frequency for X input of chart recorder, permitting long-period monitoring assignments of various systems, is generated by d-a converter and timer. Slope of ramp voltage with respect to time is determined by clock frequency.

Square-root counter calculates digitally

by S. H. Tsao
National Resarch Council, Ottawa, Canada

A square-root counter has many uses, notably the measurement of the root-mean-square output voltage of a transducer that has a square-law response. This counter finds the square root digitally, rounded off to the nearest bit, of any analog voltage that has been converted into a digital train of N pulses by a voltage-to-frequency converter. In other words, the circuit finds the square root of N.

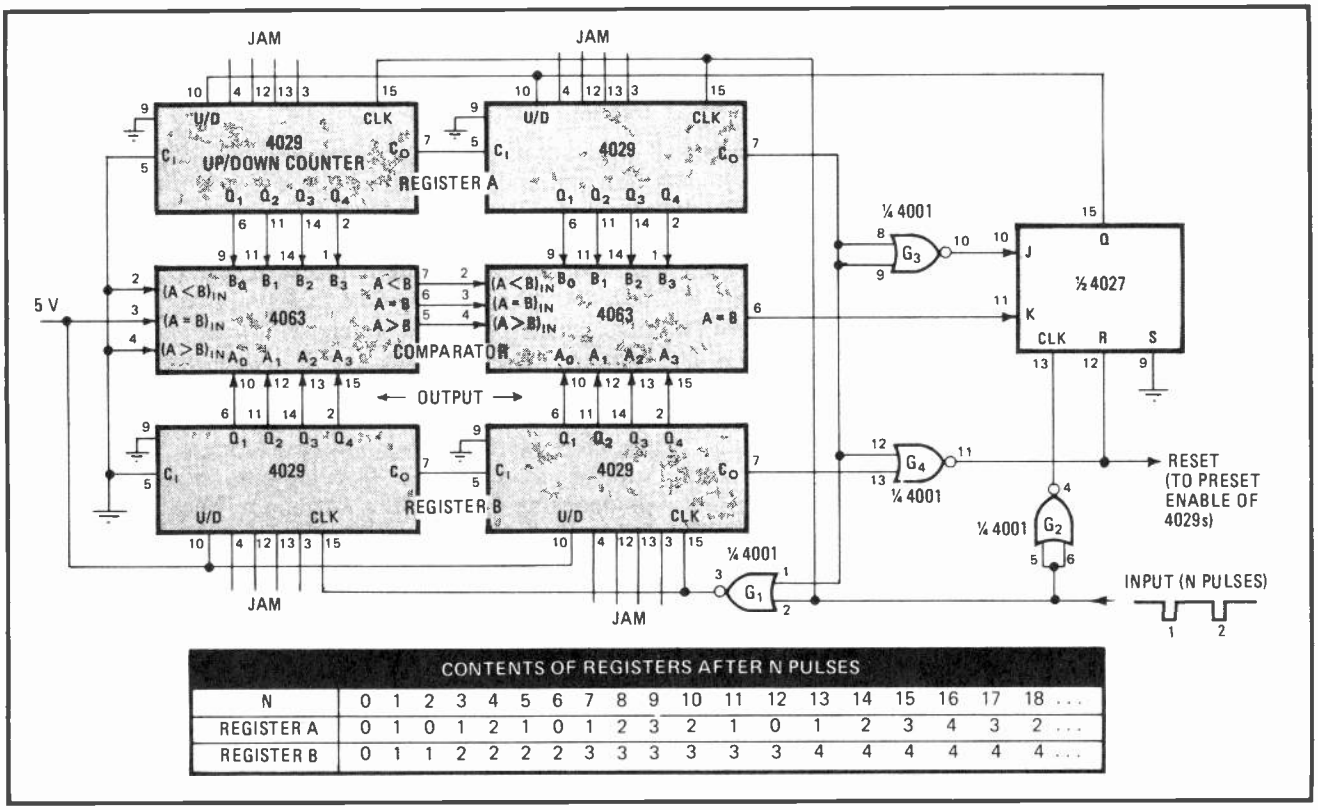
Of course, square-root circuits that generate an analog-voltage output already exist, but they usually require accurate square-law diodes and scaling components like resistor voltage dividers. This circuit, being all-digital, eliminates those shortcomings and in addition is much simpler than the digital square-root detectors now available.

Two registers and a comparator do most of the work. Four 4029 complementary-metal-oxide-semiconductor up/down counters, operating in the binary-coded-decimal mode, form the two synchronously clocked registers, A and B, as shown in the figure. Register A clocks up or down, depending on the state of the C-MOS 4027 flip-flop. Register B advances by one count any time an input clock pulse is received and the carry-out signal ($\overline{C}_o$) of register A is active, or low. The negative-going transitions of the input signal clocks both the flip-flop and B, while positive transitions clock A.

Initially, the flip-flop is reset and both registers are cleared by means of the JAM lines. After the clock pulse (N = 1), register B advances to state 1 and the flip flop is set, placing register A in the count-up mode. Register A then advances to 1 and $\overline{C}_o$ moves high, setting the J input of the flip-flop low.

The C-MOS 4063 comparator detects that the contents of registers A and B are now equal (as they were before, at initialization, and it brings the K input of the flip-flop high.

During the next pulse (N = 2), G_1 inhibits the clock input to register B, and the flip-flop is reset, placing A in the count-down mode. Register A returns to zero, again setting $\overline{C}_o$ low and J high. Then, when N = 3, register B is incremented to 2, while register A counts to 1. On the arrival of a pulse (N = 4), counter A increments to 2, and because the contents of B do not change, an A = B pulse is generated by the comparator. The entire cycle is then repeated, as shown in the table.



CONTENTS OF REGISTERS AFTER N PULSES																		
N	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18 . . .
REGISTER A	0	1	0	1	2	1	0	1	2	3	2	1	0	1	2	3	4	3	2 . . .
REGISTER B	0	1	1	2	2	2	2	3	3	3	3	3	3	4	4	4	4	4	4 . . .

$N^{1/2}$. Register B in the circuit yields the square root of N, rounded off to the nearest bit, where N is the number of input pulses received after the circuit has been reset to zero. Digital circuit eliminates shortcomings of detectors that measure analog voltages directly.

Thus, register A starts an up count one cycle after it has reached 0, and initiates a down count one cycle after it has determined its contents are equal to B. As a result, the output of register $B = N^{1/2}$.

The reset line is activated by G_4 whenever both registers overflow, and this sets both registers to their initial values. It can also be activated regularly by an appropriate timebase for time-averaging measurements. For special applications, the registers may be preset to a nonzero number via their JAM lines. The registers may also operate in the binary mode without their square-root counting function being affected, while the counters may easily be extended beyond their 8-bit capacity, simply by being cascaded. □

Optocoupler in feedback loop aids charger/regulator

by Leonard A. Cherkason
Mt. ISA Mines Ltd., Queensland, Australia

A single, inexpensive circuit that serves either as a voltage regulator or as a charger for low-capacity batteries can be built easily without resorting to usually complex voltage-sensing networks. This circuit uses the diode (emitter) of an optocoupler in a simple feedback loop, permitting easy detection of output voltage changes. It produces a 12.7-volt regulated output at 50 milliamperes or can charge a battery at the same voltage and current limits, and the limits can easily be changed.

The optocoupler is an ideal choice for a detector. The diode senses the output voltage without loading or otherwise disturbing normal operation, and the voltage drop developed across its terminals is constant and relatively small for any charge or load current.

As shown in the figure, the diode bridge and capacitor C_1 rectify and filter an ac input voltage. Assume that the circuit is in the charge mode. If the battery is not fully charged, its voltage will be below 12.7 v ($V_Z + V_D$). This voltage is selected by the choice of an appropriate zener diode, which is placed in series with the optocoupler diode. The 1N2270 pass transistor will therefore be biased on, allowing current to be supplied to the battery. I_A will be limited chiefly by the 220-ohm resistor.

When the battery voltage just exceeds ($V_Z + V_D$), the zener will fire and current I_Z will flow through the optocoupler's diode, switching on its phototransistor and turning off Q. If the battery is removed, thus placing the circuit in the regulator mode, current will be delivered to the load at 12.7 v. Now, of course, the current drain will be determined largely by the load resistance.

The ripple voltage is 25 millivolts in the regulator mode and 1 mv in the charge mode. Line regulation is 30 mv/v, and load regulation is 8 mv/mA over a 5-to-30-mA range. Both may be improved if Q is replaced with a Darlington amplifier.

The output voltage and current may be selected by proper choice of R_1, R_2, and the zener diode. In turn, the resistors may be determined if the battery capacity (C), measured in milliampere-hours, and the input voltage (across C_1) are known.

It has been determined that for best performance, I_A should equal 0.25C. This will occur if the battery is relatively drained. Assuming the input voltage, V_{in}, is much greater than the base-emitter drop across Q, then:

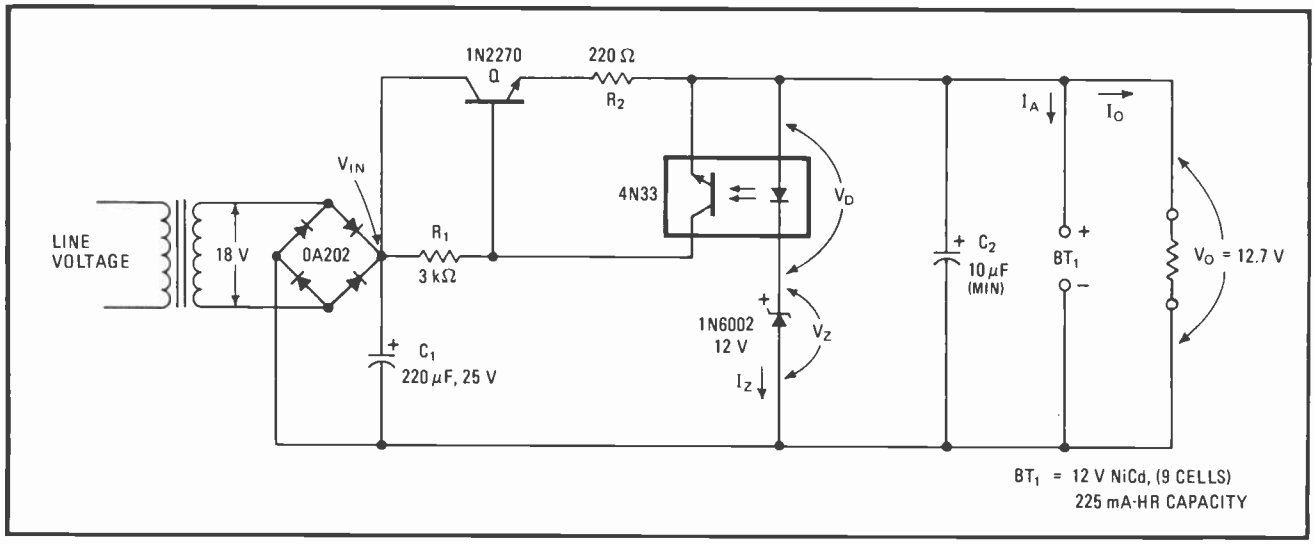
$$R_2 \geq V_{in}/0.25C - R_1/h_{fe}$$

where h_{fe} is the dc gain of Q. To find the minimum value of R_2, assume that I_O is known, from which it can be determined that:

$$R_2 \leq (V_{in} - V_O)/I_O$$

This equation assumes that I_O is greater than I_Z.

The value of R_1 is determined by the minimum value



Regulator or charger? Circuit works as low-capacity battery charger or as voltage regulator when battery is removed. Use of optocoupler eliminates complex voltage-sensing networks. Output voltage and load current can be selected by suitable choice of R_1, R_2, and zener diode.

of I_O, which occurs when Q is nearly off. It can be shown that:

$$R_1 \geq (V_{in} - V_O)/0.02C$$

This equation presumes that the minimum value I_O equals about 0.02C, a condition that again has been determined by experiment, rather than by theoretical considerations. □

Counter and switches select pulse-train length and dead time

by Héctor Gellón and Enrique Marcoleta
San Luis, Argentina

Only the more expensive pulse generators can repeatedly generate a pulse train of selectable length followed by an off time also of selectable length. But this common requirement is easily met by one cascaded counter, two switches, and some logic. The number of pulses in the train is selectable from 1 to 99, and irrespective of the number of pulses delivered to the output, the off, or dead, time can also be varied between 1 and 99 clock periods. The lengths of both the pulse train and the off time may be extended by adding to the number of stages in the counter.

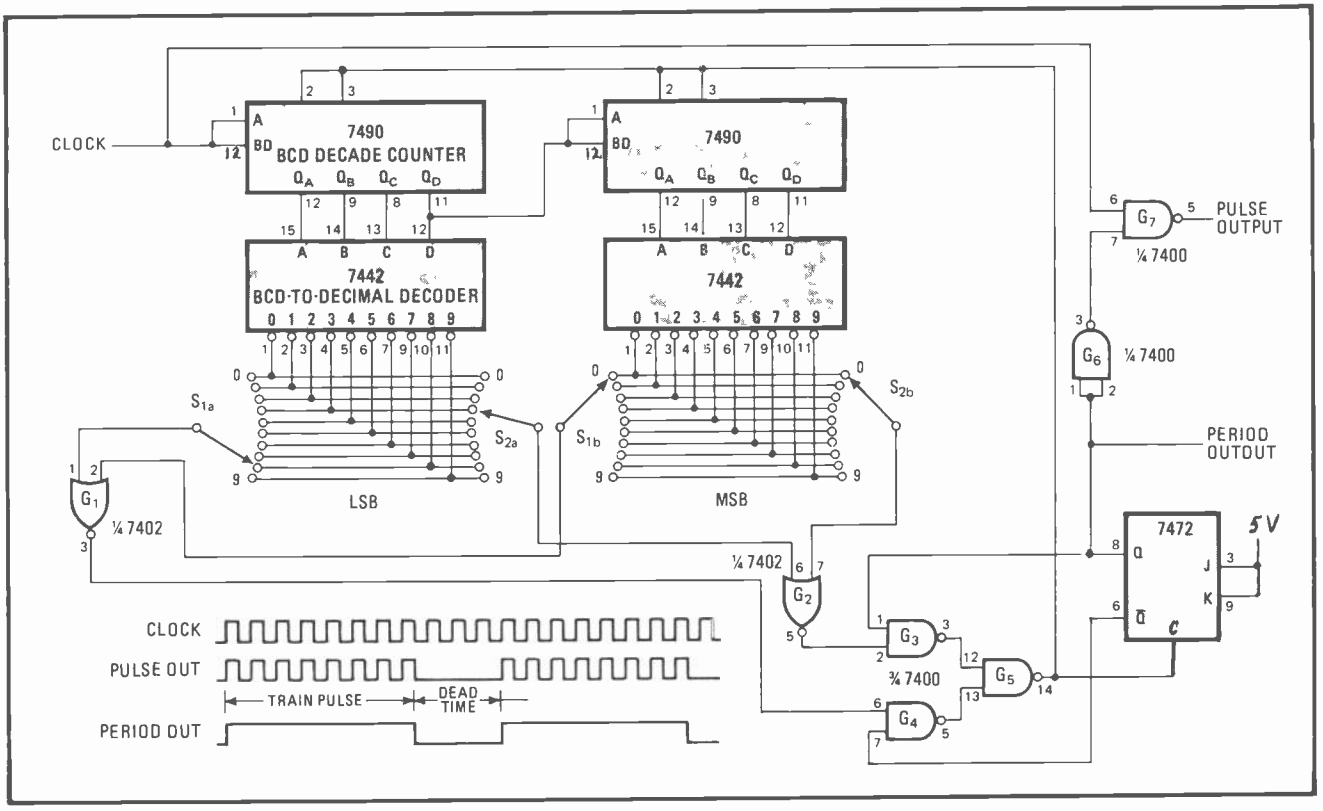
As shown in the figure, a system clock drives two cascaded 7490 binary-coded-decimal decade counters, and their outputs are converted to a decimal equivalent by the 7442 BCD-to-decimal decoders. The decoded outputs are active low, and when the count reaches the pulse-train length desired (preset in this case to 8 by switches S_{1a} and S_{1b}), gate G_1 moves high.

If the $\overline{Q}$ output of the 7472 flip-flop is high, as it will be once the circuit settles after initialization, G_4 moves low. This causes G_5 to assume a high state, resetting the counter and toggling the flip-flop, which in turn disables G_4 and output gate G_7.

There is no output until the counter reaches the number set by switches S_{2a} and S_{2b}. G_2 moves high, causing G_3 to move low and G_5 to go high. The counter is reset, and the flip-flop is toggled, thus once more enabling G_4 and G_7. The pulse train now appears at the output until the settings of switches S_{1a} and S_{1b} are reached, and the cycle repeats.

The $\overline{Q}$ output of the flip-flop is a signal having a duty cycle that may be anything from 1 to 99 times the period of the system clock. It is essentially an ungated version of the signal at the pulse-output port.

Cascading additional BCD counters and decoders to the circuit will extend its pulse-counting and dead-time limits. Of course, more switches and gates must also be added, to accommodate a greater number of inputs. □



Selectable. Generator produces train of N pulse lengths followed by dead time of M clock pulses, set by 2-pole, 10-position switches S_{1a} through S_{2b}. N and M may assume any value of from 1 to 99. Switches are shown set for pulse train of 8, dead time of 3.

Feedback extends sequence of random-number generator

by J. T. Harvey
AWA Research Laboratory, New South Wales, Australia

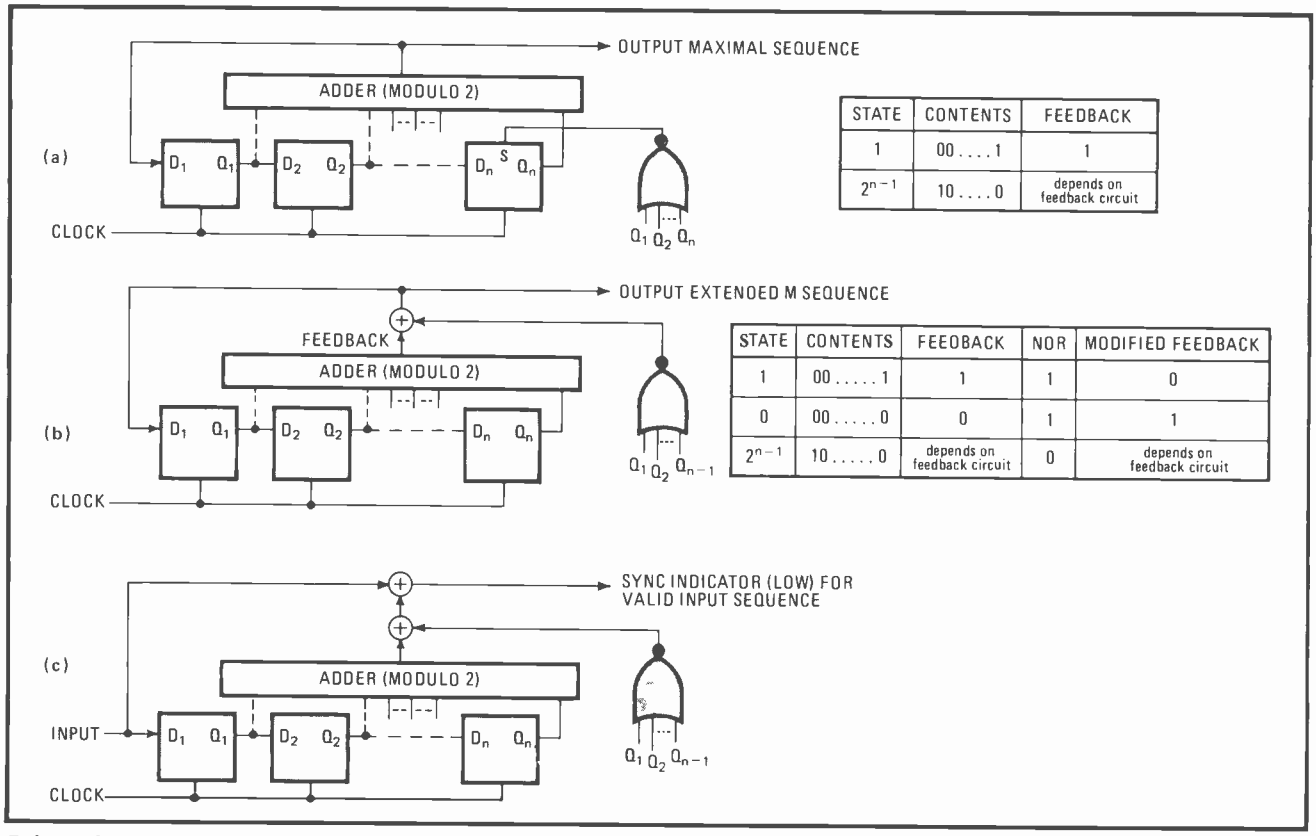
Altering the periodicity of its sequence from 2^{n-1} to 2^n makes a pseudorandom number generator more useful in such applications as frame synchronization, numbering, or identification in a digital communications system. The modification has little effect on the pseudorandomness of the number sequence, and it can be implemented with just a simple shift register and a slightly changed feedback loop.

The usual pseudorandom, or maximal-sequence, generator is shown in (a). It combines a simple feedback circuit with a shift register having a serial output that (in the binary case) is a modulo 2 sum of the nth stage output and one or more of the previous stage outputs. No matter what feedback taps are chosen, however, the output sequence will have a periodicity of 2^{n-1}, because an n-bit register cannot cycle through the zero state (where the state is defined by its binary contents). Obviously as the table in (a) indicates, it is impossible for all the stages simultaneously to contain a 0, because once in this state no new state can be generated with the simple logic used.

Most of the practical sequence generators therefore employ automatic detection of the 0 state on power up, in order to generate a logic 1 state at the output of one register, using a NOR gate as shown. After initialization, though, the random generator will cycle with a period of 2^{n-1}, because the 0 state never recurs. However, as shown in (b), the number of states cycled through can be increased to 2^n if the last input to the NOR gate is connected to the Q_{n-1} stage, instead of the output of the Q_n stage, and if the output of the NOR is connected to a summing port, instead of the set input being connected at the last flip-flop. The resulting m-sequence will now contain an equal number of 1s and 0s.

The logic needed to implement the summing port is small. In most cases, it need consist of a half-adder or a few resistors only. Note from the table in (b) that the all-zero state is detected and used to generate a logic 1.

The same basic circuit can be used in the feed-forward mode to detect a sequence of n bits, too, as (c) proves. This method for checking the presence of a given sequence is of value when the error probability is low. During high-error bursts, however, the circuit's effi-



STATE	CONTENTS	FEEDBACK
1	00....1	1
2^n-1	10....0	depends on feedback circuit

STATE	CONTENTS	FEEOBACK	NOR	MODIFIED FEEDBACK
1	00.....1	1	1	0
0	00.....0	0	1	1
2^n-1	10.....0	depends on feedback circuit	0	depends on feedback circuit

Balanced states. The usual n-stage, pseudo-random number generator cannot generate an equal number of 1s and 0s because it cannot cycle through the register's all-zero state (a). Modified circuit cycles through all 2^n states (instead of the usual 2^{n-1} states) and detects 0s (b). Circuit can be used in feed-forward mode to detect repeating sequences (c).

ciency is reduced because isolated, incorrect bits generate m+1 parity errors when there are m taps driving a half (modulo 1) adder.

Note that the sequence-recognizer circuit in (c) does not require additional logic to prohibit the acceptance of the (false) all-zero data state. A standard sequence checker will give a valid output when it is fed continually by 0s, because it would predict the next input to be a 0, once the register is filled. Thus, an additional n-input NOR gate and an exclusive-OR gate must be added to a standard feed-forward checker to reject an all-zero sequence within the data stream. □

Optocoupler transmits pulse width accurately

by Tadeuz Goszczyński
Industrial Institute of Automation and Measurements, Warsaw, Poland

Though optocouplers work fine in most pulse applications, shortcomings in their switching and temperature characteristics make them poor at such tasks as transmitting pulse-width modulated signals accurately. Adding an operational amplifier to the optocoupler circuit will improve its response time and reduce the effects of temperature on output voltage, enabling it to transmit a pulse width as small as 2 microseconds with an error of only 200 nanoseconds. If a second optocoupler is added to the circuit, temperature problems will be virtually eliminated.

An optocoupler is limited in its ability to transmit pulse width accurately because of two major factors: the response speed of the device is reduced by feedback currents that flow from the output port of the phototransistor to its base, and the current-transfer ratio is highly dependent on temperature. In either the emitter-follower or common-emitter configuration, an output voltage change produces the feedback current and an equal change across the collector-to-base capacitance. A certain time is required for the capacitor to charge to the voltage; this limits the response time and can cause errors in pulse-width transmission.

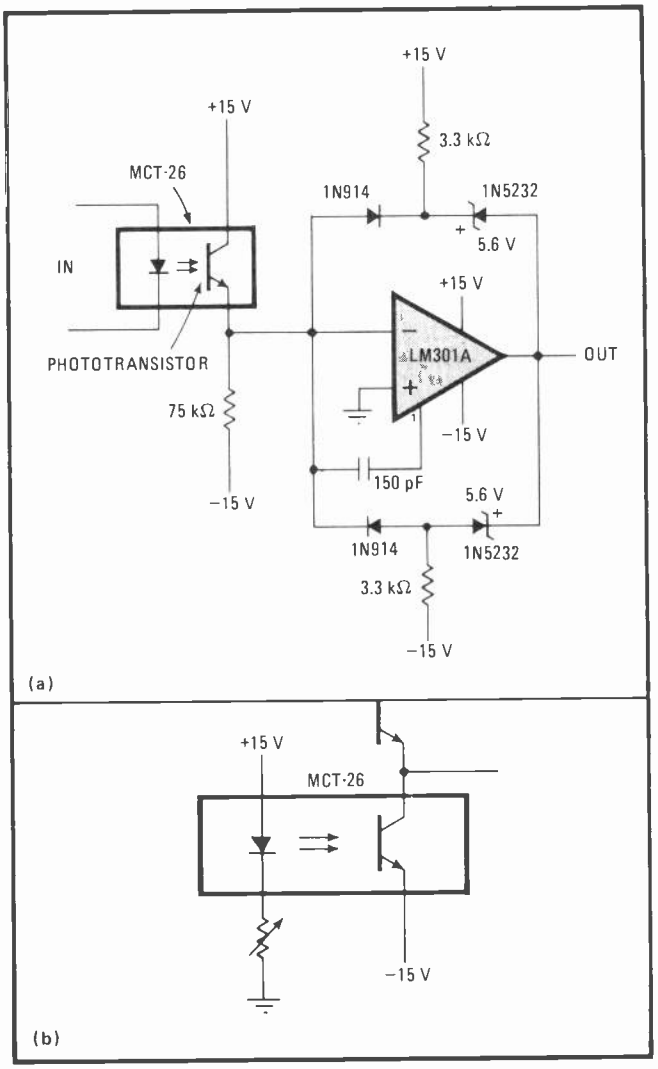
In addition, the switching times as well as the amplitude of the output pulse generated by this current source vary with temperature. All errors may be greatly reduced if the output voltage of the phototransistor is clamped to a near-zero level for any level of output current, in effect making its load resistance zero so that no feedback current is generated.

Tying a current-limiting resistor and an op amp to the output port of an MCT-26 optocoupler does the job, as shown in Fig. 1a. Two separate bidirectional feedback loops, comprising a diode in series with a 5.6-volt zener diode, are connected across the op amp. The 3.3-kilohm resistors supply sufficient bias to the zeners.

The op amp works as a zero-cross detector having essentially open-loop gain. Any signals emanating from the MCT-26 will be introduced to the LM301A op amp, causing it to saturate and switching on one of the two zeners in the feedback loop (depending on the signal polarity). The input voltage is thus forced to zero.

The switching speed of the optocoupler is high, being determined mainly by the op amp's slew rate of approximately 10 volts per microsecond. The circuit speed can thus be raised above the rated bandwidth of the optocoupler, assuming the MCT-26 equivalent load resistance is only a few ohms.

A small temperature error will still exist, because temperature variations will cause a current change in the MCT-26, and this will cause a change in the op amp's zero-crossing times. Replacing the 75-kilohm resistor with the phototransistor of another optocoupler, as shown in (b), will reduce the temperature error below



Accurate transmission. Phototransistor passes signals to output without pulse distortion. Two feedback loops with op amp work in zero-crossing detector (a) to reduce response time and prevent feedback currents that slow circuit speed, causing errors. Replacing a load resistor by second phototransistor (b) reduces temperature-generated errors by an order of magnitude.

3 ns per °C. This ensures equal temperature-dependent voltage drops across both optocouplers, and with them connected as shown, the temperature-generated voltages will cancel. The op amp's temperature coefficient is negligible in comparison and need not be considered. □

Timer IC circuit separates rep rate and duty cycle control

by Arturo Sancholuz
Laboratorio Nacional de Hidraulica, Caracas, Venezuela

Combining both halves of a 556 dual timer with an operational amplifier in this simple circuit enables independent control of the output frequency and the duty cycle. The frequency is adjustable throughout the normal 10-hertz-to-10-kilohertz range of the 556, and the duty cycle is selectable from 1% to 99% of the total waveform period.

As shown in the figure, one half of the 556 (A_1) is connected as an astable multivibrator, oscillating at a frequency given by $f = 1.4/(R_1 + R_2)C$. This oscillator is the frequency-governing element in the circuit.

The negative-going edge of signal v_1 periodically triggers timer A_2, which operates as a monostable multivibrator. An exponential ramp emanating from the threshold port of A_1 drives A_2 through the 531 op amp.

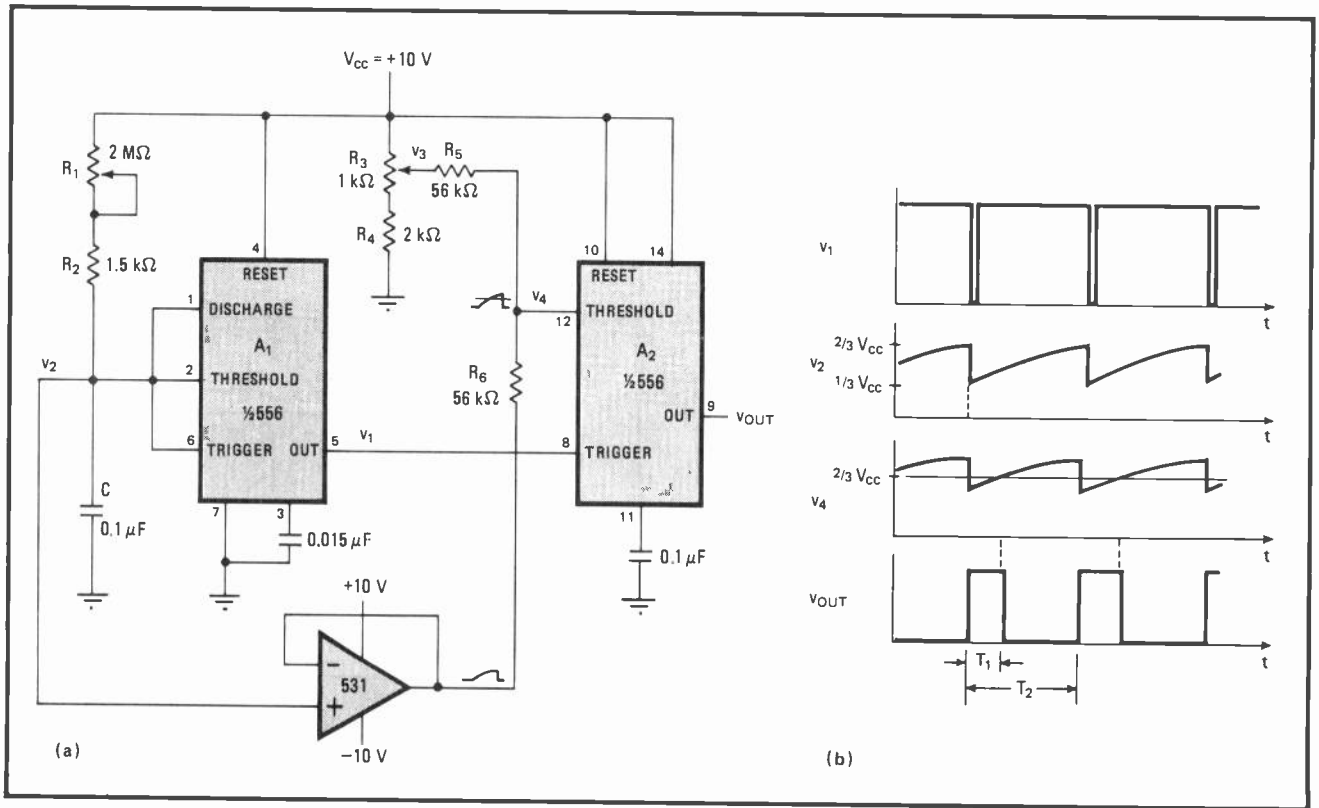
The duty cycle in this timer is determined not by external resistance-capacitance elements, but by the voltage on the threshold port. The output of A_2 will remain high if the threshold voltage stays below two thirds of the supply voltage, V_{cc}. This circuit can generate a dc offset voltage at the port to modify the threshold-switching time.

The voltage at the threshold port is determined by the two input voltages, v_2 and v_3, at the summing junction. Thus:

$$v_4 = v_2\left(\frac{R_5}{R_5+R_6}\right) + v_3\left(\frac{R_6}{R_5+R_6}\right)$$

Voltage v_2 is an exponential ramp resulting from charging C through resistances R_1 and R_2. The boundaries of the signal, determined by the internal comparators of A_1, lie between $\frac{1}{3}\ V_{cc}$ and $\frac{2}{3}\ V_{cc}$.

The 531 op amp is a buffer for the high-impedance A_2 signal and prevents current from flowing into the timing port, which could charge C from V_{cc} through R_5 and R_6. Dc voltage v_3 can be varied from $\frac{2}{3}\ V_{cc}$ to V_{cc}. Thus it can be seen that R_3 will determine how large a dc voltage is superimposed on v_2, thereby controlling the duty cycle. Since there are no feedback loops linking A_1 and A_2, it is clear that frequency and duty cycle adjustments are independent. □



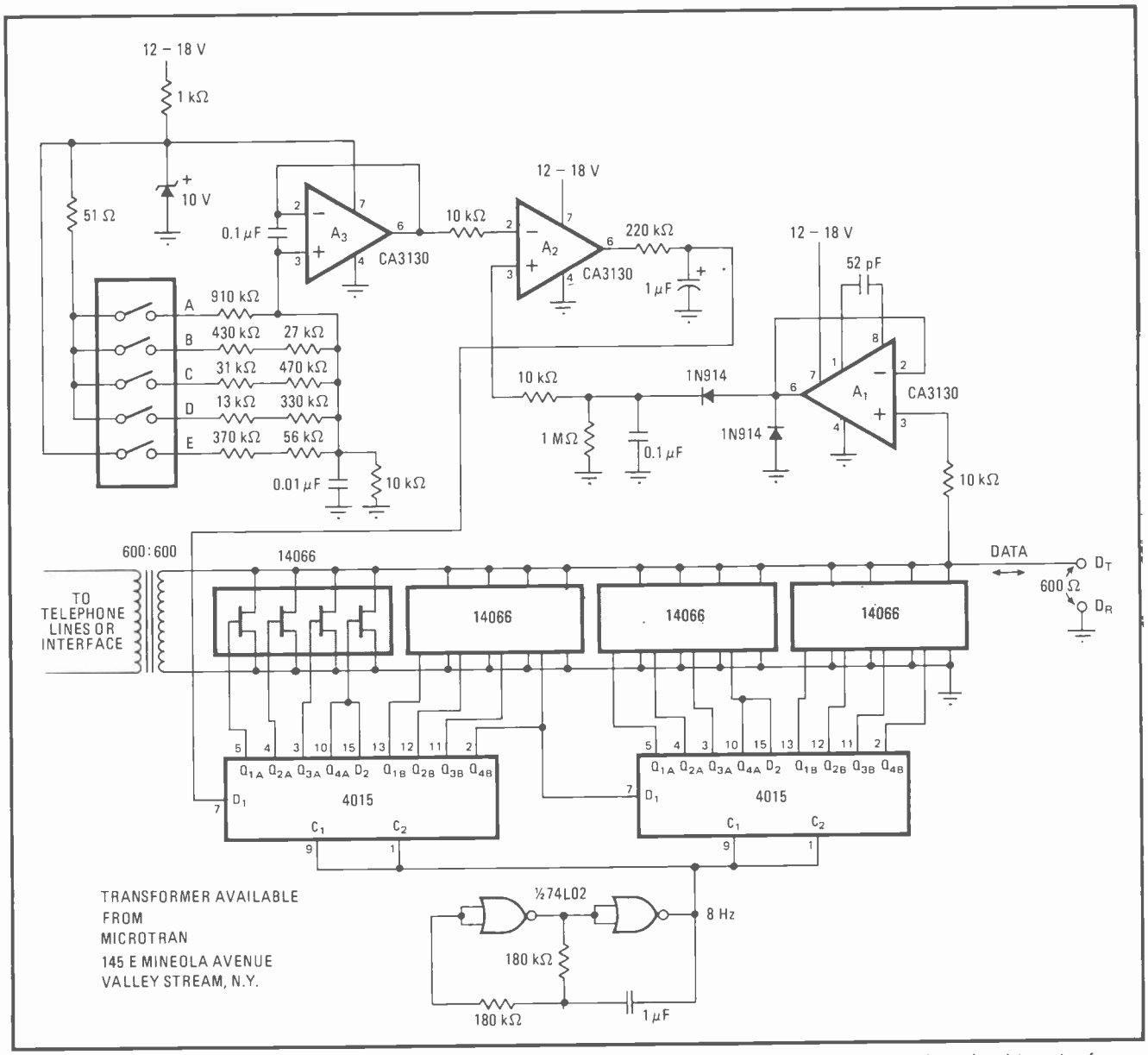
No relation. A_1 runs at frequency set by R_1. But duty cycle is selected by R_3, which controls signal offset at threshold port of A_2. No feedback loops link A_1 and A_2, thereby ensuring independent adjustment of rep rate and duty cycle. Timing diagram details operation.

Adjustable limiter controls telephone-line signal power

by Tom Hilleary
HMS Corp., Shawnee Mission, Kansas

To minimize crosstalk and other unwanted line radiation on telephone lines, it is often necessary to limit the input power of the data or voice signals, and to do so without amplitude distortion. This circuit does so by using two shift registers to monitor the relation of a set reference to the input signal amplitude (which is directly proportional to power at constant line impedance) and then divert some input current from the line transformer's primary winding whenever necessary. The limiter is effective when used with any constant-current data source. It provides 0 to −12 dBm of limiting and is accurately adjustable to 1 dB.

As shown in the figure, data or voice signals having a maximum amplitude of 1.4 volts at 0 dBm are applied to operational amplifier A_1. The output of A_1 in turn feeds



Digital limiter. Circuit provides 0 to −12 dBm of signal attenuation. Relative amplitude of constant-current data signal to set reference determines number of logic 1s generated by A_2 into 4015 registers over a given time. Signal above threshold loads more 1s into register, turning on more transmission gates as register is clocked and thus diverting the input current away from the primary winding.

the noninverting input of comparator A_2. The desired limiting (reference) level is set by five switches, operated in accordance with the table. A_3 is a voltage follower and passes the reference voltage to the inverting input of A_2.

A_2 compares the peak value of the input signal to the reference and when the reference voltage is exceeded generates a logic 1 for the data input of two 8-bit 4015 shift registers. The 4015s are configured as a single 16-bit device that is clocked at an arbitrary 8-hertz rate. If the input signal is mostly larger in amplitude than the reference, the shift register is periodically loaded with more 1s. Conversely, low-amplitude signals introduce more logic 0 signals into the register.

Thus, as the signal power rises above the value desired, more register outputs are activated and themselves activate more of the 14066 transmission gates, each of which when switched on places approximately 100 ohms across the transformer winding. As a result, more of the input current is diverted through these shunt paths, limiting the current though the transformer's primary and the induced voltage in its secondary. If the signal power drops, the shunts are in essence removed, allowing more of the signal to pass. Either way, the current output is constant, so that the effective line impedance as seen by the data source does not change.

DIGITAL LIMITER

D_T PEAK LEVEL (dBm)	CLOSE SWITCHES				
	A	B	C	D	E
0					
−1					
−2					
−3					
−4					
−5					
−6					
−7					
−8					
−9					
−10					
−11					
−12					

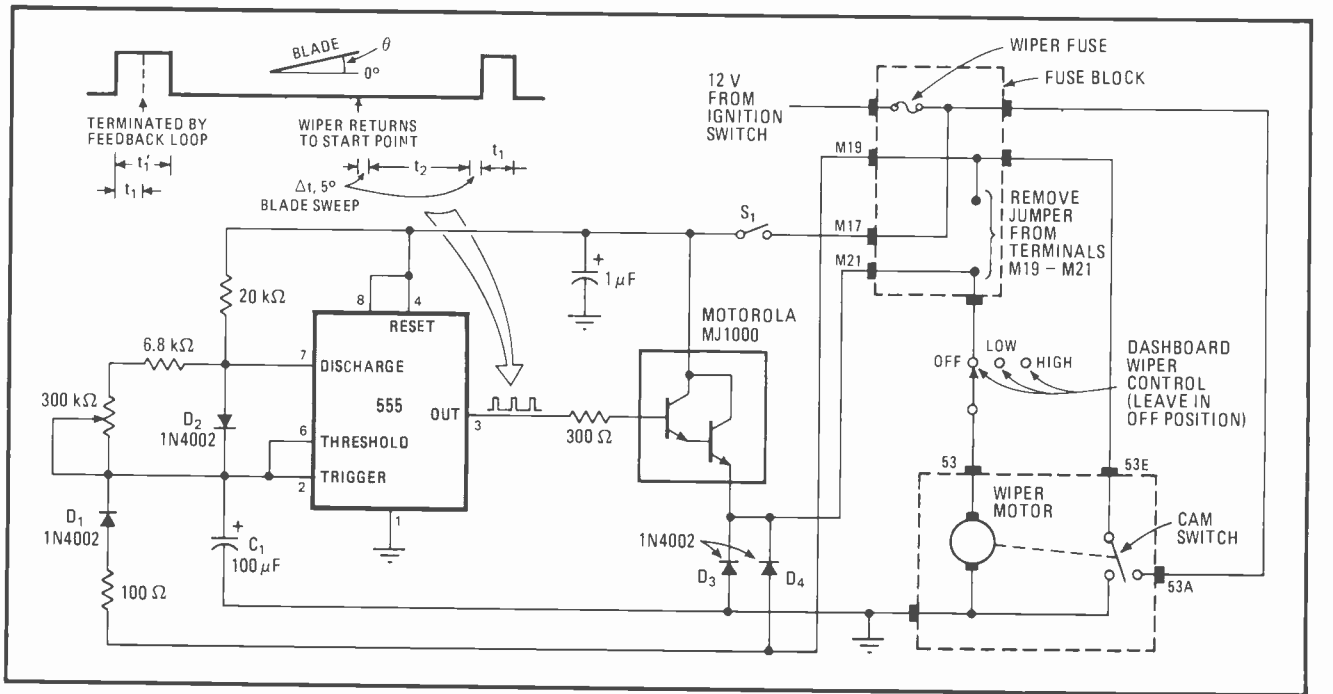
The sampling rate and the RC integrator following A_2 between them control the circuit's response time. Either or both may be altered for a specific application. □

Synchronous timing loop controls windshield wiper delay

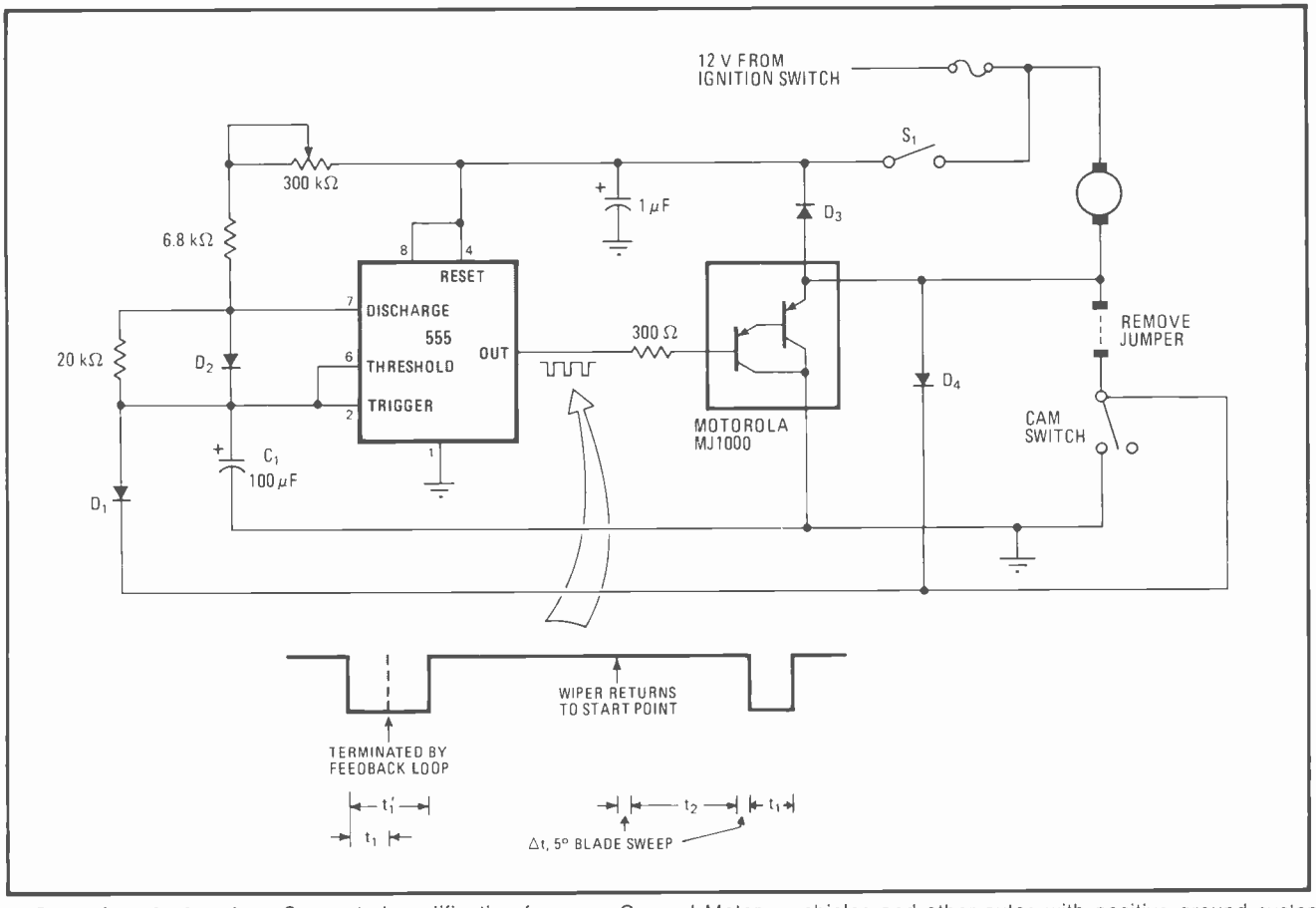
by John Okolowicz
Honeywell Inc., Fort Washington, Pa.

A 555 timer can control an auto's windshield-wiping rate by providing a selectable delay time between wipes. The timer uses a feedback signal from the cam-operated switch within the wiper motor to synchronize the delay time to the position of the wiper blades, as measured from their starting point.

With synchronization, the minimum delay time can still be reliably kept to nearly zero (normal delay for



1. Wipe-rate selection. Control over the time between sweeps in negative-ground windshield wiper systems is done by the 555 and a synchronous feedback loop. Delay time can be varied from 0 to 22 seconds. Synchronizing the feedback to the wiper blades' position ensures that sweep rate will be independent of variations in wiper speed. Terminal block notations are for Volkswagen Rabbit.



2. Ground-contact system. Suggested modification for many General Motors vechicles and other autos with positive-ground system uses same number of components as standard system. Wiper motor is energized by completing ground connection. Note that diodes D_1, D_3, and D_4 are reversed with respect to the polarities shown in Fig. 1 and that pulse-train polarity from 555 output is inverted.

standard systems), which is best for heavy rain. In addition, it ensures that the delay time is independent of the wiper speed across the windshield. Further, the maximum delay time in this circuit can be set to about 22 seconds, which is suitable for mist or light drizzle, or to any value desired, by suitable selection of the 555's timing components. This circuit offers a better approach to synchronous-delay wipers than those that use silicon controlled rectifiers in parallel with the cam switch, because cam-switch voltage is affected by dirt and grease.

The circuit shown in Fig. 1 is for a Volkswagen Rabbit, but it can be used in any car that has one end of the wiper motor always grounded (which requires a positive energizing voltage). As shown, the 555 assumes the high state on power-up (S_1 initialized), driving the MJ1000 Darlington amplifier, which in turn energizes the wiper motor. As the blades traverse through an angle of approximately 5°, the cam switch is engaged to the 12-volt ignition-line voltage. Thus a feedback voltage is presented to the trigger threshold port of the 555 through D_1. This voltage exceeds two thirds of the supply voltage on the 555; as a result, the output voltage at pin 3 falls at time t_1, which is less than the normal pulse width time usually controlled by the 20-kilohm resistor and C_1.

Normally, C_1 would now begin to charge, but because the voltage supplied to the cam switch remains high, the 555 simply sits in the low state. Meanwhile, both wiper blades reach the far end of their sweep and begin to move back toward their starting position.

As the blades approach within 5° of their starting point, the cam switch disengages from the ignition voltage and moves back to ground. Now C_1 begins its slow discharge through the 300-kΩ potentiometer. Note that t_2, the delay, is measured from the time the wiper moves within 5° to the time the 555 fires again. Triggering occurs once C_1 discharges to less than one third of the supply voltage.

D_1 prevents C_1 from discharging through the cam switch, and D_2 allows independent selection of times t_1 and t_2. D_3 provides suppression of the back voltage produced when the MJ1000 turns off; without the diode, the 555 will be retriggered falsely. D_4 allows normal operation when the circuit is not activated and also prevents the MJ1000 from shorting to ground through the cam switch.

Some cars have a reversed wiper-motor configuration. Thus one end of the wiper motor is always connected to the positive ignition-line voltage and so requires a connection to ground to energize it. Figure 2 shows a suggested modification of the wiper-delay circuit to handle such cases. □

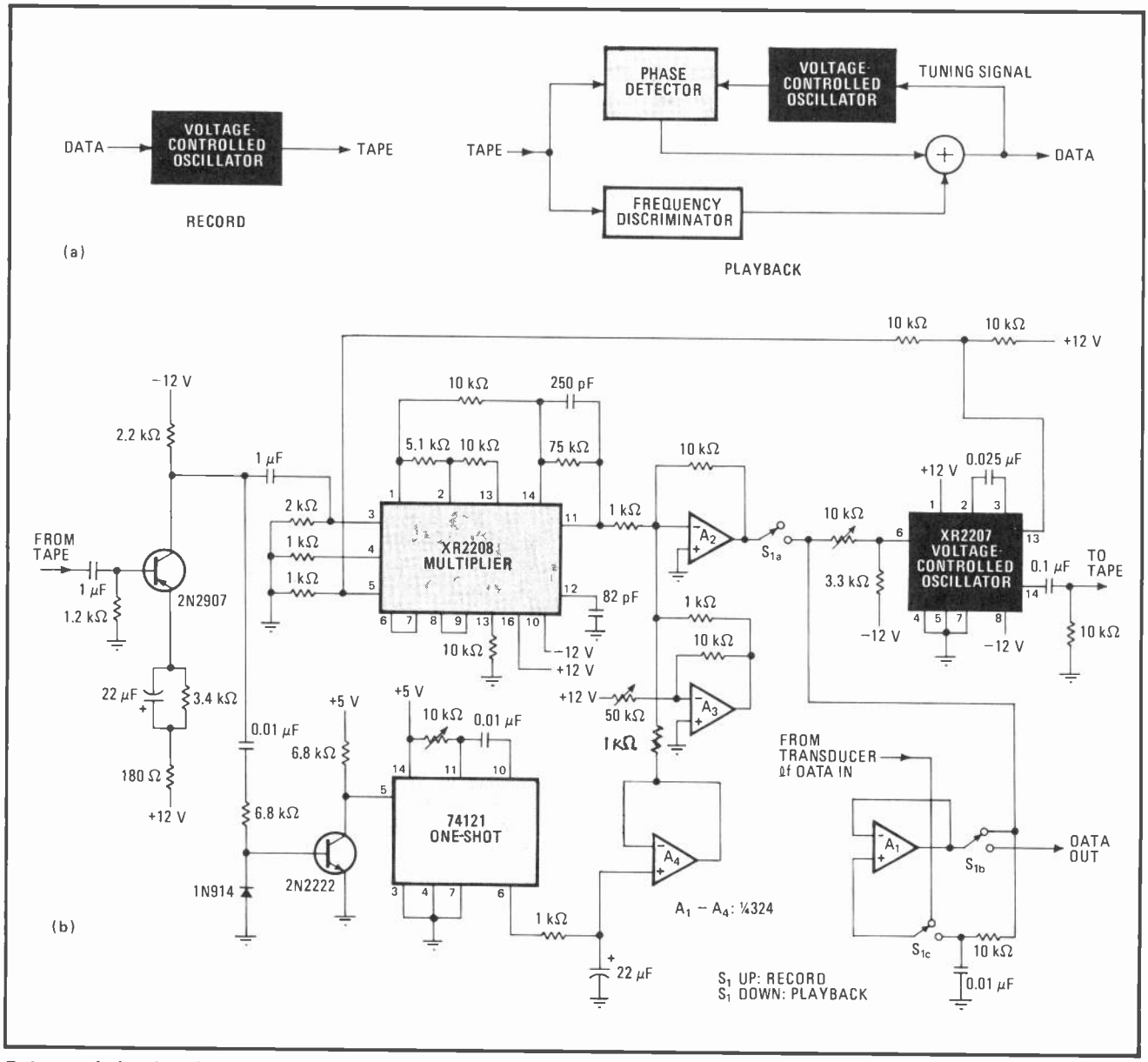
Frequency modulator extends tape recorder's lf response

by W. B. Warren and W. L. Lively
TRW Subsea Petroleum Systems Inc., Houston, Texas

Tape recorders used in low-frequency data acquisition systems are, not surprisingly, expensive. But this simple frequency-modulator circuit extends to dc the effective low-frequency response of any inexpensive tape recorder. To do this, the modulator translates a low-frequency data signal to a frequency falling within the recorder's limits, thus ensuring that the data will be properly recorded.

The block diagram in Fig. 1a illustrates the operation of the circuit. Recording low-frequency data simply requires that the frequency of a voltage-controlled oscillator be varied by the amplitude of a low-frequency input signal. On playback, the recorded data can be recovered by a phase-locked-loop demodulator, which is formed by a phase detector, frequency discriminator, and the VCO that was used to record the original data.

The circuit is shown in Fig. 1b. In the record mode,



Data translation. Low-frequency data may be recorded on an inexpensive tape recorder if the signal is first modulated to a higher frequency. Signal is recovered from recorder by demodulation, using same VCO (a). Modulator uses four chips and two transistors (b).

data signals are introduced to amplifier A_1, which in turn drives the Exar XR2207 VCO. A 0-to-10-volt data signal will vary the VCO frequency from 10 to 5 kilohertz so that the corresponding frequencies can be recorded.

On playback, the recorded data is presented to the 2N2907 buffer, then introduced to one input port (pin 3) of the XR2208 multiplier, which serves as a phase detector. Driving the other input port at pin 5 is the VCO. The output signal from the phase detector is the demodulated waveform produced by the multiplication of the playback signal times the output of the VCO.

The 74121 monostable multivibrator (one-shot) serves as a simple frequency discriminator, which drives the low-pass filter formed by the 1-kilohm resistor and the 22-micro-farad capacitor. The filter produces a voltage proportional to the frequency of the signal from the tape recorder. The addition of the discriminator to the circuit provides for rapid and reliable acquisition of the recorded data and reduces the dynamic range over which the phase-detector portion of the loop must operate.

The signals produced by the frequency discriminator and the phase detector are summed by A_2 through A_4 to generate the control voltage for the VCO. Therefore, the output signal, which is the control (tuning) voltage, is a dc voltage equal to that originally recorded. Using the same voltage-controlled oscillator for both record and playback modes ensures that VCO tuning nonlinearities have a negligible effect on system linearity.

The characteristics of the XR2207 are very stable with respect to supply-voltage and temperature variations. The primary sources of error between the record and playback signals will be those caused by tape stretch and the tape recorder's variations in speed. Both of these effects may be minimized by adjusting the potentiometer at pin 6 of the XR2207 to yield as large a frequency swing as possible for the range of signals being recorded. Better than 1% accuracy can be obtained with this circuit, even if an inexpensive tape recorder is used. □

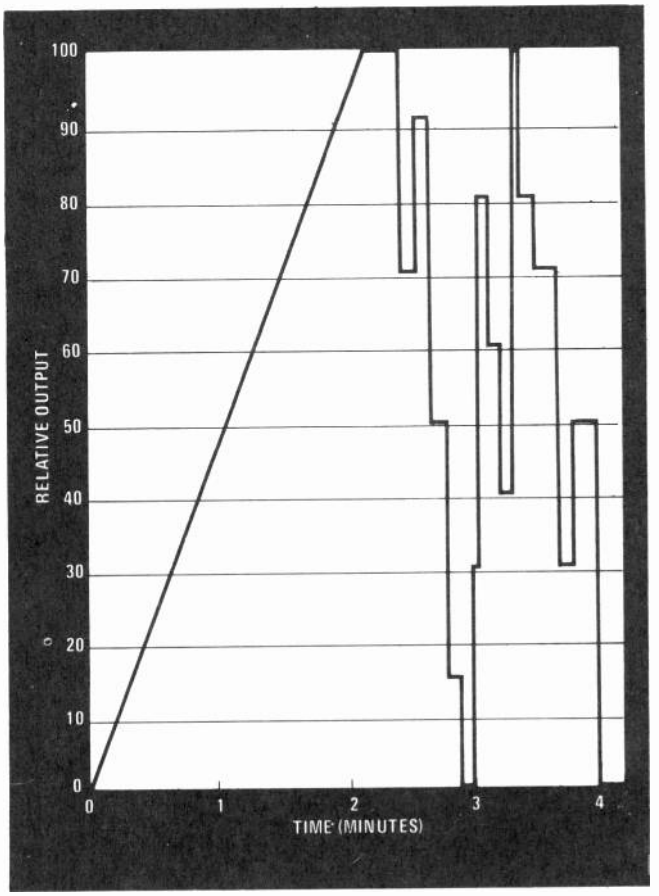
Programming a microcomputer for d-a conversion

by Richard T. Wang
Department of Zoology, University of Texas, Austin, Texas

If the speed of conversion is not an important consideration, a microcomputer can be used for digital-to-analog number conversion with the aid of this simple pulse-width modulation program. A resistance-capacitance filter and a latch, which may be connected to any one pin of the microcomputer's output ports, are the only items of microprocessor hardware required. Almost any strip-chart recorder can be used to record the filtered output voltage. Although intended for the plotting of bar graphs, histograms, and spectrograms from data stored in memory, the program needs only slight modification to be able to handle real-time data.

The program in the table was written for the Zilog Z-80 microcomputer system. All data for the graphs to be plotted is stored as an array in memory. The first two bytes of the array contain the number of data elements stored in the area labeled ARRAY. These bytes are loaded into registers B and C, which keep track of the number of bytes in ARRAY remaining to be sampled. The elements of ARRAY are loaded into register A and passed to a timing loop one at a time, where each will eventually be converted into an analog voltage.

The timing loop uses the alternate (primed) registers. Register B′ is loaded with a number (N) determined by the relationship N = PS/E, where E is the number of elements per inch recorded for a given chart speed (S) and output pulse rate (P) to the RC filter. B′ contains the number 192—the number of pulses per element (N) needed to ensure that 50 elements per in. are recorded for a given chart speed of 30 seconds/in., and a pulse rate of 320/s.



System response. Typical graph is accurately reproduced by Heath EU-205-11 strip-chart recorder. System linearity is confirmed with a ramp-test pattern, as shown on left. Right half shows a sample histogram. Total recording time is 4 minutes.

Register E′ is loaded with a selected value of 201, a number that is one greater than the largest number that may be plotted. E′ is decremented through a loop consisting of six instructions. A NOP instruction is included for timing compensation. When E′ equals the

contents of A, the state of the output is changed from a 0 to a 1 and begins to charge the capacitor in the RC filter. This continues until E′ decrements to zero. At this time the output returns to 0. E′ then returns to 201, and the process repeats until 192 pulses are generated for that element. The next element then undergoes an identical process until the entire array has been processed. The output pulse width (W_i) is related to the digital numbers (D_i) for a system clock at 2.5 megahertz by $W_i = 15.2 D_i$ where W_i is given in microseconds.

The critical timing in this program occurs between the START and TERM instructions. When the number to be converted is 1 (the smallest number that can be encoded), this instruction sequence takes 38 clock periods, or T states, exactly the same as that required by the START-TERM loop. The program is thus written so that multiples of 38T are added through the loop for numbers greater than 1, ensuring a linear relation of the output pulse width to the digital number stored.

With the output pulse rate of 320/s, an RC filter with a time constant equal to or greater than 3 milliseconds is sufficient to smooth the output voltage. To calibrate the system, the input to the chart recorder should be temporarily grounded, and its pen position should be set to zero. ARRAY is then filled with C8 (hexadecimal), the full-scale value, and the program is initiated. The recorder sensitivity control is then adjusted for a full-scale indication.

The figure shows a graph recorded on a Heath strip chart instrument. The ramp voltage is intended to display the system's linearity. □

Z-80 PULSE-WIDTH-MODULATION PROGRAM FOR DIGITAL-TO-ANALOG CONVERSION

```
LOC   OBJ CODE    STMT SOURCE STATEMENT

                     1 *H D/A CONVERSION
                     2 ; SUBROUTINE DAC: D TO A CONVERSION BY PULSE
                     3 ; WIDTH MODULATION.  THE GRAPH TO BE DISPLAYED
                     4 ; IS SET UP IN ARRAY. THE FIRST TWO BYTES
                     5 ; INDICATE THE LENGTH OF ARRAY.  ANY NUMBER
                     6 ; GREATER THAN FULL SCALE (200 DECIMAL) WILL
                     7 ; BE DISPLAYED AS ZERO.
                     8 ;
                     9 ARRAY    EQU 3000H     ;ADDRESS OF ARRAY
2800                10          ORG 2800H
2800  210030        11 DAC      LD HL,ARRAY   ;ADDRESS OF ARRAY IN HL
2803  4E            12          LD C,(HL)     ;FIRST TWO BYTES
2804  23            13          INC HL        ;  INDICATE LENGTH
2805  46            14          LD B,(HL)     ;     OF ARRAY
2806  23            15 DSLOOP   INC HL        ;DISPLAY LOOP
2807  7E            16          LD A,(HL)     ;NUMBER TO BE DISPLAYED
2808  D9            17          EXX           ;GET ALTERNATE REGISTERS
2809  06C0          18          LD B,192      ;REFRESH CYCLES
280B  0E01          19          LD C,01       ;OUTPUT PORT ADDRESS
280D  1620          20          LD D,100000B  ;BIT 5 AS OUTPUT PIN
280F  1EC9          21 SUBDAC   LD E,201      ;SET E TO MAXIMUM + 1
2811  1D            22 LOOP     DEC E         ;E AS TIMING COUNTER
2812  280B          23          JR Z,TERM     ;TO TERMINATE PULSE
2814  BB            24          CP E          ;A EQUALS TO E?
2815  2803          25          JR Z,START    ;IF YES, START PULSE
2817  00            26          NOP           ;TIMING COMPENSATION
2818  18F7          27          JR LOOP       ;LOOP IF NOT EQUAL
281A  ED51          28 START    OUT (C),D     ;START OUTPUT PULSE
281C  C31128        29          JP LOOP       ;CONTINUE LOOP
281F  ED59          30 TERM     OUT (C),E     ;TERMINATE PULSE
2821  10EC          31          DJNZ SUBDAC   ;REFRESH UNTIL B ZERO
2823  D9            32          EXX           ;GET BACK MAIN REGISTERS
2824  0B            33          DEC BC        ;END OF ARRAY?
2825  79            34          LD A,C
2826  B0            35          OR B
2827  20DD          36          JR NZ,DSLOOP  ;IF NOT, SHOW NEXT NUMBER
2829  C9            37          RET
                    38          END
```

C-MOS twin oscillator forms micropower metal detector

by Mark E. Anglin
Novar Electronics, Barberton, Ohio

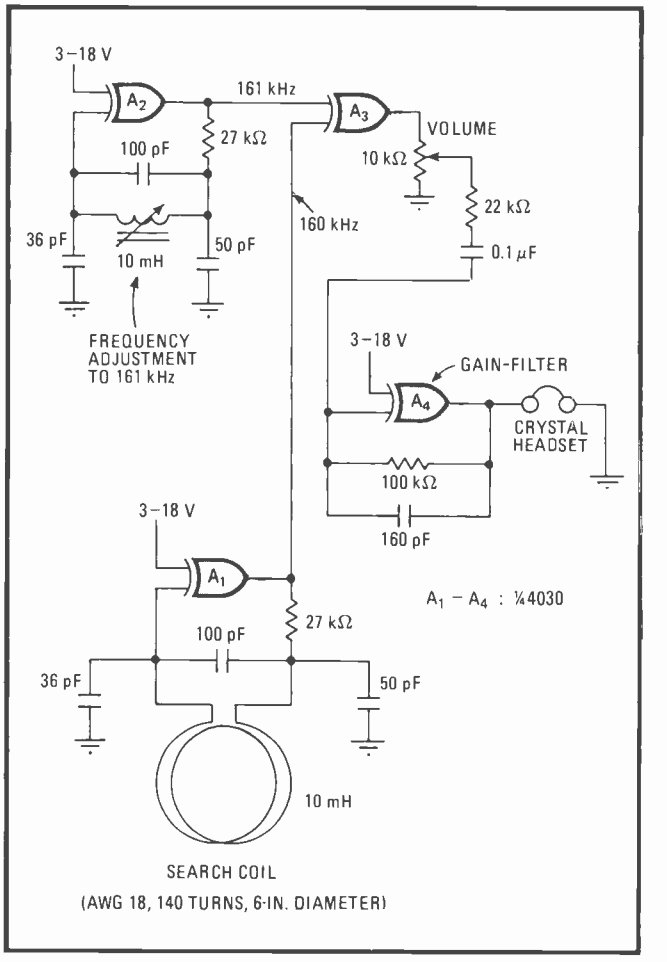
A battery-powered metal detector can be built with the four exclusive-OR gates contained in the 4030 complementary-metal-oxide-semiconductor integrated circuit. The gates are wired as a twin-oscillator circuit, and a search coil serves as the inductance element in one of the oscillators. When the coil is brought near metal, the resultant change in its effective inductance changes the oscillator's frequency.

Gates A_1 and A_2 in the figure are the active elements in the two simple oscillators, which are tuned to the fundamental frequencies of 160 and 161 kilohertz, respectively. A_1 serves as a variable oscillator containing the search coil, and A_2 oscillates at a constant frequency.

The pulses produced by each oscillator are mixed in A_3, and its output contains sum and difference frequencies at 1 and 321 kHz. The 321-kHz signal is filtered out easily by the 10-kHz low-pass filter at A_4, leaving the 1-kHz signal to be amplified for the crystal headset connected at the output. The headset has a high impedance (2,000 ohms) and therefore will not impose a big load on A_4.

A change in the output frequency indicates a frequency change in the variable oscillator due to the mutual-coupling effect between a metal and the search coil. The device's sensitivity, determined largely by the dimensions of the search coil, is sufficient to detect coin-sized objects a foot away.

This device's effectiveness derives from the twin-oscillator approach, because it is not feasible to directly vary a single oscillator operating at 1 kHz. An oscillator operating in this range requires high values of L and C, and these elements would load down the gate and consequently reduce circuit sensitivity. In addition, the cost of high-value inductors and capacitors is great. □



Metal detector. Two oscillators and a search coil form a simple metal detector. Objects near search coil change A_1's frequency of oscillation and the 1-kHz output note produced by the mixing of oscillators A_1 and A_2. A_4 amplifies and filters audio signal.

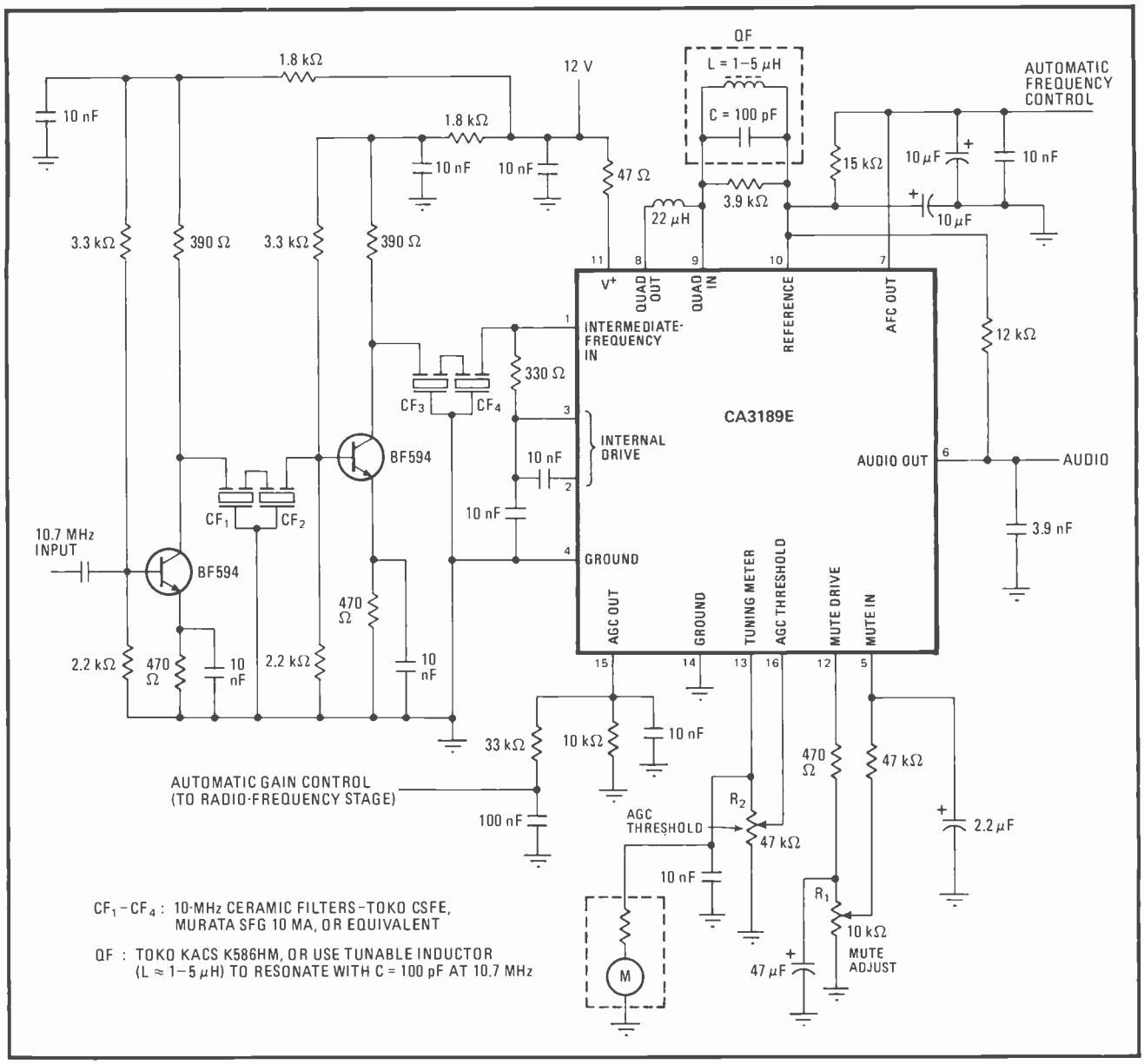
One-chip fm demodulator has improved response

by J. Brian Dance
North Worcestershire College, Worcs., England

Coupling a preamplifier that has good selectivity with the new RCA CA3189E demodulator chip builds a frequency-modulation detector that outperforms the well-known CA3089 fm/i-f system. The circuit described here provides greater rejection of input-signal noise and high amplitude-modulation signals than its predecessor, while ensuring better audio-channel muting. Also the automatic-gain-control threshold can vary.

Although the 3089 and the 3189 are similar, the external circuit shown in the figure differs considerably from the standard detector circuit used with the 3089. An input signal encounters four 10.7-megahertz ceramic filters ($CF_1 - CF_4$) and two transistors in the preamp, which provide the needed selectivity and gain to optimize the signal-to-noise ratio, even before the 3189 operates on the signal.

The bandwidth of the intermediate-frequency amplifiers in the 3189 is limited to 15 MHz, as opposed to 25 MHz in the 3089; but the narrower bandwidth



1. Improved fm detector. A good preamplifier and the CA3189 fm/i-f system provide optimum response. The circuit has greater noise immunity and better protection from a-m signal overload than detectors now used, and the agc threshold is selectable.

improves circuit stability and, if printed-circuit boards are used, makes layout less critical. More important, since the overall bandwidth is only slightly greater than the input frequency, less noise is produced in the frequency band of interest from intermodulation products caused by signals outside the band. Also, a specially constructed zener diode is employed in the regulator circuit of the 3189 to minimize noise.

Two muting circuits are used. For noise between stations, part of the voltage change appearing at the mute-drive port at pin 12 (which is driven by the noise from previous input stages) is fed to the mute-control input at pin 5 through a voltage divider that includes potentiometer R_1. The muting threshold can thus be selected.

Although this arrangement is satisfactory for interstation noise, additional components are needed to combat noise produced by tuning through a signal; otherwise, a sudden change in the output dc level will produce the familiar, low-frequency "thump" noise. An integrating circuit is formed by adding the 47- and 2.2-microfarad capacitors between pins 5 and 12 to reduce this noise, but even this step does not eliminate it if the integrating-circuit time constant is too small for fast tuning. However, the deviation-muting circuit formed by placing a resistor between pins 7 and 10 ensures the noise will be eliminated, provided the deviation is less than ±40 kilohertz. (The deviation is controlled by selecting a resistor of 15 kΩ.) Thus any voltage change caused by noise is reduced at the output, pin 6.

The agc threshold is determined by R_2, which sets the voltage fed to pin 16 from pin 13. The threshold point can be selected from 0.2 to over 200 millivolts. A 40-decibel agc range can be easily obtained if the very-high-frequency tuner driving the 3189 uses dual-gate metal-oxide-semiconductor field-effect-transistor stages or sim-

ilar stages having wide dynamic range.

The signal-to-noise ratio is 50 dB for a 3-microvolt input signal. If the first transistor stage in the preamp is omitted, a s/n value of 20 dB can be obtained for the same input level using only two ceramic filters. For a deviation of ±75 kHz, the a-m signal rejection is 60 dB for input signal amplitudes greater than 500 μV, and the limiting sensitivity of the 3189 is typically 12 μV at 3 dB. The tuning meter has an approximately logarithmic response over an input signal range of 10 μV to 100 mV.

The quadrature tuned circuit between pins 9 and 10 determines the percentage of audio harmonic distortion—typically 0.3%. This figure can be reduced to 0.1% if the network is a double-tuned circuit.

The 12-kilohm load resistor sets the audio output level. The 3.9-nanofarad capacitor provides the 50-microsecond de-emphasis required for reception in Region 1 (Europe), and a 5.6-nF capacitor is suitable for the 75-μs de-emphasis required in Region 2 (U. S.). This capacitor should be omitted when the signal is fed to a stereo decoder circuit. □

Keyboard programs the gain of an operational amplifier

by P. A. Benedetti
LAFBIC-CNR, Pisa, Italy

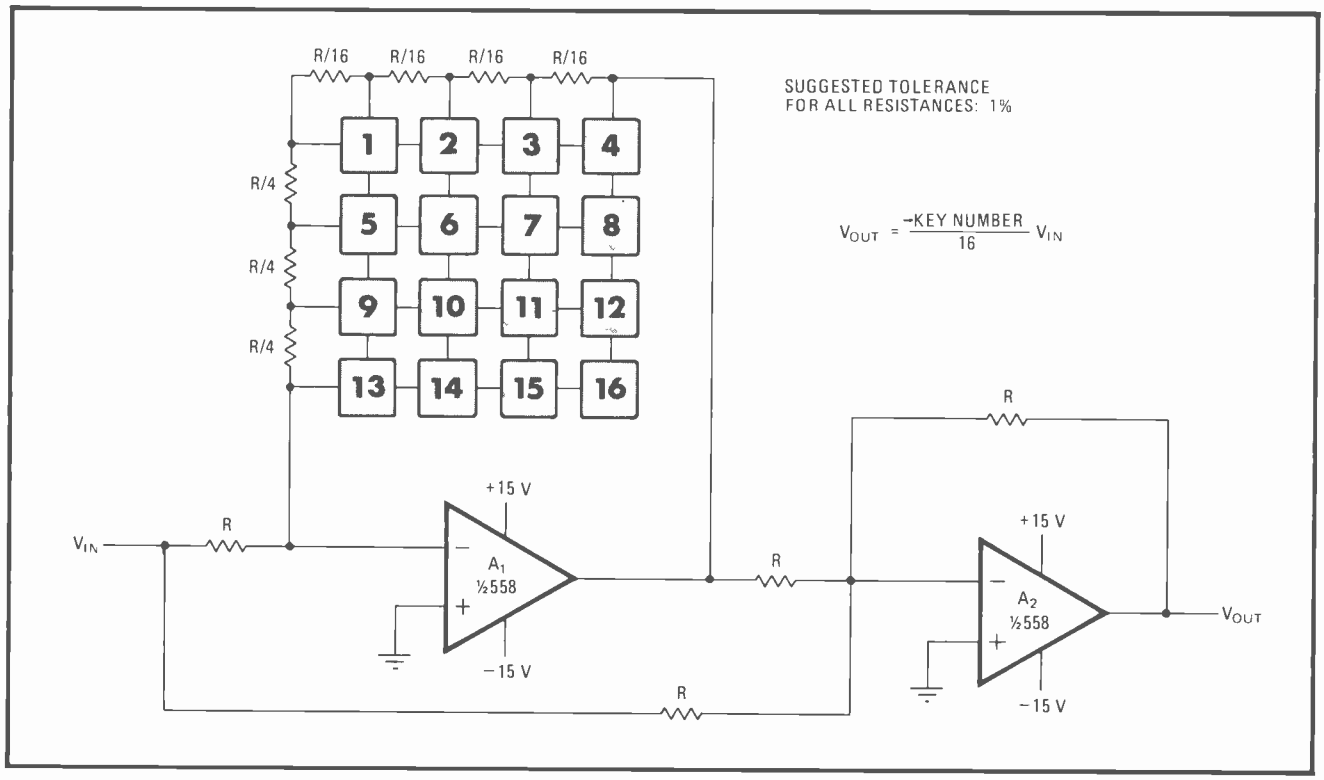
Placing a standard keyboard and a few precision resistors in the feedback loop of an operational amplifier produces a handy gain-programmable amp, useful for generating any one of several equally spaced voltages at the push of a button. Applications vary from testing components to controlling a computer program that employs an analog-input channel.

As the figure indicates, depressing 1 of 16 keys on the normally open contacts of the keyboard selects the value of the feedback resistor placed across the 558 operational amplifier A_1, to which a fixed input voltage V_{in} has been applied. A_1's gain varies with feedback resistance, of course, and so the output voltage also varies and assumes 1 of 17 equally spaced values (including 0), depending on which button has been depressed. The resistance values in the feedback loop have been selected so that the output voltage at A_2 is:

$$V_{out} = -\left[\frac{\text{Key number depressed}}{16}\right] V_{in}$$

As might be expected, the programmable-gain principle applies to a keyboard of any size. Resistor precision must vary accordingly, however, becoming greater as the number of keys increase.

Key-bounce effects are not a problem except in some computer-based applications. A solution is to include double-testing of contact points in the software. □



Digital control A standard keyboard and a few precision resistors in op amp's feedback circuit generate an output voltage proportional to the number on the key depressed. Circuit applications vary from component testing to analog-voltage control of computer systems.

PROM converts weather data for wind-chill index display

by Vernon R. Clark
Applied Automation Inc., Bartlesville, Okla.

A programmable read-only memory and four arithmetic/logic units can convert air-temperature and wind-speed data in real time into wind-chill temperature, which is displayed on a direct numerical readout.

The wind-chill equation adopted by the National Weather Service is:

$$H = (100w^{1/2} + 10.45 - w)(33 - T_a)$$

where H is the heat loss in kilogram-calories per square meters per hour, w is the wind speed in meters per second, and T_a is the actual air temperature in °C. A modified form of this equation is the basis for the well-known wind-chill temperature chart issued by the service. In this circuit, the PROM is programmed so that, in combination with the arithmetic/logic units, it will generate output values identical to those in the chart for a wide range of air temperatures and wind speeds.

Basically, the circuit determines from the incoming data the apparent temperature change (T_c) caused by the wind. Then, it adds or subtracts T_c from T_a to find the equivalent temperature (T_e).

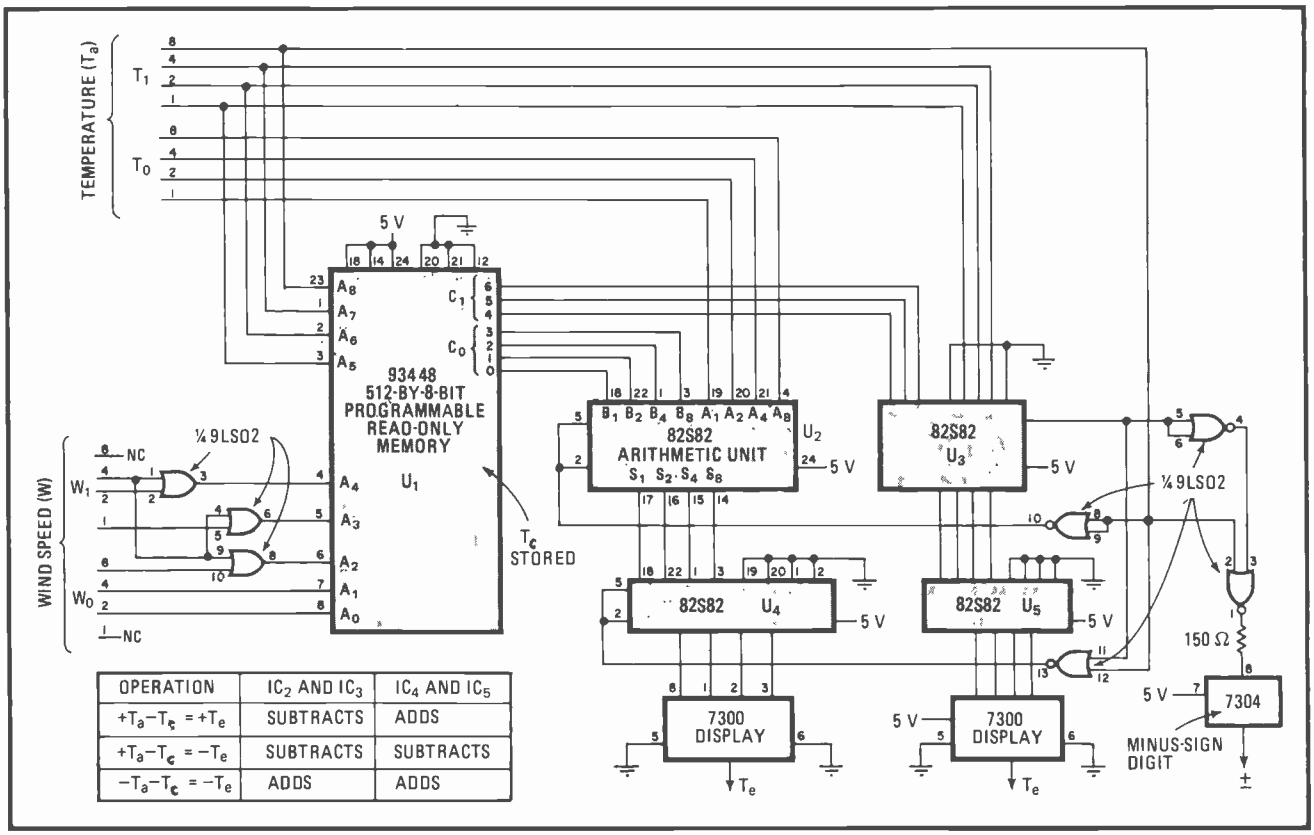
The T_c values are programmed into the PROM for all combinations of air temperature and wind speed over the range:

$$-60F \leq T_a \leq 50F \text{ (10 increments)}$$
$$0 \leq w \leq 46 \text{ miles per hour (2 mph increments)}.$$

The circuit must relate each T_a and w to each T_c to find the equivalent temperature.

As shown in the figure, each T_c may be accessed by introducing air-temperature and wind data, in binary-coded-decimal form, to the PROM (U_1) address lines. The actual values of T_c programmed in the PROM are shown in the table.

The value of T_c appearing at the output, for a given T_a and w, is introduced to two ALUs, U_2 and U_3. Also driving U_2 and U_3 is the T_a data. The ALUs compute the magnitude and sign of T_e by adding T_a and T_c. U_4 and U_5 perform a 10's complement operation in order to drive the 7300 displays properly. The operation of all four ALUs is summarized in the figure.



OPERATION	IC_2 AND IC_3	IC_4 AND IC_5
$+T_a - T_c = +T_e$	SUBTRACTS	ADDS
$+T_a - T_c = -T_e$	SUBTRACTS	SUBTRACTS
$-T_a - T_c = -T_e$	ADDS	ADDS

Cold solution. Circuit determines and displays wind-chill temperature (T_e). Air temperature (T_a) and wind-speed data (w) address PROM lines to access apparent temperature change (T_c) brought about by given w at T_a. Arithmetic/logic units U_2 and U_3 add T_a and T_c to find T_e. U_4 and U_5 perform a 10's complement operation for the digital display units, for which they serve as an interface.

PROM CONTENTS – WIND-CHILL INDICATOR

LOC		LOC		LOC		LOC		LOC	
0000R	0002	0070R	2628	00E0R	0000	0150R	4750	01C0R	0004
0002R	0409	0072R	3030	00E2R	0000	0152R	5355	01C2R	0714
0004R	1500	0074R	3100	00E4R	0000	0154R	5700	01C4R	2500
0006R	0000	0076R	0000	00E6R	0000	0156R	0000	01C6R	0000
0008R	2125	0078R	3233	00E8R	0000	0158R	5960	01C8R	3543
000AR	2933	007AR	3434	00EAR	0000	015AR	6162	01CAR	5055
000CR	3700	007CR	3637	00ECR	0000	015CR	6365	01CCR	6000
000ER	0000	007ER	3738	00EER	0000	015ER	6667	01CER	0000
0010R	3941	0080R	0001	00F0R	0000	0160R	0003	01D0R	6468
0012R	4344	0082R	0205	00F2R	0000	0162R	0511	01D2R	7275
0014R	4600	0084R	0900	00F4R	0000	0164R	2000	01D4R	7800
0016R	0000	0086R	0000	00F6R	0000	0166R	0000	01D6R	0000
0018R	4849	0088R	1215	00F8R	0000	0168R	2834	01D8R	8082
001AR	5051	008AR	1719	00FAR	0000	016AR	4044	01DAR	8485
001CR	5354	008CR	2100	00FCR	0000	016CR	4800	01DCR	8890
001ER	5556	008ER	0000	00FER	0000	016ER	0000	01DER	9294
0020R	0002	0090R	2223	0100R	0002	0170R	5255	01E0R	0000
0022R	0407	0092R	2425	0102R	0409	0172R	5759	01E2R	0000
0024R	1300	0094R	2600	0104R	1500	0174R	6200	01E4R	0000
0026R	0000	0096R	0000	0106R	0000	0176R	0000	01E6R	0000
0028R	1923	0098R	2728	0108R	2125	0178R	6466	01E8R	0000
002AR	2730	009AR	2929	010AR	2933	017AR	6768	01EAR	0000
002CR	3300	009CR	3031	010CR	3700	017CR	7071	01ECR	0000
002ER	0000	009ER	3132	010ER	0000	017ER	7273	01EER	0000
0030R	3537	00A0R	0000	0110R	3941	0180R	0004	01F0R	0000
0032R	3840	00A2R	0203	0112R	4344	0182R	0612	01F2R	0000
0034R	4200	00A4R	0700	0114R	4600	0184R	2200	01F4R	0000
0036R	0000	00A6R	0000	0116R	0000	0186R	0000	01F6R	0000
0038R	4343	00A8R	1012	0118R	4849	0188R	3036	01F8R	0000
003AR	4445	00AAR	1415	011AR	5051	018AR	4247	01FAR	0000
003CR	4749	00ACR	1700	011CR	5354	018CR	5200	01FCR	0000
003ER	5051	00AER	0000	011ER	5556	018ER	0000	01FER	0000
0040R	0002	00B0R	1818	0120R	0002	0190R	5660	0200R	
0042R	0407	00B2R	1920	0122R	0409	0192R	6365		
0044R	1200	00B4R	2100	0124R	1700	0194R	6700		
0046R	0000	00B6R	0000	0126R	0000	0196R	0000		
0048R	1620	0088R	2222	0128R	2329	0198R	6971		
004AR	2426	00BAR	2323	012AR	3337	019AR	7374		
004CR	2800	00BCR	2425	012CR	4100	019CR	7677		
004ER	0000	00BER	2526	012ER	0000	019ER	7879		
0050R	3032	00C0R	0000	0130R	4346	01A0R	0004		
0052R	3436	00C2R	0000	0132R	4850	01A2R	0613		
0054R	3700	00C4R	0000	0134R	5200	01A4R	2300		
0056R	0000	00C6R	0000	0136R	0000	01A6R	0000		
0058R	3839	00C8R	0000	0138R	5354	01A8R	3340		
005AR	4040	00CAR	0000	013AR	5657	01AAR	4652		
005CR	4142	00CCR	0000	013CR	5960	01ACR	5600		
005ER	4243	00CER	0000	013ER	6162	01AER	0000		
0060R	0002	00D0R	0000	0140R	0002	01B0R	6064		
0062R	0306	00D2R	0000	0142R	0510	01B2R	6770		
0064R	1000	00D4R	0000	0144R	1800	01B4R	7300		
0066R	0000	00D6R	0000	0146R	0000	01B6R	0000		
0068R	1418	00D8R	0000	0148R	2632	01B8R	7577		
006AR	2022	00DAR	0000	014AR	3640	01BAR	7980		
006CR	2400	00DCR	0000	014CR	4400	01BCR	8283		
006ER	0000	00DER	0000	014ER	0000	01BER	8485		

Wind speed frequently varies over a wide range in a short time. This may cause rapid flickering of the display and make it hard to determine the average wind-chill temperature. One answer to this problem is to sample the input data periodically. Another is to use average-value sensor circuits for smoothing the data. □

RAM and d-a converter form complex-waveform generator

by William A. Palm and G. A. Williamson
Magnetic Peripherals Inc., Minneapolis, Minn.

□ A random-access memory and digital-to-analog converter are at the heart of a programmable waveform generator that will produce almost any wave, however complex, at low frequency. It is only necessary to determine the digital equivalent of the desired wave and store that in a 256-word-by-8-bit RAM, for later transformation into an analog output voltage by the d-a converter.

The maximum repetition rate of the signals produced

is only 7.8 kilohertz, being limited by the RAM's access speed and the number of locations; but more often than not, a complex wave is required only in very-low-speed applications. If higher speed is desired, the use of emitter-coupled-logic RAMs will increase the repetition rate to nearly 400 kHz, on the assumption that a high-frequency clock is available.

As shown in the figure, binary-coded-decimal thumbwheel switches S_1-S_3 are used to address one of 256 RAM locations, and S_4 and S_5 select one of 256 waveform amplitudes (over the range 0 – 255 in base 2). Thus each location can be stored with an amplitude that can be resolved to 1 bit in 256.

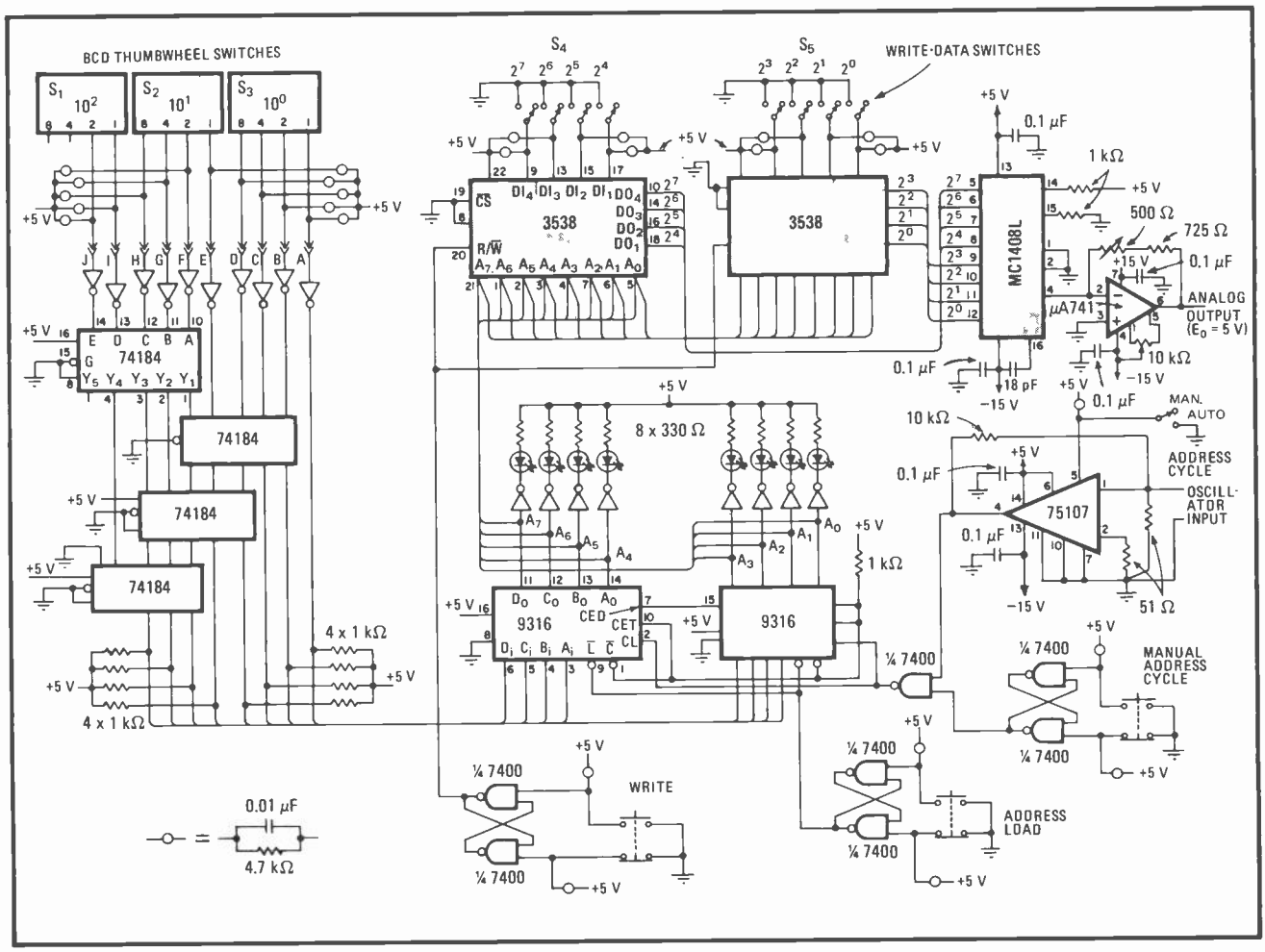
When each location of the RAM is stepped (at a maximum rate equal to the system clock frequency divided by the number of locations), its output at any given instant is in essence converted to one point in a 256-by-256 matrix. The RAM is formed by two 256-word-by-4-bit Fairchild 3538 devices.

Four 74184 BCD-to-binary counters, two 9316 4-bit counters, a 75107 line receiver, and several gates and switches make up the binary address counter. The 75107 allows flexibility in choice of the clock that addresses the RAM—almost any driving signal will do, whether a sine wave, ramp, pulse, or square wave. The address counter either may be single-stepped manually to the desired location (needed when loading the RAM) or cycled continuously when the desired waveform is generated.

Two momentary-contact switches perform the actual address-loading and data-writing operations, and the address at any given time is displayed by eight light-emitting diodes. The maximum clock frequency permitted is limited to 2 megahertz by the slow response of the RAM, and therefore the repetition rate of the output waveform is 2 MHz/256 = 7.8 kHz.

Storing 256 numbers is a tedious task, especially if it must be done often. In cases where a given waveform is needed frequently, consideration should be given to storing it permanently in a nonvolatile read-only memory. The ROM could be substituted for the RAM in this circuit.

When cycled, the output of each RAM location is converted into a current by the MC1408 d-a converter. This is then transformed into an analog voltage by the 741 operational amplifier. □



Simple storage of complex waveshapes. Programmable generator is capable of producing almost any complex low-frequency waveform. Once the digital equivalent numbers of the waveform are determined, they are stored in the 3538 random-access memories. The MC1408 digital-to-analog converter transforms the random-access memory's contents into the desired analog waveform.

Split current source damps reactive load oscillations

by Yishay Netzer
Haifa, Israel

A standard bilateral current source of the type shown in the first part of the figure (a) will often generate oscillations in circuit loads that are grounded and have an impedance (Z_L) that is not purely resistive. Inductive loads such as cathode-ray-tube deflection yokes and torque motors are best driven by the modified circuit shown in the second part of the figure (b). Adding the differential amplifier and feedback network to the circuit eliminates undesirable responses while ensuring that the output current will be virtually independent of the load impedance.

When the load is reactive, it may cause the circuit's step response to be underdamped and consequently unstable, with the result that the output current will become dependent on the load impedance. As shown in the equation in (a), the output current is dependent on the circuit transfer function, which is:

$$G(s) = K\frac{\omega_o^2}{s^2 + 2\zeta\omega_o s + w_o^2}$$

where ω_o is the natural undamped frequency of the circuit, K is a constant, and ζ is the damping factor.

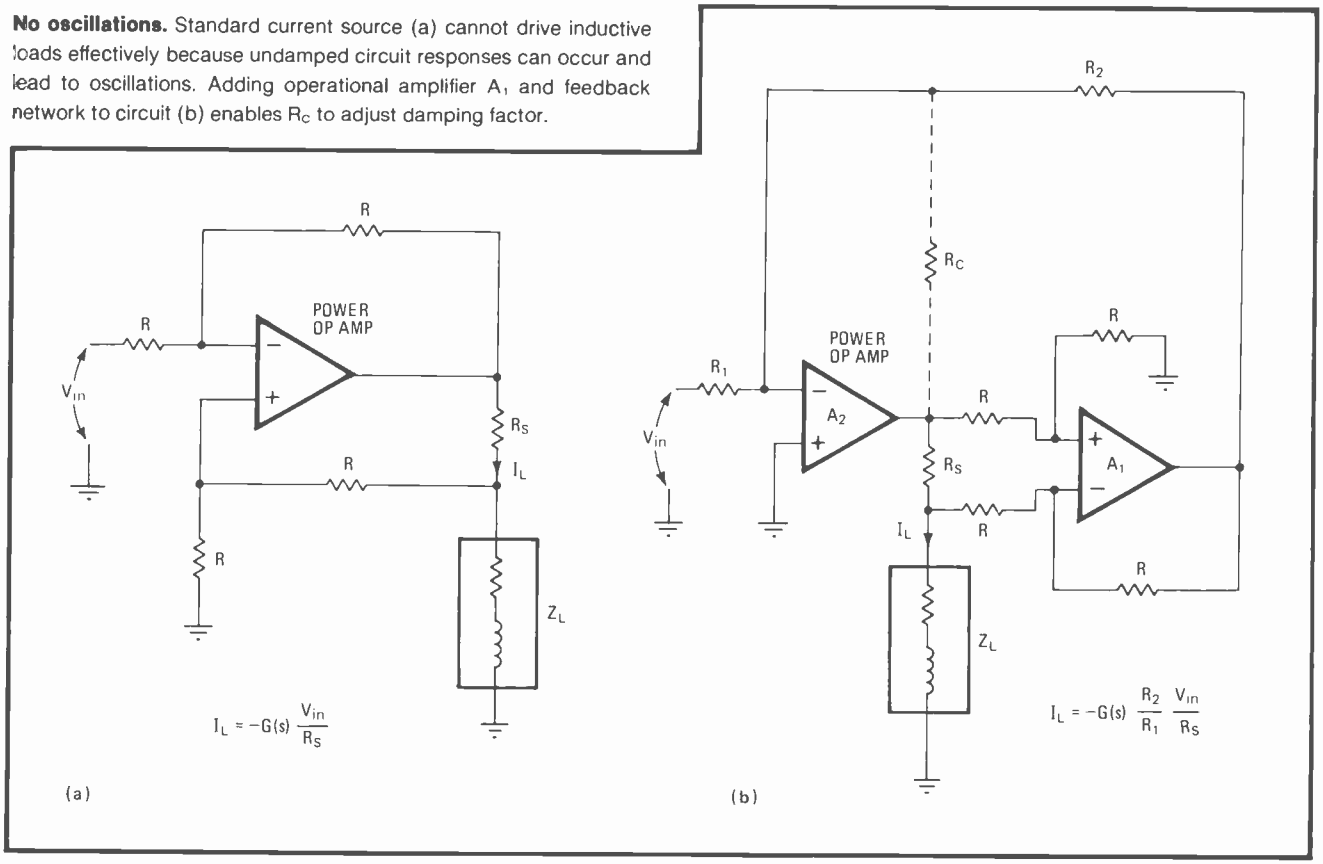
The various parameters are determined by circuit constants R, R_S, and Z_L. Of particular importance is the fact that once determined by the circuit configuration, ζ cannot be modified, and that is why oscillations can result. Furthermore, the oscillations may be impossible to eliminate in the standard circuit because adding components may affect the output impedance, making any type of compensation impractical.

The circuit in (b) circumvents the problem by splitting the current source into two parts:

- A balanced difference amplifier (A_1), which converts the load current into a single-ended voltage feedback signal.
- A power amplifier (A_2), which, aside from assuming its original function, reduces the effect of Z_L upon I_L by making use of the feedback voltage.

Note that by adding the feedback network, resistor R_C has been introduced to the circuit, and therein lies the major advantage of this circuit. R_C can vary (compensate) ζ right down to its optimum value ($2^{1/2}$ in this case), without disturbing the proportional relation of V_{in} to I_L throughout the useful range of the circuit; that is, below ω_o. The basic transfer function of the circuit is not

No oscillations. Standard current source (a) cannot drive inductive loads effectively because undamped circuit responses can occur and lead to oscillations. Adding operational amplifier A_1 and feedback network to circuit (b) enables R_C to adjust damping factor.



altered by the modified configuration, either.

The value of R_C is best found experimentally while observing the circuit response to a square-wave input. Note that the constant, K, in G(s) will be slightly smaller than its original value because of the feedback currents through R_C. □

Exclusive-OR gate and flip-flops make half-integer divider

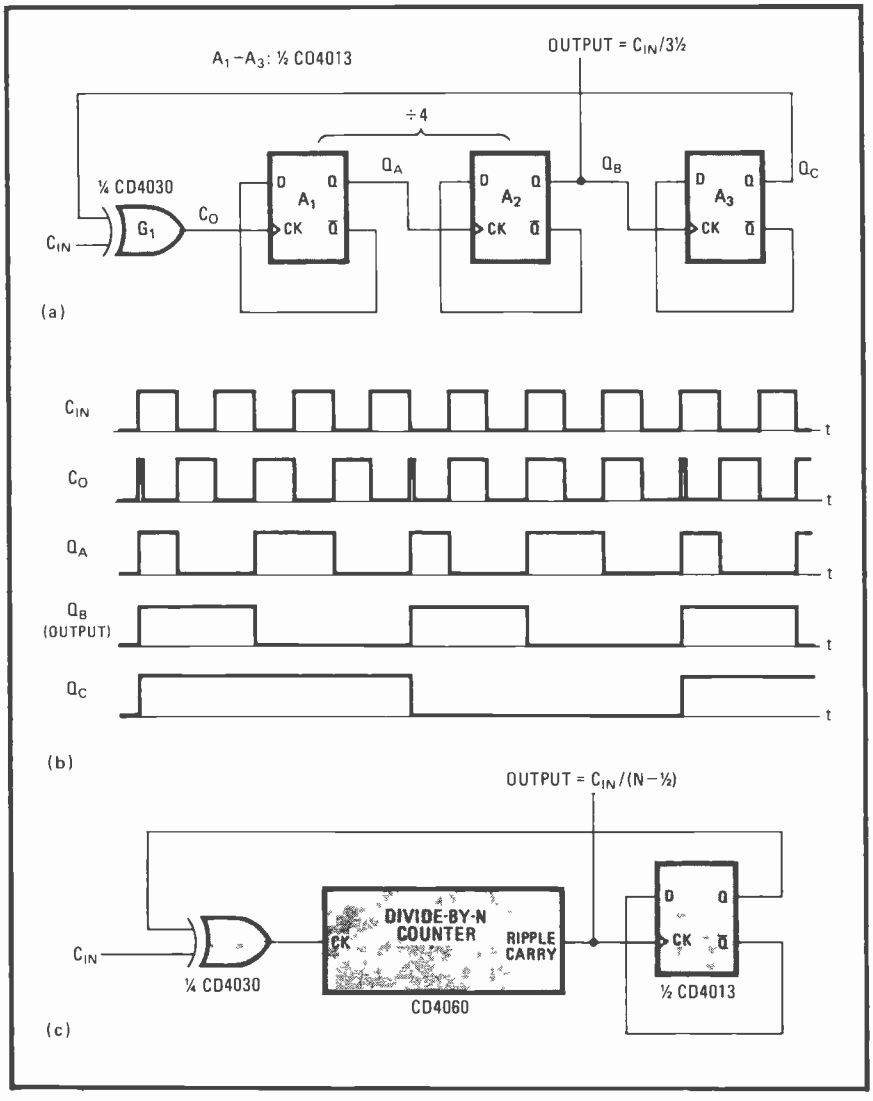
by Tung-sun Tung
University of Illinois, Urbana, Ill.

A simple and inexpensive divide-by-(N − ½) counter can be built with D flip-flops and an exclusive-OR gate. The circuit uses very few parts, largely because, unlike many such dividers, it does not rely on a collection of monostable multivibrators. Nor are there difficult timing considerations, which would also complicate the circuit and act to increase its parts count.

Various logic circuits need to be driven by what may be termed a half-integer clock signal that is derived from a master clock. For instance, the MM-57100 video-game integrated circuit is driven by a 1.0227-megahertz signal, which the chip's manufacturer (National Semiconductor Corp.) recommends be derived from the television set's 3.579545-MHz color-burst crystal oscillator. This application requires a divide-by-3½ counter, which may be built by modifying a divide-by-4 circuit as shown in Fig. 1a.

Flip-flops A_1 and A_2 form the divide-by-4 counter. The master clock, C_{IN}, drives A_1 through the exclusive-OR gate, G_1. However, the output state of G_1 is additionally controlled by A_3.

As a result, A_3 converts the divider to a divide-by-3½ counter. A_3 is situated in the feedback loop such that it enables generation of a short pulse at C_O for every 3½ counts of C_{IN}. The pulse is generated if C_{IN} either falls to logic 0 or rises to logic 1, which depends on the state of Q_C. Its shortness is due to the delay between the initial



Half-integer divider. Divide-by-3½ counter is divide-by-4 circuit modified by flip-flop A_3 and exclusive-OR gate G_1 (a). Timing diagram details operation (b). Method may be extended to form a divide-by-(N − ½) counter by replacing flip-flops A_1 and A_2 by ripple-carry, divide-by-N counter (c).

0-to-1 transition of C_O (caused by C_{IN}) and the change of state of Q_C—as Q_C changes state, it disables gate G_1, causing C_O to fall almost immediately after it has reached logic 1. The timing diagram given in Fig. 1b details circuit operation.

This method may be extended to the general case of the divide-by-$(N-\frac{1}{2})$ counter, as shown in Fig. 1c, simply by substituting a single synchronous or asynchronous counter for the flip-flops A_i that would otherwise be required. □

Dc-dc power supply regulates down to zero

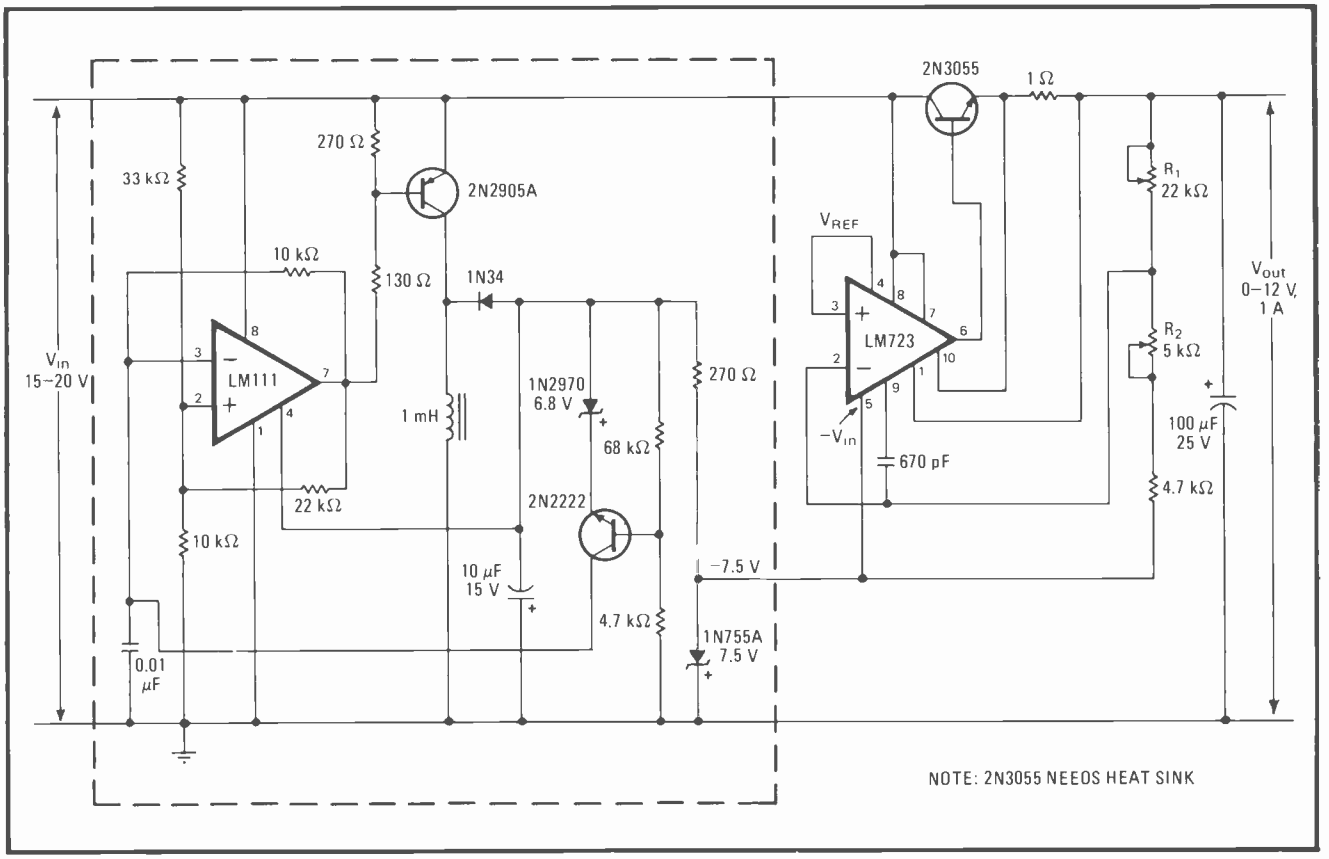
by P.R.K. Chetty and A. Barnaba
ISSP, Bangalore, India, and CNES, Toulouse, France

In most dc-input, regulated power supplies, regulation is poor when the desired output voltage is less than the source's internal reference voltage. In addition, circuit considerations usually limit the minimum reference voltage attainable and consequently the minimum regulated output voltage possible. This circuit, however, with a configuration that can bring the reference voltage to virtually zero, overcomes both problems.

The LM723 voltage regulator shown, which provides 12 volts at 1 ampere, must be biased with a negative supply voltage at its $-V_{in}$ port (pin 5) for proper operation. This voltage is provided by the switching inverter shown within the dotted lines.

The LM111 voltage comparator is configured as an astable multivibrator that oscillates at a frequency of about 10 kilohertz. With the aid of the 1-millihenry inductor, which generates the counterelectromotive force required to produce a negative potential from a switched-source voltage, the inverter delivers a well-regulated −7.5 v to the $-V_{in}$ port of the 723.

The magnitude of this voltage is essentially equal to that of the regulator's internal reference voltage, V_{REF}, appearing at pin 4, and properly biases its voltage-reference amplifier. This condition in turn precipitates a condition in the amplifier whereby V_{REF} clamps to ground potential. Thus the output voltage may be adjusted throughout its maximum possible range by potentiometers R_1 and R_2. Although the potential of V_{REF} as measured with respect to ground has been changed, the circuit will retain the regulating properties of the 723. Both the line and the load regulation of the supply are 0.4%. □



Full-range regulation. Dc-input supply is regulated all the way down to 0 V. LM111 and associated circuitry provide negative bias required for LM723 regulator. Regulator's internal-reference voltage, V_{REF}, is clamped to ground; output voltage is thus adjustable from 0 to 12 V.

Simplified priority encoder has low parts count

by Tomasz R. Tański
Warsaw, Poland

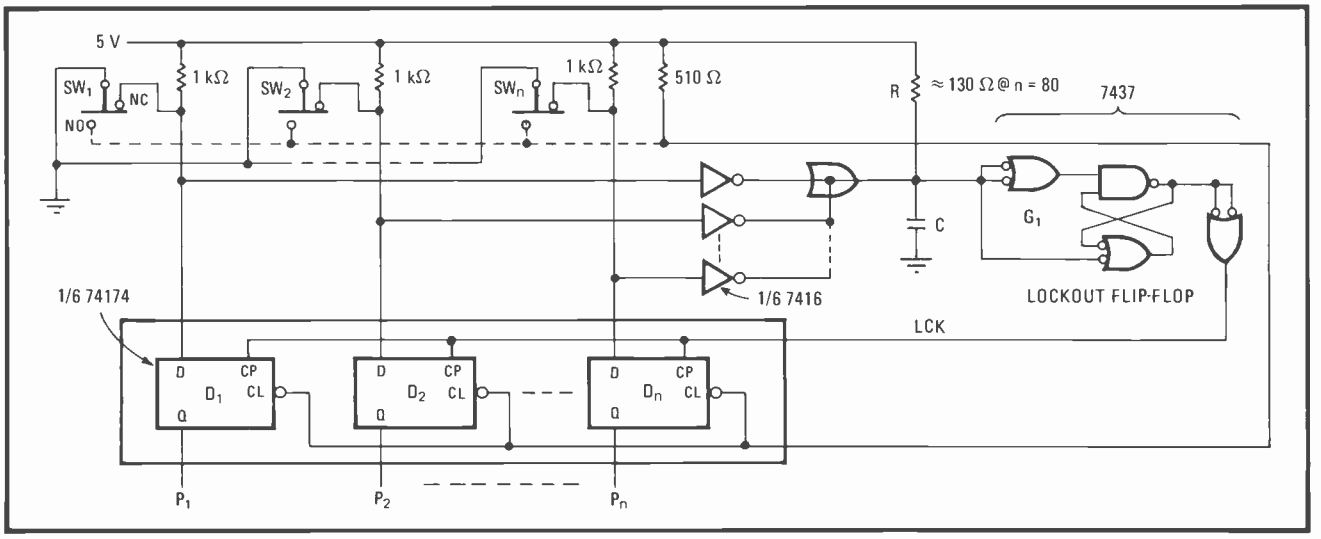
The number of chips in the priority encoder circuit described by Sterling [*Electronics,* Aug. 18, 1977, p. 114] can be drastically reduced by replacing the modularized gate arrays by D flip-flops and a wired-OR gate. As in the original circuit, the output ports of this modified momentary-contact switch array responds to the first command received and locks out all subsequent commands, so as to provide a time-sequence priority scheme that is useful in many industrial systems. But this circuit is simpler to build and test, because the interconnections between elements are minimized.

Depressing any switch, SW_n, shown in the figure sets the corresponding D input of its flip-flop, D_n, high. The switch signal also quickly propagates through the 7416 inverters, which have their open-collector outputs wired together to form an n-input OR gate, and fires the 7437 flip-flop (G). A few microseconds later, the rising edge of the resultant output from G_1 stores the signal generated by SW_n into D_n before the D line, at logic 1 for a time measured in milliseconds, can return to ground.

The strobing signal (LCK) will stay high until all switches return to their normally closed (NC) position. Thus altering the output state of any flip-flop is impossible, because all other switch commands are locked out.

Resistor R serves in a dual capacity. Its primary function is as load resistor for the open-collector inverters forming the wired-OR gate. Its value is selected so that the maximum current drawn is limited to the full-on collector current of one gate, independent of how many gates are activated. Secondly, R, in combination with C, provides effective switch debouncing. For optimum debouncing performance, the value of C should be selected (with the aid of a scope) to provide the trailing-edge delay required for signals from G_1.

Not considering the lock-out flip-flop, only one sixth of a 7416 and 74174 device are needed per switch, compared with the 1½ integrated circuits required in the original circuit. Only one 7437 is required, even for a large number of switches. Each input lead of the 7437 can accommodate an 80-input, wired-OR gate. The LCK signal can drive up to 180 flip-flops. □



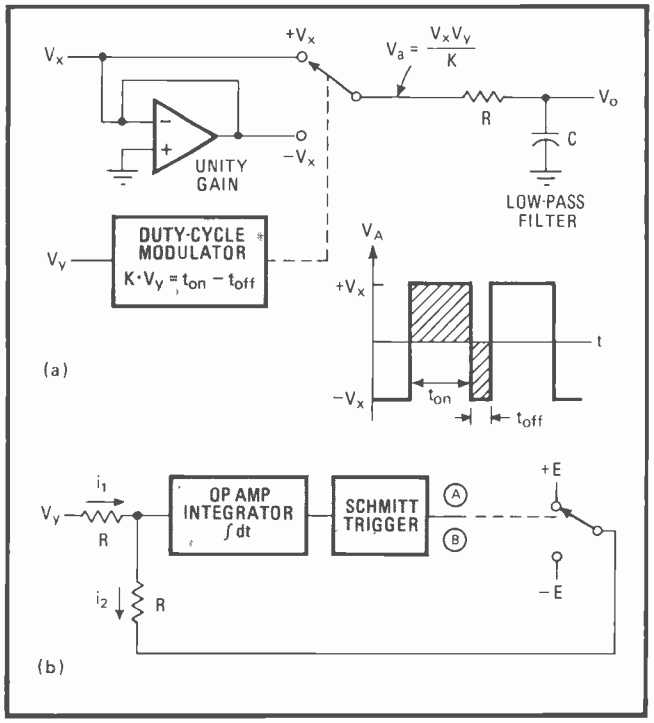
Simplification. Momentary-contact priority encoder uses about one fifth the number of chips of previous design. Circuit responds to first command received by switches and locks out all subsequent commands, thus forming a first-come, first-served switch.

Switching multiplier is accurate at low frequencies

by Harold Anderson and Peter Hiscocks
Ryerson Polytechnic Institute, Toronto, Canada

When called upon to multiply low-frequency analog waveforms, switching-type multipliers are at least an order of magnitude more accurate than those that work on the principle of variable transconductance. The typical output error of a transconductance multiplier such as the MC1595 is 1%. But this circuit finds the product of two signals to within 0.05% of the true value and costs only $5.

In the basic switching multiplier (Fig. 1a), an analog signal of constant voltage V_x is applied to the circuit. The voltage at point V_a at any given instant is a function of the switch position, and the switch position in turn depends upon the control signal emanating from the duty-cycle modulator.



1. Very linear. Switching multiplier (a) is more accurate for finding product of two signals at low frequencies than IC transconductance multipliers. Duty-cycle modulator may be built with op-amp integrator and Schmitt trigger (b). Voltages ±E and integrator together form oscillator of which the duty cycle is controlled by amplitude of V_y.

The average voltage at point A is:

$$V_a = V_x (t_{on} - t_{off}) \quad (1)$$

as shown in the graph, where t_{on} is the time during which the switch remains in contact with the $+V_x$ position and t_{off} is the time the switch remains in contact with the $-V_x$ position.

If the duty cycle, $t_{on}/(t_{on}+t_{off})$, can be made proportional to a second analog input voltage, V_y, then the following relation holds:

$$V_y = K(t_{on} - t_{off}) \quad (2)$$

where K is a constant. If Eqs. 1 and 2 are combined, the result is:

$$V_a = V_x V_y / K \quad (3)$$

A block diagram of a duty-cycle modulator which satisfies Eq. 2 can be constructed with an integrator network and Schmitt trigger (Fig. 1b).

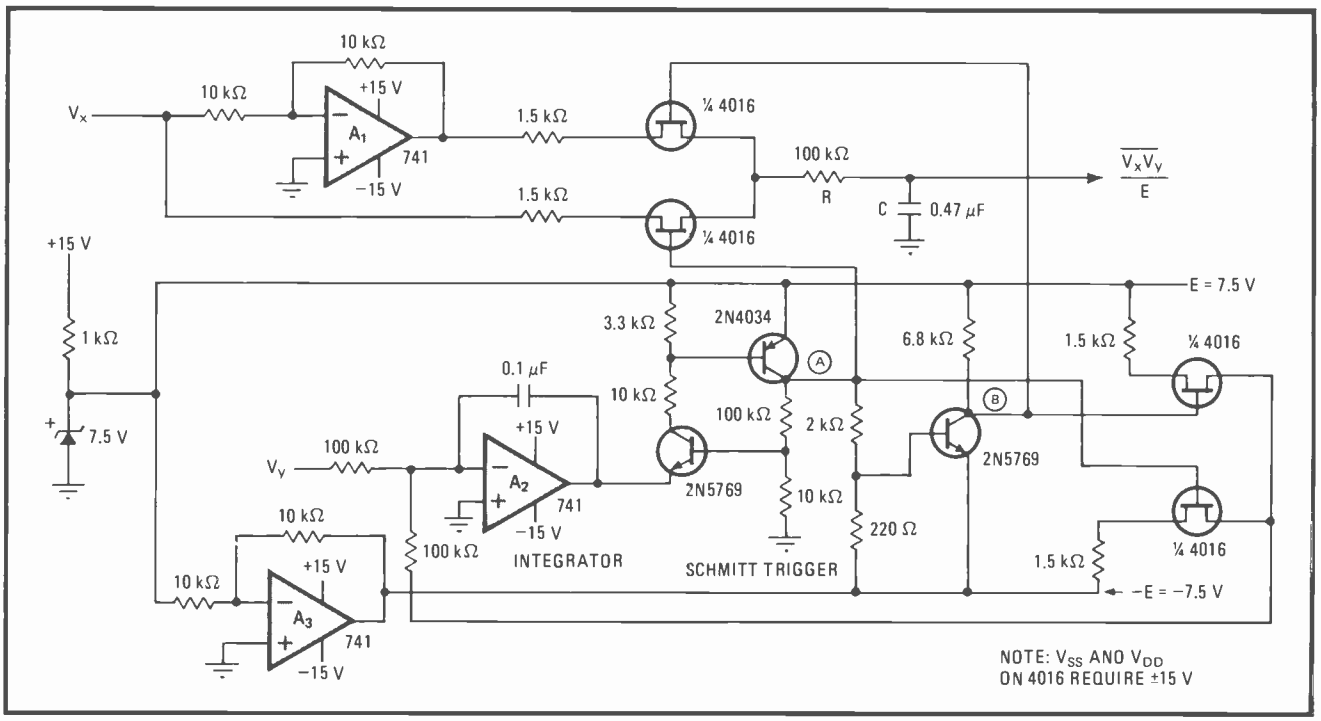
The average current into the input port of the integrator will be zero over a specified time interval, because of the high impedance of the op amp. Thus:

$$\bar{i}_1 = V_y/R = \bar{i}_2 = (E/R)t_H - (E/R)t_L \quad (4)$$

where t_H is the period during which the switch is engaged at $+E$ and t_L is the period the switch dwells at $-E$. It is found from Eq. 4 that:

$$V_y = E(t_H - t_L) \quad (4a)$$

If t_H can be made equal to t_{on} of Fig. 1a and t_L can be made equal to t_{off}, then the preceding equation, when substituted into Eq. 1, yields:



2. Multiplier. Building the circuit from the block diagram shown in Fig. 1 is straightforward. A_1 is inverting, unity-gain amplifier. A_2 serves as integrator. Three transistors form standard Schmitt trigger. Four transmission gates provide a practical switching circuit arrangement for ±E, ±V_x. Inverting operational amplifier A_3 ensures that +E is equal in magnitude to −E.

$$V_a = V_x V_y / E \quad (5)$$

This condition is met by wiring the Schmitt trigger to engage not only the $\pm E$ ports but also the $\pm V_x$ ports of the circuit in Fig. 1a as well.

The block diagrams of Fig. 1 are therefore easily transformed into the practical circuit of Fig. 2. Note that voltages $\pm E$ are the feedback voltages to the summing integrator network at the input to A_2 necessary to ensure that $t_{on} - t_{off}$ is proportional to V_y. In essence, this part of the circuit is an oscillator, excited by V_y and driven by $+E$ or $-E$ feedback.

Also, although V_y controls the duty cycle, the basic oscillator frequency is virtually independent of it. (Note than when $V_y = 0$, $t_{on} = t_{off} + 0$).

The Schmitt trigger used is standard. The low-pass filter RC smooths out any transients that are caused by the switching process. Four complementary-metal-oxide-semiconductor transmission gates implement a practical switching circuit.

As suggested by Eq. 4a, this circuit does require that the magnitude of $-E$ tracks that of $+E$. Inverting op amp A_3 generates the mirror voltage required. □

Diode sensor and Norton amp control liquid-nitrogen level

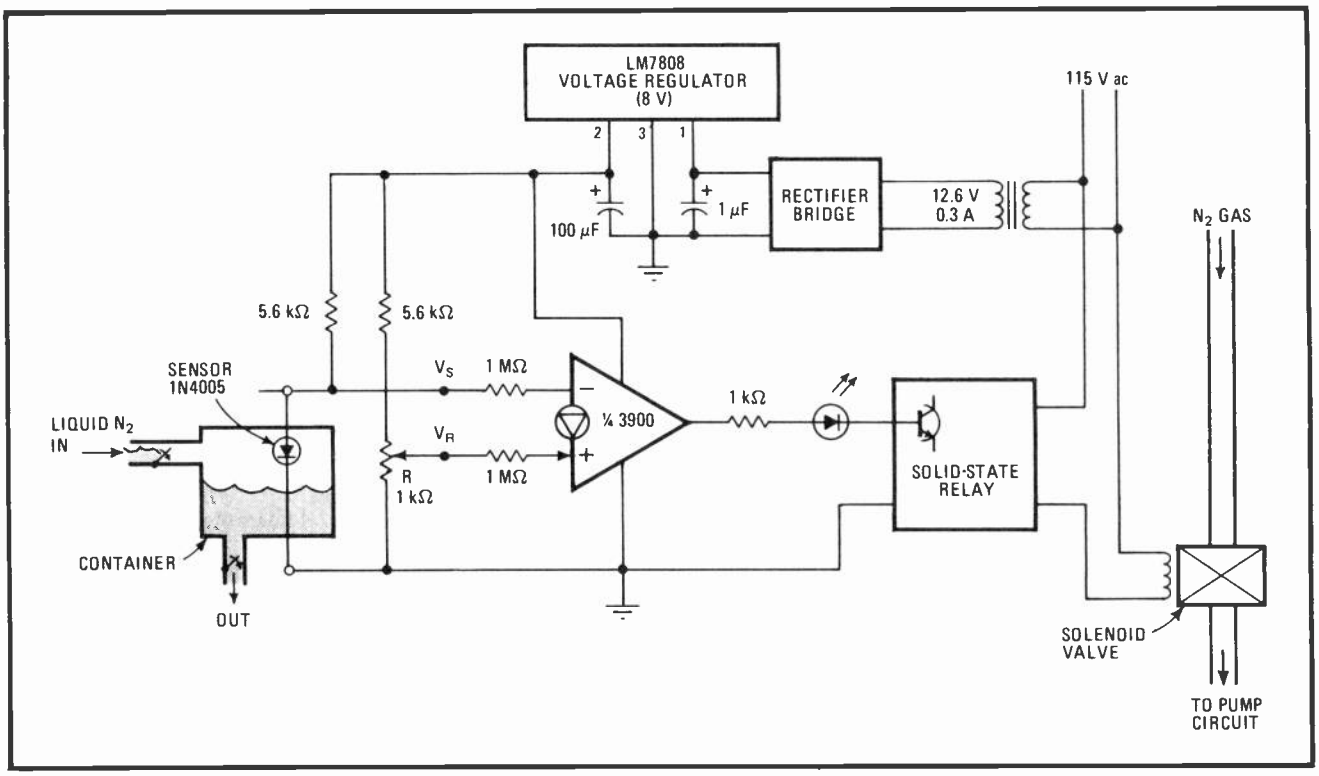
by V. J. H. Chiu
National Research Council, Ottawa, Canada

In parametric amplifier and other cryogenic applications, it would be handy to have an inexpensive sensor and controller of the level of liquid nitrogen. One can be built around a standard silicon diode and a Norton (current) amplifier.

The circuit's operation is based on the principle that the diode's junction voltage increases from 0.7 volt at room temperature to 1.05 v in liquid nitrogen (liquefaction temperature: −196°C). This voltage change is used to activate the amplifier, which controls a solenoid valve. The valve regulates a nitrogen-gas supply, which pumps liquid nitrogen from a reservoir to the desired container that houses the sensor.

The controller is shown in the figure. The sensor is placed in the container at any desired level. When liquid nitrogen rises to this level, voltage V_S reaches the preset voltage V_R almost instantly, and the output of the 3900 Norton amp becomes zero, closing the valve. When the liquid nitrogen falls below the desired level, V_S drops below V_R, and the valve opens.

Circuit sensitivity is adjusted by R. The diode need not be completely immersed in the liquid nitrogen, for its range is such that liquid as much as 2 inches below it will start the refilling of the container. Frequent cycling is thus avoided. The state of the solenoid valve may be determined by observing the light-emitting diode. □



Fixing the nitrogen level. When liquid-nitrogen level in container is below the diode position, solenoid is turned on and pumps in more N_2. When level reaches that of diode, its junction voltage jumps from 0.7 to 1.05 V, turning off solenoid and stopping N_2 inflow.

Accurate thermometer uses single quad op amp

by Yishai Nezer
Haifa, Israel

For temperature ranges up to 150°C, a thermometer built around a single integrated circuit has not only greater linearity than a thermocouple but also far greater sensitivity—approximately 2 millivolts per degree Celsius. The sensor achieves this superior performance by exploiting the well-known voltage-to-temperature relationship of a semiconductor pn junction.

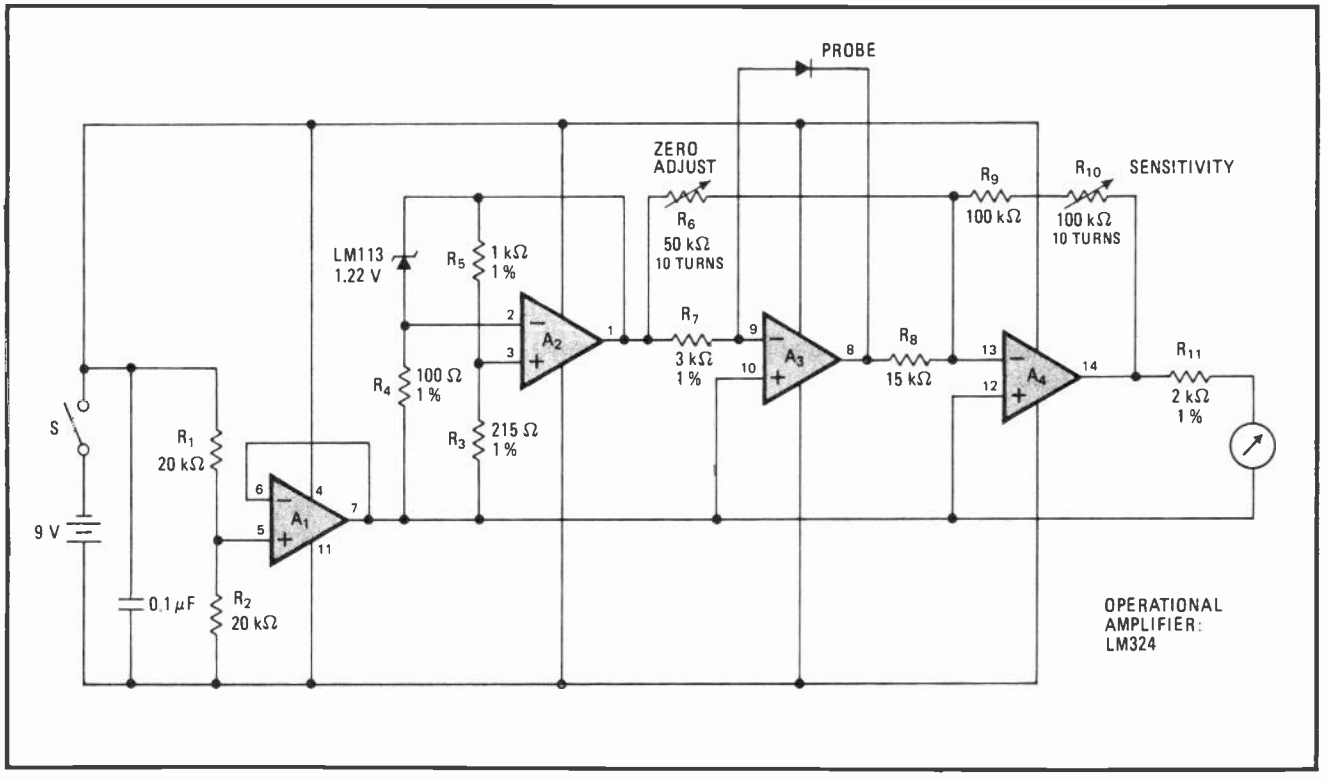
In the temperature-sensing scheme shown, the low-power LM324 quad operational amplifier and a diode probe are the central elements. The first two op amps, A_1 and A_2, have the job of keeping a constant current through the diode, to ensure that any voltage changes across the diode are a direct result of temperature changes at the probe. A_1 serves as a buffer for the input circuit divider resistors, producing an output of 4.5 volts that acts as a reference point for the other op amps and permits them to operate in their linear region. A_2, in conjunction with the LM113 reference diode, produces a constant 1.5-v output, which is practically independent of variations in battery voltage or circuit temperature and thus supplies the diode probe with a constant current of about 0.5 milliampere.

The output voltage of this diode is buffered by op amp A_3, and changes in A_3's output are reflected in the output of A_4, inserted to provide a separate point to adjust for device sensitivity and calibration.

A simple calibration procedure is necessary for proper operation. Once the range of temperatures to be measured has been determined, the zero-adjust potentiometer is set for zero output voltage at the low temperature extreme, and the sensitivity-adjust potentiometer is set for a convenient output (perhaps full-scale reading) at the upper temperature extreme. A 1-mA meter movement can be used at the output.

If a wide range of temperatures (0° – 150°C) is to be measured, a diode-connected transistor (base and collector connected) is often preferable to a diode, because its properties better approximate an ideal pn junction. But in applications where the temperature variations are small, a glass-encapsulated diode is more convenient. The probe should be isolated when the circuit's power supply is not floating with respect to the tested environment.

Precision is better than 0.1°C, provided shunt conductances are minimized at the probe. Current drawn by the circuit is typically 4 mA. Power consumption can be conserved further by use of a switch. □



Precision thermometer. Accuracy is limited primarily by ammeter readability. Thermometer is sensitive enough for medical applications where temperature variations are small. LM113 can be replaced by two silicon diodes in series for less demanding applications.

Expanded test inputs increase 4004 processor capability

by Robert F. Starr
Shell Oil Company, New Orleans, La.

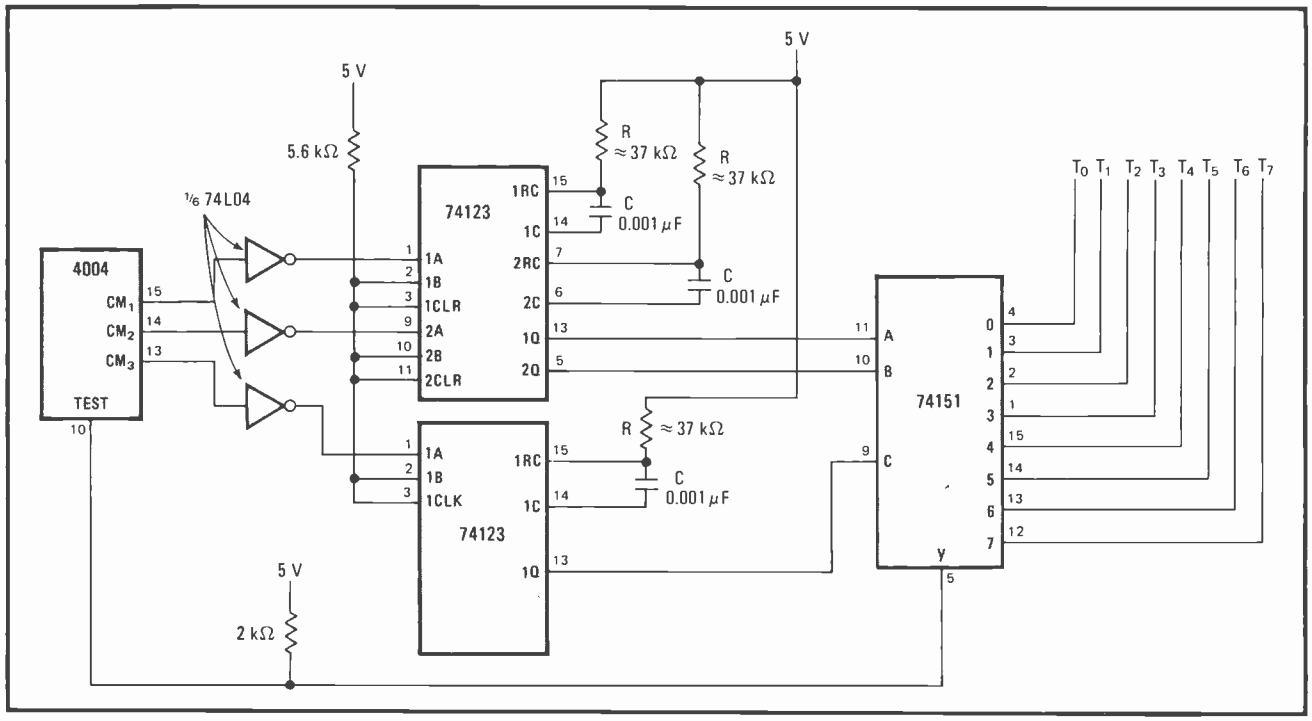
Although it was the first commercial microprocessor, the 4004 is still useful in many control and data-acquisition systems, especially those using binary-coded-decimal data, for which its 4-bit word is a convenient match. To increase its usefulness, a simple and inexpensive multiplexing circuit can furnish the equivalent of an interrupt feature by gating up to seven extra inputs to the 4004's test port.

The desired test signal can be selected by means of the 4004's three CM output lines. As generally used, the designate-command-line instruction (DCL) sets the binary code at the CM outputs to select one of eight random-access memories. But here the instruction selects lines T_0 through T_7.

The CM signals trigger their respective 74123 monostable multivibrators. The multivibrators drive the 74151 multiplexer, which routes the desired input line to the test port.

The duration of the signal generated by the one-shots is slightly greater than one instruction cycle (10.8 microseconds) to ensure that they may be retriggered. Thus, true logic signals will be generated on the multiplexer's select lines, making operation more stable. In some cases, it may be necessary to insert a no-operation instruction after the DCL command to allow the outputs of the one-shot to settle before the software attempts to check the status of the test line.

The circuit can be built for a few dollars. For the added flexibility it provides, it is well worth it. □



Expanded test capacity. Multiplexed test lines increase usefulness of 4-bit 4004 microprocessor. Selection of test lines $T_0 - T_7$ is accomplished by software. One-shots are retriggerable, transform processor's pulse output to true logic signal for selecting multiplexer lines.

Wideband preamp and LSI pair form high-quality counter

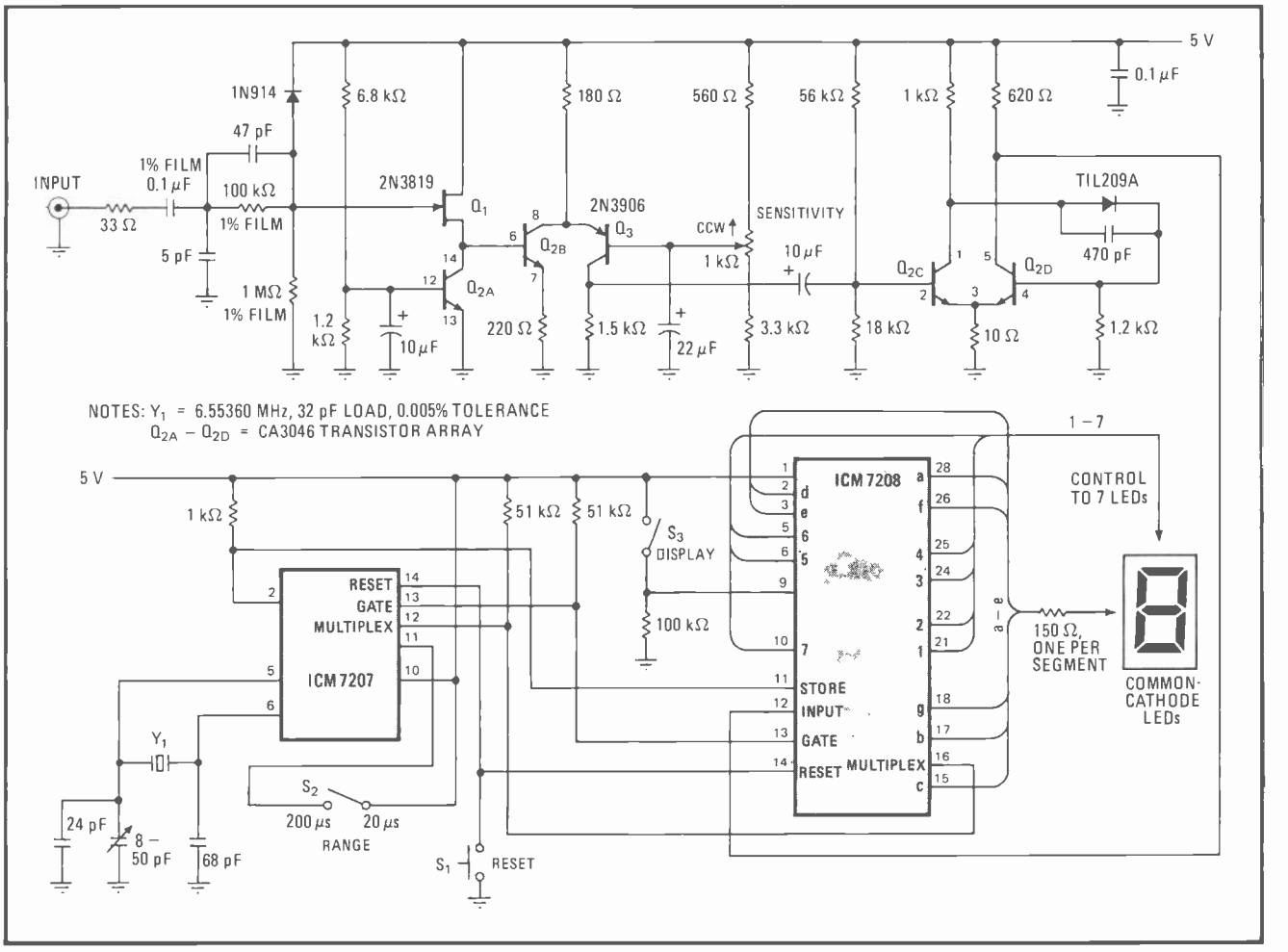
by James A. Mears
Dallas, Texas

A carefully designed preamplifier, when combined with two new large-scale-integrated circuits, forms a high-performance, low-cost frequency counter with a typical response of 5 megahertz. Among this counter's many desirable qualities are a high input impedance throughout the frequency-measuring range, a frequency response that can be extended to 30 MHz, a single voltage supply and, if the displays are powered separately, a low

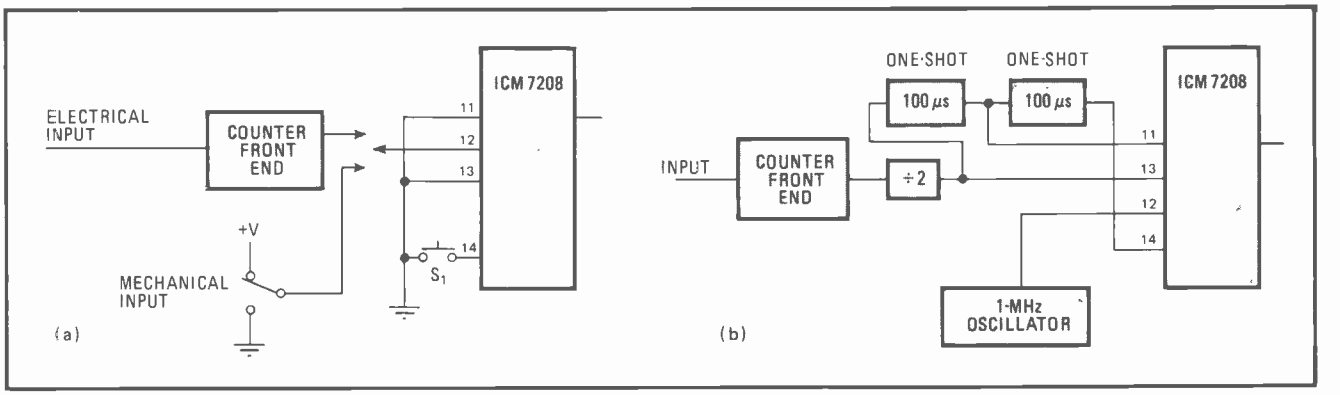
power drain that allows battery operation.

As the figure shows, the input signal is applied to the 2N3819 field-effect transistor through a frequency-compensated attenuator. The combination of the FET and attenuator produces an input impedance of 1 megohm from 0 to 30 MHz. The input circuit is protected from overdrive by the 1N914 diode. Q_1 is a current-biased source follower, providing high input impedance, low output impedance, and high stability even at low power-supply voltages.

The amplified signal is applied to the cascode amplifier composed of Q_{2b} and Q_3. The operating (bias) point is Q_3 is adjustable over a 1-volt range, so that the triggering voltage may be properly set even with noise present on the input signal. The signal is then introduced to the Schmitt trigger composed of Q_{2c} and Q_{2d}. The circuit has a fixed hysteresis determined by the TIL209A light-emitting diode (the LED acts as a low-voltage zener), which makes triggering precise even with slowly varying waveforms. This output signal, which will



1. Frequency counter. A well-designed front end and two LSI circuits permit realization of a high-performance, low-cost frequency counter. The counter's frequency response is 5 MHz, but can be expanded to 30 MHz. Total cost is $50, half that of competitive units.



2. Easily adaptable. A slight modification to the input circuit makes it absolutely versatile. The circuit can be configured to monitor the number of electrical or mechanical events (a) or as a period counter (b) for measuring input cycle duration or the time between events.

be counted by the Intersil ICM7208, has a duty cycle of approximately 50%.

The ICM7208 contains a seven-decade counter, a display multiplexer, a seven-segment decoder, and digit and segment drivers. Additional circuits within the 7208 serve to blank the display, reset the counter inhibit input, and switch the display on and off. The device can count to 5 MHz, and the circuit draws only 1 milliampere or so at 5 V. A companion device, the ICM7207, supplies a crystal-controlled time base and other signals for multiplexing the display and controlling the sampling interval of the 7208.

The output frequency of the crystal-controlled oscillator is reduced to 1.6 kilohertz by the 7207 in order to multiplex the seven-segment LED display. The 7207 is also configured to produced a gate signal of 20 or 200 microseconds for the 7208 counter. This count window is switch-selectable. Leading-zero blanking and an on/off switch for the display are provided for energy conservation.

The circuit may be simply reconfigured as a period of event counter, as shown in Fig. 2. Additional divider stages at the counter's input and control-signal channels may be used to expand the range of the counter to 30 MHz.

This counter compares favorably with other designs. Its sensitivity at 0.1 MHz is 50 millivolts, decreasing to 200 mV at 30 MHz. The current drain is 21 milliamperes at 5 V, neglecting the LED displays. Total cost for this circuit is less than $50; a transistor-transistor-logic frequency counter would cost twice as much and might dissipate as much as 40 times the power. Commercially available units cost $200 to $300. □

Bias-current network improves sample-and-hold response

by H. F. Nissink
Physics Department, University of Tasmania, Hobart, Australia

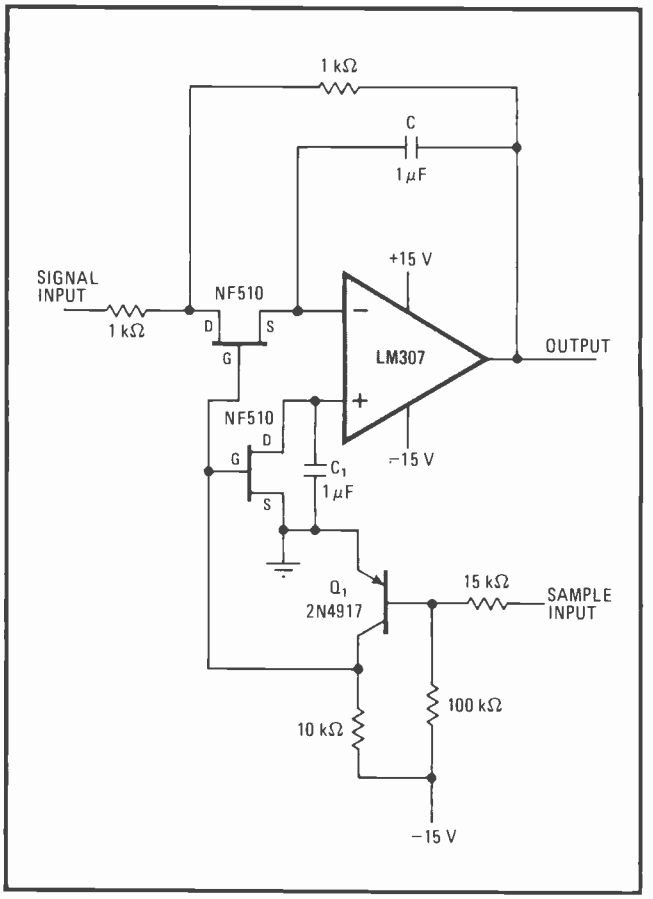
A compensating bias-current network greatly enhances the voltage-holding quality of a sample-and-hold circuit. Connected to the noninverting port of the operational amplifier, the network detects and restores the charge lost by the hold capacitor.

As shown in the figure, an input signal is sampled at the NF510 transmission gate by a pulse from switching transistor Q_1. The sampled voltage appears across C almost instantaneously and should be stored indefinitely. However, there is a small loss of charge with time because of voltage drift at the op-amp output. The drift is due to the op amp's minute bias current, which flows into the inverting input. This current lowers the output voltage and thus the voltage across C.

However, because the bias currents flowing at both inputs of the op amp are approximately equal in magnitude (although opposite in polarity) over a wide range of input voltages, circuitry added to the inputs can compensate for the bias-current flow. Specifically, if C_1 is made equal to C, each port will look out onto an identical circuit. Thus small changes in the bias current at the inverting port, which removes charge from C, will be countered by like changes in the current at the noninverting port, which charges C_1, and the op amp's input offset voltage will be minimized.

Of course, because of the inherent properties of the op amp, the magnitude of the input currents cannot continue to increase for a constant output voltage. A condition will therefore eventually occur in which the current at the inverting port will exceed the current at the noninverting port, and the output voltage will fall.

The circuit has a hold time—arbitrarily defined as the time in which the output voltage decays by 100 millivolts—of approximately 4 minutes with the values shown and about 10 minutes if both capacitors are doubled in value. The decay is independent of the magnitude or polarity of the input voltage. □



Charge restorer. Sample-and-hold response is improved if charge lost by hold capacitor C is replaced. Voltage change across capacitor due to op amp's inverting-port bias current is cancelled by compensating network. Droop rate, only 100 millivolts per 10-minute period, may be improved if capacitors C and C_1 are matched.

Fixed-voltage regulator pair forms bipolar power supply

by S. K. Wong
Torrance, Calif.

Two fixed-voltage regulators and suitable feedback circuitry can form a bipolar power supply that combines the excellent voltage regulation, trackability, and high current capacity of the three-terminal integrated-circuit voltage regulator with the voltage adjustability of more expensive supplies. This unit provides bipolar voltage from 8 to 20 volts at 1 ampere. The trackability, defined for an adjustable power supply as the voltage difference remaining between the bipolar ports at the desired output voltage, is 1%. Regulation for both line and load is about 100 millivolts.

Many IC bipolar regulators are available, but they provide only 100 milliamperes or so and their output voltages are essentially nonadjustable. Other popular regulators provide high current (up to 3 A) but are fixed-voltage devices. Although IC bipolar regulators can be modified with high-power transistors to boost the output current capability, and separate positive and negative voltage regulators can be connected directly to meet special voltage and power requirements, both designs still lack both adjustability and trackability. These features are often needed in many applications.

Figure 1 shows the regulated supply that employs two popular three-terminal regulators and a three-transistor feedback circuit. A 115-v, 60-hertz alternating current input is transformed to approximately 40 v across its center-tapped winding, and is rectified and filtered to generate ±27 v to the input of the respective regulators. The positive voltage output is:

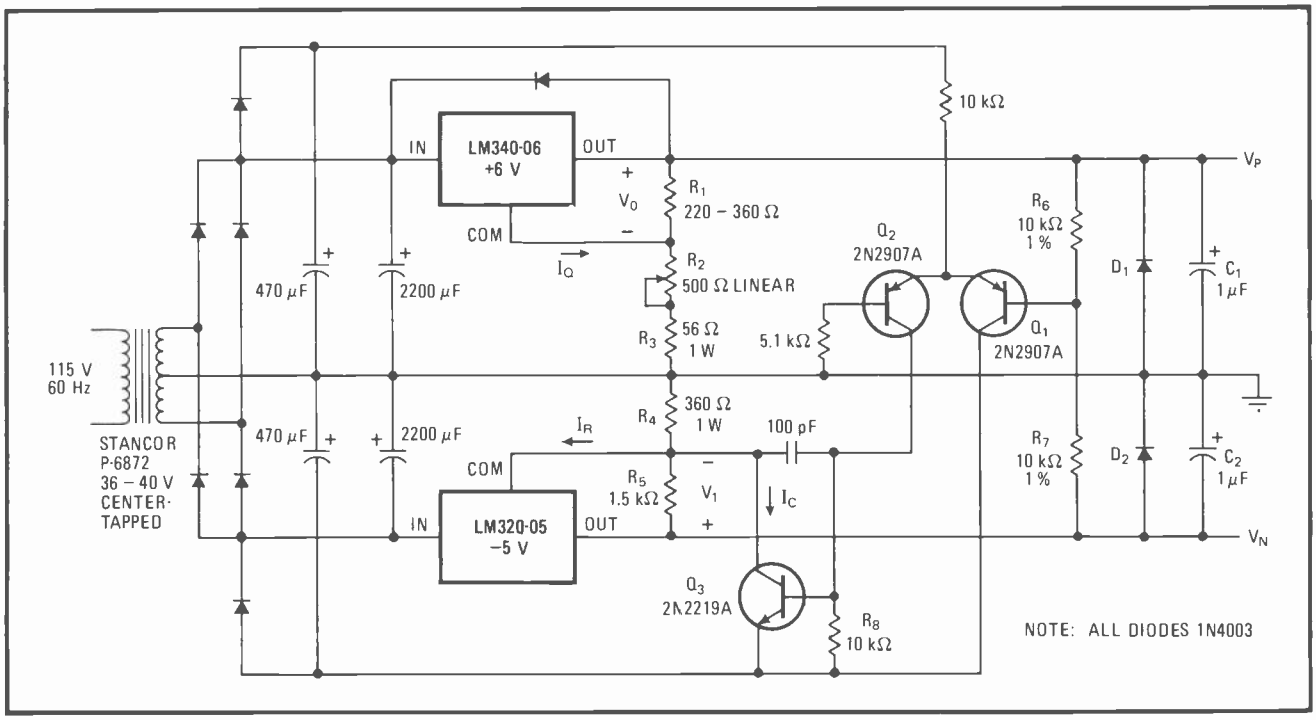
$$V_p = [1+(R_2+R_3)/R_1]\,V_o+(R_2+R_3)I_Q$$

where V_o may nominally range from 5.75 to 6.25 v for the fixed-voltage LM340-06 device and I_Q is the quiescent regulator current, which is 10 milliamperes maximum and is fairly independent of input voltage and load current. Adjustment of R_2 will change the output voltage, and accordingly, the negative voltage output V_N. The negative output is:

$$V_N = (1+R_4/R_5)V_1+R_4(I_C+I_R)$$

where I_R is the quiescent regulator current, I_C is the collector current of transistor Q_3, and V_1 is the output voltage of the negative regulator.

The LM320-05, which is a −5-v regulator, and transistors Q_1 through Q_3 form a slaved configuration. A differential amplifier composed of transistors Q_1 and Q_2 monitors the difference in magnitude between V_P and V_N through a precision voltage divider R_6 and R_7 and compares it to a zero reference. Normally, the voltage at this junction is zero, because $V_P = -V_N$. Any error voltage is amplified to cause a change in the collector



Bipolar-tracking power supply. Adjustable voltage output is obtained with fixed-voltage regulators if each regulator is connected back to back through current-varied networks. Circuit retains regulation properties, has high current capability, excellent trackability.

current of Q_3, which in turn changes the voltage across R_4 and consequently V_N.

The high output current that can be produced by the supply generates several points where power dissipation is great. Components must be selected to ensure that those levels can be adequately handled. The maximum current through Q_3 is 78 mA. The maximum power consumption is about 500 mW. The 2N2219A transistor is used for this application. Both regulators should be mounted on suitable heat sinks. Resistor R_3 prevents excessive current through R_2 when its value is low.

Heavy common-mode loads may cause difficulty in the operation of the feedback network during start-up unless diodes D_1 and D_2 are used to clamp the circuit outputs. C_1 and C_2 are tantalum capacitors for improved transient response. □

Time-shared DVM displays two inputs simultaneously

by Barry Harvey
Siliconix Inc., Santa Clara, Calif.

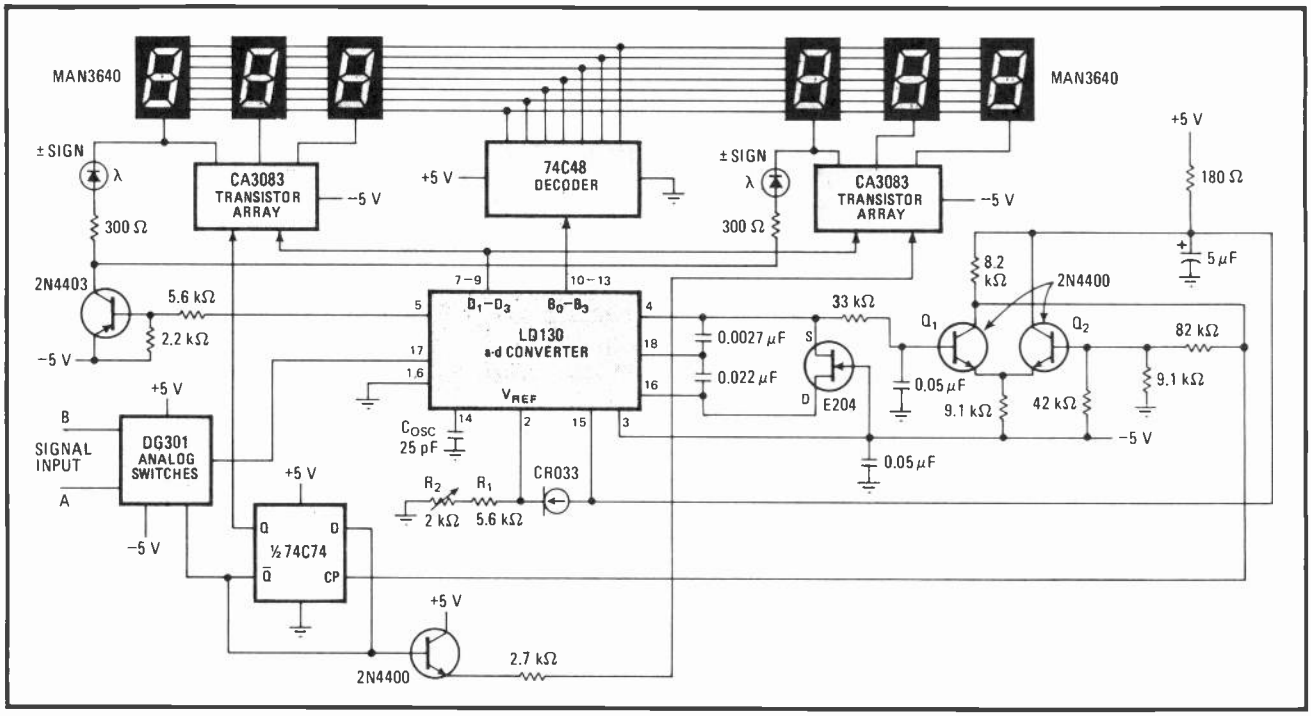
Two voltages can be measured and displayed simultaneously with one voltmeter if the voltmeter is built around a time-sharing circuit containing a fast-sampling analog-to-digital converter. The converter is united with an input-signal multiplexing network, and the system elicits a normally flicker-free response from a light-emitting-diode display, while saving the cost of the additional voltmeter and other parts that would be needed for two separate measuring units.

As implied by the figure, this circuit accomplishes two major tasks; it controls the rates at which analog signals and two banks of LEDs are sampled, and it determines the strobe rate of each LED in the banks.

The LD130 ±3-digit a-d converter was selected for its relatively fast sampling speed of up to 60 samples per second. The sampling rate of this complementary-metal-oxide-semiconductor device is controlled by external capacitor C_{osc} in conjunction with the internal oscillator circuitry of the device. Its output drives transistor pair Q_1 and Q_2, which in turn drive the sampling and multiplexing circuits through the 74C74 D flip-flop. The output of the flip-flop switches 30 times per second; the analog input signals are multiplexed at this rate through the DG301 analog switch, and one of two banks of LEDs is selected through the CA3083 transistor array. Each bank contains three MAN3640 displays.

The LD130 periodically samples each signal input and converts it into a digital output. Each display and its segments are driven through a strobe sequence; $D_1 - D_3$ determine which digit in each bank is enabled, lines $B_0 - B_3$ of the converter supply binary-coded-decimal information to the seven segments of each LED through the 74C48 decoder/driver, and the 74C74 determines which bank is chosen. The strobe rate for the LEDs is 384 times per sampling period.

Although the measurements are performed 30 times per second per channel, fast enough so that flickering would not usually be detectable, flutter of the least significant digit may occur when the LD130 is sampling



Two voltmeters in one. If the input signals can be sampled at rates of 60 times per second or greater, they can be measured, then observed simultaneously at acceptable flicker rates. Key to circuit operation is use of fast-sampling analog-to-digital converter.

the input signals, because of the ±1-count effect inherent in counter operation. However, in applications where the output is observed only occasionally, it will not bother the eye, and in any case, a full three-digit reading is discernible.

To calibrate the converter, a reference of approximately 2 volts is required at the V_{ref} terminal, and this is easily furnished by the 330-microampere constant-current diode CR033 and resistors R_1 and R_2. R_2 is adjusted to null the output for no-signal conditions. □

D-a converter controls programmable power source

by C. Viswanath
Indian Institute of Science, Bangalore, India

The output of an integrated-circuit regulator can be digitally controlled to generate any number of voltages for use in testing components or equipment. A digital-to-analog converter transforms the digital value into a current, and the current is converted to a linearly proportional voltage.

As shown in the figure, the Analog Devices' MDA-10Z-110 converter generates an output current of 0 to 2 milliamperes with a resolution determined by its 10-bit digital input. This current is transformed to an output voltage of 0 to 6 volts by the following 741 operational amplifier. The 723 is adjustable over a wide voltage range (7 – 37 volts), and for use as a 2-to-22-v regulator it requires a linear controlling voltage.

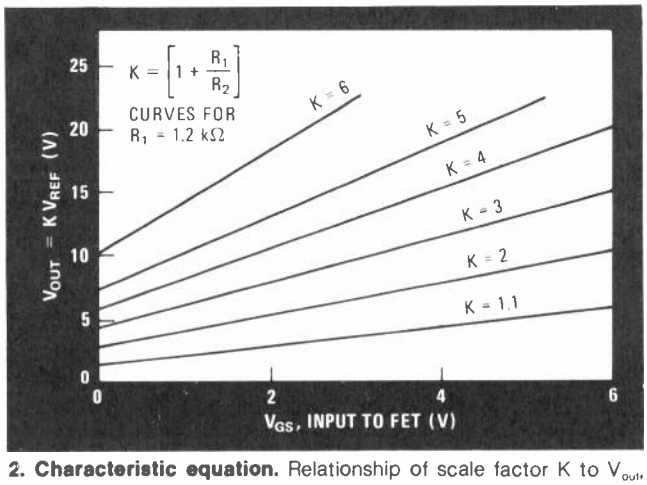
The 2N4351 field-effect transistor operates as a voltage-controlled resistor to produce voltage V_{REF}, which is essentially equal to the voltage across resistor R_6 and is linearly proportional to the digital input to the d-a converter.

The 723 was designed so that its output voltage is equal to an input voltage times a factor determined by gain-controlling resistors placed in a feedback loop. Thus, its characteristic equation may be expressed by:

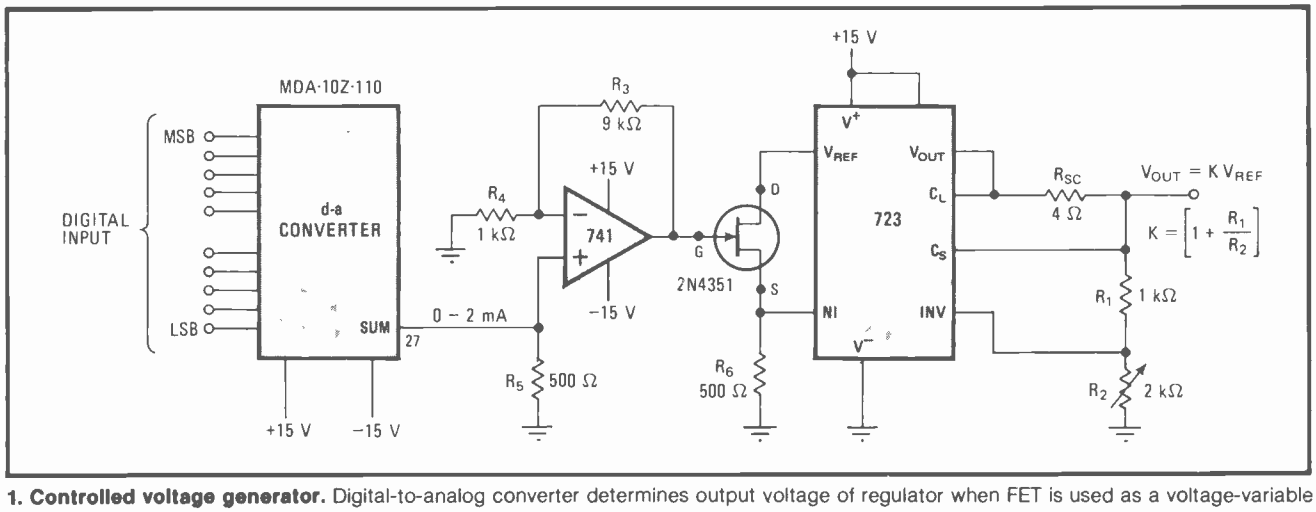
$$V_o = KV_{REF}$$

where K is equal to $1 + R_1/R_2$.

The 723 yields a load regulation of 0.02% and a line voltage regulation of 0.01% at output currents of up to 150 milliamperes. This excellent performance is made possible by the error-control amplifier in the 723, which compares V_{REF} to the scaled-down voltage derived by the resistor feedback network R_1 and R_2. Resistor R_{sc} is used in a current-limiting capacity. A value of R_{sc} = 30 ohms will limit the output current to 20 milliamperes; a value of R_{sc} = 4 ohms limits the output current to its rated maximum of 150 milliamperes. External transistor circuitry can be added to easily extend the load current capacity. □



2. Characteristic equation. Relationship of scale factor K to V_{out}. V_{GS} is linear as shown by curves. Scale factor is controlled by resistor feedback network at regulator output. FET, used as voltage-controlled resistor, assures output voltage is proportional to K.



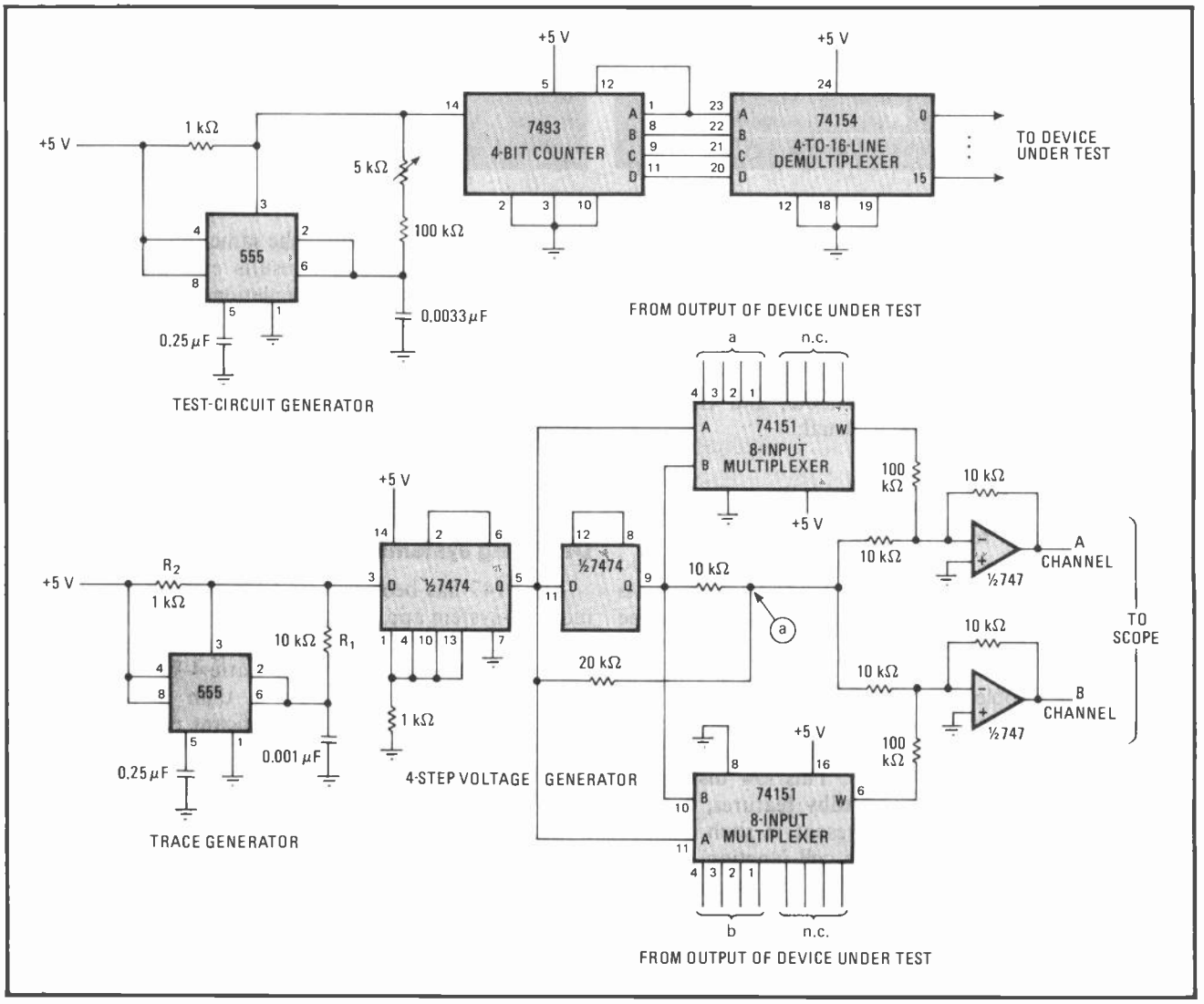
1. Controlled voltage generator. Digital-to-analog converter determines output voltage of regulator when FET is used as a voltage-variable resistor. If digital source is computer, specified voltages may be generated for automatic testing of components.

Eight-trace scope display checks analog or digital signals

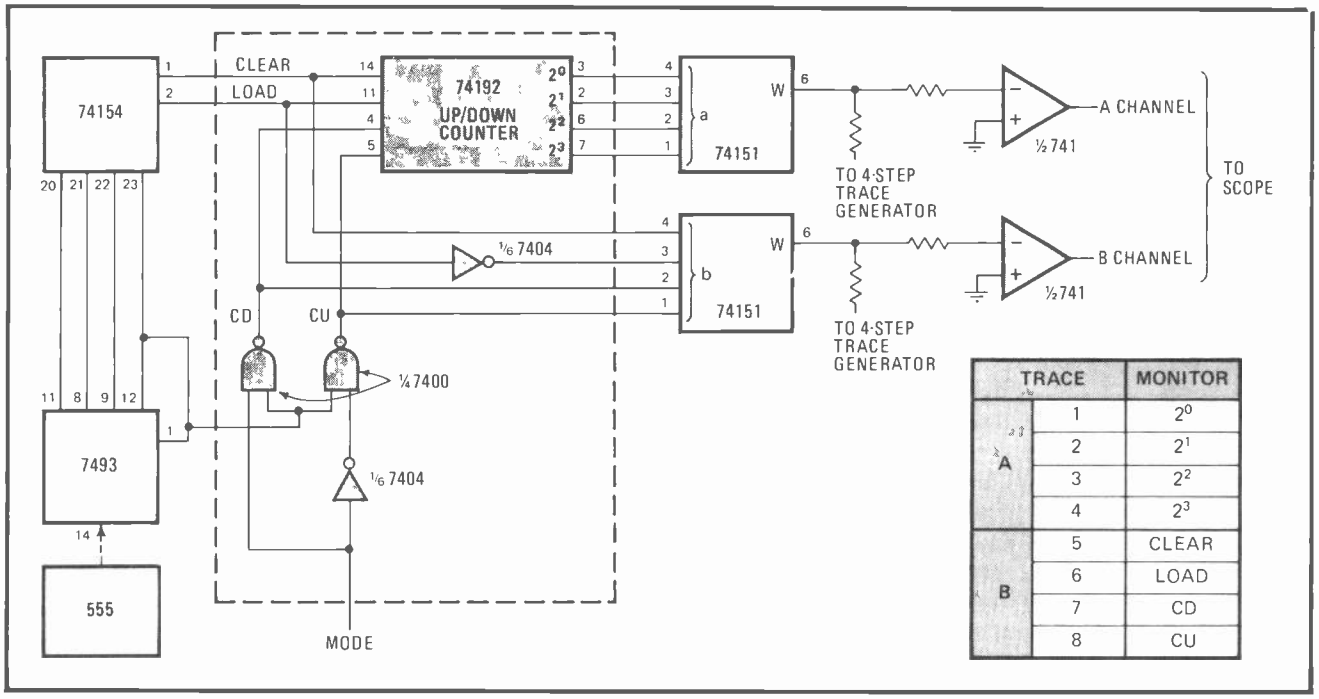
by George O. Wright
Washington, D. C.

Of all the circuits that enable a dual-trace oscilloscope to display multiple signals simultaneously, none yet provides the versatility of this one. It can be configured to monitor analog as well as digital signals. It does not require the use of the scope's sweep trigger voltage (which may not be available on some instruments) to drive the input-signal multiplexer. It also generates logic signals for stimulating devices under test. Thus the devices may be examined apart from their operating systems, which would normally supply the necessary stimulus. The circuit uses readily available integrated circuits, too, and can be built for less than $50.

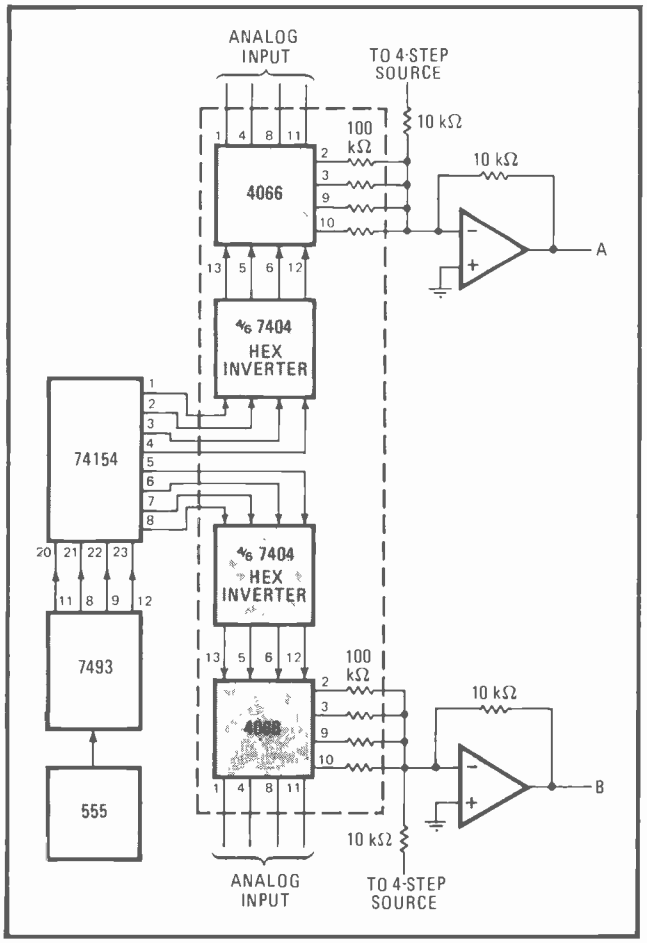
The basic circuit for observing digital signals is easily implemented, as shown in Fig. 1. A trace generator using the 555 timer and operating at 60 kilohertz drives a 7474 dual D flip-flop to produce a four-step dc voltage. The output of each flip-flop is summed across the junction of the 10- and 20-kilohm resistors at point (a) to generate an output of 1, 2, 3, and 4 volts. These voltages are then synchronously added with the signal from the output of the two 74151 multiplexers, which are driven by the selected outputs of the device under test. One flip-flop also switches the multiplexers directly, so that a total of



1. Low-cost analyzer. Four-step voltage generator, clocks, and counters generate eight-trace display for dual-input scope. Cost is under $50. Trace generator positions scope beam, while test-circuit generator derives logic signals to control device under test. Output of test circuit is digitally multiplexed through 74151s; alternatively, transmission gates may be used for observation of analog signals.



2. Digital application. Test of 74192 counter requires addition of inverters and NAND gates as shown, to derive logic signals for desired test sequence. Table specifies signal monitored by oscilloscope. Sync signal for scope is obtained from any point in trace generator chain.



3. Analog application. Replacement of 74151 multiplexers by transmission gates permits observation of eight analog signals, as shown. Logic generator continues to function in same capacity, driving 4066 analog switches with digital gating signals.

eight possible input signals can be displayed once every viewing cycle.

The test-circuit generator is similar to the trace generator but operates at 1,500 hertz. In conjunction with the 7493 decoder and 74154 multiplexer, it produces 16 logic signals for controlling the test pattern generated for the circuit under examination. The output signals from the multiplexer are sequential, each separated from its predecessor by one clock period.

Figure 2 shows a typical application of the circuit—testing the performance of an 8-bit synchronous up/down counter, in this case the 74192. Two NAND gates and two inverters have been added to derive signals that the 74154 could not itself generate, to cycle the test counter. The 74154 produces the clear and load signals, while the 7493, in conjunction with the NAND gates, derives the count-up and count-down signals (CU and CD in Fig. 2). All signals drive the 74151 multiplexers, either directly, through the counter, or through the logic gates. All eight output signals from the 74192 are multiplexed, four inputs per channel, to the oscilloscope.

As shown in Fig. 3, eight analog signals may also be observed if a slight modification is made to the basic circuit. This time, the 74154 provides the logic signals for the 7404 inverters, so that the 4066 transmission gates may be periodically sampled. The 74151 multiplexers are bypassed.

The trace generator frequency was initially set to provide acceptable scope viewing at minimum flicker rate. Step transitions of the four-value generator are not noticeable on the cathode-ray tube. The test-circuit oscillator frequency is 1/40 of the trace generator frequency to permit display of a sufficient number of events from the device under test; a 5-kilohm potentiometer has been added to permit small-range adjustments.

Both clocks should be separate and nonsynchronous to

permit the scope's sync trigger input from locking-in to the output frequency of the four-step generator. Sync for the CRT can be obtained from any point in the trace generator chain. (Both oscillators were described in *Electronics*, May 13, 1976, p. 95). As mentioned, R_1 should be at least 10 times R_2. The current through R_2 should be minimized, so that the 555 can generate sufficient drive to trigger transistor-transistor logic circuits. □

Expandable FIFO buffers improve processor efficiency

by Krishna Rallapalli
Fairchild Camera and Instrument Corp., Mountain View, Calif.

The need to service computer interrupts immediately, especially in applications where data is supplied to a computer at a fixed rate, may be eliminated by storing data in first-in, first-out registers. With the large-capacity FIFOs presently available, system-interrupt schemes are simple to design, and the use of complex and expensive direct-memory-access controllers is avoided.

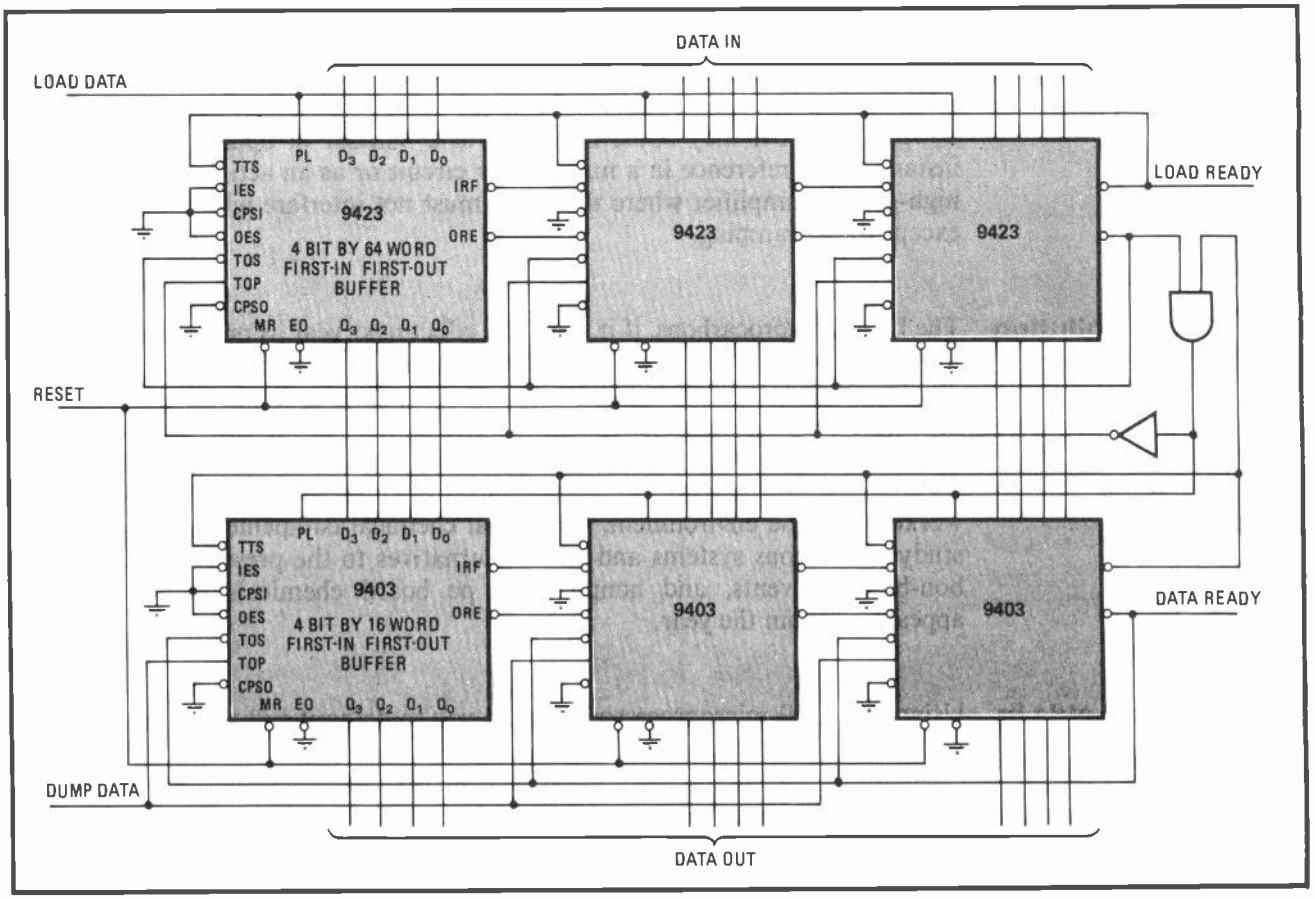
Data to the computer is typically introduced at a fixed rate by card readers. Once a card is fetched from the input hopper of most readers, it travels nonstop past the read head to the output stacker. An interrupt request must be serviced after every column of data is read, for otherwise the data is lost.

This potential problem is surmounted with the circuit shown. Three Fairchild 9403 16-word-by-4-bit FIFOs, simply cascaded with three 9423 64-word-by-4-bit FIFOs, can provide storage for up to 80 12-bit words before an interrupt request is serviced. Even with a busy computer, data is not likely to be lost.

The particular configuration of the control circuit that drives the FIFOs varies with the application. In all cases, however, it must generate a reset signal (to initialize the FIFOs), a data-ready signal, which is the interrupt request to the computer, and the load-data signal, which permits parallel loading of 12 bits of new data. The circuit must also monitor the availability of storage space in the FIFOs through the load-ready indicator, to determine if the load-data signal can be generated.

The dump-data signal, which is the interrupt-service signal, is generated by the microprocessor. It accepts the data from the output stage of the FIFOs while extracting the next data word. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.



No need for DMA controller. Expandable FIFOs can store up to 80 12-bit words before interrupt request is serviced, eliminating need for direct-memory-access port. Several easily synthesized control signals generate interrupt and load signals, determine status of FIFOs.

LED bar-segment array forms low-cost scope display

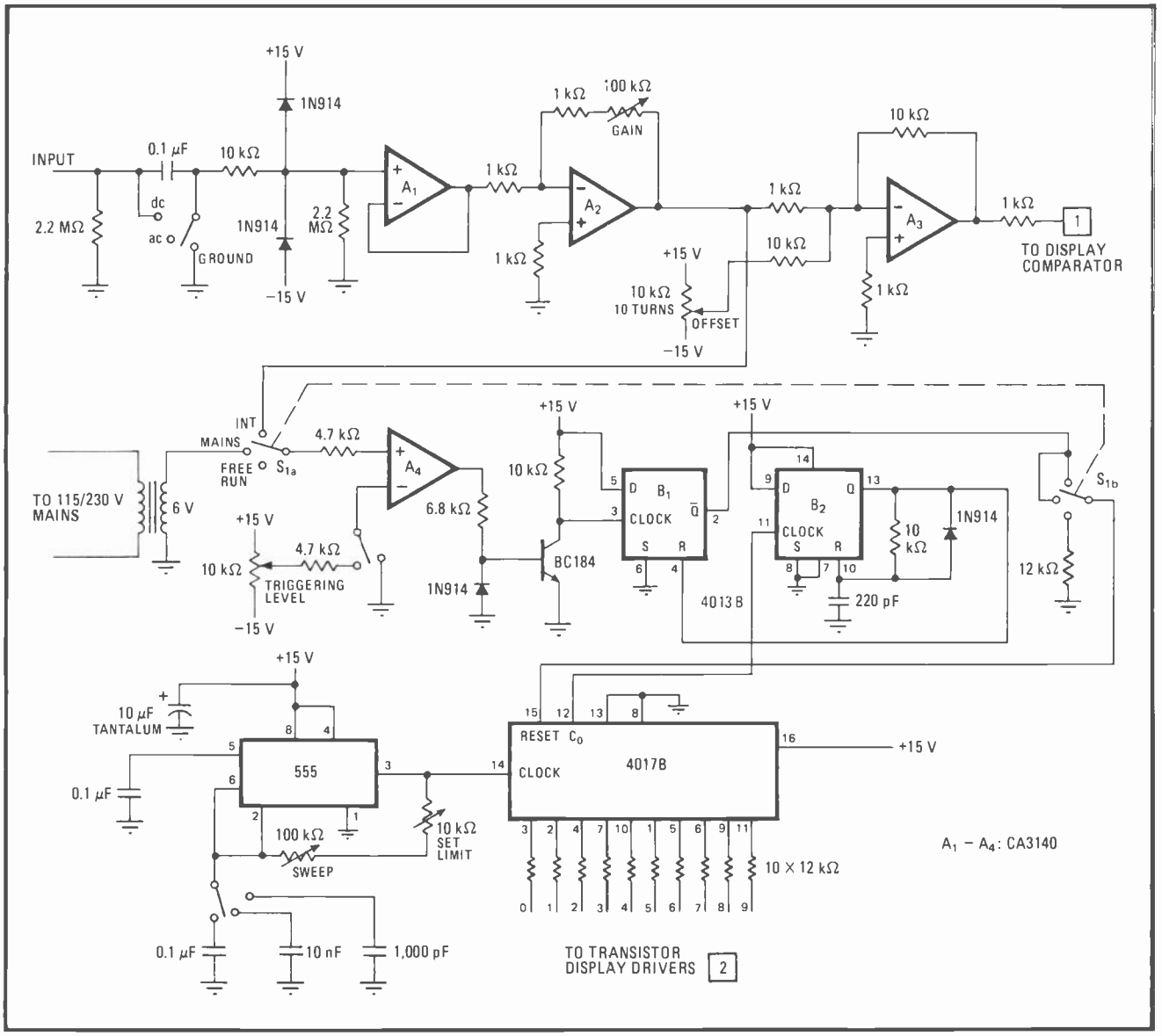
by Vernon Boyd

The Welding Institute, Abington, Cambridge, England

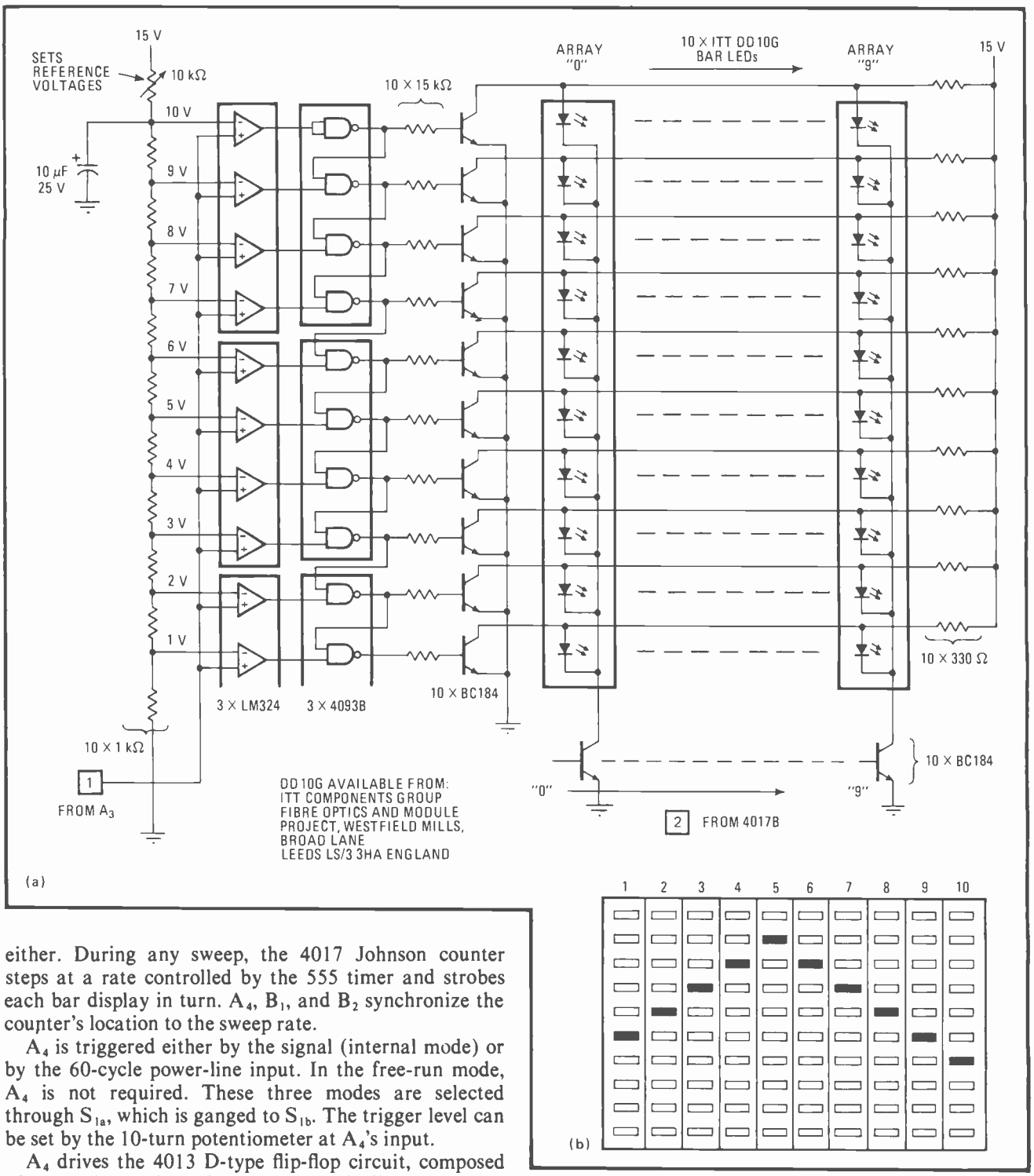
Building a small, low-powered, and low-cost oscilloscope for simple monitoring applications is easy, especially if light-emitting diodes are used in place of the cathode-ray tube. This circuit uses 10 bar displays, each containing 10 LEDs, to form a 100-dot viewing matrix. With this configuration, of course, resolution is only 10% in both the X and Y axes, but it can be improved by adding additional displays and expanding the driving circuitry.

As shown in Fig. 1, the signal-processing and logic circuits for the scope are straightforward. The signal-path circuit is extremely simple and has all of the options usually expected—ac and dc input coupling, variable Y-axis gain, and offset control. The signals to be observed pass through amplifier A_1, are amplified up to 100 times by A_2 and are inverted by A_3, and then pass through to the display comparator.

The trigger and timing circuits are not complicated,



1. Signal, timing, and logic. Driver circuits for scope's LED bar displays are straightforward. Input circuit can process ac or dc signals and has variable Y-axis gain control. $A_1 - A_3$ is input-signal path. A_4, B_1, and B_2 provide sync for 555 clock generator and 4017 counter, which strobes bar displays. Circuit has internal, free-run, or power-line triggering option. Maximum sweep rate with 555 is 10 kHz.



2. Display. Comparators, NAND gates, and transistors drive bar displays as each is strobed in succession (a). Amplitude of Y-axis signal determines which of 10 LEDs in each display is illuminated during sweep. Typical sine wave is displayed on 100-dot matrix (b).

either. During any sweep, the 4017 Johnson counter steps at a rate controlled by the 555 timer and strobes each bar display in turn. A_4, B_1, and B_2 synchronize the counter's location to the sweep rate.

A_4 is triggered either by the signal (internal mode) or by the 60-cycle power-line input. In the free-run mode, A_4 is not required. These three modes are selected through S_{1a}, which is ganged to S_{1b}. The trigger level can be set by the 10-turn potentiometer at A_4's input.

A_4 drives the 4013 D-type flip-flop circuit, composed of B_1 and B_2, through a transistor buffer. The 4013 ensures that triggering on repetitive waveforms will be reliable, for it is reset at the end of any display sweep by the final stage (C_0) of the 4017. This event causes B_2 to reset B_1, which in turn resets the 4017.

As shown in Fig. 2, the bar displays are driven by ten LM324 comparators and a ten-gate NAND decoder. The chain of reference voltages, each separated by 1 volt, are generated by a string of 10 resistors and a 10-kilohm calibration potentiometer. These resistance values must be changed to accommodate the Y-axis resolution required. For example, if there are 20 elements in the Y axis (two 10-bar displays vertically mounted one above the other), the resistances must be selected to provide 0.5-v increments. Also, the Y-axis expansion must be implemented with additional comparators and gates. The NAND gates ensure that only one LED can be activated at any given time.

Expansion of the X axis is a bit more elaborate, but

not overly difficult. Simply cascading additional 4017s will not do, however, as two output states will occur, one for each driver. Consequently, these states must be decoded using NAND gates.

The 555 clock generator will sweep at a maximum rate of 10 kilohertz. For faster sweeps, a different clock circuit is needed. The comparators' frequency limits must also be well above the sweep rate. □

Variable oscillator reacts to magnetic flux changes

by V. Vijayakumaran Nair
Vikram Sarabhai Space Center, Trivandrum, India

An oscillator employing a saturable-core reactor can detect small changes in the intensity of any magnetic field that cuts through the reactor's windings. The oscillator utilizes core hysteresis in order to generate a frequency that is directly proportional to the magnetic field component along the inductor's longitudinal axis.

As shown in (a), two 2N3020 transistors form a simple astable multivibrator that oscillates at a frequency of 11 kilohertz in the absence of an external magnetic field. The inductor, L, in the collector lead of Q_1 has a core made from μ metal, a commonly available, high-permeability magnetic alloy with the characteristics shown in (b). The μ metal consists of nickel, iron, copper, and manganese. Placed around it is an insulating layer of phenolic resin impregnated with paper or cloth, of a kind frequently used in coil forms. As shown in (c), 800 turns of AWG 36 wire, wound over the insulator, gives L a value of a few millihenries.

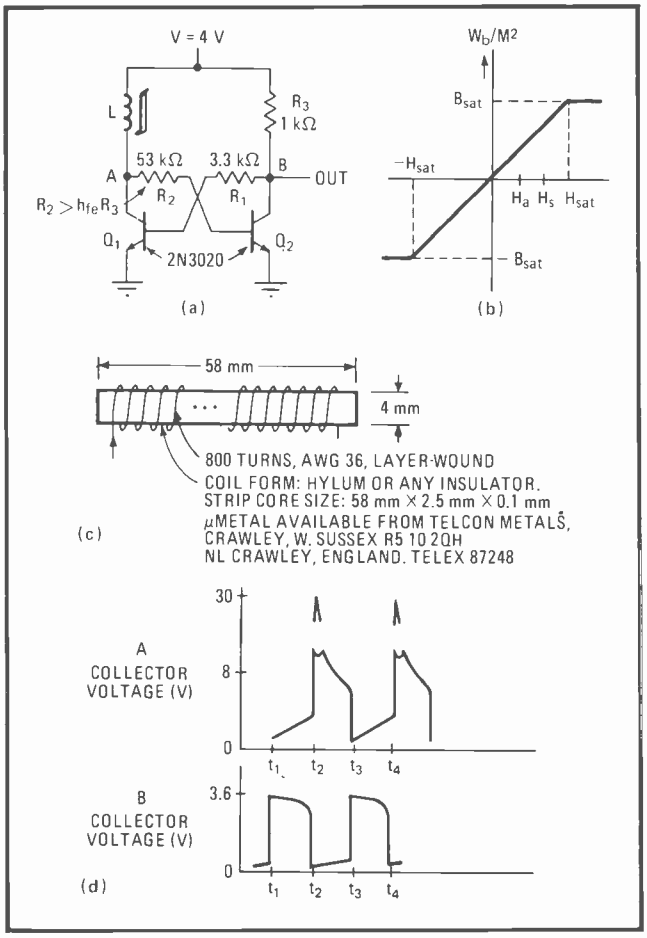
Circuit operation may be understood from (d). Disregarding any external field for the moment, and assuming an arbitrary start time of t_1, at which point Q_1 is on and Q_2 is off, current will build through L at the rate of $i=(V/L)t$, where V is the supply voltage and t is the time. Generated in the coil is a magnetic field of intensity H_s, in a direction determined by the corkscrew rule. As the field increases, the level of flux density also increases. As t_2 approaches, the current rises to a value sufficient to saturate the μ metal (H_{sat}). The flux density reaches B_{sat} and remains at that value.

As a result, the inductance drops to that of an air-core inductor, because the core permeability is proportional to $\Delta B/\Delta H$. Thus, at t_2, the current increases almost instantaneously towards an infinite value, and as Q_1's base current is about $V/(R_1+R_3)$, too little to keep the transistor in conduction, Q_1 is eventually cut off.

The base current into Q_2, which is approximately equal to V/R_2, is not quite enough to turn this transistor on, however. But as Q_1 turns off, an induced electromotive force, much greater than V, is produced across the inductor, giving rise to enough additional current to turn Q_2 on and keep it conducting. Q_2 remains on until t_3, when the induced current, which has been falling from time t_2 with a rate equal to $-L/R_2$, finally decreases to near zero. The collector of Q_2 rises, bringing Q_1 into conduction, current builds in L, and the process repeats.

Consider an external field with intensity H_a along the axis of the coil such that the actual field causing a flux change is equal to $H_s \pm H_a$, depending on the direction of the external field. When H_a is opposing the field, the current takes longer to bring the total field to a value equal to H_{sat} between times t_1 and t_2; hence the oscillator's frequency will be lower than with no external field present. Similarly, when H_a is in the same direction as H_s, the core will reach saturation sooner, and the cycle will be speeded up, causing a rise in frequency.

The frequency will increase from 8 to 14 kHz for an external field change of ± 0.4 oersted. This change can be obtained merely by rotating the coil in a horizontal plane from the east–west to the north–south direction of the earth's magnetic field. □



Field sensitive. Saturable core reactor enables oscillator to detect change in any magnetic field whose flux lines cut reactor windings (a). Oscillator frequency is determined by the core saturation time (b). Inductor is made of μ metal, insulated core form, and 800 turns of high-gauge wire (c). Timing diagram details operation (d).

What designers should know about data-converter drift

Understanding the components of worst-case degradation can help in avoiding overspecification

by Paul Prazak
Burr-Brown Research Corp., Tucson, Ariz.

☐ Exactly how inaccurate will a change in temperature make an analog-to-digital or digital-to-analog converter? As designers are well aware, a 12-bit device may provide a much lower accuracy at its operating-temperature extremes, perhaps only to 9 or even 8 bits. But for lack of more precise knowledge, many play it safe (and expensive) and overspecify.

Yet it is fairly simple to determine a converter's absolute worst-case degradation from its various drift specifications. Considering these specifications separately and examining their basis will help to unravel the labyrinth of converter drift and show how to go about calculating the actual worst-case drift error for most devices.

Accuracy drift for a d-a converter or a successive-approximation a-d converter has three primary components: its gain, offset, and nonlinearity temperature coefficients. Instead of calling out the gain and offset drifts separately, some manufacturers specify a full-scale drift, which takes both into account. Another important specification in many applications is differential nonlinearity, which reflects the equality (or rather, the inequality) of the analog steps between adjacent digital codes. But, since this parameter is really describing only the distribution of the linearity error, its temperature coefficient does not contribute to the converter's worst-case accuracy drift.

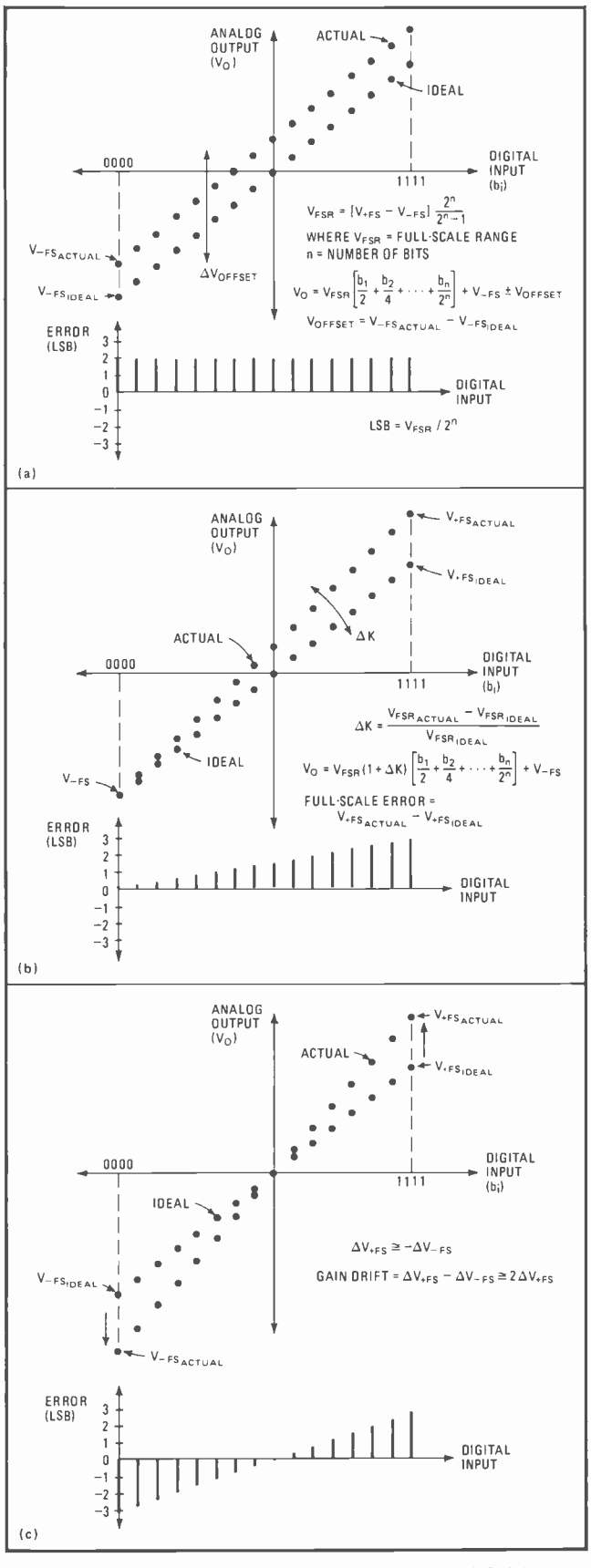
Examining the components of drift

The transfer function of a d-a converter will illustrate how the different kinds of drift degrade accuracy.

In a bipolar d-a converter, which produces both positive and negative analog voltages, offset drift changes all the output voltages by an equal amount, moving the entire transfer function up or down from the ideal in parallel to it (Fig. 1a). The drift of the converter's voltage reference is the main cause of this error—which may also be called the minus-full-scale drift, since it occurs even when all the input bits are logic 0 or off. In a unipolar unit, the offset drift is usually much smaller, being due mostly to drift in the offset voltage of the output operational amplifier and secondarily to leakage in the current switches.

Unlike offset drift, gain drift rotates the transfer function (Fig. 1b). In a bipolar unit it does so around minus full scale (all bits off), and in a unipolar unit it does so around zero (again all bits off). The gain drift affects each output voltage by the same percentage (not the same amount), tipping the transfer function at an angle to the ideal. In general, about 70% of this drift is caused by the drift of the converter's voltage reference.

Obviously, then, reference drift is a major contributor to total inaccuracy due to gain and offset drift. A positive temperature coefficient for the reference causes the transfer function to rotate about zero, as shown in Fig. 1c for a bipolar converter. Since the gain and bipolar offset drifts due to the reference will always be opposite in direction, the worst-case accuracy drift may be less than half the sum of the individual drift specifications. In a unipolar converter, the gain and offset drifts may well add together, but the unipolar offset drift is usually insignificant compared to the magnitude of the



1. Effects of drift. For a bipolar d-a converter, offset drift (a) moves the unit's transfer function up or down, whereas gain drift (b) rotates it about digital zero. Both of these errors are chiefly due to reference drift (c), which causes a rotation about analog zero.

gain drift, so it is not so important a factor.

Full-scale drift describes the change in the output voltage when all the bits are on. For a unipolar converter, it is simply the sum of the offset and gain drifts. In contrast, for a bipolar converter, the full-scale drift is the sum of half the reference drift, the gain drift exclusive of the reference, and the offset drift exclusive of the reference, or unipolar offset drift.

Poor tracking causes linearity drift

Finally, linearity drift reflects the shift in the analog output voltage from the straight line drawn between the output value when all the bits are off (minus full scale) and the output value when all the bits are on (plus full scale). This error is caused by the varying temperature coefficients of the ratio resistances of the converter's current-weighting (scaling) resistors, as well as the ratio drifts of the base-emitter voltages and betas of its transistor current switches.

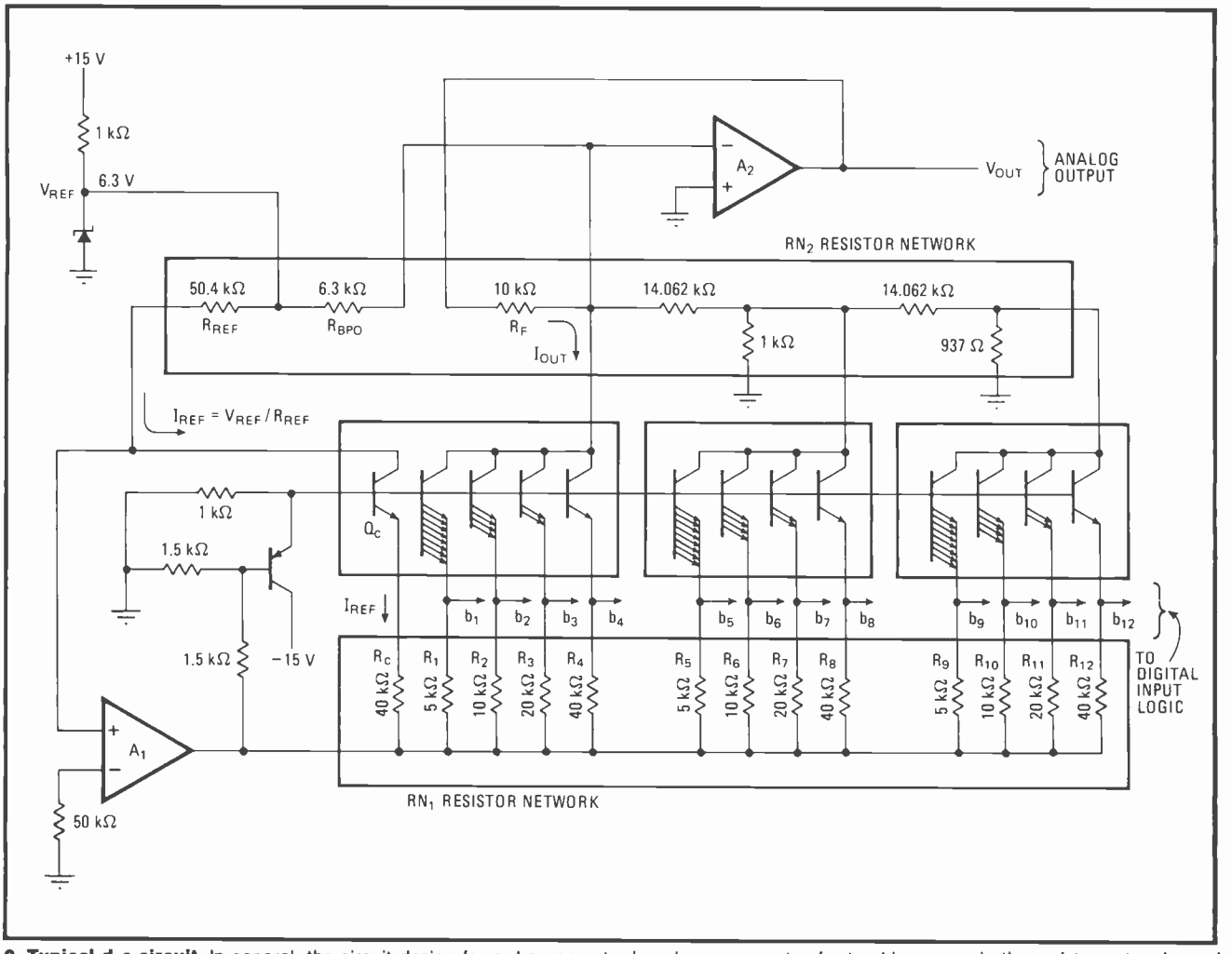
Since the change in linearity with temperature depends on how closely various parameters track each other, and not on absolute parameter values, it is fairly easy to control with present-day hybrid and monolithic technologies. As a result, linearity drift is usually much smaller than either the gain or offset drift. Moreover, it is generally guaranteed to be within some maximum limit over the converter's full operating temperature range.

Another specification that is important in some applications is bipolar zero drift, which reflects the change in the output voltage of a bipolar converter at midscale, when only the most significant bit is on and all other bits are off. This drift error at zero is not affected by reference drift at all, but is caused mainly by poor tracking in the converter's scaling resistors and current switches. Therefore, it appears as a random variation about zero, and it has a worst-case magnitude equal to the offset drift exclusive of the reference plus half the gain drift exclusive of the reference.

To understand more fully how these drift errors are generated, consider the simplified schematic (Fig. 2) of a typical 12-bit bipolar d-a converter. Circuit operation is fairly simple. The reference current flows through reference transistor Q_c, producing a voltage drop across resistor R_c. Since the base of Q_c is connected to the bases of all the other transistor current switches, the same potential is also generated across resistors R_1 through R_{12}. The multiple emitters of the transistors cause current density to be the same for each of these binarily weighted current sources, thereby providing good matching and tracking of the transistors' V_{BE} and β.

Tracking errors tend to cancel

Now suppose that, because of temperature or aging, the value of every resistor on network RN_1 increases by 1%. Since the reference current remains constant, the voltage across these resistors also increases by 1%, so the output current and the output voltage are unchanged. If, instead, the values of all the resistors on network RN_2 increase by 1%, the reference current decreases by 1%, reducing the voltage across R_c by 1% and causing the output current to drop by 1%. However, since the value



2. Typical d-a circuit. In general, the circuit design for a d-a converter largely compensates for tracking errors in the resistor networks and transistor current switches. By far the dominant error source is the drift of the zener diode that makes up the reference.

of the feedback resistor, R_F, is now 1% higher, the output voltage, which is equal to $I_{OUT}R_F$, does not change.

The converter compensates for variations in transistor V_{BE} and β in the same manner. Although the individual resistors on RN_1 and RN_2 may have temperature coefficients as high as ±50 parts per million per degree Celsius, the tracking of these resistors, and therefore their contribution to drift in linearity and gain, is typically as little as 1 to 2 ppm/°C. In fact, the only error sources for which the circuit does not compensate are the drifts in offset voltage and offset current of amplifiers A_1 and A_2, as well as the drift of the zener reference diode. By far, the dominant error source is the drift of this zener, while the offsets of A_1 contribute to the gain drift exclusive of the reference, and the offsets of A_2 contribute to offset drift exclusive of the reference.

The effect of reference drift

To evaluate the effect of variations in the reference voltage on the overall accuracy of the converter requires determining the variation in output voltage for a change in ambient temperature. A good first-order approximation is to assume that all other drift errors—those due to tracking errors and random variations—are zero.

Writing the node equation for the summing junction at the inverting input of amplifier A_2 yields:

$$\frac{V_{OUT}}{R_F} + \frac{V_{REF}}{R_{BPO}} - \frac{V_{REF}}{R_{REF}} K\left[\frac{b_1}{2} + \frac{b_2}{4} + ... + \frac{b_n}{2^n}\right] = 0$$

where K is a gain constant, and b_1 through b_n represent the digital bits, which are either 1 or 0, depending on whether a bit is on or off. This equation may be used to determine the output voltage for any digital input.

At minus full scale, with $b_1 = b_2 = ... = b_n = 0$, the output voltage becomes:

$$V_{OUT} = V_{-FS} = -\left[\frac{R_F}{R_{BPO}}\right] V_{REF}$$

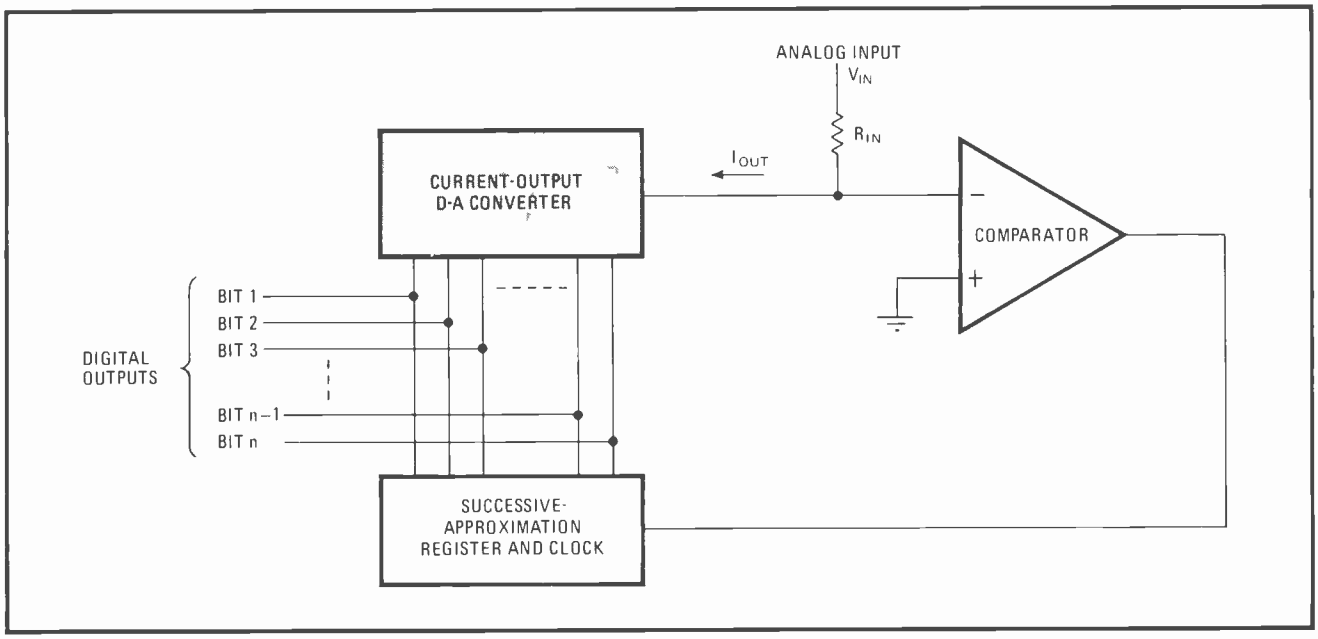
At bipolar zero ($b_1 = 1$, $b_2 = b_3 = ... = b_n = 0$), the output voltage for an ideal converter is equal to zero:

$$V_{OUT} = V_{BPZ} = 0 = \left[\frac{R_F}{2R_{REF}} K - \frac{R_F}{R_{BPO}}\right] V_{REF}$$

At plus full scale, with $b_1 = b_2 = ... = b_n = 1$, the output voltage becomes:

$$V_{OUT} = V_{+FS} = \left[\frac{R_F}{R_{REF}} K - \frac{R_F}{R_{BPO}}\right] V_{REF}$$

Solving the equation for V_{BPZ} for gain constant K yields:



3. A-d converter. All of the relationships that apply to the drift errors in a d-a converter also hold for a successive-approximation a-d converter, since this component includes a current-output d-a converter as one of its circuit blocks, as shown here.

$$K = \frac{R_F}{R_{BPO}} \frac{2R_{REF}}{R_F} = \frac{2R_{REF}}{R_{BPO}}$$

Substituting this expression for K in the appropriate equations, the variation in output voltage for a change in the reference caused by temperature may be computed. At minus full scale, this drift is:

$$\frac{\Delta V_{-FS}}{\Delta T} = -\frac{R_F}{R_{BPO}} \frac{\Delta V_{REF}}{\Delta T}$$

where ΔT is the change in ambient temperature. As mentioned previously, drift error at midscale is caused by tracking errors, not by variations in the reference, so:

$$\frac{\Delta V_{BPZ}}{\Delta T} = 0$$

At plus full scale, the change in the output becomes:

$$\frac{\Delta V_{+FS}}{\Delta T} = \frac{R_F}{R_{BPO}} \frac{\Delta V_{REF}}{\Delta T}$$

Therefore, the drift in the output voltage due to reference variations at minus full scale (or the bipolar offset drift) will be equal in magnitude but opposite in direction to that at plus full scale. Each of these drift errors amounts to half the reference drift. The gain drift due to reference variations may be written as:

$$(\Delta V_{+FS} - \Delta V_{-FS})/\Delta T$$

which is equal to the reference drift. It should be noted that the gain and reference drifts are specified in ppm/°C, while the full-scale and offset drifts are in ppm of full-scale range (FSR) per °C.

Computing the worst-case error

These results may now be used to find the worst-case total accuracy drift error for the typical converter of Fig. 2. Suppose the maximum temperature coefficient of the device's internal reference is ±20 ppm/°C, resulting in a gain drift of ±20 ppm/°C, a plus-full-scale drift of ±10 ppm of FSR/°C, and a bipolar offset drift of ±10 ppm of FSR/°C. The maximum gain drift exclusive of the reference is ±10 ppm/°C, and the offset drift exclusive of the reference is ±5 ppm of FSR/°C.

The worst-case error occurs at plus full scale. To compute it, the errors due to the reference as well as those exclusive of the reference that are due to random variations must be taken into account. Therefore, the only contributors to the worst-case full-scale accuracy drift are the plus-full-scale drift due to the reference, and the random errors of the offset drift and the gain drift exclusive of the reference. Summing these together yields a worst-case full-scale accuracy drift of ±25 ppm of FSR/°C or ±0.0025% of FSR/°C.

The converter is a 12-bit device having a linearity error of ±½ least significant bit, or ±0.01%. Also, for its operating temperature range of 0°C to 70°C, the maximum excursion from room temperature (25°C) will be 45°C. Assuming that gain and offset errors are adjusted to zero at room temperature, the total accuracy error may be computed as the sum of the linearity error and the full-scale accuracy error:

$$\begin{aligned}\text{worst-case total accuracy error} &= (\text{linearity error}) \\ &\quad + (\text{full-scale accuracy error}) \\ &= (\pm 0.01\%) + (\pm 0.0025\%/°C)(45°C) \\ &= \pm 0.12\%\end{aligned}$$

which is about 9-bit accuracy. The accuracy for many 12-bit d-a converters will typically be twice as good as this, with most devices providing 10-bit accuracy.

All of the drift relationships and causes examined in this article also apply to a successive-approximation a-d converter, which uses a d-a converter as one of its circuit blocks, as shown in Fig. 3. In the equations, simply substitute V_{IN} for V_{OUT} and R_{IN} for R_F. Also, in the a-d converter, comparator drift, rather than op-amp drift, contributes to the device's unipolar offset drift. □

Chip delta modulators revive designers' interest

Applications go beyond telecommunications into filters, speech scramblers, instruments, and remote motor control

by Raymond Steele, *University of Technology, Loughborough, Leics.*

☐ Conceived originally as a simpler alternative to pulse-code modulation, delta modulation never overcame PCM's head start. It met with success mainly in specialized military digital telecommunications systems because of its ability to perform well in the presence of many transmission errors. But the use of large-scale integration to produce delta modulator chips costing as little as $6 is opening up new areas of applications. The devices are even versatile enough for a host of non-telecommunications applications, in programmable digital filters, for remote motor control and speech scrambling, and in a variety of instruments.

Available from several manufacturers, these delta modulator integrated circuits need very few external components to encode analog signals into binary ones and vice versa. They replace all the active components of existing audio delta modulators, leaving the designer to supply only a clock signal, the supply voltage, and some external resistors and capacitors. At present the chips come in ceramic dual in-line packages, but less expensive plastic packages are just around the corner.

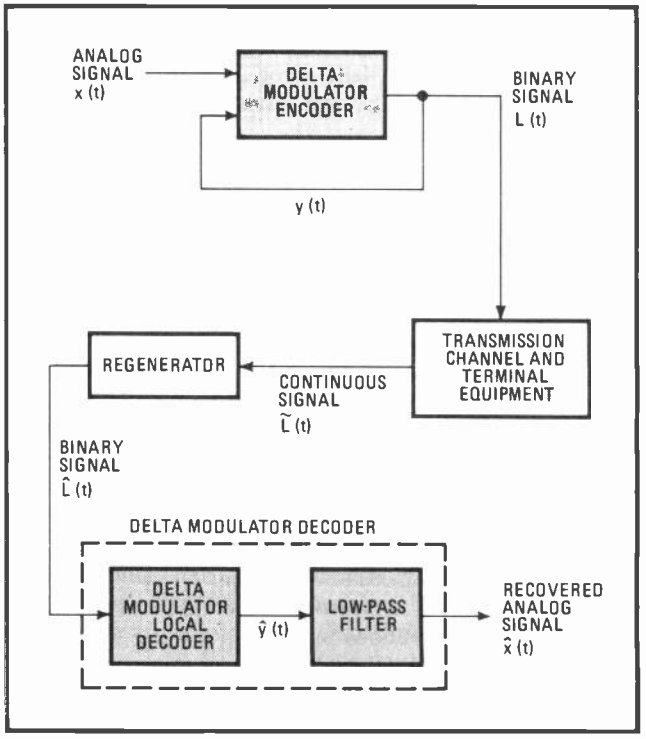
Principles of delta modulation

Like the PCM system, a delta modulation system consists basically of an encoder and a decoder, commonly called a codec. A PCM encoder samples the amplitude of a continuously varying signal at regular intervals and represents these samples by binary words. In contrast, a delta modulator generates single-bit words that represent the quantized error in a tracking signal rather than the actual input signal. (See table for a more detailed comparison.)

In essence, a delta modulator is a closed-loop sampled-data control system that transmits binary output pulses whose polarity depends on the difference between the input signal being sampled and a quantized approximation of the preceding input signal. In the transmission network of Fig. 1, the system tracks analog input signal x(t) with quantized feedback signal y(t) and encodes the difference between them into binary waveform L(t). After passing through the terminal equipment and transmission channel, the binary signal emerges at the receiver as a continuous signal $\tilde{L}(t)$, from which the regenerator reproduces the binary signal $\hat{L}(t)$. (Theoretically, $\hat{L}(t)$ is identical to L(t), but in practice it contains transmission errors due to noise, nonlinearity and disper-

DELTA MODULATION AND PULSE-CODE MODULATION COMPARED

Characteristic	Modulation	
	Delta	PCM
Ability to time-share encoder among multiple channels	unsuitable	suitable
Dependence on frequency components of signal being encoded	overloads in presense of high-amplitude, high-frequency components	independent
Cost	lower than pcm	more than delta
Word synchronization requirement	no	yes
Tolerance to transmission errors	good	poor
S/n ratio at low transmission bit rates	higher than PCM	–
S/n ratio at high transmission bit rates	–	higher than delta
Suitability for encryption	better than PCM	–
Requires accurately synchronized transmitter and receiver for signal channel transmission	no	yes
Filter requirements	simple	complex



1. Simple system. A delta modulator produces a single binary signal L(t) from an analog input signal x(t). The binary signal, degraded by transmission, is reshaped by the regenerator, decoded, and then filtered into a close replica of the original analog signal.

sion in the transmission channel and regenerator.) $\hat{L}(t)$ is decoded back into $\hat{y}(t)$, and from $\hat{y}(t)$ a continuous signal, $\hat{x}(t)$, is recovered. (Transmission errors and quantization effects generated in the delta modulator make $\hat{x}(t)$ different from $x(t)$.)

Linear delta modulation systems

The newer types of delta modulation systems adapt the step size of the feedback signal to the amplitude of the input signal, to ensure good tracking over wide ranges of input signal amplitudes. But the original and simplest form, linear delta modulation, keeps the step size of the feedback signal constant. (All delta modulators are actually nonlinear systems, but they are called linear when the local decoder producing the feedback is a linear network.)

The linear delta modulator shown in Fig. 2a uses an integrating network in its feedback loop to locally decode binary signal $L(t)$ and turn it into the multilevel waveform shown in Fig. 3. This feedback signal $y(t)$ tracks input signal $x(t)$ in the attempt to minimize the error signal, $e(t) = x(t) - y(t)$. If $e(t)$ is equal to or greater than 0, then a zero-crossing detector, called a quantizer, produces a positive voltage level, $+V$, but when $e(t)$ has a value that is less than 0, the quantizer produces a negative voltage level, $-V$.

Comparison of $x(t)$ and $y(t)$ occurs once every clock period, T. If at that instant the input signal is the larger (or at any rate not the smaller) of the two, binary output $L(t)$ becomes $+V$ for the duration of T. Integration of $+V$ increases feedback signal $y(t)$. This continues until at some later clock instant $y(t)$ exceeds the input signal. Then error signal $e(t)$ becomes a negative quantity and $L(t)$ changes from $+V$ to $-V$, and so on.

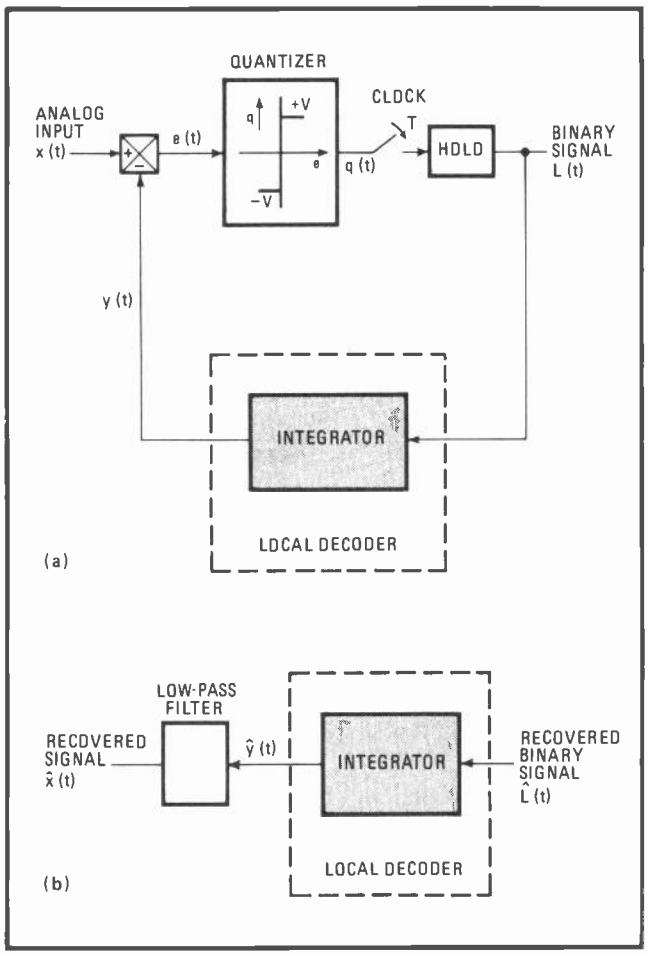
The linear delta demodulator shown in Fig. 2b consists of a local decoder followed by either a low-pass or bandpass filter. The local decoder produces $\hat{y}(t)$, which in the absence of transmission errors would be identical to $y(t)$. From Fig. 3 it can be seen that $y(t)$ approximates $x(t)$. A filter with a cutoff frequency, f_c, that is much lower than $1/T$ smooths out discrete changes in the slope of $\hat{y}(t)$, removing out-of-band quantization noise to recover $\hat{x}(t)$, which is approximately equal to $x(t)$.

As indicated earlier, the difference between the original and reconstructed analog signals is due in part to noise introduced by the quantizer. Often called granular noise, it can be decreased by increasing the sampling frequency and/or decreasing the magnitude of the step size γ. But note that the delta modulator must generate some quantization noise in order to produce the binary positive and negative voltage levels. In practice, no quantizer can produce an instantaneous change in the vicinity of zero; the change is gradual and consequently the error must be large enough to produce either $+V$ or $-V$ at the quantizer output.

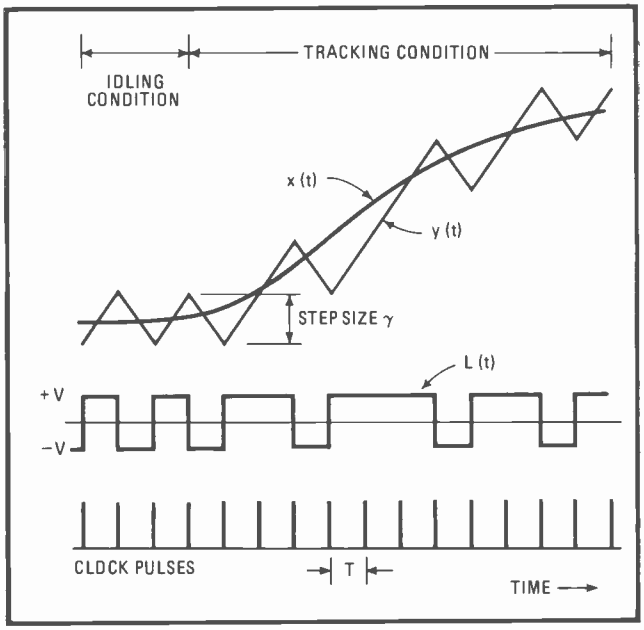
Other considerations

Several parameters such as idle-channel noise, slope overload, and signal-to-noise ratio must be considered because of their effect on the overall performance of a delta modulation system.

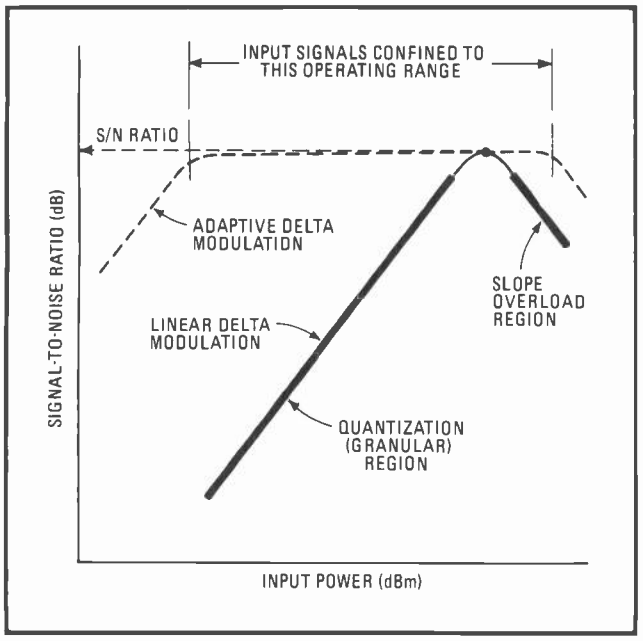
Unless care is taken in the design of the delta modula-



2. Linear delta modulation system. The encoder (shown at top) comprises a subtractor circuit, quantizer, sampling circuit, holding circuit, and local decoder, which is essentially an integrator. The decoder (bottom) needs only a local decoder and low-pass filter.



3. Watching waveforms. With no input, the tracking signal y(t) is a series of triangular waveforms corresponding to a binary signal L(t) of equal and opposite levels. In the tracking condition, the feedback signal attempts to track input signal x(t).



4. Signals and noise. The ratio is relatively constant in an adaptive delta modulation system, but in a linear delta modulation system it depends on signal level. At low input power, quantization noise predominates; a steeply sloping input produces slope overload noise.

tor, the decoded signal will not be zero when no analog input signal is present at the encoder. This unwanted noise signal is called idle-channel noise.

With no idle-channel noise the binary signal, L(t), must consist of alternate positive and negative levels (logical 1s and 0s) at successive sampling instants. When L(t) is integrated at encoder and decoder, the resulting signals y(t) and $\hat{y}(t)$ will be triangular waveforms if no transmission errors exist. These idling waveforms are shown on the left-hand side of Fig. 3. Even though the recovered signal in the decoder is triangular, no components pass through the output filter because the fundamental frequency of the triangular waveform 1/2T is much higher than the cutoff frequency of the filter. But if because of some asymmetry in the encoder L(t) does not consist of alternating 1s and 0s, $\hat{x}(t)$ may not be 0. A nonzero value of $\hat{x}(t)$ when $x(t) = 0$ is known as idle-channel noise.

Slope overload

In delta modulation the rate of occurrence of each binary level is proportional to the instantaneous slope of the analog input signal. Should this slope increase or decrease so fast that the feedback signal can no longer track the input signal, a stream of output bits of identical polarity is generated by the encoder, which is then said to be in a state of slope overload. When this occurs the signal recovered at the output of the decoder may be very different from the original input signal.

The difference between these signals is the slope overload noise, which is generally much larger than quantization or granular noise. If waveform fidelity is essential, it is to be remembered that slope overload noise will cause more waveform distortion than quantization noise. Quantization noise, on the other hand, is perceptually more annoying in speech signals.

The s/n ratio decreases with increasing signal power after slope overload has occurred (see Fig. 4). This is because noise power then increases more rapidly than the signal power.

For low input powers, too, the s/n ratio is low. The tracking is very poor because the feedback signal y(t) makes substantial variations about the small input signal and its comparatively large step size creates a significant quantization noise.

But as the input power increases, the s/n ratio improves in a linear fashion, for now quantization noise is substantially independent of the input signal. The ability of the encoder to track the input signal is progressively enhanced with increasing input power, and the improvement in s/n ratio continues until the encoder is slightly slope-overloaded.

Two applications

Figures 5 and 6 show two ways of implementing linear delta modulation systems. Both are laboratory models. One is a low-speed encoder for speech (Fig. 5), and the other is a high-speed model for TV signals (Fig. 6).

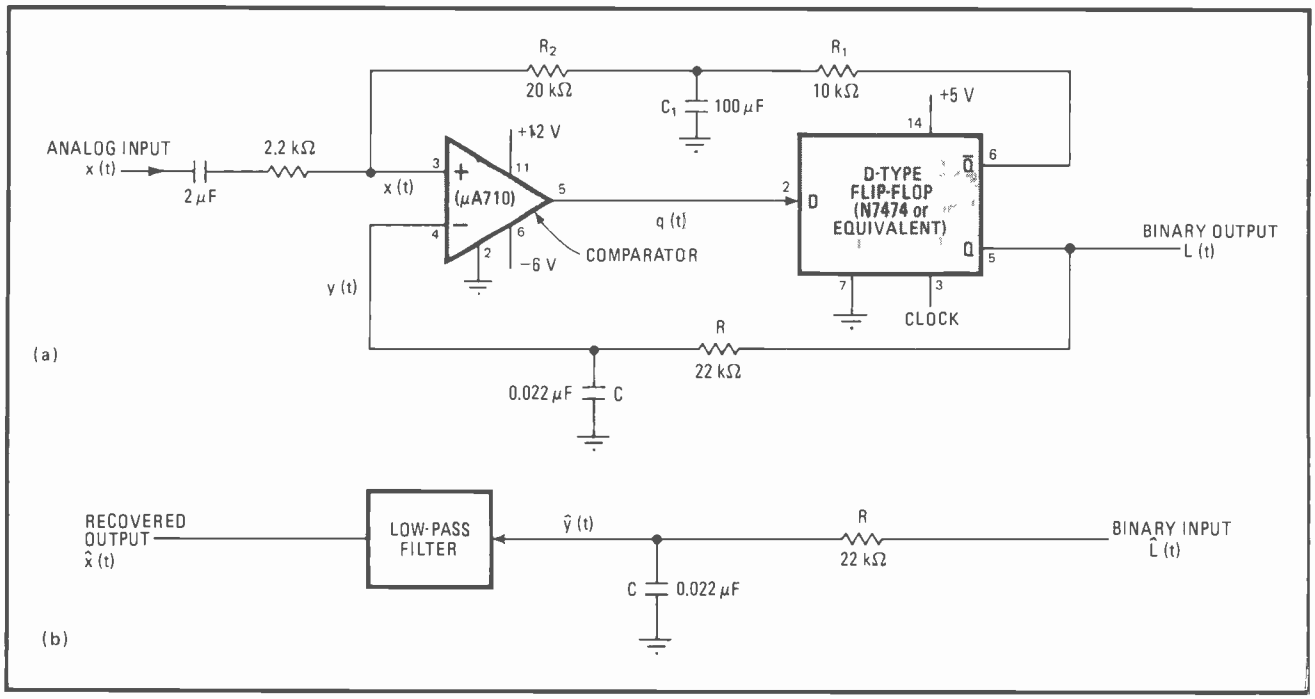
The simple D-type flip-flop of Fig. 5 implements the sample-and-hold circuit of Fig. 2. The circuit could function with a −2.5-volt and +2.5-v supply, but it is more convenient to use a single 5-v supply. The binary output signal L(t) from the Q output of the D-type flip-flop has voltage levels of approximately 0 and +4 v. When L(t) is integrated by the RC integrator, the mean value of y(t) is approximately +2 v.

The subtractor and quantizer functions are performed by an IC comparator. To ensure the encoder idles with the required pattern of alternate binary voltage levels at the output of the flip-flop, a dc voltage level of +2 v is applied to the noninverting input of the comparator via the idle channel's feedback network consisting of R_1, R_2, and C_1.

The input signal x(t) is added to the dc level on the noninverting input, and the sum is compared to the feedback signal y(t). The signal q(t) at the output of the comparator is high if x(t) is equal to or greater than y(t), and the Q output of the flip-flop is also high, thus charging capacitor C through resistor R. This process continues until at a particular clock instant x(t) is less than y(t). At that time, the Q output is low and C discharges, thus reducing the feedback voltage y(t). The process continues until x(t) is equal to or greater than y(t), and the cycle repeats.

For the high-speed encoder shown in Fig. 6, clock frequencies of 27 megahertz and 92 MHz were arbitrarily chosen to represent relatively high and low clock rates. In this circuit the separate comparator has been eliminated, its function being performed by the threshold circuitry associated with the D input of the flip-flop. The two 430-ohm resistors connected to this D input form a Kirchhoff adder, which sums the input signal x(t) and the feedback signal $\overline{y}(t)$. The feedback signal is formed by integrating the binary signal $\overline{L}(t)$ from the $\overline{Q}$ output of the flip-flop rather than using L(t). By integrating $\overline{L}(t)$ it is possible to add the feedback signal directly to the input signal x(t).

When the input signal is zero, the variable resistor R



5. Linear delta modulation. A comparator, D-type flip-flop, and a resistor-capacitor integrator are all that is needed for a low-speed linear delta modulation encoder. The delta modulation decoder requires only a simple RC integrator and a low-pass filter.

is adjusted to obtain the desired idling pattern at the output of the encoder. Approximately 50 ohms is needed for the circuit shown. When the error voltage e(t) is equal to or greater than the switching threshold V_T of the D-input circuitry, the $\overline{Q}$ output switches to the low-level state at the next clock pulse. This causes $\overline{y}(t)$ to decrease, and e(t) becomes less than V_T by the time the following clock pulse arrives. $\overline{Q}$ now switches to the high-level state, $\overline{y}(t)$ increases, and e(t) becomes equal to or greater than V_T at the next clock instant, and so on.

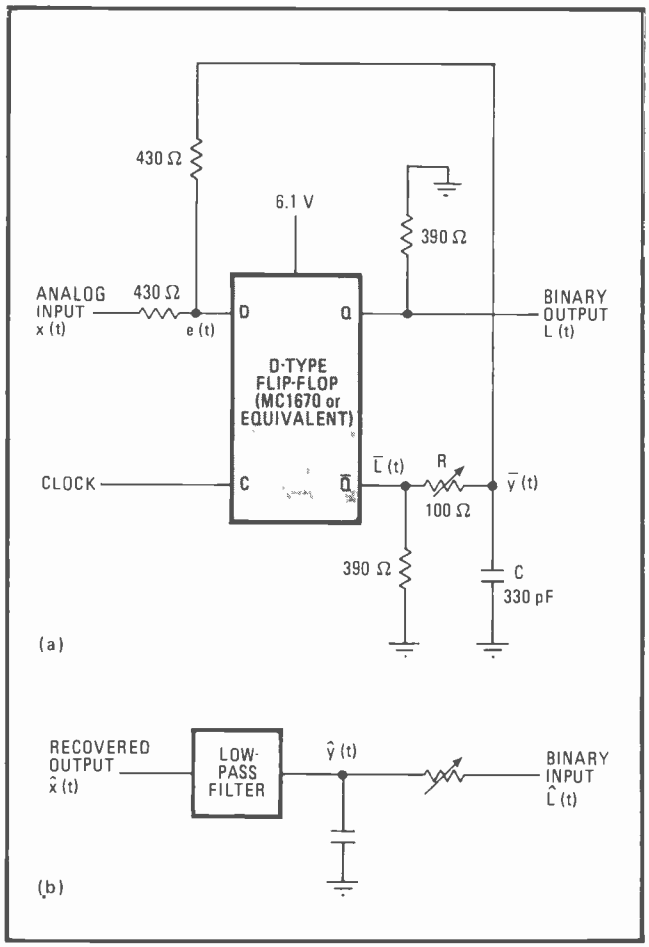
In tracking an input signal, the feedback loop attempts to maintain e(t) at V_T. If the input signal x(t) should suddenly increase, e(t) would be equal to or greater than V_T for as many clock periods as it takes for capacitor C to discharge and bring it below V_T. On the other hand, a decrease in x(t) causes e(t) to be less than V_T, and this drives $\overline{Q}$ to a high-level state, thus charging capacitor C. Consequently, e(t) increases until it is equal to or greater than V_T, and the cycle repeats.

The 390-ohm pull-down resistors are needed to accommodate the internal circuitry of the MC1670 flip-flop used. The decoder is simply an RC integrator followed by a low-pass filter. A third-order Butterworth type of filter was found to be acceptable when the analog signal is a composite PAL television signal and the clock rate is 92 MHz.

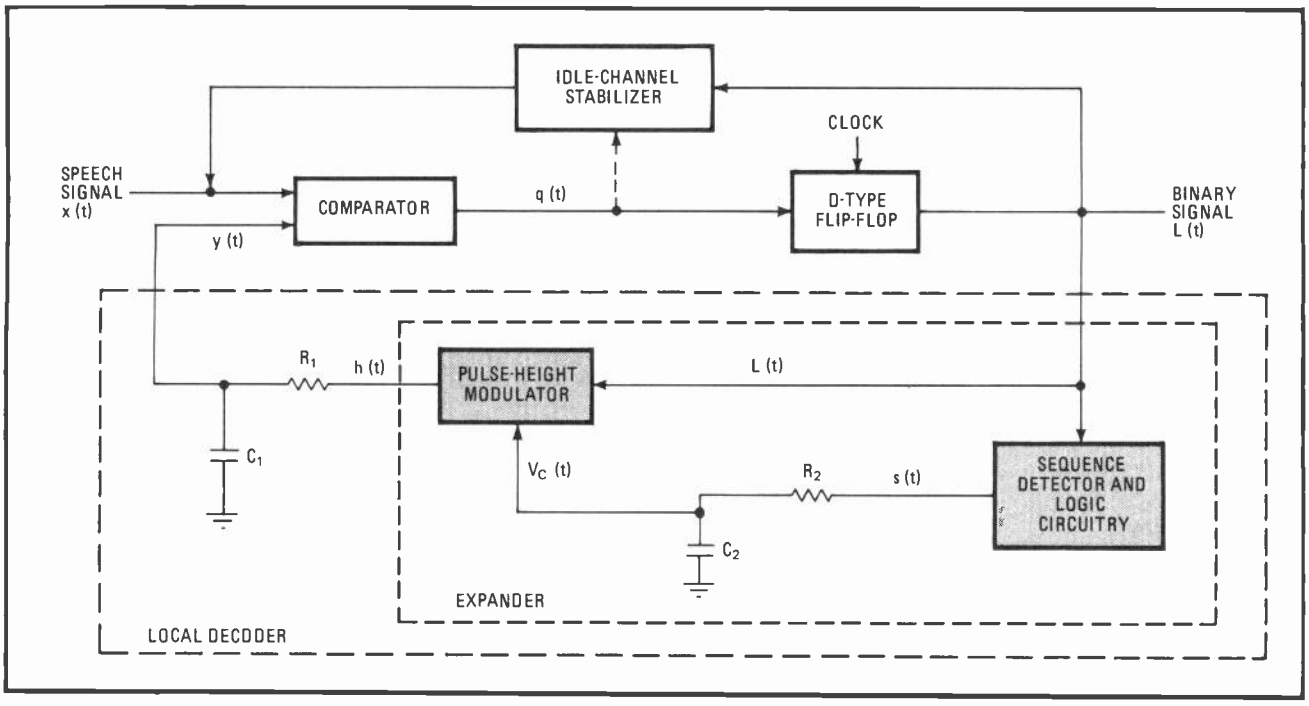
Companded delta modulation systems

A serious deficiency of linear modulation systems, both delta and pulse-code, is their inability to maintain a high s/n ratio over a wide range of analog input power. In telephone applications, for example, the varying power levels in the speech pattern of different subscribers produce significantly different s/n ratios.

Linear delta modulation systems employ a constant, or nearly constant step size in the feedback signal y(t).



6. High-speed linear system. Just two components, a D-type flip-flop and an RC integrator, provide the encoding functions. Here the D-type flip-flop replaces the comparator and sample-and-hold circuit of Fig. 2; an RC integrator and low-pass filter do the decoding.



7. Improving s/n ratio. A continuously variable slope delta (CVSD) encoder may be viewed as a collection of linear delta modulator encoders having different, but fixed, step sizes that between them provide a near peak signal-to-noise ratio over a wide dynamic range.

However, if the step size could be made small when the slope of the input signal x(t) is small, and large when the slope is steep, y(t) would track x(t) better over a wide range of input levels. As quantization noise depends on the square of step size, making the step size adaptable to input signal variations would make the noise power vary with signal power, rather than be independent of it as with linear delta modulation. Then with noise power proportional to signal power, the s/n ratio would be independent of signal power. This is what adaptive delta modulation does.

Many adaptive algorithms for changing the step size have been used,[1] but for telephony the type of adaptive delta modulation called continuous variable slope delta, CVSD, is the one most frequently used. Known also as digitally controlled or syllabically companded delta modulation, CVSD is mainly designed for handling a wide dynamic range of speech signals, although it can be used for other applications as well.

In the CVSD encoder shown in Fig. 7, the step height of the feedback signal y(t) is varied in a manner related to the envelope rather than the instantaneous value of the input signal x(t). Unlike the linear delta modulator, the input of the integrator R_1C_1 is not the output binary signal L(t), but a multilevel signal h(t) with pulses that have an amplitude H equal to $GV_c(t)$ (where G = the gain of the pulse height modulator), a duration T equal to the reciprocal of the clock rate, and the same polarity as L(t). The multilevel signal h(t) at the output of the pulse-height modulator, which is essentially a multiplier, is produced by multiplying the binary signal L(t) and the voltage $V_c(t)$, which is approximately the integral of the binary signal s(t) at the output of the sequence detector and logic circuitry.

The magnitude of the step size in the feedback voltage y(t) depends on the magnitude of $V_c(t)$, which depends on the level of the binary signal s(t). Various algorithms have been used to form s(t), but a popular one is to make s(t) equal to a voltage, V_H, if the current and previous two values of L(t) are identical. Otherwise, s(t) = V_L, which is much less than V_H, but of the same polarity.

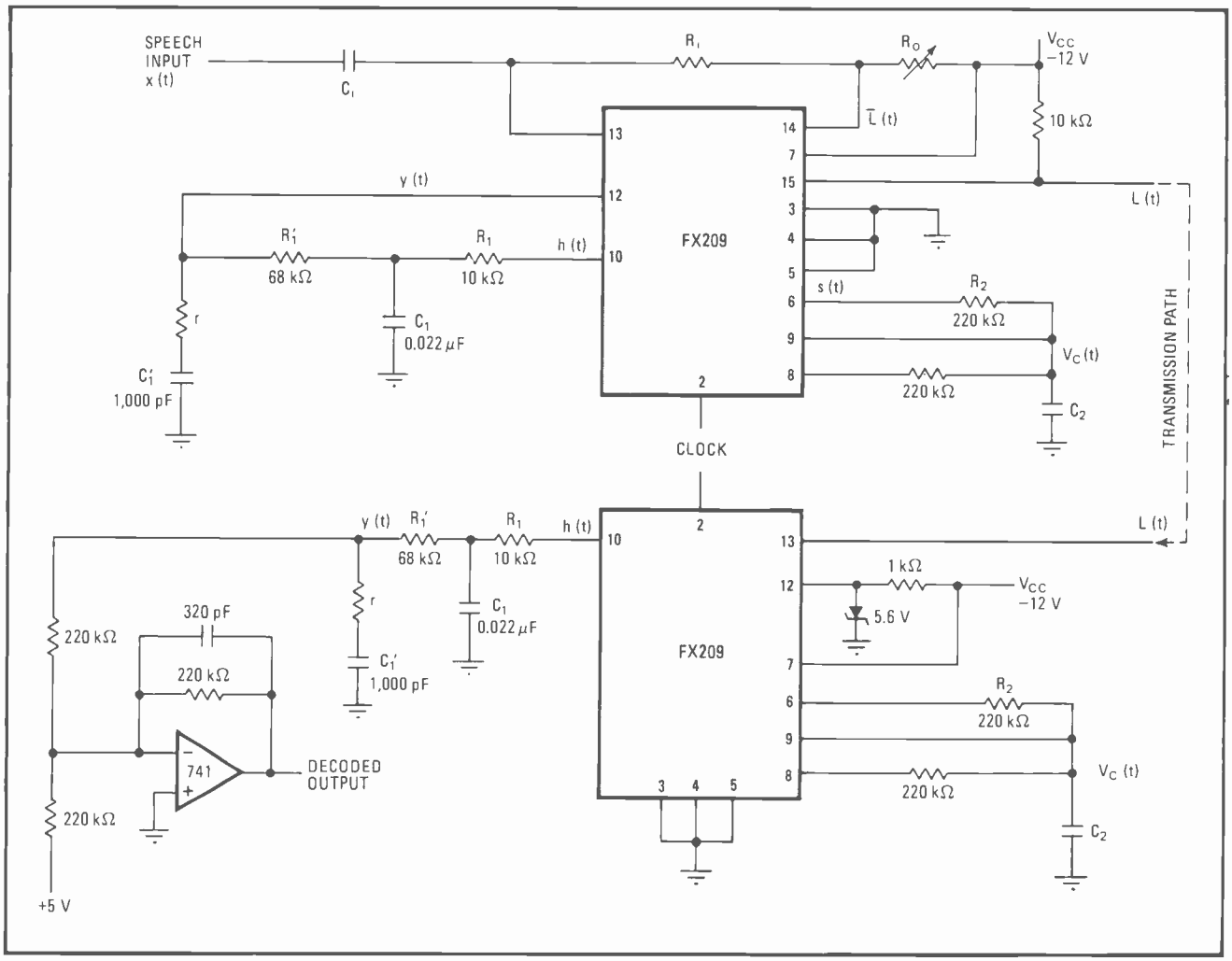
When the input analog signal x(t) is greater than y(t) for many clock periods, s(t) = V_H, and this voltage charges up C_2 via R_2. The voltage $V_c(t)$ exponentially approaches the value of V_H. Most values of R_2C_2 are 5 to 10 milliseconds, commensurate with a typical pitch period of voiced speech. But sometimes the time constant may be as high as 100 ms, which is comparable to the syllabic durations of speech. The value selected depends much on subjective preference.

The magnitude H of the pulses in h(t) also increases at a rate determined by R_2C_2, until y(t) is equal to or greater than x(t) at a clock instant when s(t) = V_L. Capacitor C_2 then discharges through R_2 and the output impedance of the logic circuitry. Consequently, the magnitude of step sizes in y(t) decreases exponentially until the input signal x(t) is again equal to or greater than y(t) at a clock instant, and so on.

Because the magnitude H of the multilevel signal h(t) varies slowly compared to the clock rate, the CVSD encoder behaves over many clock periods as a linear delta modulator. It can therefore be viewed as a collection of linear delta modulators, with different but fixed step sizes, that provide near peak s/n ratio for a wide range of input powers.

L(t) is a binary representation of a compressed speech signal x(t) and must be locally decoded for it to be possible to compare the feedback signal y(t) with x(t). Consequently, this decoding must involve an expansion of the analog signal contained in L(t).

When the speech signal x(t) = 0, $V_c(t)$ equals a small dc voltage, which is required along with the feedback



8. Building block. Putting together a CVSD encoder and decoder requires two integrated circuits, such as Consumer Microcircuits of America's FX209 delta modulator, along with several resistors and capacitors to provide the selected transmitted bit rate.

from the idle-channel stabilizer to establish the L(t) idle-channel pattern. The stabilizer can operate on binary signal L(t) or the output of the comparator, q(t).

The decoder at the receiver uses the same local decoder portion as the encoder, followed by a low-pass filter to remove out-of-band quantization noise.

CVSD chips a reality

Several manufacturers, such as Motorola, Harris, and Consumer Microcircuits of America, have produced single-chip CVSD encoders that can also be used as decoders. For example, the FX209 delta modulator IC, marketed by Consumer Microcircuits of America, Galesburg, Ill., contains all the active analog and digital circuitry necessary. The user need only connect resistors and capacitors to suit the application.

Figure 8 shows a CVSD system using two FX209 ICs and external resistors and capacitors selected for a transmitted bit rate of 32 kilobits per second. The multilevel binary signal h(t) is formed as previously described, but a double RC integrator is used to shape the overload characteristic of the CVSD encoder to the long-term spectral-density function of the speech input signal, thus increasing the s/n ratio. Adding resistor r in the double integrator ensures the stability of the encoder.

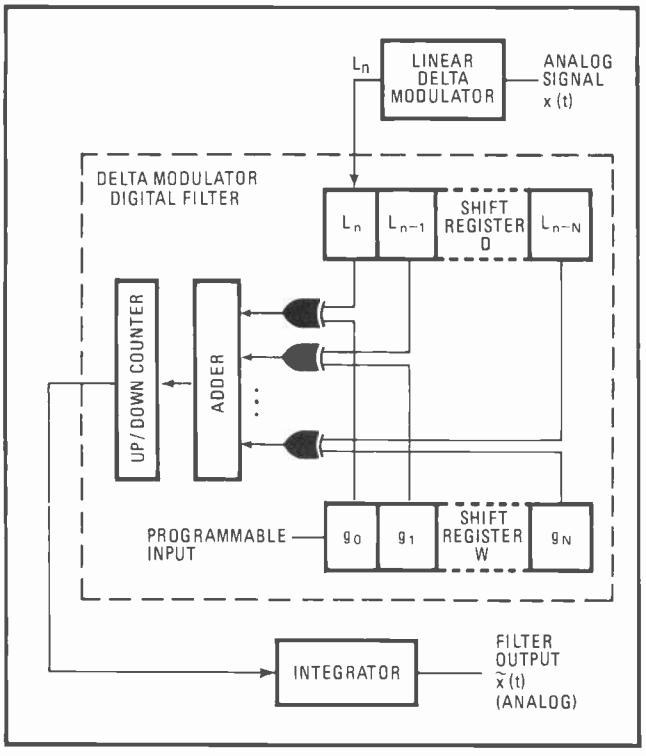
The idle-channel stabilizer of the encoder consists of C_i, R_i, and R_o. By making R_i greater than Z_{in}, the voltage input to the comparator (pin 13) is:

$$x(t) + \overline{L}(t)Z_{in}/R_i$$

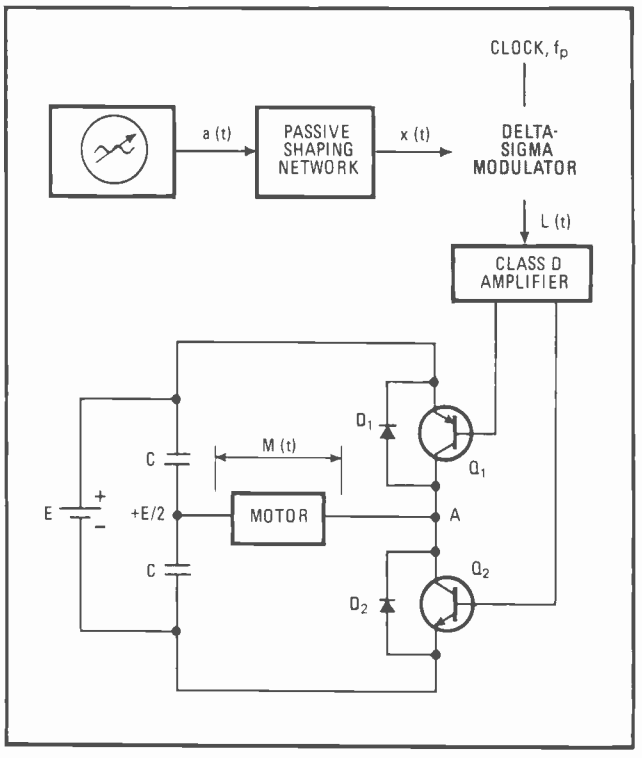
where $Z_{in} = 1/\omega C_i + Z_s$, and Z_s is the impedance of the speech source. With no input signal, resistor R_o is adjusted until the desired idle-channel pattern of alternate 1s and 0s is achieved. This occurs when $\overline{L}(t)Z_{in}/R_i = 0.45V_{cc}$ for the FX209.

When the FX209 is used as a decoder, the idle-channel loop is disconnected, and the binary signal L(t) is connected directly to the comparator in the device, which operates as a binary regenerator. The signal h(t) is recovered from pin 10 and passed through the double integrator to give y(t), the original speech signal, plus encoding noise superimposed on a dc level. The operational amplifier removes the dc component and acts as a low-pass filter having a cutoff frequency near the top of the speech band that reduces the out-of-band quantization noise.

Even if the main impetus for delta modulation has come from the telecommunications industry for binary encoding and decoding of speech signals, numerous other applications in industrial control, mobile communica-



9. Digital filter. Digital encoding and filtering using delta modulation techniques requires several components. The filter accepts a binary input from the delta modulator, and the overall filter properties are changed simply by reprogramming the input to shift register W.



10. Remote control. There is an advantage in using a delta-sigma modulator for the remote control of an induction motor—the speed-torque characteristics of the motor can be easily controlled even when it is separated from the controller by a noisy channel.

tions, and instrumentation exist as well. These applications include:

- Digital filters.
- Remote control of motors.
- Scrambling of speech signals.
- Encoding transient signals for storage and display.
- Compressing the amplitude range of an analog signal.
- Delaying an audio signal by different amounts to produce a reverberated sound.
- Encoding signals for acoustic modems.
- Encoding photographic profiles of objects for computer processing.
- Uses in instruments like voltmeters, wattmeters, etc.

A digital-filter circuit

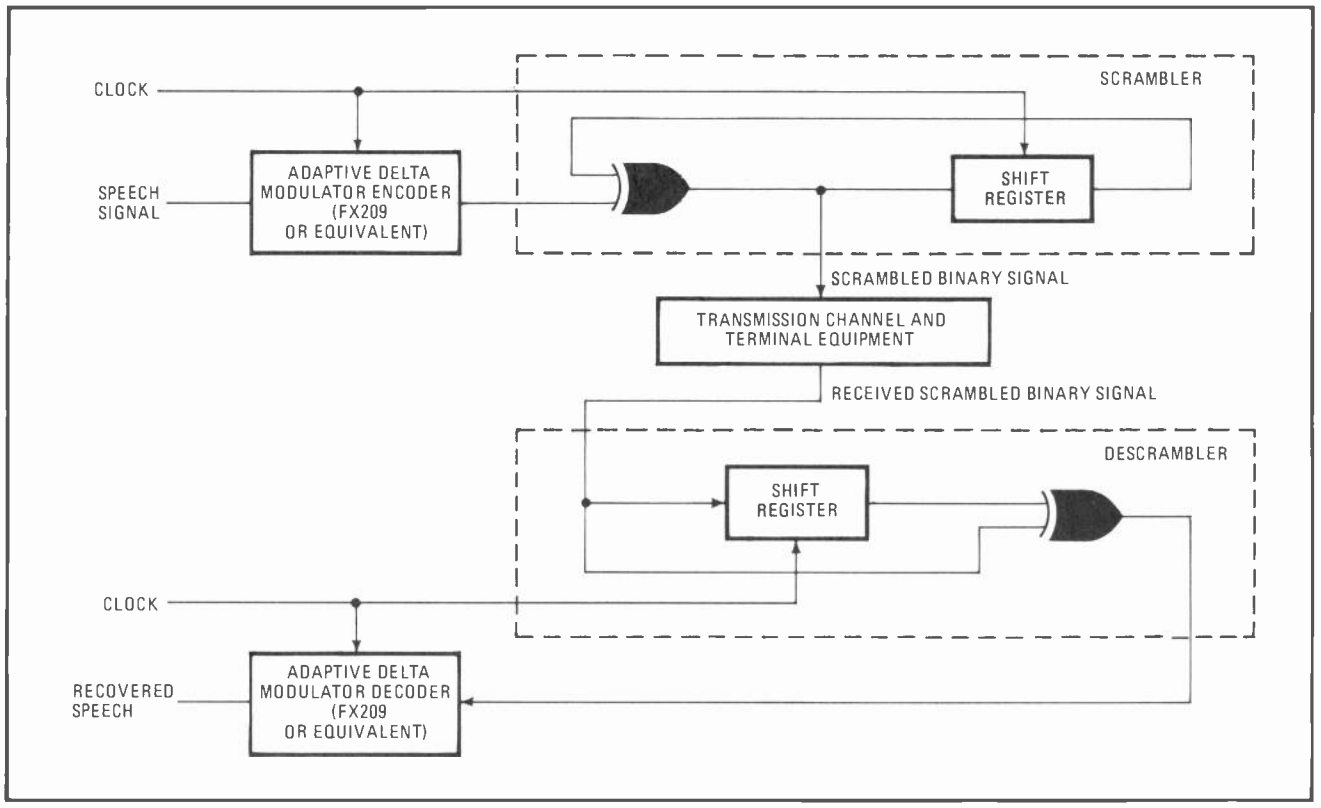
The integrator and analog filter used in previous linear delta modulator circuits are linear networks, and their order in the circuit can therefore be reversed. Provided the encoding conditions are good (high clock rate and small step size), the decoded $\hat{x}(t)$ is a close approximation to the input $x(t)$. Under these conditions the encoder and integrator in effect cancel, and the filter may be viewed as performing some filtering on the input signal $x(t)$. As the filter is now adjacent to the delta modulator output, it accepts a binary input, and hence it can be constructed as a digital filter. Now, by changing the properties of the filter, it is possible to turn $\hat{x}(t)$ into a filtered version of $x(t)$.

The circuit of Fig. 9 illustrates one of many digital filters using delta modulation techniques. The analog signal $x(t)$ is linear-delta-modulated. At the n^{th} clock instant, binary output level is L_n and shift register D contains current and previous N binary levels, L_n, $L_{n-1} \ldots L_{n-N}$. In a nonrecursive digital filter, each of these stored binary levels must be weighted and summed together. The weighting here is binary, and the levels are stored in the $(N+1)^{th}$-bit shift register W. The outputs of the exclusive-OR gates are summed in an adder, and the sum is accumulated in an up/down counter. The counter is necessary because of the binary nature of the weighting sequence $g_0, g_1 \ldots g_N$, which is the output binary sequency from an ideal linear delta modulation encoder when the input is the required multilevel weighting sequence. The contents in the counter are then integrated, or accumulated, as part of the decoding to recover the filtered signal $\tilde{x}(t)$. The counter and accumulator may be combined in a single circuit to eliminate the need for a separate integrator.

Motor control

Delta modulators can be used to control motor speed remotely by a binary signal that they transmit by either cable or radio link. As an induction motor viewed from its stator windings approximates a low-pass filter, it acts as a delta-sigma decoder. Thus a sine wave encoded into a binary waveform, amplified and applied to the stator windings, will cause the motor to respond as if a sinusoidal signal has been applied to it. Therefore, as far as the motor is concerned, a delta-sigma modulator and a binary class D amplifier behave like a linear amplifier having low odd-order harmonic distortion, a very desirable feature.

Figure 10 shows the configuration for controlling the speed-torque characteristic of an induction motor. A



11. Scrambling speech. Clocking a shift register along with an adaptive delta modulation encoder and adding an exclusive-OR gate provides a scrambled binary signal, which can be first unscrambled and then decoded by a similar setup at the receiving end of the link.

sinusoidal signal x(t) is encoded into a binary waveform L(t), is amplified, and produces binary signal M(t) having levels $\pm E/2$.

The motor speed for a constant torque depends on both the amplitude and the frequency of the sinusoidal input x(t). Varying the frequency of a constant voltage signal a(t) and adjusting its amplitude in the passive shaping network yields the x(t) signal required to satisfy the speed-torque criterion.

Two identical capacitors supply smoothing to protect the power transistors and to provide binary levels of $\pm E/2$ across the motor. When the binary signal L(t) is a 1, transistor Q_1 is switched on and transistor Q_2 is switched off. When Q_1 conducts, point A is connected to $+E$ volts, and the motor current can flow through Q_1 or D_1. When L(t) is a 0, the reverse occurs: point A becomes 0 volt and the motor current selects the appropriate path through Q_2 or D_2.

The security of speech transmissions is becoming increasingly important, and delta modulator ICs can easily be configured into simple speech-scrambler circuits (Fig. 11). Simply put, the speech signal is encoded by the delta modulator into a binary signal and then scrambled by an exclusive-OR gate and a shift register. This signal is then descrambled and decoded by a similar delta modulator circuit in the receiver.

The future of delta modulation is bright simply because of the spread of digital systems. However, its success is very much tied to the technology of large-scale integration, which allows complex adaptation algorithms to be used at relatively low cost. The availability of low-cost LSI circuits depends on the demand for delta modulators, and the size of that demand to some extent depends on how rapidly existing analog communication systems go digital. It seems likely that electronic exchanges for the telephone network may provide stimulus for these LSI devices.

Digital future

Exactly where in the telephone network these analog-to-digital and digital-to-analog converters will be introduced is still a matter for conjecture, but ultimately the complete telephone network will probably become digital, and the codecs will be placed in the local subscriber network. Also, it is possible that adaptive delta modulation codecs will be preferred to the log-PCM type, provided that they can handle touch-tone dialing and data signals. But since the rest of the network will almost certainly be designed to handle existing log-PCM signals, low-cost, all-digital adaptive-DM-to-log-PCM converters will be needed. Note that log-PCM encoders can be produced by using a delta modulator, linear or adaptive, followed by a digital filter. This technique should provide reliable codecs, cheap enough to be used one for each telephone line.

Adaptive delta modulator chips will become available for digital encoding of television signals for industrial, but not broadcast quality use, while in military communications system operating at 16 kb/s, continuously variable slope delta systems modulator chips will probably remain supreme for the next few years, mainly because of its good tolerance of transmission errors. □

References 1. R. Steele, "Delta Modulation Systems," Pentech Press, London, or Halsted Press, New York, 1975.

Quantized feedback takes its place in analog-to-digital conversion

Thanks to LSI, the charge-balancing approach to a-d conversion is cost-competitive with the dual-slope approach; yet each of these integrating techniques has advantages

by Gary Grandbois* and Ted Pickerell, *Siliconix Inc., Santa Clara, Calif.*

☐ Selecting an analog-to-digital converter has long been an either/or choice between integrating and successive-approximation conversion techniques. While that basic choice still applies, selection of the integrating method requires a further decision between two different types of converters: the dominant dual-slope models and the quantized-feedback (charge-balancing) models, which have recently licked their problems with cost effectiveness. A comparison of these two types will lay open the advantages of each.

The choice between the integrating and the successive-approximation techniques is clearcut. The successive-approximation devices shine in applications requiring conversion times less than a millisecond, while the slower integrating devices most often provide a binary-coded-decimal output useful for display applications.

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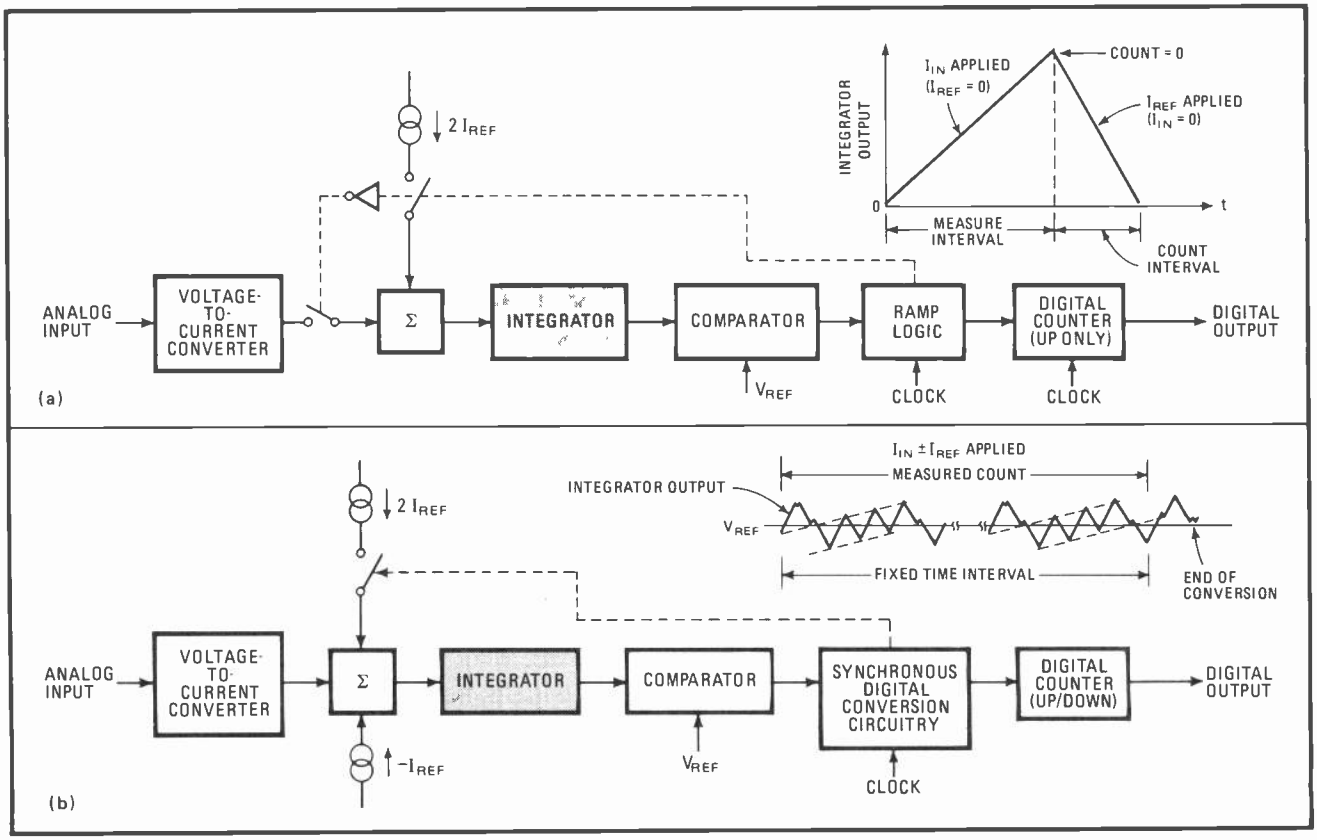
Successive approximation vs integration

Successive approximation is a fairly complex technique, requiring a high-speed digital-to-analog converter, a comparator, a successive-approximation register, and control logic. The device digitizes the analog input by successively comparing it with the output of the d-a converter, which is directly coupled to the successive-approximation register. In this way the comparator makes a decision on the state of each bit until the register's contents are the nearest digital representation to the analog input. The advantage of this technique is



1. Integrating. The dual-slope analog-to-digital converter (a) has a two-phase operating cycle made up of measure and count intervals. However, the quantized-feedback a-d converter (b) performs the measure and count functions simultaneously in a fixed-time interval.

COMPARING QUANTIZED FEEDBACK WITH DUAL SLOPE		
	Quantized feedback	Dual-slope
Operation	inherently bipolar	inherently unipolar
Comparator resolution required	1 part in 12	1 part in 2,000
Bit width around zero	inherently 1 LSB	inherently greater than 1 LSB
Typical integrator capacitor	0.068-μF Mylar	1-μF polypropylene
Conversion time	fixed	proportional to analog input
Short-term drift of clock frequency	not an error source	possible error source
Errors from capacitor dielectric absorption	no	yes
Multiplexed input	yes (sign and magnitude determined simultaneously)	no (multiple conversions required to determine sign and magnitude and to compensate for dielectric absorption)

its inherently high-speed operation—a 10-bit conversion, say, involves only 10 comparisons. Its complexity and comparatively high cost are important disadvantages.

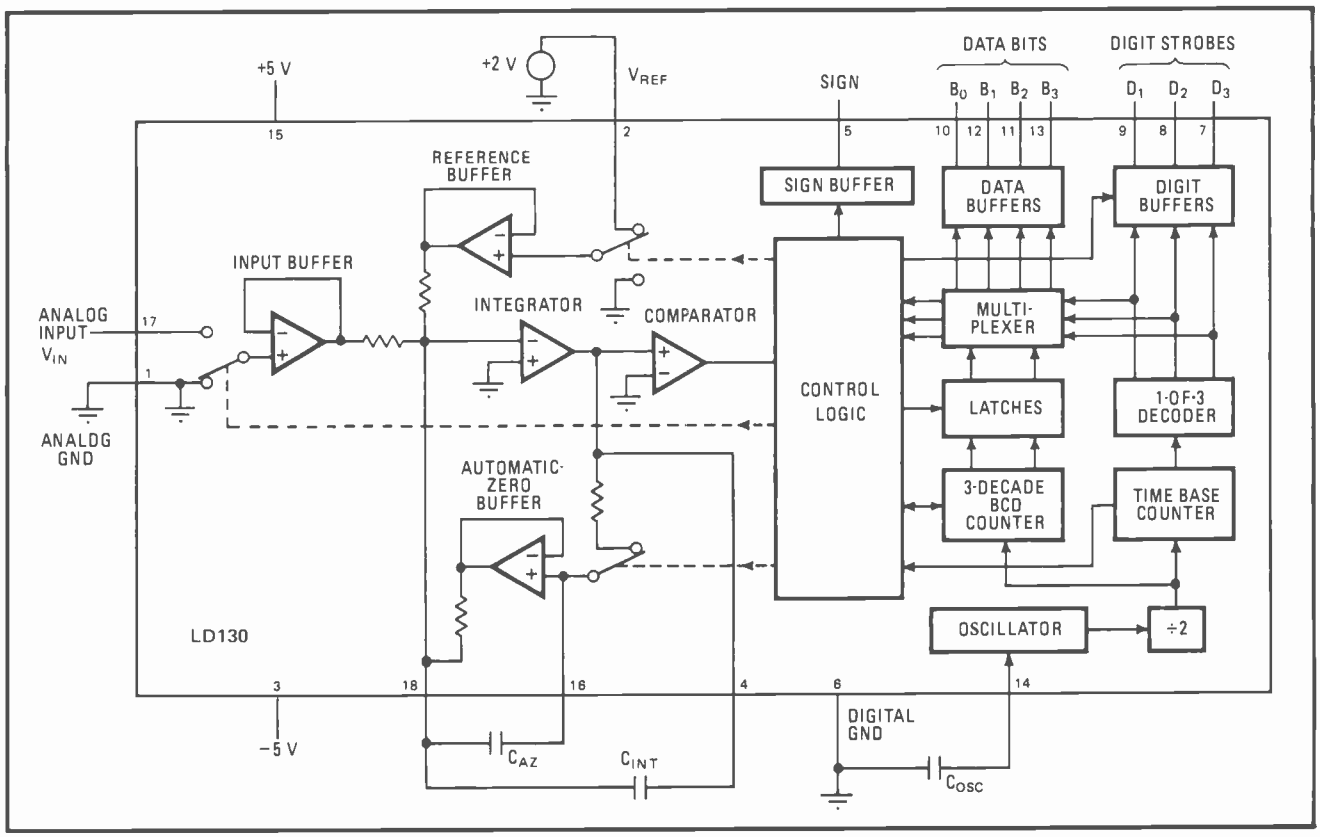
As the name implies, the integrating a-d converter makes use of the averaging property of integration. Briefly, the average charging current supplied by the analog input to a capacitor is compared, over a measured time interval, to the charge supplied by a known reference current. The digital count that results is a very accurate representation of the analog input.

Deciding whether the application needs a successive-approximation or integrating converter rests squarely on a single requirement: speed. If the conversion time must be shorter than 1 ms—when the application involves digitizing several channels, like 8 or 16, of slowly varying, multiplexed analog inputs or a single channel of a fast-changing signal—then the choice must be a successive-approximation device. The speedy conversion, however, does not negate the shortcomings of this component. These drawbacks make it a poor choice for any conversion that may be done acceptably at slow speeds. Among them: its digital output is not inherently monotonic; its input impedance is low; and it must be built with tight-tolerance components, which of course tends to bring its cost up.

On the other hand, the simplicity of the integrating converter gives it the best accuracy at low cost of any a-d device. Some models can attain accuracies as tight as 0.00075%. Several of these inexpensive devices can often replace a single multiplexed successive-approximation converter, yet provide reduced system cost and complexity. Other advantages of the integrating converter include an inherently monotonic output, high input impedance, and high noise rejection. Furthermore, it may be built with noncritical components and permits easy implementation of automatic-zeroing circuitry.

Dual slope vs quantized feedback

The two most popular integrating conversion techniques, dual slope and quantized feedback, are similar in that they both employ the principles of integration and charge equalization—but the similarity ends there. Dual slope, the older of the two techniques, is the simpler in



2. Single chip. Introduced last year, this complementary-MOS integrated circuit was the first single-chip quantized-feedback converter. Largely self-contained, the device requires only a voltage reference and three external capacitors, yet it delivers three digits of resolution.

concept and implementation, so it has been the preferred method. However, linear large-scale integration has made the more complex quantized-feedback converter practical, and its performance advantages over dual-slope can no longer be ignored.

The dual-slope converter (Fig. 1a) has a sequential two-phase operating cycle, consisting of a measure interval and a count interval. During the measure interval, the analog input charges the integrator's feedback capacitor for a set number of counts, making the accumulated capacitor charge proportional to the average value of the input over a fixed time interval. During the count phase, the counter is reset, and a reference current opposite in polarity to the analog input current charges the capacitor in the opposite direction. The counter measures this "discharge" time. Besides high accuracy, the familiar virtues of dual slope are good temperature stability, simplicity, and low cost.

The quantized-feedback converter (Fig. 1b) performs the measure and count operations simultaneously. During the single-phase digitization interval, digital control circuitry feeds quantized units of charge back to the feedback capacitor in response to the sampled state of an analog comparator. The converter produces these charge units by adding and subtracting a reference current to the integrator input for time periods that are counted and accumulated. During this time, the device keeps the integrator output voltage near the level of the reference voltage. In effect, the quantized-feedback converter measures the amount of charge required to balance the charge developed on the feedback capacitor by the analog input. However, it is the net time the reference current takes to balance the charge that provides the count that represents the input.

Examining the benefits

The advantages of such a simultaneous integration are many. For one, the conversion is done while the analog input is applied, so any drift in the clock frequency equally affects the charge supplied by the analog input and the charge of the reference current. Since the dual-slope converter integrates the analog input and reference currents during different time intervals, short-term drift of clock frequency is a possible source of error.

Furthermore, for a given clock frequency, the fixed time interval for measure and count in the quantized-feedback converter may be expanded without requiring a wider dynamic range of the integrator. With the dual-slope converter, expanding the time interval does require a wider dynamic range, perhaps one wider than the integrator being used can supply.

Since quantized-feedback conversion time is fixed, a data-acquisition system will not be tied up waiting for the newly digitized data, once it has been synchronized to the converter. The conversion time of the dual-slope device is proportional to the random analog input.

Additionally, automatic polarity selection is a natural outcome of the quantized-feedback technique, because the method uses both positive and negative reference currents. Yet the converter requires only a single reference voltage and a single full-scale adjustment.

Also, the dielectric absorption of the integrator's feedback capacitor with quantized feedback is not a source of error, as it is with dual slope. Moreover, the converter is not as sensitive to such comparator errors as noise, offset voltage, and drift.

In the quantized-feedback converter, zero occurs naturally as a number between minus full scale and plus full scale. The reference current may be at least twice as large as the maximum input current, and it is always present whether the input is at zero or some other voltage—so the change in the voltage, per unit time, at the comparator input can never approach zero. Since this is not the case with the dual-slope converter, it requires special zeroing circuitry and counter delays, leading to a dead band around zero that may be several bits wide. As a result, it tends to lose accuracy for small analog signals on the order of millivolts.

The table gives a concise comparison of the two techniques. An additional important point is that both can provide excellent 60-hertz noise rejection when the operating clock frequency that sets up the measure interval is properly selected.

Putting quantized feedback to work

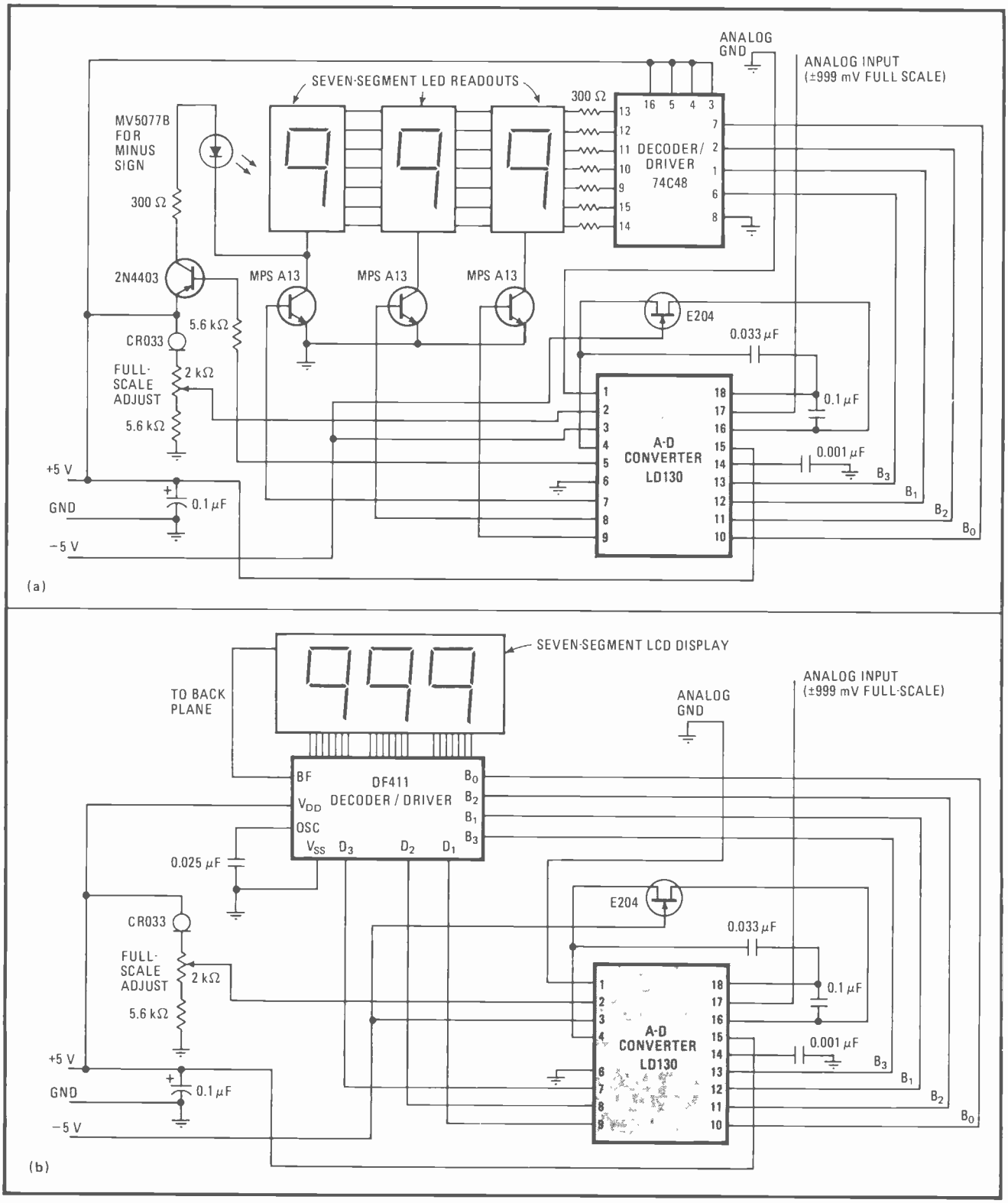
Quantized-feedback a-d converters are easy to use, and they are available from several semiconductor manufacturers. For resolutions of 3½ or 4½ digits, they come as two-chip sets, with the analog and digital circuitry separated. But in the last year, single-chip devices offering 3-digit performance have come on the market. The first of these was the LD130, a complementary-metal-oxide-semiconductor device that requires only a voltage reference and three external capacitors to make a complete converter.

On the chip (Fig. 2) are five operational amplifiers, five analog switches, three scaling resistors, and the control logic needed to implement the quantized-feedback conversion algorithm. Although the device provides automatic zeroing and automatic polarity selection, its power consumption is a low 25 milliwatts. In addition, linearity error is held to less than 0.1%, while input impedance is a high 1,000 megohms. In quantity, the price is less than $4.

The low power and low cost of this converter make it a natural choice for portable instruments. The unit may be easily interfaced to a light-emitting-diode or liquid-crystal display. To build a complete bipolar three-digit panel meter with an LED readout (Fig. 3a) requires few additional components. This DPM takes five samples per second and can make full-scale measurements to ±999 mV. High-efficiency light-emitting diodes and a C-MOS decoder/driver keep power consumption to a minimum, with input current typically measuring about 60 milliamperes.

Greater power savings may be realized by interfacing the converter with an LCD (Fig. 3b). This application utilizes only three digits of the four-digit capability of the DF411 LCD integrated driver circuit. The entire meter may be powered from a pair of standard 9-volt batteries for 150 hours of continuous operation.

Turning the converter into a digital tachometer/dwell meter is simple—just hook it up to the circuit of Fig. 4. This setup may be used for four-, six-, or eight-cylinder,

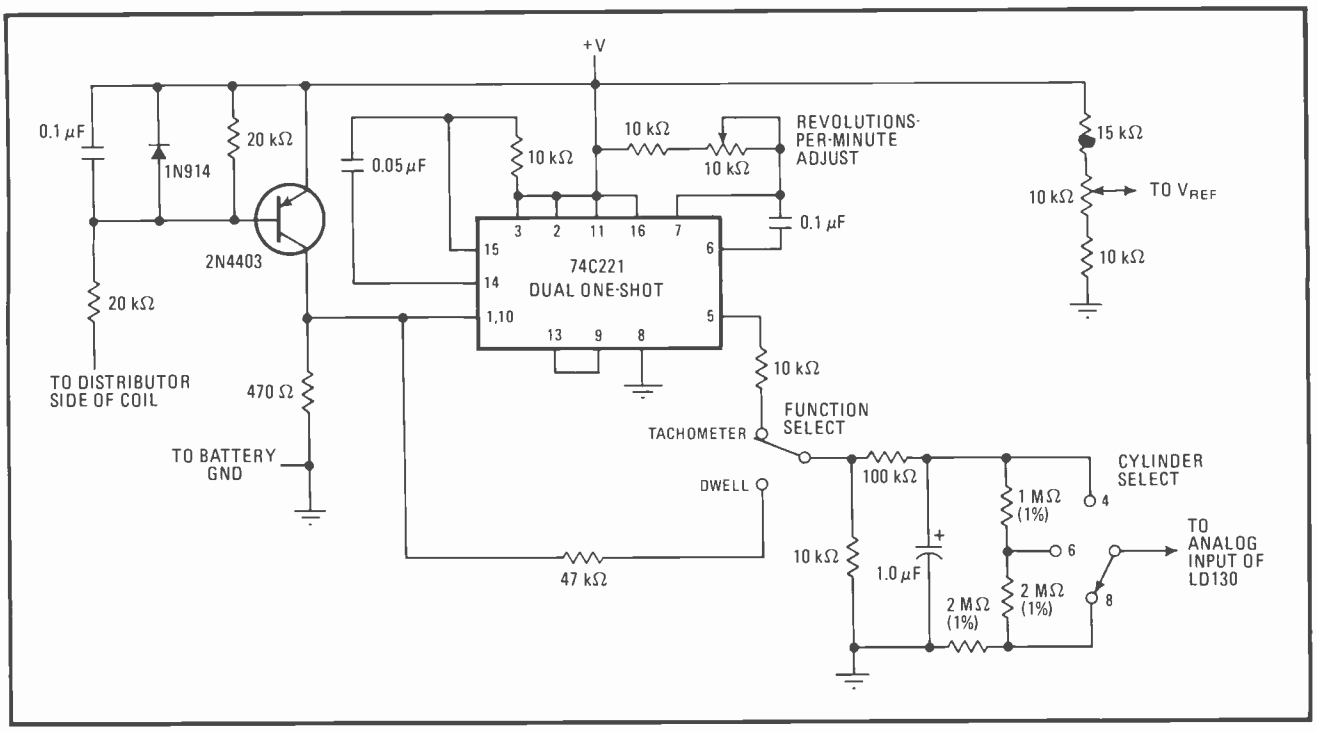


3. Choice of display. With the appropriate decoder/driver, the single-chip LD130 quantized-feedback converter can interface with either a light-emitting-diode display (a) or a liquid-crystal display (b) to form a three-digit panel meter capable of measuring to ±999 mV.

four-stroke engines with a distributor ignition system. The setting of the single-pole, three-throw switch selects the number of engine cylinders.

As a dwell meter, the circuit can make full-scale readings of 100° and, as a tachometer, 10,000 engine revolutions per minute. The dwell-time measurement is made by taking the average value of the distributor duty cycle and scaling it to degrees of rotation.

Engine rpm is measured by triggering a monostable multivibrator with each point closure. The average direct-current value of the pulse train produced is scaled to read rpm × 10. When the points open, a second one-



4. Build it. Hooking up this circuit up to the LD130 converter enables the device to measure engine revolutions per minute or the dwell time between point closures, depending on the position of the function switch. The circuit operates from a single positive supply.

shot disables the first one-shot, which is effectively serving as a frequency-to-voltage converter. This action avoids extraneous triggering from ignition ringing.

To achieve a proper zero, the circuit employs a dual C-MOS one-shot, because its output does not have the inherent saturation-voltage offset that a bipolar one-shot does. Since the circuit's outputs are all proportional to the positive supply voltage, the reference voltage for the quantized-feedback converter is derived from the supply.

One of the most common uses for a-d converters is in microprocessor-based data systems, and the LD130 offers a number of attractive features for such applications. For instance, its BCD output is the optimum digital format when the processed data is to be displayed. Since its output is multiplexed, the converter readily interfaces with both 4- and 8-bit microprocessors.

Interfacing to microprocessors

Probably the biggest problem with 4-bit processors is interfacing to the bus. The 4 BCD data bits fill the bus, so there are no bits available for the digit markers. One solution is to apply the data bits to a 4-bit input port and the digit strobes to a second identical input port, thus identifying the data. In spite of the added component, this interface is a simple one, although it does require the processor to use a significant amount of its time to synchronize itself to the converter.

In contrast, the bus of an 8-bit processor permits the data markers to accompany the 4 BCD data bits to the microprocessor's accumulator register. The eight bus lines from an 8-bit input port are taken up with the 4 BCD data bits, three digit strobes, and a data-valid bit. Such an interface configuration requires the microprocessor to poll the input port occasionally to determine if the data-valid bit is low.

The single-chip LD130 is representative of the many second-generation integrating a-d converters that call for few external components. However, it is unlikely that these few out-board parts will be put on chip in future designs. Although C-MOS processing gives high input impedance and low power drain, it cannot provide a high-quality on-chip voltage reference. A bipolar technology like integrated injection logic can handle the complexity of a largely self-contained converter while delivering the reference, but input impedance becomes low and bias current high.

The noise problem

Another constraint on the design of all monolithic a-d converters is the digital noise that inevitably crops up during the conversion. This noise problem has limited all single-chip devices to a maximum sensitivity of 1 mv for reasonable conversion stability. Therefore, the two-chip approach is likely to remain the more viable one when tighter sensitivities are needed, as is the case with 4½-digit converters. Additional problems could arise if LED displays were to be driven directly from a single-chip converter—power dissipation would have to be greater than 0.5 watt, and thermal drift could be excessive.

Third-generation integrating a-d converters are probably going to come in two basic configurations—either a 3½-digit chip requiring external display drivers, or a two-chip set incorporating an internal reference and direct display drivers. In such a two-chip setup, the external components will be cut to a minimum—just a few capacitors, a gain-setting potentiometer, and the display. Although operation from a single supply voltage will be more common, dual-supply converters will still have a place for achieving high input impedance or true bipolar conversions. □

Reducing system interconnections with multivalued logic

Sending multiple voltage and current levels over a transmission line enhances processing capabilities of otherwise all-binary systems

by Clive W. Ross, *Plessey Marine, Templecombe, Somerset, England*

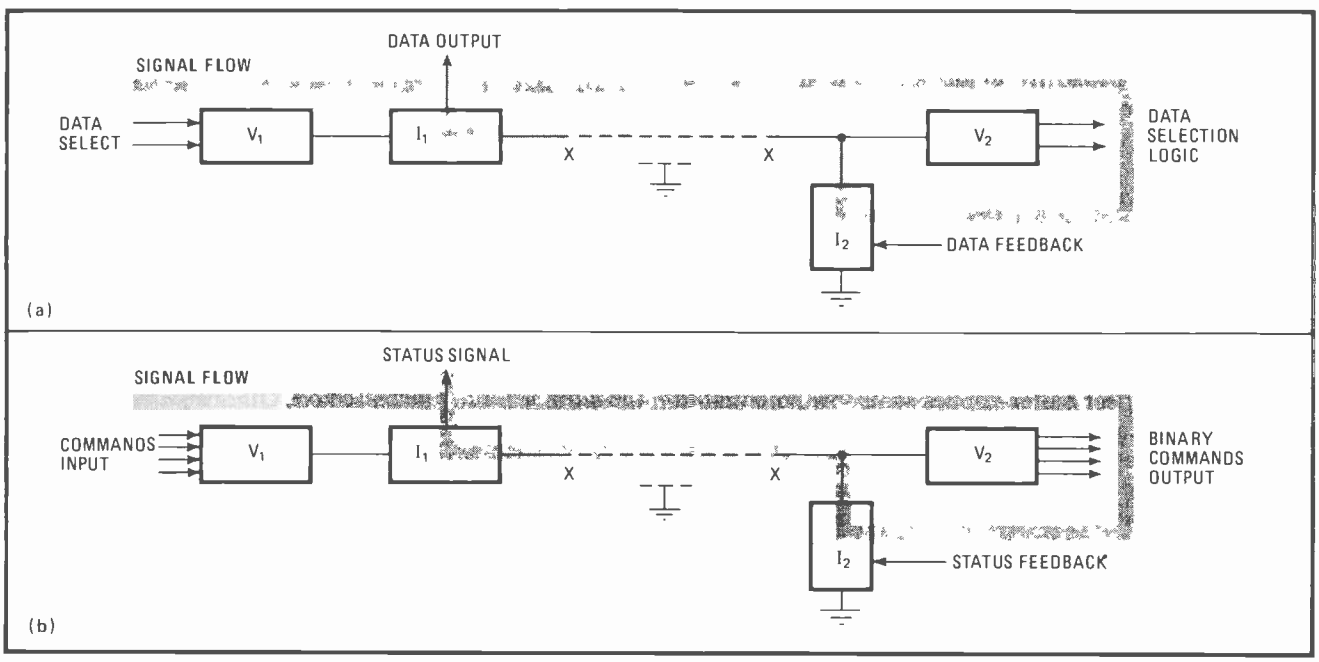
☐ Even though all present digital integrated circuits work with binary data and control signals, binary logic need not monopolize a digital system. The use of logic based on more than two levels of voltage or current—or, better yet, on multiple values of voltage *and* current—is possible in parts of today's systems. It will greatly expand the amount of information they can process and does not even require the development of new multiple-state devices.

Most efforts in multivalued logic circuits have concentrated on what may be termed a "first order" system, which quantizes either the voltage or the current levels. But greater processing capability can be obtained with a "second order" system, in which both voltage and current levels are used.

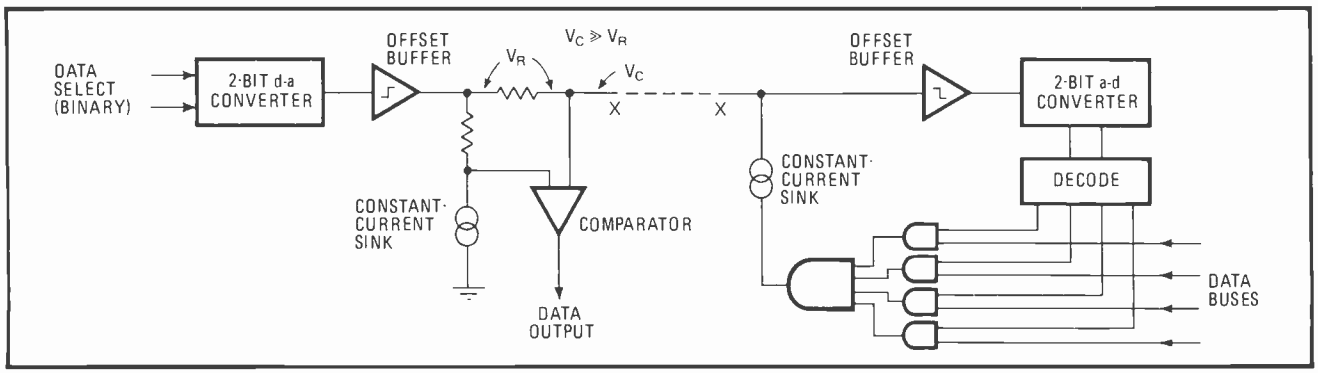
Consider a system in which a transmission path links control circuits to other circuits where data is either processed or acquired. Both ends of such a system may work in a binary mode, but if a second-order nonbinary regime is imposed on the transmission path, significantly fewer interconnection paths are required. It can be done very simply, by using present-day binary devices along with analog-to-digital and digital-to-analog converters to generate the multiple voltage and current levels required. Nor need there be more than, say, three voltage states and two or three current states to gain the promised improvement over strictly binary systems—four to ten times their information processing capability.

The simplest system

To back up a little, a simple device that can be used in a first-order nonbinary system is the familiar tri-state integrated circuit. Although the tri-state device works in the binary mode, it may actually generate more than two output states. Two of the states in a typical tri-state device are the normal 1 and 0 conditions, while the third is a high-impedance or off state, which permits the device to be controlled by some other source by means of a bus. A bias network can be used at the output of the device to assign an arbitrary voltage value to this third



1. Second-order nonbinary system. Multiple voltage and current levels are generated for single-wire multiplexing. V_1 converts the binary input signals into several voltage levels, while I_1 detects current flow in x—x line. V_2 converts the levels back into binary format so logic may pass desired data. I_2 detects data, changing current on line, passing data to output. Digital (a) and process-control systems (b) are similar.



2. Digital-data application. Practical nonbinary system may be easily implemented. Two-bit d-a converter assumes duties of V_1 in Fig. 1; a-d converter is V_2. Logic drives current sink I_2. Comparator is I_1. Offset buffers calibrate current sinks.

state. Thus it is shown to be possible for three voltage levels or, alternatively, three current levels to be generated from binary input signals.

A second-order binary system is a more complicated, but easily understood, network. Generally speaking, binary control signals retrieve data from a data source through a bidirectional transmission line and deposit it at a designated point in the operating system. To do so, they must generate several voltage levels on the transmission line. Returning on the line is a multicurrent feedback signal corresponding to the retrieved data.

The basic idea is the same for both a digital data application (Fig. 1a) and a control application (Fig. 1b). Voltage source V_1 converts the binary input signals into one of several voltage levels, while circuit I_1 detects the resulting current flow in the x – x line. Circuit V_2 detects and translates the voltage levels back into binary format at the receiver end. I_2 detects a data feedback signal, which is a function of the data on the line selected, and changes the line current. Finally the data is transferred to the output.

Some applications

The relationship of this block diagram to various applications can be easily demonstrated. In many cases, only a single wire and ground will be needed for the data multiplexing.

Figure 2 shows a digital data application—a circuit using two converters, a comparator, and two-state current sinking. Obviously there could be multistate current sinking and the use of multiple comparators, but for simplicity's sake only two current states and four voltage states are considered.

As shown, the 2-bit d-a converter generates four voltage levels and sends these control signals through line x – x. The offset buffer applies some low potential to the line to allow calibration of the current sink.

At the receiver, the voltage steps are level-shifted by the buffer and fed to a simple analog-to-digital converter, which in turn feeds a decoder and four gates. The gates are enabled by the binary signals from the a-d converter, permitting the data already on particular gates to pass through to the current sink. The constant-current sink switches on or off, depending on the state of the gate array. The data, either a 1 or a 0, is sent back through the line to appear at the output of the comparator. The comparator detects the current changes in the line by using a reference input voltage derived by a constant-current network. In this case, four lines of data have been interrogated and read out at a remote location, using a single line plus ground.

A control application is also easily implemented. Consider a magnetic-tape recording system having 24 channels and three operating modes (normal playback, playback from record head, record), in which it is desired to detect the magnitude of the bias current flowing through the tape head during a recording period. This information is to be fed to a remote unit containing a number of light-emitting diodes that indicate system status. There are thus five conditions of the system that must be identified: these three voltage states plus two bias-current states. These conditions can be detected with a three-voltage – two-current-state circuit using only a single control line per channel. For example, suppose the system has these voltages and currents:

- Normal playback: 0 volt.
- Playback from head: 10 v.
- Record: 20 v.
- Record bias current, below normal or zero: 0 – 0.5 milliampere.
- Record bias current, normal or above: 5.0 mA.

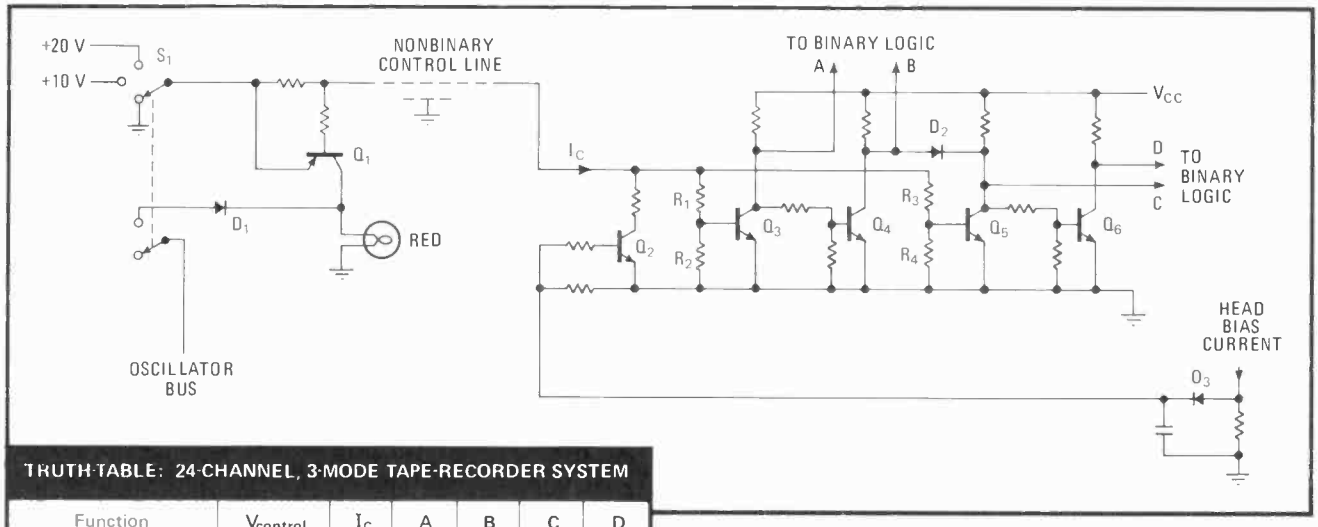
Circuit details

A simple three-voltage – two-current transmitter for this circuit is shown to the left in Fig. 3. A switch selects the mode desired, and a two-level current sensor, Q_1, determines the relative magnitude of the bias current.

When the switch is in the record mode, a 1-hertz oscillator is connected through diode D_1 to the red lamp, the bias-current indicator. Then if a logic decision made at the receive end indicates normal bias current, the command-line current rises, transistor Q_1 saturates, and the lamp will fully be biased on. Otherwise, the lamp will be controlled by the oscillator and will flash a warning indicating low bias current.

A circuit using simple comparators is needed at the receiving end, to translate the quantized voltages back into binary form. Also needed is a means of applying a binary signal to a current sink that is controlled by some final event, to acknowledge that the chain of command is by then complete.

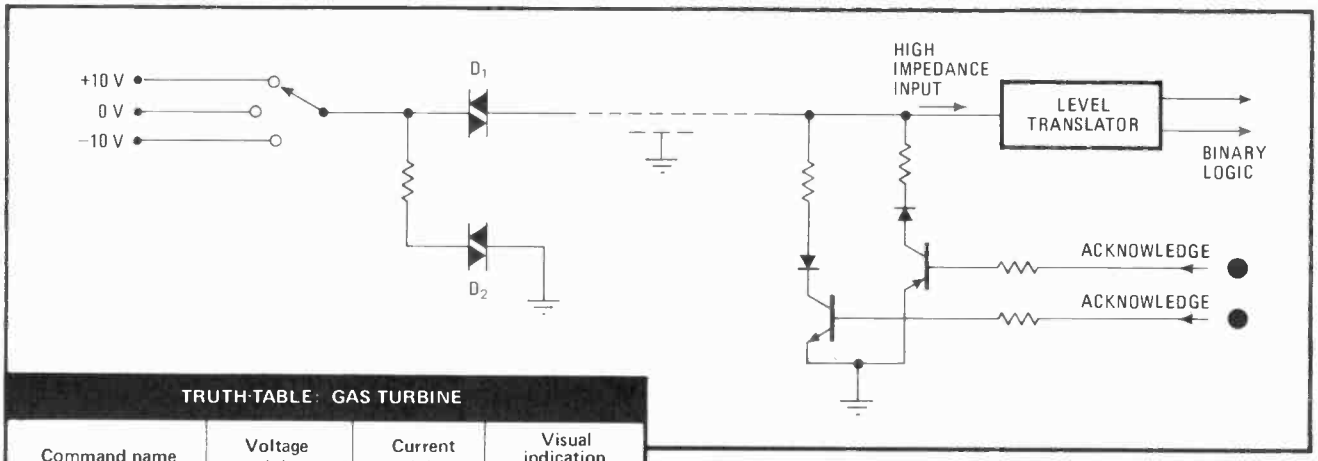
In Fig. 3, the ratios of resistors R_1 to R_2 and R_3 to R_4 are selected so that Q_3 and Q_5 saturate at control-line potentials of 10 and 20 v respectively. Under certain



TRUTH-TABLE: 24-CHANNEL, 3-MODE TAPE-RECORDER SYSTEM

Function	$V_{control}$	I_C	A	B	C	D
Play (normal)	0	0	1	0	1	0
Play (rec head)	10	0	0	1	1	0
Record (?)	20	0	0	0	0	1
Record (OK)	20	1	0	0	0	1

3. Process-control application. Value of head bias current is to be determined during record periods in this magnetic-tape recording system. Receiver detects mode, drives logic circuits so that head current is sampled if system is in required mode. D_3 conducts if current is normal. Q_2 fires, changing current I_C so as to bias red lamp fully on. Otherwise, lamp is fired by 1-Hz oscillator.



TRUTH-TABLE: GAS TURBINE

Command name	Voltage state	Current state	Visual indication D_1	Visual indication D_2
Standby	0 ±0.5 V	0 ±100 μA	none	none
Forward propulsion on, velocity low	+10 V ±2 V	0 to +500 μA	none	green
Forward propulsion on, velocity normal	+10 V ±2 V	+15 mA ±20%	green	green
Reverse propulsion on, velocity low	−10 V ±2 V	0 to +500 μA	none	red
Reverse propulsion on, velocity normal	−10 V ±2 V	+15 mA ±20%	red	red

4. Modification. The addition of one current sink and the use of two-color LEDs provide a three-voltage – three current circuit for monitoring a gas turbine system. The output circuit is simplified, because the diodes convert line current changes directly, needing no transistors, comparators, or current sinks.

circumstances Q_4 and Q_5 assume opposite logic states. So diode D_2 has the important function of preventing the condition where they try to force point B to assume two different logic states simultaneously.

When the record command is detected, the logic connected to the binary output points A through D activates the record-head circuits. The bias current is detected by D_3 and turns on Q_2 if the current is greater than 5 mA, and consequently the current on the control line will change.

An interesting transmitter is shown in Fig. 4. Though extremely simple, it produces three voltage states and three current states. Two current sources and red/green LEDs provide more capability than the previous circuit.

Conventional binary-logic circuits are in wide use, and the use of tri-state devices is expanding. It seems certain that nonbinary systems will soon have considerable impact in many areas, particularly as a practical second-order binary system could have 10 times the information capacity of its binary counterpart. □

The right gyrator trims the fat off active filters

Replacing inductors with gyrators creates almost perfect filters

by Thomas H. Lynch, *Bunker-Ramo Corp., Electronic Systems Division, Westlake, Calif.*

☐ Analog filters exhibiting nearly ideal performance can be built around a gyrator—if the right configuration of this active circuit is used. In effect, the gyrator makes a capacitance behave like an inductor, freeing the filter of the problems plaguing conventional inductors, like large size, low Q, winding capacitance, nonlinearity, and magnetic susceptibility.

Yet most designers look upon the gyrator as an idealistic circuit with a "peculiar" behavior that puts it out of touch with practical applications. This attitude completely ignores its power. Unlike other active-filter circuits, the gyrator permits the designer to take advantage of the large body of data and techniques already developed for passive LC filters. He can start with a passive prototype circuit and then replace each inductor with a gyrator, substantially reducing filter size and weight for frequencies up to about 50 kilohertz.

Fortunately, too, there is one gyrator realization that works superbly. Not all of them do—in the past, different versions have suffered from drawbacks like instability, poor control of loss, sensitivity to component matching, and even excessive complexity. But the preferred version is simple and stable and simulates a high-quality inductor, permitting very high-performance filters to be realized. In addition, this gyrator, unlike other active-filter circuits, preserves the most significant advantage of coupled LC networks—their inherently low sensitivity to changes in component values (see "The strength of LC filters," p. 116).

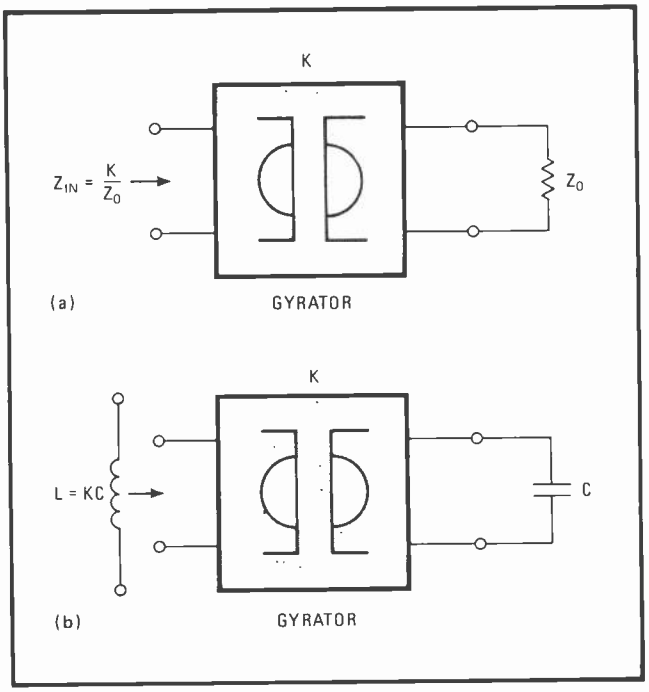
Understanding the gyrator

Basically, the gyrator is a lossless two-port circuit (Fig. 1a) that inverts a load impedance. When used with a high-Q capacitor (Fig. 1b), it simulates the virtual characteristics of a high-Q inductor. The preferred realization for the gyrator requires only two amplifiers and five impedances, as shown in Fig. 2 for both the general impedance representation (a) and the practical RC implementation (b). In the latter case, the circuit simulates an inductor having a value of KC, where K is a constant determined by the resistors:

$$K = R_1R_3R_5/R_2$$

At first glance, this gyrator's need for two amplifiers may seem a disadvantage. However, consider the major drawback of most single-amplifier resonators. They generally require an amplifier having a gain in excess of Q^2; and those that do not usually are extremely sensitive to passive-element variations. On the other hand, the gyrator does not require a high-gain amplifier—in fact, stable Qs of better than 1,000 may be obtained with only 40 decibels of gain. Furthermore, unlike other active-filter circuits, the gyrator is remarkably insensitive to any amplifier parameter, so it may be built with garden-variety devices, even quad chips, as long as they are unity-gain-stable amplifiers.

Additionally, with the gyrator, amplifier phase shift enhances Q, rather than diminishing it as in other active-



1. Ideally. Coupled LC filters simulated with gyrators have characteristics approaching the ideal. In effect, the gyrator is a lossless two-port circuit (a) that inverts a load impedance. With a capacitive load impedance, the circuit (b) simulates a high-quality inductor.

The strength of LC filters

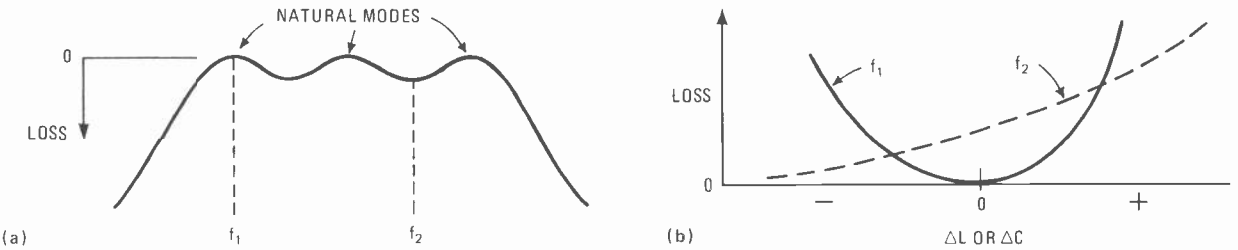
In theory, coupled LC filters have the lowest sensitivity to component variations. These doubly terminated reactive two-ports produce a frequency response by reflecting power back to the source in the stopbands.In the passband, power transfer is maximum at natural modes (a) determined by the filter's transfer function.

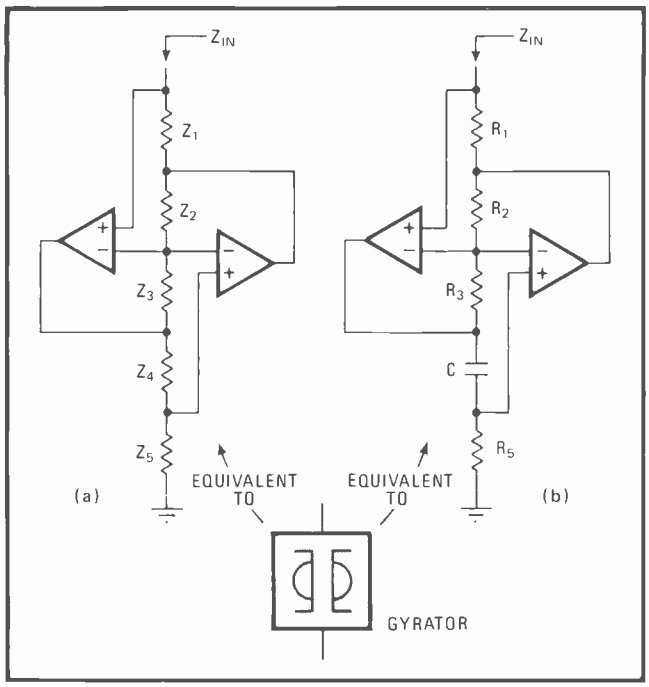
In the real world, a change in any inductor or capacitor making up the filter can only cause a loss in the load power—down from the maximum. This power loss at one of the natural modes (f_1) increases monotonically (b), while at frequencies other than the natural modes, such as f_2, a small loss exists because of the ripple caused by reflected power. At any point within the passband, then, the change in loss has a well-behaved and slowly varying characteristic that follows the changes of any inductor or capacitor in the network.

Since no one inductor or capacitor determines a natural mode, a change in any single inductance or capacitance can only partially affect the shift in a natural-mode frequency. It follows that coupled LC filters are inherently insensitive to changes in component values. Similarly, if all of the inductors in the filter are replaced by gyrators, this insensitivity to component variations does not change, since the gyrator is an active circuit and adds no dissipative elements to the filter.

Other active-filter circuits, however, like the biquad and state-variable or universal active filters, are developed from the state equations describing a second-order transfer function. Since these circuits duplicate the properties of a second-order (one complex pole pair) LC filter, their component sensitivity is still the same as for coupled second-order networks. On the other hand, extension to higher orders requires factorization of the transfer function into biquadratic (second-order plus lower-order) factors, each of which specifies a separate Q and natural-mode frequency. The desired transfer function is then realized by cascading biquadratic stages. Since these stages are uncoupled, changes can easily occur in the amplitude or frequency of the simulated modes, making the high-order filters built this way sensitive to component variations.

An alternative is the design approach called leap-frog. It implements the state equations of the prototype LC filter directly, using integrators and summing amplifiers. But though the resulting filter does have about the same low sensitivity as the equivalent coupled LC network, the final circuit can become very complex for high-order functions.





2. Realistically. Preferred gyrator realization (a) requires two amplifiers and five impedances. In practical RC implementation (b), impedance Z_4 is a capacitor, and the other impedances are resistors. The gyrator may also be represented by the special symbol shown here.

filter circuits. At the ideal phase shift of 90°, the Q of the simulated inductor is approximately equal to that of the capacitor being used. If the phase shift is greater than 90°—which is usually the case—the Q becomes even higher.

Needless to say, the inductor the gyrator simulates is not perfect—the gyrator can be no better than the resistors and capacitors with which it is built. Of the two, resistors are less worrisome, for tin-oxide, metal-film, and thin-film types all perform acceptably. Capacitors, on the other hand, are the weakest link in the gyrator circuit, and there are usually two or more of them per complex pole pair. They impose the first limitation—maximum Q—in any realization, and their capacitance may change a lot with temperature. The table reviews the important characteristics of a variety of capacitor types. Generally, NPO ceramic devices are least affected by temperature, whereas polypropylene units achieve the highest Q.

Creating a floating gyrator

One seeming limitation of the gyrator is that it is grounded at one end. But the floating inductor often needed in a filter can be simulated successfully—for example, by connecting two grounded gyrators. However, this does not necessarily mean that an extra gyrator is required for every floating inductor in a passive LC

filter. Figure 3a shows two gyrators sharing the bottom resistor, R_5, at opposite ends, so as to simulate a single floating inductor. This resistor is described in the gyration constant:

$$L = \frac{R_1 R_3 R_5}{R_2} C$$

The equation may be rewritten as:

$$L = \frac{R_1 R_3 C}{R_2} R_5$$

which says that the simulated inductance is directly proportional to the value of R_5. Therefore, if R_5 in fact becomes a loaded port for the gyrator, the simulated inductance will depend on the value of resistance connected to that port.

A cursory examination of the preferred gyrator realization (in Fig. 2b) will reveal a corollary to the above relationship. Between the top of R_1 (the input port) and the bottom of C, a voltage null exists because of the amplifiers' input connections. Therefore, the port to which R_5 is connected has the same voltage as the input port (although the currents are not the same, otherwise an apparent inductance could not exist). As a result, the input impedance, Z_{IN}, is also proportional to resistor R_5. This resistor could even be a network of resistors to describe the topological connections, of, say, a T or pi network of inductors, as indicated in Fig. 3b.

Designing another floating gyrator

Indirectly, a floating inductor may be achieved in another way—one that opens up other possibilities for converting a passive LC filter to its active equivalent. When a second capacitor is added to the gyrator and one resistor removed, the circuit becomes a functionally dependent negative resistor (FDNR)—an element that appears to be a negative resistance that decreases in value with frequency.

Consider the transfer function for the basic impedance converter of Fig. 2a:

$$Z_{IN} = (Z_1 Z_3 Z_5)/(Z_2 Z_4)$$

If Z_1 and Z_3 are capacitors and the other impedances are resistors, then:

$$Z_1 = Z_3 = 1/sC$$

where $s = j\omega$. The input impedance can then be written as:

$$Z_{IN} = \text{FDNR} = \frac{1}{s^2}\frac{R_5}{C^2 R_2 R_4} = -\frac{1}{\omega^2}\frac{R_5}{C^2 R_2 R_4}$$

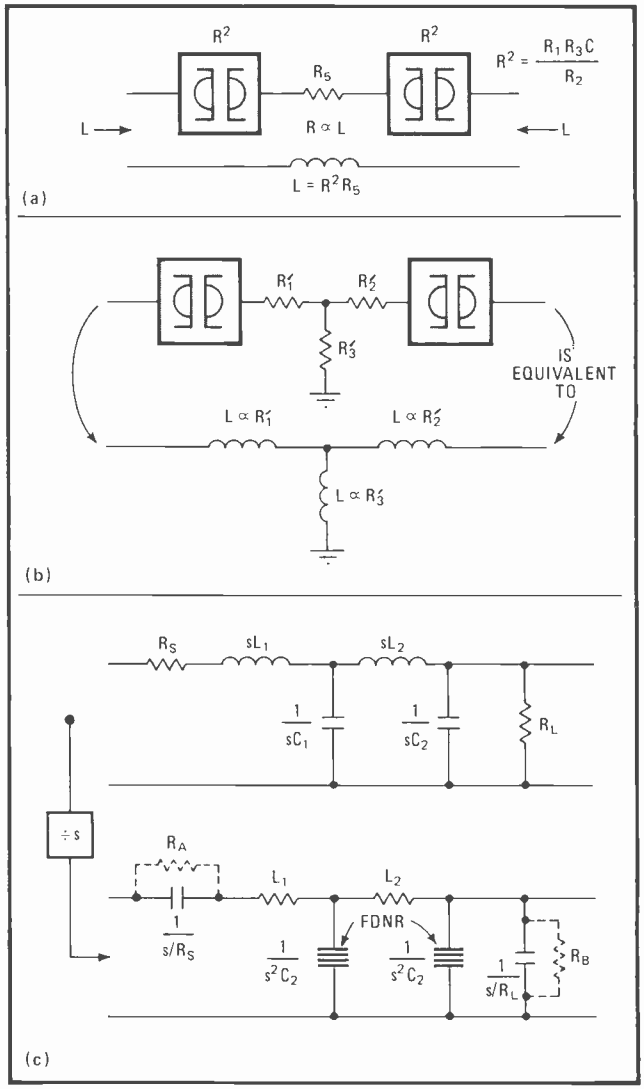
This element may be used to solve the problem of simulating floating inductors in low-pass filters. The technique is simple—just divide all elements by s, which is the complex variable, and then replace the $1/s^2$ terms with an FDNR, as shown in Fig. 3c. The floating inductors become resistors having a value of L. Resistor R_A and resistor R_B simply provide bias and response for the circuit at dc.

Although the gyrator is not the easiest circuit to understand, designing with it is really not that hard. Suppose the requirement is for a double-tuned bandpass

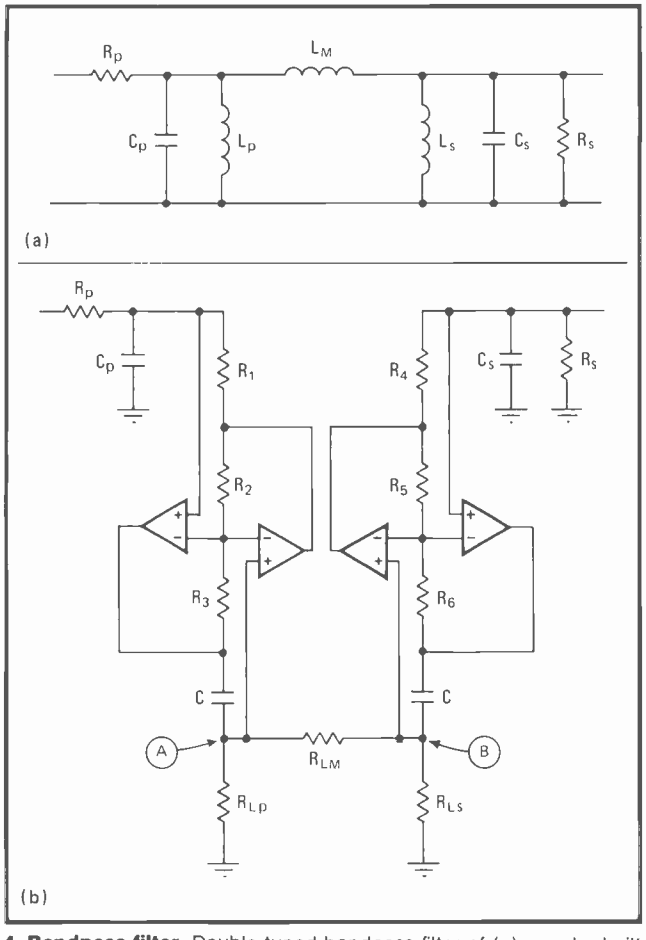
CAPACITOR CHARACTERISTICS

Type	Q (at 1 kHz)	Temperature coefficient (ppm/°C)	Temperature range (°C)
Mica	600	1 to +70	−55 to +125
Polystyrene	2,000	−150 ±50	−55 to +85
NPO ceramic	1,500	±30	−55 to +125
Polypropylene	3,000	−115	−55 to +125
Glass	1,500	+140 ±25	−55 to +125
Polycarbonate**	500	≈ 50*	−40 to +100
Mylar**	100	large	−55 to +85
Polyester**	100	−160*	−40 to +100
Porcelain	2,500	±25	−55 to +125

*0°C to 50°C **Q and C nonlinear functions of frequency and function



3. Floating. Lower terminal of basic gyrator (Fig. 2b) is grounded. To float the circuit, two gyrators may share the same resistor (a), or a network of resistors (b). Floating inductors may also be simulated (c) with functionally dependent negative resistors (FDNRs).



4. Bandpass filter. Double-tuned bandpass filter of (a) may be built with two gyrators, as in (b). Sharing resistor R_{LM}, the grounded gyrators simulate the pi network of inductors in the passive version. All of the amplifiers may be general-purpose devices.

filter, like the one drawn in Fig. 4a. The procedure is straightforward. First compile the design data required:

e_r, the desired passband ripple, expressed in peak-to-peak decibels;

f_o, the center frequency in hertz;

f_r, the ripple bandwidth in Hz;

C, the capacitance value for both C_p and C_s in farads;

r, the termination ratio of R_p/R_s.

Next, calculate these variables:

$$A = (10^{e_r/20})^{-1}$$

$$q = \left[\frac{2(1 - A^2)^{1/2} + r + (1/r)}{2 - 2(1-A^2)^{1/2}}\right]^{1/2}$$

$$Q' = f_0/f_r$$

$$\alpha = 2(1-A^2)^{1/2}$$

$$X = [\alpha (1 + q^2)]^{1/2}$$

$$Q = Q'X$$

$$X' = \left\{\frac{\alpha}{2}(1 + q^2)\left[1 + \frac{[\alpha^2 + 4(10^{6/20}-1)]^{1/2}}{\alpha^2}\right]\right\}^{1/2}$$

Then compute the design results:

$$R_s = \frac{Q}{\omega_0 C r^{1/2}}$$

$$R_p = R_s r$$

$$L_M = \frac{R_s r^{1/2}}{\omega_0 q}$$

$$L_p = L_s = \frac{L_M}{\omega_0^2 C L_M - 1}$$

$$G_0 = \frac{1}{r^{1/2}}\left[\frac{q}{1 + q^2}\right]$$

where G_0 is the midband gain.

$$BW(3\ dB) = \frac{X'}{X} f_r$$

where BW(3 dB) is the 3-dB bandwidth.

Building a double-tuned filter

Two gyrators replace the pi network of inductors, as shown in Fig. 4b. Now assign the same capacitance value for C as that chosen for C_p and C_s. The amplifiers may be a quad-type 4136, since choosing such a device ensures a good match between the amplifiers for optimum gyrator performance. Next, determine the gyrator resistances from:

$$L_p = (R_1 R_3 R_{Lp} C)/R_2$$

It is good practice to maintain the resistances at about the same value, so assume:

$$R_1 = R_2 = R_3 = R_{Lp} = R$$

Then:

$$R^2 = L_p/C$$

The value of R should be large enough to minimize amplifier loading and slightly smaller than the amplifier differential input impedance. For convenience, choose the closest standard value for R and let:

$$R = R_1 = R_2 = R_3$$

Then compute:

$$R_{Lp} = L_p/CR$$

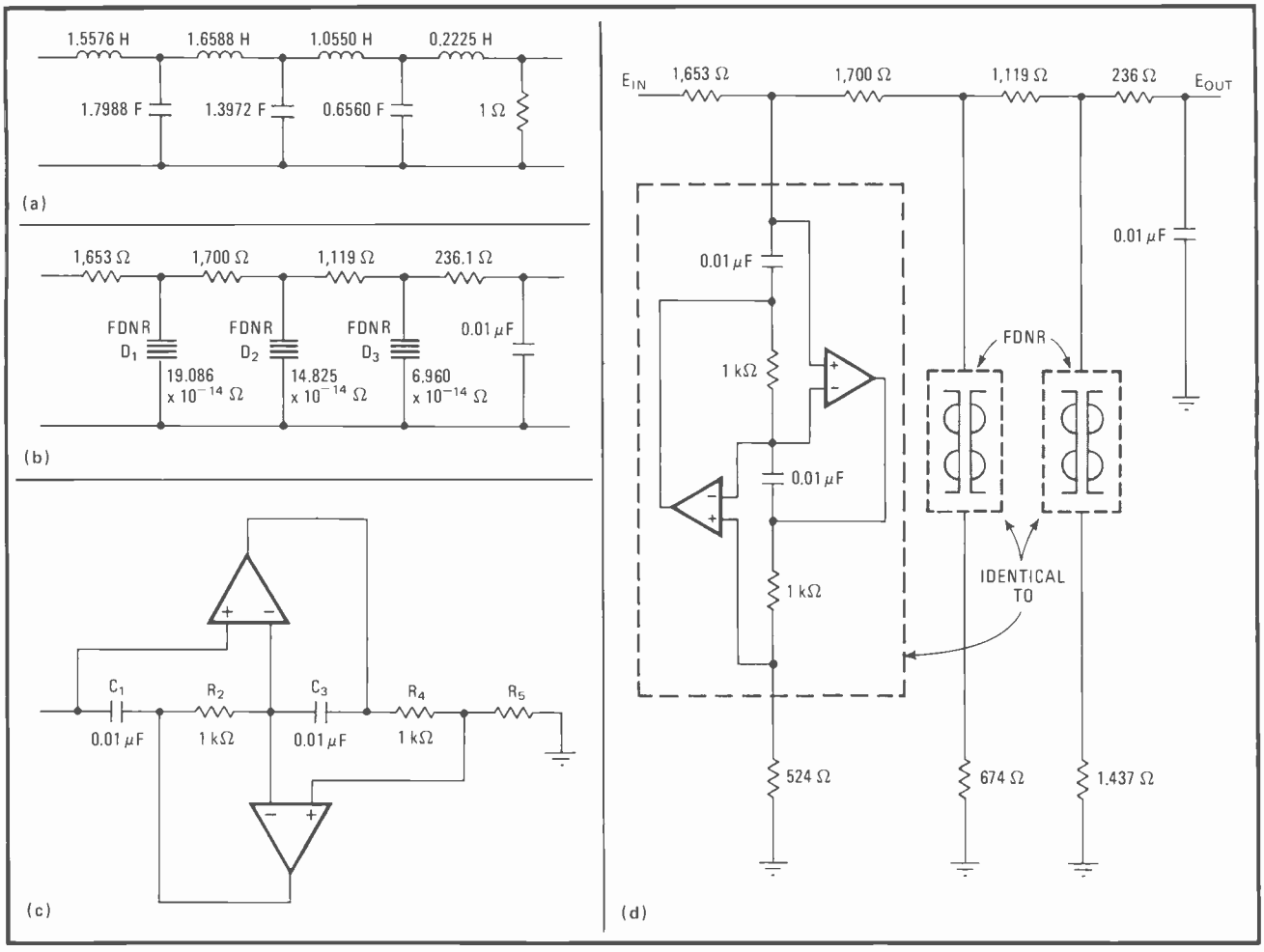
Again select a nearby standard value for R_{Lp} and scale R_{LM}:

$$R_{LM}/R_{Lp} = L_M/L_p$$

This ratio must be maintained, since it determines the coupling in the circuit. All of the component values are now known. The tolerances for C may be ±5% and ±1% for R, although the tolerances for $R_{1\text{-}6}$ could be looser as long as the devices' environmental characteristics are acceptable.

Tuning the filter

Tuning is simple. Overall Q has already been determined by the value of R_{LM}. Using point A as the output, the primary (left-hand) gyrator is set by shorting point B to ground and adjusting R_1 or R_2 to achieve resonance at the center frequency. Reducing R_1 (by shunting it) will decrease L_p, raising the resonant frequency. The reverse holds for R_2. Tune for 0° phase shift relative to the



5. Aliasing filter. Number of floating inductors in low-pass aliasing filter (a) makes implementation with grounded gyrators difficult. Instead, FDNRs may be used (b), each of which requires two capacitors (c). The final circuit (d) employs only three of these FDNRs.

source. Next, disconnect point B from ground, and tune R_4 or R_5 for 90° phase shift (at the center frequency) at the output, or point A, which is equivalent. (Tuning with a Lissajous circle can provide accuracy to better than 2°.)

A second example demonstrates how to design with FDNRs. The requirement is for a low-pass aliasing filter—a seventh-order Butterworth circuit having a 1-dB corner at 15 kilohertz.

Using functionally dependent negative resistors

A prototype circuit (Fig. 5a) is first obtained from one of the standard tables in existing literature. Here, the number of floating inductors prevents easy implementation with the grounded gyrators, and the best approach is to use their close relative—the FDNR.

To convert the LC prototype circuit to an FDNR realization, first normalize the corner frequency to 1 radian per second. Next scale the circuit for frequency by dividing the inductors and capacitors by $2\pi(15\ \text{kHz})$, and then scale the impedances for a convenient capacitor value, say 0.01 microfarad or $1/(0.01 \times 10^{-6})$ ohms, in which case multiply the inductances by 10^8 and divide the capacitances by 10^8. Finally, dividing all of the network impedances by the complex variable, s, results in the FDNR realization of Fig. 5b.

Each FDNR is actually the basic gyrator configuration, but with two capacitors (Fig. 5c) instead of just one. In this example, all of the resistors, except R_5, are set equal to 1 kilohm, and the two capacitors to 0.01 microfarad each. Then R_5 may be computed from:

$$R_5 = (R_2R_4C_1C_3)/D$$

where D is the impedance value of the FDNR. Therefore, for D_1, R_5 = 524 ohms; for D_2, R_5 = 674 ohms, and for D_3, R_5 = 1.437 kilohms.

Figure 5d shows the final circuit, in which all seven capacitors have the same value, an essential point in low-cost design. The circuit may be built with 1% resistors having values closest to those computed and with NPO ceramic capacitors screened to tolerances of ±1%. Again, garden-variety amplifiers, like the 4136 quad, perform well enough for the purpose. □

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Designing with nitride-type EAROMs

Being nonvolatile and reprogrammable, electrically alterable read-only memories fill the needs of such systems as TV tuners, phone dialers, and point-of-sale terminals

by Brian Cayton, *General Instrument Corp., Microelectronics Division, Hicksville, N. Y.*

☐ Attracting the attention of digital-system designers is the electrically alterable read-only memory, or EAROM. First available in volume production about a year ago, the electrically alterable ROM is unique among semiconductor memories in combining nonvolatility with reprogrammability. Like the ordinary ROM, it needs no power to retain data; and like the random-access memory, it is electrically erasable and system-reprogrammable over and over again—in contrast to the 2708-type reprogrammable ROM, which requires ultraviolet light for erasure. In other words, the device operates like an erasable ROM or a nonvolatile RAM.

As such, it fits the needs of a good many electronic systems better than either a RAM or a ROM. For instance, it is perfect for storing channel voltages in inexpensive digital television varactor tuners. In telephone dialing systems, it is the most efficient way of storing and updating phone numbers. It can be designed into point-of-sale terminals for updating inventory and price information or into industrial control equipment for storing process routines or numerical-control data. It can even be built into security systems as part of an electronic lock storing a code the owner can change at will.

Moreover, while not intended for mainframe applications, which require RAMs with access times in the 150-to-300-nanosecond range or for main program storage, which requires ROMs in the 500-ns range, MNOS alterable ROMs are improving dramatically in speed. Access times in new devices are as fast as 750 ns, and erase and write times are in the 10- and 1-millisecond ranges respectively. This makes their performance a perfect fit in systems wherever human input over a keyboard or a dial controls the operation, as in phones, TV sets, or calculators, and where high speed is not critical, as in some microprocessor-based systems, such as point-of-sale terminals and surveillance gear.

The longest-established way of making semiconductor storage nonvolatile is to put a nitride layer beneath the memory's metal-oxide-semiconductor gate electrode. This method is used in the memories listed in the table below. (Electrically alterable ROMs using an alternative approach—a floating-gate structure—have recently become available and are compared to the MNOS types in "An alternative," p. 110.)

A lucky chance

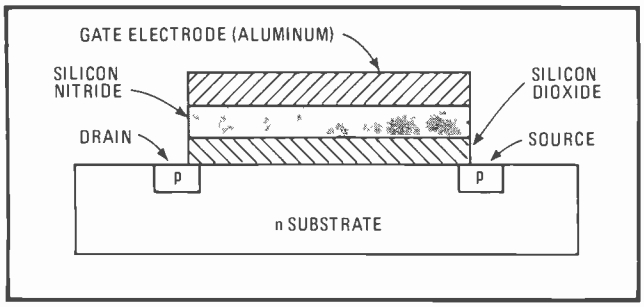
Like so many discoveries in electronics, nitride's value as a changeable yet permanent MOS storage mechanism was stumbled upon by accident. It all started with the standard p-channel MOS transistor, which with a negative bias applied to its gate repels negative charges from the substrate into the region forming the channel between the source and gate. At the same time, positive charges (holes) are attracted to the channel, changing it electrically from n- to p-type material and causing conduction between drain and source.

A simple MOS field-effect transistor of this type has an operating threshold voltage of 3 to 4 volts, too high to be driven by the 2-to-3-V signals of standard transistor-transistor logic. The most likely remedy appeared to be the substitution of silicon nitride for the silicon dioxide of the gate dielectric, because the nitride's higher dielectric constant and greater resistance to ion migration were expected to lower threshold voltage.

But to the surprise of the early experimenters, the silicon-nitride transistor exhibited an unstable threshold,

OPERATING TIME OF ELECTRICALLY ALTERABLE READ-ONLY MEMORIES

Part	Size (bits)	Organization	Alterability	Read access time (μs)	Write time (ms)	Erase time (ms)
ER1105	1,024	256 by 4	block	2	10	100
ER1400	1,400	100 by 14	word	–	10	10
ER2050	512	32 by 16	word	6	100	100
ER2401	4,096	1,024 by 4	chip	2	10	100
ER2800	8,192	2,048 by 4	chip	2.6	10	100
ER3401	4,096	1,024 by 4	word	0.95	1	10



1. The basic transistor. To decrease their operating threshold, MOSFETs use a silicon-dioxide–silicon-nitride sandwich as their gate oxide. Without the dioxide, the nitride would store charge—a characteristic exploited in nonvolatile MOS memory design.

one that varied up and down as the device was switched off and on. It turned out that charges were tunneling from the substrate into the nitride and being held there in "trap sites." So device specialists were quick to abandon this simple nitride structure for one containing a layer of silicon dioxide deposited between the silicon nitride and the silicon substrate (Fig. 1). In this structure, the so-called metal thick-oxide nitride semiconductor device, the oxide was thick enough to prevent charges from tunneling through into the nitride layer, yet thin enough to exploit the superior silicon-nitride characteristics. This MTNS transistor, which was stable and possessed a TTL-compatible threshold, became the basis for today's mainline MOS device technology.

However, in the late 1960s, researchers found that they could harness the hysteresis effect of the older silicon-nitride devices by reducing the thickness of the silicon dioxide from 500 angstroms to approximately 25 angstroms. Being so thin, the silicon dioxide allows charge to tunnel through it when a high enough voltage (25–30 v) is applied to the gate. This charge is then trapped in the silicon-dioxide–silicon-nitride interface, and since both the oxide and the nitride are high-quality insulators, it remains trapped for a very long time. (Data retention for General Instrument devices is guaranteed for 10 years.) This nitride structure is basic to today's MNOS memory devices.

A typical MNOS transistor is put (or written) into the low-condition state by the application of −25 to −30 v to the gate. This drives electrons from the interface region through silicon dioxide into the silicon substrate and leaves the interface region with a net positive charge (Fig. 2a). The charge has the same effect as a positive gate bias, opposing the field produced by normal logic-level, negative signals applied to the gate. The result is a very high threshold, typically −12 v, and this condition serves as the off state of the transistor.

How it works

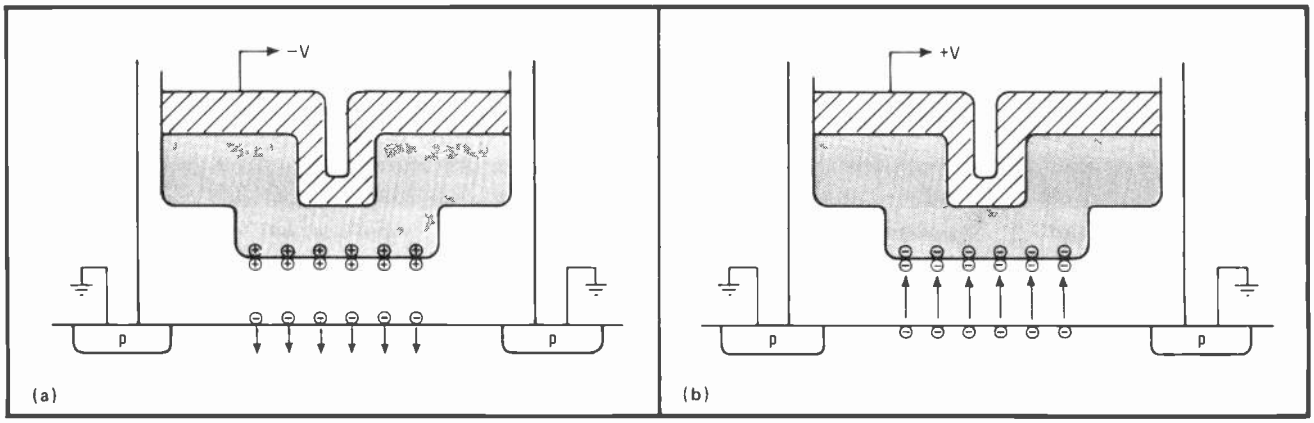
To put the cell into a low-threshold (high-conduction) or on state, a positive voltage is applied to the gate (Fig. 2b). This positive voltage attracts electrons into the interface, producing a negative charge that aids negative logic signals applied to the gate.

The memory transistor illustrated is, unfortunately, not quite practical: in the erased state, the threshold may be so far below the transistor's bias voltage that the device is always on. Additionally, the gate-enhanced source-to-drain junction breakdown is so low as to cause unreliable operation.

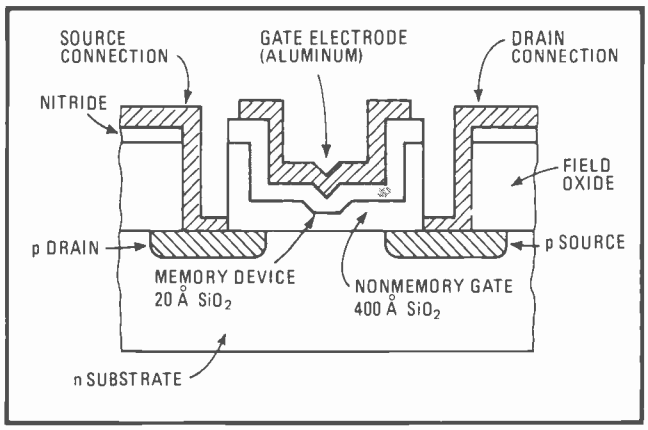
Both of these problems are solved by the three-gate structure shown in Fig. 3. In this structure, the high-threshold state is still approximately −12 v. But because the oxide in the noncritical gate region is now at least 10 times thicker than in the thin storage area—400 as against 25 angstroms—the low threshold is pegged by this nonmemory region to approximately −2 v.

Moreover, in this three-gate structure, it is possible to tailor the process parameters to fit the best possible tradeoff between data retention and erase/write or switching time. As the thickness of the silicon dioxide is decreased, the shortened charge-injection path decreases switching time. The thinner oxide, however, also allows easier charge leakage and so decreases data retention. On the other hand, increasing the nitride trap density allows faster writing and erasing, but creates dispersion paths through the nitride, shortening data retention. The decision at General Instrument was to adjust these parameters to obtain a minimum data retention of 10 years and then optimize write/erase time. The ER3401, for instance, has a guaranteed write time of 1 ms and an erase time of 10 ms.

The simplest of the circuits that can write and read



2. Writing and erasing. To write into an MNOS memory, a negative voltage is applied to the gate (a), repelling electrons from the nitride trap sites in the silicon-oxide–silicon-nitride interface and setting up a net positive charge. Conversely, erasure of data from the MNOS memory uses a positive voltage (b), which attracts electrons and results in a negative charge at the storage interface.



3. What the three gates do. This three-gate structure allows the MNOS memory designer the optimum tradeoff between storage-gate thinness and nonstorage-gate thickness. Here a 20-angstrom-thick silicon-dioxide layer in the center of the channel allows charge to tunnel from the memory's substrate to the oxide-nitride interface when a high enough voltage is applied to the gate.

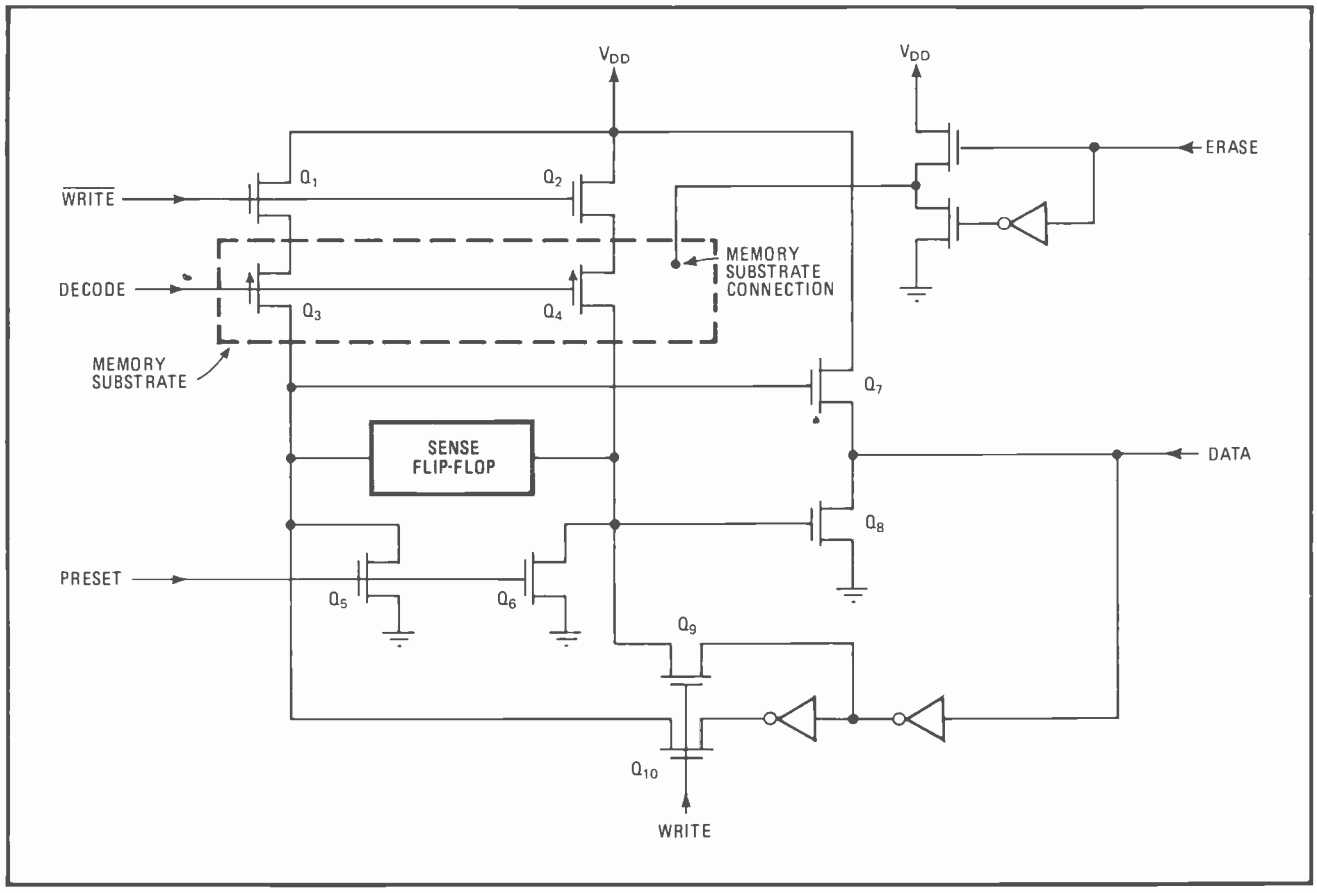
and erase data is the two-transistor structure shown in Fig. 4. (This cell is used in the 512- and 1,024-bit alterable ROMs listed in the table on p. 107.) The flip-flop detects whether an addressed memory location is in the low- or high-threshold state over a range of input voltages. The same circuitry also writes a bit into or erases it from the memory cell.

The cell's operation is unusually simple. Each contains two transistors. Before writing, both transistors are erased by being put into the low-threshold state.

To write, the gates are then biased with a negative signal, and the flip-flop is switched into the desired state. One memory transistor will then have a high gate-voltage threshold, indicating a bit has been written into it; the other, which still is kept at source potential, continues to have a low threshold. Reading is then simply a matter of using the sense flip-flop to detect the high-threshold transistor. In the erase mode, the drains of memory transistors are placed at a negative potential, as is the memory substrate. The decoder circuitry then positively biases the gates of the memory transistors at the selected address, erasing their contents.

Figure 5a is a simplified schematic of the device in the write mode. Q_1 and Q_2 are biased off, leaving the drains of memory transistors Q_3 and Q_4 floating. In this state the memory gates are biased negatively. Pass transistors Q_9 and Q_{10} are on, allowing the data signal and the inverted data signal to pass through to transistors Q_3 and Q_4, respectively. Now, if the data is a logic high (positive), Q_3 will see a negative gate-source potential and will be written. Q_4, which has its gate source at the same potential, will remain in the erased state.

In the read mode (Fig. 5b), Q_1 and Q_2 are on, providing supply voltage to the memory transistor drains. As the first part of the read sequence, an internal clock sends a preset signal to transistors Q_5 and Q_6, momentarily shorting the outputs of the sense flip-flop,



4. Two transistors. The flip-flop of this two-transistor cell detects whether an addressed memory location is in the low-threshold or in the high-threshold state over a range of voltages. The same circuitry also writes bits into the memory cell and erases them.

An alternative

Besides nitride storage, another means of building electrically alterable read-only memories is the floating-gate metal-oxide-semiconductor or Famos technique.

In the Famos process, the need for a thin oxide in the critical gate portion of the device is overcome by the use of two gate layers. One layer is buried in an insulating oxide and kept floating with reference to the substrate's voltage potential, while the other is deposited on top of the oxide and connected to the control circuitry. Data is then stored by charges trapped on the floating gate.

However, no hard connection is made to this floating gate. Also, to isolate it properly from the control gate, the oxide used to separate the two must be at least 1,000 angstroms thick—which is too thick to allow charges to tunnel in and out as in the metal-nitride-oxide-semiconductor structure. Thus writing and erasing are more difficult than with the MNOS device. With Famos cells, the trick is to apply a high enough voltage long enough to break the junction down without destroying it—a definite hazard to reliability, especially as −36 volts and 50 milliamperes are needed to do the job.

This is not the only drawback of the Famos structure. No means of word erasure exists, so the entire device must be erased, and this burns power. For example, erasing a 2,048-bit Famos device requires a supply of 76 V and peak current of 300 mA, or a power rating of over 20 watts. The erase times (60 seconds) are also much longer than for MNOS devices. As for writing, the Famos μPD454, as shown in the accompanying table, needs a supply of 28 V for 100 ms, a lot of power.

COMPARISON OF MNOS AND FAMOS ELECTRICALLY ALTERABLE ROMs

Type	Bits	Write		Read		Erase		Comments
		Voltage (V)	Time	Voltage (V)	Time	Voltage (V)	Time	
μPD454	2,048	−2, +26	100 ms	+5, +12	800 ns	+36, −40	60 s	voltage to pins must be switched
ER3401	4,096	+5, −12, −30*	1 ms	+5, −12, −30*	950 ns	+5, −12, −30*	10 ms	word erase or block erase

*no supply switching necessary

thus sensitizing the flip-flop. Then a reference-level signal is provided to the memory transistors. As the erased or low-threshold transistors will have a lower impedance than the off or written transistor, one side of the flip-flop will see a higher potential; this sets the flip-flop, so that it is ready to drive the output transistors Q_7 and Q_8, which form a totem-pole output driver pair.

Although this circuit is fine for memory devices not requiring high density (1,024 bits and less), its use of two transistors per memory cell is a drawback. For higher-density, 4,096- and 8,192-bit electrically alterable ROMs, a one-transistor cell is better (Fig. 6). In this configuration, as with the two-transistor cell, erasing is necessary to precondition the cell before writing. This is done by biasing the gate with a potential that is positive with respect to the substrate. The memory cell is then in the low-threshold (logic 0) state. To produce a high-threshold (logic 1) transistor, the gate is pulsed with a negative voltage.

For reading these states, the gate of the memory cell is provided with a reference bias voltage. A threshold lower than the reference holds the cell off; a higher threshold turns the transistor on. A constant current-source is used to overcome any leakage that might occur from the charged cell to the substrate.

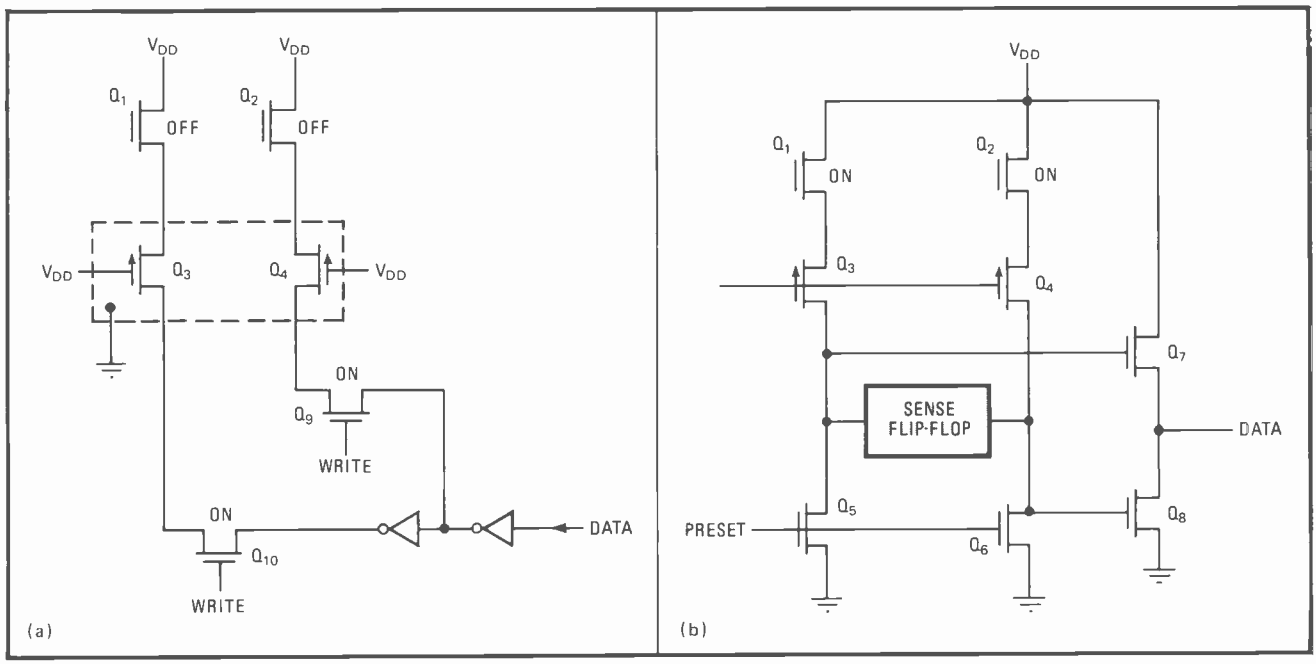
Although not apparent from the circuits shown in Figs. 4 and 5, the ability to put a complete memory on a single MNOS chip required innovative processing as well as clever circuit design. Early alterable ROMs were complicated to use because positive gate voltages were required to erase each cell. Since there was no way of internally switching the high positive voltage required at the memory transistor gates, these gates had to be brought directly out to pins. It then was up to the user to decode the gates with externally generated signals.

Processing helps, too

Epitaxial wafer processing, a technique developed for bipolar transistors, provided a means of on-chip decoding. By separating the MOS gate from the substrate with an epitaxial layer, a boron diffusion can successfully isolate the gate-memory portion of the circuit from the logic and decoding.

Secondly, because the memory substrate is now isolated from the logic circuitry, the memory cell's input voltage can be made independent of the voltage required for the logic circuitry. If the memory transistor gate is held at ground and the epitaxial layer is biased in the negative direction, a positive gate-substrate potential results that erases the device. The epitaxial layer can alternatively be held at ground, while the gate is negatively biased to allow writing. This makes it possible to design parts that are not only chip-alterable, in which an erase command erases the entire chip, but also word-alterable, in which the user can address and erase one word at a time without disturbing the contents of other memory locations.

Thirdly, once the voltage-switching circuitry has been placed outside the memory substrate on the fixed-potential substrate, all control signals can be made TTL-compatible, while on-chip circuitry can buffer and amplify them to switch supply voltages internally. This



5. Writing and reading. In the write mode of an MNOS memory cell (a), Q_1 and Q_2 are biased off, and the drains of memory transistors Q_3 and Q_4 are left floating. With pass transistors Q_9 and Q_{10} on, the data signal and inverted data signal pass through to Q_3 and write a bit onto the storage transistor. In the read mode (b), the flip-flop transistor pair sends a signal to the output totem pole driver Q_7 and Q_8.

makes the alterable ROM as easy to use as a RAM.

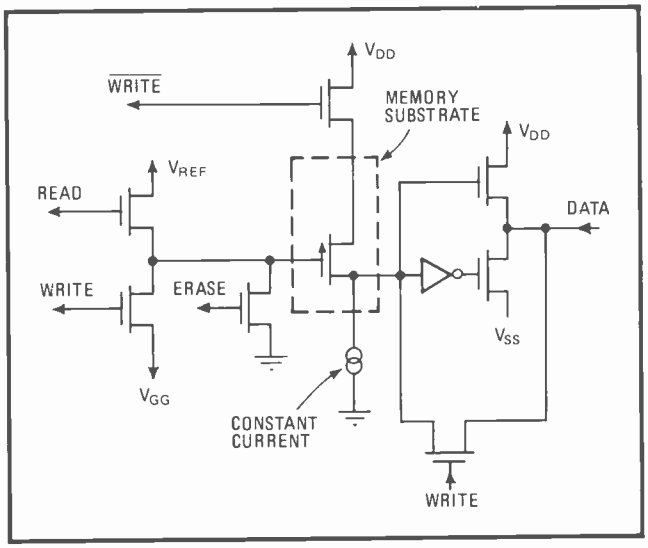
The use of epitaxy grants yet a fourth benefit, for it permits zener diodes to be fabricated with better characteristics than normal MOS processing can give. Accurate-value low-impedance zener diodes provide excellent static protection, besides serving as on-chip regulated voltage supplies.

Testing an alterable ROM

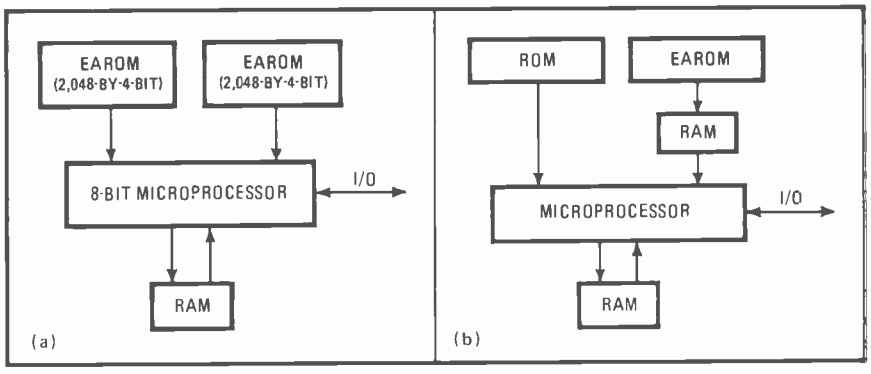
With alterable ROMs, the testing of factory parts is relatively straightforward, consisting of writing and then reversing in checkerboard fashion all 1 and then all 0 test patterns. As is the case with ordinary ROMs, the more sophisticated test patterns used in dynamic RAM are not required, since the relatively static nature of the data storage makes soft failures and pattern sensitivities unlikely.

Tests for data retentivity require plotting the decrease in threshold voltage with time. Fortunately this degradation follows a predictable relationship, requiring just a few points.

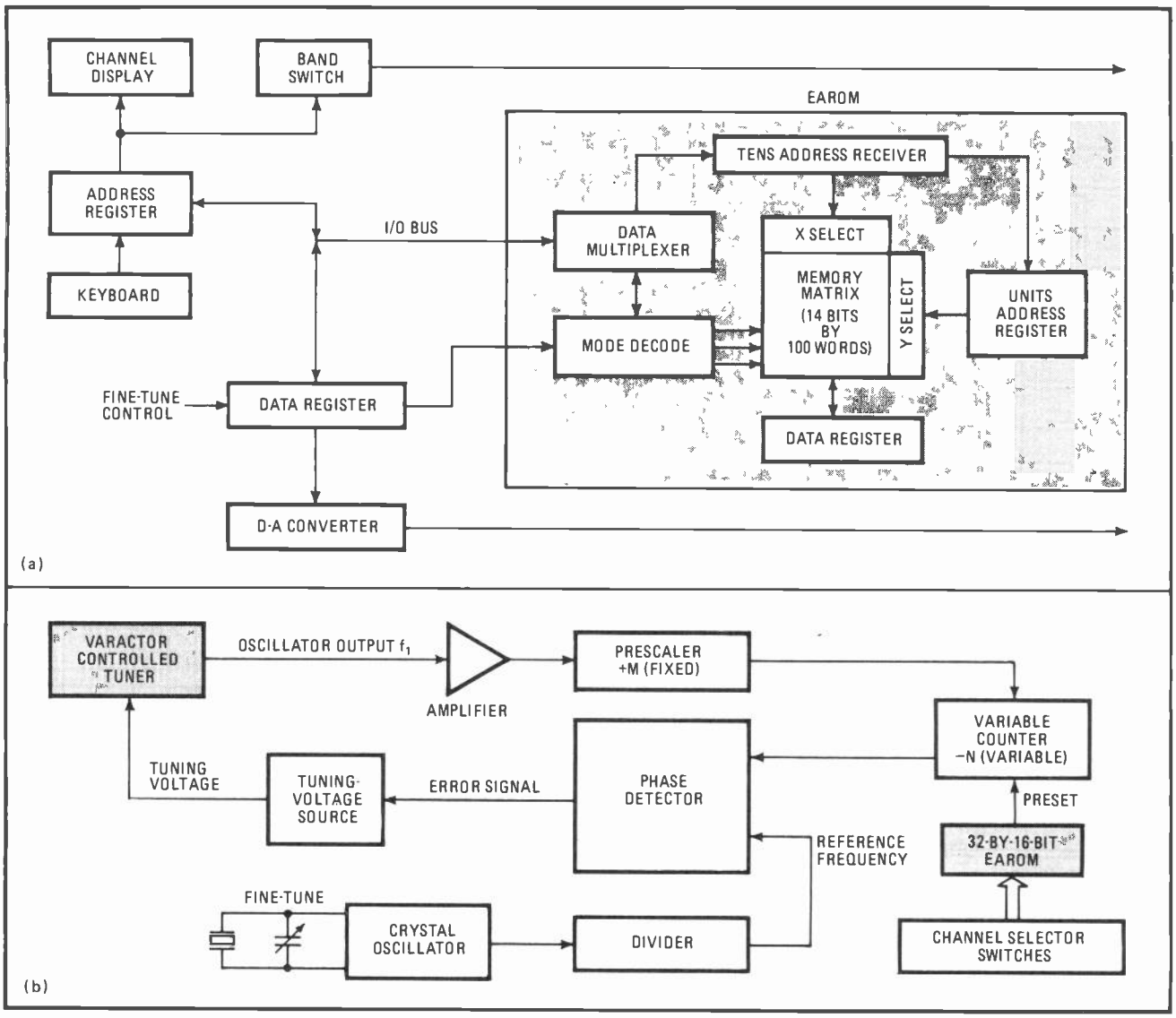
As for testing for threshold voltage, since it could vary with individual part types, each type is tested for its



6. A more compact design. Intended for use in high-density electrically alterable ROMs, this one-transistor cell is erased by having its gate biased positively and read when the threshold is compared to a reference standard. A constant current source overcomes any leakage from the charged cell to the substrate.



7. Up to date. In microcomputer-based systems such as point-of-sale terminals, the electrically alterable ROM can be used as a nonvolatile data store for updating inventory and price information. If the access time is a key factor in the application, a low-cost RAM may be used to receive the alterable ROM's contents on system power-up.



8. Tuning a television set. In varactor tuning (a), the electrically alterable ROM stores digital information that goes to a digital-to-analog converter to provide the proper bias to the varactor. In phase-locked-loop systems (b), the alterable ROM stores the proper division information for the various desired channels by controlling the count ratio of the variable counts.

internally generated voltage reference, and the threshold voltage is maintained at sufficiently reliable levels above this reference. This is done by varying the bias voltage until the point is reached at which the output of the memory cell is switched. This adjustment can be done either as wafer mapping, wafer probe, or final die testing. In addition, all devices are "margin tested," a process that consists of measuring the reference voltage, V_{ref}, and then increasing or decreasing it by an amount determined to be equivalent to the change in threshold over 10 years.

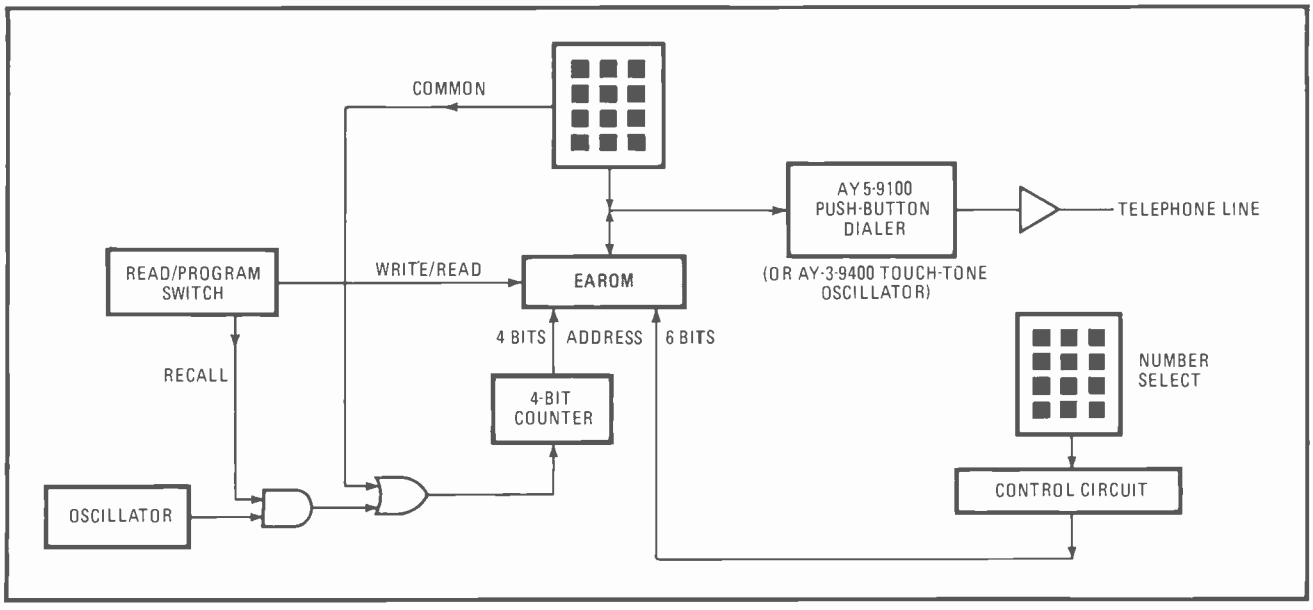
Applying the alterable ROM

Though the electrically alterable ROM is too new to have accumulated a reservoir of general application information, several basic configurations have already emerged to guide a system designer. Figure 7 shows two microprocessor-based systems that use the device.

In systems in which the microprocessor controls cash registers or other peripheral equipment that uses manual input, the electrically alterable ROM provides local nonvolatile data storage that can be frequently updated. This is the configuration of Fig. 7a, where the program information handled by the two 2,048-by-4-bit ER2800 alterable ROMs is extensive enough to cope with the inventory of many supermarkets and department stores. The 2-microsecond read times of these devices satisfy the needs of even the fastest cash-register operator.

Other systems, while still requiring some nonvolatile reprogrammable memory, may need part of their data to be immediately accessible to a computer. A credit-card−cash-register point-of-sale terminal is an example. Any data needing fast access would then be programmed into an ordinary ROM while the inventory data would be coded into the alterable ROM. Since the two kinds of ROM are generally compatible in voltage, power, and pinout configurations, the same printed-circuit board can hold both, with standard interface circuits used in reprogramming the alterable ROM.

Another configuration (Fig. 7b) combines an alterable



9. Dialing. An electrically alterable ROM in a repertory dialing system stores telephone numbers, which are then automatically supplied to the dialing mechanism when requested by the user. This 4,096-bit memory provides enough data to handle 64 16-digit numbers.

ROM with a RAM to handle real-time situations where the system must meet the requirements of many different stores yet also react quickly to an individual store's needs. On these occasions, where faster access times are required than the alterable ROM can provide, the device can automatically dump its contents into an inexpensive RAM on system power-up. The RAM then provides the program information, leaving the alterable ROM free to be updated at leisure. Moreover, although not intended as a scratchpad memory, the alterable ROM can also be used with the RAM to provide data storage off line—a configuration that could be useful for obtaining running totals, say.

Large quantities of alterable ROMs are also being used in digital TV tuners, which exploit both the nonvolatility and the reprogrammability of the devices. In the Omega system developed by General Instrument (Fig. 8a), the alterable ROM stores tuning information needed by the varactor but formerly provided by much more expensive potentiometer banks.

It works like this. The digital tuning information is passed through a digital-to-analog converter to supply the varactor with the proper tuning voltages. But since varactors differ from device to device, these voltages need tweaking, and if this is done with potentiometers during assembly, it is a costly operation. An alterable ROM, however, can be preprogrammed with the digital information that goes to the converter, adjusting for the varactor variations and providing a cheap and very accurate method of obtaining the right voltages (See *Electronics*, April 1, 1976, p. 86, for a full description.)

An alterable ROM can also be used to store the viewer's own fine-tuning settings. Here, after selecting a channel, the viewer fine-tunes the set by incrementing or decrementing the data register with a simple chassis switch. When he or she releases the switch, the data is loaded back into the alterable ROM so that it always contains the most up-to-date information.

Tuning applications are not limited to simple open-loop tuners. A phase-locked-loop tuning configuration controlled by an alterable ROM is shown in Fig. 8b. In typical phase-locked tuners, channels are selected by varying the counter division ratio, which changes the phase-locked loop frequency. In this circuit, the alterable ROM stores the proper division information for the various desired channels, controlling the count ratio of the variable counts.

In operation, the crystal oscillator frequency is divided down to provide a stable reference. The variable counter, in conjunction with the prescaler, divides the local oscillator to a frequency close to the reference. The two signals are then fed to the phase detecter. Any error between the reference and the present frequency is used to adjust the varactor tuning voltage, reducing the error and locking in the desired station.

In locks and dialers

In an electronic door lock (Fig. 9), the alterable ROM stores the key code, which may be periodically changed by the user against unauthorized entry. To drive the latch that opens the lock, data from a keyboard is compared with the data from the ROM and at the same time fed to a counter. Any error in the data will inhibit the unlatch signal. But if the full string of numbers is entered into the counter without error, the counter overruns, the solenoid is powered, and the door latch opens.

Finally, there is the telephone repertory dialer of Fig. 10. This system uses a 4,096-bit alterable ROM to store 64 16-digit numbers. To select a number, the caller uses either a push-button pad or a thumbwheel switch to enter 6 address bits. In the program mode, the keyboard provides binary-coded-decimal digit data as well as a common signal for incrementing the address counter. As each button is pushed, the digit is fed to the memory, and on completion of the phone number, the counter is incremented. To recall a number, the oscillator pulses the 4-bit counter, scanning through each of the digits of the desired telephone number. □