

# Electronics

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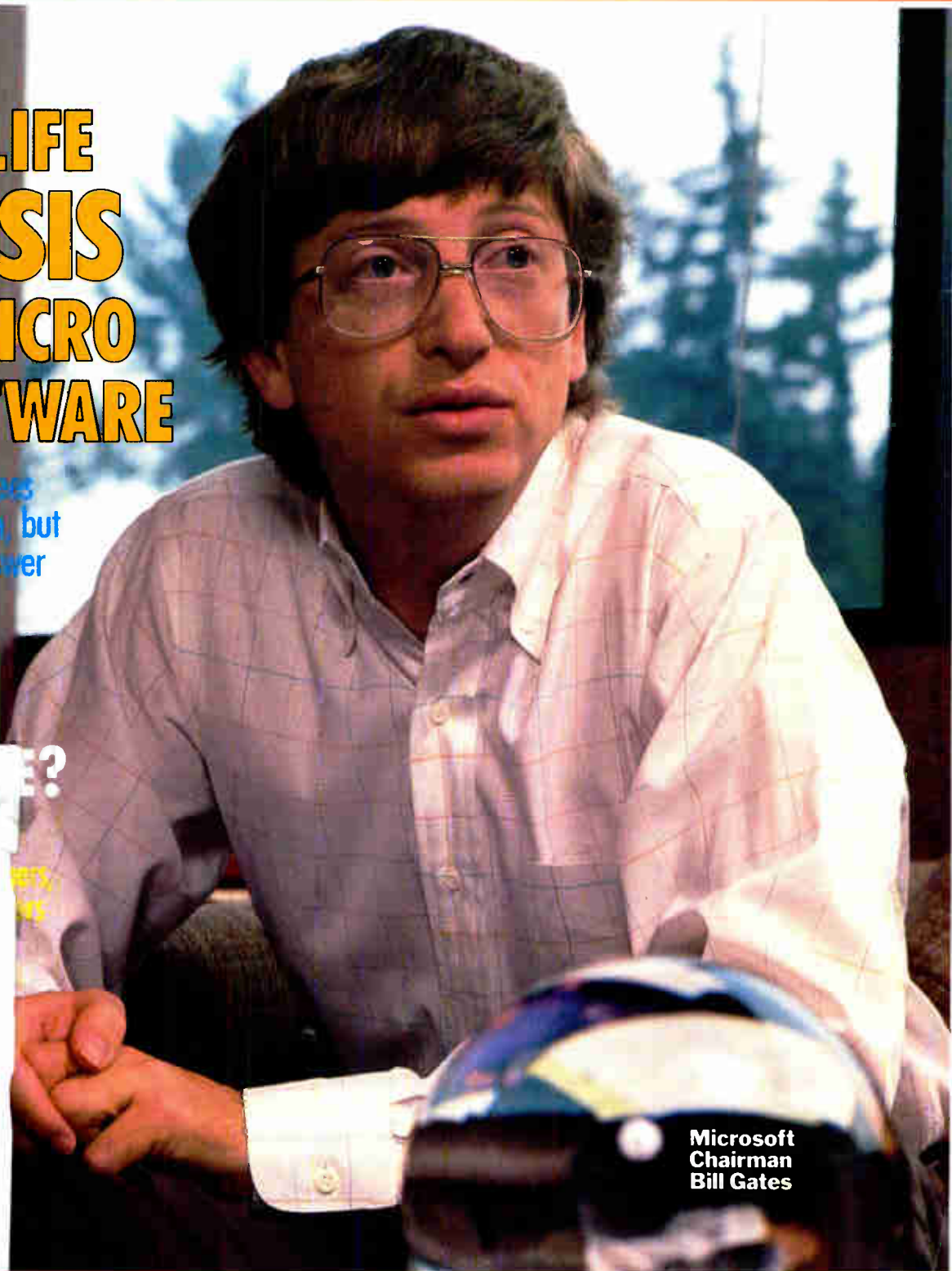
## THE MIDLIFE CRISIS IN MICRO SOFTWARE

Bill Gates sees the problem, but no easy answer

PAGE 68

### WHY

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Microsoft Chairman Bill Gates

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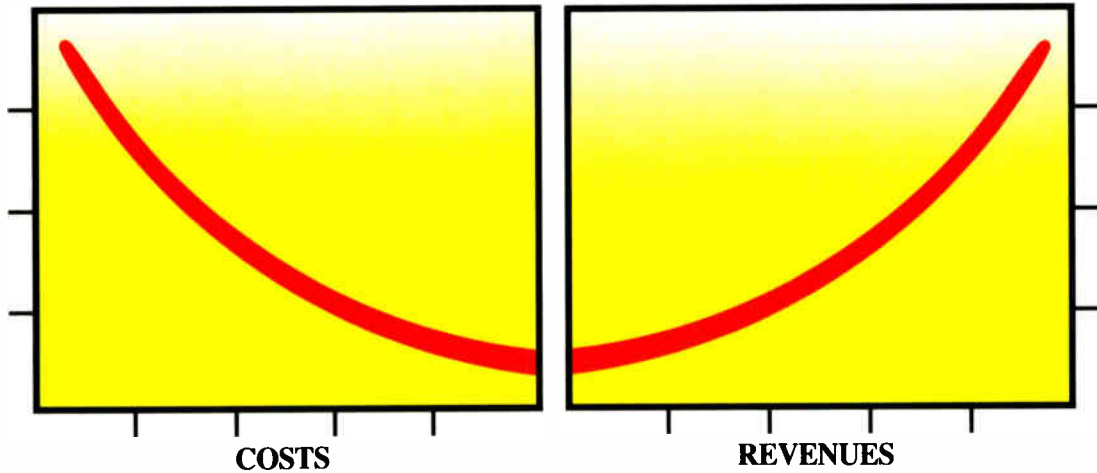
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## WHO NEEDS NEW SOFTWARE, ANYWAY?

Existing DOS-based applications never looked better, according to hardware marketers. Who do they think they're kidding?

What a season. The big leagues had played only a couple of games before Intel knocked the ball out of the park with its early April announcement of the 80486 microprocessor. Then, toward the end of May, just when the weather was getting hot enough for a pitcher to limber up his arm, Compaq stole home with its announcement of a new series of 33-MHz, 80386-based desktop machines employing 64-Kbyte cache controllers (see p. 20). The top of the line in this series sports a 650-Mbyte hard disk and sells for \$18,000. And talk about stats—Compaq had the temerity to benchmark its new machines not only against the IBM PS/2 models they were designed to exceed but also against two midrange computers from IBM and DEC. You guessed it, Compaq's 386 outperformed the 9370 and VAX in multiuser configurations with up to 38 users.

Now that Compaq is competing with work-station and minicomputer vendors—at least Compaq CEO Rod Canon believes it is—the price/performance numbers games should heat up a little. Work-station prices have swooped down, while the hanging of bells, whistles, and voluminous mass storage on 386 PC clones has catapulted prices for the top of the line up to where Sun Microsystems shines.

Referring specifically to a hardware matchup against Sun, Canon cited the IBM PC compatibles' Industry Standard Architecture and the vast array of DOS-based software applications as factors that should keep work-station vendors in their place. There it is again, the old compatibility ploy—you can't turn your back on those "thousands of applications."

But somebody—a very significant somebody—doesn't agree that existing software applications are a sufficient basis for marketing high-end desktop systems: Microsoft chairman Bill Gates (see cover and p. 68). Gates recently told *Electronics* that the clamor for new applications among users is really their way of asking for a reason to invest in high-end desktop machines. By Gates's own admission, the industry in which his company is a dominant force is a long way from meeting that demand.

Perhaps the software fraternity isn't running out of steam. Perhaps it's only the current rapid-fire pace of hardware innovation that exacerbates the gloom over product delays from software marketers. Perhaps there is a correlation between the positive light in which the financial community regards Compaq, a company that doesn't announce products it is not prepared to ship, and the negative reaction to delays announced by companies, like Microsoft, that make preemptive preannouncements.

However these forces come together, one thing is clear: hardware alone won't bring desktop computing to a new level. Entirely new applications, a better user interface, and improved end-user development tools all need the immediate attention of anybody who expects to make a living selling desktop systems.

**ROBIN NELSON**

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# Electronics

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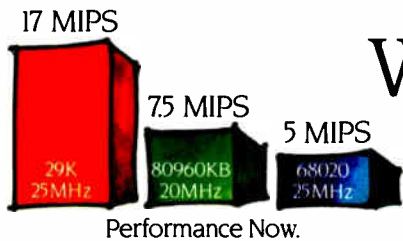
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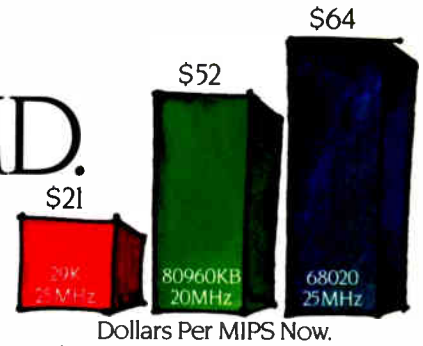
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### LETTER FROM NORTHERN VIRGINIA

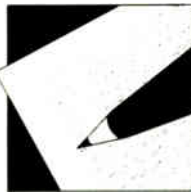
# BELTWAY BANDITS FATHER A HIGH-TECH COMMUNITY

#### ALEXANDRIA, VA.

The typical recipe for a successful startup community begins with a broad university infrastructure and a dynamic, risk-taking financial sector. That's been the model in Silicon Valley as well as along Boston's Route 128 and in smaller centers near Atlanta and Princeton, N. J. But at the northern tip of Virginia, where the Potomac River takes a westerly turn—and separates Maryland and Washington, D. C., on its north shore from the land where George Washington farmed tobacco and cotton, on its south—a high-tech community is sprouting without the benefit of either of those prime ingredients.

**FILLING A GAP.** The Washington area has for years had its share of professional services companies—technical consulting firms and defense specialists derisively known as Beltway Bandits. But over the past decade, these businesses have evolved into technically proficient problem solvers as the government's computer, communications, and software needs outgrew its ability to cope on its own. Companies like Computer Sciences Corp., BDM International Inc., and ERC International Inc. stepped in to fill the gap and became the backbone of a growing technology community.

That's true not just for northern Virginia but for the entire 40-mile corridor that joins Washington with Baltimore. But though Maryland has certainly par-



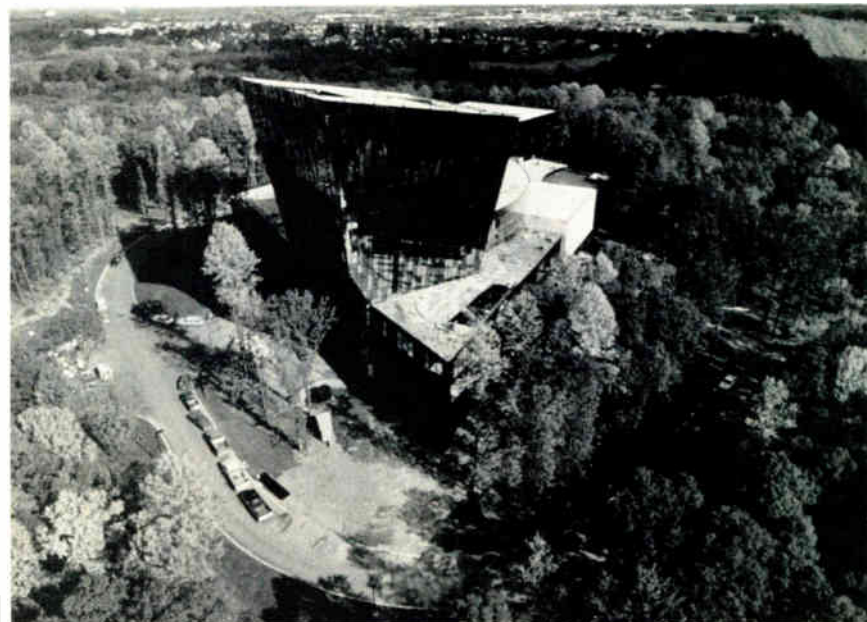
ticipated in the area's high-technology boom, most of the fastest-growing technology companies in the Washington area are in Virginia. These firms are springing up in the towns and developments surrounding Dulles International Airport, just

20 miles west of downtown Washington, in Herndon.

The centerpiece for this development is the state's Center of Innovative Technology. Housed in an inverted glass pyramid that stands out from the Herndon landscape, CIT is a nonprofit, state-supported operation dedicated to developing the state's technological prowess. Its \$12 million budget supports eight technology institutes and centers at Virginia universities and a series of incubator facilities, including one at George Mason University in nearby Fairfax.

CIT, along with George Mason, were key factors in luring the Software Productivity Consortium to Herndon, where its 125-person staff is housed in a giant glass-and-cement parallelogram built by the state adjacent to CIT's pyramid. The consortium, a joint research venture of 14 aerospace companies, lends credence to the region's claim to be the fastest-growing software center in the country.

But if CIT and the area's professional services firms are the foundation of northern Virginia's high-tech community, large corporations are the mortar. The concentration of corporate headquarters,



The Center of Innovative Technology stands out as a striking symbol of Virginia's determination to become a high-technology center.



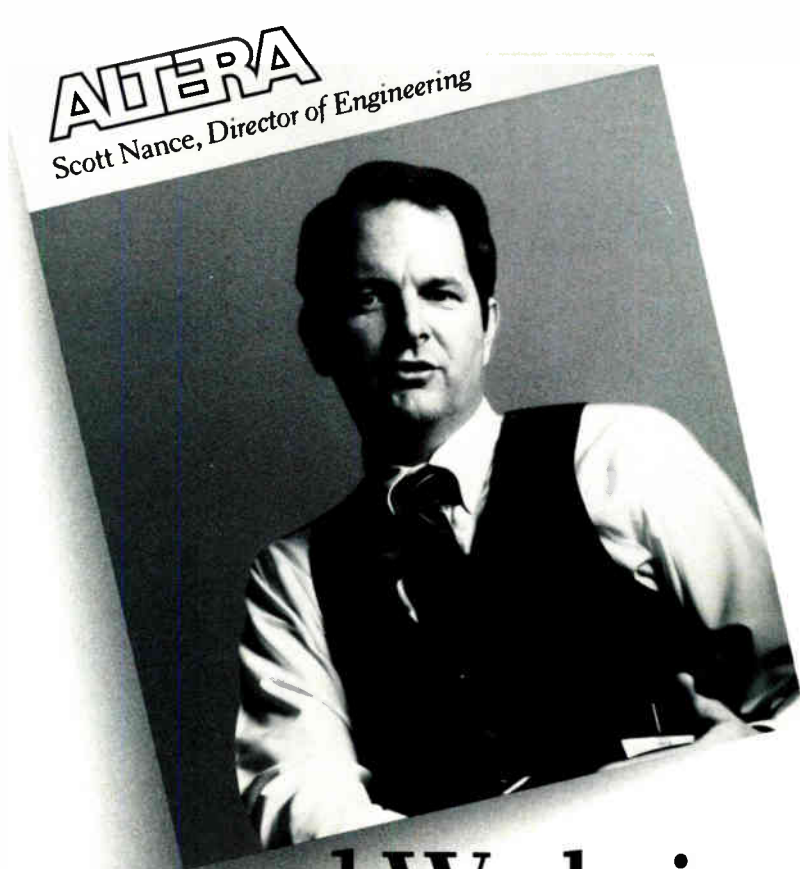
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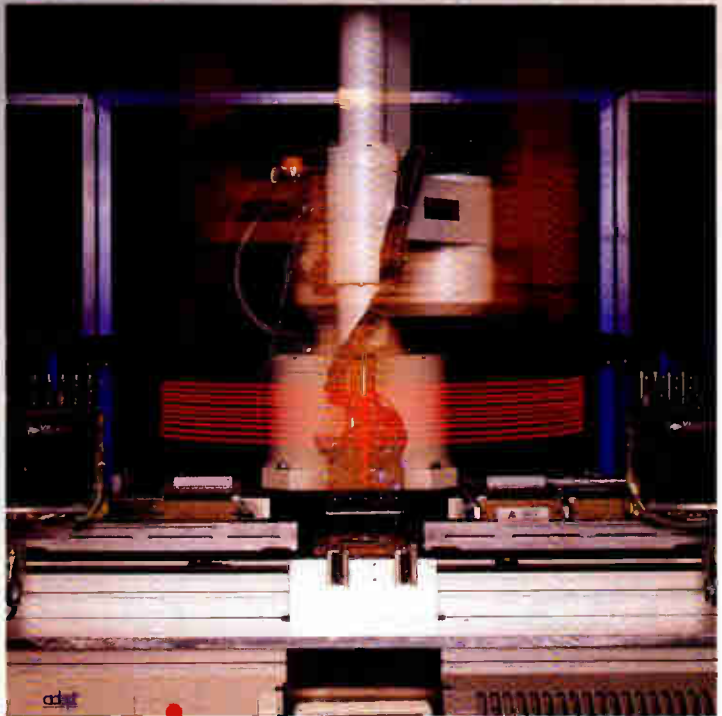
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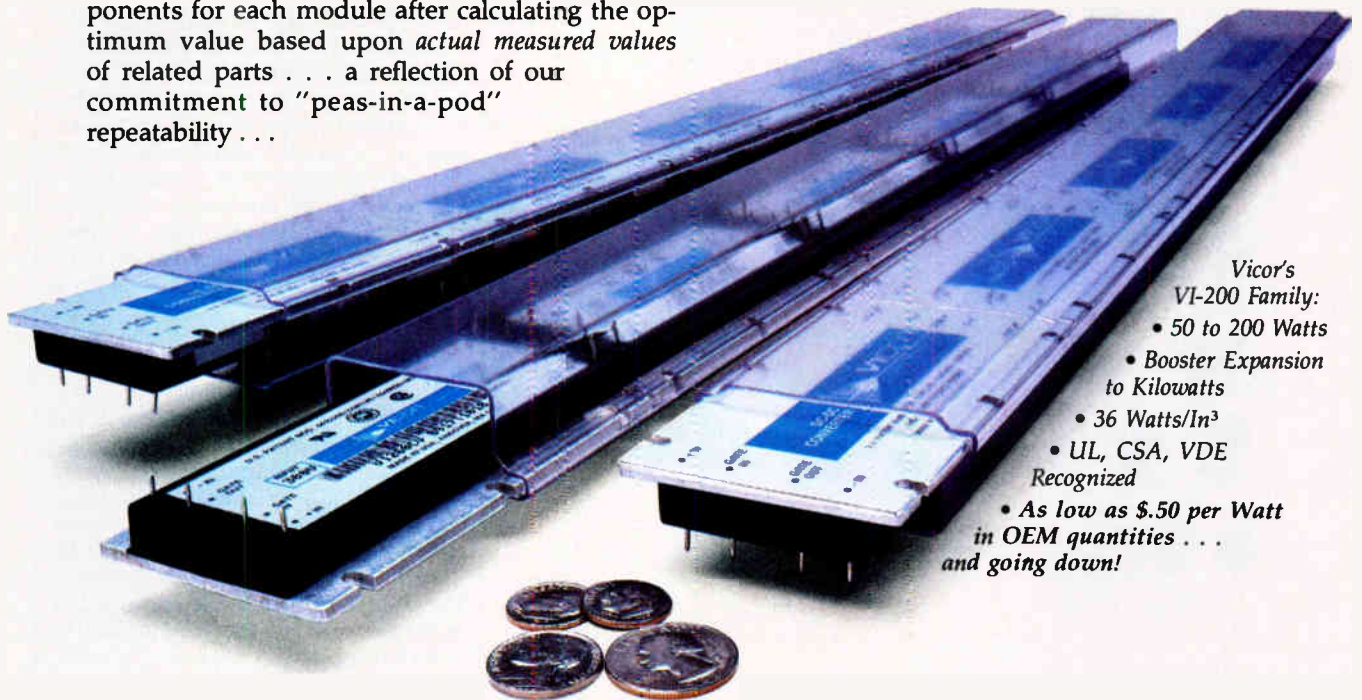
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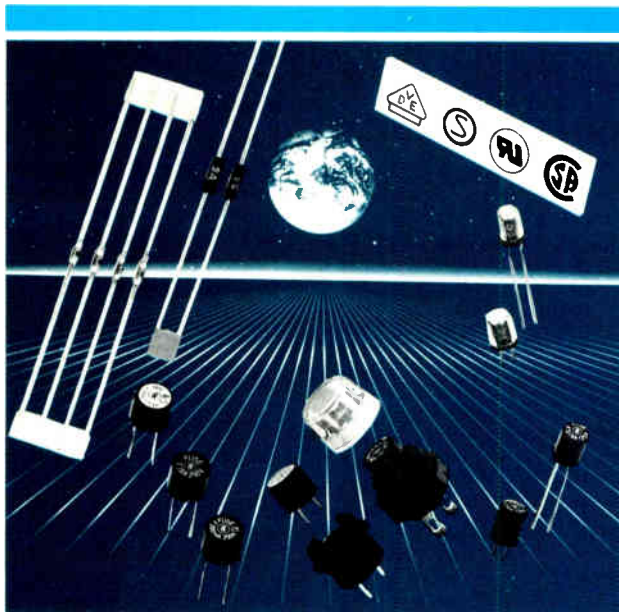
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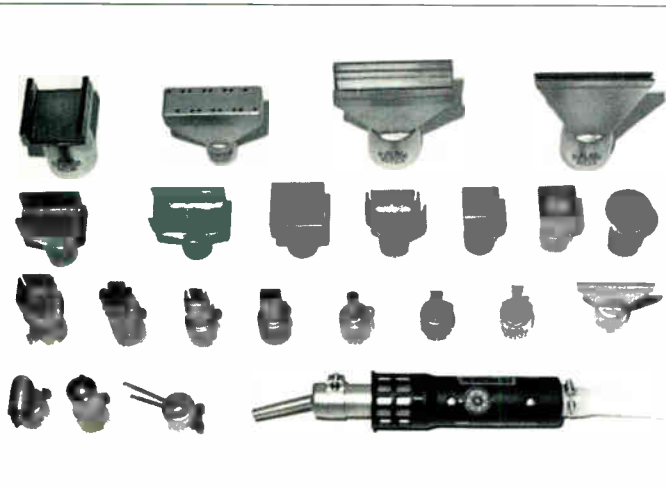
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such as Atlantic Research Corp. of Alexandria, and divisions of government and defense contractors, such as IBM Corp.'s Federal Systems Division in Manassas, combined with the professional services industry and CIT, has done for northern Virginia what Stanford University did for Silicon Valley: provide the talent pool to spawn a growing number of new high-tech companies.

"The area is finally getting a critical mass of technical people," says a Fairfax venture-capital investor. "There's a lot of startup activity." He points out, however, that the region's venture-capital funds are smaller and more conservative than the more famous funds in New York, San Francisco, or Boston, and that as a result, the area's startups are not on the scale of what can be found in those locales.

That's one reason so much of the local activity is in software and systems integration: the upfront investment for such ventures is much less than for, say, a startup chip maker. Of Virginia's 30 fastest-growing technology companies, 22 are focused on software development and systems integration and analysis.

**CAN'T MISS.** Of these, perhaps none has taken off as quickly as Verdex Corp., a Chantilly software house specializing in Ada-language software. Verdex was founded by a group of upstarts from Computer Sciences Corp., who saw the Defense Department's requirement that all military software be written in Ada as a can't-miss opportunity. They were right. Today, says Verdex president E. Gary Clark, the Ada development-tool market is growing at a 40% annual rate, and so far anyway, "We're keeping up."

Northern Virginia does have its problems, though. "There's a relative shortage of entrepreneurs around here because of the business base—it's a government town," says Stephen M. Hicks, president of United Software Security Inc. in Vienna. Government workers "may have very good technical expertise, but they don't bring the entrepreneurial flair and risk taking that's important to making a young company grow."

Star Technologies Inc., a Sterling computer maker specializing in high-speed array processors, has had similar problems. The company is one of a mere handful of hardware makers in the region. Says assistant controller Mark H. Schalk: "If we had it to do all over again, we'd probably locate in Minnesota." Star's original core staff of engineers was recruited from Control Data Corp. of Minneapolis. Several top engineers have since returned to Minnesota, leaving Star hard-pressed to replace them.

"It's hard to find people who know computer-aided design and have experience designing complex integrated circuits," Schalk says. "We're kind of out here on our own."  
—Tobias Naegele

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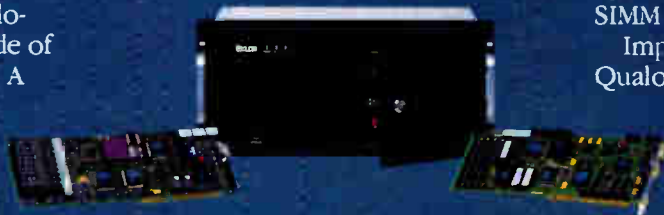
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computers win again. Our powerful **386** system is available in speeds from 16 MHz to a blazing **25 MHz** with up to 8 Megabytes of on board SIMM memory providing an alternative to VME based systems that can cost twice as much. The more economical Qualogy 286 single board computers sport speeds from 8 to 16 MHz with up to 4 Megabytes of on board SIMM memory.

Improve your score with Qualogy, call (408) 434-5200.



***Industrial PC/AT computers and peripherals.***



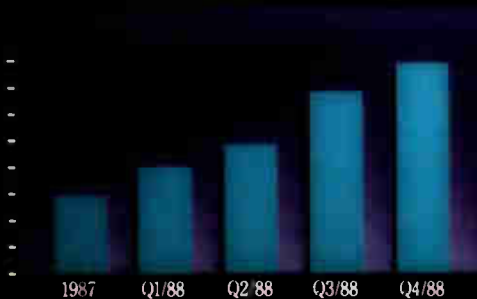
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Circle 52  
World Radio History



We've tested the future and it works.

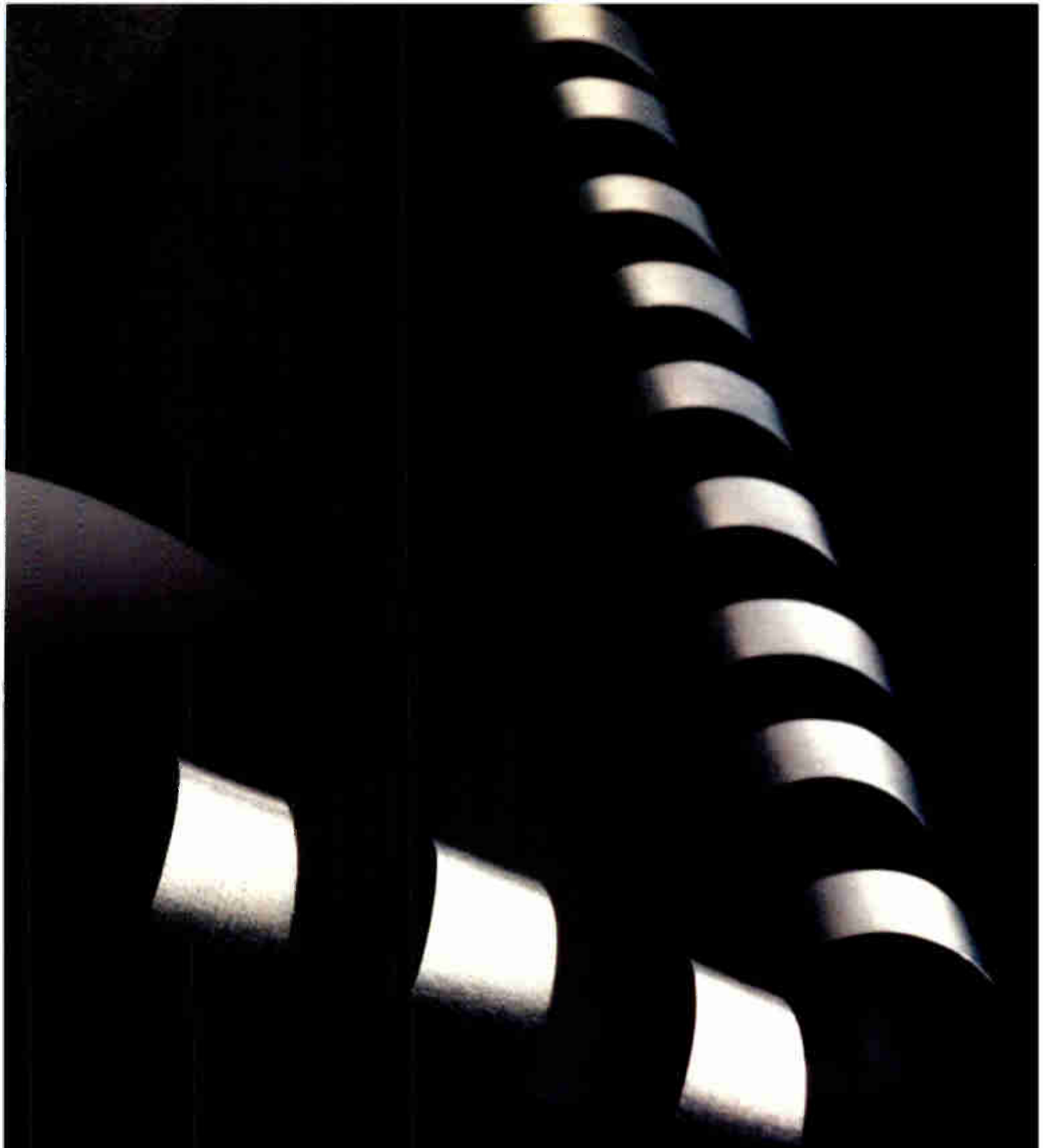


Eight of the top ten IC producers worldwide have chosen Teradyne systems to test next-generation devices. (Manufacturers' ranking per Dataquest.)

Tested by Teradyne. That's the edge that's helping the leading semiconductor and electronic equipment producers worldwide win the race to deliver their next generation of complex devices. These companies have chosen Teradyne systems across the range of VLSI applications – mixed signal, digital and memory.

**What makes Teradyne the overwhelming choice?** Whether you work with ISDN, RISC chips, color palette DACs, 32-bit microprocessors, 4-megabit memories or any





leading edge device, only Teradyne provides the superior technology you need to test devices thoroughly, while lowering your cost-to-test. Plus Teradyne's test floor management tools allow you to collect and analyze device performance data and make adjustments automatically to improve yields.

**Teradyne helps you test the future now.**

Teradyne's next-generation test systems are already in place, producing results for our customers, now. That means they're ready to help you cut critical product development time, fully

characterize your devices, and get your next-generation products to market faster.

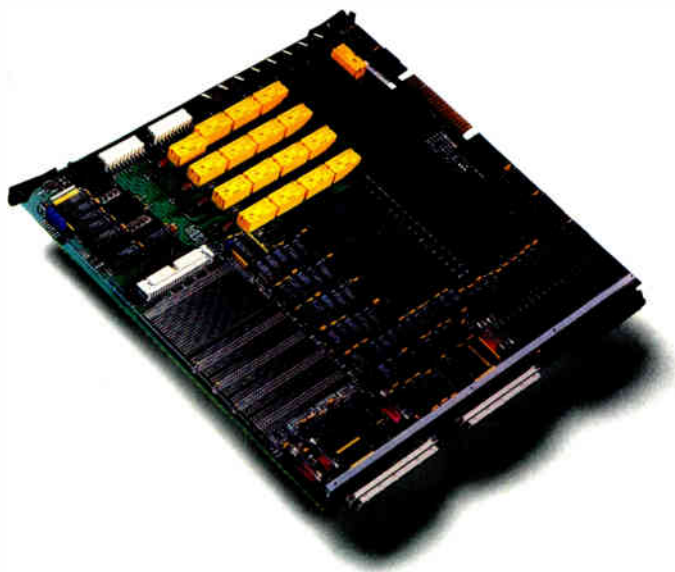
To find out how we can help you, call Terrence Drula at (617) 482-2700, ext. 2125. Or write him c/o Teradyne, 321 Harrison Ave., Boston, MA 02118. Or contact your nearest Teradyne office.

Teradyne Component Test Systems.  
What it takes to make  
the future work for you.

**TERADYNE**

Circle 19

# AGENTLE REMINDER ON THE IMPORTANCE OF LOOKING AROUND.



**C**ombinational Testers. Technically speaking, it's no longer a question of if or when you'll need one. But which system to choose.

Loyalty may take you first to the manufacturer of your present board testers. Logic should take you further.

Because the Zehntel 8000 holds a number of pleasant surprises for you — in power, flexibility, and price.

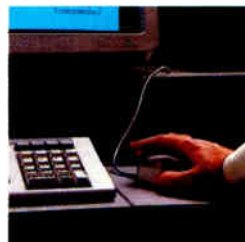
## BY ALL MEANS, COMPARE.

To appreciate its performance fully, it's only fair to judge the 8000 by comparable systems: those costing much more.

The 8000's open architecture, for example, can greatly reduce overall testing costs. Using the Functional Interface Board pictured above,

you can place your own hot-bed test directly into the 8000 system.

The 8000 is the only combinational tester with 2,048 fully-hybrid, non-multiplexed test points. Each node has a driver/receiver behind it; each can be used for either functional or in-circuit testing. All of which helps reduce the





cost of programming and implementing engineering changes.

The 8000's digital test subsystem truly warrants the term "high performance," with 10 MHz pattern rate, 8Kx4 RAM per node, programmable slew rates and 10ns programmable edge placement.

The menu-based, mouse-driven interface simplifies programming, with multiple windowing capability,

integrated logic analyzer and graphic quality analysis tools.

### A GENTLE REMINDER WHERE TO LOOK.

For complete information on the Zehntel 8000, call or write today. To help, we'll send you a specially-created reminder pad for your desk, inspired by the 8000's elegant industrial design.



### FREE REMINDER PAD

For your free notepad, call (800) 457-8326 or attach your business card here and send to:

**TERADYNE**

2625 Shadelands Drive  
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Offer expires  
July 31, 1989

ELEC/6/89

Circle 51

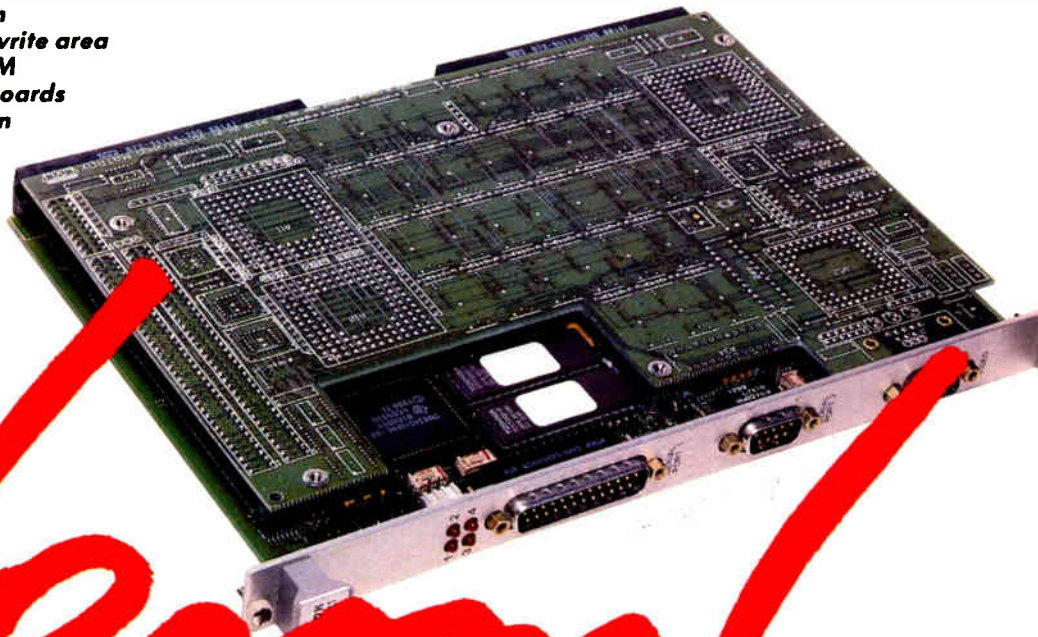


## THE VG-1281 GRAPHICS PROCESSOR

- 1280 × 1024 display resolution
- Fastest TMS34010-based design
  - 12.5 million pixels/sec. PIXBLT
  - 125,000 vectors/sec.
  - 30,000 characters/sec.
- 256 colors from 16.7 million
- 2K × 1K or 2K × 2K read/write area
- 1 megabyte display list RAM
- Supports X/Y devices, keyboards
- Real-time zoom/smooth pan
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- Flexible, expandable instruction set
- Hardware graphics cursor



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*Fast-track graphics for the VMEbus.*



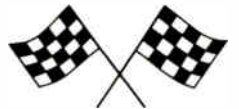
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**B**uild high-resolution graphics with flat-out speed into your process control, simulation, instrumentation or training systems using the Matrox VG-1281 display processor. Designed specifically for high-performance workstations and backed by Matrox's outstanding reputation, it has all the power and flexibility you need for the most demanding applications.

The VG-1281. It takes the checkered flag.



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ELEC-VG / 689

# matrox

THE LEADER IN VIDEO MICROTECHNOLOGY

# ELECTRONICS NEWSLETTER

## X/OPEN ANNOUNCES SOME NEW ARRIVALS IN THE UNITED UNIX FAMILY ...

It looks as if the warriors in the Unix battle are rapidly becoming one big happy family. Rivals Open Software Foundation and Unix International Inc. last month gained membership in the London-based X/Open Co. Ltd., with seats on the board of directors, says Geoffrey Morris, X/Open's president and chief executive officer. Both groups are endorsing X/Open's goal of establishing a common Unix applications environment for open systems. The OSF/1 operating system from OSF of Cambridge, Mass., supports X/Open's Portability Guide, Issue 3 (XPG.3). And early this year, the founders of Unix International in Parsippany, N. J., also pledged support for the X/Open standard. With the two rivals joining 19 leading computer makers on the X/Open board, says Morris, "the X/Open Common Applications Environment becomes the world's industry-standard application platform for the 1990s." □

## ... AS OPEN SOFTWARE FOUNDATION FIRMS UP OSF/1 TIMETABLE

The Open Software Foundation in Cambridge, Mass., has spelled out the timetable for distributing its OSF/1 Unix operating system to members and Unix users at large. First, a vendor kit will be made available in October, allowing members to begin porting the IBM AIX-3-based kernel to their platforms. In March comes an application kit, providing the complete OSF application environment for software vendors. A platform for testing at universities is due next May, allowing field testing at universities and other sites. Finally, the commercial platform, representing general availability of OSF/1 to the industry beyond OSF members, will be ready in July 1990. □

## IBM WILL FINALLY START DELIVERING SAA SOFTWARE THIS FALL

IBM Corp. is almost ready to start delivering software based on Systems Application Architecture, a scheme that the computer giant unveiled with much fanfare more than two years ago to make its software run on all of its computing platforms, from PCs through the midrange AS/400 systems on up to the mainframes. Among the initial offerings announced last month is Big Blue's first major SAA application, an integrated office system called Officevision. The suite of office automation applications will run under all four of IBM's SAA-compliant operating systems: OS/2, OS/400, VM, and MVS. At the Officevision announcement, 14 software companies also unveiled SAA applications. Two of them—the Data Interpretation System from Metaphor Computer Systems Inc. and Easel, a graphics package and user-interface development tool from Interactive Images Inc.—are being licensed by IBM and offered as IBM-supported software. Also announced were an SAA version of the Excel spreadsheet from Microsoft Corp. and a graphical version of 1-2-3 for Officevision from Lotus Development Corp. The first products are slated to start shipping in September. □

## SOI WAFERS PROGRESS IN COMPETITION WITH BULK SILICON

Don't look for commercial semiconductor devices fabricated on silicon-on-insulator wafers soon, but device makers are getting results using SOI wafers from Kopin Corp. that indicate the process could begin to encroach on the market for bulk silicon wafers. Kopin, in Taunton, Mass., has been furnishing 3-, 4-, and 5-in.-diameter SOI wafers to device makers since last fall [*Electronics*, October 1988, p. 56]. Using them, Silicon General Inc. of San Jose, Calif., has fabricated vertical-bipolar discrete devices with breakdown voltages and gains equivalent to circuits made in bulk silicon. And Westinghouse Electric Co.'s Advanced Technology Division in Baltimore has achieved first-pass success in building fully functional 16-Kbit static RAMs. □

# ELECTRONICS NEWSLETTER

## TI MOVES INTO THE ASIA-PACIFIC MEMORY MARKET

**N**ow that Texas Instruments Inc. and Acer Technologies Inc. have agreed to jointly manufacture advanced memory chips in Taiwan, the Dallas semiconductor maker boasts memory capacity in the world's four major markets—the fast-growing Asia-Pacific region, the U. S., Japan, and Europe, where TI is building a memory chip plant in Avezano, Italy. Although TI Japan has been the prime mover in developing TI's CMOS DRAM technology, the company's manufacturing facilities in other Asia-Pacific countries have concentrated on TTL and linear integrated circuits. The Acer deal, announced last month, is the first true joint venture in TI's core semiconductor business since a temporary arrangement with Sony Corp. allowed TI to enter the Japanese market in 1968 in return for TI's granting of IC patent licenses to Japanese semiconductor firms. TI quickly converted that operation into Japan's first foreign-owned semiconductor subsidiary. The 30-some other TI semiconductor subsidiaries have been wholly owned by TI from their inception. □

## HUGHES COMES UP WITH A 'LIGHTNING ROD' FOR SPACE

**H**ow do you counter the buildup of electrical charges on spacecraft? With a lightning rod, of course. But that brings up another question: how do you ground a lightning rod in space? The answer, from GMHE/Hughes Aircraft Co. scientists working at the Research Laboratories in Malibu, Calif., is to use a self-contained on-board generator to emit ions and electrons. They envelop the spacecraft in a neutralizing conductive plasma cloud that grounds the vehicle. Hughes calls the concept Spaceclamp because it effectively holds, or clamps, to near zero the spacecraft surface voltages that have the potential to zap computers and avionic packages. Hughes researchers have just delivered the system to the Air Force Geophysics Laboratory at Hanscom Air Force Base, Mass., after five years of development. □

## FROM COMPAQ, THE MOST POWERFUL DESKTOP MACHINE YET

**C**ompaq Computer Corp. has once again managed to stay ahead of the pack. The Houston-based personal computer maker has done it this time by introducing and delivering to its dealers the world's most powerful desktop computer. The Compaq Deskpro 386/33 is probably the first machine shipping in volume that uses the new 33-MHz 80386 chip that Intel Corp. announced just a couple of months ago. The top-of-the-line Compaq machine comes in three models: the 84, 320, and 650, with the model numbers signifying the number of megabytes of hard-disk storage included. Compaq's engineers have developed a machine that runs at 8 million instructions per second, a 35% performance improvement over the current industry leader, the Compaq Deskpro 386/25. The three models are priced, respectively, at \$10,499, \$14,999, and \$17,999. □

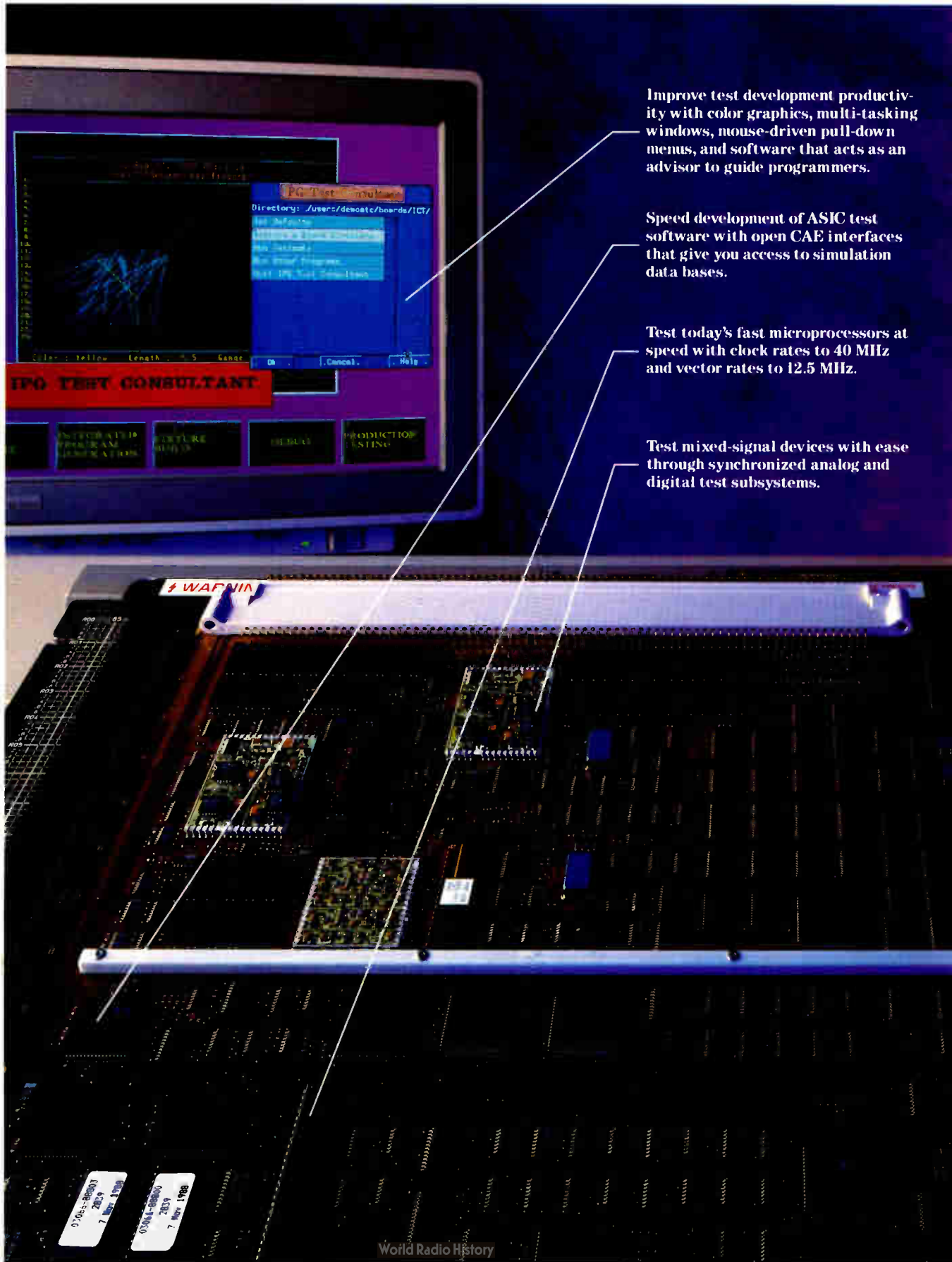
## HEWLETT-PACKARD COMPLETES APOLLO ACQUISITION, NAMES GM

**H**ewlett-Packard Co. is moving quickly to integrate its newly acquired Apollo Computer subsidiary in Chelmsford, Mass., into HP. It has named as general manager David Perozek, a 16-year HP employee who had been general manager of HP's Andover, Mass., division. The acquisition of Apollo was completed late last month, just about one month after the purchase was announced [*Electronics*, May 1988, p. 32]. At the same time Perozek's appointment was made public, HP revealed that the two firms' independent workstation lines built with the Motorola 68030 processor—the HP 9000/300 midrange unit and the Apollo DN3500 and 4500 desktop products—will be merged next year into a family of desktop work stations. □



What could  
you do with  
a board tester  
that's new from  
the pins down?

# Digital, analog, in-circuit and functional



Improve test development productivity with color graphics, multi-tasking windows, mouse-driven pull-down menus, and software that acts as an advisor to guide programmers.

Speed development of ASIC test software with open CAE interfaces that give you access to simulation data bases.

Test today's fast microprocessors at speed with clock rates to 40 MHz and vector rates to 12.5 MHz.

Test mixed-signal devices with ease through synchronized analog and digital test subsystems.

# Testing of complex boards...

Simplify programming and get top performance in complex timing situations with per-pin control of test parameters. Vary drive and receive voltage levels, slew rate, and timing placement of each pin... individually.

Achieve the highest possible performance at the device under test with a patented fixture that uses 1" wire lengths at critical nodes.

Get hundreds of thousands of test vectors without segmenting tests or reloading via HP's Vector Processing Unit architecture. And simplify cluster-test diagnostics with automatically generated backtrace trees.

Expand to 2592 nodes for large boards, and adapt the tester to new technology via a flexible modular architecture.

Here's the advanced tester you've been looking for. With no compromises. That's because the HP 3070 AT-Series is more than a new combinational tester. It's a new generation with new technology, new architecture, and new software. At a price that could change your whole perspective of board testing.

Take pin electronics. Now you can control each pin individually. Drive and receive 12.5 million patterns per second. Get  $\pm 5$ ns typical edge placement accuracy. And 40 MHz clock signals... at the pin. System architecture is new too. A flexible modular design lets you expand to more than 2500 nodes as boards grow. And gives you a practical way to keep pace with changing technology.

Then there's fixturing. The new HP Simplate Express Fixture is an integral part of the system solution. It actually lowers your fixturing costs. And, for the first time, gives you system performance where it counts... at the device under test.

Wrap it up with IPG Test Consultant software that guides and advises programmers in test development and you have several good reasons to take a fresh look at board testing.

So don't wait. Call 1-800-752-0900 today. Ask for Ext. 501D to get our detailed information packet... before you get another board tester.



Come See Us at ATE&I/East, Booth #504.



**HEWLETT  
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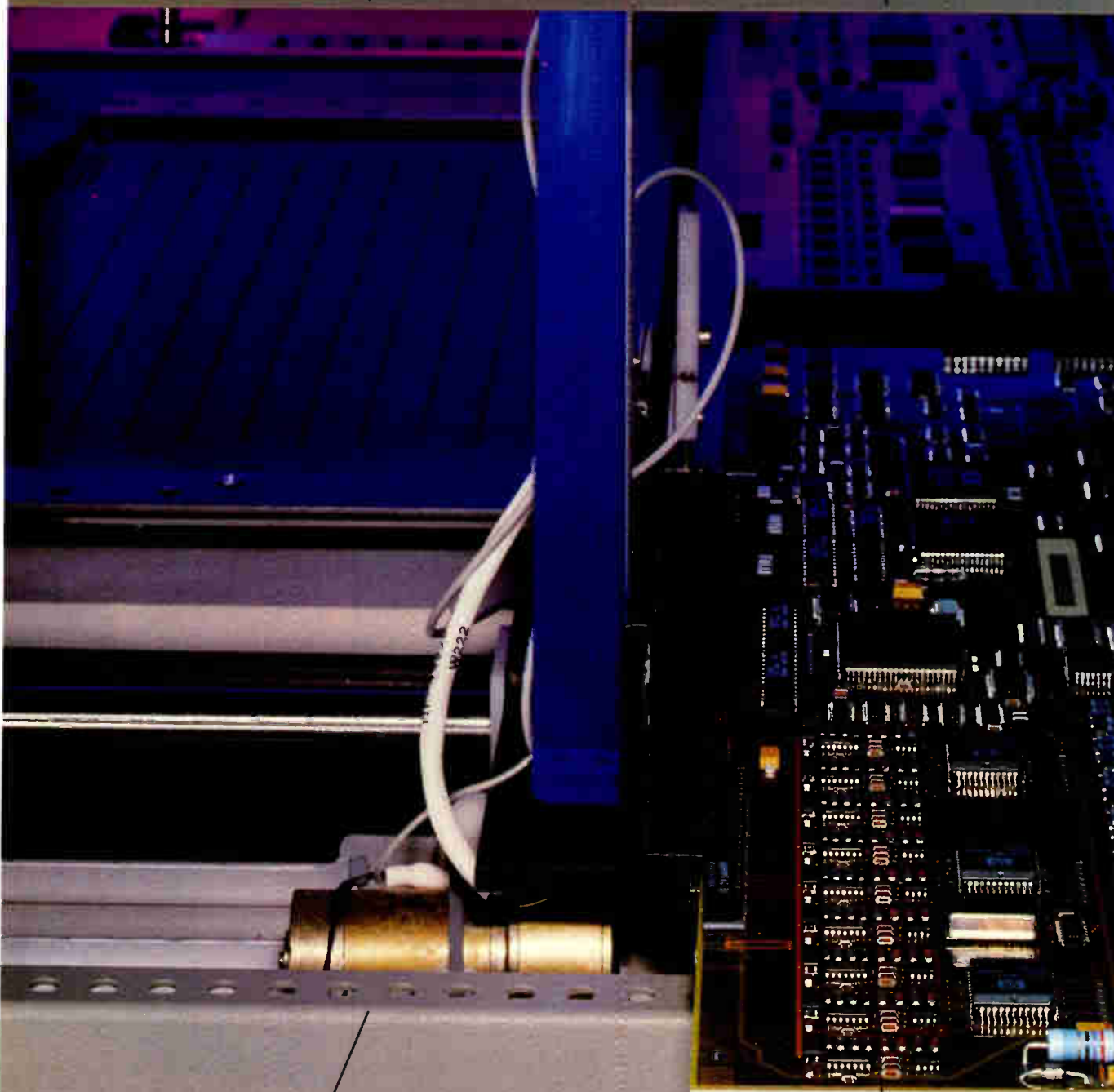
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# ...and finally, solve the

Achieve high throughput in fully automated production lines via an automatic handling system that offers 6-second handling time between boards and automatic adjustment of variable components on boards.

Increase probing accuracy and reliability with a mechanical fixturing system that delivers 10X improvement in probing accuracy and eliminates board distortion during handling and testing.

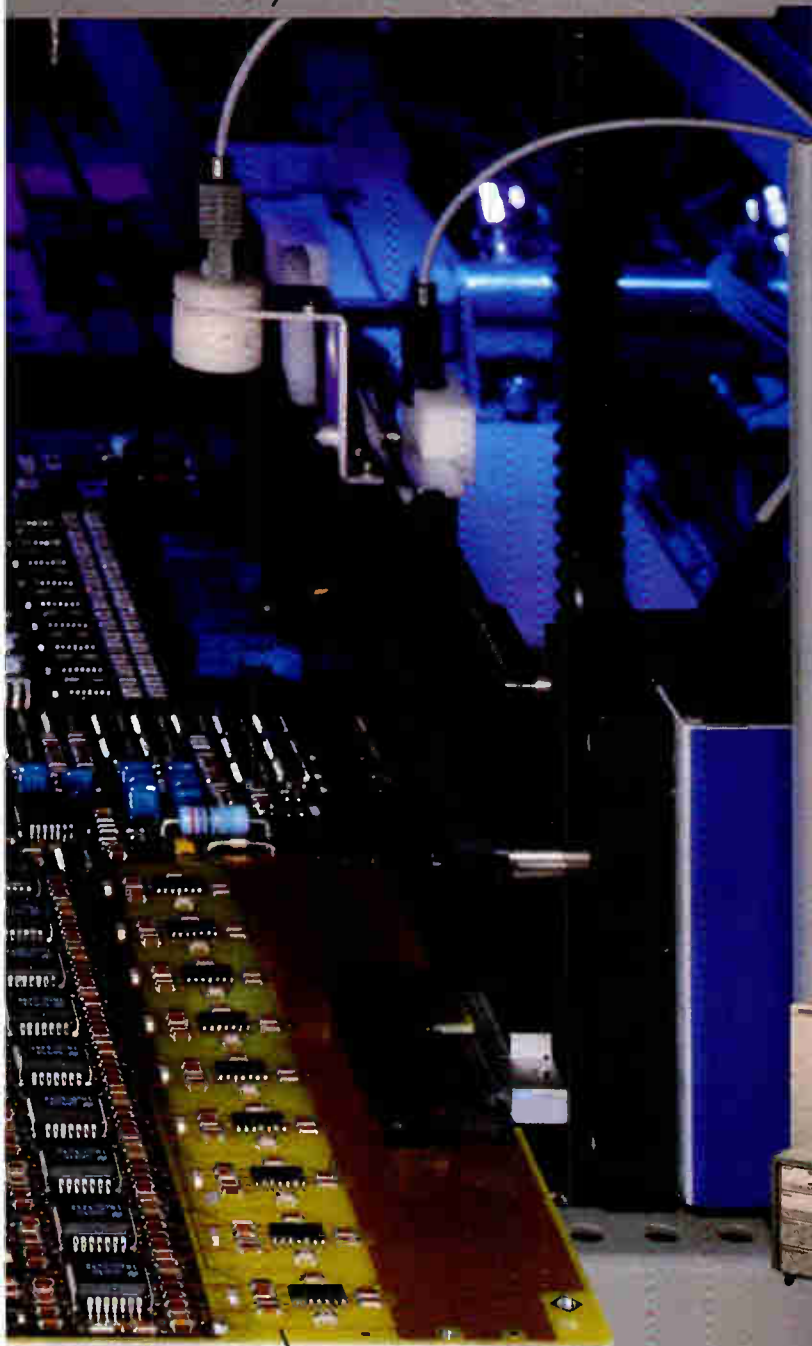


Reduce fixturing costs by as much as 30% with simplified fixture design and software that supports fast fixture construction.

Easily integrate the tester into just-in-time processes with 30-second fixture changes and automatic adjustment to PCB board widths.

# SMT board testing problem.

Achieve system-level performance at the device under test with a totally integrated fixture design that includes dual-stage probing and 1" wire lengths at critical nodes.



Overcome limited-access problems via dual-sided probing that lets you access both sides of loaded boards.

Here's a real board-test breakthrough. The new HP 3070 SMT-Series combinational tester will challenge your belief that SMT boards are hard to test. We've solved the problems. Which gives you the go-ahead on SMT production. Here's how.

First, an innovative mechanical fixturing system handles high-accuracy, dual-level, dual-sided probing. Without flexing boards, which can mask open solder joints or create new process faults. You can even integrate it easily into automated SMT lines.

Then, a new system architecture and pin electronics deliver the tester performance you need for SMT devices such as ASICs. For example, you can control each pin individually. Drive and receive 12.5 million patterns per second. Get  $\pm 5$ ns typical edge placement accuracy. And 40 MHz clock signals... at the pin.

You also get a surface-mount-device library to decrease test development time for nonstandard pin-out devices. Plus IPG Test Consultant software, which acts as an advisor in test development and simplifies quality management.

So if board testing has been a roadblock to SMT integration, investigate the HP 3070 SMT-Series. It's sure to give you a new perspective. Call 1-800-752-0900 today. Ask for Ext. 501E to get our detail packed information package on SMT board testing.



Come See Us at ATE&I/East Booth #504.

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PACKARD**

Circle 25



# Essentials for effective EMI/EMC evaluation and quality product development.

Impulses, ESD, spike, burst, and voltage dips and surges are unwanted signals that can cause momentary malfunction and, in some cases, permanent damage to the electronic products you manufacture.

Our simulators, sensors, power line detectors and components allow you to find, reproduce and contain various types of electrical noise to aid you in designing and building more reliable and trouble-free products that are noise-resistant.

Contact us now for specific details.

## Corresponding to IEC PUB 801-2



### HIGHLY REPRODUCIBLE ESD TESTING

## ELECTROSTATIC DISCHARGE SIMULATOR MODEL ESS-630A

#### Features

The TC-815 discharge gun (optional) enables the system to conduct ESD simulation corresponding to IEC standard publication 801-2 (first edition).

#### Equipment summary

ITEM	Model ESS-630A With TC-815
Output voltage	0.2 – 30kV (0.2 – 10kV, 0.5 – 30kV, Range selectable)
Polarity	Positive and negative
Energy storage capacitor	150pF ±10%
Discharge resistor	150 Ω ±5%
Charging resistor	100M Ω ±10%
Rise time of the discharge current	5ns ±30% at 4kV
Operating mode	SINGLE, COUNT, REPEAT and 20/S (20 discharges per second, activated for approx. 5 sec with each depression of the trigger switch)

**FCC**

**CISPR**

**VDE**

**VCCI**

### NEW DIAGNOSTIC TOOL FOR EMI DETECTION

## EMI NOISE SENSOR MODEL FVC-1000/FVC-30

#### Features

1. The **FVC-1000** can detect and locate sources of radiated emissions in electronic equipment.
2. The **FVC-30** can detect and locate sources of conducted emissions in electronic equipment.
3. For each classified frequency band based on the FCC, VDE, VCCI and CISPR standards, the FVC series measures electric field strength and magnetic field strength individually, which are potential sources of EMI.
4. An electric near field probe and a magnetic near field probe of high sensitivity are furnished as standard accessories.

#### Equipment summary

	FVC-1000	FVC-30
Frequency range	30MHz ~ 88MHz 88MHz ~ 216MHz 216MHz ~ 470MHz 470MHz ~ 1000MHz ※ Simultaneous 4 spectra measurement	100KHz ~ 500KHz 500KHz ~ 3MHz 3MHz ~ 10MHz 10MHz ~ 30MHz ※ Simultaneous 4 spectra measurement
Display	20-point LED bar graph display for each frequency band.	20-point LED bar graph display for each frequency band.



## NOISE LABORATORY CO., LTD.

10-18, 1-CHOME, HIGASHI-IKUTA, TAMA-KU, KAWASAKI CITY, KANAGAWA PREF 214 JAPAN  
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# PRODUCTS TO WATCH

## CIRRUS LOGIC'S CONTROLLER CHIP SPEEDS UP LASER PRINTERS

**L**aser printers can produce a page of complex graphics in as little as 10 s—compared with 60 s using present technologies—by integrating a raster-printer controller chip from Cirrus Logic Inc. Designed to execute page-description languages, the CL-GP 425 combines trapezoid-fill techniques with parallel processing to reduce the time needed to dump images. Graphics containing polygonal shapes are subdivided into trapezoids by the printer's central processor and fed to the raster-printer controller. The CL-GP 425 images each of the trapezoids in parallel. Although aimed at laser printers that operate in the 5-to-14-page-per-minute range, it can be used in printers that handle up to 25 pages/min, says the San Jose, Calif., company. Available now in sample quantities, the CL-GP 425 will be ready for production runs in July. It sells for \$25 each in 10,000-unit orders. □

## INTEL'S OEM DIVISION DELIVERS 33-MHz 386-BASED PLATFORM

**F**ast time to market and architectural flexibility are the hallmarks of Intel OEM Platforms Operation's three latest additions to its product line. Top billing goes to the Intel386 MicroComputer Model 303. Based on a 33-MHz 386DX processor, the 303's tower design accommodates up to eight half-height 5.25-in. peripheral bays for disk or tape drives, 10 expansion slots, and a 300-W power supply. The 302-20 is a standard desktop-size microcomputer powered by the 20-MHz 386DX, while the low-end 300SX offers a small footprint and is driven by the 16-MHz 386SX. All three models are compatible with the Industry Standard Architecture (ISA) bus. They are available now from the Hillsboro, Ore., division of Intel Corp. and are priced in 500-unit quantities from \$1,460 for the 300SX to \$9,905 for a fully configured 303. □

## SYMBOLICS REVS UP ITS MACIVORY SYMBOLIC-PROCESSING COPROCESSOR

**A**pple Macintosh II and IIfx personal computers that serve as symbolic-processing platforms for applications development can run 75% faster with a coprocessor upgrade package from Symbolics Inc. Besides this advantage over its predecessor, the MacIvory Model 2 now offers twice the speed of Texas Instruments Inc.'s MicroExplorer platform, says the Burlington, Mass., company. Symbolic processing makes it simpler to represent and solve unstructured problems by letting programmers use symbols and objects as well as numbers and characters. The Model 2's speed comes mainly from paring the instruction cycle of Symbolics' Ivory microprocessor from 240 to 130 ns. Prices for the Mac II/IIfx upgrade package begin at \$15,900 for the processor board, 8 Mbytes of NuBus memory, and Symbolics' Genera delivery software. Volume deliveries are slated to start in August. □

## UNISTRUCTURE'S TAB SYSTEMS SOLVE ASIC PACKAGING PROBLEMS

**A** family of multilayer tape-automated bonding (TAB) packages from UniStructure Inc. handles pin configurations with up to 804 leads as cheaply and with the same turnaround times as standard formats, claims the Irvine, Calif., company. What's more, UniStructure's liquid dielectric casting process allows the TAB product to be adapted to application-specific integrated-circuit requirements. That's important because of the packaging problems posed as ASICs move to higher and higher pin counts and nonstandard configurations. The tape comes in 35-mm, 48-mm, and 70-mm widths. Standard inner-lead bond pitches of 0.004 to 0.008 in. can be reduced below 0.002 in. Outer-lead bond pitches of 0.010 to 0.020 in. can be shaved to the 0.002-in. range. Depending on size, packages cost \$5,000 to \$8,000 for the two-layer version and \$7,000 to \$10,000 for the ground-plane type. □



# How to get a jump on the competition.

Whether you're racing a product to an early market entry, or maximizing engineering time; Orbit's comprehensive semiconductor manufacturing services can help you cross the finish line first.

## Record Setting Service.

Orbit Semiconductor routinely meets the most demanding delivery schedules and tough manufacturing challenges:

- Guaranteed quick-turn on engineering prototype runs
- Hi-rel volume runs
- Specialized MOS processes such as CCD, Readout, Detector or MUX
- Feature sizes down to 1.5 microns drawn
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Quality equipment. Commitment and teamwork. Extraordinary skill. These are the ingredients that captured a world record for the Orbit sponsored SS/AS Trans Am. And these are the ingredients that we commit to each and every Orbit customer.

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# Electronics

## CRYSTAL BALLS TURN CLOUDY AGAIN AS CHIP FORECASTS DO AN ABOUT-FACE

A flat year turns into a good one, and nobody is sure why

It never has been easy to predict the peaks and valleys of the semiconductor game. Over the years, it has become customary for the market watchers to adjust their forecasts at midyear—and 1989 is no exception.

Going into the year, the majority view was of a mostly flat world compared with the three previous years' heady growth. The *Electronics* consensus forecast was for 9% growth in 1989 [*Electronics*, January 1989, p. 95], while In-Stat Inc., the Scottsdale, Ariz., market consultant, was looking for a niggardly 5% uptick worldwide and a 4% drop for the U.S. At Dataquest Inc. in San Jose, Calif., the numbers indicated a 10.2% rise, and the Semiconductor Industry Association forecast 10% growth worldwide and 12% in the U.S.

But six months into 1989, strong orders have knocked all the bears for a loop. In-Stat is now expecting a 19% worldwide increase, with an even more dramatic jump of 13% for the U.S., though it predicts that 1990 will be a flat year. Dataquest sees a global increase of 15.3% for the year as a whole, but warns of negative growth in the last two quarters. And the SIA is talking about a global 14.4% rise, with 13.8% growth for the U.S.

All this raises the question of whether it is even possible to get an accurate advance handle on a notably slippery business. Forecasts play an important role in how companies plan their operations, so the effects of wide swings are not trivial.

For example, says market consultant Matt Crugnale of Crugnale and Associates in Palo Alto, Calif., with a semiconductor market that last year reached \$45 billion worldwide, "every 1% change is \$450 million, and 10% is \$4.5 billion. That's a big enough difference for anybody."

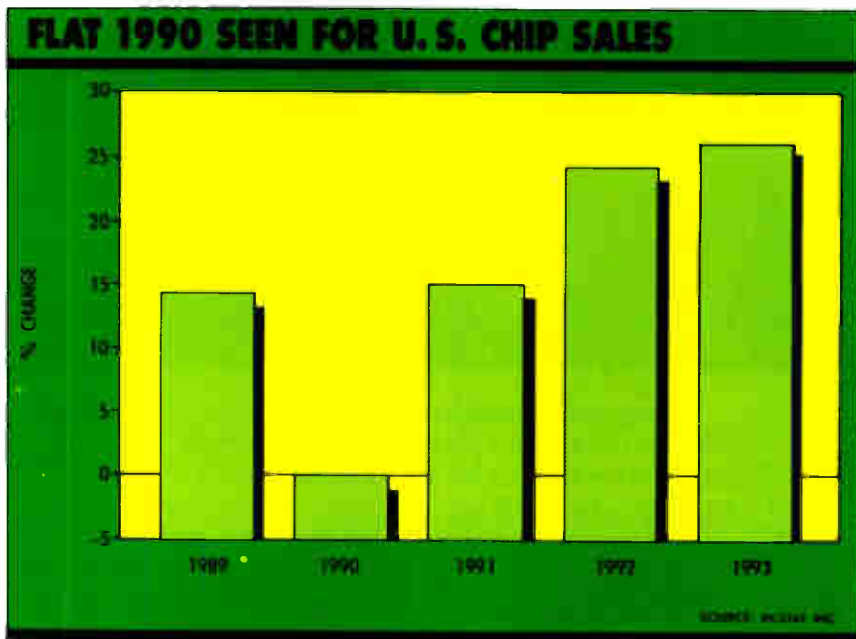
For In-Stat president Jack Beedle, "Forecasting has turned out to be like dancing on a hot tin roof: first you're down and then you're up—but you're always in motion." The veteran chip researcher, who nearly two decades ago devised the key book-to-bill ratio for measuring the strength of the semiconductor market, continually refines his numbers. His opinion is that any prediction set in concrete has little value.

As for the strength of the upsurge in

chip orders, Beedle is no more able than anyone else to pick out a single reason for it. Computer makers account for half of all the chip business, and their sales—except for the red-hot work-station segment—are sluggish. Rather, Beedle believes the "great spurt in the first half" comes from an ordering quirk on the part of these buyers. Over the past few years, he says, computer-industry buyers have ordered most of their components early in the year and sat on their hands for the re-

wide chip results, which came out in late February, showed a far stronger picture than anticipated. Instead of sales that dropped nearly 7% for the quarter, as the SIA's flash, or preliminary, report signaled, they actually dropped only about 1%—a big difference.

For Crugnale, there is another element in the mixed-up market forecasts: the growing availability of dynamic random-access memories. "As memory becomes freer, it breaks the logjam," he says.



mainder. This pattern, which he says "is true in Japan and Europe, too," gives off overly optimistic signals on the upside and overly gloomy ones on the downside.

Beedle points out that the early predictions for a flat 1989 sprang from a marked downswing in orders that started in mid-1988 and took the key SIA book-to-bill ratio into minus territory. Experience has taught that this indicator usually signals the trend for many months ahead.

But this time it went above parity (defined as a dollar's worth shipped for each one ordered) in January and has stayed there ever since. This was the clue that something was amiss, and Beedle notes that the actual 1988 fourth-quarter world-

Crugnale reasons that much new equipment, held up last year by lack of adequate DRAM supplies, is breaking out of the design phase into production, pulling demand for other chips with it. "Anything new is much more memory-intensive than what it replaces," he adds.

Meanwhile, some semiconductor industry executives fear that the happy-days-are-here-again atmosphere that has followed the updated forecasts may be overstating the positive. Among them is Thomas George, senior vice president and assistant general manager of Motorola Inc.'s Semiconductor Products Sector in Austin, Texas. The Motorola forecast calls for a 13% to 14% rise for the U.S. "I



worry about that," George says, noting that second-quarter orders hold the key. Analyst Beedle says that if they equal those of the first three months, he likely will boost his forecasts even higher.

For Japan, In-Stat currently pegs the 1989 increase at 22%, a level deemed too high by Hikotaro Masunaga, vice general manager of Fujitsu Ltd.'s Semiconductor Group. His company expects sales "to slow throughout the year to single-digit growth." Most Japanese companies have

similar forecasts, which some consultants say stem more from political considerations than economic. Faster growth would raise U. S. pressures for market access, they say.

Joining the side of the cautious is Charles M. Clough, head of Wyle Laboratories Inc.'s distribution arm. In his view, neither chip availability nor pricing signals anything like the upswing of the forecasts. His advice: "Don't get fooled by them."  
—Larry Waller

## COMPANIES

# GET READY FOR THE SUPERBATTLE OF CRAY VS. CRAY

### MINNEAPOLIS

The spring of '89 may well go down as a watershed period of restructuring at the top end of the U. S. supercomputer industry. First came the abrupt mid-April decision by Control Data Corp. to deep-six its ETA Systems Inc. supercomputer subsidiary [*Electronics*, May 1989, p. 17]. But just when it looked as though ETA's disappearance would leave the U. S. with only one traditional high-end supercomputer contender, suddenly again there are two.

In mid-May industry leader Cray Research Inc. took the industry by surprise when it announced plans to part ways with its founder, supercomputer design dean Seymour Cray. But the 63-year-old Cray—who left Control Data Corp. 17 years ago to start Cray Research—will not go away empty-handed. He will head a new company, Cray Computer Corp. in Colorado Springs, Colo., and may be well positioned to provide formidable competition for his Minneapolis supercomputer namesake later down the line, a role that ETA never fulfilled.

Cray Research plans to grubstake Cray's new company with up to \$150 million in assets and cash. Cray Computer's mission: to complete the development of Cray's latest brainchild—the revolutionary and risky gallium arsenide-based Cray-3. In turn, the Minneapolis parent will own 10% of Cray Computer. The remaining 90% will be distributed to Cray Research shareholders.

Momentum for the change has been building for 18 months, ever since Cray Research moved the Cray-3 program to Colorado Springs. As one of two parallel development efforts within Cray Research, the Cray-3 has been competing internally with the company's C-90 project in Chippewa Falls, Wis. The C-90 is to be a silicon-based successor to the company's X-MP and Y-MP line. It is due out in 1991 and will play in the same performance league as the Cray-3—10 to 20 billion floating-point operations/s.

"We've both had all the resources we needed up until now," Seymour Cray says of the dual internal-development tracks. But with the unorthodox deal to spin off the Cray-3 project, "we were anticipating a problem in the future and trying to avoid it."

Cray Research chairman John Rollwagen told shareholders at the company's annual meeting in May that the spinoff was prompted by a number of factors, in-



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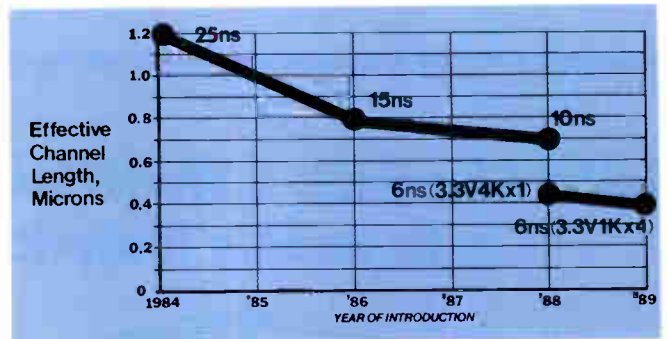
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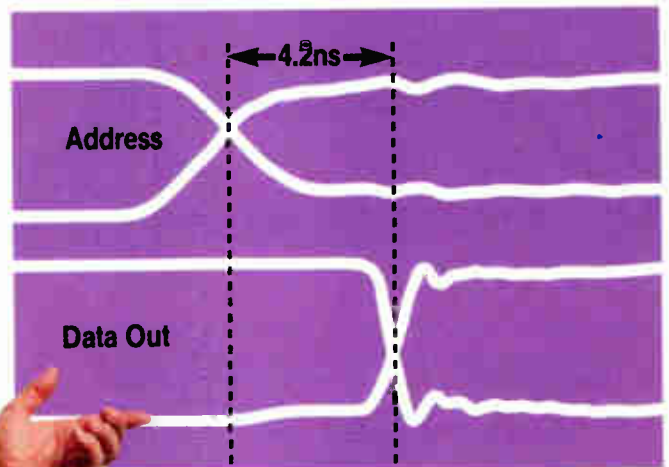
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cluding slowing industry growth and increasing pressures on Cray's bottom line, as well as faster than anticipated progress on the C-90.

Cray's research and development expenses rose by 35% last year to about \$117 million, including \$30 million for the Cray-3, which may see first deliveries next year. And the company reported an operating loss in this year's first quarter for the first time in recent memory. Meanwhile, "we don't see more than 10%

growth" during 1989, Rollwagen says, adding that he expects "a tough, tough pull" to meet 1989 financial goals.

Something had to give. And the unique scheme to split off the Cray-3 effort will solve the problem, while producing no losers, Rollwagen contends.

Cray-3 customers at first will be the same ones that were interested in fledgling Cray Research in the mid-1970s, namely, a few big government laboratories and other sophisticated supercom-

puter users, he says. "And that's what they [Cray Computer] need right now. It's a very significant part of their development process, so they don't have to be distracted by building machines in great volume, or by calling on all the different kinds of customers that need to be called on," he says. "They can leave that to us."

Cray Research, with sales of \$756 million last year, will now be free to focus its resources on the more conservative silicon-based MPs and C-90, and on expanding its base in software, networking, and marketing infrastructure. Customers will benefit by having a choice between the two technologies, Rollwagen says. "The net effect of both enterprises, I truly believe, is that the competition will create a bigger pie for everybody."

However, others have their doubts. "The two companies clearly will be going after some of the same customers, and there will be pressures on the federal budget. So it's difficult to see how this will result in a larger pie," says Barry Willman, a computer analyst at Sanford C. Bernstein & Co. in New York.

In agreement is Gary Smaby, Minneapolis technology analyst for Needham & Co. "I think I understand why they did it, but I'm still not convinced that it will be a net plus for the old Cray, because I think they have created a potentially formidable competitor for themselves," he says. There are still many unanswered questions, Smaby notes. But if Cray Computer can manufacture the Cray-3 in volume, "it's going to put a lot of pressure on Cray Research."

Reactions to the Cray move around the user community are mixed. With Minneapolis-based ETA getting out of the business, "I can see where these two pieces of Cray, which were competing anyway, will now compete a lot more. And I think that's very good for the country," says Dieter Fuss, deputy associate director for computations at the Lawrence Livermore Laboratory in Livermore, Calif.

But at the Pittsburgh Supercomputing Center, which has placed the only announced order for a Cray-3, scientific codirector Ralph Roskies takes a slightly differing view. "The Cray-3 is going to be a real machine," says Roskies, who is expecting a late 1991 delivery. "But now that Cray is two smaller companies, that doesn't reassure me that they can withstand the pressures that the vertically integrated Japanese [supercomputer vendors] can bring to bear" (see p. 48).

And some think that the repositioning is not over. As the industry leader, Cray Research faces a growing challenge not only from a trio of Japanese high-end vendors in NEC, Fujitsu, and Hitachi. The firm will also likely meet new competition from IBM Corp. and a number of smaller minisupercomputer vendors, industry watchers point out. *-Wesley R. Iversen*

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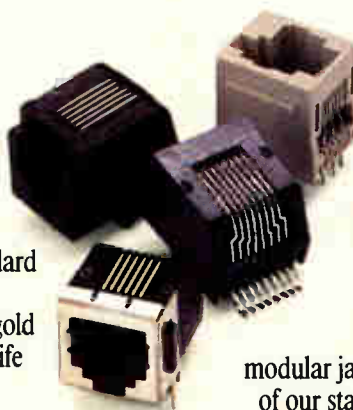


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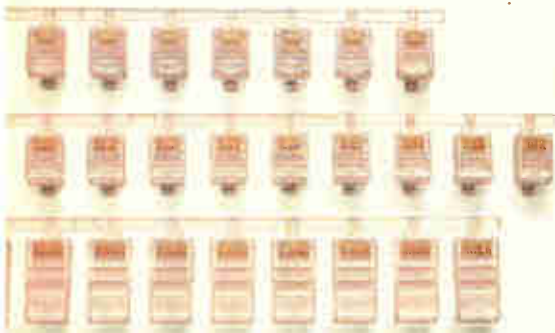
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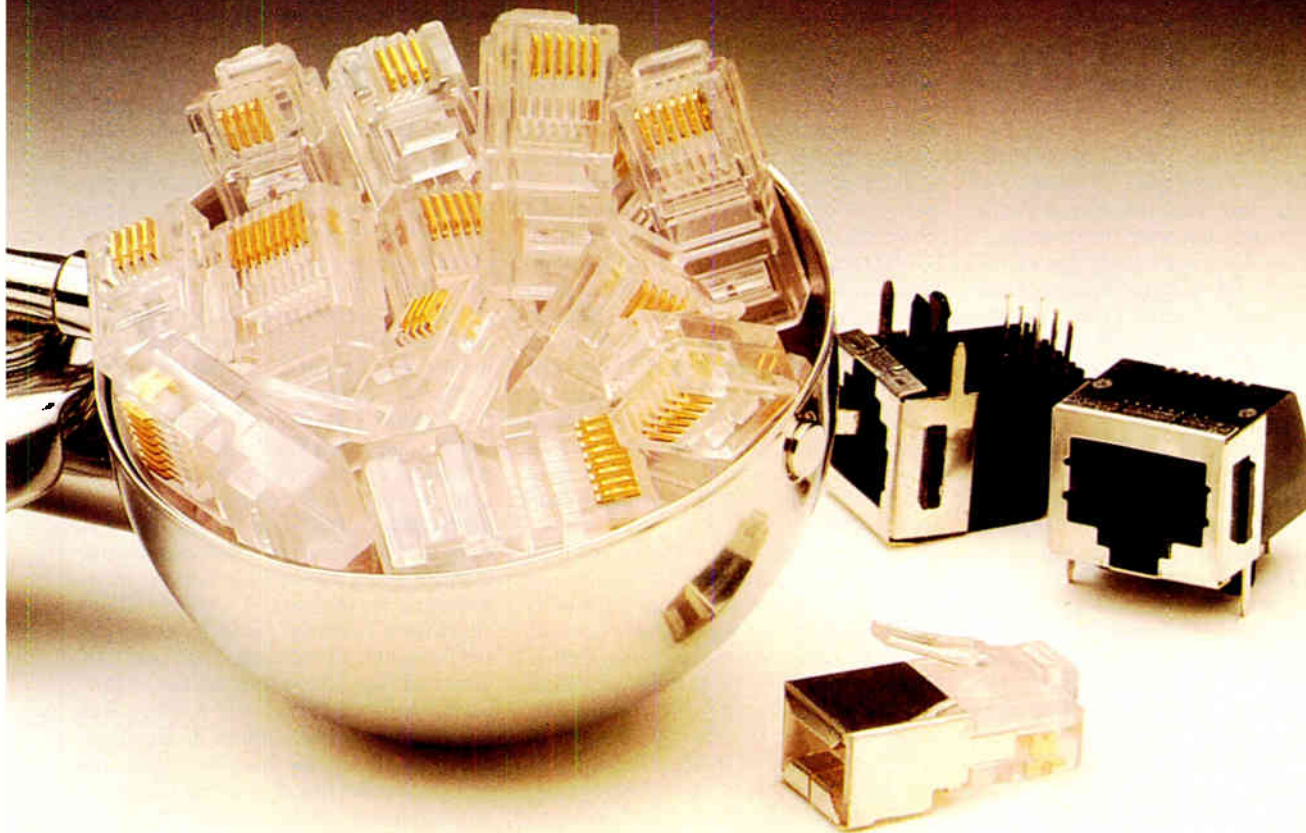
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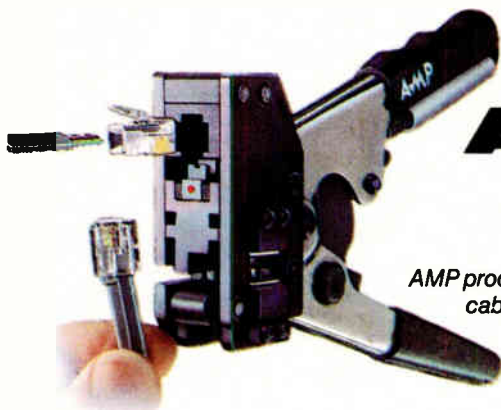


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# ROUTE 128 REASSESSES ITS STRATEGIES

## LOWELL, MASS.

In the 1960s and 1970s, the words "Route 128" conjured up images of high-flying minicomputer companies in the Boston area that were the darlings of Wall Street, logging yearly growth of 40% or more. Times have changed. Companies like Data General, Prime Computer, and Wang Laboratories are struggling for profits while fighting off takeovers and counting on new market strategies to make money.

Data General Corp. of Westboro has gone three straight years without turning a profit, and there's no guarantee the company will be profitable this year. Prime Computer Inc., based in Natick, reported a \$6.3 million loss in its first 1989 quarter, which ended April 3; the company laid off 1,200 employees last December. Lowell-based Wang Laboratories Inc. was in the red in its most recent quarter as well, losing \$63 million after rebounding nicely last year from 1987 losses. If Wang sticks to its goal of paring its employee head count to 28,500 by September, it will have to lay off some 1,700 workers by then.

The region itself isn't stagnant, say executives at these and other Boston-area computer firms. But some minicomputer makers waited too long to go after fast-growing markets, including desktop work stations, computer-aided design and engineering, and on-line transaction processing. Also inhibiting growth is the time it's taking to augment proprietary hardware and software architectures with the open-system standards computer buyers demand today, especially the Unix operating system.

Still, not all Boston-area computer companies are singing the blues or glancing nervously over their shoulders at would-be acquirers. Some are doing quite well, mining rich veins in market segments that are growing much faster than the mature minicomputer business. And some are going the merger route.

Prime has offered itself for sale after fighting for months against a hostile acquisition by MAI/Basic Four Inc. of Tustin, Calif. Prime deems the MAI bid of \$20 per share too low. Analysts say Wang is a takeover target, with Xerox Corp. of Stamford, Conn., the latest rumored suitor.

Consolidations of

computer companies aren't that infrequent along Route 128. The most recent and dramatic was Hewlett-Packard Co.'s purchase of Apollo Computer Inc., the Chelmsford work-station pioneer, in April [*Electronics*, May 1989, p. 32]. Apollo was working its way back to minimal profits from earlier losses. Prime acquired Computervision Corp. of Bedford, Mass., in a hostile takeover of its own last year. That move was intended to broaden Prime's base in CAD/CAE, a vertical market it had targeted. MAI is still trying to acquire Prime, which in April decided to seek other bidders [*Electronics*, May 1989, p. 18].

In two deals with unusual twists, smaller Boston-area computer companies bought larger ones to achieve greater critical mass in revenues—and to broaden customer bases—to compete more effectively in vertical markets they had staked out. Masscomp Inc. of Westford was only about one third the size of Concurrent Computer Corp. of Tinton Falls, N. J., which it bought last fall [*Electronics*, April 1989, p. 119]. The merged company kept the Concurrent name and its headquarters. Both companies specialize in real-time technical computing applications, still the target of the merged firm.

In a similar purchase completed last

Some minicomputer makers waited too long to go after fast-growing markets

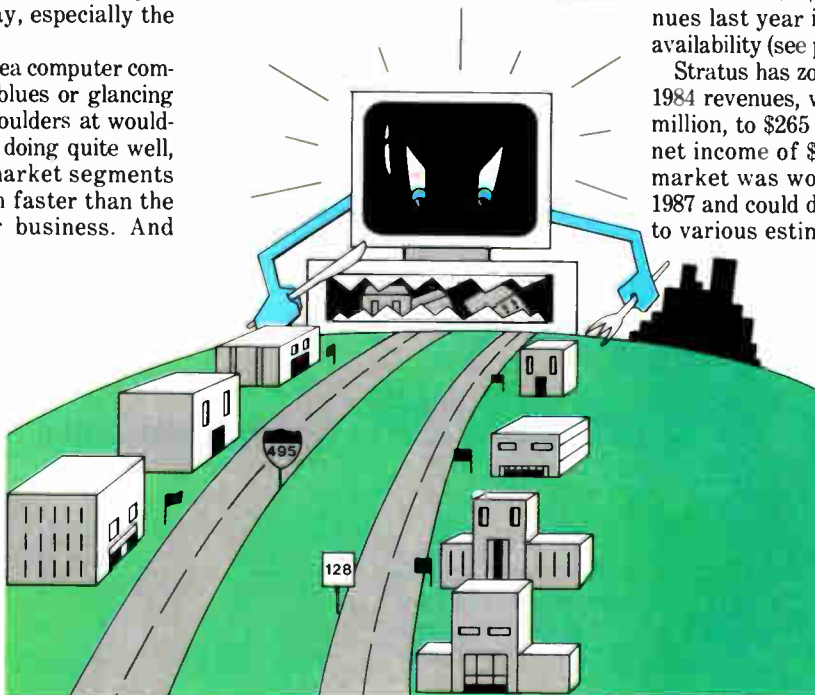
month, Encore Computer Systems Corp., formerly based in Marlboro, acquired Gould/Computer Systems Inc. from Nippon Mining Co. Ltd. [*Electronics*, April 1989, p. 18]. Encore, an early advocate of parallel-processing systems, had 1988 revenues of \$34 million; Gould Computer's 1988 revenues were \$225 million. Encore has moved its base to Gould's computer operations in Fort Lauderdale, Fla. With the purchase, helped along by a \$140 million loan from Gould to Encore, the merged organization has enhanced its presence in technical computing, especially in the simulation market.

**COUNTERPOINTS.** Digital Equipment Corp., the Maynard-based minicomputer giant, is going strong despite some hand-wringing on the part of analysts about short-term financial performance. Stratus Computer Inc. and the East Coast Division of Sun Microsystems Inc. report torrid growth rates, and Encore was growing nicely even before its Gould acquisition. Realizing they couldn't compete across the board with the Route 128 minicomputer establishment, these relative newcomers targeted markets with explosive growth potential.

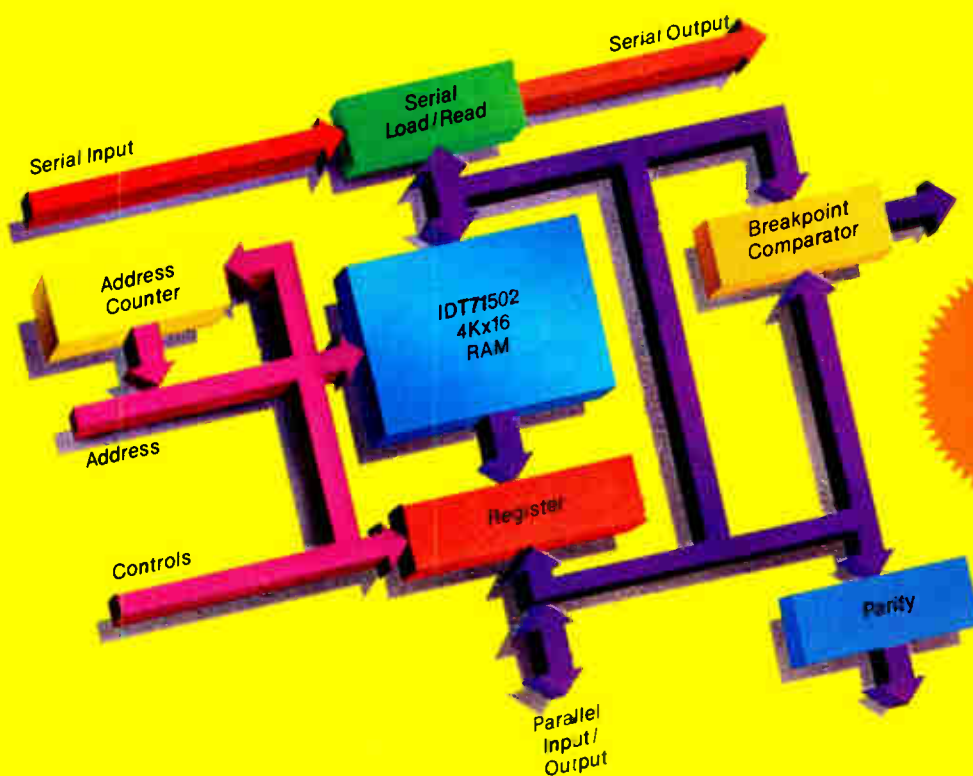
The XA2000 line of fault-tolerant computers from Marlboro-based Stratus is finding widespread use in on-line transaction processing (OLTP) applications in banks, Wall Street securities firms, and manufacturing. Sun's East Coast Division, with headquarters in Billerica, is riding the crest of the work-station wave. The division's first product, the Sun 386i, accounted for \$150 million in Sun revenues last year in its first 12 months of availability (see p. 127).

Stratus has zoomed from \$42 million in 1984 revenues, with a net income of \$5.4 million, to \$265 million last year, with a net income of \$29.3 million. The OLTP market was worth about \$20 billion in 1987 and could double by 1991, according to various estimates. "It's been a good market for us and for Tandem as well," says William E. Foster, founder, president, and chief executive officer at Stratus.

Tandem Computers Inc. of Cupertino, Calif., pioneered the market "and pulled us into it," Foster says. "We were focused on that market even before the term 'on-line transaction processing' was coined." Stratus is now sharpening its fo-



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cus even more. Initially, it supplied hardware to the overall OLTP market. In the past few years, Foster says, it has been looking especially at financial services—securities exchanges and banks—telecommunications, and retail point-of-sale applications, such as airline reservations.

William Avery, vice president and general manager of Sun's East Coast Division, says the shift to open systems has occurred more rapidly than anyone expected. "It has affected some key companies in this area more than in other regions," he says. "We were asking in 1986 if Unix would really make it." The Sun 386i, for which his division has complete responsibility, runs both Unix and MS-DOS. It accounted for more than 10% of Sun's corporate revenues last year.

DEC, which spawned the minicomputer business in the early 1960s, hasn't become stagnant despite a mature market. The company cashed in on a networking strategy adopted some years ago to provide customers with enterprise-wide computer resources—

from the desktop to the data center. That strategy is still paying off. Also, DEC is now an aggressive competitor in the work-station market and has embraced Unix in a big way. The company recently introduced a series of Unix-based reduced-instruction-set work stations, the DECstation 3100 line [*Electronics*, February 1989, p. 49].

In 1988 DEC's revenues reached nearly \$11.5 billion, up from almost \$9.4 billion in 1987. Net income was up, too, from \$1.1 billion to \$1.3 billion. Yet DEC's stock dropped more than 10 points on March 22 after the company said that revenues for the third quarter of 1989 would be lower than the expected 13% increase over 1988's third quarter.

The quarter came in at an 11% increase, to \$3.1 billion. Mark Steinkrauss, director of investor relations at DEC, attributes the 2% differential to a slowing in the U. S. economy. Steinkrauss says the company will try to boost the tempo by continuing to hammer away at the networked enterprise-wide computing theme along with further embracing industry standards, such as Unix and the International Standards Organization's Open System Interconnect model.

DEC's Unix variation, Ultrix, has yet to contribute substantially to the company's revenues. But in discussing the recent quarterly results, president Kenneth Olsen said DEC has embraced Unix "with as much enthusiasm as we have traditionally exhibited for our VAX/VMS systems."

Data General is also a late convert to Unix. The company announced a Unix push in April 1988 as part of a three-pronged growth strategy. The first part

of the strategy is to continue to develop the proprietary cash cow—the MV/Eclipse computer family. The second is a push in open-system industry standards, and the third is a strong focus on the telecommunications market.

Part one is paying off: the MV/40000, introduced last October, has sold better than expected. That system was the main reason for Data General's profitable second quarter, which many analysts expected to show a loss. But it's too early to tell if the other two elements will contribute enough in new revenues to get the company into the black again and growing faster than in recent years. Data General's revenues have increased from \$1.16 billion in 1984 to just \$1.36 billion in 1988.

The company's first foray into open systems was the introduction in late February of the initial entries in a Motorola

88000 RISC work-station and server family called Aviion, which runs under the company's proprietary DG/UX Unix variation [*Electronics*, March 1989, p. 44]. However,

"we won't see a major revenue spurt from the Aviion family this year," says Ronald Skates, executive vice president and chief operating officer.

The most visible manifestation of the company's telecommunications strategy is a contract with Japan's NTT Corp. to supply hardware and software for the private data networks that NTT provides [*Electronics*, November 1988, p. 192]. Data General is delivering equipment to NTT under the terms of that contract, which could be worth several hundred million dollars to the company and could trigger similar sales to other telecommunications firms.

One analyst suggests that Data General, among others, may be preparing to settle for minimal revenue growth as a tacit strategy. Charles Casale, president of the Aberdeen Group, a Boston-based market research firm, says that companies such as Data General, Prime, and Wang "must make up their minds to go out of business—by bankruptcy or acquisition—or remain at growth rates right around [the rate of] the Gross National Product. Data General appears to be settling for this."

Skates is quick to deny any such unspoken strategy. "We won't be satisfied with GNP-like growth," he asserts. "[Company president] Ed de Castro wouldn't buy that for a second. With the new open-system products we have now and more to come, we expect to grow a whole lot better than that when those products take hold." Nor is Data General looking to be acquired, Skates adds. "No one has approached us."

Casale concedes that Data General

### Many Boston-area firms are looking at mergers or fending off takeovers

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"has always shown technical strength, tenacity, stubbornness, and a will to survive." Those things can't be said about Wang, he says. But in Casale's view, Wang has an ability to successfully enter new businesses. "Wang started in calculators, switched to small business computers, and then to dedicated word processing," where "it stayed beyond the time it was prudent."

Now Casale questions whether Wang can make the transition soon enough into

the four vertical markets it is targeting: manufacturing, financial services, government, and professional services, such as law offices. Paul Henning, director of investor relations, stresses that the technology helping Wang compete more effectively is the imaging capability embodied in Wang's Integrated Imaging Systems, which tie images and text together in a desktop work station [*Electronics*, April 30, 1987, p. 83].

Wang's 1987 revenues of \$2.83 billion

grew to \$3.06 billion last year, and net earnings rebounded dramatically from a loss of \$70.7 million in 1987 to a \$92.7 million profit last year. "We can't be an all-purpose computer company to all markets, so we're focusing on those four vertical markets," Henning says. He says Wang's goal is to boost revenues 20% a year in each of the sectors.

Henning points out that Wang is already in the professional services market with word processing and office automation, "and we're strong in state and local government and financial services. But the potential for penetrating all of those is much greater with imaging," he says.

Wang's revenues from imaging products have grown rapidly in a short time. Imaging products contributed \$30 million to Wang's revenues in all of fiscal 1988. In the first six months of this fiscal year, they accounted for another \$30 million, and then \$30 million more in just the last three months, according to Henning. "If we can keep doubling like that, imaging will be a substantial business for us in a few years," he says.

Henning suggests that the fourth quarter, which ends June 30, will bring Wang back to the break-even point. With downsizing, Henning maintains that the company will move into fiscal 1990 with a leaner expense line and still be profitable at a lower domestic sales level. He wouldn't comment on acquisition rumors.

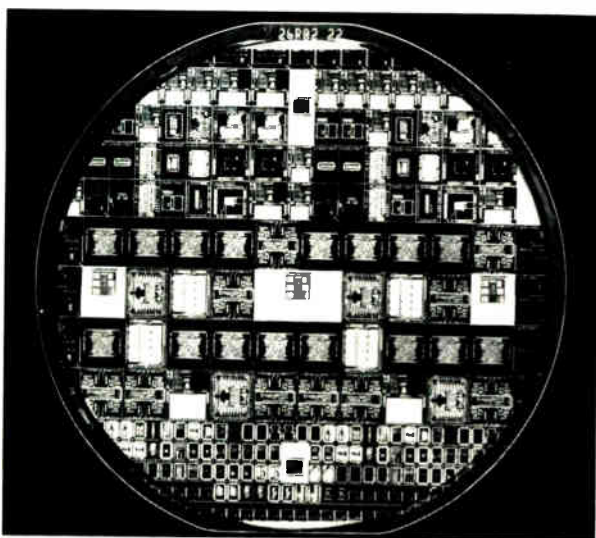
**PREOCCUPIED.** Meanwhile, acquisitions have become a preoccupation at Prime. The company's unfriendly takeover last year of Computervision was a growth move that hiked Prime's revenues from \$960 million in 1987 to almost \$1.6 billion a year later. But profits suffered as a result: net income dropped from \$64.7 million in 1987 to about \$19 million last year. Then came the \$6.3 million loss the first quarter of this year.

Now Prime is locked in combat with MAI/Basic Four, spending substantial money and energy to hold off MAI's hostile takeover bid. MAI claims that through early last month, Prime shareholders had tendered more than 50% of Prime's stock to MAI. Even if MAI fails, however, Prime has offered itself for sale in management's attempt to get a better price for the company than the \$970 million MAI is offering—or \$20 per share. Many customers have postponed purchases from Prime until the company's status is settled.

For his part, Casale of the Aberdeen Group says that Prime's growth strategy, based on CAD/CAE, will make for only modest growth even if the company is not sold. "I don't know how I would bet" on the MAI deal, he says. "No one on either side is backing down. These are two sets of greedy capitalists who may inadvertently destroy the company they're trying to salvage."

—Lawrence Curran

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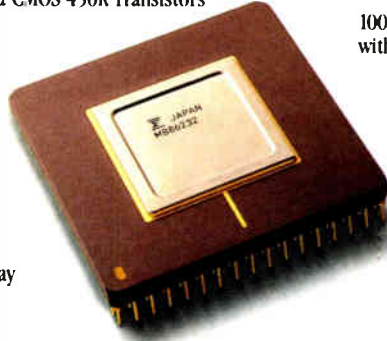
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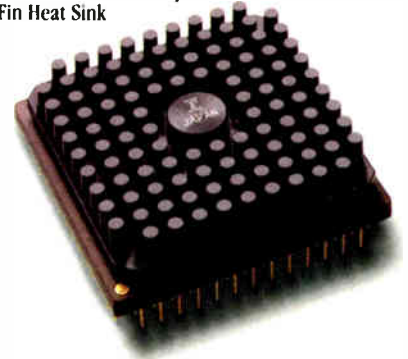
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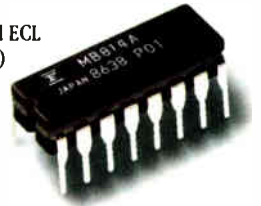


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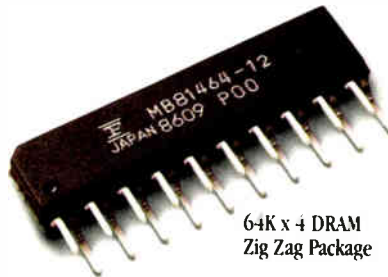


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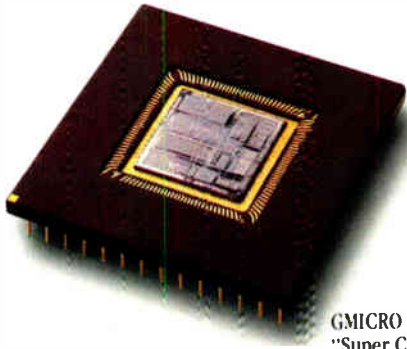
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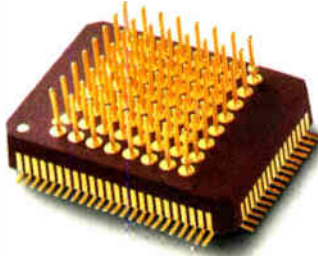
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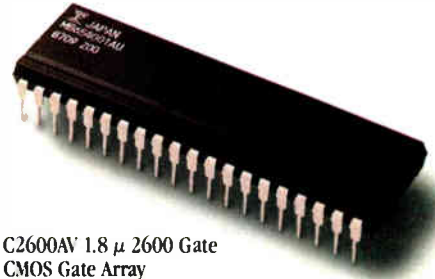
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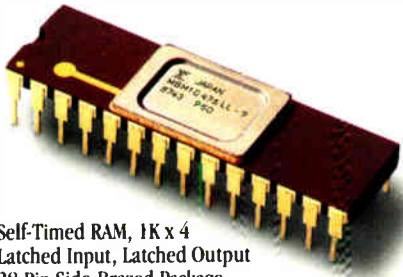
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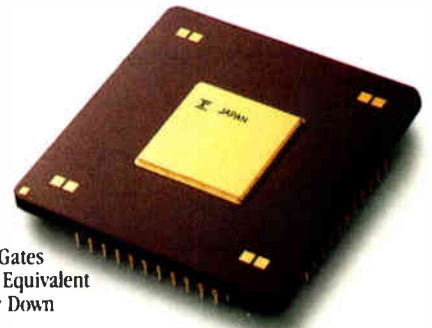
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# WANTED BY THE AEA: \$1.35 BILLION FOR HDTV

## WASHINGTON

Now there is a plan. After nearly a year of hand-wringing and ominous predictions about the fate of the U. S. electronics industry, the American Electronics Association last month produced detailed recommendations for how the U. S. could use high-definition TV as a means of reestablishing a domestic consumer electronics industry.

The plan calls for direct federal aid, low-interest loans, and loan guarantees worth a combined \$1.35 billion over the next decade, to be matched at least dollar for dollar by industry. Without such a strategy, the AEA warns, the U. S. risks losing its telecommunications and computer industries, and faces further erosion of the vital semiconductor industry—not unlike what has already happened in consumer electronics [*Electronics*, March 1989, p. 70].

"HDTV is not only a symbol, but a driver of competitiveness," says Jack Kueller, vice chairman of IBM Corp. "An intersection of TV and computers is coming. HDTV will surely be one of the drivers of semiconductor technology."

So now comes the tough part: selling

Congress and the Bush Administration on the idea. It's not that Washington isn't sympathetic to the issue—indeed, HDTV has been called a "top priority" of the Bush Administration's economic and industrial strategy. But it won't be easy to come up with more than \$1 billion when Congress is struggling with a burgeoning federal budget deficit.

Secretary of Commerce Robert A. Mosbacher has made clear his willingness to help industry by loosening antitrust restrictions, reinstating the capital-gains tax differential, and making permanent the research and development tax credit. But Mosbacher, who will deliver his own HDTV report to Congress this summer, has so far held fast in refusing to provide federal aid. "They're hoping that Uncle Sugar will fund it," he says, "and I don't think they should depend on that."

Congress may be easier to sway. Sen. Ernest F. Hollings (D., S. C.), the powerful chairman of the Senate Commerce, Science, and Transportation Committee, told Mosbacher at a committee hearing last month that "it's high time we stop wasting time with committees and meetings and come up with solutions." He

commended the AEA report, saying that the \$1.35 billion request is "in the ballpark." Combined with Mosbacher's plan, he said, the AEA proposal will play a key role in formulating congressional consensus on the issue.

Hollings maintains that HDTV is something of a motherhood-and-apple-pie issue—that few in Congress would vote against a program designed to reverse the decline of a key U. S. industry. But no matter how much the Congress may want to support a major HDTV initiative, Hollings admits, "finding the money is tough, because you've got to take it out from somewhere else."

**BACKERS.** Hollings is not alone in supporting federal investment in HDTV technology. Senators Albert Gore Jr. (D., Tenn.) and John Danforth (R., Mo.) have also indicated their support, as has Rep. Don Ritter (R., Pa.). Ritter introduced legislation in March that would authorize \$100 million a year for HDTV research over the next five years. The bill would also relax applicable antitrust laws to allow major U. S. companies, such as AT&T, IBM, and Motorola, to join in an HDTV consortium, and reinstate the R&D tax credit. Says Sen. John D. Rockefeller IV (D., W. Va.): "It's coming to the point where government-industry cooperation is not only important, it's lifesaving."

That's precisely the point of the HDTV business plan, which was prepared for the AEA by The Boston Consulting Group after interviewing experts at more than 70 companies and government agencies and visiting plants in Japan, Belgium, the U. S., and West Germany.

The proposal begins with the creation of an independent Advanced TV Corp., chartered by Congress to lead and monitor development of the industry and to administer loans and loan guarantees provided by Congress for specific development projects.

In addition, the plan calls for the Pentagon's Defense Advanced Research Projects Agency to spend \$300 million on high-definition display and component research over the next three years. Darpa seized on the HDTV initiative last winter by promising to spend at least \$30 million for display research in 1989, but has not announced formal plans for continued research programs in the future.

Rounding out the AEA plan's funding picture would be a minimum of \$50 million to be spent over three years by the National Institute of Standards and Technology for developing the applicable HDTV standards.

The key to the AEA's proposal is the way in which the technology would be

## HOW AEA WOULD BUILD HDTV INDUSTRY

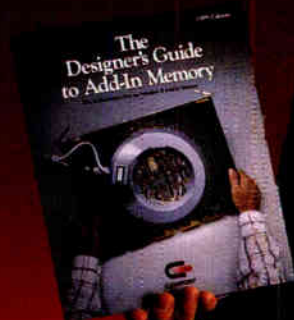
Action	Cost	Effect
Grants	\$300 million over three years	Develop basic technologies, including advanced displays and image-processing chips vital to establishing an advanced TV infrastructure
Loans	\$500 million over 5-10 years	Discount loans would be used to offset the high cost of capital in the U. S., stimulating investment in manufacturing and product-development strategies
Loan guarantees	\$500 million over 5-10 years	Encourage U. S. financial institutions to invest in HDTV ventures
Establish ATV Corp.	NA	Create an independent, government-industry body to coordinate the HDTV effort, manage the funds, and oversee standards, licensing programs, and import activities in order to protect U. S. interests
Relax antitrust rules	None	Allow major corporations, such as AT&T and Zenith, to collaborate on HDTV development without risk of government intervention
Restore the R&D tax credit and the long-term capital gains differential	NA	Encourage long-term plans and investment



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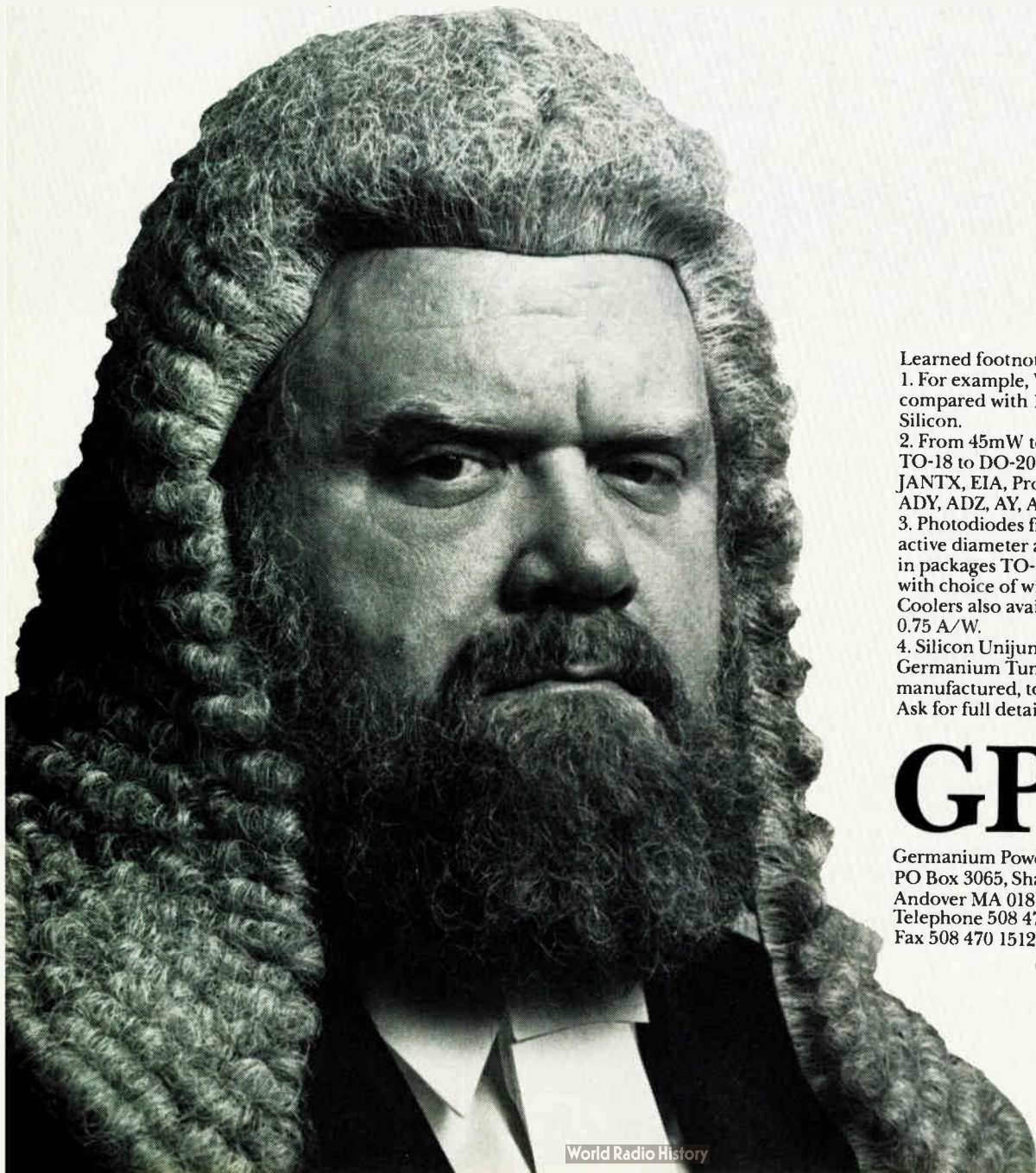
"In Amplification, from small signal to output power, Germanium devices, provide stable performance, security of supply, and specifications to meet the world's leading technical standards.

"In Photodetection, Germanium gives linearity of spectral response, peaking at 1550nm, and offers high-shunt resistance, when required.

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1. For example,  $V_f$  as little as 0.35V, compared with 1.0V or more for Silicon.
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controlled. Noting that all this investment would not solve any problems if the technology can be pirated or shipped offshore, AEA vice president Pat Hubbard says it is essential that Congress and the U. S. Patent Office develop a means to provide the proposed ATV Corp. with exclusive licenses to underlying HDTV standards and technology. The company or organization that developed the standard would receive full compensation, she says, but would have to relinquish rights to the technology so that it could be fully controlled by ATV.

**U. S. TILT.** To obtain loans or other financial assistance from ATV, companies would have to meet certain key requirements, including matching government-backed funding with their own financing; performing most or all related R&D, engineering, and manufacturing in the U. S.; and purchasing the majority of its semi-

conductors from U. S. chip makers.

Similarly, says Hubbard, who has headed the AEA's HDTV initiative, licensing-fee schedules, royalty-funded investments, direct R&D grants, and other economic incentives, including tax benefits, should be prorated according to the level of R&D, manufacturing, and product design done in the U. S. The level of use of domestically produced semiconductors and the extent that U. S. firms have market access to a given company's home country should also be factored into the equation, she says.

Hubbard bristles at the suggestion that these rules are "protectionist," but she makes their purpose very clear: government funding must not be funneled offshore by foreign-owned or controlled companies that do not invest in engineering jobs and full-scale manufacturing in the U. S. *-Tobias Naegele*

## ECL

# AT&T AIMS ITS BEST SHOT AT THE MERCHANT MARKET

### BERKELEY HEIGHTS, N. J.

In its latest strategic move toward becoming a major player in merchant chip markets, AT&T Microelectronics has turned up the speed and turned down the power of emitter-coupled logic. Its new ECL process, called BEST-I, is flexible enough to deliver switching speeds as fast as 80 ps or power consumption as low as 0.5 mW.

BEST—for bipolar enhanced self-aligned technology—boasts state-of-the-art performance and will be available in July as a standard-cell library for application-specific integrated circuits. BEST-I gate arrays will follow later in the year, and a standard-parts family hasn't been ruled out, says Mike Scott, digital bipolar product marketing manager.

The five-year game plan at the Berkeley Heights chip maker calls for boosting merchant chip sales at a much faster rate than the division's sales to AT&T Co.'s systems companies. The goal: crank up the merchant business to 50% of total sales by 1992, says marketing vice president Dick Koeltl [*Electronics*, May 1989, p. 125]. External sales currently account for 25% of AT&T Microelectronics' \$1 billion total annual revenue.

One tactic calls for leveraging advanced technologies developed for captive semiconductor production by AT&T systems companies. ECL is a prime example. Breaking a long-standing policy of keeping its ECL secrets in-house, AT&T two years ago decided to offer digital bipolar devices and technologies to the merchant market. With BEST-I, external customers will be getting an early shot at

AT&T's leading-edge technology—at a good price. "Our intent is to be equal to or better than other ECL technologies on price," Scott says, though he would not divulge a cost-per-gate figure.

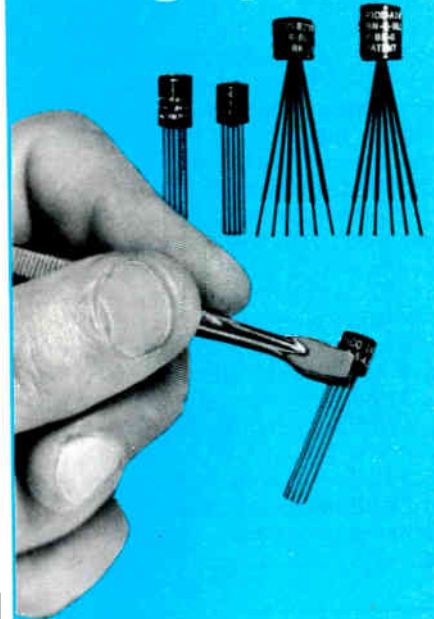
As a business strategy, BEST-I aims at an attractive niche, says analyst Jim Feldhan, vice president for operations at Integrated Circuit Engineering Corp. in Scottsdale, Ariz. "ECL tends to carry high average selling prices and there is not as much competition in bipolar arrays as in MOS arrays," he says.

**NO JAPANESE.** Also, the leading Japanese chip companies have not targeted ECL gate arrays as a big market. "It's good to have one or two markets where you're not in heavy competition with Japan," Feldhan says. "AT&T has experience in bipolar processes, and it may have looked at its production costs and concluded ECL arrays will be very profitable."

ICE projects the bipolar gate-array market—which is predominantly ECL—as growing from \$875 million in 1988 to \$2.1 billion by 1993. Although impressive, those figures pale somewhat in comparison with MOS arrays, which ICE expects to grow from \$2.35 billion to \$8.7 billion between 1988 and 1993.

Introduced at the Custom Integrated Circuits Conference in San Diego last month, BEST-I combines a super-self-aligned device structure with an advanced epitaxial/isolation scheme to deliver significantly faster switching speeds and lower power consumption than the competition. The process offers three options for trading off between speed and power consumption. Since each

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cell in the standard-cell array can be implemented in any one of the options, a device can achieve minimal power dissipation yet have high speed where needed.

At its fastest implementation, the process offers gate delays of 80 ps and power consumption of 2 mW per gate. In applications where speed can be sacrificed for lower power, the process delivers 300-ps gate delays at 0.5 mW per gate. The middle option offers 150-ps delays and 1 mW of power. AT&T's initial BEST-I standard-cell array offering will implement devices up to 20,000 gates. A library of more than 200 standard cells is available, says Scott. Other key specifications include a maximum of 200 input/output pins, a peak toggle frequency of 5 GHz, and a minimum feature size of 1.5  $\mu$ m.

AT&T will accept designs from customers in July with production scheduled for year's end. Engineering costs will be \$45,000 to \$100,000 per design. A gate-array family based on the same cell library will be introduced in the fourth quarter, and standard parts are being considered.

Among AT&T's competitors, the company offering devices closest in performance is Applied Micro Circuits Corp. of San Diego, which has a 16,000-gate offering with 130-ps gate delays and 0.6-mW power consumption. —*Jack Shandle*

## SUPERCOMPUTERS

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### BEAVERTON, ORE.

A veritable spring rain of new supercomputers is renewing the unending race for the title of the world's fastest. At stake in the global contest is not only commercial success but a considerable amount of national pride.

The claims to the title started with the mid-April announcement by NEC Corp. in Tokyo of its SX-X44 machine, with peak performance of more than 20 billion floating-point operations/s. But that seemed only to prime the pump. During the next month and a half, several U. S. companies and one from Europe announced machines that could potentially match or outperform the NEC giant.

Leading off is Thinking Machines Corp.'s CM-2A Connection Machine, a low-end version of the 64,000-processor CM-2. The Cambridge, Mass., company also claims a 20-gigaflops peak for its product and gets a leg up on NEC by the fact that the machine is already being shipped. Then there are the claimants

that have not built their machines yet.

These include Ncube of Beaverton, Ore., with its Series 6400 Scalar Supercomputer; Suprenum GmbH of West Germany with the Suprenum system, Europe's first parallel-processing supercomputer; and a prototype development announced by Intel Scientific Computers, also of Beaverton. At the low end of the supercomputer performance scale, Stellar Computer Inc. of Newton, Mass., hit the streets in late May with two new machines.

All this flopmanship leads one skeptic close to the supercomputer business to question the claims being made by some vendors. "I think there are serious problems in that some people are announcing machines that don't exist," he says. "There's a history in the industry of people doing that."

He cites as an example a system announced some time ago by Floating Point Systems Inc. of Beaverton that was rated at 100 gigaflops "after being shown running at just a few gigaflops."

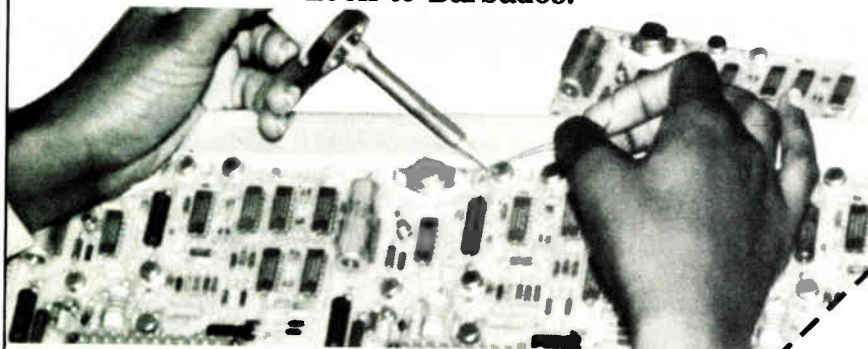
But the company "couldn't scale up from the few processors that were demonstrated and eventually withdrew the machine from the market." He adds, "There's a big difference between extrapolated performance and actually having customers who have seen the full configuration and run applications on it with measured performance."

**OLD STYLE.** As for the latest crop, only the NEC SX-X series models are traditional supercomputers, meaning that they are composed of a few very fast processors that are made from exotic state-of-the-art technology. The supercomputers now offered by the market leader, Cray Research Inc. of Minneapolis, are of this type. The other super machines rely on highly parallel architectures with thousands of processors to reach their blinding speeds.

Speed ratings notwithstanding, because the SX-X series won't be delivered until the third quarter of 1990, it seems pretty clear that there is no NEC machine today that can be evaluated at 20 gigaflops. When it does appear, it will be sold in the U. S. by HNSX Supercomputers Inc., the Burlington, Mass.-based joint venture of NEC and Honeywell Inc.

However, the CM-2A from Thinking Machines has indeed been shipped to some customers. And the 27-gigaflops Ncube 6400 series will be ready to ship in July, says the company. But the prototype machine being developed by Intel under contract from the Defense Ad-

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vanced Research Projects Agency, called the Touchstone project, is not expected to be demonstrated until the end of 1991.

So why all the fuss? The answer is that these machines—if and when they are built, if and when they are up and running, if and when live up to their makers' claims—are exciting simply because of the technology achievements they represent. Beyond that, it is spellbinding to think of what problems can be solved, what products can be designed, and what else could be done using computers with such awesome power.

Take the NEC SX-X series. It includes eight standard models with from one to four processors apiece, with each model offering options for one, two, or four pipeline sets per processor. HNSX claims the basic processor is the first general-purpose multiprocessor supercomputer to provide more than 5 gigaflops per processor. A top-of-the-line SX-X44 has four processors, each having four pipeline sets, for a total of more than 20 gigaflops. The NEC-developed processors are implemented in 20,000-gate current-mode-logic arrays that feature a 2.9-ns clock cycle and switch in 70 ps.

With its current introduction, Thinking Machines is dropping down to cover a lower end of its market. The CM-2A is an 8,192-processor system priced at \$970,000 for the university market, says Danny Hillis, a founder and director of research. Its floating-point performance is 2.2 gigaflops over a 32-bit-wide data path.

The Ncube 6400 series, in a configuration of 8,192 specially designed processors, delivers 100 billion instructions/s and 27 billion scalar floating-point operations/s, says the company.

To achieve such performance, Ncube's engineers developed an integrated VLSI processor. This advanced circuit contains a 64-bit central processing unit, 64-bit floating-point unit, error-correcting memory-management unit, message-routing hardware, and input/output processors. The machine is compatible with the current line of Ncube supercomputers.

**DUE THIS YEAR.** The first two clusters of the West German Suprenum system were shown in action at the April Industrial Fair in Hanover, but the full configuration will not be done until the end of the year [*Electronics*, May 1989, p. 67]. Each cluster of the Bonn-based company's machine boasts a speed of 320 megaflops. So when 16 of these clusters are combined into Suprenum's full configuration, the machine will sport a 5-gigaflops speed, performance rivaling that of top U. S. and Japanese supercomputing systems currently being delivered. Suprenum plans eventually to market the supercomputer in the U. S.

Meanwhile, in the Intel/Darpa Touchstone project, as many as 2,000 processors are expected to improve parallel

computing performance to 100 times above what it is today. Each CPU node to be built by the Beaverton division of Intel Corp. will have the power of the original Cray-1 supercomputer.

The Touchstone prototype will, like Intel's current iPSC/2 parallel supercomputer, contain the company's most advanced off-the-shelf microprocessors, including the recently announced i860.

At the low end, Stellar's GS2000 graphics supercomputer and DS2000 depart-

mental supercomputer series double the peak performance of the company's first machines, introduced in March 1988 [*Electronics*, March 17, 1988, p. 97]. By incorporating eight adders and eight multipliers instead of the four each in the GS1000, the GS2000 delivers 80 megaflops. An optional accelerator boosts scalar processing rates from 20 to 35 mips and peak floating-point performance to 100 megaflops. —Tom Manuel, with additional reporting by Lawrence Curran

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## MEDICAL ELECTRONICS

### OPEN WIDE: CAD/CAM GOES TO THE DENTIST

#### BENSHEIM, WEST GERMANY

Computer-aided design and manufacturing technology is finding its way into an unlikely setting: the dentist's office. Siemens AG, the Munich electronics giant, is now marketing a computer-assisted method for making tooth fillings from a piece of ceramic material.

With the company's new Cerec—for ceramic reconstruction—system, a dentist can design, make, and insert a ceramic filling for a patient in one session. Currently, ceramic fillings take several office visits to complete.

Cerec is the first use of CAD/CAM in dentistry, Siemens executives say. The method involves taking a picture of the affected tooth with a camera that produces a three-dimensional image on a monitor. Based on this "optical impression," the dentist uses the computer to design the filling right on the screen.

Then, using the filling's contour data as generated by the computer, an automatic milling machine produces the filling in just a few minutes. Finally, with a dual-cure composite material, the dentist cements the filling into the cavity, finishes the occlusion, and polishes the filling's exterior surfaces.

**ONLY AN HOUR.** The process, from cavity preparation to filling insertion and polishing, takes an experienced dentist about an hour from start to finish, Siemens says. In addition to making fillings, the Cerec system can also fabricate ceramic veneer, a thin layer of ceramic that dentists often use to cover discolored portions of front teeth, among other applications.

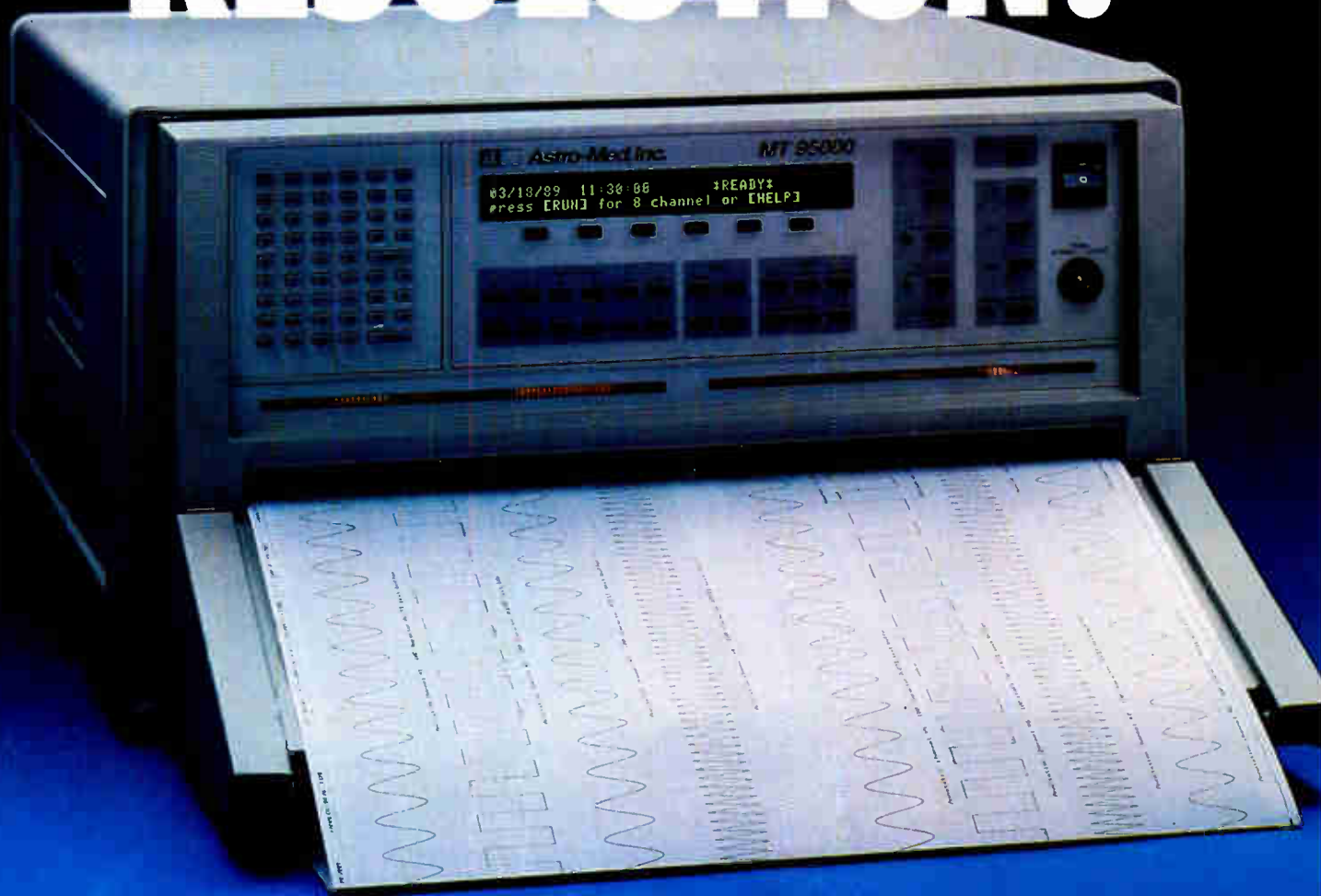
The technique was devised by two dentists—Werner Mörmann and Marco Brandestini, who are based at the Dental Institute of the University of Zurich in Switzerland. Siemens developed its system at its Dental Equipment Group at Bensheim, near Frankfurt. The group is part of the company's \$2.86 billion Medical Systems Division.

After two years of tests at a number of dental clinics, the system is now being marketed in Europe, says Günter Wiegand, a member of the Cerec consulting team at the Bensheim facility. It has been shown at an exhibition in Washington, Wiegand says, and once U.S. authorities give their approval, the system will be sold in America as well. U.S. sales could start as early as this fall, Wiegand says.

Cerec holds a number of advantages

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HPC16064	8	Yes	52	16K	512	4 ICRs
HPC16083*	8	Yes	52	8K	256	4 ICRs
HPC16104	8	Yes	32	0	512	8 CH A/D
HPC16164	8	Yes	52	16K	512	8 CH A/D
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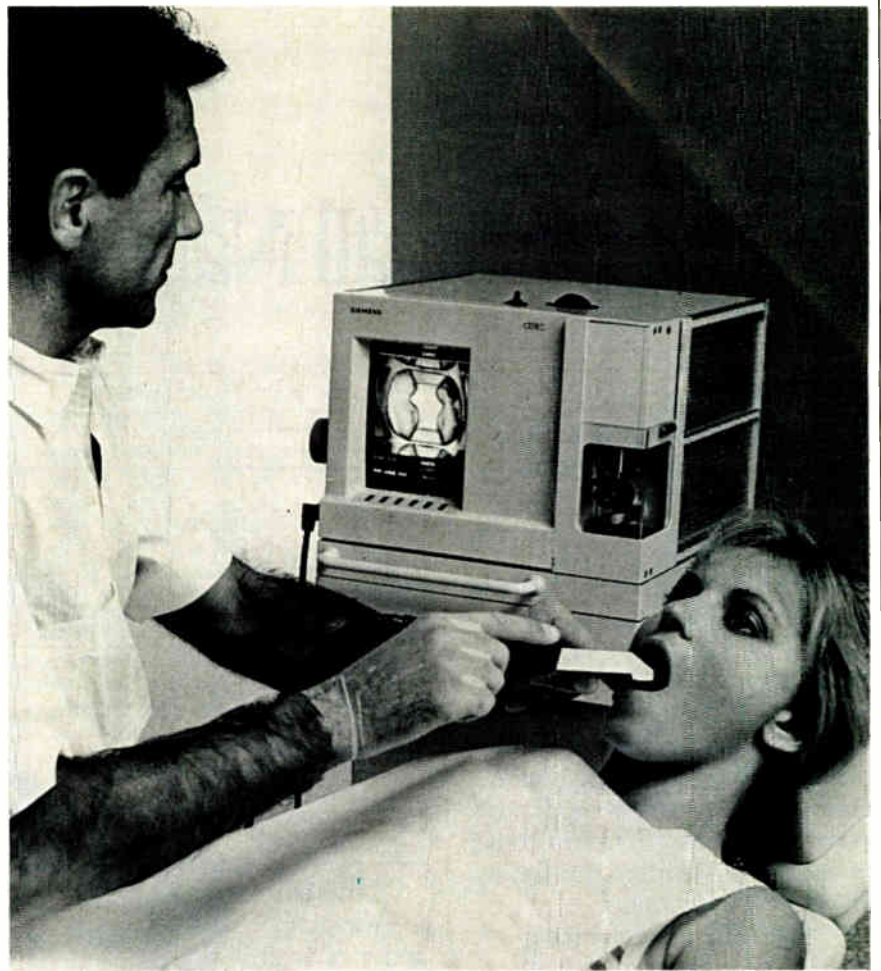
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Siemens' Cerec CAD/CAM system fabricates a ceramic filling from the image of a patient's tooth displayed on a computer screen.

over conventional dental practices and materials used for filling cavities. The most common material used for fillings today is amalgam, a moldable substance that hardens quickly. Amalgam fillings can be completed in one session, but many people object to amalgam's mercury content and its silvery appearance, especially on front teeth.

Gold, too, is increasingly unpopular because of its conspicuousness. Also, gold fillings take a number of sessions to complete. And fillings made from plastic materials are unstable and can deform under heavy bite pressures.

That leaves ceramic materials. Ceramic fillings blend in well with teeth, but up to now they haven't been widely used—mainly because, with conventional techniques, they take several sessions to complete. The dentist must make a mold, send it to a dental lab to have the filling made, and then fit—and possibly re-fit—the filling.

This is where Cerec takes over. Not only is it a time-saving, single-session treatment, but the ceramic material has a number of biological, physical, and cosmetic pluses. It is similar to natural tooth material in structure and appear-

ance, and in its manufacture, precise quality control ensures a faultless homogeneous composition. Finally, a special adhesive makes for a perfect seal.

The Cerec system consists of a hand-held camera, a monitor with integrated Siemens-designed custom computing circuitry, and a glass-encased, electronically controlled milling machine with a diamond-coated grinding disk. Cerec is priced at around \$35,000.

The water used for driving the milling machine and cooling the milling operation is contained in an internal circulating system, which means the machine doesn't have to be hooked up to a water source. The monitor and milling machine are mounted on a mobile stand so that the equipment can be operated anywhere in the dentist's office.

To master the Cerec technique, Wiegand says, a dentist must be able to interpret a 3-d object depicted on a computer screen. This ability, he says, can be acquired in a half-week training course at the Zurich dental institute. "That's a worthwhile investment," he asserts, "since detailed knowledge is needed to exploit the system's full potential."

—John Gosch



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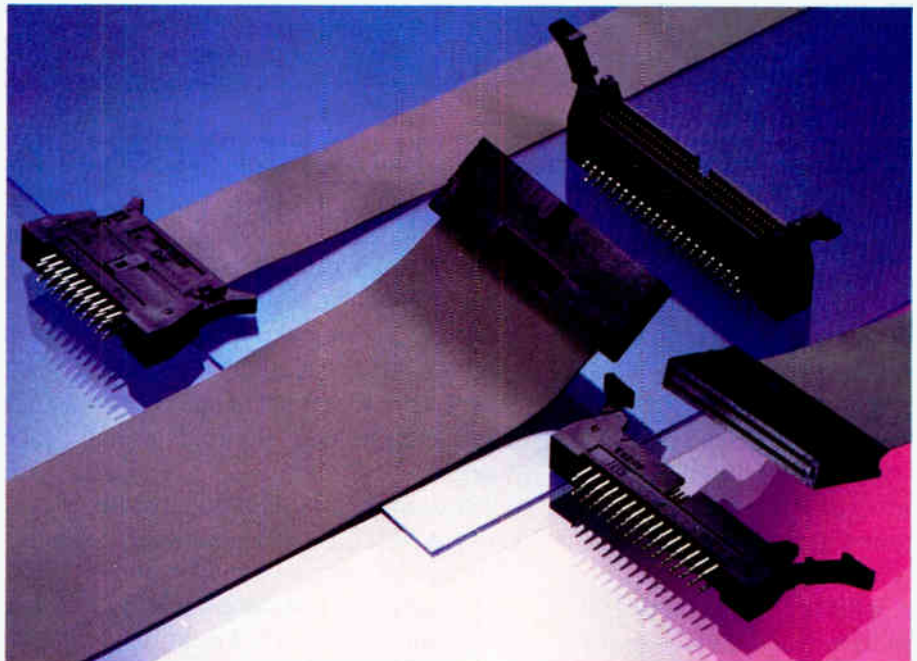
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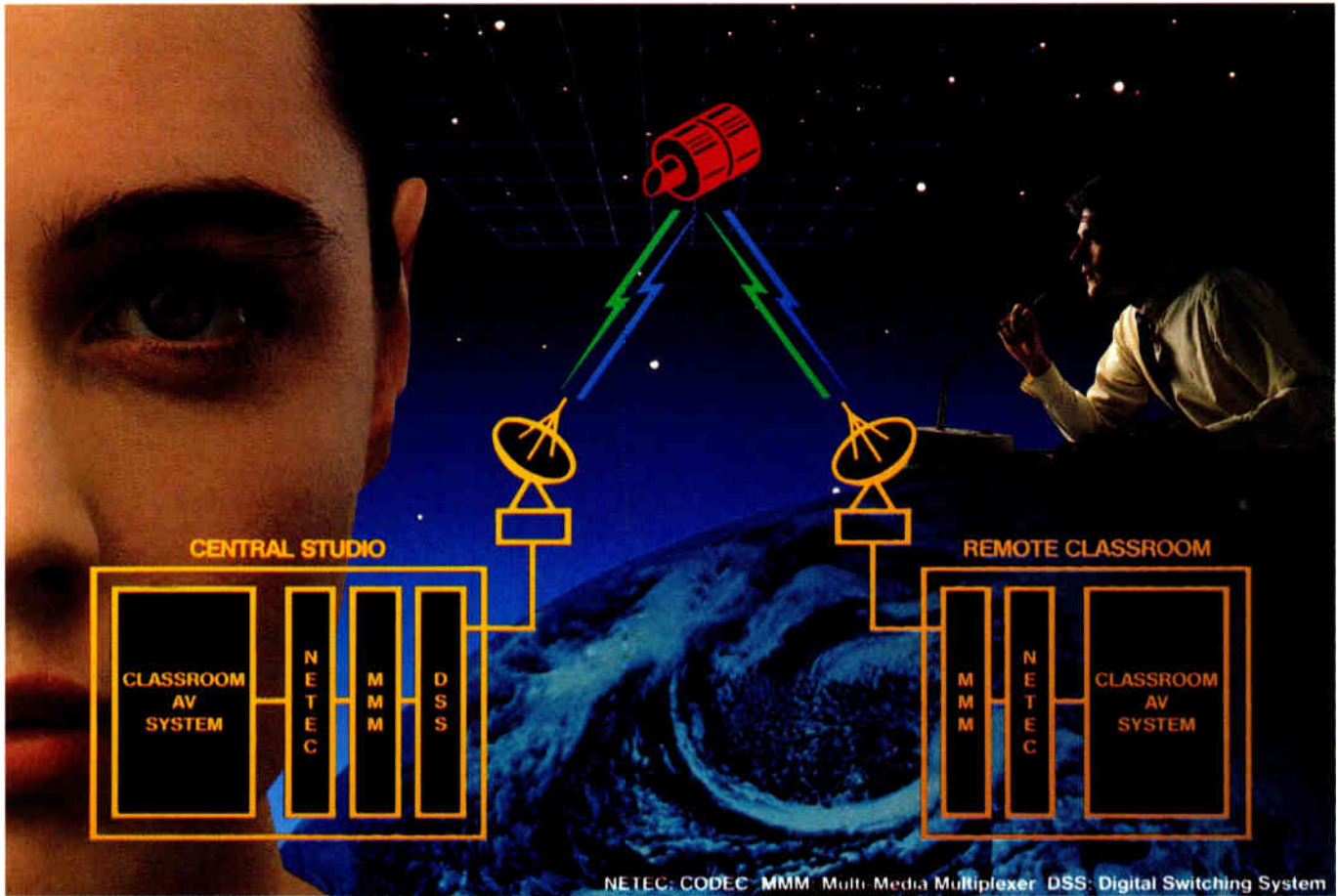
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Circle 17

## NEC NEWSCOPE



### TELE-EDUCATION VIA SATELLITE NETWORK: INTERACTIVE VIDEO AND AUDIO.

**N**EC is operating one of the world's most advanced satellite-based tele-education systems. Called NESPAC (NEC Satellite Pedagogical Network for Advanced Creative Education), the system links a central studio at the NEC Technical College near Tokyo with three other classrooms in remote locations across Japan.

The most prominent feature of NESPAC is interactive video and

audio communication between lecturer and students. The system can simultaneously transmit and receive two channels of color motion video signals, as well as one channel of audio and data signals from an electronic writing board.

For economical use of the satellite circuit, a NETEC series video codec digitizes and compresses video and audio signals to 1.544Mbps. It also scrambles the signals to ensure

information privacy. An AEC-700 echo canceller efficiently suppresses the echoes caused by satellite communication.

The NESPAC system offers a panorama of C&C technology. From the camera to the satellite transponder, from the earth station equipment to the 100-inch video projector, virtually all elements of the system are NEC products.

NEC is a leader in long-distance education systems using communications media including public telephone networks, terrestrial microwave systems, CATV fiber optic cables and satellites.

## NUMBER 141

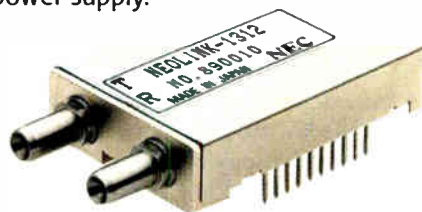
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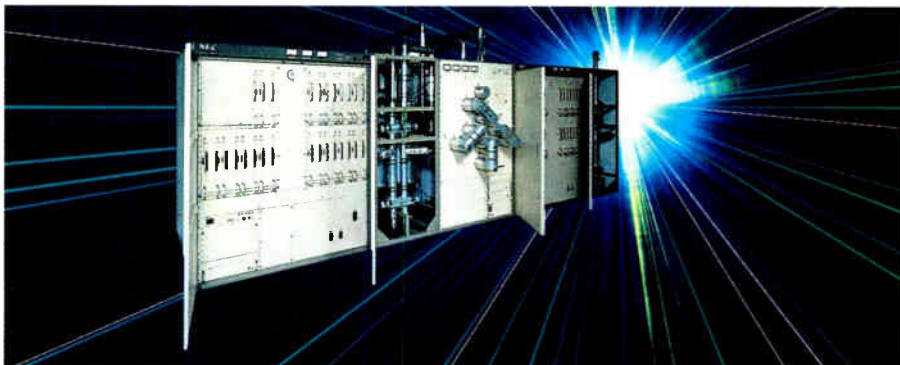
All models use 800W PA modules

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Since the transmitters operate on 28V DC power, they provide greater safety and require less maintenance. Power transistors are efficiently cooled by our "Jet Air Cooling" system.

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### VAST LIBRARY SYSTEM FOR CHINA.

NEC is supplying a large-scale information system to the National Library of China (NLC) in Beijing. With over 14 million volumes in its collection, the NLC is one of the world's largest libraries.

The library system for the People's Republic of China consists of two mainframes for database management and 270 personal computers for terminal applications. The system will handle 56 languages and allow retrieval of millions of books in each language

by category and author listing.

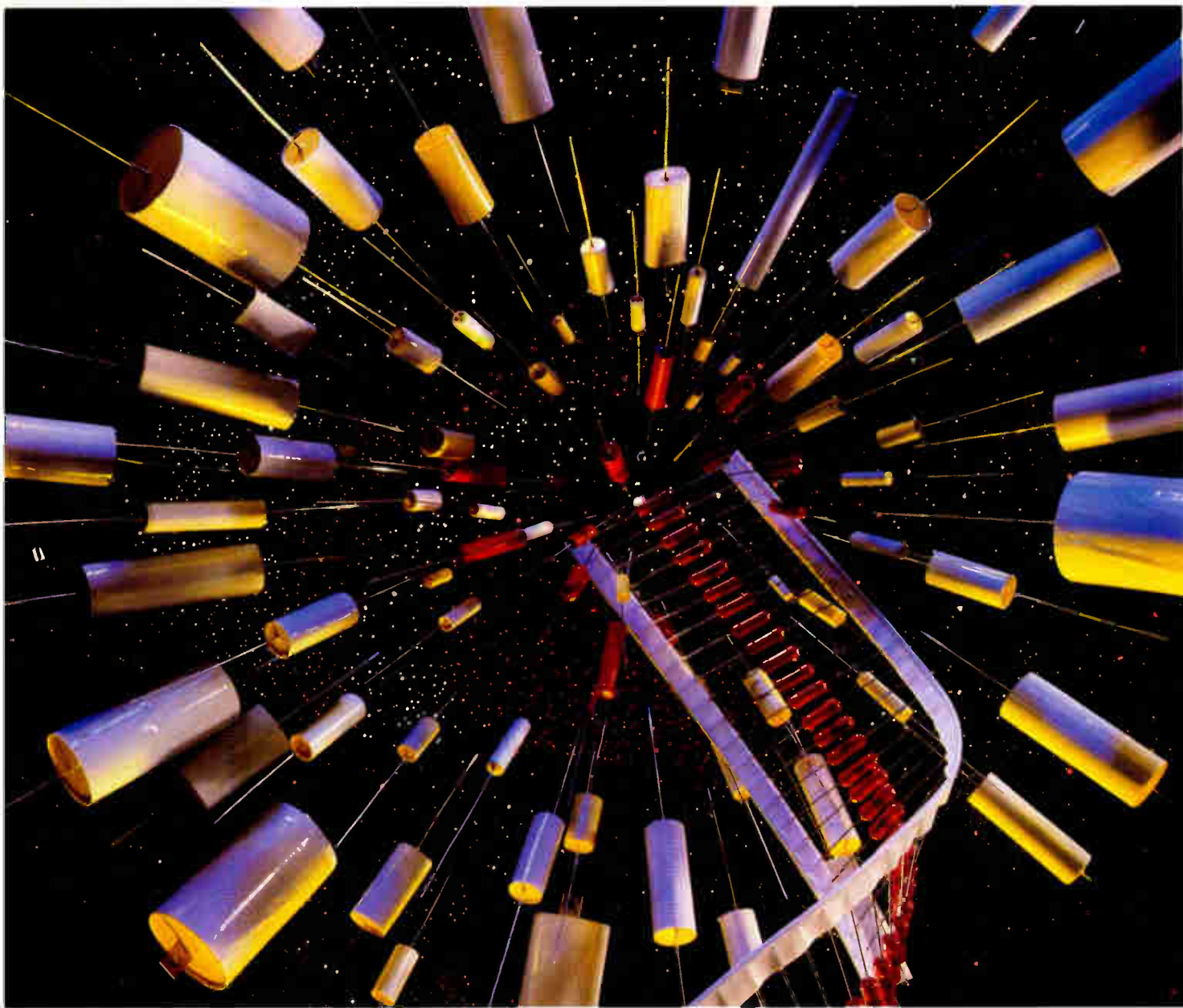
The NLC and NEC are jointly developing Chinese-language software for the system. The software will meet China's new national standard of 32,000 characters. The library system will be in full-scale operation in mid-1991.

Since the NLC is one of China's academic centers, it will use the system in the future as the core of a network linking thousands of libraries around the country.

# NEC



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Circle 56

# WASHINGTON INSIDER

## GLENN TAKES ANOTHER SHOT AT SETTING UP A CIVILIAN VERSION OF DARPA

Seeking to give the federal government a civilian arm to help manage strategic technologies, Sen. John Glenn (D., Ohio) will introduce a bill this month to establish a civilian research agency within the Department of Commerce. It's Glenn's second crack at such a program, which would serve as a civilian counterpart to the Pentagon's Defense Advanced Research Projects Agency, and it comes amid rising frustration among the Democratic Senate leadership that the Bush Administration is not pursuing an aggressive industrial strategy. "People are looking for some sort of systematic vehicle for funding nondefense industrial research programs," says a top Glenn aide. Glenn's proposed Advanced Civilian Technology Agency would invest in strategic technologies such as high-definition TV (see p. 44), high-temperature superconductors, and biotechnology. Modeled on Darpa, ACTA would have a small core of about 35 staffers managing programs worth up to \$200 million a year. And it could be just what Darpa has been waiting for: a high-tech sister that could help manage industrial-base programs like Sematech and HDTV. □

## FEDERAL USERS DRIVE AN EMERGING SOFTWARE ENGINEERING STANDARD

Complex government computer systems and networks, such as the information-management system NASA is building for its massive space station effort, are driving the computer-aided software engineering industry toward standards for interoperability. "It's very similar to what's been happening on factory floors," says Thor S. Johnson, director of product marketing at Cadre Technologies Inc., a CASE tools supplier in Providence, R. I. "They started out automating what was easiest to automate, and now they're connecting those islands of automation." In the space station project, for example, NASA is standardizing on three levels—IBM-compatible PCs, Apple Macintoshes, and Unix-based work stations. Because each level uses its own set of CASE tools, NASA needed a way to let them all communicate. Enter CDIF, the CASE Design Interchange Format. CDIF provides a universal set of hooks that lets one vendor's tool set exchange data with another's. CDIF is also being embraced by the Joint Integrated Avionics Working Group, which is trying to merge Army, Navy, and Air Force development efforts for next-generation avionics systems. "The government's need for standardization has caused it to drive the adoption of standards," Johnson says. "CDIF is now virtually a de facto standard." □

## HERE'S A WAY TO MAKE FOCAL PLANE ARRAYS DENSER—AND SMARTER

The Air Force is showing renewed interest in a technology it all but dismissed 20 years ago: metal silicides for infrared focal plane arrays. IR focal plane arrays, used in forward-looking IR night-vision systems, are key to developing passive sensors that won't broadcast their whereabouts, as radar does. But the materials usually used for these scanners—mercury cadmium telluride and arsenic-doped extrinsic silicon—are hard to process, making for very low yields. They also cannot support the electronic circuitry needed to process incoming data, requiring tedious bonding techniques to wire silicon multiplexers onto the arrays. Advances in materials processing and circuit design are fueling a new interest in an alternative technology: platinum silicide. By building on standard silicon chip-processing techniques—PtSi uses a silicon substrate coated with a thin layer of platinum—it makes integrating processing circuitry onto an array easy, says Freeman D. Shepherd, chief of the Rome Air Development Center's Electronic Device Technology Division at Hanscom Air Force Base, Mass. And while conventional focal planes integrate 500 to 1,000 detectors on a chip, Shepherd says some manufacturers have produced PtSi arrays with as many as 300,000 detectors. □



# WASHINGTON INSIDER

## THE PENTAGON TAKES ANOTHER BIG STEP TOWARD GENERIC CHIP SPECS...

**T**he Defense Department is on the verge of issuing its long-awaited Qualified Manufacturing Line standard, and will certify four chip makers to the new spec by the end of the year. The new standard—Mil-I-38535—is the second in a series of generic specifications designed to eliminate current part-by-part qualification procedures, which include expensive destructive testing and full-scale audits of plant records. The first generic spec allowed chip producers to qualify entire families of gate arrays, freeing them from qualifying each application-specific design. The QML concept goes a step further: it lets chip makers certify an entire line and process, so that any part produced on that line automatically meets military specs. The new standard imposes minimum levels of statistical process control and requires a commitment to "total quality management" and the ability to show a continuous improvement in yield for all products produced on a line, says Robert W. Thomas, a special assistant to the Reliability Directorate at the Rome Air Development Center, Rome, N. Y. Thomas isn't saying who the first QML-certified chip makers will be, but the foursome should come from this list: Harris Semiconductor, IBM, Intel, LSI Logic, National Semiconductor, Texas Instruments, and VLSI Technology. □

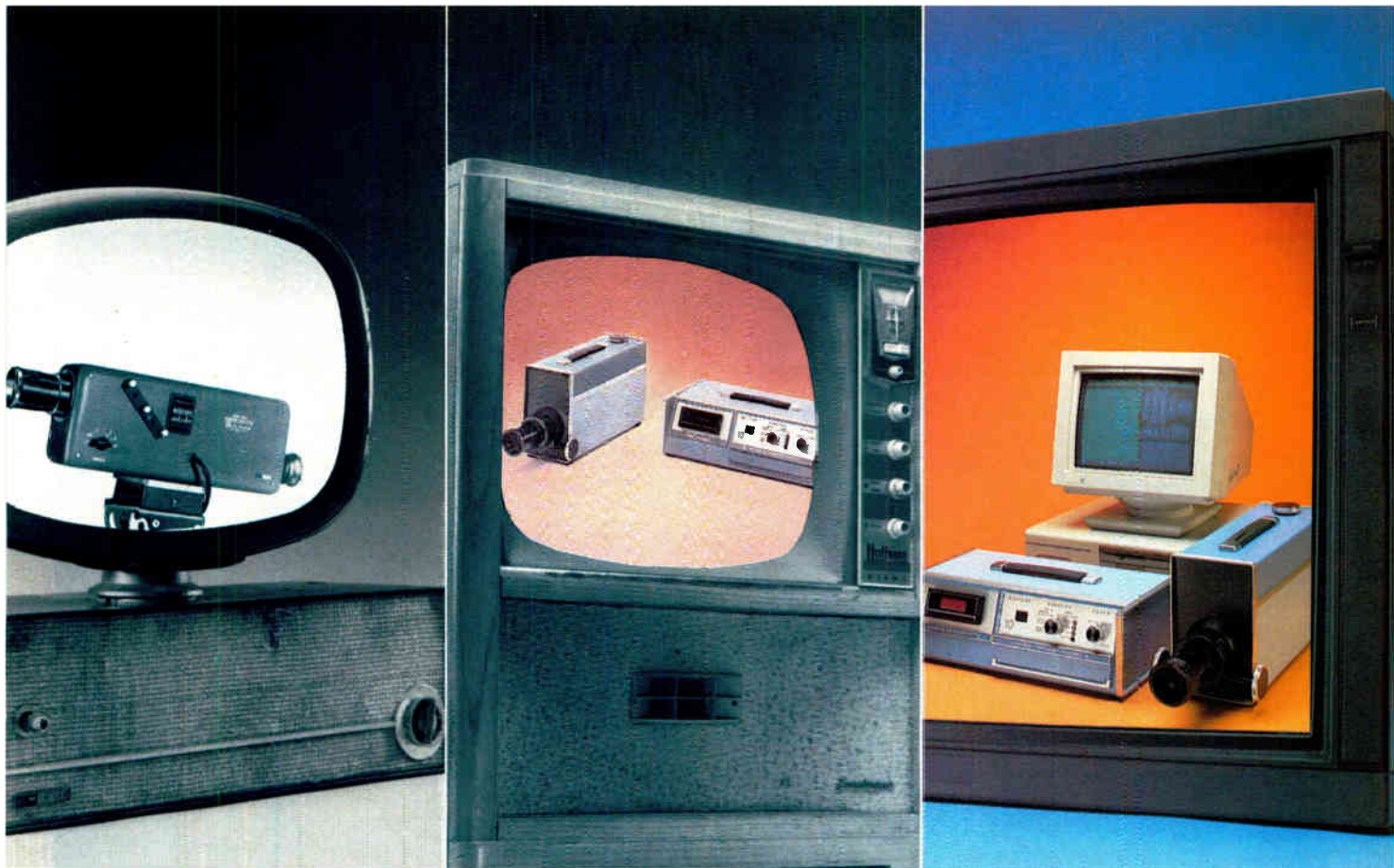
## ... AND HOPES THE COMPUTER AND AUTO INDUSTRIES WILL FOLLOW SUIT

**D**riving the military's desire for generic specifications is an underlying wish to cut the cost of military semiconductors and to narrow the distinction between commercial and military-grade chips. So the Defense Department is actively marketing its QML designation to the computer and automotive industries. Such vendors could hasten industry's acceptance of the QML spec, thereby giving the military a wider range of QML suppliers faster than could otherwise be expected. If the idea catches on, it could force every major chip maker to seek QML designation. That would put the military's cost per chip more in line with what industry now pays. "Ultimately, we'd like to see both military and commercial chips produced on the same line," says Robert W. Thomas of RADC, which is coordinating the QML program with the Defense Electronics Supply Center in Dayton, Ohio. Already Digital Equipment Corp. "is considering adopting QML to save money," he says. By specifying that suppliers meet the QML standard for its commercial chip purchases, DEC could eliminate its own costly audit burden. "We expect the computer makers to be the first to adopt QML, then the automotive people," says Thomas. □

## SMALLER AND SMARTER: SDI KEEPS REVISING ITS INTERCEPTOR STRATEGY

**B**rilliant Pebbles, a concept that places increased emphasis on sophisticated electronics and sensors, is rapidly becoming the centerpiece of the Bush Administration's revised Strategic Defense Initiative strategy, says SDI director Lt. Gen. George Monahan. It replaces earlier plans for multiple space-based garrisons of 10 antimissile weapons with a virtual cloud of "free-flying singlets," he adds. The new approach involves autonomous 3-ft-long projectiles carrying their own surveillance systems and tracking sensors in a compact 88-lb package. These weapons would destroy their targets not with explosives, but simply by colliding with them. Behind the concept are advanced microelectronics, including off-the-shelf commercial microprocessors that can pack the necessary computing power and infrared sensing systems into a tiny package. At least two prototypes—from Boeing Co. and Hughes Aircraft Co.—are using Very High Speed Integrated Circuit technology to shrink the interceptor's Inertial Measurement Unit, its central navigational device, from what Monahan says was "the size of a breadbox 10 years ago" to the size of a tennis ball. The technology is shrinking the IMU's price, too, from about \$70,000 to only \$5,000. □





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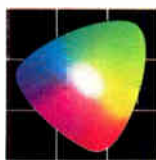
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# EUROPEAN OBSERVER

## PHILIPS UNVEILS MICROCONTROLLERS FOR LOW-COST CONSUMER GEAR . . .

**W**ith consumer applications in mind, engineers at Philips International NV's design center in Paris have readied a family of 16-bit CMOS microcontrollers that boast low power consumption and low cost coupled with high performance. Claimed to be the first 16-bit microcontroller series for high-volume consumer equipment markets, the 90C100 family extends the application spectrum of the industry-standard 68000 instruction set, which supports high-level languages such as C, works with multitasking kernels, operates in OS-9 and Unix environments, and can address up to 4 Gbytes. The family consists of three devices so far—a read-only-memory microcontroller, a version without ROM, and one with EEPROM. Despite the high density—the biggest version integrates 430,000 transistors on a 70-mm<sup>2</sup> chip—the devices consume less than 0.5 W, which suits them even for battery-powered consumer products. As samples, the ROM version sells for about \$35, but Philips says the price will eventually drop to \$8 apiece, a result of high integration levels and a small silicon area stemming from the shrinkage of feature sizes from the present 1.5 to 1.0 μm. □

## . . . AND READIES SAMPLES OF MEGA PROJECT'S 1-MBIT SRAMs

**R**ight on target with its part of the five-year Mega project, a joint effort with Siemens AG of West Germany to develop high-density memory technology, Philips International NV is ready to sample its 1-Mbit static random-access memory. The device has a 128-K-by-8-bit organization, boasts an access time of 35 ns, and is made in a single-poly, double-metal CMOS process. The 94-mm<sup>2</sup> chip consumes 30 mA at 20 MHz. The SRAM will go into full production during the second half of next year, the Dutch company says. □

## THE BRITISH ARE BRINGING RISC INTO THE HOME

**R**educed-instruction-set computing is coming home, thanks to Acorn Computers Ltd. The Cambridge, UK, company is apparently the first to market with a low-cost RISC-based personal computer, the A3000, which it says blazes away at 4 million instructions/s. Priced at £645 in the UK (about \$1,100), the machine is aimed at educational and home users. The A3000 is built around Acorn's ARM (for Acorn Risc Machine) chip and runs a proprietary operating system, RISC/OS, which provides full multitasking and a color graphical user interface based on icons and overlapping windows. The computer has 1 Mbyte of random-access memory, a single 3.5-in. floppy disk, stereo sound, and 640-by-512-pixel graphics resolution. A software option lets the A3000 emulate IBM Corp. PCs and compatibles running under MS-DOS. The machine will be available in late July; Acorn does not plan to market it in the U. S. □

## SOVIETS ENTER 'MAILBOX' VENTURE WITH WEST GERMAN FIRMS

**T**he first joint venture between Soviet communications authorities and foreign companies is off the ground. Called Interlink USSR, the \$3.8 million venture with two West German firms aims to set up a mailbox communications network that, using the country's phone lines, will eventually extend to all major cities in the Soviet Union. Supplying the mailbox computer and system savvy is Deutsche Mailbox GmbH of Hamburg. Profin GmbH of Freiburg will supply peripheral equipment such as personal computers, modems, and acoustic couplers. In its first phase, the mailbox net will cover the Greater Moscow region; subsequent phases will extend it to other metropolitan areas. The Soviet Ministry for Communications owns 51% of Interlink USSR, with each of the West German firms holding a 24.5% share. □



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64K x 4	256K	20	25	35	Early '89	
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32K x 8	256K	20	25	35	Early '89	
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BY ROBIN NELSON

# Software's Midlife Crisis



When Microsoft stock plunged due to product delays, executive vice president Steve Ballmer (center) snapped up \$46 million worth

# M

icrosoft chairman Bill Gates sees no easy solutions, but boy, can he state the problem



# If Microsoft doesn't know how long it will take to ship packages, who does?

Earlier this year, Microsoft Corp., a company that is both a unique corporate microcosm of the heady world of desktop computing and a prime beneficiary of its market explosion, became a self-confessed participant in what is being called the Software Gap. The Redmond, Wash.-based company's stock plunged overnight following its announcement of incremental delays in shipping several applications products.

When *Electronics* visited the Microsoft campus some weeks later, a spokesman mentioned that the company's executive echelon was surprised at the depth of the negative reaction, but hardly daunted. Not long after the downtick that diminished Microsoft chairman and chief executive officer Bill Gates's personal net worth by an estimated \$147 million in a single day's trading, some \$46 million of the company's stock was reported to have been acquired by Steve Ballmer, executive vice president for systems software.

So Microsoft remains bullish on itself, a posture that seems totally consistent with its latest quarterly performance statement. Yet questions remain: the company had busted product schedules any number of times before—in fact, its original Windows release established a kind of vapor-state record for software in its class—so why now the public spanking on Wall Street?

Part of the answer seems to be a growing malaise surrounding the entire packaged software industry, of which Microsoft is the natural bellwether.

After all, if the company that breakfasts with Intel, lunches with IBM, has the likes of Compaq, Hewlett-Packard, and AT&T on its dance card every night, has sold the most Macintosh software, has delivered the most Unix (Xenix) packages to microcomputers, and owns the Rosetta Stone upon which DOS, Windows, and OS/2 are inscribed—if Microsoft doesn't know how long it is going to

take to get new software packages out the door, who does?

Another part of the answer may lie in the protracted indifference to the new generation of system software, Microsoft/IBM Corp. OS/2, on the part of DOS-based corporate customers. The prime

reason for this connects back to the self-same Software Gap—there aren't yet any new and exciting OS/2 applications to provide a compelling reason for upgrading. "I certainly wish they'd come out faster, both from us and everyone else," Gates told us recently. Noting that Microsoft recommends a minimum system configuration of 4 Mbytes of random-access memory in microsystems running OS/2, he added, "It's not because we absolutely require that but to give applications developers a target [with] lots of room to grow and to run multiple applications that work together." Having thus upped the ante, Gates acknowledges that high system memory costs are the second most cited reason why OS/2 isn't selling any better.

We asked Gates to comment both on rapid gains in microprocessor development and the apparent struggle to produce software that can fully exploit the performance of newer chips.

"People are particularly confused right now, as they are at the start of any new generation," he told us. "But one thing not to forget is that software quality is more relevant than raw mips performance in delivering benefits to users. We have these incredible performance increases, then people say, 'Okay, when will software come along to exploit that?' That's a good question, because they're really asking what we're going to do to justify [users'] buying the high end versus the low end.

"I mean, with the [Intel Corp.] 386SX chip selling for way under \$100 and still coming down in price, is that going to be adequate for most office product users? Probably so—until software comes up with the next turn of the crank, which may take a while. These performance increases, even within the binary-compatible Intel 80X86 family, are outrunning what the general PC user needs."

Does Gates, we asked, see anything on the horizon, like object-oriented programming techniques, significantly boosting software development?

"There's only one trick in software," he responded, "and that is using a piece of software that's already been written. Subroutines do that, but they tend to be so specific that there are a very limited number of situations where you can reap-

ply them. The idea of object-orienting a program is to express subroutines—express codes, methods, whatever—in a way that makes them more generally useful.

"At first glance you tend to say, 'This can do anything!' But there are efficiency issues to be considered, and there are also design issues. Still, object orientation can

help simplify a lot of the software development process.

"Another way is visual programming—there isn't even a good buzzword for it yet—letting people zoom in, zoom out, and see things. The two can interplay—you can have object-oriented visual programming."

Not surprisingly, Gates sees neither Unix nor the current proliferation of high-powered RISC, BRISC, CRISP, and so on, microprocessors taking advantage of the current software crisis to make serious inroads on the office desktop—at least his admittedly very homogeneous vision of it—despite the contrary projections of some analysts.

"Unix has an important role to play," Gates postulates, "but some people overstate what it is. It's a 1960s operating system that, at the most—that's if all the confusion went away—would provide source-level compatibility among a variety of machines. It would not provide a solution for [the problems of] package software that's been the heart and soul of this industry.

"In Unix, variances are characterized by its openness and the committee-oriented nature of that process," he says. "You just can't have that committee-type thing making decisions about what's good, because it makes for so many missed opportunities."

And the new chips?

"It always amazes me," Gates told *Electronics*. "People are acting like there's going to be all this proliferation of new architectures, but they don't remember what happened in 1981. Why couldn't Digital Equipment Corp. then promote its desktop machine? Why couldn't Hewlett-Packard, Texas Instruments, or Wang? What was it that drove those things out of the marketplace? The packaged software did it. Even though those people paid a lot of money to get the current popular software moved over to their plat-



## WHAT'S BEHIND ALL THE SOFTWARE DELAYS?

The biggest names in personal computer software are hurting. Companies like Lotus, Ashton-Tate, and Microsoft are suffering from software delays. Crucial projects have slipped far beyond their original shipping dates, which delays revenue and depresses stock prices. The late-delivery syndrome goes hand in hand with another big problem in the software industry—software development has fallen way behind what's happening in hardware.

While PC hardware is flexing its muscles—managing rich graphical user interfaces and taking on complex multitasking and distributed computing tasks—the software to handle these jobs remains scarce. Application software for the new graphical and distributed-processing paradigms is large and complex—not software one bright programmer can dash off in a few days or weeks. Such coding takes teams of programmers weeks or years to write.

Indeed, the delayed packages from the software leaders are large projects requiring the coordination of hundreds of programmers and hundreds of thousands of lines of code. One big problem is that developers are still trying to produce massive software projects with old tools, outdated methods, and inadequate project management (see p. 74).

**NO QUICK CURES.** Developers underestimate how long it takes them to design, write, and test the software—hence the rash of delayed products. No quick cures are in sight either for delivery delays or for writing software that exploits the powerful new hardware. Automated tools for big software projects haven't been perfected yet. The picture isn't entirely bleak, though—there is some hope for speeding programming. It lies in object-oriented programming and hypertext tools for end-user programming.

The most glaring examples of software delays come from industry leaders. Lotus Development Corp. is at least a year behind in delivering an important upgrade to its bread-and-butter software, 1-2-3. Release 3.0 of Lotus 1-2-3 is scheduled to ship this month. To meet this deadline, though, the Cambridge, Mass., company had to break up the 1-2-3 program into two versions—Lotus engineers couldn't put all the bells and whistles for all PC configurations into one version in time. Release 3.0, a three-dimensional advanced spreadsheet, runs only on new high-end PCs—ATs, PS/2s, along with 386-based PC clones—with plenty of memory. Release 2.2, with fewer new capabilities and working within the limits of 640-Kbyte DOS machines, is scheduled to ship sometime during the third quarter.

Another delay in a flagship product is dBase IV from Ashton-Tate Inc. Writing

dBase IV soaked up about 100 programmers' time and resulted in a program about nine times bigger than the original dBase. DBase IV was three months late and full of bugs, which took another nine months to kill. The Torrance, Calif., company hopes to ship a bug-free version of the software this month.

Nor is Microsoft Corp. immune to software product delays. Earlier this year, the Redmond, Wash., company said shipping would be delayed for Microsoft Word 4.0 for the Apple Computer Inc. Macintosh along with Word 5.0 for IBM and compatible PCs. Word 4.0 shipped in April and 5.0 shipped in May, meeting the revised schedule.

Smaller companies usually fare no better, though their delays don't make headlines. Silicon Beach Software, for example, expected to ship its Supercard program for the Macintosh this month. But Supercard isn't ready, and no new release date is forthcoming. Mainstay Software is about six months behind in shipping its

while Microsoft is working on object-oriented extensions for its system software for use by its own programmers as well as for customers.

The Object Management Group was started in April to develop a standard for a common applications environment based on object management. Another 15 companies are expected to join the 11 original members.

The benefits of object-oriented programming are at least a couple of years from being realized, however. Therein lies the appeal of end-user programming.

One form of end-user programming, hypertext, relies on automatically tracking and recording a user's pathways for searching and manipulating text. Its popularity stems from the ease with which users can develop their own applications with hypertext products. Apple's Hypercard and the Supercard, developed by Silicon Beach Software, are intended for the Macintosh. And the latest entry, HyperRacks, a Hypercard add-on for the Mac,

### PRODUCT DELAYS BESET THE INDUSTRY

Company	Product	Original Date	Revised Date
Ashton-Tate	dBase IV	7/88	6/89
Lotus	1-2-3 3.0	6/88	6/89
	1-2-3 2.2	6/88	Q3 89
Microsoft	Word 4.0 MAC	10/88	Shipped 4/89
	Word 5.0 PC	1/89	5/89
	SQL Server	12/88	Shipped 4/89

Markup program, now due this month.

In large companies or small, programming is still more of an art than a science. As a result, few tools exist to speed up and automate parts of the software development process. Several computer-aided software engineering (CASE) systems are offered, but most software developers cannot pull off development breakthroughs with them. Another technique for speeding up software development is reuse of code. "There's only one trick in software and that is to use a piece of software that's already been written," says Bill Gates, Microsoft's chairman (see p. 68).

Still more promising is object-oriented programming [*Electronics*, May 1989, p. 104]. The biggest advantage in using objects and the technology behind them is that well-defined objects are easily extendable for use in a variety of situations. Using objects, previously written and debugged code can be reused quickly.

Hewlett-Packard, IBM, and Next are looking into such programming methods

was shipped last month by HyperRacks Inc. in Los Altos, Calif.

Hypertext products for the IBM machines are coming on line now too. Also from HyperRacks comes ZoomRaks for IBM PCs and compatibles. Other PC hypertext products include HyperPAD, recently introduced by Brightbill-Roberts & Co., and the Hyperdoc package from Hyperdoc Inc.

The Metaphor Data Interpretation System from Metaphor Computer Systems Inc. provides easy user-written information-managing services to Metaphor's customers. The services are available on Metaphor's work stations or on PC ATs running Metaphor software.

IBM Corp. licensed the technology from Metaphor about a year ago. Also, Asymmetrix, a Bellevue, Wash., startup, is readying a PC package that addresses end-user programming. But until these and other programming tools make writing software more efficient, users will just have to take delivery schedules with a great big dose of salt. —Tom Manuel



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## Microsoft was surprised, but hardly daunted, at Wall Street's negative reaction

forms, the [customer] knew that the latest and greatest was going to be available first on the IBM platform.

"Certainly there is going to be fragmentation in some markets, like physical modeling and computer-aided design, where we've always had fragmentation. For those areas where packaged product software is not a necessary thing, let the Sparc, the MIPS, the RT, the Spectrum, Intergraph, and a bunch of others fight it out. Our vision of the office desktop is unchanged in that binary compatibility continues to be important and that Intel architecture will dominate. Now, in the network server area, you may have some specialization and different architectures—even though our focus is, once again, on the Intel processor."

The ties to Intel become even more close when you listen to Gates talk about Microsoft's interest in a new-generation microprocessor like the 1.2-million-transistor 80860. He makes it sound like a joint development.

"We did more than look at it," he says in response to our asking for his appraisal of the 860. "Intel had done a brilliant job on the design—Les Cohen, the key designer, understands numerics. Some of our architects then took a look at it and suggested ways to make it more of a general-purpose chip, and it was improved quite a bit as a result of that feedback.

[They] were then able to place code anywhere in memory and able to do semaphores, for which instructions had [previously] not been very good. The reason our guys chose to get involved and contribute in that way is because the raw performance of the chip is quite amazing, particularly in the floating-point arena."

Gates went on to say that while Microsoft was technically able to provide a "naked, uniprocessor OS/2" to run on the 80860, the primary aim would be instead to develop ways to use it as a coprocessor in OS/2 machines. "Positioning it as a mainstream desktop chip," he added, "would get us away from the binary compatibility, which allows for package software. We're talking to a lot of customers of this chip, such as Olivetti, on how they're going to position it in their product lines."

Gates is still at his best as a visionary, but it seemed a little strange, at the time, to be talking about 50-mips coprocessors when his company was still laboring to produce its own initial OS/2 application (Microsoft Word 5.0, which shipped in mid-May). Nor was Microsoft's full-featured, Windows-based word processor—the other product delay that triggered the bad reaction from analysts—ready, and still isn't.

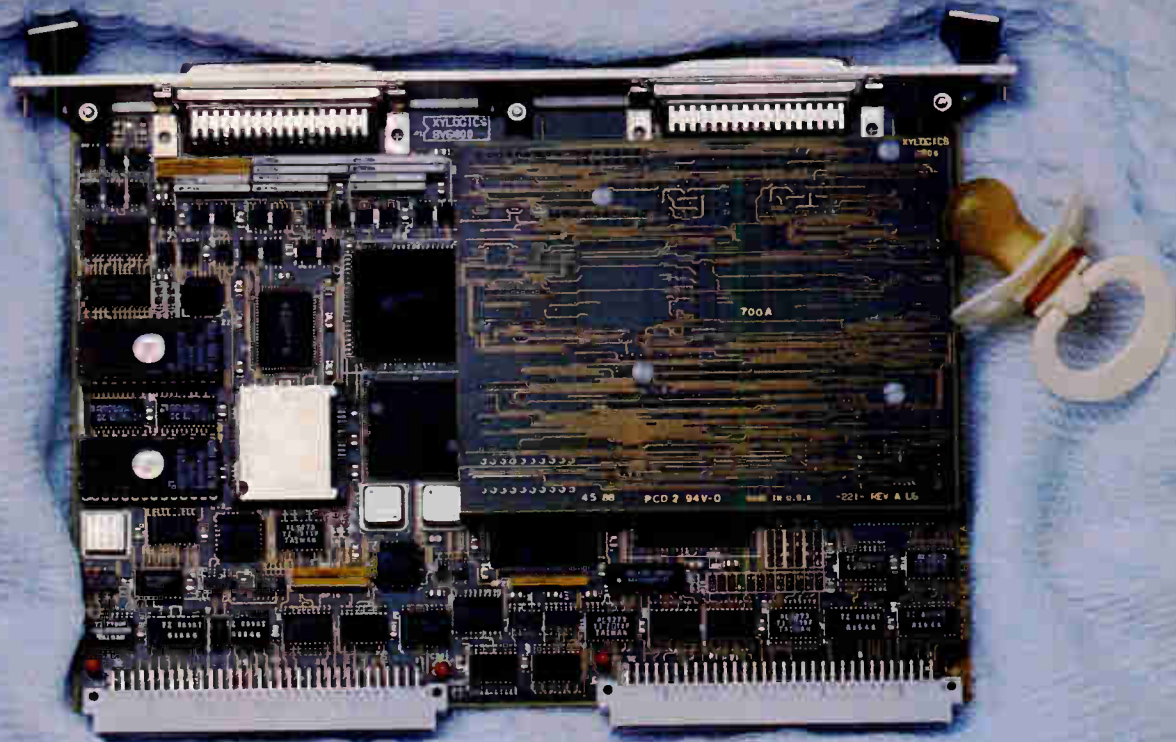
But interestingly, one is. It's called Ami, from Samna Corp., an Atlanta company

with about 170 employees. Ami has been in distribution for some five months; an upgraded Ami Professional version is due in August and appears to have most of the features that will be included in Microsoft's package. We asked Said Mohammadioun, founder and CEO of Samna, why a company like his could deliver a product running under Microsoft's own graphics-based environment so far ahead of Microsoft.

"Microsoft is much bigger [more than 3,600 employees] and has more resources than we have, but we are a very focused company," Mohammadioun told *Electronics*. "All we do is word processing. I don't know if Microsoft has 170 people working on its word processor or not—I kind of doubt it. We do."

With a network of strategic alliances that would tax a corporate data base, its broad marketing of systems, applications, and programming-language software, and the visionary zeal of its founder, Microsoft has dared to be more things to more people in its industry than any organization has before. But all the strategy in the world can't write finished code. "Software is the critical path for everything," Gates says, "for OS/2, for CD-ROM, for client-server architecture, and everything that I see having benefits for users if we exploit it properly. There is a real need for a lot more tools and a lot more innovative ideas." □





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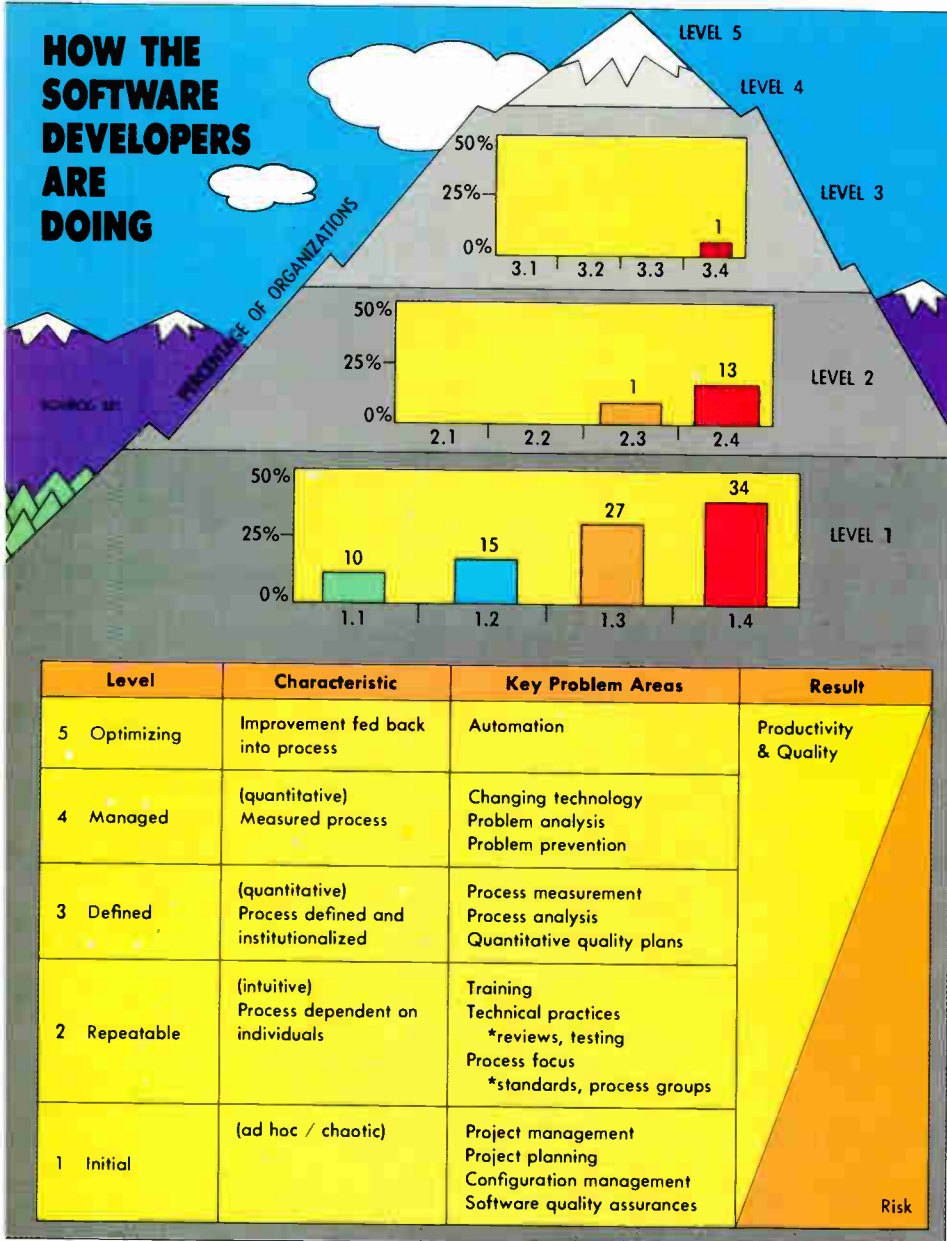
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# IT'S TIME TO GROW UP

## HOW THE SOFTWARE DEVELOPERS ARE DOING



**In terms of maturity, most software houses are at the lowest level of the SEI model**

*Why is software often so late? The problem is not in the programmers but in the management process, says the Software Engineering Institute. Its surveys show that many software operations are using 'ad hoc or possibly chaotic' methods for overseeing projects*

**W**hy are large software projects so often behind schedule? One theory holds that the complexity of software containing hundreds of thousands of lines of code has simply outstripped the methods that software houses—in both industry and government—are using to manage it. The problem is not in the programmers; it is in the process. Work conducted for the Department of Defense by the Pittsburgh-based Software Engineering Institute at Carnegie Mellon University supports the idea that project management is the Achilles heel of software organizations. Surveys by SEI's Software Process Program Group indicate that 72% of the DOD's software contractors are operating with an "ad hoc or, possibly, chaotic process" for managing projects.

Although results are sketchy and the sample of companies relatively small, commercial software houses seem to fit into the same mold, says Watts Humphrey, group director. In workshops open to commercial houses as well as government agencies and contractors, 84% of the organizations scored at the first level

**BY JACK SHANDLE**



of SEI's five-tier model for software process maturity. SEI estimates that 14% occupy the second tier and 2% rank in the third. None, so far, have reached the fourth or fifth tiers.

The SEI model ranks software operations according to their answers to 120 questions, many addressing management practices and the degree to which software quality is measured and evaluated statistically. "To date, software work has tended to get by with ad hoc or intuitive management measures," says Humphrey. "When you have a strong team of bright people, they get to a point where then can intuitively do a good job. But when you expand the task by a factor of 10, their intuition may not be as effective." Before taking the job at SEI, Humphrey logged 27 years at IBM Corp. as a software manager and executive.

From that perspective, he has concluded that a large software project needs three elements for success: creative designers, experts who understand the problem the software is meant to solve, and a disciplined management process.

While there's an abundance of software creativity, particularly in the U. S., the management process may be underdeveloped. "Software developers are creative people," he says, "and there has been a lot of reaction against disciplined management. But managing the process is not regimentation where everybody works by the numbers."

Instead, it is similar to a football team that designs and practices its plays before game time—rather than deciding in the huddle who is going to pass the ball and who is going to catch it, he says.

**DEFECTS DROP.** Although funded by the Pentagon, SEI's mission is to improve the state of software engineering practice across the board in the U. S. Within SEI, Humphrey's Software Process Program assesses software houses in and out of government. Though the individual ratings are confidential, Humphrey says SEI assessments can lead to impressive results. One large software organization improved its performance in only 18 months, he says, largely eliminating major schedule shortfalls on new projects. Customer-reported defects dropped 32.1%, and computer work-station trivial response time dropped from 7 s to 1 s.

Moving up on SEI's maturity scale is not necessarily difficult. One of the key management techniques is to form a Software Engineering Process Group to oversee and evaluate operations. Such groups are typically staffed at from 1% to 3% of the organization's professional work force and are a common recommendation when SEI evaluates a software operation. "These are groups that didn't exist be-

fore, but when you go back two years later, you find they are extremely busy," says Humphrey.

Another key is involving high-level management. "If senior management is not interested enough to review the process every four to six months," he says, "it's not going to work."

In essence, in-house engineering-process groups make sure each successive project undertaken leverages the knowledge of previous projects. "Each project has two results," says Humphrey. "The product itself and information on how it could have been done better." Among

*'When you have a team of bright people, they can intuitively do a good job. But when you expand the task by a factor of 10, their intuition may not be as effective'*

other improvements, groups can significantly improve project size estimates—that is, the amount of code—and they can devise better ways to inspect the code. The major problem organizations at maturity level 2 have in common is scaling new projects—beginning with estimating the program's size. A bad guess will throw off resource estimates for people, computing power, and time. "With a poor size estimate, they're in over their heads on the day they start the project," says Humphrey.

Testing code efficiently requires historical data for predicting which modules have the most likelihood of a high error density. But organizations do not in general collect that sort of data, so analyses are impossible. Instead, they typically run a test, fix the bugs that pop up, and ship the program. Knowing where to look for bugs is a big advantage. Humphrey cites an example of a 500,000-line program that had been in the field for three years. A close inspection showed that 3% of the code had half the errors and 16% had all the errors. In another example, a 70,000-line program was flagged by quality-control experts. A team of analysts identified more than 200 bugs in just 10% of the code.

SEI designed its software-process maturity model to represent the natural evo-

lutionary growth of an organization. Level 1 organizations have an ad hoc process that lacks formal procedures for estimating costs and planning projects. Change control is lax, and senior management is not intimately involved. When a project succeeds, it is generally because of the heroic efforts of a dedicated team rather than the capability of the organization. Moving from level 1 to level 2 can be speeded by training managers in estimating software size and required resources, SEI says. A Software Quality Assurance program should be created and supported with adequate resources.

**CONTROLS.** Level 2 organizations have built in basic controls such as project management, management oversight, and product assurance. The organization does well when the work is similar to something it has done before, but it runs into problems with new concepts and lacks an orderly framework for improvement. But SEI says most level 2 concerns can move to level 3 rapidly. Some 69% of them now have an engineering-process group; the rest need to create one. They also need to train programmers better and allocate more resources to improving the quality assurance program.

Level 3 organizations have created a framework for improvement. This includes devising a software process architecture describing the technical and management activities needed to execute it, and introducing a family of software engineering methods and technologies. In short, these organizations have succeeded in defining their development process. Since the number of level 3 organizations is so small, SEI could not develop meaningful conclusions about their specific improvement needs.

If they existed, level 4 organizations would have moved into an operational mode of statistically measuring and controlling the process of creating software. They would have a set of quality and productivity measurements and a data base for analyzing and improving the process. The key additional activity over level 3 is a rigorous analysis of why defects crop up and how to prevent them.

At the top of the pack, level 5 organizations would have automated data collection and a corporate culture that emphasizes process analysis instead of products. Data would be available to justify applying technology to critical tasks and to identify weak process elements.

Compared with other scientific disciplines, software has not been around for long. Growing up is largely a matter of implementing principles already proven in manufacturing, says Humphrey, and with SEI's maturity process defined, it also has the equivalent of a role model. □

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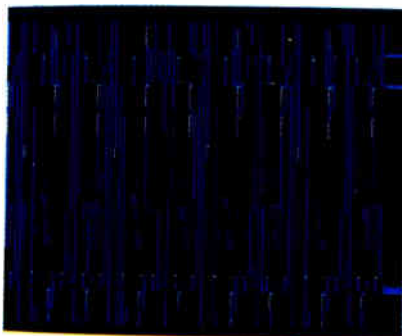
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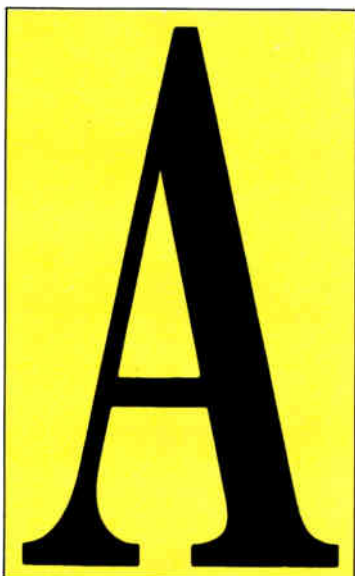
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BY JONAH McLEOD

# QUICKENING THE AUTOMATION PACE IN CAD/CAE



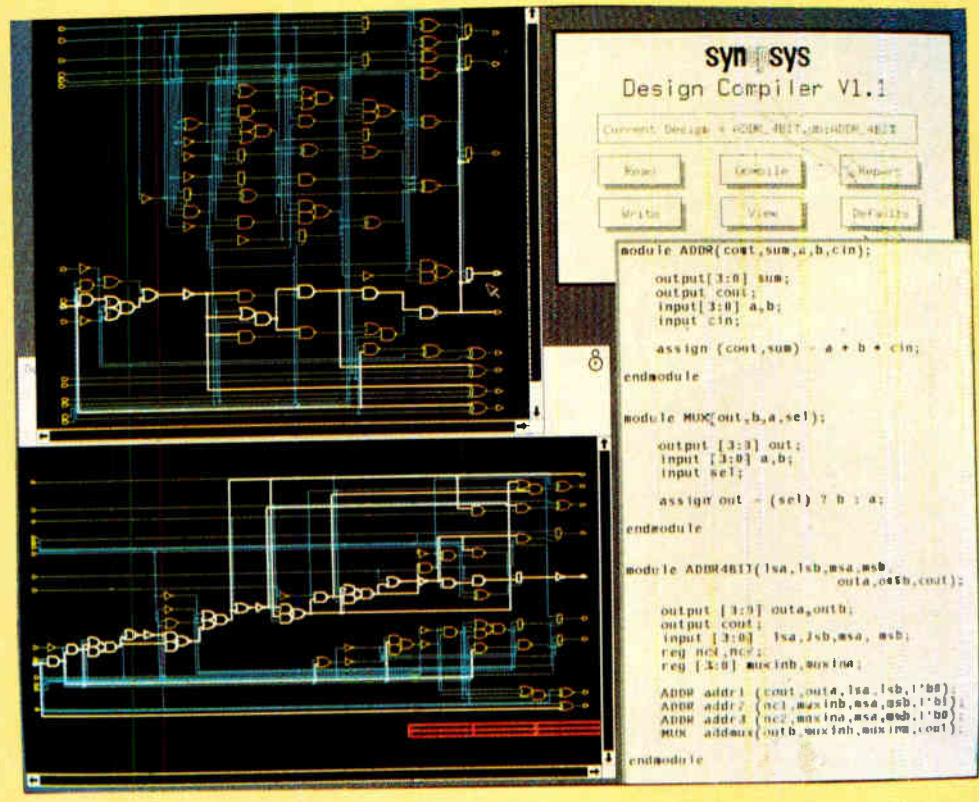
*This year's Design Automation Conference offers up a grabbag of tools that IC designers have long been hoping for.*



sk designers faced with building integrated circuits with hundreds of thousands of gates or a million transistors to draw up a design-automation wish list and they would ask for any number of tools to greatly leverage their effort. At the front end, they would want to specify complex designs using a high-level description language, increasingly the Pentagon's VHDL and Verilog in the commercial sector. Also on the list: tools for mixed analog and digital simulation. And to speed the design of the digital portions, logic synthesizers would be needed to automatically create logic gates from the high-level languages.

In the back end, at the level of computer-aided design, engineers might list tools that perform sophisticated placement and routing, such as mixing standard cells among large blocks to increase design compaction and reduce routing complexity. Ideally, those tools





**The Synopsys Compiler explores alternatives, implementing an adder two ways. Opposite: Mentor Graphics does over-the-cell routing.**

would boast added capability, such as automatic power and ground sizing, to accommodate analog and digital circuits on the same chip.

The parade of products being shown at this year's Design Automation Conference, to be held June 21 to 25 in Las Vegas, goes a long way toward making these wishes come true. The bounty of hardware and software being showcased is evidence of a high level of technology development—and a booming market.

In fact, computer-aided-engineering tools for design capture reached \$1.27 billion in sales last year, says Ron Collette, senior market analyst at Dataquest Inc. in San Jose, Calif. This market is expected to grow at a compound annual rate of 17%, reaching \$2.2 billion in 1993, he says. Back-end CAD tools will likewise flourish, growing from \$420 million in 1988 to \$740 million in 1993, according to Collette.

What most show goers will notice first is the number of vendors proclaiming support for the Pentagon's VHDL—the VHSIC (Very High Speed Integrated Circuits program) Hardware Description Language. In the wake of the announcement of VHDL support by Mentor Graphics Corp. last winter [*Electronics*, February 1989, p. 73], every CAE tool vendor is doing the same. Prime among them is Mentor's archival, Daisy/Cadnetics Inc. The Mountain View, Calif., company will introduce VHDL capability in its next re-

lease of the Daisy Logic Simulator, which will support textual as well as graphical design capture and allow for interactive debugging. "Mentor has announced this capability but it will not appear until 1990," says James Ulatowski, vice president of CAE marketing at Daisy. "Our tool is a much more complete implementation," he says; and it is available now.

**VHDL CONVERSION.** The tool handles the VHDL IEEE1076 standard except for about eight "esoteric commands" that will not be needed by most of Daisy's customers, Ulatowski says. A designer can describe a design in VHDL or use Daisy's Advanced Capture and Edit tool to describe the design and then convert it to a VHDL description. A Daisy HDL converter is also available to convert existing circuits into VHDL for simulation.

Along with the CAE vendors, application-specific IC suppliers are jumping onto the VHDL bandwagon. Harris Corp.'s Semiconductor Sector in Palm Bay, Fla., for example, is offering its Mimic simulator, now upgraded with VHDL behavioral capability, as a product on the Cadence Framework. This is the data base from Cadence Design Systems Inc. in San Jose that Harris and other ASIC vendors use to tightly integrate Cadence and other makers' design tools. Mimic accepts C, Pascal, Fortran, and PLI, in addition to CADL (computer-aided design language), Harris's own high-level

description language, says Mike Bohm, senior principal engineer. "A designer can describe behavior in one of these four languages and get binary code ready for simulation," he says.

This translation process, which is the way many vendors are implementing VHDL, is in contrast to the Mentor Graphics approach. The Beaverton, Ore., company's QuickSim simulator actually executes VHDL code without translating it into another language first. Also using native-mode implementation of VHDL is Viewlogic Systems Inc. of Marlboro, Mass., whose Viewsim simulator first shipped in July 1988. The product has found a home with more than 200 customers, Viewlogic says.

"Viewsim is a multilayer simulator," says Tony Flynn, manager of product marketing at Viewlogic. "It performs behavioral, register-transfer-level, gate-level, and transistor-level simulation." The company developed its own VHDL analyzer, which breaks down the VHDL source code into an intermediate file. Viewsim's VHDL interpreter executes the VHDL code in the intermediate file at run time. The advantage to this approach is that the designer creates a design and debugs it in VHDL instead of designing and debugging in one language and then translating into VHDL. Moreover, because designs for Defense Department applications will eventually have to be

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	AK89C47(F)	2.5V	2.5V				89/8
2K	AK89C56(F)	—	—	128 x 16	Serial	8Pin DIP SOP	89/8
	AK93C57(F)	2.5V	2.5V				
4K	AK93C66(F)	—	—	256 x 16	Serial	8Pin DIP SOP	89/7
	AK93C67(F)	2.5V	2.5V				
16K	AK28C16(F)	—	—	2K x 8	Parallel	24Pin DIP SOP	89/5
64K	AK28C64(F)	—	—	8K x 8	Parallel	28Pin DIP SOP	89/5

Extended Ope. Temp. (-40°C to +85°C) version is available.

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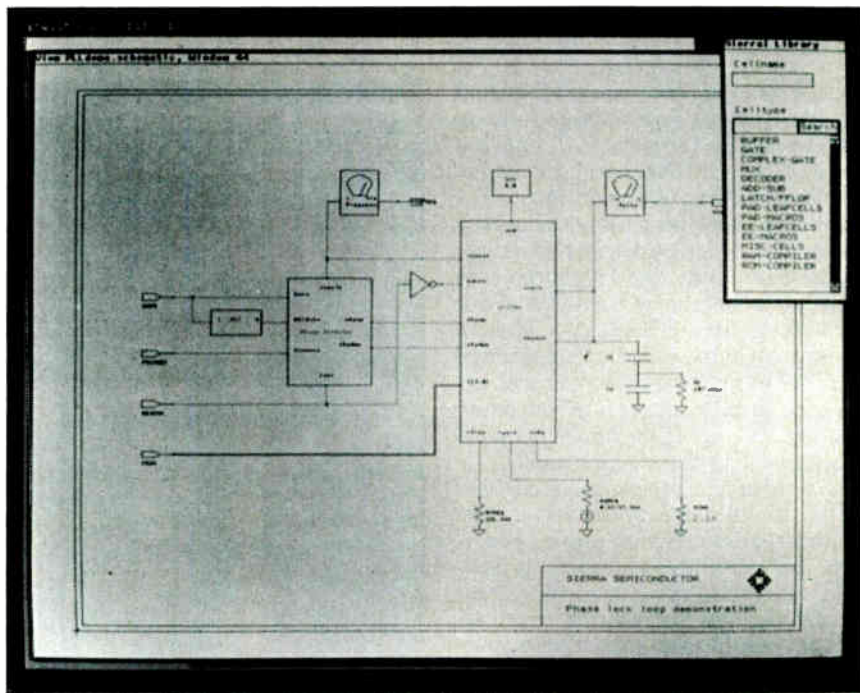
verified in VHDL, companies with native-mode implementations are well ahead of the firms using translations.

While there is a major push to VHDL, the industry is not ignoring Verilog, developed by Gateway Design Automation Corp. of Westford, Mass. "Verilog is the current commercial standard language and VHDL is the long-term industry-standard language," says Harvey Jones, president and chief executive officer at Synopsys Inc. of Mountain View. To make its language even more pervasive, Gateway—which has around 14% of the total simulation market, according to Dataquest—will roll out a new product, Verilink, at the conference. This set of object-oriented access routines gives outside tools a means of querying the Verilog data base without giving away the family jewels. It links Verilog more closely to other design tools, says Prabhu Goel, Gateway's president. Through Verilink, these tools can acquire such detailed design data as delay values of a network for better timing analysis and fan-out of gates in a network for more accurate circuit loading.

**FAMILY TIES.** Companies already using Verilink include Cadence Design Systems and Analogy Inc. Cadence uses it to tie Verilog into the Design Framework, the company's modular environment that enables diverse tools to interface with one another and to be portable across a variety of hardware platforms. And Analogy, of Beaverton, integrates Gateway's Verilog digital simulator with its own Saber analog simulator, a solution indicative of yet another trend now surfacing: mixed-signal analog-design capability.

One company recently announcing a mixed-signal scheme is Sierra Semiconductor Corp. Called Montage, the new simulator lets designers simultaneously simulate mixed analog and digital circuits to a level of accuracy previously impossible on ASICs of 40,000 gates and up. "The accuracy of the simulation is sufficient that we can guarantee the silicon produced from it," says Don McClennan, director of custom products marketing at the San Jose company. The product is built around the Lsim digital simulator from Silicon Compiler Systems Corp. in San Jose, which already has its own analog-simulation capability.

"Unlike other mixed-signal simulators, which bolt an analog and digital simulator together, we've replaced the analog-simulation capability in Lsim with algorithms of our own to provide a level of accuracy that we can guarantee," McClennan says. To get the accuracy without requiring long compute time, the simulator uses a technique called dynamic resolution, which also contributes speed.



**With Sierra Semiconductor's Montage, a phased-lock-loop simulation runs in minutes, not hours.**

When the input voltage of a comparator with a 2.5-V switching level is 0.5 V, the circuit is simulated at low resolution. When the input voltage is within millivolts of the 2.5-V switching level, the comparator's operation is simulated at very high resolution.

The simulator is very fast, too. Besides using dynamic compaction to increase speed, analog and digital events run off the same event queues, another time saver. In a combined logic and analog simulator with two independently operating event queues, simulating a phased-lock loop, for example, means halting the operation of both simulators and synchronizing the two in time to pass data between queues.

"A phase-locked loop requiring hours of simulation time on a combined mixed-signal analog and digital simulator runs

in just minutes on Montage," says McClennan.

Up to now, most mixed-signal simulators have been combinations of analog and digital simulators. NCR Corp.'s Microelectronics Division in Fort Collins, Colo., was part of the threesome that combined the Cadat simulator from HHB Systems Inc. of Mahwah, N. J., and Analogy's Saber behavioral analog simulator. While HHB and Analogy began selling the resulting product last year, NCR's effort started in January when its DesignSim A&D made its debut.

The product is part of the company's Product Design Series 2, a CAE tool kit the remainder of which NCR will roll out this month, says Earl Reinkensmeyer, NCR's director of software products. Besides the simulator, the kit contains the DesignEdit schematic-capture package and the DesignTest automatic-test-generation software, all running on Sun Microsystems Inc. work stations. Reinkensmeyer characterizes DesignSim A&D as a third-generation mixed-mode simulator, capable of handling time-domain analysis of frequency and voltage.

Viewlogic and Microsim Corp. are another set of companies that has combined a digital and analog simulator to provide mixed-signal capability: Viewlogic's Viewsim digital simulator with Microsim's P-Spice analog system.

Where analog simulation helps automate the task of building analog circuits, logic synthesis improves on digital circuits already developed and creates circuits from high-level functional descrip-

*VHDL is omnipresent:  
in the wake of  
Mentor Graphics'  
announcement of  
support, every  
CAE tool vendor is  
doing likewise*

tions. From the time logic synthesis hit the market at last year's Design Automation Conference, the major CAE suppliers and ASIC vendors have been jockeying to provide some form of support for it.

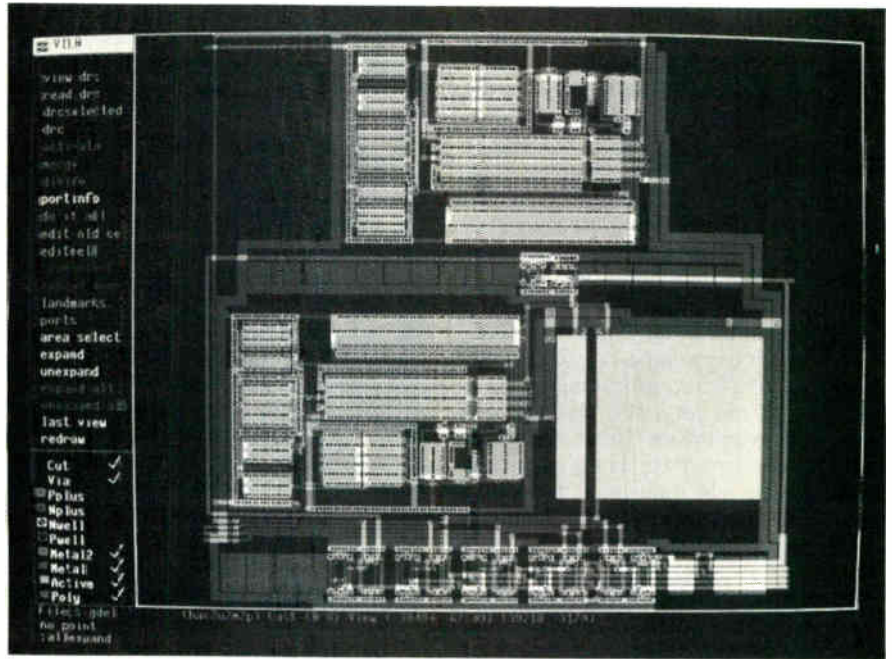
Synopsys is so far leading the pack in this market, followed closely by Trimeter Technologies Corp., the Pittsburgh company being bought by Mentor, and Silc Technologies Inc. of Burlington, Mass. A more recent entry is Silicon Compiler Systems. Though its synthesizer was announced ahead of the rest [*Electronics*, April 30, 1987, p. 54], the firm only recently began selling its tools individually.

Like these four companies, VLSI Technology Inc. of San Jose also has a logic-synthesis product [*Electronics*, Feb. 5, 1988, p. 83] that it has souped up for introduction at the conference. With their newest versions, these firms are all addressing weaknesses in their first-generation tools. Synopsys, for example, has added to its Design Compiler the ability to create hierarchies by splitting the design into elements that can be optimized individually. Each block can be optimized for different criteria, after which the entire structure can be flattened and optimized as a whole, if the designer chooses.

**BIG BLOCKS.** Silicon Compiler Systems and Silc are also offering expanded hierarchical design support. Jeffrey Fox, vice president of engineering at Silc, says designers using SilcSyn can now input all the big blocks of a large design and synthesize the glue logic around them. Silicon Compiler Systems provides this same proficiency, but with the additional ability to use soft cells. With the firm's Autologic, a designer can call modules—arithmetic logic units, counter-barrel shifters, and so on—from a library and configure them for an application, says Peter Rip, vice president of product marketing. The logic synthesizer will produce the logic to tie them together.

VLSI Technology, meanwhile, is working on a behavioral synthesizer that will take this concept one step further. With it, the designer will be able to specify the behavior of a complex design such as a controller, which contains a data path, some read-only and random-access memory, and a state machine for control. "What will set us apart is that we will be able to synthesize behavioral descriptions of complex blocks such as data paths as well as the state machine we currently do," says Chris Kingsley, software project leader. The synthesizer, due out next year, will automatically create the logic to tie RAM, ROM, a state machine, and a data path together, says Michael O'Brien, product marketing manager.

Besides improving the power of the synthesizer in handling more complex de-



**Seattle Silicon's ChipCrafter/MAX handles the analog portion of this ADC automatically.**

signs, vendors have enhanced these tools for speed. Synopsys, for one, has improved its algorithms for this reason. On a benchmark comparing version 1.0, which shipped in September 1988, with the new version 1.1, the average speed boost was 25% on 25 different circuits, says Robert Dahlberg, the firm's marketing manager.

One of the strengths of Silicon Compiler Systems' Autologic tool is its ability to map complex structures such as exclusive OR and AND/OR INVERT into a design being optimized, says Hal Allis, vice president and general manager of the company's IC CAD division. Another advantage is that Autologic uses the simulated annealing algorithm. With this approach, after a design has been optimized to some minimum result, the algorithm begins replacing an optimum circuit with a less than optimum one to see if the change creates opportunities to make circuit substitutions elsewhere that result in a better overall design. The process repeats until all possible alternatives are exhausted. The result will be a more optimal design, Allis says.

Another capability that logic synthesis suppliers are starting to add is improved library support. For a synthesizer to create an efficient circuit design in terms of gate count and performance, it must have access to the gate-array or standard-cell libraries in which the circuit will be implemented. This accommodation was an obstacle many ASIC suppliers were not willing to hurdle without a base of designers

wanting to make use of these libraries.

Now that the synthesis tools have been available for nearly a year, though, the demand exists—and ASIC vendors are leaping to meet it. NCR was one of the first to jump on board, providing library support for Silc's SilcSyn. Recently LSI Logic Corp. of Milpitas, Calif., announced library support for the Synopsys synthesizer. Synthesis vendors are all rushing to get similar support from the ASIC mavens. To ease the burden of creating these libraries, the vendors have developed tools to automate the process. Synopsys offers the Library Compiler, Silc its Builder, and Trimeter its Knowledge Consultant. These are tools the synthesizer suppliers themselves used to build libraries based on data-book information from ASIC suppliers.

**ASIC FACTS.** At the Design Automation Conference, every synthesis vendor will announce one or more agreements with ASIC suppliers. The benefits work both ways: synthesizers help sell high-density ASICs, says Dahlberg of Synopsys. Synthesis is the only way to quickly capture the large amounts of logic needed to fill these high-density devices.

Finally, synthesis tools, too, are responding to the need to support high-level description languages. With these languages, a designer can describe the behavior of a circuit and simulate its operation at the behavioral level. Once the design is debugged, a synthesizer automatically produces a gate-level implementation, a task the designer did by hand up



to now. If the long-term trend is toward VHDL, in the near term most designs are being synthesized in Verilog or the native HDL of the synthesizer.

Silc was the first to offer this capability, incorporating its proprietary DDL (design-description language) in SilcSyn. This means the designer can optimize the circuit at the functional description level before it is turned into gates.

For its part, Synopsys is using a subset of Gateway's Verilog, says Aart de Geus, senior vice president of engineering and the company's founder. Of those buying synthesis tools from Synopsys, 70% are buying or adding the HDL compiler with the design compiler, he says. The Verilog customer base is skilled in using high-level description and willing to design by writing program code rather than by creating schematics, he says. VLSI Technology also offers HDL capability in that its Logic Synthesizer accepts state-description inputs, which it converts into an optimized state machine. One recent improvement is the ability to accept a graphical bubble-diagram input.

**THE BACK END.** All these front-end developments result in tools that are performing more functions automatically, thereby allowing designers to create more complex designs. There is a commensurate development in back-end tools, with the aim of helping layout designers build chips with 100,000 to 1 million transistors and to perform automatic layout of analog functions.

Valid Logic Systems Inc. of San Jose, for instance, has just unveiled version 2.0 of its block place-and-route tools, Compose. One new capability is automatic mixed block and cell placement and routing. Up to now, there was one layout tool to perform standard-cell place and route and another to place and route large blocks. This meant that in a design with several large blocks, RAM, ROM, programmable logic array, data path, and state machine, the standard-cell logic to tie these blocks together had to be collected into a large block using a standard-cell place-and-route tool. Then this block was transferred to the block place-and-route tool for final layout.

With the new version, "you can place and route standard cells and blocks at the same level," says Donna Rigali, product marketing manager. The effect is to sprinkle standard cells among the larger blocks of the design. The capability minimizes routing, because individual stan-

dard cells can be better placed in relation to the large block each connects with.

Seattle Silicon Corp., an ASIC supplier in Seattle, introduced the same capability in its ChipCrafter APAR+ tool early last year [*Electronics*, Feb. 18, 1988, p. 101]. Seattle Silicon provides the tools to its ASIC customers while Valid, a CAE-equipment supplier, sells the tool as part of its tool-kit offering.

Mentor Graphics has just introduced this capability, too, on a tool called CellStation/Blocks. Besides laying out standard cells and large blocks at the same level, Mentor adds over-the-cell routing capability. Instead of routing in the channels around large blocks or rows of stan-

route is trimmed significantly.

Layout designers are beginning to demand one other place-and-route capability: mixed analog and digital layout. "One way designers can differentiate their product is to put analog on their digital ASIC designs," says Harrison. However, because analog circuit layout has different requirements than digital, ASIC place-and-route tools have not been well suited to handling both on the same piece of silicon. Now CAD suppliers are enhancing their tools to accommodate these differing requirements.

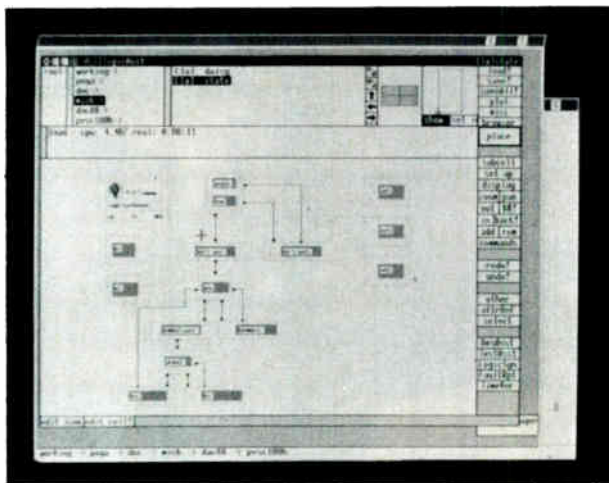
Seattle Silicon, for example, introduced in May a tool called Analog/APAR+, a fully automatic physical design tool that places and routes digital and analog components on the same chip. It automatically separates sensitive analog circuits from noisy digital logic.

**NOISE IMMUNITY.** The tool combines analog circuits into one or more big blocks. It differentiates between digital, neutral, high-sensitivity, and low-sensitivity networks, separates them to control crosstalk, and minimizes net lengths for high-sensitivity analog networks. In addition, it automatically determines the correct size of power and ground rails needed by the analog circuits. Autoroute from Silicon Compiler Systems takes a similar tack. "Its major new feature is mixed analog and digital design, with complete noise immunity and shielding," says Allis. "The tool achieves 100% complete route of combined analog

and digital blocks, and completely automatic routing of power and ground."

Handling analog with digital is also inherent in the Mentor CellStation/Blocks, says Harrison. The tool can abut groups of standard cells together by type. Hence, it knows not to abut a digital cell with an analog one. Then too, CellStation/Blocks can route power and ground automatically, and allows an unlimited number and mix of sizes and width for signal, power, and ground. Previous-generation systems tended, by contrast, to treat power and ground differently from signal, and limited the number and size of power and ground buses.

Such powerful new tools will go a long way toward giving designers the wherewithal to create complex standard and ASIC chips while turning their designs around in days rather than weeks and months. This year's Design Automation Conference promises to be a showcase for many of the products that are making this possible. □



### VLSI Technologies' Logic Synthesizer can now accept graphical bubble diagrams.

dard cells, the tool uses unused routing resources to route over the cell. Existing over-the-cell routers force the designer to identify pins on the large blocks where feedthrough paths exist across the cell, says Bob Harrison, product manager at Mentor. "As cells get more dense there is less unused routing resource," he says, "and this means the designer has to spend more time figuring out paths for the router to use."

CellStation/Blocks eliminates this chore. Harrison says the key to the tool's capability is that it imports the polygon layout data of each large block and determines the unused routing resources automatically. Earlier tools, by contrast, do not have access to the data-base description of the large blocks, he says. Combining the ability to route standard cells and blocks at the same level with the ability to route over the cell, Mentor claims to shrink composite designs as much as 25%. Moreover, because the tool is completely automatic, the time to perform place and



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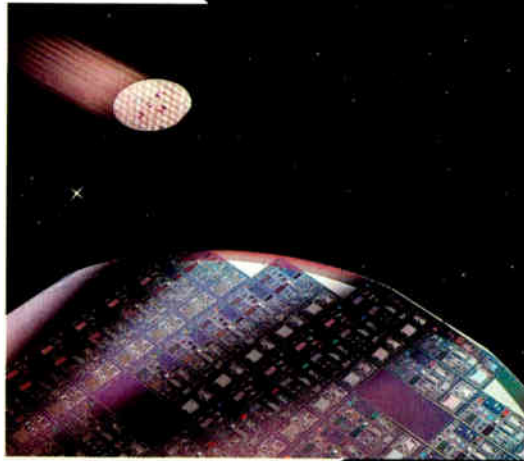


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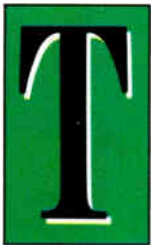
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# IKOS ENERGIZES MIXED-MODE SIMULATION



he increasing use of high-level hardware description languages in automated circuit design is putting a big strain on mixed-mode simulation. The problem is that "it's

not practical to simulate a system with behavioral models of VLSI circuits along with a 10,000-gate array, some TTL, and programmable array logic on a work station," says William Loesch, president of Ikos Systems Inc. in Sunnyvale, Calif.

Loesch says it takes 10 to 100 times more processing power to simulate the detailed gate level than to simulate the few powerful blocks of behavioral description written in an HDL. "You're lucky to [be able to] simulate 100 instruction cycles, when hundreds of thousands of cycles are required to simulate the operation of the circuit in the real world," he says.

Ikos Systems has a solution to this problem—the Ikos 2800 and 2900 mixed-level hardware simulators. The 2800 can simulate designs with 320,000 gates, and the 2900 can handle designs of up to 1.2 million gates. They feature special-purpose hardware to couple behavioral models running on a 32-bit work station into the hardware gate-level simulator.

Ikos is counting on its new product line, along with steadily increasing sales of its existing offerings, to give it the impetus to emerge as a major force in the logic simulation market, despite a troublesome lawsuit over alleged patent infringements on basic acceleration tech-

*When ASIC designs  
break the 10,000-gate  
barrier, mixed-level  
hardware simulators  
blow their software  
counterparts out  
of the water*

nology being waged with archrival Zycad Corp. of Menlo Park, Calif. Currently, the legal fighting continues, with each company suing the other.

The logic simulation market is primed for rapid growth, according to the Technology Research Group, a Boston-based market-research firm. TRG says that in 1988, some 5,600 of 37,300 application-specific IC design starts contained more than 10,000 gates. This year, nearly 10,000 of 52,900 will hit that number, and by 1990, about 18,400 of the 73,300 ASIC design starts will contain more than 10,000 gates. TRG says that the logic simulation market was worth \$207 million in 1988 and will reach \$291 million this year. It will grow at a healthy 29% rate to \$587 million by 1992.

A prototype of Ikos's new line will be shown at this month's Design Automation

Conference in Las Vegas (see p. 78), although it won't fully handle VHDL, the Pentagon's VHSIC Hardware Description Language, which is fast becoming a standard for Defense Department and other federal government projects. Beta shipments will begin late in the third quarter. Excluding the VHDL interface, the price of the basic 2800 system, which should begin shipping in 1990, will be about \$95,000.

Ikos's new hardware simulator connects to Sun Microsystems Inc. or Apollo Computer Inc. platforms linked to other work stations over a network. Support for other platforms is planned. The link between the work station and simulator is a 10-Mbit/s data path, double that of the first-generation Ikos hardware simulator. The speedier link cuts the time required to move large design files into and out of the simulator.

On the network, the simulator acts as a shared server, through which users can work with the Ikos simulation software to develop a design. Once the circuit is ready for simulation, it is loaded into the hardware simulator server for execution.

Robert Smith, director of marketing at Ikos, claims the new simulator provides equal or better performance than competing software solutions on purely behavioral simulation runs. For designs with both gate-level and behavioral-level simulation, however, the product is two to three orders of magnitude faster than software-based solutions. Indeed, "popular software simulators are beginning to run out of gas on designs with tens of thousands of gates," says Victoria Hinder, director of research at TRG. Smith also claims the system is faster than competitive hardware accelerators.

The performance advantage that Ikos claims over mixed-level software simulators stems from its system's ability to accelerate the gate-level portion and some of the behavioral processes in special-purpose hardware. Mixed-level software simulators must run both behavioral- and gate-level simulation on a work station. The hardware simulator executes the simulation algorithms at high speed, whereas the work station executes the simulation algorithms as it does any other program. An alternative approach is to run the behavioral portion of the simulation on the work station and the logic simulation on a hardware accelerator. The drawback to this approach is the time required to convert the symbolic data used by the behavioral simulator into binary

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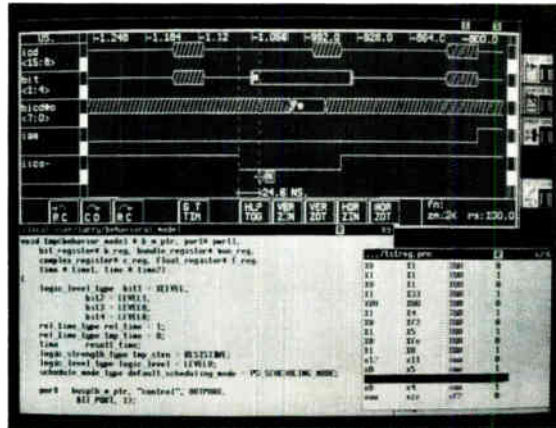


data that the logic simulator can accept, and vice versa.

On the new Ikos hardware simulator, behavioral processes and models run on work stations located on the network. The behavioral kernel, which controls the interaction between behavioral- and gate-level simulation, is implemented in special-purpose hardware. Because gate and behavioral simulations are integrated, they can pass events between themselves, synchronize timing, and execute a thousand times faster than a mixed-level software simulator, Smith claims.

The Ikos simulator includes a cluster controller, a piece of software that runs on the work station. It provides the user interface and handles all the behavioral processes; it executes the HDL descriptions provided by the system designer. It also uses external models from third-party suppliers like Logic Automation in Beaverton, Ore., and Quadtree in Sunnyvale, as well as hardware models from Logic Modeling Systems Inc. in San Jose, Calif. In executing the HDL descriptions, the cluster controller accepts VHDL, C, or other HDL inputs, and translates them into C++ for execution.

In a system simulation, a behavioral model produces a high-level description, such as unsigned integers. If the model is connected to a function implemented as a



**Ikos has a hardware solution to mixed-level simulation in the new 2800 and 2900 systems.**

gate-level description in the larger system design, the kernel converts the behavioral results—the integer in this example—into binary data that the gate-level simulator can use, and vice versa.

The kernel also performs four other functions. First, it suspends and resumes behavioral tasks that interact with gate-level operations. Second, it manages the queue of events occurring in the mixed-level simulator. Third, it automatically advances time in the event queue if no logical operations are scheduled to occur in the queue. Most gate simulators, in contrast, perform a circuit evaluation even if nothing is occurring at an increment. Finally, the kernel performs event

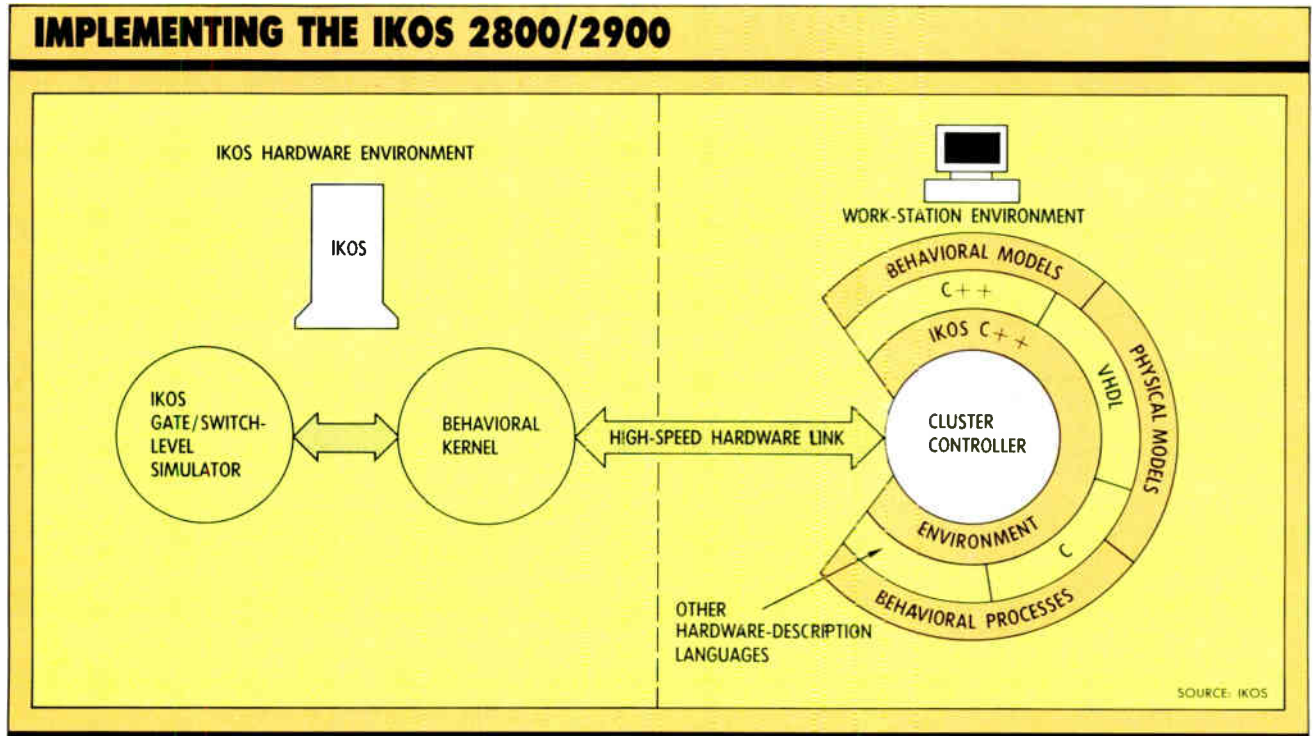
filtering, a behavioral process that prevents spurious signals created by the gate-level logic from triggering an unnecessary behavioral simulation.

Ikos, founded in 1984, shipped its first system at the end of 1986. In 1987 the company introduced the Ikos 1900 system. Ikos's first-generation products, the Ikos 800 and 1900, operate on four different platforms: Apollo, Sun, Intergraph, and the IBM Personal Computer AT. The company faces three types of competitors: CAD/CAE vendors, such as Daisy/Cadnetix and Teradyne EDA, that sell proprietary hardware simulators; hardware accelerator suppliers, such as Zycad; and independent software simulator suppliers, such as Cadat, HiLo, ataway Design Automation, and Mentor Graphics.

Ikos believes it has an edge over each of these competitors. "Although a hardware accelerator uses an existing simulator interface and library, it has to be tuned to a specific simulation environment," says Smith.

The hardware simulators rely on the host software simulator to provide simulation libraries, netlist extraction and preparation programs, stimulus entry programs, and output analysis programs. All these elements are integral to the Ikos hardware simulator. □

## IMPLEMENTING THE IKOS 2800/2900



**The behavioral kernel is special-purpose hardware that couples behavioral models running on a 32-bit work station into the hardware gate-level simulator.**

CES SHOWS OFF HIGH PRECISION

# NOW DIGITAL DOES IT ALL!



**T**

he sights and sounds of the Consumer Electronics Show, 1989 summer edition, are likely to be of higher definition and higher fidelity than ever before. Though most manufacturers were keeping their offerings under wraps until the show opens its June 3-6 run at the McCormick Center in Chicago, products incorporating a host of video and audio advances are set to be unveiled.

Indeed, the record number of advances on display this time around will amount to a digital revolution in home electronics. And since CES has traditionally served as a venue for manufacturers to gauge the market's reaction to new technologies, the industry clearly hopes to convince consumers to buy into a dizzying array of improved TVs, video cassette recorders, camcorders, compact-disk and digital-audio-tape players, and home-office electronics.

"In the near future, you're going to see electronics that are immensely flexible, that might be used as a stand-alone entertainment system but could also be integrated into a telephone system or a data-management system," says Robert Heiblim, vice president at Denon America Inc. in Parsippany, N. J.

While such integration may in fact be a few years away, this year's leading-edge introductions at CES are more versatile than ever. A new

## Digital technology pushes resolution and integration in audio and video products at this summer's Consumer Electronics Show

generation of audio components adds digital signal processing capability to create "surround sound" and other synthesized features. The video front features liquid-crystal-display TVs built around tiny active-matrix picture "tubes," improved-definition TVs that offer more than 400 lines of horizontal resolution, and camcorders exploiting 8-mm high-band technology for better performance.

Despite the wealth of new hardware at CES, the show is unlikely to bump up the curve in consumer electronics sales. "We've projected very conservative growth, certainly not the double-digit growth we became used to in the heyday of the VCR," says Tom Lauterback, vice president for communications at the Electronic Industries Association's Consumer Electronics Group in Washington. "I don't believe the VCR has pla-

By  
**Alexander  
Wolfe**





**Yamaha is introducing a \$799 CDV-1100 CD Video Combi player, which handles all audio and video optical-disk formats.**

teaved, but certainly its growth has slowed. But things that have been around for years, like color TV, continue to set records."

"I think the economy is definitely softening," says Jim Magid, senior adviser at Needham & Co. in New York. "On the other hand, the worldwide consumer electronics marketplace is relatively firm at this point in the cycle. In other words, if we were going into a consumer slowdown, normally there would be excessive inventories of TVs and VCRs. That's not happening—in fact, there are still relative shortages in those areas. So it's a healthy environment, even if the economy is slowing down."

**RECORD SALES.** "Last year saw record sales of color TVs, and this year will also see record sales," offers David Lachenbruch, editorial director of the industry publication *TV Digest*. "People are replacing their existing sets, and they're gradually buying better ones."

Several manufacturers are offering improved-definition TVs—the best that consumers can buy today. Unlike high-definition TV, IDTV is essentially a collection of receiver-side enhancements; an IDTV set receives a conventional NTSC broadcast signal. Chief among IDTV's improvements is that the signal is painted on the screen using 525 lines of noninterlaced scanning, eliminating visible scanning lines and improving vertical resolution by up to 40%.

The IDTV entry from New York-based Sony Corp. of America is the 27-in. KV27FX10. Besides its double-scan noninterlaced design, it boasts a digital frame memory to reproduce colors more accurately and to block out interference not related to the broadcast signal. Blurring between blacks and whites is eliminated with a digital vertical control enhancer. Motion-detection and -adaptation circuitry reduces smearing during motion scenes by switching to line doubling—repeating an adjacent horizontal line—when motion is detected. The set, which

will ship immediately, will retail for \$4,000.

Panasonic Co. is unveiling the biggest IDTV entrant. The Secaucus, N. J., company's 51-in. direct-view Prism PTL-5199S IDTV promises more than 450 lines of horizontal resolution. It also employs such innovations as extended digital signal processing, a line-locking three-dimensional filter to overcome dot crawl and cross-colors, motion-detection circuitry and a motion-adaptive frame comb filter, and digital noise reduction. The set will be available in September; its price hasn't been announced.

North American Philips Co. in New York will

**A Sony GV-8 hand-held TV/VCR combination features an LCD color screen and uses 8-mm videotape cartridges.**



introduce a major new TV line, according to spokesman Patrick Wilson. Speculation centers on additions to the company's IDTV line, which currently includes the 27-in. model 27J245 and 31-in. 32J460. Philips says it can stretch resolution to 480 horizontal lines. The company's IDTVs use a patented median filter algorithm, said to overcome the distortion common in other double-scan systems.

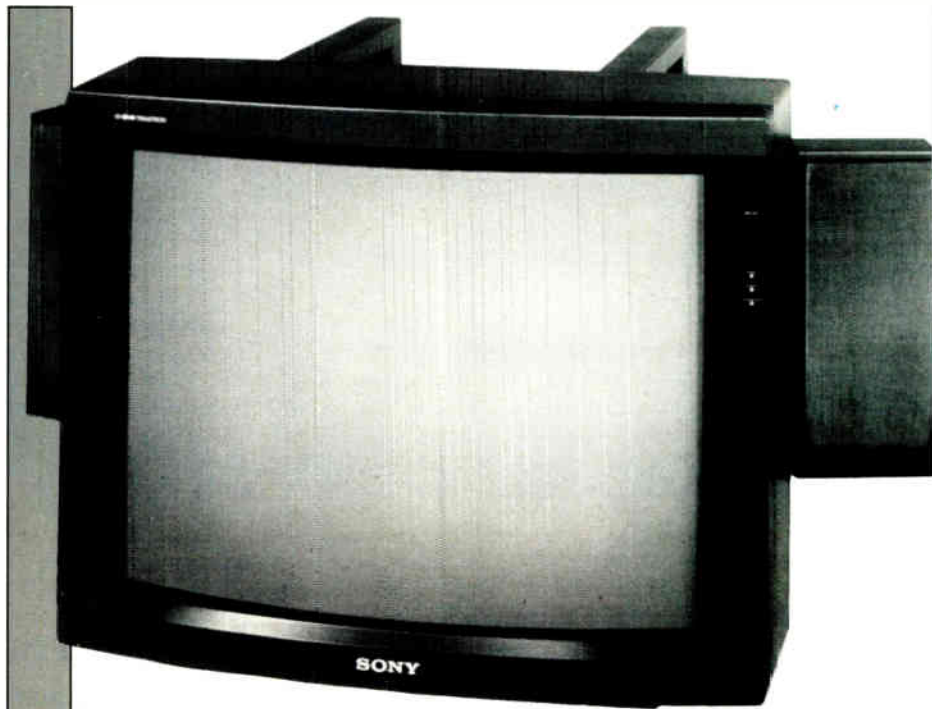
**HIGH GROUND.** Turning to conventional receivers, RCA Corp. will likely stake out the high ground in standard-scanning sets. "We're going to see a super set from RCA, featuring a new chassis with a new tube that is supposed to be brighter and higher resolution," says *TV Digest's* Lachenbruch. A version of that chassis will probably be offered on both of RCA's premier color lines, Dimensia and Colortrak 2000. However, Lachenbruch adds, "I think RCA will de-emphasize Dimensia because it hasn't caught on."

The new color picture tube featured in the RCA chassis will probably be its newly announced 27-in. cathode-ray tube, called VHP, for very high performance. Although not a technological breakthrough, the tube is viewed as an effort to set a new engineering standard and to compete with Japanese-developed CRTs. Following the introduction of this big tube, smaller versions are expected. Indeed, these are a virtual certainty, because all tubes 19 in. or larger used in sets manufactured in North America are made in the U. S.—it's currently too expensive to import those tubes from manufacturers in the Far East.

From Japan, Toshiba Corp. is expected to show off its new 32-in. color CRT. The tube, though again not a breakthrough product, will find ready demand in the new generation of larger—greater than 25-in.—direct-view TV sets. Because of the tremendous capital investment required to engineer a new tube, such introductions highlight the high hopes of manufacturers in the potential of large-format direct-view sets.

Zenith Electronics Corp., a TV powerhouse that doesn't usually exhibit at CES, remains mum about introductions. But the Glenview, Ill., company has made a big splash with its projection sets that incorporate a sound system designed by Bose, the Framingham, Mass., high-fidelity house. Its late-model, two-piece projection set is based on an advanced digital chassis. Refinements of the digital chassis, as well as a number of new projection sets, are apparently being readied.

Interesting variations on the conventional picture tube are also developing apace. A very thin, flat TV set using a new type of tube has been shown to the press by Panasonic in Japan; however,



**Sony's 27-in. IDTV entry, the KV27FX10, offers double-scan, noninterlaced design and a digital frame memory to reproduce colors accurately and block interference.**

Panasonic won't comment on its release in the U. S.

Sharp Electronics Corp. of Mahwah, N. J., will also be introducing new LCD TVs. Sharp, which unveiled its LCD projection TV at the Winter CES in January, says it will show off several new models this time around.

The basic design of Sharp's projection set, which has a horizontal resolution of about 300 lines and will sell for roughly \$4,000, uses three 3-in. LCD panels and a single lens in place of a conventional projection set's three CRTs and three lenses. "There are a number of advantages, the first of which is you no longer have to worry about convergence," says Steve Search, Sharp's national marketing manager for video. "Second, the unit is relatively compact and lightweight, in the neighborhood of 25 lbs. It allows the flexibility of putting a picture on the wall with a screen size as small as 20 in. or as large as 200 in., because the unit will have a built-in zoom lens."

The top-of-the-line model with projection unit and a 100-in. screen will retail for \$5,000 to \$6,000, according to Search. Future introductions may include a complete entertainment center that supplements the basic projection unit with a wall system containing an electric screen and a Super-VHS VCR.

In these new LCDs, based on active-matrix technology, active elements consist-

ing of thin-film transistors are placed next to each LCD picture element. Improved picture quality results from the fact that the transistors allow the picture elements to be addressed without crosstalk between elements.

**WHITHER HDTV?** While the promise—and the hype—of HDTV has commanded much industry attention [*Electronics*, March 1989, p. 70], HDTVs won't move from the showroom floor to consumers' living rooms for quite a while. "Although HDTV has sparked everyone's curiosity, we're a few years away from delivery of the first sets," says EIA's Lauterback. "It's going to be even longer until those sets are popularly priced, so you've got a real lag time built in."

At Summer CES, a host of manufacturers will reprise their Winter CES HDTV product displays, none of which are yet marketed to U. S. consumers. This select group should include Barco Electronics, Boffi Vidikron, Fisher, Philips, and Sony.

"HDTV is something that people have to be educated to," says *TV Digest's* Lachenbruch. "Bear in mind that it was 13 years after color was approved by the FCC that the industry sold its first million sets, and color has much more impact than HDTV."

In VCRs, the proliferation of new formats will continue as manufacturers search for a winner to entice consumers into a more expensive format that com-



bins higher-resolution video with higher profit margins. "In VCRs we're going to see all sorts of more sophisticated systems in the hopes that one or more of them will catch on," says Lachenbruch.

Standard VHS and Beta recorders offer some 250 lines of horizontal resolution. Because Super-VHS records the luminance signal in the 5.4-to-7.0-MHz band, as compared with the 3.4-to-4.4-MHz band of standard VHS, it achieves about 400 lines of horizontal resolution. In the compact formats, VHS-C cassettes offer performance equivalent to that of the standard VHS format. S-VHS-C, the down-size version of Super-VHS, matches its 400-line resolution specification.

In their quest for clout with the consumer, manufacturers such as Canon, Fisher, NEC, Panasonic, Ricoh, Sanyo, and Sharp are working to eliminate the need for an adapter between VCRs and VHS-C cassettes, the smaller-format VHS tape spawned by the camcorder. At least one company is expected to show a VHS VCR that accepts VHS-C cassettes—without an adapter.

Just as significant, JVC Corp. is increasing the running times of VHS-C and S-VHS-C tapes from 20 to 30 minutes at the fast speed and from 60 to 90 minutes at the slow speed to make the tapes more attractive to consumers. Indeed, such smaller formats are taking on increasing importance. "It's possible that JVC or Matsushita will bring out a small VHS-C video player comparable to the Sony Video Watchman," predicts Needham & Co.'s Magid.

In the regular VHS VCRs that dominate the market and the higher-resolution Super-VHS VCRs, ease of use is becoming a marketing tool. As a result, more VCRs will offer easier programming by means of bar codes, like Panasonic's new PV-S4990. In some cases, bar-code programmers will be integrated with the VCR's remote-control unit.

In camcorders, while most consumers prefer VHS, the smaller-format high-band 8 mm is making the most news. This upgrade of the 8-mm videotape format, with 400 lines of horizontal resolution, offers performance equivalent to Super-VHS. At the Winter CES, high-band proved to be a major nonevent as expected product introductions—with the exception of a high-band deck displayed by Canon—didn't materialize. This time around, Sony is leading the push with its \$2,200 CCD-V99 Handycam; other manufacturers appear to be ready with lightweight models that will weigh in at less than 3 lbs.

Turning to the audio offerings, digital signal processing will be the most important emerging area at CES. DSP components do all their audio processing in the digital domain until it reaches the speakers, thus avoiding many of the amplitude, phase distortion, and imaging problems associated with analog circuitry. The built-in DSP stages in the new DSP amplifiers and preamps also will allow for the creation of audio "special effects." These stages will perform surround-sound or delay-mode processing for re-creating ambience, as well as digital dynamic-range compression, filtering, tone control, and equalization.

"There are tremendous possibilities for the future if this type of technology is combined with more expensive memory circuits," says Mark Finer, director of Communications Research Inc., a Pittsburgh consulting firm. "You can have at the touch of a button all the digital parameters preset to fit your favorite musical genre or environmental mode, whether it be in the home, in the car, or portable."

X911DG integrated amplifier with four digital inputs and digital-to-analog conversion at user-selected sampling frequencies. Other manufacturers, according to Finer, should be introducing models with digital processing at CES.

Along with digital processing, integrated entertainment is becoming a watchword as the line between audio and video components begins to blur. One result: the lackluster videodisk may move into the limelight.

"Videodisk has been a sleeping business in the U. S. for the last 10 years," says Don Palmquist, president of Yamaha Electronics Corp. USA in Buena Park, Calif. "At the same time, it's been a big business in Japan, where every company makes a player. Those companies are now entering the U. S. market." U. S. participants will include Sony, which has already introduced a player, as well as Hitachi, Panasonic, and Sharp, which are expected to introduce products soon.



**In the high-band camcorder arena, Sony's 2.5-lb CCD-V99 Handycam goes for \$2,200. The high-band 8-mm format raises horizontal resolution to 400 lines.**

At the Winter CES, Sony demonstrated a production DSP component, the TA-V925E preamp, which is currently available in Japan. An American model is said to be slated for introduction at or shortly after the Chicago show, though the preamp was noticeably absent from Sony's pre-CES announcements. Denon is also testing the digital waters and will be showing an all-digital preamp featuring digital equalization and volume control, as well as surround-sound processing. The preamp will be displayed at the show and shipped in the fall, according to the company.

Yamaha has also begun to incorporate this technology in the form of digital de-emphasis and surround-sound circuitry in selected preamps and amps. Sansui Electric Co. is checking in with the AU-

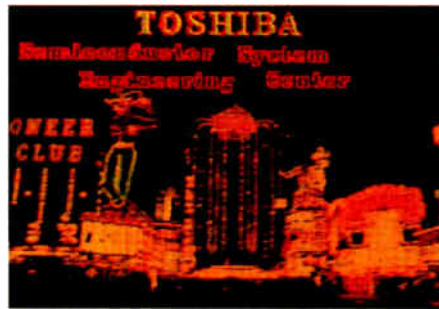
Today, the format is driven not by the conventional 12-in. video platter, which comes in either CLV or CAL formats, or the alternative 8-in. version. Rather, the 5-in. CD video (CDV) that emerged as a takeoff on the audio CD has pumped new life into this play-only medium.

Yet manufacturers must contend with the full range of video formats if they are to curb customer confusion over software. This lies behind Yamaha's CES introduction of its \$799 CDV-1100 CD Video Combi player; it handles all audio and video optical-disk formats, including 3-in. audio singles, 5-in. audio-only compact disks, 5-in. CD videos, 8-in. video disks, and 12-in. CLV and CAL platters. Philips, too, will be showing off its new CDV 488 all-format videodisk player, which retails for \$1,399.

"The problem has been consumer



Large-screen LED video displays



Combined text/graphic displays



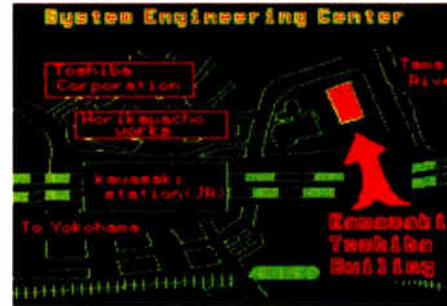
Computer-generated displays



Advertising and promotional displays



Arrival and departure boards



News and information displays

# LED GRAPHICS: A NEW WINDOW ON THE WORLD



Toshiba, the first name in LED modules, opens a new window on graphic display media with the latest breakthrough in LED technology.

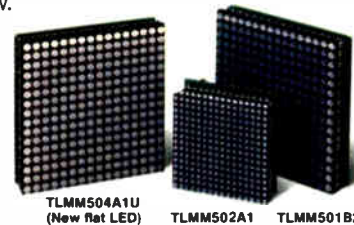
As easy to use as conventional CRT displays, Toshiba's new LED dot-matrix modules provide clear, colourful display of letters and graphics for the coming generation of LED televisions.

Each module features an advanced gate array for interfacing with video equipment and personal computers. And with versatile capabilities such as superimposition and stop motion, these modules can handle virtually any computer-generated graphic display.

Toshiba LED modules also boast a powerful, high-speed 20 MHz input clock, and 16-gradient control for improved colour contrast. In addition, we've successfully developed a new flat LED which provides a clear image from any angle of view.

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awareness regarding the distribution of software," says Palmquist. The VCR market has leveled off, he says, and consumers are ready to look at something new. "We still don't expect the market to explode in 1989, but we're looking at 150,000 units this year, he says. "And in 1990, there will be a quadrupling of sales as more manufacturers enter the business."

In the compact-disk market, sales have taken off. Today, CD players are estimated to be in 10% to 15% of U. S. homes. As for software, according to the Recording Industry Association of America, 151.3 million CDs were shipped in 1988 at a retail value of \$2.10 billion.

At CES, audio CD hardware manufacturers have adopted a trickle-down approach to the technology, packing more sophisticated features in lower-priced players. Both Denon and Yamaha, for example, are introducing players with 20-bit digital-to-analog conversion that retail from under \$400. NEC, Pioneer, Sansui, and Sony also have new products, many boasting the much-vaunted oversampling technology, which reads a CD's digital data at more than 40,000 times per second and applies sophisticated error detection to ensure superaccurate music reproduction.

Spurred by the new players, manufacturers are looking forward to even headier growth. "A 30% to 40% penetration in the audio CD category alone is easy to see," says Denon's Heiblim. "But if we carry forward a combination of audio, video, and data processing that the system allows, then we can get much higher penetration."

**IN FLUX.** The technology for that combination hasn't been completed. CDV enjoys the advantage of the current availability of players. Another possibility, compact-disk interactive (CDI), places limited-motion video, sound, and software on a 5¼-in. disk. As a result, CDI players can be connected to a TV to play back home-shopping catalogs, encyclopedias, or educational courseware. Such applications were highly touted when CDI was first announced by Sony and Philips in 1986. It now appears that CDI will loom largest in the computer marketplace.

In the home, some of CDI's thunder is being stolen by an attractive alternative: Digital Video Interactive, a still-developing technology first announced to the public in March 1987. Developed at the David Sarnoff Research Center in Princeton, N.J., DVI uses digital data compression to pack 72 minutes of full-motion video at 30 frames/s onto a platter the size of

a standard CD. This video is decompressed in real time during playback to create pictures on the screen. DVI disks also can store various combinations of motion video, still video, audio, and text; DVI packs up to an hour of full-motion video on a 5¼-in. disk.

"DVI holds a lot of promise because it's backward compatible," says Heiblim. "We can have a single player that plays an audio disk, a full-motion audio/video disk, a data disk, and is interactive. That's an attractive kind of product. And since we may also be able to make a recorder

there seems finally to be a regular dialogue with hardware and music label companies sitting down to discuss the ramifications of the technology. Hopefully, there will soon be some common understanding, not just about digital audio tape, but about all recordable digital media that could emerge in the future."

At the heart of the dispute is the position of the Recording Industry Association of America that DAT recorders could be used for widespread unauthorized copying of prerecorded records, cassettes, and CDs. As a result, DAT hardware in the U. S. is sold mostly on the gray market [*Electronics*, February 1989, p. 60]. DAT decks from 13 major vendors, including the likes of JVC, Panasonic, Sharp, and Sony, are being sold here through DAT/USA International of Trenton, N. J. Over the counter, the first U. S. entrant is Nakamichi. Its \$10,000 Model 1000 DAT recorder will be on view at CES.

In other CES categories, the technology may be less lofty but not the sales. Coming on as strong as ever is what has been dubbed "edutainment," led by the Nintendo game computer, along with game software for that and other machines from Apple Computer Inc.—mostly the IIe series—Commodore, and even IBM Corp. PCs and compatibles.

Also viewed as a fast-growing area of the CES marketplace are "pocket smarts." This category of hand-held electronics products encompasses everything from pocket video games with LCD screens to traveler's dictionaries, and, most notably, the daily diaries such as Sharp's Wizard electronic organizer and Casio's SF-2000 Digital Diary.

The home-office boom is still on, as is evident at CES. A host of facsimile machines, personal copiers, answering machines, and multiline telephones will be on display. Indeed, the year's hottest product probably falls in this category, although it won't be ready in time for CES.

The biggest consumer electronics product of the year: the 5-lb "box of candy"-sized, personal, portable, battery-operated computer, predicts Needham & Co. analyst Magid. Companies including Zenith Data Systems are expected by the end of the summer to introduce full-featured portables with only moderate compromises compared with today's desktop models. "There will be over a million of these machines sold within 18 months [of introduction]," Magid says. "This will become the personal home computer in the U. S., not Nintendo." □



**The Sharp VC-V540 portable TV and VCR combination boasts a 4-in. color LCD screen.**

that either plays back prepressed read-only disks or records them, that's even more attractive."

Indeed, recordable compact disks are already available behind closed doors. At the Winter CES, Japanese manufacturer Taiyo Yuden became the first company to show—in a hush-hush private demo—a prototype of a recordable compact disk. But the company has said it won't sell the product on the consumer market until copyright issues are resolved.

Such copyright issues are at the center of the digital-audio-tape controversy. At CES, DAT should be a leading display. Instead, manufacturers are adopting a furtive tone. That's because DAT has become as much a political issue as a technical one. "The politics of DAT are still at a very, very difficult stage," says Finer of Communications Research. "However,

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CXX5863M	8K x 8	25/30/35	SOP 450 mil
CXX5863J	8K x 8	25/30/35	SOJ 300 mil
CXX5464AP	16K x 4	25/30/35	DIP 300 mil
CXX5464AJ	16K x 4	25/30/35	SOJ 300 mil
CXX5465P*	16K x 4	25/30/35	DIP 300 mil
CXX5465J*	16K x 4	25/30/35	SOJ 300 mil
CXX5164P	64K x 1	25/30/35	DIP 300 mil
CXX5164J	64K x 1	25/30/35	SOJ 300 mil
CXX5971P	8K x 9	25/30/35	DIP 300 mil
CXX5971J	8K x 9	25/30/35	SOJ 300 mil
CXX58255AP	32K x 8	25/30	DIP 300 mil
CXX58255AJ	32K x 8	25/30	SOJ 300 mil
CXX58258P	32K x 8	35/45	DIP 600 mil
CXX58258SP	32K x 8	35/45	DIP 300 mil
CXX54256P	64K x 4	35/45/55	DIP 300 mil
CXX51256P	256K x 1	35/45/55	DIP 300 mil
*0/E			



BY TOBIAS NAEGELE

TEN YEARS  
AND \$1 BILLION LATER,  
WHAT DID WE GET FROM

# VHSIC?

**L**eonard Weisberg remembers it as if it were yesterday. A Soviet sonobuoy was recovered in the open sea in the winter of 1977 and shipped to the U. S. for a thorough investigation. The results were startling: inside the submarine detector was an array of integrated circuits that were direct copies of off-the-shelf chips made in the U. S. by Texas Instruments Inc. The Soviets were



"by pure imitation closing the technological gap" between U. S. and Soviet capability, Weisberg noted in a memo that would eventually reach then-Secretary of Defense Harold Brown. And they were doing it much faster than anyone thought possible. By early summer that memo came back to Weisberg, then the Pentagon's director of electronic and physical sciences, with a note from Brown scribbled in the margin: "What should we do about it?"

This was no ordinary challenge. The problem wasn't so much Soviet technology as it was the inability of the U. S. to integrate its own advanced technology into weapons systems. But with the newfound Soviet capability to copy U. S.-made commercial chips, the stakes were that much higher.

Weisberg's response was radical: spur the pace of innovation in the semiconductor industry, "take a giant leap forward that would leave the Soviets behind." He estimated that his plan would cost something under \$200 million and take five years. But the results would be worth it, he believed. America's weapons would be more sophisticated, its soldiers, sailors, and pilots better prepared, and its electronics industry more advanced.

Thus was VHSIC—the Very High Speed Integrated Circuits program—



**W**eisberg's only mistake was to let systems makers lead VHSIC

born. But the program, launched in 1979, quickly outgrew Weisberg's plan. Over the next 10 years, the Pentagon spent nearly \$1 billion—matched, some say, with at least twice that by industry—to advance the state of the art in military semiconductor technology from clunky 7.0- $\mu\text{m}$  bipolar parts to some of the most complex digital CMOS ICs ever built.

VHSIC helped bring on the computer-aided design revolution, accelerated the emergence of surface-mount packaging technology and on-chip testability, and even led the military to relax its restrictions on the use of nonmilitary-standard semiconductors in weapons systems.

In these ways, the VHSIC program—which ends this September—was a success. But VHSIC also had a dark side. Cost overruns, missed deadlines, and a seeming inability to get VHSIC parts into fielded military systems all took their toll. It even became fashionable to bash VHSIC as a symbol of everything that's wrong with military research and development.

In fact, the program had two major flaws: first, it failed to get top U. S. chip makers more closely involved in the effort, and second, because it wasn't tied closely enough to technology-insertion efforts from its inception, VHSIC technology has yet to flow from the R&D laboratories into fielded weapons systems.

"When VHSIC started, there wasn't a single weapons system in the U. S. arsenal with electronics as sophisticated as what you could find then in video games," says Gene Strull, vice president of technology at the Westinghouse Defense Electronics Center in Baltimore, one of six Phase 1 VHSIC contractors.

## JUST WHAT MAKES A CHIP VHSIC, ANYWAY?

**M**ick Blackledge stood up before a recent gathering of electronics executives in Alexandria, Va., and told them that without VHSIC, the space-based missile interceptors being developed for the Strategic Defense Initiative "wouldn't be possible." But Blackledge, the assistant director for interceptors and command control at SDI headquarters, wasn't referring to chips designed under the watchful eye of the VHSIC program. The chips he was talking about included Intel Corp.'s 80386, the highly successful commercial microprocessor found in many high-end personal computers.

Blackledge's statement is typical of what is now happening in the military community, where VHSIC—Very High Speed Integrated Circuits—has come to mean the same thing as VLSI—very large-scale integration. In addition to the prototype SDI weapons, such high-profile weapons systems as the Advanced Tactical Fighter—called "a VHSIC plane" by some—will include parts that can be called VHSIC-class, VHSIC-like, or VHSIC-equivalent, but not, in the strict-

est sense of the term VHSIC

In fact, it is one of the ironies of the VHSIC program that the companies now reporting the greatest marketing success with what they call VHSIC devices either weren't VHSIC contractors at all or lost their share of the program after Phase 1. By contrast, the three companies that won VHSIC's Phase 2 contracts—Honeywell, IBM, and TRW—all have struggled with either marketing the technology, developing it, or both.

Indeed, the success of VHSIC can probably best be determined not by the success of individual contractors demonstrating individual chips and brassboards, but by the level of independent investment in VHSIC-like efforts. At least nine companies that didn't win major VHSIC contracts mounted such initiatives on their own, and one—General Electric Co.'s Microelectronics Center—claims to have shipped more VHSIC-class devices than any of its competitors. GE officials say they've shipped over 150,000 CMOS VHSIC-class chips to Air Force contractors for use in some F-16 radars.

The parts, pin-for-pin replacements for high-power emitter-coupled logic chips, reduce the radar's power consumption by 76%, from 5,000 to 1,200 W.

To meet VHSIC standards, a chip must be designed with line rules of 1.25  $\mu\text{m}$  or less; have a functional throughput rate of at least  $5 \times 10^{11}$  gate-Hz/cm<sup>2</sup>; be produced using functional descriptions in the VHSIC Hardware Description Language (VHDL); include on-chip test features that cover 95% of the chip's logic gates; operate at a minimum clock speed of 25 MHz; and meet basic reliability, radiation-hardness, and temperature specs.

The standards are stiff. But when Intel reduced its original 1.5- $\mu\text{m}$  12-MHz 80386 to 1.0- $\mu\text{m}$  line widths and boosted its speed to 25 MHz, the company reports, military customers came running. For example, the chip is being inserted into one version of the ATF, and it is also at the heart of a Hughes Aircraft Co. design for the Light Exo-Atmospheric Projectile, a developmental space-based missile interceptor for SDI.

Texas Instruments Inc., which worked





IBM Corp.'s Manassas, Va., fab helped Big Blue beat fellow Phase 2 contractors Honeywell and TRW to every VHSIC milestone. But IBM has had a struggle in marketing the technology

"More information was coming into our radar systems, electronic warfare systems, and communications systems than could be number-crunched. We were trying to catch a moving train."

The moving train was commercial industry, and 10 years and \$950 million later, the military is barely getting on board. The snail's pace of military procurement,

coupled with the intransigence of military program managers afraid of risking their programs, schedules, budgets, and careers on what they consider "unproven" or "high-risk" technology, have conspired to keep VHSIC out of any volume applications. The biggest selling points for VHSIC—increased long-term reliability and decreased life-cycle maintenance

costs—were all but ignored by the people in charge of building and procuring military systems.

The original idea for managing the VHSIC program was to bring in a series of merchant semiconductor companies that would then sign up systems integrators and weapons builders as subcontractors, recalls Weisberg, now vice president

on bipolar technology in Phase 1, has adapted its Epic II commercial 0.8- $\mu$ m CMOS process for military products and is now producing a chip set based on the Air Force standard 1750A instruction-set architecture. Along with a set of peripheral devices and memory chips, the 1750A chip set will make up the mission computer in the Lockheed Corp. version of the ATF and the McDonnell Douglas-Bell version of the Army's LHX helicopter. The computer will ultimately tie together all the fighter's displays, sensors, and communications modules.

It's been tougher sledding for the three Phase 2 contractors. TRW Inc. had to scale back its Superchip effort, dropping the bipolar component and settling for a less-super chip than planned. IBM Corp. has had a hard time convincing the market that it is serious about selling VHSIC chips. And Honeywell Inc., probably the most active marketer of the three, never quite found the demand for its VHSIC devices that it had anticipated. "We ended up with excess capacity," says a Honeywell executive.

-T. N.

## WHERE TO GO FOR VHSIC-EQUIVALENT CHIPS

Company	VHSIC contractor?	Fabrication processes	Products
GE Microelectronics Center	No	1.25- $\mu$ m CMOS 1.25- $\mu$ m SOS	Standard cells and gate arrays
Harris Semiconductor	No	1.25- $\mu$ m CMOS	Standard cells
Honeywell Solid-State Electronics	Phases 1 & 2	1.25- $\mu$ m CMOS 0.5- $\mu$ m CMOS	Standard cells and gate arrays
Hughes Microelectronics Center	Phase 1	1.25- $\mu$ m CMOS 1.1/0.9- $\mu$ m HCMOS	Standard cells, gate arrays, and foundry
IBM Federal Systems Div.	Phases 1 & 2	1.0- $\mu$ m CMOS 0.5- $\mu$ m CMOS $\#$	Standard cells, gate arrays, and foundry
Intel	No	1.0- $\mu$ m CMOS	Standard products only
LSI Logic	No	1.0- $\mu$ m CMOS 1.2- $\mu$ m CMOS	Standard cells, gate arrays, and foundry
National Semiconductor	Phase 1 w/ Westinghouse	1.25- $\mu$ m CMOS	Standard cells, gate arrays, and foundry
Raytheon Microelectronics Center	No	1.25- $\mu$ m CMOS	Gate arrays, foundry
Texas Instruments	Phase 1	1.0- $\mu$ m CMOS 0.8- $\mu$ m CMOS	Standard cells, gate arrays, and standard products
TRW	Phases 1 & 2 w/ Motorola	1.0- $\mu$ m bipolar	Standard parts
Westinghouse Advanced Technology Labs	Phase 1	1.25- $\mu$ m CMOS	Gate arrays

$\#$  Uses 3.3-V instead of standard 5-V power supplies.

SOURCE: VHSIC PROGRAM OFFICE

## HOW ITAR HURT VHSIC

**P**entagon officials gave the hard sell to the House and Senate Armed Services Committee staffs when the Very High Speed Integrated Circuits program was getting started. VHSIC, they promised, was going to change the world. "It was presented as a golly-gee-whiz program," recalls one committee staffer. "It was going to be the biggest thing ever."

It is, of course, the nature of the way things are done in Washington that VHSIC may have been overpromised. After all, the House Armed Services Committee voted at first to "zero" the program. "That sent a shock wave around," the staffer says. The Department of Defense was very determined to get VHSIC through, but Congress was worried that if the new technology was indeed going to change the world, then VHSIC needed to be protected as a precious national resource. So when Congress gave VHSIC the green light, it was only after exacting an agreement from the Pentagon: VHSIC would be covered by ITAR—the International Traffic in Arms Regulations. To many, it was the single biggest blow the program took in its 10 years.

ITAR, the government's toughest set of export controls, requires companies dealing with classified information not only to keep it secret, but to have a formal plan drawn up for its protection. If one company wants to discuss the information with another, it must make sure that the second firm also has a formal plan for protecting the information.

Applying ITAR rules to VHSIC was unusual, because the regulations are normally used to make sure that already built military systems do not get into the hands of an adversary. By slapping a pure technology program such as VHSIC with the restrictions, critics say, the government stifled the kind of information exchanges that would have accelerated technological progress.

"ITAR inhibited the whole program," asserts Larry W. Sumney, president of the Semiconductor Research Corp. in Research Triangle Park, N. C. Sumney was the director of the VHSIC program from

1979 through May of 1982.

The first fallout from the ITAR decision was that the nation's universities all but dropped their support for VHSIC. "Up until that time, the university community had expressed strong interest in the long-term basic research projects that would be part of VHSIC's Phase 3," Sumney says. But "because of [ITAR], the Phase 3 university effort, which was supposed to be a \$40 million or \$70 million program, never happened the way it was supposed to."

The universities refused to go along with ITAR's restrictions, Sumney says. "They ran away from VHSIC as fast as

they could." The big problem for universities: their foreign graduate students, who could not be stopped from taking VHSIC know-how—or what could be perceived as VHSIC know-how—home to their native countries.

"ITAR put classified controls on a technology that was by nature unclassified," says Dick Urban, the third and final VHSIC program manager. He says ITAR hurt the program in more ways than just forcing universities to bypass the effort. ITAR also forced manufac-

turers to separate their VHSIC development staffs and their counterparts in commercial operations. Texas Instruments Inc., for example, kept the VHSIC program within its Defense Systems and Electronics Group, leaving out its Semiconductor Group. That cut down on interaction between design and process engineers on each side of the fence and may have retarded development, Urban says. Chip makers were worried that process or design techniques that weren't unique to VHSIC might fall under ITAR anyway, thereby hampering their ability to sell their wares.

Most experts also believe ITAR was at least partly responsible for the slow pace of VHSIC insertion. "In the grand scheme of things, it probably contributed to the problems we had in transitioning the technology," says E. D. "Sonny" Maynard Jr., who ran the VHSIC program office for six years. "It gave companies one more excuse not to use [VHSIC]." —T. N.

**'ITAR put  
classified  
controls  
on a technology  
that was  
by nature  
unclassified'**

of corporate research and engineering at Honeywell Inc. in Minneapolis.

But when Weisberg and Larry W. Sumney, who managed the VHSIC effort for its first three years, asked industry's opinion on the structure, "to my amazement, they proposed that the systems houses lead the project," Weisberg says. "They said this would guarantee that what was developed really would meet the military's needs."

Most of the VHSIC money went to in-house development efforts at captive military chip foundries. It was a mistake Weisberg says he hasn't lived down. "I think I blew it when I let the systems guys lead," he says. Chip makers would have marketed the technology more actively, he says, and that would have gotten it into fielded systems more quickly. What happened instead was that the military systems makers viewed VHSIC technology as a competitive weapon. They had an inherent conflict of interest: their only potential customers for chips were the same people they were fighting for lucrative weapons contracts.

**LOTS OF PROMISES.** IBM Corp., for example, which beat TRW Inc. and Honeywell Inc. to every major Phase 2 milestone, has been criticized for not aggressively marketing VHSIC. "They don't share anything," says one competitor. IBM insists, however, that while it hasn't seen any wild success yet, it is actively marketing chips, circuit boards, and design and foundry services. The company blames its troubles on the failures of competitors like TRW to meet their VHSIC goals. "There have been a lot of promises made about VHSIC that haven't been delivered on," says an IBM executive. "That hurts us because we can deliver."

So a big part of the government's investment, particularly what was spent on pilot lines and on individual chip designs, didn't pay off. "We didn't see the teaming that we wanted," says Sumney, now president of the Semiconductor Research Corp. in Research Triangle Park, N. C. "The barriers between companies just didn't let that happen."

From that point of view, "VHSIC was a miserable failure," says Bud Kaiser, manager of strategic marketing for General Electric Co.'s Microelectronics Center in Research Triangle Park. But from another viewpoint, he adds, it was a big success, since by investing in a few companies, the government reaped the rewards of its investment many times over.

Fear of being left behind drove GE and other major military systems houses to create their own VHSIC-like processes. "Look," Kaiser says, "it's difficult for a GE or an IBM to use a Honeywell chip set. If you're a major system house and



you're tied down to a competitor's chip set, you're going to be uncomfortable. You want to have your own."

In many ways, VHSIC's success hinged less on the companies that won government contracts than on the ones that worked on their own. As a direct result of their work, the military is now seeing a gradual blurring of the terms VLSI—for very large-scale integration—and VHSIC so that the latter is now used to mean any VLSI circuit being considered for a military application (see p. 98).

GE's Kaiser is probably right when he says that "the guys who won the contracts are in the catbird seat, because the government paid for their work" and that "they probably would have built those chip sets anyway." But how fast would they have done the work? And without VHSIC, how quickly would other companies have followed suit and pushed their chip technology development beyond the 1.0- $\mu$ m barrier?

**WHAT WENT RIGHT.** There are no definitive answers to those questions. But most experts agree that without VHSIC, semiconductor development in the U. S. wouldn't have progressed so quickly toward submicron geometries, even in the commercial world. As with Japan's early VLSI project, which served as further impetus to get VHSIC started, government funding and goals helped speed the development process. Even executives at Intel Corp.—which, led by cofounders Robert Noyce and Gordon Moore, vigorously opposed the program in its early days—now admit that VHSIC helped to drive commercial development in the 1980s. VHSIC might have had an even greater commercial impact were it not for special restrictions imposed on the program by Congress (see p. 100).

"VHSIC helped," says Ron Williams, general manager of Intel's Military Division in Chandler, Ariz. "It helped a lot of the people who didn't believe that chip densities would increase as fast as they did. It pushed commercial technology."

Among the technical breakthroughs spawned by VHSIC is the use of multiple layers of metal in advanced semiconductors, now a routine design feature in high-density ICs. Surface-mount packaging technology, also virtually unheard of a decade ago, has since revolutionized the way chips are mounted on circuit boards. On-chip self-testing capabilities, which incorporate in silicon all the test functions a given chip might need, are now finding their way into commercial chips. And gate arrays, which were just coming into vogue in the early 1980s, were given a boost by VHSIC support.

VHSIC also contributed to the development of dry etching techniques and of



## Westinghouse's VHSIC Signal Processor won't fly in the F-16 until 1991

more purified silicon with the low-defect densities essential to making fine-line geometries work. "There are 100 subtleties where VHSIC really helped; most people have forgotten about that contribution," says Westinghouse's Strull.

That was the point: to set goals that industry could reach and surpass, says Dick Urban, VHSIC program director since last summer. "The legacy for VHSIC is that by setting clear technical goals, we got companies to push forward much faster than they would have otherwise. Some contractors say they're three to five years ahead of where they would have been without the program."

**NO INSERTION.** While the VHSIC program succeeded in advancing the state of the art in technology, it failed to advance the pace of technology insertion in military systems. A 1982 Defense Science Board report on the VHSIC program's first two years concluded that unless the Defense Department changed the way it did business, VHSIC would not make it into systems until long after it had slipped from the leading edge of technology.

The classic example: when VHSIC was first being discussed in 1978, the radar processor in the Air Force's F-16 fighter was considered a prime candidate for the new technology. Today, VHSIC still is not flying in the F-16, although the Air Force says that the souped-up radar in the upcoming F-16 Block 50 upgrade will include Westinghouse's VHSIC programmable signal processor. The Air Force promises to use the most advanced chips available when procurement begins. But that won't be until at least 1991.

Why has it taken so long? First, systems are upgraded not when technology rolls along, but according to a schedule

written long before the system is ever fielded. Second, the budgetary process encourages program managers to cut upfront costs, often by forgoing development in favor of available technology. Third, there are no incentives for program managers to gamble on advanced technology (see p. 103).

"The average time between conception and fielding of a major [weapons] system is 12 to 14 years," says Strull. The delay virtually guarantees that by the time a system is in the field, the technology that makes it work is obsolete. Indeed, the few applications in which VHSIC-class parts have found their way into systems have been as gate or logic arrays mimicking components that, some time between system validation and procurement, were suddenly no longer available.

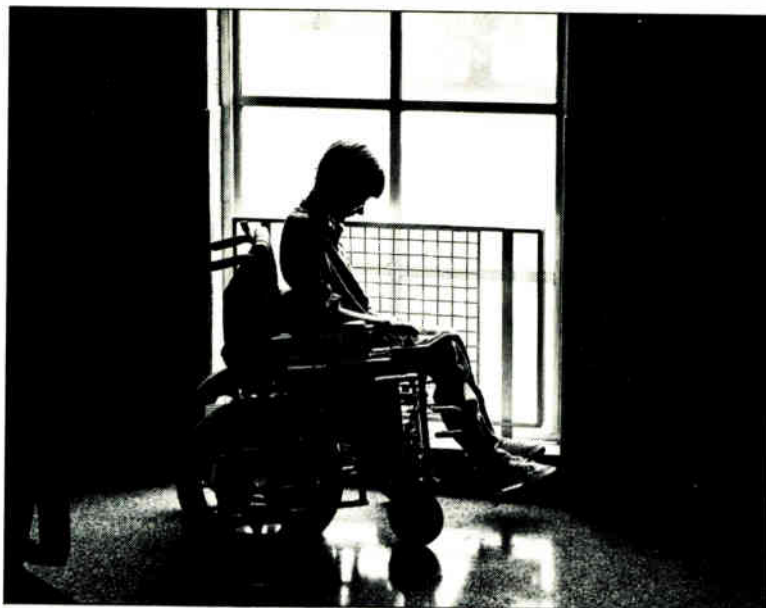
**UNCOUNTED MILLIONS.** To combat those problems, the VHSIC program office began funding specific technology-insertion programs in 1984. Yet despite uncounted millions—Urban says specific figures for the insertion effort aren't available—most of the insertion efforts continue to labor along without any apparent progress. There is a VHSIC circuit board in the AN/ALQ-131 airborne countermeasures pod, which is gradually finding air time as a retrofit spare part in the F-111 aircraft. But beyond that, no one in a position to know is willing to identify one fielded application of VHSIC.

That's not to say that VHSIC technology won't be fielded, of course. But most of the systems that VHSIC will be in won't make it out into the field until the mid-1990s. For example, the Army's Enhanced Position Location and Reporting System should save the government \$100 million over the lifetime of the program by using VHSIC technology in its Signal Message Processor module. It sounds like a VHSIC success story. The system, however, won't be fielded for at least several years.

Industry, Pentagon, and congressional sources agree that until VHSIC is in wide use and on the battlefield, it will be hard to call the program a success. "I think we will reap the benefits of VHSIC over the next decade," says Urban. "We'll see a lot more advanced technology getting into weapons systems as a result of a lot of the products of VHSIC. Not the specific chips, necessarily, but they were test vehicles after all, designed to prove a concept. But we did a lot of the technological groundwork that has allowed other things to happen."

VHDL—the VHSIC Hardware Description Language—and other VHSIC derivatives have brought the Pentagon much closer to being able to buy commercial chips, Urban says. More significant still,

What's  
more paralyzing  
is the way  
he gets treated.



The hardest part about having a disability is being constantly reminded that you have one. Sometimes that happens when people stare at you. Or point at you. Or don't even think of including you in every day activities. Maybe it's time to start treating people with disabilities like people.





it has opened the doors for a recent push toward generic specifications [*Electronics*, March 31, 1988, p. 83]. The Defense Electronics Supply Center, which certifies semiconductors and fabrication facilities, now has a generic spec for gate arrays that allows a chip maker to qualify a whole family of arrays with one evaluation circuit. Once that's done, manufacturers can sell any design produced on one of those arrays as if it were on DESC's Qualified Parts List.

Taking that a step further, DESC and the Rome Air Development Center are now creating the specifications to approve Qualified Manufacturing Lines. QML designation will eventually allow a manufacturer to produce military-qualified parts without having to subject large numbers of sample chips of each design to destructive testing, a time-consuming, expensive process. "QML is supposed to address VHSIC and VLSI, the high-densi-

ty, low-volume circuits that are too expensive to run through destructive testing," says Mike Adams, a DESC engineer involved with the QML program.

**DID VHSIC SUCCEED?** Compared with the military technology of the 1970s, today's systems are without question worlds ahead. Tomorrow's weapons will be even more advanced. Thanks to VHSIC technology, if not VHSIC-program chips, the Advanced Tactical Fighter will be the most sophisticated fighter aircraft ever built, the M-1 tank will be more intelligent than any other tank in history, and the LHX will be the world's most advanced attack helicopter.

The real impact of the VHSIC program won't be felt until the 1990s and beyond. But some things are clear now. VHSIC didn't succeed in helping the government leapfrog the commercial sector. But, says Sumney, "They were so far behind that the commercial industry to begin with that

leapfrogging was probably impossible. Catching up was pretty good." What the VHSIC program did, he adds, was "focus the attention of both sides of the house—commercial chip makers and military systems people—to move more rapidly. Clearly, the Japanese spurred the industry to do better too. But VHSIC focused attention on finer resolutions much faster than would have happened otherwise."

VHSIC had still another effect, Sumney says: "From the systems standpoint, it caused the weapons systems engineers to be more aware of what they really needed, to be less constrained by perceived limits on the technology, and to really take a freer view and strive for the greatest capability imaginable." And that, perhaps, is VHSIC's greatest legacy. Just as the personal computer unleashed the power of microelectronics on every worker's desk, time will credit VHSIC with doing the same on the battlefield. □

## WHY HASN'T VHSIC GOTTEN INTO MORE SYSTEMS?

**W**hen the Very High Speed Integrated Circuits program was just getting off the ground, the Air Force said the F-16 was a prime target for VHSIC technology. "The Pentagon's VHSIC program would mean faster processing for radar, weapons control systems, and imaging systems aboard such aircraft as the F-16," said *Electronics'* first story on the VHSIC effort, in September 1978. More than a decade later, the Air Force is still promising to fly VHSIC in standard versions of its F-16C/D fighters—but not before 1991, at the earliest.

Delays like the one that struck the F-16 program hit every VHSIC-insertion effort. "If the system-acquisition community had gotten serious about VHSIC, if any one of the major applications had come through, the individual contractors would have been saturated—they'd have been working around the clock," says E. D. "Sonny" Maynard Jr., vice president for engineering and operations at the McDonnell Douglas Electronic Systems Co. in McLean, Va., and VHSIC program director from the summer of 1982 through the summer of 1988.

But that didn't happen. And if there's any major failure that could be pinned on VHSIC today, that's it—the technology has yet to make it to the battlefield.

When asked what went wrong, Maynard's answer is simple: "We have a system-acquisition process

that is bulletproof to technology."

The process drives procurement officers and companies alike away from new technology and toward what's safe and easy, Maynard says. While the Defense Department has tried to be serious about life-cycle costs—where VHSIC technol-

ogy promises major gains in overall reliability and therefore offers sizable maintenance savings—other policies have made a sham of the initiative. The budgeting process drives program managers toward minimizing front-end acquisition and development costs, Maynard says, scaring them off new technologies that require development expense up front—even if they promise savings in the future. Instead, he adds, the system encourages managers to stick to the tried and true, even if it's obsolete.

"It's a systemic problem," Maynard says. "And you can't fix that with R&D." More attention should have been focused on technology insertion at VHSIC's outset, he says, and once the VHSIC technology insertion effort began, in 1984, more money should have been spent to make sure those insertions happened. In 1984, for example, the Pentagon allocated only \$14 million for VHSIC insertion efforts—well below the \$50 million a year a Defense Science Board study group recommended in 1982.

Looking back, Maynard says, a lot more could have been done to make the VHSIC program more successful. "The secretary [of Defense] should have dictated by fiat that VHSIC be used. The commitment to modifying the acquisition process should have been made up front. We tried to jump in in the middle and back-fit things." And it didn't quite work. —T. N.



**M**aynard: the technology was a hit, but insertion fell short





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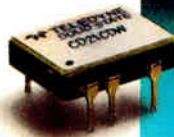
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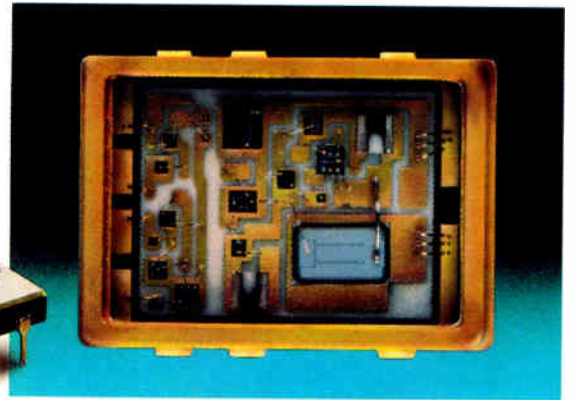
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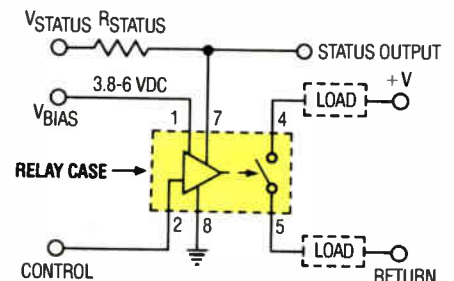
PART # CD21CDW

Review the electrical characteristics and call us for immediate application assistance.\*

ELECTRICAL CHARACTERISTICS (-55°C to +105°C unless otherwise noted)				
	Min	Max	Units	
Bias Voltage ( $V_{BIAS}$ )	3.8	6.0	$V_{DC}$	See Note 1
Bias Current ( $I_{BIAS}$ )		15.0	mA	$V_{BIAS} = 5V_{DC}$
Control Voltage ( $V_{IN}$ )	0	18.0	$V_{DC}$	
Control Current ( $I_{IN}$ )		250	$\mu A$	$V_{IN} = 5V_{DC}$
Turn-Off Voltage ( $V_{IN(OFF)}$ )	3.2		$V_{DC}$	
Turn-On Voltage ( $V_{IN(ON)}$ )		0.3	$V_{DC}$	
Continuous Load Current $I_{LOAD}$ @ 60 VDC		1.2	A	-55°C to +25°C
		0.7	A	+85°C
Output Trip Current ( $I_{TRIP}$ )	2.4 (Typ.)			+25°C, 100ms
On-Resistance ( $R_{ON}$ )		0.65	Ohms	
Turn-On Time ( $T_{ON}$ )		1.5	ms	
Turn-Off Time ( $T_{OFF}$ )		0.25	ms	
Status Voltage ( $V_{STATUS}$ )	1	18	$V_{DC}$	
Status Current ( $I_{STATUS}$ )		2	mA	$V_{SAT} \leq 0.3V_{DC}$ See Note 2

- Notes: 1. Series resistor is required for bias voltages above 6V<sub>DC</sub>.  $R_S = (V_{BIAS} - 6V_{DC})/15\text{ mA}$   
 2. A pull up resistor is required for the status output.  $R_{STATUS} = (V_{STATUS} - 0.3)/I_{STATUS}$   
 3. Output will drive loads connected to either terminal (sink or source).  
 4. Status circuit is a built-in test feature checking the input circuitry of the relay. Status output is low (on) when the input is on.

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BY LARRY WALLER

# Is smart power really a smart idea?

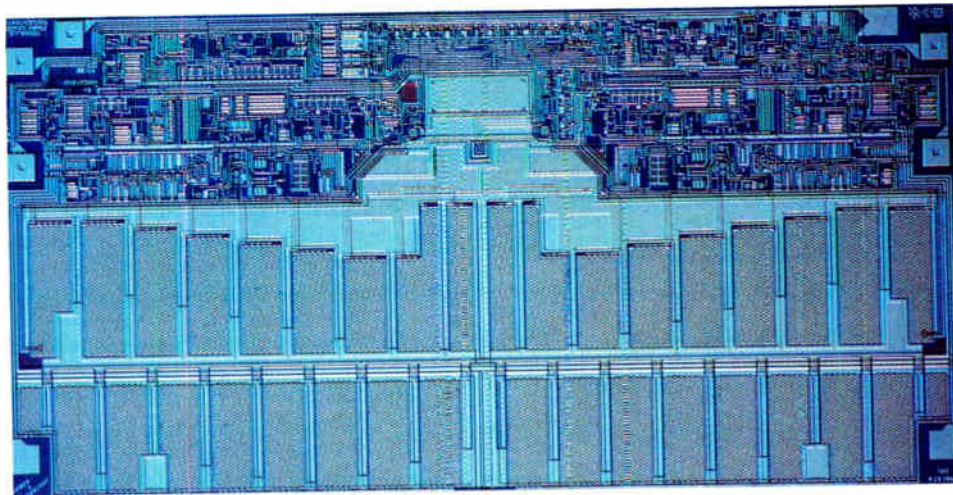
These glamour chips haven't taken off the way the pundits once predicted. The reasons: steep prices, inflated expectations

**W**ith an inspired name like "smart power," how can a promising new part of the semiconductor business miss being a big winner? As the glamorous one-chip showcase of power integrated circuits that neatly bundle a power-switching element and logic-control circuitry, smart power began to seize the imagination of users and suppliers some five years ago. Advances in MOS-FET design along with the process technology to knit these parts together monolithically promised to solve the snags that previously made one-chip answers impractical.

But smart power seems to have stalled in what industry watchers once predicted would be a steady upward path to the big time. Forecasters expected that by now, smart power would be on its way to becoming a billion-dollar market worldwide. In point of fact, the best-informed sources put current sales of pure smart power, in monolithic single-chip form only, at less than a third that size. "Things just didn't happen as quickly as we expected," says Roger Janikowski, who manages Motorola Inc.'s brand of smart power, called Smartmos, at its Semiconductor Products Sector in Phoenix. "There

was a lot of technology and marketing hype out there. Now reality is starting to set in."

The faltering course of this technology has little to do with smart power's advantages—there is no question about what draws users to the concept. Because all electronic equipment needs power switch-



**Smart power neatly bundles a power-switching element and logic circuitry, as in the IR8200 from International Rectifier**

ing in one form or another, it is loaded with bulky discrete component assemblies or electromechanical switches and relays that control power distribution. Boosting the performance of this equipment depends on replacing components and switches with solid-state devices incorporating logic-control circuitry. That's the bailiwick of smart power.

The benefits of moving to this technology are vast, says a report on intelligent power published last year by the industry consultant Dataquest Inc. in San Jose, Calif. They start with enhanced reliability of equipment, more efficient energy management, and space savings. Once smart-power devices are available in volume at volume-production prices, all this will come at lower cost than current solutions, thanks to the need for fewer parts, Dataquest says.

Applications vary widely, from industrial gear running at more than 1,000 V to automotive tasks needing less than 100 V and microprocessor controls at 5 V. As a result, the potential market is so huge and relatively untapped by solid-state parts that its very size is subject to debate. One reason is that other intelligent-power approaches, such as multichip sets and hybrid packages, get lumped in with pure smart power. "It's very difficult to get data, the market is so widespread," says Peter Weber, executive vice president of marketing at smart-power pioneer Siliconix Inc. in Santa Clara, Calif.

Most executives at the 20 or so firms engaged in smart power in the U. S. believe they have sorted through the confusion that initially stymied their industry. Indeed, solid products are starting to appear that offer real utility to users, and

## Solid products are finally here, and the market should rise 30% annually for the next five years

smart-power makers say the business has now reached critical mass: they're predicting market expansion at about a 30% annual clip for the next five years.

A wild card in the calculations is what the big Japanese chip makers are doing. They are a "hidden part of the market in power," says one U. S. executive, due to the vertical integration that keeps most advanced chips inside these mammoth companies for their own new hardware. The big fear is that some of these ICs will suddenly be sprung on the U. S. market as proven products, creating stiff competition for domestic vendors.

One tip-off that smart power is moving again is the plethora of sophisticated devices coming to market in recent months. SGS-Thomson, which leads the intelligent-power field in sales volume, according to Dataquest, offers its VIPower line in a mix of three process technologies: CMOS, n-MOS, and bipolar. The family is aimed at automotive applications such as electronic ignitions and at driving industrial motors.

Motorola's Smartmos line, with some 30 patents and seven years of development behind it, has some eye-catching new offerings as well. These include the MPC1510 logic-to-power IC, which is used for switching power loads directly from microprocessor inputs, and the just introduced MPM3003. This device is a three-phase bridge driver for powering dc motors in disk and tape drives.

**MOTOR CONTROL.** One new chip attracting much attention because of its complexity is the IR8200, built jointly by International Rectifier Corp. of El Segundo, Calif., and National Semiconductor Corp. of Santa Clara. It targets a wide number of jobs by controlling motors of up to one-quarter horsepower. The chip incorporates four power FETs on about 60% of its 140-by-270-mil die. International Rectifier has also had some success with an earlier chip set, the IR2110 half-bridge driver and the IR2100 buck converter bias supply. These parts simplify the design of advanced off-line switched-mode power supplies and motor controls, reducing system design time and board space [*Electronics*, April 28, 1988, p. 93].

The newest player is Power Integrations Inc., which started up in May 1988 and is planning to unveil a smart-power line this month. The Mountain View, Calif., company has a power-transistor technology that it claims trims device area by more than half compared with competing products. It can control more than 400 V, operating in some cases directly from the ac line.

Arthur E. Fury, vice president of marketing at Power Integrations, says the firm's advances give it a marked edge in the field. "We have broken the code on making smart power economical," he says. The first three products, in 200-, 300-, and 400-V versions, target the interface between wall electrical outlets and all kinds of equipment that needs logic controls. Fury says the prices will run about \$2 per device in volume purchases, far under the \$10-and-up custom-based tabs presently prevailing for similar parts. Power Integrations is backed by a blue-chip lineup of venture capitalists and will use outside foundries to produce its products.

In the midst of this flurry of activity, it's easy to lose sight of the factors that initially slowed smart power's takeoff. One key element was extravagant expectations on the part of both vendors and users, industry insiders say. Vendors erred in interpreting the wish lists of potential customers confronted with a flashy new technology as firm buying plans; they were anything but.

For their part, customers—many of them in the industrial markets and unfa-

### WHERE SMART POWER IS HEADED

Year	World Total	United States	U.S. Share	Rest Of World's Share
(Millions of Constant U.S. Dollars)				
1987	\$255	\$166	65%	35%
1988	365	241	66	34
1989	505	333	66	34
1990	690	462	67	33
1991	835	593	67	33
1992	1137	773	68	32
1995	2410	1663	69	31
5-year Compound Annual Growth Rate 1987-1992	34.85%	36.02%		
5-year Compound Annual Growth Rate 1990-1995	28.42%	29.20%		
8-year Compound Annual Growth Rate 1987-1995	32.41%	33.38%		

SOURCE: DATAQUEST INC.



miliar with the semiconductor business's lengthy prototyping process—believed that products were already finished rather than in early stages of development. They soon found otherwise and then had to foot some of the development cost in the form of high prices, says Ian Wilson, manager of the Power and Analog Marketing Group at SGS-Thomson's U. S. headquarters in Phoenix. "There's a big difference between [a customer] liking a technology and shelling out hard-earned dollars for it," he says.

In fact, power ICs still cost eight to 10 times more than users conditioned to off-the-shelf electromechanical parts are willing to pay to replace them. Automotive engineers, for example, aren't ready to replace a 30-amp relay for switching that they've been using successfully for years at \$1 a pop with a smart-power package costing \$8 to \$10.

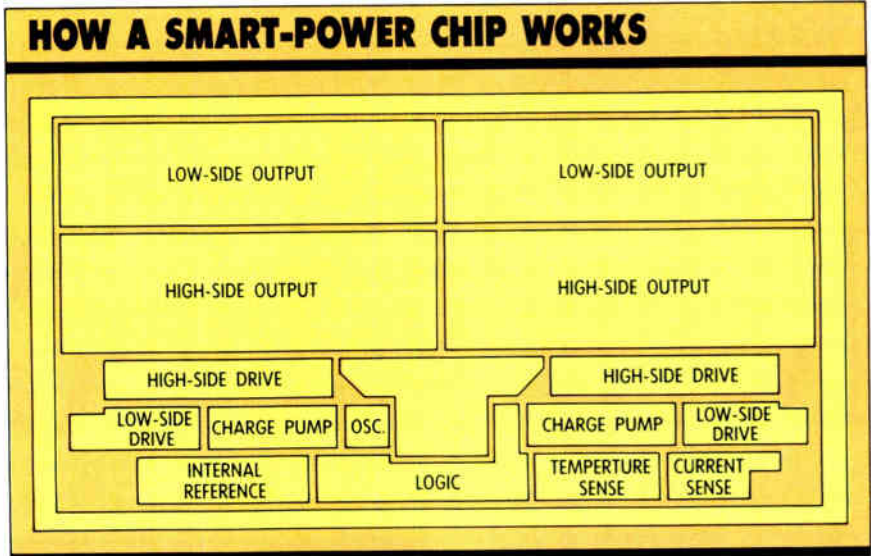
**HIGH COSTS.** Moreover, costs will stay high until the industry is selling smart power in volume, simply because of the complexity of making power devices. Depending on the type, smart chips may need upwards of 10 mask levels, more than commodity dynamic random-access memories. High costs are less a barrier, however, in brand-new designs where performance is the key.

Perhaps more troubling than these problems was the chip makers' initial difficulty in coming up with properly designed devices. Source after source concedes that suppliers first designed devices showcasing their specialties in fairly general approaches that didn't cut the mustard for particular users' needs.

Companies believed that such standard parts could be developed early in the game for specific customers and then sold to a wide cross-section of users. But this wasn't the case; most customers have unique requirements that keep a smart-power device designed for them from being easily, or economically, revamped. In this respect, smart power follows in the tracks of application-specific ICs, which suffered a number of false starts along these lines before matching products more realistically to customer needs. The custom aspect of the smart power business jangled buyers' nerves, too, because of the lack of second-source suppliers.

It took some years, of course, for smart power makers to sort all this out. The approach they have settled upon to handle it is a semicustom scheme akin to ASICs, where a basic module can be tweaked for other customers.

Added to the custom-IC stumbling block was technological confusion. Most entrants came at the technology from either the discrete-power field or the IC



## These ICs integrate on one chip a multitude of elements that were once separate parts; here, the IR8200

side, and had to hustle to acquire expertise in the other realm. To get a balanced product, "the discrete guys had to go for smarter chips, and the IC guys went for more power," says Ed Day, vice president for marketing at Ixys Corp. in San Jose, which sells multichip power ICs for industrial systems needing high voltage. Expanding into another unfamiliar technology took longer and cost more than they anticipated, he says, creating a lag in offering products.

A number of other things have conspired against smart power and, indeed, all power ICs during past few years:

- The tardiness of the U. S. automotive business to become the massive user that had been forecast, although smart power is now appearing on upscale models.

Equipment like the long-awaited multiplexed automotive control systems and antiskid brakes, which require smart power, is still years away from generating big markets. In Europe, by contrast, West Germany's Siemens AG says the auto sector is growing faster than the industrial market, and now gobbles up 80% of the Munich electronics giant's smart power devices.

- Because many of the applications targeted by power ICs are now done by mechanical or electromechanical means, converting them to solid-state power requires hard-to-find expertise.

The conversion therefore is taking longer than anyone expected. The same holds true for new applications in industrial and consumer fields, where suppliers have been hard put to adapt the de-

vices to many different fields.

- The myth of the monolithic "smart power superchip," promulgated widely several years ago, hurt other intelligent-power solutions whose implementation would have smoothed the way toward eventual one-chip power.

Two-chip answers are better in both performance and price in most applications, such as motor controls, converters, and power supplies, except where space is tight. Siemens, for example, says that putting logic and power on different chips allows it to use the best technology for both without monolithic compromises, and of its 13 smart solutions, six are two-chippers.

Whatever the factors that kept smart power from immediate success, the result has been a cloudy financial picture for suppliers. Many say they are worried about how to recoup their big stake in power-IC development. One smaller firm reports pouring more than \$10 million into its program, which has turned out high-quality products but continues to eat up capital with no profits in sight. Industry watchers believe that market leader SGS-Thomson is likely seeing a small operating profit on its smart-power line. Motorola remains mum on the subject of how well Smartmos is doing.

While profits so far elude suppliers, the potential of power keeps luring new hopefuls to the field. And the promise of this technology is such that some industry watchers believe smart power may yet become the important semiconductor sector once envisioned. □

CPU'S ARE  
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BY BERNARD C. COLE

# NEW BRISC BEAT

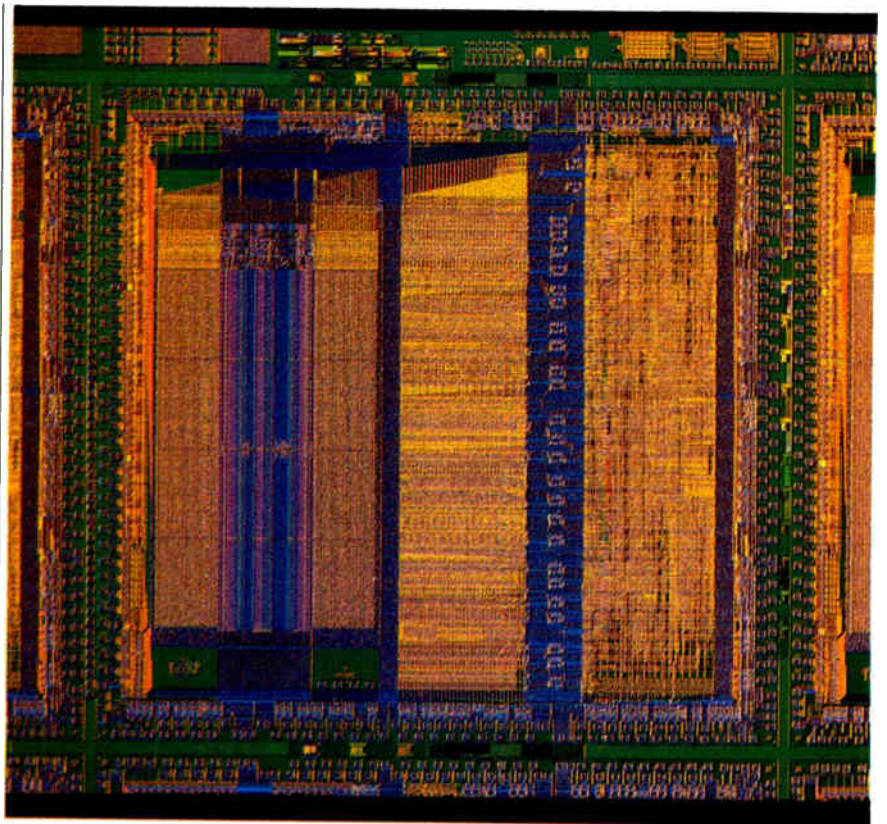
THESE BIPOLAR OR BICMOS RISC PROCESSORS WILL PUSH CLOCK RATES TO 100 MHz WITH MIPS TO MATCH

**A**dd another acronym to the alphabet soup of today's overheated microprocessor market: BRISC. Even as manufacturers of complex- and reduced-instruction-set devices are gearing up for a new generation of 30-to-40-MHz machines running 20 to 25 million instructions/s, chip designers are readying the next wave: bipolar or biCMOS RISC processors. These BRISC central processing units can be expected to push clock rates to 100 MHz or more, with mips to match.

Among the first to jump into this market is Bipolar Integrated Technology Inc., which this month will start sampling a bipolar emitter-coupled-logic version of Sun Microsystems Inc.'s Sparc chip set. In its first iteration, the set will achieve throughputs as high as 50 to 60 mips with cycle rates of 80 to 100 MHz. By the time the Beaverton, Ore., company is in volume production by the end of the year, it expects to be well along in development with higher-speed versions pushing throughput to 100 mips or more.

Nor is BIT alone. At least one other company, Motorola Inc., in cooperation with Data General Corp., is marching ahead with a bipolar ECL implementation of its 88000 RISC architecture. Also in the works, from NEC Corp., is a bipolar ECL version of the MIPS Computer R2000/3000 architecture.

On the biCMOS side, Cypress Semiconductor Corp. is reportedly working on a



**First into the market is Bipolar Integrated Technology, with a bipolar ECL version of the Sparc chip set boasting throughputs of 50 to 60 mips.**

biCMOS ECL version of the Sparc architecture, and Integrated Device Technology Inc. is said to be developing an ECL version of the R2000/R3000. Another Sparc player, Fujitsu Ltd., is also planning an ECL implementation, either in biCMOS or pure bipolar. The company will also be the foundry for a bipolar version of Intergraph Corp.'s Clipper that is expected out early next year.

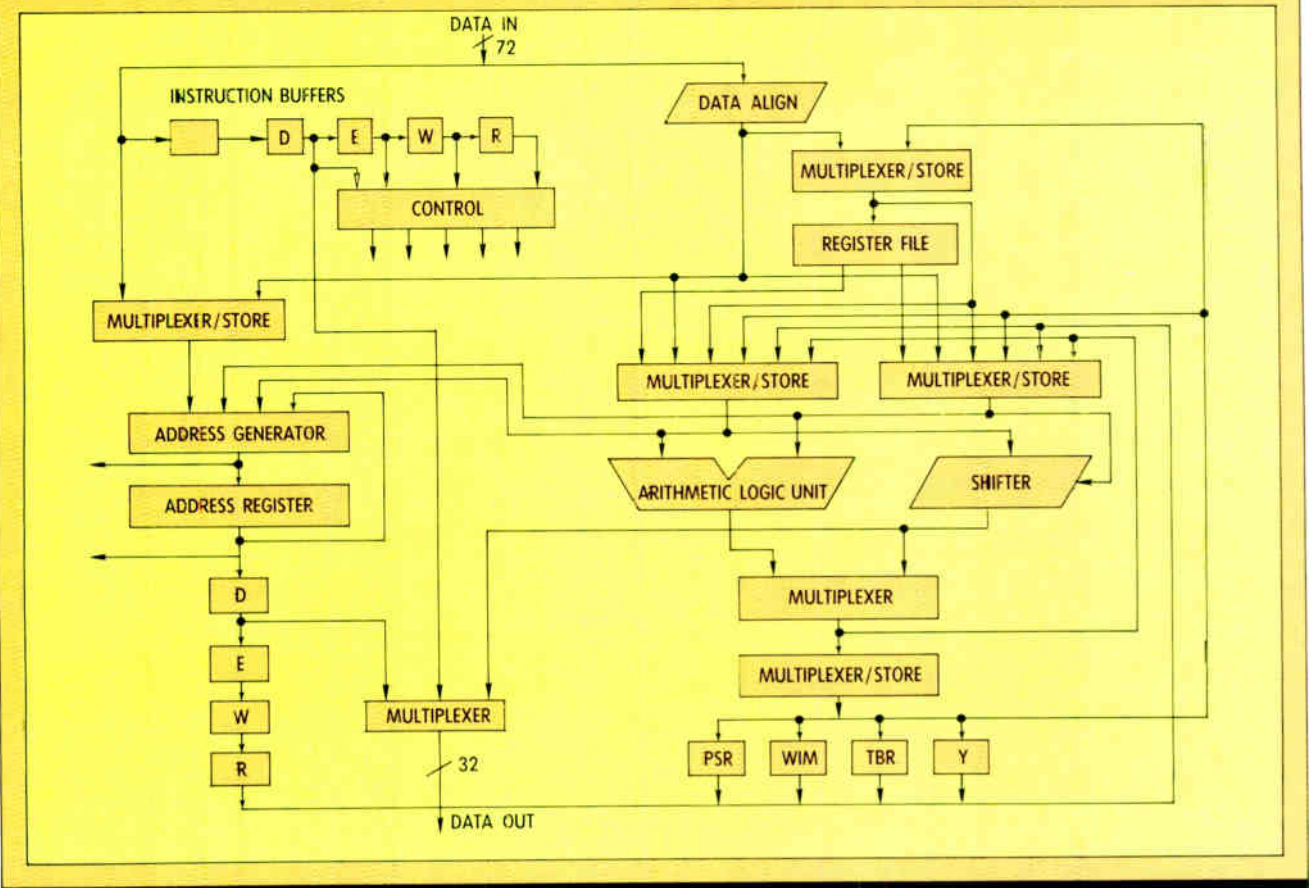
These new high-speed RISC devices are not targeted at replacing current CMOS chip sets but are, rather, complementary

to them. Where the CMOS RISC offerings are aimed at high-end personal computers, low- to midrange work stations, and embedded applications [*Electronics*, May 1989, p. 70], the BRISC chip sets are intended for high-end work stations, minicomputers, and superminis.

Users at this level are shifting away from proprietary architectures, customized chips, and proprietary operating systems to a more universal hardware platform that supports a standardized operating system such as Unix, says Christo-



## HOW BIT'S INTEGER UNIT IS PUT TOGETHER



The BIT implementation consists of the B5000 integer unit, above, which performs all instruction fetches and integer operations; and the B5100 floating-point controller, which supports floating-point coprocessor instructions.

pher DeMonico, vice president of marketing at BIT. "But they will only make the shift," he says, "if they can get the performance they want, with reasonable power dissipation and at an integration level at least equivalent to what they could get with CMOS RISC offerings."

**ZOOMING GROWTH.** While the market's size is relatively modest by CMOS RISC standards, its growth rate certainly is not. By some estimates, the market for ECL RISC in bipolar/biCMOS could grow from virtually zero at present to \$35 million by the end of 1990 and as much as \$70 million annually by 1992. Even more tantalizing to many of the companies exploring BRISC is the "drag" effect this new breed of chip sets will have on the sale of all the other components needed to make a complete system: peripherals, glue logic, and memory.

From a larger perspective, the excitement generated by the anticipated introduction of these new chips is rejuvenating the entire ECL market. After several years of essentially flat growth and a market rise from about \$475 million in 1988 to a projected \$500 million in 1990, the market for VLSI ECL circuits is now expected to shoot forward to about \$750

million by 1993. ECL memories should grow from about \$350 million this year to about \$510 million by 1993 [*Electronics*, February 1989, p. 84]. ECL-based programmable logic, meanwhile, is expected to grow from \$15 million in 1988 to about \$250 million in 1993.

Aiming to establish a leading position in this emerging marketplace, BIT executives are taking note of the history lessons of the semiconductor industry: if you want to be a major player, especially when competing with much larger companies, it is important to get to the market first with a product that offers a reasonable performance boost over existing technology. Ideally, the product should be fabricated with a process that offers the potential of future speed and density improvements, better yield, and lower cost. It also must be supported by development tools, operating systems, and application software that will allow original-equipment manufacturers to implement a design and get to market ahead of the competition.

By choosing Sun's popular Sparc architecture, says DeMonico, BIT satisfies the latter part of the equation. And there's ample evidence that the first require-

ments—for better performance now and potential improvements along the way—are being satisfied, too.

The chip set being sampled consists of the B5000 integer unit, which performs all instruction fetches as well as integer operations, and the B5100 floating-point controller, which supports floating-point coprocessor instructions. Complementing these two binary-compatible Sparc chips and rounding out BIT's RISC offerings are three of the company's already existing bipolar VLSI products: the B3210A, a 16-K-by-4-bit three-port register file; and the B3110A/B3120A floating-point multiplier and arithmetic logic unit.

**GOOD NUMBERS.** First silicon on the new integer unit and floating-point controller yielded some impressive results, says James Peterson, BIT's engineering design manager: the dice were tested at 65 mips with a 100-MHz clock. Even though the chip set that is being sampled this month is specified somewhat more conservatively—50 VAX-based integer mips at 80 MHz—it far outperforms comparable CMOS offerings from Fujitsu (10 mips) and Cypress (20 mips). Simulated Linpack benchmarks are between 10 million and 15 million floating-point opera-

tions/s for order 100 double precision.

The big surprise in all this is the process. Unlike some of the advanced submicron bipolar and biCMOS processes being proposed to build competitive ECL BRISC implementations, the BIT chip set is being manufactured with essentially the same relatively conservative approach that's used on the firm's bipolar VLSI products.

The 3210A, 3110A, and 3120A are fabricated with the company's 2.0- $\mu$ m BIT101 process. This two-level-metal scheme incorporates transistor structures with minimum critical dimensions of no more than 1.2  $\mu$ m and a metal pitch of 4.0  $\mu$ m, allowing densities as high as 20,000 to 25,000 gates. The new BRISC chips are built pretty much the same way, except that three levels of metal are used and the basic transistor structure has been modified.

**KEY-SHAPED.** Where the original transistor is roughly rectangular and has equivalently sized collector, emitter, and base elements, in the new process the transistor is key-shaped and has a larger collector area with smaller base and emitter structures. This results in a significant reduction in output emitter-follower capacitance, allowing an increase in the cutoff frequency of about 25%, from 5 to 6.25 GHz. It also means a reduction in the unloaded delay time, from 300 to 250 ps. In addition to the performance boost, the process improvements have also pushed the integration level to about 40,000 to 50,000 gates for about the same die area, 380 by 400 mils, says Peterson.

The overall impact of this increase in density is twofold. BIT designers have introduced an integer-unit/floating-point-controller Sparc chip set that is binary-compatible and roughly the functional equivalent of the CMOS implementations. But they've also managed to incorporate architectural enhancements to improve the cycles-per-second execution rate.

The most obvious difference between the BIT implementation and earlier Sparc chip sets is in the pipeline complexity. Instead of the present four-stage pipeline, BIT uses a five-stage pipeline: fetch, decode, execute, memory access, and write back. A second difference is that unlike earlier versions, the BIT integer unit in-

corporates an instruction prefetch unit and a set of internal instruction buffers with a four-word queuing capacity, four times that of existing implementations.

The overall bus structure has also been considerably modified, Peterson says. Most important is a shift from a bidirectional bus structure typical of CMOS Sparc implementations to a unidirectional structure compatible with 10K ECL design methodology to simplify the design of controlled-impedance circuit boards.

At the same time, buses have been widened. Internally, the integer unit incorporates a 72-bit-wide data-fetch bus, versus 32 bits on other Sparc implementations. Also, 64-bit-wide paths separate the floating-point subsystem and cache memory for high-speed double-precision data transfers.

Overall, says Peterson, the improvements result in 1.2 cycles per instruction, versus 1.4 for the Cypress CMOS Sparc implementation and 1.6 for the Fujitsu version. This is due to the fact that the BIT integer unit can perform load and stores in a single cycle, says Peterson. This operation requires multiple cycles

in many of the present RISC machines. Also, he says, because the load and stores for many floating-point operations are performed on separate 64-bit data paths, double-precision operations are improved considerably by the BIT approach.

When used with the existing 3110A/3210A, the new BIT chip set can do double-precision multiplications with only a 50-ns latency time and 25-ns double-precision ALU operations. This compares with 60 ns for both types of operation with the TI8847 controller used with the Cypress chip set.

Even more impressive is the effort under way at Motorola and Data General, where engineers are defining the overall structure and partitioning of a bipolar ECL version of the 88000 RISC chip set that aims at throughput rates beyond 100 mips. Current plans are to fabricate the BRISC version using Motorola's fourth-generation submicron bipolar ECL process, says Jeff Nutt, microprocessor technical marketing manager at the company's Semiconductor Products Sector in Austin, Texas.

It will pack anywhere from 40,000 to

50,000 gates onto a single chip and implement logic functions that toggle at frequencies above 1 GHz. The scheme employs four levels of interconnection, three for signal routing and one for power and ground.

Less well defined is the actual partitioning. Though development is still in the early stages, Nutt expects a final decision to be made before the end of the year, with introduction scheduled for late 1990 or early 1991. One implementation under discussion, which shows where the company is going, splits the present integrated 88100 into two chips, an integer and a floating-point unit.

Also partitioned is the cache memory-management unit, which now integrates memory management, cache control, and 16 Kbytes of cache static random-access memory. Two such CMMUs are used in present implementations, one for data cache and one for instruction cache. In the bipolar ECL implementation, the control logic from the two CMMUs is combined onto a single cache control unit (CCU), with the cache and associated tag stores implemented with discrete SRAMs.

Also added to the chip set is a system-bus interface unit, which connects the chip set to a very fast ECL system bus, controls the flow of data between the CCU and the bus, and is responsible for maintaining cache consistency in multiprocessor applications.

**100 MIPS.** With such an arrangement or something closely resembling it, says Nutt, it should be possible to design a bipolar ECL RISC chip set capable of fetching and executing instructions at a 140-mips peak rate, with a sustained throughput of about 100 mips. In simulations, this implementation produced a typical Dhrystone rating of 240,000 and a single-precision Whetstone rating of about 90,000 kilo-Whetstones.

Not to be outdone, BIT's founder, chairman, and chief technical officer, George Wilson, points out that by the time Motorola and others begin shipping samples of their first-generation BRISC designs, BIT will be well on its way to producing a second-generation design using its third-generation bipolar VLSI process, BIT201.

With three levels of metal and a 1.0- $\mu$ m minimum critical dimension, the new process will allow integration levels up to 80,000 gates with no substantial increase in die size. And when combined with a variety of architectural improvements, the second-generation parts should easily top 100 mips.

Using 0.8- $\mu$ m design rules approximately equivalent to those Motorola is using on its first-generation BRISC chip set, Wilson expects a third generation of BIT

## BRISC IS BREATHING NEW LIFE INTO THE ECL MARKET; AFTER SOME YEARS OF FLAT GROWTH, IT SHOULD SHOOT TO \$750 MILLION BY 1993



devices with a throughput of 200 mips by mid-1993.

Such extraordinarily high data rates represent a big challenge to systems designers and a big opportunity to makers of ECL SRAMs, specialty memories, and programmable and standard logic, says Bill Snow, strategic marketing manager at Integrated Device Technology in Santa Clara, Calif. Even with traditional CMOS-based CISC architectures, such as the Intel Corp. 80386/486 and the Motorola 68030/040, throughputs are moving into the 15-to-25-mips range. This is "forcing systems designers to rethink how to implement their memory hierarchy to get a minimum number of wait states," Snow says. "In many cases, because of economics, it is not even realistic to think in terms of zero wait states."

With the new RISC designs pushing up into the 30-mips, 40-to-50-MHz range, it will be necessary to rethink not only the process used to fabricate such chips, but also how to partition designs and implement caching, says David Ford, director of marketing at Aspen Semiconductor in San Jose, Calif. "With the new CMOS RISC architectures, speed requirements for a single level of cache have moved from 35 ns to 10 ns or so," he says. "With some of the bipolar/biCMOS RISC implementations being considered, the speed

requirement gets even more serious, with 3-to-10-ns access times an absolute necessity."

What this will mean is a serious rethinking of systems-implementation parameters, says Gary Baum, director of marketing at Intergraph's Advanced Processor Division in Palo Alto, Calif.

"Not only will it be necessary to increase the number of levels of cache," he says, "but caching algorithms will also have to become more sophisticated, shifting from direct mapping to two-, three-, and four-way set-associative schemes."

Indicative of this trend are some of the differences in the way BIT and Motorola/Data General have chosen to implement caching in their BRISC chips. In BIT's first-generation 50-mips design, the chip set is used with a single level of 128-Kbyte direct-mapped virtual address cache. The Motorola version, running at 100 mips or more, will have two cache levels.

The first level, which is addressed from the integer unit, can be configured with 8

## FUTURE CHIPS WILL BLAZE AWAY AT 140 TO 200 MIPS, CREATING CHALLENGES FOR SYSTEM BUILDERS

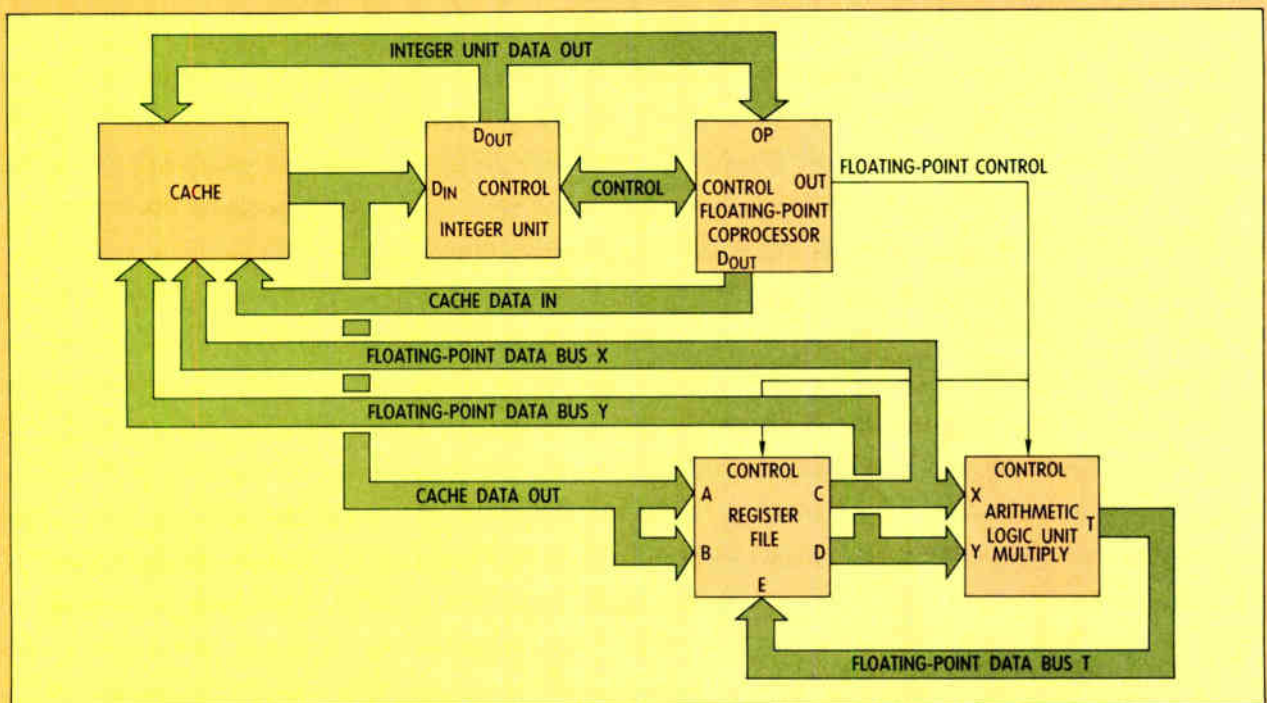
to 256 Kbytes using SRAMs with at least a 5-ns access time. The second level, which is addressed from the cache control unit, can be configured with between 64 Kbytes and 1 Mbyte using SRAMs with an access time of 12 ns.

At the speeds being considered for BRISC designs, says Intergraph's Baum, it may be necessary to reconsider how disk-based mass-storage memory is implemented. "With

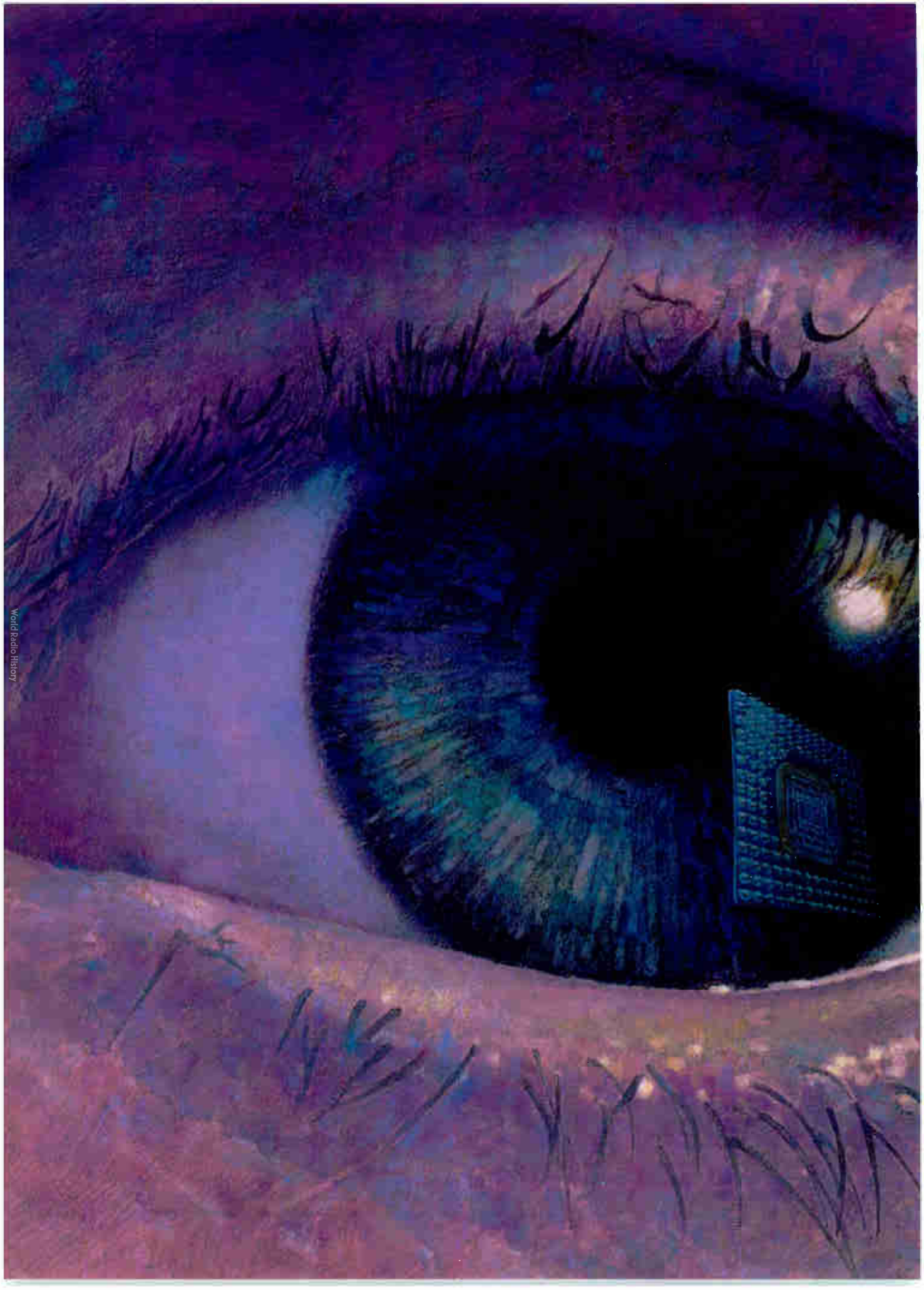
present CMOS RISC implementations, there is about a 10- or 20-to-1 difference in latency time between the CPU and the disk-based memory," he says. "Most of the time, this difference can be disguised with all sorts of interleaving and virtual memory schemes."

But at the speeds proposed for some of the advanced bipolar designs, says Baum, "it may be necessary to go to faster solid-state disks or to additional levels of caching, not only between main memory and the CPU but between main memory and the disk-based storage." □

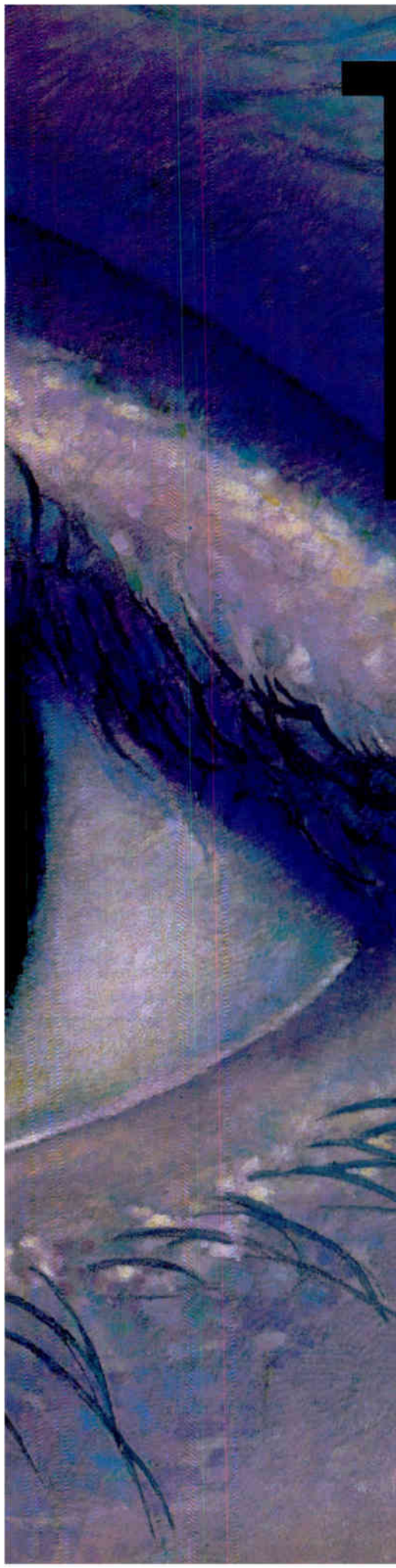
### INTEGRATING BIT'S RISC CHIPS



The big surprise in the BIT approach is the process, which is not dramatically different from the company's BIT101 scheme. Motorola, by contrast, is aiming for tighter geometries but greater partitioning in its bipolar 88000.







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# HOW ZILOG MANAGED TO TURN ITSELF AROUND

The key is a concept called forward controllership

**W**hen Ed Sack became president of Zilog Inc. in early 1985, the company was hemorrhaging after several years of crippling losses. "It did not seem as if there were any way to recover," says William Walker, senior vice president and chief financial officer of the Exxon Corp. subsidiary. It had reached the point, says Sack, that his charter upon arriving was short and simple: "Turn it around or shut it down."

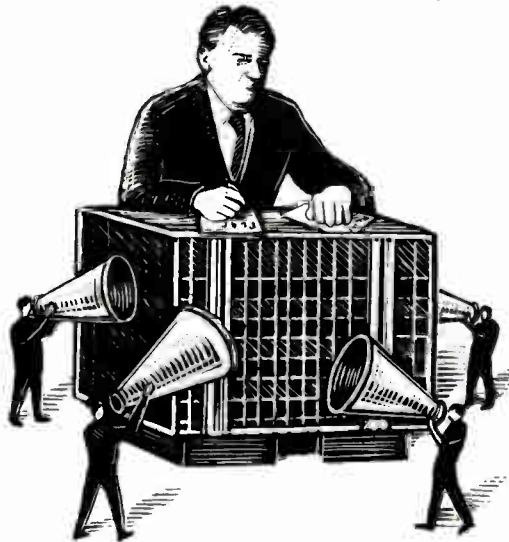
But recover Zilog has. By early 1986 the Campbell, Calif., company had reduced its losses by almost 75%, and by the middle of that year it had moved into the black. This year, it is moving aggressively forward with a strategy featuring cell-based application-specific integrated circuits and semistandard products in a number of key microprocessor peripheral markets [*Electronics*, February 1989, p. 112].

More important to Sack, for the 12 quarters since Zilog turned the corner, the company has generated a positive cash flow, returning revenue to Exxon. Moreover, it has done so without sacrificing internal investment. Zilog continues to plow back 10% of its sales each year into capital expenditures and a similar amount into research and development.

The key, says Sack, is discipline in the form of a management concept he calls forward controllership, a scheme he started developing during his 14 years at General Instrument Corp. of Hicksville, N. Y., and had refined by the time he arrived at Zilog. Forward controllership is a closed-loop system that Zilog uses to manage revenue, variance costs, fixed costs, and cash. "Rather than focusing on past performance, the aim is to get a handle on what is going on right now and what it means in terms of future growth and costs," says Sack.

It all begins with an operating plan that details the current month week by week and projects the next three

months' activities. Four areas—sales, marketing, manufacturing, and finance—have input into the plan, and their data are fused into a document published on the 10th of each month depicting unit costs for raw material, direct labor, and other direct costs. Actual unit variable costs are extended by



shipment plan to yield extended variable costs, and average selling prices are calculated from the shipment plan and revenue for that period. Subtracting the variable costs from the revenue yields the gross gain.

This information is then consolidated for the sales and marketing staffs in the form of lead time and variable costs by product, plus planned product introductions. The manufacturing arm, meanwhile, receives building plans and data on labor, raw materials, and fixed costs. Finance gets a rolling four-month revenue and budget plan and cost-reduction projections.

Zilog uses a technique it calls "lock limits" to place ceilings on variable costs and fixed-cost items. Locks prevent further spending until the next budget period.

By measuring this accumulated data, the company can calculate gross margins to determine profit and loss before taxes. Profit and loss, of course, is only one line on the balance sheet.

by Bernard C. Cole

Also important are inventory, accounts receivable, accounts payable, capital expenditures, and depreciation.

Zilog manages cash flow in all these areas by monitoring the changes in the items that make up cash. For example, the system helps the finance department determine what kind of profit-improvement programs to initiate to trim costs. Forward controllership measures performance against the plan, with corrective action and appropriate feedback provided on a weekly basis.

This reporting procedure has been transformed into a proprietary set of algorithms that model Zilog's operation on a product-by-product basis, part number by part number, says Walker. Yields from the factories are fed back to the computer, which then calculates production costs as though the parts were being manufactured that day, rather than statistical averages based on older data. This information is then incorporated into a model that extrapolates for a month into the future. "As yields go up one day and down on another, the model tells us that, on the basis of yield numbers that day, a particular part will come in at a particular cost with a specific profit margin," Walker says.

With the computer modeling, says Walker, it's possible to determine down to the die or package level what happened the day before in Zilog's assembly facility in the Philippines and on the last shift in its fabrication line in Idaho—by part, by process, and by product. With this base in real-time data, Walker adds, it's much easier to predict accurately, for example, the pricing and marketing strategy needed to ensure maximum profitability, as much as four months out. "Because everything and everyone are linked," he says, "we know exactly what must be done, who must do it, when it must be done, what yield is possible, what yield is necessary, and what's needed to get there."

Underpinning the whole process, says Sack, is a corporate focus on profit improvement rather than sheer revenue growth. "Normally, in a semiconductor company, when you are in a period of growth, the emphasis is on more growth to the detriment of profit," he says. "The key to long-term success and more than average growth is to balance the two." □

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# OK...SO THE TRANSPUTER IS POWERFUL, BUT WHAT ABOUT REAL APPLICATIONS??

They're everywhere. Worldwide over one thousand Transputer designs are in today's marketplace or are entering production. Here are details of just four significant Transputer applications.

## Data Transmission

Kokusai Denshin Denwa (KDD), the Japanese international telecommunications company, has developed an image-

processing video telephone using Transputers to manipulate and condense images for transmission over telephone links.

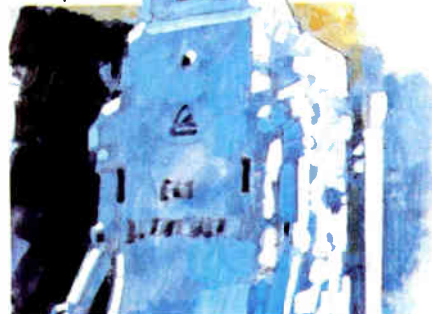
This image communications system uses 32 Transputers operating in parallel for ultrafast image processing. It can be connected to PC's to transmit images over telephone lines, function as a video

phone, or be programmed to match the specifications of other receiving equipment, such as facsimile machines and TV monitors.

## Robotics

Transputers are ideally suited for robotics applications because their special on-chip links make communication between control centers naturally easy. They are often used in the central control area for dumb robots, in multi-jointed robots, and in machine vision systems.

At the Houston Space Center, NASA and Lockheed are using Transputers in the development of an intelligent, self-manoeuvring, voice-controlled robot named EVA Retriever. EVAR is being built to investigate the autonomous retrieval of objects and become de-tached from astronauts that Station.



## System Control

As the number of Transputers in a system design are increased, a proportional increase in performance can be achieved.

In West Germany, Parsytec GmbH is using this principle in their Megaframe Superclusters. Superclusters represent a complete series of reconfigurable industrial control boards as used in the automotive industry, which exploit the Transputer's parallel processing capability.

The basic Model 64, built with T800's, has a performance of 640 MIPS and 96 MFLOPS. The Model 256 comprises four Model 64 cabinets connected by cables and provides 2,560 MIPS and 384 MFLOPS.

Parsytec believes there is no limit to the size Superclusters can grow to. Two Model 256s can be combined easily to realize twice the raw performance of one system.



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Transputers are being used in the Generic Checkout System at the NASA Kennedy Space Center.



They are embedded within VME based front-end Data Acquisition Modules to provide data filtering for the system.

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IMST800-25	32-bit	25	PGA	IMST222-20	16-bit	20	PGA/PLCC
IMST800-20	32-bit	20	PGA	IMST222-17	16-bit	17	PGA/PLCC
IMST425-25	32-bit	25	PGA	IMSM212-15	16-bit	15	PGA

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# COMPANIES TO WATCH

## WHY CADENCE IS THE TOP DOG IN THE IC DESIGN PACK

The answer for this maker of CAD chips is mergers, timing, and product

### SAN JOSE, CALIF.

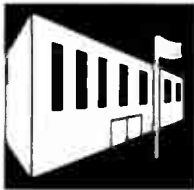
Everyone knows the way to the top: all you have to do is engineer some astute mergers, leap into the breach when your competitors stumble, and come up with products that the market wants. The catch is that few companies have the coordination and dexterity to do all three at the same time.

But Cadence Design Systems Inc. has managed to hew to the three-pronged formula for success, and as a result it has become the company to beat in the rapidly growing market for integrated circuits for computer-aided design. Last year, the San Jose-based company posted \$67.1 million in revenue, up from \$40 million in 1987. And Baltimore investment firm Alex. Brown & Sons expects Cadence to reach \$114 million this year.

In the merger arena, Cadence picked up ECAD Inc. of Santa Clara, Calif., in May 1988 and Tangent Systems Corp., also of Santa Clara, this past March. The mergers helped Cadence fill a market void when IC CAD vendors failed to field adequate next-generation products and sellers of computer-aided-engineering systems were slow to pick up the gauntlet. CAE/CAD designers, meanwhile, are satisfied with Cadence's strategy of an open framework tightly integrating offerings from third-party CAE/CAD vendors.

Cadence managed to pull off the ECAD and Tangent mergers without much trouble, says Joseph E. Costello, the company's 35-year-old president and chief executive officer. No key technology people were lost in either deal, he says, although the president and CEO of ECAD did not join Cadence. As a result of the mergers, Cadence now has more than 200 people in research and development, which Costello says is the largest team developing an IC design system.

In both deals, Cadence acquired software tools not previously available to it. It also picked up a strong



revenue generator: Draeula, ECAD's design rule-checking product. Draeula is used by most IC CAD vendors on an original-equipment-manufacturer basis, says Peter Schleider, a partner in the investment banking firm of Wessels, Arnold & Henderson in Minneapolis. Cadence also gained a superior polygon layout and compaction tool in ECAD's Symbad product line.

Schleider says the Tangent acquisition enabled Cadence to get into the lucrative system-design market. That market is vital now, as gate arrays move from the old designs with typically 5,000 to 10,000

gates into the latest sea-of-gates technology with arrays of 100,000 gates—although only half are used for any given design. Tangent is considered to have a superior set of sea-of-gates design tools.

But gate-array and standard-cell design tools were only part of the acquisition, Costello says. Other technology in the Tangent and Tancell lines will provide even more synergy to Cadence in time, he asserts. He also hints that Tangent was already busy on second-generation versions of its tools. "These are the hidden jewels that came in the acquisition."

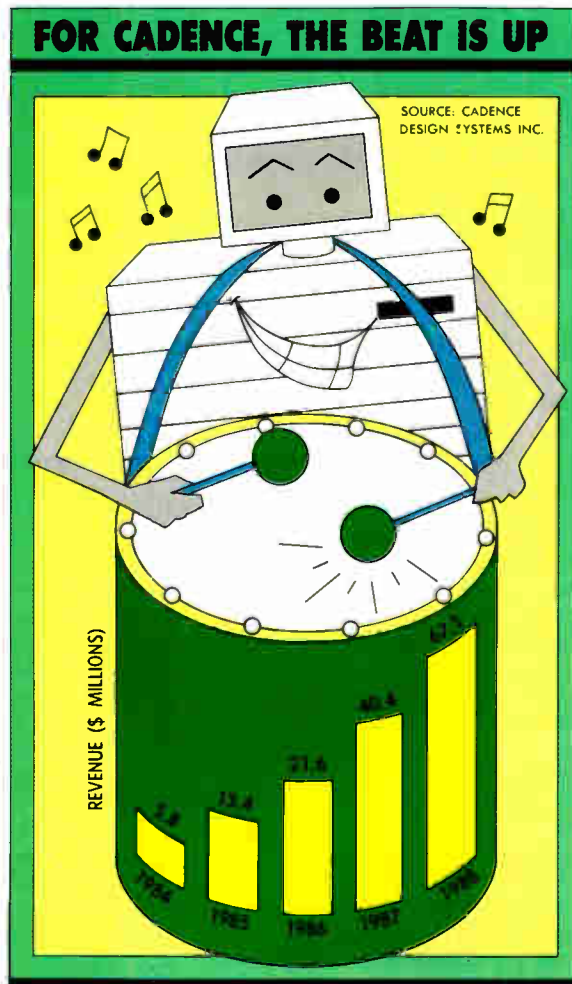
Cadence's acquisition spree began at a propitious time in the development of the IC CAD market. The EDS III tools from

Calma Co. of Milpitas, Calif., arrived late [*Electronics*, Sept. 17, 1987, p. 92] and won't start to ship until this year, says Ron Collett, senior industry analyst at Dataquest Inc., a market research firm in San Jose. And Calma's closest rival in the IC layout arena, Caeco Inc. of Sunnyvale, Calif., was too short on capital and credibility to take over the leadership position, although its tools were considered superior.

Calma's tardiness gave companies in the back-end IC design market an opportunity to gain market share, says Robert Herwick, senior technology analyst at Hambrecht & Quist Inc. in New York. The fact that CAE vendors were slow to step into the breach made that opportunity even more inviting. Daisy/Cadnetix Inc. of Mountain View, Calif., was too involved in trying to get its house in order, and Mentor Graphics Corp. of Beaverton, Ore., seemed content to sell what it had without making an aggressive move to bring new technology into the market.

The opening in the IC CAD market won't last forever, however. The Cadence-ECAD merger stung Mentor; company officials realize that Cadence has taken the initiative in the IC CAD market. Mentor will come back into the market with a vengeance, Herwick predicts.

While the ECAD merger put Ca-



dence well on its way to being the leader of the pack in IC design, the acquisition of Tangent makes Cadence a more formidable competitor in the system-design business. Dataquest's Collett says that Cadence has the largest portion of the IC design market, 15.4%. In its grouping, Dataquest includes hardware suppliers like Apollo Computer Inc. of Chelmsford, Mass., and Sun Microsystems Inc. of Mountain View, Calif., because many IC designers purchase hardware separately from software. Among Cadence's competitors in the software tools market, Seiko Instrument and Electronics holds an 11.5% market share—mostly in Japan—just ahead of Mentor, at 8.4%. Next come two San Jose companies, Silicon Compiler Systems Corp., with 7.3% of the

market, and Valid Logic Systems Inc., with 5.8%. The Silicon Compiler total includes the small percentage owned by Caeco, while Valid's allocation includes Calma's slice of the pie.

**OPEN SYSTEMS.** Cadence's open-systems approach to design tools, called Design Framework, helped set the company apart from the competition early on. Although other vendors are now embracing the approach, Costello believes Cadence will keep ahead of the pack for the near term. "Framework is a nontrivial effort to put together," he says. "Cadence will be on [its] second generation when other companies are still working on their first generations."

Cadence has added another arrow to its quiver: an OEM program called Silicon

Access Alliance. Under the program, Cadence and other participating members of the alliance can tailor a design-automation system for the user's internal use and for resale.

If there is one company that could give Cadence a fight, says Schleider, it's Silicon Compiler. The company recently rolled out its own design framework, called Foundation, and unbundled its suite of design tools. Silicon Compiler also offers a strong mixed-level simulator, a vital tool because a designer spends half his time in the front end of the design process capturing and simulating a circuit. Until Cadence purchased the source code for Silos II from HHB Systems Inc. of Mahwah, N. J., it had no simulator of its own. —Jonah McLeod

## GETTING BACK TO BASICS PAYS OFF AT ANALOGIC

### PEABODY, MASS.

**B**usiness is better at Analogic Corp. these days, and one of the big reasons is that the Peabody-based company is getting back to basics.

Under its new strategy, Analogic is putting more effort into the product lines with which it started some 20 years ago: precision data-conversion and instrumentation products. With the renewed emphasis on these products, along with a number of cost-cutting measures and a corporate reorganization, Analogic is well on the way to recovering from a major setback it suffered five years ago.

Ironically, that setback came in a market that propelled Analogic from a \$9 million company in 1975 to a \$143.7 million operation in 1984. In the mid-1970s, the company embarked on a profitable new road as a supplier of "instant imaging" electronics to manufacturers of computerized tomography (CT) scanners.

Analogic got into the CT scanner business by designing and manufacturing the data-acquisition electronics for a scanner made by Siemens Medical Systems, an arm of West Germany's Siemens AG. The design phase of that crash project took just two weeks, and by the time it was delivered six months later, Analogic had hitched itself to a rocket.

The rocket soared until 1984, when the U. S. government required hospitals to obtain certificates of need to justify the installation of CT scanners. That requirement caused the CT scanner market to plummet. As a result, Analogic's revenues from products and services sagged from \$143.7 million in 1984 to \$113.5 million last year.

The CT scanner market has now rebounded, and Analogic's revenues are again growing. Bernard Gordon, Analogic's founder, chairman, and president, estimates that the company's product and

service revenues will grow about 22% this year, to about \$138.4 million. With the first six months already reported at \$61.2 million, that estimate looks plausible.

But company executives attribute the growth less to improvements in the CT scanner market than to a recent restructuring, including facilities consolidations, along with the renewed emphasis on its nonmedical instrument business. Last year, Analogic was reorganized into

three groups: Signal Processing Technology, Electronic Products, and Medical Technology Products. Facilities consolidation cut costs further, as did trimming the labor force from 1,710 at the end of 1987 to the current level of about 1,350.

Gordon acknowledges that Analogic had lost some of its initiative in developing proprietary products for end users, particularly instrumentation products. "Our primary inventive engineers were tied up with our major medical customers and that business was good," Gordon says. "But we weren't paying much attention to new product development and business directions on the instrumentation side of the house."

### ANALOGIC BOUNCES BACK

	(In \$ Millions)				
	1985	1986	1987	1988	1989*
Product/service revenue	128.7	126.7	128.9	113.5	138.4
Total revenue	135.9	148.2	155.4	134.3	149.1
Net income	9.9	10.0	14.5	1.1	N.A.

\* ELECTRONICS estimate SOURCE: ANALOGIC CORP.

three groups: Signal Processing Technology, Electronic Products, and Medical Technology Products. Facilities consolidation cut costs further, as did trimming the labor force from 1,710 at the end of 1987 to the current level of about 1,350.

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At the peak of the CT scanner market, medical subsystems and instrumentation

equipment manufacturers, test and measurement products, and power test equipment, as well as waveform analyzers and synthesizers for end users.

In addition to the reorganization, Gordon took a major step to revitalize development of proprietary end-user instruments by hiring Jack Lieberman, a corporate vice president who now heads the group. Lieberman joined Analogic in late 1986, bringing with him 28 years in the electronic products business, 22 of them with Hewlett-Packard Co.

**20% ANNUAL DROP.** At HP, Lieberman had profit-and-loss responsibility for the Palo Alto, Calif., company's instrument and systems operations. "Instrumentation products tend to fall off in revenue production 20% per year," Lieberman





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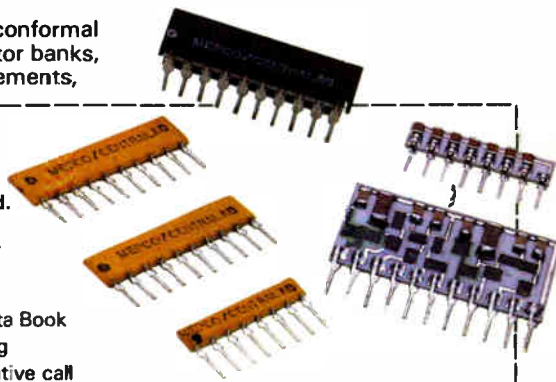
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says. "You've got to make up for that [drop-off] and grow as well, so you've got to have new products coming along constantly to survive."

Lieberman sees the \$8 billion instrumentation industry as being made up of many niche markets. "If you do \$40 million worth of business," he says, "it will be because you have forty \$1 million products, not one \$40 million product."

Gordon is quick to point out that Analogic will continue to pursue the CT scanner market. He says his company supplied the front-end imaging systems for 90% of the 2,400 CT scanners installed worldwide last year.

The company's Medical Technology Products Group also supplies subsystems for ultrasound diagnostic imaging, ultrasound fetal heart monitoring, digital X-

ray equipment, and nuclear magnetic resonance imaging instrumentation.

With the Electronic Products Group back on the right track, the reorganization complete, and the cost structure leaner, Gordon sees Analogic growing 15% to 20% per year for the foreseeable future. That's no pipe dream, he says, "assuming there is a reasonable economic climate."  
—Lawrence Curran

## A STARTUP THAT'S OFF TO A FAST START

### FREMONT, CALIF.

As high tech becomes low priority on Wall Street, Silicon Valley's image as the source of hot new technology companies is losing some of its luster. Yet although the pace of development may have slowed, the lure of fame and fortune is still charging the entrepreneurial batteries at new companies determined to achieve stardom—like Asix Systems Corp., a Fremont-based manufacturer of low-cost test equipment for application-specific integrated circuits.

Since January 1988, when the company began shipping products, Asix has installed more than 65 systems. For the past 12 months, it has racked up a respectable \$10 million annual run rate. To fund further growth, the company successfully completed a third round of financing in April that added \$6.3 million to its coffers, for a total of \$14.8 million.

Asix executives credit the company's rapid start to its strategy of selling into two markets, ASIC verification and IC production testing, while its competitors concentrate on one or the other. Richard Bullen, a company founder and the director of marketing, pegs potential sales in the verification market at \$50 million to \$60 million, and in the production testing market at \$200 million.

But the two-market strategy contains pitfalls as well as advantages, says Carolyn Rogers, technology analyst at Hambrecht & Quist Inc. in San Francisco. The main drawback, she says, is that competing in two markets means two sets of competitors and, in most cases, a need for two sales forces.

The Asix strategy may not be so much the result of planning and prescience as of necessity, says Jerry Hutcheson, chief executive officer of VLSI Research Inc., a San Jose, Calif., market research firm. Even if the general perception that there



Richard Bullen, an Asix founder, pegs the production testing market at \$200 million.

is a separate design verification market—in which designers purchased ASIC verifiers to debug their designs—is correct, he says, that market is now being integrated back into the general tester market.

Conventional wisdom holds that designers use dedicated test systems for verification. But Hutcheson contends that simulation software is now so sophisticated that most designers are not verifying their work. If verification is done, he adds, the job will most often be carried out on a test system at the ASIC supplier's facility.

If Hutcheson is correct, Asix's strategy may be completely in tune with the way the market really operates, and the company is well positioned no matter which way the market turns. The reason: Asix has one hardware system that can be configured for either verification or production testing by adding software.

For now, however, two separate markets exist, and both are fiercely competi-

tive. In the verification market, Asix is going up against the likes of Cadic, Hewlett-Packard, HiLevel Technology, Integrated Measurement Systems, and Tektronix. Cadic, HiLevel, and IMS have all either been acquired or have received an infusion of capital from other companies. In fact, Asix is the only player funded solely by venture capital.

The production testing market is even tougher. Asix is in the automatic test equipment market, selling production testers to IC manufacturers. Heavyweights in the ATE market include Advantest, Ando, LTX, Megatest, Schlumberger, Semiconductor Test Systems, and Tera-dyne. Japanese equipment manufacturers are hotly contesting a market once dominated by U. S. companies.

Technologically, what first made Asix successful in the verification market is that its test system has a dc parametric unit, which tests the performance of a device under adverse conditions, such as excessive or inadequate voltage, excessive temperature, and so on. This instrumentation, typically found on production test systems, was not part of early ASIC verifiers, although it is now.

Rogers of Hambrecht & Quist says there is a crying need for lower-cost testing solutions in the production test market. The average cost of these test systems now tops \$1 million. A company with a lower-cost solution could grab a big share of the market, she asserts.

That contention is certainly borne out by Asix's customer base, which on the production testing side includes VLSI Technology Inc. of San Jose and LSI Logic Corp. of Milpitas, Calif. LSI Logic and Asix have jointly developed software that automatically creates test programs using the information in LSI Logic's data base. The Asix system creates full program sequences, test vectors with timing information, and all dc parametrics for ASIC testing.

With money in the bank, a good marketing strategy, and a growing customer base, Asix appears to have all the momentum it needs to become a star in Silicon Valley. The only thing that remains to be seen is whether it has the stamina to continue the climb.  
—Jonah McLeod

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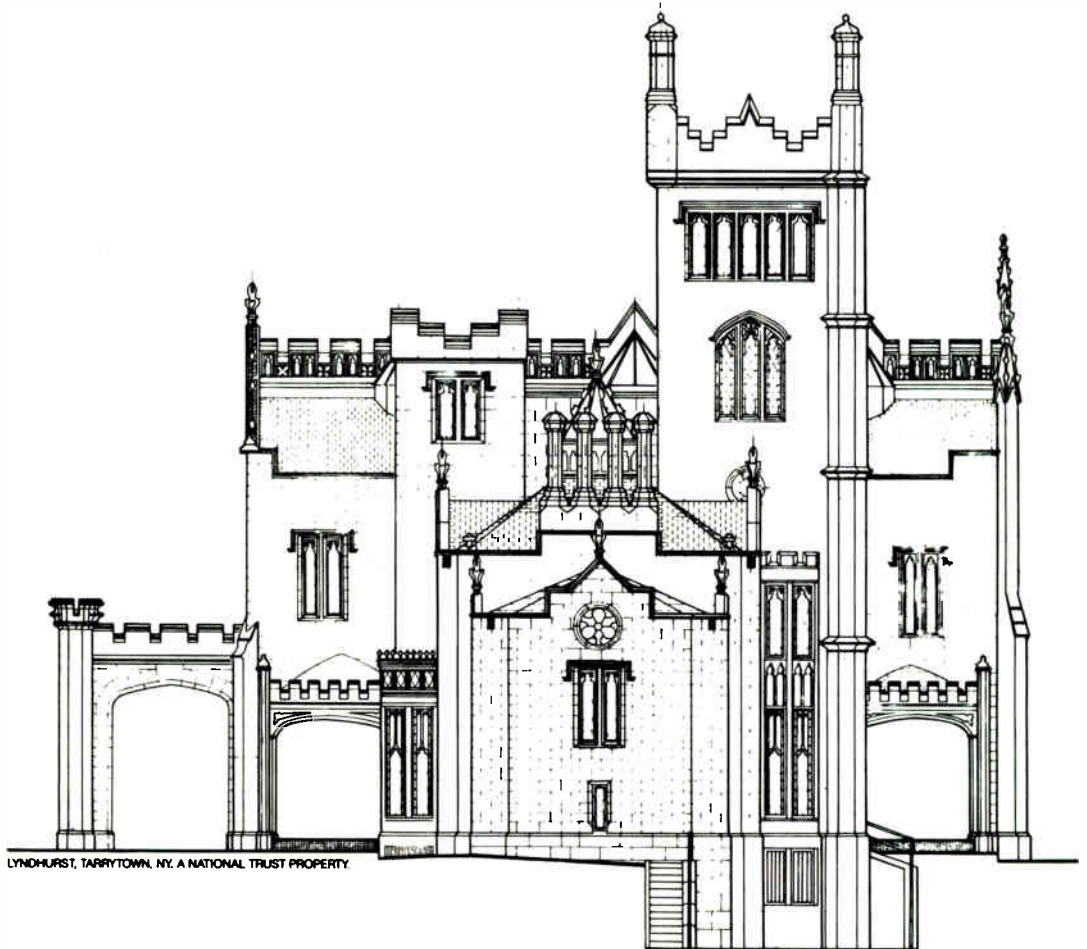
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# PEOPLE TO WATCH

## FURY'S STARTUP HEWS TO HIS CREDO: BE FIRST AND BE NECESSARY

Power Integrations aims to bring smart power into the mainstream

### MOUNTAIN VIEW, CALIF.

**A**rt Fury has never been one to hesitate when he spots a good idea. Once a technology proves itself in the laboratory, he moves quickly to bring products to market. "If you want your products to succeed, it is important not only to be there first with a technology capability that no one else can offer, but also to define a set of products that are ubiquitous and hard to replace," he says.

Fury, a veteran of almost 25 years in the semiconductor industry, is bringing that philosophy to bear in his new role as cofounder of startup Power Integrations Inc. in Mountain View. Founded just a year ago, the firm is now introducing its first products in the high-stakes smart power arena (see p. 107).

Fury is hoping to duplicate his earlier successes as a marketer of power semiconductors and analog circuits from 1969 to 1976, when he worked at Fairchild, National, and Signetics. At those companies, he was responsible for a number of high-volume linear products, including the 555 timer, the first phased-locked-loop integrated circuits, and the first Dolby ICs. Fury then signed on for a nine-year stint as vice president of marketing at Siliconix Inc., where he was responsible for introducing the first MOS power transistors in the industry.

In early 1988, while working as an independent consultant at Data General Corp.'s Semiconductor Division in Sunnyvale, Calif., he met Klaus Eklund, who had developed a power MOS-FET technology "with capabilities unlike anything I had come across in the industry," says Fury. With the blessing of Data General, Fury and Eklund developed a business plan, and by May 1988 had founded Power Integrations and attracted the attention of a number of blue-chip backers.

The startup is already moving into limited production on three products, precursors of a half dozen or so offerings it expects to introduce by year's end. A proprietary high-voltage power CMOS technology developed by Eklund serves as the company's foundation. It sports p-channel MOS FETs that can handle up to 300 V and n-channel MOS FETs that can handle up to 400 V and which in some cases can



After 25 years in the semiconductor business, Art Fury is running a startup maker of smart power devices.

operate directly from the ac power line.

The new technology holds significant size, performance, and cost advantages over present power and smart power MOS-FET technologies, Fury says. In terms of die size, it yields devices that are anywhere from one half to one sixth the size of competitive designs.

Unlike present power MOS-FET technologies, Power Integrations' technique allows for the fabrication of devices with threshold voltages of only 1 V. This

means devices can be controlled from standard 5-V logic, Fury says, whereas today's power MOS FETs typically require a drive voltage of 10 to 15 V. The new technology also features capacitances that are two to four times lower, which with the 5-V gate drive reduces power requirements by an order of magnitude.

But the most impressive aspect of the new process, Fury says, is that it yields p-channel power MOS FETs that are only 50% larger than n-channel devices. P-channel MOS FETs made with current techniques are typically three times larger than n-channel devices.

Fury has a two-pronged strategy to move this technology quickly into the mainstream. For the short term, Power Integrations is readying improved versions of a variety of industry standards in high-volume applications. For long-term growth, it is using its technology to develop unique products. This month, the company will introduce the PWR-DRV1, a universal relay and solenoid driver that Fury expects to become as ubiquitous as the 555 timer.

—Bernard C. Cole

## SUN RISES IN THE EAST UNDER AVERY'S DIRECTION

### BILLERICA, MASS.

**I**t's no secret that Sun Microsystems Inc. is one of the hottest technology companies in the U. S. The Mountain View, Calif.-based leader in the engineering work-station business saw its revenue grow 96% last year, breaking the \$1 billion mark. What isn't widely known is that Sun's East Coast Division is one of the hottest operations in the company. That division is responsible for the Sun 386i work-station family, which in its first year of availability contributed an astounding \$150 million to Sun's revenues.

Sun's East Coast Division is now headed by William Avery, an affable 49-year-

old career engineer and engineering manager. In February, Avery was named vice president and general manager of the Billerica-based division—a move that Avery says fulfilled a decade-long desire to run his own organization. "I've done engineering management my entire career," he says, "but I've had a strong desire to break into general management."

Most recently, Avery served as senior vice president for product development at Encore Computer Corp. in Marlborough, Mass. Before that, he was director of central processor development at Data General Corp. in Westboro, Mass., and spent 10 years at Digital Equipment Corp. in

# New Power in Waveform Acquisition and Analysis

Unique software helps make the System 500 "turn-key" ready

At first glance, Nicolet Instrument's unveiling of its new System 500 seems newsworthy because of the 500's industry-leading hardware. Indeed, in the world of waveform acquisition and analysis, where more is better, the System 500 is in a class by itself. The 500 has more channels, more memory, more speed and more resolution.

Each digitizer board, with its own independent trigger circuitry, time base and up to 1 megasample record length, is worthy of a full review. This multi-channel system can be configured to have as many inputs you need — up to several hundred. The digitizer boards are designed to be the equivalent of having a 12 bit digital scope on a card.

## Turn-key system

But after you get your hands on the System 500, the most important news becomes apparent. Someone has finally developed a very powerful, competitively priced system for waveform acquisition and analysis that truly is a "turn-key" system.

You literally can take this system out of the box, plug in the power cord, connect the GPIB cable between the acquisition unit and the controller, and turn it on. The System 500 is now ready to take data. This turn-key readiness promises to save time by considerably reducing the learning curve needed to perform complex waveform acquisition and analysis.

## Intuitive windows software

The primary reason for System 500's easy operation is Nicolet's unique software which operates under Microsoft Windows/386®. The powerful Nicolet software can easily be controlled through pulldown menus that can be accessed by mouse or keyboard.

Measuring waveforms becomes as simple as pointing to the data point of interest on a waveform and clicking the mouse — the voltage and time values for the selected point is

immediately displayed on the screen. By using the Delta Numerics function relative measurements like peak to peak or rise time can easily be made.

Also, Nicolet's unique software, combined with the System 500's built-in processor and co-processor, make incredibly fast waveform processing and analysis possible.

## Local processing

While other data acquisition systems need to transfer data to another computer for analysis, Nicolet has built calculation capabilities into the new System 500. Complex calculations can be performed on acquired data as it resides in the digitizer's memory.

There is no need to transfer data to a computer for analysis, no need for complex programming to handle normalizing sets and long record lengths. Functions are performed on the powerful 32 bit processors with a few clicks of the mouse. This local processing of data greatly decreases the time it takes to generate answers.

The bottom line is that the System 500 is a unique turn-key waveform acquisition system. For full details you'll need to read the product brochure.

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Maynard, Mass., in various engineering management positions. "After 10 years at Digital—which I never thought I'd leave—I decided that I'd have to run my own operation," Avery says.

He now has his chance. His charter, Avery says, is "to develop the Intel [Corp.] architecture and get Sun into new applications where it wouldn't get with technical work stations." That means helping customers migrate from DOS-based personal computers to a Unix platform, or enabling them to run both operating systems, which the 386i does.

Avery says that Intel—developer of the 80386 processor used in the 386i—is one company that is benefiting from his division's ability to "take work-station technology and move it into markets that are combinations of DOS and Unix." The Santa Clara, Calif., company recently selected the Sun 386i as the standard desktop work station for its circuit-design department. An agreement with Sun calls for delivery of several hundred of the machines in the next two years.

Aside from the challenge of managing an entire business, Avery is looking forward to developing new markets for his company. He doesn't want the division to be a one-product operation, so even as he sets his sights on insurance and financial-services customers, which he believes are outgrowing their DOS machines, Avery is eyeing new products.

That's okay by Sun, which, Avery says, established its East Coast Division in 1985 to develop a low-end work station for customers other than its technical users. One of the reasons that Sun moved east, Avery says, is that management realized that the West Coast doesn't have a monopoly on technical talent. Massachusetts "is the other area where engineering talent is readily available," he says. And Avery plans to use that talent to keep Sun from becoming a one-product company.

—Lawrence Curran



Sun's William Avery has finally satisfied his yen to break into general management.



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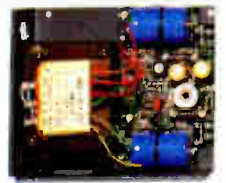
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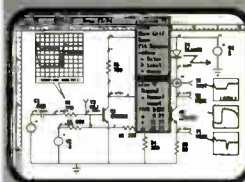
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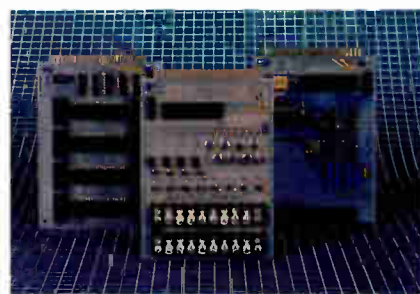
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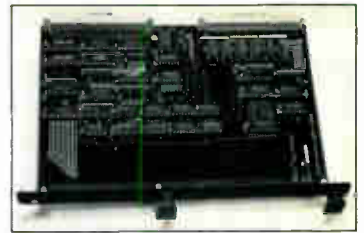
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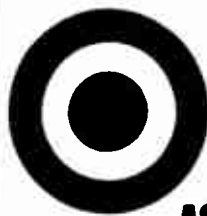
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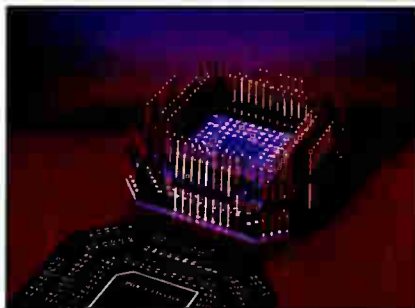
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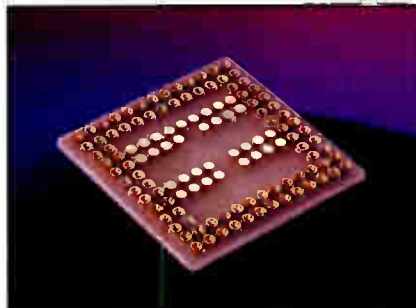
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## UPDATE: GALLIUM ARSENIDE BREAKS THROUGH, FINALLY

If the track record of the few semiconductor startups over the past year is any indication, gallium arsenide is no longer the industry's 98-pound weakling. Last June, companies such as Gazelle Microcircuits, Gigabit Logic, and Vitesse Semiconductor announced a new generation of 1.0- $\mu\text{m}$  and submicron digital GaAs processes that, the chip makers said, would compete directly with bipolar and biCMOS emitter-coupled-logic, TTL, and CMOS products [*Electronics*, June 1988, p. 65]. And it looks as if those companies are well on their way to their goals.

Gazelle threw down the gauntlet to makers of high-speed and low-power programmable logic devices with the industry's first programmable-logic-array circuit based on GaAs. The Santa Clara, Calif., company chose as its vehicle the industry-standard 22V10, a 24-pin PLA device with 10 outputs that can accommodate an 8-bit word plus 2 control bits. When the GA22V10 was introduced, its raw speed immediately captured the attention of system designers. With an internal clock rate of 90 MHz, the device far outpaced the 30-to-37-MHz clock rates of silicon bipolar implementations from the likes of Advanced Micro Devices, National Semiconductor, and Texas Instruments.

Within weeks, makers of silicon PLDs rushed to market with parts that matched Gazelle's for speed. But Gazelle countered with new GaAs devices that pushed clock rates up to 110 MHz and propagation delays down to 7.5 ns, from an already low 10 ns. Even faster versions are now in development, says David MacMillan, Gazelle's vice president of marketing. "The advantage we have," he says, "is that where silicon PLD makers are pushing the limits of their process to gain higher speeds, we actually have had to throttle back the performance of our circuits to make them compatible with TTL signal levels." Gazelle is also putting price pressure on its competitors. From an initial \$48 each in 1,000-piece quantities, the price dropped two months after introduction by almost 25%, to \$35. Further cuts can be expected, says product marketing manager Robert Gunn.

Gazelle has added to its PLD product family with a GaAs version of the 23S8, targeted at state-machine and sequencer applications. When using its six buried registers for internal feedback, Gunn says, the device can run at clock rates of 165 MHz, compared with 40 MHz for equivalent silicon-based chips. Using external feed-

back, the GA23S8 can run at 95 MHz, compared with 33 MHz for its silicon counterparts, he says.

According to MacMillan, Gazelle intends to focus on the TTL bipolar and CMOS markets, pushing competitive silicon devices not only in speed but also in density. He adds that Gazelle has achieved hundreds of design wins. "Within a few months, as some of these designs come to the market, everyone will be surprised at how widespread the use of GaAs PLDs has become in solving speed bottlenecks in computer-based systems," he says. They range from personal computers to work stations and superminicomputers.

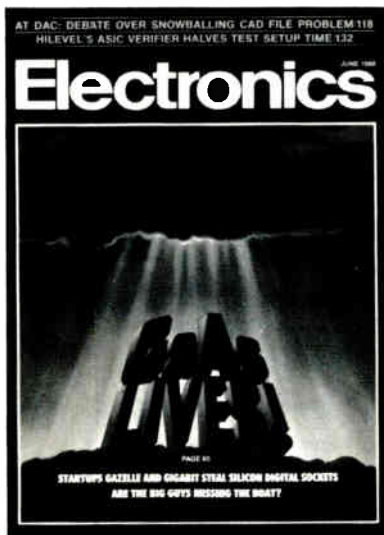
Meanwhile, Gigabit Logic Inc. and Vitesse Semiconductor Corp. are making inroads in the ECL marketplace with standard-cell and gate-array GaAs offerings that are as dense as bipolar silicon devices. Last November, the Newbury Park, Calif.-based Gigabit began sampling the 12G044, a 1-K-by-4-bit static random-access memory with an incredible 3.5-ns cycle time, about twice as fast as equivalently sized bipolar ECL SRAMs. That same month, Gigabit also announced its 10,000-gate GaAs standard-cell array family, which allows designers to create 10,000-gate circuits operating at up to 4 GHz.

These devices feature loaded gate delays as low as 50 ps and dissipation as low as 100  $\mu\text{W}$  per gate—both of which are 10 times lower than equivalent bipolar ECL implementations. And the average price is 5 cents a gate, down sharply from the 10 to 15 cents for earlier GaAs arrays, says vice president of marketing Michael Pawlik. "With ECL prices ranging from 2.5 to 5 cents per gate, we have closed in on silicon very quickly."

Matching Gigabit gate for gate in density and speed, Vitesse Semiconductor of Camarillo, Calif., has zoomed up the density curve in both gate arrays and standard cells. Using its proprietary 1.0- $\mu\text{m}$  enhancement and depletion GaAs process, Vitesse has pushed densities from its initial 4,500-gate-array offering up to 15,000 gates. By year's end, the company says, it will get as high as 30,000 gates.

But Vitesse is making its most impressive gains in the standard-cell arena. In January it introduced a new cell family that director of marketing Tom Dugan says boasts integration levels as high as 22,000 gates at twice the speed of comparable ECL products but using a quarter of the power. The VCB50K series cell library has been optimized for performance at clock rates of up to 3.5 GHz.

By the end of this year, says Dugan, cell-based offerings as high as 50,000 gates should be possible. Overall, he says, Vitesse has more than 100 gate-array and cell-based designs in development. —Bernard C. Cole



While silicon chips are hitting their limits, GaAs devices are just getting started



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