IS THE SEARCH FOR RAD-HARD CHIPS ON TRACK?/82
THE PROMISES AND PITFALLS OF HIRING TEMPORARY HELP/91

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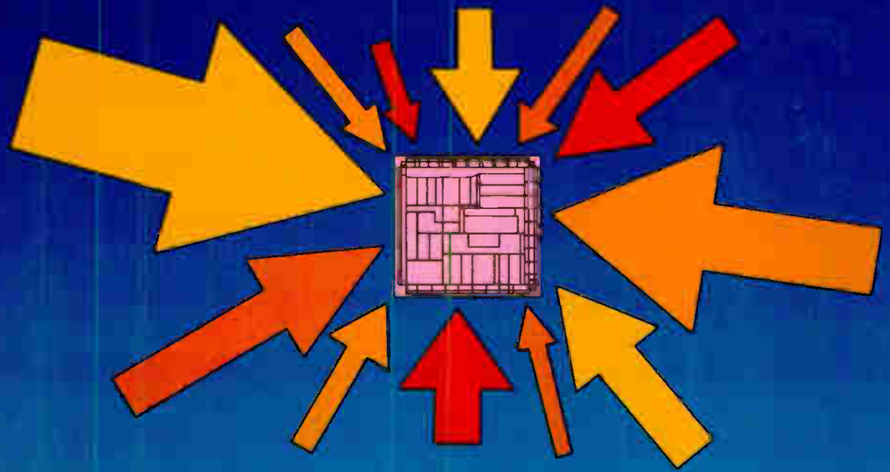
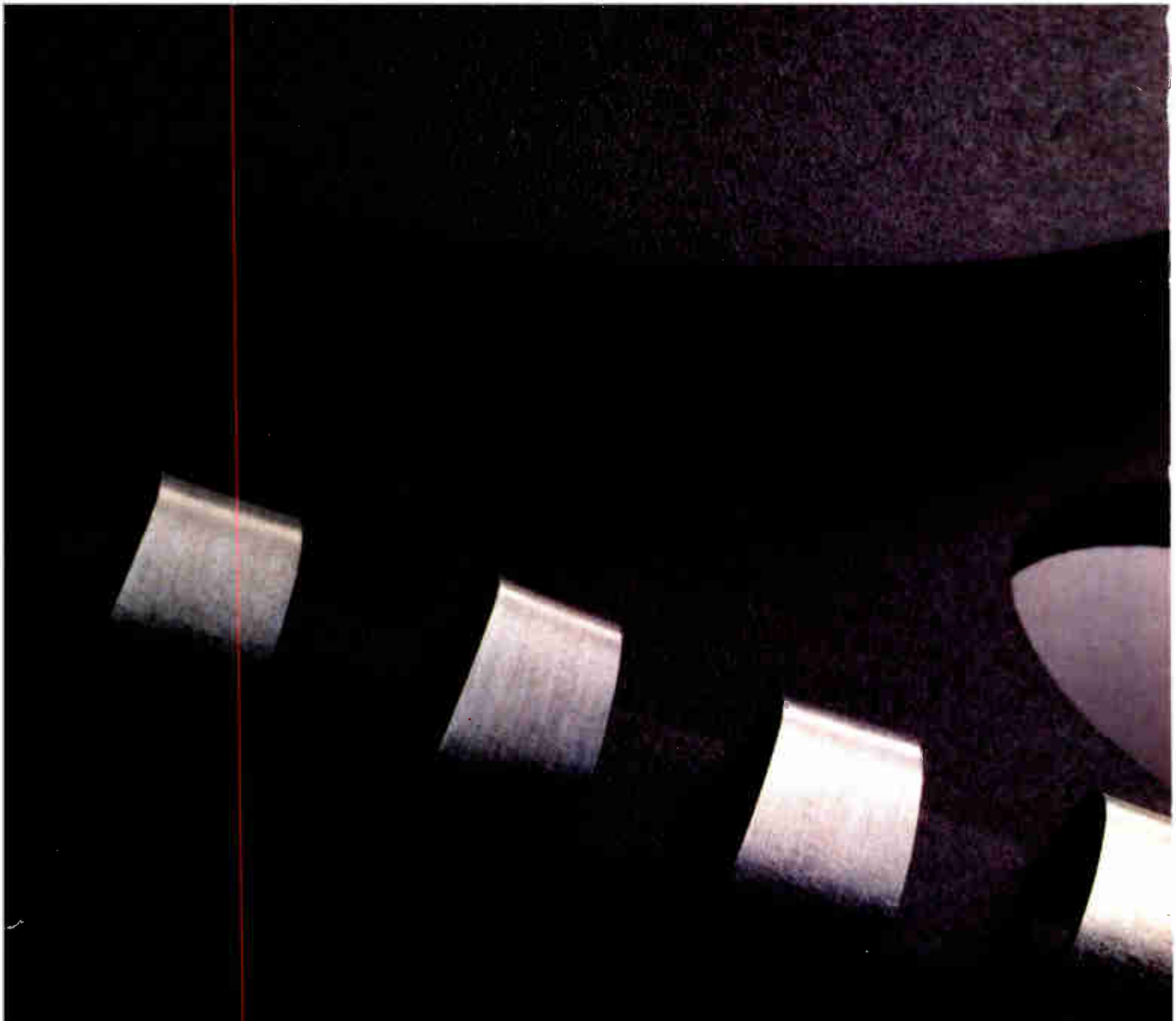


MICROPROCESSORS

PAGE 70

RISC, CISC, AND CRISP—THEY ALL MEAN MORE POWER, MORE SPEED, AND MORE FEATURES, BUT HOW DO YOU CHOOSE?



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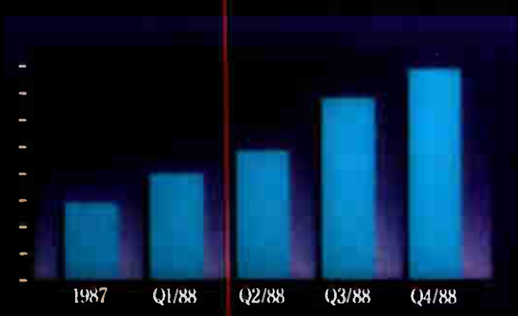

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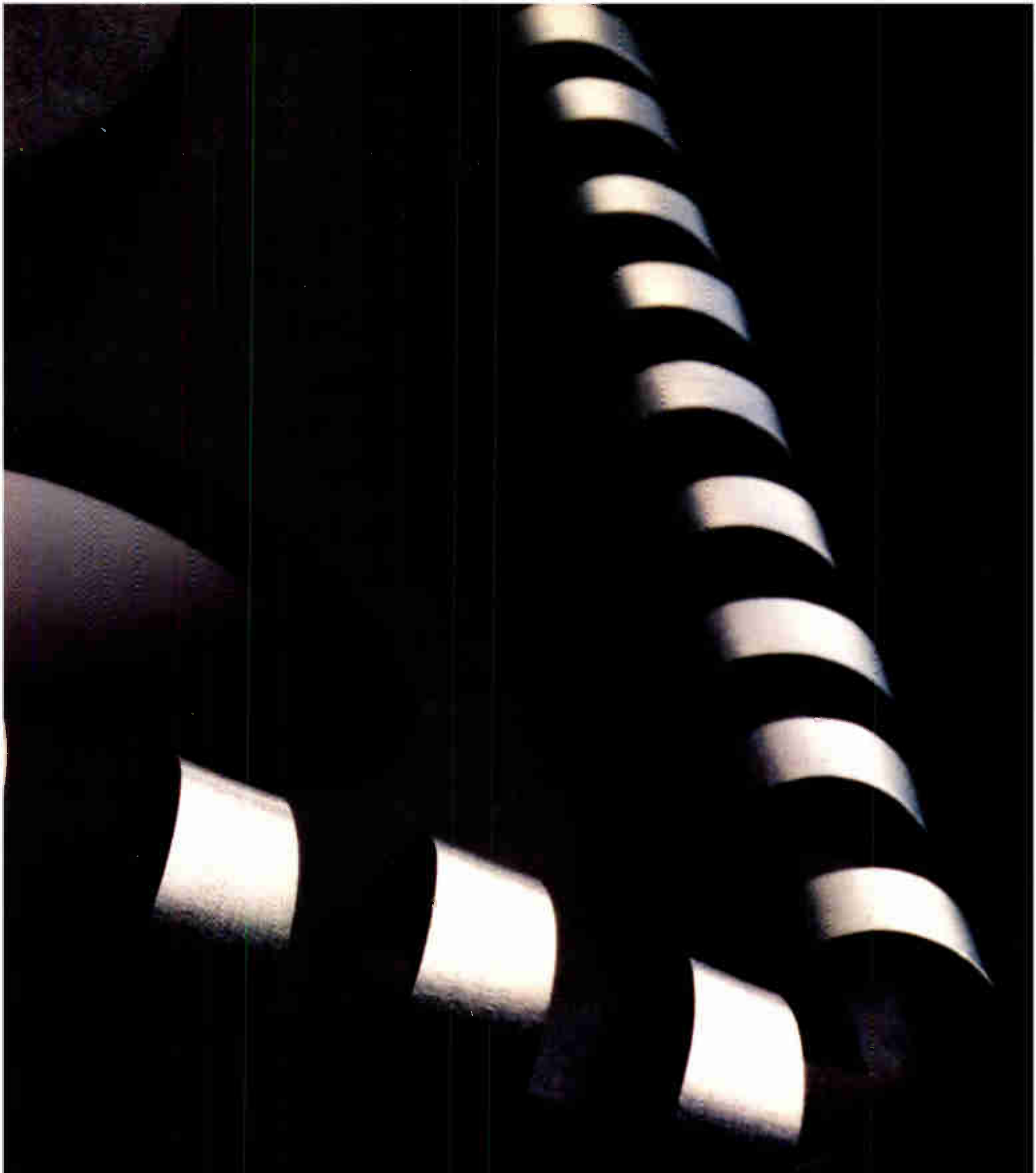

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	AK93C47(F)	2.5V	2.5V				89/8
2K	AK93C56(F)	—	—	128×16	Serial	8Pin DIP SOP	89/8
	AK93C57(F)	2.5V	2.5V				
4K	AK93C66(F)	—	—	256×16	Serial	8Pin DIP SOP	89/7
	AK93C67(F)	2.5V	2.5V				
16K	AK28C16(F)	—	—	2K×8	Parallel	24Pin DIP SOP	89/5
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Circle 40

SO YOU'VE GOT A MILLION TRANSISTORS

As a new communications art form, today's mega-microprocessor announcements are a tough act—of faith—to follow

We are about a month shy of announcing a full line of components based on deuterium-enriched palladium. However, even if we had that story in the bag, it would still probably have yielded up this issue's cover to the microprocessor report (p. 70). No matter how you cut it—RISC vs. CISC, Intel against Motorola, quantum leaps for hardware opposed to the Black Hole of lagging software development—the microprocessor circus is today's hot ticket.

There was a time when you could say with certainty that, as an industry-wide syndrome, the marketeers were constantly co-opting the techies. Now, very possibly, things have swung the other way. Processor performance has outstripped even the ad writers' capacity for the appropriate hyperbole. For example, the frustrated wordsmith charged with polishing one trade ad for Sun's new SPARCstation could but refer to its "blinding speeds"—which is certainly an attribute I would prefer not to see (pardon the pun) in *my* work station. At the same time, responsible, technically grounded managers like Intel's microprocessor chief, David House, can look you right in the eye and promise, because his company's new 80486 is such a wonderfully compatible chip off the old block, to "protect your $15 billion software investment."

I don't know of any discrete organization—even one that might have paid full price—with anything like $15 billion tied up in software. House can be excused, of course, because he was—or believed he was—addressing an entire universe.

It is not wrong to think in terms of marketing to a universe. It could be a trap, however, to forget that universes are composed of individual users. Individual users who, over the course of the ensuing year, will have an opportunity to discover for themselves that mips can be manipulated, flops will fluctuate, that pipelines can stall, and that a superfast CPU coupled with available commodity RAM can amount to a floating submarine. Thus, from that perspective, does the power and glory of the typical new microprocessor run downhill, these days, from the time of its introduction. The higher its raw, naked power at birth the more it may seem, in eventual system configuration, to degrade.

All of which is to say that, ultimately, the delivery of total systems performance—real-world value—is what will determine the true merit of these wonder chips. It may be worth pausing to consider something that used to be called the home-computer market. According to the San Francisco consulting firm Volpe & Covington, American households are currently throwing out computers at the rate of 1.3 million per year, or about one for every three that are being installed. These are mostly toylike machines, many that cost less than $500, bearing little resemblance to the PCs people buy for home use today. But inside some of them you'll find microprocessors that were called, in their day, miraculous.

ROBIN NELSON

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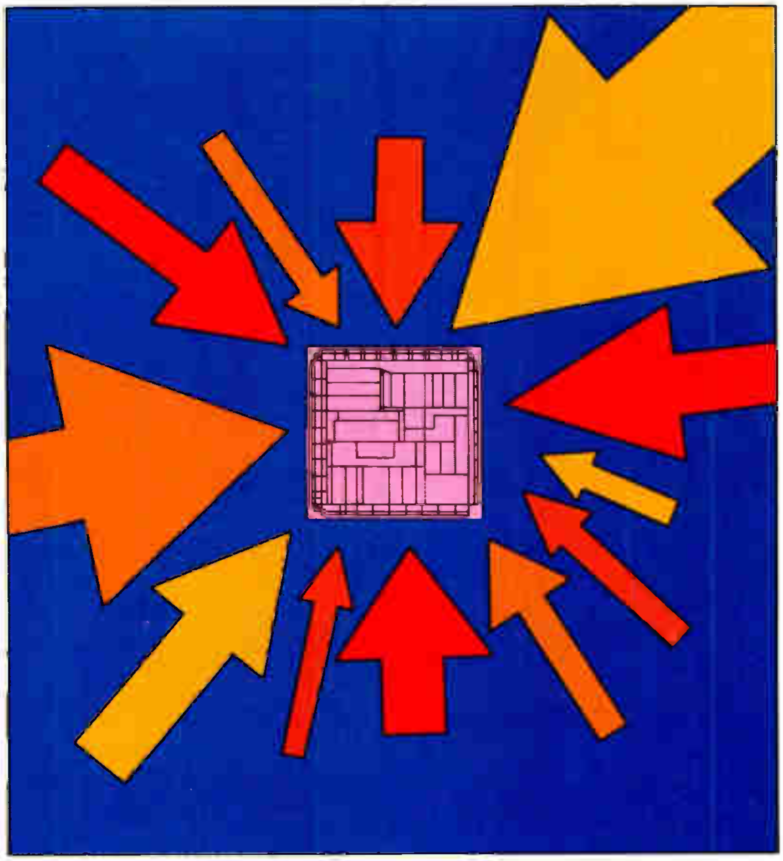

PAGE 70

WORLDWIDE NEWS ANALYSIS

COMPANIES TO WATCH

PEOPLE TO WATCH

DEPARTMENTS

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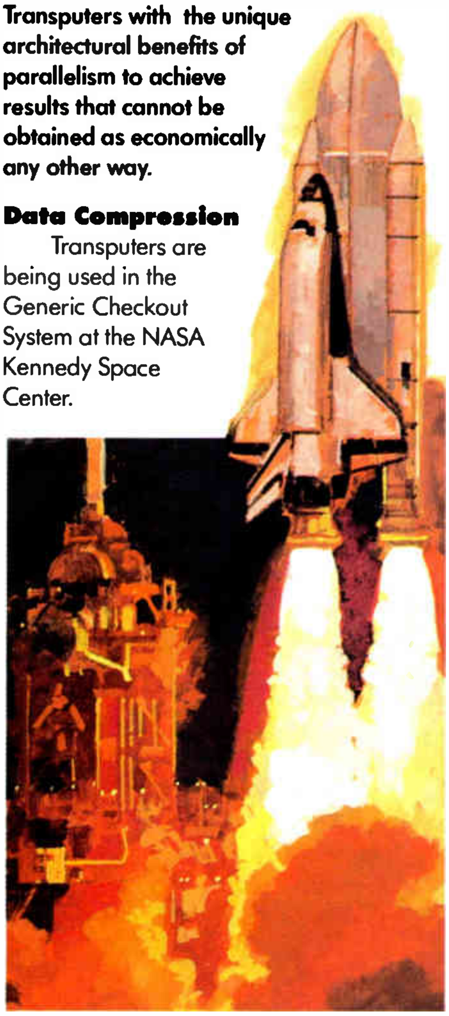
Circle 9

Circle 18

"OK...SO THE TRAN
BUT WHAT ABOUT I

They're everywhere. Worldwide over a thousand Transputer designs are in today's marketplace or are entering production. Some belong to Fortune 500 companies committed to using Transputers to build their next-generation products.

Although Transputer applications are diverse, the theme for each is the same – combining the power of individual Transputers with the unique architectural benefits of parallelism to achieve results that cannot be obtained as economically any other way.



Data Compression

Transputers are being used in the Generic Checkout System at the NASA Kennedy Space Center.

They are embedded within VME based front-end Data Acquisition Modules to provide data filtering for the system.

These modules pre-process data for a network of Unix based workstations that provide real-time control and monitoring of ground and flight equipment, like that used by the Space Shuttle. Only Transputers offered the degree of parallelism needed for this application.

Medical Imaging

University College London is using the parallel processing power of Transputers to convert CAT, NMR and laser scans into rotating 3-D images. These facial, skeletal, and soft-tissue images provide accurate computerized measurements to assist doctors with each step of an operation, and are also used by plastic surgeons to 'rehearse' operations for reconstruction.

Data Collection

British Steel is implementing an intelligent system that is designed to dramatically cut its multimillion dollar annual energy costs. It is built around T800 floating point microprocessors which process information from a highly complex data gathering system. These Transputers operate in parallel, condensing enormous amounts of data into information which helps energy management decide how to respond to a plant's changing demands for different fuels.

Data Transmission

Kokusai Denshin Denwa (KDD), the Japanese international telecommunications company, has developed an image-processing video telephone using Transputers to manipulate and condense images for transmission over telephone links.

This image communications system uses 32 Transputers operating in parallel for ultrafast image processing. It can be connected to PC's to transmit images over telephone lines, function as a video phone, or be programmed to match the specifications of other receiving equipment, such as facsimile machines and TV monitors.

Space

The European Space Agency is using Transputers to build a light-weight, radiation-tolerant, on-board computer for spacecraft. Programs which utilize Transputers in scientific computing and spacecraft control applications are also being developed in the U.S.

Transputers are manufactured on epitaxial silicon and have been shown to withstand aggressive tactical radiation levels.

PUTER'S TERRIFIC,
AL APPLICATIONS?"

light Simulation

British Aerospace have used Transputers to develop a low-cost flight simulator comprising a flat world, ground-grid, buildings, trees and mountains – with an optional Head-up display. Future enhancements will include the addition of undulating terrain and a single or triple window display option.

American companies are also using Transputers to build high-performance flight simulators more cheaply. One U.S. manufacturer utilizes over one thousand T800 processors per system.

3-D Rendering

Pixar in the US has developed a Transputer-based rendering system which quickly renders photorealistic images from 3-D models. The system consists of Transputer boards for VME and AT-bus systems optimized to run Pixar's sophisticated rendering software.

The system holds great promise for such applications as architecture, automobile styling, package design, simulation as well as animation. Pixar's recent computer generated film 'Tin Toy' could not have been done without using this Transputer-based accelerator.

System Control

As the number of Transputers in a system design are increased, a proportional increase in performance can be achieved.

In West Germany, Parsytec GmbH is using this principle in their Megaframe Superclusters. Superclusters represent a complete series of reconfigurable industrial control boards as used in the automotive industry, which exploit the Transputer's parallel processing capability.

The basic Model 64, built with T800's, has a performance of 640 MIPS and 96 MFLOPS. The Model 256 comprises four Model 64 cabinets connected by cables and provides 2,560 MIPS and 384 MFLOPS.

Parsytec believes there is no limit to the size Superclusters can grow to. Two Model 256s can be combined easily to realize twice the raw performance of one system.

Robotics

Transputers are ideally suited for robotics applications because their special on-chip links make communication between control centers naturally easy. They are often used in the central control area for dumb robots, in multi-jointed robots, and in machine vision systems.

At the Houston Space Center, NASA and Lockheed are using Transputers in the development of an intelligent, self-manoeuvering, voice-controlled robot named EVA Retriever. EVAR is being built to investigate the autonomous retrieval of objects and astronauts that become detached from the Space Station.

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Circle 10

been hit by layoffs. The company now has 4,000 employees on the Island—down from a peak of 5,500 in 1987, says spokesman Dick Dunne.

Problems of another sort have stymied Unisys Corp., the Blue Bell, Pa., computer maker, which has offices in Great Neck, as well as Hazeltine Corp. in Greenlawn. Both have been locked out of bidding on new defense contracts until allegations arising from the Operation Ill Wind procurement investigation have been settled.

Some smaller companies have been nimble enough to prosper. Astro Systems Inc., a manufacturer of custom-designed military power supplies in Lake Success, has fashioned a survival strategy around using state-of-the-art technology and finding opportunity where it arises. "We work with large defense contractors in the Midwest, California, and Boston," says Sol Ginzberg, director of military product marketing. "We have good contacts with whoever gets the contract." While other companies move manufacturing offshore, Astro Systems has found a solution closer to home—20 minutes away, in fact, in Jamaica, Queens.

ILC Data Device Corp. in Bohemia has leveraged technology and opportunity in a similar fashion. This maker of hybrid circuits—mostly for defense—keeps its competitive edge by designing its own monolithics, says Jim Sheahan, senior vice president of marketing. The U. S. market—which accounts for 65% of ILC's business—is flat, but ILC's presence in Europe is growing.

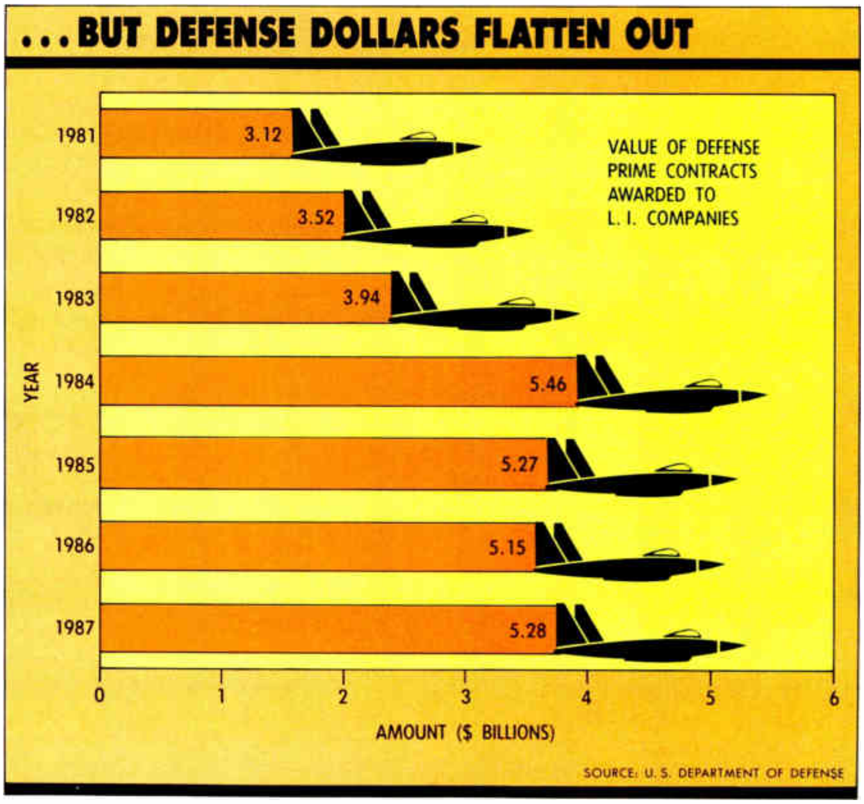
ILC does share one problem with other Long Island-based electronics firms: despite all the layoffs, there's an acute shortage of production workers. "There's 2% unemployment in Suffolk County," Sheahan says. "We have a real problem competing with fast-food restaurants that pay $6.50 to $7 an hour."

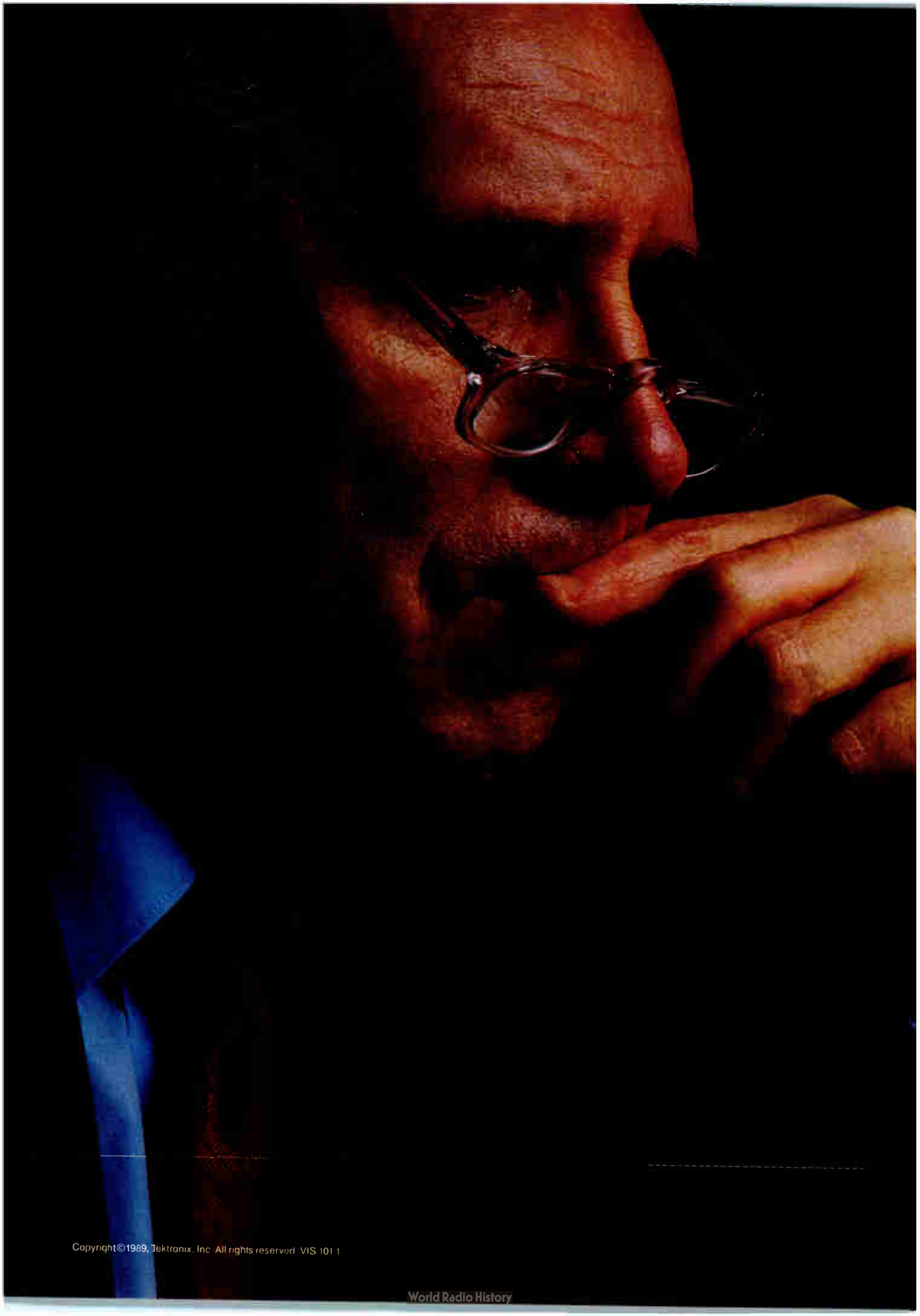
Other bright spots in the electronics landscape here include Computer Associates International Inc., a Garden City-based software house, and Symbol Technologies Inc., a manufacturer of bar-code readers in Bohemia.

GETTING TOGETHER. The problems on the Island have prompted companies large and small to band together to form the Long Island Forum for Technology (LIFT), whose goal is to boost the region's fortunes by networking. The organization, based at the Farmingdale campus of New York's Polytechnic University, will develop a data base holding the manufacturing capabilities, technical expertise, and product-development research going on in member companies. More than 1,000 companies will be represented, says George Soos, president of LIFT. To the corporate data, information about the capabilities resident in Long Island's universities will be added.

The Long Island industry may be struggling, but the shark hasn't gotten to it yet. "Long Island is associated with a good life style," says Soos. "We produce a higher quality of work product plus strong service. Although they might cost a little more, I think that merits attention." *–Jack Shandle*

...BUT DEFENSE DOLLARS FLATTEN OUT





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Circle 49

ELECTRONICS NEWSLETTER

MOTOROLA JUMPS INTO THE IBM PC-CLONE ARENA . . .

It seems pretty strange on the face of it that Motorola Inc. would make products to support the microprocessors of archrival Intel Corp. But the new products are microcomputer chip sets for making IBM Corp. Personal Computer AT clones, which are built around Intel processors. Motorola will market two chip sets for PC AT-compatible machines: one that supports the Intel 80286 and one for the higher-powered 80386 processor. The chips come to Motorola by way of an alliance with ACC Microelectronics Corp. of Taiwan. Motorola's Semiconductor Products Sector in Austin, Texas, has acquired from ACC the rights to manufacture and sell that company's ACC82020 chip set for 16- and 20-MHz PC AT-compatible computers and the ACC82300 set for the 20-to-25-MHz 386 machines, as well as the ACC16C451 family of multifunction input/output controllers. □

. . . AND VIA TECHNOLOGIES LOOKS TO CHALLENGE THE LEADERS

As Motorola gears up to enter the IBM Personal Computer-clone chip-set market, one of the sector's established players—Via Technologies Inc. of Fremont, Calif.—is pitting its next generation of chips against those of market leaders Chips & Technologies, G2, and Intel/Zymos. Via's modular SL90XX Generic PC AT Core Logic Set attacks one problem plaguing PC-clone chip sets: partitioning. "Functions that require critical timing and speed, such as high-speed memory control, have typically been spread over the multiple chips in the set," says Idris Kothari, vice president of engineering. Making all these chips fast enough can destroy any price advantage the chip set would have over a discrete solution, he says. Via is putting all the critical timing functions on one high-performance universal-clock chip. A core logic set that doesn't require critical timing is also offered; it can be used in all Intel 80286- and 386SX-based computers, as well as in 386 systems using the AT bus. The Via chip set includes four controller chips—one each for the system, data, addresses, and peripherals—and memory-controller chips that can be tailored to a specific system-design architecture. The result, claims Via, is a chip set with optimum partitioning that offers the right performance for each PC system, at a cost below that of discrete parts. □

CONTROL DATA BOWS OUT OF THE SUPERCOMPUTER BUSINESS

The supercomputer business is getting so competitive that even the pioneer of supercomputing can't keep up the pace. Control Data Corp., which as the inventor of supercomputers has been in the business longer than any other company, announced last month that it was discontinuing its ETA Systems supercomputer division. The Minneapolis-based computer maker had spun off ETA Systems as a separate company about five years ago to build the follow-on to Control Data's Cyber 205 supercomputer. At the time, Control Data hoped to get additional financing for ETA by selling part of the operation to other investors. Although outside money didn't exactly flow freely, Control Data kept ETA Systems going by funding the ETA-10 development project, with the aim of building the world's most powerful supercomputer, itself. The spin-off company successfully developed a broad family of very powerful parallel supercomputers using high-density CMOS technology, a development effort that culminated in the mighty ETA-10 machine. But sales lagged, and last October Control Data brought ETA Systems back into the fold as a division in an attempt to stem the losses. Competition from Cray Research Inc. and Convex Computer Corp. in the U. S. and looming competition from the biggest Japanese computer companies inflicted severe losses on ETA Systems. Control Data won't say what it spent on ETA, but the company acknowledges losing $100 million in the supercomputer business last year. □

ELECTRONICS NEWSLETTER

TDK'S ACQUISITION BID REKINDLES JAPANESE INTEREST

If successful, the proposed acquisition of Silicon Systems Inc. by Tokyo-based TDK Corp., the first such pass at a U. S. chip firm in more than two years and expected to be completed by summer, could augur more such deals—done even faster. What has snagged Japanese purchases of U. S. technology companies since late 1986 is the fallout from Fujitsu Ltd.'s abortive attempt to take over Fairchild Semiconductor. U. S. government officials nixed it on the grounds of military security because Fairchild supplied key integrated circuits to defense programs. This failed bid effectively killed any plans of Japanese companies to acquire outright commercially oriented U. S. firms, although the Japanese continued to invest in them. The lack of flap over the proposed Silicon Systems acquisition shows that the period of Japanese restraint is over, analysts say. TDK is paying about $200 million, or $20 a share, for the Tustin, Calif., company, which reaps about $121 million in sales from its line of chips for telecommunications gear and peripherals. The price represents a 70% premium over the company's market value at the time of the deal. TDK, with $3.4 billion in sales, is the world's leader in magnetic recording tape. □

COMPACT VIDEO TRANSMITTER DOES AWAY WITH COAX

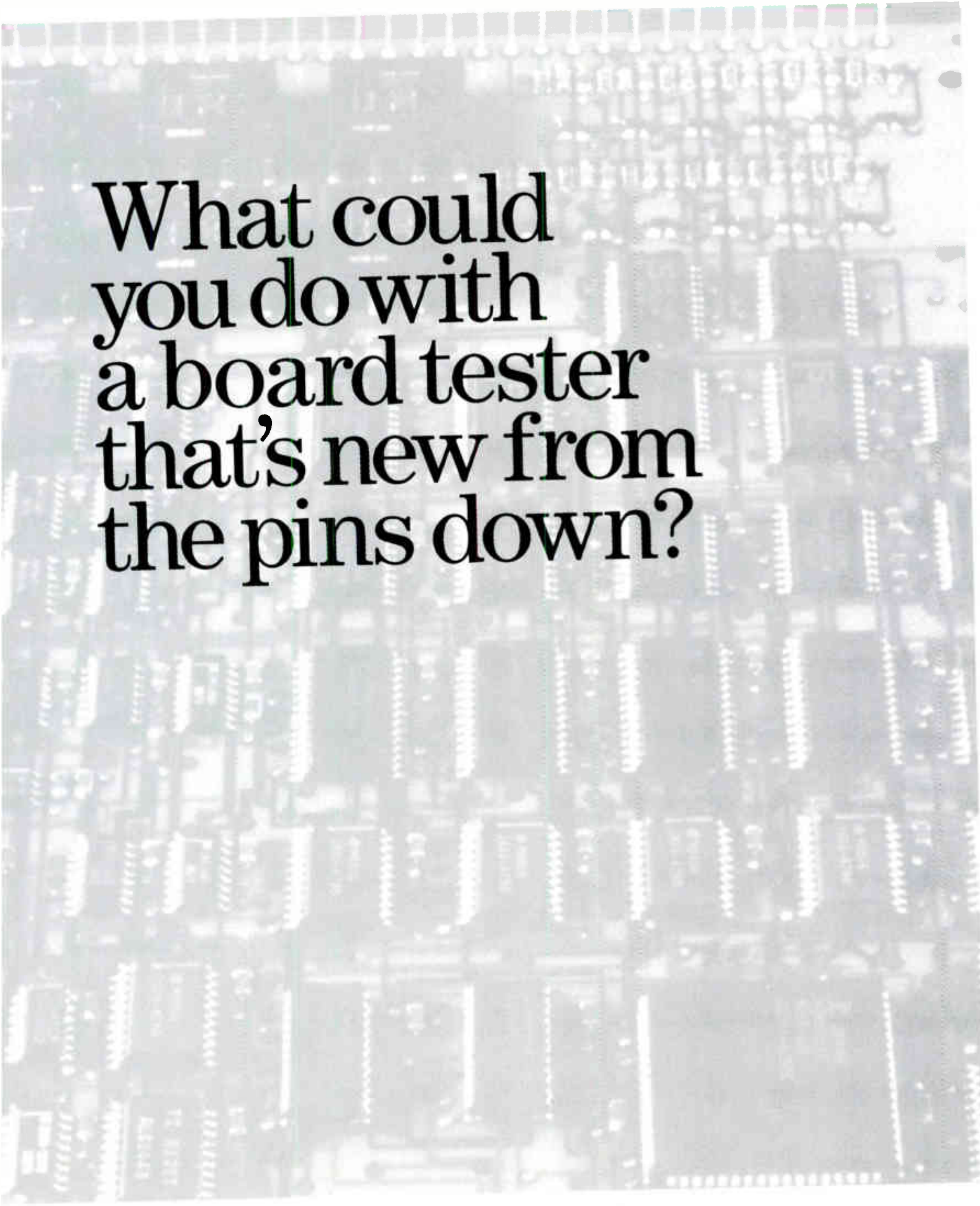
Whose communication equipment using fiber optics has made rapid strides in industrial equipment? If your answer is "PCO Inc.," you're more informed than most, because the hardware so far hasn't caught the public eye. What might be the ticket to bring PCO's promising technology into wider view is a new 2-lb, 3-oz video-transmission package for remote electronic news gathering, security, military surveillance, and other communications tasks. Running for eight hours on a lithium battery, the unit, a first of its kind, is meant to do away with the limitations of heavy coaxial cable, says the Chatsworth, Calif., company. Small enough to be clipped to a belt or attached to a portable camera, the PCO-5050 supplies broadcast-quality links of up to 8 km without repeaters. PCO, jointly owned by Corning Glass Works and IBM Corp., sells the unit for $4,195. □

TRW GEARS UP FOR PHASE 1 GaAs PRODUCTION

TRW Inc. was the only one of four Mimic-program companies to lack a volume production line in the competition to produce affordable gallium arsenide wafers for the military in Phase 1 of the Pentagon's Millimeter Wave and Microwave Monolithic Integrated Circuits program. To remedy that, the Cleveland-based company built a $25 million GaAs pilot production fabrication line at its Manhattan Beach, Calif., plant. The 3-in.-wafer line, slated to begin operating by year's end, will make 100 wafers a week. □

PRIME SOLICITS SUITORS AS IT CONTINUES TO RESIST MAI

Prime Computer Inc. has stepped up its resistance to the months-long unfriendly takeover attempt by MAI Basic Four Inc. by soliciting proposals from other prospective buyers. In this latest of several so-far successful moves to prevent being purchased by MAI, Prime, of Natick, Mass., has asked its financial advisers to "vigorously pursue" suitors willing to pay more than the $20-per-share tender offer from MAI, which is based in Tustin, Calif. Those advisers are The First Boston Corp. and Smith Barney, Harris Upham & Co. Prime continues to advise its stockholders against tendering their shares to MAI, and has rescheduled its annual stockholders' meeting from May 12 to June 14 in the hope of attracting a more favorable deal for shareholders to consider. □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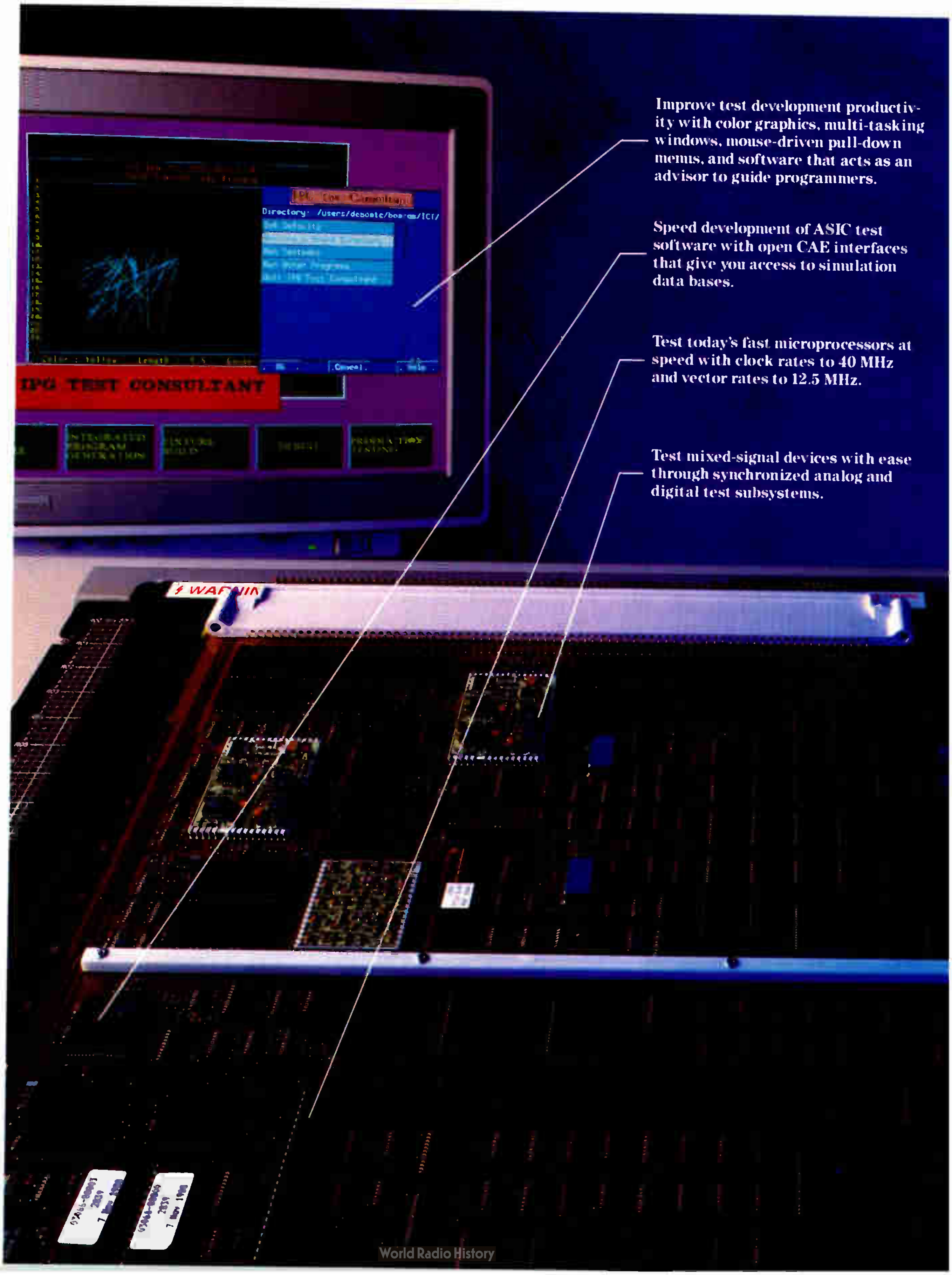
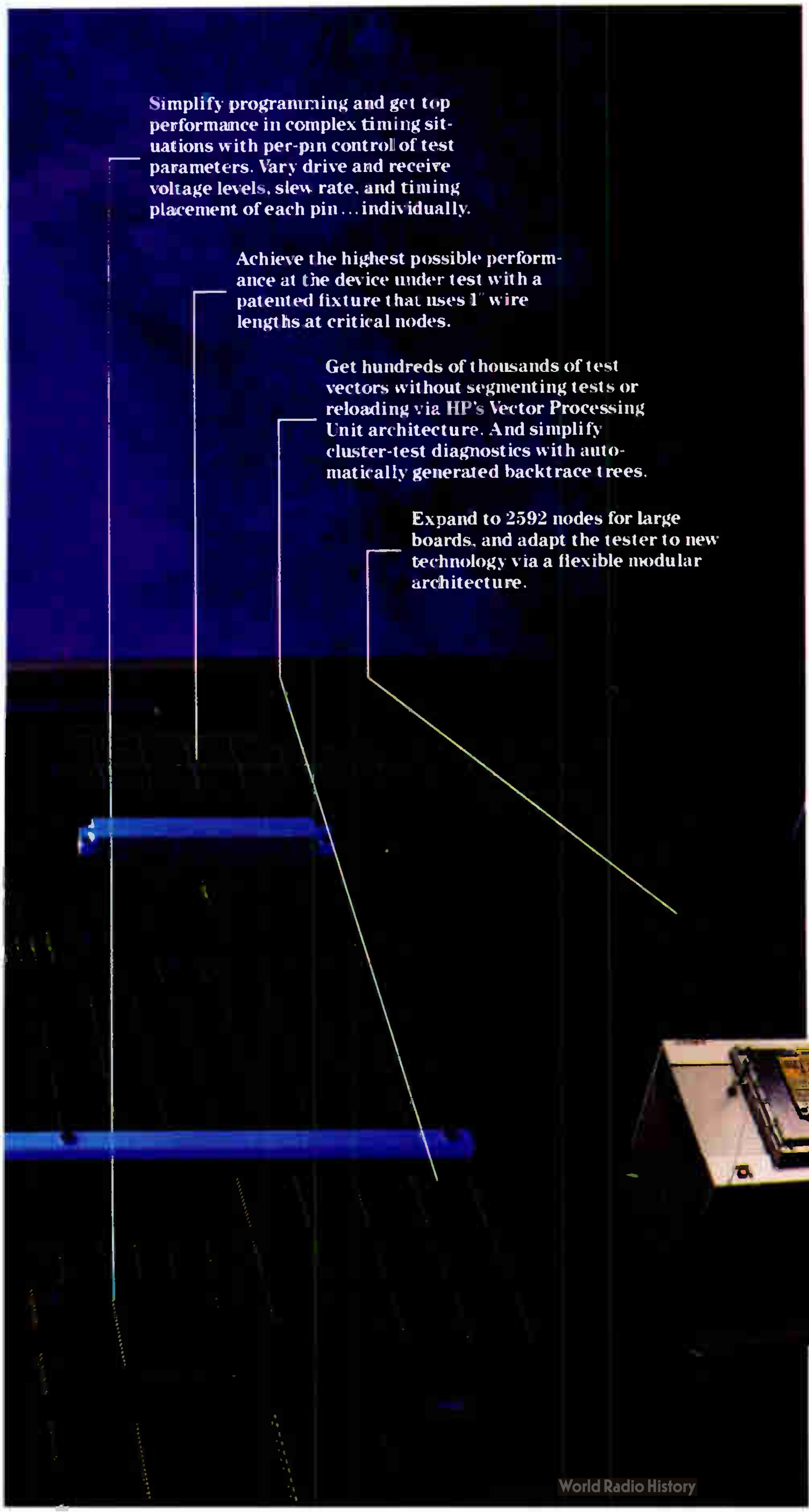
you do with
a board tester
that's new from
the pins down?

Digital, analog, in-circuit and functional



testing of complex boards...



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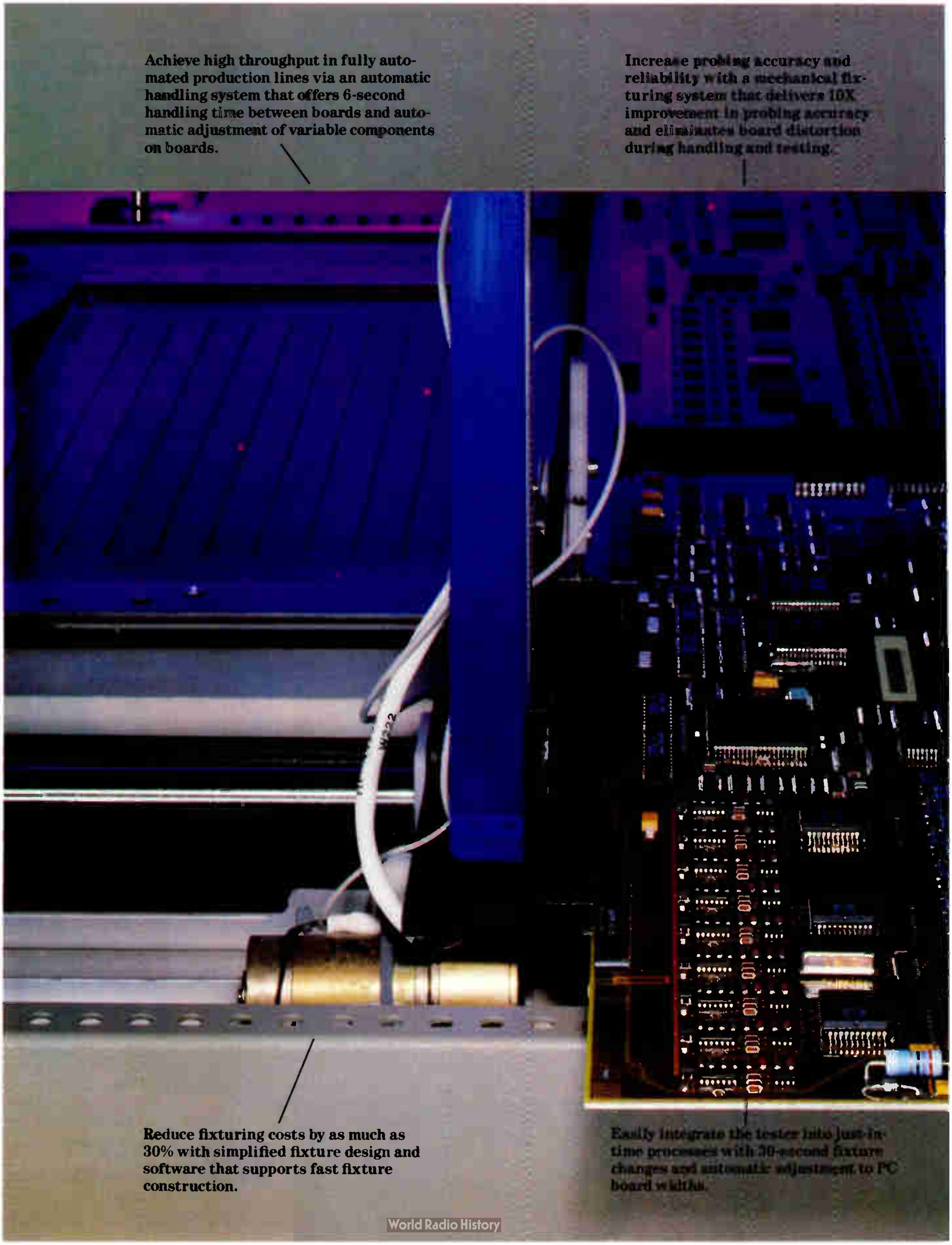
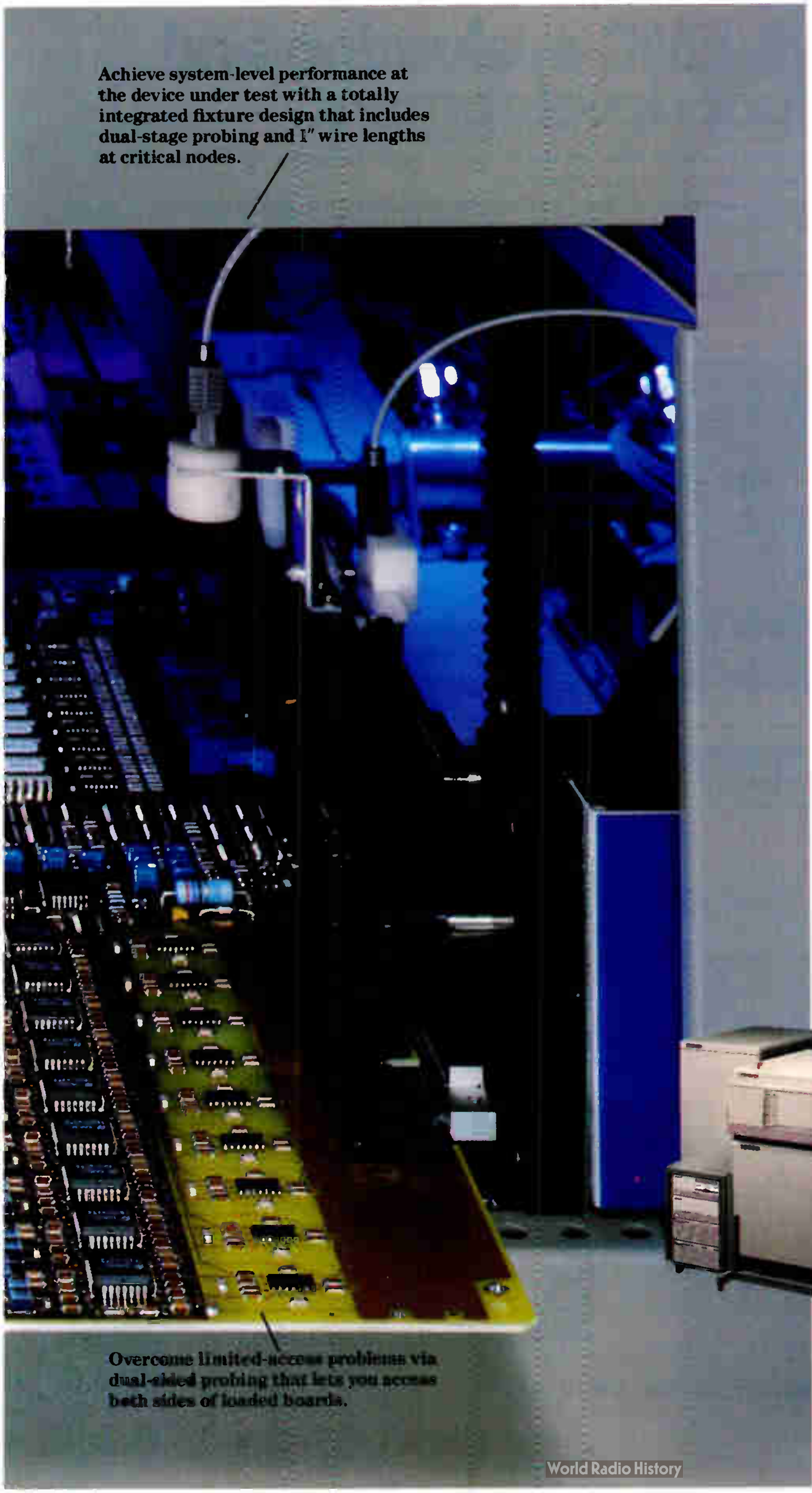
Circle 24

...and finally, solve the



SMT board testing problem.



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First, an innovative mechanical fixturing system handles high-accuracy, dual-level, dual-sided probing. Without flexing boards, which can mask open solder joints or create new process faults. You can even integrate it easily into automated SMT lines.

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So if board testing has been a roadblock to SMT integration, investigate the HP 3070 SMT-Series. It's sure to give you a new perspective. Call **1-800-752-0900** today. Ask for **Ext. 501E** to get our detail packed information package on SMT board testing.

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ELECTROSTATIC DISCHARGE SIMULATOR

MODEL ESS-630A

Features

The TC-815 discharge gun (optional) enables the system to conduct ESD simulation corresponding to IEC standard publication 801-2 (first edition).

Equipment summary

ITEM	Model ESS-630A With TC-815
Output voltage	0.2 – 30kV (0.2 – 10kV, 0.5 – 30kV, Range selectable)
Polarity	Positive and negative
Energy storage capacitor	150pF±10%
Discharge resister	150Ω ±5%
Charging resister	100MΩ ±10%
Rise time of the discharge current	5ns ±30% at 4kV
Operating mode	SINGLE, COUNT, REPEAT and 20/S (20 discharges per second, activated for approx. 5 sec with each depression of the trigger switch)

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Features

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4. An electric near field probe and a magnetic near field probe of high sensitivity are furnished as standard accessories.

Equipment summary

	FVC-1000	FVC-30
Frequency range	30MHz~ 88MHz 88MHz~ 216MHz 216MHz~ 470MHz 470MHz~1000MHz *Simultaneous 4 spectra measurement	100KHz~500KHz 500KHz~ 3MHz 3MHz~ 10MHz 10MHz~ 30MHz *Simultaneous 4 spectra measurement
Display	20-point LED bar graph display for each frequency band.	20-point LED bar graph display for each frequency band.

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PRODUCTS TO WATCH

WHILE SILICON COMPILER SYSTEMS ATTACKS THE TURNKEY DESIGN MARKET . . .

Breaking out of its high-end niche of tools for custom integrated-circuit design, Silicon Compiler Systems Corp. is introducing a modular product family that integrates its leading-edge software with existing circuit-design environments. The San Jose, Calif., company's new Explorer Series comes in three versions: SCS Foundation lets highly specific design tools developed in-house by customers work with Silicon Compilers' software suite; Explorer Tools are 15 modular programs for design entry, synthesis, simulation and analysis, and physical design and test; and Explorer Design Systems are six preconfigured IC design schemes optimized for custom and application-specific chips. The systems address the needs of a broad range of designers, from logic designers using ASICs to layout engineers in standard-part design groups. Explorer Series products are available now and run on Unix-based hardware from Apollo Computer, Digital Equipment, and Sun Microsystems. □

. . . SIERRA SEMICONDUCTOR MELDS DIGITAL AND ANALOG DESIGN TOOLS

Sierra Semiconductor Corp. has overcome the speed problems that plagued previous attempts to combine digital and analog design tools. While other design packages use separate analog and digital simulators, the San Jose, Calif., company has integrated its proprietary mixed-signal simulator algorithms into Silicon Compiler Systems Corp.'s schematic-capture software and Lsim logic simulator. The resulting software—called Montage—takes 11 seconds to simulate designs that a Spice simulator does in 6 hours. It includes simulation models from Sierra's 300-cell library, including 25 analog circuits, more than 245 digital parts, and nine electrically erasable read-only memories. Priced at $29,500, Montage now runs on Sun Microsystems Inc. work stations and will run on Apollo Computer Inc. machines later this year, the company says. □

CREE ADDS LOW-COST BLUE TO THE LIGHT-EMITTING DIODE SPECTRUM

A tiny Durham, N. C., company has developed a silicon-carbide blue-light-emitting diode that will sell for a small fraction of the $45 to $80 charged by giants like West Germany's Siemens AG and Japan's Sanyo Electric Co. for similar LEDs. Cree Research Inc. is pricing volume quantities at $2 apiece packaged and $1 unpackaged. Samples are priced at $40. Used with readily available red and green LEDs, the low-cost blues mean LED displays can now compete with incandescent lights in giant-screen displays for stadiums and other applications. The new diodes can also be used in digital color printers and medical equipment, where there is a need for near-ultraviolet light sources. Cree plans to offer a variety of diodes, ranging from single-color LEDs to chips that will emit multiple wavelengths and colors. □

SIGNETICS CHIP SET SHRINKS CELLULAR-PHONE CHIP COUNT BY 60%

The next generation of pocket-size, battery-powered cellular-radio handsets gets a boost from a six-chip set from Signetics Corp. Four CMOS and two bipolar circuits cut chip count in cellular phones by up to 60%, says the Sunnyvale, Calif., company. Other mobile-radio applications will benefit as well. The CMOS chips include the UMA1000, which handles filtering associated with cellular-control data, supervision, and signaling; the 80C552 microcontroller; the NE5751 audio-band filter; and the TDD1742 frequency synthesizer. The two bipolar parts are the NE5750, which integrates compaction/expansion, noise canceling, power amplification, and control functions, and the NE605 FM IF mixer/oscillator, amplifier, and demodulator. Available in September, the chip set will cost less than $60 in high-volume purchases. □

PRODUCTS TO WATCH

SPRAGUE'S HALL-EFFECT SENSOR IC CUTS AUTO-WIRING COUNT

A first-of-a-kind Hall-effect magnetic-sensing circuit from Sprague Electric Co. replaces reed or mechanical switches to dramatically trim the number of wires in auto-wiring harnesses. In a car with 30 modules in the driver's door, for example, the the UGN3055U cuts the number of wires to the on-board computer from 60 to a mere two. Developed at Sprague's Semiconductor Group in Worcester, Mass., the digital sensor monitors a variety of functions in a car, from an engine's fluid levels to door locks and ajar indicators. The chip operates under the CSC sequential-addressing protocol developed by Chrysler Corp. Its output drives high-density CMOS address decoding and control logic. The UGN3055U, which can also be used in a wide variety of security systems, sells for $1.60 each in quantities of 1,000. It is available 12 weeks after ordering. □

TI'S WIDEBUS SERIES DELIVERS MORE BUS WIDTH IN LESS SPACE

Glue logic doesn't have to be a limiting factor in designing board-level systems anymore. Texas Instruments Inc.'s Widebus series of its advanced CMOS logic family delivers the wider word lengths demanded by 32- and 64-bit microprocessors as well as the small package size possible with finer pitch leads, says the Dallas company. In all, 41 functions such as bus drivers, transceivers, latches, buffers, and D-type flip-flops will be available in 16-, 18-, and 20-bit word sizes compatible with 32- and 64-bit microprocessors. Space saving are also in the offing because the 25-mil pitch on the new, wider bus trims the package to about the same size as those for 8-bit devices. The chips will be fabricated in both CMOS and TTL. The first device, a 16-bit transceiver, will cost about $3 when it becomes available in the third quarter; that compares with a $1 price tag for an 8-bit transceiver. □

TEKTRONIX'S HIGH-VOLUME IC TESTER TARGETS FAST, LOW-PIN DEVICES...

Those fast glue-logic families from the major semiconductor houses fabricated in CMOS, TTL, and ECL have met their match in an integrated-circuit tester from Tektronix Inc. that costs about the same as older, slower production testers. The LT-1201 can be configured for either 32- or 64-pin devices and boasts 100-MHz test speeds, 16 timing sets, and operating voltages of –2.5 to +7.5 V. Systems have two test heads, each capable of parallel testing, which allows interfacing with dual or quad handlers for high throughput. Since the LT-1201's test head is small and lightweight—it measures 16 by 17 by 12 in. and weighs 45 lbs—it can be moved without mechanical manipulators. The Beaverton, Ore., company has priced the LT-1201 at $290,000 for an entry-level 32-pin system and $370,000 for an entry-level 64-pin system. □

...AND ITS 88000-BASED RISC WORK STATIONS HIT 17 MIPS

Tektronix Inc. takes aim at the reduced-instruction-set computer market with a family of four Motorola 88000-based processors rated at 14 million to 17 million instructions/s, 16 million single-precision Whetstones, and 7 million to 12 million floating-point operations/s. Keeping compatibility in mind, the Beaverton, Ore., company designed the XD88 family so that previous products can be upgraded by swapping processors. The XD88/30 3-d graphics work station is priced from $34,950 and the XD88/20 2-d work station, from $29,950. Graphics support comes from an independent 68020-based processor. The XD88/01 applications processor—a host compute server for networked Tektronix terminals and netstations—is priced at $24,950. When equipped with 1.8 gigabytes of disk storage and 2 gigabytes of streamer tape, this machine becomes the XD88/05 file server, which is priced at $75,000. □

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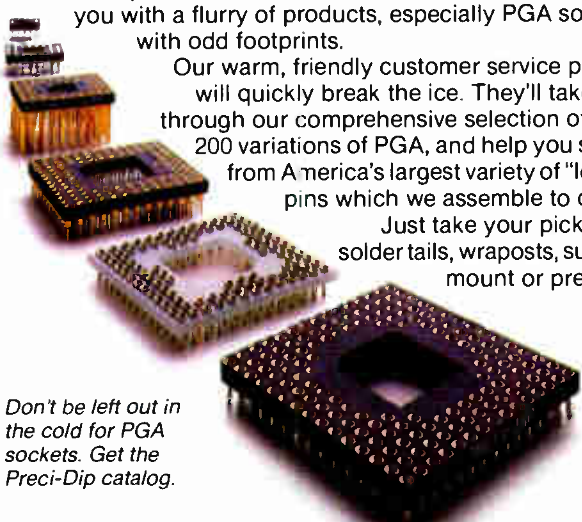

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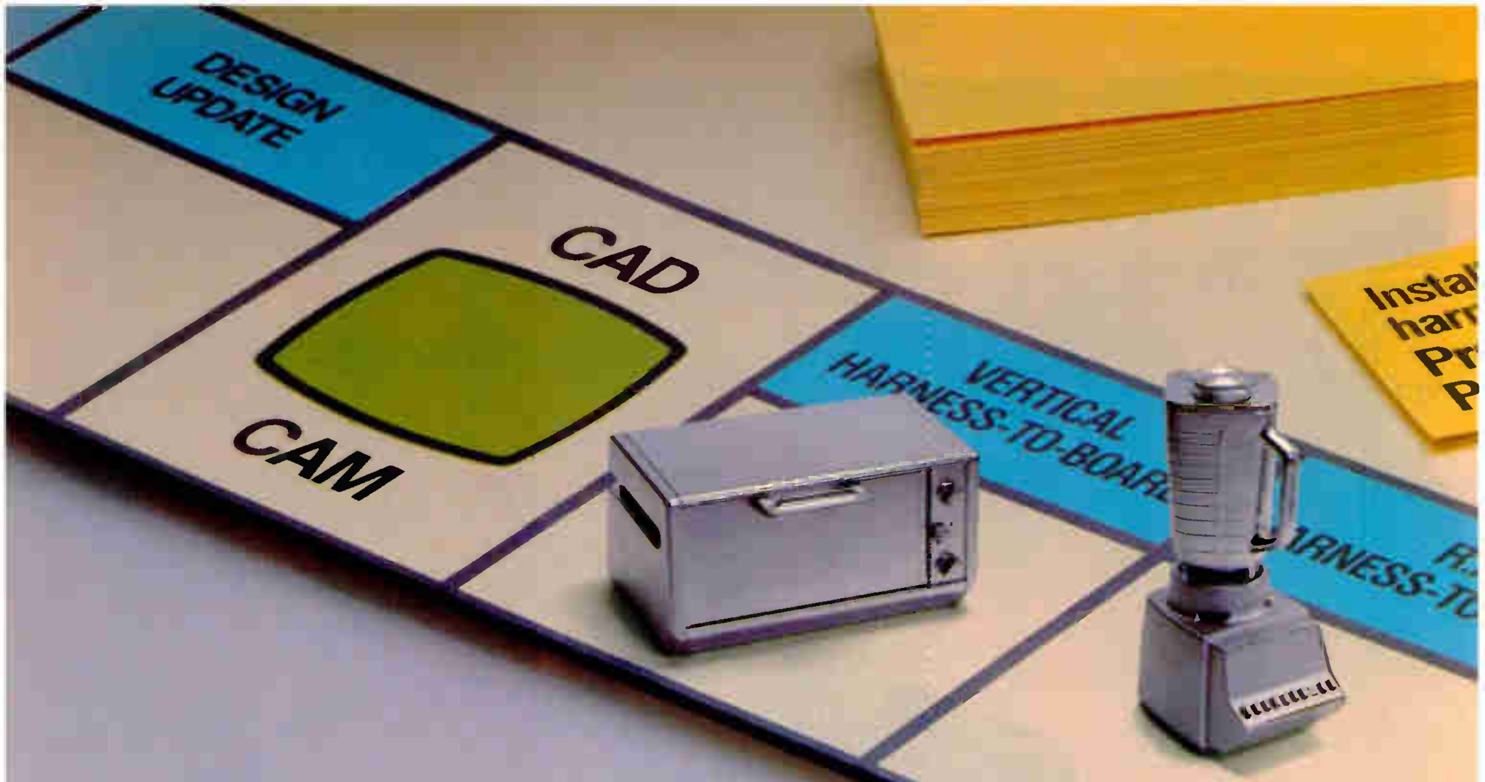

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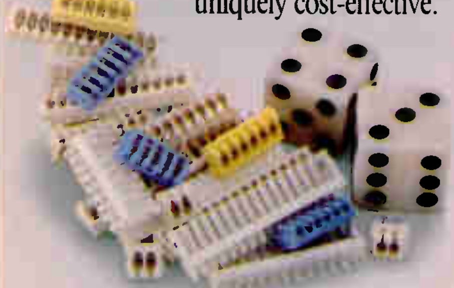

Or boom-box with. Or TV-game with. Because our unique CT (Common Termination) 2mm centerline connector system is uniquely cost-effective.

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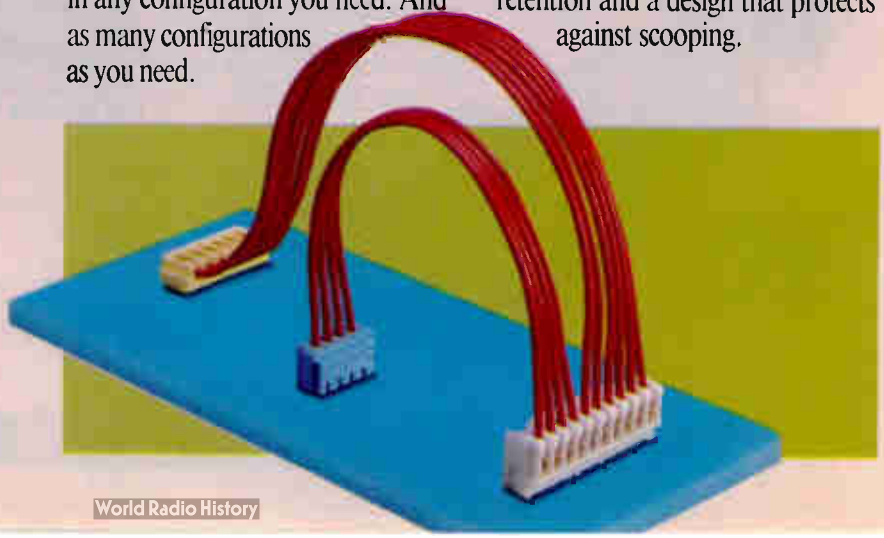
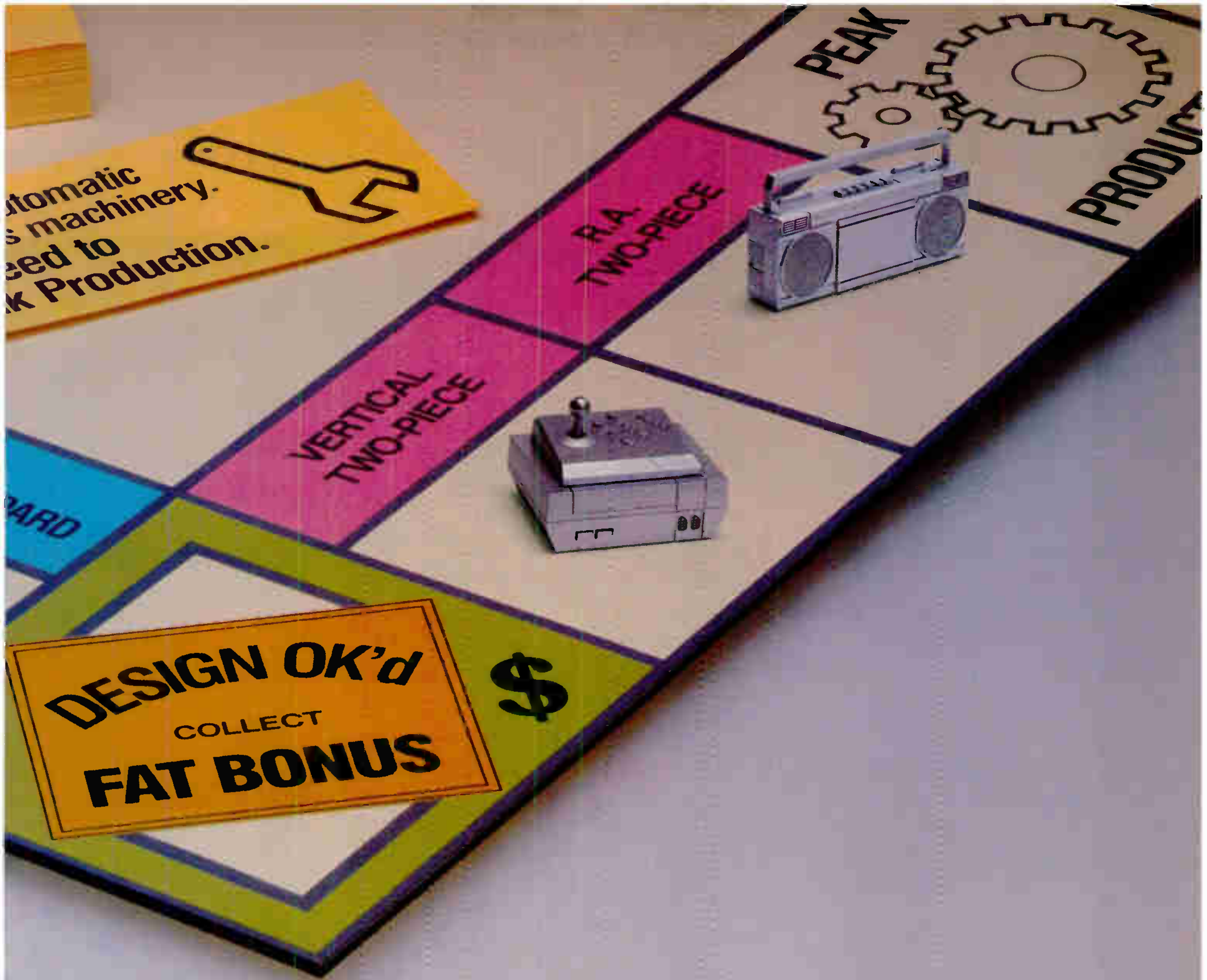
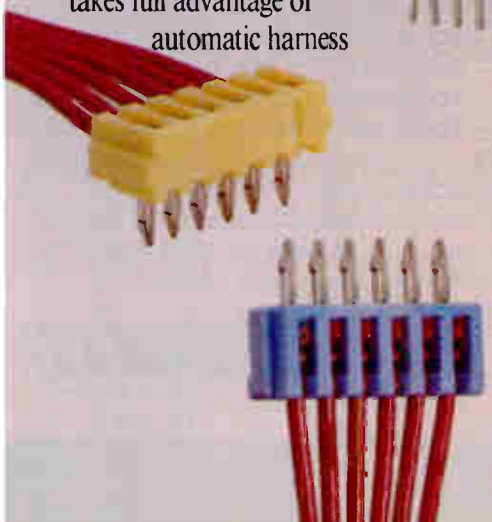




And where you'd normally solder wire by wire for direct-to-the-board connection, now you can mass terminate. Our special one-piece header takes full advantage of automatic harness machinery and lets you plug from 2 to 15 wires directly into the board for soldering. Also with self-retaining tails. Also a real time-saver.

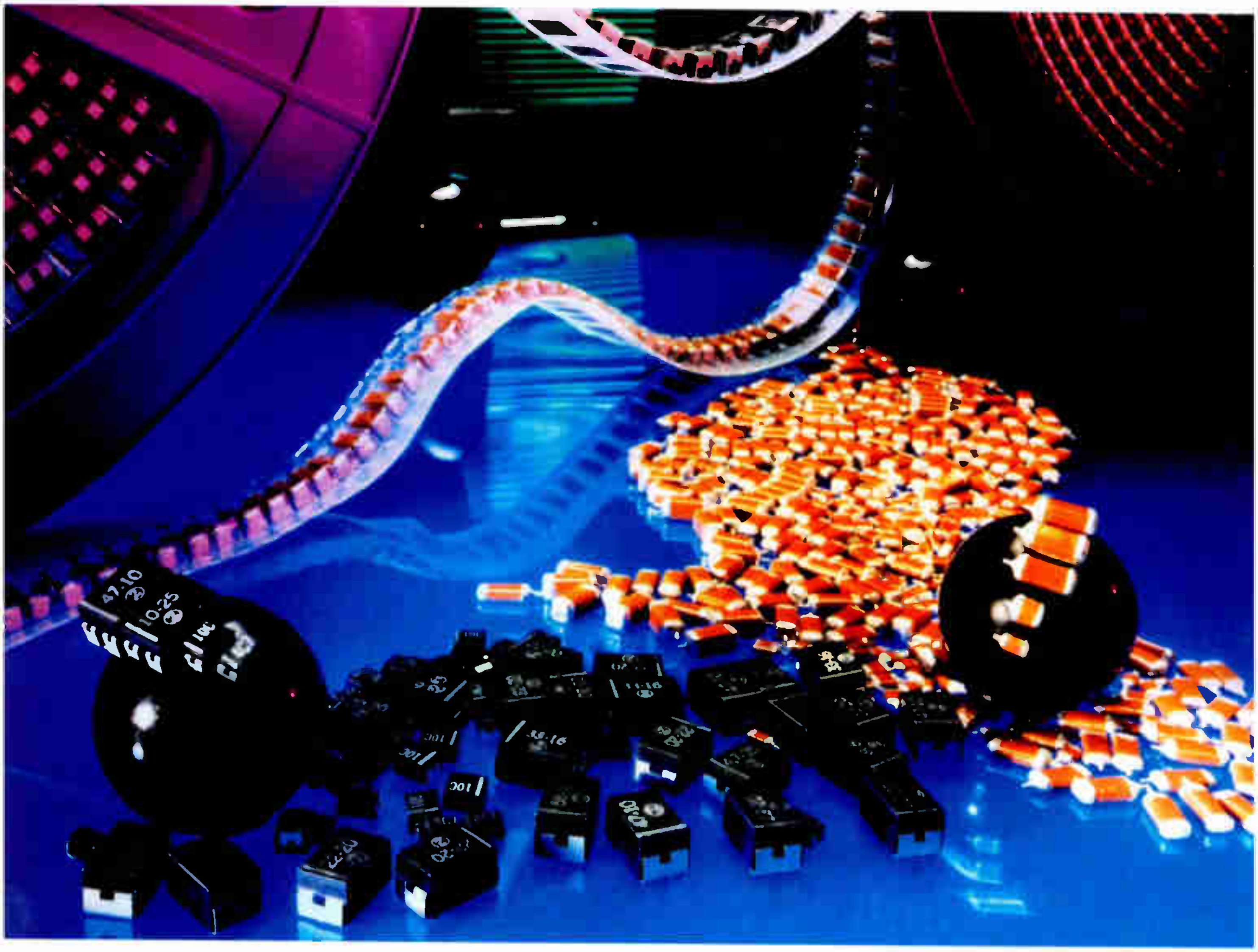


For technical literature and information on the AMP CT 2mm-centerline connector system, call 1-800-522-6752.
AMP Incorporated, Harrisburg, PA 17105-3608.

AMP Interconnecting ideas

Circle 17

SMT STANDARDS.



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Electronics

MOTOROLA TAKES THE WRAPS OFF COMMODITY-MEMORY THRUST

Word is out—the semiconductor giant is producing DRAMs and SRAMs in volume

AUSTIN, TEXAS

In an industry where secrets can seldom be kept for long, Motorola Inc.'s success in keeping its commodity memories program under wraps is exceptional. Despite the attention generated by an all-out, three-year effort that reportedly has cost some $300 million, executives in the company's Semiconductor Sector and MOS Memory Products Division have been able to keep details from leaking. Until now, Motorola has shared information about the project, one of the most ambitious currently being attempted by a major U. S. chip maker, only with major customers.

This period of self-enforced silence is coming to an end, however. Motorola's effort, with the aid of a pact with Toshiba Corp., to build its presence in the memory market has now passed a critical point. In recent months, the company has taken some giant strides in establishing a solid base in the memory market—and now it's talking about them.

The memory shortage of the past several years has helped Motorla's efforts, of course, since it provides a seller's market for dynamic random-access memories. But the proof is in the pudding, and now Motorola has shown that it can turn out state-of-the-art 1-Mbit DRAMs in growing volume at its plants in Austin, Mesa, Ariz., and East Kilbride, Scotland. The DRAMs are based on designs from Toshiba, the world leader in memory production; the two companies make a million 1-Mbit DRAMs per month at their joint facility in Sendai, Japan.

When it comes to fast static RAMs, which computer makers continue to gobble up as quickly as they are produced, Motorola's own design technology is key. Its latest SRAM offering, a 256-Kbit 20-ns chip, is now at the sample stage.

Motorola has come a long way since late 1985, when plummeting prices caused by DRAM dumping in the middle of a chip recession forced it to quit the DRAM market entirely. The Schaumburg, Ill.-based semiconductor giant doesn't break down its sales figures by product line, but Adam F. Cuhney, a financial analyst at Kidder, Peabody & Co. Inc. in San Francisco, estimates that memories accounted for about $300 million in sales at Motorola last year. Of that total, he says, $270 million came from DRAM sales and the rest from SRAMs. The 1988 DRAM sales were entirely from dies on wafers supplied by Toshiba, but assembled, tested, and packaged by Motorola. The analyst expects Motorola to post big gains this year in both categories.

Motorola's stated goals for the memory market are ambitious. By 1994 it is aiming for close to a 10% share of the worldwide DRAM market, which is expected to reach $12 billion that year. It also hopes to gain 10% of the projected $3 billion to $4 billion SRAM market in 1994.

"Motorola has made the decision to be a big player in the memory market," says Charles M. Clough, president of Wyle Laboratories Inc., an Irvine, Calif., distributor that handles Motorola's memory chips. But the company is "not yet the strong player [it] wants to be," he says.

Motorola's initial reluctance to divulge information about its memory program no doubt stems from the beating it took in 1985. For a company that prides itself on offering a broad product line powered by its own technology, the defeat was particularly galling. "We've kept it all low-key," acknowledges Jim George, corporate vice president and general manager of the MOS Memory Division. "We've had new technologies coming out of the oven on a crash basis every year to 18 months." George points out that one reason Motorola stayed quiet for so long is that the company views its efforts through a long-range lens. "When we came back [into the memory market], we pushed a 10-year button," he says.

MOTOROLA'S MEMORY ROADMAP

Technology (in microns)	Products SRAM	Products DRAM	Development start	Introduction date	Peak output
1.8	64 Kbit	256 Kbit	1977	1982-83	1988
1.2	256 Kbit	1 Mbit	1980	1985-86	1991
0.8	1 Mbit	4 Mbit	1983	1988-89	1994
0.5	4 Mbit	16 Mbit	1986	1991-92	1997
0.35	16 Mbit	64 Mbit	1989	1994-95	2000
0.25	64 Mbit	256 Mbit	1992	1997-98	2003
0.15	256 Mbit	1 Gbit	1995	2000-01	2006

SOURCE: MOTOROLA INC.

To date, Motorola is the only U. S. chip maker to pull off a successful reentry into the memory business [*Electronics*, April 1989, p. 28]. It had to overcome some formidable obstacles to do so. One such barrier is the very long lead time required to design and manufacture memories. When Motorola pulled out of the market in late 1985, for example, memory makers were just readying 1-Mbit DRAMs for introduction—those chips had been in development since 1980. Development of the 4-Mbit chips now appearing in small quantities was well under way in 1985, and work was just beginning on the 16-Mbit DRAMs that will debut in 1991–92. Lead times for SRAM development are similarly lengthy. "It's a technology treadmill," says Bud Broeker, director of operations at the division. "When we jumped back in, we had to run even faster than the treadmill moves, and we're still doing it."

But Motorola had no choice but to get back into the memory business to protect its leadership position in microprocessors, says Cuhney of Kidder Peabody. He says many processor buyers, especially the smaller ones dealing with distributors, demand a package deal—with memory included. "If Motorola wanted to stay a microprocessor company, it had to have memory," Cuhney says. (Intel Corp. linked up with South Korea's Samsung several years ago on the same grounds.)

There was another powerful kicker, too: along with most of the industry, Motorola executives regard DRAM design and process technology as the driver for all other chip work. The holdup back in 1986 was a DRAM technology gap, notably in mass-manufacturing techniques developed by Japanese firms. "Motorola couldn't jump back in without technology help," says Broeker.

The alliance with Toshiba neatly bridges the gap. The cooperative effort has proved to be all that could have been expected by both sides, according to George and Broeker. "Toshiba has been a good partner, with super technology and a very positive attitude," says George. As Motorola's own worldwide production of DRAMs expands from the present rate of about 12 million units a year, it will become less dependent on Toshiba for wafers, but it intends to keep taking small quantities. "We'll continue buying them as benchmarks," says George.

To make best use of Toshiba's designs and processes, which support DRAMs and slower (upwards of 55 ns) SRAMs, Motorola has spared no horses to keep pace internally. "We couldn't be in memory in any bigger way," says George.

SRAM SAVVY. The SRAM product line is largely Motorola's own show; the underlying technology comes mainly from its own laboratories. Several years ago, Motorola researchers came up with a synchronous architecture that, according to Motorola, allows for higher speeds by eliminating interconnection delays. Using this design as its base, Motorola has steadily beefed up its CMOS product portfolio of 1.5- and 1.2-μm devices, and now has a core family of 25-ns SRAMs that are in solid demand.

Its top-of-the-line CMOS SRAM, a 1-Mbit, 0.8-μm chip that runs at 25 ns, is due out the third quarter of next year, as is its first biCMOS SRAM, a 64-Kbit, 1.0-μm device that runs at 10 ns.

Motorola is clearly positioning itself for a leading role in the memory market, but intentions don't always become reality, as analyst Cuhney points out. Producing top-quality SRAMs on tight schedules has proved troublesome in the past for Motorola, he notes, and problems could resurface as the higher complexities make chips even tougher to build. Cuhney adds that some competitors—like Integrated Device Technology Inc. of Santa Clara, Calif.—have a head start that might be difficult to overcome.

And as one marketing official at a rival memory maker notes, manufacturing commodity memories efficiently with good margins is not getting any easier. "If anything trips Motorola up, that will be it," he says.

Motorola executives, particularly those at the MOS Memory Division, credit their comeback in the memory business to the 1986 Semiconductor Trade Accord between the U. S. and Japan. "It leveled the playing field," says Broeker. Some U. S. memory users claim otherwise, saying the pact created conditions for a memory shortage and extreme price hikes that led to windfall profits by Japanese firms.

But Broeker says the accord's provisions for barring Japanese producers from dumping memory chips into the U. S. at ruinous prices gave Motorola a chance to regroup after the 1985 disaster.

In that year, prices fell to as low as $0.25 for a 64-Kbit chip and $1.30 for a 256-Kbit chip—levels that did not cover direct costs, much less pay for investments. The rules set forth in the accord also provide a consistent economic framework that allows Motorola to plan its memory operations over a period of years, Broeker says. The company hopes the pact is extended beyond its current five-year term. *–Larry Waller*

MERGERS

HOW WILL HP-APOLLO SIFT OVERLAPPING PRODUCT LINES?

CHELMSFORD, MASS.

The general euphoria on both sides following the surprise merger between Hewlett-Packard Co. and Apollo Computer Inc. last month masks some concerns among industry watchers about the future of the ground-breaking Apollo line of work stations—and, indeed, about the future of the work-station market itself.

On the face of it, it's undeniable that the acquisition of Apollo, which had revenues of $653 million last year, by the $9.83 billion HP is blockbuster. It vaults the joint company over Sun Microsystems Inc. and Digital Equipment Corp. into the lead in work-station market share, significantly altering the lineup of key players there. HP and Apollo together had 30.4% of that market at the end of last year, according to estimates by Dataquest Inc., the San Jose, Calif., market-research organization. That puts them just ahead of Sun, with a 28.3% share.

> The companies have competing lines in RISC and 68000 machines

But it might be an early indication that this market is starting to slow down, in the view of at least one analyst. "This sort of consolidation is to be expected," says Mark Stahlman, a work-station market watcher at Sanford C. Bernstein & Co. in New York. "I wouldn't be surprised to see more of it."

A more immediate question is the direction that the new Apollo, now a division in HP's Workstation Group, will take. Both companies design and build Motorola 68000-based work stations, and both have reduced-instruction-set systems as well. Apollo, in fact, has been attempting a corporate revitalization with its Series 10000 RISC-based desktop supercomputer [*Electronics*, March 3, 1988, p. 69]. The high-end machine has made a major contribution to bolstering the Chelmsford company's dwindling profits and slowing revenues since it began shipping last fall [*Electronics*, September 1988, p. 158].

"I can't see [HP and Apollo] keeping two competing lines of 68000-based and RISC-based work stations," says David Card, an analyst who tracks work stations for International Data Corp., the Framingham, Mass., market-research firm. "I imagine Apollo's [68000] line will eventually die out."

For his part, Michael Gallup, Apollo's vice president for product marketing and programs, hints that this might be so. Gallup says he can envision one of Apollo's two 68000-oriented engineering groups being designated to continue that development effort, with the other being freed to undertake new tasks.

As for the overlap in RISC-based products, Gallup says, "We have to figure out soon where we go with these, but it's too soon to have that worked out yet."

Rumors had been circulating for months that Apollo was a takeover target, but most of them had the suitors as European or Japanese firms. Virtually no one would have named the Palo Alto, Calif.-based HP as a bidder: the giant manufacturer of integrated instrument and computer systems hasn't made a major acquisition since the 1960s, when it bought what is now a medical electronics division in Waltham, Mass.

But at a time when hostile takeovers have become routine, HP and Apollo quietly got together and pulled off a deal unanimously endorsed by both firms' boards, with HP offering $476.4 million for Apollo. The sale needs approval by the federal Securities and Exchange Commission and stock tendering by 51% of Apollo's shareholders. Assuming no problems crop up, the deal should be completed in June or July.

Since its founding in 1980, Apollo has become known for innovative technology and for its early recognition of the importance of distributed computing and networking. But the hard times it has encountered in recent years left the once preeminent company lagging behind Sun in work-station market share.

In the aftermath of the merger announcement, top executives at both HP and Apollo spoke glowingly of joining forces. "Both companies are recognized for technical innovation and high-quality computer products, and for a commitment to the industry's move toward cooperative computing environments based on open industry standards," says John A. Young, HP's president and chief executive officer. For his part, Apollo chairman and CEO Thomas A. Vanderslice says that HP's "commitment to the work-station business and to open industry standards, its product strengths, and its well-known concern for its people add up to a very good fit."

Perhaps Apollo's most important contribution to the deal is its strong installed base of more than 93,000 work stations used by "customers who are happy with their products and technology," says Richard Watts, director of marketing for HP's Computer Products Sector. Another asset is Apollo's strong presence in electronic design automation, including the software technology contributed by its leading customer, Mentor Graphics Corp. in Beaverton, Ore.

SIZE AND STABILITY. Watts also cites Apollo's Network Computing System approach to distributed work-group computing and its RISC architecture, first introduced in the Series 10000. HP had already become a licensee for the networking software, he says, "but now we get access to that technology ahead of everyone else." In return, Watts says, HP lends Apollo size, stability, and financial resources sufficient to relieve the anxieties of its customers. Some of them were worried about Apollo's financial condition as revenues sagged and profits shrunk or disappeared in recent quarters. "We think we can put customers at ease about that," Watts says.

Most industry analysts assess the acquisition as a good one for both sides, despite the problems stemming from product-line overlaps. As for morale at Apollo, Gallup at least sounds upbeat. He says that the odds "are about a million to one that we would have been acquired by someone as well suited to us as HP is."

But an elegiac note was sounded by Apollo cofounder David Nelson. "From a founder's point of view, the assimilation of Apollo's identity into HP is somewhat disappointing," says Nelson, who recently resigned as vice president and chief technical officer to start his own company, Envision Systems Inc. in the Boston area. "It's not the final chapter we all would have written." *–Lawrence Curran*

MANAGEMENT

THE CHANGING STYLE AT SEMATECH

WASHINGTON

In the weeks after the management shakeup that left Sematech's chief operating officer, Paul Castrucci, walking the streets of Austin, Texas, in search of a job, critics of the chip-manufacturing consortium came out in full force, pointing to the incident as proof that U. S. companies couldn't work together. But officials both inside and outside Sematech say that's not the case at all—that the sudden firing of Castrucci was neither a comment on Sematech's progress nor a surprise move.

Now Sematech is on the verge of a major management reorganization that will probably result in a much more active role for chief executive officer Robert Noyce, who joined the consortium last summer ostensibly to play Mr. Outside to Castrucci's Mr. Inside. In the coming months, Sematech insiders say, Noyce may well do away with Castrucci's position altogether, replacing the single operations officer with a corps of deputies focused on specific parts of the Sematech puzzle, all reporting directly to the CEO.

Under the original plan, Noyce was supposed to have been a cheerleader and politician, handling Sematech's interface with industry and government; Castrucci was to have run the facility day to day. But that's not the way it turned out. "There were too many cooks in the kitchen," Castrucci says. "[Noyce] was around more than we expected."

The reason? Says C. Scott Kulicke, a Sematech board member and the chairman of Kulicke & Soffa Industries Inc., a semiconductor-equipment concern: "Bob Noyce is too qualified to be just a cheerleader. He's involved right up to his nose." Kulicke acknowledges that the Sematech management structure may not have been the ideal choice. The fact is, he and others say, Sematech may just be too small to support both a chief executive and a chief operating officer.

Now, with Castrucci out and Turner Hasty, a 30-year chip research veteran from Texas Instruments Inc., acting in his role, Noyce is expected to play with the management structure. Hasty, who has been with Sematech since its inception in September 1987 and who has already put in one four-month stint as interim COO, says he would "have no problem moving back into the ranks again" if that's what Noyce asks.

> Is Sematech just too small to support both a CEO and a chief operating officer?

Meanwhile, Castrucci says he could tell "right from the start that the chemistry between Bob and me wasn't that good." Nonetheless, he says he was completely surprised when Noyce called him to a breakfast meeting March 20 and asked him to quit. He says his management team had met each of the goals it set in his first six months on the job, including getting the wafer fab up and running before the end of March.

"With time, I'm sure things would have worked themselves out," Castrucci says now. "Just look at the record. The fab got built. We ramped up the staff from 45 to over 500 people in six months. Wafers got processed. We got negotiations started with outside vendors [to develop advanced processing equipment]. It wasn't because things weren't getting done."

But getting things done was apparently harder than it needed to be. "What you're not looking at is the amount of effort it took to get all that work done," says Kulicke. "Differing management styles are a substantive problem."

Indeed, the problems boil down to differences in management and personal style. Noyce, a cofounder of chip giant Intel Corp., came from the free-thinking entrepreneurial environment of Silicon Valley; Castrucci arrived fresh from 32 years as a loyal IBM Corp. soldier. Noyce favored a participatory style of management, while Castrucci did things the IBM way: assign tasks, assist where possible, and wait for results to be reported back.

For some outside observers, Castrucci's departure has ominous implications. He is "a damned good manufacturing guy," says Charles Minnihan, a retired vice president from Perkin-Elmer Corp. now working as a consultant. "He's probably started more new products than anyone else in the world. This blows my mind. It really sets [Sematech] back."

Now the day-to-day management job falls to Hasty, who is currently working on signing up companies to develop the next-generation equipment, materials, processes, and test-chip demonstration vehicles for the 0.5- and 0.35-µm phases of Sematech's research program. That's the line width needed to produce a reasonably sized 64-Mbit dynamic random-access memory. The first of the contracts should be awarded by early May, with others coming over the rest of the spring and summer. *–Tobias Naegele*

ARE MULTIMEDIA PCs AROUND THE CORNER?

PRINCETON, N. J.

Multimedia personal computing—the integration of full-motion video, audio, and graphics into a PC—has finally gotten its act together. It will be playing on an IBM Personal System/2 by early 1990. But industry watchers still see formidable hurdles in seamlessly stitching together several technologies, including interactive video, high-performance graphics, high-fidelity audio, and compact-disk, read-only-memory storage.

Far from calming the waters, IBM Corp.'s recent bombshell endorsements of Intel Corp.'s Digital Video Interactive technology and of the CD-ROM XA audio standard are a starting gun for competitors claiming they can solve some small piece of the puzzle better. "The race is on," says Satish Gupta, manager of IBM's Mixed Media Products Division in White Plains, N. Y. "We're going to see people inventing better and better hardware."

Another hurdle is software. "The real barrier is getting applications created and having products that make people think they should put [multimedia] in their box," says Robert Gutenstein, an analyst with Kalb, Voorhis in New York.

The ferment began in earnest March 30 with IBM's endorsements, which Big Blue announced at the Microsoft CD-ROM Conference in Anaheim, Calif. For the upcoming video-bred generation of PC users, IBM will integrate into its PS/2 platform Intel's DVI technology for storing full-motion, full-color video on CD-ROM disks. DVI's key attraction is its ability to compress bit-hungry video data at a 125 : 1 ratio so that more than an hour of full-motion video can be stored on a standard CD-ROM disk [*Electronics*, February 1989, p. 57]. For the audiophile, IBM has endorsed the CD-ROM XA standard, sponsored by Microsoft Corp., for storing digital audio information on the same optical disks.

> IBM's support for DVI and a CD-ROM standard is setting off a ripple effect

IBM's support of DVI and CD-ROM XA means the company has finally taken the multimedia plunge, says Linda Helgerson, editor of *CD Data Report*, a Falls Church, Va., newsletter for the CD-ROM industry. James Cannavino, president of IBM's Entry Systems Division, left little doubt, she says, that the announcements were of "equal magnitude and comparable significance" to its introduction of the IBM Personal Computer.

There are also implications for DVI's main competitor, the proprietary Compact Disc-Interactive standard being pushed by Philips International NV of the Netherlands and Sony Corp. of Japan. By teaming up with Intel and Microsoft, IBM has given CD-I the cold shoulder. "This is the beginning of the mutual growth and sharing in the benefits and rewards of an open standard," Helgerson says, instead of "control through the insistence on a proprietary standard."

A more recent competitor—one just as interested in open architectures as IBM and Intel—is two-year-old Universal Video Communications Corp. of Irvine, Calif. It claims to have a solution to DVI's major shortcoming. While DVI can decompress stored images in real time, the compression algorithm for coding information onto the disk is so demanding that it requires a high-end parallel-processing computer.

"We can do real-time compression in the same box that's doing the playback," says vice president John Music. Although Universal Video has publicly positioned its VP-2000 video work station directly against DVI, a third-party developer familiar with both systems is not so sure. While DVI produces full-motion video at 30 frames/s, the VP-2000 "is designed to do 10-frame/s video," says David Dering, president of American Helix Corp., a Lancaster, Pa., software developer that used the VP-2000 in a demonstration at the CD-ROM Conference. VP-2000 has potential, he says, and American Helix wants to develop software tools for it. But "people like to see 15, 20, or 30 frames/s." Universal's Music claims that when adjustments for flicker are made, viewers cannot discern the difference between 10 and 30 frames/s.

Meanwhile, Intel is filling in its software gap—and the acknowledged void in applications. "We're working with two companies to develop high-level authoring tools," says Bob Brannon, general manager of Intel's DVI operations in Princeton. The authoring package is set for release at the end of the third quarter and will run on Intel's 80386-based Pro750 applications-development platform. The Pro750 will ship in July, Brannon says. *–Jack Shandle*

TRANSACTION PROCESSING

WALL STREET LOOKING TO ROCK AROUND THE CLOCK

OLTP vendors scramble to give traders 24-hour service

NEW YORK, N. Y.

Life in the financial fast lane is getting faster. Global traders in markets from treasury bills to pork bellies have their eyes on 24-hour operation, and the securities and commodities exchanges that handle the transactions are girding for fierce competition to be first to deliver round-the-clock service.

Brokerage houses desperately "need a way to involve ourselves with the markets all around the world and pivot them around New York," says Joseph Macchia, vice president for communications at New York-based Liberty Brokerage Inc. The implications for the electronics industry have a distinctly green glow, especially for systems houses that sell on-line transaction processing mainframes and minicomputers. Stratus Computer Inc., a Marlboro, Mass.-based maker of OLTP systems, expects the exchange-automation market to grow at a 40% clip each year through the early 1990s, according to Mark Smith, director of financial services marketing.

Other technologies also stand to thrive in the push toward 24-hour global trading services. For starters, exchanges will need to upgrade their wide-area networking systems. Then too, the emerging trader's work-station market will become a battlefield for faster, smarter personal computers. There will even be a growing need for artificial intelligence applications, particularly in object-oriented programming.

Round-the-clock global trading will require more than just upgrading equipment. A major challenge is the conversion of securities clearing and settlement systems from overnight batch operations to on-line operations. "The move from 100% batch to an on-line environment is not just a matter of buying new equipment," says Smith. "The only way to handle on-line settlement is relational data bases, and they have just started to appear in on-line transaction processing in the past two years." Whether relational data bases can handle on-line the high volumes of data generated in securities trading remains to be seen, Smith says.

Until round-the-clock trading becomes a reality, the operation of global trading systems will be limited. One obstacle that stands in the way of current global trading is the difference in time zones. For now, the problem of timely settlements is being solved by adjusting trading hours. For example, the American Stock Exchange altered the trading hours for its Major Market Index when it franchised the index to the European Options Exchange in Amsterdam. One criterion for trading the Major Market Index is that it must have a uniform settlement, which means trading hours in New York and Amsterdam must coincide. Optimally, trading would take place from 10 a.m. to 4 p.m., Amsterdam time, which means 4 a.m. to 10 a.m., New York time.

But because settlements are processed in overnight batches in New York, the offices there are not ready to start trading until 6 a.m., so trading hours are noon to 6 p.m., Amsterdam time.

Simulating the action that takes place on the trading floor when the floor is not open is particularly important to some exchanges, such as the Chicago Board of Trade. The CBT trades 26 items, including treasury bonds and notes, agricultural futures, market indexes, and metals. It needs a system that provides an adequate electronic replication of the "open outcry" system employed in the trading pits.

Existing systems match buy and sell orders, but they don't simulate the action of an auction, in which each bidder can see—and hear—what the competition is bidding. "The auction system introduces a competitive element as opposed to just sitting around and waiting for a match," says Michael O'Connell, assistant manager for financial products at the CBT.

BUILD YOUR OWN. And instead of just sitting around and waiting for a suitable system to be developed, the CBT is putting together its own: Aurora, an electronic auction for after-hours trading. Tandem Computers Inc. of Cupertino, Calif., will supply the mainframes, and Apple Computer Inc., also of Cupertino, will supply AI work stations based on Macintosh II personal computers with Texas Instruments Inc.'s Micro Explorer AI hardware and software. A prototype of Aurora will be up and running in September, O'Connell says.

With Aurora, traders will have before them "a screen that replicates the pit, with icons for each bidder along with other information, such as the size of the contract and bid or asked price," O'Connell says. By using a mouse to move the cursor, a trader can select another trader to deal with. Even after a selection is made, the screen will continue to display the contracts and prices being offered by other traders who, if they were in the trading pit, might be within a point of being in the market.

Although Tandem's high-reliability, high-speed OLTP mainframes provide raw processing power, the key technology is TI's Micro Explorer. The system includes the Dallas-based company's Lisp (for List-oriented programming) programming language, says John Mandell, AI product marketing manager at TI.

The rapid system prototyping made available by Lisp is what made the work station attractive to the CBT. Economists employed by the board developed a concept of how the electronic system could mimic trading in the pits. "Once that was done," says Mandell, "we could prototype it very rapidly. The idea is that you get a program shell running very fast to tell you what the end system is going to look like." The prototype allows for a quick

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Circle 37

evaluation of the concept, Mandell says. "We are now in the process of filling in all the functionality," he adds.

Key to Lisp's rapid prototyping capacity is the ability to incrementally compile lines of new code without having to compile the entire program. Also, a library of about 15,000 object-oriented subroutines can be plugged in with a high probability that they will not have to be altered.

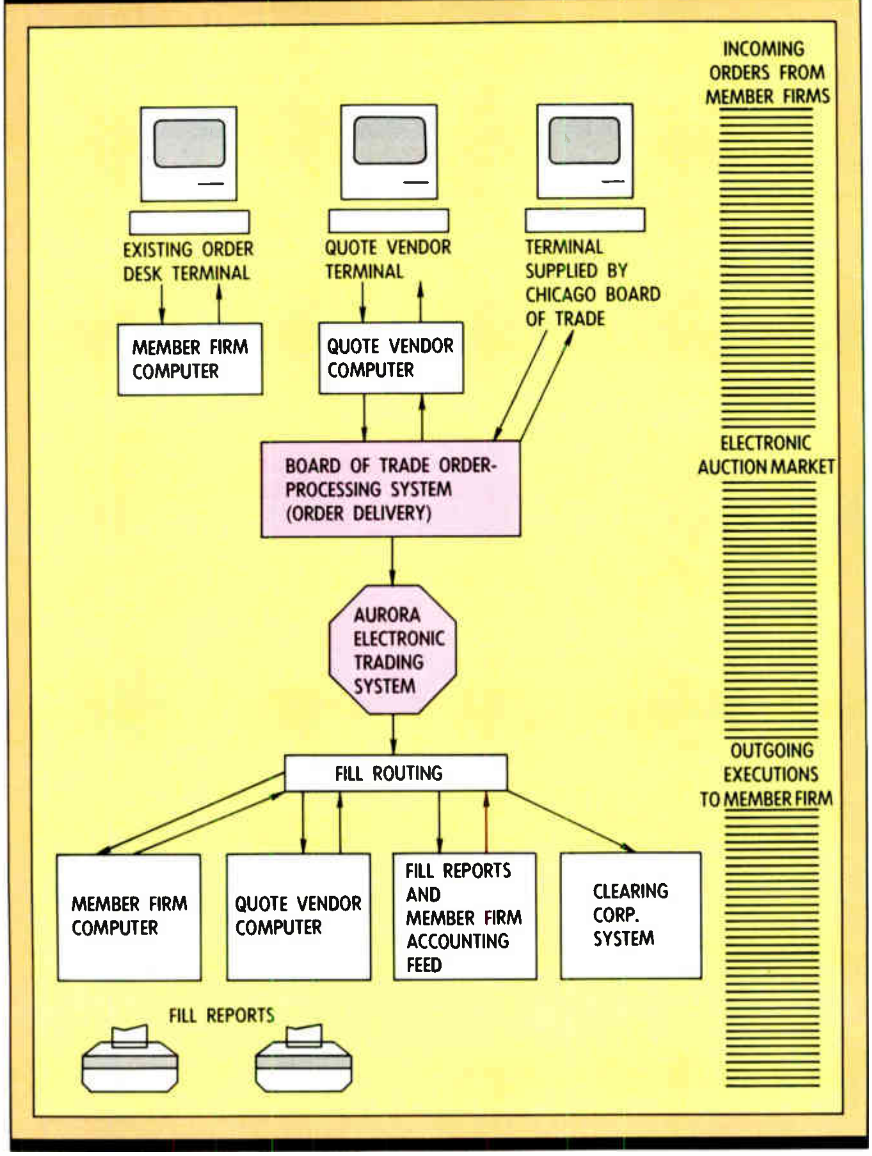
NATURAL LANGUAGE. Finally, the ability of Lisp to handle natural-language inputs is critical. "You can develop similar functionality in conventional programming languages," says Mandell, "but it's more like writing the program in stone. If you want to change something, you have to chip away at a corner and run the risk of breaking the stone."

In a another manifestation of the need for highly flexible, quick-change technology, the CBT is using Tandem's top-of-the-line VLX mainframe, which can be scaled up by adding processors as needed without reprogramming. A VLX with four processors can execute 7.5 transactions/s, says Ray Villareal, Tandem's assistant to the senior vice president for sales and marketing. Other vendors, notably Concurrent Computer, Digital Equipment, IBM, and Stratus, are also vying for the exchange-automation market for 24-hour global trading.

Among the qualities Villareal sees as crucial for this market are processor modularity, the ability to place mainframes in remote sites without on-site service, and the ability to switch computing resources from region to region as financial activity changes in time zones.

A second tier of requirements, says Villareal, includes maintaining data integrity, a feature that involves not just redundancy but also assuring that bad data, when it crops up, is not passed around the network. *–Jack Shandle*

TRADERS OF THE ELECTRONIC PIT



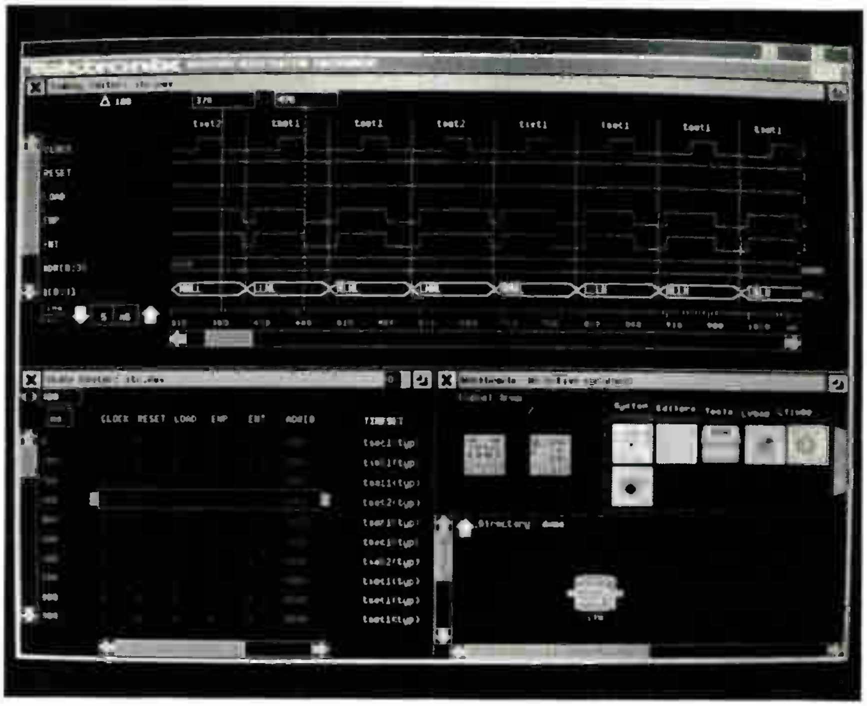
HERE'S SOFTWARE TO SPEED VECTOR CREATION

BEAVERTON, ORE.

Circuit-design systems and testers have been integrated only very loosely up to now. And though the start of a trend toward linking them more closely is discernible, the solutions so far have not addressed the real problem of designing for test while designing the chip. The latest attempt to address this problem is a new software package from Tektronix Inc.

Some systems can now convert simulation vectors into test vectors. But the Tekwaves package from the Beaverton company takes the next logical step forward. While it doesn't go all the way—it can't incorporate testing into the chip-design process—Tekwaves does provide an efficient means of automatically creating test vectors for a device that has been designed. It's easier to use than most systems thanks to a graphical user interface akin to the one on the Apple Computer Inc. Macintosh, says Chris Pieper, verification automation manager at Tektronix.

The task facing a design engineer is to create enough test vectors to find any glitches in his prototype. For a test engineer creating a test program for an integrated circuit, the job is to increase fault



The Tekwaves software from Tektronix uses waveform subroutines to create additional test vectors; it boasts a Macintosh-like graphical user interface.

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coverage from the 65% typically achieved with design vectors from a simulator up to the 95% required to assure adequate testing. Historically, both designer and test engineer have had to resort to typing in test vectors manually, a long, tedious, and error-prone process. Most stimulus creation today is still done in this manner.

Tekwaves provides a more effective way of creating these extra vectors with waveform subroutines. To produce a subroutine, the designer, using a TTL data book or application-specific IC, describes a waveform for each pin of a device being tested. An IC typically has signals such as chip select, clock, read/write line, and address latch enable. Each signal must occur at a certain point in time. With Tekwaves, the designer creates waveform subroutines for each signal; the software will then replicate the waveform just as a signal generator would.

Once the user has written subroutines for every pin of the device, he has a time set, or frame, of signals. Each of these frames—or individual signals within a frame—can be "cut and pasted" into the frame for another device.

Also, Tekwaves brings some new capability to the task of turning simulation vectors into test vectors. Like other tools available, Tekwaves acquires vectors from simulators from GenRad Inc., Mentor Graphics Corp., and other vendors and converts them into waveforms. "Tekwaves knows the characteristic of the final tester, minimum pulse width, maximum cycle length, edge-placement accuracy, and so on," says Bob Turner, senior software engineer at Tektronix.

The program identifies by time and signal name all the points in the data where a tester violation has occurred, and presents them in text form in a window. As

The Tektronix package is an attempt to link test and circuit design

the designer looks at the waveforms on the screen, he can see where the errors have occurred. To eliminate the error, which might be a waveform edge in the wrong place, for example, the designer simply points to the edge with a mouse controller and moves it. The waveform data base is automatically revised to incorporate the change.

Once the vector errors are fixed, the software automatically creates a test program. For test systems that Tekwaves does not support, the designer simply wires together several icons on the screen and the software does the rest.

Tekwaves is available now for $5,000. The package runs on Apollo Computer Inc. work stations under a variety of graphic environments, such as X Windows. It can handle simulation files from Cadat's HHB, Daisy Systems' VLAIF, GenRad's Hilo, Mentor's Quicksim, Teradyne's Lasar, and Valid Logic Systems' SIM simulators. The system produces test programs automatically for Tektronix' LV-500 ASIC Verifier; support for other testers will follow.

Tektronix is not alone in seeking solutions to the design-test dilemma. Systems from Asix Systems Corp. of Fremont, Calif., and Daisy Systems Corp. of Mountain View, Calif., can convert simulation vectors into test vectors, providing a solution for a specific set of hardware.

But one major competitor to Tekwaves that serves multiple simulators and test systems is PBridge from Test System Strategies Inc., a Beaverton neighbor of Tektronix. It has the current advantage of automatically creating tester-specific test programs for a wide variety of testers. Though Tektronix executives concede the broader support, they point out that the TSSI tool does not have graphical editing of the waveform and, at $20,000 plus $15,000 for required software, it's much more expensive than Tekwaves.

Finally, one other software product that addresses the testing problem much earlier in the design cycle than any of the competitors is the Test Assistant from VLSI Technology Inc. in San Jose (see p. 116). *–Jonah McLeod*

SHOWS

AT THE CICC, THE ACCENT IS ON ANALOG

SAN DIEGO

Of all the professional meetings attended by electronics-industry movers and shakers, the Custom Integrated Circuits Conference is the most accurate reflection of the preoccupations of original-equipment manufacturers and system designers. Most other IC conferences are technology-driven, motivated by the eagerness of chip designers and process engineers to show what they can do in terms of performance, density, and functionality.

USER-DRIVEN. But the CICC is, by and large, user- and customer-driven. Historically, many of the custom and semicustom circuits described at the annual clambake have been developed, designed, and—in the case of large vertically integrated OEMs—made by the users themselves. And the computer-assisted-design tools and methodologies described also mirror the concerns of OEMs and their systems designers as they assess the continuing trend toward higher speed and greater integration.

So OEMs are looking with great interest at this year's CICC, being held this month in San Diego, where three things are on everyone's mind: analog, analog, and analog. Of the 185 session papers, tutorials, and panel topics, 43% are devoted to analog or mixed analog/digital design, fabrication, and simulation.

Many papers reflect a concern with how to integrate analog and digital functions on the same chip, with higher density. Equally important is the development of design tools that simplify the process of analog design, making it as easy and automatic as digital. There is also a focus on improving the processing of analog and mixed analog and digital circuits in CMOS, bipolar, and biCMOS technologies. With biCMOS in particular, attention is being paid to processes that give users the power savings and density of CMOS plus the speed and enhanced linear performance of bipolar.

Why all the interest in analog? As the level of chip integration increases, designers and users are bumping up against an incontrovertible fact of life: the real world is analog. And the industry is aware of the need to address the issue of interfacing to the real world, according to Britain's Marconi Electronic Devices Ltd.'s IC Division. But for all the talk about its importance, there is little solid information about the functions needed.

To repair that omission, Marconi surveyed industrial-system designers and OEMs and came up with a CMOS-based set of analog functions that are compatible with the traditional double-level-metal interconnect approach used in digital gate arrays. It differs from the traditional analog tile-cell approach in that the array has no special areas set aside for specific analog functions. Also, it incorporates process features that can be used with equal advantage by both analog and digital designs.

Such simplification of analog design is being addressed on several fronts. One of the most ambitious is a design-automation system for analog circuits based on the oxymoronic concept of fuzzy logic and developed at the University of Tokushima in Japan. Rather than requiring the designer to develop a design completely by hand, the aim is a system that deduces automatically the optimum circuit values of an analog IC quickly and accurately. The system consists of a design program, a circuit simulator, and a fuzzy-logic rule base that is used to evaluate the suitability of a given circuit.

Here's how it works: the designer en-

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Now you can replace 27 ICs with only 5 chips using our new CacheRAM™, the IDT 71586. You can save two-thirds of your board space and reduce power consumption by a third. The IDT 71586 makes the ideal 2-set associative, 32 K byte cache. Optimized for Intel's 82385 cache controller, the IDT 71586 matches 33 MHz Intel80386™ designs with its 25 ns access time.

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25 MHz	35 ns
33 MHz	25 ns

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When cost-effective performance counts

Integrated Device Technology

Circle 26

ters the required specifications, and the system creates and simulates a draft design with a known configuration. Then a performance-suitability level is derived using the fuzzy-logic rule base. If the specs are not met, the rule base is modified until they are, on the known design. The debugged rule base is then used to design and simulate the new circuit. The loop is repeated for each of the specifications until all are met within the designer's predetermined limits.

SIMPLIFY DESIGN. Taking another path to analog design simplification, researchers at General Electric Co.'s corporate research and development center in Schenectady, N. Y., have devised a floor-planning algorithm strictly for analog circuits. Although several such techniques have been proposed in the past, all have had the unfortunate byproduct of lengthening the design cycle. But the GE method, based on the standard leaf-cell approach used in many of the digital methodologies, simplifies design and reduces design time as well.

Unlike the standard leaf-cell approach, in which sensitive and insensitive sides of each leaf are adjacent to one another, the analog leaf cells are arranged so that the sensitive sides are adjacent. This serves to form sensitive and insensitive channels. The sensitive are used for analog signal and power routing and the insensitive for digital.

Researchers at Carnegie-Mellon University in Pittsburgh are taking an even more comprehensive approach to the problem. Scientists in the department of electrical and computer engineering have created a design system called Acacia that automates the entire design path from specification to silicon for critical analog modules. Its proprietary interface allows analog designers to explore various circuit trade-offs automatically.

Two of Acacia's most important components are tools called Oasys and Anagram. Oasys provides a general framework for hierarchical synthesis of circuit schematics from performance and process specifications; it's also a synthesis tool incorporating knowledge of CMOS operational-amplifier and comparator design. At any level in the hierarchy, a set of block-diagram topologies is available, and heuristics are used to select the best approach. Oasys then employs approximate analytical equations to refine the block specifications into specs. It also incorporates algorithms for automatically generating schematic drawings.

The second tool, Anagram, transforms device-level schematics into mask geometry and operates like a digital macrocell place-and-route system. The macrocells can be individual devices, such as transistors and capacitors, or groups of devices with special matching requirements, such as differential pairs, matched switches, and large folded devices. Anagram places these blocks using an annealing algorithm and then routes them using a novel analog scheme that models noisy and sensitive wiring, crosstalk, shielding, and ground loops. Anagram has laid out a variety of Oasys-synthesized op amps and comparators with what the researchers describe as good accuracy—within 10% in most cases—considering the simplified device models used.

To bring automated analog design into the range of the average designer, a new CAD methodology, called Liberty, has been developed by Custom Arrays Corp. It can be implemented on a low-cost work station, much like digital design. The Sunnyvale, Calif., company's package consists of five modules: a schematic design-entry package, a Spice simulator, an interactive symbolic layout-design editor, a mask-pattern generator, and a proprietary logic-verification routine called Decorus, which supports design-rule and electrical-connectivity checking plus post-layout netlist extraction and schematic back annotation.

OEMs are bumping up against a fact of life: the real world is analog

Still, as important as automating the analog portion of a design is, it comes to naught if it can't be merged at the chip level with the digital portion. But design of analog and mixed-mode analog/digital application-specific ICs has lagged behind pure digital.

For one thing, analog performance is much more sensitive to the manufacturing process, says Edmund Chung, a researcher at Silicon Compiler Systems Corp. in San Jose, Calif. Then too, modeling analog circuits requires much greater accuracy than digital. Unlike digital ASICs, semicustom analog designs need elaborate characterization of the analog cells and frequent layout tweaking.

One approach to this problem comes from researchers at IMP Europe Ltd. in Swindon, UK. It makes use of so-called personalized cells, which are introduced to fit the specific needs of a design. Also factored in are layout-dependent circuit features that locate crosstalk, analog and digital noise, parasitic resistance, supply buses, and grounding.

Meanwhile, from the IC Design Center at the University of Hawaii comes a technique for constructing analog cells to be used in mixed analog/digital designs based on a technique reminiscent of the spreadsheet programs used in business. Applicable to both CMOS and biCMOS and scalable to below 1 μm, the technique is based on the tiling of modules using an internally designed layout editor. The editor incorporates a generic layout rule set that allows conversion between different mask rules and includes rules for two layers of polysilicon and for npn devices.

In this generic scheme, the first-layer metal always runs vertically within a module and is used to strap active contacts; second-level metal always runs horizontally between modules and is used, together with selective placement of vias, for interconnect. Since gates run vertically, gate width can be increased simply by adding modules in parallel. A spreadsheet-like program then performs various "what-if" analyses of different design alternatives, with the software calculating circuit specifications directly.

When the design is complete, the spreadsheet produces code to generate the layout using a tiling program. It also generates a Spice netlist, including parasitics, which checks the predicted performance. Used in several outside projects for industry, the new technique, the researchers say, resulted in the redesign of an existing op-amp cell library with 10% to 20% area savings.

A development that could lead to an industry-wide rethinking of the problem of mixed-mode simulation is iSPLICE3 from the Coordinated Science Laboratory in Urbana, Ill. Mixed-mode simulators let the designer trade off simulation accuracy for speed by representing different parts of the same circuit at different levels of abstraction and combining them into one simulation.

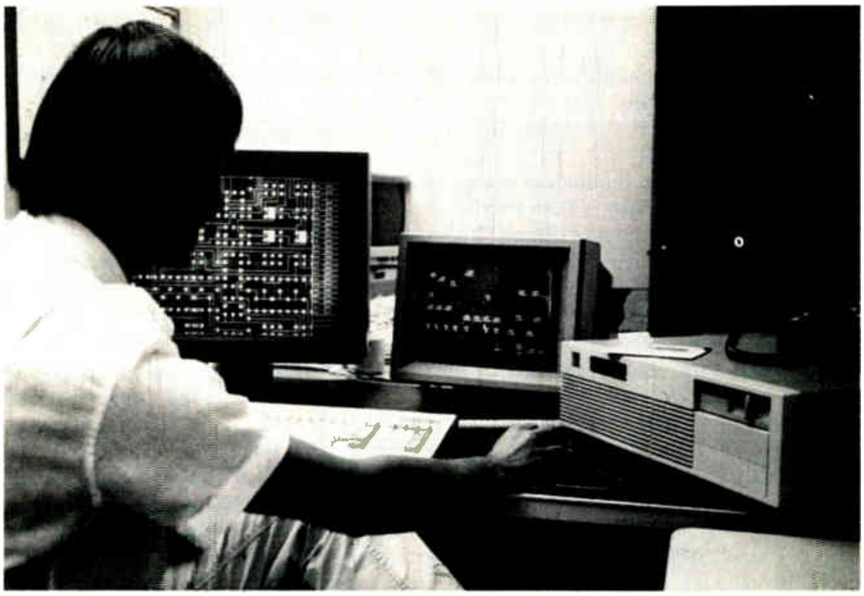
The iSPLICE3 program has a number of novel features. In the dc solution, for example, it uses a technique that is four to five times faster than the standard Newton approach on digital circuits. The circuit is first solved at time zero using switch-level simulation and logic simulation to derive the initial conditions at each node. Then the Newton method is applied. Since the Newton method relies on an initial guess being close enough to the eventual solution to guarantee convergence, using switch-level logic on initialization makes the dc solution more reliable.

SPICE INTERFACE. The company has also developed a unique interactive Spice interface with a schematic-entry capability and graphical display of simulation results. Using this tool, schematic designs may be entered, edited, and thoroughly analyzed within a common front end. In the simulation of a number of circuits, such as dynamic random-access memories, phase-locked loops, and analog-to-digital converters, it nets a tenfold speed increase over Spice implementations.

At the process- and circuit-design level, the problem of mixed analog/digital designs is being approached from three directions: CMOS, bipolar emitter-coupled logic, and biCMOS.

Most significantly, researchers at AT&T Bell Laboratories in Allentown, Pa., have developed a 0.6-μm analog CMOS technology that allows designers to add many analog functions to a digital technology without any appreciable change in the basic properties of the transistors. The resulting technology is suitable for applications requiring switched-capacitor filters, successive-approximation data conversion, and other combined analog and digital functions, according to the researchers.

The process is a modular enhancement of a fifth-generation twin-tub technology process developed for digital applications.



Custom Arrays' Liberty CAD system brings automated analog design within reach of the average designer, since it can be implemented on a low-cost work station like digital packages.

Systems to simplify analog design abound; one relies on fuzzy logic

Most of the additional analog processing occurs after the growth of a sacrificial gate oxide: a mask to block a threshold-adjustment implant from the low threshold n-channel devices, with a second one to allow a larger implant going into just the low-threshold p-channel devices. A capacitor bottom plate is built from a doped amorphous silicon layer; after patterning, the film is oxidized during the gate oxidation to form a double-poly capacitor.

At the high-speed ECL end of the spectrum, Applied Micro Circuits Corp. of San Diego and LTX Corp. of San Jose have developed a semicustom array that combines 100-ps digital speeds with high-speed RAM and precision analog performance. Based on a 14-GHz trench-isolated bipolar process, the new circuit, the Q20D080, combines a 1,024-transistor analog section with an 8,000-gate digital section and a RAM block organized as two 1,280-bit arrays.

Also garnering much attention are the bipolar/CMOS offerings, as much for their potential in mixed analog/digital applications as for their speed and density advantages. Examples come from Hitachi, NEC, Stanford University, the Technical University of Nova Scotia, Texas Instruments, and Toshiba.

Traditional switched capacitors have been limited to CMOS analog designs and lower performance ranges, well under 1 MHz. To push into megahertz range, the Nova Scotia group has built npn bipolar junction transistors on the same substrate with n-MOS and p-MOS devices using a p-well CMOS technology.

At Japan's NEC Corp., researchers in Kanagawa have developed a vertical pnp triple-diffused transistor to a 2-μm digital CMOS process. Measured unity-gain frequency in a single-supply op amp is 32 MHz, five times better than when a more traditional lateral pnp transistor is used.

The speed, density, and power advantages of biCMOS are not being ignored at this conference. One of the most aggressive designs comes from Tokyo's Hitachi Ltd., a 0.5-μm channelless gate array with an average gate-delay time of 220 ps, twice as fast as that of CMOS with similar capacitive loading. This speed is only slightly slower than bipolar ECL, but the power dissipation is about one tenth. The Hitachi scientists have built a 54,000-gate array without dedicated routing areas. Using more conservative 1.2-μm design rules, NEC's biCMOS gate-array family is capable of 270-ps gate delays with densities up to 24,000 gates.

With a 0.8-μm CMOS process only slightly less aggressive than Hitachi's, Texas Instruments Inc. of Dallas has been able to achieve much higher densities—up to 100,000 gates or more. In exchange for the density boost, the TI offering sacrifices some gate delay, about 360 ps, making it 30% slower than the Hitachi array. *–Bernard C. Cole*

Next-generation analog: Advanced Linear ICs

A new breed of linear chips, born of leadership processing at Texas Instruments, can help you design superperformance systems.

Sophisticated design and simulation tools shorten development cycles of TI's Advanced Linear ICs, helping you get to market faster. By using these tools, TI can offer as standard circuits many designs that previously would have had to have been customized.

The human brain has separate but dependent left and right sides. Similarly, an electronic "brain" or system has separate but dependent parts, one digital, one analog. Designers accustomed to the spectacular performance gains made in digital chips are now demanding comparable improvements in analog devices so that both parts of their systems can function to full potential. Leading the analog evolution: Advanced Linear circuits from Texas Instruments.

These new chips are called *advanced* for one or more reasons. They are more highly integrated than ever before, often combining digital and analog functions on a single chip. They offer higher performance and greater flexibility. They are often the result of advanced processing that may merge two or more technologies.

Better parameters from better processing

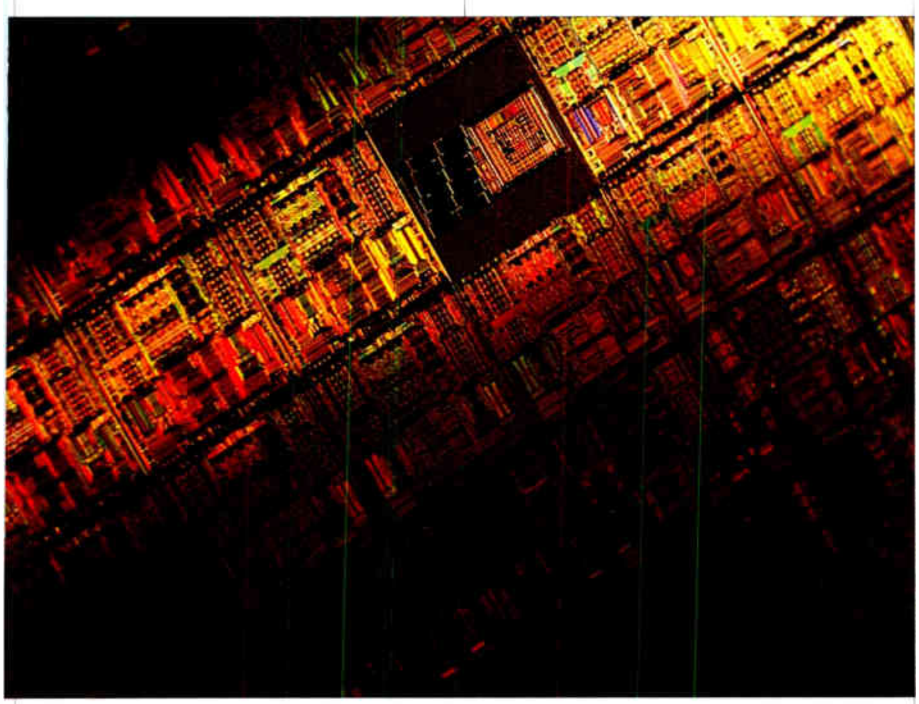
Because advanced analog system requirements for performance and flexibility vary greatly, a single workhorse technology typically can't do the job any longer. Nor can creative circuit designs alone. We at TI are convinced the key to driving the linear evolution lies in the excellence of our processing technologies.

TI is committed to developing and implementing a range of leadership wafer-fabrication processes (*see descriptions on back page*). The result: TI's Advanced Linear devices are already helping system designers link digital brains to advanced analog worlds more efficiently and with greater ease in many applications. Here are a few examples.

Advanced Linear: Displaying greater brilliance

Out of our pacesetting LinEPIC™ processing comes our high-performance Color Video Palette, operating at 125 MHz with a very high-resolution 1024 x 1024 pixel count. Because of one-micron CMOS processing, power consumption is reduced more than 40% compared to other CMOS implementations. Additionally, the device is pack-

...the key to driving the linear evolution lies in the excellence of processing technologies.



High-density Analog Interface Circuit chips demonstrate the greater integration achieved by TI's innovative linear processing technologies. These DSP interfaces allow you to alter circuit configuration under software control without external adjustments.

aged in reliable, economical plastic.

LinEPIC has also produced such high-speed, high-density interface chips as our Flash A/D and our Video DAC for use in graphics displays, imaging systems, monitors, and cameras. Both devices require about five times less power than bipolar equivalents.

Advanced Linear: Intelligent power for every car

Chips fabricated with our Power DMOS-based BIDFET™ processing are replacing electromechanical relays in many automotive applications, such as driving headlamps and motors. Power BIDFET allows us to minimize power loss in the switch and add high-complexity logic functions.

Multi-EPI bipolar processing, a very cost-effective technology, is used to produce chips having inherent reverse battery protection and high operating voltages. Such chips are ideal for use in automotive antilock braking systems, electronic transmissions, and active suspension systems.

Either technology can produce devices with low-side drive, high-side drive, or H-bridge configurations.

In the future, these developments may lead to multiplexed systems for cars, replacing bulky wiring harnesses.

Advanced Linear: Enhancing modems and facsimiles

TI's dual driver/receiver is a good example of the integration achieved with advanced processing technologies. LinBiCMOS™ processing has enabled us to put the drivers and receivers needed for RS-232 voltage levels on the same chip with the charge pump required to generate the necessary split rails from a single 5-V supply. You eliminate external power supplies and get a device that's easier to design with—it is available in our LinASIC™ cell library for integration with digital ASICs.

A new family of Analog Interface Circuits (AICs) is emerging from our Advanced LinCMOS™ processing. The voice-band AICs, designed for modems and fax equipment, combine high-performance analog functions—14-bit A/D and D/A converters and switched capacitor filters—with digital functions such as control circuitry, program registers, and DSP interface. The usual clutter of resistors, capacitors, and pots is eliminated.

High-speed AICs are available for use in servo controllers and hard-disk-drive applications.

These AICs are also high-performance members of our LinASIC standard-cell library. Based on TI's proven digital ASIC methodologies, the LinASIC library has allowed us to develop complex, semicustom chips in as little as 16 weeks.

Advanced Linear: Boosting instrumentation accuracy

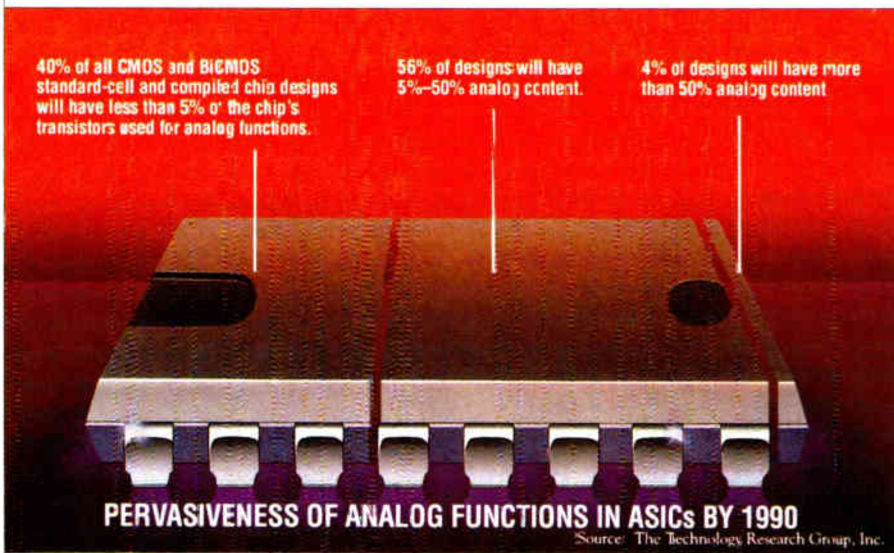
Even one of the most basic analog building blocks, the operational amplifier, is benefiting from TI's Advanced Linear technologies. Our Excalibur op amp family combines low power consumption with a 5X speed improvement while retaining low offset voltages. Offset-voltage drift has been cut from 300 µV to 60 µV to reduce your calibration, test, and measurement expenses.

For high-accuracy applications, Advanced LinCMOS is making possible Chopper Stabilized Op Amps with chopping frequencies 10 times higher than previously available (10 kHz). Noise levels are the lowest on the market.

The evolution in analog devices has only begun. Dramatic progress lies ahead throughout the 1990s. As the Advanced Linear leader, Texas Instruments is pledged to remain at the forefront, supplying you with new ways to link digital brains to advanced analog worlds.

For suggestions on choosing a linear supplier, turn the page.

A PERSPECTIVE ON ANALOG SYSTEM DESIGN



Circuits combining analog functions with digital logic will soon be widespread in ASIC chip designs. TI is taking a leadership role with the development of its LinASIC methodology.

Checkpoints for choosing an analog supplier in the 1990s.

Questions and answers with Tom Engibous, Vice President, Semiconductor Group, and Manager, Linear Products, Texas Instruments Incorporated.

Q. What is the first thing to look for in choosing a linear supplier?

A. Product performance is definitely the first priority. Our customers are asking for ever-increasing linear device performance. At TI, we believe creative circuit designs alone won't meet the challenge. Advanced process technologies—note the plural—are becoming the keys to success in linear device performance of the '90s.

Q. What else should a designer look for?

A. Whether or not the supplier has experience with digital as well as analog devices. These two worlds are merging (*see chart above*). Functions once performed by analog are now done digitally, and a growing percentage of our Advanced Linear devices combines analog and digital circuitry on one chip.

At TI, we've leveraged our 30 years of digital expertise into the development of our Advanced Linear products and processing with highly satisfactory success. This has been especially noticeable with our LinASIC methodology.

Q. Do you expect ASICs to play a major role in your linear future?

A. Very definitely, as they already do today. Cell-based designs will be the rule in both user-specified functions and highly integrated standard products. Digital ASIC methodologies are also the key to cutting system design cycles. As our digital experience proves, suppliers who have advanced process technologies and fast, accurate design-automation tools will be the best equipped to deliver single-chip solutions.

Today, we have customers doing their own LinASIC designs using our advanced processes and design-automation tools.

Q. What role does manufacturing capability play in picking a supplier?

A. It is always a factor, and the need for efficient worldwide manufacturing facilities such as TI has in place will become even more important. Today's semiconductor market is global in nature. You can't serve worldwide customers from a single plant—you have to be "multilocal." This is particularly true with ASICs.

Q. Any other important factors?

A. Yes, I'd suggest that, in choosing a linear supplier, the designer find one he can live with for a long time. Close supplier-customer relationships are essential to the development of products that will provide the highest performance and lowest cost systems.

TI's Leadership Linear Processing Technologies

LinBiCMOS—Combines Advanced LinCMOS, digital ASIC CMOS, and up to 30-V bipolar technologies to allow the integration of digital and analog standard cells and handcrafted analog components on a monolithic chip.

LinEPIC—One-micron CMOS double-level metal, double-level polysilicon technology which adds highly integrated, high-speed analog to the high-performance digital EPIC process.

Advanced LinCMOS—An N-well, silicon-gate, double-level polysilicon process featuring improved resistor and capacitor structures and having three-micron minimum feature sizes.

Power BIDFET—Merges standard linear bipolar, CMOS, and DMOS processes and allows integration of digital control circuitry and high-power outputs on one chip. Primarily used for circuits handling more than 100 V at currents up to 10 A.

Multi-EPI Bipolar—A very cost-effective technology that utilizes multiple epitaxial layers instead of multiple diffusion steps to reduce mask steps by more than 40%. Used to produce intelligent power devices that can handle loads as high as 20 A and voltages in excess of 100 V.

Excalibur—A true, single-level poly, single-level metal, junction-isolated, complementary bipolar process developed for high-speed, high-precision analog circuits providing the most stable op amp performance available today.

Our just-published *Advanced Linear Circuits* brochure examines more fully the changes taking place in analog system design and their impact on linear devices. The brochure also describes TI's leadership processing technologies and explains the performance improvements that result. **For your copy, call 1-800-232-3200, ext. 3407, today.**

TEXAS INSTRUMENTS

WASHINGTON INSIDER

DARPA SEEKS TERA-OPS SPEED FROM REVAMPED STRATEGIC COMPUTING PROGRAM . . .

The Defense Advanced Research Projects Agency is now sorting through industry proposals designed to guide its Strategic Computing Program into the next generation of computer performance. "We are in the process of redirecting [the program] toward a new set of goals," says Darpa's outgoing director, Raymond Colladay, who is leaving this month to join industry. He says Darpa has "achieved the kinds of goals we set out to get five years ago"—namely, massively parallel computer designs based on standard microprocessor architectures and capable of 10 billion instructions/s. Now the agency is seeking to up the ante still further, targeting more advanced microprocessor technology, three-dimensional chip-packaging techniques, high-speed gallium arsenide digital circuits, and optical interconnects—all with the aim of getting a computer that runs a trillion operations/s. In conjunction with the National Aeronautics and Space Administration, it's also going after a nationwide distributed computing network with data rates in excess of 1 gigabit/s. "We think we realistically can achieve these goals by the mid-1990s," Colladay says. Key to the effort will be advanced chip and packaging technologies designed to squeeze the maximum computing punch into the smallest space. Hoping to boost the intelligence quotients of future missiles, aircraft, ships, and portable battlefield equipment, Colladay says, "We're shooting to get gigaflops performance in a soup-can-like volume." □

. . . AND FUNDS INTEL TO DESIGN 2,000-PROCESSOR COMPUTER BASED ON i860

The goal: a massively parallel computer that's 2,000 times faster than a Cray 1 supercomputer yet as simple to use as today's technical work stations. The trick: a massively parallel architecture linking 2,000 of Intel Corp.'s most advanced microprocessors, including the fast-as-a-Cray i860 [*Electronics*, March 1989, p. 25]. A full configuration, Intel says, will be capable of running 128 billion 64-bit floating point operations/s. The Santa Clara, Calif., company expects to spend $27.5 million on the project, to be called Touchstone, over the next three years, of which Darpa will contribute $7.6 million. Development will focus on system software to harness the powerful Touchstone computer; a high-speed communications network to tie all the processors together and distribute data at speeds over 100 Mbytes/s; and advanced packaging technology that will allow the prototype machine, which is due in 1991, to operate in an air-cooled environment, rather than the liquid-cooled environments used for today's most advanced supercomputers. □

AT THE HEART OF SDI'S ANTIBALLISTIC MISSILES LIE THE GUTS OF A PC

The microprocessor that powers an experimental antimissile weapon now under development for the Strategic Defense Initiative is the same one that runs many top-of-the-line desktop computers: Intel Corp.'s 80386. That chip, surrounded by a set of semicustom gate arrays built with Very High Speed Integrated Circuit technology, enables the Light-weight Exo-Atmospheric Vehicle developed by Hughes Aircraft Co. to process more than 100 images/s and track down a soaring nuclear missile, says Mick Blackledge, assistant director for interceptors and command control at the SDI organization in the Pentagon. The unit receives the images from a mercury-cadmium-telluride infrared focal-plane array with 128-by-128-pixel resolution. The Hughes projectile's intelligence comes from an 80386-based CPU that can calculate 4.2 million instructions/s at a sizzling 300-MHz clock rate. What's more, all that computing power fits into a 1-kg package. That's 6.3 kg lighter than the data-processing module inside the Advanced Medium-Range Air-to-Air Missile—and six times as fast. The next step? Shrinking the processor board to an even smaller 0.3 kg and forging the circuitry in radiation-hardened silicon. □

WASHINGTON INSIDER

MIMIC SCORES ITS FIRST INSERTION: THE HARM MISSILE . . .

Texas Instruments Inc. is building advanced monolithic amplifiers into its High-Speed Anti Radiation Missile, marking the first application of technology developed under the Pentagon's Microwave and Millimeter Wave Integrated Circuits Program. The eight amps, fabricated in gallium arsenide by one of four Mimic teams, a TI-Raytheon Co. joint venture, replace hybrid devices that were included in the HARM's original design. The result is a "part-count reduction that's a factor of four fewer parts and interconnects," says Dave McQuiddy, TI's Mimic program manager. That translates into a two- to tenfold reliability improvement, he adds. It also means savings: hybrid yields are low, and when parts don't meet rigorous performance specifications, they have to be manually tuned, which dramatically increases labor and cost. The new monolithic devices, however, sport very good first-pass yields, McQuiddy says; and since wire bonding and rework are eliminated, manufacturing costs are one half to one quarter what they were for the hybrids. □

. . . AND SEEMS TO BE OFF TO A FASTER START THAN VHSIC

The effort to develop a set of monolithic amplifiers to replace the hybrid components in the HARM missile predates the Pentagon's Mimic program by at least a year, but it underscores how Mimic program managers learned from mistakes made in the Very High Speed Integrated Circuits program. Unlike their VHSIC counterparts, Mimic contractors were required to closely tie their efforts to ongoing weapons-system development from the start, so that the Defense Department's $230 million investment in Mimic technology over the next three to four years could be leveraged as quickly as possible. As a result, while VHSIC contractors are still struggling to find programs interested in their wares, Mimic technology is taking an express route into systems. Without Mimic, "I'm not so sure we'd be this far along with the HARM," says Dave McQuiddy, Texas Instruments Inc.'s Mimic program manager. The program helped TI "work through all of the wickets" in the technology-insertion process much faster, he says. Most VHSIC parts, by contrast, were generic technology test vehicles that never found their way into real systems. "It looks like our market penetration will happen much faster than was the case with VHSIC," says Eliot Cohen, the Mimic program manager at the Defense Advanced Research Projects Agency. The Air Force's Anti Medium-Range Air-to-Air Missile program and the Navy's Global Positioning Satellite project are likely to join the Mimic bandwagon shortly. □

BAD TIMES IN THE DEFENSE INDUSTRY ARE GETTING WORSE

Defense electronics companies aren't doing enough to help themselves in a hotly competitive and shrinking market, industry insiders say. While the Justice Department is making hay with its ongoing Pentagon procurement investigation and Congress is continuing to threaten defense industry players with tighter restrictions, most defense companies are just rolling over and playing dead, says Anthony Battista, who resigned as head of the House Armed Services Committee staff 18 months ago to become a consultant. The industry, he says, is too worried about its public image and has been battered into submission by the media. "Now there's excess capacity relative to the money being spent," Battista says. "We're in for a mighty tough time, with a lot of Chapter 11 [bankruptcies], especially at the smaller companies." But big companies are in trouble too. Companies like Grumman Corp. and GTE Corp., which are now winding down major military programs, face the 1990s with no big revenue producers in sight. Says one worried GTE planner: "We're in a position where if we don't win a couple of big things now, we're going to see a real big downturn around 1991 or '92." □

Sizing Up the Earth in 200 B.C.

Eratosthenes believed the earth was round. As director of the great library at Alexandria in Egypt, he decided to go beyond abstract argument and actually measure it to back up the argument.

Eratosthenes

Knowing that the midsummer noon sun shone straight down a vertical well in Syene far to the south, he measured the slight angle of the sun's shadow in Alexandria on the same day. He figured the distance between the two cities by how long it took a camel to walk there. Then, with a little simple geometry, Eratosthenes came up with fairly accurate figures for the earth's circumference and radius. His pioneering measurement made a significant impact on history.

Communications Support for 2000 A.D.

Today, Anritsu's pioneering efforts in communications measurement are also paying off. Anritsu has long been a leader in the most sophisticated measuring methods, and continues to reach new levels of accuracy. The complex technologies behind modern multiplex techniques, for example, demand the highest degrees of precision. That's why carriers and manufacturers alike turn to Anritsu for the answers when it comes to accurate measuring and test equipment for communications.

Anritsu continues the pioneering tradition in measurement.

MP1601A 5GHz Pulse Pattern Generator

Anritsu

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Circle 55

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Circle 21

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EUROPEAN OBSERVER

COMING: A 5-GIGAFLOPS SUPERCOMPUTER FROM WEST GERMANY

Joining the small ranks of high-performance supercomputer makers, Suprenum GmbH of Bonn has unveiled the first clusters of a system that, fully configured, will boast a computing power of 5 billion floating-point operations per second. That performance would put the machine in the class of supercomputers built by the likes of Cray Research Inc., Fujitsu Ltd., and Hitachi Ltd. The system, also called Suprenum, is the result of a four-year research and development effort at a number of West German universities, institutes, and industrial firms. Suprenum GmbH coordinated the project and is marketing the machine, which carries a $14 million price tag. The company says it has already held sales talks with 10 research institutes and universities in West Germany. Suprenum plans to extend its marketing effort to the rest of Europe next year and eventually to sell its system in the U. S. The first Suprenum clusters, each consisting of 16 processing nodes that together offer 320 megaflops of computing power, debuted at last month's Industrial Fair in Hanover. A fully configured system, slated to be available by year's end, will comprise 16 clusters, making for a total of just over 5 gigaflops. □

PHILIPS BUILDS A DEFENSE AGAINST TAKEOVER BIDS

Speculation about an unfriendly takeover of Philips International NV in the Netherlands should end now that the company has bolstered its defenses. The Eindhoven-based electronics giant gained some takeover insurance by altering its so-called Articles of Association agreement with its holding company, NV Gemeenschappelijk Bezit van Aandeelen Philips' Gloeilampenfabrieken—Bezit, for short. At the annual shareholders meeting last month, the authorized share capital of Bezit was doubled, from 5 billion to 10 billion Dutch guilders (about $4.74 billion). The move gives Philips a combination of priority shares and the power to issue preference shares that it can use to counter a hostile takeover attempt. The shareholders also moved to set up a foundation that will be granted an option on Bezit's preference shares to be exercised if an unfriendly takeover is attempted. There has been some speculation in the West German press that Japanese companies may be interested in taking over Philips to gain a foothold in the unified Western European market, which is scheduled to become a reality by 1992. □

SIEMENS ANTICIPATES A BOOM IN WORK-STATION SALES

Work stations are turning out to be one of Siemens AG's hottest items. Last year, the Munich-based company sold $54 million worth of its Sicomp WS30 work stations. That works out to more than 2,000 machines and a 40% increase over 1987 sales. Siemens expects this year's sales to increase by another 40%, thanks largely to the introduction of two new models: the Sicomp WS30-430 and WS30-450. At the heart of these machines are the MC68030 microprocessor and the MC68882 floating-point processor. Working at 25 and 33 MHz, respectively, the new systems operate at from 4 million to 8 million instructions per second. □

TOSHIBA TO MAKE LAPTOP COMPUTERS IN WEST GERMANY

With demand for its laptop computers on the rise in Europe, Toshiba Corp. of Japan is drawing up plans for a production facility for the machines in West Germany. The plant, expected to begin production next spring, will be located in Regensburg, Bavaria, and will be run by Toshiba Europa GmbH. Initially, the plant will turn out 5,000 laptops a month, but Toshiba expects it to be producing 20,000 machines a month by 1993. Toshiba's goal is to produce half of all the laptops it sells in Europe in Regensburg. □

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Part #	16-bit Timers	UPI	I/O	Memory ROM	Memory RAM	Features
HPC16003*	8	Yes	32	0	256	4 ICRs
HPC16004	8	Yes	32	0	512	4 ICRs
HPC16064	8	Yes	52	16K	512	4 ICRs
HPC16083*	8	Yes	52	8K	256	4 ICRs
HPC16104	8	Yes	32	0	512	8 CH A/D
HPC16164	8	Yes	52	16K	512	8 CH A/D
HPC16400	4	No	52	0	256	2 HDLC & 4 DMA
HPC16083MH	8	Yes	52	8K UV	256	UV Emulator

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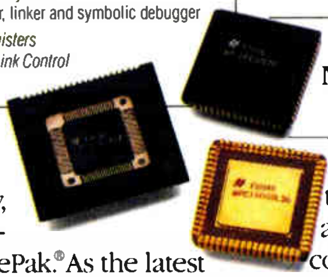

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National Semiconductor

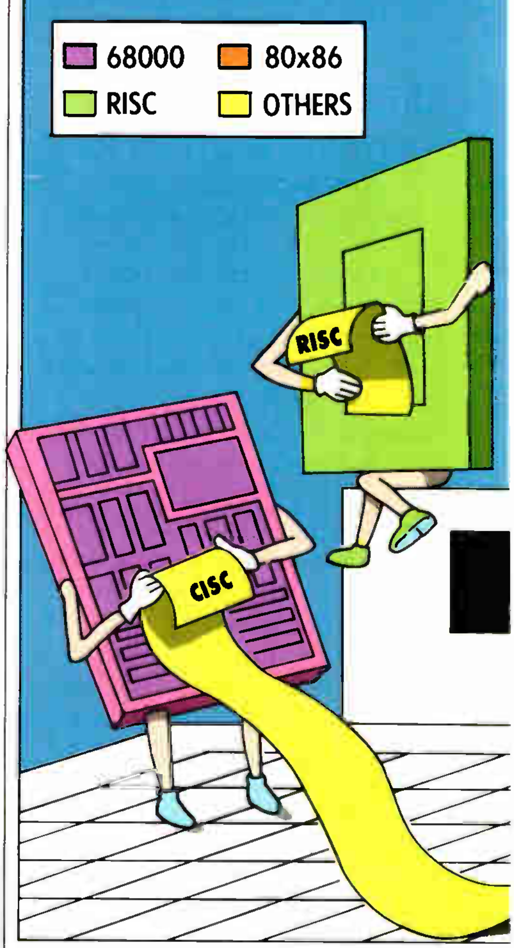
Circle 13

BY JONAH McLEOD

TOUGH CHOICES AHEAD

The new processors bring more power for the desktop—and hard decisions for OEMs

RISC VS. CISC: WHERE THE MARKET'S HEADING



The latest crop of microprocessors gives designers more power to work with than they've ever had—they can put on a desktop a machine that's the equal of a first-generation supercomputer. At the same time, the newest processors are confronting original-equipment manufacturers with harder decisions than they've ever had to make.

They must choose among RISC, CISC, and CRISP architectures—reduced-instruction-set, complex-instruction-set, and the hybrid that mates the two, complex-reduced-instruction-set computing—and then among an increasing number of different implementations of those architectures. Those decisions involve a series of calculations about which trade-offs to make. The designer can choose RISC for its performance, but in doing so he will sacrifice access to a vast installed base of systems and applications software written for CISC. He can try to have it both ways by using one of the new CRISP chips, but that leaves him wondering whether he's ignoring what seems to be the wave of the future, RISC, and heading down a technological dead end.

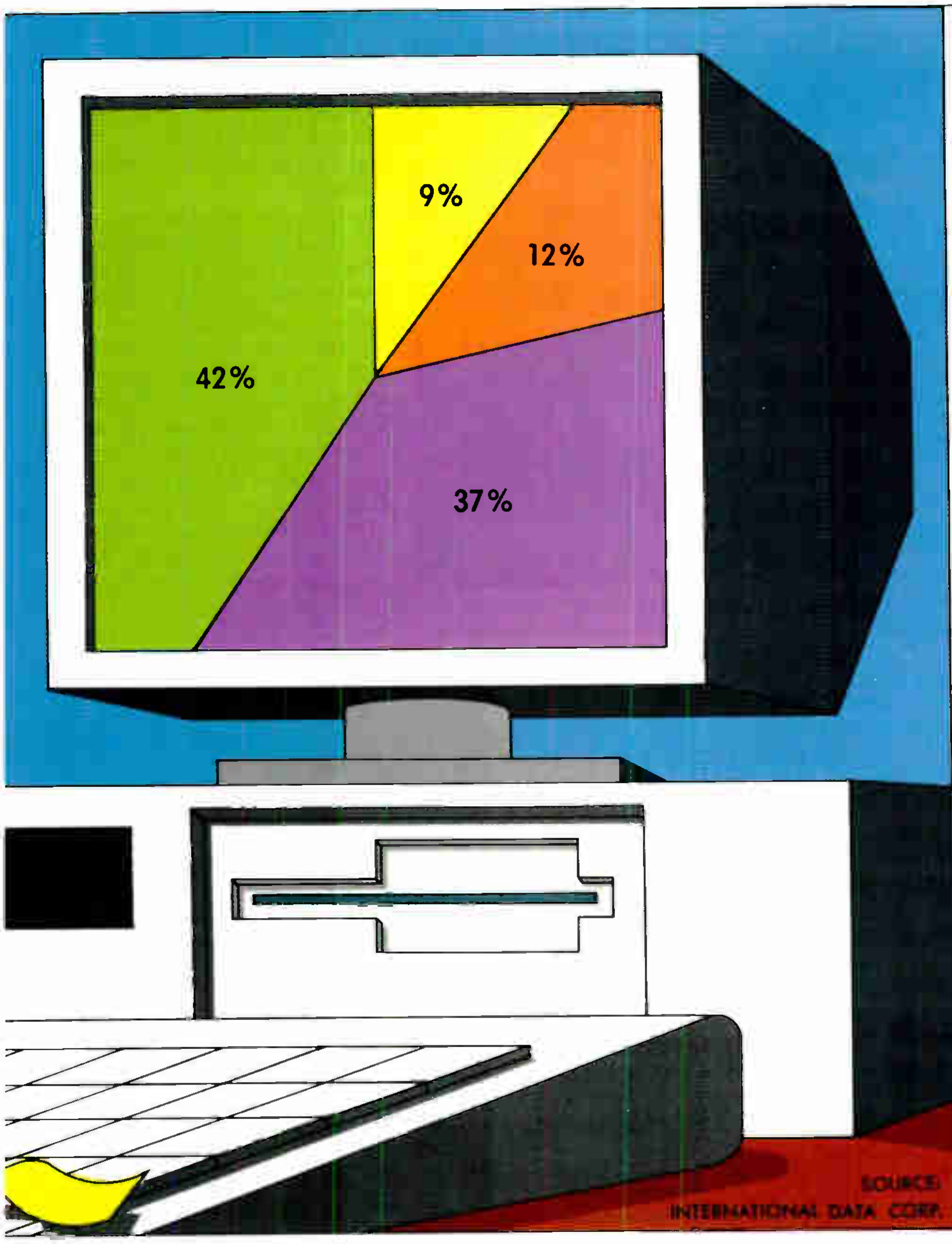
All of the confusion stems from several trends in technology that arose early in this decade and now are converging. A revolution in architectures is culminating in sophisticated reduced-instruction-set computing. Rapid advances in semiconductor process technology are producing chips holding up to a million transistors. Vast strides in circuit design are making it possible to cram more and more features onto those chips.

The most important of these trends is the emergence of RISC chips and RISC-based systems. "RISC processors replaced the instruction microcode in the random-access memory of CISC processors with the instruction cache in which optimizing compilers generate highly efficient binary code," says Mike Butts, senior research engineer at Mentor Graphics Inc. in Beaverton, Ore. As a result, he says, RISC-chip makers could build a complete central-processing unit on a single chip sooner than CISC-chip makers could. Having the whole computer on a single chip boosted performance by eliminating delays in signals going on and off the chip.

A year and a half ago, RISC processors appeared that offered performance of 10 million instructions per second and more. The CISC processors available then—including the Intel Corp. 80386 and the Motorola Inc. 68020, the two most widely used commercial chips—could provide only 2 to 3 mips. Market pundits began predicting the death of CISC processors and CISC-based systems.

But the reports of the death of CISC are highly exaggerated. At least two factors assure it a measure of good health for some time to come. One is the installed base of machines built around the existing CISC-chip product lines or, more precisely, the software written to run on those machines. The other is the potential that exists in the newest class of semiconductors, with their million transistors and enhanced circuit designs.

The existing CISC software amounts to a huge reservoir of customers for hardware built around the two most important CISC processors, the Intel and Motorola chips—a reservoir of customers no



OEM can afford to ignore. "There are around 4,000 applications written for 68020-based Unix platforms," says Travis Lutton, editor and publisher of *PC/ Workstation Wars*, a San Jose, Calif., monthly newsletter on work stations. "But only around 400 have been written for RISC-based work stations." In addition, there are 2,200 applications running under Xenix on the 80286- and 80386-based computers, says Richard Yanowich, the manager of developer relations and market development at the Santa Cruz Operations in Santa Cruz, Calif.

Both users and software developers have a vested interest in this installed base. For their part, users have a wide variety of different applications available on these CISC-based platforms. And applications developers can add more features and functions to existing software to take advantage of the increased computing power of next-generation platforms. Or they can write new programs that can sell into a large installed base of compatible systems.

Porting that software to a new platform is expensive and time-consuming, no matter how clean the new architecture or how compatible the compilers on different platforms, says Butts at Mentor. Developing and maintaining two separate sets of software starts to cost a significant amount of money after a while. Mentor's product line comprises around 5 million lines of source code; doubling that amounts to a substantial investment in programmers' time.

In addition, getting software developed for a new platform is a Catch-22 situation. Software developers are reluctant to create programs for a platform until it has a decent number of users. Users are reluctant to buy the platform until it has a respectable amount of software that can run on it.

The advantage that existing CISC chips have in software ties into the potential that opens up for them with the newer, bigger semiconductors. Using the enormous number of transistors now available and working with far more effective circuit-design tools, CISC-chip makers are creating what amounts to a new class of microprocessor: the CRISP chip.

Both Intel and Motorola's newest chips—the 80486 and 68040, respectively—qualify for the new designation. They incorporate RISC-like features to run in under two clock cycles instructions that once took four to six cycles, and they take advantage of more transistors and better design to cram onto one chip floating-point and memory-management units and caches to further boost performance. Both rival RISC chips in their power—but at the same time they are direct descendants of their CISC predecessors, and so they maintain software compatibility with them. The immense library of CISC-based applications packages is available to their users.

"Having less than two cycles per instruction on a CISC machine means that frequently executed instructions such as Load, Store, and Add are implemented in hardware rather than microcode," says Mentor's Butts. That takes more gates, of course, "but with 1 million gates possible on a chip, CISC designers have gates to spend," he says.

Both new chips incorporate an integer unit that is fully compatible with earlier members of their families. Both of them contain MMUs that first appeared on-chip with the previous-generation 80386 and 68030. However, both companies have improved the MMUs on the newer devices to up performance. For example, Motorola added two independent address-translation caches to the 68040 paged-MMU which allow simultaneous translation of both instruction and data accesses.

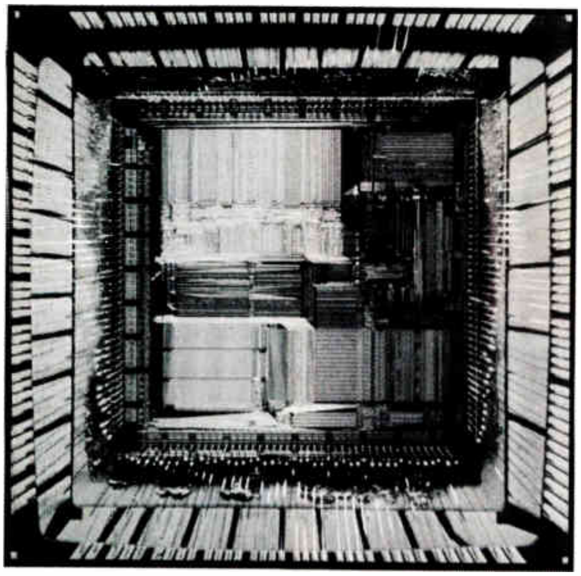
Both processors have on-board four-way set-associative caches. The 80486 has an 8-Kbyte shared cache. The 68040 has separate address and data caches, although Motorola will not reveal their capacity. With the MMU's address-translation caches, the independent address and data caches allow the 68040's integer and floating-point unit to access the instruction and data cache simultaneously.

That means the on-board floating point

units—something not available on either of the predecessor chips—execute in parallel with the integer units. In addition, the same kind of RISC-like design techniques enhancing the integer-unit performance are used in the floating-point units. Motorola also hardwired some instructions in the 68040 and added capability to perform transcendental functions, says Jeff Nutt, Motorola's technical marketing manager.

For the time being, then, the older CISC architectures, at least in the form of the CRISP hybrids, are not only unendangered but prospering. Nevertheless, it looks as if in the long run the field belongs to RISC. Ironically, the same factors that are prolonging the life of the CISC architectures eventually will begin to work in favor of RISC. Further developments in software combined with big chips and the attendant improvements in design can do just as much for RISC as they do for CISC.

In software, the major restraint on developing applications for RISC-based systems is the Catch-22: system builders look for users before they will commit to a processor and therefore spur software development, but users won't commit to a processor until enough software is written for it to make a worthwhile system. The vicious circle is already on its way to being broken. Software developers are willing to invest in a separate, RISC-oriented version of an application if the application benefits sufficiently from running on a machine with the improved performance of RISC.



Motorola's 88000 RISC series is built around the CPU, this 88100 cache/MMU chip, and the 88200, another memory chip.

Mentor Graphics has ported its software to the DN10000, the RISC-based work station from Apollo Computer Inc. of Chelmsford, Mass., to cite one example. Daisy-Cadnetics Inc. in Boulder, Colo., is now adapting its software to the entire family of work stations from Sun Microsystems Inc. in Mountain View, Calif., to cite another.

The willingness to adapt software to new platforms will increase dramatically if a standard operating-system environment is established, cutting across architectural lines. Such an environment seems virtually assured. The efforts of organizations like the Open Software Foundation and Unix International eventually will make some version of the Unix operating system a standard.

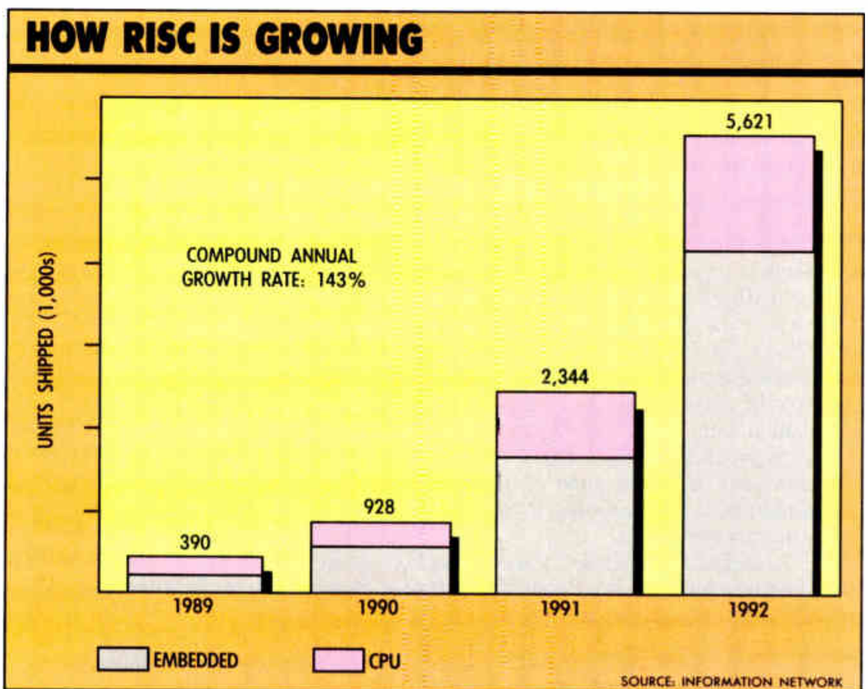
Daisy-Cadnetics is already moving in that direction by adapting its software to run on a variety of different platforms. The mechanism is a set of interface libraries, says David Neihaus, director of systems marketing at the company. Applications programmers write to the interface, and proprietary algorithms inside the libraries ensure the software will run on any of six platforms in the Daisy product line without sacrificing performance. The libraries also include Sun's XDR protocols, to handle the byte ordering between different platforms. The idea is that software developers writing applications to execute on a core set of Unix functionality can transport their code from one hardware to another by merely recompiling the source code.

A project at Mentor called Falcon aims at the same transportability, says Steve Swerling, vice president of technology and a founder of Mentor. The company is trying to develop an underlying modular and transportable software architecture that can run on any hardware.

POWERFUL MOTIVATOR. And just as it becomes easier to write software for RISC machines, another powerful motivation is emerging to impel software developers to create RISC-oriented applications: the same improvements in chip capacity and design capabilities that make CRISP chips possible. In effect, bigger, more sophisticated chips give RISC the same performance boost they give to CISC. Hence, the advantages in performance to be derived from RISC programs are growing.

With a million transistors, RISC-chip makers can use the same techniques CISC-chip companies are using to create CRISP. They can put multiple integer and floating-point processing units and larger caches on a single chip. But instead of enabling the processors to execute instructions in under two clock cycles, as they do with CRISP chips, the advantages in number of transistors and circuit design will enable RISC chips, with their inherently greater speed, to execute instructions in a fraction of a single clock cycle. About the only restraint on RISC-system proliferation that will be left is the necessity to create efficient compilers that can exploit the full potential of RISC architectures. Developing such compilers is not a significantly difficult feat—it's not simple, but the techniques exist.

In time, then, RISC's domination of the



microprocessor world is inevitable, barring the development of some unforeseen technology that will eclipse RISC, CISC, and CRISP alike. The trend is evident in the market projections people are making for the various architectures.

For example, International Data Corp., the Framingham, Mass., market-research firm, expects sales of all work stations to grow at a compound annual rate of over 36% through 1992. But work stations built around RISC chips will grow at 83%, from 50,000 units shipped this year to 225,000 units in 1992. Of the 540,000 work stations of all kinds expected to ship in 1992, IDC predicts 42% will be RISC-based machines, 37% CISC-based, and the rest CRISP or some other architecture.

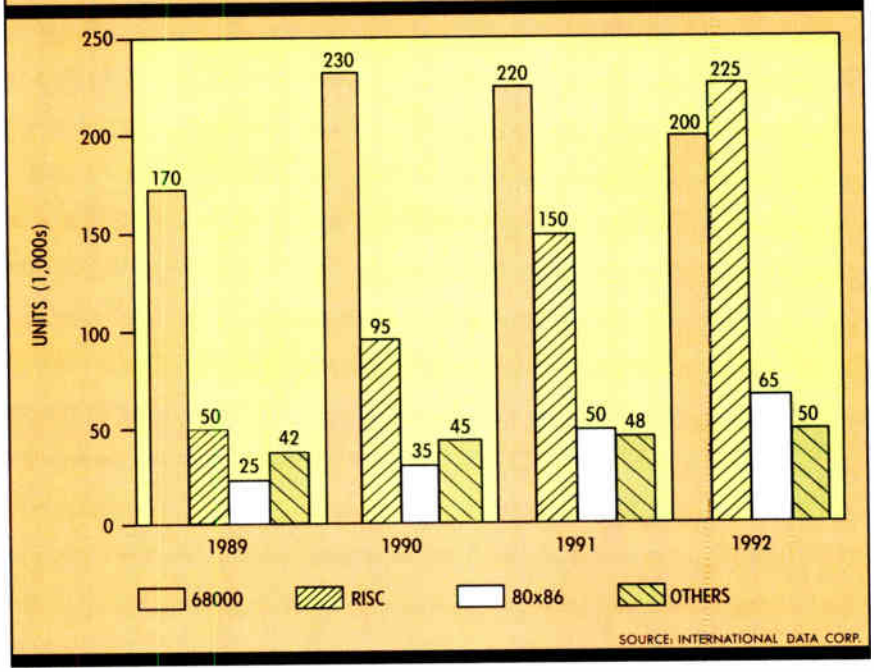
Perhaps the greatest evidence that RISC is the wave of the future is not market figures but the actions of the market leaders. Both Intel and Motorola, the leading sellers of conventional CISC processors, have introduced RISC processors of their own. Intel's chip, the 80860, is the newer of the two, arriving a little more than two months ago [*Electronics*, March 1989, p. 25]. Motorola's 88000 came out a little more than a year ago [*Electronics*, April 28, 1988, p. 75].

A FIRST. The 80860 from the Santa Clara, Calif.-based Intel is the first RISC processor to take advantage of the chip capacity made possible by the latest semiconductor technology. Along with the 32-bit integer processor—which uses a very small set of 32 instructions—are a floating-point unit, memory-management unit, graphics processor, and cache. Connecting all of them is an extensive network of 64-bit-wide buses moving data at the rate of a gigabyte per second around the chip. Most other RISC chips have a 32-bit internal architecture.

However, Intel's competitors say the compilers for the Unix operating system are, so far, not sufficiently developed to make the chip a competitive threat. Intel announced C and Fortran compilers and Fortran vectorizers when it introduced the chip.

Nevertheless, a number of system makers have signed on to use the 860. Mercury Computer Systems Inc., a manufacturer of application accelerator boards in Lowell, Mass., is one of them. Stratus Computer Inc., a Marlboro, Mass., manufacturer of fault-tolerant computers, is another. Mercury's first products, using the 33-MHz version, are scheduled for introduction in the fourth quarter of this year, with volume shipments to begin in early 1990. Stratus is actually switching from another RISC chip, the Motorola 88000, to the Intel 860 as its central processor for a future product family to be introduced in the early 1990s.

RISC IS GAINING ON CISC



Reports of the death of CISC are exaggerated, but if current trends continue, the future belongs to RISC

The 88000 from Motorola, based in Austin, Texas, is not as highly integrated as Intel's chip. The 88000 actually consists of two chips, one holding the integer and floating-point units and the second carrying the memory management, cache memory, and cache logic. On the other hand, it's been around longer and hence has been designed into more systems—depending on production volumes, some 20 companies are planning 88000-based systems.

Chief among them is Data General Corp. in Westboro, Mass. The chips are being used in a 20-MHz single-processor version and a 40-MHz dual-processor version of Data General's machines.

The 88000 uses an instruction set slightly larger than the Intel 860's, but is still quite small at only 51 commands, none larger than 32 bits wide. It can execute in less than 1.5 instructions per cycle, using an architecture divided into independent execution units: the data unit, the instruction unit, the floating-point adder, and the floating-point multiplier. Each unit has its own pipeline and can execute concurrently. The companion chip provides memory-management logic, 16 Kbytes of fast-cache static RAM, and cache-control logic.

The first version of the chip set is now entering volume production. It can run at 14 to 17 mips of throughput using a 20-MHz clock. This month, Motorola will start offering samples of a 25-MHz version that will push performance up to 20 mips or more.

A number of architectural variations are also being considered. One obvious one is an integrated version, putting the processing units and the memory functions on one chip. Another is a less expensive version, without the floating-point processor, targeted at embedded processor applications (see p. 74). Yet another would be specialized application-specific variations with instruction-set extensions. Also being considered are architectural variations that incorporate expanded data, address, and instruction buses to push the execution rate faster, to under one clock cycle per instruction.

In cooperation with Data General, Motorola is also working on a multichip, bipolar emitter-coupled-logic version of the 88000. Scheduled for completion in early 1990, the new chip set would be blindingly fast: a sustained data rate of 100 mips and a peak rate of at least 140 mips.

Even higher performance will result from the ECL variant of the 80486 that will be jointly developed for a multiprocessor system by Intel and Prime Computer Inc. of Natick, Mass. However, the companies do not anticipate releasing a product for another three years.

Both Intel and Motorola, in short, are fielding impressive implementations of CRISP and RISC. It's a good thing they did so. The two companies may well have gotten aboard the RISC bandwagon just in time. The first generation of RISC chips is giving way to newer, more powerful processors. At the same time, the chip makers are looking beyond simply implementing a particular architecture and toward advances, especially in software, that will carry them to the next level of performance.

In the RISC world now, it's no longer enough to choose an architecture and try to wring as much performance as possible from it. As a practical matter, it's fair to say that each high-end microprocessor has some strengths and weaknesses, from the Intel 860 to Sun's Sparc. "We have taken a step beyond architecture now," says Brian Halla, vice president of the microprocessor products group at LSI Logic Inc. in San Jose, a maker of Sparc chips. "Other issues are more important, especially software support."

Most RISC architectures fall into one of two competing camps. One is based on work done at the University of California at Berkeley, the other on research done at Stanford University. The basic architectural feature of the Berkeley approach is the use of a large number of windowed registers.

The Stanford approach uses fewer registers; the compiler optimizes execution by putting instructions into a pipeline.

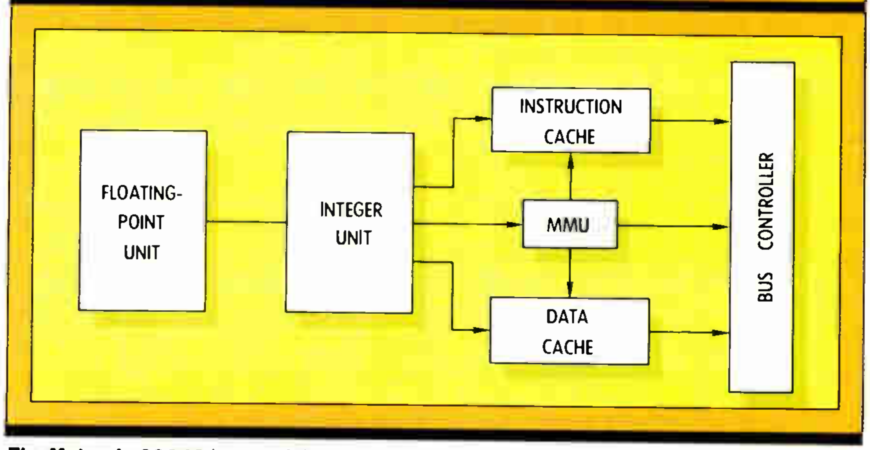
The leading implementation of the Berkeley approach is probably the Sparc processor, which Sun is working vigorously to establish as a standard. Sparc is a RISC architecture that emphasizes simplicity, so that it can be quickly implemented in the emerging high-performance semiconductor process technologies. Sun has licensed five semiconductor vendors to produce Sparc processor implementations. Besides LSI Logic, they are Bipolar Integrated Technology, Cypress Semiconductor, Fujitsu Microelectronics, and Texas Instruments.

Sparc makes use of traditional RISC principles, such as single-cycle execution for a majority of instructions. Separate 32-bit buses are used for data and addresses. A large, windowed register file with three ports stores and accesses frequently used variables. There are 120 thirty-two-bit registers organized into seven register windows in the initial implementation.

An advantage of the basic Sparc RISC integer processor is that it can be implemented in as few as 50,000 transistors. This makes possible the broad scalability touted for the design, since it is relatively easy to put 50,000 transistors on a chip using most of the emerging process technologies.

In fact, at the time Sparc was introduced, the only standard definition was the instruction-set architecture for the in-

HOW MOTOROLA'S 68040 IS PUT TOGETHER



The Motorola 68040 is one of the so-called CRISP chips—a combination of RISC and CISC that takes advantage of new process technology and circuit design.

IT'S NOT JUST COMPUTERS—EMBEDDED CONTROLLERS ARE HOT, TOO

Not all the 32-bit microprocessor action is in the work-station and personal-computer arenas—there's plenty going on in the embedded-processor market, too. The number of players is smaller, but the competition is no less intense. The reason: a rollicking market. "Over the next four years, we estimate that the number of RISC chip sets sold into the embedded market will increase almost 20 times," says John Peskuric, marketing manager for the Am29000 reduced-instruction-set processor at Advanced Micro Devices Inc. in Austin, Texas. Embedded processors will constitute about half of the RISC chip-set market this year—about 195,000 units. By 1992, they will make up 75%, Peskuric says.

Up until a year ago, a handful of companies had the high end of this field to themselves. Motorola Inc.'s general-purpose, complex-instruction-set devices, the 68000, 68010, and 68020, were widely used as embedded processors in the absence of any other more application-specific solution. Also weighing in were Intel, with its 80186; VLSI Technology, with its VL86C010 Acorn; and National Semiconductor, with a version of its 32-bit NS32000 family.

But all that changed when Intel Corp. introduced new 32-bit embedded processors last year. They were the 16-MHz 8096KA, running 7 million instructions per second, and the 25-MHz 80860KB, ranked at 12 mips. Then AMD moved into the market with its Am29000, and other companies followed.

Now AMD is pushing to increase performance in its 29000 family. With 16-, 20-, and 25-MHz CMOS parts in production, the company has just started offering samples of a 30-MHz, 20-mips version, and work is under way on a 40-to-45-MHz device offering throughput up to 35 mips. AMD will get the performance boost through process enhancements and architecture improvements.

Meanwhile, National Semiconductor Corp. in Santa Clara, Calif., has undertaken a major shift in strategy by refocusing its 3200 architecture for embedded processing rather than work stations. Its family of 32-bit CPUs will become the core of a series of customized processors, with special instructions augmenting the existing general-purpose commands. The first effort in this direction was the 10-MHz 32CG16 [*Electronics*, March 17, 1988, p. 66], which was followed last month by the 20-MHz 32GX32.

At the low end of the embedded-processor market is VLSI Technology Inc., which is one of two companies—the other is Intergraph—in volume production (about 40,000 chip sets since 1986). The four-chip Acorn RISC chip set consists of the 12-MHz, 6-to-8-mips VL86C10 CPU and three peripheral chips for memory, video, and input/output. Over the past year, VTI has converted the chip set into megacells, which have been added to its semicustom cell library. The plan is to develop a range of application-specific RISC-based embedded controllers says James Farrell, technical communications manager at VTI's logic products division in Tempe, Ariz. The first step in that diteger processor. No standard definition for an MMU, cache controller, cache scheme, or floating-point unit was available. And the only implementation was a gate-array version, from Fujitsu Microelectronics Inc. in San Jose of the integer processor and a floating-point controller chip for Weitek floating-point units. The MMU, cache control and configuration, and floating-point computational units were left up to the customers and the chip vendors.

A movement is afoot now to standardize some Sparc reference architecture definitions for these features. For example, a new implementation from Cypress Semiconductor Corp. in San Jose provides a complete architecture including the integer processor, floating-point unit, memory management, and cache, and sets up support for multiprocessing.

The multiprocessing support includes a direct-data-intervention multiprocessing protocol for maintaining cache consistency. The chip's memory-management unit conforms to the Sparc reference MMU architecture. Other reference specifications adopted include one for the module bus. In addition, Cypress is circulating the specs for its cache-consistency protocol among the members of Sparc International with the suggestion that it become a Sparc reference standard available to all Sparc licensees.

The Cypress chips—the 7C600 family—are being built using a 0.8-μm CMOS process technology, which the company

There's a Catch-22 in software: developers wait until a platform has users, users wait until there's lots of software

claims is the most advanced CMOS in production. With this process, Cypress can produce highly integrated processor chip sets running at 33 to 50 MHz.

So far, the integer unit is rated at 25 and 33 MHz in different versions. Currently, floating-point support requires a CY7C608 floating-point controller and CY7C609 floating-point unit. But this quarter Cypress will have samples of an integrated 64-bit floating-point engine, the CY7C602, that completely implements the Sparc floating-point instruction set. The CY7C602 will be offered in 25- and 33-MHz versions delivering over 5 million double-precision Linpak floating-point operations per second.

To round out the set, Cypress is building an integrated cache controller and MMU chip in two flavors. The CY7C604 is a complete implementation of the Sparc reference MMU architecture. This chip will make Sparc the first RISC architecture to support real-time processing—it will have the capability of locking entries in the on-chip translation lookaside buffer and entries in the cache's RAM.

The second flavor is the CY7C605, which is a superset of the CY7C604 CMU that supports multiprocessing with a dual-cache-tag architecture, plus a cache model that allows each processor to access each cache directly while maintaining coherency among them. The CY7C604 will be available in sample quantities this quarter at 20, 24, and 33 MHZ; samples of the CY7C605 will be available in the third quarter at 25 and 33 MHz.

Fujitsu, the makers of the first Sparc chip, now has its second-generation implementation in production. The 25-MHz S-25 integer chip, implemented with the Fujitsu 1.2-μm CMOS process, can achieve sustained performance of 15 mips. Fujitsu also makes floating-point controller chips to go with the Sparc integer processors. It expects to ship in volume in a couple of months.

A third generation of Sparc architecture, Sparc-H, has been in the works for the past year at Fujitsu's Advanced Products Division. Samples should be available in the second half of this year. "Sparc-H is the next level of price/performance beyond the Cypress implementation," says Susan Mason, Fujitsu's marketing development manager. Sparc-H

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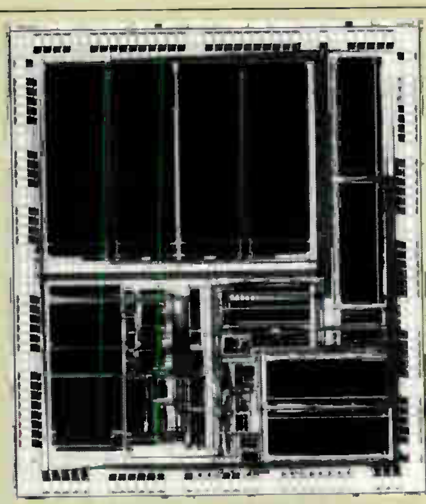
rection was the introduction in late April of sample quantities of a 32-bit RISC processor, the 20-MHz, 16-mips VL86C020.

Meanwhile, Motorola has announced that toward the end of the year it will begin offering samples of the MC68332, a high-end, 16-MHz embedded processor/controller built around a 68000/68020 core. Motorola's basic strategy is to offer an upgrade path to users of both the 8-bit 68HC05 and the 16-bit 68HC11 microcontrollers and to designers of 68000-based embedded-processing applications, says Brian Wilke, advanced MCU operations manager for Motorola.

Containing all of the 68000/68010 instructions and some of those from the 68020, the CPU core, with a two-clock bus, has a respectable 8-mips peak performance at 16 MHz. That gives it 65% to 80% of the performance of the 68020. A 16-by-16 multiply takes 1.5 μs and a 32-by-16 divide takes 1.9 to 2.5 μs.

Coming later this year from Intel in Santa Clara, Calif., is the second generation of application-specific 80860 proces-



VLSI Technology's VL86C010 is the core of a set of application-specific controllers.

sors. The first device will be built around a core CPU with throughput rates up to 66 mips with only a 33-MHz clock. Fabricated in the company's 1.0-μm CMOS process, the core gets its high performance by its ability to execute up to three instructions in a single clock in most cases, and up to two instructions per clock doing time-consuming loads and branches.

The next-generation 960 core will have seven basic units: the instruction sequencer, execution unit, address generation and multiply-divide units, the local register cache, register file, and instruction cache. It will contain a three-stage pipeline for the basic ALU; a three-, four-, or five-stage pipeline for loads; and a two stage-pipeline for branches.

Although the performance of the various application-specific 860 processors depends on the environment, the company says, the core element itself has been tested using a number of benchmarks. Assuming zero wait state external memory, 33-MHz operation, and no data cache, the 860 core runs a matrix multiply at 66 mips, a copy operation at 45 to 60 mips, and a compare operation at 66 mips—speeds more than 10 times greater than the previous generation of Intel controllers. *– Bernard C. Cole* will have a Harvard architecture—separate instruction and data buses—64-bit buses, an integer unit able to execute more than one instruction per cycle, and a faster floating-point unit in better balance with the integer unit.

LSI Logic is busy making both Fujitsu-compatible and Cypress-compatible Sparc integer units, using its 1.0-μm CMOS process. LSI Logic is also working on a chip that is a combination of a Sparc MMU, cache controller, and cache-tag memory, for introduction in the fourth quarter. By the end of the year, it will be offering a three-chip Sparc set consisting of the Cypress-compatible integer unit, the MCP, and a floating-point unit.

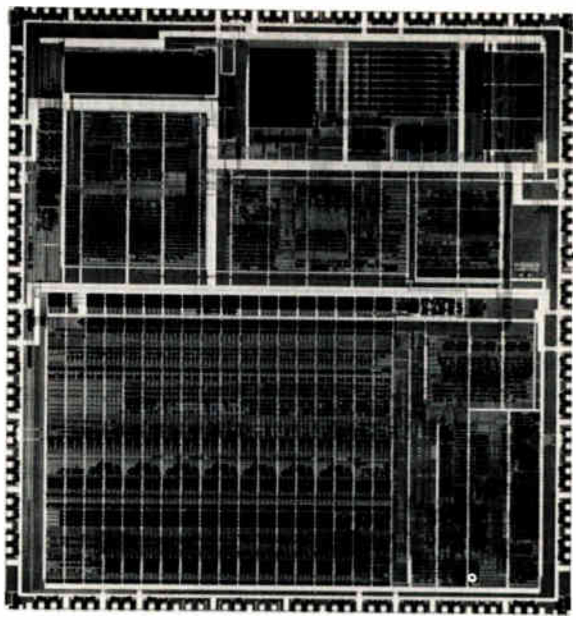
Meanwhile, Bipolar Integrated Technology Inc. in Beaverton is trying to get its high-speed ECL version of the Sparc integer processor ready to go to market. BIT will be using its high-density, low-power BIT P111 bipolar process to produce the Sparc chips. The key to BIT's bipolar VLSI is the small transistor size—$14\mu m^2$—produced by a self-aligned, triple-implanted structure. Yields and density of this process are as high as CMOS.

The range of Sparc implementations would make it a popular choice as a RISC processor regardless of whether it had anything else to recommend it. But what makes Sparc a leading contender for the role of a de facto standard is the wealth of application software available to run on Sparc chips. The Sparc instruction-set architecture is source-code compatible with the Sun work stations that are based on the Motorola 680X0 CISC processors. Such compatibility makes it easy to quickly port the many applications already written for Sun hardware.

Also helpful is system and development software, which is available from Phoenix Technologies Ltd. and Interactive Systems Corp.; both are licensed to resell Sun's complete offering of Sparc systems software. The combination of compatibility and system-software availability has produced, at last count, more than 500 application packages that run on the Sparc architecture.

More important, a standard application binary interface is being developed by Sparc International and AT&T Co. for the Sparc architecture and AT&T's Unix System V, release 4. A compatible binary code interface allows shrink-wrap binary application software to be produced for a broad offering of system products from a variety of vendors. (Sparc International was set up two months ago by the five Sparc chip makers to take over development of a Sparc application binary interface with AT&T, after Sun bowed out as AT&T's partner.)

Despite its formidable strengths, Sparc is by no means alone in the RISC field. Among its rivals, one of the strongest is the architecture developed by MIPS Computer Systems Inc. in Sunnyvale, Calif.



The newest member of the oldest commercially available family of RISC chips is Intergraph's C311 version of the Clipper.

The MIPS architecture derives from the Stanford approach to RISC. Both the latest version, the R3000, and the earlier R2000 were designed as full-custom VLSI implementations by MIPS's own design team. The R3000, introduced in early 1988, represents an advance over the R2000 in several respects. It has a faster clock rate, 25 MHz versus 16 MHz; cache enhancements; and better support for multiprocessing. Those specs make the R3000 probably the fastest RISC processor on the market today.

Each processor consists of a CPU with an integrated MMU and floating-point unit. As with Sun's Sparc, the chips themselves are fabricated by five semiconductor companies. MIPS specifies the chip architecture and implementation and provides the design to the chip makers (some of which also make Sparc chips). But the Sparc group of chip vendors offers a variety of chip sets, partitioning the architecture in a number of different ways, while the processors from the MIPS chip vendors are all plug-compatible, regardless of which of the semiconductor companies actually makes the chip. The chip makers can define extensions and alternate form factors in addition to the basic-set building blocks.

Also like Sparc, the MIPS architecture follows the Harvard model, with separate data and address buses. The cache scheme is a physical cache rather than a virtual cache, which helps in implementing multiprocessor systems. It has 32 general-purpose registers in the CPU, plus sixteen 64-bit floating-point registers in the floating-point unit. The optimizing software performs the register allocation for fast context switching.

The five MIPS chip makers bring various strengths in process technology to bear. LSI Logic offers high-quality capability in application-specific integrated circuits, using its powerful 1.0-μm CMOS process. LSI Logic also has a fast biCMOS process for its ASIC technology. Both Integrated Device Technology Inc. in Santa Clara and Performance Semiconductor in Sunnyvale offer state-of-the-art static-RAM technology.

In addition, IDT plans to use its CEMOS III process, which is a 1.2-μm CMOS technique, to produce a 33-MHz version sometime this year. IDT then plans to switch to its 1.0-μm CEMOS V process, which it is using now to build memories. This will increase the yield and availability of 33-MHz parts.

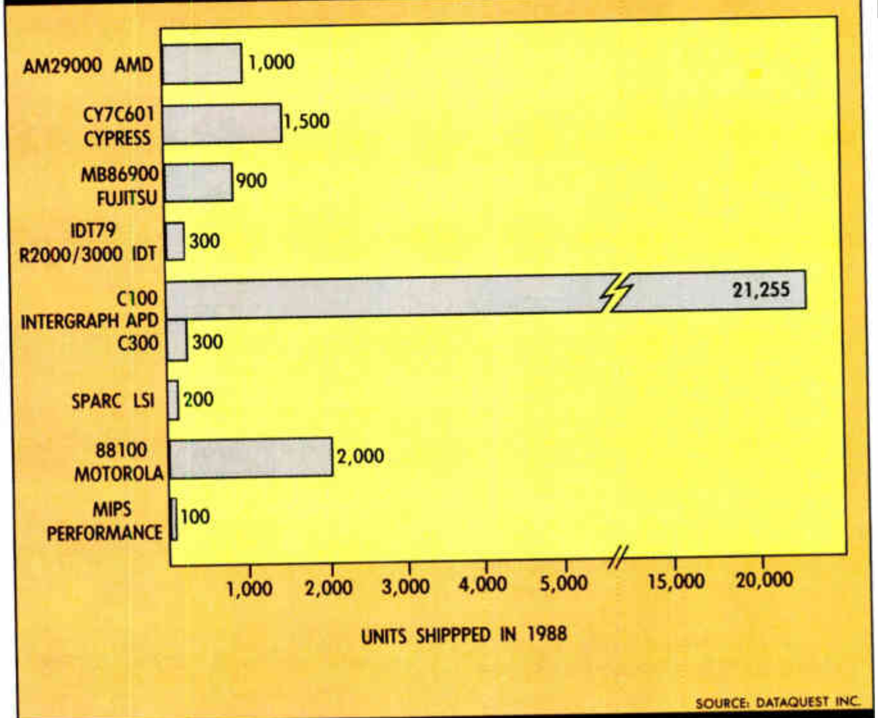
SAMPLES COMING. "Some evaluation units of the 33-MHz chips will be available in 1989—they will be very limited in the summer, restricted availability in the fourth quarter—and they will be generally available in early 1990," says Larry Jordan, IDT's vice president of marketing. As part of its CEMOS V process, IDT has a superset process to add bipolar modules; it may use the biCEMOS process on a 40-MHz R3000 in the first half of 1990.

The two newest members of the MIPS semiconductor team, NEC Corp. in Tokyo and Siemens AG in Munich, are not delivering chips yet. NEC plans to deliver its first CMOS implementation in the third quarter and Siemens is expected to follow in the fourth quarter. Both companies are expected to use MIPS chips in some of their own systems as well.

In software, the MIPS architecture is supported currently by the RISC/os operating system, a combination of AT&T's System V.3 Unix and the Berkeley Unix. "One of the particularly strong areas of software support is the MIPS compiler support," says Halla of LSI Logic. MIPS has invested many man-years in its optimizing compiler and run-time executive, and in return is getting very high performance from its processors. "MIPS has a large lead in compiler and run-time Executive," Halla says.

To provide a source for MIPS-compati-

WHO'S IN FRONT: 32-BIT RISC CHIP SHIPMENTS



ble applications software, an independent company, Synthesis Software Solutions Inc. of Sunnyvale, was set up by MIPS a year ago to be a software services and development organization to all companies building computers out of the MIPS chip set. "Synthesis does its job two ways: by contracting to license or relicense products developed by others and, over time—within the next year—developing its own tools," says Owen Brown, the company's president and chief executive officer. Synthesis is concentrating on horizontal packages—tools and tool sets, such as compilers along with tools for optimization and porting.

The Synthesis software catalog, issued last January, contains 24 software packages distributed by Synthesis and references 48 packages distributed by other companies. Data-base systems are the dominant type of software currently available. The second most popular category is languages. Synthesis plans to expand in the next two years beyond the data-base emphasis with communications and interoperability tools and more languages, according to Brown.

POPULAR. MIPS's approach is proving commercially attractive—industry experts say 30 to 35 major computer companies are building systems around it or plan to in the immediate future. Vendors with systems on the market include Silicon Graphics Inc. of Mountain View, Calif., the leading supplier of high-performance, three-dimensional-graphics work stations, and Ardent Computer Corp., Sunnyvale, Calif., with its Titan supercomputer work station.

The biggest and best-known company to sign up with MIPS did so early this year: Digital Equipment Corp. in Maynard, Mass., introduced a series of high-end work stations based on the MIPS processors [*Electronics*, February 1989, p. 49]. Another big name, Sony Corp., has announced that it will use MIPS processors for future Sony NeWs work stations. And MIPS itself has gotten into the systems business with a line of desktop work stations.

The Sparc and MIPS architectures both are technological leaders and strong market contenders, but the market leader is the first commercially available RISC processor, the Clipper, from Intergraph Corp. in Huntsville, Ala. Intergraph, a work-station vendor, bought the Clipper technology from Fairchild Semiconductor Corp. in Cupertino, Calif., when Fairchild was acquired by National Semiconductor Corp. of Santa Clara; National already had its own RISC offering, the 3200 family. Some 20,000 Clipper chip sets have been sold.

The Clipper series—there are two products, the C100 and the newer C300—is similar in architecture to Motorola's 88000. The two processors have in common their ancestry and architectural philosophy, but diverge on the details of hardware implementation and instruction-set makeup. Unlike the MIPS architecture with its roots at Stanford and the Sparc architecture with its Berkeley origin, the Intergraph and Motorola implementations can trace their genesis to the supercomputer designs of Seymour Cray, founder of Cray Research Inc., the supercomputer market leader.

Both use register scoreboarding to allow multiple instructions to execute concurrently with a guarantee that "stale" data will never be used. Both architectures are oriented toward multiprocessing applications and therefore are partitioned similarly, with the integer and floating-point units on one chip and the cache memory and logic integrated on another chip. In both cases, a minimum three-chip set is required: the CPU and separate cache/memory-management chips for instruction and data. All data transfers to and from main memory are done via an external multimaster bus that allows multiple chip sets to share main memory.

Internally, the CPUs reflect a similar philosophy with multiple execution units that operate concurrently. Both are pipelined, with three stages for the Clipper and four for the 88000.

One major advantage OEMs see in the Clipper family compared with other RISC machines, including the 88000, is availability, not just in sample quantities, but in volume production. Where the Clipper departs from the 88000 is not in its technology but in its longevity in the market.

"When we started development on our product, we looked at everything that had been announced," says one Clipper user, Dale Petros, a software engineer at Lennane Advanced Devices Inc. in Sacramento, Calif. "We found that the only real RISC machine around that was in volume production and that we could reliably depend on for parts in the quantities we needed was Intergraph's."

Similar concerns were what brought Intergraph one of its most important customers to date: E. I. Du Pont de Nemours and Co., based in Wilmington, Del. The deal allows for volume purchases of 50,000 units or more per year, which will

The Sparc and MIPS architectures are both strong contenders, but in the RISC market, the leader is still the Clipper go into products targeted at instrumentation, fingerprint recognition, optical character recognition, industrial real-time control, and flight simulation. "When we began our design, it was the only chip set around in volume production and with a well-defined upgrade path and a timetable for new versions," says Kevin Cook, the division's imaging-product manager.

The upgrade path through the various levels of Clipper is indeed the best-defined in the RISC business. Intergraph's strategy is to offer a range of chip- and system-level products that starts with low-end work stations, where cost is as important as performance, and goes up to very high-end work stations and mainframe computer nodes.

CLIPPER RANGE. At the low end is the C100 Clipper, in two versions. One is a 25-MHz, 6-mips chip set; the second a 33-MHz, 8-mips set. Both are fabricated in a 2.0-μm CMOS process. Intergraph has just cut the C100 price by between 30% and 40%. In the midrange is the C300 chip set, a 40- to 50-MHz implementation fabricated using a 1.5-μm CMOS process. Capable of throughput up to 14 mips, this second-generation chip set is just now going into volume production.

For the high end, Intergraph will offer the C311, a chip set fabricated in the same process as the C300 but capable of 50-MHz, 20-mips performance. It will use a 128-bit-wide demultiplexed system bus that interfaces to large discrete cache memories along with a discrete memory-management unit, as opposed to the integrated cache and MMU of the earlier implementations. That version of the C311 is available now in sample form. Intergraph is also working with its foundry, Fujitsu, on a bipolar ECL version capable of clock rates up to 100 MHz and throughput of up to 80 mips.

Under development is a new Clipper architecture that will be implemented in a 1.0-μm CMOS process incorporating such advanced features as wider address, data, and instruction buses; delayed branching, hardware scoreboarding, and more pipelining and parallelism. The CMOS implementation should reach 50 mips; an ECL version could hit 100 mips or more.

Despite its current advantages in the market, Intergraph takes a realistic view of the future. When competing RISC-chip makers ramp up production, its lead over them inevitably will narrow, says Gary Baum, the company's director of marketing. But Intergraph does expect to maintain its momentum, as several OEM customers go into production with Clipper-based systems.

The company is also broadening its marketing effort, by setting up a Clipper Products Division that will sell separately Intergraph's own Clipper-based work stations and software designed for them. Heretofore, the hardware and software were sold bundled into a turnkey system. The move in effect unbundles the Intergraph sales force, too, freeing them to market either hardware or software, and therefore puts on the market the all-important component of a successful RISC sales effort: applications software. About 180 application packages—ranging from computer-aided design and manufacturing software to office-automation applications—are ready now, and by the end of the year that number should reach more than 200. "This is at least four times the number of application-software packages available on any competitive RISC machine," says Du Pont's Cook.

In addition to the wealth of applications, Intergraph supports at the system level the Unix System V operating system, remote file sharing, and the Transmission Control Protocol/Internet Protocol and Network File System standards. Compilers are offered for C, Fortran, Pascal, Ada, and Lisp; new optimizations for the C, Fortran, and Pascal compilers have just been introduced that will provide up to 30% higher system performance. A second phase of the optimization program should boost performance another 20%.

To simplify software development, Intergraph has adopted the X Windows windowing interface and the Open Software Foundation's Motif as its basic application program interface. Adoption of the OSF/Motif, says Baum, will make available to Clipper users the many third-party applications that will be written to conform with the standard.

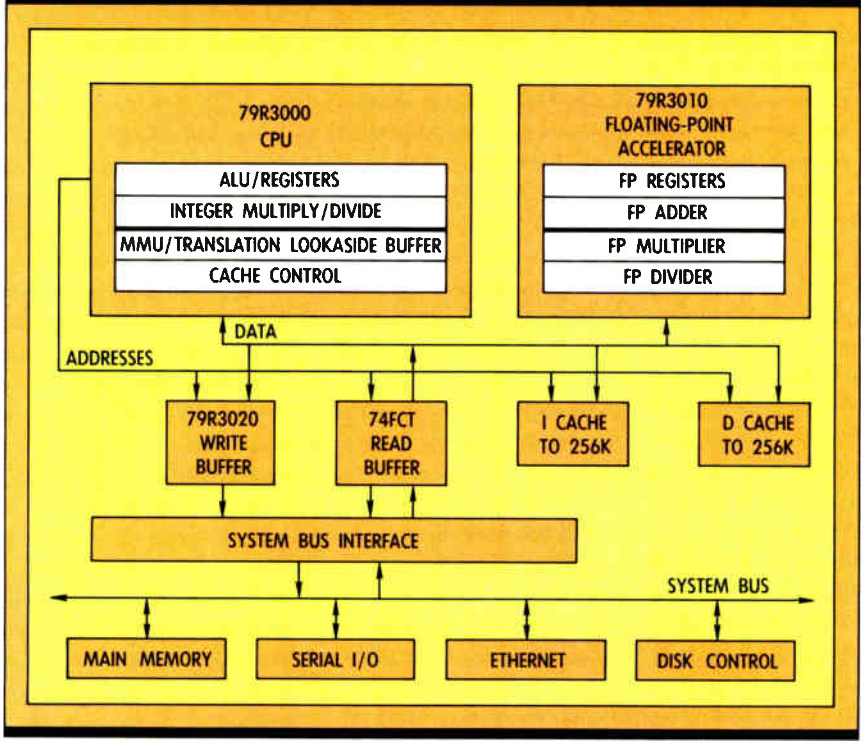
RISC WARS. If software is the ground over which the RISC wars will be fought and won, Intergraph and the Clipper should have enough artillery to more than hold their own. Their better-armed opponent, fittingly enough, may turn out to be Motorola and the Clipper's technological cousin, the 88000.

Motorola has developed a standard for binary compatibility that is essentially a subset of the AT&T Unix specification. Its backers say it is complete enough to allow a wide range of software developers to produce software that will work without modification on any system complying with the standard.

Promotion and refinement of the standard are now handled by the 88open Consortium Ltd., based in Wilsonville, Ore. The consortium is a nonprofit organization whose members include Motorola, software developers, and systems suppliers. It tests products for compliance with the standard and issues certificates of compliance. It also has devised the Software Initiative, an effort to promote the development of software for 88000-based systems.

Additional reporting by Bernard C. Cole and Tom Manuel

INTEGRATING THE CPU AND FPU ON THE R3000



The fastest RISC processor is probably the R3000 from MIPS Computer, a two-chip set with the CPU on one chip and the floating-point unit on another.

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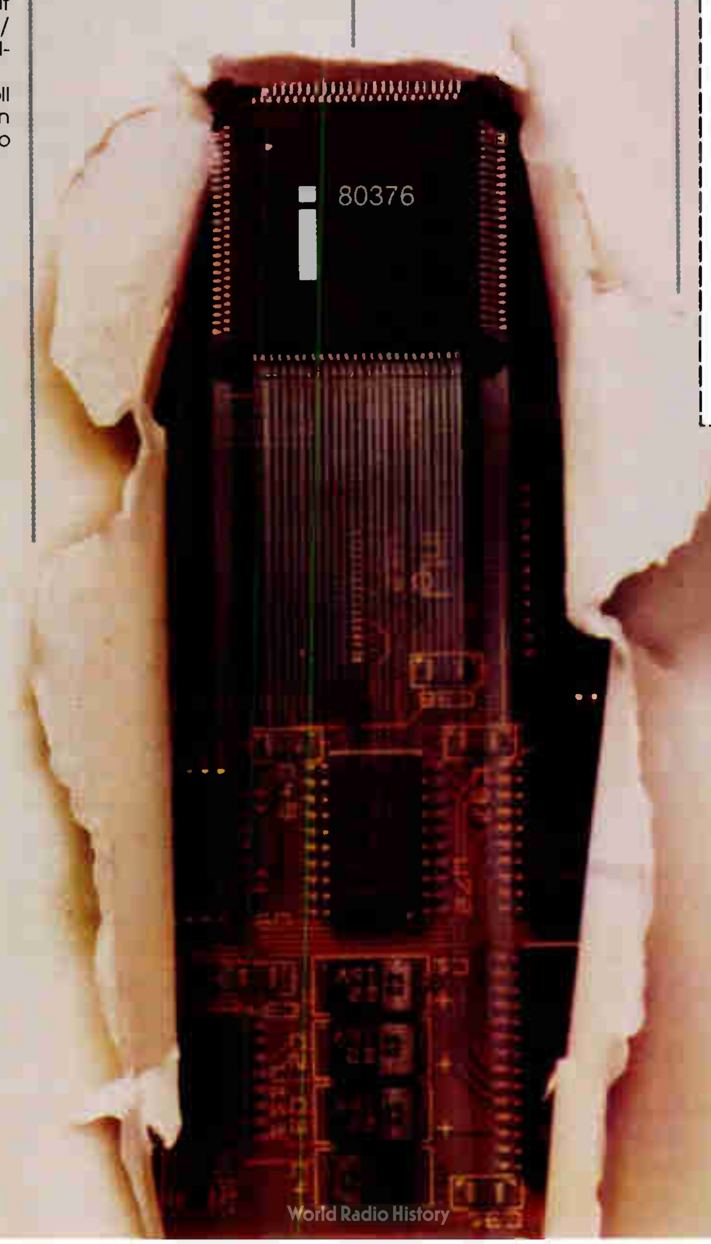

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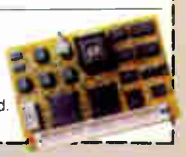

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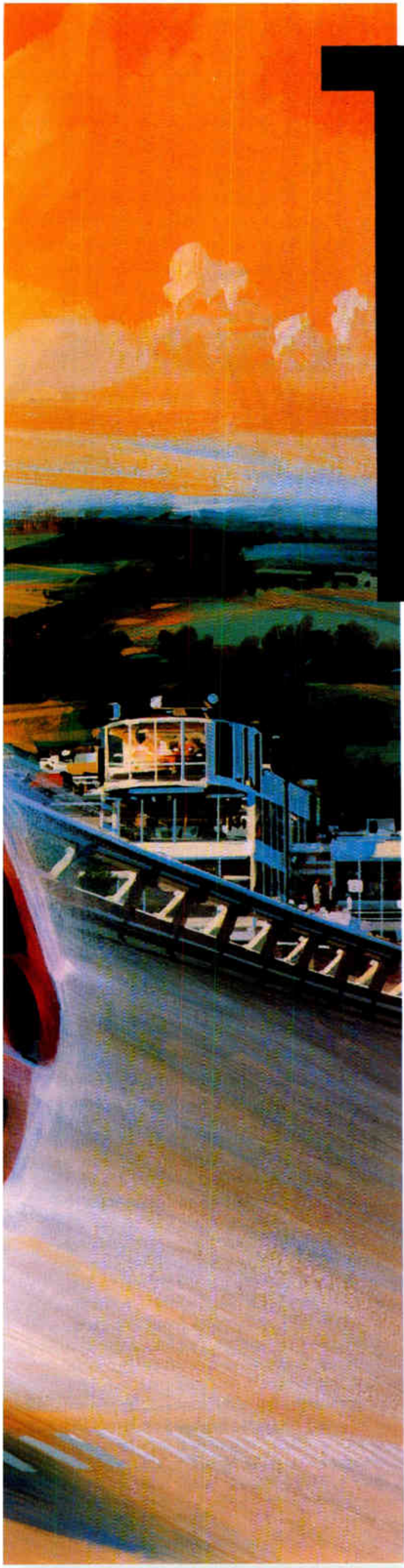
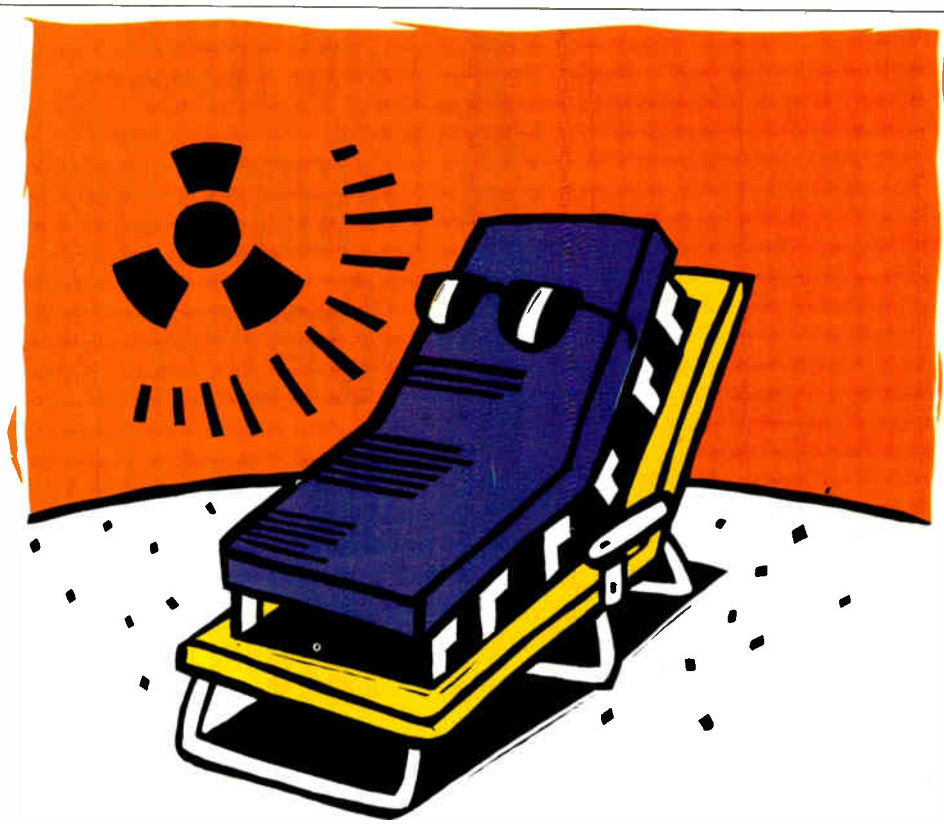




BY TOBIAS NAEGELE

HARD TIMES IN RAD-HARD

With a tightening defense budget, the Pentagon is looking for near-term solutions to making ICs that can withstand heavy doses of radiation. Critics fear some promising technologies may get lost in the shuffle

It's the oldest problem in military electronics: how do you make chips impervious to radiation damage? Companies have offered up a number of solutions over the years, ranging from exotic new semiconductor materials such as gallium arsenide and synthetic sapphire to careful design tricks that effectively isolate neighboring transistors from each other on a chip's surface. The Defense Department, the primary buyer of this hardened, or rad-hard, circuitry, has invested in all of them.

But today, with the Bush Administration actively backing a near-term implementation of Star Wars technology in the midst of a tightening budget environment, defense agencies are being forced to make tough decisions about which technologies have the most promise. "The suggestion I'm getting from the Strategic Defense Initiative is to put my emphasis on the near-term technologies," says one program manager, who manages funds from SDI, the Defense Nuclear Agency, and elsewhere for rad-hard chip research. As a result, some promising but unproven technologies are not getting the key investment they deserve, critics say. These are technologies that offer greater resistance to radiation than current processes, but need time to develop into viable methods for producing even modest volumes of chips.

These technologies—and the companies that back them—have to compete for funds at very early stages in their development, raising the risk level for SDI investments. "What we've got here in the government is just about the same problem you've got in industry—there are too many people who are only really interested in the short-term goals," says Dick Dudney, who as program manager for rad-hard silicon technologies at the Army Strategic Defense Command in Huntsville, Ala., will spend $28.7 million on rad-hard development work in 1989.

The biggest loser in this technology battle is GaAs. Even though no one questions the material's unparalleled ability to weather huge doses of radiation, SDI officials have shown impatience with industry's inability to boost circuit densities and drive yields up to respectable, silicon-like levels. Instead, they've shifted their attention to more mature silicon-based technologies.

SDI cut GaAs development funding from $35 million in 1987 to $16 million in 1988 and sought to cut it further, to just $14.7 million, this year. Only a last-minute $18 million reprieve from Congress last fall—in response to pleas from the Defense Advanced Research Projects Agency, which manages DOD's GaAs programs—kept alive any semblance of a viable program, says Sven Roosild, Darpa's assistant director for electronic sciences. Yet in a report to Congress in March listing the 22 "most critical" technologies to the future defense of the U. S., the Pentagon ranked GaAs development second only to microelectronics advances in general.

This mixed message has already irked some congressmen and may become a topic of debate when serious discussions of the fiscal 1990 budget get under way. That debate has already started, with Darpa firing the first salvo: Roosild says the $19 million SDI is seeking for GaAs research in 1990 "is not really enough to support a program that goes anywhere."

Why has GaAs lost its luster? The answer lies primarily in the more immediate success of two alternatives—bulk CMOS silicon and silicon-on-insulator, a variant of the older silicon-on-sapphire technology that is now the most common choice for critical rad-hard applications. Experts agree that GaAs will always be tougher than any silicon technology when it comes to "total-dose" radiation—the ability to survive a lifetime of repeated exposure. This can ultimately damage the material of a chip, slowing it down and otherwise degrading performance. But the difference in yield, cost, and, more important, circuit density, have made these alternative technologies more and more attractive.

GaAs also has an edge over most silicon technologies in terms of speed, but because of the huge weight concerns of space platforms, density is often a more critical consideration. So experts now expect GaAs to be used only in niche applications, where its unique combination of speed, power, and hardness are expressly called for. "The only place GaAs is better is total dose," says Barry Dunbridge, assistant general manager for technology at TRW Inc.'s Electronics and Technology Division in Redondo Beach, Calif. "Since it's no better with the other [criteria], it simply doesn't have anything to offer. You've got to ask: do you really need the speed for the higher cost?"

So for the short term, silicon in some form is the answer. That solution seems remarkable in light of the conventional wisdom of a decade ago, when silicon MOS technologies were considered "too soft" for space and missile applications, Dunbridge says. At that time, the military and the National Aeronautics and Space Administration leaned on conventional or dielectrically isolated bipolar technologies for their nuclear and space-based missions. But as the industry shifted away from n-channel MOS to CMOS while embracing smaller and smaller geometries, designers also had to move to thinner oxide layers on their chips. In so doing, they fell upon a happy accident: once oxides were cut in half, to about 250 Å or less, it turned out that "CMOS was good enough for peaceful space applications," Dunbridge says.

Total-dose hardness levels of 100 Krads and higher were easily attainable. Likewise, as operating speeds improved, CMOS became less susceptible to dose-rate attack, a sudden blast of radiation that can cause photon-induced currents to course through a chip, causing a spike effect that can upset memory bits and cause logic transitions. Halving the oxide thickness produces a factor-of-eight improvement in total-dose hardness and a four-times improvement in dose-rate protection, Dunbridge says.

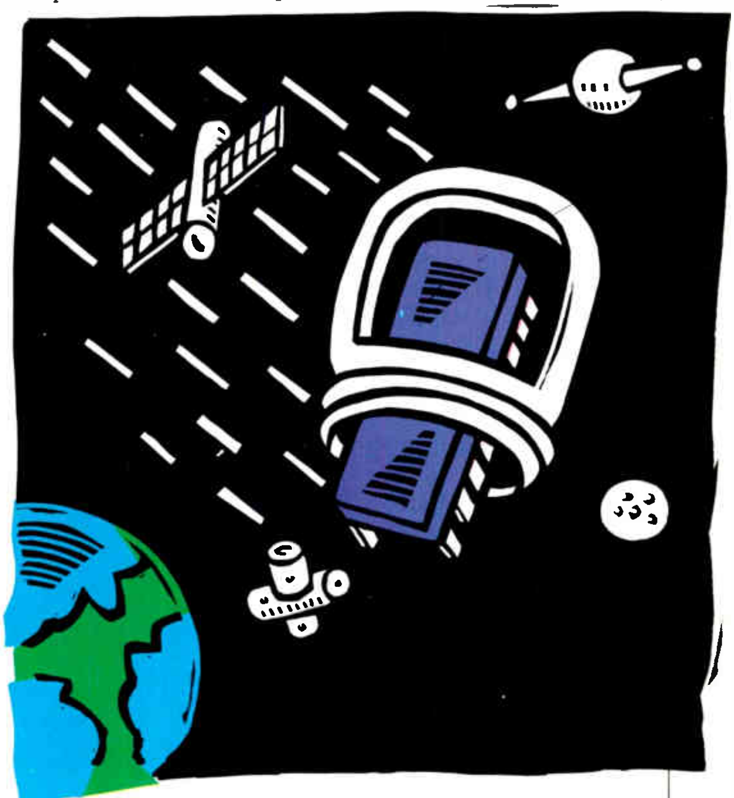
Later, chip developers realized that hardening CMOS further was a matter of insulating individual transistors from one another. They found that by building silicon circuitry on an insulating substrate of synthetic sapphire, or by somehow growing an insulating layer onto the silicon substrate itself, they could produce still harder circuits.

More recently, IBM Corp.'s Federal Systems Division in Manassas, Va., and Honeywell Inc.'s Solid State Electronics Division in Colorado Springs, Colo., have pushed straight CMOS as potential solutions to even the most stringent rad-hard problems. Using extensions of the processes they developed for the Pentagon's Very High Speed Integrated Circuit program, both companies have produced rad-hard CMOS 64-Kbit static random-access memories with SDI funding, using an isolation technique that essentially amounts to building a silicon wall and moat around each transistor. Their success has thrown the rest of the rad-hard world into a tizzy.

Unlike most rad-hard programs, which require only a modicum of memory and which off-load most if not all of the processing needs to ground-based systems, SDI satellites must be capable of instantaneously reacting to nuclear events around the globe. And their need to handle tremendous on-board computing tasks means they will require levels of memory capacity never before seen in space-based systems. "SDI birds are memory-hungry," says the Army's Dudney. "Little 4- and 16-Kbit memories aren't going to do it."

Hence the extensive investment in SRAMs in virtually every technology, from GaAs—where 16-Kbit SRAMs are now available—to silicon. Having successfully developed 64-Kbit silicon technology, IBM and Honeywell are now working on the 256-Kbit level. Other funding, from SDI and the DNA, has boosted development of a silicon-on-insulator 64-Kbit SRAM from Texas Instruments Inc. of Dallas and a silicon-on-sapphire 64-Kbit part from General Electric Co.'s Microelectronics Center in Research Triangle Park, N. C.

These new technologies are beginning to edge out the oldest, silicon bipolar, which is currently flying in more satellites than any other. Silicon bipolar was the first technology to reach a high enough maturity level to satisfy the historically cautious space community. But this process is today very limited in den-



Gallium arsenide is tougher than any silicon technology but is plagued by high cost, low yield, and low circuit density. The Pentagon has cut back GaAs funding by more than half sity—4-Kbit SRAMs are the biggest available memories. What's more, bipolar circuits are not very hard compared with ICs built in competing technologies. They can withstand a lifetime radiation dose of only about 100,000 rads, 10 to 100 times less than specially designed CMOS or SOI parts and 1,000 times less than GaAs. So while bipolar is still used in specialized applications, it is by no means the technology of choice today.

That title belongs to one of two silicon technologies: dielectrically isolated CMOS or silicon-on-sapphire, the process RCA Corp. developed in the 1960s and '70s for high-speed commercial applications and which owes its survival to its hardness characteristics. SOS incorporates CMOS circuits on top of an insulating substrate of synthetic sapphire, which acts as a ground for radiation-induced electrical currents. Dielectrically isolated silicon, on the other hand, protects its circuits from the effects of transient radiation by isolating each transistor within an individual "tub" of silicon, making it harder for electrical activity at one transistor to set off a chain reaction among its neighbors, says Joe Tirado, manager of strategic marketing for military and high-reliability circuits at Harris Corp.'s Semiconductor Sector in Melbourne, Fla., the undisputed world leader in rad-hard chip sales.

Each leading technology has its problems, however. In bulk silicon, designers pay a steep real-estate price for isolating every transistor from its neighbor. Honeywell's rad-hard CMOS 64-Kbit SRAM is almost four times the size of a comparable 160-by-300-mil 64-Kbit part TI is developing with SOI technology. And bulk silicon's performance is nothing to brag about: typical access time for a CMOS 64-Kbit SRAM is 40 ns or slower, against only 25 ns for SOI or SOS.

As Star Wars takes off, the pressure for rad-hard solutions intensifies; this SDI experiment was launched last year from a Delta 181 rocket

For SOS, the problems are all materials-related: synthetic sapphire substrates are expensive, brittle, and limited in size—the biggest wafers measure just 3 in. across. As a result of these three factors, chips are outrageously expensive and yields notoriously low. In fact, just getting sapphire substrates can be an ordeal. For most of the 1980s, U. S. companies depended on Japanese suppliers, until the Pentagon coughed up $21 million to establish a guaranteed domestic source at Union Carbide Corp. in San Diego. Under the agreement, Union Carbide will also try to develop larger sapphire wafers to help reduce the processing cost for SOS.

Also, some experts warn that SOS technology may have reached its fullest density potential with today's 1.25-μm design rules. "Sapphire material is very limited in integration density because of the stress between the silicon and sapphire layers," says a DNA official. By contrast, IBM has broken the 1.0-μm barrier with its bulk-silicon processes, working at 1.0 and 0.5 μm.

Even SOS's strongest supporters—companies like GE, Harris, and Rockwell—admit that SOS will bow out in favor of other solutions in coming years. "We know there's going to be a changeover one day," says Quent Cassen, director of IC engineering at Rockwell International's Microelectronics Technology center in Newport Beach, Calif. "But for now, SOS is the only silicon-based technology that has been proven in military systems."

The likely replacement: silicon-on-insu-

WHAT MAKES A CHIP RAD-HARD?

What makes one chip capable of withstanding high doses of radiation and others fail? The answer lies in a complex relationship between the characteristics of the semiconductor material and the circuit design itself. Even the average commercial-grade CMOS chip has some inherent immunity to radiation. In many cases, in fact, builders of military and space systems merely screen such chips through a careful series of tests, rather than go out and shop for—or commission the design of—specialized parts.

The French Spot-1 Remote Imaging Satellite, for example, makes its photographs of the Earth with an array of carefully screened, solid-state, charged-coupled-device cameras that were designed for use in facsimile machines by SGS-Thomson Microelectronics.

But screening is acceptable in only the mildest of radiation environments. For critical applications such as nuclear arms or the space-based Star Wars weapons, much higher tolerances are required. Hence the major funding for rad-hard technology development over the past five years. The Pentagon has spent well over $250 million on rad-hard research since 1984, and it plans to spend an additional $52 million in fiscal 1990—a figure its own experts insist is far too frugal.

Calculating how much rad-hard technology the military buys, however, is not so easy; accurate figures simply don't exist. Most estimates place the total at around 5% of the $3 billion military-chip market, or around $150 million a year.

What all that money is going for is a chip's ability to weather some combination of four radiation parameters: total dose, dose-rate upset, neutron radiation, and single-event upset. Total dose is defined as the maximum cumulative dose of radiation that a part can be expected to withstand and still continue to operate; dose-rate upset measures the maximum radiation a chip can survive over a given time frame; the neutron figure predicts the maximum level of neutron bombardment that can attack a chip's surface before it fails; and single-event upset measures a part's hardness against sudden bursts of gamma radiation, usually emitted by the sun.

Different applications will require different parameters, depending on the mission, its orbit and operable lifetime, and the levels of radiation it is expected to encounter in normal operation. *—T. N.*

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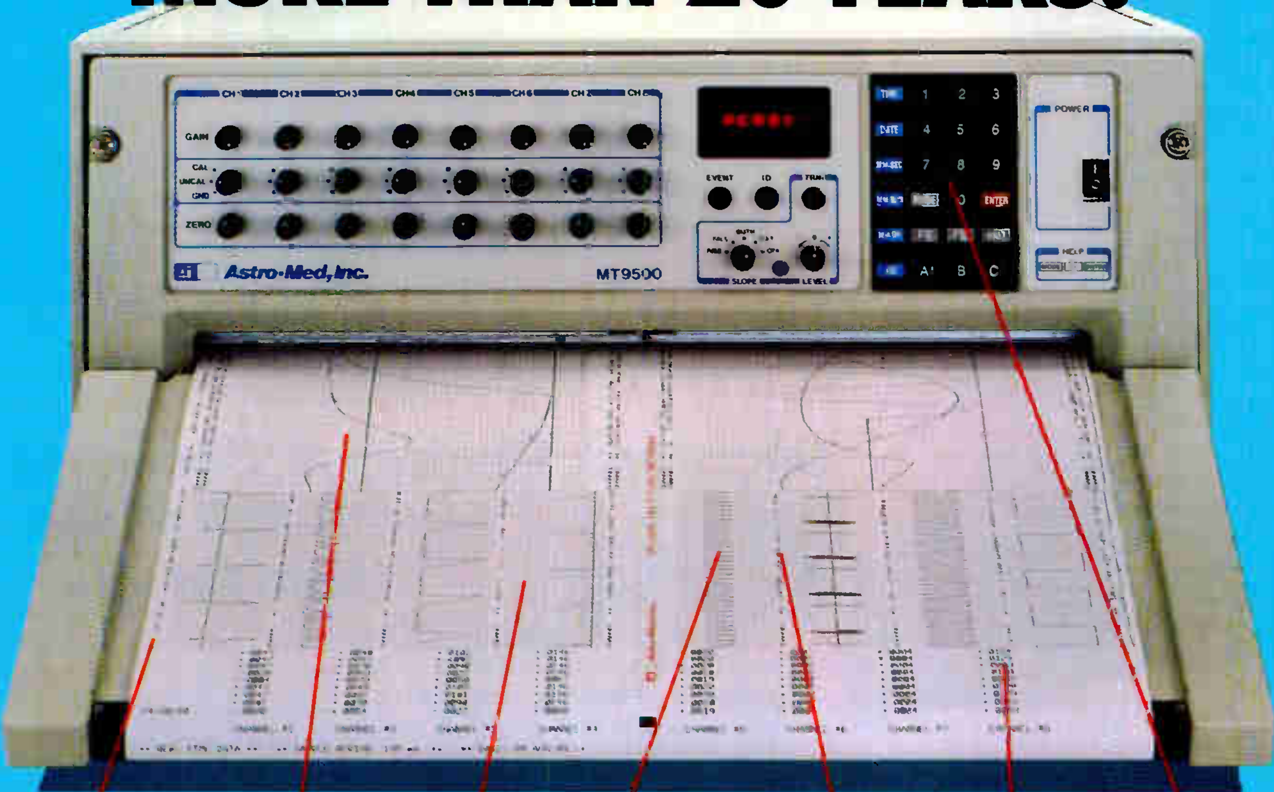

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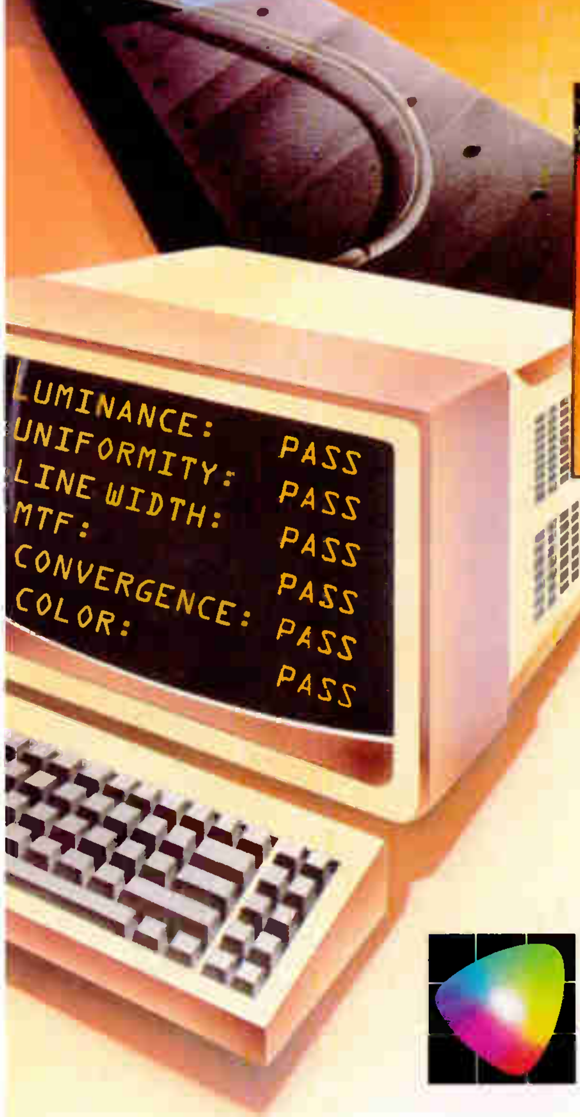

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THE NEXT GREAT HOPE: DIAMOND CHIPS

Silicon in all its varieties dominates today's market for radiation-hardened microcircuits, but scientists say the technology is ultimately too soft for the harshest radiation-packed environments. Their slogan: silicon lasts a while, but diamonds are forever.

Diamonds? Well, diamond semiconductors. If engineers can master the fine art of growing diamond substrates, diamond chips—not the kind that go into earrings, but working electronic circuits etched into diamond substrates—will be the preferred technology for all space and nuclear applications. No matter how advanced silicon or gallium arsenide technologies get, both materials will always be limited by inherent characteristics that, sooner or later, make them vulnerable to radiation damage. Not so diamonds.

"The higher hardness in diamond is going to run circles around everything else," says Dwight Duston, director of innovative science and technology at the Strategic Defense Initiative Organization, which has spent about $13 million in diamond research in the last four years.

Of all potential semiconductor materials, diamond has the highest breakdown voltage, the highest saturated electron velocity, the highest thermal conductivity, and the lowest dielectric constant. "Combine all those things and what you get is high power, high frequency, and rad-hard," says F. Thomas Wooten, vice president for electronics and systems at the Research Triangle Institute in Research Triangle Park, N. C., which has an ongoing diamond program funded in part by SDIO. "Diamond technology is stimulating a lot of interest."

What's more, diamond has mainstream potential in non-rad-hard markets. Any application where high frequency, high speed, and the ability to operate at high temperatures are needed is ripe for a diamond solution, say officials at SDIO, the Office of Naval Research, and several private laboratories that are working on diamond development.

The high-temperature operation is particularly attractive for satellite applications, since 65% of the average satellite is dedicated to thermal management, Duston says. Since diamond circuits could operate at upwards of 600°C—475°C higher than silicon or GaAs—much of that cooling equipment could be eliminated. That would give satellite designers the chance to greatly increase a bird's capability or to decrease its size, so that smaller, less expensive launch vehicles could be used. Immunity to heat would also permit the use of diamond chips inside aircraft engines or nuclear reactors to monitor performance.

But immunity to heat is only one facet of diamond's brilliance. Based on a formula developed in 1972 to derive "figures of merit" for large-scale integrated-circuit materials, diamond is at least 32.2 times superior to silicon, says Max Yoder, a program manager at the Office of Naval Research. Another formula developed for microwave and millimeter-wave ICs rates diamond 8,200 times better than silicon and nearly 1,200 times better than GaAs, the preferred MMIC technology.

"If we could build diamond semiconductors today, we could revolutionize the Mimic program," says Duston, referring to the Pentagon's five-year, $250 million effort to develop high-density MMICs.

And there's the rub: diamond semiconductors can't be built today. One researcher, Michael Geis at the Massachusetts Institute of Technology's Lincoln Labs in Lexington, Mass., has had some success in building circuits on natural diamond. But fabricating dense circuits in volume will remain nothing but a pipe dream until someone learns how to make usable diamond substrates.

Natural diamond is too expensive and stones are too small to be used for anything but research, so synthetic diamond is the key. The problem, says Duston, is that diamond "has a hard lattice constant to match."

So while it can be grown epitaxially with relative ease, finding a suitable substrate to grow it on has so far perplexed scientists. Without a good lattice match, growing anything more than an ultrathin diamond layer is impossible—the material will crack under the strain of the mismatched molecular structures.

There are materials that do match diamond's lattice, says James A. Hutchby, director of RTI's Center for Semiconductor Research. But none of these are capable of withstanding the 700-to-800°C temperatures that diamond must be grown at. The institute's latest hope: finding a copper-nickel alloy that can come close to matching diamond's lattice.

Meanwhile, researchers at Crystallume, a Menlo Park, Calif., company, are taking a different tack. They're trying to develop a lower-temperature process for growing diamond that might allow the use of lithium-fluoride and other materials that, while they match diamond's lattice closely, disintegrate at between 300 and 400°C. If they can grow diamond at a low enough temperature, they can use these substrates to get started and then burn them off at a later stage in the chip-making process, says SDIO's Duston.

Likewise, the Naval Research Laboratories are also interested in lower-temperature processing, says James Butler, an NRL researcher. "Right now, we sort of have a simple-minded view of why diamond can be grown by chemical vapor deposition," he says. "The next aspect of our research is to understand the surface chemistry of diamond so we can grow the material at lower temperatures." *–T. N.*

The key to producing diamond ICs is finding a substrate to match diamond's unusual lattice lator, which is, in fact, a superset of technologies that includes SOS. Harris, TI, and others have been making enormous strides in recent years toward creating an insulating substrate without the problems inherent to sapphire. The leading approach is TI's Simox process, in which the natural properties of bulk silicon are altered through a series of process steps so that the silicon becomes, at once, an active semiconductor layer and an insulating substrate.

The industry is placing its bets on SOI technology, and has made big strides in finding an insulating substrate without the problems of sapphire. The leading approach: Simox, from Texas Instruments

With Simox, TI literally embeds an insulating layer inside the silicon substrate. TI won't say just how high the yields are, but they're "at least double the yield of SOS, simply because we've got a better substrate," says Tom Powell, rad-hard branch manager for TI. Moreover, power dissipation at standby is "three orders of magnitude better than bulk" CMOS, he adds—about 100 nA to 1 μA vs. 0.5 to 1 mA.

But what is most remarkable about the TI technology is how fast it has matured. With the firm backing of the DNA, "they've brought that technology along much faster than anyone thought possible," says the Army's Dudney, who has overseen the work for DNA. "They've split the maturity gap between SOI and SOS from five to two and a half years." Now Dudney says he wants to narrow the gap further by funding submicron SOI work.

With all its promise, Simox has problems of its own. Ion-implantation equipment, needed to create the insulating layer within the substrate, is expensive. And since Simox is new, it will take time for it to gain the confidence of DOD program managers, the rank-and-file specifiers whose decisions will ultimately determine the winner of the rad-hard battle. The success or failure of a program under, say, a major's watch, can go a long way in determining if he ever makes colonel. And with that in mind, insiders say, few are likely to take a risk. "The program manager's got his career riding on these decisions," Dudney says.

That attitude has hurt GaAs especially, and was the reason that Congress eventually set aside extra money to fund a series of GaAs insertion efforts. And it is the kind of thinking that could untrack TI in its effort to get SOI parts into a variety of low-hardness programs. The company hopes that by reaching out to these lower levels it can boost orders, cut costs, and broaden its market. "Business projections for SDI are huge, but they keep getting pushed out and pushed out again," says TI's Powell. "We want to be a player in that market, but we also want to look at the lower-rad markets as well."

TI's strategy is rooted, at least in part, in the notion that Simox may be a viable commercial technology of the future. Unlike SOS, which will never make it in the commercial world thanks to its miserable yield, Simox may hold better promise than traditional CMOS for all circuits, once design rules descend to the 0.3 μm level and below.

That's because the insulating SiO_2 that makes Simox rad-hard could also make it immune to current leakage or crosstalk between neighboring transistors, a problem that's already leading IBM and Honeywell to consider dropping voltage levels to 3 rather than 5 V for their next-generation 0.5-μm 256-Kbit SRAMs. A source at the DNA goes even further: not only would Simox conceivably be able to operate at the standard 5 V, he says, but it might even become cost-competitive with conventional CMOS at that level, because the CMOS isolation problems would be that much harder to master. □

HOW THEY STACK UP: THE TOP FIVE RAD-HARD TECHNOLOGIES

Chip Technology	Key Companies	Biggest Available Static RAM (Kbits)	Typical Access Speed (ns)	Stage of Development	Total Dose (rads)	Dose Rate Upset (rads/s)	Neutron Radiation (neutrons/cm^2)	Single-Event Upset (errors/bit/day)
Silicon (Bipolar)	AMD, Harris, National, TI	4	10	Mature technology, but losing ground to lower-power MOS processes	10^5–10^7	10^8	10^{14}	10^{-5}
Silicon (bulk MOS)	Honeywell, IBM	64	40	Emerging as the technology of choice in most applications	10^6	10^9	10^{15}	10^{-7} to 10^{-8}
Silicon-on-Sapphire	GE, Harris, Hughes, Rockwell	64	25	Most mature of the silicon-on-insulator technologies, but believed limited in terms of much higher integration	10^5–10^6	10^{10}–10^{11}	10^{15}	10^{-9}
Silicon-on-Insulator	Harris, TI	64	25	Believed to be the rad-hard technology of the future, with potentially lower cost than SOS and higher integration than bulk silicon	10^5–10^6	10^{10}–10^{11}	10^{15}	10^{-9}
GaAs	Gigabit Logic, McDonnell-Douglas, Rockwell, TriQuint	16	5	Hardest technology against total-dose radiation, but very limited by integration level with the material. Ultimately a niche technology for microwave and millimeter-wave ICs	10^9–10^{10}	10^7	10^{15}	10^{-7} to 10^{-8}

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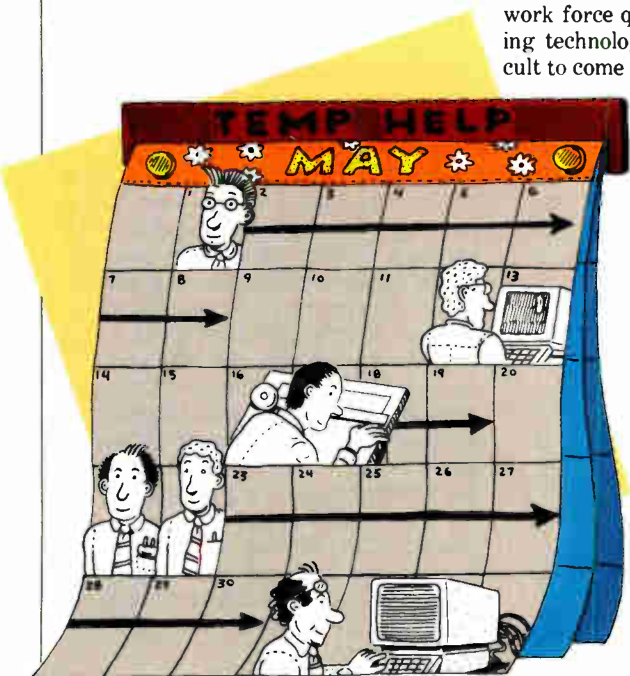
Circle 4

HERE COME THE TEMPS

BY LARRY WALLER

HIRE RATE IS SOARING

Electronics-industry managers are relying more heavily on contract engineers and third-party development houses as pressures on profit margins dictate keeping a leaner full-time staff



There's a valued new employee on the scene in the electronics industry these days, but you won't find his or her name on the regular payroll roster. The engineer, designer, or project manager in question is a "temp"—a highly skilled hired gun brought on for a particular project with a limited life span.

Though using temps is not a new concept, the hire rate has soared, spurred by heightened competition that puts a premium on a company's ability to change its work force quickly in response to changing technology. Hard statistics are difficult to come by, but some sources believe high-technology firms account for up to 25% of all salaries paid to temps in the U. S. today. Another index of the robustness of the trend is found in the temp-agency business itself, which has scored annual growth rates of more than 20% over the past 10 years running.

Hand-in-hand with the increasing reliance on outside help—whether individual contractors or those recruited through a high-tech temp agency—is the related phenomenon of third-party development houses. Such businesses, which in effect are subcontractors that handle a project from the design stage through pilot manufacturing, are flourishing. As an industry, they've skyrocketed from a mostly insignificant role a decade ago to be worth a combined $1 billion annually, according to estimates by business consultant Arthur D. Little Inc. of Cambridge, Mass.

A notably open-minded bunch, electronics-industry managers have long been hiring temps to smooth out workload peaks or to fill in for absent hands. As far back as the mid-1970s, they discovered that skillful weaving in of outside talent could give them an edge over the competition. In fact, the peaks and valleys associated with the semiconductor business cycle are tailor-made for temps. Motorola Inc.'s Semiconductor Products Sector, for one, has avoided the heavy layoffs that come with the down part of the cycle by depending more heavily on contract labor than its peers.

But today, competitive pressures on profit margins require keeping the leanest possible full-time staff and make finding quality temps more urgent. Technology talent usually comes through technical service agencies, which supply designers, engineers, and scientists as readily as Kelly Services agencies deliver office help. These "nonstandard types of staffing," as the Conference Board, a business-research organization, calls temps, may be referred to as alternative, contingent, or peripheral employees. Some talk about the trend as a "core-ring" concept, where a work force is divided into a core of full-time workers surrounded by an

WHO ARE THE TECHNICAL TEMPS? NOT YOUR 'AVERAGE JOES'

If you think the technical brain trust working as temporary or contract employees consists of engineers who are momentarily between jobs, think again. Executives in the temporary-service business say there's an abundant pool of technical talent, perhaps topping 150,000 people, that prefers to work freelance.

"Technical temporaries aren't just your average-Joe engineers," says Joseph B. Morris, executive director of the National Technical Services Association in Alexandria, Va. Most have advanced skills and in many cases are better qualified than anyone who could be hired on a permanent basis, he says. "They get up to speed immediately. This is definitely not a field for beginners."

Founded in 1966, NTSA has 84 member companies employing its temps as on-site contract engineers. The firms range in size from about $2 million to over $50 million in yearly sales. Morris estimates the temp-placement industry itself at about $3 billion annually, growing at a 12% to 15% rate.

John Ferguson prefers overseeing Tidewater's turnkey projects to corporate life.

Another type of temp is one who works for a product-development company, a firm that handles projects on a turnkey basis for larger corporations. One such engineer is John Ferguson, an engineering project leader for Tidewater Associates Inc. in Union City, Calif., one of the leading product-development outfits.

At any one time, Feguson may be directing several development programs for a number of companies. He is responsible for all facets of each job, which typically last six to nine months from concept to delivery of the prototype.

Ferguson has more than 10 years of experience in digital and computer-system design, including a stint with Hewlett-Packard Co., and holds BSEE and MSEE degrees from the University of California at Berkeley.

But the business side of his projects often claims more of his time than the technology. "Scheduling [of delivery] is generally the No. 1 interest of our customers," Ferguson says.

Ferguson believes that he is in the ideal spot, always supervising designs that test his mettle by pushing into the higher levels of technology. So he has no thought of going back to work directly for companies. "I get to work on something here from start to finish. It's a stimulating environment," he says. *–L. W.*

outer ring of part-timers, temps, or contract workers.

During flush times, companies can take on temps without committing to full-time salaries and the benefit packages that typically add some 40% and as much as 60% in "hidden costs" for each employee. Then, if business conditions hit the skids, as inexorably happens from time to time in the recurrent product and commodity cycles, companies can trim the temps first, sidestepping the need to fire permanent employees.

While the pluses are apparent, there are some negatives to consider, too. Topping the list is maintaining work quality, along with the closely related issue of insuring that temps are as energetically motivated as the full-timers.

Managers must also consider the possibility that federal regulation may be in the offing regarding the treatment of temporaries. Already, the Internal Revenue Service has gotten into the action with its Section 89 provision, which became official this year. Its intent is fairly clear, say sources at temp agencies: to broaden benefit coverage for temps. But just how the regulation will work in practice, and the liabilities associated with it, are still subject to interpretation.

"If corporate executives think using contingent workers is going to be a free lunch, they are going to be surprised," says labor economist Richard Belous of the National Planning Commission in Washington. Companies will have to make investments in training and in setting up workable structures to reach their quality-control and motivation goals for temps, he says.

Because of the sensitivity of the subject, along with reluctance about giving valuable information to competitors, most electronics companies decline to talk for the record about how they use temporary workers. And high-tech temp agencies are forbidden to identify their clients. Even Motorola, which in the past has been outgoing about its success in using temps, is now keeping mum.

A notable exception is Hewlett-Packard Co., which late last year unveiled a plan to build an in-house alternative labor pool. The strategy carries extra weight since the Palo Alto, Calif.-based HP has over the years earned a reputation as perhaps the most advanced and benevolent organization in the industry in terms of employee relations. Its no-fire policy—employees are hired for life, and not laid off due to hard times—is widely admired, if not emulated.

HP's new Flexible Work Force became official at the start of its fiscal year, Nov. 1, as a sort of internal temp agency, says Stephanie Decker, who runs the program. "We're trying to build in lots more flexibility for the company because there's so much more competition, and this is a way to respond to the changes," she says. Although HP will continue to hire temps from the outside, keeping an internal pool is a means toward tighter control of temps, Decker says. The Flex Force spans all parts of the company, but no manager can use it for more than 10% of his or her programs. After studying the interplay between temps and permanent employees, HP has set guidelines intended to get the advantages of flexibility "without changing the culture," she says.

The key to the program's success, says

WHY COMPANIES HIRE TEMPS

To Alleviate Work Overloads	70%
For Special Projects	61%
To Fill in for Workers on Leave	52%
To Fill in for Vacationing Workers	51%
To Fill Vacancies Left by Resignation or Firing	44%
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Base Salary	$200.00
Mandatory Payroll Taxes	25.20
Time Not Worked (vacation, holidays, sick days, paid breaks from work)	29.60
Hiring and Administrative Costs (training, bookkeeping, miscellaneous clerical work)	14.00
Company Benefits (pension, profit sharing, insurance, miscellaneous benefits)	51.40
TOTAL COST	$320.20

SOURCE: UNIFORCE

Decker, is choosing personnel "who truly want to be temporaries." Although salaries are comparable with those of full-time counterparts, the jobs carry no medical, pension, or other benefits, so the ideal hires are retirees, students, or part-timers who have coverage elsewhere. The bedrock requirement is that Force workers cannot use temp jobs as steppingstones to permanent slots at HP. "This is not a screening device" for full-time employment, Decker says. To this end, there are built-in time limits in two categories: contract workers of from one to six months, extendable to two years maximum; and pool workers who come and go, to a total of 1,400 hours a year. So far, attracting the right mix of workers has been no problem, the company says.

Part of the impetus for Flex Force springs from HP's no-fire policy, a stance that cost it dearly in 1985. During that downturn, HP kept several thousand unneeded workers on its payroll and "learned a lesson," Decker says, about how temp help interleaved with the permanent staff might ease the pangs without violating the no-layoff policy.

PIONEERING EFFORT. With its vast resources, HP can afford to hand-tool an internal temp force to precise needs. "It is one of the programs that is particularly interesting," notes Helen Axel, an economist at the Conference Board. "It is a positive approach that is testing the waters." But most other high-tech firms have to depend on agencies to supply them, creating opportunities these temp outfits are eager to meet. The action is spirited both in specialized technical agencies that are proliferating throughout the country and in general-purpose temp companies that are adding high-tech workers to their employee rosters.

With the added interest has come a change in attitude, says Michael Iandoli, executive vice president of Technical Aid Corp. of Newton Upper Falls, Mass. "Temporary technical talent commands more respect today than 10 years ago," he says. His company, located adjacent to Boston's Route 128 electronics and computer hotbed, is 20 years old this year, and Iandoli can't think of a major company in the region that hasn't used its talent bank. The payroll averages about 9,000 persons per week, he says, from office locations throughout the U. S. in three major areas: design engineers and draftsmen; software personnel for business applications; and software designers and programmers for scientific tasks.

Most executives say that in the minds of their clients, the watershed for temporaries came during the major recession in 1981-82. "That was the jump-off point," says Phil Bratspis, president of United Temporary Personnel Services in Brea, Calif. "Before that, companies primarily wanted work-overload and vacation relief—we were a necessary evil." But the concept of flexible staffing, allowing companies to hold their direct work force to a minimum, then became so attractive that "overnight it changed."

Also contributing was the word- and data-processing revolution brought on by the personal computer, which "parallels the growth of temporary companies," he says. "Most companies buying the equipment couldn't run it, and this forced them to come to the temporary-help industry, which had people who could."

A new twist in the technology field that's giving strong signs of taking off for United involves managing entire production plants for clients on a turnkey basis. The firm now has a half dozen such facilities-management projects, compared with none a year ago, says Bratspis. This approach allows the phased use of temporaries as what amounts to "just-in-time" personnel. Expect to hear more of JIT temps, says Bratspis, because the concept dovetails so smoothly with what may be the hottest idea for increased productivity now being pursued in the U. S.

DESIGNERS. The bulk of agency personnel, however, is employed not for JIT reasons but for design projects, says Jerry Kapalko, senior vice president of temp supplier Olsten Corp. of Westbury, N. Y. "There was a tremendous expansion in this market when companies realized the design side of their business was cyclic, and stopped hiring full-time employees to do what amounted to a part-time job." Even the hefty premiums that clients must pay for a highly skilled temp designer—which could amount to as much as 50% more than a typical salary—is no hindrance: "They know the work will go away in a few weeks or months."

If hiring design specialists on a project basis works well for a growing list of firms, then it makes sense for many to take a further step into turnkey product development by third-party houses. The emergence of Tidewater Associates Inc. during the past several years has shown what these houses have to offer. Founded in 1984, the Union City, Calif., firm has built design expertise in some of the hottest product categories, along with an enviable client list. It offers one-stop development, from concept to pilot manufacturing, or handles any part of that process.

A successful series of assignments helped overcome ingrained industry resistance about letting key research and development move outside direct control, says founder and chief executive Bernard Daines. Besides delivering the goods with the promised performance, he says, Tidewater does it on a stepped-up schedule that clients couldn't hope to match internally. "We have a different mentality, geared to a faster pace," he says. Unlike contract engineers from temp firms, Tidewater does all the work at its own site with the help of the newest computer-aided design gear and a design team "at the cutting edge, which would be prohibitively expensive for most organizations," Daines says.

ASIC SPECIALISTS. It is not coincidental that Tidewater's core technology is in application-specific integrated circuits, which support most new products. All companies are aware of the value of ASIC advances, Daines says, "but haven't bitten that bullet yet" in terms of in-house expertise. That's where Tidewater steps in.

Among the jobs that have propelled Tidewater's revenue to more than $8 million currently was the development of complex printed-circuit boards for a Pacific Bell trial communications system at an unheard-of one-a-week pace for some 35 weeks. When Bell & Howell Co. asked Tidewater to streamline the design for an optical-disk-based system to be used as an on-line graphics data base, the firm responded posthaste. Within five months, it created system architecture, designed hardware and software, and packaged the product for beta testing. Since speed in getting a product to market is preeminent among managers' concerns, says Daines, Tidewater's turnaround time justifies its stiff fees, which can reach six figures. "A substantial share of Tidewater's business stems from repeat clients and referrals," he says.

Additional reporting by Lawrence Curran and Jack Shandle

"What do you think of when I say 4 Megabit DRAM?"

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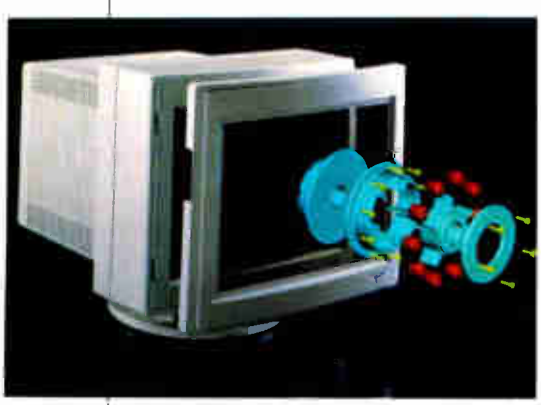
Circle 41

IT'S A NEW AGE

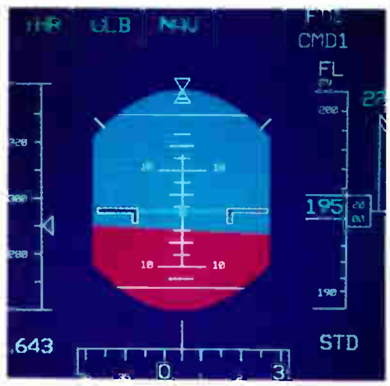
As the HDTV era dawns, liquid-crystal displays are starting to challenge the CRT as the scheme of choice for flat-panel TVs. Large LCDs with vivid color and high contrast are on the scene as vendors perfect the active-matrix approach



Tektronix uses liquid crystals as a color shutter to produce color graphics in 3-d.

If any flat-panel technology looks like a sure bet to replace the venerable cathode-ray tube, it's liquid-crystal displays. LCD technology is making rapid strides toward vivid color, larger screens, higher contrast, and greater viewing angles, thanks to improvements in materials, driving circuitry, and manufacturing. And it's especially attractive as the electronics industry casts its collective eye toward high-definition TV.

The demand for LCDs is coming mostly from the consumer side, as evidenced by the proliferation of 2- and 3-in. hand-held color TV sets. This segment will show a compound annual growth rate of more than 30% between now and 1994, when sales will top $1 billion, says Joseph A. Castellano, the president of Stanford Resources Inc., a San Jose, Calif., market-research firm. Larger TVs are embracing LCDs, as well—table models with 6-in.-diagonal screens will make their debut later this year, and 14-in. models will probably be on the market in 1990, Castellano says.



For military applications, GE offers a very high-resolution TFT display.

And ultimately, LCD flat panels may be the technology of choice for the hotly pursued HDTV market, with wall-type displays of up to 40 in. diagonally.

A secondary driver is the growing market for laptop computers and auto, military, and avionics displays. Some of the smaller TV panels will soon be found, for example, in the backs of airline seats, giving passengers more in-flight entertainment options. By 1994, Castellano says, the nonconsumer market for LCDs will grow to $2.1 billion. Unless some radical shifts occur, Japan, which has about 75% of the worldwide LCD market, will continue to dominate, though its share will dip to 55% by 1994, Castellano says.

Of course, relegating CRTs to the dust heap is a bit premature—the cost differential between them and LCDs will keep the tubes at the top of the display world well into the 1990s. But there's no question that LCDs are in hot pursuit. Thomas Credelle, manager of a military LCD project at General Electric Co.'s Research and Development Center in Schenectady, N. Y., pegs the crossover point for replacing CRTs at two or three years for sizes below 5 in., the mid-1990s for displays up to 10 in., and 10 years for sizes 13 to 15 in.

Generating most of the excitement in LCD development is work being done in active-matrix technology. It has "the best chance [in the LCD-CRT battle], because that has attracted the heaviest investment in R&D of all the display technologies," Credelle notes. In this approach, arrays of thin-film transistors (TFTs) or diodes—usually of amorphous silicon—are incorporated directly into the display module to drive the individual picture elements. Active-matrix displays yield high contrast, good color, and a wide viewing angle.

They also "preserve two of the most attractive features of LCDs—namely, low power consumption, which translates to portability, and low voltage, which means they can be driven from TTL logic levels," says Lionel Robbins, vice president of sales and marketing for Ovonic Imaging Systems in Troy, Mich. Even more important, he says, active-matrix technology pushes the inherently slow-switching LC material to video speed, "which you can't get out of earlier kinds of LCDs."

Analyst Castellano says that by 1994, active-matrix types will dominate the higher-range LCD products, such as TVs, computers, and instruments. Right now, though, production comes at some cost. The active matrix is actually a very large integrated circuit deposited on glass, and the larger the display, the more thin-film active elements are required and the greater the chance for defects.

Further complicating production is the fact that in a color display, the number of pixels is quadrupled and filters must be added with somewhat critical alignment. All this makes for relatively low yield and keeps the cost of manufacture high. But manufacturers are learning how to increase yield with better processing equip-

FOR LCDs

BY SAMUEL WEBER

LCDs are finding their way into a new generation of small-screen TVs for both the consumer and nonconsumer markets, including this one set into an airline seat. The technology is also being primed for the large-screen HDTV arena.

ment and control of equipment, as well as by the use of redundancy in their designs.

As their name implies, LCs are materials with an orderly molecular structure but which have the properties of a liquid. The most common LC material in use today is the so-called nematic, in which the molecules are all oriented in the same direction. A recently developed variation is twisted nematic (TN), in which the LC molecules form a twisted helix.

A display is formed by sandwiching the nematic material between two glass plates. Without an applied voltage, the molecules remain twisted. Light entering the upper polarizing plate becomes oriented in one direction and passes through the twisted LC material, which rotates the polarization by 90°. The light's orientation now matches that of the rear polarizing plate and passes through, yielding a bright display.

With a voltage applied, the LC molecules line up in the same direction perpendicular to the polarized light. This blocks the light, yielding a dark display. To implement a graphic or alphanumeric display in its simplest form, an array of row-select electrodes is formed on one piece of glass and an array of column-data electrodes is formed on a second piece. Voltage applied to these causes the liquid crystal to act as a shutter, either transmitting or blocking light.

The earliest TN liquid-crystal displays suffered from poor contrast and narrow viewing angle, and they degraded at elevated temperatures. Continued improvements in recent years have overcome most of these problems. A further advance was the development of the supertwist (STN) display: with the addition of another LC polarizer plate, it yields improved contrast and viewing angle. But such displays had a characteristic blue tinge that users didn't like. To overcome this, the double supertwist (DSTN) LCD was developed. In the DSTN approach, an extra color-compensating LC glass substrate is added, resulting in an almost pure black and white display with double the contrast of the STN and a better viewing angle. Most black and white LCD panels today use the DSTN technology.

One way to improve the quality of DSTN black and white displays is to increase the twist angle of LC molecules. This creates a steeper distortion vs. voltage curve, resulting in a sharper transition threshold from off to on. When rapidly multiplexed, the result is a high-contrast, wide-viewing-angle display. Most STN displays have an angle of 180° or more. Recently, LCDs with twists of 270°, such as the Hypertwist from Tektronix Inc. of Beaverton, Ore., have been introduced for even higher contrast and greater viewing angle.

But DSTN produces greater light-transmission losses than the STN process, so it needs an intense backlighting source—a requirement that results in increased power consumption, thickness, and weight. Recently, Japan's Hitachi Ltd. and Toshiba Corp. introduced DSTN displays that replace the extra layer of LCD glass with a thin polymer film. Both companies claim substantial reductions in weight, thickness, and power consumption.

Because of the limitations of the STN and DSTN approaches, LCD developers are today embracing active-matrix technology to get the response time and resolution required of a high-quality color display. Here, a nonlinear element such as a diode or transistor is placed in series with each LC element, with a resultant increase in switching speed. Combining the liquid crystal, the TFT array, and a color filter produces a creditable full-color array. But while large displays up to 14-in. have been produced in the laboratory, the commercial technology is currently limited to a 5- or 6-in. diagonal screen.

In a typical TFT layout, amorphous silicon is the thin-film material used for the active devices. Some developers are experimenting with polysilicon, which boasts a higher mobility than amorphous silicon, thereby making it possible to integrate driver circuits right on the display substrate. But fabrication requires a high-temperature process and ion implantation, which is slow and costly. Also, storage capacitors are needed at each pixel to retain the charge during an entire frame. So despite its low mobility, amorphous silicon seems to be the technology of choice in the active-matrix arena, mainly because it can be deposited over large areas at low temperatures.

Among the companies exploring active-matrix technology is Ovonic Imaging Systems, which has developed an approach using thin-film diodes as switches instead of transistors. The diodes are vertical mesa types measuring 14 by 14 μm, and the company holds that this scheme offers a higher yield than is possible with TFTs. This is because you avoid crossing the addressing lines on any one substrate, Robbins says.

"When you build a matrix with TFTs," he explains, "you have insulated crossovers at every pixel on one of the pieces of glass that make up the display. Since the insulation is a thin film, the possibility of a pinhole or a short-through is a very real one." But with diodes, he says, "you can have the horizontal conductors on one layer of glass and the vertical on the other, so you avoid insulated crossovers."

Redundancy produces another yield advantage, according to Ovonic, since this approach makes it easy to overcome pixel defects due to diode shorts. Since diodes are two-terminal devices, introducing one or more of them in series prevents shorted pixels. The extra diodes work automatically, add no processing steps, and take up very little additional area.

COLOR IN THE COCKPIT. With this technology, Ovonic has produced prototypes of a 6-by-8-in. black and white computer display. It has 640 by 480 pixels, a contrast ratio of higher than 20 : 1, and a viewing angle wider than 140°. The company has also entered a $4.5 million codevelopment program with Allied Signal Inc. of Morristown, N. J., to develop high-resolution full-color cockpit displays of up to 8 by 8 in. for military and civilian aircraft and spacecraft. Also, it has developed for Korea's Samsung Electron Devices Co. Ltd. prototypes of a full-color 3-in. flat panel destined for hand-held TVs.

Hitachi is one of the leaders in bringing to market larger color LCD panels that can compete with CRTs in many applications. The company is utilizing both supertwist and TFT technology. Color TV sets with Hitachi's 5-in.-diagonal TFT panels are selling briskly in Japan, although they are not yet available in the U. S. Designed for portable TVs, the panels are made with a triad pixel construction, and they boast 480-by-240-pixel resolution. Only 4.2 mm thick, each unit weighs 190 grams and consumes 1 W.

The company is now offering samples in the U. S. of two versions of a 6.3-in. TFT panel, one color and one monochrome, aimed at monitor and video data-terminal applications. The color version is the largest color TFT LCD panel in production, Hitachi says. It offers a contrast ratio of 40 : 1, response time of 40 ms, and power consumption of 5 W, with fluorescent-lamp backlighting. Though it has no gray scale, the panel yields eight colors thanks to an eight-color transmissive color mode arranged as three horizontal stripes. Its resolution is thus 640 by (200 × 3); the viewing angle is 45°.

But Hitachi is not ignoring supertwisted-nematic LCD technology. At the Society for Information Displays meeting this month in Baltimore, Hitachi researchers will describe an 11-in. eight-color LCD and a 10.8-in. monochrome display implemented in this process. Intended as CRT replacements, the 11-in. unit has 640-by-480-pixel resolution and the 10.8-in. display 1,024 by 768. Hitachi America's Electron Tube Division in Schaumburg, Ill., is marketing the panels in the U. S.

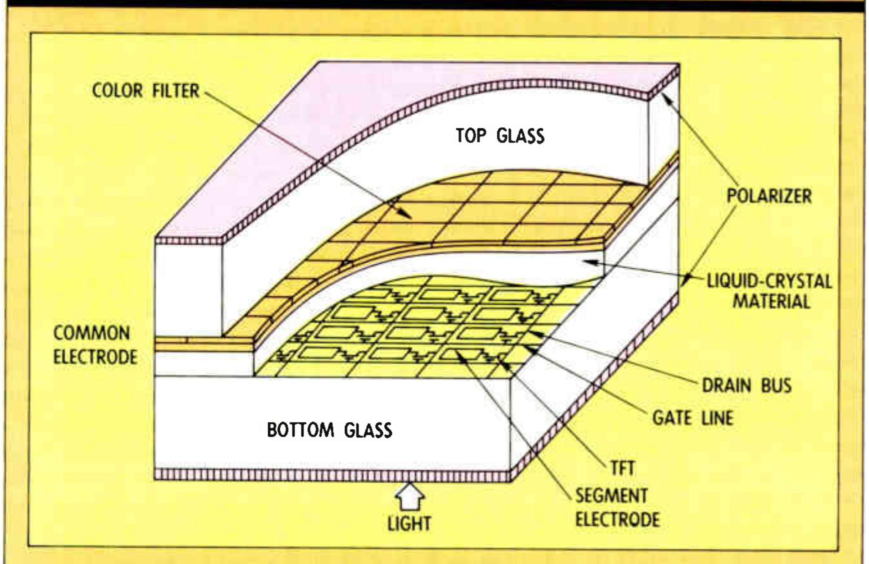
Among the highest-resolution color TFT displays fabricated so far is the one GE has developed for military and avionics applications. A joint effort by the company's Schenectady R&D center and its Aircraft Electronics Division in Utica, N. Y., has produced a 6.25-by-6.25-in. panel with a color display that can resolve 512 by 512 pixels. Its 1,024 by 1,024 elements are set out in a quad color arrangement (two greens, one red, and one blue per pixel), with 16 levels of gray scale.

Implemented with an amorphous silicon TFT matrix, the GE twisted-nematic display has more than a million transistors and a color-filter array with a thin layer of liquid crystal sandwiched in between. The TFT matrix arrays are fabricated on glass substrates using conventional thin-film processes. The TFTs are formed by depositing amorphous silicon with a plasma-enhanced chemical vapor-deposition process. Titanium gate electrodes, molybdenum source and drain electrodes, and indium-tin-oxide output electrodes are deposited by sputtering. Photolithography is accomplished with a stepper, and the films are etched with either wet or dry processes.

The color filter is formed on a gelatin layer. A negative photoresist is used to mask the gelatin layer and expose selected areas to the dyes. This process is repeated three times for the three colors. Before assembly, the TFT circuits are tested and the locations of all line defects and point defects are determined and repaired using a pulsed laser system. The yield is "quite good, considering our volume is low," says project manager Credelle. "We have the capability of producing several thousand displays a year—it's not a high-volume facility." Other sources estimate the GE yield at 55%.

Something of a landmark in large-size full-color TFT arrays appeared at the 1988 International Display Research Conference held in San Jose, Calif., when Ja-

THE ANATOMY OF A TFT DISPLAY



In active-matrix technology, TFTs or diodes are incorporated into the display module to drive the picture elements. In effect, an active matrix is a very large IC.

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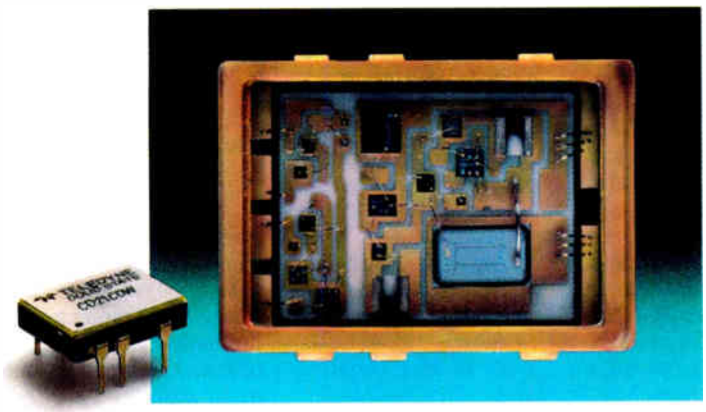
- Cost Effective



ACTUAL SIZE CERAMIC PACKAGE

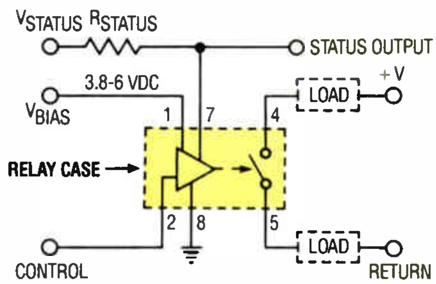
PART # CD21CDW

Review the electrical characteristics and call us for immediate application assistance.*

ELECTRICAL CHARACTERISTICS (−55°C to +105°C unless otherwise noted)	Min	Max	Units	
Bias Voltage (V_{BIAS})	3.8	6.0	V_{DC}	See Note 1
Bias Current (I_{BIAS})		15.0	mA	$V_{BIAS} = 5 V_{DC}$
Control Voltage (V_{IN})	0	18.0	V_{DC}	
Control Current (I_{IN})		250	µA	$V_{IN} = 5 V_{DC}$
Turn-Off Voltage $V_{IN(OFF)}$	3.2		V_{DC}	
Turn-On Voltage $V_{IN(ON)}$		0.3	V_{DC}	
Continuous Load Current		1.2	A	−55°C to +25°C
I_{LOAD}		0.7	A	+85°C
Output Trip Current (I_{TRIP})	2.4 (Typ.)		A	+25°C, 100ms
On-Resistance (R_{ON})		0.65	Ohms	
Turn-On Time (T_{ON})		1.5	ms	
Turn-Off Time (T_{OFF})		0.25	ms	
Status Voltage (V_{STATUS})	1	18	V_{DC}	
Status Current (I_{STATUS})		2	mA	$V_{SAT} \leq 0.3 V_{DC}$ See Note 2

Notes:
1. Series resistor is required for bias voltages above $6V_{DC}$. $RS = (V_{BIAS} - 6 V_{DC})/15$ mA
2. A pull up resistor is required for the status output. $R_{STATUS} = (V_{STATUS} - 0.3)/I_{STATUS}$
3. Output will drive loads connected to either terminal (sink or source).
4. Status circuit is a built-in test feature checking the input circuitry of the relay. Status output is low (on) when the input is on.

All power FET relays may drive loads connected to either positive or negative referenced power supply lines (source or sink modes).



TELEDYNE SOLID STATE
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Circle 39

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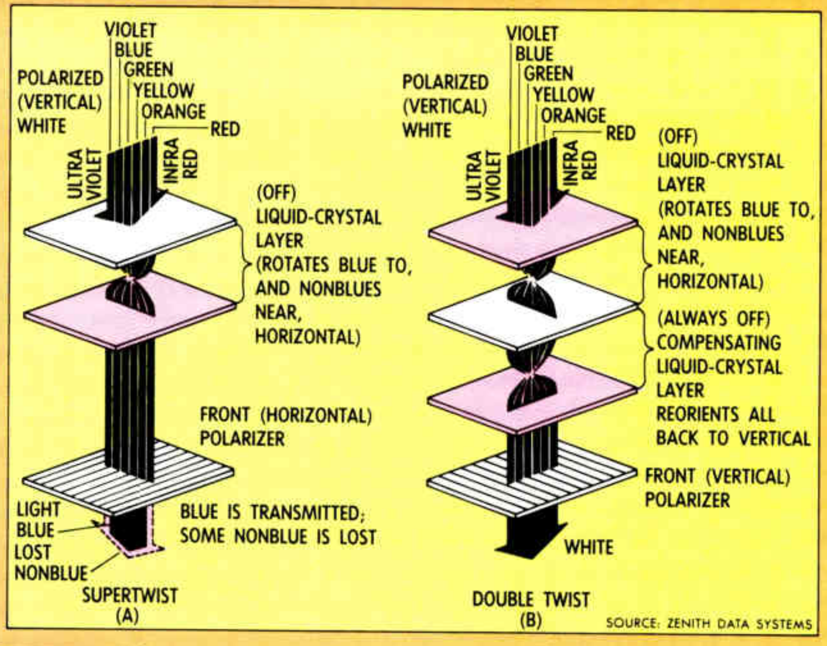
pan's Sharp Corp. demonstrated a 14-in. unit. The 642-by-480-pixel panel is implemented with a triangular pixel arrangement, and each pixel is divided into four subpixels. Each of the resulting 1,232,640 subpixels consists of a TFT and a transparent electrode placed at a point of intersection of separated gate and source bus lines. This scheme sidesteps any bending of the bus lines; also, a defect in any of the subpixels is unnoticeable in moving scenes. The panel exhibits a contrast ratio of greater than 100 : 1 at the optimum viewing angle. Sharp hasn't announced any plans for full production, but industry observers see this as a precursor of a commercial model in the next year or two.

DOING THE TWIST



To overcome the blue tinge characteristic of supertwist LCDs (A), the double-supertwist scheme (B) adds an extra LC glass substrate.

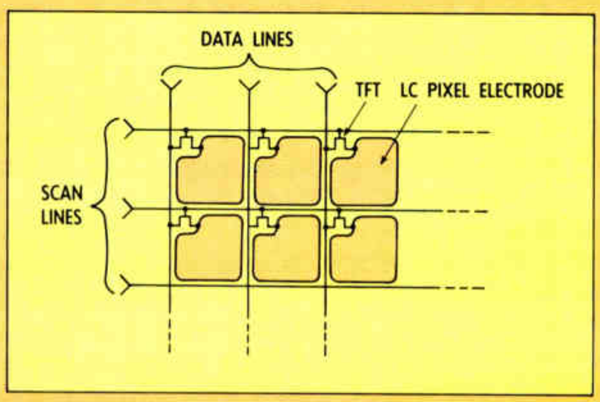
STICKING POINT. In producing high-quality, large-area LCD panels, the main technological sticking point is the ability to deposit on glass defect-free arrays of TFTs or diodes and to obtain accurate registration of such arrays with the accompanying LC cell structure. Most LCD producers use photolithographic techniques employing modified steppers, originally developed for the IC industry, to transfer circuit patterns from a master photomask to the LCD substrate. But these wafer steppers are limited in their area of coverage and too slow for efficient high-volume production of large panels. MRS Technology Inc. of Chelmsford, Mass., last year introduced the Model 4500 PanelPrinter especially designed for manufacturing active-matrix LCDs. It can go a long way toward boosting throughput and yield.

The $1.2 million system can pattern pieces of glass measuring up to 18-in. at a rate of up to 35 panels per hour, against about 10 panels/h for glass of 12 in. maximum using a modified IC wafer stepper. The 4500 also allows the gang printing of several small displays on one large piece of glass. The unit's two-camera format offers sharp focus over large areas for the photo process, while the system controls the movement of the glass substrate with high accuracy.

Though most of the work on LCDs is aimed at TVs and computer displays, LCs are finding their way into other products, too. For example, Greyhawk Systems Inc. of Milpitas, Calif., is exploiting the storage capabilities of a smectic type of LC cell in a full-color paperless plotter. It's also working on a projection system for printed-circuit-board manufacture with Du Pont Co. of Wilmington, Del.

The paperless plotter, SoftPlot, displays a full-color 22-by-34-in. (40-in. diagonal) image with 16 gray levels, 4,096 colors, and 2,200-by-3,400-pixel resolution. Its contrast ratio is 16 : 1. At its heart is a single storage-type electronic "slide," in which the LC is the storage medium controlled by a host computer. Images are written on the slide by means of a scanning infrared laser beam produced by two semiconductor laser diodes and projected by an optical system. A major application is engineering-design reviews, which can be extremely slow if hampered by the need to wait for a mechanical plotter to produce revised drawings. With SoftPlot, changes can be made instantaneously.

LAYING OUT A TFT ARRAY



Amorphous silicon is the thin-film material most often used in TFT layouts; it can be easily deposited over large areas.

The same principles are being applied to the SeriFLASH projection direct-imager system being marketed by Du Pont. Used in conjunction with Du Pont's SeriCAM work station, the system accepts manufacturing data, writes it on the LC cell, and projects it directly onto resist-coated substrates. "What this does is bring the advantages of projection lithography to pc-board fabrication," says Fred Kahn, vice president of physical technology at Greyhawk.

Elsewhere, Tektronix is developing products using the LC as a color shutter to produce three-dimensional color displays aimed at instrumentation, avionics, and medical monitors, along with the work-station and computer-aided design market. An LC shutter is an electrically activated optical bandpass filter that selects between the transmission of two colors. When the LC cell is "off," it rotates the polarization of light passing through it 90°. When electrically stimulated to "on," polarization of the incident light is left unaltered. This characteristic can be used to alternately select or reject one of two colors, and is the basis of a field-sequential display system using a monochrome CRT.

Tektronix has applied this principle to a system that produces stereo viewing—color graphics in 3-d. The Tektronix stereoscopic viewing system creates the impression of depth by first displaying the right-eye view and then the left-eye view, which the viewer sees thanks to a liquid-crystal modulator and matching viewing glasses. The main markets are in molecular modeling, surveillance, cartography, and the like. □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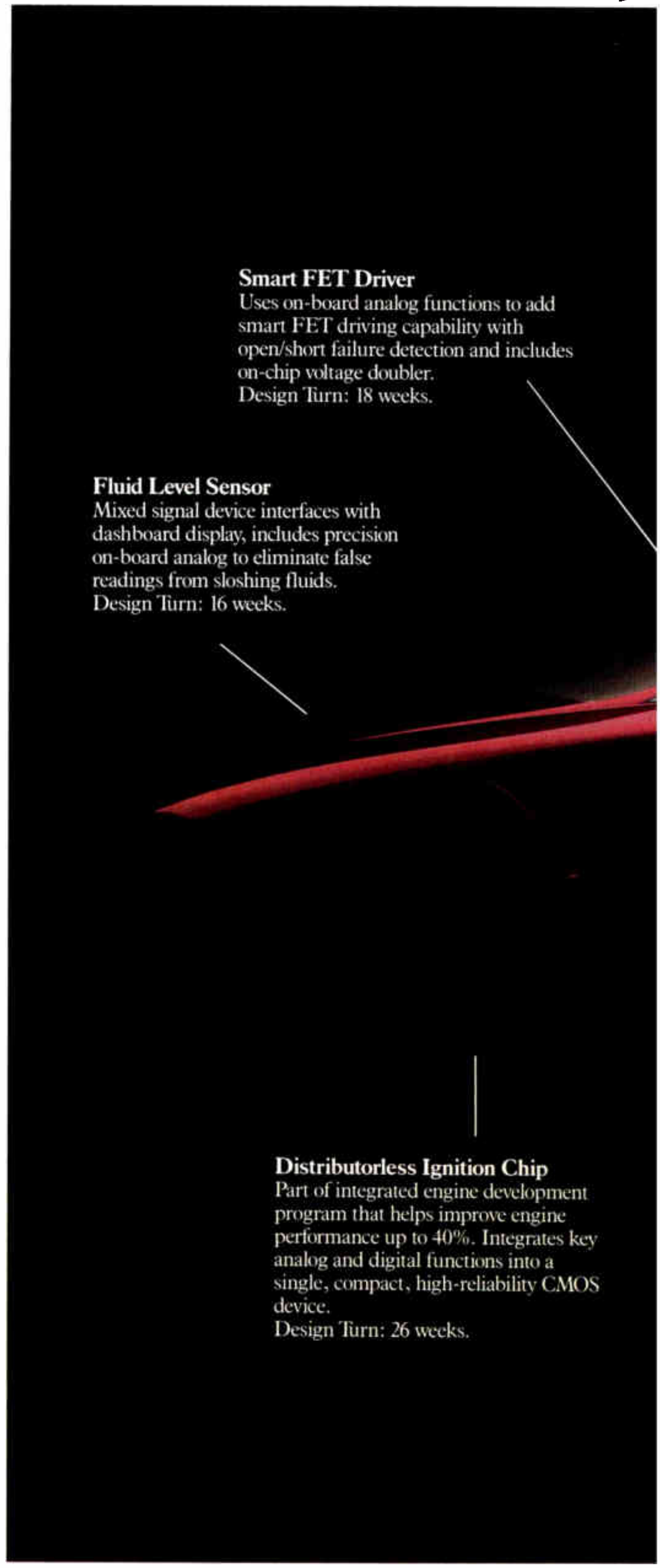

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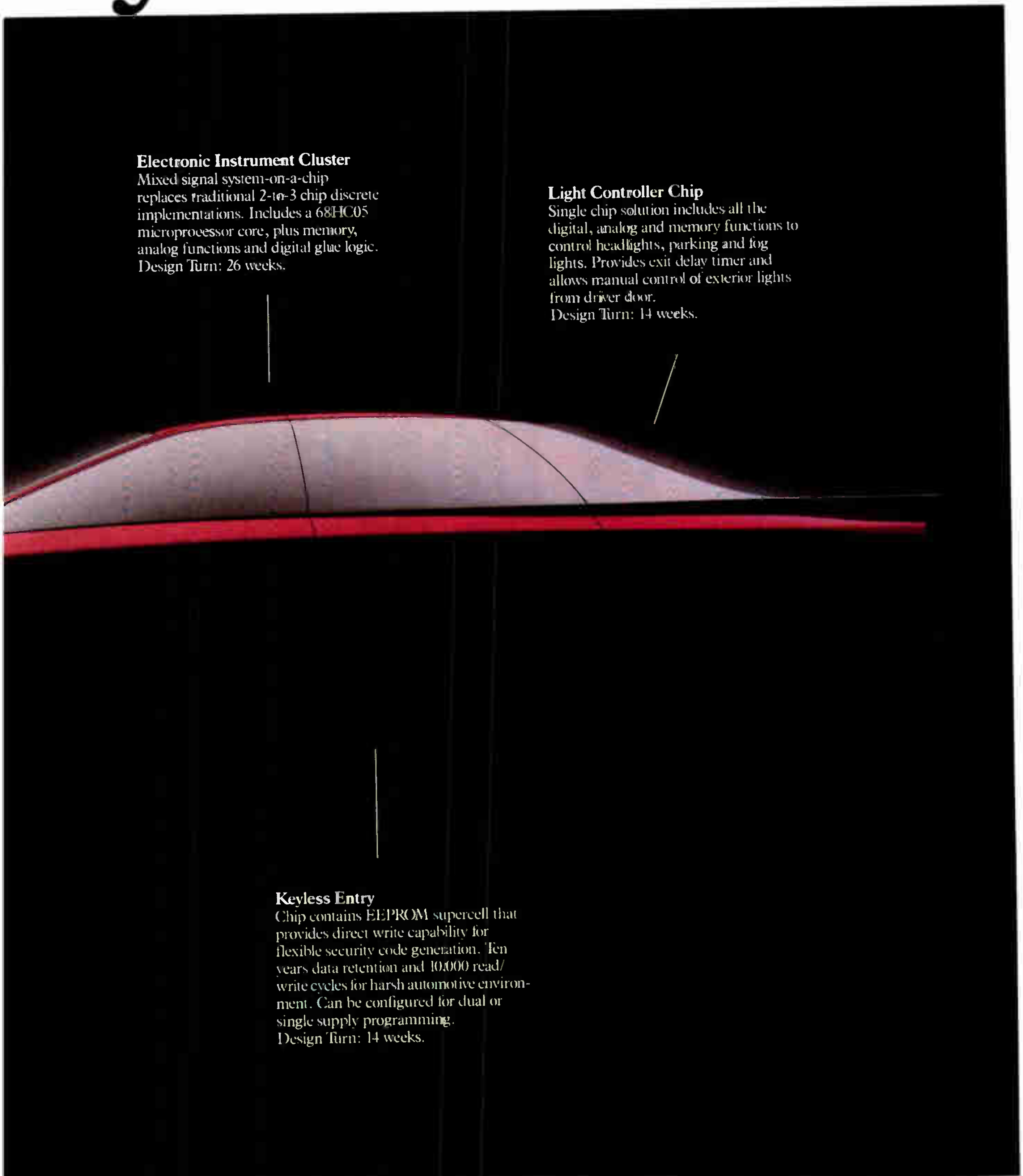


Circle 8

BY TOM MANUEL

Object-oriented programming: a star is born

It's more than • a buzzword; • real products • are here, from • full computer • systems to • languages

The software industry needs a miracle—something that can deliver on the promise and the dream of quick and easy software development. And some designers think they've found it in object-oriented programming, the technology that has become the computer industry's new buzzword. This approach, they say, goes a long way toward realizing the superhuman task that software developers must fulfill: making their products easy to use, modular, robust, extensible, portable, reusable, and free of bugs. With object-oriented programming, proponents say, even end users will be able to program without realizing that's what they're doing.

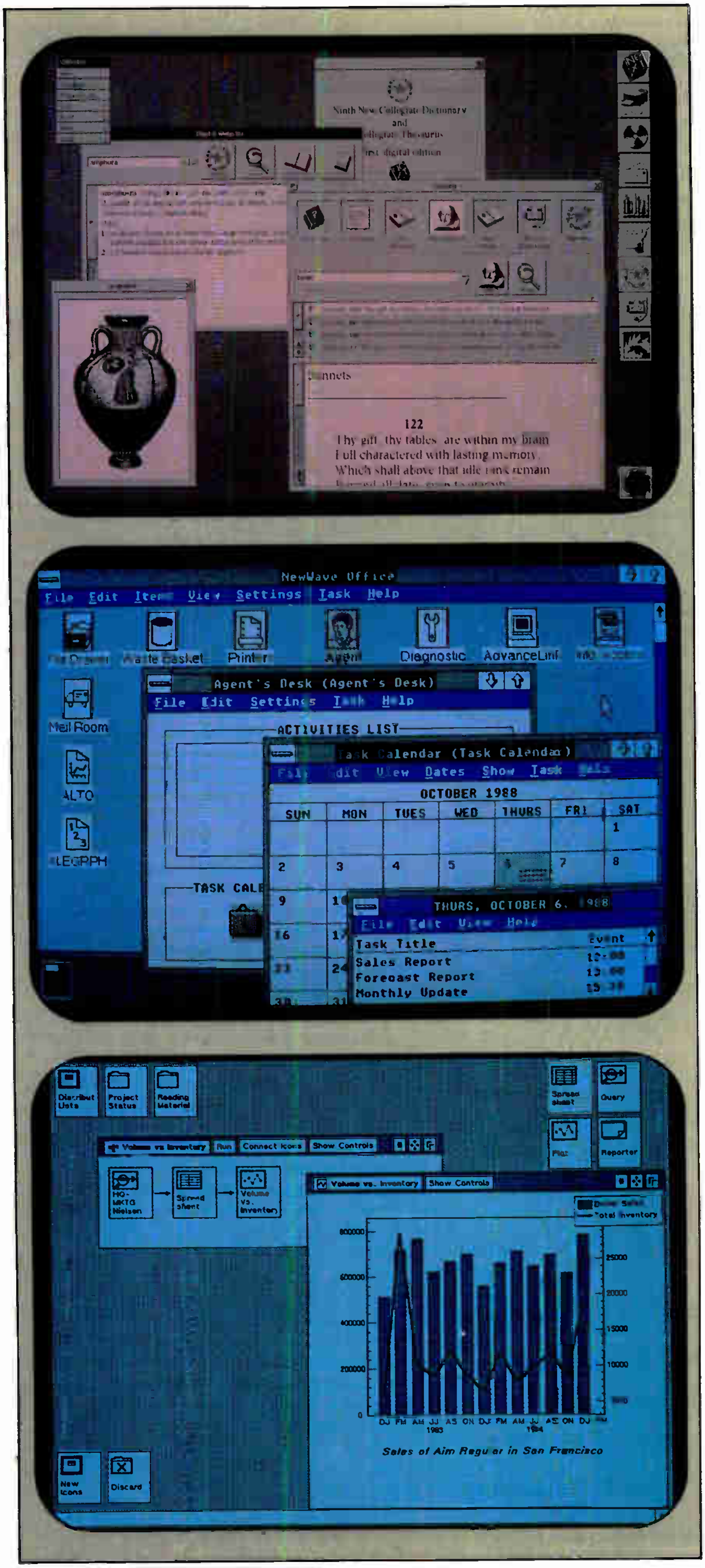
In fact, object-oriented technology is making its way into areas beyond programming. It's being used in three new computer systems that were designed from scratch as object-oriented schemes—the Next Computer System, the BiiN machine, and the IBM Corp. Application System/400. Object-oriented technology is also being applied to operating systems, programming languages, data-base management systems, user interfaces, and application-building environments.

Good examples of real products exist in all these categories. For instance, both the BiiN and IBM computers have proprietary object-oriented operating systems, while Carnegie-Mellon University in Pittsburgh has developed a Unix-compatible open operating system, Mach, that Next Inc. uses for its machine. And Microsoft Corp. of Redmond, Wash., is planning significant object-oriented extensions to OS/2. Moreover, a minor flood of products is hitting the market in programming languages (there are about a dozen that are object-oriented or possess some object-model capabilities), data bases (there are at least five specifically object-oriented data-base management systems on the market), and graphical user interfaces (some are object-based, and all the interfaces that manipulate program and data services through icons at least give the appearance of dealing with objects). And more than a half dozen products offer object-oriented application-development environments.

Despite this flurry of activity, and regardless of the fact that object-oriented programming has been a big research area for the past 10 years, this technology is still poorly understood. Users and even system developers are not clear about what object-oriented tools and technology are available, how good they are, and how they can be used.

The meaning of object-oriented programming involves an entirely new way of thinking about procedures, data, and the relationships among them. The definition is based on not one, but several, key concepts. "There are a couple or so requirements for object-orientation; there is a very exact definition," says Dave Liddle, chairman of Metaphor Computer Systems Inc., the Mountain View, Calif., maker of the Metaphor Data Interpretation System. This extremely easy-to-use object-oriented system analyzes and interprets data from multiple sources.

One requirement is the concept of packaging data and procedures together in a single, autono-



For the end user, object-oriented programming results in an easy-to-use interface laced with windows, icons, and pull-down menus. From top, the Next interface (the Shakespeare icon calls up the complete works), Hewlett-Packard's NewWave, and Metaphor's Data Interpretation System. Programming in these environments is a matter of simply manipulating objects.

mous structure, often referred to as an object. This concept is called encapsulation. "A system that embodies the concept of data structures and methods being stored together has an object model," says Liddle. Another important concept is reusability. Because objects are self-contained, they can serve as standard software modules to be used over and over in a variety of programs.

Finally, "to be truly object-oriented, a system must also embrace the notion of classes and inheritance," says Liddle. Objects are placed in an inheritance hierarchy and new objects can be created simply by defining how they differ from their parents. New objects inherit the characteristics (data structure and procedures) of all preceding objects in the hierarchy.

A STRETCH. In some systems, multiple inheritance allows subclasses to inherit characteristics from more than one branch of the hierarchy. Object generation becomes simpler and simpler as the hierarchy grows. This concept is often called extensibility. One of the big advantages of object orientation is that the more subclasses that exist, the more code can be reused. A disadvantage is that as subclasses are added, programs get bigger and lots of memory is required.

These ideas spring from "three independent and separate evolutions of object-oriented technology," says Daniel Wood, manager of software-product planning at BiiN in Hillsboro, Ore. First, he says, is the graphics world, with its windowing and iconic interfaces, such as those used in Apple Computer Inc.'s Macintosh and in such software as X Windows and Microsoft Windows. Second is conventional programming, where in the face of the inadequacies of structured programming designers have hit upon an object-oriented concept, defining subunit building blocks for creating complex systems. In Ada, for example, the definition of objects is not all that different from the object definition in the graphics-object world.

Third is the world of computer-system architecture exemplified by BiiN, Next, and the IBM AS/400. Object-oriented technology offers a new way to think about computing—a human-centered way. Its critical theme is based on the observation that the things (objects) that we wish to model in computing change much less rapidly than the ways we wish to use them. Object-oriented technology offers a way to describe the content and behavior of application entities (objects) in an efficient, controlled, and manageable way. Once objects are defined, they can be freely used without worrying that their behavior will change as the behavior of other objects changes. For example, a change in the detailed behavior of an account will not cause changes in the definition of a ledger.

Objects can be constructed that are different from existing objects by simply specifying the differences—the structure of a debit transaction differs very little from that of a credit transaction, for instance. Objects of any degree of complexity are easily defined by composing them out of existing objects in this way.

The architecture of the Next Computer System, introduced last year, "is almost completely object oriented, from the perspective of the operating system on up," says Bob Fraike, Next's system software product manager. "We chose the Mach operating system because it provides an object-oriented approach to a Unix kernel," he says. "The Next system provides a path of least resistance for porting Unix applications," since third-party Unix applications can be quickly ported to it. And they will all have the same user interface. "This is the future of Unix," he says.

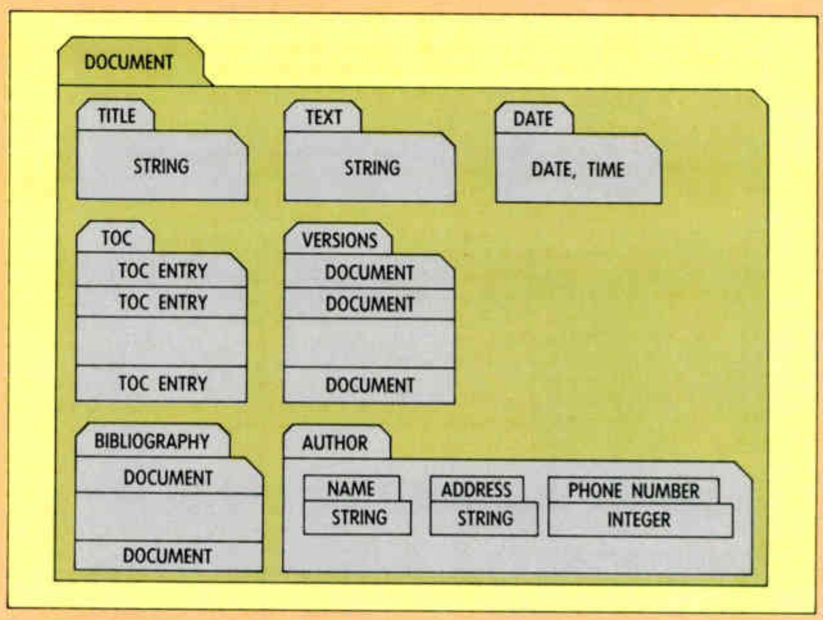
Using the object-oriented programming language Objective C from the Stepstone Corp. in Sandy Hook, Conn., Next built the NextStep development and user-interface environment. The Palo Alto, Calif., company used the features of Mach and Objective C to develop kits, such as an application kit and a music kit, which along with a simple-to-use interface builder let developers create very interesting, consistent applications quickly. For example, one programmer, Greg Cockcroft at Frame Technology Corp., was able to port that San Jose, Calif., firm's popular FrameMaker application to the Next system in just two weeks.

Next also supports other object-oriented programming languages, such as Allegro Common Lisp from Franz Inc. and Absoft's object-oriented Fortran. Language developers want to see the same thing done with Pascal and other languages, Fraike says. When developers use the Next interface builder, all applications built with it over time will have a consistent look and feel. Users will be able to instantly learn new programs.

At $9,995, the Next machine will be available, starting this month, from a new Advanced Systems division of Businessland. Since its introduction last October, the machine has been sold (at a discount) to the higher-education market only. Businessland will position it as a high-end business work station.

At BiiN, a joint venture of Intel Corp. of Santa Clara, Calif., and Siemens AG of Munich, another complete object-oriented computer architecture has been developed, with object orientation built in from the chip level to the applications. The system evolved out of earlier work on an object-oriented microprocessor development, called the 80432, at Intel. Its main design goal is to completely support mission-critical computing applications—those that are crucial to the day-to-day operation of a business. "Systems today must be as dynamic, flexible, and agile as the organizations that use them, and therefore must provide enhanced flexibility, maintainability, security, and availability," says Joseph J. Kroger, BiiN's president and chief executive officer.

REPRESENTING A REAL-WORLD DOCUMENT



A document represented as an object may contain any number of autonomous subunits; users can change any one of them with no fear of disordering the overall file.

The BiiN engineers designed and built a complete integrated system of hardware and operating software with the sole goal of serving application programs. The design of these systems focuses on the services required. It becomes very complex, especially when the security, reliability, and availability of these services are paramount, as in mission-critical systems. Such a system must deal effortlessly and reliably with internal and external objects.

In the case of BiiN, anything that enters the system is treated as an object. There are no exceptions. An object definition accommodates everything the computer can handle, such as a user's file, internal operating-system tables, and operating-system functions, such as device drivers. Data and the routines to operate on them are just one type of object in this system. The fundamental service objects in the BiiN system are secure and can be trusted.

Object-oriented technology offers a new way to think about computing: a human-centered way. It's a means of describing behavior efficiently

The third computer system exhibiting object-oriented features is IBM's new midrange AS/400, introduced last June. The AS/400 architecture has built-in features supporting data-base, security, graphics, and image functions. It also incorporates communications support and a number of programming tools.

For these computer systems to work, their designers needed a brand-new object-oriented operating system. One of the benefits of such an OS is the simplification of programming. For example, programmers writing for IBM's proprietary solution, OS/400, can avoid the tedious tasks normally required, such as defining the location of files on disks or the allocation of program sizes, by simply defining objects. Once a data structure is defined as an object, no further definition is required. For example, if a user changes a Zip code or extends the size of one to include four extra digits, the system-object manager makes those same changes on all other programs accessing that data object.

BiiN's solution, also proprietary, is BiiN/OS, which has built-in support for Posix and other industry standards for Unix, though it is nothing like Unix inside. Instead, BiiN/OS consists of more than 200 thoroughly tested packages written in Ada. Because each package is defined, like everything in the BiiN system, as a conventional object, the OS can easily be extended by creating new objects. If the extension does not work right, it cannot

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*Christopher Kreager, Systems Specialist, UNITED DATA SYSTEMS

Circle 2

affect the existing stable objects in the operating system and the integrity of the computer system is maintained. "This capability provides an easy and safe path to future functions; conventional systems cannot do this," says BiiN's Dan Wood.

The one nonproprietary OS that's object-oriented is Mach. Its kernel can be easily extended by adding kernel objects that run in user space. "Mach furnishes a basic kernel onto which a number of different operating-system environments can be layered," says Richard F. Rashid, Mach's chief researcher and associate professor of computer science at Carnegie-Mellon. Traditional Unix kernels, which all run in system space, are getting too big and unwieldy and are too hard to modify safely. With Mach, the basic system kernel is small. System vendors can add whatever kernel objects they want to create their specific systems. For example, from the base of kernel objects, the Next system developers looked outward to create an object-oriented development and application environment.

Other features in Mach include the ability to execute multiple activities or threads within a single program. Mach integrates communications with the virtual memory management, a facility for programs to exchange large amounts of data at very low cost. It also lets user programs create and manage memory objects, which can be mapped into the address space of user-level programs and managed by these programs, allowing efficient implementation of system services such as transaction processing.

The next object-oriented operating system to surface might well be OS/2. Microsoft, the developer of operating systems for IBM's personal computers and compatibles, has revealed extensive plans for objected-oriented features to be added to future versions. Support for object-oriented programming is planned for the OS itself in the form of an application-object protocol and a system-object manager. Also, Microsoft will provide a storage-mechanism object by building an object-oriented file system on top of the OS/2 file system. This will support compound objects, remote objects, and hot links between objects. An external control language for objects will also be added. The new OS/2 will support object-oriented programming languages, development tools, and user interfaces.

NEW TONGUES. Along with operating systems, programming languages that support the object model are emerging as important tools in this new field. Conventional languages can be used to produce object-oriented environments and write object-oriented programs, as Hewlett-Packard Co. proves with its NewWave environment. But the object-oriented languages make the job easier.

The earliest object-oriented programming was accomplished primarily by using a once-obscure language, Smalltalk. Now the pendulum is swinging toward languages that are object-oriented extensions to better-known languages, such as C and Basic. Two languages that provide strong support for objects are outgrowths of C; these are C++ and Objective C. Programs written with them can be compiled with a C compiler.

Microsoft will offer C++ for OS/2 and will also develop an object-oriented version of Basic it calls visual Basic. Next is offering, as well as using, Stepstone's Objective C. Smalltalk, C++, and Objective C are also available for a number of other computers and work stations. C++ was developed at AT&T Bell Labs. Versions are offered by several vendors, including the Oasys division of Green Hills Software Inc. of Waltham, Mass., and Oregon Software Inc. of Beaverton.

A number of data-base management systems based on object-oriented technology are now on the market. They include Gemstone from Servio Logic Development, Vbase from Ontologic, Object Store from Object Design, G-base from Graphael, and Hoops, an object-oriented graphics data base from Ithaca Software.

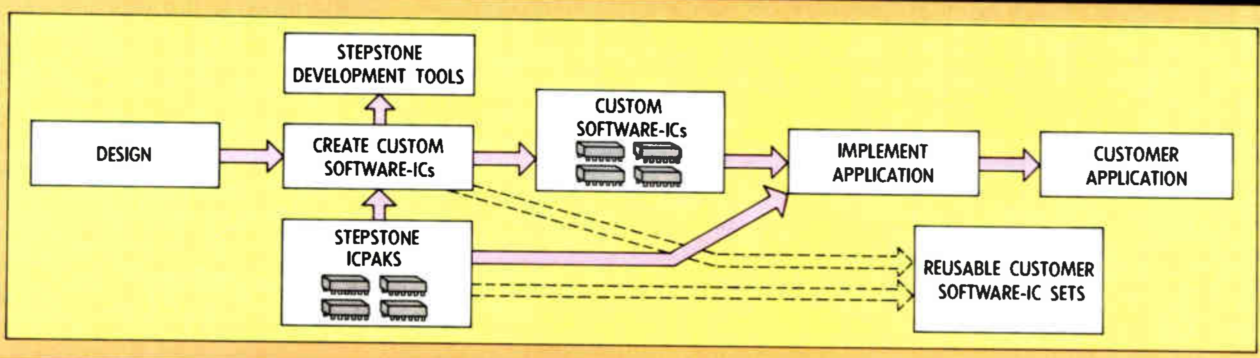
Another approach to object programming is HP's NewWave, a PC-based application environment that offers a way to get the advantages of object-oriented programming using conventional programming and existing applications. The Palo Alto company is "applying the technology and concepts of object-oriented programming at the application level only," says Beatrice Lamb, the manager in charge of the Object Management Facility within NewWave. The objects in NewWave are a manifestation of an application binding to data, Lamb says. The NewWave development kit is currently available for industry-standard MS-DOS PCs with 286 and 386 processors. The end-user version will be ready this summer.

The graphical user interface for the MS-DOS version is supplied by the Microsoft Windows program, to which HP has added an object-management facility and task automation. NewWave objects can be many different types, including spreadsheets, data bases, text, graphics, voice, and scanned images. The object-management facility (OMF) keeps track of the data needed for each object and the application that knows how to manipulate it. NewWave also maintains persistent links between objects and everywhere they are used, so that an update to an object is automatic throughout the system.

One of the big advantages of NewWave is that the applications used with it are written using conventional methods. The OMF provides an object-based file system on top of the MS-DOS file system to manage the data and applications relationships—it becomes the file system, and the standard file system is hidden from the user.

Another major benefit of an object system like NewWave is the ease with which a user can combine information of different types to create compound objects containing, for example, text, graphics, scanned images, and voice. The OMF manages the links among the composite objects so that all the components are kept intact. □

DEVELOPING AN OBJECT-ORIENTED LANGUAGE



To enhance its Objective C language, which is used in the Next machine, Stepstone Corp. uses what it calls ICpaks, predefined objects that are the modular-software equivalents of plug-in application-specific integrated circuits.

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	5.00	4.30	3.20	–	$4\frac{9}{32} \times 3\frac{13}{16} \times 9$	390	370	**LMS-4008**
	10.00	7.90	6.30	–	$4\frac{9}{32} \times 3\frac{13}{16} \times 10$	462	440	**LMS-5008**
	20.00	20.00	16.50	13.5	$4\frac{9}{32} \times 3\frac{13}{16} \times 11$	620	590	**LMS-6008**
	100.00	90.00	78.00	57.0	$4\frac{9}{32} \times 8 \times 11\frac{7}{8}$	1176	1120	**LMS-9008**
0-18 VOLTS	1.60	1.30	0.80	–	$4\frac{9}{32} \times 3\frac{13}{16} \times 8$	263	250	**LMS-3018**
	2.40	2.10	1.50	–	$4\frac{9}{32} \times 3\frac{13}{16} \times 9$	390	370	**LMS-4018**
	4.50	3.50	2.80	–	$4\frac{9}{32} \times 3\frac{13}{16} \times 10$	462	440	**LMS-5018**
	9.00	9.00	8.20	6.6	$4\frac{9}{32} \times 3\frac{13}{16} \times 11$	620	590	**LMS-6018**
	45.00	40.00	33.00	25.0	$4\frac{9}{32} \times 8 \times 11\frac{7}{8}$	1176	1120	**LMS-9018**
0-40 VOLTS	0.70	0.60	0.35	–	$4\frac{9}{32} \times 3\frac{13}{16} \times 8$	263	250	**LMS-3040**
	1.00	1.00	0.85	–	$4\frac{9}{32} \times 3\frac{13}{16} \times 9$	390	370	**LMS-4040**
	2.00	1.60	1.30	–	$4\frac{9}{32} \times 3\frac{13}{16} \times 10$	462	440	**LMS-5040**
	4.00	4.00	3.80	3.1	$4\frac{9}{32} \times 3\frac{13}{16} \times 11$	620	590	**LMS-6040**
	20.00	18.00	15.00	11.0	$4\frac{9}{32} \times 8 \times 11\frac{7}{8}$	1176	1120	**LMS-9040**
0-60 VOLTS	0.50	0.42	0.25	–	$4\frac{9}{32} \times 3\frac{13}{16} \times 8$	263	250	**LMS-3060**
	0.70	0.70	0.60	–	$4\frac{9}{32} \times 3\frac{13}{16} \times 9$	390	370	**LMS-4060**
	1.40	1.10	0.90	–	$4\frac{9}{32} \times 3\frac{13}{16} \times 10$	462	440	**LMS-5060**
	2.80	2.80	2.60	2.1	$4\frac{9}{32} \times 3\frac{13}{16} \times 11$	620	590	**LMS-6060**
	14.00	12.00	10.00	8.0	$4\frac{9}{32} \times 8 \times 11\frac{7}{8}$	1176	1120	**LMS-9060**
0-120 VOLTS	0.25	0.21	0.13	–	$4\frac{9}{32} \times 3\frac{13}{16} \times 8$	263	250	**LMS-3120**
	0.36	0.36	0.30	–	$4\frac{9}{32} \times 3\frac{13}{16} \times 9$	390	370	**LMS-4120**
	0.70	0.55	0.45	–	$4\frac{9}{32} \times 3\frac{13}{16} \times 10$	462	440	**LMS-5120**
	1.40	1.40	1.30	1.0	$4\frac{9}{32} \times 3\frac{13}{16} \times 11$	620	590	**LMS-6120**
	7.00	6.00	5.00	4.0	$4\frac{9}{32} \times 8 \times 11\frac{7}{8}$	1176	1120	**LMS-9120**

LMS SERIES

Specifications

DC OUTPUT
Voltage range shown in table.

REGULATED VOLTAGE
CONSTANT
regulation, line ...... 0.05% for line variations from 85 to 132VAC or 170 to 265VAC. 0.01% + 1mV for LMS-3000.
regulation, load ..... 0.05% for load variations from 0 to full load. 0.01% + 1mV on LMS-3000 Series.
remote programming resistance .... customer adjustable from 200Ω/V to 1000Ω/V. (200Ω/V on LMS-3008 through LMS-3060. 400Ω/V on LMS-3120.)
remote programming voltage .... volt per volt or 0-5 volt signal for zero to full voltage out, customer selectable.
ripple and noise ..... 1mV RMS, 5mV pk-pk on all LMS-3000 models.
5mV RMS, 35mV pk-pk on 8V and 18V models.
10mV RMS, 75mV pk-pk on 40V and 60V models.
20mV RMS, 150mV pk-pk on 120V models.
temperature coefficient .... 0.03%/°C. (0.01%/°C on LMS-3000 Series.)

CONSTANT CURRENT
(Current regulated line and load) Automatic Crossover.
current range .... 5% to full load current. (1% for LMS-3000)
regulation, line ...... 0.3% of Io (max) for line variations from 85 to 132VAC or 170 to 265VAC. 2.5mA or 0.1% (whichever is greater) on LMS-3000 models. 2.5mA or 0.3% (whichever is greater) on LMS-4000 models.
regulation, load ..... 0.3% of Io (max) for load variations from short circuit to rated DC voltage. 2.5mA or 0.1% (whichever is greater) on LMS-3000 models. 2.5mA or 0.3% (whichever is greater) on LMS-4000 models.
current ripple .... .1% Io(max) RMS.
remote programming current .... 0-5 Volt signal for zero to Io (max).

AC INPUT
line .... 85 to 132VAC or 170 to 265VAC, user selectable.
power .... LMS-3000 Series: 62 watts max.
LMS-4000 Series: 79 watts max.
LMS-5000 Series: 135 watts max.
LMS-6000 Series: 245 watts max.
LMS-9000 Series: 1100 watts max.
RMS current .... LMS-3000 Series: 1.2A RMS max.
LMS-4000 Series: 1.35A RMS max.
LMS-5000 Series: 2.7A RMS max.
LMS-6000 Series: 4.2A RMS max.
LMS-9000 Series: 17.5A RMS max.

EFFICIENCY

Model	Minimum Efficiency at Max P_{out}
LMS-3000	45%
LMS-4008, 4018	55%
LMS-4040, 4060, 4120, 5008, 5018	60%
LMS-5040, 5060, 5120, 6008, 6018	65%
LMS-6040, 6060, 6120	70%
LMS-9008	72.5%
LMS-9018, 9040	75%
LMS-9060, 9120	77.5%

OPERATING TEMPERATURE RANGE
Continuous duty from 0°C to +71°C with appropriate deratings from 40°C to 71°C (0°C to 0 +60°C for LMS-3000, 4000 and 5000).

STORAGE TEMPERATURE RANGE
−55°C to +85°C.

OVERLOAD PROTECTION
THERMAL
Internal temperature sensing circuit protects unit from excessive ambient temperature on the LMS-3000, 4000 and 5000 Series. The LMS-6000 and LMS-9000 Series are protected from inadequate air velocity by an internal airflow sensing circuit. When shutdown occurs, a rear panel LED indicator will turn on. AC power must be momentarily removed from the unit after thermal shutdown in order to restore operation.
ELECTRICAL
External overload protection — adjustable, automatic electronic current-limiting circuit limits output current to preset value. Current-limiting setability to 100% of rated current via front panel adjust. In addition an internal peak inverter current limit circuit protects the power supply during load transients.

OVERVOLTAGE PROTECTION
Built-in, adjustable overvoltage protection is standard on all sets. When pre-set voltage is exceeded, the overvoltage protector removes the inverter drive. AC power must be momentarily removed from unit after overvoltage shutdown in order to restore operation. Trip point is set by screwdriver adjust.

Overvoltage Protection Adjustable Ranges

Model	Vov(Min)	Vov(Max)
LMS-3008, 4008, 5008, 6008, 9008	4V	11V
LMS-3018, 4018, 5018, 6018, 9018	4V	24V
LMS-3040, 4040, 5040, 6040, 9040	8V	50V
LMS-3060, 4060, 5060, 6060, 9060	8V	70V
LMS-3120, 4120, 5120, 6120, 9120	20V	130V

IN-RUSH CURRENT LIMITING
Limits in-rush current at turn-on to 20A on LMS-6000 and LMS-9000 Series, 90A on LMS-3000 Series, 20A on LMS-4000 and 5000 when connected for 110VAC input and 40A when connected for 220VAC input.

COOLING
The LMS-3000, 4000 and 5000 are convection cooled. The LMS-6000 and LMS-9000 are fan cooled. Leave adequate clearance for air intakes and exhausts.

CONTROLS
DC OUTPUT CONTROLS
Simple screwdriver adjustment over the entire voltage range.

EMI
All units will meet FCC 20780 Class A and VDE 0871 Class A.

INPUT AND OUTPUT CONNECTIONS
Input connections via an IEC power line connector. DC output connectors via heavy duty, PC board mounted barrier strips (threaded bus bars on LMS-9008 and LMS-9018 units). (AC mating connector available, consult factory.)

LED STATUS INDICATOR
Overvoltage or overtemperature indicator on rear panel.

REMOTE SENSING
Provision is made for remote sensing to eliminate effect of power output lead resistance on DC regulation.

REMOTE ON/OFF
A TTL low or short enables the unit. A TTL high or open circuit turns the unit off.

PHYSICAL DATA

Package Model	Weight Lbs. Net	Weight Lbs. Ship	Size Inches
LMS-3000	6	7	4 9/32 × 3 13/16 × 8
LMS-4000	4.5	5.5	4 9/32 × 3 13/16 × 9
LMS-5000	7	8	4 9/32 × 3 13/16 × 10
LMS-6000	7.25	8	4 9/32 × 3 13/16 × 11
LMS-9000	14.5	19	4 9/32 × 8 × 11 7/8

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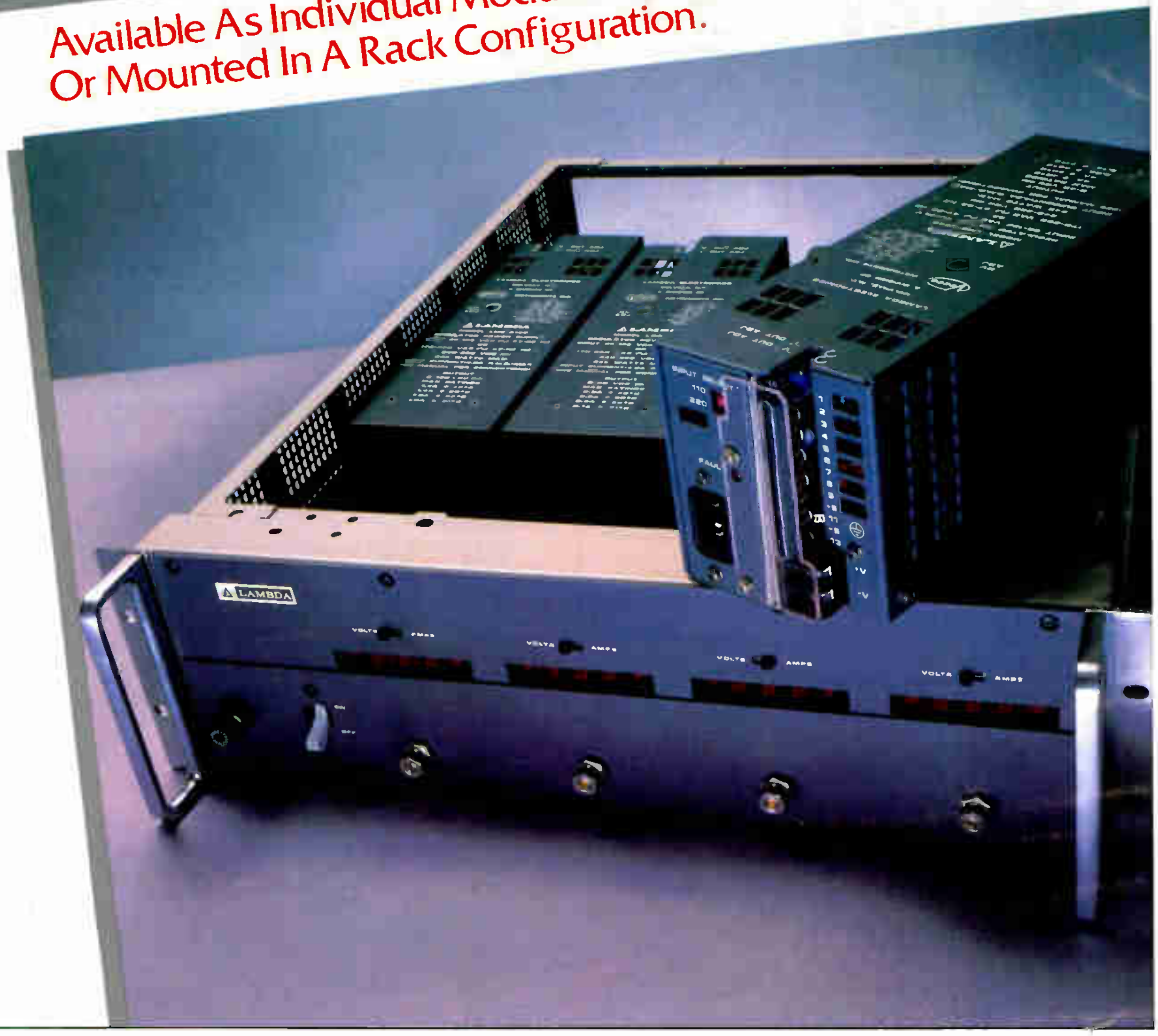

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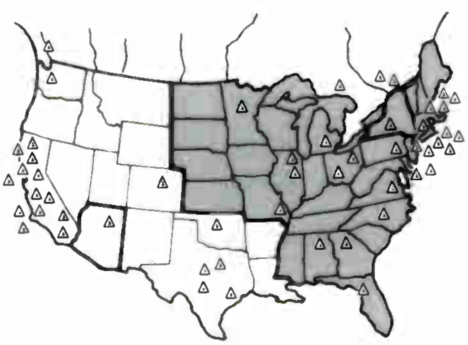

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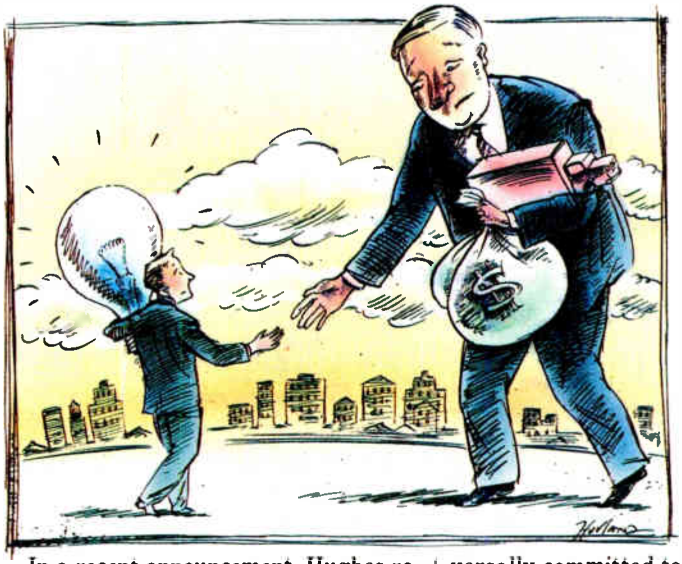
BY JACK SHANDLE

UNITED WE CONNECT

A rash of new partnerships in LANs and WANs is raising hopes that true standards-based multivendor networking may be on the way. The big winner is the customer



Desktop-to-desktop connectivity isn't just a pipe dream anymore. Partnerships and acquisitions among local-area and wide-area networking companies are putting real muscle behind the long-heard call for standards-based, multivendor networking. Simply put, companies smaller than Digital Equipment Corp. and IBM Corp. just can't go it alone in the wide, wide world of global connectivity. "We all have the same strategic plan: to offer complete networking solutions for our customers," says Pradman Kaul, president of Hughes Network Systems in Germantown, Md., one of the world's premier WAN companies.

A number of firms, including Hughes, are teaming up to fill gaps in their corporate offerings. Each deal is unique, but most share three themes. First, TCP/IP—the Transmission Control Protocol/Internet Protocol—is the de facto interoperability standard. Anybody without TCP/IP capability across the board had better get it. Second, network management is the Achilles heel of connectivity. Building in a coherent, powerful, and efficient set of network-management functions requires top-to-bottom cooperation between LAN and WAN vendors. Third, global networks need global sales and service support.

In a recent announcement, Hughes revealed plans to acquire Sytek Inc. of Mountain View, Calif., a leader in large broadband LAN installations. The acquisition follows on the heels of Hewlett-Packard Co.'s teaming with LAN-vendor 3Com Corp. of Santa Clara, Calif., in a sales and marketing partnership. HP runs one of the largest in-house WANs and is aggressively marketing its WAN expertise and products.

Not to be outdone by rival 3Com, the Provo, Utah-based Novell Inc. on March 23 announced a merger with Excelan Inc., a LAN protocol specialist based in San Jose, Calif. Earlier in the year, Excelan forged a marketing partnership with mainframe-to-mainframe networking wizard Network Systems Corp. of Minneapolis, which itself has just unveiled another marketing agreement, this one with Wellfleet, a WAN vendor based in Bedford, Mass.

Although networking companies are universally committed to supporting standards, the partnership trend makes it clear that true standards-based, multivendor connectivity is still in the future. Increasingly, corporate customers have migrated to private WANs to connect their LANs, says Mike Sprayberry, director of integrated network solutions for CAP International, the Norwell, Mass., analysts. But LANs "grew out of the backplane of personal computers and work stations," he says, while WANs were conceived as data bridges between mainframes. This makes interconnecting LANs over a WAN tough.

"In one instance, we found a company that had 13 different network-management systems to deal with when it started to internetwork its LANs," says Bill Way, Network Systems' product-line manager. The solution being sold by the bevy of new partnerships is essentially one-stop shopping at a multivendor store, with service contracts and guarantees that everything will play together. "In these strategic partnerships, they exchange information about proprietary protocols and proprietary network-management schemes," says Sprayberry. "The partnerships wouldn't be needed if Open Systems Interconnect were here today."

A key element in the agreements is getting TCP/IP capability across every possible computer-to-computer interface. Network Systems' LAN II product line, which rebrands Excelan and Wellfleet products, is essentially a TCP/IP-oriented offering, says Way. It melds Network Systems' Hyperchannel bus, connecting mainframes and supercomputers, with Excelan's TCP/IP interfaces to Apple Computer Inc.'s Macintosh, IBM's Personal System/2, and other work stations. Wellfleet adds WAN router products. In return, Wellfleet and Excelan gain access to Network Systems' Fortune 100 customers, otherwise untouchable because of their size.

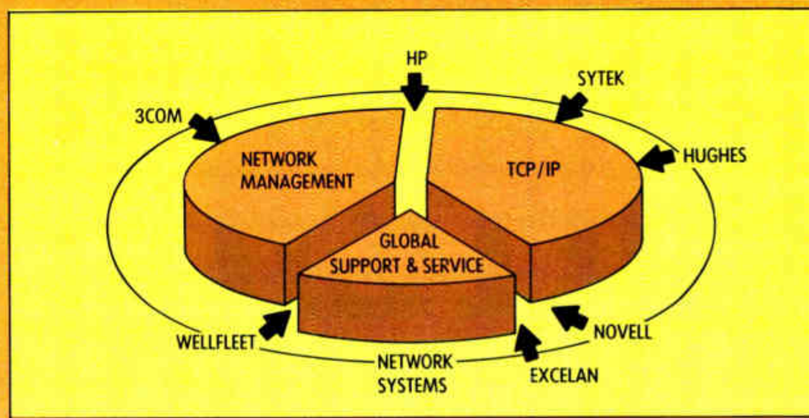
DISTRIBUTED COMPUTING. TCP/IP is also important in the HP-3Com deal, in which HP gets a 5% stake in 3Com. "The strategy is to provide distributed computing solutions to customers as soon as possible," says Ormond Rankin, HP's product marketing manager for PC networks. The Palo Alto, Calif., company can move into the low end at a much faster rate through the partnership, he says. Ultimately, computers running DOS, OS/2, or Unix will network transparently using 3Com and HP computers and software.

The two partners will back Microsoft Corp.'s LAN Manager software as a network-management standard. This is no surprise—LAN Manager was jointly developed by 3Com and the Redmond, Wash., software giant for PCs, and HP is codeveloping a LAN Manager/X product with Microsoft for Unix and Xenix. The extensions of LAN Manager are just as important. HP will use 3Com's 3+Open for OS/2 systems as the basis for its LAN Manager 3+Open OS/2 offering. To tie everything together, HP and 3Com are codeveloping a common TCP/IP protocol. They are also codeveloping the next version of HP's OpenView architecture based on TCP/IP and OSI network-management standards.

TCP/IP played a role, too, in Hughes's decision to acquire Sytek. Multiple protocol support is one of Sytek's strengths, says Phil Edholm, director of marketing. Besides TCP/IP, this includes DECnet, IBM's SNA, and, ultimately, OSI.

For Sytek, which will become Hughes's LAN Systems Division after the merger, network management will be a key selling point to clients. Sytek's network-management software offers advanced network-configuration capabilities, access control, and high-level performance management, Edholm says. Although the new division will put the TCP/IP-based Simple Network Management Protocol on all its products—and support OSI's

SOLVING THE CONNECTIVITY PUZZLE



Recent alliances among the companies shown here revolve around the same aims: acquiring TCP/IP capability, a network-management scheme, and worldwide customer service.

Common Management Interface Protocol when it becomes available—Edholm says the value added to standard protocols is proprietary, and that makes the difference in performance.

"If we control the entire [data] path," Edholm says, "we can build in the network-management tools along the way." Standards without added value limit performance, he says. "You can knit together various network-management systems under OSI, but you still can't move all the information you need up and down the network, because the systems don't collect the same information."

Network management is the Achilles heel of desktop-to-desktop nets; building it requires multivendor cooperation

Network management is indeed critical—and almost impossible to achieve, says analyst Sprayberry. "If you sat down and put the number of network-management systems used in nodal processors [in WANs] on one axis and the number of systems on LANs on the other axis, you would have a very large matrix," he says. "For one nodal processor to work with all the LANs would take an enormous overhead in computing power."

Global service and support—the third factor in the recent spate of partnerships—is a simple acknowledgment that global systems don't run themselves. For the smaller companies, such as Excelan and Wellfleet, a deal can open new distribution channels. "It's a matter of buying behavior," says Bill Siefert, Wellfleet's vice president for advanced engineering. "Large customers restrict the number of vendors with which they do business by insisting on strict service and support, and that's a group of customers a little startup can't approach alone."

OPENING DOORS. But Network Systems "has been around as long as local networking has existed as a term," Siefert says. "And since they operate at the very high end they have many customers in the Fortune 100 category, and that opens many doors for us."

HP, too, is legendary for its service operations, and that's a plus for 3Com. The HP-3Com agreement stipulates that HP will provide worldwide support for 3Com workgroup products. Specifically, HP customers will be able to obtain service for their HP and 3Com computer and network systems under one contract.

Global service was not a high-profile issue in the Hughes-Sytek merger because Sytek operates at the high end of the LAN spectrum. Many of its customers fall in the same Fortune 100 group that demands on-site service. Hughes also has extensive service capabilities, but not on customer premises. Instead, it maintains a large and growing network of very small aperture terminal satellites along with a large terrestrial packet-switching network. "That combination makes Hughes the largest WAN vendor in the world," says Edholm.

In the world of LANs and WANs, the merger and partnership beat is on. Prior to the most recent groupings, Tandem Computers Inc. of Cupertino, Calif., acquired networking specialist Ungermann-Bass Inc. of Santa Clara, and Bridge Communications Inc. of Mountain View had merged into 3Com. "You'll see more consolidation over the next three or four years," says Hughes's Kaul. "Customers want one-stop shopping." □

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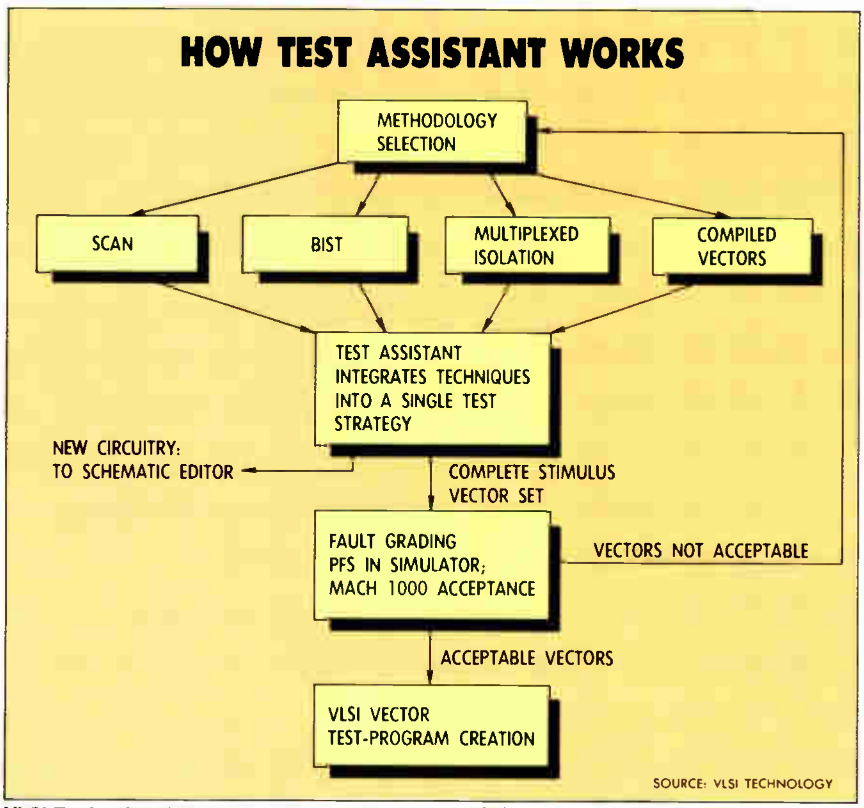
HERE'S AN EASY WAY TO TEST ASICs

VLSI Technology's new tool cuts the time and effort needed to get 95% fault coverage on any cell-based ASIC design



VLSI Technology's Test Assistant evaluates an ASIC design block by block, automatically producing the circuits needed to connect the blocks to the chip's I/O pads.

Testing is the bane of application-specific integrated-circuit design, and as chip complexity rises test-program development is accounting for as much as 50% of the total ASIC design time. The reason: the relationship among gate count, input/output pins, and the number of test vectors needed to achieve 95% or higher fault coverage, says G. Dan Hutcheson, president of VLSI Research Inc., the San Jose, Calif., market-research firm.

"As gate count goes up, the number of I/O pins go up by the square root of the number of gates," Hutcheson says. "The number of test vectors to achieve near 100% fault coverage is equal to 2 raised to the *n*th power, where *n* is the number of inputs."

To the rescue comes VLSI Technology Inc. with the Test Assistant. This new tool, which the San Jose semiconductor maker uses in its own foundry, neatly trims the time needed to achieve 95% fault coverage or higher on any cell-based ASIC design of any degree of complexity, the company says.

Test Assistant automatically inserts the additional circuits needed to increase the fault coverage to 95% or more with little effort on the part of the designer, says Jeff Lewis, product manager for simulation and test at VLSI Technology. And it does it in just a day or less, he says. The tool runs on Apollo Computer Inc. work stations and costs $35,000. It will be generally available in July.

HOW IT WORKS. The Test Assistant performs four tasks. Automatically or in concert with the designer, it develops programs to test each block that goes into a larger ASIC design. With no designer input, the tool produces the circuits that must be added to each block to isolate them from one another and to connect them to the ASIC's I/O pads. It also creates the control circuit that switches each block in turn to the I/O pads for testing. Finally, when the designer tells it to, Test Assistant compiles and installs built-in self-test circuits to evaluate individual blocks, especially memory and other compiled cells.

"Isolating blocks and testing each individually is one easy way of getting around the two-to-the-*n*th increase in test vectors," says Hutcheson. The complexity of the individual block is lower than that of the ASIC as a whole. And since the number of I/O pins is proportionately less, fewer test vectors are required. In addition, partitioning takes the least amount of silicon real estate, according to Hutcheson.

Blocks in a large ASIC design come in

By Jonah McLeod

three different forms. There are large blocks, such as the microprocessor cores found in a foundry's ASIC library; compiled cells, such as random-access and read-only memories, and programmable logic arrays; and semicustom blocks containing logic the designer has created with standard cells.

For the large microprocessor-type library cells, VLSI Technology provides a comprehensive set of test vectors for 95% fault coverage. The silicon compiler that produces a ROM, RAM, or PLA produces all the test vectors needed to provide this same level of fault coverage for those blocks. Lewis says that if a designer builds an ASIC with just these two types of big blocks, Test Assistant's wiring and testing procedure will be fully automatic and fault coverage of 95% or higher will be assured. However, for a semicustom block made up of standard cells, the designer does have to perform some test-program development.

To use the tool, the designer first gives the Test Assistant the netlist of the ASIC for which a test program is to be developed. From a block-level representation of the design, he selects the first block to be isolated, and the tool shows how it will route the block's I/O pins to the ASIC.

In the isolation phase, the tool installs multiplexers at the block's I/O pins to switch them out of the normal signal-flow path and route them to the ASIC's I/O pads. A rule that the tool adheres to is not to insert more than one level of multiplexer between the block's I/O pin and its internal circuit. This ensures that the test circuits do not affect the timing in the ASIC's critical paths.

INTERACTION. At any point in the tool's operation, the designer can interact with Test Assistant to change the implementation manually. For example, the operator can direct the tool not to multiplex certain ASIC I/O pads that lie in a critical path. If this restriction means there will not be enough I/O pads to access the I/O pins of internal blocks, Test Assistant can change any pad specified as output-only into a bidirectional pad to attain the additional number required.

If the designer accepts the tool's proposed isolation and signal routing, Test Assistant automatically changes the netlist to incorporate the test circuits.

Thereafter the process is repeated with all the other blocks. Besides isolating and wiring, the tool also creates the control circuit needed to configure the ASIC in test mode and to switch each individual block to the I/O pads for testing. It adds this circuit into free space on the ASIC and routes the test-signal wiring between the control unit and each block.

To activate the test circuit, the designer can specify a vector that, when applied to the ASIC's I/O pads, switches the test circuit on. Using a vector eliminates the need to use an I/O pad to switch the test circuit on and off. With the test circuit turned on, each block can be individually switched. At the I/O pads, a component test system can send stimulus into and measure responses from the block.

To create test programs for a semicustom block, the designer typically produces test vectors using simulation vectors developed in the design phase along with vectors written later to increase fault coverage. He also performs a fault simulation to determine if the desired fault coverage has been achieved. Once the test program is developed, Test Assistant isolates and reroutes the semicustom block's I/O pins to the ASIC in the same way it handled the other blocks.

One important function of Test Assistant is its built-in self-test (BIST) capability. The designer can direct the tool to add a linear feedback shift register to the input and output of a compiled block. At the input, the circuit serves as an autonomous pseudo-random pattern generator, while at the output, it acts as a signature analyzer. This is particularly attractive for highly regular compiled RAM and ROM blocks.

"Built-in self-test puts a tester on the chip," Hutcheson says. "It facilitates the device tester's job during production, thus cutting test time." It also facilitates field service, he says, "since the service technician has instruments on-chip to help diagnose a field failure."

In the compiled RAM or ROM block, the compiler can add the signal generator and signature analyzer so that the resulting BIST produces a 1-bit pass or fail indication to one of the ASIC's output pins. Alternatively, the designer can route the block's output pins to the ASIC's I/O pins for analysis by the device tester.

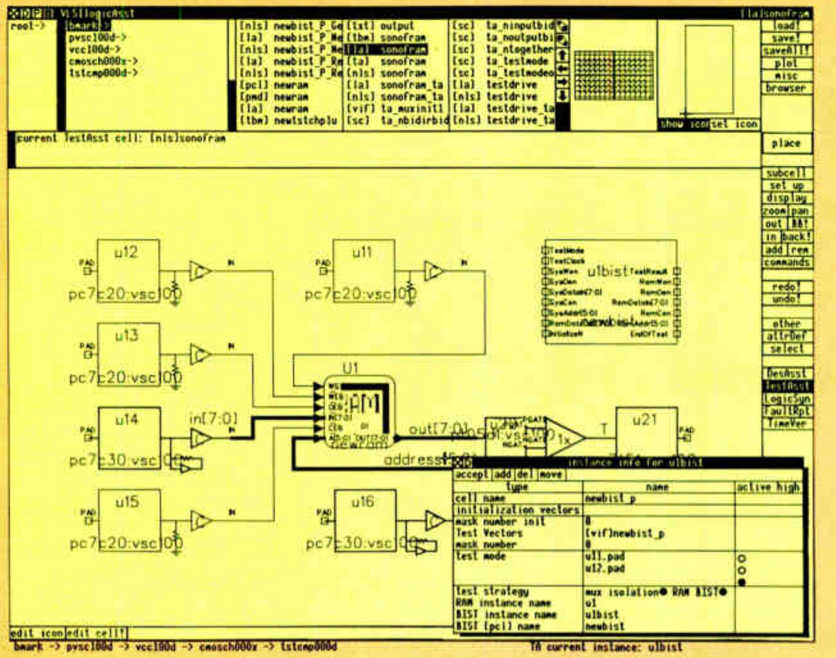
Self-test can also be used on a semicustom block. Here, the designer adds the signal generator and then simulates the operation of the circuit with the pattern generator installed to determine if all the nodes in the design are being tested and if the pattern actually catches each possible fault node.

Because the generator produces the same sequence of random patterns each time it runs, using the linear feedback shift register, the designer can create a circuit that performs an X-NOR logic operation on the responses received from the block. The result is a signature that indicates the block is good or bad. The entire signature can be sent to the ASIC I/O pads for verification.

In the future, the Test Assistant will be able to add level-sensitive scan design to blocks within a chip as an alternative to isolation, VLSI Technology says. Instead of bringing signals to the ASIC I/O pads, it will serially shift test vectors to hidden nodes within the ASIC, stimulate the hard-to-access circuit behind the hidden node, and serially shift the results back to the ASIC I/O pads.

With this powerful tool to drastically cut the time needed to write an exhaustive test program, designers can get back to spending most of their time designing chips rather than worrying about how to test them. □

TEST ASSISTANT TAKES ON A 'MEGOCHIP'



In testing a hypothetical "megochip," the tool can add a built-in self-test (BIST) block upon the designer's command; to do so, the user simply fills out a three-line menu.

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TROUBLE IS BREWING OVER CFCs IN CALIFORNIA

The AEA calls one proposal a potential 'disaster'

To John Masterman, it seems only natural that the state of California emerge as a proving ground for legislative efforts to curtail the use of ozone-destroying chlorofluorocarbons. "California continues to be the birthplace of [environmental] laws," observes Masterman, chairman of the American Electronics Association's California Environmental-Occupational Hazards (EOH) Legislative Committee.

Any laws enacted by California concerning CFC use are likely to have a tremendous impact on the U. S. electronics industry, which uses CFCs in the manufacture of a wide range of products [*Electronics*, April 1989, p. 92]. The California state senate is pondering a proposal to rein in CFC use even more severely than has been called for by international guidelines. The proposal pretty well reflects the regulatory mood in the Golden State and perhaps offers electronics manufacturers everywhere a picture of the difficulties and bureaucratic confusion that the future holds for them.

The action in California also illustrates the problems that a trade organization like the AEA faces when it gets a late start in its lobbying efforts. Masterman concedes that the AEA is getting into the environmental hazards game on the state level relatively late. Although the AEA tracks environmental affairs from its Washington headquarters, the scene in California is a hyperactive arena in which the big organization has not played a part for nearly five years.

The AEA is alarmed by the California CFC initiative. If the measure passes in its present form, California's Air Resources Board essentially would gain the power to manage every application for which CFCs could be used. It could determine whether substitutes exist and then mandate their use. The degree of control and the opportunity for error appall Masterman. "It's a bad law that could be a disaster," he says.

Masterman's committee is now working to avert that disaster. It has already had an impact on getting some proposed environmental bills apart from the CFC arena changed before they became state law. One of these would have banned any use of arsine and phosphine gases—both widely employed in electronics manufacturing—within 25 miles of any residence. In its original form, the proposal "would have wiped out the electronics industry," Masterman asserts. Partly through the AEA's efforts, the proposal was changed to bar only the manufacture of arsine and phosphine gases, not their use.

In Masterman's view, the proposed Toxic Gas Model Ordinance for Santa Clara County (Silicon Valley) is a model for how environmental legislation should be approached. The proposal, the product of three major groups that sat down and hammered out an approach acceptable to all, offers a method of assessing the hazard of every toxic gas and providing safeguards for each of them.

Meanwhile, the AEA last November launched a big effort to get what it deems both a balanced outlook and solid technical data to legislators on a continuous basis. Masterman, who is director of health, safety, and environmental affairs for Intel Corp. in Folsom, Calif., notes that the AEA's move into the EOH game from an inactive status requires diplomacy and a deliberate pace, due to the emotionally charged nature of the subject.

by Larry Waller

The AEA legislative committee, with some 20 companies currently taking part, meets monthly at different locations throughout the state. Plans are afoot to raise funds for a full-time lobbyist in the state capital at Sacramento to monitor legislative doings.

Masterman's committee is likely to have a wider role in the CFC battle than individual AEA member companies in California. Since they lack any other central clearinghouse or sounding board for their environmental interests, companies by themselves are hard put to deal with escalating regulatory and reporting requirements from all levels of government.

Their greatest headache lies in the staggering number of requirements—many of them overlapping—to be met and the range of official bodies overseeing them. A company typically has to deal with about 10 entities, from the federal Environmental Protection Agency through state and regional regulatory groups, right on down to local fire and safety departments and sewer and water districts.

Companies say their chief need is getting up-to-date information about new requirements and how to handle them. "There is no magic wand to bring you into easy compliance with these ever-shifting regulations," says Edwin K. Isely, manager of the Los Angeles office of A. T. Kearney Inc., management consultants with an extensive environmental consulting practice. Instead, companies have to seek these answers for themselves.

Isely and Masterman both advise executives in California to get involved with state and local organizations that are up to speed on environmental issues, particularly the California Manufacturing Association and chambers of commerce. "Stay in touch with your local organizations," says Masterman. "You can't monitor [the issues] by yourself. It's a noble goal, but no one can afford it." □

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month technology lead over competitors proved to be more like two years.

Hutcheson, who is president of San Jose, Calif.-based VLSI Research, points out another edge exploited by Teradyne in Japan. Both of its main competitors, Ando and market leader Advantest, are allied with a giant vertically integrated chip combine—Ando with NEC Corp. and Advantest with Fujitsu Ltd. So other Japanese chip makers can diplomatically avoid offending either by picking Teradyne, and justify the decision on the basis of its technology lead. Hitachi, Mitsubishi—and even NEC—are customers.

But Teradyne is not resting on its laurels. It's rounding out the J937 into a series that offers software compatibility from the low-cost 30-MHz version through the new 100-MHz unit now being shipped for the first time. Multiple orders are being received for both, says division vice president and manager Ed Rogas. And a decision is imminent on whether to develop yet another generation of testers that can handle the ever-increasing density and speed of next-generation DRAMs.

For all the inroads made into Japan, Teradyne still trails Advantest as a memory-tester supplier there, notes Rogas. He hopes to improve market position even more, to match that in the U. S and Europe, where "we clearly are the leaders." *–Larry Waller*

DISTRIBUTION

HOW SAI IS BECOMING A NATIONAL REGIONAL

MELVILLE, N. Y.

Telemarketing is not the first sales tool to flash to mind when thinking of electronics distributors, where the top 10 thoroughbreds run with gaudier colors. But Semispecialists of America Inc. is using telemarketing to break out of the pack and will continue to make calls as it installs a new corporate strategy.

The aim is to cover North America yet retain a regional focus

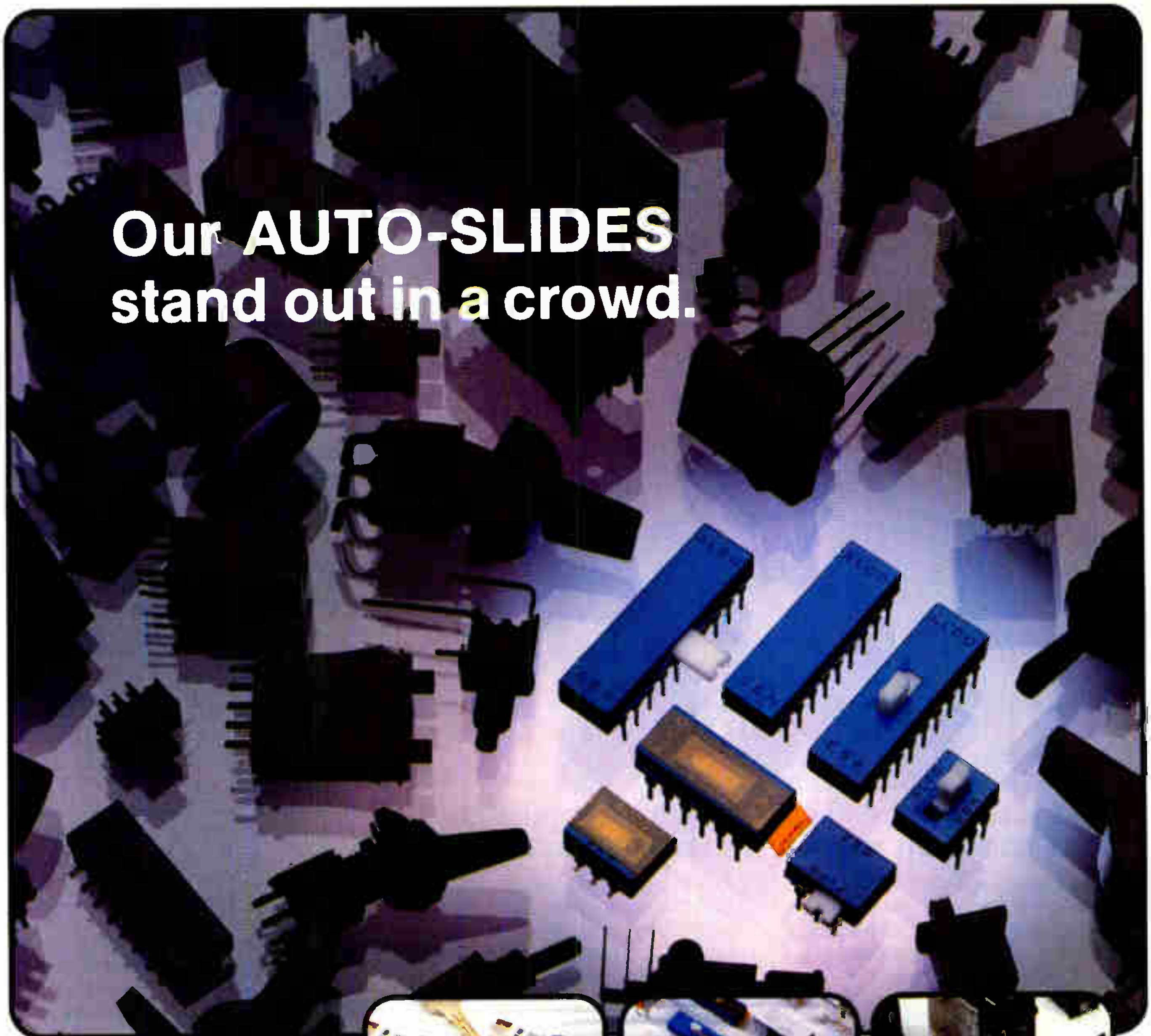
From 40th place in gross sales for 1981, the privately owned Melville distributor finished 12th in 1988 with $160 million in sales. In volume, that still leaves it way behind market leader Hamilton-Avnet Electronics' near $1 billion. Semispecialists wants to narrow that gap by fostering its success as a regional distributor into a national presence.

The 15-year-old company is positioning itself as a "national [firm] with a difference," says Jeff Curlander, vice president for corporate operations. The aim is to cover North America while keeping a regional focus, which means the company is selectively choosing which regions it stakes out. The people managing these regional operations will do so with a high degree of autonomy.

Telemarketing—which is known in the distribution community as "purchasing service"—will remain a key sales tactic in the company's growth plans. "That's how we started the business," says Curlander, "and we're the best in the world at it."

Telemarketing simply means calling customers, finding out what they need, and buying it for them. This lets the distributor sell products—both components and systems—for which it does not have a franchise, and it also gives the customer the benefits of one-stop shopping. Semispecialists' telemarketing effort will be centralized in Melville as a means of keeping overhead at a minimum.

Management, on the other hand, is being decentralized. Vice presidents in charge of a region will live there and run



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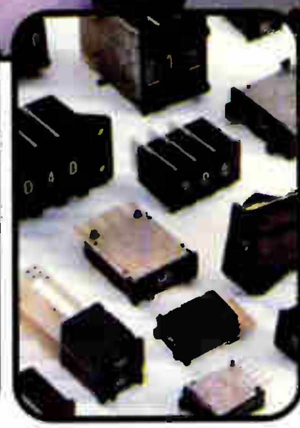

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Circle 3

the ship, even to the point of deciding which franchised lines they will carry. A franchise for the Dallas branch may not be aggressively marketed in the Boston area. "Every region will have a different product mix," says Curlander. "I don't think anybody else has approached the market that way. We don't want competing lines in any one region."

The concept of being a national distributor with a regional focus grew largely out of the company's "share-of-mind" concept, which Curlander explains as the attention a distributor's salesperson can give to any one product line he or she represents. In short, a sales force does best when it knows the products it represents, and a salesperson with a manageable portfolio can give each product line greater attention, or share of mind. "National distributors have lost focus and commitment to mature product lines such as TTL," says Curlander. "Their salespeople have too many masters to serve—too many vendors and too small a mind share for any one of them—yet they're always adding more lines."

Not everyone concurs with the company's strategy of selectivity on vendors. While agreeing that "a salesperson can't do 75 or 100 accounts justice," Steve McGill, vice president for national sales at Scheweber/Lex Inc. in nearby Westbury, N. Y., believes that a broad product line is still necessary for success in the distribution business.

The real issue, he says, is in user-ready services. "Customers want services like kitting, packaged solutions, and value-added engineering. It helps to be a broad-line distributor, because those services require a broad base of suppliers." For example, McGill says, "about 90% of the parts you put in a kit must come from franchises for you to have any hope of being able to ship on time."

As the industry grapples with the pros and cons of regional versus national distribution, it remains clear that customers perceive these two groups as having strikingly different strengths and weaknesses. One customer survey gives nationals high marks in pricing, where 55% see them as having an advantage over regionals. Nationals also scored high in availability of obsolete parts, where 57% give them the nod, and depth of inventory, where 60% see them as substantially better than their regional confreres.

SERVICE ADVANTAGE. The regionals clobber the nationals, however, in service. On-time delivery is rated by 79% of the respondents as a reason to use a regional distributor. "Understanding purchasing needs" impresses 77% of them as an advantage of using a regional. "Regional distributors have been profitable for one reason," says Curlander. "Their salespeople have better focus and less overlap of product lines."

Currently, Semispecialists has eight branch locations and two regional support centers, all added in 1988; it will expand to 17 branches over the next couple of years. Those 17 were chosen from a generally recognized total of 30 major metropolitan markets, says Curlander. Although they represent just a little more than half the markets, the 17 make up 88% of the total distribution resale market in dollars. Left out of the plan are less important cities such as Pittsburgh, Cleveland, and Detroit.

The company's two major warehouses are in the Melville headquarters and in Sunnyvale, Calif. Readily available overnight delivery service plus efficient transportation between major metropolitan centers, says Curlander, make on-site warehousing expensive. Branches with minimal warehousing are in Altamonte, Fla.; Atlanta; Dallas; Irvine, Calif.; Rutland, Vt.; Toronto; Wallingford, Conn.; and Wilmington, Mass. *–Jack Shandle*

Circle 200

PEOPLE TO WATCH

AT&T'S KOELTL SAVORS THE CHALLENGE OF TAKING ON MERCHANT CHIP GIANTS

His strategy is based on partnerships with customers, alliances with rivals

BERKELEY HEIGHTS, N. J.

As a young engineer fresh out of New York's Manhattan College and looking for adventure, Dick Koeltl had an important decision to make: would he specialize in locomotives or semiconductors?

Semiconductors—the technology was called "solid-state" back in 1964—won the battle. Koeltl's 25-year odyssey through power integrated circuits, analog-to-digital converters, telecommunications chips, and linear ICs in companies as legendary in the chip business as Advanced Micro Devices, General Electric, Fairchild, and Raytheon was a near-perfect training ground for his new job as AT&T Microelectronics' marketing czar.

"There is all this technological capability here, and for a marketeer, that has to be an exciting prospect," Koeltl says. "Despite its technology, up until now AT&T Co. has not been known for strong marketing."

From a modern, spacious office overlooking the rolling green hills of rural central New Jersey in Berkeley Heights, Koeltl is not that far removed geographically from his cadet days in General Electric Co.'s engineer-in-training program in Schenectady, N. Y. "When I came on with GE," he says, "they had five separate businesses—everything from locomotives to semiconductors. When I got to the semiconductor division, the people all around me were in their 20s. It was obviously a dynamic, growing business."

Infusing more dynamism and growth into AT&T Microelectronics has been at the top of Koeltl's docket since he arrived six months ago to become marketing vice president, fresh from a similar job at GE Intersil. AT&T Microelectronics sells 25% of its ICs in external sales; the rest go to AT&T's various systems divisions.

AT&T's aim is to do more than $1 billion in external sales by 1992, and that means over 50% of its business will be in the merchant market, says Koeltl. If it happens, AT&T Microelectronics would be playing in the major leagues with the likes of Fujitsu, Intel, National, NEC, and Texas Instruments.

The strategy is to get AT&T Microelectronics out of the marketing closet by becoming partners—with customers, and via strategic marketing alliances with competitors. Such partnerships with system-house customers aren't new. Companies like IBM Corp. and Intel Corp. have been pretty successful at it, with Intel producing microprocessors for IBM's personal computers and Personal System/2.

"We're looking at specific markets for equipment segments that fit well with our technologies," say Koeltl. AT&T is "well into" talks with "two or three" major system houses and will be unfurling the agreements as early as the next six to twelve months. Although Koeltl is coy about naming the prospective corporate brides-to-be, he describes them as being in the data-processing, telecommunications, and military markets. "We're looking for major potential markets where we can codevelop technology," he says. One recent example: high-definition TV and Zenith Electronics Corp.

On the competitors' side, AT&T Microelectronics has already teamed up with Intel to exchange technology in areas where product lines are complementary. The agreement is complex, but it boils down to Intel contributing local-area-networking chips and AT&T pitching in its expertise in integrated services digital network chips.

Dick Koeltl's goal is to continue to double AT&T Microelectronics' sales in the merchant market, now at $200 million, each year.

Another prime growth area for AT&T is in better utilization of its silicon foundry capacity. AT&T and Logic Devices Inc. have signed a foundry agreement committing Logic Devices to purchase up to $75 million worth of finished silicon wafers over the next three years.

Aggressively second-sourcing standard parts is also in the cards, "and you'll see results in that arena over the next few months," says Koeltl. "We've got plenty of opportunities to fill out our standard-parts offering." Lastly, price reductions—once seldom heard words in Berkeley Heights—will liven up the company's marketing blitz. AT&T has already slashed the price of its high-performance digital signal processor, the DSP32, by almost 50% thanks to a new plastic-packaged version.

Obviously enjoying the prospect of butting heads with the giant merchant chip makers on three continents, Koeltl talks with exuberance. His selection as head of marketing was atypical for AT&T, which usually promotes from within. "To do over $1 billion business in merchant sales by 1992 means you have to have a world-class marketing organization," he says. Koeltl promises to import more whiz kids from outside to shake up the telecom giant's somnolent posture. Also, "We're going to become much more applications-oriented. Instead of just chips and technology, we're going to show customers solutions," he says.

Not surprisingly, Koeltl thinks AT&T Microelectronics can blast into the top tier of merchant chip vendors. "Between 1987 and 1988, we doubled merchant sales and we're up in the $200 million range now. We've doubled sales each year for the past few years. To continue that pace we have to keep offering customers more solutions," he says, adding that "each doubling step gets bigger"—and harder, too. *–Jack Shandle*

APITZ: THE NEW WAVE IN EAST GERMANY

LEIPZIG, EAST GERMANY

In a sense, Jürgen Apitz is a revolutionary. The new director general of East Germany's VEB Kombinat Nachrichtenelektronik—the country's 37,000-worker combine for communications electronics—wants to change what has been a staid, protected, and bureaucracy-ridden organization into a dynamic, hard-hitting unit that can compete profitably in the world marketplace.

It's too early to tell whether Apitz can forge his combine into a productive, efficient, and innovative organization. But the young executive strikes people as a doer, as one of a new breed of East Germans who are determined to move the country ahead on world markets.

The combine, based in East Berlin, unites nearly all East German activities in communications. It operates 18 production facilities and one research institute and is active in a wide range of technologies—everything from exchange systems, transmission equipment, and terminals to studio gear, instruments, and medical electronics.

In recent years, the combine's sales have risen from 3% to 5% annually, reaching about $2 billion in 1988. Roughly 40% of its output goes abroad, with sales to the Soviet Union accounting for almost two thirds of the total exports.

Exports are the lifeblood of the East German economy; they account for about half of the nation's gross national product. East Germany needs a strong export market because it is small—about the size of Kansas, with only 17 million people as a potential domestic market. More important, the country has virtually no mineral resources and therefore needs cash to import raw materials.

To increase exports, Apitz is turning his attention westward. Countries outside the Soviet sphere currently account for only about 10% of the combine's foreign sales. To boost sales to the West, the combine must meet three formidable challenges: it must streamline operations, increase productivity, and raise product quality to international standards.

Apitz, who at the age of 40 is one of the youngest leaders of an East German industry combine, insists that the challenges can be met. He dismisses the West's contention that East Germany is reluctant to change.

"For many years, a process has been under way to give our industrial organizations more self-responsibility," he says. Apitz maintains that this process has already led to more efficient and productive combines that have begun to do substantial business even in Western countries. He singles out VEB Carl Zeiss Jena, the

big optics and electronics producer, as a case in point. Of course, government planning will remain a bedrock element of East Germany's economic policy. But the bureaucratic strings are being loosened, giving the combines more leeway to run largely on their own and strive for what East German officials call financial gains—"profits" is still too capitalistic a word for most officials.

In some ways, the efforts of Apitz and like-minded colleagues resemble a form of East German economic *perestroika*—although that term was seldom heard from industry officials at this spring's Leipzig Fair, where VEB Kombinat Nachrichtenelektronik displayed its wares. East Germans prefer to describe the changes as *wirtschaftliche Rechnungsführung*, which, roughly translated, means an economic accounting of balances. Among other things, this concept permits a combine to invest part of its financial gains in its own operations.

GLOBAL NEEDS. Apitz doesn't think the combine's heavy exports to countries in Eastern Europe and the Third World, which are less demanding technologically, will keep it from making high-quality products that satisfy global needs. "The existing concept [for exports] calls for cooperation on a Comecon-wide scale," Apitz says. (Comecon—the Council for Mutual Economic Assistance—is Eastern Europe's equivalent of Western Europe's Common Market.)

Jürgen Apitz is determined to market his combine's telecom technology in the West.

"But we want to increase sales in Western countries, so we must increase capacity and develop a technological base to meet global requirements." In the face of international competition, Apitz adds, "we are forced to stay on a par with other industrialized countries to advance our society, help meet the needs of our home market, and maintain a high export rate."

Apitz is counting on a series of cooperative efforts to help boost his combine's status in the West. The combine has struck a deal with Intracom in Greece involving exchange and transmission equipment. A similar deal is being discussed with Telindus, a Belgian communications equipment maker. And preliminary talks concerning joint projects in other countries have been held with Siemens AG of Munich.

Apitz is the prototypical production man—amiable but forceful and quick of mind. He was trained as a tool and die maker, studied general engineering at the Technical University in Karl-Marx-Stadt, and then worked as a technologist in the plastics industry. Ten years ago he moved into electronics and worked for most of the time as production manager in an instruments factory before being put in charge of VEB Kombinat Nachrichtenelektronik.

The technological challenge Apitz faces is to move his combine from the analog to the digital era and into the age of integrated services digital networks. One of the first results of this effort is the NZ400D, a private-branch exchange for speech, data, and text that features ISDN characteristics. The combine displayed the product at the Leipzig Fair. If Apitz successfully administers the transition to ISDN and turns his organization into an efficient and profitable unit, he will indeed be a true revolutionary in East German electronics. *–John Gosch*

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SKATES: PUTTING DATA GENERAL BACK ON TRACK

WESTBORO, MASS.

The title is a new one for Data General Corp.—executive vice president and chief operating officer. And it's a new one for the man who carries it, Ronald L. Skates. Though he has worked for the big computer maker for less than three years, he is already settling into his role as the right-hand man to the founder, Edson de Castro. Most other senior managers report to him in his new position.

Skates, who took on responsibility for day-to-day operations after giving up his post as senior vice president for finance and administration, in turn reports directly to de Castro. "It's almost a classic U. S. business organization," Skates says. "I'm his only direct reporter, but he's the boss." He adds that the restructuring may be two to three years overdue, "but it didn't happen earlier because the company was on a roll. Few organizations make such changes when they're growing 40% a year."

But after the roll came the rock. Beginning in 1986, Data General's growth slowed, and the company suffered three losing years in a row. It also sustained a $19.5 million loss in the first quarter of this year. But this losing streak may be coming to an end. Significantly, Skates has taken over de Castro's traditional role of explaining financial results. Both say the firm should return to profitability in fiscal 1989, ending in October.

OPTIMISM. Some of the optimism in Westboro these days results from a revamped strategic plan that has three major thrusts: continuing to upgrade the proprietary MV/Eclipse computer line; launching a major initiative in open systems, especially reduced-instruction-set Unix platforms; and making a move into telecommunications and networking.

The first evidence of the telecom initiative was a contract late in 1987 with Japan's NTT Corp. calling for Data General to deliver hardware and software for NTT's private data networks. And Data General unveiled its first RISC work stations in late February.

Skates, a certified public accountant, says he's had a long-standing relationship with Data General from his days at New York-based Price Waterhouse, where Data General was a client. He spent 20 years at the accounting firm and became a partner. "I always liked Data General in those days, and I became familiar with computers and computer companies from auditing them." But he wasn't content to remain strictly a bean counter at Data General. "I've always wanted to be operations-oriented," he says.

Part of Skates's aim at Data General is to "bring a stronger sales and marketing focus to the company. The knock on us is that we have great products but don't seem to be able to sell them well. The focus has been on technology and building a better product so people will beat a path to our door—but that doesn't work anymore," he says. *–Lawrence Curran*

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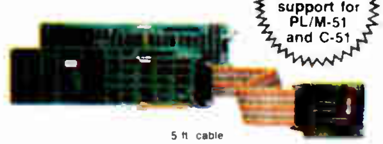

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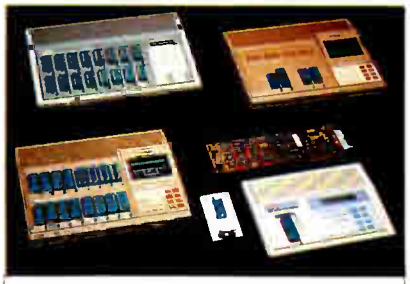

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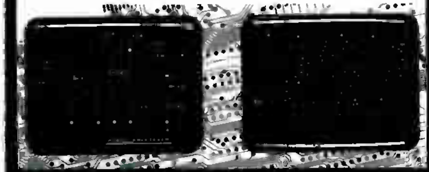

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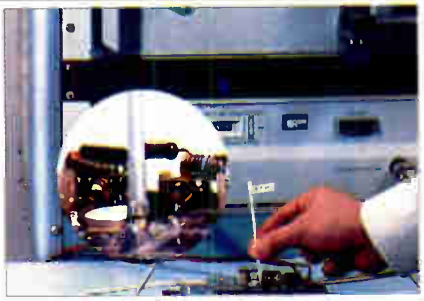

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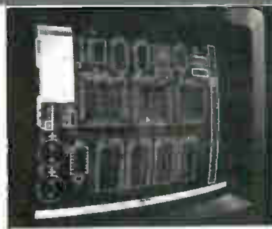

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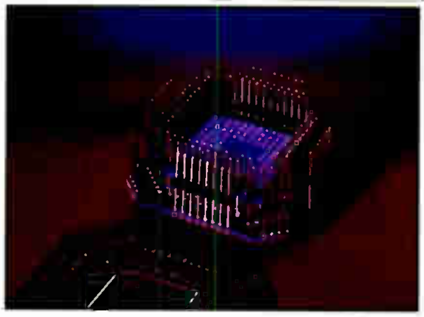

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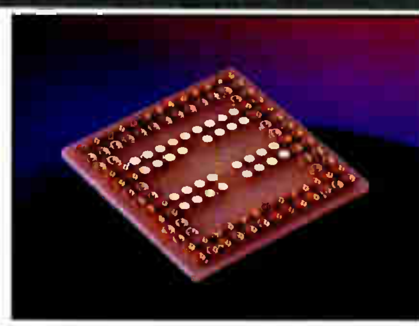

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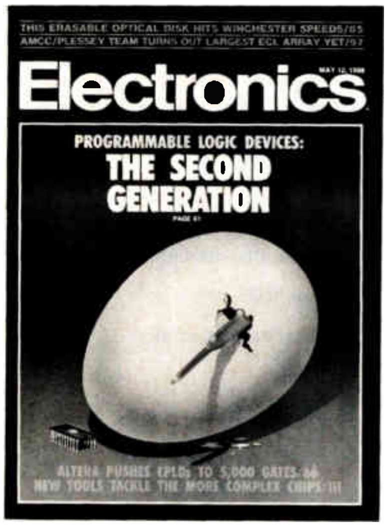
UPDATE: IN PLDs, IT'S A MAD, MAD, MAD, MAD WORLD

Some technologies have a rhythm all their own when it comes to cycles of significant advances and announcements. For memories, the cycle is about two years; for microprocessors, it's about one. But for programmable logic devices, the cycle seems to be a quarter—or even a month.

In the 12 months since the last *Electronics* survey of the PLD market [*Electronics*, May 12, 1988, p. 61], activity has continued at a hot and heavy pace. Current estimates hold that worldwide sales of PLDs will top the $1 billion mark this year, up from $500 million in 1987. The number of players is increasing; 19 companies (16 U. S., one European, one Japanese, and one Korean) are now in the market, and at least two other Japanese firms plan to enter soon.



Sales will top $1 billion this year, and the number of players is increasing

One of the most active companies is Altera Corp. of Santa Clara, Calif., which has been seeking to protect its 20%-to-30% share of the CMOS erasable PLD market. In May 1988, Altera announced the first in a new family of high-density multiple-array-matrix PLDs, initially fabricated by Cypress Semiconductor Corp. of San Jose, Calif. The first device—the EPM5032—was followed by the debut in January of the EM5128, with 68 pins, 128 macrocells, and 5,000 gates.

Since then, Altera has filled out its new family with 24- and 64-macrocell versions, plus a software package for designing with the devices. And it's adding faster CMOS versions to its lower-density line of EPLDs to give bipolar PLDs a run for their money. One such part is the EP1800, which at 35 ns is 50% faster than its earlier implementation.

Altera's activity hasn't been limited to product announcements. Last July, the company entered into a seven-year strategic alliance with Texas Instruments Inc., exchanging its EPLD hardware and software technology for the use of TI's high-voltage EPIC CMOS manufacturing process. In January, TI entered the CMOS EPLD market with the first results of this pact: direct second-source versions of Altera's 600-gate EP610 and 900-gate EP910 devices. The parts boast speeds ranging from 25 to 40 ns. On the bipolar side, TI in January introduced the TIBPAD18N8-6, a 6-ns programmable address decoder.

Also looking to the high-density end of the market, TI has entered into a strategic alliance with Actel Corp. of Sunnyvale, Calif., which last July introduced the first in its Act-1 line. These antifuse-based channeled arrays, which range in density from 1,200 to 6,000 gates, are customer-configurable and one-time programmable.

Intel Corp., which originally entered the EPLD market with a family of devices second-sourced from Altera, has since established its own identity with a new CMOS family that features a proprietary programmable AND, allocatable OR architecture. In February, the Santa Clara-based company introduced the 5AC324, which doubles the density of the first family member, the 5AC312, while maintaining a 30-ns propagation delay. With 10 programmable inputs and 24 configurable input/outputs, the 5AC324 reduces component count in microprocessor-based systems that require a pipelined throughput of at least 50 MHz.

In March, Intel threw its hat into the high-speed ring with the 85C508, an EPLD fabricated with the company's new 1.0-μm CMOS process. With a 7.5-ns propagation delay, the 85C508 is aimed at the same applications as TI's EPLD: high-speed microprocessor-to-memory interfaces.

Signetics Corp. is also accelerating its pace. In addition to its family of programmable AND, programmable OR logic arrays (PLAs), the Sunnyvale firm in the last year has introduced more than 24 PALs, both bipolar and CMOS. Signetics is now looking to take on the high-speed 22V10, 20RA10, and 32VX10 PAL-based sequencers of Advanced Micro Devices Inc., also of Sunnyvale, with a trio of PLA-based devices: the CMOS PLC42VA12, and the bipolar PLUS37V12 and PLUS38VA12.

Activity has been heavy on the reprogrammable electrically erasable PLD side as well. EEPLD industry leader Lattice Semiconductor Corp. of Beaverton, Ore., isn't ignoring the move toward higher densities by such competitors as International CMOS Technology Inc. of San Jose, but it is concentrating for now on what it considers the fastest-growing portion of the market: the replacement of bipolar PLDs with high-speed CMOS EEPLDs. Lattice has moved into production with its Ultramos III 1.2-μm CMOS process. And its strategic alliances with National Semiconductor Corp. of Santa Clara and SGS-Thomson Semiconductor of Phoenix are beginning to bear fruit; both companies are moving into production with 20- and 35-ns devices.

AMD, which still dominates the market (with a 52% share) due mostly to its bipolar PLDs, is looking to shore up its CMOS offerings. AMD will continue to support its bipolar and CMOS EPLD product lines, but it will fabricate all future CMOS PALs in electrically erasable form. The company last month introduced the 20-pin PALCE16V8H, a generic-array-logic-compatible device it believes will attract as much as 25% of the PLD market by 1992. It also has introduced an electrically erasable version of its industry-standard 22V10. *–Bernard C. Cole*

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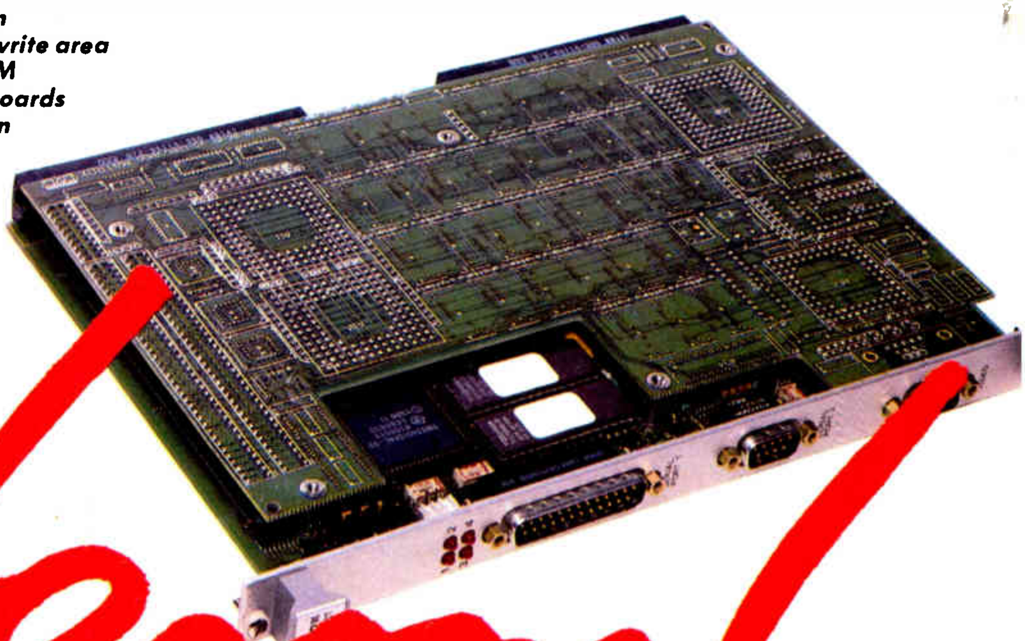

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