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Electronics

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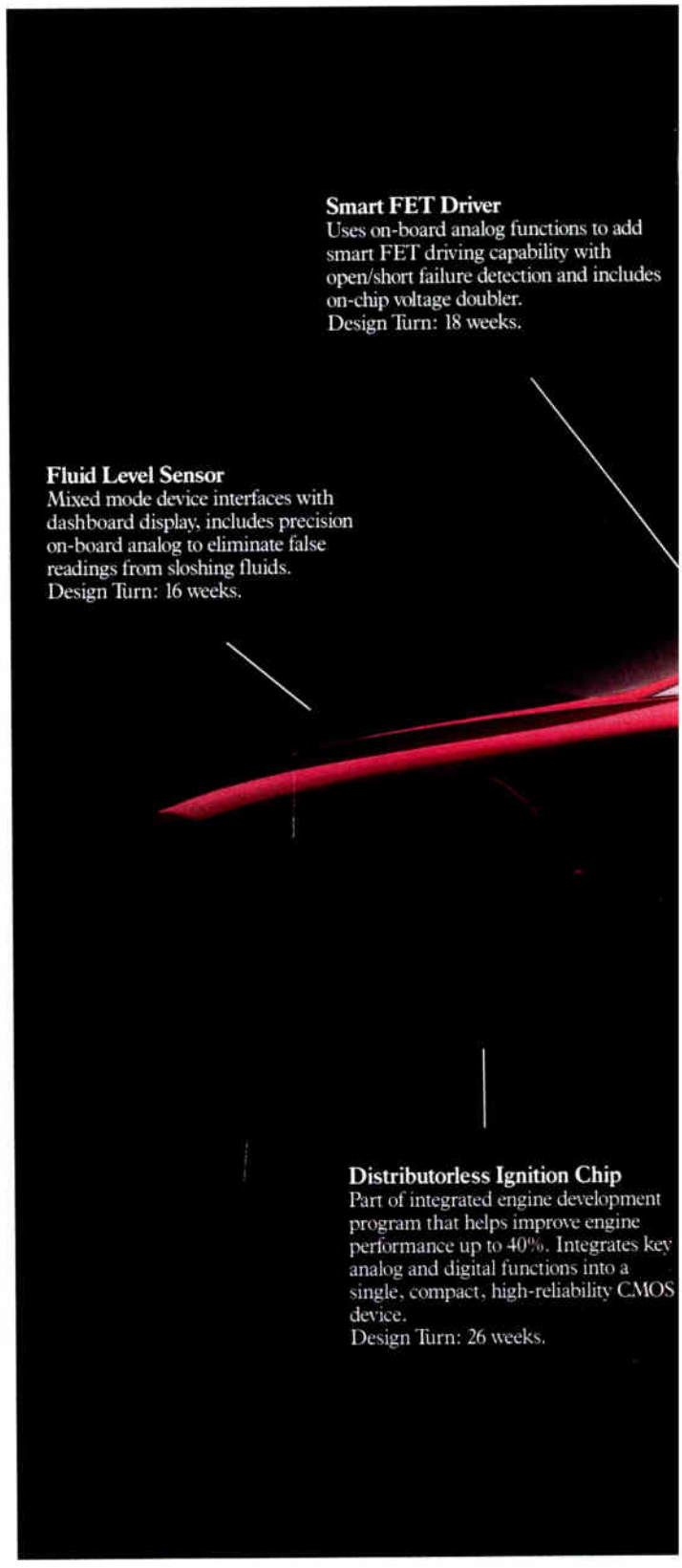

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Electronics

CAN HARDWARE ARTISTS LEARN TO CODE?

The new era of product design will have hardware people doing something suspiciously like programming—and many may resist

Hey, I've been called a wirehead myself, and taken it as a compliment, too. But I've also dabbled in software, just to see.

The time has come, however, for hardware-oriented wirehead engineers to do more then dabble in code. You've heard it before: *hardware is software.* This time it's coming true, though—hardware design is fast becoming a coding exercise. Engineering work for most circuits above the transistor level can be done by writing lines of code that look just like lines of C or Ada.

It wasn't hard to predict, as computer-aided engineering grew in popularity, that eventually the computers would give up the pretense of being drafting tables and demand to be fed not diagrams but modules, procedures, *lines of code.* Now the hardware-is-software crowd has gotten together on a language standard: VHDL. (That's V as in VHSIC, for the Pentagon's Very High Speed Integrated Circuits program, and HDL for hardware description language.) Last year the IEEE set its stamp on a version of the DOD-mandated language, and now CAE's biggest gun, Mentor Graphics Corp., San Jose, Calif., has jumped into the game (see p. 77).

It's time for hardware engineers to start learning to write VHDL code. There are very few now who can, say participants in the still small VHDL-simulator market. Some observers are very doubtful about the ability of most system engineers to make so radical a change in their way of thinking. Vantage Analysis Systems Inc. of Fremont, Calif., for example, has gone to great lengths in its VHDL simulation product to hide the language from the user. Vantage's simulator presents him with familiar schematic views and a library of VHDL function models. If he should need a new one, says Vantage, he'll commission it from specialists.

The approach would appear sensible at a time when next to no engineers are competent in VHDL, and while satisfying Uncle Sam with VHDL documentation is the main aim. But in the long run, Mentor's courageous position promises the industry a bigger payoff. Mentor's new VHDL tools draw the CAE user into the language; to get any real leverage from them, the user must learn how to write code. But once he does, he can do things he never did before. He can play around with simulations of his system using high-level behavioral descriptions, finding flaws and bottlenecks in an architecture before fixing them means murdering the schedule.

The people at Mentor know that there's but a handful of engineers who can use their tools; that's why they're setting up a big training program. Until engineering schools get geared up, Mentor must educate every new user. It's going to be a hard row to hoe.

It *is* a giant leap. Many engineers won't make it. But I'm convinced that system builders who move fast to build a cadre of VHDL-literate engineers will win a valuable time-to-market edge. Tell your wireheads a secret: writing code can be fun! **JEREMY YOUNG**

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NEWSLETTERS

FEATURES

COVER: FRANK AIELLO

PAGE 73

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PEOPLE

DEPARTMENTS

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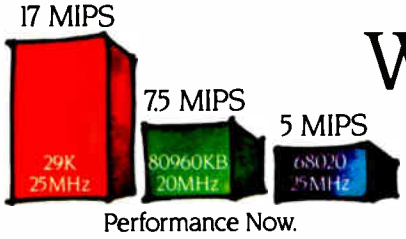

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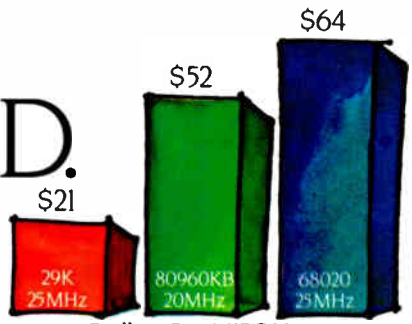

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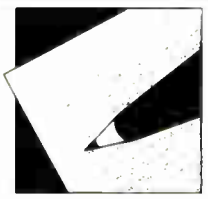
Circle 5

LETTER FROM ARIZONA

A BAD YEAR MAKES ARIZONA SEARCH ITS HIGH-TECH SOUL

PHOENIX



After four decades of steady growth, Arizona's electronics industry hit some snags last year. Now executives and government officials around the state are wondering if the setbacks were precursors of tough times to come in the years ahead.

The first of two major disappointments came early in 1988 when Sematech, the industry's manufacturing research consortium, chose Texas over Arizona (and the other contenders) as the site for its headquarters and research facility. Then, in November, the federal government decided not to base its superconducting-supercollider project, a mammoth program slated to last for the next decade, in the state. The winner, again, was Texas.

The Arizonan dismay was exacerbated by overly optimistic expectations. Many of the state's industry figures and politicians believed they would land one or both projects. Some of them still cling to the notion that Texas won out through underhanded politicking.

Besides losing the plums they hoped to get, Arizona's electronics executives also lost some things they already had. The semiconductor market slumped and defense-related orders dropped in the second half of 1988. And in a crowning blow, IBM Corp. announced that during 1989 it would take some 2,800 jobs away from its mainframe plant in Tucson and consolidate them in a plant in San Jose, Calif.

STILL STRONG. But the setbacks of 1988 do not mean the electronics industry in Arizona is on the brink of disaster. Despite them, it remains very healthy. Statewide statistics are hard to come by, but the Arizona council of the American Electronics Association estimates that revenue from aerospace and electronics was about $6 billion last year, which means they've doubled since 1982. Total employment in the industry reached some 70,000 people, about half of Arizona's manufacturing jobs, with an annual payroll of about $1.9 billion. Electronics has now, for the first time, leapfrogged tourism and construction in annual revenue.

Such growth is what Arizona has come to expect ever since World War II. The first high-tech companies started moving in then, lured by the climate and the state's ferociously pro-business environment. General Electric, Hughes Aircraft, Motorola, and Sperry were among the first; since then, they've been joined by other giants like Honeywell, IBM, and Intel, plus a host of smaller companies.

The climate and the pro-business attitude remain potent lures. Added to them is a favorable economy, one that benefits both employers and employees. The cost of doing business is some 20% cheaper than it is in Southern California, according to an Arizona Department of Commerce study. Similarly, a house in Arizona costs less than half the price of a comparable house on the West Coast.

The year-round sunshine, healthy economy, and laid-back lifestyle have attracted a competent and stable labor force. Few people who put down roots ever leave, says Richard G. Loeb, chairman of Optifab Inc. in Phoenix. He tells the occasional defecting employee, "you'll be back." The same holds true for companies: those that have established themselves seldom leave. Generally, they expand. Motorola, for example, is putting its world-class MOS 6 dynamic-random-access-memory facility in Mesa, an investment representing upwards of $100 million. And Intel continually stepped up activities at its Chandler complex during the recent chip boom.

But the events of last year made industry executives aware that they couldn't rely on the natural advantages of Arizo-

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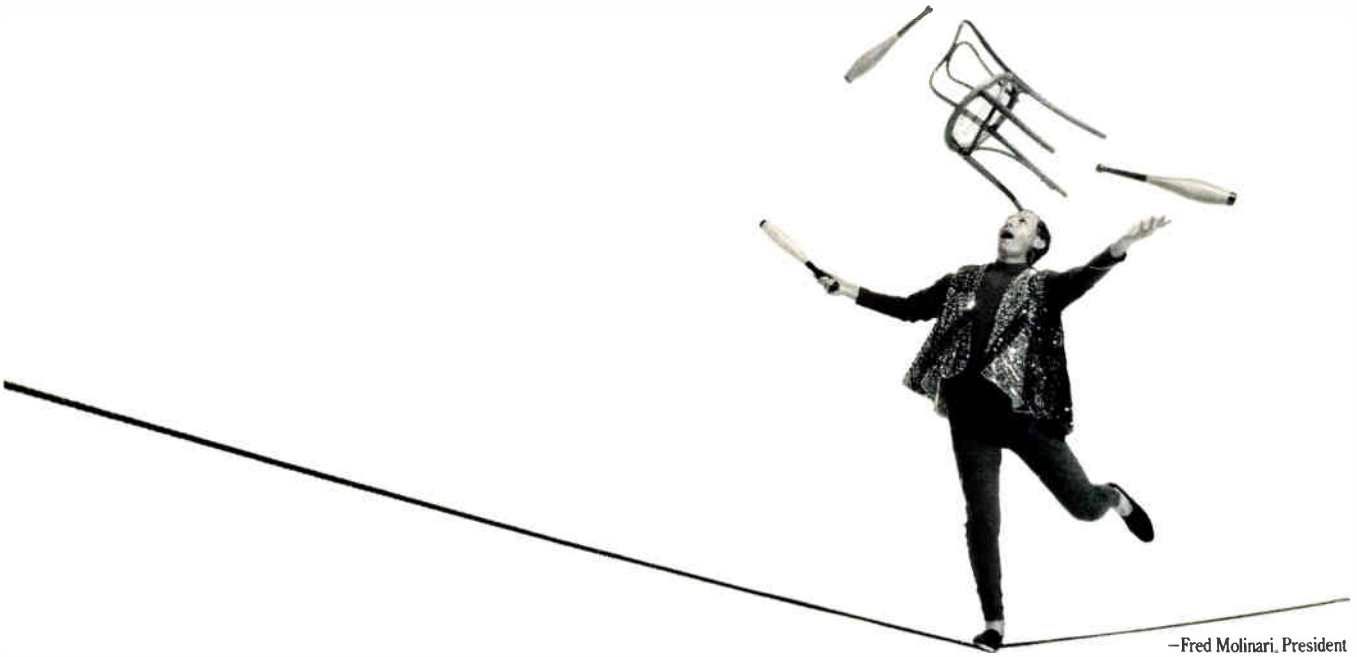
* ANNUAL GEOGRAPHICALLY VARIABLE OPERATING COSTS IN $MILLIONS

SOURCE: ARIZONA DEPARTMENT OF COMMERCE



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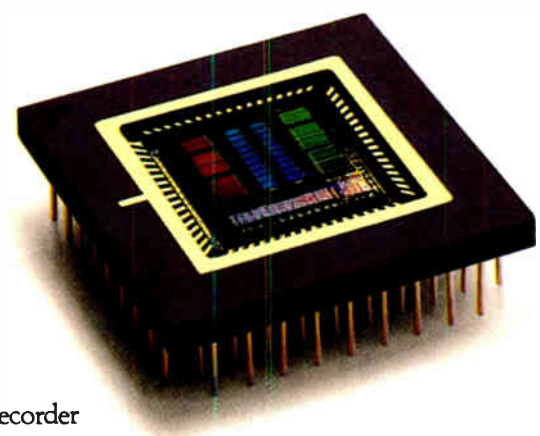

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Circle 11

na to guarantee continued growth. In fact, a number of them had already come to that conclusion; 1988 simply added a sense of urgency to plans they were starting to make.

These executives belong to a loosely organized network revolving around the state AEA council. They have set themselves an ambitious task: to define their goals for growth and how they can best reach them. The group began its work when the members started to realize that some kind of statewide planning couldn't be put off any longer. "We're at a decision point—how we mature," says Terry Bibbens, chairman of the council and a senior vice president at Loral Corp.'s Defense Systems in Litchfield Park.

The first concrete action focuses on the state legislature—the group is trying to get it to set up a high-tech committee that can help guide state policy. "We recognize that companies will come and we'll get growth, no matter what," says Optifab's Loeb. "The trick is to manage it rather than react to it."

Part of the problem is that years of easy growth have made the state's leaders complacent, a growing number of executives think. Experience in states like Texas and Massachusetts shows that landing Sematech-type projects demands a well-organized, well-financed effort that draws on the resources of the entire state. By all accounts, nothing of this sort has ever happened in Arizona. Unlike a number of other states, Arizona has no high-tech advisory groups.

Can the state shake its frontier mentality to start cooperative planning?

The setbacks therefore also jolted at least one state agency, Arizona's Department of Commerce, whose charter includes luring new industries. The department just didn't have a mechanism in place for coordinating the state's major players, says its director, David P. Jankofsky. That's always been a weakness, he says, and last year it proved disastrous. But it did teach a school-of-hard-knocks type of lesson, says Jankofsky, namely, the need for local economic development groups (notably in Phoenix and Tucson), state authorities, and companies "to speak with one voice." Now Jankofsky's chief goal is to put together a mechanism, backed by the state, for this purpose. While the task amounts to "a delicate balancing act," due to egos and divergent interests, he expects to have something organized by spring.

Meanwhile, the AEA activists are wary. Even though they're pitching in, in the knowledge that the state has to lend a hand, past disappointments have made them skeptical of promises such as Jankofsky's. One reason is that historically, knowledgeable industry types have seldom been consulted by the state. So if a state development plan is unveiled soon, as promised, its fate will be determined by who's behind it. "Watch for the names," says one executive. "If it's the same old vested interests in banks and real estate, then it won't work."

In short, Arizona does not have an effective "old-boy network," that confederation of bankers, industry heavyweights, real estate interests, and old money that makes things happen. Rather, it runs on a frontier mentality, says R. Dale Lillard, the president of Lansdale Semiconductor Inc. in Tempe. "This remains a very conservative state."

NO WONDER. Given the prevalent attitudes, says one observer, it's no wonder Arizona lost Sematech and the collider project. "It is painfully obvious that Arizona is not yet in a position to attract these world-class projects," says Walter J. Schuch, editor of the *Southwest Technology Report*, a widely read newsletter. Texas, by contrast, "has statewide depth in technical and scientific competence; it has a stable, broad-based, high-tech industry; and it has strong local financial resources. Arizona does not."

Finances are a particular sore point for high-tech businesses, especially the startups and small companies in need of local financing. The problem lies with Arizona's bankers. They are for the most part a play-it-safe breed, who neither understand high-tech businesses nor appreciate their importance to the state. They prefer real estate loans, industry veterans say.

"If you don't go in there pushing a wheelbarrow, you come right back out," says David R. Buchanan, a veteran start-up and venture-capital executive who is president of Three-Five Systems Inc. in Phoenix.

The bankers' tunnel vision exemplifies a more general lack of appreciation for technology, says Schuch: "People don't know the difference between a semi truck and a semiconductor." He proposes putting more emphasis on helping existing companies grow and on developing a "high-tech master plan that includes specific goals and objectives, that involves all facets of the community."

Which is more or less what the state's electronics executives are thinking these days. Arizona has seen its technology growth pause and then take off again without intervention, but few of them believe they can make further headway without planning and support at the top levels of state government.

The AEA group is trying to get that. Bibbens and his colleagues realize they are charting new territory. "But if we don't develop the right goals," he says, "others will [step in]." *–Larry Waller*

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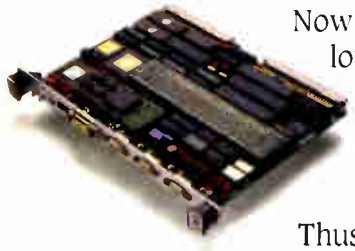

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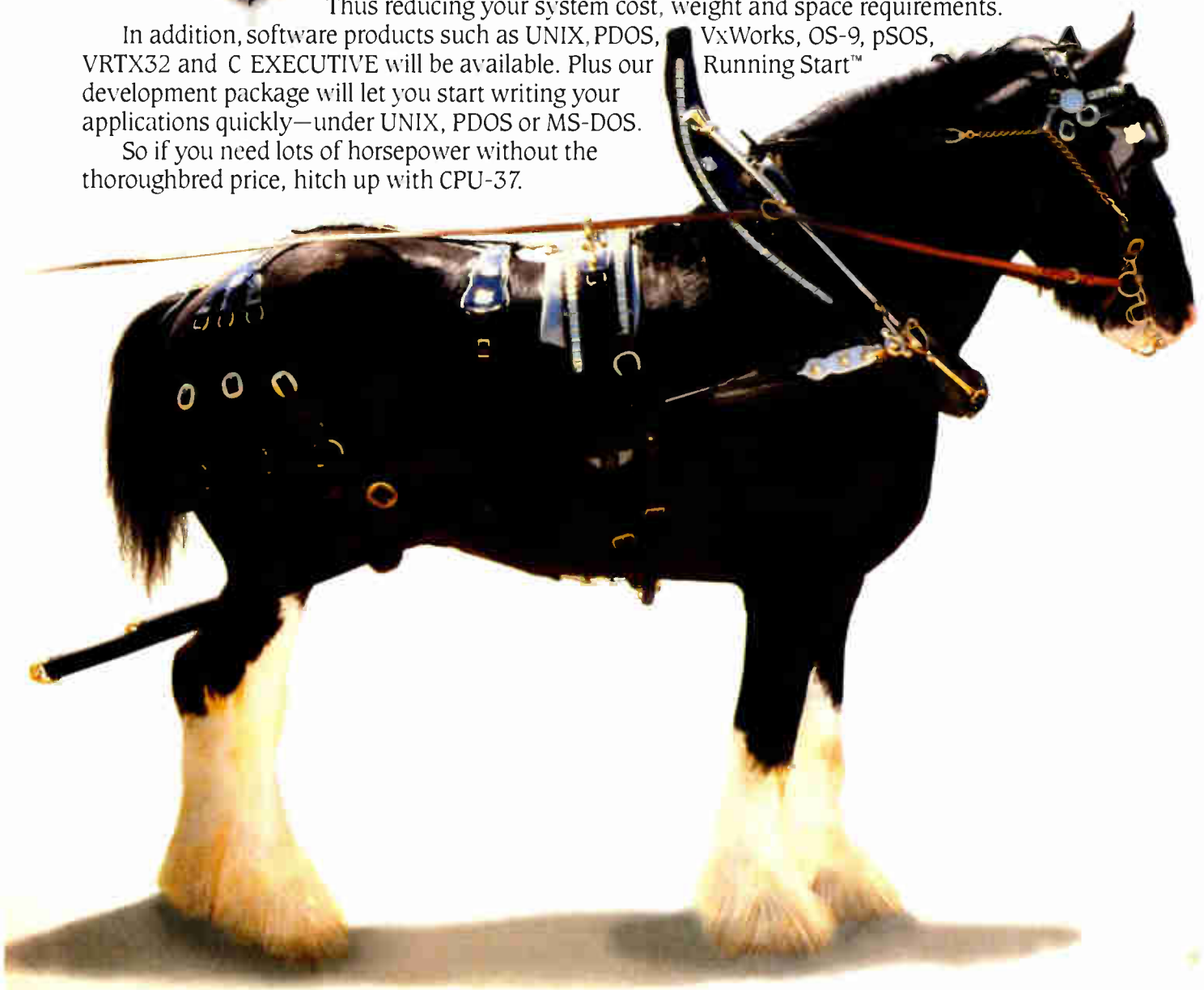

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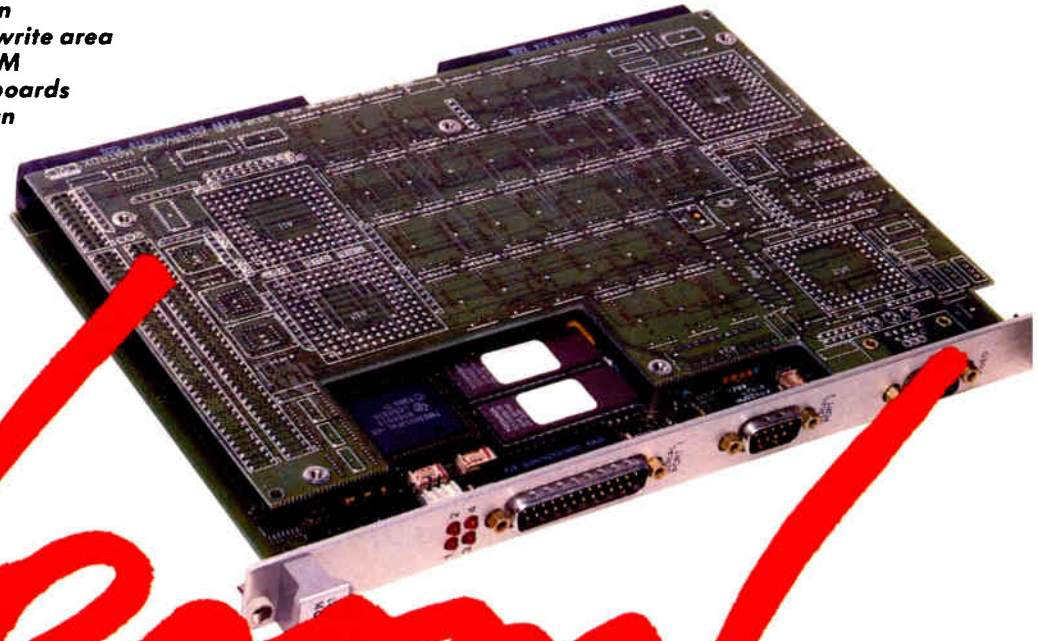

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ELECTRONICS NEWSLETTER

GRAPHICS SYSTEM FOR APOLLO'S DESKTOP SUPERCOMPUTER FINALLY DEBUTS

Apollo Computer Inc. finally has some good news. After two profitless quarters, the Chelmsford, Mass., work-station pioneer finally introduced its graphics subsystem for the Apollo Series 10000 desktop supercomputer—several months late. Apollo expects the Series 10000, which uses reduced-instruction-set computing, to lead the company back into the black. A server version of the 10000 [*Electronics*, March 3, 1988, p. 69] began shipping last fall. The enhanced version is designated Series 10000VS to denote the visualization system. Tight coupling of its drawing engine to as many as four central-processing units over a 64-bit-wide, 150-Mbyte/s bus enables simultaneous intensive number crunching and 3-d graphics rendering. Delays in laying out the 22,000-gate CMOS arrays used in the RISC drawing engine caused a slippage of about four months in the subsystem's introduction. □

HERE'S A PEEK AT MOTOROLA'S MICROCONTROLLER PLANS

New details of what Motorola Inc. is planning for its microcontroller family are leaking out. The broad outlines of the company's next-generation microcontroller—the MC68HC32—were sketched last month at a special session for university teachers and researchers in Tempe, Ariz. Scheduled for introduction later this year, it is a radical departure from the original concept, a 16-bit or mixed 8- and 16-bit design that was compatible with the existing 8-bit MC68HC11 family. Instead, Motorola is going for a design that combines an internal 32-bit central-processing unit with an external 16-bit data and address bus. Code-compatible with the 68000, its instruction set also includes selected commands from the MC68010 and the MC68020. The new controller will be fabricated with a 1.0-μm CMOS process. In addition to 1.5 Kbytes of on-chip standby static random-access memory, it sports 12 independently programmable chip selects, a bus response-time monitor, a double bus-fault monitor, and a software watchdog system. Other features include a spurious interrupt monitor, a periodic interrupt monitor, and a programmable on-board phase-locked loop for system clocking. □

OSF DELIVERS A USER-INTERFACE TECHNOLOGY—AND IT'S ON TIME

The Open Software Foundation has pulled off its first success—and in doing so has gained some welcome early credibility. The foundation, which was set up by a number of computer vendors early last year to develop alternative open-system software standards based on AT&T Co.'s Unix operating system, has announced its selection of a user-interface technology combining elements contributed by Digital Equipment, Hewlett-Packard, and Microsoft. Almost as important as the announcement itself is that OSF did what it said it would do when it said it would do it—in the face of industry skepticism about the ability of its open selection process to produce technical developments at all, let alone in the time set by the organization. The process involved detailed evaluation of 23 of the 39 responses to its July request for technology. The user interface, called OSF/Motif, consists of DEC's Application Program Interface and the HP/Microsoft Window Manager, providing a look compatible with Microsoft's Presentation Manager (the user interface for OS/2) combined with a 3-d appearance from HP, and icon grouping from DECWindows. The industry consensus is that the OSF staff has probably zeroed in on the best possible combination—one that could garner industry-wide acceptance and eclipse the OpenLook user interface being offered by AT&T. OSF/Motif will be available for several operating-system environments, including the forthcoming OSF/1 and Unix System V.4. The next milestone awaited by the industry is the development and release of the OSF/1 operating system itself, which is expected in the second half of the year. □

ELECTRONICS NEWSLETTER

HEWLETT-PACKARD SETS A NEW PRICE/PERFORMANCE STANDARD FOR BOARD TESTERS

Hewlett-Packard Co. is breaking the $1 million barrier for automatic testers that can handle dense boards with lots of application-specific integrated circuits and surface-mounted devices mounted on both sides. The Palo Alto, Calif., company has come up with a combination in-circuit and functional tester that sets a new low in price and a new high in performance for combinational testers. Designated either the HP3070AT or HP3070SMT, it costs $301,000 to $778,000. It allows unattended automatic testing, tests two-sided boards, and increases the probe-placement accuracy by a factor of 10. Also, the design decreases the error rate to 48 parts per million—currently available models achieve only 465 ppm. While other testers add lots of random-access memory to hold all the patterns needed to perform a test, HP's comes with powerful pattern-generation capability. □

STARTUP DEVISES MICROPROCESSOR FOR FUZZY LOGIC

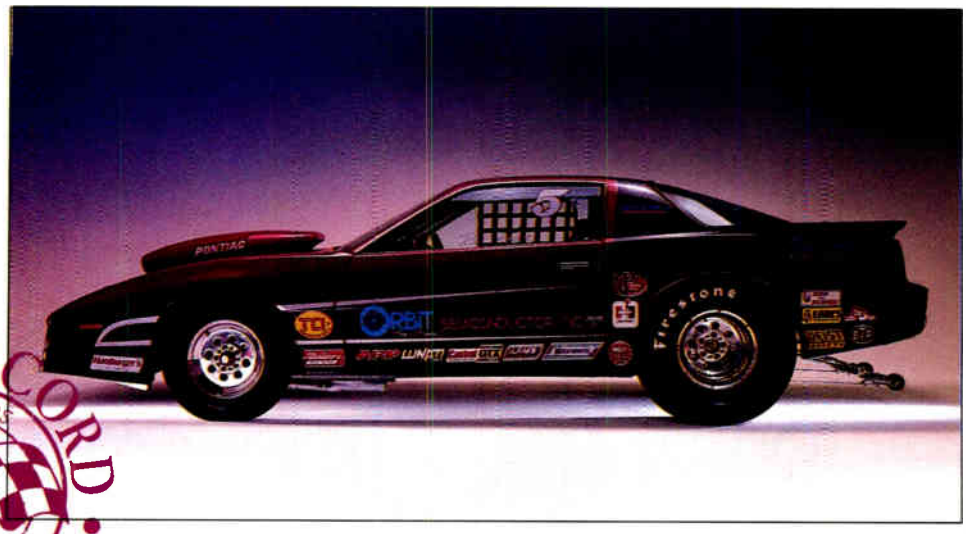
An Irvine, Calif., startup is almost ready to unveil a standard microprocessor dedicated to so-called fuzzy logic, which may be the key to computers that "think" more like humans than machines. If Togai InfraLogic Inc. succeeds, the device could be just the ticket to bring this infant technology into the reach of commercial users. The firm's FC110 Digital Fuzzy Processor provides on-chip algorithms that work in concert with a separate 128-Kbyte electrically programmable read-only memory containing the knowledge base necessary for a specific task. Together they offer the simplest approach yet to getting the benefits of fuzzy logic, which is being billed as the best way to implement both artificial-intelligence packages and neural-network technology. The Togai development is one of several fuzzy-logic efforts now under way, including one in Japan (see p. 69). □

CERAMIC PIN-GRID-ARRAY PACKAGES RACK UP HUGE SALES

The beat goes on for ceramic pin-grid arrays in the packaging business, with the technology dwarfing other segments of the materials industry. Sales of the packages zoomed to $1.7 billion in 1988, based on some 173 million units, says consultant Daniel J. Rose, an authority on materials. That tops silicon's $1.5 billion intake (as a raw material), he says. Because of their high gold content, and the upward spiral of nickel and copper prices, the packages are expensive—about $10 each. But their popularity is fed by the increase in high-pin-count chips, such as top-of-the-line microprocessors and gate arrays, for which they are uniquely suitable, says Rose, who was a speaker at last month's annual seminar of the Semiconductor Equipment and Materials International trade group at Newport Beach, Calif. □

RESEARCHERS USE MICROSCOPIC WIRES TO CREATE A QUANTUM DEVICE

Many experts believe the answer to getting the fast, dense superchips of the next decade lies in structures taking advantage of quantum effects [*Electronics*, October 1988, p. 143]. So researchers at the University of California at Santa Barbara have created what they call a quantum-wire superlattice, which in the active region of a device employs millions of parallel 50-by-50-A wires fabricated of gallium arsenide. Building the superlattice wire structure, which the developers say is the first of its type, will enable them to determine whether wires are more efficient in moving electrons because they offer less resistance than solid material, as theory predicts. Other quantum approaches, such as the one reported by Texas Instruments Inc. of Dallas, use thin layers of material in a well structure to get the wavelike quantum effect of electrons moving through the transistor wall. □



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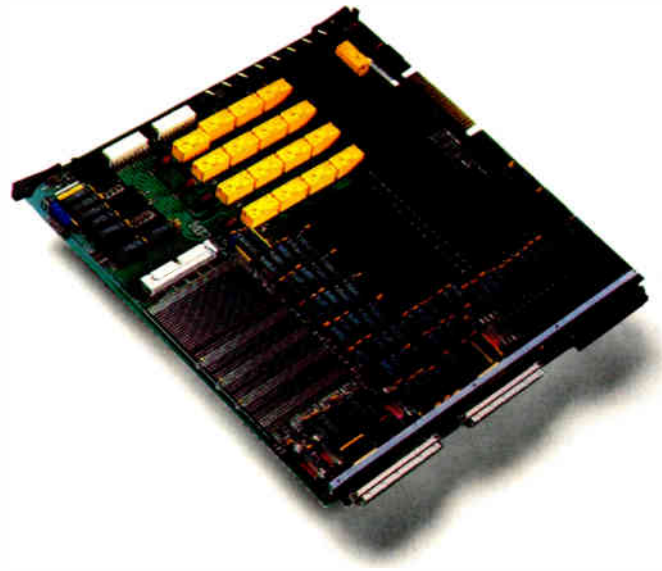
Circle 19

A GENTLE REMINDER ON THE IMPORTANCE OF LOOKING AROUND.



Combinational Testers. Technically speaking, it's no longer a question of if or when you'll need one. But which system to choose.

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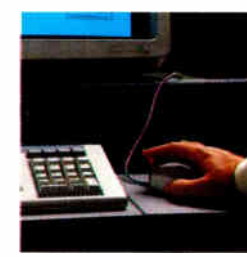
Because the Zehntel 8000 holds a number of pleasant surprises for you —in power, flexibility, and price.

BY ALL MEANS, COMPARE.

To appreciate its performance fully, it's only fair to judge the 8000 by comparable systems: those costing much more.

The 8000's open architecture, for example, can greatly reduce overall testing costs. Using the Functional Interface Board pictured above,



you can place your own hot-bed test directly into the 8000 system.

The 8000 is the only combinational tester with 2,048 fully-hybrid, non-multiplexed test points. Each node has a driver/receiver behind it; each can be used for either functional or in-circuit testing. All of which helps reduce the

cost of programming and implementing engineering changes.

The 8000's digital test subsystem truly warrants the term "high performance," with 10 MHz pattern rate, 8Kx4 RAM per node, programmable slew rates and 10ns programmable edge placement.

The menu-based, mouse-driven interface simplifies programming, with multiple windowing capability, integrated logic analyzer and graphic quality analysis tools.

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Circle 21

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Circle 22

Seiko Instruments

PRODUCTS TO WATCH

HEURIKON'S VME BOARD MOVES BLOCKS TWICE AS FAST AS THE COMPETITION

By integrating National Semiconductor Corp.'s newest graphics chip set into its VMEbus HK85/VRGP board, Heurikon Corp. is doubling the boundary-bit-block-transfer (BitBLT) rates of comparably priced VME boards, claims the Madison, Wis., company. Based on National's DP85XX chip set, the HK85/VRGP includes 1 Mbyte of video random-access memory, 512 Kbytes of program memory, 64 Kbytes of electrically programmable read-only memory, and support for both the X-Windows and Graphical Kernel System standards. It also provides maximum resolution of 1,024-by-1,024 pixels by 8 bit planes. The board's processing power comes from the DP8500 Raster Graphics Processor, a 20-MHz programmable device working with a set of DP8511 BitBLT processors, one per plane, but expands to 24 with a second card. It will be available next month for $3,220 in 100-unit quantities. □

DATA COMPRESSION DOUBLES CAPACITY OF QUARTER-INCH TAPE DRIVES

System integrators can double the capacity of ¼-in. tape drives—the current crop of backup tape drives for IBM Corp.'s Personal Computers, Personal System/2, and compatibles—at no additional cost by switching to Colorado Memory Systems Inc.'s QFA-500 drive. The Loveland, Colo., company uses a 2 : 1 data-compression algorithm developed by STAC in Pasadena, Calif., in the drive's control software. Boasting 500 Mbytes of storage and a 5.25-in. form factor, the QFA-500 can achieve data-transfer speeds of up to 2 Mbytes/min for backing up hard disks in PCs based on Intel Corp.'s 80386 microprocessors. Since the data compression is done in software, data-transfer rates drop with less powerful machines. The drive's bit-error rate is 10^{-15}. STAC will offer a single-chip hardware implementation of the algorithm later this year. Prices for the QFA-500 start at $1,395. □

DATA GENERAL SHIFTS ITS OSI INTEROPERABILITY IMAGE INTO HIGH GEAR

Continuing its product strategy of gearing up for international communications standards, Data General Corp. has rounded out its software offerings that completely implement the International Standards Organization's seven-layer Open Systems Interconnection reference model. The Westboro, Mass., computer maker's three newest packages let customers link Data General and non-Data General computers into interoperable networks. One of the latest packages, called DG/FTAM, enables Data General users on an OSI network to perform file transfer and file management with other computers that comply with the OSI specifications for those functions. The DG/OAPI tool kit helps users create OSI applications that can operate on heterogeneous networks. The DG/OTS is a complete OSI communications platform. Available in the fourth quarter, low-end systems begin at $1,500 for DG/FTAM, $2,500 for DG/OAPI, and $900 for DG/OTS. □

88000 RISC PROCESSOR IS AVAILABLE, MOTOROLA SAYS

The Microprocessor Products Group of Motorola Inc., Austin, Texas, has begun accepting orders for its widely publicized 88000 reduced-instruction-set microprocessor. More than 50 customers have sampled the two-chip set since early last year. Broader sampling is now under way, with full production scheduled for the second quarter. The 88100 central-processing unit integrates integer and floating-point execution, while the 88200 cache-memory-management unit offers a single-chip approach to cache-memory design. The 88000 performance is rated at 14 to 17 VAX-equivalent mips at 20 MHz. Each chip is housed in a 180-pin grid array. Samples of the 88000 cost $494 and the 88200, $619. □

PRODUCTS TO WATCH

JUPITER ATTACKS THE LAN-SERVER MARKET WITH A USER-CONFIGURABLE SYSTEM

By slimming down its System 1000, Jupiter Technology Inc. of Waltham, Mass., has conjured up a user-programmable data-communication computer to compete in price with single-function devices. The $8,500 System 100 can be configured to control a remote site in large networks or as a network server and a gateway device between networks. When used as a local-area-network server or a multiaccess-terminal-cluster controller, it competes with nonprogrammable single-function boxes, such as protocol converters, which sell in the $6,000 range. It interconnects systems using many incompatible communications standards, including Ethernet, TCP/IP, and CCITT's X.25 packet-switching protocol. The System 100 serves from four to 384 communications lines and can accommodate up to eight Motorola 68000-based microprocessors. □

VERDIX MAKES WRITING ADA CODE FOR REAL-TIME CPU BOARDS EASIER

A real-time Ada development system from a duo of small software companies breaks new ground by letting software engineers working at a Unix work station develop Ada code for central-processing-unit boards. The software, VADS/Works, combines Verdix Corp.'s Ada Development System with a real-time operating system from Wind River Systems of Emeryville, Calif. By performing most of the basic conversion work between Unix and Ada, it saves time and money compared with development environments now in use that have to be tacked together in-house, says the Chantilly, Va.-based Verdix. Now available for Motorola 68020 boards from Heurikon Corp. of Madison, Wis., the system is in beta test with boards from Force Computer Corp., Los Gatos, Calif.; Motorola Inc., Phoenix, Ariz.; and others. VADS/Works pricing ranges from $27,500 to $100,500, depending on the work station on which it will run. □

NEC BOOSTS ITS V70 MICROPROCESSOR'S CLOCK RATE 75%

Scaled-down versions of NEC Corp.'s V70 microprocessor that boost clock speeds by 75% will be available this year, and even faster versions are waiting in the wings. The Tokyo-based company is speeding up its present 20-MHz CMOS chip to 33 MHz by going from 1.2-μm design rules to the 0.8-μm design rules that NEC developed for its forthcoming 4-Mbit dynamic random-access memories. The new chip features a silicide overlay on the polysilicon gates to maintain low-resistance first-level interconnection despite the fine pattern. Chip size is cut almost in half, raising hopes for both lower pricing and the possibility that it could be used as a core in future application-specific integrated circuits. Samples will be available this autumn, with 40-MHz and higher-speed versions to follow. □

HERE'S A 32-MEGAFLOPS COMPUTE SERVER FOR MACINTOSH NETWORKS

High-end processing has arrived for networks of Apple Computer Co.'s Macintosh machines with Chorus, a supercomputer designed by Human Devices Inc. Containing up to 16 high-speed floating-point processors, Chorus connects Macintoshes to form a multiuser desktop-computing environment boasting performance that ranges from 8 to 32 million floating-point operations/s, depending on the number of processors. The compute server opens new vistas for the Macintosh in engineering simulations, financial modeling, and photorealistic graphics, says New York City-based Human Devices. Available now, base configurations go for $9,700 for a single-processor version to $25,500 for a four-processor version. Additional four-processor add-on modules cost $16,800. □

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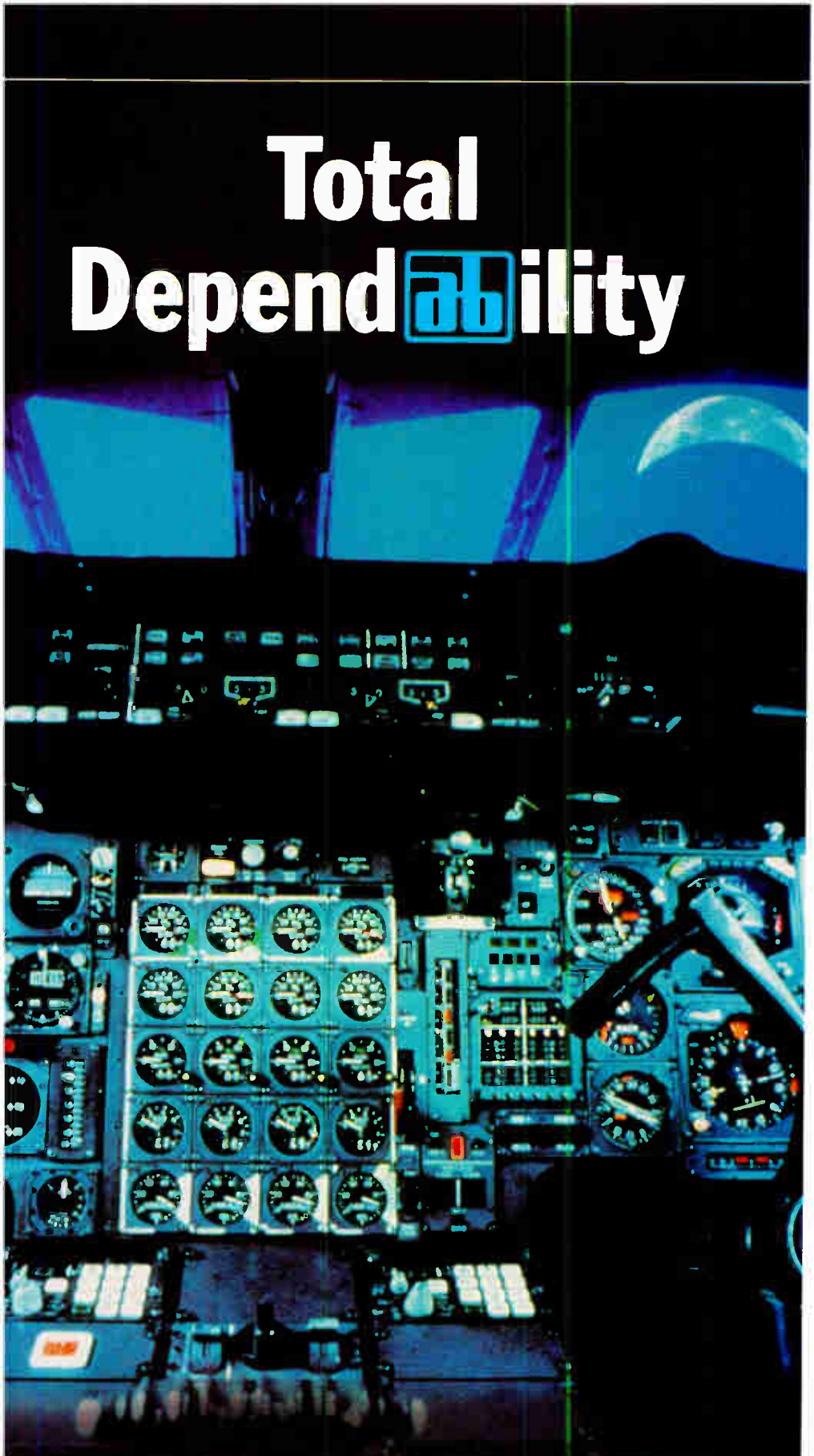

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Circle 25

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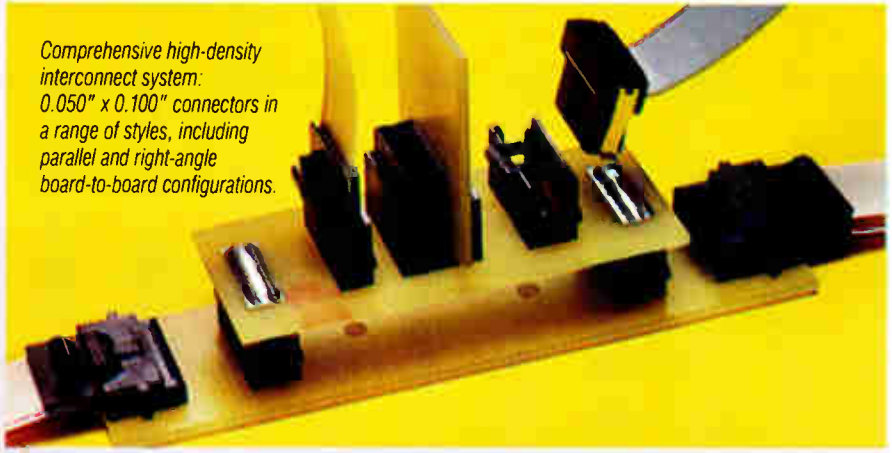
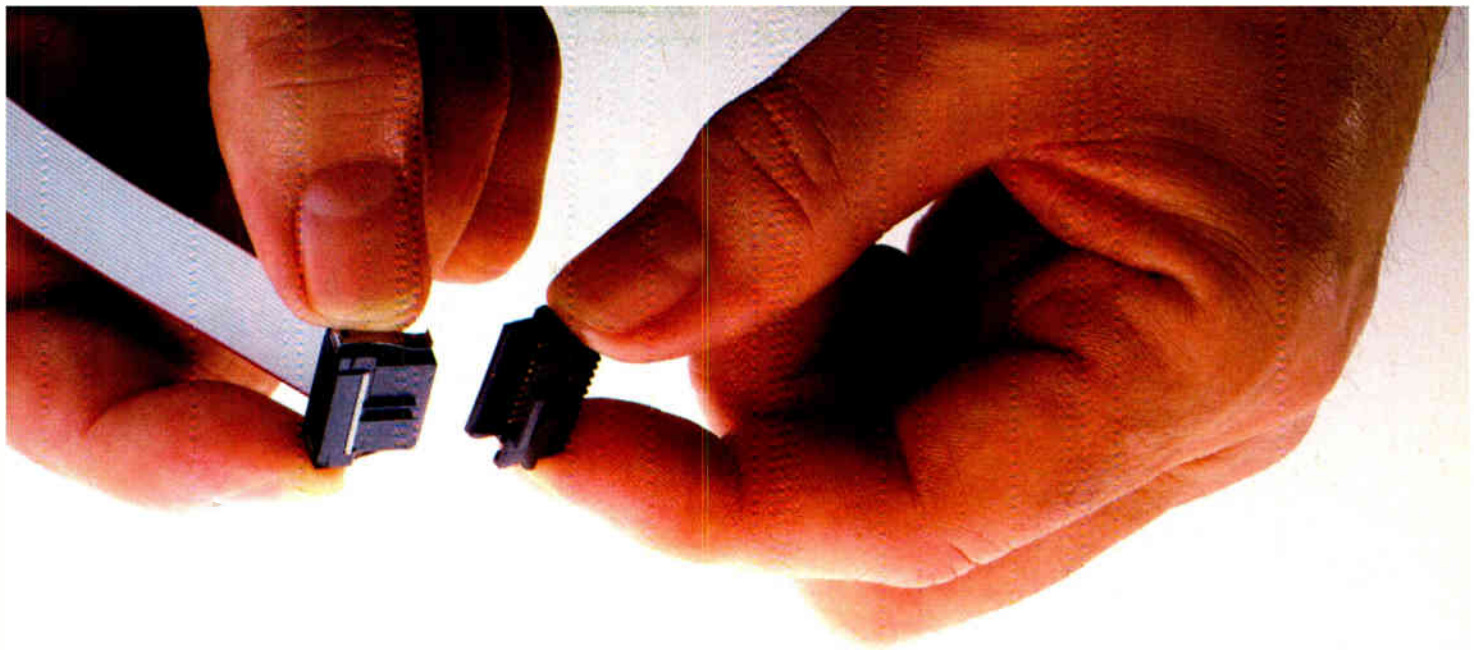
Special design innovations (such as putting the latch hardware on the *cable* side) shrink our System 50 line to the least board space of any connector in this class. Even 0.050″ x 0.050″ types.

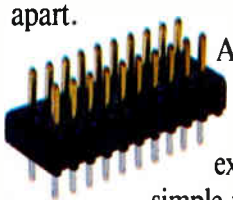


Comprehensive high-density interconnect system: 0.050″ x 0.100″ connectors in a range of styles, including parallel and right-angle board-to-board configurations.



no small idea.

Example: 2x25 position shrouded headers occupy 1.5″ x 0.284″ of board surface. And parallel boards mount with inside faces a mere 0.450″ apart.



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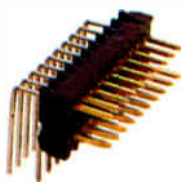

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INSTRUMENTS OF DISCOVERY

Circle 28

Electronics

HOW WILL TECHNOLOGY FARE UNDER PRESIDENT BUSH?

This will be a key year for budget decisions as megaprojects eat up billions

WASHINGTON

Now it's all up to George Bush. President Reagan, in the waning days of his administration, submitted a budget to Congress that most experts agree was dead on arrival, a document that at best could serve as a springboard for Bush to establish his own science and technology agenda. How Bush modifies that budget in the coming weeks will tell the story of federal science and technology spending for years to come.

Make no mistake about it—fiscal 1990 will be a key year for science and technology investment. Funds that in the coming year are sunk into expensive projects like the superconducting super collider, the space station, and the National Aerospace Plane will commit the U. S. to spend billions more over the next decade just to complete them. And with such megadollar commitments, funds may be scarce for the less glamorous research-and-development programs that many critics believe could revitalize U. S. technological competitiveness.

LINE FORMS. That worries some in Congress, who point to a spate of industry groups that, emboldened by the apparent success of the Sematech chip-making consortium, are seeking federal support for their own critical research initiatives. High-definition TV, X-ray lithography, and precision optics are just three areas in which various groups and government agencies are now clamoring for dollars.

The optimistic Reagan budget seeks $315 billion for the military—that's inflation plus 2% real growth over 1989. It includes a $2 billion increase in spending for the Strategic Defense Initiative and hundreds of millions more for the other budget-eating pet projects.

So now comes the hard part: waiting for the changes. Bush will surely submit a budget revision, although no one knows exactly when it will come or how drastic it will be. Congress will just as surely make changes of its own. The overriding question is, just how different will President Bush be from Vice President Bush—how closely will he hew to the Reagan line?

With the federal government facing a number of crises—the deficit and the high-priced bailout of failing savings and loan institutions, to name just two—funds will be tight for at least the next decade. So no one in Washington thinks Reagan's plan for 2% real growth in defense spending is even plausible. "The $315 billion in there for defense is hopelessly optimistic," says John Mancini, vice president of domestic affairs at the American Electronics Association. "I don't think anyone thinks they'll do better than keep pace with inflation over the next five years." Even Bush has acknowledged a willingness to keep the Pentagon on a zero-growth budget plan.

In other areas, the questions center less on how much money to spend than on how to spend it. If any of the plans to have federally assisted research programs akin to Sematech pan out—and if Congressional goals to boost military investment in its technology base are met—cuts, delays, or even cancellations may hit those big-ticket programs: SDI, the super collider, the space station, and the National Aerospace Plane, a joint effort by the Air Force and the National Aeronautics and Space Administration to develop a hypersonic spacecraft that could take off and land like a conventional airplane. That program alone will cost $426.7 million in 1990, according to the Reagan plan, of which roughly two thirds will be paid for by the military.

Then there's the National Science Foundation, which is on the path to doubling its 1987 budget by 1993, assuming its planned 14% hike for 1990 goes through. Much of that growth is being channeled into a major initiative in education, which NSF director Erich Bloch calls "one of the most persistent and limiting problems this country faces." But in the basic sciences, where NSF's charter lies, more growth is needed, he says: "The average grant today is about $75,000. We've got to get that up to $100,000 or $120,000."

NOTHING FOR NIST. In contrast to the sexy megabuck projects, the Reagan budget seeks no funds whatsoever for the new technology-base responsibilities of the National Institute of Standards and Technology, the rechristened National Bureau of Standards. The Omnibus Trade Bill of 1988 renamed the agency and gave it a mandate to fund regional manufacturing-technology centers; advanced R&D in preproduct commercial technology; and small companies seeking to capitalize on inventions. The idea was to help struggling industries compete with foreign competitors, who often are government-subsidized.

Other projects, such as the space station, will have significant long-range costs. NASA, for example, says that it will have to double its 1990 budget—set by Reagan at $5.75 billion—by the year 2000 just to maintain ongoing programs such as the space shuttle and the space station. An exploratory mission to Mars or other science programs in space would

THE PENTAGON'S BIG R&D PROGRAMS

Project	1988 ($ Millions)	1989 ($ Millions)	1990 ($ Millions)
Strategic Defense Initiative	3,553	3,627	5,591
Space Station	NA	900	2,050
National Aerospace Plane	300	426	556
Superconducting Super Collider	NA	100	160
Sematech	100	100	100
Remotely Piloted Vehicles	46	40	123
Joint Surveillance/Target Attack Radar	337	236	153
Electronic Warfare Development	NA	97	150
Mimic	49	67	82

SOURCE: DEPARTMENT OF DEFENSE

add to that cost, NASA says.

This leaves little money for the kind of investment in the technology base that many in industry, Congress, and the government believe is essential for U. S. business. "It's the Reagan view of science—it's Big Science," says an aide to Jeff Bingham (D., N. M.), the outspoken chairman of the Senate Defense, Science, and Technology Subcommittee and a prime architect of Sematech. He maintains that these programs cost too much and benefit too few, and that federal dollars would be better invested in developing technologies, such as semiconductors and computers, that hold the key to U. S. technological competitiveness in the 1990s and beyond.

Take the superconducting super collider, for example. The Reagan budget seeks $250 million for the Texas-based facility in 1990, $160 million of which is earmarked for construction. Under the current plan, that $160 million investment would pave the way for as much as $5.9 billion by the time the project is completed in 1998. "The key thing is to get some construction funds," says a DOE official. "That's a commitment, because you don't start building something you don't intend to finish."

Last year saw several top-level reports emerge from both inside and outside the government on the need to revitalize the struggling U. S. technology and industrial base, and yet another is expected shortly, this time from the Congressional Office of Technology Assessment. But this interest is not reflected in the Reagan administration's budget plan. Rather than providing more money for such initiatives, it provides less.

For example, the Defense Advanced Research Project Agency, the Pentagon's chief research arm, faces a $260 million cut in 1990, and almost all of that comes from its technology-base account. Darpa's budget will drop from about $1.3 billion this year to $1.1 billion in 1990, followed by a modest 4% increase in 1991. Other technology-base investments, including advanced military research in universities, would suffer losses in excess of $100 million. By contrast, the Reagan proposal seeks nearly $2 billion in spending increases for SDI in 1990 and an additional $1.1 billion in 1991, by which time SDI would cost $6.7 billion a year using the current five-year defense plan as a guideline. (That includes a combined $689 million for initial deployment of the technology in 1990 and 1991.)

Decisions that Bush makes now will set technology policy for at least five years

Ironically, the Pentagon officials announcing the budget took pains to credit the Reagan administration with dramatically increasing R&D expenditures over the last eight years—despite the impending 13% drop in Darpa funding. The increases in R&D spending during the Reagan years are indisputable—defense R&D has almost doubled since 1982 and nondefense R&D is up 50% since then. But critics argue that these increases largely represent spending on SDI, the stealth bomber, and other big-scale programs, while strategic and tactical technologies, such as surveillance and smart weapons, have suffered.

Darpa's 1990 budget plan would cut strategic technology programs by more than $130 million and tactical programs by almost $25 million. Smaller line items would also suffer. The Consolidated DOD Software Initiative, for example, is being cut back 10%, or $3.75 million, to $32.4 million in 1990. As of 1988, it combined DOD's Joint Ada Program Office, the Software Technology for Adaptable, Reliable Systems program, and the Software Engineering Institute into a single Darpa-controlled program.

In addition materials and electronics technology, which includes advanced semiconductor research, is being cut back

by more than $2 million, or roughly 6%.

That doesn't mean Darpa won't seek any new programs in 1990. For the third year running it is trying to get its Infrared Focal Plane Array program off the ground. Darpa sought $45 million in 1989 for the program, which is aimed at dramatically reducing the cost of the IR arrays by developing new manufacturing technologies. It had to settle for less than $9 million when Congress refused to fund it without a more detailed development plan. This year, Darpa is seeking $33 million for the project.

Not surprisingly, virtually the only Darpa programs to have survived unscathed are its high-profile stars: Sematech and the Microwave/Millimeter Wave Integrated Circuits Program. The administration tried to cut both back in 1989 and failed. "I think they learned that we're committed to these programs for the next five years or so, and that we're not going to play any games," says one congressional aide.

In total, the Reagan budget would spend $455 million on semiconductor and fiber-optics research in 1990. The superconductor research total for the year is $287 million, including $47 million from the Department of Energy and another $26 million from the National Science Foundation for high-temperature superconductor work. *–Tobias Naegele*

TAKEOVERS

THE GEC-PLESSEY DUEL: JOUSTING FOR COMPANIES

LONDON

The struggle between Plessey Co. and General Electric Co. is looking more and more like one of those confusing religious wars that made the Middle Ages such a trial. Lords and knights are launching attacks, defending their realms, signing up and abandoning allies, and just generally thundering about the landscape.

What it all will mean for the map of England is exceedingly difficult to say. But clearly, what began as a straightforward takeover bid has turned into transatlantic combat. Depending on who gets what, the end of hostilities could see vast changes in the British electronics industry, and possibly some significant rearrangements among Continental companies, as well.

The tussle began simply enough. In November, GEC and Siemens AG, the West German electronics giant, formed a joint venture called GEC Siemens plc, which attacked Plessey in a hostile takeover attempt. As each side maneuvered, though, other companies in Europe and the U. S. smelled opportunities. They started lining up to support one or the other combatant—or even to make their own takeover moves.

A key move came on Jan. 15, when Plessey counterattacked against an unguarded GEC flank—GEC Plessey Telecommunications Ltd., London. The telecom company is a joint venture between the two that dates back to a more peaceful era (March 1988). Plessey announced that it is beginning legal maneuvers to take over full ownership. It charges that the GEC-Siemens takeover attempt violates certain provisions of the agreement setting up the joint venture, and that GEC is therefore obligated to sell its 50% share to Plessey.

The counterattack came at the opportune moment, tactically speaking. The GEC-Siemens attack had stalled, thwarted by the intervention of the British government's Monopolies and Mergers Commission on Jan. 12. The commission is evaluating the proposed GEC-Siemens takeover to determine whether it would be against the national interest, a process

.ke three months. The Euro-
ıic Community is also inves-
ıee whether the deal violates
ions intended to promote

The move against GEC's share in GEC-Plessey Telecommunications should, if nothing else, buy Plessey even more time. GEC presumably will resist the Plessey buyout attempt, in which case the issue will be tossed into the courts.

The delays appeared to be crucial. After GEC and Siemens made their move against Plessey, a consortium of other companies banded together and announced on Jan. 7 that it would try to take over GEC. If the consortium had succeeded, GEC would of course have been in no position to take over anything, since it would no longer have existed.

But two weeks later, the consortium, called Metsun Ltd., canceled that plan after some major defections. Among them: STC plc, another British company, and General Electric Co. of Fairfield, Conn. This alone would not have been fatal to the consortium's efforts; AT&T Co. and Northern Telecom Ltd. were reported to have been discussing joining Metsun. As telecommunications companies, both would seem to be most interested in owning GEC-Plessey. This might have complicated Plessey's own effort to buy out GEC, but war is a brutal business.

GE's defection was more serious. It didn't just drop out of the battle for GEC, it switched sides. On Jan. 13, GE announced that it would merge with GEC its interests in Europe in consumer products, medical equipment, and some power-generation equipment. (Beyond the coincidence of their names, the two companies are not related.) A combined GE-GEC would have been in a far better position to fight off Metsun.

An anti-GEC consortium fell apart as a key member quit and another switched sides

But all that is just so much blown-away smoke now. It is believed that the Metsun withdrawal was brought about by its ultimate inability to win new allies; speculation in the City—London's financial district—is that AT&T finally decided not to play to avoid straining its relationships with Philips NV of the Netherlands (they have a public-switching joint venture called AT&T Philips Telecommunications). And Siemens, with whom AT&T is reported to be discussing joint ventures in Italy, also no doubt would have been put out.

The intriguing question now is where all of this maneuvering leaves Siemens. The West German firm allied with GEC against Plessey for specific reasons. It wanted to bolster its position in three British markets—telecommunications, medical equipment, and power-generation gear.

By aligning now with GE, GEC could well end up freezing Siemens out of those markets. If Plessey succeeds in buying out GEC-Plessey Telecommunications, or the Metsun consortium takes over Plessey in a white knight's role—as one rumor has it—Siemens probably would get shut out of the telecom market, too.

With all that in mind, more than one observer has suggested that the logical thing for Siemens to do is borrow a leaf from GE and switch sides. Besides giving Siemens a shot at all three of the markets it's interested in, the breakup of GEC could help the West Germans regain Siemens' assets and subsidiary businesses in Great Britain, which were sequestered during World War II.

There is no indication that Siemens is contemplating turning its coat, but the way things are going, no one would be surprised if it did. Meanwhile, perhaps the best advice is that being offered in the City, where analysts are recommending that their clients "sell GEC stock, hold onto Plessey, and buy STC."

–Peter Fletcher and Larry King

WHY AT&T AND INTEL ARE TEAMING UP

BURLINGAME, CALIF.

A new alliance between AT&T Co.'s Microelectronics Division and Intel Corp. could give each company a commanding position as chip suppliers for two markets on the verge of enormous growth. The AT&T division becomes a force to be reckoned with in the fast-growing market segment for 10-Mbit/s Ethernets that run on the common twisted-pair wiring used for telephone lines. Intel Corp. strengthens itself in the integrated services digital network market.

The two companies announced a five-year agreement early this month. The first move under the pact is for AT&T Microelectronics to provide Intel with chip designs for five ISDN devices and two twisted-pair Ethernet devices; Intel is providing designs for two complementary twisted-pair Ethernet devices and one ISDN device.

More important, the agreement establishes a strategic relationship for developing new products, and it unites AT&T and Intel to pursue common goals in standards-committee deliberations. Neither company will comment on those future products, except to say the first will arrive in 1990 and that they also will address the emerging markets for ISDN and twisted-pair Ethernets.

The agreement also shows that even the largest corporations cannot muster the resources and expertise needed to handle the diverse—but quickly merging—technologies of telecommunications and data communications.

From Intel's point of view, "to take on the task of being a telecom giant is almost impossible," says Conrad Weiderhold, general manager of Intel's Microcomputer Group in Folsom City, Calif. "The same is true for AT&T—it can hardly hope to market as broad a silicon line as Intel."

Although the intention of the agreement is to get AT&T and Intel to work together on products, for the first year it boils down to a second-sourcing deal. Intel will concentrate on making the LAN chips and AT&T will fabricate most of the ISDN chips in 1989, says Weiderhold. Both companies, however, are contributing to the development of products.

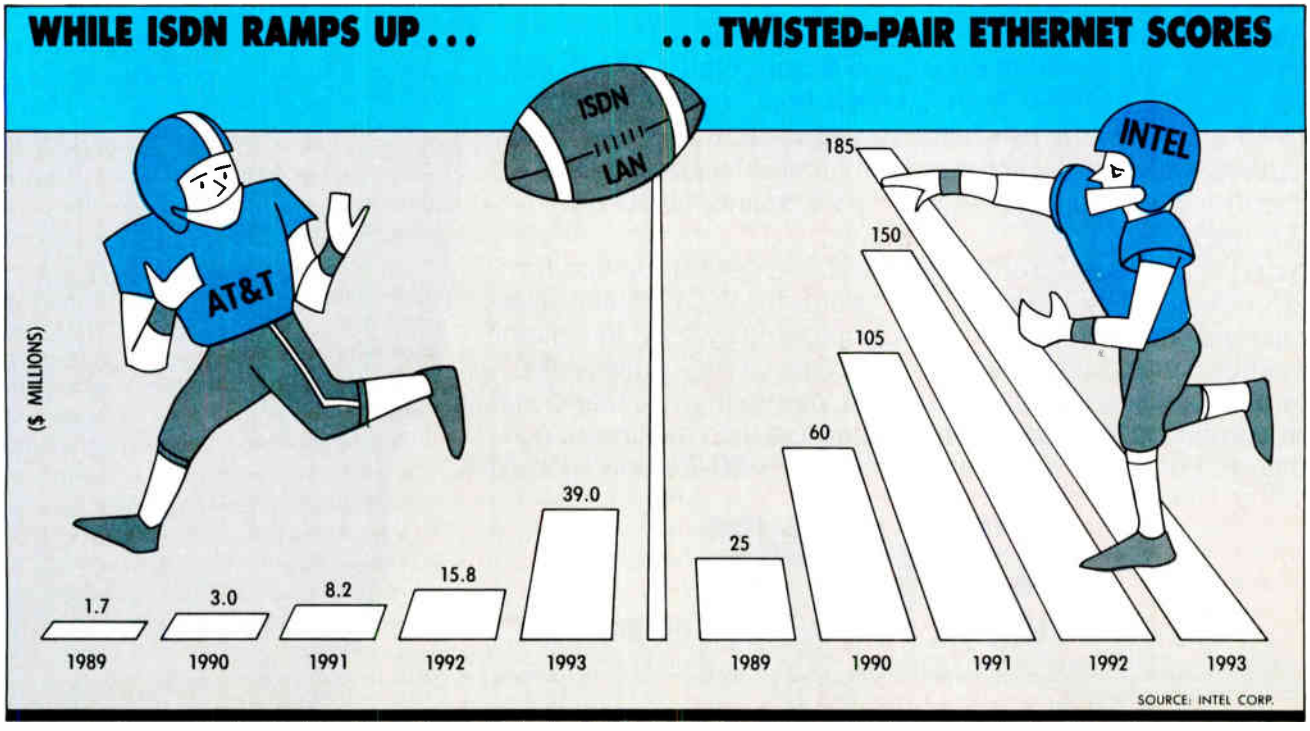
> The duo is staking out the high ground in chips for ISDN and twisted-pair Ethernets

In twisted-pair Ethernet chips, AT&T gains access to Intel's 82586 high-performance controller and 82592 low-cost controller. Intel gets AT&T's T7210 interface-to-twisted-pair line drivers and receivers and its T7200, which implements multiport repeater functions when combined with the T7210. Basically, Intel is contributing the controller chips that work in any Ethernet implementation and AT&T is contributing the retiming chips that will handle the interface to telephone wire. Prior to the agreement, neither company had a complete Ethernet twisted-pair chip set.

The new products will go into a market set to take off. Sales of twisted-pair Ethernet chips—as opposed to end-user products such as controller boards—will grow from about $10 million in 1988 to $185 million in 1993, according to Intel. By then, twisted-pair networks will account for almost half the Ethernets in use, growing from virtually zero last year. The technology will get its real push around the middle of this year, when the IEEE is set to formally approve standards for it. "The ramp will begin next year," says AT&T's Lynn Ditty, who is the product marketing manager for communications devices in Allentown, Pa.

In the ISDN half of the deal, Intel is contributing one S-interface chip, and AT&T is providing two chips for the 1.54-Mbit/s primary-rate service and three devices for the 164-Kbit/s basic-rate service. The primary-rate devices include AT&T's primary-rate framer, which assembles several 64-Kbit/s channels into the faster primary-rate service, along with the Spyder, a 32-channel high-level-data-link controller.

The basic-rate devices include Subat, a two-chip implementation of the ISDN U interface between the central office and subscriber; Intel's S-interface chip between serial devices and microprocessor buses; the Unite S-interface chip between PBXs and network termination devices;



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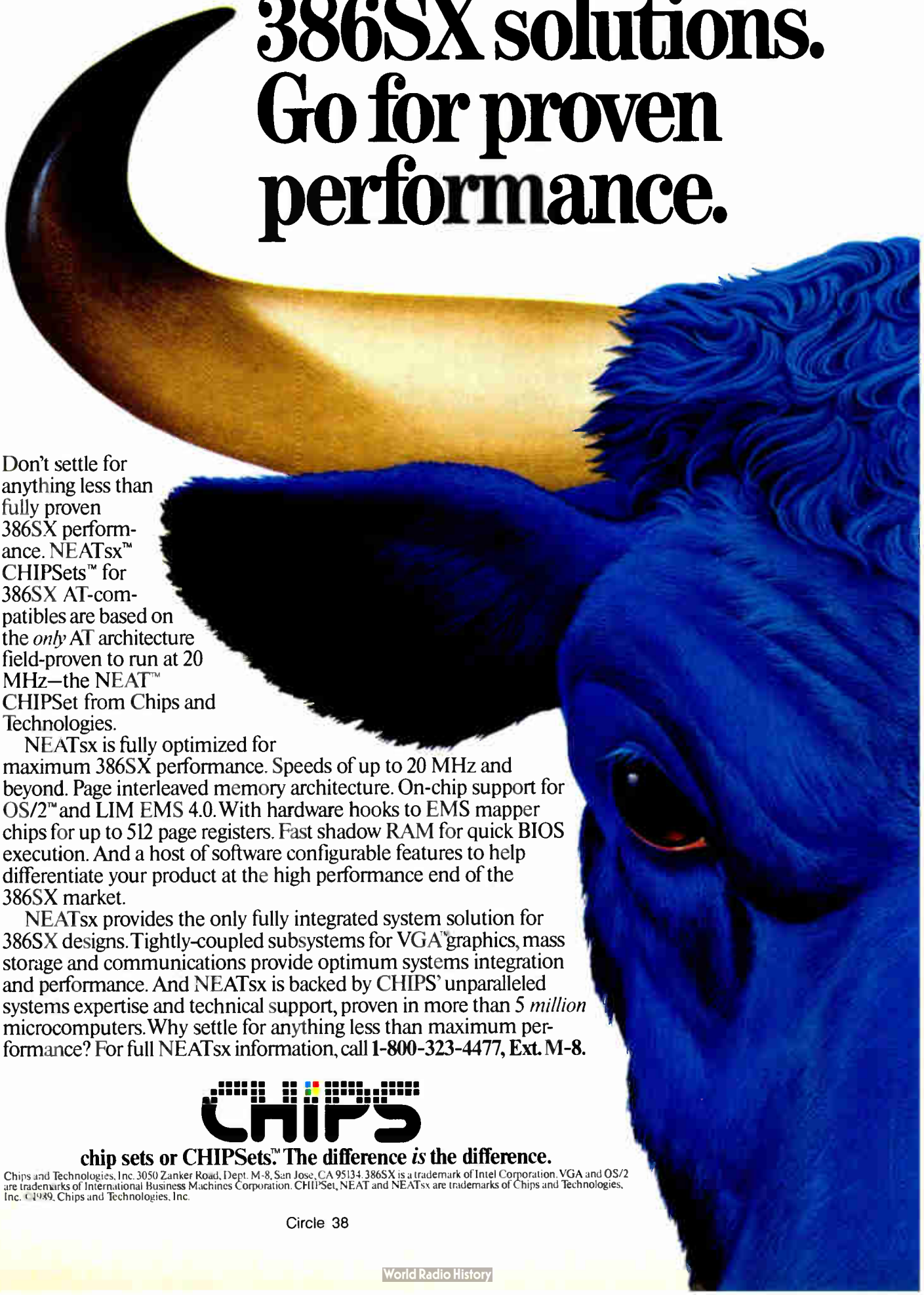

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and a single-channel high-level-data-link controller chip, the HIFI-64.

Intel and AT&T contend the ISDN market is finally poised to take off, now that trials are over and the dust is settling around the ISDN standards. They expect a growth rate of better than 100% annually through 1993. The strongest spurt should come at the end of that period, when ISDN-compatible local phone lines will be abundant.

Since ISDN terminals—PCs hooked directly to the public telecommunications network—will be a major market, the strategic alliance of the leading PC chip maker (Intel) with the semiconductor division of the preeminent U. S. telecom company (AT&T) creates an intimidating market presence. AT&T Microelectronics' Ditty is quick to point out, however, that his organization "is anxious to sell our chips to everybody." The parent company is "just another customer."

ISDN software—the linchpin for compatibility between subscriber-premises equipment and phone company central-office switches—is left out of the agreement. But both companies have subcontracted much of their ISDN software development to the same third party: DGM&S Corp. in Mt. Laurel, N. J. Original-equipment manufacturers using either Intel or AT&T chips "will be guaranteed their products will talk, in this particular case, to the AT&T switch," says Ditty. Compatibility with other switches "will be assured through standards-making activity." *–Jack Shandle*

ROBOTICS

IT MAY GET EASIER TO PROGRAM ROBOTS OFF LINE

ANN ARBOR, MICH.

A long-standing dispute over how to improve off-line programming of robots may be near resolution. The Robotic Industries Association is readying a black-box approach intended to improve the software models of robots used in simulation systems. Better models would mean that any application created on a simulation system could be routinely downloaded onto robots and would run without extensive tweaking. Easier, more accurate off-line programming could, in turn, give the sluggish robot business a needed shot in the arm.

The problem has been disagreement between robot manufacturers and simulation-system vendors over proprietary robot data needed for more accurate software models. Enter the black box, actually a set of specifications to be developed by a committee of the robotic association for writing a software model. A robot maker would write a model according to the specs, then license it to vendors of robot-simulation systems. The model would give all the information the systems need to simulate the behavior of a particular robot. But the proprietary data that robot makers don't want to disclose will be protected by encryption and other means.

Compared with conventional manual programming methods, off-line programming dramatically slashes the time required to get a robot work cell up and operating. This could mean a big boost for robot sales, which grew just 3% in the U. S. last year, to $414 million.

The new RIA Robot Simulation Technical Committee was set to hold its first formal meeting late last month. Including robot suppliers, simulation vendors, and large robot users, the committee's goal is creation of a standard interface and methodology for the exchange of robot modeling information. The group hopes

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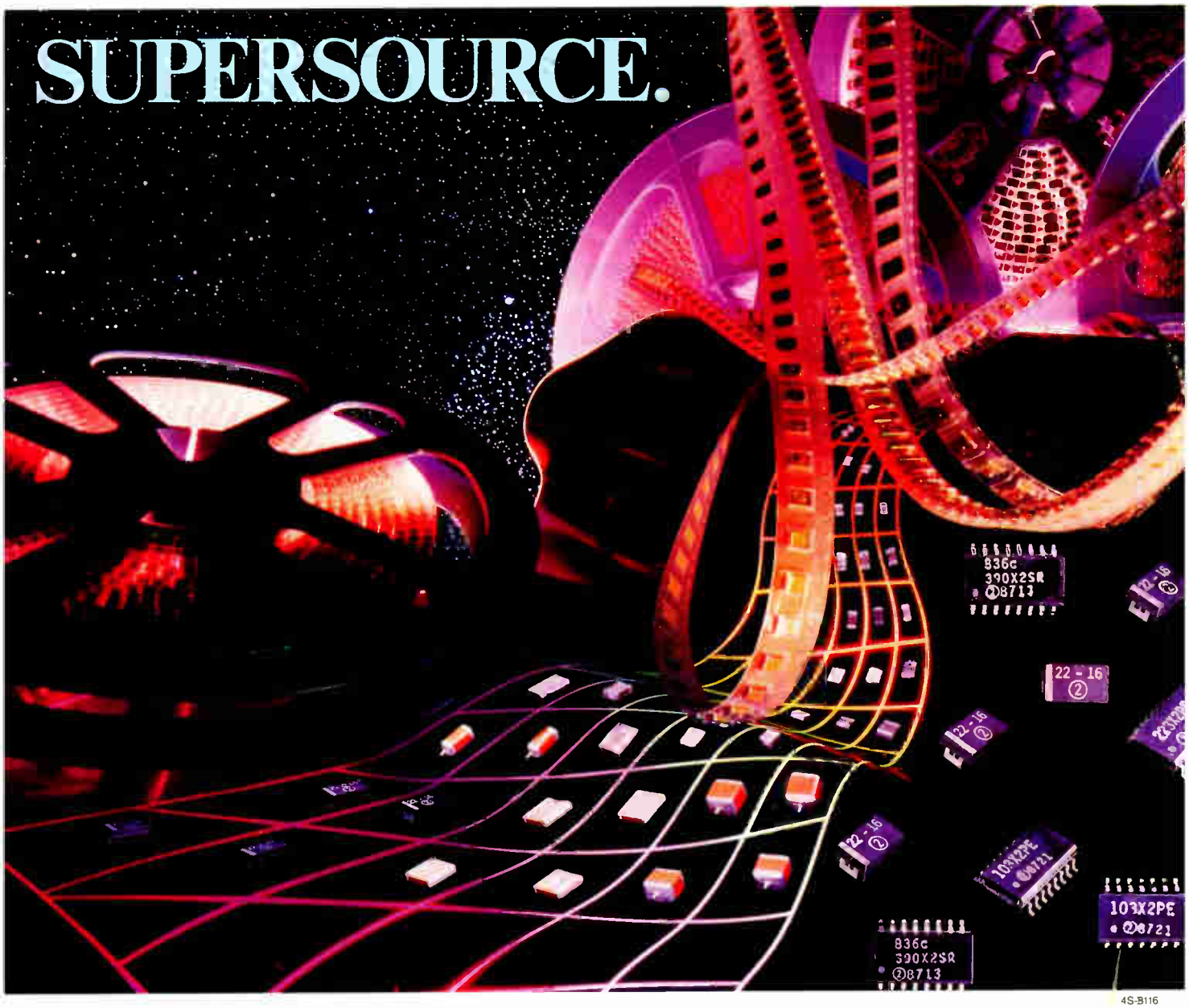

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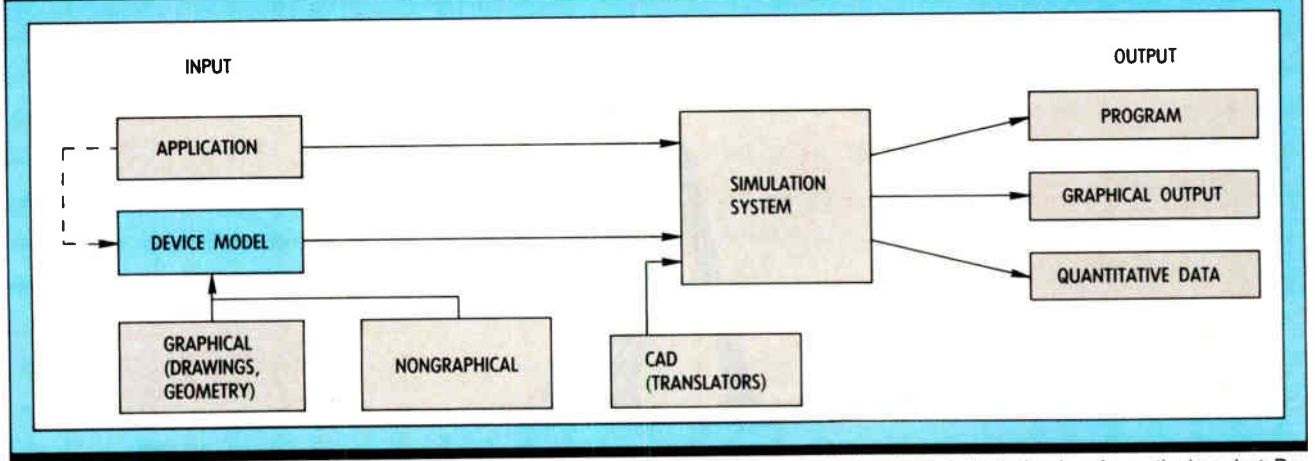
THE BLACK BOX FOR ROBOT SIMULATION



With the black-box concept, a robot maker develops a device model with all the data needed to simulate the behavior of a particular robot. Proprietary data would be protected, and the software would comply with a standard interface that an industry committee is developing.

to develop a workable set of specifications within about 12 months, says James A. Peyton, the RIA's manager of standards development, in Ann Arbor, Mich. "Eventually, we plan to send it through the American National Standards Institute for approval." The RIA group intends to base its work on existing open-system models, Peyton adds.

By coming up with a standard that the vendors of both robots and simulation systems can agree upon, the committee hopes to break the impasse that has so far been a major roadblock for off-line robot programming. The technique could cut by 70% or more the time required to get a robot application program running, proponents say, but fewer than 5% of robots used today are programmed off line. Most users instead still rely on cumbersome and time-consuming manual methods, which require users to shut down a production line while a robot is walked through a routine to learn the program.

The problem is that current simulation systems often aren't accurate. Many robot users use work-station or VAX-based simulation packages provided by any of about a half dozen vendors for the graphic design and modeling of robot work cells. But when it comes to the next step—downloading the application program directly to the robot—the simulation systems of-

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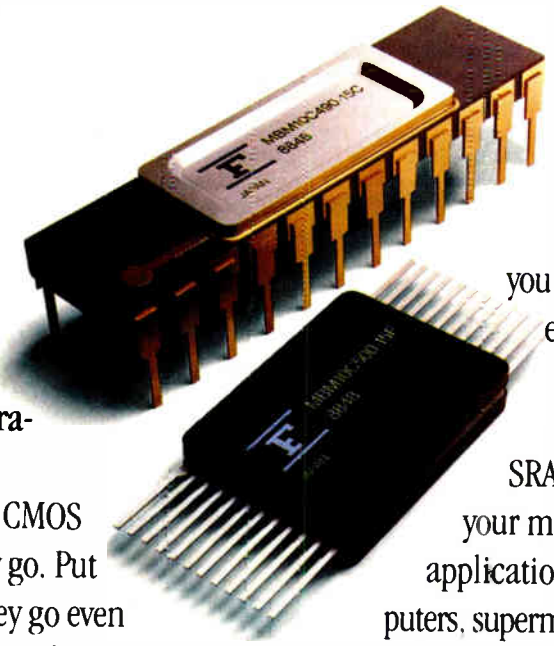

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ten fall short, the robot users say.

Most of the time, programs developed on a simulation system need a lot of work on the factory floor to correct the inaccuracies, says Dave Kase, a manufacturing engineer for General Motors Corp.'s Chevrolet-Pontiac-GM of Canada Group in Detroit. Big robot users, including GM and Chrysler, have been pressuring the robot industry to come up with a solution.

Simulation vendors concede the problems with accuracy. But the real problem, they say, lies with inaccuracies in software models of different robots with which their systems work. The simulation vendors contend that robot vendors are to blame for the poor models, because they won't provide the information needed to produce better ones. "Sometimes we have to spend hours just to get information that they could have picked out of a book and given to us," says Rakesh Mahajan, president of simulation vendor Deneb Robotics Inc. in Troy, Mich.

Robot makers counter that a certain amount of this information is proprietary; they say it will never be revealed to simulation houses. They also complain that simulation vendors sometimes ask for detailed data that isn't even available, or could be provided only at great cost with no apparent payoff to robot makers.

The problem came to a head about 18 months ago, when Deneb, frustrated by the impasse, gathered support from big automotive-industry robot users and invited them and the robot makers to a meeting to discuss the situation. That session produced sometimes-heated public exchanges between robot makers and simulation vendors [*Electronics*, Oct. 15, 1987, p. 32]. But it also produced the black-box idea that sparked formation of the new RIA committee.

SOLVING PROBLEMS. The approach would seem to solve many of the problems. The software model would contain all the information, both graphical and nongraphical, that is needed for the accurate simulation of a given robot. But instead of requiring reverse engineering by the simulation vendors to create the robot models, models would be provided by the robot makers themselves in a protected format. The data would be encrypted and would be provided in object code instead of source code.

Robot makers would maintain the information, be responsible for its accuracy, and make the models available to any simulation vendor under a licensing agreement. By modifying their systems to conform to the standard interface and making other appropriate changes, simulation vendors could plug the models directly into their systems and be assured of an accurate output. The approach would thus give simulation vendors access to the information they need while allowing robot makers to keep crucial information secret. An incentive for the robot makers is a new source of revenue from the model license fees.

The idea looks good on paper, but Deneb's Mahajan is still skeptical that robot makers are serious. "They may be just trying to kill time and believe that the whole thing is going to die off," he says. And he worries that even if the standard is successfully developed, some robot vendors may want to charge exorbitant licensing fees for the models.

Others are more enthusiastic. Licensing fees shouldn't be a hangup, says Guy Potok, a vice president at GMFanuc Robotics Corp. in Auburn Hills, Mich. And he says that GMFanuc, the U. S. robot industry leader, is strongly behind the effort. "I think the concept is excellent," he says. "And I think it's the right forum to get the robot companies and the simulation companies out of the hair-pulling contest they've been in, and into something that's very productive." – *Wesley R. Iversen*

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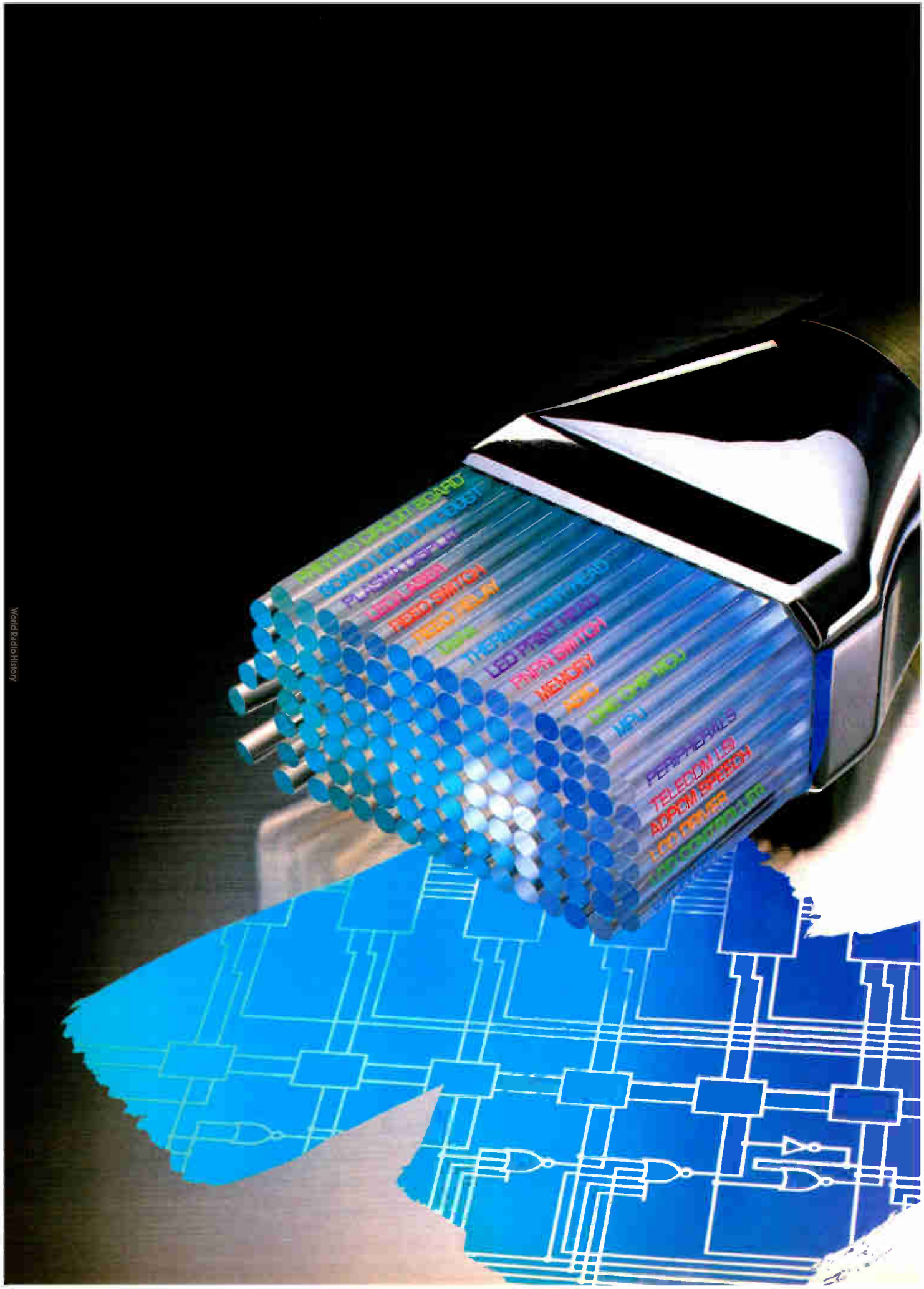

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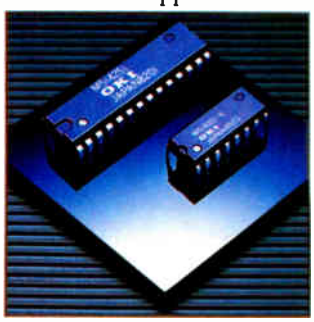

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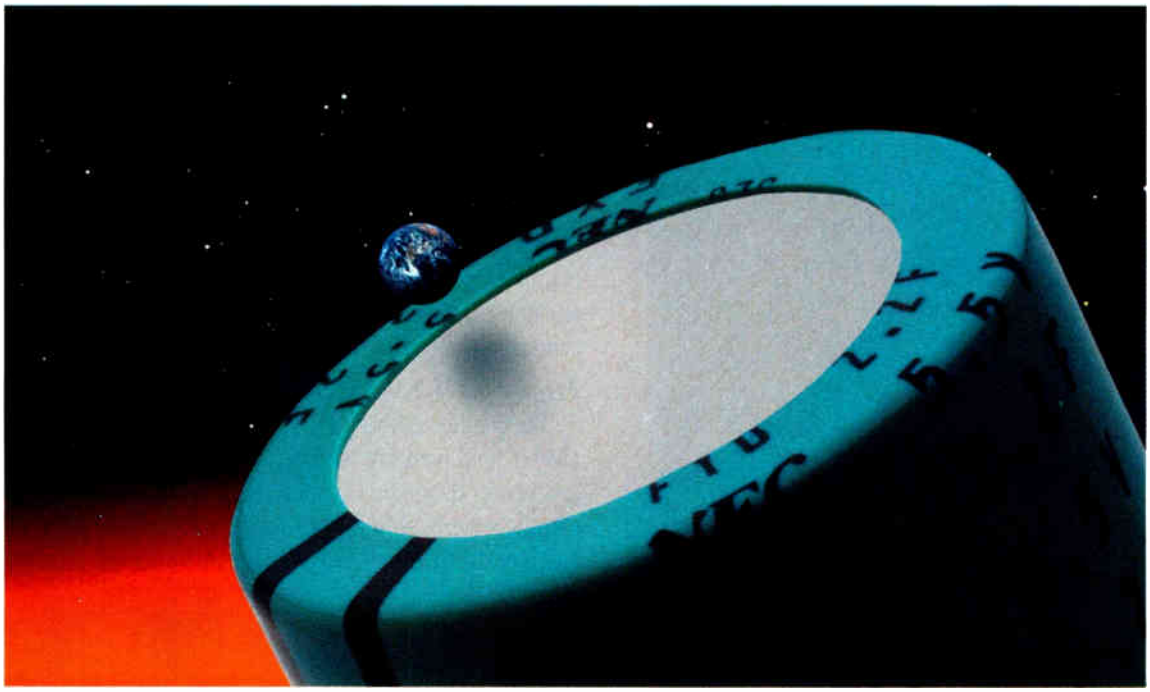

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NEC

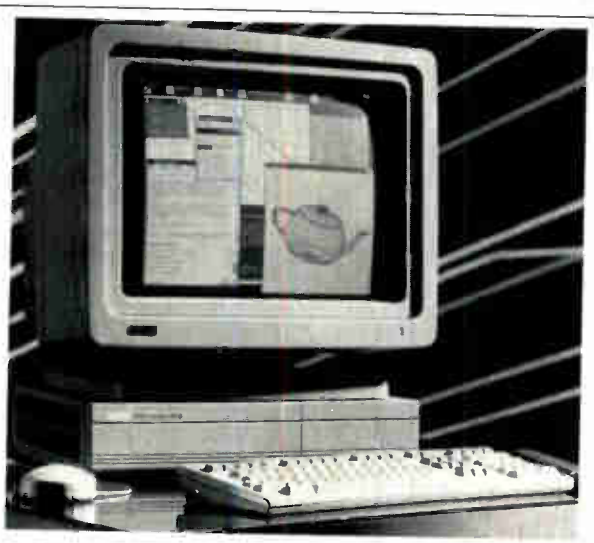
Circle 48

DEC LETS RISC GENIE OUT OF THE BOTTLE

LITTLETON, MASS.

Digital Equipment Corp. let sail a fleet of new products last month. It announced additions to its big VAX superminicomputer line, that it would sell a line of personal computers built by Tandy Corp. of Fort Worth, Texas, and two work stations. The technical community pricked up its ears particularly at the work-station announcements, which included one each of DEC's old kind (a VAXstation) and its new kind.

The new kind is the first incarnation of DEC's move to reduced-instruction-set computing. The DECstation 3100—not to be confused with the new VAXstation 3100, which can run under DEC's VMS operating system—runs only under Ultrix, the company's version of Unix. And it's built around the RISC chips from MIPS Computer Systems Inc., Sunnyvale, Calif.



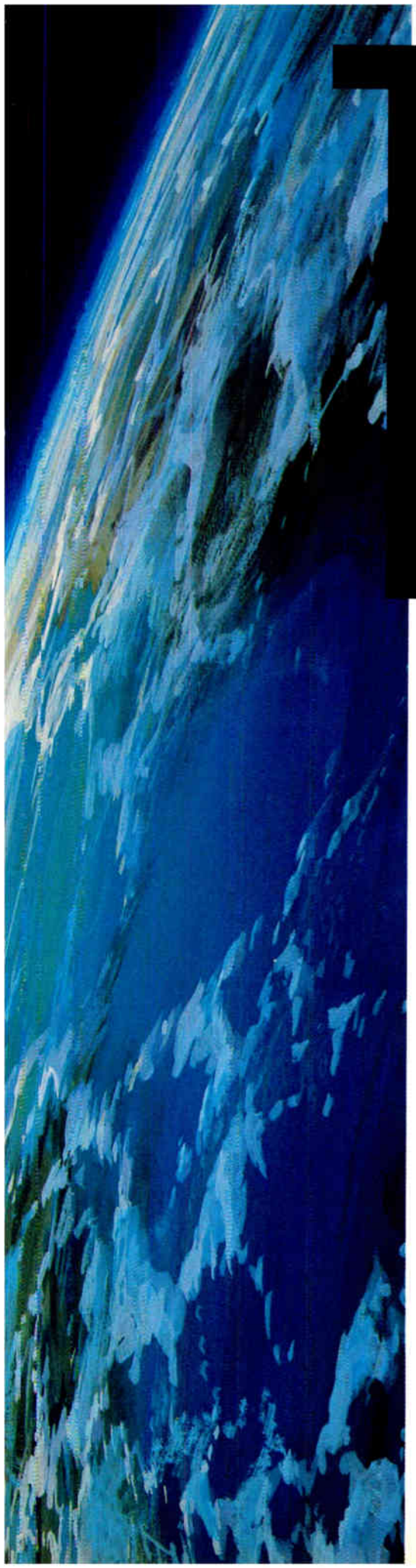
The DECstation 3100, DEC's first RISC machine, offers an unequaled price/performance ratio of $850/mips.

The new machine represents a major broadside at work-station market leader Sun Microsystems Inc. of Mountain View, Calif., offering a major increase in price/performance ratio for the desktop market. But it also proves that DEC has decided it must fight Sun on Sun's own terms with a RISC-under-Unix technical strategy, instead of sticking exclusively to its time-honored proprietary-architecture strategy.

The Maynard, Mass., minicomputer giant has set its sights on becoming the leading supplier of technical work stations, notwithstanding Sun's entrenched position. In fact, some observers think DEC is already No. 2 and that Sun is taking its challenge too lightly.

The RISC machine is very aggressively priced at $11,900. That translates into $850 per mips, considering that the system delivers 14-million-instruction/s performance executing the Dhrystone benchmark. And it's a price/performance ratio that's nothing short of "incredible," says Vicki Brown, senior analyst at International Data Corp., Framingham, Mass. By comparison, she says, Sun's best price/performance ratio is about $2,700/mips.

At the introductory gala in January, Domenic LaCava, vice president for low-end systems, threw down the gauntlet before Sun by naming DEC the fastest-growing work-station vendor around. The company, he says, has catapulted to a spot second only to Sun worldwide.



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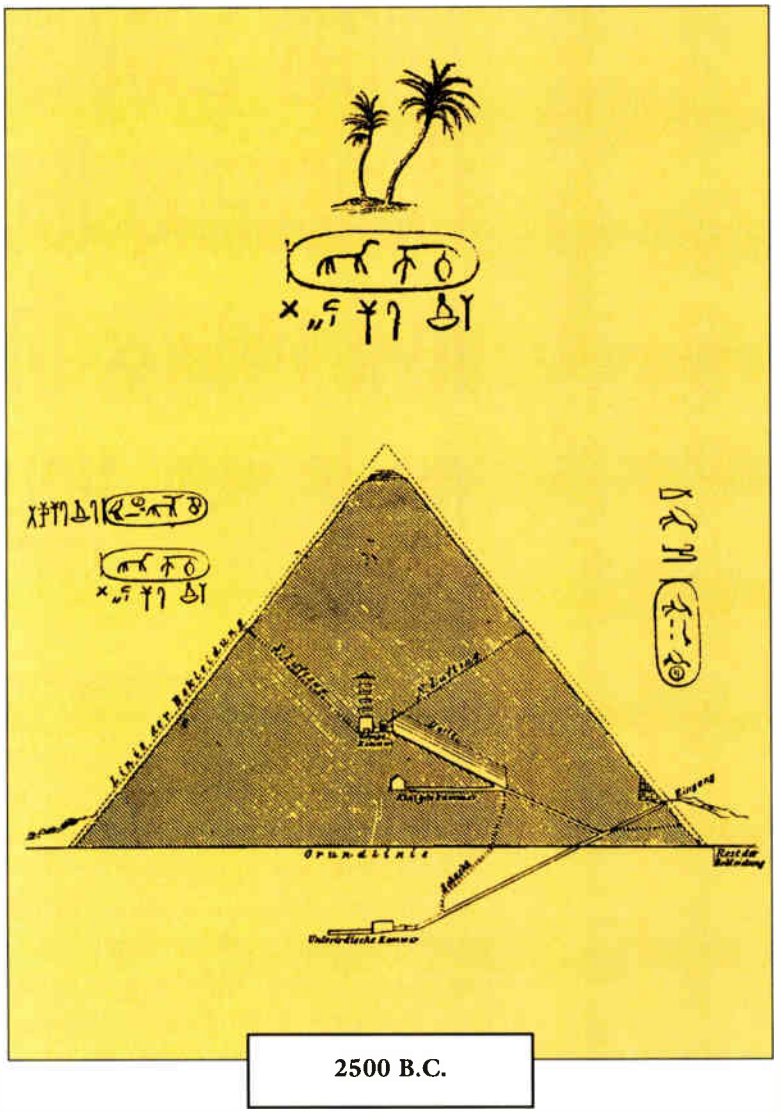

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IDC's Brown, who closely tracks the work-station market, says LaCava's contentions are probably accurate in that DEC most likely finished 1988 as No. 2 in terms of work stations shipped.

"DEC is sending Sun a challenge that Sun is not taking seriously enough," she says. "Sun has become arrogant about its dominance in work stations. DEC and Sun will be beating each other up over this new system, but it's just the first of a series of DEC RISC work stations."

For its part, Sun thinks otherwise. "We think we can beat DEC," says Edward F. Zander, Sun's vice president for corporate marketing. "We don't ever underestimate what DEC, IBM Corp., or Hewlett-Packard Co. can do in the market," he says, and "we're not arrogant. But we're confident and self-assured of our strategy." While he allows that beating DEC "won't be easy, because they'll be aggressive," he says that Sun has a counterthrust of its own. "We have a great year planned at Sun. We'll be there in the front part [of 1989] with some exciting things."

Also, Zander says, DEC's move to RISC and a Unix-based operating system means that "DEC has validated our strategy. We don't have to change strategy; we just have to keep executing. They're doing for us what IBM did for the personal computer industry" by making a strong commitment to RISC.

Use of the MIPS Computer chip set—a central processor and a floating-point processor—represents the first fruits of an affiliation between DEC and MIPS announced last fall [*Electronics*, October 1988, p. 30]. DEC terminated its own RISC development program in favor of the MIPS liaison, with the idea of getting a RISC product on the market fast.

AT THE TOP. Donald McInnis, vice president for DEC's Engineering Systems Group, says that MIPS won out over several other candidates "because we felt they were one of the top two. They also had the best lineup of new chip technology in the pipeline, in both CMOS and bipolar emitter-coupled logic."

The other work station announced last month, the VAXstation 3100, is a $7,950 VAX-based system that runs DEC's VMS operating system. DEC offers no direct comparison between its performance and that of the RISC-based DECstation, but it does say that the VAXstation 3100 delivers about four times the performance of the VAXstation 2000.

VMS software itself came in for some retooling. Version 5.1 includes a new desktop DECwindows user interface to more easily integrate VMS products. Finally, the company came out with a new version of Ultrix Workstation Software, which also includes DECwindows. The program is designed to run on all major DEC work stations, including the new RISC machine. *–Lawrence Curran*

MILITARY

RENEWING A RESOURCE: OLD PARTS SPRING ANEW

WASHINGTON

The industry calls them obsolete, or reduced-demand products. The Pentagon calls them unavailable. Either way, they are a giant thorn in the side of the defense community: low-volume electronic components, fabricated in old-line technologies, that are vital to the upkeep of essential military systems but often don't represent enough of a market to justify their manufacture. Now there are new solutions to this problem. For one, Teledyne Semiconductor, a unit of Teledyne Inc., is betting it can make money manufacturing old lines

Sizing Up the Earth in 200 B.C.

Eratosthenes believed the earth was round. As director of the great library at Alexandria in Egypt, he decided to go beyond abstract argument and actually measure it to back up the argument.


Eratosthenes

Knowing that the midsummer noon sun shone straight down a vertical well in Syene far to the south, he measured the slight angle of the sun's shadow in Alexandria on the same day. He figured the distance between the two cities by how long it took a camel to walk there. Then, with a little simple geometry, Eratosthenes came up with fairly accurate figures for the earth's circumference and radius. His pioneering measurement made a significant impact on history.

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that it buys from other companies. For another, the military itself is shouldering the task of re-creating the circuit functions using up-to-date technology.

Thousands of such parts are discontinued every year, leaving defense officials scrambling for a way to meet future demand for seemingly insignificant parts whose absence can render a $20 million fighter plane impotent. In fiscal 1988 alone, 7,400 of the 1 million parts inventoried by the Defense Electronic Supply Center in Dayton, Ohio, were discontinued. Hundreds more controlled by the individual services suffered a similar fate.

Making matters worse is the lack of a coordinated Defense Department policy for dealing with the problem, says one official at DESC who asked not to be identified. "There's nobody in charge at DOD who's really pulling all these efforts together," he says.

So DESC—or the Army, Navy, or Air Force—must decide on its own whether to buy a lifetime supply, re-engineer the system that uses that component, or try to find an alternate source for the part. Each approach is risky. It's hard to determine how many parts might be needed over a 10-to-20-year system life span. Re-engineering is expensive, and alternate sources aren't always available.

Teledyne Semiconductor has set up a division expressly to address this problem [*Electronics*, December 1988, p. 50]. Teledyne Military and Industrial Logic—Teledyne MIL, for short—will find product lines that no longer make enough money for, say, Motorola Inc. or Texas Instruments Inc., but could still be run profitably in its more streamlined operation. The Mountain View, Calif., firm launched its effort with the purchase from National Semiconductor Corp. of the former Fairchild 10K emitter-coupled-logic family, and division president Mitch Goozé says he's negotiating with virtually every major U. S. vendor for other lines.

HIGHER PRICES? While the defense community applauds such efforts, some experts worry that problems and costs involved with transferring the technology can unreasonably raise the prices. "There's always some risk in having someone else manufacture a part," says Gary J. Smith, an engineer in the Defense Logistics Agency's Production Division. "The environment may be different, and there may be other problems." For example, prices of the parts are likely to rise.

But this after-market approach is limited, because often the military's need for a given part is less than 100 chips a year. In these cases, the best approach may be to re-create the part using more modern technology, says Gary D. Gaugler, chief of advanced technology in the engineering division of the Air Logistics Center at McClellan Air Force Base, Sacramento, Calif. Gaugler founded an Air Force effort two years ago to develop a set of generic device arrays that could be manufactured in a VHSIC process and later personalized to mimic many devices.

So far, his group has produced two such arrays, which differ from gate arrays in that they are not arrangements of gates but of devices—capacitors, transistors, and resistors—that can be chained together to build circuits. The first, the Bipolar Device Array, can mimic 60 part types in the diode-transistor-logic family. The second, the VHSIC TTL Array, can mimic hundreds of 5400-family TTL parts—many of which are still available. "But we have to plan ahead," Gaugler says. "Past solutions were always knee-jerk reactions. This was planned."

The arrays are manufactured by Honeywell Inc.'s Solid State Division in Colorado Springs, Colo., and then shipped to McClellan, where Gaugler's group "personalizes" them on a custom basis. The bipolar array cost $300,000 to develop, Gaugler says, and each design costs about $20,000 to $40,000 to engineer; the TTL array cost $1.5 million to develop, and nonrecurring engineering costs are around $30,000 to $50,000. Once the engineering is done, each part costs only about $50, and the Air Force can make as many or as few as it needs.

"It's a matter of spending $30,000 one time and maybe $50 a part for 100 pieces versus spending millions on a redesign," Gaugler says. *–Tobias Naegele*

INSTRUMENTS

THE FASTEST MICROPROCESSORS WON'T FAZE THIS EMULATOR

REDMOND, WASH.

An in-circuit emulation package that can keep up with today's high-speed microprocessors is coming from Applied Microsystems Corp. The new tool should make it easier to integrate hardware and software in system designs—an increasingly difficult chore with processors that run at clock rates as high as 33 MHz, since most in-circuit emulators can't function in real time at those speeds.

The Applied Microsystems tool also makes it easier to debug software for the newer microprocessors, which tend to be large programs containing multiple levels of nested routines, where bugs can easily hide.

PARTNERSHIP WITH SUN. The Redmond company is teaming up with Sun Microsystems Inc., the Mountain View, Calif., work-station maker, to produce the EL3200 Microprocessor Development System, which can do complex logical evaluations of program executions on targeted microprocessors at full speed—up to 33 MHz—without wait states. The tool has an advanced event system that allows the programmer to probe a target system's program flow for hidden bugs.

The EL3200 consists of two or three elements, depending on configuration. One is a base module, which accepts object code downloaded from the software development system. It performs all triggering and breakpoint functions and controls operation of the second element, a probe module. The probe is located at the target system and linked to the base module over a high-speed, real-time link. The initial EL3200 probe is designed for Motorola Inc.'s 68030; probes for other processors will follow. The third element is an optional overlay-memory module.

Applied Microsystems has struck a deal with Sun Microsystems to jointly market the emulator and a Sun work station, along with the associated software to link them. Future product offerings from Applied Microsystems will extend the emulator's capabilities to a variety of 8-, 16-, and 32-bit microprocessors.

As a stand-alone product, the EL3200 can operate in conjunction with work stations and personal computers running the Unix, VMS, and MS-DOS operating systems, says Richard Jensen, vice president of product development for Applied Microsystems. The unit will sell for around $40,000 depending on configuration, and will be available in the second quarter for evaluation. Production units will be available in the third quarter.

One key to the EL3200's operation is a CMOS application-specific integrated circuit that integrates all the breakpoint logic. The ASIC enables the emulator to evaluate a number of logical conditions and perform a breakpoint in real time—a difficult achievement for other emulators.

Another key is the optional overlay memory. The emulator can use it to record events occurring at every location in the target memory. This history of events makes it much easier for the programmer to trace faults step by step.

Before the EL3200 performs breakpoints or captures the state of a target system in real time, the emulator must be able to make sophisticated logical decision in real time. To make this possible, the EL3200 has an advanced event system. It allows the programmer to specify one or a series of conditions and look for the occurrence of them during execution on the target system. The conditions the programmer can specify include address, data, status, and other outside logical-trigger conditions. *–Jonah McLeod*

DVI MAY BE PROGRAMMERS' NEXT GOLD MINE

PRINCETON, N. J.

Developers of personal computer software who missed the brass ring with PCs a decade ago may get another chance to code their way to fame and fortune. Digital Video Interactive, a technology marrying the PC to full-motion TV-style video, offers virtually virgin territory for independent software developers. As Intel Corp. vice president David House noted at the press conference announcing the Santa Clara, Calif., company's purchase of the technology from General Electric Co. last October, DVI is waiting for the application software that will spur its market acceptance in much the same way that Lotus Development Corp.'s Lotus 1-2-3 software drove the success of IBM Corp.'s original personal computer [*Electronics*, November 1988, p. 32].

By combining more than an hour of video, audio, and graphics on a CD-ROM disk, DVI serves up an appetizing menu of opportunities in training, education, and consumer applications. With all this multimedia power to be harnessed, the development system created by Intel's DVI operation in Princeton confronts the software developer with a new mix of challenges.

The development system consists of a three-board set that plugs into a PC AT or compatible machine, plus two piggyback digitizer boards, system software, authoring tools and developer training. Besides handling the compression/decompression and video display functions required just to run a DVI application, the board set includes audio- and video-digitizer piggyback boards.

The software consists of a real-time operating system, an audio/video data-management system, a graphics library, and a microcode library for paging support, graphics, and video compression and decompression. Among the authoring tools are programs for still-image capture and compression, edit-level motion-video compression and playback, audio compression, and a rich library of microcode development tools.

When Intel purchased the technology, 23 alpha-test sites established by GE/RCA were winding down. Intel has about 20 beta-test sites operating, with 20 more scheduled to start up by April. Intel will not say what it charges a beta site for the development system, but industry observers agree that it is a hefty charge—around $25,000. The same observers expect a major production run of boards in April to alleviate the supply problems. Intel may then unbundle its board set from the training program, and could roll out some enhanced authoring tools as well.

DVI programming presents a steep learning curve. Among the challenges, programmers must master a proprietary windowing system, grasp the use of a microcode library of functions for manipulating bit-mapped images, and handle separate data streams for video, audio, and graphics.

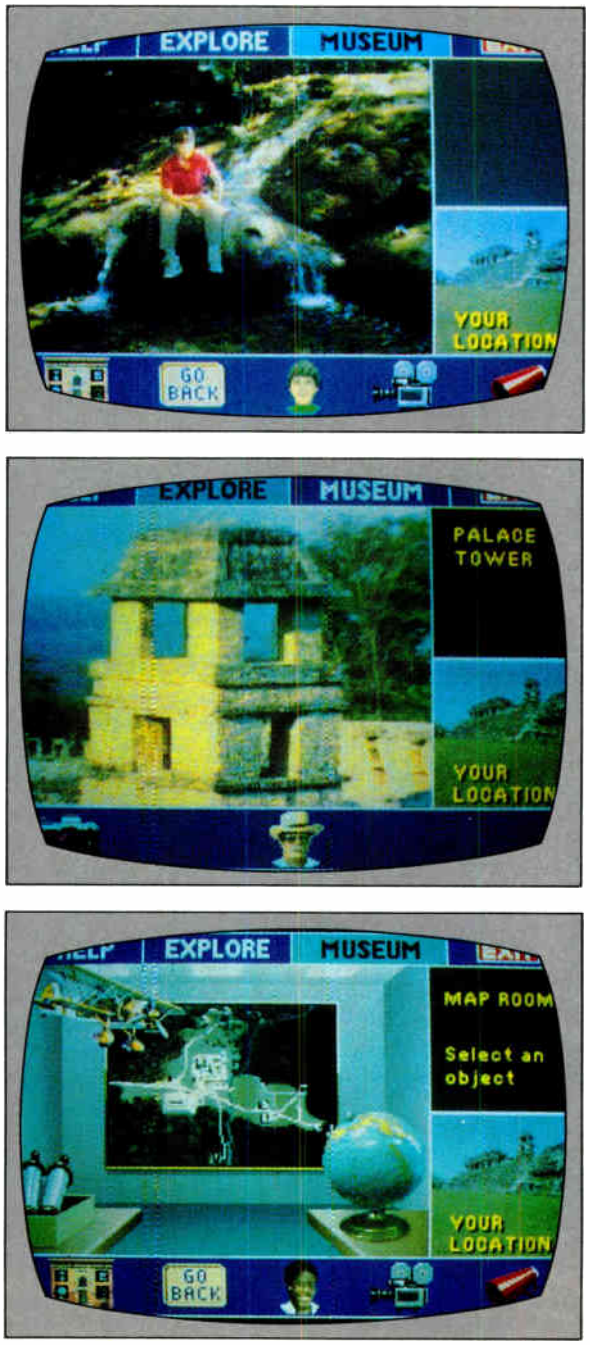
But the biggest challenge to software developers familiar with personal-computer applications lies in a new and virtually uncharted area for most of them: audio and video production, says Dave Ripley, Intel's manager of application market development in Princeton. To surmount the problem of creating interactive-video applications that rise above the quality and interest level of home movies, says Ripley, PC software developers will be making strategic alliances with audio-video experts.

"You need creative people to do all the aesthetic things that programmers in general know very little about," says Peter Wolf, president of Red Shark Software, Cambridge, Mass. For example, Wolf's company has teamed up with Ogilvy & Mather, the New York advertising giant, on several DVI applications, including video-shopping kiosks and a multimedia data base—audio, video, graphics, and text—for the advertising agency's internal use.

"Ogilvy & Mather is a data-rich company," says Jeffrey Woll, senior vice president for corporate development at the agency. "With DVI, we can integrate that data, tying the worlds of sight, sound, and motion together and putting them on the desktop."

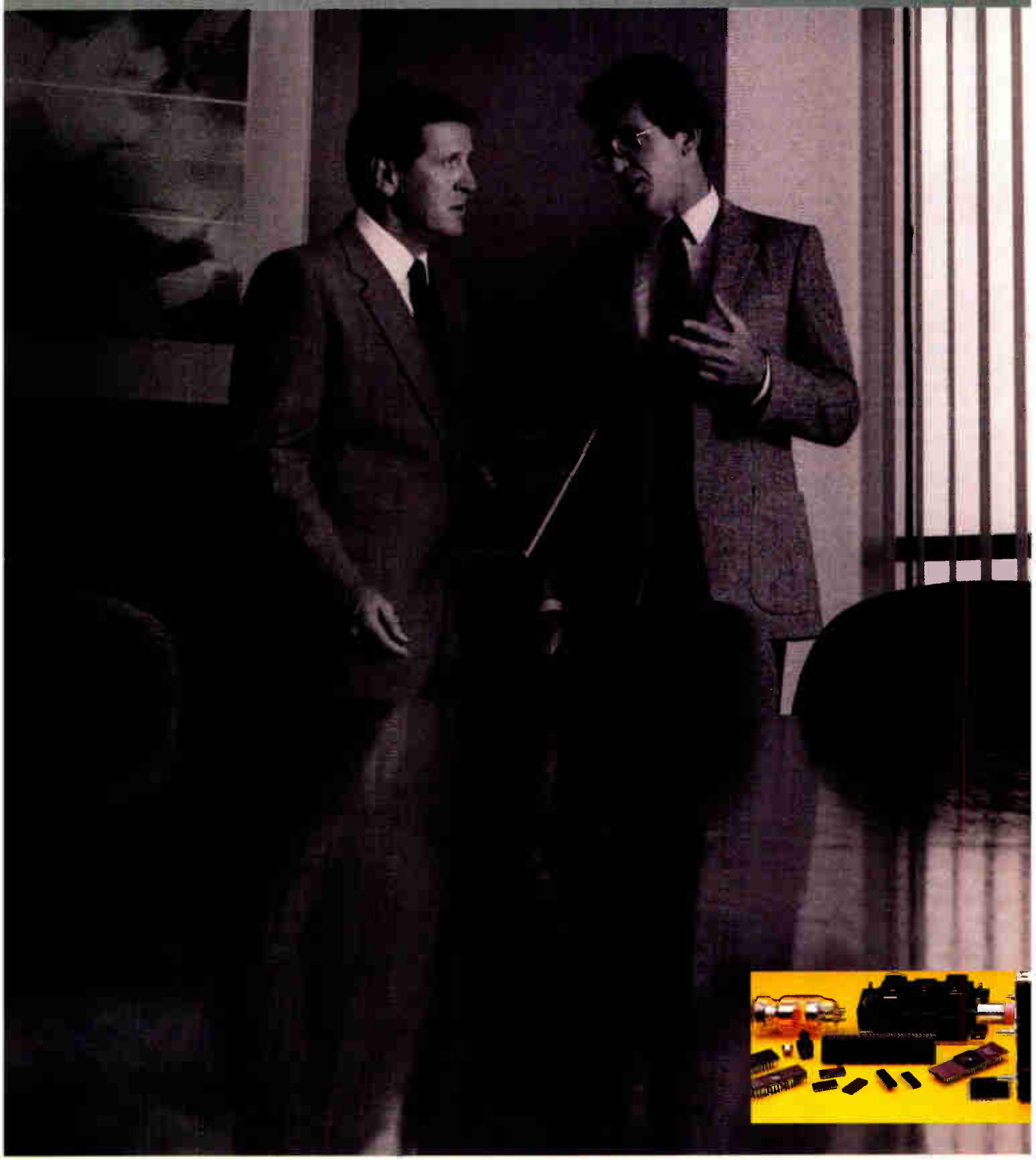
Applications that take maximum advantage of DVI's full-motion, interactive technology are most likely to start with video design concepts, which are foreign to programmers. In one of the most ambitious pilot projects, the Bank Street College of Education in New York created a video tour of a Mayan archaeological site in Mexico. Kathleen Wilson, the project director, created the conceptual design in a series of cartoonlike story boards that represent single frames of specific video segments.

Intended for 8-to-14-year-olds, the program—which is named after the site, Palenque—allows students to make a video exploration of the ruins and a surrounding rain forest, along with what is in effect a museum that exists only on the optical disk. Students browse



A video tour of a Mayan archaeological site includes (top to bottom) the surrounding rain forest, the site itself, and a "museum" that exists only on the optical disk.

"Do we have to have a different supplier for every



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through the program by making choices from menus that appear at the top and the bottom of each screen.

Using DVI's windowing capability, students call particular audiovisual segments from the disk to continue their exploration. They can call up the museum, for example, to learn more about the artifacts they see lying about in the ruins. In the museum's rain-forest room, students can interactively mix sounds in the rain forest by using the cursor to select photographs of the animal or insect that makes each sound.

Wilson's production team consisted of the usual audio-video specialists and programmers along with archaeologists familiar with the site. "To be a project director, you have to be comfortable putting your feet in all those camps," she says.

In the most general sense, the programmer's job is threefold: to create a program architecture that allows the user to move at will from one program segment to another; to combine three data streams—video, audio, and graphics; and to maximize the program's impact by using Intel's library of video-display functions, which manipulate the digitized images from the CD-ROM disk.

30 FRAMES/S. To achieve real-time manipulation of the bit-mapped images, the function library is stored in microcode on the DVI plug-in board. Programmers specify a particular function and designate what part of the bit-mapped video frame it is to manipulate. Since the functions are in microcode, execution of complex bit-manipulation operations can be accomplished at the 30-frame/s speed required for full-motion video.

These microcode routines include graphics-drawing functions for ellipses, rounded rectangles, and 10 varieties of polygons. For color-filling graphics, two-dimensional figures can be Gouraud-shaded or texture-mapped. Three-dimensional images can be z-buffered or texture-mapped. Images can be processed for brightness, contrast, tint, and saturation. Special video effects include warp—in which an image can be wrapped around a 3-d polygon—fade, dissolve, contouring, solarization, and arbitrary 2-d functions.

Still more microcode creates bit-mapped text, including soft fonts and high-quality, anti-aliased text from outlines. Since input data arrives in a variety of media—videotape, audio, and still images—Intel has provided for microcoded format conversions for different pixel-depth formations, color specifications, and pixel resolutions.

Creating a DVI application can mostly be done in-house with Intel's development system, except for the highest-quality video compression and disk mastering. After the conceptual design of an application is complete, videotape or other audio/video media is produced. This video-production phase, says Intel's Ripley, is the most expensive part of the project, typically costing upwards of $500,000, depending on the application.

The video must be digitized before being manipulated by the DVI development system. Digitized audio, still photos, or single video frames can be compressed by the board set at presentation level—that is, at sufficiently high quality for use on the CD-ROM master disk that will be used to manufacture production disks. To achieve the full 120 : 1 compression that is DVI's key technology for producing full-motion video, users must send their videotape to Intel for processing. The development system is capable, however, of real-time compression at a 25 : 1 ratio, which Intel calls edit-level video. Although edit-level video exhibits jerkiness and other deficiencies, it is adequate for the development cycle. Presentation-level full-motion video from Intel is the last step before final test and mastering.

The video digitizer piggybacks onto the standard DVI video board and accepts NTSC video signals. Developers can then superimpose graphics atop the NTSC input. Because the data is written into video random-access memory, it can be displayed on screen immediately. The audio digitizer can handle two audio channels and piggybacks onto the standard DVI audio board. *–Jack Shandle*

CONSUMER

THE GRAY MARKET IS OPEN FOR DIGITAL AUDIO TAPE

LAS VEGAS

With the U. S. mass-market introduction of play/record consumer digital-audio-tape units still blocked by political and copyright issues, gray-market importers are gearing up to capitalize on the situation. The result could be wider retail availability for DAT player/recorders in the U. S., despite objections from the recording industry.

The most visible player is DAT/USA International of Trenton, N. J., which says it expects to deliver at least 5,000 DAT machines into the U. S. market between now and June. And the number "could be closer to 10,000," says Nathaniel Gurien, managing director. What's more, the firm is unperturbed by the possibility of legal action by the Recording Industry Association of America, which has threatened to sue anyone who introduces play/record DAT machines in the U. S. "The chances of the RIAA obtaining a preliminary injunction against us are small," Gurien says.

> Startup DAT/USA plans to ship 5,000 to 10,000 DAT players by June

The RIAA contends that sales of high-quality DAT recorders here could spawn widespread unauthorized pirating of prerecorded records, analog tapes, and compact disks. But the group is taking a "wait-and-see attitude," says Hilary Rosen, RIAA's vice president for government relations in Washington, D. C. "I couldn't really say whether we would or wouldn't [take legal action]," Rosen says; but if DAT/USA sells the kind of DAT volume that Gurien is talking about, "we'll pay attention to them."

The company was formed last November to import and distribute DAT hardware and supplies to U. S. audio stores for sale to the retail market. DAT/USA is associated with American International Audio Video, also of Trenton, which imports the hard-to-get DAT gear for the U. S. professional and government markets, and for mail-order consumer sales.

Through last September, American International had sold about 600 DAT machines in all, primarily to studios and to government agencies, including the Department of Defense, Gurien says. And when it became evident that major Japanese consumer electronics vendors were not going to export DAT products to the U. S. during this year's first half, "we decided to get more serious," he says.

DAT/USA was out to drum up business at last month's Winter Consumer Electronics Show in Las Vegas. The New Jersey importer offers portable and home play/record DAT decks from 13 foreign manufacturers, including big names like JVC, Panasonic, Sharp, and Sony. And Gurien contends that DAT/USA has put together a package that overcomes past retailer objections to gray-market DAT gear. It offers marketing advice, retail orientation, and sales-training seminars. It also delivers its products with the step-down power converter needed for the U. S. market. The price at retail is still high—$2,000 to $4,000. But DAT/USA says Japanese vendors are now introducing lower-priced, third-generation DAT machines for their marketplace.

DAT/USA has so far signed up a few East Coast dealers. Discorama, a New York audio retailer, is already selling DAT machines supplied by DAT/USA, Gurien says. And the company says it's currently negotiating with several regional chains. *–Wesley R. Iversen*

Telecommunications Industry Update

A REPORT FROM THE NETHERLANDS FOREIGN INVESTMENT AGENCY

In 1989, the Netherlands will be one of the first European countries to substantially open up its telecommunications equipment and services market—a response to deregulation and market conditions, globalization, and telematics progress. The Dutch telecommunications equipment market is projected to reach nearly $800 million by 1990, while the European-wide market for equipment and services could exceed $50 billion.

Holland has ensured that its infrastructure—including PTT Nederland which will become a private company January 1 without regulatory responsibilities—will be able to handle not only today's basic speech, text and data exchanges, but tomorrow's needs for fast total digitalization, mobile and other new value-added services.

Here are some examples of Dutch developments in advanced telecommunications services that will be available to consumers, industry and governments.

ISDN Picture Phone—Since 1983, the Dutch have been helping to define the operational standards, compatible with both CCITT and CEPT, for a worldwide small band ISDN videophone terminal. This international effort is being coordinated by the PTT Dr. Neher Laboratories and foresees low-priced picture phones for office and home use in 1992. High-quality moving pictures accompanied by high-quality voice are transmitted over a 64kbit/second network. The bit rate is achieved by data compression techniques that eliminate redundant information using a hybrid method combining DPCM- and transform-coding. Encryption will ensure privacy. To enhance a possible videophone service, high quality videotext images can be transmitted with the same equipment.

Teleports—Designed jointly by Rotterdam's municipal authorities and its business community, the teleport uses the International Transport Information System (INTIS) for the electronic exchange of standardized messages between shippers and suppliers of all modes of transportation. Shippers and freight forwarders already access the network to send shipping instructions to deep-sea carriers and liner agents. They, in turn, communicate electronically with container terminals. Both PCs and mainframes, equipped with a 3780 emulator and a V22bis modem, can access the network. Access by X.25 protocol will be available soon. Amsterdam is also developing a teleport.

Transportation Databases—A standard IBM SNA system with videotext is providing more than 1,500 subscribers throughout Europe with cost savings and real-time information about space availability, type of cargo handled, destinations, departure and arrival times for trucks, trains, ships and airplanes throughout Holland. Called Transpotel, this Dutch database service has expanded through franchising to the United Kingdom, Switzerland, Belgium, Austria, France, Germany and Scandinavia, and soon will extend to Italy and Denmark.

In addition, Holland is a major manufacturing location not only for N.V. Philips's data communications products, but also for Alcatel, N.V., which builds and markets its System 12 for small and medium-sized firms; for Swedish multinational L.M. Ericsson, which manufactures telephones for the Dutch PTT and other telecommunications equipment; for West German multinational Siemens, which produces data communications products; and for the AT&T/ Philips joint venture, which is building a new generation PBX.

Further, three technology universities—at Delft, Twente and Eindhoven—and more than 100 technical institutes along with the Netherlands Organization for Applied Scientific Research (TNO) and major software houses assist companies, regardless of location, with research and development from defining systems needs to designing networks to building prototypes or writing code.

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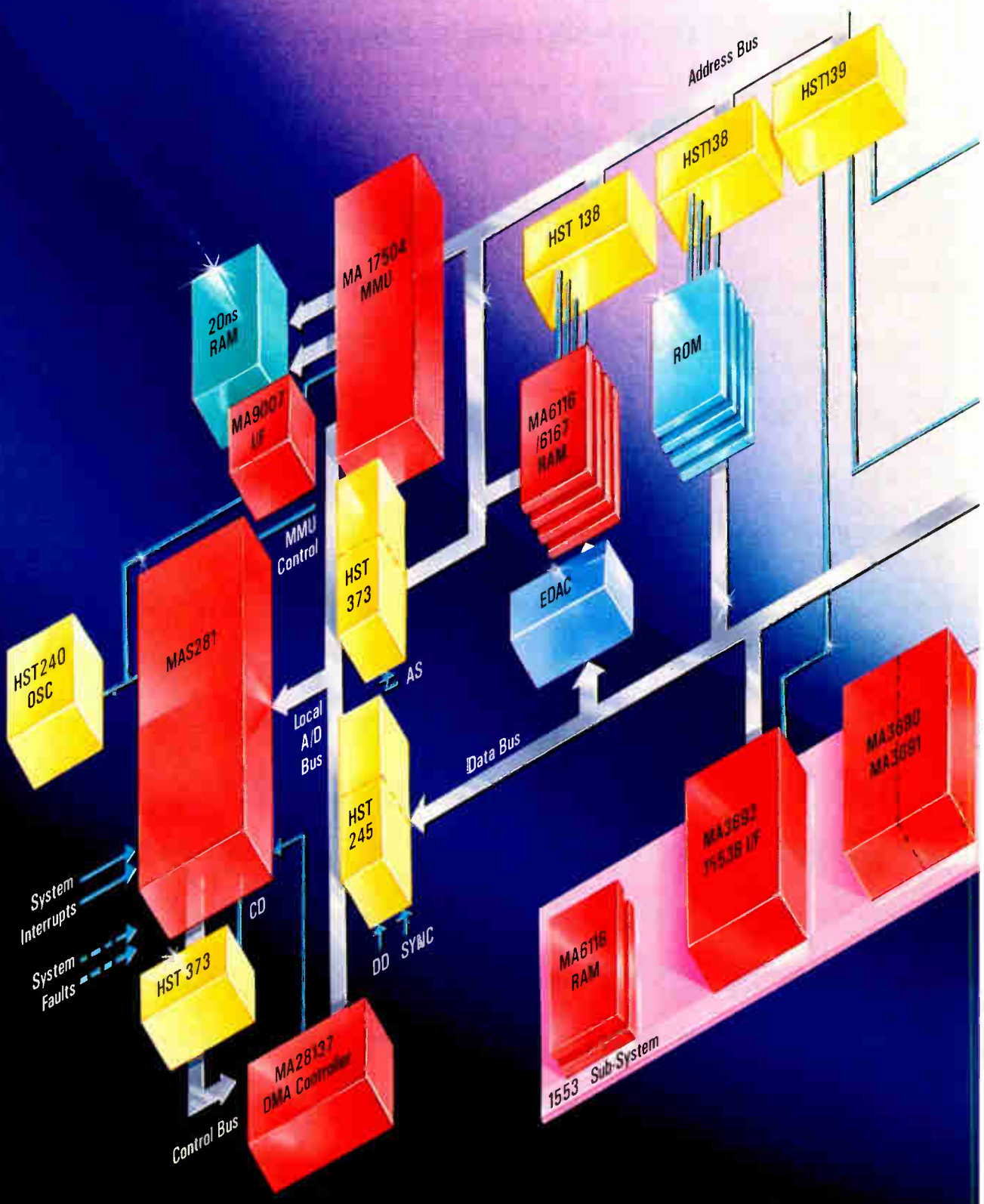

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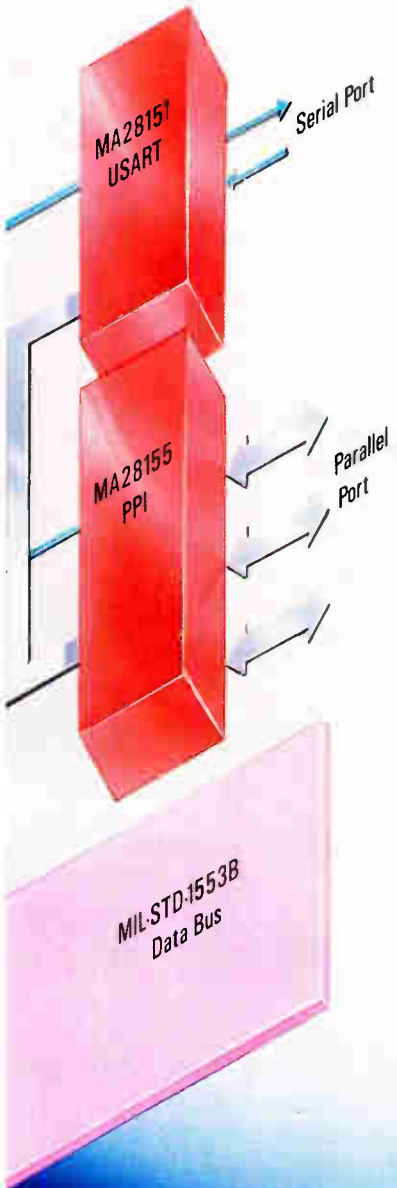

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WASHINGTON INSIDER

EQUIPMENT MAKERS ARE ASKED TO STIMULATE U. S. DRAM PRODUCTION...

The American Electronics Association wants to get systems houses to prod U. S. chip makers back into the dynamic random-access-memory business. So by next month, the AEA will produce a model request for proposals that spells out ways the equipment makers can sweeten the pie by sharing the chip makers' burden of investment and risk. "We'll send the RFP to systems companies, and then they can modify it or whatever and send it off to potential producers," says William K. Krist, vice president for international trade affairs at the AEA in Washington. "The systems companies want increased U. S.-based DRAM production—we're still in a period of real shortage." U. S. companies were forced out of the DRAM business in the mid-1980s, when foreign competitors started dumping the devices on the market below cost. But Krist says the government won't let that happen again and that systems companies, hungry for a broader supplier base, "may be interested in assured-purchase agreements or some other type of risk sharing. What you have here is the customer crying out for more production, and they are willing to help pay for it." □

...AND, WITH CHIP MAKERS, MAY HAVE A NEW SOLUTION FOR PRICING

After more than six months of debate between systems houses and chip makers over how to change the fair-market-value pricing system used by the Commerce Department to guard against dumping by Japanese DRAM producers, the two groups are starting to see eye to eye. The Semiconductor Industry Association and the American Electronics Association are expected to jointly recommend that the government change the way it determines fair-market value for new generations of products, for which prices can fluctuate wildly during the early months of production. Systems producers have been concerned that when 4-Mbit DRAMs become available, unpredictable price changes might cause the Commerce Department to penalize their suppliers, thereby affecting availability. Sources familiar with the SIA-AEA discussions say the groups will soon give the Commerce Department a new formula that takes into account yield fluctuations and production-line down time, along with the R&D and depreciation costs previously included, as problems associated with bringing up new technologies. Says an SIA insider: "This would be a more deliberate method of spreading out startup costs." □

WILL CONGRESS TAKE ON SOME RISK IN HDTV GAMBLE?

The U. S. electronics industry has been pushing Congress for the last eight months to support a federally aided drive to regain a share of the worldwide consumer electronics market, but so far it has been able to attract only modest support. The reason? "The TV industry—the electronics industry—hasn't come together," says one congressional aide familiar with the issue. Now that could be changing. The American Electronics Association has rallied the financial support of 20 member companies to develop a business plan for a federally aided, for-profit HDTV company. On the roster are such industry giants as AT&T, Digital Equipment, Hewlett-Packard, and IBM, among others. The plan, which will be developed by an outside contractor, should be completed by March, says AEA vice president Pat Hill Hubbard. But it won't focus solely on technology. "The technology question is not the biggest hurdle in this thing," Hubbard says. "The problem is reducing the level of risk so that investment [in HDTV] makes sense." That means some combination of loan guarantees, tax credits, antitrust waivers, and direct federal aid will be at the heart of the proposal. And the companies want something more: "Unless there is an assurance that the government would enforce its antidumping laws," says Hubbard, "these companies aren't interested." □

WASHINGTON INSIDER

WILL THE LAST MAJOR U. S. WAFER MAKER SLIP INTO FOREIGN HANDS?

Semiconductor industry insiders are up in arms after an interagency government panel, the Committee on Foreign Investment in the U. S., cleared the way for Monsanto Co. to sell its Electronic Materials Division in Palo Alto Calif., to a West German chemicals concern, Huels AG. The division is the last major independent manufacturer of silicon wafers in the U. S. owned by an American firm, and the sale "is a darned shame," says Charles Sporck, president of National Semiconductor Corp. Officials at Sematech, the government-industry chip consortium, say they view the deal "with alarm." But Monsanto, of St. Louis, Mo., which has been trying to sell the division for the last year, says it had little choice. "No other viable offers were made," says Joseph F. Dennin, Monsanto's Washington attorney. "We don't believe there were any established firms out there that had guaranteed financing" or would offer indemnities against possible future claims on the division for environmental damage, which Monsanto was seeking. Monsanto did get three offers from U. S. companies, says Denin, but "they were all leveraged-buyout-type deals—plus one required a government guarantee and one was conditioned on closing one of our plants. They weren't stable." The issue is still alive because the council's decision is just a recommendation. The final decision rests with President Bush. □

REGULATING DOD CONSULTANTS: HOW MUCH DISCLOSURE IS ENOUGH?

The Office of Federal Procurement Policy proposed new rules late last month regulating consultants who do business with either the government or its prime contractors—but Congress is already complaining that the regulations are not strict enough. The proposed rules require consultants to disclose only foreign clients, not domestic ones. Congressional critics complain that such a policy leaves gaping the very loophole that the OFPP was told to seal—a consultant's ability to work for two competing contractors at once and thereby obtain sensitive bidding information that can make or break a bidder. Sen. David Pryor (D-Ark.), who has campaigned for regulating consultants for more than a decade, didn't even wait for the OFPP to release its rules. He has promised to reintroduce a measure that would force consultants to divulge all current and former clients, as well as details of the nature of the work performed for them. His push for the bill last fall failed, surviving only as an amendment to the 1989 Defense Authorization bill that directed the OFPP to come up with its regulatory solution. □

AEROSPACE GROUP PLANS A 'KEY TECHNOLOGIES' DATA BASE

The Aerospace Industries Association plans an on-line data base on leading-edge research efforts in such high-technology areas as artificial intelligence and ultra-reliable electronics. "We'll build a data base of accessible information on what's going on: who's doing what and how much money is being spent," says Dick Hartke, director of technology programs at the Washington-based industry group. One important ingredient will be road maps for developing the "key technologies for the 1990s," an ambitious effort on which tasks forces of the aerospace group are working. Besides these road maps, the data base, tentatively called the National Center for Advanced Technology, will include information about which companies and laboratories are involved in particular research-and-development topics, and which companies and government agencies are in the market for those technologies. It will also try to include other technology data bases, such as those offered by the Strategic Defense Initiative Organization and several state governments, including those of New Mexico, New York, and Ohio. It will take about a year to get the data base up and running. □

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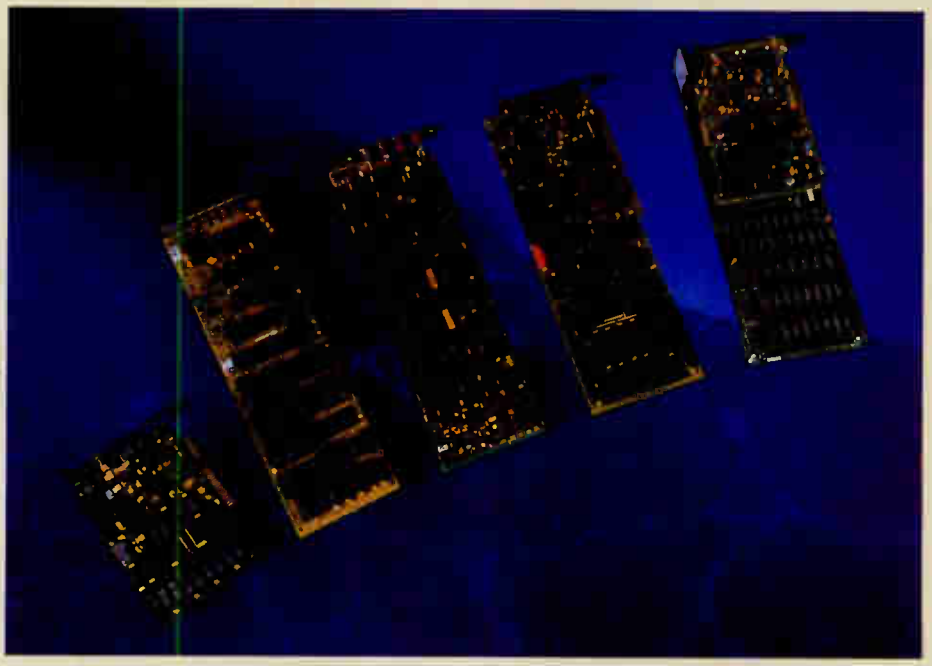

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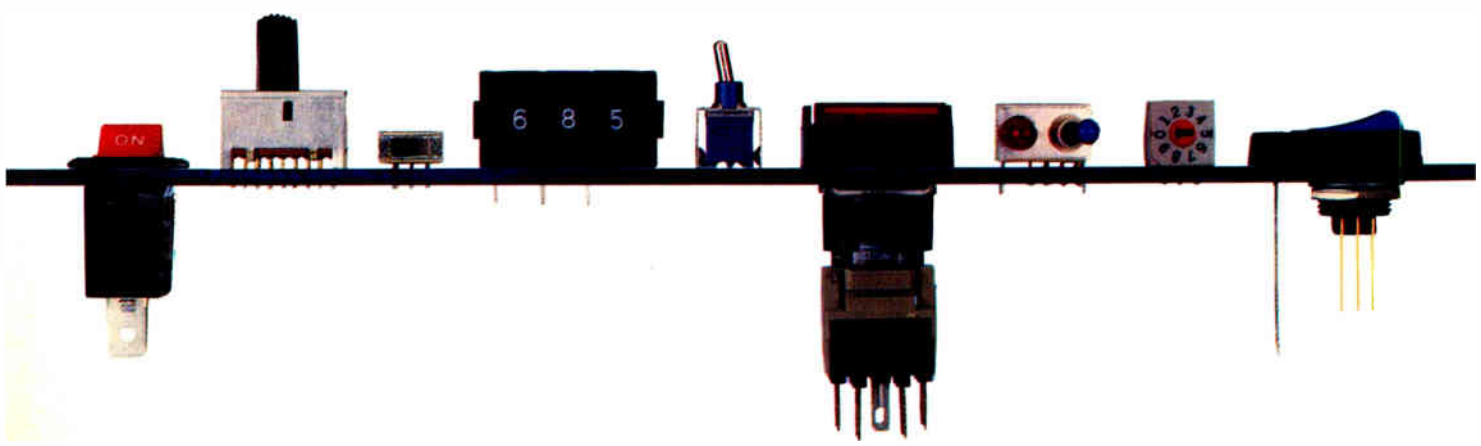

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PACIFIC RIM TRENDS

NTT REPORTS DRAMATIC ADVANCES IN OPTICAL DATA TRANSMISSION

Researchers at Nippon Telegraph & Telephone Corp. say they are well on the way toward a hotly contested goal: the development of many of the basic technologies needed for coherent optical communications systems. Such systems will use parallel transmission of multiple data streams in the same fiber, giving greater capacity than is possible by merely increasing the speed of a single data stream. Among the NTT developments is a monolithic array of 20 distributed-feedback laser diodes, each operating at a differnt frequency. The pitch of the frequency-determining grating of each diode is generated by electron-beam lithography and replicated by synchrotron radiation lithography. Also notable are a periodic-filter demultiplexer with a tunable optical waveguide, and a completely optical synchronization circuit for exchanges. NTT has demonstrated a system with eight channels of 400 Mbits/s each—twice the capacity of the fastest system now in use, 1.6 Gbits/s. □

A NEW JAPANESE CONSORTIUM PLANS TO DEVELOP FUZZY COMPUTERS

A government-industry consortium led by the Ministry of International Trade & Industry will set up an institute for research and development of fuzzy computers, the still-theoretical machines that go beyond simple "yes" and "no" answers to add a "maybe." The Yokohama institute, to be called Laboratory for International Fuzzy Engineering Research, will cooperate with government laboratories, academia, and foreign research organizations. Its goal is no less than the fabrication of a computer for fuzzy-logic applications. The estimated six-year budget of $37 million will come from some 40 companies, including three affiliates of non-Japanese firms—Yamatake-Honeywell, Nippon Thomson, and Fuji Xerox. Japanese members include Hitachi, Toshiba, Toyota, and Yamaichi Securities. □

IBM AND DEC IN JAPAN GET A FOOTHOLD WITH NTT-SPONSORED PROJECT

There have been complaints from the U. S. that Japan's Nippon Telegraph & Telephone Corp. isn't trying hard enough to increase its purchases from Yankee vendors. Now NTT has enlisted two Japanese subsidiaries of giant U. S. companies to work with three Japanese counterparts on a multivendor systems-integration architecture that should put them on equal footing as suppliers with NTT's three traditional computer vendors—Fujitsu, Hitachi, and NEC. The pair, IBM Japan Ltd. and Nihon Digital Equipment Corp., and the three Japanese suppliers will do the work for NTT Data Communications Systems Corp. of Tokyo. Recently spun out of NTT, it is Japan's largest computer buyer and largest integrator of on-line systems. The two-year project has three major goals. First is development of an application interface that includes common system calls, data format, programming languages, and data-base-access languages. Second is creation of an interface between systems that includes a data-transfer format, channel interface, and open-systems protocols. And third is development of a man-machine interface that includes a display layout, command language, and icons. □

NEC PUSHES EUROPEAN CHIP PRODUCTION AS 1992 LOOMS

The time remaining until the 1992 launch of a European Community free of internal barriers is growing short, so Tokyo-based NEC Corp. is accelerating the transfer of semiconductor production to its plants in the UK. For example, the company is considering making microcomputers at NEC Semiconductors UK in Livingston, Scotland, which now fabricates 256-Kbit and 1-Mbit dynamic random-access memories. The Scottish firm is the only Japanese operation in Europe that has a wafer-fabrication facility. NEC is also considering making application-specific integrated circuits and logic ICs at this plant. □

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EUROPEANS HAMMER OUT THE FINANCIAL DETAILS FOR JESSI

Jessi is shaping up, at least financially. A proposed $7.6 billion budget calls for dividing the Joint European Submicron Silicon Initiative into four subprograms. An applications subprogram will get 34% of the funding, mostly for computer-aided-design tools. Chip technology will account for 29%, with the emphasis on CMOS memories, logic circuits, and production engineering. About 15% will go for the materials and equipment subprogram, which will stress lithographic apparatus and systems like ion implanters, plus work on testing and clean-room engineering. The remaining 22% will be spent on research aimed at improved design methods, process integration, new manufacturing techniques, and modeling and simulation. The Jessi budget was thrashed out by some 60 experts from 30 corporations and institutions, representing the six European countries involved so far in the eight-year program—Belgium, France, Italy, the Netherlands, the UK, and West Germany [*Electronics*, September 1988, p. 52]. Jessi officials expect government approval to come soon enough so that work can start by mid-1989. □

ANOTHER ALLIANCE: SIEMENS BUYS MAJORITY SHARES IN FRANCE'S IN2

Another strand is being added to the web of mergers, acquisitions, alliances, and joint ventures that Europe's electronics industry is weaving. France's Intertechnique SA is accepting an offer from West Germany's Siemens AG to acquire a majority interest in Intertechnique's affiliate IN2 for an undisclosed price. Paris-based IN2 makes small and medium-size personal-computer and minicomputer systems. For Siemens, the majority acquisition means an expansion of one of its core businesses, the $5.5 billion Data and Information Technology sector. It also means a return to the French computer market, 14 years after the breakup of the ill-fated French-German-Dutch Unidata computer combine. □

INTERMETALL'S NEW AUDIO CHIP SET LURES A MAJOR U. S. CARMAKER

A new three-chip set for audio applications is hardly out of development at ITT Semiconductors Group, but one major user has already grabbed it. ITT says a U. S. auto and auto-radio manufacturer has signed up to buy the chip set from Intermetall GmbH in Freiburg, West Germany, the group's lead house. It won't identify the client, but industry sources speculate it's Chrysler. The carmaker is committed to deliveries in "seven-digit numbers a year for several years," according to Intermetall. The chips were announced in November at the Electronica Components Show in Munich; they will go into volume production this year. The three VLSI circuits cover all signal-processing functions in both the radio-frequency and the audio-frequency ranges. □

THIS AGC AMP CAN KEEP UP WITH 2.5-GBIT/S OPTICAL-FIBER SYSTEMS

Researchers with their eyes on Europe's next generation of optical-fiber data-transmission systems have developed a linear automatic-gain-control amplifier on one chip that operates at up to 3 gigabits/s—fast enough to handle the 2.5-Gbit/s transmission rate of the fiber systems. The bipolar silicon circuit also features a dynamic range up to 40 dB and a maximum gain of 40 dB. The developers say no other such single-chip silicon amp combines as high an operating speed with so large a dynamic range. The combination of a conservative 2-μm process and the single-chip architecture will make the device inexpensive and easy to use, according to the developers, Hans-Martin Rein and Reinhard Reimann at the Ruhr University in Bochum, West Germany. The pair have a good track record in producing real-world designs, so there's a good chance the amp will become a commercial product. □

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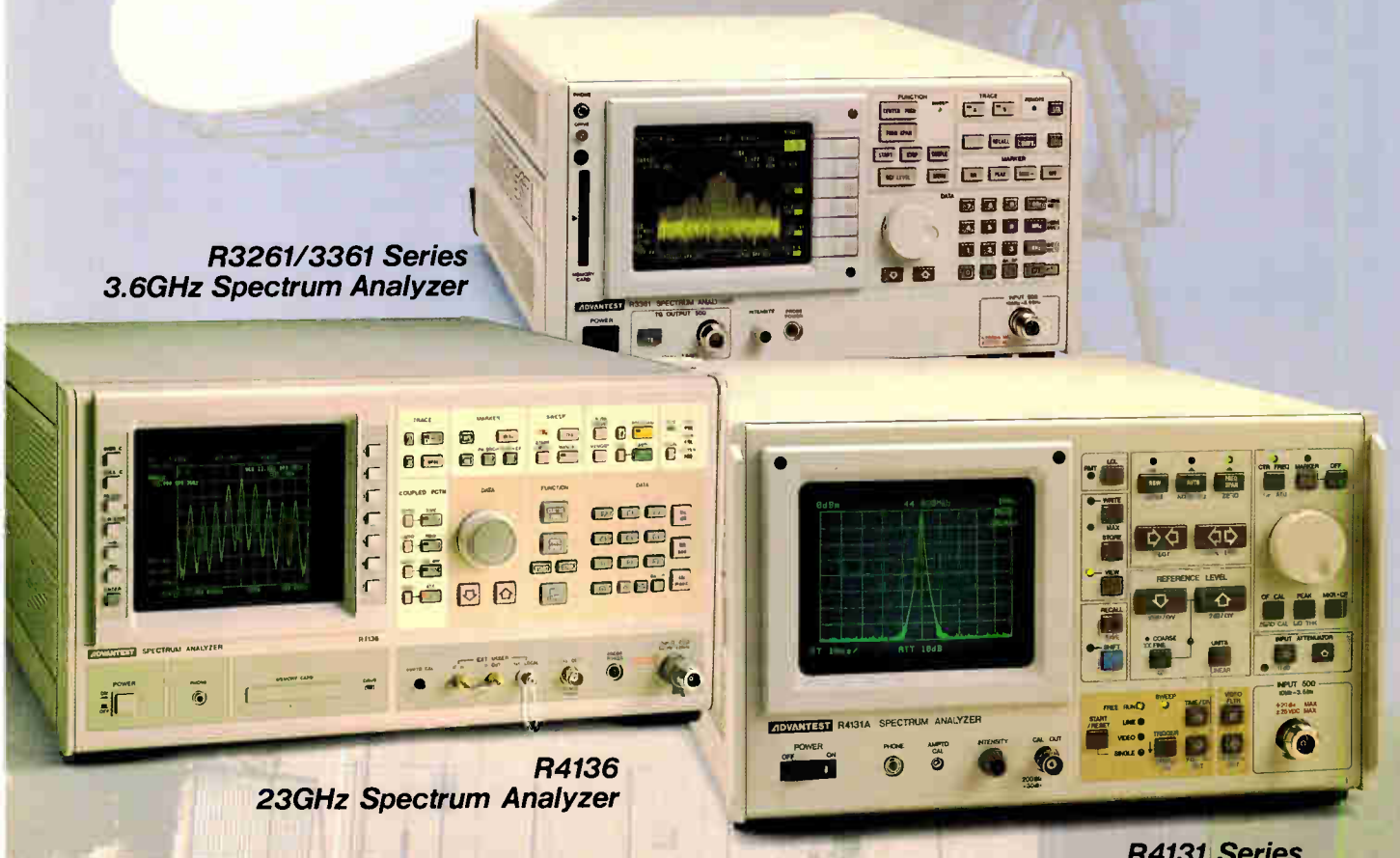

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Circle 72

A GIANT LEAP FOR SIMULATION

How Mentor and other vendors of CAE tools are pulling system builders toward the VHDL age of product design

by Jonah McLeod

Uncle Sam is known for setting forth technical mandates that commercial equipment vendors blithely ignore or craftily circumvent. This they do by claiming to meet the spirit of the mandate without actually meeting the precise intent, as in the case of the computer language Ada. But there are unmistakable signs now that the recently established Very High Speed Integrated Circuits program's Hardware Description Language requirement will enjoy a happier history. The U. S. Department of Defense, after developing the language under the auspices of the VHSIC program, has asked that all electronic designs for government contracts be submitted not just in silicon and brassboards but as abstract expressions coded in VHDL.

The success of VHDL has profound implications for the way systems will be designed in the near future. Hardware designers may chafe at the prospect of having to learn to write code—to write software that expresses the functions of the hardware they are working on. But once they do, they will be able to design better systems, and design them faster.

Most notably, they will be able to use a computer-aided-engineering system to experiment with design ideas at an architectural level, and to see the results of their explorations immediately in simulation. No longer will they have to wait until detailed gate-level designs are done to get practical simulation results; no longer will they have to wait until it's too late to go back and change fundamental decisions about a system's overall architecture without great expense and loss of time. The truly creative part of design, the part that's done at a high level of abstraction, will get direct support from simulation, thanks to the behavioral-level descriptions written in VHDL.

But design creativity wasn't foremost in the minds of the Pentagon brass who launched the VHDL push. The DOD is a well-known stickler for documentation, and the demand for VHDL is an outgrowth of the desire for more precise documentation. VHDL is a highly formalized way to describe and document electronic circuitry, and once a circuit is so described, the theory is that the DOD can go to any vendor and have it successfully duplicate the chip or board or system—not down to the precise arrangement and geometry of the transistors and other components, but to build a functionally identical circuit. Such duplication might even be done, given the right tools, without engineers reading a single line of the VHDL code handed them by the DOD. They would simply load the VHDL file onto their systems and use the systems to interpret the code and implement a design.

The fast-rising success of VHDL can be attributed in part to the history of its standardization. Unlike Ada, VHDL was developed with extensive industry involvement as an Institute of Electrical and Electronic Engineers standard, IEEE-1076-1987, for architectural-level simulation. Thus the IEEE has backed it as the best choice for a lingua franca for design.

In a practical sense, VHDL's success depends heavily on the support of major vendors of CAE systems for electronic design. Now, Mentor Graphics Corp. of Beaverton, Ore.—arguably the most important vendor of such systems, with its installed base and marketing prowess—has introduced a full VHDL simulator, forcing competitors to follow its lead (see p. 77).

Mentor is not the first to make its VHDL strategy known, however. Other vendors of CAE systems and software, such as Gateway Design Automation Corp. of Lowell, Mass. (see p. 80), are attempting to accommodate the DOD mandate. Gateway Design and others have developed or are working on translation software that converts code written in their existing simulation languages to and from VHDL. These companies are supporting VHDL subsets initially, and plan to move to the full specification later. In addition, vendors of hardware accelerators for simulation and logic-synthesis tools are devel-

oping software that allows their products to operate with subsets of VHDL.

This ground swell of support for VHDL is reflected in market projections for simulators into the 1990s. "There is a whole new generation of design-automation tools becoming available to inject new life into the market in the next decade," says Victoria Hinder, vice president of research at the Technology Research Group market analysts in Boston. She points to tools for architectural-level simulation, as well as logic synthesis and simulators with analog and digital capability.

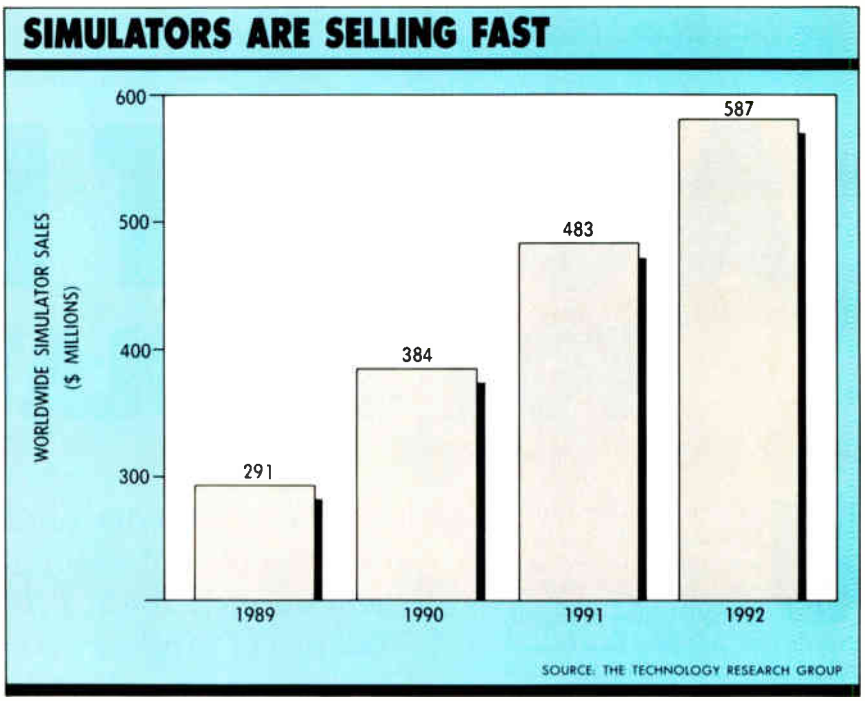
The simulation market in 1989 will be worth $291 million, says Hinder. It will grow 32% in 1990; growth of over 20% is expected to continue in 1991 and 1992, pushing the market up to some $587 million. Both the growth and dollar volume testify to the vitality and importance of what is largely a software-only market.

"Thanks to sub-1.2-μm CMOS process technology, it is possible to build application-specific chips with capacities of up to 200,000 gates," declares James Koford, vice president of CAD at LSI Logic Corp. in Milpitas, Calif. The problem is that designing such a large system with the gate-level design tools currently available is simply not practical. That's why architectural-level simulators such as Verilog from Gateway Design have become popular.

BLOCKS OF FUNCTION. This type of simulation enables the designer to work at a higher level of design complexity in a simulation environment. For example, at the architectural level, a designer might describe (in VHDL or Verilog, for example) a computer system with a central processor, memory system, and associated peripherals. The design is represented as major blocks linked by buses and signal-flow paths.

With VHDL, these blocks are represented by high-level-language descriptions of what happens at the block's inputs and outputs. Many design-trade-off decisions about the system's complexity, function, cost, and performance are typically thrashed out at much expense in time and effort during low-level hardware design. But with high-level simulations, these decisions can be considered intelligently early in the design cycle when making major changes has minimal impact on system cost and time to market.

In addition, a VHDL model is an unambiguous specification of the system that can be communicated among a number of different vendors. It is a common language in which to conduct business, a way that a design team can communicate with an ASIC vendor or board-layout people. Moreover, VHDL will ensure that systems developed today are as well understood in the future as they are in the present. This is an important characteristic for government contracts for systems that may have 10-to-20-year life expectancies.



Beneath the system-level description are descriptions of elements or subsystems within the larger system. Today, the designer can define these elements at the behavioral level using hardware modeling languages or off-the-shelf models from independent model vendors. At the next level in the design hierarchy are register-transfer descriptions of elements within subsystems. These elements are divided further into logic- or gate-level descriptions and the gates are further broken down into transistor-level implementations.

> Architectural-level simulators make it practical to design ASICs of over 100,000 gates

Some gate-level simulators already offer simulation capability operating at other levels, such as the register-transfer level, or the ability to accommodate higher-level models of complex subsystem components. Companies such as Gateway and Zycad Corp. of St. Paul, Minn., offer architectural-level simulators, but their simulators do not support VHDL directly.

To forward their own marketing plans, suppliers with VHDL solutions ready for the market are banking on the DOD requiring designs not only be documented in VHDL but simulated as well. "The DOD mandate, Mil-Std-454L, requires VHDL documentation on all ASIC-level designs," says Ronald Abelmann, president of Vantage Analysis Systems Inc., Fremont, Calif., one of the few companies with a simulator written for VHDL. Paragraph 4.5.1 in Mil-Std-454L, Requirement 64, and a Data Item Description tell how the 454L requirement is to be implemented. "It implies not only that the design be documented in VHDL but that the design be validated in a VHDL simulator as well," he says.

"The manufacturer must supply test vectors in VHDL," points out Abelmann. "The implication is very strong that the supplier has to do VHDL simulation. Sure, you can translate something, but unless you run the simulation on a VHDL simulator, how does the buyer verify that the VHDL documentation he has been given is correct?"

Intermetrics Inc. of Cambridge, Mass., and Vantage are the only companies at present with VHDL solutions. But that will change this year as two more companies roll out competitive VHDL offerings. Mentor Graphics will have a product called the System-1076 ready to ship in the third quarter. By the second quarter Zycad plans to have rolled out Endot-VHDL, a language in development at Endot Inc., Cleveland, when Zycad bought the firm out.

But Vantage believes it is ready for the competition. "The Vantage spreadsheet is unique not only because of implementing the VHDL language," says Abelmann. "It is an advanced multilevel architectural simulator that happens to use VHDL." The benefit to the user is its incremental design-change capability, dubbed the Vantage spread-

sheet. Vantage expects the user to get a three- to tenfold improvement in productivity through using their spreadsheet, says Abelmann.

Intermetrics had the original DOD contract to develop the VHDL, which was then turned over to the IEEE so the industry could participate in setting the standard. "The IEEE solicited significant industry input and the language was changed on the order of 30%," says Abelmann.

BIG IMPACT. Of all these products, the Mentor Graphics and Zycad announcements will have the biggest impacts on the market due to the large installed base both companies already have. "In order for the industry to benefit from VHDL models, mainstream simulator suppliers, such as Mentor Graphics or HHB Systems—two simulators that NCR supports—must fully support the IEEE standard," says Earl Reinkensmeyer, director of software products at NCR Corp.'s Microelectronics Division in Ft. Collins, Colo., a major ASIC vendor. "And the design engineer has to accept the language."

"Mentor's System 1076 provides complete VHDL language capability compatible with and operating within the company's existing design-tool environment," says Robert Mendes da Costa, VHDL product manager at Mentor. One of the more novel capabilities of the Mentor Graphics offering, when it is released in early 1990, will be its graphical architectural-level design editor. This will allow designers to draw a block diagram of a large system, assign models to individual blocks, and connect the blocks with buses and signal paths. The editor will link the text descriptions of blocks and connections with the associated graphics to allow system-level simulation of the block diagram. It will allow system engineers to think in a familiar way, as they do when they sketch out a block diagram on a piece of paper, while at the same time capturing design information in a rigorous way.

However, the graphics interface may not be a strong selling point with existing users of hardware description languages. "The typical designers using HDLs are those that do not put a high demand on graphical interfaces," says Stephen Manner, vice president of marketing at Zycad's Menlo Park, Calif., facility. "They are familiar with hardware description languages and accept programmatic interfaces."

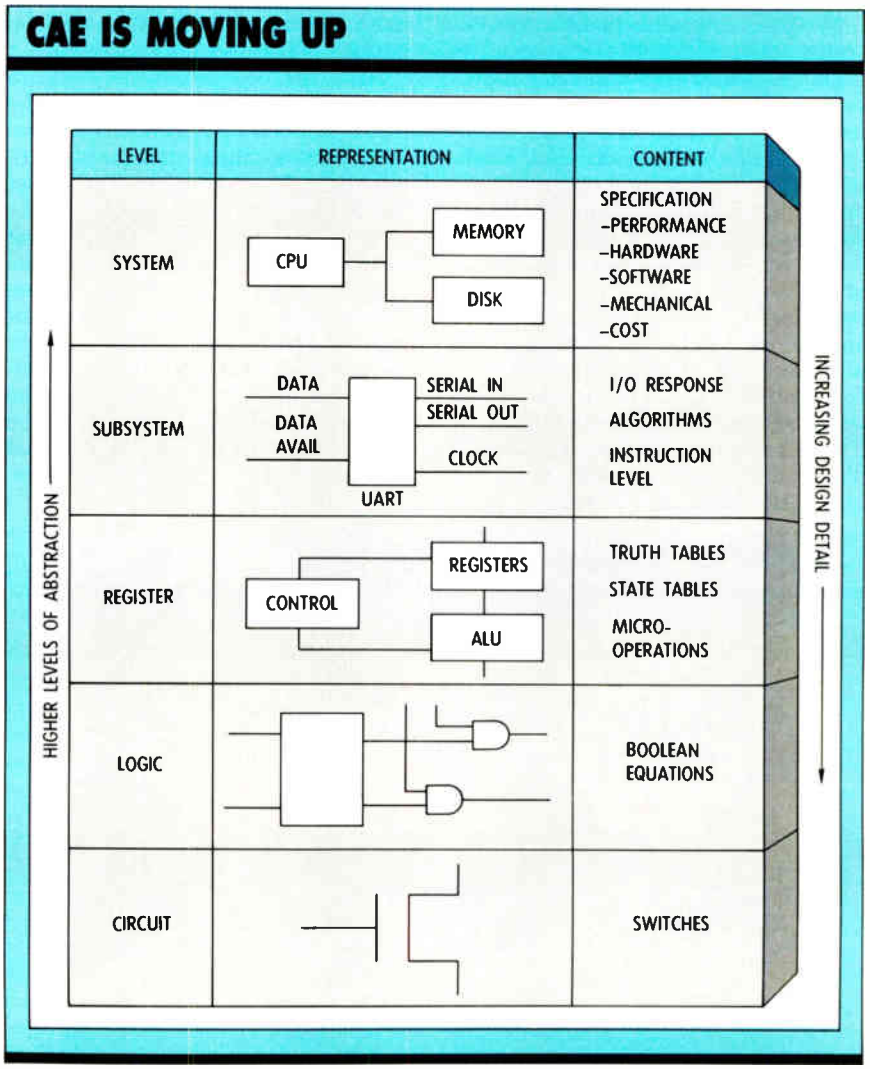
Zycad has alpha versions of its Endot-VHDL simulator now and beta versions will be available in the second quarter. "It is an extension of the Endot software," says Manner. "The core engineering team developing the simulator comes from a group within Endot which had been developing VHDL for a year when we acquired the company." The VHDL team has developed a new simulator from the ground up, but it will tie into some of the tools in Zycad's current product offerings.

While tool suppliers buy time to roll out full implementations of VHDL products, many are using translators between existing simulators and VHDL. Two companies making a business of supplying such translators are CAD Language Systems Inc. of Rockville, Md., and Intermetrics. "We have announced business relationships with a number of companies about developing translators for VHDL," says Moe Shahdad, president of CAD Language Systems. The company is working with GenRad, for example, and its HiLo simulator. "We are working with others as well," says Shahdad.

"The drawback to [translation] is that only a subset of the langauge can be implemented, since all VHDL features are not available with other HDLs," says Geoffrey Bunza, general manager of the design and analysis division at Mentor Graphics.

Drawback or not, the translation method is a quick way for companies to gain a level of DOD compliance while working to develop a native-mode implementation. "We are writing our own translator [for moving] between VHDL and Verilog," says Prabhu Goel, president of Gateway. Verilog maps into a subset of VHDL. It is a subset because not all of the language constructs of VHDL can be mapped into Verilog. "Because VHDL is at the behavioral level, you have to transfer structural net-list data plus an elaborate behavioral description written in VHDL," he says. "This must be translated just as a programming language is translated. In addition, models written in native Verilog language will be translated."

Gateway delivered the first phase of the two-way translator to customer beta sites in December. The company is also writing a translator that converts VHDL simulator output back into Verilog form. "We will be taking the VHDL



Simulation offered on CAE systems now operates mainly down at the logic-gate and switch levels; VHDL-based tools permit simulation at higher levels of design abstraction.

subset we created and resimulating it with our own [Verilog] simulator," says Goel. The longer-term goal is to extend Verilog to incorporate some VHDL constructs that it lacks.

Another company planning to offer translated VHDL capability is Silicon Compiler Systems Corp. of San Jose, Calif. "We are committed to providing a bidirectional VHDL interface from our hardware description language L-Sim into VHDL and also from VHDL into our environment so designers can use the VHDL language and simulate and debug their design in VHDL," says John Odryna, vice president of product marketing at Silicon Compiler Systems. The company will add direct VHDL support midyear, it says.

At present there are two camps among the VHDL proponents, one claiming the full specification has to be implemented, another declaring that subsets of the specification are acceptable. "We think subsets are okay," says Fred Odence, product marketing manager for Lasar, the simulation product from Teradyne Inc. in Boston.

"VHDL is so flexible that you can describe electronics—13-state logic for example—which cannot be built at present; subsets that make sense for the technology available today. As technology increases, you can change the subset. There are IEEE and electronics industry association groups which are defining subsets that make sense."

One reason that translated subsets of VHDL are likely to be popular is that designers have become familiar with and like the feature set of existing simulators. "The majority of the market for simulators is held by companies with existing simulators—Gateway, HHB Systems, Mentor, etc.," says Shahdad of CAD Language Systems. "If a VHDL simulator supplier says to the designer, 'you either implement the full VHDL implementation or a well-known simulator with a subset of VHDL,' the user is more likely to choose the latter."

"Most hardware designers tend to view VHDL as cumbersome," chimes in Odence of Teradyne. "It has more of a software look and feel."

MEANINGFUL SUBSETS. Logic synthesizers are yet another factor likely to promote the development of subsets of VHDL. "It is not meaningful to synthesize all the VHDL language elements," says Shahdad. "There are features in the language which are difficult to synthesize. As a result, subsets are being defined for synthesis."

CAD Language Systems and Carnegie-Mellon University in Pittsburgh have a contract with the Army to demonstrate that there is a usable subset of VHDL for logic synthesis. "We are developing a prototype that must be able to run certain benchmarks showing that you can synthesize VHDL statements," says Shahdad. The subset will ultimately be made public.

On the way are subsets of VHDL for logic synthesis

The effort is aimed at demonstrating the capability that lets a designer describe a component as complex as a 6502 microprocessor using a subset of VHDL and has a logic synthesizer create the detailed circuit design automatically, in a matter of a few days. The promise of logic synthesis is that the design will be as efficient as if it had been done by expert designers spending months on the task.

That research effort is addressing future problems of synthesis with the VHDL language, "but they are still having to deal with the bottom line of chip size," says Art deGeus, founder and vice president of engineering at synthesizer vendor Synopsis Inc. of Mountain View, Calif. "If you can synthesize a 6502 automatically, but the result requires a 2-cm² chip, the tool is not practical. The quality of the result determines the acceptance rate of new tools in the commercial environment." DeGeus contends that while it will be practical some time in the future, designers using commercially available synthesizers today must content themselves with specifying their designs in a VHDL subset at the register-transfer level to achieve practical results.

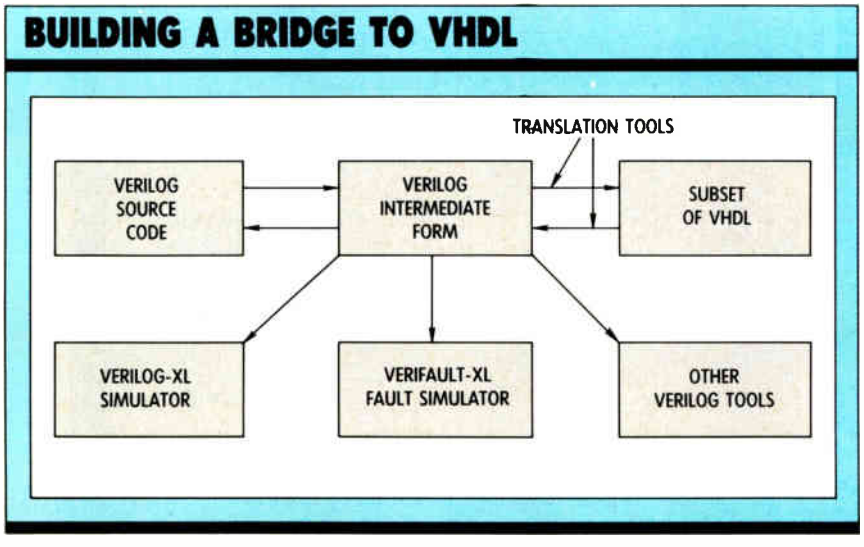
But it is unlikely that a single VHDL subset will evolve for all logic synthesizers, because "the techniques used for synthesis are divided along the lines of structured synthesis, data-flow synthesis, and behavioral synthesis," says Shahdad. "The technologies are different, therefore each resulting subset will be different. There are four or five subsets evolving at this time."

Simulation accelerators are another factor contributing to the proliferation of VHDL subsets. Subsets are needed to solve the problem of simulating—on a practical time scale—a large design in which some portions are represented as behavioral models and others represented in gate-level descriptions. "It takes 10 to 100 times more processing power to simulate the detailed gate-level [design] than it does to simulate the few powerful blocks of behavioral description written in VHDL," says William Loesch, president of Ikos Systems Inc. in Sunnyvale, Calif. "As a result, the gate-level simulation can require over 90% of the total simulation time."

In designs containing both behavioral and gate-level descriptions, the former is typically executed on a work station and the latter is run on a high-speed computation server or simulation accelerator. But the behavioral simulator running on the work station must be able to communicate its results to the gate-level simulator running on the accelerator, and vice versa. Ikos is building a hardware product that converts high-level VHDL statements into detailed simulation vectors for the gate-level simulator and vice versa.

"What is unique about the Zycad VHDL simulator is that it will be integrated with the Zycad accelerator environment," says Manner. "The designer will be able to run VHDL models at the behavioral level and link them with VHDL gate-level models, or models described in other formats, running on an accelerator." □

BUILDING A BRIDGE TO VHDL



For a designer already used to working in the Verilog language, Gateway will offer translation options that allow him to import VHDL models and generate VHDL documentation.

CAE GIANT MENTOR GRAPHICS BITES THE VHDL BULLET

Design and simulation using the DOD's language is the centerpiece of its new strategy

The empire is striking back. Mentor Graphics Corp., the Beaverton, Ore., company that now dominates the electronics computer-aided-engineering galaxy, has been taking some major hits as another vendor's simulator infiltrated its customer base. Gateway Design Automation Corp. of Lowell, Mass., has a product called Verilog XL that fits right into the Mentor environment, among Mentor's other tools. Although Mentor isn't saying how much business it has lost to Gateway, it's clearly significant, because inside Mentor the company's new product has been dubbed the "Verilog killer."

The Verilog simulator is based on a hardware description language also called Verilog. The Mentor empire's response has been to strike back with a powerful new set of tools built around the language mandated by the Department of Defense: VHDL, for VHSIC hardware description language (VHSIC is the DOD's Very High Speed Integrated Circuits program). The move is bold because right now there are very few engineers trained to use VHDL.

BACK TO SCHOOL. Some industry experts say it will be hard to get hardware-oriented engineers to reorient their design thinking process to use VHDL. Hardware guys, used to schematics, block diagrams, gates, transistors, and netlists, will need to do something that looks a lot like what software programmers do: write lines of code in a high-level language similar to software languages. Recognizing this, Mentor is gearing up to offer training programs to customers in the hope that enlightened managers will nudge their engineers to learn something new and different.

What Mentor is hoping they'll learn to use is a major revision of its QuickSim simulator, which simulates designs expressed in VHDL. Another part of the picture will be filled in early in 1990, when a graphical specification editor will make it much easier to capitalize on the architectural-level design possibilities inherent in the language. Mentor's VHDL design debugger will ship in the third quarter of 1989, however. It will allow debugging directly in VHDL, in contrast to some other companies' approaches, which have the user debugging in a proprietary environment and language and then translating the design into VHDL afterward.

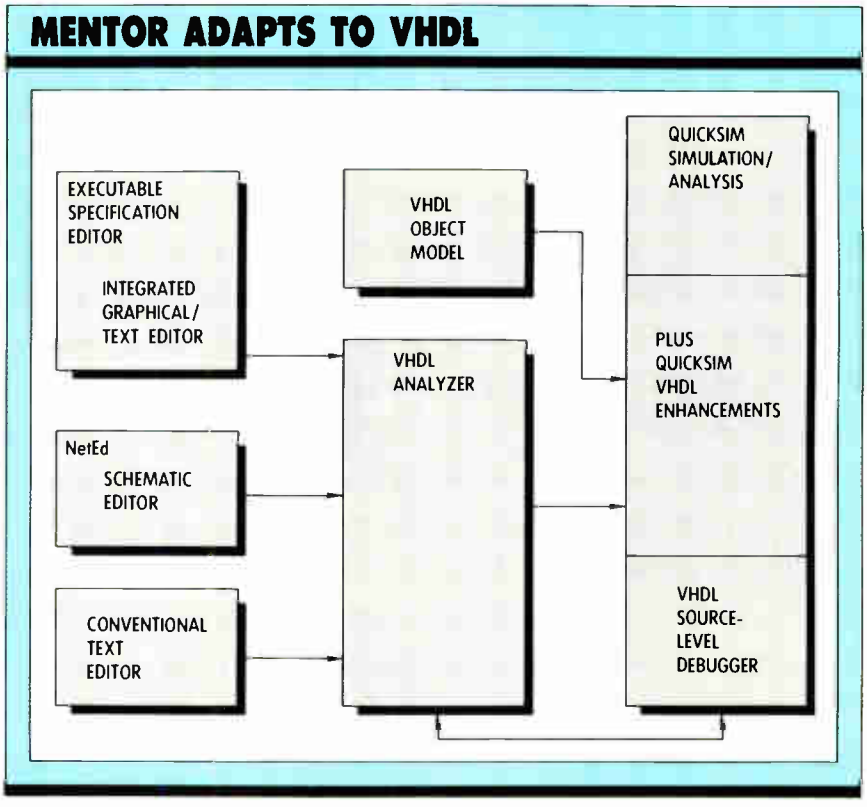
"We have a new modeling and design environment that is completely compatible with our other modeling and analysis tools," says Geoffrey Bunza, general manager of the design and analysis division at Mentor. Called the System 1076, it supports fully the IEEE-1076 standard for VHDL within Mentor's existing integrated design environment. The designer gets all the functionality of VHDL, not just a subset, as others are offering.

Account control is a critical long-term strategy for Mentor as it attempts to maintain its lead position in the increasingly competitive electronics CAE market. And a CAE-tool vendor's simulator is the key to account control, as Mentor president and chief operating officer Gerald Langeler is fond of saying.

Starting now, VHDL-based simulation is the technical centerpiece of Mentor's account-control strategy. And according to Jark Carveth, treasurer at the company, "approximately one third of the company's total revenue each year comes from simulation tools."

While Mentor is pinning its hopes on a VHDL-based strategy, the ultimate success of VHDL itself may be dependent to a large degree on Mentor's success. Because of Mentor's commanding position in the industry, its VHDL thrust combines the chicken and the egg. Mentor will thrive—and VHDL will take off, leaving a flock of competing HDLs in the dust—if enough companies decide to invest their engineers' time in learning a new methodology for product design.

Cindy Thames, vice president at the Technology Research Group, a CAE market research firm in Boston, says that Mentor's size and the industry's recognition of the need for an HDL standard work in favor of VHDL competing with suppliers of other HDLs for new installations. "I believe that, in general, the market perceives that VHDL will be a standard because of the DOD mandate," she says. "Just as newer installations are Unix-based, more than VMS-based, users are going to prefer a vendor that supports VHDL over those that have non-



To bring VHDL into its design environment, Mentor is enhancing its QuickSim simulator and adding a VHDL source-level debugger, a VHDL analyzer, and a specification editor.

standard implementations."

Thames says that in competing with other VHDL vendors, Mentor is bolstered by its reputation and by a broader range of integrated products than is offered by newer suppliers. However, she points out that the current announcement only stakes out Mentor's position in this emerging market. The product will not arrive until the fall and the graphical editor will come months later. "There are certain companies that can afford to wait and that will, but not all," she says.

In adopting VHDL as its high-level language, Mentor is leveraging off the inherent benefits of the language. "The product will allow designers to work with a language that is synergistic with the way they think," says Bunza. Unlike other HDLs, VHDL does not impose a particular design method, but rather allows a designer to choose behavioral, data-flow, structural, or other design styles and allows him to design from the top down, from the bottom up, or to use a mixture of the two approaches.

One powerful feature of VHDL is its arbitrary data types, which allow the designer to create an abstract description of a function and provide its details as the design becomes better defined. For example, the message packets in a networking system can be defined as having an address, a string of bits, and some control characters, with details on each to be provided later. "Other HDLs do not have this richness," says Robert Mendes da Costa, VHDL product manager at Mentor.

Another benefit is that the designer can work at a very high system-architecture level all the way down to the detailed gate level. "High-level descriptions can be combined with lower-level schematic diagrams," explains da Costa. "We currently have tools that support all the lower-level design capability, integrated schematic capture, libraries, ASIC tools, links to manufacturing test, etc."

By contrast, he says, other HDL-based CAE systems provide some of the behavioral capability of VHDL but lack Mentor's complete tool kit. Some tie into the Mentor system, but are not totally integrated, as is the VHDL product from Mentor. As a result, the designer is either working at the behavioral level with a foreign simulator or in Mentor's environment at the lower levels.

To achieve tight integration of VHDL-based designs into its existing design environment, the company is adding to its QuickSim simulator a set of enhancements with associated VHDL object models and a source-level debugger for VHDL. The tools will include a VHDL analyzer, an integrated graphical text editor, and associated schematic and text editors. The system, System 1076 (less the graphical editor), will ship in the third quarter at $24,900.

VHDL work is split into two parts in the system. The VHDL analyzer evaluates the design in terms of its static characteristics, without stimulus. For example, the analyzer performs syntax and type checking on the design description.

After static evaluation, the VHDL analyzer feeds QuickSim with information needed to perform dynamic analysis. The QuickSim enhancements analyze the dynamic behavior of the design. "The enhancement contains capability that allows QuickSim to understand what time is and how a circuit element can utilize time," says William McKenney, engineering manager for VHDL. Other enhancements deal with abstract data types—integers, record types, and so on.

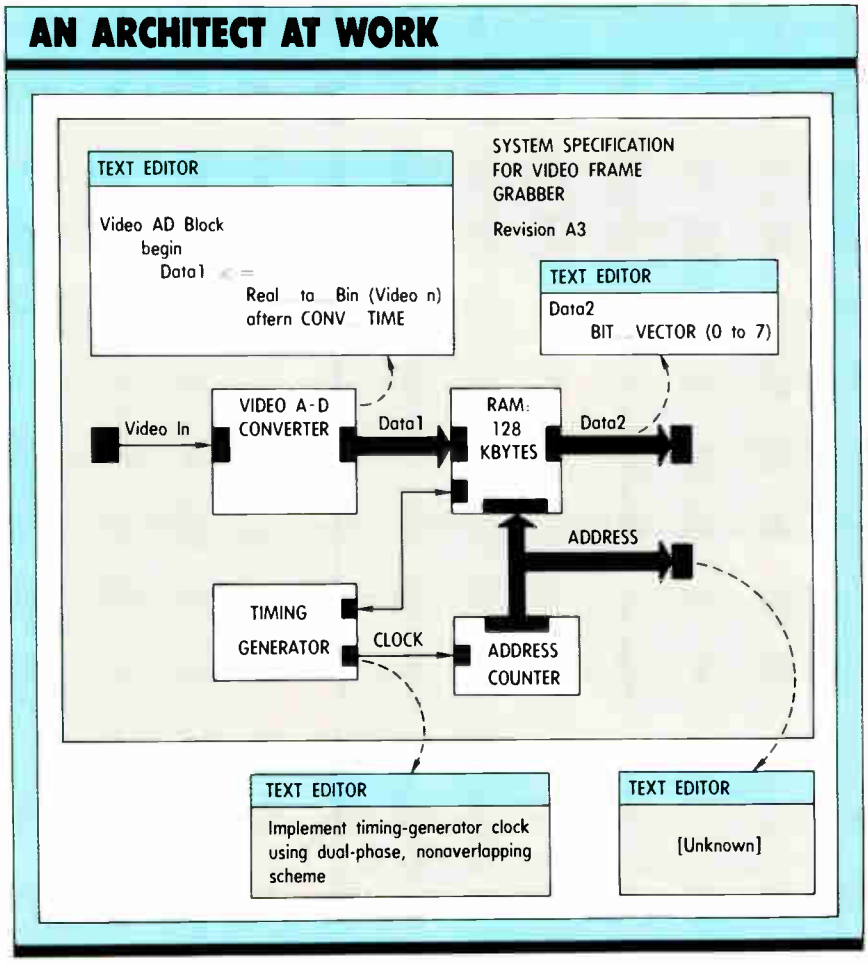
System 1076 compiles VHDL language statements into a data structure that is an integral part of the QuickSim environment and has been optimized for the simulator. VHDL instructions are executed in native mode during a simulation run. Because Mentor has implemented VHDL within the existing QuickSim environment, there is no translation step from one language to another before simulation, as is necessary in using Gateway's Verilog simulator, for example.

THINK ONE WAY. When VHDL is translated into another language, its capability is limited by the capability of the other HDL. "One direct benefit from [Mentor's] approach is that no time is wasted in translation," adds da Costa. "An indirect benefit is that designers don't have to think one way to design at the gate level and another way at the behavioral level."

The innovative graphical interface will consist of an integrated graphical and text editor that make up an executable-specification editor. Conventional design and specification methods associate text and graphics by proximity. As a result, architectural specifications have become large collections of loosely associated documents and files. Cross-referencing this data has become difficult and time-consuming with the complexity of today's designs. And the clutter of data makes understanding the design intent and flow of the architectural specification difficult.

"Designers do not approach system designs during the first stages textually," Bunza contends. "They draw diagrams, blocks of functionality with interconnections and signal flow, and communications running between them." At this stage, designers are more interested in conceptualizing a design and communicating its intent. With System 1076, Men-

AN ARCHITECT AT WORK



A sketch pad with flexible drawing capability is the basis of Mentor's executable specification editor. Function blocks and interconnect lines are linked to underlying descriptions.

tor is allowing them to perform this same kind of graphical design specification.

The architectural editor allows designers to create and organize architectural-specification data into a meaningful network of representations and hierarchical structures that represent design flow and intent. In addition, the software executes the architectural specification for analysis—a behavioral-level (or mixed-level) simulation. Today, this architecture is specified with VHDL statements. In the future, the specification and analysis will both be done through logic synthesis.

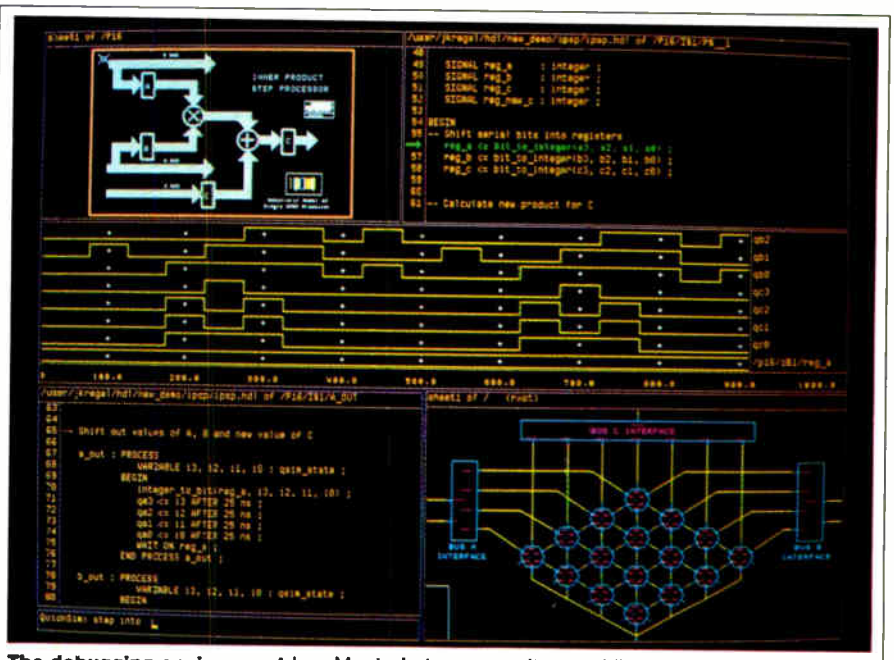
In describing a frame-grabber circuit containing a video analog-to-digital converter, memory, a timing generator, and an address counter, for example, the designer simply draws the elements as blocks on a screen. He then connects the blocks with buses and control lines. The process mimics the way a designer makes a rough sketch of a design idea before adding increasing levels of complexity. "It's an extremely flexible sketch-pad drawing capability," says da Costa.

Once the graphic is created, the designer may write a simple text or a rigorous VHDL description of each block's behavior using the text editor. For example, he could note that the timing generator is to be implemented using a dual-phase, nonoverlapping scheme. Or he might write VHDL code describing the behavior of the a-d converter. In many instances, some blocks in the design may be ASIC cells already designed, or off-the-shelf standard parts—the address counter for example—in which case the block can have an underlying register-transfer-level or gate-level representation called in from a library of models.

The graphical and text editor together create a complete windowing environment, in which the windows represent the links between graphical objects and their underlying description. The editor links blocks with executable VHDL descriptions or those that could be purely textual, gate-level representations, state-machine descriptions, and so on.

Because VHDL models are executed in Mentor's QuickSim, they can be mixed with other models within the simulator, such as gate primitives, switch-level primitives, and hardware models. For example, the address counter can be a gate-level model and all other blocks can be high-level VHDL models. To look at a block's underlying lower-level representation, the designer simply selects the block to be viewed with a cursor.

When the architectural description has been entered into the system, it can be compiled for analysis and debugging. During simulation, the graphical information contained in the specification can be viewed. In addition, probes can be placed on graphical objects—buses or signal paths—and on the inputs and outputs



The debugging environment has Mentor's trace, monitor, and list functions, but adds the ability to open windows of textual VHDL statements for dubugging at the source level.

of larger blocks, to view their values.

"Today, designers spend a majority of their time in the debug and analysis phase of the design process," says da Costa. "Finding and correcting design errors and bad assumptions early in the design process greatly reduces development costs and shortens time to market."

With System 1076, because the designer is debugging in the QuickSim environment,

Mentor's debugger handles concurrent operations, unlike many competing tools

he has access to the simulator's trace, list, and monitor windows to view the external values of a model as well as its internal data. He can open VHDL text windows to view source-level statements.

Because VHDL allows designers to define their own data types, QuickSim's trace and list windows were enhanced to display this information. The ability to display abstract data, such as character strings, real numbers, integers, as well as standard logic data, makes it possible for designers to analyze highly abstract, architectural-level designs with lower-level designs, all in the same environment.

"It is a design-oriented debugger, which supports concurrent operation and offers capability to single-step through the VHDL code," says da Costa. "Such capability is important in being able to view the flow and execution of the code." VHDL mimics the concurrent operation of hardware.

The ability to debug concurrent operations is what makes Mentor's native-mode implementation of VHDL different from translation-based implementations. When the designer sets a breakpoint on a VHDL statement, the debug environment breaks on the very same VHDL statement. When the designer stops a simulation at a breakpoint in a set of concurrent interrelated operations, there are a number of statements in the VHDL code that are scheduled for evaluation. The designer needs to be able to observe all these breakpoints resulting from the single VHDL breakpoint.

A breakpoint in the design halts all activity in the circuit at a single point in time. At the breakpoint there are a number of processes scheduled for execution. The source-level debugger shows a breakpoint menu listing all the possible concurrent operations occuring at the time. The designer can select from the list those processes he wishes to view. In addition, he can use the cursor as a probe, as is done with the current schematic-capture package of the Mentor system.

Major drawbacks are inherent in translating from VHDL to another HDL, says da Costa. If a designer develops his design in VHDL, he is forced to debug in a language in which the design was not developed. "Given the translation methods, I don't know how a designer is going to be able to debug," da Costa says.

With System 1076, the designer specifies and debugs the design in VHDL. "He does not have to remember what environment he is in or how the translator works," says da Costa. What's more, "he does not have to change his thinking depending on whether he is entering a design or debugging it. He does not have to understand how the symbols are mapped or other housekeeping matters." *–Jonah McLeod*

GATEWAY'S SIMULATOR IMPROVES ITS TIMING

Gateway Design Automation Corp. is strengthening its hand in more ways than one in the head-to-head design-simulation battle with rival Mentor Graphics Corp. Gateway is working on a VHSIC Hardware Description Language strategy (see p. 73). But it is also pushing ahead on other fronts—like improving timing analysis for today's breed of high-speed chip and board designs.

The timing verifiers found in most logic simulators, which use simple static-path analysis or minimum/maximum timing delays to ensure that critical paths do not violate design-timing constraints, are no longer adequate. Veritime, the Lowell, Mass., company's new timing-analysis package, is the kind of tool designers are looking for. It is the first that enables the designer to specify logical conditions in which timing analysis is to occur. This capability means a designer can trace a signal path with several forks, each enabled by a different set of logical conditions; trace through feedback loops; or perform timing analysis at the system level before detailed logic has been designed.

Veritime is being beta tested now. Gateway says it will be ready to ship in the second quarter at prices ranging up from $20,000, depending on the hardware it runs on. The tool is fully integrated with the company's Verilog XL simulator and uses the Verilog language.

With Veritime, the designer can use pure static timing analysis, the kind provided by conventional timing analyzers, or a hybrid of static and simulation-based analysis. With the hybrid approach, simulation patterns provide the qualifying logic signals to open the gates through a critical path to be analyzed. The hybrid capability uses a timing template to specify how to exercise the clock, control, and data-flow logic of a design.

"Veritime simulates the timing template and uses the simulation to derive the regions of the logic through which critical-path analysis is to be performed," says Prabhu Goel, president of Gateway. The designer can create and use multiple timing templates. And these templates require very few simulation vectors.

> With Gateway's Veritime, designers can easily trace a path with several forks

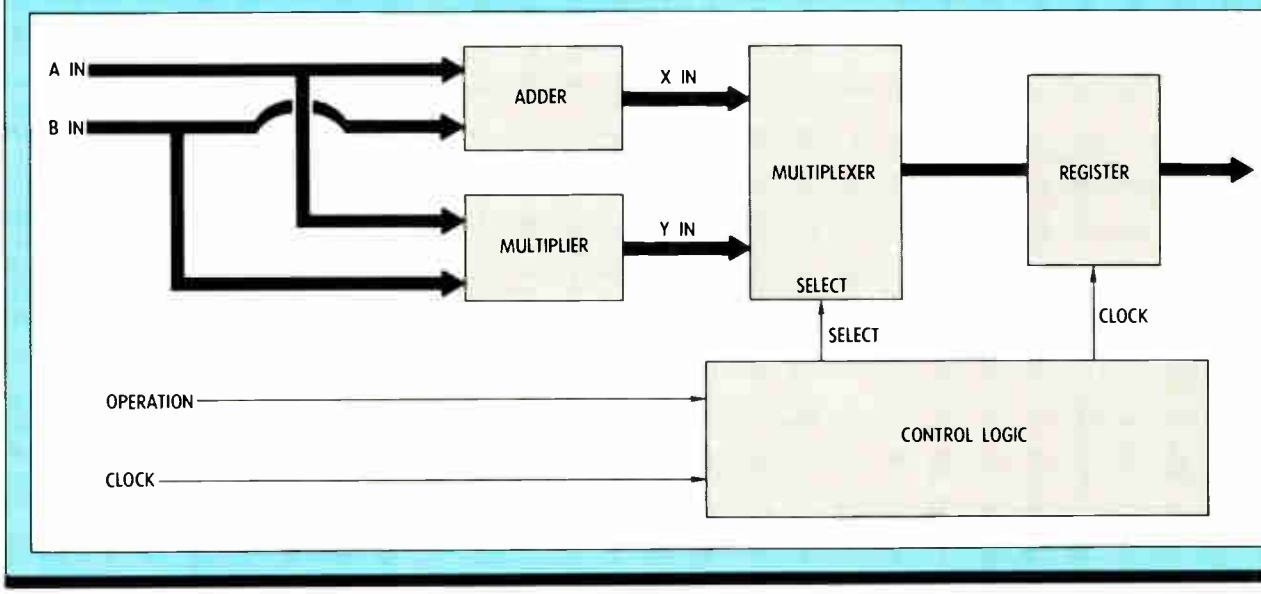
To illustrate the power of this capability, consider a logic circuit in an arithmetic unit that can be in the multiply or add mode. The designer may want to check the path first for one mode and then for the second. Other analyzers cannot distinguish between the two modes. Veritime, by contrast, enables conditional timing checks, in which analysis occurs only when certain logical values specified in the timing template exist.

In the arithmetic unit, the timing template allows the designer to select which of the two paths through the device to perform timing analysis on by specifying a qualifying logic level. If the designer wants to check the add mode, he specifies in the timing template the control signals for an add, then changes the specification in the timing template for a multiply.

Selecting which path to trace through is only one way to use the template. Another is to determine the time required to move from one point in a set of logic to another point, starting at a specified point in time. To determine the time it takes for a clock signal to move through control logic to become a derived clock at the output, the designer sets a start time in the template, the leading edge of a clock pulse, say, and then measures how long it takes data gated by the clock pulse to move through the logic.

Also unlike other critical-path analyzers, Veritime is capable of tracing through a feedback loop. Other analyzers end up executing continuously when traversing through a feedback path or they stop executing on recognizing such a loop. To analyze time through a feedback loop, the designer simply tells Veritime the length of the loop. The analyzer then proceeds through the loop one node at a time. When it recognizes a node it has already passed, the analyzer determines that it has gone through the loop once already. The total of all of the delays accumulated during Veritime's traverse through all of the nodes is the amount of delay in the loop. *–Jonah McLeod*

SPEEDING UP TIMING ANALYSIS



Gateway's Veritime is the first timing-analysis package that allows a designer to specify the logical conditions in which analysis is to occur. For example, in a circuit with an add mode and a multiply mode, he can specify a logical condition on the Select line to analyze add-mode timing.

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NOW THERE'S MORE THAN JUST RAW SPEED IN THE ECL ARENA

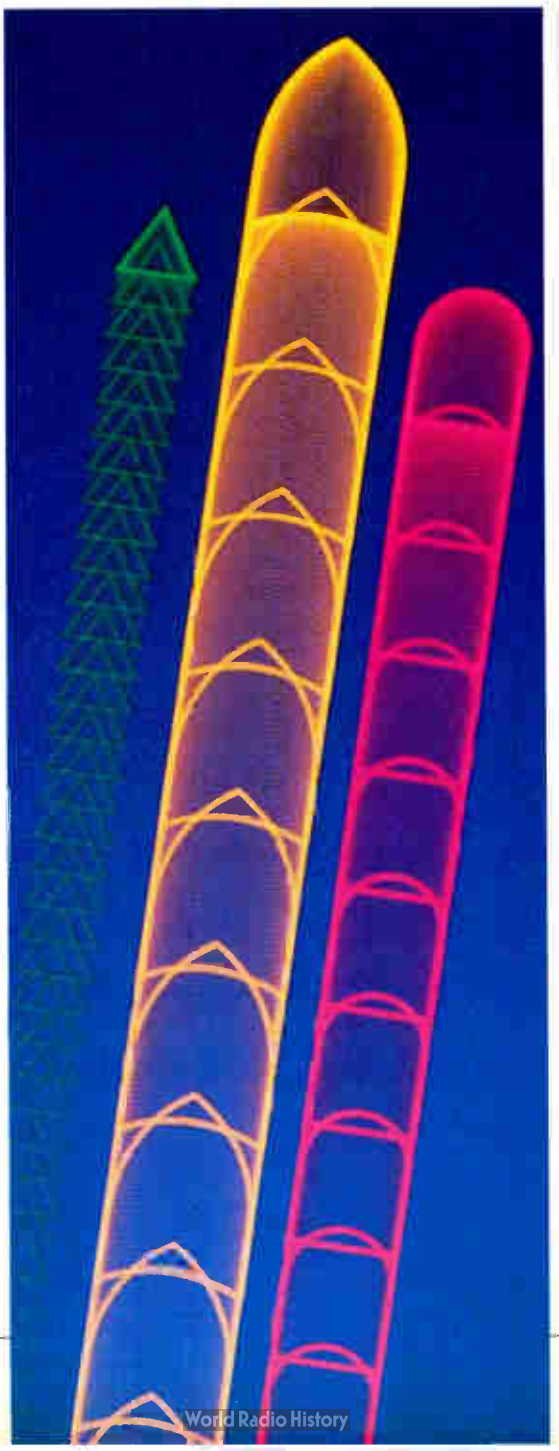
by Bernard C. Cole

There's a new drumbeat in the high-performance integrated-circuit market. And its message is: system designers no longer demand just raw speed. They demand speed combined with lower cost, higher density, better noise immunity, and lower power consumption. As a result, the emitter-coupled-logic IC marketplace is in the throes of a rapid transformation. For one thing, ECL, designed for high-performance applications, will no longer be associated with just silicon bipolar technology, but also with gallium arsenide and bipolar-CMOS processes.

Nor will it be associated only with low-density logic and sub-64-Kbit static random-access memories. Improvements in GaAs, biCMOS, and bipolar processes are driving densities for high-performance circuits to the level of very large-scale integration. At the same time, these improvements are increasing speed—with gate delays dropping from as high as 1 ns to as low as 50 ps—and lowering power dissipation from 10 mW per gate to less than 250 μW.

The result is the emergence of a wide range of ECL and ECL-compatible circuits that will expand the number of options available to systems designers. Among these:

- Bipolar ECL gate arrays with densities of 40,000 to 70,000 gates and 100,000-gate standard-cell designs that dissipate no more power than present-generation 10,000-gate arrays and 25,000-gate standard-cell circuits;
- ECL-compatible GaAs gate arrays with densities of up to 16,000 gates and 25,000-gate standard-cell designs—and with power dissipation levels closer to silicon CMOS than to equivalently sized bipolar circuits;
- GaAs and bipolar ECL programmable logic devices with propagation delays below 10 ns and going for under 5 ns;
- Standard small- and medium-scale-integrated bipolar and GaAs logic circuits pushing into the picosecond range;
- 1- and 4-Kbit bipolar, biCMOS and GaAs SRAMs pushing to below 5-ns access times;
- BiCMOS SRAMs with higher densities than ever possible with bipolar technology—256 Kbits now and pushing toward 1 Mbit.



Also in the works are a variety of VLSI ECL-compatible standard products including multipliers, multiplier-accumulators, and 32-bit processors, fabricated in bipolar, biCMOS, and GaAs.

Fueling all of this product proliferation in the ECL marketplace is the demand for greater and greater speed in all segments of the marketplace. At the high end of the market are the traditional users of ECL: mainframe makers plus their newer competitors, the makers of superminicomputers, supercomputers, and minisupercomputers. But what is causing a big expansion of the ECL market beyond all previous expectations is the emergence of demand by designers and users of microprocessor-based systems.

Based on the potential new markets, and the increasing number and diversity of product offerings, many companies and industry analysts are revamping their estimates of market growth. An *Electronics* survey of half a dozen semiconductor com-

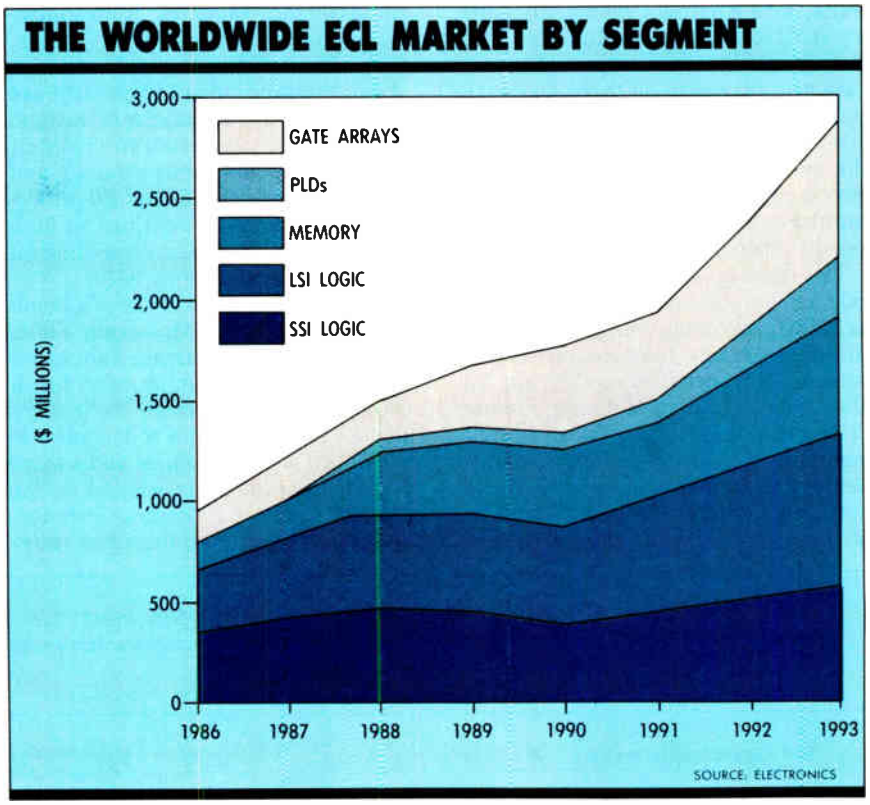
panies disclosed a trend that indicates the ECL market is in for an era of explosive growth in the early 1990s. After a period of modest growth from about $1.5 billion worldwide in 1988 to perhaps $1.75 billion in 1990, demand is expected to accelerate rapidly, reaching between $2.75 billion and $3 billion by 1993. And where the major portion of the ECL market is currently based on bipolar silicon, by 1993 biCMOS and GaAs offerings will also be contributing substantially.

ECL gate arrays are still expected to contribute significantly to overall growth, increasing from about $425 million in annual sales in 1989 to about $725 million in 1993. Almost as dramatic is the ECL SRAM segment, which after an essentially flat period through 1988 and 1989, with about $300 million to $350 million in annual sales, will grow to about $510 million by 1993.

A new high-growth segment of the ECL market will be LSI and VLSI cell-based custom and standard products such as multipliers, multiplier-accumulators, bit-slice processors oriented toward digital signal processing, and 32-bit processors based on reduced-instruction-set-computer architectures. After several years of essentially flat growth of about $475 million to $500 million from 1988 to 1990, this market segment will rise to about $750 million in annual sales by 1993.

THE NEED FOR GLUE. Reflecting the overall trend in the marketplace, ECL, MSI, and SSI standard-logic families are expected to decline from about $480 million in 1988 to $450 million in 1989 and 1990. After that, according to many company estimates, this segment is expected to benefit from the need for fast glue logic in high-performance systems based on ECL-based processors, peripherals, and memory circuits, growing to about $510 million in 1993. Also taking advantage of the need for high-speed glue logic in ECL-based designs is programmable logic, which is expected to grow from between $10 million and $15 million in 1987 and 1988 to about $250 million by 1993.

Two features are making ECL more attractive to a wider range of designers: its very high switching speeds and its ability to drive transmission lines with high capacitive loads, says Joseph Vithayathil, ECL marketing manager at Synergy Semiconductor Corp., Santa Clara, Calif. ECL's speed derives from two of its characteristics, he adds. One is that the voltage swings defining the 0s and 1s are smaller in ECL than they are in TTL or CMOS. The other is that unlike TTL, ECL is a nonsaturating logic, which operates only in the cutoff and active modes, allowing the transistors to operate in a semiready state.



Explosive growth is coming in the relatively placid ECL marketplace, thanks to a new technology thrust that's boosting density and lowering power, as well as hiking speed.

And the fact that ECL has a very high input impedance and low output impedance makes it desirable for driving high-capacitance loads.

Other attractive features of ECL include its ability to operate over a wider temperature range than either TTL or CMOS and its use of a relatively constant current derived from the supply rails, eliminating power-rail spikes that plague both CMOS and TTL designs.

> The difficulty of designing with ECL is now more a matter of perception than reality

And no inverters are needed in ECL, because the logic block that produces any given function also produces its complement. Also, ECL's use of emitter-followers means that outputs can be designed to drive as many similar circuits as desired, eliminating the need for special power and line drivers often called for with TTL and CMOS.

The traditional disadvantage of ECL is that the small logic swings (800 mV versus 1 V for TTL) and higher speed tend to create significant voltage and current transients, with noise margins of only 250 mV versus 1 V for TTL. To compensate for these transients, designers have had to lay out their boards to include microstrip transmission lines and make sure that the circuits are properly grounded.

Add to this the fact that ECL has traditionally been a power-hungry bipolar technology and that two power supplies are required, says Robert Lutz, president and CEO at Aspen Semiconductor Corp., San Jose, Calif. So it is no surprise that systems designers have traditionally limited ECL to leading-edge systems that need to eliminate every picosecond of gate delay and every nanosecond of circuit propagation delay.

"However, with the new bipolar process technologies that are emerging, in which gate power dissipations have dropped from milliwatts to microwatts, the power-hungry designation is not quite as true," Lutz says. Also changing the power/speed equation is the emergence of lower-power biCMOS and GaAs alternatives to bipolar ECL.

Furthermore, the difficulty of designing a system with ECL is now more a matter of perception rather than reality, says industry analyst William McClean of Integrated Circuit Engineering Corp., Scottsdale, Ariz. "Many chip makers and systems designers are finding that the same noise and drive problems occur as you push any process or logic family to its limits."

For these reasons, ECL is emerging as the logic of choice for chip input/output circuitry in three different process technologies: bipolar, biCMOS, and

GaAs, says Andrew Prophet, an industry analyst at Dataquest Inc., San Jose. Nowhere is this more apparent than in gate arrays, where all three approaches have been battling for niches at the low-density, 1,000-to-6,000-gate end of the market. Now the competition is moving upward, with array vendors regularly leapfrogging each other on density, speed, and speed/power.

The starting point on the bipolar ECL side are gate arrays available with up to 16,000 or so gates with gate delays in the 100-ps range from vendors as diverse as Advanced Micro Devices, Applied Micro Circuits, Motorola, National Semiconductor, and Texas Instruments, as well as such Japanese competitors as Fujitsu and Hitachi. In the first generation of GaAs ECL-compatible arrays, offerings range in density from 2,000 to 7,000 gates, from companies such as Ford Microelectronics, Gigabit Logic, Triquint, and Vitesse.

Leapfrogging ahead in density are several new bipolar silicon offerings. Available this year from the likes of Motorola, National Semiconductor, and Raytheon, they use 1.5- and 2.0-μm design rules to achieve densities as high as 25,000 to 70,000 gates, depending on the counting methodology used.

First out is Raytheon Corp.'s Semiconductor Division, Mountain View, Calif., with a line of arrays fabricated in a second-generation process developed by Bipolar Integrated Technology Inc. (see p. 90). Using a redesigned T-shaped transistor structure and a more populated version of its original 14,000-gate ECL array, Raytheon is introducing a new family with densities ranging from 25,000 to 70,000 gates.

Also in the running is Motorola Inc.'s ASIC Division in Phoenix, Ariz., with a fourth generation in its MCA series of bipolar silicon ECL arrays. Scheduled to be released to production in the latter half of 1989, the largest chip in the new family will pack over 40,000 gates and implement logic functions that toggle at frequencies above 1 GHz. It will employ a sea-of-cells architecture and four levels of interconnection, three for signal routing and one for power and ground, to achieve a gate utilization of up to 80%.

Another player at the high end will be National Semiconductor Corp., Santa Clara, Calif., which currently offers ECL arrays with up to 15,000 gates using its 2.0-μm Aspect I process. Scheduled for introduction toward the middle of 1989 is a new family of arrays with densities up to 30,000 gates, fabricated in its 0.8-μm Aspect III process. Four metal layers and local polysilicon interconnections yield 90% gate utilization.

In GaAs, second-generation offerings based on relatively tight 1.0-μm design rules are emerging with densities up to 16,000 gates. One of the first such devices comes from Vitesse Semiconductor Corp., Camarillo, Calif. (see p. 92). Designated the VSC10000, it has about 14,000 gates, of which about 10,000 are available for use. It is the first in a family of GaAs arrays.

There are also some biCMOS ECL gate arrays from AMCC and Motorola with densities ranging from 6,000 to 15,000 gates. Motorola is pushing toward much higher densities and is planning to introduce by the end of this year a 250,000-gate array using a 0.8-μm ECL-compatible biCMOS process.

ECL CELLS. In the ECL standard-cell ASIC market, new competition also is appearing. For a long while companies such as VTC Inc. of Minneapolis, Minn., and National Semiconductor have dominated this arena, with standard-cell offerings up to 12,000 to 20,000 gates. Recently, offerings on the GaAs side from Gigabit Logic, Triquent, and Vitesse (see p. 92) have emerged at similar densities and performance.

Upping the ante, National, for one, is moving on to the next stage with its Aspect III, a 0.8-μm bipolar process, which will allow the fabrication of ECL-based standard-cell designs with up to 40,000 gates. Not to be outdone, Vitesse is now working on its next-generation submicron GaAs process, which will allow the design of cell-based circuits with similar densities.

As bipolar design rules push to the submicron range, densities in the 100,000-gate range are not too unreasonable to expect, says William Snow, National's ECL marketing manager.

HIGH-SPEED LOGIC: WHO'S GOT WHAT

Company	Gate Arrays	ASICs*	SRAMs	Standard Logic	PLDs	Process
Advanced Micro Devices (and Monolithic Memories)	X		X	X	X	Bipolar
Applied Micro Circuits	X	X				Bipolar and biCMOS
Aspen/Cypress			X		X	Bipolar and biCMOS
Bipolar Integrated Technology				X		Bipolar
Ferranti		X				Bipolar
Ford Microelectronics	X					GaAs
Fujitsu	X	X	X	X		Bipolar and biCMOS
Gigabit Logic	X	X	X	X		GaAs
Hitachi	X		X	X		Bipolar and biCMOS
Honeywell		X				Bipolar
Integrated Device Technology			X			BiCMOS
Motorola	X	X		X		Bipolar and biCMOS
National Semiconductor (and Fairchild)	X	X	X	X	X	Bipolar and biCMOS
NEC		X	X			Bipolar
Raytheon	X					Bipolar
Saratoga Semiconductor		X	X			BiCMOS
Signetics		X		X		Bipolar
Sony				X		Bipolar
Synergy			X			Bipolar
Texas Instruments	X		X	X	X	Bipolar, BiCMOS, and GaAs
Toshiba		X				Bipolar and biCMOS
Triquint	X	X				GaAs
Vitesse	X	X	X			GaAs
VTC		X				Bipolar and biCMOS

*Standard-cell

SOURCE: *ELECTRONICS*

And riding on the increase in density in both CMOS and bipolar technology, ECL-compatible biCMOS designs approaching 150,000 to 200,000 gates are in the offing.

Fighting it out for the title of the fastest SRAM around at the low-density 1-to-4-Kbit level are a variety of ECL-compatible designs. There are a number of GaAs research prototypes with sub-5-ns access times, but little is commercially available in significant quantities. One of the first is a 1-Kbit design from Gigabit Logic Inc., Newbury Park, Calif., called the 12G014 NanoRAM, with a cycle time of 3 ns. Another GaAs-based SRAM is Vitesse's 4-Kbit ECL-compatible design, the VS12G422ED, with an access time of 4 ns.

On the silicon side, the low-density ECL SRAM market is dominated by such vendors as Fujitsu and NEC, with 4-Kbit designs ranging in access time from 5 to 9 ns. Two newcomers, both startups, are upping the ante in terms of speed in this portion of the market. Aspen Semiconductor, a subsidiary of Cypress Semiconductor Corp. of San Jose, is using a proprietary biCMOS process and a new eight-transistor SRAM cell design in a 4-Kbit SRAM that moves access times below 5 ns (see p. 88). And nearby Synergy has developed a proprietary trench-isolated bipolar process that it's using for another 4-Kbit SRAM, with similar access times (see p. 89).

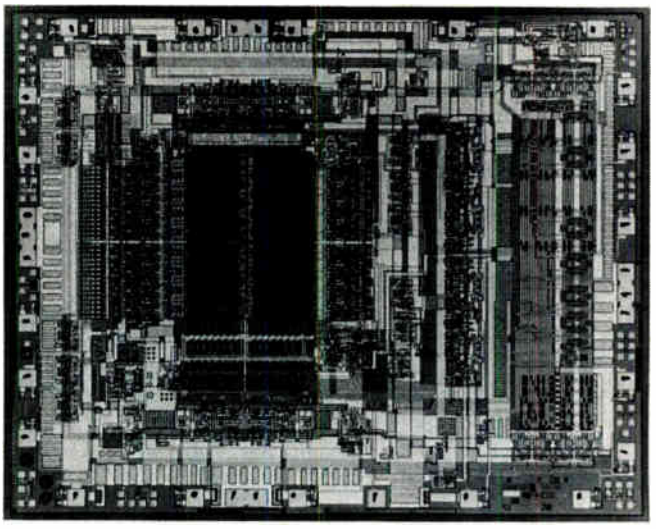
At the 64-Kbit level and above, the action in ECL RAMs is all biCMOS. It is most crowded at the 64-Kbit level with players including such companies as Fujitsu, Hitachi, Integrated Device Technology, NEC, and Saratoga Semiconductor. Using 1.5- and 2.0-μm design rules, such devices range in access times from 15 to 25 ns.

Just now coming into volume production are a trio of 256-Kbit ECL BiCMOS SRAMs from Fujitsu, Hitachi, and National Semiconductor, all of which have access times hovering around 10 to 12 ns. Players who plan to enter the fray at this level in 1989 include Integrated Device Technology and Saratoga.

JOINING SRAM BATTLE. Another new player in the ECL SRAM arena is Motorola. It will introduce 64- and 256-Kbit devices, with samples appearing later this year. It will use the same biCMOS process as its gate arrays.

One indicator of things to come in ECL is the ever-increasing level of integration and diversity. Currently, most ECL LSI standard products are bit-slice or DSP peripherals. But in development are a number of bipolar and biCMOS RISC-based microprocessor designs that offer the potential of pushing cycle times up to an unprecedented 250 to 500 MHz. One of the first ECL RISC machines due out is a bipolar version of Intergraph's Clipper C300, built by Fujitsu Ltd. of Atsugi, Japan. It is scheduled for introduction in the second half of 1989. Also under development at Motorola is an ECL version of the 88000 RISC microprocessor using the company's next-generation Mosaic IV submicron bipolar process.

In terms of standard architectures, there is considerable activity in the Sparc 32-bit RISC microprocessor originated by Sun Microsystems and available in CMOS from several chip makers. For example, Bipolar Integrated Technology Inc., Beaverton, Ore., which has focused on bipolar LSI and VLSI components, is planning to build a bipolar ECL version of the Sparc architecture. And Cypress Semiconductor, another Sparc chip maker, is investigating implementing the design in biCMOS. Another Sparc player, Fujitsu, is also developing an ECL version in either bipolar or biCMOS.



Programmable array logic such as National Semiconductor's PAL16D series can replace four to eight ECL standard-logic circuits.

Another standard 32-bit RISC architecture is the R3000 processor originated by MIPS Computer Systems Inc. Santa Clara, Calif. As a part of its technology agreement with MIPS, Digital Equipment Corp. is reported to be planning a bipolar implementation of the R3000 capable of execution cycle times in the 100-to-200-MHz range. Integrated Device Technology Corp., Santa Clara, which has opted for the MIPS design, is planning a biCMOS follow-up to the present CMOS implementation.

Well under way toward final implementation is a 500-MHz, 250-million-instruction-per-second RISC chip set from Tektronix Inc., Beaverton, Ore. It uses a proprietary submicron bipolar process and a differential ECL-based cell library, based on an architecture developed by the Center for Integrated Electronics at Rensselaer Polytechnic Institute, Troy, N. Y..

Nor is GaAs being ignored. Texas Instruments Inc., Dallas, using its 2.0-μm heterojunction bipolar GaAs process, has demonstrated a 100-MHz 32-bit processor based on the same Stanford University design that MIPS used as a basis for its R3000. TI plans to shrink the design by April, and to achieve a sustained 200 million instructions/s by 1991. Also, Gigabit Logic and Prisma Corp., Colorado Springs, Colo., have entered into an agreement to produce a complete family of GaAs custom logic and memory circuits incorporating the proprietary 32-bit RISC architecture the latter company has developed for its family of real-time supercomputers.

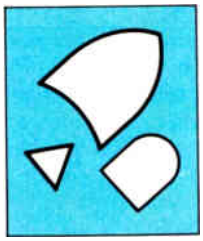
If further evidence of the continued growth and vitality of the ECL marketplace is necessary, one need only look at the MSI/SSI glue-logic segment, says Ed Barnett, product marketing manager for high-speed ECL at Fujitsu's Standard Products Division in San Jose. Unlike standard-logic offerings in TTL and CMOS, which are declining or flattening, ECL standard logic is remarkable not only for its continued modest but steady growth, but also for its growing diversity of offerings.

Still dominated by 10K and 100K offerings initially developed by Motorola but extensively second-sourced by companies such as National Semiconductor and Signetics, family offerings are diversifying both in terms of family types and processes used. Where current offerings are in the 600-to-900-ps range, new families such as Gigabit's GaAs-based PicoLogic family and Motorola's Eclips Mosaic III ECL family push performance to the 300-to-500-ps range. Also considering entry are companies such as Aspen/Cypress, Signetics, and Synergy.

And for those requiring a higher level of glue-logic integration, the number of vendors offering ECL PLDs is expanding. Already offering ECL programmable array logic are AMD, National Semiconductor, and TI, with 7-to-10-ns products. A newcomer is Aspen, which is offering samples of an asynchronous ECL PAL, the 3-to-6-ns 16P8, fabricated using the bipolar module in its proprietary STAR process. Also considering entry are Signetics and Synergy. □

ASPEN SHOWS BICMOS CAN YIELD FAST SRAMs

BiCMOS has the punch to duke it out in the arena of small, fast static random-access memories, says Aspen Semiconductor Corp. The San Jose, Calif., startup is unveiling a new biCMOS 4-Kbit ECL-compatible SRAM with access times as low as 3 ns—a big jump over the 5 to 9 ns for the bipolar competition.



The new SRAM gets its speed from a combination of proprietary circuit-design techniques and advanced bipolar and CMOS processing. Aspen uses an eight-transistor memory cell with CMOS storage circuitry and ECL access circuitry, melded in a novel design that Aspen calls a CMOS-storage emitter-access memory cell.

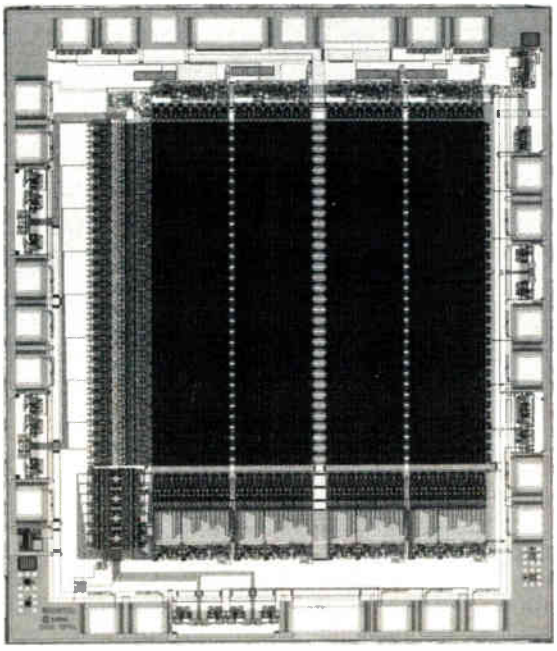
The 1-K-by-4-bit SRAM will be fabricated and marketed by Aspen's parent company, Cypress Semiconductor Corp., nearby in San Jose. Available in sample quantities, the biCMOS SRAM will be offered in models compatible with 10K and 100K input/output schemes, the CY10E474 and the CY100E474. In the high-power, high-speed versions, array access time is 3 ns and power dissipation is 1.14 W. In the low-power versions, access time is 5 ns and power dissipation is 850 mW.

The base for Aspen's memory products and all of its future memory and logic products is a process it calls STAR, for scaled transistors and resistors. This single-polysilicon, double-metal process combines Cypress's 0.8-μm CMOS process with Aspen's bipolar process, which allows the fabrication of npn transistors with 1-μm emitters. STAR begins with twin-tub n-MOS and p-MOS structures fabricated using self-aligned buried layers with thin epitaxial layers and local oxidation. The process uses a titanium aluminum silicide for the metal layers.

STAR is a modular process, says Anthony Alvarez, manager of biCMOS development. That means modules can be deleted from the baseline process to achieve only npn structures or added to build double-polysilicon EPROM or EEPROM structures. Under development is a second-generation process that will further boost performance and density.

The biggest performance boost for the Aspen chips comes from the use of a proprietary cell design drawing upon work done at Stanford University on memory cells that unites CMOS storage with bipolar emitter-access circuitry. These storage emitter-access cells combine ECL-level voltage swings on the word line and ECL emitter-follower bit-line coupling with a static CMOS latch. Alvarez notes that most biCMOS SRAMs combine conventional CMOS cells with bipolar transistors in the sense amplifiers and as drivers for large capacitive loads. In these designs, he says, access time is limited by such factors as the large voltage swings on the word lines and the number of circuit stages required.

In storage emitter-access cells, small word-line swings are combined with emitter-follower coupling to the bit line to minimize word-line delay while at the same time increasing the bit-line charging current. In addition, a static CMOS latch reduces the standby power consumption of the array.



Aspen's 4-Kbit SRAM has access times as low as 3 ns, thanks to a novel design approach. It is ECL-compatible.

Where the standard bipolar or CMOS cell uses either four or six transistors, the storage emitter-access cell employs at least eight. In this design, the read word line serves as the positive supply for the cell's internal latch, and the cell is read by raising this word line. When a high output is stored in the cell, the increase on the read word line is coupled directly to the base of the output emitter-follower. This device forms a differential pair with the sense-amplifier input transistor. The cell is written through the pass transistor, which is controlled by the write control line.

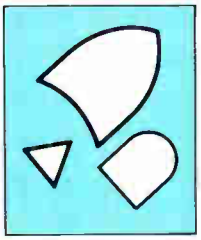
Selection of the read word line is done with bipolar current-switching circuits that have low voltage swings. The logic levels in these circuits are achieved by means of an on-chip, supply-compensated bandgap reference. Push-pull address input buffers provide fast transitions at the input to the row decoders. The word lines are driven by Darlington emitter-followers tied through resistors to a common pull-down current. To ensure that the bit reference tracks the high level of the read word line in the selected cell, the level of the selected word line is monitored with a wired-OR of emitter-followers driven by each of the word lines. The write path of the storage emitter-access cell is similar to that of conventional biCMOS SRAMs. The write address decoding is implemented using dynamic series decoders that are clocked by the write enable signal.

A drawback to previous implementations of the storage emitter-access cell has been their use of a single-ended write structure, Alvarez says. As result, care must be taken to avoid disturbing the unselected cells in the row where the write word line is selected. One step toward avoiding such disturbances is to bias the unselected write bit lines at a level close to the logic levels of the CMOS latch inverters when the read word line is at its low level, says Alvarez. In addition, he says, Aspen designers have shifted to a double-ended write scheme. Also, proprietary circuitry reduces the noise that commonly occurs in such designs.

The main drawback to using an eight-transistor design is that it is limited to small densities, says Robert Lutz, president and chief executive officer. "We see this basic cell having usefulness up to perhaps about 64 Kbits," he says. "Beyond that we will have to go back to the more traditional four- or six-transistor design and use such things as scaling, stacking, and trenching to achieve higher densities without sacrificing speed." Overall, he says, Aspen sees biCMOS as the way to go for densities above 64 Kbits. Below that, he says, either biCMOS or bipolar might be used, especially in ECL.

While initial emphasis is on memories, logic is not being ignored. Aspen and Cypress are introducing a family of high-speed programmable logic devices, fabricated in STAR's bipolar module. First out are the CY10E301 and CY100E301, 10K- and 100K-compatible versions of the 16P8, a 16-input, 8-output programmable-array-logic circuit with a propagation delay of 3 ns at 240 mA. *–Bernard C. Cole*

WHY SYNERGY TAPS ISOLATION OVER A SHRINK



Relatively conservative 1.5-μm design rules can still yield high performance, says Synergy Semiconductor Corp. The Santa Clara, Calif., startup has developed a radically new bipolar emitter-coupled-logic process capable of speeds matching or beating those of many submicron bipolar and biCMOS processes now nearing production.

Called Asset, for all-spacer-separated-element technology, the new process uses two advanced isolation techniques: spacers, which are oxide inserts between device elements and between transistors, and exceptionally deep trenches. Thanks to these techniques, basic transistor size is only 7.5 μm^2—half that of bipolar processes using more advanced design rules—and performance improves as a result.

Another key feature is the use of double polysilicon layers, which let the Asset process be used for both memory and logic. Asset implements a cell with closely matched npn and pnp transistors, resulting in an unusual combination of fast read/write capability and low power.

Scheduled to debut next quarter in sample quantities, initial Synergy products implemented in the new process will be two 4-K-by-1-bit ECL static random-access memories, the 10K-compatible SY10474, and the 100K-compatible SY100474. At 4.5 V, access time is only 3 ns and total power dissipation 1.125 W. Typical die size, he says, is 15,700 $mils^2$.

These specs beat or match those of many bipolar and biCMOS SRAMs that use much tighter design rules, says Ralph Cognac, vice president of marketing. Generally, power and performance on comparably sized SRAMs range from 8 ns and about 1.1 W for ECL-compatible biCMOS implementations to 3 ns and 1.6 W for state-of-the-art bipolar ECL parts.

Such breakthroughs in performance and power required some dramatic design changes, says vice president of technology Larry J. Pollack. "What is required is a complete rethinking of bipolar processes and circuit implementations," he maintains. That's why Asset uses both trenches and spacers.

Throughout the chip, isolation between gates and cells is achieved through trenching, which, Pollack says, translates into 40% tighter device pitches and more than a twofold decrease in gate area. The use of trench isolation also minimizes parasitic capacitances, which translates into decreased delay and higher performance at lower power.

The Synergy process replaces oxide isolation with trenches that are 7 μm deep—two to three times that used in leading-edge CMOS dynamic RAMs. Not only does this reduce the area required for a particular gate or cell by twofold, it reduces both the total number of process steps and the number of critical steps, Pollack says. "Although a difficult art to master, trench isolation, once understood, is more easily manufacturable" than oxide isolation, he says.

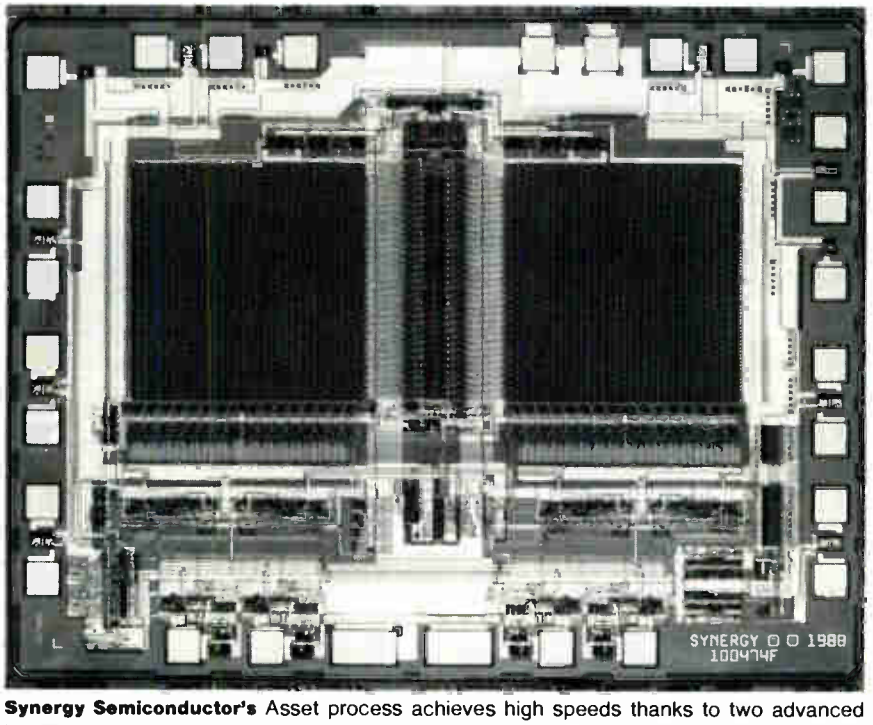
Complementing the trench isolation is a proprietary localized isolation technique that involves placing the special oxide inserts called spacers between the n- and p-elements in the npn and pnp transistors and between transistors in a logic gate or SRAM cell. This scheme further reduces the overall area required to implement a particular function.

Unlike many of the advanced bipolar and biCMOS processes optimized for the manufacture of SRAMs, the Synergy process is designed for the manufacture of both memory and logic. A key element in this optimization is the use of double polysilicon layers and contacts. The double polysilicon allows the implementation of peripheral logic in a more compact manner. It also allows the design of a proprietary cell that eliminates unnecessary space between elements in the SRAM structure.

Synergy designers also have come up with proprietary SRAM circuit innovations that Cognac says combine the benefits of both diode-clamped and pnp-loaded cells. The first, typically used in low-density, high-speed SRAMs, offers very high-speed read and write capability, but has the disadvantage of higher power, high alpha-particle sensitivity, and large cell size. The pnp-loaded cell, on the other hand, boasts a small cell size and lower power, but requires the use of a nonstandard pnp transistor in a standard npn process. The Synergy design implements a cell with closely matched npn and pnp transistors, resulting in a low-power cell equivalent in size to a pnp-loaded cell, but with the balanced fast read/write capabilities of the diode-clamped approach.

Initially, says Cognac, the company is going to target the market for small but very fast SRAMs in data and cache-tag applications. At the 4-Kbit level, the present design is being specified conservatively at 3 ns. "However, as we more fully characterize the part, we feel that we may eventually be able to offer 4-Kbit SRAMs with below-2-ns access times," he says. In development, he says, are several 1-Kbit designs that the company believes will come in with access times at 1 ns or below.

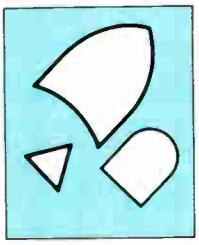
Also under consideration are smart memories—parts with logic. "Because we have a process optimized for both logic and memory, we feel we will have an advantage over competitors with processes optimized for either logic or memory alone," Cognac says. *–Bernard C. Cole*



Synergy Semiconductor's Asset process achieves high speeds thanks to two advanced isolation techniques: spacers, or oxide inserts between elements, and deep trenches.

BOOSTING DENSITY IN A 2-MICRON PROCESS

For most manufacturers, chasing after high density in emitter-coupled logic means making one crucial design decision: to push geometries to 1 μm and below. But one company has pulled two- and threefold density boosts out of the hat with a radically different approach. Raytheon Corp.'s Semiconductor Division accomplishes this feat with an innovative fine-tuning of its 2-μm process, and gets hefty increases in speed to boot.



The architecture results in a family of ECL gate arrays ranging in density from 5,700 to as many as 25,000 to 70,000 gates, depending on the measurement scheme. That's way ahead of the ECL competition, both in bipolar silicon, where 16,000 is typical at the high end, and gallium arsenide, where 12,000 to 14,000 is the maximum so far attained.

In addition, the Mountain View, Calif., company has increased transistor switching speeds by at least 25% and cut chip delays by as much as 30% to 35%. And the speed rise comes at virtually no increase in power dissipation. All this magic is accomplished with a combination of subtle process improvements, a more efficient gate-layout scheme, and multiple layers of interconnection.

The new family of Raytheon arrays is fabricated by Bipolar Integrated Technology Inc., Beaverton, Ore., using a variation of its BIT100 bipolar 2-μm process—the same one used in Raytheon's earlier series of 3,500-to-10,000-gate ECL and TTL-compatible arrays. The family includes the 209,920-transistor 40E26S; the 76,960-transistor 15E18S; and the 46,200-transistor 10E12S. Those counts translate into a density range of 15,000 to 70,000 gates, according to one common measurement scheme, which uses a three-transistor gate as the fundamental unit.

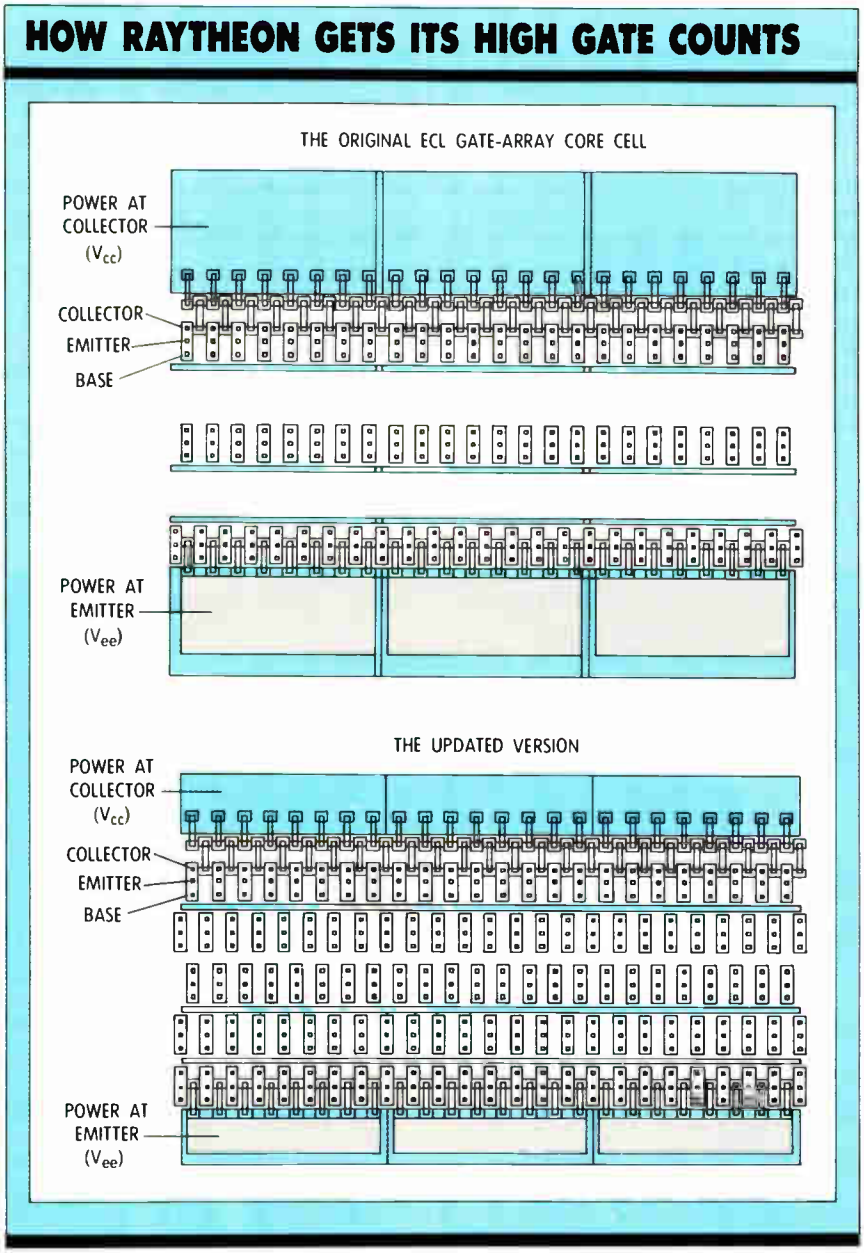
However, Raytheon uses a much more conservative measuring stick, says Jack Van Den Heuvel, product marketing manager: it populates an array with a given macrofunction and determines the number of equivalent gates required. Using a multiplexer as the basic function, the density range is 9,600 to 42,752 gates. The most bare-bones configuration yields a 5,700-gate count.

TRANSPARENT. All the process improvements are essentially transparent to the design methodology, Van Den Heuvel says. This means that engineers can upgrade their designs with the same cell library used in the earlier, lower-density devices. Added to the cell library, he says, are a number of analog macrofunctions that will make mixed-mode analog/digital designs practical. They include a 200-MHz phase-locked loop, high-speed 1-ns comparators, 200-MHz six-bit flash analog to digital converters and 8-bit digital to analog converters, analog multiplexers, and an amplifier with a 500-MHz gain-bandwidth product.

Pricing in 1,000-piece quantities is $195 each for the 10E12S in a 149-pin grid array; $350 each for the 15E18S in a 232-pin PGA; and $975 each for the 40E26S in a 312-pin PGA or leaded chip carrier. Chips are available now in sample quantities.

Like its earlier family of arrays—the 12,800-gate 70E18, the 7,750-gate 40E12, and the 4,580-gate 1ME12—the new family uses a contiguous-row topology rather than one based on fixed-position cells, as is common in traditional ECL arrays. In the fixed topology, cells are positioned horizontally or vertically to form rows, between which are dedicated routing channels. Some logic functions fully utilize the cell components—output emitter-follower transistors, terminating resistors, current-switching transistors, and resistors. But most functions do not, resulting in unused components and poor

HOW RAYTHEON GETS ITS HIGH GATE COUNTS

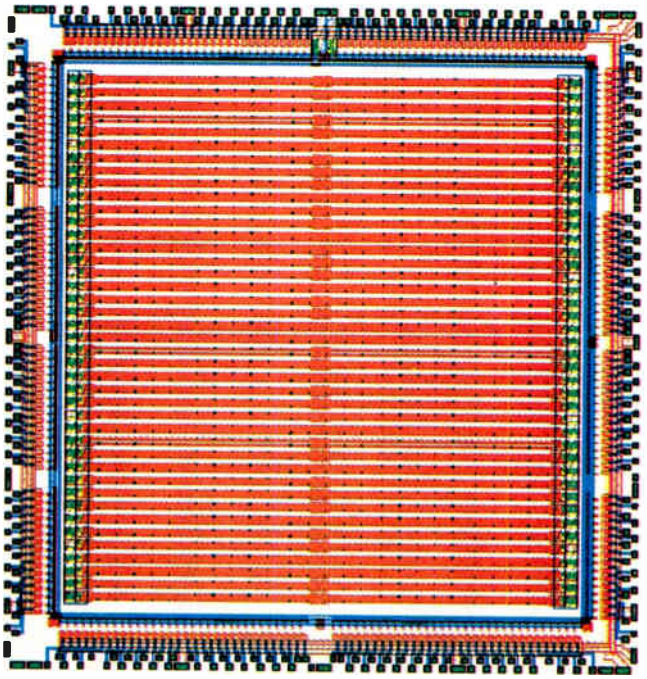


A contiguous-row topology is at the heart of both Raytheon families: in the original series (top), rows are separated by routing channels. In the new series, this space is filled with transistors.

silicon efficiency, says Van Den Heuvel. Another disadvantage, he says, is that circuits requiring large feedback-oriented buses use up the available routing tracks, and entire cells are wasted as additional routing channels are added.

But Raytheon's choice of a contiguous-row topology circumvents these problems. In this setup, an array contains adjacent rows with reference-voltage generators, termed bias cells, situated at each end. This scheme minimizes the width of the reference-voltage buses, allowing more routing channels.

In the original family, the rows are separated by routing channels that accommodate the first metal interconnect level, with a second level routed vertically over the entire core. The new arrays use the same basic concept, except that the space allocated for interconnect channels for intra-macrocell routing has been filled with transistors. When routing is required, says Van Den Heuvel, channels are formed over the transistors. Also, a third layer of metal interconnect has been added. This setup offers one big advantage: in the original family, signal and power routing are shared in both levels, and this affects overall gate utilization; but in the new arrays, power is distributed in the third level, with the other two levels used exclusively for signal routing.



The new arrays pack as many as 70,000 gates, and they are also 30% to 35% faster than the family on which they are based.

The end result of the contiguous-row topology is the more efficient construction of macrocells, says Van Den Heuvel. Since all transistors and resistors can be configured either for switching or for output emitter followers, each macrocell is built with the minimum amount of silicon, regardless of the amount of logic or the number of outputs required. This means fewer wasted components per die and more customizable macrocells.

The impact of these improvements is most apparent in the density of the family's basic building blocks—the minimum addressable placement sites (MAPS), or the area between two resistors and two power buses. Where in the original array each MAPS measures 160 by 16 μm and contains six transistors and six resistors, in the new topology the same MAPS area contains 10 transistors and six resistors.

BETTER UTILIZATION. This increases gate density and utilization in three ways, says Van Den Heuvel. First, it means that three levels of series gating can be used, in effect increasing the functionality per unit area of silicon by almost 30% over the previous two-level gating approach. Second, the presence of more transistors per unit area allows more compact macrofunction layouts. This serves to decrease the interconnect metal delays and improves the performance of the macro.

Finally, the presence of more transistors allows for paralleling these devices to increase the tree currents in the macros without materially increasing the silicon area required for the function. The combination of these improvements, according to Van Den Heuvel, means that while the standard macrofunction still has a tree current of 80 μA, a high-performance macrofunction now has a tree current of 160 μA. While highly dependent on paths and macrofunctions, Van Den Heuvel says, performance improvements over the earlier arrays for equivalent functions is on the order of 33% or more.

The performance enhancements are partly due to a retooling of Bipolar Integrated Technology's BIT100 process. The new version, BIT111, also keeps down power dissipation per gate. In both processes, says Van Den Heuvel, the basic transistor area is about 14 μm^2. The difference lies in device shapes. Where the original transistor is roughly rectangular and has equivalently sized collector, emitter, and base structures, in the new process the transistor is key shaped and has a larger collector structure with smaller emitter and base structures. The effect is to increase the capacitance of the collector and reduce the capacitance of the base and emitter, he says. This results in a significant reduction in output emitter-follower capacitance, allowing an increase in the cutoff frequency of about 25%—from about 5 GHz to about 6.25 GHz. At the same time, he says, the resulting power consumption per gate is the same as that for the earlier process: about one tenth the power of comparable ECL technologies, while maintaining a 300-ps average unloaded gate delay. For a typical gate structure, the speed-power product for the new arrays is about 9.1 pJ, about 30% to 40% lower than that of the original Raytheon family.

Despite the fact that the transistor structure has been altered, the contacts for the collector, emitter, and base remain in the same location as in the BIT100 process. As a result, the metal interconnect patterns for a particular design being migrated from the earlier family of arrays are compatible, according to Van Den Heuvel.

Input/output cells are situated around the die periphery for input, output, and bidirectional operations. They can be linked to 10K or 100K ECL and TTL; dual-mode TTL and ECL; or tri-mode ECL, TTL, and CMOS. In lieu of group bias cells in the chip corners, each output driver contains its own voltage-compensated bias cell. This configuration provides improved noise rejection and consistent dc output-voltage tracking over temperature. The new series boasts a maximum of 256 I/O cells, against 128 in the previous generation.

Typical power dissipation for the 10E12S is 5.2 W, evenly divided between the core and the I/O. On the 15E18S, power dissipation is 8 W, also evenly divided, and in the high-end 40E26S, it's 17.2 W, with about 10.8 W in the core.

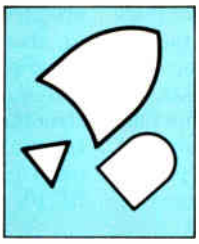
For designers, there's one additional bonus inherent in the new arrays: because the locations of the transistors in the arrays remain unchanged from the old series to the new, users of the original family can migrate to higher densities without any modifications to the basic macrocell library.

Optimized for use in an array's minimum addressable placement sites, Raytheon's ECL macrocell methodology allows designs to be entered hierarchically with the chip signal pins and top-level modules. Hierarchical schematics allow a structured design approach, taking advantage of functional circuit blocks for regularity and, in some cases, a bit-slice approach to optimize bit-to-bit performance by tracking symmetry.

By taking advantage of the flexibility of the ECL transistor design, the methodology also allows custom macrocell development for critical paths and the merger of several general-purpose macrocells in critical paths, thereby greatly improving silicon efficiency. *–Bernard C. Cole*

NOW POWER-SAVING GaAs EQUALS ECL DENSITY

An alternative to bipolar silicon emitter-coupled-logic gate arrays and standard-cell application-specific integrated circuits is on the way. Vitesse Semiconductor Corp. is jumping into the ECL marketplace with gallium arsenide offerings that match bipolar silicon in both density and speed. The VSC10000, a 14,000-gate ECL-compatible gate array, and the 22,000-gate VCB50K standard-cell library are available. These new ASIC capabilities mean GaAs has finally caught up to ECL in density and cost, and at much lower power consumption, says Thomas Dugan, director of marketing at the Camarillo, Calif., company.

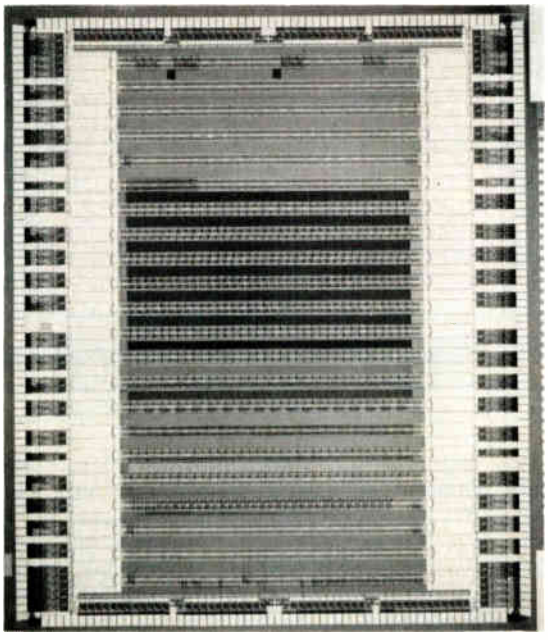


Fabricated using a 0.8-μm, four-layer-metal n-MOS-like process, both the gate array and the standard-cell offerings attack the weaknesses of bipolar ECL technology while offsetting its advantages. A typical ECL NOR gate, the basic logic building block, for example, contains six bipolar transistors and three resistors, and operates on two power supplies. Each ECL circuit tree is designed with a differential input to allow signals to be passed differentially throughout the logic array. To accept single-ended input signals, the chip must also include a master-reference voltage generator, which fans out to several main slave-buffer amplifiers. In turn, each main slave buffer services several macrocell columns, each of which contains three or four small slave buffers. The main slave and small slave buffers are necessary to provide the load-in sensitivity required by the ECL circuits. Besides consuming up to 3 W of power, the reference-voltage distribution scheme uses chip space that would otherwise be used for signal routing.

The same function in the Vitesse design uses just three transistors and one 2-V power supply, Dugan says.

To offset the fact that bipolar silicon transistors inherently have greater current capability than GaAs transistors of the same size, the Vitesse offerings use a proprietary transistor-interconnection technique called "squirt buffering." This design causes transistors in the macrocells to deliver a high-current spike when switching on or off, thereby precharging metal-line capacitance before signal transmission. The result is ECL-like performance. Typical line delay is just 80 ps/mm, and worst-case delay for a two-input buffered NOR gate is 120 ps at 1.5 mW. Contributing to this relatively low power dissipation is the small standby current of the GaAs MES FETs, which is a fraction of the dc bias current used by ECL emitter-followers. In a conventional high-performance ECL array this current can be as high as 1.6 mA.

The initial part in Vitesse's family of GaAs gate arrays is the VSC10000, the core of which contains 22 columns of depletion- and enhancement-mode MES FETs resembling a CMOS-channeled gate array. The core is optimized from a maximum of 13,376 internal cells (two-input NOR gates), up to 1,114 high-drive buffered D-type flip-flops, or some mixture of each. The core cells have 100% utilization.



New gallium arsenide ECL offerings by Vitesse match bipolar silicon in both density and speed.

Positioned on the chip's periphery are 100 input/output cells and 92 input cells. The input cells work with single-ended or differential signals at ECL or GaAs logic levels and produce inverted or noninverted differential outputs. Because the I/O cells account for about 650 equivalent gates, total gate count for the VSC10000 is about 14,026.

A latch in each input cell lets the cell perform logic-level conversion of ECL inputs without the time delay otherwise encountered with a straight receiver. The same is true for the outputs of the latched I/O cells, which also perform logic-level conversion to work with 100K, 10K, and 10KH ECL signals, GaAs, or mixed ECL and GaAs signal levels. A smaller array, the VSC5000, contains half as many gates and has the capacity for up to 6,000 NOR gates and 500 flip-flops. Available with 120 ECL- and TTL-compatible I/O lines, the 5-W VSC5000 will compete with 5,000-gate, high-speed ECL arrays typically dissipating from 8 to 12 W.

The Vitesse VCB50K Portable GaAs Standard-Cell Library offers the circuit complexity and breadth of megacells heretofore available only in much slower CMOS standard-cell offerings. Using the same high-yielding process as the VSC10000 gate array, today's customers can design standard-cell circuits with up to 22,000 gates. This cell capability allows users to reach complexity levels well above other ECL or GaAs offerings while remaining in an air-cooled system.

The integration level of the initial VCB50K release is limited to approximately 22,000 two-input NOR gates. But that's only the beginning, says Vitesse. Projections based on yields of 10,000-gate arrays indicate that 50,000-gate cell-based designs will be possible by late 1989 and 100,000-gate designs will show up by 1991.

The first release of the VCB50K has more than 40 cells including different types of gates, multiplexers, flip-flop cells, buffers, and ECL and TTL I/O cells. Both single-ended and differential ECL I/O cells are available as well as bidirectional TTL and ECL cells. Commercial, industrial, and military temperature ranges are supported. Nonrecurring engineering costs for VCB50K development vary from $65,000 to $175,000 depending on the complexity of the circuit. Production pricing is 3 to 5 cents per gate.

The VCB50K cell library has been optimized for performance at clock rates of up to 3.5 GHz. Speed/power trade-offs can be made by choosing between cells using direct-coupled FET logic and source-coupled FET logic. The direct-coupled versions of the cells operate at clock speeds in excess of 1.5 GHz and consume very little power. The source-coupled cells are suitable for operations approaching 4 GHz at modest power consumption.

To vie for higher-density applications, Vitesse will introduce the VSC20000 gate array next summer. This 10-W array will have twice as many gates as the VSC10000 and be capable of having up to 28,000 NOR gates and 2,400 flip-flops to compete with 40-to-50-W ECL arrays of the same density. The VSC20000 will have 264 ECL-, TTL-, and GaAs-compatible I/O lines. *–Bernard C. Cole*

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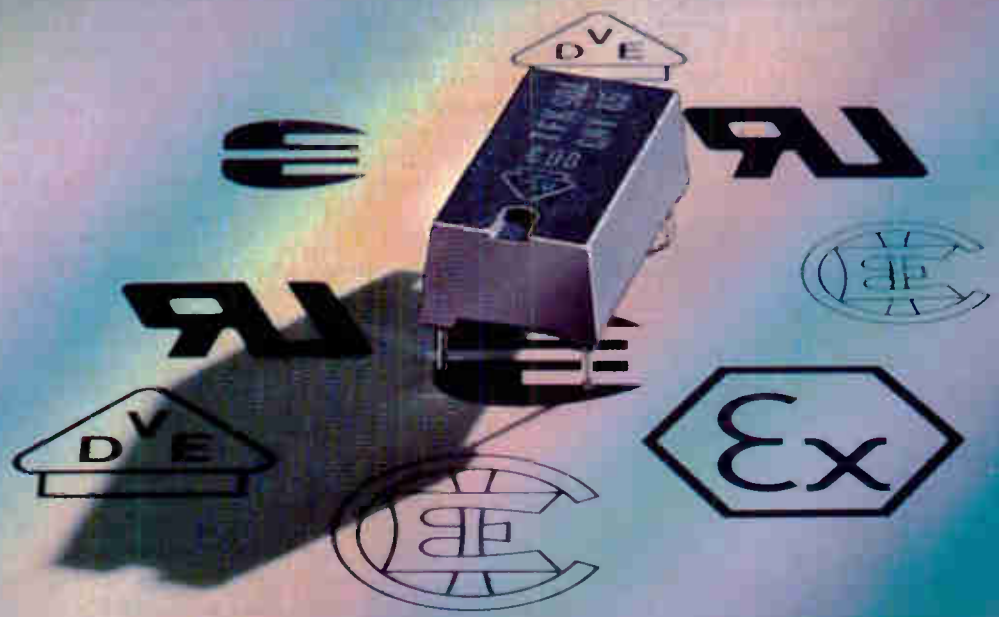

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FIBER'S NEW BATTLEGROUND: CLOSING THE LOCAL LOOP

Phone companies are vying with cable-TV firms to install lines in this huge market

by Larry Waller

The breakup of the Bell Telephone System in 1984 set the stage for what might be called the fiber revolution, the sudden dash by competing long-distance telephone carriers to replace copper wires with mile after mile of fiber-optic cable. Today, just five years after the breakup, optical fibers have made it to within a mile or so of most U. S. homes. And now makers of fiber-optic cable and components, who have long eyed this local loop as a potential gold mine, are beginning to see their way to the end of the line.

These companies believe that "the last mile"—the final link between the average American living room and the telephone branch exchanges where main long-transmission lines terminate—will provide booming business for years to come. Not only will telephone services be channeled into the home with high-bandwidth optical technology, but so will high-definition TV, data, and other services. And after nearly five years of waiting for regulatory roadblocks to be undone, these equipment vendors—along with the phone companies they supply—are seeing a quickening pace of events that could spark a brand new wave of fiber installations.

In Washington, the loosening of the regulatory strings began last October, when the Federal Communications Commission tentatively concluded that there may be reason to relax the rules that currently prevent phone companies from owning or operating cable-TV businesses within their designated service areas. Although the Cable Act of 1984, which contains the prohibition, would require an act of Congress to repeal, the FCC wants to see what people in industry think about the issue.

The commission asked interested parties to comment by mid-December. It may still be months before it concludes its study of the responses, though some observers expect a ruling as early as March. Whatever the timetable, it seems clear that the agency's decision could be the key to the opening of this market.

If the FCC recommends to Congress that it repeal the law, and Congress agrees to do so, the seven regional Bell operating companies will suddenly find themselves able to compete with local cable distributors—but only if they install sufficient bandwidth to carry both TV and telephone service into the home. To do it, they will have to turn to fiber.

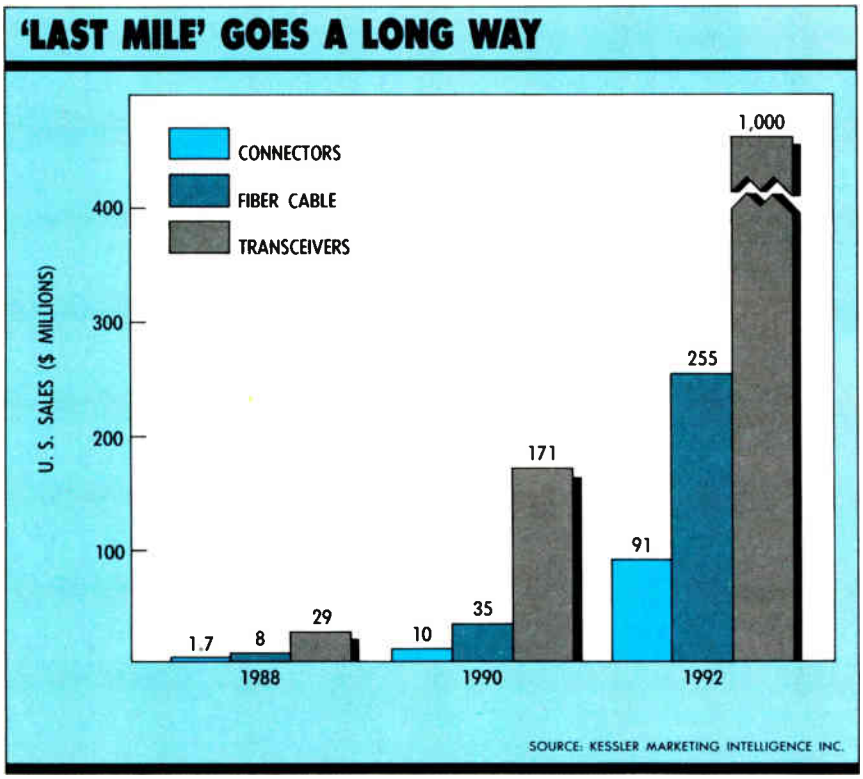
It's enough to scare the wits out of the cable-TV industry. "It's a potential major problem for us," says Brian James, director of engineering at the National Cable Television Association in Washington. He says phone companies can't be trusted to price their services fairly, and may subsidize their fledgling TV businesses by pushing up phone rates. "I don't think the FCC has enough auditors to keep an eye on everything the phone companies are doing," he says.

STRUGGLING NO MORE. But at the FCC, the prevailing feeling is that the once small and struggling cable industry has come of age, and in most cases, its companies are operating as unregulated monopolies. Having grown somewhat fat in recent years, the theory goes, cable companies may no longer deserve the special protection they once enjoyed.

"The cable companies aren't the little struggling businesses they were 20 years ago," declares an FCC staff member who is close to the issue. "There's a question of whether they need to be protected anymore, or whether some new competition would be better."

More competition in the form of phone-company participation in cable is a pivotal precondition for the takeoff of fiber in the local loops, say most industry observers. By their reasoning, economics and competition will drive the last-mile market, depending on how the FCC or Congress change the regulatory climate. Within this framework, the single biggest factor is the looming presence of high-definition TV—the next generation of television, which promises more than twice the resolution seen in present sets.

"In my opinion, [HDTV] is the major driver" for installing fiber in the local loop, says Michael K. Barnoski, president of PCO Inc., a Corning Glass Works subsidiary in Chatsworth, Calif., that sells the electronic and optical components needed to make a fiber network run. (Last month, IBM Corp. bought a 25% stake in the company.) He and other knowledgeable sources expect HDTV to



move quickly into the U. S. consumer scene in the 1990s. And since cable already serves a significant and growing share of U. S. households, it will be a most important delivery medium.

But Barnoski says HDTV will demand a very big piece of bandwidth, far more than the capacity of most present cable systems (although the precise amount won't be known until the FCC fixes a standard). As a result, the potential for selling new hardware is huge. But James of the cable-TV association disputes this bandwidth assessment, saying that most cable companies today have sufficient capacity to deliver HDTV to their customers. And those that don't have the capacity yet will have it by the time HDTV sets start showing up in U. S. homes, he adds.

That doesn't mean cable companies aren't interested in fiber, though: James says that several major cable firms are studying ways to use fiber optics to improve transmission from their central offices to the minihubs that deliver TV to their customers.

BEARING FRUIT. And that points up the main advantage phone companies have over their rivals in the cable business: they already have in place a fiber-optic backbone for their networks, while cable companies are still in the planning stages with fiber. That's why many industry watchers believe that if cable and phone companies could lay aside their dispute, they might be able to find profits together. The phone companies could run fiber in the local loops and then lease capacity to the cable operators. In fact, such cooperation is already bearing fruit, according to Timothy Davis, president of Aster Corp. of Milford, Mass., which makes optical transceivers. He points, for example to such showcase installations as the joint venture between GTE Corp. and Apollo Cablevision Inc. in Cerritos, Calif. (see story, this page).

As a result of the telephone companies' head start in fiber optics, industry analysts like John Kessler, president of Kessler Marketing Intelligence Inc. of Newport, R. I., think it's a cinch that they will be in the cable-TV business by 1992. Some sort of Congressional action between now and that time will clear the decks, he predicts.

Based on that expectation, Kessler forecasts a heady five-year growth span ahead for local-loop hardware: fiber cable, transceivers, and connectors. "Those three elements combined represent a 1988 market of $39 million that will jump to $1.35 billion in 1992," Kessler predicts. Adds PCO's Barnoski: "taking fiber to the home dwarfs anything we've ever looked at. The numbers are huge."

While the scope of the market potential is starting to become clear, credit for getting this phase started must go to the regional telephone companies. Because they understand fiber and recognize a lucrative future in it, they are pushing hard to be in a position to operate last-mile distribution links.

They contemplate changes in the law that will allow offering a whole range of things beyond "plain old telephone service"—what the industry calls POTS, says Davis of Aster. His company is right in the middle of this business, supplying the couplers and transceivers necessary for cable systems.

TRUE ISDN. "The telephone companies are the strongest force in the market," he says, with "all seven of the Bell operating companies pushing fiber-to-home trials." Additional services such as videophone, enhanced telephones, security alarms, and power metering—a true implementation of an integrated services digital network—could double average revenues from $20 to $40 per home each month, in Davis's view.

On the other hand, the virtual monopoly enjoyed by cable-TV firms since their inception has created little incentive for them to consider a fiber-optic subscriber loop. With fiber obviously destined to play a role, this was one reason the FCC in October decided to examine whether or not to relax the rules.

Not surprisingly, the battle lines have already formed and the first verbal salvos have been fired. "There's no burning need for the phone companies to wire fiber into the home," says James of the cable-TV group. But he does acknowledge that fiber could make other phone services, such as multiple private phone lines in a single home, easier to deliver. And the worry from his side is that once that fiber is there, the phone companies won't be patiently sitting by while loads of bandwidth goes unused.

Meanwhile, the cable camp has found itself with an unlikely ally in its campaign to keep the phone companies out of the TV game: TV broadcasters. The National Association of Broadcasters urged the FCC in December "not to act hastily in modifying its telephone company/cable television cross-ownership rules." Broadcasters are already worried that cable will beat them to the punch with the abili-

TWO FIRMS LINK ARMS TO RUN THE LAST MILE

Planners at both GTE Corp. and Apollo Cablevision Inc. regard their linking in Cerritos, Calif., as a prototype of the kind of cooperation that can occur when far-sighted city officials, a telephone operating company, and a cable-TV company team up to provide "last-mile" services to subscribers. Field trials are under way in Cerritos, Calif., that will include interactive video, video on demand, and video telephone, as well as conventional telephone service, on both coaxial and fiber-optic cable.

In Cerritos, GTE is "trying to find out how to bring information-age capabilities to reality in an existing city," says Thomas Gillett, director of advanced operations testing for GTE Service Corp. of Stamford, Conn.

Field trials are under way to test both fiber-optic and coaxial cable

Cerritos is about 20 miles southeast of Los Angeles, has a population of 56,000, some 16,000 homes, and about 2,000 businesses. A fortuitous set of circumstances combined to bring the city, Apollo Cablevision, and GTE together, says Gillett.

"Cerritos had no cable-TV company, and the city was looking for one to provide advanced services to be delivered underground to preserve the city's attractiveness," Gillett says. The local operating company, GTE California, was looking for a partner to serve Cerritos when the city asked for a cable-TV system, "and we [GTE] were searching for a place to test advanced services and technologies. We and Apollo Cablevision were both anxious to work with the city."

GTE got permission from the Federal Communications Commission two years ago to install a coax net to distribute the TV signals provided by Apollo Cablevision, headquartered in San Luis Obispo, Calif. A year later, GTE sought FCC permission to install a single-mode fiber-optic system. That permission is expected this month, Gillett says.

"The coax net will pass all 16,000 homes," Gillett reports. "As we build it, we will leave vacant conduit in the same trench to be filled with fiber cable, setting up a competition between the two technologies." The fiber links will serve about 1,000 homes. Gillett expects all of the above services to be available on fiber, and most of them on coax, by midyear. He won't reveal the overall cost of installation or the cost per subscriber site.

Coax can't provide video on demand, Gillett says, but fiber can. "If you want to watch *Top Gun* at 8:13 p.m., you can do it on a fiber network but not on coax. The field trial will test demand to determine which medium is desired and which combination to move forward with." Apollo will bill subscribers for video services and GTE will bill for phone and videophone. Once the system is installed, security alarm and utility-meter monitoring may be added. *–Lawrence Curran*

ty to deliver HDTV pictures. And the specter of aggressive new competitors in the cable field—especially ones with the financial and technical resources of the telephone companies—could only accelerate the jump to HDTV. Regardless, cable firms are welcoming all the help they can get to hold the line against the oncoming phone companies.

While the political battle rages over the next couple of years, the attention of fiber-equipment suppliers already is focusing on defining the hardware needs of a fiber local-loop architecture. The technology for all the parts is in hand, they say, from solid-state lasers for transmission to photo detectors for reception—but a detailed configuration is not yet set. Still to be resolved are such factors as distribution architecture and whether the transmission mode will be AM or FM.

Numerous architectures have been proposed; typical is the one outlined by Bellcore, the research arm of the seven Bell operating companies in Livingston, N. J. The plan Bellcore is suggesting to the phone companies would put 622 Mbits/s of bandwidth in the fiber-optic subscriber loop, and provides for 64-Kbit/s radio transmission from the central office to portable equipment.

Always guiding this development is the invisible hand of telecommunications economics—getting the hardware prices down under the $150-per-installation mark that most experts agree must be the target. Aster's Davis says economics are on the side of the phone companies. They have already managed to push the cost for each subscriber location or home down to less than $1,500 from about $2,500. Because fiber is nearing the twisted-pair/coaxial-cable figure of $800 to $1,200, incentives exist to install more fiber, Davis says.

PCO's Barnoski says his company is still looking for its place in this emerging scenario. "We're sorting out how to play it," he says. He sees the supplier lineup divided between "old boys" and upstarts.

Phone and cable companies are trying to 'string fiber now and fight it out later'

The old boys, he says, are the traditional telecommunications hardware houses, such as Fujitsu, GTE, Hitachi, and Siemens. Among the upstarts are newer firms such as Aster and PCO. The Japanese acknowledge particular interest in the last-mile market, says Barnoski, and he expects them to offer some very tough competition.

No matter how the last mile shakes out, companies like Aster and PCO with established fiber-equipment footholds stand to be winners. "We sit right smack in the catbird seat," says Davis. His couplers sell today for $100 each in moderate quantities, with two required per fiber link. The price tag will begin to drop soon, he says, and will eventually hit $25 or so.

The goal of $150 each for transceivers presents a tougher proposition, notes Barnoski. That's because transceivers "combine three technologies—semiconductor, electro-optical, and packaging."

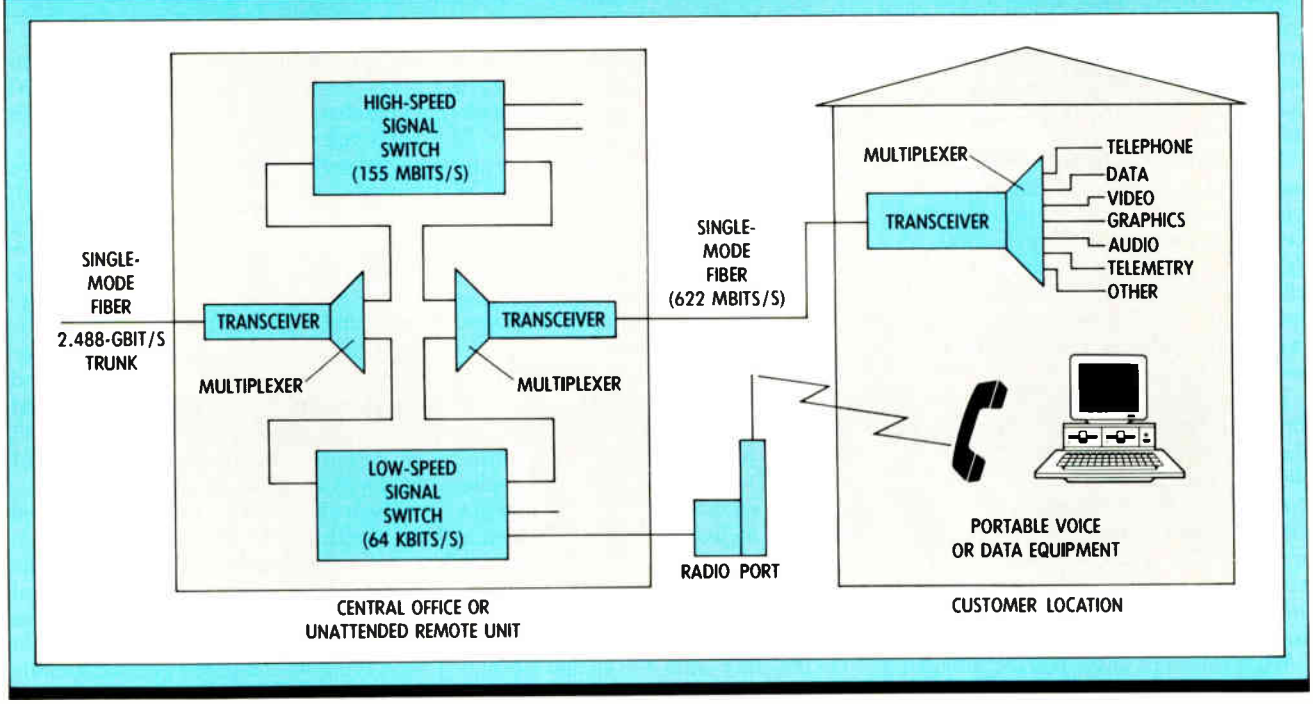
The unit itself consists of lasers, photo detectors, and couplers, along with enough glue circuitry to make them work. Typically, transceivers sell today for considerably more than $1,000 apiece. For example, Aster's transceivers, which use gallium arsenide transmitter/receiver pairs, carry a $1,200 price tag for the 1,550-nm wavelength. But Barnoski and Davis, along with most industry executives, foresee the prices dropping—and performance improving—as current experimental installations help to spell out requirements in more detail.

Just who will get ultimate responsibility for the last fiber mile remains to be settled, of course, but old hands such as Barnoski and Davis believe that experience provides a good road map. Already the phone companies are moving ahead faster—and the cable outfits are waking up to the threat.

"All are trying to string as much [fiber] as possible now, and then fight for it later," in Barnoski's view. When installations are done, the likelihood is for them to be grandfathered, or protected. Chances are, he says, that fiber optics will be down in American homes and working before all the legal issues have been settled.

Additional reporting by Lawrence Curran, Tobias Naegele, and Jack Shandle

BELLCORE MAPS OUT THE LAST MILE



One of many proposals for architectures with which to implement fiber-optic connections between telephone offices and subscribers is this one from Bellcore. Bellcore's role as a coordinator of the technology used by Bell companies may prove vital as architecture standards are set.

BREAKING THE DATA-RATE LOGJAM WITH ARRAYS OF SMALL DISK DRIVES

Parallel processing hits the disk-drive industry with the advent of disk arrays

It's a given that most computer systems run only as fast as their data-storage subsystems let them. But finding the best way to boost the performance of disk drives so that they measure up to the new breed of high-speed processors and memories is a sticky problem. Although magnetic-disk drives have zoomed ahead in density and capacity, they have been less successful in reducing average access times. Nor have they delivered order-of-magnitude increases in data-transfer rates. But that picture is about to change with the advent of disk arrays.

Just as system builders are using parallel-processor architectures to speed up computation, they are now looking at parallel architectures for disk subsystems to speed up data transfer. Large arrays of small, inexpensive disk drives are being designed that promise big gains in performance and reliability over big, expensive single drives. At the heart of this trend is the low-cost Winchester disk-drive technology. Originally developed for personal computers, it is being put to effective use in larger systems—all the way up to supercomputers.

Disk-array technology could have a huge impact on the computer industry by changing the way it builds large mass-storage subsystems. The major bonus is fast access to data, which is particularly important in two quite different application areas: supercomputing and data-base transaction-processing systems. Disk arrays can be optimized for either, or even for both. On the down side, designers are still wrestling with the disk-array scheme's single major drawback: the overall mean time before failure drops dramatically as many drives are strung together. To counteract the compounding of potential failures of many small drives, various forms of redundancy, error checking, and correction must be devised.

Despite this stumbling block, the march toward disk arrays is quickening. System builders are asking their suppliers—notably peripheral-controller vendors—about the arrays, and a number of big companies are said to be designing their own disk arrays. Commercially, several disk-array products are available or under development by peripheral-subsystem companies, computer makers, and disk-drive-controller vendors.

Driving this movement is overall computer technology, where speed is rising at an unprecedented rate. Main memories are keeping up with the growth in processor speed, but only with the help of cache architectures and the static random-access-memory technology with which to build the caches. But computers are not just processors and main memory. Secondary storage, commonly called mass storage, which is necessary for supplying data to main memory, is important to overall system performance. But here lies a bottleneck. "Mass-storage technology is falling behind in throughput," says Ernest E. Godsey, product marketing manager at Interphase Corp., the Dallas-based peripheral-controller company.

Magnetic-disk technology has been approximately doubled in capacity and halved in price about every three years over the past decade. But however important that added capacity is in matching the greatly increased capacity of main memories, capacity alone is not enough. The speed with which instructions and data are delivered to processors also contributes significantly to determining a computer's overall performance.

SEEK PROBLEM. In this regard, the large and expensive disk drives built for mainframes and superminicomputers have improved in performance only modestly. The raw seek time for magnetic heads—the time it takes to position a read/write head from one track address to another location—has fallen no more than a factor of two in many years, and the big drives' rotation speeds have not changed.

Indeed, the mechanical limitations of rotating disks and head-positioning devices virtually preclude any dramatic breakthroughs. This points to a pending mass-storage performance crisis, and also explains why the disk-array solution holds so much promise.

After all, the reasoning goes, computers with awesome computation capability have been successfully built using clusters of inexpensive microprocessors. In fact, parallel-processing computers can outrun most of the big single-processor machines and do it at a much lower cost. And for quite some time now, very large main memories have been built by stringing together lots of inexpensive high-capacity memory chips. So why not apply the same idea to disk drives, now that inexpensive 5.25-in. and 3.5-in. drives of very respectable capacity and performance are available?

The cost of storage on 3.5-in. drives is dropping faster than the cost per megabyte of the big drives. And clearly, the technology is ready. For example, some of the small drives are approaching gigabytes of capacity, while many drives with several hundred megabytes of storage are already available. In addition, the number of input/output operations per head that the small drives can perform has risen to almost half that of the big, expensive drives.

If disk arrays successfully live up to their potential, they could change the face of the mass-storage industry by pushing the big disk drives out of the market. Rather than waiting for the mak-

AN ARRAY OF DISKS BEATS A SINGLE DISK

	One Large Disk	100 Small Disks	Multiple vs. Single
Capacity (Gbytes)	7.5	10	1.33
Data rate (Mbytes/s)	12	100	8.33
I/O rate (I/Os/s)	200	3,000	15
Power (kW)	7	1	7
Cost ($)	100,000	100,000	—
Cost per Mbyte	13.33	10	1.33
Reliability (mean time to failure h)	30,000	820,000	27.33
Volume (ft^3)	24	10	2.4

SOURCE: UNIVERSITY OF CALIFORNIA AT BERKELEY

ers of big disk drives to solve their significant technical challenges, subsystem designers could instead produce very high-capacity arrays with much faster access to data than the big drives, with the added bonus of lower cost per megabyte. The other very important parameter is reliability. Arrays will have to be at least as reliable as big single drives.

One event that galvanized the computer industry into taking disk-array technology seriously was a landmark paper titled "A Case for Redundant Arrays of Inexpensive Disks (RAID)." Authors David A. Paterson, Garth Gibson, and Randy H. Katz of the Computer Science Division of the University of California at Berkeley compare the high-performance IBM Corp. 3380 model AK4 14-in. mainframe disk drive with an array of Conner Peripherals CP3100 3.5-in. drives.

The paper points out that an array of 100 Conner drives would have 15 times the I/O rate, more than 8 times the data rate, and 1.3 times the capacity of the 3380, with lower power consumption at the same cost. The bad news is reliability—or the lack thereof. Magnetic-disk drives are unreliable enough to cause system managers to back up the information on them nightly in major computer installations. (PC users should do it too, but more often than not they don't.) Indeed, the Berkeley team comes to the conclusion that "without fault-tolerance, large arrays of inexpensive disks are too unreliable to be useful."

The more drives in the array, the lower the reliability, the Berkeley paper says. "What would be the impact on reliability of having 100 disks?" it asks. "Assuming a constant failure rate—that is, an exponentially distributed time to failure—and that failures are independent, the reliability of an array is the reliability of a single disk divided by the number of disks in the array." Using the rated mean time to failure of the 3380 and the Conner drive of 30,000 hours (greater than three years), this formula yields an MTTF for an array of 100 Connor drives of 30,000 divided by 100—300 hours, or less than two weeks. If one were to build an array of 1,000 such small disks, the MTTF drops to 30 hours, just over one day. A disk system that failed about once a day would be totally unacceptable.

FAILURE RECOVERY. To overcome their inherent unreliability, disk arrays must have failure-recovery mechanisms. Designers are exploring a number of solutions, including sophisticated error-detection and correction schemes, and extra disks containing redundant information from which to recover the original data.

Besides grappling with reliability problems, disk-array designers must take into account the two types of fast data access required for two major computer-system applications today. Supercomputer and other computation-intensive applications demand fast transfers of very large blocks of data, though not a high number of transfers in a given time. In contrast, high-volume transaction-processing systems require a fast data rate that supports the transfer of a very large number of short data blocks.

The Berkeley researchers describe a five-level specification of redundant arrays of inexpensive disks, naming them RAID 1 through RAID 5. These five different architectures vary in performance and cost as well as in suitability for the two types of applications. Some are better for transaction processing and others for supercomputer applications. At least one architecture, RAID 5, is good for both, according to Paterson and his Berkeley colleagues.

Without fault tolerance, large disk arrays are too unreliable to be useful

For supercomputers, where the number of reads and writes per second for large blocks of data is the important metric, all the disks in an array should act as a single unit, each reading or writing a portion of the data block in parallel. The parallel drives can even be synchronized—that is, the heads on each drive are simultaneously positioned over the same track and sector, for efficient parallel operation.

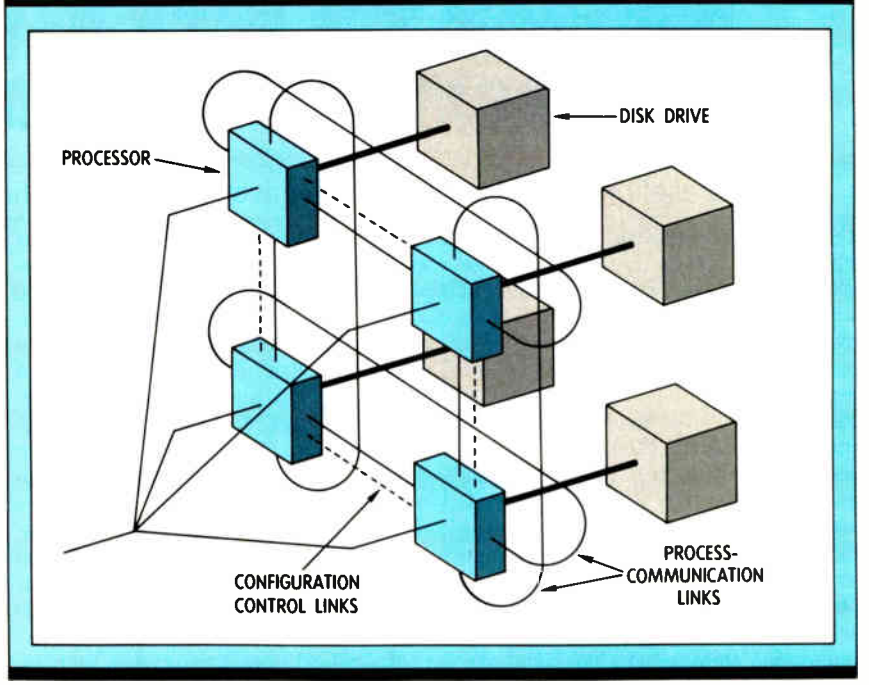
On the other hand, for data-base transaction processing, the speed of a read-modify-write sequence of operations is critical to overall performance. A disk array for transaction processing would handle a small block of read-modify-writes quickly and be optimized to do many of these small blocks independently in a second. In this kind of array, each disk acts independently, doing a data transfer whenever one is assigned to it.

TAKE YOUR TIME. The complexity of devising a suitable array architecture for both large-block and small-block transfers is one reason why there are not many array products on the market yet. Designing, building, and testing a reliable and properly fault-tolerant disk array is no trivial task. "A formidable array is not a short project; you just don't crank out a RAID 5 array quickly," says Mike Gamerl, the disk-marketing product-line manager at Fujitsu America Inc., San Jose, Calif., one of the disk-drive companies working on an array product.

Of the five RAID architectures outlined by the Berkeley researchers, the first level, called RAID 1, or mirrored disks, has been in use for some time in fault-tolerant systems. It is mainly an attempt to improve the reliability of magnetic disks rather than speed up data transfer. Mirrored disks are a requirement for the most critical fault-tolerant transaction-processing systems.

Mirrored disks are also the most expensive type of disk array, since in this architecture every disk is duplicated by a check disk—each write goes to two disks.

SETTING UP A DISK ARRAY



A built-in disk array is part of the SuperSet.64 parallel supercomputer built by Computer System Architects, in which drives are embedded within an array of processors.

Tandem Computers Inc., Cupertino, Calif., has a version of mirrored disks that doubles the number of controllers, which helps speed up the disk reads by doing them in parallel.

Mirrored disks are extremely reliable, especially if only two big drives are used. The MTTF of such subsystems is several hundred years, greatly exceeding the useful product lifetime. But the overhead cost is 100%, since the user is buying twice as much storage capacity as he needs and, in some cases, twice the number of controllers.

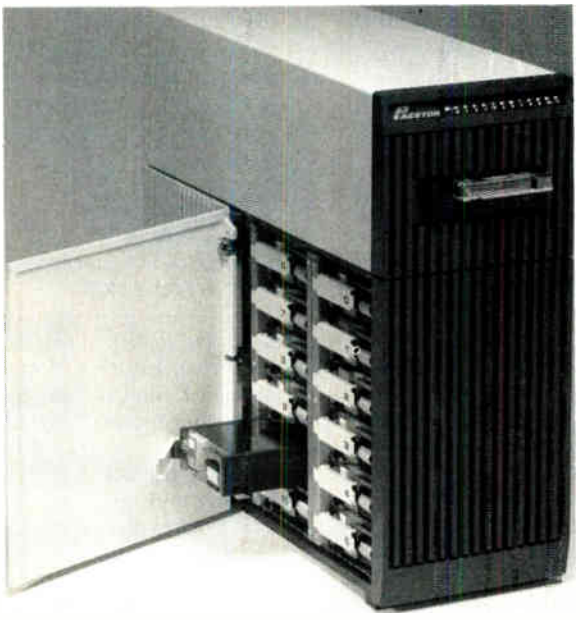
The second level of disk arrays, using a Hamming code for error correction, gets by with much less redundancy than mirrored disks. The idea is to have enough check disks to store the error-detecting and correcting codes to find and fix a single error.

According to the Berkeley researchers, a single parity drive can detect a single error on the data drives, "but to correct an error, we need enough check disks to identify the disk with the error." For example, an array of 10 data disks would require another four as check disks. This 40% overhead is much less costly than the 100% for mirrored disks.

For large-block transfers, a level 2 disk array with two drives has the same performance as level 1 mirrored disks, but lower overhead. The MTTF of a 10-disk system is an acceptable 50 years. For supercomputer applications, then, an array of 10 small drives is better than mirrored large disks, since the 10 drives running in parallel provide a data-transfer rate 10 times faster than that of a single drive. But this architecture offers dismal performance for the small, fast data transfers of transaction-processing systems, because all the disks must be accessed for each small transfer.

ONE CHECK DISK. The third RAID level reduces overhead even further by using just a single check disk. This scheme can work because the other check disks are not needed to identify the disk that has an error, since most disk controllers can identify a drive failure. The check disk detects a data error and the controller pinpoints the drive containing the error. In an array of 10 data drives, the redundancy overhead is reduced to only 10%. The performance of level 3 arrays is the same as for level 2. And reliability is a little higher, since fewer total drives are in use. Thus level 3 brings the cost of reliability redundancy to its lowest point.

The next two disk-array levels, 4 and 5, address the problem of improving performance for large numbers of small-block accesses for transaction processing. In levels 2 and 3, bit interleaving across the array is used for easy calculation of the Hamming code for error detection and correction. However, bit interleaving causes small transfers to access all drives. In the level 4 scheme, individual transfers are kept to one sector of a single disk. Errors are then detected by the controller on an individual read without accessing any other disk. As a result, reads can be independent, and they can operate at the disk's maximum rate while still detecting errors.



The Pacstor Integra III fault-tolerant disk-array subsystem uses up to a dozen 100-Mbyte 3.5-in. disk drives.

The main difference between level 4 and the preceding two levels is that data is interleaved on a sector level rather than on a bit level. At level 4, read access for small blocks is improved dramatically. However, writes must still access all disks to generate new parity information, and the read-modify-write sequence still suffers from low performance. So level 4 is still not a good choice for transaction-processing systems.

Level 5 comes to the rescue. At all the other levels, the check disk is the bottleneck inhibiting performance for small-block writes. This final level of disk-array architecture eliminates the separate check disk by spreading the parity bits over all the disks in the array.

Small writes have a little impact on performance, because this scheme makes multiple individual writes possible. As a result, level 5 offers the best solution for both transaction processing and computation-intensive applications. While keeping the performance high for large-block transfers, keeping the redundancy overhead low, and speeding up small-block reads, level 5 appears to be the way to build disk arrays.

Of the several commercial disk-array products now on the market, none yet use the level 5 approach. However, Fujitsu America has such an array design in the works. Due out early next year, "it will be able to accommodate any of the five levels and be able to serve both the high-bandwidth [supercomputer] and the on-line transaction-processing markets," says Gamerl of Fujitsu. But it will take time to do a proper level 5 product, he says.

Toshiba America Inc. of Irvine, Calif., is another vendor that is keeping an eye on developments. "Disk arrays are a logical step for users who are looking for higher transfer rates and are increasingly interested in obtaining very long times before failure—over five years," says Dave Tovey, director of marketing. While admitting that arrays are the way of the future, Tovey points out some problems.

If suppliers of original-equipment manufacturers package multiple drives and controllers in a box and offer completed array subsystems, will they be taking away the added value that their customers want to put in? "Such customers may want to buy an array-friendly drive and do it [the array subsystem] themselves," says Tovey. On the other hand, Tovey points out, since building a disk array is not an easy task, it makes sense for a disk-drive company to do it. Yet, he asks, "can one design suit all customers?" No one in the industry knows the answer. "It will take a year or two before it is clear how disk-drive vendors should proceed with arrays," Tovey says.

Although no level 5 disk arrays are available, products using the array concept have been built. Besides the disk mirroring (level 1) used in many fault-tolerant systems, some vendors are tinkering with higher RAID levels. For example, a design under development by System Industries, Milpitas, Calif., will use concepts of the higher RAID levels, and several now-available disk-array systems follow the principles of levels 2 to 4.

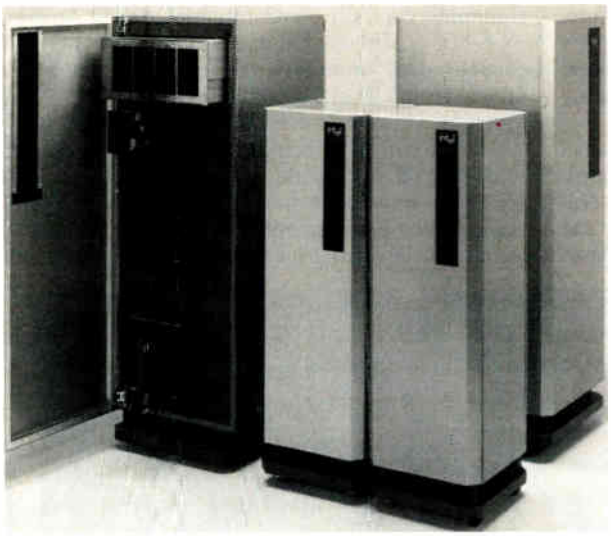
One example is from Plus Development Corp., which recently annnounced the Plus Impulse disk server for PC networks using up to 32 disk drives. The Milpitas company's hard-disk server achieves a 12-ms effective access time and total capacity up to 2.6 Gbytes.

Another new product is the Integra III fault-tolerant storage-array subsystem from Pacstor Inc. of Los Gatos, Calif. This array uses up to 12 high-speed, 100-Mbyte, 3.5-in. drives. Error-correction code is distributed across all drives, as in level 5. As many as two drives can fail without any loss of data, and failed drives can be replaced and data regenerated on the replacement drives without interrupting operation.

Disk arrays like the Integra III are de-

signed to be servers for multiple-user and multiple-host transaction systems, where the highest level of data integrity and availability is required. On the other side of the market, supercomputer companies are starting to get into the act. Three of them—Computer System Architects, Intel Scientific Computers, and Thinking Machines—have built their own disk arrays.

The array developed by Thinking Machines Inc. in Cambridge, Mass., for the massively parallel Connection Machine supercomputer is called the DataVault and offers 10 Gbytes of storage. The DataVault is a level 2 RAID system with 32 drives for data and 8 check drives, including one hot standby. Up to eight DataVaults may be used in parallel on the Connection Machine Model CM-2. This scheme yields 80 Gbytes of total capacity and a transfer rate of more than 150 Mbytes/s.



An integrated supercomputer disk array uses high-capacity drives to give Intel's iPSC/2 a concurrent I/O subsystem.

The Scientific Computer division of Intel Corp. in Beaverton, Ore., recently announced the Concurrent I/O subsystem for its iPSC/2 concurrent supercomputer [*Electronics*, November 1988, p. 24]. This array of up to 127 I/O nodes can support disk drives and other I/O devices at a total data bandwidth of more than 700 Mbytes/s. Each I/O node typically controls two 700-Mbyte disk drives. The architecture of the Concurrent I/O subsystem has the potential to support disk arrays of hundreds of disks with up to 500 Gbytes of total capacity. The first version handles a disk configuration of up to 40 Gbytes using 344- and 574-Mbyte drives.

Intel provides software, called the Concurrent File System, that makes the parallelism of the array transparent to programs and programmers. Each I/O node sees a single large virtual disk.

FOR PARALLEL COMPUTATION. The architecture of the new SuperSet.64 supercomputer from Computer System Architects in Provo, Utah, includes a switching system that allows drives to be embedded within the array of processors the machine is built around. Each processor node can have a disk drive or some data-acquisition equipment attached to it in a setup much like Intel's [*Electronics*, December 1988, p. 112].

Teradata Corp., the Los Angeles maker of data-base computers, pioneered parallel-processor-hardware architecture for data-base management that makes use of arrays of disk drives.

To build disk arrays, the drives themselves need not be changed. The changes come in controllers, interface architecture, error detection and correction, and access software. For example, Maximum Strategy Inc. makes a controller designed just for disk arrays, while other controller companies, such as Ciprico, Interphase, Storage Concepts, and Xylogics are looking closely at the array concept for future development.

The Maximum Strategy array controller is designed for controlling multiple banks of standard disk drives in arrays of up to 40. The Strategy 2 controller offered by the San Jose, Calif., company can be used for disk subsystems of up to 32 Mbytes with sustained data-transfer rates up to 20 Mbytes/s and burst rates up to 40 Mbytes/s. A variety of Enhanced Small Disk Interface and Storage Module drives can be selected. Maximum Strategy uses a 48-bit error-correction polynomial, which is stored with every 1,024 bytes of data to provide error recovery. Parity drives, standby drives, and dual ports help achieve a high level of fault-tolerant data integrity.

> The first flood of arrays will likely be done in house by systems and computer firms

For ease of use with a variety of computer systems, Maximum Strategy has engineered a device-independent, logical-block host-command interface for its array products. This enables the host programs to communicate with the controller (and hence the array subsystem) in terms of logical blocks rather than physical disk parameters, such as cylinders, tracks, and sectors. Thus it eliminates the need for applications to handle logical-to-physical-block mapping, bad block management, and data-error recovery. These are handled by the controller, making details of the array invisible to the programs.

Although other peripheral-controller vendors report a great deal of customer interest in arrays, the major players—such as Ciprico, Interphase, and Xylogics—have not yet revealed any product plans. However, they do offer some tantalizing hints. "Arrays are a legitimate scheme for assembling high-performance disk systems," says Interphase's Godsey. And in the next breath: "Interphase is committed to supplying high-performance disk controllers to the industry."

Meanwhile, at Xylogics Inc. in Burlington, Mass., "we find that people are interested in the concept [of disk arrays] and are using disk striping now to get data rates up," says Chappell Cory III, senior vice president of marketing operations. Disk striping means spreading data across multiple drives. "That's why Xylogics did a dual-channel controller"—a recently announced product. "A wide array [more than two channels] can do even higher data rates," he adds.

Although a dual-channel controller can help a lot to speed up data rates, arrays can take the process much further. It seems safe to assume that controllers designed specifically for building large arrays of disks will be forthcoming. Yet, Cory cautions, "we have a way to go before we see lots of arrays, at least in the OEM environment."

Another cautionary note is offered by Interphase's Godsey. "It's not a given that real RAID systems always provide lower cost per megabyte. For example, you can get very poor formatting efficiency with arrays, especially with small block sizes," he says. Ciprico Inc. in Plymouth, Minn., is another of the leading peripheral-controller companies that is mulling disk arrays. "We believe that parallel arrays will be a technology that will be useful, and there will be a market for them in the future," says Don Peterson, director of marketing.

Most industry watchers, Godsey and Cory included, believe that the first flood of disk arrays are likely to be those assembled by big system houses and computer companies for their own use rather than as products offered to the general OEM market.

Many OEMs will design their own array controllers, but some may purchase them. This could lead to problems of deciding who is responsible for the array subsystem. With controller firms building disk-drive subsystems using their array controllers, or disk-drive companies building array controllers to package with their drives, customers may see a lot of finger pointing. That's a good reason for system houses to buy drives from a drive maker, controllers from a controller maker, and integrate their own subsystems. *–Tom Manuel*

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OARD
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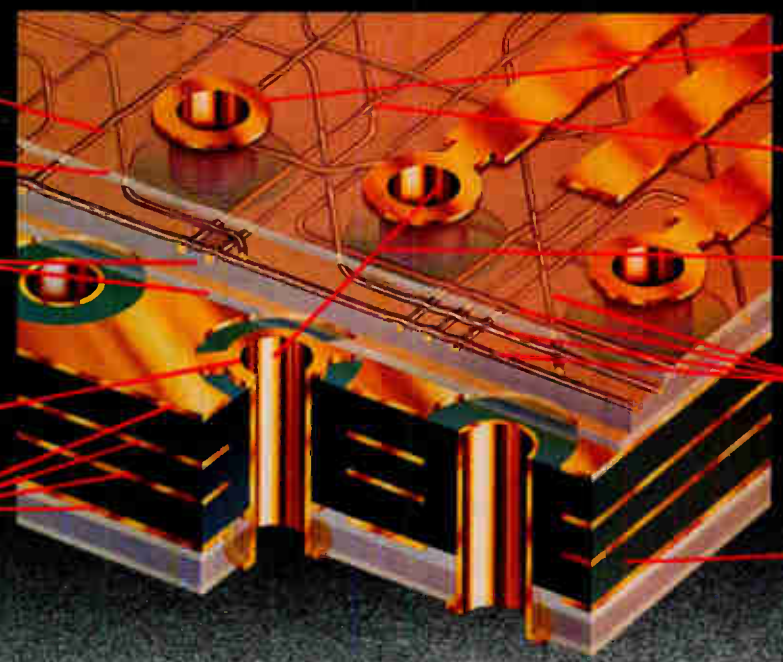

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For example, if you need a monolithic high speed, ECL-compatible converter, there's our AD770 or AD9002.

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The AD9002 has a guaranteed sample rate of 125MSPS – yet its nominal power dissipation is a mere 750mW – and it operates from a single −5.2V power supply. The AD9002 is also available with MIL-STD-883 processing, making it ideal for a wide range of applications.

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The AD9012 is the industry's fastest TTL-compatible converter, with a guaranteed sampling rate nearly twice that of its

ANALOG DEVICES

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AD770

High Bandwidth,
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- **400MHz Small-Signal Bandwidth**
- **19pF Input Capacitance**
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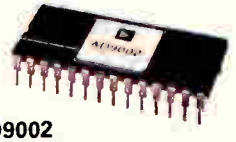
All inputs and outputs are ECL compatible, and analog inputs can be either bipolar or unipolar signals with up to 4V range. High accuracy and minimum temperature drift are preserved with end point reference Force and Sense connections.

There are three grades available. JD and KD grades are specified over a 0 to +70°C range; the SD grade is specified for temperatures from −55°C to +125°C. All standard grades are packaged in 40-pin ceramic DIPs; contact the factory for other package options.



AD9002

Low Power,
ECL Compatible, 125MSPS

- **160MHz Analog Input Bandwidth**
- **17pF Input Capacitance**
- **750mW Power Dissipation**
- **Single −5.2V Power Supply**

Designs for radar, digital oscilloscopes, ATE systems, electronic warfare, communications/signal intelligence systems and a wide variety of other applications can be made easier with the AD9002 High Speed Monolithic A/D Converter.

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Input capacitance is typically 17pF and only 22pF maximum, simplifying the choice of a driving amplifier. Cooling requirements and power supply problems are also eased because of the low 750mW dissipation of the AD9002.

Two grades are available; one has 0.5LSB linearity, and the other has 0.75LSB linearity. Both versions are offered for operation from −25°C to +85°C packaged as 28-pin DIPs or 28-pin PLCCs. Military temperature range devices of −55°C to +125°C are available as ceramic DIP and LCC packages; they are compliant to MIL-STD-883 requirements.

FOR THE WHOLE STORY
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nearest competitor. Plus the AD9012 offers excellent ac performance, low power operation and low input capacitance.

The AD9048 is an improved version of an industry-standard 8-bit TTL- compatible A/D converter, with the highest sampling rate, widest bandwidth, lowest input capacitance and lowest power. And the AD9048, as well as the AD9012, is available to MIL-STD-883.

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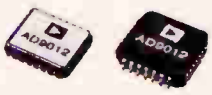


AD9012
Low Power, Wide Bandwidth, TTL Compatible, 75MSPS
- 160MHz Input Bandwidth
- 16pF Typical Input Capacitance
- Power Dissipation<1W
- Minimum 46dB SNR

The AD9012 is a TTL compatible A/D converter fabricated in an advanced bipolar process which makes it possible to operate at typical conversion speeds up to 100MSPS.

For commercial and industrial applications, the AD9012 is an excellent choice for professional video, instrumentation, digital radio and PC-based video digitizing equipment.

In military applications, the requirement for mil-qualified devices can be met with MIL-STD-883 units in electronic countermeasures, missile guidance, radar, radar warning and other military systems equipment.

The AD9012 is available in two grades: one has 0.5LSB linearity, and the other has 0.75LSB linearity. Both operate from −25°C to +85°C and are packaged as 28-pin DIPs or 28-pin PLCCs. Military temperature range devices of −55°C to +125°C are available as ceramic DIP and LCC packages.

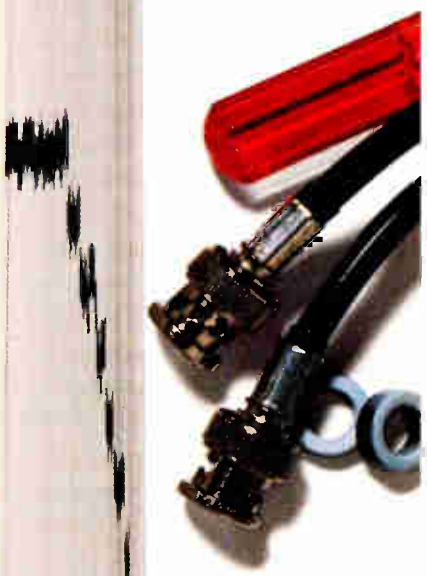
AD9048
Low Power, Low Cost, TTL Compatible, 35MSPS
- 15MHz Typical Bandwidth
- Input Capacitance Typically 16pF
- 550mW Power Dissipation
- Industry-Standard Pinouts

As its name implies, the monolithic AD9048 Video A/D Converter is an ideal choice for real-time conversion of video signals.

Its full power bandwidth is typically 15MHz, with no missing codes, and is a guaranteed minimum of 10MHz.

Low power dissipation of 550mW typical makes the AD9048 adaptable and attractive for a broad range of applications. In addition to professional video systems and video imaging, it is an excellent choice for electro-optics, digital radio and electronic warfare systems, among others.

The AD9048 has industry-standard pinouts and is available over two temperature ranges, with two grades of linearity. Linearities of either 0.5LSB or 0.75LSB can be ordered for 0 to +70°C commercial ranges, or −55°C to +125°C military temperatures. Commercial versions are in 28-pin DIPs and PLCCs; military versions are in ceramic DIP and LCC packages. Both commercial units and MIL-STD-883-compliant devices are standard products.



ON FLASH CONVERTERS
ED READING.

Circle 103

COMING SOON: HIGH-PERFORMANCE SON OF SCSI

It looks as if the high-performance successor to the popular Small Computer Systems Interface bus standard is finally about to emerge—after seven draft revisions and nearly two and a half years of committee wrangling. Backers of the new SCSI-2 standard are hoping for big things, and already a few original-equipment manufacturers are jumping out with early SCSI-2 products.

Ciprico Inc. in Plymouth, Minn., for example, is introducing the industry's first SCSI-2 host bus adapter for the VMEbus this month. Cipher, Laser Magnetic Storage, and Wangtek have already introduced tape drives with embedded controllers that offer SCSI-2 features. Other vendors are expected to enter the fray this year, as SCSI-2 winds its way through the American National Standards Institute approval process.

In its most elaborate form, SCSI-2 will eventually allow synchronous data-transfer rates of up to 40 Mbytes/s. That will put it in the same performance league as the Intelligent Peripheral Interface, and some think it could give IPI a run for its money by the early 1990s in high-end disk- and tape-drive applications, despite SCSI's small-system orientation.

Others have their doubts about that. And some think market acceptance could be slowed by confusion over just what SCSI-2 is, since the voluminous SCSI-2 document allows for a multitude of vendor options (see below).

Whatever its impact, SCSI-2 should help fuel an already fast-growing market in SCSI-based gear. Sales of SCSI integrated circuits, boards, and embedded SCSI disk drives and tape transports together accounted for over $1 billion in OEM revenues last year, according to Technology Forums Ltd., a Chanhassen, Minn., technical publishing firm. The firm sees the SCSI and SCSI-2 market growing 36% in 1989 to $1.45 billion.

SCSI-2 is designed for backward compatibility with SCSI—both SCSI and SCSI-2 devices can coexist on the same bus. That should provide an easy migration path for SCSI users, allowing SCSI-2 to be added incrementally. But when making SCSI-2 purchasing decisions, OEM managers will want to make sure they know exactly what they're buying, since one vendor's products won't necessarily match those of another.

> SCSI-2 could give IPI a run for its money in high-end disk-drive applications

The SCSI-2 document is a phone-book-size treatise encompassing nearly 600 pages. "People keep talking about a SCSI-2 standard. But what it is, is a standard laundry list," says Joe Molina, president of Technology Forums. And because of the standard's all-encompassing nature, initial SCSI-2 products will implement only a subset of the standard.

Cipher's ST150S2 half-height 5.25-in. tape drive, for example, adopts the SCSI-2 Common Command Set but doesn't make use of SCSI-2 options for boosting bus data-transfer rates. Ciprico's Rimfire 3550 VMEbus SCSI-2 host bus adapter, on the other hand, will incorporate the so-called "wide SCSI" option of SCSI-2. By using a second cable to extend the width of the 8-bit SCSI bus to either 16 or 32 bits, wide SCSI can transfer data at up 20 Mbytes/s—four times the rate of today's 4-to-5-Mbyte/s SCSI maximum.

FAST AND WIDE. SCSI-2 will get to its ultimate 40-Mbyte/s speed by doubling the SCSI bus clock rate, using the so-called "fast SCSI" option. But fast SCSI, unlike wide SCSI, will require new controller chips, which probably won't be available even in sample form until around mid-year or later. That means OEM products that combine the fast SCSI option with wide SCSI are unlikely to show up in volume until next year at the earliest.

Even before the SCSI-2 standard is set in stone, work on a successor SCSI-3 standard is already under way. And one industry watcher who is high on the long-term outlook for SCSI is Molina of Technology Forums, which publishes product source guides for SCSI, IPI, and other buses. "It's possible, though not entirely probable, that SCSI-2 and SCSI-3 will totally throw out IPI," Molina says. There are currently over 200 suppliers of SCSI components and equipment, compared with only about a half dozen IPI vendors, he points out. "And there's a school of thought that says if the SCSI people had taken IPI more seriously a few years ago, there wouldn't be an IPI now."

Others disagree. Unlike SCSI-2, the IPI standard was completed in 1985, they point out, and IPI is already used in computer systems sold by heavyweights like

SOUPED-UP STANDARD BOASTS HIGHER THROUGHPUT

The Small Computer System Interface was already a de facto standard when it was formally approved in June 1986. And SCSI today is one of the most widely known and widely used bus standards. It is commonplace in low- to medium-performance magnetic-disk environments and is also used for connecting tapes and optical-disk peripherals.

In developing the successor SCSI-2 standard, the American National Standards Institute's X3T9.2 committee has taken pains to maintain backward compatibility with SCSI. Both SCSI and SCSI-2 devices can coexist in the same bus. But SCSI-2 has a lot more going for it.

SCSI-2 addresses numerous software issues aimed at better plug-and-play compatibility and higher throughput. Also, it contains two hardware options (wide SCSI and fast SCSI) for boosting bus data-transfer rates beyond today's 4-to-5-Mbyte/s range. It contains a number of distinguishing features:

- The Common Command Set developed in 1985 by an industry group for use with SCSI disk drives is given a formal stamp of approval under SCSI-2. CCS has been further defined and extended for use with tape transports and optical drives. And SCSI-2 defines command sets for other peripherals, including compact-disk read-only memories, scanners, medium changers, and communication devices.
- Command queuing is supported. Whereas SCSI allows only one command to be outstanding to each logical unit on a bus, an SCSI-2 host can send up to 256 "tagged" commands to any SCSI-2 peripheral. These are assigned a tag value so they can be intelligently manipulated and queued at the target peripheral to improve execution sequences. This can minimize seek times and mechanical latencies for improved throughput.
- The wide SCSI option extends the 8-bit SCSI bus to either 16 or 32 bits, providing maximum synchronous data-transfer rates of 10 and 20 Mbytes/s, respectively. Wide SCSI maintains compatibility with SCSI through the use of a second cable, which requires a 68-pin connector and carries the control signals and data for the extra 8 or 24 lines.
- The fast SCSI option relies on better cabling and tighter tolerances to double today's SCSI clock rates to 10 MHz. Fast SCSI can be used with an 8-bit-wide bus to provide 10-Mbyte/s synchronous data-transfer rates. When combined with either 16-bit- or 32-bit-wide SCSI, fast SCSI pushes SCSI-2 performance to a maximum 40 Mbytes/s. *–W. R. I.*

Fujitsu, Hitachi, Siemens, and Tandem. And that's not to mention IBM Corp., which uses IPI drives on its 9370 mid-range systems and other equipment [*Electronics*, September 1988, p. 40].

Also, SCSI's short cable lengths (a maximum of 25 meters in voltage-differential mode or 6 meters in single-ended mode) will prevent SCSI-2 from competing in the market for very large computer systems, says Dal Allan, president of ENDL Consulting of Saratoga, Calif., and also vice chairman of the ANSI X3T9.2 task force charged with SCSI-2 development. "You can't hook up 160 disk drives to a large IBM mainframe in that kind of space," he points out.

There are also questions of cost. "The SCSI market is still a Kentucky Fried Chicken world. The perception of SCSI is that it's cheap, cheap, cheap," says Allan. And SCSI-2 will add cost as well as take up more board real estate, due to fast SCSI's need for expensive outboard differential transceivers and wide SCSI's need for a second cable.

HOT AND COLD. So far, OEM vendors are embracing SCSI-2 to varying degrees. At Ciprico, managers are so high on SCSI-2's long-term outlook that the firm has put IPI product plans on the back burner. Others are less enthusiastic, at least for the near term. "We don't see anybody today who is particularly interested in SCSI-2. We're getting a huge 'ho hum' in the marketplace. The guys doing the high-performance I/O systems today are interested in IPI," declares Ernest E. Godsey, product marketing director at Interphase Corp. The Dallas firm, a Ciprico competitor, currently has three SCSI controller products on the market. "Yes, we believe SCSI is going to play a large role in peripheral interfaces. But do we think that translates into SCSI-2 being an immediate success? The answer is no," Godsey says.

And there are those in the middle. "We're hearing preferences from some customers to use SCSI," says Chappell Cory III, vice president for marketing operations at Xylogics Inc., Burlington, Mass., another open-bus-controller supplier. "But other people don't want it. And I've found the market is composed of both types."

One key to getting SCSI-2 on track is the standards-approval process. Barring further revisions, the X3T9.2 group is expected to forward the SCSI-2 document to the parent X3T9 committee this month for a letter ballot and public review. Chip makers including Emulex, National Semiconductor, NCR, Scientific Micro Systems, Western Digital, and others are already working on SCSI-2 controller chips. If the SCSI-2 approval process goes as expected, the betting among observers is that the first dedicated SCSI-2 controller chips could be arriving in sample form by around midyear. *–Wesley R. Iversen*

FIRST OUT: CIPRICO'S SCSI-2 RIMFIRE ADAPTER

One company that is betting heavily on SCSI-2 is Ciprico Inc. The Plymouth, Minn.-based firm this month is rolling out the industry's first SCSI-2 host adapter for the VMEbus. Ciprico's Rimfire 3550 VMEbus SCSI-2 host bus adapter supports the SCSI-2 common command set and the tagged-command techniques to allow command queuing at the target peripheral for improved throughput. The 3550 also raises bus data-transfer rates by adopting the SCSI-2 wide option.

"In our implementation, SCSI-2 means we're going from an 8-bit-wide data path to 16 or 32 bits wide," says Donald C. Peterson, Ciprico's director of marketing. That means the Rimfire 3550 is able to handle SCSI-2 data-transfer rates of up to 8 Mbytes/s in an asynchronous mode and up to 20 Mbytes/s in a synchronous mode, compared with today's 4-to-5-Mbyte/s synchronous SCSI rates.

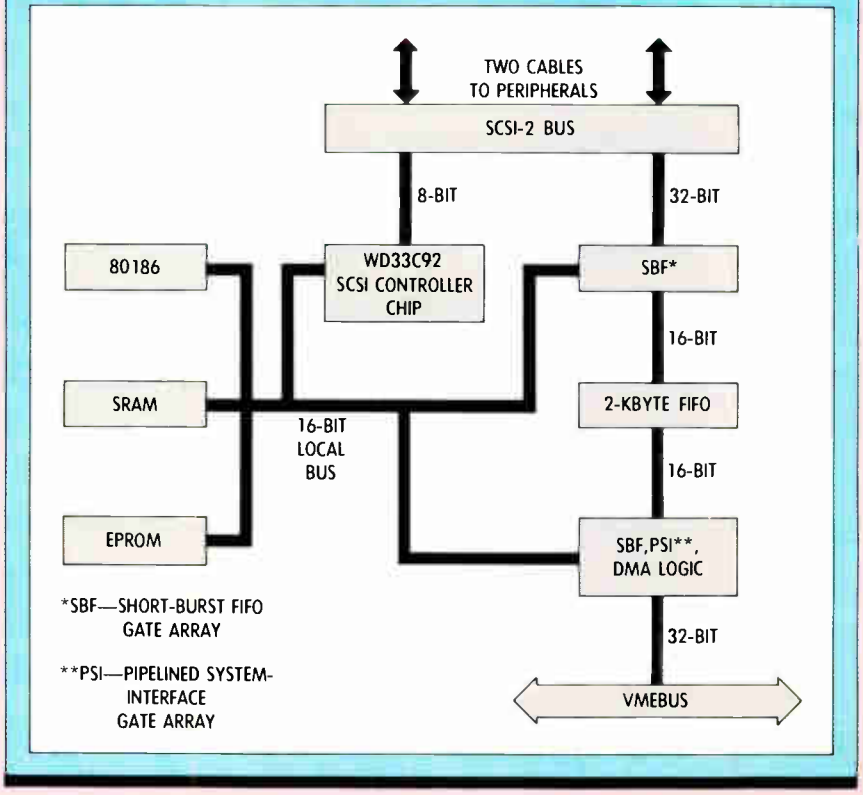
The Rimfire 3550 is equipped with faceplate connectors for both the 8-bit-wide A cable (the same as standard SCSI) and the B cable required for the extra data and control lines used in wide SCSI. Since dedicated SCSI-2 controller chips are not yet available, the 3550 relies on the same Western Digital WD33C92 SCSI controller circuit used in Ciprico's earlier Rimfire 3510 VMEbus SCSI host bus adapter. And as with the 3510, the WD33C92 works with an on-board 80186 chip to handle SCSI protocols.

Ciprico builds additional circuitry into the 3550 to handle the wider SCSI-2 data path. This includes a 2-Kbyte first-in, first-out circuit that acts as a buffer for handling high SCSI-2 data rates and for more efficient coupling to the VMEbus. Ciprico has also put in two proprietary 32-byte short-burst FIFO circuits that are able to transfer at 20 Mbytes/s.

Input/output on each side of the short-burst FIFOs is programmable for making the conversion between variable-width SCSI or SCSI-2 data and the 32-bit-wide format used on the VMEbus. The 3550's 80186 uses firmware housed in erasable programmable read-only memory for negotiating with SCSI target devices on whether 8-, 16-, or 32-bit bus transfers will be used, and programs the short-burst FIFOs accordingly. Data for both the A cable and B cable is routed through the FIFOs over a 16-bit local bus on the 3550, under WD33C92 control.

Evaluation units of the Rimfire 3550 are due in March and production quantities should appear in June. In single-unit quantities, the 3550 will sell for $1,495 for a version with single-ended transceivers. A unit equipped with differential transceivers will be priced to sell at approximately $1,895. *– W. R. I.*

CONNECTING TO SCSI-2



Q: Which workstation has full I/C layout and editing capabilities?

▲ 4 billion x 4 billion point database;

▲ Power:

fast, crisp graphics; intuitive and flexible data entry; GDSII and/or Gerber compatibility.

▲ Productivity:

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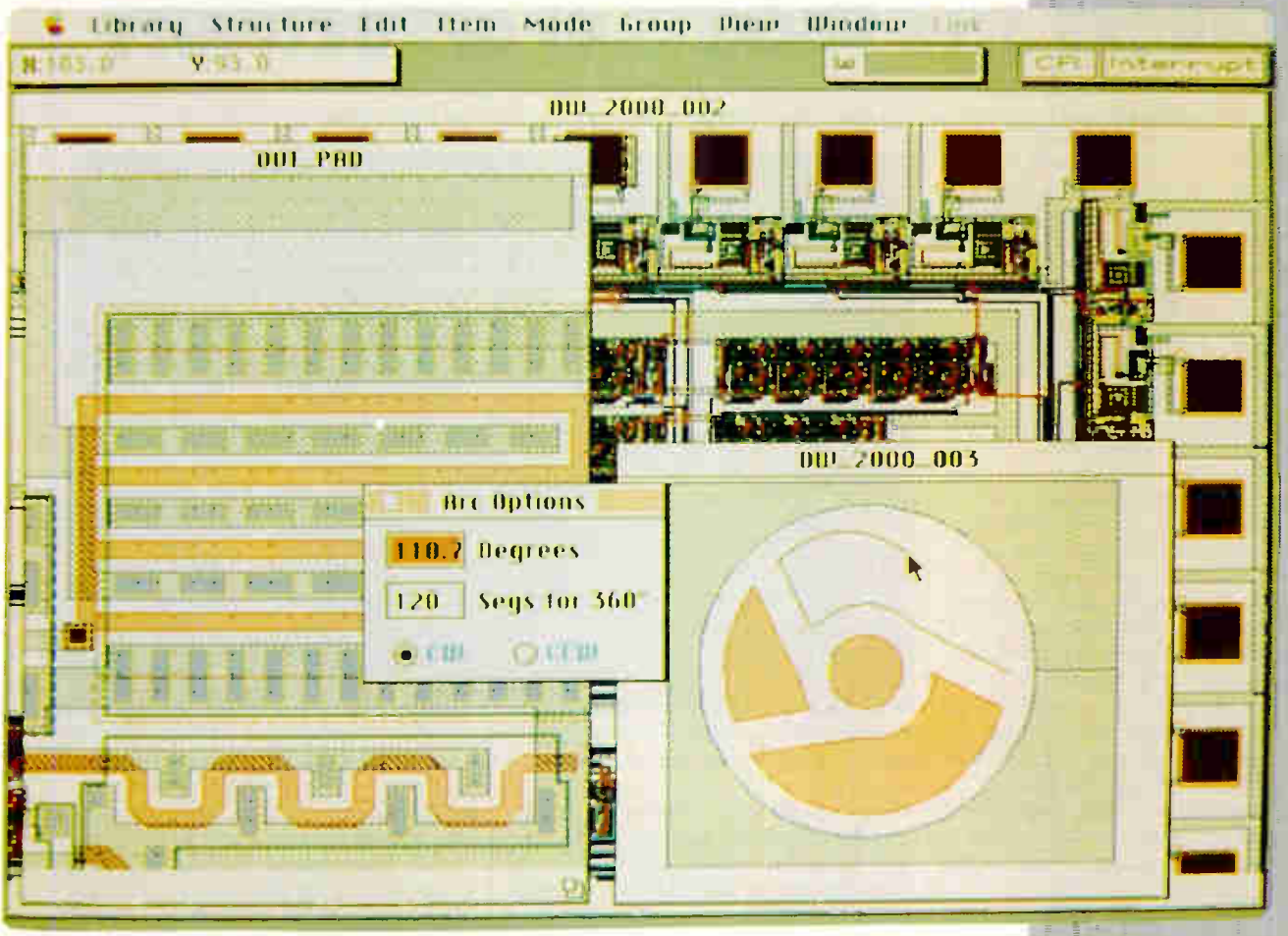

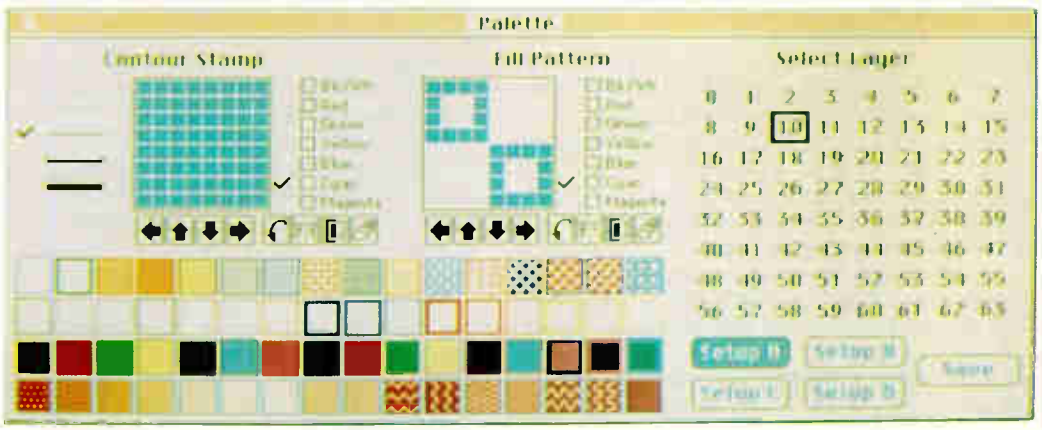

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AS THE U. S. RETOOLS ITS SPACE EFFORTS, VENDORS SEEK POCKETS OF OPPORTUNITY

Spending will rise—but most of the dollars will go to big, entrenched programs

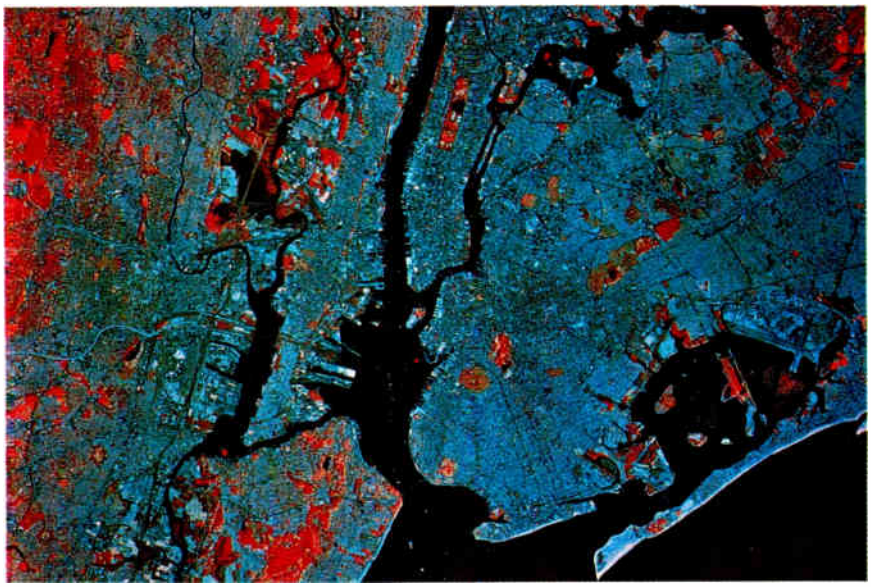
After more than two years of turmoil following the Challenger space shuttle disaster, the U. S. space program is slowly getting itself back on its feet. The shuttle Discovery carried a key Tracking and Data Relay Satellite (TDRS) into orbit in September; the Atlantis successfully launched a not-so-secret military surveillance satellite in November; and this month Discovery will launch the third and final satellite in the TDRS system. Says National Aeronautics and Space Administration director James C. Fletcher: "The space program is back on track."

But that doesn't mean the dollars are flowing in space electronics. "It's a pretty negative environment," says analyst Gregory L. Sheppard of market-research giant Dataquest Inc., San Jose, Calif. NASA is seeking a record $13.3 billion in funding in 1990, up $2.4 billion from this year. But despite the mammoth increase—mostly aimed at developing the space station—Fletcher insists that there "isn't enough money in the budget" to pay for all of NASA's needs. He adds that the agency will seek over $200 million a year in support from the private sector beginning in 1990.

The bulk of the space platforms to be launched in the next several years are systems that have had to wait while NASA re-engineered the shuttle's rocket boosters—and while Congress re-engineered NASA and Defense Department budgets. The resulting program stretchouts put a squeeze on the space industry in the mid-1980s that is only now beginning to show signs of easing up. Even so, that won't change the highly specialized nature of space electronics. "Space is all very custom," says Sheppard. "It's hard even to call it a market."

Whatever you call it, civilian space spending will rise to about $4.4 billion in 1989, up $500 million from last year, Sheppard predicts. He says this market will continue to grow at a better than 10% annual rate through 1994. That's mostly due to NASA, plus long-planned commercial communications satellites. On the military side, space-electronics spending dipped to $5.6 billion last year from $6 billion in 1987, according to the Electronic Industries Association, and will rebound only slightly this year, to $5.9 billion.

But even with those comparatively rosy projections, only a few companies will benefit. "There aren't any huge opportunities out there if you're not well-entrenched already," says Steven R. Bell, senior market analyst at GTE Government Systems in Arlington, Va., one of a team of industry analysts who did a space-market study for the EIA almost two years ago. "I don't see anything really new coming on the scene in the next 10 years," he adds.



Remote sensing satellites, such as France's Spot 1 and 2, are pushing for ever higher resolution. This photo of the New York area is by Spot 1, which delivers 20-meter resolution in color.

The key space technologies reside mostly in the grasp of a handful of major systems builders—Ford Aerospace, General Electric, Hughes Aircraft, Lockheed, and TRW are names that come up over and over again as participants in virtually every major space-systems contract. The remaining opportunities will be for radiation-hardened semiconductor technology (see story, opposite), plus a fair amount of ground-based processing and maintenance work.

MORE COMPETITIVE. Indeed, 20 cents of every dollar spent on space electronics goes toward ground-based control, data-processing, and communications equipment, Sheppard says. "And ground systems are perhaps a little more [open to competition] because, for many of these systems, you can use commercial computers and components. It's not so specialized."

One likely opportunity lies in the growing field of remote-sensing satellites, which use scanning technologies to photograph the earth in order to track geologic and human-induced changes on its surface. The French Space Agency will launch Spot 2, its second imaging satellite, this year, and plans are already in the works for Spot 3 and Spot 4. And sources say that a Japanese entry is imminent. Spot 2 will be identical to Spot 1, but future Spots and perhaps the Japanese system may try to push for higher resolution than the 10- and 20-meter resolution that Spot 1 delivers in monochrome and color, respectively.

But moving to higher resolutions will require some ground-based innovations, says Philippe Delclaux, director of technical operations at Spot Image Corp., the Reston, Va., unit of Spot Image SA of Toulouse, France, which has rights to Spot 1 data and markets photographic images produced by Spot 1. The problem is that a single image today—a 60-by-60-km square—records in 9 seconds at the current 50-Mbit/s rate, so it doesn't take long to fill up a 45-Gbyte high-density magnetic tape.

Increasing resolution to 5 meters, Delclaux says, would mean boosting transmission rates from 50 to 200 Mbits/s and would require a new method of capturing such huge data dumps. Current alternatives to the high-density tape that Spot now uses include optical-disk and even optical-tape technologies, but so far neither has proven fast enough.

NASA will face a similar problem when

it launches its own imaging satellite into polar orbit some time in 1996, says Al Fleigh, program manager for the project at Goddard Space Flight Center in Greenbelt, Md. Unlike Spot, which can record imaging data only in daylight and transmit only when within reach of one of a handful of ground stations, the NASA system will record and transmit data 24 hours a day, 365 days a year. "If you talk about the amount of data that's got to be taken down and processed, it gets frightening," Fleigh says.

Most of the processing for the polar platforms will be confined to the ground, and such data-handling problems are driving a major push on both the civilian and military fronts to focus on better ways to handle and retrieve data obtained from space. For example, systems such as Spot cannot see through clouds—and fully three-quarters of the data in Spot Image's archive are cloudy, Delclaux says. So there's a big need for a system capable of identifying useless data—and determining the difference between clouds and bright ground cover such as snow and ice.

But Delclaux adds that such problems will not be easy to solve—and that they may not be worth the trouble. "If we add all these fancy features on board and don't sacrifice the quality, then the cost and weight of the spacecraft will be driven up considerably," he says. In most cases, "it's cheaper to solve the problem on the ground than on board."

One important on-board innovation that's likely to materialize is more intelligence. Most current communication satellites provide little more than what industry insiders call "bent-pipe" communications—that is, they accept a signal from the ground and bounce it back unchanged to another location. But NASA and other space organizations foresee the future satellite as acting not so much as a pipe, but as a switchboard.

DOUBLE WHAMMY. This notion of "a switchboard in the sky," as one NASA contractor calls it, will be tested when the agency finally launches the Advanced Communications Technology Satellite in 1992. Originally set for a September 1988 liftoff, ACTS was delayed by a double whammy: the shuttle accident and budget cuts. But it will likely be the most advanced civilian space-communication experiment to date and will serve as a model for future commercial systems, says Ron Schertler, chief of experiments in the ACTS Project Office at NASA's Lewis Research Center near Cleveland.

President Reagan's proposed 1990 budget seeks to cancel ACTS, but NASA director Fletcher says he is confident that Congress, which has shown strong support for the program in the past, will restore funding. While the President's budget office annually derides ACTS as a federal subsidy for the commercial communications industry, he says, Congress recognizes the importance of the $499 million program.

The system would be used primarily for long-distance telephone service and would be transparent to the user. The key to the technology is a space-borne baseband processor—built for prime contractor General Electric Co. of Fairfield, Conn., by Motorola Inc.— that handles the decompression and demultiplexing.

NASA's launch of the ACTS satellite will test the 'switchboard in the sky'

ACTS will demonstrate only a portion of what could eventually be a whole system of communications satellites that could channel data and voice all over the world, says C. Larry Brown, ACTS program manager at Motorola's Government Electronics Group in Chandler, Ariz. The development of burst demodulators that acquire huge bursts of data, demodulate the signals, then pass them on to a routing and switching system was a key step along the way, he says, and one that will have a payoff. "The next generation of commercial and military satellites will start using some form of baseband processing," Brown predicts.

Indeed, in 1990 the Pentagon will launch what may be the most advanced satellite system in history, when the first of 20 or more Milstar communications satellites makes its way into space. Milstar, a classified program believed to cost several hundred million dollars a year, will mark the first major foray into extremely high-frequency communication bands, while continuing to support the ultrahigh-frequency communications links now used by U. S. defense forces.

But Milstar will also demonstrate highly sophisticated processing that experts say has never before been used in space. This includes antijamming systems that use fast frequency-hopping and signal-processing techniques; 60-GHz satellite-to-satellite cross links; and two entirely different modulating schemes for the up- and downlinks. To frustrate potential eavesdroppers, frequency-division multiple-access technology will be used for earth-to-satellite transmissions, while a time-division multiple-access scheme will be used for the downlink. "That's the state of the art in the labs, and they're trying to put it up now," says GTE's Bell.

Lasers are also getting attention for use in space. NASA, the European Space Agency, and the military all are keen on using lasers in intersatellite communications, and the Navy is considering using them to communicate with submarines as an alternative to flying specially equipped aircraft. *–Tobias Naegele*

RAD-HARD IC MARKET SET TO SOAR IN 1990s

The few companies that have positioned themselves in the market for space-class chips are sure to profit in the 1990s. Many space systems still use conventional integrated-circuit technologies and elaborate radiation-shielding techniques to protect them. But demand for true radiation hardening is increasing, experts say. The technology lag that has till now kept VLSI on the ground is beginning to give way.

With the National Aeronautics and Space Administration and the military both looking to add on-board processing capabilities to their satellite systems, the weight and space considerations of fancy shielding schemes are making inherently rad-hard ICs seem like a better bet than ever. "Rad-hard is going to be one of the more buoyant areas in the space market," says Gregory L. Sheppard of Dataquest Inc. in San Jose, Calif. Although it remains a small niche market dominated by Harris Corp. of Melbourne, Fla., "this is going to be a very strong area in the mid-1990s," he says.

The efforts of companies such as Harris, Hughes Aircraft, IBM, Texas Instruments, and Westinghouse, which have all invested heavily in developing rad-hard chip technologies, appear to be nearing a payoff. While the high levels of risk inherent in space systems have so far grounded chips developed under the Very High Speed Integrated Circuits program, that seems to be changing. A spokesman for IBM Corp.'s Federal Systems Division in Manassas, Va., says the division is committed to becoming a major supplier of rad-hard static random-access memories, using technology leveraged from its VHSIC contracts. While IBM hasn't written orders for any rad-hard SRAMs yet, "we think we're close to selling some," says Philip B. Johnson, one of IBM's VHSIC program managers.

VHSIC has been greeted rather coolly by military program managers in general. But VHSIC technology will finally break through the stratosphere this spring in a classified, experimental space shot that will test the viability of replacing mechanical tape recorders in reconnaissance satellites with arrays of solid-state memory chips. Researchers at Lawrence Livermore National Laboratories are now assembling hybrid packages of ten 64-Kbit SRAMs fabricated by National Semiconductor Corp. in 1.25-μm VHSIC Phase 1 technology. *–T.N.*

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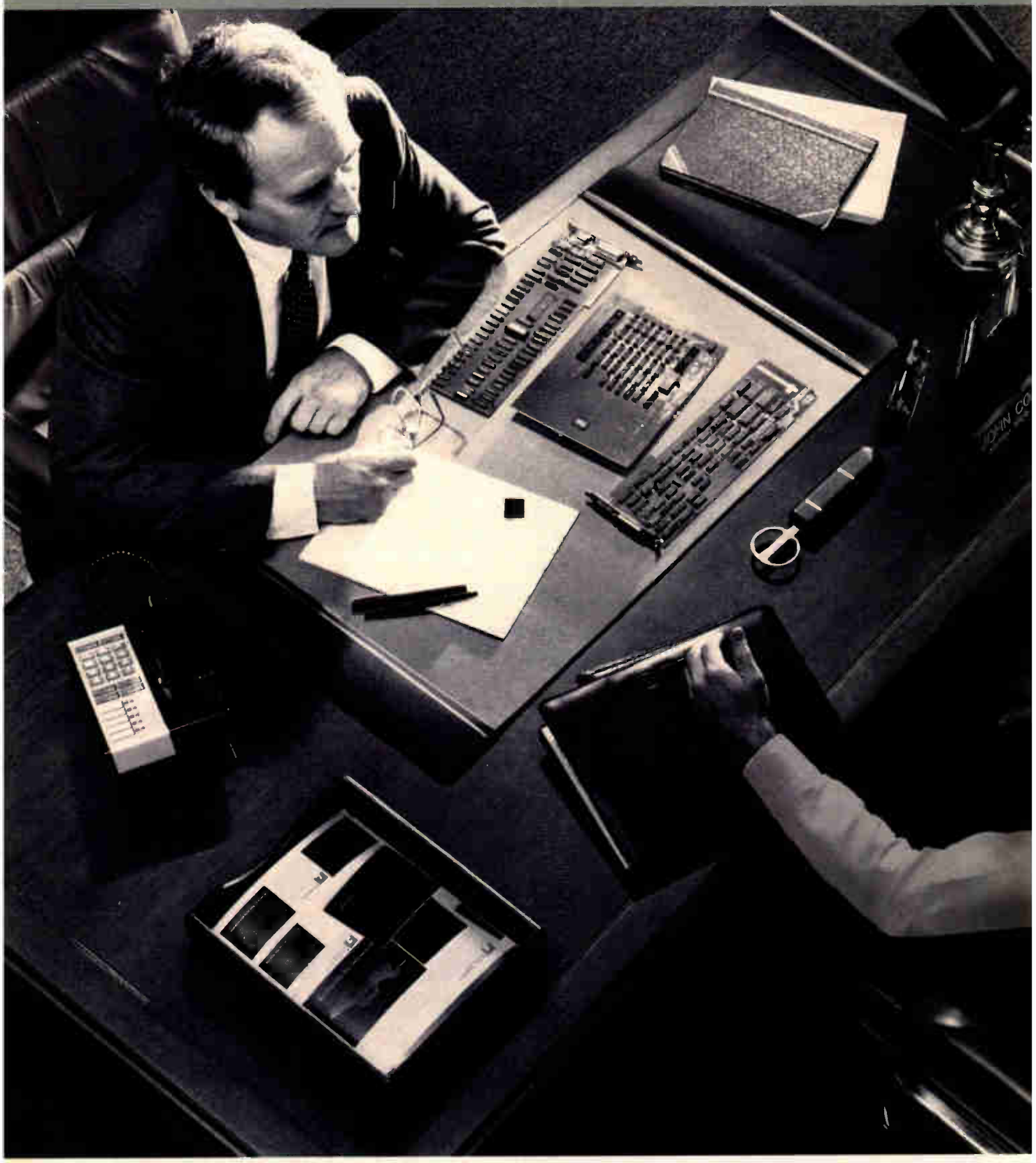

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ZILOG HITS BACK IN SERIAL COMMUNICATIONS

Once a dominant supplier of serial-communications controllers, Zilog Corp. is flexing its muscles again. The Campbell, Calif., company is about to release not just one, but an entire family of general-purpose serial-communication controller chips. All of the new devices will provide speeds of up to 10 Mbits/s—that's four times the transmission performance of Zilog's previous generation of general-purpose controller. In addition, all the chips will feature dual-channel communications capability and support 12 different serial formats.

The first device to debut is the 16-bit Z16C30, a universal serial-communications controller fabricated with the company's 1.6-μm n-well CMOS process. It features two full-duplex channels, two baud-rate generators, two 32-byte first-in, first-out memories, and a digital phase-locked loop. It also boasts logic to support eight protocols and eight different formats, including asynchronous, bit and byte synchronous, isochronous, Ethernet, and Mil-Std-1553B. The other chips making up the new family of controllers will follow over the next two years, the company says.

The Z16C30 is designed to work as either a serial-to-parallel or parallel-to-serial conversion-and-control device. It is aimed at such applications as linking a central processing unit and serial network, on the one hand, with serial peripherals such as diskette, cassette, and tape drives and CRTs on the other.

Available now in sample quantities, the part is priced at $105 each in 100-unit quantities; it comes in a 68-pin plastic leaded-chip carrier. Volume pricing, in quantities of 10,000, is expected to fall below $30 each within 12 months, says Mike Hulme, director of the company's Z8000 product line, the predecessor to the Z16C30.

The chips represent a push to regain dominance in serial communication controllers

The Z16C30 is more than just another new product for Zilog. It represents the company's big push to regain a dominant position as a supplier of serial communications controllers.

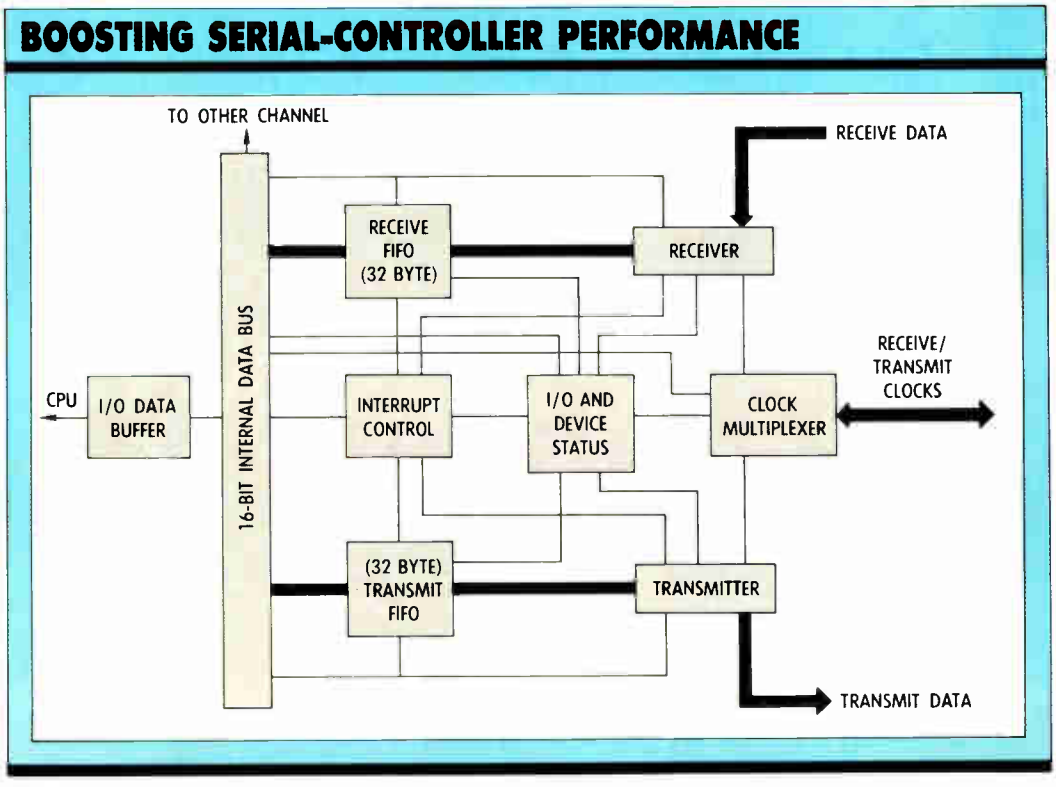
The new controller is the 16-bit follow-on to the n-MOS 8030/8530 and CMOS 80C30/85C30. These general-purpose, 8-bit, multiplexed and demultiplexed, dual-channel, serial-communications controllers were introduced in 1981, Hulme says. With speeds of 2.5 Mbits/s, they soon became the serial controller of choice. They replaced the universal synchronous and asynchronous receiver/transmitters then most commonly used, which topped out in performance at about 9.6 Mbits/s. As the leader in its market, the Zilog architecture has been widely second-sourced by semiconductor companies as diverse at National Semiconductor, Signetics, and VLSI Technology, to name a few.

But in the past few years, Zilog's parts have been forced to share the market with a variety of other general-purpose multiprotocol, multichannel, and specialized-protocol designs. These newer devices have eroded the preeminence of the earlier Zilog products.

In the first category of competitors are Signetics' 4-Mbit/s SCN68562, NEC's 2-Mbit/s μPD72001, and AT&T's T7110 Spyder. In the second are the SCC2698 octal UART from Signetics; a similar octal device from Standard Microsystems, capable of operation up to 38.4 Mbits/s; and the CL-CD100 family from Cirrus Logic, running at 10 Mbits/s. In the third are companies such as Chips & Technologies Inc. and National Semiconductor Corp. Chips & Technologies' offering is a two-chip set, the 82C570, which implements IBM Corp.'s 3270 serial-terminal protocol and runs at 4.7 Mbits/s. It serves as an input-output processor to emulate most of the IBM terminals and printers, including the 3276, 3274, and 3174 control units. Targeting the same IBM serial-protocol market is National with its 2- to 4-Mbit/s biphase dual-channel communications processor, the BCP8344. A 20-MHz multiprotocol device, it implements the IBM 3270/3299 coaxial protocol, the 5250 twin-axial protocol, or a general-purpose, 8-bit, serial-protocol channel.

The Z16C30 is an impressive first step toward reestablishing Zilog's dominance in the market. The chip contains two independent full-duplex serial channels, each with the necessary support circuitry: two baud-rate generators, a digital phase-lock loop for clock recovery, two character counters for message-length count-

BOOSTING SERIAL-CONTROLLER PERFORMANCE



Zilog's 16-bit controller family has two independent full-duplex channels like this one.

ing, full interrupt support, and a full-duplex interface to external direct-memory-access circuitry. Each chananel also contains a 32-byte FIFO, by which the controller can move 32-byte blocks of data in single bursts, which works out to 8 to 10 times faster than current devices. Zilog's own 8-bit controller, for example, requires multiple 3-byte transfers in the receive mode and 1-byte transfers in the transmit mode.

Also contained on-chip is 48 Kbits of read-only memory, which is divided into 12-Kbit arrays for both the transmit and receive sections on both channels. The ROMs hold the microcode and instructions for implementing eight different serial communications protocols—asynchronous, isochronous, monosync, bisync, transparent bisync, HDLC, IEEE 802.3 Ethernet, and Mil-Std-1553B. They can also implement eight different data formats, including four nonrecurring-zero variants and four biphase alternatives.

In essence, both the receiver and transmitter in each channel are microcoded serial processors in which data shifts through the send and receive shift registers, says Monte Dalrymple, Zilog's director of architectural design. The microcode in each channel is used to watch for specific bit patterns and to count bits. At the appropriate time, data is transferred to and from the FIFOs. The microcode also checks status and generates status interrupts when appropriate.

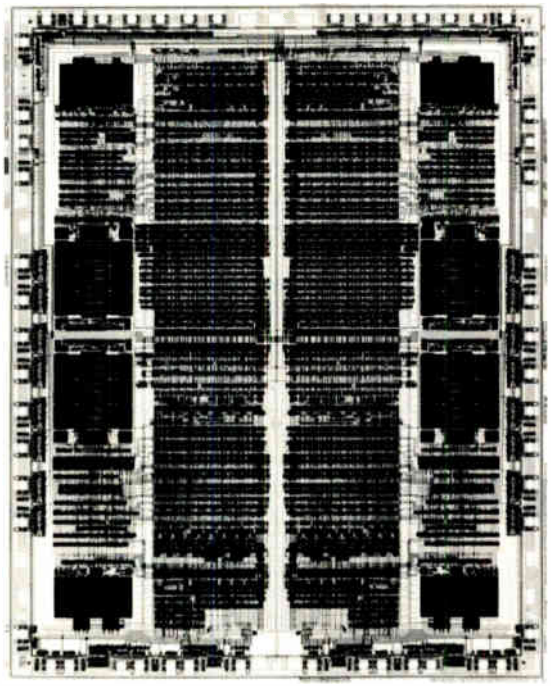
The two channels share an internal 16-bit bus interface, which incorporates a full set of control and strobe signals for direct interface to 8-, 16-, or 32-bit multiplexed or nonmultiplexed buses. Using on-board logic, the circuit watches the external microprocessor bus to determine whether it is multiplexed or nonmultiplexed, and determines the bus width and the wait/ready protocol to use during interrupt-acknowledge cycles. The bus cycle time is 160 ns; the access time, 85 ns.

Interrupts are supported with a CPU-to-universal-serial-controller daisy-chain hierarchy. This scheme is designed to support easy bus arbitration, with each channel having completely independent interrupt structures.

As a bonus, the Zilog device incorporates logic for bus-oriented testability. Such testability is a significant advantage over competitive products, according to Hulme.

In the bus-oriented testing method, dedicated test registers are buried in the device and accessible via the data bus through two registers in the register set. One register is used as an address pointer to select the specific test register desired, while the other functions as a window to the desired test register.

Incorporation of such structures was deemed vitally important in the design of the Z16C30, Hulme says, because access to internal nodes is particularly difficult in a serial input/output device. The difficulty results from the large number of cycles that are required to create specific conditions. For example, testing the RAM-based FIFOs on the chip requires large numbers of messages to be transferred to test for pattern sensitivities in the status bits. With bus-oriented testing, a test register is present at the input to the receive FIFO, allowing arbitrary data and status bits to be written directly into the FIFO. Similarly, for the transmitter, a test register is located at the output to the FIFO to extract data that otherwise would have to be shifted out of the transmitter.



On the Z16C30, microcode implements eight different communications protocols and eight different data formats.

STATE MACHINES. A similar approach is used in the interrupt logic section, which contains small asynchronous state machines that track interrupt conditions. These state machines are difficult to test, Hulme says, because they resolve simultaneous inputs and are many levels of logic away from the I/O signals. However, a test register at the inputs of the state machines allows consistent creation of this special case, so correct operation can be guaranteed.

Other test registers located throughout the device allow access to the on-board 32-bit cyclic redundancy checker and generator, both the receive and transmit data paths, and the state of the on-board digital phase locked-loop circuitry. The device also contains a large multi-input and multi-output multiplexer for clock signals, with test registers on both the input and output.

Other important features include automatic 8-, 16-, and 32-bit cycle redundancy checking, mark idle synchronization, programmable synchronization characters, channel-load commands for direct-memory-access-controlled initialization, as well as a transmitter-to-receiver character synchronization.

To make designing with the controller simpler and faster, Zilog is offering development kits for use with the company's Z280 and the Motorola 68000 processors, for $445 and $495 each, respectively. Each kit contains a development board with a socket-mounted controller, on-board direct-memory-access circuitry, and 64 Kbytes of ROM; schematics; and a diskette with sample application software.

Also being offered is a utility called the Programmer's Assistant, an electronic work sheet that automates the initialization process by allowing the user to quickly locate controller registers and their bit-value options. Hulme says the utility, which will be available for a nominal charge, steps the user through a series of menu selections in which all controller functions are displayed and from which the user selects the features that reflect a particular application and hardware design.

Despite the Z16C30's advanced features and higher performance, Hulme says, it is not expected to go it alone. The Z16C30 is only the first of a number of serial communications controllers the company plans to introduce over the next two years, at a rate of approximately one every six months.

The next to arrive will be a 16-Mbit version of the universal serial controller, fabricated with a new 1.4-μm CMOS process, that incorporates four DMA channels. Scheduled for early 1990 is a smart universal serial controller that will be capable of operation at up to 20 Mbits. Fabricated with a 1.2-μm CMOS process, it will contain a 16-bit Z8000 processor, a single universal-serial-control channel, two DMA channels, on-board erasable programmable ROM or ROM, and a dual-port random-access memory.

A similar upgrade pathway is planned for the 8-bit serial communications controller, with an integrated version containing four on-board DMA channels scheduled for mid-1989 along with a smart serial communications controller with an embedded Z80 processor, dual-port RAM, and on-board EPROM or ROM. *–Bernard C. Cole*

A ONE-CHIP BOOST FOR DESKTOP GRAPHICS

System makers can build desktop computers that deliver the same color graphics as high-end work stations at a fraction of work-station prices, with a video-controller chip from Inmos Corp. The Colorado Springs, Colo., company's IMS G300 is a general-purpose controller that integrates all the control and data-conversion functions needed to implement a bit-mapped graphics subsystem. All a designer needs to build such a system without going over budget is the G300, a microprocessor to serve as a central-processing unit, a frame-buffer memory, and a few other circuits.

The G300 offers a single-chip solution for all of the real-time functions of a graphics subsystem, including interfaces to the CPU and video random-access-memory array, with a minimum of external circuitry. The analog outputs can be configured to drive a wide variety of display devices, ranging from a high-resolution graphics monitor to a standard RS 170A TV screen. Pricing had not yet been set as of late last month.

The controller integrates video timing, screen refreshing, and pixel-flow control with color expansion and digital-to-analog conversion in one 84-pin package. The internal architecture is 24 bits wide, ensuring a large enough address range and high enough resolution for most applications. Any CPU can be used, since the G300 is compatible with 8-, 16-, and 32-bit interfaces. It handles screens of any size and resolution, limited only by the bandwidth of the video dynamic RAMs.

Business computer users are beginning to demand both increased computing power and the kind of graphics that the G300 can help provide. They want a desktop tool that can perform heavy computation while interpreting and displaying the results in complex graphics, even three-dimensional graphics.

To get that kind of performance and still keep the desktop system competitively priced, however, designers cannot afford to use the highly specialized and expensive graphics architectures common to big work stations. One common method of producing high-quality graphics, for example, has been to use a coprocessor with a set of microcoded or hardware-implemented drawing instructions to take over the low-level graphics tasks, such as line and arc drawing. This is not a very flexible solution, since new chips or microcodes have to be developed when new and better algorithms come along.

Business users now demand graphics power that the G300 can help provide

What efficient graphics systems need is not more special instructions but large amounts of general-purpose processing power—a simple architecture where the response time is determined by the power of the processors used and the bandwidth for delivering drawing instructions to the frame buffer (bit map). This kind of architecture gives the host processor free access to the pathway to the graphics frame-buffer memory.

In such an environment, the potential for performance improvements is found mainly in the raw speed of the host processor and the efficiency with which it supports core graphics operations. To aid the design of systems with this type of free-access graphics architecture, what is needed is a simple, inexpensive way to handle all the tasks required to transform the data in the frame buffer into the pixels to be delivered to the display device. It is precisely these capabilities that Inmos has built into the G300.

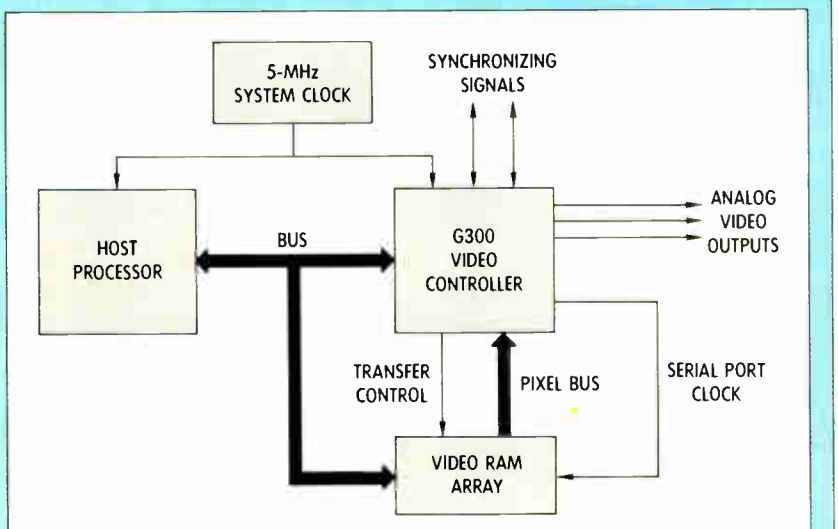
The chip is powerful enough to handle all of the operations required to turn data into pixels and move them from the frame buffer to the screen. It includes screen-refresh address generation—both interlaced and noninterlaced—video synchronization, and data conversion. It also boasts automatic line-increment capability, a color-lookup table, a triple video DAC, and a phase-locked loop.

The video-timing generator is a programmable state machine that accepts a simple description of the video system as a set of numerical parameters. The screen parameters include the width of the horizontal synchronization pulse, the duration of the setup, the number of pixels dislayed in both a full-scan line and a half-scan line, the width of the frame-synchronization equalizing pulse, the width of the frame-sync pulse, the number of blanked lines per frame, and the number of displayed lines per frame.

For sophisticated control of the screen refreshing, a small set of registers holds the description of the video system and the bit-map configuration. The screen-refresh mechanism uses direct memory access to read the data in the video RAM frame buffer, allowing a seamless mid-line update of the screen. This approach keeps the impact of the screen update function on the processor-to-frame-buffer bandwidth to a minimum.

In the color-lookup table, the color of each pixel is defined as the 8-bit address of a color that is described by more than 8 bits—possibly up to 24 bits for a very large range. The price incurred by using a color-lookup table is a reduction in the number of colors that can be displayed simultaneously. High-end graphics systems, which require many simultaneous colors, use 24-bit direct addressing, but require much more frame-buffer memory than an 8-bit indirect color-lookup table to do it. The table built into the G300 is a 256-location 24-bit table. *–Tom Manuel*

PUTTING HIGH-QUALITY GRAPHICS ON A DESKTOP



The Inmos G300 offers the real-time functions of a bit-mapped graphics subsystem.

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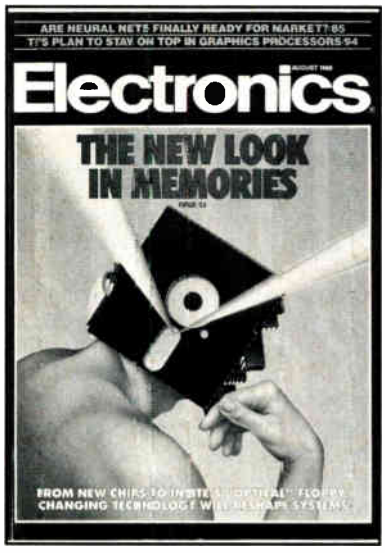

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FINALLY, PROGRAMMABLE ARRAYS MAKE SENSE

Programmable gate arrays are starting to get a lot of attention from system builders in spite of the lack of design aids available for them. Now Data I/O Corp. is bringing out a tool for in-circuit verification and debugging of the arrays that ought to make them far easier to use.

The programmable gate array differs from conventional gate arrays in that the user, rather than a silicon foundry, programs them. They are becoming more popular as they offer the designer more complexity; up to 15,000 gates are available now. Some $30 million worth of them were designed into systems last year, according to Dataquest Inc., a San Jose, Calif., market research firm, up from virtuallly nothing a few years ago.

At the same time, more gates on an array demand better instrumentation to help design with the devices. "What's needed is an instrument that will help the designer verify that his design has been properly downloaded into the PGA," says John Watson, a product marketing manager at Data I/O Corp. in Redmond, Wash. "And it should also help isolate the chip from the target system so the designer can examine what's going on inside the PGA."

Data I/O's Mesa 1 development tool kit does just that. It is a multipurpose, hardware-based tool for in-circuit verification and debugging designs based on programmable gate arrays. Its name derives from the four broad functions it covers: modeling, emulation, simulation, and analysis. The tool kit supports 68- and 84-pin plastic-leaded-chip-carrier packages. It sells for $9,400 each in quantity and is available eight weeks after order.

Mesa 1 enables designers to verify that design data is correctly downloaded; to physically observe register states within the array; to isolate specific signals from the target system and force states to isolate problems; and to experiment with design alternatives in real time in the target system. It also acts as an instant breadboard so that designers can experiment with a variety of alternatives.

A key feature of the Mesa 1 is its ability to run the array being tested in parallel with its own on-board shadow array, says David Kohlmeier, engineering manager.

> More gates demand better instrumentation to help design with the devices

The device under test and the instrument running in parallel receive all input stimulus concurrently. At any time, the designer can halt system operation from the instrument. Once the system has been stopped, the designer can examine the registers of the device under test by viewing the registers of the shadow array on the Mesa 1.

Connecting to and controlling the operation of an array in a target system without loading the device down is no mean feat. Mesa 1 contains a flexible circuit probe at the end of which is a 68- or 84-pin connector. The connector allows the designer to remove the target array under test and insert the probe between the target array and its socket. The designer loads the programmed configuration of the target array from his design system, which is usually a personal computer, via Mesa 1. "We can control the configuration pins to load the chip's programming," says Kohlmeier.

During analysis, the instrument is able to switch between the target part and the shadow array. It can also stimulate the target array by running test vectors through the system, which allows the designer to determine if the system is responding correctly. By doing so, he can isolate whether the problem is inside the array or outside in the surrounding system.

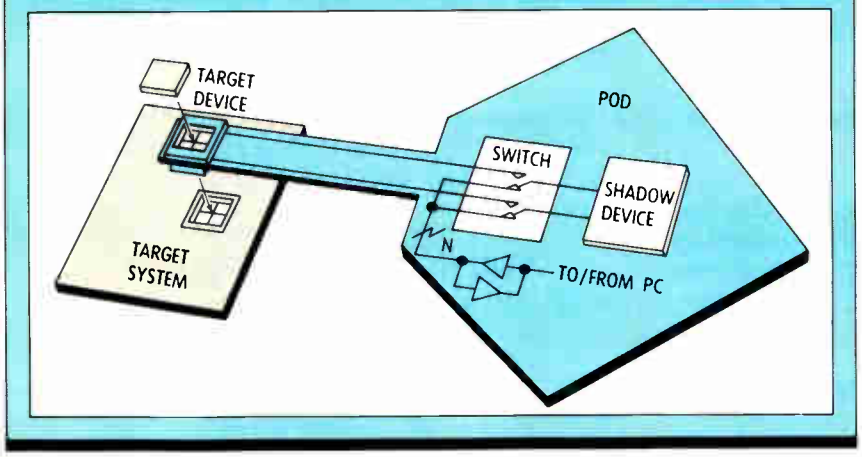
In addition, the designer can run design-verification vectors or the equivalent of simulation right on the target array. He can stimulate the target array with simulation vectors to see how it operates by taking snapshots of the register contents after a set of vectors has been applied. The designer can apply a stimulus pattern, check the array, apply another pattern and check the array, and continue the process as long as necessary. He can also connect the array responses to a logic analyzer. "We chose not to put logic-analyzer features on the Mesa 1 because so many designers already had these instruments," says Watson. "To ask them to buy a logic analyzer packaged in with the Mesa 1 would have driven the price up and possibly alienated buyers in the process. This way the designer can use his existing logic analyzer."

Because programmable gate arrays are high-speed CMOS parts with sharp, subnanosecond 5-V pulses, controlling impedance is a critical element in the instrument's design. The probe tip intercepts signals at the target array's pins and transmits them to the Mesa 1 pod, says David Nierescher, Mesa 1's mechanical engineering manager. Data I/O jointly designed the probe and its associated cable with Tektronix Inc. of Beaverton, Ore. The design uses some Tektronix patents on impedance control in flexible circuits to accurately control the transmission-line impedance.

A patented interdigitizing method developed by Tektronix provides the cable with high-impedance signal lines. Each signal is compressed between two adjacent ground lines forming a zigzag pattern between the top and bottom planes. This reduces capacitance, raises transmission-line impedance, and helps to minimize crosstalk.

Mesa 1 also contains 10 programmable gate arrays used as pin-logic integrated circuits. Each array has a hybrid termination circuit virtually butted against it. A hybrid termination circuit with 50-mil pin pitch provides termination right at the pin-logic ICs. *–Jonah McLeod*

PROBING A PROGRAMMABLE GATE ARRAY



The Mesa 1 tool kit makes life easier for designers working with programmable gate arrays. Its hardware and software target modeling, emulation, simulation, and analysis.

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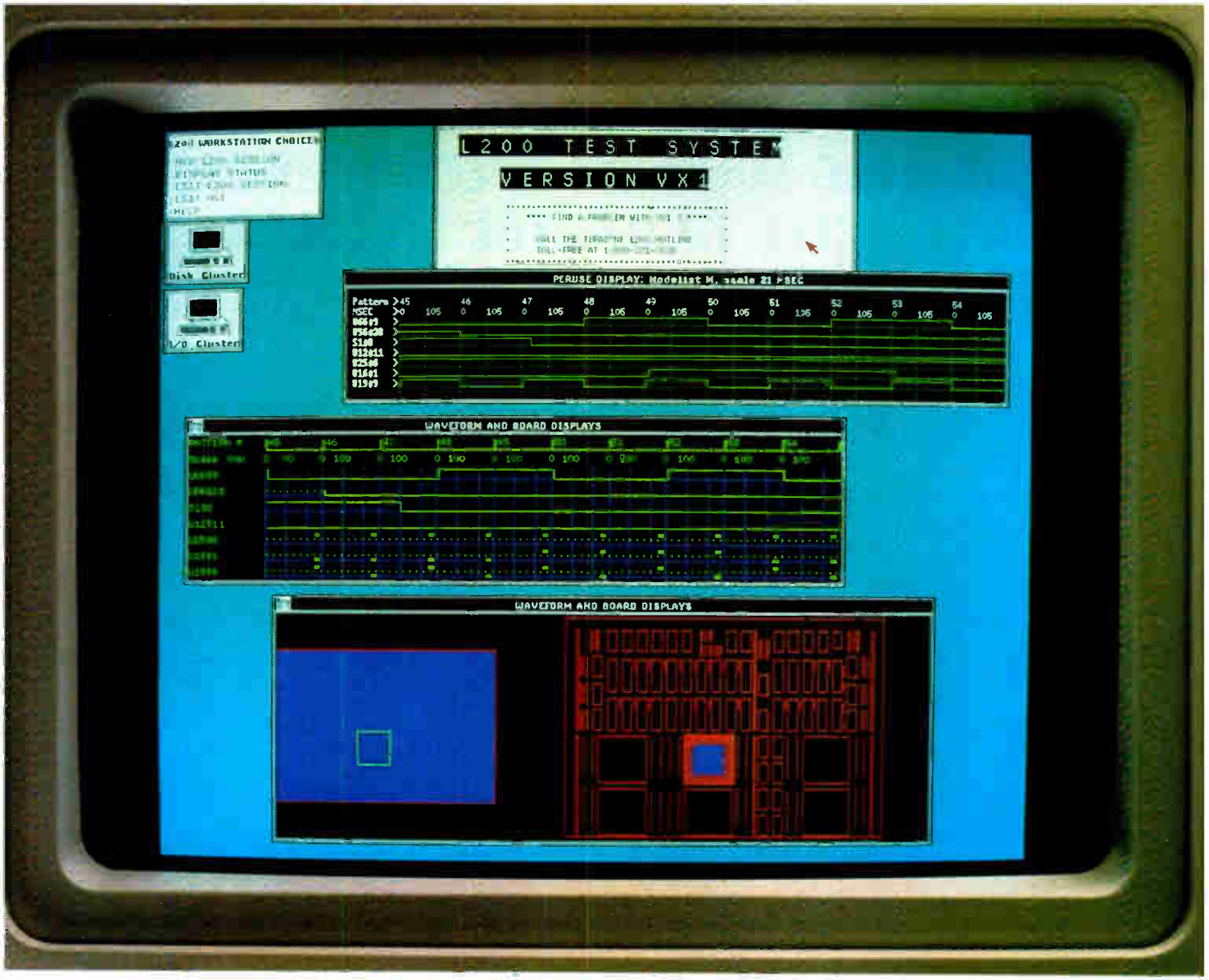

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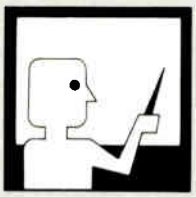
Circle 119

SIZZLING MARKETS SPEED VENDORS IN DRIVE TO DIGITAL CELLULAR

A standard, expected this year, will quell the battle between two architectures

by Jack Shandle



EXECUTIVE BRIEFING is a monthly feature of Electronics *that provides managers with a concise review of developments in fields that are making frequent headlines.*

The cellular-telephone boom is a classic case of success breeding new challenges, both technological and marketing. Less than five years after compact, reliable car phones began cropping up in major metropolitan areas, a few places—notably Los Angeles—are already pushing the upper limit of call-carrying capacity. To meet the spiraling demand, the industry is hustling to replace the first generation of cellular technology—which is based on analog signaling—with digital solutions.

Virtually everyone agrees that digital is the answer: cellular-system vendors say it will provide at least three times greater call-carrying capacity in the same bandwidth. But just which digital technology will win the day is a matter of debate. Currently, two architectures—one based on time-division multiplexing and the other on frequency-division multiplexing—are vying to become the new North American industry standard. Systems based on both are now being field-tested.

The date of the changeover from analog to digital will depend on the timing of the Telecommunications Industry Association's digital-technology standard, says analyst Herschel Shosteck, president of Herschel Shosteck Associates Inc. in Silver Spring, Md. It's expected early this year, and will be followed by federal regulations based on the TIA's recommendations. Wide-scale implementation could begin as early as 1991.

The technology drive is being spurred by marketplace sizzle. Europe is poised for rapid cellular growth, thanks to the commitment to pan-European communications standards that will arrive in 1992. Elsewhere, developing nations that lack wired telephone systems are turning to cellular as a more economical means of implementing a telecommunications infrastructure. And in the U. S., the Federal Communications Commission has begun awarding cellular franchises in the rural areas that make up 70% of the nation's land area.

All these developments add up to a spectacular worldwide market for the next decade. By 1992 there will be between 6 million and 7 million cellular subscribers worldwide, says a survey conducted for the Cellular Telecommunications Industry Association by the New York analysts Booz, Allen & Hamilton Inc. It forecasts that by 1995, this number will have climbed to perhaps 18 million. Jim Caile, director of cellular marketing for Motorola Inc.'s Schaumburg, Ill.-based Cellular Division, has roughly the same predictions: from a base of 4 million worldwide subscribers this year, he says, the number will skyrocket to 20 million by the mid-1990s and to 50 million by the end of the century.

The U. S. will account for most of the subscribers through the early 1990s. From a base of just 5,000 in 1983, the U. S. market soared to 2.1 million by the end of 1988, says analyst Shosteck. He projects the U. S. market rising to 3.2 million subscribers by the end of 1989; 4.5 million by the end of 1990; and 12 million by 1995.

Meanwhile, Shosteck predicts the retail price of analog cellular phones will continue its free-fall—from a "low drive-away price of $760 in 1988, it will drop to about $490 in 1990." But the introduction of digital technology in 1991 or 1992 will send prices shooting back up. Caile estimates that the price of a digital system will be 50% to 75% higher than for analog sets. "Most of the service providers have endorsed a dual-mode mobile unit that can operate as either analog or digital," he says. "That in itself will make them more expensive initially, because you are manufacturing two units in one." Digital prices will, however, follow the same price curve as the analog generation, he says, falling about 30% for every cumulative doubling of the total subscriber base.

MORE CAPACITY. The digital drive is being fueled by the need for greater channel capacity. "In Los Angeles, sometimes you just can't get through. You can't complete your call," says Jerry Schumacher, executive vice president of International Mobile Machines Corp. in Philadelphia. That's why International Mobile Machines is conducting a field trial of its time-division multiple-access (TDMA) system in the Philadelphia area.

Simply put, digital systems provide more efficient use of the 30-KHz frequency band used for each call, because bit streams can be more easily processed than analog signals. The powerful new digital signal processors are what make digital cellular possible, says Nils Rydbeck, director of cellular-radio research for Ericsson Inc. in Richardson, Texas. Among such DSPs are Texas Instruments Inc.'s 32020 and 32025 and AT&T Co.'s DSP16A.

Ultimately, digital techniques may boost capacity far beyond the threefold

CELLULAR SHIFTS INTO HIGH GEAR

	Number of U. S. cellular subscribers	Net U. S. subscriber growth	Telephones sold
1983	5,000	5,000	5,000
1984	125,000	120,000	130,000
1985	329,000	204,000	220,000
1986	655,000	326,000	390,000
1987	1,114,000	459,000	570,000
1988*	2,100,000	1,000,000	1,300,000
1989*	3,250,000	1,150,000	1,550,000
1990*	4,550,000	1,300,000	1,800,000

* ESTIMATED

SOURCE: HERSCHEL SHOSTECK ASSOCIATES, SILVER SPRING, MD.

increase now foreseen: Rydbeck sees a tenfold increase over analog capability in the long run, and International Mobile Machines' Schumacher a sixteenfold rise. But digital offers other benefits as well. "It will allow the use of more robust algorithms for handing off calls from one cell to another," says Shosteck, "and it will provide better voice quality." Digital technology will also position cellular systems for the advent of the integrated services digital network in the mid-1990s.

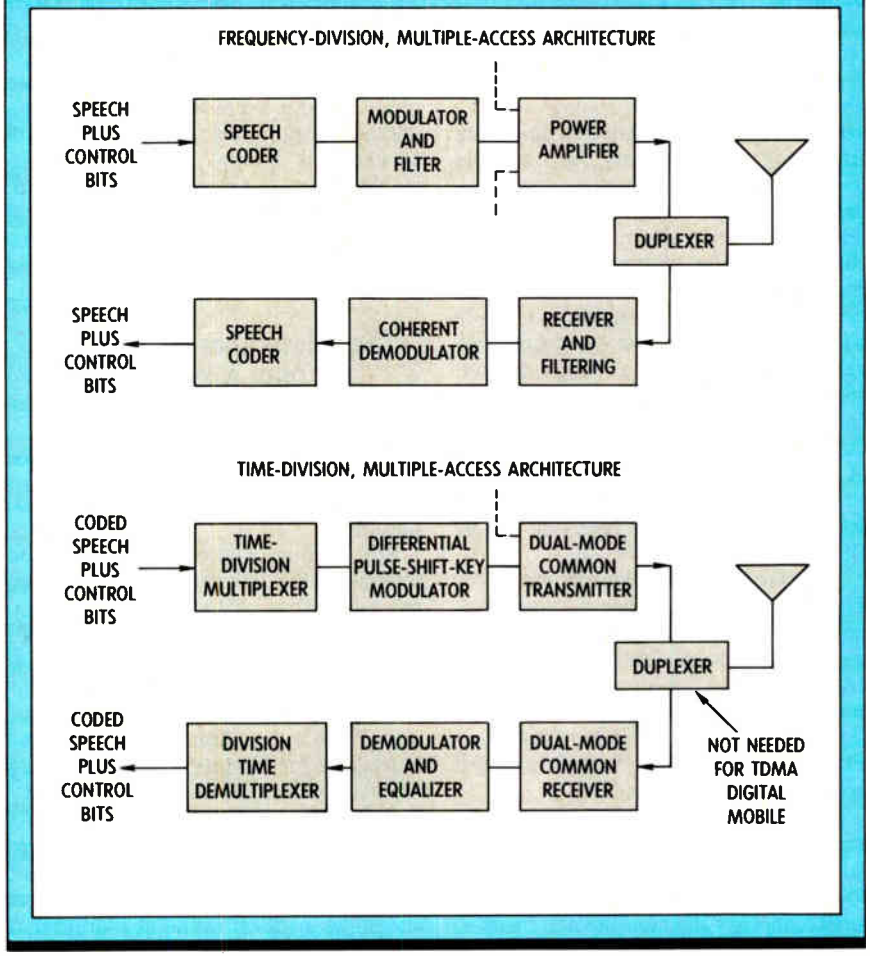
Going head to head for the digital top spot are two types of multiplexing systems: TDMA and frequency-division multiple access (FDMA). In the field trials now under way, TDMA systems use the same 30-KHz band for signaling as analog. But instead of allowing the signal transmitting one conversation to tie up the channel continuously, TDMA assigns time slots for three conversations. The conversations are burst across the radio band sequentially, identified at the cell site, and then reconstructed by the DSP. In addition to International Mobile Machines' TDMA trial in Philadelphia, Ericsson concluded its test in Los Angeles last month and Northern Telecom Inc. of Richardson will try out its TDMA system in Dallas this month.

The competing FDMA technology has its own champions—and powerful ones at that. Both Motorola and AT&T Bell Labs in Basking Ridge, N. J., favor this approach, which gets its increased channel capacity by dicing the 30-KHz band into either three 10-KHz bands or four 7.5-KHz bands. Motorola began field trials last month in Los Angeles, and AT&T conducted one last April in Chicago.

SLOW START? Of course, not every industry observer is enthusiastic about the rapid switch to digital. Dominic Clancy, an analyst for London's BIS Mackintosh, says digital phones "will get off to a slow start in Europe largely because analog will be less expensive." Another inhibiting factor, says Clancy, is that digital systems can't cover as large an area as analog, and the transmission won't be much better than in the existing generation of analog systems. "Users will switch to digital only when it becomes significantly cheaper," he says, "which will not happen till the mid-1990s."

TDMA systems operate by digitally coding speech and adding the control bits that direct the decoding. The bit stream is fed into a time-division multiplexer that assigns it to a time slot. A differential pulse-code modulator converts the bit stream into a signal 30-KHz wide, and a dual-mode transmitter sends it out in the correct band within the 825-to-896-MHz bandwidth allotted for all cellular communications. The reverse process takes place on the receiving side of the conversation. FDMA systems also start by digitally coding speech, but they require a more sophisticated modulating and filtering system to put the bit stream on a 10-KHz carrier.

CELLULAR'S DIGITAL-ACCESS CONTENDERS



Using present speech-coding, DSP, and software technologies, both TDMA and FDMA offer about a 3-to-1 increase in bandwidth over analog systems. The two methods differ, however, in how they affect overall system capacity. Both require sending additional bits so the DSP on the receiving end can reconstruct the message. TDMA requires overhead bits for framing, synchronization, identifying each time slot, and accommodating radio-wave propagation-time differences among the various time slots. Since FDMA is a continuous signal, it doesn't need the same amount of overhead. Besides bits for framing and synchronization, it requires bits to allow the receiver to know where each bit is positioned relative to the boundaries of the data field. Bits are also needed to recover synchronization if the signal fades significantly.

Until the field trials are complete, there will be little hard data about the relative merits of the competing technologies in terms of capacity and cost. In the meantime, the contending camps are hard at work touting their respective systems.

FDMA can now boost channel efficiency fourfold using a 7.5-KHz band, says Motorola's Caile. "Later in the 1990s, we can use 5-KHz bands and below," he says. "There's no reason why we can't go to time-division multiplexing within a 7.5- or 5-KHz band." Caile contends that FDMA can be implemented about a year ahead of TDMA, "because we already know how to build narrow-band systems. A pure TDMA system has not been implemented in a mobile system. No one really knows how well TDMA is going to operate."

Motorola's Los Angeles field test will give a fourfold increase in channel capacity, he says: "that's here now." To get the same fourfold increase, TDMA needs DSPs boasting speeds on the order of 20 million instructions/s. Such parts are available now—but any further increases will depend on DSPs running at 100 mips, he adds; and parts that fast won't be available until the mid-1990s.

Not surprisingly, Ericsson's Rydbeck offers a more optimistic assessment of the TDMA migration path to higher and higher channel efficiency. Initially, he says, a three-to-fourfold boost is all that's needed to satisfy market pressure in even the heaviest metropolitan areas. Present

TDMA technology can increase channel capacity by a factor of 3.7, he says—with the three channels running in one 30-KHz band and the extra seven-tenths of a channel coming about through enhanced trunking efficiency.

Additional capacity—up to about seven channels per 30-KHz band—can be achieved by adding auxiliary equipment. Installing two receivers, each with its own antenna for the frequency band, improves reception enough to allow higher-level multiplexing—more time slots. The channel-efficiency multiplier can jump to the order of 10 through speech interpolation. This technique is already in use in wire-based phone systems and takes advantage of the fact that people are not speaking nonstop during a conversation. Instead of leaving the channel inactive during those pauses in conversation, bits of other conversations are used to fill up the space, with all the conversations stitched together at the receiving end by DSP techniques.

A major technological challenge for TDMA, Rydbeck says, lies in compensating for echoes bouncing off buildings and mountains. Since the timing of signals is critical in TDMA, an echo arriving at a receiver a few milliseconds after the true signal can destroy the bit stream's integrity. DSPs can eliminate this effect, which is called time dispersion.

In the regulatory arena, the FCC kicked off the competition for a new digital technology in late 1987 by proposing to open up the cellular marketplace to any technology the marketplace chooses. The industry is implementing this commitment to an open architecture under the aegis of the Cellular Telecommunications Industry Association in Washington, D. C. The CTIA will evaluate the trials conducted by AT&T, Ericsson, International Mobile Machines, Motorola, and Northern Telecom and report its findings to the TIA. That body, also Washington-based, is expected to make a decision on a digital standard early this year, says International Mobile Machines' Schumacher. Once it has adopted a standard, the FCC will pass regulations to control interference between systems by means of standards that limit field intensity and power output of base and mobile transmitters.

Digital cellular technology will play a key role in providing rural phone service

Still another open regulatory question facing the FCC is ensuring compatibility among vendors' systems. "Right now you can't drive from an area served by an AT&T cellular system and still make calls if the new franchise area uses a Motorola, NEC, Ericsson, or Novatel system," says Piush Sodha, director of product-line marketing for Northern Telecom Corp.'s Cellular Systems Division in Richardson.

But incompatibility actually becomes a selling point as new franchises are awarded, he says. Operators in adjacent franchises often argue that their system should be installed in the new area; that way, they say, people who are traveling through both locales can still use their car phones. The TIA has developed a standard protocol to allow transparent call delivery and hand-off from franchise to franchise, says Sodha, "but the protocol has gaps and the standard probably will not be defined until 1990."

A third regulatory issue—serving the 70% of the U. S. that makes up rural America—has been resolved and will result in rapid expansion of cellular systems. The rural market lies not in mobile phones, but as an alternate means of providing stationary phone service where a conventional wired system doesn't exist or is too expensive to implement.

Reflecting the particular needs of rural America, the FCC has carved out rural franchises that are served by different frequency bands and have much different rate structures than metropolitan areas. In its recent Basic Exchange Telecommunications Radio Exchange Ruling, the FCC doubled the number of frequencies available for rural cellular service. It also lets phone companies use cellular service instead of wire as the primary means of providing phone service there.

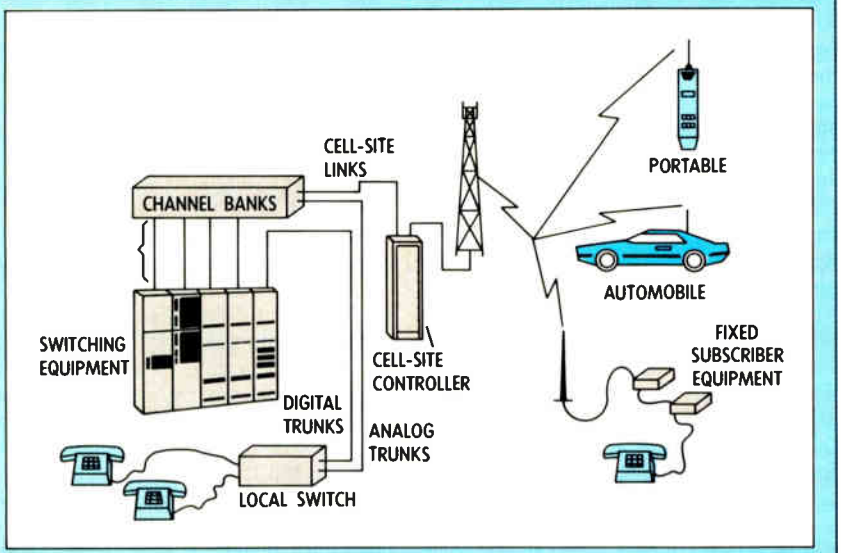
Digital technology and its enhanced channel efficiency will play a key role in providing rural cellular service, says International Mobile Machines' Schumacher, because "it beats the cost of current analog systems by a factor of three. In a digital system, we buy one radio to serve four customers instead of buying four." Rural service is particularly price-sensitive, because the FCC does not allow phone companies to levy access charges—charges per call—in rural areas. Depending on the locale, a subscriber will pay a flat rate of $8 to $12 a month, says Schumacher. The FCC has begun licensing rural franchises, says Northern Telecom's Sodha, but so far none have been constructed.

Just as digital approaches are driven by the new DSPs, cellular telephony in a broad sense is made possible by two enabling technologies: microprocessors that deliver the processing power needed to handle instantaneous switching as the mobile unit passes from one cell to another; and microcomponents such as resistors, capacitors, and VLSI circuits that reduce the volume of a mobile phone from 1,000 in.^{3} down to just 56 in.^{3}.

The first, and still current, generation of cellular technology transmits analog signals in 30-KHz bands within the 825-to-896-MHz band allocated by the FCC. Each cell has a maximum capacity of 832 channels and can serve an area up to 20 miles in diameter. In heavily used metropolitan areas, however, cell size typically shrinks to 1 mile in diameter in order to pack as much channel availability into the service area as possible.

At each cell site, the major pieces of hardware are a controller and multichannel transmitter/receiver. The controller

CELLULAR: IT'S MORE THAN CAR PHONES



Cellular system intelligence resides largely in the switch: linked to the cell site by either a microwave station or a leased line, it provides all standard telephone services, such as dial tone, plus most optional functions, such as call forwarding, call waiting, and conference calls.

sets up message transfers between radios receiving messages from mobile units and switches in the phone-company office that link the message to the conventional wired-telephone system. Controller functions include monitoring and controlling rf equipment; voice-channel assignment; call setup, supervision, and hand-off; and internal diagnostics.

Most of the cellular system's intelligence resides in the switch, which is linked to the cell site by either a microwave station or a leased line. The switch provides all standard telephone services, such dial tones, plus optional functions, such as call forwarding, call waiting, and conference calls.

There are now four worldwide standards. The North American AMPS standard operates in the 800-MHz band and offers 832 channels per cell. The other three all operate in the 900-MHz band. They include the European TACS standard, the Japanese JTACS standard, and the Nordic Mobile Telephone standard.

Cellular systems are becoming increasingly important in developing nations. That's because constructing a wired phone system represents a huge investment compared with the cost of setting up cellular. Third-world countries that opt for cellular service typically use a satellite system as a communications backbone and connect it to local service via cellular technology. In one of the more ambitious projects, Canada's Novatel Communications Ltd. is constructing a cellular system in the People's Republic of China. "It will be installed for about one third the cost of a wired infrastructure system," says Bob Betteridge, marketing manager of the Calgary, Alberta, company. The pilot system, which operates in the 450-MHz range, will have six stations in Chun King, China's third-largest city.

In Europe, too, the market for cellular systems is booming and should reach $3 billion by 1993, says Frost & Sullivan Ltd., a London-based research firm. Shipments of phones are forecast to jump from 483,000 in 1987 to 1.6 million in 1993. The subscriber base, which was 941,000 in 1987, will reach 4.9 million by 1993.

ECONOMIES OF SCALE. Pan-European standardization is a major reason for the market growth, because it lets manufacturers take advantage of the economies of scale to drive prices down. Earlier this year, the Normes Européenes de Télécommunications set equipment specifications for cellular phones. Plans are under way for an all-digital pan-European network using TDMA technology. Eighteen countries from Finland to Portugal and from Iceland to Greece will participate in the GSM (for Groupe Special Mobile) network. When the first cells start working in 1991, they will be able to send data at 2,400 bits/s as well as handling facsimile, videotext, and, of course, voice.

Standardization will result in low-end terminals selling for about half their present price, according to West German estimates. Cognizant of the market potential, many major communications firms are teaming up to bid on development contracts that will be awarded by each country separately. West Germany's AEG AG and SEL AG have teamed with France's Alcatel NV and the Finnish Nokia group. ANT Telecommunications, Robert Bosch GmbH, and Telenorma GmbH—all of West Germany—have banded with Philips International of the Netherlands' German subsidiary, PKI. What's more, Siemens AG has teamed with Sweden's Ericsson, and other groups are involved as well.

Shaye's Forum may be the smallest cordless phone to date, at 143.5 by 61 by 20 mm.

In the UK, the two cellular-network operators—Racal Telecom plc and Telecom Securicor Cellular Radio Ltd., popularly known as Cellnet—each have about 250,000 subscribers and each is adding about 3,000 a week. The demand, which shows no sign of slackening, has squeezed channel capacity of the analog service in London and other cities, and the operators have responded by shrinking cell size down to 2 km in diameter.

The UK was not involved in the early stages of formulating specifications for the pan-European GSM cellular network. To have a voice in the project, the government and British Telecom gave Plessey plc a contract to carry out a technical evaluation of the seven proposals offered to the GSM standards committee. After Europe adopted the solution proposed by Ericsson in 1988, the UK immediately began implementing it. The new digital services will be run by Cellnet and Racal Telecom. Both have ordered equipment, Racal from Ericsson and UK supplier Orbitel Mobile Communications Ltd, and Cellnet from Motorola.

The big problem now—both in Europe and the UK—is in developing user equipment for the new services. The specification is very complex, including a requirement for a technique that allows the base station to remotely adjust the power output from the users' telephones. This requires the design of some very complex application-specific integrated circuits.

The UK is out in front of the rest of the world in initiating a radio-telephone service that goes one step beyond cellular by shrinking phones down to shirt-pocket size. Known generically as second-generation cordless telephones, the technology associates a telephone number with an individual rather than a fixed location. The same phone will work in the home as a vastly superior replacement for first-generation analog cordless telephones, and as a cordless private-branch-exchange extension at work. The service itself will be known as Telepoint, and the UK Office of Telecommunications said it will award two operators' licenses this month.

Ferranti plc and Shaye Communications Ltd. have both introduced shirt-pocket-sized mobile telephone for the Telepoint market priced at under $300. Both operate over 40 dynamically allocated channels in the 864.1-to-868.1-MHz frequency band. (Conventional cellular service operates in the 900-MHz band in the UK.) Power output is limited, since the phone can work no more than 200 meters from its base station. But with a specified battery life of 50 hours of continuous speech, efficiency has to be high.

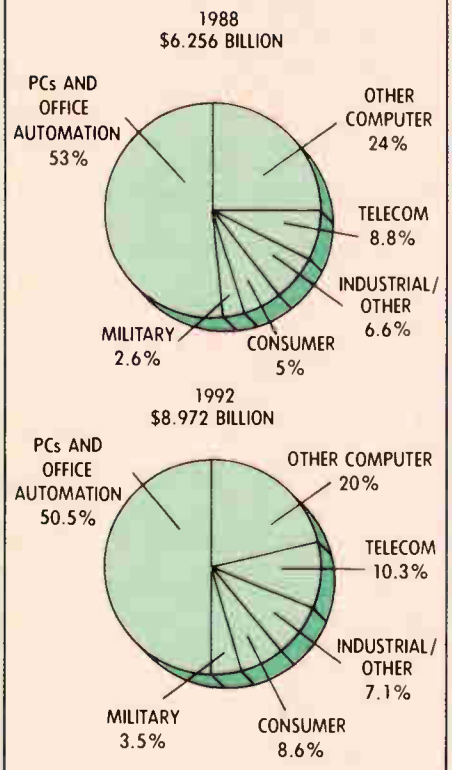
As cellular technology grows, new applications are mushrooming. The first commercially available secure cellular phone hit the market in October 1988. The CVAS III-C from AOE International Inc. of Tucker, Ga., encrypts conversations using the DES encryption algorithm sanctioned by the National Bureau of Standards. Another product—the CVAS III-CE—uses a proprietary algorithm. Both units can operate in either a secure mode or in a "clear" mode when encryption is not required.

Last December, Sungard Recovery Services Inc. in Wayne, Pa., started using cellular phones as part of the disaster-recovery service it offers Fortune 500 companies. The SunNet Cellular V service is more ingenious than it is high-tech, says Jim Domanico, vice president for network products. "Typically, after a fire or other loss of normal telecommunications service, we would have the data-processing operations up and running in a few hours," he says. "But we had a real struggle reestablishing the voice links. Just to get the phone company to install a few extra lines requires 10 hours' notice." SunGard will deliver up to 50 cellular phones to a company that has lost normal phone service. Using AT&T's call-forwarding option, Sungard reroutes to cellular numbers incoming calls to the disaster-struck company.

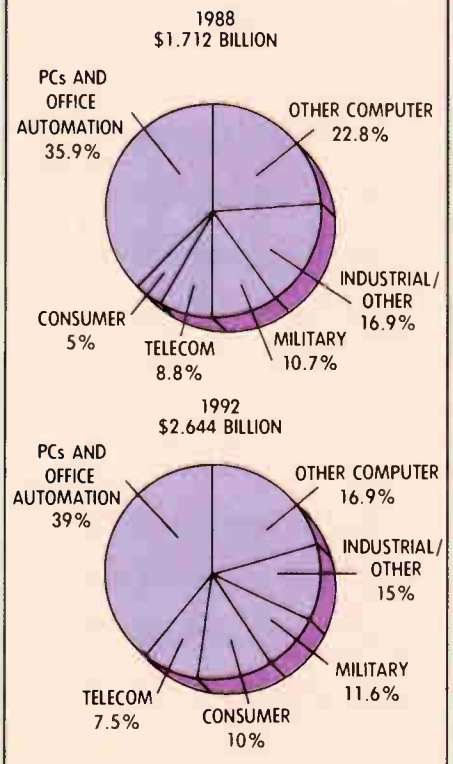
Additional reporting by Peter Fletcher

INDICATORS

WHERE THE DRAMs . . .

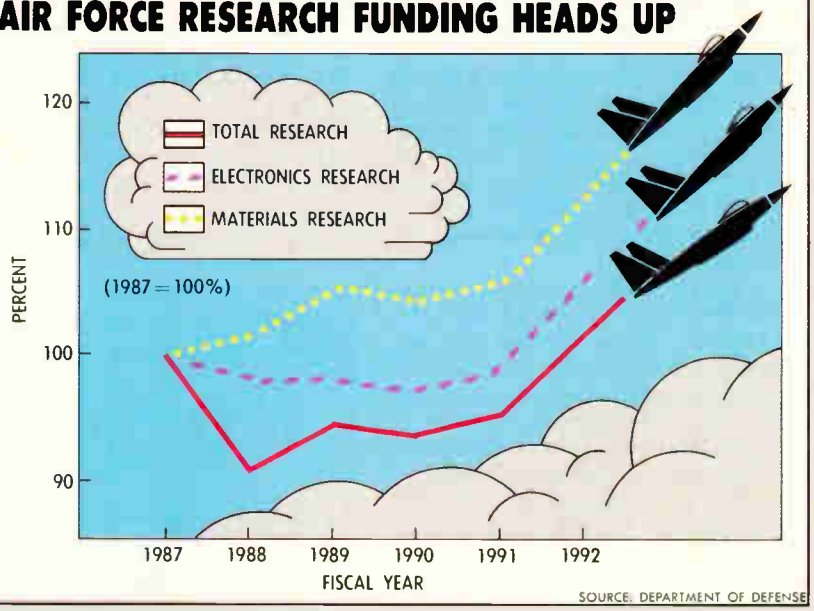


. . . AND SRAMs ARE GOING



SOURCE: HTE RESEARCH INC.

AIR FORCE RESEARCH FUNDING HEADS UP



SOURCE: DEPARTMENT OF DEFENSE

WHERE TO PLAY: THE GROWING MARKETS . . .

Segment	Estimated revenue ($ Billions) 1988	1992	Compound annual growth rate (%)
Processing terminals	0.1	1.0	86.7
Optical-disk drives	0.4	3.0	61.8
Electronic publishing	1.6	6.6	42.2
3- to 4-in. Disk drives	3.7	14.2	39.5
Work stations	1.9	4.8	25.6
Manufacturing networks	0.7	1.7	23.9
LAN connections	2.4	5.4	22.4
Cellular rodio	3.6	7.9	21.9

. . . AND STAY AWAY: THE SHRINKING MARKETS

Segment	Estimated revenue ($ Billions) 1988	1989	Compound annual growth rate (%)
5.25-in. Flexible disk drives	1.3	1.1	(15)
Alphanumeric display terminals	3.0	2.7	(11)
Modems	1.2	1.1	(7)
Line printers	1.4	1.3	(4)
8- to 10.5-in. Rigid disk drives	3.4	2.8	(18)
Electronic typewriters	2.4	2.3	(5)
½-in. Tape drives	2.4	2.3	(2)

SOURCE: DATAQUEST INC.

IF YOU'RE USING THICK-FILM CUSTOM HYBRIDS IN YOUR PRODUCTS, WE'VE GOT A PROPOSITION THAT YOU'LL FIND HARD TO RESIST...

WE'LL STUDY YOUR PRESENT SUPPLIER'S HYBRIDS, AND QUICKLY RETURN WITH:

☐ At least one (and probably several) significant engineering design innovations that will improve reliability/performance, reduce cost, or both.

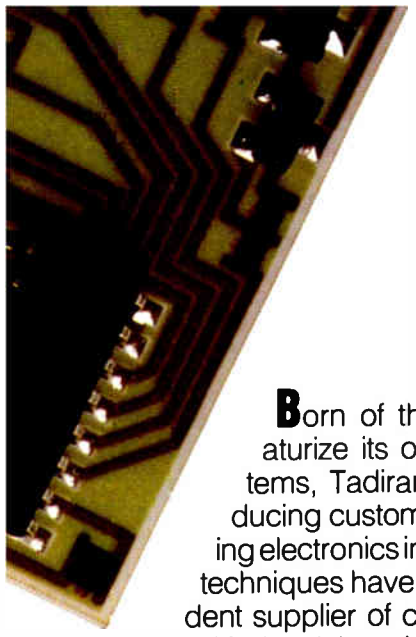
☐ Highest-quality working prototypes for you to test and evaluate.

☐ A production-quantity proposal that will brighten your day.

WE'RE THE HYBRIDS DIVISION OF TADIRAN AND WE WANT TO BECOME YOUR SECOND SOURCE. WHY NOT LET US SHOW YOU? YOU HAVE EVERYTHING TO GAIN.

S. Barkan, Hybrid Product Manager

Call me at 516-621-4980.
It can be the start of a wonderful relationship!



Born of the company's needs to miniaturize its own advanced electronic systems, Tadiran, since 1968, has been producing custom hybrid circuits for a demanding electronics industry. Innovative and proven techniques have made Tadiran a leading indedent supplier of custom hybrids to commercial and industrial markets worldwide.

Tadiran stands for skilled personnel, modern facilities and getting it right the first time. Experience and capability pay off from initial design consultation and fabrication through testing, to packaging and final shipment. Tadiran can offer its customers an outstanding service over a broad spectrum: telecommunications, computers, peripherals, high-tech instrumentation.

Cost effectiveness...when we talk to you, the customer, about circuit design, layout, device selection, packaging and testing, we mean to ensure a final product that meets all your technical requirements. CAD gives maximum flexibility in the initial stages of circuit design and allows easy updating. High accuracy at minimum cost. Tadiran's global purchasing network is the key to multisourcing and low-cost procurement of components.

Our thick-film hybrid circuits reflect state-of-the-art technology, chip and wire or reflow solder. Automatic substrate printers, computer-controlled pick and place, bonding and laser trimming machines all guarantee high reliability even with high-volume production runs. Tadiran also has a pilot line for prototype development, experimentation, fast turnaround of samples and low-volume production.

Tadiran's packaging capabilities include conformal encapsulation, ceramic covers and hermetically-sealed packages. We're now working with chip carrier technology, the latest packaging technique for assembly of high-density modules.

Our record of achievement in the U.S. is impressive, as is our list of long-term customers.

PROFILE OF TADIRAN

Sales

Total Sales	$900 Million
Total Export	50%
U.S. Market	20%

Business Areas

Electronic Systems, Telecommunications, Components	76%
Electro-Optical Systems, Electrical Appliances	24%

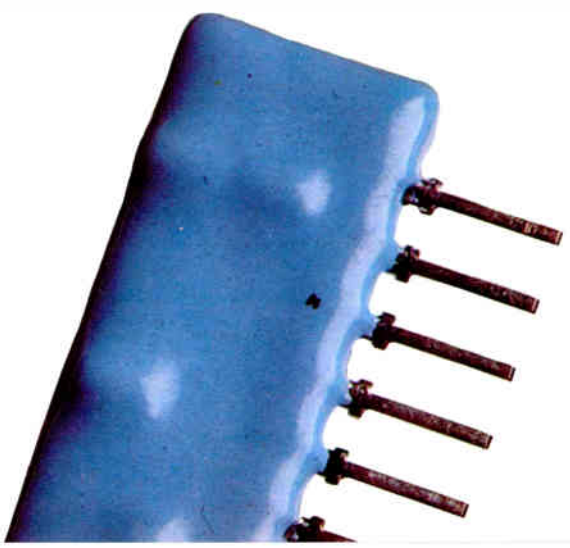
HYBRID DIVISION

History, Overview

- 20 Years in Business
- 15 Million Hybrids in Field, 20% in U.S.
- 30,000 Sq. Ft. Production Area
- Fully-Automated Production Line
- More than 20 Customers in U.S., All Significant Successes.

Excellent Quality: 30 PPM.

- Out of 3 Million Hybrids Delivered to U.S. Market, less than 100 pcs. have been rejected at incoming inspection or in the field.
- CPC (Computerized Process Control) in Manufacturing
- Fully-Automated Production Line
- 100% Temperature Cycling



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BOOK REVIEW

JUST HOW SECURE IS UNIX? YOU'D BE SURPRISED

X/OPEN SECURITY GUIDE
by X/Open Co. Ltd.
Englewood, N. J.: Prentice-Hall Publishing, $29.95

The Unix operating system is often criticized as being inherently insecure, because it is an open system designed to accommodate multiple users. As such, the critics contend, it is poorly suited to commercial applications. But now comes a dissenting view: *The X/Open Security Guide* argues strongly that Unix has a good complement of security features built into it. The book's main purpose is to document those features and provide some guidelines on how to implement them. This makes it a good read for top executives and operations managers who are interested in learning either a little or a lot about their systems' security potential.

Produced by the technical staff of X/Open Co. Ltd., the international organization devoted to creating open computer systems, the *Security Guide* is the very first effort to gather together and carefully spell out the Unix security features. A new edition can be expected when the IEEE, X/Open, and other organizations develop additional standard security features for Unix, which they are now working on.

Separate chapters are devoted to security for users and programmers, but the bulk of the book correctly concentrates on security management and administration—the heart of any computer-system security program. So it's probably most useful to system administrators charged with the responsibility for security.

At 117 pages, the book is not long—and it's easy to read. Security concepts are clearly explained—so clearly, in fact, that at first glance, it may seem too nontechnical. The reader wonders if it goes into enough technical detail. But a closer look dispels this impression. The book appears to provide enough information to show system administrators how they can implement Unix systems that at least are secure enough for many commercial applications.

IN THE SOFTWARE. Much is made of software security; an entire chapter is devoted to describing how Unix provides a great variety of software security features. Among them are authentication, access control, isolation, accountability, privilege, and least privilege. The guide goes on to discuss the relationship of software security to the other forms of security—physical, administrative, personnel, hardware, firmware, and communication security, among others.

The largest single section, chapter six, describes the various actions a system administrator takes to manage the computer securely. The administrator has by far the greatest responsibility for the security of a computer system, so it makes sense to treat his role at length. But doing so makes the other chapters look skimpy by comparison; they leave the reader feeling that perhaps there should have been more on each subject. One is left wondering whether the lapse is because Unix offers so little security, a perception that gnaws away at the book's thesis. A more generous explanation is that not much really needs to be said, because it's so easy to implement the security features that are available.

Which raises another question: even if all the security features documented here are implemented, just how secure is Unix? The guide does not really answer that question. It says only that a computer system using a version of Unix conforming to the X/Open Common Applications Environment recommendations meets most of the requirements of Class C1 (Discretionary Security), as specified in the U. S. Department of Defense publication "Trusted Computing Security Evaluation Criteria," commonly called the Orange Book. The Orange Book classifies computer systems into four divisions: A, B, C, and D, with D the least and A the most secure. Division C has two classes, C1 and C2, with C2 the more secure of the two. So what the guide ends up saying is that Unix systems can qualify for the less secure classification of the next-to-the-lowest division of security, by Pentagon standards. Whether this is enough for any given commercial system is a question left unanswered.

In any case, the book succeeds in its primary aim, as a guide to implementing Unix security. It also reveals the security features built into Unix that many people are unaware of.

The guide also has an extensive index that makes it somewhat useful as a reference work on Unix security features. However, an appendix contains only a few tables of utility programs and files. More of this kind of material would have made the guide more useful as a quick reference. *–Tom Manuel*

AUTOMATING PAPERWORK: A MATTER OF SURVIVAL

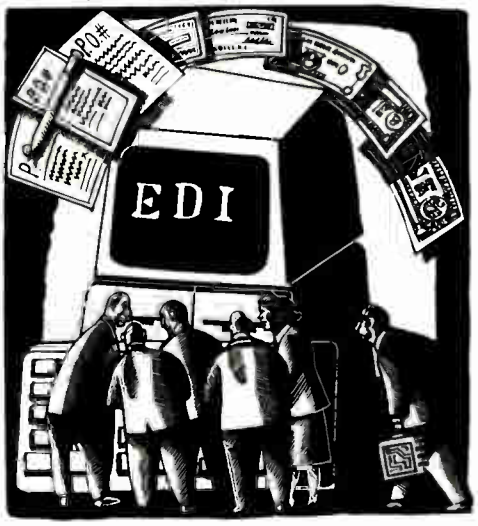
Electronics firms must warm to the 20-year-old idea

The idea is more than 20 years old: automate the purchasing, billing, and shipping processes so that the paperwork of business—purchase orders, bills of lading, and the rest—can be handled by computers instead of people. It saves labor, time, and money; it makes a company more responsive to its customers; and it provides a vital competitive edge.

Such systems are now dramatically changing the way business is done in the U. S. automotive, retail, and apparel industries. But ironically, the electronics industry—the very companies that created the technology to make what is called electronic data interchange (EDI) possible—have been slow to embrace the concept for themselves.

Now that's starting to change. Experts say the companies that don't start investing in EDI today could find themselves short of customers in the 1990s. That's because it is more and more becoming a flat-out requirement for doing business with many major manufacturers. Chrysler, Ford, and General Motors have all warned suppliers that if they aren't equipped with an EDI capability by next summer, their business will no longer be welcome in Detroit. IBM Corp. is driving its top 2,000 vendors, which account for 80% of IBM's worldwide purchases, to obtain EDI capability over the next two years. Dallas-based Texas Instruments Inc., a pioneer in EDI 20 years ago, is shooting to handle 75% of its purchases electronically by 1991. And that's just the tip of the iceberg.

In addition to TI and IBM, companies as diverse as Georgia Power Co. and Levi Strauss & Co. say they can reduce their purchasing cycle by as much as a week or more through EDI. "To become more effective and competitive globally, our members need to learn how to communicate better locally," says John C. Belden, marketing vice president for the American Electronics Association, which is now mounting an EDI thrust. "This is a competitive tool." Belden says the automotive industry has seen the cost of processing a purchase order drop from $55 to $18, and that the same kind of savings can come to electronics companies. "Almost 70% of what comes out of a computer as hard copy ends up getting rekeyed into another computer at its destination," he says. "Imagine the savings if you can eliminate the need to rekey everything."



But the payoffs go beyond clerical savings, says Tony Zerafa, managing director of the Automotive Industry Action Group, an association of automotive companies and their suppliers that was instrumental in the establishment of an EDI standard. "Not only do you eliminate the rekeying of data, the lost-in-the-mail orders, the time it takes for orders to travel through the mails, and all of that labor. In addition, now you have more data, in a standard format, that you can massage and work with for your own specific needs," says Zerafa, who is on loan to the industry group from Chrysler. "So there is not only the savings that are hard and real, but there is also the utilization of the data that can help you to integrate your computer systems."

Yet despite all this action, a recent survey of 1,136 electronics firms by the AEA found that an amazing 48.5% of respondents were entirely unfamiliar with EDI. Only 5.7% said they had such a system in place. So the AEA is trying to do its part to get the industry in gear. In setting up its on-line AEA/Link network (in conjunction with IBM Network Services, which won a contract to handle the program), the AEA made EDI a major priority. "This is a competitive edge we can give ourselves," says Belden. "It's not something we have to go to the government or anyone else for."

EDI capability is rapidly becoming essential to survival for many makers of components and subsystems, Belden says, and executives at the major buying firms agree. Adding to the rapid acceleration in EDI usage, however, are two other factors: the development of industry-standard formats, such as the American National Standards Institute's X12 standard, which was first set in 1984 and is still evolving; and the move toward a unified European market in 1992. "Europe 1992 is really driving this thing," Belden says. Companies all over the world are trying to position themselves to make the best of the powerful European market, and many of them consider EDI a vital tool in helping them match the responsiveness of competitors from overseas.

Even the U. S. Customs Service is involved. Customs already has a system that lets companies obtain export licenses electronically, and it is testing what it calls an Automated Importer Interface with TI and North American Philips Corp. of New York, among others. It plans to implement the interface later this year. This system will help slash the delays caused when Customs wants to review import documents and make an intensive examination, which can take four hours or more and requires paper documents. The new system would use EDI documentation, permitting a swifter review, says Kenneth Shoquist, who manages EDI systems for TI through its Information Systems & Services branch in Dallas. "Half a day is significant," he says. "That's big bucks, even millions of dollars a year, when you look at how it stretches out our cycle times."

With data stored in a common format, purchasing, accounting, manufacturing, and marketing arms can all be tied together electronically. That was an objective at TI from the start, says Shoquist. "We determined early on that we didn't just want EDI to help us out in shipping," he says. TI wanted instead to make EDI a part of a total automation package, so today 75% of TI's freight bills come in electronically

by Tobias Naegele

and are rated, audited, and even paid automatically by a rule-based system. Only if there are problems, such as discrepancies between the bill and an order, does a person have to intervene. "That's where the savings is," Shoquist says.

EDI also promises huge savings in manufacturing and inventory control as a key tool in setting up a just-in-time production facility. "For real just-in-time manufacturing, you can't keep up with paper," says Zarafa of the Automotive Industry Action Group. "You've got to have electronic communications." For example, he says, Chrysler has one plant that broadcasts its production levels daily for its own internal needs and to a nearby seat manufacturer. The seat maker, in turn, delivers only the specified number of seats, in specified styles and colors, and in a specified order, all based on the daily broadcast. Without EDI, the only other way to handle such a task would be by telephone, which costs more and is more likely to cause errors than the EDI message.

And while the technology is not quite there yet, Zarafa and others hold out the hope that EDI may one day be used to help speed development and design as well as manufacturing. The goal is to develop standards and channel capacity so that computer-aided-design equipment and the mechanical drawings that these design systems can produce will also be transmittable electronically. With that advantage, prototypes for subassemblies and components could conceivably be developed much more quickly than is presently possible. "Eventually, EDI will help shrink the development time of a car from the five-to-six-year level to around three years," Zarafa says.

With so much going for it, how has the electronics industry managed to let EDI go by the boards for so long? One major reason is that the purchasing of electronic components and manufacturing of subsystems is generally different from less complex manufacturing jobs such as building automobile seats. Defect rates are higher, purchase quantities are often smaller, and business is conducted differently.

"In the electronics distribution industry, ordering is done primarily over the phone, with buyers asking what's in stock and claiming it directly," says Michael Ribet, an interorganizational systems consultant at IBM's Information Network in Tampa, Fla. (The network is one of several private distribution networks, such as Compuserve, Geisco, and Redinet, that offer EDI services to customers.) "They need a real-time on-line system that can let users call in, check inventory availability, and claim stock automatically. It's a little more complex."

Distributors were, in fact, among the first companies to install automated ordering systems in the early 1970s, but their individual efforts rapidly became a logistical nightmare: their suppliers each had proprietary systems, and so did many of their customers. Distributors often found themselves maintaining 20 or more dedicated terminals. "Everybody found it onerous because of the maintenance problems," Ribet says.

But the distributor problem goes beyond that. The benefits of EDI accrue mainly to suppliers, such as chip makers, and to customers, such as AT&T, IBM, and TI, that process hundreds of purchase orders and checks daily. The small distributor often doesn't have the business incentive to install EDI, says LeRoy W. Luce, marketing manager for national accounts at Automatic Data Processing in Chicago. "The number of customers and suppliers who want to deal with distributors electronically isn't the majority," he says. "You've got to have bottom-line issues such as reduced inventory to convince them to invest money in making EDI work."

WANT TO SEE MODERN MANUFACTURING? HERE'S THE TICKET

Everybody talks about manufacturing as one of the keys to Japanese dominance of many parts of the electronics business. Even so, not everybody has accepted the challenge and converted to the latest fabrication technology. But there is an organization that is determined to smooth the road to modern manufacturing.

Called the Association for Manufacturing Excellence Inc., the four-year-old nonprofit group adds a new wrinkle to the usual methods used by trade associations to educate their members. In addition to meetings and publications, members of AME can sign up for what the group calls workshops, which are actually tours of plants that offer examples of different approaches to manufacturing excellence.

There, members can interview in depth the people at the front lines, those who have actually pushed the state of the art to its limit. And though the AME is not limited to the electronics community, it is heavily slanted in that direction. In fact, the 1988 on-site workshops involved such industry heavyweights as Allen-Bradley, Control Data, Digital Equipment, Hewlett-Packard, IBM, Motorola, Tandem, and Xerox. Likewise, electronics companies are heavily represented on the group's board of directors.

"The mission of our organization is to share experiences in the strategies that give a company a competitive advantage," says Kenneth J. Stork, the association's president and chief executive officer. His full-time job is at Motorola Inc. in Schaumburg, Ill., where he is corporate director of materials and purchasing. "It evolved from an older, narrower organization called the Repetitive Manufacturing Group. In 1981, we visited the Kawasaki motorcycle plant and discovered just-in-time manufacturing," he recalls. "That's when we started to realize that what we needed was a group that provides value for very senior executives. The AME is the result."

In its workshops, the organization tries to give as broad a picture of innovative manufacturing techniques as possible. For example, those conducted last year offered this mix:

- **Statistical process control.** At Allen-Bradley in Milwaukee, a world-class automated assembly plant uses a "scorekeeping" system. At 3,500 points along the the line, the computer-integrated-manufacturing system compares performance of each unit to a statistical norm. Also, the factory has a cellular design where the close proximity of all the functions makes teamwork natural.
- **Team approach.** What Hewlett-Packard Co. labels its Frontier Team has revolutionized computer-terminal manufacturing. Design, operations, purchasing, and marketing personnel crossed lines that had traditionally kept them apart. The result: higher quality and lower costs.
- **Total new approach.** Motorola developed the cellular telephone but found that a dozen competitors were underselling it. So it redesigned its phones for ease of manufacturing, reeducated its employees, and formed partnerships with its suppliers.
- **Competitive benchmarking.** That's how Xerox Corp. won back market share for its copiers. The company developed closer relationships with its suppliers and streamlined its manufacturing by reducing its supplier base from 5,000 to 30.

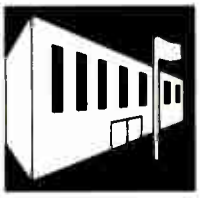
This year, workshops are scheduled to be held at the likes of Compaq Computer in Houston; Motorola in Tempe, Ariz.; and Beckman Instruments in Fullerton, Calif. Meanwhile, the organization is growing fast. "Last year, our membership increased 100%" to 2,500, says Stork. Dues are $100 a year, and the association's address is 380 West Palatine Road, Wheeling, Ill. 60090. *–Howard Wolff*

COMPANIES TO WATCH

TELECOM-VENDOR INFOTRON GOES FOR THE GOLD OVERSEAS

It feels international sales are the ticket to getting back in the black

CHERRY HILL, N. J.



Watching the 1988 Olympics unfold in Seoul, South Korea, reminded the 750 workers at Infotron Systems Corp. of the thrill of victory and the agony of defeat in a very special way. The Cherry Hill, N. J., company's NX4600 Network Exchange was routing the Olympic competition's results to hundreds of terminals manned by officials, sportswriters, and sportscasters. Every score that flashed on the TV screen back home was a victory for a firm that was on the ropes just a year ago.

Though the games have slipped into memory, Infotron is still pursuing the international market strategy symbolized by its Olympic presence. Just as important to Infotron's future, says James Castle, president and chief operating officer, is the company's hunt for strategic technology agreements in the U. S. to assure a timely flow of cutting-edge products.

Over the past four years, Infotron, maker of a wide range of telecommunications networking products, has radically altered the geographical source of its revenue. The percentage of income from abroad has nearly tripled in the three years since 1985, first jumping to 27% in 1986 from 17% in 1985. An even greater gain followed in 1987, when international revenue rose to 43% of the total. Although fourth-quarter results for 1988 are not available, the upswing from foreign sales is expected to level off at about 46%. The firm's domestic and international customer base includes value-added resellers and system integrators as well as large corporations.

Also, the company has managed to close technological gaps in its product line by acquiring systems from smaller companies. The most recent example is an agreement with Licom Inc. of Herndon, Va., that lets Infotron market Licom's 45-Mbit/s T3 multiplexer technology. Also crucial, says Castle, is a joint-development effort with Licom for even higher-speed fiber-optic networking.

The 20-year-old company started its tumble in 1983 when it failed to develop a 1.5-Mbit/s T1 multiplexer—which was the next step in its product cycle, says Castle. As the T1 market exploded over the next five years, the company played catch-up, but badly. Revenue hit a plateau and expenses continued their upward spiral. The result was a $4 million loss in the fourth quarter of 1986, a $3 million loss in the first quarter of 1987, two profitable quarters, and an $8.7 million loss in the last quarter of 1987. Revenue in 1986 was $81 million, and in 1987, $83.3 million.

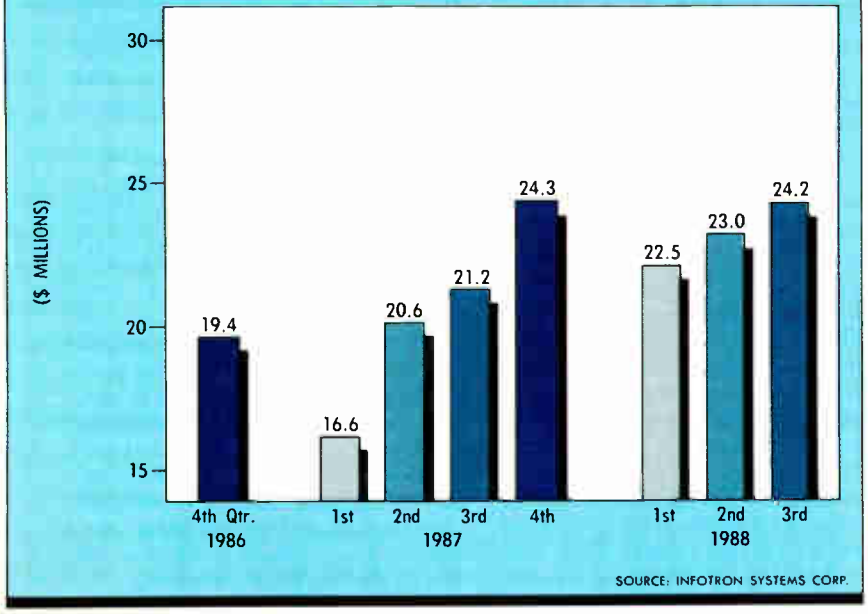
BELT TIGHTENING. Castle came on board in October 1987, just in time to preside over the largest losing quarter in the company's history. Among the new president's first decisions was to have the company take its financial lumps by writing off about $6 million of the value of its investments, which included closing its plant in Ponce, Puerto Rico. He also decided to hire a new management team and replace much of the sales force. The austerity program paid off with net profits in the first three quarters of 1988, when the company earned $859,000, $980,000, and $1.03 million, respectively. The firm expects another strong showing in the fourth quarter, says Castle.

For the time being, at least, Infotron's international strategy hinges heavily on its UK operations. Although it has sales offices or distributors in 57 countries, the UK accounts for about 75% of Infotron's international revenue, says David Barnhill, senior vice president of finance.

"The UK was the biggest data communications market outside the U. S. It was ripe and ready," he says. Although Infotron's NX4600 T1 multiplexer arrived late for the big move to T1 networking in the U. S., it was right on time for the UK and Europe, says Barnhill. U. S.-based competitors such as Timeplex Corp. and NET Inc. did not seize the opportunity abroad and the UK's own major networking companies—Racal and CASE—did not have a T1 product. Nabbing the private-data-network contract for Lloyd's of London gave Infotron high visibility.

Infotron is betting it can repeat its UK success in the rest of Europe. Last November, it announced a joint venture with Secre SA, a $60 million French electronics company, to market Infotron's products

INFOTRON'S UPS AND DOWNS



in France. "By the end of 1989, we will have established at least three more joint ventures abroad, primarily for marketing and sales," says Castle.

Strategic alliances are also key to Infotron's effort to keep pace technologically. By licensing Licom's T3 multiplexer technology and packaging it as the Streamline 45 product, Infotron will soon offer system integrators an intelligent T3 multiplexer with control and configuration functionality.

These capabilities were lacking in the first generation of T3 multiplexers, which were designed for long-distance-carrier corporations and do not require sophisticated network management, says Dan Raup, product-line manager for Streamline 45.

"We are designing the network-management capability that will be integrated with the rest of our product line," he says. The second part of the alliance will lead to fiber-optic networks. *–Jack Shandle*

ISRAELI FIRM BEATS THE BIG BOYS WITH R&D

HACKENSACK, N. J.

When you're competing in a market against companies that are bigger, richer, and better-known, then you had better have something else going for you. The people at IIS Inc. of Hackensack and its parent, Intelligent Information Systems Ltd. of Haifa, Israel, have managed to do just that in their eight years of existence.

IIS makes peripheral and communications equipment to be used with IBM Corp.'s medium and large mainframes. Many of its products wind up on the factory floor, where the company numbers among its competitors such well-established names as Alcatel Courier, Harris, Lee Data, and Memorex Telex. Nevertheless, the company's growth is impressive: IIS officials expect 1988 sales to top $18 million, marking another year of steady growth. In 1987, sales rose about 26% over the 1986 total to reach approximately $13.6 million.

Jacob Herbst, IIS's chairman, president, and chief executive officer, agrees that the numbers are good. "We've had an eight-year record of 20% post-tax profit," says the stocky Israeli. "And we have no debt. I like to think that we have a CFO [chief financial officer] problem: how to invest, not borrow."

Behind IIS's success is an approach that grew out of an analysis made eight years ago by the founders of the company—Herbst and three others who left Israel's Elbit Industries with $30,000 from their pension funds to start a new company. "We entered a market that is now $2 billion annually with products that have a short life—a year to a year and a half," says Herbst. "That means we need substantial R&D to come up with unique features. The products don't have to be innovative—just unique."

At the same time, the standard products cannot be ignored. "We find that in up to 10% of our sales of the special items, the customer also takes some standard products," says Herbst. So it is vital for IIS to continue to invest in research and development to keep that sales mix alive and growing.

That's where IIS has something special going for it. It does its R&D in Israel, spending 8% to 10% of its gross. "It's about a quarter of [R&D costs] in the U. S.," says Herbst, "so that 8% to 10% is the equivalent of 20% in the U. S." What's more, "the cost of living and salaries in Israel are about half" of what they are in the U. S., says Herbst, "and the government gives a 50% R&D subsidy." As a result of these factors, of IIS's 150 employees in Haifa's Technion City, some 40 are engaged in R&D. Its U. S. headquarters in New Jersey handles marketing.

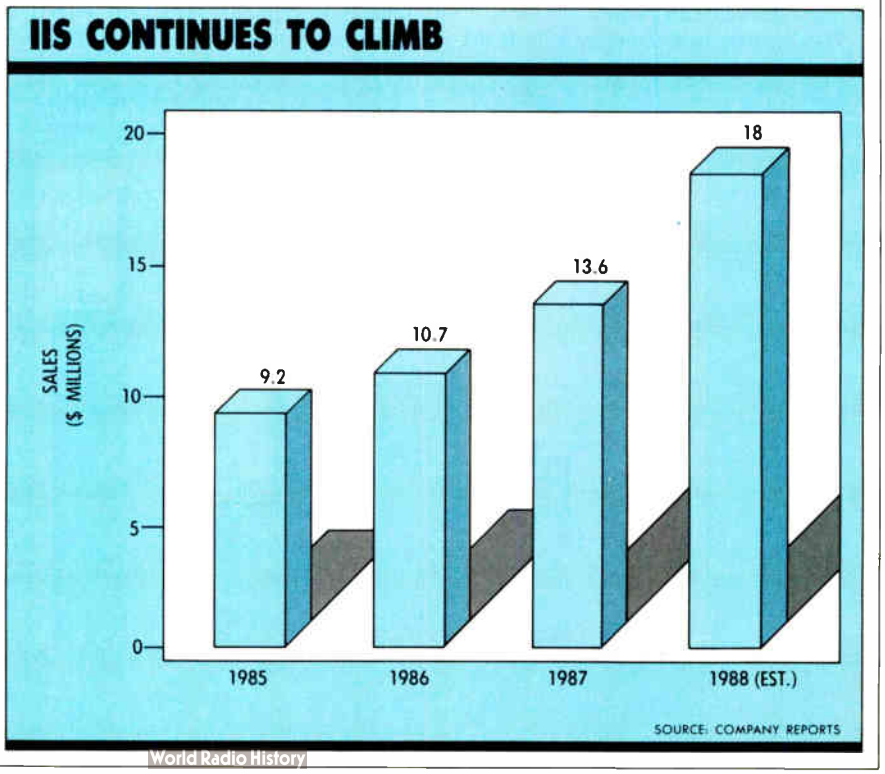
> Intelligent Information Systems scrambles to stay ahead in peripherals

The company splits its market into two parts. In one segment are the standard products, those that are compatible and price-competitive with others in the industry. "These are the follow-the-leader items for which the target is well-known," says Herbst.

In the other group are the special products, those that are unique enough to grab an unassailable market share for IIS. "We make all the mistakes on these, burn our fingers because there are no other fingers to look at," he says. But here, too, there is an advantage to having an Israeli base. "We get beta-test sites and the first customer away from the crowd. We can test in Israel for two years, and no one in the U. S. knows. Our specials are still special after two years."

Among the special items is the shop-floor automation equipment—magnetic stripe readers and printers, and bar-code readers—that can be used by the IBM community with no changes in software. The latest product in this line is a terminal that can read both bar codes and magnetic stripes. IIS sells this gear to customers like Bell Helicopter, Loral, and McDonnell Douglas.

Then there is the peripheral equipment for the AS/400 computer that replaces IBM's System 36 and 38. It's a different product line, with customers, a philosophy, and a marketing approach of its own. The latest in this area is the remote-access module, which takes a local channel through a modem to a remote site. And it does this without architectural



changes. Coming by midyear is an interconnection for IBM Corp. and Digital Equipment Corp. machines that can bridge small and large systems.

IIS also has plans for growth. "We'll accomplish that in two ways," says Herbst. One is by using "the traditional technique of opening more sales offices and adding distributors. We expect this type of growth in 1989 to be 50%." The second method is via mergers and acquisitions. "We're looking at some now," says Herbst, of possible targets.

Will IIS be successful in its quest? Before placing your bet, consider this: the only market in which a competing 3270-peripherals maker outsells IBM is Israel. The competitor is IIS. *–Howard Wolff*

THIS MICROSYSTEM MAKER LIKES ANONYMITY

TORONTO

At first glance, it's just another computer named after a fruit. But first impressions can be deceiving, because in the garden of computer networking systems, Britain's Apricot has some strong roots and it's ready to grow in new soil.

After spending three years developing a North American base in Canada, Apricot is now poised to enter the U. S. Encouraging it considerably is the new trade agreement between Canada and the U. S., which gradually will remove all trade barriers between the two countries over the next 10 years. For companies like Apricot, the treaty is a boon. Most observers agree that the new agreement will make it much easier to enter the U. S. market through Canada. And with a market the size of California or New York State, Canada provides a near-perfect testing ground for a U. S. strategy.

But Apricot's British executives began plotting their entry into North America three years ago, well before the trade deal was drafted. "Our plan was to establish a strong beachhead in Canada and then enter the United States," says Gerald Sumner, president of Apricot in Canada (AIC) Computers Inc. "Free trade is a bonus; it makes it all easier."

The privately held company sells its networking-oriented computers exclusively through value-added resellers (VARs), and this is the key to its marketing strategy. "It's a solution approach vs. a box-buying approach," says Sumner. "We're looking for quality distribution, not quantity."

As far as Sumner knows, Apricot is the only computer company in North America to focus solely on VARs. And judging from its growth, the strategy is a wise one. The company entered the Canadian market very cautiously in 1986. Today, it has some 70 Canadian VARs (it plans to limit the number to 100). Sales are expanding between 10% and 20% a month. They're expected to multiply three to four times this year, double in 1990, and grow 30% to 40% annually from there on.

> The UK's Apricot plans a big role in the U. S., but only through VARs

The U. S. debut is also very cautious. Apricot expects to sign up 30 U. S. VARs this year, another 40 in 1990, and reach 200 by 1991. And that's where the growth stops. Says Sumner: "It's more effective to do business with smaller groups of people and do more business with them."

The company doesn't force VARs to carry its line exclusively, but finds they often do. "We can give them an equivalent system for substantially less money," says Sumner. Besides, "most VARs get poor support from [other] manufacturers, because those manufacturers have multiple channels of distribution," he says.

At the Canadian Computer Show in Toronto last November, the Apricot exhibit featured booths for no less than 14 VARs. They were displaying Apricot's 1989 product line, the machines that will move the company into the U. S.

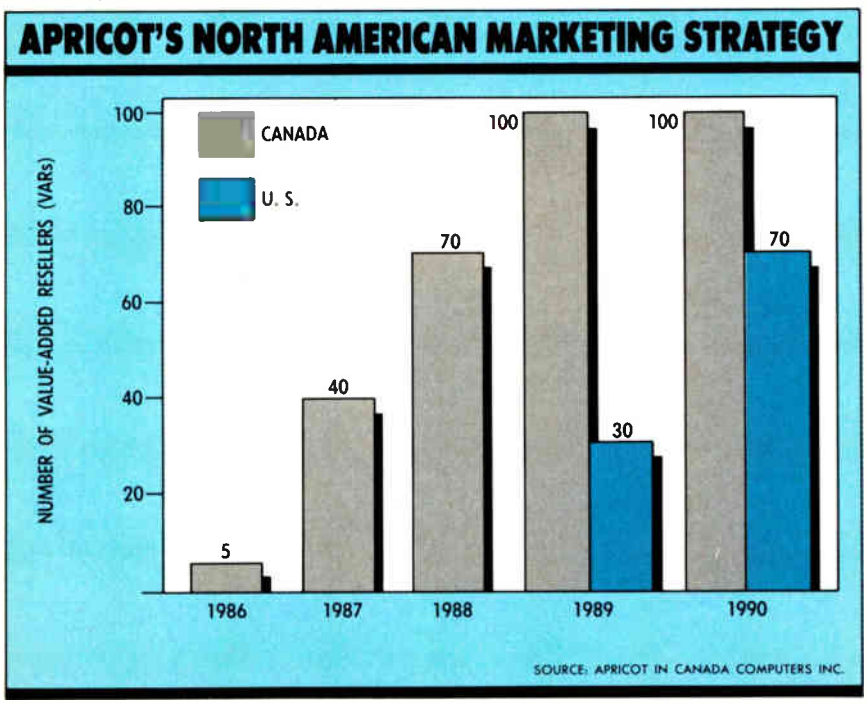
Apricot offers three ranges of products, all 80386-based. The entry-level XEN-i range operates at 16 MHz with 1 Mbyte of memory. With an AT bus architecture, it's designed for work stations in an IBM OS/2 or DOS environment. Serial, parallel, and Ethernet ports are on the motherboard. And it's a pretty cost-effective machine, listing at $2,500 to $3,500.

Apricot also provides high-performance desktops, known as the Qi (pronounced "key") series and boasting a Micro Channel architecture. And though it uses the Chips & Technologies chip set (which come with an IBM Corp. license), it takes IBM's Personal System/2 a few steps further. Qi machines offer not only parallel and mouse ports on the motherboard, but also an Ethernet port, dual asynchronous communication channels, security processors, and a VGA graphics controller. Drives range from a single floppy to a 120-Mbyte hard disk. The list price for all this is still relatively low at $3,695 to $7,995.

While the Qi line has boosted Apricot's reputation in England and Canada, the company has even higher hopes for its new VX 2000 Mini series, which it touts as an industry-standard minicomputer. Operating at 25 MHz, the VX 1000 Mini is a central server in an MS-DOS or OS/2 network. The heart of the system is an MCA Small Computer Systems Interface card with a 128-Kbyte buffer. The VX 1000 offers up to 4 Gbytes of storage with access times of 16 ms. The system will ultimately be upgradable to 80486 technology.

Says Sumner: "We've taken micro-based technology into the mini performance world, utilizing high-performance Small Computer Systems Interface controllers, high-performance drives, and tape backups."

The VX 1000, says Sumner, provides



equivalent performance to systems by IBM and Digital Equipment Corp. for about one third the cost. It lists between $15,000 and $22,000.

Even at such low prices, Apricot has its work cut out for it. Despite its high-profile marketing, the company is still relatively unknown in Canada. "In terms of unit shipments, Apricot is not one of the top five or six players," says Shelley Burke, a senior research analyst with International Data Corp.'s office in Toronto. Burke says one of the reasons for this is that the company's products are still relatively new. But she admits the potential to gather a bigger share is there.

Apricot manufactures its hardware in Scotland, but the company intends to open a North American assembly plant. That's an indication that it plans to be around for a long time. *–Rick Kuwayti*

SHED NO TEARS FOR MINISUPER-MAKER MULTIFLOW

BRANFORD, CONN.

If you've had the impression that Convex Computer Corp. of Richardson, Texas, has steamrollered all of its minisupercomputer competitors, look again. Multiflow Computer Inc. is not among the casualties. The company is rolling right along, its principals say, partly because its systems shine in market segments where Convex offerings don't.

Only a year and a half after shipping its first machine, Multiflow has now installed more than 70 parallel-computer systems, says Donald Eckdahl, president and chief executive officer of the Branford company. And this month the firm is getting set to roll out its second generation of very-long-instruction-word machines. The new line will boost computation and input/output performance by more than a factor of four, says Eckdahl, while holding the line in terms of price/performance ratio.

Proving that a startup is not a one-act show is important, and that's one thing the new products will do, says Jeffrey Canin, senior technology analyst for Hambricht & Quist Inc. in San Francisco. The announcements will catch the attention of the financial community, he says. Thanks to the Convex juggernaut, most analysts are now skeptical about the future of companies relying on minisupercomputer products, he says.

BALANCE SHEET. Luckily for Multiflow, the firm does not have to struggle to turn that attitude around. Full financial data is not available on the closely held company, but "as I understand it, Multiflow's balance sheet is quite comfortable, and they're not in any immediate need of financing," says Canin.

The new machines will extend the upgrade path Multiflow can offer to users of Digital Equipment Corp.'s VAX systems, among others. The unique Multiflow advantage is its combination of trace-scheduling, compacting-compiler software, and the very-long-instruction-word hardware, a mix that brings parallel-processing elements to bear on existing software without any need for retuning programs or adding statements to aid a parallelizing compiler. Customers can simply recompile and run, thereby obtaining what Eckdahl calls "the best time to performance" of any minisupercomputer. There are a great many potential customers, he says, who are either unable or unwilling to fiddle with their software.

Multiflow president Donald Eckdahl (left) and executive vice president Joseph Fisher will unleash this month new Trace computers that boost performance as much as fourfold.

The computers of Multiflow's current line, called the Trace/200, perform up to 14 operations concurrently. The compilers look for parallelisms inherent in ordinary serial code and common scalar routines, whereas most parallel systems only really get to work when a loop or some kind of vector or array operation is executed. Thus, Eckdahl argues, the systems are far more "general purpose" than most parallel machines, which tend to be most useful in scientific and technical applications. Indeed, some 70% of Multiflow's systems have gone to commercial customers, rather than universities or research institutions.

The second-generation systems will demonstrate how this basic technology can be built upon. "Enhancements have boosted Trace performance to the point where we compete in some applications with enterprise-wide supercomputers like the Cray X/MP-14 in performance, for a fraction of the cost," claims Eckdahl.

And the technology has a long lifetime of performance upgrades ahead of it, says Joseph (Josh) Fisher, executive vice president and one of Multiflow's founders. For example, Multiflow's systems are built with conservative CMOS chip technology. So there are obvious ways to increase speed by moving to more aggressive processes. Compiler improvements have been steady, too.

Multiflow foresees a large potential market-growth path. Its systems compete directly with those from Convex and other minisupercomputer makers, but they also suit users who would be very unlikely to buy a Convex or other parallel system because of the software hassle. Getting software to work efficiently on a parallel computer can be a lot of work, says Fisher, and any time a trusty old program is messed with, a new raft of bugs is bound to invade it.

Canin of Hambricht & Quist feels that Multiflow's ability to differentiate itself from other minisupercomputer vendors is vital to its marketing strategy. In effect, it is positioning itself instead against DEC, Hewlett-Packard, and IBM. Against them it can claim a substantial price/performance advantage, he says, until the time when it grows large enough so that they feel compelled to react. People base their buying decisions on more than price/performance, Canin says; "but Multiflow has been building an impressive list of customers." *–Jeremy Young*

PEOPLE TO WATCH

IS ROCKWELL'S BOWEN THE NEW LOOK IN SEMICONDUCTOR EXECUTIVES?

What he brings to the party is expertise in the semiconductor-equipment field

NEWPORT BEACH, CALIF.

When they named James D. Bowen to head their Semiconductor Products Division, the people at Rockwell International Corp. departed from the accepted way of doing such things in the chip business. And in the process, they just may have started something. Bowen, whose title is vice president and general manager, has a background that is firmly rooted in the semiconductor-equipment field—not the device side, from which the top chip managers usually hail.

But the choice is no anomaly, says one industry watcher. "It is the beginning of a trend," declares Jerry D. Hutcheson, president of VLSI Research Inc. of San Jose, Calif., which watches the chip-equipment industry. He reasons that executive expertise in manufacturing advances is what U. S. semiconductor makers lacked during the past decade as they steadily lost ground to Japanese rivals. "Expect to see a strong movement of experienced equipment people back into chips," Hutcheson predicts.

Bowen's experience fills the bill perfectly, running the gamut from work with testers to fabrication gear. Now 58, he was head man during the big growth period of the late 1970s at Fairchild Camera & Instrument Corp.'s Century tester operation. And from 1980 to 1986 he held top posts at Eaton Corp.'s Semiconductor Equipment Group. In Hutcheson's words, "he's done it all."

NO LINE. Bowen himself believes that if a clear boundary ever existed between expertise in chips and in equipment, renewed emphasis on efficient production methods has dissolved it. In fact, the interaction between new production equipment with submicron precision and the silicon components necessary to build it means "a lot of similarities between test equipment and what we are trying to do here," he says.

Bowen was hand-picked by his boss at Rockwell, Gilbert F. Amelio, who was promoted to president of the realigned Rockwell Communication Systems Group last year. From 1983, Amelio ran the chip division, which is now part of that group [*Electronics*, August 1988, p. 117], transforming it from a marginal supplier of a range of silicon products into a unit tightly focused on telecommunication chips, boards, and systems. Along the way the division established a most profitable niche: it now supplies the bulk of modems for world facsimile production, primarily to the Japanese companies that dominate fax. Rockwell does not disclose division results, but industry sources say 30% to 40% growth rates have propelled annual sales to around $300 million.

By any standard, Bowen is stepping up to the helm of a very healthy operation. "For the first time ever, I have the luxury of planning," he says. Among his duties will be guiding Rockwell's move over the next year or so into submicron densities and 6-in. wafers, tough advances to manage anywhere. He'll also find ample challenge in Rockwell's telecom businesses.

For example, fax manufacturers seek to penetrate the OEM market for home machines, and they will need more affordable chips to do that. And the firm is looking ahead to color machines for which modems must be developed. These will require improved modem chips and

If there was a line between IC and equipment expertise, it's been eliminated by a renewed stress on efficient production methods, says Rockwell's new chip boss, James D. Bowen.

boards, with such features as data and video compression and better error-correction methods. All need complex software, which today is a problem for chip makers as well as their customers.

In fact, it is this steady growth into equipment-level sophistication that makes the semiconductor label misleading, Bowen says: "The way I see it, it's a misnomer. We're in the systems business, with semiconductor capability."

An evolution into the systems end of the business is the all-important goal for smart chip companies, Bowen adds. That's because any technological edge, no matter how secure at the moment—Rockwell's chip niche in modems, for example—presents a target for competitors. "In high technology," he says, "it's hard for a company to keep a lead for more than 10 years." *–Larry Waller*

AT&T'S HYTHA IS READY TO SELL CHIPS IN JAPAN

TOKYO

For David A. Hytha, the long wait is over. After 2½ years of circulating samples of devices from AT&T Microelectronics in Japan, Hytha is officially in business as managing director of its Japanese unit. And if he had any illusions about the road ahead, the shakedown period has removed them.

"This is a very tough market," he says, "but AT&T has one big advantage over most other companies. Market access is much easier than for a small company whose name is not known. All the engineers in our target markets know us. They also know what our systems are capable of, because they monitor us for competitiveness."

AT&T has an advantage in Japan, says David A. Hytha, the head of AT&T Microelectronics Japan—name recognition.

Moreover, Hytha says, "our semiconductor business is easier than many systems businesses. There is a customer base of about 30 data-communications and telecommunications firms, rather than 1,000, for our high-end semiconductors. We are not selling, for example, into consumer or automotive markets." Hytha predicts that by 1993 he will be running a $100 million business in Japan. But AT&T will leave direct sales to Japanese trading firms. It will provide business development, technical product support, field application engineering, and the design lab.

Hytha says it is crucial for AT&T that the Japanese subsidiary include a lab and design facilities from the beginning—the first time that an AT&T Bell Laboratories product-design organization will be located in a foreign country. The Sun Microsystems 3/60 work stations for front-end design will be installed in April; back-end design will be done in Allentown, Pa.

Hytha points to another first. He says that AT&T Microelectronics is the first AT&T group to be divided into strategic business units. That way, Bell Laboratories' resources are put to work developing new products while local autonomy is enhanced. Headquarters' technology is provided to the customer but the local units do not have to go to headquarters for everything.

In addition to getting his devices around to Japanese companies, Hytha has spent his 2½ years of preliminary work for AT&T Microelectronics Japan hiring and training staff. He now has 15 people but expects to increase that number to 50 by the end of 1989 and to 100 by the beginning of 1991. In the spring, his expatriate staff of designers will be up to seven, but a year later it will be down to three or four as the company builds the Japanese staff.

Hytha expects to work himself out of a job by the mid-1990s and be replaced by a Japanese executive. But it won't be the first time he's done so since he came to AT&T. He says that he has been involved in some way in six of the seven ventures that AT&T now has in Japan—in fact, he started when there was one person in Japan and one in the U. S. running the operation; he was the one in the U. S.

Hytha moved to AT&T Microelectronics in 1985 after joining AT&T in 1982 to do financial analysis in its new investments department. In 1983 he played a role in AT&T's purchase of a share of Ing. C. Olivetti & Co. SpA, Ivrea, Italy, as well as in a joint venture with Philips International NV of the Netherlands.

But most of Hytha's career has had an Asian backdrop. After getting a political science degree from the College of the Holy Cross in Worcester, Mass., he worked on cultural and trade exchange programs for the Asia Society.

In 1980 he went to New York to get his MBA from Columbia, specializing in operations research and operations management, with particular interest in statistics, quality control, and consumer-behavior patterns. "These studies, especially my knowledge of quality control and statistics—and being in the right place at the right time—got me my position as head of AT&T Microelectronics Japan," Hytha says. *–Charles L. Cohen*

COMMODITIES MAN JOHNSON MOVES OVER TO ASICs

SANTA CLARA, CALIF.

You wouldn't ordinarily ask a veteran of the memory business to run your application-specific integrated circuit operation. After all, memories are commodity items and ASICs are just the opposite. But Robert Johnson is out to show that such reasoning is specious.

Johnson is the new vice president in charge of the ASIC division at National Semiconductor Corp. in Santa Clara. A 10-year man at National, he has moved over from his post as vice president of the memory division. He replaces Lanny Ross, one of the last upper-level management holdovers from the Fairchild Semiconductor acquisition, who has joined Pittsburgh, Pa.-based Rockwell International Corp.

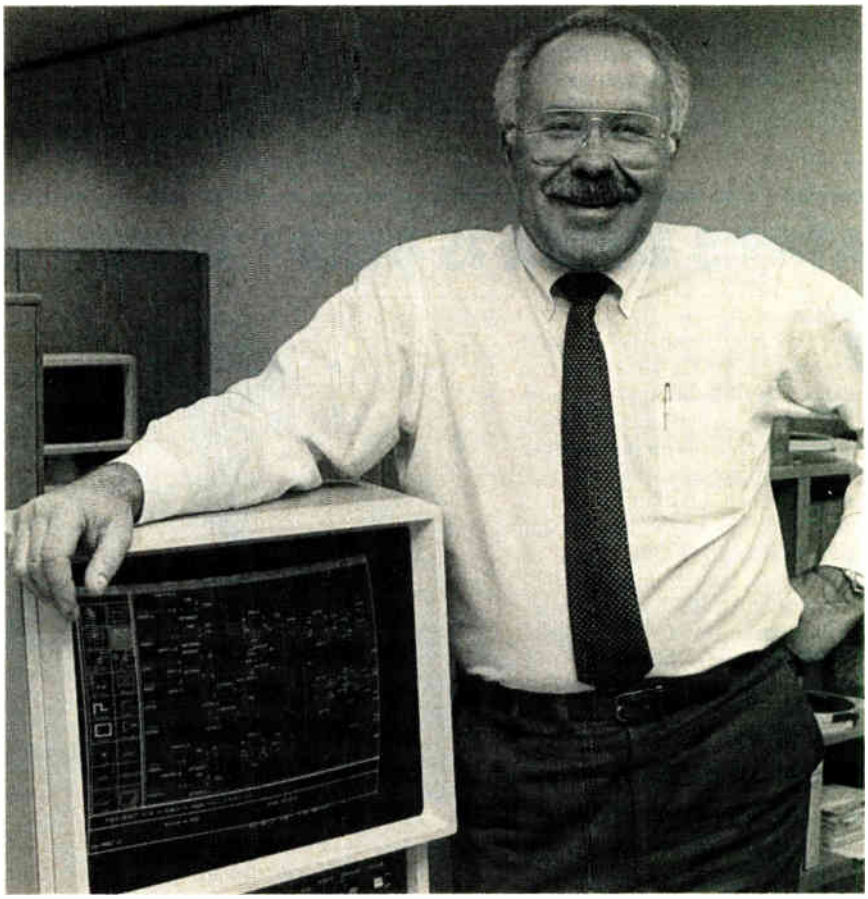
The 50-year-old Johnson, who holds a BSEE from Oregon State University, says that the move from memory to ASICs is not as incongruous as it sounds. In fact, he says, there are more similarities than might be immediately apparent, especially at the operations level. On the memory side, he says, three things are important if one expects to survive, especially in the commodity-device environment: inventory, costs, and competition.

"In some aspects of the ASIC business, especially gate arrays, the only way to survive is to view it as a commodity business," says Johnson. "The Japanese do.

And we must, if we expect to compete head to head with them on a cost and performance basis." At the same time, it is necessary to apply technology innovation selectively, using it where it results in greater performance that can be translated into higher margins.

This requires a balanced product offensive. "In memory, what I tried to do is develop a good commodity thrust, but at the same time develop a high-performance segment that was somewhat countercyclical to it," he says. And so National has built up a good commodity business in low-density erasable programmable read-only memories, he says. And with the acquisition of high-speed CMOS, biCMOS, and emitter-coupled-logic technology from Fairchild, the company has achieved a good position at the high-performance end. A counterbalance between the two, he says, is the company's medium-to-high-speed electrically erasable programmable ROM business.

In ASICs, he sees a similar strategy evolving. In CMOS gate arrays, says Johnson, National has established a leadership position in the low-density segment, making use of its manufacturing expertise to keep production costs down. And with the acquisition of Fairchild's Aspect bipolar process, the company is a technology leader at the high-performance end. That leaves Johnson's ASIC charter a simple one, he says: to beef up the middle. *–Bernard C. Cole*



Robert Johnson, National's new ASIC chief, maintains that there are more similarities between the memory and the ASIC businesses than meet the eye.

THIELS AND STEPHANSEN CATCH THE SPIRIT

SUNNYVALE, CALIF.

Two veterans of Silicon Valley have caught the entrepreneurial spirit at a Sunnyvale, Calif., startup, Integrated CMOS Systems Inc. They have left their old-guard semiconductor companies to join an upstart enterprise.

Roy P. Thiels quit his post as general manager of the $60 million application-specific integrated circuit business at National Semiconductor Corp. in Santa Clara, Calif., to become executive vice president at Integrated CMOS. And Steve Stephansen walked away from his position as director of sales at Advanced Micro Devices Inc. in Sunnyvale to become vice president of sales.

Thiels, 51, says, "I was impressed with the component- and system-level design tools" at Integrated CMOS, which he had come to know while still at National. The two companies had been working together in a marketing initiative to pursue major U. S. customers. Thiels says Integrated CMOS has solved the problem of cost-effectively testing complex ASIC chips using an automatic scan-test insertion tool [*Electronics*, September 1988, p. 92].

For Stephansen, 33, what clinched it was Integrated CMOS's logic synthesizer. "Their logic-synthesis tools are far and away the best of any company in the market," he says.

Another factor that attracted both men was the company's engineering and management staff, industry veterans who gravitated to the new company in pairs or in groups. Stephansen says the Integrated CMOS brain trust hails from IBM, Amdahl, and Storage Technology. "When a group of guys stays together as long as these characters have, they have to have learned something," Thiels adds.

Both men point to the customer base as another lure. Though the number of customers is limited, Stephansen says the roster includes such heavy hitters as Apollo Computer, which used Integrated CMOS tools to design its DN10000 work station. "These companies have tremendous resources at their disposal and can get the attention of any ASIC vendor," he says. "For them to choose Integrated CMOS speaks well of the company."

Thiels explains his new role this way: "Lin Wu [president and chief executive officer] wanted someone to assist him as the company grew into its manufacturing phase—it had been largely in a design phase up to now. He needed someone to help manage the engineering, marketing, and manufacturing. He and I will work together as a team. I know a lot about component design as well as manufacture and costing. I think I will fit in well."

Thiels also will help increase the volume of the business. "We're looking at doubling the size of the business in the next year," he says. At the end of the last fiscal year in September, the company had $6 million in revenue for the last six months of the year, which is an annualized run rate of $15 million.

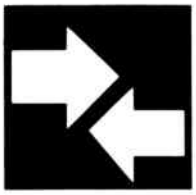
That meshes with Stephansen's tasks. First, his job is to expand the customer base. "We plan to concentrate on customers concerned with high-performance designs, that need a fast time-to-market and do not want multiple design iterations to get a final part," he says.

Also, he must boost the company's recognition in the marketplace. "The company has not done enough to get its message to the public: its view of the gate-array business, where the ASIC market is going, and so on," Stephansen says. "I plan to change that." *–Jonah McLeod*

READER'S REPORT

We were first

To the editor: You erred in "Orcad's PC design tool puts complex functions in reach" [*Electronics*, November 1988, p. 132], which states that Orcad/PLD is the "first to offer high-level descriptions of complex logic elements" on a PC. Data I/O's ABEL, the de facto industry standard in PLD design software, was introduced in 1984 and our Gates product in 1986. Both were available on the PC and both offer higher-level descriptions of PLDs that are equivalent to computer programming languages like Basic or C. On the other hand, Orcad/PLD's method of entry (indexed and Boolean equations) is equivalent to writing software code in assembly language.



The article states that currently available PLD tools "generally lack the power to handle more than one PLD at a time, and most cannot handle a mixture of PLDs and other types of logic." It also says that the "designer can create his design without considering the particular PLD structure in which it will be located."

While ABEL is a PLD design tool for single PLDs, Gates is a tool for multiple PLD designs. Both can handle complex and irregular (glue) logic designs, and both allow designers to input their designs without specifying either the PLD structure or the technology to implement their designs.

Kyu Lee
Data I/O Corp.
Richmond, Wash.

HDTV standard? Forget it!

To the editor: Re. "The FCC won't allocate new spectrum for advanced TV broadcasts . . ." [*Electronics*, October 1988, p. 61]: here we go again, stuck with an inferior system because the "powers" (FCC and industry?) want compatibility. We got stuck with NTSC when those same powers forced compatibility at the beginning of color TV—both PAL and Secam present superior video. Then we had to wait for stereo and MTS audio for TV because they argued over the method.

I vote for full HDTV! Why should we Americans again be stuck with second- or third-best quality, while the Japanese laugh at our bureaucracy?

Eugene B. Simmons Jr.
Harvest, Ala.

Addendum

Important contributions to the 1989 World Market Forecast came from Instat Inc., Scottsdale, Ariz. The company's name was left off the list of credits on p. 57 of the January issue.

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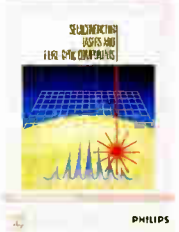

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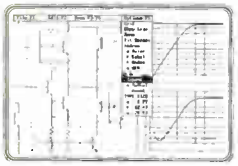

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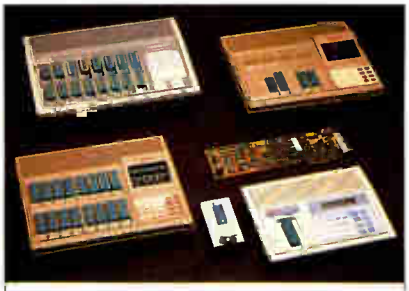

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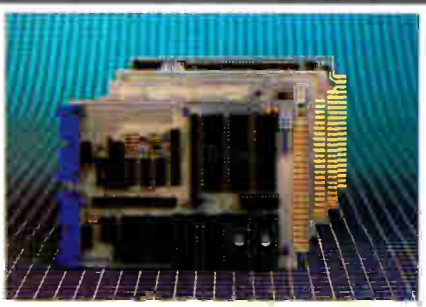

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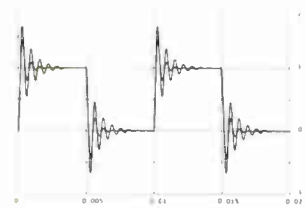

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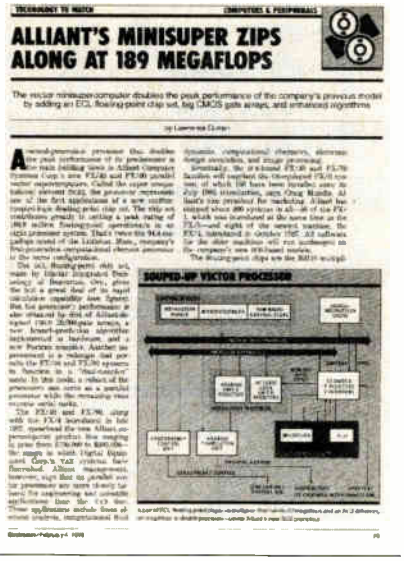
UPDATE: DESPITE LOSSES, ALLIANT HAS A WINNER

The two parallel-vector minisupercomputers Alliant Computer Systems Corp. introduced a year ago [*Electronics*, Feb. 4, 1988, p. 89] are a hit, say executives at the Littleton, Mass., firm. And that's good news, since Alliant is sailing some heavy financial seas.

The FX/40 and FX/80 "have been successful in doing precisely what we said they would do—giving customers the added value of parallel computing at a very competitive price," in the words of Craig Mundie, vice president for research and development at Alliant. Mundie won't reveal how many of the machines have been shipped, but the company does say they now account for roughly half of its revenue.

Still, the increase in revenue hasn't translated into profits. Final figures for fiscal 1988 are not tallied yet, but Alliant lost money in the second and third quarters. It expects to post a loss in the fourth quarter too.

Alliant's slowdown is primarily based on two factors, says president Ronald Gruner. The first is an erosion in profit margins due to intense competition in the minisupercomputer market. The second is the cost of assimilating last year's acquisition of Raster Technologies, a supplier of high-performance three-dimensional graphics displays.


ALLIANT'S MINISUPER ZIPS ALONG AT 189 MEGAFLOPS

The vector minisupercomputer doubles the peak performance of the company's previous model by adding an ECL floating-point chip set, big CMOS gate arrays, and enhanced algorithms

SOUPED-UP VECTOR PROCESSOR

The VFX mixes 3-d graphics with computation-intensive applications

Price erosion has indeed battered profits in the minisupercomputer market, says Jennifer Johnson, senior analyst for technical computing at International Data Corp. in Framingham, Mass. But she also thinks Alliant needs to develop a clearer market focus to overcome its slowdown. She points out that Alliant isn't a leader in any of the top four application segments International Data identifies: design engineering and analysis, scientific research, classified defense, and biological and chemical engineering. "Alliant needs to pick a market segment and go after it like gangbusters. They're developing a plan, but they need to be more vocal about it," she says.

Just what is that plan? "We're now focusing on four applications that take best advantage of our technology: chemistry, VLSI design, mechanical design, and simulation control," says an Alliant spokesperson, who agrees that the company has heretofore lacked this kind of sharp market focus.

Meanwhile, Alliant laid off 75 employees early last month and took an as yet undisclosed charge against first-quarter earnings for that move, which is intended to cut annual costs by some $20 million. Mundie says the layoff represented "the second wave of digesting the merger" between Alliant and Raster.

The merger is already paying off, in the form of the VFX—or Visualization series of visual supercomputers—machines that excel at graphics and imaging work. Introduced last August, the systems combine simultaneous computation-intensive applications and high-performance 3-d graphics, Alliant says.

The Visualization series incorporates the FX/40 and FX/80 vector processor and Raster's 3-d graphics displays. Prices for multiuser VFX systems range from $75,000 to $125,000 per user. The low end of that range puts Alliant well below the $90,000 to $100,000 starting price of available visual supercomputers.

The extension of the FX/40-FX/80 technology into the Visualization series indicates how pivotal the technology is to Alliant's future products. The main difference between the 40 and the 80 is the number of vector processors included: a maximum of four in the 40 and up to eight in the 80. Fundamental to their technology is a second-generation processor called the supercomputer element, or SCE, which was one of the first products to use an emitter-coupled-logic floating-point chip set from Bipolar Integrated Technology Inc. in Beaverton, Ore. BIT's chips make the biggest contribution toward enabling the SCE to deliver 188.8 million floating-point operations/s in an eight-processor configuration. That doubles the 94.4 megaflops of Alliant's first-generation eight-processor system in a similar configuration.

Other reasons for the SCE's heady performance are Alliant-designed 20,000-gate arrays in CMOS; a revised hardware-based branch-prediction algorithm; and a Fortran compiler. Both the branch-prediction algorithm and Fortran compiler were new for the SCE. The Fortran compiler—version 4.0 of Alliant's own FX/Fortran compiler—employs a register-allocation algorithm that uses the new hardware more efficiently. The FX/40 and FX/80 will eventually replace the earlier FX/8, more than 150 of which have been installed. Moreover, Mundie says that so far in each quarter since the new systems have been shipping, more units have been sold to new customers than to existing customers. There haven't been any surprises in how the systems are being used, he adds. Their applications range from finite-element analysis to computational fluid dynamics and computational chemistry.

Mundie expects Alliant to regain momentum as customers seek higher performance. "A lot of budget dollars were siphoned out of the high-performance market into desktop systems," he says. "Now people are finding they need higher performance, and the pendulum is beginning to swing back." *–Lawrence Curran*

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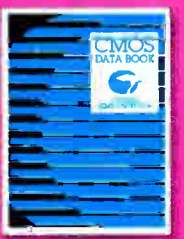

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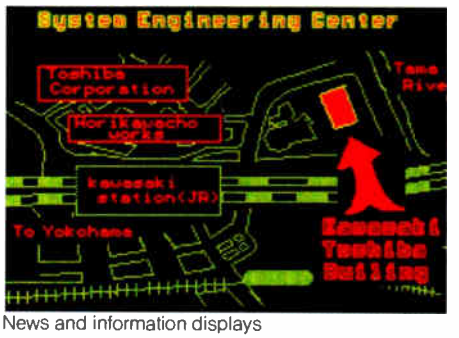

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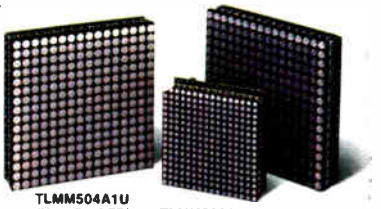

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