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A VNU PUBLICATION

Electronics

MAY 12, 1988

PROGRAMMABLE LOGIC DEVICES:

THE SECOND GENERATION

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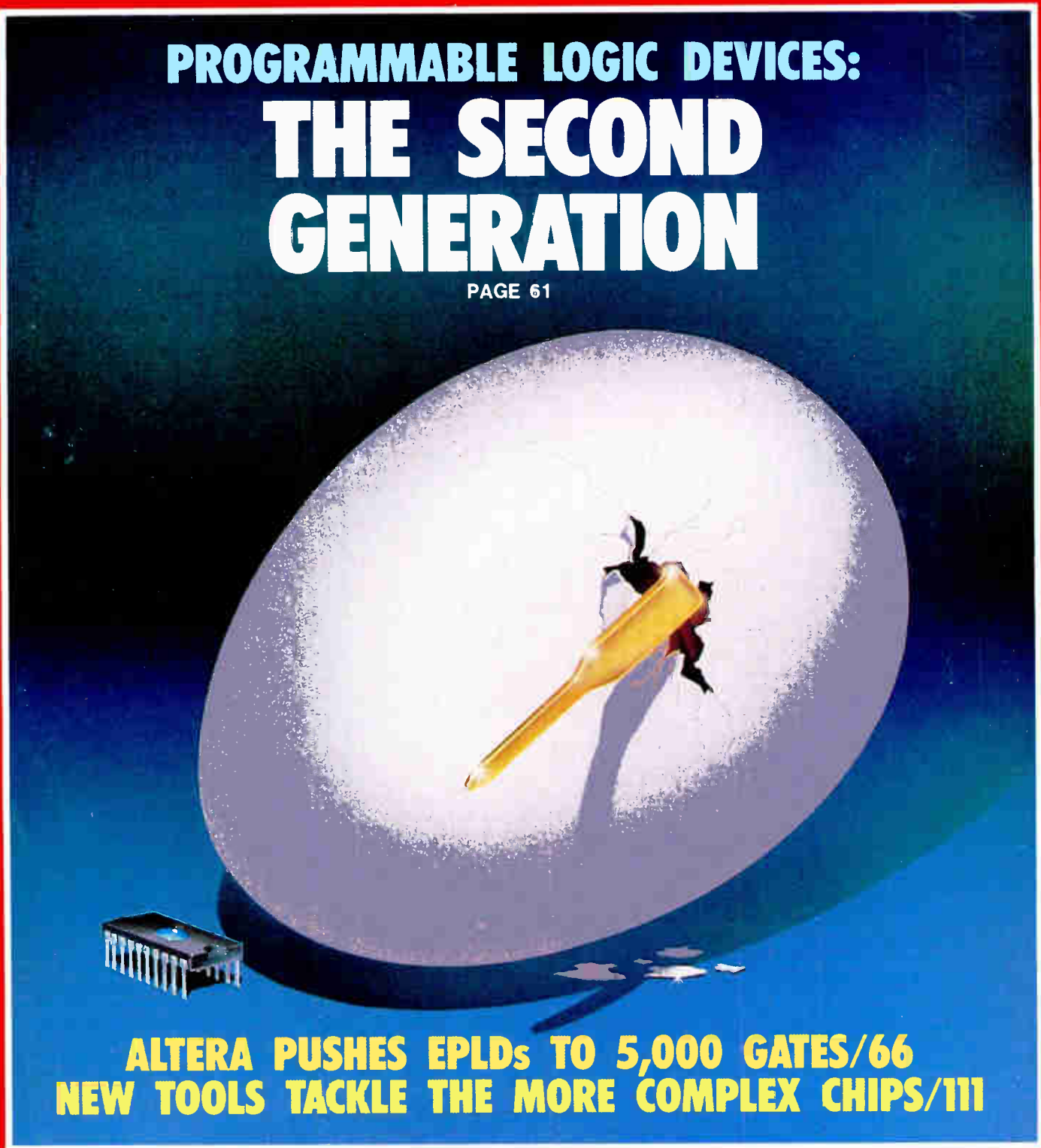

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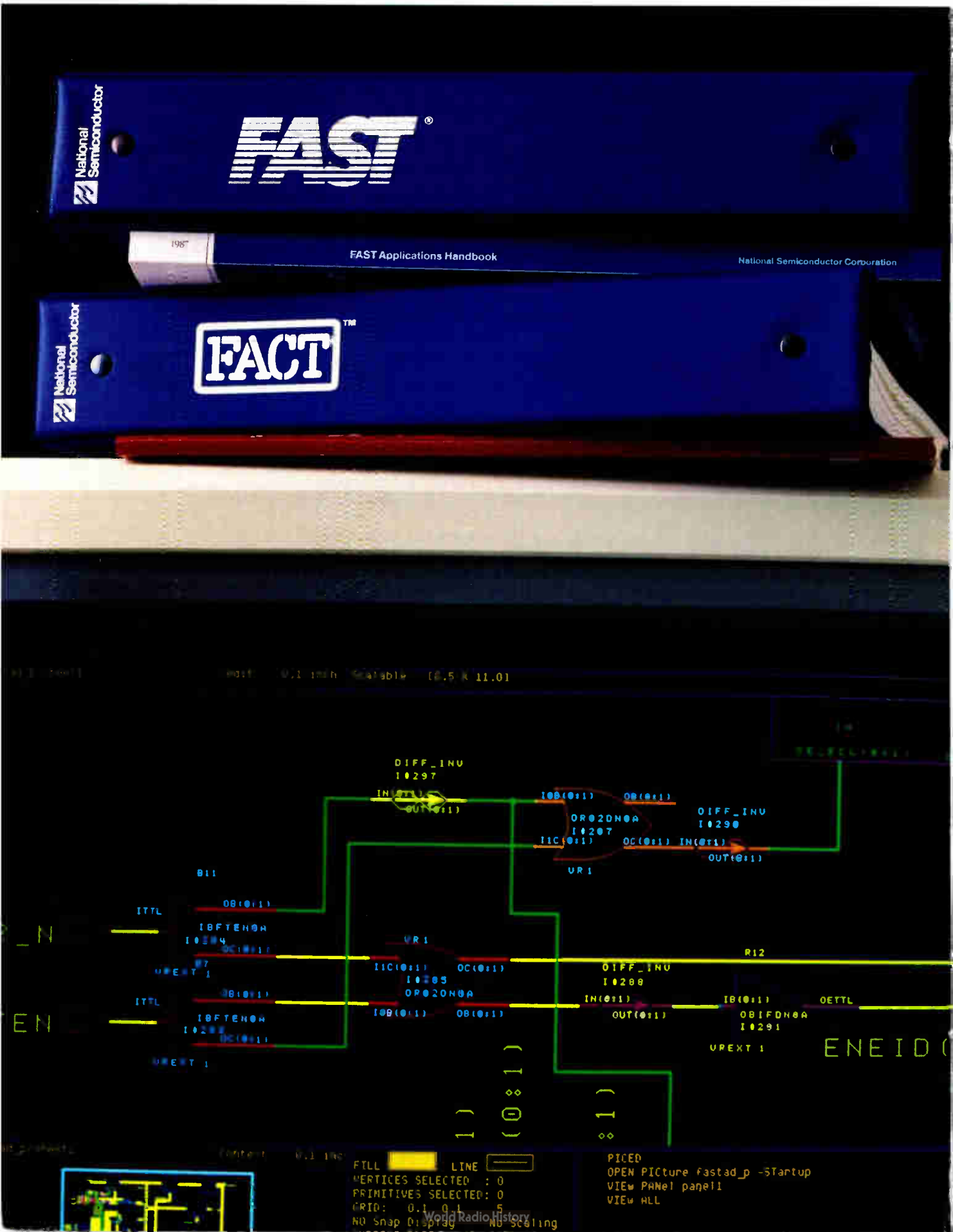
National Semiconductor



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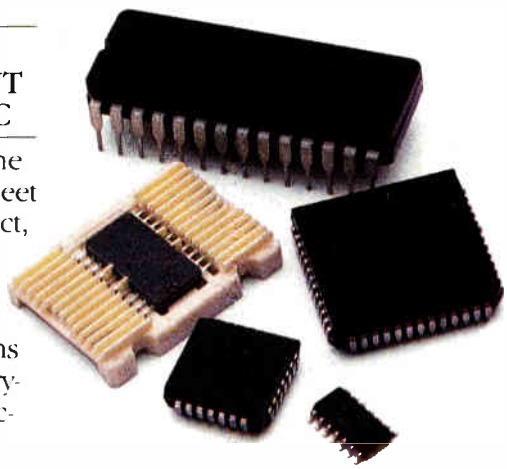

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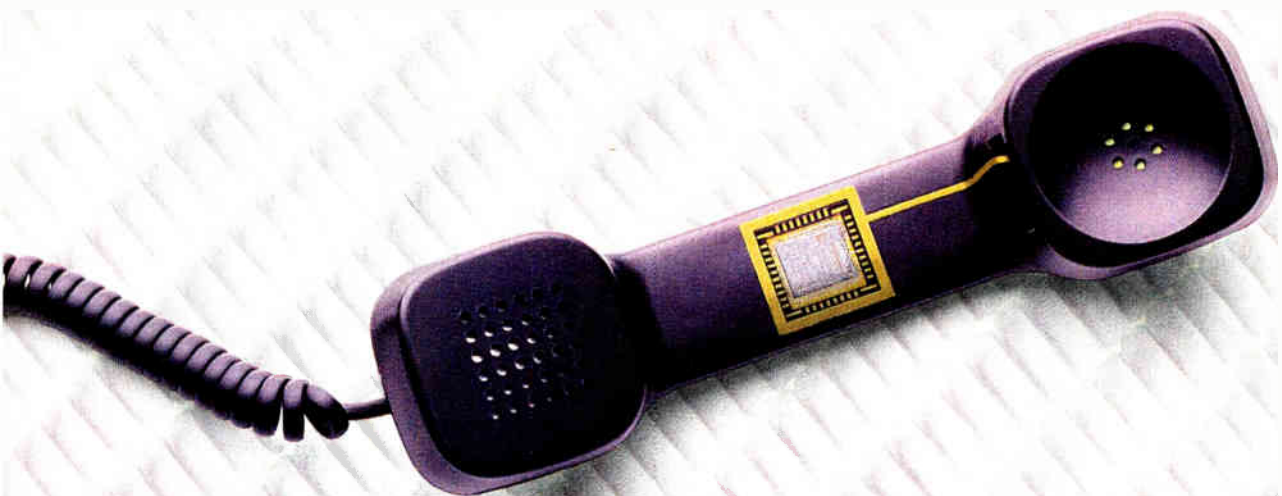

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THE U.S. SEMICONDUCTOR INDUSTRY LIVES!

We agree wholeheartedly with author-economist George Gilder: the entrepreneur remains the driving force of growth in the U. S. chip business

We have always strongly believed that a key U.S. asset was, and still is, the startup culture of Silicon Valley. But entrepreneurs have taken their lumps recently; even some Valley leaders believe the startup culture has become the chip industry's biggest weakness in competing with Japan. Hogwash!

Author-economist George Gilder might not use the word hogwash, but he does believe the entrepreneur remains the driving force of growth in the U.S. chip business. Gilder digs into the subject—a major point in his upcoming book on the semiconductor industry—in the current issue of *Harvard Business Review*, beginning a major debate there on the role of small vs. large enterprises in future U.S. competitiveness. Both of us vote for the little guy.

To Silicon Valley patriarchs, Gilder says, the remedy to counteract intensifying competition from Japan has been intervention by the U.S. government to reshape and subsidize their industry. These ideas bore fruit in Sematech, but Gilder opposes such government intervention as this to help the larger firms compete. The secret of U.S. success in chips and computers has been the very venture system that the critics condemn, he says. It counteracts high capital costs by efficiently targeting funds and fosters a wildfire diffusion of technology that compensates for the lack of national coordination. Future integration will move downward onto the chip, and small companies, entrepreneurs, inventors, and creators will benefit greatly, he says. Large centralized organizations will lose relative efficiency and power.

So to say that huge conglomerates will take over the information industry because they have the most efficient chip factories is like saying Canadians will dominate world literature because they have the tallest trees, Gilder says. If the doomsayers are correct, the 97 chip makers started up between 1982 and 1987 would be in big trouble today. But the vast majority are already profitable and their success ratio far exceeds the performance of those startups in the industry's heyday. Those who lament the passing of the U.S. chip business are dead wrong, Gilder says. "The American semiconductor industry is alive and well, only it's taking on a different shape from that of its Japanese rivals." Attaboy, George! **ROBERT W. HENKEL**

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MAY 12, 1988

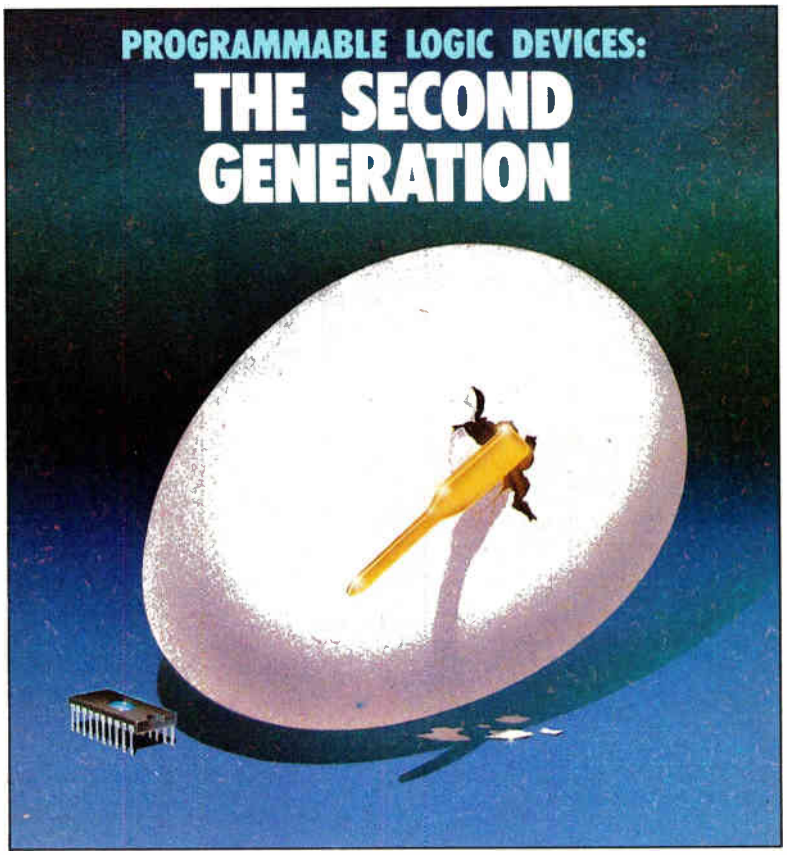
Electronics

NEWS

INSIDE TECHNOLOGY

PROBING THE NEWS

COVER: JEFFREY LYNCH



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DEPARTMENTS

(Forward Thinking, Re

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HOW A MUSICIAN SPEARHEADS THE MOVE TO BETTER FM

GREENWICH, CONN.

Scientists who are also accomplished musicians are rare. But Emil L. Torick has managed to merge the two fields—and thanks to his latest work, FM stereo radio broadcasting now appears headed for its first major upgrade since it was authorized in 1961.

Formerly vice president for audio technology at the defunct CBS Technology Center, the 56-year-old Torick was once a symphony violinist and still plays as an avocation. His professional focus these days, though, is on the FMX Stereo Broadcast System.

Torick was a coinventor of FMX at CBS, which shares FMX patents with the National Association of Broadcasters. (Thomas Keller, chief scientist for the NAB's Science and Technology Division, is the other FMX inventor.) After CBS closed the Stamford, Conn., center in 1986, Torick found financial backing to continue FMX development [*Electronics*, April 16, 1987, p. 39]. The result was Technology Broadcast Partners. Formed a year ago with Torick as president and chief executive officer, it plans to market and license the FMX technology.

In practical terms, FMX significantly increases broadcasting range for stereo FM—by up to four times in early tests. It also enhances fidelity considerably, by eliminating a great deal of the 26-dB signal-to-noise penalty incurred by a convention FM stereo signal. Preliminary tests showed signal-to-noise-ratio reductions up to 23 dB.

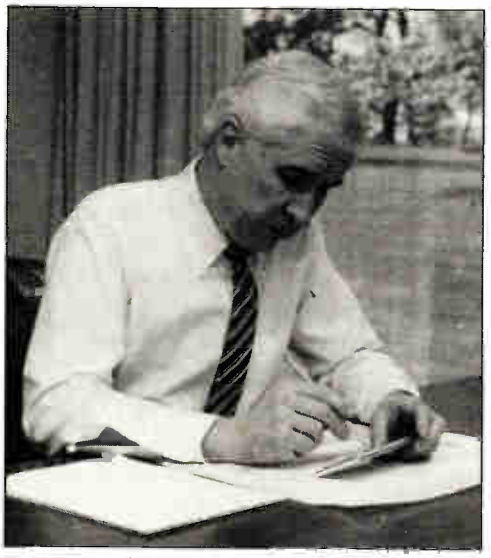
FMX works by using a compressor/expander system that works in conduction with an adaptive expander in a radio receiver. The expander can conform to any compression curve transmitted by a broadcaster. The system differs in that respect from conventional compandor systems, in which the expander must be precisely tuned to a predetermined compression ratio. A 38-KHz double-sideband suppressed carrier stereo difference channel acts as a decoding reference for the expander.

Requiring no Federal Communications Commission approval, FMX maintains compatibility with conventional FM stereo broadcasts—today's FM radio can pick up tomorrow's FMX signal. An FMX-compatible radio is needed, though, to hear the difference in sound quality.

Torick's company plans to show off prototype FMX receivers from about a dozen vendors at the Summer Consumer Electronics Show in Chicago, June 4-7. The first production FMX decoder chips are expected from Sanyo Semiconductor this summer, Torick says, and FMX-equipped radios could be on the market by year's end. Already, at least nine U.S. stations are on the air with FMX. And CBS announced plans in April to convert its owned-and-operated FM stations in 11 major markets by midsummer. FMX broadcast generators are already available commercially from one vendor, with four others developing products. Torick expects 100 stations to be broadcasting in FMX by the end of the year.

None of this might have happened had Torick stayed on his original career path. As a high-school student in Pittsburgh, he says, "it was a tough call whether I was going to go into science or music, because I loved them both." He first chose music. A bachelor's degree in music from Duquesne University in 1953 led to work as a professional musician. Then he went back for another bachelor's degree, this one in physics, from the University of Pittsburgh. He joined CBS upon graduation in 1958.

FMX crowns a career in audio recording and broadcast equipment. It's potentially his most satifying achievement, he says, because the improvement in broadcast quality will be noticeable to a large FMX-radio audience. "Just like I can feel real good about a performance that has something musically good to say," Torick says, "it's the same way when a science project gets recognized." *–Wesley R. Iversen*



Emil Torick finds his work on the development of FMX potentially the most satisfying of his career.

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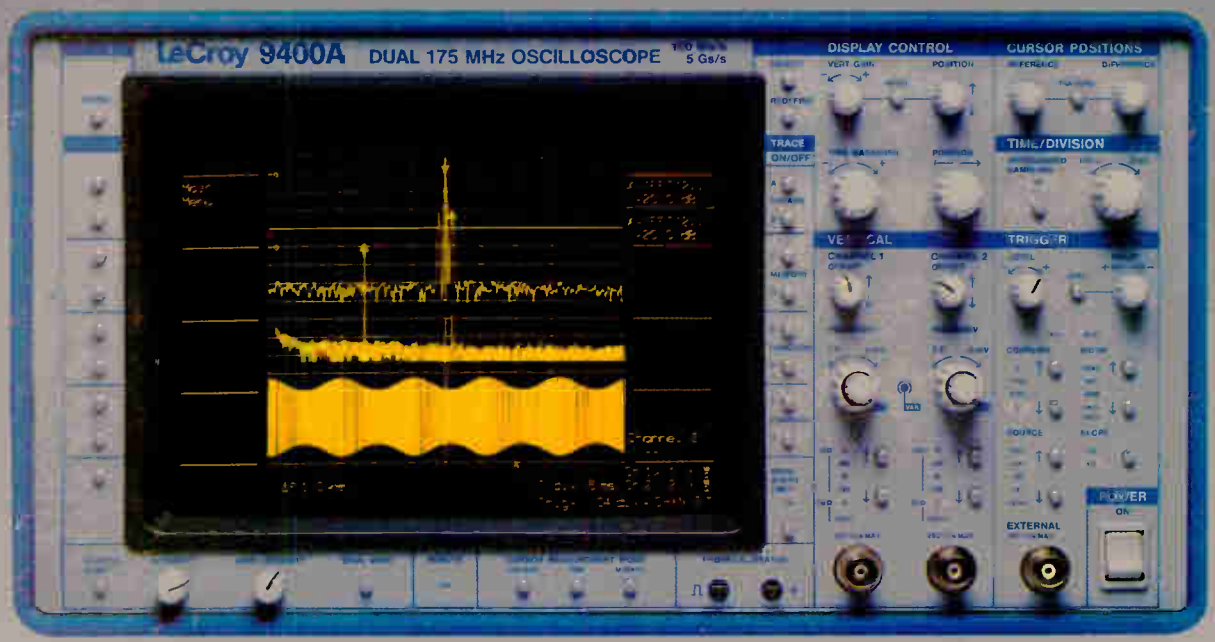

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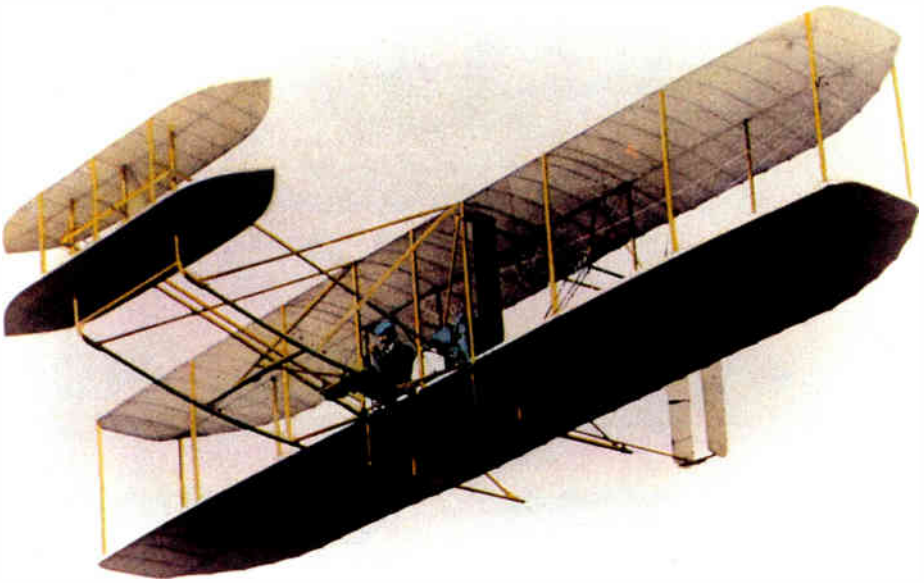
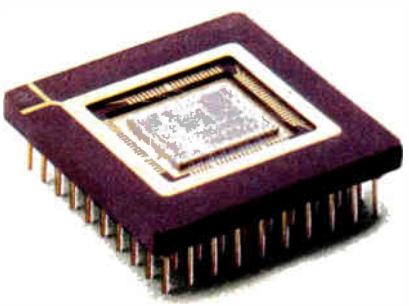


"IT'S GOT POSSIBILITIES, BUT IT'S JUST TOO POWERFUL FOR MY APPLICATION NEEDS."

DESIGN ENGINEER, 1988



Over the centuries, people have looked at the latest in technology with a bit of skepticism. The Transputer from INMOS is no exception.

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LETTERS

Did Hunter decide the undecidable?

To the editor: I got a chuckle and a shudder from your article, "Now, a practical way to run DOS code under Unix/80" [*Electronics*, March 31, p. 80].

The chuckle came from the claim that the Hunter conversion program computes "every possible path in the program" and computes condition codes only along those where they're actually used. A little thought shows this is equivalent to solving the famous halting problem (which is known to be undecidable). While I'm sure it's possible to write a very good 80286-to-68000 decompiler, no program can be quite as good as claimed without overthrowing the foundations of computer science.

The shudder came from the article's statement that using the decompiler is an easy way to get multiuser versions of DOS software. The very act of transliterating code to another format violates most licensing agreements.

Andrew Wilson
Epiphany Inc.
Portland, Ore.

☐ *Hunter Systems says its software makes an exhaustive search of possible program paths; it has demonstrated that the program works. When* DOS *programs are ported to multiuser systems, the licensee is responsible for purchasing a license for each user.*

More comments on DSP, from Zoran

To the editor: I read with interest your article, "Digital signal processing: chips are here, but software isn't" [*Electronics*, March 31, 1988, p. 57]. Although I appreciate the coverage given Zoran Corp., I would like to correct information about Zoran products. The DSP functions are not really in read-only memory on the chip, but rather are hardwired.

The comment from David Fair of Analog Devices Inc. that the VSP161 can only perform six functions is inaccurate. The VSP161 can obviously perform many more than six functions. The statement that I concede the prewritten algorithms limit where Zoran chips can be used implies that Mr. Fair's statement is true, but I emphatically do not agree with his statement. Zoran products may be somewhat less flexible than, say, the Analog Devices 2100, but that was intentional by design. We traded that generality to get much higher performance and ease-of-use in our products. Also we realized, as William Fleck of Hewlett-Packard points out in the following paragraph, that most DSP applications contain a general-purpose microprocessor, which can perform the functions not handled by the VSP161.

Michael Stauffer
Zoran Corp.
Santa Clara, Calif.

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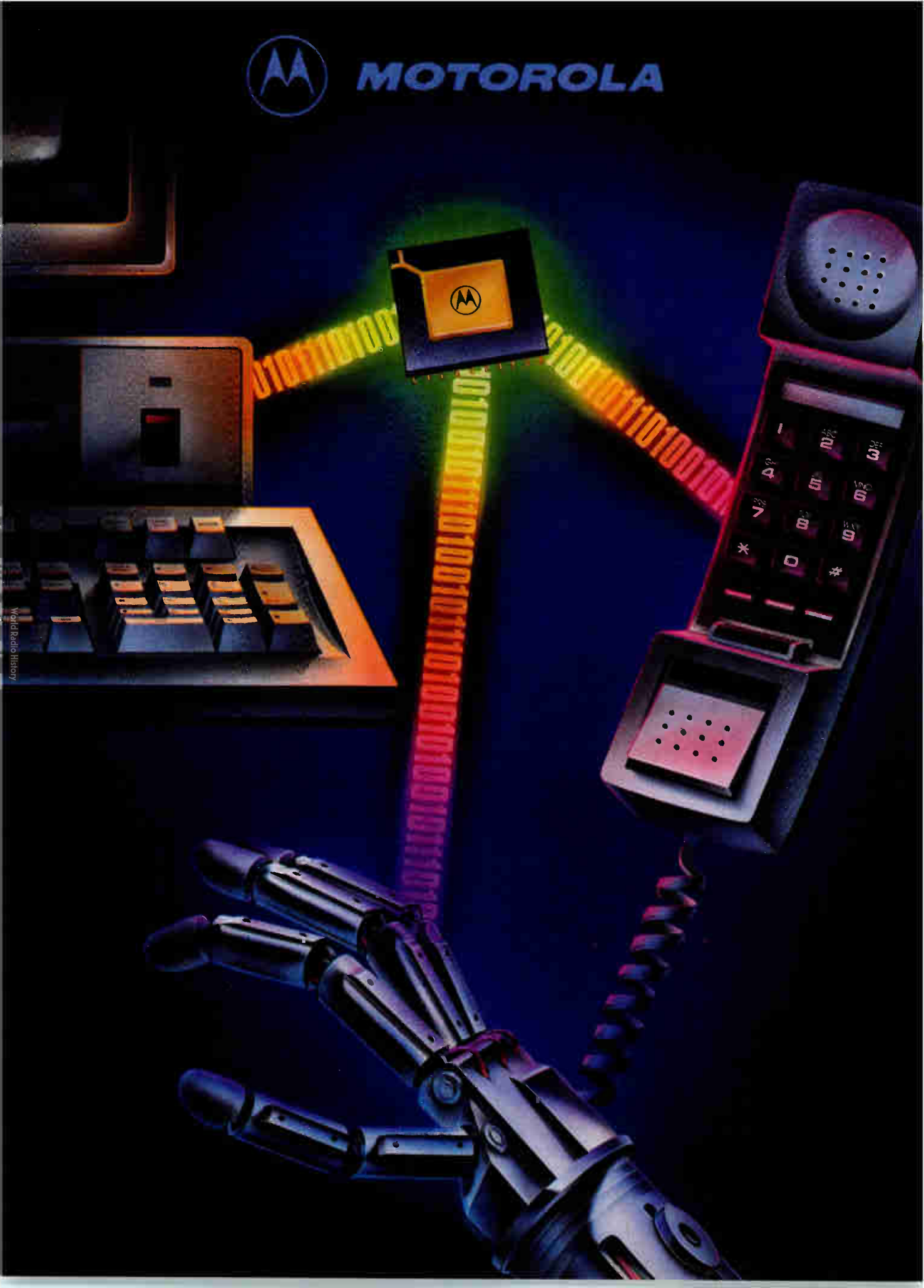

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This VLSI device provides a cost-effective solution to ISDN link-level processing with simultaneous support for up to 8K logical links. The MC68606 is an intelligent communications protocol controller compatible with AT&T specifications for ISDN devices and features low power consumption and high performance, with an aggregate data rate in excess of 2.048 Mbps.

Token Bus Controller IEEE 802.4 MAC.

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The MC68KTBFA Token Bus Frame Analyzer Software (TBFA) is a real-time software tool that speeds development of token bus networks. The TBFA keeps track of statistics while monitoring network performance. By using the simple menu-driven interface, the user can define triggers to selectively store and display frames, creating a powerful tool for network analysis.

The TBFA is a set of four EPROMs which runs on a VMEbus MVME372 Token Bus Controller board and requires a modem, a VT100 terminal, and a power source. The cost-effective TBFA sells for about one-tenth the cost of existing token bus protocol analyzers.

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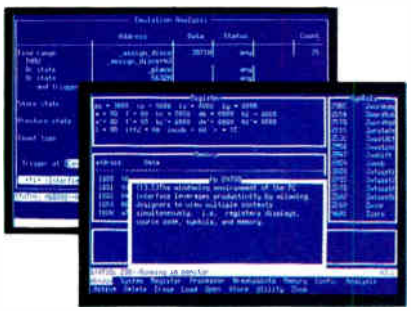

Multiwindow viewing allows up to eight displays on-screen simultaneously.

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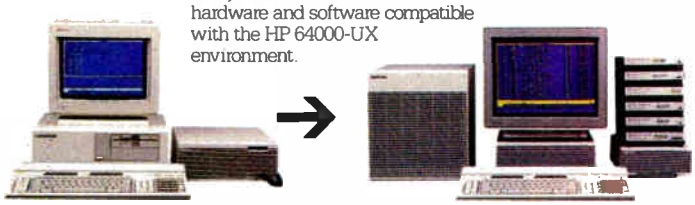

interface for superior download and upload speed, code coverage analysis for efficient software testing and design, host-independent portability, and compatibility with popular absolute file formats such as Tektronix and Intel hexadecimal and Motorola S record.

Once you get your hands on an HP 64700 emulator, you'll agree that this is the new standard in the field. Especially at a starting price of $8,900.

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For a free demo disc that gives you the "hands-on" feel for HP 64700 Series capabilities, call HP at 1-800-752-0900 ext. 501A, or mail the attached business reply card.

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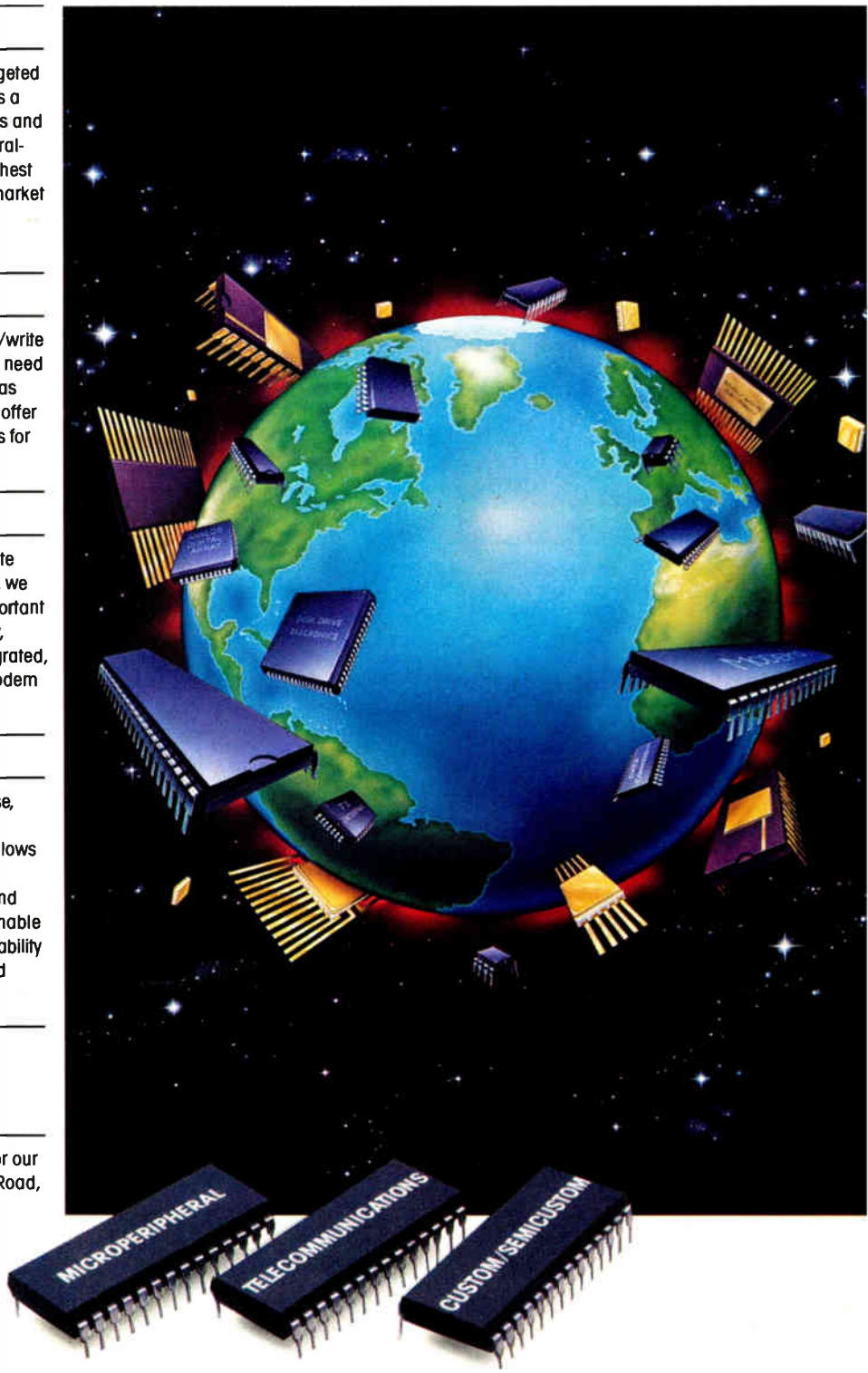

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ELECTRONICS NEWSLETTER

A DOZEN TOP COMPUTER AND COMMUNICATIONS FIRMS JOIN OSI ENDORSEMENT PARADE

A dozen of the world's biggest computer and communications companies have joined in a resounding endorsement for the Open Systems Interconnect networking protocols. The adoption of the seven-layer OSI standard for managing multivendor networks will mean users can give greater weight to performance—and less to compatibility—in purchasing decisions, says Murray Weidenbaum, who heads the Center for the Study of American Business in Washington and is the former chairman of the President's Council of Economic Advisers. He predicts customers will see productivity gains of about 30% as a result of the agreement. Now, instead of competing with proprietary systems, the dozen companies will form alliances among themselves and compete on the "eighth level of OSI"—how to most efficiently manage distributed computer systems—says Wim Roelandts, vice president of Hewlett-Packard Co.'s Networked Systems Group. The 12 companies read like a who's who in computing: AT&T, Control Data, Data General, Digital Equipment, Hewlett-Packard, Honeywell-Bull, IBM, Sun Microsystems, Telenet Communications, Unisys, Wang Laboratories, and Xerox. The 12 companies account for 80% of U. S. computer and telecommunication sales. □

FORD BUILDS A 1,000-GATE GaAs-ON-SILICON ARRAY

Add Ford Microelectronics Inc. to the list of firms demonstrating large-scale integrated circuits etched in gallium arsenide on a silicon substrate. Ford says it has fabricated fully functional 1,000-gate-equivalent arrays on 3-in. GaAs-on-silicon wafers. At about 6,600 transistors, the array is second in density only to a GaAs-on-silicon 1-K static random-access memory from Texas Instruments Inc., say Ford executives. The TI part has 7,500 transistors [*Electronics*, Sept. 18, 1986, p. 31]. The Colorado Springs, Colo., subsidiary of Ford Motor Co. reports yields of up to 11% on its arrays, which incorporate test circuitry including dividers, 8-bit adders, a 263-gate inverter string, and D flip-flops. But at 1.2 ns, gate delays are still three to four times longer than is common with bulk GaAs devices. Ford is pursuing GaAs-on-silicon with an eye toward mixed-mode chips, in which high-density silicon circuits could be combined on one chip with high-speed GaAs circuits. □

INTEL PLANS AN ASSAULT ON THE JAPANESE MARKET WITH ITS UV-ERASABLE PLDs

Intel Corp. is taking the first steps to aggressively market its ultraviolet erasable programmable logic devices in Japan. The Santa Clara, Calif., chip maker is offering a development system there for its entire line of EPLDs. The EPLD-LOC software runs on the NEC Corp. Personal Computer PC-9800 series, which is the Japanese standard for desktop engineering, says Mohammed Aboobaker, general manager of programmable logic development at Intel in Folsom, Calif. EPLD-LOC contains a set of tools for compiling all of Intel's PLDs, such as its enhanced 1-μm 5AC312. □

TAIWANESE CLONE MAKER IS SELLING ITS CHIP SET

The U. S. subsidiary of Taiwan's Acer Inc., which clones IBM Corp.'s Personal Computer line, is plunging into the crowded market for PC-clone chips. Acer Laboratories Inc. of Sunnyvale, Calif., is offering a family of 13 CMOS chips for the various system-, graphics-, and peripheral-control functions used in IBM's PC XT, AT, and PS/2 systems. By combining the eight chips in the PC86 series—which is priced at $77 in 1,000-set quantities—users can get the functions necessary to build a fully compatible PS/2 model 20 or 30, Acer says. The graphics and peripheral-control circuits can be used separately in PC XT and AT designs. □

ELECTRONICS NEWSLETTER

AT&T MOVES INTO THE TWISTED-PAIR CHIP MARKET FOR ETHERNET

AT&T Co. is getting into the local-area-network chip business with two CMOS circuits based on an emerging standard for 10-Mbit/s Ethernet communications. AT&T is getting a jump on the competition by unveiling the T7210 Manchester decoder and interface chip and the T7200 multiport repeater controller at the Electro show in Boston May 10—just ahead of the expected approval of the new IEEE standard this month. The standard—IEEE 802.3 10 Base.T—sets the communication protocols for Ethernet LANs on twisted-pair wiring. A competing standard proposed by Digital Equipment Corp. and 3Com Corp. has been withdrawn, paving the way for easy approval. "We envision twisted pair as the dominant media for 10-Mbit/s LANs in the future, supplanting coaxial cable," says Thomas V. Gates, product manger for MOS LAN products at AT&T Microelectronics in Allentown, Pa. Although there are practically no twisted-pair LANs of this sort now in place, he predicts they will make up 60% of such installations in five years. □

MENTOR AND VLSI TECHNOLOGY FORGE A STRONGER LINK BETWEEN DESIGN AND SIMULATION

In one of the first alliances between a major vendor of application-specific integrated circuits and an equally powerful computer-aided-design automation company, VLSI Technology Inc. and Mentor Graphics Corp. have agreed to integrate VLSI's ASIC tools into Mentor's CAD line. The integrated system allows users of VLSI's high-density ASIC technology to design chips and then simulate them in board- and system-level applications before committing to a design. For VLSI, the move continues its effort to merge its design tools with those of CAD work-station vendors; last year the San Jose, Calif., chip maker made its Portable Macro Library available on Daisy Systems work stations. □

CRAY CANCELS ITS X-MP IN FAVOR OF A CHEAPER, MORE POWERFUL HYBRID

Supercomputer leader Cray Research Inc. is replacing its popular X-MP with a hybrid machine that can run software for both its four-processor predecessor and the newer eight-processor Y-MP. Cray says the X-MP EA (for extended architecture) will account for about 25% of the 65 new and used supercomputers that Cray will sell this year. The X-MP EA is based on a hybrid processor built with both the X-MP's 16-gate emitter-coupled-logic chips and the 2,500-gate ECL arrays employed in the Y-MP. It runs software written for either machine. Although it offers identical performance to the top X-MP—1.2 billion floating point operations/s—the X-MP EA has four times the main memory capacity—64 million 64-bit words. The result is a dramatic increase in price/performance: a four-processor X-MP EA/464 with 64 million words of memory sells for $14 million—$2 million less than the best X-MP. □

MAYBE THE CHIP ACCORD ISN'T TO BLAME FOR THE DRAM SHORTAGE

The U. S.-Japan semiconductor trade accord of 1986 has received much of the blame for the current shortage of dynamic random-access memory chips, but a former U. S. official who helped write the treaty says that theory is unfair. "The chip agreement by itself is not responsible for the DRAM shortages," says Clyde Prestowitz, a former Commerce Department undersecretary and now a senior associate with the Carnegie Endowment for International Peace in Washington. Prestowitz, who wrote *Trading Places*, a best-seller on the changing economic roles of the U. S. and Japan, discounts the theory that the Japanese are using the agreement as a tool to limit production. He suggests the shortage is part of a historical supply and demand cycle in which cheap memory prices, as the U. S. enjoyed until recently, have spurred DRAM use beyond capacity. When capacity rises, he says, prices should fall. □

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DT2651 High Res. Frame Grab and DT2658 Aux. Frame Proc.	512x512	256	✓	✓	✓	4	✓	✓	2 Buffers 512x512x8 (512 KB) and 1 Buffer 512x512x16 (512 KB)	✓	✓	✓	DT-IRIS ($1995) DT/IDL ($3750)	$2995 $1895

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PRODUCTS NEWSLETTER

SMC VIDEO CONTROLLER GIVES TERMINALS SUPER FAST WINDOWING

Designers of the next generation of terminals can build in sophisticated windowing capability—up to 127 windows per screen—with Standard Microsystems Corp.'s CRT97C11 Video Engine for Windows chip. Fabricated in 2-μm CMOS, the View chip handles the multisession, multihost terminal applications coming in the next two years, says the Hauppauge, N.Y., company. Besides greatly enhancing functionality, the View chip will cut windowing-software development time 80%. That's because windowing is implemented mostly in hardware, which also boosts speed on an order of magnitude compared with software-implemented windows. What's more, since the chip uses a character-mapped—not bit-mapped—display scheme, it requires less memory—just 4 Kbytes instead of 256 Kbytes for a 512-by-512-pixel screen. Available now, the CRT97C11 costs $32.35 each in 100-unit quantities. □

MIPS 12-MIPS SYSTEM ACHIEVES UP TO 15 TIMES BETTER PRICE/PERFORMANCE

MIPS Computer Systems Inc. is delivering 12 million instructions/s in its newest multiuser computer system based on the Sunnyvale, Calif., company's R2000 reduced-instruction-set multichip processor. At $2,500/mips, the M/120 also offers the lowest cost per mips of any server or minicomputer class machine on the market—typically 5 to 15 times more cost-effective than competing systems. Running at a 16.7-MHz clock speed, the M/120 executes over 27,400 Dhrystones/s and 9,100 KWhetstones/s. By tightly coupling the R2010 floating-point chip with the R2000 processor, MIPS engineers attained 2.1 million floating-point operations/s on the M/120. It is available now in both 9- and 12-mips versions for about $26,500 and $30,000, respectively. □

HUGHES TESTER MAKES IT EASIER TO FIND FLAWS IN WIRE ASSEMBLIES

Finding the minute discontinuities in solder and crimp connections that often plague complex wiring assemblies can be made considerably easier with a new tester developed to improve reliability on missile programs at GM Electronics/Hughes Aircraft Co. The Model 303 discontinuity tester proved itself by increasing manufacturing yields of flexible printed wire assemblies by more than 100%, says an official of Hughes' Industrial Products Division, Carlsbad, Calif. It works by continuously applying a dc current through all circuits of a wire harness during the environmental (vibration or thermal cycling) testing cycle. The tester detects microscopic breaks by increasing impedance, in a process also called "intermittence monitoring." The basic unit, at under $30,000, is modular, so the number of output channels can be expanded. Delivery takes about 90 days. □

SOFTWARE GIVES ON-LINE TRANSACTION PROCESSING AN IBM ALTERNATIVE

The new wave of distributed hardware architectures can now attain its full parallel-processing-performance potential in on-line transaction processing by using VIS Systems Inc.'s Unix-based VIS/TPS software package. Furthermore, OLTP shops can now look at cost-effective alternatives to IBM Corp. hardware. Until now, Unix's multitasking capabilities have been degraded in OLTP applications because Unix—created for academic and engineering uses—has gaping holes in connectivity and could not handle applications programs written in CICS Cobol. Within VIS/TPS, the VIS/Online-Exec executes applications in CICS Cobol translated from IBM's MVS or DOS to the Unix environment. Communications and file server software handle the distributed processing interface; other modules translate most CICS Cobol applications into the Unix environment. Available now from the Dallas startup, VIS/TPS software systems start at $50,000. □

PRODUCTS NEWSLETTER

HARRIS 16-BIT MICROCONTROLLER TARGETS REAL-TIME APPLICATIONS

Look for Harris Corp. to invade the market in real-time applications such as vision systems and robotics with a 16-bit microcontroller that runs at 10 million instructions/s. Although not as fast as some recently announced 32-bit microcontrollers [*Electronics*, March 17, 1988, p. 64], the Forth-based RTX2000 features a unique bus that allows the attachment of external application-specific peripherals by providing a path directly through the internal arithmetic logic unit and register stacks. By using a proprietary Quadbus architecture that is not dependent on pipelining to achieve performance, the RTX2000 features interrupt response times of less than 400 ns and context switching times of less than 2 μs. Available in sample quantities now from the Melbourne, Fla., company, the RTX2000 is $190 each in 1,000-unit lots. □

SIEMENS GATE ARRAYS LET DESIGNERS MIX CML AND ECL ON SAME CHIP

Designers of high-speed semicustom logic can now mix current-mode and emitter-coupled logic on the same chip, thanks to a new family of gate arrays from Siemens Semicustom Products of Santa Clara, Calif. The 1,500-, 2,500-, 7,000-, and 10,000-gate SH100E arrays team the high-density, low-power advantages of CML in circuit paths where speed is not crucial with ECL's raw speed in the circuit's critical paths. The arrays also offer a range of power-programming options for each gate, allowing further tailoring of the power/speed trade-offs appropriate for each area of a design. The input/output circuits can be customized individually to TTL or ECL levels, as well. At full clip, gate delays are 120 ps, or 90 ps when differential drive is used. The arrays will be available in the third quarter, but the Oxis IIIH process used for the arrays is in production. Design manuals are available now. □

ANALOG DEVICES FLASH CONVERTER BOASTS DOUBLE THE FULL-POWER BANDWITH

Analog Devices Inc.'s 8-bit AD770 flash converter may not be the fastest on the market at that resolution, but the Norwood, Mass., company says its 250-MHz full-power bandwidth is more than double the best the competition has to offer. It closest competitor's full-power bandwidth is 120 MHz. The AD770 is no speed slouch either, running at 200 megasamples/s compared with the competition's 300 megasamples/s. The bipolar AD770 flash converter is fabricated with an emitter-coupled-logic process and extensively tested so that Analog Devices can specify better signal-to-noise performance—45 dB at 10 MHz, 30 dB at 100 MHz—at higher frequencies than any competitor. The chip's bandwidth will be especially useful in digital oscilloscopes, radar signal processing, and digital radio. It will be available in late May, priced at $175 each in 100-unit quantities. □

NATIONAL INSTRUMENTS KIT TURNS SUN WORK STATIONS INTO LAB CONTROLLERS

Engineers who want to use Sun Microsystems Inc.'s models 3 or 4 work stations as instrumentation controllers can get a big assist from a new kit from National Instruments Corp., Austin, Texas. The GPIB-S3/4 kit includes a high-speed VMEbus IEEE-488 interface board, adapter bracket, interconnecting cable, and Unix software handler on a Sun cartridge. National Instruments says its Unix software handler is more extensive than boards offered by the competition, and includes 30 of the more frequently used function calls between the computer and an instrument. In addition, the kit is fully assembled mechanically, with the backplane connector mounted on the assembly bracket, a step that is often left to users with similar products. The kit provides data transfer between instruments and the Sun work stations at 500 Kbytes/s. The $2,745 kit is available immediately. □

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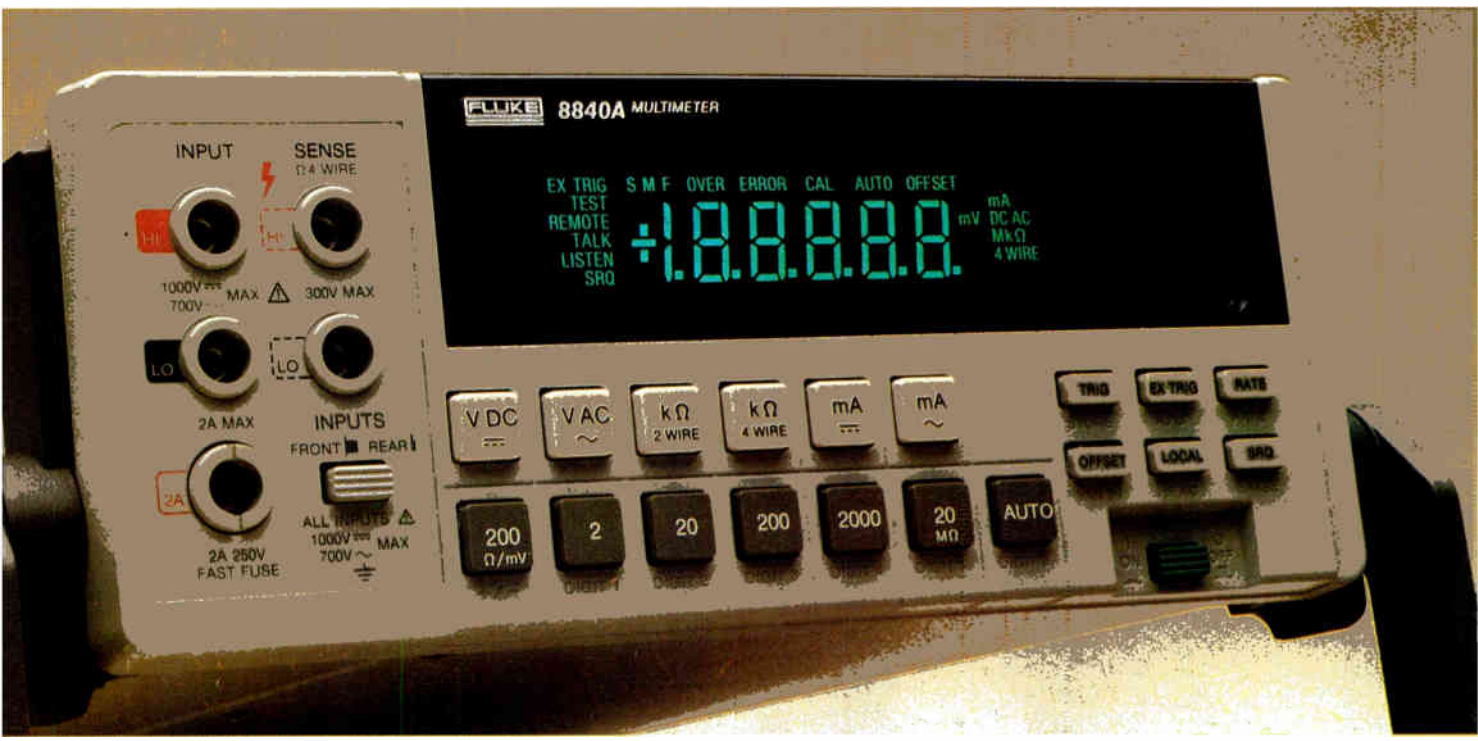

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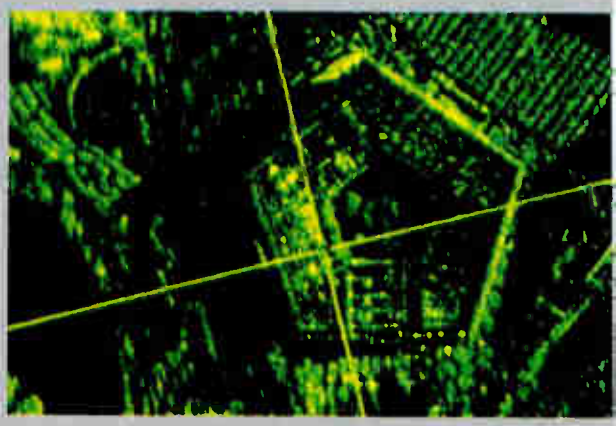
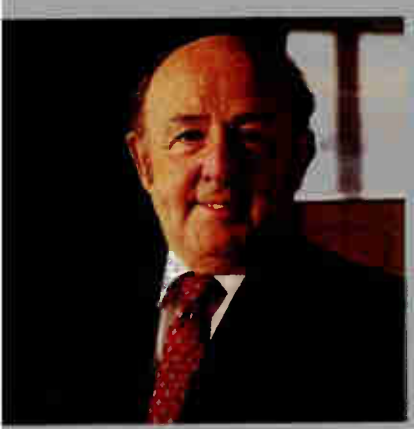


While developing software for the B1-B Bomber radar system, Westinghouse Defense landed on a tough problem – integrating its computer resources. "We needed a complete network that would allow hundreds of software engineers across the country to interact, create, enhance and modify the software," says Ron Clanton, Manager of Software and Information Systems.

The solution was a network from Digital.

Remarks Clanton, "The network is so comprehensive, it extends even to the air in our Flying Software Lab. Giving us real-time, in-flight software testing and development capabilities. The Software Lab alone provides a cost savings of up to 98% versus traditional in-flight testing in the B1-B Bomber."



"A networked software engineering environment that helped Westinghouse Defense zero in on ways to cut in-flight test costs by 98%."

"But our savings don't stop there," continues Clanton. "With the VAX™ architecture and the VMS™ operating environment, engineers both on the ground and in the air can react instantly to each other's modifications." He adds, "That's sharing their knowledge and expertise faster and more productively than they ever thought possible. Which, of course, provides for a better end product."

Clanton sums it up this way, "Our Digital network and The Flying Software Lab allow us to cut software development time and costs across the board. And that's increasing our productivity and ability to compete for similar projects."

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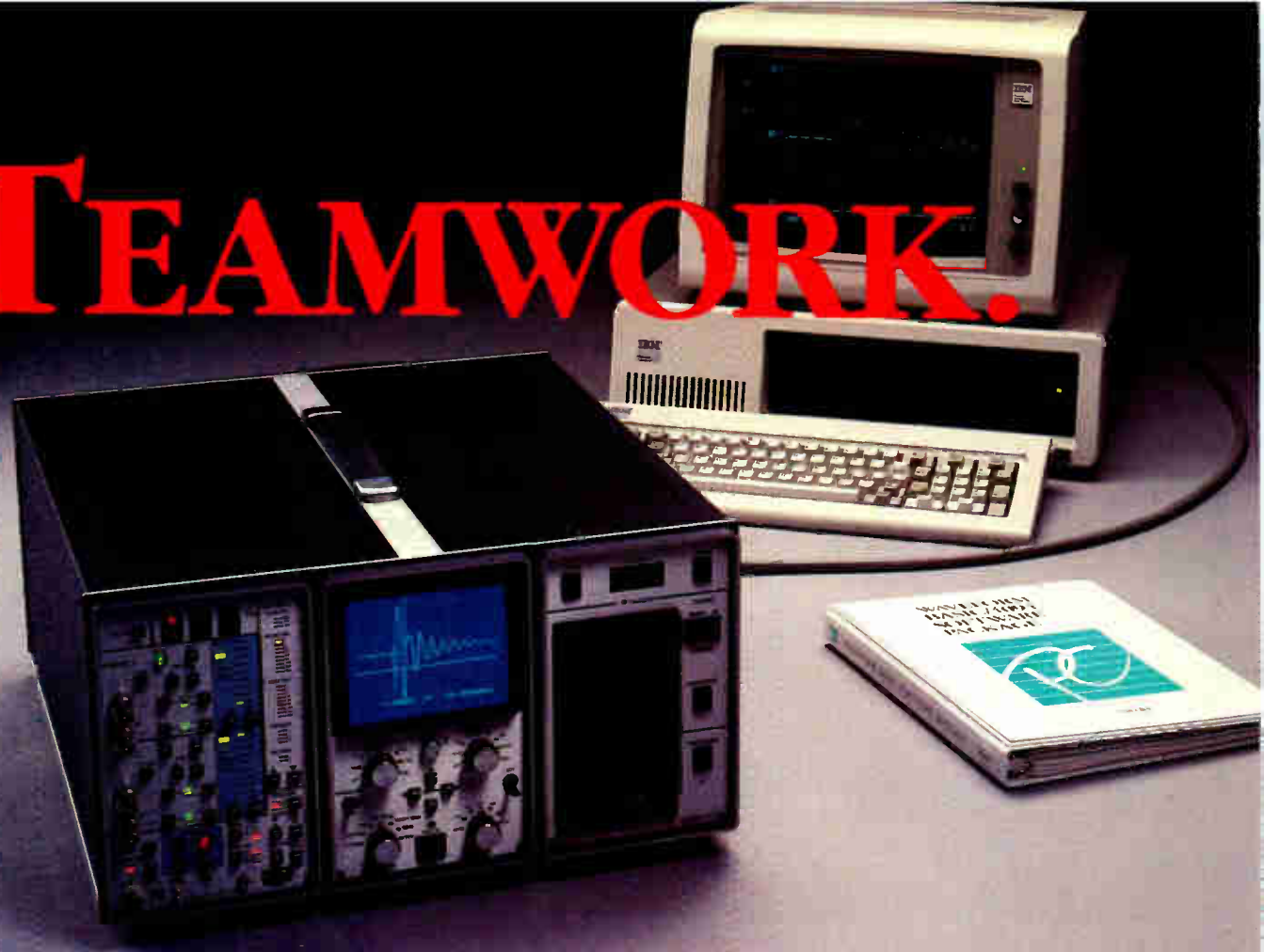

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Electronics

CHIP BUSINESS PICKS UP SPEED; GROWTH HEADS TOWARD 30% THIS YEAR

But In-Stat's Beedle sees the present quarter as the 'peak of this cycle'

PHOENIX

Buoyed by the strength of a 16-month comeback from the depths of its worst decline ever, the chip business is still picking up speed in the first months of 1988. In fact, prospects appear so good that projections of 1988 worldwide sales growth are continuing to head toward the 30% level.

But amid the satisfaction and congratulations, some veteran market watchers and industry insiders, scarred by previous boom-and-bust experiences, are beginning to pick up bad vibes from the system's abuses that often signal a downturn. Others believe that newly placed safeguards will cushion any such fall.

As April turned into May, a flurry of new forecasts arrived for semiconductor industry experts to mull over. They came from In-Stat, Dataquest, and the World Semiconductor Trade Statistics Committee. The crystal-ball gazers tend to agree on a continued strong 1988, but some see gathering clouds for 1989.

Jack Beedle, president of In-Stat Inc. and a well known bear, is among those detecting early warning signs. He posed some pregnant questions and gave some worrisome replies in Phoenix last week at his annual forum for the semiconductor industry. "Are we overheating? Are we worried? Have we learned anything from the last time? The answer is 'Yes' to the first two questions, and 'I hope so' to the last."

His prognostications are cautious. They call for orders to peak this quarter, traditionally the strongest, with a gain of nearly 14%. This strength is apparent from March U. S. bookings, the latest available monthly semiconductor results. "March bookings hit an all-time record high of $1.359 billion, surpassing the previous high of $1.274 billion in April 1984," Beedle says.

Moreover, the pattern of new orders is also encouraging, he says. "They appear to be based from all segments of the end-use markets, rather than isolated to just the computer industry, as has been the story in past upturns." The key office-and-computer-equipment segment itself, the main semiconductor customer whose own sales picture had been somewhat flat during 1987, turned up strongly earlier this year, he points out. The first two months of 1988 saw computer shipments running some 23% ahead of those recorded in 1987, the best performance since the boom years of 1983-1984.

But Beedle says that despite all the good news, a study of past chip cycle patterns and reports of growing abuses stirred by the continuing shortage of dynamic random-access memories cause him to call the present quarter "the peak of this cycle." He predicts that bookings will plunge in the third quarter, winding up with an increase of only 4.8%, and actually decline by about 3% in the fourth quarter.

His reasoning is that big device orders now being placed should satisfy demand for months ahead and buyers will therefore pull back sharply. Double and even triple ordering of DRAMs by hard-pressed computer manufacturers, which is now being widely reported by industry insiders, also ranks as one of the best signs of a market peak, he says.

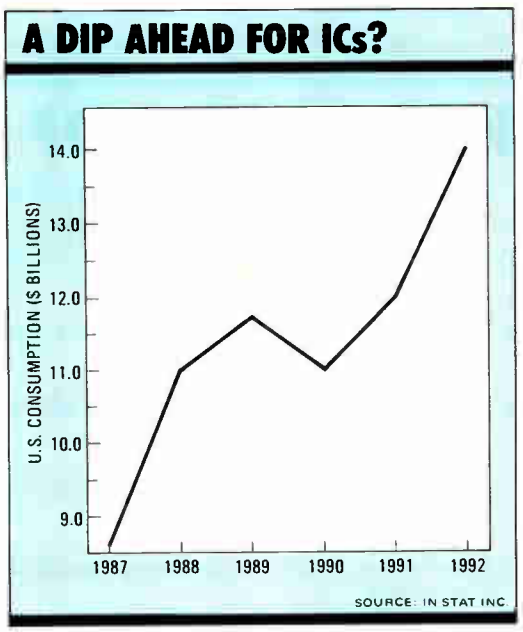
Thus for 1988 overall, Beedle is sticking with his forecast, which is for 26.5% U. S. growth in 1988, from 1987's $10.259 billion. This will decline to just 6.2% growth next year, he says, and slide even further—to 5.7%—in 1990 (see figure).

Other chip market researchers have somewhat similar outlooks, but differ on timing. Dataquest Inc., for example, thinks that chip consumption is still "gathering momentum and will not eventually peak until next year," according to Joseph Borgia, semiconductor analyst at the San Jose, Calif., consulting firm. Buyers still have not let inventories get out of hand and the build-up phase of this chip cycle generally is under better control than in the past, he says.

Dataquest sees "good news for the next 12 months," says Manny Fernandez, its president and chief executive officer. But Dataquest spots the U. S. market higher than does In-Stat: $11.1 billion last year, going to $20.9 billion in 1992. The forecast spots the fastest growth in the Far East. In its view, the Asia-Pacific region will surpass Europe in semiconductor consumption by 1992. The compound annual growth rate from 1987 to 1992 will run 24%, twice that of the U. S. and Japan, Dataquest estimates.

The World Semiconductor Trade Statistics, gathered by a committee that groups the globe's major chip makers, show "expansive growth through the end of 1988." Douglas Andrey, industry statistics manager for the SIA and the U. S. representative for the committee, sees an upward bound of 30.1% to $42.3 billion for world semiconductor sales in 1988, then expects growth will moderate to 3.9% in 1989 as demand from equipment makers eases and chip makers build up their capacity, particularly for DRAMs. "But the industry will return to double-digits in 1990 and 1991 as the cyclical demand recovers," Andrey adds.

Japan now ranks as the world's top



According to In-Stat, U. S. chip business will hit a trough in 1990 after good 1988 growth and a modest 1989 rise.

market, with $12.7 billion last year and with a projected rise to $22.8 billion by 1991. The U. S. market does not qualify as a close second. It posted $10.2 billion in 1987 and will fall further behind by 1991 with a forecasted $16.8 billion. Western Europe runs a distant third: $6.1 billion last year, $9.7 billion in sight for 1991.

The most dramatic growth, the world survey predicts, will take place in the "other international marketplace"—essentially the Asia-Pacific region outside of Japan. The region should double its market size to $7.1 billion by 1991.

BUST COMING? So why are Beedle's figures so bearish, and why are he and others concerned? They know the cyclical nature of semiconductors. Very strong boom times such as those the industry is now experiencing are characterized by book-to-bill ratios rising well above parity, leading to product scarcity and long delivery times. The euphoria of strong business in turn encourages excess expansion of capacity to meet that demand, over-ordering by customers amid price increases, and a feeling that the good times will never end. But when supply grows to the point where it exceeds demand—and it happens every time—a classic economic bust follows on its heels.

The most recent example, still haunting the industry, is the nightmare period of 1984-85. That free fall was caused largely by wild over-ordering stemming from the explosive growth of the personal computer market earlier in the decade. In 1984, U. S. chip production grew an astounding 49.4% to record sales levels, only to plunge 30.2% in 1985, according to the In-Stat records. Total industry losses over the next two years ran up into billions of dollars, most sources say, with even the highly integrated Japanese component producers suffering.

TAKING PRECAUTIONS. That's why officials at the Phoenix gathering said they are determined not to suffer the pain again. And by most accounts, their actions back up their words. Production capacity is being added slowly and cautiously, and bookings are being tracked closely to avoid the double and triple orders (the situation where customers place the same order with several chip suppliers to make sure of delivery).

One school of thought is that those tight controls will keep the situation in check—to a point. "It is not at all like it was in 1984," observes Charles E. Sporck, president of National Semiconductor Corp., Santa Clara, Calif. However, he adds, "it could happen if we continue the current trend." His biggest worry is lead times on deliveries, which are still stretching out in most integrated-circuit areas, in addition to DRAMs. Sporck, for one, welcomes Beedle's forecast that there will be a slowdown for the second half of 1988. "Right now, the business [book-to-bill] is more hectic than I would like."

James Norling, vice president and general manager of Motorola Inc.'s Semiconductor Products Sector in Phoenix, scoffs at the accuracy of the bullish figures for 1988, "Who's to say the rest of 1988 will be such a smasher?" he asks. He says that Motorola's chip orders are strong, promising a good third quarter. Visibility after that becomes cloudy, but the final three months are traditionally the weakest booking period of the year. *–Larry Waller*

SOFTWARE

VHDL: THE LINGUA FRANCA OF DESIGN?

NEW YORK

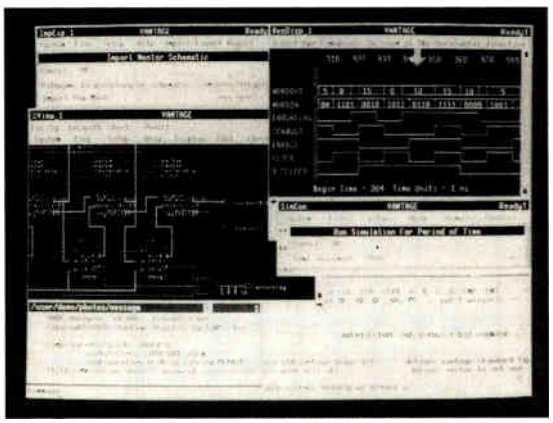
The Pentagon for years has wanted a standard hardware description language and it even designed one—VHSIC Hardware Description Language, or VHDL. There was only one catch: potential users didn't adopt VHDL, because they didn't want to take the time to learn it. But now that attitude is changing as the arrival of practical tools permits even those who don't understand the language to use it.

In fact, VHDL could "become the *lingua franca* of electronic design," says Larry Saunders, an advisory engineer at IBM Corp.'s Application Business Systems Division in Rochester, N.Y. Saunders is also chairman of the VHDL Analysis and Standardization Group, a subgroup of the IEEE's Design Automation Standards Subcommittee.

The reason: with VHDL, a design specification expressed in multiple levels of abstraction can be written in a form readable by both human beings and computers. The design can then be verified through simulation before hardware is constructed. VHDL also provides a vehicle for accurate, systematic design documentation.

The key that opens that door is a set of sophisticated "what-if" simulation tools for VHDL from Vantage Analysis Systems Inc. The Fremont, Calif., startup has developed the Electronic Design Spreadsheet, VHDL-based design tools that fit seamlessly into the window-based Mentor Graphics Corp. design environment and make the little-known language disappear from view (see figure). This is a distinct advantage, because only a handful of VHDL experts understand the language and can read and write hardware descriptions expressed in it. With Vantage, the VHDL component remains in the background, transparent except when models not already in the library must be written.

The Electronic Design Spreadsheet thus makes a ready vehicle for defense-contract design, the first tool to do so within the context of a complete, integrated design environment. It also utilizes the performance advantages of highly integrated design tools and the behavioral-level simulation made possible by the presence of a library of VHDL models. A designer can check out the functionality of his board or semicustom-chip design through simulation very quickly. He can make incremental changes in his design and get it back into simulation almost as fast as a financial spreadsheet can be rejiggered and recalculated. The developers say the tools make the design environment three to ten times more productive.



VHDL is invisible to a designer using Vantage tools: he only sees his schematic and the waveforms from the simulator.

This marks a major change for electronic design simulation, which exists almost exclusively in a batch-oriented environment requiring a long sequence of steps before a changed design can be simulated. In batch-oriented environments, the schematic is checked; the netlist is expanded, generated, translated, and compiled; and the simulator is initialized and set up. Only then can simulation begin, often hours or even days after the design change was made.

The time lag is reduced to one or two minutes by Vantage's software, says Ronald Abelmann, com-

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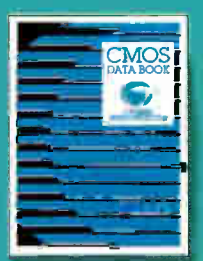

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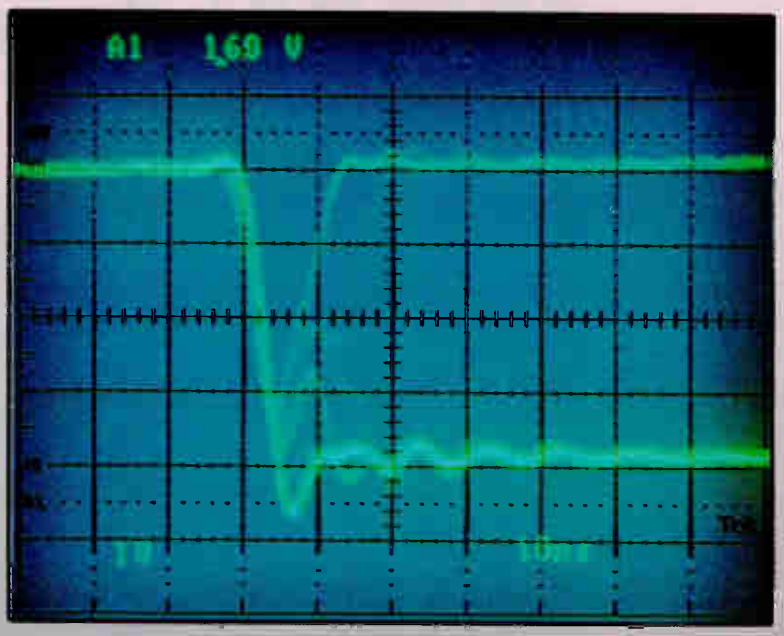

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pany president. He expects the software's impact on hardware design to be similar to that of spreadsheets in the financial community—making incremental "what-if" electronic design possible for the first time. The designer can see a waveform-based simulation display reflecting the results of a change made at the schematic-entry level almost immediately.

VHDL is an offshoot of the Pentagon's Very High Speed Integrated Circuit project; its goal is a standard to supersede the Babel of hardware-description languages used in the design of military electronic systems.

The DOD developed the first several versions of VHDL through contracts with such companies as Texas Instruments Inc., Dallas, and Intermetrics Inc. of Cambridge, Mass. The DOD's latest version, VHDL 7.2, is now being replaced by IEEE 1076. A VHDL workshop held in April at the University of Virginia marked the first time that several companies revealed work they are doing on VHDL-based tools outside of direct DOD contract efforts, says IBM's Saunders. IBM has major internal efforts to develop these tools, he adds. Also, General Electric Co. has developed a VHDL simulator. *–Jeremy Young*

APPLICATION-SPECIFIC ICs

GE IS TAKING THE FASTRACK TO CATCH UP IN ASICs

SOMERVILLE, N.J.

GE Solid State isn't happy with its ranking in the application-specific integrated-circuit market, although it's the 10th biggest supplier of standard-cell ASICs in the U.S., and 18th in gate arrays—and rising fast. So GE is adding something to its arsenal: Fastrack, a design-automation software system that ties its ASIC design tools together in a single user-friendly environment.

GE's ASIC sales totaled $57 million in 1987, according to Integrated Circuit Engineering Corp., a Scottsdale, Ariz., market researcher. GE says its CMOS standard-cell and gate-array sales were up 175% from 1986, and that it expects to continue that kind of explosive growth in the future—more than double that of the industry at large. GE's standard-cell sales hit $31 million in 1987. In gate arrays, where it is still a relative newcomer, sales were $26 million.

Enter Fastrack. Instead of offering customers basic software support for the Daisy, Mentor, P/CAD, or Valid work stations, it is making available a fully automated ASIC design system—the first of its kind, the company claims. The package will debut in Anaheim, Calif., at the Design Automation Conference, June 12-15, and will be available by the end of the year.

Based on a design-automation package licensed from EDA Systems Inc., a two-year-old Santa Clara, Calif., startup, Fastrack will expand the reach of design tools like Mimic, GE's design-simulation system. Right now only about 20% of its customers have that simulation capability, instead relying on GE to do the simulation before committing a design to silicon, says Paul Sferrazza, Solid State's manager of ASIC product marketing.

EDA's Electronic Design Management System, the core technology in Fastrack, coordinates, tracks, and controls

GE HAS A WAY TO GO

Gate arrays		Standard cells	
1987 sales in $ millions			
1. Fujitsu	420	1. AT&T	160
2. NEC	265	2. TI	91
3. LSI Logic	255	3. NCR	75
4. Plessey/Ferranti	125	4. VTI	71
5. Motorola	103	5. Toshiba	64
6. Honeywell	N/A	6. OKI	N/A
7. Toshiba	N/A	7. Int'l Micro. Products	N/A
8. Siemens	N/A	8. Mitsubishi	N/A
9. Hitachi	N/A	9. Zymos	N/A
10. AT&T	N/A	10. GE Solid State	64
⋮			
18. GE Solid State	26		

SOURCE INTEGRATED CIRCUIT ENGINEERING INC

With a total of $57 million in ASIC sales in 1987, GE trails the pack in both gate arrays and standard cells. But the company says its growth—175% since 1986—is double the industry's.

data from the various design tools—such as Vital, GE's place-and-route program, or Mimic—and presents that data to users through a graphical interface.

The result, GE hopes, is a tool that will enhance its ability to attract new ASIC customers by putting more of GE's software tools into the customers' hands. Although GE, like other ASIC vendors, offers design software for use on Apollo Computer Inc. work stations and Digital Equipment Corp. VAX minicomputers, until now it hasn't been able to provide an integrated package.

"Many of these tools have been locked pretty much on VAX VMS systems," says James Gillberg, GE's director for ASIC products. Since GE's in-house designers use VAX work stations, he adds, "historically, we've always introduced new tools or libraries on the VAX first." Three months to a year later, tool kits for use in Valid, Daisy, and Mentor Graphics work-station environments would begin to hit the market.

IN A HURRY. But customers who wanted their design completed yesterday won't wait six months for a tool to run on their work stations. They want the most powerful tools, the latest cell libraries, and the ability to create entire designs in their own engineering labs now. Fast-track, Gillberg says, is the answer.

"By encapsulating our software in EDA's [system], we can differentiate our software," Gillberg explains. "We can offer a second level of capability that's not readily available elsewhere."

Today, users cannot freely jump from one design tool to the next—they have to exit each program before entering the next. Data has to be handed off from program to program, a process that can lead to errors and delays. But by tying the programs together in one environment that includes a shared data base, a common interface, and a data-management system, GE expects to boost users' productivity and eliminate data-transfer errors. *–Tobias Naegele*

AVIONICS

THE NEXT AVIONICS COMPUTER IS LIKELY TO BE RISC

NEW YORK

The Air Force is looking for a 32-bit standard architecture for its next generation of avionics computers, and it now seems likely that the choice will be a reduced-instruction-set-computer design. Actually, the service has three options: it can design an instruction-set architecture from scratch, choose one from a commercially available microprocessor, or build on work the Pentagon has already paid for—the Defense Advanced Research Projects Agency's Core MIPS Instruction Set.

The Air Force has asked the Society of Automotive Engineers to recommend a new standard. It would succeed the current workhorse, the 16-bit 1750A, as the primary avionics computer in future airplanes, helicopters, and missiles.

The SAE's Avionics Division isn't going to sort out its options overnight, though. It will take a year or more for its task groups to provide any real results of their work, and some disagreement is already apparent. About all that is clear, in fact, is that option one, designing a new instruction-set architecture from scratch, is probably too difficult, time-consuming, and expensive, says Jim James, chairman of the SAE Avionics Processors Committee.

The second route, standardizing on a currently available commercial microprocessor, would also cause problems, says James, who is manager of avionics

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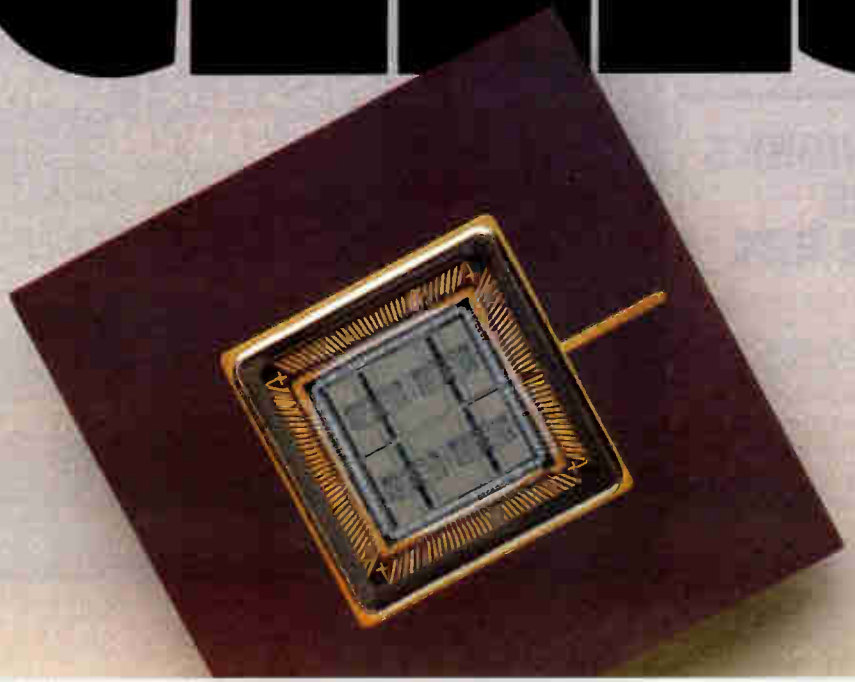

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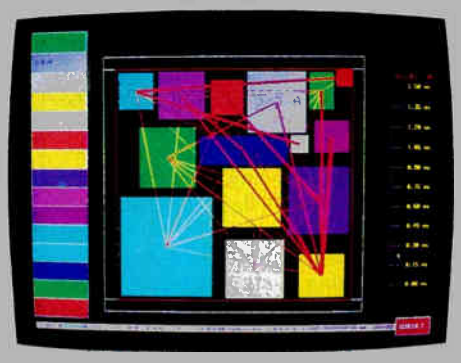

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Circle 41 on reader service card

computer architecture in the Information Sciences Division of Control Data Corp. in Bloomington, Minn. It "may be very practical, but in a group this large, I don't think we're going to get a consensus on any one vendor," he says.

That leaves MIPS, which defines a set of instructions but does not offer specifics for memory management or other functions vital to a computer architecture. Nevertheless, James says a RISC design based on MIPS is likely to be the chosen route for three reasons: flexibility, simplicity, and popularity.

Fewer instructions means more flexibility for the software programmer. And, he says, "It's a lot easier to redesign and upgrade a chip with 30,000 gates than one with 100,000 gates." The third reason is perhaps the most important: RISC technology is still relatively new and it's getting a lot of attention.

But since the Core MIPS Instruction Set is not a full architecture—it is really an interface definition, says a Darpa official familiar with the program—it will take time to define such basic elements as a memory-management scheme, says Terry Rasset, manager of advanced processors at McDonnell Douglas Aeronautics Co. in Huntington Beach, Calif. Rasset, who heads the SAE task group that is already working on that definition, promises "a draft document of a complete instruction-set-architecture standard suitable for an Ada compiler within a year."

The resulting standard would still support a variety of processors, allowing a platform from which specific systems could be optimized. "The Darpa core does everything symbolically; it defines instructions by name and function, but it doesn't say how a design must be implemented," Rasset says. So with a common interface, a single Ada compiler could be shared by any processor.

But settling on such an intermediate-level standard would mean sacrificing one of the main objectives of the 32-bit project: creating a standard that would allow machine code portability from one processor board to the next, says Paul Cook, an engineer with Ameritech Services. Cook heads the SAE task group that is considering choosing a commercial instruction-set architecture instead. However, Rasset points out that "the 1750A doesn't offer as much standardization at the spec level as some people think—there is no binary-level compatibility between 1750s."

Cook recommends choosing a commercially available design from among the four that have been offered—National Semiconductor Corp.'s 32000, Zilog Inc.'s 80000, the Clipper from Intergraph Corp., and Advanced Micro Devices Inc.'s brand-new 29000, the first pure RISC chip in the contest. He says Sun Microsystems Inc. may offer Sparc, its 32-bit RISC design.

"Accepting a commercial [instruction-set architecture] would save the government hundreds of millions of dollars and help put a real standard in use earlier," he says. "If we wait too long, 32-bit processors will be obsolete. That's what happened with the [16-bit] 1750A. It's only in the last couple of years that it's been used extensively."–*Tobias Naegele*

CONSUMER

EUROPE'S DIGITAL TV CHIP WARS GET HOT

MUNICH

The battle lines for Europe's digital-TV chip makers are drawn. In one corner are two semiconductor giants, Philips of the Netherlands and West Germany's Siemens AG. With their combined engineering savvy and marketing clout, they're ready to take on the heavyweight in the other corner: Intermetall GmbH, lead house of the ITT Semiconductors Group, which pioneered digital TV in the early 1980s and is already well entrenched in the market.

The stakes are high. Each chip set now costs up to $60, and Siemens experts figure that within half a decade about 50% of the 40 million to 50 million color TV sets made worldwide annually will be digital. So far ITT-Intermetall, with its Digit 2000 chip set, and Philips-Siemens are the only two with production chips to offer.

Siemens executives say they have an edge, especially in the high end of the market, because their set offers a better picture as well as add-on features such as videotext. By comparison, says Maximilian J. Huber, deputy in Siemens's Components Group in Munich, Intermetall "is just substituting analog with digital techniques without offering a better picture."

But Philips and Siemens are facing an entrenched foe. Since the end of 1983, when ITT-Intermetall started delivering them [*Electronics*, April 5, 1984, p. 89], the Digit 2000 chips have been used in more than 5 million color sets worldwide. "The year 1987 was the year of Digit 2000's full acceptance, when our chips entered 2½ million sets," says spokesman Reinhard Preuss. The company is now delivering chips or sending samples to some 23 set producers around the world.

Meanwhile, samples of the Philips-Siemens chips are in the hands of a dozen or so set makers in Europe, the U. S., and the Far East, says Huber. "With some, supply contracts for more than 100,000 chips have been negotiated," he says. They are now in volume production and the first TV sets using them will be in showrooms by year's end.

The two firms are offering chips that reflect their respective strengths in TV circuit design. Philips has led the effort in designing the circuits for color signal processing while Siemens has called the shots in developing those for horizontal and vertical deflection. Siemens also designed the chips that improve picture performance and provide add-on features.

The chips work with all TV transmission standards now in use—NTSC, employed in Japan and the U. S.; PAL, for most of Western Europe; and Secam, for France and most of Eastern Europe. Intermetall's Digit 2000 chip set also handles these three norms plus the new standards for direct-broadcast satellite transmissions.

Picture improvement and features are taken care of by several chips that, together with the array of dynamic random-access memories, form what Siemens calls the feature box. This unit, with its nine 256-Kbit DRAMs, now implements three features: a flicker-free picture, achieved by doubling frame frequency from 50 Hz to 100 Hz (or 60 Hz to 120 Hz for NTSC); still or freeze-frame pictures; and videotext, also flicker-free.

Siemens's feature box will provide a number of additional features without the need for more memory capacity. These are: up to nine different pictures from as many channels displayed simulta-

Cards from Philips and Siemens digitize TV color signal processing and horizontal and vertical deflection.

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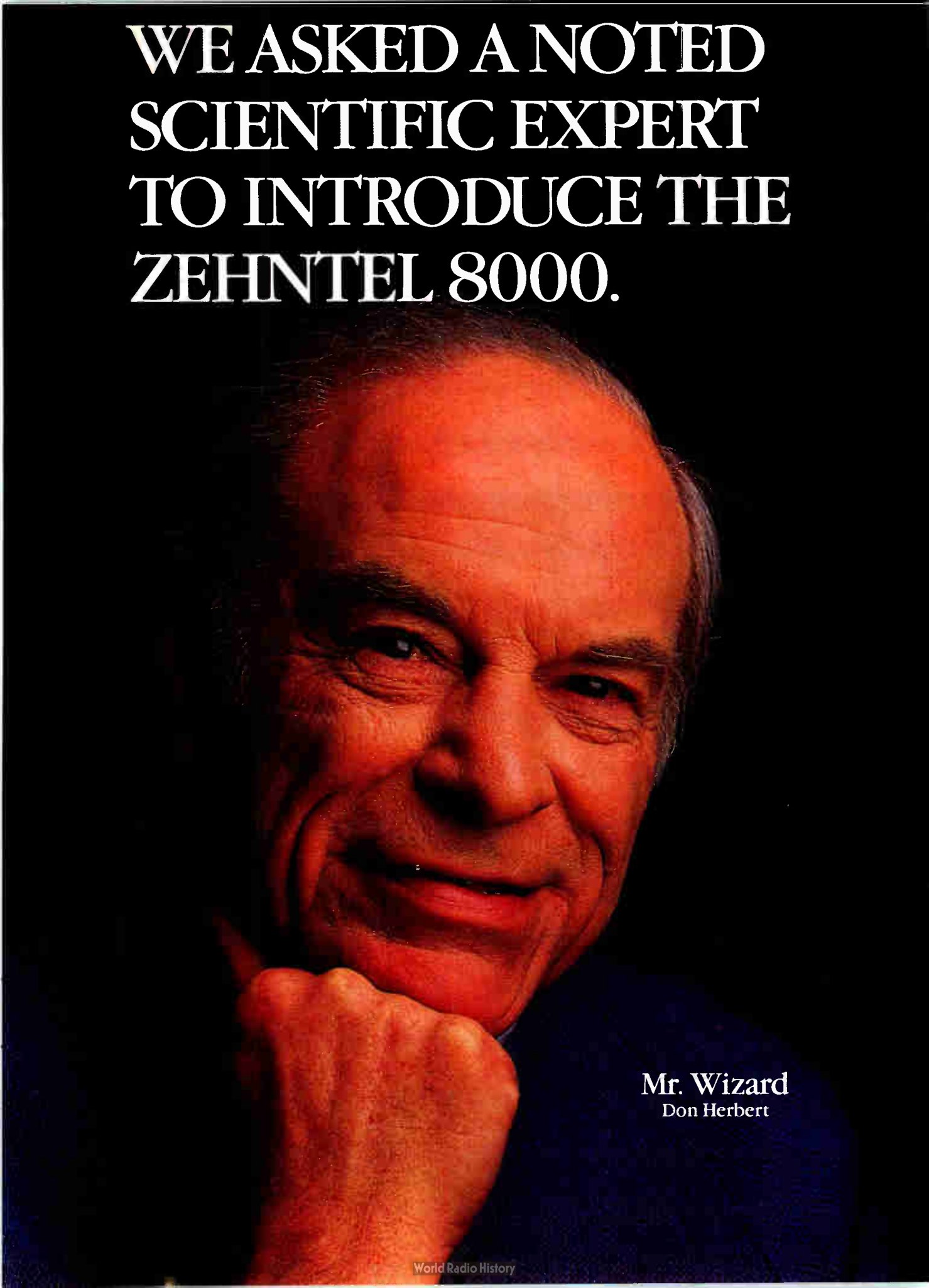

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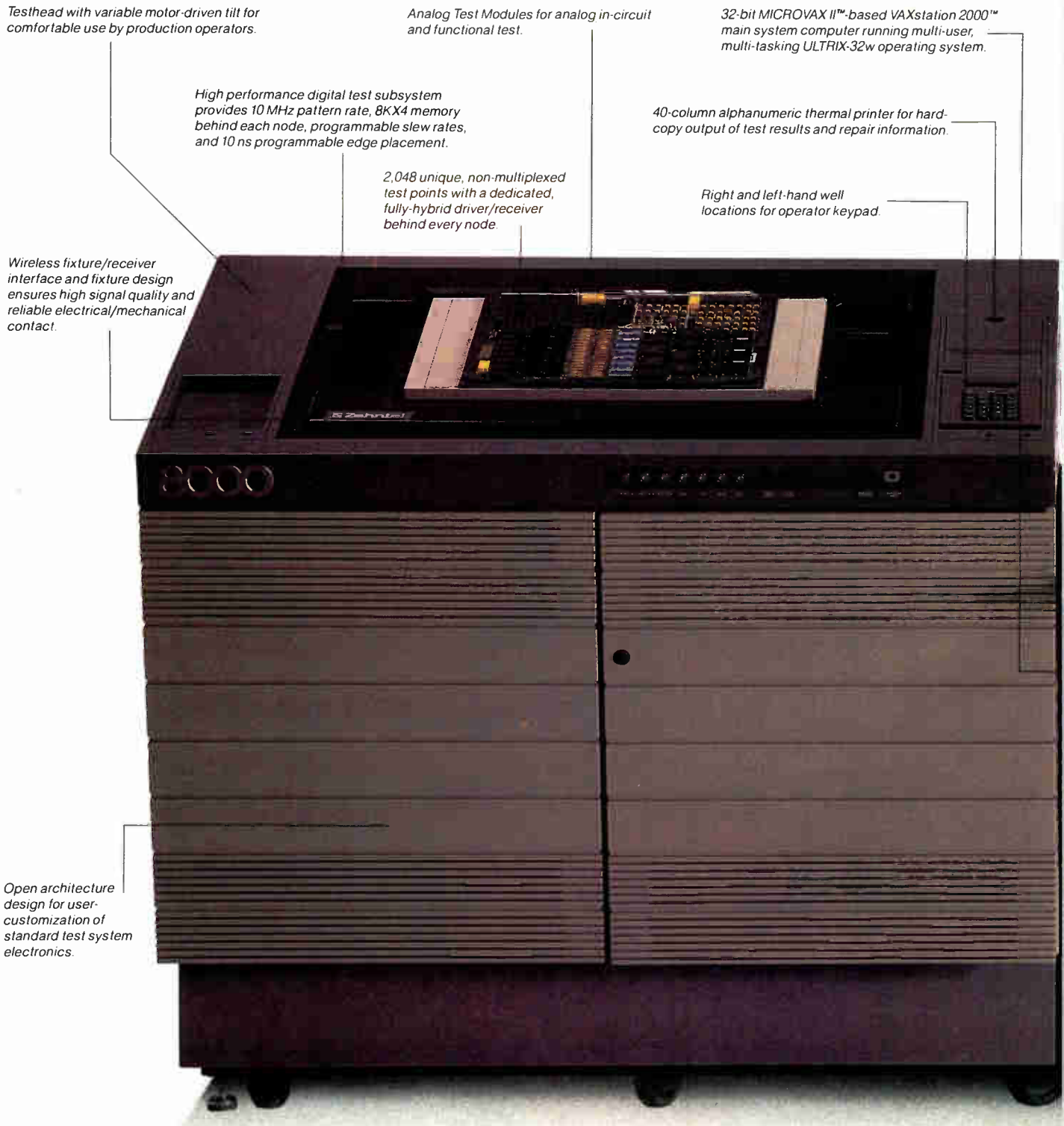

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neously on the screen for monitoring purposes, reduced picture noise (achieved by recursive filtering), and fewer cross-color effects.

Also coming are a zoom and a picture-within-a-picture capability where a small picture is displayed off to one side within the main picture. Either a still picture can be displayed in a larger moving picture, or a moving picture can be displayed in a larger still picture.

So far, the Philips and Siemens designers have found no satisfactory solution for digitizing the sound. So stereo dematrixing, pilot-tone evaluation, and volume and balance control are still handled by analog techniques. "At present, the cost to digitize these functions would not be justified by the results," Siemens's Huber says.

ITT-Intermetall, though, claims it has mastered digital sound processing but admits that it had some serious problems. "But now we have found a good solution, one that provides sound with compact-disk quality," says Intermetall's Preuss. *–John Gosch*

MILITARY

HERE'S AN AFFORDABLE WAY TO SIMULATE SDI

MANHATTAN BEACH, CALIF.

At first glance, the bank of color monitors displaying Star Wars-type graphics could be running any one of a number of popular video war games. But the flashy setup put together by Forth Inc. has a serious purpose. Called Dew-Sim, for simulating the Pentagon's proposed directed-energy weapons in a space defense network, it is destined for an important role in planning the Strategic Defense Initiative—at a down-to-earth price. And Forth executives are aggressively marketing the system for a broad range of simulation jobs ranging from traffic control to robotics.

The Dew-Sim software package, written in Forth's polyForth operating-system and programming language, models graphically the essential aspects of a realistic space battle: ground-based lasers, orbiting satellite mirrors, and incoming missiles aimed at U.S. targets. Its purpose: to evaluate many combinations of defense elements to arrive at the most cost-effective way to build SDI.

HIGH COST. Though similar packages are known to exist at some SDI contractors, say defense industry sources, they do not run in real time or boast the wealth of detail offered by Dew-Sim. Moreover, these models need elaborate programming schemes and run on big computers with six-figure price tags.

By contrast, Dew-Sim uses off-the-shelf polyForth and "conventional hardware that altogether costs less than $10,000," explains Elizabeth D. Rather, Forth's president. The system requires only an IBM Corp. PC-AT or equivalent computer, an 80287 math coprocessor, and a minimum 9 Mbytes of hard-disk storage. It drives four CGA color monitors, through commercial Tecmar graphics cards with special programmable logic to allow all four monitors to be used at once.

During simulation, graphic output is fed to the four displays simultaneously, showing the geometry of the satellites, laser beams, and target trajectories from four viewpoints chosen by the user—for example, there could be several from the U.S. vantage point, one from the attacker's side, and another over the North Pole. For evaluation, the data is archived, and exhaustive tabular

reports produced, organized in a number of ways for interpretation. A typical problem is to determine how many satellites are needed in a specific orbit to provide best coverage for a given set of ground-based lasers. Provided that the offensive-defense assumptions are not changed, various combinations can be evaluated about four times an hour.

Although the real-time graphics present a dramatic display, Rather emphasizes the intent. "Dew-Sim doesn't just draw pretty pictures, but enables SDI analysts to think about their problems and to visualize results," she says.

PolyForth's strength as an operating system designed for multiuser tasks provides the programming efficiencies required to construct an exotic system at low cost, notes Rather. Many packages with polyForth software now are used in industrial process control, robotics, and for digital signal processing. Furthermore, polyForth allows Dew-Sim to be organized so users can easily change most system parameters.

Forth's initial Dew-Sim customer is the Aerospace Operation of Kaman Corp., Arlington, Va., which is active in SDI work. A Kaman officer declines to provide details. But, says one engineer familiar with SDI programs who has seen Dew-Sim, "It's the best thing of its type I've seen." *–Larry Waller*

PACKAGING

A PACKAGE THAT'S SMALL ENOUGH FOR PACEMAKERS

LOS ANGELES

State-of-the-art pacemakers now need so many passive components for their complex analog circuitry that ordinary hybrid packages often can't fill the bill—if they're big enough to carry the components, they're too big to be implanted. But an engineer at Pacesetter Systems Inc., Sylmar, Calif., has designed just what the doctor ordered, a dual-cavity vertically integrated package.

"The [vertically integrated package] optimizes board space by nearly 2:1 and makes it possible to burn-in major components," says Alvin Weinberg, who began developing the co-fired ceramic package in early 1982 with W. Kinzy Jones, when both worked for the Cordis Corp. in Miami.

And Weinberg insists the price is right for the application. "A Japanese firm supplied them at $10 each for a batch of 5,000." Cordis pacemakers with vertically integrated packages are already in clinical trials in Europe, he says.

In the hope that the packaging concept will find takers among designers of equipment other than pacemakers, Weinberg went public with it at the 38th Electronics Components Conference in Los Angeles, held May 9-11. The package—1 in. long by 0.48 in. wide—carries an 84-pin custom integrated circuit, nine field-effect transistors, four diodes, and 50 passive components.

TOP AND BOTTOM. The chip and other parts that require hermetic protection are housed in a cavity on the bottom side. The passives cover the top side, where the heat sink would be in a conventional package of this type. Interconnections are made through five interconnect layers. Because of the interconnections, the package needs only 66 external input/output contacts.

Process flow to assemble the package is very similar to that of conventional chip-and-wire hybrids. Before dice are attached by epoxy in the cavity, they are baked for at least 15 hours to prevent epoxy from bleeding into the ceramic. Then the epoxy is cured and components in the cavity wirebonded with automatic equipment. After that, the parts are inspected visually, tested electrically, and burned-in before the cavity is sealed. Finally, the top-side components are attached and the whole assembly tested. *–Arthur L. Erikson*

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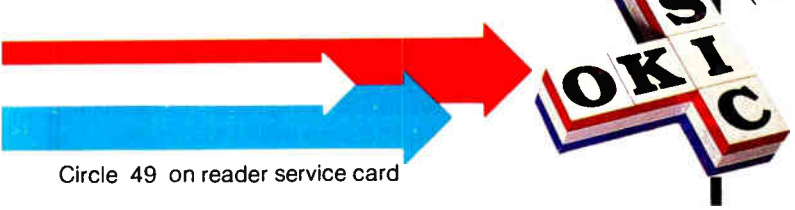

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PROBING THE NEWS

THE DRUMBEAT WILL BE ANALOG AT NEXT WEEK'S CUSTOM IC CONFERENCE

A parade of analog/digital design technologies reflect new trends at this year's show

by Bernard C. Cole

The fast-growing concern over how to simplify and speed up the design of analog and mixed analog/digital circuits will be visible in all its urgency in Rochester, N. Y., May 16 to 19 at the Custom Integrated Circuits Conference. Long a bellwether of significant trends in the semiconductor industry, this year's CICC will feature no less than 49 papers on analog and analog/digital design out of about 150 papers.

As levels of integration increase from large-scale to very large-scale integration and beyond, systems designers must concern themselves more and more with the analog aspects of a design, in addition to the digital logic and memory, says Peter Hillen, director of strategic marketing at International Microelectronic Products Inc. of San Jose, Calif. And this need comes at a time when the number of designers with an interest—let alone expertise—in the intricacies of analog circuit design is declining. The combination of these two trends is boosting the pressure to develop design tools, circuit methodologies, and special services that not only allow the experienced analog designer to be more productive but also enable the digital designer to work more easily with analog circuits.

IMP will join IBM Corp. and Exar Inc. in describing macrocell-based technology for designing application-specific integrated circuits mixing analog and digital functions at the CICC. IMP uses parasetic bipolar devices to enhance its CMOS process; IBM and Exar use full biCMOS process technology. Several other companies from around the world will present papers about computer-aided engineering tools for doing a better, faster job of analog and mixed analog/digital design—tools for block synthesis, simulation, routing, layout, and other tasks.

DATA CONVERSION. The analog and digital worlds also meet in data-conversion chips, and CICC attendees will hear about nearly 30 of them. One of the most interesting is a data-acquisition subsystem with data converters and digital signal processing on a single chip from General Electric Co., which should make the analog part of the design a much smaller task for some systems.

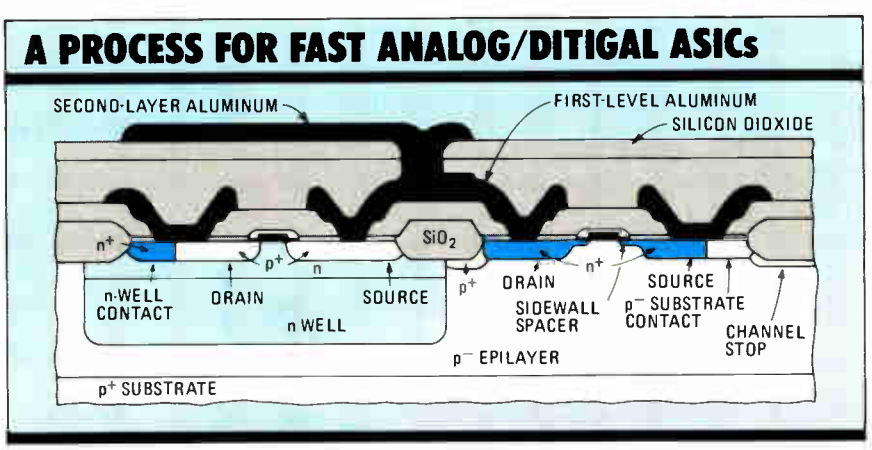
Leading off the parade of efforts to make analog and analog/digital design easier is a major effort by IMP, which chose the CICC to announce a new 1.2-μm CMOS family of analog and digital macrocells. They are the first commercially available mixed-technology library to be manufactured in a process with design rules of less than 1.5 μm (see figure). The new analog and digital cell libraries—designated DCL 1.2 and ACL 1.2, respectively—will be composed of predesigned analog and digital functions created using a architecture of cells that all have the same height but varying width, Hillen says. Containing 46 core cells and 24 peripheral cells, the DCL 1.2 library and its associated C1201 digital CMOS process will be available in May. The analog CMOS module, designated C1202, and its associated cell library, will be available in the fourth quarter.

A key element in IMP's new process is a shift from its previous p-well based process to one using n-well structures. This allows IMP designers to take advantage of the higher-quality npn structures inherent in the CMOS process. They can do this because the process allows them to build fully isolated field-effect transistors that can be used as the collectors of bipolar transistors that have separately diffused base layers. The result is the fabrication of circuits that support system clock rates as high as 40 MHz and that boast gain-bandwidth products of more than 300 MHz, according to Hillen.

Even more impressive is a 1.0-μm biCMOS mixed analog/digital standard-cell family developed for internal use by IBM's System Products Division in Rochester, Minn. Incorporating p-type resistors, MOS capacitors with n^+ backplates for higher storage, and a range of npn structures, the new family integrates analog functions with supply levels of up to 12 V on the same chip with 5-V logic. Included in the family are more than 10 classes of analog circuits, including data converters, operational amplifiers, references, and oscillators.

A/D MACROCELL PROCESS. Another biCMOS offering comes from Exar of San Jose, Calif., which will describe a modular 2-μm biCMOS process that has been used to fabricate a family of analog/digital macrocells as well as a library of electrically erasable programmable read-only memories.

CICC papers also describe numerous new tools for making analog and mixed analog/digital design easier. Addressing the difficulties of designing analog/digi-



Predesigned analog and digital functions can be combined easily on high-speed semicustom chips built by International Microelectronics Products in its 1.2-μm n-well CMOS process.

tal circuits with high voltage requirements, for example, General Electric researchers from Schenectady, N. Y., will tell attendees about a new compilation technique that incorporates the synthesis of analog functional blocks as well as the physical assembly of mixed analog/digital circuits. Typical analog blocks that can be compiled using the technique are op amps, comparators, bandgap references, and voltage-controlled oscillators, all of which can be referenced at up to 500 V with respect to the p-type substrate.

MIXED SIMULATION. Another tough problem facing designers is the simulation of a chip containing both analog and digital blocks. There are two approaches that are normally used: the user either simulates the two blocks separately and assumes they will work together, or he models the behavior of the analog and digital functions and simulates them together on a single digital simulator. Designers at AT&T Bell Laboratories in Murray Hill, N. J., propose the use of two specialized simulators, a circuit simulator to simulate the analog portion and the use of a switch-level simulator for the digital portion.

Looking for better ways to implement mixed analog/digital designs, researchers at North Carolina State University in Raleigh will describe a two-layer channel routing algorithm that takes into account capacitive coupling between analog and digital networks on the same or adjacent layers, a significant design hurdle in present designs.

Evident at the CICC is a lot of activity outside the U. S. in the field of mixed analog/digital tools. Researchers from Beijing University in the People's Republic of China will describe Mixmod, a program that models the dynamic behavior of functional blocks using macromodels. Two papers from Switzerland discuss design tools falling in this category. One, from the Swiss Federal Institute of Technology, Lausanne, is a layout-generation tool called Salim, which integrates both expert-system and algorithmic features, either interactively or automatically. The other is ILAC from the Centre Suisse d'Electronique et Microtechnique in Neuchatel. It is a process-independent layout tool for analog CMOS circuits that works from net-list information, similar to methods used for digital design, and subject only to constraints on cell bounds and input/output locations.

Engineers from AEG AG's research center in Ulm, West Germany, will describe a sophisticated hierarchical cell-based system for the design of semicustom analog circuits for standalone use or for incorporation into mixed analog/digital designs. The system's functions include schematic capture, circuit simulation, layout, and verification. The paper's authors have built a 4,000-gate master array with the system and fabricated it using a proprietary bipolar process, the company says.

As data-conversion devices get more sophisticated, they are making the analog side of mixed designs easier for the majority of engineers, whose training falls on the digital side of the border. One of the most sophisticated chips described at the CICC pushes toward the ultimate goal of integrating a complete analog/digital subsystem on a chip. It is a multichannel data-acquisition chip from General Electric of Schenectady, N. Y., with on-chip digital-signal-processing circuitry. It is composed of three delta-sigma analog-to-digital converters with 11-bit resolution and an oversampling rate of 3.58 MHz. The chip's 32-bit DSP engine uses a fixed-point 2's-complement format and performs low-pass filtering, accumulation, data selection, and comparison.

There are many other mixed analog/digital chips on the menu at the CICC:

New tools promise faster design of better analog and mixed analog/digital circuits

four sessions and 26 papers are devoted exclusively to such designs. Among the most impressive is a 100-MHz pipelined CMOS comparator for flash conversion from Stanford University in Palo Alto, Calif. It uses pipelined-cascade regenerative-sense amplifiers and offset cancellation to achieve high accuracy.

Other significant data-conversion offerings include a quad 12-bit digital-to-analog converter with software control, mode control, and readback functions on chip from Analog Devices Inc. of Wilmington, Mass.; a three-stage pipelined flash ADC from IMP that achieves 12-bit accuracy and 1-MHz sampling by making use of high-speed offset-cancelled op amps and comparators; and a two-step flash ADC from Crystal Semiconductor Corp. of Austin, Texas, that achieves 12-bit accuracy and 1.5-MHz throughput using a switched-capacitor integrator and 66 sample-and-hold amplifiers.

An alternative approach comes from the University of California at Berkeley, where researchers have developed a 10-bit two-step flash CMOS ADC that operates at 1 MHz using a resistor-string, capacitor-array architecture. A CMOS circuit from Toshiba Corp., Kawasaki, Japan, features a new successive-approximation ADC architecture that combines 10-bit accuracy with a 5-μs conversion rate. And from Xerox Corp., El Segundo, Calif., comes a simple pipelined quasi-passive CMOS DAC, which features a 330,000-sample/s throughput and 11-bit accuracy. □

INTERNATIONAL NEWSLETTER

VALVO PUTS ITS CHIPS ON CONTACTLESS SMART CARD THAT NEEDS NO BATTERY...

Valvo has brought a new twist to smart-card technology with a card that has no contacts to wear out and no battery to run down. The 0.76 mm-thick, credit-card size device employs inductive techniques to feed energy from a read-write module to the card and to transfer data from the card to the reader. The Hamburg, West Germany, components-producing affiliate of Dutch electronics giant Philips, based its card on an idea of a small German electronics firm, Angewandte Digital Elektronik GmbH, Brunstorf. Valvo officials say their card differs significantly from an earlier one from AT&T Corp., which employs capacitive methods for data transfer and inductive methods for energy coupling. Also, they point out that the AT&T card does not meet the norms laid down by the International Standards Organization, as Valvo's does. □

...AND SGS-THOMSON DEALS ITSELF A STRONGER HAND IN SMART CARDS

SGS-Thomson Microelectronics plans to bolster its already-strong position as a major supplier of chips for smart cards by backing a French startup that will produce a range of smart cards plus the necessary terminal equipment, software, and systems services. Other players in the deal include Innovatron Smart Card Venture NV, which holds key patents on smart cards; Ingenico SA, a leading point-of-sale terminals maker; and three venture-capital companies. The as-yet-unnamed company, temporarily based in Aix-en-Provence, has set revenue goals of 45 million francs (roughly $8 million) by the end of 1988 and 110 million francs ($19 million) by the end of 1989, which works out to 6 million modules and 10 million finished cards. The startup will be headed by Marc Lassus, formerly the general manager of SGS-Thomson's MOS division. □

NTT DIGITAL MICROWAVE MATCHES FIBER-OPTICS TRANSMISSION CAPACITY

Don't write off microwave links for heavy telecommunications traffic yet. Nippon Telegraph and Telephone Corp. plans to install later this year a digital microwave communications system with the same capacity as present optical cable. The new system will be able to transmit 400 Mbits/s—double the capacity of NTT's current large-capacity microwave systems. Based on a 256 Quadrature Amplitude Modulation method developed by NTT in which a transmitted symbol represents 8 bits, the system has managed to span more than 50 km without repeaters in experimental transmissions in the 4-, 5-, and 6-GHz bands. The Tokyo-based carrier will first use the new system to supplement the optical cable network installed between Tokyo and Osaka, via Nagoya, and later extend it nationwide. Modulation and demodulation systems will be supplied by NEC Corp. and Fujitsu Ltd. □

EAST GERMANS EYE CAD/CAM MARKETS IN WESTERN EUROPE

East Germany's data-processing-equipment organization, VEB Kombinat Robotron, intends to make its mark in Western European markets with its computer-aided design and computer-aided manufacturing systems. The Dresden-based, state-owned combine scored sales of $25 million in West Germany last year, mainly from measuring equipment and office gear like electronic typewriters and printers, and now is convinced it can move upscale to CAD/CAM systems with competitive hardware and an extensive repertoire of software. Robotron shipped well over $1 billion worth of data-processing equipment to the Soviet Union and may take on a West German partner to get its computer sales to take off in that country. Robotron, a 70,000-employee organization, runs 20 manufacturing facilities across East Germany. □

INTERNATIONAL WEEK

JAPANESE TO DOUBLE 1-MBIT DRAM OUTPUT

Japanese chip makers plan to at least double their production of 1-Mbit dynamic random-access memories by year's end. Mitsubishi Electric Corp., Tokyo, will boost production to 3.5 million units a month from 1.5 million and Hitachi Ltd., Tokyo, will expand to 4 million units from 2 million. Oki Electric Industry Co., Tokyo, and Fujitsu Ltd., Tokyo, each now producing 1 million units a month, will also double output. Meanwhile, Toshiba Corp., Tokyo, which now ships 5 million a month, will go to 6 million during July, probably hitting 7 million by the year's end.

OLIVETTI PONDERS 88000 VS. SPARC . . .

The April 28 appointment of Vittorio Cassoni, head of AT&T's Data Systems Group in the U. S., as Olivetti's new group managing director comes at a time when the Ivrea, Italy, company must decide which work-station standard it will adopt. Tension with AT&T over Olivetti's proposed LSX line centers on the choice between Motorola Inc.'s 68900 and 88000 superchips versus AT&T/Sun Microsystem Inc.'s new Sparc chip. AT&T, which owns 20% of Olivetti, has denied trying to impose the Sparc but its objectives are obvious. Olivetti is insisting on independence, say insiders.

. . . WHILE BUYING A NORWEGIAN FIRM

In a move designed to strengthen Olivetti's position in minicomputers and integrated Unix systems, the Italian company has spent about $75 million for a 51% stake in Norway's Scanvest Ring A/S, a leading Scandinavian information technology group. Scanvest Ring includes SRC, a PABX power; SRD, a Norwegian-based systems integrator; CLS of Sweden, a Unix systems house; SMS, a Danish systems integrator; and Kitron, a Norwegian producer of electronic components and communications equipment. An associated company, NCI, is a Norwegian producer of Unix-based minicomputers sold both in Scandinavia and in the U. S.

PC OUTPUT DIPS FOR FIRST TIME IN JAPAN

Annual production of Japanese personal computers has decreased for the first time since 1981. Japan's Electronic Industry Development Association reports 1987 output at 2.06 million units, a 4% decrease from the previous fiscal year. Domestic shipments, which account for almost two-thirds of the overall output, decreased by 3% and exports decreased 6%. But the total value of PC equipment—including peripherals—showed an increase of 22% for the domestic market. The export value grew only 3% because trade sanctions halted exports of 16-bit machines to the U. S.

PHILIPS TUBES MEET RADIATION STANDARD

Philips of the Netherlands has developed a family of gamma-radiation-measuring Geiger-Müller tubes. The Eindhoven-based company claims the tubes are the first to meet new standards for ambient-dose equivalent specified by the International Commission on Radiological Protection. The four tubes cover a dose-rate measuring range from 10 $_3$ to 20,000 milli-gray/hr. The polar response is almost constant over 360°, ensuring accurate radiation detection regardless of source radiation direction.

SIEMENS INSTALLS FIBER-OPTIC NET

In a major move toward implementing the West German Bundespost's planned fiber-optic-cable network, Siemens AG has installed the country's first 565-Mbit/s tranmission systems. The lines will handle traffic over three key links in southern Germany: between Karlsruhe and Stuttgart (50 miles); Munich and Ulm (90 miles); and Munich and Nuremberg (120 miles). The links will be part of West Germany's nationwide digital communication network for telephone and broadband services such as video conferences and high-definition TV.

EUROPE'S R&D TEAM GETS MORE FUNDING

The second stage of the European Community's research and development program, Esprit 2, has been formally endorsed by the EC's research ministers. Some £1 billion will spent on collaborative information technology research by 1992, and an equal amount will be spent by participants. In addition, £120 million has been allocated to promote cooperation among scientists in the EC and £40 million for research in European high technology standards, this in preparation for the European Single Market in 1992.

STEP TAKEN TO OPEN JAPANESE IC MARKET

Japanese semiconductor purchasers will form a committee in Tokyo on May 17 to help foreign chip makers gain better access to the Japanese market. Foreign chips account for about 12% of the Japanese market at the present time. About 70 users including major manufacturers such as Hitachi, Mitsubishi, NEC, and Toshiba will join the committee. The Ministry of International Trade and Industry has been the driving force for setting up the committee within the Electronic Industries Association of Japan to share views with U. S. and European chip makers and systems integrators.

FUJITSU TO SELL ISDN GEAR IN U. S.

Fujitsu Ltd. will be the first Japanese firm to supply products for Integrated Services Digital Networks in the U. S. Its San Jose, Calif., subsidiary has agreed to supply U. S. West Information Systems Inc., Denver, Colo., with ISDN terminals, digital telephones, and adapters for use under its own brand name starting in June. Fujitsu plans to sell $10 million worth of ISDN products to U. S. West Information Systems over three years.

UK SHIFTS GaAs POLICY AFTER REBUFF

Despite dismay that its £25 million offer to establish a gallium arsenide foundry in the UK was rejected by Plessey Co. plc [*Electronics*, April 28, 1988, p. 38], the British government says it still intends to promote the technology—but at reduced funding. The Department of Trade and Industry will encourage collaborative ventures including the development of demonstrator systems. Universities and small startups will select which existing UK GaAs foundry they wish to use. But the choice is practically limited to Plessey's full commercial foundry or a pilot line at General Electric Company plc's fab.

BUYOUT GIVES H&B A U. S BASE

West Germany's Hartmann & Braun AG has purchased Applied Automation Inc. of Bartlesville, Okla., from Phillips Petroleum Co. The purchase adds process-optimizing systems, flow-through measuring equipment, and process chromatographs to Frankfurt-based H&B's equipment lineup and also strengthens the German firm's U. S. market position. The deal must be approved by antitrust authorities in both countries.

INTERNATIONAL PRODUCTS

PHILIPS' DIGITAL SCOPE HANDLES 2-GHz SIGNALS AND IS EASY TO USE

Fast enough for GaAs, the PM3340 also features automatic measurement settings

A digitizing oscilloscope from Philips boasts a signal-acquisition and measurement capability of up to 2 GHz—twice the bandwidth of oscilloscopes now on the market, according to the Dutch company. The PM3340's bandwidth results in rise times as short as 175 ps, fast enough to handle practically any high-end measurement, including the debugging of most gallium arsenide circuits.

The PM3340's functions are software selectable, and as many as 250 front panel settings can be stored for instant recall.

Philips's designers coupled the scope's speed with features—such as automatic measurement settings—that make it as easy to use as a less sophisticated scope. "Although it is a high-performance instrument, it handles like any conventional lower-frequency scope," says Gary Burgess, a product manager at the Philips Industrial and Electroacoustic Systems Division in Eindhoven.

SAMPLING. The 3340 owes its large 2-GHz bandwidth to the sequential sampling technique, says Andreas Lüttgering, marketing manager for oscilloscopes at Philips's instruments subsidiary in Kassel, West Germany. This contrasts with random sampling used in most other digitizing scopes.

In sequential sampling as the Dutch designers have implemented it, one sample point is taken on each sweep to build up the waveform on the display. Without being amplified, the input signal is fed directly to a sampling gate consisting of two high-speed Schottky diodes. Only after being transformed in that gate and amplified and analog-to-digital converted in subsequent circuitry is the signal applied to the display.

For all its measuring power, the 3340 is as convenient to operate as a less sophisticated oscilloscope. That's because of features such as autoset and trigger auto-select. The autoset key automatically sets acquisition and display parameters for any input signal.

The auto-select facility automatically selects the most suitable of the scope's three trigger modes—normal, countdown, and synchronized triggering—for any type of input signal. The instrument's 2-GHz triggering performance allows the available bandwidth to be used right up to its limits for all practical measurements.

The scope's functions are selected by way of softkeys, with on-screen menus showing the available options. As many as 250 front panel settings can be stored for instant recall whenever required. This eliminates the need for frequent manual entry of standard set-ups. The instrument provides automatic operation—for example, for repetitive measurement routines—without the need for a separate controller or computer.

The 3340 simultaneously measures, analyzes, and stores two recurrent input signals from 1 mV upward. Its 10-bit vertical resolution, coupled with 512 measuring points along the time axis, ensures high-accuracy measurements. That makes the unit ideal for checking devices such as those based on emitter-coupled logic, CMOS, and gallium arsenide technologies—the kind of devices used, for example, in digital communications, radar, laser research, satellite broadcasting, and data links.

Another significant feature of the 3340 is its high dynamic range, Lüttgering says. It helps make signal analysis easier by allowing signals greater than 1 V to be examined on a scale of 1 mV per division. The resulting noise at this magnification is suppressed by the instrument's "running-average" mode, a mode that shows even the small test signal details as a sharp and clean display.

Along the time axis, pre- and post-triggering allow signals to be displayed both before and after the moment of triggering. The signal prior to and directly after a particular event can then be observed.

The 3340 marks Philips's entry into the gigahertz-performance oscilloscope market. Other models in the firm's line-up of digital scopes start at 50 MHz and cover virtually all requirements for digital signal acquisition and measurement. With its new high-end model, the Dutch electronics giant is aiming squarely at the best that U. S. and Japanese companies can offer, the company says.

According to Burgess, the potential world market for sampling oscilloscopes with gigahertz capability amounted to 3,500 units in 1987. He forecasts the new 3340 will account for a 20% share of the market this year. In 1989, when the global demand for high-end sampling scopes should reach 5,000 units, it will account for a much bigger share, Burgess says.

FOUR REGISTERS. The 3340 has a total of four signal registers in which up to eight signals can be stored. All eight can be simultaneously displayed on the cathode-ray tube's 10-by-12 cm screen. The screen's division into signal, parameter, and softkey fields makes it easy to evaluate the display.

The new instrument offers a number of dedicated processing modes to allow extra information to be obtained from the signals acquired. For example, the "eye-pattern" mode serves to test digital communication signals. Voltage histograms can be produced to show amplitude probability. This allows observing a signal's noise distribution.

In addition to signal analysis in the time domain, analysis in the frequency domain is made possible by a fast Fourier transform facility. Another capability is offered by the save/stop-on-difference-function. This function allows any

input signals differing from a stored reference signal to be detected and stored in memory for later analysis.

Once signals have been acquired, a range of advanced measuring functions is available to determine any selected voltages, amplitudes, and time intervals, as well as standard parameters like peak-to-peak and root-mean-square voltages and risetimes. Mathematical functions such as signal addition, subtraction, multiplication, differentiation, and integration are standard.

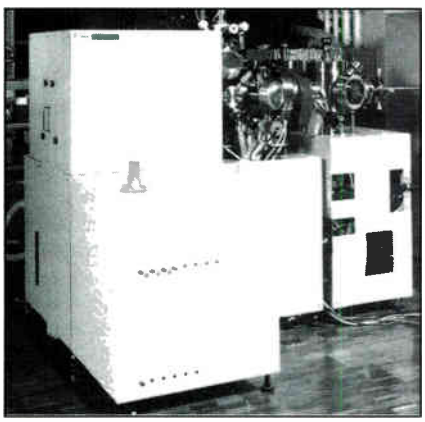
Standard built-in IEEE-488 and RS-232-C interfaces make the 3340 suitable for use in quality control and automatic test equipment environments. Complete computer control and downloading of measurement data for further processing is also possible. Hard-copy output of displayed signals and measurement parameters can be obtained using standard plotters or printers.

The delivery time for the PM3340 is from four to eight weeks. It sells for 34,450 DM. – *John Gosch*

Philips I & E Systems Div., Building HKF, NL-5600 MD Eindhoven, the Netherlands.
Phone 31-40-788620 [Circle 500]

ION-DEPOSITION SYSTEM TARGETS GaAs CHIPS

Anelva Corp.'s UHV-ECR series of ion-deposition equipment targets applications in gallium arsenide and high-illuminance semiconductors that are used for laser techonology by using an ultra-high vacuum, or UHV, environment for elec-



tron-cyclotron resonance, or ECR, technology.

By combining the two technologies, the UHV-ECR series delivers high quality epitaxial film growth and etching with steep profile. The ECR ion source produces a stable, highly ionized plasma, which results in high-speed thin-film fabrication and improved repeatability.

The ultra-high vacuum is implemented by a 550-liter turbomolecular pump that can realize a vacuum of 10^{-9} Torr.

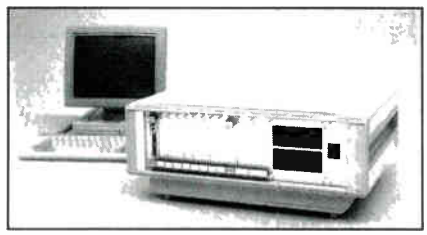
Available now, models of the UHV-ECR series vary in price according to customer configuration; a representative export price is about $580,000.

Anelva Corp., 5-8-1 Yotsuya, Funchu, Tokyo 183, Japan.
Phone 81-423-64-2111 [Circle 701]

VME DEVELOPMENT SYSTEM TARGETS 68000

BICC-Vero Microsystems Ltd.'s VME OS-9/68000 development system for single-board computers based on Motorola Inc.'s 68000 microprocessor provides eight expansion slots to accommodate a wide range of add-on boards for specialty applications.

For use with single-height VMEbus



boards, the system uses the OS/9 operating system and includes a 10-MHz microprocessor, a high-speed, direct-memory-access disk controller connected to a 20-Mbyte hard disk, 512 Kbytes of dynamic random-access memory, and a 1-Mbyte floppy disk.

The OS/9 operating system incorporates a C complier, editor assembler, and other utilities. The complete development system is available now for £3,550.

BICC-Vero Microsystems Ltd., Flanders Road, Hedge End, Southampton, S03 3LG, UK.
Phone 44-703-266300 [Circle 704]

VMEBUS INTERFACE CARD MEETS MILITARY SPECS

DY-4 Inc.'s SVME-653 VMEbus interface card conforms to MIL-STD 1553B and offers dual redundant interfaces, a bit-slice processor for message processing, and 64 Kbytes of dual-port memory.

On-board firmware allows users to configure the SVME-653 as either a bus controller or as a remote terminal simply by initializing.

Data exchange areas are allocated for transmissions and receptions within the dual-ported memory. The location of the data exchange areas is programmable by the host, as is the size and number of buffers in each area.

The board targets the relatively new market for airborne VMEbus applications and makes the use of VMEbus attractive for any system using the MIL-STD 1553B serial bus.

The SVME-653 is available now. Price depends on importing country and quantity purchased.

DY-4 Systems Inc., 21 Credit Union Way, Nepean, Ontario, Canada.
Phone 613-596-9911 [Circle 703]

CABLE SPLICER DOES 400 CONNECTIONS/HOUR

The Type SEK mechanized work station from Harting Elektronik GmbH connects two cables in one operation without a previous stripping operation. It boasts a minimum throughput of approximately 400 connections/hr.

The station has two trays for connector magazines as well as modular connector holding tools. A feed table has an electrically driven press, and the movement of the table automatically initiates the press operation. Exact guidance of cables permits quick and easy insertion of the cable into the connector.

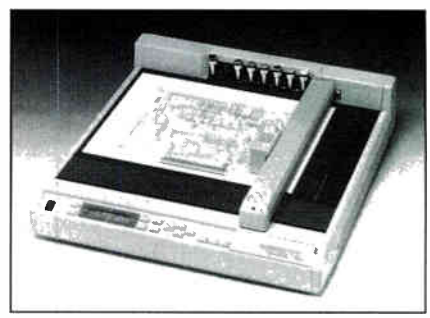
To customers using Harting connectors, the Type SEK work station is made available free of charge. It can be ordered now.

Harting Elektronik GmbH, P.O. Box 1140, D-4992 Espelkamp, West Germany.
Phone: 49-5772-47244 [Circle 702]

PEN PLOTTER OFFERS 64-CM/S OPERATION

The FP6302 pen plotter from Graphtec Corp. features a servo drive controlled by a 16-bit microprocessor, which allows the device to attain plotting speeds of up to 64 cm/s.

The plotter uses a wide variety of pen types in up to 24 colors. Automatic pen-up, pen-return, and pen-capping prevent ink clogging and drying. The FP6302 can be interfaced with virtually any host



computer through its standard RS-232-C/Centronix interface. It also offers the RS-488 interface and Graphtec's own GP-PL interfaces as options.

Maximum plotting area is 420 by 297 mm, which is suitable for both DIN A3/A4 and ANSI B/A size plotting papers. The FP6302 is available now. Price depends on importing country.

Graphtec Corp., Mori Building, 13-16, Mita 3-chrome, Minato-ku, Tokyo, 108 Japan.
Phone 81-3-453-7187 [Circle 705]

MULTIMETER HANDLES 320-KHz MEASUREMENTS

The low-cost digital multimeter Digavi 3 from Hartmann & Braun AG delivers the functionality normally found only on midrange and high-end multimeters. Be-

sides measuring dc and ac voltages up to 650 V, dc and ac currents up to 10 A, and resistance from 0.1 Ω to 32 MΩ, the Digavi 3 measures frequencies from 40 Hz to 320 KHz.

Other functions include continuity checks and semiconductor testing. Overload protection is provided for all measuring ranges. Measured values are indicated on a liquid-crystal display. The instrument switches off automatically one hour after not being used, which helps save battery power.

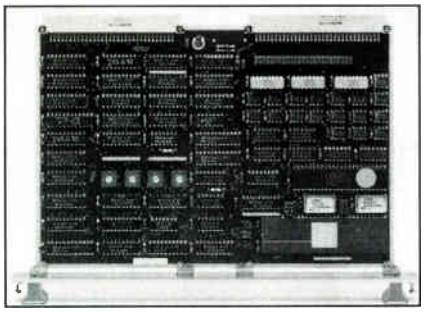
The Digavi 3 is available from stock and sells for 250 DM.

Hartmann & Braun AG, Gräfstr. 97, D-6000, Frankfurt 90, West Germany.
Phone: 49-69-7992403 [Circle 706]

BOARD TRIPLES RANGE OF SCSI BUS TO 25 METERS

Compcontrol BV's CC-174 VMEbus board extends the range of the Small Computer System Interface from seven to 25 meters by using differential output drivers.

The board works in multiprocessor systems and uses Motorola Inc.'s 68450 high-performance direct-memory-access controller as well as NCR Corp.'s 5386 SCSI protocol controller. It transmits at



data rates up to 1.5 Mbytes/s (asynchronous) and 4 Mbytes/s (synchronous).

DMA transfers can be input/output-to-memory, memory-to-I/O, or memory-to-memory. It can mix byte and word transfers on the VMEbus and can also be used by a random-access memory disk subroutine.

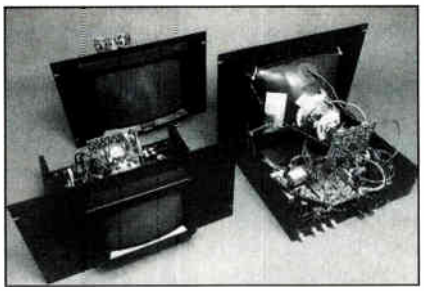
The CC-174 is available now at an export price of about $1,775.

Compcontrol BV, Stratumsedijk 31, P.O. Box 193, 5600 AD, Eindhoven, the Netherlands.
Phone 31-40-124955 [Circle 707]

COLOR MONITOR LINES HAVE MODULAR DESIGN

A series of rack-mountable color monitors from Centronic Ltd. comes in three sizes: 9, 12, and 14 in. in diameter. All feature a modular design to keep component count low and to increase system reliability.

The 14-in. model is available with medium, high, or super-high resolution. All



models have versions that vary from 15- to 35-KHz scan lines. The rack-mounting system includes a rack, compatible faceplate, carrying tray, and front bezel.

The rear of the carrying tray is prepunched for several interconnection options. The monitors are available now. Prices start at £550.

Centronic Ltd., Information Systems Div., 275 King Henry Dr., New Addington, Croydon, CR9 0BG, UK.
Phone 44-689-47911 [Circle 708]

HARD-DISK MODULES ARE ONLY 1-INCH HIGH

Alps Electric Co. Ltd.'s 20-Mbyte and 40-Mbyte DRP/DRQ series of 3½-in. disk-drive modules are only 1 in. thick. The slimmer profile targets a growing demand for more compact personal computers.

The single disk DRP020A stores 20 Mbytes and offers an access time of 75 ms. The double-disk DRQ040A stores 40 Mbytes and offers an average access time of 45 ms.

Both drives weigh 550 grams. The 20-Mbyte drive consumes 4.59 W; the 40-Mbyte drive, 4.95 W. An embedded Small Computer Systems Interface controller is available as an option.

The drives are available now. Price depends on importing country.

Alps Electric Co. Ltd., 1-7 Yukigawa Otsukacho, Ota-ku, Tokyo 145, Japan.
Phone 81-3-726-1211 [Circle 709]

OP AMP DISCONNECTS ITSELF INDEPENDENTLY

The power operational amplifier TCA1365B from Siemens AG combines free-running diodes and an "inhibit-input" feature on one chip. It handles peak currents of 4 A.

The inhibit-input function selectively switches off the op amp without the need to shut down other loads or the line power. The TCA1365B can be used as a switch in dc motors rated at up to several dozen watts that are installed in ventilators and in cars for windows and sliding roof motors.

The TCA1365B is available as samples now. Price will be given on request.

Siemens AG, P.O. Box 103, D-8000 Munich 1, West Germany.
Phone: 49-89-41448080 [Circle 710]

IMAGE SENSORS FORM SEAMLESS ARRAYS

By designing the input/output connections on just one side of its TH X31157 full-frame image sensor, Thomson-CSF lets users form the large area arrays that are needed in military and astronomy applications.

Based on charge-coupled-device technology, the X31157 chip contains 579 rows of 400 pixels, each measuring 23 by 23 μm. All charge transfers are in buried-channel mode, with four driving clocks for the photosensitive area and two for the output register.

The integrated circuits come glued to a ceramic substrate with an overhang on the three buttable sides. Circuit access is by a flexible pc board soldered on the ceramic connections.

The X31157 is available now. Price varies with importing country.

Thomson-CSF, Electron Tube Division, 29 Rue Vathier/BP 305, 92102 Boulogne-Billancourt Cedex, France.
Phone 33-46-03-46-85 [Circle 711]

CONTROLLER DELIVERS 4-MBYTE/S TRANSFERS

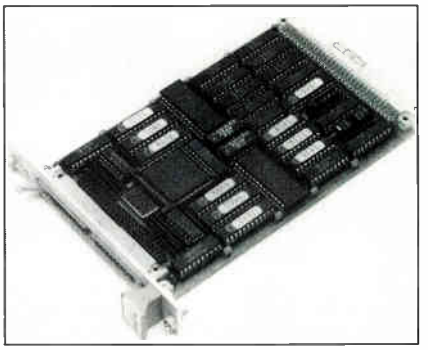
A new VMEbus single-height controller module from PEP Modular Computers GmbH transfers data at up to 3 Mbytes/s asynchronously. It also boasts a synchronous transfer rate of up to 4 Mbytes/s.

The VSCSI module acts as an interface for SCSI peripherals such as Winchester drives, floppy drives, streaming tape drives, printers, scanners, and optical disk drives. It allows multitasking functions within the input/output subsystem.

When a command is received, the I/O devices disconnect themselves from the SCSI bus while performing an operation. This leaves the bus free to handle other I/O operations while the peripherals perform lengthy tasks.

Delivery of the VSCSI module takes about 4 weeks. Price depends on importing country but is 1,450 DM in Germany.

PEP Modular Computers GmbH, P. O. Box 1652, D-8950 Kaufbeuren, West Germany.
Phone 49-8341-81001 [Circle 713]

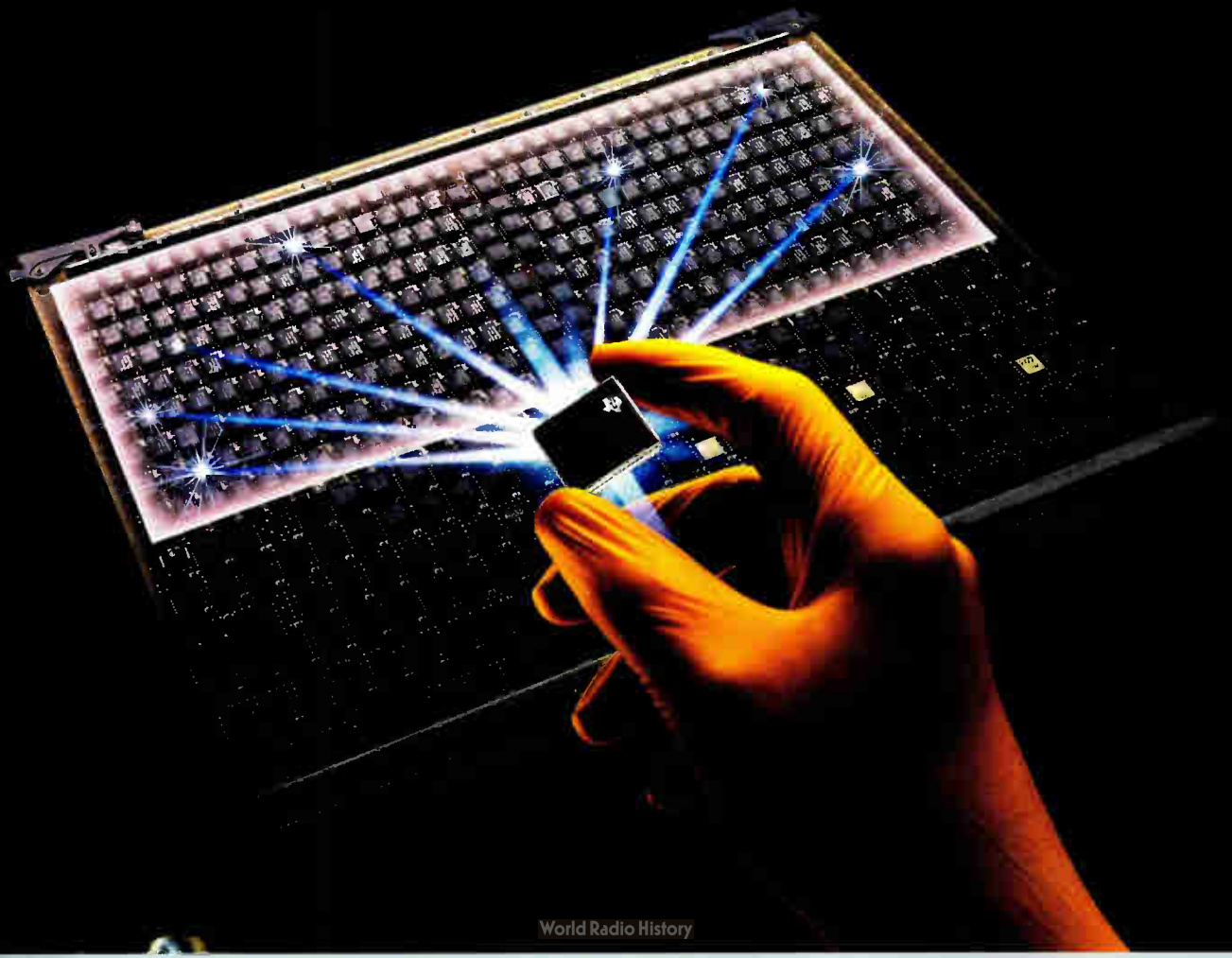


TEXAS INSTRUMENTS REPORTS ON

MEMORY MANAGEMENT

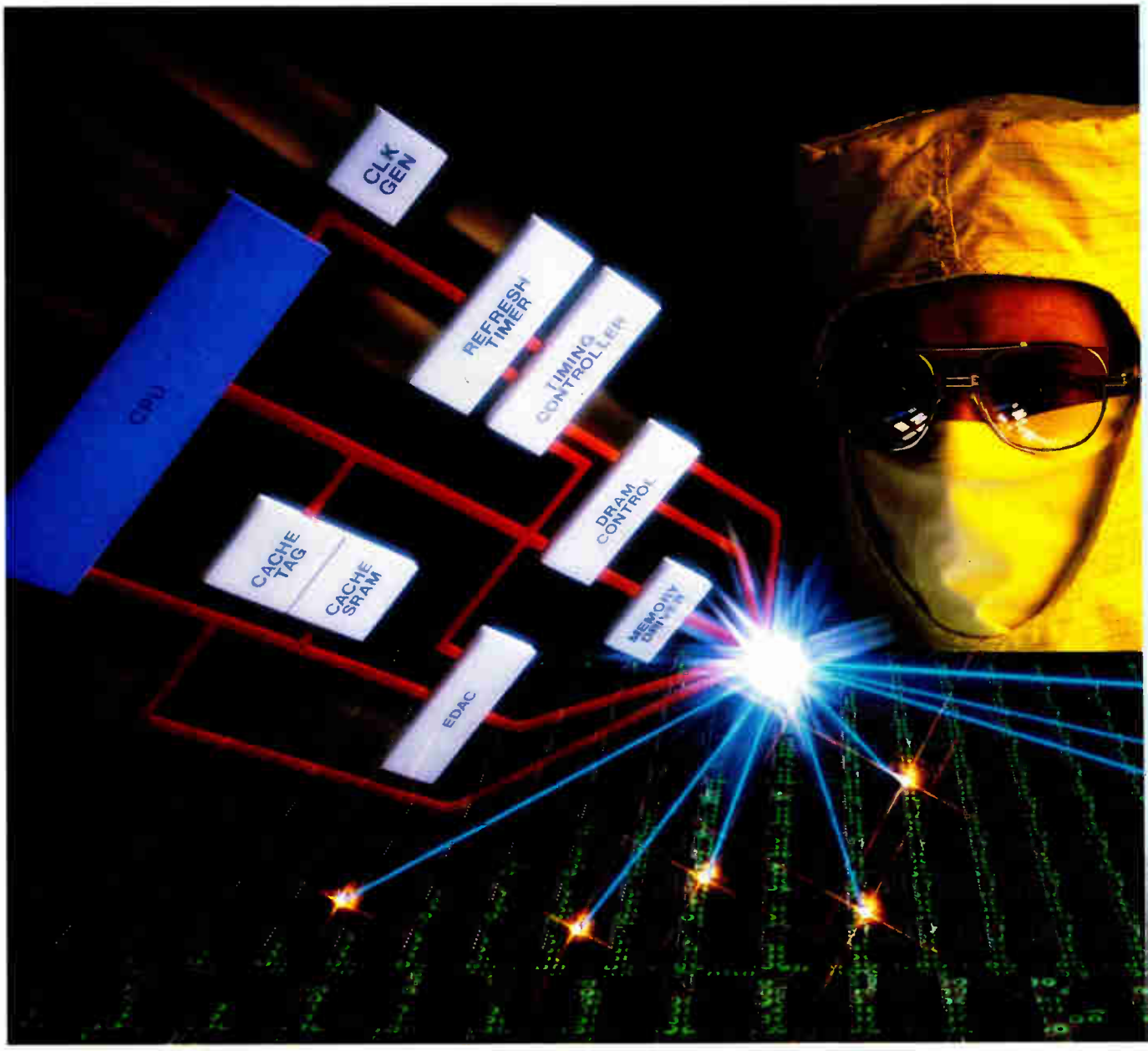
IN THE ERA OF

MegaChip TECHNOLOGIES



Memory management in the Era of MegaChip Technologies:

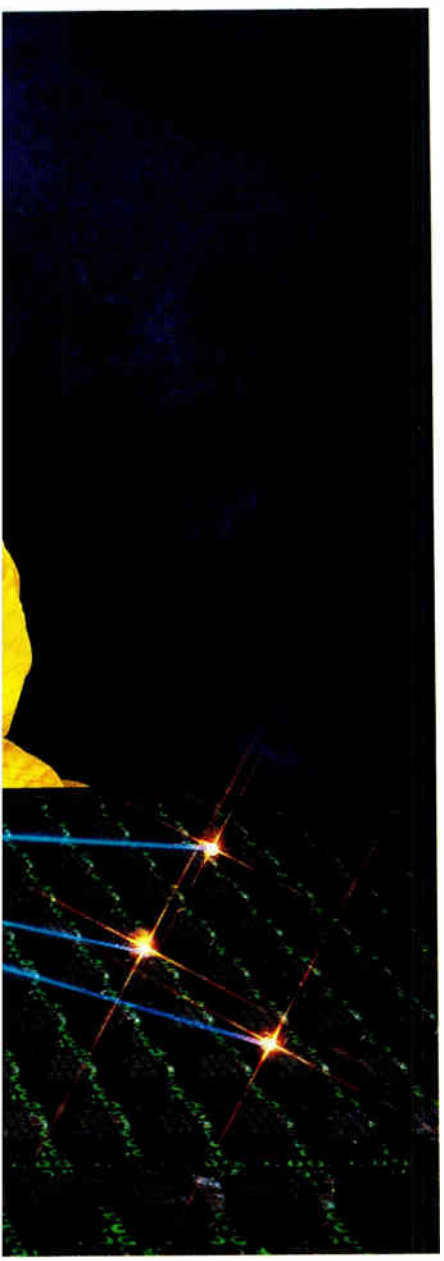
Memory-management ICs from you bring memory arrays up to



Memory systems are a prime area for significant improvements in overall system throughput. Read how TI's memory-management ICs can get you in and out of memory faster no matter which processor you choose.

You can now solve a problem whose solution has eluded design engineers for years: How to catch memory speeds up to CPU speeds. The solution lies with TI's advanced memory-management circuits, and you can use them with whichever processor best suits your application.

Texas Instruments can help processor speeds.



A universal architecture enables these TI devices to work with — and enhance — virtually any high-speed microprocessor or bus structure, even custom engines.

In addition, your component count is cut because these are single-chip VLSI circuits. Your design time and effort are shorter and easier because of TI's comprehensive Memory Management Design Kit *(see page 4)*.

TI addresses your major memory-design concerns

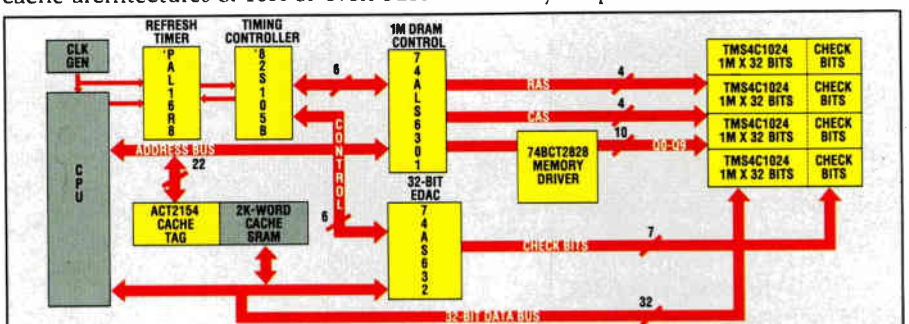
To immediately improve memory-access time, use both main and cache memories, as shown in the block diagram. This approach can produce up to a 3X increase in system performance.

Frequently accessed data and instructions are stored in a few high-speed static random-access memories and "tagged" by a TI industry-standard cache controller (SN74ACT2151/4). These 2K×8 CMOS controllers are the fastest available and can support deep cache architectures of 16K or even 32K.

TI's MegaChip Technologies

Our emphasis on volume manufacturing of high-density circuits is the catalyst for ongoing advances in how we design, process, and manufacture semiconductors and in how we serve our customers. These are our MegaChip™ Technologies. They are the means by which we can help you and your company get to market faster with better, more competitive products.

tions on chip to improve flexibility and speed and to allow for custom timing routines. This controller supports nibble- and page-mode access and scrubbing-mode refresh to increase memory output.



High-speed memories can be designed with less effort and implemented more cost-effectively by using TI's family of universal memory-management ICs. These devices, all of which are contained in TI's Memory Management Design Kit, will work with and enhance almost any high-speed processor.

This scheme is cost-effective because slower, less expensive dynamic random-access memories (DRAMs) can be used for main memory.

When you must assure system integrity, use of an error-detection-and-correction (EDAC) circuit can improve system reliability 500-fold. Since this approach is necessary with memory arrays larger than half a million bits, TI offers its leadership 32-bit EDAC.

The SN74AS632 detects dual-bit errors and detects and corrects single-bit errors while avoiding processor wait states. And at 25 ns for error detection, it meets your high-performance needs.

Interfacing between processor and main memory gets tougher as speeds increase. But TI has the SN74ALS6301 DRAM timing controller. It can handle any DRAM up to 1 Mbit and incorporates only the essential functions on chip to improve flexibility and speed and to allow for custom timing routines. This controller supports nibble- and page-mode access and scrubbing-mode refresh to increase memory output.

Soon to come: An ASIC (application-specific integrated circuit) solution.

Reducing over/undershoot is accomplished by TI's 2000 Series buffers and drivers — 25-ohm series-damping resistors on the output prevent false reads at DRAM input. For example, the SN74BCT2828 driver can reduce undershoot by 40% compared to traditional approaches. TI's 2000 Series has a high-drive current suitable for VME and MULTIBUS® II bus structures.

You can use any or all of TI's memory-management ICs to obtain the superior performance that marks a market winner. And there's no design rule that says your memory-management chips and your CPU have to come from the same supplier.

▶ *Turn page for more information.*

The tools you need to design a high-performance memory-management system are between these covers:

At $149, the value of TI's Design Kit far outweighs its cost. In one compact file, we've included just about everything you'll need to bring your memory array up to speed. Everything, that is, except your imagination in creating your own unique product differentiators. Here's what you get:

- All necessary high-performance ICs, including
  - —SN74ACT2154 2K×8 Cache Address Comparator
  - —SN74AS632 32-bit EDAC
  - —SN74ALS6301 16K to 1 Mbit DRAM Controller
  - —SN74BCT2828 10-bit Buffer/Driver with series-damping resistor
  - —TIBPAL16R8-10 and TIB82S105B High-speed Programmable-logic Devices for user-defined timing control
  - —TMS4464 256K DRAM
- *Memory Management Applications Handbook* containing applications reports and briefs that supply valuable insights into memory-management system design.
- Data sheets on TI circuits designed for efficient memory management.
- Memory-management-product software graphic-symbol libraries and supporting documentation for use with Futurenet™ or Mentor Graphics™ CAE systems.

For more information on TI's Memory Management Design Kit, call 1-800-232-3200, ext. 3203, or contact your nearest TI field sales office or authorized distributor.

Texas Instruments Incorporated SDV063EC800C
P.O. Box 809066
Dallas, Texas 75380-9066

YES, please send me more details on TI's universal memory-management ICs.

NAME _____

TITLE _____

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® MULTIBUS is a registered trademark of Intel Corporation.

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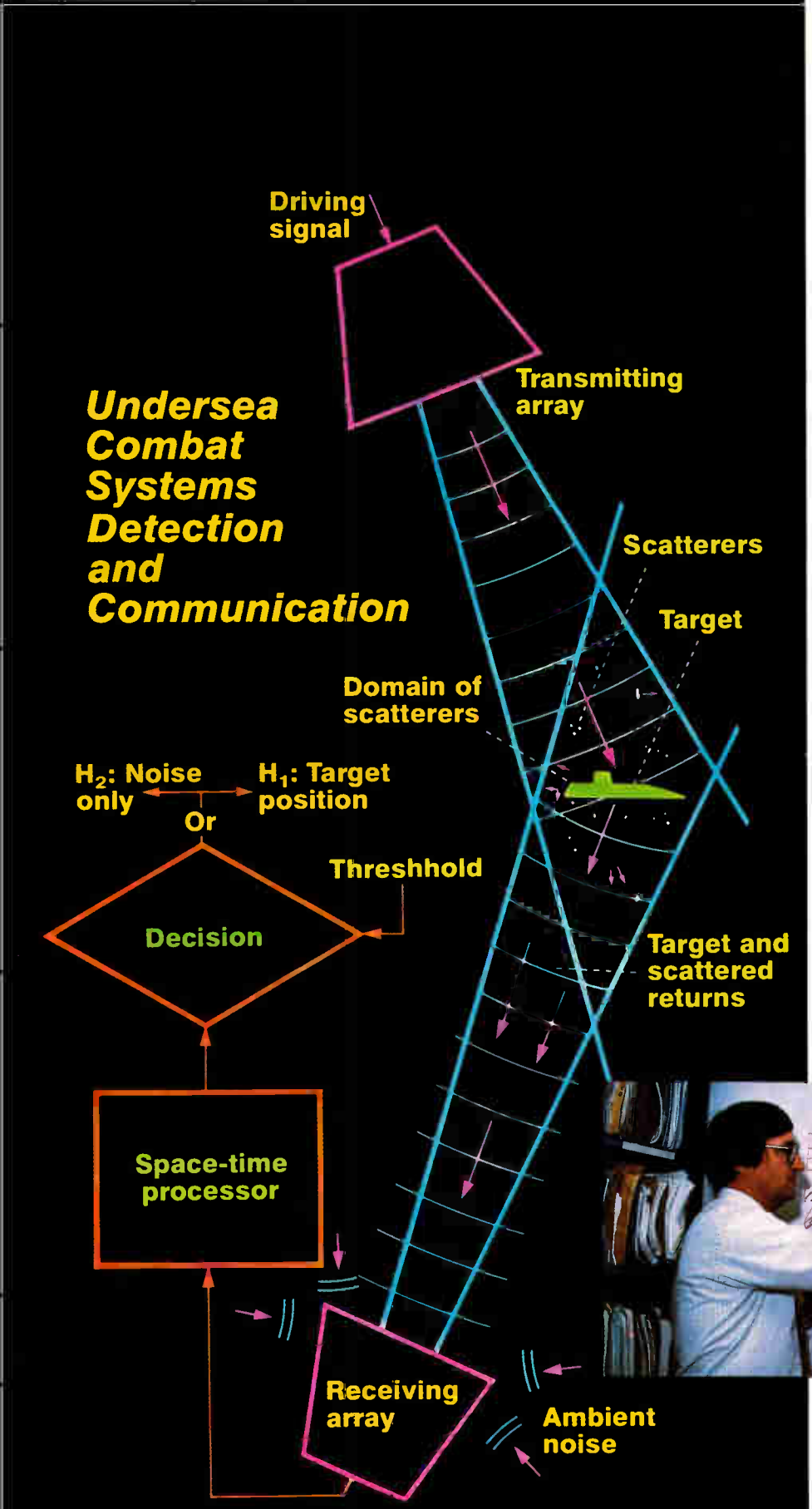
TEXAS INSTRUMENTS



CAN YOUR THEORIES SOLVE THE UNSOLVABLE?

Engineers and scientists at the Naval Underwater Systems Center are the foremost experts in underwater technologies. Their exploitation of the underwater environment as a transmission medium is a major factor in the U.S. Navy's technological superiority. But critical problems still are unsolved. In acoustic arrays. In signal processing. In underwater communications and decision-making systems. In hydrodynamics. Finding solutions is critical to national security. To world peace.

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Your rewards will exceed even the great personal satisfaction of solving the unsolvable. Intelligence and initiative are recognized quickly at the Center. You'll become one of the acknowledged experts in one or more fields of international importance. You'll work with other world-class scientists . . . in the U.S. and overseas. You'll interact at the highest levels of our government.

To apply or for more information, write to:

Naval Underwater Systems Center,
Code 083 E
Newport, Rhode Island
02841-5047
Or call 401-841-3585

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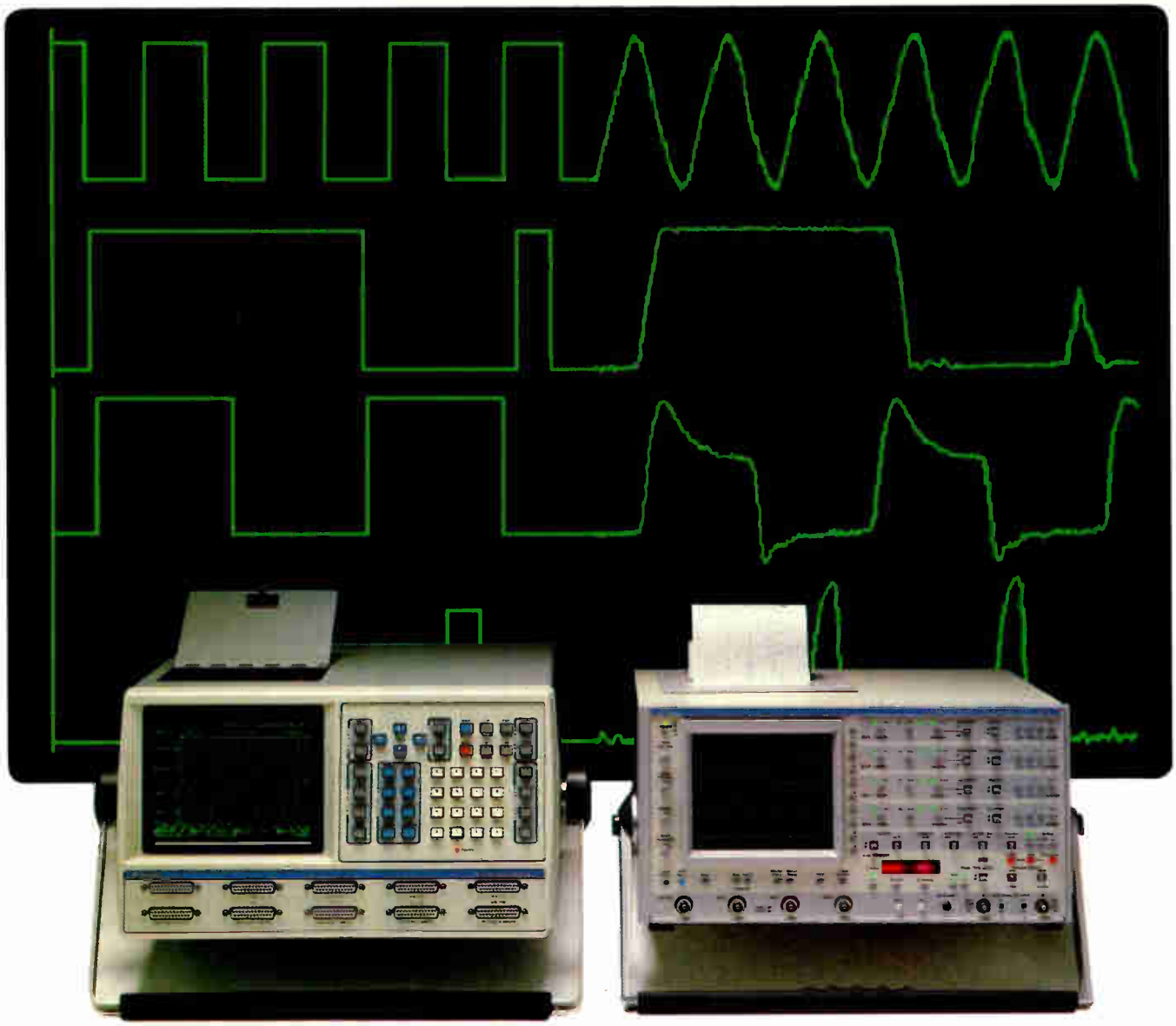

The best of both worlds.

The K450B Logic Analyzer and the 4074 Digital Storage Oscilloscope from Gould...

State-of-the-art test instruments for designers of today's superfast digital and data communications systems.

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The K450B Logic Analyzer, with up to 80 channels at 100 MHz or 40 channels at 200 MHz and glitch capture across all channels, provides top performance. AND the 4074 DSO—the only 4 channel instrument with 400 MSample/Sec 8 bit converters on every channel—is the most sophisticated oscilloscope available for the high speed pulse measurements required by electronics designers and test engineers. TOGETHER—they work as an integrated system without any of the compromises of hybrid systems; APART—two high performance instruments available for separate test applications.

ease of use...
We provide that on both the K450B and the 4074 with our AUTO SETUP facility.

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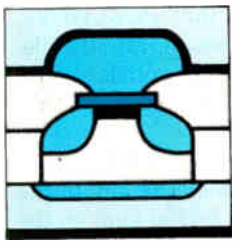
INSIDE TECHNOLOGY

PROGRAMMABLE LOGIC DEVICES: THE SECOND GENERATION



A slew of new products that break records for density, gate utilization, architectural flexibility, and speed is on the way; but PLD makers are finding that investments in software are now needed to ease their transition into a multibillion dollar market

by Bernard C. Cole

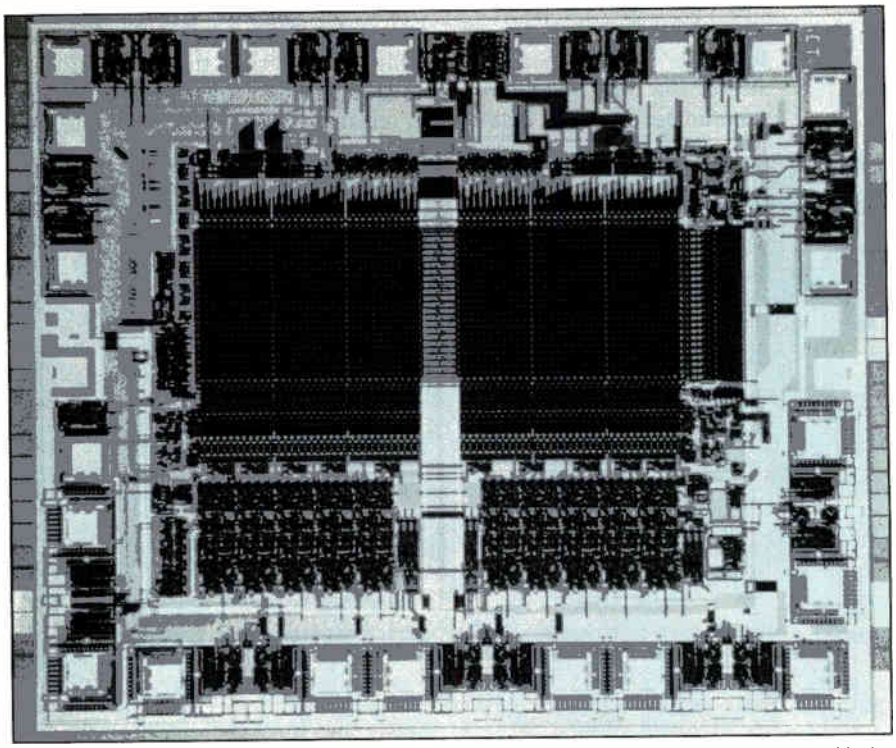
Makers of electrically erasable and programmable logic devices are set to unleash a second generation of products that break records for density, gate utilization, architectural flexibility, and speed. At stake is the multibillion dollar market for small-, medium-, and large-scale standard logic circuits that have been steadily replaced by complementary MOS gate arrays ranging in density from 1,000 to 10,000 gates.

Accounting for about 80% of gate-array sales, these densities are being targeted by PLD makers using a variety of architectural and process innovations. But there is a price to pay. By moving out from under the umbrella of the familiar programmable array logic architecture (programmable AND, fixed OR), which still dominates at densities below 1,000 gates, PLD makers must now shell out substantial investments in software to ease the transition to higher densities and new architectures.

Using CMOS-based programmable gate structures, the industry has evolved at least five architectural approaches to achieving higher density. One approach is the logic cell array (LCA), a static random-access-memory-based technology pioneered by Xilinx Inc. of San Jose, Calif., and later endorsed by Advanced Micro Devices Inc., Sunnyvale, Calif. A second group is looking to extend traditional programmable array logic devices to higher functional density by modifying them to increase gate utilization to 60% to 80% from the present 30% to 50%. Falling into this category are companies such as International CMOS Technology Inc. of Hayward, Calif., and Intel Corp. of Folsom, Calif.

A third approach is the use of a folded-array multiple-level-logic structure, favored by companies such as Signetics Corp., Sunnyvale, Calif., with its NAND-based programmable macro logic, and Exel Corp. of San Jose, Calif., with its NOR-based Erasic. Yet a fourth group is taking a closer look at the predecessor of the programmable AND/Fixed OR approach, the traditional programmable logic array, which has a programmable OR as well as a programmable AND array. These companies are adding features and options to the PAL approach to increase its functionality and flexibility. This group includes Lattice Semiconductor Corp. of Beaverton, Ore., National Semiconductor Corp. of Santa Clara, Calif., and SGS/Thomson.

The most recent approach, using an architecture developed by Altera Corp. of Santa Clara, Calif., is the multiple array matrix (see p. 66). It is manufactured using an 0.8-μm CMOS process from Cypress Semi-



1. The 22CV10C PEEL chip made by International CMOS Technology Inc. incorporates 12 kinds of devices in its programmable electrically erasable logic.

conductor Corp. of San Jose, Calif.

When moving to higher densities, the approach involving LCA devices offers some advantages. LCA devices use an uncommitted structure, in which there are no prefixed logic structures such as macrocells and registers. The current pace-setter in high-density CMOS PLDs is Xilinx, which late last year introduced the first in its new family of LCA devices capable of densities up to 9,000 gates. Fabricated using an advanced 1.2-μm double-layer metal CMOS process, the first member in the family—a 2,500-gate device—went into production in December. Now nearing production is the 9,000-gate version. Over the next four to six months, the company expects to fill in the family by introducing 2,700-, 4,000-, and 6,000-gate devices.

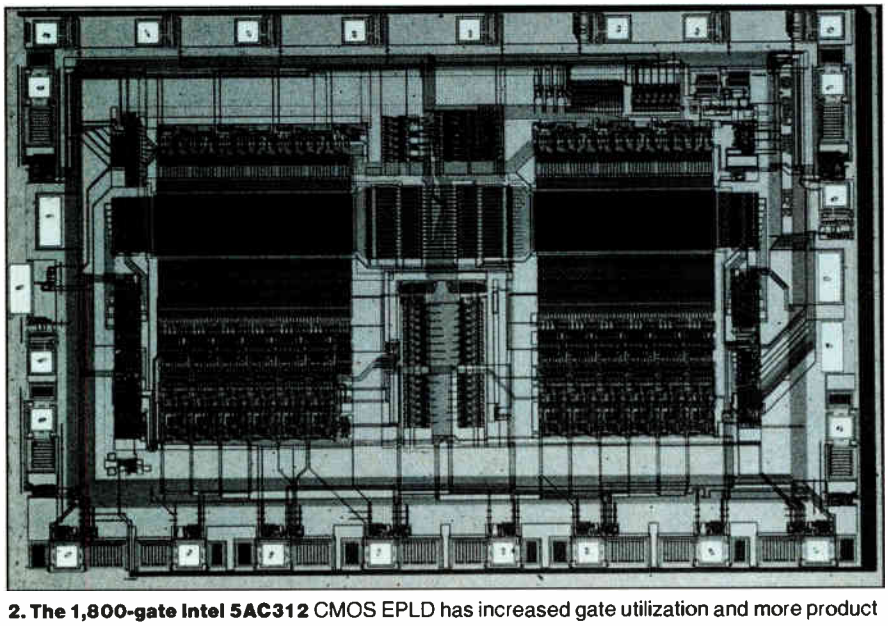
Following quickly on Xilinx's heels will be Advanced Micro Devices. The company plans to go into production in June with a 2,400-gate LCA device, followed in the late third quarter by a 9,000-gate device, according to Andy Robbins, PLD marketing director. What makes the LCA unique, Robbins says, is that unlike traditional PLDs it is based on an architecture in which the internal logic is essentially an array of uncommitted logic blocks. The logic blocks are surrounded by uncommitted programmable input/output blocks, all of which are linked by programmable interconnect lines controlled by a configuration program stored in an internal 16-bit SRAM.

Current programmable array-logic architectures are difficult to scale up in density much beyond 2,000 or so gates, says Robbins. "A problem with traditional PLDs has been gate utilization," he says. "This is due to the fact that unlike gate arrays, they are based on committed logic structures such as macrocells and registers, associated with specific pins. So when you use one function and one pin, other functions associated with that pin are unused." At low densities, this is tolerable. But when scaling to higher densities, the size of the registers and macrocells increases as does the number of gates that remain unused. By going to an uncommitted structure, such as in the LCA, most of these problems are avoided, he says.

An alternative to increasing density that companies such as Intel and ICT are considering is to modify, rather than replace, existing PLD architectures. Until recently, the main emphasis at ICT was the development of direct replacement of current 20- and 24-pin devices with its programmable electrically erasable logic (PEEL) devices, says Robin Jigour, director of marketing. Now going into production is the first in a family of what the company calls superset replacement PEEL devices, which incorporate not only the functions of current devices, but a wide range of new functions as well. Designated the PEEL18CV8, 20CG10, 18CV8Z, and 22CV10C (see fig. 1), the devices incorporate not only a specific standard programmable array logic configuration, but 11 other variations as well.

Depending on the device, between 18 and 22 inputs and 8 and 10 macrocells are available. The key to the flexibility of the device is that each logical sum on the devices is directly associated with a multifunction I/O macrocell and its I/O pin, says Jigour. Each of these macrocells contains a D type flipflop, an output multiplexer, and a feedback multiplexer as well as four EE memory cells that can be programmed to configure each macro in 12 different ways. The 12-way macrocell gives the user control of output polarity, feedback path, and output type—registered or combinatorial, dedicated input or output, or bidirectional I/O—allowing them to be used to implement functions which might require multiple conventional PLDs.

An alternative approach is being taken by Intel in its 5ACXXX family, which aims at increasing the gate utilization and efficiency by adding proprietary enhancements to the I/O macrocells. The first device in this family is the 5AC312 (see fig. 2), a 1.5-μm CMOS EPLD with a density of about 1,800 equivalent gates. The device incorporates special features to increase its flexibility in high-performance CPU systems as well as increase the number of product terms available to the user without using up valuable pin resources.



2. The 1,800-gate Intel 5AC312 CMOS EPLD has increased gate utilization and more product terms available as a result of enhancements to the I/O macrocells.

In the first case, the 5AC312 incorporates an input-latch register combination that allows each input to be configured in one of five ways: flowthrough input; synchronous or asynchronous latched input; and synchronous or asynchronous registered input.

To give the designer as much access to internal gates as possible without sacrificing pins, Intel has incorporated special-product term-sharing logic that divides the eight P-terms in each macrocell into two groups. These quads or subsums of products can then either be combined into a second OR stage, or allocated to serve as input into the second OR stage of adjacent megacells.

By using this feature, each 312 macrocell can support up to 16 P-terms, versus three to eight for standard de-

vices, without giving up any pins, says Larry Palley, PLD product marketing manager. "Even with all the P-terms in a particular macrocell allocated away, the I/O registers and all the secondary control signals are still available for use," he says. Current plans call for moving to a 1.0-μm process and extending the traditional PLD functions up to about 3,000 to 4,000 gates. "After that, it is clear that it is necessary to consider other alternatives," he says.

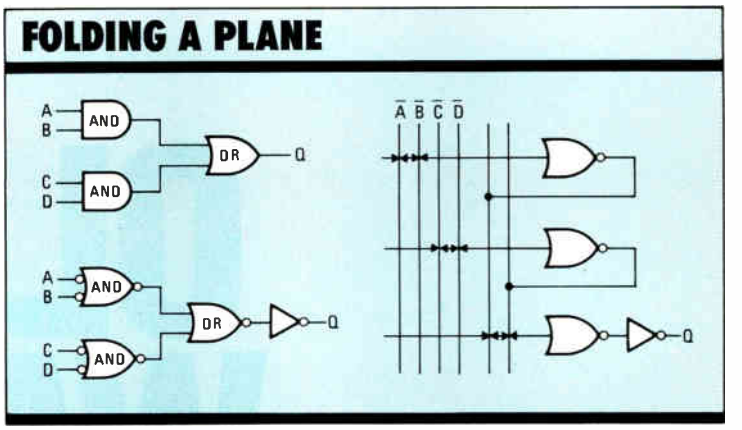
Looking for ways to increase the number of gates and product terms without sacrificing pins, many manufacturers are turning away from the simpler—but more limited—programmable array logic structure to the more flexible programmable logic array pioneered by Signetics, which incorporates both programmable AND as well as programmable OR elements. In an attempt to take advantage of the PLA structure but give it some of the features of PALs that users have found helpful, Lattice Semiconductor and its PLD partners—National Semiconductor and SGS/Thomson—have developed the GAL39V18.

First out is Lattice, which uses its 1.1-μm double-level metal CMOS EEPROM technology to build a device which combines the programmable AND/programmable OR structure of a PLA with the additional functionality of such PAL style features as macrocells and buried registers. Further scaling of the process and new architectural features should allow the company to push the architecture from its current 600- to 800-gate equivalent to above 1,000 gates, says William Wiley Smith, Lattice's PLD product marketing manager.

In addition to limited densities, a drawback to traditional PAL and PLA structures is that they are essentially single level logic, says Eric Goetting, PLD program manager at Exel Semiconductor Inc. of San Jose, Calif. "That is, they are good at implementing one level, or type, of logic function," he says. "This is okay where you want to reduce the chip count devoted to interface glue logic. But if you want to implement an LSI or VLSI system function which incorporates a variety of logic types, it is necessary to use multiple PLDs."

To address this problem, Exel developed the Erasic architecture, a NOR-based architecture in which a plane of NOR gates is folded back onto itself and thus can generate any number of levels of logic by simply passing signals back through the array the desired number of times, using asynchronous feedback terms to act as both array outputs and inputs, but to generate the multiple-logic-level signals (see fig. 3). Currently in production with an 800-gate device, the XL78C800, the company is developing higher-density versions. The first, a 1,600-gate device, is expected to be available early next year.

An alternative folded-array approach, undertaken by Signetics Corp., is the programmable macro logic architecture. It combines a NAND-based network to allow the direct interconnection of any number of logic nodes within the single matrix, with macrocells formed and interconnected to the I/O structure. The company's first PML offering is the bipolar PLHS501 a 400- to 800-gate equivalent device aimed primarily at combinatorial logic applications. A second device, the PLHS502, is now being sampled; it is aimed at synchronous/asynchronous state machines, as well as event-driven controller applications. CMOS versions of the architecture are now in development, which will extend densities up to at least 10,000 gates, says Joel Rosenberg, PLD marketing manager at Signetics.



3. Exel's Erasic PLDs use a NOR-based architecture in which a plane of NOR gates is folded back onto itself.

A common problem facing the PLD makers—no matter which of the five approaches they are pursuing—is that by venturing into new architectures and higher densities, they must invest a lot of money in software development. "Developing a new architecture appropriate to higher densities involves almost as much investment in software as in hardware," says David Laws, director of marketing at Altera. "With integration levels doubling each year, traditional PLD design tools are no longer effective." Using Boolean equations, a 5,000-gate MAX PLD would require an average of 50 pages, not including text, and would take weeks to enter, as well as months to debug, he says. To address this problem, the company has developed the MAX PLUS software package (see p. 90), which incorporates a logic synthesizer as well as a hierarchical-schematic-capture mechanism that combines schematics with traditional Boolean-equation and state-machine-entry mechanisms.

Similarly, to address its new high-density XL3000 arrays, Xilinx has upgraded its existing development system. Xilinx added logic synthesis software and a TTL library, in addition to its already available design entry, simulation, design implementation, and in-circuit design software.

Vendors of folded arrays, such as Exel and Signetics, say there is another alternative. According to Exel's Goetting, unlike other high-integration PLD strategies, using folded arrays based on NAND or NOR logic allows the use of design methodologies that are upwardly compatible with existing software used for AND/OR-based PLDs. "But there is no free lunch," he says. "The transition from one architecture to another, and to higher densities, is not without problems. What good software-development tools can do is ease the transition." To that end, the company has developed a set of software called Multimap and Multisim design and simulation software. They are designed to interface transparently with the widely available ABEL PLD design software package from Data I/O Corp. of Beaverton, Ore. □

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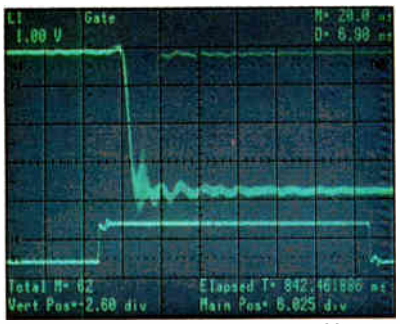
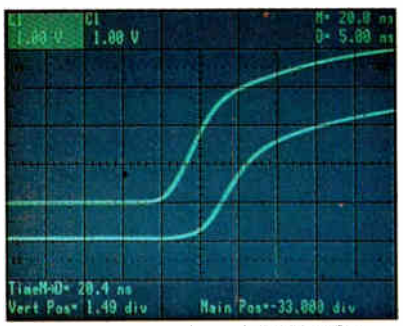


Microchannel CRT makes metastable events visible. Counter shows total number of events during elapsed time.



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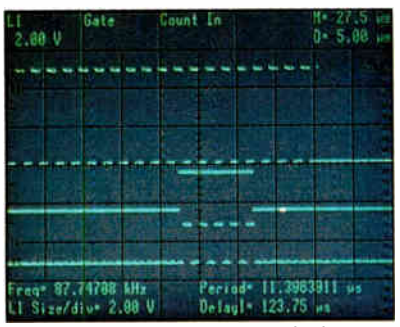
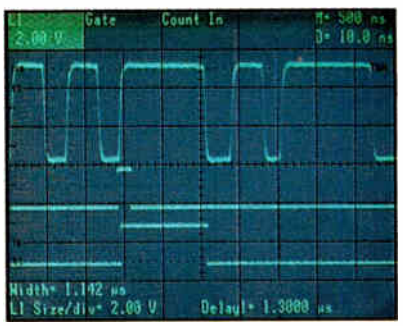


Gated frequency: top trace is pulse burst input; center is counter gate; bottom is view of what's being counted.



Make gated pulse width measurements with counter accuracy. Center is counterview trace, bottom clearly shows pulse width measured.

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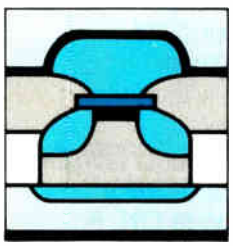
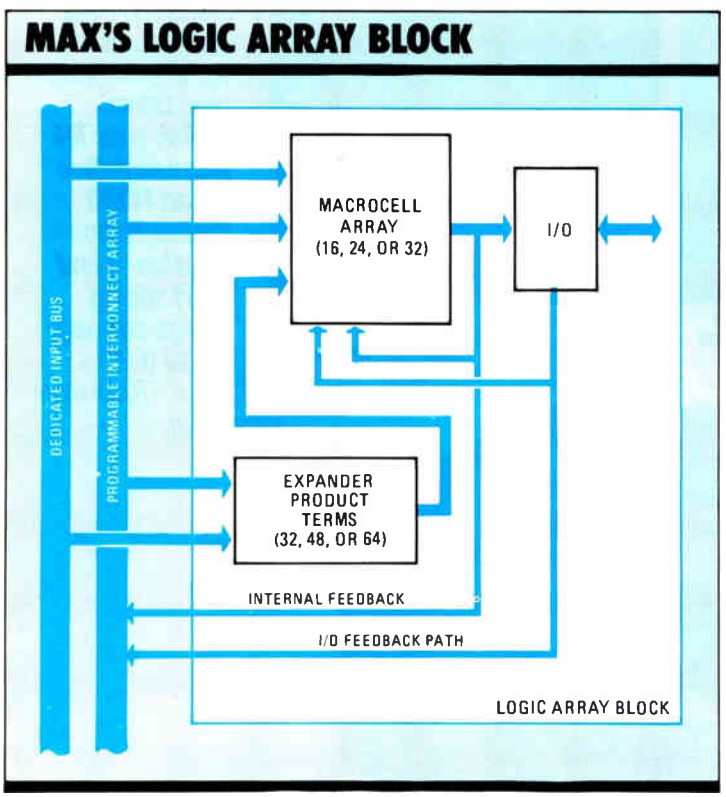
ALTERA PUSHES EPLDs TO 5,000 GATES AND 60 MHz

Its new MAX architecture quadruples density and doubles clock rates compared with its CMOS EPLDs



A radical new architecture for ultra-violet-erasable programmable logic devices from Altera Corp. doubles the clock rate and quadruples the density of AND/OR EPLD arrays over the largest CMOS EPLDs, which also come from Altera. Called the multiple-array matrix, or MAX, the Santa Clara, Calif., company's new architecture makes possible arrays with up to 5,000 gates and internal clock rates as high as 60 MHz.

Fabricated using a 0.8-μm CMOS EPROM process developed by Cypress Semiconductor Corp. of San Jose, Calif., the MAX structure is being incorporated into a family of six modular building blocks. The blocks will range in density from 600 up to about 5,000 gates and from 16 macrocells in a 20-pin package up to 128 macrocells in a 68-pin package. This improvement in density comes with no substantial performance penalty, says David Laws, Altera's vice president of marketing—the devices operate internally at 60 MHz, so they can be designed into systems with clock rates above 40 MHz.



1. The MAX Logic Array Block contains a macrocell array of 16 to 32 macrocells, logic expanders, and input/output functions.

Until now, a major limitation facing manufacturers who have tried to increase the densities of EPLDs has been the fan-in increase of each macrocell logic array, says Donald Faria, applications manager at Altera. As standard single-array PLDs are increased in size, he says, the number of inputs to the logic array increases directly with the number of devices and macrocells. This increase in fan-in, he says, consumes silicon area, and reduces overall speed due to the added parasitic loading.

To overcome these limitations, Altera has developed the MAX architecture, which consists of multiple logic-array blocks, or LABs, linked by a dedicated programmable interconnect array. Other key features of the family include: a unique macrocell structure that combines the benefits of programmable logic arrays (programmable AND and OR arrays) and programmable array logic structures with fixed AND, programmable OR arrays, special logic expander circuits to increase the functionality of a device without using up valuable pin resources, decoupled I/O pins and register resources to increase design flexibility, and enhanced register options that allow operation as either a flow-through latch or edge-triggered register.

The result, says applications engineer Robert Beachler, is an internal device structure optimized to accommodate exact functional equivalents of 7400-type medium-scale-integration and small-scale-integration standard-logic-part types. Faria says register-intensive functions such as counters, shift registers, and state machines can be accommodated with the same efficiency as gate-intensive logic, such as address decoders, adders, and comparators. According to Laws, "Engineers will be able to standardize on just a few MAX device types in place of hundreds of different part numbers currently employed in most digital systems. That will allow the integration of as many as 50 typical 7400-type elements into a single MAX part."

The first device in the family is the EPM5032. Scheduled for sampling by midsummer, it is a 32-macrocell device containing 240 product terms and the equivalent of 1,200 gates in a 28-pin dual in-line or J-leaded chip carrier. Intended for register-intensive functions, it features eight dedicated input signals and 16 dual feedback I/O pins, plus a total of 32 user-definable D, JK, SR, or T flipflops.

The other members of the family will be introduced over the next six months, Laws says. They include the 16-macrocell EPM5016, with 600 equivalent gates and 110 product terms; the 24-macrocell EPM5024, with 800 gates and 240 product terms; the 64-macrocell EPM5064, with 2,400 gates and 640 product terms; and the top-of-the-line EP5128, a 128-macrocell device, with 5,000 gates and up to 1,280 product terms. Incorporating a total programmable EPROM bit count that ranges from about 50,000 to more than 220,000, the devices have die sizes ranging from slightly less than 20,000 to slightly over 85,000 square mils.

At the heart of the MAX architecture is the logic-array block, which consists of three elements: the macrocell, the logic expander, and the I/O block (see

fig. 1). The various members of the MAX family incorporate from one to eight LABs. Macrocells per LAB can range from 16 to 32.

Each macrocell (see fig. 2) contains eight product terms and a programmable flipflop as well as multiple control inputs, so that each macrocell can be controlled independently of any of the others. Each flipflop can be configured for either D, T, JK, or SR operation or bypassed entirely for purely combinatorial functions. Also, says Faria, each flipflop supports both asynchronous preset and clear functions, allowing asynchronous loading of counters or shift registers found in many TTL functions. Clocking options include both synchronous (dedicated input) or asynchronous (logic), independently configured for each flipflop.

Each macrocell flipflop can be programmed to operate as either a flow-through or an edge-triggered register. Flow-through latching provides minimum input to output delays for speed-critical applications such as chip select decoding, while edge triggering guarantees glitch-free outputs for applications requiring synchronous counters or state machines.

Adding to the flexibility of the MAX architecture is a proprietary I/O block organization in which the I/O pins and the internal flipflops have been decoupled so that all registers can be buried. Faria says this allows an extremely versatile I/O structure in which the I/O pins can be used for dedicated outputs, bidirectional outputs, or additional dedicated inputs. That means, he says, that applications requiring many buried flipflops, in the form of counters, shift registers, storage registers, or state machines, need no longer consume both the macrocell and the associated I/O pin. "What this means," he says, "is that large amounts of logic can be incorporated while still retaining the use of all of the I/O pins." An additional benefit, he says, of decoupling the I/O pin from the internal macrocell is that it provides a dual feedback capability for each macrocell, useful in applications requiring large amounts of input pins, while still reserving the macrocell feedback for buried logic.

If the logic-array blocks incorporated just the enhanced macrocell and I/O blocks, the MAX family would rate as one of the most flexible and versatile programmable array logic structures around. However, says Laws, for Altera designers this was not enough. "What we really wanted was a structure that combined the best of both worlds—the superior I/O delays of the programmable-AND, fixed-OR structure and more efficient use of product terms," he says.

The main problem with most devices based on programmable array logic has been in the inefficient use of resources because of the fixed allocation of product terms. While an average logic function might only require two or three product terms, Faria says, most programmable-AND, fixed-OR structures come with eight or more product terms to handle anything from simple to more complex functions.

To give each logic-array block the additional flexibility of a programmable logic array when needed, Altera designers have incorporated a new structure called a logic-expander product-term array. These expanders, says Faria, can be viewed as single product terms with inverting outputs feeding back into each logic array block. Thus, if the logic function to be implemented is gate-intensive (as in address decoding, adders, and comparator functions, requiring many product terms) or register-intensive (as in counters, shift registers, and state machines) expander blocks can be distributed to any macrocell requiring more than three product terms.

To address two problems common to most PLD structures, undesired skews among logic signals due to the varying length of interconnections between gates as well as the often long delay paths, the new family of MAX devices incorporates a special programmable interconnect array (PIA) that links each LAB to another. Unlike the routing channels found in mask or programmable gate arrays, the PIA block provides a single, uniform delay from point to point. "The PIA acts like a programmable communications highway between logic functions," says Faria, "so that all input and macrocell feedback signals can be connected to any other macrocell within the device." By providing a fixed delay, he says, the PIA eliminates skews among logic signals that may cause glitches in internal or external logic. *-Bernard C. Cole*

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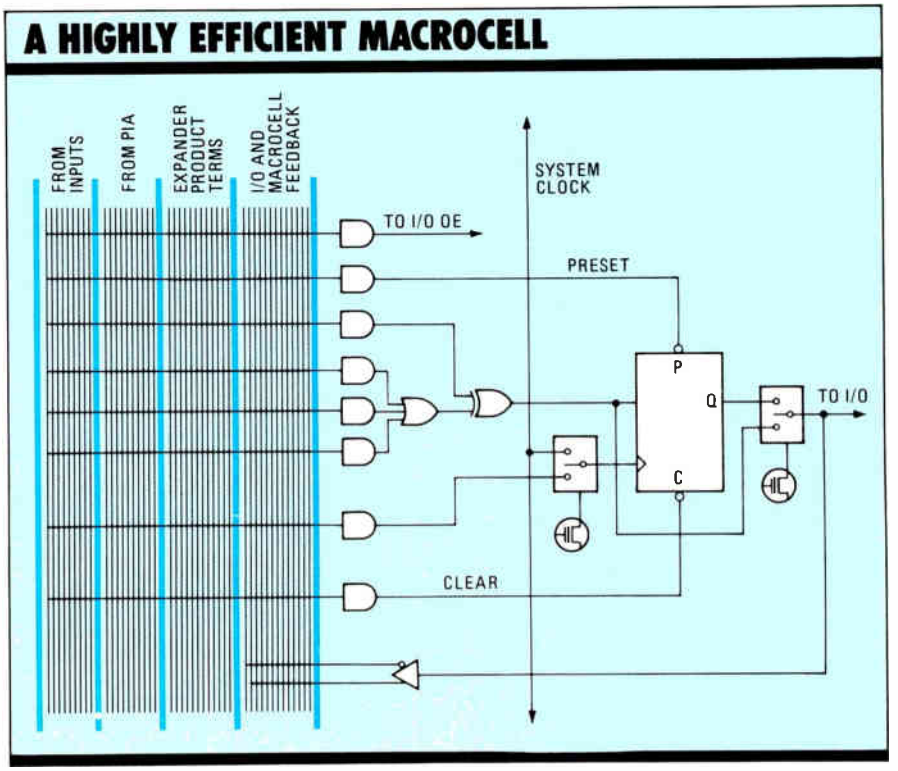

2. MAX macrocells' eight logic product terms will satisfy 80% of typical needs. When required, more terms are assigned from a separate expander product term function.

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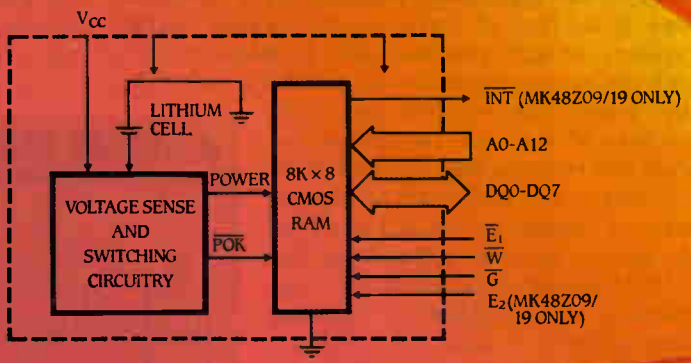
MK48Z12	0-70 C	4.5V	11 yrs.	Yes	120-250ns	2K × 8 SRAM unltd. write cycles
MKI48Z02	-40-85 C	4.75V	6 yrs.	Yes	120-250ns	2K × 8 SRAM indust. temp. range
MK148Z12	-40-85 C	4.5V	6 yrs.	Yes	120-250ns	2K × 8 SRAM indust. temp. range
MK48T02	0-70 C	4.75V	11 yrs.*	Yes	120-250ns	2K × 8 SRAM w/realtime clock
MK48T12	0-70 C	4.5V	11 yrs.*	Yes	120-250ns	2K × 8 SRAM w/realtime clock
MK48Z08/09	0-70 C	4.75V	11 yrs.	Yes	150-250ns	8K × 8 SRAM w/additional CE and power fault flag (– 09)
MK48Z18/19	0-70 C	4.5V	11 yrs.	Yes	150-250ns	8K × 8 SRAM w/additional CE and power fault flag (– 19)

*3.3 yrs. minimum clock operating in battery backed mode.



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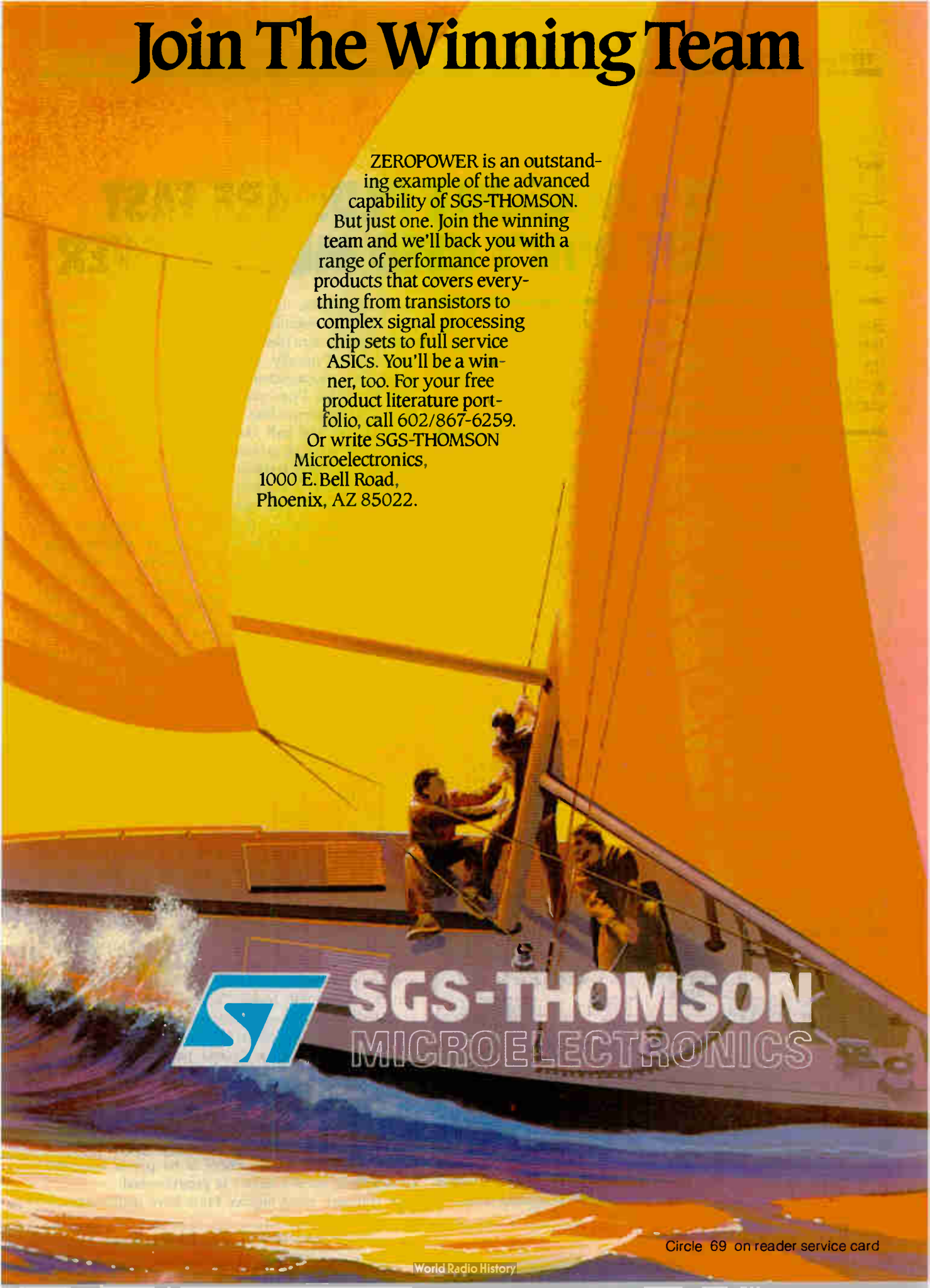

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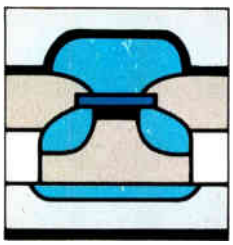


TI's ERASABLE PLDs ARE FAST BUT DON'T NEED MUCH POWER

Based on a new high-voltage CMOS process, TI's family of erasable programmable logic devices vie for sockets with bipolar parts by giving the designer a new point on the PLD speed-power trade-off curve—25-ns speed and zero standby power

Bipolar technology-based programmable array logic devices are fast but power-hungry. Now a series of new parts from Texas Instruments Inc., made with a high-voltage CMOS process and aimed at replacing bipolar programmable logic devices will not only perform at the relatively high speed of 25 ns, but will also operate at virtually zero standby power.

Some of the newer CMOS-based erasable PLD devices on the market consume less power but rely on substrate pumps and other techniques to boost their speeds into the bipolar class. These EPLD parts, however, pay a penalty for this speed in standby power consumption.

Many system designs exist where the utmost in speed is not critical and where a greatly reduced (virtually zero) standby power consumption can be a real system plus. In short, there are many present and future bipolar PLD sockets that system designers can replace with EPLD devices operating at a new speed-power point.

System designers and planners will soon have these cost-effective EPLD parts. Based on TI's high-voltage enhanced performance implanted CMOS (HVEPIC) process, the EPLDs use a 14-mask process and special circuit design techniques to achieve both 25-ns speeds and virtually zero (fewer than 500 mW) standby power (see fig. 1). Typically, today's 2- to 3-μm bipolar PLDs with 15-ns propagation delay times dissipate 0.75 to 0.90 W. And a 1-μm modified CMOS-based EPLD with back-gate substrate bias yields devices with about the same speed and half the power dissipation. In contrast, TI's product strategy for EPLDs calls for the use of true CMOS technology to achieve virtually zero standby power at a small speed penalty (25- to 35-ns parts) compared with bipolar PLDs.

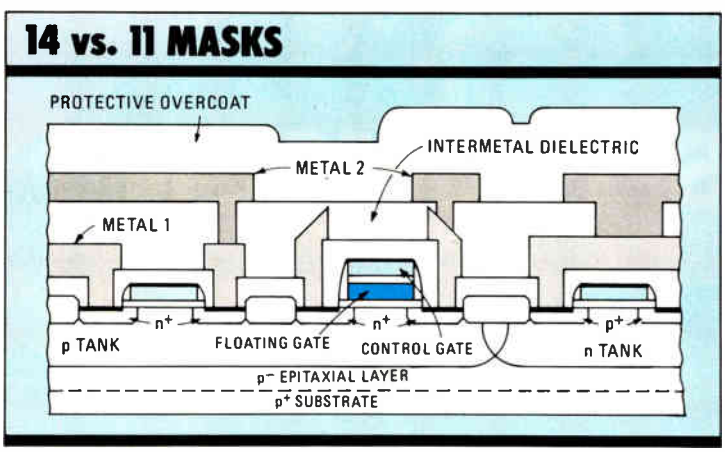
Key to the success of the new EPLD design is the use of FAMOS cells that require 12.5-∞ programming voltages. To have a fast programmable cell suited to CMOS EPLSs, an EPLD must be able to handle this high voltage and this is the reason for development of the HVEPIC CMOS process. Normal CMOS processes such as TI's EPIC cannot handle 12.5 V.

Among the system-level benefits to the designer or planner specifying HVEPIC-based EPLDs is reprogrammability. Bipolar PLDs are not reprogrammable; if the designer blows a fuse, the PLD configuration is permanently committed. CMOS EPLDs suffer no such permanent configuration and the system designer using them can allow for errors, program changes, and, perhaps most importantly, the ability to fully test the part during the manufacturing process to ensure 100% programming yield. In contrast, to test a bipolar part, the PLD designer must employ additional circuitry to test around the array. Even with the additional circuits, the designer cannot test all the fuse array elements.

In a bipolar part, all of the logic circuitry dissipates power all the time. A CMOS logic circuit dissipates power only when it switches. Thus, the EPLD designer can add many programmable features and circuits—and complexity—to an EPLD to make the system designer's life a bit easier. Moreover, since power is essential for speedy operation, the fact that an EPLD's programmable architecture features do not cause a power drain from the "speed paths" of the EPLD array further enhances the EPLD's ability to be a high-speed device.

EPLD designers can, for example, add programmable macro cells onto the EPLD outputs. These outputs are configurable as combinatorial- or register-types as a programmable option. There is no power overhead to run them once a device is programmed.

In contrast, most bipolar PLDs have dedicated out-



1. TI's HVEPIC process requires 14 masks—compared with 11 for its standard 1.0-μm EPIC CMOS process—to hit 25-ns speeds with no standby power.

puts that cannot be programmed. When macro programmability is provided, it consumes standby power that diverts power from the PLD speed paths.

There are CMOS EPLDs on the market which are faster than those TI will offer but they do not offer zero standby power. These devices gain their high speed by using special circuit features; for example, the sense amplifiers so critical to read and write operations are kept on all the time in these devices. In contrast, in the TI design, edge-detection wake-up circuits quickly turn the sense amps on when they are needed. Most of the time the sense amps are off and draw no standby current. There is some speed penalty paid in the time it takes to wake up the sense amps and propagate signals through EPLDs built with wake-up and sleep circuits. However, the power saved is substantial.

Another technique used by conventional CMOS-based EPLDs that contributes to their speed is back-gate bias of the EPLD substrate. This bias current is on all the time and causes standby power dissipation not seen in the TI design.

HVEPIC was developed at 1.0-μm geometry. Moreover, the process was developed to be compatible with plastic packaging so one-time-programmable parts could be had at low cost. To prove out the EPLD designs with minimal fuss, the first parts, currently under development and test, have been built at 1.2-μm geometry. Regardless of feature size, HVEPIC is a 14-mask, n-twin-well, double-level metal, double-level polysilicon CMOS process technology. HVEPIC requires the use of titanium silicide-clad moats and gates as well as double-level metal interconnects and double-level polysilicon to achieve the desired EPLD speed-power point.

An EPLD FAMOS programmable element has its gates tied to input lines and drains tied to product lines. In their erased state, FAMOS cells function like normal n-channel MOS transistors. When the cell gate is addressed (logical one) the device is on and the cell drain is a logical zero. Similarly, if the cell gate is not addressed (logical zero), the transistor is not conducting and the cell drain is a logical one. Whenever a FAMOS cell is programmed, the cell threshold level is shifted to a high enough level so the transistor will never turn on. The drain of a programmed FAMOS cell is always a logical one.

The two-transistor FAMOS cell (see fig. 2) is optimized for both EPLD reads and writes. The WRITE transistor, which programs the FAMOS cell, receives a patterned threshold voltage implant to increase its hot electron injection while it is programmed. This injection improves the cell's programming behavior.

The READ transistor drives the sense amplifier during the read operation and is blocked from the threshold adjust implant. Because of this blocking, the READ transistor has a higher drive current, which leads to improved circuit speed.

It's not just the design of the READ transistor that designers who want high-speed CMOS EPLDs must worry about. There are, for example, RC time delays associated with the polysilicon interconnects that must be minimized. This is accomplished by the use of the self-aligned titanium silicide incorporated in the HVEPIC process.

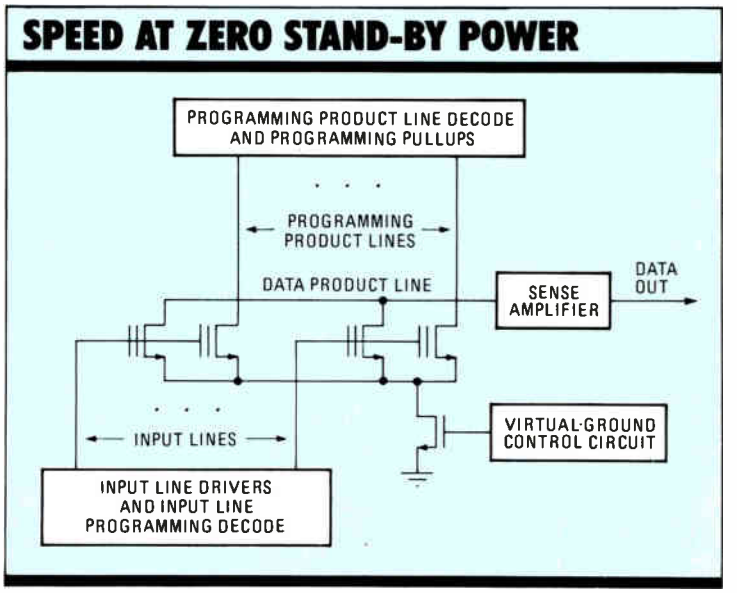
Both the periphery logic gate polysilicon and the FAMOS stack gate polysilicon are silicide-clad. This design not only reduces RC delays, but it also gives the EPLD designer greater layout flexibility since using polysilicon for relatively long interconnects does not introduce large RC delays.

The silicide yields sheet resistances an order of magnitude lower than that available from traditional n-moat and double poly procedures and almost two orders of magnitude reduction compared to p-moat. The RC time constant is reduced accordingly. This cladding is another bonus since the silicide-clad moats require fewer contacts and can be made smaller to reduce parasitic junction capacitance.

The double-level metallization contributes greatly to improved circuit speed. The normal function of the double-level metal interconnects is to allow the EPLD designer to lay out a given design with a smaller die area compared to single-level metal parts. Among its other achievements, double-level metal also contributes to lower interconnect resistance, lower resistance input lines, and easier power bus routing.

But, in the TI EPLD design, the double-level metal also allows partitioning of the FAMOS array to reduce its bitline capacitance by up to one- half. This reduction shortens the time required for a sense amplifier to read a product term. Furthermore, array wordlines are strapped with double-level metal between each partitioned array. This reduces wordline resistance. Finally, all critical speed paths are metal-strapped to minimize RC delays.

The EPLD parts were the work of TI product design team members Bob Gruebel, Frank Sweeney, Scott Herrington, Dave Wilmoth, and Shailesh Kedekia. The HVEPIC team members are: Howard Tigelaar, Keith McDonald, Toan Tran, Jim Paterson, Kueing-Long Chen, and Johnson Lin.



2. Key elements of TI's EPLDs are the two transistor FAMOS cells, ground control circuits for source bias, drivers, decoders, and sense amplifiers.

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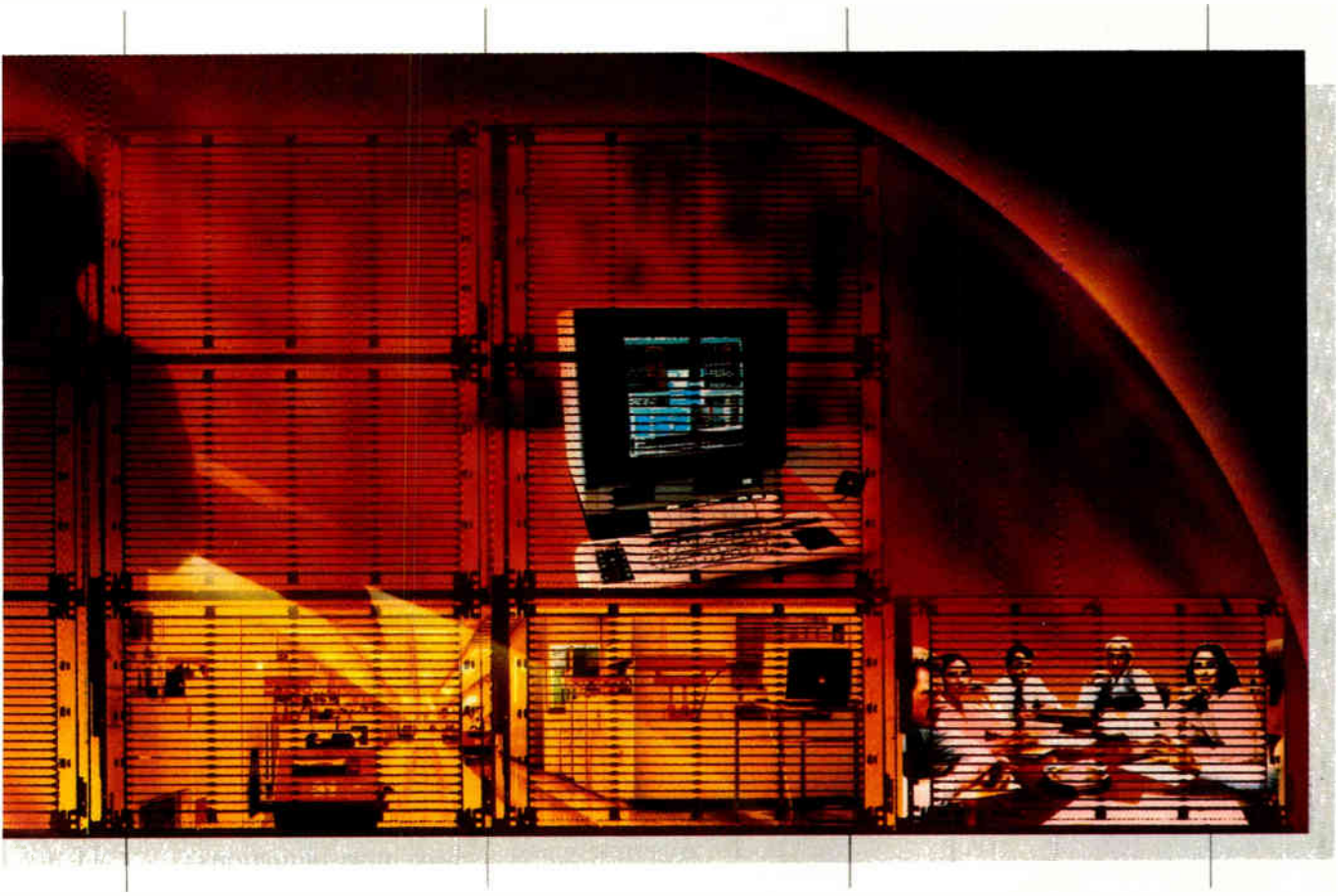

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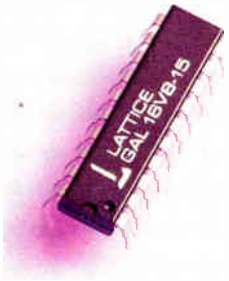

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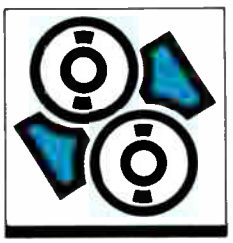


The barriers to acceptance are being overcome: new software makes system integration simpler, standards will establish uniform formats, and upcoming erasable units should deliver performance

by Jonah McLeod

Optical data storage may finally be on the verge of breaking through to a large-scale market, fulfilling the promise that's been made for five years. High hopes—and a lot of hype—accompanied the introduction in 1983 of the first systems, but several drawbacks relegated them to a few, relatively small niches. Blessed by extraordinarily high capacity, they were cursed by lack of software, which was aggravated by an absence of standards governing formats that made it hard to build the first write-once disks into systems. Later, the mediocre performance of some early erasable systems, compared with Winchester drives, kept original-equipment manufacturers from choosing them as an alternative to conventional magnetic storage systems.

But now those obstacles are being overcome. Software is beginning to appear that should spur the growth of write-once, or nonerasable, systems. A wave of erasable 5¼-in. magneto-optic disk-drive systems is about to hit the market, with a variety of companies announcing products that come close to Winchester drives on performance and beat them on capacity. Also appearing are 3½-in. erasable disk drives and a new class of erasable compact disks. Format standards should be set by the American National Standards Institute for 5¼-in. nonerasable disk drives this year, and eventually expanded to include erasable disks as well.

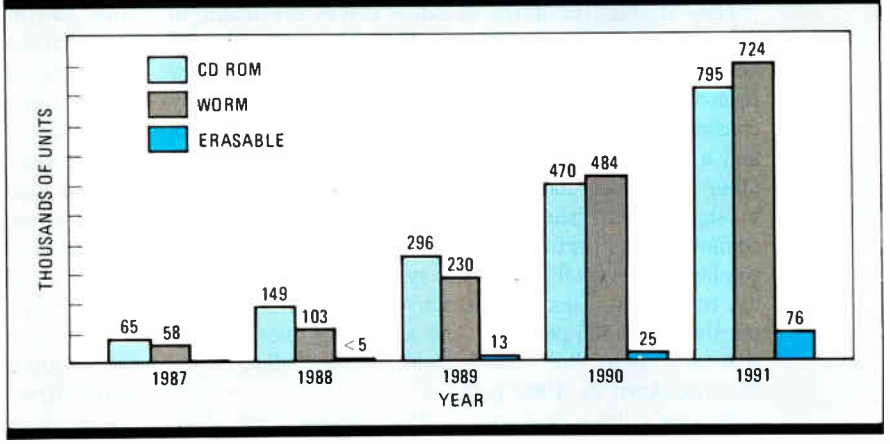
Even so, the market is not going to explode, with optical systems smashing the grip of magnetic disk and tape on storage applications all at once. Largely because the new software coming onstream will make it easier to build write-once disk drives into systems, growth will show up first in the nonerasable segment of the market (see chart), according to Gene Selven, president of Electronic Trend Publications Inc., a market research firm in Saratoga, Calif. Selven expects 149,000 write-once and 103,000 compact-disk read-only-memory shipments this year. Unit shipments in both categories should double each year thereafter through 1991.

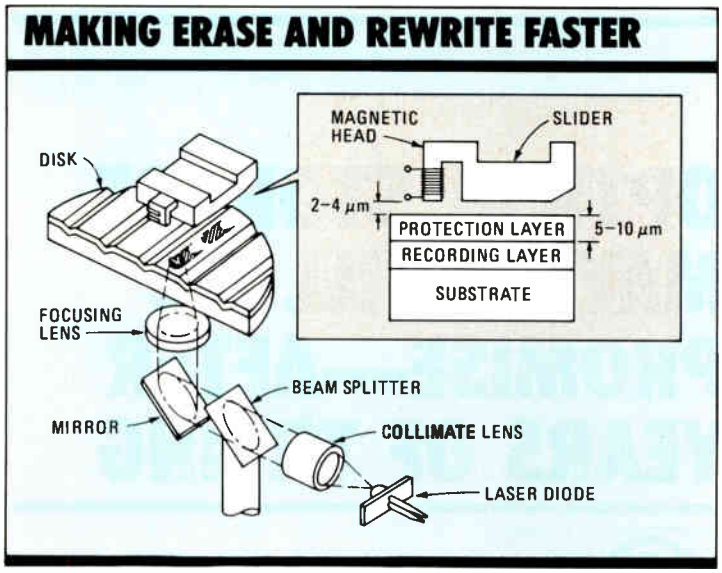
By comparison, the number of 5¼-in. erasable drives shipped should grow from a few thousand drives this year to about 76,000 units in 1991, with most of the growth taking place in 1990 and 1991. That makes sense to George Scalise, president of Maxtor Corp. The San Jose, Calif., company is one of those introducing a new high-performance magneto-optic system based on an erasable 5¼-in. disk (see p. 85). "System integrators will be quick to build optical drives into add-on and add-in subsystems," Scalise says. "But large OEMs will take up to two years to evaluate the drives before building them into final systems." Once they are evaluated, though, the erasable systems inevitably will pose a threat to the nonerasable drives—all things considered, a disk that can be erased and rewritten has far more potential applications than one which can't be erased.

Meanwhile, nonerasable systems don't have to be evaluated; they've been around a while, waiting for software. Now, third-party vendors such as Optical Storage Solutions Inc. in Concord, Calif., and Optisys, a division of Micro Mart Inc. in Phoenix, Ariz., are shipping that software.

At the same time, ANSI standards on formats for 5¼-in. write-once drives, which would in effect make disks from different vendors' system interchangeable, are within sight. Proposed standards were scheduled

NONERASABLE DISKS LEAD THE PACK





1. Hitachi heats one disk surface and applies a magnetic head to the other to save revolutions in magneto-optic erasing and rewriting.

to go in April from ANSI's X3B11 committee to its Accredited Standards Committee X3 for public review, according to Joseph Zajaczkowski, vice president of marketing at Cherokee Data Systems in Boulder, Colo., and chairman of the X3B11 committee. The review will take four to six months, after which the proposal will go to ANSI for formal release. The proposed standards have also been sent to the International Organization for Standards for consideration as an ISO standard.

With software in place and standards in the wings, the components for a total system are finally available. One of the first such systems comes from IBM Corp., which resells as its model 3363 a write-once, 5¼-in. disk drive it buys from Matsushita Electric Industrial Co. "The software contains a file system optimized for write-once storage," says Al Rizzi, low-end optical products manager at IBM. "But it appears like an erasable magnetic-disk storage system to a computer system."

Unlike write-once disks, erasable systems will get plenty of evaluation—OEMs are going to give them a long, hard look after their experience of the past few years. Too many companies promised too much, then failed to deliver (see p. 80).

Now it looks as if the erasable drives are about to deliver. Maxtor's new drive, the Tahiti I, apparently will be the first to reach the kind of performance necessary to compete with Winchester drives, which is generally considered to be an average access time of about 65 ms and a data-transfer rate of about 5 Mbits/s. A host of other companies, mostly Japanese, are shipping or plan to ship at least sample quantities of drives providing somewhat less performance than the Maxtor drive. Also coming are low-end 3½-in.-disk systems with high-capacity, removable disks and attractive prices—under $1,000 per drive and $25 per disk. And appearing unexpectedly is a new competitor—the erasable compact disk [*Electronics*, April 21, 1988, p. 21].

Maxtor's drive features average access time of 43 ms and a data transfer rate of 13 Mbits/s. Skip Kilsdonk, vice president of marketing at Maxtor, believes this performance—coupled with storage capacity of up to 1 gigabyte—will make the drive attractive immediately as primary storage in work stations, network file servers, and many other magnetic disk-drive applications. Samples are ready for shipment now.

Appearing about the same time will be the Sony model SMO-D501, word of which first came out around a year ago. Sony shipped 25 units or so early, although its official timetable has samples appearing in May, according to Robert Wilson, director of the optical storage technology group at Sony Corp. of America in Park Ridge, N. J. Production should begin by fall, depending on customer response. Following Sony, Olympus Optical of Tokyo will ship samples of a 5¼-in. drive this summer. By the end of this year or the beginning of next year, Sony and Olympus will be joined by Hitachi, Laser Magnetic Storage, Matsushita, Optotech, and Toshiba. Sharp Corp., in Osaka, is already shipping an erasable optical drive, but it's built into Sharp's JY-500 personal-computer add-on subsystem.

All of these drives rate about the same in performance. The Sony drive is typical, with an average access time of 100 ms and a data-transfer rate of 7.4 Mbits/s. At that level of performance, they will compete mainly for secondary storage applications which might have gone to write-once disks.

However, one of the problems limiting the performance of magneto-optic-disk performance—the fact that it takes a full revolution to erase an old block of data before new data can be recorded—is in the process of being solved. For example, the Central Research Laboratory of Hitachi Ltd. in Tokyo announced a method in late 1987 (see fig. 1). In this solution, to write a "0" or "1" in the bit cell coming under the head, a laser heats the disk surface while a separate magnetic read/write head on the other side of the disk switches between -300 and +300 oersteds. One drawback to the approach is that the disk can only be recorded on one side. Another is that the disk suffers more oxidation, which shortens its useful life. The first drawback is unavoidable, but there are ways of extending the life of the storage medium.

While manufacturers strive to boost performance of 5¼-in. erasable optical drives, they are also working to produce a 3½-in. unit that deliberately sacrifices some performance in favor of a low price. Thanks to their greater capacity, the smaller drives could eventually replace tape in back-up applications and floppy disks in program-load and on-line data storage in low cost personal computers.

But, like most of the 5¼-in. drives on their way, the smaller systems will compete first with nonerasable systems, says Al McDowell, manager of optical storage products at Fujitsu America Inc. in San Jose, Calif. "Smaller 3½-in. units could replace low-performance, write-once drives in disk back-up and other secondary storage applications." Scott McCready, a senior analyst at the Marshfield, Mass., market research firm of CAP International Inc., agrees. He says low-performance storage applications will be served

by aggressively priced 3½-in. erasable optical drives. Again, Maxtor will be in the lead, introducing in June a 3½-in. drive called Fuji (see p. 87).

Both Sony and Matsushita are also developing a 3½-in. unit, but neither appears near to announcing a product this year. One other major 3½-in. player is Verbatim Corp., the Sunnyvale, Calif., subsidiary of Eastman Kodak Co. The Verbatim drive is supposed to store 50 Mbytes on a one-sided disk and have a 70-ms average access time while writing as well as a 50-ms access time while reading.

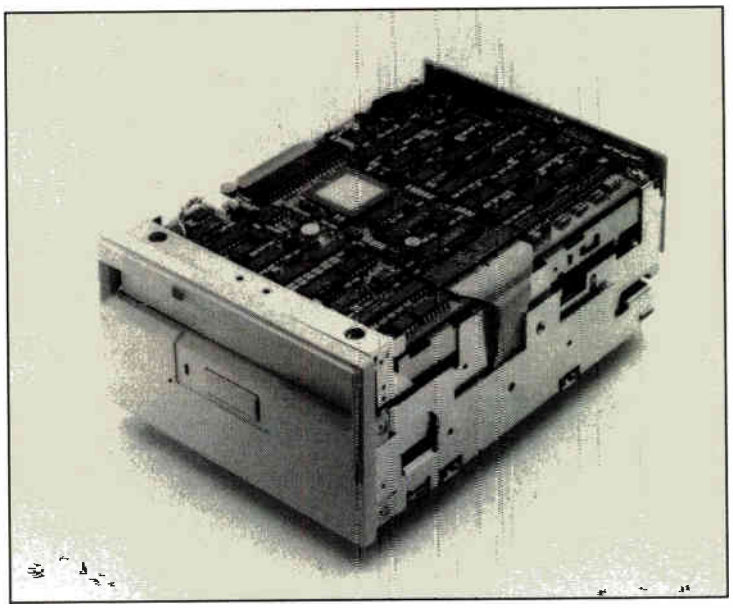
But the small drives may face some competition for low-end applications from an unexpected source, although they should have some lead time. Thomson's Consumer Laboratories in Villingen, West Germany [*Electronics*, March 17, 1988, p. 42] and Tandy Corp. in Fort Worth, Texas, both claim they have already developed an erasable compact disk. Each expects to sell the product first as a consumer item and later adapt it for data storage. The adaptation will take about three years, says Robert McClure, president of Tandy Electronics Manufacturing. Work on similar erasable CDs is reportedly also underway at Nippon Kogaku KK in Japan and IBM and Carnegie Mellon University in the U. S.

The bulk of these upcoming erasable systems pose less of a threat to magnetic storage, at least at first, than they do to their optical cousins, the nonerasable systems. The major problem that originally kept OEMs from using nonerasable systems—the lack of software—is being solved just at a time when erasable systems are coming onto the market, says Victor Jipson, director of the optical storage laboratory at the IBM Almaden Research Center in San Jose, Calif. He thinks that many OEMs with applications that could use write-once units are forestalling purchases and waiting for erasable drives.

However, Jipson also believes that the write-once capability offers advantages to certain applications. He says that write-once systems can serve in financially oriented record-keeping, for example, such as banking, where an audit trail of all transactions is required. Whether this niche will be large enough to make write-once a major market for drive manufacturers is open to question.

The drive manufacturers themselves think it is. Contrary to the speculation that IBM is losing its enthusiasm for the model 3363 disk drive, Al Rizzi says that the company is continuing to push the product, although the company is disappointed in its sales. At Maxtor, George Scalise says his company is continuing to fund research and development in write-once optical systems, and most major write-once manufacturers are doing the same.

One reason for this optimism is the fact that the ANSI standards are arriving. The market for the current generation of write-once disks is fragmented because every vendor's drive writes to its disk differently—a disk written on one drive cannot be read by any other drive. The proposed standards will allow any 5¼-in. write-once disk to be read by any 5¼-in. disk drive. However, the ANSI standards carry their own threat to nonerasable drives. ANSI plans to expand the standards eventually, so that also includes erasable units. After that happens, the erasable disk drives will be able to read the write-once disks, too.



Fujitsu's write-once disk, the M2505B, is being reworked to meet proposed ANSI standards for 5¼-in. write-once disks.

At any rate, drive manufacturers are working now to redesign their products so they can accommodate the 5¼-in. write-once standard. The new WM-D070 5¼-in. drive from Toshiba America's Disk Products Division in Irvine, Calif., will be one of the first to be completely compatible with the standard, says Ronald Haglund, director of marketing for optical products the company. Evaluation units are scheduled for shipment at the end of summer. The drive—typical of what can be expected from other write-once drive makers—will come with two modes. In one mode, the drive conforms to the standard and provides 596 Mbytes of storage using a 512-byte sector, or 652 Mbytes using a 1,024-byte sector. A second mode will not conform to standards, but will make up for the lack of standardization by using a proprietary recording scheme to achieve a much higher capacity—900 Mbytes—for the user willing to sacrifice standards for storage.

Fujitsu, Hitachi, and Mitsubishi all have write-once drives. All were designed to meet a preliminary versions of the standards, so none are completely compatible—Al McDowell at Fujitsu America, for example, says some changes are required to the on-board Small Computer Systems Interface controller in his company's drive, the M2505B (see photo). At the moment, though, all three companies are planning to have a product ready to ship by the end of this summer.

The latter part of 1987 should see most drive manufacturers roll out products that conform to the standard. But there are exceptions. One will be Information Storage Inc. of Colorado Springs, Colo., which has shunned standards altogether and is offering a 1.2-gigabyte, 5¼-in. drive, the ISi525GB. The company is one of the few that has a relatively large installed base of drives—about 5,000 units—and it doesn't see any reason to tamper with a winner. □

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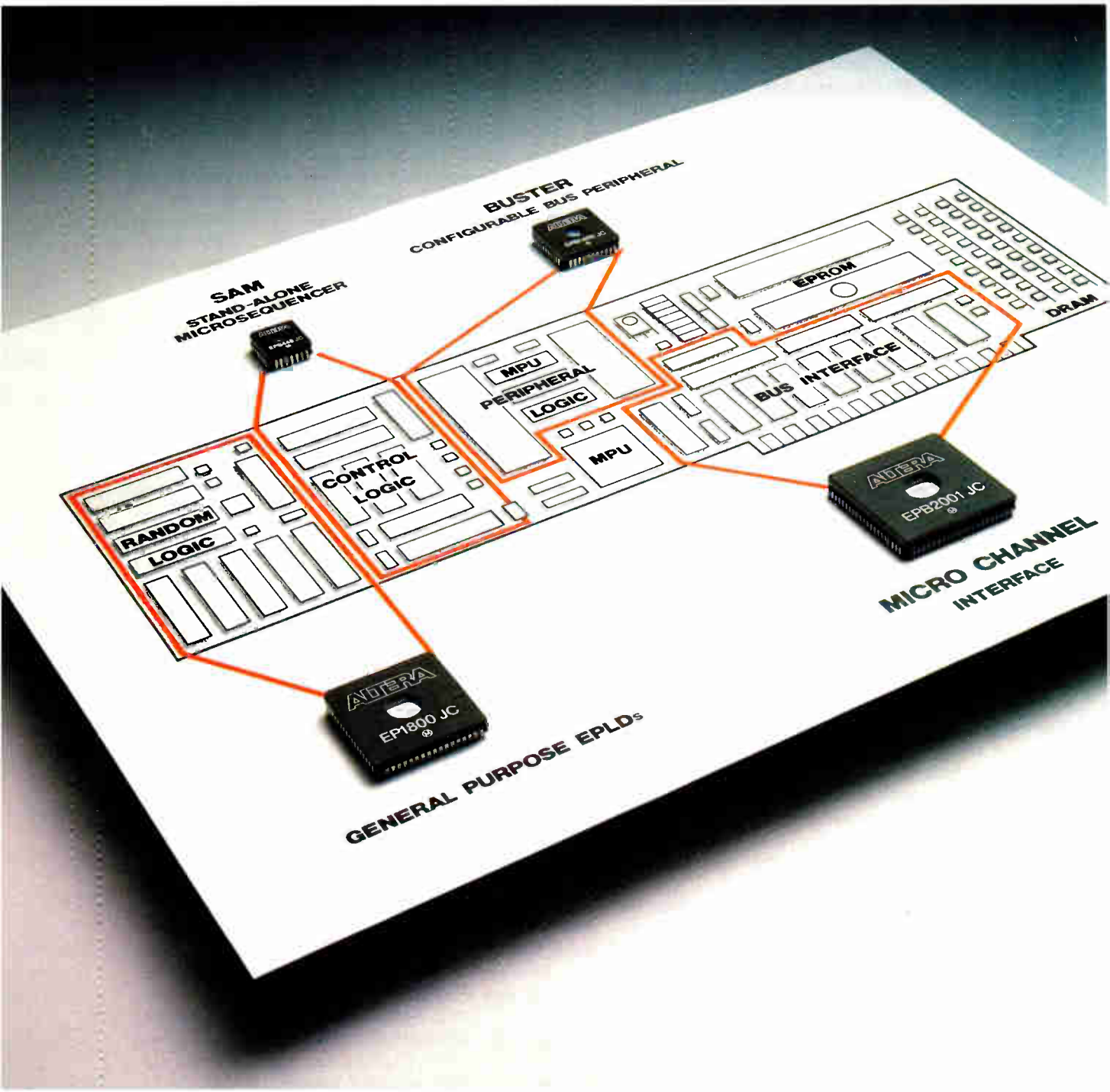

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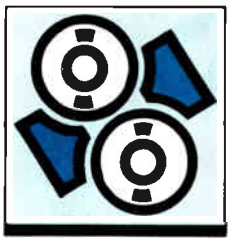
OPTICAL STORAGE—WHAT A LONG, STRANGE TRIP IT'S BEEN



Trouble has stalked optical disk drives since work started on them in the mid-1970s. False starts have plagued the technology and they multiplied as more companies began optic development in the early 1980s. The false starts bred disappointed customers. Once burned, the customers were twice shy, so each company to come along with an optical storage system would find fewer customers than it had counted on. Sales would lag, development costs often would race ahead of the budget, and another optical effort would quietly fade from sight.

The pattern emerged as far back as the late 1970s, when what was then Burroughs Corp., now Unisys, in Detroit, began to investigate optical storage. The technical problems and their attendant costs caused Burroughs to bail out in 1982.

Also in 1982, Storage Technology Corp. of Louisville, Colo.—perhaps oblivious to Burroughs' example—began a program to develop a high-capacity, 14-in., write-once optical disk drive. Three years later, the company had filed for protection from its creditors under Chapter 11 of the federal bankruptcy statute—not because of the optical disk program, but not in spite of it, either. In December 1985, Ryal Poppa, Storage Tech's new chief executive officer, killed the project, which had cost the company $100 million.

About a year after Storage Tech started working on its optical system, two other companies actually introduced theirs. Optimem, then a division of Shugart Corp. in Santa Clara, Calif., and Alcatel Thomson Gigadisc, a subsidiary of Thomson CSF, based in Le Plessis Robinson, France, rolled out compatible 12-in. drives in October 1983. Problems arose in less than a year. The French company was supposed to provide a bubble-forming media for each company's drive. But by mid-1984, Gigadisc couldn't produce enough media for both companies. It took the sensible, if somewhat unsporting, step of curtailing shipments to Optimem. Optimem spent six months qualifying another media supplier, 3M Company. Eventually, even Gigadisc would turn to 3M for extra media for its own needs as well.

Inability to produce sufficient media was Gigadisc's downfall—customers were reluctant to buy drives without media. In October 1986, the company followed Storage Tech into the French equivalent of Chapter 11. According to Edward Rothchild, editor and publisher of the *Optical Monthly News* newsletter, "estimates of ATG's [Gigadisc's] losses ranged from about $19.7 million since incorporation to $970,000 for [1986] alone."

The company managed to survive. In March 1987, French investors purchased its assets. They renamed it Art Tech Gigadisc, moved it to Toulouse, France, and eventually made it profitable.

A year before Gigadisc stumbled, Optimem had begun a program with 3M to develop a multifunction 5¼-in. drive—one that could operate with optical read-only memory; write-once, read-many disks; and magneto-optic disks. 3M had developed its own magneto-optic media and convinced Optimem to build a drive which could use it.

The two companies showed the result of their work at the 1985 Fall Comdex in Las Vegas, Nev. But the project was doomed. Optimem ran into problems with the first stage—a drive that could function with both read-only and erasable disks—and never made it to the write-once function before the project was killed.

Like Gigadisc, Optimem survived by virtue of an acquisition, becoming part of Cipher Data Products, Inc. of San Diego, Calif. After the acquisition, the multifunction disk drive was cancelled in a cost-cutting move, never to be heard of again.

THE BIGGER THEY COME...

But of all the false starts, the one that stands out is the announcement a few months before the Optimem-Gigadisc drive's debut. On April 6, 1983, Matsushita Electric Industrial Co. proclaimed that it was introducing the first erasable optical memory. Based on an erasable phase-change recording medium, Matsushita's drive seemed too good to be true. It was.

The system Matsushita introduced was actually an engineering prototype; the company hoped its announcement would lure at least one large-scale customer into a deal. No such customer appeared; the system never made it past the prototype stage. But Matsushita's drive did get the attention of Stanford Ovshinsky, who added insult to injury by suing Matsushita. Ovshinsky is president and chief executive officer of Energy Conversion Devices Inc. in Troy, Mich., and he holds extensive patents in phase-change recording. In November 1983, Matsushita agreed to buy a license for Ovshinsky's technology.

The optical-storage industry is still beset by problems—almost willfully so, it sometimes seems. Optimem and Gigadisc, for example, tried to set a standard by shipping compatible 12-in disk drives. Every other 12.-in.-drive maker chose to use a completely incompatible product. Later, fully aware of the trouble that a non-standard 12-in. drive had in achieving market acceptance, early manufacturers of 5¼-in. drives made a passing attempt to set a standard, then gave up.

A determined committee of the American National Standards Institute has now come up with a proposed standard. True to form, though, it incorporates two different standards. One uses a servo scheme for determining the drive is on track, the second a sampled servo mechanism. The two are mutually exclusive.

Eventually, though, one of the standards should prevail. That will pave the way for greater acceptance 5¼-in. write-once drives. Meanwhile, a new generation of erasable 5¼-in. drives promises to compete with magnetic disk drives in performance. Maybe, at long last, the optical industry is about to overcome its checkered past. *—Jonah McLeod*

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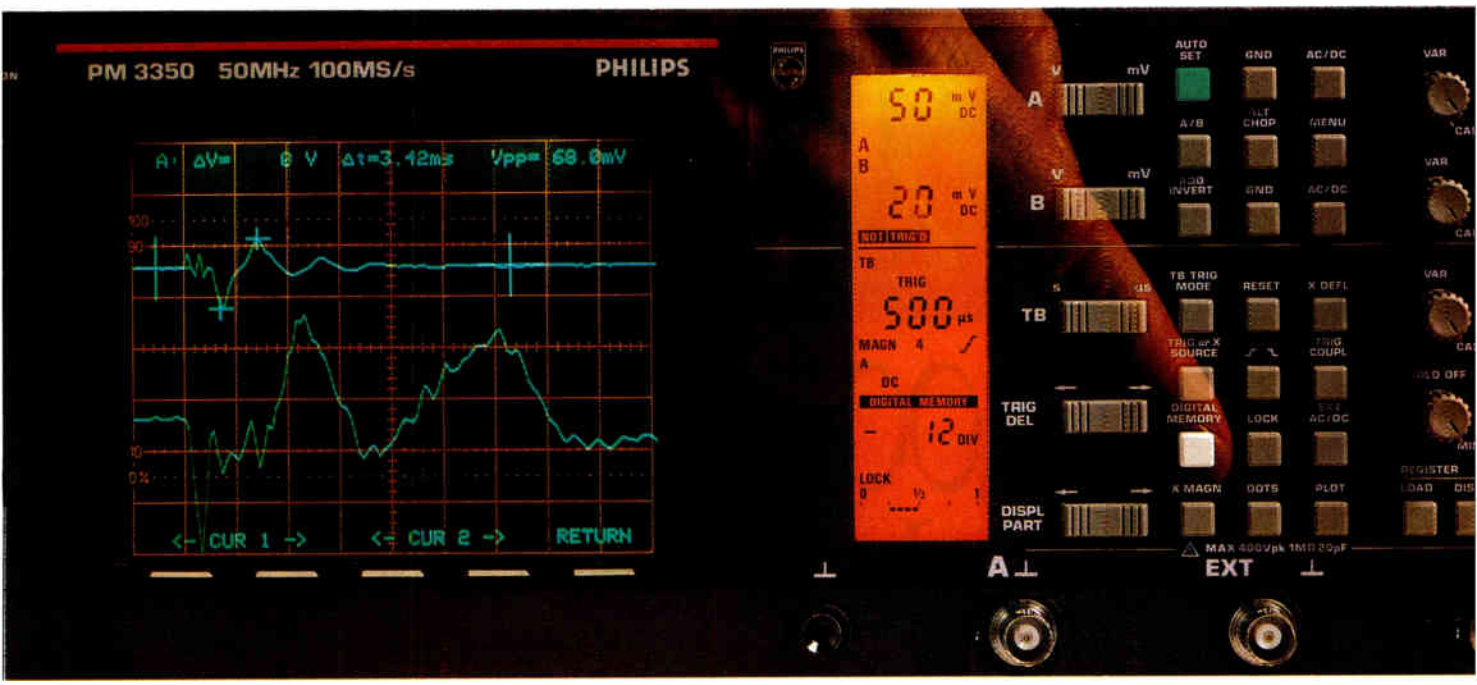

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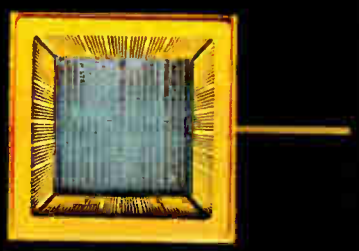

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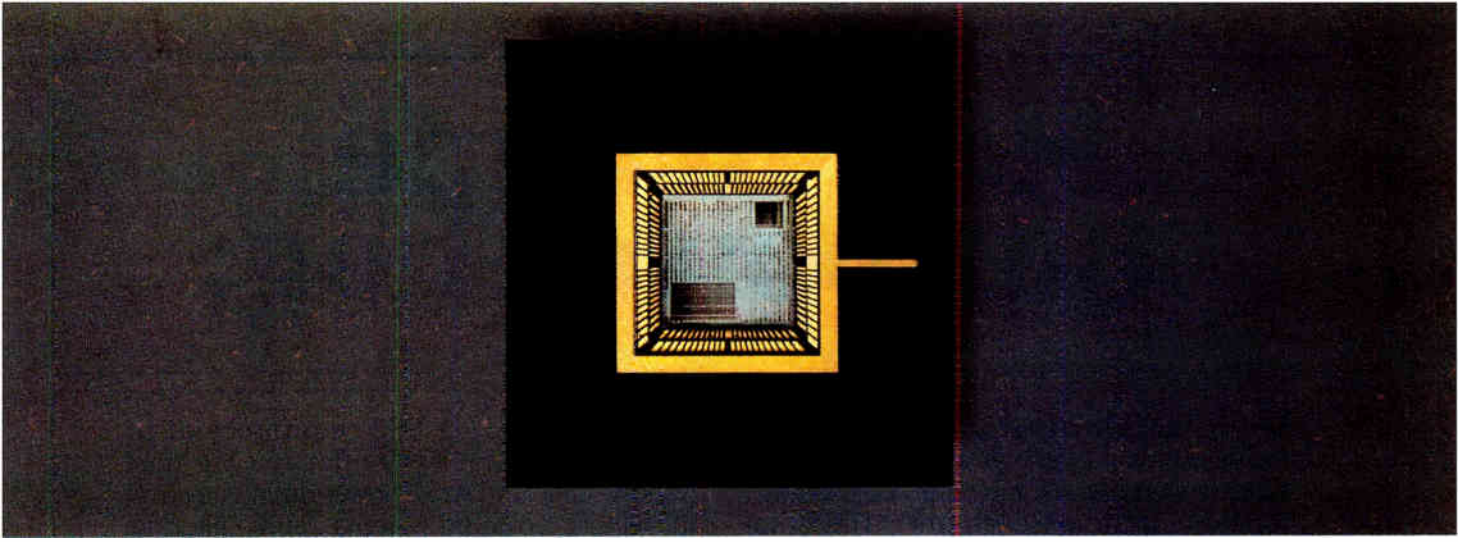

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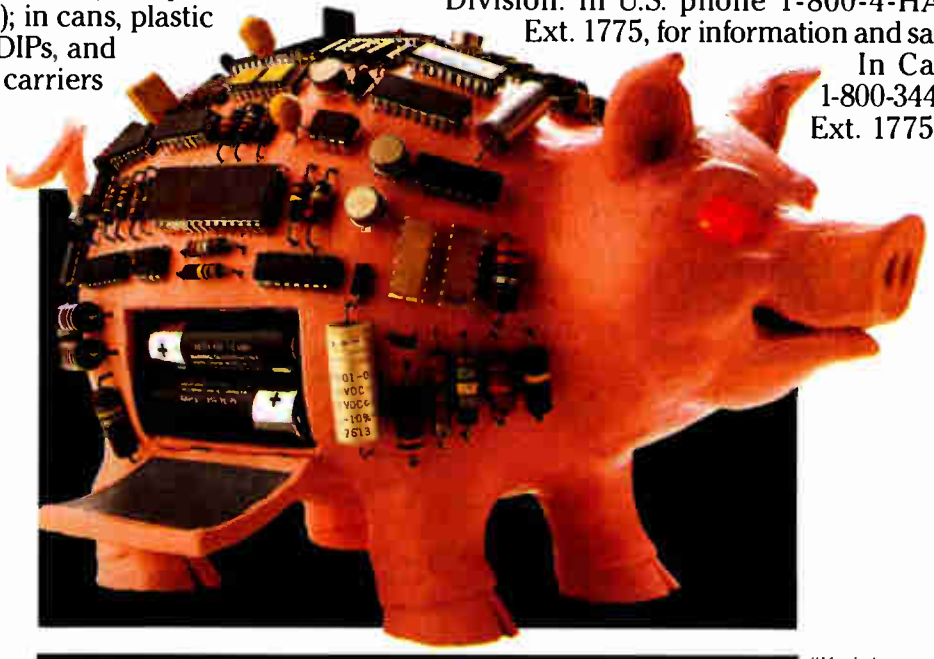

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WRINGING WINCHESTER SPEED FROM ERASABLE OPTICAL DISKS

The long wait for an optical-based disk drive that has both the capacity and speed to compete with Winchester drives is over—the Tahiti I offers a gigabyte of storage with access times of 43.5 ms and a data-transfer rate of 13.7 Mbits per second

by Jonah McLeod

Maxtor Corp. aims to resolve the dilemma that faces systems integrators who want the capacity of magneto-optic storage systems but need more speed than such drives can now provide. So far, using the up and coming erasable magneto-optic contenders has meant gaining the capacity but sacrificing performance. For instance, earlier Hitachi Ltd. and Sony Corp. units exhibited rather sluggish average access times of 100 ms and data transfer rates of 7 Mbits/s or less. Basically, these products have only removable high capacity—around a half a gigabyte—to commend them to system integrators. Their performance is just not good enough to serve as the main storage device in a computer system.

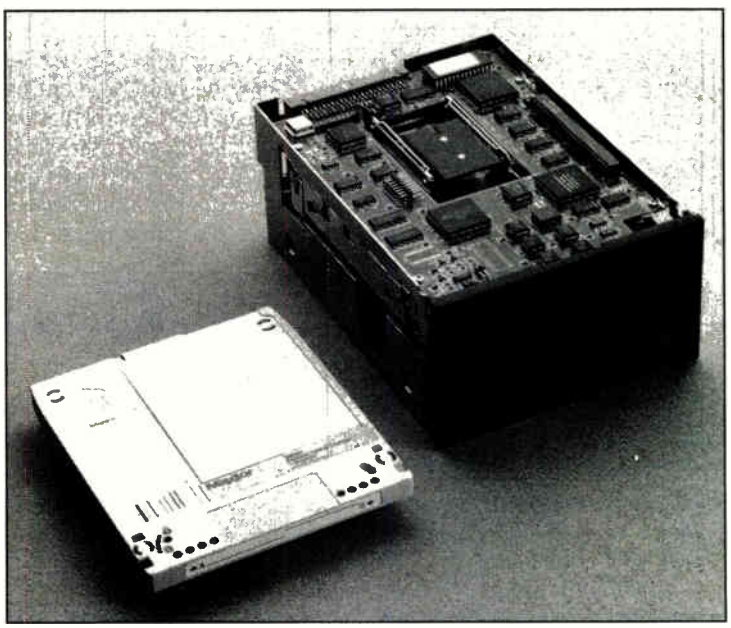
Now Maxtor is rolling out a 5¼-in. magneto-optic disk drive that the San Jose, Calif., company calls the Tahiti I. The new drive drops the average access time to 43.5 ms and transfers data at a fast 13.7 Mbits/s—but at the same time offers up to a gigabyte of storage (see fig. 1). Maxtor expects the drive to sell for $2,500 in original-equipment-manufacturer quantities; it has samples ready to ship now. As for the magneto-optic media, the company has one qualified source, the Philips-Du Pont Optical Company of Wilmington, Del., and is close to qualifying two Japanese vendors. Disks will sell to the end user for around $150 each.

To achieve its fast average access time, the Maxtor drive uses an innovative split-optic read/write head that reduces the mass to be moved—typically 100 grams—by 50%, to 50 grams. Contributing to the faster access time is a proprietary one-step seek which reduces seek time by 10 ms over the two-step processes of other optical drives.

To achieve its fast data-transfer rate, the drive's read/write electronics borrows heavily from the company's Winchester disk-drive technology. Earlier drives with 7-Mbit/s transfer rates have a window of time 80-ns wide to capture each bit read from the disk. By contrast, the Tahiti I drive performs the capture in 37 ns with equal data reliability.

And the drive can store up to 650 Mbytes of data, the maximum specified by the American National Standards Institute's X3B11 committee, which is attempting to set a 5¼-in. magneto-optic disk format standard. Or the drive can go to a nonstandard recording method, called zone CAV (constant angular velocity) recording, which allows it to pack a full gigabyte on the 5¼-in. disk. The drive can read and write to either an ANSI-standard or a zone CAV disk at any time.

The magneto-optic drive should penetrate many traditional magnetic storage applications, predicts Skip Kilsdonk, vice president of marketing at Maxtor. "Our high-end 5¼-in. unit comes close to meeting Winchester drive performance," he says, "so we expect to begin appearing in work stations and file servers currently using Winchesters. A work-station manufacturer can replace a low-end Winchester with an erasable optical drive. Or the system builder can stay with a single high-capacity Winchester and offer additional storage capacity in the form of an erasable optical disk drive." In this configuration, the system's magnetic disk drive contains information that is not subject to frequent change, like the operating system or application programs. The magneto-optic drive con-



1. Maxtor's erasable magneto-optic disk drive can compete with Winchester drives on performance and meets proposed ANSI format standards.

tains data that is to be processed on the system, and its disk can be removed just like a floppy; however, performance and capacity are comparable to a Winchester. Back-up of the Winchester comes automatically because of the removable disk.

The main problem in reducing average access time below 100 ms has been the mass of the optical read/write head, a mass that must be moved during a seek operation. A typical read/write head consists of a complex system of associated lenses, prisms, and mirrors, along with a laser diode and detector. In addition, servo information determines whether the head's lateral or vertical position should be changed. The information is used to keep the head centered over the track and the read/write laser beam in focus. This entire assembly plus the actuator arm can weigh over 100 g. By contrast, the read/write head and actuator arm of a high-performance Winchester weighs less than 10 g. It's no wonder that Winchester drives have access times of less than 30 ms, while optical drives' access times are higher than 100 ms.

To achieve its faster access, the Maxtor design separates the read/write head into two parts, one fixed and one movable (see fig. 2). "The movable part of the optics contains only the turning mirror, which moves the laser beam laterally over a track and the objective lens," says Gordon Knight, director of optical technology at Maxtor. Every other head component is contained on the fixed part of the head. "Besides a 50% reduction in weight of the movable element," says Dana Gauthier, marketing director for optical products at Maxtor, "the drive becomes much more resilient to shock and vibration." Because the mass of the head is much reduced, it can be more easily moved back on track if accidentally knocked off.

The Tahiti I's proprietary seek operation also helps to cut the time it takes to get access to data. Normally, an optical drive performs a seek operation in two steps. First, a coarse seek moves the head to within a few tracks of the desired one; then a fine seek moves a tracking mirror to the desired track.

The Maxtor drive, by contrast, requires only one step. "During a seek, the read/write head accelerates toward the target track," says Knight. "As the actuator moves the head across the disk surface, the head detects the tracks that are being crossed and the drive's microprocessor controller counts the number of tracks being crossed, so it can determine where the head is on the disk surface, relative to the target track." As the actuator nears the target track, the microprocessor begins to decelerate the head and read the sector headers of tracks being crossed to determine the actual track number.

Once it finds the correct track, the microprocessor stops the read/write head and begins to read servo data so that it can adjust the head exactly in the center of the track. In this manner, the actuator brings the head to rest right on the target track without having to perform a second fine seek operation. The Maxtor approach cuts about 10 ms off the average seek time over a drive using the two-step seek operation. "Our technique in performing this one-step seek operation is so unusual that we are applying for a patent," says Knight.

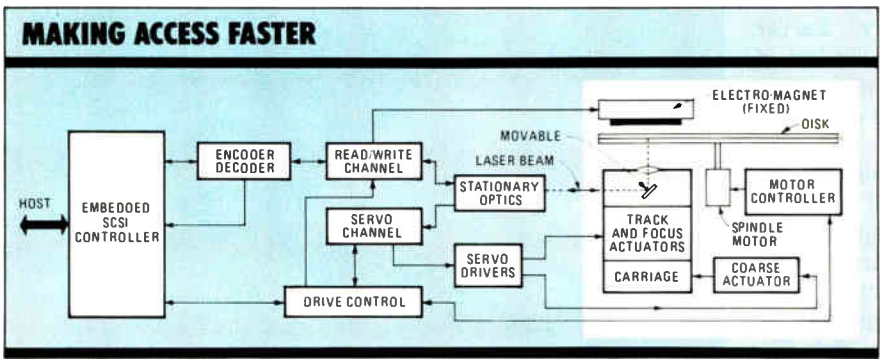
SPEEDY TRANSFER

A fast average access is one element of a drive's overall performance. Another is how fast data can be transferred from the disk surface to the computer system. Factors affecting that rate are the spacing of bits within a track and the rotational speed of the disk.

Transfer rate can be easily increased by keeping bit density constant and increasing the rotational speed of the disk. However, a third factor limiting the data transfer rate is the drive's read/write electronics, which must be able to handle the stream of bits coming off the disk. "The disk on the Maxtor drive spins at 2,200 RPM, significantly faster than the 1,800 RPM of most other optical drives," says Gauthier. As a result, the 13.7-Mbit/s data transfer rate of the drive is nearly twice that of most other drives.

In reading data from a disk, the drive must synchronize to a clock signal derived from the disk data, and at the appropriate interval or window look for the presence or absence of a pulse to determine if a 0 or 1 bit is coming from the disk. A phase-locked loop in the drive's read/write electronics locks the drive's local oscillator to the clock from the disk. The local oscillator provides timing of all operations within the read/write circuits. By synchronizing the local oscillator to the clock derived from the disk, the read/write circuit can accurately determine when to look for a data pulse coming from the disk. A drive operating at a 7-Mbit/s transfer rate has a window that is over 70 ns wide to find the data pulse. Because the Maxtor drive moves data at twice the speed of other units, its window is only 37 ns wide.

One feature of the Maxtor drive's read/write electronics, not common on others, is its ability to switch frequencies to accommodate rapid changes in data transfer rates. This is necessary for the two recording modes, normal and zoned CAV, selectable from the host computer. The bit density on a disk using normal mode recording is 20,484 bits/in. at the inside diameter of the disk. Thereafter, in each track outward from the center, the bit density decreases until the track nearest the outside diameter of the disk has 50% of



2. To achieve its faster 43.5 ms average access time, the Maxtor drive design separates the read/write head into two parts, one fixed and one movable.

the bit density of the innermost track.

Zoned CAV recording takes advantage of the fact that outward tracks hold more data. For this mode, the microprocessor divides the tracks into bands and puts more sectors in the bands further from the disk center. This achieves greater storage capacity. To accommodate the abrupt changes in bit density from one band to the next, the read/write electronics can quickly switch the oscillator frequency to synchronize to a different disk clock frequency.

Achieving capacity and performance would seem difficult to pull off in a drive compatible with the emerging ANSI X3B11 standard. The standard fixes capacity. It defines the disk recording format, details the sector size, the number of sectors per track, and the number of tracks on the disk. The total capacity then is simply the number of tracks times the fixed capacity of each track. The standard allows either 512- or 1024-byte sector sizes. With the former, a disk can hold 596 Mbytes; with the latter, 652 Mbytes on both sides of the disk, which must be flipped over manually. No currently available optical drive supports two-sided disk operation.

The dual recording modes are Maxtor's way of getting around the ANSI capacity limitation. In normal mode, the drive adheres correctly to the ANSI X3B11 committee recording standard specification and provides the specified capacity. "For the user who wants capacity and is willing to accept a nonstandard recording format, we offer him zoned CAV recording," says Gauthier. "With this format, the user can store 1.024 gigabytes of data on a two-sided disk if he chooses 1024-byte sector sizes. Or using 512-byte sectors, he can store 932 Mbytes on a two-sided disk. Moreover, he can still read and write standard disks on the same drive."

In zoned CAV with 1024-byte sectors, the microprocessor divides the 18,816 tracks on the disk surface into 16 bands; 29 bands, if recorded with 512-byte sectors. To achieve greater storage capacity, the drive stores more sectors in each track in bands further from the disk center. On disks formatted with 1,024-byte sectors, there are 17 sectors in each track in the band nearest the disk center. In tracks within the next band outward from the disk center, 18 sectors are stored in each track. In the band nearest the outside diameter of the disks, tracks contain 33 sectors. Disks recorded with the 512-byte sector sizes contain 31 sectors per track within the innermost band and 60 sectors per track in the outermost band. □

For more information, circle 482 on the reader service card.

IF YOU LIKE TAHITI, WAIT UNTIL YOU SEE FIJI

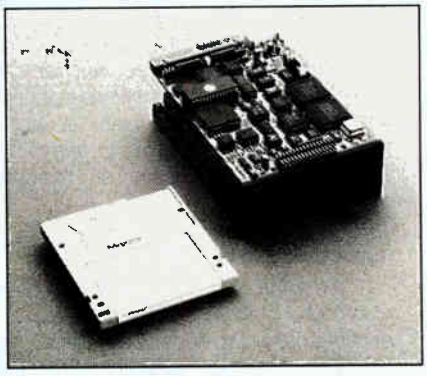
In addition to its 5¼-in. Tahiti I, Maxtor Corp. is also launching an aggressively priced, high-capacity 3½-in. magneto-optic drive, the Fiji I. Offering 160 Mbytes of storage capacity, 100-ms average access time, and a data transfer rate of 2 Mbits/s, the drive sells for less than $1,000 in large original-equipment-manufacturer quantities (see figure). Disks for the erasable optical drives will cost on the order of $25.

Maxtor sees the smaller drive as a commodity product sold in high volumes for use in personal-computer applications, replacing tape drives for backup purposes, says Skip Kilsdonk, vice president of marketing at Maxtor. The disk will not be used for main disk storage on any of these systems because its performance is not sufficient. However, it will outperform the floppy-disk and tape drives now commonly used in these systems and will offer much greater storage capacity than either.

The 3½-in. drive comes without a Small Computer Systems Interface controller, which is contained on a separate board. (The controller is the same as the one used in the 5¼-in. drive.) To make it easy to incorporate the drive into a system, the company provides a half-high bezel that the user can put around the 3½-in. disk to allow it to go into a half-high floppy slot of a personal computer.

"The technology in the Fiji I is similar to that of the larger drive," says Kilsdonk. "It uses the same recording techniques so that the OEM has a common product using either drive." The drive is the product of a joint development effort between Maxtor and Seiko Epson Corp. of Tokyo.

Kilsdonk believes the 3½-in. disk will require a major OEM coming into the market and taking large quantities of drives for this market to take off. "The disk will be a super-hot floppy for a PC," he says. "In the IBM PS/ 2 and Macintosh II there is room for floppy, Winchester, and erasable optical disk drives." However, he expects the largest market will be among OEMs who are building the drive into totally new designs, not adding it to a current system.



High capacity at low cost is the promise of Maxtor's 3½-in. Fiji I magneto-optic drive.

If there is one hurdle blocking the wider use of the 3½-in. drive, it is a lack of standards. Two other 3½-in. products are under development and none of the three are compatible. One is from Verbatim. Another is being developed by several Japanese drive makers. Each of the three has a different disk-cartridge design, and a debate is raging over the size, thickness, and diameter of the cartridge. The Maxtor disk has a hub; the others do not. Maxtor's cartridge is thinner than the alternatives, small enough to allow it to fit into a shirt pocket, which the company believes could be a key user feature.

Both Maxtor and the Japanese contingent are are opting for a single-sided disk, while Verbatim is after a double-sided disk. Single-sided disks provide the lowest possible media cost, since there is twice the chance of getting a good disk. Whether the market will demand standard media before buying up the 3½-in. magneto-optic drives remains to be seen. What is certain, though, is that Maxtor and the others think this is a fast-breaking market. They are pushing ahead with product offerings, hoping to land that first major OEM account.—*J. McL.*

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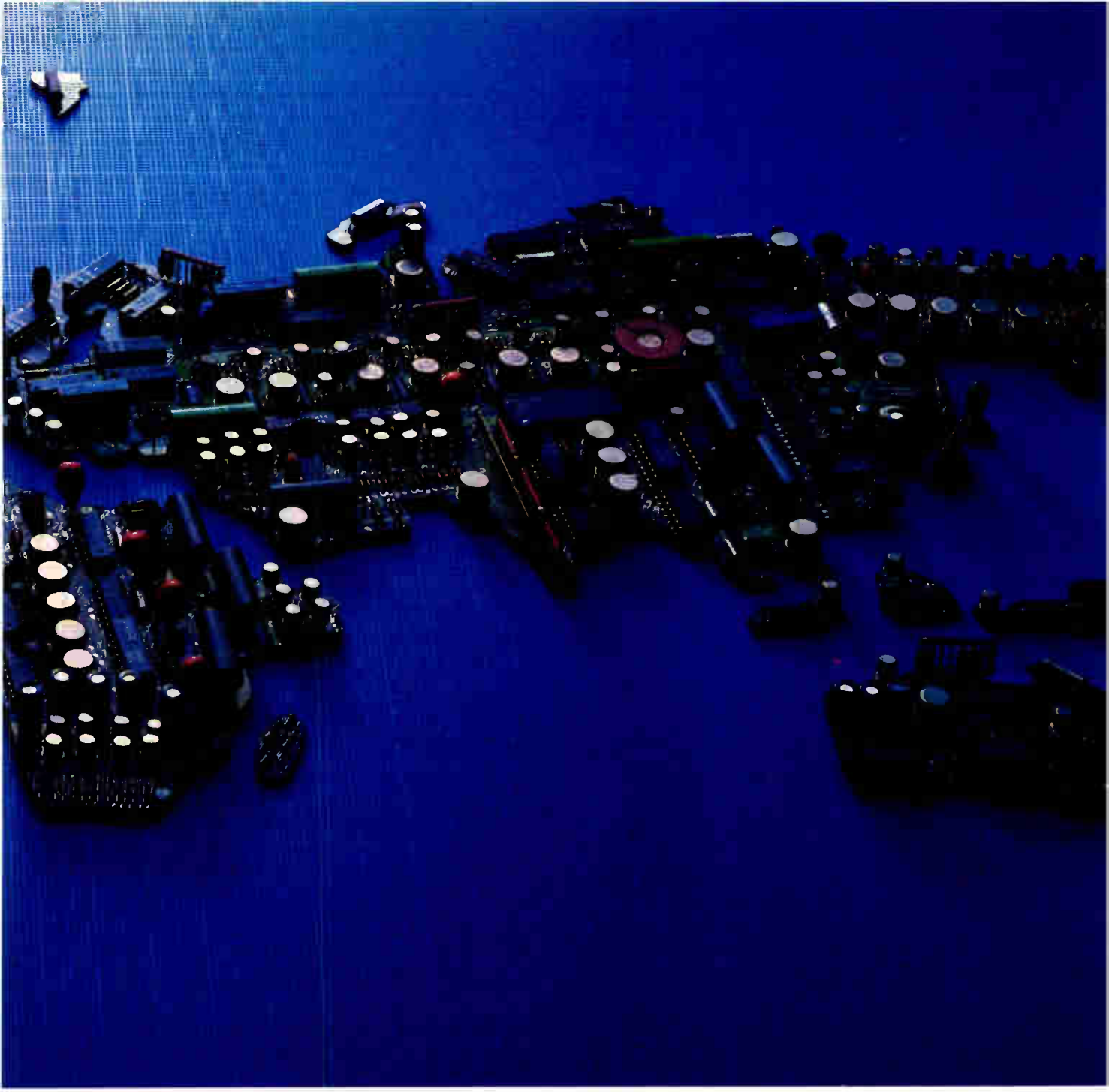

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HOW MAXTOR GOT BACK ON ITS GROWTH TRACK

At this time last year, Maxtor Corp. was riding high—in each quarter for two years, sales were setting records. It had scored big by using leading-edge technology to dominate the high-capacity, high-performance Winchester disk drive market [*Electronics*, June 11, 1987, p. 49]. But in its all-out drive for fast growth, the San Jose, Calif., company had taken a major risk with a fragile manufacturing process and it was about to get into big trouble as a result.

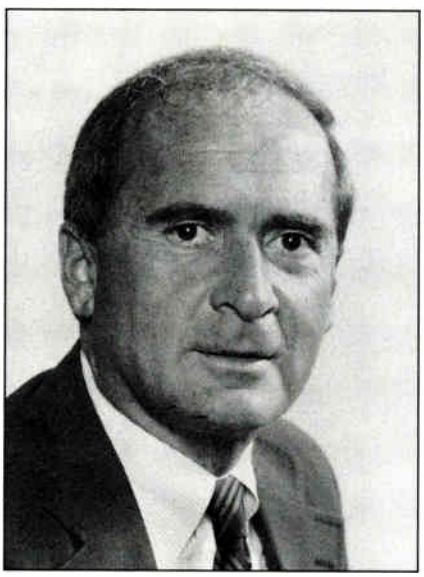
What Maxtor had done was to bank the entire company on one primary thin-film read/write head supplier, Read-Rite Corp. And in the spring of 1987, that Milpitas, Calif., manufacturer suddenly found that it had real trouble getting sufficient yields to meet its commitments to Maxtor. By June 1987, it was shipping significantly fewer heads to Maxtor; it admitted that its production was down by 50%. Maxtor was getting only about 80,000 read/write heads per month, which slowed down its own disk-drive production lines significantly.

As a result, Maxtor's sales and earning were hit hard and the disk driver maker suddenly lost its momentum. "In the first three quarters of 1987, our revenues were relatively flat," concedes George Scalise, Maxtor's president and chief executive officer. While quarter-to-quarter sales had increased by a resounding 25% late in 1986, quarterly sales throughout most of last year hovered around the $50 million level.

Maxtor moved fast. It began checking out alternate suppliers for the hard-to-build head. Fortunately for the company, when the trouble arose "there was a program underway inside Maxtor to bring additional sources of the heads on line," says Scalise. But they had to be qualified individually, and each drive had to be tweaked and a small redesign effort done before they qualified. The company eventually signed up four firms to supply heads along with Read-Rite: Peripherals Components International, a division of Control Data Corp.; Applied Magnetics; Dastek; and TDK Electronics. Maxtor also began redesigning its drives to use the more readily available ferrite head.

Things started improving rapidly by fall. "By September we were beginning to see the first improvement in availability of the heads," Scalise says. The company was then receiving 120,000 heads a month. "Revenues started turning up," he says, rising to $60 million in the quarter ended in December.

But fourth fiscal quarter results, announced in late April for the period ended March 27, were the real proof that the company had indeed got back on its growth track. Sales shot up 55% to $85.7 million from the year-ago quarter, while net income was up 37% over the same period to $6.1 million. For the fiscal year, sales rose 49% to $274.2 million, while net income—although rising in the fourth quarter—was still off a third to $14.1 million for the year.



CEO Scalise: Maxtor moved quickly to revamp operations that stagnated 1987 revenues.

But Maxtor didn't stop there. The shortfall in heads and the resulting flat revenues spurred the company to revamp its operation elsewhere. Manufacturing was automated to improve quality. A manufacturing information system was installed, allowing Maxtor respond more quickly to customer demands. And the company invested heavily in new optical-storage technology to expand into new markets.

In addition, the company established a disk-drive group under Leon Melman, vice president of disk-drive products. "Now we have someone responsible for the disk-drive program who is focused on satisfying the customer, getting the cost out of the drive, getting the yields up—all of the factors associated with running a business," Scalise says.

The automation program was originally intended to improve quality, which it did, but Maxtor also found that it helped to cut costs. One part of the program is an automatic disk loader, which is going into production at the company's Singapore manufacturing facility. "We have the ability to automate the rest of the assembly as well," Scalise says. But he plans to mechanize production in stages, to prevent disruptions in the production flow.

To supplement the automation, Scalise says, the company has installed an ambitious system that tracks product lots through the entire process, controling inventory as well. "Having the information system will help us make more commitments to our customer with much greater assurance of delivering on time," Scalise says. "I believe we will get to the point where we are shipping on time 95% of the time," he says. The industry norm today is 80% on-time delivery.

While the company was busy getting back on its growth track, it did not neglect research and development of new products. Scalise recognized that getting an optical-storage product into volume production was going to require a large investment and that it was not going to provide an immediate return—the RXT800 write-once optical drive was shipping in hundreds of units a month, where a comparable Winchester would have been shipping in thousands a month. Nevertheless, he increased funding for the project in the latter part of last year.

Scalise says Maxtor is well positioned for the next few years. It has high-end 380-Mbyte Winchesters and lower-priced, smaller Winchesters to generate revenues in 1988. He sees the latest 760-Mbyte and 3½-in. drives—to be announced in June—coming on line in 1989 to carry the company into the next decade. Following closely behind, he says, will be the company's newest magneto optic erasable drives—Tahiti and Fiji. Scalise expects them to begin generating significant revenues in 1990.

–Jonah McLeod

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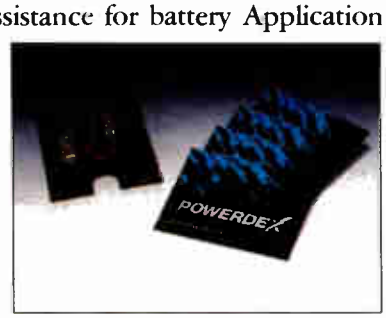

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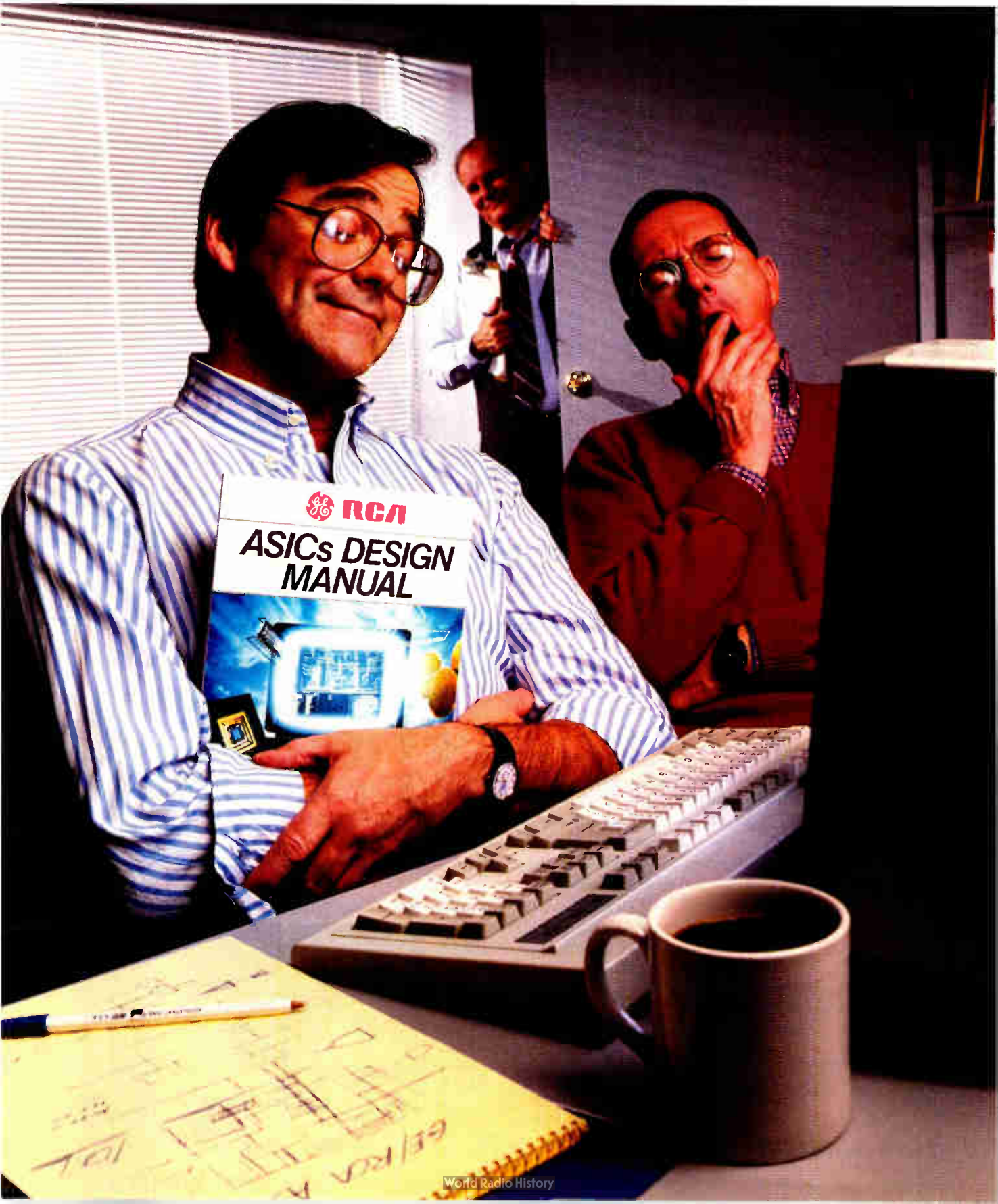

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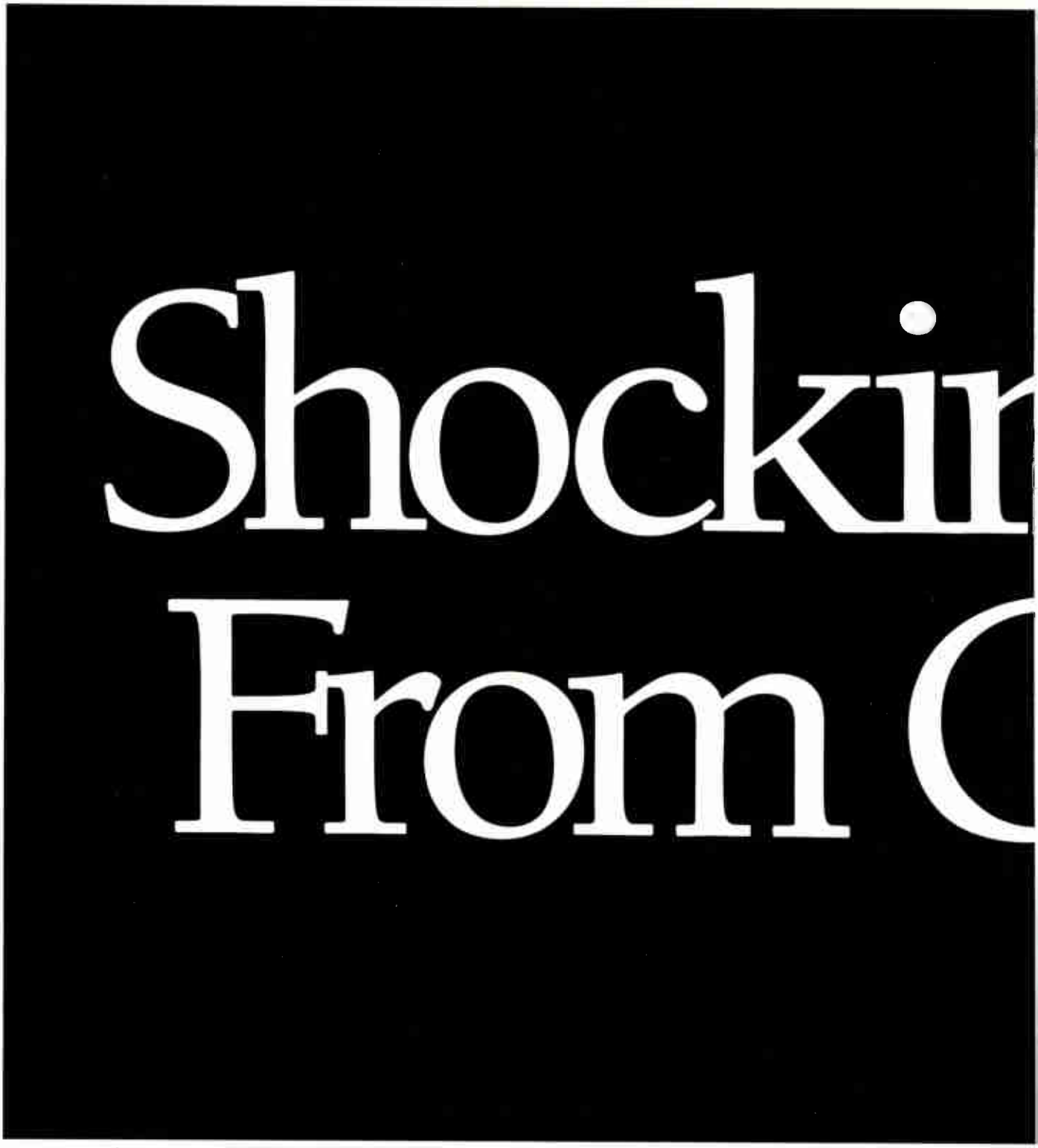

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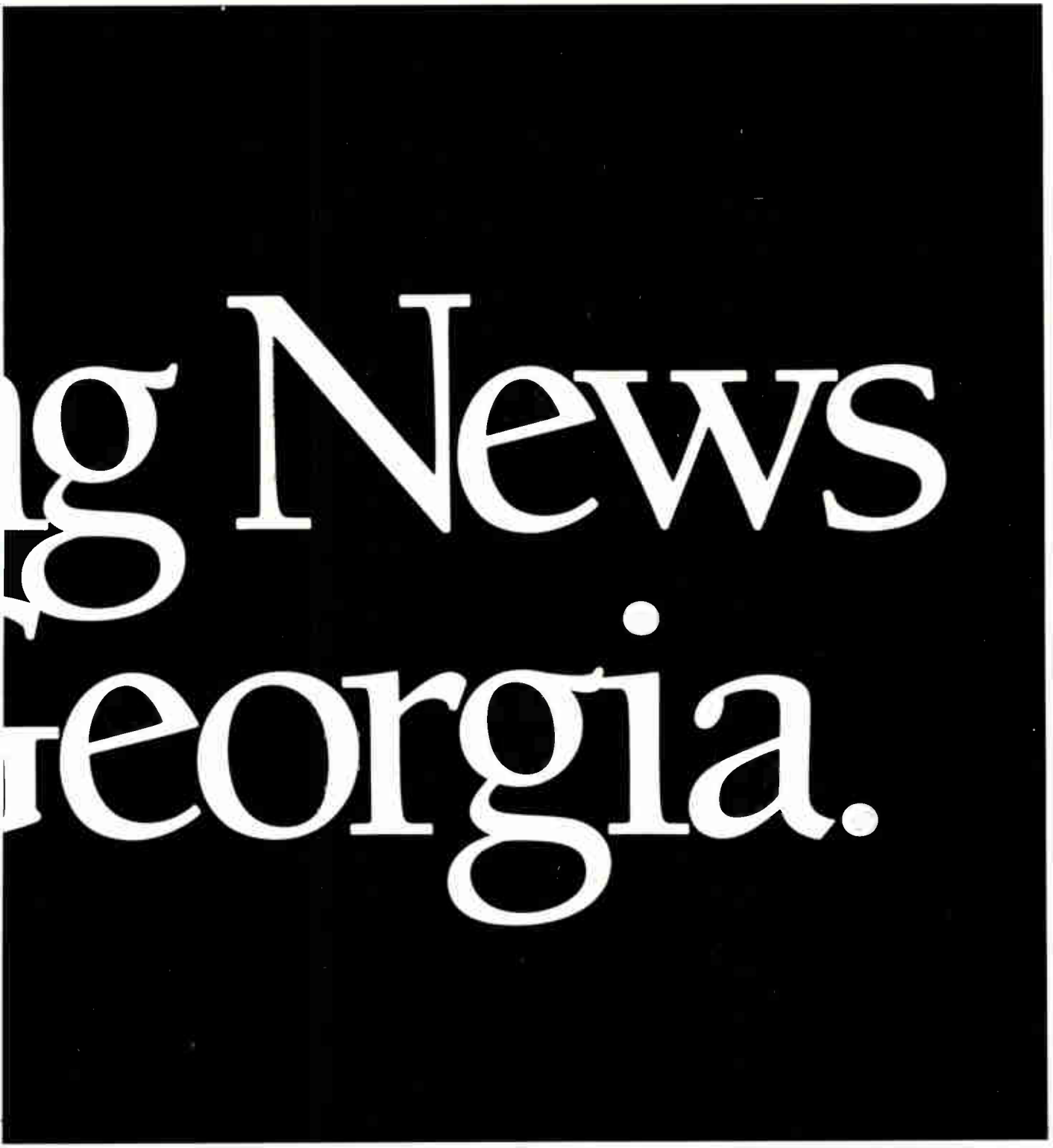

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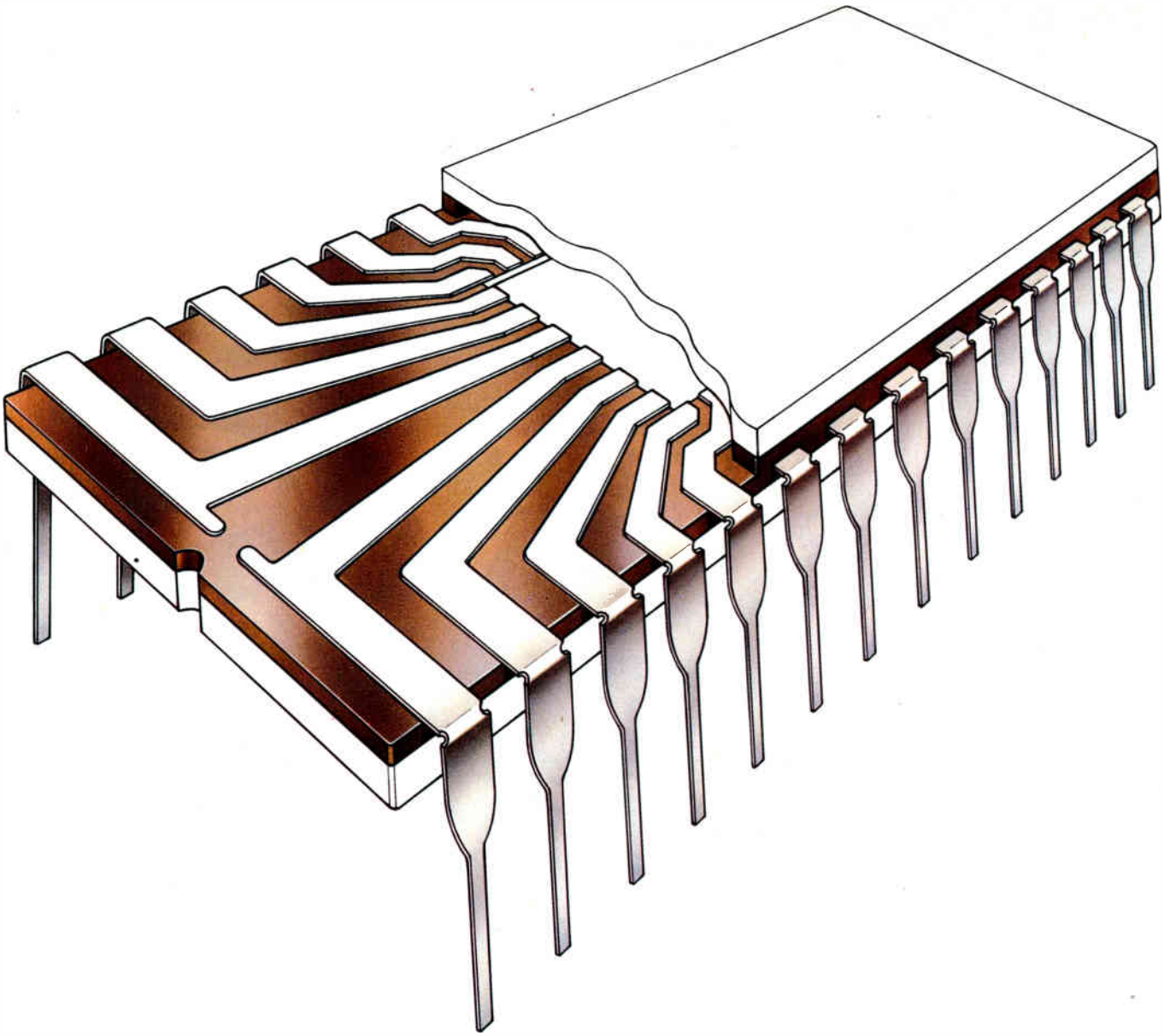

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COMING SOON—AN ECL ARRAY THAT'S THE BIGGEST YET

A 16,000-gate device from Plessey/AMCC achieves 100-ps delays with a channelless architecture

Joining forces to take on the leaders in the high-speed bipolar emitter-coupled-logic marketplace, Applied Micro Circuits Corp. of San Diego, Calif., and Plessey Semiconductors Ltd., Swindon, UK, have come up with a blockbuster: the first-ever 16,000-gate bipolar ECL array and the first bipolar array to use a channelless architecture. The array also sports a spectacular 100-ps-per-gate delay with a worst-case power consumption per chip of no more than 16 W. In addition to the use of the channelless architecture, key elements in achieving this amazing combination of speed, power, and density are the use of an advanced 0.6-μm trenched-emitter-bipolar process from Plessey and the use of a three-level sea-of-cells methodology incorporating proprietary circuit techniques developed by AMCC to minimize delay as well as increase gate utilization to 95%.

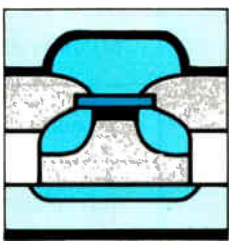
To date, the highest-density bipolar ECL arrays available reach 12,000 to 13,000 gates and then only with the use of four levels of metal interconnect. Moreover, gate delays on present high-density ECL arrays range from about 300 to 400 ps, but at the cost of higher power. To achieve comparable power dissipations, present arrays run slower—in the range of 400 to 600 ps.

To be formally introduced May 16-19 at the Custom Integrated Circuits Conference in Rochester, N. Y., the 16,000-gate Q20160 is the flagship of a new Q20000 family. Initial devices in the family will also include the 8,000-gate Q20080 and the 1,500-gate Q20015. Test devices ranging in density from 200 to 500 gates have already been fabricated with first silicon on first members of the 1,500- to 16,000-gate family expected in June. Sampling is expected to begin in December and volume production will start in the first quarter of 1989.

Ray Gleason, Plessey's chief marketing executive, says the joining of forces between his company and AMCC gives both a leg up—technically and marketwise—in the highly competitive bipolar ECL-gate-array business [*Electronics*, March 3, 1988, p. 42] that neither could have achieved separately. "Each of us had developed an expertise that gave us individually a good foothold in the market," he says. On the AMCC side, although the company has always had a good state-of-the-art bipolar process, its claim to fame has been its ECL circuit-design expertise and its macrocell library of semicustom circuit building blocks.

On the other hand, Gleason says Plessey has always had a good reputation for pushing the state of the art in bipolar processes [*Electronics*, Aug. 20, 1987, p. 39], but has until recently applied that expertise to its own differential logic circuit technology. "It was quite clear that if Plessey was to play a major role in the bipolar ECL gate-array business, we would have had to make a major investment in developing a state-of-the-art library of building blocks," says Gleason. "Similarly, at AMCC, company executives were faced with making a significant investment in process technology."

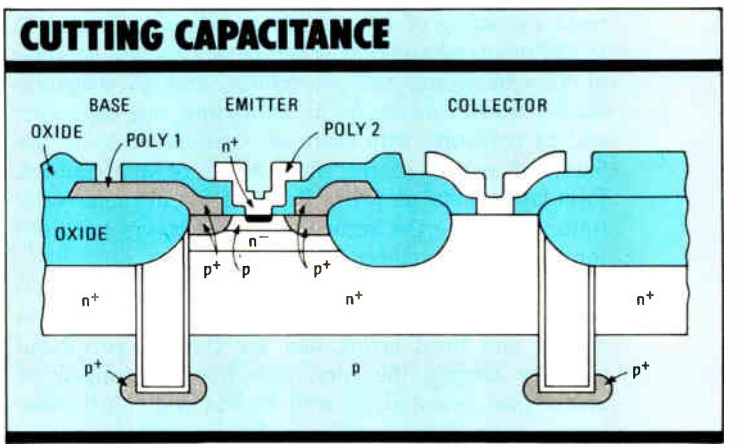
Plessey's contribution to the package is its new HE bipolar process, which incorporates polysilicon-based emitter contacts, trench isolation, and an advanced base emitter structure (see fig. 1). The company says the trench isolation reduces the collector-substrate capacitance to only half that of the standard local oxidation isolation technique and increases packing density by a similar amount. To reduce parasitic capacitances, and thus improve performance, polysilicon resistors are used. Polysilicon-polysilicon capacitors are employed to stabilize the ECL 100-K reference voltage generators.



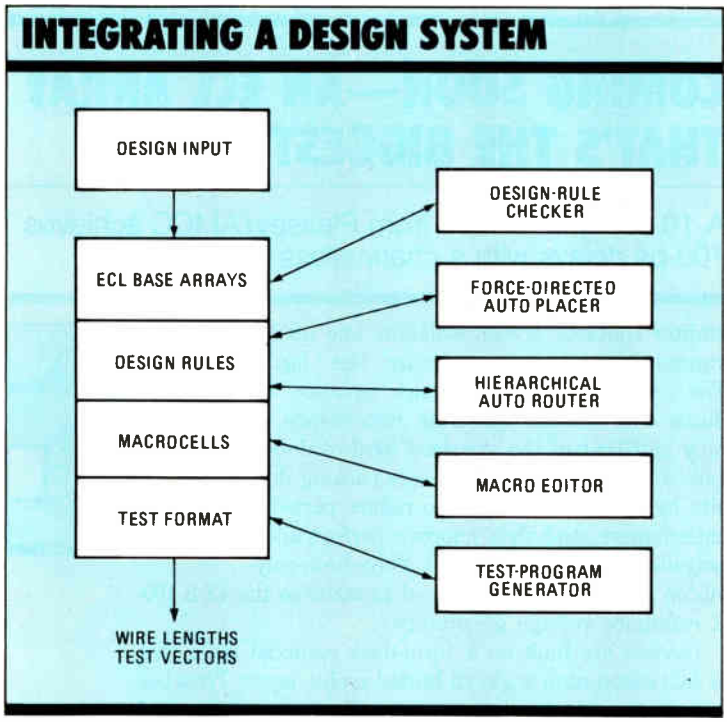
Devices are built on a 1-μm-thick epitaxial layer that is fabricated atop a global buried n-plus layer. Trenches are 1-μm wide by 5.5-μm deep, lined by nitride and oxide, and filled with polysilicon. To eliminate parasitic buried n-plus/substrate/buried n-plus transistor structures and suppress other undesirable side-effects, the process uses channel stop implants, followed by oxide growth and nitride deposition over the whole layer.

In the first-generation process, HE1, which will initially be used in the current round of AMCC/Plessey arrays, peak toggle rates have reached 14 GHz at 5 mA per gate. Whereas the HE1 features 5-μm metal and via pitches, a second-generation process, called HE2, is under development.

Incorporating a more advanced base emitter, an optimized epitaxial layer, and a 3.5-μm pitch, the second-generation process allows the fabrication of gates with toggle frequencies in excess of 22 MHz at only 2.5 mA. And where the upper limit of the present process which is used in conjunction with the AMCC architecture is about 20,000 gates, the future HE2 process will allow the fabrication of bipolar ECL arrays as dense as 30,000 to 50,000 gates with no sub-



1. Plessey's new HE1 bipolar process uses trench isolation and polysilicon resistors and capacitors to reduce collector-substrate capacitance.



2. The gate-array design system offered by AMCC puts circuit design, simulation, layout, and testing all in one package.

stantial increase in die size or chip power dissipation.

Using this process as a starting point, AMCC engineers have developed a family of ECL/TTL arrays with densities up to 16,000 gates by combining for the first time in an ECL array three levels of metalization with a channelless sea-of-cells architecture. This combination allows the fabrication of an array with gates that can achieve 100-ps delays with a fanout of three, about twice the performance of any other comparable device, says Michael Hollabaugh, director of marketing at AMCC. At the same time, die area was reduced by about 40% by eliminating routing channel space between the columns of cells. When applied to this new family, the HE1 process results in arrays with gate-toggle rates of 1.2 GHz, a power dissipation per gate ranging from 1.5 to 2 mW, and chip power dissipation ranging from 8 to 16 W.

There are 1,500 to 16,000 gates in the array, depending on density, organized into a sea-of-cells arrrangement consisting of 400 to 4,290 basic core cells and 80 to 292 input/output cells. Each basic core cell consists of 42 transistors, two capacitors, and 25 resistors. Each I/O cell consists of 20 transistors, one capacitor, and 24 resistors, with each cell customized using the first and second of the three levels of interconnect. First-layer metal is primarily used for intramacrocell routining, while the second and third layers are used for global interconnect.

The first level of metal is also autorouted for I/O communications to the core cells, allowing busing on second and third layers and for the I/O peripheral circuitry ringing the core, reducing the number of power pins required, as well as bus width. All three layers, says Hollabaugh, can also be used for power bussing. Containing 714 horizontal and 840 vertical routing channels for global interconnect, the core cells are arranged in a square matrix. In the 13,000-gate array, they are organized into 42 rows by 42 columns with one extra column on each side for use by the on-chip threshold and clamp generator circuits. The I/O cells are organized with 64 cells on each side of the array, three of which are designed to support ECL 10K/100K signals while the fourth is capable of handling either ECL, TTL, or a combination of the two.

A key design goal of the AMCC half of the development team, says Hollabaugh, was developing an ECL array that could take full advantage of the internal gate delays of 100 ps possible with Plessey's 0.6-μm HE1 process without substantially increasing chip power. The key was in finding some way to enhance the drive capability of the I/O circuitry but do it with less power than conventional ECL output circuitry, according to AMCC designers Bruce Coy, An Mai, and Ray Yeun. The aim, says Hollabaugh, was designing an architecture that even in its most dense form—the 13,000-gate array—would consume under 10 W, permitting it to be used in low-cost air-cooled computer systems.

However, say the designers, this is easier said than done, especially at the small submicron device geometries employed in the Q20000 family. One of the most troublesome problems is that interconnect parasitics tend to dominate the net gate delay.

The standard solution to this problem is to buffer the high-speed gate with an emitter-follower circuit, biased with a simple current source. The sourced current from this standard configuration, they say, is more than adequate for most ECL designs. However, the sink current is limited by the static bias level of the emitter follower. While this was bearable in arrays using 2-μm and above geometries, at submicron levels, the output emitter follower bias levels become a higher and higher percentage of the cell current, producing skewed or asymmetric propagation delays.

To overcome this problem, AMCC developed a proprietary dynamic discharge current circuit to reduce static cell current, the culprit in current designs. The trick, its designers say, is to use a biasing scheme that in essence equalizes the dynamic and static discharge currents, producing symmetrical propagation delays.

An extra benefit of the approach is that the output stage also provides level shifting for the second and third levels of series gating, allowing signal noise margins to be maintained over a wider temperature range than in most ECL designs. This is because the temperature coefficient of the static current signal tracks and balances out the signals from the gate and threshold generators, preventing the interaction of the three levels of series gating in the circuit.

Hollabaugh notes that users will be able to design with the new ECL arrays using the same design-tool methodology now used in the company's CMOS, BiCMOS and low-density ECL and TTL arrays, but with an expanded macrocell library. Called Macromatrix (see fig. 2), the AMCC design system integrates circuit design, simulation, layout, and testing, with the output of one tool providing the input to the next. Macros for the new family were designed on this in-house macrocell development system, which is configured to provide correct-by-construction circuits. *–Bernard C. Cole*

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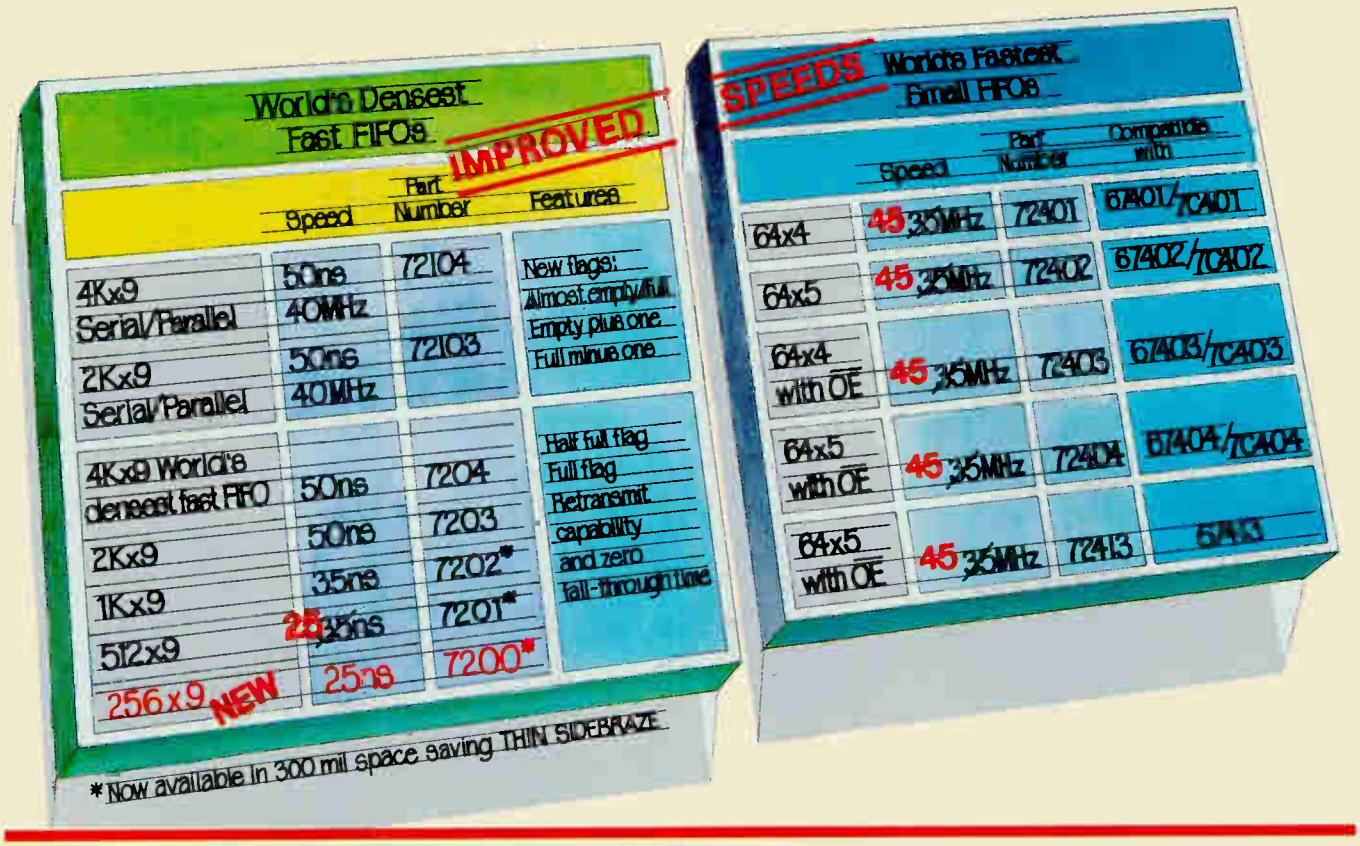

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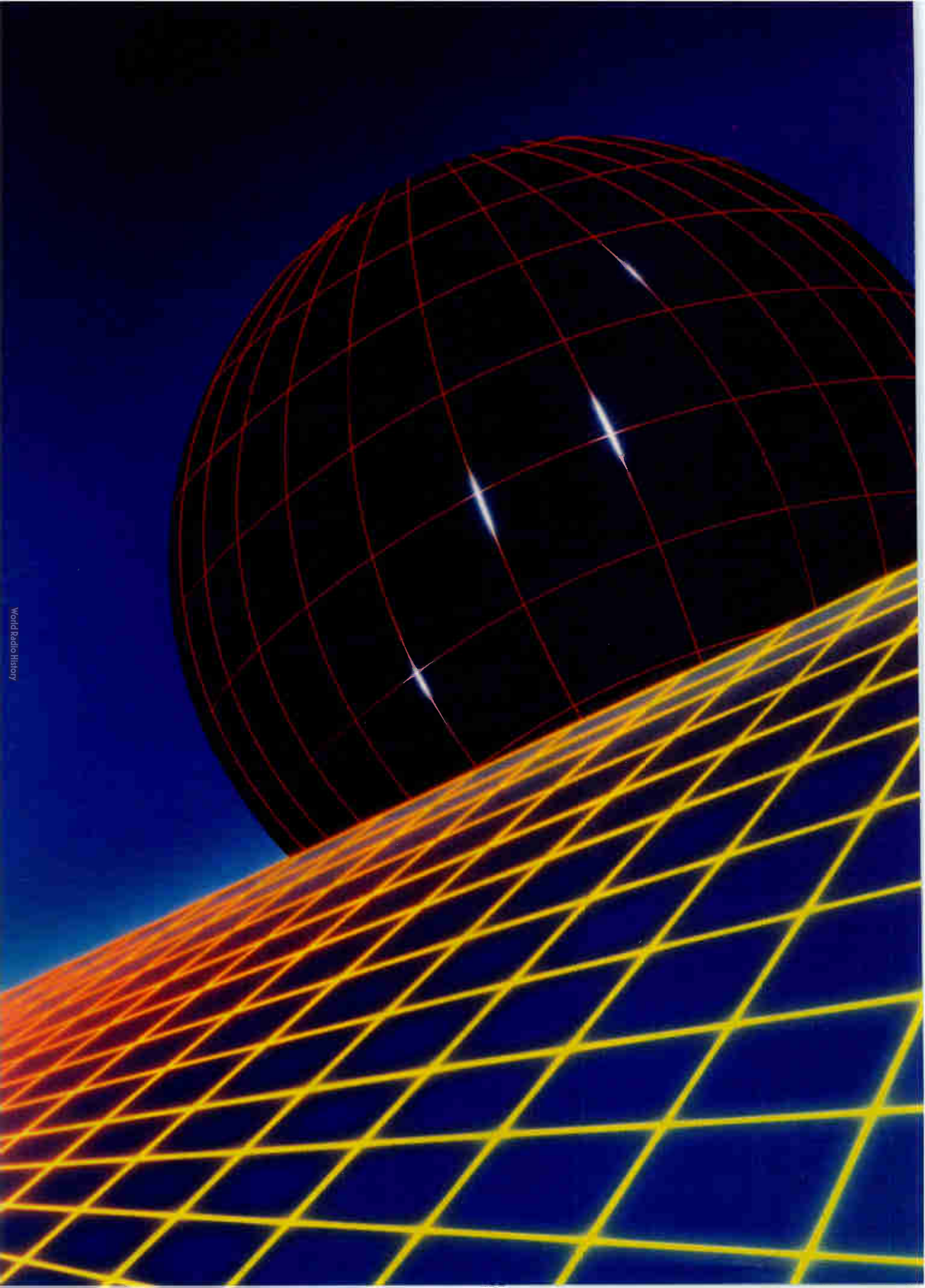

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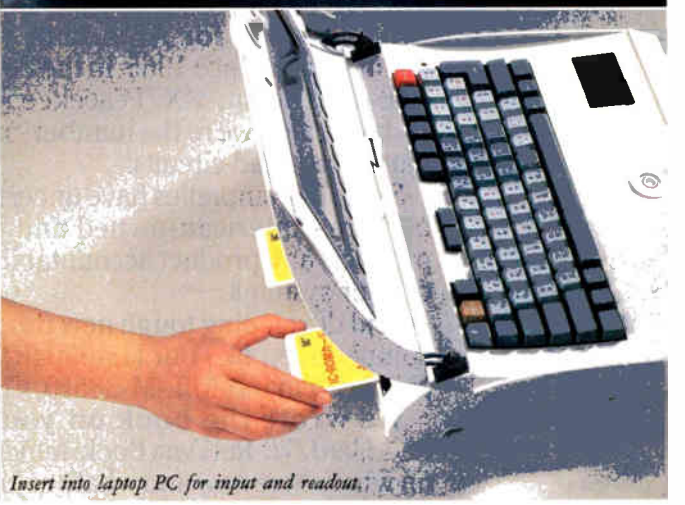

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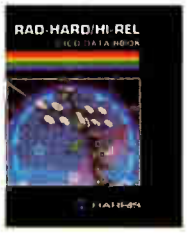

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MILITARY/AEROSPACE NEWSLETTER

PENTAGON GIVES DARPA CONTROL OF OSD RESEARCH PROGRAMS...

The Pentagon is switching some of its biggest electronics research programs out of the Office of the Secretary of Defense and into the hands of the Defense Advanced Research Projects Agency. The move could mean trouble for the programs—which are all manufacturing-oriented—because Darpa's experience in managing such projects is nil. A spokesman says Robert Costello, undersecretary of defense for acquisition, wanted his office—which had control over the programs until the transfer was made April 15—to get out of the business of program management and concentrate on what its job is supposed to be: policy guidance and oversight. Included in the move are five programs, which combined for $175 million in funding for 1988: Sematech, the joint industry-government project to develop leading-edge chip manufacturing technology; Mimic, the Microwave and Millimeter Wave Integrated Circuits program; the Infrared Focal Plane Array Initiative; and two software programs—the Software Engineering Institute, which is operated by Carnegie Mellon University, and the Joint-Stars program, which stands for Software Technology for Adaptive, Reliable Systems. The software programs are being combined in 1989 in an effort to better coordinate defense software research and development. The move leaves OSD with only two in-house efforts: the Very High Speed Integrated Circuits program, which will conclude at the end of 1989, and the Joint Ada Program Office, which is considered a policy-making organization and therefore did not fit into Darpa's charter. □

...BUT CAN DARPA HANDLE THOSE MANUFACTURING RESEARCH EFFORTS?

The big move to clean out the bulk of electronic research programs from the Office of the Secretary of Defense is not without some irony. As recently as October 1987, E.D. Sonny Maynard—director of the Science and Technology Office in OSD and the manager for four of the five programs moving to Darpa—claimed manufacturing-intensive programs like Mimic did not belong under Darpa's purview. "We're looking at putting technology in systems," he said. "Darpa looks at the next step beyond, at future technologies." Now Maynard and his crew are working for Darpa. Sources in his office say major changes are not planned—"not in the short term, anyway, though perhaps some programs will have to change in the long term." □

FINALLY, A REAL-TIME ADA KERNEL FOR DISTRIBUTED PROCESSING

Researchers at the Software Engineering Institute are developing what they say will be the first real-time Ada operating-system kernel capable of running in a distributed-processing environment. Nicknamed DARK—for Distributed Ada Real-time Kernel—the project aims to produce a portable set of building blocks from which contractors can construct their real-time Ada application environments, says Roger Van Scoy, a member of the technical staff at the Pentagon-sponsored Institute. The research team has so far completed a top-level design and is now implementing and defining the first version of the operating system kernel, using Motorola Inc.'s 68000 microprocessor as a target. But key to DARK's success, Van Scoy says, will be what comes next: "porting the kernel to a second target." For DARK to be successful, it must be able to work independently of specific compilers and processors, says Judy Bamberger, who is also working on the project. The Software Engineering Institute in Pittsburgh is already talking to potential industrial partners about adapting the kernel for use with a second processor. The only real-time Ada kernel now available is RTAda, from Ready Systems of Menlo Park, Calif. [*Electronics*, Oct. 29, 1987, p. 85]. But the researchers contend that RTAda works on only one compiler and is suited only to serial-processing systems. □

MILITARY/AEROSPACE NEWSLETTER

THIS CAD SYSTEM PICKS THE BEST VENDOR FOR ANY VHSIC DESIGN

The military market is rife with vendors hawking their custom Very High-Speed Integrated Circuit capabilities, but choosing the one best suited to produce a given design can be a dizzying task. Equipment makers must pick a vendor with whom to design the chip, yet have no way of predicting how well the part will perform when it is finally produced. McDonnell Douglas Astronautics Co. got so tired of the time-consuming and expensive process that it took matters into its own hands—the company developed a generic computer-aided design system from which circuit designs can be transferred onto CAD systems from a variety of VHSIC-class chip suppliers. Designing custom chips still takes roughly six months, but within a week the aerospace giant can compare performance characteristics—such as speed, gate delay, fault-tolerance, and power dissipation—and choose the vendor whose process best suits the particular design, says William A. Hanna, a senior technical specialist at McDonnell Douglas in St. Louis. The system has already been proven with a 12,000-gate device that was produced for McDonnell Douglas by Texas Instruments Inc. "We tried three vendors and TI's was the best performance in that application," Hanna says. "It can save months in the design process; it's the way we are going to design from now on." □

THIS AVIONICS PACKAGE WOULD ALLOW A PILOT TO TELL IT WHAT TO DO...

There's plenty of talk about putting voice-recognition systems aboard military aircraft in the future but several problems remain to be solved. The units need to be made small and light enough so they don't add critical bulk to the plane, and they need to be smart enough so they can operate when the pilot and aircraft are subjected to high g-forces, which can severely distort the pilot's voice at a critical juncture. Allied-Signal Aerospace Co., and its partner in the project, Crouzet SA, say the first problem will be easy to lick. They're already building prototype connected-word voice recognizers into a compact 12-by-7.5-by-5 in. box, and a board-level version is coming next, says Thomas Bizzoco, senior marketing representative for Allied-Signal Aerospace Co.'s Flight Systems Division in Teterboro, N. J. But battling the distortion problem will be tougher. "We've done it so far through filtering and compression techniques," he says, but "we're not sure how any great g-forces would affect the system." The Allied-Signal design is aimed at reducing a pilot's work load by allowing him to call up displays and flight data with his voice—and not his hands, which stay on the control stick. Airframe contractors are beginning to look at these systems, he says, and at least one major builder is seeking to evaluate competing voice systems. □

...WHILE THIS SYSTEM WOULD NEED ONLY A THOUGHT TO REACT

In his 1982 film *Firefox*, Clint Eastwood steals a Soviet fighter plane and then flies it by mentally giving his flight commands—in Russian, of course. While that's still the stuff of science fiction, researchers at the Wright-Patterson Aerospace Medical Research Laboratory near Dayton, Ohio, say it might some day be possible. Basic research indicates that a pilot could one day control an airplane's mechanical systems with his brain waves. In experiments performed last year, each of eight human subjects tested was able, with training, to regulate the amount of brain energy produced at specific frequencies. Key to the approach is a closed-loop, biofeedback technique based on analog electronics instead of the digital circuitry and open-loop approach used by most brain researchers. All eight were able in some degree to willfully raise or lower the intensity of a light and the volume of an audio tone using brain waves. The next step, beginning in about a month, is to demonstrate the same kind of brain control in a roll-axis flight simulator. □

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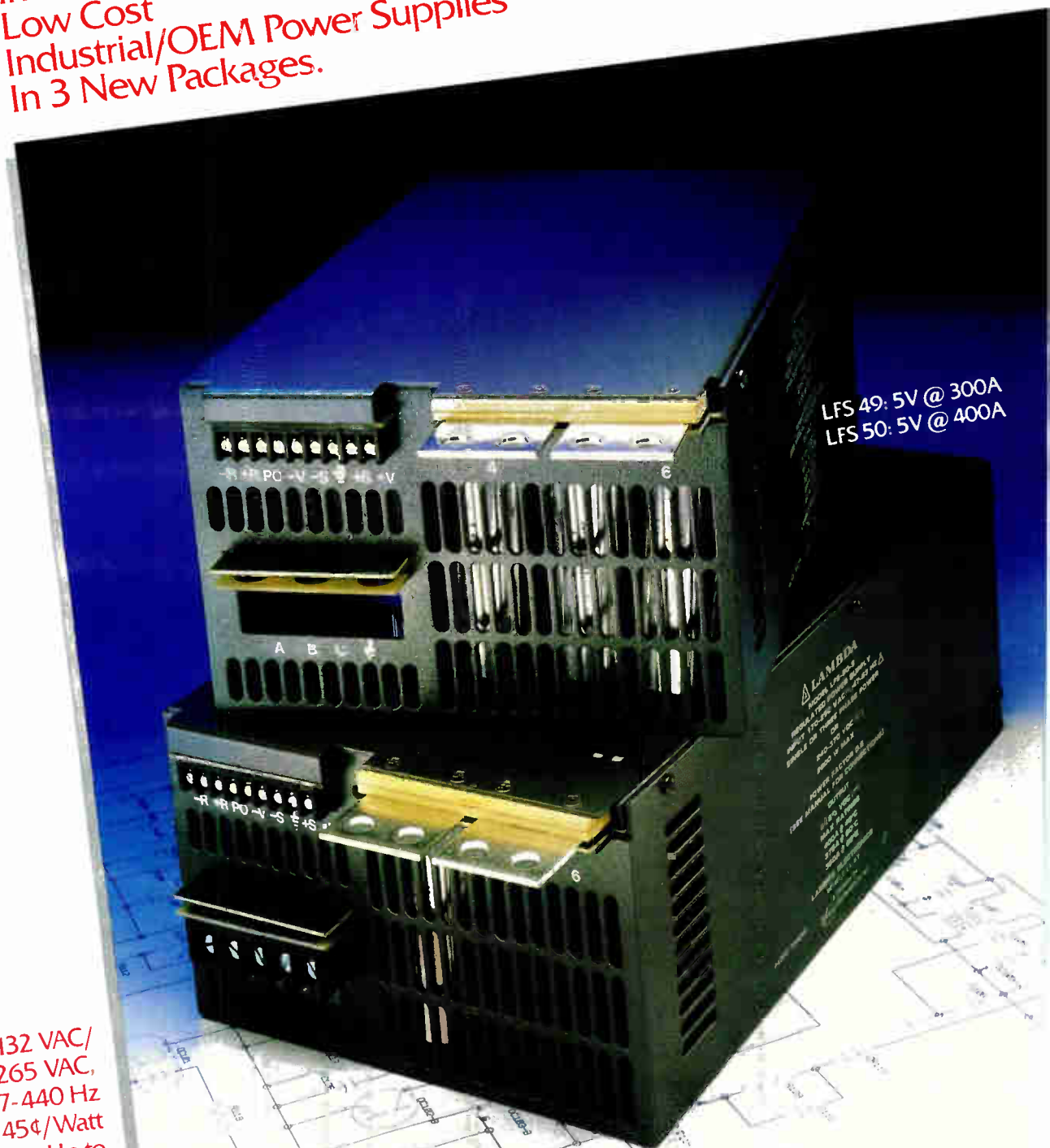

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	40.0	33.5	25.0	1.9 × 4.75 × 9.125	280	228	207	189	LFS-43-2
	60.0	45.0	33.5	1.9 × 4.75 × 11.75	360	297	270	252	LFS-44-2
	90.0	67.5	45.0	1.9 × 4.75 × 16	480	392	371	342	LFS-4S-2
	120.0	112.0	93.5	5 × 4.875 × 7.25	580	450	428	403	LFS-46-2
	150.0	142.5	120.0	5 × 4.875 × 8.875	680	560	478	450	LFS-47-2
	200.0	185.0	157.0	5 × 4.875 × 11	800	680	600	560	LFS-48-2
	335.0	318.0	291.0	4.875 × 7.375 × 11.50	1090	900	780	760	LFS-49-2
	400.0	375.0	350.0	4.875 × 7.375 × 12.875	1300	1100	940	920	LFS-50-2
5V ±5% ADJ.	25.0	21.8	17.5	1.9 × 4.75 × 5.687	235	170	155	140	LFS-42-S
	40.0	33.5	25.0	1.9 × 4.75 × 9.125	280	228	207	189	LFS-43-S
	60.0	45.0	33.5	1.9 × 4.75 × 11.75	360	297	270	252	LFS-44-S
	90.0	67.5	45.0	1.9 × 4.75 × 16	480	392	371	342	LFS-4S-S
	120.0	112.0	93.5	5 × 4.875 × 7.25	580	450	428	403	LFS-46-S
	150.0	142.5	120.0	5 × 4.875 × 8.875	680	560	478	450	LFS-47-S
	200.0	185.0	157.0	5 × 4.875 × 11	800	680	600	560	LFS-48-S
	300.0	285.0	261.0	4.875 × 7.375 × 11.50	1090	900	780	760	LFS-49-S
	400.0	375.0	350.0	4.875 × 7.375 × 12.875	1300	1100	940	920	LFS-50-S
6V ±5% ADJ.	21.0	18.3	14.5	1.9 × 4.75 × 5.687	235	170	155	140	LFS-42-6
	35.0	28.0	20.5	1.9 × 4.75 × 9.125	280	228	207	189	LFS-43-6
	50.0	37.5	28.0	1.9 × 4.75 × 11.75	360	297	270	252	LFS-44-6
	75.0	56.0	37.5	1.9 × 4.75 × 16	480	392	371	342	LFS-4S-6
	101.0	94.5	79.0	5 × 4.875 × 7.25	580	450	428	403	LFS-46-6
	126.0	120.0	107.0	5 × 4.875 × 8.875	680	560	478	450	LFS-47-6
	168.0	155.0	132.0	5 × 4.875 × 11	800	680	600	560	LFS-48-6
	260.0	244.0	224.0	4.875 × 7.375 × 11.50	1090	900	780	760	LFS-49-6
	345.0	325.0	300.0	4.875 × 7.375 × 12.875	1300	1100	940	920	LFS-50-6
12V ±5% ADJ.	10.5	9.5	8.0	1.9 × 4.75 × 5.687	235	170	155	140	LFS-42-12
	19.0	15.0	11.0	1.9 × 4.75 × 9.125	280	228	207	189	LFS-43-12
	26.0	18.5	13.5	1.9 × 4.75 × 11.75	360	297	270	252	LFS-44-12
	40.0	30.0	20.0	1.9 × 4.75 × 16	480	392	371	342	LFS-4S-12
	51.5	48.0	40.0	5 × 4.875 × 7.25	580	450	428	403	LFS-46-12
	64.5	61.5	55.0	5 × 4.875 × 8.875	680	560	478	450	LFS-47-12
	86.0	79.5	67.5	5 × 4.875 × 11	800	680	600	560	LFS-48-12
	145.0	138.0	126.0	4.875 × 7.375 × 11.50	1090	900	780	760	LFS-49-12
	190.0	180.0	170.0	4.875 × 7.375 × 12.875	1300	1100	940	920	LFS-50-12
15V ±5% ADJ.	8.5	7.5	6.3	1.9 × 4.75 × 5.687	235	170	155	140	LFS-42-1S
	15.5	12.0	9.0	1.9 × 4.75 × 9.125	280	228	207	189	LFS-43-1S
	21.0	15.5	11.5	1.9 × 4.75 × 11.75	360	297	270	252	LFS-44-1S
	32.5	24.5	16.0	1.9 × 4.75 × 16	480	392	371	342	LFS-4S-1S
	42.0	39.0	33.0	5 × 4.875 × 7.25	580	450	428	403	LFS-46-1S
	52.5	50.0	44.5	5 × 4.875 × 8.875	680	560	478	450	LFS-47-1S
	70.0	64.5	55.0	5 × 4.875 × 11	800	680	600	560	LFS-48-1S
	115.0	108.0	100.0	4.875 × 7.375 × 11.50	1090	900	780	760	LFS-49-1S
	153.0	143.0	133.0	4.875 × 7.375 × 12.875	1300	1100	940	920	LFS-50-1S
20V ± 5% ADJ.	6.7	6.1	5.1	1.9 × 4.75 × 5.687	235	170	155	140	LFS-42-20
	11.8	9.2	6.8	1.9 × 4.75 × 9.125	280	228	207	189	LFS-43-20
	16.0	11.5	8.5	1.9 × 4.75 × 11.75	360	297	270	252	LFS-44-20
	25.0	19.0	12.5	1.9 × 4.75 × 16	480	392	371	342	LFS-4S-20
	32.0	30.0	25.0	5 × 4.875 × 7.25	580	450	428	403	LFS-46-20
	40.0	38.0	34.0	5 × 4.875 × 8.875	680	560	478	450	LFS-47-20
	53.0	49.0	41.5	5 × 4.875 × 11	800	680	600	560	LFS-48-20
	85.0	80.0	72.0	4.875 × 7.375 × 11.50	1090	900	780	760	LFS-49-20
	111.0	104.0	97.0	4.875 × 7.375 × 12.875	1300	1100	940	920	LFS-50-20
24V ±5% ADJ.	5.7	5.1	4.3	1.9 × 4.75 × 5.687	235	170	155	140	LFS-42-24
	10.0	7.8	5.7	1.9 × 4.75 × 9.125	280	228	207	189	LFS-43-24
	13.0	10.0	7.5	1.9 × 4.75 × 11.75	360	297	270	252	LFS-44-24
	20.0	15.0	10.0	1.9 × 4.75 × 16	480	392	371	342	LFS-4S-24
	27.0	25.0	21.0	5 × 4.875 × 7.25	580	450	428	403	LFS-46-24
	33.5	32.0	28.5	5 × 4.875 × 8.875	680	560	478	450	LFS-47-24
	44.5	40.5	35.0	5 × 4.875 × 11	800	680	600	560	LFS-48-24
	72.0	68.0	63.0	4.875 × 7.375 × 11.50	1090	900	780	760	LFS-49-24
	97.0	90.0	84.0	4.875 × 7.375 × 12.75	1300	1100	940	920	LFS-50-24
28V ±5% ADJ.	5.0	4.4	3.7	1.9 × 4.75 × 5.687	235	170	155	140	LFS-42-28
	8.6	6.8	5.0	1.9 × 4.75 × 9.125	280	228	207	189	LFS-43-28
	11.5	8.5	6.3	1.9 × 4.75 × 11.75	360	297	270	252	LFS-44-28
	17.5	13.0	8.5	1.9 × 4.75 × 16	480	392	371	342	LFS-4S-28
	23.0	21.5	18.0	5 × 4.875 × 7.25	580	450	428	403	LFS-46-28
	29.0	27.5	24.5	5 × 4.875 × 8.875	680	560	478	450	LFS-47-28
	38.5	35.0	30.0	5 × 4.875 × 11	800	680	600	560	LFS-48-28
	64.0	61.0	56.0	4.875 × 7.375 × 11.50	1090	900	780	760	LFS-49-28
	86.0	80.0	75.0	4.875 × 7.375 × 12.875	1300	1100	940	920	LFS-50-28
48V ±5% ADJ.	2.8	2.6	2.1	1.9 × 4.75 × 5.687	235	170	155	140	LFS-42-48
	5.0	4.0	3.0	1.9 × 4.75 × 9.125	280	228	207	189	LFS-43-48
	6.5	5.0	3.8	1.9 × 4.75 × 11.75	360	297	270	252	LFS-44-48
	10.0	7.5	5.0	1.9 × 4.75 × 16	480	392	371	342	LFS-4S-48
	13.5	12.5	10.5	5 × 4.875 × 7.25	580	450	428	403	LFS-46-48
	17.0	16.0	14.5	5 × 4.875 × 8.875	680	560	478	450	LFS-47-48
	22.5	20.5	17.5	5 × 4.875 × 11	800	680	600	560	LFS-48-48
	37.0	34.0	31.0	4.875 × 7.375 × 11.50	1090	900	780	760	LFS-49-48
	48.0	45.0	42.0	4.875 × 7.375 × 12.875	1300	1100	940	920	LFS-50-48

LFS SERIES

Specifications

DC OUTPUT
Voltage range shown in tables.

REGULATED VOLTAGE

regulation, line	0.1% from 95 to 132VAC or 187 to 265VAC (85 to 132VAC or 170 to 265VAC on LFS-42. 170 to 265VAC or 3 phase on LFS-49 and LFS-50).
regulation, load	0.1% from 0 to full load.
ripple and noise	15mV RMS, 75mV pk-pk for 2V, 5V and 6V models. 20mV RMS, 150mV pk-pk for 12V through 28V models. 35mV RMS, 200mV pk-pk for 48V models.
temperature coefficient	0.03%/°C.
remote programming resistance	1000Ω/V nominal.
remote programming voltage	volt per volt.

AC INPUT
(User selectable.)

line	95 to 132VAC / 187 to 265VAC, 47-440Hz. 85 to 132VAC / 170 to 265VAC, 47-440Hz on LFS-42. 170 to 265VAC, 47-440Hz single phase or three phase on LFS-49 and LFS-50.
power	LFS-42: 186 watts maximum. LFS-43: 326 watts maximum. LFS-44: 440 watts maximum. LFS-45: 682 watts maximum. LFS-46: 882 watts maximum. LFS-47: 1103 watts maximum. LFS-48: 1470 watts maximum. LFS-49: 2457 watts maximum. LFS-50: 3220 watts maximum.
RMS current	3.7A RMS maximum on LFS-42. 5.7A RMS maximum on LFS-43. 7.5A RMS maximum on LFS-44. 12.0A RMS maximum on LFS-45. 15.0A RMS maximum on LFS-46. 18.0A RMS maximum on LFS-47. 25.0A RMS maximum on LFS-48. 22.0A RMS maximum (single phase); 16.0A RMS maximum (three phase) on LFS-49. 30.0A RMS maximum (single phase); 20.0A RMS maximum (three phase) on LFS-50.

EFFICIENCY
55% minimum on 2V models. 72% minimum on 5V through 15V models of LFS-42. 75% minimum on all other 5V through 15V models. 80% minimum on 20V through 48V models.

DC INPUT
260 to 370VDC. (Unit must be wired for 220V configuration on LFS-42 through 48.) 240 to 370VDC on LFS-49,50.

OVERSHOOT
No overshoot at turn-on, turn-off or power failure.

OPERATING TEMPERATURE RANGE
Continuous duty 0° to 60°C with suitable derating above 40°C. Guaranteed turn-on at −10°C with reduced specifications.

OVERLOAD PROTECTION
ELECTRICAL
External overload protection. Automatic electronic current limiting circuit limits the output current to a preset value, thereby providing protection for the load as well as the power supply.

HOLD UP TIME
2V, 5V and 6V models will remain within regulation limits for at least 16.7 msec. after loss of AC power when operating at full load, Vo max and 105VAC input at 60Hz. (When configured at 220V input: 20 msec holdup when operating at maximum output power and 210VAC input at 50Hz.)

IN-RUSH CURRENT LIMITING
All models are provided with in-rush current limiting to limit the current to a preset value.

OVERVOLTAGE PROTECTION
Non-crowbar, inverter shutdown type OV protection is standard on all models.

COOLING
LFS-42, 43, 44, 45 are convection cooled. LFS-46, 47, 48, 49, 50 are fan cooled.

DC OUTPUT CONTROLS
Simple screwdriver adjustment over the entire voltage range.

INPUT AND OUTPUT CONNECTIONS
All input, sensing and remote on/off connections are made via PC board mounted terminal block. DC output connections are made via heavy duty bus bars. Ground connections are made via chassis stud.

MOUNTING
One mounting surface and one mounting position on LFS-42, 43, 44, 45. One mounting surface, multiple mounting positions on LFS-46, 47, 48, 49, 50.

REMOTE TURN-ON / TURN-OFF
TTL compatible signal enables remote turn-on/turn-off of the power supply. A voltage of 2.8V to 5.0V applied to remote on/off terminals will initiate turn-off. Open circuit or short circuit condition, or a zero to 2.8V signal will cause turn-on.

REMOTE SENSING
Provision is made for remote sensing to eliminate the effects of power output lead resistance on DC regulation.

ISOLATION RATING
3750V RMS input to output (8mm spacing). 1500V RMS input to ground. 500V RMS output to ground.

CURRENT SHARING
The LFS-49 and LFS-50 have internal circuitry that allows units operated in parallel to share load current. Effects of different supply ambient temperatures are compensated for. For example, the hottest unit will automatically supply less load current. A single additional connection must be run between the supplies. This connection is available on the terminal block.

PHYSICAL DATA

Package Model	Weight Lbs. Net	Weight Lbs. Ship	Size Inches
LFS-42	1.30	2.30	1.9 x 4.75 x 5.687
LFS-43	3.00	4.00	1.9 x 4.75 x 9.125
LFS-44	3.50	4.50	1.9 x 4.75 x 11.75
LFS-45	6.00	7.00	1.9 x 4.75 x 16
LFS-46	8.75	11.75	5 x 4.875 x 7.25
LFS-47	9.19	12.19	5 x 4.875 x 8.875
LFS-48	12.31	15.31	5 x 4.875 x 11
LFS-49	16.00	19.00	7.375 x 4.875 x 11.50
LFS-50	18.00	21.00	7.375 x 4.875 x 12.875

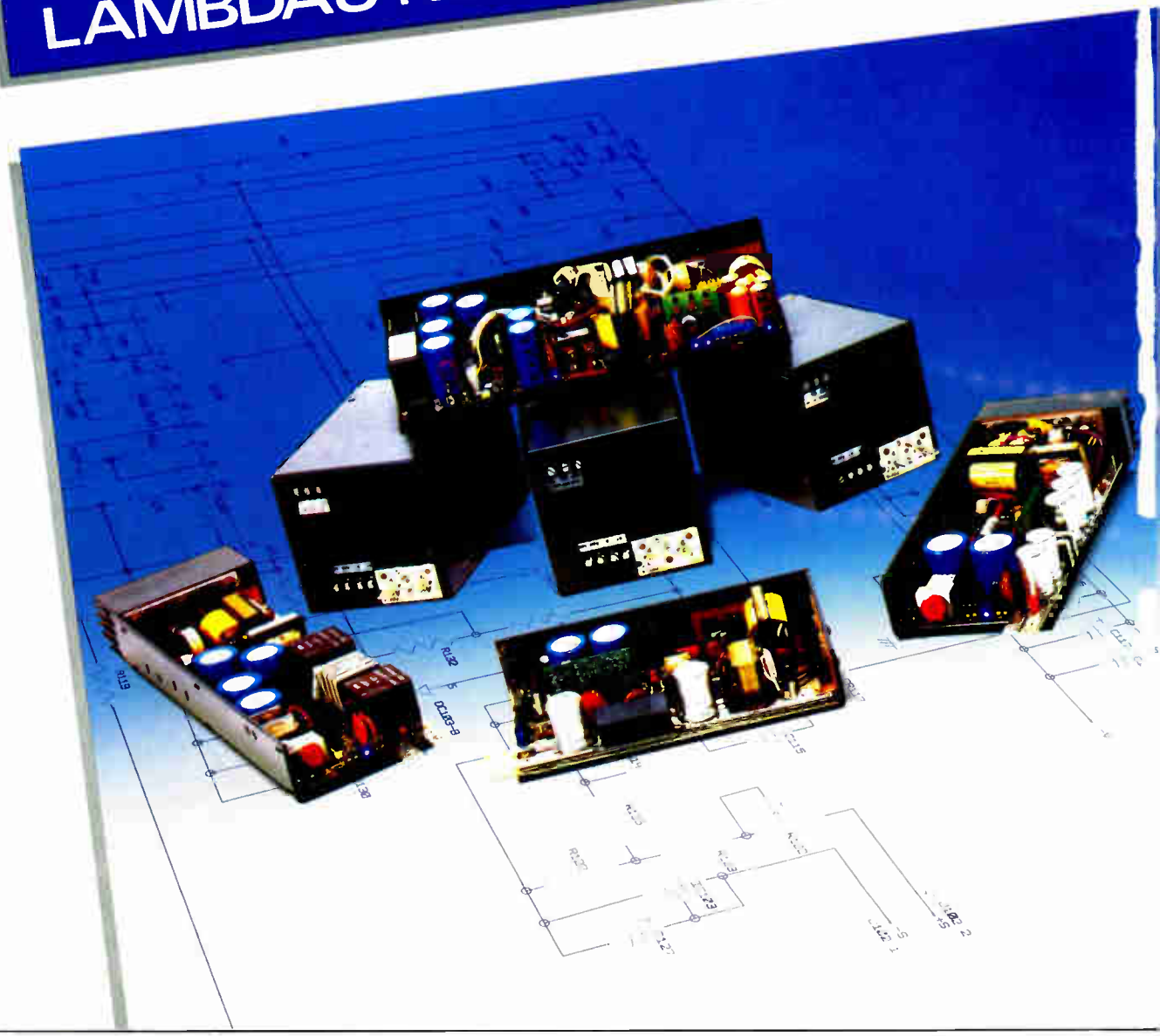
FINISH
Gray, Fed. Std. 595, No. 26081.

ACCESSORIES
LRA-17 and LRA-18 Rack Adapter available. LRA-15 Rack Adapter also available for LFS-42, 43, 46, 47, and 48 only. Cable system available on all models (consult factory).

GUARANTEED FOR 1 YEAR
One-year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of one year.

UL / CSA / TUV / IEC
All models are under evaluation. Most units have received formal agency approval or have passed all tests and are waiting for formal notification.

LAMBDA'S NEW LFS SERIES



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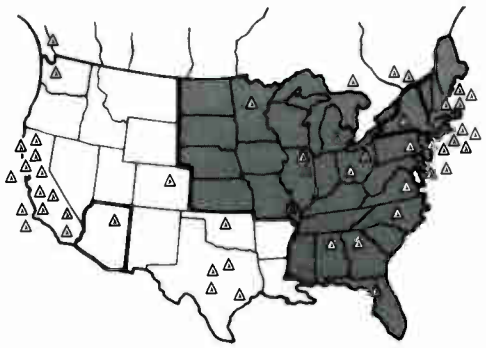

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2/88

NEW PRODUCTS

ADVANCED TOOLS TACKLE MORE COMPLEX CHIPS IN THE NEW GENERATION OF PLDs

Kits from Altera and Xilinx eliminate the need to learn new PLD methodologies

Designers grappling with the latest round of high-density programmable logic devices now have a handful of upgraded design tools to solve the learning-curve problems that are part and parcel of the new architectures.

At least two PLD vendors—Altera Corp. and Xilinx Inc.—are offering innovative tool-kit additions that eliminate the need to learn the methodologies involved in the current PLD architectures, which are radically different from the AND/OR structure of traditional PLD devices. The tools will make it easier to create PLDs with higher gate counts, better gate utilization, and significantly improved architectural flexibility.

TTL LIBRARY. Xilinx is offering two additions to its design system: a logic-synthesis package and a TTL library. These tools round out a software offering that already includes design entry, simulation, design implementation, and in-circuit emulation. The tool kit targets the San Jose, Calif., company's Logic Cell Array programmable gate arrays, which offer designers devices boasting the equivalent of 1,200 to 9,000 gates.

For its part, Altera, in Santa Clara, Calif., is introducing the MAX PLUS software to support its new multiple-array-matrix architecture (MAX). MAX PLUS incorporates a logic synthesizer as well as a hierarchical-schematic-capture mechanism that combines schematics with traditional Boolean-equation and state-machine entry mechanisms.

Using the new Xilinx tools, engineers currently implementing designs with traditional-logic integrated circuits can switch to the company's LCA architecture without learning a new design methodology. This means they can easily take advantage of the high-density Xilinx LCAs, including the 9,000-gate XC3090 (see p. 61), to replace printed-circuit boards filled with low-density TTL devices and PLDs.

Virtually all logic designers are familiar with TTL design and many have used PLDs, so the new logic-synthesis program combined with a TTL library gives them a simple migration route when higher-density logic is required to improve system speed, cost, or size. The new Xilinx TTL library for programmable gate arrays includes the most commonly used TTL medium-scale-integration functions and operates at the schematic level.

One complication in converting from TTL logic to programmable gate arrays is wasted resources: the designer frequently does not use all the functions of a TTL device. But the Xilinx design tools automatically delete the unused portions of the TTL macros so that no resources are wasted.

In addition to removing unused logic, the designer must also optimize the logic for the architecture in which it will finally be implemented. Here is where Xilinx's logic-synthesis program enters the picture. It is based on the Espresso program developed at the University of California at Berkeley, with the algorithms modified to optimize the results for Xilinx's LCA parts.

In logic synthesis—the automatic conversion and optimization of a design into a specific technology—the design may be specified in terms of another technology, or it may be specified in higher-level terms such as Boolean equations, state machines, or hardware-description languages. Logic-synthesis programs then take this design description and optimize it for a specific technology.

With the Xilinx approach, the designer can specify minimum logic resources or maximum performance as the primary goal for optimization. Although any logic network can be optimized with the design program, its primary use is for translating designs done using standard PLD techniques.

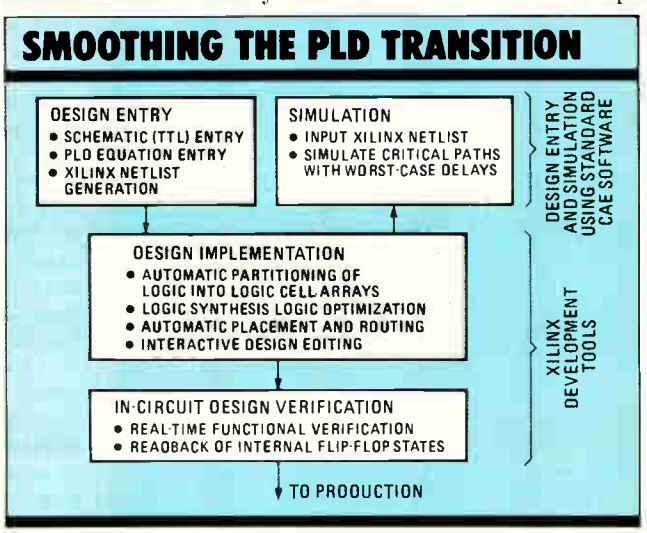
The Xilinx logic-synthesis program is now included as part of the company's $1,500 DS23 Automated Design Implementation system. The DS40 TTL library is also available now, for $500. It includes more than 40 common medium-scale-integration functions that supplement the company's standard XACT library of over 100 counters, decoders, multiplexers, and registers.

Altera's new multiple-array-matrix architecture also requires a new generation of PLD design software. The company's new devices offer the equivalent of up to 5,000 gates and more than 200,000 unique programmable elements.

IBM PC. The solution is MAX PLUS, a tool kit that runs on IBM Corp. Personal Computer ATs or compatibles. MAX PLUS provides a comprehensive front-to-back design methodology for the entire MAX family, including such features as hierarchical design entry, automatic logic minimization, and timing simulation, says David Laws, vice president of marketing. It also handles device fitting, a technique roughly analogous to place and route, he adds.

The package consists of a graphics-design editor, a design-processing engine, a timing simulator, and various programming software modules—all under the control of a supervisor task-control module.

Incorporating a graphics-oriented in-



By enhancing its PLD design tools with a TTL library and logic-synthesis software, Xilinx gives designers a direct migration path.

terface, MAX PLUS allows macrofunction entry using small- and medium-scale-integration-package symbols. "Instead of forcing him to learn a new software-entry methodology, this approach allows the designer to enter his design using his language," says Laws. But input using traditional state-machine entry is also accepted. Multiple menus provide access to various MAX design-processing and simulation subsystems. Errors discovered during design processing are reported as highlighted sections of the appropriate schematic, for easy debugging.

Whereas current PLD software requires the designer to enter and exit several programs, MAX PLUS is designed as an integrated environment under the control of the supervisor module, says Laws. This feature allows the designer to gain access to any phase of the design process without leaving the schematic stage. In addition, the supervisor automatically locates the source of design errors and if a design-rule violation is detected, a cursor points to the problem node. Once the error is corrected, the compilation process is restarted with a single keystroke, Laws says.

A mouse-driven schematic tool that allows for either a hierarchical top-down or bottom-up design approach, the graphics editor allows the designer to start a design with an overall device block diagram and then proceed to define each block individually. Alternatively, Laws says, the user can design and simulate small logic functions before building them up into a complete design.

HIERARCHICAL. Logic symbols available as a part of the package range from simple gate primitives to a complete 7400 TTL medium- and small-scale-integration-series library. Another advantage of the hierarchical approach is that it allows the use of state-machine descriptions, truth tables, or Boolean equations interchangeably for various portions of an overall design, Laws notes.

The design-processing engine consists of a netlist executor, logic synthesizer, fitter, and assembler. These functions reduce the design input to the minimum logical format, matching it to the logic resources of the target device and creating an appropriate programming file. This process is roughly equivalent to a place-and-route routine in a gate array, except that it is executed in minutes, rather than hours, he says.

Timing delays within the circuit can be determined with a timing predictor that is linked to the graphics editor. The designer locates the "probe-contact points" by moving the cursor on the schematic, and the timing predictor displays the worst-case delay between the two points.

Altera's new tools are designed to run

on either 6-MHz PC-ATs or PS/2 model 50s or compatibles with at least 2 Mbytes of internal random-access memory. They also require version 3.1 or higher of the PC-DOS or MS-DOS operating systems. Scheduled to be available when the MAX family is sampled, MAX PLUS will be offered in two packages; it can be purchased as a software-only version called PLS-MAX or as a complete development system that includes programming hardware and device samples. This version will be marketed under the name PLDS-MAX.

– *Tom Manuel and Bernard C. Cole.*

Xilinx Inc., 2069 Hamilton Ave., San Jose, Calif. 95125.
Phone (408) 559-7778 [Circle 380]

Altera Corp., 3525 Monroe St., Santa Clara, Calif. 95051.
Phone (408) 984-2800 [Circle 381]

SOFTWARE USES AI TO DEBUG PC BOARDS

The Diagnostic Expert System from Array Analysis Inc. cuts weeks off the time needed to debug populated printed-circuit boards by eliminating the need to write test programs.

Using artificial intelligence techniques, the DES software can learn to recognize fault conditions in analog and digital signals. It runs on IBM Corp. Personal Computer XTs, ATs or compatibles and requires Array Analysis's MFI-1000 logic analyzer.

The software has two operating modes. A fault directory can be created either by simulating failure conditions or by learning faults as they occur.

Other features include the ability to store analog and digital test vectors, reference data, and tolerance guidebands in a graphics format, so that language-specified timing is not required.

For more advanced testing, macro control sequences can be created by executing a test sequence manually and storing the result on disk. The software is available now for $1,985.

Array Analysis Inc., 200 Langmuir Lab, Brown Road, Ithaca, NY 14850.
Phone (800) 451-8514 [Circle 385]

MENTOR ADDS 80960 SIMULATION TO TOOL KIT

Mentor Graphics Corp. has added the industry's first simulation model for Intel Corp.'s 80960 microprocessor to its Graphics Hardware Modeling Library.

The addition provides designers with an opportunity to start work on 80960-based systems almost immediately upon the chip's release. The 80960 is a high-performance, embedded 32-bit microprocessor that features an on-board floating-point unit, interrupt controller, and read-only memory.

Mentor's HML system lets designers use the actual 80960 during QuickSim logic and QuickFault fault simulations. The fully functional 80960 model consists of software that enables the simulator, running on a work station, to communicate with the physical chip inserted into the HML.

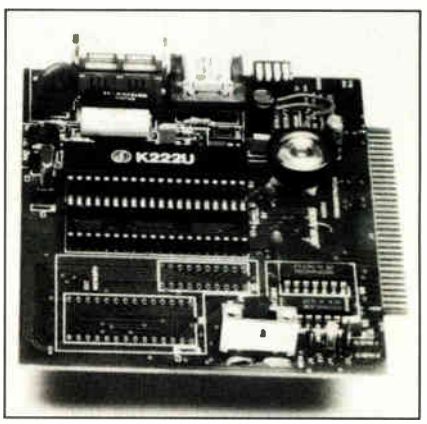
The HML is available now and costs $44,800. The 80960 HML model is priced at $2,000.

Mentor Graphics Corp., 8500 S.W. Creekside Place, Beaverton, Ore. 97005.
Phone (503) 626-1231 [Circle 388]

DESIGN KIT HANDLES ONE-CHIP MODEMS

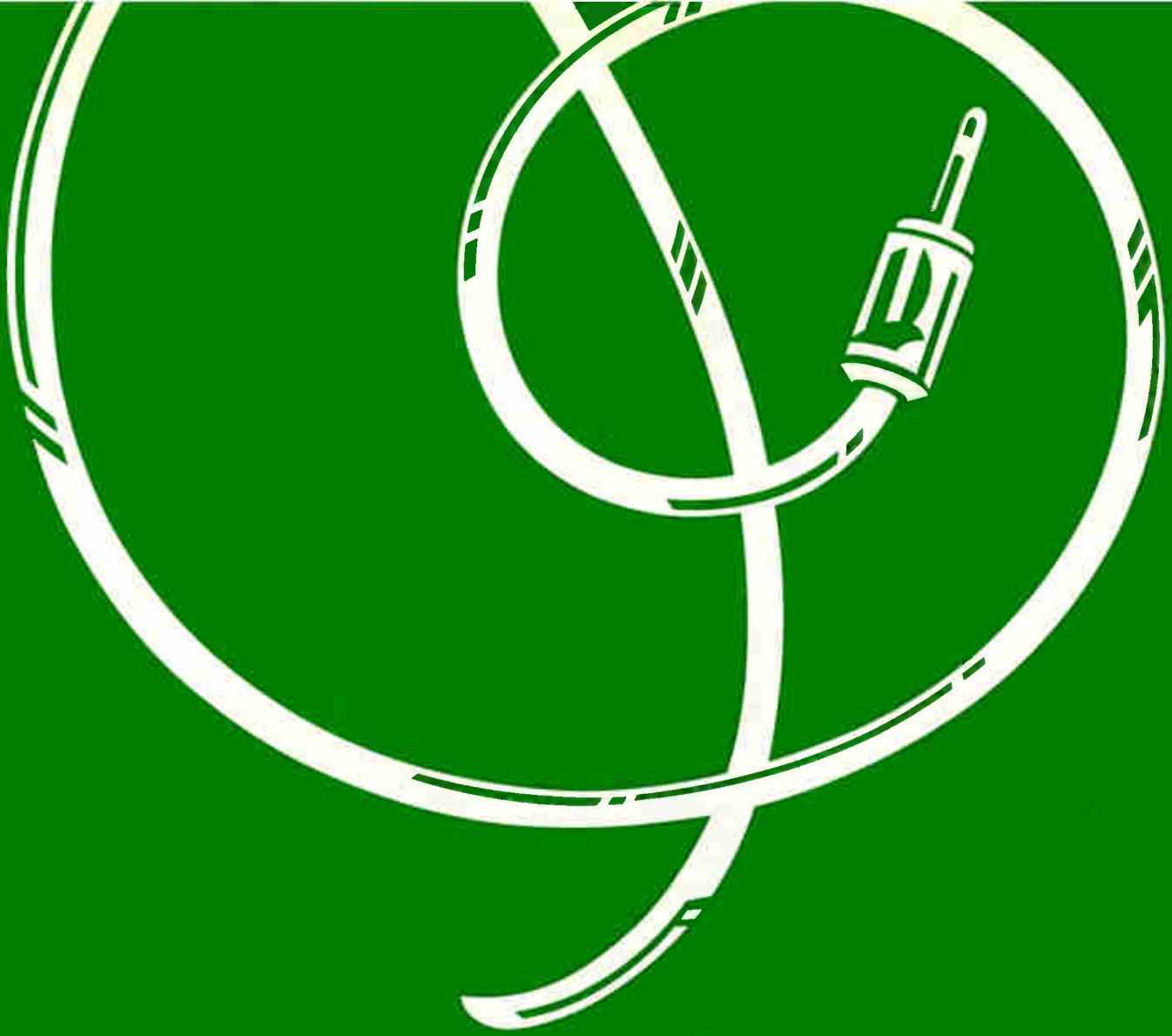
A design evaluation kit from Silicon Systems Inc. supports the company's K-series of single-chip modem products with integral universal asynchronous receiver/transmitter functions.

The K22U Design Evaluation Kit handles beginning-to-end modem design. Running on an IBM Corp. Personal Computer AT or compatible, it can significantly shorten development time by serving as a prototyping tool—thereby eliminating the need to breadboard a complete circuit before debugging it.



It comes with the basic board, a K222U chip, a user/design manual, and diskette-based software. The complete package is available now. Pricing starts at $199.

Silicon Systems Inc., 14351 Myford Road, Tustin, Calif. 92680.
Phone (213) 540-2426 [Circle 387]



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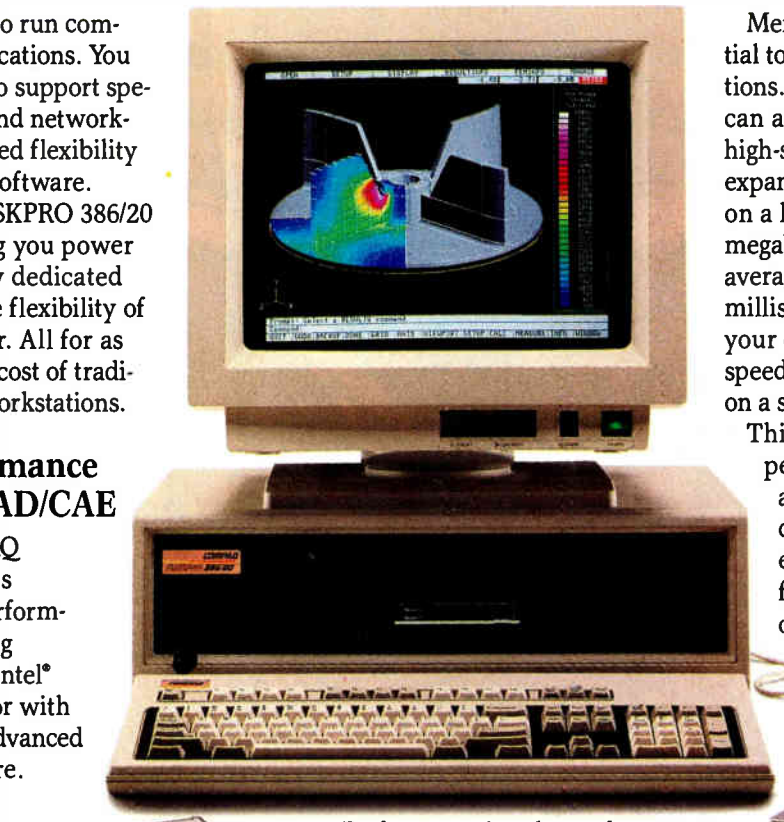

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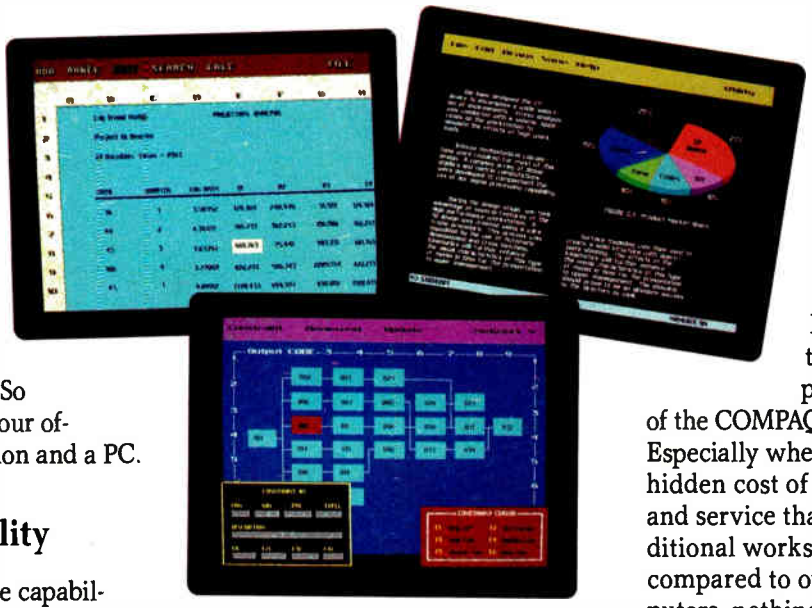
with operating systems such as UNIX®, XENIX®, MS-DOS® or MS• OS/2. This provides the multitasking capability to run design applications simultaneously with your project management and documentation, database, spreadsheet and other productivity applications. So you don't have to clutter your office with both a workstation and a PC.



Compaq gives you the flexibility to run the world's largest library of productivity software.

Built-in compatibility

Compaq also gives you the capability to build a CAD/CAE system designed specifically for your needs. That's because the COMPAQ DESKPRO 386/20 is compatible with a wide variety of industry-standard peripherals. Graphics boards to work with your choice of super high-resolution monitors. Digitizing tablets, mice and pens. Printers and plotters. It can also be connected to dedicated workstations or other PC's by using Ethernet, Token Ring or other high-speed networks.

The low cost of high performance

No other workstation offers the price/performance advantage of the COMPAQ DESKPRO 386/20. Especially when you factor in the hidden cost of training, support and service that go along with traditional workstations. And when compared to other personal computers, nothing comes close to its total system performance.

A custom-built solution

An Authorized COMPAQ Computer Dealer can custom-configure a CAD/CAE solution built around the COMPAQ DESKPRO 386/20. For the location of your nearest dealer, call 1-800-231-0900, Operator 53. In Canada, 1-800-263-5868, Operator 53.

Performance Comparisons

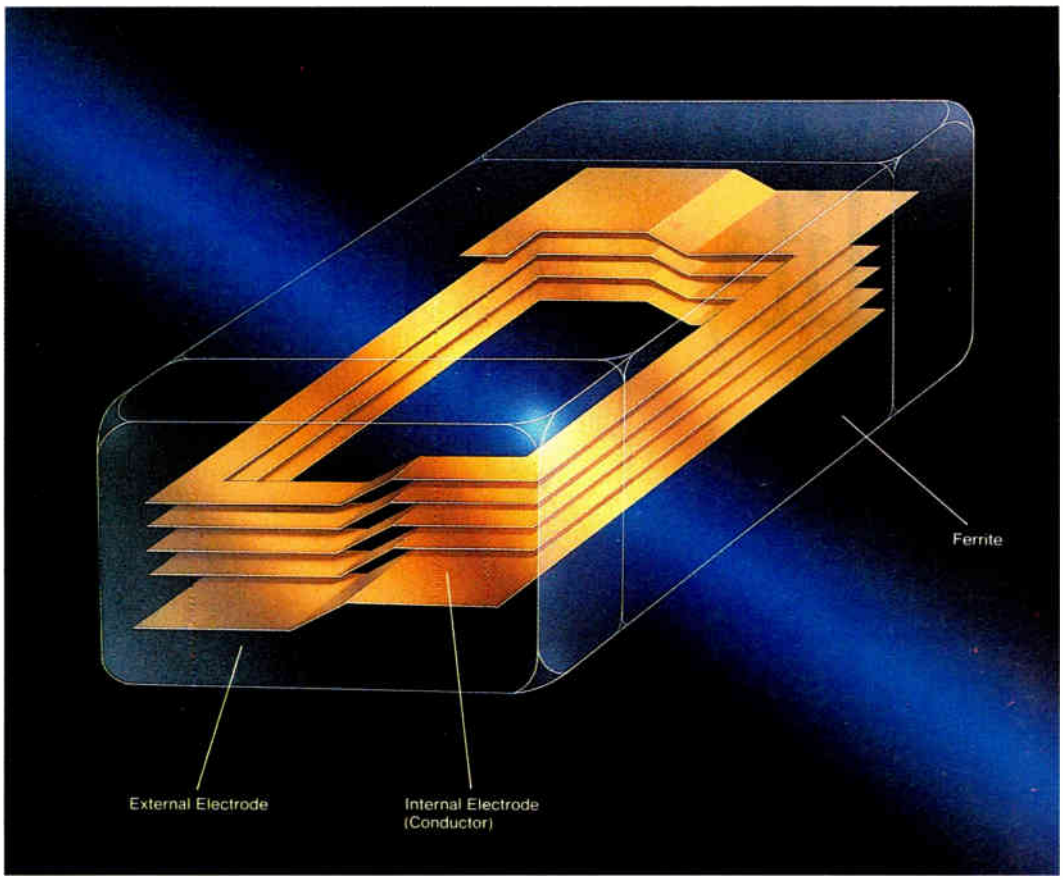
Performance Benchmark	COMPAQ DESKPRO 386/20*	IBM PS/2™ Model 80-111†	SUN® 3/260*	APOLLO® DN 4000*
Dhrystones/sec.	7800	5514	7142	6250
MWhetstones/sec.	4.6	1.8	3.4	3.8
Linpack (KFLOPS)	900	630	865	800

*Using Weitek Coprocessor †Using 80387 Coprocessor

The COMPAQ DESKPRO 386/20 is faster on standard performance benchmarks than comparable workstations.

COMPAQ

It simply works better.



TDK Multilayer and Integration Technology Stands at the Leading Edge with TDK Multilayer Chip Inductors.

For the first time ever, inductors can be made without actual winding. Consider TDK Multilayer Chip Inductors. Thanks to TDK, they eliminate the problems of high density circuit boards.

Multilayer surface mount devices from TDK include ceramic chip capacitor networks, chip band pass filters and chip LC traps that require both designs and manufacturing technology of a sophisticated nature. Furthermore, TDK is making significant progress toward "super multilayer" and high circuits integration.

TDK technology ranges from raw materials to finished multilayer chip components to automatic mounting equipment, namely, our Avimount series. We strive to meet the requirements of the industry for high quality, high performance chip components. And we're striving to achieve total surface mount technology from start to finish.

When it comes to SMT, come to TDK.

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TDK Surface Mount Devices

Multilayer Ceramic Chip Capacitor
C1608 (CC0603)
C: 0.5~22,000pF
C2012 (CC0805)
C: 0.5~100,000pF
C3216 (CC1206)
C: 0.5~220,000pF
C3225 (CC1210)
C: 750~470,000pF
C4532 (CC1812)
C: 2,400pF~1μF
C5650 (CC2220)
C: 5,100pF~1.5μF

Multilayer Chip Capacitor Network
MCN7575
TC: CH, 1~100pF (10 capacitors)
SL, 10~1,000pF (10 capacitors)
Class II, 100~470,000pF (10 capacitors)

Multilayer Ceramic Chip Capacitor (High Frequency, Low Loss)
FC1414
C: 0.5~3,300pF
FC2828
C: 0.5~22,000pF
FR1414
C: 0.5~3,300pF
FR2828
C: 0.5~22,000pF

Multilayer Chip Inductor
MLF3216
L: 0.047~33μH
MLF3225
L: 39~220μH

Multilayer Chip LC Trap
MXT4532
F: fo ±2%

Multilayer Chip IFT
MIA4532
F: 455, 459, 464kHz
MIF4532
F: 10.7MHz

Multilayer Chip Transformer
MTT4532
L: 10~200μH

Multilayer Chip LC Filter
MXF4532H
HPF (Tuner)
MXF4532B
BPF (FM radio)
MXB5050B
BPF (VCR)
MXB5050L
LPF (VCR)
MXB5050D
Delay Line (VCR)
A variety of characteristics are available. Please specify when ordering.

Leadless Inductor (Wound Chip Inductor)
NL322522
L: 0.01~220μH
NL453232
L: 1.0~1,000μH
NL565050
L: 1,200~10,000μH
NLF453232
L: 1.0~1,000μH
(Shielded Inductor)

Leadless LC Trap (Wound Chip LC Trap)
NLT4532
F: 630kHz~13MHz
Tolerance: ±2%
Attenuation: 20dB min.

Leadless EMI Filter (Wound Chip EMI Filter)
NLL4532
C: 33pF~100,000pF
L: 1μH~220μH

Ferrite Chip Bead
CB201209
Zo: 7, 10, 11Ω
CB321611
Zo: 19, 26, 31Ω
CB322513
Zo: 31, 52, 60Ω
CB453215
Zo: 70, 120, 125Ω

NTC Chip Thermistor
NTC CS3216
R typical: 1.0~150kΩ at 25°C
Temp. Range: −25 to +85°C

SM Active Delay Line
FDL
Delay time: 20~75 nsec.

SM Transformer/ Inductor
EE5
ER9.5
ER11
T2
A variety of characteristics are available. Please specify when ordering.

SM Step-up Inductor (Piezoelectric Buzzer)
OL3.3 x 1.6
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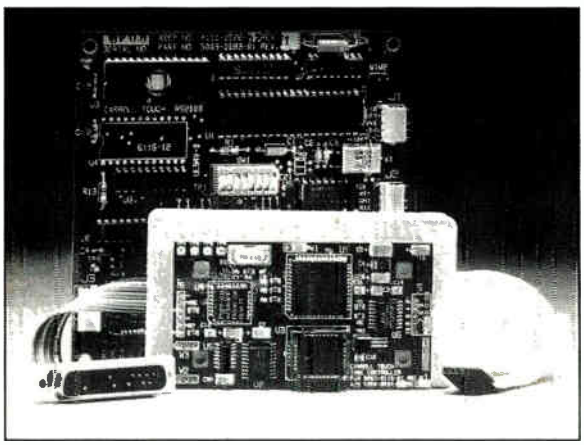
Circle 118 on reader service card

TOUCH-SCREEN CONTROLLER CUTS PART COUNT 75% BY USING CUSTOM IC

Carroll Touch's analog part teams with microcontroller for enhanced functions

By integrating a custom CMOS analog controller chip into its touch-screen technology, Carroll Touch Inc. has cut the resistive-overlay system's control-electronics parts count by 75% and shrunk the controller board itself from the previous generation's 4 by 6 in. down to just 2 by 4 in.

The full-custom analog chip was jointly developed over 18 months by the Round Rock, Texas, company and NCR Microelectronics Division, Fort Collins, Colo. Working in tandem with a digital support chip, the analog chip handles a variety of enhanced control functions, including automatically storing and maintaining touch-screen parameters such as display size. Since the new board reduces parts count, it also saves energy, cutting power requirements by about 250 mW, according to Wayne Wehrer, Carroll Touch's research and development manager.



Carroll Touch's new controller lets users recalibrate their touch screen to compensate for drifting images on the monitor.

Building on the advances derived from a higher level of integration, Carroll Touch also enhanced its manufacturing techniques to trim the cost of sensors used in the system, says John Chenault, vice president and general manager for Carroll Touch's Commercial Systems Division.

PRICE BREAK. The 1302 series resistive overlay for a 13-in. monitor, for example, sells for about 70% of the competition's price when purchased in 1,000-piece quantities.

The analog chip replaces about a dozen parts and provides touch-sensor control and measurement as well as touch detection. Fabricated in 3-μm CMOS, it integrates a bandgap reference, 8-bit analog-to-digital converter, two circuit-calibration digital-to-analog converters, and a screen driver.

The companion CMOS digital part—Motorola Inc.'s high-end 8-bit 68HC11 microcontroller—stores calibration values and system parameters in electrically erasable programmable read-only memory. Other firmware stores filtering algorithms to lock in touch points. This procedure solves a nagging problem of the technology, caused by the tendency of images on the monitor to drift over time. Recalibrating the touch screen to counteract the monitor's drift can be accomplished by simply touching four different positions on the screen. The same digital filtering technique also has the added advantage of reducing overall circuit noise.

But as far as users are concerned, says Chenault, the raft of technology improvements really adds up to making the adjustment of the system much easier. The new system's software-based alignment feature—implemented by the digital filtering techniques—allows users to align the screen by touching the target area of the screen and using software commands to set the command inputs. This is easier to do than the traditional mechanical method of alignment. Software for the resistive-overlay product is compatible with Carroll Touch's universal software interface for its line of touch-screen products, called Smart Frame.

Users can also define their own resolution. The controller can simulate any touch coordinate range up to 256-by-256 touch points, bringing the resolution to 65,536 touch points.

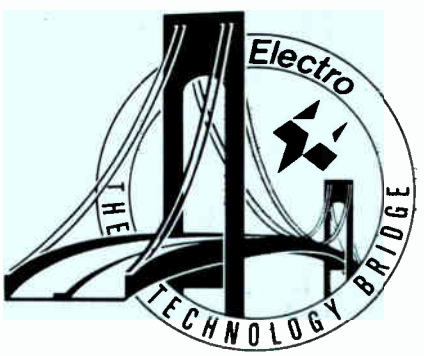
With the steady reduction of touch-screen system prices, the applications for such products are increasing, according to Chenault. Now, the leading applications for touch screens are medical systems, industrial process control, retail information systems, instrumentation, and personal computers used as intelligent controllers—using touch in place of a keyboard for commands.

Because the touch-screen parameters are software-controlled, the controller communication interface with the host computer takes on more importance. Carroll Touch engineers have opted to use an RS-232-C serial communication line. The commands from the digital-support chip initialize the touch system, select touch operating modes, request special messages, and manage the transfer of touch data.

9,600 BAUD. Touch reports from the controller and the host are transferred at a rate of 9,600 bits/s, which translates into a response time of 25 ms. The reports can be either coordinates—*x-y* pairs for processing by applications programs—or control information. These control reports requested by the host generally address capabilities such as error reporting, firmware versions, operational settings, and resolution levels.

The touch screen will be shown at Electro and is available now. The price for a touch screen sized to fit 13-in. monitors is $264 in quantities of 1,000. The 19-in. product costs $352, and the 9-in. product costs $202. – *Jack Shandle*

Carroll Touch Inc., Division of AMP, P.O. Box 1309, Round Rock, Texas 78680. Phone (512) 244-3500 [Circle 400]



The 45,000 registrants and 900 exhibitors expected at the Electro/88 show in Boston's World Trade Center and Bayside Exposition Center May 10 through 12 will find one of the most comprehensive displays of industrial electronics held in the East. This special section provides an advance look at some products that will be exhibited—from the latest touch-screen technology to semiconductors.

EPSON'S LCD PANEL CAN COMPETE ON PRICE WITH CRT

By using flexible-circuit-board technology to reduce manufacturing costs, Epson America Inc. has cut the price of its liquid-crystal displays to $142 each in quantity—10% under its previous models. The advance brings LCD technology into the realm of being a cost-effective alternative to cathode-ray tubes.

The 6-in. diagonal EG7500B uses super-twisted, nematic, liquid-crystal technology in a chip-on-flex design to offer a 10 : 1 contrast ratio and a pixel format of 320 by 200 dots. It is 40 characters wide by 25 lines deep.

The key in reducing both the size and weight of the display is an innovative chip-on-flexible board packaging approach that eliminates an entire printed-circuit board required on previous LCDs. Doing away with the pc board, which typically contains numerous surface-mounted devices, also lowers manufacturing costs, says Jack Confrey, director of sales and marketing for Epson's Torrance, Calif., original-equipment-manufacturer division.

ECONOMICAL. "This new display provides design and system engineers with a practical alternative to using CRTs," he says. Not only has the price—quoted for quantities of 100—been reduced, but the new technology also delivers enhanced reliability and lower service and ownership costs for the customer.

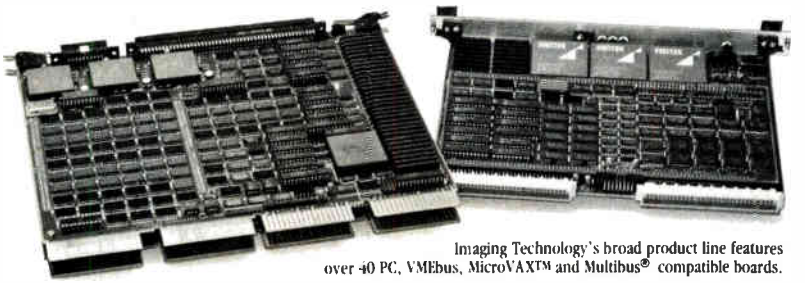
The EG7500B has a life expectancy of 50,000 hrs., compared with less than 20,000 hrs. for an average CRT phosphor, the company says. It has a modular, white flourescent backlight for readability in low-light conditions.

While the new LCD is intended for all display equipment, the low power requirement and compact size make it particularly suitable for portable gear used on manufacturing floors and in many instrumentation applications, Confrey says. Its 40-character/line format is compatible with the industry standard.

Total power consumption of the Epson display is 100 mW, maximum. Supply voltage for logic is 5 V, typical, and supply current 8 mA, maximum. For the display, a supply voltage of –14 V to –23 V is required, and a supply current of 6 mA, maximum. The display is 6.45 in. long by 5.63 in. wide by 0.98 in. deep. It weighs 16.08 oz.

To drive the LCDs, the EG7500B uses CMOS large-scale integrated circuits that were designed specifically for this task. It employs a 4-bit parallel data transfer and works with all the major

VMEbus and MicroVAX imaging subsystems from Imaging Technology. Advanced vision for advanced architectures.



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controller devices from a number of vendors. The 320-by-200 dot-matrix format is supported by commonly available graphics software, allowing display of alphanumerics as well as special characters, graphics, charts, and patterns, the company says. – *Larry Waller*

Epson America, Inc., OEM Division, 3415 Kashiwa St., Torrance, Calif. 90505.
Phone (213) 534-4500 [Circle 401]

SWITCHED-POWER SUPPLY HANDLES FIVE OUTPUTS

Deltron Inc.'s CV series of closed-frame, switched-power supplies ranges in output from 360 to 600 W, handles up to five outputs, and features a dual-loop architecture for better regulation of auxiliary outputs.

The switchers also offer the ability to trim-adjust not only the main output but the first and second auxiliary outputs as well. Specifications for the series include 80% typical efficiency, remote sensing, overload protection, ac underwattage, and reverse voltage protection.

Multiple output models provide high-peak-current capabilities for disk drives. The CV series of switchers is available now. Prices begin at $312 each for single output models in 100-unit purchases. Multiple-output unit pricing begins at $376 each in 100-unit purchases.

Deltron Inc., P. O. Box 1369, Wissahickon Ave., North Wales, Pa. 19454.
Phone (215) 699-9261 [Circle 405]

SONY'S ECL FAMILY RUNS UP TO 4 GHz

A high-speed family of emitter-coupled-logic devices from Sony Corp. of America's Components Division achieves speeds of up to 4 GHz, yet maintains power consumption under 1 W.

The ECL Logic Family gets its power to speed performance from Sony's proprietary ECL 3 Process—a 1-μm technology with a transition frequency of 10 GHz and gate delays of 80 ps at 300 μA.

First products in include the CXB1100Q quad three-input OR/NOR device with a speed of 1.5 GHz; the CXB1104Q dual D flipflop that runs at 3.2 GHz; the CXB1110Q 16-to-1 multiplexer that runs at 1.5 GHz; and the CXB1138Q four-bit arithmetic logic unit. The first group of products includes a total of 24 devices.

Available now in 24-lead flat packs, the devices run on a single –4.5 V power supply and offer ECL-100K output compatibility. Prices range from $40 to $150 each depending on device and quantity purchased.

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NEC

LOGIC DEVICES' 16-BIT ALU DELIVERS 60% SPEED BOOST

CMOS chip executes math or logic operations in as little as 20 ns and replaces up to 20 fast TTL devices in pipelined DSP applications

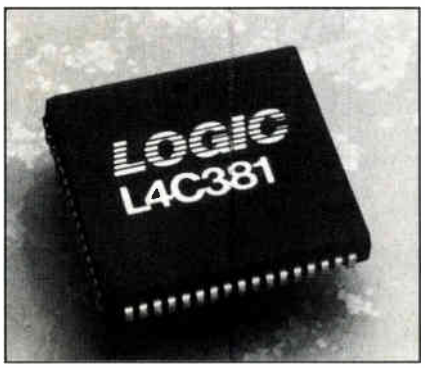
Designers of digital-signal-processor circuits with pipelined architectures can get up to a 60% speed boost in math operations—compared with competitive TTL solutions—with Logic Devices Inc.'s 16-bit CMOS arithmetic logic chip.

The L4C381 takes just 20 ns to perform any of five arithmetic or five logic operations on its dual 16-bit inputs when operating in its fast registered-add mode. In its flow-through mode, the chip takes 26 ns for the same operations, says the Sunnyvale, Calif., company.

MONOLITHIC. The chip's speed advantage over competing solutions is derived largely from its advanced level of integration. The L4C381 delivers the same functionality as up to 20 TTL chips in the 74Fxxx series developed by Fairchild Semiconductor Corp. and currently being supplied by Texas Instruments Inc. and National Semiconductor Corp.

The L4C381's dual-input architecture contributes to speed and versatility, as well. Using conventional solutions, designs of many image processing applications, for example, are forced to implement two pipelines to attain the required operating speed, says Joel Dedrick, director of development.

The L4C381 can achieve the same throughput with a single pipeline because each of its two 16-bit inputs has its own data register. This allows two data values to be loaded simultaneously from a 32-bit bus or one data value at a time to be loaded from a 16-bit bus.



The L4C381 gets its speed from two 16-bit inputs, each with its own data register.

Similarly, a register is implemented on the L4C381's output, which permits it to recycle output data back to an input. This feedback loop between output and input—also known as an accumulation path—is not usually implemented in a single chip. It is important to have in digital-signal-processing applications, however, because DSP results are often derived from successive approximations through iteration. In most other solutions, designing in an accumulation path requires the addition of another chip.

To enhance flexibility, Logic Devices' design team engineered the chip to bypass either of the dual registers when the circuit design did not require them. This architectural innovation means designers can, for example, position the chip at the beginning, middle, or end of their overall DSP-pipeline circuit without sacrificing functionality.

Among the 10 functions that can be implemented using the L4C381 are subtract, accumulate, negate, and twos complement. The 68-pin device includes output pins that allow full arithmetic logic unit status checks, including carry, carry-look-ahead, and overflow.

The chip maintains full performance and functional compatibility with solutions utilizing the 74Fxxx or Texas Instruments' 74Sxxx chips, but its 1.5-μm CMOS implementation results in significant power savings: more than 650 mA for a bipolar, multiple-device solution compared with 15 mA for the L4C381.

Available now in 68-pin plastic leaded-chip-carrier packages, and 68-pin ceramic pin-grid arrays, the L4C381 comes in three speed grades: 26 ns, 40 ns, and 55 ns. The plastic part is rated for the commercial temperature range of 0°C to +70°C, while the ceramic part is rated for −55°C to +125°C.

In the plastic package, the 26-ns part costs $24 each in purchases of 1,000; the 40-ns part costs $22 each; and the 55-ns part, $20 each. Pricing for the ceramic pin-grid-array-packaged parts is: $34 for the 26-ns part, $32 for the 40-ns part, and $30 for the 55-ns part. A military version that complies with the requirements of MIL-STD-883C Class B will be available in July. – *Jack Shandle*

Logic Devices Inc., 628 E. Evelyn Ave., Sunnyvale, Calif. 94086.
Phone (408) 720-8630 [Circle 360]

NCR OFFERS 1.5-MICRON MIXED-MODE CELLS

A family of 1.5-μm CMOS analog cells from NCR Corp. allows designers of application-specific integrated circuits for the first time to combine analog functions with high-speed digital cells, supercells, and core microprocessors available in NCR's 1.5-μm VS1500 CMOS digital standard cell library.

Other ASIC vendors offer analog cells typically at 2- and 3-μm geometries, but NCR's Microelectronics Division in Fort Collins, Colo., is the first to offer mixed-mode (analog and digital) standard-cell-chip capability at the 1.5-μm level, says Patrick L. Ham, manager of circuit design. The new cells are functionally equivalent to the family of 2-μm analog cells NCR introduced last month, and provide smooth migration for ASIC customers.

The 1.5-μm analog family consists of an operational amplifier, a comparator, a bandgap-voltage reference, two analog switches, an emitter-coupled-logic input interface, matched-resistor building blocks, and analog input and output pads. It will be available in July.

"Smaller geometries are not necessarily better for analog, but the idea is to just make them available, so that people migrating to 1.5 μm for valid digital reasons don't have to give up analog capability," Ham says. For certain types of circuit designs the finer lined analog cells will pay performance dividends, he adds. A digital-to-analog converter designed with the 1.5 μm comparator level might run 20% to 30% faster than NCR's 2-μm VS2000 family design.

Unlike other vendors of mixed-mode standard cells, NCR provides separate operational specifications for the analog cells across each of four temperature ranges: 0° to 70° C; −40° to +85°C; −40° to +125°C; and −55° to +125°C.

NCR expects the analog cells will be particularly useful in circuits in automotive and industrial environments. And thanks to the inherent low power advantages of CMOS, mixed-mode VS1500 chips will also serve well in commercial battery-powered gear and other low voltage applications, the company says. The analog cells are specified for use in single source 5-V applications, but the op amp, comparator, and switch cells will operate with supplies as low as 2.7 V, Ham says. Power consumption on the analog cells can be further reduced with a "power down" mode that can be triggered by a digital-logic-level input.

Both the 1.5-μm comparator and op amp cells are designed for general pur-

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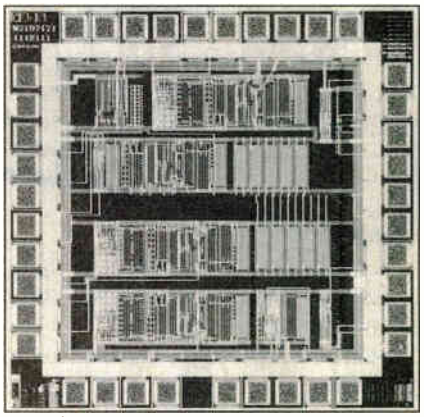
pose use, featuring low-input offset voltage at less than 5 mV typical. The comparator uses positive feedback for fast, 90-ns response time, while the op amp cell features typical gain bandwidth at 2.8 MHz. The input interface cell supports standard ECL 10K-switch points, meaning that NCR's mixed-mode CMOS semicustom devices can be driven directly with standard 10K ECL-logic circuitry. The two analog switch cells offer a choice, with on resistance specified at either 350 Ω or 3,500 Ω, to meet varying circuit needs.



Low power consumption will help VS1500-based chips do well in battery-powered gear.

The analog cells are compatible with NCR's current ASIC design tools. For circuit level simulation, NCR currently relies on Precise, a package from Electrical Engineering Software Inc., Santa Clara, Calif.

Kit parts in 40-pin dual in line packages housing typical 1.5-μm analog cell configurations will be available in July for breadboarding and evaluation. Nonrecurring engineering costs for designs containing both cell types begin at $49,500. – *Wesley R. Iversen*

NCR Microelectronics Division, 2001 Danfield Court, Fort Collins, Colo. 80525. Phone (800) 334-5454 [Circle 362]

GRAPHICS CHIP IS KEY TO SMALLER CONTROLLER CARDS

Graphics controller boards can be designed with up to an eight-fold area reduction compared with existing solutions by using Hitachi America Ltd.'s highly integrated HD63487 graphic support chip. But the mini-board, which is the size of a business card, still delivers high-end performance for slimmed-down personal computers, hand-held instruments, and point-of-sale terminals.

The HD63487 integrates all the circuitry needed to control graphics memo-

ry, move images on a cathode-ray-tube screen at a 33 million pixels/s, and implement display functions such as horizontal scrolling and zooming, says H. Kim Wheeler, product marketing engineer for the San Jose, Calif., company.

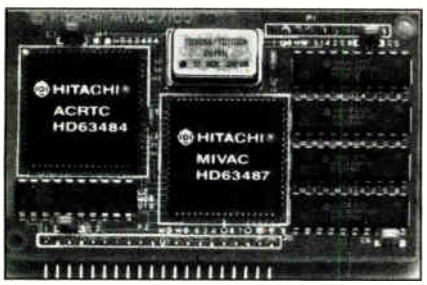
Competing boards offering the same functionality generally fit into a half-size slot on an IBM Corp. Personal Computer and measure about 12 by 5 in.

Hitachi's engineers were able to pack onto a single chip both the complex, high-density logic circuitry and the high-drive circuits needed to interface directly with dynamic random-access memories by utilizing its proprietary HiBiCMOS process. The CMOS process provides high density; the bipolar handles the drive currents.

MIVAC. All that is needed to build a high-end graphics controller card around the HD63487—also known as the Memory Interface and Video Attribute Controller, or Mivac—is Hitachi's HD63484 Advanced CRT Controller (ACRTC) chip, four 1-Mbit DRAMs, a clock crystal, and a programmable logic device to implement the bus interface, says Wheeler.

The controller card's small size is particularly important to equipment designers working on add-on boards to IBM Corp.'s Personal System/2 products, which have boards one-third smaller than its PC line.

Key parameters on the chip can be changed to configure the controller board for a wide range of applications. Adjustable parameters include resolution, number of colors, pixel-shift rate, and frame-buffer size.



Hitachi's Mivac chip helps shrink graphics controller boards to business-card size.

An example of programming the chip, Wheeler says, would be to provide 640-by-400-pixel resolution along with 16 colors and a 2-Mbyte frame buffer.

Packaged in a 68-pin surface-mount plastic-leaded chip carrier, the HD63487 will be available in the third quarter. Pricing will be $25 each in 5,000 piece quantities. The HD63484 ACRTC chip also costs $25 in volume purchases. It is available in both plastic-leaded chip carrier packaging and 64-pin plastic dual in-line packages. – *Jack Shandle*

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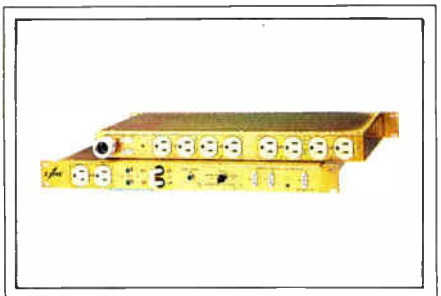

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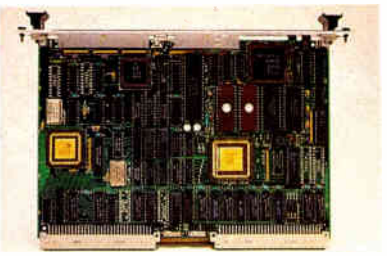

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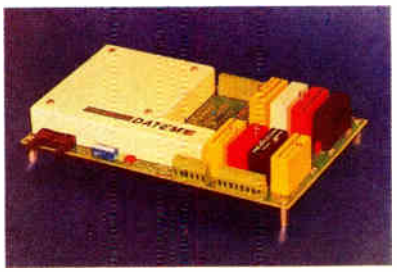

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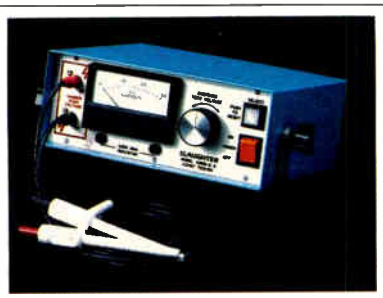

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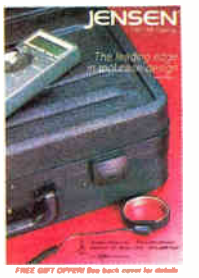

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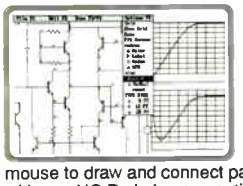

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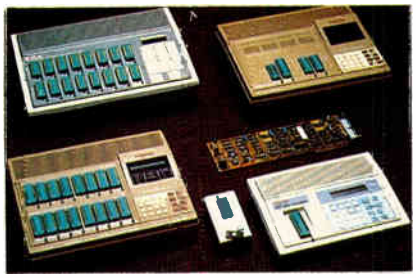

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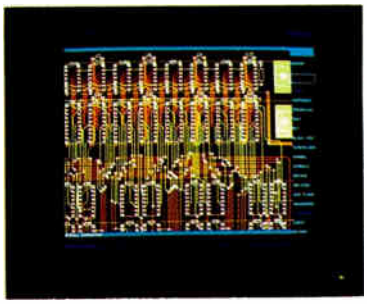

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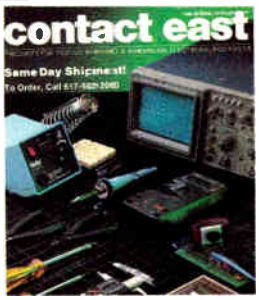

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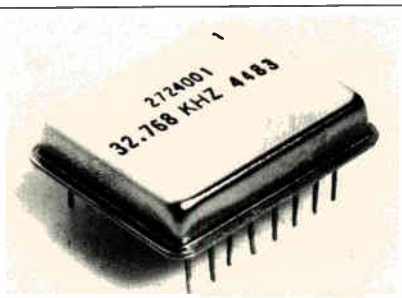

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ELECTRONICS WEEK

SEMATECH DELAYS CLEAN ROOM PLANS

Sematech, the consortium of 14 U.S. semiconductor makers, will delay completion of its first clean room from August to November to reap longer-term research benefits. The change will ultimately allow Sematech to perform more advanced Phase 2 research activities in the Phase 1 facility now under construction in Austin, Texas. The enhanced clean room will have a lower particulate count, Sematech says, as well as better vibration, temperature, and humidity control. These are not the first delays for Sematech, which has been unable to fill its top management posts—positions that should have been filled by January.

SANDIA: THIN-FILM SUPERCONDUCTORS

Researchers at Sandia National Laboratories in New Mexico have produced thin films of a thallium-based material that they say becomes superconducting at 97 K—the highest transition temperature yet recorded for thin-film superconductors. The films can carry high current densities of 110 A/cm^2 when cooled to 77 K in liquid nitrogen, a key factor if they are ever to be used in electronic applications.

BNR IC COMBINES LASER AND MESFETs

BNR, the research subsidiary of Canada's Northern Telecom, says its scientists have produced the world's most advanced monolithic optoelectronic transmitter. The technology combines an aluminum gallium arsenide laser with digital GaAs MESFET circuitry on a single integrated circuit, and even includes two built-in light-reflecting mirrors. The resulting IC converts electronic signals to light at a 2-gigabit/s rate. Integrating the two technologies would drive down the cost of fiber-optic networking and give the technology a huge boost, BNR says.

MODEM SALES GROW BUT PRICES WILL FALL

Modem sales will grow almost 50% in the U.S. between now and 1992, but declining prices will keep revenue down, say forecasters at Frost & Sullivan Inc., a New York market research firm. Unit sales in six categories of modems will jump from 2.6 million in 1987 to almost 4.7 million in 1992, although falling prices—at an annual average rate of 20%—will keep income growth low. Sales in dollars will peak at $1.3 billion in 1989, Frost & Sullivan reports, up from $1.1 billion last year, but are expected to fall below the $1 billion level in 1992.

SALES AND SHIPMENTS OF COMPUTERS RISE

Orders and shipments of U.S.-made computer and business equipment are both up better than 20% so far in 1988, says the Computer and Business Equipment Manufacturers Association in Washington. Shipments rose 20% in February, from $3.9 billion in 1987 to $4.7 billion this year, as orders were up 19% from $4.4 billion last year to $5.3 billion in February 1988. For January and February combined, sales were up from almost 6.4 billion to about $8.5 billion and orders up from about $6.5 billion to about $9.2 billion.

AT&T UNVEILS ISDN INTERFACE CHIPS

AT&T Microelectronics has announced a new primary rate interface chip set that offers designers of Integrated Services Digital Networks a vertically integrated solution for multiplexing voice and/or data over the same high speed transmission lines. The Berkeley Heights, N.J., company says the chip set meets both T1 (U.S.) and Cept (European) transmission standards. Included in the set is a 16-channel adaptive differential pulse code modulation transcoder, which can compress 64 Kbits of voice information into a 32-Kbit packet, thus doubling transmission capacity.

A TOUGH WEEK FOR CULLINET SOFTWARE

Cullinet Software Inc., the Westwood, Mass., company that's struggling to find growth outside its traditional niche—mainframe data-base software—had a tough first week of May. Three vice presidents resigned, the company laid off 400 workers, and it announced the sale of two divisions—all in the wake of nine months worth of losses totalling $26.5 million. The moves came a month after founder John Cullinane returned from retirement as chairman and chief executive officer to replace David Chapman, who had come to Cullinet from Data General Corp. in 1986. Cullinane and George Tamke, the new president and chief operating officer, will attempt to return the company to profitability.

GOULD BAILS OUT OF FACTORY AUTOMATION

Faced with slipping market share and a changing competitive environment, Gould Inc. is getting out of the factory-automation business it helped to pioneer. As part of a continuing restructuring, the Rolling Meadows, Ill., firm said at the beginning of May that it is selling its Industrial Automation Systems Group to AEG AG of Frankfurt, West Germany, for about $290 million. The group accounted for about 20% of Gould's $933 million in 1987 revenues, but was unprofitable last year due to restructuring costs and weak industrial capital spending.

WANG DEVELOPS ITS OWN LAN

Piggybacking on IEEE 802.3 (Ethernet) and 802.5 (Token Ring) networking standards, Wang Laboratories Inc. has developed its own personal computer local-area network. Wang's PC LAN includes hardware and software that links Wang with IBM Corp. PCs and compatibles in networks that include other LANs, Wang VS minicomputers, and mainframes, says the Lowell, Mass., company. Hardware includes network servers that support Banyan Systems Inc.'s Vines network operating system.

DATA GENERAL WILL CLOSE CHIP FACTORY

Data General Corp. says it will close its Sunnyvale, Calif., semiconductor pilot fabrication plant in December. In the meantime, however, the plant's 150 workers will continue to stockpile devices used in many of the Westboro, Mass., computer manufacturer's systems. The company says the shutdown is part of a cost-reduction program begun last year, but will not affect either the Sunnyvale design team or the Westboro designers now developing an emitter-coupled-logic version of Motorola Inc.'s 88000 reduced-instruction-set-computer microprocessor [*Electronics*, April 28, 1988, p. 32].

CALMA SELLS IC CAD BUSINESS TO VALID

General Electric Co. subsidiary Calma Co. announced in late April that it was selling its integrated-circuit computer-aided-design business to competitor Valid Logic Systems of San Jose, Calif. Calma's IC CAD business had sales of $40 million in 1987 and an installed base of 2,700 users, a good match for Valid, which had revenues of $67 million in 1987 and a 4,500-user installed base.

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4 19 34 49	64 79 94 109	124 139 154 169	184 199 214 229	244 259 274 351	366 381 396 411	426 441 456 471	486 501 706 900
5 20 35 50	65 80 95 110	125 140 155 170	185 200 215 230	245 260 275 352	367 382 397 412	427 442 457 472	487 502 707 901
6 21 36 51	66 81 96 111	126 141 156 171	186 201 216 231	246 261 338 353	368 383 398 413	428 443 458 473	488 503 708 902
7 22 37 52	67 82 97 112	127 142 157 172	187 202 217 232	247 262 339 354	369 384 399 414	429 444 459 474	489 504 709 951
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14 29 44 59	74 89 104 119	134 149 164 179	194 209 224 239	254 269 346 361	376 391 406 421	436 451 466 481	496 701 716 959
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SPECIFICATIONS

MODEL	FREQ. MHz	GAIN, dB 100 MHz	1000 MHz	2000 MHz	Min. (note)	•MAX. PWR. dBm	NF dB	PRICE $ Ea.	Qty.
MAR-1	DC-1000	18.5	15.5	—	13.0	0	5.0	0.99	(100)
MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8□	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

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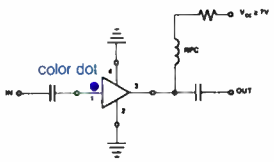

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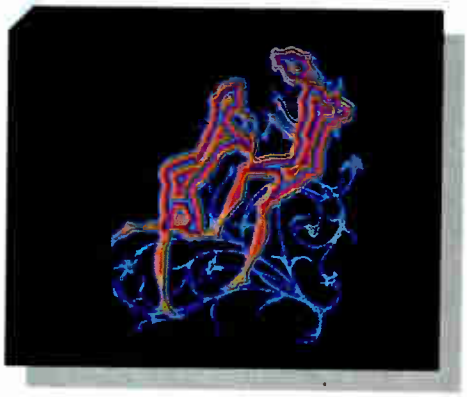

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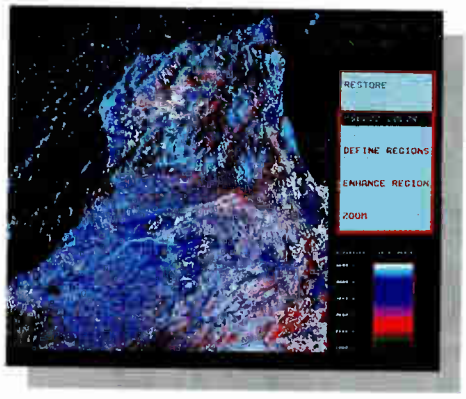

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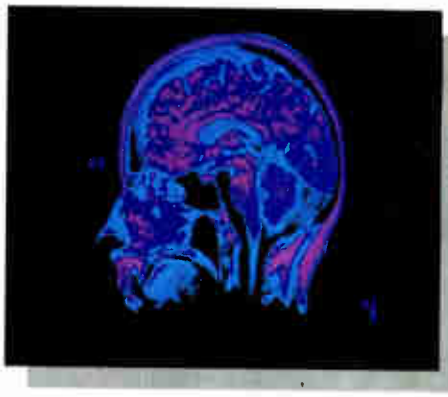

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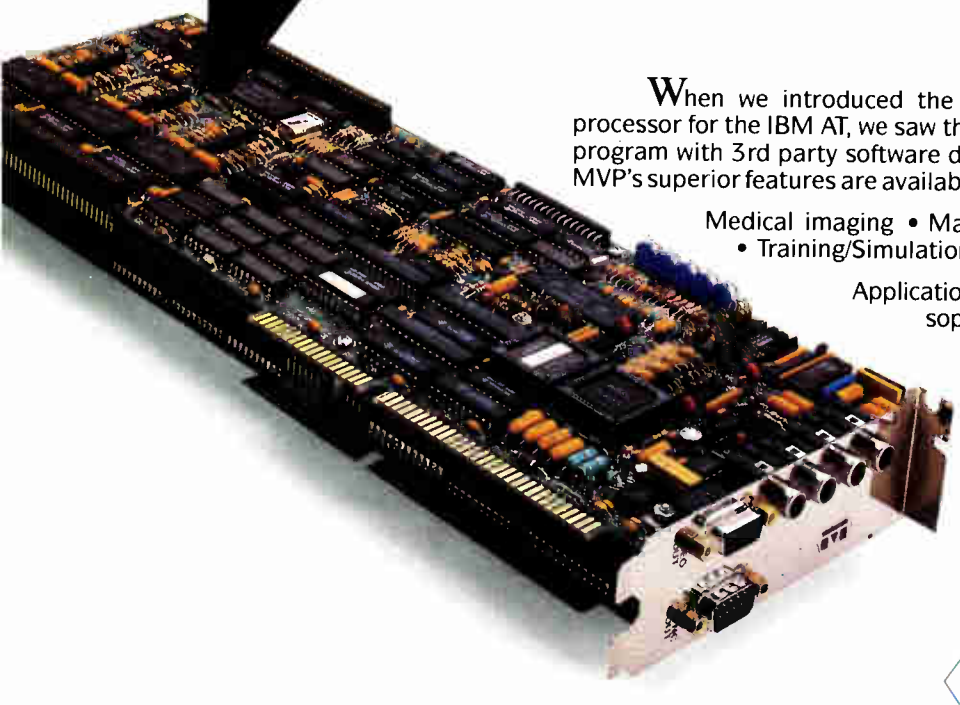

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