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NOVEMBER 12, 1987 A McGRAW-HILL PUBLICATION SIX DOLLARS

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FIXING THE BIGGEST PROBLEM IN GATE ARRAYS

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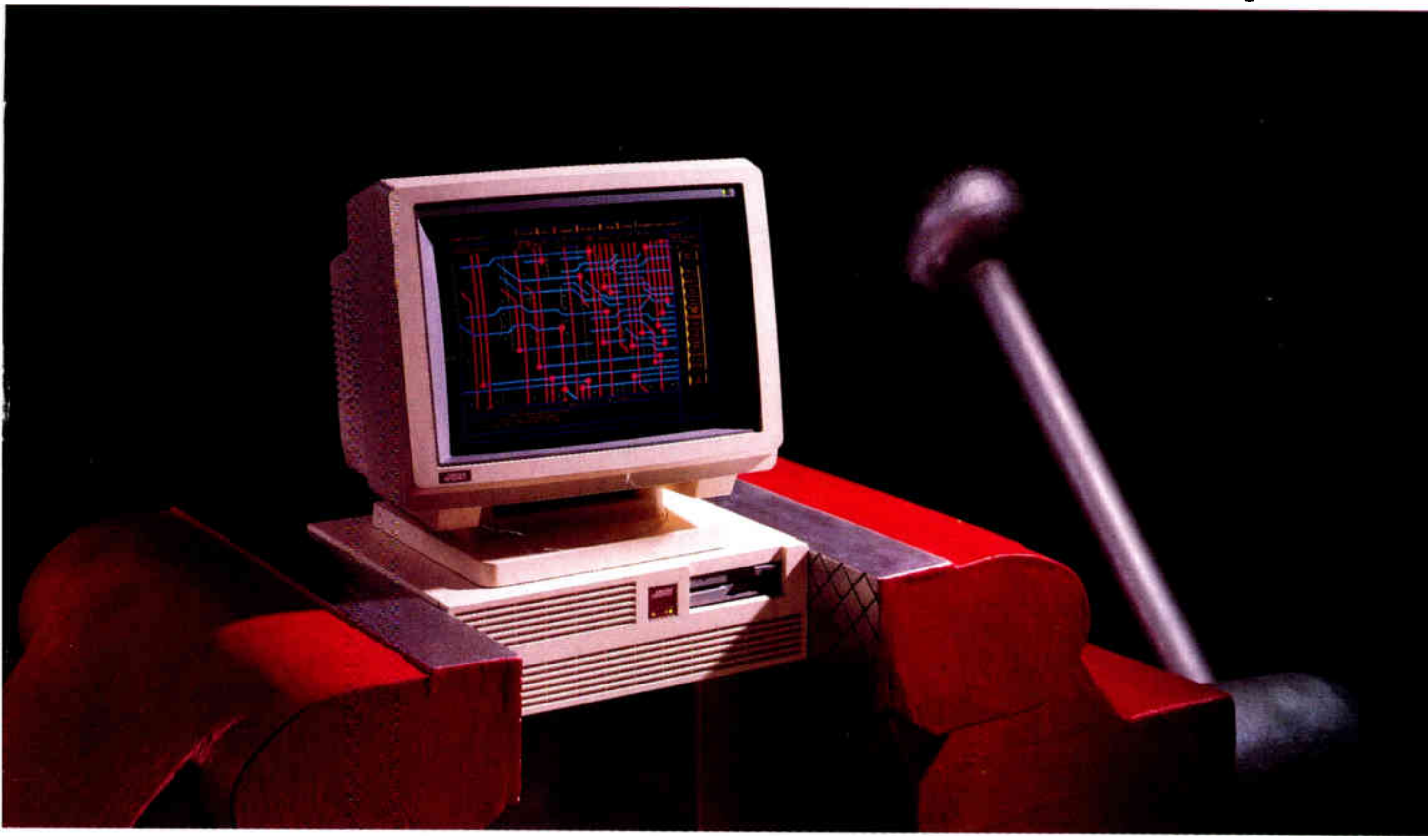
Only Mentor Graphics stands up to the pressures on PCB layout.



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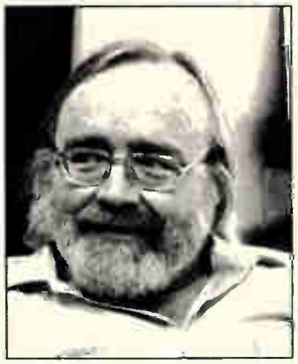
In our technology stories, we steer away from the term "revolutionary" because so few electronic developments really are, and also because the word has been abused by overuse elsewhere. But the package of articles featured on the cover of this issue is the exception: if the developments it describes aren't truly revolutionary, then they're certainly the closest thing that we've seen in many a moon.



COLE: Witness at a revolution in the semicustom business.

We're talking about laser-based systems that make possible fast-turnaround prototypes of semicustom chips. Though those systems are just starting out—they can do up to 6,000 gates—it is not inconceivable that someday they will evolve into production tools. Bernard Cole, who wrote the four articles, is convinced that they will engender some major changes.

"These systems are going to revolutionize the business in three ways," Bernie says. "First, they will eliminate disagreements between the vendor and the customer. Second, they are going to open new vistas to distributors. And third, they will make it possible to literally start an integrated-circuits business in your garage.

"The vendor-customer disagreements occur now," says Bernard, our San Mateo-based semiconductor editor, "when a customer takes his specs to a semicustom house, gets the chip back in a few weeks—and finds that it doesn't work. Most often, the problem is that the device has been specified wrong—a 0 instead of a 1 has been slipped in somewhere.

"But with these new fast-turn systems, a chip can be made in hours and plugged in without test. Since the part zips out the door so fast, it becomes practical to use a trial-and-error method. If the chip doesn't work, the suspected defect may be in a particular quadrant. So the user just plugs in a part without that quadrant; if it works, then he knows where the problem lies. It's simple: no test, no fuss, and no weeks of going back and forth until the defect is pinpointed."

The second part of the revolution in the semicustom business will be the effect of the new equipment on distributors. "They have been programming logic parts for a while," says Bernie, "but with the new systems they will actually be able to help turn out prototypes—for an additional charge."

But perhaps the most fascinating wrinkle is that the latest in high technology could be instrumental in encouraging a return to the old days, when an entrepreneur could start a business on a comparative shoestring. "The new systems will enable someone, with a relatively small investment, to build working prototypes and show them, rather than just designs, to prospective system customers," says Bernard.

And he points out that the price of the machines, as low as $500,000 in one case, will certainly make it easier for an embryo operation to raise venture capital. "It would be easier to finance one of these laser systems than a $100 million fab line," he says.

The systems are going to create a good deal of excitement, and we're going to keep an eye on them.

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Electronics

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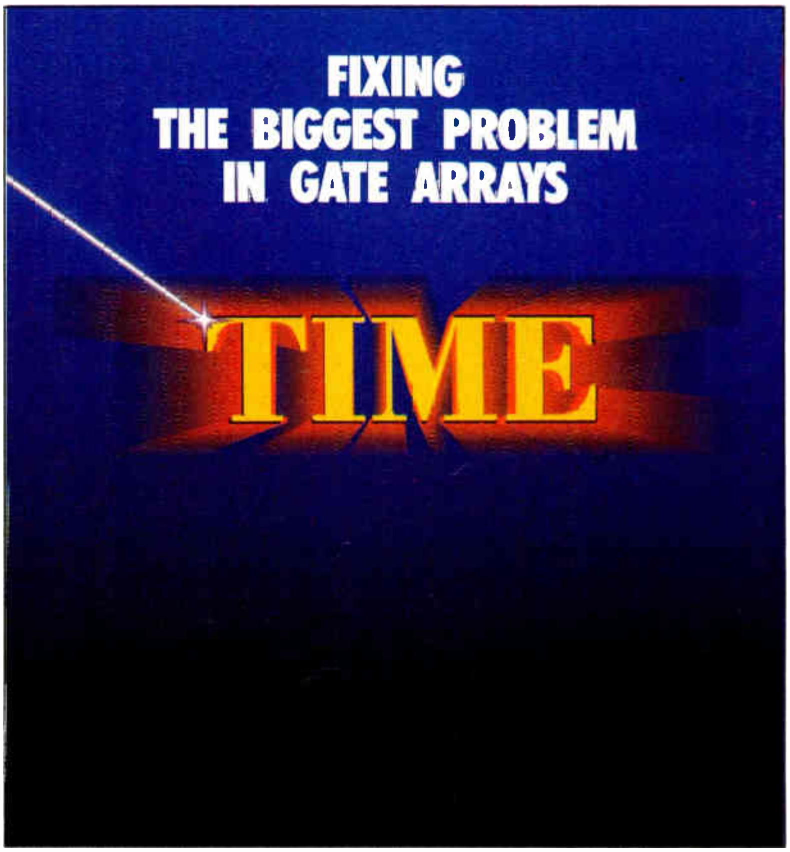
INSIDE TECHNOLOGY

PROBING THE NEWS

VOLUME 60, NO. 23

COVER: GRAPHIC MEDIA INC.



NEW PRODUCTS

DEPARTMENTS

from 99¢

dc to 2000 MHz amplifier series

SPECIFICATIONS

MODEL	FREQ. MHz	GAIN, dB 100 MHz	1000 MHz	2000 MHz	Min. (note)	• MAX. PWR. dBm	NF dB	PRICE $ Ea.	Qty.
MAR-1	DC-1000	18.5	15.5	—	13.0	0	5.0	0.99	(100)
MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8□	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

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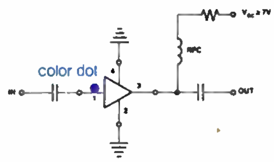

Unbelievable, until now...tiny monolithic wide-band amplifiers for as low as 99 cents. These rugged 0.085 in.diam.,plastic-packaged units are 50ohm* input/output impedance, unconditionally stable regardless of load*, and easily cascadable. Models in the MAR-series offer up to 33 dB gain, 0 to +11dBm output, noise figure as low as 2.8dB, and up to DC-2000MHz bandwidth.

*MAR-8, Input/Output Impedance is not 50ohms, see data sheet. Stable for source/load impedance VSWR less than 3:1

Also, for your design convenience, Mini-Circuits offers chip coupling capacitors at 12 cents each.†

Size (mils)	Tolerance	Temperature Characteristic	Value
80 × 50	5%	NPO	10, 22, 47, 68, 100, 470, 680, 100 pf
80 × 50	10%	X7R	2200, 4700, 6800, 10,000 pf
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† Minimum Order 50 per Value

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Pwr Dissipation mW/gate	35/32**	35	44/40**
Speed-Power Product-pJ	11.5/10.5**	35	42/30**
Edge Speed Tr, Tf-ns	0.5	1.0	0.7

* Flat/DIP package
**V_{EE}=-5.2V/-4.5V

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MC10/ MC100	Function	Features	Output Type	General Sampling
E111	1:9 Differential Clock Driver	Low Skew, Enable, Vbb	Diff.	Now
E142	9-Bit Shift Register, 500MHz	Async. Reset	SE	4Q 87
E155	6-Bit 2:1 Mux-Latch	Common Enable, Reset	SE	4Q 87
E143	9-Bit Hold Register, 500MHz	Async. Reset	SE	1Q 88
E336	3-Bit Registered Cutoff Bus XVCR	25 ohm Cut off Outputs	SE	1Q 88
E151	6-Bit D Register	Common CLK, Reset	Diff.	1Q 88
E167	6-Bit 2:1 Mux-Register	Common CLK, Reset	SE	1Q 88
E158	5-Bit 2:1 Multiplexer	Common Select	Diff.	1Q 88
E154	5-Bit 2:1 Mux-Latch	Common Enable, Reset	Diff.	1Q 88
E131	4-Bit D Flip-Flop	Individual CLK, Reset	Diff.	2Q 88
E171	3-Bit 4:1 Multiplexer	Split Select	Diff.	2Q 88
E156	3-Bit 4:1 Mux-Latch	Common Enable, Reset	Diff.	2Q 88
E160	12-Bit Parity Generator/Checker	Register-Shiftable	Diff.	2Q 88
E451	6-Bit D Register, Diff. Data & Clk Inputs	Vbb, Common Reset	SE	2Q 88

All resets are asynchronous. Diff. = Differential, SE = Single Ended.

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LETTERS

Comparing RISC and CISC

To the editor: I enjoyed reading the articles on computer architectures [*Electronics*, Sept. 3, 1987, pp. 59-74], although my quotes may have put me in several doghouses.

The arguments pitting reduced-instruction-set computer chips against complex-instruction-set chips imply that Hewlett-Packard's RISC-based Spectrum would win the argument for RISC chips. A comparison of the Spectrum with a CISC machine, the HP 3000, is interesting.

First, the HP 3000 is 16 bits, while the Spectrum is 32 bits, giving the Spectrum the benefit of a wide address, 4 bytes/throw, and fewer I/O cycles. Second, the HP 3000 has a memory-stack architecture, while the Spectrum has a register-intensive architecture, enabling the Spectrum's CPU registers to provide higher performance. Finally, the 4.5 mips of the Spectrum is four times faster than the 1.1 mips of the HP 3000.

The results? HP says that the Spectrum has 1.6 times the performance of the HP 3000 in "native mode." The RISC machine can squeeze out only 60% more than the 1974 vintage 16-bit HP 3000. (HP has stated that they hope to get the performance up to twice the performance of the HP 3000.)

I must be missing something. Could it be that the equation on page 60, T = N x I x C, when applied to a RISC computer, shows that, counting overhead in the RISC computers, the function I, for average number of clocks per instruction, is much larger than expected? T, time to execute program, is observed; N, number of instructions in the program, is an actual count; and C, basic clock cycle time, is measured. It seems to be a wish that doesn't hold up in the real world. Perhaps by a factor of four? If Spectrum were 6.4 times the performance of the HP 3000, even Davin might look at RISC.

D. H. Methvin
Founder
Davin Computer Corporation
Irvine, Calif.

Correction:
In the Sept. 17 issue [Electronics, *p. 95*], *Calma Co. was described as having 70% of the full-custom integrated circuit layout market, which was estimated to be worth $200 million at the end of 1987. Instead, the article should have reported that Calma has 13% of the worldwide IC layout market, which was worth $281 million in 1986, according to Dataquest Inc. Of the total 4,000 systems installed in 1986 for full-custom IC layout, a segment of the total IC layout market, however, Calma has 75%.*

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ELECTRONICS NEWSLETTER

TRADE SANCTIONS SEEM TO BE CUTTING JAPAN'S SHARE OF CHIP MARKET

Trade sanctions imposed by the U. S. last April helped stop Japan from dumping chips and cut into its share of the world chip market last summer, says Michael A. Gumport, an analyst with Drexel Burnham Lambert Inc. in New York. Even so, it took the Reagan Administration until early November to ease the punitive sanctions. Japan's share of the world merchant chip market slipped in August to 52.1% of a total $2.6 billion market, from 53.7% of $2.7 billion in July, Gumport says. In the U. S., Japan's share dropped from 14.9% in July—which was good for $126.6 million in sales—to just 13.7%, or $120.3 million, in August. Gumport notes that if price wars resume, the tariffs on certain Japanese color TVs, computers, and power tools could be reinstated quickly. Not all the sanctions are being lifted, though. Some will remain in effect until Japan opens its market to U. S.-made chips. ☐

INTEL OFFERS A PEEK AT THE FUTURE: THE MAINFRAME-ON-A-CHIP

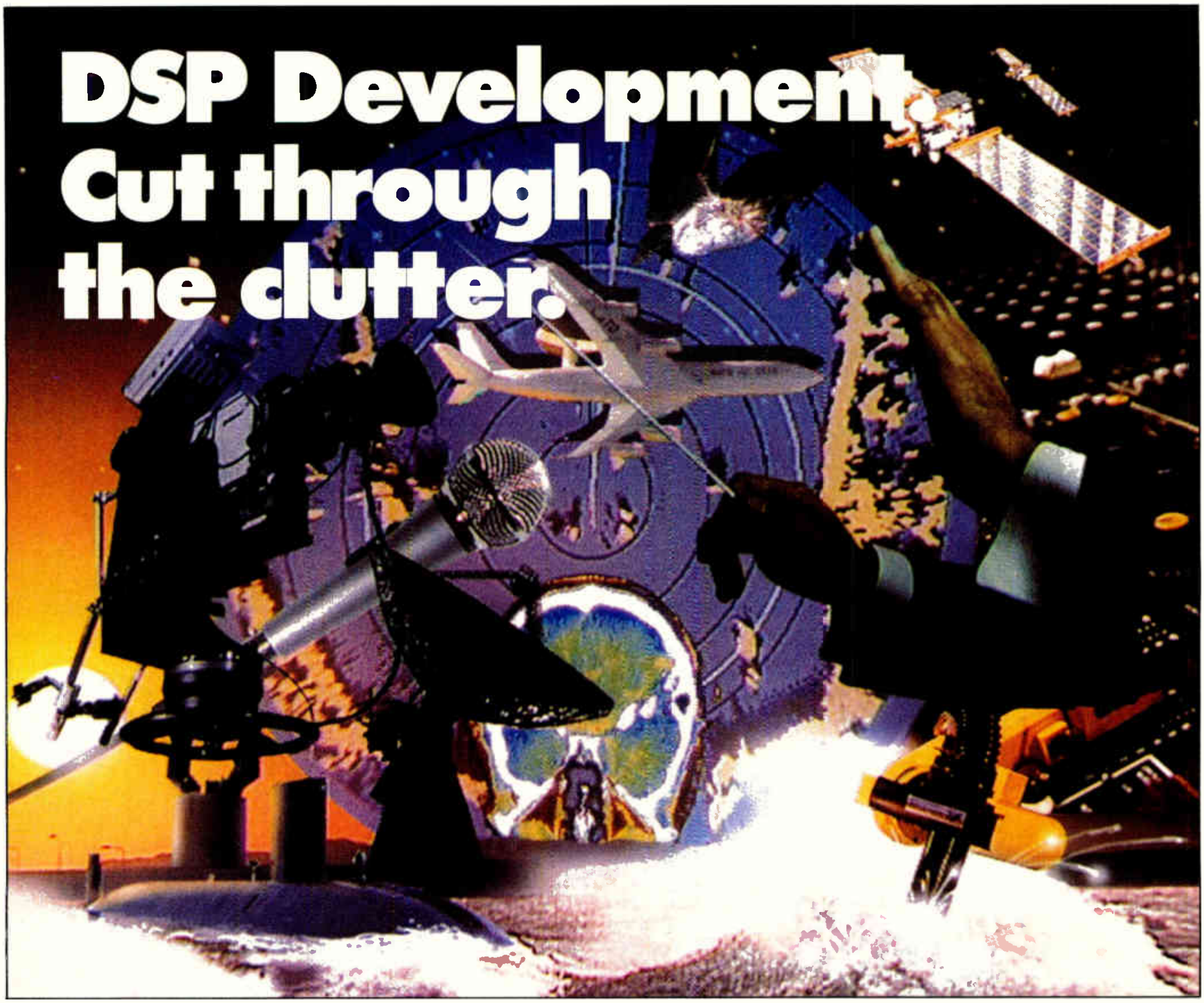
IBM wasn't the only one trying to create a bandwagon effect at Comdex (see p. 31). Intel Corp. "opened up the kimono" on what will become the successor to its 32-bit 80386 microprocessor. Perhaps to be called the 486, it will be announced sometime in 1989. The million-transistor chip will be fully compatible with the 386, says Dave House, Intel senior vice president. He estimates that mainframe-class machines built around the new microprocessor would be available commercially in 1990. "Between now and 1990, we'll be introducing silicon for every segment of computer product," House said. In his ongoing battle with Motorola over 32-bit microprocessor leadership, he told a Comdex audience the 386 has now chalked up more than 400 design wins. Claiming that Intel is already outshipping Motorola, company managers say they'll be disappointed if they don't ship 2 million 386s next year. ☐

MOTOROLA AND NATIONAL END FEUD, TEAM UP ON FACT LOGIC

The falling out between Motorola Inc. and National Semiconductor Corp. over an ill-fated 1982 gate-array alliance has finally ended and the two chip makers are announcing a major alternate-sourcing pact. The three-year deal will cover 108 advanced CMOS logic components. National and Motorola will take on National's advanced CMOS process (FACT) in three phases. The first 30 designs are now being given to Motorola. Data is being exchanged to assure CMOS compatibility, but no process technology is being traded. In phase 2, National will give Motorola 16 more devices early next year. In return, Motorola will help speed National's introduction of 22 FACT logic parts by completing device characterization and qualification work. In the final phase, the companies will share 40 new FACT designs in 1989. ☐

AMD AND READY SYSTEMS POINT THE 29000 AT EMBEDDED CONTROL

Advanced Micro Devices Inc. is trying to stake out an early claim in the virgin 32-bit microcontroller market by aiming its Am29000 reduced-instruction-set microprocessor at real-time embedded control. AMD and Ready Systems Corp. of Palo Alto, Calif., have entered into a joint-technology pact to produce a real-time operating system for the RISC chip, which boasts peak performance of 25 million instructions/s [*Electronics*, March 19, 1987, p. 61]. To adapt its VRTX32 operating system to the 29000, Ready Systems plans to add more than 30 directives, enabling the RISC processor to run functions required in such real-time embedded control applications as industrial robotics, communications, and weapons systems. In addition to creating a 29000 version of VRTX32, Ready Systems will provide versions of a multitasking debugger, called RTscope, and a system monitor for the processor. ☐



You've seen the advantages offered by the A100 Digital Signal Processor. The single-chip DSP solution that features 32 multiply-accumulators, executes up to 320 MOPs, and easily attaches to microprocessors.

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PRODUCTS NEWSLETTER

NEC'S 2-MBIT EPROM PROGRAMS 72 TIMES FASTER PER BIT

The tedious process of programming large ultraviolet-erasable programmable read-only memories will be speeded up considerably with NEC Corp.'s 2-Mbit EPROM. It can be programmed in just 10 seconds—72 times per bit faster than using 256-Kbit EPROMs that each take 90 seconds. Chip designers turned the trick with a method that simultaneously programs 4 bytes with each 0.1-ms, 12.5-V pulse. Fabricated in 1.2 μm design rules, the 7-by-10.48-mm μpD27C2001D boasts 150-ns access times—fast for a device its size. Operating current is 30 mA maximum at 6.7 MHz and 100 μA maximum standby. Operating voltage for the 32-pin ceramic dual in-line package is 5 V. The Tokyo-based company is now offering samples of the device priced at about $70, with production slated for March 1988. ☐

IDT BOOSTS SPEED 75% IN ITS 16-BY-16-BIT MULTIPLIERS

High-speed applications in radar, digital filtering, and fast Fourier transforms could open up for 16-by-16-bit parallel multipliers, now that Integrated Device Technology Inc. has built a 75% speed improvement into its multiplier family, already a performance leader. Its 1.2-μm logic-oriented process has spawned the IDT7216 and 7217, both boasting 20-ns multiplication times, compared with the 35-ns speed of their predecessors. The Santa Clara, Calif., company's CMOS multipliers consume 120-mA, one-tenth the power of compatible bipolar parts. The 7216 is pin-compatible with the MPY016H/K from TRW Inc., Redondo Beach, Calif., and the Am29516 from Advanced Micro Devices Inc., Sunnyvale, Calif. The 7217 requires a single clock with a register to be compatible with AMD's bipolar 29517. In 100-piece lots, the multipliers sell for $145 each in plastic 64-pin dual in-line packages. Samples are available now. Volume shipments will begin in the first quarter of 1988. ☐

HIGH-END GRAPHICS SUBSYSTEM COSTS 40% LESS THAN COMPETITION

System integrators can grab about a 40% cost savings with a graphics subsystem from Metheus Corp. that delivers 1,024-by-768-pixel resolution and a 10-million-pixels/s drawing rate for $2,495—performance now available only in systems costing $4,000. At the unit's heart is the Hillsboro, Ore., company's UGA 1104 graphics coprocessor board [*Electronics,* Oct. 1, 1987, p. 98]. In addition to its speed and resolution, the 1104 handles four bit planes and supports interlaced scan rates of 40 Hz, and noninterlaced scan rates of 60 Hz. Packaged with the card are a Sony Corp. of America 13-in. color monitor, diagnostic software, and drivers for computer-aided-design applications. The Ultra Graphics Video Subsystem is available now. ☐

AUTOMATION CONTROLLER COMBINES MULTITASKING POWER AND MS-DOS

Automation engineers can now take advantage of the vast software library written for IBM Corp. Personal Computers and compatibles, thanks to Square D Co.'s Sy/Gate Minicell controller. At the same time, they can harness the power of a proprietary multitasking operating system that addresses up to 1.5 Mbytes of memory compared with MS-DOS's 640 Kbytes. Based on an Intel Corp. 80286 processor and 80287 math coprocessor, the MiniCell boots up on MS-DOS but also runs a proprietary operating system that boasts an integrated set of functions for cell-control applications such as communication with factory peripherals and report generation. Industrialized IBM PC AT systems typically require a fan for cooling, but the MiniCell runs without a fan. That contributes to its 14-by-6.25-by-6.5-in. cabinet size—one-fifth that of comparable products. Equipped with 1.5 Mbytes of random-access memory, the MiniCell will be available by year's end for $14,995. ☐

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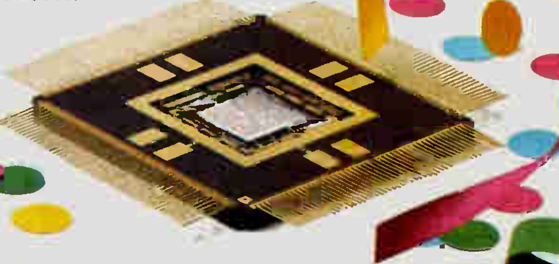

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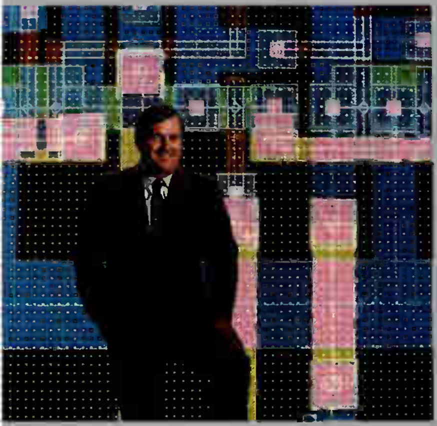

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Electronics

AT COMDEX: PC MAKERS FIGHT HARD TO UPSTAGE IBM

SO IBM GOES ALL OUT TO CREATE A PS/2 'BANDWAGON'

LAS VEGAS

An outpouring of personal computers built around Intel's 80386 microprocessor showed up at last week's Comdex to challenge IBM Corp.'s PS/2 line and its Micro Channel bus architecture. With at least 40 exhibitors showing these new 32-bit machines, IBM Corp. fought back by attempting to create a PS/2 bandwagon. Challenges to Micro Channel from PC-compatible makers and other suppliers had already reached the flash point and IBM uncharacteristically decided to counter them by reporting PS/2 shipping rates, detailing growing software support, and speeding up the delivery of vital operating systems needed to make PS/2 work.

"It is our intention to have the industry move to the PS/2 [standards]," vowed William Lowe, president of the Entry Systems Division, at a hastily called meeting of dealers at the Las Vegas show. Leaving no doubt that the PS/2 and Micro Channel represent IBM's entire thrust in personal computers [*Electronics*, April 18, 1987, p. 46], Lowe slammed the door on any possibilities that the company would return to earlier open standards. IBM also announced that OS/2 software, believed to be behind schedule, would instead be brought out Dec. 4, about four months earlier than planned. However, that is less than meets the eye, because a crucial part of the system, the Windows Presentation Manager, won't be ready until the end of 1988.

VITAL ISSUE. But it is the issue of Micro Channel that is vital to compatible-PC makers since the architecture, unlike that of the original PC, is protected by patents—among them one that IBM acquired from Computer Automation Inc., which developed it in 1974 for minicomputers. That patent position becomes, in the view of most observers, the prime means by which IBM can restrict outsiders from copying the PS/2.

The company says an upgraded bus like Micro Channel is needed for the 80386-based PS/2 computers since it is faster and more reliable than the AT bus and can efficiently accommodate multiple intelligent processors for peripheral control and other tasks. Nevertheless, of the million PS/2 units shipped so far, only 350,000 have been equipped with Micro Channel—and few of them have been the top-of-the-line Model 80s.

The result has been that since April, Big Blue has sown confusion about its intentions with Micro Channel by saying nothing. Competitors, and a vast array of board and chip suppliers, have had to strike out on their own, without any solid guidelines from the company that has set PC standards. While this guarantees a fast hardware start in getting PS/2-like computer hardware to market, the risk is that a decisive move by IBM to impose the Micro Channel as a standard could put many competitors out on a shaky limb with incompatible clone hardware.

The confusion became a central issue at Comdex. "We're still unsure of the details or implications of Micro Channel," says Enzo Torresi, senior vice president for product and strategic planning at Businessland Inc. in San Jose, Calif. He chaired a panel of IBM-watchers who discussed the topic.

The panel couldn't agree on when or even if IBM would license Micro Channel. IBM is "dragging its feet" on licensing its utility patents—"the most they'll license," says William F. Zachman, vice president of International Data Corp., Framingham, Mass. IBM will license other firms if it doesn't sell enough of its own Micro Channel products to make it the standard, he maintains. "If IBM doesn't want Micro Channel to be cloned, it will not get built," he says. "IBM will sue their pants off."

Esther Dyson, newsletter publisher and software guru, disagreed. She says IBM will license "sooner rather than later because they realize this is the way to build the market." But the panelists did agree that it will take other computer makers at least a year to come up with Micro Channel clones and that these products would show up at next fall's Comdex.

But there is no question about the market potential. The worldwide market in 1987 for personal computers and related equipment will come to some $35 billion, of which IBM sells about $7 billion. That opportunity has computer suppliers rushing to fill the market, and at Comdex they were in their glory. Judging from Comdex, the Intel 80386 is the microprocessor of choice, as nearly 40 new PCs based on the fast chip were shown. Among them:

- AST Research Inc., Irvine, Calif., demonstrated its Premium/386 that runs at 20 MHz and uses a proprietary Smartslot architecture that the company says provides the same multiprocessor functionality as Micro Channel. It is actually an extension of the AT bus, so it is compatible with existing software. Shipments start this month.
- Compaq Computer Corp., Houston, offers the Deskpro 386/20 with 20-MHz speed and an optional coprocessor board that boosts it to engineering work-station status. Compaq believes Micro

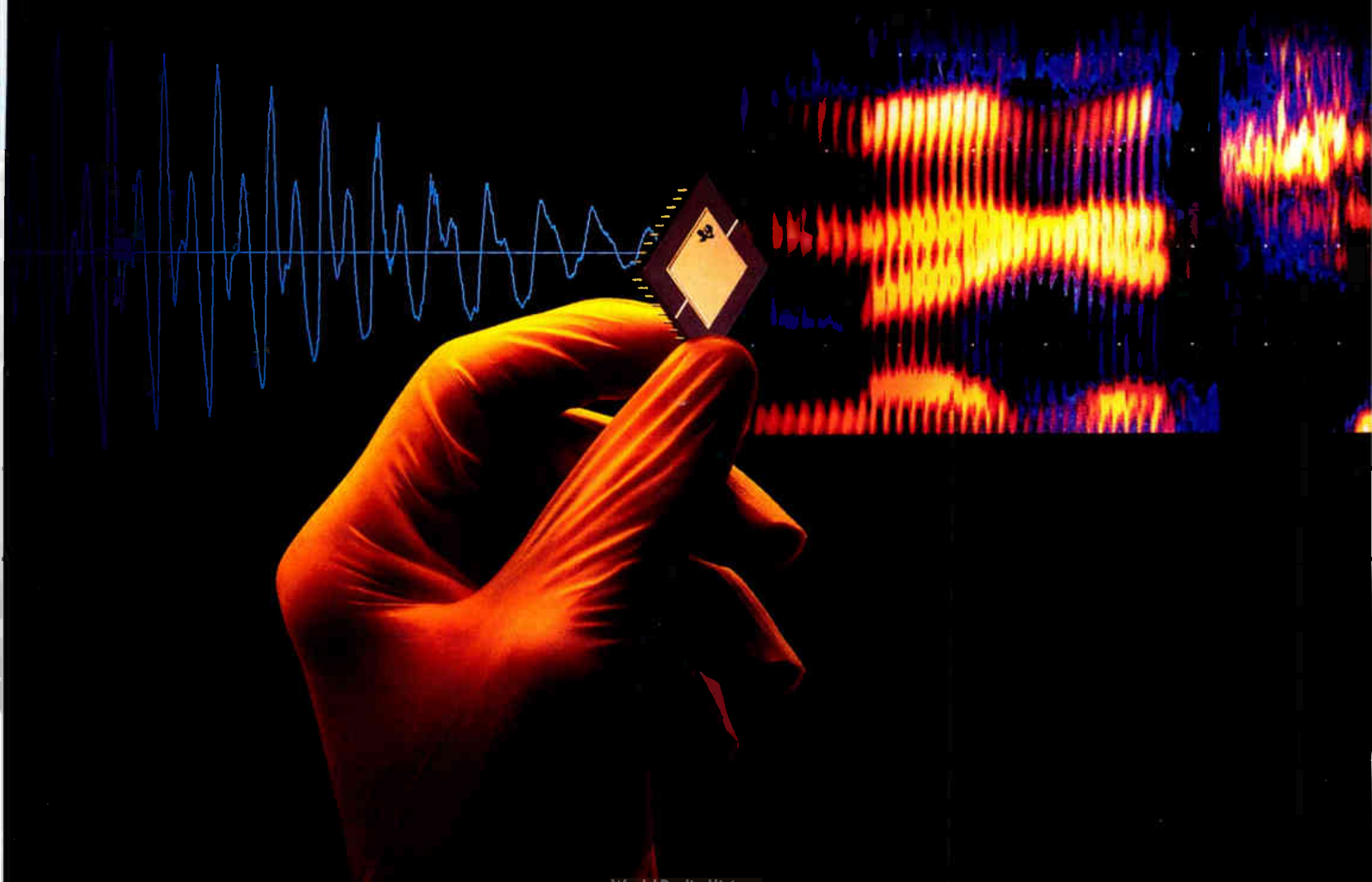
THE BIG QUESTION AT COMDEX: JUST HOW SUCCESSFUL IS THE PS/2?
Even as IBM moved at Comdex to head off challengers in its drive to make the PS/2 an industry standard, a big question at the show was, can it be called a success? IBM was quick to ballyhoo that it has shipped 1 million PS/2s—only a third of them with the Micro Channel architecture—with the OS/2 operating system not shipping until December. The answer: not yet.

TEXAS INSTRUMENTS REPORTS ON

DSP

IN THE ERA OF

MegaChip TECHNOLOGIES



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"Handling performance is up there next to speed in Formula 1 racing. TI's TMS320 gives us a real advantage — enough to win a Grand Prix." Peter G. Wright, Technical Director, Lotus Engineering

Lotus designed the active suspension in their Camel-Lotus-Honda Formula 1 car to approach the theoretical maximum-control point which gives the best balance between handling and performance. At racing speeds, each wheel is positioned by the TMS320-controlled hydraulics. A single TMS320 chip measures wheel forces and displacements and reads data from a body-mounted inertial platform. Then, in real time, the chip computes wheel position and controls actuators that adjust the suspension components to precise settings.

The TMS320 can also handle closed-loop engine control and more responsive braking systems, as well as many other automotive applications.

"The TMS320 helps us with one of our toughest tasks — designing toys with exciting features at prices that will sell." Dave Small, VP Engineering, Worlds of Wonder, Inc.

Worlds of Wonder is a pioneer in developing interactive toys and now has an innovative new doll named Julie™ Using a single TMS320 chip, Julie's designers are able to give her voice-recognition ability, coupled with synthesized speech and coordinated facial movement.

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There are 15 compatible members in the TMS320 family (*see the road map below*), featuring two new DSPs with on-chip EPROM, the TMS320E15 and the TMS320E17. For applications requiring off-chip memory, there is the new CMOS EPROM, the TMS27C292, with 35-ns speed.

New interface alternatives include the low-cost CMOS TCM29C18/19 Combo Codecs with A/D, D/A, and filters all on a single chip.

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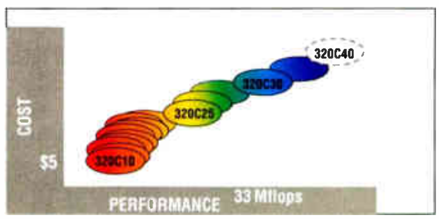

From $5 to 33 Mflops: With three generations covering 15 products, the TMS320 family offers software compatibility to protect your development investment and provide a smooth path to future applications.

For more information on support for the TMS320 family, please turn the page.

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TEXAS INSTRUMENTS

NEC PUTS 100 LASER BEAMS ON ONE FIBER

KAWASAKI, JAPAN

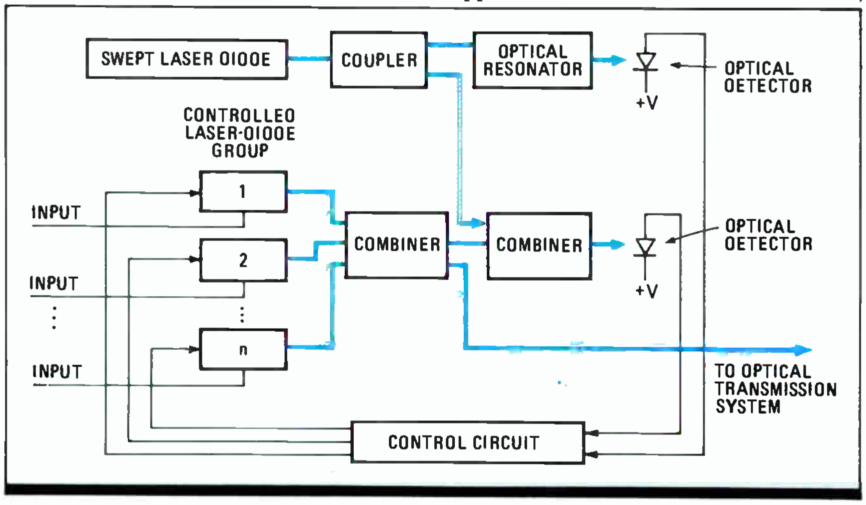
Today's fiber-optic systems can transmit up to three or four digitally modulated laser beams per fiber, but one-beam systems predominate. However, researchers at NEC Corp.'s Opto-Electronics Research Laboratories in Kawasaki have demonstrated a way to use microwave techniques that can transmit a hundred or more beams over one fiber.

Though large-scale use may be as much as five years away, NEC sees first applications in local area networks, leased subscriber lines, and switching systems. In the long range, similar systems could see residential use.

The method is based on frequency-division multiplexing to get those separate channels on different frequency carriers. Heterodyne reception techniques make it possible to tune to desired channels, each of which might be a single high-definition TV channel or be further divided into a large number of digital time-division multiplexed channels in the manner of present fiber-optic systems.

NEC's experimental gear has multiple channels with only 15 GHz between them. But according to preliminary calculations, the system will handle from 140 channels with 5-GHz spacing to 50 channels with 15-GHz spacing. The same technology should be applicable to optical switching networks as replacements for electronic switching.

There are two keys, says Mitsuhito Sakaguchi, general manager at the labs. One is a method of stabilizing a large number of individual laser diodes with frequency spacings of about 15 GHz,



PACKING THEM IN. With microwave-like techniques for carrier-frequency stabilization and frequency-division multiplexing, NEC's system gets 100 laser beams on a fiber.

with short-term stability improved to about 20 MHz from about 1 GHz. The other is optical heterodyne reception, enabling the system to be tuned to separate channels in the manner of superheterodyne microwave receivers. Wavelength-division multiplexing has been used in a small number of systems, but the difficulty of building filters to separate closely spaced wavelength beams at the receiving end has limited such systems to three or four channels.

FEEDBACK LOOP. The implementation of the NEC carrier-frequency stabilization method is innovative. It uses a feedback loop that includes a swept-frequency laser developed earlier by the lab and an optical resonator, used as an optical comb filter, that is about 10 mm long. This is the length of one round trip in air at 15 GHz, the spacing of the optical channels.

The starting frequency of the swept-frequency laser is slightly lower than that of the system's lowest-frequency channel, and its highest frequency is somewhat above the highest-frequency channel. The resonator filters out all but harmonics of 15 GHz from the swept-frequency laser as the rising laser frequency successively passes through integral multiples of 15 GHz.

Each signal peak at the output of the resonator can be considered similar to one of the high-order harmonics from the crystal oscillator often used as a reference to lock the frequency of a microwave system. One difference is that the time at which each appears during the excursion of the swept-frequency laser indicates which of the many resonances it is—that is, its frequency.

As shown in the figure, the resonator output signal is detected to provide timing information. A portion of the swept-laser signal obtained ahead of the resonator is fed into an automatic frequency-control loop where it is used as the reference signal to control in turn the frequency of each of the many lasers in the system.

Outputs of the modulated lasers are combined for transmission. A small portion of the combined outputs is tapped off for use by the automatic frequency-control circuit. The swept-laser signal at the resonator output and the combined modulated laser signals are heterodyned together in the second optical detector to generate a microwave signal whose frequency determines the AFC loop-correction current applied to each particular laser.

At the receiving side, a laser diode is used as the local oscillator to heterodyne in a balanced mixer the signals arriving from the transmitter. Arriving signals would be pulse-frequency or pulse-phase modulated in the manner of modem signals.

Coherent reception provides higher sensitivity than is possible with present systems. In a nonmultiplexed system with its new technology, NEC researchers have achieved transmission over 300 km at a data frequency of 34 Mbits/s, without repeaters. *–Charles L. Cohen*

MILITARY

A PAPERLESS DOD: ARE SUPPLIERS SET?

DETROIT

The Defense Department's two-year-old drive to convert its weapons systems documentation from paper to an electronic data base will cost billions of dollars and take more than a decade. But despite top-level industry involvement, knowledge of CALS (for Computer-aided Acquisition and Logistics Support) and its implications has not yet trickled down to many second- and third-tier defense suppliers, DOD officials say. That's why the Autofact show that starts Nov. 10 in Detroit will devote

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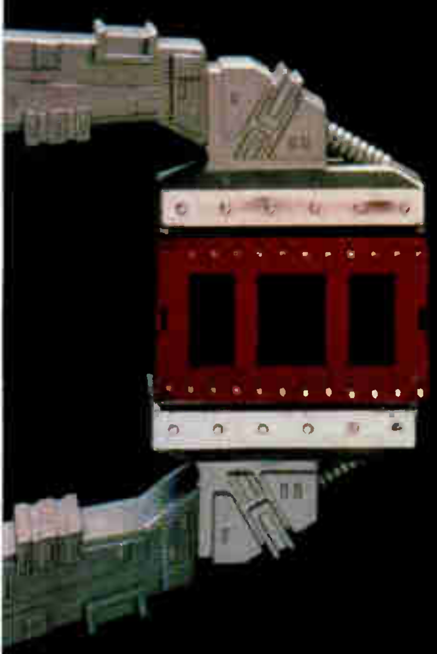

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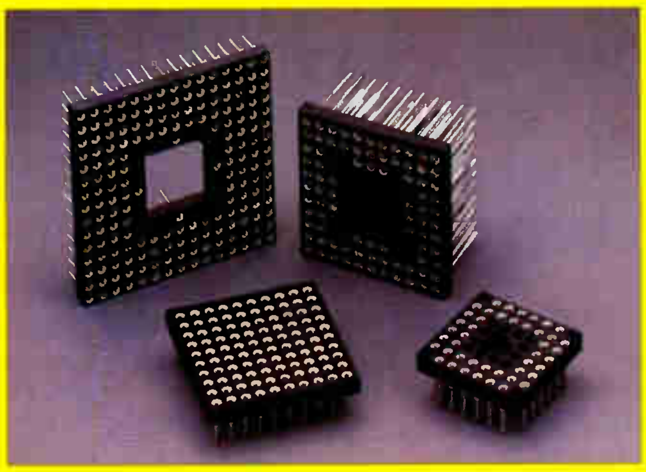

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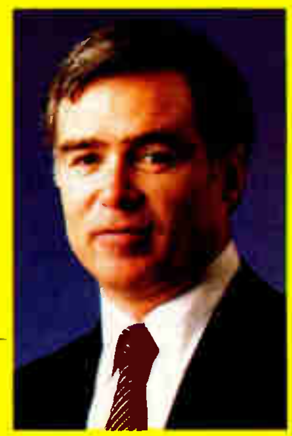

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INTERNATIONAL NEWSLETTER

TURNABOUT IS FAIR PLAY: IBM COMPUTERS NOW RUN FUJITSU SOFTWARE

IBM Corp. is getting a chance to reclaim some of the Japanese mainframe market that had been captured by IBM-compatible mainframes. That's because the recently arbitrated settlement between IBM and Fujitsu Ltd. cuts both ways. It gives the Japanese computer maker access—for a price—to IBM system software so its systems can run IBM applications with little adaptation. But it also opens the way for IBM systems to use Fujitsu software. Under the terms of the settlement, IBM Japan has come up with special software, called migration programs, that let software written for Fujitsu machines run on IBM computers. Kawasaki-based Fujitsu had never licensed its operating-system software for use on any but its own machines, but the American Arbitration Association's order gives customers a right to license Fujitsu software, in countries where it is marketed, for use on IBM machines. Unpatched applications written for Fujitsu machines can thus run in Fujitsu's OSIV/F4 MSP E20 operating environment, which in turn runs under the VM operating system of an IBM 4381 computer thanks to the migration-program interface. Although it sounds cumbersome, this arrangement does not impose significant overhead, largely because of the similarity between the IBM and Fujitsu machines. Migration programs have also been developed for Hitachi software, so it is now possible to replace Fujitsu or Hitachi mainframes with an IBM product or to add an IBM system in a Fujitsu or Hitachi environment. Only time will tell whether IBM can regain market share in this way. □

IBM AND SIEMENS TEAM UP TO STUDY WAYS TO BUILD SMART NETWORKS

The web of international linkups in information processing, which unites friends and sometimes foes, now ties West Germany's Siemens AG to IBM Deutschland GmbH, a subsidiary of the U. S. computer maker. The two are embarking on a joint study of intelligent communication networks. They are considering linking IBM computers with Siemens telephone-exchange systems to form networks that allow callers to charge call fees to credit cards and use other new types of services. The pact brings together two powerful partners, each strong in an area where the other is weak. IBM, the world's biggest computer maker, could use a boost in communications technology. And Siemens, No. 3 in the world in communications, could use a shot in the arm to bolster its relatively weak presence in international computer markets. Industry observers in West Germany suspect that after its rather unhappy marriage to Rolm of Santa Clara, Calif., IBM sees the need for a stronger partner to develop the networks of the 1990s. □

NEC IS PILING ON MORE ASIC CAPACITY IN JAPAN AND U. S.

In reaction to a rapidly increasing demand for application-specific integrated circuits, NEC Corp., Tokyo, plans to build a new line for assembling ASICs into their packages at its Roseville, Calif., plant, and two ASIC wafer-fabrication lines at a manufacturing subsidiary, NEC Kyushu Ltd., in Kumamoto. The new line at the Roseville plant, which is now manufacturing 3 million to 3.5 million 256-Kbit dynamic random-access memories a month, will start assembling gate arrays into packages at the rate of 10,000 to 20,000 units a month at the beginning of next year. NEC will invest $7.3 million for the new line. At Kyushu, some $62 million will initially go into the 6-in. wafer-fab lines, which are scheduled to manufacture custom and semicustom microcontroller chips and gate arrays at the rate of 1,000 wafers per month starting next April. With additional investment, the lines' capacity will be boosted to some 10,000 wafers a month by the latter half of next year. NEC expects the ASIC percentage of its semiconductor sales to rise from the present 38% to 50% within two to three years. □

INTERNATIONAL WEEK

OUTPUT OF GERMAN PROCESSORS FALL

West German production of data-processing equipment during the first seven months of 1987 fell 6% compared with the same period last year, says the country's electronics industry association, based in Frankfurt. The prime reason for the decline is the slowing output of data-storage systems, which dropped 21%, and of plotters and other recording systems, which fell 15%. Central processing units stayed at last year's level.

JAPANESE TO MAKE ERASABLE DISKS

Japanese chemical companies are preparing for mass production of erasable magneto-optic disks starting next year. Three firms, Daicel Chemical Industries Ltd. and Sumitomo Chemical Co., both of Osaka, and Mitsui Petrochemical Industries Co. of Tokyo, have developed prototypes, but are disclosing specifications only to disk-drive makers actively developing drives. Sumitomo will start marketing first, in January 1988, with 100,000 units in the initial year. Mitsui and Daicel do not have firm plans yet. All the disks are plastic-based, such as polycarbonate substrate for Daicel and amorphous polyolefin for Mitsui.

STRONG GROWTH SEEN FOR EUROPE

The year ahead could be the best one for the European electronics industry since 1984, reports a British market forecaster. The 1988 market for electronics equipment and components is estimated to be $144 billion (at constant 1986 values and exchange rates), a real growth of 7.5% over 1987. By contrast, 1987 growth is estimated at 4.4%. Growth higher than 7.5% was last logged in 1984, when a spurt of 13% was recorded, according to Benn Electronics Publications in its 1988 *Yearbook of West European Electronics Data.* The Luton, England, forecaster singles out data processing as the most buoyant sector for 1988 and consumer electronics as the least promising.

ASAHI ENTERS LCD TV MARKET

The first Japanese camera maker to enter the market for liquid-crystal-display TV sets, Asahi Optical Co. of Tokyo, will market a color LCD TV with a 3-in. screen starting Dec. 1 in Japan. The thin-film-transistor active-matrix screen, with a resolution of 92,160 dots, will be supplied by Sharp Corp., Osaka. It is a redesigned private-label version of the 3-in. color LCD TV that Sharp started selling last month [*Electronics*, Oct. 15, 1987, p. 54]. Asahi expects its set to help increase the sales of its 8-mm camcorder, which is made by Hitachi Ltd., since the TV can be used as a portable monitor for the camcorder. The firm hopes to sell 2,000 units a month at 49,800 yen.

NATIONAL TO CLOSE GERMAN PLANT

Look for National Semiconductor Corp. of Santa Clara, Calif., to shut down its Wasserburg, West Germany, production plant by the end of this year. The facility was part of Fairchild Semiconductor Corp., which has been bought by National. About 270 people will be affected by the shutdown. National will shift the Wasserburg production to its plant in Singapore.

SIEMENS, DEC TO LINK OA EQUIPMENT

Munich-based Siemens AG and Digital Equipment Corp. of Maynard, Mass., have agreed to cooperate in applying each other's equipment in office automation. That means that the German firm's private switching systems could be coupled to DEC computers in certain office environments. For example, a DEC VAX computer could make a Siemens switch establish phone connections. Conversely, a Siemens switch could make a VAX computer display on a terminal screen information stored by the computer.

ALCATEL TEAMS WITH SGS-THOMSON...

Alcatel NV, the European telecommunications giant formed last year when France's Compagnie Générale D'Electricité bought the European telecommunications interest of ITT [*Electronics*, July 24, 1987, p. 113], has signed up an ally for semiconductor expertise. The new partner is SGS-Thomson, the joint company that France's Thomson Semiconducteurs and Italy's SGS-Microelettronica recently put together [*Electronics*, June 11, 1987, p.54C]. From the deal, Alcatel will get a leg up for telecommunications chips. SGS-Thomson, in turn, will have better access than its competitors to the technology of Alcatel, whose sales last year reached $12.7 billion.

...ADDS PARTNERS IN CELLULAR RADIO

To cash in on the booming European cellular radio market, Alcatel will throw its lot in with Nokia Group of Finland and AEG of West Germany. The three firms have agreed to form a consortium to develop and market cellular radio gear.

PLESSEY TO SUPPLY SYSTEM X TO CHINA

Plessey Telecommunications Systems has won a contract worth over 6 million pounds to supply China Railways in the People's Republic of China with its System X, a public switching system. Twenty-six local exchanges with a capacity of 24,000 lines and remote concentrators will be delivered by 1989 for the Zhengzhou to Baoji Railway Electrification Project. This was Plessey's second major System X international sale, after one to Colombia.

ADVANCED E-BEAM PLANT OPENS

European Silicon Structures Ltd. of Edinburgh has opened the first second-generation electron-beam processing plant in Europe. The direct-write, fast-turnaround silicon prototyping plant in Rousset, in southern France, will produce small quantities of application-specific integrated circuits under tight deadlines. A year ago, the company installed the world's first such machine in San Jose, Calif., for Exel.

CHIPS BOUNCE BACK IN UK

The UK book-to-bill ratio for semiconductor sales bounced back to 1.36 in September after tumbling from 1.40 in July to 0.91 in August, says the Electronic Components Industry Federation. The industry shows signs of growth compared with a year ago, when the book-to-bill ratio was 0.82 in September. The growth, however, is primarily in data processing, notes the ECIF.

SIEMENS PRINTERS GET 18 NEEDLES

Siemens AG has added two color units to its lineup of needle printers, both based on 18-needle print technology. Intended for Siemens-made personal computers and all IBM PC-AT-compatible systems, the new printers can produce up to three copies. The $940 PT18 and $1,165 PT19, for paper widths up to 250 mm and up to 400 mm, respectively, print as many as 300 characters per second in the rapid-print mode.

L-117

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INPUT VOLTAGE	95 to 132 VAC / 187 to 265 VAC, 47-440 Hz	________
DOLLARS/WATT	From 52¢/Watt	
SIZE/DENSITY	Up to 4 Watts/in³	

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Now, Lambda's LFS Series single output switching power supplies are even more economical, with prices reduced up to 20% in single piece quantities. The LFS Series has been designed for applications where high power density...up to 4.0W / in³...and high reliability are of paramount importance.

The LFS Series is available in 54 models in 6 package sizes, from 2V to 48V, with currents up to 200A, and is priced below $190.00. All models feature customer selectable dual input, turn-on in-rush current limiting, built-in overvoltage protection, remote turn-on / turn-off, and an isolation rating of 3750V RMS.

Using new advances in surface mount technology and by incorporating Lambda's unique new monolithic PWM control circuit, the LFS Series has achieved a 40% reduction in parts, thereby increasing reliability.

Lambda's LFS Series has been designed to meet UL, CSA, VDE and IEC specifications (some units have already been approved, the balance are in evaluation). All models are guaranteed for one year and are available for one day delivery from stock.

VOLTAGE AND CURRENT RATINGS

	MAX CURRENT (AMPS AT)				PRICE				
	40°C	50°C	60°C	DIMENSIONS (Inches)	QTY. 1	QTY. 100	QTY. 250	QTY. 1000	MODEL
2V ±5% ADJ.	40.0	33.5	25.0	1.9 × 4.75 × 9.125	$280	$228	$207	$189	LFS-43-2
	60.0	45.0	33.5	1.9 × 4.75 × 11.75	360	297	270	252	LFS-44-2
	90.0	67.5	45.0	1.9 × 4.75 × 16	480	392	371	342	LFS-45-2
	120.0	112.0	93.5	5 × 4.875 × 7.25	580	450	428	403	LFS-46-2
	150.0	142.5	120.0	5 × 4.875 × 8.875	680	560	478	450	LFS-47-2
	200.0	185.0	157.0	5 × 4.875 × 11	800	680	600	560	LFS-48-2
5V ±5% ADJ.	40.0	33.5	25.0	1.9 × 4.75 × 9.125	280	228	207	189	LFS-43-5
	60.0	45.0	33.5	1.9 × 4.75 × 11.75	360	297	270	252	LFS-44-5
	90.0	67.5	45.0	1.9 × 4.75 × 16	480	392	371	342	LFS-45-5
	120.0	112.0	93.5	5 × 4.875 × 7.25	580	450	428	403	LFS-46-5
	150.0	142.5	120.0	5 × 4.875 × 8.875	680	560	478	450	LFS-47-5
	200.0	185.0	157.0	5 × 4.875 × 11	800	680	600	560	LFS-48-5
6V ±5% ADJ.	35.0	28.0	20.5	1.9 × 4.75 × 9.125	280	228	207	189	LFS-43-6
	50.0	37.5	28.0	1.9 × 4.75 × 11.75	360	297	270	252	LFS-44-6
	75.0	56.0	37.5	1.9 × 4.75 × 16	480	392	371	342	LFS-45-6
	101.0	94.5	79.0	5 × 4.875 × 7.25	580	450	428	403	LFS-46-6
	126.0	120.0	107.0	5 × 4.875 × 8.875	680	560	478	450	LFS-47-6
	168.0	155.0	132.0	5 × 4.875 × 11	800	680	600	560	LFS-48-6
12V ±5% ADJ.	19.0	15.0	11.0	1.9 × 4.75 × 9.125	280	228	207	189	LFS-43-12
	26.0	18.5	13.5	1.9 × 4.75 × 11.75	360	297	270	252	LFS-44-12
	40.0	30.0	20.0	1.9 × 4.75 × 16	480	392	371	342	LFS-45-12
	51.5	48.0	40.0	5 × 4.875 × 7.25	580	450	428	403	LFS-46-12
	64.5	61.5	55.0	5 × 4.875 × 8.875	680	560	478	450	LFS-47-12
	86.0	79.5	67.5	5 × 4.875 × 11	800	680	600	560	LFS-48-12
15V ±5% ADJ.	15.5	12.0	9.0	1.9 × 4.75 × 9.125	280	228	207	189	LFS-43-15
	21.0	15.5	11.5	1.9 × 4.75 × 11.75	360	297	270	252	LFS-44-15
	32.5	24.5	16.0	1.9 × 4.75 × 16	480	392	371	342	LFS-45-15
	42.0	39.0	33.0	5 × 4.875 × 7.25	580	450	428	403	LFS-46-15
	52.5	50.0	44.5	5 × 4.875 × 8.875	680	560	478	450	LFS-47-15
	70.0	64.5	55.0	5 × 4.875 × 11	800	680	600	560	LFS-48-15
20V ± 5% ADJ.	11.8	9.2	6.8	1.9 × 4.75 × 9.125	280	228	207	189	LFS-43-20
	16.0	11.5	8.5	1.9 × 4.75 × 11.75	360	297	270	252	LFS-44-20
	25.0	19.0	12.5	1.9 × 4.75 × 16	480	392	371	342	LFS-45-20
	32.0	30.0	25.0	5 × 4.875 × 7.25	580	450	428	403	LFS-46-20
	40.0	38.0	34.0	5 × 4.875 × 8.875	680	560	478	450	LFS-47-20
	53.0	49.0	41.5	5 × 4.875 × 11	800	680	600	560	LFS-48-20
24V ±5% ADJ.	10.0	7.8	5.7	1.9 × 4.75 × 9.125	280	228	207	189	LFS-43-24
	13.0	10.0	7.5	1.9 × 4.75 × 11.75	360	297	270	252	LFS-44-24
	20.0	15.0	10.0	1.9 × 4.75 × 16	480	392	371	342	LFS-45-24
	27.0	25.0	21.0	5 × 4.875 × 7.25	580	450	428	403	LFS-46-24
	33.5	32.0	28.5	5 × 4.875 × 8.875	680	560	478	450	LFS-47-24
	44.5	40.5	35.0	5 × 4.875 × 11	800	680	600	560	LFS-48-24
28V ±5% ADJ.	8.6	6.8	5.0	1.9 × 4.75 × 9.125	280	228	207	189	LFS-43-28
	11.5	8.5	6.3	1.9 × 4.75 × 11.75	360	297	270	252	LFS-44-28
	17.5	13.0	8.5	1.9 × 4.75 × 16	480	392	371	342	LFS-45-28
	23.0	21.5	18.0	5 × 4.875 × 7.25	580	450	428	403	LFS-46-28
	29.0	27.5	24.5	5 × 4.875 × 8.875	680	560	478	450	LFS-47-28
	38.5	35.0	30.0	5 × 4.875 × 11	800	680	600	560	LFS-48-28
48V ±5% ADJ.	5.0	4.0	3.0	1.9 × 4.75 × 9.125	280	228	207	189	LFS-43-48
	6.5	5.0	3.8	1.9 × 4.75 × 11.75	360	297	270	252	LFS-44-48
	10.0	7.5	5.0	1.9 × 4.75 × 16	480	392	371	342	LFS-45-48
	13.5	12.5	10.5	5 × 4.875 × 7.25	580	450	428	403	LFS-46-48
	17.0	16.0	14.5	5 × 4.875 × 8.875	680	560	478	450	LFS-47-48
	22.5	20.5	17.5	5 × 4.875 × 11	800	680	600	560	LFS-48-48

LFS SERIES Specifications

DC OUTPUT
Voltage range shown in tables.

REGULATED VOLTAGE
regulation, line ....0.1% from 187 to 265 VAC;
0.1% from 95 to 132 VAC.
regulation, load ....0.1% from 0 to full load.
ripple and noise ....15mV RMS, 75mV p-p for 2V, 5V and 6V models.
20mV RMS, 150mV p-p for 12V through 28V models.
35mV RMS, 200mV p-p for 48V models.
remote programming resistance ....1000 Ω / V nominal.
remote programming voltage ....volt per volt.
temperature coefficient ....0.03% / °C

AC INPUT
(User selectable.)

line ....95 to 132 VAC / 187-265 VAC, 47-440 Hz

power ....LFS-43: 326 watts maximum.
LFS-44: 440 watts maximum.
LFS-45: 682 watts maximum.
LFS-46: 882 watts maximum.
LFS-47: 1103 watts maximum.
LFS-48: 1470 watts maximum.

RMS current ....5.7A RMS maximum on LFS-43.
7.5A RMS maximum on LFS-44.
12.0A RMS maximum on LFS-45.
15.0A RMS maximum on LFS-46.
18.0A RMS maximum on LFS-47.
25.0A RMS maximum on LFS-48.

Efficiency.................55% minimum on 2V models.
75% minimum on 5V through 15V models.
80% minimum on 20V through 48V models.

DC Input....................260 to 370 VDC.

OVERSHOOT
No overshoot at turn-on, turn-off or power failure.

AMBIENT OPERATING TEMPERATURE
Continuous duty 0° to 60°C with suitable derating above 40°C. Guaranteed turn-on at −10°C with reduced specifications.

OVERLOAD PROTECTION ELECTRICAL
External overload protection. Automatic electronic current limiting circuit limits the output current to a preset value, thereby providing protection for the load as well as the power supply.

HOLD UP TIME
2V, 5V and 6V models will remain within regulation limits for at least 16.7 msec after loss of AC power when operating at full load, Vo max and 105 VAC input at 60 Hz. (When configured at 220V input: 20 msec holdup when operating at maximum output power and 210 VAC input at 50 Hz.)

IN-RUSH CURRENT LIMITING
All models are provided with in-rush current limiting to limit the current to a preset value.

OVERVOLTAGE PROTECTION
Non-crowbar, inverter shutdown type OV protection is standard on all models.

COOLING
LFS-43, 44, 45 are convection cooled. LFS-46, 47, 48 are fan cooled.

DC OUTPUT CONTROLS
Simple screwdriver adjustment over entire voltage range.

INPUT AND OUTPUT CONNECTIONS
All input, sensing and remote on / off connections are made via PC board mounted terminal block. DC output connections are made via heavy duty bus bars. Ground connections are made via chassis stud.

MOUNTING
One mounting surface and one mounting position on LFS-43, 44, 45. One mounting surface, multiple mounting positions on LFS-46, 47, 48.

REMOTE TURN-ON / TURN-OFF
TTL compatible signal enables remote turn-on / turn-off of the power supply. A voltage of 2.8V to 5.0V applied to remote on / off terminals will initiate turn-off. Open circuit or short circuit condition, or a zero to 2.8V signal will cause turn-on.

REMOTE SENSING
Provision is made for remote sensing to eliminate the effects of power output lead resistance on DC regulation.

ISOLATION RATING
3750V RMS input to output, (8mm spacing). 1500V RMS input to ground. 500mV RMS output to ground.

PHYSICAL DATA

Package Model	Lb. Net	Lb. Ship	Size (In.)
LFS-43	3.00	4.00	1.9 x 4.75 x 9.125
LFS-44	3.50	4.50	1.9 x 4.75 x 11.75
LFS-45	6.00	7.00	1.9 x 4.75 x 16
LFS-46	8.75	11.75	5 x 4.875 x 7.25
LFS-47	9.20	12.20	5 x 4.875 x 8.875
LFS-48	12.30	15.30	5 x 4.875 x 11

FINISH
Grey, Fed. Std. 595, No. 26081

ACCESSORIES
LRA-17 Rack Adapter available. LRA-15 Rack Adapter also available on LFS-43, 46, 47, and 48 only. Cable system available on all models (consult factory).

GUARANTEED FOR 1 YEAR
One-year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of one year.

UL / CSA / VDE / IEC
Under evaluation.

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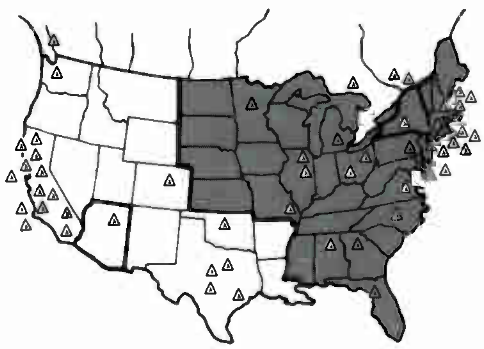

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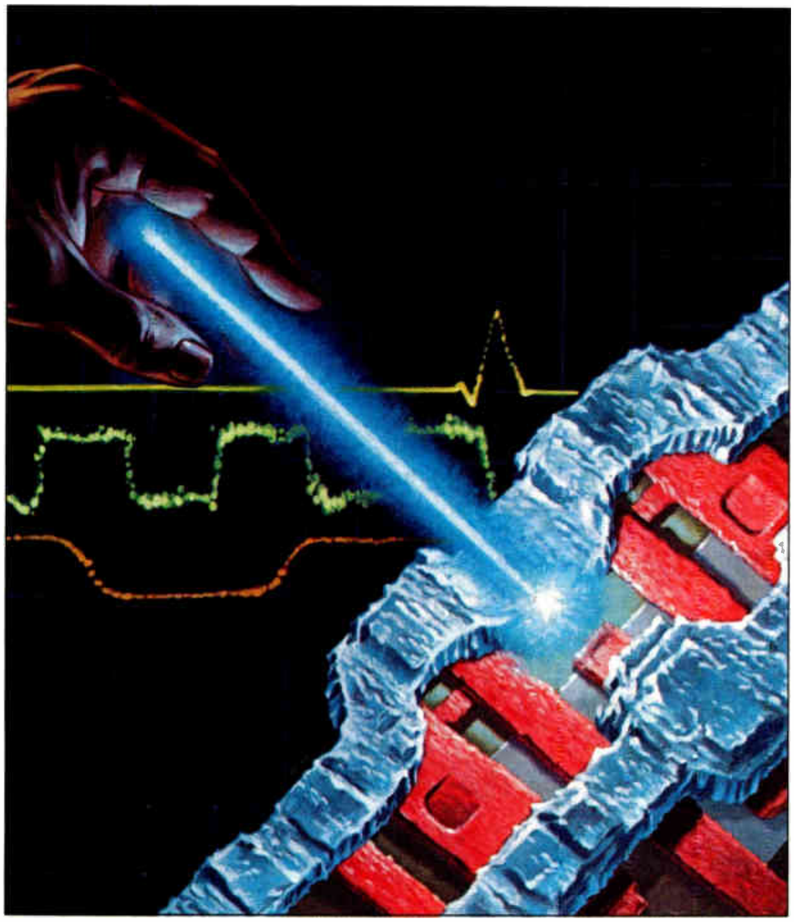
9/87

BUG ZAPPER.



The IDS 5000 integrates E-beam probing with CAD/CAE tools; it marries netlists, layout, and scope with a 'live' microscopic image of the chip.

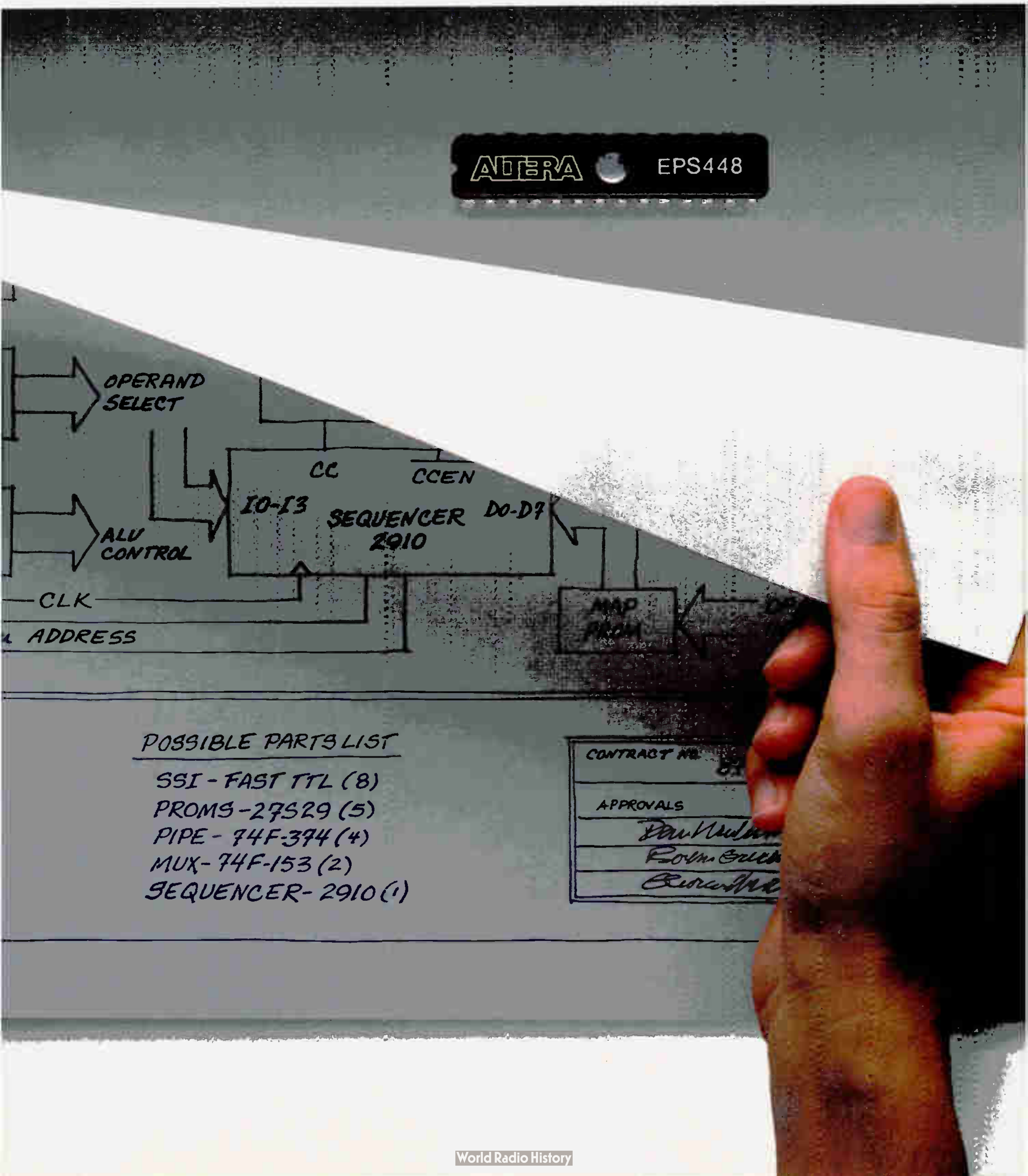
Sentry Schlumberger's New Tool Slashes VLSI Debugging Time.

"A new diagnostic tool promises to cut weeks off the time required to debug prototype VLSI devices that have submicron feature sizes. The Integrated Diagnosis System 5000 from Sentry Schlumberger Inc. of San Jose, Calif., uses an electron-beam probe and combines data from a complex VLSI chip's CAD netlist with an actual microscope image of the chip.

The IDS 5000 is the first debugging system to integrate front-end design data—netlists and connectivity—with back-end layout data—the physical chip layout. In addition, this system for the first time makes scanning-electron-microscope technology available to designers in an engineering lab..."

Excerpted from an exclusive article in the April 30, 1987 issue.

State of Mind.



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Our 54/74 AHCT advanced high-speed CMOS logic family gives you speeds and drives equivalent to, or better than, ALS, and can be used as direct plug-in replacements for ALS and FAST.™ In fact, 24mA drive is guaranteed for bus drivers.

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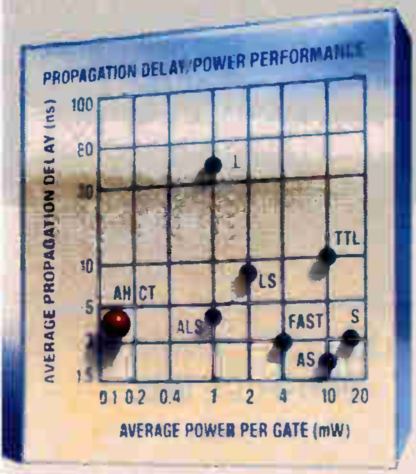

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Samsung's AHCT CMOS logic family, with 157 part types, has the most comprehensive selection of standard logic functions, so you can replace your ALS or FAST with our much lower-power CMOS part, right away.

And our 54/74 AHCT does not have a premium price tag. In fact, it costs the same as ALS. Which means you'll actually save money in your system cost because of lower power requirements and improved reliability.

Circle 67 on reader service card

CMOS LOGIC KS74AHCT Part Types

Gates and Inverters

00	20
01	21
02	22
03	27
04	30
05	32
08	51*
09	58*
10	86
11	132*
12	133*
14*	266

Buffers & Line Drivers

125*	367
126*	368
210	465*
240	466*
241	467*
244	468*
365	540
366	541

Flip-Flops

73	399*
74	534
76	564
78	574
107	670*
109	794*
112	821*
173*	822*
174	823*
175	824*
273	825*
374	826*
377*	

Latches

75*	793*
77*	841*
259	842*
373	843*
533	844*
563	845*
573	846*

Transceivers/Registered Transceivers

242*	643	652*
243*	645	658*
245	646	659*
640	648	664*
	651*	665*

Counters

160	190	590*
161	191	591*
162	192	592*
163	193	593*
168	390*	
169	393	

Decoders/Encoders

42*	148*	238
138	154*	239
139	155*	

Multivibrators

121*	123*	423*

Multiplexers

151	253*
153	257
157	258
158	352*
251	353

Shift Registers

164	299*
165	595*
166	596*
194	597*
195*	

Arithmetic Circuits

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518*	682*
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520*	686*
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Title: ______________________

Company: ______________________

Address: ______________________

City/State/Zip: ______________________

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Send coupon to: Samsung Semiconductor, CMOS Logic Marketing, 3725 N. First Street, San Jose, CA 95134-1708.

E 11/12/87

GATE ARRAYS' BIG PROBLEM: THEY TAKE TOO LONG TO BUILD

Four firms are now offering laser-based answers for fast prototyping to shorten their customers' product lead times; are instant custom circuits next?

by Bernard C. Cole

Time to market is always a bugaboo for makers of electronic systems, but the problem has been intensifying as product lifetimes have progressively shortened. And makers and users of semicustom chips feel the pressure even more because of the need to generate prototypes before a system can be debugged and demonstrated, much less marketed.

Now, relatively low-cost laser-based fast-turnaround prototype methodologies promise to solve this problem for gate arrays, putting prototypes in the hands of system designers in hours or even minutes so they can make sure their systems work and start demonstrating them to customers. They join direct-writing electron-beam systems—far more expensive at $5 million to $10 million apiece—in the business of producing gate-array prototypes fast.

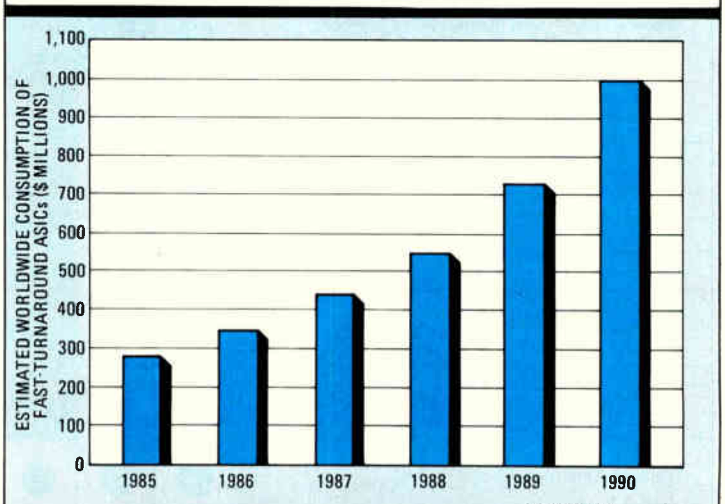
Such companies as Laserpath, Lasa, Elron, and Lasarray are developing very different laser-based technologies: lasers are being used, for example, both to cut prefabricated interconnect lines and to write them directly. They have equally varied approaches to the marketplace.

Laserpath Corp. of Sunnyvale, Calif., keeps its system in-house, where it offers quick-turn services to gate-array users. Lasa Industries Inc. of Santa Clara, Calif. (see p. 72), and Elron Electronic Industries Ltd., Haifa, Israel (see p. 76), sell complete turnkey systems. Lasarray Corp. of Irvine, Calif., and Bid, Switzerland, does both: it offers fabrication services and sells systems.

Besides gate-array manufacturers, other segments of the electronics industry should benefit from the new quick-turn technologies. Large original-equipment manufacturers will use them to shorten product lead times; computer makers should be particularly intrigued. Consumer- and military-electronics companies are likely prospects. And IC distributors may well see the new systems as a way of making deeper inroads into the semicustom business.

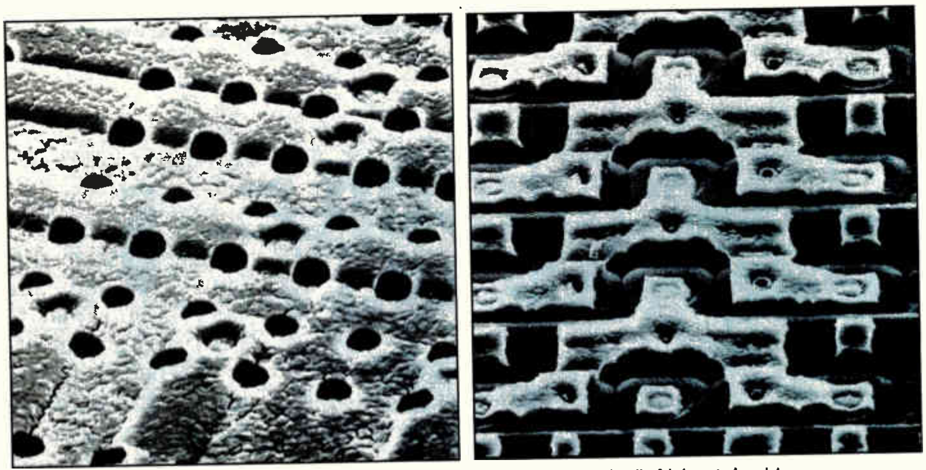
Because of its cost, e-beam technology is an option open to the only the largest OEMs and systems houses. E-beam is increasingly used at companies such as AT&T, Hewlett-Packard, Hitachi, and Philips, as well as some of the larger chip companies, such as Texas Instruments and Fairchild. But in most cases, their applications have been limited to customizing the photoresist,

STRONG GROWTH FOR FAST-TURNAROUND CHIPS



SOURCE: DATAQUEST INC.

Laserpath keeps secret the details of its technology, operating as a quick-turnaround service for customers who need prototypes in days. The company uses preprocessed and prepackaged 2- and 3-μm chips and claims a turnaround time of no more than seven days from netlist to first prototypes. Plans are under way to cut that to under three days for prototypes.



QUICK PATTERN. A layer of metal on a 2,400-gate Lasarray chip (left) is etched to form interconnect patterns (right) through a laser-based positive-resist exposure.

Laserpath's initial family of single- and double-layer-metal CMOS gate arrays ranges in density from 880 to 3,600 gates. They are customized using an yttrium-aluminum-garnet infrared laser that etches away metal traces on specially prepared dice using a "cut-point extraction" control program to identify points that must be cut. In a new generation of higher-density arrays ranging from 5,000 to 8,400 gates, the company uses a combination of laser etching plus a nonlaser fabrication technique.

Lasa and Elron are nearly ready to take the wraps off laser-fabrication systems that will be offered directly to customers as turnkey systems. But here the similarities end.

The $500,000 Elron system uses a direct-write laser micromachining technology in which specially prepared and prepackaged dice are customized by cutting interconnect lines at certain points. In addition to dice with some built-in special features, this approach requires that the CAD-based design be translated into a special "cut list" using an Elron-supplied program. Elron says the system can handle CMOS gate arrays with densities up to 50,000 gates. Initial offerings, however, will allow fabrication of arrays only up to about 2,500 to 5,000 gates.

The $3 million Lasa system, on the other hand, uses a laser to actually lay down the last two layers of metal interconnect on standard unmodified gate arrays that have been prepackaged. Capable of working with gate arrays with geometries as small as 1 μm, the Lasa system lays down either one or two layers of tungsten interconnect atop standard gate arrays, plus silicon dioxide dielectric between the tungsten layers.

According to Zvi Or-Bach, inventor of the Elron system, the first beneficiaries of laser-based gate-array metalization systems will be the manufacturers of gate arrays themselves. With costs of gate arrays dropping rapidly, a major point of differentiation among vendors will be their ability to deliver finished prototypes faster.

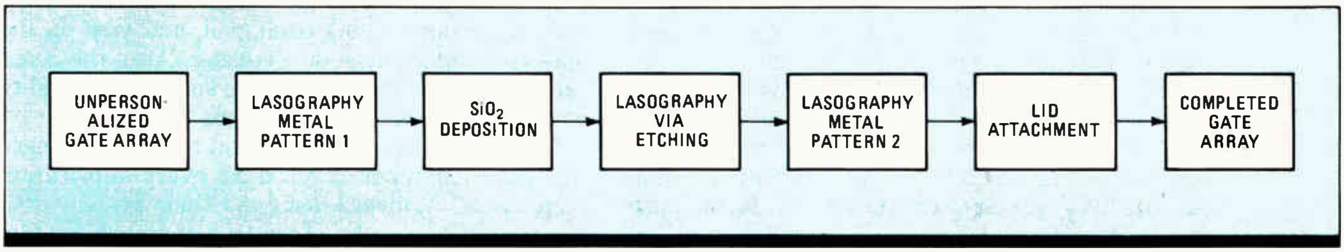
Also at the head of the user line will be large OEMs, says Dan Dooley, president of Lasa. "Some of these companies are spending as much as $25 million a year in nonrecurring engineering costs just to get those first 10 or 20 prototypes," he says. Besides giving such OEMs a lower-cost way of generating high-density prototypes, says Dooley, the new systems will slash the time it takes to get products to market. Even more important, he says, is that such quick-turn systems bring more of the design and fabrication process back under the control of the users.

Large and small computer makers will also jump on the bandwagon, Dooley predicts. "No matter whether it is a supermini or a personal computer," he says, "the designers need to know as quickly as possible in the system-development cycle whether a chip works and if not, why."

Laser-fabrication systems could open up new possibilities for gate arrays in the consumer market, too. "In such areas as electronic games and toys, semicustom gate arrays are not used because of the high nonrecurring engineering costs involved," Dooley says. "These guys need prototype systems that they can take around to customers and to shows, to see what the response is."

Yet another significant potential market is the military. "In the military, the need is critical for a quick and efficient way of turning out a lot of different designs quickly, but in relatively small quantities," says Or-Bach of Elron. The new systems also enhance security: "Everything can be done in one room—design with a standard CAD system, fabrication with the system, and testing," says Dooley. "The data tapes are secured and nothing has to come out of the room except the final parts."

Dooley also expects systems such as Lasa's to have an effect on the distribution business, which has been having a hard time adapting to semicustom technologies. "In addition to their traditional roles as the middlemen in the standard-IC business, many IC distributors have been active in setting up their own design centers to take advantage of the semicustom business," he says. They already make CAD tools available and take a fee on that; now distributors will be able to produce and sell prototypes. □



2. STAGES. Uncommitted gate arrays in open-top packages are loaded into the QT-GA system for metal and oxide deposition.

ASIC; three miniaturized chambers for metalization, oxide deposition, and packaging; and a robotic system for moving the packaged circuit from chamber to chamber. Above the table is a bay containing a distributed microprocessor system, random-access memory, and tape drive for overseeing the operation.

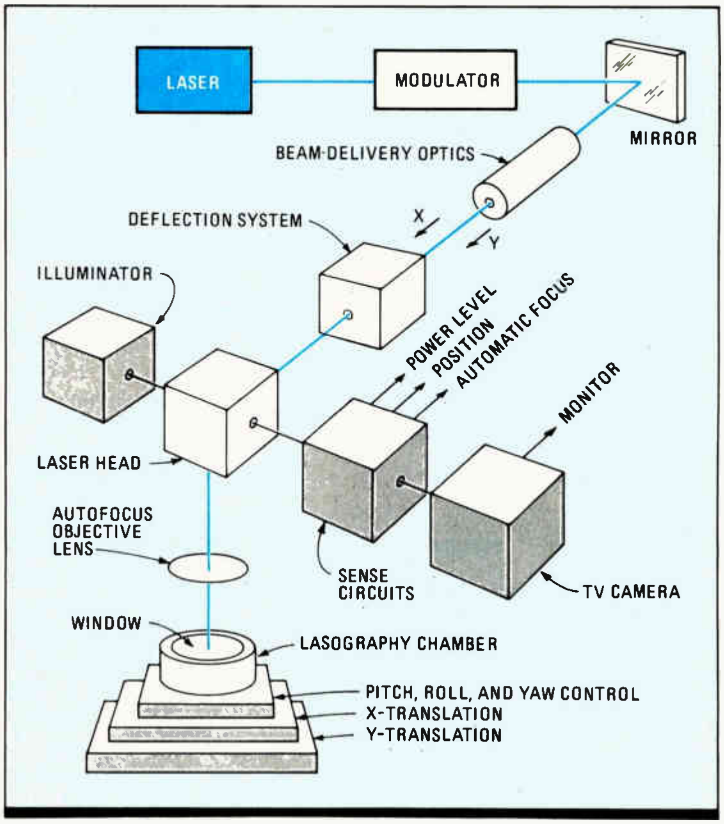
Achieving this combination of high throughput, ease of use, and compactness took Lasa almost two years and a number of design and process breakthroughs, says Dooley. New solutions had to be found in laser-beam control, robotics, image recognition, and low-temperature processing. Lasa engineers also had to tinker with process-equipment design, packaging and handling, and hardware and software control.

In the Lasa system, the fabrication process (see fig. 2) starts with uncommitted gate-array base wafers that have been taken through the aluminum metalization stage by conventional techniques. Metalization patterns defining uncommitted bond pads have been laid down and metal is left in the device contact areas, but otherwise the array remains uncommitted, explains Dooley. After evaluation of the wafer test pattern for device characteristics, the wafer is sawed, the dice are separated, optically inspected, and then mounted and wire-bonded in specially designed packages. These open-topped packages are then loaded into a carrier of proprietary design, which can hold up to 12 such parcels, and sealed in a nitrogen-purged plastic bag for delivery to the user.

On location at the user facility, all the circuit designer needs to do is take a design he has worked out on a standard CAD work station and load the design-topology data into the QT-GA in the form of a GDS-II formatted output on a magnetic tape cassette. There it is reformatted. An operator breaks open the sealed bag, inserts the uncommitted gate arrays into the cassette, and initiates action by pushing the appropriate location on a menu-driven, touch-activated screen.

"After the tape is loaded, all the operator has to do is tell the system how many parts are needed," says Dooley. The QT-GA then proceeds to direct-write the metal interconnects on each of the dice sequentially to create the appropriate design. The QT-GA handles the entire process under computer control. Its robotic system sends the gate arrays through the metalization chamber and into the final assembly area, where a ceramic lid seals the packages. Finally, the system delivers completed units at an output cassette location, all packaged and ready to test. No mask tooling or photolithography is involved. If the design is to be reused, the reformatted data will be stored on a 50-Mbyte disk drive.

Lasa's additive interconnection approach, in which metal lines are laid down by the laser, is opposed to the subtractive techniques of competitors Laserpath, Lasarray, and Elron in their own efforts to find a quick-turnaround way of fabricating gate arrays (see p. 69). In Dooley's opinion, the disconnect, or subtractive, approach is a dead end. "For one thing, the disconnect approach, in which the laser is used to cut the metal, causes a great deal of damage to the underlying silicon substrate if not done carefully," he says. "This places considerable restraint on throughput, especially at higher densities, and on yield, since there is a greater probability of damage as the number of cuts increases." And since the disconnect approach is precisely



3. OPTICS. Upping intensity of a focused 1-μm-diameter beam from an argon-ion laser raises local temperature wherever an interconnection is required.

HOW A WORRY TURNED INTO A COMPANY

In 1984, National Semiconductor Corp. made a financial decision that worried Dan Dooley, who was then a vice president and group manager at the company. "I had just come out of a management technology meeting where we had made a commitment to invest in excess of $100 million in a state-of-the-art fabrication facility for VLSI circuits," says the man who founded Lasa Corp. last year. "I was aghast. What we were talking about was an investment comparable to that needed to build a steel mill. I asked myself: 'How can we possibly expect to get a return on that kind of investment?' "

The answer he formulated to that question—"with great difficulty"—led to other questions. These, in turn, spawned an idea that ultimately became the basis for Lasa, the San Jose, Calif., company that Dooley founded with Leslie Burns, the founder of Xidex Corp. and former president of Burns Research.

The idea behind Lasa is that a market exists for a less expensive, less time-consuming fabrication technology, one that can be used for much smaller orders than would be practical at the $100 million facility National Semiconductor was planning. "The only way such [huge] investments pay off is with volume production in the hundreds of millions of units," Dooley says.

But such high-volume markets are getting scarce. The trend, in fact, is toward higher levels of integration, which implies ever more system- and application-specific circuits. That means fabricating fewer, not more, chips, with the average number of units per circuit type in the tens of thousands at best.

"I felt there had to be a fabrication technology or methodology that could impact this capital intensity," Dooley says. He saw particular potential in the fabrication of prototypes, whether for standard circuits, custom or semicustom designs, or gate arrays.

In all cases, he says, the problem is the same—generating working ICs quickly for testing and for evaluation in actual systems. The turnaround time is anywhere from six months to a year for standard circuit design, six to eight months for a custom design, and two to six months for a semicustom design. "And what happens if you get the circuit and it doesn't work in your design?" he asks. "You have two choices: either start all over again, or abandon the project."

DOOLEY: He figured there had to be a better way than $100 million fab facilities.

To find a way to create a system that can allow the fabrication of chips in hours or days, rather than in months, Dooley drew on the 10 years he spent as vice president of engineering at Precision Monolithics Inc., a Santa Clara, Calif., manufacturer of linear ICs. His work there with the laser trimming of linear ICs convinced Dooley that what he calls "lasography" was the key.

But Dooley decided against exploring the traditional approaches to laser use, in which a laser beam blows fuses and cuts interconnects. He felt that an additive, not a subtractive, technique was the ticket. There are problems with subtractive methods, he says: "Using lasers as a micromachining tool to cut patterns is inherently lower yielding, harder to control, and requires considerable expertise to operate."

Dooley mentioned the idea of an additive technique to Burns, a longtime friend. Burns's response, as Dooley recalls, was, "Funny you should mention that. I think there is a way."

The two put their heads together and came up with the idea of using the laser as an additive tool—one that would be used for laying down interconnect, rather than for cutting it. Ultimately, their brainstorm resulted in Lasa's new QT-GA (for quick-turn gate array), a laser-based chip-fabrication system (see p. 72).

With initial funding from Peter Sprague, chairman of the board of National Semiconductor, Dooley and Burns formed Lasa to build and sell QT-GA. Sprague's money was a personal investment; there is no official connection between Lasa and National. In the past year, the company has attracted about $12 million in additional funding in equity from a variety of private investors, mostly European.

Dooley views the QT-GA as the first member of a family of flexible manufacturing systems that are the antithesis of the rigid and increasingly costly semiconductor equipment now in wide use. While initial QT-GA sales will be to chipmakers, who are currently using the older, slower process, Dooley's long-term goal is to provide full-custom manufacturing capability directly to the users of standard, semicustom, and custom circuits.

The QT-GA system is in the beta-site stage now, being tested by semiconductor chipmakers. The company expects to be taking orders and delivering systems by the first quarter of 1988. A complete QT-GA system is expected to sell for $3 million. *-B.C.C* have a density range from 1,200 to 35,000 available gates, half that of the mask-programmable versions. "When the Elron micromachining laser technique is used with more traditional channeled arrays with predefined routing channels, densities are about 80% to 95% of a conventional finished array," Or-Bach says—and that's close to what mask programming can achieve. A second company with which Elron is working to develop specially modified arrays is Seiko. The family will be based on Seiko's SI6000, a 2-μm 6,000-gate channeled array, of which 5,500 to 5,900 will be available in the laser-based versions.

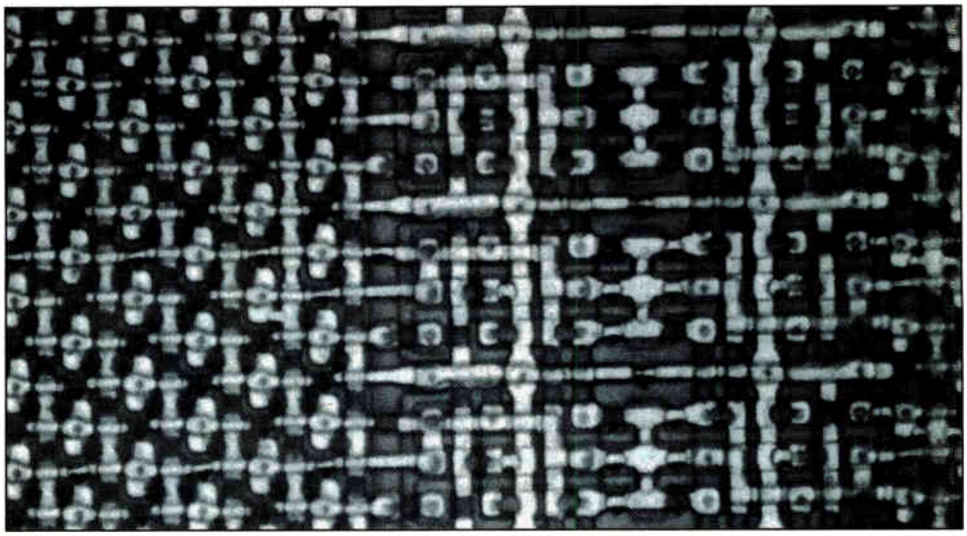
Unlike the Lasa approach (see p. 72), which uses standard blank gate arrays, the Elron laser micromachining technique can be used only with base arrays that have been modified by the circuit manufacturers in four key areas: input/output cells, the core logic array, the core routing, and the core interface with the I/O cells. In addition, the vendor must set aside a special calibration region on the die to calibrate the power of the laser. To design a circuit using the Quick system, the designer must also reconfigure his layout program using special software consisting of macrocells and a place-and-route routine supplied by Elron. This software reflects the modifications made to the base array.

In the VTI array, for example, the metalization of the I/O region was defined so that mask programmability was retained; each I/O location can be programmed as an input buffer, output buffer, I/O buffer, V_{dd}, or V_{ss}. In addition, care was taken to retain a pull-up resistor in each I/O cell to allow the output drive to be programmed to 2, 4, 8, or 12 mA.

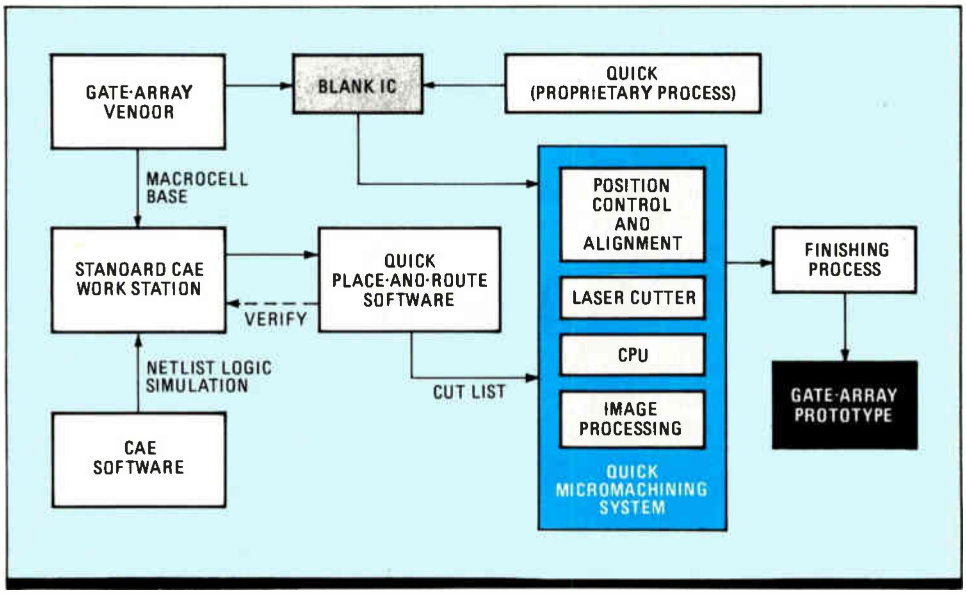
In the core area, the metalization was modified so that the Elron technique could be used in the interconnect scheme used in VLSI Technology's continuous-gate-array architecture, says Or-Bach. Unlike other channel-free schemes, in which the first- and second-level metals run in the same direction, the VTI approach runs the first layer of metal horizontally and the second layer vertically.

In order to increase the yield of good dice, modifications that Elron won't discuss also must be made in the core routing. In the case of the VTI continuous-gate-array architecture, this was particularly important since the company's parts include no predefined routing channels as do ordinary gate arrays. Instead, inter- and intramacrocell connections coexist in the same regions, with routing running over the top of active macrocells. To build a laser-programmable macrocell with this architecture, it was necessary to use up more area than with a conventional channeled gate array in the macrocell metal definition, says Or-Bach. The laser-written array ends up like a conventional array with alternating rows of macrocells and routing channels to connect macrocell wiring.

In the core-to-I/O-cell interface, additional modifications were made in order to bring all the



2. PERSONALIZED. Using a laser micromachining technique, a 2-μm, double-level metal, 2,500-gate CMOS array can be personalized by cutting interconnect in a predetermined pattern.



3. CUTTING. From a verified netlist, a data base is derived and modified by Elron software to produce laser cutting instructions.

Keep telling yourself
it's only a game.
it's only a game.
it's only a game.
it's only a game.
it's only a game.
it's only a game.
it's only a game.
it's only a game.
it's only a game.

(Or is it?)

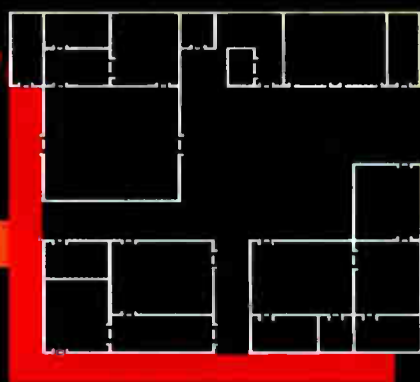


Diagram of Cramoisy Brigade camp. You'll need this to complete your mission.

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SECOND-GENERATION CLIPPER HITS A RECORD 50 MHz

The latest version of the RISC processor builds on the original architecture but uses finer line geometry and improved circuit design to boost performance

by Stan Runyon

The computing power that users increasingly are demanding for applications ranging from high-quality graphics to networking is coming. The 50-MHz, 32-bit Clipper C300 packs more power into a single three-chip module than any of today's microprocessors stuff onto a single chip.

One reason for the Clipper's speed is its use of a Harvard architecture, which separates data and instruction streams, plus the inclusion of on-chip data and instruction caches, memory management, and a floating-point unit. However, the latest 32-bit contenders are closing in on Clipper. The Motorola 68030 and the National Semiconductor NS32532 contain all of those features but the FPU. Even so, the new Clipper 300 boasts the highest clock speed of all—50 MHz, compared with 30 MHz for the 532 and 20 MHz for the 68030 (with samples of a 25-MHz version due next month).

The C300 emerges just as Intergraph Corp. has finished taking over the Clipper operation from National Semiconductor Corp. (see p. 88). National sold the former Fairchild Advanced Processor Division because it felt it could not support two 32-bit-processor efforts.

The new Clipper gets its punch by building on the reduced-instruction-set architecture used for its predecessor, the C100. That architecture has been refined for higher performance. At the same time, compatibility was maintained between the two Clippers, so the new processor has the same range of software as its predecessor, with several compilers available and more coming. Key Clipper concepts, such as its cache memory scheme, are retained, but the C300 boasts finer line geometries and improved circuit design. The new Clipper also adds some new features, such as a new generator controlling the clock for the central processing unit, floating-point unit, and the two memory-management units. Tying the whole package together is an implementation of the Unix operating system.

The engineers at APD say that with the C300, the capabilities that until now were found only in sophisticated work stations can be built into a relatively inexpensive system that consumes a moderate amount of power and fits comfortably on a desktop. In the past, the circuitry to build such an engine required an entire board or even two. But with the latest silicon design rules and

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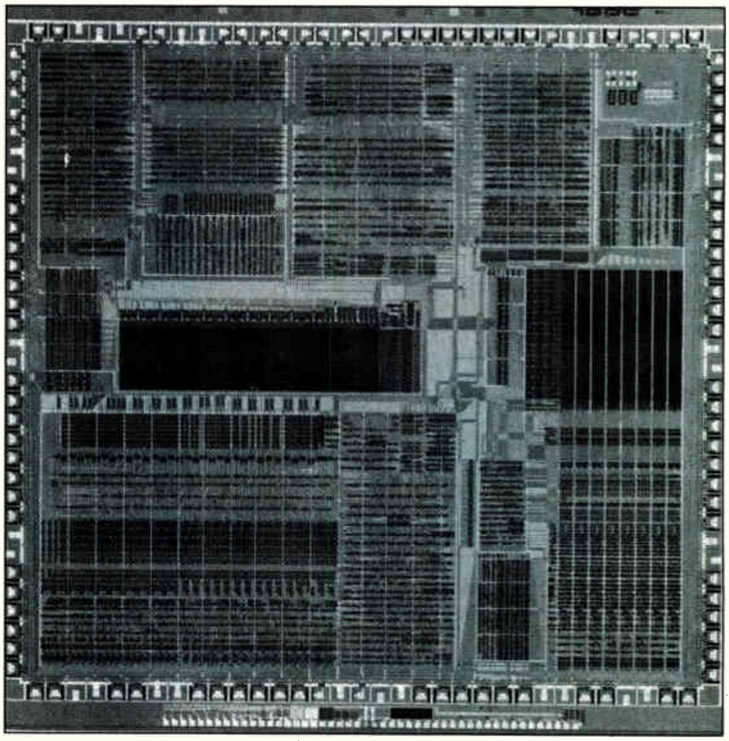


1. FAST CHIP. The 50-MHz Clipper's CPU builds personal computers that fit on desktops but have the power of work stations.

units. Running at an input frequency of 100 MHz, the clock generator also provides all system clocks and synchronizes multiprocessing applications. The input frequency is divided into individual 25-MHz and 50-MHz clocks to run the compute engine and other circuits.

Although clock speed is an important factor in determining effective system speed and instruction execution time, speed alone does not tell the full performance story; clock phases are just as important. For example, some 32-bit machines need not only a high-frequency clock but a multiple-phase one as well. Such a scheme can lead to control and skew problems, especially when interfacing to static RAMcache subsystems. A better method is the technique proven in supercomputers: a simple, single-phase, high-speed clock. Such a clock is easier to control and it delivers the same number of working edges as a multiple-phase clock.

The Clipper 300, like its predecessor, runs an implementation of Unix System V, release 3, called Clix. In the C300's implementation of Clix, extensive use is made of the engine's copy-back caching and overlapped virtual-memory mechanisms. For example, read, write, and execute access protection is enforced on a per-page basis, along with three different caching strategies—non-caching, write-through, and copy-back.

The C300's Clix operating system works in a distributed I/O system with an I/O processor. I/O drivers are provided to run the processor and pass messages to the main Clipper-hosted kernel. A distributed-line discipline can be implemented to increase terminal handling capability. □

For more information, circle 482 on the reader service card.

HOW TO MEASURE A PROCESSOR'S PERFORMANCE IN THE REAL WORLD

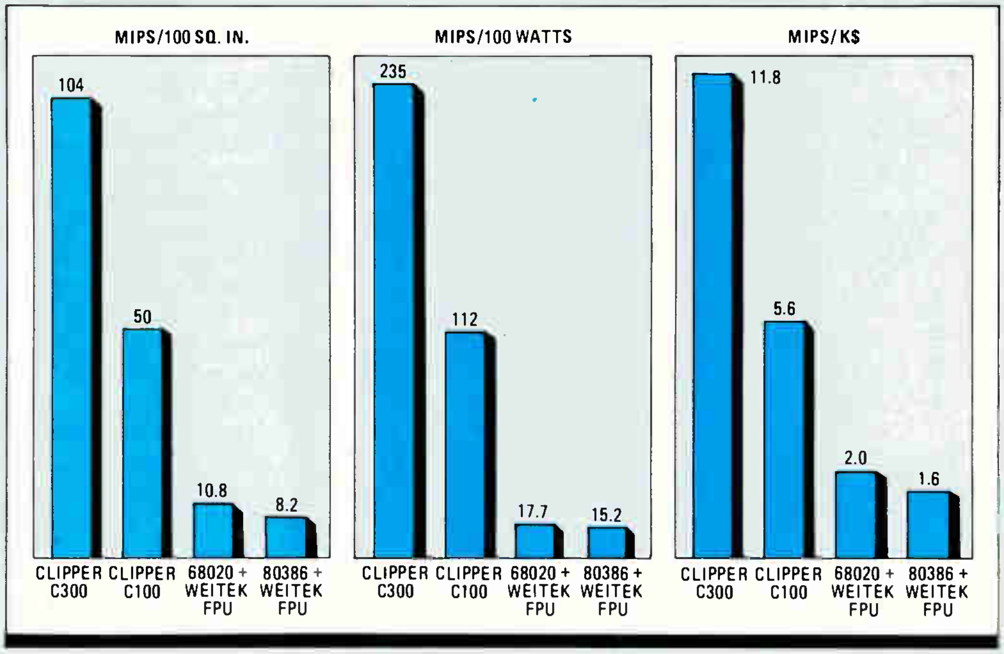
Most users of desktop computers are on the lookout for machines that offer more performance, but that desire must be tempered by the realities of a system's cost, size, power consumption, cooling requirements, and other factors. So the goal of computer makers is to design machines that deliver the high performance and still fit a user's budget, operating environment, and desk space. Figuring out the performance of any given system while taking into account all of these variables is hard to do. The Advanced Processor Division of Intergraph Corp. thinks it has come up with a way, using what it calls mips density.

Used alone, mips, or millions of instructions per second, provide only a rough measure of power. A better criterion is VAX mips, with a Digital Equipment Corp. VAX serving as the standard for comparison. The comparison is somewhat more precise in that case, since it provides a constant to measure against. But VAX mips still only measure sheer speed.

Mips density is a far more precise gauge than either raw mips or VAX mips. It accounts for performance, or efficiency, with respect to physical size, power consumption, and cost. The accompanying figure compares the mips-density performance of four 32-bit processors: the 33-MHz Clipper C100, the 50-MHz Clipper C300, the 25-MHz Motorola 68020, and the 20-MHz Intel 80386.

The first panel of the figure shows mips performance as a function of circuit-board area. Obviously, the more computing power compressed into a given area, the more dense the machine. With the C300 module occupying just 12 square inches of board area, it delivers considerably more computing power than competing processors, which require more board area to accomplish the same functions. The size of the compute engine is critical because it affects the number of boards in the system. Too many boards devoted to the processor means fewer expansion slots in the machine.

The C300 also provides about 13 times more processing power than a 68020 (second panel) for every watt of power consumed by the system processor. Excessive power dissipation can drastically alter a system's potential location in an office, its reliability, or its cooling requirements. Finally, the C300 outdoes its competitors at the basic level of cost. It is more cost-effective than the other computation engines by six times or more.



INTERGRAPH WILL HAWK CLIPPER TO ALL COMERS

The company chose the chip because of its blazing speed—now it hopes that same speed can win the RISC processor a place in the designs for other high-end systems

by Lawrence Curran

The question on everyone's mind when Intergraph Corp. bought the Clipper 32-bit microprocessor from National Semiconductor Corp. was whether the Huntsville, Ala., company was buying it to sell on the market. Its motive could have been to protect its supply of the powerful 32-bit processor around which it has designed its new generation of work stations—and other Clipper users could take a back seat. But, says Jim Meadlock, Intergraph chairman and president, his company is committed to making the Clipper succeed in the global market, as well as using the processor in its interactive graphics and mapping systems.

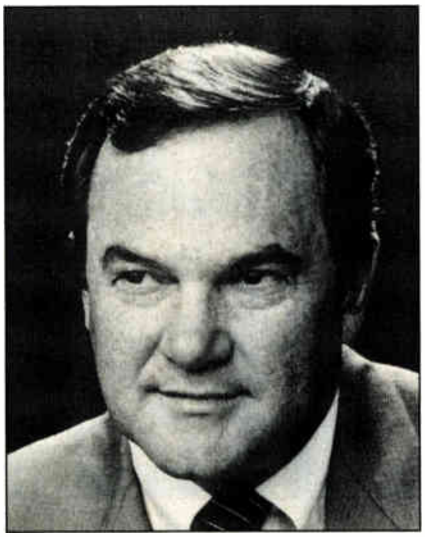
After joining in an unsuccessful buyout bid for Fairchild, Intergraph decided to take under its corporate wing—for just under $10 million—the Advanced Processor Division that spawned the Clipper [*Electronics*, Oct. 1, 1987, p. 36]. Clipper is the core processor in Intergraph's high-speed InterPro and InterAct design work stations and the InterView mapping work station family.

APD now becomes a division that must compete for system design wins for the Clipper. But where Intel's 80386 and Motorola's 680000 are more suitable for low-end to mid-range work stations, Intergraph is counting on the Harvard architecture and high-speed reduced-instruction-set-computer design of the Clipper C300 (see p. 85) to give it the appeal for high-end graphics systems and other applications that made its predecessor, the C100, Intergraph's choice in the first place.

That choice was made more than two years ago, when Intergraph was looking for microprocessor performance suitable for its high-end work stations, which are used in mechanical computer-aided design and cartography applications. Meadlock says that no other microprocessor could approach the Clipper C100's 5 million instructions per second: "It was the premier microprocessor in development at that time," he says.

The platforms in which the C100 is used, along with the Digital Equipment Corp. VAX- and MicroVAX II-based hosts to which they can be connected, have made Intergraph the world's second-largest vendor of mechanical CAD and mapping applications, behind IBM Corp. The company cracked the *Fortune* 500 for the first time in 1986 with revenues of $605 million. Intergraph is looking to the electrical CAD market to fuel additional growth, although Meadlock expects 1987 revenues to be about the same as last year's.

The company has slipped a point in worldwide



JIM MEADLOCK: Intergraph plans to continue to sell the Clipper on the open market.

systems being added each month. "That's the market we're after and we think we can persuade from 2% to 3% of the 140,000 users and 10,000 newcomers per month to convert to a Clipper processor," Seng says. "We are aiming at 3,000 to 4,000 installations a year."

So far, Spea has the European market to itself. It's the only company selling Clipper-based equipment, although a few others have started experimenting with the Intergraph processor. To better exploit its position, Spea is considering setting up before the end of this year a subsidiary in the U. S., "the world's most important market," as Seng sees it.

It already has software available for a U. S. push. For example, one of the American market's most important CAD software packages, Autocad from Autodesk Inc. of Sausalito, Calif., has been ported by Spea to the Clipper board. The latest version of Autocad, announced early this month, is expected to run six to eight times faster on a Clipper-based machine than on one using the Intel 386.

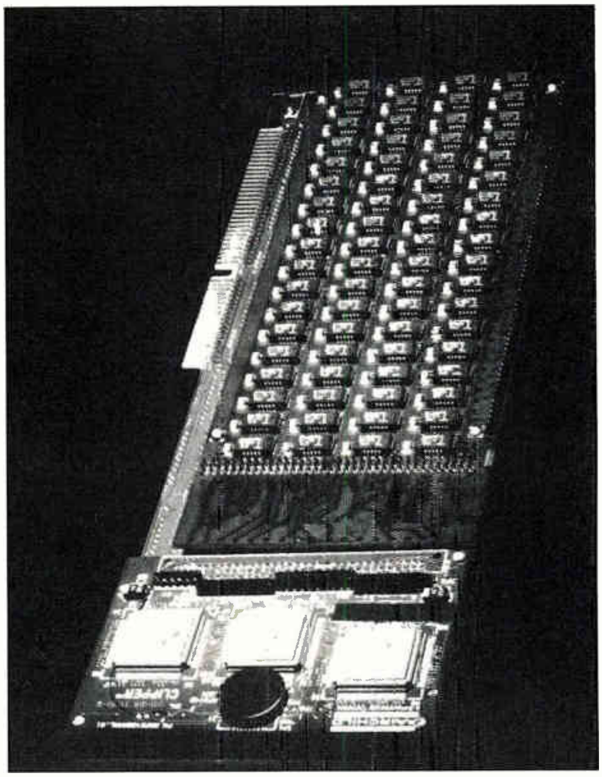
And based on its past performance, Spea could reap sizable rewards in the U. S. Founded in January 1986, Spea originally developed and sold graphics controllers, 32-bit Unix cards, and computer-aided-engineering software. It was not until this summer that it branched out into selling Clipper-based boards for upgrading personal computers to work stations. Business boomed, with sales hitting about $560,000 a month, up from $110,000 for the entire first half of 1987. They should reach $780,000 a month toward the end of this year, Seng figures.

Actually, success came a bit late to Spea, Seng says. The company's sales curve could have started its steep upward climb a few months earlier, if Fairchild had been able to deliver the Clipper processors as originally scheduled. Also, when the first 25-MHz versions finally became available last summer, the Starnberg company had to eliminate a few bugs, mainly compiler and assembler errors, from the devices. "We are now happy with the product," Seng says.

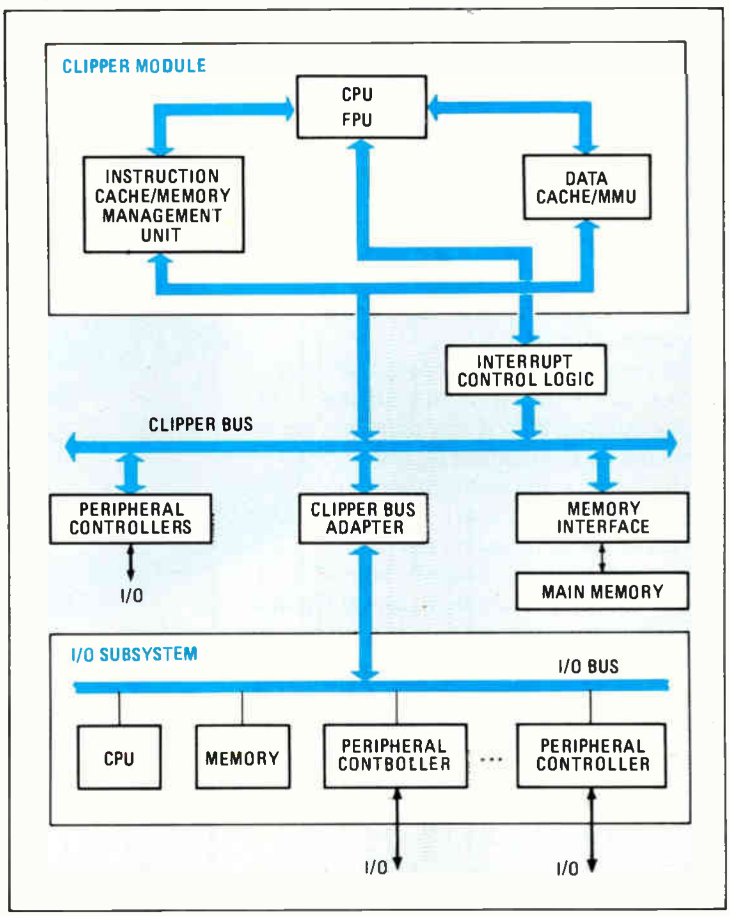
Problems also delayed the introduction of boards and systems using the Clipper's 33-MHz version. These were initially plagued by the development of excessive heat, a problem Spea has meanwhile solved by proper equipment cooling. "So it's we who have helped make the Clipper error-free and start a market for it in Europe," Seng says. Boards and systems using the 33-MHz version will be available early next year.

For continued success, Spea is banking on steady deliveries of the Clipper, now that Intergraph Corp. in Huntsville, Ala., has bought the Fairchild Semiconductor Corp. division that developed the processor. And as for the latest Clipper, the C300, Seng says he can hardly wait. He hopes to become the first company to offer 300-based boards. □

For more information, circle 484 on the reader service card.



SCREAMER. Intergraph's Clipper lets Spea build a powerful one-card accelerator that turns PC ATs into 5- to 8-mips machines.



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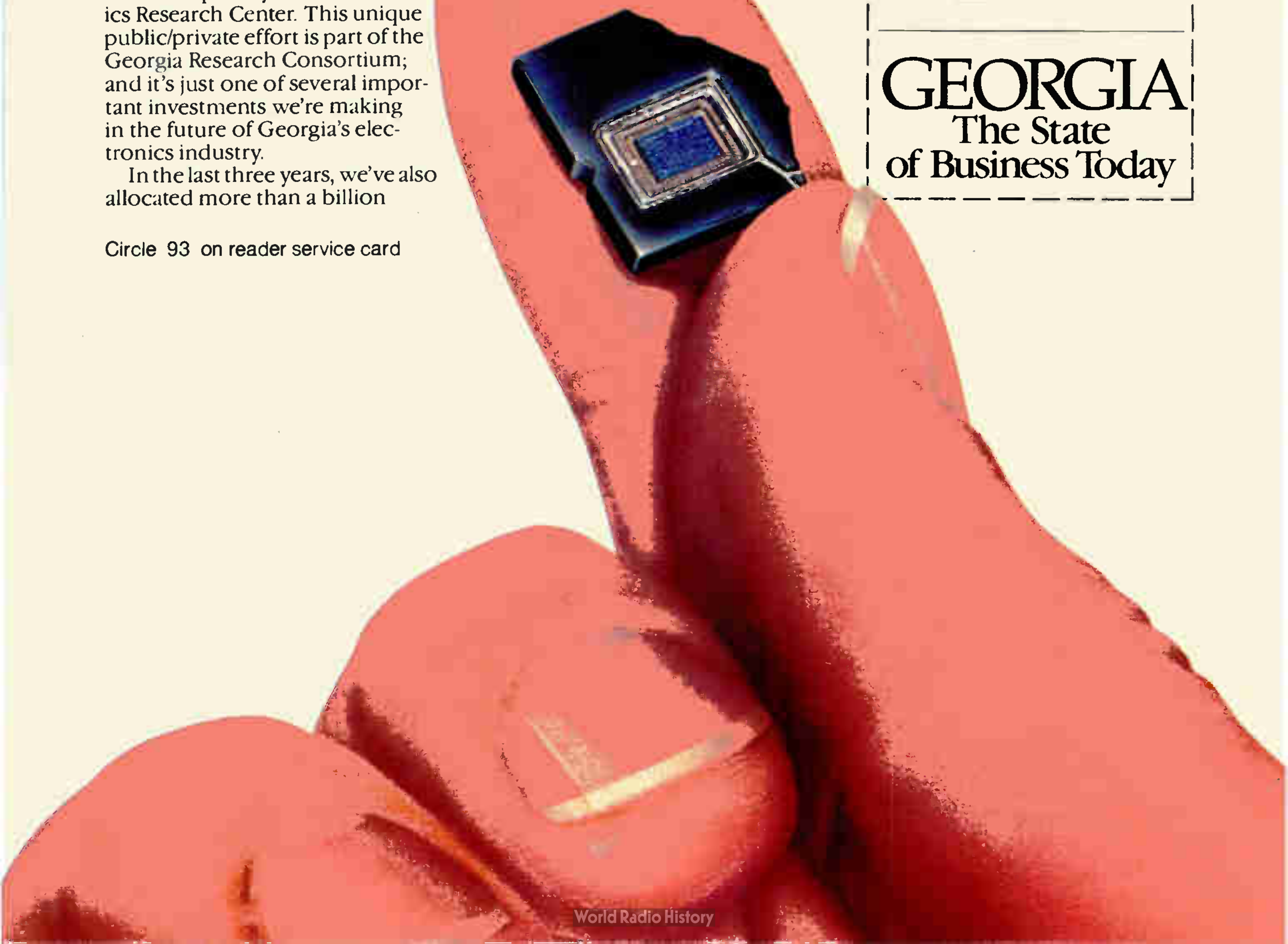

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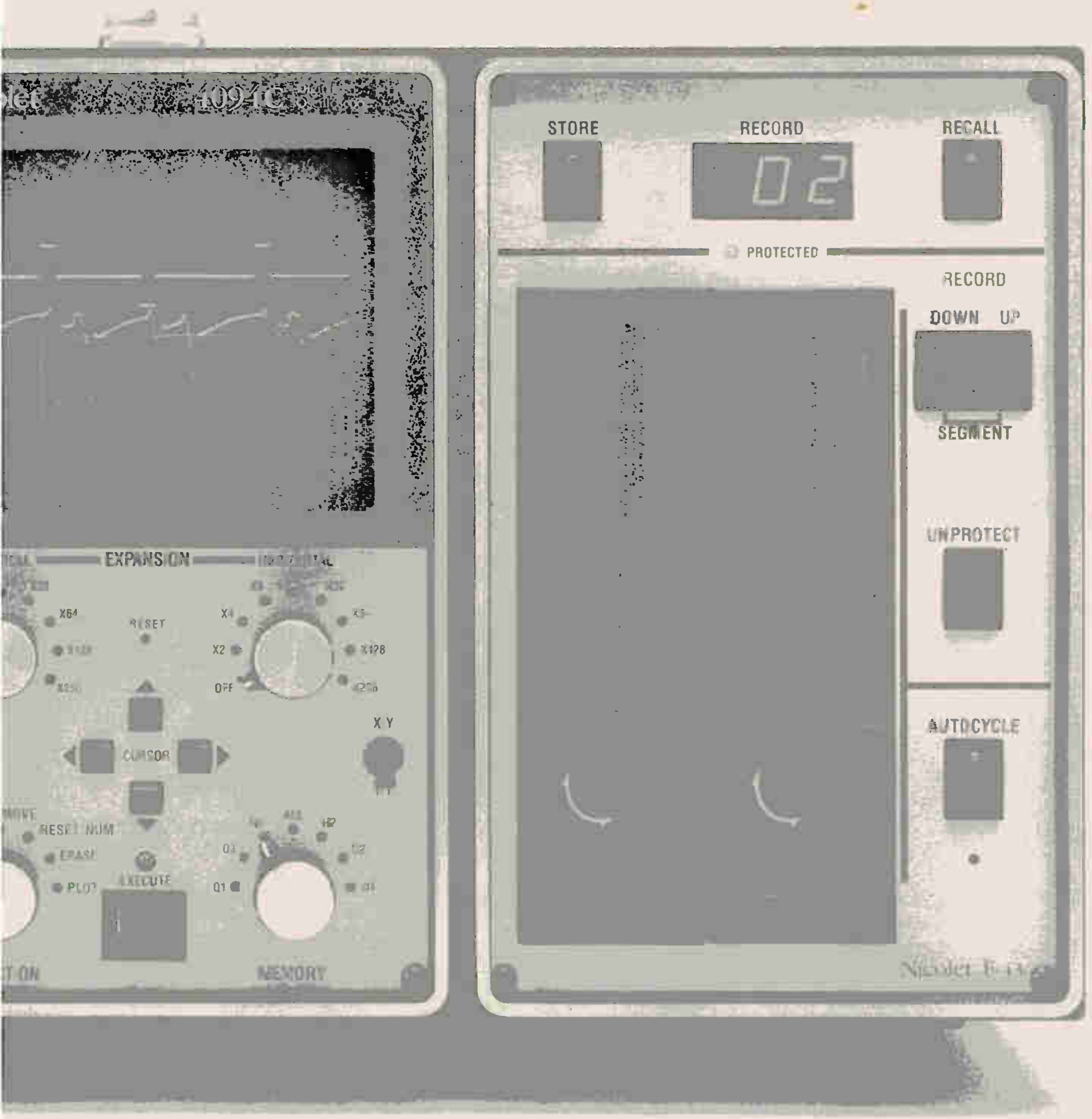

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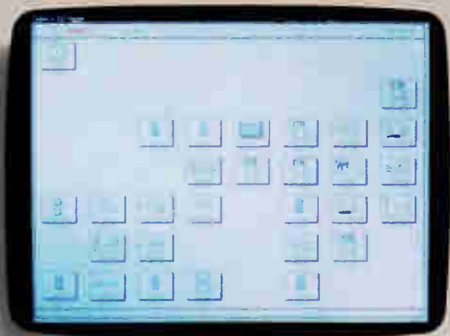

Emerging technologies demand a new set of design solutions. Advances in ASICs, high-frequency components and fine-line design are creating new challenges in engineering, design and manufacturing. A new level of CAE/CAD/CAM sophistication is required to get the job done, and stay competitive. Companies must have even tighter integration between engineering, design and manufacturing, plus open access to all the equipment that's needed to produce a product quickly.

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68000™ FAMILY UPDATE NO. 3

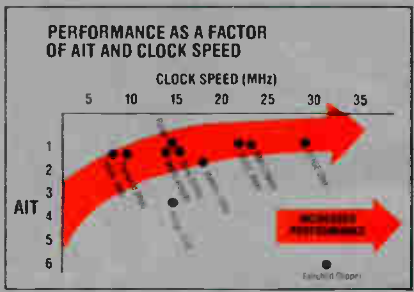
NOVEMBER, 1987

"CISC VS. RISC" DEBATE IGNORES KEY ISSUES OF SYSTEM SOFTWARE AND ON-GOING SUPPORT COSTS

The continuing debate over whether CISC or RISC technology is the answer to boosting computer performance levels tends to focus on machine speed, often ignoring an equally important issue: architectural compatibility. Computer manufacturer's with 68000-based CISC architectures considering a move to RISC technology for their high-end product offering need to recognize the enormous costs they face. Current systems software must be adapted and supported on different architectures. Two different operating systems as well as diagnostics have to be ported and supported. Compilers for high level languages need to be developed. And these are just a few of the obstacles.

The EDGE 2000 Series VME board set recently introduced by Edge Computer proves that a 68000-compatible CISC system can operate with RISC-like efficiency. But performance is only one side of the coin. Value and the ability to leverage your investment in existing 68000-based software are equally important. By driving costs to approximately $1K per MIPS in OEM quantities, while maintaining 68000-compatibility, Edge makes CISC a more attractive option than other implementations of CISC or RISC. 68000-based manufacturers can stay with CISC and forego a sizeable portion of software porting costs, as well as the on-going expense of supporting and maintaining two different architectures.

In the industry's continuing quest for improved machine performance, Edge has set the pace by achieving faster clock speeds and reducing cycles per instruction. At 1.4 cycles per instruction, the EDGE 2000's AIT (Average Instruction Time) is already lower than most products on the market today.



Nonetheless, the CISC RISC debate will continue. But for 68000-based manufacturers faced with the need to expand their product lines and bring high-performance 68000-compatible products to market economically and on time, the EDGE 2000 is a clear winner.

SYMETRIX UNITES PICK, UNIX V.2 OTHER OPERATING SYSTEMS TO FOLLOW

Edge Computer now offers SYMETRIX*, a concurrent operating system environment, on its line of high performance computer systems.

SYMETRIX provides an architecture that allows multiple standard operating systems to operate at the same time on the same system.

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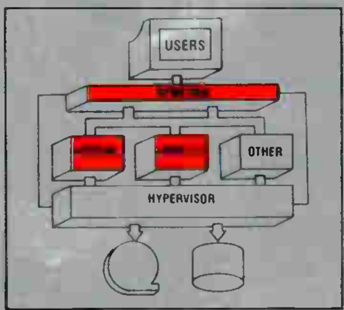

SYMETRIX provides a seamless, menu-driven PICK/UNIX interface that allows transparent access to PICK and UNIX. The end-user literally never need know which operating system is being used.

SYMETRIX is undergoing further enhancements that will allow transparent interfacing of as many as three, four or more popular operating systems.

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Circle 98 on reader service card

MOTOROLA'S ARRAYS HIT A NEW HIGH: 80% GATE UTILIZATION

They do it with triple-metal CMOS and flexible power-bus routing

by J. Robert Lineback

Three levels of metal interconnection and a new power-bus routing scheme are helping Motorola Inc. redefine the meaning of high density in CMOS gate arrays. No longer must arrays hog huge amounts of real estate or boast a gargantuan gate count to deliver a lot of usable logic.

That is the message behind a new family of triple-metal, 1-μm CMOS arrays from Motorola (see fig. 1). The new series promises up to 80% utilization of logic on channelless master slices ranging from less than 6,000 total gates to over 100,000. Comparable 100,000-gate arrays from other companies deliver at most 50,000 usable gates.

The ability to program gates with all three metal layers and the use of a flexible power-bus routing scheme, say managers at the Application-Specific Integrated-Circuit Division, result in more efficient use of logic compared to competing channelless architectures using the third level of metal only for power distribution. This makes for more efficient use of chip real estate. "High density in our book is not just a whole bunch of raw gates on a chip," says John Carey, product marketing manager at the Chandler, Ariz., division. Other recent sea-of-gate product introductions offer over 200,000 gates on larger die sizes [*Electronics,* Oct. 29, 1987, p. 55]. "High density in our definition is 1,097 μm^2 per gate, which comes about through the triple metal routing capabilities."

The new family sports typical internal gate speeds of 300 ps on fanouts of 2 pF at 25° C and 5 V. It also has a flexible bond-pad structure around the periphery that can accommodate either wire bonding or high-pin count tape-automated bonding. Wire bonding offers up to 300 input/output pads having a pitch of 5.6 mils. The current TAB will support a total of 460 ground, power, and I/O pads on a 4.0-mil pitch.

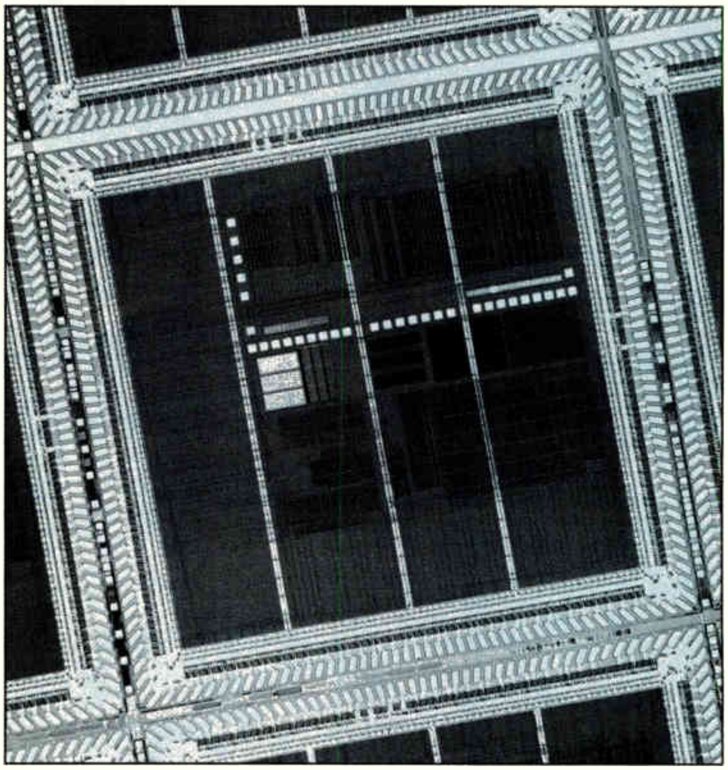
The new HDC family will consist of 10 master slices, spanning from 5,670 to 104,832 total gates. The total die size of the smallest HDC5000 array is 159 mils on a side, and the biggest family member measures only 483 mils on a side. Other channelless arrays in the 100,000-gate range are much larger—as much as 597 mils on a side.

Initially, Motorola's ASIC Division is offering three sea-of-gate master slices for 16,000-gate arrays. Joining those three family members in the first quarter of 1988 will be arrays for gate implementations totaling 5,000, 8,000, 12,000, 25,000, 45,000, 62,000, and 80,000 gates.

Motorola product managers estimate per-unit prices will fall in a range between $0.003 and $0.008 per usable gate, depending upon package selection and array density. Nonrecurring engineering charges of between $35,000 and $250,000 will be placed on array designs ranging from 16,000 to 100,000 gates. Motorola is launching the series with 12-to-14-week turnaround cycles, from the time customers sign off on a design to the shipment of the first prototypes. The turnaround times are expected to shorten during the coming year.

The HDC series, also dubbed the "Max" family, are made from a process Motorola calls TRIM, which not only stands for triple-level metal technology but also refers to the process's ability to cut the silicon real estate usually associated with large semicustom logic arrays.

A key feature of Motorola's HDC gate array



1. TRIPLE PLAY. Motorola's new Max family of high-density CMOS gate arrays features three metal layers and offers up to 100,000 total gates.

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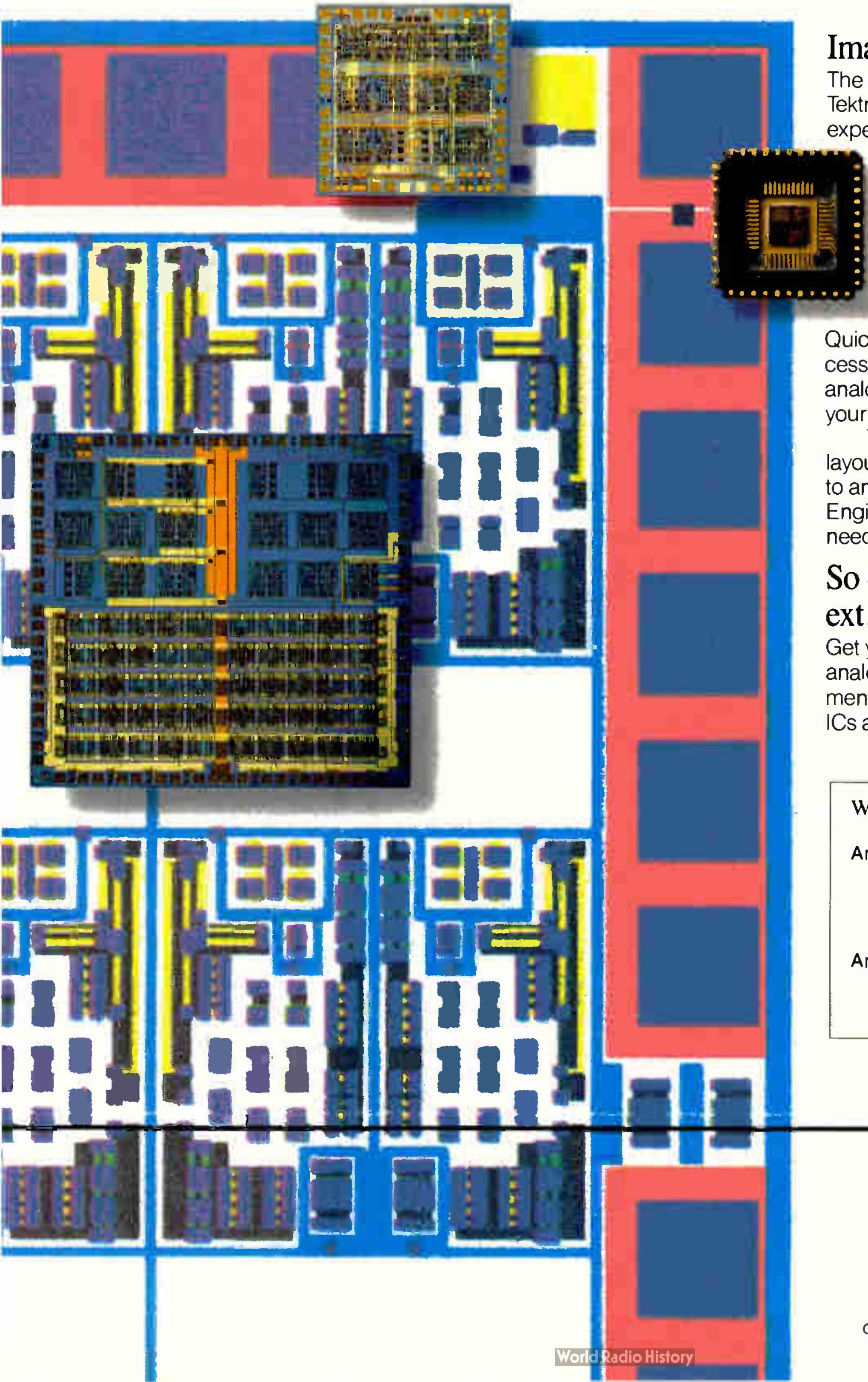

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TC511000 - 10	1 Mb x 1	CMOS	100 ns	Fast Page	18 pin
TC511000 - 12	1 Mb x 1	CMOS	120 ns	Fast Page	18 pin
TC511001 - 85	1 Mb x 1	CMOS	85 ns	Nibble	18 pin
TC511001 - 10	1 Mb x 1	CMOS	100 ns	Nibble	18 pin
TC511001 - 12	1 Mb x 1	CMOS	120 ns	Nibble	18 pin
TC511002 - 85	1 Mb x 1	CMOS	85 ns	Static Column	18 pin
TC511002 - 10	1 Mb x 1	CMOS	100 ns	Static Column	18 pin
TC511002 - 12	1 Mb x 1	CMOS	120 ns	Static Column	18 pin
TC514256 - 85	256K x 4	CMOS	85 ns	Fast Page	20 pin
TC514256 - 10	256K x 4	CMOS	100 ns	Fast Page	20 pin
TC514256 - 12	256K x 4	CMOS	120 ns	Fast Page	20 pin
TC514258 - 85	256K x 4	CMOS	85 ns	Static Column	20 pin
TC514258 - 10	256K x 4	CMOS	100 ns	Static Column	20 pin
TC514258 - 12	256K x 4	CMOS	120 ns	Static Column	20 pin

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TC55257L-10	32K x 8	CMOS	100 ns	100μA MAX	28 pin
TC55257AL-12	32K x 8	CMOS	120 ns	100μA MAX	28 pin
TC55257AL-85L	32K x 8	CMOS	85 ns	30μA MAX	28 pin
TC55257AL-10L	32K x 8	CMOS	100 ns	30μA MAX	28 pin
TC55257AL-12L	32K x 8	CMOS	120 ns	30μA MAX	28 pin

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NOW, A WAY TO DO ON-THE-SPOT CHECKS OF IC DESIGN CHANGES

SDA Systems' tools no longer need verify the entire design to check out one change

by Jonah McLeod

A powerful new version of SDA Systems' design-verification tools promises designers of full-custom integrated circuits capabilities they've never had before—capabilities that can cut significantly the time and effort spent on verification. Now designers can interact with the verification tools, adding changes or making corrections and then checking immediately to see if they work. They can also verify designs the same way that they build them—hierarchically, adding levels of complexity and verifying the design at that level, rather than waiting while the tools break each level down to its basic transistors and check the design at that elementary level.

Until now, checking a circuit layout to see that it observes the design rules of the process technology to be used for that circuit, and that it conforms with good design practice, was done mostly on large mainframe computers and was run in batch mode. The task is computation-intensive and time-consuming because the design must be reduced to elementary individual transistors to perform the analysis. Even the newer design-verification tools that can run on work stations evaluate the entire design for every change. Doing so is not only time-consuming, but precludes interaction—the designer cannot simply make one change to a design and check only the change, but must verify the whole design all over again.

The four tools in SDA Systems' kit include new versions of PD (for physical design) Check, PD Extract, and PD Compare. The upgraded tools allow the designer to extract a network description from his layout data base and compare it with the original schematic to detect any differences much more automatically than do other tools. The San Jose, Calif., company also has added a fourth, completely new tool, ERC, for electrical rules check. The tools are all tightly integrated, using a common data base called Framework [*Electronics*, June 25, 1987, p. 57].

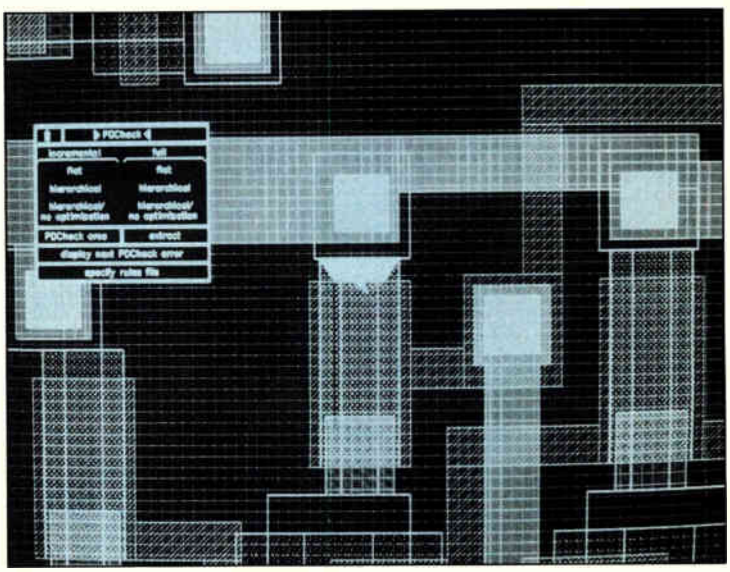
The revised PD Check offers capabilities not provided by competing tools. Using it, a designer can, for the first time, perform an incremental, hierarchical check of his layout.

That means he checks each step of the design as he gets to it. The system keeps track of changes between incremental checks, verifying only additions to the circuit rather than checking on the whole circuit. An hour of design work can be verified in a minute. "Not only is the check performed very quickly, but the designer catches his mistakes at the earliest stage in the process," says Dwight Couch, product marketing manager at SDA Systems. Checking the design as he goes saves the designer the typical two-month verification at the end of his design cycle.

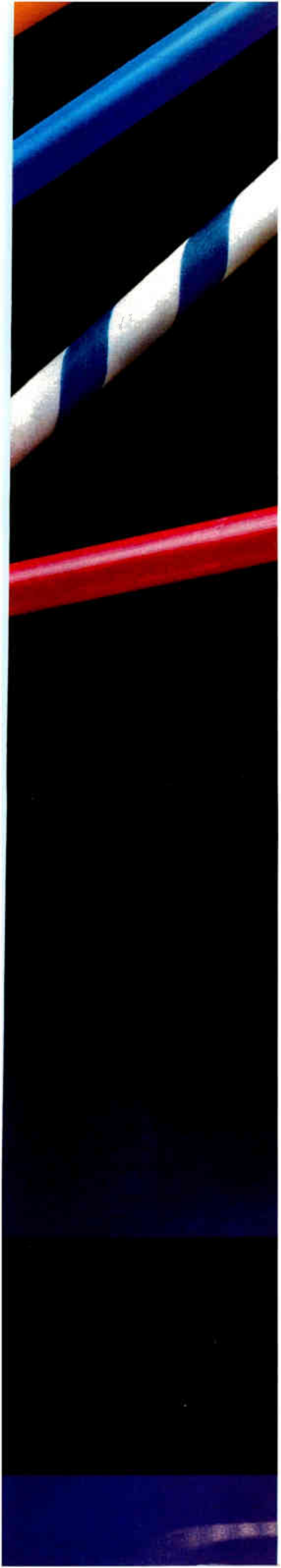
The hierarchical verification capability is a logical extension of the way designers work. "Designers are already using hierarchical design methods," says Couch. "They should also verify their designs hierarchically. It is just a much more efficient way to check a design." In practice, it means, for example, that once the tools verify a circuit—say a 4-bit counter—every occurrence of the counter thereafter in the design hierarchy need not be reverified. PD Check can also verify designs at the "flattened" or transistor level, if necessary.

"This tool currently provides the fastest throughput of any design-verification system currently available, even before this latest release," says Couch. And by using new algorithms, the speed of operation of the latest version has been doubled. In addition, the amount of disk space the program takes up has been cut in half, making the program much more efficient when running on a work station.

In operation, PD Check shows the designer, with a flashing indicator on his work-station



1. CHECK. The PD Checker tool allows fast hierarchical and incremental checking of complex circuits interactively.



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But with a system so advanced, the heart is only the start of it.

AT&T's WE 32201 Memory Management Unit (MMU) incorporates an unprecedented 4 Kbyte on-chip data cache, supports zero-wait-state virtual accesses at up to 30 MHz, and greatly reduces CPU overhead. This MMU has a variety of protection mechanisms to maintain system integrity. It is a 400,000-transistor testimonial to AT&T's technological leadership.

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Add to this a 32-bit DRAM Controller that supports 1 MEG DRAMs and a DMA Controller with a super-high transfer rate: 14 Mbytes/sec. memory to memory at 18 MHz.

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For more on how AT&T's WE 32200 Microprocessor chip set can help you bring top-line computer solutions to the multiuser/multitasking marketplace, call **1 800 372-CHIP.**

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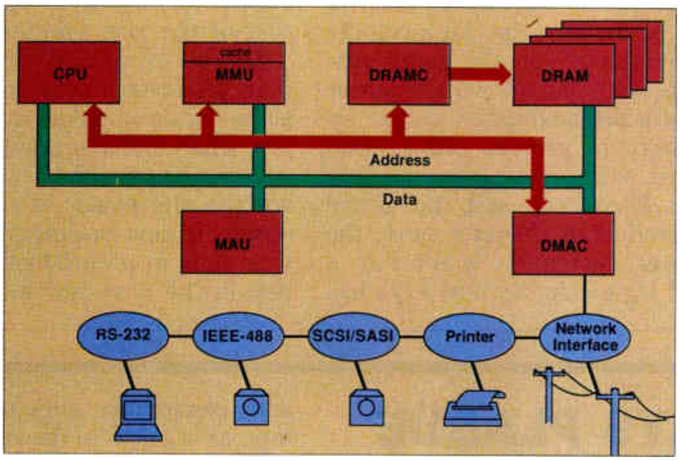

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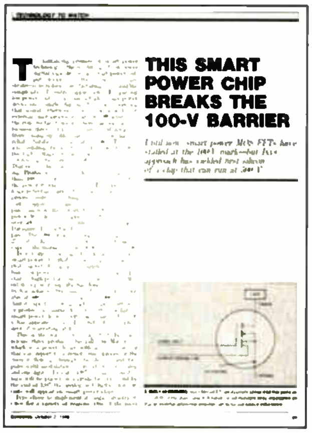
UPDATE: IXYS NIXES PLANS FOR SMART-POWER CHIPS

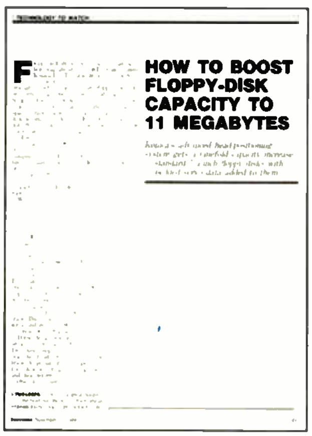

THIS SMART POWER CHIP BREAKS THE 100-V BARRIER

Last year, it looked as if Ixys Corp. would be the first chip maker to achieve smart-power capability—the combining of low-power logic devices and high-power output devices on the same chip substrate [*Electronics*, Oct. 2, 1986, p. 89]. The San Jose, Calif., company planned to put MirrorFET, its high-voltage power device, on the same substrate with one of two low-power pulse-width-modulator chips, resulting in greater integration and savings in board space. But Ixys ran into problems packaging MirrorFET, and the device has yet to go into production. What's more, the company now believes customers won't buy a combined power and logic chip. So now Ixys has put its smart-power technology plans on hold. Instead it will add additional logic to the MirrorFET: temperature- and current-sensing circuitry.

The two control logic devices, the IXMS150 analog current-mode pulse-width modulator and the IXDP610 digital pulse-width modulator, are already on the market and doing well, says Nathan Zommer, executive vice president and chief technical officer. But the MirrorFET amplifier has yet to roll off the production line. When it does, it will be sold separately, rather than on the same chip as one of the two pulse-width controllers. "We found that the market prefers to have power and logic devices on separate chips," is how Zommer puts it. The delay was one factor, he says, and another was the extra cost of the Ixys single-chip solution.

MirrorFET, named for the current-sensing lead that produces a current drain 1/1000th of the actual drain current, ran into a packaging problem while under production. "We found that the leads on the TO-25 package could not handle the voltage and power of the device and we had to design a new package," Zommer says. The device, now in preproduction, should be in production in the next few months. *–Jonah McLeod*

UPDATE: DELAYS PLAGUE KONICA'S BIG FLOPPY DISK


HOW TO BOOST FLOPPY-DISK CAPACITY TO 11 MEGABYTES

A year after introducing its KT-510 5¼-in. floppy-disk drive [*Electronics*, Nov. 13, 1986, p. 81], Konica Technology Inc. is finally getting it into large-volume production. The drive stores 11 Mbytes on a conventional IBM Corp. PC AT floppy disk, nine times the normal capacity, but now events have overtaken it.

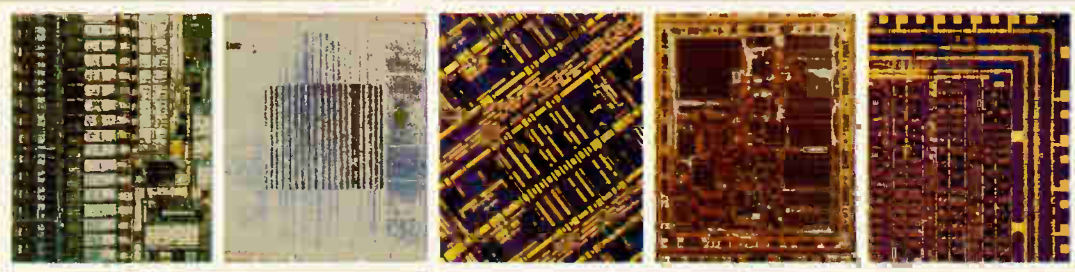
While Tokyo parent company Konica Corp.'s engineers were unraveling the production problems faced by its Sunnyvale, Calif., subsidiary, IBM introduced its successor to the PC, the PS/2 system—which uses a 3½-in. floppy disk. IBM's use of the smaller disks makes it unlikely that makers of PC-compatible systems will incorporate the KT-510 in their systems, which is what Konica was hoping for. And Brier Technology Inc. is introducing a 20-megabyte 3-½-in. floppy (see p. 154).

But Konica Technology marketing manager Maurice Webb is hopeful that a market exists for the disk drive as an add-on to the IBM PC AT and compatible computer products, replacing tape as a back-up device. Also, he says that the Unix-based work-station and supermicro computer markets are showing interest in the KT-510. These users are looking at the high-capacity floppy drive instead of tape as a means of transferring programs and data between systems.

Webb says that the major original-equipment manufacturers have evaluation units of the drive. "We have a backlog of orders for production units from the small- to medium-size system integrators and OEMs," he says. "But major OEMs have been waiting to see that we solved all the manufacturing problems before they committed themselves."

He says that the monthly production rate, which hovered until recently at around 100, is up to 1,000. "Production should reach 2,000 a month in November, 5,000 a month in December, and finally beyond 10,000 a month starting next year," Webb predicts.

The company is already looking to upgrade the KT-510. It is considering a 20-Mbyte version as well as a 10-Mbyte 3½-in. floppy. Both units would use media with slightly higher coercivity than the standard 600-oersted media used on the IBM PC AT class. The standard media allow the KT-510 to store 20,000 bits per inch at 480 tracks per inch. By using higher-coercivity media, the higher-capacity unit would increase track density only slightly, while hiking bit density to approximately 36,000 bpi. *–Jonah McLeod*



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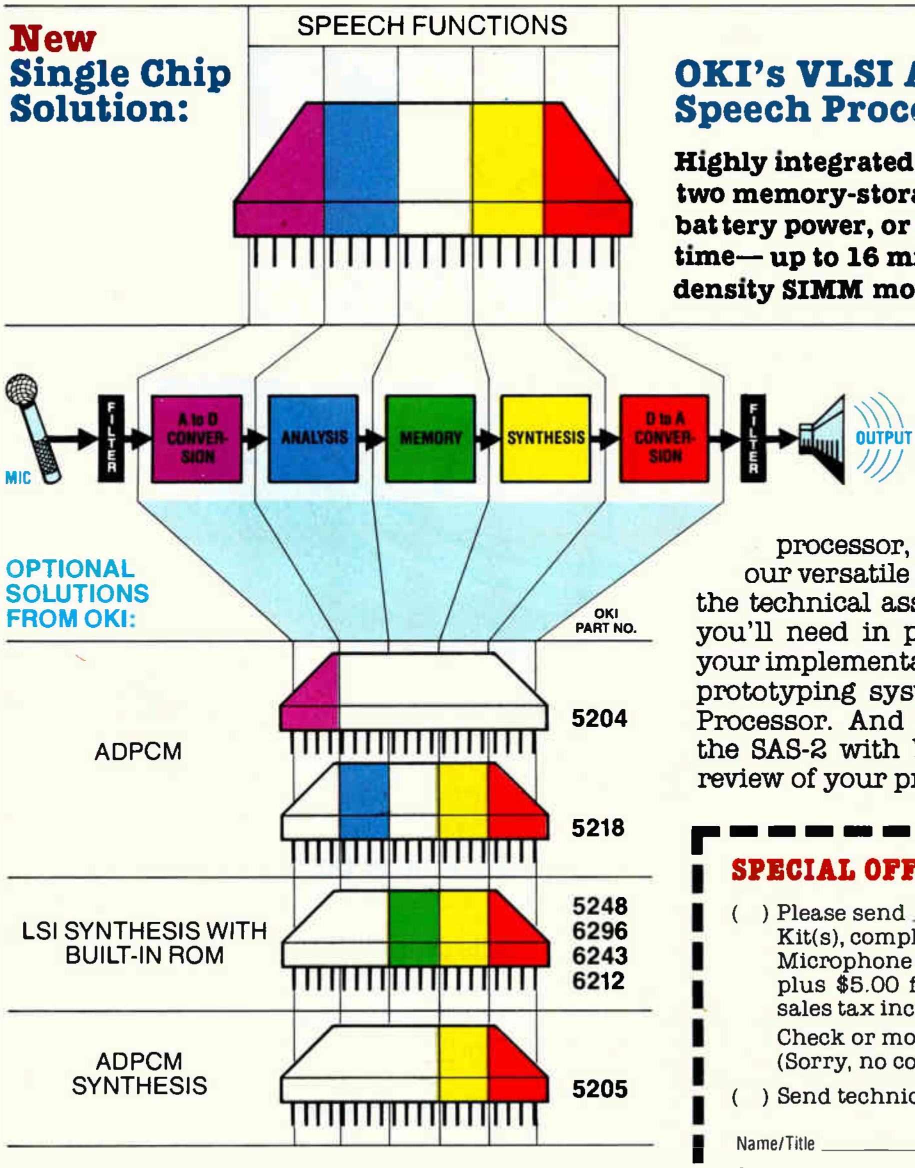

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MILITARY/AEROSPACE NEWSLETTER

TASK FORCE SLAMS DOD FOR BUNGLING MILITARY SOFTWARE EFFORTS

The Defense Department's efforts in software development are disjointed, uncoordinated, and lack support, charges the Defense Science Board's Task Force on Military Software. The task force reports it "is convinced that today's major problems with military software are not technical problems, but management problems." It lambastes the DOD for having "not provided the vital leadership needed" in Stars, the Software Technology for Adaptable Reliable Systems. It complains that Ada, the high-level programming language the DOD is pushing to make a standard for all military systems, "has been overpromised." It warns that "the Strategic Defense Initiative has a monumental software problem" and that "no program to address the software problem is evident." To solve the management problem, the task force urges the DOD to bring together Stars, Ada, and the Software Engineering Institute under the Air Force Electronic Systems Division. It also wants representatives from the three programs and from the Defense Advanced Research Projects Agency's Strategic Computing Initiative to produce a "one-time joint plan to demonstrate a coordinated DOD Software Technology Program." What does the DOD have to say? Not much just yet. Officials at the Ada Program office did not respond to calls, and a Darpa spokesman would say only that the agency "has no plans to implement any of the changes that the report recommends" at this point but will take them under consideration. □

EVEN VHSIC FAILURES HAVE TURNED OUT WELL, MAYNARD SAYS

The Defense Department's Very High-Speed Integrated Circuits program is a success overall, says E. D. "Sonny" Maynard, VHSIC program director and director of computer and electronic technologies at the DOD. Maynard says a number of VHSIC nightmares have turned, overnight, into success stories. Texas Instruments Inc., for example, "had delays with its bipolar process and fell years behind," he says. "Now TI is a big winner, getting its 1750A VHSIC chip into the Advanced Tactical Fighter program." Honeywell Inc. "had some difficulty getting its CMOS process on line, but no loss," he adds, pointing to Honeywell's success as a chip supplier to supercomputer maker ETA Systems Inc., of Minneapolis. Finally, Maynard says, "perhaps the most used VHSIC chips of all" are gate arrays and memory parts from Westinghouse Corp.—even though Westinghouse's other parts never made it into a single system. "My assessment is that the total effort has more than achieved the goals that it started with," Maynard says, disputing criticism that the program has taken too long to accomplish too little. "We needed to get over the idea that we could just use commercial microprocessors." But as Phase 2 prototype chips begin to arrive, Maynard has another worry: "one of the trickiest parts of any program is bringing it to conclusion." □

U. S. AND FIVE NATO ALLIES WILL DEVELOP NEW ANTIAIRCRAFT WEAPONS

The U. S. and five allies will explore ways to improve shipborne antiaircraft weapons under an agreement to develop future air defenses for ships belonging to North Atlantic Treaty Organization members. Canada, the Netherlands, Spain, the UK, and West Germany joined the U. S. late last month in agreeing to enter the exploratory phase of the NATO Anti-Air Warfare Weapon System Program. The program is aimed at defending NATO ships against airborne threats, particularly short-range ones such as that posed by anti-ship missiles. Antiaircraft weapons developed under the NATO program will have "direct application to the NATO frigate replacement" program, says a U. S. Navy spokesman, and will be used to retrofit existing ships as well. The program will be managed by an international program office that will be based in Washington. □

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PROBING THE NEWS

HAS SILICON VALLEY LOST ITS ZING?

NO, BUT IT'S CHANGING: CHIP COMPANIES NO LONGER LEAD ITS GROWTH

by Jeremy Young

It's showtime in San Francisco, and no one knows it better than the denizens of the sprawling technology center a few miles to the southeast. It's Silicon Valley that has given the San Francisco editions of Wescon their heft, a good bit of their sparkle, and most of their showgoers. But this year's show, from Nov. 17 to 19, may be a bit subdued—the Valley has been taking some lumps lately.

Are the days of glory past for Silicon Valley, where the integrated-circuit business so central to the high technology industries first blossomed, and then boomed? After the long semiconductor market slump of 1985 and 1986, after the chilling blast from the financial markets last month, will the Valley ever gestate strong new technology startups again? Or is its vitality gone?

Media reports of late would have it so, but rumors of the Valley's death are premature. Tremendous innovative and entrepreneurial energy still drives the region. No one would deny the fact that there are problems in the Valley, probably foremost among them the struggles of the U.S. semiconductor industry. And in recent years past, so many companies were being started so rapidly that inevitably, perhaps, a number got launched that were too weak, in terms of concept, management, or market potential, so some weeding out was required, adding to the bad news that has dogged Silicon Valley of late.

But bad press has not stopped the Valley's growth. Strong expansion continues, although not at the breakneck pace of the last decade, and not in the same sectors of the industry. The chip sector may never reach the prominence it once held, but other types of business are doing very well (see figure). Computer businesses, for example, systems, peripherals, and software look good. So does instrument manufacturing in the areas of medicine and biotechnology.

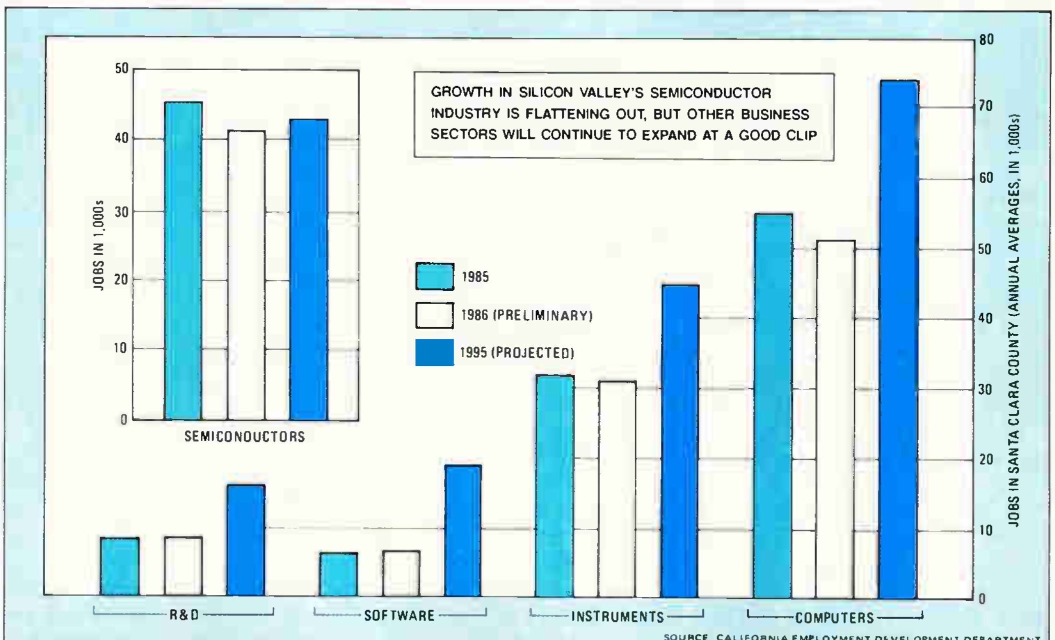
Industry observers expect much of the growth to come from young companies, startups, and small companies growing to successful midsize organizations. Such companies thrive in Silicon Valley, most say, because of the kind of people who live there: intelligent, skilled, highly motivated people, many of whom came there to be among their peers and to enjoy the physical surroundings of northern California.

And though October's stock-market debacle has left the question of available capital very much up in the air for startups, many cite the presence of active and experienced venture capitalists in the valley as one of its prime assets. Smart venture-capital people also link their fledgling companies with other parts of the Valley's wide network of support services. This infrastructure makes Silicon Valley a fertile garden bed for small high-tech companies that may well have no equal, anywhere.

Even real estate has its advantages in Silicon Valley. The cost of housing is high, but in the last two or three years, office and plant space has been plentiful, to the point where new companies could find a place to set up without laying out much cash, if any at all.

HIGH-TECH SEEDS. Nearby universities and research institutions also contribute to the Valley's technological health and diversity. Graduates from the engineering schools seed the Valley with young talent, and technology developed in academic and government-backed research labs often provides the foundation for new companies building new kinds of high-tech products.

All of these factors add up to a technological critical mass, a hot reactor of ideas and businesses that, when examined, shows no sign of growing cold. The Valley is changing, and its growth is likely to be more paced in the coming years, but it is not dying. Founders of several recently started companies, when asked, unanimously recommend



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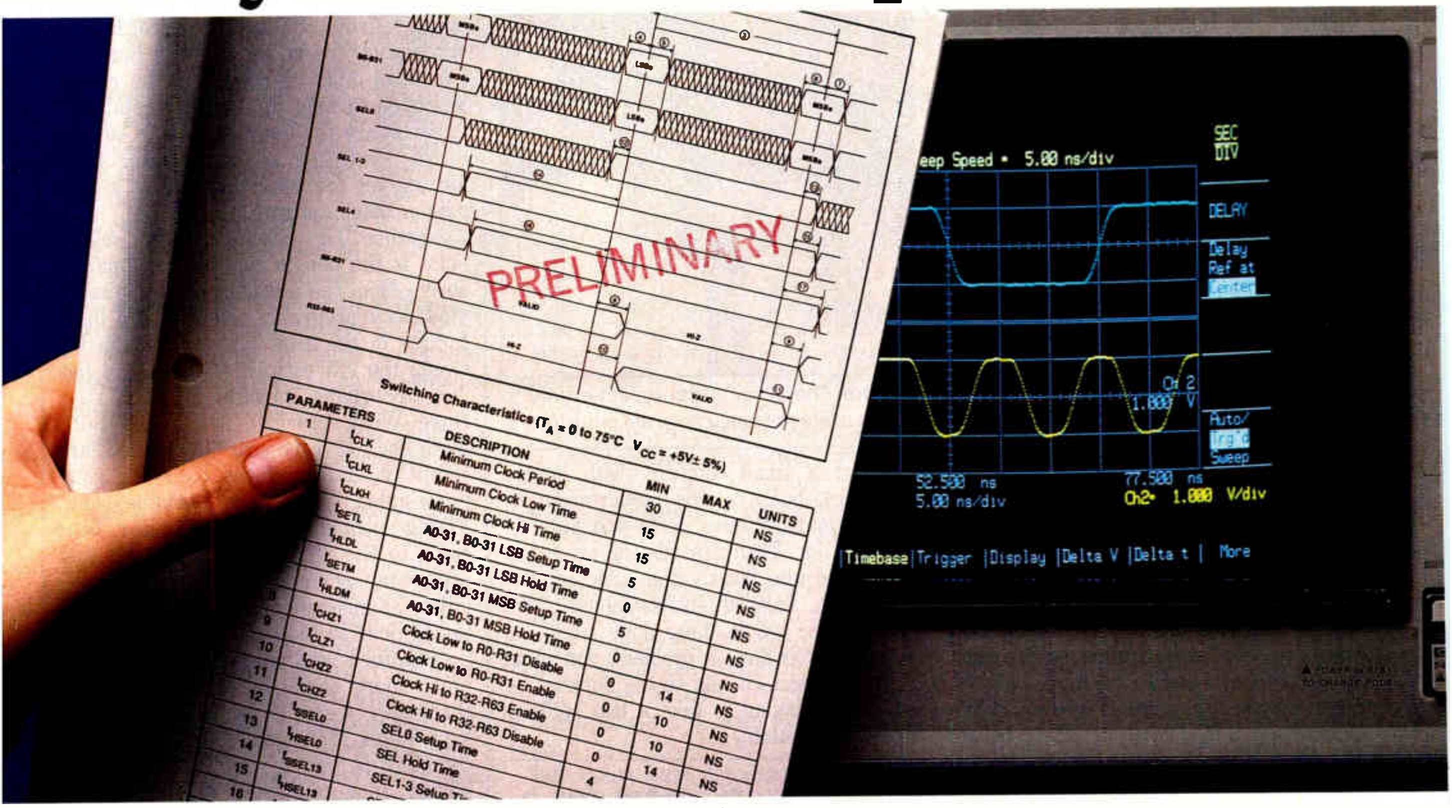

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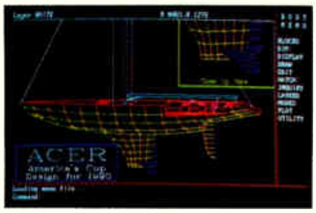

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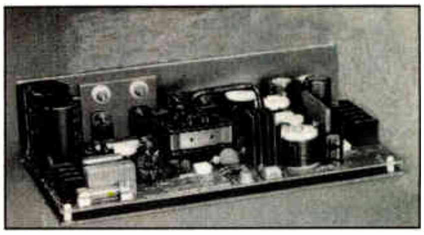

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– Tobias Naegele

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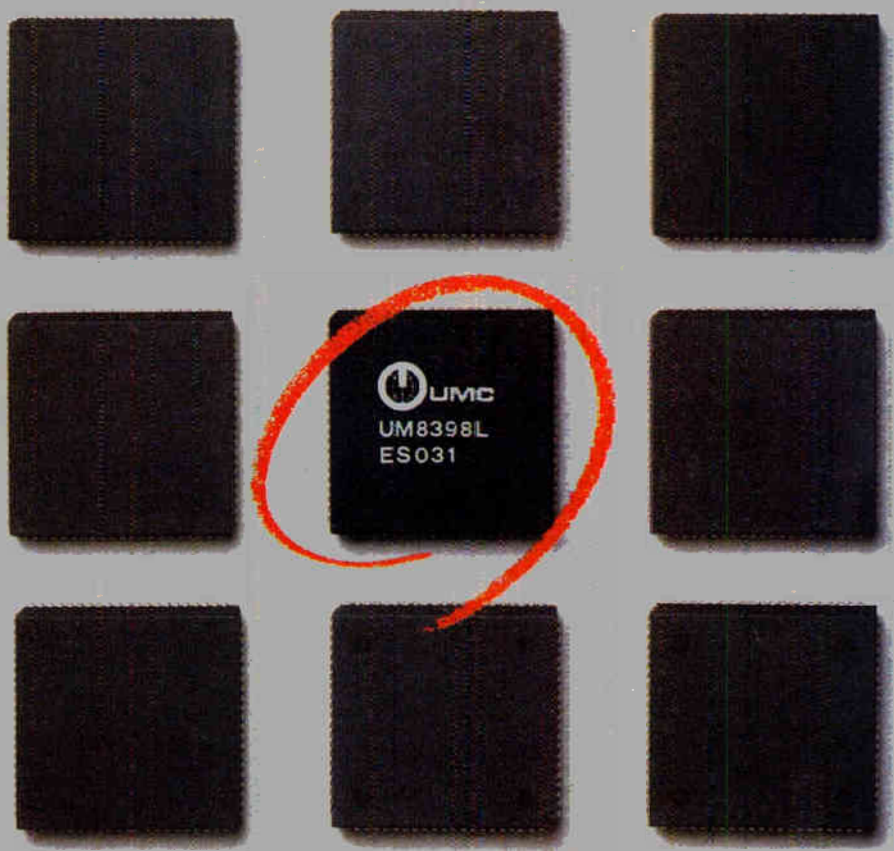

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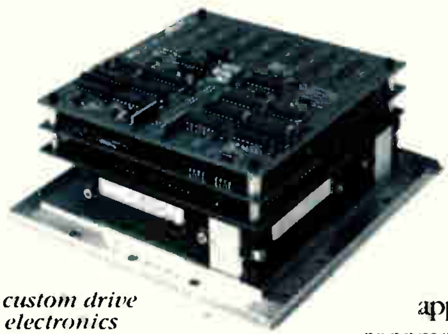

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SIERRACIN/MAGNEDYNE's Design Guide helps you select the optimal configuration for your needs. Our Design Guide provides a simple step-by-step method to describe your application, and only when we understand *your* needs will we make recommendations.

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Once again, Compaq raises the standard of performance for personal computers.

This time by a factor of two…

Introducing the two on earth

The new COMPAQ DESKPRO 386/20™

Last year, we introduced the COMPAQ DESKPRO 386,™ the most advanced personal computer in the world. Now the world has two new benchmarks from the leader in high-performance personal computing. The new 20-MHz COMPAQ DESKPRO 386/20 and the 20-lb., 20-MHz COMPAQ PORTABLE 386 deliver system performance that can rival minicomputers.* Plus they introduce advanced capabilities, without obsoleting your investment in software, hardware and training.

Our new computers employ an industry-standard 20-MHz 80386 microprocessor and sophisticated 32-bit architecture. But to make these two of the world's fastest PC's, we did more than just increase the clock speed.

For instance, both are built around a concurrent bus architecture. Two buses—one for memory and one for peripherals—eliminate information bottlenecks, allowing each component

It simply works better.

most powerful PC's and off.

and the new 20-MHz COMPAQ PORTABLE 386™

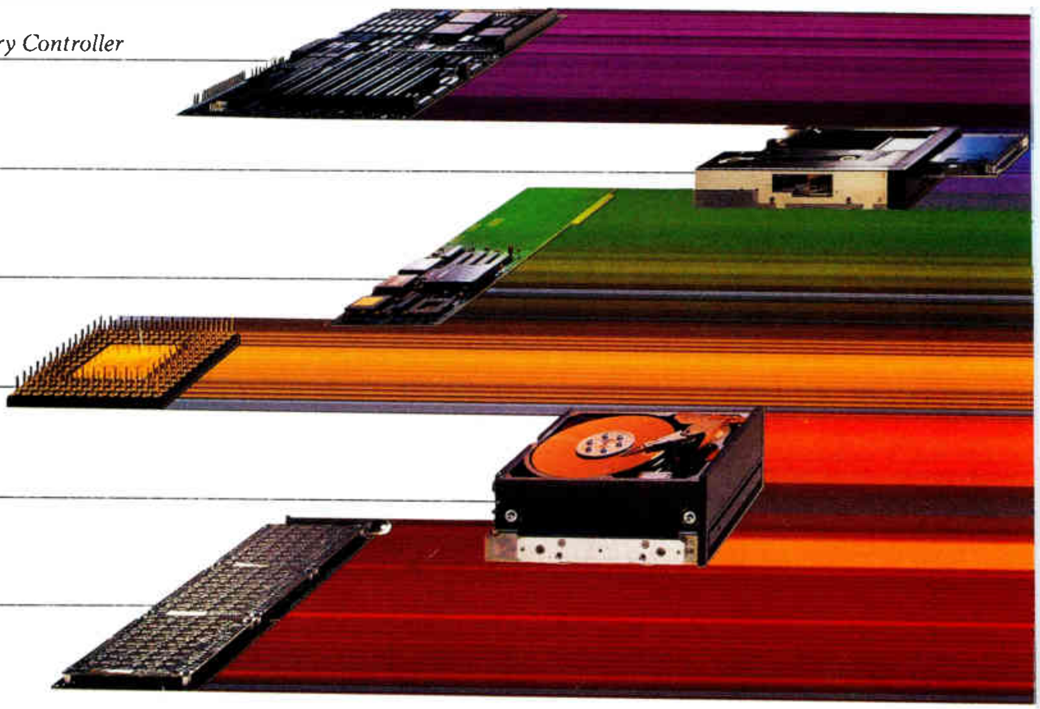
to run at its maximum speed. Together, they insure the highest system performance without sacrificing compatibility with industry-standard peripherals.

Both computers offer disk caching. Both offer the most memory and storage within their classes. Both let you run software being written to take advantage of 386 technology. And both run new MS-DOS®/BASIC Version 3.3 as published by Compaq. With it, our new portable and our new desktop can break the 32-megabyte limit on file sizes that handcuffs other PC's, allowing you to build files up to the size of your entire fixed disk drive.

And from now until December 31, 1987, both computers come with a free package of new Microsoft® Windows/386 Presentation Manager. It provides multitasking and switching capabilities with today's DOS applications to make you more productive. But that's just the beginning. To find out more, read on.

COMPAQ®

The question wasn't but how to get the



The most powerful personal computer in the world

The COMPAQ DESKPRO 386/20 is an impressive 50% faster than 16-MHz 386-based personal computers. Even more impressive is the fact that it's up to 25% faster than other 20-MHz 386's. That's because the processor is just one small part of how the COMPAQ DESKPRO 386/20 outperforms every other PC in the world today and even many minicomputers.

The big reason is the new COMPAQ Flexible Advanced Systems Architecture, which optimizes overall system throughput while maintaining full compatibility with industry-standard peripherals. It does this by combining an advanced memory caching scheme with memory and peripheral buses that operate concurrently.

Complementing the speed of the microprocessor is the new advanced 20-MHz Intel® 82385 Cache Memory Controller. Like an efficient secretary that keeps frequently used information close at hand, it allows the microprocessor to operate at 0-wait states 95% of the time.

While one bus handles these high-speed operations, another *simultaneously* handles periph-

It simply works better.

how to get to 20 MHz, most out of 20 MHz.

erals operating at the industry-standard 8 MHz.

This flexible approach allows you to dramatically increase system throughput while preserving your investment in monitors, disk drives, and expansion boards. It can also accommodate today's and tomorrow's most advanced peripherals without constraining their performance.

Take options like our new Weitek™ Coprocessor Board. Never before offered in a PC, it can increase the speed of calculation-intensive, engineering and scientific applications by a factor of six, giving the COMPAQ DESKPRO 386/20 the performance of a dedicated engineering workstation at a fraction of the cost.

Compaq also provides 130- and 300-Megabyte Fixed Disk Drives with some of the industry's fastest access times. And when used with disk caching software, they represent the highest-performance storage subsystems available.

As for memory, Compaq offers 32-bit high-speed RAM. One full megabyte comes standard and is expandable to 16 megabytes without using an expansion slot. Plus, we included the COMPAQ Expanded Memory Manager. It supports the LIM standard so your software can break the 640-Kbyte barrier even before OS/2™ is released.

As tasks become more complex and users demand more advanced capabilities, Compaq responds by raising the standard of performance in personal computing.

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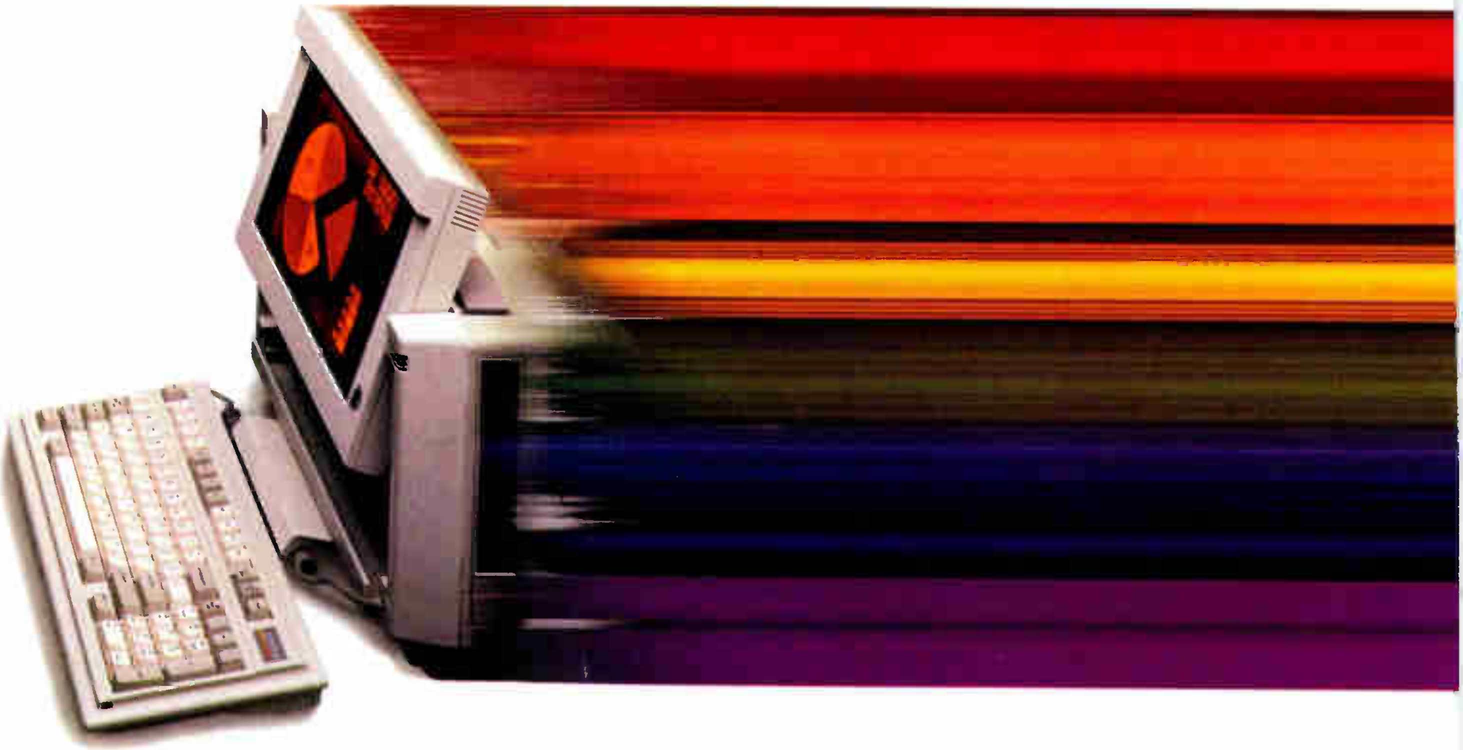
DESKPRO 386/20™

Everyone expected Compaq
But no one



?ound for pound, it is the /orld's most powerful computer

'ompaq has long been recog-
ized as the world leader in both
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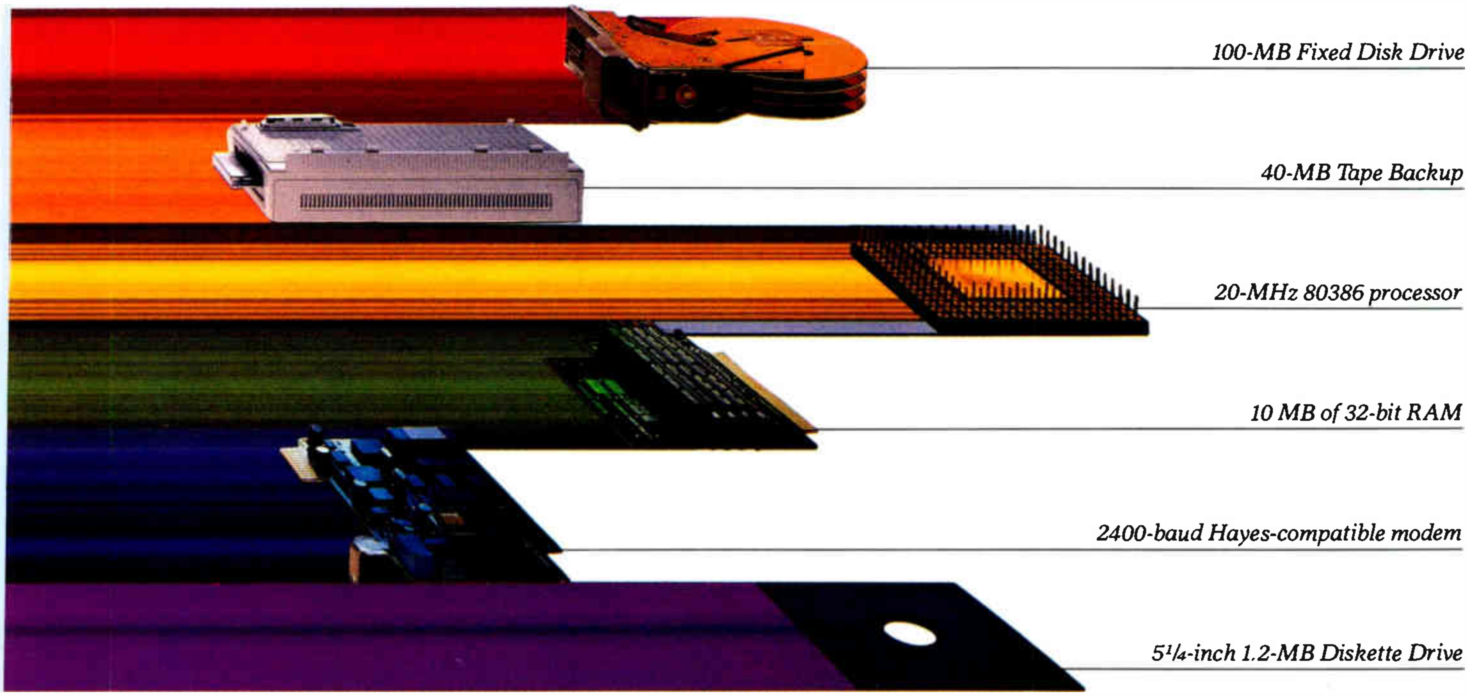
omputing. So it isn't surprising
hat we would combine the two.
But no one expected the new
'OMPAQ PORTABLE 386 to run
t 20 MHz. And no one even dreamed that it would offer 100 megabytes of storage, disk caching, and much, much more.

Our newest 20-lb. portable computer goes far beyond an 80386 microprocessor with a handle. It's not just the most advanced portable in the world. Pound for pound, it's the world's most powerful computer. Period.

Like the recent COMPAQ PORTABLE III,™ which changed the shape of full-function portable computing, the COMPAQ PORTABLE 386 makes no compromises. It offers more speed, memory, storage and features than any other portable PC. It runs your current software up to 25% faster than 16-MHz 386 PC's. Beyond that, its performance in calculation-intensive

t simply works better.

o introduce a 386 portable PC. xpected all this.



applications is increased even more when you add an optional 20-MHz 80387 coprocessor.

Memory? Get one megabyte of 32-bit, high-speed RAM standard or go as high as 10 MB internally. And like all of the COMPAQ 386-based PC's, it features the COMPAQ Expanded Memory Manager.

With our high-performance 100-megabyte internal fixed disk drive, you can actually fit 500 lbs. of data-filled pages into a 20-lb. PC, unsurpassed storage for a portable. If that's too much for you, we also offer a 40-megabyte model.

We've become famous for building desktop computer capabilities into our portables without leaving anything out. The COMPAQ PORTABLE 386 is more proof. It has a high-resolution, 640 × 400, 10-inch plasma display; a full-size, portable enhanced keyboard; two industry-standard expansion slots in a lightweight, optional plug-on unit; a choice between an optional 2400- or 1200-baud Hayes®-compatible modem; a full-size 5¼-inch 1.2-MB diskette drive; even an optional 40-MB tape backup.

These features, combined with the ultimate in portable performance, make the COMPAQ PORTABLE 386 the *biggest* PC this *small*.

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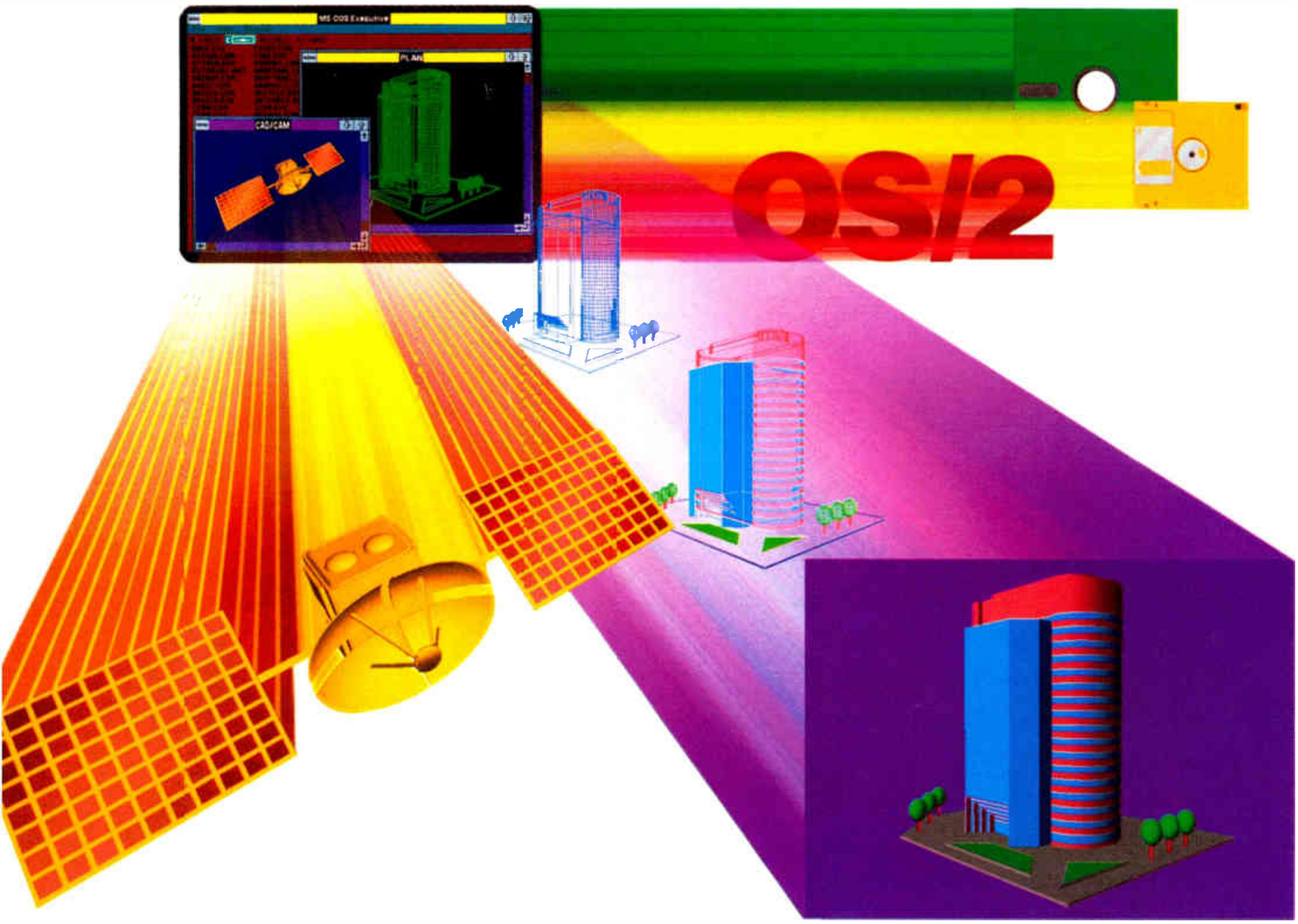
PORTABLE 386™

Compaq moves you ahead without leaving you behind.



Compaq offers the most complete line of high-performance 386 solutions. They all run industry-standard software and hardware, protecting the investments you've already made.

At the same time you won't be left behind when other technologies become important. Multitask with existing applications using Microsoft Windows/386 Presentation Manager. Add VGA graphics if you wish. Run OS/2 when it's available. And now 3½-inch drives are even an option for our desktops.

We optimize the most advanced technology while maintaining compatibility with the past, present and future. This makes COMPAQ PC's a wise decision for serious business users. Because at Compaq, we don't burn bridges, we build them.

See the COMPAQ DESKPRO 386/20 and COMPAQ PORTABLE 386 at an Authorized COMPAQ Computer Dealer. *And from now through December 31, 1987, get Microsoft Windows/386 Presentation Manager free when you buy a 386-based COMPAQ computer.* For more information, call 1-800-231-0900, Operator 40. In Canada, call 416-733-7876, Operator 40.

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Recent Ministry of International Trade and Industry guidelines and the rising value of the yen have created a $124 billion market for U.S.-manufactured electronic products, a market the likes of which U.S. electronics manufacturers have never seen.

In fact, Japan's commitment to the development of supercomputers, 1-megabit DRAM (dynamic random access memory) chips, DAT (digital audio tape) recorders, and other advanced equipment, has the demand for electronic devices, computers, and measuring instruments at an all-time high.

A $124,000,000,000 market in Japan for U.S.-manufactured electronics. And the way to cash in.

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Indeed, for a piece of Japan's $124 billion electronics market, a piece in **NIKKEI ELECTRONICS** is all the U.S. electronics manufacturer requires. That and a good product is all it takes to cash in.

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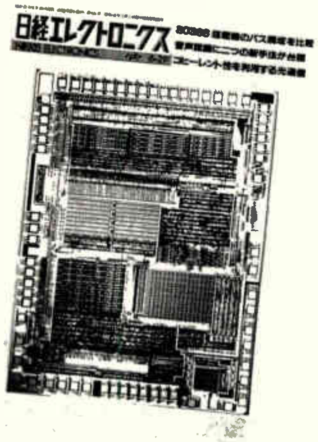

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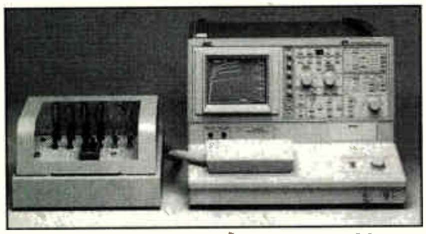

An internal bubble memory holds up to 16 front-panel setups that can be recalled by pressing a button. An industry-standard GPIB interface gives it connectivity to other test instruments.

Available now, the 371 costs $19,450.

Tektronix Inc., Marketing Communications Dept., P.O. Box 1700, Beaverton, Ore. 97075.

Phone (800) 547-1512 [Circle 385]

SCHEMATIC SOFTWARE DOES ANALOG, DIGITAL

Intelligent Applications USA has introduced Synergist, a diagnostic and schematic capture software program that can check out mixed analog and digital circuits from system level or board level down to individual components.

Synergist now runs on the Symbolics LISP machine, but the software will be adapted to the Apollo, Sun, and VAX work stations within the next year.

Available now, the software license for Synergist costs $10,000, and software support is priced at $1,500 a year.

Intelligent Applications USA, 9841 Broken Land Pkwy., Suite 206, Columbia, Md. 21046.

Phone (301) 381-6360 [Circle 387]

TOOLKIT HELPS DATA CAPTURE

The Helios Toolbox software package from John Fluke Manufacturing Co. saves engineers the time of writing custom software for Fluke's Helios-I data-acquisition and control computer.

Written in Microsoft Corp.'s QuickBasic, the Helios Toolbox assists in gathering real-time data for parameters such as temperature, pressure, and flow rates. It runs on IBM Corp. Personal Computers AT, XT, and compatibles. Data can be scanned and logged using simple one-line statements, and analysis is speeded by automatically creating spreadsheets compatible with Lotus Development Corp.'s 1 2 3.

Available now, the Helios Toolbox software costs $295.

John Fluke Mfg. Co., P.O. Box C9090, Everett, Wash. 98206.

Phone (800) 426-0361 [Circle 388]

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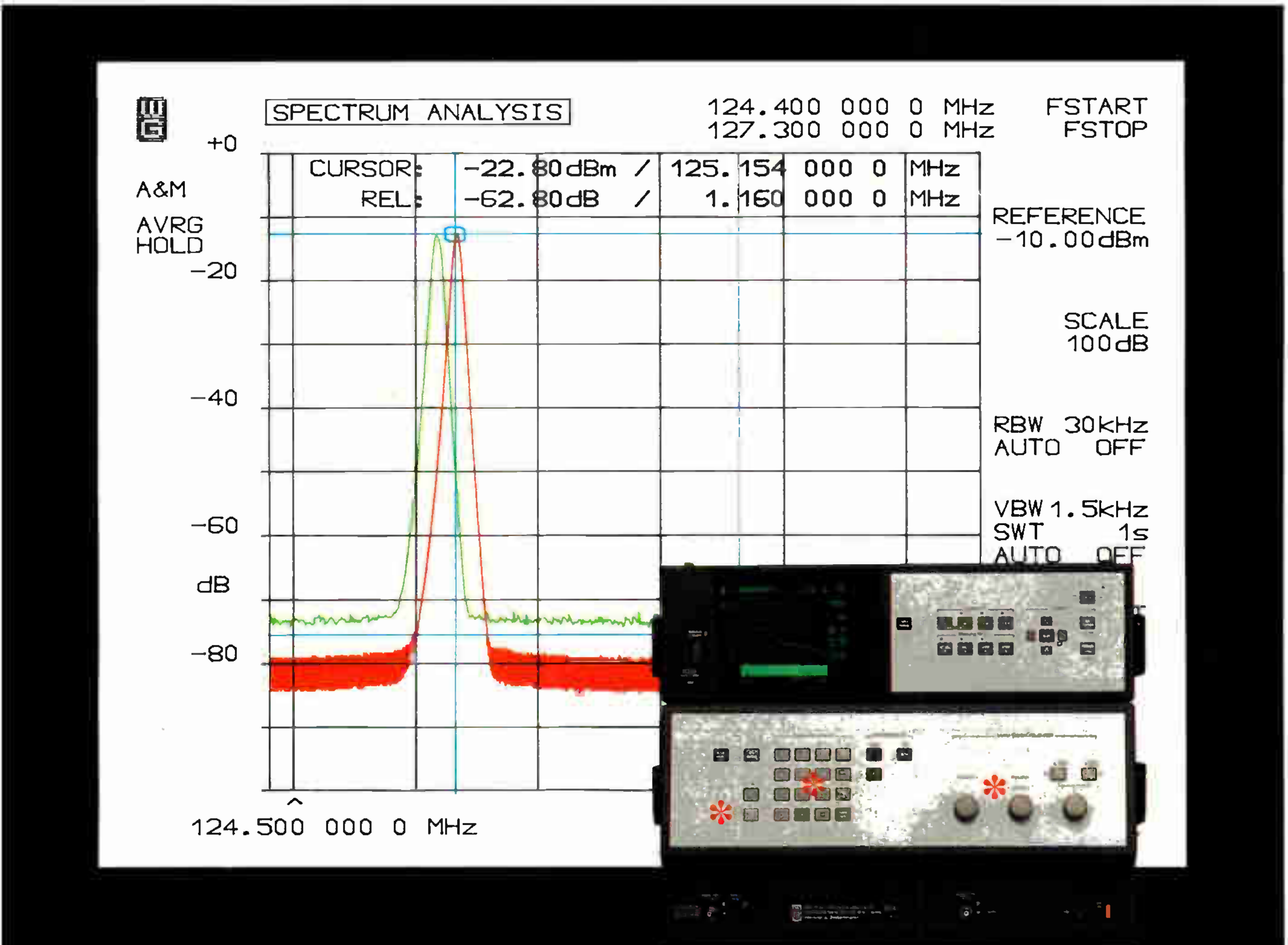

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DUAL-SPEED LAPTOP WEIGHS 10 LBS.

The Snap 1+1 modular laptop computer from Datavue Corp. offers switchable clock speeds of 9.5 and 4.77 MHz and a 20-Mbyte internal hard disk drive but weighs less than 10 lbs.

The computer's front module contains the keyboard, screen, and input/output ports as well as a battery and 512 Kbytes of memory. The rear module contains the disk drives, 640 Kbytes of memory, a battery, and an expansion slot.

The front and rear modules can be separated to make portability easier.

Available now, the Snap 1+1 laptop costs $2,295.

Datavue Corp., One Meca Way, Norcross, Ga. 30093.
Phone (404) 564-5555 [Circle 354]

VISION COMPUTER RUNS ON 80386

Intelledex Inc.'s Intellevue 386 Vision Computer runs up to 20 times faster than software-based competitors thanks to a 16-MHz Intel Corp. 80386 processor.

For an additional performance boost, the board-level vision system also incorporates an Intel 80387 math coprocessor and zero-wait-state memory. The system executes pattern matching independent of linear or nonlinear changes in light intensity and contrast.

It also has a windowing function in which six image buffers can be viewed as a contiguous image. Source and target windows are definable across the boundaries of the individual buffers.

Other functions include nonlinear array processing, binary morphology, edge-vector transforms, and connectivity analysis.

Four camera ports are provided with standard RS-170 camera interfaces that allow users to select from a number of camera manufacturers. A calibration system automatically compensates for nonorthogonal cameras.

Available now, the single-layer board costs $11,900 with delivery in 60 days.

Intelledex Inc., 4575 SW. Research Way, Corvallis, Ore. 97333.
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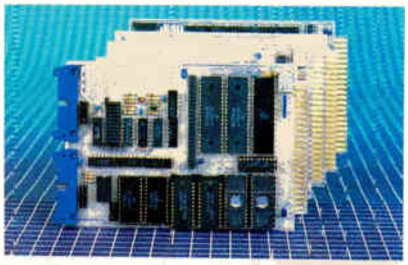

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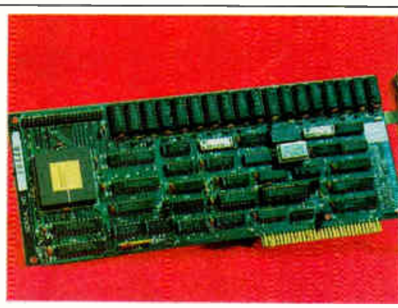

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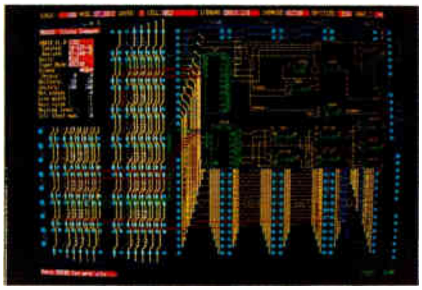

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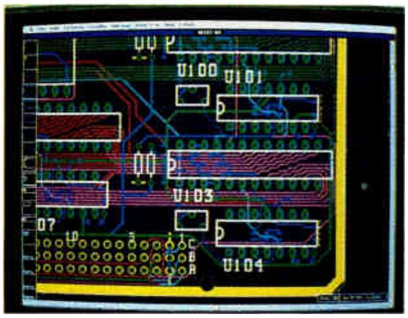

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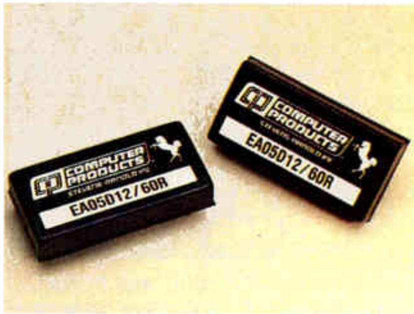

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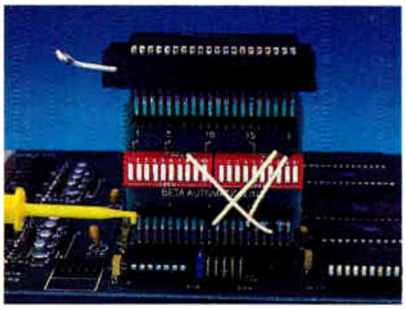

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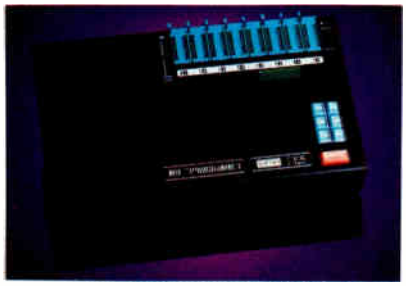

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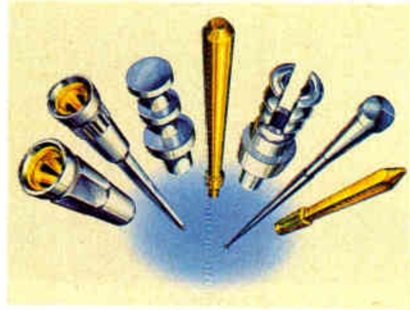

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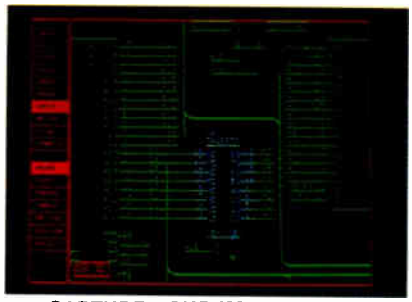

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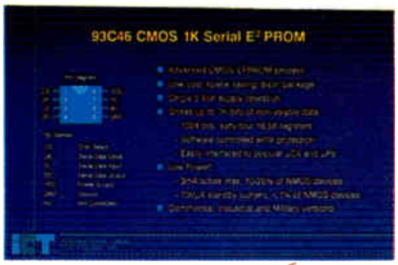

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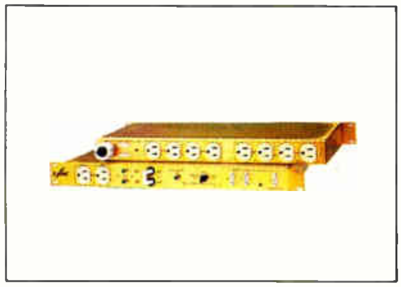

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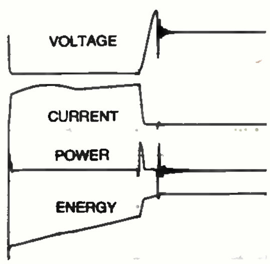

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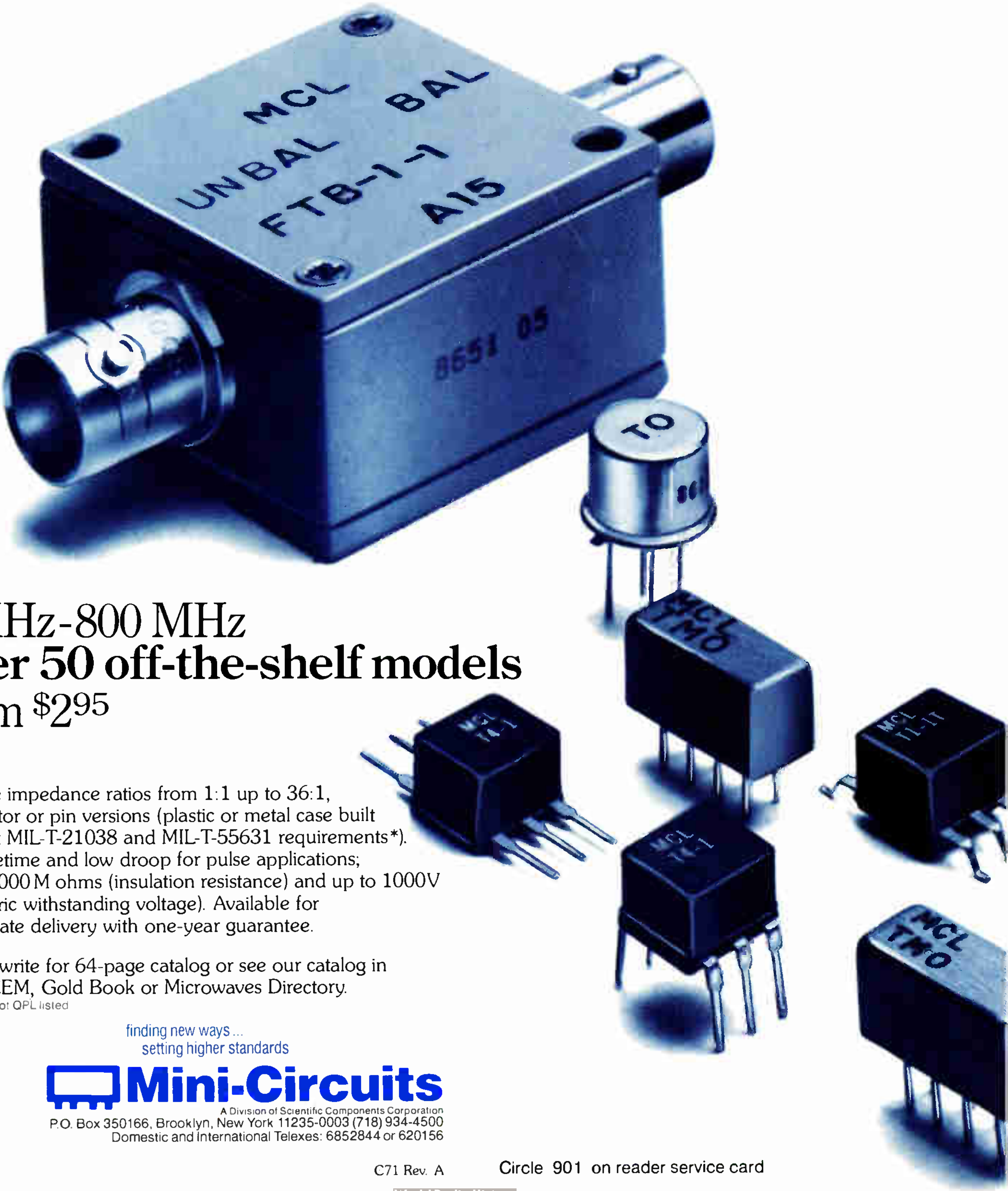

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